

Semiconductor Databook 1984-85

DB-300



UNITRODE

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INTRODUCTION

Unitrode is recognized today as a world-wide leader in the design, manufacture and marketing of electronic components. From its inception more than twenty-two years ago, Unitrode has earned and maintained a reputation of setting the highest standards of reliability and performance. Excellence was first established with a unique packaging concept for axial-leaded rectifiers and zeners for the military market. This fused-in-glass product is still unsurpassed in its reliability and performance.

Unitrode's products are designed to meet the demands of many markets including:

- Data Processing
- Military
- Telecommunications
- Industrial Controls
- Instrumentation

Today, Unitrode offers a broad line of high quality, high performance electronic components, including:

- Power Transistors and Darlingtons
- Power Hybrid Circuits and Modules
- Power Rectifiers
- Rectifier Assemblies
- Power Zeners and Transient Voltage Suppressors
- Thyristors
- Switching and General Purpose Diodes
- PIN Diodes
- Monolithic Ceramic Capacitors
- Linear Integrated Circuits

We are also a leading manufacturer of data acquisition and conversion products through our Micro Networks Division in Worcester, Massachusetts and miniaturized power supply modules through our Powercube subsidiary in Billerica, Massachusetts. Two recent acquisitions joined our ranks of product offering; US Microtek Components of Sun Valley, California, a manufacturer of monolithic ceramic capacitors and (EMI) filters adding to our leadership position in the ceramic capacitor business and, Power General Corporation of Canton, Massachusetts, a manufacturer of multiple output switching power supplies and DC-DC converters.

This DATABOOK lists today's broadest line of discrete semiconductors, linear integrated circuits and capacitors.

We take pride in our products, and know they will add more value to your company's products.

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10-5	2N1872A, J	1.25A@100°C 100V; TO-9	*	2N2687	.28A@55°C 30V; TO-18
10-5	2N1873A	1.25A@100°C 150V; TO-9	*	2N2688	.28A@55°C 60V; TO-18
10-5	2N1874A, J	1.25A@100°C 200V; TO-9	*	2N2689	.28A@55°C 100V; TO-18
10-9	2N1875	1.25A@100°C 15V; TO-9	*	2N2690	.28A@55°C 200V; TO-18
10-9	2N1876	1.25A@100°C 30V; TO-9			POWER TRANSISTOR
10-9	2N1877	1.25A@100°C 60V; TO-9	*	2N2828	NPN; 3A; 60V; TO-59
10-9	2N1878	1.25A@100°C 100V; TO-9	*	2N2829	NPN; 3A; 60V; TO-59
10-9	2N1879	1.25A@100°C 150V; TO-9	*	2N2858	NPN; 3A; 80V; TO-5
10-9	2N1880	1.25A@100°C 200V; TO-9	*	2N2859	NPN; 3A; 100V; TO-5
10-11	2N1881	1.0A@100°C 30V; TO-9	*	2N2877, 2N2878	NPN; 5A; 80V; TO-59
10-11	2N1882	1.0A@100°C 60V; TO-9	*	2N2879	NPN; 5A; 100V; TO-59
10-11	2N1883	1.0A@100°C 100V; TO-9	4-15	2N2880, J, JTX, JTXV	NPN; 5A; 80V; TO-59
10-11	2N1884	1.0A@100°C 150V; TO-9	*	2N2890, 2N2891	NPN; 5A; 80V; TO-5
10-11	2N1885	1.0A@100°C 200V; TO-9	*	2N2892, 2N2893	NPN; 5A; 80V; TO-59
		POWER TRANSISTOR	*	2N2983	NPN; 3A; 80V; TO-5
*	2N1886	NPN; 3.0A; TO-59	*	2N2984	NPN; 3A; 120V; TO-5
			*	2N2985	NPN; 3A; 80V; TO-5

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*	2N2987	NPN; 1A; 80V; TO-5	*	2N4001	NPN; 1.0A; 100V; TO-5
*	2N2988	NPN; 1A; 100V; TO-5	*	2N4070	NPN; 10.0A; 100V; TO-3
*	2N2989	NPN; 1A; 80V; TO-5	*	2N4075	NPN; 3.0A; 80V; TO-111
*	2N2990	NPN; 1A; 100V; TO-5	*	2N4076	NPN; 3.0A; 80V; TO-111
*	2N2991	NPN; 1A; 80V; TO-5 Stud			SCR
*	2N2992	NPN; 1A; 100V; TO-5 Stud	*	2N4108	180mA@25°C 50V; TO-18
*	2N2993	NPN; 1A; 80V; TO-5 Stud	*	2N4109	180mA@25°C 100V; TO-18
*	2N2994, 2N2995	NPN; 1A; 100V; TO-5 Stud	*	2N4110	180mA@25°C 200V; TO-18
		SCR	*	2N4144	250mA@75°C 15V; TO-18
*	2N3001	.25A@55°C 30V; TO-18	*	2N4145	250mA@75°C 30V; TO-18
*	2N3002	.25A@55°C 60V; TO-18	*	2N4146	250mA@75°C 60V; TO-18
*	2N3003	.25A@55°C 100V; TO-18	*	2N4147	250mA@75°C 100V; TO-18
*	2N3004	.25A@55°C 200V; TO-18	*	2N4148	250mA@75°C 150V; TO-18
*	2N3005	.25A@55°C 30V; TO-18	*	2N4149	250mA@75°C 200V; TO-18
*	2N3006	.25A@55°C 60V; TO-18			POWER TRANSISTOR
*	2N3007	.25A@55°C 100V; TO-18			NPN; 10.0A; 70V; TO-5
*	2N3008	.25A@55°C 200V; TO-18			SCR
10-16	2N: 027, J, JTX	500mA@100°C 30V; TO-18	4-27	2N4150, J, JTX, JTXV	1.0A@85°C 25V; TO-39
10-16	2N3028, J, JTX	500mA@100°C 60V; TO-18	*	2N4212	1.0A@85°C 50V; TO-39
10-16	2N3029, J, JTX	500mA@100°C 100V; TO-18	*	2N4213	1.0A@85°C 100V; TO-39
10-16	2N3030, J, JTX	.5A@100°C 30V; TO-18	*	2N4214	1.0A@85°C 150V; TO-39
10-16	2N3031, J, JTX	.5A@100°C 60V; TO-18	*	2N4215	1.0A@85°C 200V; TO-39
10-16	2N3032, J, JTX	.5A@100°C 100V; TO-18	*	2N4216	1.0A@85°C 250V; TO-39
*	2N3273	2.2A@85°C 100V; TO-39	*	2N4217	1.0A@85°C 300V; TO-39
*	2N3274	2.2A@85°C 200V; TO-39	*	2N4218	1.0A@85°C 400V; TO-39
*	2N3275	2.2A@85°C 300V; TO-39	*	2N4219	
*	2N3276	2.2A@85°C 400V; TO-39			POWER TRANSISTOR
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4-19	2N3419, J, JTX, JTXV	NPN; 3.0A; 80V; TO-5	4-31	2N5038, J, JTX, JTXV	NPN; 20.0A; 150V; TO-3
4-19	2N3420, J, JTX, JTXV	NPN; 3.0A; 60V; TO-5	4-31	2N5039, J, JTX, JTXV	NPN; 20.0A; 120V; TO-3
4-19	2N3421, J, JTX, JTXV	NPN; 3.0A; 80V; TO-5	*	2N5074-2N5075	NPN; 3A; 200V; TO-59
*	2N3445	NPN; 7.5A; 60V; TO-3	*	2N5076-2N5077	NPN; 3A; 250V; TO-59
*	2N3446	NPN; 7.5A; 80V; TO-3	*	2N5334	NPN; 3A; 60V; TO-39
*	2N3447	NPN; 7.5A; 60V; TO-3	*	2N5335	NPN; 3A; 80V; TO-39
*	2N3448	NPN; 7.5A; 80V; TO-3	*	2N5336-2N5337	NPN; 5A; 80V; TO-39
*	2N3469	NPN; 5.0A; 25V; TO-5	*	2N5338-2N5339	NPN; 5A; 100V; TO-39
		SCR	*	2N5346-2N5347	NPN; 7A; 80V; TO-59
*	2N3555	1.6A; 30V; TO-39	*	2N5348-2N5349	NPN; 7A; 100V; TO-59
*	2N3556	1.6A; 60V; TO-39	*	2N5477-2N5478	NPN; 7A; 80V; TO-59
*	2N3557	1.6A; 100V; TO-39	*	2N5479-2N5480	NPN; 7A; 100V; TO-59
*	2N3558	1.6A; 200V; TO-39	4-35	2N5552	NPN; 10A; 80V; TO-5
*	2N3559	1.6A; 30V; TO-39	4-35	2N5552.4	NPN; 10A; 80V; TO-5 (Stud)
*	2N3560	1.6A; 60V; TO-39	4-37	2N5658	NPN; 20A; 80V; TO-59
*	2N3561	1.6A; 100V; TO-39	4-37	2N5659	NPN; 20A; 80V; TO-111
*	2N3562	1.6A; 200V; TO-39	4-39	2N5660, J, JTX, JTXV	NPN; 3A; 200V; TO-66
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*	2N3744	NPN; 5.0A; 40V; TO-111	4-39	2N5662, J, JTX, JTXV	NPN; 3A; 200V; TO-5
*	2N3745	NPN; 5.0A; 60V; TO-111	4-39	2N5663, J, JTX, JTXV	NPN; 3A; 300V; TO-5
*	2N3746	NPN; 5.0A; 80V; TO-111	4-44	2N5664, J, JTX, JTXV	NPN; 5A; 200V; TO-66
*	2N3747	NPN; 5.0A; 40V; TO-111	4-44	2N5665, J, JTX, JTXV	NPN; 5A; 300V; TO-66
*	2N3748	NPN; 5.0A; 60V; TO-111	4-44	2N5666, J, JTX, JTXV	NPN; 5A; 200V; TO-5
4-15	2N3749, J, JTX, JTXV	NPN; 5.0A; 80V; TO-111	4-44	2N5667, J, JTX, JTXV	NPN; 5A; 300V; TO-5
*	2N3750	NPN; 5.0A; 40V; TO-111	4-49	2N5671	NPN; 30A; 120V; TO-3
*	2N3751	NPN; 5.0A; 60V; TO-111	4-49	2N5672	NPN; 30A; 150V; TO-3
*	2N3752	NPN; 5.0A; 80V; TO-111			SCR
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*	2N3851	NPN; 5.0A; 80V; TO-59	10-22	2N5725	1.6A@85°C 100V; TO-39
*	2N3852	NPN; 5.0A; 40V; TO-59	10-22	2N5726	1.6A@85°C 200V; TO-39
*	2N3853	NPN; 5.0A; 40V; TO-59	10-22	2N5727	1.6A@85°C 300V; TO-39
4-23	2N3996, J, JTX, JTXV	NPN; 5.0A; 80V; TO-111	10-22	2N5728	1.6A@85°C 400V; TO-39
4-23	2N3997, J, JTX, JTXV	NPN; 5.0A; 80V; TO-111			POWER TRANSISTOR
4-23	2N3998, J, JTX, JTXV	NPN; 5.0A; 80V; TO-59	4-53	2N5838	NPN; 3A; 275V; TO-3
4-23	2N3999, J, JTX, JTXV	NPN; 5.0A; 80V; TO-59	4-53	2N5839	NPN; 3A; 300V; TO-3

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*	2N6078	NPN; 7A; 300V; TO-66	4-114	2N6759	4.5A; 350V; 1.5Ω; TO-3
		NPN; 7A; 275V; TO-66	4-114	2N6760, J, JTX, JTXV	5.5A; 400V; 1.0Ω; TO-3
		PUT	4-118	2N6761	4A; 450V; 2.0Ω; TO-3
10-26	2N6119	400mW@25°C 40V; TO-18	4-118	2N6762, J, JTX, JTXV	4.5A; 500V; 1.5Ω; TO-3
10-26	2N6120	400mW@25°C 40V; TO-18	4-122	2N6763	31A; 60V; 0.08Ω; TO-3 (Modified)
10-30	2N6137	300mW@25°C 40V; TO-18	4-122	2N6764, J, JTX, JTXV	38A; 100V; 0.055Ω; TO-3 (Modified)
*	2N6233	POWER TRANSISTOR	4-126	2N6765	25A; 150V; 0.120Ω; TO-3 (Modified)
*	2N6234	NPN; 5A; 225V; TO-66	4-126	2N6766, J, JTX, JTXV	30A; 200V; 0.085Ω; TO-3 (Modified)
*	2N6235	NPN; 5A; 275V; TO-66	4-130	2N6767	12A; 350V; 0.4Ω; TO-3
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4-57	2N6251	NPN; 10A; 375V; TO-3	4-134	2N6770, J, JTX, JTXV	12A; 500V; 0.4Ω; TO-3
4-61	2N6306, J, JTX, JTXV	NPN; 10A; 450V; TO-3	4-138	2N6781	3.5A; 60V; 0.6Ω; TO-39
4-61	2N6307	NPN; 8.0A; 500V; TO-3	4-138	2N6782	3.5A; 100V; 0.6Ω; TO-39
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*	2N6333	2.0A@80°C 30V; TO-39	4-150	2N6786	1.25A; 400V; 3.6Ω; TO-39
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*	2N6337	2.0A@80°C 300V; TO-39	4-162	2N6790	3.5A; 200V; 0.8Ω; TO-39
		2.0A@80°C 400V; TO-39	4-168	2N6791	2.0A; 350V; 1.8Ω; TO-39
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4-65	2N6351, J, JTX, JTXV	NPN; 10.0A; 80V; TO-33	4-174	2N6793	1.5A; 450V; 3.0Ω; TO-39
4-65	2N6352, J, JTX, JTXV	NPN; 10.0A; 150V; TO-33	4-174	2N6794	1.5A; 500V; 3.0Ω; TO-39
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4-78	2N6543	NPN; 5A; 850V; TO-3	8-8	469-2, J, JTX	1 ph; 10A; 400V
4-82	2N6544	NPN; 8.0A; 650V; TO-3	8-8	469-3, J, JTX	1 ph; 10A; 600V
4-82	2N6545	NPN; 8.0A; 850V; TO-3	8-10	483-1, JTX	3 ph; 25.0A; 200V
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*	2N6580	NPN; 10A; 400V; TO-3	8-12	673-2	1 ph; 1.5A; 200V
*	2N6581	NPN; 10A; 450V; TO-3	8-12	673-3	1 ph; 1.5A; 300V
*	2N6582	NPN; 10A; 350V; TO-3	8-12	673-4	1 ph; 1.5A; 400V
*	2N6583	NPN; 10A; 400V; TO-3	8-12	673-5	1 ph; 1.5A; 500V
*	2N6584	NPN; 10A; 450V; TO-3	8-12	673-6	1 ph; 1.5A; 600V
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4-90	2N6672	NPN; 8A; 550V; TO-3	8-14	673-7.5	1 ph; 0.5A; 1800V
4-90	2N6673	NPN; 8A; 650V; TO-3	8-14	673-8	1 ph; 0.4A; 2400V
4-94	2N6674	NPN; 10A; 450V; TO-3	8-14	673-8.5	1 ph; 0.3A; 3000V
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8-23	681-3	15A; 300V	8-27	700-1	3 ph; 2.5A; 100V
8-23	681-4	15A; 400V	8-27	700-2	3 ph; 2.5A; 200V
8-23	681-5	15A; 500V	8-27	700-3	3 ph; 2.5A; 300V
8-23	681-6	15A; 600V	8-27	700-4	3 ph; 2.5A; 400V
		FULL WAVE BRIDGE	8-27	700-5	3 ph; 2.5A; 500V
8-17	682-1	3 ph; 20A; 100V	8-27	700-6	3 ph; 2.5A; 600V
8-17	682-2	3 ph; 20A; 200V	8-27	701-1	3 ph; 2.25A; 100V
8-17	682-3	3 ph; 20A; 300V	8-27	701-2	3 ph; 2.25A; 200V
8-17	682-4	3 ph; 20A; 400V	8-27	701-3	3 ph; 2.25A; 300V
8-17	682-5	3 ph; 20A; 500V	8-27	701-4	3 ph; 2.25A; 400V
8-17	682-6	3 ph; 20A; 600V	8-27	701-5	3 ph; 2.25A; 500V
8-20	683-1	1 ph; 20A; 100V	8-27	701-6	3 ph; 2.25A; 600V
8-20	683-2	1 ph; 20A; 200V	8-29	800-1	3 ph; 40A; 50V
8-20	683-3	1 ph; 20A; 300V	8-29	800-2	3 ph; 40A; 100V
8-20	683-4	1 ph; 20A; 400V	8-29	800-3	3 ph; 40A; 125V
8-20	683-5	1 ph; 20A; 500V	8-29	800-4	3 ph; 40A; 150V
8-20	683-6	1 ph; 20A; 600V	8-29	801-1	3 ph; 20A; 50V
8-20	684-1	1 ph; 10A; 100V	8-29	801-2	3 ph; 20A; 100V
8-20	684-2	1 ph; 10A; 200V	8-29	801-3	3 ph; 20A; 125V
8-20	684-3	1 ph; 10A; 300V	8-29	801-4	3 ph; 20A; 150V
8-20	684-4	1 ph; 10A; 400V	8-32	802-1	1 ph; 35A; 50V
8-20	684-5	1 ph; 10A; 500V	8-32	802-2	1 ph; 35A; 100V
8-20	684-6	1 ph; 10A; 600V	8-32	802-3	1 ph; 35A; 125V
		RECTIFIER MODULE	8-32	802-4	1 ph; 35A; 150V
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7-13	688-12	12kV	8-32	803-2	1 ph; 20A; 100V
7-13	688-15	15kV	8-32	803-3	1 ph; 20A; 125V
7-13	688-18	18kV	8-32	803-4	1 ph; 20A; 150V
7-13	688-20	20kV			DOUBLER OR CENTER-TAP
7-13	688-25	25kV	8-35	804-1	20A; 50V
			8-35	804-2	20A; 100V

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8-35	804-4	20A; 125V	*	BAX12	300mA; 75V; DO-35
		20A; 150V	*	BAX13	400mA; 90V; DO-35
		SCR	*	BAX16	75mA; 50V; DO-35
10-34	AA100	0.5A@100°C 60V; TO-18	*	BAX17	200mA; 150V; DO-35
10-34	AA101	0.5A@100°C 100V; TO-18	*	BAX81	200mA; 200V; DO-35
10-34	AA102	0.5A@100°C 200V; TO-18	*	BAX84	350mA; 90V; DO-35
10-34	AA103	0.5A@100°C 300V; TO-18	*	BAX92	75mA; 50V; DO-35
10-34	AA104	0.5A@100°C 400V; TO-18	*	BAY18	75mA; 50V; DO-35
10-34	AA107	0.5A@100°C 60V; TO-18	*	BAY19	250mA; 60V; DO-35
10-34	AA108	0.5A@100°C 100V; TO-18	*	BAY20	250mA; 120V; DO-35
10-34	AA109	0.5A@100°C 200V; TO-18	*	BAY21	250mA; 180V; DO-35
10-34	AA110	0.5A@100°C 300V; TO-18	*	BAY21	250mA; 350V; DO-35
10-34	AA111	0.5A@100°C 400V; TO-18	*	BAY31	15V; DO-35
10-34	AA114	0.5A@100°C 60V; TO-18	*	BAY36	100mA; 30V; DO-35
10-34	AA115	0.5A@100°C 100V; TO-18	*	BAY41	225mA; 40V; DO-35
10-34	AA116	0.5A@100°C 200V; TO-18	*	BAY42	225mA; 60V; DO-35
10-34	AA117	0.5A@100°C 300V; TO-18	*	BAY43	225mA; 80V; DO-35
10-34	AA118	0.5A@100°C 400V; TO-18	*	BAY44	250mA; 50V; DO-35
10-37	AD100	1.6A@85°C 60V; TO-39	*	BAY45	250mA; 150V; DO-35
10-37	AD101	1.6A@85°C 100V; TO-39	*	BAY46	250mA; 300V; DO-35
10-37	AD102	1.6A@85°C 200V; TO-39	*	BAY60	115mA; 25V; DO-35
10-37	AD103	1.6A@85°C 300V; TO-39	*	BAY71	75mA; 70V; DO-35
10-37	AD104	1.6A@85°C 400V; TO-39	*	BAY72	225mA; 125V; DO-35
10-37	AD107	1.6A@85°C 60V; TO-39	*	BAY73	225mA; 125V; DO-35
10-37	AD108	1.6A@85°C 100V; TO-39	*	BAY80	250mA; 150V; DO-35
10-37	AD109	1.6A@85°C 200V; TO-39			POWER TRANSISTOR
10-37	AD110	1.6A@85°C 300V; TO-39	*	BDY55	NPN; 15A; 60V; TO-3
10-37	AD111	1.6A@85°C 400V; TO-39	*	BDY56	NPN; 15A; 120V; TO-3
10-37	AD114	1.6A@85°C 60V TO-39	*	BDY57	NPN; 25A; 80V; TO-3
10-37	AD115	1.6A@85°C 100V; TO-39	*	BDY58	NPN; 25A; 125V; TO-3
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10-37	AD118	1.6A@85°C 400V; TO-39	*	BDY91	NPN; 15A; 80V; TO-3
		DIODE	*	BDY92	NPN; 15A; 60V; TO-3
*	BA127D	200mA; 100V; DO-35	*	BUR23	NPN; 30A; 325V; TO-3
*	BA129	225mA; 200V; DO-35	*	BUR24	NPN; 30A; 400V; TO-3
*	BA130	75mA; 35V; DO-35	*	BUS11	NPN; 5A; 400V; TO-3
		SCR	*	BUS11A	NPN; 5A; 450V; TO-3
*	BA150	0.5A@100°C 30V; TO-18	*	BUS12	NPN; 8A; 400V; TO-3
*	BA151	0.5A@100°C 60V; TO-18	*	BUS12A	NPN; 8A; 450V; TO-3
*	BA152	0.5A@100°C 100V; TO-18	*	BUS13	NPN; 15A; 400V; TO-3
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*	BA155	100mA; 150V; DO-35	*	BUS14	NPN; 30A; 400V; TO-3
*	BA166	50mA; 20V; DO-35	*	BUS14A	NPN; 30A; 450V; TO-3
*	BA167W	50mA; 25V; DO-35	*	BUT10	NPN; 2A; 400V; TO-220
*	BA180	50mA; 10V; DO-35	*	BUT10A	NPN; 2A; 450V; TO-220
*	BA181	50mA; 20V; DO-35	*	BUT11	NPN; 5A; 400V; TO-220
*	BA209	225mA; 100V; DO-35	*	BUT11A	NPN; 5A; 450V; TO-220
*	BA219	100mA; 100V; DO-35	*	BUV23	NPN; 30A; 325V; TO-3
*	BA220	200mA; 10V; DO-35	*	BUV24	NPN; 20A; 400V; TO-3
*	BA221	200mA; 30V; DO-35	*	BUV46	NPN; 6A; 400V; TO-220
*	BA317	100mA; 30V; DO-35	*	BUW24	NPN; 10A; 350V; TO-3
*	BAV10	300mA; 60V; DO-35	*	BUW25	NPN; 10A; 400V; TO-3
*	BAV18	250mA; 60V; DO-35	*	BUW26	NPN; 10A; 450V; TO-3
*	BAV19	250mA; 120V; DO-35	*	BUW34	NPN; 10A; 400V; TO-3
*	BAV20	250mA; 180V; DO-35	*	BUW35	NPN; 10A; 400V; TO-3
*	BAV21	250mA; 250V; DO-35	*	BUW36	NPN; 10A; 450V; TO-3
*	BAW24	600mA; 50V; DO-35	*	BUW42	NPN; 15A; 400V; TO-3
*	BAW25	600mA; 50V; DO-35	*	BUW44	NPN; 15A; 400V; TO-3
*	BAW26	600mA; 75V; DO-35	*	BUW45	NPN; 15A; 400V; TO-3
*	BAW27	600mA; 75V; DO-35	*	BUW46	NPN; 15A; 450V; TO-3
*	BAW62	100mA; 75V; DO-35	*	BUW88	NPN; 6A; 375V; TO-220
*	BAW75	300mA; 35V; DO-35	*	BUW88A	NPN; 6A; 400V; TO-220
			*	BUX11	NPN; 20A; 200V; TO-3
			*	BUX12	NPN; 20A; 250V; TO-3

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*	BUX14	NPN; 10A; 400V; TO-3	*	BYW27-150	2.0A; 150V
*	BUX23	NPN; 30A; 325V; TO-3	*	BYW27-200	2.0A; 200V
*	BUX24	NPN; 20A; 400V; TO-3	*	BYW29-50	7.0A; 50V; TO-220AC
*	BUX39	NPN; 30A; 90V; TO-3	*	BYW29-100	7.0A; 100V; TO-220AC
*	BUX40	NPN; 20A; 125V; TO-3	*	BYW29-150	7.0A; 150V; TO-220AC
*	BUX41	NPN; 15A; 200V; TO-3	*	BYW29-200	7.0A; 200V; TO-220AC
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*	BUX43	NPN; 10A; 325V; TO-3	*	BYW31-100	25A; 100V; DO-4
*	BUX44	NPN; 8A; 400V; TO-3	*	BYW31-150	25A; 150V; DO-4
*	BUX46	NPN; 3.5A; 400V; TO-3	*	BYW51-50	16A; 50V; TO-220AB
*	BUX47	NPN; 9A; 400V; TO-3	*	BYW51-100	16A; 100V; TO-220AB
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*	BUX82	NPN; 6A; 400V; TO-3	*	BYW77-200	30A; 200V; DO-4
*	BUX83	NPN; 6A; 450V; TO-3	*	BYW78-50	50A; 50V; DO-5
*	BUX84	NPN; 2A; 400V; TO-220	*	BYW78-100	50A; 100V; DO-5
*	BUX85	NPN; 2A; 450V; TO-220	*	BYW78-150	50A; 150V; DO-5
*	BUX97	NPN; 6A; 350V; TO-3	*	BYW78-200	50A; 200V; DO-5
*	BUX97A	NPN; 6A; 400V; TO-3	*	BYW80-50	7.0A; 50V; TO-220AC
*	BUX97B	NPN; 6A; 450V; TO-3	*	BYW80-100	7.0A; 100V; TO-220AC
*	BUX98	NPN; 30A; 400V; TO-3 (Modified)	*	BYW80-150	7.0A; 150V; TO-220AC
*	BUX98A	NPN; 30A; 450V; TO-3 (Modified)	*	BYW80-200	7.0A; 200V; TO-220AC
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*	BUY69B	NPN; 10A; 325V; TO-3	*	BYW81-100	25A; 100V; DO-4
*	BUY69C	NPN; 10A; 200V; TO-3	*	BYW81-150	25A; 150V; DO-4
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*	BY402	500mA; 100V; DO-7	*	BYW93-100 μ	70A; 100V; DO-5
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*	BYS75-45	75A; 45V; DO-5	*	BZV16C6V8	7%; 3W
*	BYV19-35	12A; 35V; TO-220AC	*	BZV16C7V8	7%; 3W
*	BYV19-40	12A; 40V; TO-220AC	*	BZV16C8V2	7%; 3W
*	BYV19-45	12A; 45V; TO-220AC	*	BZV16C9V1	7%; 3W
*	BYV23-35 μ	75A; 35V; DO-5	*	BZV16C10	7%; 3W
*	BYV23-45 μ	75A; 45V; DO-5	*	BZV16C11	7%; 3W
		RECTIFIER	*	BZV16C12	7%; 3W
*	BYV27-50	2.5A; 50V	*	BZV16C13	7%; 3W
*	BYV27-100	2.5A; 100V	*	BZV16C15	7%; 3W
*	BYV27-150	2.5A; 150V	*	BZV16C16	7%; 3W
*	BYV28-50	3.5A; 50V	*	BZV16C18	7%; 3W
*	BYV28-100	3.5A; 100V	*	BZV16C20	7%; 3W
*	BYV28-150	3.5A; 150V	*	BZV16C22	7%; 3W
*	BYV28-200	3.5A; 200V	*	BZV16C24	7%; 3W
		SCHOTTKY RECTIFIER	*	BZV16C27	7%; 3W
*	BYV33-35	16A; 35V; TO-220AB	*	BZV16C30	7%; 3W
*	BYV33-40	16A; 40V; TO-220AB	*	BZV16C33	7%; 3W
*	BYV33-45	16A; 45V; TO-220AB	*	BZV16C36	7%; 3W
		RECTIFIER	*	BZV16C39	7%; 3W
*	BYV79-50	16A; 50V; TO-220AC	*	BZV16C43	7%; 3W
*	BYV79-100	16A; 100V; TO-220AC	*	BZV16C47	7%; 3W
*	BYV79-150	16A; 150V; TO-220AC	*	BZV16C51	7%; 3W
*	BYV79-200	16A; 200V; TO-220AC	*	BZV16C56	7%; 3W
*	BYW27-50	2.0A; 50V	*	BZV16C62	7%; 3W
			*	BZV16C68	7%; 3W
			*	BZV16C75	7%; 3W
			*	BZV16C82	7%; 3W

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*	CB200	0.5A@100°C 30V; TO-18			5.0kV
*	CB201	0.5A@100°C 60V; TO-18	7-23	HVH5000	7.5kV
*	CB202	0.5A@100°C 100V; TO-18	7-23	HVH7500	10kV
*	CB203	0.5A@100°C 200V; TO-18	7-23	HVH10000	12.5kV
*	CD200	1.6A@85°C 30V; TO-39	7-23	HVH12500	15kV
*	CD201	1.6A@85°C 60V; TO-39	7-23	HVH15000	20kV
*	CD202	1.6A@85°C 100V; TO-39	7-23	HVH20000	25kV
*	CD203	1.6A@85°C 200V; TO-39	7-23	HVH25000	5.0kV
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10-40	GA101	400mA@100°C 60V; TO-18	7-25	HVHF7500	10kV
10-40	GA102	400mA@100°C 80V; TO-18	7-25	HVHF10000	12.5kV
10-44	GA200-GA200A	60V; TO-18	7-25	HVHF12500	15kV
10-44	GA201-GA201A	100V; TO-18	7-25	HVHF15000	20kV
10-44	GA300-GA300A	60V; TO-18	7-25	HVHF20000	25kV
10-44	GA301-GA301A	100V; TO-18	7-25	HVHF25000	15kV
10-44	GB200-GB200A	60V; TO-59	7-27	HVHJ15K	20kV
10-44	GB201-GB201A	100V; TO-59	7-27	HVHJ20K	22.5kV
10-47	GB300-GB300A	60V; TO-59	7-27	HVHJ25K	25kV
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7-15	HA15	1.5kV	7-27	HVHJ40K	40kV
7-15	HA20	2.0kV	7-27	HVHJ45K	45kV
7-15	HA25	2.5kV	7-29	HVHS2500	2.5kV
7-15	HA30	3.0kV	7-29	HVHS5000	5.0kV
7-15	HA40	4.0kV	7-29	HVHS7500	7.5kV
7-15	HA50	5.0kV	7-29	HVHS10000	10kV
7-15	HA75	7.5kV	7-29	HVHS12500	12.5kV
7-15	HA100	10kV	7-29	HVHS15000	15kV
7-17	HS10	1.0kV	7-29	HVHS17500	17.5kV
7-17	HS15	1.5kV	7-29	HVHS20000	20kV
7-17	HS20	2.0kV	7-31	HVJX15K	15kV
7-17	HS25	2.5kV	7-31	HVJX20K	20kV
7-17	HS30	3.0kV	7-31	HVJX22.5K	22.5kV
7-17	HS40	4.0kV	7-31	HVJX25K	25kV
7-17	HS50	5.0kV	7-31	HVJX30K	30kV
7-17	HS75	7.5kV	7-31	HVJX35K	35kV
7-17	HS100	10kV	7-31	HVJX37.5K	37.5kV
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7-17	HVE25 (1N3646)	2.5kV	7-15	HVX15	1.5kV
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7-17	HVE100 (1N5184)	10kV	7-15	HVX50	5.0kV
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7-19	HVF5000	5.0kV	7-15	HVX100	10kV
7-19	HVF7500	7.5kV			
7-19	HVF10000	10kV			
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7-19	HVF20000	20kV	10-50	ID102	0.5A@100°C 100V; TO-18
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7-21	HVFS5000	5.0kV	10-50	ID105	0.5A@100°C 300V; TO-18
7-21	HVFS7500	7.5kV	10-50	ID106	0.5A@100°C 400V; TO-18
7-21	HVFS10000	10kV	10-53	ID200	1.6A@70°C 50V; TO-39
7-21	HVFS12500	12.5kV	10-53	ID201	1.6A@70°C 100V; TO-39
7-21	HVFS15000	15kV	10-53	ID202	1.6A@70°C 150V; TO-39
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3-133	UC7815AK	1A; +15V; TO-3; Precision Fixed Reg.	*	UCDA1F	15A; 100V
3-127	UC7815CK	1A; +15V; TO-3; Fixed Reg.	*	UCDA2F	15A; 200V
3-127	UC7815CT	1A; +15V; TO-220; Fixed Reg.	*	UCDA4F	15A; 400V
3-127	UC7815K	1A; +15V; TO-3; Fixed Reg.	*	UCDA6F	15A; 600V
3-145	UC7905ACK	1A; -5V; TO-3; Precision Fixed Reg.	*	UCNA1	15A; 100V
3-145	UC7905ACT	1A; -5V; TO-220; Precision Fixed Reg.	*	UCNA2	15A; 200V
3-145	UC7905AK	1A; -5V; TO-3; Precision Fixed Reg.	*	UCNA4	15A; 400V
3-139	UC7905CK	1A; -5V; TO-3; Fixed Reg.	*	UCNA6	15A; 600V
3-139	UC7905CT	1A; -5V; TO-220; Fixed Reg.	*	UCNA1F	15A; 100V
3-139	UC7905K	1A; -5V; TO-3; Fixed Reg.	*	UCNA2F	15A; 200V
3-145	UC7912ACK	1A; -12V; TO-3; Precision Fixed Reg.	*	UCNA4F	15A; 400V
3-145	UC7912ACT	1A; -12V; TO-220; Precision Fixed Reg.	*	UCNA6F	15A; 600V
3-145	UC7912AK	1A; -12V; TO-3; Precision Fixed Reg.	*	UCPA1	15A; 100V
3-139	UC7912CK	1A; -12V; TO-3; Fixed Reg.	*	UCPA2	15A; 200V
3-139	UC7912CT	1A; -12V; TO-220 Fixed Reg.	*	UCPA4	15A; 400V
3-139	UC7912K	1A; -12V; TO-3; Fixed Reg.	*	UCPA6	15A; 600V
3-145	UC7915ACK	1A; -15V; TO-3; Precision Fixed Reg.	*	UCPA1F	15A; 100V
3-145	UC7915ACT	1A; -15V; TO-220; Precision Fixed Reg.	*	UCPA2F	15A; 200V
3-145	UC7915AK	1A; -15V; TO-3; Precision Fixed Reg.	*	UCPA4F	15A; 400V
3-139	UC7915CK	1A; -15V; TO-3; Fixed Reg.	*	UCPA6F	15A; 600V
3-139	UC7915CT	1A; -15V; TO-220; Fixed Reg.	7-37	UDA5	RECTIFIER MODULE
3-139	UC7915K	1A; -15V; TO-3; Fixed Reg.	7-37	UDA7.5	5.0kV
*	UCBA1	FULL WAVE BRIDGE	7-37	UDA10	7.5kV
*	UCBA2	1 ph; 25A; 100V	7-37	UDA15	10kV
*	UCBA4	1 ph; 25A; 200V	7-37	UDA15	15kV
*	UCBA6	1 ph; 25A; 400V	7-37	UDB2.5	2.5kV
*	UCBA1F	1 ph; 25A; 600V	7-37	UDB5	5.0kV
		1 ph; 20A; 100V	7-37	UDB7.5	7.5kV
			7-37	UDC5	5.0kV
			7-37	UDC7.5	7.5kV
			7-37	UDC10	10kV
			7-37	UDC15	15kV
			7-37	UDD2.5	2.5kV
			7-37	UDD5	5.0kV
			7-37	UDD7.5	7.5kV
			7-37	UDE2.5	2.5kV
			7-37	UDE5	5.0kV
			7-37	UDF2.5	2.5kV
			7-37	UDF5	5.0kV
			9-18	UDZ707-UDZ790	ZENER
			9-18	UDZ807-UDZ890	Bidirectional; 3W; 5%
			9-18	UDZ5707-UDZ5790	Bidirectional; 3W; 10%
			9-18	UDZ5807-UDZ5890	Bidirectional; 5W; 5%
			9-18	UDZ8707-UDZ8791	Bidirectional; 5W; 10%
			9-18	UDZ8807-UDZ8891	Bidirectional; 1W; 5%
			9-18	UDZ8807-UDZ8891	Bidirectional; 1W; 10%

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6-24	UES102 (1N5803)	2.5A; 75V	7-41	UFB5	5.0kV
6-24	UES103 (1N5804)	2.5A; 100V	7-41	UFB7.5	7.5kV
6-24	UES104 (1N5805)	2.5A; 125V			POWER MOSFET
6-24	UES201 (1N5807)	6.0A; 50V			TRANSISTOR
6-24	UES202 (1N5808)	6.0A; 75V	4-212	UFNA11	1.0A; 60V; 1.5Ω; TO-92
6-24	UES203 (1N5809)	6.0A; 100V	4-212	UFNA12	1.0A; 100V; 1.5Ω; TO-92
6-24	UES204 (1N5810)	6.0A; 125V	4-214	UFND120	0.5A; 100V; 2.4Ω; DIL-4
*	UES301	20.0A; 50V	4-214	UFND123	0.4A; 60V; 3.2Ω; DIL-4
*	UES302	20.0A; 75V	4-220	UFND110	1.0A; 100V; 0.6Ω; DIL-4
*	UES303	20.0A; 100V	4-220	UFND113	0.8A; 60V; 0.8Ω; DIL-4
*	UES304	20.0A; 125V	4-226	UFND120	1.3A; 100V; 0.3Ω; DIL-4
6-67	UES501	50.0A; 50V; DO-5	4-226	UFND123	1.1A; 60V; 0.4Ω; DIL-4
6-67	UES502	50.0A; 75V; DO-5	4-232	UFND210	0.6A; 200V; 1.5Ω; DIL-4
6-67	UES503	50.0A; 100V; DO-5	4-232	UFND213	0.45A; 150V; 2.4Ω; DIL-4
6-67	UES504	50.0A; 125V; DO-5	4-238	UFNF110	3.5A; 100V; 0.6Ω; TO-39
6-67	UES505	50.0A; 150V; DO-5	4-238	UFNF111	3.5A; 60V; 0.6Ω; TO-39
6-70	UES701	25.0A; 50V; DO-4	4-238	UFNF112	3.5A; 100V; 0.8Ω; TO-39
6-70	UES702	25.0A; 100V; DO-4	4-238	UFNF113	3.5A; 60V; 0.8Ω; TO-39
6-70	UES703	25.0A; 150V; DO-4	4-244	UFNF120	6A; 100V; 0.30Ω; TO-39
6-72	UES704	20.0A; 200V; DO-4	4-244	UFNF121	6A; 60V; 0.30Ω; TO-39
6-72	UES705	20.0A; 300V; DO-4	4-244	UFNF122	5A; 100V; 0.40Ω; TO-39
6-72	UES706	20.0A; 400V; DO-4	4-244	UFNF123	5A; 60V; 0.40Ω; TO-39
6-75	UES801	70.0A; 50V; DO-5	4-250	UFNF130	8A; 100V; 0.18Ω; TO-39
6-75	UES802	70.0A; 100V; DO-5	4-250	UFNF131	8A; 60V; 0.18Ω; TO-39
6-75	UES803	70.0A; 150V; DO-5	4-250	UFNF132	7A; 100V; 0.25Ω; TO-39
6-78	UES804	50.0A; 200V; DO-5	4-250	UFNF133	7A; 60V; 0.25Ω; TO-39
6-78	UES805	50.0A; 300V; DO-5	4-256	UFNF210	2.2A; 200V; 1.5Ω; TO-39
6-78	UES806	50.0A; 400V; DO-5	4-256	UFNF211	2.2A; 150V; 1.5Ω; TO-39
6-81	UES1001	1A; 50V	4-256	UFNF212	1.8A; 200V; 2.4Ω; TO-39
6-81	UES1002	1A; 100V	4-256	UFNF213	1.8A; 150V; 2.4Ω; TO-39
6-81	UES1003	1A; 150V	4-262	UFNF220	3.5A; 200V; 0.8Ω; TO-39
6-83	UES1101	2.5A; 50V	4-262	UFNF221	3.5A; 150V; 0.8Ω; TO-39
6-83	UES1102	2.5A; 100V	4-262	UFNF222	3.0A; 200V; 1.2Ω; TO-39
6-83	UES1103	2.5A; 150V	4-262	UFNF223	3.0A; 150V; 1.2Ω; TO-39
6-86	UES1104	2.0A; 200V	4-268	UFNF230	5.5A; 200V; 0.4Ω; TO-39
6-86	UES1105	2.0A; 300V	4-268	UFNF231	5.5A; 150V; 0.4Ω; TO-39
6-86	UES1106	2.0A; 400V	4-268	UFNF232	4.5A; 200V; 0.6Ω; TO-39
6-89	UES1301	6.0A; 50V	4-268	UFNF233	4.5A; 150V; 0.6Ω; TO-39
6-89	UES1302	6.0A; 100V	4-274	UFNF310	1.35A; 400V; 3.6Ω; TO-39
6-89	UES1303	6.0A; 150V	4-274	UFNF311	1.35A; 350V; 3.6Ω; TO-39
6-92	UES1304	5.0A; 200V	4-274	UFNF312	1.15A; 400V; 5.0Ω; TO-39
6-92	UES1305	5.0A; 300V	4-274	UFNF313	1.15A; 350V; 5.0Ω; TO-39
6-92	UES1306	5.0A; 400V	4-280	UFNF320	2.5A; 400V; 1.8Ω; TO-39
6-95	UES1401	8.0A; 50V; TO-220AC	4-280	UFNF321	2.5A; 350V; 1.8Ω; TO-39
6-95	UES1402	8.0A; 100V; TO-220AC	4-280	UFNF322	2.0A; 400V; 2.5Ω; TO-39
6-95	UES1403	8.0A; 150V; TO-220AC	4-280	UFNF323	2.0A; 350V; 2.5Ω; TO-39
6-95	UES1404	8.0A; 200V; TO-220AC	4-286	UFNF330	3.5A; 400V; 3.5Ω; TO-39
6-98	UES1501	16A; 50V; TO-220AC	4-286	UFNF331	3.5A; 350V; 3.5Ω; TO-39
6-98	UES1502	16A; 100V; TO-220AC	4-286	UFNF332	3.0A; 400V; 3.0Ω; TO-39
6-98	UES1503	16A; 150V; TO-220AC	4-286	UFNF333	3.0A; 350V; 3.0Ω; TO-39
6-98	UES1504	16A; 200V; TO-220AC	4-292	UFNF420	1.6A; 500V; 3.0Ω; TO-39
		RECTIFIER, CENTER-TAP	4-292	UFNF421	1.6A; 450V; 3.0Ω; TO-39
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6-101	UES2402	16A; 100V; TO-220AB	4-292	UFNF423	1.4A; 450V; 4.0Ω; TO-39
6-101	UES2403	16A; 150V; TO-220AB	4-298	UFNF430	2.75A; 500V; 1.5Ω; TO-39
6-101	UES2404	16A; 200V; TO-220AB	4-298	UFNF431	2.75A; 450V; 1.5Ω; TO-39
6-104	UES2601	30A; 50V; TO-3	4-298	UFNF432	2.25A; 500V; 2.0Ω; TO-39
6-104	UES2602	30A; 100V; TO-3	4-298	UFNF433	2.25A; 450V; 2.0Ω; TO-39
6-104	UES2603	30A; 150V; TO-3	4-304	UFN120	8A; 100V; 0.30Ω; TO-3
6-107	UES2604	30A; 200V; TO-3	4-304	UFN121	8A; 60V; 0.30Ω; TO-3
6-107	UES2605	30A; 300V; TO-3	4-304	UFN122	7A; 100V; 0.40Ω; TO-3
6-107	UES2606	30A; 400V; TO-3	4-304	UFN123	7A; 60V; 0.40Ω; TO-3
			4-310	UFN130	14A; 100V; 0.18Ω; TO-3

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4-310	UFN132	12A; 100V; 0.25Ω; TO-3	4-382	UFN432	4A; 500V; 2.0Ω; TO-3
4-310	UFN133	12A; 60V; 0.25Ω; TO-3	4-382	UFN433	4A; 450V; 2.0Ω; TO-3
4-316	UFN140	27A; 100V; 0.85Ω; TO-3 (Modified)	4-388	UFN440	8A; 500V; 0.85Ω; TO-3
4-316	UFN141	27A; 60V; 0.85Ω; TO-3 (Modified)	4-388	UFN441	8A; 450V; 0.85Ω; TO-3
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4-316	UFN143	24A; 60V; 0.11Ω; TO-3 (Modified)	4-388	UFN443	7A; 450V; 1.10Ω; TO-3
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4-322	UFN153	33A; 60V; 0.08Ω; TO-3 (Modified)	4-394	UFN453	12A; 450V; 0.5Ω; TO-3
4-328	UFN220	5A; 200V; 0.8Ω; TO-3	4-400	UFN510	4A; 100V; 0.6Ω; TO-220AB
4-328	UFN221	5A; 150V; 0.8Ω; TO-3	4-400	UFN511	4A; 60V; 0.6Ω; TO-220AB
4-328	UFN222	4A; 200V; 1.2Ω; TO-3	4-400	UFN512	3.5A; 100V; 0.8Ω; TO-220AB
4-328	UFN223	4A; 150V; 1.2Ω; TO-3	4-400	UFN513	3.5A; 60V; 0.8Ω; TO-220AB
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4-334	UFN231	9A; 150V; 0.4Ω; TO-3	4-406	UFN521	8A; 60V; 0.30Ω; TO-220AB
4-334	UFN232	8A; 200V; 0.6Ω; TO-3	4-406	UFN522	7A; 100V; 0.40Ω; TO-220AB
4-334	UFN233	8A; 150V; 0.6Ω; TO-3	4-406	UFN523	7A; 60V; 0.40Ω; TO-220AB
4-340	UFN240	18A; 200V; 0.18Ω; TO-3 (Modified)	4-412	UFN530	14A; 100V; 0.18Ω; TO-220AB
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4-340	UFN243	16A; 150V; 0.22Ω; TO-3 (Modified)	4-412	UFN533	12A; 60V; 0.25Ω; TO-220AB
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4-346	UFN251	30A; 150V; 0.085Ω; TO-3 (Modified)	4-418	UFN541	27A; 60V; 0.085Ω; TO-220AB
4-346	UFN252	25A; 200V; 0.120Ω; TO-3 (Modified)	4-418	UFN542	24A; 100V; 0.11Ω; TO-220AB
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4-352	UFN321	3A; 350V; 1.8Ω; TO-3	4-424	UFN611	2.5A; 150V; 1.5Ω; TO-220AB
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4-352	UFN323	2.5A; 350V; 2.5Ω; TO-3	4-424	UFN613	2A; 150V; 2.4Ω; TO-220AB
4-358	UFN330	5.5A; 400V; 1.0Ω; TO-3	4-430	UFN620	5A; 200V; 0.8Ω; TO-220AB
4-358	UFN331	5.5A; 350V; 1.0Ω; TO-3	4-430	UFN621	5A; 150V; 0.8Ω; TO-220AB
4-358	UFN332	4.5A; 400V; 1.5Ω; TO-3	4-430	UFN622	4A; 200V; 1.2Ω; TO-220AB
4-358	UFN333	4.5A; 350V; 1.5Ω; TO-3	4-430	UFN623	4A; 150V; 1.2Ω; TO-220AB
4-364	UFN340	10A; 400V; 0.55Ω; TO-3	4-436	UFN630	9A; 200V; 0.4Ω; TO-220AB
4-364	UFN341	10A; 350V; 0.55Ω; TO-3	4-436	UFN631	9A; 150V; 0.4Ω; TO-220AB
4-364	UFN342	8A; 400V; 0.80Ω; TO-3	4-436	UFN632	8A; 200V; 0.6Ω; TO-220AB
4-364	UFN343	8A; 350V; 0.80Ω; TO-3	4-436	UFN633	8A; 150V; 0.6Ω; TO-220AB
4-370	UFN350	15A; 400V; 0.3Ω; TO-3	4-442	UFN640	18A; 200V; 0.18Ω; TO-220AB
4-370	UFN351	15A; 350V; 0.3Ω; TO-3	4-442	UFN641	18A; 150V; 0.18Ω; TO-220AB
4-370	UFN352	13A; 400V; 0.4Ω; TO-3	4-442	UFN642	16A; 200V; 0.22Ω; TO-220AB
4-370	UFN353	13A; 350V; 0.4Ω; TO-3	4-442	UFN643	16A; 150V; 0.22Ω; TO-220AB
4-376	UFN420	2.5A; 500V; 3.0Ω; TO-3	4-448	UFN710	1.5A; 400V; 3.6Ω; TO-220AB
4-376	UFN421	2.5A; 450V; 3.0Ω; TO-3	4-448	UFN711	1.5A; 350V; 3.6Ω; TO-220AB
4-376	UFN422	2A; 500V; 4.0Ω; TO-3	4-448	UFN712	1.3A; 400V; 5.0Ω; TO-220AB
4-376	UFN423	2A; 450V; 4.0Ω; TO-3	4-448	UFN713	1.3A; 350V; 5.0Ω; TO-220AB
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			4-472	UFN822	2.0A; 500V; 4.0Ω; TO-220AB
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4-478	UFN832	4.0A; 500V; 2.0Ω; TO-220AB	4-527	UPT211	NPN; 2.0A; 40V; TO-5
4-478	UFN833	4.0A; 450V; 2.0Ω; TO-220AB	4-527	UPT212	NPN; 2.0A; 60V; TO-5
4-484	UFN840	8.0A; 500V; 0.85Ω; TO-220AB	4-527	UPT213	NPN; 2.0A; 80V; TO-5
4-484	UFN841	8.0A; 450V; 0.85Ω; TO-220AB	4-527	UPT214	NPN; 2.0A; 100V; TO-5
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7-44	UGB5	5.0kV	4-529	UPT321	NPN; 2.0A; 150V; TO-66
7-44	UGB7.5	7.5kV	4-529	UPT322	NPN; 2.0A; 200V; TO-66
7-44	UGB10	10kV	4-529	UPT323	NPN; 2.0A; 250V; TO-66
7-44	UGD5	5.0kV	4-529	UPT324	NPN; 2.0A; 300V; TO-66
7-44	UGD7.5	7.5kV	4-529	UPT325	NPN; 2.0A; 300V; TO-66
7-44	UGD10	10kV	4-531	UPT521	NPN; 3.5A; 150V; TO-66
7-44	UGE2.5	2.5kV	4-531	UPT522	NPN; 3.5A; 200V; TO-66
7-44	UGE5	5.0kV	4-531	UPT523	NPN; 3.5A; 250V; TO-66
7-44	UGE7.5	7.5kV	4-531	UPT524	NPN; 3.5A; 300V; TO-66
7-44	UGF2.5	2.5kV	4-531	UPT525	NPN; 3.5A; 300V; TO-66
7-44	UGF5	5.0kV	4-533	UPT611	NPN; 5.0A; 40V; TO-5
7-44	UGF7.5	7.5kV	4-533	UPT612	NPN; 5.0A; 60V; TO-5
		PIN DIODE	4-533	UPT613	NPN; 5.0A; 80V; TO-5
12-9	UM4000 series	0.5Ω, 3.0pF, 25W, 100-1200V	4-533	UPT614	NPN; 5.0A; 100V; TO-5
12-14	UM4300 series	1.5Ω, 2.2pF, 18W, 100-1000V	4-533	UPT615	NPN; 5.0A; 100V; TO-5
12-9	UM4900 series	0.5Ω, 3.0pF, 37W, 100-600V	4-535	UPT721	NPN; 5.0A; 150V; TO-66
12-20	UM6000 series	1.7Ω, 0.5pF, 6W, 100-1000V	4-535	UPT722	NPN; 5.0A; 200V; TO-66
12-20	UM6200 series	0.4Ω, 1.1pF, 6W, 100-400V	4-535	UPT723	NPN; 5.0A; 250V; TO-66
12-20	UM6600 series	2.5Ω, 0.4pF, 4W, 100-1000V	4-535	UPT724	NPN; 5.0A; 300V; TO-66
12-25	UM7000 series	1.0Ω, 0.9pF, 10W, 100-1600V	4-537	UPT725	NPN; 5.0A; 300V; TO-66
12-25	UM7100 series	0.6Ω, 1.2pF, 10W, 100-800V	4-537	UPTA510	NPN; 0.5A; 100V; TO-92
12-25	UM7200 series	0.25Ω, 2.2pF, 10W, 100-400V	4-537	UPTA520	NPN; 0.5A; 200V; TO-92
12-14	UM7300 series	3.5Ω, 0.7pF, 7.5W, 100-1000V	4-537	UPTA530	NPN; 0.5A; 300V; TO-92
12-30	UM9301 series	CATV Attenuator Diodes	4-539	UPTB520	NPN; 0.1A; 200V; TO-92
12-33	UM9401	2-Way Radio Switch Diodes	4-539	UPTB530	NPN; 0.1A; 300V; TO-92
12-33	UM9402	2-Way Radio Switch Diodes	4-539	UPTB540	NPN; 0.1A; 400V; TO-92
12-33	UM9415	2-Way Radio Switch Diodes	4-539	UPTB550	NPN; 0.1A; 500V; TO-92
12-38	UM9441	Radiation Detector			RECTIFIER
12-40	UM9601-UM9608	Microstrip PIN	6-110	UR105	2.0A; 50V
12-50	UM9701	Low R _s Antenna Switch	6-110	UR110	1.0A; 100V
		POWER TRANSISTOR	6-110	UR115	1.0A; 150V
4-490	UMT1006	NPN; 5A; 400V; TO-3	6-110	UR120	1.0A; 200V
4-490	UMT1007	NPN; 5A; 500V; TO-3	6-110	UR125	1.0A; 250V
4-494	UMT1008	NPN; 8A; 300V; TO-3	6-110	UR205	2.0A; 50V
4-494	UMT1009	NPN; 8A; 400V; TO-3	6-110	UR210	2.0A; 100V
4-498	UMT1011	NPN; 15A; 400V; TO-3	6-110	UR215	2.0A; 150V
4-498	UMT1012	NPN; 15A; 500V; TO-3	6-110	UR220	2.0A; 200V
4-502	UMT1203	NPN; 3.0A; 300V; TO-220	6-110	UR225	2.0A; 250V
4-502	UMT1204	NPN; 3.0A; 400V; TO-220	*	UR710	1.0A; 100V
4-506	UMT2000	NPN; 15A; 850V; TO-3	*	UR720	1.0A; 200V
4-510	UMT2003	NPN; 30A; 850V; TO-3 (Modified)	7-48	US12	RECTIFIER MODULE
4-513	UMT13004	NPN; 4.0A; 600V; TO-220	7-48	US15	1.2kV
4-513	UMT13005	NPN; 4.0A; 700V; TO-220	7-48	US18	1.5kV
4-517	UMT13006	NPN; 8.0A; 600V; TO-220	7-48	US20	1.8kV
4-517	UMT13007	NPN; 8.0A; 700V; TO-220	7-48	US25	2.0kV
4-521	UMT13008	NPN; 12.0A; 600V; TO-220	7-48	US25	2.5kV
4-521	UMT13009	NPN; 12.0A; 700V; TO-220	7-48	US30	3.0kV
4-525	UPT111	NPN; 1.0A; 40V; TO-5	7-48	US35	3.5kV
4-525	UPT112	NPN; 1.0A; 60V; TO-5	7-48	US40	4.0kV
4-525	UPT113	NPN; 1.0A; 80V; TO-5	7-48	US45A	4.5kV
4-525	UPT114	NPN; 1.0A; 100V; TO-5	7-48	US50A	5.0kV
			7-48	US60A	6.0kV
			7-48	US70A	7.0kV

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PAGE	PART NUMBER	DESCRIPTION	PAGE	PART NUMBER	DESCRIPTION
		RECTIFIER MODULE			RECTIFIER MODULE
7-48	US80A	8.0kV	7-48	USR45A	4.5kV
7-48	US100A	10kV	7-48	USR50A	5.0kV
7-48	US120A	12kV	7-48	USR60A	6.0kV
7-48	US150A	15kV	7-48	USR70A	7.0kV
7-48	US180A	18kV	7-48	USR80A	8.0kV
7-48	US200A	20kV	7-48	USR100A	10kV
7-41	USB2.5	2.5kV	7-48	USR120A	12kV
7-41	USB5	5.0kV	7-48	USR150A	15kV
7-41	USB7.5	7.5kV	7-48	USR180A	18kV
7-41	USB10	10kV	7-41	USS5	5.0kV
		SCHOTTKY RECTIFIER	7-41	USS7.5	7.5kV
6-113	USD320C	30A; 20V; TO-3	7-41	USS10	10kV
6-113	USD335C	30A; 35V; TO-3	7-41	USS15	15kV
6-113	USD345C	30A; 45V; TO-3			RECTIFIER
6-115	USD520	75A; 20V; DO-5	*	UT111 (1N536)	0.75A; 50V
6-115	USD535	75A; 35V; DO-5	*	UT112 (1N537)	0.75A; 100V
6-115	USD545	75A; 45V; DO-5	*	UT113 (1N3656)	0.75A; 200V
6-118	USD545HR2	75A; 45V; DO-5	*	UT114 (1N539)	0.75A; 300V
6-115	USD550	75A; 50V; DO-5	*	UT115 (1N3657)	0.75A; 400V
6-121	USD620	6A; 20V; TO-220AC	*	UT117 (1N547)	0.75A; 500V
6-121	USD635	6A; 35V; TO-220AC	*	UT118 (1N3658)	0.75A; 600V
6-121	USD640	6A; 40V; TO-220AC	*	UT119	0.75A; 800V
6-121	USD645	6A; 45V; TO-220AC	*	UT120	0.75A; 1000V
6-123	USD620C	12A; 20V; TO-220AB	*	UT211 (1N645)	0.75A; 225V
6-123	USD635C	12A; 35V; TO-220AB	*	UT212 (1N646)	0.75A; 300V
6-123	USD640C	12A; 40V; TO-220AB	*	UT213 (1N647)	0.75A; 400V
6-123	USD645C	12A; 45V; TO-220AB	*	UT214 (1N648)	0.75A; 500V
6-125	USD720	8A; 20V; TO-220AC	*	UT215 (1N649)	0.75A; 600V
6-125	USD735	8A; 35V; TO-220AC	*	UT221 (1N676)	0.5A; 100V
6-125	USD740	8A; 40V; TO-220AC	*	UT222 (1N677)	0.75A; 100V
6-125	USD745	8A; 45V; TO-220AC	*	UT223 (1N678)	0.5A; 200V
6-127	USD720C	16A; 20V; TO-220AB	*	UT224 (1N679)	0.75A; 200V
6-127	USD735C	16A; 35V; TO-220AB	*	UT225 (1N681)	0.5A; 300V
6-127	USD740C	16A; 40V; TO-220AB	*	UT226 (1N682)	0.75A; 300V
6-127	USD745C	16A; 45V; TO-220AB	*	UT227 (1N683)	0.5A; 400V
6-129	USD820	12A; 20V; TO-220AC	*	UT228 (1N684)	0.75A; 400V
6-129	USD835	12A; 35V; TO-220AC	*	UT229 (1N685)	0.5A; 500V
6-129	USD840	12A; 40V; TO-220AC	*	UT231 (1N686)	0.75A; 500V
6-129	USD845	12A; 45V; TO-220AC	*	UT232 (1N687)	0.5A; 600V
6-131	USD920	16A; 20V; TO-220AC	*	UT233 (1N689)	0.75A; 600V
6-131	USD935	16A; 35V; TO-220AC	6-139	UT234	1.0A; 200V
6-131	USD940	16A; 40V; TO-220AC	6-139	UT235	1.0A; 400V
6-131	USD945	16A; 45V; TO-220AC	6-139	UT236	1.0A; 100V
6-133	USD1120	1.0A; 20V; ASA	6-139	UT237	1.0A; 500V
6-133	USD1130	1.0A; 30V; ASA	6-139	UT238	1.0A; 600V
6-133	USD1140	1.0A; 40V; ASA	6-139	UT242	1.25A; 200V
*	USD6035	60A; 35V; DO-5	6-139	UT244	1.25A; 400V
*	USD6045	60A; 45V; DO-5	6-139	UT245	1.25A; 500V
		SCHOTTKY MODULE	6-139	UT247	1.25A; 600V
6-135	USM140C	100A; 40V; M1	6-139	UT249	1.25A; 100V
6-135	USM145C	100A; 45V; M1	6-139	UT251	1.5A; 100V
6-135	USM150C	100A; 50V; M1	6-139	UT252	1.5A; 200V
6-137	USM20040C	200A; 40V; M2	6-139	UT254	1.5A; 400V
6-137	USM20045C	200A; 45V; M2	6-139	UT255	1.5A; 500V
6-137	USM20050C	200A; 50V; M2	6-139	UT257	1.5A; 600V
		RECTIFIER MODULE	6-139	UT258	1.5A; 800V
7-48	USR12	1.2kV	6-139	UT261	2.0A; 100V
7-48	USR15	1.5kV	6-139	UT262 (1N3981)	2.0A; 200V
7-48	USR18	1.8kV	6-139	UT264 (1N3982)	2.0A; 400V
7-48	USR20	2.0kV	6-139	UT265	2.0A; 500V
7-48	USR25	2.5kV	6-139	UT267 (1N3983)	2.0A; 600V
7-48	USR30	3.0kV	6-139	UT268	2.0A; 800V
7-48	USR35	3.5kV	6-139	UT347	1.0A; 1000V
7-48	USR40A	4.0kV	6-139	UT361	1.0A; 800V
			6-139	UT362	1.2A; 800V

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PAGE	PART NUMBER	DESCRIPTION	PAGE	PART NUMBER	DESCRIPTION
		RECTIFIER			RECTIFIER
6-139	UT363	1.2A; 1000V	6-154	UTR2340	2.0A; 400V
6-139	UT364	1.5A; 1000V	6-154	UTR2350	2.0A; 500V
6-143	UT2005	2.0A; 50V	6-154	UTR2360	2.0A; 600V
6-143	UT2010	2.0A; 100V	6-154	UTR3305	3.0A; 50V
6-143	UT2020	2.0A; 200V	6-154	UTR3310	3.0A; 100V
6-143	UT2040	2.0A; 400V	6-154	UTR3320	3.0A; 200V
6-143	UT2060	2.0A; 600V	6-154	UTR3340	3.0A; 400V
*	UT2080	2.0A; 800V	6-154	UTR3350	3.0A; 500V
6-143	UT3005	3.0A; 50V	6-154	UTR3360	3.0A; 600V
6-143	UT3010	3.0A; 100V	6-154	UTR4305	4.0A; 50V
6-143	UT3020	3.0A; 200V	6-154	UTR4310	4.0A; 100V
6-143	UT3040	3.0A; 400V	6-154	UTR4320	4.0A; 200V
6-143	UT3060	3.0A; 600V	6-154	UTR4340	4.0A; 400V
6-143	UT3080*	3.0A; 800V	6-154	UTR4350	4.0A; 500V
6-143	UT4005	4.0A; 50V	6-154	UTR4360	4.0A; 600V
6-143	UT4010 (1N5180)	4.0A; 100V	6-158	UTR4405	6.0A; 50V
6-143	UT4020	4.0A; 200V	6-158	UTR4410	6.0A; 100V
6-143	UT4040 (1N5207)	4.0A; 400V	6-158	UTR4420	6.0A; 200V
6-143	UT4060	4.0A; 600V	6-158	UTR4430	6.0A; 300V
*	UT4080	4.0A; 800V	6-158	UTR4440	6.0A; 400V
*	UT4100	4.0A; 1000V	6-158	UTR5405	7.5A; 50V
6-147	UT5105	7.5A; 50V	6-158	UTR5410	7.5A; 100V
6-147	UT5110	7.5A; 100V	6-158	UTR5420	7.5A; 200V
6-147	UT5120	7.5A; 200V	6-158	UTR5430	7.5A; 300V
6-147	UT5130	7.5A; 300V	6-158	UTR5440	7.5A; 400V
6-147	UT5140	7.5A; 400V	6-158	UTR6405	9.0A; 50V
6-147	UT5150	7.5A; 500V	6-158	UTR6410	9.0A; 100V
6-147	UT5160	7.5A; 600V	6-158	UTR6420	9.0A; 200V
6-147	UT6105	9.0A; 50V	6-158	UTR6430	9.0A; 300V
6-147	UT6110	9.0A; 100V	6-158	UTR6440	9.0A; 400V
6-147	UT6120	9.0A; 200V	6-161	UTX105	1.0A; 50V
6-147	UT6130	9.0A; 300V	6-161	UTX110	1.0A; 100V
6-147	UT6140	9.0A; 400V	6-161	UTX115	1.0A; 150V
6-147	UT6160	9.0A; 600V	6-161	UTX120	1.0A; 200V
6-147	UT8105	12.0A; 50V	6-161	UTX125	1.0A; 250V
6-147	UT8110	12.0A; 100V	6-161	UTX205	2.0A; 50V
6-147	UT8120	12.0A; 200V	6-161	UTX210	2.0A; 100V
6-147	UT8130	12.0A; 300V	6-161	UTX215	2.0A; 150V
6-147	UT8140	12.0A; 400V	6-161	UTX220	2.0A; 200V
6-147	UT8160	12.0A; 600V	6-161	UTX225	2.0A; 250V
6-150	UTR01	1.0A; 50V	6-164	UTX3105	3.0A; 50V
6-150	UTR02	2.0A; 50V	6-164	UTX3110	3.0A; 100V
6-150	UTR10	0.5A; 100V	6-164	UTX3115	3.0A; 150V
6-150	UTR11	1.0A; 100V	6-164	UTX3120	3.0A; 200V
6-150	UTR12	2.0A; 100V	*	UTX3125	3.0A; 250V
6-150	UTR20	0.5A; 200V	6-164	UTX4105	4.0A; 50V
6-150	UTR21	1.0A; 200V	6-164	UTX4110	4.0A; 100V
6-150	UTR22	2.0A; 200V	6-164	UTX4115	4.0A; 150V
6-150	UTR30	0.5A; 300V	6-164	UTX4120	4.0A; 200V
6-150	UTR31	1.0A; 300V	*	UTX4125	4.0A; 250V
6-150	UTR32	2.0A; 300V			ZENER
6-150	UTR40	0.5A; 400V	9-21	UZ110-UZ119	3W; 5%
6-150	UTR41	1.0A; 400V	9-21	UZ120-UZ140	3W; 5%
6-150	UTR42 (1N5206)	2.0A; 400V	9-21	UZ210-UZ219	3W; 10%
6-150	UTR50	0.5A; 500V	9-21	UZ220-UZ240	3W; 10%
6-150	UTR51	1.0A; 500V	9-21	UZ706-UZ760	3W; 5%
6-150	UTR52	2.0A; 500V	9-21	UZ770-UZ790	3W; 5%
6-150	UTR60	0.5A; 600V	9-21	UZ806-UZ860	3W; 10%
6-150	UTR61	1.0A; 600V	9-21	UZ870-UZ890	3W; 10%
6-150	UTR62	2.0A; 600V	9-23	UZ4110-UZ4120	5W; 5%
*	UTR70	0.5A; 700V	9-23	UZ4210-UZ4220	5W; 10%
*	UTR71	1.0A; 700V	9-23	UZ4706-UZ4791	5W; 5%
6-154	UTR2305	2.0A; 50V	9-23	UZ4806-UZ4891	5W; 10%
6-154	UTR2310	2.0A; 100V	9-25	UZ5110-UZ5119	5W; 5%
6-154	UTR2320	2.0A; 200V			

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		ZENER			
9-25	UZ5120	5W; 5%			
9-25	UZ5210-UZ5240	5W; 10%			
9-25	UZ5706-UZ5760	5W; 5%			
9-25	UZ5770-UZ5790	5W; 5%			
9-25	UZ5806-UZ5860	5W; 10%			
9-25	UZ5870-UZ5890	5W; 10%			
9-27	UZ7110	10W; 5%			
9-27	UZ7110L	6W; 5%			
9-27	UZ7210	10W; 10%			
9-27	UZ7210L	6W; 10%			
9-27	UZ7706-UZ7750	10W; 5%			
9-27	UZ7706L-UZ7750L	6W; 5%			
9-27	UZ7756-UZ7790	10W; 5%			
9-27	UZ7756L-UZ7790L	6W; 5%			
9-27	UZ7806-UZ7850	10W; 10%			
9-27	UZ7806L-UZ7850L	6W; 10%			
9-27	UZ7856-UZ7890	10W; 10%			
9-27	UZ7856L-UZ7890L	6W; 10%			
9-29	UZ8110-UZ8120	1W; 5%			
9-29	UZ8210-UZ8220	1W; 10%			
9-29	UZ8706-UZ8790	1W; 5%			
9-29	UZ8806-UZ8890	1W; 10%			
*	UZS306-UZS440	3W; 5%			
*	UZS506-UZS640	3W; 10%			

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POWER SUPPLY DESIGNERS' GUIDE

POWER HYBRIDS & MODULES

Circuit	Type	Output Current, Pk.	Input/Output Voltage	Polarity	Fall Time		On-State Voltage (V) @ (A)	Pkg.
					Volt. (ns)	Cur. (ns)		
	PIC600 PIC601 PIC602 PIC610 PIC611 PIC612	5A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	75	150	1.5 @ 2	4 PIN TO-66 (Isolated)
	PIC660 PIC661 PIC662 PIC670 PIC671 PIC672	10A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	150 250	250	1.5 @ 5	4 PIN TO-66 (Isolated)
	PIC625 PIC626 PIC627 PIC635 PIC636 PIC637	15A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	175 300	300	1.5 @ 7	4 PIN TO-66 (Isolated)
	PIC645 PIC646 PIC647 PIC655 PIC656 PIC657	20A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	150 300	300	1.5 @ 7	3 PIN TO-3
	PIC730 PIC740	30A	30 40	Pos. Pos.	350	300	1 @ 20	3 PIN TO-3
	PIC800 PIC801	8A	350 400	Pos.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)
	PIC810 PIC811	8A	350 400	Neg.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)

Type	Description	Key Features	Pkg.
PIC900 B, C, D	5A; 60V, 80V, 100V H-Bridge Hybrid Circuit	<ul style="list-style-type: none"> • Designed and Characterized for Inductive Loads as Stepper Motors, DC Motor Drives, Full Bridge DC Converters • Fast Switching Times with Low (5mA) Drive Current • Electrically Isolated 18-Pin Dip with Integral Heat Spreader • Compatible with Automatic Insertion 	18 PIN DIL with Integral Heat Spreader

POWER SUPPLY DESIGNERS' GUIDE

LINEAR INTEGRATED CIRCUITS

Pulse Width Modulators

TYPE	PERFORMANCE CHARACTERISTICS																	
	Voltage Reference ± 1%	Voltage Reference ± 1% Soft Start	Voltage Reference ± 1% PWM Latch	Under-Voltage Lockout	Reverse-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Uncommitted Oscillator	Single-Ended Output	Tolerant Output	Separate Output	Adjustable Oscillator Sync Terminal	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package
Regulating PWMs UC1524/2524/3524 UC1524/883B	X					X	100mA	300kHz	X									16 Pin DIP
Advanced Regulating PWMs UC1524A/2524A/3524A UC1524A/883B		X	X	X	X	X	200mA	500kHz	X						X			16 Pin DIP
Advanced Regulating PWMs UC1525A/2525A/3525A UC1525A/883B		X	X	X	X	X	100mA 0.4A Pulse	500kHz			X	X	X					16 Pin DIP
Advanced Regulating PWMs UC1527A/2527A/3527A UC1527A/883B		X	X	X	X	X	100mA 0.4A Pulse	500kHz			X	X	X					16 Pin DIP
Advanced Regulating PWMs UC1526/2526/3526 UC1526/883B		X	X	X	X	X	100mA	400kHz			X	X	X		X			18 Pin DIP
Regulating PWMs UC493/UC494/ UC495		X					200mA	300kHz	X				X		X			16 Pin DIP 18 Pin DIP
Advanced Regulating PWMs UC493A/UC493AC UC494A/UC494AC		X			X		200mA	300kHz	X			X			X			16 Pin DIP 18 Pin DIP
Current Mode PWM Controllers UC1846/2846/3846 UC1846/883B		X	X	X	X	X	200mA	500kHz			X	X	X	X	X			16 Pin DIP
Current Mode PWM Controllers UC1847/2847/3847 UC1847/883B		X	X	X	X	X	200mA	500kHz			X	X	X	X	X			16 Pin DIP
Programmable Primary Side PWMs UC1840/2840/3840 UC1840/883B		X	X	X	X	X	200mA	500kHz		X		X	X	N/A	X			18 Pin DIP
Programmable Primary Side PWMs UC1842/2842/3842 UC1842/883B		X		X	X	X	100mA 1A Pulse	500kHz		X		X		N/A	X			8 Pin DIP

POWER SUPPLY DESIGNERS' GUIDE

LINEAR INTEGRATED CIRCUITS

Power Supply Support Functions

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1543/2543/3543 UC1544/2544/3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	<ul style="list-style-type: none"> • Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC1544 series only) 	16 Pin DIL (1543 Series) 18 Pin DIL (1544 series)
UC1706/2706/3706	Dual High Current MOSFET Compatible Output Driver	<ul style="list-style-type: none"> • Dual, 1.5A, Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current 	16 Pin DIL
UC1834/2834/3834	High Efficiency Linear Regulator, Low Input-Output Differential	<ul style="list-style-type: none"> • Minimum $V_{IN}-V_{OUT}$ less than 0.5V at 5A Load with External Pass Device • Equally Usable for either Positive or Negative Regulator Design • Adjustable Low Threshold Current Sense Amplifier • Under- and Over-Voltage Fault Alert with Programmable Delay • Over-Voltage Fault Latch with 100mA Crowbar Drive Output 	16 Pin DIL
UC1901/2901/3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	<ul style="list-style-type: none"> • An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock 	14 Pin DIL
UC1903/2903/3903	Quad Supply and Line Monitor Precision System	<ul style="list-style-type: none"> • Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal Inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP 	18 Pin DIL

Functional Circuit

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1704/3704	Bridge Transducer Switch	<ul style="list-style-type: none"> • Dual Matched Current Sources • High-Gain Differential Sensing Circuit • Wide Common-Mode Input Capability • Complimentary Digital Open-Collector Outputs • Externally Programmable Time Delay • Optional Output Latch with Reset • Built-in Diagnostic Activation • Wide Supply Voltage Range • High Current Heater Power Source Driver 	16 Pin DIL

POWER SUPPLY DESIGNERS' GUIDE

LINEAR INTEGRATED CIRCUITS

Voltage Regulators

Three Terminal Voltage Regulators, Adjustable

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)	PACKAGE
UC117K/LM117K UC217K/LM217K *UC317K/LM317K	1.5A	Pos.	Adjustable from 1.2V to 37V	TO-3 TO-3 TO-3
UC137K/LM137K UC237K/LM237K *UC337K/LM337K	1.5A	Neg.	Adjustable from -1.2V to -37V	TO-3 TO-3 TO-3
UC150K/LM150K UC250K/LM250K *UC350K/LM350K	3.0A	Pos.	Adjustable from 1.2V to 33V	TO-3 TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Positive

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7800AK/LM140AK SERIES *UC7800ACK/LM340AK SERIES	1.5A	Pos.	5V ± 1%	12V ± 1%	15V ± 1%	TO-3 TO-3
UC7800K/LM140K SERIES *UC7800CK/LM340K SERIES	1.5A	Pos.	5V ± 4%	12V ± 4%	15V ± 4%	TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Negative

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7900AK/LM120K SERIES *UC7900ACK SERIES	1.5A	Neg.	-5V ± 1%	-12V ± 1%	-15V ± 1%	TO-3 TO-3
UC7900K SERIES *UC7900CK/LM320K SERIES	1.5A	Neg.	-5V ± 4%	-12V ± 4%	-15V ± 4%	TO-3 TO-3

* Also available in TO-220 package.

POWER SUPPLY DESIGNERS' GUIDE

N-CHANNEL POWER MOSFETS

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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
500	0.4	2N6770	7.75	12.0	48	150
500	0.4	UFN450	8.0	13.0	52	150
500	0.5	UFN452	7.0	12.0	48	150
500	0.85	UFN440	5.0	8.0	32	125
500	1.1	UFN442	4.0	7.0	28	125
500	1.5	2N6762	3.0	4.5	18	75
500	1.5	UFN430	3.0	4.5	18	75
500	2.0	UFN432	3.5	4.0	16	75
500	3.0	UFN420	1.5	2.5	10	40
500	4.0	UFN422	1.0	2.0	8	40
450	0.4	UFN451	8.0	13.0	52	150
450	0.5	2N6769	7.0	11.0	44	150
450	0.5	UFN453	7.0	12.0	48	150
450	0.85	UFN441	5.0	8.0	32	125
450	1.1	UFN443	4.0	7.0	28	125
450	1.5	UFN431	3.0	4.5	18	75
450	2.0	2N6761	2.5	4.0	16	75
450	2.0	UFN433	2.5	4.0	16	75
450	3.0	UFN421	1.5	2.5	10	40
450	4.0	UFN423	1.0	2.0	8	40
400	0.3	2N6768	9.0	14.0	56	150
400	0.3	UFN350	9.0	15.0	60	150
400	0.4	UFN352	8.0	13.0	52	150
400	0.55	UFN340	6.0	10.0	40	125
400	0.8	UFN342	5.0	8.0	32	125
400	1.0	2N6760	3.5	5.5	22	75
400	1.0	UFN330	3.5	5.5	22	75
400	1.5	UFN332	3.0	4.5	18	75
400	1.8	UFN320	2.0	3.0	12	40
400	2.5	UFN322	1.5	2.5	10	40
350	0.3	UFN351	9.0	15.0	60	150
350	0.4	2N6767	7.75	12.0	48	150
350	0.4	UFN353	8.0	13.0	52	150
350	0.55	UFN341	6.0	10.0	40	125
350	0.8	UFN343	5.0	8.0	32	125
350	1.0	UFN331	3.5	5.5	22	75
350	1.5	2N6759	3.0	4.5	18	75
350	1.5	UFN333	3.5	4.5	18	75
350	1.8	UFN321	2.0	3.0	12	40
350	2.5	UFN323	1.5	2.5	10	40



V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
200	0.085	2N6766	19.0	30.0	120	150
200	0.085	UFN250	19.0	30.0	120	150
200	0.12	UFN252	16.0	25.0	100	150
200	0.18	UFN240	11.0	18.0	72	125
200	0.22	UFN242	10.0	16.0	64	125
200	0.4	2N6758	6.0	9.0	36	75
200	0.4	UFN230	6.0	9.0	36	75
200	0.6	UFN232	5.0	8.0	32	75
200	0.8	UFN220	3.0	5.0	20	40
200	1.2	UFN222	2.5	4.0	16	40
150	0.085	UFN251	19.0	30.0	120	150
150	0.12	2N6765	16.0	25.0	100	150
150	0.12	UFN253	16.0	25.0	100	150
150	0.18	UFN241	11.0	18.0	72	125
150	0.22	UFN243	10.0	16.0	64	125
150	0.4	UFN231	6.0	9.0	36	75
150	0.6	2N6757	5.0	8.0	32	75
150	0.6	UFN233	5.0	8.0	32	75
150	0.8	UFN221	3.0	5.0	20	40
150	1.2	UFN223	2.5	4.0	16	40
100	0.055	2N6764	24.0	38.0	152	150
100	0.055	UFN150	25.0	40.0	160	150
100	0.08	UFN152	20.0	33.0	132	150
100	0.085	UFN140	17.0	27.0	108	125
100	0.11	UFN142	15.0	24.0	96	125
100	0.18	2N6756	9.0	14.0	56	75
100	0.18	UFN130	9.0	14.0	56	75
100	0.25	UFN132	8.0	12.0	48	75
100	0.3	UFN120	5.0	8.0	32	40
100	0.4	UFN122	4.0	7.0	28	40
60	0.055	UFN151	25.0	40.0	160	150
60	0.08	2N6763	20.0	31.0	124	150
60	0.08	UFN153	20.0	33.0	132	150
60	0.085	UFN141	17.0	27.0	108	125
60	0.11	UFN143	15.0	24.0	96	125
60	0.18	UFN131	9.0	14.0	56	75
60	0.25	2N6755	8.0	12.0	48	75
60	0.25	UFN133	8.0	12.0	48	75
60	0.3	UFN121	5.0	8.0	32	40
60	0.4	UFN123	4.0	7.0	28	40

POWER SUPPLY DESIGNERS' GUIDE

N-CHANNEL POWER MOSFETS

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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
500	0.85	UFN840	5.0	8.0	32	125
500	1.1	UFN842	4.0	7.0	28	125
500	1.5	UFN830	3.0	4.5	18	75
500	2.0	UFN832	2.5	4.0	16	75
500	3.0	UFN820	1.5	2.5	10	40
500	4.0	UFN822	1.0	2.0	8	40
450	0.85	UFN841	5.0	8.0	32	125
450	1.1	UFN843	4.0	7.0	28	125
450	1.5	UFN831	3.0	4.5	18	75
450	2.0	UFN833	2.5	4.0	16	75
450	3.0	UFN821	1.5	2.5	10	40
450	4.0	UFN823	1.0	2.0	8	40
400	0.55	UFN740	6.0	10.0	40	125
400	0.80	UFN742	5.0	8.0	32	125
400	1.0	UFN730	3.5	5.5	22	75
400	1.5	UFN732	3.0	4.5	18	75
400	1.8	UFN720	2.0	3.0	12	40
400	2.5	UFN722	1.5	2.5	10	40
400	3.6	UFN710	1.0	1.5	6	20
400	5.0	UFN712	0.8	1.3	5	20
350	0.55	UFN741	6.0	10.0	40	125
350	0.8	UFN743	5.0	8.0	32	125
350	1.0	UFN731	3.5	5.5	22	75
350	1.5	UFN733	3.0	4.5	18	75
350	1.8	UFN721	2.0	3.0	12	40
350	2.5	UFN723	1.5	2.5	10	40
350	3.6	UFN711	1.0	1.5	6	20
350	5.0	UFN713	0.8	1.3	5	20
200	0.18	UFN640	11.0	18.0	72	125
200	0.22	UFN642	10.0	16.0	64	125

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
200	0.4	UFN630	6.0	9.0	36	75
200	0.6	UFN632	5.0	8.0	32	75
200	0.8	UFN620	3.0	5.0	20	40
200	1.2	UFN622	2.5	4.0	16	40
200	1.5	UFN610	1.5	2.5	10	20
200	2.4	UFN612	1.25	2.0	8	20
150	0.18	UFN641	11.0	18.0	72	125
150	0.22	UFN643	10.0	16.0	64	125
150	0.4	UFN631	6.0	9.0	36	75
150	0.6	UFN633	5.0	8.0	32	75
150	0.8	UFN621	3.0	5.0	20	40
150	1.2	UFN623	2.5	4.0	16	40
150	1.5	UFN611	1.5	2.5	10	20
150	2.4	UFN613	1.25	2.0	8	20
100	0.085	UFN540	17.0	27.0	108	125
100	0.11	UFN542	15.0	24.0	96	125
100	0.18	UFN530	9.0	14.0	56	75
100	0.25	UFN532	8.0	12.0	48	75
100	0.3	UFN520	5.0	8.0	32	40
100	0.4	UFN522	4.0	7.0	28	40
100	0.6	UFN510	2.5	4.0	16	20
100	0.8	UFN512	2.0	3.5	14	20
60	0.085	UFN541	17.0	27.0	108	125
60	0.11	UFN543	15.0	24.0	96	125
60	0.18	UFN531	9.0	14.0	56	75
60	0.25	UFN533	8.0	12.0	48	75
60	0.3	UFN521	5.0	8.0	32	40
60	0.4	UFN523	4.0	7.0	28	40
60	0.6	UFN511	2.5	4.0	16	20
60	0.8	UFN513	2.0	3.5	14	20

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N-CHANNEL POWER MOSFETS

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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			100°C Case	25°C Case		
500	1.5	UFNF430	1.75	2.75	11	25
500	1.5	2N6802	1.5	2.5	11	25
500	2.0	UFNF432	1.5	2.25	9	25
500	3.0	UFNF420	1.0	1.6	6.5	20
500	3.0	2N6794	0.95	1.5	6.5	20
500	4.0	UFNF422	0.9	1.4	5.5	20
450	1.5	UFNF431	1.75	2.75	11	25
450	1.5	2N6801	1.5	2.5	11	25
450	2.0	UFNF433	1.5	2.25	9	25
450	3.0	UFNF421	1.0	1.6	6.5	20
450	3.0	2N6793	0.95	1.5	6.5	20
450	4.0	UFNF423	0.9	1.4	5.5	20
400	1.0	UFNF330	2.0	3.5	14	25
400	1.0	2N6800	1.6	3.0	14	25
400	1.5	UFNF332	1.6	3.0	12	25
400	1.8	UFNF320	1.45	2.5	10	20
400	1.8	2N6792	1.25	2.0	10	20
400	2.5	UFNF322	1.2	2.0	8	20
400	3.6	UFNF310	0.85	1.35	5.5	15
400	3.6	2N6786	0.80	1.25	5.5	15
400	5.0	UFNF312	0.70	1.15	4.5	15
350	1.0	UFNF331	2.0	3.5	14	25
350	1.0	2N6799	1.6	3.0	14	25
350	1.5	UFNF333	1.6	3.0	12	25
350	1.8	UFNF321	1.45	2.5	10	20
350	1.8	2N6791	1.25	2.0	10	20
350	2.5	UFNF323	1.2	2.0	8	20
350	3.6	UFNF311	0.85	1.35	5.5	15
350	3.6	2N6785	0.80	1.25	5.5	15
350	5.0	UFNF313	0.70	1.15	4.5	15
200	0.4	2FNF6798	3.5	5.5	22	25
200	0.4	UFNF230	3.5	5.5	22	25
200	0.6	UFNF232	2.8	4.5	18	25
200	0.8	2N6790	2.1	3.5	14	20
200	0.8	UFNF220	2.1	3.5	14	20
200	1.2	UFNF222	1.75	3.0	12	20
200	1.5	2N6784	1.45	2.25	9	15
200	1.5	UFNF210	1.4	2.2	9	15
200	2.4	UFNF212	1.1	1.8	7.5	15
150	0.4	2N6797	3.5	5.5	22	25
150	0.4	UFNF231	3.5	5.5	22	25
150	0.6	UFNF233	2.8	4.5	18	25
150	0.8	2N6789	2.1	3.5	14	20
150	0.8	UFNF221	2.1	3.5	14	20
150	1.2	UFNF223	1.75	3.0	12	20
150	1.5	2N6783	1.45	2.25	9	15
150	1.5	UFNF211	1.4	2.2	9	15
150	2.4	UFNF213	1.1	1.8	7.5	15
100	0.18	2N6796	5.0	8.0	32	25
100	0.18	UFNF130	5.0	8.0	32	25
100	0.25	UFNF132	4.5	7.0	28	25
100	0.3	2N6788	3.5	6.0	24	20
100	0.3	UFNF120	3.5	6.0	24	20
100	0.4	UFNF122	3.0	5.0	20	20

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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			100°C Case	25°C Case		
100	0.6	2N6782	2.25	3.5	14	15
100	0.6	UFNF110	2.25	3.5	14	15
100	0.8	UFNF112	2.0	3.0	12	15
60	0.18	2N6795	5.0	8.0	32	25
60	0.18	UFNF131	5.0	8.0	32	25
60	0.25	UFNF133	4.5	7.0	28	25
60	0.3	2N6787	3.5	6.0	24	20
60	0.3	UFNF121	3.5	6.0	24	20
60	0.4	UFNF123	3.0	5.0	20	20
60	0.6	2N6781	2.25	3.5	14	15
60	0.6	UFNF111	2.25	3.5	14	15
60	0.8	UFNF113	2.0	3.0	12	15

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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)	I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			25°C Case		
100	1.5	UFNA12	1.0	2.0	2.4
60	1.5	UFNA11	1.0	2.0	2.4

4 PIN DIP

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)	I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			25°C Case		
200	1.5	UFND210	0.6	2.5	1.0
150	2.4	UFND213	0.45	1.8	1.0
100	0.3	UFND120	1.3	5.2	1.0
100	0.6	UFND110	1.0	4.0	1.0
100	2.4	UFND120	0.5	2.0	1.0
60	0.4	UFND123	1.1	4.4	1.0
60	0.8	UFND113	0.8	3.0	1.0
60	3.2	UFND123	0.4	1.5	1.0

POWER SUPPLY DESIGNERS' GUIDE

NPN POWER SWITCHING TRANSISTORS

Plastic Packaging

Type	V _{CE(sat)} (V)	Min. h _{FE} @ I _C	Max. V _{CE(sat)} @ I _C (V)	Max. Switching Time (μs) @ I _C (A)				Pkg.
				t _r	t _s	t _f	@ I _C	
3.0A								
UMT1203 UMT1204	300 400	7 @ 2.0 7 @ 2.0	1.2 @ 2.0 1.2 @ 2.0	1.0 1.0	4.0 4.0	0.7 0.7	2.0 2.0	TO-220 TO-220
4.0A								
UMT13004 UMT13005	300 400	8 @ 2.0 8 @ 2.0	0.6 @ 2.0 0.6 @ 2.0	0.7 0.7	3.5 3.5	0.9 0.9	2.0 2.0	TO-220 TO-220
8.0A								
UMT13006 UMT13007	300 400	6 @ 5.0 6 @ 5.0	1.5 @ 5.0 1.5 @ 5.0	1.0 1.0	3.0 3.0	0.7 0.7	5.0 5.0	TO-220 TO-220
12.0A								
UMT13008 UMT13009	300 400	6 @ 8.0 6 @ 8.0	1.5 @ 8.0 1.5 @ 8.0	1.0 1.0	3.0 3.0	0.7 0.7	8.0 8.0	TO-220 TO-220

POWER SUPPLY DESIGNERS' GUIDE

NPN POWER SWITCHING TRANSISTORS (continued)

Metal Can Packaging

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Type	V _{CE(sat)} (V)	Min. h _{FE} @ I _C	Max. V _{CE(sat)} @ I _C (V)	Max. Switching Time (μs) @ I _C (A)				Pkg.
				t _r	t _s	t _f	@ I _C	
3.0A								
2N5838	250	10 @ 2.0	1.0 @ 3.0	1.5	3.0	1.5	3.0	TO-3
2N5839	275	10 @ 2.0	1.5 @ 2.0	1.5	3.75	1.5	2.0	TO-3
2N5840	350	10 @ 2.0	1.5 @ 2.0	1.7	3.75	1.5	2.0	TO-3
5.0A								
2N6542	300	7 @ 3.0	1.0 @ 3.0	0.7	4.0	0.8	3.0	TO-3
2N6671	300	10 @ 5.0	1.0 @ 5.0	0.5	2.5	0.4	5.0	TO-3
UMT1006	350	7 @ 3.0	1.0 @ 3.0	0.4	4.0	0.4	3.0	TO-3
2N6672	350	10 @ 5.0	1.0 @ 5.0	0.5	2.5	0.4	5.0	TO-3
UMT1007	400	7 @ 3.0	1.0 @ 3.0	0.4	4.0	0.4	3.0	TO-3
2N6543	400	7 @ 3.0	1.0 @ 3.0	0.7	4.0	0.8	3.0	TO-3
2N6673	400	10 @ 5.0	1.0 @ 5.0	0.5	2.5	0.4	5.0	TO-3
8.0A								
2N6306	250	15 @ 3.0	0.8 @ 3.0	0.6	1.6	0.4	3.0	TO-3
2N6307	300	15 @ 3.0	0.8 @ 3.0	0.6	1.6	0.4	3.0	TO-3
2N6544	300	7 @ 5.0	1.5 @ 5.0	1.0	4.0	1.0	5.0	TO-3
UMT1008	300	7 @ 5.0	1.5 @ 5.0	0.4	4.0	0.4	5.0	TO-3
2N6308	350	12 @ 3.0	1.5 @ 3.0	0.6	1.6	0.4	3.0	TO-3
2N6545	400	7 @ 5.0	1.5 @ 5.0	1.0	4.0	1.0	5.0	TO-3
UMT1009	400	7 @ 5.0	1.5 @ 5.0	0.4	4.0	0.4	5.0	TO-3
10.0A								
2N6354	120	10 @ 10.0	1.0 @ 10.0	0.3	1.0	0.2	5.0	TO-3
2N6249	200	10 @ 10.0	1.5 @ 10.0	2.0	3.5	1.0	10.0	TO-3
2N6250	275	8 @ 10.0	1.5 @ 10.0	2.0	3.5	1.0	10.0	TO-3
2N6674	300	8 @ 10.0	1.0 @ 10.0	0.6	2.5	0.5	10.0	TO-3
2N6251	350	6 @ 10.0	1.5 @ 10.0	2.0	3.5	1.0	10.0	TO-3
2N6675	400	8 @ 10.0	1.0 @ 10.0	0.6	2.5	0.5	10.0	TO-3
15.0A								
2N6496	100	12 @ 8.0	1.0 @ 8.0	0.5	1.5	0.5	8.0	TO-3
2N6546	300	6 @ 10.0	1.5 @ 10.0	0.7	4.0	0.7	10.0	TO-3
2N6676	300	8 @ 15.0	1.0 @ 15.0	0.6	2.5	0.5	15.0	TO-3
UMT1011	350	6 @ 10.0	1.0 @ 10.0	0.4	4.0	0.4	10.0	TO-3
2N6677	350	8 @ 15.0	1.0 @ 15.0	0.6	2.5	0.5	15.0	TO-3
UMT1012	400	6 @ 10.0	1.0 @ 10.0	0.4	4.0	0.4	10.0	TO-3
2N6547	400	6 @ 10.0	1.5 @ 10.0	0.7	4.0	0.7	10.0	TO-3
2N6678	400	8 @ 15.0	1.0 @ 15.0	0.6	2.5	0.5	15.0	TO-3
UMT2000	450	7 @ 15.0	1.5 @ 10.0	0.22	0.9	0.2	10.0	TO-3
20.0A								
2N5039	75	20 @ 10.0	1.0 @ 10.0	0.5 ⁽¹⁾	—	0.5 ⁽²⁾	10.0	TO-3
2N5038	90	20 @ 12.0	1.2 @ 12.0	0.5 ⁽¹⁾	—	0.5 ⁽²⁾	12.0	TO-3
30.0A								
2N5671	90	20 @ 15.0	0.75 @ 15.0	0.5	1.5	0.5	15.0	TO-3
2N5672	120	20 @ 15.0	0.75 @ 15.0	0.5	1.5	0.5	15.0	TO-3
UMT2003	400	10 @ 15.0	1.5 @ 20.0	1.0	3.0	0.8	20.0	TO-3

⁽¹⁾Turn-on Time

⁽²⁾Turn-off Time

POWER SUPPLY DESIGNERS' GUIDE

SCHOTTKY BARRIER POWER RECTIFIERS

Type	V _{RRM}	V _F @ I _F [*] (V)	I _R @ V _{RRM} [*] (mA)	Peak Reverse Transient Current (A)	Pkg.
1A					
1N5817 1N5818 1N5819	20V 30V 40V	0.45 @ 1A 0.55 @ 1A 0.60 @ 1A	10.0	N/A	Axial Leaded Plastic
USD1120 USD1130 USD1140	20V 30V 40V	0.450 @ 1A 0.475 @ 1A 0.500 @ 1A	10.0	N/A	Axial Leaded Plastic
3A					
1N5820 1N5821 1N5822	20V 30V 40V	0.475 @ 3A 0.500 @ 3A 0.525 @ 3A	20.0	N/A	Axial Leaded Plastic
6A					
USD620 USD635 USD640 USD645	20V 35V 40V 45V	0.48 @ 6A	50.0	1.0	TO-220AC (2 Lead)
8A					
USD720 USD735 USD740 USD745	20V 35V 40V 45V	0.48 @ 8A	50.0	1.0	TO-220AC (2 Lead)
12A					
USD820 USD835 USD840 USD845	20V 35V 40V 45V	0.51 @ 12A	50.0	1.0	TO-220AC (2 Lead)
16A					
USD920 USD935 USD940 USD945	20V 35V 40V 45V	0.53 @ 16A	50.0	2.0	TO-220AC (2 Lead)
50A					
1N6097 1N6098	30V 40V	0.86 @ 157A	250.0	2.0	DO-5 (DO-223AB)
60A					
SD51	45V @ T _J = 25°C 35V @ T _J = 125°C	0.6 @ 60A	200.0 @ 35V	2.0	DO-5 (DO-223AB)
75A					
USD520 USD535 USD545 USD550	20V 35V 45V 50V	0.6 @ 60A	50.0 75.0	2.0	DO-5 (DO-223AB)

*Elevated Temperature

POWER SUPPLY DESIGNERS' GUIDE

SCHOTTKY BARRIER POWER RECTIFIERS (continued)

Schottky Center-Tap Rectifiers

Type	V_{RWM}	$V_F @ I_F$ (V)	$I_R @ V_{RWM}$ (mA)	Peak Reverse Transient Current (A)	Pkg.
12A					
USD620C USD635C USD640C USD645C	20V 35V 40V 45V	0.6 @ 12A	50.0	1.0	TO-220AB
16A					
USD720C USD735C USD740C USD745C	20V 35V 40V 45V	0.6 @ 16A	50.0	1.0	TO-220AB
30A					
USD320C USD335C USD345C	20V 35V 45V	0.6 @ 20A	50.0	2.0	TO-3 Center-Tap
SD241	45V @ $T_J = 25^\circ\text{C}$ 35V @ $T_J = 125^\circ\text{C}$	0.6 @ 20A	100.0 @ 35V	2.0	TO-3 Center-Tap
100A					
USM140C USM145C USM150C	40V 45V 50V	0.63 @ 60A	75.0	2.0	TO-3 Base (Top Connector Module)
200A					
USM20040C USM20045C USM20050C	40V 45V 50V	0.64 @ 100A	125.0	2.0	M2 Power Block (see datasheet)

POWER SUPPLY DESIGNERS' GUIDE

P/N JUNCTION RECTIFIERS

Low Voltage, Ultra-Fast Recovery ($t_{rr} \leq 50\text{ns}$)

Type	V_{RWM}	$V_F @ I_F^*$ (V)	$I_R @ V_{RWM}^*$ (mA)	t_{rr} (ns)	Pkg.
1A					
UES1001 UES1002 UES1003	50V 100V 150V	.895 @ 1A	0.05	25	Axial Leaded Glass
2.5A					
UES1101 UES1102 UES1103	50V 100V 150V	.895 @ 2A	0.05	25	Axial Leaded Glass
6A					
UES1301 UES1302 UES1303	50V 100V 150V	.850 @ 6A	0.15	30	Axial Leaded Glass
8A					
UES1401 UES1402 UES1403 UES1404	50V 100V 150V 200V	.895 @ 8A	0.15 0.15 0.15 0.50	35	TO-220AC (2 Lead)
16A					
UES1501 UES1502 UES1503 UES1504	50V 100V 150V 200V	.830 @ 16A	0.80 0.80 0.80 1.00	35	TO-220AC (2 Lead)
25A					
UES701 UES702 UES703	50V 100V 150V	.825 @ 25A	4.0	35	DO-4 (DO-203AA)
70A					
UES801 UES802 UES803	50V 100V 150V	.840 @ 70A	30.0	50	DO-5 (DO-203AB)

High Voltage, Ultra-Fast Recovery ($t_{rr} \leq 50\text{ns}$)

Type	V_{RWM}	$V_F @ I_F^*$ (V)	$I_R @ V_{RWM}^*$ (mA)	t_{rr} (ns)	Pkg.
2A					
UES1104 UES1105 UES1106	200V 300V 400V	1.15 @ 1A	0.20	50	Axial Leaded Glass
5A					
UES1304 UES1305 UES1306	200V 300V 400V	1.15 @ 3A	0.50	50	Axial Leaded Glass
20A					
UES704 UES705 UES706	200V 300V 400V	1.15 @ 20A	10.0	50	DO-4 (DO-203AA)
50A					
UES804 UES805 UES806	200V 300V 400V	1.15 @ 50A	30.0	50	DO-5 (DO-203AB)

*Elevated Temperature

POWER SUPPLY DESIGNERS' GUIDE

P/N JUNCTION RECTIFIERS (continued) Ultra-Fast Recovery Center-Tap Rectifiers ($t_{rr} \leq 50\text{ns}$)

Type	V_{RWM}	$V_F @ I_F^*$ (V)	$I_R @ V_{RWM}^*$ (mA)	t_{rr} (ns)	Pkg.
16A					
UES2401	50V	.895 @ 8A	0.15	35	TO-220AB
UES2402	100V		0.15		
UES2403	150V		0.15		
UES2404	200V		0.50		
30A					
UES2601	50V	.825 @ 15A	4.0	35	TO-3 Center-Tap
UES2602	100V				
UES2603	150V				
UES2604	200V	1.15 @ 15A	10.0	50	TO-3 Center-Tap
UES2605	300V				
UES2606	400V				

Super-Fast Recovery Rectifiers ($t_{rr} = 100\text{ns}$)

Type	V_{RWM}	$V_F @ I_F$ (V)	$I_R @ V_{RWM}$ (mA)	t_{rr} (ns)	Pkg.
2A					
SES5001	50V	.895 @ 1A		100	Axial Leaded Glass
SES5002	100V				
SES5003	150V				
5A					
SES5301	50V	.895 @ 5A	.15	100	Axial Leaded Glass
SES5302	100V				
SES5303	150V				
8A					
SES5401	50V	.945 @ 8A	.15	100	TO-220AC (2 Lead)
SES5402	100V		.05		
SES5403	150V				
SES5504	200V				
20A					
SES5701	50V	.830 @ 20A	4.0	100	DO-4 (DO-203AA)
SES5702	100V				
SES5703	150V				
60A					
SES5801	50V	.850 @ 60A	30.0	100	DO-5 DO-203AB
SES5802	100V				
SES5803	150V				

Type	V_{RWM}	$V_F @ I_F$ (V)	$I_R @ V_{RWM}$ (mA)	t_{rr} (ns)	Pkg.
16A					
SES5401C	50V	.945 @ 8A	.15	100	TO-220AB
SES5402C	100V				
SES5403C	150V				
SES5404C	200V				
25A					
SES5601C	50V	.830 @ 12.5A	4.0	100	TO-3 Center-Tap
SES5602C	100V				
SES5603C	150V				

*Elevated Temperature

MOTOR CONTROL DESIGNERS' GUIDE

Motor Control Circuits

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
L292	2A, 36V, 30KHz, H-Bridge Motor Driver	<ul style="list-style-type: none"> • External Loop Adjustment • Single Power Supply (18-36V) • Input Signal Symmetric to Ground • Thermal Protection 	15 Pin Power SIP
L293/293E	Four Channel Push-Pull Drivers for Inductive Loads	<ul style="list-style-type: none"> • 1A Output per Channel (2A peak non-repetitive) • Supply Voltage to 36V • Inhibiting Facility • Thermal Protection • High Noise Immunity • E-Version Provides for External Emitter Sense Resistors • Compatible with Standard TTL Logic Inputs 	L293 16 Pin "Batwing" Dip L293E 20 Pin "Batwing" Dip
L295	Dual PWM Solenoid Driver and Stepper Motor Driver	<ul style="list-style-type: none"> • 3A Peak Current Per Driver • Supply Voltage to 40V • Current Limiting • Thermal Protection • Compatible with Standard TTL Logic Inputs 	15 Pin Power SIP
PIC900 B, C, D	5A; 60V, 80V, 100V H-Bridge Hybrid Circuit	<ul style="list-style-type: none"> • Designed and Characterized for Inductive Loads as Stepper Motors, DC Motor Drives, Full Bridge DC Converters • Fast Switching Times with Low (5mA) Drive Current • Electrically Isolated 18-Pin Dip with Integral Heat Spreader • Compatible with Automatic Insertion 	18 Pin DIL with Integral Heat Spreader
UC1637/2637/3637	Switched Mode Controller for DC Motor Drive	<ul style="list-style-type: none"> • Single or Dual Supply Operation • ± 2.5 to $\pm 20V$ Input Supply Range • $\pm 5\%$ Initial Oscillator Accuracy; $\pm 10\%$ Over Temperature • Pulse-by-Pulse Current Limiting • Under-Voltage Lockout • Uncommitted PWM Comparators for Design Flexibility 	18 Pin Dip
UC1717/UC3717	Stepper Motor Drive Circuit	<ul style="list-style-type: none"> • Half-Step and Full-Step Mode • Bipolar Constant Current Chopper Drive • Built-In Protection Diodes (Schottky) • Wipe Range of Current Control 5-1000mA • Wide Voltage Range 10-45V • Designed for Unregulated Motor Supply Voltage • Thermal Overload Protection 	16 Pin Dip

Note: U2TA506, 8 & 10 and U2TA606, 8 & 10 TO-92 Darlington's are appropriate for driving DC brushless motors and other inductive loads.

MILITARY DESIGNERS' GUIDE

SILICON RECTIFIERS Schottky

TYPE	OUTPUT CURRENT	V _{RWM}	MAXIMUM FORWARD VOLTAGE At T _c = 25°C	MAXIMUM REVERSE CURRENT At T _j = 125°C	PACKAGE	MIL-S-19500
1N6391	25A	45V	0.44V @ 5A (pk)	15mA @ 45V (pk)	DO-4	/553*
1N6392	60A	45V	0.47V @ 10A (pk)	20mA @ 45V (pk)	DO-5	/554*

* Series available as JAN, JANTX and JANTXV

High Efficiency, Fast Switching

TYPE	OUTPUT CURRENT	V _{RWM}	MAXIMUM FORWARD VOLTAGE	REVERSE RECOVERY TIME	PACKAGE	MIL-S-19500
1N5802	2.5A	50V	.875V	25ns	Axial	/477*
1N5804		100V	@		Axial	/477
1N5806		150V	1A		Axial	/477
1N5807	6.0A	50V	.875V	30ns	Axial	/477*
1N5809		100V	@		Axial	/477
1N5811		150V	4A		Axial	/477
1N5812	20A	50V	.900V	35ns	DO-4	/478*
1N5814		100V	@		DO-4	/478
1N5816		150V	10A		DO-4	/478
1N6304	70A	50V	.975V	50ns	DO-5	/550*
1N6305		100V	@		DO-5	/550
1N6306		150V	70A		DO-5	/550

* Series available as JAN, JANTX and JANTXV

General Purpose, Fast Recovery

TYPE	OUTPUT CURRENT	V _{RWM}	MAXIMUM FORWARD VOLTAGE	REVERSE RECOVERY TIME	PACKAGE	MIL-S-19500
1N4942	1A	200V	1.3V @ 1A	150ns	Axial	/359*
1N4944	1A	400V	1.3V @ 1A	150ns	Axial	/359
1N4946	1A	600V	1.3V @ 1A	250ns	Axial	/359
1N5615	1A	200V	1.6V @ 3A	150ns	Axial	/429*
1N5617	1A	400V	1.6V @ 3A	250ns	Axial	/429
1N5619	1A	600V	1.6V @ 3A	250ns	Axial	/429
1N5186	3A	100V	1.5V @ 9A	150ns	Axial	/424**
1N5187	3A	200V	1.5V @ 9A	200ns	Axial	/424
1N5188	3A	400V	1.5V @ 9A	250ns	Axial	/424
1N5189	3A	600V	1.5V @ 9A	400ns	Axial	/424
1N5415	3A	50V	1.5V @ 9A	150ns	Axial	/411*
1N5416	3A	100V	1.5V @ 9A	150ns	Axial	/411
1N5417	3A	200V	1.5V @ 9A	150ns	Axial	/411
1N5418	3A	400V	1.5V @ 9A	150ns	Axial	/411
1N5419	3A	500V	1.5V @ 9A	250ns	Axial	/411
1N5420	3A	600V	1.5V @ 9A	400ns	Axial	/411

* Series available as JAN, JANTX and JANTXV

** Series available as JAN and JANTX

MILITARY DESIGNERS' GUIDE

SILICON RECTIFIERS (continued)

General Purpose, Standard Recovery

TYPE	OUTPUT CURRENT	V_{RWM}	MAXIMUM FORWARD VOLTAGE	SURGE CURRENT	PACKAGE	MIL-S-19500
1N457	75mA	60V	1.0V @ 20mA	225mA	DO-7	/193***
1N458	55mA	125V	1.0V @ 7mA	165mA	DO-7	/193
1N459	40mA	175V	1.0V @ 3mA	120mA	DO-7	/193
1N483B	200mA	70V	1.0V @ 100mA	2A	DO-7	/118**
1N485B	200mA	180V	1.0V @ 100mA	2A	DO-7	/118
1N643	40mA	175V	1.0V @ 10mA	500mA	DO-7	/256***
1N645	400mA	270V	1.0V @ 400mA	5A	DO-7	/240**
1N645-1	400mA	270V	1.0V @ 400mA	5A	DO-35	/240*
1N647	400mA	480V	1.0V @ 400mA	5A	DO-7	/240**
1N647-1	400mA	480V	1.0V @ 400mA	5A	DO-35	/240*
1N4245	1A	200V	1.3V @ 3A	25A	Axial	/286*
1N4246	1A	400V	1.3V @ 3A	25A	Axial	/286
1N4247	1A	600V	1.3V @ 3A	25A	Axial	/286
1N4248	1A	800V	1.3V @ 3A	25A	Axial	/286
1N4249	1A	1000V	1.3V @ 3A	25A	Axial	/286
1N5614	1A	200V	1.3V @ 3A	30A	Axial	/427*
1N5616	1A	400V	1.3V @ 3A	30A	Axial	/427
1N5618	1A	600V	1.3V @ 3A	30A	Axial	/427
1N5620	1A	800V	1.3V @ 3A	30A	Axial	/427
1N3611	2A	200V	1.1V @ 1A	20A	Axial	/228**
1N3612	2A	400V	1.1V @ 1A	20A	Axial	/228
1N3613	2A	600V	1.1V @ 1A	20A	Axial	/228
1N3614	2A	800V	1.1V @ 1A	20A	Axial	/228
1N5550	3A	200V	1.2V @ 9A	100A	Axial	/420*
1N5551	3A	400V	1.2V @ 9A	100A	Axial	/420
1N5552	3A	600V	1.2V @ 9A	100A	Axial	/420
1N5553	3A	800V	1.2V @ 9A	100A	Axial	/420

* Series available as JAN, JANTX and JANTXV

** Series available as JAN and JANTX

*** Series available as JAN only

Radiation Tolerant Rectifiers

TYPE	OUTPUT CURRENT	PIV	MAXIMUM FORWARD VOLTAGE	SURGE CURRENT	MAXIMUM RADIATION TOLERANCE	PACKAGE
UR105	1A	50V	1.0 @ 0.5A	20A	>10 ¹⁴	Axial
UR110	1A	100V	1.0 @ 0.5A	20A	>10 ¹⁴	Axial
UR115	1A	150V	1.0 @ 0.5A	20A	>10 ¹⁴	Axial
UR120	1A	200V	1.0 @ 0.5A	20A	>10 ¹⁴	Axial
UR125	1A	250V	1.0 @ 0.5A	20A	>10 ¹⁴	Axial
UR205	2A	50V	1.0 @ 1A	25A	>10 ¹⁴	Axial
UR210	2A	100V	1.0 @ 1A	25A	>10 ¹⁴	Axial
UR215	2A	150V	1.0 @ 1A	25A	>10 ¹⁴	Axial
UR220	2A	200V	1.0 @ 1A	25A	>10 ¹⁴	Axial
UR225	2A	250V	1.0 @ 1A	25A	>10 ¹⁴	Axial

High Efficiency, Center-Tap Rectifiers and Doublers

TYPE	V_{RWM}	MAXIMUM FORWARD VOLTAGE	REVERSE RECOVERY TIME	OUTPUT CURRENT	SURGE CURRENT	PACKAGE
UES2601	50V	.930V	35ns	30A	400A	TO-3
UES2602	100V	@				TO-3
UES2603	150V	15A				TO-3
UES2604	200V	1.15V	50ns	30A	400A	TO-3
UES2605	300V	@				TO-3
UES2606	400V	15A				TO-3

MILITARY DESIGNERS' GUIDE

SWITCHING DIODES

Low Current

TYPE	OUTPUT CURRENT	V _{RWM}	MAXIMUM FORWARD VOLTAGE	REVERSE RECOVERY TIME	PACKAGE	MIL-S-19500
1N251	14mA	40V	1.0V @ 5mA	30ns	DO-7	/188***
1N662	40mA	80V	1.0V @ 10mA	500ns	DO-7	/256***
1N663	100mA	80V	1.0V @ 100mA	500ns	DO-7	/256***
1N914	75mA	100V	1.0V @ 10mA	5ns	DO-35	/116**
1N3064	75mA	75V	1.0V @ 10mA	4ns	DO-7	/144**
1N3070	200mA	200V	1.0V @ 100mA	50ns	DO-35	/169**
1N3595	150mA	150V	.80V @ 10mA	3μs	DO-7	/241*
1N3600	200mA	75V	.74V @ 10mA	4ns	DO-7	/231*
1N4148	150mA	100V	1.0V @ 10mA	5ns	DO-35	/116*
1N4148-1	150mA	100V	1.0V @ 10mA	5ns	DO-35	/116*
1N4150-1	200mA	75V	.74V @ 10mA	4ns	DO-35	/231*
1N4153	150mA	75V	.88V @ 20mA	4ns	DO-35	/337*
1N4153-1	150mA	75V	.88V @ 20mA	4ns	DO-35	/337*
1N4454	200mA	75V	1.0V @ 10mA	4ns	DO-35	/144*
1N4454-1	200mA	75V	1.0V @ 10mA	4ns	DO-35	/144*
1N4500	300mA	80V	.77V @ 20mA	6ns	DO-35	/403*
1N4531	125mA	100V	1.0V @ 10mA	8ns	DO-34	/116*
1N4532	125mA	75V	1.0V @ 10mA	4ns	DO-34	/144*
1N4534	150mA	75V	.88V @ 20mA	4ns	DO-34	/337*
1N4938	150mA	250V	1.0V @ 100mA	50ns	DO-7	/169**
1N4938-1	150mA	250V	1.0V @ 100mA	50ns	DO-7	/169**

- * Series available as JAN, JANTX and JANTXV
- ** Series available as JAN and JANTX
- *** Series available as JAN only

SWITCHING REGULATOR POWER OUTPUT CIRCUITS

TYPE	OUTPUT CURRENT, PK.	INPUT/OUTPUT VOLTAGE	POLARITY	FALL-TIME CURRENT		ON-STATE VOLT. @ CURR. (V) @ (I)	PACKAGE
				VOLTAGE (V)	CURRENT (ns)		
PIC600 PIC601 PIC602 PIC610 PIC611 PIC612	5A	60V 80V 100V 60V 80V 100V	Pos. Pos. Pos. Neg. Neg. Neg.	75	150	1.5 @ 2	4 PIN TO-66 (Isolated)
PIC625 PIC626 PIC627 PIC635 PIC636 PIC637	15A	60V 80V 100V 60V 80V 100V	Pos. Pos. Pos. Neg. Neg. Neg.	175 300	300	1.5 @ 7	4 PIN TO-66 (Isolated)
PIC645 PIC646 PIC647 PIC655 PIC656 PIC657	20A	60V 80V 100V 60V 80V 100V	Pos. Pos. Pos. Neg. Neg. Neg.	150 300	300	1.5 @ 7	3 PIN TO-3
PIC730 PIC740	30A	30V 40V	Pos. Pos.	350	300	1.0 @ 20	3 PIN TO-3
PIC800 PIC801	8A	350V 400V	Pos. Pos.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)
PIC810 PIC811	8A	350V 400V	Neg. Neg.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)

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LINEAR INTEGRATED CIRCUITS Pulse Width Modulators

TYPE	PERFORMANCE CHARACTERISTICS																	
	Voltage Reference ± 4%	Voltage Reference ± 1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feet Forward	Maximum Frequency Oscillator	Dual Uncommitted Outputs	Single Ended Output	Totem Pole Output	Separate Oscillators	Adjustable Oscillator Sync Terminal	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up
Regulating PWMs UC1524 UC1524/883B	X						X	100mA	300kHz	X								
Advanced Regulating PWMs UC1524A UC1524A/883B	X	X	X	X	X	X		200mA	500kHz	X								X
Advanced Regulating PWMs UC1525A UC1525A/883B	X	X	X	X	X	X		100mA 0.4A Pulse	500kHz		X	X	X					
Advanced Regulating PWMs UC1527A UC1527A/883B	X	X	X	X	X	X		100mA 0.4A Pulse	500kHz		X	X	X					
Advanced Regulating PWMs UC1526 UC1526/883B	X	X	X	X	X	X		100mA	400kHz		X	X	X					X
Advanced Regulating PWMs UC493A/UC494A/UC495A* UC493AC/UC494AC/UC495AC* UC495B/UC495BC	X		X	X				200mA	300kHz	X			X					X
Current Mode PWM Controllers UC1846 UC1846/883B	X	X	X	X	X	X		200mA	X	500kHz		X	X	X	X	X		
Current Mode PWM Controllers UC1847 UC1847/883B	X	X	X	X	X	X		200mA	X	500kHz		X	X	X	X	X		
Programmable Primary Side PWMs UC1840 UC1840/883B	X	X	X	X	X	X		200mA	X	500kHz	X		X	X	N/A			X
Programmable Primary Side PWMs UC1842 UC1842/883B	X		X	X	X			100mA 1A Pulse	X	500kHz	X		X		N/A			X

*Available with 883B screening.

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LINEAR INTEGRATED CIRCUITS (continued)

Three Terminal Voltage Regulators, Adjustable*

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC117K UC217K UC317K	1.5A	Pos.	Adjustable from 1.2V to 37V			TO-3 TO-3 TO-3
UC137K UC237K UC337K	1.5A	Neg.	Adjustable from -1.2V to -37V			TO-3 TO-3 TO-3
UC150K UC250K UC350K	3.0A	Pos.	Adjustable from 1.2V to 33V			TO-3 TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Positive*

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7800AK SERIES UC7800ACK SERIES	1.5A	Pos.	5V ± 1%	12V ± 1%	15V ± 1%	TO-3 TO-3
UC7800K SERIES UC7800CK SERIES	1.5A	Pos.	5V ± 4%	12V ± 4%	15V ± 4%	TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Negative*

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7900AK SERIES UC7900ACK SERIES	1.5A	Neg.	-5V ± 1%	-12V ± 1%	-15V ± 1%	TO-3 TO-3
UC7900K SERIES UC7900CK SERIES	1.5A	Neg.	-5V ± 4%	-12V ± 4%	-15V ± 4%	TO-3 TO-3

*MIL-STD-883 Screening

Unitrode offers all of the above devices screened to MIL-STD-883, customer requirements, and will perform tests as specified by MIL-M-38510.

When ordering MIL-STD-883 Screening, specify:

- Prime electrical and military temperature range, generic part number and package type
- Class of 883 screening (class A, B or C)

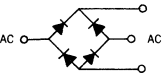
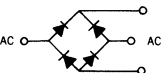
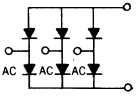
MIL-STD-883 Screening Tests

- Internal Visual Pre or Post Cap
- Stabilization Bake
- Temperature Cycling
- Constant Acceleration
- Hermeticity
 - a) Fine
 - b) Gross
- Pre-Burn-in Electrical Test
- Burn-in Test
- Final Electrical Test
 - a) DC @ 25°C
 - b) DC @ Max. and Min. Rated Temperature
 - c) Dynamic @ 25°C
 - d) Functional @ 25°C
- Radiographic
- Qualification and Quality Conformance Testing
- External Visual

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BRIDGE RECTIFIERS

40Hz - 5kHz

TYPE	CONFIGURATION	OUTPUT CURRENT	REVERSE VOLTAGE	SPECIFICATIONS	MIL-S-19500
469-1 469-2 469-3	Single Phase 	10A	200V 400V 600V	$V_F @ 15.7A, 1.35V \text{ Max.}$ $I_R @ V_R, 2\mu A \text{ Max.}$ $I_{SURGE}, 100A$	/469*
SPA25 SPB25 SPC25 SPD25	Single Phase 	25A	100V 200V 400V 600V	$V_F @ 39A, 1.4V \text{ Max.}$ $I_R @ V_R, 2\mu A \text{ Max.}$ $I_{SURGE}, 150A$	/446*
483-1 483-2 483-3	Three Phase 	25A	200V 400V 600V	$V_F @ 39A, 1.3V \text{ Max.}$ $I_R @ V_R, 3\mu A \text{ Max.}$ $I_{SURGE}, 150A$	/483**

* Series available as JAN and JANTX
** Series available as JANTX only

HIGH VOLTAGE DOORBELL® MODULES

40Hz - 5kHz

TYPE	OUTPUT CURRENT	REVERSE VOLTAGE	MAXIMUM REVERSE CURRENT @ V_R	MAXIMUM FORWARD VOLTAGE	SURGE CURRENT	MIL-S-19500
1N5597	1A	10kV	1 μ A	19V @ 1A	30A	/404*
1N5600	2A	5kV	5 μ A	10V @ 2A	80A	
1N5603	5A	5kV	5 μ A	10V @ 5A	200A	

Doorbell® is a registered trademark of Unitorde Corporation
* Series available as JAN only

SENSISTORS®

TYPE	MIL SPEC NUMBER	DESCRIPTION
RTH22ESXXXJ	MIL-T-23648A/9	Molded, 5% tolerance, 33-10K Ω
RTH22ESXXXK	MIL-T-23648A/9	Molded, 10% tolerance, 33-10K Ω
RTH42ESXXXJ	MIL-T-23648A/19	Glass, 5% tolerance, 10-2.7K Ω
RTH42ESXXXK	MIL-T-23648A/19	Glass, 10% tolerance, 10-2.7K Ω

Sensistors® is a registered trademark of Unitorde Corporation

POWER MOSFETS

N-Channel

TYPE	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current (Amps)		I_{DM} Pulsed Drain Current	P_D MAX Power Dissipation (Watts)	MIL-S-19500
			100°C Case	250°C Case			
2N6756	100	0.18	9	14	56	75	/542A
2N6758	200	0.4	6	9	36	75	/542A
2N6760	400	1.0	3.5	5.5	22	75	/542A
2N6762	500	1.5	3.0	4.5	18	75	/542A
2N6764	100	0.055	24	38	152	150	/543A
2N6766	200	0.085	19	30	120	150	/543A
2N6768	400	0.3	9	14	56	150	/543A
2N6670	500	0.4	7.75	12	48	150	/543A

* Series available as JAN, JANTX and JANTXV.

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NPN POWER SWITCHING TRANSISTORS

TYPE	MAXIMUM COLLECTOR CURRENT	V _{CE0(max)} (V)	MINIMUM h _{FE} @ I _C (A)	MAXIMUM V _{CE(sat)} @ I _V (A)	MAXIMUM FALL-TIME (t _f)	PACKAGE	MIL-S-19500
2N5660	2A	200V	40 @ .5A	.4V @ 1A	0.4μs	TO-66	/454*
2N5661	2A	300V	25 @ .5A	.4V @ 1A	0.6μs	TO-66	/454
2N5662	2A	200V	40 @ .5A	.4V @ 1A	0.4μs	TO-5	/454
2N5663	2A	300V	25 @ .5A	.4V @ 1A	0.6μs	TO-6	/454
2N3418	3A	60V	20 @ 1A	.5V @ 2A	1.2μs	TO-5	/393*
2N3419	3A	80V	20 @ 1A	.5V @ 2A	1.2μs	TO-5	/393
2N3420	3A	60V	40 @ 1A	.5V @ 2A	1.2μs	TO-5	/393
2N3421	3A	80V	40 @ 1A	.5V @ 2A	1.2μs	TO-5	/393
2N2151	5A	80V	40 @ 1A	1.0V @ 1A	—	TO-59	/277**
2N2880	5A	80V	40 @ 1A	.25V @ 1A	0.3μs	TO-59	/315*
2N3749	5A	80V	40 @ 1A	.25V @ 1A	0.3μs	TO-111	/315
2N3996	5A	80V	40 @ 1A	.25V @ 1A	0.8μs	TO-111	/374*
2N3997	5A	80V	80 @ 1A	.25V @ 1A	1.0μs	TO-111	/374
2N3998	5A	80V	40 @ 1A	.25V @ 1A	0.8μs	TO-59	/374
2N3999	5A	80V	80 @ 1A	.25V @ 1A	1.0μs	TO-59	/374
2N5664	5A	200V	40 @ 1A	.4V @ 3A	0.8μs	TO-66	/455*
2N5665	5A	300V	25 @ 1A	.4V @ 3A	1.0μs	TO-66	/455
2N5666	5A	200V	40 @ 1A	.4V @ 3A	0.8μs	TO-5	/455
2N5667	5A	300V	25 @ 1A	.4V @ 3A	1.0μs	TO-5	/455
2N6306	8A	250V	15 @ 3A	0.8V @ 3A	0.4μs	TO-3	/498
2N6308	8A	350V	12 @ 3A	1.5V @ 3A	0.4μs	TO-3	/498
2N6544	8A	300V	7 @ 5A	1.5V @ 3A	0.9μs	TO-3	N/A
UMT1008	8A	300V	7 @ 5A	1.5V @ 3A	0.4μs	TO-3	N/A
2N6545	8A	400V	7 @ 5A	1.5V @ 5A	0.9μs	TO-3	N/A
UMT1009	8A	400V	7 @ 5A	1.5V @ 5A	0.4μs	TO-3	N/A
2N4150	10A	70V	10 @ 10A	0.6V @ 5A	0.4μs	TO-5	/394*
2N6354	10A	120V	10 @ 10A	1.0V @ 10A	0.2μs	TO-3	N/A
2N6496	15A	100V	12 @ 8A	1.0V @ 8A	0.3μs	TO-3	N/A
2N6546	15A	300V	12 @ 5A	1.5V @ 10A	0.7μs	TO-3	/525
2N6547	15A	400V	12 @ 5A	1.5V @ 10A	0.7μs	TO-3	/525
2N5038	20A	90V	20 @ 12A	1.2V @ 12A	0.5μs	TO-3	/439*
2N5039	20A	75V	20 @ 10A	1.0V @ 10A	0.5μs	TO-3	/439
2N5671	30A	90V	20 @ 15A	0.75V @ 15A	0.5μs	TO-3	N/A
2N5672	30A	120V	20 @ 15A	0.75V @ 15A	0.5μs	TO-3	N/A

* Series available as JAN, JANTX and JANTXV

** Series available as JAN and JANTX

POWER DARLINGTONS

TYPE	D.C. COLLECTOR CURRENT	V _{CE0}	MINIMUM h _{FE} @ 5A	PACKAGE	MIL-S-19500
2N6350	5A	80V	2000	TO-33	/472**
2N6351	5A	150V	1000	TO-33	/472
2N6352	5A	80V	2000	TO-66	/472
2N6353	5A	150V	1000	TO-66	/472

** Series available as JAN and JANTX

PROGRAMMABLE UNIJUNCTION TRANSISTORS

TYPE	V _{AK}	PEAK CURRENT	VALLEY CURRENT	PACKAGE	MIL-S-19500
2N6137	40V	2μA @ R _G = 1MEGΩ	1.5mA @ R _G = 200Ω	TO-18	/493*

* Available as JAN, JANTX and JANTXV

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POWER ZENERS AND TRANSIENT SUPPRESSORS

TYPE	AVERAGE D.C. POWER	BREAKDOWN VOLTAGE RANGE	PEAK POWER	PACKAGE	MIL-S-19500
1N4461-96	1.5W	6.8V-200V	140W	Axial	/406*
1N6461-68 (TVS)	2.5W	5.6V-54V	500W	Axial	/551*
1N5968-69	5.0W	5.6V-6.2V	900W	Axial	/356*
1N4954-96	5.0W	6.8V-390V	900W	Axial	/356*
1N5610-13 (TVS)	6.0W	33V-191V	1500W	Axial	/434*
UZ7706-7110	10W	6.8V-100V	2000W	Stud Mount	N/A

* Series available as JAN, JANTX and JANTXV

THYRISTORS

Silicon Control Rectifiers

TYPE	D.C. ON STATE CURRENT	V _{DRM}	MAXIMUM I _{GT}	MAXIMUM V _{GT}	PACKAGE	MIL-S-19500
2N3027	0.5A	30V	20μA	0.6V	TO-18	/419**
2N3028	0.5A	60V	20μA	0.6V	TO-18	/419
2N3029	0.5A	100V	20μA	0.6V	TO-18	/419
2N3030	0.5A	30V	20μA	0.6V	TO-18	/419
2N3031	0.5A	60V	20μA	0.6V	TO-18	/419
2N3032	0.5A	100V	20μA	0.6V	TO-18	/419
2N1870A	1.25A	30V	200μA	0.8V	TO-9	/198***
2N1871A	1.25A	60V	200μA	0.8V	TO-9	/198
2N1872A	1.25A	100V	200μA	0.8V	TO-9	/198
2N1873A	1.25A	150V	200μA	0.8V	TO-9	N/A
2N1874A	1.25A	200V	200μA	0.8V	TO-9	/198
2N2323AS†	1.6A	50V	20μA	0.6V	TO-39	/276*
2N2324AS†	1.6A	100V	20μA	0.6V	TO-39	/276
2N2325A	1.6A	150V	20μA	0.6V	TO-39	N/A
2N2326AS†	1.6A	200V	20μA	0.6V	TO-39	/276
2N2327A	1.6A	250V	20μA	0.6V	TO-39	N/A
2N2328AS†	1.6A	300V	20μA	0.6V	TO-39	/276
2N2329	1.6A	400V	20μA	0.6V	TO-39	/276

* Series available as JAN, JANTX and JANTXV

** Series available as JAN and JANTX

*** Series available as JAN only

† Available in "A" and non "A" versions

Ultra Fast Switching

TYPE	D.C. ON STATE CURRENT	V _{DRM}	RISE TIME	COMMUTATED TURN-OFF TIME	PACKAGE
GA200	0.4A	60V	25ns	2.0μs	TO-18
GA201	0.4A	100V	20ns	2.0μs	TO-18
GB200	6A	60V	25ns	2.0μs	TO-59
GB201	6A	100V	20ns	2.0μs	TO-59

Radiation Resistant

TYPE	D.C. ON STATE CURRENT	V _{DRM}	MAXIMUM I _{GT}	MAXIMUM V _{GT}	PACKAGE
GA100	0.4A	30V	20mA	1.5V	TO-18
GA101	@	60V	20mA	1.5V	TO-18
GA102	T _c = 100°C	80V	20mA	1.5V	TO-18

† Post 3×10¹⁴ NVT

1. The first part of the document discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes that this is crucial for ensuring transparency and accountability in the organization's operations.

2. The second part of the document outlines the various methods and tools used to collect and analyze data. It highlights the need for consistent data collection procedures and the use of advanced analytical techniques to derive meaningful insights from the data.

3. The third part of the document focuses on the role of technology in data management and analysis. It discusses how modern software solutions can streamline data collection, storage, and analysis processes, thereby improving efficiency and accuracy.

4. The fourth part of the document addresses the challenges associated with data management, such as data quality, security, and privacy. It provides strategies to mitigate these risks and ensure that the data remains reliable and secure throughout its lifecycle.

5. The fifth part of the document concludes by summarizing the key findings and recommendations. It stresses the importance of a data-driven approach in decision-making and the need for continuous monitoring and improvement of data management practices.

TYPE	PERFORMANCE CHARACTERISTICS																	
	Voltage Reference \pm 4%	Voltage Reference \pm 1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Uncommitted Outputs	Single-Ended Outputs	Totem Pole Output	Separate Oscillator	Adjustable Deadtime Control	Latch Off or Continuous Run Mode	Double Pulse Suppression	Low Current Start Up Package
Regulating PWMs UC1524/2524/3524 UC1524/883B	X					X	100mA	300kHz	X									16 Pin DIP
Advanced Regulating PWMs UC1524A/2524A/3524A UC1524A/883B	X		X	X	X	X	200mA	500kHz	X							X		16 Pin DIP
Advanced Regulating PWMs UC1525A/2525A/3525A UC1525A/883B	X	X	X	X		X	100mA 0.4A Pulse	500kHz			X	X	X					16 Pin DIP
Advanced Regulating PWMs UC1527A/2527A/3527A UC1527A/883B	X	X	X	X		X	100mA 0.4A Pulse	500kHz			X	X	X					16 Pin DIP
Advanced Regulating PWMs UC1526/2526/3526 UC1526/883B	X	X	X	X	X	X	100mA	400kHz			X	X	X		X			18 Pin DIP
Regulating PWMs UC493/UC494/ UC495	X						200mA	300kHz	X				X		X			16 Pin DIP 18 Pin DIP
Advanced Regulating PWMs UC493A/UC493AC UC494A/UC494AC UC495A/UC495AC UC495B/UC495BC	X			X			200mA	300kHz	X				X		X			16 Pin DIP 18 Pin DIP
Current Mode PWM Controllers UC1846/2846/3846 UC1846/883B	X	X	X	X	X	X	200mA	X 500kHz			X	X	X	X	X			16 Pin DIP
Current Mode PWM Controllers UC1847/2847/3847 UC1847/883B	X	X	X	X	X	X	200mA	X 500kHz			X	X	X	X	X			16 Pin DIP
Programmable Primary Side PWMs UC1840/2840/3840 UC1840/883B	X	X	X	X	X	X	200mA	X 500kHz		X			X	X	N/A	X		18 Pin DIP
Programmable Primary Side PWMs UC1842/2842/3842 UC1842/883B	X		X	X	X		100mA 1A Pulse	X 500kHz		X			X		N/A	X		8 Pin DIP

Power Supply Support Functions

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1543/2543/3543 UC1544/2544/3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	<ul style="list-style-type: none"> • Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC1544 series only) 	16 Pin DIL (1543 Series) 18 Pin DIL (1544 series)
UC1706/2706/3706	Dual High Current MOSFET Compatible Output Driver	<ul style="list-style-type: none"> • Dual, 1.5A, Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current 	16 Pin DIL
UC1834/2834/3834	High Efficiency Linear Regulator, Low Input-Output Differential	<ul style="list-style-type: none"> • Minimum $V_{IN}-V_{OUT}$ less than 0.5V at 5A Load with External Pass Device • Equally Usable for either Positive or Negative Regulator Design • Adjustable Low Threshold Current Sense Amplifier • Under- and Over-Voltage Fault Alert with Programmable Delay • Over-Voltage Fault Latch with 100mA Crowbar Drive Output 	16 Pin DIL
UC1901/2901/3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	<ul style="list-style-type: none"> • An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock 	14 Pin DIL
UC1903/2903/3903	Quad Supply and Line Monitor Precision System	<ul style="list-style-type: none"> • Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal Inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP 	18 Pin DIL

Functional Circuit

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1704/3704	Bridge Transducer Switch	<ul style="list-style-type: none"> • Dual Matched Current Sources • High-Gain Differential Sensing Circuit • Wide Common-Mode Input Capability • Complimentary Digital Open-Collector Outputs • Externally Programmable Time Delay • Optional Output Latch with Reset • Built-in Diagnostic Activation • Wide Supply Voltage Range • High Current Heater Power Source Driver 	16 Pin DIL

Voltage Regulators

3

Three Terminal Voltage Regulators, Adjustable

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)	PACKAGE
UC117K/LM117K UC217K/LM217K *UC317K/LM317K	1.5A	Pos.	Adjustable from 1.2V to 37V	TO-3 TO-3 TO-3
UC137K/LM137K UC237K/LM237K *UC337K/LM337K	1.5A	Neg.	Adjustable from -1.2V to -37V	TO-3 TO-3 TO-3
UC150K/LM150K UC250K/LM250K *UC350K/LM350K	3.0A	Pos.	Adjustable from 1.2V to 33V	TO-3 TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Positive

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7800AK/LM140AK SERIES *UC7800ACK/LM340AK SERIES	1.5A	Pos.	5V ± 1%	12V ± 1%	15V ± 1%	TO-3 TO-3
UC7800K/LM140K SERIES *UC7800CK/LM340K SERIES	1.5A	Pos.	5V ± 4%	12V ± 4%	15V ± 4%	TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Negative

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7900AK/LM120K SERIES *UC7900ACK SERIES	1.5A	Neg.	-5V ± 1%	-12V ± 1%	-15V ± 1%	TO-3 TO-3
UC7900K SERIES *UC7900CK/LM320K SERIES	1.5A	Neg.	-5V ± 4%	-12V ± 4%	-15V ± 4%	TO-3 TO-3

* Also available in TO-220 package.

Motor Control Circuits

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
L292	2A, 36V, 30KHz, H-Bridge Motor Driver	<ul style="list-style-type: none"> • External Loop Adjustment • Single Power Supply (18-36V) • Input Signal Symmetric to Ground • Thermal Protection 	15 Pin Power SIP
L293/293E	Four Channel Push-Pull Drivers for Inductive Loads	<ul style="list-style-type: none"> • 1A Output per Channel (2A peak non-repetitive) • Supply Voltage to 36V • Inhibiting Facility • Thermal Protection • High Noise Immunity • E-Version Provides for External Emitter Sense Resistors • Compatible with Standard TTL Logic Inputs 	L293 16 Pin "Batwing" Dip L293E 20 Pin "Batwing" Dip
L295	Dual PWM Solenoid Driver and Stepper Motor Driver	<ul style="list-style-type: none"> • 3A Peak Current Per Driver • Supply Voltage to 40V • Current Limiting • Thermal Protection • Compatible with Standard TTL Logic Inputs 	15 Pin Power SIP
UC1637/2637/3637	Switched Mode Controller for DC Motor Drive	<ul style="list-style-type: none"> • Single or Dual Supply Operation • ± 2.5 to $\pm 20V$ Input Supply Range • $\pm 5\%$ Initial Oscillator Accuracy; $\pm 10\%$ Over Temperature • Pulse-by-Pulse Current Limiting • Under-Voltage Lockout • Uncommitted PWM Comparators for Design Flexibility 	18 Pin Dip
UC1717/UC3717	Stepper Motor Drive Circuit	<ul style="list-style-type: none"> • Half-Step and Full-Step Mode • Bipolar Constant Current Chopper Drive • Built-In Protection Diodes (Schottky) • Wipe Range of Current Control 5-1000mA • Wide Voltage Range 10-45V • Designed for Unregulated Motor Supply Voltage • Thermal Overload Protection 	16 Pin Dip

Note: U2TA506, 8 & 10 and U2TA606, 8 & 10 TO-92 Darlington's are appropriate for driving DC brushless motors and other inductive loads.

LINEAR INTEGRATED CIRCUITS

L292

Switchmode Driver for DC Motors

FEATURES

- Driving capability: 2A, 36V, 30KHz
- Two logic chip enable inputs
- External loop gain adjustment
- Single power supply (18 to 36V)
- Input signal symmetric to ground
- Thermal protection

DESCRIPTION

The L292 is a monolithic LSI circuit in a 15-lead Multiwatt® package. It is intended to drive DC motors controlling positioning devices such as used in typewriters, printers, plotters and other computer peripherals.

The device contains a level shifter, triangle waveform oscillator, error amplifier, PWM comparator, current sensing amplifier, H-bridge output stage with a 2A, 36V driving capability and two output enable inputs. Protection circuitry includes under-voltage output inhibit and thermal protection.

3

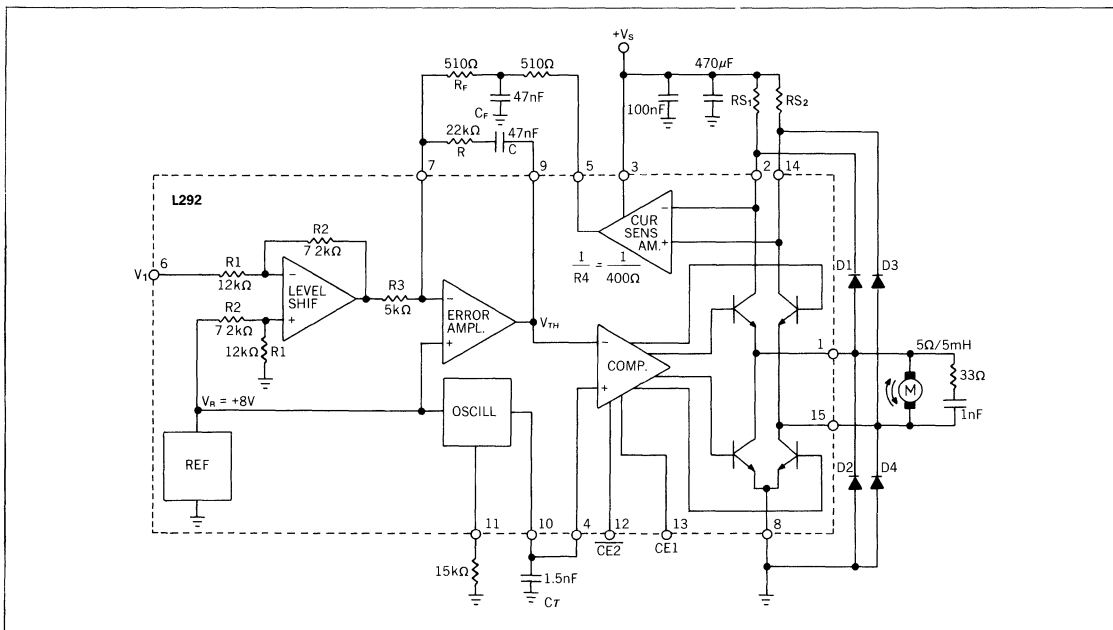
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s	36V
Input Voltage, V_1	-15 to $+V_s$ V
Inhibit Voltage, $V_{inhibit}$	0 to V_s V
Output Current, I_o	2.5A
Total Power Dissipation ($T_{case} = 75^\circ\text{C}$).....	25W
Storage and Junction Temperature, T_{stg}	-40 to $+150^\circ\text{C}$
Thermal Resistance Junction-Case, θ_{JC}	3°C/W

THERMAL DATA

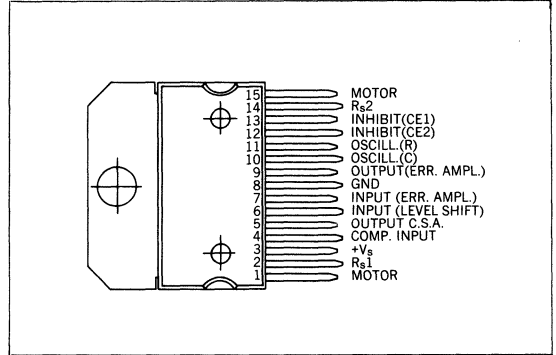
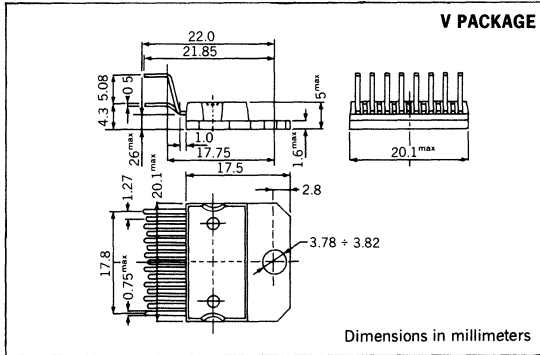
Thermal Resistance Junction-Case, θ_{JC} 3°C/W max

BLOCK DIAGRAM



MECHANICAL DATA

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $f_{osc} = 20\text{KHz}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Voltage	V_s		18		36	V	
Quiescent Drain Current	I_d	$V_s = 20\text{V}$ (offset null)		30	50	mA	
Input Offset Voltage (Pin 6)	V_{os}	$V_s = 36\text{V}$, $I_o = 0$			± 350	mV	
Inhibit Input Voltage (Pin 12, 13)	$V_{inh. L}$				2	V	
	$V_{inh. H}$		3.2			V	
Inhibit Input Current	$I_{inh. L}$	$V_{inh. (L)} = 0.4\text{V}$			-100	μA	
	$I_{inh. H}$	$V_{inh. (H)} = 3.2\text{V}$			10	μA	
Input Current (Pin 6)	I_i		$V_i = -8.8\text{V}$			-1.8	mA
			$V_i = +8.8\text{V}$			0.5	mA
Input Voltage (Pin 6)	V_i	$R_{S1} = R_{S2} = 0.2\Omega$	$I_o = 2\text{A}$		9.1	V	
			$I_o = -2\text{A}$		-9.1	V	
Output Current	I_o	$V_i \pm 9.8\text{V}$, $R_{S1} = R_{S2} = 0.2\Omega$	± 2			A	
Total Drop Out Voltage	V_D	(including sensing resistors)	$I_o = 2\text{A}$			5	V
			$I_o = 1\text{A}$			3.5	V
Sensing Resistor Voltage Drop	V_{RS}	$T_j = 150^\circ\text{C}$, $I_o = 2\text{A}$			0.44	V	
Transconductance	$\frac{I_o}{V_i}$	$R_{S1} = R_{S2} = 0.2\Omega$	220	240	260	mA/V	
		$R_{S1} = R_{S2} = 0.4\Omega$		120		mA/V	
Frequency Range (Pin 10)	f_{osc}		1		30	KHz	

TRUTH TABLE

$V_{inhibit}$		Output Stage Condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal Operation
H	L	Disabled
H	H	Disabled

FUNCTIONAL DESCRIPTION

The error signal input has been designed to accept a bidirectional error signal symmetrical to ground. The level shifter converts the \pm error signal into a single positive signal with the aid of an internally generated 8V reference. This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_T , C_T - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \quad (\text{with } R \geq 8.2K\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{S1} , R_{S2} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in this RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5 Ω , 5mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ , is programmed by C_T in conjunction with an internal resistor R_T .

This can be found from:

$$\tau = R_T \cdot C_{PIN\ 10} \quad (C_T \text{ in the diagram})$$

Since R_T is approximately 1.5 K Ω and the recommended τ to avoid simultaneous conduction is 2.5 μ S, $C_{PIN\ 10}$ should be around 1.5nF.

The current sense resistors R_{S1} and R_{S1} should be high precision types (maximum tolerance $\pm 2\%$) and the recommended value is given by:

$$R_{max} \cdot I_{o\ max} \leq 0.44V$$

It is possible to synchronize two L292s, if desired, using the network shown in Figure 1.

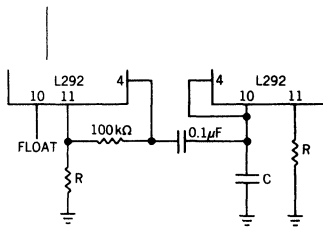


Figure 1.

Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively). Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generate spikes as high as 1.5V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see Figure 2).

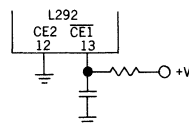


Figure 2.

APPLICATION INFORMATION

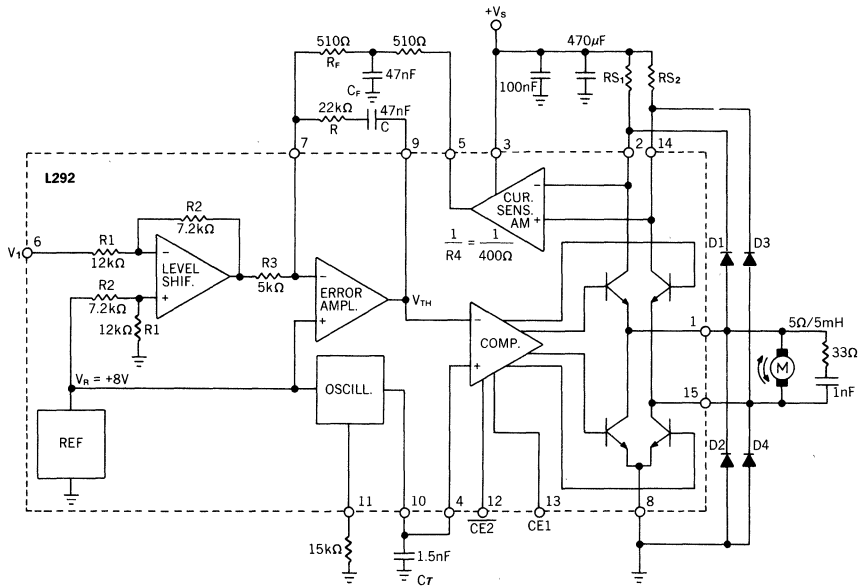
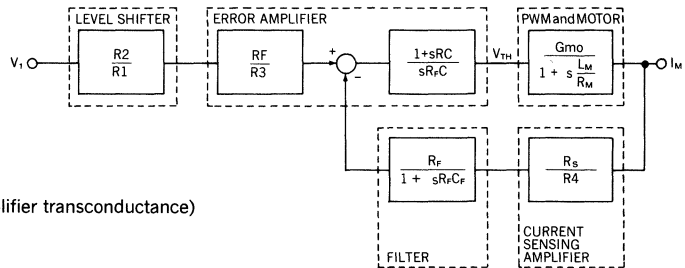


Figure 3.

The schematic diagram used for the Laplace analysis of the system is shown in Figure 4.



$R_{S1} = R_{S2} = R_s$ (sensing resistors)

$$\frac{1}{R_4} = 2.5 \cdot 10^{-3} \Omega \text{ (current sensing amplifier transconductance)}$$

L_M = Motor inductance

R_M = Motor resistance

I_M = Motor current

$$G_{mo} = \left. \frac{I_M}{V_{TH}} \right|_{s=0} \text{ (DC transfer function from the input of the comparator } (V_{TH}) \text{ to the motor current } (I_M)).$$

Figure 4.

APPLICATION INFORMATION (continued)

Neglecting the $V_{CE\ sat}$ of the bridge transistor and the V_{BE} of the diodes:

$$G_{mo} = \frac{1}{R_M} \frac{2V_S}{V_R} \quad \text{where: } V_S = \text{supply voltage} \quad (1)$$

$V_R = 8V$ (reference voltage)

DC Transfer Function

In order to be sure that the current loop is stable the following condition is imposed:

$$1 + sRC = 1 s \frac{L_M}{R_M} \quad (\text{pole cancellation}) \quad (2)$$

$$\text{from which } RC = \frac{L_M}{R_M} \quad (\text{Note that in practice } R \text{ must be greater than } 5.6K\Omega)$$

The transfer function is then, (3)

$$\frac{I_M}{V_i}(s) = \frac{R_2 R_4}{R_1 R_3} G_{mo} \frac{1 + sR_F C_F}{G_{mo} R_s + s R_4 C + s^2 R_F C_F R_4 C}$$

In DC condition, this is reduced to

$$\frac{I_M}{V_i}(0) = \frac{R_2 R_4}{R_1 R_3} \cdot \frac{1}{R_s} = \frac{0.048}{R_s} \left[\frac{A}{V} \right]$$

Open-Loop Gain and Stability Criterion

For $RC = L_M/R_M$, the open loop gain is: (5)

$$A\beta = \frac{1}{sR_F C} \cdot G_{mo} \frac{R_s}{R_4} \frac{R_F}{1 + sR_F C_F} = \frac{G_{mo} R_s}{R_4 C} \frac{1}{s(1 + sR_F C_F)}$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_F C_F}$, $|A\beta|$ must be < 1
(see Figure 5), that is:

$$|A\beta|_f = \frac{1}{2\pi R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \frac{R_F C_F}{\sqrt{2}} < 1 \quad (6)$$

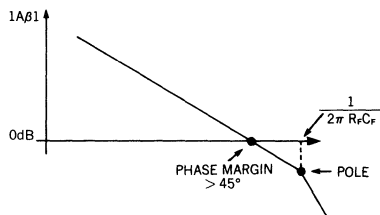


Figure 5. Open-Loop Frequency Response

Closed-Loop System Step Response**a) Small-signals analysis**

The transfer function (3) can be written as follows:

$$\frac{I_M}{V_i}(s) = \frac{0.048}{R_s} \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \quad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo} R_s}{R_4 C R_F C_F}}$ is the cutoff frequency

where: $\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_s}}$ is the damping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

1) $\xi = 1$ from which

$$I_M(t) = \frac{0.048}{R_s} [1 - e^{-\frac{t}{2R_F C_F}} (1 + \frac{t}{4 R_F C_F})] \cdot V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.048}{R_s} (1 - \cos \frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}}) V_i$$

From Figure 7 it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier is locked to the reference voltage V_R , present at the non-inverting input of the same amplifier).

The previous linear analysis is correct for this example.

Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \quad (\text{phase margin} = 45^\circ)$$

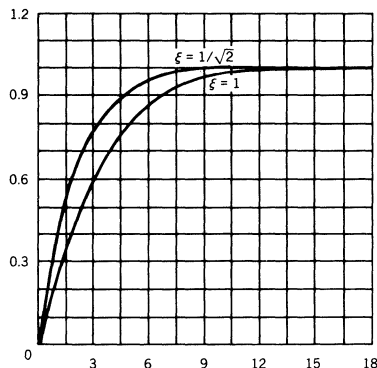


Figure 6. Small Signal Step Response
(Normalized Amplitude vs $t/R_F C_F$)

APPLICATION INFORMATION (continued)

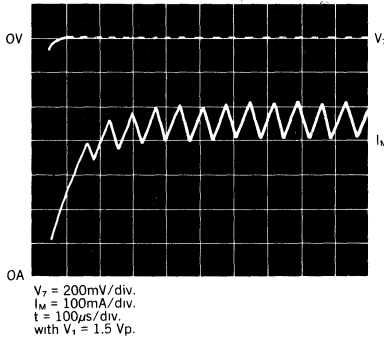


Figure 7. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Small Signal Response

b) Large signal response

The large step signal response is limited by slew-rate and inductive load. In this case, during the rise-time of the motor current, the L292 works in open-loop condition, as can be seen from Figure 8.

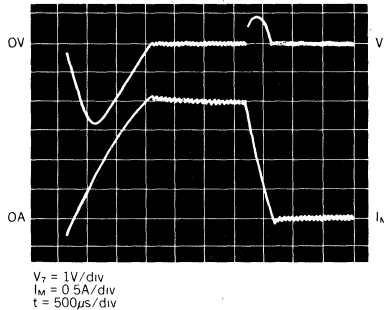


Figure 8. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Large Signal Response

The voltage at pin 7 (inverting input of the error amplifier) departs from the reference voltage V_R present at the non-inverting input and the feedback loop is open.

The feedback loop is on when the motor current reaches its steady-state value (2A).

Closed Loop System Bandwidth

A good choice for ξ is the value $1/\sqrt{2}$. In this case:

$$\frac{I_M}{V_i} (s) = \frac{0.048}{R_s} \frac{1 + s R_F C_F}{1 + 2s R_F C_F + 2s^2 R_F^2 C_F^2} \quad (8)$$

The module of the transfer function is: (9)

$$\left| \frac{I_M}{V_i} \right| = \frac{0.048}{R_s} \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}}$$

The cutoff frequency is derived from expression (9) by putting

$$\left| \frac{I_M}{V_i} \right| = 0.707 \cdot \frac{0.048}{R_s} (-3\text{dB});$$

from which:

$$\omega_T = \frac{0.9}{R_F C_F} \quad f_T = \frac{0.9}{2\pi R_F C_F} \quad (10)$$

Note that R_F must be less than $1.5\text{K}\Omega$ in order to have the maximum current swing at the output of current sensing amplifier.

Working Frequency and Motor Current Ripple

For a value of rotation speed ω the e.m.f. E is equal to $K_E \omega$, where K_E is the motor speed constant.

Neglecting the motor resistance R_M , the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes, we have:

$$\Delta t_1 = \frac{\Delta I_M}{V_s - E} L_M \quad (\text{transistors conduction period}) \quad (11)$$

$$\Delta t_2 = \frac{\Delta I_M}{V_s + E} L_M \quad (\text{diodes conduction period})$$

Where ΔI_M is the current ripple in the motor (see Figure 9).

The working frequency is:

$$f = \frac{1}{2 R_T C_T} = \Delta t_1 = \Delta t_2 \quad (12)$$

where R_T is the resistance at pin 11 and C_T the capacitor at pin 10. R_T must be $\geq 8.2\text{K}\Omega$ due to the output current capability at pin 11. If we consider $E = 0$ ($\omega = 0$; motor stopped) we have:

$$\Delta t_1 = \Delta t_2 = \frac{\Delta I_M}{V_s} L_M \quad (13)$$

from this formula we can write

$$\Delta I_M = \frac{V_s}{L_M} \frac{T}{2} \quad \left(\frac{T}{2} = \Delta t_1 = \Delta t_2 = \text{half period} \right) \quad (13 \text{ bis})$$

The motor current ripple ΔI_M must be limited in order to reduce dissipation in the motor and the peak output current of the L292.

ΔI_{Mmax} should be less than 10% of I_{Mmax} (see Figure 9).

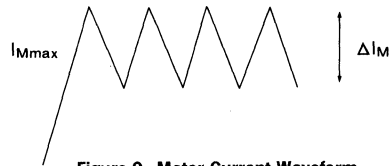


Figure 9. Motor Current Waveform

From the equation (13 bis) and considering $\Delta I_M = 0.1 I_{Mmax}$ we have:

$$0.1 I_{Mmax} = \frac{V_s}{2f L_{Mmin}} \quad (14)$$

from which:

$$L_{Mmin} = \frac{5 V_s}{f I_{Mmax}} \quad (15)$$

The switching characteristics of the L292 demand that the working frequency f is less than 30KHz.

If for $f = 30\text{KHz}$, L_M is less than $L_{M\text{min}}$, an external inductor should be put in series with the motor.

From relationship (15) we have:

$$L_{\text{series}} = \frac{5 V_s}{f I_{M\text{max}}} - L_M \quad (16)$$

Deadtime

A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which, if it were allowed to occur would damage them. To overcome this the comparator that drives the final stage in effect consists of two separate comparators (Figure 10): both receive the same V_t signal but on opposite inputs. The other two inputs are driven by V_{TH} shifted by plus or minus $R_T I'$. This voltage shift when compared with V_t results in a delay in switching from one comparator to the other. In this way there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor R_T (1.5K) and an external capacitor C_T connected to pin 10 which also fixes oscillator frequency.

It is: $\tau = R_T C_T$

In a typical application, a capacitor of 1.5nF is used to give a switching delay of 2.25 μs , a more than adequate time when you consider that the switch-off delay of the integrated transistors is only 0.5 μs .

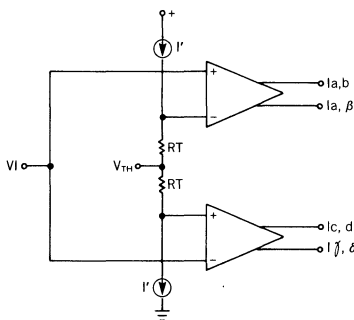


Figure 10. L292 Deadtime Control

Efficiency and Power Dissipation

The expression for the bridge efficiency, independently of the losses due to the switching times and neglecting the dissipation due to the motor current ripple, is:

$$\eta = 1 - \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{\text{sat}}}{V_s} - \frac{\Delta t_2}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{\text{over}}}{V_s} \quad (17)$$

where

$$\begin{aligned} V_{\text{over}} &\cong 2V (2V_{BE} + R_s I_M) \\ V_{\text{sat}} &\cong 4V (2V_{CE\text{ sat}} + 3V_{BE}) \\ \Delta t_1 &= \text{transistors conduction period.} \\ \Delta t_2 &= \text{diodes conduction period.} \end{aligned}$$

If $\Delta t_1 \gg \Delta t_2$ and $V_s = 20\text{V}$, we obtain:

$$\eta = 1 - \frac{4}{20} = 80\% \quad (18)$$

In practice, the efficiency will be slightly lower due to the signal circuit dissipation (1W @ 20V) and the finite switching times (about 1W). If we transfer to the motor a power of 40W the bridge power dissipation from (18) is 10W and the total dissipation is 12W. This is an actual efficiency of 77%. Considering a maximum dissipation equal to 20W for the L292 (Multiwatt package), it is possible to handle continuous powers greater than 60W.

EXAMPLE

- a) Data
- Motor characteristics: $L_M = 5\text{mH}$
 $R_M = 5\Omega$
 $L_M/R_M = 1\text{msec}$
 - Voltage and current characteristics:
 $V_s = 20\text{V}$ $I_M = 2\text{A}$ $V_i = 8.3\text{V}$
 - Closed loop bandwidth: 3kHz.
- b) Calculation
- From relationship (4):

$$R_s = \frac{0.048}{I_M} V_i = 0.2\Omega$$

and from (1):

$$G_{m0} = \frac{2V_s}{R_M V_R} 1\Omega^{-1}$$

— $RC = 1\text{msec}$ [from expression (2)].

— Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{400 C}{4 R_F C_F \cdot 0.2}$$

The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 3\text{kHz}$$

- c) Summarizing
- $RC = 1 \cdot 10^{-3} \text{ sec}$
 - $\frac{1000 C}{R_F C_F} = 1$
 - $R_F C_F \cong 47\mu\text{s}$
- } $C = 47\text{nF}$
} $R = 22\text{K}\Omega$
} For $R_F = 510\Omega \rightarrow$
} $C_F = 92\text{nF}$

LINEAR INTEGRATED CIRCUITS

Push-Pull Four Channel Driver

L293
L293E

FEATURES

- Output current 1A per channel
- Peak output current 2A per channel (non repetitive)
- Inhibit facility
- High noise immunity
- Separate logic supply
- Over-temperature protection

DESCRIPTION

The L293 and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293E has external connections to the lower emitter of each driver, permitting the connection of sensing resistors, for switchmode control.

The L293 and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit boards.

ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_c 36V
 Logic Supply Voltage, V_{ss} 36V
 Input Voltage, V_i 7V
 Inhibit Voltage, V_{inh} 7V
 Peak Output Current (Non-Repetitive), I_{out} 2A
 Total Power Dissipation at $T_{ground-pins} = 80^\circ\text{C}$, P_{tot} 5W
 Storage and Junction Temperature, T_{stg} , T_j -40 to +150°C

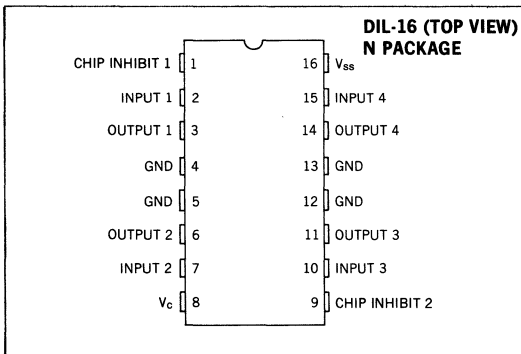
THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} 14°C/W max
 Thermal Resistance Junction-Ambient, θ_{JA} 80°C/W max

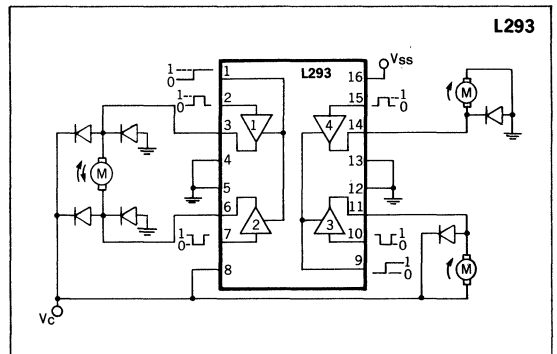
ORDERING NUMBERS

L293B (16 leads)
 L293E (20 leads)

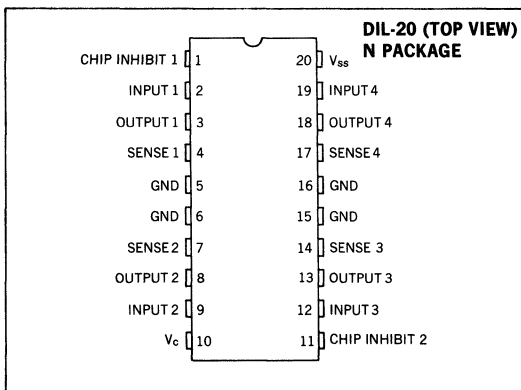
CONNECTION DIAGRAM



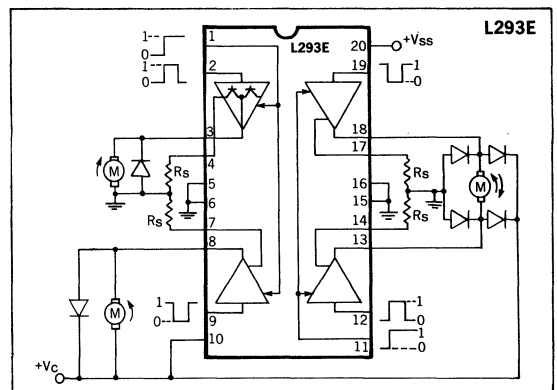
BLOCK DIAGRAM



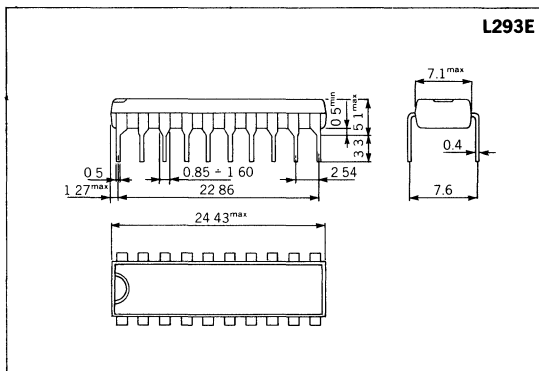
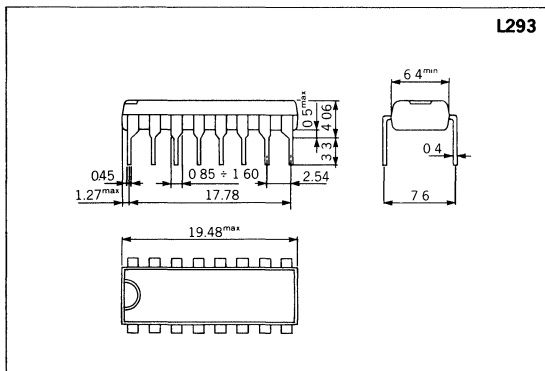
CONNECTION DIAGRAM



BLOCK DIAGRAM



MECHANICAL DATA



ELECTRICAL CHARACTERISTICS (For each channel, $V_o = 24V$, $V_{ss} = 5V$, $T_{amb} = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_c				36	V
Logic Supply Voltage	V_{ss}		4.5		36	V
Collector Supply Current	I_c	$V_i = L, I_o = 0, V_{inh.} = H$		2	6	mA
		$V_i = H, I_o = 0, V_{inh.} = H$		16	24	
		$V_{inh.} = L$			4	
Total Quiescent Logic Supply Current	I_{ss}	$V_i = L, I_o = 0, V_{inh.} = H$		44	60	mA
		$V_i = H, I_o = 0, V_{inh.} = H$		16	22	
		$V_{inh.} = L$		16	24	
Input Low Voltage	V_{iL}		-0.3		1.5	V
Input High Voltage	V_{iH}	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Input Current	I_{iL}	$V_i = L$			-10	μA
High Voltage Input Current	I_{iH}	$V_i = H$		30	100	μA
Inhibit Low Voltage	$V_{inh.L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{inh.H}$	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Inhibit Current	$I_{inh.L}$			-30	-100	μA
High Voltage Inhibit Current	$I_{inh.H}$				10	μA
Source Output Saturation Voltage	V_{CEsatH}	$I_o = -1A$		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	$I_o = 1A$		1.2	1.8	V
Sensing Voltage (Pins 4, 7, 14, 17)**	V_{SENS}				2	V
Rise Time	t_r	0.1 to 0.9 V_o *		250		ns
Fall Time	t_f	0.9 to 0.1 V_o *		250		ns
Turn-On Delay	t_{ON}	0.5 V_i to 0.5 V_o *		450		ns
Turn-Off Delay	t_{OFF}	0.5 V_i to 0.5 V_o *		200		ns

*See Figure 1.

**Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.}^{**}$
H	H	H
L	L	H
H	X*	L
L	X*	L

*High output impedance.
**Relative to the considered channel.

Figure 1. Switching Times

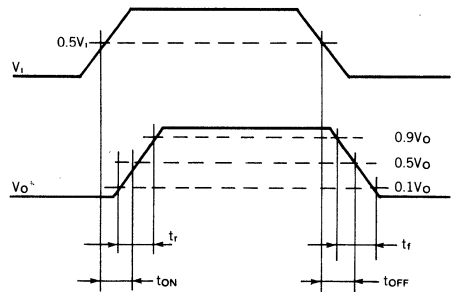


Figure 2. Saturation Voltage vs Output Current

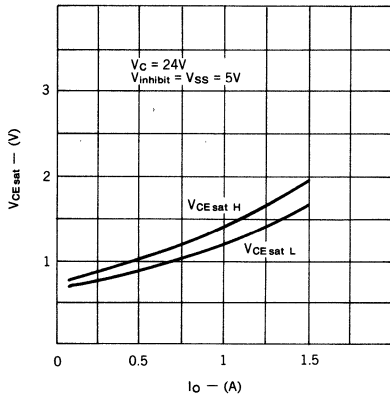


Figure 3. Source Saturation vs Ambient Temperature

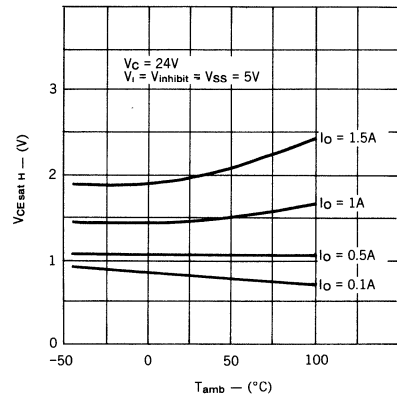


Figure 4. Sink Saturation Voltage vs Ambient Temperature

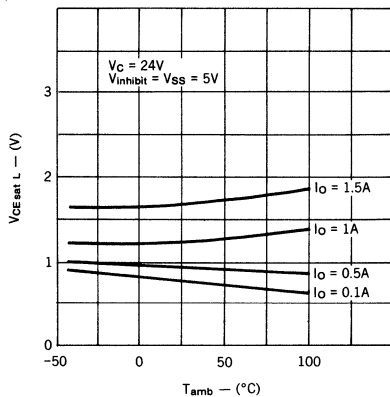


Figure 5. Quiescent Logic Supply Current vs Logic Supply Voltage

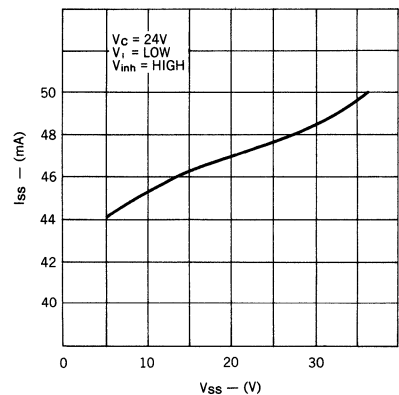


Figure 6. Output Voltage vs Input Voltage

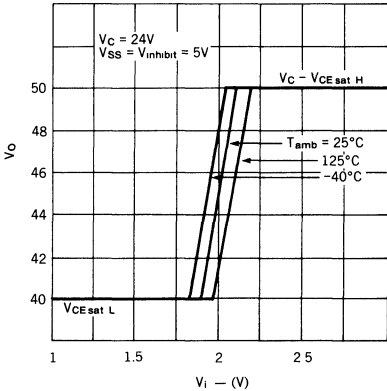


Figure 7. Output Voltage vs Inhibit Voltage

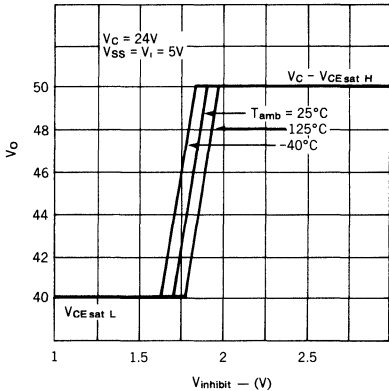


Figure 8. DC Motor Controls (with Connection to Ground and to the Supply Voltage)

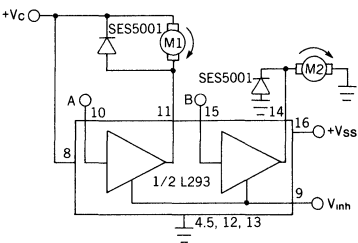
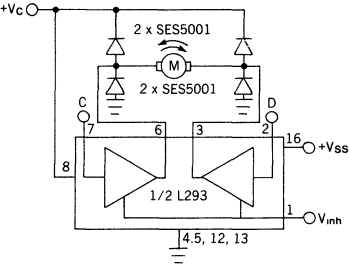


Figure 9. Bidirectional DC Motor Control



V _{inh.}	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't care

INPUTS		FUNCTION
V _{inh.} = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
V _{inh.} = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 10. Bipolar Stepping Motor Control

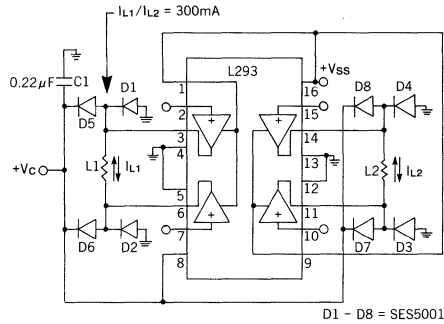
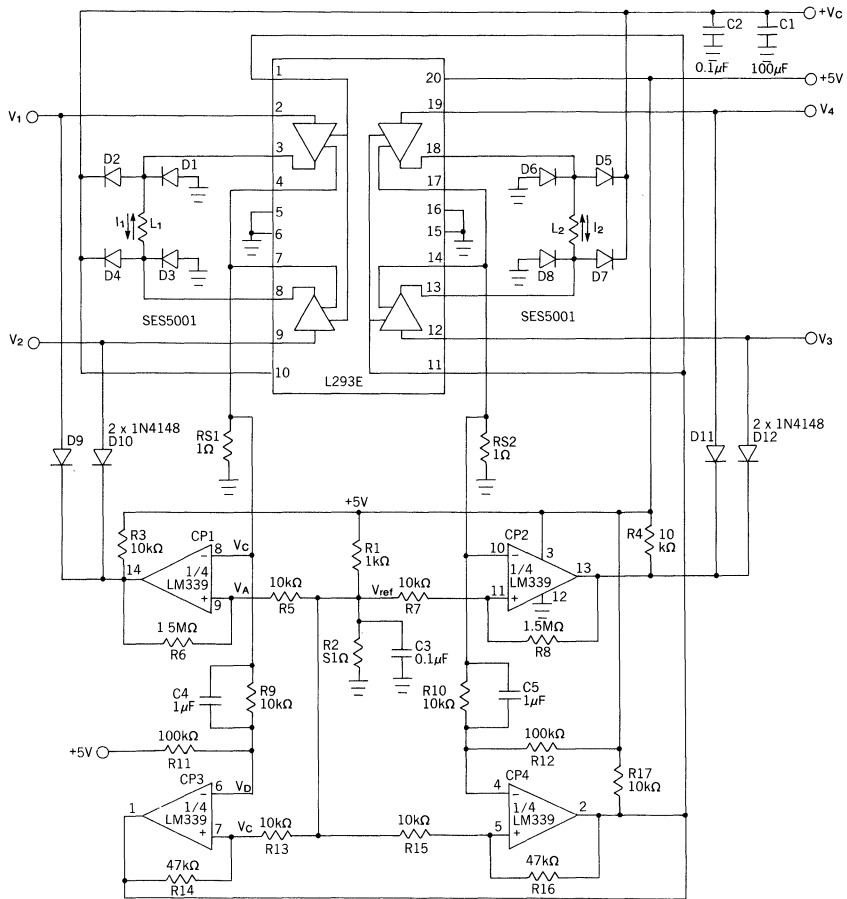


Figure 11. Stepping Motor Driver with Phase Current Control and Short Circuit Protection



D1 - D8 : 0.5A fast diodes (SES5001 or equivalent).

MOUNTING INSTRUCTIONS

The $R_{thj-amp}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power P_{tot} and the θ_{JA} as a function of the side " ℓ " of two equal square

copper areas having a thickness of 35μ (see Figure 12). In addition, it is possible to use an external heatsink (see Figure 14).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12. Example of P.C. Board Copper Area which is used as Heatsink

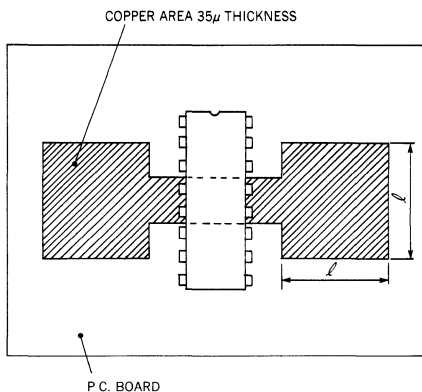


Figure 13. Maximum Package Power and Junction to Ambient Thermal Resistance vs Size " ℓ "

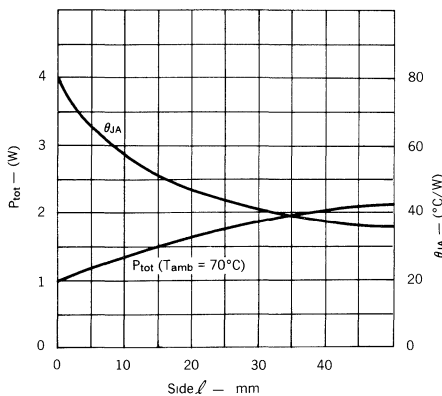


Figure 14. External Heatsink Mounting Example ($\theta_{JA} = 25^{\circ}\text{C/W}$)

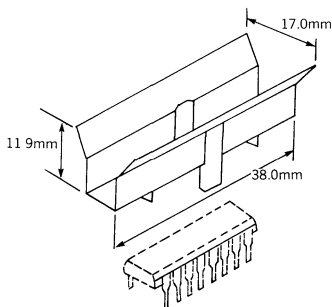
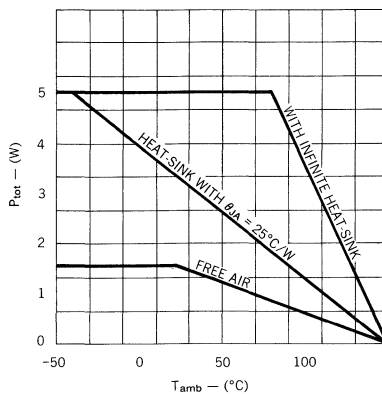
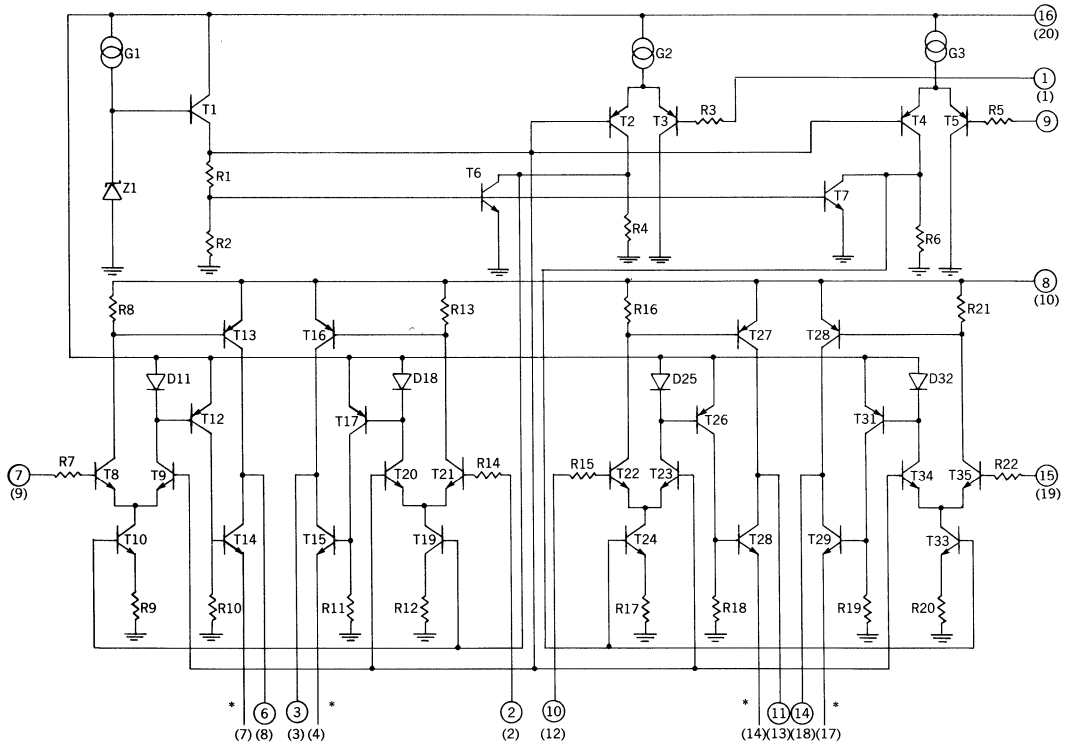


Figure 15. Maximum Allowable Power Dissipation vs Ambient Temperature



SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 () Pins of L293E

LINEAR INTEGRATED CIRCUITS

Dual Switchmode Solenoid Driver

L295

3

FEATURES

- High current capability (up to 2.5A per channel)
- High voltage operation (up to 46V for power stage)
- High efficiency switchmode operation
- Regulated output current (adjustable)
- Few external components
- Separate logic supply
- Thermal protection

DESCRIPTION

The L295 is a monolithic integrated circuit in a 15-lead Multiwatt® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels and drive 2 independent solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and separate power supply inputs for bilevel operation such as interfacing with peripherals running at higher voltage levels.

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.

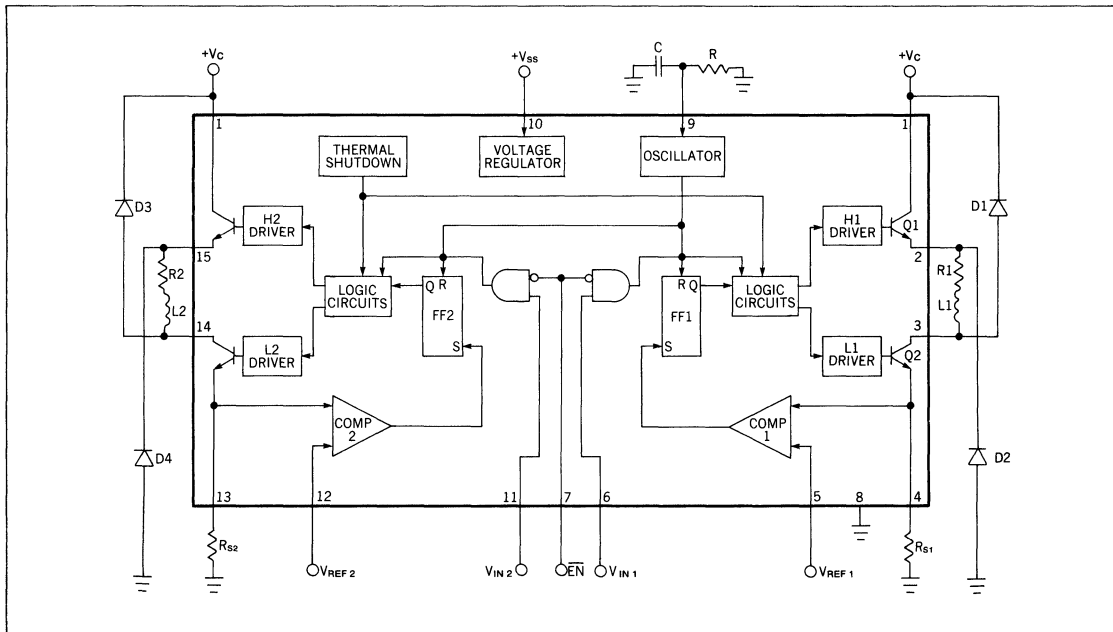
ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_C	50V
Logic Supply Voltage, V_{SS}	12V
Enable and Input Voltage, V_{EN} , V_I	7V
Reference Voltage, V_{REF}	7V
Peak Output Current (each channel)	
Non-Repetitive, (t = 100µsec), I_o	3A
Repetitive (80% on -20% off; $t_{ON} = 10ms$)	2.5A
DC Operation	2A
Total Power Dissipation (at $T_{Case} = 75^\circ C$)	25W
Storage and Junction Temperature	-40 to +150°C

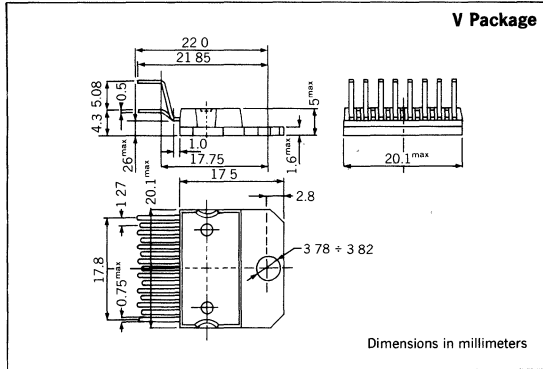
THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC}	3°C/W max
Thermal Resistance Junction-Ambient, θ_{JA}	35°C/W max

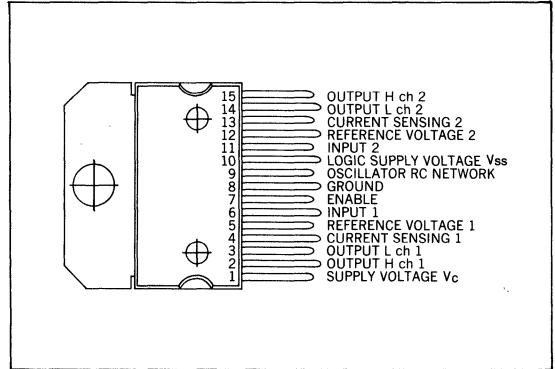
BLOCK DIAGRAM



MECHANICAL DATA



CONNECTION DIAGRAM (TOP VIEW)

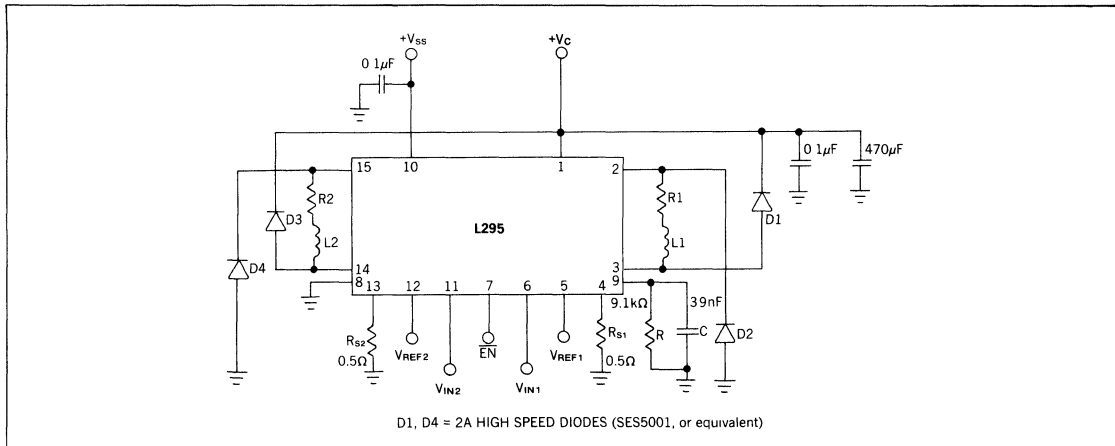


ELECTRICAL CHARACTERISTICS (Refer to the application circuit, $V_{SS} = 5V$, $V_C = 36V$, $T_J = 25^\circ C$; unless otherwise specified, L = Low; H = High)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_C		12		46	V
Logic Supply Voltage	V_{SS}		4.75		10	V
Quiescent Drain Current (from V_C)	I_C	$V_C = 46V$; $V_{I1} = V_{I2} = V_{EN} = L$			4	mA
Quiescent Drain Current (from V_{SS})	I_{SS}	$V_{SS} = 10V$			46	mA
Low Input Voltage	V_{I1L}, V_{I2L}		-0.3		0.8	V
High Input Voltage	V_{I1H}, V_{I2H}		2.2		7	V
Low Enable Input Voltage	V_{ENL}		-0.3		0.8	V
High Enable Input Voltage	V_{ENH}		2.2		7	V
Input Current	I_{I1}, I_{I2}	$V_{I1} = V_{I2} = L$			-100	μA
		$V_{I1} = V_{I2} = H$			10	
Enable Input Current	I_{EN}	$V_{EN} = L$			-100	μA
		$V_{EN} = H$			10	
Input Reference Voltage	V_{REF1}, V_{REF2}		0.2		2	V
Input Reference Current	I_{REF1}, I_{REF2}				-5	μA
Oscillation Frequency	f_{osc}	$C = 3.9nF, R = 9.1k\Omega$		25		KHz
Transconductance (each channel)	$\frac{I_p}{V_{REF}}$	$V_{REF} = 1V, R_s = 0.5\Omega$	1.9	2	2.1	A/V
Total Output Voltage Saturation (each channel)*	V_{sat}	$I_o = 2A$		2.8	3.6	V
External Sensing Resistors Voltage Drop	V_{sens1}, V_{sens2}				2	V

* $V_{sat} = V_{CEsatQ1} + V_{CEsatQ2}$.

APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are;

\overline{EN} chip enable (digital input, active low), enables both channels when in the low state.

V_{IN1} ,
 V_{IN2} channel inputs (digital inputs, active high), enable each channel independently. A channel is activated when both \overline{EN} and the appropriate channel input are active.

V_{REF1} ,
 V_{REF2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{REF} .

Since the two channels are identical, only channel one will be described. The following description applies equally to channel two, replacing FF2 for FF1, V_{REF2} for V_{REF1} etc. When the channel is activated by a low level on the \overline{EN} input and a high level on the channel input V_{IN1} , the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law:

$$I = \frac{V}{R1} \left(1 - e^{-\frac{R1t}{L1}} \right)$$

where: R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load

The current increases until the voltage on the external sensing resistor, R_{S1} , reaches the reference voltage, V_{REF1} . This peak current, I_{p1} , is given by:

$$I_{p1} = \frac{V_{REF1}}{R_{S1}}$$

At this point the comparator output, Comp 1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1} , decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{p1} \right) e^{-\frac{R1t}{L1}} - \frac{V_A}{R1}$$

where: $V_A = V_{CEsat} Q2 + V_{sense} 1 + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in Figure 1.

At time t_2 , channel 1 is disabled by taking the inputs V_{IN1} low and/or \overline{EN} high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{t2} \right) e^{-\frac{R1t}{L1}} - \frac{V_B}{R1}$$

where: $V_B = V_C + V_{D1} + V_{D2}$
 I_{t2} = current value at the time t_2 .

Figure 2 shows the current waveform obtained with an RC network connected between pin 9 and ground. From t_0 to t_1 the current increases as in Figure 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{S1} is equal to V_{REF1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in Figure 4 and must be chosen in the range 10 to 30KHz.

It is possible with external hardware to change the reference voltage V_{REF} in order to obtain a high peak current I_p and a lower holding current I_h (see Figure 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{REF1} , V_{REF2}) can be left open or connected to V_{SS} ; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_s :

$$I_p = \frac{2.5}{R_s}$$

SIGNAL WAVEFORMS

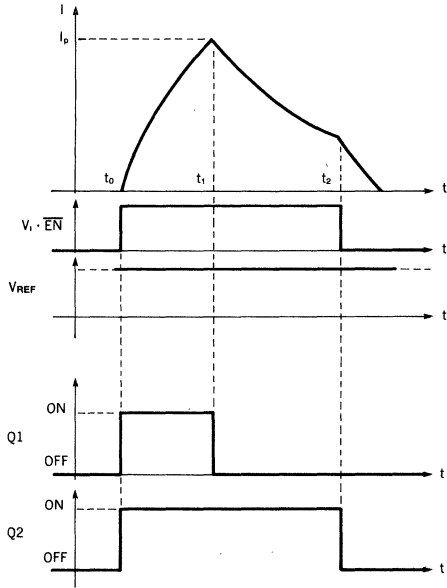


Figure 1. Load current waveform with pin 9 connected to GND

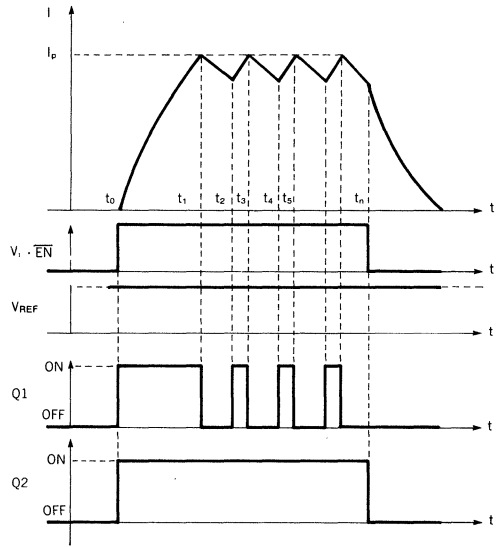


Figure 2. Load current waveform with external R-C network connected between pin 9 and ground

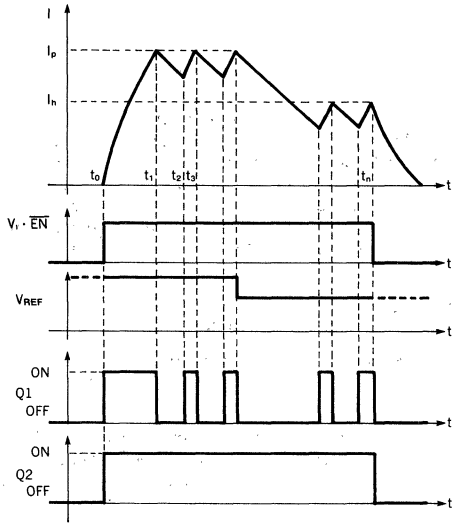


Figure 3. With V_{REF} changed by hardware

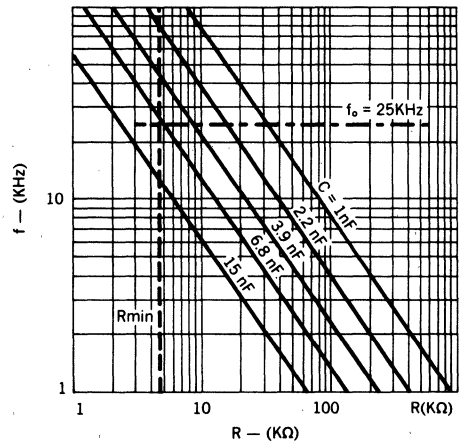


Figure 4. Switching frequency vs values of R and C

LINEAR INTEGRATED CIRCUITS

1.5A, Three Terminal Adjustable Positive Voltage Regulators

UC117
UC217
UC317

3

FEATURES

- Output voltage adjustable from 1.2 to 37V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Temperature-independent current limit
- Standard 3-lead transistor packages (TO-3, TO-220)

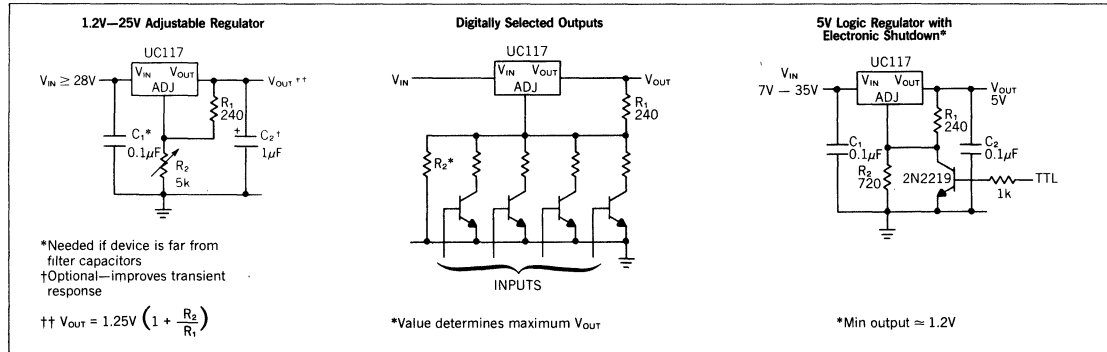
DESCRIPTION

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range. Although ease of setting the output voltage to any desired value with only two external resistors is a major feature of this circuit, exceptional line and load regulation are also offered. In addition, full overload protection consisting of current limiting, thermal shutdown and safe-area control are included in this device which is packaged in TO-3 and TO-220 packages. The UC117 is rated for operation from -55°C to +150°C, the UC217 from -25°C to +150°C and the UC317 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally limited
Input—Output Voltage Differential	40V
Operating Junction Temperature Range	
UC117	-55°C to +150°C
UC217	-25°C to +150°C
UC317	0°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL APPLICATIONS



ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	TEST CONDITIONS	UC117/UC217			UC317			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	$T_A = 25^\circ\text{C}$, $3\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$, (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_{OUT} \leq I_{MAX}$ $V_{OUT} \leq 15\text{V}$, (Note 2) $V_{OUT} \geq 5\text{V}$, (Note 2)		5 0.1	15 0.3		5 0.1	25 0.5	mV %
Thermal Regulation	$T_A = 25^\circ\text{C}$, 20ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\text{mA} \leq I_L \leq I_{MAX}$ $2.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$ $10\text{mA} \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3 \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\text{mA} \leq I_{OUT} \leq I_{MAX}$, (Note 2) $V_{OUT} \leq 5\text{V}$ $V_{OUT} \geq 5\text{V}$		20 0.3	50 1		20 0.3	70 1.5	mV %
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 40\text{V}$		3.5	5		3.5	10	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 15\text{V}$ K Package T Package $(V_{IN} - V_{OUT}) = 40\text{V}$ K Package T Package	1.5 1.5	2.2 2.2		1.5 1.5	2.2 2.2		A A A A
RMS Output Noise	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10\text{V}$, $f = 120\text{Hz}$ $C_{ADJ} = 10\mu\text{F}$	66	65 80		66	65 80		dB dB
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs.		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package T Package		2.3	3		2.3	3	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:

UC117: $-55^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$

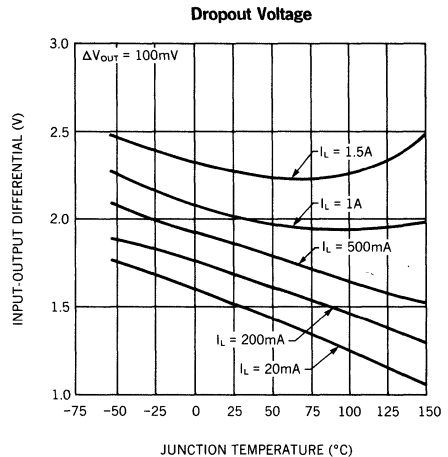
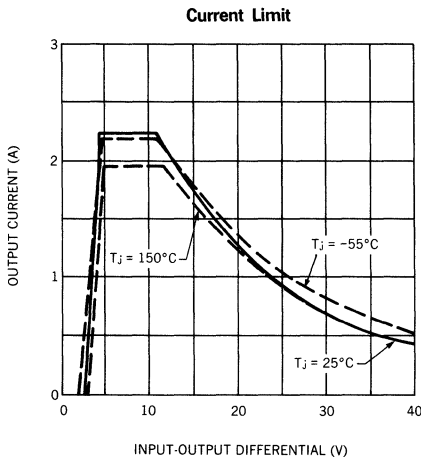
UC217: $-25^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$

UC317: $0^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$

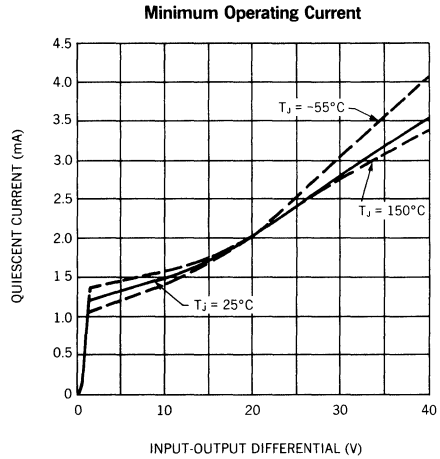
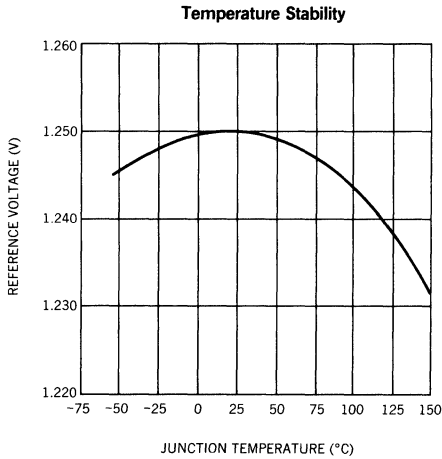
$(V_{IN} - V_{OUT}) = 5\text{V}$, $I_O = 0.5\text{A}$, $I_{MAX} = 1.5\text{A}$

2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS



3

MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

UC117 UC217 UC317

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)

UC317

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

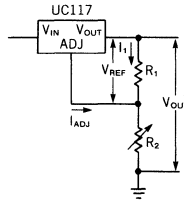
T(TO-220)

Note: When ordering, add suffix "K" (for TO-3 package) or "T" (for TO-220 package) to the Part Number.

APPLICATION HINTS

In operation, the UC117 develops a nominal 1.25V reference voltage, V_{REF} , between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2 , giving an output voltage of

$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

**Figure 1**

Since the 100 μ A current from the adjustment terminal represents an error term, the UC117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μ F disc or 1 μ F solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the UC117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μ F bypass capacitor 80 dB ripple rejection is obtainable at any output level.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μ F in aluminum electrolytic to equal 1 μ F solid tantalum at high frequencies.

Although the UC117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500pF and 5000pF. A 1 μ F solid tantalum (or 25 μ F aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The UC117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240 Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation.

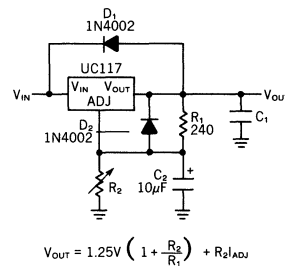
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor by using 2 separate leads to the case. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μ F capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN} . In the UC117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μ F or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when either the input or output is shorted. Internal to the UC117 is a 50 Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μ F capacitance. Figure 2 shows a UC117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1} \right) + R_2 I_{ADJ}$$

D_1 protects against C_1
 D_2 protects against C_2

Figure 2. Regulator with Protection Diodes

LINEAR INTEGRATED CIRCUITS

1.5A, Three Terminal Adjustable Negative Voltage Regulators

UC137
UC237
UC337

3

FEATURES

- Output voltage adjustable from -1.2 to -37V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- Standard 3-lead transistor packages (TO-3, TO-220)

DESCRIPTION

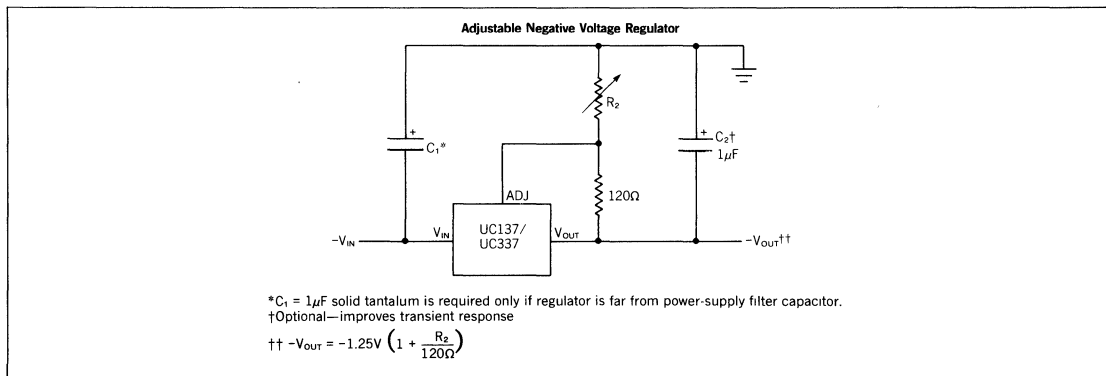
The UC137/UC237/UC337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of -1.5A over an output voltage range of -1.2V to -37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the UC137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The UC137/UC237/UC337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The UC137/UC237/UC337 are ideal complements to the UC117/UC217/UC317 adjustable positive regulators. These devices are available in TO-3 and TO-220 packages. The UC137 is rated for operation from -55°C to +150°C, the UC237 from -25°C to +150°C and the UC337 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally limited
Input—Output Voltage Differential	40V
Operating Junction Temperature Range	
UC137	-55°C to +150°C
UC237	-25°C to +150°C
UC337	0°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	TEST CONDITIONS	UC137/UC237			UC337			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	$T_A = 25^\circ\text{C}$, $3\text{V} \leq V_{IN} - V_{OUT} \leq 40\text{V}$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_{OUT} \leq I_{MAX}$ $ V_{OUT} \leq 5\text{V}$, (Note 2) $ V_{OUT} \geq 5\text{V}$, (Note 2)		15 0.3	25 0.5		15 0.3	50 1.0	mV %
Thermal Regulation	$T_A = 25^\circ\text{C}$, 10ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\text{mA} \leq I_L \leq I_{MAX}$ $2.5\text{V} \leq V_{IN} - V_{OUT} \leq 40\text{V}$, $T_A = 25^\circ\text{C}$		2	5		2	5	μA
Reference Voltage	$T_A = 25^\circ\text{C}$ $3 \leq V_{IN} - V_{OUT} \leq 40\text{V}$ $10\text{mA} \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	-1.225 -1.200	-1.250 -1.250	-1.275 -1.300	-1.213 -1.200	-1.250 -1.250	-1.287 -1.300	V V
Line Regulation	$3\text{V} \leq V_{IN} - V_{OUT} \leq 40\text{V}$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\text{mA} \leq I_{OUT} \leq I_{MAX}$, (Note 2) $ V_{OUT} \leq 5\text{V}$ $ V_{OUT} \geq 5\text{V}$		20 0.3	50 1		20 0.3	70 1.5	mV %
Temperature Stability	$T_{MIN} \leq T_J \leq T_{MAX}$		0.6			0.6		%
Minimum Load Current	$ V_{IN} - V_{OUT} \leq 40\text{V}$ $ V_{IN} - V_{OUT} \leq 10\text{V}$		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
Current Limit	$ V_{IN} - V_{OUT} \leq 15\text{V}$ K Package T Package $ V_{IN} - V_{OUT} = 40\text{V}$ K Package T Package	1.5 1.5	2.2 2.2		1.5 1.5	2.2 2.2		A A A A
RMS Output Noise	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10\text{V}$, $f = 120\text{Hz}$ $C_{ADJ} = 10\mu\text{F}$	66	60 77		66	60 77		dB dB
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package T Package		2.3	3		2.3 4	3	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:

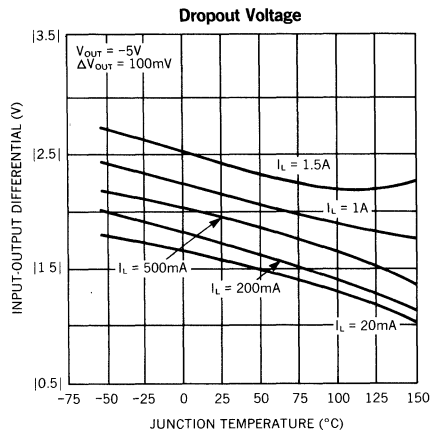
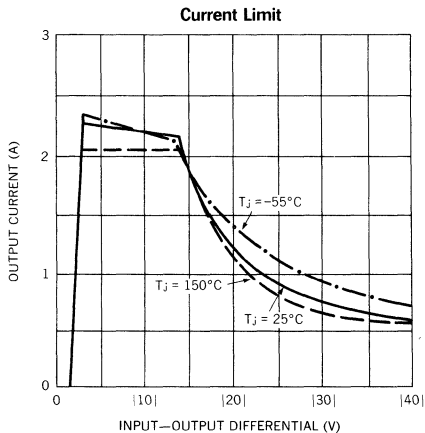
UC137: $-55^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$

UC237: $-25^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$

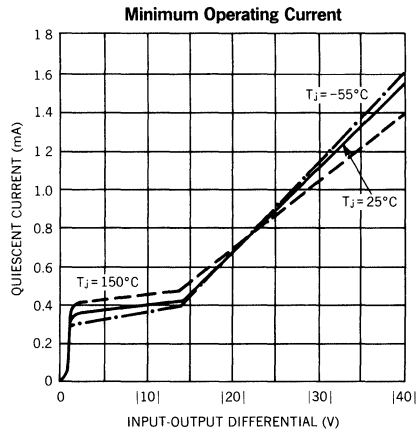
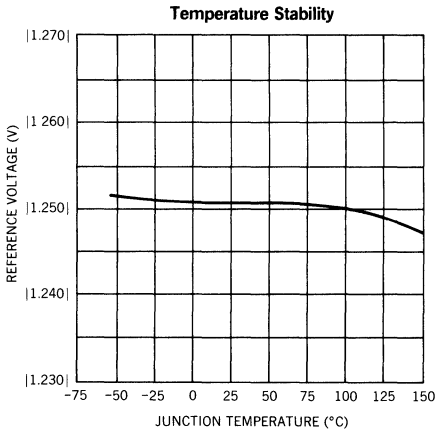
UC337: $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$

$|V_{IN} - V_{OUT}| = 5\text{V}$, $I_O = 0.5\text{A}$, $I_{MAX} = 1.5\text{A}$

2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.



TYPICAL PERFORMANCE CHARACTERISTICS



3

MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

UC137 UC237 UC337

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

Bottom View

TO-204AA K(TO-3)

UC337

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

1-Adjustment
2-Output
3-Input
4-Input

T(TO-220)

Note: When ordering, add suffix "K" (for TO-3 package) or "T" (for TO-220 package) to the Part Number.

LINEAR INTEGRATED CIRCUITS

3A, Three Terminal Adjustable Positive Voltage Regulators

UC150
UC250
UC350

FEATURES

- Output voltage adjustable from 1.2V to 33V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- Standard 3-lead transistor package

DESCRIPTION

The UC150/UC250/UC350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs.

In addition to higher performance than fixed regulators, the UC150 series offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

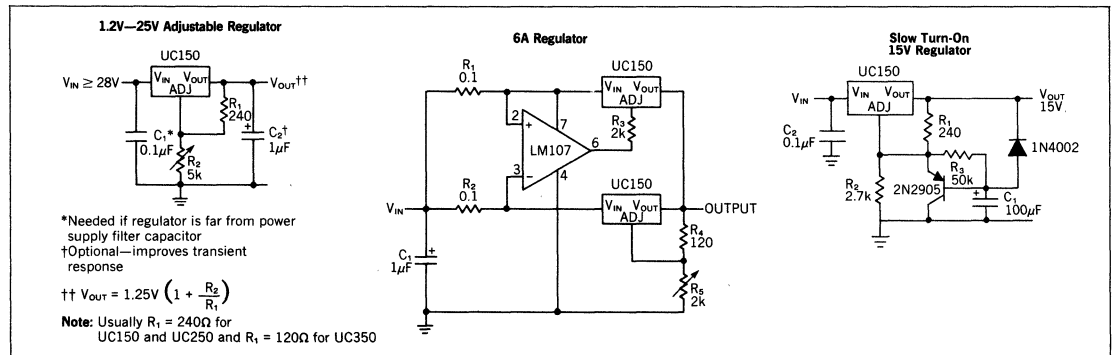
Supplies requiring electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The UC150/UC250/UC350 are packaged in standard TO-3 transistor packages. The UC150 is rated for operation from -55°C to +150°C, the UC250 from -25°C to +150°C and the UC350 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally limited
Input—Output Voltage Differential.....	35V
Operating Junction Temperature Range	
UC150	-55°C to +150°C
UC250	-25°C to +150°C
UC350	0°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL APPLICATIONS



ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	TEST CONDITIONS	UC150/UC250			UC350			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	$T_A = 25^\circ\text{C}$, $3V \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_{OUT} \leq 3A$ $V_{OUT} \leq 5V$, (Note 2) $V_{OUT} \geq 5V$, (Note 2)		5 0.1	15 0.3		5 0.1	25 0.1	mV %
Thermal Regulation	Pulse = 20ms		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\text{mA} \leq I_L \leq 3A$ $3V \leq (V_{IN} - V_{OUT}) \leq 35V$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 35V$, $10\text{mA} \leq I_{OUT} \leq 3A$, $P \leq 30W$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3 \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$V_{OUT} \leq 5V$ $10\text{mA} \leq I_{OUT} \leq 3A$, (Note 2) $V_{OUT} \geq 5V$		20 0.3	50 1		20 0.3	70 1.5	mV %
Temperature Stability	$T_{MIN} \leq T_J \leq T_{MAX}$		1			1		%
Minimum Load Current	$(V_{IN} - V_{OUT}) = 35V$		3.5	5		3.5	10	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 10V$ $(V_{IN} - V_{OUT}) = 30V$	3.0	4.5 1		3.0	4.5 1		A A
RMS Output Noise	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, $f = 120\text{Hz}$ $C_{ADJ} = 10\mu\text{F}$	66	65 86		66	65 86		dB dB
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs.		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case				1.5			1.5	$^\circ\text{C}/\text{W}$

Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:

UC150: $-55^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$

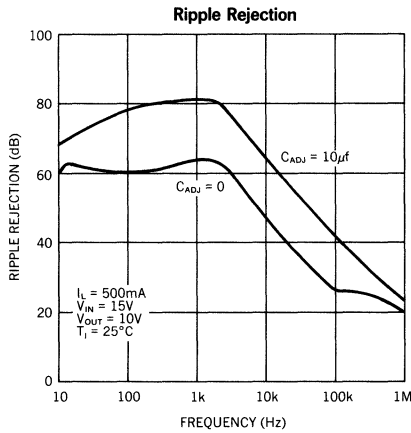
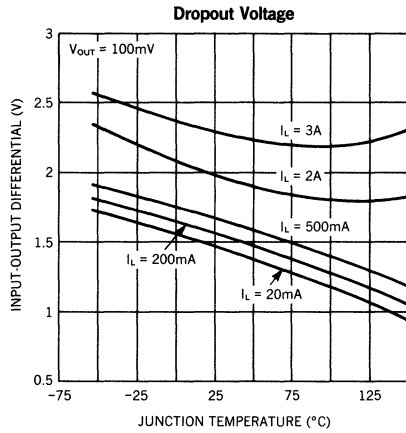
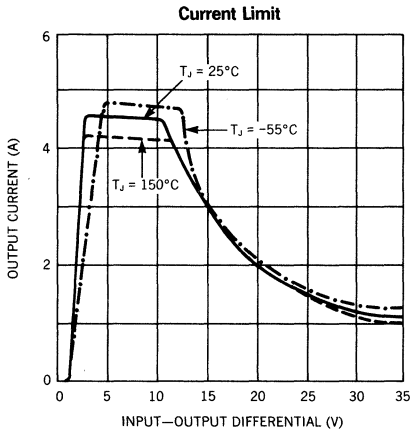
UC250: $-25^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$

UC350: $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$

$(V_{IN} - V_{OUT}) = 5V$, $I_{OUT} = 1.5A$

2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS



MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAM

Bottom View

UC150 UC250 UC350

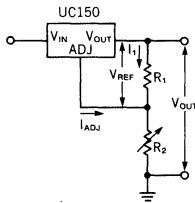
	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)

APPLICATION HINTS

In operation, the UC150 develops a nominal 1.25V reference voltage, V_{REF} , between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2 , giving an output voltage of

$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ}R_2$$

**Figure 1**

Since the $50\mu\text{A}$ current from the adjustment terminal represents an error term, the UC150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A $0.1\mu\text{F}$ disc or $1\mu\text{F}$ solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the UC150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a $10\mu\text{F}$ bypass capacitor 86 dB ripple rejection is obtainable at any output level.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about $25\mu\text{F}$ in aluminum electrolytic to equal $1\mu\text{F}$ solid tantalum at high frequencies.

Although the UC150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500pF and 5000pF . A $1\mu\text{F}$ solid tantalum (or $25\mu\text{F}$ aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The UC150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation.

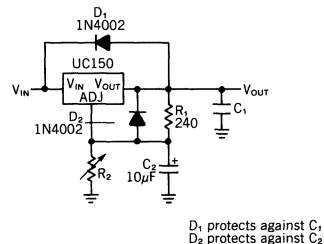
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor by using 2 separate leads to the case. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most $10\mu\text{F}$ capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharged current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN} . In the UC150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of $25\mu\text{F}$ or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the UC150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and $10\mu\text{F}$ capacitance. Figure 2 shows a UC150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



D_1 protects against C_1
 D_2 protects against C_2

$$V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1} \right) + R_2 I_{ADJ}$$

Figure 2. Regulator with Protection Diodes

LINEAR INTEGRATED CIRCUITS

Advanced Regulating Pulse Width Modulators

UC493A UC493AC
 UC494A UC494AC
 UC495A UC495AC
 UC495B UC495BC

FEATURES

- Dual uncommitted 40V, 200mA output transistors
- 1% accurate 5V reference
- Dual error amplifiers
- Wide range, variable deadtime
- Single-ended or push-pull operation
- Under-voltage lockout with hysteresis
- Double pulse protection
- Master or slave oscillator operation
- UC493A/UC495B: Built in 80mV threshold for current limiting
- UC495A/UC495B: Internal 39V zener diode
- UC495A/UC495B: Buffered steering control

DESCRIPTION

This entire series of PWM modulators each provide a complete pulse width modulation system in a single monolithic integrated circuit. These devices include a 5V reference accurate to $\pm 1\%$, two independent amplifiers usable for both voltage and current sensing, an externally synchronizable oscillator with its linear ramp generator, and two uncommitted transistor output switches. These two outputs may be operated either in parallel for single-ended operation or alternating for push-pull applications with an externally controlled dead-band. These units are internally protected against double-pulsing of a single output or from extraneous output signals when the input supply voltage is below minimum.

The UC495A and UC495B also contain an on-chip 39V zener diode for high-voltage applications where V_{cc} would be greater than 40V, and a buffered output steering control that overrides the internal control of the pulse steering flip-flop.

UC493A and UC494A are packaged in a 16-pin DIP, while the UC495A and UC495B are packaged in an 18-pin DIP. The UC493A, UC494A, UC495A and UC495B are specified for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$, while the UC493AC, UC494AC, UC495AC and UC495BC are designed for industrial applications from 0°C to $+70^{\circ}\text{C}$.

ABSOLUTE MAXIMUM RATINGS (Note 1)

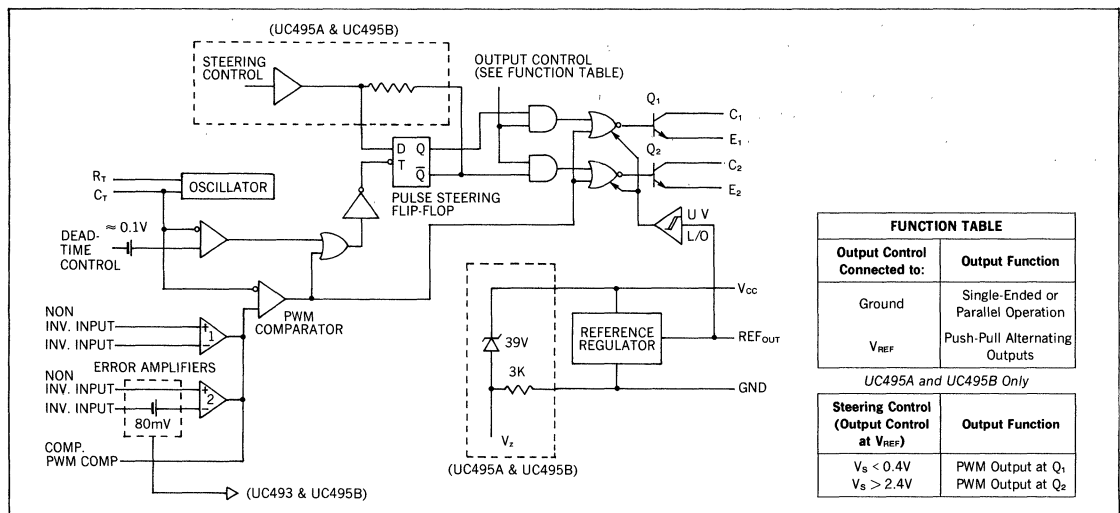
Supply Voltage, V_{cc} (Note 2)	45V
Amplifier Input Voltages	$V_{cc} + 0.3\text{V}$
Collector Output Voltage	41V
Collector Output Current	250mA
Continuous Total Dissipation	1000mW
@ (or below) 25°C free air temperature range (Note 3)	
Storage Temperature Range	-65° to $+150^{\circ}\text{C}$
Lead Temperature $1/16"$ (1.6mm) from case for 60 seconds, J Package	300°C
Lead Temperature $1/16"$ (1.6mm) from case for 10 seconds, N Package	260°C

- Notes:**
1. Over operating free air temperature range unless otherwise noted.
 2. All voltage values are with respect to network ground terminal.
 3. For J package, derate at $8.2\text{mW}/^{\circ}\text{C}$ for ambient temperature above $+28^{\circ}\text{C}$. For N package, derate at $9.2\text{mW}/^{\circ}\text{C}$ for ambient temperature above $+41^{\circ}\text{C}$.

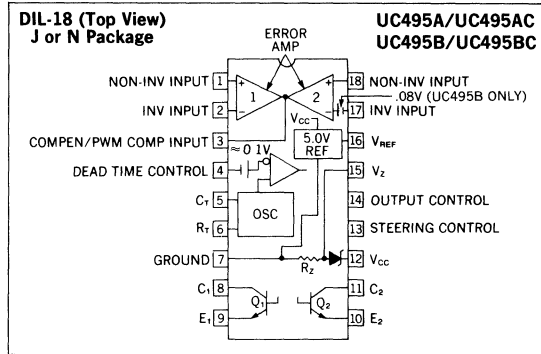
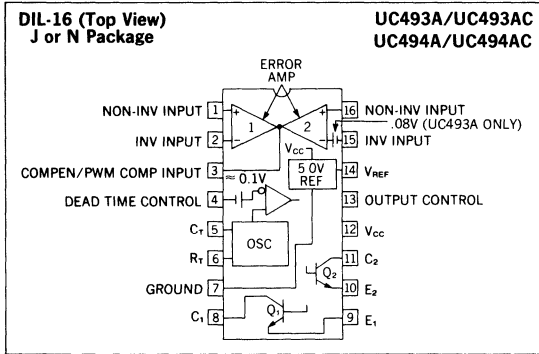
RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{cc}	7V to 40V
Error Amplifier Input Voltages	-0.3V to $V_{cc}-2\text{V}$
Collector Output Voltage	40V
Collector Output Current (each transistor)	200mA
Current into Feedback Terminal	0.3mA
Timing Capacitor, C_T	0.47nF to 10,000nF
Timing Resistor, R_T	1.8k Ω to 500k Ω
Oscillator Frequency	1kHz to 300kHz
Operating Free Air Temperature	
UC493A, UC494A, UC495A, UC495B	-55°C to $+125^{\circ}\text{C}$
UC493AC, UC494AC, UC495AC, UC495BC	0°C to $+70^{\circ}\text{C}$

BLOCK DIAGRAM



CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, over recommended operating free-air temperature range, $V_{CC} = 15V$, $f = 10kHz$.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Reference Section						
Output Voltage (V_{REF})	$I_O = 1mA$, $T_A = 25^\circ C$	4.95	5	5.05	V	
Input Regulation	$V_{CC} = 7V$ to $40V$		2	25	mV	
Output Regulation	$I_O = 1mA$ to $10mA$		1	15	mV	
Output Voltage over Temperature	$\Delta T_A = \text{Min. to Max.}$	4.90		5.10	V	
Short Circuit Output Current (Note 1)	$V_{REF} = 0$, $T_A = 25^\circ C$	10	35	50	mA	
Oscillator Section						
Frequency (Note 2)	$C_T = 0.01\mu F$, $R_T = 12k\Omega$		10		kHz	
Standard Deviation of Frequency (Note 3)	All values of V_{CC} , C_T , R_T , T_A constant		10		%	
Frequency Change with Voltage	$V_{CC} = 7V$ to $40V$, $T_A = 25^\circ C$		0.1		%	
Frequency Change with Temperature	$C_T = 0.01\mu F$, $R_T = 12k\Omega$ $\Delta T_A = \text{Min. to Max.}$			2	%	
Deadtime Control Section (Output Control connected to V_{REF})						
Input Bias Current (Pin 4)	$V_{(PIN 4)} = 0V$ to $5.25V$		-2	-10	μA	
Maximum Duty-Cycle (Each Output)	$V_{(PIN 4)} = 0V$	45			%	
Input Threshold Voltage (Pin 4)	Zero Duty-Cycle		3	3.3	V	
	Maximum Duty-Cycle	0				
Amplifier Section (Current Limit specifications apply to UC493A and UC495B only)						
Input Offset Voltage	Error	$V_O (PIN 3) = 2.5V$		2	10	mV
	Current Limit		70	80	90	
Input Offset Current		$V_O (PIN 3) = 2.5V$		25	250	nA
Input Bias Current	Error	$V_O (PIN 3) = 2.5V$		-0.2	-1	μA
	Current Limit			-1	-2	
Common-Mode Input Voltage Range		$V_{CC} = 7V$ to $40V$	0.3 to $V_{CC} - 2$			V
Open Loop Voltage Gain	Error	$\Delta V_O = 3V$, $V_O = 0.5V$ to $3.5V$	70	95		dB
	Current Limit		66	90		
Unity Gain Bandwidth			800			kHz
Common-Mode Rejection Ratio	Error	$V_{CC} = 40V$, $T_A = 25^\circ C$	65	80		dB
	Current Limit		50	70		
Output Sink Current (Pin 3)		$V_{ID} = -15mV$ to $-5V$, $V_{(PIN 3)} = 0.7V$	0.3	0.7		mA
Output Source Current (Pin 3)		$V_{ID} = 15mV$ to $5V$, $V_{(PIN 3)} = 3.5V$	-2			mA

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, over recommended operating free-air temperature range, $V_{CC} = 15V$, $f = 10kHz$.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Section					
Collector Off-State Current	$V_{CE} = 40V$, $V_{CC} = 40V$		2	100	μA
Emitter Off-State Current	$V_{CC} = V_C = 40V$, $V_E = 0$			-100	μA
Collector-Emitter Saturation Voltage	Common-Emitter	$V_E = 0$, $I_C = 200mA$	1.1	1.3	V
	Emitter-Follower	$V_C = 15V$, $I_E = -200mA$	1.5	2.5	
Output Control Input Current	$V_I = V_{REF}$			3.5	mA
PWM Comparator Section					
Input Threshold Voltage (Pin 3)	Zero Duty-Cycle		4	4.5	V
Input Sink Current (Pin 3)	$V_{(PIN\ 3)} = 0.7V$	0.3	0.7		mA
Steering Control (UC495A and UC495B only, see Function Table)					
Input Current	$V_{(PIN\ 13)} = 0.4V$, Q_1 active			-200	μA
	$V_{(PIN\ 13)} = 2.4V$, Q_2 active			300	
Deadband			500		mV
Zener Diode Circuit (UC495A and UC495B only)					
Breakdown Voltage	$V_{CC} = 45V$, $I_Z = 2mA$	36	39	45	V
Sink Current	$V_{(PIN\ 15)} = 1V$	0.2	0.3	0.6	mA
Total Device					
Standby Supply Current	Pin 6 at V_{REF} . All other inputs and outputs open.	$V_{CC} = 15V$	6	10	mA
		$V_{CC} = 40V$	9	15	
Under-Voltage Lockout		3.5		6.5	V
Hysteresis			300		mV
Switching Characteristics ($T_A = 25^\circ C$)					
Output Voltage Rise Time	Common-Emitter Configuration		100	200	ns
Output Voltage Fall Time	$R_L = 68\Omega$, $C_L = 15pF$		25	100	ns
Output Voltage Rise Time	Emitter-Follower Configuration		100	200	ns
Output Voltage Fall Time	$R_L = 68\Omega$, $C_L = 15pF$		40	100	ns

Notes: 1. Duration of the short circuit should not exceed one second.

2. Frequency for other values of C_T and R_T is approximately $f = \frac{1.1}{R_T C_T}$

3. Standard deviation is a measure of the statistical distribution about the mean as derived from the formula

$$\sigma = \sqrt{\frac{\sum_{n=1}^n (x_n - \bar{x})^2}{n - 1}}$$

Figure 1. Slaving Two or More Control Circuits

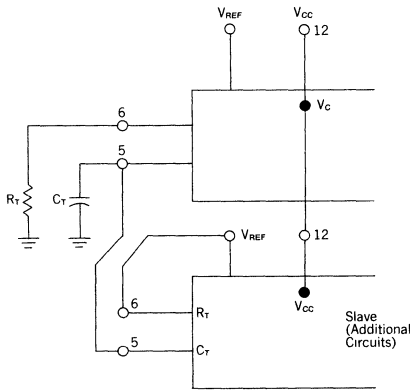


Figure 2. Output Circuit of Error Amplifiers

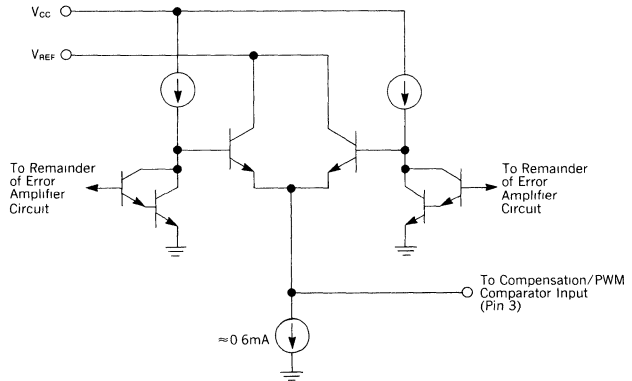


Figure 3. Output Connections for Single-Ended and Push-Pull Configurations

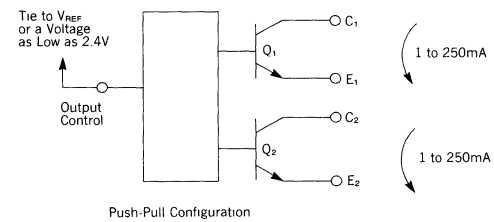
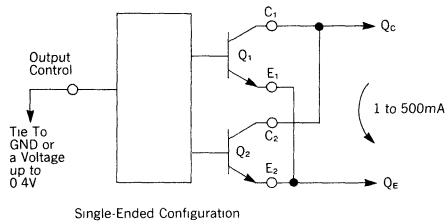


Figure 4. Internal Buffer with Deadband for Steering Control on UC495A and UC495B

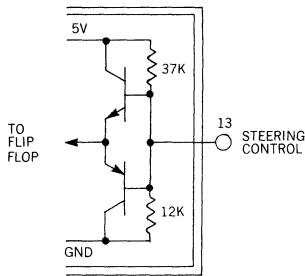


Figure 5. Operation with $V_{IN} > 40V$ Using Internal Zener (UC495A and UC495B Only)

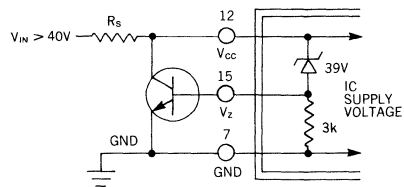
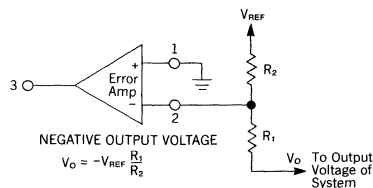
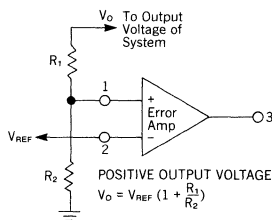


Figure 6. Error Amplifier Sensing Techniques



LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulators

UC1524
UC2524
UC3524

FEATURES

- Complete PWM Power control circuitry
- Uncommitted outputs for single-ended or push-pull applications
- Low standby current ... 8mA typical
- Interchangeable with SG1524, SG2524 and SG3524, respectively

DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. The UC2524 and UC3524 are designed for operation from -25°C to $+85^{\circ}\text{C}$ and 0°C to $+70^{\circ}\text{C}$, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC} (Notes 2 and 3)	40V
Collector Output Current	100mA
Reference Output Current	50mA
Current Through C_T Terminal	-5mA
Power Dissipation at $T_A = +25^{\circ}\text{C}$ (Note 4)	1000mW
Thermal Resistance, Junction to Ambient	$100^{\circ}\text{C}/\text{W}$
Power Dissipation at $T_c = +25^{\circ}\text{C}$ (Note 5)	2000mW
Thermal Resistance, Junction to Case	$60^{\circ}\text{C}/\text{W}$
Operating Junction Temperature Range	-55°C to $+150^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$

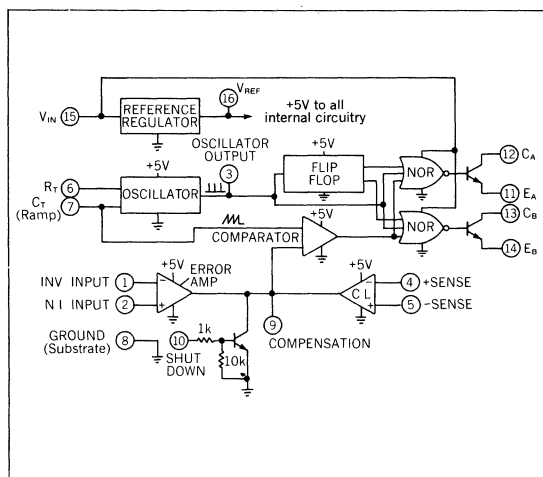
Notes: 1. Over operating free-air temperature range unless otherwise noted.

2. All voltage values are with respect to the ground terminal, pin 8
3. The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.
4. Derate at $10\text{mW}/^{\circ}\text{C}$ for ambient temperatures above $+50^{\circ}\text{C}$
5. Derate at $16\text{mW}/^{\circ}\text{C}$ for case temperatures above $+25^{\circ}\text{C}$

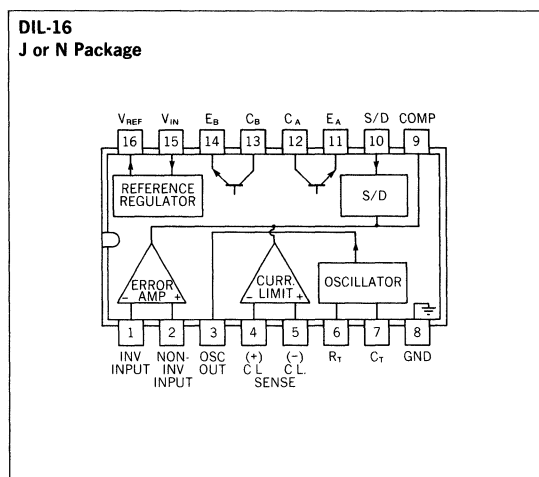
RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}	8V to 40V
Reference Output Current	0 to 20mA
Current through C_T Terminal	-0.03mA to -2mA
Timing Resistor, R_T	$1.8\text{K}\Omega$ to $100\text{K}\Omega$
Timing Capacitor, C_T	$0.001\mu\text{F}$ to $0.1\mu\text{F}$
Operating Ambient Temperature Range	
UC1524	-55°C to $+125^{\circ}\text{C}$
UC2524	-25°C to $+85^{\circ}\text{C}$
UC3524	0°C to $+70^{\circ}\text{C}$

BLOCK DIAGRAM



CONNECTION DIAGRAM

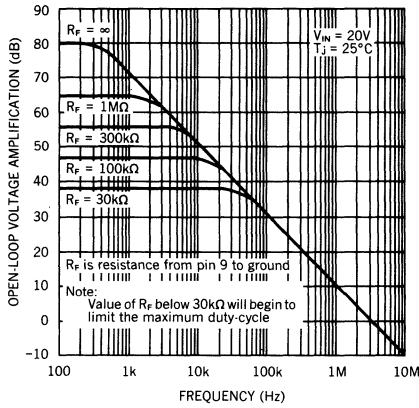


ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1524, -25°C to $+85^\circ\text{C}$ for the UC2524, and 0°C to $+70^\circ\text{C}$ for the UC3524, $V_{IN} = 20\text{V}$, and $f = 20\text{kHz}$)

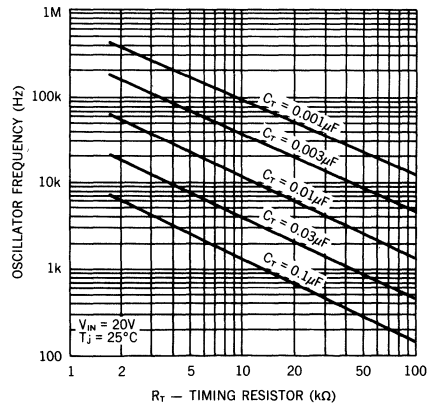
PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	$V_{IN} = 8$ to 40V		10	20		10	30	mV
Load Regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Ripple Rejection	$f = 120\text{Hz}$, $T_j = 25^\circ\text{C}$		66			66		dB
Short Circuit Current Limit	$V_{REF} = 0$, $T_j = 25^\circ\text{C}$		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	$T_j = 125^\circ\text{C}$, $t = 1000$ Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	$C_T = .001\text{mfd}$, $R_T = 2\text{k}\Omega$		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	$V_{IN} = 8$ to 40V , $T_j = 25^\circ\text{C}$			1			1	%
Temperature Stability	Over Operating Temperature Range			2			2	%
Output Amplitude	Pin 3, $T_j = 25^\circ\text{C}$		3.5			3.5		V
Output Pulse Width	$C_T = .01\text{mfd}$, $T_j = 25^\circ\text{C}$		0.5			0.5		μs
Error Amplifier Section								
Input Offset Voltage	$V_{CM} = 2.5\text{V}$		0.5	5		2	10	mV
Input Bias Current	$V_{CM} = 2.5\text{V}$		2	10		2	10	μA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	$T_j = 25^\circ\text{C}$	1.8		3.4	1.8		3.4	V
Common Mode Rejection Ratio	$T_j = 25^\circ\text{C}$		70			70		dB
Small Signal Bandwidth	$A_V = 0\text{dB}$, $T_j = 25^\circ\text{C}$		3			3		MHz
Output Voltage	$T_j = 25^\circ\text{C}$	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		μA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, $T_j = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/ $^\circ\text{C}$
Common Mode Voltage		-1		+1	-1		+1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	μA
Saturation Voltage	$I_C = 50\text{mA}$		1	2		1	2	V
Emitter Output Voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V
Rise Time	$R_C = 2\text{K ohm}$, $T_j = 25^\circ\text{C}$		0.2			0.2		μs
Fall Time	$R_C = 2\text{K ohm}$, $T_j = 25^\circ\text{C}$		0.1			0.1		μs
Total Standby Current	$V_{IN} = 40\text{V}$		8	10		8	10	mA
(Excluding oscillator charging current, error and current limit dividers, and with outputs open)								

TYPICAL CHARACTERISTICS

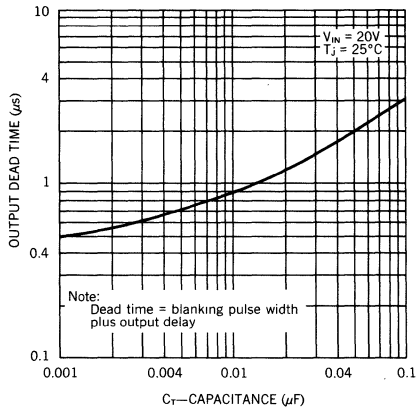
Open-Loop Voltage Amplification of Error Amplifier vs Frequency



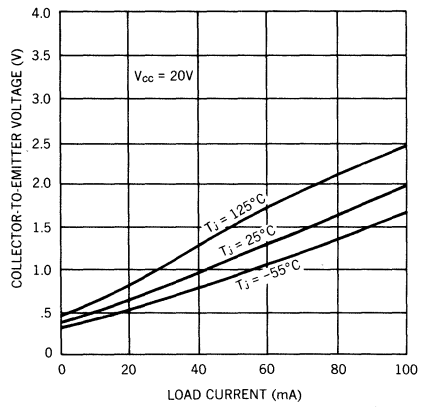
Oscillator Frequency vs Timing Components



Output Dead Time vs Timing Capacitance Value



Output Saturation Voltage vs Load Current



PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T . This results in a linear voltage ramp at C_T , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T . The resulting modulated pulse out of the high-gain comparator is

then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

3

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \approx \frac{1.18}{R_T C_T}$$

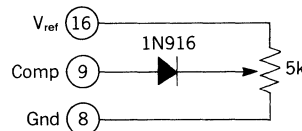
where R_T is in kilohms
 C_T is in microfarads
 f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T . If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty

cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

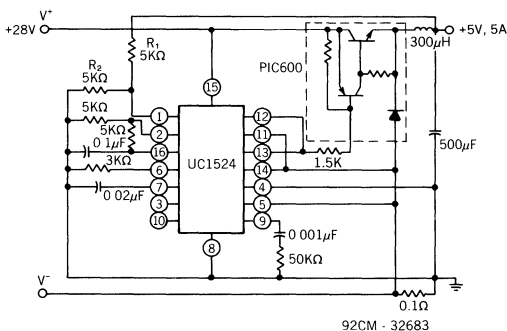


Synchronous Operation

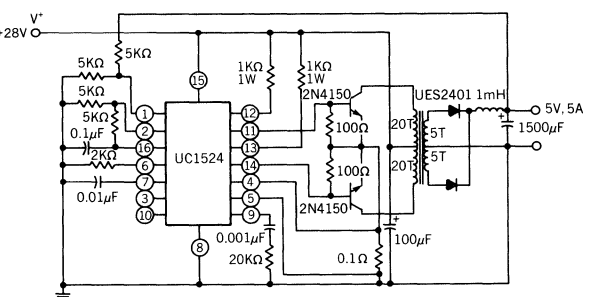
When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration $R_T C_T$ must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF} . Minimum lead lengths should be used between the C_T terminals.

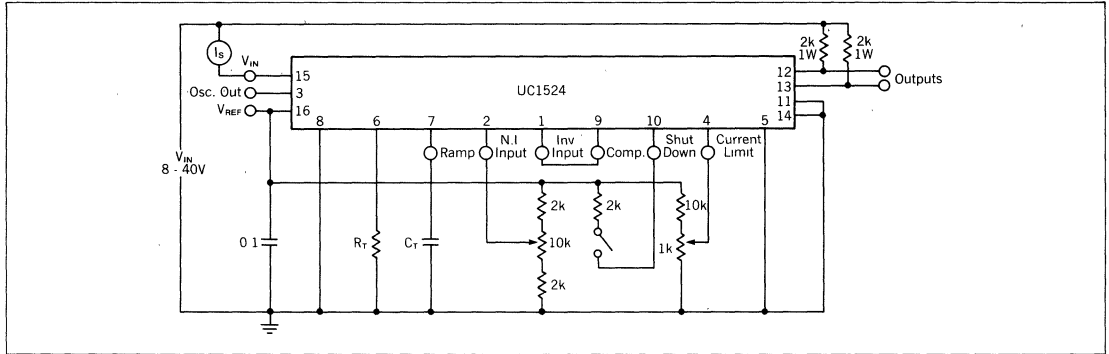
Single-Ended LC Switching Regulator Circuit



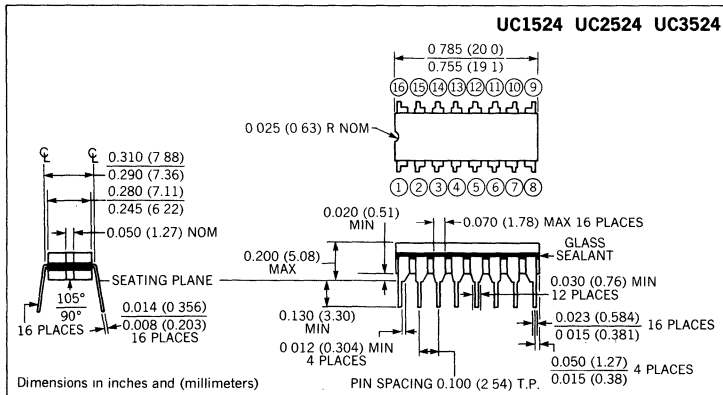
Push-Pull Transformer-Coupled Circuit



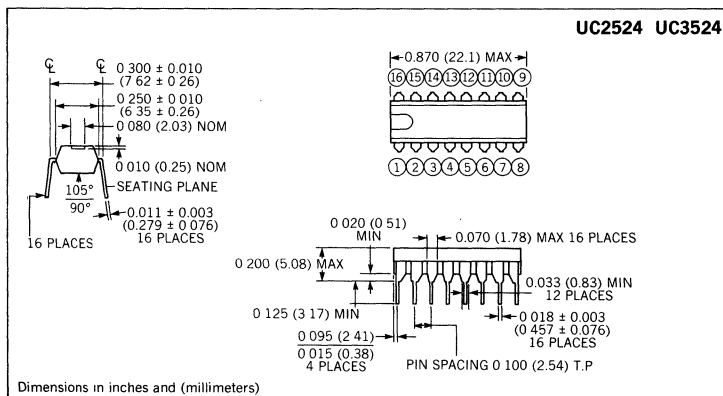
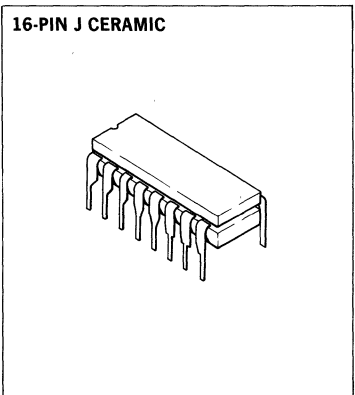
OPEN LOOP TEST CIRCUIT



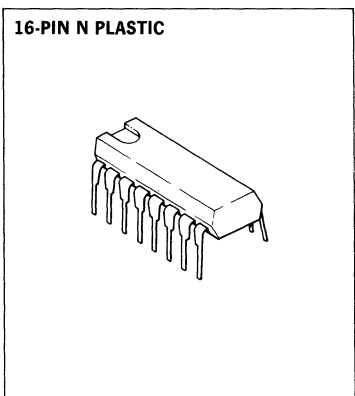
MECHANICAL SPECIFICATIONS



16-PIN J CERAMIC



16-PIN N PLASTIC



Note: When ordering, add suffix "J" (for 16 pin ceramic package) or "N" (for 16 pin plastic package) to the part number.

LINEAR INTEGRATED CIRCUITS

Advanced Regulating Pulse Width Modulators

UC1524A
UC2524A
UC3524A

3

FEATURES

- Fully interchangeable with standard UC1524 family
- Precision reference internally trimmed to $\pm 1\%$
- High-Performance current limit function
- Under-voltage lockout with hysteretic turn-on
- Start-up supply current less than 4mA
- Output current to 200mA
- 60V output capability
- Wide common-mode input range for both error and current limit amplifiers
- PWM latch insures single pulse per period
- Double pulse suppression logic
- 200ns shutdown through PWM latch
- Guaranteed frequency accuracy
- Thermal shutdown protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to $\pm 1\%$ accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

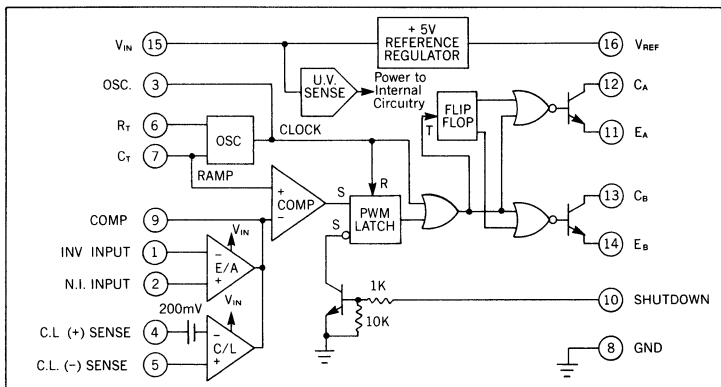
Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to $+125^{\circ}\text{C}$. The UC2524A and UC3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to $+85^{\circ}\text{C}$ and 0°C to 70°C , respectively.

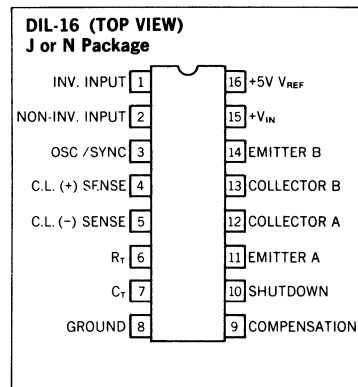
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN})	40V
Collector Supply Voltage (V_C)	60V
Output Current (Each Output)	200mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at $T_A = +25^{\circ}\text{C}$	1000mW
Derate above $+50^{\circ}\text{C}$	10mW/ $^{\circ}\text{C}$
Power Dissipation at $T_C = +25^{\circ}\text{C}$	2000mW
Derate for Case Temperature above $+25^{\circ}\text{C}$	16mW/ $^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 10 seconds)	$+300^{\circ}\text{C}$

BLOCK DIAGRAM



CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1524A, -25°C to $+85^\circ\text{C}$ for the UC2524A, and 0°C to $+70^\circ\text{C}$ for the UC3524A; $V_{IN} = V_C = 20\text{V}$.)

PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		5.5	7.5	8.5	5.5	7.5	8.5	V
Turn-on Current	$V_{IN} = 6\text{V}$		2.5	4		2.5	4	mA
Operating Current	$V_{IN} = 8$ to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.6			0.6		V
Reference Section								
Output Voltage	$T_j = 25^\circ\text{C}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$V_{IN} = 10$ to 40V		10	20		10	30	mV
Load Regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Temperature Stability*	Over Operating Range*		20	50		20	50	mV
Short Circuit Current	$V_{REF} = 0$, $T_j = 25^\circ\text{C}$		80	100		80	100	mA
Output Noise Voltage*	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_j = 25^\circ\text{C}$		40			40		μV_{rms}
Long Term Stability*	$T_j = 125^\circ\text{C}$, 1000 Hrs.		20	50		20	50	mV
Oscillator Section (Unless otherwise specified, $R_T = 2700\Omega$, $C_T = 0.01$ mfd)								
Initial Accuracy	$T_j = 25^\circ\text{C}$	41	43	45	39	43	47	kHz
Temperature Stability	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency*	$R_T = 150\text{k}\Omega$, $C_T = 0.1$ mfd			140			120	Hz
Maximum Frequency	$R_T = 2.0\text{k}\Omega$, $C_T = 470$ pF	500			500			kHz
Output Amplitude*	$T_j = 25^\circ\text{C}$		3.5			3.5		V
Output Pulse Width*	$T_j = 25^\circ\text{C}$		0.5			0.5		μs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	$T_j = 25^\circ\text{C}$	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/ $^\circ\text{C}$
Error Amplifier Section (Unless otherwise specified, $V_{CM} = 2.5\text{V}$)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current			.05	1		0.5	1	μA
Common Mode Rejection Ratio	$V_{CM} = 1.5$ to 5.5V	60	75		60	75		dB
Power Supply Rejection Ratio	$V_{IN} = 10$ to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open Loop Voltage Gain	$\Delta V_O = 1$ to 4V , $R_L \geq 10$ Meg Ω	72	80		60	80		dB
Gain-Bandwidth*	$T_j = 25^\circ\text{C}$, $A_V = 0\text{dB}$	1	3		1	3		MHz
DC Transconductance**†	$T_j = 25^\circ\text{C}$, $30\text{k}\Omega \leq R_L \leq 1\text{M}\Omega$	1.7	2.3		1.7	2.3		mS

* These parameters are guaranteed by design but not 100% tested in production.

† DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground.

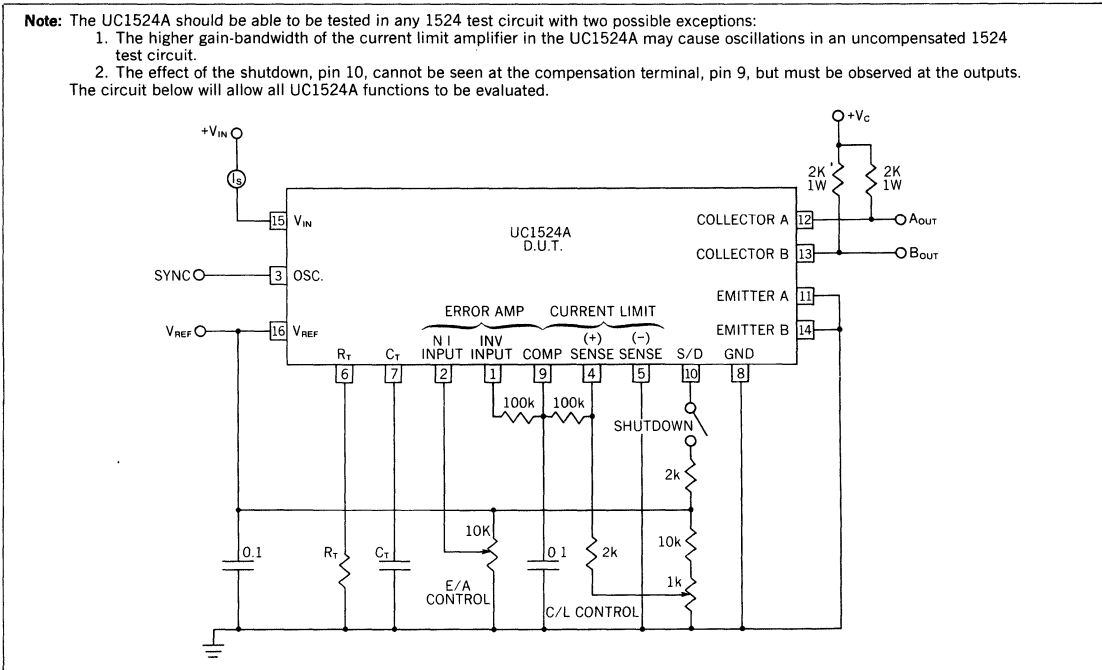
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

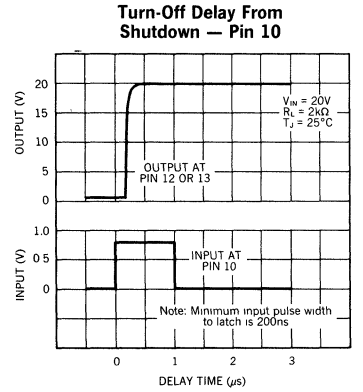
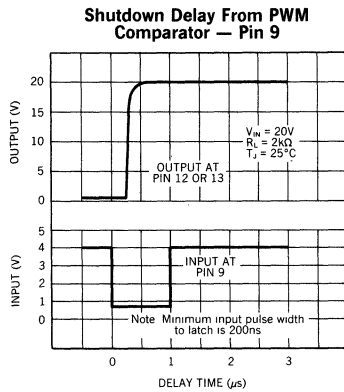
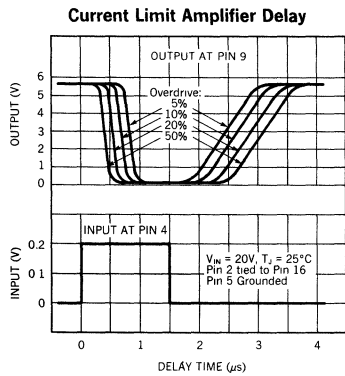
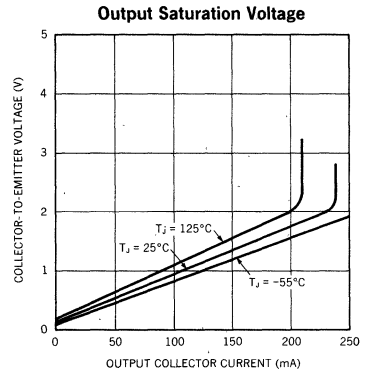
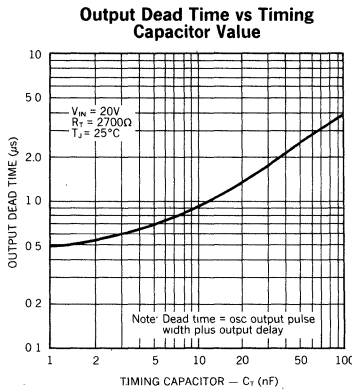
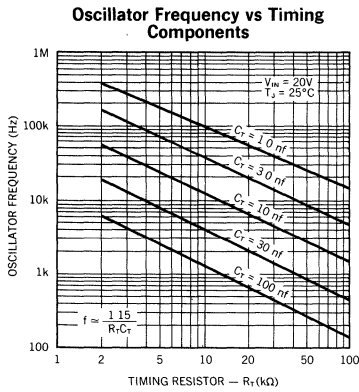
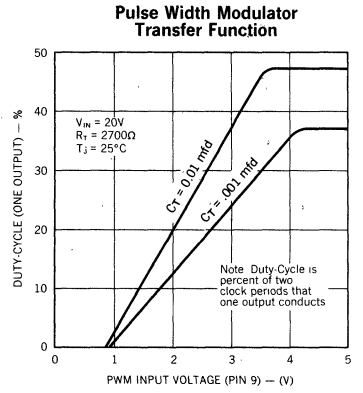
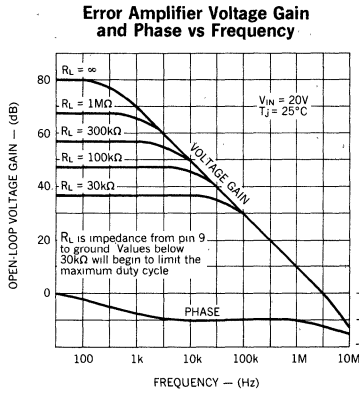
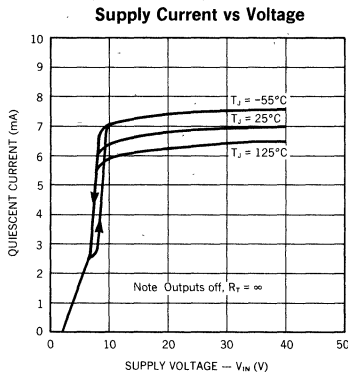
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1524A, -25°C to $+85^\circ\text{C}$ for the UC2524A, and 0°C to $+70^\circ\text{C}$ for the UC3524A; $V_{IN} = V_C = 20\text{V}$.)

PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	$T_J = 25^\circ\text{C}$, E/A Set for Maximum Output	190	200	210	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	μA
Common Mode Rejection Ratio	$V_{(\text{Pin } 5)} = -0.3\text{V}$ to $+5.5\text{V}$	50	60		50	60		dB
Power Supply Rejection Ratio	$V_{IN} = 10$ to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open-Loop Voltage Gain	$\Delta V_O = 1$ to 4V , $R_L \geq 10 \text{ Meg } \Omega$	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, $\Delta V_{IN} = 300\text{mV}$		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	$I_C = 100\mu\text{A}$	60	80		50	80		V
Collector Leakage Current	$V_{CE} = 50\text{V}$.1	20		.1	20	μA
Saturation Voltage	$I_C = 20\text{mA}$.2	.4		.2	.4	V
	$I_C = 200\text{mA}$		1	2.2		1	2.2	V
Emitter Output Voltage	$I_E = 50\text{mA}$	17	18		17	18		V
Rise Time*	$T_J = 25^\circ\text{C}$, $R = 2\text{K } \Omega$		200			200		ns
Fall Time*	$T_J = 25^\circ\text{C}$, $R = 2\text{K } \Omega$		100			100		ns
Comparator Delay*	$T_J = 25^\circ\text{C}$, Pin 9 to output		300			300		ns
Shutdown Delay*	$T_J = 25^\circ\text{C}$, Pin 10 to Output		200			200		ns
Shutdown Threshold	$T_J = 25^\circ\text{C}$, $R_C = 2\text{K } \Omega$	0.6	.7	1.0	0.6	.7	1.0	V
Thermal Shutdown*			165			165		$^\circ\text{C}$

* These parameters are guaranteed by design but not 100% tested in production.

OPEN-LOOP TEST CIRCUIT





LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulators

UC1525A UC1527A
UC2525A UC2527A
UC3525A UC3527A

3

FEATURES

- 8 to 35V operation
- 5.1V reference trimmed to $\pm 1\%$
- 100Hz to 500kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Pulse-by-pulse shutdown
- Input undervoltage lockout with hysteresis
- Latching PWM to prevent multiple pulses
- Dual source/sink output drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to $\pm 1\%$ and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (+V _{IN})	+40V
Collector Supply Voltage (V _C)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to +V _{IN}
Output Current, Source or Sink	500mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T _A = +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T _C = +25°C (Note 3)	2000mW
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

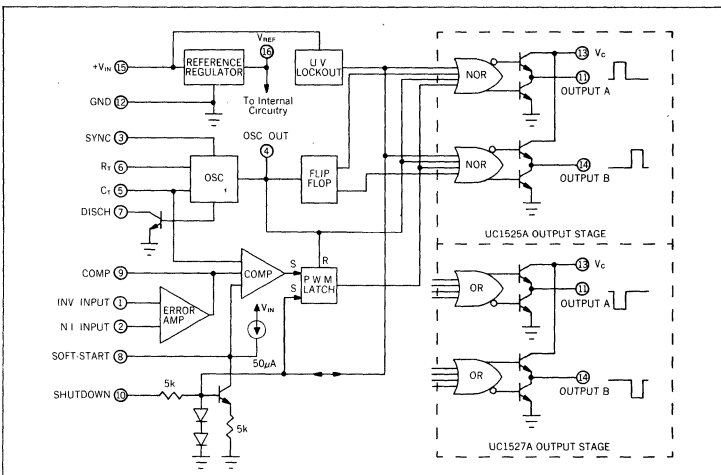
RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage (+V _{IN})	+8V to +35V
Collector Supply Voltage (V _C)	+4.5V to +35V
Sink/Source Load Current (steady state)	0 to 100mA
Sink/Source Load Current (peak)	0 to 400mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	100Hz to 400kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	.001μF to 0.1μF
Dead Time Resistor Range	0 to 500Ω
Operating Ambient Temperature Range	
UC1525A, UC1527A	-55°C to +125°C
UC2525A, UC2527A	-25°C to +85°C
UC3525A, UC3527A	0°C to +70°C

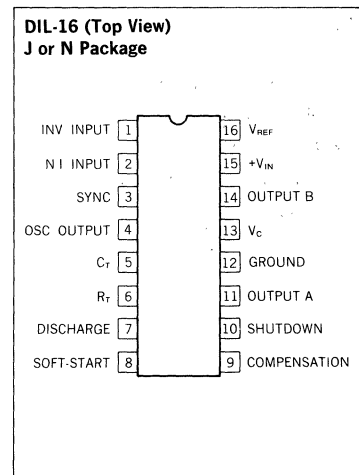
Notes: 4. Range over which the device is functional and parameter limits are guaranteed.

- Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 16mW/°C for case temperatures above +25°C.

BLOCK DIAGRAM



CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T _J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V _{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I _L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	mV
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V _{REF} = 0, T _J = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T _J = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T _J = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T _J = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 5 & 6)	V _{IN} = 8 to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 5)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	R _T = 200kΩ, C _T = 0.1μF			120			120	Hz
Maximum Frequency	R _T = 2kΩ, C _T = 470pF	400			400			kHz
Current Mirror	I _{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T _J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R _L ≥ 10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A _v = 0dB, T _J = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T _J = 25°C, 30kΩ ≤ R _L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V _{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V _{IN} = 8 to 35V	50	60		50	60		dB

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

6. Tested at f_{OSC} = 40kHz (R_T = 3.6kΩ, C_T = 0.1μF, R_D = 0Ω). Approximate oscillator frequency is defined by: $f = \frac{1}{C_T(0.7R_T + 3R_D)}$
7. DC transconductance (g_M) relates to DC open-loop voltage gain (A_v) according to the following equation: A_v = g_MR_L where R_L is the resistance from pin 9 to ground.
 The minimum g_M specification is used to calculate minimum A_v when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

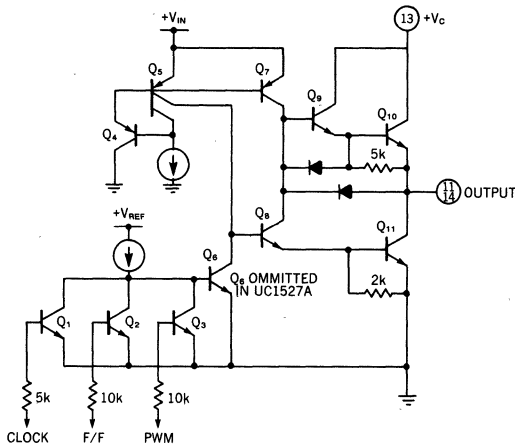
PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 6)	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	μA
Shutdown Section								
Soft Start Current	V _{SD} = 0V, V _{SS} = 0V	25	50	80	25	50	80	μA
Soft Start Low Level	V _{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V _{SS} = 5.1V, T _J = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V _{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V _{SD} = 2.5V, T _J = 25°C		0.2	0.5		0.2	0.5	μS
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I _{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I _{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I _{SOURCE} = 20mA	18	19		18	19		V
	I _{SOURCE} = 100mA	17	18		17	18		V
Under-Voltage Lockout	V _{COMP} and V _{SS} = High	6	7	8	6	7	8	V
Collector Leakage	V _C = 35V			200			200	μA
Rise Time (Note 5)	C _L = 1nF, T _J = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C _L = 1nF, T _J = 25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	V _{IN} = 35V		14	20		14	20	mA

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
 6. Tested at f_{OSC} = 40KHz (R_T = 3.6kΩ, C_T = 0.1μF, R_D = 0Ω).

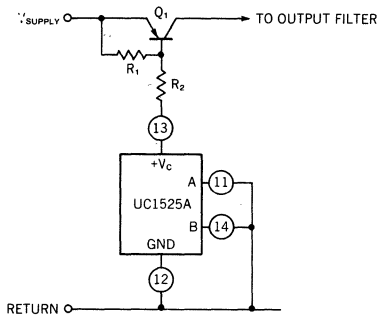
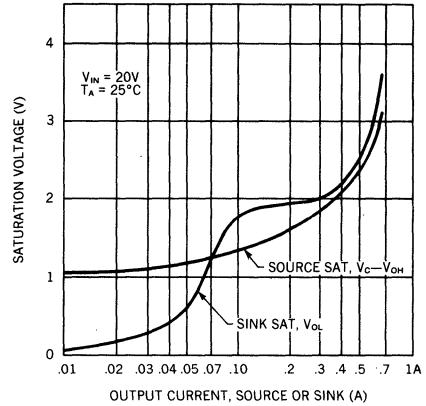
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A UC1527A
UC2525A UC2527A
UC3525A UC3527A

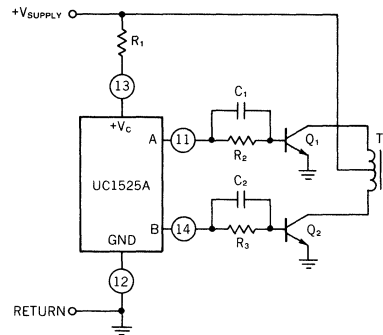
UC1525A Output Circuit
(1/2 Circuit Shown)



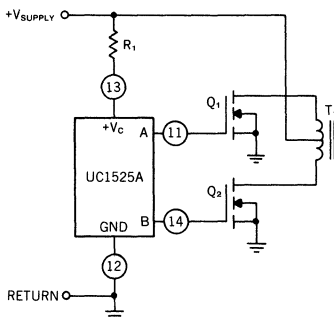
UC1525A Output Saturation Characteristics



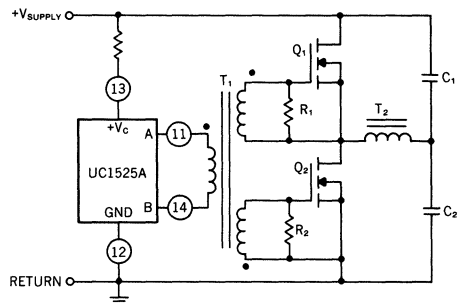
For single-ended supplies, the driver outputs are grounded. The V_c terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R₁-R₃. Rapid turn-off times for the power devices are achieved with speed-up capacitors C₁ and C₂.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

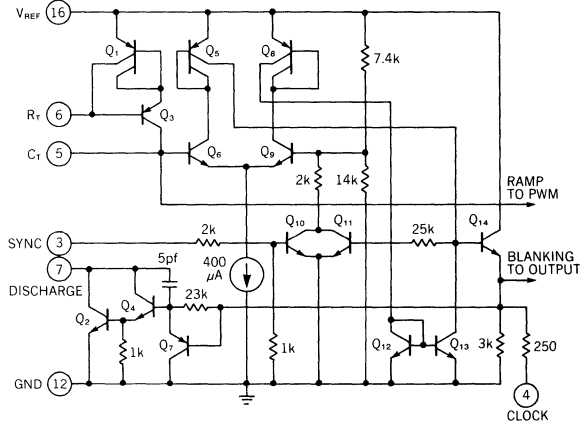
SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μ A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

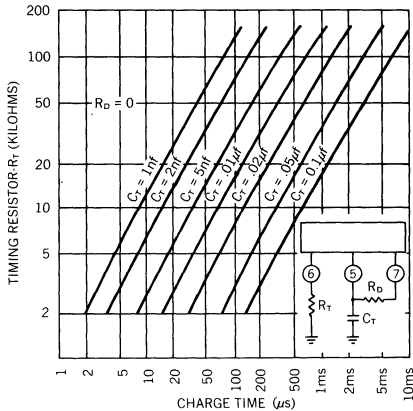
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μ A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

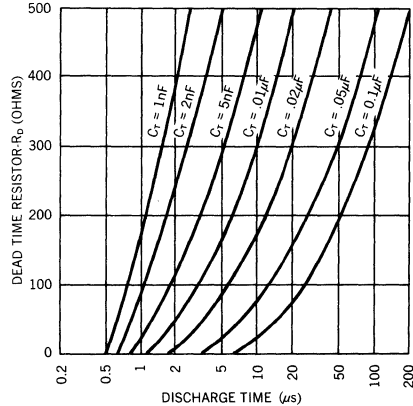
UC1525A Oscillator Schematic



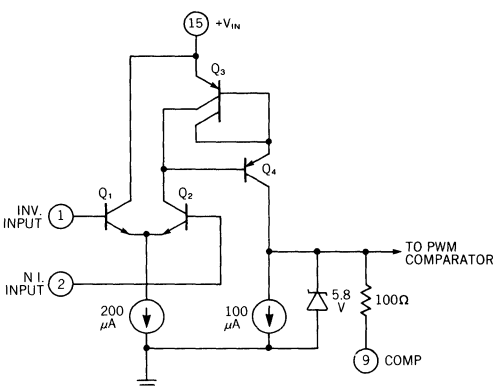
Oscillator Charge Time vs. R_r and C_T



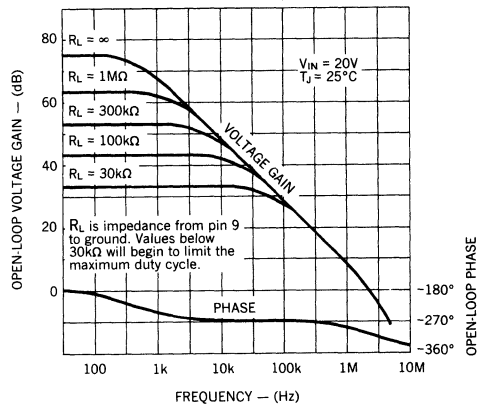
Oscillator Discharge Time vs. R_0 and C_T



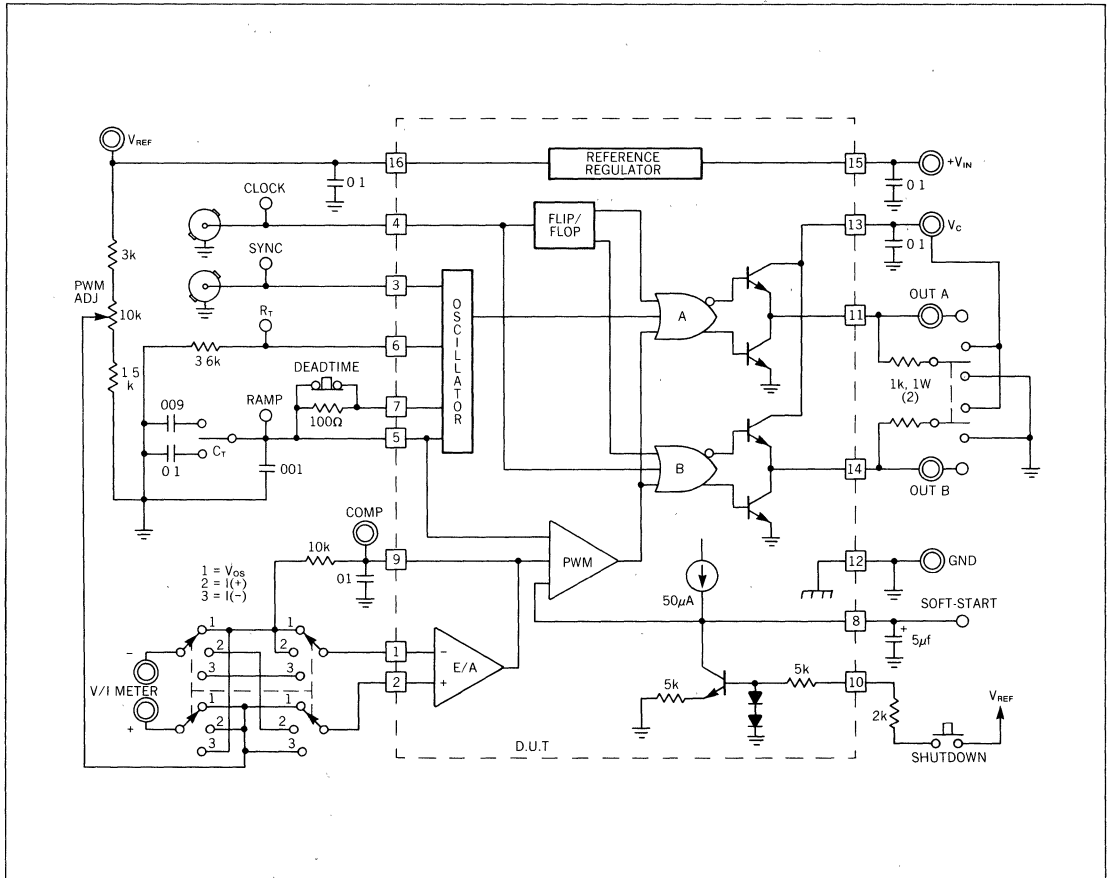
UC1525A Error Amplifier



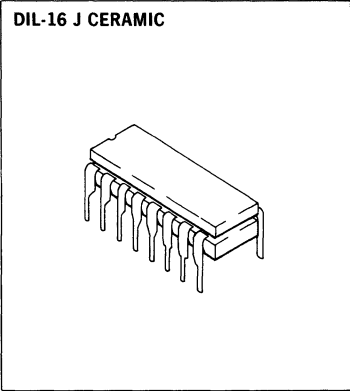
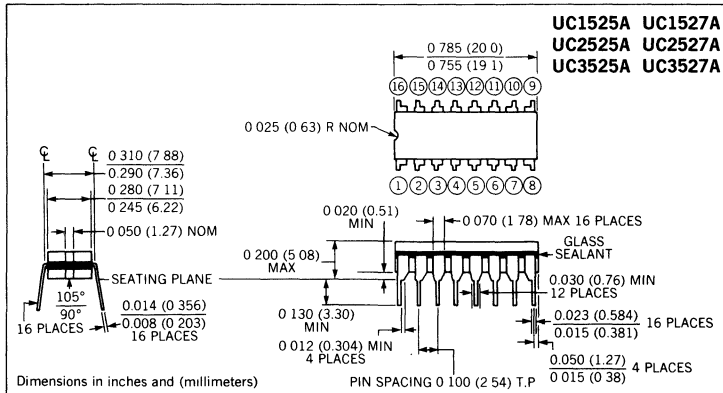
Error Amplifier Voltage Gain and Phase vs Frequency



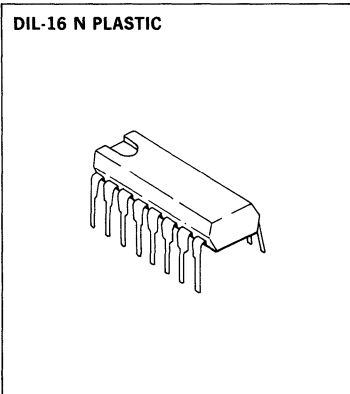
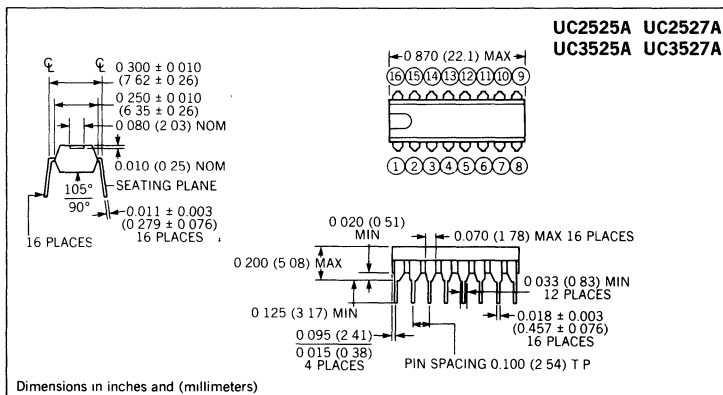
LAB TEST FIXTURE



MECHANICAL SPECIFICATIONS



3



Note: When ordering, add suffix "J" (for 16 pin ceramic package) or "N" (for 16 pin plastic package) to the part number.

LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulator

UC1526
UC2526
UC3526

FEATURES

- 8 to 35V operation
- 5V reference trimmed to $\pm 1\%$
- 1Hz to 400kHz oscillator range
- Dual 100mA source/sink outputs
- Digital current limiting
- Double pulse suppression
- Programmable deadtime
- Under-voltage lockout
- Single pulse metering
- Programmable soft-start
- Wide current limit common mode range
- TTL/CMOS compatible logic ports
- Symmetry correction capability
- Guaranteed 6 unit synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. The UC2526 is characterized for operation from -25°C to $+85^{\circ}\text{C}$, and the UC3526 is characterized for operation from 0°C to $+70^{\circ}\text{C}$.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (+V _{IN})	+40V
Collector Supply Voltage (+V _C)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to +V _{IN}
Source/Sink Load Current (each output)	200mA
Reference Load Current	50mA
Logic Sink Current	15mA
Power Dissipation at T _A = +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T _C = +25°C (Note 3)	3000mW
Thermal Resistance, Junction to Case	42°C/W
Operating Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

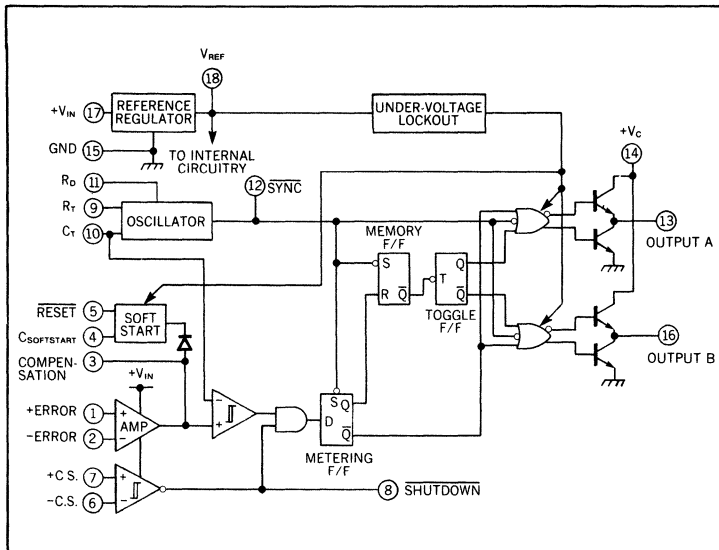
- Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 24mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

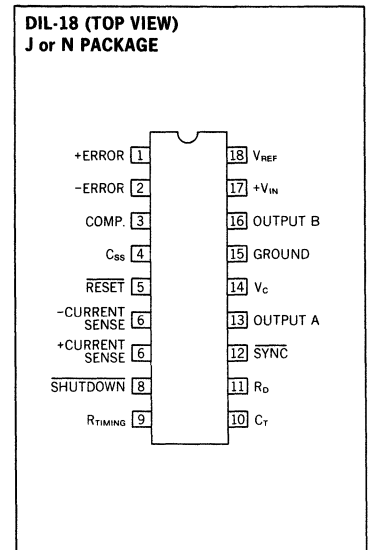
Input Voltage	+8V to +35V
Collector Supply Voltage	+4.5V to +35V
Sink/Source Load Current (each output)	0 to 100mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	1Hz to 400kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	1nF to 20μF
Available Deadtime Range at 40kHz	3% to 50%
Operating Ambient Temperature Range	
UC1526	-55°C to +125°C
UC2526	-25°C to +85°C
UC3526	0°C to +70°C

Note: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified)

3

PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section (Note 5)								
Output Voltage	T _J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V _{IN} = 8 to 35V		10	20		10	30	mV
Load Regulation	I _L = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating T _J		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V _{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
RESET Output Voltage	V _{REF} = 3.8V		0.2	0.4		0.2	0.4	V
RESET Output Voltage	V _{REF} = 4.8V	2.4	4.8		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T _J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V _{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T _J		7	10		3	5	%
Minimum Frequency	R _T = 150kΩ, C _T = 0.2mF			100			100	Hz
Maximum Frequency	R _T = 2kΩ, C _T = 470pF	400			400			kHz
Sawtooth Peak Voltage	+V _{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V _{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 7)								
Input Offset Voltage	R _S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R _L ≥ 10 Meg Ω	64	72		60	72		dB
HIGH Output Voltage	V _{pin1} -V _{pin2} ≥ 150mV, I _{source} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V _{pin2} -V _{pin1} ≥ 150mV, I _{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R _S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V _{IN} = 1.2 to 18V	66	80		66	80		dB
P.W.M. Comparator (Note 6)								
Minimum Duty Cycle	V _{compensation} = +0.4V			0			0	%
Maximum Duty Cycle	V _{compensation} = +3.6V	45	49		45	49		%
Digital Ports (SYNC, SHUTDOWN, and RESET)								
HIGH Output Voltage	I _{source} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I _{sink} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V _{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V _{IL} = +0.4V		-225	-360		-225	-360	μA

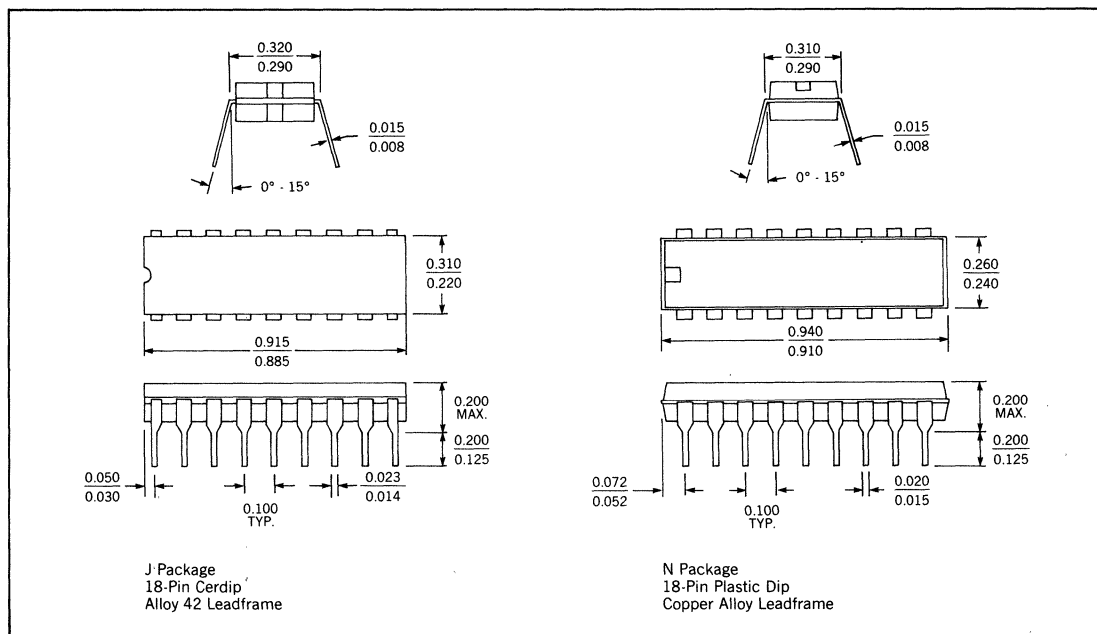
Notes: 5. I_L = 0mA.
6. F_{osc} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01μF ± 1%, R_D = 0Ω)
7. V_{CM} = 0 to +5.2V

ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified)

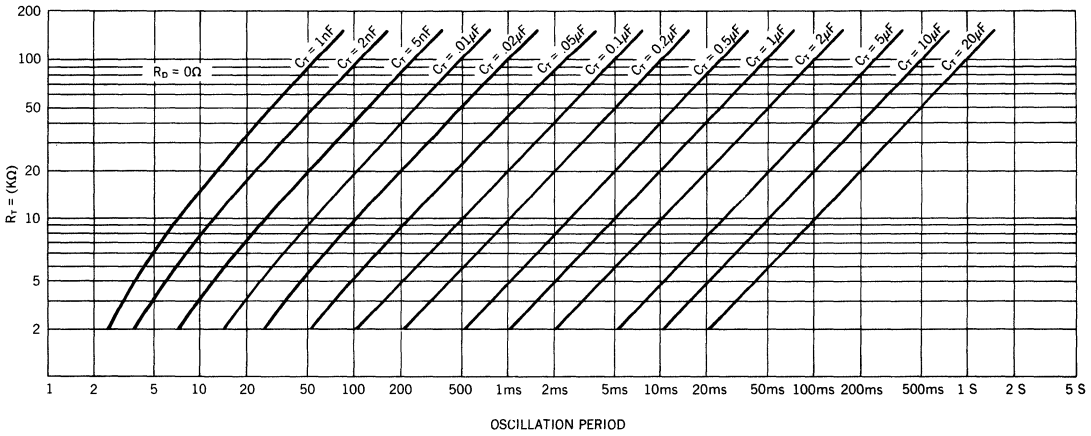
PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Comparator (Note 8)								
Sense Voltage	R _S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Soft-Start Section								
Error Clamp Voltage	RESET = +0.4V		0.1	0.4		0.1	0.4	V
C _S Charging Current	RESET = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I _{source} = 20mA	12.5	13.5		12.5	13.5		V
	I _{source} = 100mA	12	13		12	13		V
LOW Output Voltage	I _{sink} = 20mA		0.2	0.3		0.2	0.3	V
	I _{sink} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V _C = 40V		50	150		50	150	μA
Rise Time	C _L = 1000pF		0.3	0.6		0.3	0.6	μs
Fall Time	C _L = 1000pF		0.1	0.2		0.1	0.2	μs
Power Consumption (Note 10)								
Standby Current	SHUTDOWN = +0.4V		18	25		18	25	mA

- Notes: 8. V_{CM} = 0 to +12V
 9. V_C = +15V
 10. +V_{IN} = +35V, R_T = 4.12kΩ

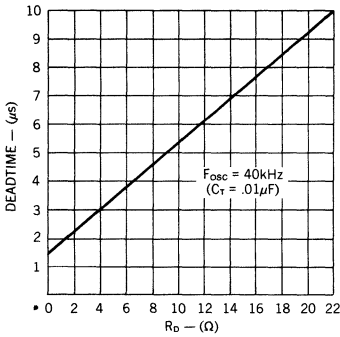
PACKAGE DIMENSIONS



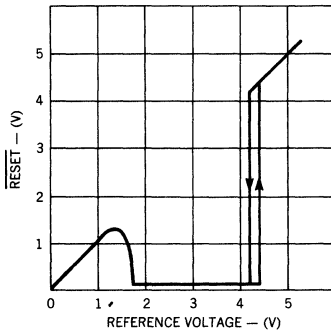
Oscillator Period vs R_T and C_T



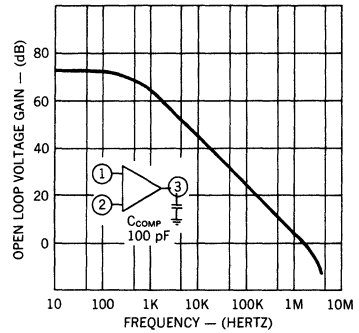
Output Driver Deadtime vs R_o Value



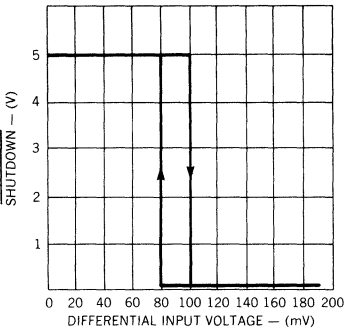
Under-Voltage Lockout Characteristic



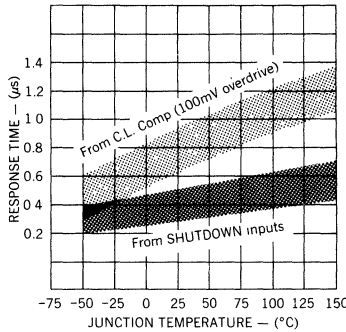
Error Amplifier Open Loop Gain vs Frequency



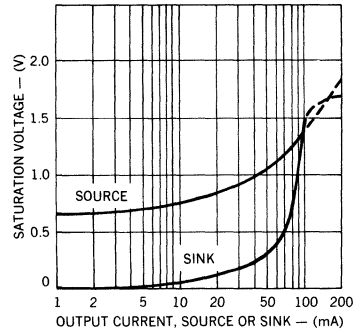
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

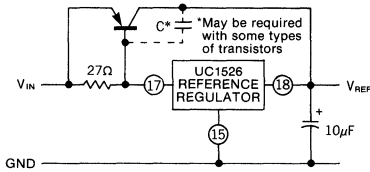


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage. If V_{IN} is too low, the circuit disables the output drivers and holds the RESET pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the RESET pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls RESET LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2V.

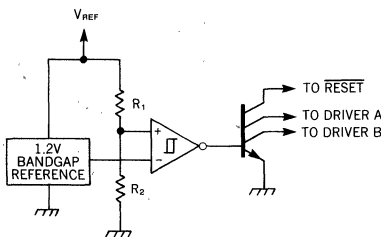


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds RESET LOW with Q_3 . Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, RESET will go HIGH. Q_1 turns off, allowing the internal 100μA current source to charge C_s . Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_s . As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

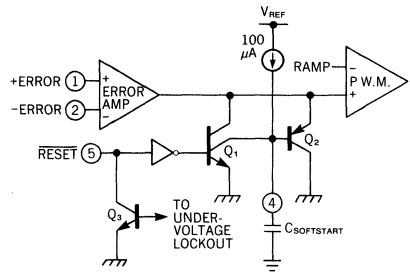


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding RESET LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

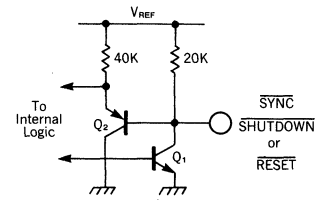


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T , C_T and R_D . Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D . At 40kHz dead time increases by 400ns/ Ω .
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5 μ s wide at the SYNC pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all SYNC terminals are likewise connected to the SYNC pin of the master. Slave R_T terminals are left open or connected to V_{REF} . Slave R_D terminals may be either left open or grounded.

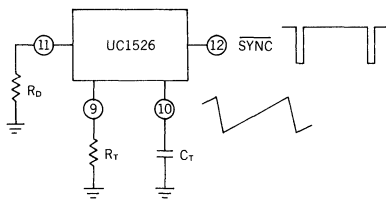


Figure 5. Oscillator Connections and Waveforms

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2M Ω . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 400Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

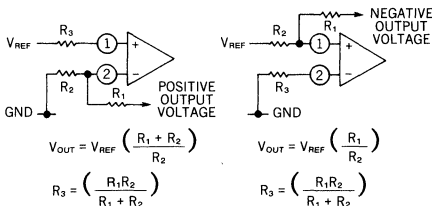


Figure 6. Error Amplifier Connections

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

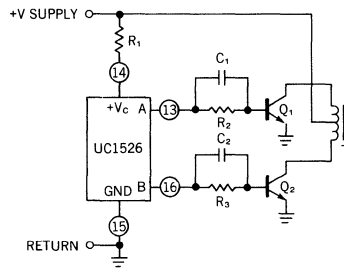


Figure 7. Push-Pull Configuration

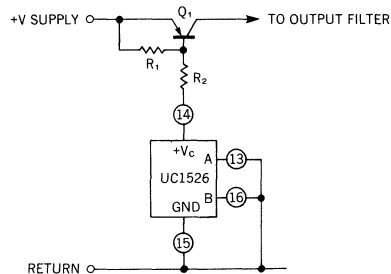


Figure 8. Single-Ended Configuration

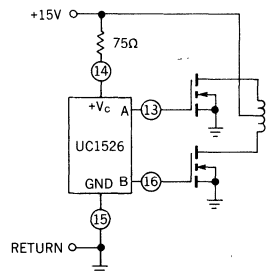


Figure 9. Driving N-Channel Power Mosfets

LINEAR INTEGRATED CIRCUITS

Power Supply Supervisory Circuit

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

FEATURES

- Includes over-voltage, under-voltage, and current sensing circuits
- Internal 1% accurate reference
- Programmable time delays
- SCR "crowbar" drive of 300mA
- Remote activation capability
- Optional over-voltage latch
- Uncommitted comparator inputs for low voltage sensing (UC1544 series only)

DESCRIPTION

These monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage.

The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

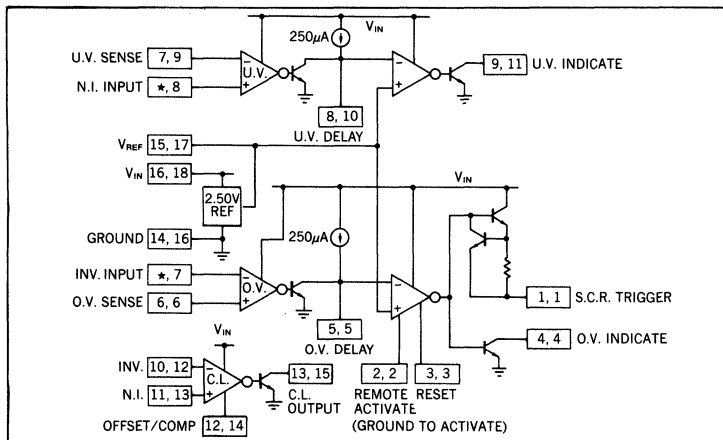
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs, Voltage Range	0 to V_{IN}
SCR Trigger Current	-600mA*
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA
Power Dissipation (Package Limitation)	1000mW
Derate Above 25°C	8.0mW/°C
Operating Temperature Range	
UC1543, UC1544	-55°C to +125°C
UC2543, UC2544	-25°C to +85°C
UC3543, UC3544	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

*At higher input voltages, a dissipation limiting resistor, R_{th} , is required.

Note: Currents are positive-into, negative-out of the specified terminal.

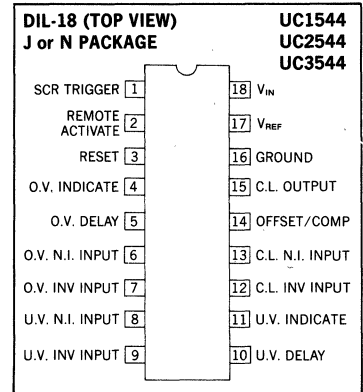
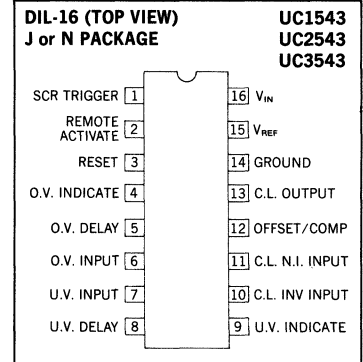
BLOCK DIAGRAM



Note: For each terminal, first number refers to 1543 series, second to 1544 series.

★ On 1543 series, this function is internally connected to V_{REF} .

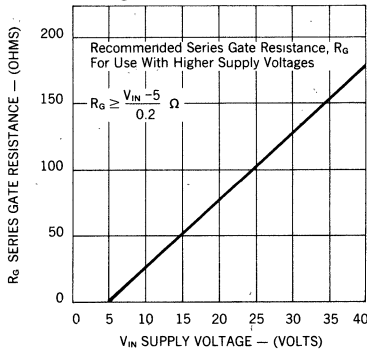
CONNECTION DIAGRAMS



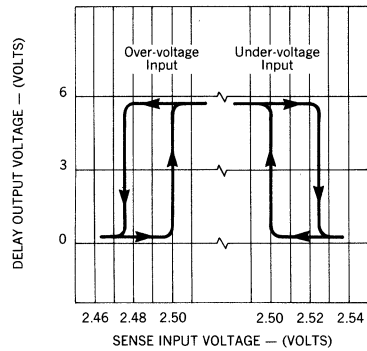
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1543 & UC1544; -25°C to $+85^{\circ}\text{C}$ for the UC2543 & UC2544; and 0°C to $+70^{\circ}\text{C}$ for the UC3543 & UC3544; and for $V_{IN} = 5$ to 35V . Electrical tests are performed with $V_{IN} = 10\text{V}$ and $2\text{k}\Omega$ pull-up resistors on all indicator outputs. All electrical ratings and specifications for the UC1544, UC2544 & UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference.)

PARAMETER	TEST CONDITIONS	UC1543/UC2543 UC1544/UC2544			UC3543 UC3544			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Voltage Range	$T_J = 25^{\circ}\text{C}$ to T_{MAX}	4.5		40	4.5		40	V
Input Voltage Range	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	$V_{IN} = 40\text{V}$, Outputs Open		7	10		7	10	mA
Reference Section								
Output Voltage	$T_J = 25^{\circ}\text{C}$	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	$V_{IN} = 5$ to 30V		1	5		1	5	mV
Load Regulation	$I_{REF} = 0$ to 10mA		1	10		1	10	mV
Short Circuit Current	$V_{REF} = 0$	-12	-20	-40	-12	-20	-40	mA
Temperature Stability			50			50		ppm/ $^{\circ}\text{C}$
SCR Trigger Section								
Peak Output Current	$V_{IN} = 5\text{V}$, $R_{\theta} = 0$, $V_{O} = 0$	-100	-300	-600	-100	-300	-600	mA
Peak Output Voltage	$V_{IN} = 15\text{V}$, $I_{O} = -100\text{mA}$	12	13		12	13		V
Output Off Voltage	$V_{IN} = 40\text{V}$		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Reset Voltage	Reset Open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time			400			400		mA/ μs
Prop. Delay from R/A	$R_L = 50\Omega$, $T_J = 25^{\circ}\text{C}$, $C_D = 0$		300			300		ns
Prop. Delay from O/V input			500			500		ns
Comparator Sections								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	$T_J = 25^{\circ}\text{C}$	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		-0.3	-1.0		-0.3	-1.0	μA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	$V_D = 0$	-200	-250	-300	-200	-250	-300	μA
Indicate Saturation	$I_L = 10\text{mA}$		0.2	0.5		0.2	0.5	V
Indicate Leakage	$V_{IND} = 40\text{V}$.01	1.0		.01	1.0	μA
Propagation Delay	Input Overdrive = 200mV $T_J = 25^{\circ}\text{C}$	$C_D = 0$		400			400	ns
		$C_D = 1\mu\text{F}$		10			10	ms
Current Limit Section								
Input Voltage Range		0		($V_{IN}-3\text{V}$)	0		($V_{IN}-3\text{V}$)	V
Input Bias Current	Offset Pin Open, $V_{CM} = 0$		-0.3	-1.0		-0.3	-1.0	μA
Input Offset Voltage	Offset Pin Open, $V_{CM} = 0$		0	10		0	10	mV
Input Offset Voltage	10k Ω from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	$0 \leq V_{CM} \leq 12\text{V}$, $V_{IN} = 15\text{V}$	60	70		60	70		dB
AVOL	Offset Pin Open, $V_{CM} = 0\text{V}$	72	80		72	80		dB
Output Saturation	$I_L = 10\text{mA}$		0.2	0.5		0.2	0.5	V
Output Leakage	$V_{IND} = 40\text{V}$.01	1.0		.01	1.0	μA
Small Signal Bandwidth	$A_v = 0\text{dB}$, $T_J = 25^{\circ}\text{C}$		5			5		MHz
Propagation Delay	$V_{overdrive} = 100\text{mV}$, $T_J = 25^{\circ}\text{C}$		200			200		ns

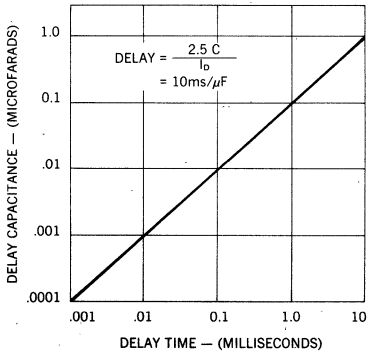
SCR Trigger Power Limiting



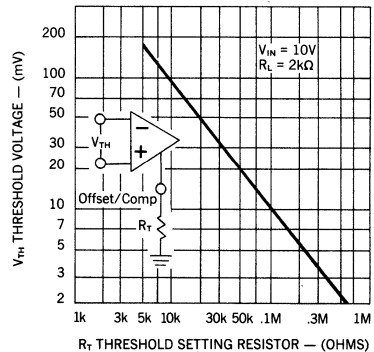
Comparator Input Hysteresis



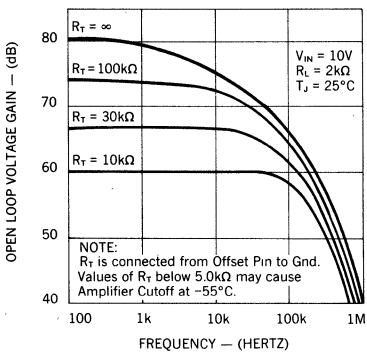
Activation Delay vs Capacitor Value



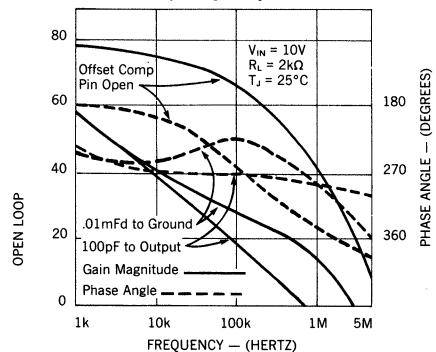
Current Limit Input Threshold



Current Limit Amplifier Gain



Current Limit Amplifier Frequency Response



APPLICATIONS (Pin Numbers given for UC1543 series devices)

Typical Application

The values for the external components are determined as follows:

Current limit input threshold, $V_m \approx \frac{1000}{R_1}$

C_s is determined by the current loop dynamics

Peak current to load, $I_p \approx \frac{V_m}{R_{sc}} + \frac{V_o}{R_{sc}} \left(\frac{R_2}{R_2 + R_3} \right)$

Short circuit current, $I_{sc} = \frac{V_m}{R_{sc}}$

Low output voltage limit, $V_o(\text{Low}) = \frac{2.5(R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit, $V_o(\text{High}) = \frac{2.5(R_4 + R_5 + R_6)}{R_6}$

Voltage sensing delay, $t_d = 10,000 \text{ Cd}$

SCR trigger power limiting resistor, $R_a > \frac{V_{in} - 5}{0.2}$

Sensing Multiple Supply Voltages

BIAS SUPPLY ← TO SG139 COMPARATORS

MAIN POSITIVE SUPPLY

GROUND

ADDITIONAL POSITIVE SUPPLY

NEGATIVE SUPPLY VOLTAGE

TO SHUTDOWN CIRCUIT

MASTER POWER SUPPLY CONDITION INDICATOR

Input Line Monitor

LINE INPUT

2.5V REF.

UC1543

U.V.

C.L.

PIN 7 INPUT

PIN 8 DELAY

PIN 9 OUTPUT

OFF ON

Overcurrent Shutdown

MAIN SUPPLY BUS

BIAS VOLTAGE

UC1543

2.5V REF.

C.L.

SCR TRIGGER

SCR "CROWBAR"

SUPPLY BUS RETURN

LINEAR INTEGRATED CIRCUITS

Switched Mode Controller for DC Motor Drive

UC1637
UC2637
UC3637

FEATURES

- Single or dual supply operation
- $\pm 2.5V$ to $\pm 20V$ input supply range
- $\pm 5\%$ initial oscillator accuracy; $\pm 10\%$ over temperature
- Pulse-by-pulse current limiting
- Under-voltage lockout
- Shutdown input with temperature compensated 2.5V threshold
- Uncommitted PWM comparators for design flexibility
- Dual 100mA, source/sink output drivers

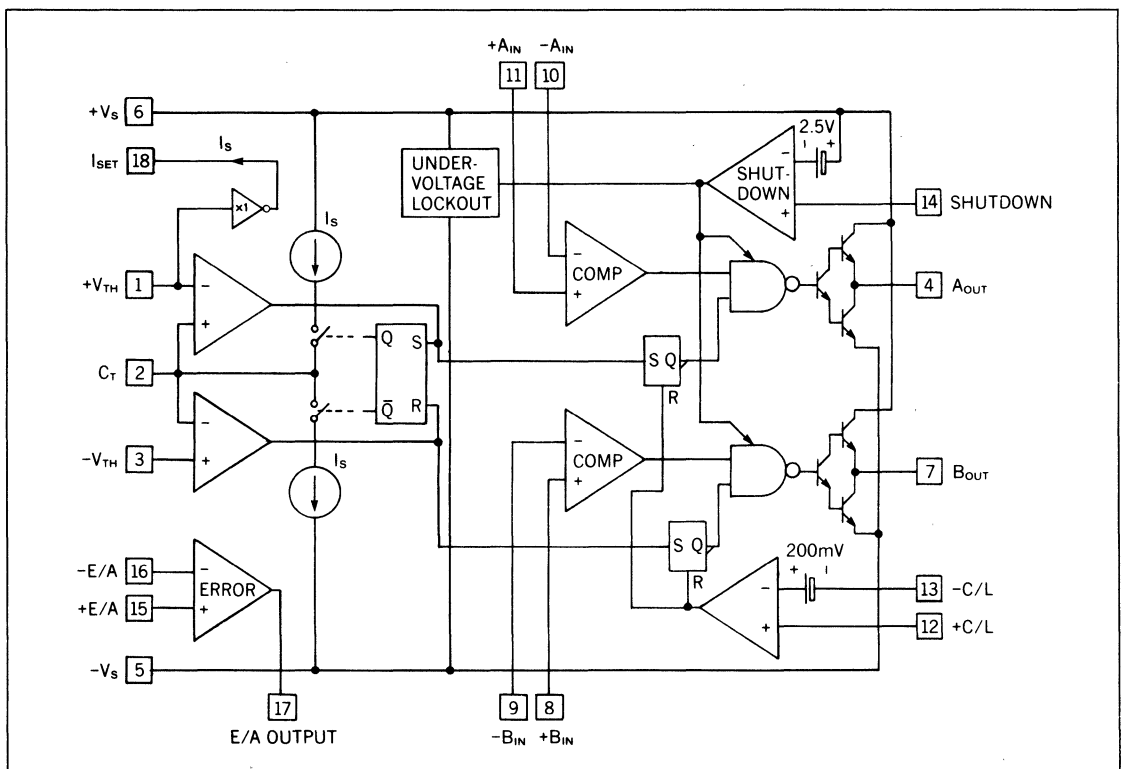
DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with $\pm 100mA$ output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

The UC1637 is characterized for operation over the full military temperature range of $-55^{\circ}C$ to $+125^{\circ}C$, while the UC2637 and UC3637 are characterized for $-25^{\circ}C$ to $+85^{\circ}C$ and $0^{\circ}C$ to $+70^{\circ}C$, respectively.

BLOCK DIAGRAM

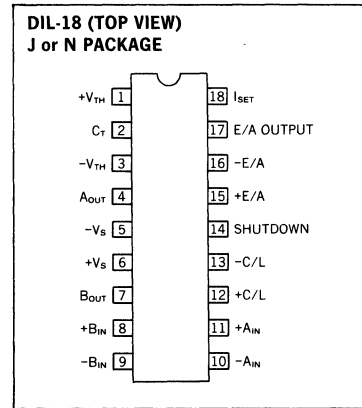


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($\pm V_S$)	$\pm 20V$
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15, 16)	$\pm V_S$
Error Amplifier Output Current (Pin 17)	$\pm 20mA$
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at $T_A = 25^\circ C$	1000mW
Derate at 10mW/ $^\circ C$ For T_A Above 50 $^\circ C$	
Power Dissipation at $T_C = 25^\circ C$	2000W
Derate at 16mW/ $^\circ C$ for T_C above 25 $^\circ C$	
Thermal Resistance, Junction to Ambient	100 $^\circ C/W$
Thermal Resistance, Junction to Case	60 $^\circ C/W$
Storage Temperature Range	-65 $^\circ C$ to +150 $^\circ C$
Lead Temperature (Soldering, 10 Seconds)	+300 $^\circ C$

Note: 1. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM



3

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ C$ to +125 $^\circ C$ for UC1637; -25 $^\circ C$ to +85 $^\circ C$ for the UC2637; and 0 $^\circ C$ to +70 $^\circ C$ for the UC3637; $+V_S = +15V$, $-V_S = -15V$, $+V_{TH} = 5V$, $-V_{TH} = -5V$, $R_T = 16.7k\Omega$, $C_T = 1500pF$)

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator								
Initial Accuracy	$T_j = 25^\circ C$	9.4	10	10.6	9	10	11	kHz
Voltage Stability	$V_S = \pm 5V$ to $\pm 20V$, $V_{PIN 1} = 3V$ $V_{PIN 3} = -3V$		5	7		5	7	%
Temperature Stability	Over Operating Range		0.5	2		0.5	2	%
+ V_{TH} Input Bias Current	$V_{PIN 2} = 6V$	-10	0.1	10	-10	0.1	10	μA
- V_{TH} Input Bias Current	$V_{PIN 2} = 0V$	-10	-0.5		-10	-0.5		μA
+ V_{TH} , - V_{TH} Input Range		+ V_S-2		- V_S+2	+ V_S-2		- V_S+2	V
Error Amplifier								
Input Offset Voltage	$V_{CM} = 0V$		1.5	5		1.5	10	mV
Input Bias Current	$V_{CM} = 0V$		0.5	5		0.5	5	μA
Input Offset Current	$V_{CM} = 0V$		0.1	1		0.1	1	μA
Common Mode Range	$V_S = \pm 2.5$ to 20V	- V_S+2		+ V_S	- V_S+2		+ V_S	V
Open Loop Voltage Gain	$R_L = 10K$	75	100		80	100		dB
Slew Rate			15			15		V/ μs
Unity Gain Bandwidth								
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	$V_S = \pm 2.5V$ to $\pm 20V$	75	110		75	110		dB
Output Sink Current	$V_{PIN 17} = 0V$		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN 17} = 0V$		5	11		5	11	mA
High Level Output Voltage			13	13.6		13	13.6	V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	$V_{CM} = 0V$		20			20		mV
Input Bias Current	$V_{CM} = 0V$		2	10		2	10	μA
Input Hysteresis	$V_{CM} = 0V$		10			10		mV
Common Mode Range	$V_S = \pm 5$ to $\pm 40V$	- V_S+1		+ V_S-2	- V_S+1		+ V_S-2	V

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for UC1637; -25°C to $+85^\circ\text{C}$ for the UC2637; and 0°C to $+70^\circ\text{C}$ for the UC3637; $+V_S = +15\text{V}$, $-V_S = -15\text{V}$, $+V_{TH} = 5\text{V}$, $-V_{TH} = -5\text{V}$, $R_T = 16.7\text{k}\Omega$, $C_T = 1500\text{pF}$)

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit								
Input Offset Voltage	$V_{CM} = 0\text{V}$, $T_j = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/ $^\circ\text{C}$
Input Bias Current		-10	-1.5		-10	-1.5		μA
Common Mode Range	$V_S = \pm 2.5\text{V}$ to $\pm 20\text{V}$	$-V_S$		$+V_S - 3$	$-V_S$		$+V_S - 3$	V
Shutdown								
Shutdown Threshold	(Note 3)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14} = +V_S$ to $-V_S$	-10	-0.5		-10	-0.5		μA
Under-Voltage Lockout								
Start Threshold	(Note 4)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	$I_{SINK} = 20\text{mA}$		-14.9	-13		-14.9	-13	V
	$I_{SINK} = 100\text{mA}$		-14.5	-13		-14.5	-13	
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 100\text{mA}$	12	13.5		12	13.5		
Rise Time	(Note 2) $C_L = 1\text{nf}$, $T_j = 25^\circ\text{C}$		100	600		100	600	ns
Fall Time	(Note 2) $C_L = 1\text{nf}$, $T_j = 25^\circ\text{C}$		100	300		100	300	ns

- Notes:**
2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
 3. Parameter measured with respect to $+V_S$ (Pin 6).
 4. Parameter measured at $+V_S$ (Pin 6) with respect to $-V_S$ (Pin 5).

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{set} , and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and

$-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{set} terminal to develop the capacitor charging current through R_T . If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

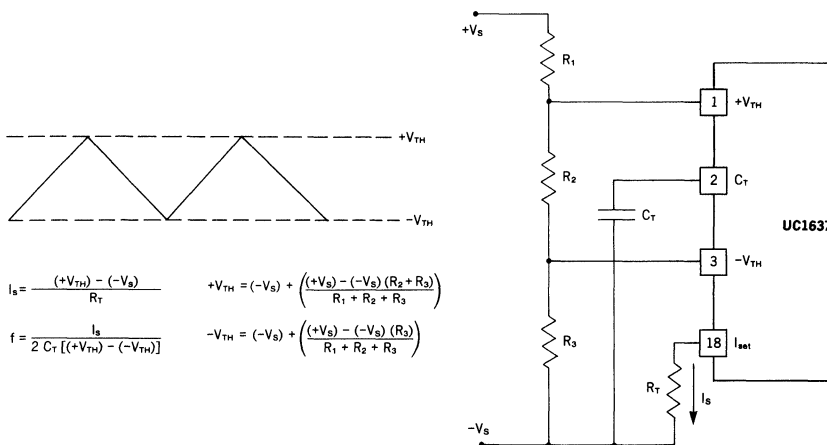


Figure 1. Oscillator Set Up

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high-state of output A and

shorten the high-state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the threshold set on Pin 10 and 8.

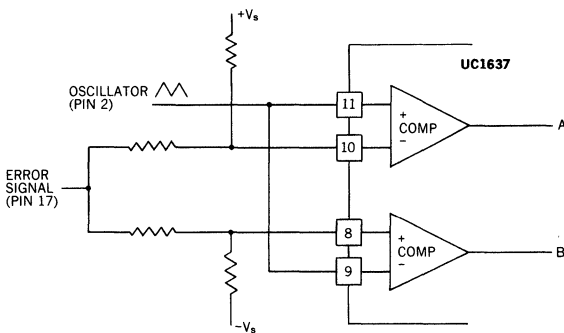


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 10 and Pin 8)

In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 10 > Pin 8)

A small differential voltage between Pin 10 and 8 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where

power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode (Voltage on Pin 10 > Pin 8)

With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

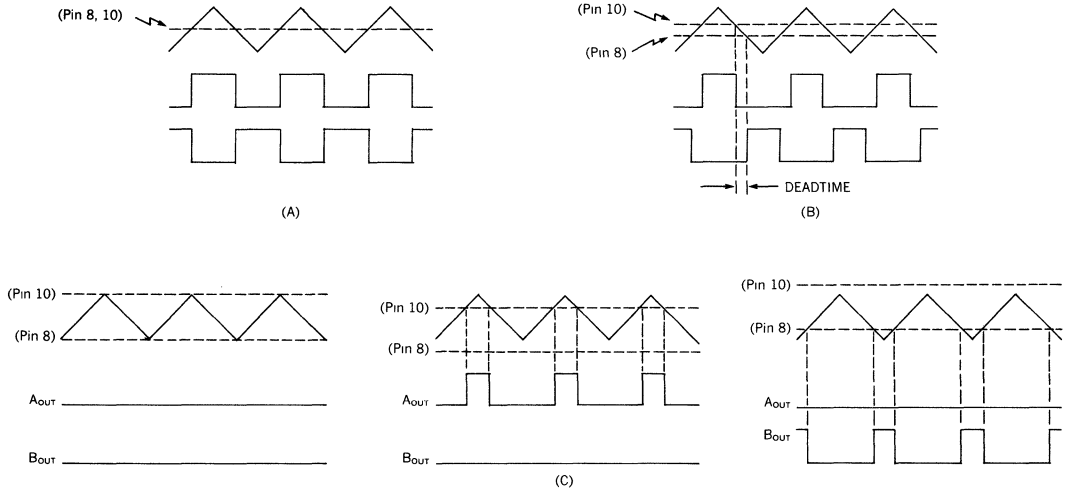


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations.

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_s + 0.2V$ @ 50mA low level and $+V_s - 2.0V$ @ 50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate ($15V/\mu s$) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the $\pm V_s$ supply voltage, the common mode input range and the voltage output swing is within 2V of the V_s supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the off state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are switched on. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

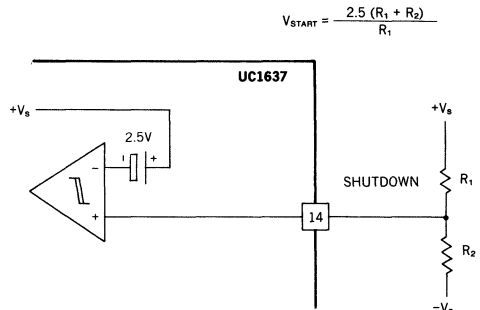


Figure 4. External Under-Voltage Lockout

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below V_{IN} , the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to

either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5.

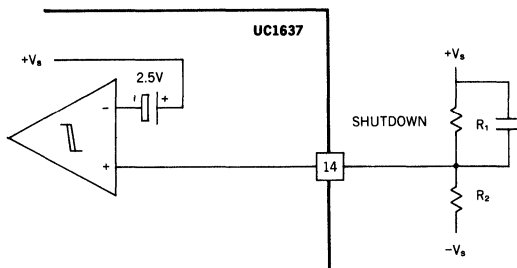


Figure 5. Delayed Start-Up

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from $-V_S$ to within 3V of

the $+V_S$ supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

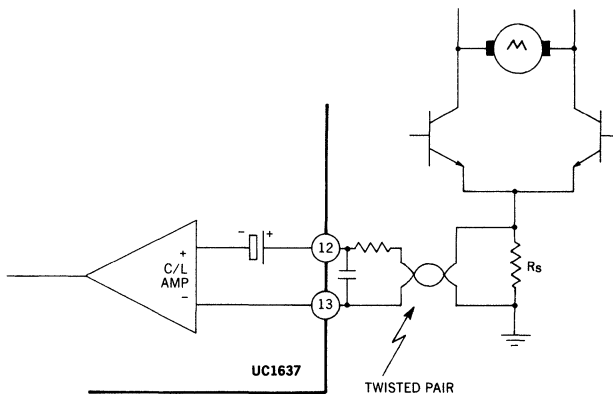


Figure 6. Current Limit Sensing

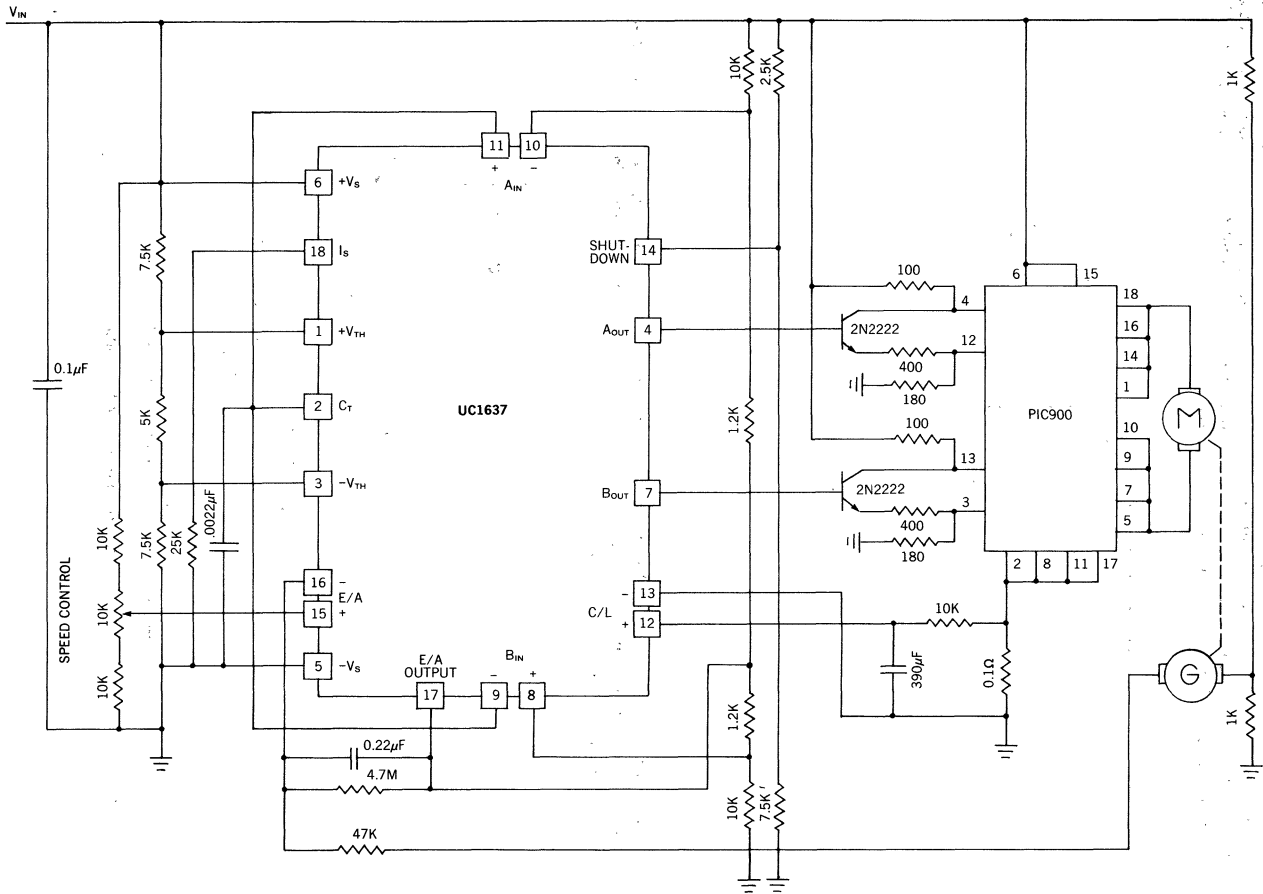


Figure 7. Bi-Directional Motor Drive with Speed Control and Power-Amplifier

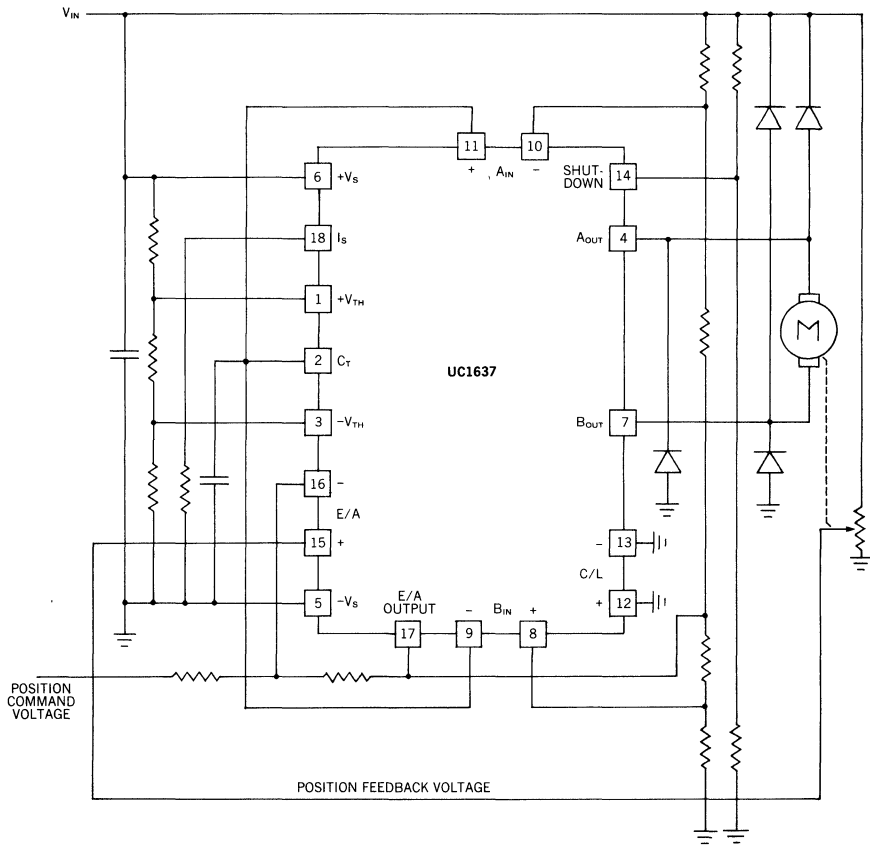


Figure 8. Single Supply Position Servo Motor Drive

LINEAR INTEGRATED CIRCUITS

Bridge Transducer Switch

UC1704
UC3704

UC1704 COMPATIBLE SENSORS

SENSOR TYPE	ACTIVATION SOURCE						
	Temperature	Pressure	Force	Position	Displacement	Velocity	Shock
Thermistor	X						X
Sensistor	X						X
Thermocouple	X						
Semiconductor	X	X	X				
Photo Voltaic				X	X	X	
Photo Resistive				X	X	X	
Strain Gage		X	X	X	X	X	X
Piezoelectric		X	X		X	X	X
Magneto Resistive				X	X		
Inductive				X	X	X	X
Hall Effect				X	X		
Capacitive							X

FEATURES

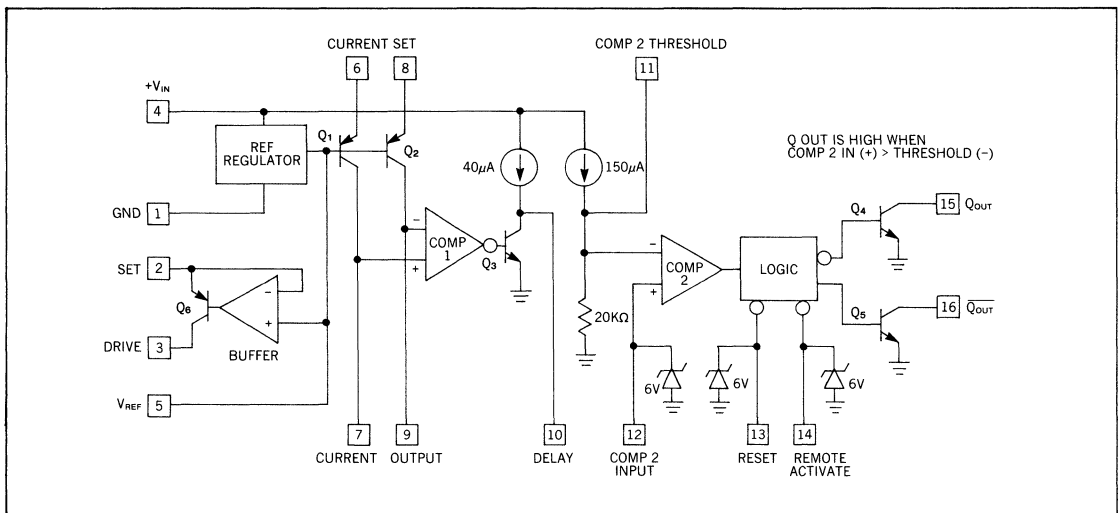
- Dual matched current sources
- High-gain differential sensing circuit
- Wide common-mode input capability
- Complimentary digital open-collector outputs
- Externally programmable time delay
- Optional output latch with reset
- Built-in diagnostic activation
- Wide supply voltage range
- High current heater power source driver

DESCRIPTION

This integrated circuit contains a complete signal conditioning system to interface low-level variable impedance transducers to a digital system. A pair of matched, temperature-compensated current sources are provided for balanced transducer excitation followed by a precision, high-gain comparator. The output of this comparator can be delayed by a user-selectable duration, after which a second comparator will switch complimentary outputs compatible with all forms of logic. This output section can be separately activated for diagnostic operation and has an optional latch with external reset capability. An added feature is a high current power source useful as a heater driver in differential temperature sensing applications.

The UC1704 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$ while the UC3704 is designed for 0°C to $+70^{\circ}\text{C}$ environments.

BLOCK DIAGRAM

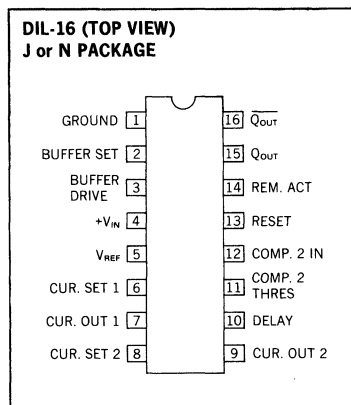


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V _{IN})	40V
Output Current (each output)	50mA
Buffer Power Source Current	200mA
Comparator 1 Inputs	-0.5V to V _{REF}
Comparator 2 Inputs	0 to 5.5V
Remote Activation and Reset Inputs	0 to 5.5V
Power Dissipation at T _A = 25°C	1000mW
Derate at 10mW/°C for T _A > 50°C	
Operating Junction Temperature	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

NOTE: Unless otherwise specified, all voltages are with respect to ground (Pin 1).
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM



3

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1704 and 0°C to +70°C for the UC3704; V_{IN} = 15V)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Inputs					
Supply Voltage Range	T _A > 0°C	4.2		36	V
Supply Current	V _{IN} = 36V		5	10	mA
Reference Section (with respect to V_{IN})					
V _{REF} Value V _{IN} - V _{REF}	T _J = 25°C	2.1	2.2	2.3	V
V _{REF} Temperature Coefficient	Note 1	-1	-2	-3	mV/°C
Line Regulation	ΔV _{IN} = 4.2 to 25V		2	10	mV
Load Regulation	ΔI _O = 0 to 4mA		2	10	mV
Short Circuit Current	V _{IN} = 36V V _{REF} = V _{IN} or Ground			±25	mA
Current Sources (Q₁ and Q₂)					
Output Current (Note 2)	Current Set = 10μA	-9	-9.5	-10	μA
	Current Set = 200μA	-180	-195	-200	μA
Output Offset Current	R _{EB} = R _{EB} = 20KΩ		0	±1	μA
Comparator One					
Input Offset Voltage			±1	±4	mV
Input Bias Current			-100	-300	nA
Input Offset Current				±60	nA
CMRR	V _{CM} = 0 to 12V	60	70		dB
Voltage Gain	R _L > 150KΩ	70	85		dB
Delay Current Source		34	40	52	μA
Output Rise Time	Overdrive = 10mV, C _D = 15pF, T _J = 25°C		2		V/μs

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1704 and 0°C to $+70^\circ\text{C}$ for the UC3704; $V_{IN} = 15\text{V}$)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Comparator Two (Q_{OUT} and \bar{Q}_{OUT})					
Threshold Voltage		2.2	3.0	3.8	V
Threshold Resistance	To Ground	14	20	24	$\text{K}\Omega$
Input Bias Current	V_{IN} (Pin 12) = 5V		1	3	μA
Remote Activate Current	Pin 14 = 0V		0.2	0.5	mA
Reset Current	Pin 13 = 0V		0.2	0.5	mA
Remote Activate Threshold	$T_A = 25^\circ\text{C}$	0.8	1.2		V
Reset Threshold	$T_A = 25^\circ\text{C}$	0.8	1.2		V
Output Saturation	$I_{OUT} = 16\text{mA}$		0.2	0.5	V
	$I_{OUT} = 50\text{mA}$		0.7	2.0	V
Output Leakage	$V_{OUT} = 40\text{V}$		0.2	10	μA
Output Response	Comp. Overdrive = 1V $R_L = 5\text{K}$ to V_{IN}	Turn-on	0.4		μs
		Turn-off	1.0		
Buffer					
Set Voltage ($V_{IN} - V_S$)	$T_J = 25^\circ\text{C}$, $I_S = 100\text{mA}$	1.9	2.1	2.3	V
Drive Current	$T_J = 25^\circ\text{C}$, $R_S = 200\Omega$, $V_D = 0\text{V}$	90	100	120	mA

Note: 1. Parameter guaranteed by design, not tested in production.

2. Collector output current =
$$\frac{V_{IN} - V_{REF} - V_{BE}}{R_E} \approx \frac{1.5\text{V}}{R_E}$$

APPLICATIONS INFORMATION

Sensor Section

The input portion of the UC1704 provides both excitation and sensing for a low-level, variable impedance transducer. This circuitry consists of a pair of highly matched PNP transistors biased for operation as constant current sources followed by a high gain precision comparator.

The reference voltage at the bases of the PNP transistors has a TC to offset the base-emitter voltage variation of these transistors resulting in a constant voltage across the external emitter resistors and correspondingly constant collector currents. With the emitter resistors external, the user has the option of tailoring the collector currents for balancing, offsetting, or to provide a unique temperature characteristic.

With the PNP transistors' optimum current ranging from 10 to $200\mu\text{A}$, and the common-mode input voltage of the comparator usable from ground to $(V_{IN} - 3\text{V})$, a wide range of transducer impedance levels is possible.

The sensor comparator has a current source pull-up at the output so that an external capacitor from this point to ground can be used to provide a programmable delay before reaching the second comparator's threshold. The low-impedance on-state of Comp 1's output provides quick reset of this capacitor. This programmable delay function is useful for providing transient protection by requiring that Comp 1 remain activated for a finite period of time before Comp 2 triggers. Another application is in counting repetitive pulses where a missing pulse will allow Comp 1's output to rise to Comp 2's threshold. This time delay function is:

$$\text{Delay} = \frac{\text{Comp 2 Threshold}}{\text{Delay Current}} \times C_D \approx 175 \text{ ms}/\mu\text{F}$$

If hysteresis is desired for Comparator 1, it may be accommodated by applying positive feedback from the delay terminal to the non-inverting input on Pin 7. This will aid in providing oscillation-free transitions for very slowly changing inputs.

Output Section

The output portion of the UC1704 is basically a second comparator with complimentary, open-collector outputs. This comparator has a built-in, ground-referenced threshold implemented with a high-impedance current source and resistor so that it may be easily overridden with an external voltage source if desired. Comp 2's input transistors are NPN types which require at least 1V of common-mode voltage for accurate operation and should not see a differential input voltage greater than 6V.

For diagnostic or latching purposes, the output logic is equipped with a Remote Activate and Reset function. These pins have internal pull-ups and are only active when pulled low below a threshold of approximately 1V. A low signal at the Remote Activate Pin causes the outputs to change state in exactly the same manner as if Comp 2's input is raised above the threshold on Pin 11. If Pin 16 is connected to Pin 14, positive feedback results and the outputs will latch once triggered by Comp 2's input. Pulling the

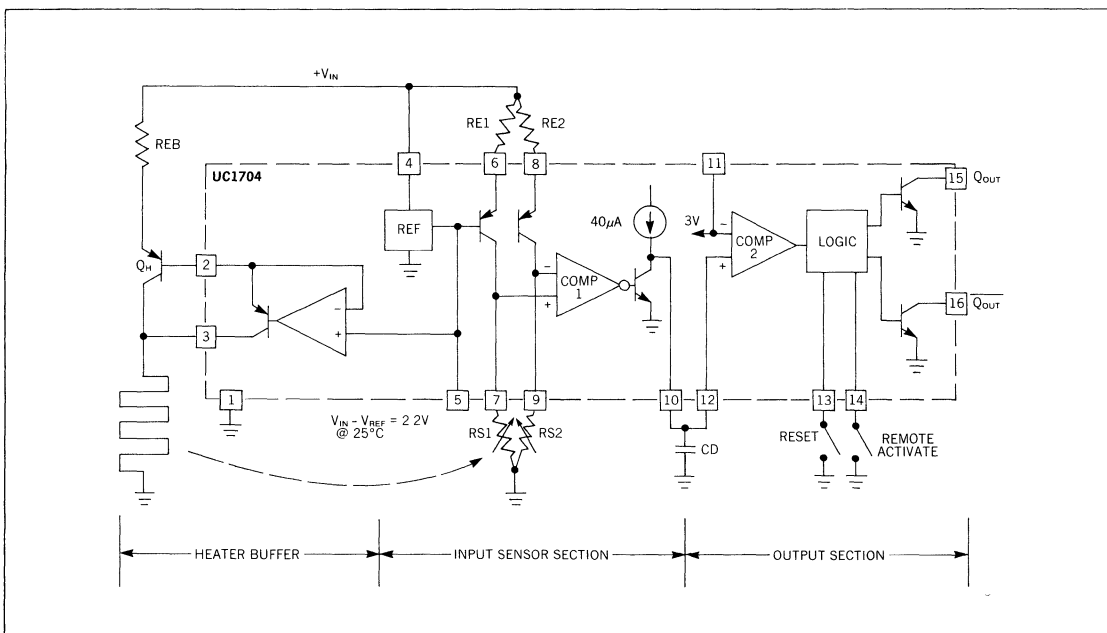
Reset terminal low overrides the Remote Activate Pin releasing the latch.

Reference Buffer

This circuit is designed to provide up to 100mA to drive a high-current external PNP transistor useful for powering a heater for differential temperature measurements. Care must be taken that power dissipation in Q₆ does not cause excessive thermal gradients which will degrade the accuracy of the sensing circuitry.

Using a heating element attached to a temperature sensitive resistor, RS1, in one leg of the input bridge implements a flow sensor for either gasses or liquids. As long as there is flow, heat from the element is carried away and the sensor voltage remains below threshold. Using an identical sensor, RS2, without a heater to establish this threshold compensates for the ambient temperature of the flow.

Typical Application For Monitoring Liquid or Gas Flow



LINEAR INTEGRATED CIRCUITS

Dual Output Driver

UC1706
UC3706

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below:

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0° to +70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation.

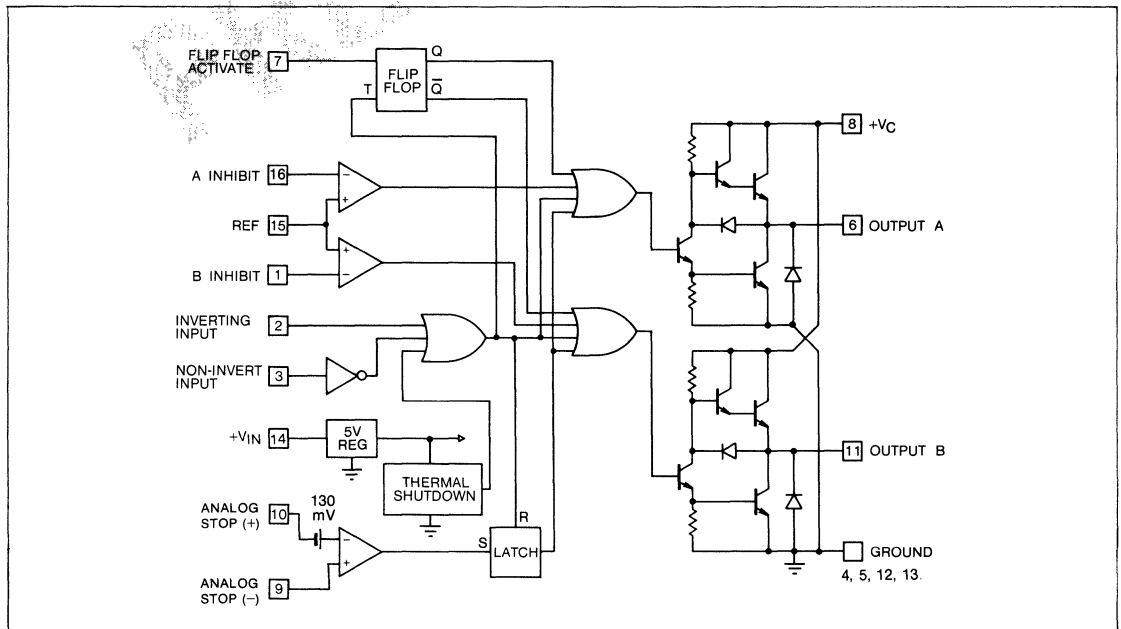
TRUTH TABLE

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

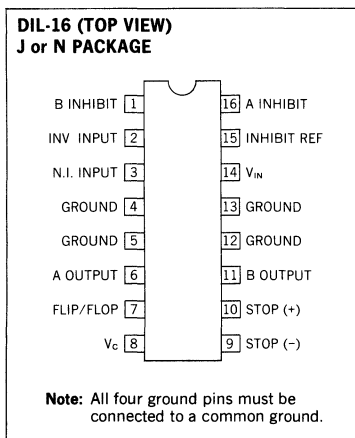
OUT = \overline{INV} and N.I.

\overline{OUT} = INV or $\overline{N.I.}$

BLOCK DIAGRAM



CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	$\pm 500\text{mA}$	$\pm 500\text{mA}$
Peak Transient	$\pm 1.5\text{A}$	$\pm 1.0\text{A}$
Capacitive Discharge Energy	20 μJ	15 μJ
Digital Inputs	5.5V	5.5V
Inhibit Inputs	5.5V	5.5V
Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at $T_A = 25^\circ\text{C}$.2W	.1W
Derate above 50°C	20mW/ $^\circ\text{C}$	10mW/ $^\circ\text{C}$
Power Dissipation at T (Leads/Case) = 25°C	.5W	.2W
Derate for Ground Lead Temperature above 25°C	40mW/ $^\circ\text{C}$	—
Derate for Case Temperature above 25°C	—	16mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$	
Load Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1706 and 0°C to $+70^\circ\text{C}$ for the UC3706; $V_{IN} = V_C = 20\text{V}$.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IN} Supply Current	$V_{IN} = 40\text{V}$		8	10	mA
V_C Supply Current	$V_C = 40\text{V}$, Outputs Low		4	5	mA
V_C Leakage Current	$V_{IN} = 0$, $V_C = 40\text{V}$.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	$V_I = 0$		-0.6	-1.0	mA
Input Leakage	$V_I = 5\text{V}$.05	0.1	mA
Output High Sat., $V_C - V_O$	$I_o = -50\text{mA}$			2.0	V
Output High Sat., $V_C - V_O$	$I_o = -500\text{mA}$			2.5	V
Output Low Sat., V_O	$I_o = 50\text{mA}$			0.4	V
Output Low Sat., V_O	$I_o = 500\text{mA}$			2.5	V
Inhibit Threshold	$V_{REF} = 0.5\text{V}$	0.4		0.6	V
Inhibit Threshold	$V_{REF} = 3.5\text{V}$	3.3		3.7	V
Inhibit Input Current	$V_{REF} = 0$		-10	-20	μA
Analog Threshold	$V_{CM} = 0$ to 15V	100	130	150	mV
Input Bias Current	$V_{CM} = 0$		-10	-20	μA
Thermal Shutdown			155		$^\circ\text{C}$

TYPICAL SWITCHING CHARACTERISTICS ($V_{IN} = V_C = 20V$, $T_A = 25^\circ C$. Delays measured 50% in to 50% out.)

PARAMETER	TEST CONDITIONS	OUTPUT $C_L =$			UNITS
		open	1.0	2.2	
From Inv. Input to Output:					nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (-) Input = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION**Outputs**

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs — the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-

on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to ($V_{IN} - 3V$). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

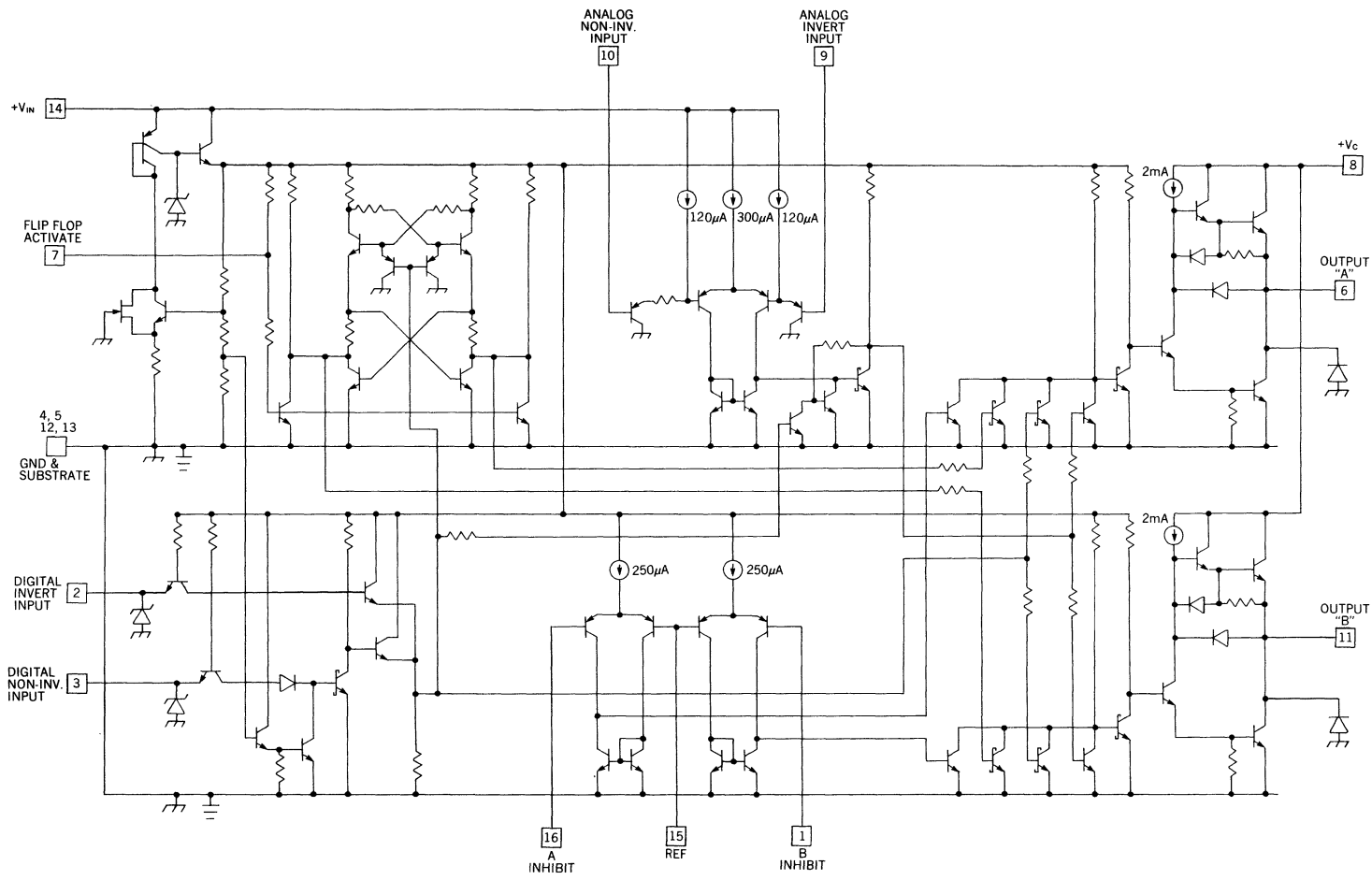
Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C . When combined with a UC1840 PWM, the Driver Bias switch can be used to supply V_{IN} to the UC1706. V_{IN} switching should be fast as if V_C is high, undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

SIMPLIFIED SCHEMATIC DIAGRAM



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UC1706
 UC3706

LINEAR INTEGRATED CIRCUITS

Stepper Motor Drive Circuit

UC1717
UC3717

FEATURES

- Half-step and full-step capability
- Bipolar constant current motor drive
- Built-in fast recovery Schottky commutating diodes
- Wide range of current control 5-1000mA
- Wide voltage range 10-45V
- Designed for unregulated motor supply voltage
- Current levels can be selected in steps or varied continuously
- Thermal overload protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$, while the UC3717 is characterized for 0°C to $+70^{\circ}\text{C}$.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage

Logic Supply, V_{CC} 7V

Output Supply, V_m 45V

Input Voltage

Logic Inputs (Pins 7, 8, 9) 6V

Analog Input (Pin 10) V_{CC}

Reference Input (Pin 11) 15V

Input Current

Logic Inputs (Pins 7, 8, 9) -10mA

Analog Inputs (Pins 10, 11) -10mA

Output Current (Pins 1,15)

..... $\pm 1\text{A}$

Junction Temperature, T_j

..... $+150^{\circ}\text{C}$

Thermal Resistance, Junction to Ambient (NE Package)

..... $45^{\circ}\text{C}/\text{W}$

Thermal Resistance, Junction to Case (NE Package)

..... $11^{\circ}\text{C}/\text{W}$

Thermal Resistance, Junction to Ambient (J Package)

..... $100^{\circ}\text{C}/\text{W}$

Thermal Resistance, Junction to Case (J Package)

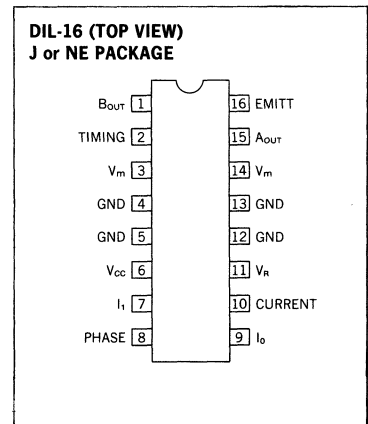
..... $60^{\circ}\text{C}/\text{W}$

Storage Temperature Range, T_s

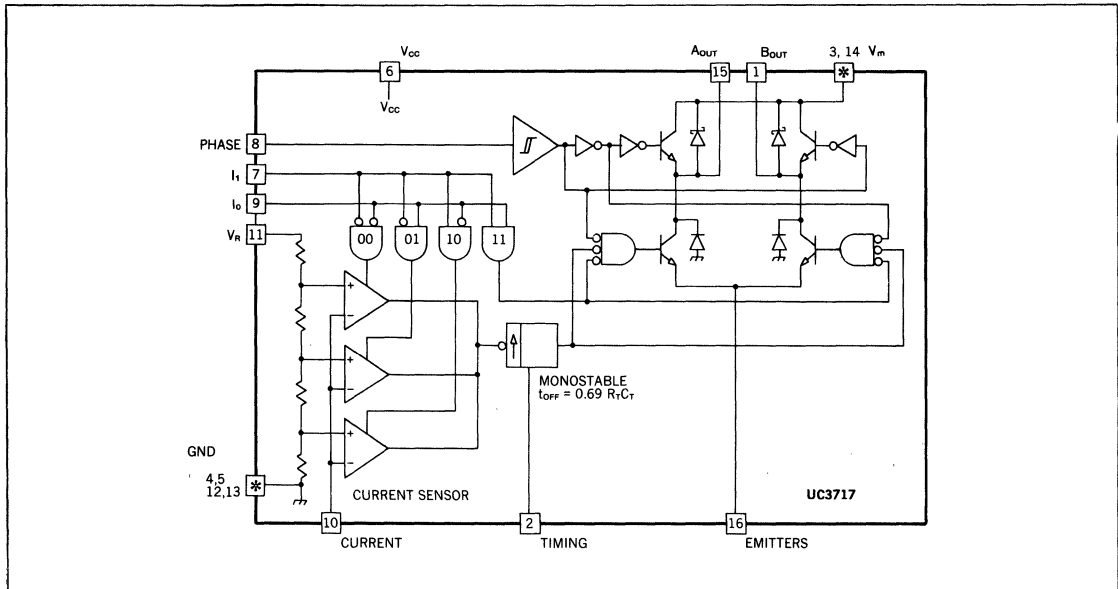
..... -55°C to $+150^{\circ}\text{C}$

Note: 1. All voltages are with respect to ground, Pins 4, 5, 12, 13.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_m	10		40	V
Output Current, I_m	20		800	mA
Rise Time Logic Inputs, t_r			2	μs
Fall Time Logic Inputs, t_f			2	μs
Ambient Temperature, T_a				$^{\circ}C$
UC1717	-55		125	$^{\circ}C$
UC3717	0		70	$^{\circ}C$

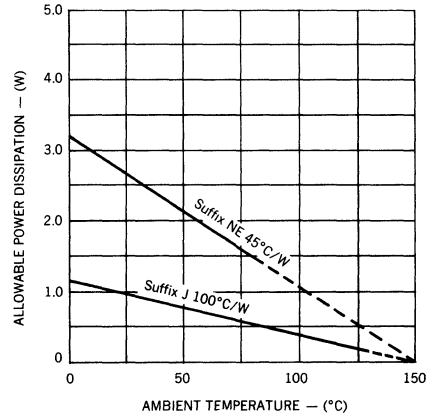


Figure 1.

ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current, I_{CC}				25	mA	
High-Level Input Voltage, Pins 7, 8, 9		2.0			V	
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V	
High-Level Input Current, Pins 7, 8, 9	$V_i = 2.4V$			20	μA	
Low-Level Input Current, Pins 7, 8, 9	$V_i = 0.4V$	-0.4			mA	
Comparator Threshold Voltage	$I_o = 0$ $I_i = 0$	$V_R = 5.0V$	390	420	440	mV
	$I_o = 1$ $I_i = 0$		230	250	270	mV
	$I_o = 0$ $I_i = 1$		65	80	90	mV
Comparator Input Current		-20		20	μA	
Output Leakage Current	$I_o = 1$ $I_i = 1$ $T_A = +25^{\circ}C$			100	μA	
Total Saturation Voltage Drop	$I_m = 500mA$			4.0	V	
Total Power Dissipation	$I_m = 500mA$, $f_s = 30kHz$		1.4	2.1	W	
	$I_m = 800mA$, $f_s = 30kHz$		2.9	3.1	W	
Cut Off Time, t_{OFF}	See Figure 5 and 6 $V_m = 10V$ $t_{ON} \cong 5\mu s$	25	30	35	μs	
Turn Off Delay, t_d	See Figure 5 and 6 $T_A = +25^{\circ}C$; $dV_c/dt \cong 50mV/\mu s$		1.6	2.0	μs	
Thermal Shutdown Junction Temperature		+160		+180	$^{\circ}C$	

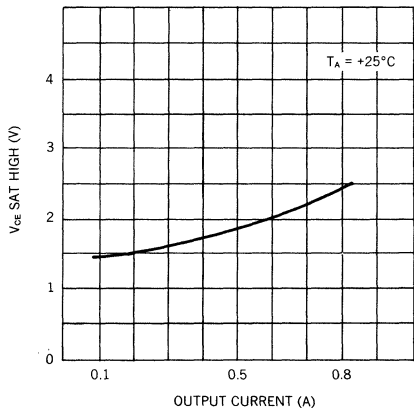


Figure 2. Typical Source Saturation Voltage vs Output Current

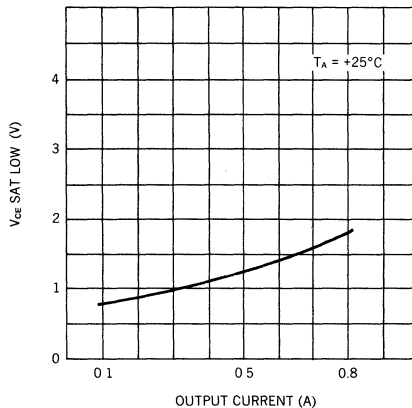


Figure 3. Typical Sink Saturation Voltage vs Output Current

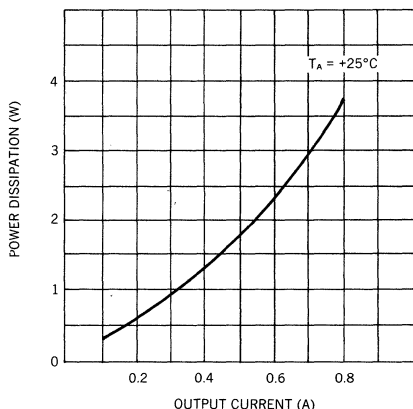


Figure 4. Typical Power Losses vs Output Current

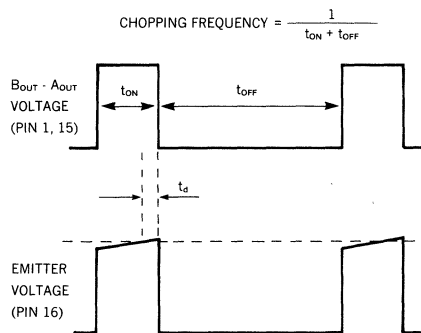


Figure 5. Connections and Component Values as in Figure 6

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions.

- (1) Phase Logic and H-Bridge Output Stage
- (2) Voltage Divider with three Comparators for current control
- (3) Two Logic inputs for Digital current level select
- (4) Monostable for off time generation

Input Logic

If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input

The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input

coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage

The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used across the source transistors. The Schottky diodes allow the current to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

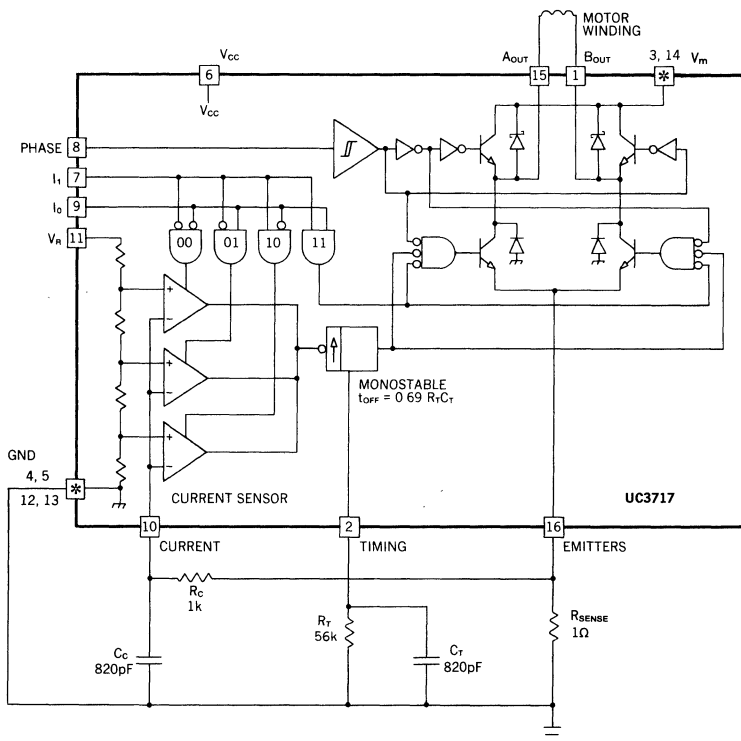


Figure 6.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

TABLE 1

I ₀	I ₁	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	CURRENT INHIBIT

Current Control

The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I₀, I₁) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by R_T and C_T connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and micro-stepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor R_s (pin 16).

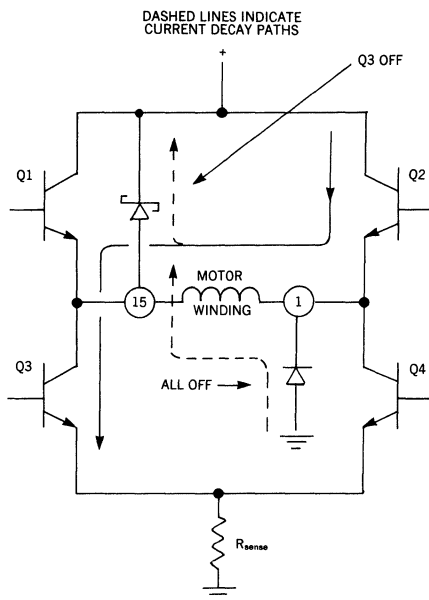


Figure 7. Simplified Schematic of Output Stage

Single-Pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components R_T and C_T as:

$$t_{OFF} = 0.69 R_T C_T$$

If a new trigger signal should occur during t_{OFF} , it is ignored.

Overload Protection

The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation

When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low-pass filter R_C , C_C to the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noticed at this time that the

slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

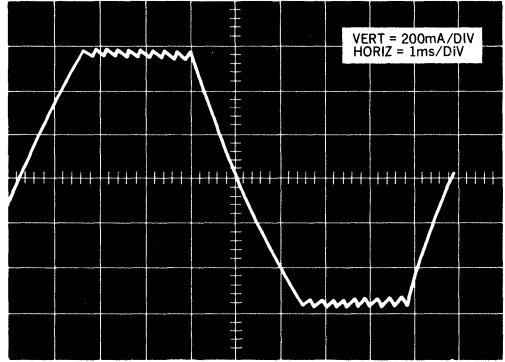


Figure 8.

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

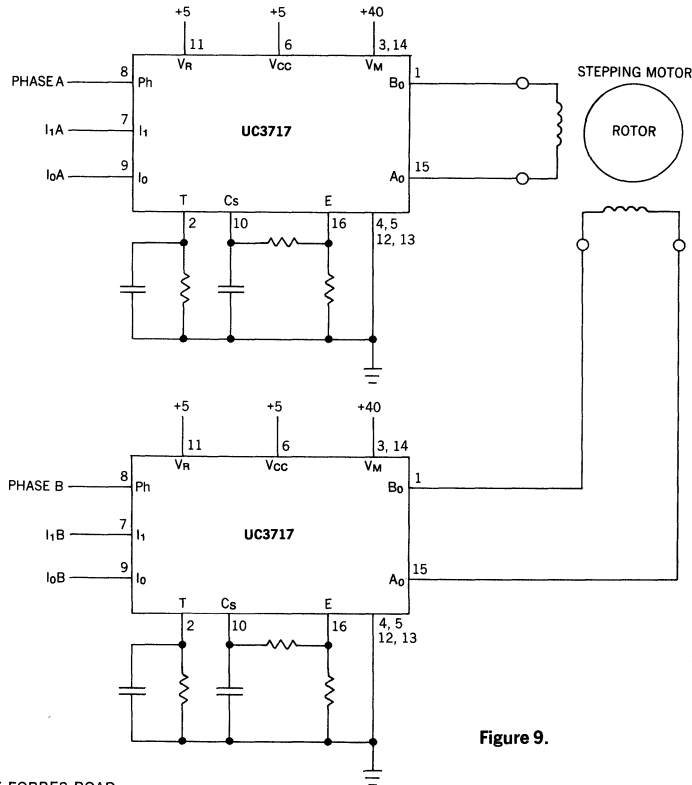


Figure 9.

The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

The UC3717 can also be used to drive an external high power output stage such as the Unitrode PIC900 hybrid circuit in an 18-Pin dual-in-line package. The 5A output of the PIC900 can be controlled with as little as 5mA base drive. Using the UC3717 to drive the PIC900 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

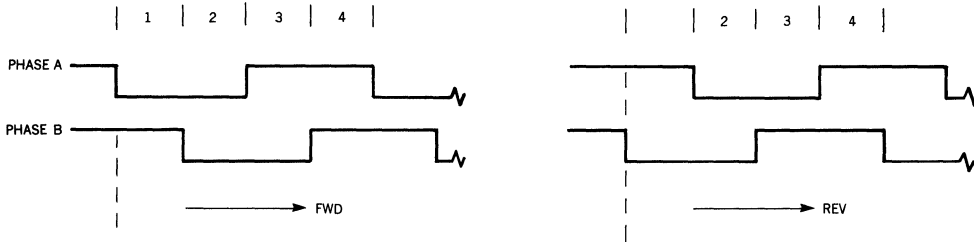


Figure 10. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

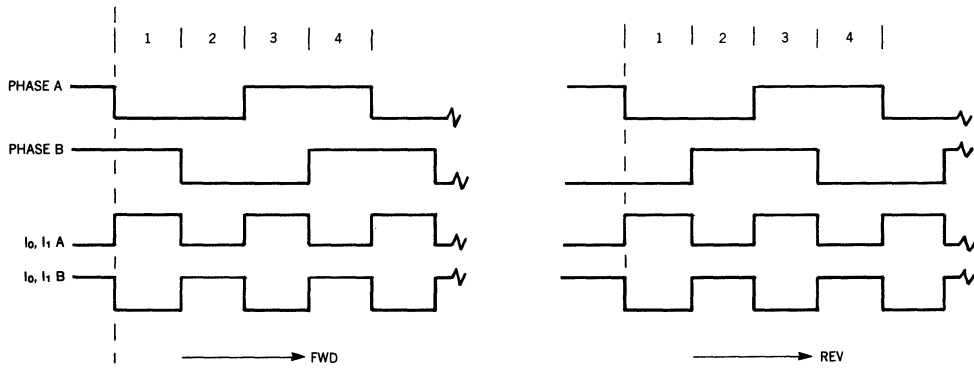


Figure 11. Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

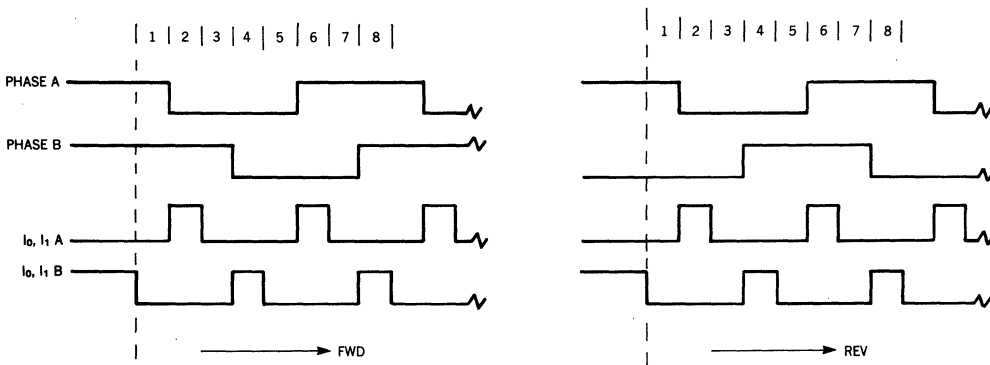


Figure 12. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

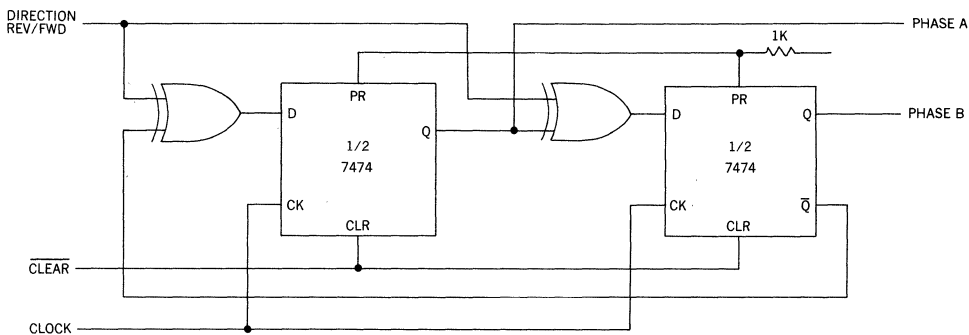


Figure 13. Full Step, Bidirectional Two Phase Drive Logic

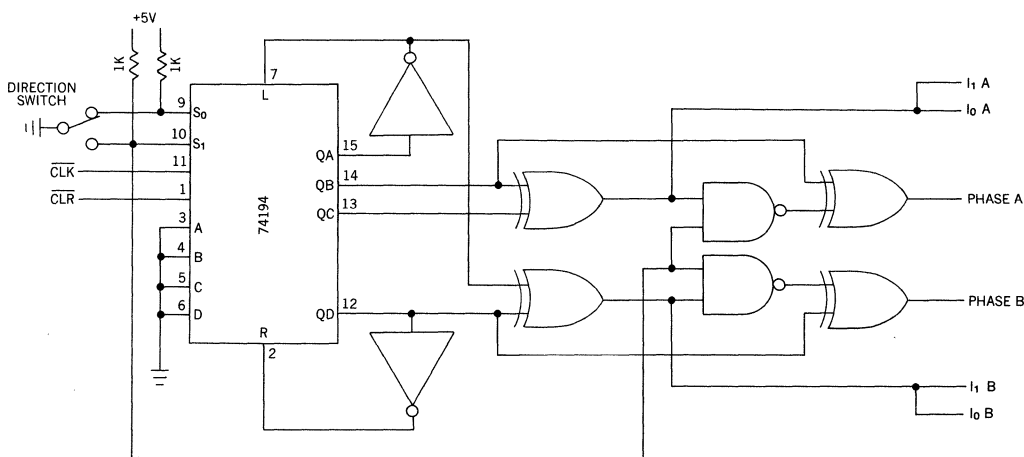


Figure 14. Half Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping

In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_A input can be used to boost the current of the single energized winding.

Ramping

Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses

Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponential matter as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference

Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1 μ F ceramic capacitors for high frequency bypass located near the drive package across $V+$ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

- UNITRODE TYPE NUMBER
- UC3717NE — 16 Pin Dual-in-line (DIL) "Bat Wing" Package
- UC3717J — 16 Pin Dual-in-line Ceramic Package
- UC1717J — 16 Pin Dual-in-line Ceramic Package

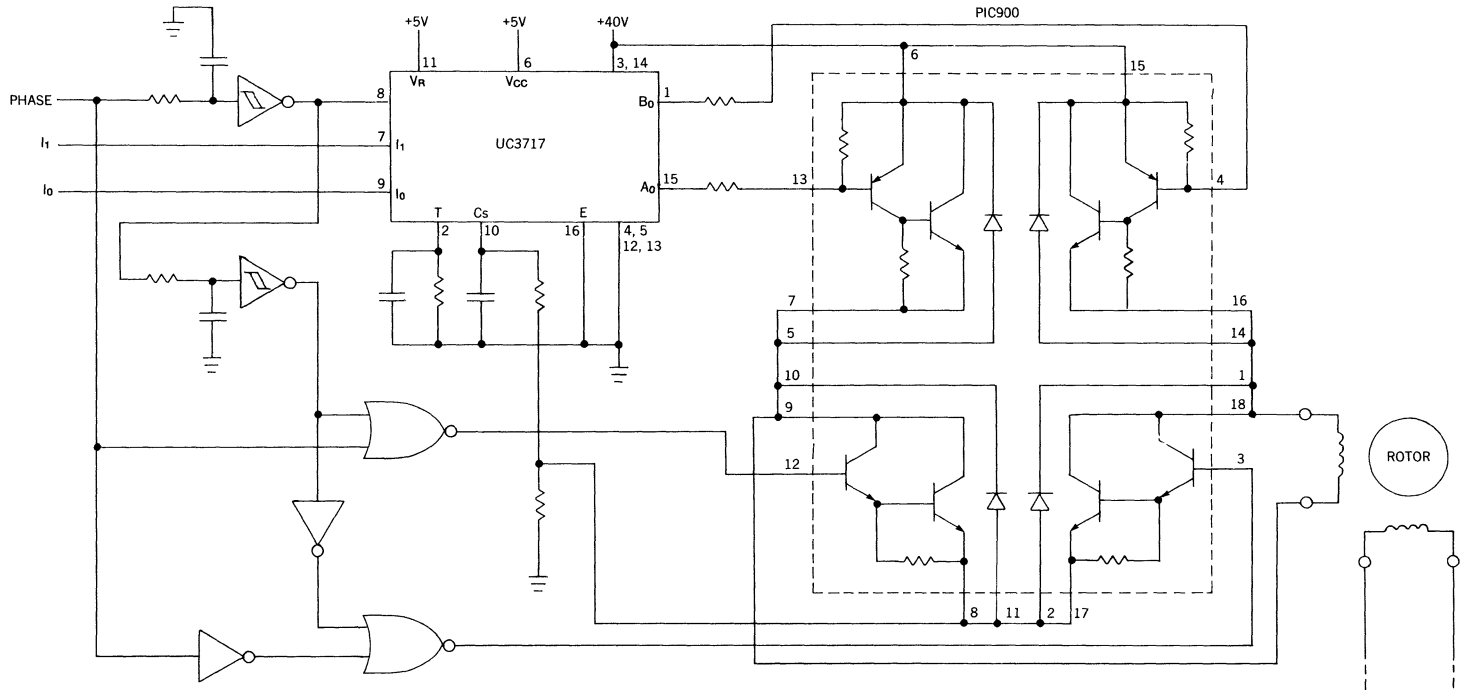


Figure 15. UC3717 with PIC900 Power Amplifier

LINEAR INTEGRATED CIRCUITS

High Efficiency Linear Regulator

UC1834
UC2834
UC3834

FEATURES

- Minimum $V_{IN} - V_{OUT}$ less than 0.5V at 5A load with external pass device
- Equally usable for either positive or negative regulator design
- Adjustable low threshold current sense amplifier
- Under and over-voltage fault alert with programmable delay
- Over-voltage fault latch with 100mA crowbar drive output

DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

ABSOLUTE MAXIMUM RATINGS (Note 1)

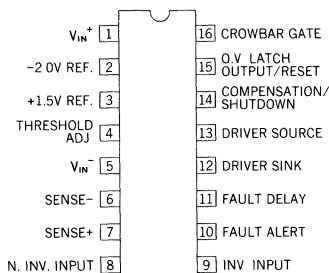
Input Supply Voltage, V_{IN}^+	40V
Driver Current	400mA
Driver Source to Sink Voltage	40V
Crowbar Current	-200mA
+1.5V Reference Output Current	-10mA
Fault Alert Voltage	40V
Fault Alert Current	15mA
Error Amplifier Inputs	-0.5V to 35V
Current Sense Inputs	-0.5V to 40V
O.V. Latch Output Voltage	-0.5V to 40V
O.V. Latch Output Current	15mA
Power Dissipation at $T_A = 25^\circ\text{C}$ Derate at 10mW/ $^\circ\text{C}$ above $T_A = 50^\circ\text{C}$	1000mW
Power Dissipation at $T_C = 25^\circ\text{C}$ Derate at 16mW/ $^\circ\text{C}$ above $T_C = 25^\circ\text{C}$	2000mW
Thermal Resistance, Junction to Ambient	100 $^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	60 $^\circ\text{C}/\text{W}$
Operating Junction Temperature	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10 seconds)	300 $^\circ\text{C}$

Note: 1. Voltages are reference to V_{IN}^- , Pin 5.

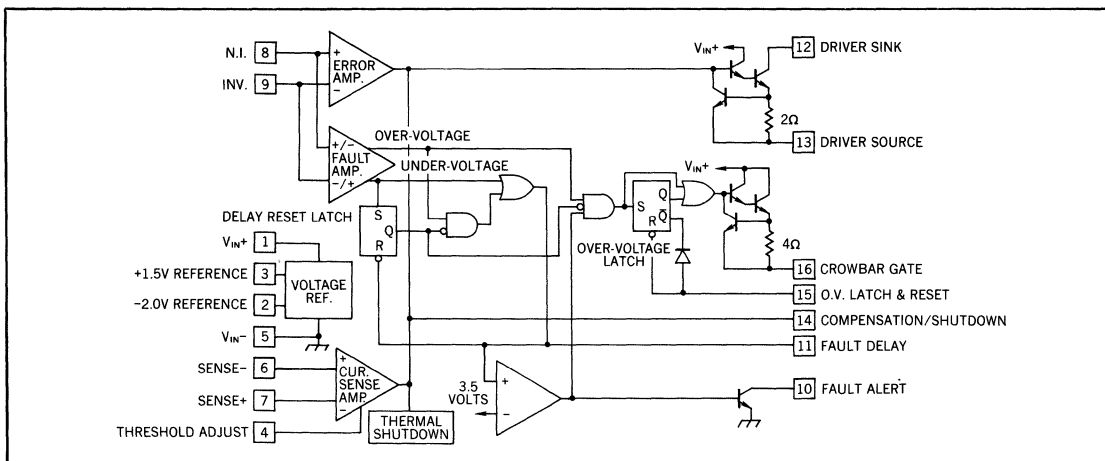
Currents are positive into, negative out of the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1834; -25°C to $+85^{\circ}\text{C}$ for the UC2834; and 0°C to $+70^{\circ}\text{C}$ for the UC3834; $V_{IN}^+ = 15\text{V}$, $V_{IN}^- = 0\text{V}$.)

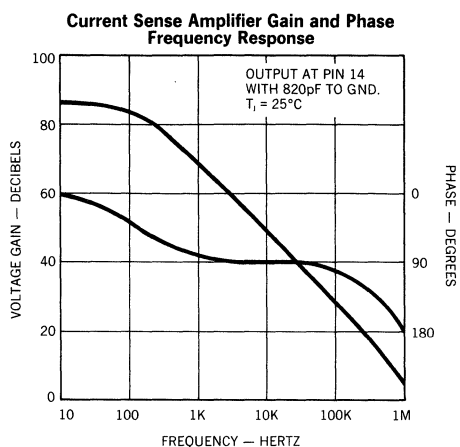
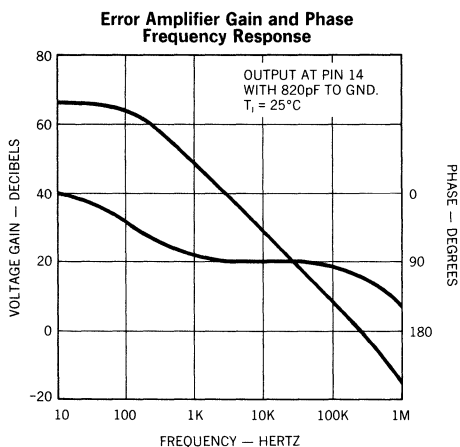
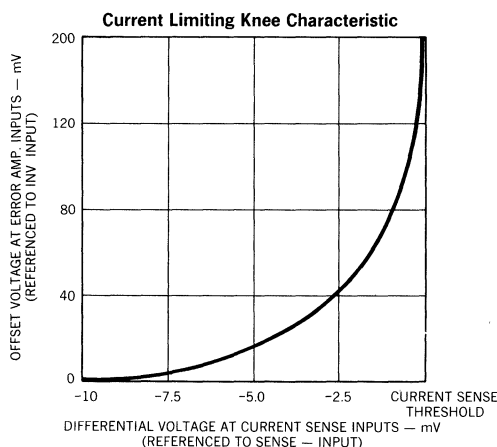
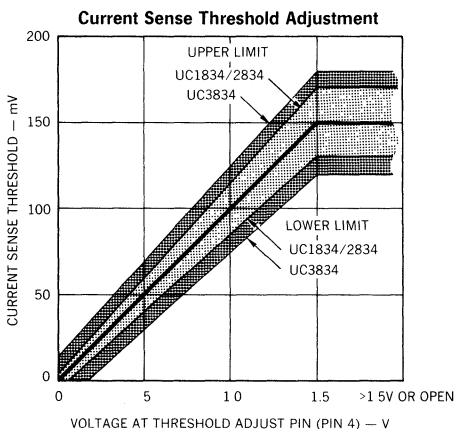
PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	$T_I = 25^{\circ}\text{C}$	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{I(\text{MIN})} \leq T_I \leq T_{I(\text{MAX})}$	1.47		1.53	1.455		1.545	
Line Regulation	$V_{IN}^+ = 5$ to 35V		1	10		1	15	mV
Load Regulation	$I_{OUT} = 0$ to 2mA		1	10		1	15	mV
-2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN}^+)	$T_I = 25^{\circ}\text{C}$	2.04	-2	1.96	2.06	-2	1.94	V
	$T_{I(\text{MIN})} \leq T_I \leq T_{I(\text{MAX})}$	2.06		1.94	2.08		1.92	
Line Regulation	$V_{IN}^+ = 5$ to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		k Ω
Error Amplifier Section								
Input Offset Voltage	$V_{CM} = 1.5\text{V}$		1	6		1	10	mV
Input Bias Current	$V_{CM} = 1.5\text{V}$		-1	-4		-1	-8	μA
Input Offset Current	$V_{CM} = 1.5\text{V}$		0.1	1		0.1	2	μA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN}^+ Pin 13, 20Ω to V_{IN}^-	50	65		50	65		dB
CMRR	$V_{CM} = 0.5$ to 33V , $V_{IN}^+ = 35\text{V}$	60	80		60	80		dB
PSRR	$V_{IN}^+ = 5$ to 35V , $V_{CM} = 1.5\text{V}$	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	$I_{OUT} = 100\text{mA}$		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V , Pin 13 = V_{IN}^- , Pin 14 = V_{IN}^-		0.1	50		0.1	50	μA
Shutdown Input Voltage at Pin 14	$I_{OUT} \leq 100\mu\text{A}$, Pin 13 = V_{IN}^- , Pin 12 = V_{IN}^+	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN}^- , Pin 12 = V_{IN}^+ , $I_{OUT} \leq 100\mu\text{A}$, Pin 13 = V_{IN}^-		-100	-150		-100	-150	μA
Thermal Shutdown (Note 3)			165			165		$^{\circ}\text{C}$
Fault Amplifier Section								
Under- and Over- Voltage Fault Threshold	$V_{CM} = 1.5\text{V}$, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	$V_{IN}^+ = 35\text{V}$, $V_{CM} = 1.5$ to 33V		-0.4	-0.8		-0.4	-1.0	%/V
Supply Sensitivity	$V_{CM} = 1.5\text{V}$, $V_{IN}^+ = 5$ to 35V		-0.5	-1.0		-0.5	-1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/ μF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	$I_{OUT} = 1\text{mA}$		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	$I_{OUT} = 1\text{mA}$		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		-100	-175		-100	-175		mA
Crowbar Gate Leakage Current	$V_{IN}^+ = 35\text{V}$, Pin 16 = V_{IN}^-		-0.5	-50		-0.5	-50	μA

Note: 2. When using both the 1.5V and -2.0V references the current out of Pin 3 should be balanced by an equivalent current into Pin 2. The -2.0V output will change -2.3mV per μA of imbalance.

3. Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown), the O.V. Latch will be reset.

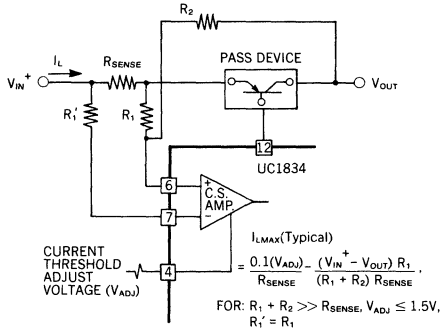
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1834; -25°C to $+85^\circ\text{C}$ for the UC2834; and 0°C to $+70^\circ\text{C}$ for the UC3834; $V_{IN^+} = 15\text{V}$, $V_{IN^-} = 0\text{V}$.)

PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, $V_{CM} = V_{IN^+}$ or V_{IN^-}	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, $V_{CM} = V_{IN^+}$ or V_{IN^-}	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, $V_{CM} = V_{IN^-}$, $V_{IN^+} = 5$ to 35V		-0.1	-0.3		-0.1	-0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		-2	-10		-2	-10	μA
Sense Input Bias Current	$V_{CM} = V_{IN^+}$		100	200		100	200	μA
	$V_{CM} = V_{IN^-}$		-100	-200		-100	-200	

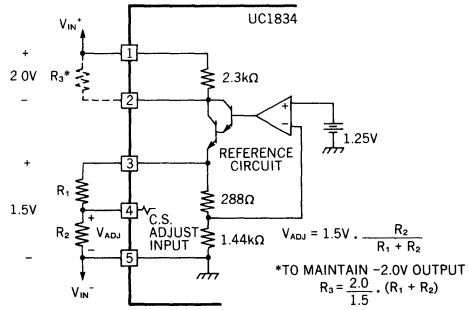


APPLICATION INFORMATION

Foldback Current Limiting



Setting The Threshold Adjust Voltage (V_{ADJ})



3

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V_{E/A}} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V_{C.S./A}} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500\text{kHz}$ and $|Z_L(f)| \leq 1\text{M}\Omega$,

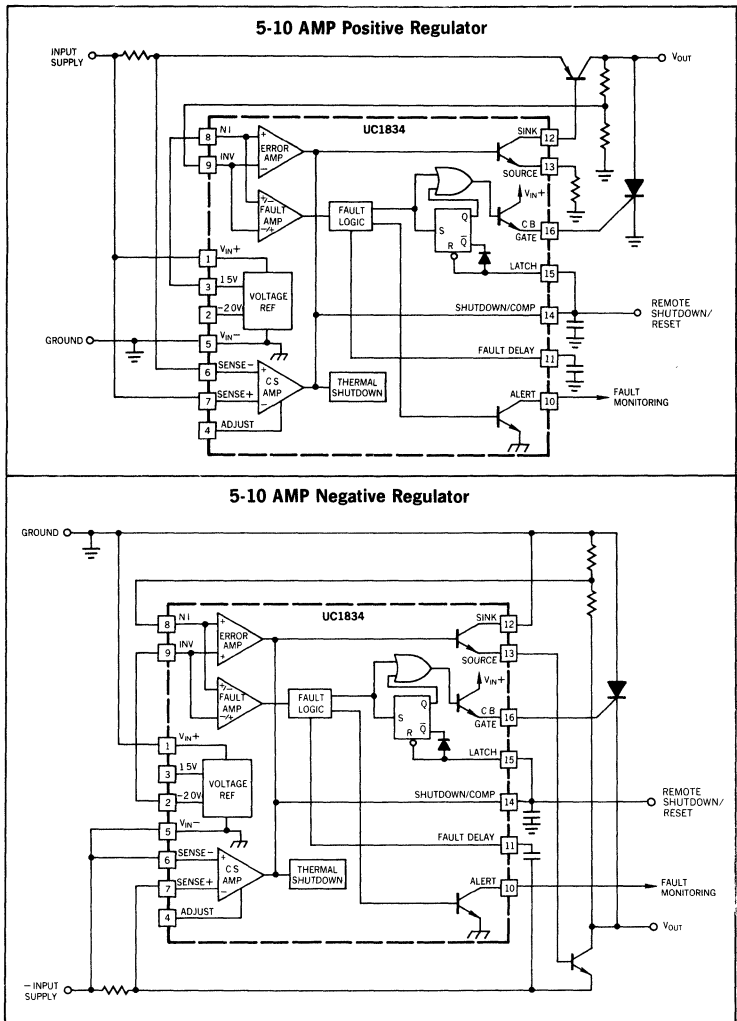
where:

A_V = small signal voltage gain to Pin 14,
 $Z_L(f)$ = load impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

TYPICAL APPLICATIONS



LINEAR INTEGRATED CIRCUITS

Programmable, Off-Line, PWM Controller

UC1840
UC2840
UC3840

FEATURES

- All control, driving, monitoring, and protection functions included
- Low-current, off-line start circuit
- Feed-forward line regulation over 4 to 1 input range
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- No start-up or shutdown transients
- Slow turn-on and maximum duty-cycle clamp
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- Remote, pulse-commandable start/stop
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 18-pin DIL package

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

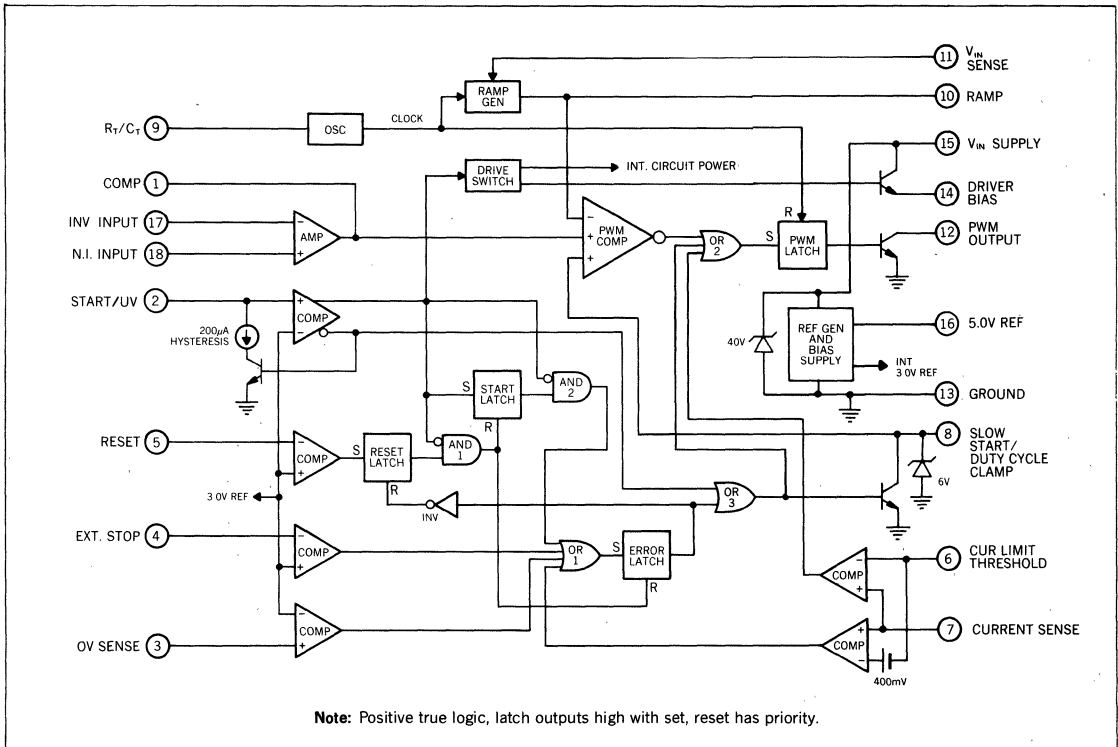
In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. The UC2840 and UC3840 are designed for operation from -25°C to $+85^{\circ}\text{C}$ and 0°C to $+70^{\circ}\text{C}$, respectively.

BLOCK DIAGRAM



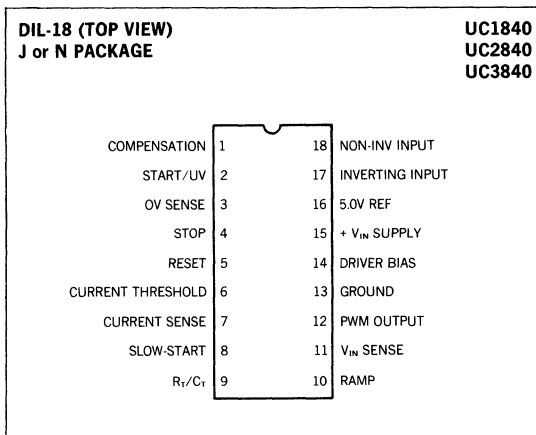
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +V_{IN} (Pin 15)

Voltage Driven	+32V
Current Driven, 100mA maximum	Self-limiting
PWM Output Voltage (Pin 12)	40V
PWM Output Current, Steady-State (Pin 12)	400mA
PWM Output Peak Energy Discharge	20μJoules
Driver Bias Current (Pin 14)	-200mA
Reference Output Current (Pin 16)	-50mA
Slow-Start Sink Current (Pin 8)	20mA
V _{IN} Sense Current (Pin 11)	10mA
Current Limit Inputs (Pins 6 & 7)	-0.5 to +5.5V
Comparator Inputs (Pins 2, 3, 4, 5, 17, 18)	-0.3 to +32V
Power Dissipation at T _A = 25°C	1000mW
Derate at 10 mW/°C for T _A above 50°C	
Power Dissipation at T _C = 25°C	2000mW
Derate at 16 mW/°C for T _C above 25°C	
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Notes: 1. All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1840, -25°C to +85°C for the UC2840, and 0°C to 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV)

PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Power Inputs									
Start-Up Current	V _{IN} = 30V, Pin 2 = 2.5V, T _J = 25°C		4	5.5		4	5.5	mA	
Start-Up Current T.C.*	V _{IN} = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C	
Operating Current	V _{IN} = 30V, Pin 2 = 3.5V		5	10	15	5	10	15	mA
Supply OV Clamp	V _{IN} = 20mA		33	40	45	33	40	48	V
Reference Section									
Reference Voltage	T _J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V	
Line Regulation	V _{IN} = 8 to 30V		10	15		10	20	mV	
Load Regulation	I _L = 0 to 20mA		10	20		10	30	mV	
Temperature Coefficient*	Over operating temperature range			±0.4			±0.4	mV/°C	
Short Circuit Current	V _{REF} = 0, T _J = 25°C		-80	-100		-80	-100	mA	
Oscillator									
Nominal Frequency	T _J = 25°C	47	50	53	45	50	55	kHz	
Voltage Stability	V _{IN} = 8 to 30V		0.5	1		0.5	1	%	
Temperature Coefficient*	Over operating temperature range			±0.08			±0.08	%/°C	
Maximum Frequency	R _T = 2kΩ, C _T = 330pF	500			500			kHz	
Ramp Generator									
Ramp Current, Minimum	I _{SENSE} = -10μA		-11	-14		-11	-14	μA	
Ramp Current, Maximum	I _{SENSE} = 1.0mA	-0.9	-0.95		-0.9	-0.95		mA	
Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V	
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V	

*Guaranteed by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1840, -25°C to $+85^\circ\text{C}$ for the UC2840, and 0°C to 70°C for the UC3840; $V_{IN} = 20\text{V}$, $R_T = 20\text{k}$, $C_T = .001\text{mfd}$, $C_R = .001\text{mfd}$, Current Limit Threshold = 200mV)

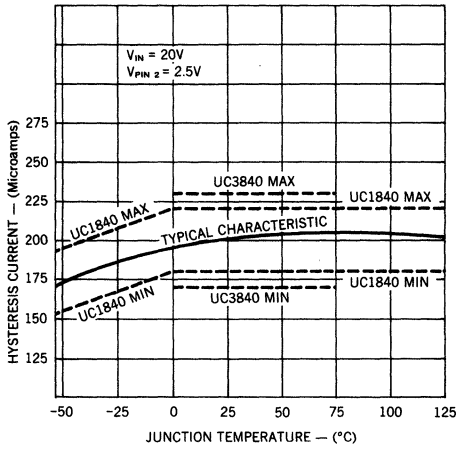
PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	$V_{CM} = 5.0\text{V}$		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	$\Delta V_o = 1$ to 3V	60	66		60	66		dB
Output Swing (Max. Output \leq Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	$V_{CM} = 1.5$ to 5.5V	70	80		70	80		dB
PSRR	$V_{IN} = 8$ to 30V	40	50		40	50		dB
Short Circuit Current	$V_{COMP} = 0\text{V}$		-4	-10		-4	-10	mA
Gain Bandwidth*	$T_J = 25^\circ\text{C}$, $A_{VOL} = 0\text{dB}$	1	2		1	2		MHz
Slew Rate*	$T_J = 25^\circ\text{C}$, $A_{VCL} = 0\text{dB}$		0.8			0.8		$\text{V}/\mu\text{s}$
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak $< 4.2\text{V}$	5		95	5		95	%
Output Saturation	$I_{OUT} = 20\text{mA}$		0.2	0.4		0.2	0.4	V
Output Saturation	$I_{OUT} = 200\text{mA}$		1.7	2.2		1.7	2.2	V
Output Leakage	$V_{OUT} = 40\text{V}$		0.1	10		0.1	10	μA
Comparator Delay*	Pin 8 to Pin 12 $T_J = 25^\circ\text{C}$, $R_L = 1\text{k}\Omega$		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		-1.0	-3.0		-1.0	-3.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V , $T_J = 25^\circ\text{C}$	180	200	220	170	200	230	μA
Input Leakage	Input V = 20V		0.1	10		0.1	10	μA
Driver Bias Saturation Voltage, $V_{IN} - V_{OH}$	$I_B = -50\text{mA}$		2	3		2	3	V
Driver Bias Leakage	$V_B = 0\text{V}$		-0.1	-10		-0.1	-10	μA
Slow-Start Saturation	$I_S = 2\text{mA}$		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	$V_S = 4.5\text{V}$		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	μA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	$T_J = 25^\circ\text{C}$, Pin 7 to 12, $R_L = 1\text{k}$		200	400		200	400	ns

*Guaranteed by design. Not 100% tested in production.

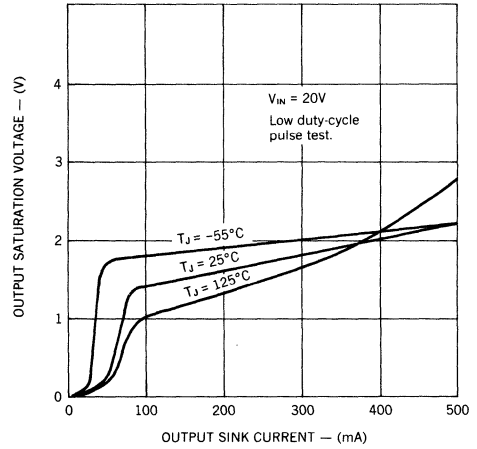
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T . Frequency = $\frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	This comparator performs three functions— With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200 μ A hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider $R_S R_{DC}$.
5. Start Latch:	Keeps low input voltage at initial turn-on from being defined as a UV fault. Sets at start level to monitor for UV fault.
6. Reset Latch:	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the UV low threshold, allowing a restart.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold. Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.

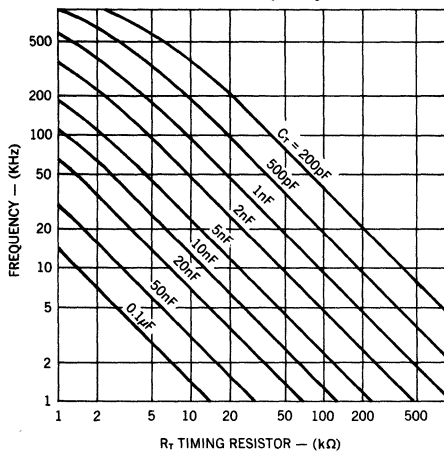
Start/UV Hysteresis Current



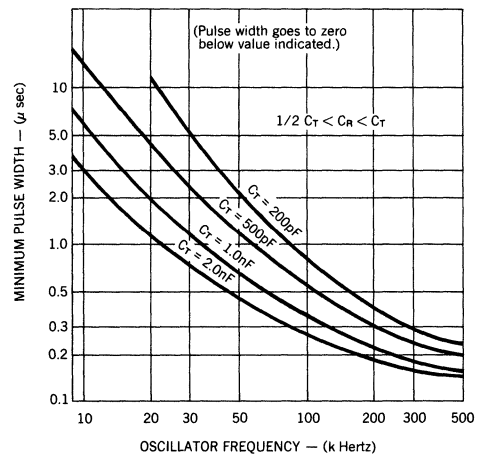
PWM Output Saturation Voltage



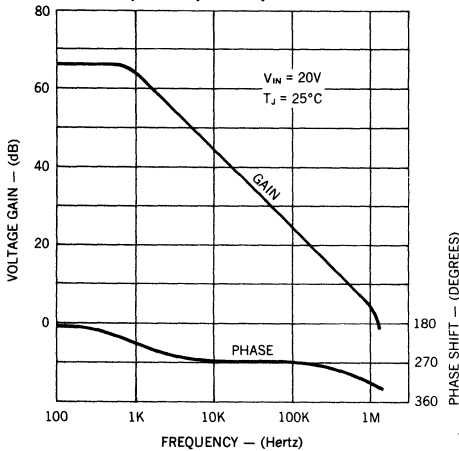
Oscillator Frequency



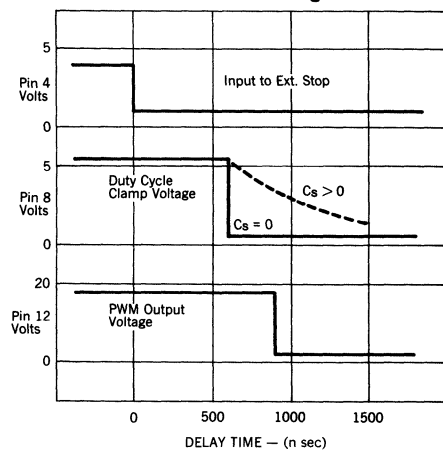
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Phase

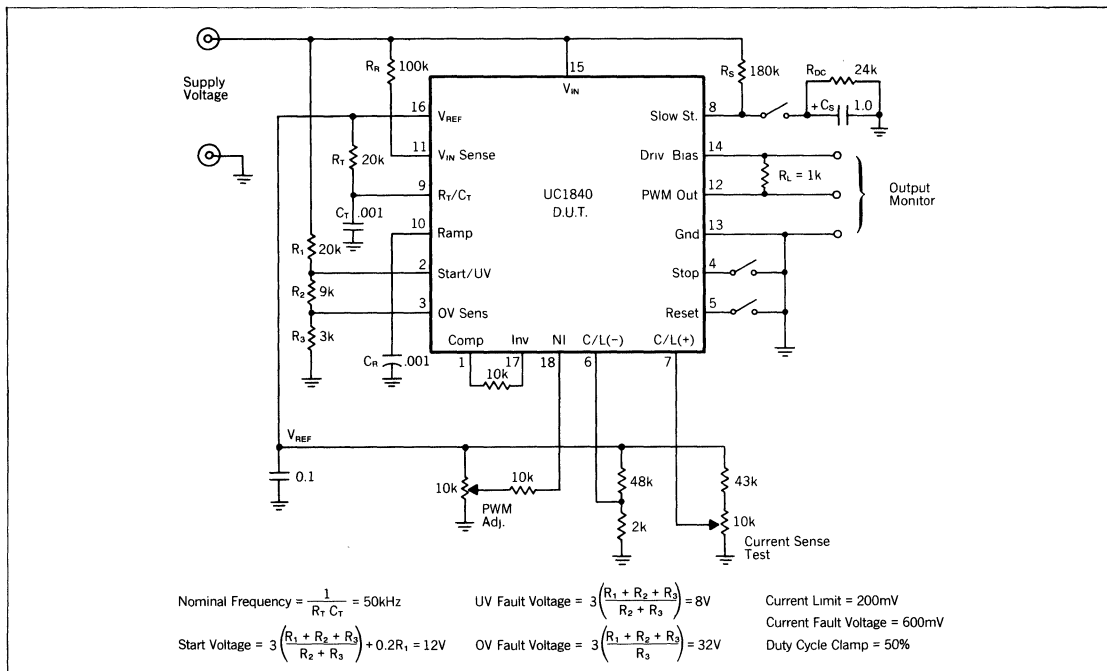


Shutdown Timing



OPEN-LOOP TEST CIRCUIT

3



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line regulation.

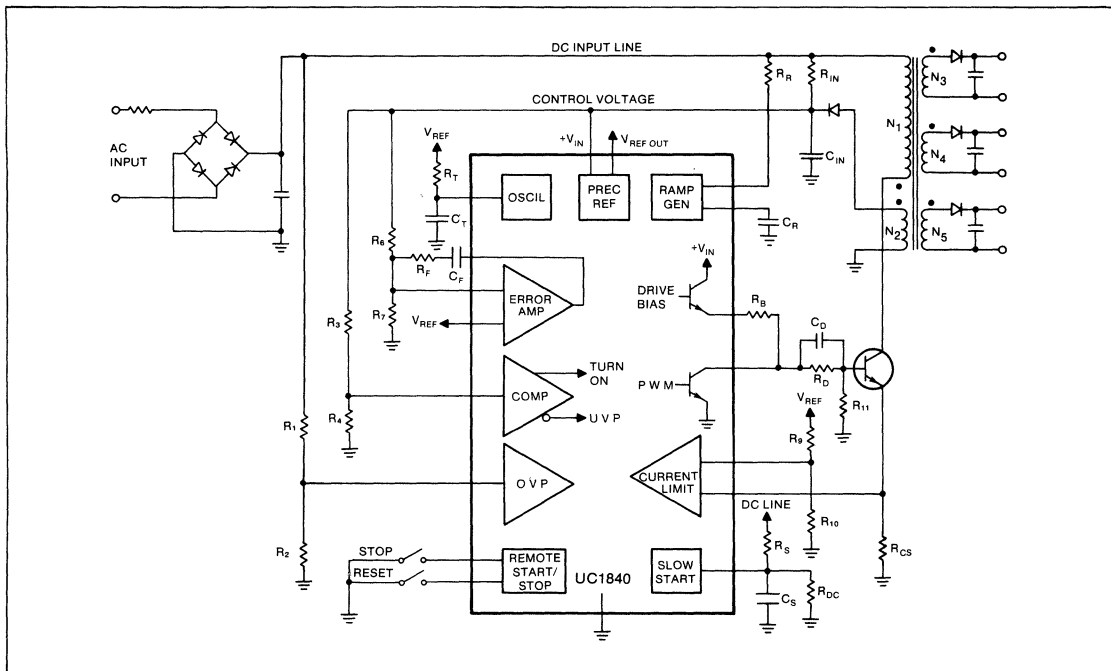
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output. The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

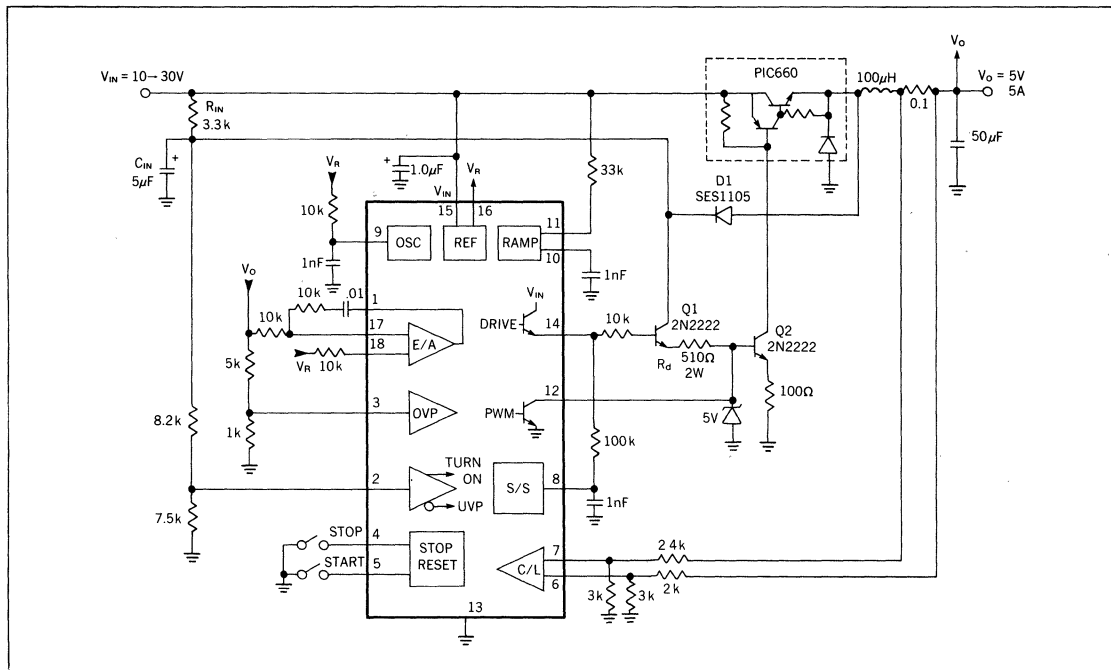
REGULATOR APPLICATION (B)

Although primarily intended for transformer-coupled power systems, the UC1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the UC1840 requires recycling the voltage sensed by the Start/UV Comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown in Figure B (next page). In this simple, non-isolated, buck regulator; diode D1 provides a low-impedance bootstrapped drive power source after start-up is achieved through R_{IN} and C_{IN} . When a fault shutdown terminates switching action, the loading of Q1 and R_d will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

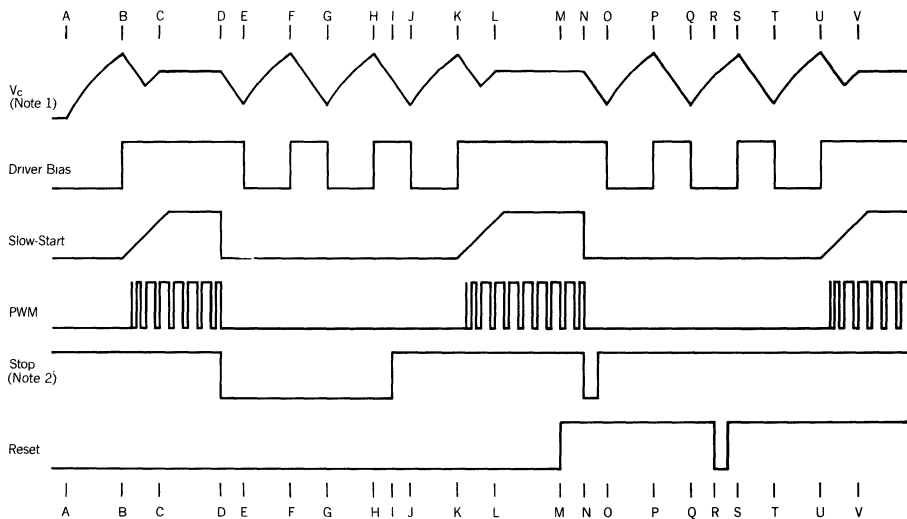
UC1840 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR (A)



UC1840 CONTROLS A HIGH-CURRENT NON-ISOLATED BUCK REGULATOR (B)



UC1840 POWER SEQUENCING FUNCTIONS



Notes: 1. V_c represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, V_{IN} , for the UC1840.
2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

UC1840 POWER SEQUENCING FUNCTIONS

TIME	EVENT
A	Initial turn-on, V_c rises with light load
B	Start threshold. Driver Bias loads V_c
C	Operating PWM regulates V_c
D	Stop input sets Error Latch turning off PWM
E	UV low threshold, Error Latch remains set
F	Start turns on Driver Bias but Error Latch still set
G } H }	V_c and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P } Q }	V_c and Driver Bias recycle with no turn-on.
R	Reset Latch set is set with momentary Reset signal
S	V_c must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

LINEAR INTEGRATED CIRCUITS

Off-Line Current Mode PWM Controller

UC1842
UC2842
UC3842

FEATURES

- Optimized for off-line control
- Low start up current (<1mA)
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with 6V hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500kHz operation

DESCRIPTION

The UC1842 family of control ICs provides in an eight pin mini-dip the necessary features to implement off-line, fixed frequency current mode control schemes with a minimal external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built in under-voltage lockout and current limiting. Other features include fully latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

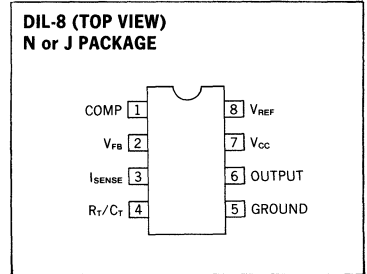
These devices feature a totem pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N Channel power devices, the output is low in the OFF state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

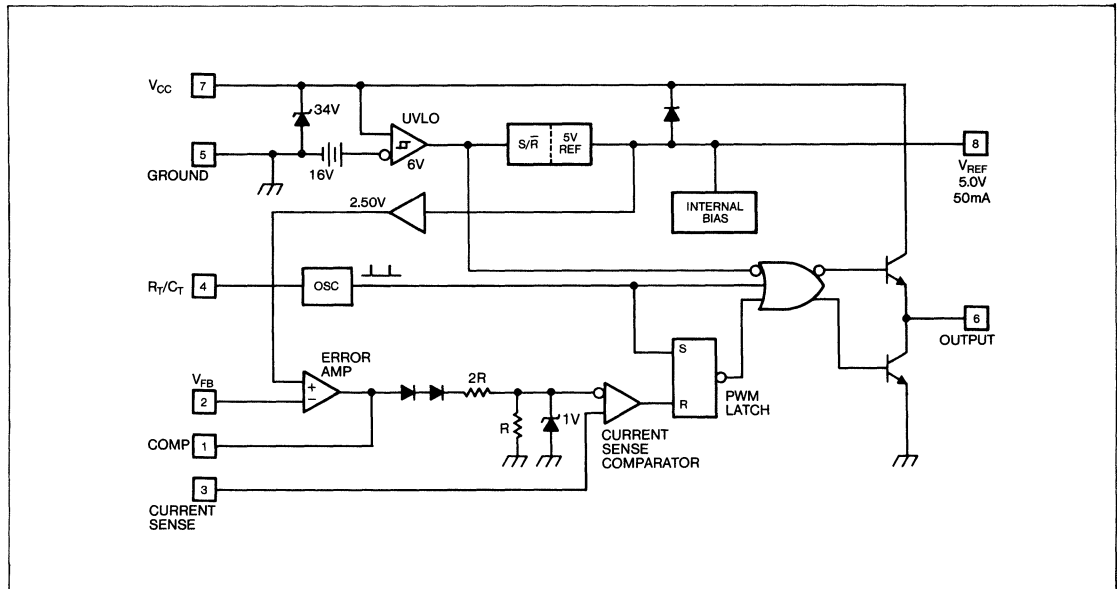
Supply Voltage ($I_{CC} < 30mA$)	Self Limiting
Supply Voltage (Low Impedance Source)	30V
Output Current	$\pm 1A$
Output Energy (Capacitive Load)	5 μ J
Analog Inputs (Pin 2, Pin 3)	-0.3V to V_{CC}
Error Amp Output Sink Current	10mA
Power Dissipation at $T_A \leq 70^\circ C$	1W
Derate 12.5mW/ $^\circ C$ for $T_A > 70^\circ C$	
Storage Temperature Range	-65 $^\circ C$ to +150 $^\circ C$
Lead Temperature (Soldering, 10 Seconds)	300 $^\circ C$

Note: 1. All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125^\circ\text{C}$ for UC1842; $-25 \leq T_A \leq 85^\circ\text{C}$ for UC2842; $0 \leq T_A \leq 70^\circ\text{C}$ for UC3842; $V_{CC} = 15\text{V}$ (Note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$.)

3

PARAMETER	TEST CONDITIONS	UC1842 UC2842			UC3842			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	$T_j = 25^\circ\text{C}$, $I_o = 1\text{mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{V}$		6	20		6	20	mV
Load Regulation	$1 \leq I_o \leq 20\text{mA}$		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_j = 25^\circ\text{C}$ (Note 2)		50			50		μV
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	$T_A = 25^\circ\text{C}$		-100	-130		-100	-130	mA
Oscillator Section								
Initial Accuracy	$T_j = 25^\circ\text{C}$	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN 4}$ peak to peak		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN 1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	$2 \leq V_o \leq 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN 2} = 2.7\text{V}$, $V_{PIN 1} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{PIN 2} = 2.3\text{V}$, $V_{PIN 1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
$V_{OUT High}$	$V_{PIN 2} = 2.3\text{V}$, $R_L = 15\text{K}$ to ground	5	6		5	6		V
$V_{OUT Low}$	$V_{PIN 2} = 2.7\text{V}$, $R_L = 15\text{K}$ to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN 1} = 5\text{V}$ (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	$T_j = 25^\circ$ (Note 2)		200	400		200	400	ns
Output Section								
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		1.5	2.2		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12	13.5		12	13.5		V
Rise Time	$T_j = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
Fall Time	$T_j = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns

- Notes:** 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN 2} = 0$.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN 1}}{\Delta V_{PIN 3}}; 0 \leq V_{PIN 3} \leq 0.8\text{V}.$$

5. Adjust V_{CC} above the start threshold before setting at 15V.

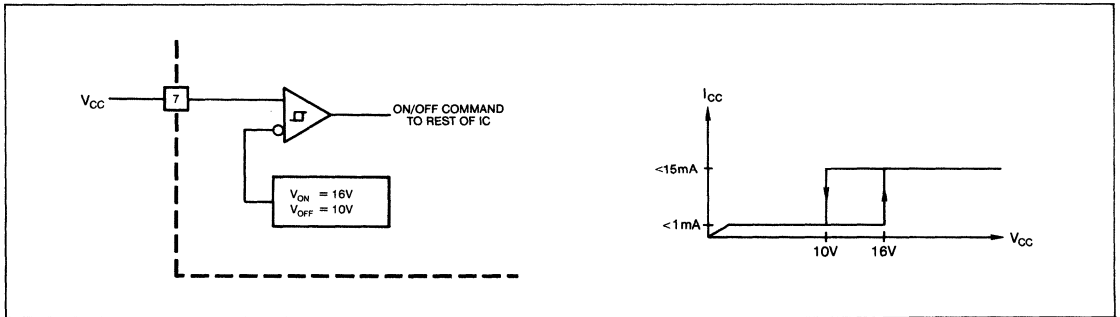
ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125^\circ\text{C}$ for UC1842; $-25 \leq T_A \leq 85^\circ\text{C}$ for UC2842; $0 \leq T_A \leq 70^\circ\text{C}$ for UC3842; $V_{CC} = 15\text{V}$ (Note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$.)

PARAMETER	TEST CONDITIONS	UC1842 UC2842			UC3842			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold		15	16	17	14.5	16	17.5	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10	11.5	V
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3} = 0\text{V}$		11	15		11	15	mA
V_{CC} Zener Voltage	$I_{CC} = 25\text{mA}$		34			34		V

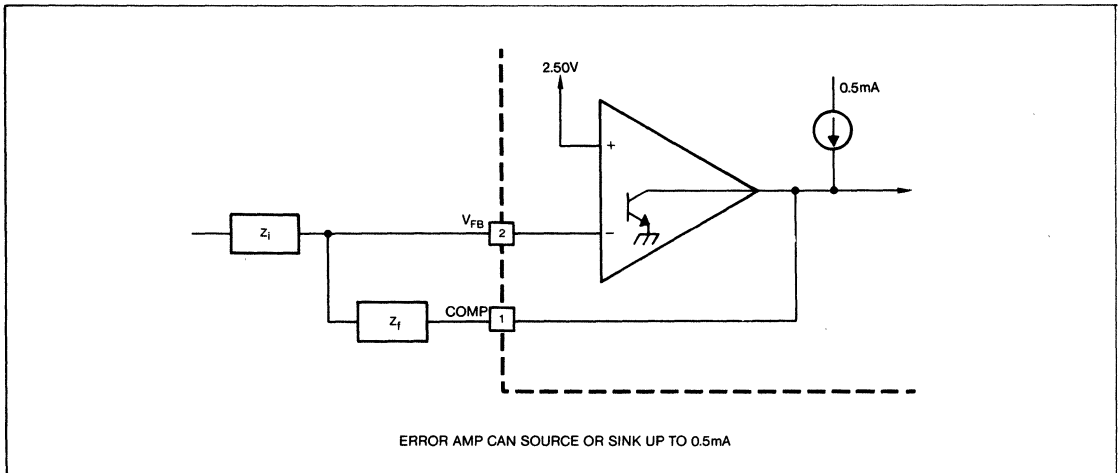
- Notes:**
2. These parameters, although guaranteed, are not 100% tested in production.
 3. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
 4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; 0 \leq V_{PIN\ 3} \leq 0.8\text{V}.$$
 5. Adjust V_{CC} above the start threshold before setting at 15V.

UNDER-VOLTAGE LOCKOUT

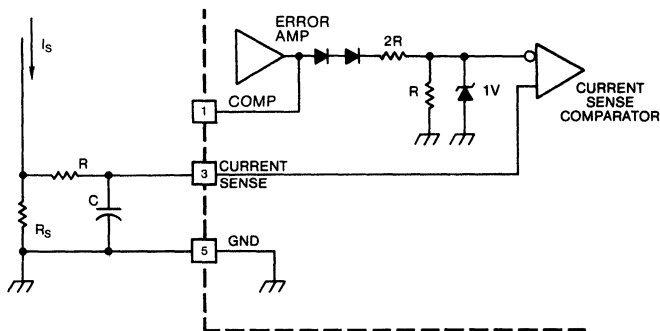


ERROR AMP CONFIGURATION



CURRENT SENSE CIRCUIT

3

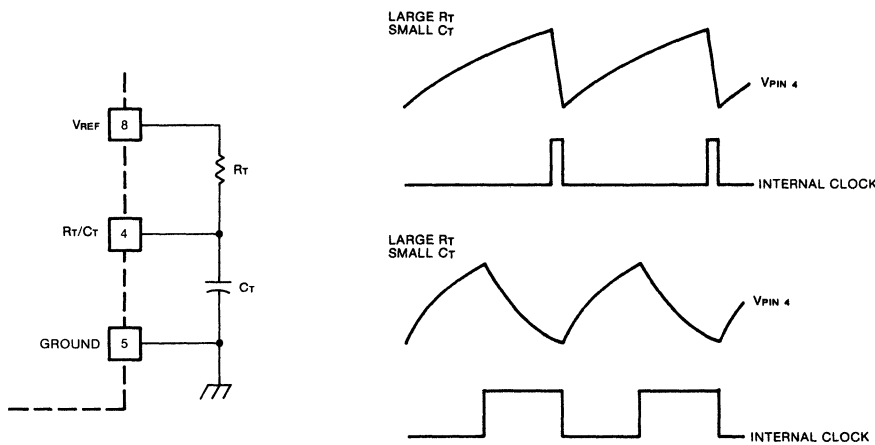


PEAK CURRENT (I_s) IS DETERMINED BY THE FORMULA:

$$I_{smax} \approx \frac{1.0V}{R_s}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

OSCILLATOR WAVEFORMS AND MAXIMUM DUTY CYCLE



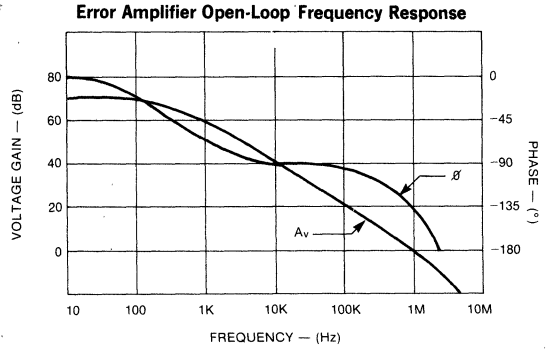
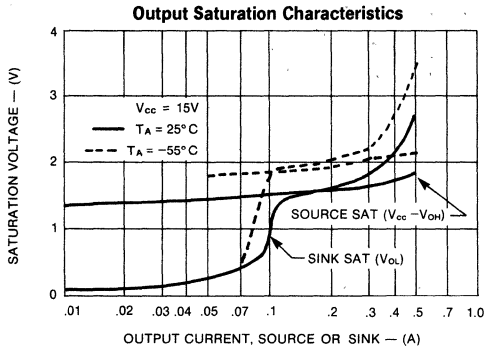
Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$$t_c \approx 0.55 R_T C_T$$

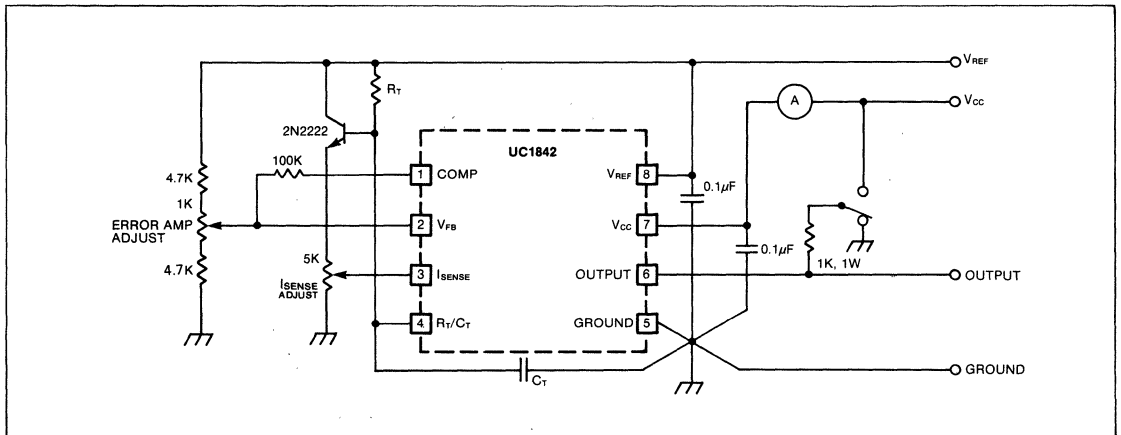
$$t_d \approx R_T C_T \ln \left(\frac{6.3 R_T - 2.7}{6.3 R_T - 4} \right) \quad (R_T \text{ in } K\Omega)$$

Frequency, then, is: $f = (t_c + t_d)^{-1}$.

$$\text{For } R_T > 5k \quad f \approx \frac{1.8}{R_T C_T}$$



OPEN-LOOP LABORATORY TEST FIXTURE

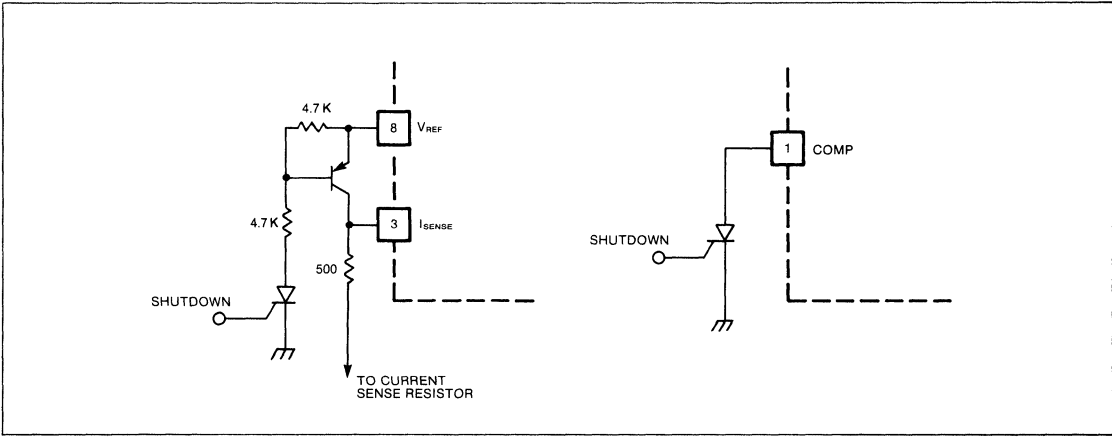


High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUTDOWN TECHNIQUES

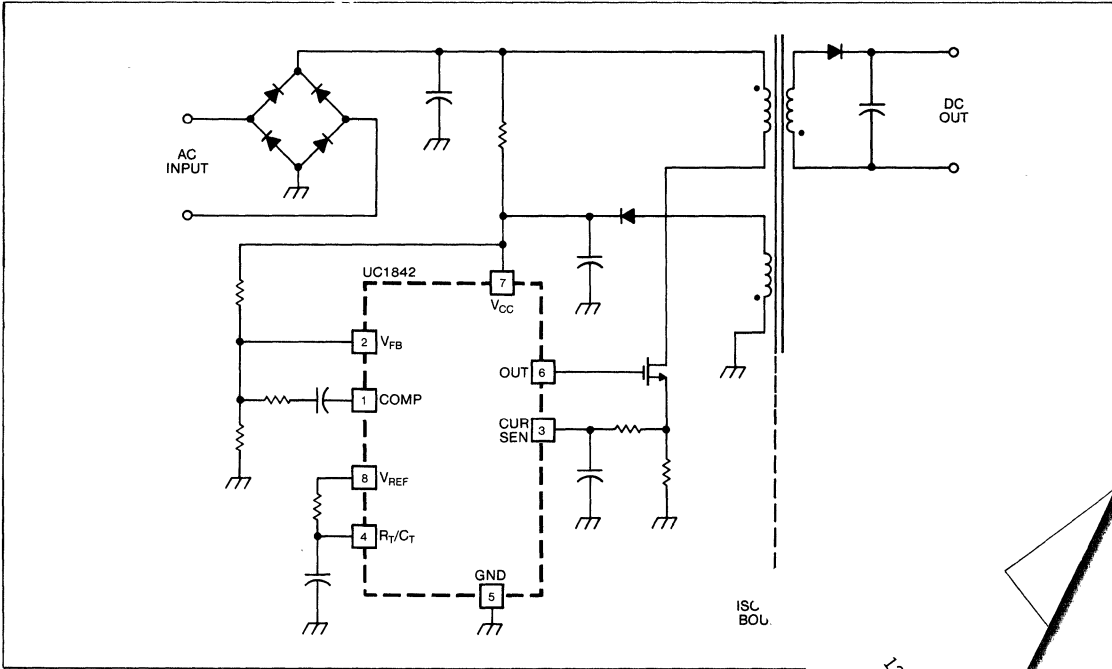
3



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next

clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In the examples shown, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed allowing the SCR to reset.

OFF-LINE FLYBACK REGULATOR



LINEAR INTEGRATED CIRCUITS

Current Mode PWM Controller

UC1846 UC1847
 UC2846 UC2847
 UC3846 UC3847

FEATURES

- Automatic feed forward compensation
- Programmable pulse by pulse current limiting
- Automatic symmetry correction in push-pull configuration
- Enhanced load response characteristics
- Parallel operation capability for modular power systems
- Differential current sense amplifier with wide common mode range
- Double pulse suppression
- 200mA totem-pole outputs
- $\pm 1\%$ bandgap reference
- Under-voltage lockout
- Soft start capability
- Shutdown terminal
- 500kHz operation

DESCRIPTION

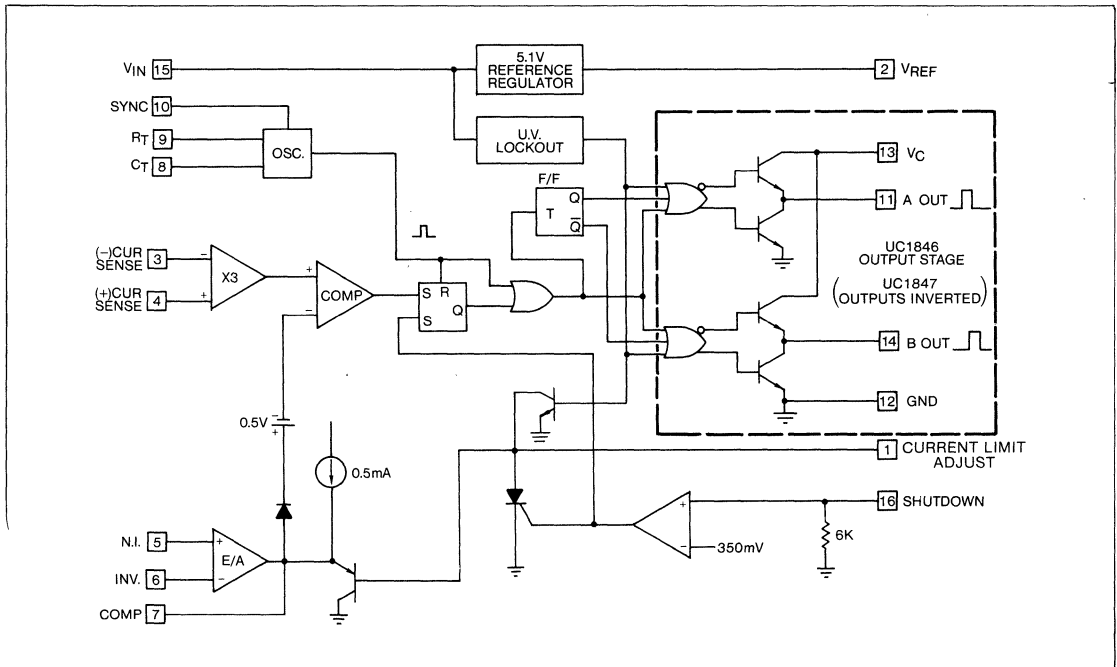
The UC1846/1847 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadtime adjust capability, and a $\pm 1\%$ trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM

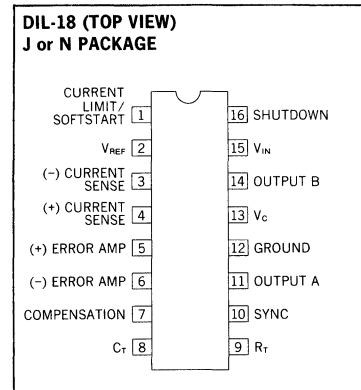


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15)	+40V
Collector Supply Voltage (Pin 13)	+40V
Output Current, Source or Sink (Pins 11, 14)	500mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	-0.3V to +V _{IN}
Reference Output Current (Pin 2)	-30mA
Sync Output Current (Pin 10)	-5mA
Error Amplifier Output Current (Pin 7)	-5mA
Soft Start Sink Current (Pin 1)	50mA
Oscillator Charging Current (Pin 9)	5mA
Power Dissipation at T _A = 25°C	1000mW
Derate at 10mW/°C for T _A above 50°C	
Power Dissipation at T _C = 25°C	2000mW
Derate at 16mW/°C for T _C above 25°C	
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

Note: 1. All voltages are with respect to Ground, Pin 13.
 Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for UC1846/UC1847; -25°C to +85°C for the UC2846/UC2847; and 0°C to +70°C for the UC3846/UC3847; V_{IN} = 15V, R_T = 10k, C_T = 4.7nF)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T _I = 25°C, I _o = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V _{IN} = 8 to 40V		5	20		5	20	mV
Load Regulation	I _L = 1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T _I = 25°C (Note 2)		100			100		μV
Long Term Stability	T _I = 125°C, 1000Hrs., (Note 2)		5			5		mV
Short Circuit Output Current	V _{REF} = 0V	-10	-45		-10	-45		mA
Oscillator Section								
Initial Accuracy	T _I = 25°C	39	43	47	39	43	47	kHz
Voltage Stability	V _{IN} = 8 to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			3	2.5		3	2.5	V
Sync Input High Level	Pin 8 = 0V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0V			2.5			2.5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	μA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V _{IN} = 8 to 40V	0		V _{IN} -2V	0		V _{IN} -2V	V
Open Loop Voltage Gain	ΔV _O = 1.2 to 3V, V _{CM} = 2V	80	105		80	105		dB
Unity Gain Bandwidth	T _I = 25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V _{CM} = 0 to 38V, V _{IN} = 40V	75	100		75	100		dB
PSRR	V _{IN} = 8 to 40V	80	105		80	105		dB
Output Sink Current (7)	V _{ID} = -15mV to -5V, V _{PIN 7} = 1.2V		2	6		2	6	mA
Output Source Current (7)	V _{ID} = 15mV to 5V, V _{PIN 7} = 2.5V	-0.4	-0.5		-0.4	-0.5		mA

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for UC1846/UC1847; -25°C to $+85^\circ\text{C}$ for the UC2846/UC2847; and 0°C to $+70^\circ\text{C}$ for the UC3846/UC3847; $V_{IN} = 15\text{V}$, $R_T = 10\text{k}\Omega$, $C_T = 4.7\text{nF}$)

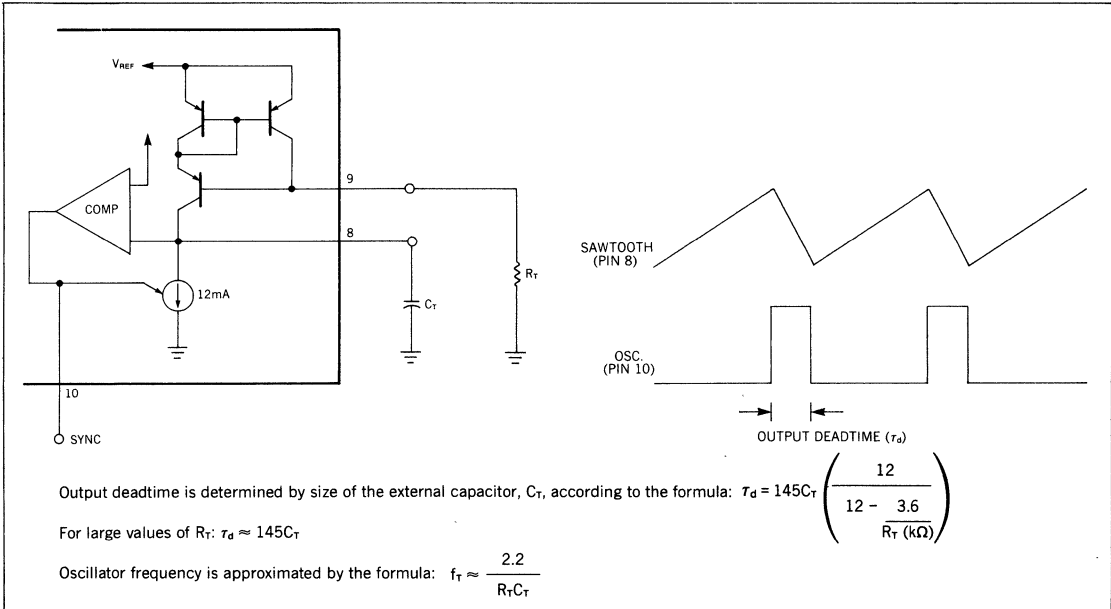
PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amp Section (continued)								
High Level Output Voltage	$R_L = (\text{Pin } 7) 15\text{k}\Omega$	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	$R_L = (\text{Pin } 7) 15\text{k}\Omega$		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{\text{Pin } 3} = 0\text{V}$, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{\text{Pin } 4} - V_{\text{Pin } 3}$)	Pin 1 Open (Note 3) $R_L (\text{Pin } 7) = 15\text{k}\Omega$	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{\text{Pin } 1} = 0.5\text{V}$ Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	$V_{\text{CM}} = 1$ to 12V	60	83		60	83		dB
PSRR	$V_{\text{IN}} = 8$ to 40V	60	84		60	84		dB
Input Bias Current	$V_{\text{Pin } 1} = 0.5\text{V}$, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	μA
Input Offset Current	$V_{\text{Pin } 1} = 0.5\text{V}$, Pin 7 Open (Note 3)		0.08	1		0.08	1	μA
Input Common Mode Range		0		$V_{\text{IN}} - 3$	0		$V_{\text{IN}} - 3$	V
Delay to Outputs	$T_J = 25^\circ\text{C}$, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{\text{Pin } 3} = 0\text{V}$, $V_{\text{Pin } 4} = 0\text{V}$, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{\text{Pin } 5} = V_{\text{REF}}$, $V_{\text{Pin } 6} = 0\text{V}$		-10	-30		-10	-30	μA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{\text{Pin } 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching Current ($I_{\text{Pin } 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$T_J = 25^\circ\text{C}$ (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_C = 40\text{V}$ (Note 5)			200			200	μA
Output Low Level	$I_{\text{SINK}} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{\text{SINK}} = 100\text{mA}$		0.4	2.1		0.4	2.1	
Output High Level	$I_{\text{SOURCE}} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{\text{SOURCE}} = 100\text{mA}$	12	13.5		12	13.5		
Rise Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
Fall Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		
Total Standby Current								
Supply Current			17	21		17	21	mA

Notes:

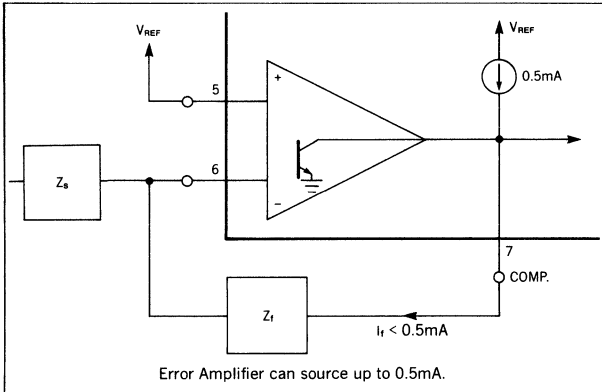
- These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
- Parameter measured at trip point of latch with $V_{\text{Pin } 5} = V_{\text{REF}}$, $V_{\text{Pin } 6} = 0\text{V}$.
- Amplifier gain defined as: $G = \frac{\Delta V_{\text{Pin } 7}}{\Delta V_{\text{Pin } 4}}$; $\Delta V_{\text{Pin } 4} = 0$ to 1.0V
- Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
- Current into Pin 1 guaranteed to latch circuit in shutdown state.
- Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

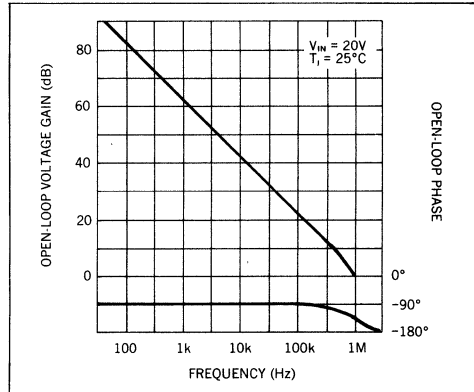
Oscillator Circuit



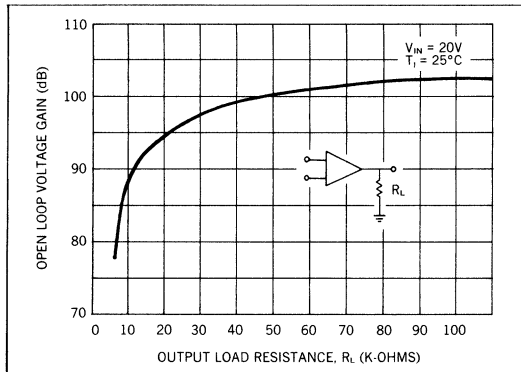
Error Amp Output Configuration



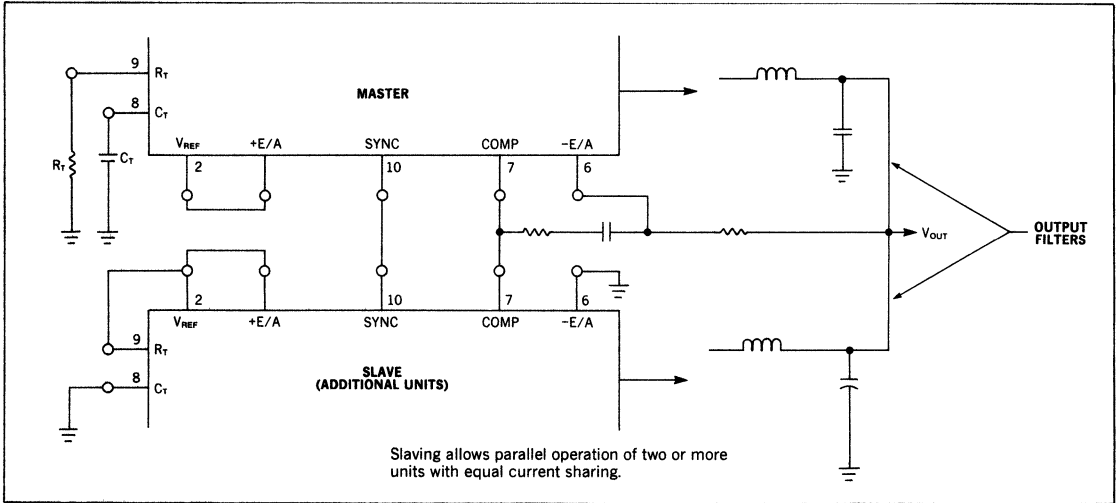
Error Amp Gain and Phase vs Frequency



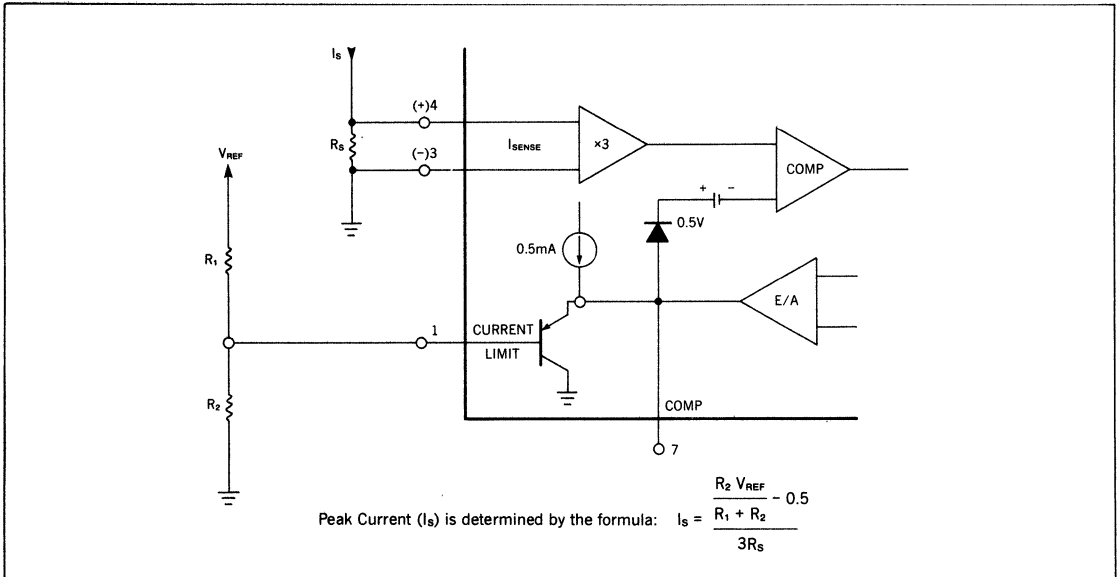
Error Amp Open-Loop D.C. Gain vs Load Resistance



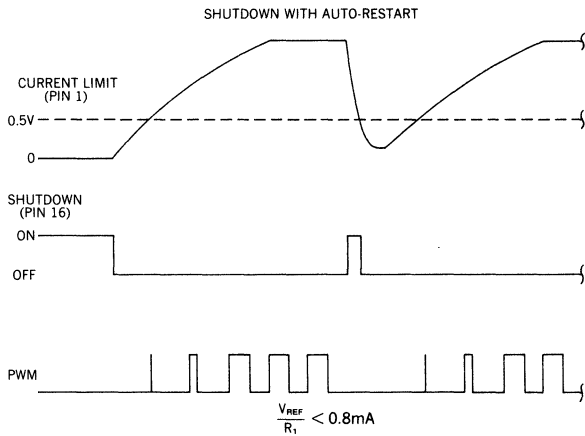
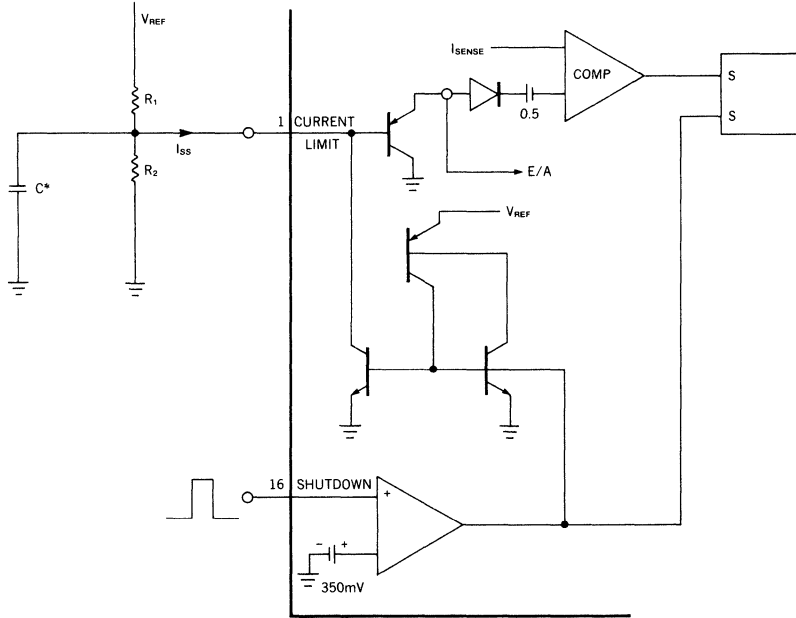
Parallel Operation



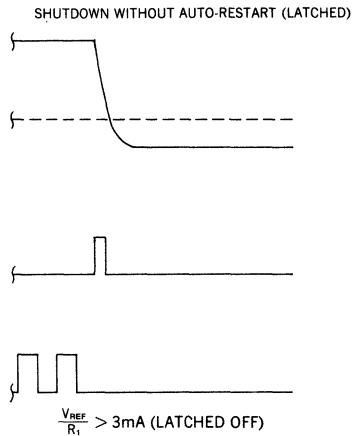
Pulse by Pulse Current Limiting



Soft Start and Shutdown/Restart Functions

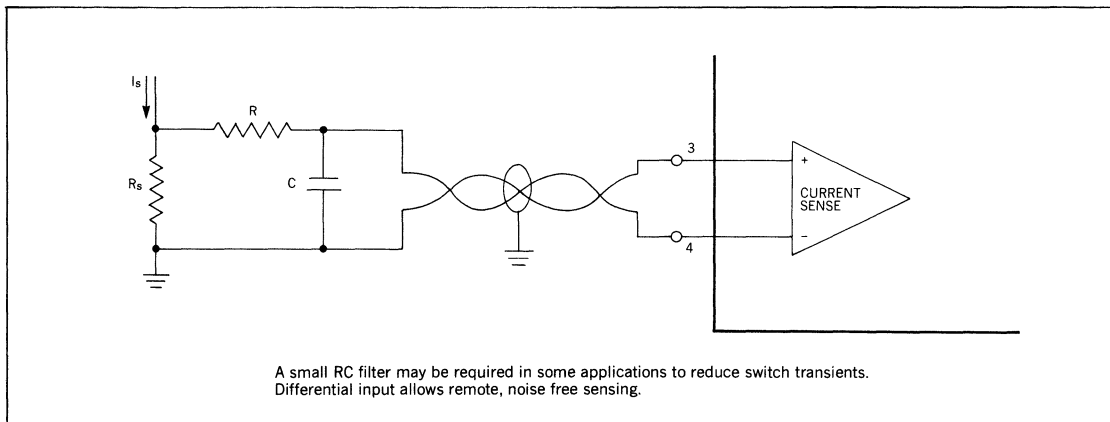


If $\frac{V_{REF}}{R_1} < 0.8mA$, the shutdown latch will commutate when $I_{SS} = 0.8mA$ and a restart cycle will be initiated.

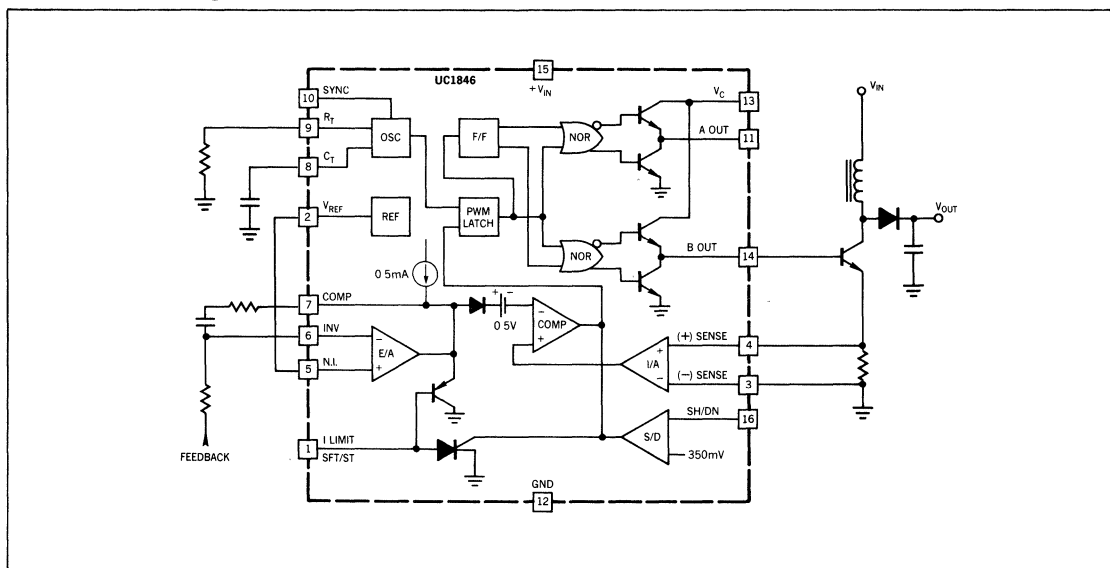


If $\frac{V_{REF}}{R_1} > 3mA$, the device will latch off until power is recycled.

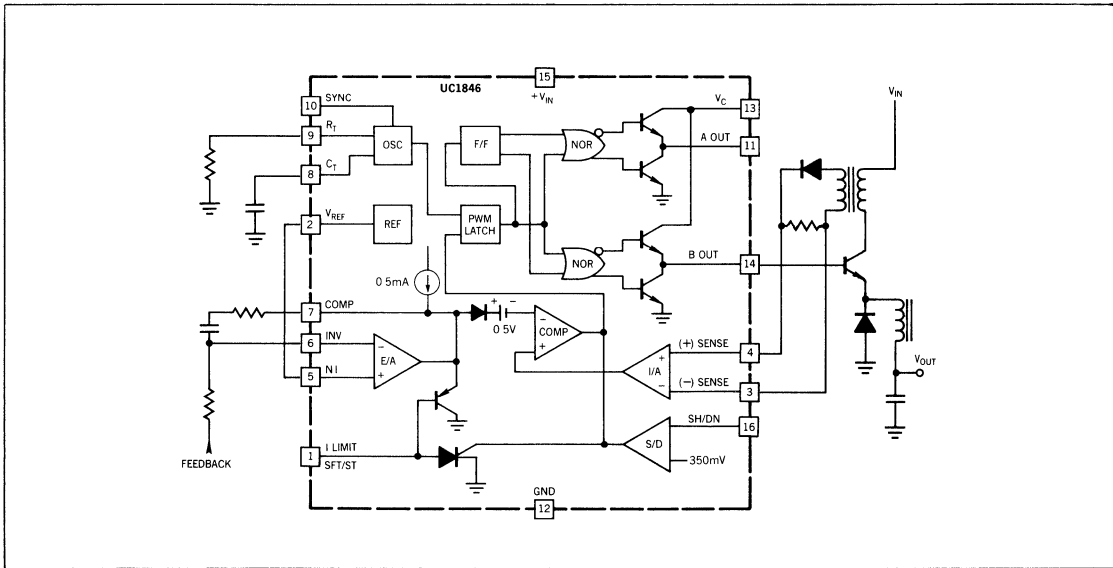
Current Sense Amp Connections



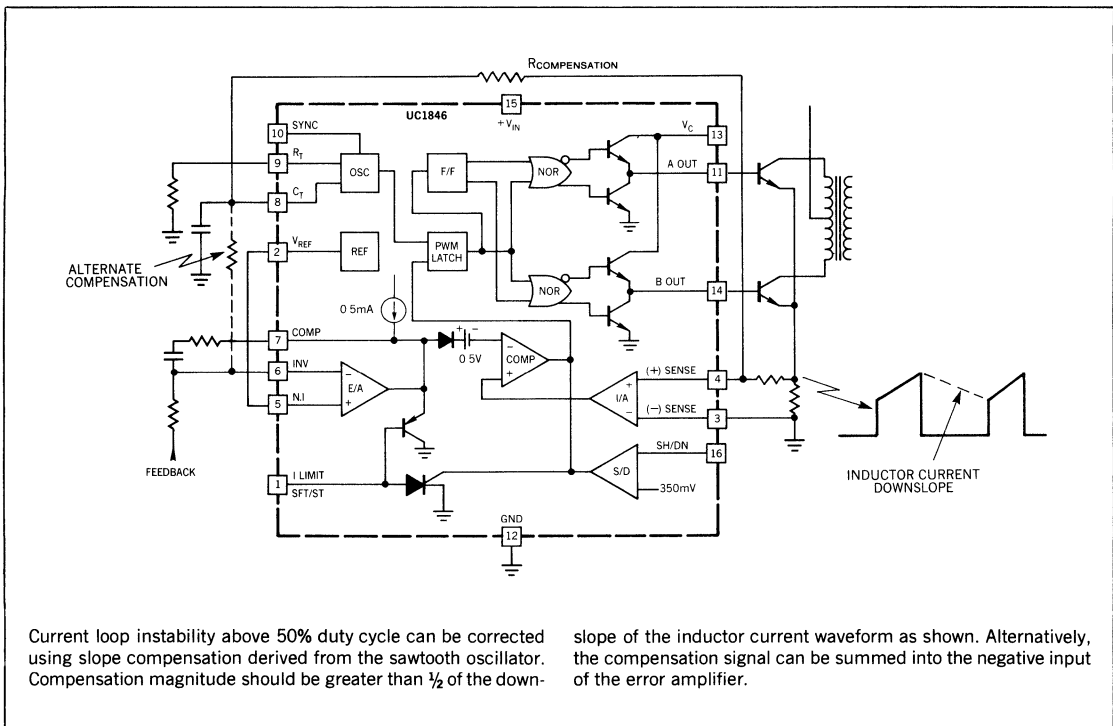
Single Ended Boost Configuration



Buck Converter with Current Sense Winding



Push/Pull Converter with Slope Compensation



LINEAR INTEGRATED CIRCUITS

Isolated Feedback Generator

UC1901
UC2901
UC3901

FEATURES

- An amplitude-modulation system for transformer coupling an isolated feedback error signal
- Low-cost alternative to optical couplers
- Internal 1% reference and error amplifier
- Internal carrier oscillator usable to 5MHz
- Modulator synchronizable to an external clock
- Loop status monitor

DESCRIPTION

The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within $\pm 10\%$ of the reference.

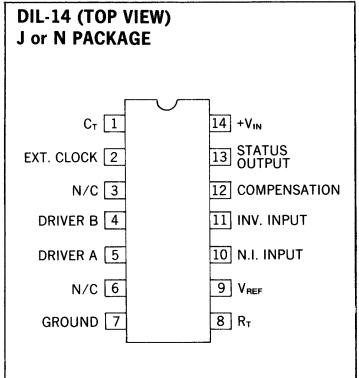
Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

ABSOLUTE MAXIMUM RATINGS (Note 1)

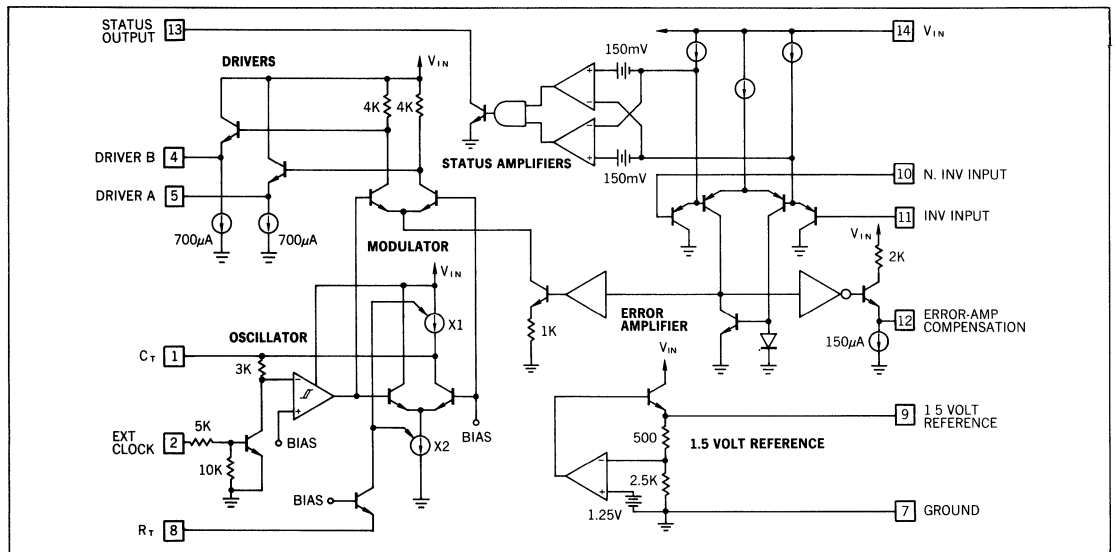
Input Supply Voltage, V_{IN}	40V
Reference Output Current	-10mA
Driver Output Currents	-35mA
Status Indicator Voltage	40V
Status Indicator Current	20mA
Ext. Clock Input	40V
Error Amplifier Inputs	-0.5V to +35V
Power Dissipation at $T_A = 25^\circ\text{C}$	
Derate at $10\text{mW}/^\circ\text{C}$ above $T_A = 50^\circ\text{C}$	1000mW
Power Dissipation at $T_C = 25^\circ\text{C}$	
Derate at $16\text{mW}/^\circ\text{C}$ above $T_A = 25^\circ\text{C}$	2000mW
Thermal Resistance, Junction to Ambient	$100^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$60^\circ\text{C}/\text{W}$
Operating Junction Temperature	-55°C to $+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: Voltages are referenced to ground, Pin 7.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM



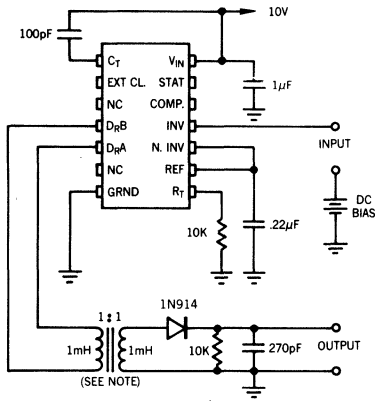
UC1901 SIMPLIFIED SCHEMATIC



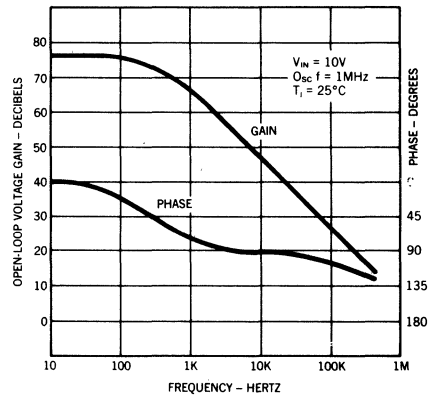
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1901; -25°C to $+85^{\circ}\text{C}$ for the UC2901; and 0°C to $+70^{\circ}\text{C}$ for the UC3901; $V_{IN} = 10\text{V}$, $R_T = 10\text{k}\Omega$, $C_T = 820\text{pF}$)

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	$T_j = 25^{\circ}\text{C}$	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \leq T_j \leq T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	$V_{IN} = 4.5$ to 35V		2	10		2	15	mV
Load Regulation	$I_{OUT} = 0$ to 5mA		4	10		4	15	mV
Short Circuit Current	$T_j = 25^{\circ}\text{C}$		-35	-45		-35	-45	mA
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	$V_{CM} = 1.5\text{V}$		1	4		1	8	mV
Input Bias Current	$V_{CM} = 1.5\text{V}$		-1	-3		-1	-6	μA
Input Offset Current	$V_{CM} = 1.5\text{V}$		0.1	1		0.1	2	μA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	$V_{CM} = 0.5$ to 7.5V	60	80		60	80		dB
PSRR	$V_{IN} = 5$ to 25V	80	100		80	100		dB
Output Swing, ΔV_o		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		μA
Maximum Source Current		-2	-3		-2	-3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		$\text{V}/\mu\text{s}$
Modulator/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		± 1.6	± 2.8		± 1.6	± 2.8		V
Driver Sink Current		500	700		500	700		μA
Driver Source Current		-15	-35		-15	-35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	$T_j = 25^{\circ}\text{C}$	140	150	160	130	150	170	kHz
	$T_{MIN} \leq T_j \leq T_{MAX}$	130		170	120		180	
Line Sensitivity	$V_{IN} = 5$ to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	$R_T = 10\text{K}$, $C_T = 10\text{pF}$		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, $V_{CM} = 1.5\text{V}$	± 135	± 150	± 165	± 130	± 150	± 170	mV
Saturation Voltage	E/A Δ Input = 0V , $I_{SINK} = 1.6\text{mA}$			0.45			0.45	V
Max. Output Current	Pin 13 = 3V , E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V , E/A Δ Input = 0.2V		.05	1		.05	5	μA
Supply Current	$V_{IN} = 35\text{V}$		5	8		5	10	mA

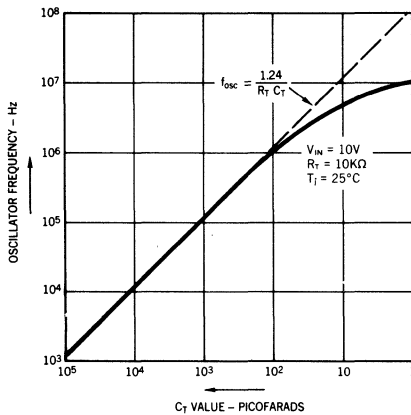
Transformer Coupled Open Loop Transfer Function



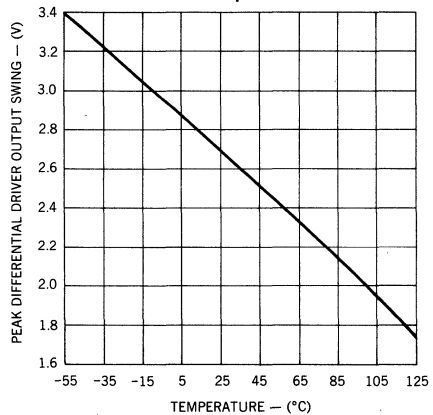
Transformer Data N1 = N2 = 20T AWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O D toroid
Carrier Frequency = 1MHz



Oscillator Frequency



Typical Driver Output Swing vs Temperature



APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

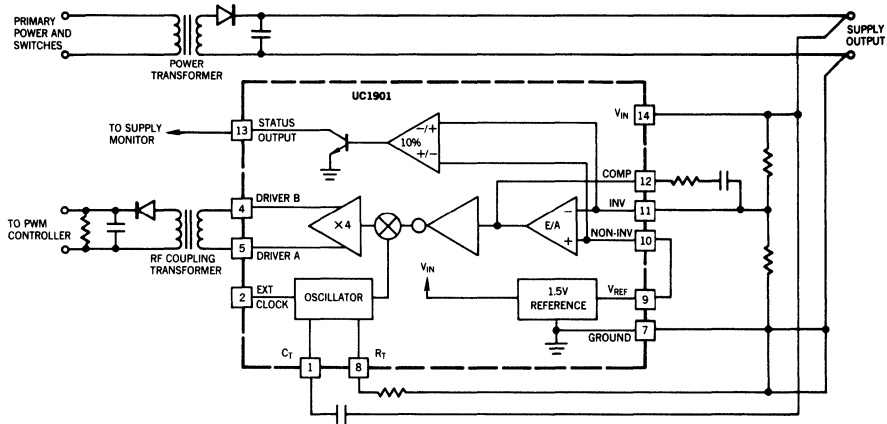
The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator

the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_T, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is no clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

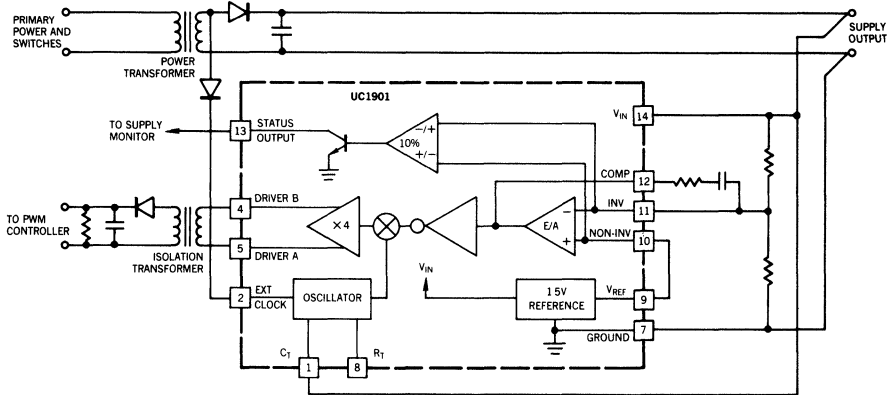
The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700μA, can be increased by adding resistors to ground at the driver outputs.

TYPICAL APPLICATIONS

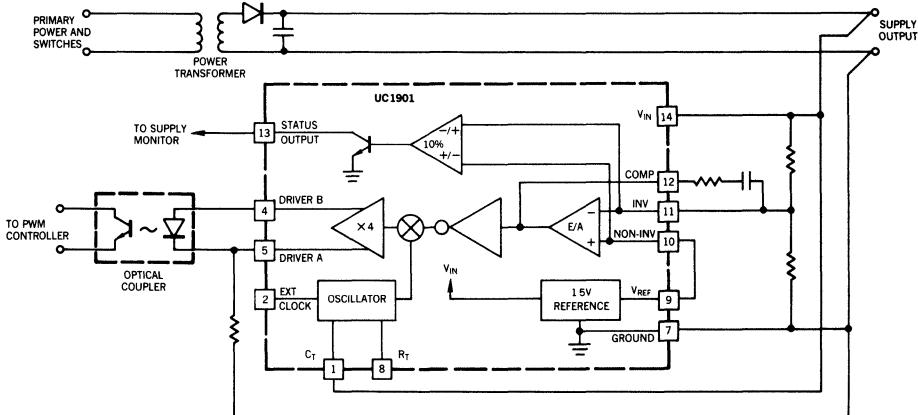
R.F. Transformer Coupled Feedback



Feedback Coupled at Switching Frequency



Optically Coupled DC Feedback



LINEAR INTEGRATED CIRCUITS

Quad Supply and Line Monitor

UC1903
UC2903
UC3903

FEATURES

- Inputs for monitoring up to four separate supply voltage levels
- Internal inverter for sensing a negative supply voltage
- Line/switcher sense input for early power source failure warning
- Programmable under- and over-voltage fault thresholds with proportional hysteresis
- A precision 2.5V reference
- General purpose op-amp for auxiliary use
- Three high current, 40mA, open-collector outputs indicate over-voltage, under-voltage and power OK conditions
- Input supply under-voltage sensing and start-latch eliminate erroneous fault alerts during start-up
- 8-40V supply operation with 6mA stand-by current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

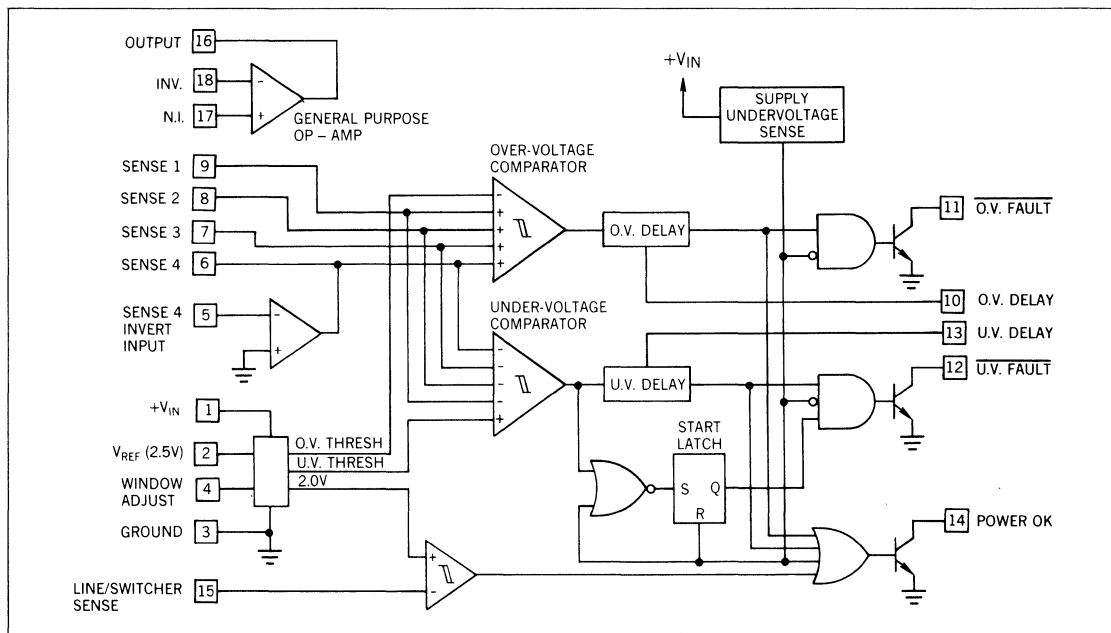
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 40mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8-40V input supply range and require a typical stand-by current of only 6mA.

BLOCK DIAGRAM

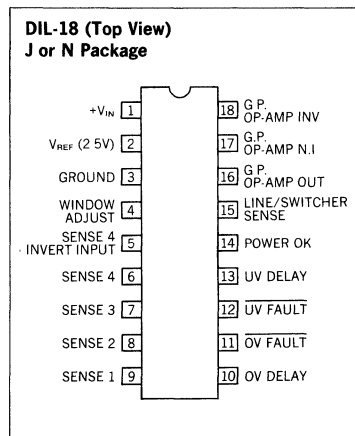


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+V _{IN})	+40V
Open Collector Output Voltages	+40V
Open Collector Output Currents	50mA
Sense 1-4 Input Voltages	-0.3V to +20V
Line/Switcher Sense Input Voltage	-0.3V to +40V
Op-Amp and Inverter Input Voltages	-0.3V to +40V
Op-Amp and Inverter Output Currents	-40mA
Window Adjust Voltage	0.0V to +10V
Delay Pin Voltages	0.0V to +5V
Reference Output Current	-40mA
Power Dissipation at T _A = 25°C	1000mW
Derate at 10mW/°C above T _A = 25°C	
Power Dissipation at T _C = 25°C	2000mW
Derate at 16mW/°C above T _C = 25°C	
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65° to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note: 1. Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

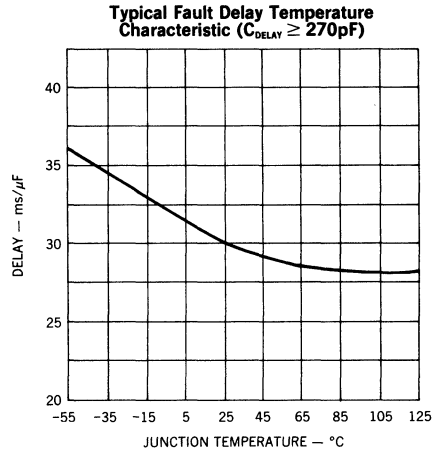
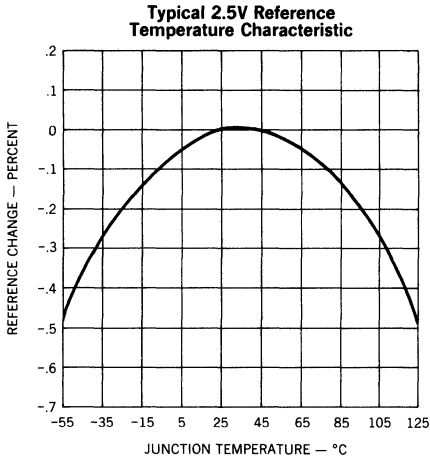
(Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1903; -25°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; +V_{IN} = 15V; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V; V_{PIN 4} = 1.0V.)

PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply								
Input Supply Current	No Faults	—	6	9	—	6	11	mA
	UV, OV and Line Fault	—	10	15	—	10	18	mA
Supply Under Voltage Threshold (V _{SUV})	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output		—	3.0	4.0	—	3.0	4.0	V
Reference								
Output Voltage (V _{REF})	T _J = 25°C	2.485	2.5	2.515	2.465	2.5	2.535	V
	Over Temperature	2.465	—	2.535	2.45	—	2.55	V
Load Regulation	I _L = 0 to 10mA	—	1	8	—	1	15	mV
Line Regulation	+V _{IN} = V _{SUV} + 0.1V to 40V	—	1	4	—	1	8	mV
Short Circuit Current	T _J = 25°C	—	40	—	—	40	—	mA
Fault Thresholds								
OV Threshold Adj.	Offset from V _{REF} as a function of V _{PIN4} Input = Low to High, .5V ≤ V _{PIN 4} ≤ 2.5V	.235	.25	.265	.225	.25	.275	V/V
UV Threshold Adj.	Offset from V _{REF} as a function of V _{PIN4} Input = High to Low, .5V ≤ V _{PIN 4} ≤ 2.5V	-.265	-.25	-.235	-.275	-.25	-.225	V/V
OV & UV Threshold Hyst.	.5V ≤ V _{PIN 4} ≤ 2.5V	15	20	28	10	20	35	mV/V
OV & UV Threshold Supply Sensitivity	+V _{IN} = V _{SUV} + 0.1V to 40V	—	.002	.01	—	.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	.5V ≤ V _{PIN 4} ≤ 2.5V	—	±1	±6	—	±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1903; -25°C to $+85^\circ\text{C}$ for the UC2903; and 0°C to $+70^\circ\text{C}$ for the UC3903; $+V_{IN} = 15\text{V}$; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V ; $V_{PIN\ 4} = 1.0\text{V}$.)

PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)	—	1	3	—	1	6	μA
	Input = 2.2V (Note 2)	—	-1	-3	—	-1	-6	μA
Line Sense Input Bias Current	Input = 2.3V (Note 2)	—	1	3	—	1	6	μA
OV and UV Fault Delay								
Charging Current		—	60	—	—	60	—	μA
Threshold Voltage	Delay Pin = Low to High	—	1.8	—	—	1.8	—	V
Threshold Hysteresis	$T_J = 25^\circ\text{C}$	—	300	—	—	300	—	mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/ μF
Fault Outputs (OV, UV, & Power OK)								
Maximum Current	$V_{OUT} = 2\text{V}$	40	70	—	40	70	—	mA
Saturation Voltage	$I_{OUT} = 12\text{mA}$	—	.25	.45	—	.25	.45	V
Leakage Current	$V_{OUT} = 40\text{V}$	—	3	50	—	3	100	μA
Sense 4 Inverter								
Input Offset Voltage		—	2	8	—	2	10	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Open Loop Gain		65	80	—	65	80	—	dB
PSRR	$+V_{IN} = 8$ to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/ μs
Short Circuit Current	$T_J = 25^\circ\text{C}$	—	40	—	—	40	—	mA
G.P. Op-Amp								
Input Offset Voltage		—	1	5	—	1	8	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Input Offset Current		—	.01	.5	—	.01	1.0	μA
Open Loop Gain		65	120	—	65	120	—	dB
CMRR	$V_{CM} = 0$ to $+V_{IN} - 2.0\text{V}$	65	100	—	65	100	—	dB
PSRR	$+V_{IN} = 8$ to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/ μs
Short Circuit Current	$T_J = 25^\circ\text{C}$	—	40	—	—	40	—	mA

Note: 2. These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.



OPERATION AND APPLICATION INFORMATION

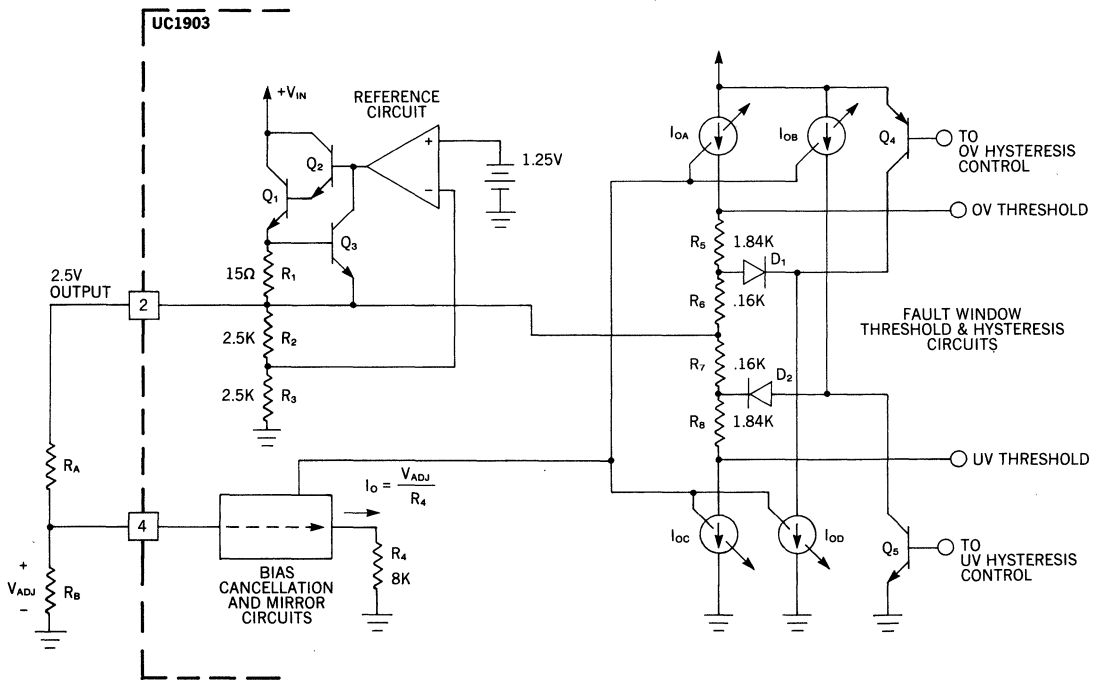


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION (continued)

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R₄, an 8K resistor. The resulting current is mirrored four times to generate current sources I_{0A}, I_{0B}, I_{0C}, and I_{0D}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q₃ and Q₄ are turned on. In combination with D₁ and D₂ this prevents I_{0B} and I_{0D} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to V_{REF} + I_{0A}(R₅ + R₆) and V_{REF} - I_{0C}(R₇ + R₈) respectively. The fault window can be expressed as:

$$(1) \quad 2.5V \pm \frac{V_{ADJ}}{4}$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

$$(2) \quad V_S \pm (10 \cdot V_{ADJ})\%$$

When a sense input moves outside the fault window given in equation (1), the appropriate hysteresis control signal turns off Q₄ or Q₅. For the under-voltage case, Q₅ is disabled and current source I_{0B} flows through D₂. The net current through R₇ becomes zero as I_{0B} cancels I_{0C}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q₄ turning off, allowing I_{0D} to cancel the current flow, I_{0A}, through R₆. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

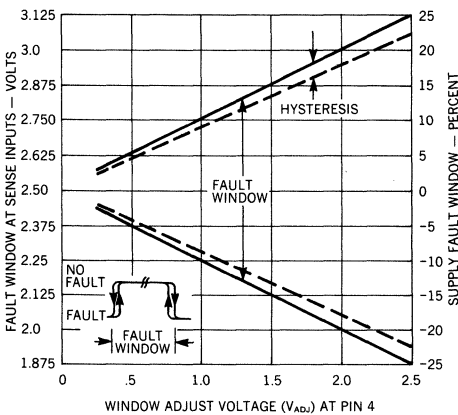


Figure 2. The fault window and threshold hysteresis scales as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

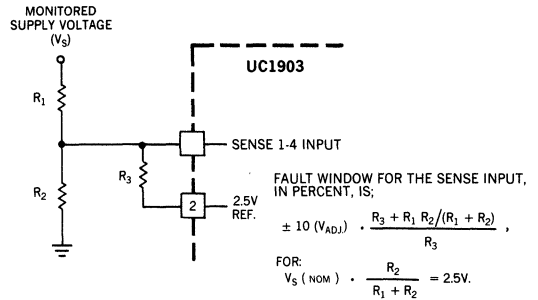


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

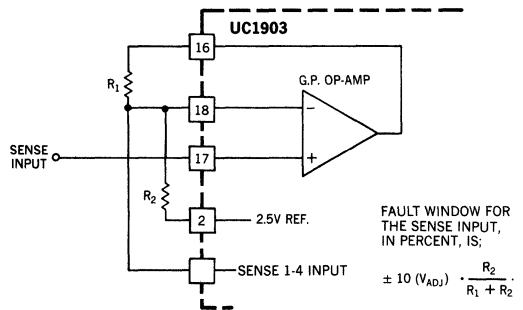


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability, ≥20mA, while the substrate device, Q₃, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

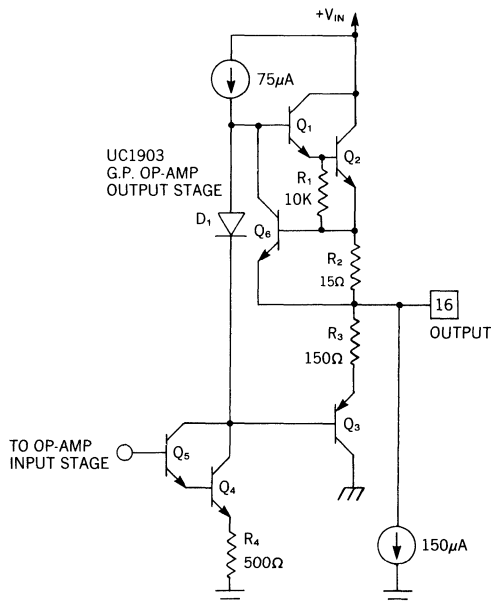


Figure 5. The G.P. op-amp on the UC1903 has a high source current ($\geq 20\text{mA}$) capability and enhanced transient sinking capability through substrate device Q_3 .

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of this inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.

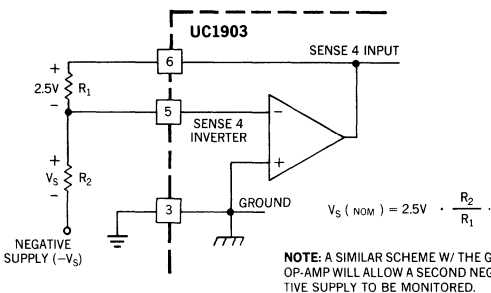


Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned-off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from

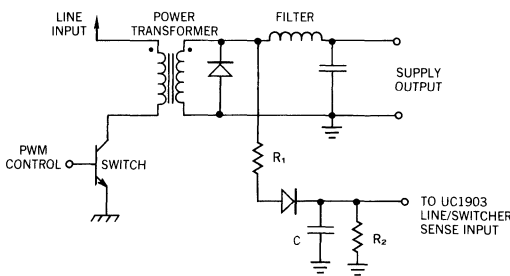


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{\text{OV}}$ and $\overline{\text{UV}}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2K resistor, R_1 , and zener diode, Z_1 , prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1 , is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above -0.3V . The same type of input protection exists at the line sense input, Pin 15, except a 5K series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal $60\mu\text{A}$ current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{\text{OV}}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

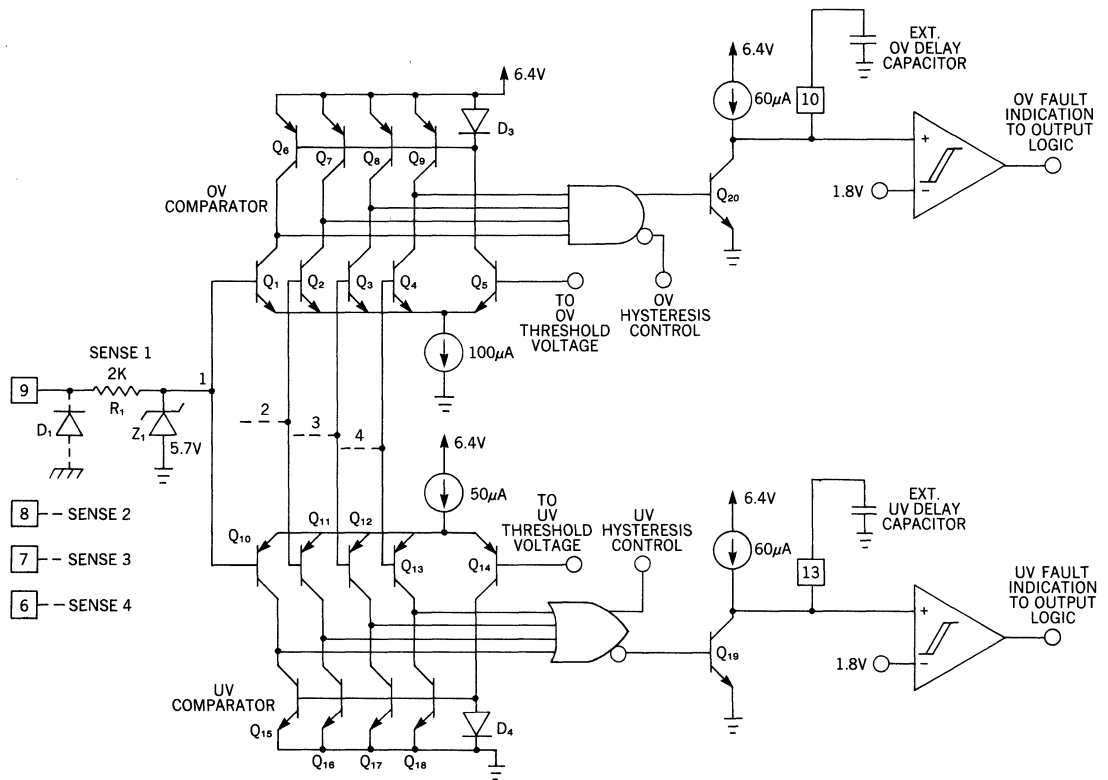


Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply ($+V_{IN}$) conditions. When the input supply voltage is below the supply under-voltage threshold the \overline{OV} and \overline{UV} fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With $+V_{IN}$ below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry

resets the start-latch. With the start-latch set, the \overline{UV} fault output will remain disabled as the input supply rises to its normal operating level (8-40V). The latch stays set until all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the \overline{UV} fault output will respond if any of the sense inputs drop below the under-voltage threshold.

LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Positive Regulators

UC7800
UC7800C
SERIES

3

FEATURES

- ±4% preset output voltage
- Complete specifications at 1A load
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe area compensation
- Available in TO-3 and TO-220 packages
- Output voltages of 5, 12 and 15V (For other voltages, please contact the factory)

DESCRIPTION

These three terminal monolithic positive voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. These units feature an on-chip trimming system to set the output voltages to within ±4% of nominal. Two companion series, the UC7800A and UC7800AC, offer tighter output tolerances, and improved line and load regulation characteristics.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35V
Power Dissipation	Internally limited
Operating Junction Temperature Range	
UC7800 SERIES	-55°C to +150°C
UC7800C SERIES	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
K (TO-3) package	300°C
T (TO-220) package	230°C
Power/Thermal Characteristics	

K (TO-3) Package T (TO-220) Package

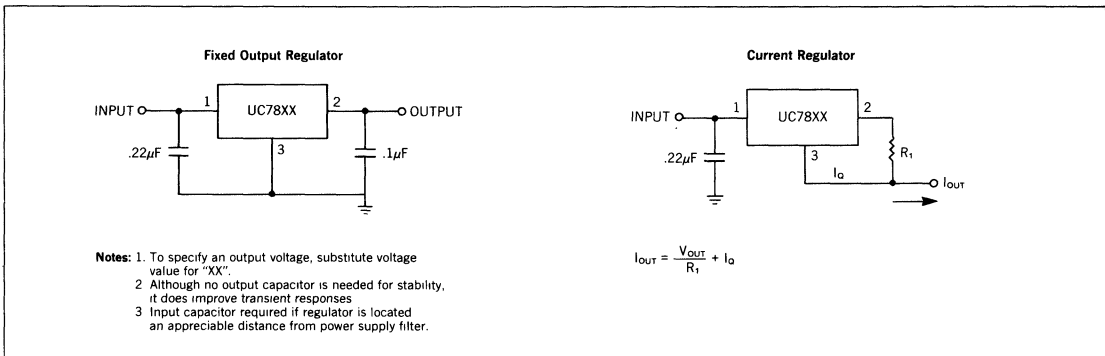
Rated Power @ 25°C

T_C	20W	15W
T_A	4.3W	2W

Thermal Resistance

θ_{JC}	3°C/W	3°C/W
θ_{JA}	35°C/W	60°C/W

TYPICAL APPLICATIONS



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7805			UC7805C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$	4.8		5.2	4.8		5.2	V
	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}, P_D \leq 15\text{W}$	4.8		5.2	4.77		5.23	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	4.75		5.25	4.75		5.25	V
Line Regulation	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}, I_o = 500\text{mA}$			25			35	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		10	50		10	50	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		20	26		20	40	mV
	$V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			50			50	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$.4			.4	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.5			.5	mA
	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}, I_o = 500\text{mA}$.8			.8	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			1.0			1.0	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, 8\text{V} \leq V_{IN} \leq 18\text{V}, I_o = 500\text{mA}$	63			63			dB
Output Noise Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$		40			40		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		2			2		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}$		2.1			2.1		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = 10\text{V}, I_o = 5\text{mA}$		-4			-4		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 5\text{mA}$		20			20		mV
Thermal Shutdown	$V_{IN} = 10\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7812			UC7812C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}, I_O = 1\text{A}$	11.52		12.48	11.52		12.48	V
	$T_J = 25^\circ\text{C}, 14.5\text{V} \leq V_{IN} \leq 27\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}, P_D \leq 15\text{W}$	11.52		12.48	11.46		12.54	v
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$	11.40		12.60	11.40		12.60	v
Line Regulation	$T_J = 25^\circ\text{C}, 14.5\text{V} \leq V_{IN} \leq 27\text{V}, I_O = 500\text{mA}$			60			84	mV
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$		20	120	20	120		mV
Load Regulation	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}, 5\text{mA} \leq I_O \leq 1.5\text{A}$		50	64	50	100		mV
	$V_{IN} = 19\text{V}, 5\text{mA} \leq I_O \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$			120		120		mV
Quiescent Current	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}, I_O = 1\text{A}$		4.5	7	4.5	7		mA
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$			6.5		6.5		mA
Quiescent Current Change	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}, 5\text{mA} \leq I_O \leq 1\text{A}$.4		.4		mA
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$.5		.5		mA
	$T_J = 25^\circ\text{C}, 14.5\text{V} \leq V_{IN} \leq 27\text{V}, I_O = 500\text{mA}$.8		.8		mA
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$			1.0		1.0		mA
Ripple Rejection	$T_J = 25^\circ\text{C}, 15\text{V} \leq V_{IN} \leq 25\text{V}, I_O = 500\text{mA}$	56			56			dB
Output Noise Voltage	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}, I_O = 5\text{mA}$		75		75			μV
Dropout Voltage	$T_J = 25^\circ\text{C}, I_O = 1\text{A}$		2		2			V
Short Circuit Current	$T_J = 25^\circ\text{C}, V_{IN} = 19\text{V}$		1.5		1.5			A
Peak Output Current	$T_J = 25^\circ\text{C}$		2.4		2.4			A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_J \leq T_{MAX}, V_{IN} = 19\text{V}, I_O = 5\text{mA}$		-8		-8			mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_J = 125^\circ\text{C}, V_{IN} = 19\text{V}, I_O = 5\text{mA}$		50		50			mV
Thermal Shutdown	$V_{IN} = 19\text{V}, I_O = 5\text{mA}$		175		175			$^\circ\text{C}$
	T_{MAX}		150		125			$^\circ\text{C}$
	T_{MIN}		-55		0			$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

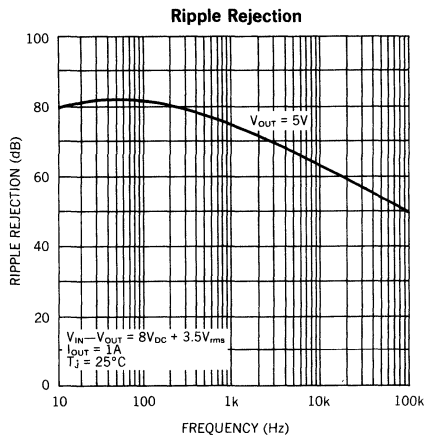
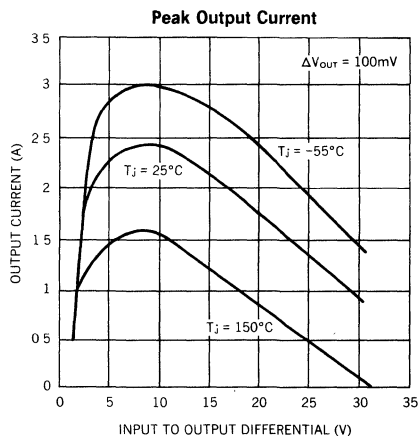
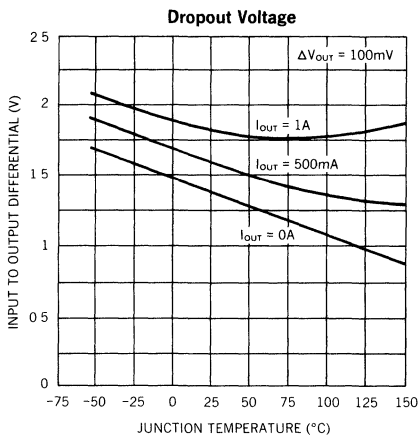
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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7815			UC7815C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 1\text{A}$	14.4		15.6	14.4		15.6	V
	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}, P_o \leq 15\text{W}$	14.4		15.6	14.3		15.7	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	14.25		15.75	14.25		15.75	V
Line Regulation	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}, I_o = 500\text{mA}$			75			100	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		22	150		22	150	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		50	80		50	120	mV
	$V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			150			150	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 1\text{A}$		4.5	7		4.5	7	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$.4			.4	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.5			.5	mA
	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}, I_o = 500\text{mA}$.8			.8	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			1.0			1.0	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, 18.5\text{V} \leq V_{IN} \leq 28.5\text{V}, I_o = 500\text{mA}$	54			54			dB
Output Noise Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		90			90		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		2			2		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}$		1.2			1.2		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		-1.0			-1.0		$\text{mV}/^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		60			60		mV
Thermal Shutdown	$V_{IN} = 23\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

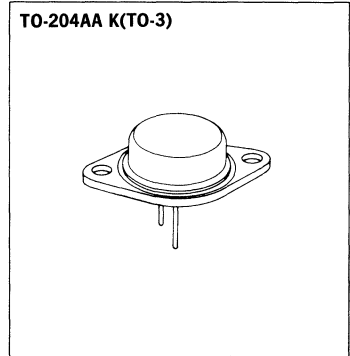
TYPICAL PERFORMANCE CHARACTERISTICS



MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

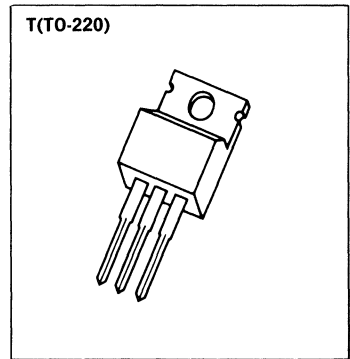
**UC7800 SERIES
UC7800C SERIES**

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.



UC7800C SERIES

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85



ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX	
	K(TO-3)	T(TO-220)
5V	UC7805K UC7805CK	— UC7805CT
12V	UC7812K UC7812CK	— UC7812CT
15V	UC7815K UC7815CK	— UC7815CT

LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Positive Regulators

Precision Version

UC7800A
UC7800AC
SERIES

3

FEATURES

- $\pm 1.0\%$ preset output voltage
- Complete specifications at 1A load
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe area compensation
- Available in TO-3 and TO-220 Packages
- Output voltages of 5, 12, and 15V (For other voltages, please contact the factory)
- Pinout identical to UC7800 series

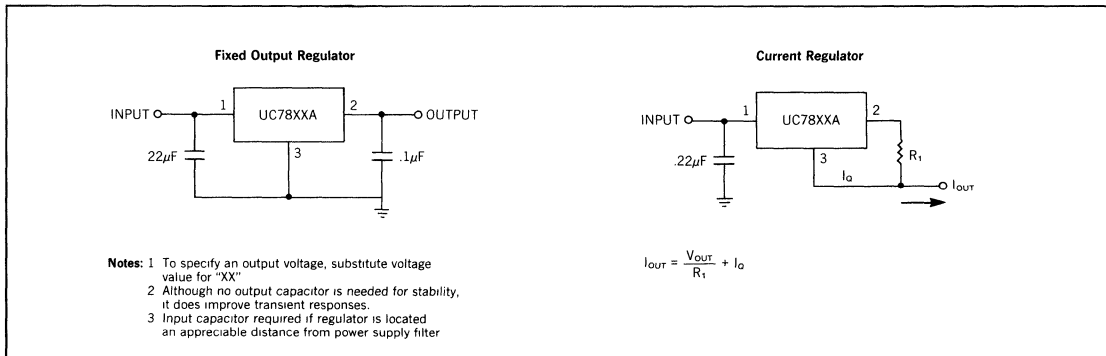
DESCRIPTION

These three terminal monolithic positive voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. These units feature an on-chip trimming system to set the output voltages to within $\pm 1.0\%$ of nominal. They also offer improved line and load regulation characteristics over the UC7800 series.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V	
Power Dissipation Internally limited	
Operating Junction Temperature Range		
UC7800A SERIES -55°C to $+150^{\circ}\text{C}$	
UC7800AC SERIES 0°C to $+125^{\circ}\text{C}$	
Storage Temperature Range -65°C to $+150^{\circ}\text{C}$	
Lead Temperature (Soldering, 10 seconds)		
K (TO-3) Package 300°C	
T (TO-220) Package 230°C	
Power/Thermal Characteristics	K (TO-3) Package	T (TO-220) Package
Rated Power @ 25°C		
T_c 20W 15W
T_A 4.3W 2W
Thermal Resistance		
θ_{JC} $3^{\circ}\text{C}/\text{W}$ $3^{\circ}\text{C}/\text{W}$
θ_{JA} $35^{\circ}\text{C}/\text{W}$ $60^{\circ}\text{C}/\text{W}$

TYPICAL APPLICATIONS



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7805A			UC7805AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$	4.95		5.05	4.95		5.05	V
	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}, P_D \leq 15\text{W}$	4.9		5.1	4.87		5.13	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	4.85		5.15	4.85		5.15	V
Line Regulation	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}, I_o = 500\text{mA}$			5			6	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		3	10		3	10	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		10	12		10	17	mV
	$V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			25			25	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$.4			.4	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.5			.5	mA
	$T_j = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 20\text{V}, I_o = 500\text{mA}$.6			.6	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.8			.8	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, 8\text{V} \leq V_{IN} \leq 18\text{V}, I_o = 500\text{mA}$	69			69			dB
Output Noise Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 1\text{A}$		40			40		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		2			2		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = 10\text{V}$		2.1			2.1		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = 10\text{V}, I_o = 5\text{mA}$		-4			-4		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = 10\text{V}, I_o = 5\text{mA}$		20			20		mV
Thermal Shutdown	$V_{IN} = 10\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7812A			UC7812AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $I_o = 1\text{A}$	11.88		12.12	11.88		12.12	V
	$T_j = 25^\circ\text{C}$, $14.5\text{V} \leq V_{IN} \leq 27\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}$, $P_D \leq 15\text{W}$	11.76		12.24	11.70		12.30	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	11.64		12.36	11.64		12.36	V
Line Regulation	$T_j = 25^\circ\text{C}$, $14.5\text{V} \leq V_{IN} \leq 27\text{V}$, $I_o = 500\text{mA}$			12			15	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		4	18	4	18		mV
Load Regulation	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		12	32	12	50		mV
	$V_{IN} = 19\text{V}$, $5\text{mA} \leq I_o \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			60		60		mV
Quiescent Current	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $I_o = 1\text{A}$		4.5	6	4.5	6		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5		6.5		mA
Quiescent Current Change	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $5\text{mA} \leq I_o \leq 1\text{A}$.4		.4		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.5		.5		mA
	$T_j = 25^\circ\text{C}$, $14.5\text{V} \leq V_{IN} \leq 27\text{V}$, $I_o = 500\text{mA}$.6		.6		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.8		.8		mA
Ripple Rejection	$T_j = 25^\circ\text{C}$, $15\text{V} \leq V_{IN} \leq 25\text{V}$, $I_o = 500\text{mA}$	62			62			dB
Output Noise Voltage	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $I_o = 5\text{mA}$		75		75			μV
Dropout Voltage	$T_j = 25^\circ\text{C}$, $I_o = 1\text{A}$		2		2			V
Short Circuit Current	$T_j = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$		1.5		1.5			A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.4		2.4			A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}$, $V_{IN} = 19\text{V}$, $I_o = 5\text{mA}$		-8		-8			mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}$, $V_{IN} = 19\text{V}$, $I_o = 5\text{mA}$		50		50			mV
Thermal Shutdown	$V_{IN} = 19\text{V}$, $I_o = 5\text{mA}$		175		175			$^\circ\text{C}$
	T_{MAX}		150		125			$^\circ\text{C}$
	T_{MIN}		-55		0			$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

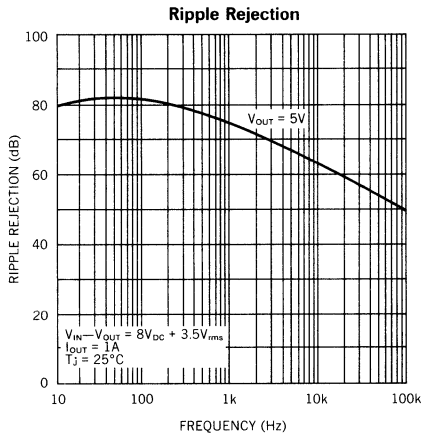
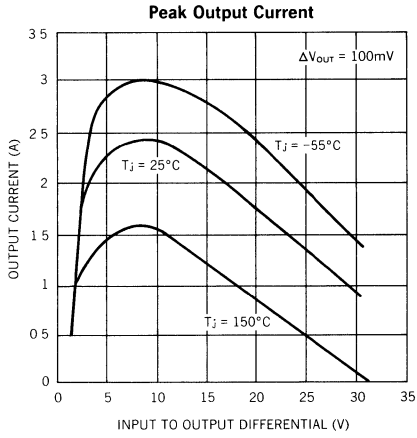
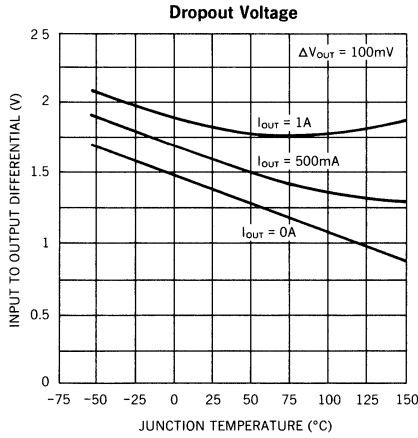
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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7815A			UC7815AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 1\text{A}$	14.85		15.15	14.85		15.15	V
	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1\text{A}, P_D \leq 15\text{W}$	14.7		15.3	14.60		15.40	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	14.55		15.45	14.55		14.45	V
Line Regulation	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}, I_o = 500\text{mA}$			15			19	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		4	22		4	22	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		12	35		12	50	mV
	$V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$ Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			75			75	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 1\text{A}$		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, 5\text{mA} \leq I_o \leq 1\text{A}$.4			.4	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.5			.5	mA
	$T_j = 25^\circ\text{C}, 17.5\text{V} \leq V_{IN} \leq 30\text{V}, I_o = 500\text{mA}$.6			.6	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$.8			.8	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, 18.5\text{V} \leq V_{IN} \leq 28.5\text{V}, I_o = 500\text{mA}$	60			60			dB
Output Noise Voltage	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		90			90		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		2			2		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = 23\text{V}$		1.2			1.2		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		-1.0			-1.0		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = 23\text{V}, I_o = 5\text{mA}$		60			60		mV
Thermal Shutdown	$V_{IN} = 23\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

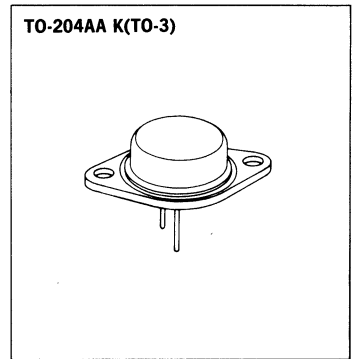
TYPICAL PERFORMANCE CHARACTERISTICS



MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

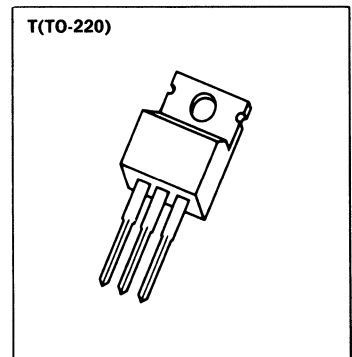
**UC7800A SERIES
UC7800AC SERIES**

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.



UC7800AC SERIES

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85



ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX	
	K(TO-3)	T(TO-220)
5V	UC7805AK UC7805ACK	— UC7805ACT
12V	UC7812AK UC7812ACK	— UC7812ACT
15V	UC7815AK UC7815ACK	— UC7815ACT

LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Negative Regulators

UC7900
UC7900C
SERIES

3

FEATURES

- $\pm 4\%$ preset output voltage
- Output current to 1.5A
- One external component
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe area compensation
- Available in TO-3 and TO-220 packages
- Output voltages of -5, -12 and -15V (For other voltages, please contact the factory)

DESCRIPTION

These three terminal monolithic negative voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. These units feature an on-chip trimming system to set the output voltages to within $\pm 4\%$ of nominal. This regulator series is an optimum complement to the UC7800/7800C line of three terminal positive regulators. Two companion series, the UC7900A and UC7900AC, offer tighter output tolerances, and improved line and load regulation characteristics.

ABSOLUTE MAXIMUM RATINGS

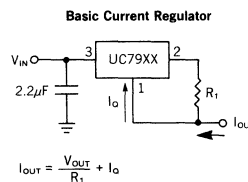
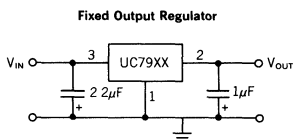
Input Voltage	-35V
Input-Output Voltage Differential	30V
Power Dissipation	Internally limited
Operating Junction Temperature Range	
UC7900 SERIES	-55°C to +150°C
UC7900C SERIES	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
K (TO-3) package	300°C
T (TO-220) package	230°C
Power/Thermal Characteristics	

	K (TO-3) Package	T (TO-220) Package
Rated Power @ 25°C		
T_C	20W	15W
T_A	4.3W	2W
Thermal Resistance		
θ_{JC}	3°C/W	3°C/W
θ_{JA}	35°C/W	60°C/W

TYPICAL APPLICATIONS

Input bypass capacitors are recommended for stable operation of the UC7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.2 μ F on the input, 1 μ F on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μ F or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7905			UC7905C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}, I_o = 5\text{mA}$	-5.20		-4.80	-5.20		-4.80	V
	$T_J = 25^\circ\text{C}, -25\text{V} \leq V_{IN} \leq -8\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}, P \leq P_D$	-5.20		-4.80	-5.23		-4.77	V
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$	-5.25		-4.75	-5.25		-4.75	V
Line Regulation	$T_J = 25^\circ\text{C}, -25\text{V} \leq V_{IN} \leq -7\text{V}, I_o = 5\text{mA}$		25	50		25	50	mV
Load Regulation	$T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$			50			100	mV
Quiescent Current	$T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}, I_o = 500\text{mA}$		1	2.5		1	2.5	mA
	Over Temperature, $T_{MIN} \leq T_J \leq T_{MAX}$			3			3	mA
Quiescent Current Change	$T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$			1.0			1.0	mA
	$T_J = 25^\circ\text{C}, -25\text{V} \leq V_{IN} \leq -8\text{V}, I_o = 500\text{mA}$.5			.5	mA
Ripple Rejection	$T_J = 25^\circ\text{C}, -18\text{V} \leq V_{IN} \leq -8\text{V}, I_o = 500\text{mA}$	54			54			dB
Output Noise Voltage	$f = 10\text{Hz to } 100\text{KHz}, C_L = 1\mu\text{f}$ $T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}, I_o = 500\text{mA}$		100			100		μV
Dropout Voltage	$T_J = 25^\circ\text{C}, I_o = 1\text{A}$		2.0			2.0		V
Short Circuit Current	$T_J = 25^\circ\text{C}, V_{IN} = -10\text{V}$		1.8			1.8		A
Peak Output Current	$T_J = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_J \leq T_{MAX}, V_{IN} = -10\text{V}, I_o = 5\text{mA}$		-4			-4		$\text{mV}/^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_J = 125^\circ\text{C}, V_{IN} = -10\text{V}, I_o = 5\text{mA}$		20			20		mV
Thermal Shutdown	$V_{IN} = -10\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T); $\text{Min } |V_o - V_{IN}| @ -55^\circ\text{C} = 2.5\text{V}$.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7912			UC7912C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$	-12.48		-11.52	-12.58		-11.52	V
	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}, P \leq P_D$	-12.48		-11.52	-12.54		-11.46	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	-12.60		-11.40	-12.60		-11.40	V
Line Regulation	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}, I_o = 5\text{mA}$		30	80		30	80	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$			120			240	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 500\text{mA}$		3			3		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			4			4	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$.8			.8	mA
	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}, I_o = 500\text{mA}$.5			.5	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, -25\text{V} \leq V_{IN} \leq -15\text{V}, I_o = 500\text{mA}$	56			56			dB
Output Noise Voltage	$f = 10\text{Hz to } 100\text{KHz}, C_L = 1\mu\text{f}$ $T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 500\text{mA}$		200			200		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		1.1			1.1		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}$		1.3			1.3		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$		-9			-9		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$		48			48		mV
Thermal Shutdown	$V_{IN} = -17\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T).

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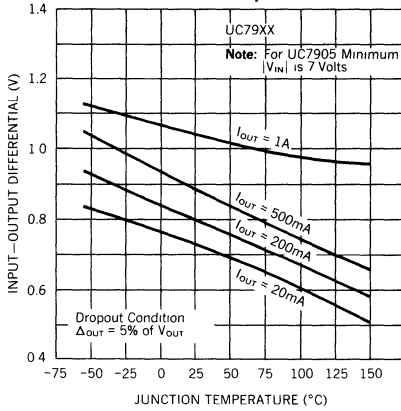
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7915			UC7915C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = -20\text{V}, I_o = 5\text{mA}$	-15.60		-14.40	-15.00		-14.40	V
	$T_j = 25^\circ\text{C}, -35\text{V} \leq V_{IN} \leq -17\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}, P \leq P_D$	-15.60		-14.40	-15.68		-14.32	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	-15.75		-14.25	-15.75		-14.25	V
Line Regulation	$T_j = 25^\circ\text{C}, -35\text{V} \leq V_{IN} \leq -17\text{V}, I_o = 5\text{mA}$		35	100		35	100	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = -20\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$			150			300	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = -20\text{V}, I_o = 500\text{mA}$		3			3		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			4			4	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = -20\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$.8			.8	mA
	$T_j = 25^\circ\text{C}, -35\text{V} \leq V_{IN} \leq -17\text{V}, I_o = 500\text{mA}$.5			.5	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, -28\text{V} \leq V_{IN} \leq -18\text{V}, I_o = 500\text{mA}$	56			56			dB
Output Noise Voltage	$f = 10\text{Hz to } 100\text{KHz}, C_L = 1\mu\text{f}$ $T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 500\text{mA}$		250			250		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		1.1			1.1		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = -20\text{V}$		1.1			1.1		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = -20\text{V}, I_o = 5\text{mA}$		-1.0			-1.0		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = -20\text{V}, I_o = 5\text{mA}$		60			60		mV
Thermal Shutdown	$V_{IN} = -20\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

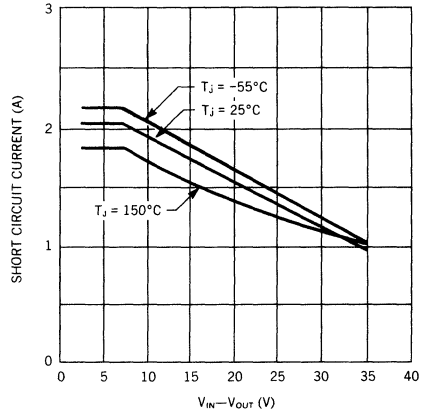
Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T).

TYPICAL PERFORMANCE CHARACTERISTICS

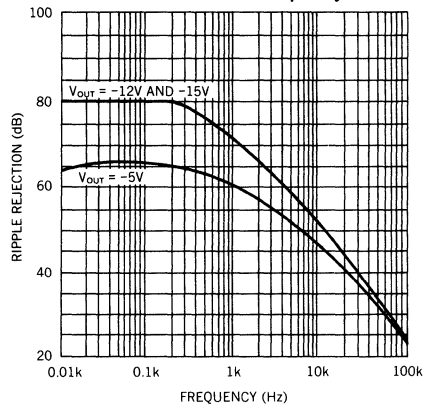
Dropout Voltage as a Function of Junction Temperature



Peak Output Current



Ripple Rejection as a Function of Frequency

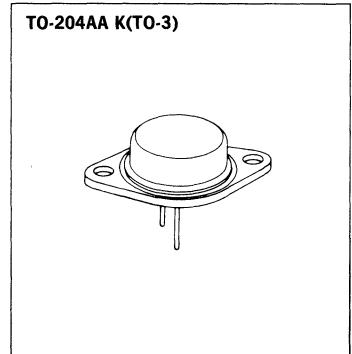


MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

**UC7900 SERIES
UC7900C SERIES**

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

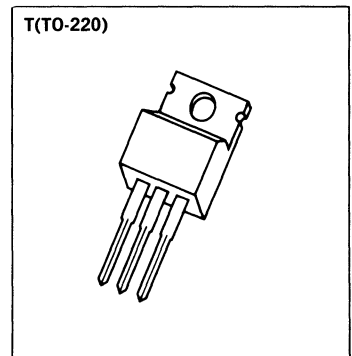
Bottom View



UC7900C SERIES

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

1-Ground
2-Output
3-Input
4-Input



ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX	
	K(TO-3)	T(TO-220)
-5V	UC7905K UC7905CK	— UC7905CT
-12V	UC7912K UC7912CK	— UC7912CT
-15V	UC7915K UC7915CK	— UC7915CT

LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Negative Regulators

Precision Version

UC7900A
UC7900AC
SERIES

3

FEATURES

- $\pm 1.0\%$ preset output voltage
- Output current to 1.5A
- One external component
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe area compensation
- Available in TO-3 and TO-220 packages
- Output voltages of -5, -12 and -15V (For other voltages, please contact the factory)

DESCRIPTION

These three terminal monolithic negative voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. These units feature an on-chip trimming system to set the output voltages to within $\pm 1.0\%$ of nominal. They also offer improved line and load regulation characteristics over the UC7900 series.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-35V
Input-Output Voltage Differential	30V
Power Dissipation	Internally limited
Operating Junction Temperature Range		
UC7900A SERIES	-55°C to +150°C
UC7900AC SERIES	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)		
K (TO-3) package	300°C
T (TO-220) package	230°C

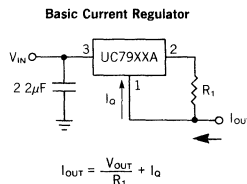
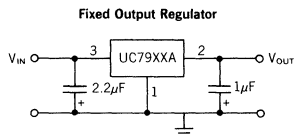
Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package
Rated Power @ 25°C		
T _C	20W	15W
T _A	4.3W	2W
Thermal Resistance		
θ_{JC}	3°C/W	3°C/W
θ_{JA}	35°C/W	60°C/W

TYPICAL APPLICATIONS

Input bypass capacitors are recommended for stable operation of the UC7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.2 μ F on the input, 1 μ F on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μ F or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7905A			UC7905AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$, $I_o = 5\text{mA}$	-5.05		-4.95	-5.05		-4.95	V
	$T_j = 25^\circ\text{C}$, $-25\text{V} \leq V_{IN} \leq -8\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}$, $P \leq P_D$	-5.10		-4.90	-5.13		-4.87	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	-5.15		-4.85	-5.15		-4.85	V
Line Regulation	$T_j = 25^\circ\text{C}$, $-25\text{V} \leq V_{IN} \leq -7\text{V}$, $I_o = 5\text{mA}$		10	15		10	25	mV
Load Regulation	$T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		20	50		20	100	mV
Quiescent Current	$T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$, $I_o = 500\text{mA}$		1	2		1	2	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			2.5			2.5	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$.4			.4	mA
	$T_j = 25^\circ\text{C}$, $-25\text{V} \leq V_{IN} \leq -8\text{V}$, $I_o = 500\text{mA}$.4			.4	mA
Ripple Rejection	$T_j = 25^\circ\text{C}$, $-18\text{V} \leq V_{IN} \leq -8\text{V}$, $I_o = 500\text{mA}$	54			54			dB
Output Noise Voltage	$f = 10\text{Hz}$ to 100KHz , $C_L = 1\mu\text{f}$ $T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$, $I_o = 500\text{mA}$		100			100		μV
Dropout Voltage	$T_j = 25^\circ\text{C}$, $I_o = 1\text{A}$		2.0			2.0		V
Short Circuit Current	$T_j = 25^\circ\text{C}$, $V_{IN} = -10\text{V}$		1.8			1.8		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}$, $V_{IN} = -10\text{V}$, $I_o = 5\text{mA}$		-4			-4		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}$, $V_{IN} = -10\text{V}$, $I_o = 5\text{mA}$		20			20		mV
Thermal Shutdown	$V_{IN} = -10\text{V}$, $I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T); Min $|V_o - V_{IN}|$ @ $-55^\circ\text{C} = 2.5\text{V}$.

ELECTRICAL CHARACTERISTICS

3

PARAMETER	TEST CONDITIONS	UC7912A			UC7912AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$	-12.12		-11.88	-12.12		-11.88	V
	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}, P \leq P_D$	-12.24		-11.76	-12.30		-11.70	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	-12.36		-11.64	-12.36		-11.64	V
Line Regulation	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}, I_o = 5\text{mA}$		10	20		10	30	mV
Load Regulation	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		40	80		40	80	mV
Quiescent Current	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 500\text{mA}$		3			3		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			4			4	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$.4			.4	mA
	$T_j = 25^\circ\text{C}, -32\text{V} \leq V_{IN} \leq -14\text{V}, I_o = 500\text{mA}$.4			.4	mA
Ripple Rejection	$T_j = 25^\circ\text{C}, -25\text{V} \leq V_{IN} \leq -15\text{V}, I_o = 500\text{mA}$	56			56			dB
Output Noise Voltage	$f = 10\text{Hz to } 100\text{KHz}, C_L = 1\mu\text{f}$ $T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 500\text{mA}$		200			200		μV
Dropout Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{A}$		1.1			1.1		V
Short Circuit Current	$T_j = 25^\circ\text{C}, V_{IN} = -17\text{V}$		1.3			1.3		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$		-9			-9		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}, V_{IN} = -17\text{V}, I_o = 5\text{mA}$		48			48		mV
Thermal Shutdown	$V_{IN} = -17\text{V}, I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T).

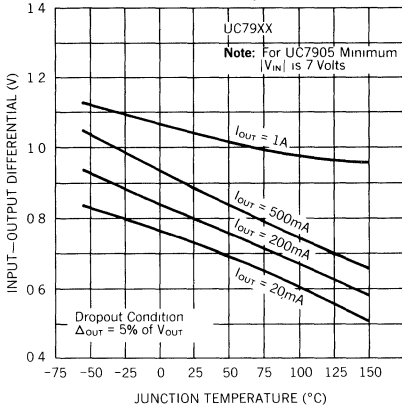
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7915A			UC7915AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	$T_j = 25^\circ\text{C}$, $V_{IN} = -20\text{V}$, $I_o = 5\text{mA}$	-15.15		-14.85	-15.15		-14.85	V
	$T_j = 25^\circ\text{C}$, $-35\text{V} \leq V_{IN} \leq -17\text{V}$ $5\text{mA} \leq I_{OUT} \leq 1.0\text{A}$, $P \leq P_D$	-15.30		-14.70	-15.38		-14.63	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	-15.45		-14.55	-15.45		-14.55	V
Line Regulation	$T_j = 25^\circ\text{C}$, $-35\text{V} \leq V_{IN} \leq -17\text{V}$, $I_o = 5\text{mA}$		10	20		10	30	mV
Load Regulation	$T_j = 25^\circ\text{C}$, $V_{IN} = -20\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		50	80		50	80	mV
Quiescent Current	$T_j = 25^\circ\text{C}$, $V_{IN} = -20\text{V}$, $I_o = 500\text{mA}$		3			3		mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			4			4	mA
Quiescent Current Change	$T_j = 25^\circ\text{C}$, $V_{IN} = -20\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$.4			.4	mA
	$T_j = 25^\circ\text{C}$, $-35\text{V} \leq V_{IN} \leq -17\text{V}$, $I_o = 500\text{mA}$.4			.4	mA
Ripple Rejection	$T_j = 25^\circ\text{C}$, $-28\text{V} \leq V_{IN} \leq -18\text{V}$, $I_o = 500\text{mA}$	56			56			dB
Output Noise Voltage	$f = 10\text{Hz}$ to 100KHz , $C_L = 1\mu\text{f}$ $T_j = 25^\circ\text{C}$, $V_{IN} = -17\text{V}$, $I_o = 500\text{mA}$		250			250		μV
Dropout Voltage	$T_j = 25^\circ\text{C}$, $I_o = 1\text{A}$		1.1			1.1		V
Short Circuit Current	$T_j = 25^\circ\text{C}$, $V_{IN} = -20\text{V}$		1.1			1.1		A
Peak Output Current	$T_j = 25^\circ\text{C}$		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	$0^\circ\text{C} \leq T_j \leq T_{MAX}$, $V_{IN} = -20\text{V}$, $I_o = 5\text{mA}$		-1.0			-1.0		mV/ $^\circ\text{C}$
Long Term Stability	1000 Hrs. @ $T_j = 125^\circ\text{C}$, $V_{IN} = -20\text{V}$, $I_o = 5\text{mA}$		60			60		mV
Thermal Shutdown	$V_{IN} = -20\text{V}$, $I_o = 5\text{mA}$		175			175		$^\circ\text{C}$
	T_{MAX}		150			125		$^\circ\text{C}$
	T_{MIN}		-55			0		$^\circ\text{C}$

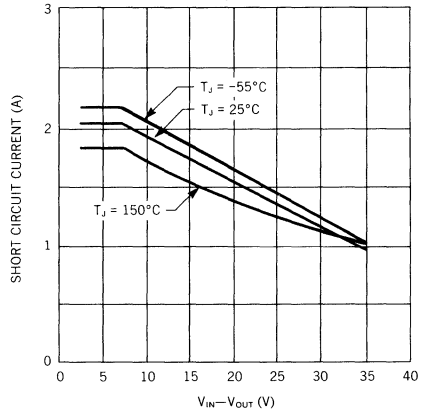
Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10\text{ms}$, duty-cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
 $P_D = 20\text{W}$ for TO-3 (K) and 15W for TO-220 (T).

TYPICAL PERFORMANCE CHARACTERISTICS

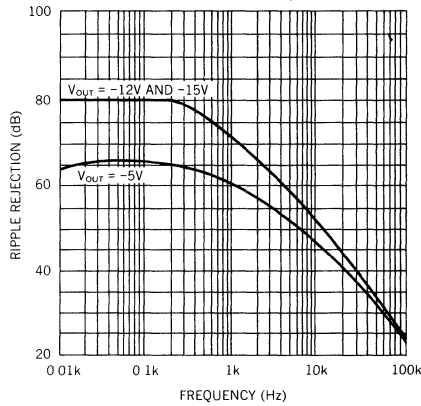
Dropout Voltage as a Function of Junction Temperature



Peak Output Current



Ripple Rejection as a Function of Frequency



MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

Bottom View

**UC7900A SERIES
UC7900AC SERIES**

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)

1-Ground
2-Output
3-Input
4-Input

UC7900AC SERIES

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

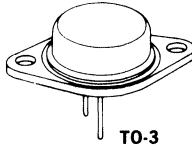
T(TO-220)

ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX	
	K(TO-3)	T(TO-220)
-5V	UC7905AK UC7905ACK	— UC7905ACT
-12V	UC7912AK UC7912ACK	— UC7912ACT
-15V	UC7915AK UC7915ACK	— UC7915ACT

N-CHANNEL POWER MOSFETS

PRODUCT SELECTION GUIDE



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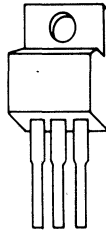
V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
500	0.4	2N6770*	7.75	12.0	48	150
500	0.4	UFN450	8.0	13.0	52	150
500	0.5	UFN452	7.0	12.0	48	150
500	0.85	UFN440	5.0	8.0	32	125
500	1.1	UFN442	4.0	7.0	28	125
500	1.5	2N6762*	3.0	4.5	18	75
500	1.5	UFN430	3.0	4.5	18	75
500	2.0	UFN432	3.5	4.0	16	75
500	3.0	UFN420	1.5	2.5	10	40
500	4.0	UFN422	1.0	2.0	8	40
450	0.4	UFN451	8.0	13.0	52	150
450	0.5	2N6769	7.0	11.0	44	150
450	0.5	UFN453	7.0	12.0	48	150
450	0.85	UFN441	5.0	8.0	32	125
450	1.1	UFN443	4.0	7.0	28	125
450	1.5	UFN431	3.0	4.5	18	75
450	2.0	2N6761	2.5	4.0	16	75
450	2.0	UFN433	2.5	4.0	16	75
450	3.0	UFN421	1.5	2.5	10	40
450	4.0	UFN423	1.0	2.0	8	40
400	0.3	2N6768*	9.0	14.0	56	150
400	0.3	UFN350	9.0	15.0	60	150
400	0.4	UFN352	8.0	13.0	52	150
400	0.55	UFN340	6.0	10.0	40	125
400	0.8	UFN342	5.0	8.0	32	125
400	1.0	2N6760*	3.5	5.5	22	75
400	1.0	UFN330	3.5	5.5	22	75
400	1.5	UFN332	3.0	4.5	18	75
400	1.8	UFN320	2.0	3.0	12	40
400	2.5	UFN322	1.5	2.5	10	40
350	0.3	UFN351	9.0	15.0	60	150
350	0.4	2N6767	7.75	12.0	48	150
350	0.4	UFN353	8.0	13.0	52	150
350	0.55	UFN341	6.0	10.0	40	125
350	0.8	UFN343	5.0	8.0	32	125
350	1.0	UFN331	3.5	5.5	22	75
350	1.5	2N6759	3.0	4.5	18	75
350	1.5	UFN333	3.5	4.5	18	75
350	1.8	UFN321	2.0	3.0	12	40
350	2.5	UFN323	1.5	2.5	10	40

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
200	0.085	2N6766*	19.0	30.0	120	150
200	0.085	UFN250	19.0	30.0	120	150
200	0.12	UFN252	16.0	25.0	100	150
200	0.18	UFN240	11.0	18.0	72	125
200	0.22	UFN242	10.0	16.0	64	125
200	0.4	2N6758*	6.0	9.0	36	75
200	0.4	UFN230	6.0	9.0	36	75
200	0.6	UFN232	5.0	8.0	32	75
200	0.8	UFN220	3.0	5.0	20	40
200	1.2	UFN222	2.5	4.0	16	40
150	0.085	UFN251	19.0	30.0	120	150
150	0.12	2N6765	16.0	25.0	100	150
150	0.12	UFN253	16.0	25.0	100	150
150	0.18	UFN241	11.0	18.0	72	125
150	0.22	UFN243	10.0	16.0	64	125
150	0.4	UFN231	6.0	9.0	36	75
150	0.6	2N6757	5.0	8.0	32	75
150	0.6	UFN233	5.0	8.0	32	75
150	0.8	UFN221	3.0	5.0	20	40
150	1.2	UFN223	2.5	4.0	16	40
100	0.055	2N6764*	24.0	38.0	152	150
100	0.055	UFN150	25.0	40.0	160	150
100	0.08	UFN152	20.0	33.0	132	150
100	0.085	UFN140	17.0	27.0	108	125
100	0.11	UFN142	15.0	24.0	96	125
100	0.18	2N6756*	9.0	14.0	56	75
100	0.18	UFN130	9.0	14.0	56	75
100	0.25	UFN132	8.0	12.0	48	75
100	0.3	UFN120	5.0	8.0	32	40
100	0.4	UFN122	4.0	7.0	28	40
60	0.055	UFN151	25.0	40.0	160	150
60	0.08	2N6763	20.0	31.0	124	150
60	0.08	UFN153	20.0	33.0	132	150
60	0.085	UFN141	17.0	27.0	108	125
60	0.11	UFN143	15.0	24.0	96	125
60	0.18	UFN131	9.0	14.0	56	75
60	0.25	2N6755	8.0	12.0	48	75
60	0.25	UFN133	8.0	12.0	48	75
60	0.3	UFN121	5.0	8.0	32	40
60	0.4	UFN123	4.0	7.0	28	40

* Available as JAN, JANTX, and JANTXV types.

N-CHANNEL POWER MOSFETS

PRODUCT SELECTION GUIDE

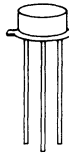


TO-220AB

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
500	0.85	UFN840	5.0	8.0	32	125
500	1.1	UFN842	4.0	7.0	28	125
500	1.5	UFN830	3.0	4.5	18	75
500	2.0	UFN832	2.5	4.0	16	75
500	3.0	UFN820	1.5	2.5	10	40
500	4.0	UFN822	1.0	2.0	8	40
450	0.85	UFN841	5.0	8.0	32	125
450	1.1	UFN843	4.0	7.0	28	125
450	1.5	UFN831	3.0	4.5	18	75
450	2.0	UFN833	2.5	4.0	16	75
450	3.0	UFN821	1.5	2.5	10	40
450	4.0	UFN823	1.0	2.0	8	40
400	0.55	UFN740	6.0	10.0	40	125
400	0.80	UFN742	5.0	8.0	32	125
400	1.0	UFN730	3.5	5.5	22	75
400	1.5	UFN732	3.0	4.5	18	75
400	1.8	UFN720	2.0	3.0	12	40
400	2.5	UFN722	1.5	2.5	10	40
400	3.6	UFN710	1.0	1.5	6	20
400	5.0	UFN712	0.8	1.3	5	20
350	0.55	UFN741	6.0	10.0	40	125
350	0.8	UFN743	5.0	8.0	32	125
350	1.0	UFN731	3.5	5.5	22	75
350	1.5	UFN733	3.0	4.5	18	75
350	1.8	UFN721	2.0	3.0	12	40
350	2.5	UFN723	1.5	2.5	10	40
350	3.6	UFN711	1.0	1.5	6	20
350	5.0	UFN713	0.8	1.3	5	20
200	0.18	UFN640	11.0	18.0	72	125
200	0.22	UFN642	10.0	16.0	64	125

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX Power Dissipation (Watts)
			100°C Case	25°C Case		
200	0.4	UFN630	6.0	9.0	36	75
200	0.6	UFN632	5.0	8.0	32	75
200	0.8	UFN620	3.0	5.0	20	40
200	1.2	UFN622	2.5	4.0	16	40
200	1.5	UFN610	1.5	2.5	10	20
200	2.4	UFN612	1.25	2.0	8	20
150	0.18	UFN641	11.0	18.0	72	125
150	0.22	UFN643	10.0	16.0	64	125
150	0.4	UFN631	6.0	9.0	36	75
150	0.6	UFN633	5.0	8.0	32	75
150	0.8	UFN621	3.0	5.0	20	40
150	1.2	UFN623	2.5	4.0	16	40
150	1.5	UFN611	1.5	2.5	10	20
150	2.4	UFN613	1.25	2.0	8	20
100	0.085	UFN540	17.0	27.0	108	125
100	0.11	UFN542	15.0	24.0	96	125
100	0.18	UFN530	9.0	14.0	56	75
100	0.25	UFN532	8.0	12.0	48	75
100	0.3	UFN520	5.0	8.0	32	40
100	0.4	UFN522	4.0	7.0	28	40
100	0.6	UFN510	2.5	4.0	16	20
100	0.8	UFN512	2.0	3.5	14	20
60	0.085	UFN541	17.0	27.0	108	125
60	0.11	UFN543	15.0	24.0	96	125
60	0.18	UFN531	9.0	14.0	56	75
60	0.25	UFN533	8.0	12.0	48	75
60	0.3	UFN521	5.0	8.0	32	40
60	0.4	UFN523	4.0	7.0	28	40
60	0.6	UFN511	2.5	4.0	16	20
60	0.8	UFN513	2.0	3.5	14	20

N-CHANNEL POWER MOSFETS



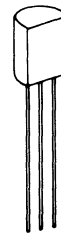
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V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			100°C Case	25°C Case		
500	1.5	UFNF430	1.75	2.75	11	25
500	1.5	2N6802	1.5	2.5	11	25
500	2.0	UFNF432	1.5	2.25	9	25
500	3.0	UFNF420	1.0	1.6	6.5	20
500	3.0	2N6794	0.95	1.5	6.5	20
500	4.0	UFNF422	0.9	1.4	5.5	20
450	1.5	UFNF431	1.75	2.75	11	25
450	1.5	2N6801	1.5	2.5	11	25
450	2.0	UFNF433	1.5	2.25	9	25
450	3.0	UFNF421	1.0	1.6	6.5	20
450	3.0	2N6793	0.95	1.5	6.5	20
450	4.0	UFNF423	0.9	1.4	5.5	20
400	1.0	UFNF330	2.0	3.5	14	25
400	1.0	2N6800	1.6	3.0	14	25
400	1.5	UFNF332	1.6	3.0	12	25
400	1.8	UFNF320	1.45	2.5	10	20
400	1.8	2N6792	1.25	2.0	10	20
400	2.5	UFNF322	1.2	2.0	8	20
400	3.6	UFNF310	0.85	1.35	5.5	15
400	3.6	2N6786	0.80	1.25	5.5	15
400	5.0	UFNF312	0.70	1.15	4.5	15
350	1.0	UFNF331	2.0	3.5	14	25
350	1.0	2N6799	1.6	3.0	14	25
350	1.5	UFNF333	1.6	3.0	12	25
350	1.8	UFNF321	1.45	2.5	10	20
350	1.8	2N6791	1.25	2.0	10	20
350	2.5	UFNF323	1.2	2.0	8	20
350	3.6	UFNF311	0.85	1.35	5.5	15
350	3.6	2N6785	0.80	1.25	5.5	15
350	5.0	UFNF313	0.70	1.15	4.5	15
200	0.4	2FNF6798	3.5	5.5	22	25
200	0.4	UFNF230	3.5	5.5	22	25
200	0.6	UFNF232	2.8	4.5	18	25
200	0.8	2N6790	2.1	3.5	14	20
200	0.8	UFNF220	2.1	3.5	14	20
200	1.2	UFNF222	1.75	3.0	12	20
200	1.5	2N6784	1.45	2.25	9	15
200	1.5	UFNF210	1.4	2.2	9	15
200	2.4	UFNF212	1.1	1.8	7.5	15
150	0.4	2N6797	3.5	5.5	22	25
150	0.4	UFNF231	3.5	5.5	22	25
150	0.6	UFNF233	2.8	4.5	18	25
150	0.8	2N6789	2.1	3.5	14	20
150	0.8	UFNF221	2.1	3.5	14	20
150	1.2	UFNF223	1.75	3.0	12	20
150	1.5	2N6783	1.45	2.25	9	15
150	1.5	UFNF211	1.4	2.2	9	15
150	2.4	UFNF213	1.1	1.8	7.5	15
100	0.18	2N6796	5.0	8.0	32	25
100	0.18	UFNF130	5.0	8.0	32	25
100	0.25	UFNF132	4.5	7.0	28	25
100	0.3	2N6788	3.5	6.0	24	20
100	0.3	UFNF120	3.5	6.0	24	20
100	0.4	UFNF122	3.0	5.0	20	20

PRODUCT SELECTION GUIDE

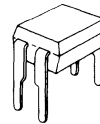
4

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			100°C Case	25°C Case		
100	0.6	2N6782	2.25	3.5	14	15
100	0.6	UFNF110	2.25	3.5	14	15
100	0.8	UFNF112	2.0	3.0	12	15
60	0.18	2N6795	5.0	8.0	32	25
60	0.18	UFNF131	5.0	8.0	32	25
60	0.25	UFNF133	4.5	7.0	28	25
60	0.3	2N6787	3.5	6.0	24	20
60	0.3	UFNF121	3.5	6.0	24	20
60	0.4	UFNF123	3.0	5.0	20	20
60	0.6	2N6781	2.25	3.5	14	15
60	0.6	UFNF111	2.25	3.5	14	15
60	0.8	UFNF113	2.0	3.0	12	15



TO-92

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			25°C Case	25°C Case		
100	1.5	UFNA12	1.0	2.0	2.4	
60	1.5	UFNA11	1.0	2.0	2.4	

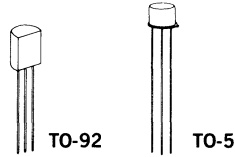


DIL-4

V _{DS} Drain Source Voltage (Volts)	R _{DS(on)} On-State Resistance (Ohms)	Part Numbers	I _D Continuous Drain Current (Amps)		I _{DM} Pulsed Drain Current (Amps)	P _D MAX. Power Dissipation (Watts)
			25°C Case	25°C Case		
200	1.5	UFND210	0.6	2.5	1.0	
150	2.4	UFND213	0.45	1.8	1.0	
100	0.3	UFND120	1.3	5.2	1.0	
100	0.6	UFND110	1.0	4.0	1.0	
100	2.4	UFND120	0.5	2.0	1.0	
60	0.4	UFND123	1.1	4.4	1.0	
60	0.8	UFND113	0.8	3.0	1.0	
60	3.2	UFND123	0.4	1.5	1.0	

NPN BIPOLAR POWER SWITCHING TRANSISTORS

.5-30A, 60-500V



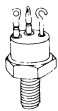
LOW VOLTAGE

Maximum Collector Current		1 AMP (PEAK)	2 AMP	3 AMP	
Package Style		TO-92	TO-5	TO-5	
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sat)}$	60V		UPT212	2N3418*	2N3420*
	80V		UPT213	2N3419*	2N3421*
	100V	UPTA510	UPT214 UPT215		
h_{FE} Minimum		20 @ 1A	30 @ .5A	20 @ 1A	40 @ 1A
$V_{CE(sat)}$ Max.		1V @ .5A	1V @ 2A	5V @ 2A	5V @ 2A
t_f Maximum		0.2 μ s (typical)	0.1 μ s (typical)	1.2 μ s ($t_{OFF} = t_s + t_f$)	

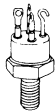
HIGH VOLTAGE

Maximum Collector Current		.5 AMP (PEAK)	1 AMP (PEAK)	2 AMP*	
Package Style		TO-92	TO-92	TO-5	
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sat)}$	150V			UPT311	
	200V	UPTB520	UPTA520	UPT312	2N5662*
	250V			UPT313	
	275V				
	300V	UPTB530	UPTA530	UPT314 UPT315	2N5663*
	350V				
	400V	UPTB540			
	500V	UPTB550			
h_{FE} Minimum		20 @ 25mA	25 @ .1A	30 @ .5A	40 @ .5A (2N5662) 25 @ .5A (2N5663)
$V_{CE(sat)}$ Max.		1.2v @ 50mA	1V @ .5A	1V @ 2A	4V @ 1A
t_f Maximum		1.0 μ s (typical)	0.2 μ s (typical)	0.3 μ s (typical)	0.4 μ s (2N5662) 0.6 μ s (2N5663)

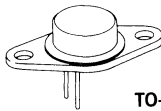
*Available as JAN, JANTX, JANTXV.



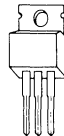
TO-59



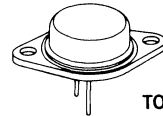
TO-111



TO-66



TO-220AB



TO-3

LOW VOLTAGE

Maximum Collector Current		5 AMP				
Package Style		TO-5	TO-59		TO-111	
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sus)}$	60V	UPT612				
	80V	UPT613	2N2151** 2N2880* 2N3998*	2N3999*	2N3749* 2N3996*	2N3997*
	100V	UPT614 UPT615				
h_{FE} Minimum		30 @ 1A	40 @ 1A	80 @ 1A	40 @ 1A	80 @ 1A
$V_{CE(sat)}$ Max.		1V @ 5A	.25V @ 1A (1V @ 1A for 2N2151)			
t_f Maximum		0.1 μ s (typical)	0.3 μ s (2N2880) 0.8 μ s (2N3998)	1.0 μ s	0.3 μ s (2N3749) 0.8 μ s (2N3996)	1.0 μ s

HIGH VOLTAGE

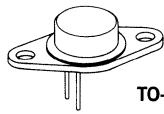
Maximum Collector Current		2 AMP		3 AMP		4 AMP	8 AMP	
Package Style		TO-66		TO-66	TO-220AB	TO-3	TO-220AB	TO-3
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sus)}$	150V	UPT321		UPT521				
	200V	UPT322	2N5660*	UPT522				
	250V	UPT323		UPT523		2N5838		
	275V					2N5839		
	300V	UPT324 UPT325	2N5661*	UPT524 UPT525	UMT1203		UMT13004	2N6671
	350V					2N5840		2N6672
	400V				UMT1204		UMT13005	2N6673
	500V							
h_{FE} Minimum		30 @ .5A	40 @ .5A (2N5660) 25 @ .5A (2N5661)	25 @ 1A	7 @ .2A	10 @ 2A	8 @ 2A	10 @ 5A
$V_{CE(sat)}$ Max.		1V @ 2A	.4V @ 1A	1V @ 3A	3V @ 3A	1.5V @ 2A	0.6V @ 2A	1.0 @ 5A
t_f Maximum		0.3 μ s (typical)	0.4 μ s (2N5660) 0.6 μ s (2N5661)	0.4 μ s (typical)	0.7 μ s	1.5 μ s	0.9 μ s	0.4 μ s

* Available as JAN, JANTX, JANTXV

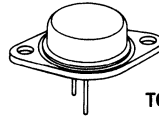
** Available as JAN, JANTX

NPN BIPOLAR POWER SWITCHING TRANSISTORS

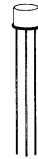
.5-30A, 60-500V



TO-66



TO-3



TO-5

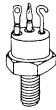
LOW VOLTAGE

Maximum Collector Current		10 AMP		
Package Style		TO-5		TO-3
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sus)}$	70V	2N4150**		
	75V			
	80V		2N5552	
	90V			
	100V			
	120V			2N6354
h_{FE} Minimum		50 @ 5A	50 @ 5A	10 @ 10A
$V_{CE(sat)}$ Max.		0.6V @ 5A	0.5V @ 5A	1.0V @ 10A
t_r Maximum		0.5 μ s	0.45 μ s	0.2 μ s

HIGH VOLTAGE

Maximum Collector Current		5 AMP					8AMP				
Package Style		TO-5		TO-66		TO-3		TO-220AB	TO-3		
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CE(sus)}$	150V					UPT721					
	200V	2N5666*		2N5664*		UPT722					
	250V					UPT723			2N6306		
	275V										
	300V		2N5667*		2N5665*	UPT724 UPT725	2N6542		UMT13006	2N6307	
	350V							UMT1006			2N6308
	400V						2N6543	UMT1007	UMT13007		
	450V										
h_{FE} Minimum		40 @ 1A	25 @ 1A	40 @ 1A	25 @ 1A	25 @ 1A	7 @ 3A	7 @ 3A	6 @ 5A	15 @ 3A	12 @ 3A
$V_{CE(sat)}$ Max.				0.4V @ 3A		1V @ 3A	1.0V @ 3A	1.0V @ 3A	1.5V @ 5A	0.8V @ 3A	1.5V @ 3A
t_r Maximum		0.8 μ s	1.0 μ s	0.8 μ s	1.0 μ s	0.5 μ s (typical)	0.8 μ s	0.4 μ s	0.7 μ s	0.4 μ s	

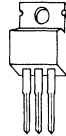
*Available as JAN, JANTX, JANTXV.



TO-59



TO-111



TO-220AB

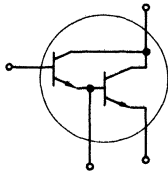
LOW VOLTAGE

Maximum Collector Current		10 AMP		15 AMP	20 AMP		30 AMP
Package Style		TO-59	TO-111	TO-3	TO-3	TO-3	TO-3
COLLECTOR-EMITTER SUSTAINING VOLTAGE V_{CE0} (ISUS)	70V						
	75V					2N5039*	
	80V	2N5658	2N5659				
	90V					2N5038*	2N5671
	100V			2N6496			
	120V						2N5672
h_{FE} Minimum		50 @ 5A		12 @ 8A	20 @ 12A	20 @ 10A	20 @ 15A
V_{CE} (sat) Max.		0.5V @ 5A		1.0V @ 8A	1.2V @ 12A	1.0V @ 10A	0.75V @ 15A
t_r Maximum		0.5 μ s		0.5 μ s	0.5 μ s	0.5 μ s	0.5 μ s

*Available as JAN, JANTX, JANTXV.

HIGH VOLTAGE

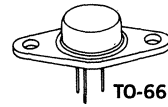
8 AMP	10 AMP					12 AMP	15 AMP			30 AMP
TO-3	TO-3					TO-220AB	TO-3			TO-3
	2N6249									
				2N6250						
UMT1008 2N6544		2N6674				UMT13008		2N6546		2N6676
				2N6251		UMT1011				2N6677
UMT1009 2N6545		2N6675				UMT13009	UMT1012	2N6547		2N6678
								UMT2000		
7 @ 5A	10 @ 10A	8 @ 10A	8 @ 10A	6 @ 10A	6 @ 8A	6 @ 10A	6 @ 10A	7 @ 15A	8 @ 15A	5 @ 20A
1.5V @ 5A	1.5V @ 10A	1.0V @ 10A	1.5V @ 10A	1.5V @ 10A	1.5V @ 8A	1.0V @ 10A	1.5V @ 10A	3.0V @ 10A	1.0 @ 15A	1.5 @ 20A
0.9 μ s (2N6544, 5) 0.4 μ s (UMT1008, 9)	1.0 μ s	0.5 μ s	1.0 μ s	1.0 μ s	0.7 μ s	0.4 μ s	0.7 μ s	0.15 μ s	0.5 μ s	0.8 μ s



External bias types — for fast switching or other special purpose applications



TO-33



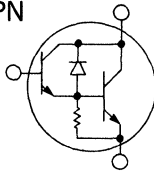
TO-66 (3-Pin)

NPN Power Darlingtons

Maximum Collector Current		2A				5A			
Package Style		TO-33		TO-66 (3-Pin)		TO-33		TO-66 (3-Pin)	
COLLECTOR-EMITTER SUSTAINING VOLTAGE V_{CE0} (US)	60V	U2T301		U2T401					
	80V					2N6350* U2T101		2N6352* U2T201	
	150V		U2T305		U2T405		2N6351* U2T105		2N6353* U2T205
h_{FE} Minimum		1000 @ 2A		1000 @ 2A		2000 @ 5A	1000 @ 5A	2000 @ 5A	1000 @ 5A
$V_{CE(sat)}$ Maximum		1.5V @ 2A	2.5V @ 2A	1.5V @ 2A	2.5V @ 2A	1.5V @ 5A	2.5V @ 5A	1.5V @ 5A	2.5V @ 5A
t_r Typical		0.3 μ s				0.5 μ s			

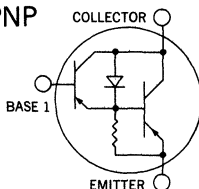
*Available as JAN, JANTX, and JANTVX types

NPN



Plastic Package types with integral bias resistance and shunt diode for maximum economy in standard applications

PNP



Plastic NPN Power Darlingtons

Maximum Collector Current		5A (PEAK)		
Package Style		TO-92		
COLLECTOR-EMITTER SUSTAINING VOLTAGE V_{CE0} (US)	60V	NPN	PNP	
		80V	U2TA508	U2TA608
		100V	U2TA510	U2TA610
h_{FE} Minimum		500 @ 3A		
$V_{CE(sat)}$ Maximum		1.5V @ 3A		
t_r Typical		0.8 μ s		

POWER TRANSISTORS

2 Amp, 80V, Planar NPN

JAN & JANTX 2N2151

FEATURES

- Meets MIL-S-19500/277
- Collector-Base Voltage: up to 150V
- D.C. Collector Current: 2A
- Beta Guaranteed at 3 Current Levels
- Characterized for Safe Operating Area

DESCRIPTION

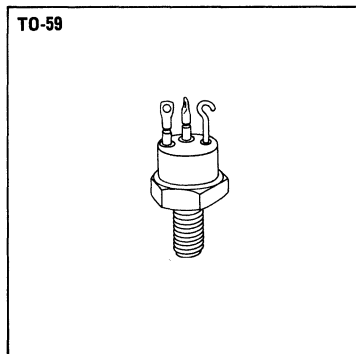
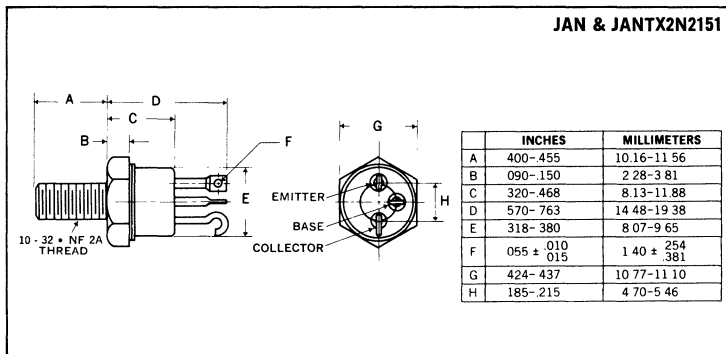
Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

4

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	150V
Collector-Emitter Voltage, V_{CEO}	100V
Emitter-Base Voltage, V_{EBO}	8V
D.C. Collector Current, I_C	2A
Base Current, I_B	2A
Power Dissipation	
100°C Case	30W
Operating Temperature Range	-55°C to 175°C
Storage Temperature Range	-65°C to 200°C

MECHANICAL SPECIFICATIONS

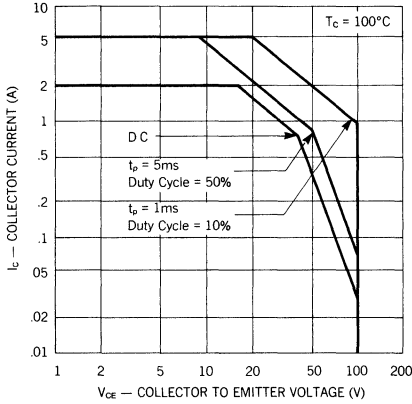


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

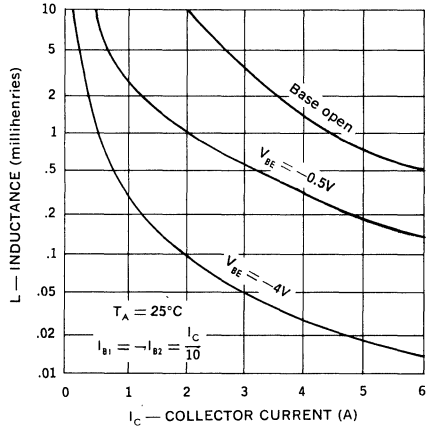
Test	Symbol	Min.	Max.	Units	/277C Sub- group	Method	MIL-STD-750 Test Conditions
25°C							
Collector-Base Breakdown Voltage	V_{CB0}	150	—	Vdc	A-2	3001	$I_C = 100\mu\text{Adc}$, Cond. D
Collector-Emitter Breakdown Voltage (Note 1)	V_{CEO}	100	—	Vdc	A-2	3011	$I_C = 50\text{mAdc}$, Cond. D
Collector-Emitter Cutoff Current	I_{CES}	—	5	μAdc	A-2	3041	$V_{CE} = 120\text{Vdc}$, $V_{BE} = 0$, Cond. C
Collector-Emitter Cutoff Current	I_{CEX}	—	5	μAdc	A-2	3041	$V_{CE} = 120\text{Vdc}$, $V_{EB} = 1\text{Vdc}$, Cond. A
Collector-Emitter Cutoff Current	I_{CE0}	—	10	μAdc	A-2	3041	$V_{CE} = 80\text{Vdc}$, Cond. D
Collector-Base Cutoff Current	I_{CB0}	—	5	μAdc	A-2	3036	$V_{CB} = 120\text{Vdc}$, Cond. D
Emitter-Base Cutoff Current	I_{EBO}	—	2	μAdc	A-2	3061	$V_{EB} = 8\text{Vdc}$, Cond. D
D.C. Current Gain (Note 1)	h_{FE}	40	120	—	A-3	3076	$I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$
D.C. Current Gain (Note 1)	h_{FE}	40	120	—	A-3	3076	$I_C = 0.5\text{Adc}$, $V_{CE} = 5\text{Vdc}$
D.C. Current Gain (Note 1)	h_{FE}	40	—	—	A-3	3076	$I_C = 0.1\text{Adc}$, $V_{CE} = 5\text{Vdc}$
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})$	0.1	1.0	Vdc	A-3	3071	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})$	—	1.2	Vdc	A-3	3066	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$, Cond. A
Base-Emitter Voltage (Note 1)	V_{BE}	—	1.2	Vdc	A-3	3066	$I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$, Cond. B
A.C. Current Gain	h_{fe}	40	160	—	A-5	3206	$I_C = 0.1\text{Adc}$, $V_{CE} = 30\text{Vdc}$, $f = 1\text{kHz}$
Gain-Bandwidth Product	f_T	10	70	MHz	A-5	3306	$I_C = 0.1\text{Adc}$, $V_{CE} = 30\text{Vdc}$, $f = 10\text{MHz}$
Output Capacitance	C_{ob}	—	160	pf	A-5	3236	$V_{CB} = 20\text{Vdc}$, $I_E = 0$, $f = 1\text{MHz}$
Thermal Resistance	θ_{J-C}	—	2.5	$^{\circ}\text{C}/\text{W}$	C-1	3151	
100°C							
Forward-Biased Second Breakdown	$I_{S/B}$	2	—	Adc	B-9	—	$V_{CE} = 15\text{Vdc}$, $t = 60$ sec, see curve
Forward-Biased Second Breakdown	$I_{S/B}$	200	—	mAdc	B-9	—	$V_{CE} = 57\text{Vdc}$, $t = 60$ sec, see curve
Forward-Biased Second Breakdown	$I_{S/B}$	25	—	mAdc	B-9	—	$V_{CE} = 100\text{Vdc}$, $t = 60$ sec, see curve
Unclamped Inductive Sweep	$E_{S/B}$	20	—	mj	B-5	—	$I_C = 2\text{Adc}$, $L = 10\text{mh}$
Clamped Inductive Sweep	$E_{S/B}$	80	—	mj	B-6	—	$I_C = 2\text{Adc}$, $L = 40\text{mh}$, $V_{\text{clamp}} = 150\text{V}$
150°C							
Collector-Emitter Cutoff Current	I_{CES}	—	100	μAdc	A-4	3041	$V_{CE} = 120\text{Vdc}$, $V_{BE} = 0$, Cond. C
Collector-Emitter Cutoff Current	I_{CEX}	—	100	μAdc	A-4	3041	$V_{CE} = 120\text{Vdc}$, $V_{EB} = 1\text{Vdc}$
Emitter-Base Cutoff Current	I_{EBO}	—	20	μAdc	A-4	3061	$V_{EB} = 8\text{Vdc}$, Cond. D
-55°C							
D.C. Current Gain (Note 1)	h_{FE}	20	—	—	A-4	3076	$I_C = 0.5\text{Adc}$, $V_{CE} = 5\text{Vdc}$

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

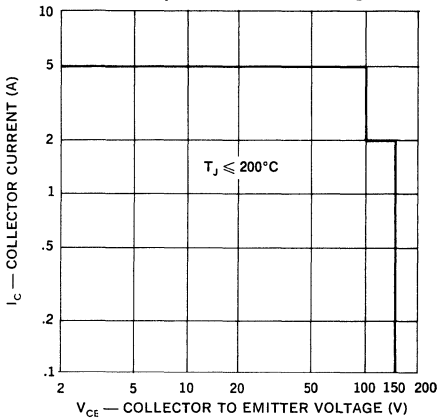
**Forward Bias
Safe Operating Area**



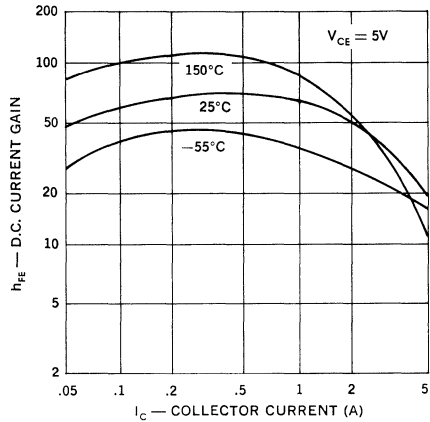
**Unclamped Reverse Bias
Second Breakdown**



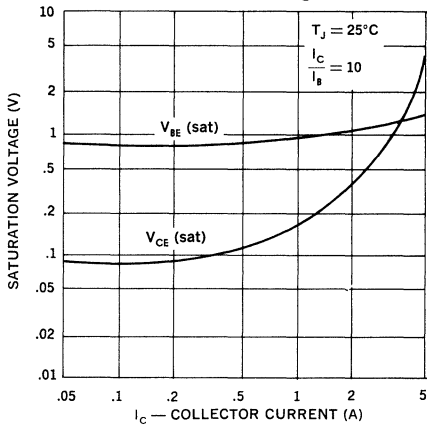
**Reverse Bias
Safe Operating Area
Clamped Inductive Switching**



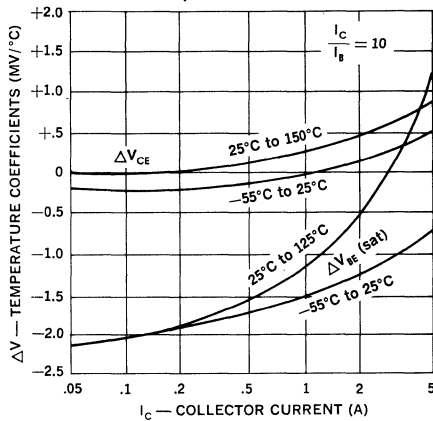
D.C. Current Gain



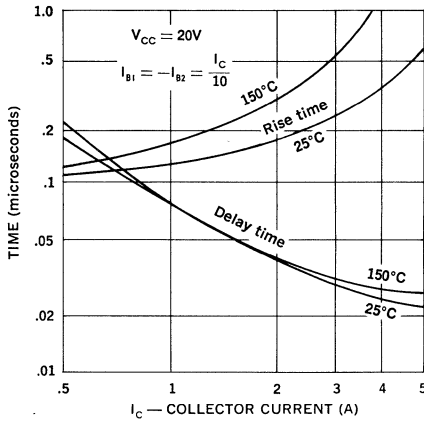
Saturation Voltages



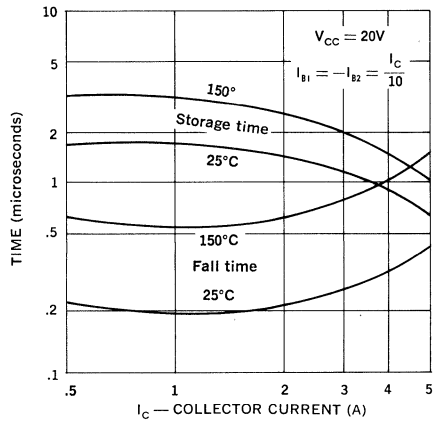
**Saturation Voltage
Temperature Coefficients**



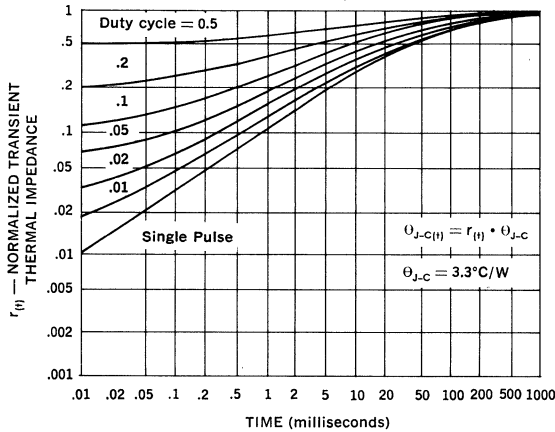
Switching Speed Characteristics



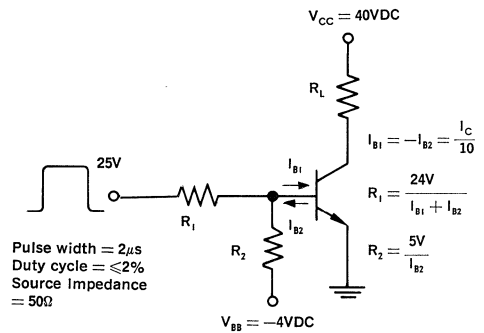
Switching Speed Characteristics



Thermal Response



Switching Speed Circuit



POWER TRANSISTORS

5 Amp, 80V, Planar, NPN

JAN, JANTX, & JANTXV 2N2880
 JAN, JANTX, & JANTXV 2N3749

FEATURES

- Meets MIL-S-19500/315
- Collector-Base Voltage: 110V
- Fast Switching: $t_r, t_f = 300\text{nSec max}$
- Low Saturation Voltage: 0.25V max @ 1A

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply, pulse amplifier and similar high efficiency power switching applications.

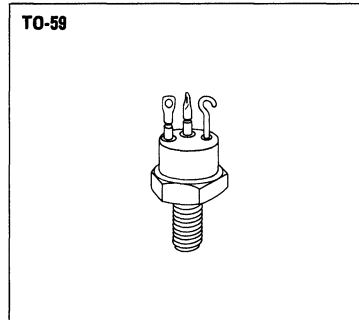
ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	110V
Collector-Emitter Voltage, V_{CEO}	80V
Emitter-Base Voltage, V_{EBO}	8V
D.C. Collector Current, I_C	5A
Power Dissipation	
25°C Ambient	2W
100°C Case	30W
Operating and Storage Temperature Range	-65°C to +200°C

MECHANICAL SPECIFICATIONS

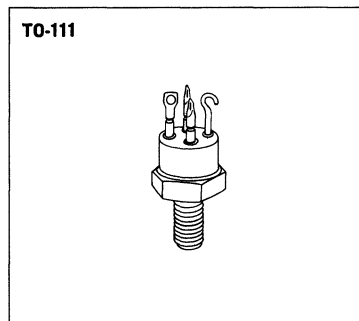
JAN, JANTX, & JANTXV 2N2880

	INCHES	MILLIMETERS
A	400 - 455	10.16 - 11.56
B	090 - 150	2.28 - 3.81
C	320 - 468	8.13 - 11.88
D	570 - 763	14.48 - 19.38
E	318 - 380	8.07 - 9.65
F	055 ± 0.010 015	1.40 ± 0.254 381
G	424 - 437	10.77 - 11.10
H	185 - 215	4.70 - 5.46



JAN, JANTX, & JANTXV 2N3749

	INCHES	MILLIMETERS
A	400 - 455	10.16 - 11.55
B	090 - 250	2.28 - 6.35
C	320 - 468	8.13 - 11.88
D	570 - 763	14.48 - 19.38
E	065 - 090	1.65 - 2.28
F	313 - 318	7.95 - 8.07
G	070 - 090	1.77 - 2.28
H	423 - 438	10.74 - 11.12
J	135 - 215	3.43 - 5.46

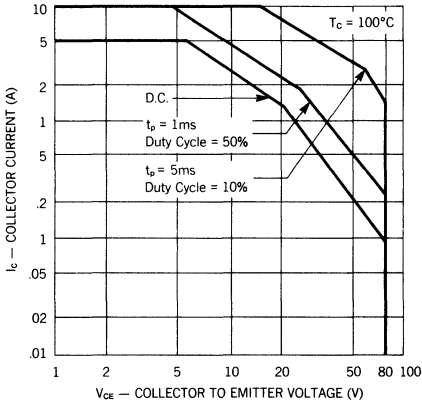


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

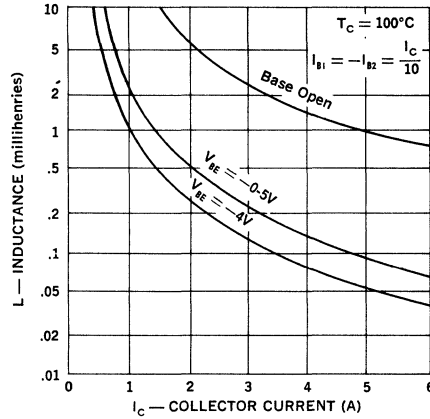
TEST	SYMBOL	MIN.	MAX.	UNITS	/315 Sub group	MIL - STD - 750	
						METHOD	TEST CONDITIONS
Visual and Mechanical	—	—	—	—	A-1	2071	See Mechanical Data
Collector-Base Voltage	BV_{CBO}	110	—	Vdc	A-2	3001	$I_C = 10\mu\text{Adc}$, Cond. D $I_C = 0.1\text{Adc}$, Cond. D $I_E = 10\mu\text{Adc}$, Cond. D $V_{CE} = 60\text{Vdc}$, Cond. D $V_{CE} = 110\text{Vdc}$, $V_{EB} = 0.5\text{Vdc}$, Cond. A $V_{CB} = 80\text{Vdc}$, Cond. D $V_{EB} = 6\text{Vdc}$, Cond. D
Collector-Emitter Voltage (1.)	BV_{CEO}	80	—	Vdc	A-2	3011	
Emitter-Base Voltage	BV_{EBO}	8	—	Vdc	A-2	3026	
Collector-Emitter Cutoff Current	I_{CEO}	—	100	μAdc	A-2	3041	
Collector-Emitter Cutoff Current	I_{CEX}	—	10	μAdc	A-2	3041	
Collector-Base Cutoff Current	I_{CBO}	—	0.4	μAdc	A-2	3036	
Emitter-Base Cutoff Current	I_{EBO}	—	0.4	μAdc	A-2	3061	
D.C. Current Gain (1.)	h_{FE}	40	—	—	A-3	3076	$I_C = 50\text{mAdc}$, $V_{CE} = 5\text{Vdc}$ $I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$ $I_C = 5\text{Adc}$, $V_{CE} = 5\text{Vdc}$ $I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$ $I_C = 5\text{Adc}$, $I_B = 0.5\text{Adc}$ $I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$ $I_C = 1\text{Adc}$, $V_{CE} = 2\text{Vdc}$
D.C. Current Gain (1.)	h_{FE}	40	120	—	A-3	3076	
D.C. Current Gain (1.)	h_{FE}	15	—	—	A-3	3076	
Collector Saturation Voltage (1.)	$V_{CE(sat)}$	—	0.25	Vdc	A-3	3071	
Collector Saturation Voltage (1.)	$V_{CE(sat)}$	—	1.5	Vdc	A-3	3071	
Base Saturation Voltage (1.)	$V_{BE(sat)}$	—	1.2	Vdc	A-3	3066	
Base On-Voltage (1.)	$V_{BE(on)}$	—	1.2	Vdc	A-3	3066	
A.C. Current Gain	h_{FE}	40	120	—	A-4	3206	$I_C = 50\text{mAdc}$, $V_{CE} = 5\text{Vdc}$, $f = 1\text{KHz}$ $I_C = 1\text{Adc}$, $V_{CE} = 10\text{Vdc}$, $f = 10\text{MHz}$ $V_{CB} = 10\text{Vdc}$, $I_E = 0$, $f = 1\text{MHz}$ } See Switching Speed Circuit
Gain-Bandwidth Product	f_T	20	120	MHz	A-4	3306	
Output Capacitance	C_{ob}	—	150	pf	A-4	3236	
Switching Parameters							
Delay Time	t_d	—	60	ns	A-4	—	
Rise Time	t_r	—	300	ns	A-4	—	
Storage Time	t_s	—	1.7	μs	A-4	—	
Fall Time	t_f	—	300	ns	A-4	—	
Thermal Resistance	θ_{JC}	—	3.33	°C/W	C-1	3151	
100°C Forward-Biased Second Breakdown	$I_{S/B}$	5	—	Adc	B-5	3051	$V_{CE} = 6\text{Vdc}$, $t = 60\text{Sec}$, $T_C = 100^\circ\text{C}$ $V_{CE} = 80\text{Vdc}$, $t = 60\text{Sec}$, $T_C = 100^\circ\text{C}$ $I_C = 5\text{A}$, $L = 1\text{mH}$, $V_{Clamp} = 110\text{V}$, $T_C = 100^\circ\text{C}$
Forward-Biased Second Breakdown	$I_{S/B}$	80	—	mAdc	B-5	3051	
Clamped Reverse-Biased Second Breakdown	$E_{S/B}$	12.5	—	mj	B-7	—	
Unclamped Revers. -Biased Second Breakdown	$E_{S/B}$	12.5	—	mj	B-6	3053	$I_C = 5\text{A}$, $L = 1\text{mH}$ Base Open $I_C = 1.6\text{A}$, $L = 10\text{mH}$ Base Open
Unclamped Reverse-Biased Second Breakdown	$E_{S/B}$	12.8	—	mj	B-6	3053	
150°C Collector-Emitter Cutoff Current	I_{CEX}	—	50	μA	A-5	3041	$V_{CE} = 80\text{Vdc}$, $V_{EB} = 0.5\text{Vdc}$ Cond. A, $T_A = 150^\circ\text{C}$
-65°C D.C. Current Gain (1.)	h_{FE}	15	—	—	A-5	3076	$I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$ $T_A = -65^\circ\text{C}$

Note 1. Pulse Width = 300 μSec , duty cycle $\leq 2\%$

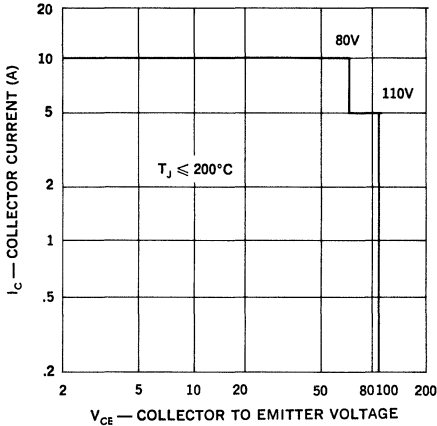
**Forward Bias
 Safe Operating Area**



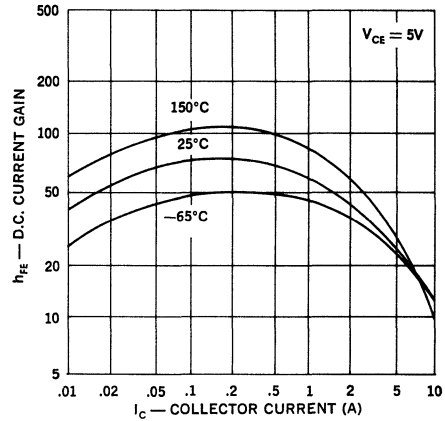
**Unclamped Reverse Bias
 Second Breakdown**



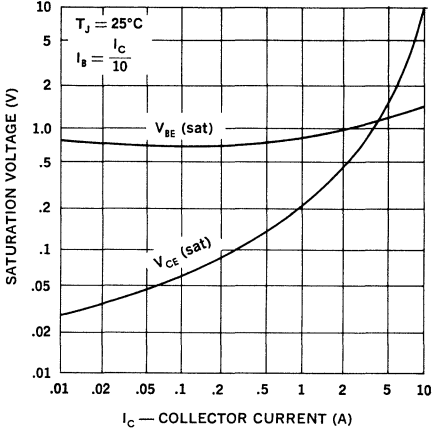
**Reverse Bias
 Safe Operating Area
 Clamped Inductive Switching**



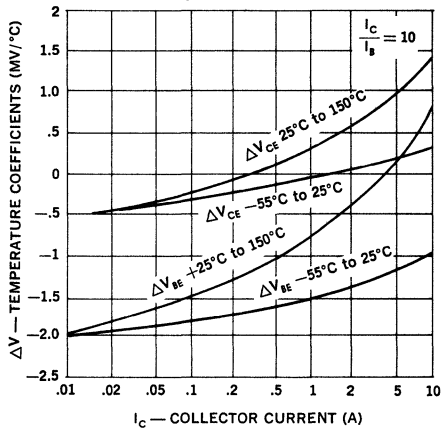
**D.C. Current Gain
 2N2880-2N3749**



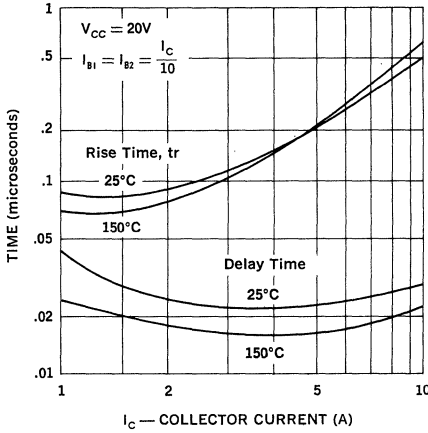
Saturation Voltages



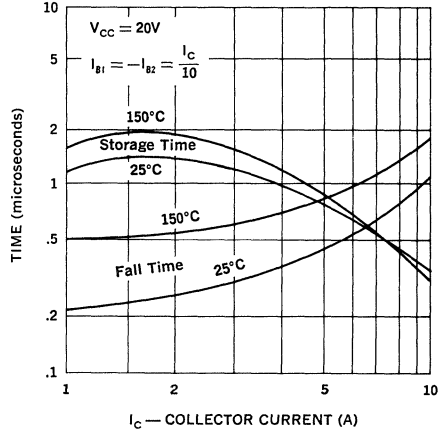
**Saturation Voltage
 Temperature Coefficients**



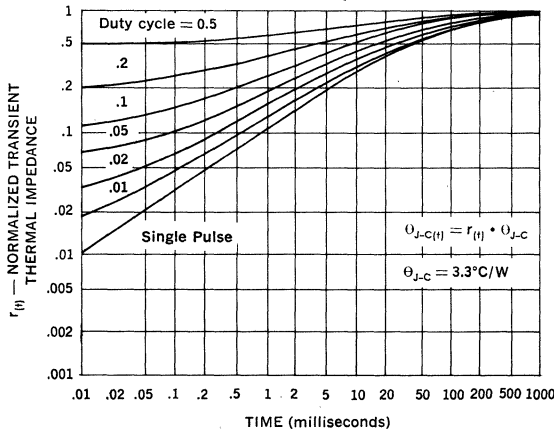
Switching Speed Characteristics



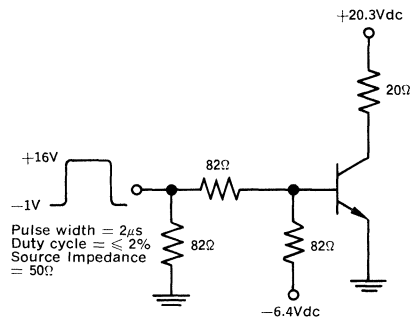
Switching Speed Characteristics



Thermal Response



Switching Speed Circuit



NOTES:

1. $I_C \approx 1A$, $I_{B1} \approx -I_{B2} \approx 100mA$
2. The values of collector current and base current are nominal. The actual values will vary slightly with transistor parameters.

POWER TRANSISTORS

3 Amp, 80V, Planar NPN

JAN, JANTX, & JANTXV 2N3418
 JAN, JANTX, & JANTXV 2N3419
 JAN, JANTX, & JANTXV 2N3420
 JAN, JANTX, & JANTXV 2N3421

FEATURES

- Meets MIL-S-19500/393
- Collector-Base Voltage: up to 125V
- Peak Collector Current: 5A
- High Power Dissipation in TO-5:
 15W @ $T_C = 100^\circ\text{C}$
- Fast Switching

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain, and fast switching. They are ideally suited for power supply, pulse amplifier and similar high frequency power switching applications.

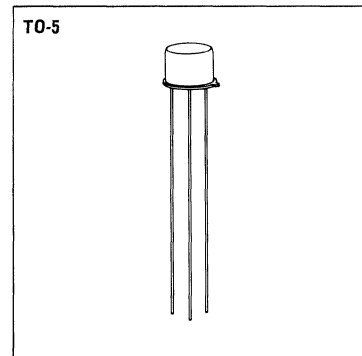
ABSOLUTE MAXIMUM RATINGS

	JAN, JANTX, & JANTXV		JAN, JANTX, & JANTXV	
	2N3418 2N3420		2N3419 2N3421	
Collector-Base Voltage, V_{CBO}	85V		125V	
Collector-Emitter Voltage, V_{CEO}	60V		80V	
Emitter-Base Voltage, V_{EBO}	8V		8V	
D.C. Collector Current, I_C	3A		3A	
Peak Collector Current, I_C	5A		5A	
Power Dissipation				
25°C Ambient	1.0W		1.0W	
100°C Case	15W		15W	
Operating and Storage Temperature Range	-65°C to +200°C			

MECHANICAL SPECIFICATIONS

JAN, JANTX, & JANTXV 2N3418-2N3421

	INCHES	MILLIMETERS
A	335-370	8.51-9.40
B	305-335	7.75-8.51
C	240-260	6.09-6.60
D	1.5 MIN	38.10 MIN
E	0.10-0.30	2.54-7.62
F	0.17 ± 0.02 0.01	4.32 ± 0.51 0.25
G	200	5.08
H	100	2.54
J	0.31 ± 0.03	7.87 ± 0.76
K	0.29-0.45	7.36-11.4
L	100	2.54

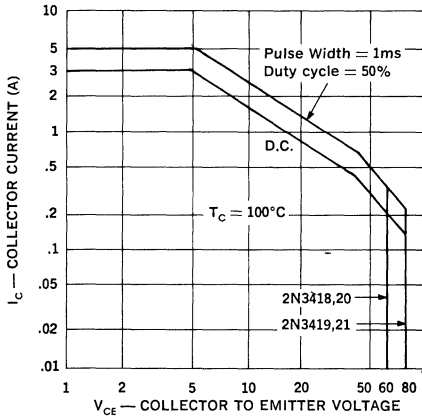


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

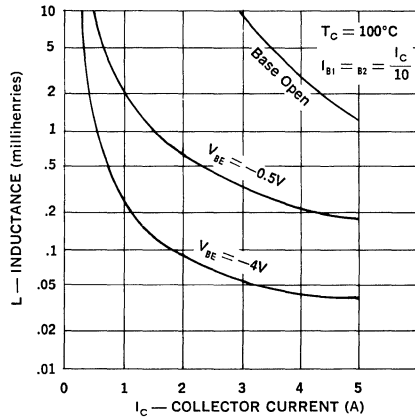
TEST	SYMBOL	MIN.	MAX.	UNITS	/393 Sub-group	MIL - STD - 750	
						METHOD	TEST CONDITIONS
Visual and Mechanical	—	—	—	—	A-1	2071	See Mechanical Data
Collector-Emitter Breakdown Voltage (1.) 2N3418, 2N3420 2N3419, 2N3421	V_{CEO}	60 80	— —	Vdc Vdc	A-2	3011	$I_C = 50\text{mAdc}$, Cond. D
Collector-Emitter Cutoff Current 2N3418, 2N3420 2N3419, 2N3421	I_{CEX}	— —	0.5 0.5	μAdc μAdc	A-2	3041	$V_{EB} = 0.5\text{Vdc}$, Cond. A $V_{CE} = 80\text{Vdc}$ $V_{CE} = 120\text{Vdc}$
Collector-Emitter Cutoff Current 2N3418, 2N3420 2N3419, 2N3421	I_{CEO}	— —	5.0 5.0	μAdc μAdc	A-2	3041	Cond. D $V_{CE} = 45\text{Vdc}$ $V_{CE} = 60\text{Vdc}$
Emitter-Base Cutoff Current	I_{EBO}	—	0.5	μAdc	A-2	3061	$V_{EB} = 6\text{Vdc}$, Cond. D
Emitter-Base Cutoff Current	I_{EBO}	—	10	μAdc	A-2	3061	$V_{EB} = 8\text{Vdc}$, Cond. D
D.C. Current Gain (1.) 2N3418, 2N3419 2N3420, 2N3421	h_{FE}	20 40	— —	— —	A-3	3076	$I_C = 100\text{mAdc}$, $V_{CE} = 2\text{Vdc}$
D.C. Current Gain (1.) 2N3418, 2N3419 2N3420, 2N3421	h_{FE}	20 40	60 120	— —	A-3	3076	$I_C = 1\text{Adc}$, $V_{CE} = 2\text{Vdc}$
D.C. Current Gain (1.) 2N3418, 2N3419 2N3420, 2N3421	h_{FE}	15 30	— —	— —	A-3	3076	$I_C = 2\text{Adc}$, $V_{CE} = 2\text{Vdc}$
D.C. Current Gain (1.) 2N3418, 2N3419 2N3420, 2N3421	h_{FE}	10 15	— —	— —	A-3	3076	$I_C = 5\text{Adc}$, $V_{CE} = 5\text{Vdc}$
Collector-Emitter Saturation Voltage (1.)	$V_{CE(sat)}$	—	0.25	Vdc	A-3	3071	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$
Collector-Emitter Saturation Voltage (1.)	$V_{CE(sat)}$	—	0.5	Vdc	A-3	3071	$I_C = 2\text{Adc}$, $I_B = 0.2\text{Adc}$
Base-Emitter Saturation Voltage (1.)	$V_{BE(sat)}$	0.6	1.2	Vdc	A-3	3066	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$
Base-Emitter Saturation Voltage (1.)	$V_{BE(sat)}$	0.7	1.4	Vdc	A-3	3066	$I_C = 2\text{Adc}$, $I_B = 0.2\text{Adc}$
Gain Bandwidth Product	f_T	40	160	MHz	A-4	3306	$I_C = 0.1\text{Adc}$, $V_{CE} = 10\text{Vdc}$, $f = 20\text{MHz}$
Output Capacitance	C_{ob}	—	150	pf	A-4	3236	$V_{CB} = 10\text{Vdc}$, $I_E = 0$, $f = 1\text{MHz}$
Switching Parameters							
Turn-on Time	t_{on}	—	0.3	μS	A-4	—	$I_C = 1\text{Adc}$, $I_{B1} = -I_{B2} = 0.1\text{Adc}$ See Switching Speed Circuit
Turn-off Time	t_{off}	—	1.2	μS	A-4	—	
100°C							
Forward Biased Second Breakdown	$I_{S/b}$	3	—	Adc	B-6	3005	$V_{CE} = 5\text{Vdc}$, $t = 60\text{sec}$, $T_C = 100^\circ\text{C}$
Forward Biased Second Breakdown	$I_{S/b}$	1	—	Adc	B-6	3005	$V_{CE} = 15\text{Vdc}$, $t = 60\text{sec}$, $T_C = 100^\circ\text{C}$
Forward Biased Second Breakdown	$I_{S/b}$	0.4	—	Adc	B-6	3005	$V_{CE} = 37\text{Vdc}$, $t = 60\text{sec}$, $T_C = 100^\circ\text{C}$
Forward Biased Second Breakdown	$I_{S/b}$	185 120	— —	mAdc mAdc	B-6	3005	$t = 60\text{sec}$, $T_C = 100^\circ\text{C}$ $V_{CE} = 60\text{Vdc}$ $V_{CE} = 80\text{Vdc}$
Unclamped Reverse Biased Second Breakdown	$E_{S/b}$	45	—	mj	B-7	—	$I_C = 3\text{Adc}$, $L = 10\text{mH}$, Base Open
Clamped Reverse Biased Second Breakdown	$E_{S/b}$	180	—	mj	B-8	—	$I_C = 3\text{Adc}$, $L = 40\text{mH}$, $V_{clamp} = \text{Rated } V_{CBO}$
150°C							
Collector-Emitter Cutoff Current 2N3418, 2N3420 2N3419, 2N3421	I_{CEX}	— —	50 50	μAdc μAdc	A-5	3041	$V_{EB} = 0.5\text{Vdc}$, Cond. A, $T_A = 150^\circ\text{C}$ $V_{CE} = 80\text{Vdc}$, $V_{CE} = 120\text{Vdc}$,
—55°C							
D.C. Current Gain (1.)	h_{FE}	10	—	—	A-5	3076	$I_C = 1\text{Adc}$, $V_{CE} = 2\text{Vdc}$, $T_A = -55^\circ\text{C}$

Note: 1. Pulse width = 300 μSec , duty cycle \leq 2%.

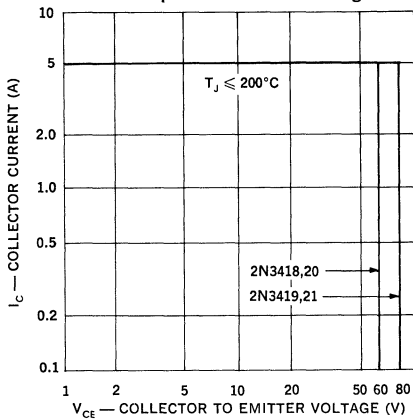
**Forward Bias
Safe Operating Area**



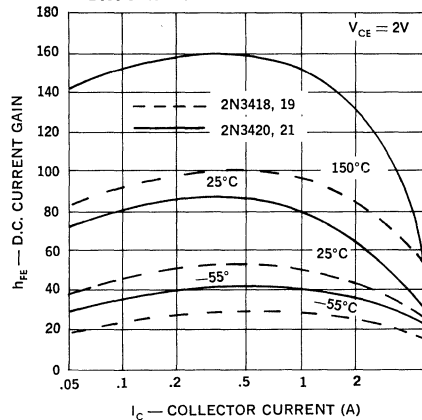
**Unclamped Reverse Bias
Second Breakdown**



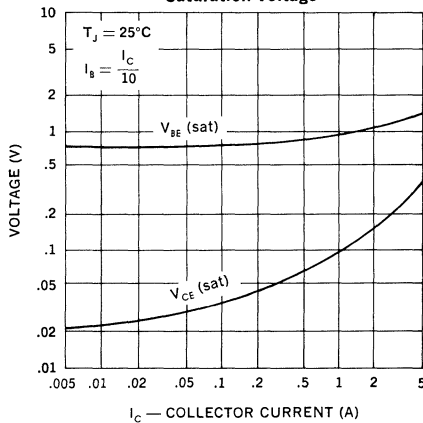
**Reverse Bias
Safe Operating Area
Clamped Inductive Switching**



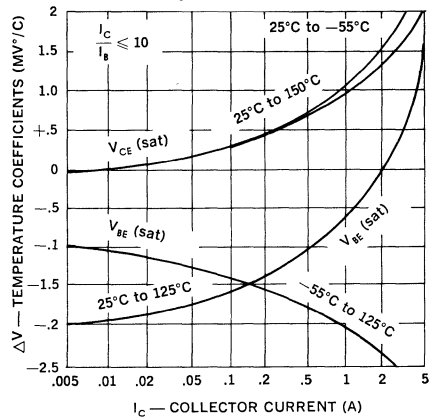
D.C. Current Gain Vs. Collector Current



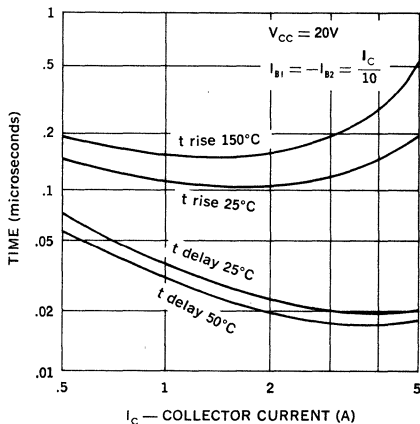
Saturation Voltage



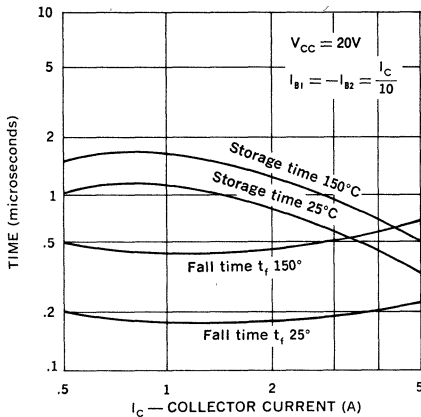
**Saturation Voltage
Temperature Coefficients**



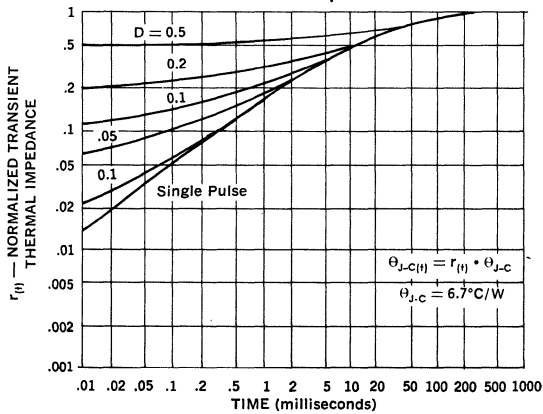
Switching Speed Characteristics



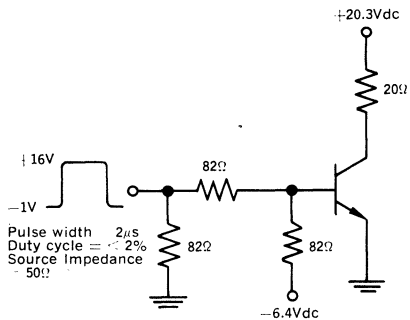
Switching Speed Characteristics



Thermal Response



Switching Speed Circuit



POWER TRANSISTORS

5 Amp, 80V, Planar NPN

JAN, JANTX, & JANTXV 2N3996
 JAN, JANTX, & JANTXV 2N3997
 JAN, JANTX, & JANTXV 2N3998
 JAN, JANTX, & JANTXV 2N3999

FEATURES

- Meets MIL-S-19500/374*
- Collector-Base Voltage: Up to 100V
- D.C. Collector Current: 5A
- Fast Switching
- Beta Guaranteed at 3 Current Levels

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

4

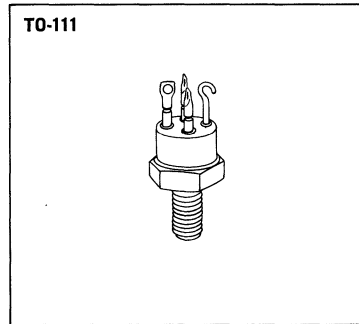
ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	100V
Collector-Emitter Voltage, V_{CER}	80V
Emitter-Base Voltage, V_{EBO}	8V
D.C. Collector Current, I_C	5A
Peak Collector Current, I_{c}	10A
Power Dissipation	
25°C Ambient	2W
100°C Case	30W
Operating and Storage Temperature Range	-65°C to 200°C

MECHANICAL SPECIFICATIONS

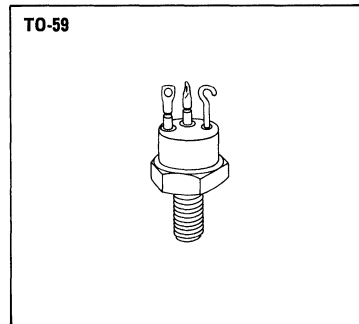
JAN, JANTX, & JANTXV 2N3996, 2N3997

	INCHES	MILLIMETERS
A	400 - 455	10.16 - 11.55
B	090 - 250	2.28 - 6.35
C	320 - 468	8.13 - 11.88
D	570 - 763	14.48 - 19.38
E	065 - 090	1.65 - 2.28
F	313 - 318	7.95 - 8.07
G	070 - 090	1.77 - 2.28
H	423 - 438	10.74 - 11.12
J	135 - 215	3.43 - 5.46



JAN, JANTX, & JANTXV 2N3998, 2N3999

	INCHES	MILLIMETERS
A	400-455	10.16-11.56
B	090-150	2.28-3.81
C	320-468	8.13-11.88
D	570-763	14.48-19.38
E	318-380	8.07-9.65
F	055 ± 010 015	1.40 ± .254 381
G	424-437	10.77-11.10
H	185-215	4.70-5.46



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

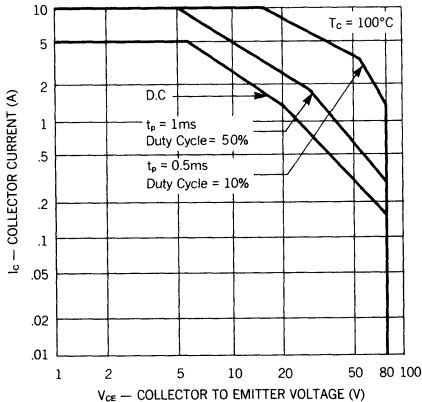
Test	Symbol	2N3996* 2N3998*		2N3997* 2N3999*		Units	Test Conditions	
		Min.	Max.	Min.	Max.			
D.C. Current Gain	h_{FE}	30	—	60	—	—	$I_C=50\text{ mA}, V_{CE}=2\text{V}$	
D.C. Current Gain (Note 1)	h_{FE}	40	120	80	240	—	$I_C=1\text{A}, V_{CE}=2\text{V}$	
D.C. Current Gain (Note 1)	h_{FE}	15	—	20	—	—	$I_C=5\text{A}, V_{CE}=5\text{V}$	
D.C. Current Gain, -55°C (Note 1)	h_{FE}	10	—	20	—	—	$I_C=1\text{A}, V_{CE}=2\text{V}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})$	—	0.25	—	0.25	V	$I_C=1\text{A}, I_B=100\text{ mA}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})$	—	2	—	2	V	$I_C=5\text{A}, I_B=500\text{ mA}$	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})$	0.6	1.2	0.6	1.2	V	$I_C=1\text{A}, I_B=100\text{ mA}$	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})$	—	1.6	—	1.6	V	$I_C=5\text{A}, I_B=500\text{ mA}$	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}	80	—	80	—	V	$I_C=50\text{ mA}, I_B=0$	
Emitter-Base Cutoff Current	I_{EBO}	—	0.2	—	0.2	μA	$V_{BE}=5\text{V}, I_C=0$	
Emitter-Base Cutoff Current	I_{EBO}	—	10	—	10	μA	$V_{BE}=8\text{V}, I_C=0$	
Collector Cutoff Current	I_{CES}	—	5	—	5	μA	$V_{CE}=90\text{V}, R_{BE}=0$	
Collector Cutoff Current	I_{CEO}	—	10	—	10	μA	$V_{CE}=60\text{V}, I_B=0$	
Collector Cutoff Current, 150°C	I_{CES}	—	50	—	50	μA	$V_{CE}=90, R_{BE}=0$	
Collector Capacitance	C_{ob}	—	150	—	150	pf	$V_{CB}=10\text{V}, I_E=0, f=1\text{ MHz}$	
A.C. Current Gain (High Frequency)	h_{fe}	4	—	4	—	—	$I_C=1\text{A}, V_{CE}=5\text{V}, f=10\text{ MHz}$	
Switching Speeds	Turn-on Time	t_{on}	—	0.3	—	0.3	μS	$I_C=1\text{A}$
	Turn-off Time	t_{off}	—	1.5	—	2	μS	$I_{B1}=100\text{mA}, I_{B2}= -100\text{ mA}$

Notes:

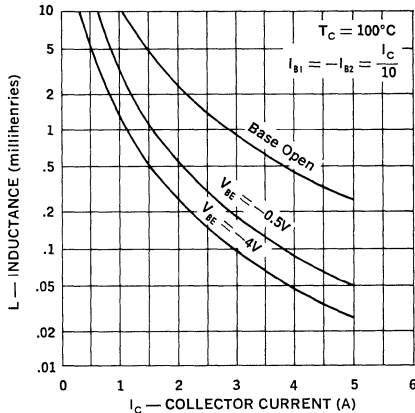
- 1. Pulse width = 300 μS ; duty cycle $\leq 2\%$.
- † All values in this table are JEDEC registered.

*Also applicable to JAN and JANTX versions

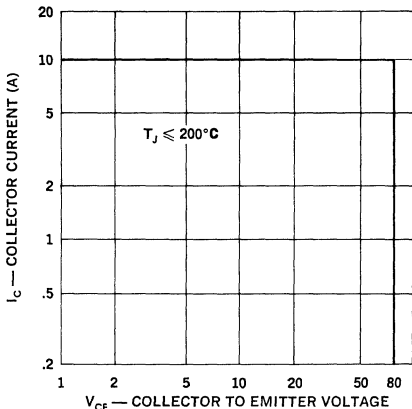
**Forward Bias
Safe Operating Area**



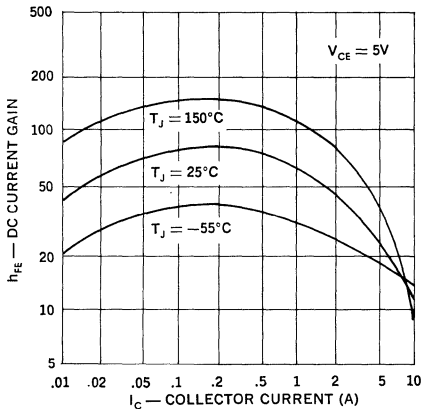
**Unclamped Reverse Bias
Second Breakdown**



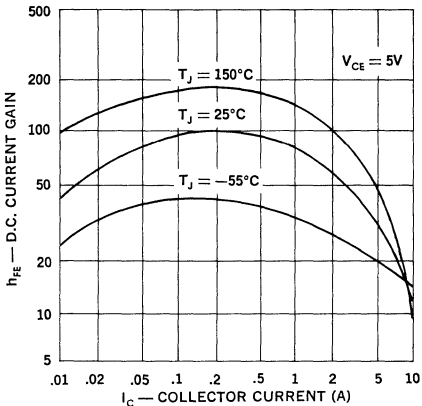
**Reverse Bias
Safe Operating Area
Clamped Inductive Switching**



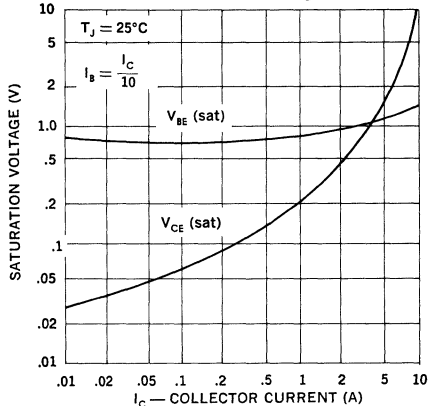
**D.C. Current Gain
2N3996-2N3998**



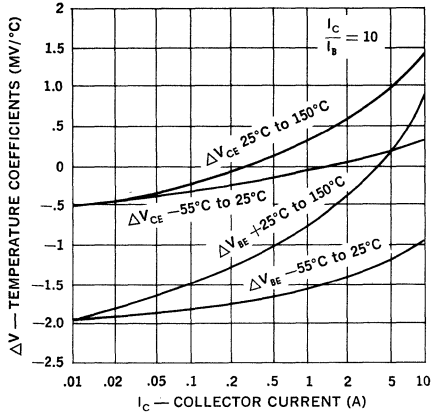
**D.C. Current Gain
2N3997-2N3999**



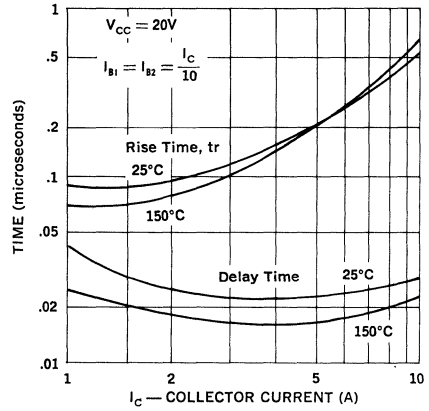
Saturation Voltage



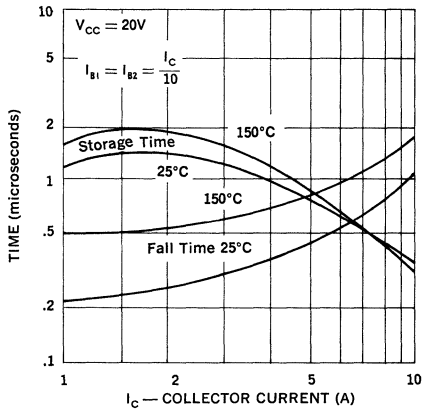
**Saturation Voltage
Temperature Coefficients**



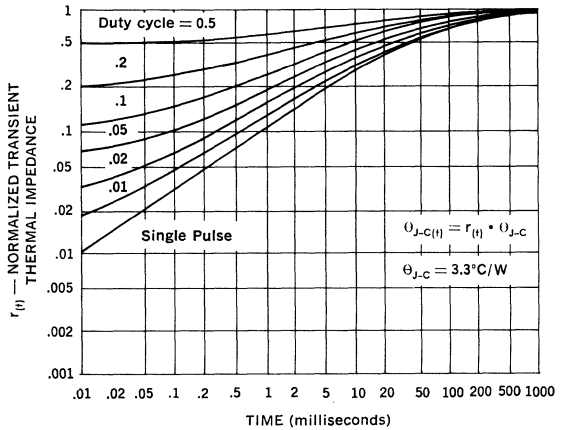
**Switching Speed
Characteristics**



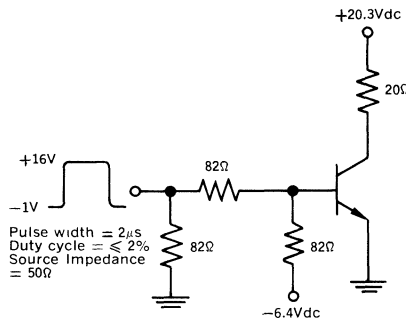
**Switching Speed
Characteristics**



Thermal Response



Switching Speed Circuit



NOTES:

1. $I_C \approx 1A$, $I_{B1} \approx -I_{B2} \approx 100mA$
2. The values of collector current and base current are nominal. The actual values will vary slightly with transistor parameters.

POWER TRANSISTORS

10 Amp, 70V, Planar NPN

JAN, JANTX & JANTXV 2N4150

FEATURES

- Meets MIL-S-19500/394
- Collector-Base Voltage: up to 100V
- Peak Collector Current: 10A
- Fast Switching
- Low Saturation Voltage

DESCRIPTION

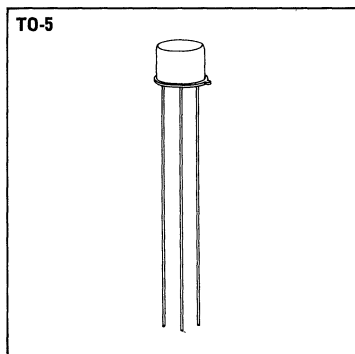
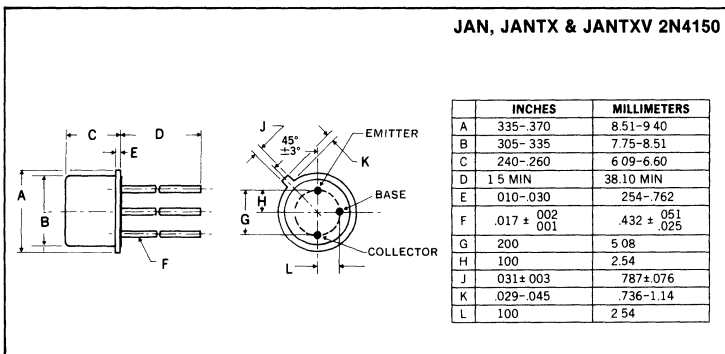
Unijunction power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

4

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	100V
Collector-Emitter Voltage, V_{CEO}	70V
Emitter-Base Voltage, V_{EBO}	7V
Peak Collector Current, I_C	10A
Power Dissipation	
25°C Ambient	1.5W
100°C Case	5W
Operating and Storage Temperature Range	-65°C to 200°C

MECHANICAL SPECIFICATIONS

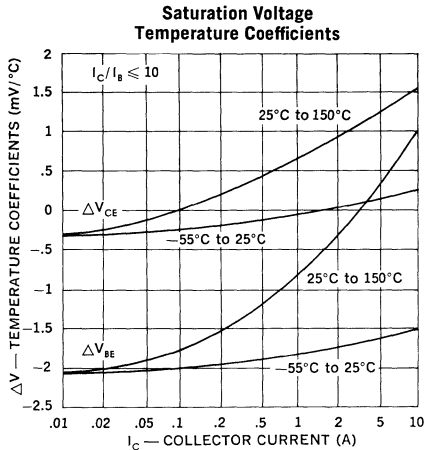
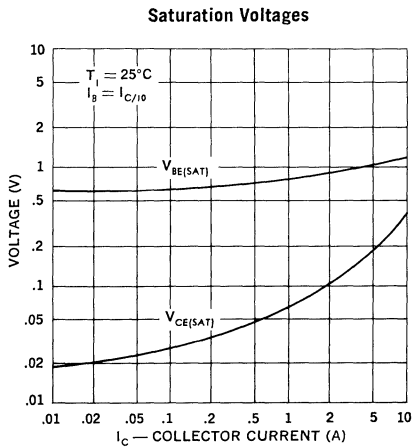
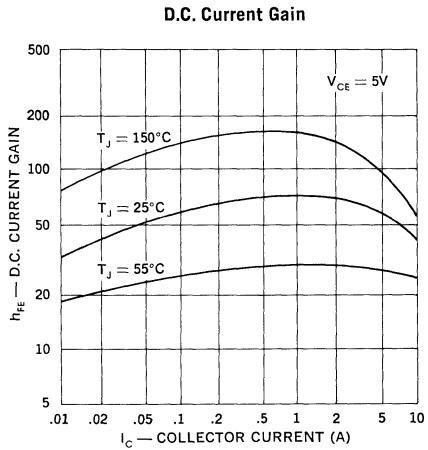
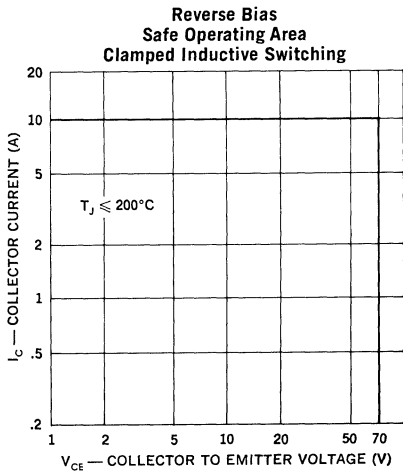
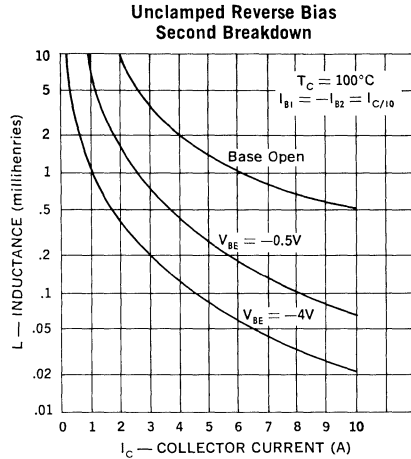
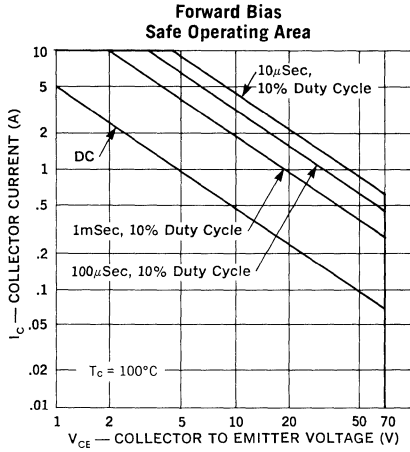


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

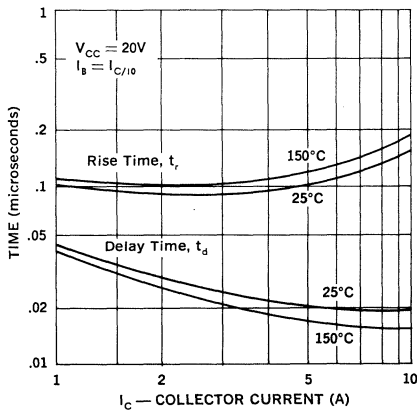
Test		Symbol	Min.	Max.	Units	/394 Sub group	Method	MIL-STD-750
								Test conditions
Visual and Mechanical						A-1	2071	See Mechanical Data
25°C								
Collector-Base Breakdown Voltage		BV_{CBO}	100	—	Vdc	A-2	3001	$I_C = 10\mu\text{Adc}$; Cond. D
Collector-Emitter Breakdown Voltage (Note 1)		BV_{CEO}	70	—	Vdc	A-2	3011	$I_C = 0.1\text{Adc}$; Cond. D
Emitter-Base Breakdown Voltage		BV_{EBO}	7	—	Vdc	A-2	3026	$I_E = 10\mu\text{Adc}$; Cond. D
Collector-Emitter Cutoff Current		I_{CEO}	—	10	μAdc	A-2	3041	$V_{CE} = 60\text{Vdc}$; Cond. D
Collector-Emitter Cutoff Current		I_{CEX}	—	10	μAdc	A-2	3041	$V_{CE} = 100\text{Vdc}$, $V_{EB} = 0.5\text{Vdc}$; Cond. A
Collector-Base Cutoff Current		I_{CBO}	—	0.1	μAdc	A-2	3036	$V_{CB} = 80\text{Vdc}$; Cond. D
Emitter-Base Cutoff Current		I_{EBO}	—	0.1	μAdc	A-2	3061	$V_{EB} = 5\text{Vdc}$; Cond. D
D.C. Current Gain (Note 1)		h_{FE}	40	120	—	A-3	3076	$I_C = 5\text{Adc}$, $V_{CE} = 5\text{Vdc}$
D.C. Current Gain (Note 1)		h_{FE}	10	—	—	A-3	3076	$I_C = 10\text{Adc}$, $V_{CE} = 5\text{Vdc}$
D.C. Current Gain (Note 1)		h_{FE}	50	—	—	A-3	3076	$I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$
Collector Saturation Voltage (Note 1)		$V_{CE}(\text{sat})$	—	0.6	Vdc	A-4	3071	$I_C = 5\text{Adc}$, $I_B = 0.5\text{Adc}$
Collector Saturation Voltage (Note 1)		$V_{CE}(\text{sat})$	—	2.5	Vdc	A-4	3071	$I_C = 10\text{Adc}$, $I_B = 1\text{Adc}$
Base Saturation Voltage (Note 1)		$V_{BE}(\text{sat})$	—	1.5	Vdc	A-4	3066	$I_C = 5\text{Adc}$, $I_B = 0.5\text{Adc}$; Cond. A
Base Saturation Voltage (Note 1)		$V_{BE}(\text{sat})$	—	2.5	Vdc	A-4	3066	$I_C = 10\text{Adc}$, $I_B = 1\text{Adc}$; Cond. A
A.C. Current Gain		h_{fe}	40	160	—	A-4	3206	$I_C = 50\text{mAdc}$, $V_{CE} = 5\text{Vdc}$, $f = 1\text{KHz}$
Gain-Bandwidth Product		f_T	15	75	MHz	A-4	3306	$I_C = 0.2\text{Adc}$, $V_{CE} = 10\text{Vdc}$, $f = 10\text{MHz}$
Output Capacitance		C_{ob}	—	350	pf	A-4	3236	$V_{CB} = 10\text{Vdc}$, $I_E = 0$, $f = 1\text{MHz}$
Thermal Resistance		θ_{J-C}	—	20	$^{\circ}\text{C}/\text{W}$	C-1	3151	
Switching Speeds	Delay Time	t_d	—	50	ns	A-4	—	$V_{CC} = 20\text{V}$ $I_C = 5\text{A}$ $I_{B1} = I_{B2}$, $I_{B1} = 0.5\text{A}$
	Rise Time	t_r	—	500	ns	A-4	—	
	Storage Time	t_s	—	1.5	μs	A-4	—	
	Fall Time	t_f	—	500	ns	A-4	—	
100°C								
Forward-Biased Second Breakdown		$I_{S/I}$	5	—	Adc	B-6	3005	$V_{CE} = 1\text{Vdc}$, $t = 60\text{Sec}$,
Forward-Biased Second Breakdown		$I_{S/B}$	70	—	mAdc	B-6	3005	$V_{CE} = 1\text{Vdc}$, $t = 60\text{Sec}$,
Unclamped Reverse Biased Second Breakdown		$E_{S/B}$	12.5	—	mj	B-7	—	$I_C = 5\text{Adc}$, $L = 1\text{mh}$
Clamped Reverse Biased Second Breakdown		$E_{S/B}$	200	—	mj	B-8	—	$I_C = 5\text{Adc}$, $L = 40\text{mh}$, $V_{clamp} = 70\text{V}$
150°C								
Collector-Emitter Cutoff Current		I_{CEX}	—	100	μAdc	A-5	3041	$V_{CE} = 80\text{Vdc}$, $V_{EB} = 0.5\text{Vdc}$, Cond. A
−55°C								
D.C. Current Gain (Note 1)		h_{FE}	20	—	—	A-5	3076	$I_C = 5\text{Adc}$, $V_{CE} = 5\text{Vdc}$

Note:

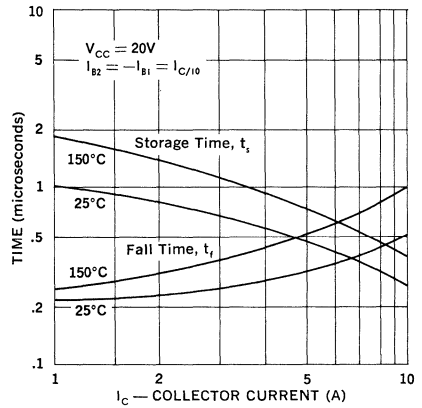
1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.



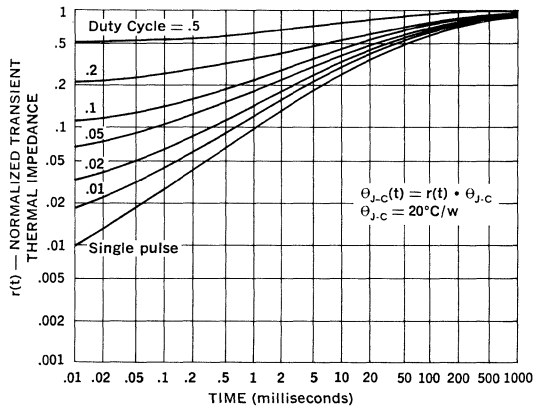
Switching Speed Characteristics



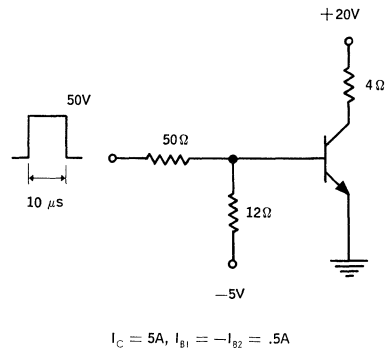
Switching Speed Characteristics



Thermal Response



Switching Speed Circuit



POWER TRANSISTORS

20 Amp, 150V, Double Diffused
NPN Mesa

JAN, JANTX, JANTXV 2N5038
JAN, JANTX, JANTXV 2N5039

4

FEATURES

- Collector-Base Voltage: up to 150V
- Peak Collector Current: 30A
- t_{on} Time ≤ 500 nS
- t_{off} Time ≤ 2 μ S
- Qualified to MIL-S-19500/439

DESCRIPTION

These MIL approved double diffused glass passivated mesa power transistors combine fast-switching, low saturation voltage and rugged E_{sb} capability. They are designed for use in switching regulators, converters, inverters and switching-control amplifiers.

ABSOLUTE MAXIMUM RATINGS

	JAN, JANTX & JANTXV 2N5038	JAN, JANTX & JANTXV 2N5039
Collector-Base Voltage, V_{CBO}	150V	125V
Collector-Emitter Sustaining Voltage, V_{CER} (SUS) (1)	110V	95V
V_{CEO} (SUS)	90V	75V
Emitter-Base Voltage, V_{EBO}	7V	7V
Collector Current, I_C continuous	20A	20A
Collector Current, I_{CM} peak	30A	30A
Base Current, I_B continuous	5A	5A
Power Dissipation, 25°C Case	140W	140W
Operating and Storage Temperature Range	-65 to 200°C	

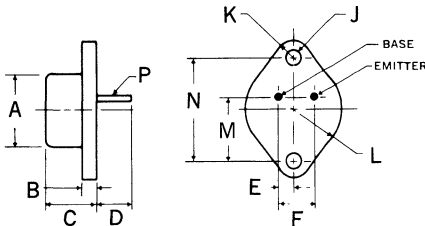
(1) With $R_{BE} \leq 50\Omega$

MECHANICAL SPECIFICATIONS

NOTE:

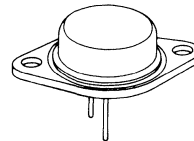
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.

JAN, JANTX, JANTXV 2N5038, 2N5039



	ins.	mm
A	.875 MAX.	2.22 MAX.
B	.135 MAX.	0.34 MAX.
C	.250—450	0.64—1.14
D	.312 MIN.	0.79 MIN.
E	.205—225	0.52—0.57
F	.420—440	1.07—1.12
J	.151—161 DIA.	0.38—0.41
K	.188 MAX. RAD.	0.48 MAX. RAD.
L	.525 MAX. RAD.	1.33 MAX. RAD.
M	.655—675	1.66—1.71
N	1.177—1.197	2.99—3.04
P	.038—.043 DIA.	0.10—0.11 DIA.

TO-204AA (TO-3)



Electrical Specifications (at 25°C unless noted)

Test	Symbol	2N5038		2N5039		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	50	—	30	—	—	$I_C = 0.5, V_{CE} = 5V$
		50	200	30	150		$I_C = 2A, V_{CE} = 5V$
D.C. Current Gain (Note 1)	h_{FE}	—	—	20	—	—	$I_C = 10A, V_{CE} = 5V$
		20	—	—	—		$I_C = 12A, V_{CE} = 5V$
D.C. Current Gain —65°C	h_{FE}	—	—	10	—	—	$I_C = 10A, V_{CE} = 5V$
		10	—	—	—		$I_C = 12A, V_{CE} = 5V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	—	—	1.0	V	$I_C = 10A, I_B = 1.0A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	—	V	$I_C = 12A, I_B = 1.2A$
		—	2.5	—	2.5		$I_C = 20A, I_B = 5A$
Base-Emitter Voltage (Note 1)	V_{BE}	—	—	—	1.8	V	$I_C = 10A, V_{CE} = 5V$
		—	1.8	—	—	V	$I_C = 12A, V_{CE} = 5V$
Collector-Emitter Sustaining Voltage (Notes 2, 3)	$V_{CEO(sus)}$	90	—	75	—	V	$I_C = 0.2A, L = 15mH$
Collector-Emitter Sustaining Voltage (Notes 2, 3)	$V_{CEX(sus)}$	150	—	125	—	V	$I_C = 0.2A, L = 2mH$ $V_{BE} = -1.5V$ $I_B = 0$ $R_{BE} = 100\Omega$
Collector-Emitter Sustaining Voltage (Notes 2, 3)	$V_{CER(sus)}$	110	—	95	—	V	$R_{BE} = 50\Omega, I_C = 0.2A, L = 15mH$
Emitter-Base Voltage	V_{EBO}	7.0	—	7.0	—	V	$I_E = 25mA$
Collector Cutoff Current	I_{CBO}	—	—	—	25	mA	$V_{CB} = 125V$
		—	25	—	—		$V_{CB} = 150V$
Collector Cutoff Current	I_{CEO}	—	—	—	10	mA	$V_{CE} = 55V$
		—	10	—	—		$V_{CE} = 70V$
Collector Cutoff Current	I_{CEX}	—	—	—	5.0	mA	$V_{CE} = 85V, V_{BE} = -1.5V$
		—	5.0	—	—		$V_{CE} = 100V, V_{BE} = -1.5V$
Collector Cutoff Current, 150°C	I_{CEX}	—	—	—	10	mA	$V_{CE} = 85V, V_{BE} = -1.5V$
		—	10	—	—		$V_{CE} = 100V, V_{BE} = -1.5V$
Emitter Cutoff Current	I_{EBO}	—	5.0	—	5.0	mA	$V_{BE} = -5V$
Magnitude of Small Signal Forward — Current Transfer Ratio	$ h_{fo} $	12	48	12	48	—	$V_{CE} = 10V, I_C = 2A, f = 5MHz$
Collector Capacitance	C_{ob}	—	500	—	500	μF	$V_{CB} = 10V, f = 1MHz$
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$	—	1.25	—	1.25	°C/W	$V_{CE} = 10V, I_C = 10A$

Notes:

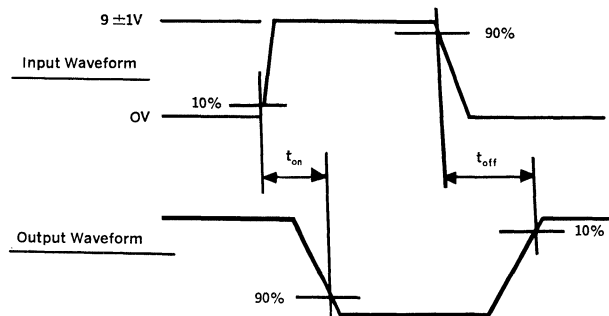
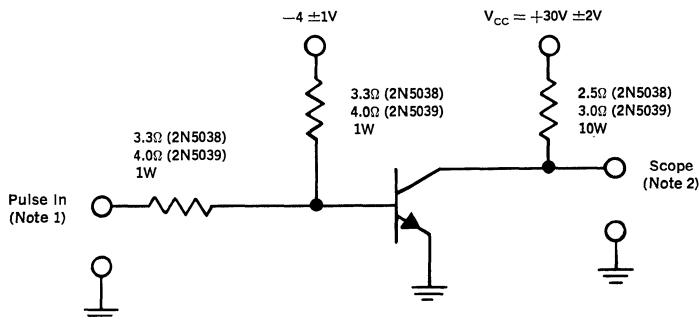
1. Pulse width = 250 μ S; duty cycle \leq 1%.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length \approx 50 μ S; duty cycle \leq 1%. Voltage clamped at maximum collector-emitter voltage.
3. Unclamped inductive load.

Electrical Specifications (at 25°C unless noted)

Test	Symbol	2N5038		2N5039		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
Second Breakdown Energy	$E_{s/b}$ clamped	14	—	14	—	mJ	$I_C = 20\text{Adc}$, $L = 70\mu\text{H}$, 0.1Ω $V_{CC} = 75\text{V}$, 90V $R_L = 3.75\Omega$, 4.5Ω
	$E_{s/b}$ unclamped	5.06	—	5.06	—		$I_C = 4.5\text{Adc}$, $L = 500\mu\text{H}$, 0.1Ω $V_{CC} = 10\text{Vdc}$
Forward Bias Second Breakdown Collector Current	$I_{s/b}$	5.0	—	5.0	—	A	$V_{CE} = 28\text{V}$, $t = 1\text{s}$, non-rep.
		0.9	—	0.9	—		$V_{CE} = 45\text{V}$, $t = 1\text{s}$, non-rep.
Switching Speeds Turn-on Time	t_{on}	—	0.5	—	—	μS	$I_C = 12\text{Adc}$ $I_{B1} = I_{B2} = 1.2\text{Adc}$ $V_{CC} = 30\text{Vdc} \pm 2\text{V}$
Turn-on Time	t_{on}	—	—	—	0.5	μS	$I_C = 10\text{Adc}$ $I_{B1} = I_{B2} = 1\text{Adc}$ $V_{CC} = 30\text{Vdc} \pm 2\text{V}$
Turn-off Time	t_{off}	—	—	—	2.0	μS	$I_C = 10\text{Adc}$ $I_{B1} = I_{B2} = 1.0\text{Adc}$ $V_{CC} = 30\text{Vdc} \pm 2\text{V}$
Turn-off Time	t_{off}	—	2.0	—	—	μS	$I_C = 12\text{Adc}$ $I_{B1} = I_{B2} = 1.2\text{Adc}$ $V_{CC} = 30\text{Vdc} \pm 2\text{V}$

4

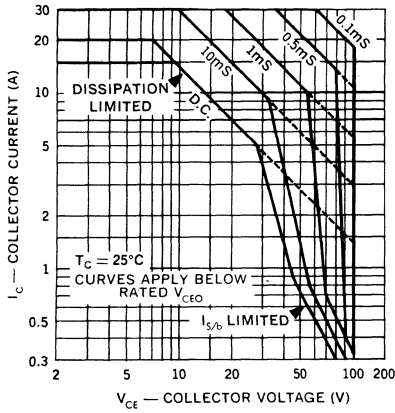
Switching Time Test Circuit



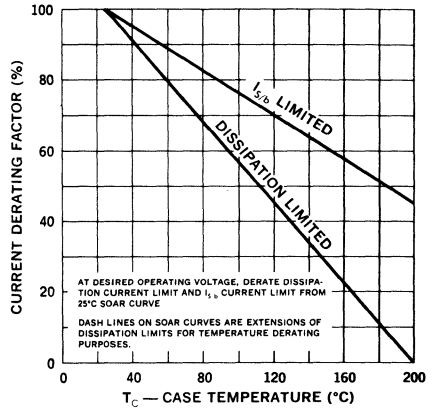
Notes

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 20 nanoseconds; duty cycle $\leq 2\%$; generator source impedance shall be 50 ohms; Pulse width = 20 μs
2. Output sampling oscilloscope: $Z_{in} \geq 100\text{K}$ ohms; $C_{in} \leq 50\text{pf}$; rise time ≤ 20 nanoseconds.

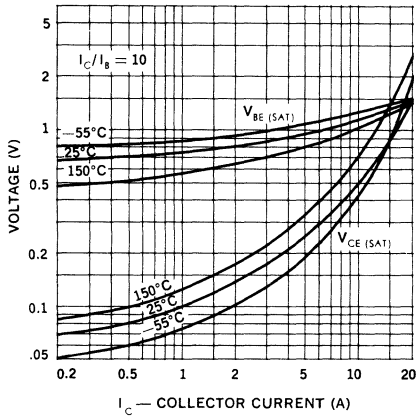
**Forward Bias Safe Operating Area
 for 2N5038 and 2N5039**



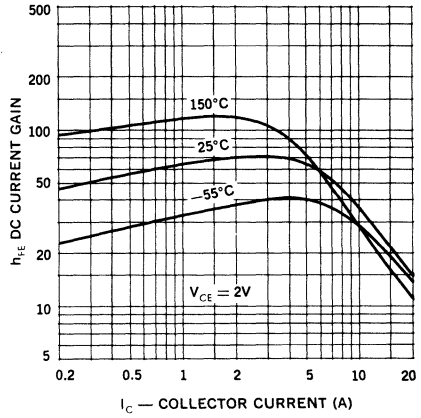
Power Derating



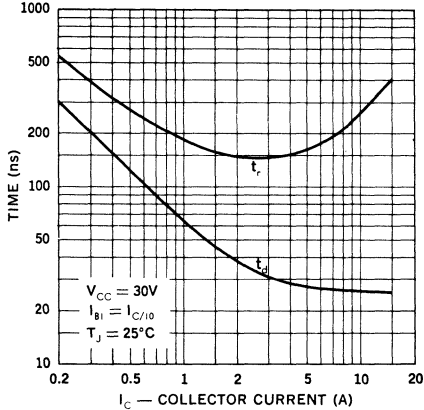
Saturation Voltages



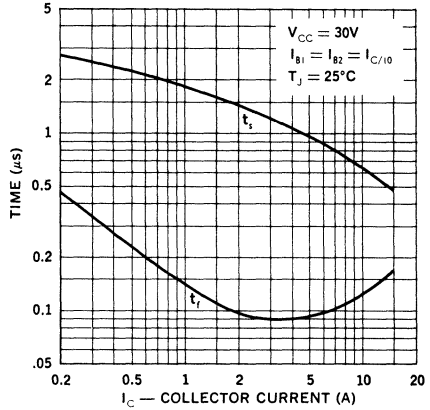
DC Current Gain



Turn-On Time



Turn-Off Time



POWER TRANSISTORS

2N5552 5552-4

10 Amp, 120V, Planar NPN

FEATURES

- Collector-Base Voltage: up to 120V
- Peak Collector Current: 10A
- Fast Switching
- Beta Guaranteed at 3 Current Levels

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

4

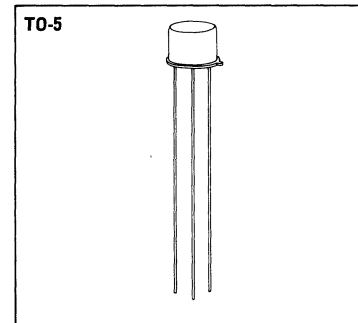
ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	120V
Collector-Emitter Voltage, V_{CEO}	80V
Emitter-Base Voltage, V_{EBO}	7V
D.C. Collector Current, I_C	10A
Power Dissipation	
25°C Ambient	1.25W
100°C Case	1.5W
Operating and Storage Temperature Range	-65°C to 200°C

MECHANICAL SPECIFICATIONS

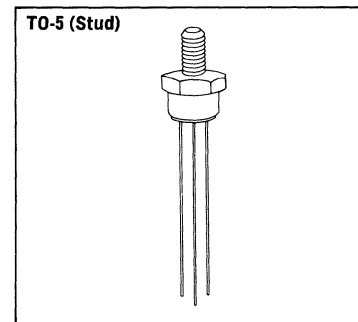
2N5552

	INCHES	MILLIMETERS
A	.335 - .370	8.51 - 9.40
B	.305 - .335	7.75 - 8.51
C	.240 - .260	6.09 - 6.60
D	1.5 MIN.	38.10 MIN.
E	.010 - .030	254 - 762
F	0.17 ± .002 0.001	432 ± .051 0.025
G	.200	5.08
H	.100	2.54
J	.031 ± .003	787 ± 0.76
K	.029 - .045	736 - 1.14
L	.100	2.54



5552-4

	INCHES	MILLIMETERS
A	.340 - .360	8.63 - 9.14
B	.315 - .335	8.00 - 8.51
C	.095 - .115	2.41 - 2.92
D	1.5 MIN.	38.10 MIN.
E	0.17 ± .001	432 ± .0254
F	.337 - .387	9.57 - 9.83
G	.424 - .437	10.77 - 11.10
H	.200	5.08



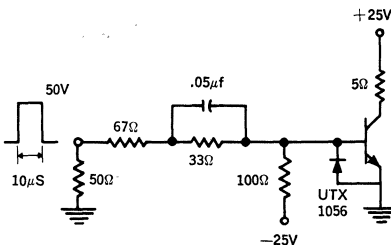
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

Test	Symbol	Min.	Max.	Units	Test Conditions	
D.C. Current Gain	h_{FE}	40	250	—	$I_C = 0.5A, V_{CE} = 2V$	
D.C. Current Gain (Note 2)	h_{FE}	50	150	—	$I_C = 5A, V_{CE} = 5V$	
D.C. Current Gain (Note 2)	h_{FE}	30	—	—	$I_C = 10A, V_{CE} = 5V$	
Collector Saturation Voltage (Note 2)	$V_{CE(sat)}$	—	0.5	V	$I_C = 5A, I_B = 0.5A$	
Collector Saturation Voltage (Note 2)	$V_{CE(sat)}$	—	1.0	V	$I_C = 10A, I_B = 1A$	
Base Saturation Voltage (Note 2)	$V_{BE(sat)}$	—	1.3	V	$I_C = 5A, I_B = 0.5A$	
Base Saturation Voltage (Note 2)	$V_{BE(sat)}$	—	1.8	V	$I_C = 10A, I_B = 1A$	
Collector-Emitter Sustaining Voltage (Note 2)	BV_{CER}	120	—	V	$I_C = 100mA, R_{BE} = 10\Omega$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	80	—	V	$I_C = 100mA, I_B = 0$	
Collector-Emitter Voltage (Note 2)	BV_{CES}	120	—	V	$I_C = 0.2\mu A, R_{BE} = 0$	
Emitter-Base Breakdown Voltage	BV_{EBO}	7	—	V	$I_E = 10\mu A, I_C = 0$	
Collector Cutoff Current	I_{CES}	—	0.2	μA	$V_{CE} = 120V, R_{BE} = 0$	
Collector Cutoff Current, 150°C	I_{CES}	—	0.1	mA	$V_{CE} = 80, R_{BE} = 0, T = 150^\circ C$	
Collector Capacitance	C_{obo}	—	150	pf	$V_{CB} = 10, I_E = 0, f = 1MHz$	
A.C. Current Gain	h_{fe}	3	—	—	$I_C = 0.5A, V_{CE} = 5V, f = 10MHz$	
Switching Speeds	Turn-on Time	t_{on}	—	100	ns	$I_C = 5A$
	Turn-off Time	t_{off}	—	700	ns	$I_{B1} = 250ma, I_{B2} = -250ma$

Notes:

- The device may be switched between maximum rated collector current and maximum rated collector-emitter voltage along a resistive load line provided the switching time is less than 10 microseconds. Switching at low speed through regions of high instantaneous power dissipation may cause second breakdown to occur, with consequent damage to the device.
 - Pulse width = 300 μ s; duty cycle \leq 2%.
- † All values in this table are JEDEC registered.

Switching Speed Circuit



POWER TRANSISTORS

20 Amp, 80V, Planar NPN

2N5658
2N5659

FEATURES

- Collector-Base Voltage: up to 120V
- Peak Collector Current: 20A
- High Gain
- Fast Switching

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage, V_{CBO}	120V
Collector-Emitter Voltage, V_{CEO}	80V
Emitter-Base Voltage, V_{EBO}	7V
Peak Collector Current, I_C	20A
Power Dissipation	
100°C Case	30W
Operating and Storage Temperature Range	-65°C to 200°C

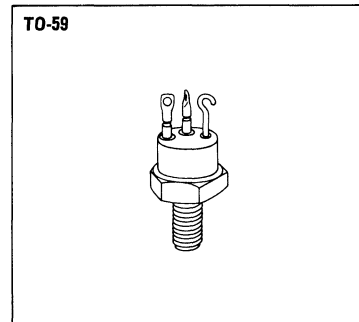
MECHANICAL SPECIFICATIONS

10-32 • NF 2A
THREAD

EMITTER
BASE
COLLECTOR

2N5658

	INCHES	MILLIMETERS
A	400-455	10.16-11.56
B	090-150	2.28-3.81
C	320-468	8.13-11.88
D	570-763	14.48-19.38
E	318-380	8.07-9.65
F	055 ± 010 015	1.40 ± 254 381
G	424-437	10.77-11.10
H	185-215	4.70-5.46



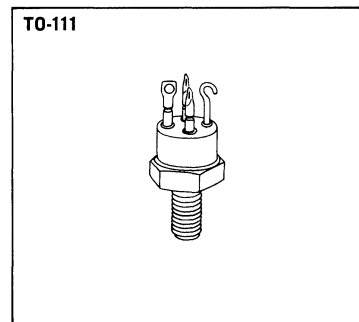
10-32 • NF-2A
THREAD

EMITTER
CASE
COLLECTOR
BASE

2N5659

	INCHES	MILLIMETERS
A	400 - 455	10.16 - 11.55
B	090 - 250	2.28 - 6.35
C	320 - 468	8.13 - 11.88
D	570 - 763	14.48 - 19.38
E	.065 - 090	1.65 - 2.28
F	313 - 318	7.95 - 8.07
G	070 - 090	1.77 - 2.28
H	423 - 438	10.74 - 11.12
J	.135 - 215	3.43 - 5.46

Collector Isolated from Case.



Electrical Specifications (at 25°C unless noted)†

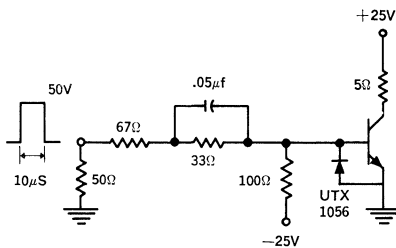
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain	h_{FE}	40	250	—	$I_C = 0.5A$, $V_{CE} = 2V$
D.C. Current Gain	h_{FE}	50	150	—	$I_C = 5A$, $V_{CE} = 5V$ (Note 1)
D.C. Current Gain	h_{FE}	30	—	—	$I_C = 10A$, $V_{CE} = 5V$ (Note 1)
Collector Saturation Voltage	$V_{CE(sat)}$.5	V	V	$I_C = 5A$, $I_B = 0.5A$ (Note 1)
Collector Saturation Voltage	$V_{CE(sat)}$	1.0	V	V	$I_C = 10A$, $I_B = 1A$ (Note 1)
Base Saturation Voltage	$V_{BE(sat)}$	1.3	V	V	$I_C = 5A$, $I_B = 0.5A$ (Note 1)
Base Saturation Voltage	$V_{BE(sat)}$	1.8	V	V	$I_C = 10A$, $I_B = 1A$ (Note 1)
Collector-Emitter Breakdown Voltage	BV_{CER}	120	V	V	$I_C = 100mA$, $R_{BE} = 10\Omega$
Collector-Emitter Breakdown Voltage	BV_{CES}	120	V	V	$I_C = 0.2\mu A$, $R_{BE} = 0$
Collector-Emitter Breakdown Voltage	BV_{CEO}	80	V	V	$I_C = 100mA$, $I_B = 0$ (Note 1)
Emitter-Base Breakdown Voltage	BV_{EBO}	7	V	V	$I_E = 10\mu A$, $I_C = 0$
Collector Cutoff Current	I_{CES}	0.2	μA	μA	$V_{CE} = 120V$, $R_{BE} = 0$
Collector Cutoff Current, 150°C	I_{CES}	0.1	mA	mA	$V_{CE} = 80V$, $R_{BE} = 0$, $T = 150^\circ C$
Collector Capacitance	C_{obo}	150	pf	pf	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$
A.C. Current Gain	h_{fe}	3	—	—	$I_C = 0.5A$, $V_{CE} = 5V$, $f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	150	ns	$I_C = 5A$
	Turn-off Time	t_{off}	800	ns	$I_{b1} = 250mA$ $I_{b2} = -250mA$ Note 2.

Notes:

1. Pulse width = 300 μ S; duty cycle \leq 2%.
2. Measured in saturated switching speed circuit.

† All values in this table are JEDEC registered.

Switching Speed Circuit



POWER TRANSISTORS

2 Amp, 300V, Planar NPN

JAN, JANTX, & JANTXV 2N5660
 JAN, JANTX, & JANTXV 2N5661
 JAN, JANTX, & JANTXV 2N5662
 JAN, JANTX, & JANTXV 2N5663

FEATURES

- Meets MIL-S-19500/454
- Collector-Base Voltage: up to 400V
- D.C. Collector Current: 5A
- Peak Collector Current: 10A
- Fast Switching

DESCRIPTION

Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

4

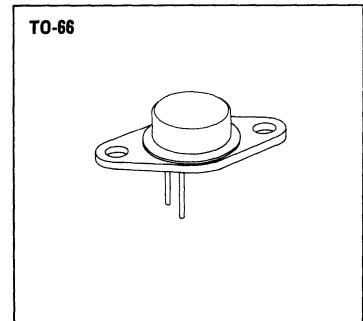
ABSOLUTE MAXIMUM RATINGS

	JAN, JANTX, & JANTXV 2N5660	JAN, JANTX, & JANTXV 2N5661	JAN, JANTX, & JANTXV 2N5662	JAN, JANTX, & JANTXV 2N5663
Collector-Base Voltage, V_{CBO}	250V	400V	250V	400V
Collector-Emitter Voltage, V_{CEO}	200V	300V	200V	300V
Emitter-Base Voltage, V_{EBO}	6V	6V	6V	6V
D.C. Collector Current, I_C	2A	2A	2A	2A
Peak Collector Current, I_C	5A	5A	5A	5A
Power Dissipation				
25°C Ambient	2.0W	2.0W	1.2W	1.2W
100°C Case	20W	20W	15W	15W
Operating and Storage Temperature Range	-65°C to 200°C			

MECHANICAL SPECIFICATIONS

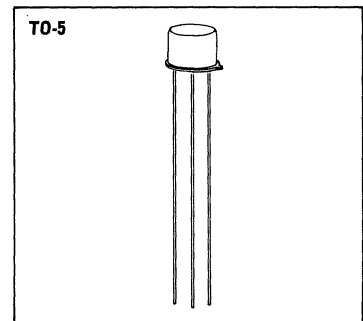
JAN, JANTX, & JANTXV 2N5660 JAN, JANTX, & JANTXV 2N5661

	INCHES	MILLIMETERS
A	620 MAX.	15.75 MAX.
B	.050 - .075	1.27 - 1.90
C	.250 - .340	6.35 - 8.63
D	.360 MIN.	9.14 MIN.
E	.028 - .034 DIA.	.711 - .863
F	.958 - .962	24.33 - 24.43
G	.570 - .590	14.47 - 14.98
H	.145 MAX. RAD.	3.68 MAX. RAD.
J	.142 - .152 DIA.	3.60 - 3.86 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190 - .210	4.82 - 5.33
M	.093 - .107	2.36 - 2.72



JAN, JANTX, & JANTXV 2N5662 JAN, JANTX, & JANTXV 2N5663

	INCHES	MILLIMETERS
A	.335 - .370	8.51 - 9.40
B	.305 - .335	7.75 - 8.51
C	.240 - .260	6.09 - 6.60
D	1.5 MIN.	38.10 MIN.
E	.010 - .030	254 - 762
F	.017 ± .002 .001	432 ± .051 .025
G	.200	5.08
H	.100	2.54
J	.031 ± .003	787 ± .076
K	.029 - .045	736 - 1.14
L	.100	2.54



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)
2N5660, 2N5662

Test	Symbol	Min.	Max.	Units	/454 Sub group	MIL-STD-750		
						Method	Test conditions	
Visual and mechanical					A-1	2071	See Mechanical Data	
25°C								
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEB}^*	250	—	Vdc	A-2	3011	$I_C = 10\text{mAdc}$; $R_{BE} = 100\Omega$; Cond. B	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}^*	200	—	Vdc	A-2	3011	$I_C = 10\text{mAdc}$; Cond. D	
Emitter-Base Breakdown Voltage	BV_{EBO}^*	6	—	Vdc	A-2	3026	$I_E = 10\mu\text{Adc}$; Cond. D	
Collector-Emitter Cutoff Current	I_{CES}^*	—	0.2	μAdc	A-2	3041	$V_{CE} = 200\text{Vdc}$; Cond. C	
Collector-Base Cutoff Current	I_{CBO}	—	0.1	μAdc	A-2	3036	$V_{CB} = 200\text{Vdc}$; Cond. D	
Collector-Base Cutoff Current	I_{CBO}	—	1.0	mAdc	A-2	3036	$V_{CB} = 250\text{Vdc}$; Cond. D	
D.C. Current Gain (Note 1)	h_{FE}^*	40	—	—	A-3	3076	$I_C = 50\text{mAdc}$, $V_{CE} = 2\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	40	120	—	A-3	3076	$I_C = 0.5\text{Adc}$, $V_{CE} = 5\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	15	—	—	A-3	3076	$I_C = 1\text{Adc}$, $V_{CE} = 5\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}	5	—	—	A-3	3076	$I_C = 2\text{Adc}$, $V_{CE} = 5\text{Vdc}$	
Collector Saturation Voltage (Note 1)	$V_{CE(\text{sat})}^*$	—	0.4	Vdc	A-3	3071	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$	
Collector Saturation Voltage (Note 1)	$V_{CE(\text{sat})}$	—	0.8	Vdc	A-3	3071	$I_C = 2\text{Adc}$, $I_B = 0.4\text{Adc}$	
Base Saturation Voltage (Note 1)	$V_{BE(\text{sat})}^*$	—	1.2	Vdc	A-3	3066	$I_C = 1\text{Adc}$, $I_B = 0.1\text{Adc}$; Cond. A	
Base Saturation Voltage (Note 1)	$V_{BE(\text{sat})}$	—	1.5	Vdc	A-3	3066	$I_C = 2\text{Adc}$, $I_B = 0.4\text{Adc}$; Cond. A	
Gain-Bandwidth Product	f_r^*	20	70	MHz	A-4	3306	$I_C = 0.1\text{Adc}$, $V_{CE} = 5\text{Vdc}$, $f = 10\text{MHz}$	
Output Capacitance	C_{ob}	—	45	pf	A-4	3236	$V_{CB} = 10\text{Vdc}$, $I_E = 0$, $f = 1\text{MHz}$	
Thermal Resistance	θ_{J-C}	—	5.0	°C/W	C-1	3151		
2N5660		—	6.7	°C/W				
2N5662		—	6.7	°C/W				
Switching Speeds	Turn-on time	t_{on}^*	—	0.25	μs	A-4	—	$I_C = 0.5\text{Adc}$
	Turn-off time	t_{off}^*	—	0.85	μs	A-4	—	
100°C								
Forward Biased Second Breakdown								
2N5660	$I_{S/B}$	2	—	Adc	B-6	3051	$V_{CE} = 10\text{Vdc}$, $t = 1\text{Sec}$	
	$I_{S/B}$	0.5	—	Adc	B-6	3051	$V_{CE} = 40\text{Vdc}$, $t = 1\text{Sec}$	
	$I_{S/B}$	36	—	mAdc	B-6	3051	$V_{CE} = 200\text{Vdc}$, $t = 1\text{Sec}$	
2N5662	$I_{S/B}$	2	—	Adc	B-7	3051	$V_{CE} = 7.5\text{Vdc}$, $t = 1\text{Sec}$	
	$I_{S/B}$	0.6	—	Adc	B-7	3051	$V_{CE} = 25\text{Vdc}$, $t = 1\text{Sec}$	
	$I_{S/B}$	27	—	mAdc	B-7	3051	$V_{CE} = 200\text{Vdc}$, $t = 1\text{Sec}$	
Unclamped Reverse Biased Second Breakdown	$E_{S/B}$	0.2	—	mJ	B-8	3053	$I_C = 2\text{Adc}$, $L = 0.1\text{mh}$	
Clamped Reverse Biased Second Breakdown	$E_{S/B}$	80	—	mJ	B-9	3053	$I_C = 2\text{Adc}$, $L = 40\text{mh}$, $V_{\text{clamp}} = 200\text{V}$	
150°C								
Collector-Emitter Cutoff Current	I_{CES}^*	—	100	μAdc	A-5	3041	$V_{CE} = 200\text{Vdc}$, Cond. C	
−65°C								
D.C. Current Gain (Note 1)	h_{FE}	15	—	—	A-6	3076	$I_C = 0.5\text{Adc}$, $V_{CE} = 5\text{Vdc}$	

Notes:1. Pulse width = $300\mu\text{s}$; duty cycle $\leq 2\%$.

* Those parameters marked with a * are JEDEC registered and devices meeting these specifications are available as commercial 2N devices.

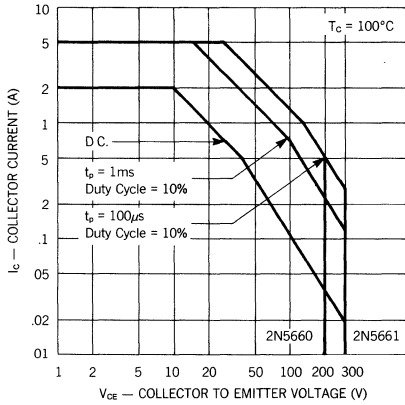
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)
2N5661, 2N5663

Test	Symbol	Min.	Max.	Units	/454 Sub group	MIL-STD-750		
						Method	Test conditions	
Visual and mechanical					A-1	2071	See Mechanical Data	
25°C								
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}^*	400	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; $R_{BE} = 100\Omega$; Cond. B	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}^*	300	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; Cond. D	
Emitter-Base Breakdown Voltage	BV_{EBO}^*	6	—	Vdc	A-2	3026	$I_E = 10\mu\text{A}$; Cond. D	
Collector-Emitter Cutoff Current	I_{CES}	—	0.2	μA	A-2	3041	$V_{CE} = 300\text{Vdc}$; Cond. C	
Collector-Base Cutoff Current	I_{CBO}	—	0.1	μA	A-2	3036	$V_{CB} = 300\text{Vdc}$; Cond. D	
Collector-Base Cutoff Current	I_{CBO}	—	1.0	mA	A-2	3036	$V_{CB} = 400\text{Vdc}$; Cond. D	
D.C. Current Gain (Note 1)	h_{FE}^*	25	—	—	A-3	3076	$I_C = 50\text{mA}$; $V_{CE} = 2\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	25	75	—	A-3	3076	$I_C = 0.5\text{A}$; $V_{CE} = 5\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	15	—	—	A-3	3076	$I_C = 1\text{A}$; $V_{CE} = 5\text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}	5	—	—	A-3	3076	$I_C = 2\text{A}$; $V_{CE} = 5\text{Vdc}$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}^*$	—	0.4	Vdc	A-3	3071	$I_C = 1\text{A}$; $I_B = 0.1\text{A}$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}^*$	—	0.8	Vdc	A-3	3071	$I_C = 2\text{A}$; $I_B = 0.4\text{A}$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}^*$	—	1.2	Vdc	A-3	3066	$I_C = 1\text{A}$; $I_B = 0.1\text{A}$; Cond. A	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}^*$	—	1.5	Vdc	A-3	3066	$I_C = 2\text{A}$; $I_B = 0.4\text{A}$; Cond. A	
Gain-Bandwidth Product	f_T^*	20	70	MHz	A-4	3306	$I_C = 0.2\text{A}$; $V_{CE} = 10\text{Vdc}$; $f = 10\text{MHz}$	
Output Capacitance	C_{ob}	—	45	pf	A-4	3236	$V_{CB} = 10\text{Vdc}$; $I_E = 0$; $f = 1\text{MHz}$	
Thermal Resistance	θ_{J-C}				C-1	3151		
			—	5.0	°C/W			
			—	6.7	°C/W			
Switching Speeds	Turn-on time	t_{on}^*	—	0.25	μs	A-4	—	$I_C = 0.5\text{A}$
	Turn-off time	t_{off}^*	—	0.85	μs	A-4	—	
100°C								
Forward Biased Second Breakdown								
2N5661	$I_{S/B}$	2	—	A	B-6	3051	$V_{CE} = 10\text{Vdc}$; $t = 1\text{Sec}$	
	$I_{S/B}$	0.5	—	A	B-6	3051	$V_{CE} = 40\text{Vdc}$; $t = 1\text{Sec}$	
	$I_{S/B}$	19	—	mA	B-6	3051	$V_{CE} = 300\text{Vdc}$; $t = 1\text{Sec}$	
2N5663	$I_{S/B}$	2	—	A	B-7	3051	$V_{CE} = 7.5\text{Vdc}$; $t = 1\text{Sec}$	
	$I_{S/B}$	0.6	—	A	B-7	3051	$V_{CE} = 25\text{Vdc}$; $t = 1\text{Sec}$	
	$I_{S/B}$	14	—	mA	B-7	3051	$V_{CE} = 300\text{Vdc}$; $t = 1\text{Sec}$	
Unclamped Reverse Biased Second Breakdown	$E_{S/B}$	0.2	—	mJ	B-8	3053	$I_C = 2\text{A}$; $L = 0.1\text{mH}$	
Clamped Reverse Biased Second Breakdown	$E_{S/B}$	80	—	mJ	B-9	3053	$I_C = 2\text{A}$; $L = 40\text{mH}$; $V_{clamp} = 300\text{V}$	
150°C								
Collector-Emitter Cutoff Current	I_{CES}	—	100	μA	A-5	3041	$V_{CE} = 300\text{Vdc}$; Cond. C	
−65°C								
D.C. Current Gain (Note 1)	h_{FE}	10	—	—	A-6	3076	$I_C = 0.5\text{A}$; $V_{CE} = 5\text{Vdc}$	

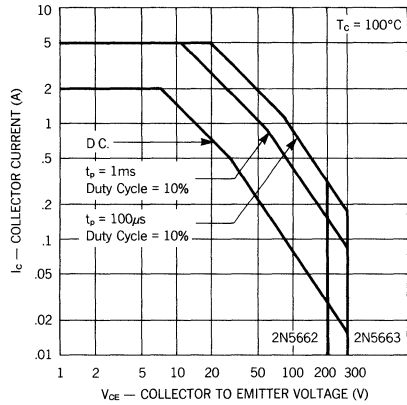
Notes:
 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.
 * Those parameters marked with a * are JEDEC registered and devices meeting these specifications are available as commercial 2N devices.



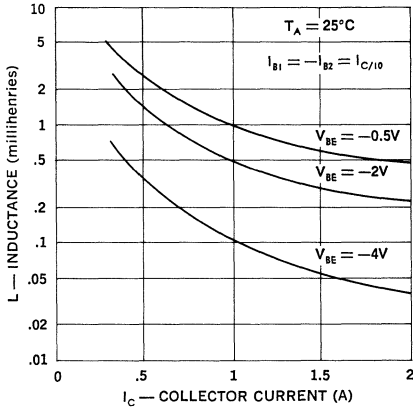
**Forward Bias
 Safe Operating Area
 2N5660, 2N5661**



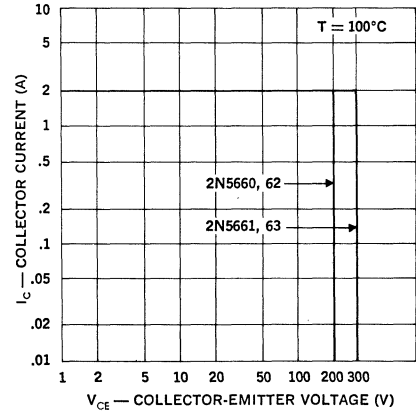
**Forward Bias
 Safe Operating Area
 2N5662, 2N5663**



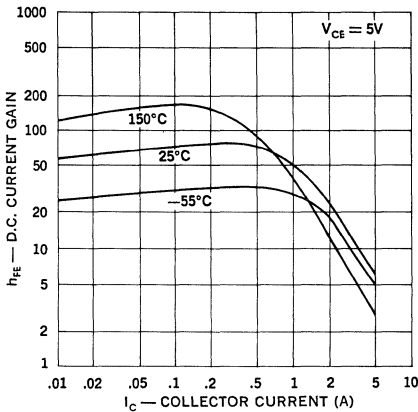
**Unclamped Reverse Bias
 Second Breakdown**



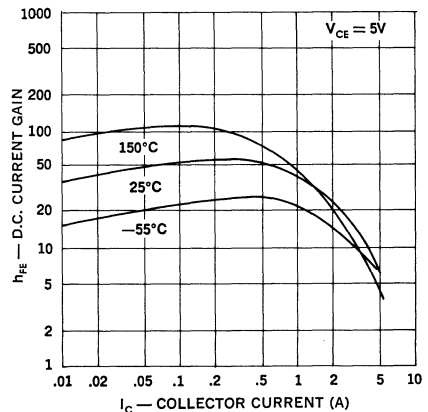
**Reverse Bias
 Safe Operating Area
 Clamped Inductive Switching**



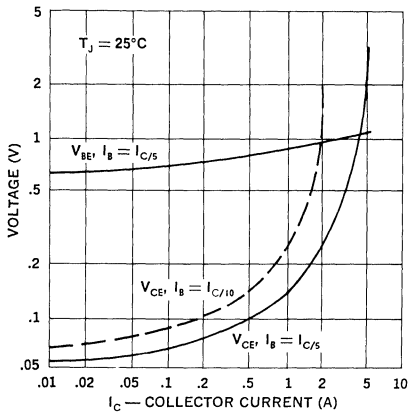
**D.C. Current Gain
 2N5660, 2N5662**



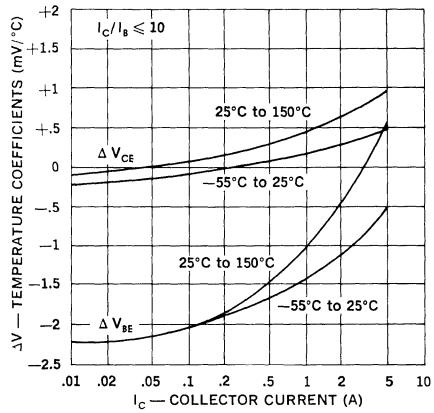
**D.C. Current Gain
 2N5661, 2N5663**



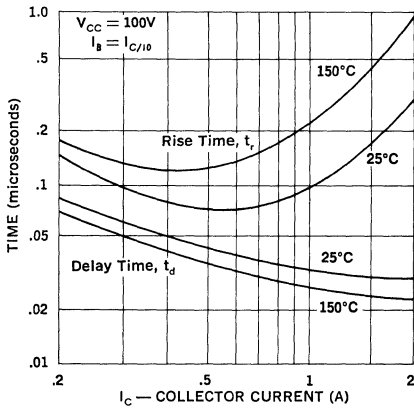
Saturation Voltages



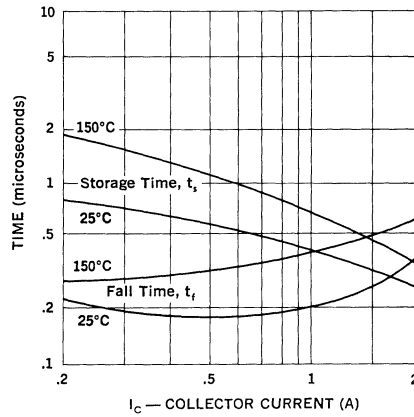
Saturation Voltage Temperature Coefficients



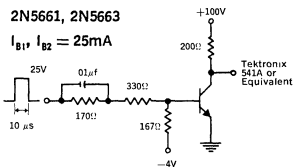
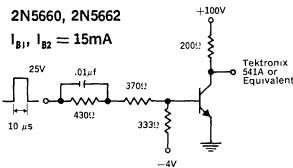
Switching Speed Characteristics



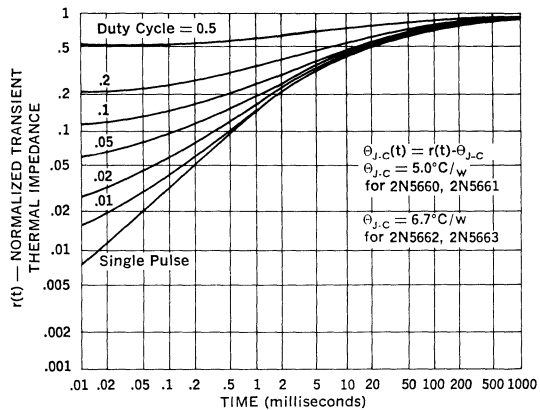
Switching Speed Characteristics



Switching Speed Circuits



Thermal Response



POWER TRANSISTORS

5 Amp, 300V, Planar NPN

JAN, JANTX, & JANTXV 2N5664
 JAN, JANTX, & JANTXV 2N5665
 JAN, JANTX, & JANTXV 2N5666
 JAN, JANTX, & JANTXV 2N5667

FEATURES

- Meets MIL-S-19500/455
- Collector-Base Voltage: up to 400V
- D.C. Collector Current: 5A
- Peak Collector Current: 10A
- Fast Switching

DESCRIPTION

Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

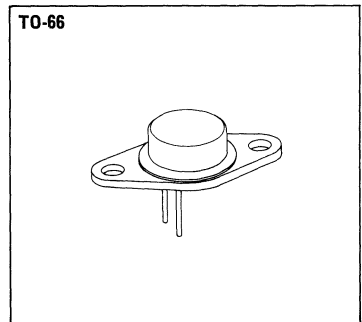
ABSOLUTE MAXIMUM RATINGS

	JAN, JANTX, & JANTXV 2N5664	JAN, JANTX, & JANTXV 2N5665	JAN, JANTX, & JANTXV 2N5666	JAN, JANTX, & JANTXV 2N5667
	Collector-Base Voltage, V_{CBO}	250V	400V	250V
Collector-Emitter Voltage, V_{CEO}	200V	300V	200V	300V
Emitter-Base Voltage, V_{EBO}	6V	6V	6V	6V
D.C. Collector Current, I_C	5A	5A	5A	5A
Peak Collector Current, I_C	10A	10A	10A	10A
Power Dissipation				
25°C Ambient	2.5W	2.5W	1.2W	1.2W
100°C Case	30W	30W	15W	15W
Operating and Storage Temperature Range	-65°C to 200°C			

MECHANICAL SPECIFICATIONS

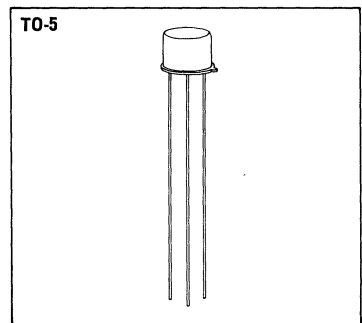
JAN, JANTX, & JANTXV 2N5664 JAN, JANTX, & JANTXV 2N5665

	INCHES	MILLIMETERS
A	.620 MAX.	15.75 MAX.
B	.050 - .075	1.27 - 1.90
C	.250 - .340	6.35 - 8.63
D	.360 MIN.	9.14 MIN.
E	.028 - .034 DIA.	.711 - .863
F	.958 - .962	24.33 - 24.43
G	.570 - .590	14.47 - 14.98
H	.145 MAX. RAD.	3.68 MAX. RAD.
J	.142 - .152 DIA.	3.60 - 3.86 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190 - .210	4.82 - 5.33
M	.093 - .107	2.36 - 2.72



JAN, JANTX, & JANTXV 2N5666 JAN, JANTX, & JANTXV 2N5667

	INCHES	MILLIMETERS
A	.335 - .370	8.51 - 9.40
B	.305 - .335	7.75 - 8.51
C	.240 - .260	6.09 - 6.60
D	1.5 MIN.	38.10 MIN.
E	.010 - .030	.254 - .762
F	.017 ± .002 .001	.432 ± .051 .025
G	.200	5.08
H	.100	2.54
J	.031 ± .003	.787 ± .076
K	.029 - .045	.736 - 1.14
L	.100	2.54



ELECTRICAL SPECIFICATIONS (at 25 °C unless noted)
2N5664, 2N5666

Test	Symbol	Min.	Max.	Units	/455 Sub group	MIL-STD-750		
						Method	Test conditions	
Visual and mechanical					A-1	2071	See Mechanical Data	
25°C								
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}^*	250	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; $R_{BE} = 100\ \Omega$, Cond. B	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}^*	200	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; Cond. D	
Emitter-Base Breakdown Voltage	BV_{EBO}^*	6.0	—	Vdc	A-2	3026	$I_E = 10\ \mu\text{A}$; Cond. D	
Collector-Emitter Cutoff Current	I_{CES}	—	0.2	μA	A-2	3041	$V_{CE} = 200\ \text{Vdc}$; Cond. C	
Collector-Base Cutoff Current	I_{CBO}	—	0.1	μA	A-2	3036	$V_{CB} = 200\ \text{Vdc}$; Cond. D	
Collector-Base Cutoff Current	I_{CBO}	—	1.0	mA	A-2	3036	$V_{CB} = 250\ \text{Vdc}$; Cond. D	
D.C. Current Gain (Note 1)	h_{FE}^*	40	—	—	A-3	3076	$I_C = 0.5\ \text{A}$; $V_{CE} = 2\ \text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	40	120	—	A-3	3076	$I_C = 1\ \text{A}$; $V_{CE} = 5\ \text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}^*	15	—	—	A-3	3076	$I_C = 3\ \text{A}$; $V_{CE} = 5\ \text{Vdc}$	
D.C. Current Gain (Note 1)	h_{FE}	5	—	—	A-3	3076	$I_C = 5\ \text{A}$; $V_{CE} = 5\ \text{Vdc}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})^*$	—	0.4	Vdc	A-3	3071	$I_C = 3\ \text{A}$; $I_B = 0.3\ \text{A}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})$	—	1.0	Vdc	A-3	3071	$I_C = 5\ \text{A}$; $I_B = 1\ \text{A}$	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})^*$	—	1.2	Vdc	A-3	3066	$I_C = 3\ \text{A}$; $I_B = 0.3\ \text{A}$; Cond. A	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})$	—	1.5	Vdc	A-3	3066	$I_C = 5\ \text{A}$; $I_B = 1\ \text{A}$; Cond. A	
Gain-Bandwidth Product	f_T^*	20	70	MHz	A-4	3306	$I_C = 0.5\ \text{A}$; $V_{CE} = 5\ \text{Vdc}$; $f = 10\ \text{MHz}$	
Output Capacitance	C_{oh}	—	120	pf	A-4	3236	$V_{CB} = 10\ \text{Vdc}$; $I_E = 0$; $f = 1\ \text{MHz}$	
Thermal Resistance	θ_{J-C}				C-1	3151		
2N5664		—	3.3	°C/W				
2N5666		—	6.7	°C/W				
Switching Speeds	Turn-on Time	t_{on}^*	—	0.25	μs	A-4	—	$I_C = 1\ \text{A}$
	Turn-off Time	t_{off}^*	—	1.5	μs	A-4	—	
100°C								
Forward Biased Second Breakdown 2N5664	$I_{S/B}$	5	—	A	B-6	3051	$V_{CE} = 6\ \text{Vdc}$; $t = 1\ \text{sec}$	
	$I_{S/B}$	0.75	—	A	B-6	3051	$V_{CE} = 40\ \text{Vdc}$; $t = 1\ \text{sec}$	
	$I_{S/B}$	43	—	mA	B-6	3051	$V_{CE} = 200\ \text{Vdc}$; $t = 1\ \text{sec}$	
2N5666	$I_{S/B}$	5	—	A	B-7	3051	$V_{CE} = 3\ \text{Vdc}$; $t = 1\ \text{sec}$	
	$I_{S/B}$	0.4	—	A	B-7	3051	$V_{CE} = 37.5\ \text{Vdc}$; $t = 1\ \text{sec}$	
	$I_{S/B}$	27	—	mA	B-7	3051	$V_{CE} = 200\ \text{Vdc}$; $t = 1\ \text{sec}$	
Unclamped Reverse Biased Second Breakdown	$E_{S/B}^*$	0.81	—	mJ	B-8	3053	$I_C = 5\ \text{A}$; $L = .065\ \text{mH}$	
Clamped Reverse Biased Second Breakdown	$E_{S/B}$	500	—	mJ	B-9	3053	$I_C = 5\ \text{A}$; $L = 40\ \text{mH}$; $V_{clamp} = 200\ \text{V}$	
150°C								
Collector-Emitter Cutoff Current	I_{CES}	—	100	μA	A-5	3041	$V_{CE} = 200\ \text{Vdc}$; Cond. C	
−65°C								
D.C. Current Gain (Note 1)	h_{FE}	15	—	—	A-6	3076	$I_C = 1\ \text{A}$; $V_{CE} = 5\ \text{Vdc}$	

Notes:

1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

* Those parameters marked with a * are JEDEC registered and devices meeting these specifications are available as commercial 2N devices.



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)
2N5665, 2N5667

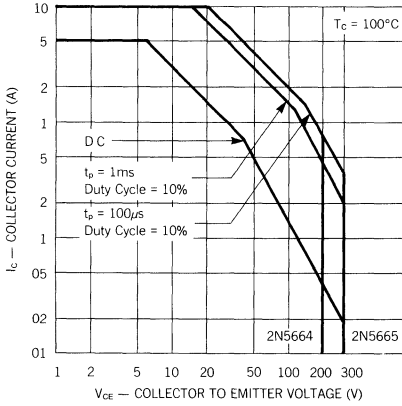
Test	Symbol	Min.	Max.	Units	/455 Sub group	MIL-STD-750		
						Method	Test conditions	
Visual and mechanical					A-1	2071	See Mechanical Data	
25°C								
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}^*	400	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; $R_{BE} = 100\ \Omega$, Cond. B	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}^*	300	—	Vdc	A-2	3011	$I_C = 10\text{mA}$; Cond. D	
Emitter-Base Breakdown Voltage	BV_{EBO}^*	6	—	Vdc	A-2	3026	$I_E = 10\ \mu\text{A}$; Cond. D	
Collector-Emitter Cutoff Current	I_{CES}	—	0.2	μA	A-2	3041	$V_{CE} = 300\text{V}$; Cond. C	
Collector-Base Cutoff Current	I_{CBO}	—	0.1	μA	A-2	3036	$V_{CB} = 300\text{V}$; Cond. D	
Collector-Base Cutoff Current	I_{CBO}	—	1.0	mA	A-2	3036	$V_{CB} = 400\text{V}$; Cond. D	
D.C. Current Gain (Note 1)	h_{FE}^*	25	—	—	A-3	3076	$I_C = 0.5\text{A}$, $V_{CE} = 2\text{V}$	
D.C. Current Gain (Note 1)	h_{FE}^*	25	75	—	A-3	3076	$I_C = 1\text{A}$, $V_{CE} = 5\text{V}$	
D.C. Current Gain (Note 1)	h_{FE}^*	15	—	—	A-3	3076	$I_C = 3\text{A}$, $V_{CE} = 10\text{V}$	
D.C. Current Gain (Note 1)	h_{FE}	5	—	—	A-3	3076	$I_C = 5\text{A}$, $V_{CE} = 5\text{V}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})^*$	—	0.4	Vdc	A-3	3071	$I_C = 3\text{A}$, $I_B = 0.6\text{A}$	
Collector Saturation Voltage (Note 1)	$V_{CE}(\text{sat})$	—	1.0	Vdc	A-3	3071	$I_C = 5\text{A}$, $I_B = 1\text{A}$	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})^*$	—	1.2	Vdc	A-3	3066	$I_C = 3\text{A}$, $I_B = 0.6\text{A}$; Cond. A	
Base Saturation Voltage (Note 1)	$V_{BE}(\text{sat})$	—	1.5	Vdc	A-3	3066	$I_C = 5\text{A}$, $I_B = 1\text{A}$; Cond. A	
Gain-Bandwidth Product	f_T^*	20	70	MHz	A-4	3306	$I_C = 0.5\text{A}$, $V_{CE} = 5\text{V}$, $f = 10\text{MHz}$	
Output Capacitance	C_{ob}	—	90	pf	A-4	3236	$V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$	
Thermal Resistance	θ_{J-C}				C-1	3151		
2N5665		—	3.3	°C/W				
2N5667		—	6.7	°C/W				
Switching Speeds	Turn-on time	t_{on}^*	—	0.25	μs	A-4	—	$I_C = 1\text{A}$
	Turn-off time	t_{off}^*	—	2.0	μs	A-4	—	
100°C								
Forward Biased Second Breakdown 2N5665	$I_{S/B}$	5	—	A	B-6	3051	$V_{CE} = 6\text{V}$, $t = 1\text{sec}$	
	$I_{S/B}$	0.75	—	A	B-6	3051	$V_{CE} = 40\text{V}$, $t = 1\text{sec}$	
	$I_{S/B}$	21	—	mA	B-6	3051	$V_{CE} = 300\text{V}$, $t = 1\text{sec}$	
	2N5667	$I_{S/B}$	5	—	A	B-7	3051	$V_{CE} = 3\text{V}$, $t = 1\text{sec}$
		$I_{S/B}$	0.4	—	A	B-7	3051	$V_{CE} = 37.5\text{V}$, $t = 1\text{sec}$
		$I_{S/B}$	14	—	mA	B-7	3051	$V_{CE} = 300\text{V}$, $t = 1\text{sec}$
Unclamped Reverse Biased Second Breakdown	$E_{S/B}$	0.81	—	mJ	B-8	3053	$I_C = 5\text{A}$, $L = .065\text{mH}$	
Clamped Reverse Biased Second Breakdown	$E_{S/B}$	500	—	mJ	B-9	3053	$I_C = 5\text{A}$, $L = 40\text{mH}$, $V_{clamp} = 300\text{V}$	
150°C								
Collector-Emitter Cutoff Current	I_{CES}	—	100	μA	A-5	3041	$V_{CE} = 300\text{V}$, Cond. C	
-65°C								
D.C. Current Gain (Note 1)	h_{FE}	10	—	—	A-6	3076	$I_C = 1\text{A}$, $V_{CE} = 5\text{V}$	

Notes:

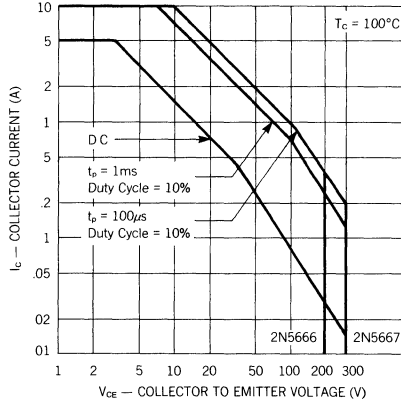
1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

* Those parameters marked with a * are JEDEC registered and devices meeting these specifications are available as commercial 2N devices.

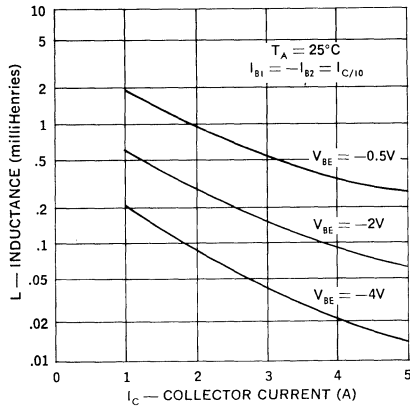
**Forward Bias
 Safe Operating Area
 2N5664, 2N5665**



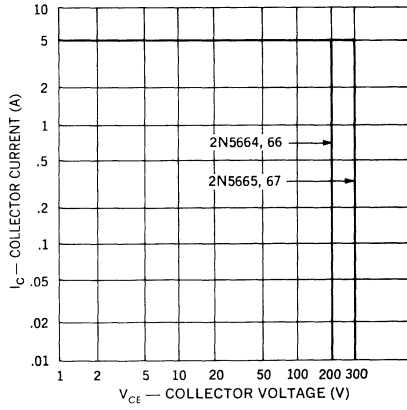
**Forward Bias
 Safe Operating Area
 2N5666, 2N5667**



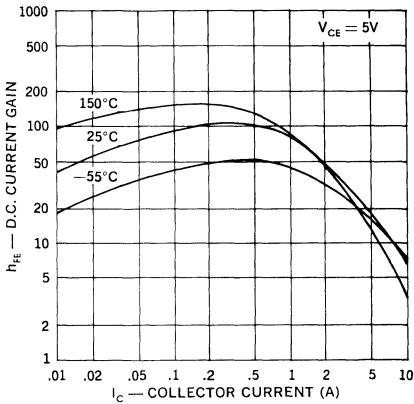
**Unclamped Reverse Bias
 Second Breakdown**



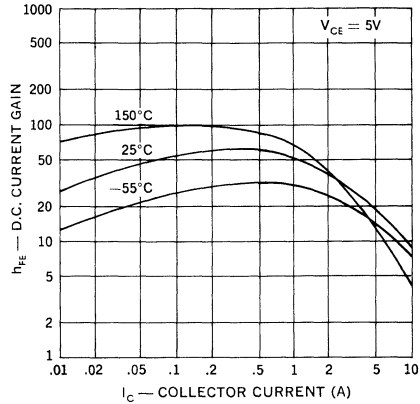
**Reverse Bias
 Safe Operating Area
 Clamped Inductive Switching**



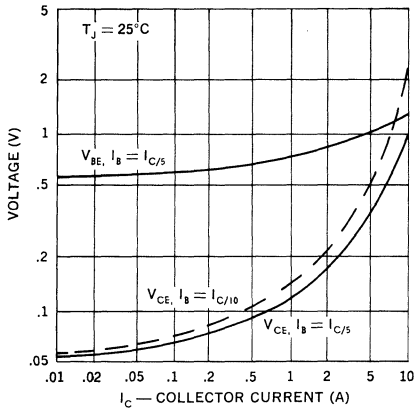
**D.C. Current Gain
 2N5664, 2N5666**



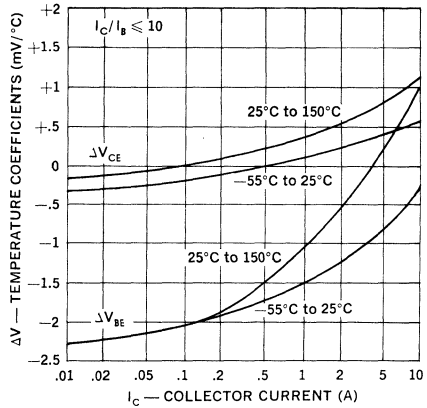
**D.C. Current Gain
 2N5665, 2N5667**



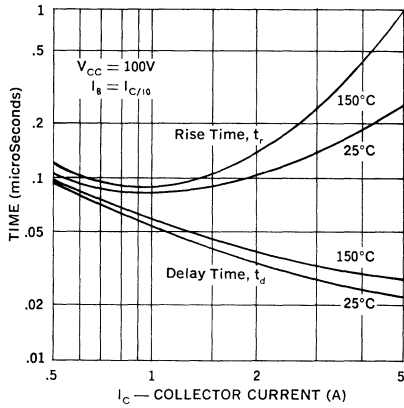
Saturation Voltages



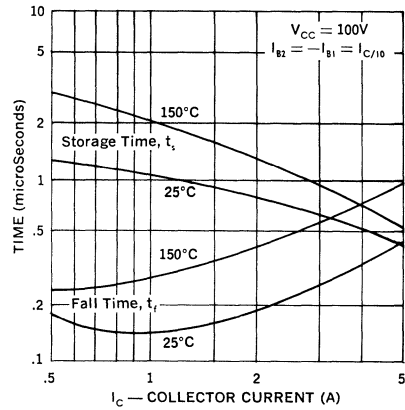
Saturation Voltage Temperature Coefficients



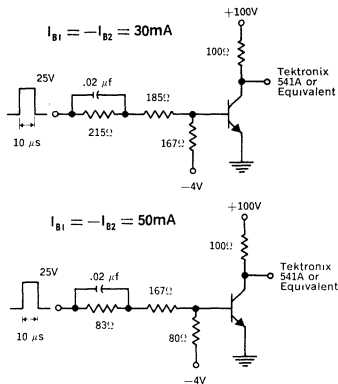
Switching Speed Characteristics



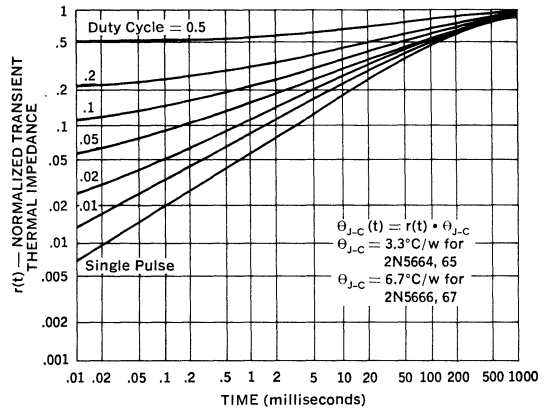
Switching Speed Characteristics



Switching Speed Circuits



Thermal Response



POWER TRANSISTORS

30A, 150V, Fast Switching,
Silicon NPN Mesa

2N5671
2N5672

4

FEATURES

- Collector-Base Voltage: up to 150V
 - DC Collector Current = 30A
 - Low $V_{CE(SAT)} = 0.75V$ Max.
 - $t_{on} = 0.5\mu S$
 - $t_{fall} = 0.5\mu S$
- } @ $I_C = 15A$

DESCRIPTION

These glass passivated power transistors combine fast-switching, low saturation voltage and rugged E_{slb} capability. They are designed for use in switching regulators, converters, inverters and switching-control amplifiers.

ABSOLUTE MAXIMUM RATINGS *

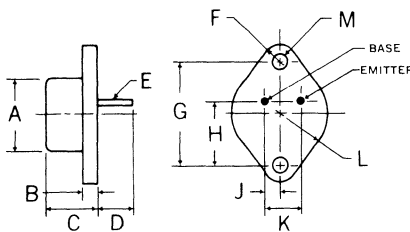
	2N5671	2N5672
* Collector-to-Base Voltage, V_{CBO}	120V	150V
Collector-Emitter Sustaining Voltage, $V_{CEX(SUS)}$	120V	150V
$V_{CER(SUS)}$	110V	140V
$V_{CEO(SUS)}$	90V	120V
* Emitter-Base Voltage, V_{EBO}	.7V	.7V
* Collector Current, I_C continuous	30A	30A
* Base Current, I_B continuous	10A	10A
* Power Dissipation, 25°C Case	140W	140W
* Operating and Storage Temperature Range	-65 to 200°C	

* JEDEC registered values.

MECHANICAL SPECIFICATIONS

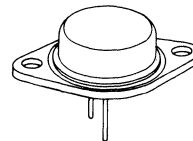
NOTE:
Leads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.

2N5671-2N5672



	ins.	mm.
A	875 MAX	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-450	6.35-11.43
D	312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	151-161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

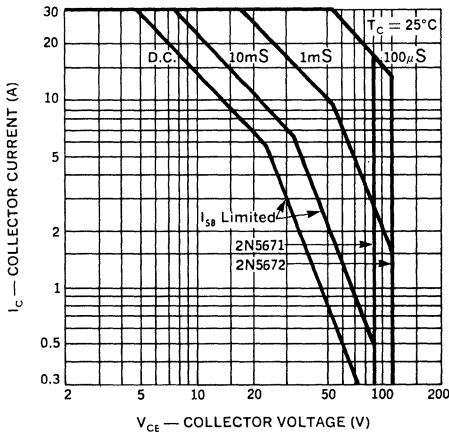
Test	Symbol	2N5671		2N5672		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
* D.C. Current Gain (Note 1)	h_{FE}	20	100	20	100		$I_C = 15A, V_{CE} = 2V$
D.C. Current Gain (Note 1)	h_{FE}	20	—	20	—		$I_C = 20A, V_{CE} = 5V$
* Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	0.75	—	0.75	V	$I_C = 15A, I_B = 1.2A$
* Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	—	1.5	V	$I_C = 15A, I_B = 1.2A$
Base to Emitter Voltage (Note 1)	V_{BE}	—	1.6	—	1.6	$\frac{V}{V}$	$I_C = 15A, V_{CE} = 5V$
* Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	90	—	120	—	V	$I_C = 0.2A, I_B = 0$
* Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEX(sus)}$	120	—	150	—	V	$I_C = 0.2A$ $V_{BE} = -1.5V$ $I_B = 0$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CER(sus)}$	110	—	140	—	V	$R_{BE} = 50\Omega, I_C = 0.2A$
* Emitter-Cutoff Current	I_{EBO}	10	—	10	—	mA	$V_{EB} = 7.0V$
Collector Cutoff Current	I_{CEO}	—	10	—	10	mA	$V_{CE} = 80V$
* Collector Cutoff Current	I_{CEV}	—	12	—	—	mA	$V_{CE} = 110V, V_{BE} = -1.5V$
		—	—	—	10		$V_{CE} = 135V, V_{BE} = -1.5V$
		—	15	—	10		$V_{CE} = 100V, V_{BE} = -1.5V,$ $T_C = 150^\circ C$
Magnitude of Small Signal Forward — Current Transfer Ratio	h_{fo}	10	—	10	—		$V_{CE} = 10V, I_C = 2A, f = 5MHz$
Collector Capacitance	C_{ob}	—	900	—	900	pF	$V_{CB} = 10V, f = 1 MHz$
* Second Breakdown Energy	$E_{S/b}$	20	—	20	—	mJ	$V_{BE} = 4V, I_C = 15A$ $R_{BE} = 20\Omega, L = 180\mu H$
Forward Bias Second Breakdown Collector Current	$I_{S/b}$	5.8	—	5.8	—	A	$V_{CE} = 24V, t = 1s, non-rep.$
		0.9	—	0.9	—		$V_{CE} = 45V, t = 1s, non-rep.$
* Switching Speeds: Turn-on Time (Delay + Rise)	t_{on}	—	0.5	—	0.5	μS	$I_C = 15A$ $I_{B1} = I_{B2} = 1.2A$ $V_{CC} = 30V$
Storage Time	t_s	—	1.5	—	1.5	μS	
Fall Time	t_f	—	0.5	—	0.5	μS	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$	—	1.25	—	1.25	$^\circ C/W$	$V_{CE} = 40V, I_C = 0.5A$

Notes:

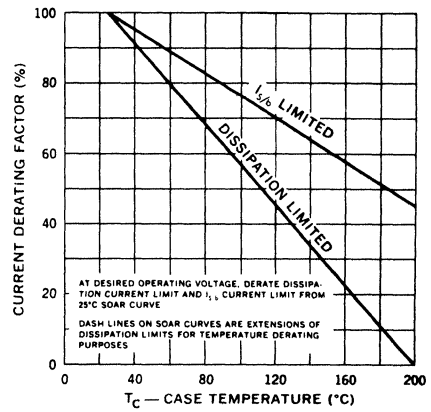
- Pulse width = 250 μ S; duty cycle $\leq 1\%$.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu$ S; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

* JEDEC registered values.

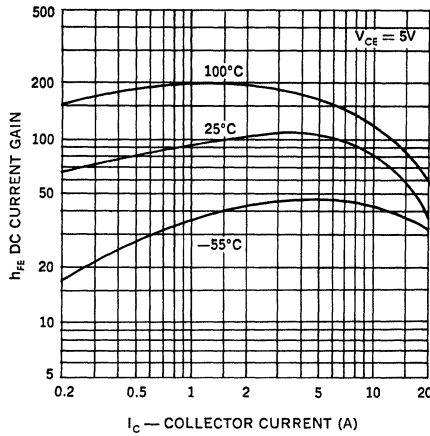
Forward Bias Safe Operating Area



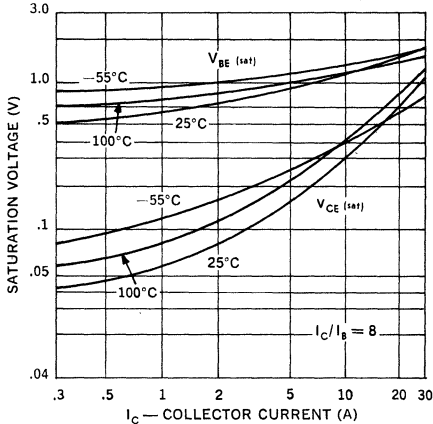
Power Derating



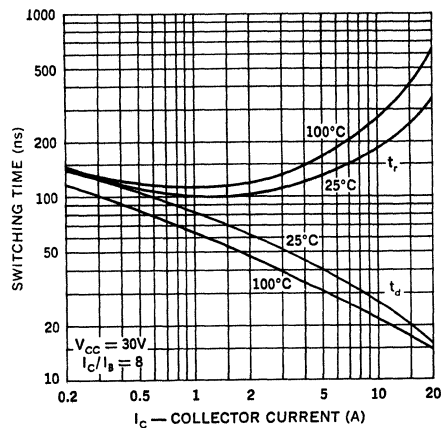
DC Current Gain



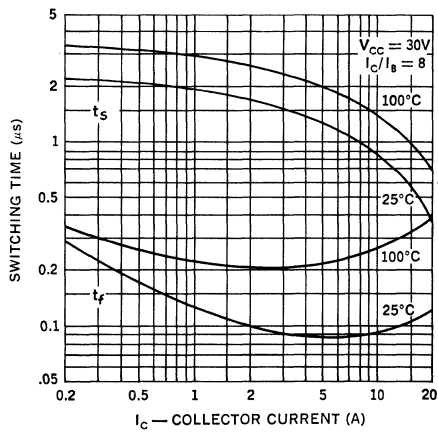
Transistor — Saturation Voltages



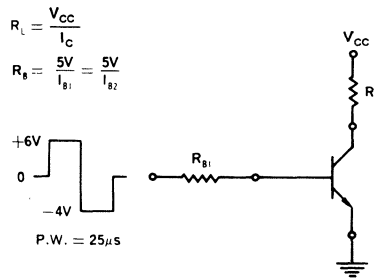
Resistive — Turn-On Time



Resistive Turn-Off Time



Switching Time Test Circuit



POWER TRANSISTORS

3A, 375V
Silicon NPN Mesa

2N5838
2N5839
2N5840

4

FEATURES

- Collector-Base Voltage: up to 375V
- Peak Collector Current: 5A
- Low Saturation Voltage
- High Second Breakdown Energy

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

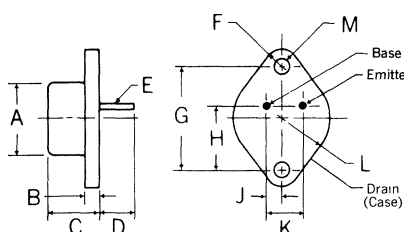
ABSOLUTE MAXIMUM RATINGS *

	2N5838	2N5839	2N5840
Collector-Base Voltage, V_{CBO}	275V	300V	375V
Collector-Emitter Voltage, V_{CEO}	250V	275V	350V
Emitter-Base Voltage, V_{EBO}	6V	6V	6V
Collector Current, I_C continuous	3A	3A	3A
Collector Current, I_{CM} peak	5A	5A	5A
Base Current, I_B continuous	1.5A	1.5A	1.5A
Power Dissipation, P_T 25°C Case	100W	100W	100W
Operating and Storage Temperature Range	-65 to +200°C		

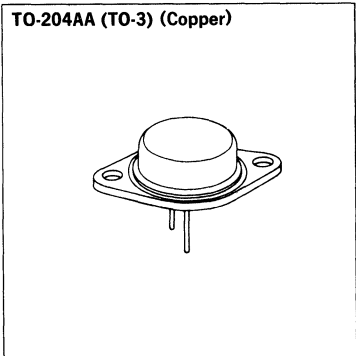
* JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



	ins.	mm.
A	875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	312 MIN.	7.92 MIN.
E	0.057-0.063 DIA.	1.45-1.60 DIA.
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1177-1197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	.151- .161 DIA.	3.84-4.09 DIA.



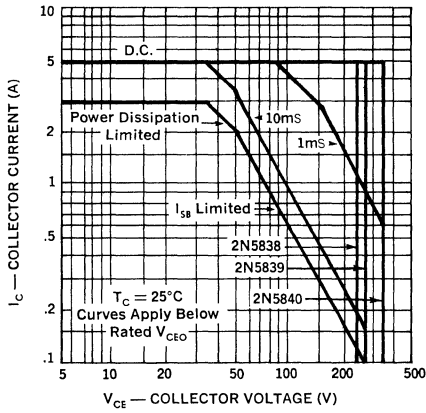
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	2N5838		2N5839		2N5840		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	20	—	20	—	20	—		$I_C = 0.5A, V_{CE} = 5V$
* D.C. Current Gain (Note 1)	h_{FE}	—	—	10	50	10	50		$I_C = 2A, V_{CE} = 3V$
* D.C. Current Gain (Note 1)	h_{FE}	8	40	—	—	—	—	V	$I_C = 3A, V_{CE} = 2V$
* Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	—	—	1.5	—	1.5	V	$I_C = 2A, I_B = 0.2A$
* Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	—	—	—	V	$I_C = 3A, I_B = 0.375A$
* Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	—	—	2.0	—	2.0	V	$I_C = 2A, I_B = 0.2A$
* Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	2.0	—	—	—	—	V	$I_C = 3A, I_B = 0.375A$
* Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	250	—	275	—	350	—	V	$I_C = 200mA, I_B = 0$
* Collector-Emitter Sustaining Voltage	V_{CEX}	275	—	300	—	375	—	V	$I_C = 0.1A, V_{BE} = -1.5V, L = 10mH$
* Emitter-Base Cutoff Current	I_{EBO}	—	1.0	—	1.0	—	1.0	mA	$V_{EB} = 6V$
Collector Cutoff Current	I_{CEO}	—	2.0	—	—	—	—	—	$V_{CE} = 200V$
		—	—	—	2.0	—	2.0	mA	$V_{CE} = 250V$
* Collector Cutoff Current	I_{CEV}	—	5.0	—	—	—	—	mA	$V_{CE} = 265V$
		—	—	—	2.0	—	—		$V_{CE} = 290V$
		—	—	—	—	—	2.0		$V_{CE} = 360V$
* Collector Cutoff Current, 150°C	I_{CEV}	—	8.0	—	—	—	—	mA	$V_{CE} = 265V$
		—	—	—	5.0	—	—		$V_{CE} = 290V$
		—	—	—	—	—	5.0		$V_{CE} = 360V$
Forward Bias Second Breakdown	$I_{S/B}$	—	2.5A	—	2.5A	—	2.5A		$V_{CE} = 40V, t_p = 1 \text{ Sec.}$
* Second Breakdown Energy	$E_{S/B}$	0.45	—	0.45	—	0.45	—	mJ	$R_{BE} = 50\Omega, L = 100\mu H$
Collector Capacitance	C_{ob}	—	150	—	150	—	150	pF	$V_{CB} = 10V, I_E = 0, f = 1 \text{ MHz}$
* Small Signal High Frequency Gain	h_{fe}	5	—	5	—	5	—	MHz	$I_C = .2A, V_{CE} = 10V, f = 1 \text{ MHz}$
* Switching Speeds:									
Delay Time	t_d	—	—	—	0.7	—	0.7	μS	$I_C = 2A, V_{CE} = 200V, I_{B1} = I_{B2} = (0.2A)$
	t_d	—	0.6	—	—	—	—		$I_C = 3A, V_{CE} = 200V, I_{B1} = I_{B2} = (.375A)$
Rise Time	t_r	—	—	—	1.5	—	1.75	μS	$I_C = 2A, V_{CE} = 200V, I_{B1} = I_{B2} = (0.2A)$
	t_r	—	1.5	—	—	—	—		$I_C = 3A, V_{CE} = 200V, I_{B1} = I_{B2} = (.375A)$
Storage Time	t_s	—	—	—	3.75	—	3.0	μS	$I_C = 2A, V_{CE} = 200V, I_{B1} = I_{B2} = (0.2A)$
	t_s	—	3.0	—	—	—	—		$I_C = 3A, V_{CE} = 200V, I_{B1} = I_{B2} = (.375A)$
Fall Time	t_f	—	—	—	1.5	—	1.5	μS	$I_C = 2A, V_{CE} = 200V, I_{B1} = I_{B2} = (0.2A)$
	t_f	—	1.5	—	—	—	—		$I_C = 3A, V_{CE} = 200V, I_{B1} = I_{B2} = (.375A)$
Thermal Resistance	$R_{\theta JC}$	—	1.75	—	1.75	—	1.75	°C/W	

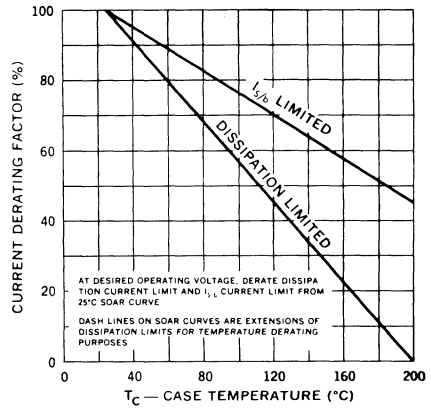
Notes:

- Pulse width = 250 μS ; duty cycle $\leq 1\%$.
 - Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.
- * JEDEC registered values.

Forward Bias Safe Operating Area

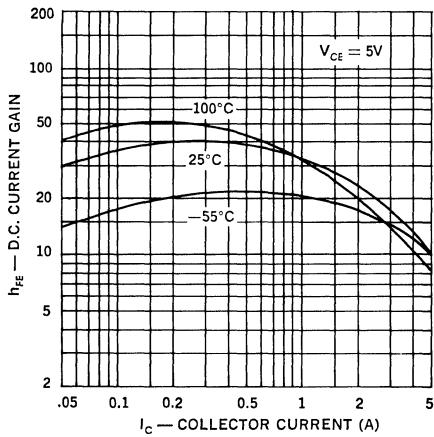


Power Derating

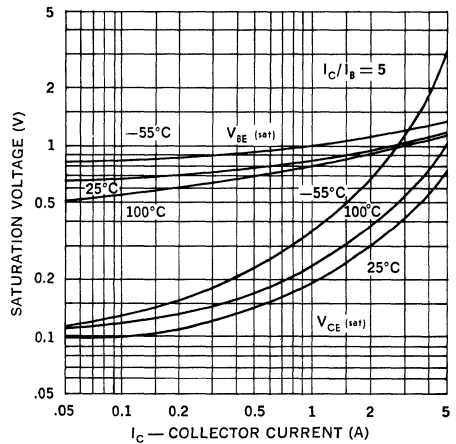


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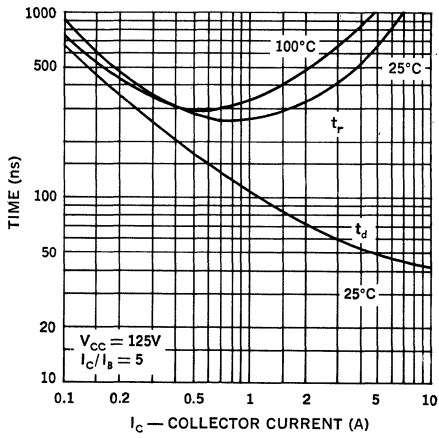
D.C. Current Gain



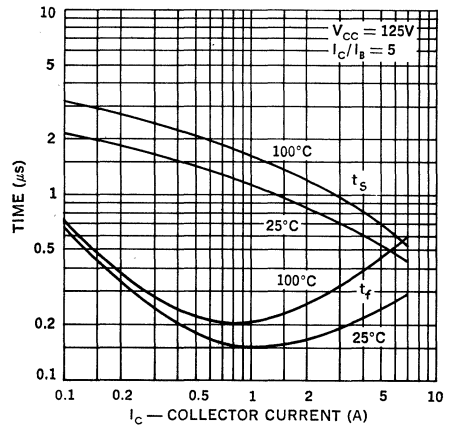
Saturation Voltages



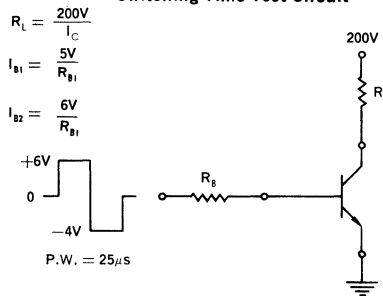
Resistive — Turn-On Time



Resistive — Turn-Off Time



Switching Time Test Circuit



POWER TRANSISTORS

10A, 450V, Fast Switching,
Silicon NPN Mesa

2N6249
2N6250
2N6251

4

FEATURES

- Collector-Base Voltage: up to 450V
- Peak Collector Current: 30A
- Low Saturation Voltage
- Maximum Safe Area of Operation

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

ABSOLUTE MAXIMUM RATINGS

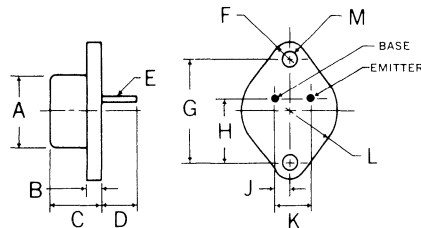
	2N6249	2N6250	2N6251
* Collector-Base Voltage, V_{CBO}	300V	375V	450V
* Collector-Emitter Voltage, V_{CEO}	200V	275V	350V
Emitter-Base Voltage, V_{EBO}	6V	6V	6V
* Collector Current, I_C continuous	10A	10A	10A
Collector Current, I_{CM} peak	30A	30A	20A
* Base Current, I_B continuous	10A	10A	10A
* Power Dissipation, P_T 25°C Case	175W	175W	175W
* Operating and Storage Temperature Range	-65 to +200°C		

* JEDEC registered values.

MECHANICAL SPECIFICATIONS

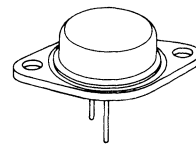
NOTE:
Leads may be soldered to within $1/16$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.

2N6249-2N6251



	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	312 MIN	7.92 MIN
E	0.38-0.43 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

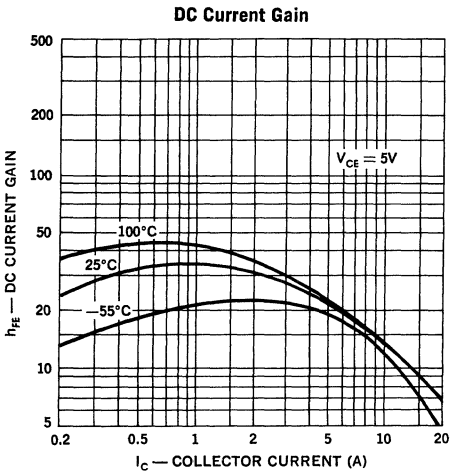
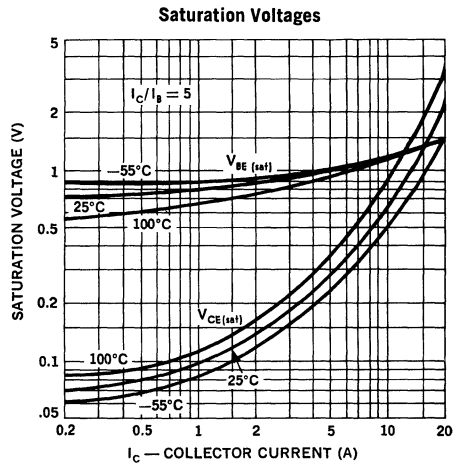
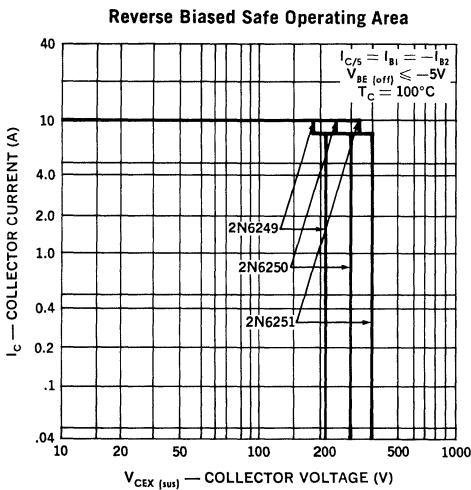
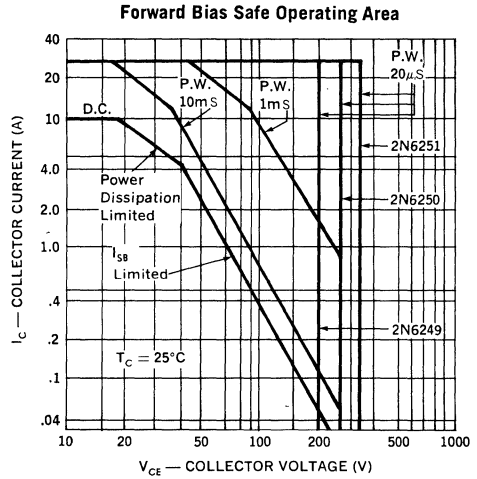
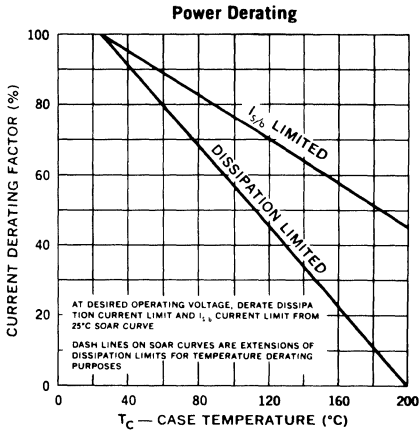
Test	Symbol	2N6249		2N6250		2N6251		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
* D.C. Current Gain (Note 1)	h_{FE}	10	50	8	50	6	50		$I_C = 10A, V_{CE} = 3.0V$
* Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	—	1.5	V	$I_C = 10A$ $I_B = 1.0A$ (2N6249) $I_B = 1.25A$ (2N6250) $I_B = 1.67A$ (2N6251)
* Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	2.25	—	2.25	—	2.25	V	
* Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	200	—	275	—	350	—	V	$I_C = 200mA$
* Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEX(sus)}$	225	—	300	—	375	—	V	$I_C = 200mA, R_{BE} = 50\Omega$ $L = 14mH$
* Emitter Base Cutoff Current	I_{EBO}	—	1.0	—	1.0	—	1.0	mA	$V_{EB} = 6V$
Collector Cutoff Current	I_{CEO}	—	5.0	—	5.0	—	5.0	mA	$V_{CE} = 50V$ less than rated $V_{CEO(sus)}$
* Collector Cutoff Current	I_{CEV}	—	5.0	—	5.0	—	5.0	mA	$V_{BE} = -1.5V$
* Collector Cutoff Current, 125°	I_{CEV}	—	10	—	10	—	10	mA	$V_{CE} = \text{rated } V_{CER(sus)}$
* Second Breakdown Energy	$E_{S/b}$	—	2.5	—	2.5	—	2.5	mJ	$I_C = 10A, L = 50\mu H$ $R_{BE} = 50\Omega, V_{BE(off)} = -4V$
* Forward Bias Second Breakdown	$I_{S/b}$	5.8 0.3	— —	5.8 0.3	— —	5.8 0.3	— —	A	$V_{CE} = 30V$ $V_{CE} = 100V$
* Thermal Resistance	$R\theta_{JC}$	—	1.0	—	1.0	—	1.0	°C/W	$V_{CE} = 10V, I_C = 5A$
* High Frequency Gain	$ h_{FE} $	2.5	—	2.5	—	2.5	—		$I_C = 1A, V_{CE} = 10V, f = 1\text{ MHz}$
* Switching Speeds:									
Rise Time	t_r	0.8	2.0	0.8	2.0	0.8	2.0	μS	$I_C = 10A$ $I_{B1} = I_{B2} = 1.0A$ (2N6249)
Storage Time	t_s	1.8	3.5	1.8	3.5	1.8	3.5		$I_{B1} = I_{B2} = 1.25A$ (2N6250)
Fall Time	t_f	0.5	1.0	0.5	1.0	0.5	1.0		$I_{B1} = I_{B2} = 1.67A$ (2N6251)

Notes:

1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$.

Voltage clamped at maximum collector-emitter voltage.

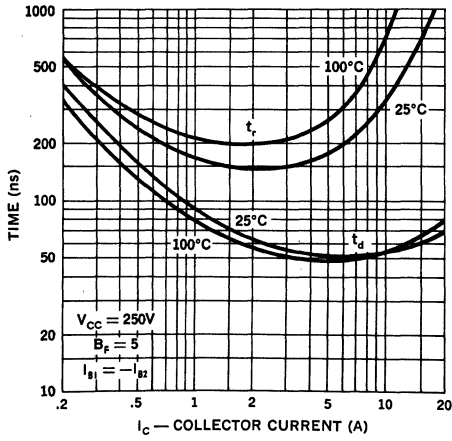
* JEDEC registered values.



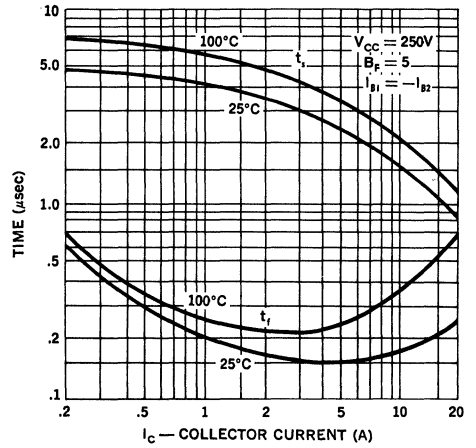
Typical Inductive Load Switching Performance

I_c Amps	T_J °C	t_t μS	t_{fv} nS	t_{fi} nS
3	25	.8	.14	.025
	100	1.10	.18	.035
5	25	.9	.14	.025
	100	1.2	.16	.030
10	25	1.2	.05	.050
	100	1.5	.12	.100

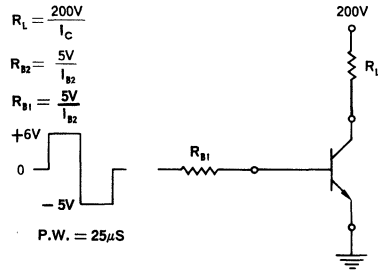
Resistive Turn-On Time



Resistive Turn-Off Time



Switching Time Test Circuit



POWER TRANSISTORS

8 Amp, 700V,

Triple Diffused NPN Mesa

JAN, JANTX, & JANTXV 2N6306

2N6307

JAN, JANTX, & JANTXV 2N6308

FEATURES

- Collector-Base Voltage: up to 700V
- Peak Collector Current: 16A
- Rise Time: $\leq 600\text{ns}$
- Fall Time: $\leq 400\text{ns}$
- JAN, JANTX, & JANTXV available in
- 2N6306 and 2N6308

DESCRIPTION

These high voltage triple diffused glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

4

ABSOLUTE MAXIMUM RATINGS *

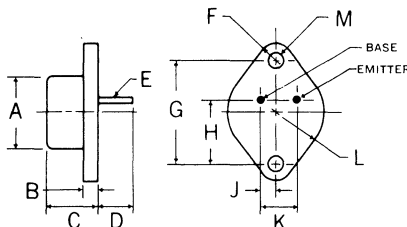
	JAN, JANTX, & JANTXV 2N6306	2N6307	JAN, JANTX, & JANTXV 2N6308
Collector-Base Voltage, V_{CBO}	500V	600V	700V
Collector-Emitter Voltage, V_{CEO}	250V	300V	350V
Emitter-Base Voltage, V_{EB0}	8V	8V	8V
Collector Current, I_C continuous	8A	8A	8A
Collector Current, I_{CM} peak	16A	16A	16A
Base Current, I_B continuous	4A	4A	4A
Power Dissipation, P_T 25°C Case	125W	125W	125W
Operating and Storage Temperature Range	-65 to +200°C		

* JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

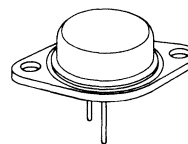
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



JAN, JANTX, & JANTXV 2N6306
2N6307
JAN, JANTX, & JANTXV 2N6308

	ins.	mm.
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)



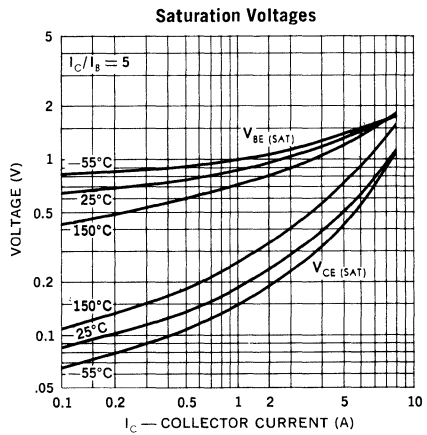
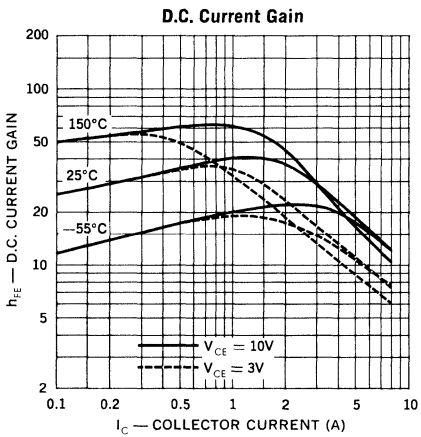
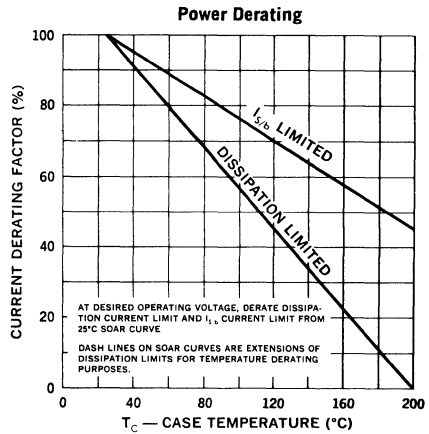
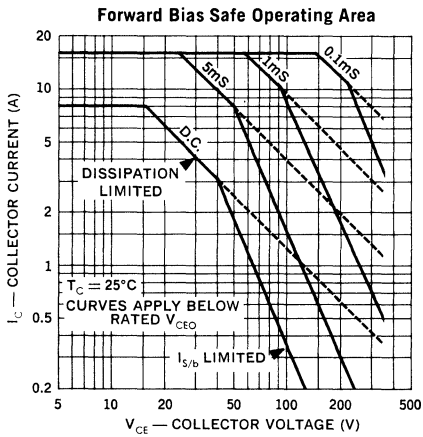
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

Test	Symbol	J, JTX, JTXV 2N6306		2N6307		J, JTX, JTXV 2N6308		Units	Test Conditions	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
D.C. Current Gain (Note 1)	h_{FE}	15	75	15	75	12	60		$I_C = 3A, V_{CE} = 5V$	
D.C. Current Gain (Note 1)	h_{FE}	4	—	4	—	3	—		$I_C = 8A, V_{CE} = 5V$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	0.8	—	1.0	—	1.5	V	$I_C = 3A, I_B = 0.6A$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	—	—	V	$I_C = 8A, I_B = 2A$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	—	—	—	—	5.0	V	$I_C = 8A, I_B = 2.67A$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	2.3	—	2.3	—	—	V	$I_C = 8A, I_B = 2A$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	—	—	—	—	2.5	V	$I_C = 8A, I_B = 2.67A$	
Base-Emitter Voltage (Note 1)	$V_{BE(on)}$	—	1.3	—	1.3	—	1.5	V	$I_C = 3A, V_{CE} = 5V$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(SUS)}$	250	—	300	—	350	—	V	$I_C = 100mA, I_B = 0$	
Emitter-Base Cutoff Current	I_{EBO}	—	1.0	—	1.0	—	1.0	mA	$V_{EB} = 8V$	
Collector Cutoff Current	I_{CEO}	—	0.5	—	—	—	—	mA	$V_{CE} = 250V$	
		—	—	—	0.5	—	—		$V_{CE} = 300V$	
		—	—	—	—	—	0.5		$V_{CE} = 350V$	
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	—	—	mA	$V_{BE} = -1.5V$	
		—	—	—	0.5	—	—			$V_{CE} = 500V$
		—	—	—	—	—	0.5			$V_{CE} = 700V$
Collector Cutoff Current, 150°C	I_{CEV}	—	2.5	—	—	—	—	mA	$V_{BE} = -1.5V$	
		—	—	—	2.5	—	—			$V_{CE} = 500V$
		—	—	—	—	—	2.5			$V_{CE} = 700V$
Second Breakdown Energy	$E_{S/b}$	180	—	180	—	180	—	mJ	$I_C = 3.0A, L = 40mH$ $R_{BE} = 3K\Omega, V_{BB2} = 1.5V$	
Collector Capacitance	C_{ob}	—	250	—	250	—	250	pF	$V_{CB} = 10V, I_E = 0, f = 1MHz$	
Gain-Bandwidth Product	f_T	5	—	5	—	5	—	MHz	$I_C = .3A, V_{CE} = 10V, f = 1MHz$	
Switching Speeds:										
Rise Time	t_r	—	0.6	—	0.6	—	0.6	μs	$V_{CC} = 125V, I_C = 3A$ $I_{B1} = 0.6A$	
Storage Time	t_s	—	1.6	—	1.6	—	1.6	μs	$V_{CC} = 125V, I_C = 3A$ $I_{B1} = 0.6A, I_{B2} = 1.5A$ Pulse Width = 25 μs	
Storage Time	t_s	—	0.8	—	0.8	—	0.8	μs	$V_{CC} = 125V, I_C = 3A$ $I_{B1} = 0.6A, I_{B2} = 1.5A$ Pulse Width = 5.0 μs	
Fall Time	t_f	—	0.4	—	0.4	—	0.4	μs	$V_{CC} = 125V, I_C = 3A$ $I_{B1} = 0.6A, I_{B2} = 1.5A$	
Thermal Resistance	$R_{\theta JC}$	—	1.0	—	1.0	—	1.0	°C/W		

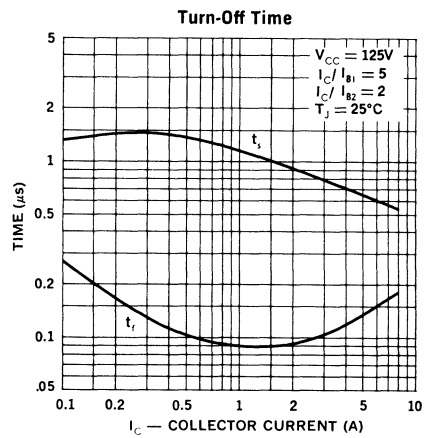
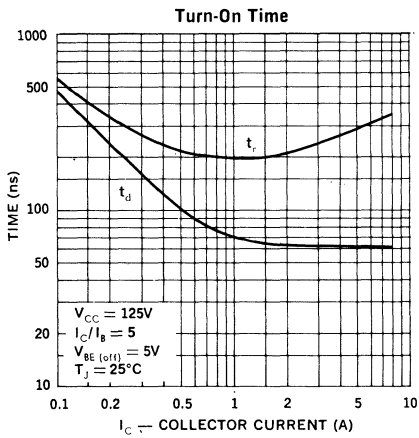
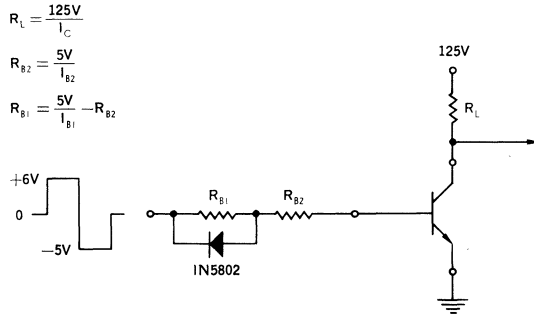
Notes:

1. Pulse width = 250 μs ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu s$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

* JEDEC registered values.



Switching Time Test Circuit



POWER DARLINGTONS

5 Amp, 150V, NPN

JAN, JANTX & JANTXV 2N6350
 JAN, JANTX & JANTXV 2N6351
 JAN, JANTX & JANTXV 2N6352
 JAN, JANTX & JANTXV 2N6353

FEATURES

- High Current Gain: up to 2000 min. @ $I_C = 5A$
- Low Saturation Voltage: as low as 1.5V max. @ $I_C = 2A$
- Peak Current: to 10A
- JAN/JANTX/JANTXV versions meet MIL-S-19500/472

DESCRIPTION

Unitrode NPN Darlington's consist of a two transistor circuit on a single monolithic planar chip. The 2N6350 series is characterized for fast switching applications.

4

ABSOLUTE MAXIMUM RATINGS

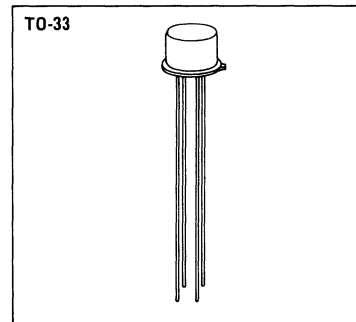
	TO-33		3 PIN TO-66	
	JAN, JANTX & JANTXV 2N6350	JAN, JANTX & JANTXV 2N6351	JAN, JANTX & JANTXV 2N6352	JAN, JANTX & JANTXV 2N6353
Collector—Emitter Voltage	80V	150V	80V	150V
Emitter—Base Voltages				
V_{EB2}	6V	6V	6V	6V
V_{EB1}	12V	12V	12V	12V
D.C. Collector Current	5A	5A	5A	5A
Peak Collector Current	10A	10A	10A	10A
Base 1 Current	0.5A	0.5A	0.5A	0.5A
Power Dissipation				
25°C Ambient	1W	1W	2W	2W
100°C Case	5W	5W	25W	25W
Thermal Resistance				
Junction-to-Case				
Operating and Storage Temperature Range				

MECHANICAL SPECIFICATIONS

JAN, JANTX & JANTXV 2N6350 JAN, JANTX & JANTXV 2N6351

	ins	mm
A	305-335	7.75-8.51
B	335-370	8.51-9.40
C	240-260	6.10-6.60
D	0.17 + 0.02 / 0.01	4.32 ± 0.51 / 0.25
E	1.5 MIN	38.10 MIN
F	0.18 MAX	0.46 MAX
G	0.31 ± 0.03	0.79 ± 0.08
H	200	1.02
J	100	2.54
K	0.29-0.45	0.74-1.14
L	100	2.54

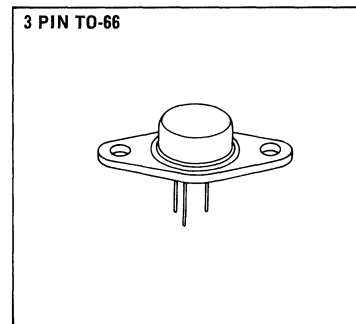
COLLECTOR CONNECTED TO CASE



JAN, JANTX & JANTXV 2N6352 JAN, JANTX & JANTXV 2N6353

	ins	mm
A	250-340	6.35-8.64
B	620 MAX	15.75 MAX
C	0.50-0.75	1.27-1.91
D	0.28-0.34	0.71-0.86
E	360 MIN	9.14 MIN
F	9.58-9.62	24.33-24.43
G	190-210	4.83-5.33
H	190-210	4.83-5.33
J	350 MAX RAD	8.89 MAX RAD
K	5.70-5.90	14.48-14.99
L	1.42-1.52	3.61-3.86
M	1.45 MAX RAD	3.68 MAX RAD

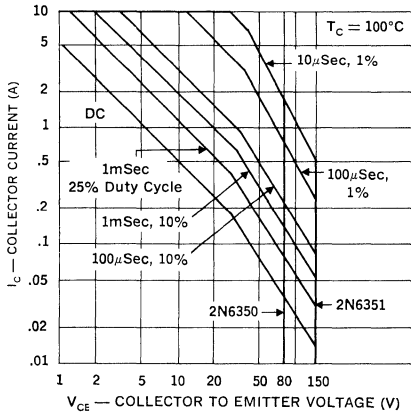
COLLECTOR CONNECTED TO CASE



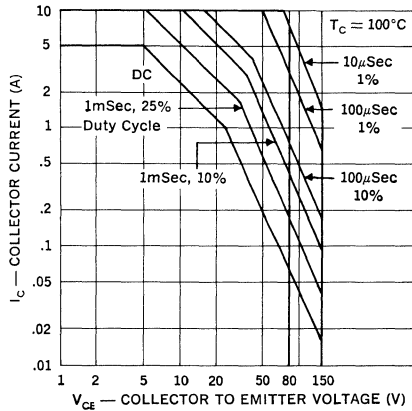
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Max.	Units	MIL-STD-750	
					Method	Test Conditions
Visual and Mechanical					2071	See Mechanical Data
25°C Collector-Emitter Breakdown Voltage 2N6350, 2N6352 2N6351, 2N6353	BV_{CER}	80 150		Vdc Vdc	3011	$I_C = 25mA, R_{BE1} = 2.2K, R_{BE2} = 100\text{ Ohms}$
Emitter Base Breakdown Voltage, Base 1 Emitter Base Breakdown Voltage, Base 2 Collector - Emitter Cutoff Current D.C. Current Gain 2N6350, 2N6352 2N6351, 2N6353	BV_{EBO1} BV_{EBO2} I_{CEX} h_{FE}	12 6 2000 1000	1.0	Vdc Vdc μAdc	3026 3026 3041 3076	$I_E = 12mA$ Base 2 Open $I_E = 12mA$ Base 1 Open $V_{CE} = BV_{CER}$ Rating $V_{CE} = 5Vdc; I_C = 1.0A$ (pulse) $R_{BE2} = 1K$
D.C. Current Gain 2N6350, 2N6352 2N6351, 2N6353	h_{FE}	2000 1000	10000 10000		3076	$V_{CE} = 5Vdc; I_C = 5.0Adc$ (pulse) $R_{BE2} = 100\text{ Ohms}$
D.C. Current Gain 2N6350, 2N6352 2N6351, 2N6353	h_{FE}	400 200			3076	$V_{CE} = 5Vdc; I_C = 10Adc$ (pulse) $R_{BE2} = 100\text{ Ohms}$
Collector Saturation Voltage 2N6350, 2N6352 2N6351, 2N6353	$V_{CE(sat)}$		1.5 2.5	Vdc Vdc	3071	$I_C = 5.0Adc, R_{BE2} = 100\text{ Ohms}$ $I_{B1} = 5mAdc$ (pulse) $I_{B1} = 10mAdc$ (pulse)
Base Saturation Voltage A.C. Current Gain Output Capacitance	$V_{BE1(on)}$ $ h_{FE} $ C_{OBO1}	5	2.5 25 120	Vdc pf	3066 3066 3236	$I_C = 5.0Adc$ (pulse), $V_{CE} = 5Vdc$ $R_{BE2} = 100\text{ Ohms}$ $V_{CE} = 10Vdc, I_C = 1.0Adc, f = 10MHz$ $R_{BE2} = 100\text{ Ohms}$ $V_{CB1} = 10Vdc, 100KHz \leq f \leq 1MHz$ Base 2 open
Turn-on Time Turn-off Time	t_{on} t_{off}		0.5 1.2	μs μs	3251 3251	$V_{CC} = 30Vdc; I_C = 5.0Adc$ See Switching Speed Circuit $V_{CC} = 30Vdc; I_C = 5.0Adc$ See Switching Speed Circuit
150°C Collector-Emitter Cutoff Current	I_{CEX}		1.0	μAdc	3041	$V_{BE1} = 2Vdc, R_{BE2} = 100\text{ Ohms}$ $V_{CE} = BV_{CER}$ Rating
-65°C D.C. Current Gain 2N6350, 2N6352 2N6351, 2N6353	h_{FE}	400 200			3076	$V_{CE} = 5Vdc, I_C = 5.0Adc$ (pulse) $R_{BE2} = 100\text{ Ohms}$

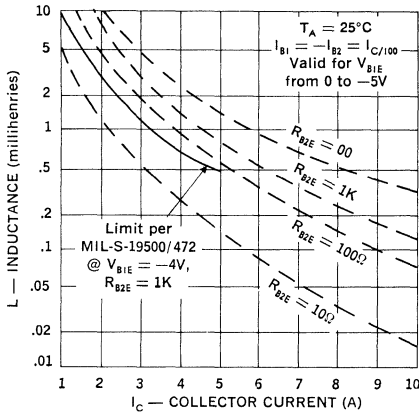
**Forward Bias
 Safe Operating Area
 2N6350, 2N6351**



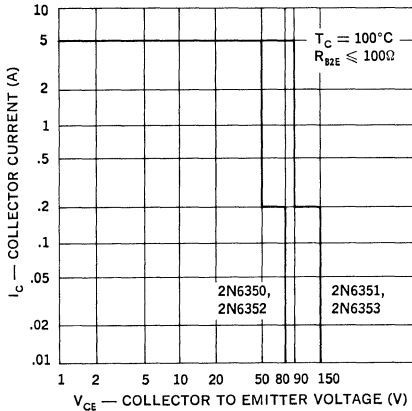
**Forward Bias
 Safe Operating Area
 2N6352, 2N6353**



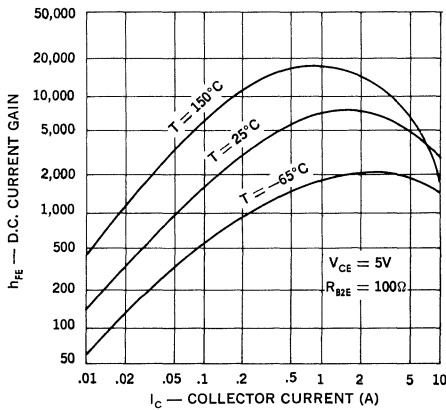
**Unclamped Reverse Bias
 Second Breakdown**



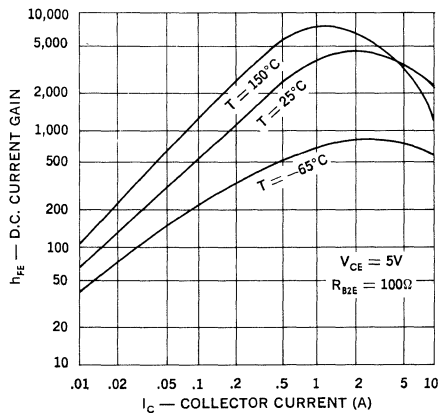
**Reverse Bias
 Safe Operating Area
 Clamped Inductive Switching**



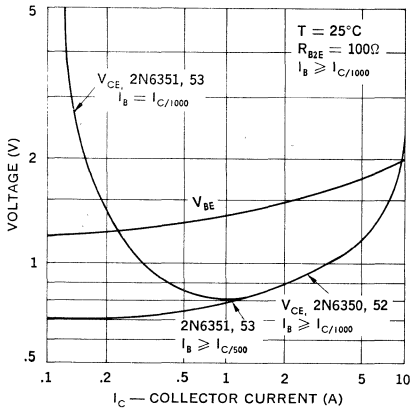
**D.C. Current Gain
 2N6350, 2N6352**



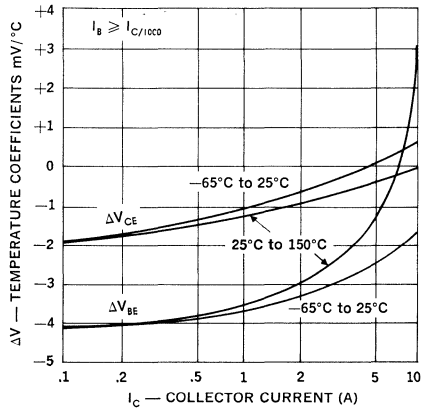
**D.C. Current Gain
 2N6351, 2N6353**



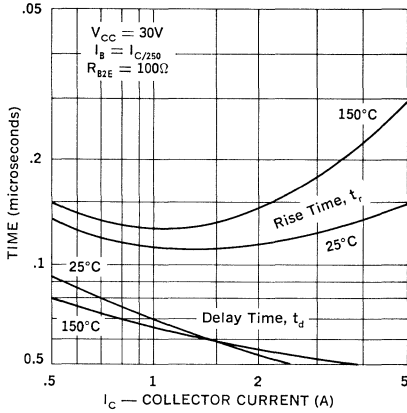
Saturation Voltages



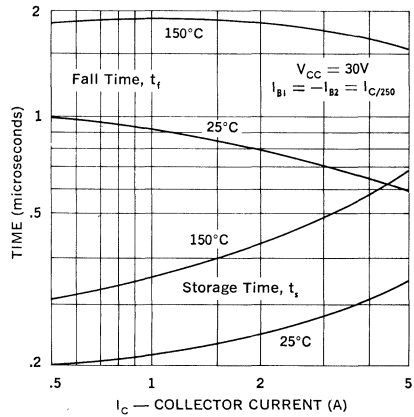
Saturation Voltage Temperature Coefficients



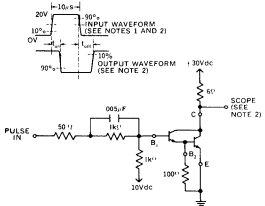
Switching Speed Characteristics



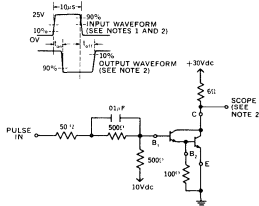
Switching Speed Characteristics



2N6350 & 52 Switching Speed Circuit

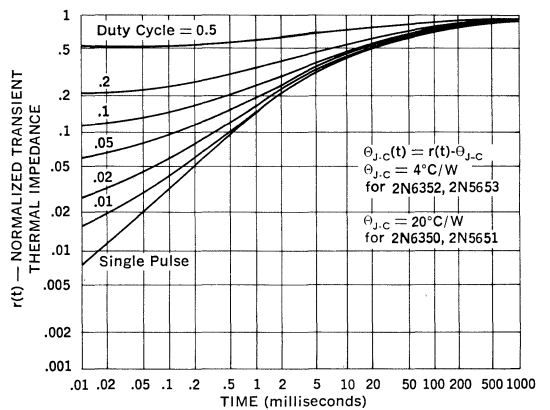


2N6351 & 3 Switching Speed Circuit

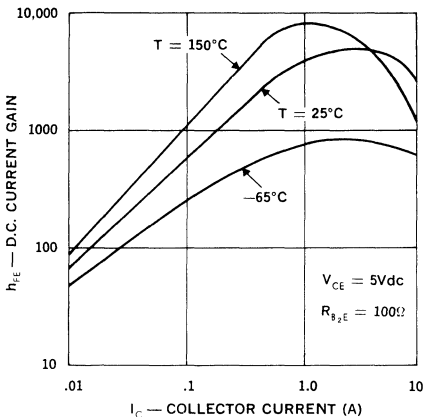


- NOTES**
1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_o = 50\Omega$, $PW = 10$ μ s, Duty cycle $\leq 2\%$.
 2. Output waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $Z_o \geq 10$ M Ω , $C_i \leq 11.5$ pF.
 3. Resistors shall be noninductive types.
 4. The DC power supplies may require additional by-passing in order to minimize ringing.

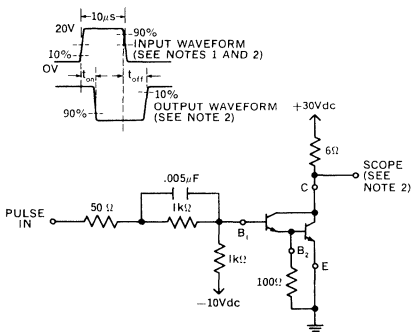
Thermal Response



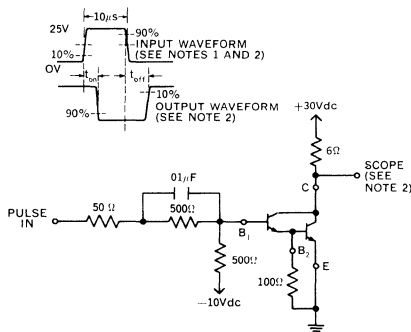
**D.C. Current Gain vs. Collector Current
 2N6350 — 2N6353**



2N6350 & 52 Switching Speed Circuit



2N6351 & 3 Switching Speed Circuit



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:
 $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{o,1} = 50\Omega$, $PW = 10 \mu s$,
 Duty cycle $\leq 2\%$.
2. Output waveforms are monitored on an oscilloscope with the following characteristics:
 $t_r \leq 15$ ns, $Z_{in} \geq 10 M\Omega$, $C_{in} \leq 11.5$ pF.
3. Resistors shall be noninductive types.
4. The DC power supplies may require additional by-passing in order to minimize ringing.

POWER TRANSISTORS

20 Amp, 150 V, Double Diffused NPN Mesa

2N6354
2N6496

FEATURES

- Collector-Base Voltage: up to 150V
- Peak Collector Current: 30A
- Rise Time: $\leq 500\text{ns}$ }
- Fall Time: $\leq 500\text{ns}$ } @ I_C up to 12A

DESCRIPTION

These double diffused glass passivated mesa power transistors combine fast-switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in switching regulators, converters, inverters and switching-control amplifiers.

ABSOLUTE MAXIMUM RATINGS*

	2N6354	2N6496
Collector-Base Voltage, V_{CBO}	150V	150V
Collector-Emitter Sustaining Voltage, $V_{CER(SUS)}$ (1)	—	130V
	$V_{CEO(SUS)}$ 120V	110V
Emitter-Base Voltage, V_{EBO}	6.5V	7V
Collector Current, I_C continuous	10A	15A
Collector Current, I_{CM} peak	12A	—
Base Current, I_B continuous	5A	.5A
Power Dissipation, 25°C Case	140W	140W
Operating and Storage Temperature Range	-65 to 200°C	

(1) With $R_{BE} \leq 50\Omega$

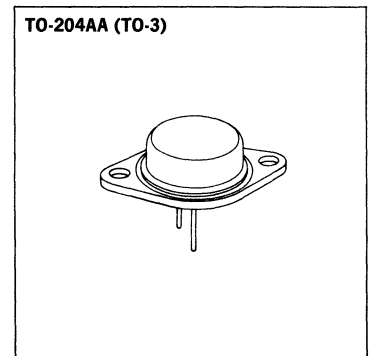
* JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.

2N6354, 2N6496

	ins.	mm.
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.



Electrical Specifications (at 25°C unless noted)

4

Test	Symbol	2N6354		2N6496		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
* D.C. Current Gain (Note 1)	h_{FE}	—	—	—	—		$I_C = 2A, V_{CE} = 5V$ $I_C = 5A, V_{CE} = 2V$
* D.C. Current Gain (Note 1)	h_{FE}	10	100	12	100		$I_C = 8A, V_{CE} = 2V$ $I_C = 10A, V_{CE} = 2V$
* D.C. Current Gain (Note 1)	h_{FE}	—	—	—	—		$I_C = 10A, V_{CE} = 5V$ $I_C = 12A, V_{CE} = 5V$
* Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	0.5	—	—	V	$I_C = 5A, I_B = .5A$ $I_C = 8A, I_B = .8A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	—	V	$I_C = 10A, I_B = 1.0A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	—	—	—	V	$I_C = 12A, I_B = 1.2A$ $I_C = 20A, I_B = 5A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.3*	—	—	V	$I_C = 5A, I_B = 0.5A$ $I_C = 8A, I_B = 0.8A$
* Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	2.0	—	—	V	$I_C = 10A, I_B = 1A$ $I_C = 20A, I_B = 5A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	120	—	100	—	V	$I_C = 0.2A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEX(sus)}$	—	—	—	—	V	$I_C = 0.2A$ $V_{BE} = -1.5V$ $I_B = 0$ $R_{BE} = 100\ \Omega$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CER(sus)}$	130	—	130	—	V	$R_{BE} = 50\ \Omega, I_C = 0.2A$ $R_{BE} = 100\ \Omega, I_C = 0.2A$
* Emitter-Base Voltage	V_{EBO}	6.5	—	—	—	V	$I_E = 5mA$ $I_E = 50mA$
* Collector Cutoff Current	I_{CBO}	—	5	—	—	mA	$V_{CB} = 150V$
Collector Cutoff Current	I_{CEO}	—	—	—	—	mA	$V_{CE} = 55V$ $V_{CE} = 70V$ $V_{CE} = 100V$
* Collector Cutoff Current	I_{CEV}	—	—	—	20	mA	$V_{CE} = 110V, V_{BE} = -1.5V$ $V_{CE} = 130V, V_{BE} = 0$ $V_{CE} = 140V, V_{BE} = -1.5V$ $V_{CE} = 140V, V_{BE} = 0$
* Collector Cutoff Current, 125°C	I_{CEV}	—	20	—	—	mA	$V_{CE} = 140V$
* Collector Cutoff Current, 150°C	I_{CEV}	—	—	—	—	mA	$V_{CE} = 85V, V_{BE} = -1.5V$ $V_{CE} = 100V, V_{BE} = -1.5V$ $V_{CE} = 130V, V_{BE} = 0V$
* Emitter Cutoff Current	I_{EBO}	—	5.0	—	—	mA	$V_{BE} = -5V$ $V_{BE} = -6.5V$ $V_{BE} = -7V$
Magnitude of Small Signal Forward — Current Transfer Ratio	$ h_{fe} $	8.0	—	12	—		$V_{CE} = 10V, I_C = 2A, f = 5\text{ MHz}$ $V_{CE} = 10V, I_C = 1A, f = 10\text{ MHz}$
Collector Capacitance	C_{ob}	—	300	—	300	pF	$V_{CB} = 10V, f = 1\text{ MHz}$
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$	—	—	—	1.25	°C/W	$V_{CE} = 10V, I_C = 10A$ $V_{CE} = 20V, I_C = 1A$

Notes:

1. Pulse width = 250 μ S; duty cycle \leq 1%.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length \approx 50 μ S; duty cycle \leq 1%.

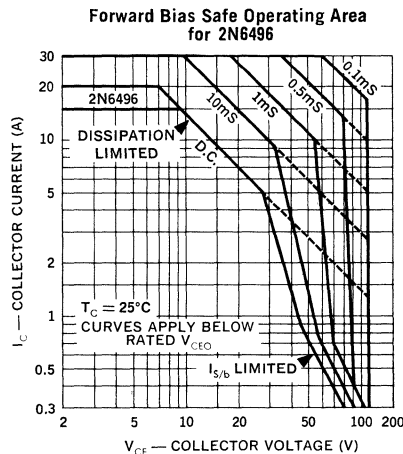
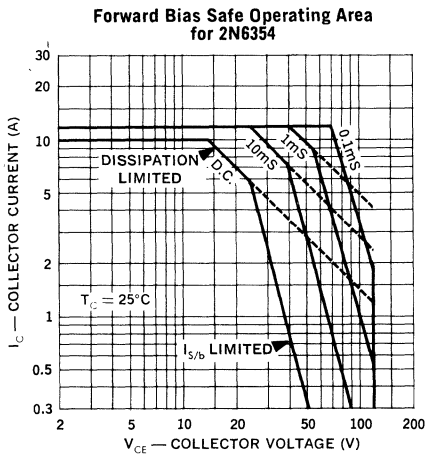
Voltage clamped at maximum collector-emitter voltage.

* JEDEC registered values.

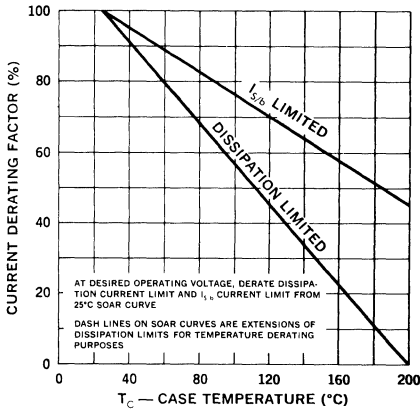
Electrical Specifications (at 25°C unless noted)

Test	Symbol	2N6354		2N6496		Units	Test Conditions	
		MIN.	MAX.	MIN.	MAX.			
Second Breakdown Energy	$E_{s/b}$	0.3	—	—	—	mJ	$I_C = 5A, V_{BE} = -1.0V$ $R_{BE} = 51 \Omega, L = 25\mu H$	
		—	—	5.7	—		$I_C = 8A, V_{BE} = -4.0V$ $R_{BE} = 20 \Omega, L = 180\mu H$	
		—	—	—	—		$I_C = 13A, V_{BE} = -4.0V$ $R_{BE} = 20 \Omega, L = 180\mu H$	
Forward Bias Second Breakdown Collector Current	$I_{s/b}$	5.5	—	—	—	A	$V_{CE} = 25V, t = 1s, \text{non-rep.}$	
		—	—	5.0	—		$V_{CE} = 28V, t = 1s, \text{non-rep.}$	
		—	—	0.9	—		$V_{CE} = 45V, t = 1s, \text{non-rep.}$	
* Switching Speeds	Rise Time	t_r	—	0.3	—	μS	$I_C = 5A$ $I_{B1} = I_{B2} = .5A$ $V_{CC} = 30V$	
	Storage Time	t_s	—	1.0	—			
	Fall Time	t_f	—	0.2	—			
	Rise Time	t_r	—	—	—	0.5	μS	$I_C = 8A$ $I_{B1} = I_{B2} = .8A$ $V_{CC} = 30V$
	Storage Time	t_s	—	—	—	1.5		
	Fall Time	t_f	—	—	—	0.5		
	Rise Time	t_r	—	—	—	—	μS	$I_C = 10A$ $I_{B1} = I_{B2} = 1.0A$ $V_{CC} = 30V$
	Storage Time	t_s	—	—	—	—		
	Fall Time	t_f	—	—	—	—		
	Rise Time	t_r	—	—	—	—	μS	$I_C = 12A$ $I_{B1} = I_{B2} = 1.2A$ $V_{CC} = 30V$
	Storage Time	t_s	—	—	—	—		
	Fall Time	t_f	—	—	—	—		

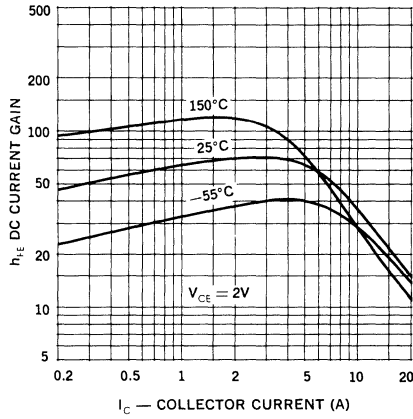
* JEDEC registered values.



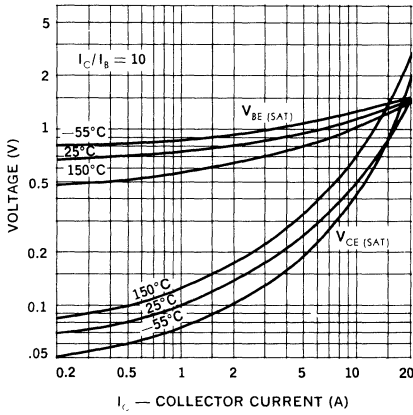
Power Derating



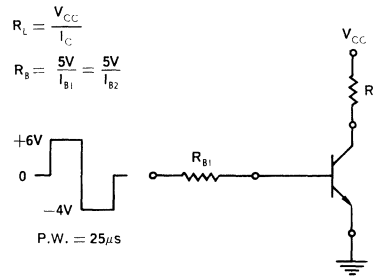
DC Current Gain



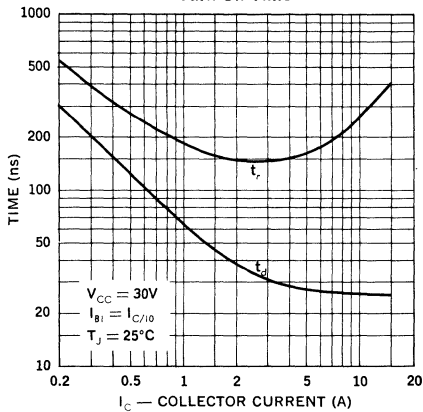
Saturation Voltages



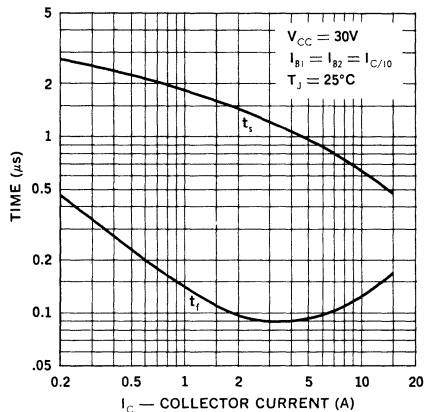
Switching Time Test Circuit



Turn-On Time



Turn-Off Time



POWER TRANSISTORS

7 Amp, 400V, Triple Diffused NPN Mesa

2N6510
2N6511
2N6512
2N6513
2N6514

FEATURES

- Collector-Base Voltage: up to 400V
- Peak Collector Current: 10A
- Rise Time: $\leq 1.5\mu\text{s}$
- Fall Time: $\leq 1.5\mu\text{s}$ } @ $I_C = 4\text{A}$

DESCRIPTION

These high voltage triple diffused glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

ABSOLUTE MAXIMUM RATINGS

	2N6510	2N6511	2N6512	2N6513	2N6514
*Collector Base Voltage, V_{CPO}	250V	300V	350V	400V	350V
Collector-Emitter Sustaining Voltage, $V_{CER(sus)}$ (1)	250V	300V	350V	400V	350V
*Collector-Emitter Sustaining Voltage, $V_{CEO(sus)}$	200V	250V	300V	350V	300V
*Emitter-Base Voltage, V_{EBO}	6V	6V	6V	6V	6V
*Collector Current, I_C continuous	7A	7A	7A	7A	7A
*Base Current, I_B	10A	10A	10A	10A	10A
*Emitter Current, I_E	3A	3A	3A	3A	3A
*Power Dissipation, P_T 25°C Case	120W	120W	120W	120W	120W
*Operating and Storage Temperature Range	-65 to +200°C				

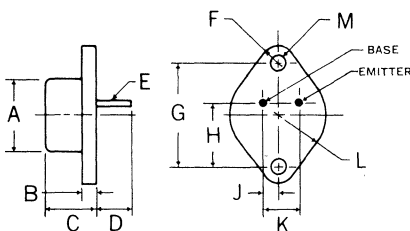
(1) $R_{\theta E} = 50\Omega$

*JEDEC registered values

MECHANICAL SPECIFICATIONS

NOTE:

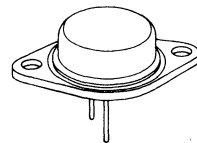
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



2N6510 2N6511 2N6512 2N6513 2N6514

	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	.312 MIN	7.92 MIN
E	.038-.043 DIA.	0.97-1.09 DIA
F	188 MAX RAD.	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	.525 MAX. RAD	13.34 MAX. RAD
M	151-161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	2N6510		2N6514		Units	Test Conditions
		Min.	Max.	Min.	Max.		
*D.C. Current Gain (Note 1)	h_{FE}	10	50	—	—		$I_C = 3A, V_{CE} = 3V$
		—	—	10	50		$I_C = 5A, V_{CE} = 3V$
*Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	—	V	$I_C = 3A, I_B = 0.6A$
		—	—	—	1.5		$I_C = 5A, I_B = 1A$
		—	2.5	—	2.5		$I_C = 7A, I_B = 3A$
*Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.7	—	—	V	$I_C = 3A, I_B = 0.6A$
		—	—	—	1.7		$I_C = 5A, I_B = 1A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	200*	—	300*	—	V	$I_C = 0.2A$
	$V_{CER(sus)}$	250	—	350	—	V	$I_C = 0.2A, R_{BE} = 50\Omega$
*Collector Cutoff Current	I_{CEV}	—	5.0	—	—	mA	$V_{CE} = 250V, V_{BE} = -1.5V$
		—	—	—	5.0		$V_{CE} = 350V, V_{BE} = -1.5V$
*Collector Cutoff Current 100°C	I_{CEV}	—	10	—	—	mA	$V_{CE} = 250V, V_{BE} = -1.5V$
		—	—	—	10		$V_{CE} = 350V, V_{BE} = -1.5V$
*Switching Speeds						μS	$V_{CC} = 200V$ $I_C = 3A$ $I_{B1} = I_{B2} = 0.6A$
Delay Time	t_d	—	0.2	—	—		
Rise Time	t_r	—	1.5	—	—		
Storage Time	t_s	—	5.0	—	—		
Fall Time	t_f	—	1.5	—	—		
Delay Time	t_d	—	—	—	0.2	μS	$V_{CC} = 200V$ $I_C = 5A$ $I_{B1} = I_{B2} = 1A$
Rise Time	t_r	—	—	—	1.5		
Storage Time	t_s	—	—	—	5.0		
Fall Time	t_f	—	—	—	1.5		

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	2N6511		2N6512		2N6513		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
*D.C. Current Gain (Note 1)	h_{FE}	10	50	10	50	10	50		$I_C = 4A, V_{CE} = 3V$
*Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	—	1.5		V
		—	2.5	—	2.5	—	2.5	$I_C = 7A, I_B = 3A$	
*Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.7	—	1.7	—	1.7	V	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	250	—	300	—	350	—	V	$I_C = 0.2A$
	$V_{CER(sus)}$	300	—	350	—	400	—	V	$I_C = 0.2A, R_{BE} = 50\Omega$
*Collector Cutoff Current	I_{CEV}	—	5.0	—	—	—	—	mA	$V_{CE} = 300V, V_{BE} = -1.5V$
		—	—	—	5.0	—	—		$V_{CE} = 350V, V_{BE} = -1.5V$
		—	—	—	—	—	5.0		$V_{CE} = 400V, V_{BE} = -1.5V$
*Collector Cutoff Current, 100°C	I_{CEV}	—	10	—	—	—	—	mA	$V_{CE} = 300V, V_{BE} = -1.5V$
		—	—	—	10	—	—		$V_{CE} = 300V, V_{BE} = -1.5V$
		—	—	—	—	—	10		$V_{CE} = 400V, V_{BE} = -1.5V$
*Switching Speeds								μS	$V_{CC} = 200V$ $I_C = 4A$ $I_{B1} = I_{B2} = 0.8A$
Delay Time	t_d	—	0.2	—	0.2	—	0.2		
Rise Time	t_r	—	1.5	—	1.5	—	1.5		
Storage Time	t_s	—	5.0	—	5.0	—	5.0		
Fall Time	t_f	—	1.5	—	1.5	—	1.5		

Notes:

1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\cong 50\mu S$; duty cycle $\leq 1\%$.

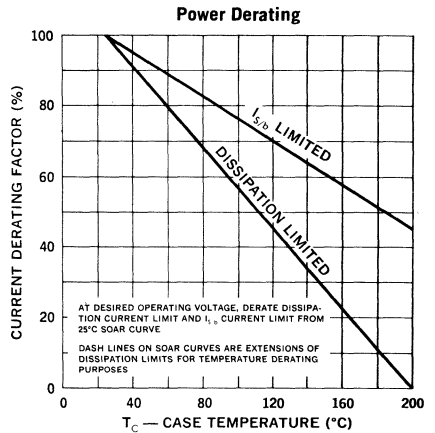
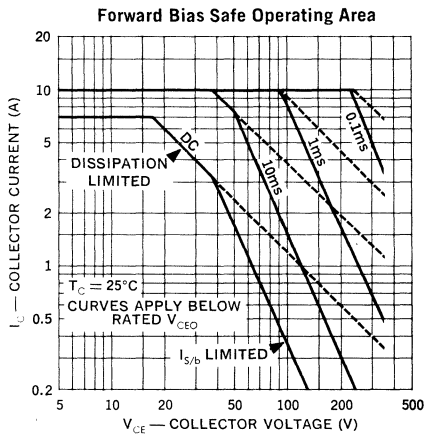
* Voltage clamped at maximum collector-emitter voltage.

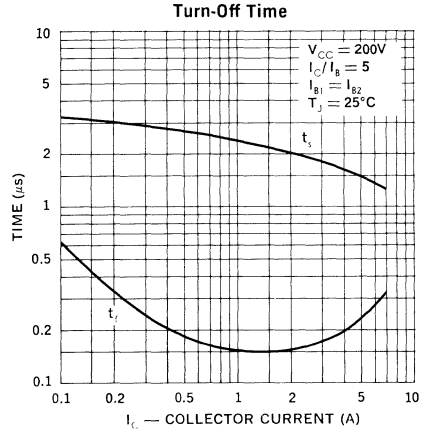
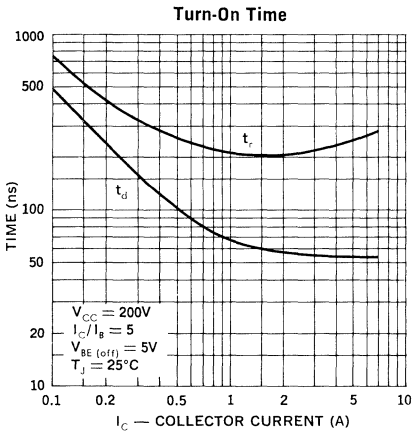
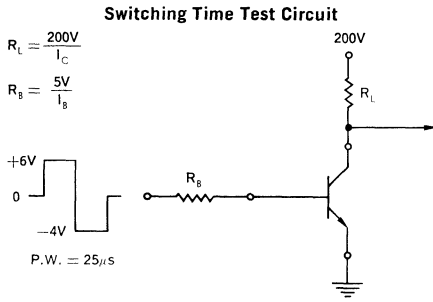
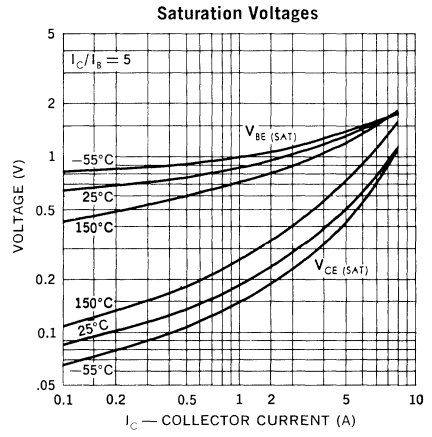
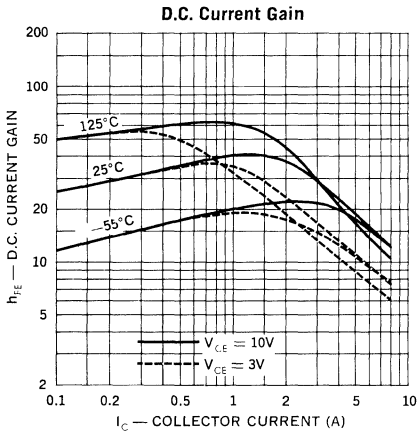
* JEDEC registered values.

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

Test	Symbol	All Types		Units	Test Conditions
		Min.	Max.		
Emitter-Base Cutoff Current	I_{EBO}	—	3.0	mA	$V_{EB} = 6V$
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio	$ h_{fe} $	3	9		$I_C = 1A$ $V_{CE} = 10V$ $f = 1MHz$
Forward-Bias Second Breakdown Collector Current	$I_{S/b}$	3.16	—	A	$V_{CE} = 35V, t = 1s, \text{non-rep.}$
		0.1	—	A	$V_{CE} = 200V, t = 1s, \text{non-rep.}$
Collector Capacitance	C_{ob}	100	200	pF	$V_{CB} = 10V, f = 1MHz$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.46	°C/W	$V_{CE} = 20V, I_C = 5A$

* All values in this table are JEDEC registered.





POWER TRANSISTORS

5A, 850V, Fast Switching,
Silicon NPN Mesa

2N6542
2N6543

FEATURES

- Collector-Base Voltage: up to 850V
 - Peak Collector Current: 10A
 - Rise Time: $\leq 0.7 \mu\text{S}$
 - Fall Time: $\leq 0.8 \mu\text{S}$
 - Key Parameters characterized at 100°C
- @ $I_C = 3A$

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

ABSOLUTE MAXIMUM RATINGS *

	2N6542	2N6543
Collector-Base Voltage, V_{CBO}	650V	850V
Collector-Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter-Base Voltage, V_{EBO}	9V	9V
Collector Current, I_C , continuous	5A	5A
Collector Current, I_C , peak	10A	10A
Base Current, I_B , continuous	5A	5A
Power Dissipation, 25°C Case	100W	100W
Derating Factor	.571W/°C	.571W/°C
Operating and Storage Temperature Range	-65 to 200°C	

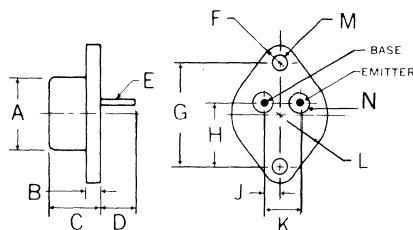
* JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

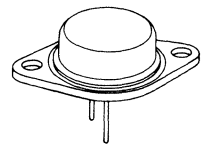
Leads may be soldered to within $1/16$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.

2N6542 2N6543



	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	312 MIN	7.92 MIN
E	0.38-0.43 DIA	0.97-1.09 DIA
F	1.88 MAX RAD	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	5.25 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA
N	190-210	4.83-5.33

TO-204AA (TO-3)



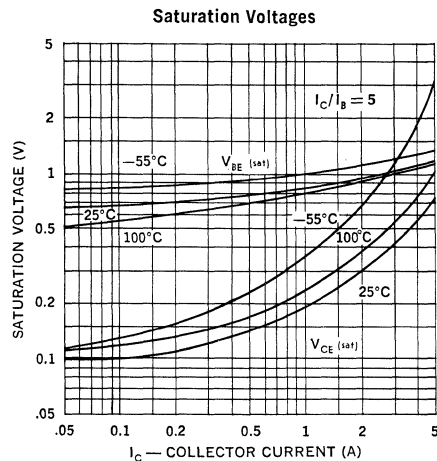
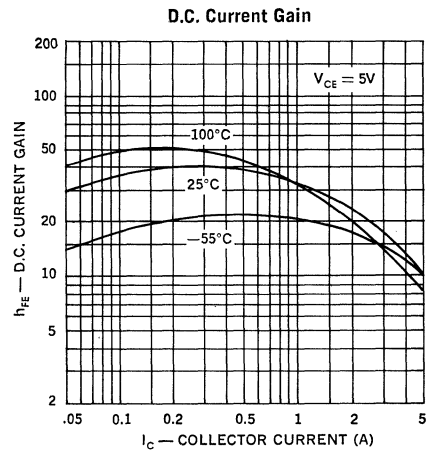
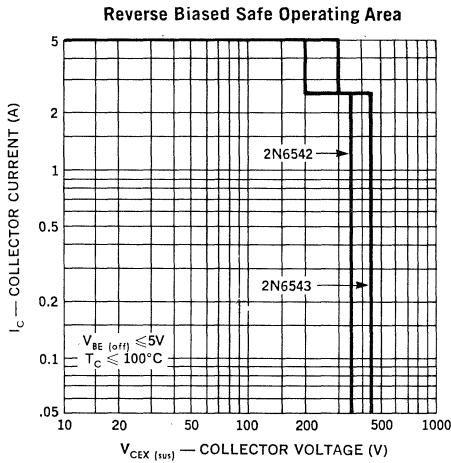
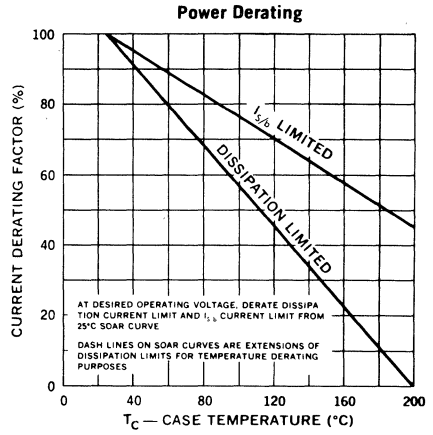
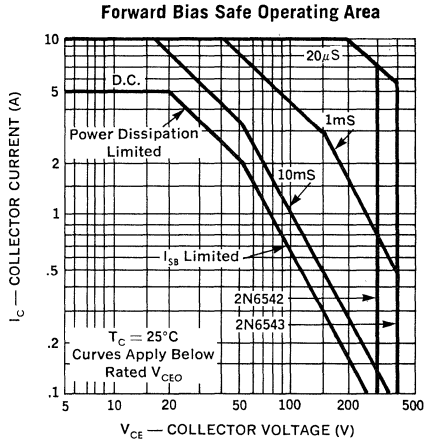
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

Test	Symbol	2N6542		2N6543		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 1.5A, V_{CE} = 2V$
D.C. Current Gain (Note 1)	h_{FE}	7	35	7	35		$I_C = 3.0A, V_{CE} = 2V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 3.0A, I_B = 0.6A$
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2.0	—	2.0	V	$I_C = 3.0A, I_B = 0.6A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 5.0A, I_B = 1.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.4	—	1.4	V	$I_C = 3.0A, I_B = 0.6A$
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.4	—	1.4	V	$I_C = 3.0A, I_B = 0.6A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A, I_B = 0$
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$L = 180\mu H, I_C = 2.6A$ $V_{BE} = -5V$ V_{CE} clamped to rated $V_{CEX(sus)}$
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	200	—	300	—	V	$L = 180\mu H, I_C = 5A$ $V_{BE(off)} = -5V$ V_{CE} clamp to $V_{CEO} - 100V$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
		—	—	—	0.5		$V_{CE} = 850V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	2.5	—	—	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
		—	—	—	2.5		$V_{CE} = 850V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 650V, R = 50\Omega$
		—	—	—	3.0		$V_{CE} = 850V, R = 50\Omega$
Output Capacitance, Common Base	C_{obo}	50	150	50	150	pF	$V_{CB} = 10V, f = 1\text{ MHz}$
Gain-Bandwidth Product	F_T	6	24	6	24	MHz	$V_{CE} = 10V, I_C = 0.2A, f = 1\text{ MHz}$
Forward Bias Second Breakdown	$I_{S/b}$	200	—	200	—	mA	P.W. = 1 sec. single shot $V_{CE} = 100V$
Energy Second Breakdown (unclamped)	$E_{S/b}$	180	—	180	—	μJ	$I_C = 3.0A$ $L = 40\mu H, V_{BE(off)} = 4.0\text{ Vdc}$
Resistive Switching Speeds							
Delay Time	t_d	—	0.05	—	0.05	μS	$I_C = 3.0A, t_p = 100\mu sec$ $V_{CC} = 250V$ $I_{B1} = I_{B2} = 0.6A$ $V_{BE(off)} = 5V$
Rise Time	t_r	—	0.7	—	0.7		
Storage Time	t_s	—	4.0	—	4.0		
Fall Time	t_f	—	0.8	—	0.8		
Inductive Switching Speeds							
$T_C = 100^\circ C$							$I_C = 3.0A$ $I_B = 0.6A, V_{BE(off)} = 5.0\text{ Vdc}$
Storage Time	t_s	—	4.0	—	4.0	μS	$V_{BE(off)} = 5V$ V_{CE} clamp = rated $V_{CEX(sus)}$
Fall Time	t_f	—	0.8	—	0.8		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.75	—	1.75	$^\circ C/W$	

Notes:

1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

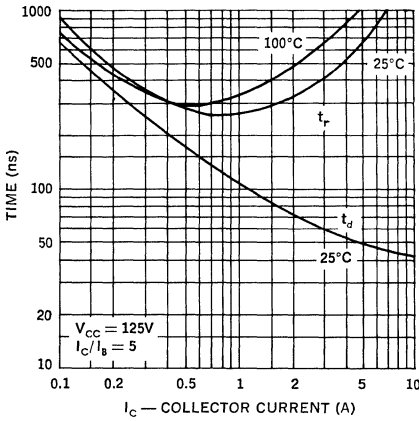
* JEDEC registered values.



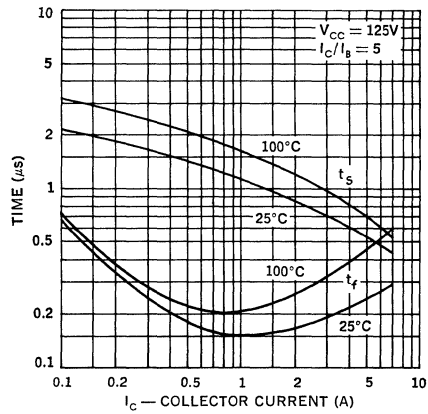
Typical Inductive Load Switching Performance

I_C Amps	T_J $^\circ\text{C}$	t_s μs	t_{fv} nS	t_{fi} nS
3.0	25	.45	70	10
	100	.575	100	20
5.0	25	.475	25	4
	100	.60	45	10
8.0	25	.525	20	10
	100	.625	45	15

Resistive Turn-On Time



Resistive Turn-Off Time



TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEQ}(I_{C(SUS)})$	$V_{CEX}(I_{C(SUS)})$ AND INDUCTIVE SWITCHING	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>+10V 20Ω 0 PW Varied to Attain $I_c = 100mA$</p>	<p>Drive Circuit +4V -4V 1k 0.01μF 20 100 0.1μF 20 100 0.5μF 100 +V_{in} -5V Set +V_{in} to Obtain a Forced $h_{FE} = 5$ and Adjust PW to Attain Specified Peak I_{C1}. Duty Cycle $\leq 3\%$ $f = 1kHz$ Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933</p>	<p>15Ω 10Ω +175V 4V PW Varied to Attain I_c</p>	<p>≈ +13V ≈ -11V $I_c = 3A$ PW $\leq 100\mu s$ $t_s \leq 5ns$ $t_f \leq 50ns$ Duty Cycle $\leq 2\%$</p>
CIRCUIT VALUES	$L_{coil} = 80mH$ $V_{CC} = 10V$ $R_{coil} = 0.7\Omega$ V_{clamp} (Unclamped)	$L_{coil} = 180\mu H$ $R_{coil} = 0.05\Omega$ $V_{CC} = 20V$ $f_o = 500kHz$ $V_{clamp} = \text{Rated } V_{L,EX} \text{ Value}$	$L_{coil} = 40\mu H$ $V_{CC} = 10V$ $R_{coil} = 0.2\Omega$ V_{clamp} (Unclamped)	$V_{CC} = 250V$ $R_L = 83\Omega$ D1 = 1N5820 or Equiv. $R_B = 20\Omega$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_r Clamped t_f Unclamped = t_s</p> <p>$t_1 \approx \frac{L_{coil}(I_{Cpl})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpl})}{V_{clamp}}$</p> <p>Test Equipment Tektronix Scope 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>	

POWER TRANSISTORS

8 Amp, 850V, Triple Diffused, NPN, Mesa

2N6544
2N6545

FEATURES

- Collector-Base Voltage: up to 850V
- Peak Collector Current: 16A
- Rise Time: $\leq 1.0\mu\text{s}$
- Fall Time: $\leq 1.0\mu\text{s}$ } @ $I_C = 5\text{A}$
- Key Parameters characterized at 100°C

DESCRIPTION

These high voltage triple diffused glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

ABSOLUTE MAXIMUM RATINGS*

	2N6544	2N6545
Collector-Base Voltage, V_{CBO}	650V	850V
Collector-Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter-Base Voltage, V_{EBO}	9V	9V
Collector Current, I_C , continuous	8A	8A
Base Current, I_B , continuous	8A	8A
Emitter Current, I_E , continuous	16A	16A
Power Dissipation, 25°C Case	125W	125W
Derating Factor	.714W/°C	.714W/°C
Operating and Storage Temperature Range	-65 to 200°C	

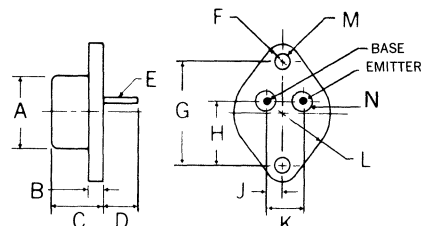
* JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

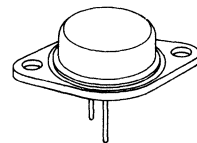
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.

2N6544 2N6545



	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	312 MIN	7.92 MIN
E	038-043 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA
N	190-210	4.83-5.33

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

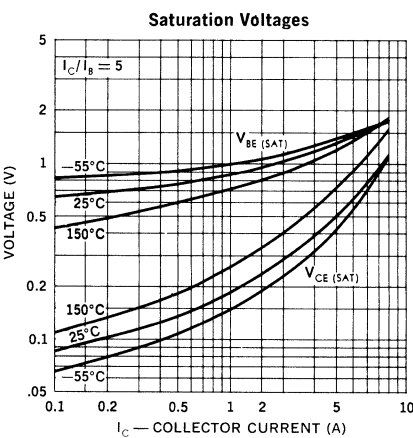
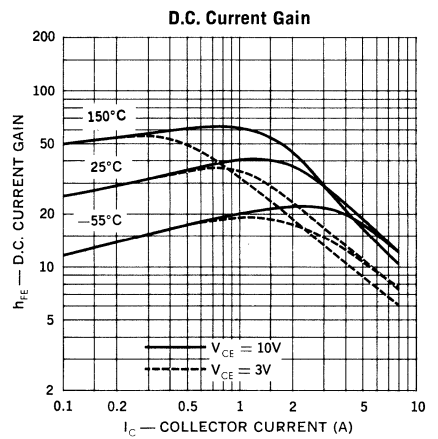
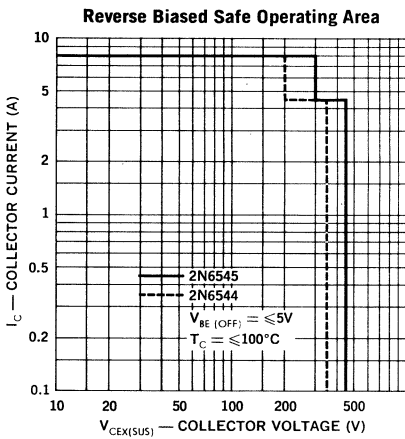
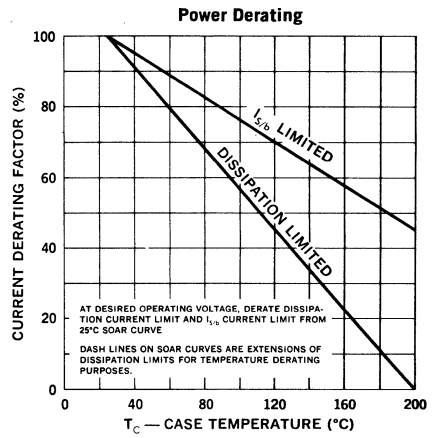
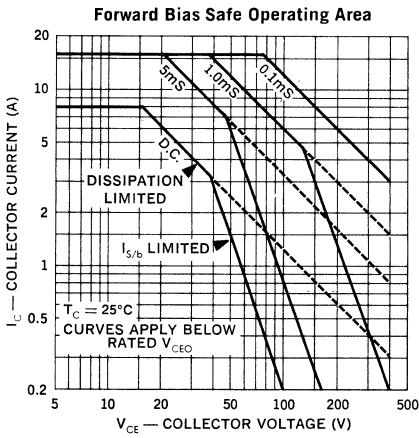
Test	Symbol	2N6544		2N6545		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 2.5A, V_{CE} = 3V$
D.C. Current Gain (Note 1)	h_{FE}	7	35	7	35		$I_C = 5.0A, V_{CE} = 3V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 5.0A, I_B = 1.0A$
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2.5	—	2.5	V	$I_C = 5.0A, I_B = 1.0A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 8.0A, I_B = 2.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 5.0A, I_B = 1.0A$
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 5.0A, I_B = 1.0A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A$
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$L = 180\mu H, I_C = 4.5A$ $V_{BE} = -5V$ V_{CE} clamped to rated $V_{CEX(sus)}$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
		—	—	—	0.5		$V_{CE} = 850V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	2.5	—	—	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
		—	—	—	2.5		$V_{CE} = 850V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 650V, R = 50\Omega$
		—	—	—	3.0		$V_{CE} = 850V, R = 50\Omega$
Output Capacitance, Common Base	C_{obo}	100	200	100	200	pF	$V_{CB} = 10V, f = 1 MHz$
Gain-Bandwidth Product	F_T	6	24	6	24	MHz	$V_{CE} = 10V, I_C = 0.3A, f = 1 MHz$
Energy Second Breakdown (unclamped)	$E_{S/b}$	500	—	500	—	μJ	$I_C = 5.0A$ $I_B = 1.0A$ $L = 40\mu H$
Resistive Switching Speeds	Delay Time	—	0.05	—	0.05	μs	$I_C = 5.0A$ $V_{CC} = 250V$ $I_{B1} = I_{B2} = 1.0A$ $V_{BE(off)} = 5V$
	Rise Time	—	1.0	—	1.0		
	Storage Time	—	4.0	—	4.0		
	Fall Time	—	1.0	—	1.0		
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	—	4.0	—	4.0	μs	$I_C = 5.0A$ $I_B = 1.0A$ $V_{BE(off)} = 5V$ V_{CE} clamp = rated $V_{CEX(sus)}$
	Fall Time	—	0.9	—	0.9		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.4	—	1.4	$^\circ C/W$	

Notes:

- Pulse width = 250 μs ; duty cycle $\leq 1\%$.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\cong 50\mu s$; duty cycle $\leq 1\%$.

Voltage clamped at maximum collector-emitter voltage.

* JEDEC registered values.

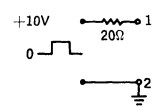
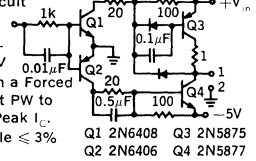
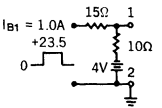
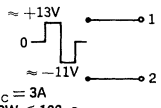
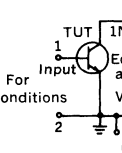
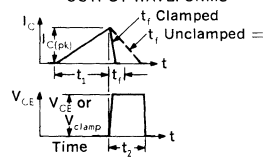
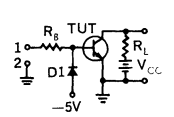


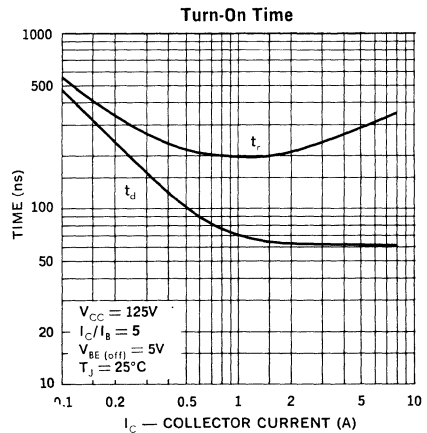
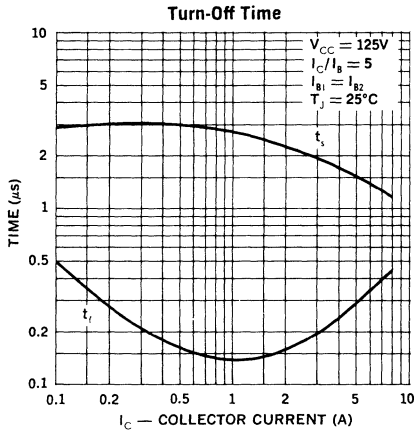
Inductive Load Switching Performance

I_C Amps	T_J $^\circ\text{C}$	t_s μs	t_{fv} μs	t_{fi} μs
3.0	25	.90	.07	.07
	100	1.40	.12	.15
5.0	25	.98	.10	.11
	100	1.52	.15	.20
8.0	25	1.10	.14	.11
	100	1.70	.20	.18

t_{fv} = voltage fall time; 10-90%
 t_{fi} = current fall time; 10-90%

TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE(SUS)}	V _{CEX (SUS)} AND INDUCTIVE SWITCHING	E _{S/b}	RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain I_C = 100mA</p>	<p>Drive Circuit</p>  <p>Set +V_{in} to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1kHz Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933</p>	<p>E_{S/b}</p>  <p>I_{B1} = 1.0A PW Varied to Attain I_C</p>	<p>RESISTIVE SWITCHING</p>  <p>I_C = 3A PW ≤ 100μs t_r ≤ 5ns t_f ≤ 50ns Duty Cycle ≤ 2%</p>	
<p>CIRCUIT VALUES</p> <p>L_{coil} = 80mH V_{CC} = 10V R_{coil} = 0.7Ω V_{clamp} (Unclamped)</p>	<p>L_{coil} = 180μH R_{coil} = 0.05Ω V_{CC} = 20V f_o = 500kHz V_{clamp} = Rated V_{CEX} Value</p>	<p>L_{coil} = 40μH V_{CC} = 10V R_{coil} = 0.2Ω V_{clamp} (Unclamped)</p>	<p>V_{CC} = 250V R_L = 83Ω D1 = 1N5820 or Equiv. R_B = 20Ω</p>	
<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_i Clamped t_f Unclamped = t_f</p>	<p>t_i Adjusted to Obtain I_C</p> $t_{i1} \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_{i2} \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Tektronix Scope 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 	



POWER TRANSISTORS

15A, 850V, Fast Switching,
Silicon NPN Mesa

JAN, JANTX, & JANTVX 2N6546
JAN, JANTX, & JANTVX 2N6547

FEATURES

- Collector-Emitter Voltage: up to 850V
 - Peak Collector Current: 30A
 - Rise Time: $\leq 0.7\mu\text{s}$
 - Fall Time: $\leq 0.7\mu\text{s}$
 - Qualified to MIL-S-19500/525
- } @ $I_C = 10\text{A}$

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/f}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

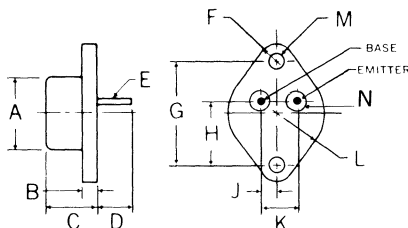
ABSOLUTE MAXIMUM RATINGS

	2N6546	2N6547
Collector-Emitter Sustaining Voltage, V_{CE}	650V	850V
Collector-Emitter Voltage, V_{CE0} (sus)	300V	400V
Emitter-Base Voltage, V_{EB0}	8V	8V
Collector Current, I_C , continuous	15A	15A
Collector Current, I_C peak	30A	30A
Base Current, I_B , continuous	10A	10A
Emitter Current, I_E , continuous	25A	25A
Power Dissipation, 25°C Case	175W	175W
Derating Factor	1W/°C	1W/°C
Operating and Storage Temperature Range	-65 to +200°C	

MECHANICAL SPECIFICATIONS

NOTE:

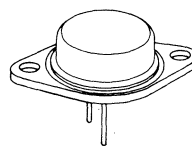
Leads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.



JAN, JANTX, & JANTXV 2N6546 JAN, JANTX, & JANTXV 2N6547

	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	312 MIN	7.92 MIN
E	0.38-0.43 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA
N	190-210	4.83-5.33

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

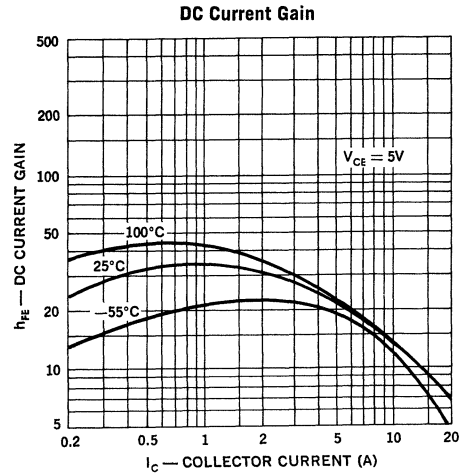
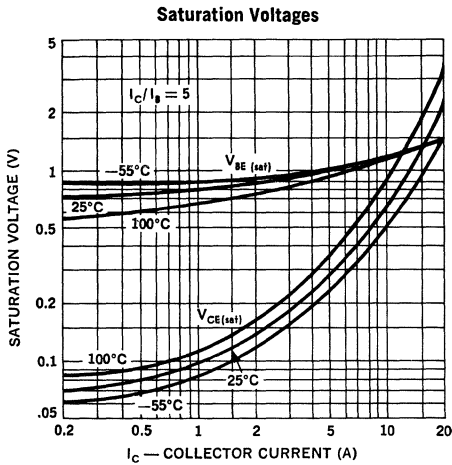
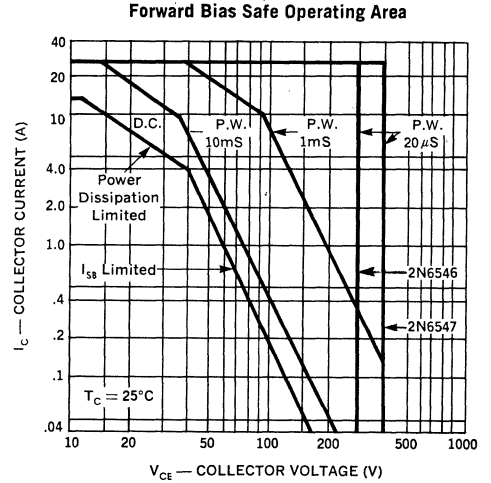
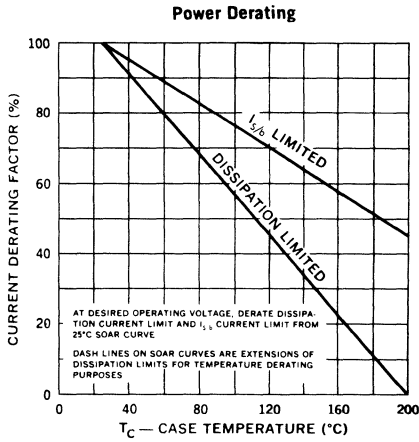


Test	Symbol	2N6546		2N6547		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 5.0A, V_{CE} = 2.0V$
D.C. Current Gain (Note 1)	h_{FE}	6	—	6	—		$I_C = 10A, V_{CE} = 2.0V$
D.C. Current Gain (Note 1)	h_{FE}	15	—	15	—		$I_C = 1A, V_{CC} = 2V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 10A, I_B = 2.0A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 15A, I_B = 3.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 10A, I_B = 2.0A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A, I_B = 0$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 8V$
Collector Cutoff Current	I_{CEX}	—	1	—	1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$ $V_{CE} = 850V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 150^\circ C$	I_{CEX}	—	30	—	30	mA	$V_{CE} = 650V, V_{BE} = -1.5V$ $V_{CE} = 850V, V_{BE} = -1.5V$
Output Capacitance Common Base	C_{obo}	—	500	—	500	pF	$V_{CB} = 10V, f = 1MHz$
Resistive Switching Speeds							
Turn-on Time	t_{ON}	—	1.0	—	1.0	μS	$I_C = 10A$ $V_{CC} = 250V$
Turn-off Time	t_{OFF}	—	4.7	—	4.7		$I_{B1} = I_{B2} = 2.0A$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.0	—	1.0	$^\circ C/W$	

Notes:

1. Pulse width = 250 μ S; duty cycle \leq 1%.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length \approx 50 μ S; duty cycle \leq 1%. Voltage clamped at maximum collector-emitter voltage.

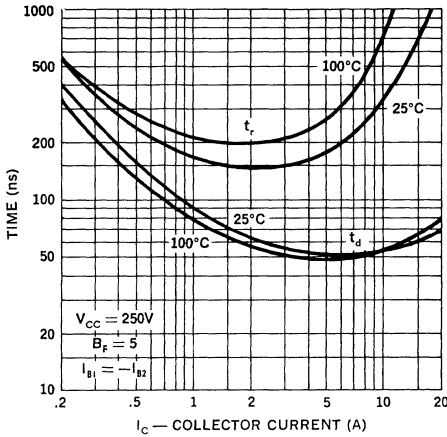
* JEDEC registered values.



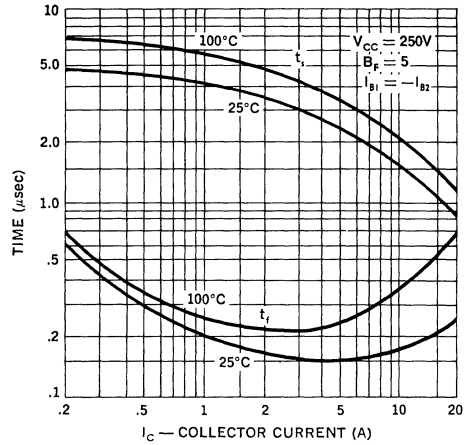
Typical Inductive Load Switching Performance

I_C Amps	T_J °C	t_t µS	t_{fv} nS	t_{fi} nS
3	25	.8	.14	.025
	100	1.10	.18	.030
5	25	.90	.14	.025
	100	1.20	.16	.030
10	25	1.20	.05	.050
	100	1.50	.12	.10

Resistive Turn-On Time



Resistive Turn-Off Time



TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	$E_{5/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>+10V 20Ω PW Varied to Attain $I_C = 100\text{mA}$</p>	<p>Drive Circuit</p> <p>Set +V_{in} to Obtain a Forced $h_{FE} = 5$ and Adjust PW to Attain Specified Peak I_C. Duty Cycle $\leq 3\%$ $f = 1\text{KHz}$ Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933</p>	<p>$I_{BA} = 2.0A$ 38.5V 4V PW Varied to Attain I_C</p>	<p>$\approx +13V$ 0 $\approx -11V$ $I_C = 10A$ PW $\leq 100\mu\text{s}$ $t_r \leq 5\text{ns}$ $t_f \leq 50\text{ns}$ Duty Cycle $\leq 2\%$</p>
CIRCUIT VALUES	$L_{coil} = 80\text{mH}$ $V_{CC} = 10V$ $R_{coil} = 0.7\Omega$ V_{clamp} (Unclamped)	$L_{coil} = 180\mu\text{H}$ $R_{coil} = 0.05\Omega$ $V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$ $V_{CC} = 20V$ $f_c = 500\text{kHz}$	$L_{coil} = 40\mu\text{H}$ $V_{CC} = 10V$ $R_{coil} = 0.2\Omega$ V_{clamp} (Unclamped)	$V_{CC} = 250V$ $R_L = 25\Omega$ $D1 = 1N5820$ or Equiv. $R_B = 6\Omega$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Tektronix Scope 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>	

POWER TRANSISTORS

8A, 400V, NPN Mesa

2N6671
2N6672
2N6673

FEATURES

- Collector Emitter Voltage: up to 650V
 - Peak Collector Current: 10A
 - Storage Time $\leq 2.5\mu\text{s}$
 - Fall Time $\leq 0.4\mu\text{s}$
- } at $I_C = 5A$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

ABSOLUTE MAXIMUM RATINGS*

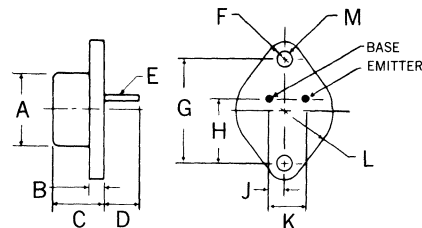
	2N6671	2N6672	2N6673
Collector Emitter Voltage, V_{CEV}	450V	550V	650V
Collector Emitter Voltage, V_{CEX}	350V	400V	450V
Collector Emitter Voltage, $V_{CEO (ISUS)}$	300V	350V	400V
Emitter Base Voltage, V_{EBO}		8V	
Collector Current, I_C continuous		8A	
Collector Current, $I_{CM(PEAK)}$		12A	
Base Current, I_B continuous		4A	
Power Dissipation, up to 25°C		150W	
above 25°C, derate linearly		0.86W/°C	
Operating and Storage Temperature Range		-65°C to +200°C	

*JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

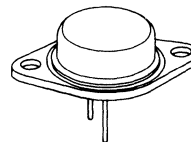
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



2N6671 2N6672 2N6673

	INCHES	MILLIMETERS
A	875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-.043 DIA	6.35-11.43
D	312 MIN	7.92 MIN
E	038-.043 DIA	0.97-1.09 DIA
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1 177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-.440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	.151- .161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)

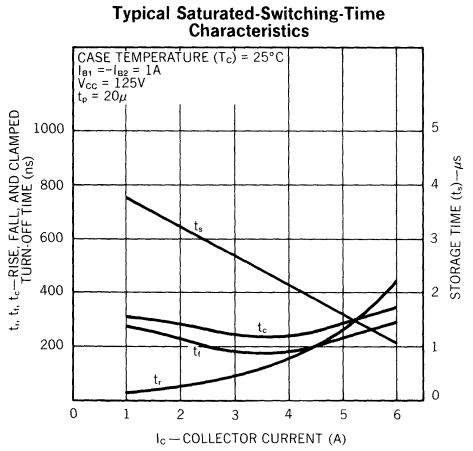
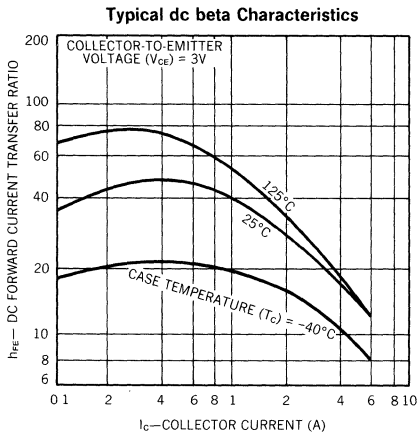
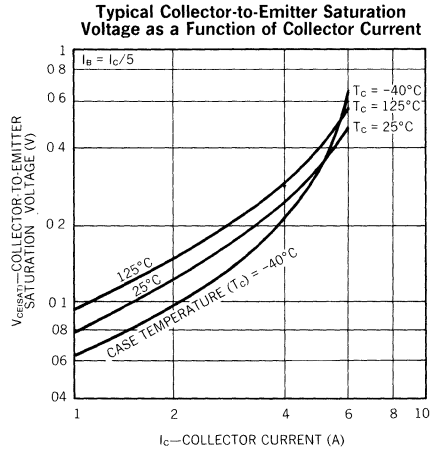
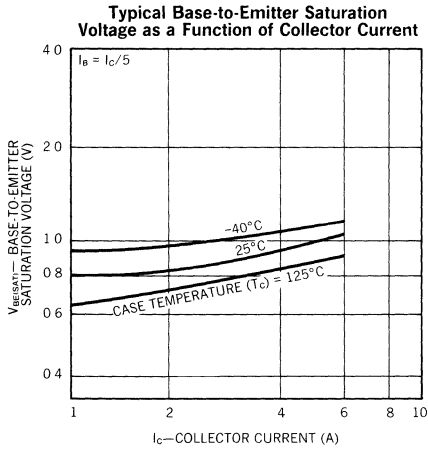


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

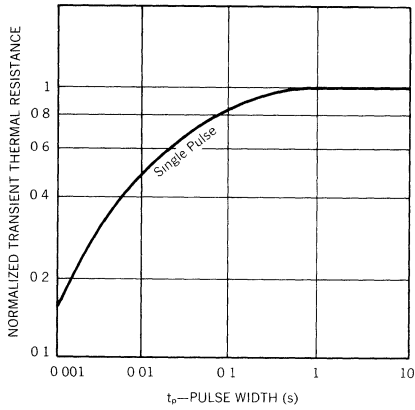
TEST	SYMBOL	2N6671		2N6672		2N6673		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Collector Cutoff Current	I_{CEV}	—	0.1	—	—	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	0.1	—	—	mA	$V_{CE} = 550V, V_{BE} = -1.5V$
		—	—	—	—	—	0.1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Collector Cutoff Current $T_C = 125^\circ C$	I_{CEV}	—	1	—	—	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	1	—	—	mA	$V_{CE} = 550V, V_{BE} = -1.5V$
		—	—	—	—	—	1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Emitter Base Cutoff Current	I_{EBO}	—	2	—	2	—	2	mA	$V_{BE} = -8V, I_C = 0$
Collector Emitter Sustaining Voltage (Notes 1 & 2)	$V_{CEO(sus)}$	300	—	350	—	400	—	V	$I_C = 0.2A, I_B = 0$
DC Current Gain (Note 1)	h_{FE}	10	40	10	40	10	40		$I_C = 5A, V_{CE} = 3V$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	—	1.6	V	$I_C = 5A, I_B = 1A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1	—	1	—	1	V	$I_C = 5A, I_B = 1A$
Collector Saturation Voltage $T_C = 125^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2	—	2	—	2	V	$I_C = 5A, I_B = 1A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	2	—	2	—	2	V	$I_C = 8A, I_B = 4A$
Collector Emitter Voltage (Note 2)	V_{CEX}	350	—	400	—	450	—	V	$L = 170\mu H, R_{BB} = 5\Omega$ $V_{BE} = -5V$ $I_C = 5A, I_B = 1A$
		200	—	250	—	300	—	V	$L = 170\mu H, R_{BB} = 5\Omega$ $V_{BE} = -5V$ $I_C = 8A, I_B = 3A$
AC Current Gain	$ h_{re} $	3	12	3	12	3	12		$I_C = 0.2A$ $V_{CE} = 10V$ $f = 5MHz$
Gain-Bandwidth Product	f_T	15	60	15	60	15	60	MHz	$V_{CE} = 10V, I_C = 0.2A$
Output Capacitance Common Base	C_{ob0}	50	300	50	300	50	300	pF	$V_{CB} = 10V, f = 0.1MHz$
Switching Speeds									
Delay Time	t_d	—	0.1	—	0.1	—	0.1	μs	$I_C = 5A, I_B = 1A$ $V_{CC} = 125V$ $t_p = 20\mu s$
Rise Time	t_r	—	0.5	—	0.5	—	0.5		
Storage Time	t_s	—	2.5	—	2.5	—	2.5	μs	$I_C = 5A, -I_B = 1A$ $V_{CC} = 125V$ $t_p = 20\mu s$
Fall Time	t_f	—	0.4	—	0.4	—	0.4		
Crossover Time	t_c	—	0.4	—	0.4	—	0.4	μs	$I_C = 5A, I_{B2} = 1A$ $V_{CC} = 125V$ $L_C = 170\mu H, R_C = 25\Omega$ Collector clamped to V_{CEX}
Switching Speeds $T_C = 125^\circ C$									
Rise Time	t_r	—	0.8	—	0.8	—	0.8	μs	$I_C = 5A, I_B = 1A$ $V_{CC} = 125V$ $t_p = 20\mu s$
Storage Time	t_s	—	4	—	4	—	4	μs	$I_C = 5A, -I_B = 1A$ $V_{CC} = 125V$ $t_p = 20\mu s$
Fall Time	t_f	—	0.8	—	0.8	—	0.8		
Crossover Time	t_c	—	0.8	—	0.8	—	0.8	μs	$I_C = 5A, I_{B2} = 1A$ $V_{CC} = 125V$ $L = 170\mu H, R_C = 25\Omega$ Collector clamped to V_{CEX}
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	1.17	—	1.17	—	1.17	$^\circ C/W$	

*JEDEC registered values.

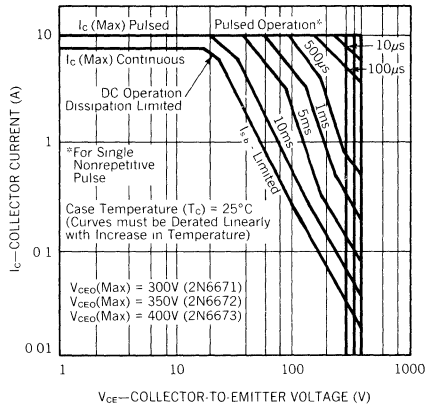
Notes: 1. Pulse duration = 300 μs ; duty factor $\leq 2\%$ 2. CAUTION: The sustaining voltage $V_{CEO(sus)}$ and V_{CEX} must not be measured on a curve tracer.



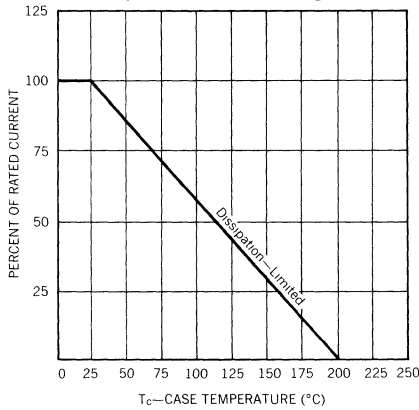
Typical Thermal-Response Characteristics (Normalized)



Maximum Operating Areas (T_c = 25°C)



Dissipation and I_s/β Derating Curves



POWER TRANSISTORS

10A, 400V NPN Mesa

2N6674
2N6675

FEATURES

- Collector Emitter Voltage: up to 650V
 - Peak Collector Current: 20A
 - Storage Time $\leq 2.5\mu\text{s}$
 - Fall Time $\leq 0.5\mu\text{s}$
- } at $I_c = 10\text{A}$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

ABSOLUTE MAXIMUM RATINGS*

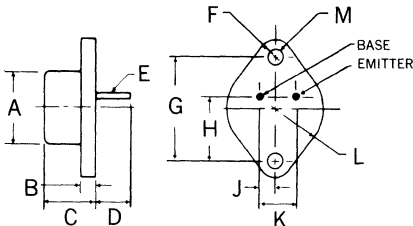
	2N6674	2N6675
Collector Emitter Voltage, V_{CEV}	450V	650V
Collector Emitter Voltage, V_{CEX}	350V	450V
Collector Emitter Voltage, $V_{CEO(sus)}$	300V	400V
Emitter Base Voltage, V_{EBO}	7V	
Collector Current, I_c continuous	15A	
Collector Current, $I_{cM(peak)}$	20A	
Base Current, I_b continuous	5A	
Power Dissipation, up to 25°C	175W	
above 25°C, derate linearly1W/°C	
Operating and Storage Temperature Range	-65°C to +200°C	

*JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

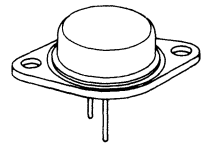
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



2N6674 2N6675

	INCHES	MILLIMETERS
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-043 DIA	6.35-11.43
D	312 MIN.	7.92 MIN.
E	038-043 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD.
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)



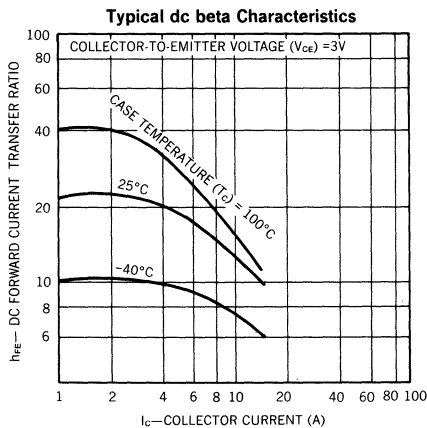
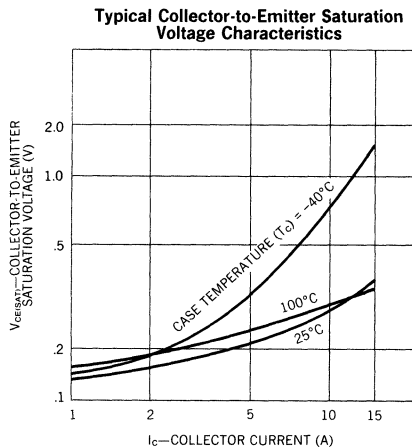
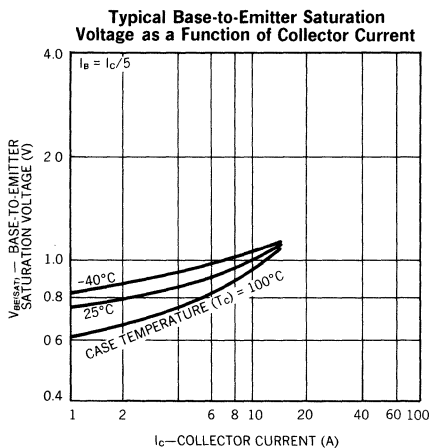
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

TEST	SYMBOL	2N6674		2N6675		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
Collector Cutoff Current	I_{CEV}	—	0.1	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	0.1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Collector Cutoff Current $T_C = 100^\circ C$	I_{CEV}	—	1	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Emitter Base Cutoff Current	I_{EBO}	—	2	—	2	mA	$V_{BE} = -7V, I_C = 0$
Collector Emitter Sustaining Voltage (Notes 1 & 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.2A, I_B = 0$
DC Current Gain (Note 1)	h_{FE}	8	20	8	20		$I_C = 10A, V_{CE} = 2V$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	—	1.5	V	$I_C = 10A, V_{CE} = 2A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1	—	1	V	$I_C = 10A, I_B = 2A$
Collector Saturation Voltage $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2	—	2	V	$I_C = 10A, I_B = 2A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5	—	5	V	$I_C = 15A, I_B = 5A$
Collector Emitter Voltage (Note 2)	V_{CEX}	350	—	450	—	V	$L = 50\mu H, R_{BB} = 2\Omega$ $V_{BE} = -4V, V_{CE}$ is clamped $I_C = 10A, I_B = 2A$
AC Current Gain	$ h_{fe} $	3	10	3	10		$I_C = 1A$ $V_{CE} = 10V$ $f = 5MHz$
Gain-Bandwidth Product	f_T	15	50	15	50	MHz	$V_{CE} = 10V, I_C = 1A$
Output Capacitance Common Base	C_{obo}	150	500	150	500	pF	$V_{CB} = 10A, f = 0.1MHz$
Switching Speeds							
Delay Time	t_d	—	0.1	—	0.1	μs	$I_C = 10A, I_B = 2A$ $V_{CC} = 125V, V_{BE} = -6V$ $t_p = 20\mu s$
Rise Time	t_r	—	0.6	—	0.6		
Storage Time	t_s	—	2.5	—	2.5	μs	$I_C = 10A, -I_B = 2A$ $V_{CC} = 125V, V_{BE} = -6V$ $t_p = 20\mu s$
Fall Time	t_f	—	0.5	—	0.5		
Crossover Time	t_c	—	0.5	—	0.5	μs	$I_C = 10A, I_{B2} = 2A$ $V_{CC} = 135V, V_{BE} = -6V$ $L_C = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Switching Speeds $T_C = 100^\circ C$							
Rise Time	t_r	—	1	—	1	μs	$I_C = 10A, I_B = 2A$ $V_{CC} = 125V, V_{BE} = -6V$ $t_p = 20\mu s$
Storage Time	t_s	—	4	—	4	μs	$I_C = 10A, -I_B = 2A$ $V_{CC} = 125V, V_{BE} = -6V$ $t_p = 20\mu s$
Fall Time	t_f	—	1	—	1		
Crossover Time	t_c	—	0.8	—	0.8	μs	$I_C = 10A, I_{B2} = 2A$ $V_{CC} = 135V, V_{BE} = -6V$ $L = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	1	—	1	$^\circ C/W$	

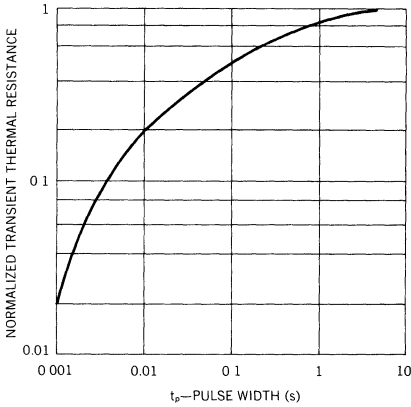
*JEDEC registered values

Notes: 1. Pulse duration = 300 μs ; duty factor $\leq 2\%$ 2. CAUTION: The sustaining voltage $V_{CEO(sus)}$ and V_{CEX} must not be measured on a curve tracer.

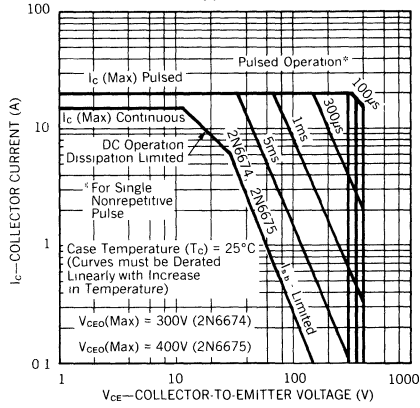
4



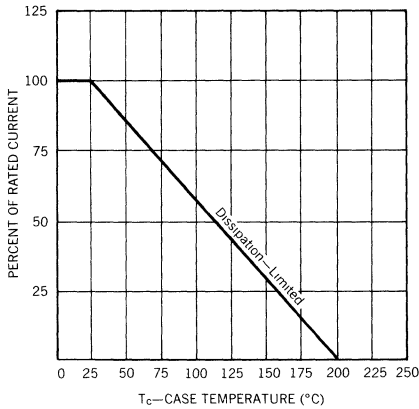
Typical Thermal-Response Characteristics (Normalized)



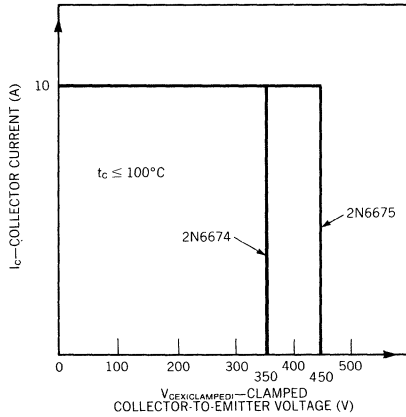
Maximum Operating Areas For All Types (T_c = 25°C)



Dissipation and I_s/β Derating Curves



Maximum Operating Conditions for Switching Between Saturation and Cutoff



POWER TRANSISTORS

15A, 400V NPN Mesa

2N6676
2N6677
2N6678

FEATURES

- Collector Emitter Voltage: up to 650V
 - Peak Collector Current: 20A
 - Storage Time $\leq 2.5\mu\text{s}$
 - Fall Time $\leq 0.5\mu\text{s}$
- } at $I_C = 15\text{A}$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

ABSOLUTE MAXIMUM RATINGS*

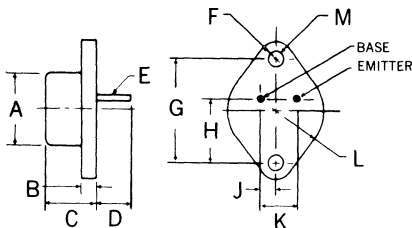
	2N6676	2N6677	2N6678
Collector Emitter Voltage, V_{CEV}	450V	550V	650V
Collector Emitter Voltage, V_{CEX}	350V	400V	450V
Collector Emitter Voltage, $V_{CEO(sus)}$	300V	350V	400V
Emitter Base Voltage, V_{EBO}	8V		
Collector Current, I_C continuous	15A		
Collector Current, $I_{CM(peak)}$	20A		
Base Current, I_B continuous	5A		
Power Dissipation, up to 25°C	175W		
above 25°C, derate linearly	1W/°C		
Operating and Storage Temperature Range	-65°C to +200°C		

*JEDEC registered values.

MECHANICAL SPECIFICATIONS

NOTE:

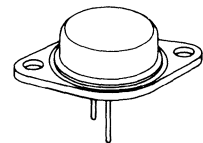
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



2N6676 2N6677 2N6678

	INCHES	MILLIMETERS
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250- .043 DIA	6.35-11.43
D	312 MIN	7.92 MIN.
E	.038- .043 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD.
G	1.177-1.197	29.90-30.40
H	655- 675	16.64- 17.15
J	205- 225	5.21- 5.72
K	420- 440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151- 161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)

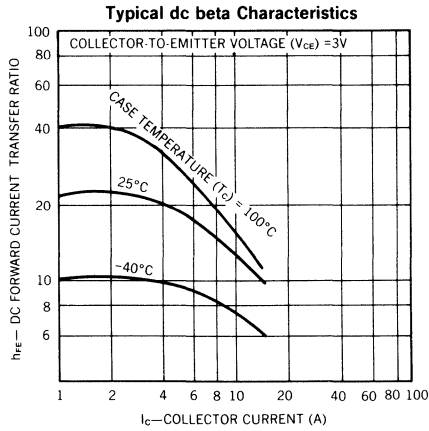
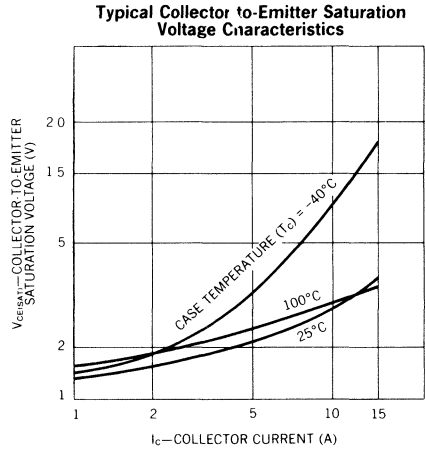
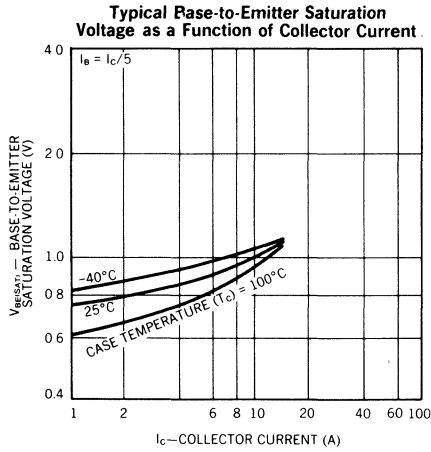


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

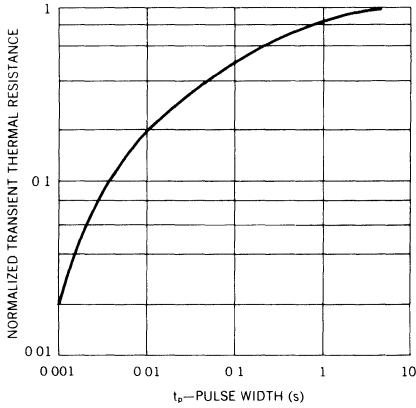
TEST	SYMBOL	2N6676		2N6677		2N6678		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Collector Cutoff Current	I_{CEV}	—	0.1	—	—	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	0.1	—	—	mA	$V_{CE} = 550V, V_{BE} = -1.5V$
		—	—	—	—	—	0.1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Collector Cutoff Current $T_c = 100^\circ C$	I_{CEV}	—	1	—	—	—	—	mA	$V_{CE} = 450V, V_{BE} = -1.5V$
		—	—	—	1	—	—	mA	$V_{CE} = 550V, V_{BE} = -1.5V$
		—	—	—	—	—	1	mA	$V_{CE} = 650V, V_{BE} = -1.5V$
Emitter Base Cutoff Current	I_{EBO}	—	2	—	2	—	2	mA	$V_{BE} = -8V, I_C = 0$
Collector Emitter Sustaining Voltage (Notes 1 & 2)	$V_{CE(iss)}$	300	—	350	—	400	—	V	$I_C = 0.2A, I_B = 0$
DC Current Gain (Note 1)	h_{FE}	8	—	8	—	8	—		$I_C = 15A, V_{CE} = 3V$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	—	1.5	—	1.5	V	$I_C = 15A, I_B = 3A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1	—	1	—	1	V	$I_C = 15A, I_B = 3A$
Collector Saturation Voltage $T_c = 100^\circ C$	$V_{CE(sat)}$	—	2	—	2	—	2	V	$I_C = 15A, I_B = 3A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	—	1.5	V	$I_C = 15A, I_B = 3A$
Collector Emitter Voltage (Note 2)	V_{CEX}	350	—	400	—	450	—	V	$L = 50\mu H, R_{BB} = 2\Omega$ $V_{BE} = -6V, V_{CE}$ is clamped $I_C = 15A, I_B = 3A$
AC Current Gain	$ h_{fe} $	3	10	3	10	3	10		$I_C = 1A$ $V_{CE} = 10V$ $f = 5MHz$
Gain-Bandwidth Product	f_T	15	50	15	50	15	50	MHz	$V_{CE} = 10V, I_C = 1A$
Output Capacitance Common Base	C_{obo}	150	500	150	500	150	500	pF	$V_{CB} = 10V, f = 0.1MHz$
Switching Speeds									
Delay Time	t_d	—	0.1	—	0.1	—	0.1	μs	$I_C = 15A, I_B = 3A$ $V_{CC} = 200V, -V_{BE} = -6V$ $t_p = 20\mu s$
Rise Time	t_r	—	0.6	—	0.6	—	0.6		
Storage Time	t_s	—	2.5	—	2.5	—	2.5	μs	$I_C = 15A, -I_{B2} = 3A$ $V_{CC} = 200V, -V_{BE} = -6V$ $t_p = 20\mu s$
Fall Time	t_f	—	0.5	—	0.5	—	0.5		
Crossover Time	t_c	—	0.5	—	0.5	—	0.5	μs	$I_C = 15A, I_B = 3A$ $V_{CC} = 200V, V_{BE} = -6V$ $L = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Switching Speeds $T_c = 100^\circ C$									
Rise Time	t_r	—	1	—	1	—	1	μs	$I_C = 15A, I_B = 3A$ $V_{CC} = 200V, V_{BE} = -6V$ $L = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Storage Time	t_s	—	4	—	4	—	4	μs	$I_C = 15A, -I_{B2} = 3A$ $V_{CC} = 200V, V_{BE} = -6V$ $L = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Fall Time	t_f	—	1	—	1	—	1		
Crossover Time	t_c	—	0.8	—	0.8	—	0.8	μs	$I_C = 15A, I_B = 3A$ $V_{CC} = 200V, V_{BE} = -6V$ $L = 50\mu H, R_C \leq 13.5\Omega$ Collector clamped to V_{CEX}
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	1	—	1	—	1	$^\circ C/W$	

*JEDEC registered values.

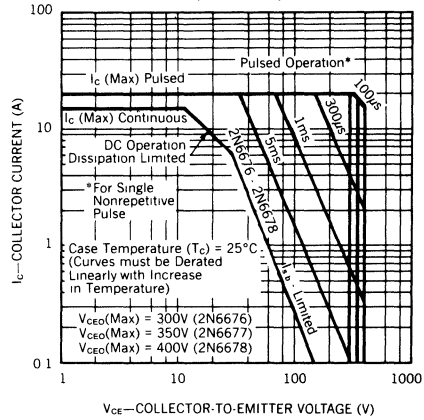
Notes: 1. Pulse duration = 300 μs ; duty factor $\leq 2\%$ 2. CAUTION: The sustaining voltage $V_{CE(iss)}$ and V_{CEX} must not be measured on a curve tracer.



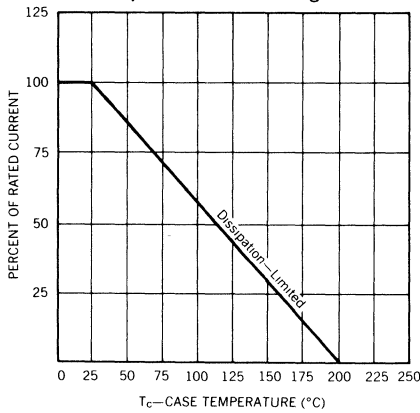
Typical Thermal-Response Characteristics (Normalized)



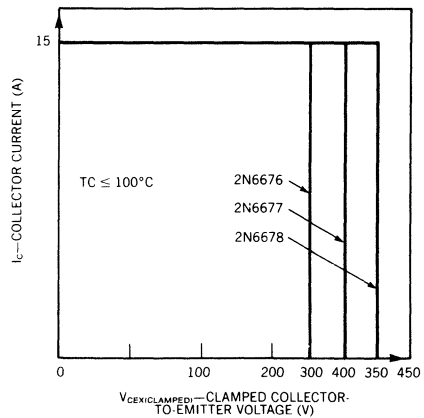
Maximum Operating Areas (T_c = 25°C)



Dissipation and I_{s/2} Derating Curves



Maximum Operating Conditions For Switching Between Saturation and Cutoff



POWER TRANSISTORS

15A, 400V NPN Mesa

JAN, JANTX, & JANTXV 2N6676
 JAN, JANTX, & JANTXV 2N6678

FEATURES

- Collector Emitter Voltage: up to 650V
 - Peak Collector Current: 20A
 - Storage Time $\leq 2.5\mu\text{s}$
 - Fall Time $\leq 0.5\mu\text{s}$
- } at $I_c = 15\text{A}$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

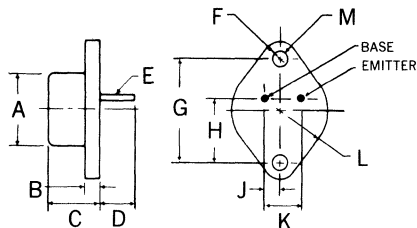
ABSOLUTE MAXIMUM RATINGS*

	2N6676	2N6678
Collector Base Voltage, V_{CBO}	450V	650V
Collector Emitter Voltage, V_{CEX}	450V	650V
Collector Emitter Voltage, $V_{CEO(sus)}$	300V	400V
Emitter Base Voltage, V_{EBO}	.8V	
Collector Current, I_C continuous	15A	
Collector Current, $I_{CM(peak)}$	20A	
Base Current, I_B continuous	.5A	
Power Dissipation, up to 25°C	1.75W	
Power Dissipation, above 25°C, derate linearly	.1W/°C	
Operating and Storage Temperature Range	-65°C to +200°C	

MECHANICAL SPECIFICATIONS

NOTE:

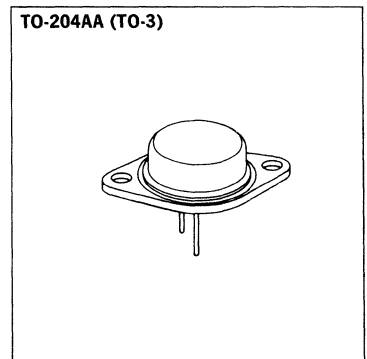
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



JAN, JANTX, & JANTXV 2N6676 JAN, JANTX, & JANTXV 2N6678

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	1.35 MAX.	3.43 MAX.
C	.250-.043 DIA.	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)*

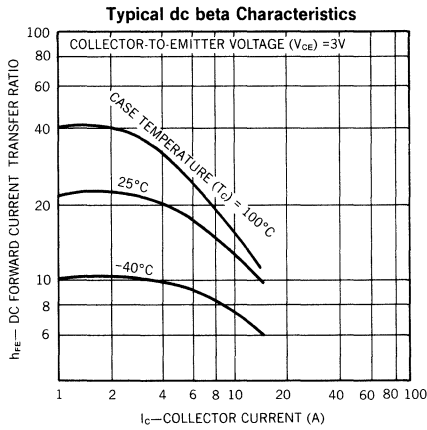
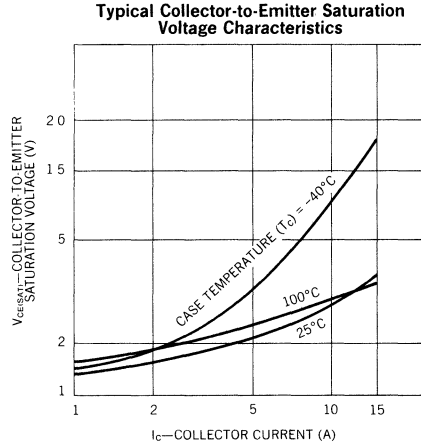
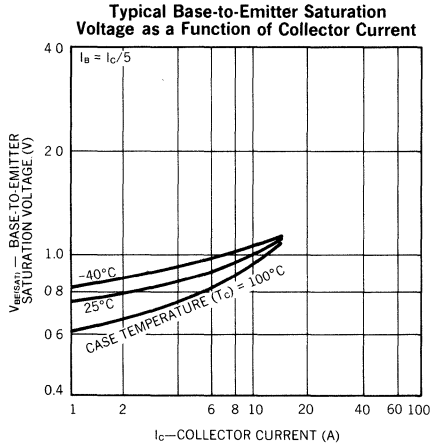
TEST	SYMBOL	2N6676		2N6678		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
Collector Cutoff Current	I _{CEX}	—	0.1	—	—	mA	V _{CE} = 450V, V _{BE} = -1.5V
		—	—	—	0.1	mA	V _{CE} = 650V, V _{BE} = -1.5V
Collector Cutoff Current T _C = 125°C	I _{CEX}	—	1	—	—	mA	V _{CE} = 450V, V _{BE} = -1.5V
		—	—	—	1	mA	V _{CE} = 650V, V _{BE} = -1.5V
Emitter Base Cutoff Current	I _{EBO}	—	2	—	2	mA	V _{BE} = -8V, I _C = 0V
Collector Emitter Sustaining Voltage (Notes 1 & 2)	V _{CEO(sus)}	300	—	400	—	V	I _C = 0.2A, I _B = 0V
DC Current Gain (Note 1)	h _{FE}	15	40	15	40		I _C = 1.0A, V _{CE} = 3V
DC Current Gain (Note 1)	h _{FE}	8	20	8	20		I _C = 15A, V _{CE} = 3V
Base Saturation Voltage (Note 1)	V _{BE(sat)}	—	1.5	—	1.5	V	I _C = 15A, I _B = 3A
Collector Saturation Voltage (Note 1)	V _{CE(sat)}	—	1	—	1	V	I _C = 15A, I _B = 3A
Collector Saturation Voltage T _C = 125°C	V _{CE(sat)}	—	2	—	2	V	I _C = 15A, I _B = 3A
Collector Saturation Voltage (Note 1)	V _{CE(sat)}	—	1.5	—	1.5	V	I _C = 15A, I _B = 3A
AC Current Gain	h _{fe}	3	10	3	10		I _C = 1A V _{CE} = 10V f = 5MHz
Gain-Bandwidth Product	f _T	15	50	15	50	MHz	V _{CE} = 10V, I _C = 1A
Output Capacitance Common Base	C _{obo}	150	500	150	500	pF	V _{CB} = 10V, f = 0.1MHz
Switching Speeds Delay Time	t _d	—	0.1	—	0.1	μs	I _C = 15A, I _B = 3A V _{CC} = 200V, -V _{BE} = -6V t _p = 20μs
Rise Time	t _r	—	0.6	—	0.6		
Storage Time	t _s	—	2.5	—	2.5	μs	I _C = 15A, -I _{B2} = 3A V _{CC} = 200V, -V _{BE} = -6V t _p = 20μs
Fall Time	t _f	—	0.5	—	0.5		
Crossover Time	t _c	—	0.5	—	0.5	μs	I _C = 15A, I _B = 3A V _{CC} = 200V, V _{BE} = -6V L = 50μH, R _C ≤ 13.5Ω Collector clamped to V _{CEX}
Switching Speeds, T _A = 125°C Delay Time	t _d	—	0.1	—	0.1	μs	I _C = 15A, I _B = 3A V _{CC} = 200V, V _{BE} = -6V L = 50μH, R _C ≤ 13.5Ω Collector clamped to V _{CEX}
Rise Time	t _r	—	1	—	1		
Storage Time	t _s	—	4	—	4	μs	I _C = 15A, -I _{B2} = 3A V _{CC} = 200V, V _{BE} = -6V L = 50μH, R _C ≤ 13.5Ω Collector clamped to V _{CEX}
Fall Time	t _f	—	1	—	1		
Crossover Time	t _c	—	0.8	—	0.8	μs	I _C = 15A, I _B = 3A V _{CC} = 200V, V _{BE} = -6V L = 50μH, R _C ≤ 13.5Ω Collector clamped to V _{CEX}
Thermal Resistance, Junction to Case	R _{θJC}	—	1	—	1	°C/W	

*JEDEC registered values.

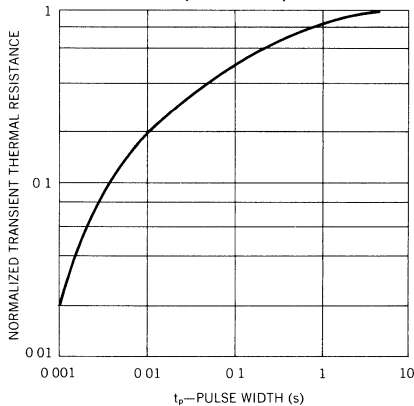
Notes: 1. Pulse duration = 300μs; duty factor ≤ 2%

2. CAUTION: The sustaining voltage V_{CEO(sus)} and V_{CEX} must not be measured on a curve tracer.

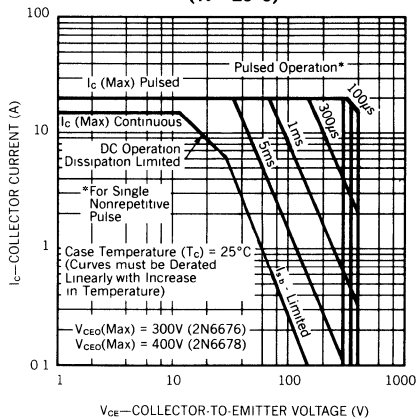
4



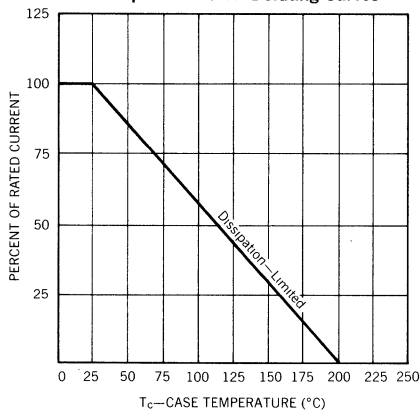
Typical Thermal-Response Characteristics (Normalized)



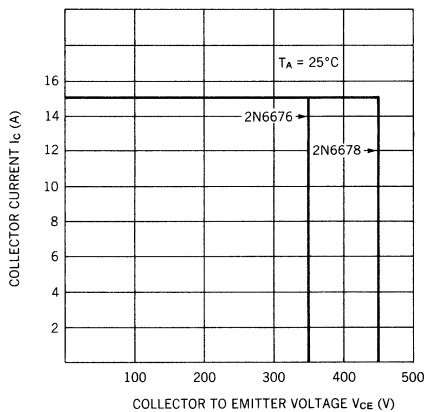
Maximum Operating Areas (T_c = 25°C)



Dissipation and I_s Derating Curves



Safe Operating Area For Switching Between Saturation And Cutoff (Clamped Inductive Load)



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

2N6755
J, JTX, JTXV 2N6756

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/542A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

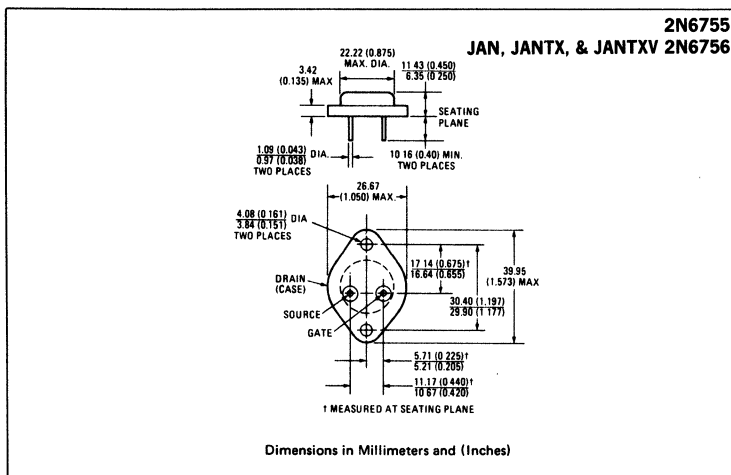
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

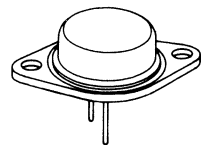
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6755	60V	0.25 Ω	12A
2N6756	100V	0.18 Ω	14A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6755	2N6756	Units
V _{DS} Drain - Source Voltage	60*	100*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ)	60*	100*	V
I _D @ T _C = 25°C Continuous Drain Current	12*	14*	A
I _D @ T _C = 100°C Continuous Drain Current	8.0*	9.0*	A
I _{DM} Pulsed Drain Current	25	30	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	75* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	30* (See Fig. 11)		W
Linear Derating Factor	0.6* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 25 30		A
T _J Operating and Storage Temperature Range	-55* to 150*		°C
T _{stg} Lead Temperature	300* (0.063 in (1.6mm) from case for 10s)		°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	2N6755	60	-	-	V	V _{GS} = 0
	2N6756	100	-	-	V	I _D = 1.0 mA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	-	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate - Body Leakage Forward	ALL	-	-	100*	nA	V _{GS} = 20V
I _{GSSR} Gate - Body Leakage Reverse	ALL	-	-	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	-	0.1	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0
		-	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6755	-	-	3.0*	V	V _{GS} = 10V, I _D = 12A
	2N6756	-	-	2.52*	V	V _{GS} = 10V, I _D = 14A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6755	-	0.20	0.25*	Ω	V _{GS} = 10V, I _D = 8A
	2N6756	-	0.14	0.18*	Ω	V _{GS} = 10V, I _D = 9A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6755	-	-	0.45*	Ω	V _{GS} = 10V, I _D = 8A, T _C = 125°C
	2N6756	-	-	0.33*	Ω	V _{GS} = 10V, I _D = 9A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (Ω)	V _{DS} = 15V, I _D = 9A
C _{iss} Input Capacitance	ALL	350*	600	800*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	150*	300	500*	pF	
C _{rss} Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
t _{d(on)} Turn-On Delay Time	ALL	-	-	30*	ns	V _{DD} ≥ 36V, I _D = 9A, Z _o = 15Ω
t _r Rise Time	ALL	-	-	75*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	-	-	40*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	-	-	45*	ns	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	-	-	1.67*	K/W	
R _{thCS} Case-to-Sink	ALL	-	0.1	-	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	-	-	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6755	-	-	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6756	-	-	14*	A	
I _{SM} Pulsed Source Current (Body Diode)	2N6755	-	-	25	A	
	2N6756	-	-	30	A	
V _{SD} Diode Forward Voltage ①	2N6755	0.85*	-	1.7*	V	T _C = 25°C, I _S = 12A, V _{GS} = 0
	2N6756	0.90*	-	1.8*	V	T _C = 25°C, I _S = 14A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	-	300	-	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	-	4.0	-	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values ① Pulse Test Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 - Clamped Inductive Test Circuit

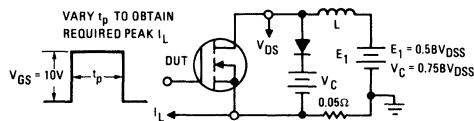


Fig. 2 - Clamped Inductive Waveforms

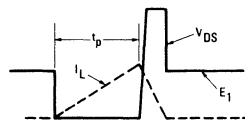


Fig. 3 — Typical Output Characteristics

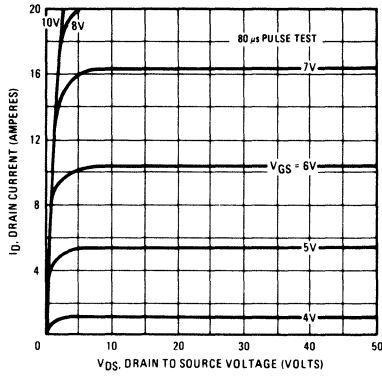


Fig. 4 — Typical Transfer Characteristics

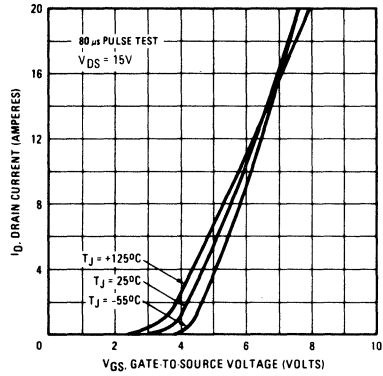


Fig. 5 — Typical Saturation Characteristics (2N6755)

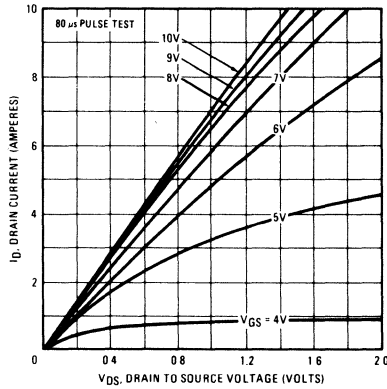


Fig. 6 — Typical Saturation Characteristics (2N6756)

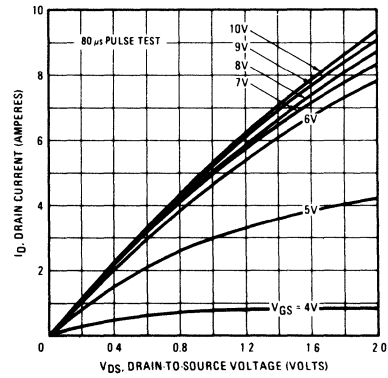


Fig. 7 — Typical Transconductance Vs. Drain Current

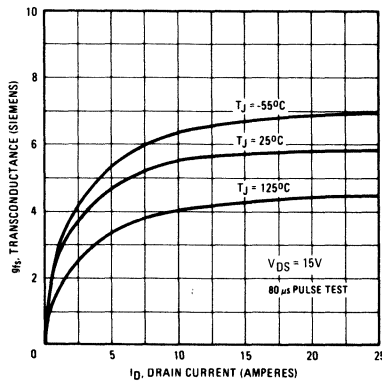


Fig. 8 — Maximum Safe Operating Area

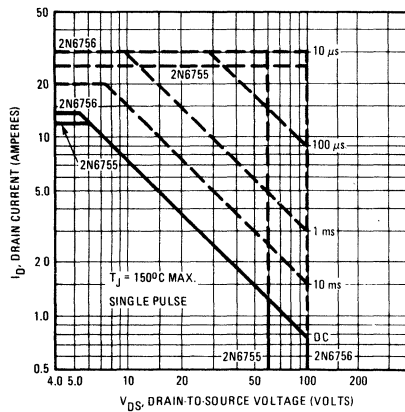


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

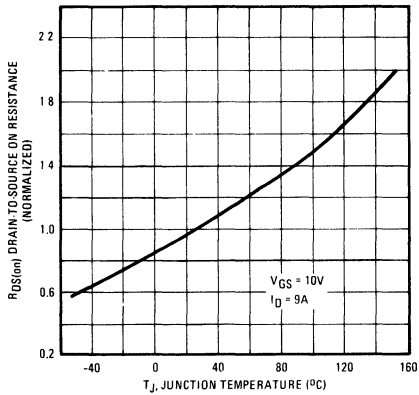


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

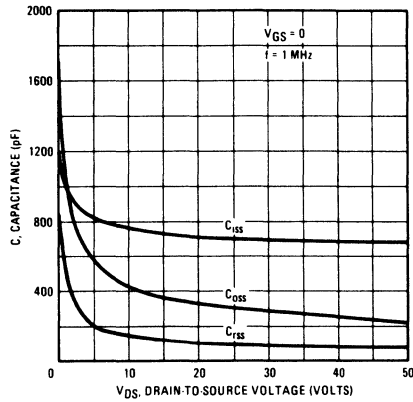


Fig. 11 – Power Vs. Temperature Derating Curve

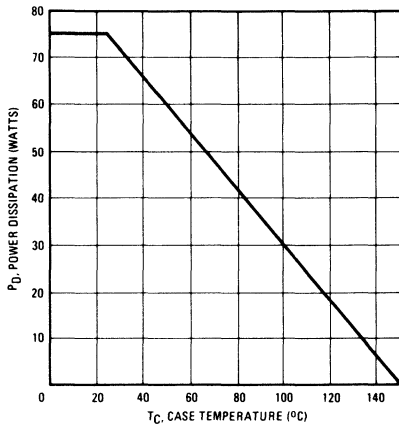


Fig. 12 – Typical Body-Drain Diode Forward Voltage

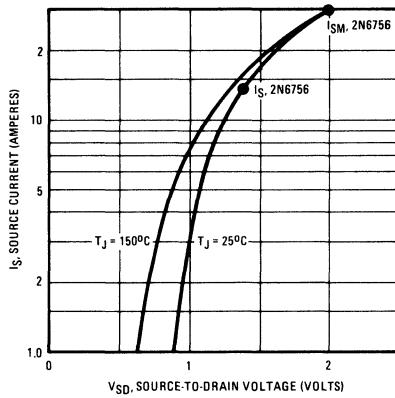


Fig. 13 – Switching Time Test Circuit

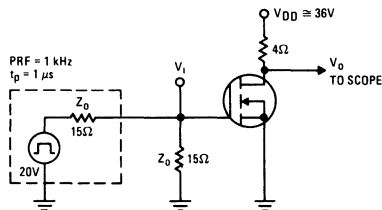
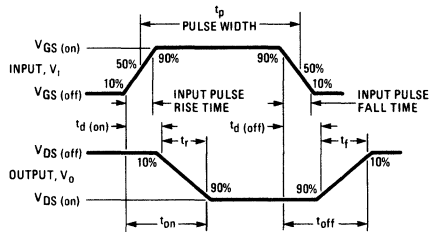


Fig. 14 – Switching Time Waveforms



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm N-Channel

2N6757
J, JTX, JTXV 2N6758

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/542A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

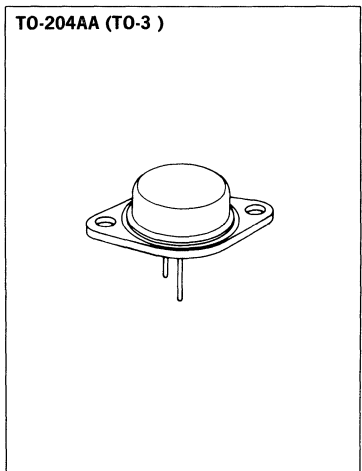
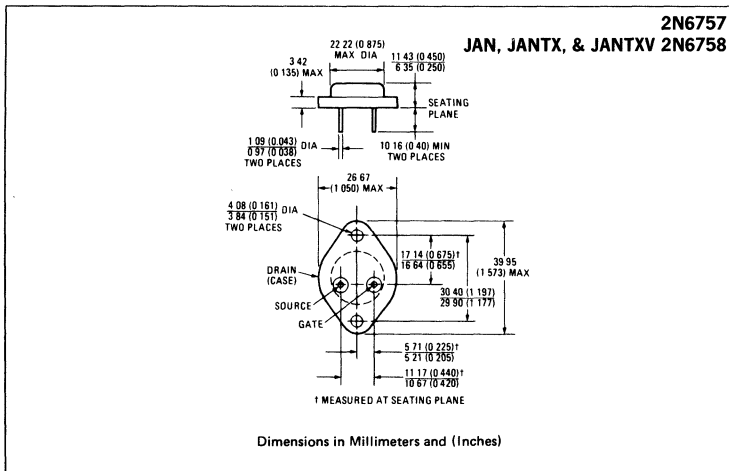
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6757	150V	0.6Ω	8A
2N6758	200V	0.4Ω	9A

MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter		2N6757	2N6758	Units
V _{DS}	Drain – Source Voltage	150*	200*	V
V _{DGR}	Drain – Gate Voltage (R _{GS} = 1 MΩ)	150*	200*	V
I _D @ T _C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I _D @ T _C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I _{DM}	Pulsed Drain Current	12	15	A
V _{GS}	Gate – Source Voltage	±20*		V
P _D @ T _C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P _D @ T _C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I _{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
T _J	Operating and Storage Temperature Range	-55* to 150*		°C
T _{stg}	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	V _{GS} = 0
		2N6758	200	–	–	V	I _D = 1.0 mA
V _{GS(th)}	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V _{GS} = 20V
I _{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0
			–	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 125°C
V _{DS(on)}	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.8*	V	V _{GS} = 10V, I _D = 8A
		2N6758	–	–	3.6*	V	V _{GS} = 10V, I _D = 9A
R _{DS(on)}	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	V _{GS} = 10V, I _D = 5A
		2N6758	–	0.25	0.4*	Ω	V _{GS} = 10V, I _D = 6A
R _{DS(on)}	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	V _{GS} = 10V, I _D = 5A, T _C = 125°C
		2N6758	–	–	0.75*	Ω	V _{GS} = 10V, I _D = 6A, T _C = 125°C
g _{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (Ω)	V _{DS} = 15V, I _D = 6A
C _{iss}	Input Capacitance	ALL	350*	600	800*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C _{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
t _{d(on)}	Turn-On Delay Time	ALL	–	–	30*	ns	V _{DD} ≅ 90V, I _D = 6A, Z ₀ = 15Ω
t _r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
t _{d(off)}	Turn-Off Delay Time	ALL	–	–	50*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f	Fall Time	ALL	–	–	40*	ns	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R _{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R _{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I _{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V _{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	T _C = 25°C, I _S = 8A, V _{GS} = 0
		2N6758	0.80*	–	1.60*	V	T _C = 25°C, I _S = 9A, V _{GS} = 0
t _{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≦ 300 μsec, Duty Cycle ≦ 2%

Fig. 1 – Clamped Inductive Test Circuit

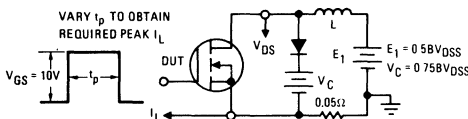


Fig. 2 – Clamped Inductive Waveforms



Fig. 3 – Typical Output Characteristics

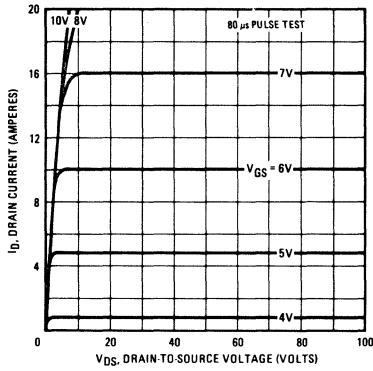


Fig. 4 – Typical Transfer Characteristics

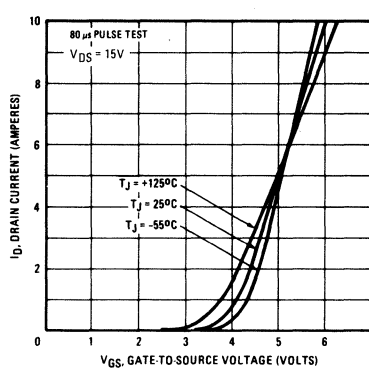


Fig. 5 – Typical Saturation Characteristics (2N6757)

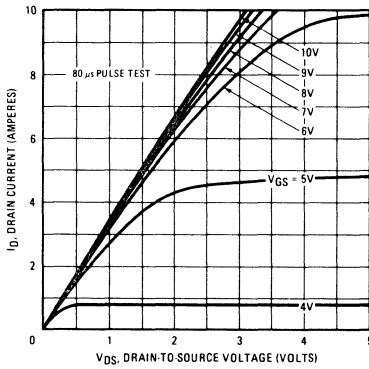


Fig. 6 – Typical Saturation Characteristics (2N6758)

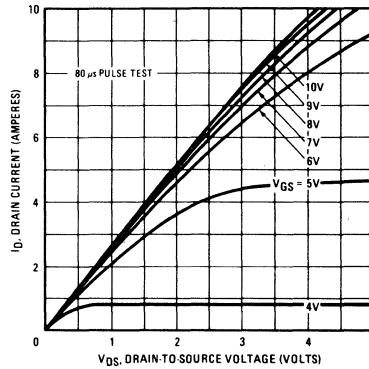


Fig. 7 – Typical Transconductance Vs. Drain Current

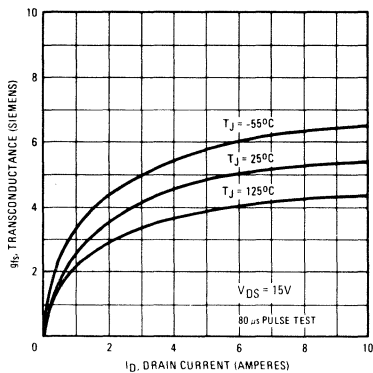


Fig. 8 – Maximum Safe Operating Area

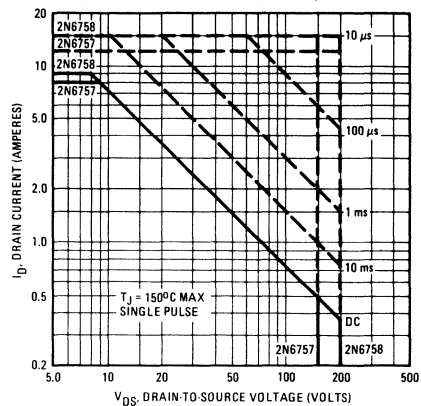


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

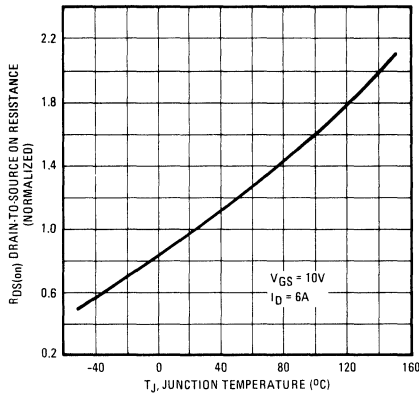


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

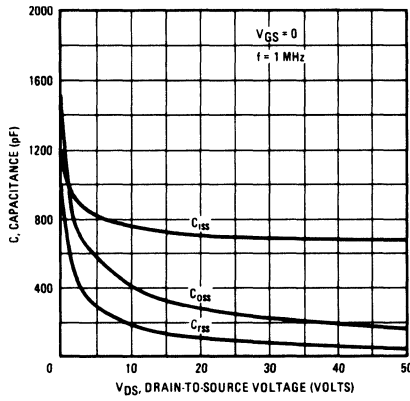


Fig. 11 — Power Vs. Temperature Derating Curve

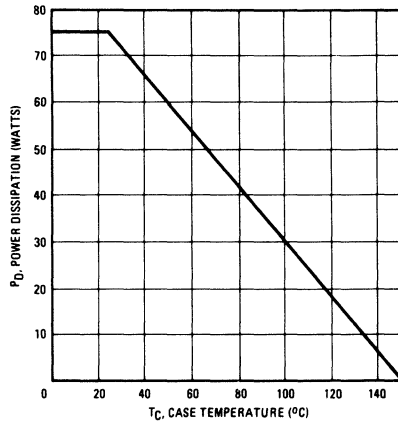


Fig. 12 — Typical Body-Drain Diode Forward Voltage

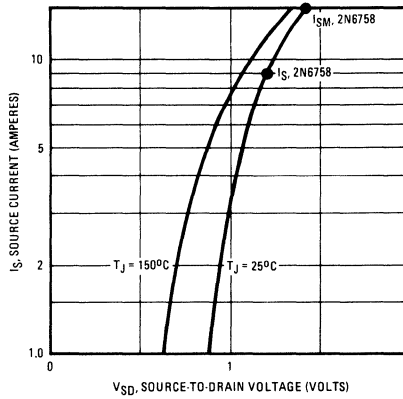


Fig. 13 — Switching Time Test Circuit

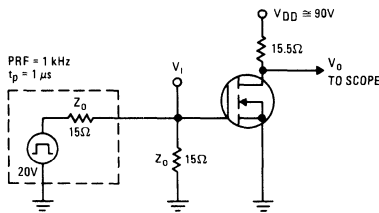
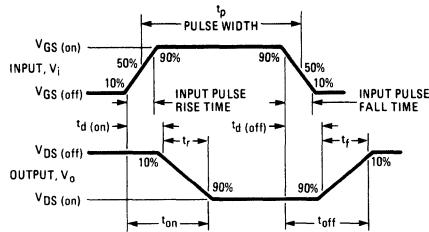


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm
N-Channel

J, JTX, JTXV 2N6759
2N6760

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/542A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

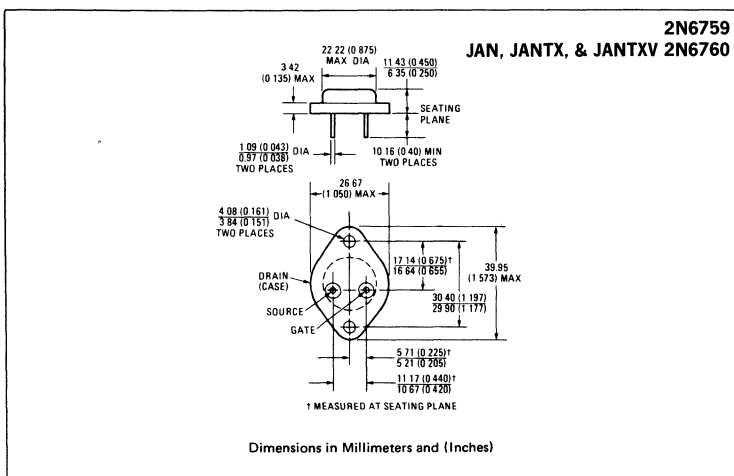
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

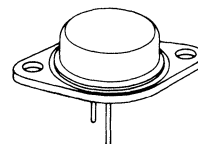
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6759	350V	1.5 Ω	4.5A
2N6760	400V	1.0 Ω	5.5A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS



Parameter	2N6759	2N6760	Units
V_{DS} Drain – Source Voltage	350*	400*	V
V_{DGR} Drain – Gate Voltage ($R_{GS} = 1\text{ M}\Omega$)	350*	400*	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	4.5*	5.5*	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	3.0*	3.5*	A
I_{DM} Pulsed Drain Current	7.0	8.0	A
V_{GS} Gate – Source Voltage	$\pm 20^*$		V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75* (See Fig. 11)		W
$P_D @ T_C = 100^\circ\text{C}$ Max. Power Dissipation	30* (See Fig. 11)		W
Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM} Inductive Current, Clamped	(See Fig. 1 and 2) $L = 100\text{ }\mu\text{H}$		A
T_J Operating and Storage Temperature Range	-55* to 150*		$^\circ\text{C}$
T_{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		$^\circ\text{C}$


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain – Source Breakdown Voltage	2N6759	350	–	–	V	$V_{GS} = 0$
	2N6760	400	–	–	V	$I_D = 1.0\text{ mA}$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$
I_{GSSF} Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20\text{V}$
I_{GSSR} Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0$
		–	0.2	4.0*	mA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0, T_C = 125^\circ\text{C}$
$V_{DS(on)}$ Static Drain-Source On-State Voltage (1)	2N6759	–	–	7.0*	V	$V_{GS} = 10\text{V}, I_D = 4.5\text{A}$
	2N6760	–	–	6.7*	V	$V_{GS} = 10\text{V}, I_D = 5.5\text{A}$
$R_{DS(on)}$ Static Drain-Source On-State Resistance (1)	2N6759	–	1.0	1.5*	Ω	$V_{GS} = 10\text{V}, I_D = 3\text{A}$
	2N6760	–	0.8	1.0*	Ω	$V_{GS} = 10\text{V}, I_D = 3.5\text{A}$
$R_{DS(on)}$ Static Drain-Source On-State Resistance (1)	2N6759	–	–	3.3*	Ω	$V_{GS} = 10\text{V}, I_D = 3\text{A}, T_C = 125^\circ\text{C}$
	2N6760	–	–	2.2*	Ω	$V_{GS} = 10\text{V}, I_D = 3.5\text{A}, T_C = 125^\circ\text{C}$
g_{fs} Forward Transconductance (1)	ALL	3.0*	4.5	9.0*	S (τ)	$V_{DS} = 15\text{V}, I_D = 3.5\text{A}$
C_{iss} Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	50*	150	300*	pF	
C_{rss} Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 175\text{V}, I_D = 3.5\text{A}, Z_o = 15\Omega$
t_r Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$ Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	–	–	35*	ns	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS} Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6760	–	–	5.5*	A	
I_{SM} Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
	2N6760	–	–	8.0	A	
V_{SD} Diode Forward Voltage (1)	2N6759	0.70*	–	1.4*	V	$T_C = 25^\circ\text{C}, I_S = 4.5\text{A}, V_{GS} = 0$
	2N6760	0.75*	–	1.5*	V	$T_C = 25^\circ\text{C}, I_S = 5.5\text{A}, V_{GS} = 0$
t_{rr} Reverse Recovery Time	ALL	–	550	–	ns	$T_J = 150^\circ\text{C}, I_F = I_{SM}, dI_F/dt = 100\text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	ALL	–	8.0	–	μC	$T_J = 150^\circ\text{C}, I_F = I_{SM}, dI_F/dt = 100\text{ A}/\mu\text{s}$

* JEDEC registered values. (1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$

Fig. 1 – Clamped Inductive Test Circuit

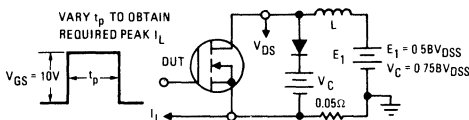


Fig. 2 – Clamped Inductive Waveforms



Fig. 3 – Typical Output Characteristics

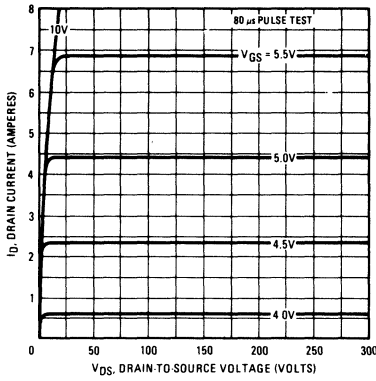


Fig. 5 – Typical Saturation Characteristics (2N6759)

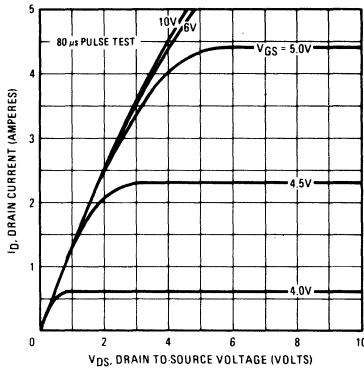


Fig. 4 – Typical Transfer Characteristics

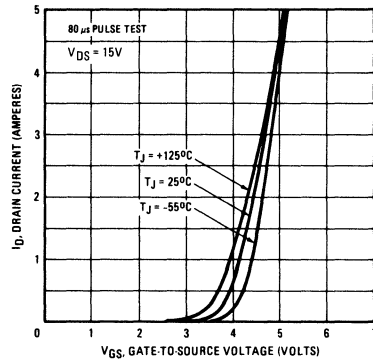


Fig. 6 – Typical Saturation Characteristics (2N6760)

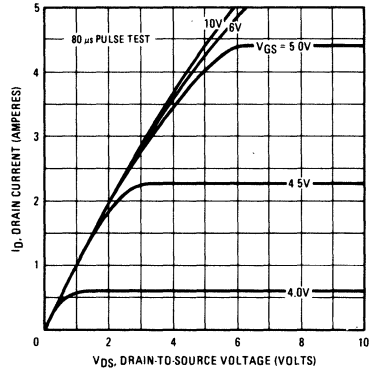


Fig. 7 – Typical Transconductance Vs. Drain Current

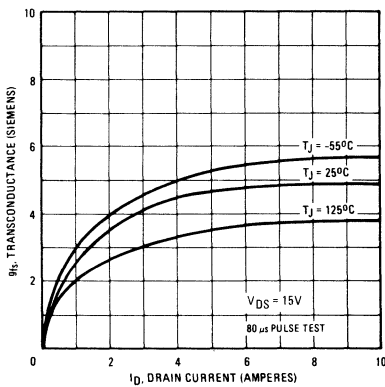


Fig. 8 – Maximum Safe Operating Area

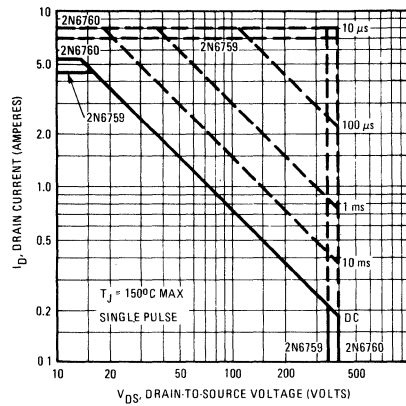


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

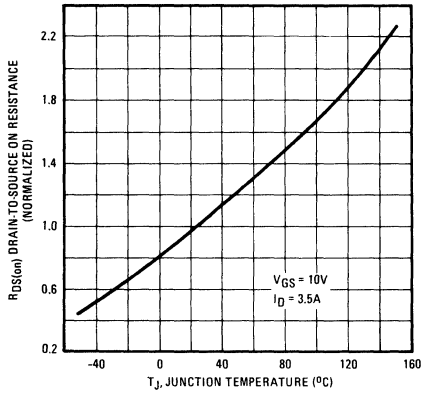


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

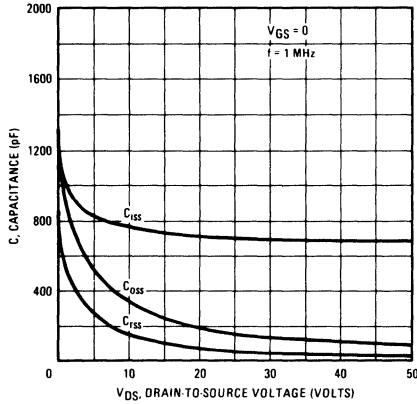


Fig. 11 — Power Vs. Temperature Derating Curve

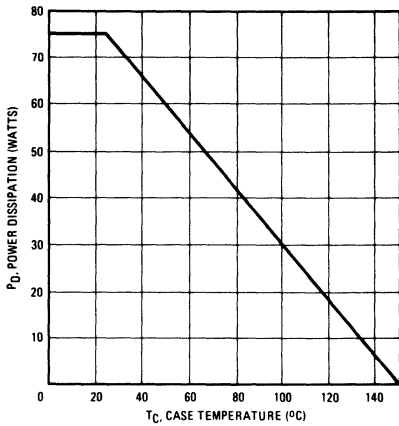


Fig. 12 — Typical Body-Drain Diode Forward Voltage

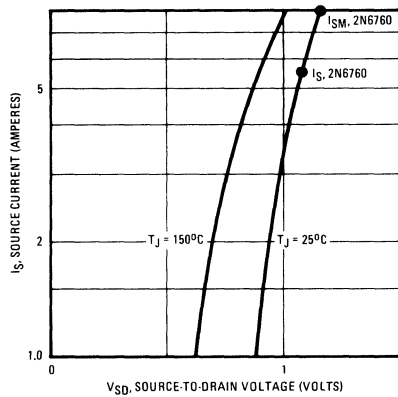


Fig. 13 — Switching Time Test Circuit

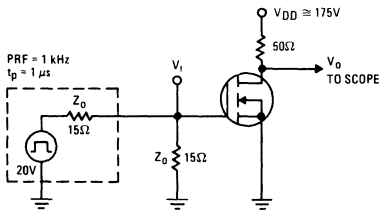
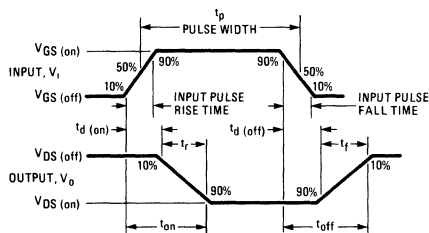


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

2N6761
J, JTX, JTXV 2N6762

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/542A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

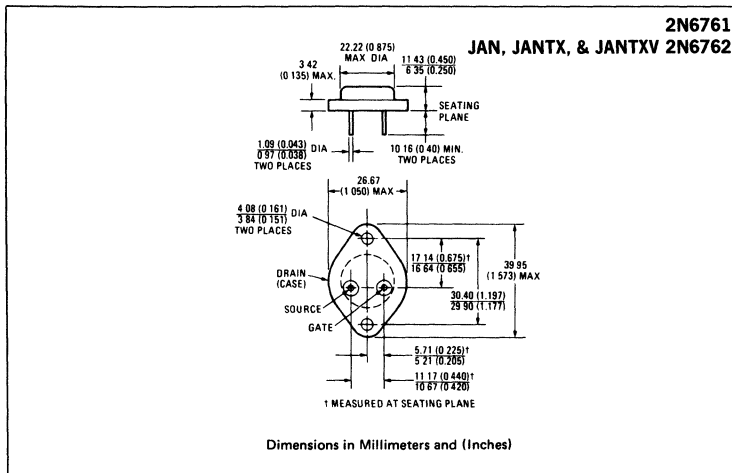
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

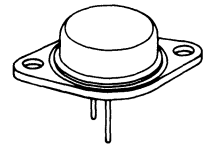
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6761	450V	2.0 Ω	4.0A
2N6762	500V	1.5 Ω	4.5A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6761	2N6762	Units
V _{DS} Drain – Source Voltage	450*	500*	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ)	450*	500*	V
I _D @ T _C = 25°C Continuous Drain Current	4.0*	4.5*	A
I _D @ T _C = 100°C Continuous Drain Current	2.5*	3.0*	A
I _{DM} Pulsed Drain Current	6.0	7.0	A
V _{GS} Gate – Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	75* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	30* (See Fig. 11)		W
Linear Derating Factor	0.6* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped (See Fig. 1 and 2) L = 100 μH	6.0	7.0	A
T _J Operating and Storage Temperature Range	-55° to 150°		°C
T _{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

4


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V _{GS} = 0 I _D = 4.0 mA
	2N6762	500	–	–	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate – Body Leakage Forward	ALL	–	–	100*	nA	V _{GS} = 20V
I _{GSSR} Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V _{DS} = 0.8 x Max. Rating, V _{GS} = 0
		–	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 25°C to 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V _{GS} = 10V, I _D = 4A
	2N6762	–	–	7.7*	V	V _{GS} = 10V, I _D = 4.5A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V _{GS} = 10V, I _D = 2.5A
	2N6762	–	1.3	1.5*	Ω	V _{GS} = 10V, I _D = 3.0A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V _{GS} = 10V, I _D = 2.5A, T _C = 125°C
	2N6762	–	–	3.3*	Ω	V _{GS} = 10V, I _D = 3.0A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (Ω)	V _{DS} = 16V, I _D = 3A
C _{iss} Input Capacitance	ALL	350*	600	800*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	25*	100	200*	pF	
C _{rss} Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
t _{d(on)} Turn-On Delay Time	ALL	–	–	30*	ns	V _{DD} ≅ 225V, I _D = 3A, Z _o = 15Ω
t _r Rise Time	ALL	–	–	30*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	–	–	30*	ns	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	–	–	1.67*	K/W	
R _{thCS} Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6762	–	–	4.5*	A	
I _{SM} Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
	2N6762	–	–	7.0	A	
V _{SD} Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	T _C = 25°C, I _S = 4A, V _{GS} = 0
	2N6762	0.7*	–	1.4*	V	T _C = 25°C, I _S = 4.5A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	–	500	–	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	–	7.0	–	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 – Clamped Inductive Test Circuit

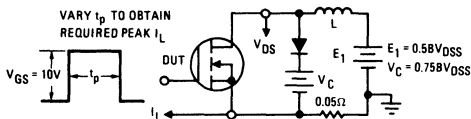


Fig. 2 – Clamped Inductive Waveforms



Fig. 3 – Typical Output Characteristics

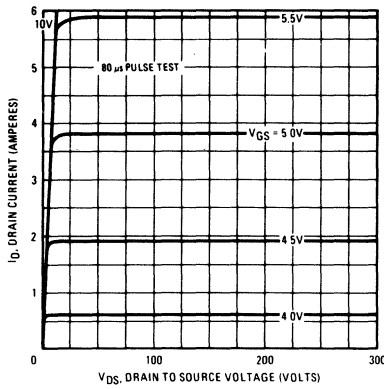


Fig. 4 – Typical Transfer Characteristics

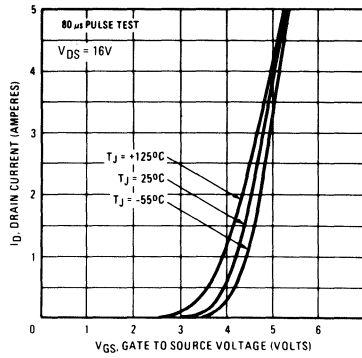


Fig. 5 – Typical Saturation Characteristics (2N6761)

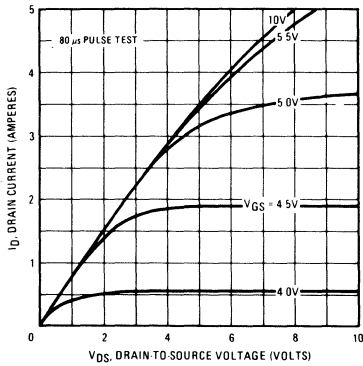


Fig. 6 – Typical Saturation Characteristics (2N6762)

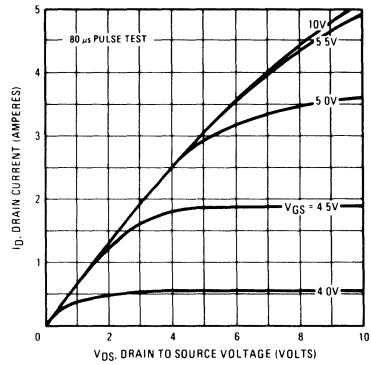


Fig. 7 – Typical Transconductance Vs. Drain Current

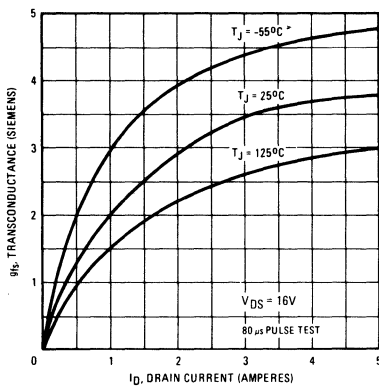


Fig. 8 – Maximum Safe Operating Area

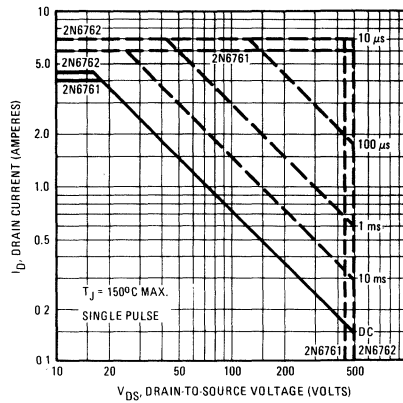


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

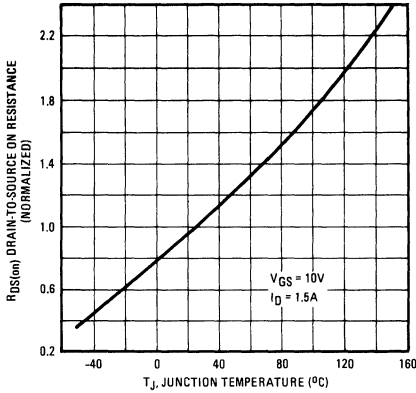


Fig. 10—Typical Capacitance Vs. Drain-to-Source Voltage

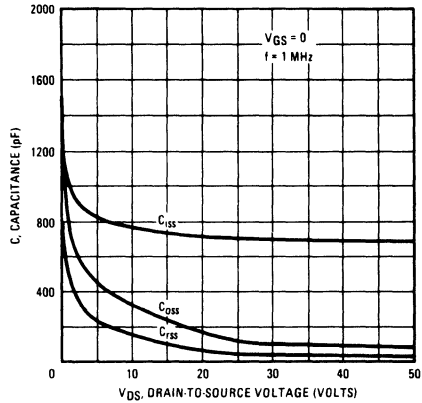


Fig. 11—Power Vs. Temperature Derating Curve

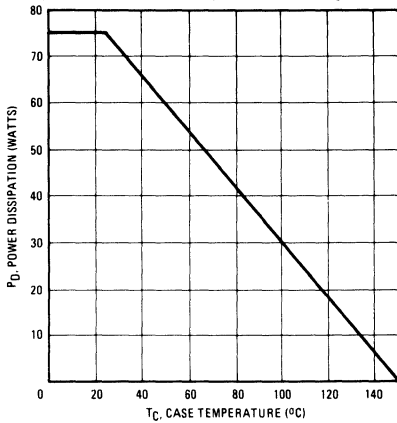


Fig. 12—Typical Body-Drain Diode Forward Voltage

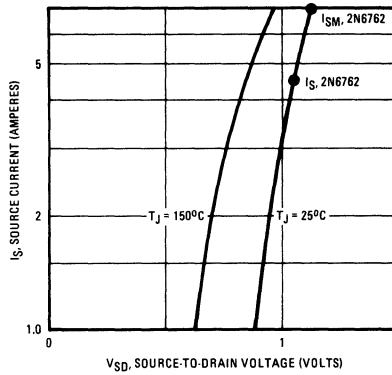


Fig. 13—Switching Time Test Circuit

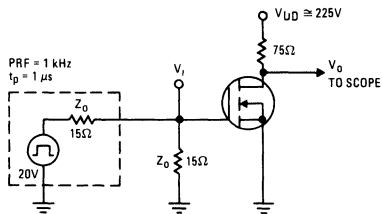
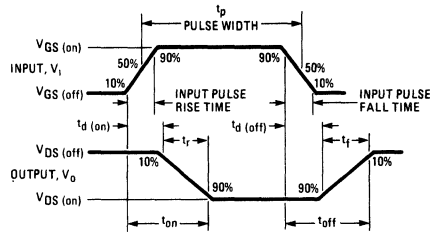


Fig. 14—Switching Time Waveforms



POWER MOSFET TRANSISTORS

100 Volt, 0.055 Ohm
N-Channel

2N6763
J, JTX, JTXV 2N6764

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/543A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

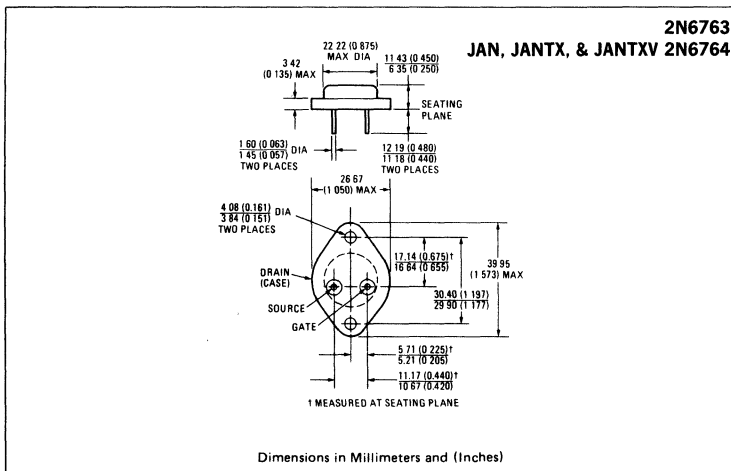
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

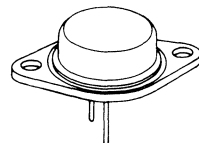
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6763	60V	0.08 Ω	31A
2N6764	100V	0.055 Ω	38A

MECHANICAL SPECIFICATIONS



TO-204AE (TO-3 modified)



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6763	2N6764	Units
V _{DS} Drain – Source Voltage	60*	100*	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ)	60*	100*	V
I _D @ T _C = 25°C Continuous Drain Current	31*	38*	A
I _D @ T _C = 100°C Continuous Drain Current	20*	24*	A
I _{DM} Pulsed Drain Current	60	70	A
V _{GS} Gate – Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	150* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	60* (See Fig. 11)		W
Linear Derating Factor	1.2* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60 70		A
T _J Operating and Storage Temperature Range	-55* to 150*		°C
T _{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C




ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V _{GS} = 0 I _D = 1.0 mA
	2N6764	100	–	–	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate – Body Leakage Forward	ALL	–	–	100*	nA	V _{GS} = 20V
I _{GSSR} Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0
		–	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6763	–	–	2.48*	V	V _{GS} = 10V, I _D = 31A
	2N6764	–	–	2.09*	V	V _{GS} = 10V, I _D = 38A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6763	–	0.06	0.08*	Ω	V _{GS} = 10V, I _D = 20A
	2N6764	–	0.045	0.055*	Ω	V _{GS} = 10V, I _D = 24A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6763	–	–	0.136*	Ω	V _{GS} = 10V, I _D = 20A, T _C = 125°C
	2N6764	–	–	0.094*	Ω	V _{GS} = 10V, I _D = 24A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	9.0*	12.5	27*	S (Ω)	V _{DS} = 15V, I _D = 24A
C _{iss} Input Capacitance	ALL	1000*	2000	3000*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	500*	1000	1500*	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
t _{d(on)} Turn-On Delay Time	ALL	–	–	35*	ns	V _{DD} ≅ 24V, I _D = 24A, Z _o = 4.7Ω
t _r Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	–	–	100*	ns	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	–	–	0.83*	K/W	
R _{thCS} Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	2N6764	–	–	38*		
I _{SM} Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
	2N6764	–	–	70		
V _{SD} Diode Forward Voltage ①	2N6763	0.90*	–	1.8*	V	T _C = 25°C, I _S = 31A, V _{GS} = 0
	2N6764	0.95*	–	1.9*	V	T _C = 25°C, I _S = 38A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	–	500	–	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	–	10	–	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 – Clamped Inductive Test Circuit

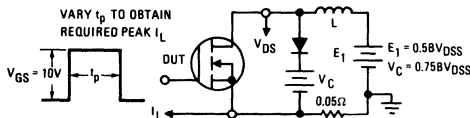


Fig. 2 – Clamped Inductive Waveforms

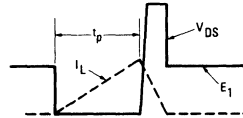


Fig. 3 – Typical Output Characteristics

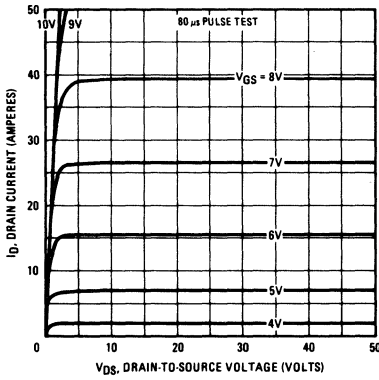


Fig. 4 – Typical Transfer Characteristics

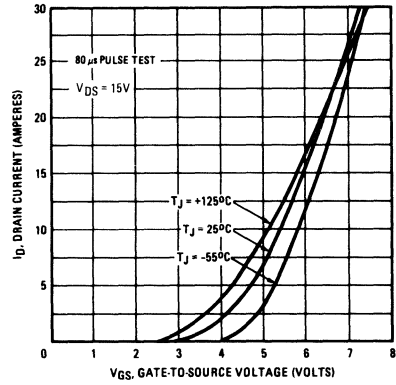


Fig. 5 – Typical Saturation Characteristics (2N6763)

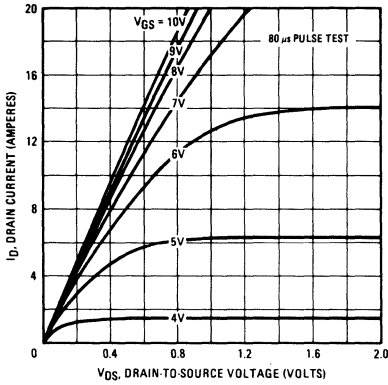


Fig. 6 – Typical Saturation Characteristics (2N6764)

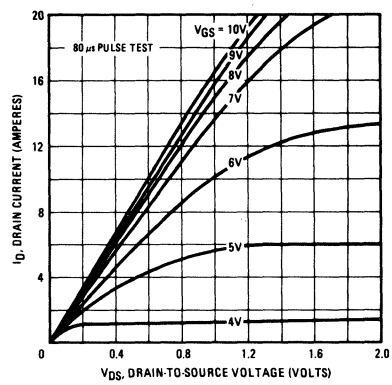


Fig. 7 – Typical Transconductance Vs. Drain Current

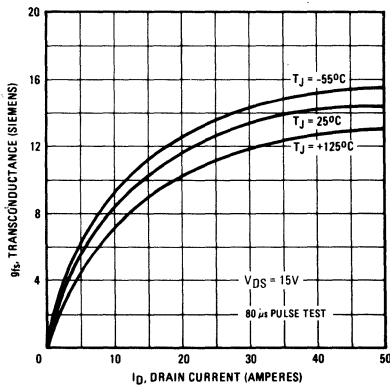


Fig. 8 – Maximum Safe Operating Area

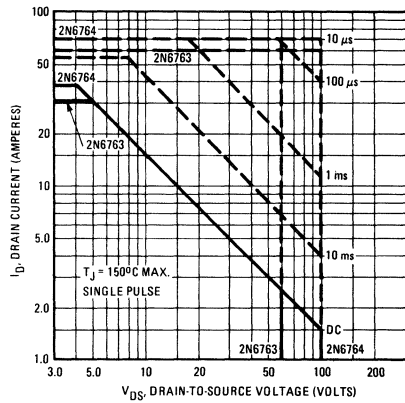


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

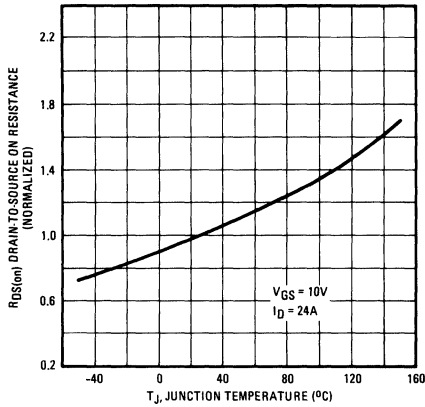


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

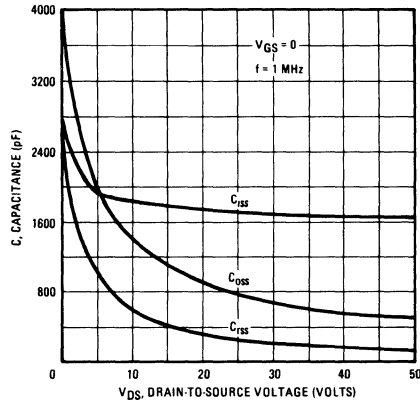


Fig. 11 — Power Vs. Temperature Derating Curve

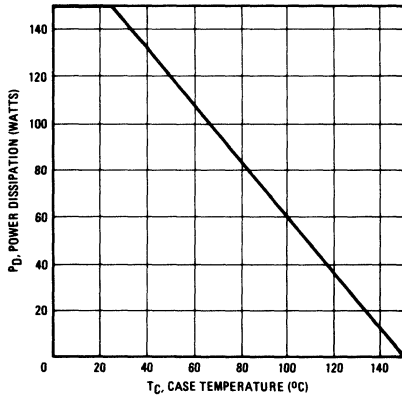


Fig. 12 — Typical Body-Drain Diode Forward Voltage

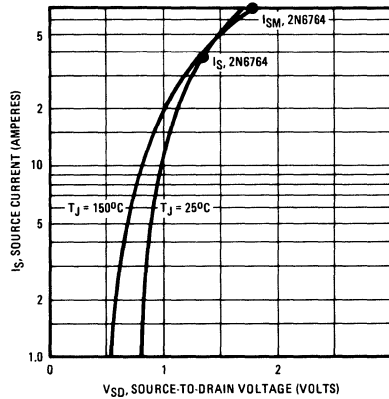


Fig. 13 — Switching Time Test Circuit

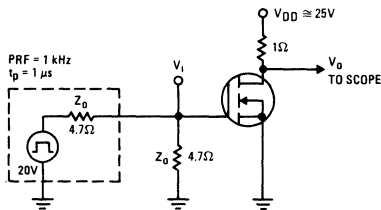
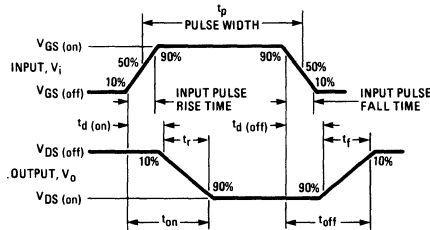


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

200 Volt, 0.085 Ohm
N-Channel

2N6765
J, JTX, JTXV 2N6766

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/543A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

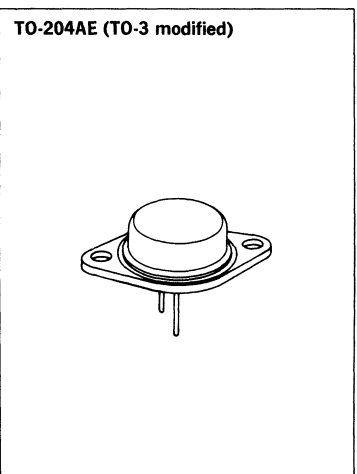
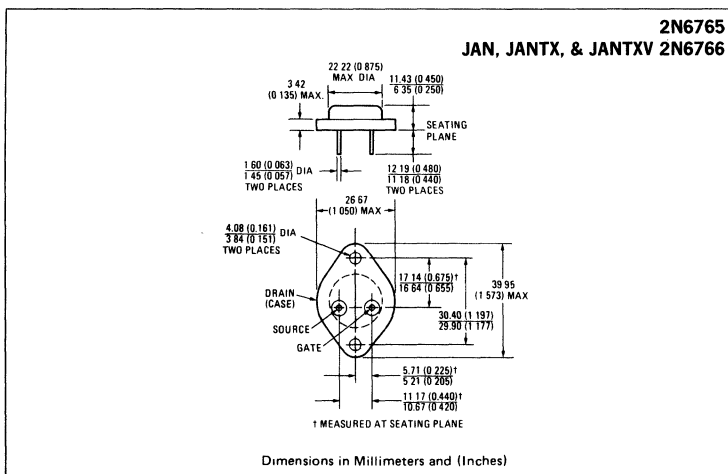
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6765	150V	0.120 Ω	25A
2N6766	200V	0.085 Ω	30A

MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6765	2N6766	Units
V _{DS} Drain – Source Voltage	150*	200*	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ)	150*	200*	V
I _D @ T _C = 25°C Continuous Drain Current	25*	30*	A
I _D @ T _C = 100°C Continuous Drain Current	16*	19*	A
I _{DM} Pulsed Drain Current	50	60	A
V _{GS} Gate – Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	150* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	60* (See Fig. 11)		W
Linear Derating Factor	1.2* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 50 60		A
T _J Operating and Storage Temperature Range	-55* to 150*		°C
T _{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V _{GS} = 0
	2N6766	200	–	–	V	I _D = 1.0 mA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate – Body Leakage Forward	ALL	–	–	100*	nA	V _{GS} = 20V
I _{GSSR} Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0
		–	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6765	–	–	3.0*	V	V _{GS} = 10V, I _D = 25A
	2N6766	–	–	2.7*	V	V _{GS} = 10V, I _D = 30A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6765	–	0.09	0.12*	Ω	V _{GS} = 10V, I _D = 16A
	2N6766	–	0.07	0.085*	Ω	V _{GS} = 10V, I _D = 19A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6765	–	–	0.216*	Ω	V _{GS} = 10V, I _D = 16A, T _C = 125°C
	2N6766	–	–	0.153*	Ω	V _{GS} = 10V, I _D = 19A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	9.0*	15.5	27*	S (Ω)	V _{DS} = 15V, I _D = 19A
C _{iss} Input Capacitance	ALL	1000*	2000	3000*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	450*	800	1200*	pF	
C _{rss} Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
t _{d(on)} Turn-On Delay Time	ALL	–	–	35*	ns	V _{DD} ≅ 95V, I _D = 19A, Z _o = 4.7Ω
t _r Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	–	–	100*	ns	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	–	–	0.83*	K/W	
R _{thCS} Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6766	–	–	30*	A	
I _{SM} Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
	2N6766	–	–	60	A	
V _{SD} Diode Forward Voltage ①	2N6765	0.85*	–	1.7*	V	T _C = 25°C, I _S = 25A, V _{GS} = 0
	2N6766	0.9*	–	1.8*	V	T _C = 25°C, I _S = 30A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	–	500	–	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	–	10	–	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≦ 300 μsec, Duty Cycle ≦ 2%

Fig. 1 – Clamped Inductive Test Circuit

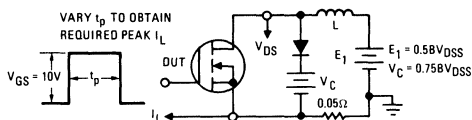


Fig. 2 – Clamped Inductive Waveforms



Fig. 3 – Typical Output Characteristics

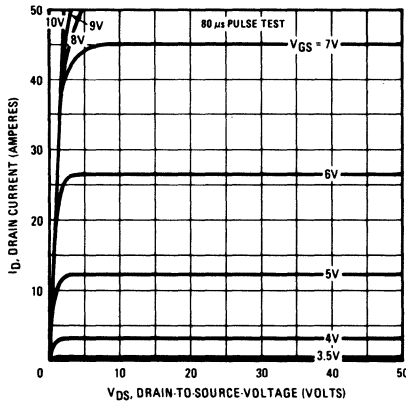


Fig. 5 – Typical Saturation Characteristics (2N6765)

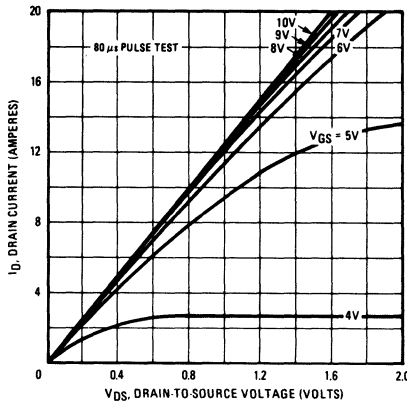


Fig. 7 – Typical Transconductance Vs. Drain Current

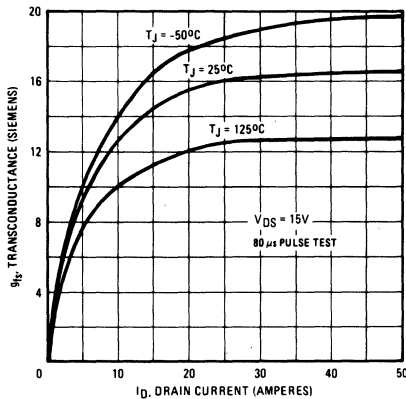


Fig. 4 – Typical Transfer Characteristics

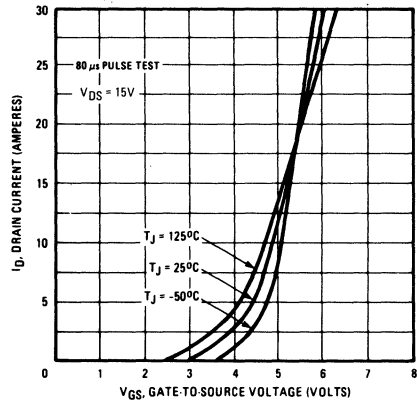


Fig. 6 – Typical Saturation Characteristics (2N6766)

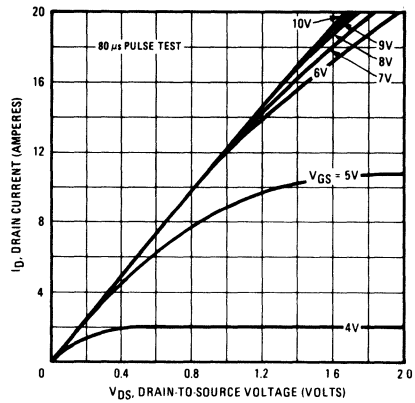


Fig. 8 – Maximum Safe Operating Area

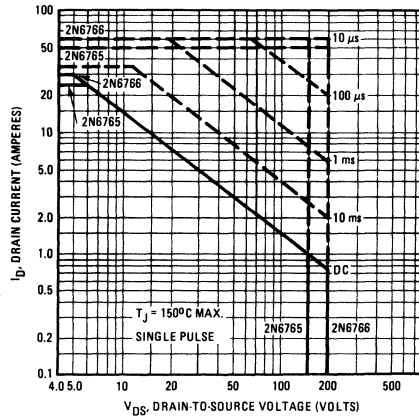


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

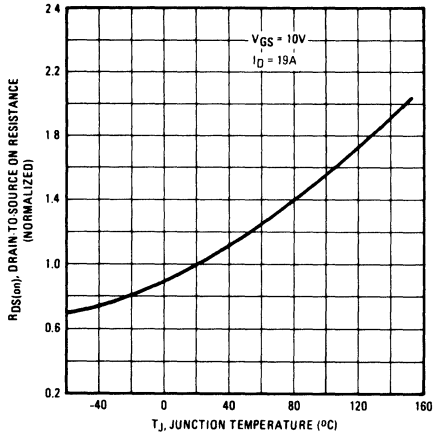


Fig. 11 — Power Vs. Temperature Derating Curve

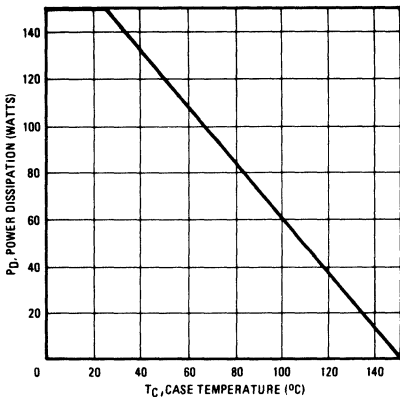


Fig. 13 — Switching Time Test Circuit

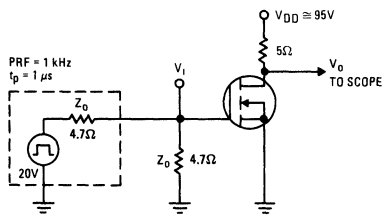


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

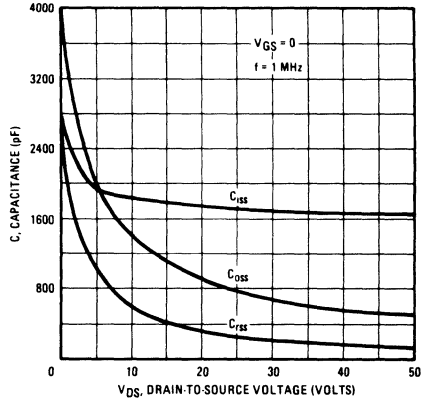


Fig. 12 — Typical Body-Drain Diode Forward Voltage

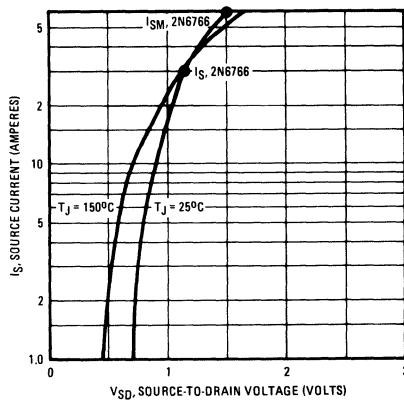
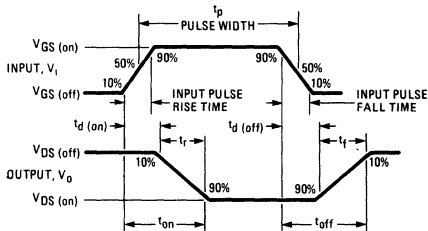


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

400 Volt, 0.3 Ohm
N-Channel

2N6767
J, JTX, JTXV 2N6768

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/543A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

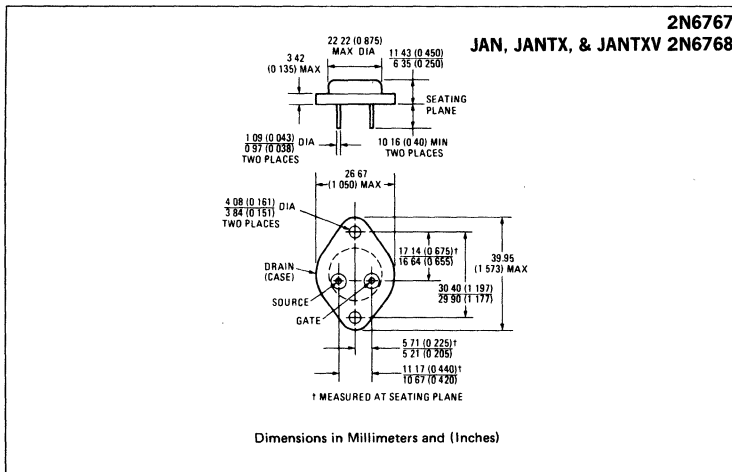
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

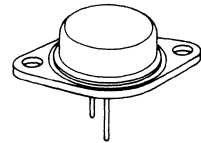
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6767	350V	0.4 Ω	12A
2N6768	400V	0.3 Ω	14A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6767	2N6768	Units
V _{DS} Drain - Source Voltage	350*	400*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ)	350*	400*	V
I _D @ T _C = 25°C Continuous Drain Current	12*	14*	A
I _D @ T _C = 100°C Continuous Drain Current	7.75*	9.0*	A
I _{DM} Pulsed Drain Current	20	25	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	150* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	60* (See Fig. 11)		W
Linear Derating Factor	1.2* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 20 25		A
T _J Operating and Storage Temperature Range	-55° to 150°		°C
T _{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	2N6767	350	-	-	V	V _{GS} = 0 I _D = 1.0 mA
	2N6768	400	-	-	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	-	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate - Body Leakage Forward	ALL	-	-	100*	nA	V _{GS} = 20V
I _{GSSR} Gate - Body Leakage Reverse	ALL	-	-	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	-	0.1	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0
		-	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6767	-	-	5.4*	V	V _{GS} = 10V, I _D = 12A
	2N6768	-	-	5.6*	V	V _{GS} = 10V, I _D = 14A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6767	-	0.3	0.4*	Ω	V _{GS} = 10V, I _D = 7.75A
	2N6768	-	0.25	0.3*	Ω	V _{GS} = 10V, I _D = 9.0A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6767	-	-	0.88*	Ω	V _{GS} = 10V, I _D = 7.75A, T _C = 125°C
	2N6768	-	-	0.66*	Ω	V _{GS} = 10V, I _D = 9.0A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	8.0*	11.0	24*	S (Ω)	V _{DS} = 15V, I _D = 9.0A
C _{iss} Input Capacitance	ALL	1000*	2000	3000*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	200*	400	600*	pF	
C _{rss} Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
t _{d(on)} Turn-On Delay Time	ALL	-	-	35*	ns	
t _r Rise Time	ALL	-	-	65*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	-	-	150*	ns	
t _f Fall Time	ALL	-	-	75*	ns	
(MOSFET switching times are essentially independent of operating temperature)						

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	-	-	0.83*	K/W	
R _{thCS} Case-to-Sink	ALL	-	0.1	-	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	-	-	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6767	-	-	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6768	-	-	14*	A	
I _{SM} Pulsed Source Current (Body Diode)	2N6767	-	-	20	A	
	2N6768	-	-	25	A	
V _{SD} Diode Forward Voltage ①	2N6767	0.8*	-	1.6*	V	T _C = 25°C, I _S = 12A, V _{GS} = 0
	2N6768	0.85*	-	1.7*	V	T _C = 25°C, I _S = 14A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	-	1000	-	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	-	25	-	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

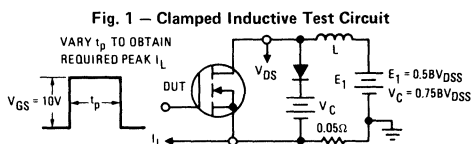


Fig. 1 - Clamped Inductive Test Circuit

Fig. 2 - Clamped Inductive Waveforms



Fig. 3 – Typical Output Characteristics

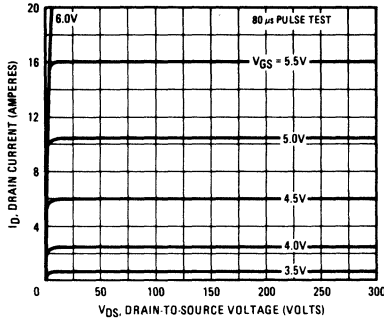


Fig. 5 – Typical Saturation Characteristics (2N6767)

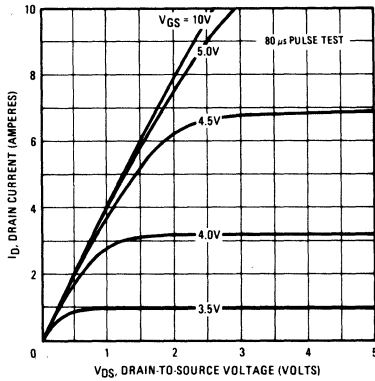


Fig. 7 – Typical Transconductance Vs. Drain Current

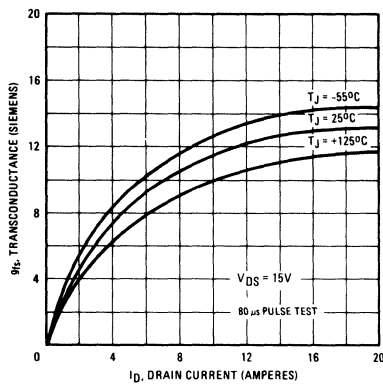


Fig. 4 – Typical Transfer Characteristics

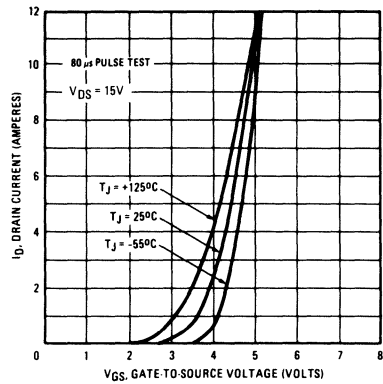


Fig. 6 – Typical Saturation Characteristics (2N6768)

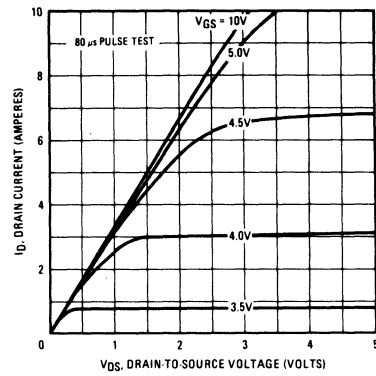


Fig. 8 – Maximum Safe Operating Area

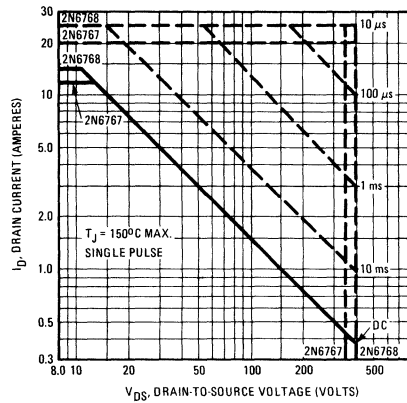


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

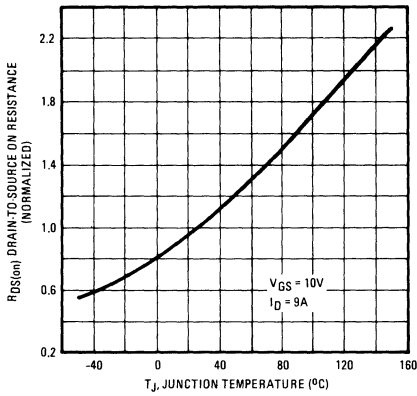


Fig. 10—Typical Capacitance Vs. Drain-to-Source Voltage

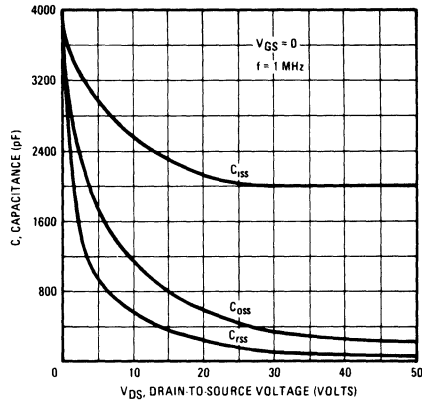


Fig. 11—Power Vs. Temperature Derating Curve

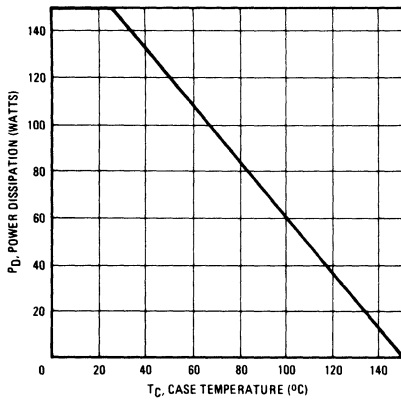


Fig. 12—Typical Body-Drain Diode Forward Voltage

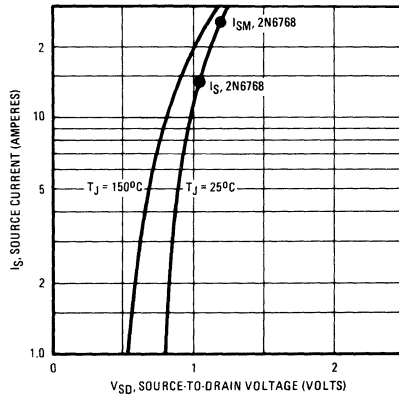


Fig. 13—Switching Time Test Circuit

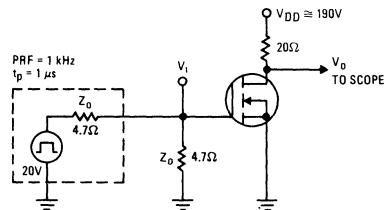
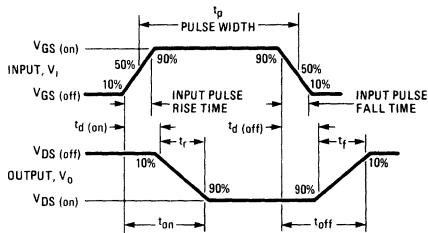


Fig. 14—Switching Time Waveforms



POWER MOSFET TRANSISTORS

500 Volt, 0.4 Ohm
N-Channel

2N6769
J, JTX, JTXV 2N6770

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability
- Qualified to MIL-S-19500/543A

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

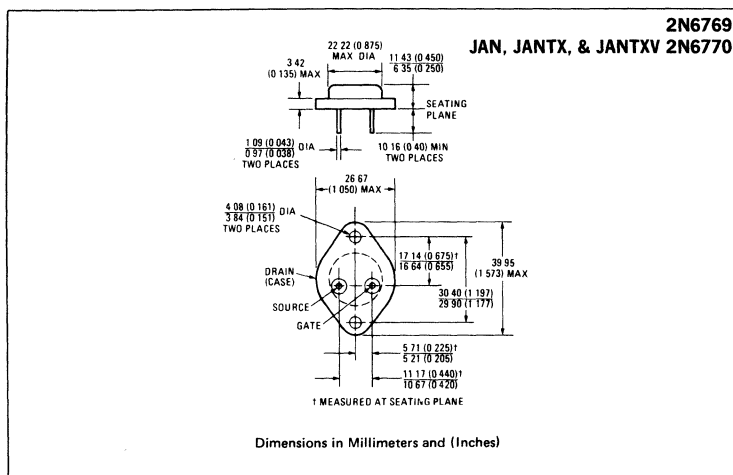
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

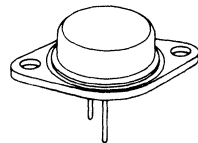
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6769	450V	0.5Ω	11A
2N6770	500V	0.4Ω	12A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6769	2N6770	Units
V _{DS} Drain – Source Voltage	450*	500*	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ)	450*	500*	V
I _D @ T _C = 25°C Continuous Drain Current	11*	12*	A
I _D @ T _C = 100°C Continuous Drain Current	7.0*	7.75*	A
I _{DM} Pulsed Drain Current	20	25	A
V _{GS} Gate – Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	150* (See Fig. 11)		W
P _D @ T _C = 100°C Max. Power Dissipation	60* (See Fig. 11)		W
Linear Derating Factor	1.2* (See Fig. 11)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 20 25		A
T _J Operating and Storage Temperature Range	-55° to 150°		°C
T _{stg} Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C




ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain – Source Breakdown Voltage	2N6769	450	–	–	V	V _{GS} = 0
	2N6770	500	–	–	V	I _D = 4.0 mA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V _{DS} = V _{GS} , I _D = 1 mA
I _{GSSF} Gate – Body Leakage Forward	ALL	–	–	100*	nA	V _{GS} = 20V
I _{GSSR} Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V _{DS} = 0.8 x Max. Rating, V _{GS} = 0
		–	0.2	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0, T _C = 25°C to 125°C
V _{DS(on)} Static Drain-Source On-State Voltage ①	2N6769	–	–	6.0*	V	
	2N6770	–	–	6.0*	V	
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6769	–	0.4	0.5*	Ω	V _{GS} = 10V, I _D = 7.0A
	2N6770	–	0.3	0.4*	Ω	V _{GS} = 10V, I _D = 7.75A
R _{DS(on)} Static Drain-Source On-State Resistance ①	2N6769	–	–	1.1*	Ω	V _{GS} = 10V, I _D = 7.0A, T _C = 125°C
	2N6770	–	–	0.88*	Ω	V _{GS} = 10V, I _D = 7.75A, T _C = 125°C
g _{fs} Forward Transconductance ①	ALL	8.0*	12.0	24*	S (Ω)	V _{DS} = 15V, I _D = 7.75A
C _{iss} Input Capacitance	ALL	1000*	2000	3000*	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	200*	400	600*	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
t _{d(on)} Turn-On Delay Time	ALL	–	–	35*	ns	V _{DD} ≅ 210V, I _D = 7.75A, Z _o = 4.7Ω
t _r Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
t _{d(off)} Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	–	–	70*	ns	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	–	–	0.83*	K/W	
R _{thCS} Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6770	–	–	12*	A	
I _{SM} Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
	2N6770	–	–	25	A	
V _{SD} Diode Forward Voltage ①	2N6769	0.75*	–	1.5*	V	T _C = 25°C, I _S = 11A, V _{GS} = 0
	2N6770	0.80*	–	1.6*	V	T _C = 25°C, I _S = 12A, V _{GS} = 0
t _{rr} Reverse Recovery Time	ALL	–	400	–	ns	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	–	10	–	μC	T _J = 150°C, I _F = I _{SM} , dI _F /dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≦ 300 μsec, Duty Cycle ≦ 2%

Fig. 1 – Clamped Inductive Test Circuit

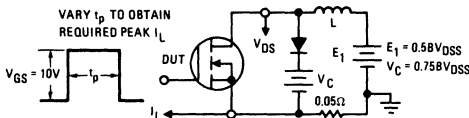


Fig. 2 – Clamped Inductive Waveforms

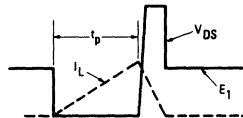


Fig. 3 — Typical Output Characteristics

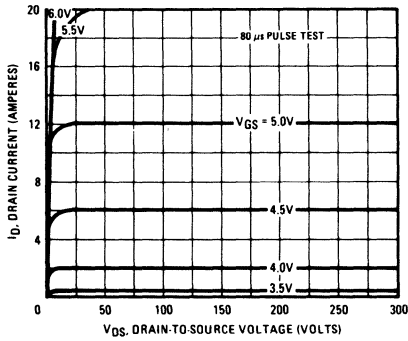


Fig. 4 — Typical Transfer Characteristics

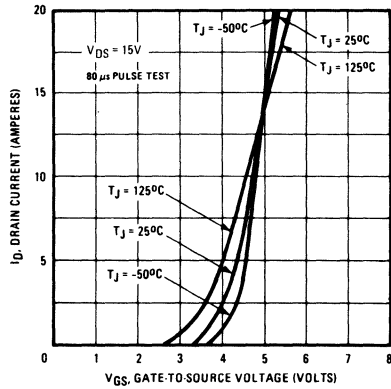


Fig. 5 — Typical Saturation Characteristics (2N6769)

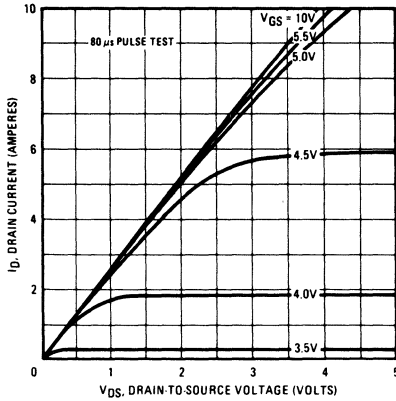


Fig. 6 — Typical Saturation Characteristics (2N6770)

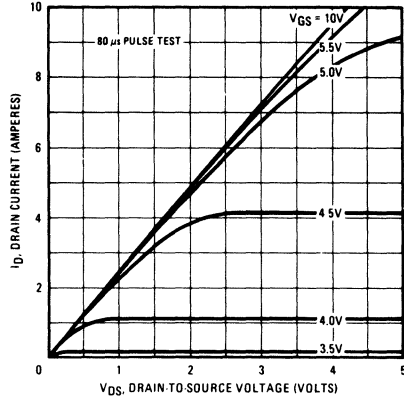


Fig. 7 — Typical Transconductance Vs. Drain Current

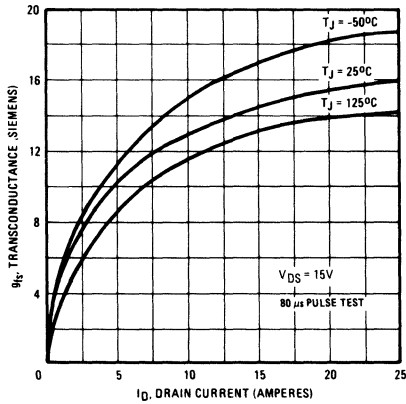


Fig. 8 — Maximum Safe Operating Area

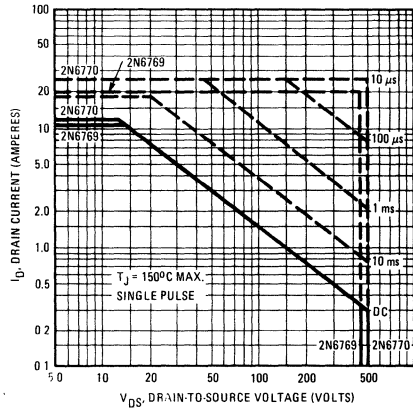


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

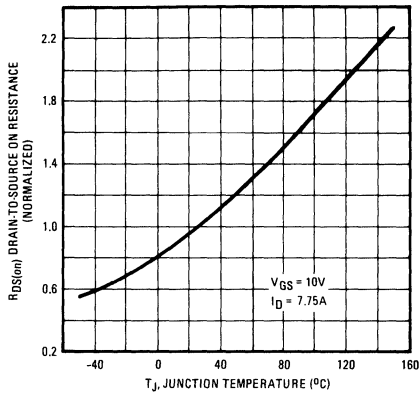


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

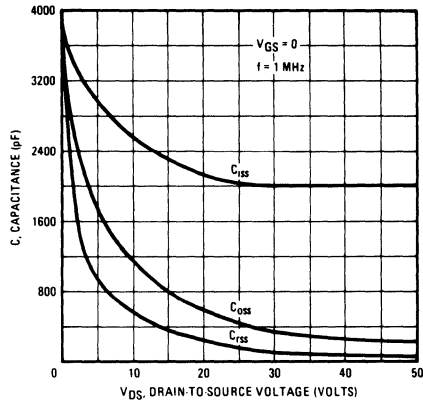


Fig. 11 – Power Vs. Temperature Derating Curve

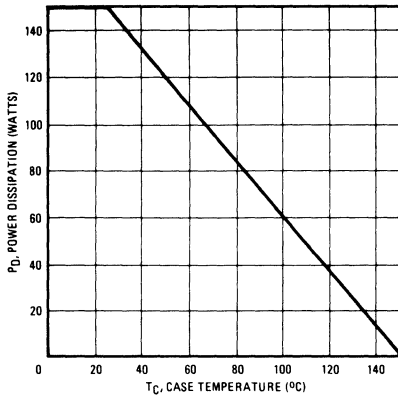


Fig. 12 – Typical Body-Drain Diode Forward Voltage

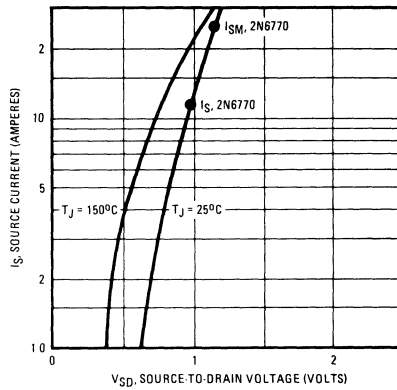


Fig. 13 – Switching Time Test Circuit

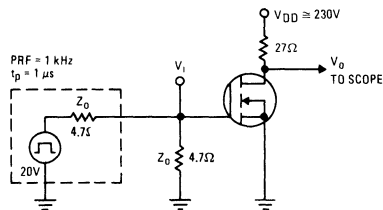
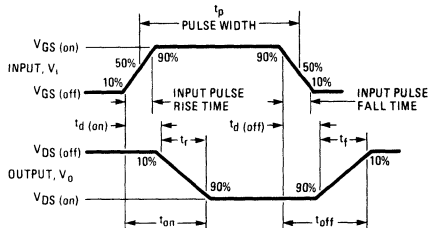


Fig. 14 – Switching Time Waveforms



POWER MOSFET TRANSISTORS

100 Volt, 0.6 Ohm
N-Channel

2N6781
2N6782

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

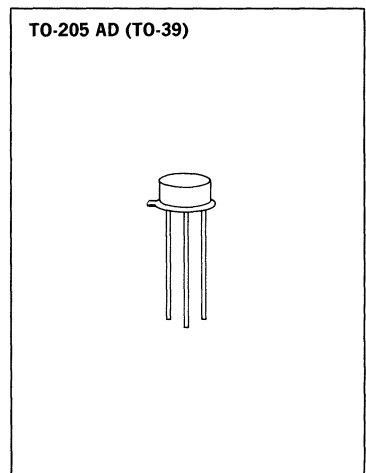
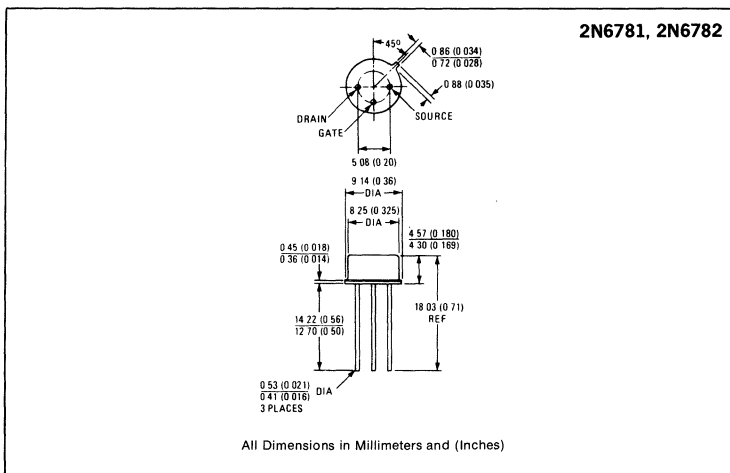
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6781	60V	0.6Ω	3.5A
2N6782	100V	0.6Ω	3.5A

MECHANICAL SPECIFICATIONS

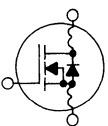


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6781	2N6782	Units
V _{DS} Drain - Source Voltage ①	60*	100*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	60*	100*	V
I _D @ T _C = 25°C Continuous Drain Current	3.5*	3.5*	A
I _{DM} Pulsed Drain Current ③	14	14	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	15* (See Fig. 14)		W
Linear Derating Factor	0.12* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	14	(See Fig. 15 and 16) L = 100μH 14	
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6781	60*	—	—	V	V _{GS} = 0V	
	2N6782	100*	—	—	V	I _D = 500μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 500μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	500*	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	2000*	μA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	3.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.6*	Ω	V _{GS} = 10V, I _D = 2.25A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.08*	Ω	V _{GS} = 10V, I _D = 2.25A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	2.1*	V	V _{GS} = 10V, I _D = 3.5A	
g _{fs} Forward Transconductance ②	ALL	1.0*	—	3.0*	S(Ω)	V _{DS} = 15V, I _D = 2.25A	
C _{iss} Input Capacitance	ALL	60*	—	200*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	40*	—	100*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	10*	—	25*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	15*	ns	V _{DD} = 35V, I _D = 2.25A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	25*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	25*	ns		
t _f Fall Time	ALL	—	—	20*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC		V _{GS} = 10V, I _D = 8.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	2.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	8.33*	K/W	Free Air Operation
R _{thJA} Junction-to Ambient	ALL	—	—	175	K/W	

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	3.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	14	A		
V_{SD}	Diode Forward Voltage ②	ALL	.75*	—	1.5*	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$	
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{rr}	Reverse Recovered Charge	ALL	—	1.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

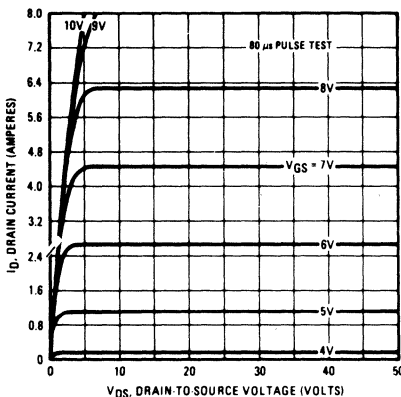


Fig. 2 – Typical Transfer Characteristics

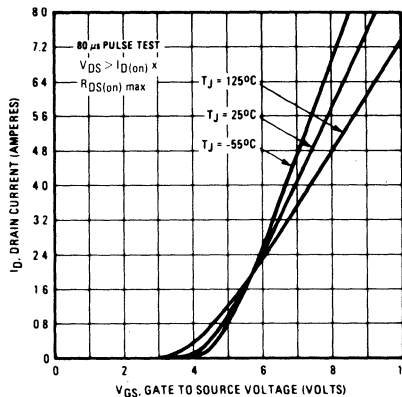


Fig. 3 – Typical Saturation Characteristics

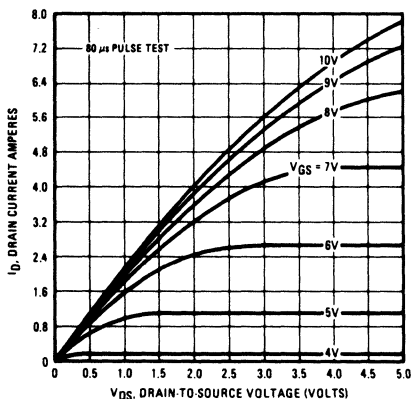


Fig. 4 – Forward Bias Safe Operating Area

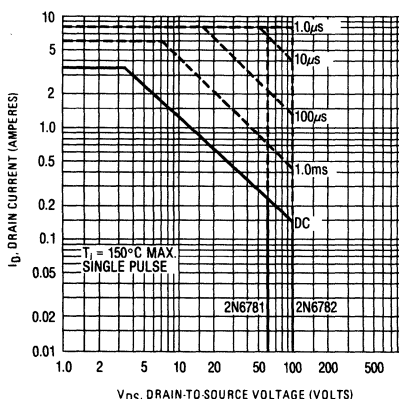
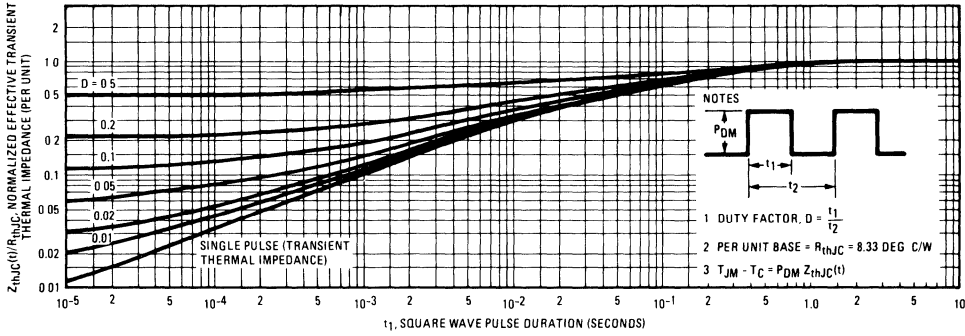


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

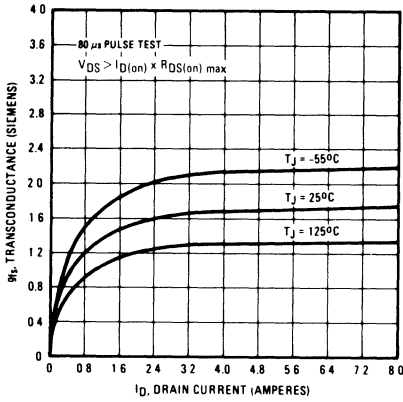


Fig. 7 – Typical Source-Drain Diode Forward Voltage

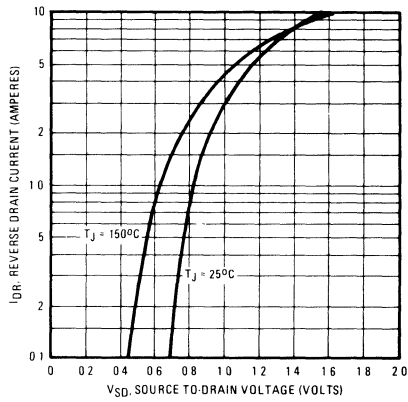


Fig. 8 – Breakdown Voltage Vs. Temperature

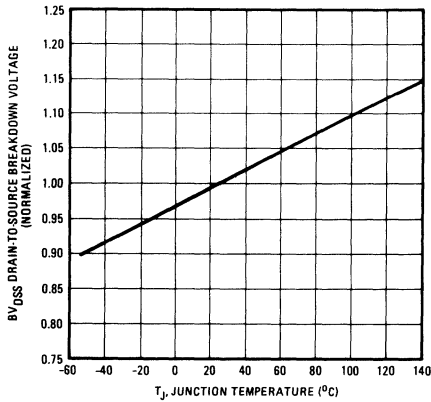


Fig. 9 – Normalized On-Resistance Vs. Temperature

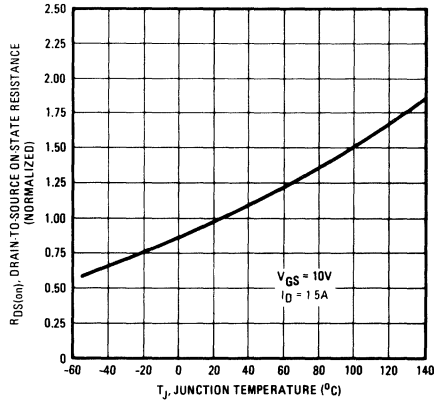


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

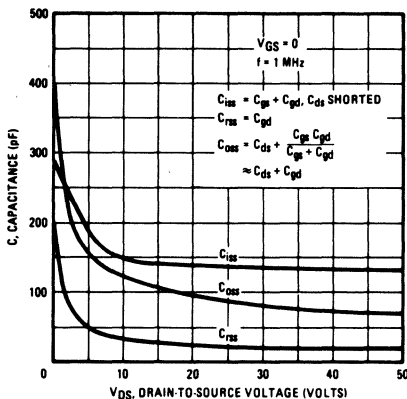


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

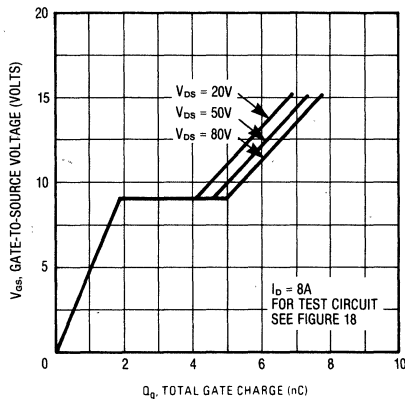


Fig. 12 – Typical On-Resistance Vs. Drain Current

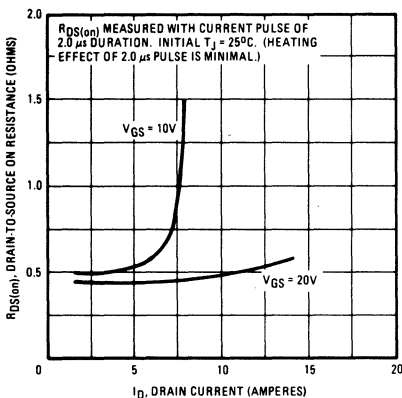


Fig. 13 – Maximum Drain Current Vs. Case Temperature

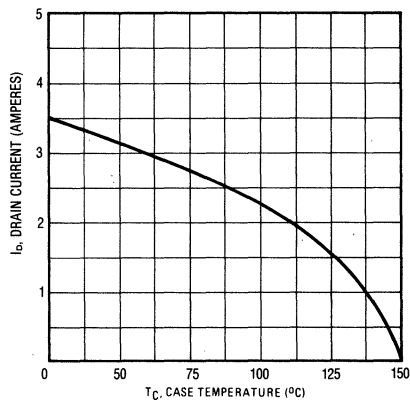


Fig. 14 – Power Vs. Temperature Derating Curve

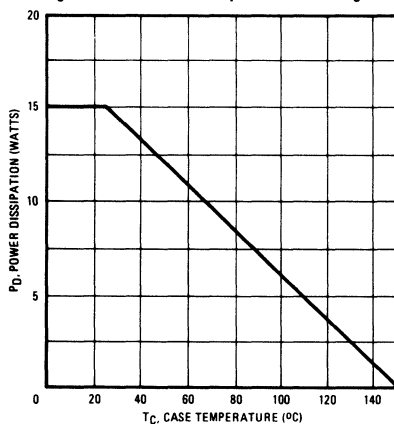


Fig. 15 – Clamped Inductive Test Circuit

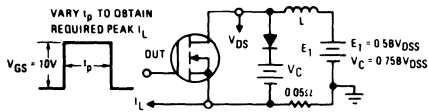


Fig. 16 – Clamped Inductive Waveforms

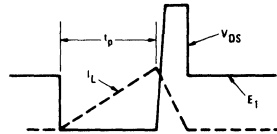


Fig. 17 – Switching Time Test Circuit

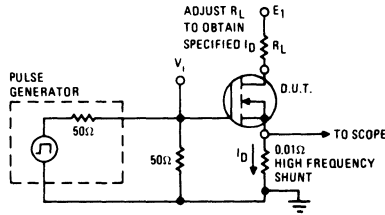
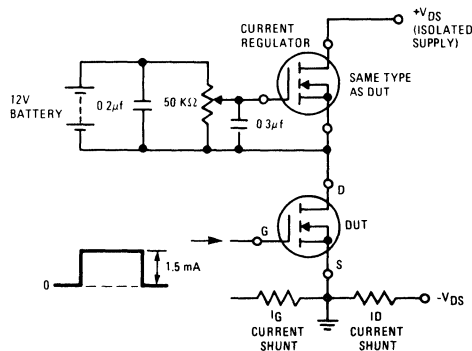


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

2N6783
2N6784

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

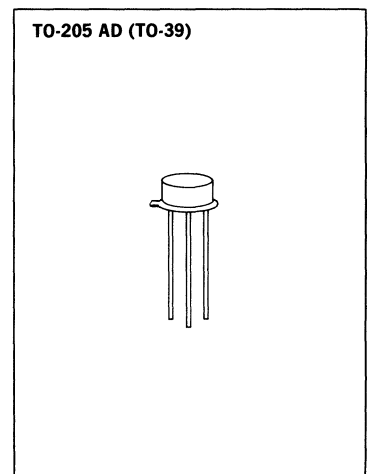
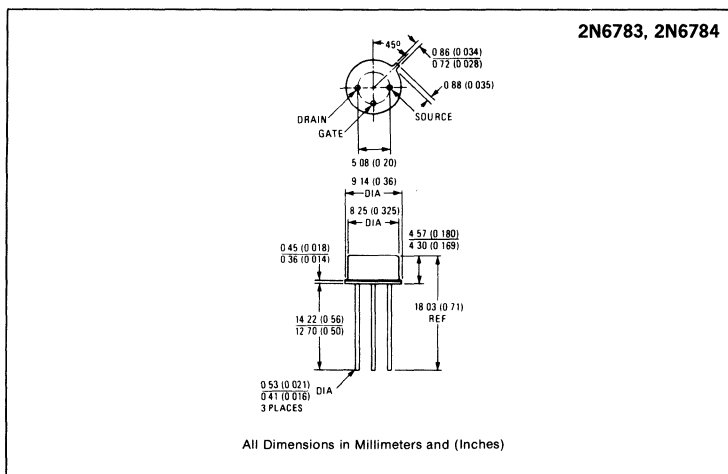
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6783	150V	1.5Ω	2.25A
2N6784	200V	1.5Ω	2.25A

MECHANICAL SPECIFICATIONS

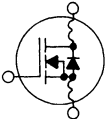


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6783	2N6784		Units
V _{DS} Drain - Source Voltage ①	150*	200*		V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	150*	200*		V
I _D @ T _C = 25°C Continuous Drain Current	2.25*	2.25*		A
I _{DM} Pulsed Drain Current ③	9.0	9.0		A
V _{GS} Gate - Source Voltage	±20*			V
P _D @ T _C = 25°C Max. Power Dissipation	15* (See Fig. 14)			W
Linear Derating Factor	0.12* (See Fig. 14)			W/K
I _{LM} Inductive Current, Clamped	9.0	(See Fig. 15 and 16) L = 100μH 9.0		A
T _J Operating Junction and Storage Temperature Range	-55 to 150			°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*			°C

4

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
B _{Voss} ****	2N6783	150*	—	—	V	V _{GS} = 0V	
	2N6784	200*	—	—	V	I _D = 500μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 500μA	
I _{GS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	500*	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	2000*	μA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	2.25	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.5*	Ω	V _{GS} = 10V, I _D = 1.5A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	2.81	Ω	V _{GS} = 10V, I _D = 1.5A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	3.37*	V	V _{GS} = 10V, I _D = 2.25A	
g _{fs} Forward Transconductance ②	ALL	.9*	—	2.7*	S(Ω)	V _{DS} = 15V, I _D = 1.5A	
C _{iss} Input Capacitance	ALL	60*	—	200*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	20*	—	80*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	5*	—	25*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	15*	ns	V _{DD} = 75V, I _D = 1.5A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	20*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	30*	ns		
t _f Fall Time	ALL	—	—	20*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V _{GS} = 10V, I _D = 4.5A, V _{DS} = 0.8 Max. Rating, See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	2.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	8.33*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	2.25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	9	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.7	—	1.5*	V	$T_C = 25^\circ\text{C}$, $I_S = 2.25\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 2.25\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 2.25\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

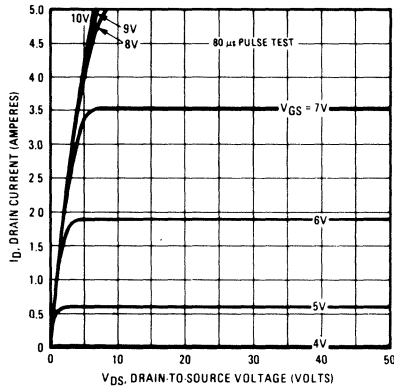


Fig. 2 – Typical Transfer Characteristics

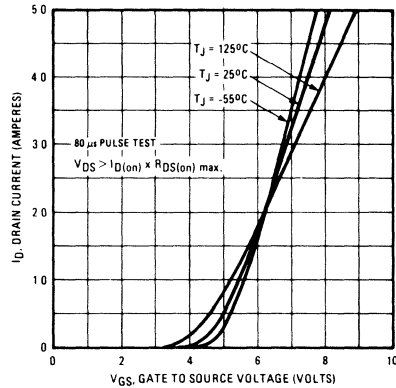


Fig. 3 – Typical Saturation Characteristics

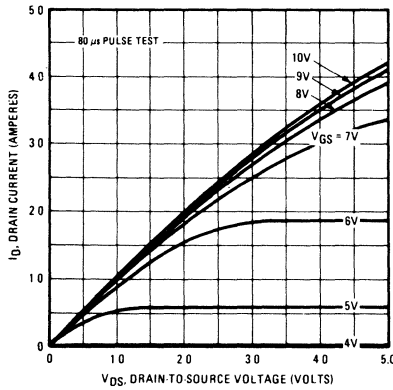


Fig. 4 – Maximum Safe Operating Area

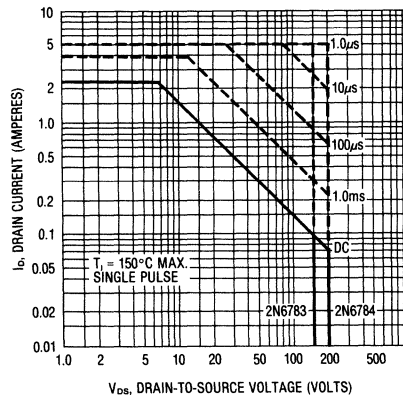
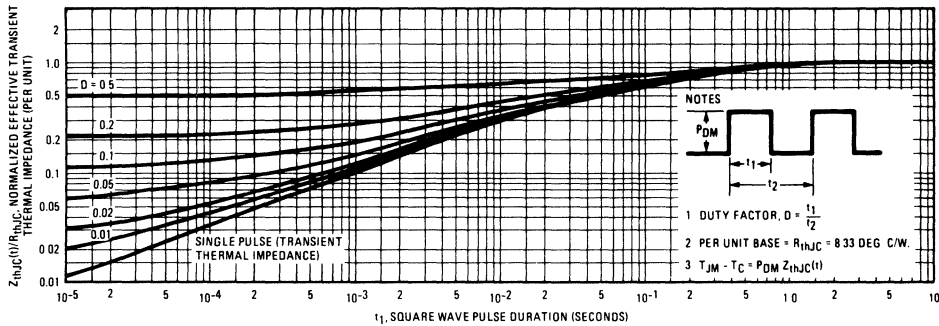


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

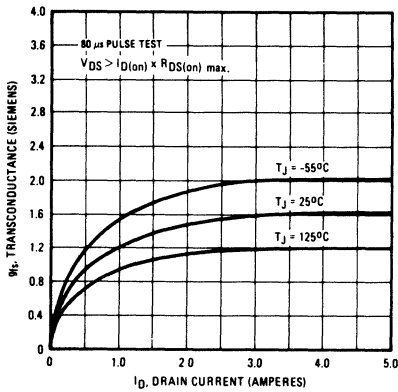


Fig. 7 – Typical Source-Drain Diode Forward Voltage

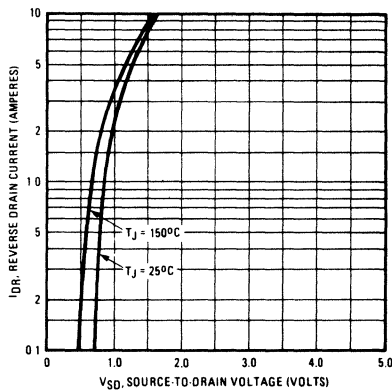


Fig. 8 – Breakdown Voltage Vs. Temperature

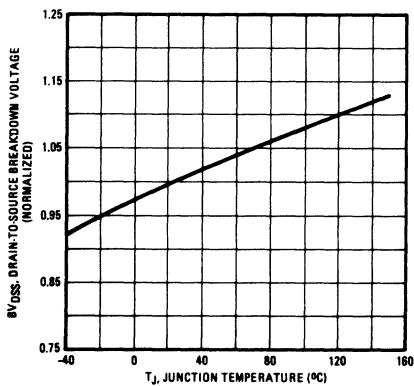


Fig. 9 – Normalized On-Resistance Vs. Temperature

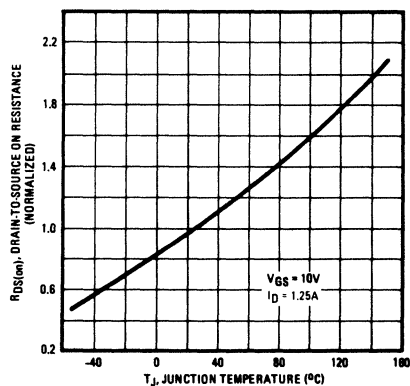


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

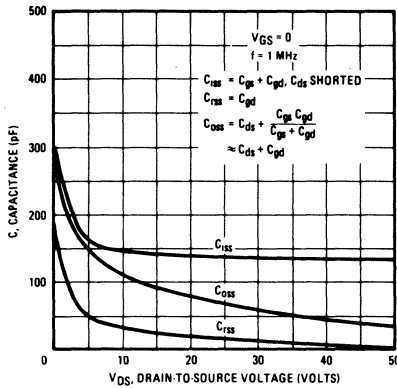


Fig. 11 — Typical Gate Charge vs. Gate-to-Source Voltage

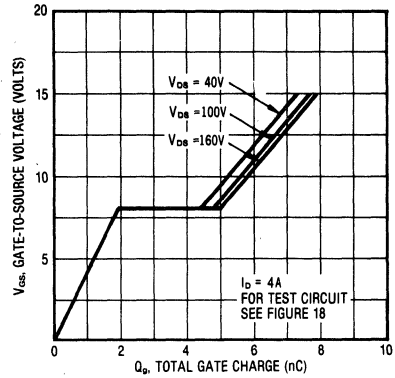


Fig. 12 — Typical On-Resistance Vs. Drain Current

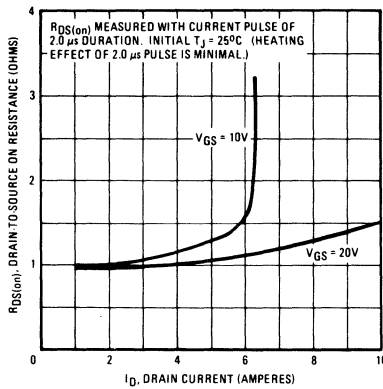


Fig. 13 — Maximum Drain Current vs. Case Temperature

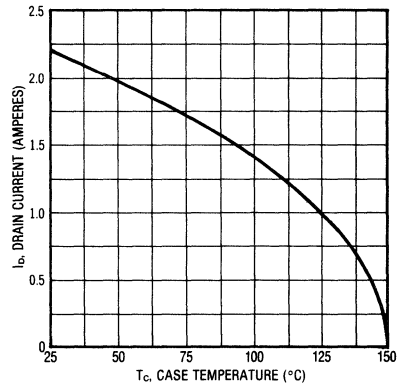


Fig. 14 — Power Vs. Temperature Derating Curve

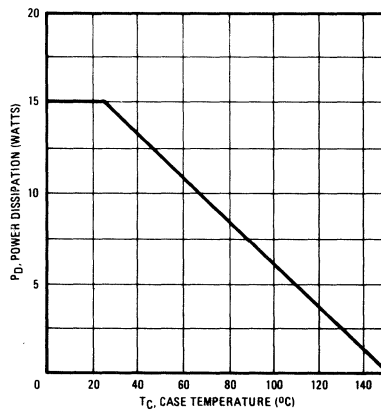


Fig. 15 — Clamped Inductive Test Circuit

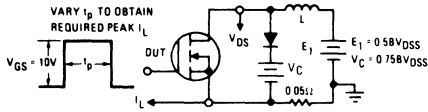


Fig. 16 — Clamped Inductive Waveforms

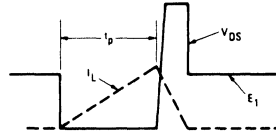


Fig. 17 — Switching Time Test Circuit

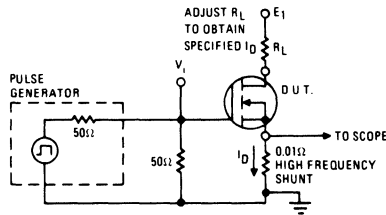
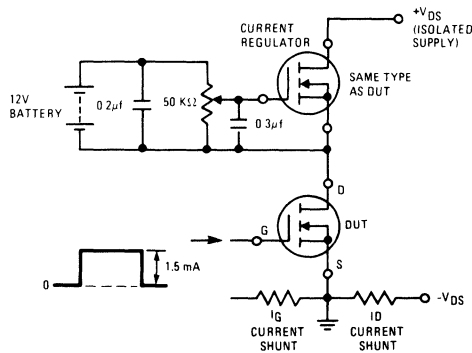


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 3.6 Ohm
N-Channel

2N6785
2N6786

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

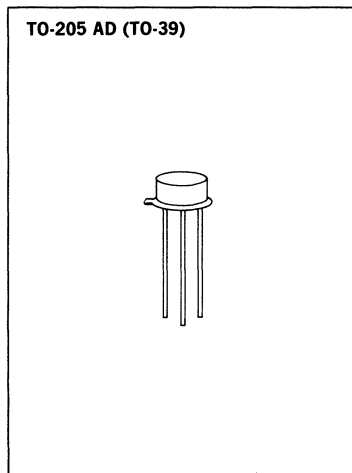
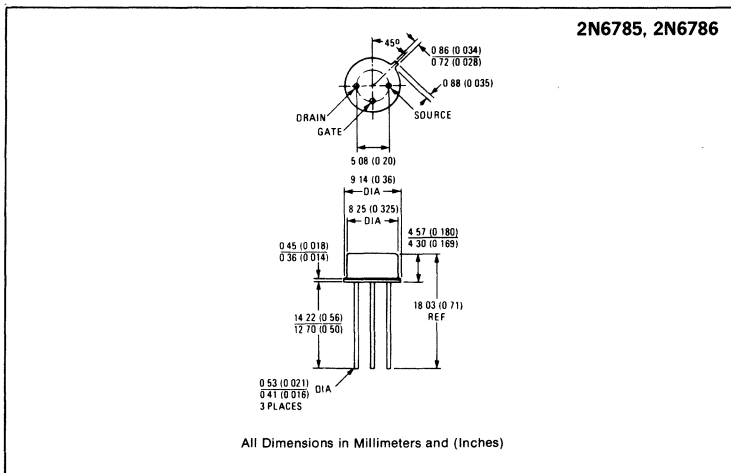
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6785	350V	3.6Ω	1.25A
2N6786	400V	3.6Ω	1.25A

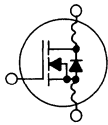
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6785	2N6786	Units
V _{DS} Drain - Source Voltage ①	350*	400*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	350*	400*	V
I _D @ T _C = 25°C Continuous Drain Current	1.25*	1.25*	A
I _{DM} Pulsed Drain Current ③	5.5	5.5	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	15* (See Fig. 14)		W
Linear Derating Factor	0.12* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 5.5		A
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		°C

ELECTRICAL CHARACTERISTICS @ T_c = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6785	350*	—	—	V	V _{GS} = 0V I _D = 500μA	
	2N6786	400*	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 500μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	500*	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
		—	—	2000*	μA		
I _{D(on)} On-State Drain Current ②	ALL	1.25	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	3.6*	Ω	V _{GS} = 10V, I _D = 0.8A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	7.92*	Ω	V _{GS} = 10V, I _D = 0.8A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	4.5*	V	V _{GS} = 10V, I _D = 1.25A	
g _{fs} Forward Transconductance ②	ALL	0.7*	—	2.1*	S(Ω)	V _{DS} = 15V, I _D = 0.8A	
C _{iss} Input Capacitance	ALL	60*	—	200*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	15*	—	50*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	2*	—	15*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	15*	ns	V _{DD} = 170V, I _D = 0.8A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	20*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	35*	ns		
t _f Fall Time	ALL	—	—	30*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	V _{GS} = 10V, I _D = 2.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	3.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	8.33*	K/W	
R _{thJA} Junction-to Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	1.25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	5.5	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.6*	—	1.4*	V	$T_C = 25^\circ\text{C}, I_S = 1.25\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.25\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.25\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

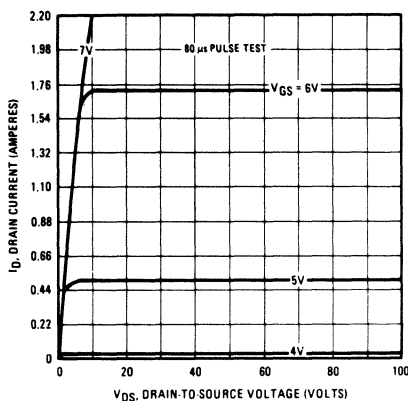


Fig. 2 – Typical Transfer Characteristics

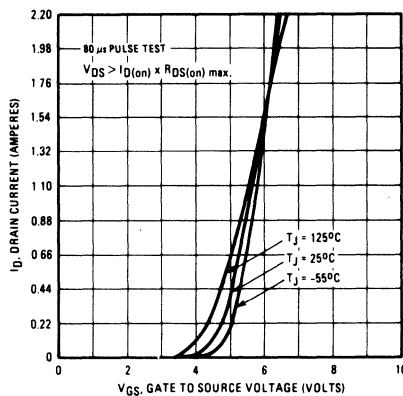


Fig. 3 – Typical Saturation Characteristics

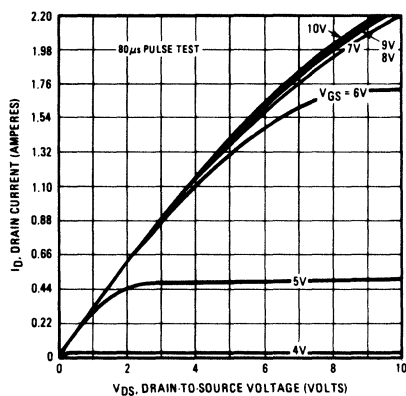


Fig. 4 – Forward Bias Safe Operating Area

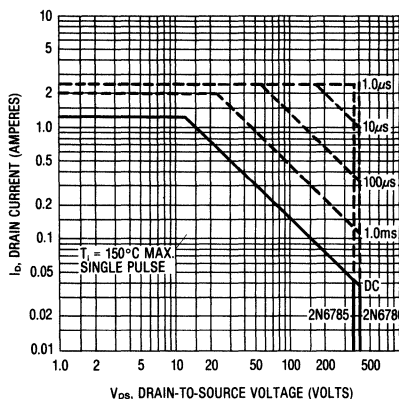


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

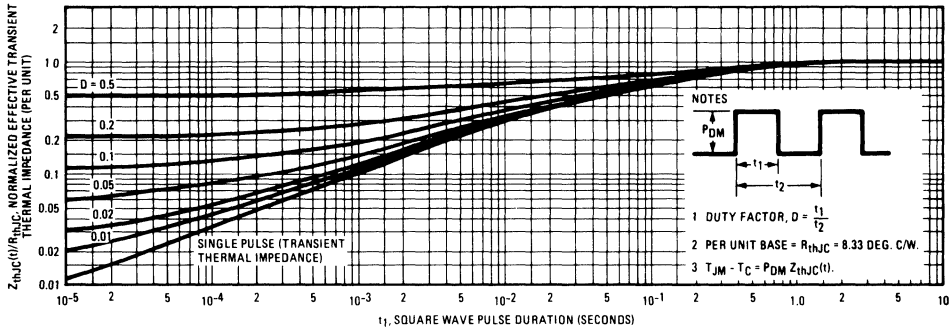


Fig. 6 — Typical Transconductance Vs. Drain Current

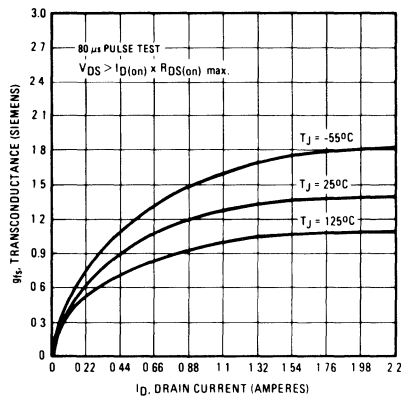


Fig. 7 — Typical Source-Drain Diode Forward Voltage

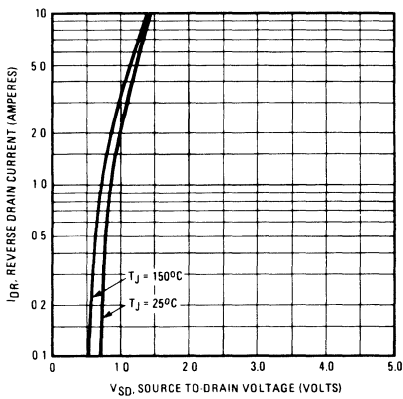


Fig. 8 — Breakdown Voltage Vs. Temperature

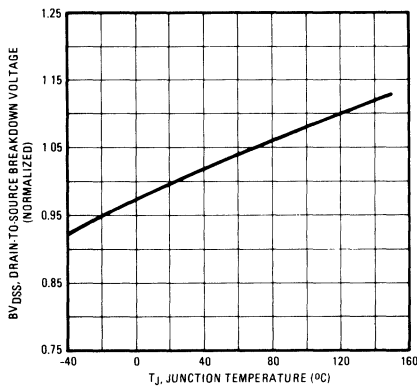


Fig. 9 — Normalized On-Resistance Vs. Temperature

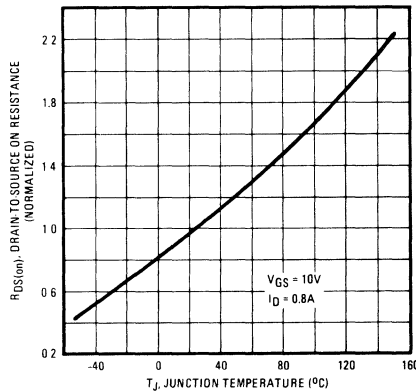


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

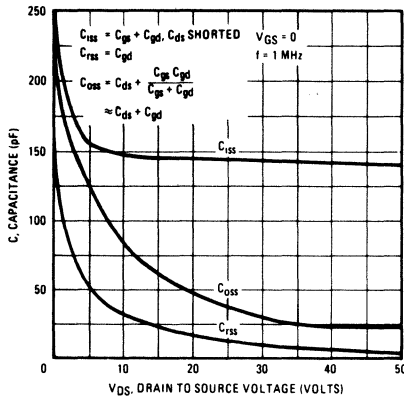


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

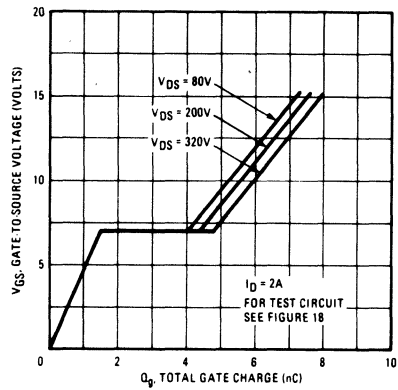


Fig. 12 — Typical On-Resistance Vs. Drain Current

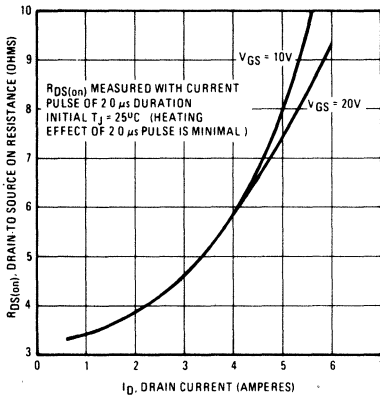


Fig. 13 — Maximum Drain Current Vs. Case Temperature

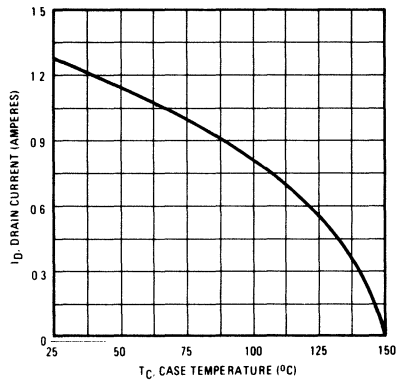


Fig. 14 — Power Vs. Temperature Derating Curve

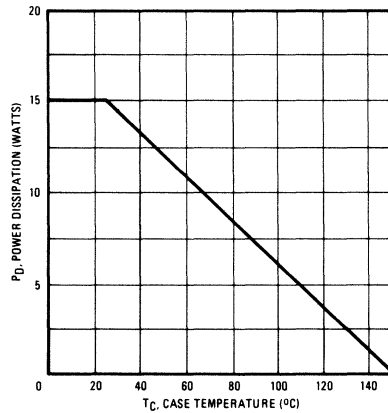


Fig. 15 – Clamped Inductive Test Circuit

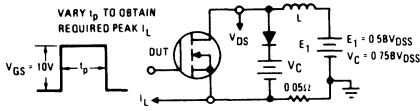


Fig. 16 – Clamped Inductive Waveforms

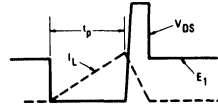


Fig. 17 – Switching Time Test Circuit

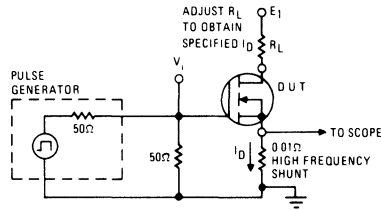
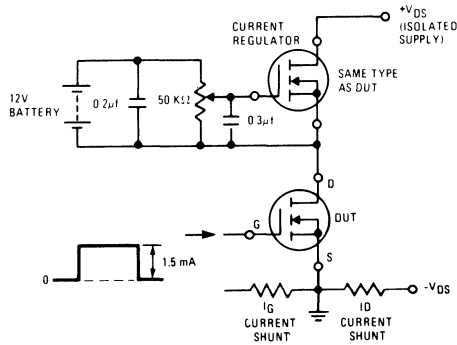


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.30 Ohm
N-Channel

2N6787
2N6788

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

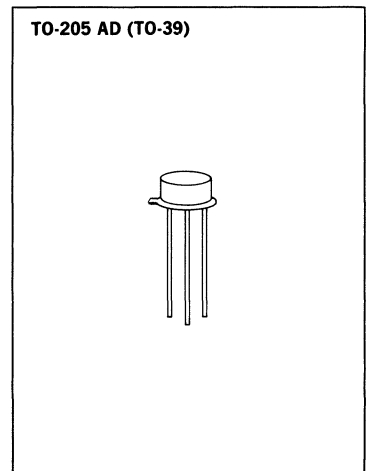
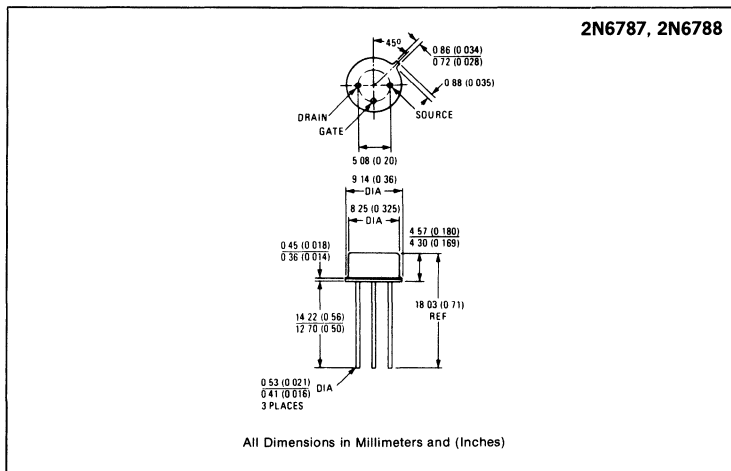
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6787	60V	0.30Ω	6.0A
2N6788	100V	0.30Ω	6.0A

MECHANICAL SPECIFICATIONS

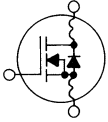


ABSOLUTE-MAXIMUM RATINGS

Parameter	2N6787	2N6788	Units
V _{DS} Drain - Source Voltage	60*	100*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1M Ω)	60*	100*	V
I _D @ T _C = 25°C Continuous Drain Current	6.0*	6.0*	A
I _{DM} Pulsed Drain Current	24	24	A
V _{GS} Gate - Source Voltage	±20*		
P _D @ T _C = 25°C Max. Power Dissipation	20* (See Fig. 14)		
Linear Derating Factor	0.16* (See Fig. 14)		
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100 μ H 24		
T _J Operating Junction and Storage Temperature Range	-55 to 150		
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		

4

ELECTRICAL CHARACTERISTICS @ T_c = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6787	60*	—	—	V	V _{GS} = 0V	
	2N6788	100*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
				4.0*			V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	ALL	6.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.30*	Ω	V _{GS} = 10V, I _D = 3.5A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.54*	Ω	V _{GS} = 10V, I _D = 3.5A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	1.80*	V	V _{GS} = 10V, I _D = 6.0A	
g _{fs} Forward Transconductance ②	ALL	1.5*	—	4.5*	S(ν)	V _{DS} = 15V, I _D = 3.5A	
C _{iss} Input Capacitance	ALL	200*	—	600*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	100*	—	400*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	20*	—	100*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	40*	ns	V _{DD} = 35V, I _D = 3.5A, Z _o = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	70*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	40*	ns		
t _f Fall Time	ALL	—	—	70*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC	V _{DD} = 35V, I _D = 2.25A, Z _o = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	6.25*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	24	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.8*	—	1.8*	V	$T_C = 25^\circ\text{C}, I_S = 6.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	$T_J = 150^\circ\text{C}, I_F = 6.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	1.2	—	μC	$T_J = 150^\circ\text{C}, I_F = 6.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

- ① $T_J = 25^\circ$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

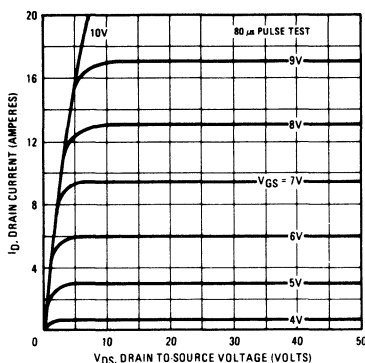


Fig. 3 – Typical Saturation Characteristics

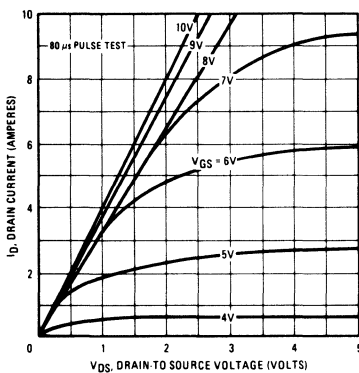


Fig. 2 – Typical Transfer Characteristics

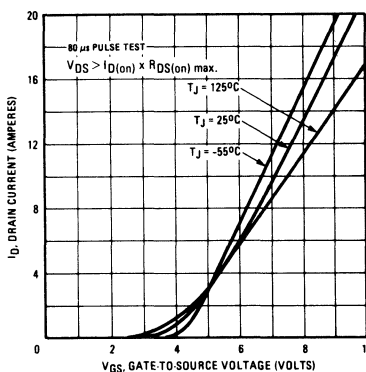


Fig. 4 – Forward Bias Safe Operating Area

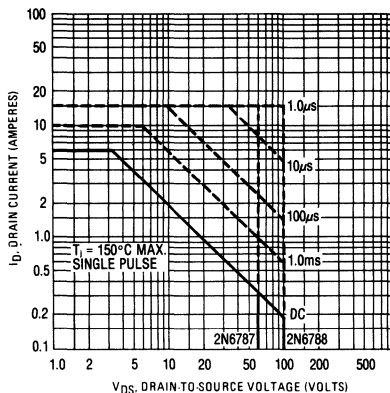


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

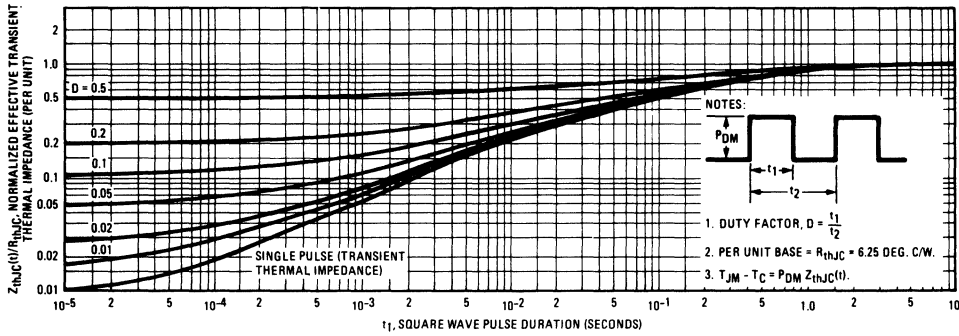


Fig. 6 – Typical Transconductance Vs. Drain Current

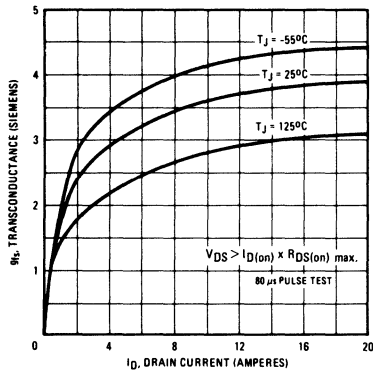


Fig. 7 – Typical Source-Drain Diode Forward Voltage

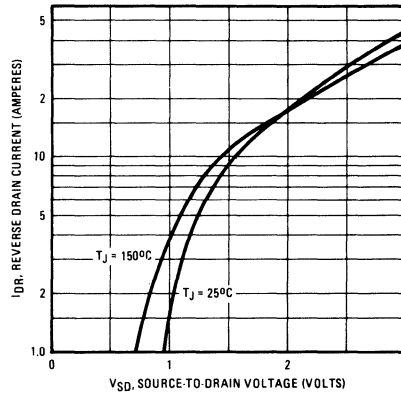


Fig. 8 – Breakdown Voltage Vs. Temperature

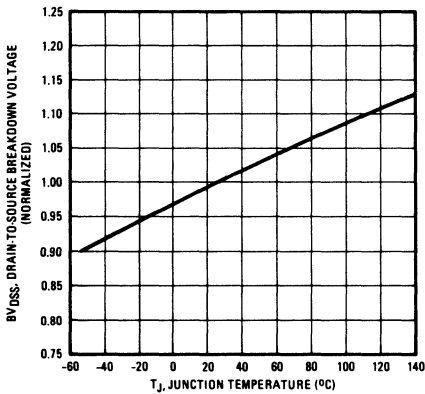


Fig. 9 – Normalized On-Resistance Vs. Temperature

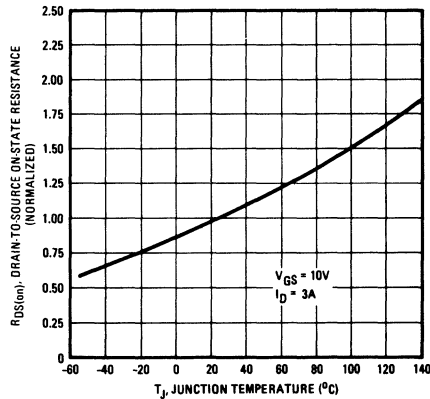


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

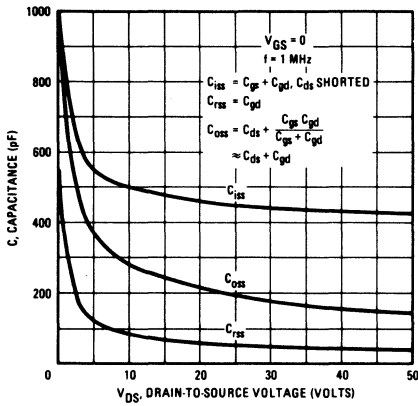


Fig. 11 — Typical Gate Charge vs Gate-to-Source Voltage

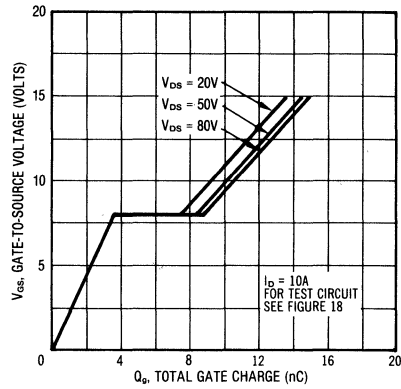


Fig. 12 — Typical On-Resistance Vs. Drain Current

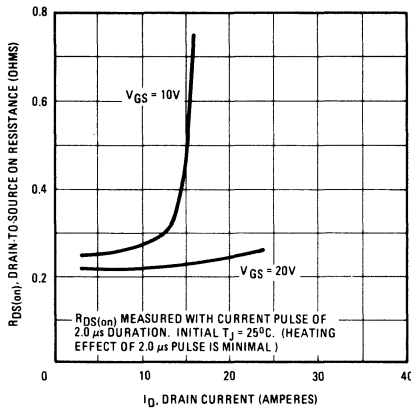


Fig. 13 — Maximum Drain Current vs Case Temperature

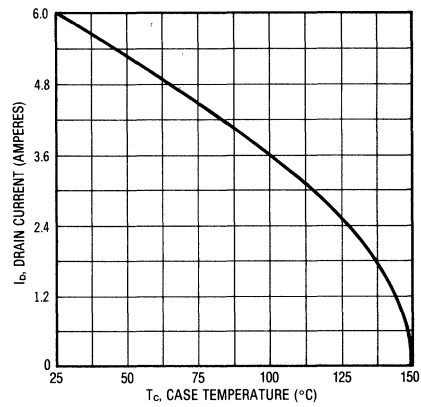


Fig. 14 — Power Vs. Temperature Derating Curve

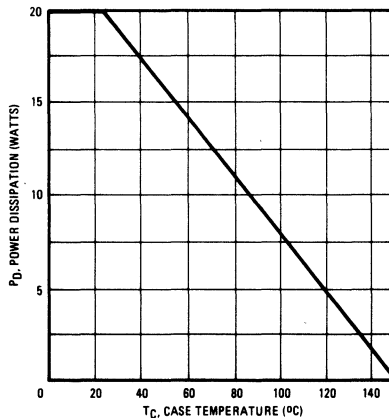


Fig. 15 – Clamped Inductive Test Circuit

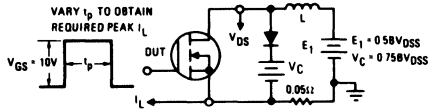


Fig. 16 – Clamped Inductive Waveforms

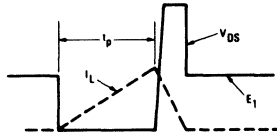


Fig. 17 – Switching Time Test Circuit

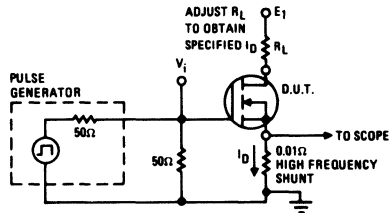
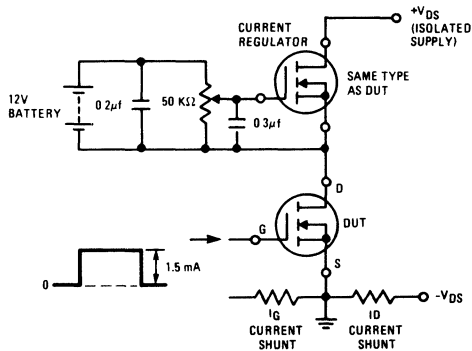


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.80 Ohm
N-Channel

2N6789
2N6790

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

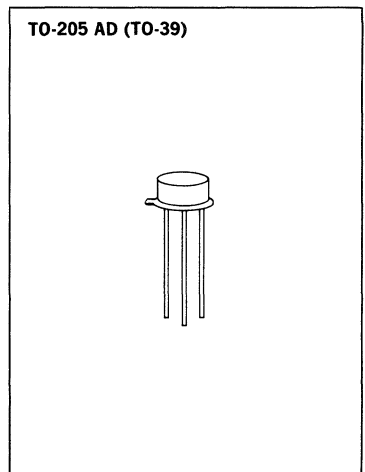
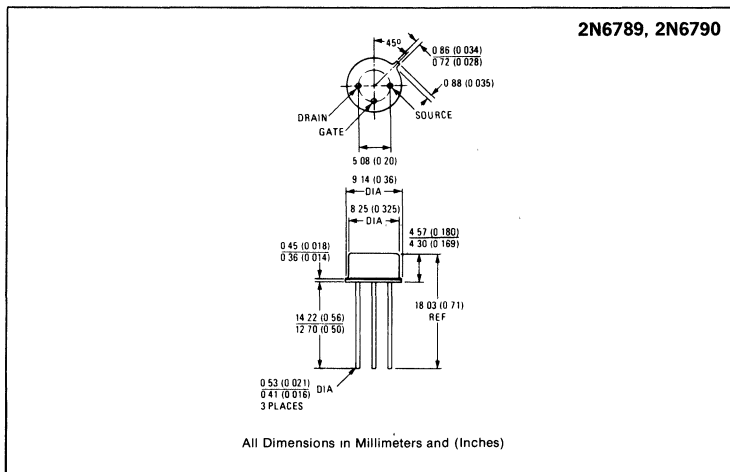
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{ds}	R _{DS(on)}	I _d
2N6789	150V	0.80Ω	3.5A
2N6790	200V	0.80Ω	3.5A

MECHANICAL SPECIFICATIONS

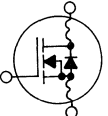


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6789	2N6790		Units
V _{DS} Drain - Source Voltage ①	150*	200*		V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	150*	200*		V
I _D @ T _C = 25°C Continuous Drain Current	3.5*	3.5*		A
I _{DM} Pulsed Drain Current ③	14	14		A
V _{GS} Gate - Source Voltage	±20*			V
P _D @ T _C = 25°C Max. Power Dissipation	20* (See Fig. 14)			W
Linear Derating Factor	0.16* (See Fig. 14)			W/K
I _{LM} Inductive Current, Clamped	14	(See Fig. 15 and 16) L = 100μH 14		A
T _J Operating Junction and Storage Temperature Range	-55 to 150			°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*			°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
B _{VDS} Drain - Source Breakdown Voltage	2N6789	150*	—	—	V	V _{GS} = 0V	
	2N6790	200*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	μA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	3.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.8*	Ω	V _{GS} = 10V, I _D = 2.25A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.5*	Ω	V _{GS} = 10V, I _D = 2.25A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	2.8*	V	V _{GS} = 10V, I _D = 3.5A	
g _{fs} Forward Transconductance ②	ALL	1.5*	—	4.5*	S(Ω)	V _{DS} = 15V, I _D = 2.25A	
C _{iss} Input Capacitance	ALL	200*	—	600*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	60*	—	300*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	15*	—	80*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	40*	ns	V _{DD} = 74V, I _D = 2.25A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	50*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	50*	ns		
t _f Fall Time	ALL	—	—	50*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	5	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	6.25*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	3.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	14	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.7*	—	1.5*	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

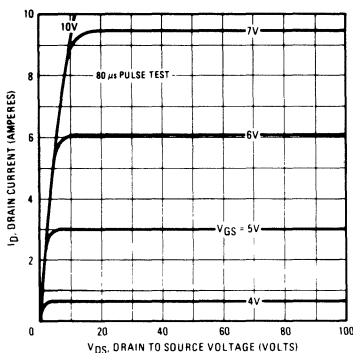


Fig. 2 – Typical Transfer Characteristics

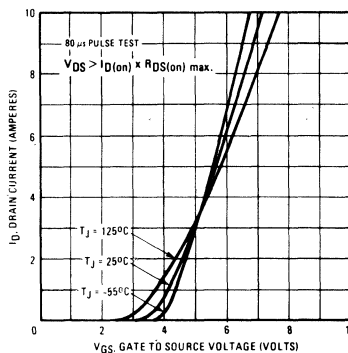


Fig. 3 – Typical Saturation Characteristics

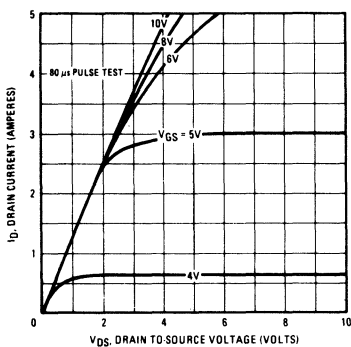


Fig. 4 – Forward Bias Safe Operating Area

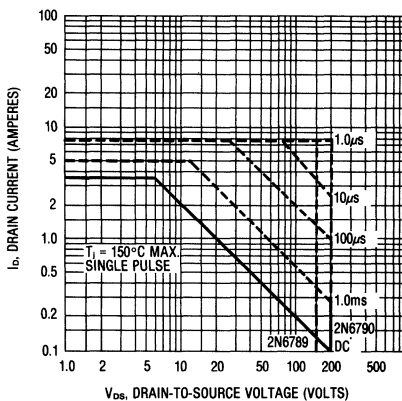
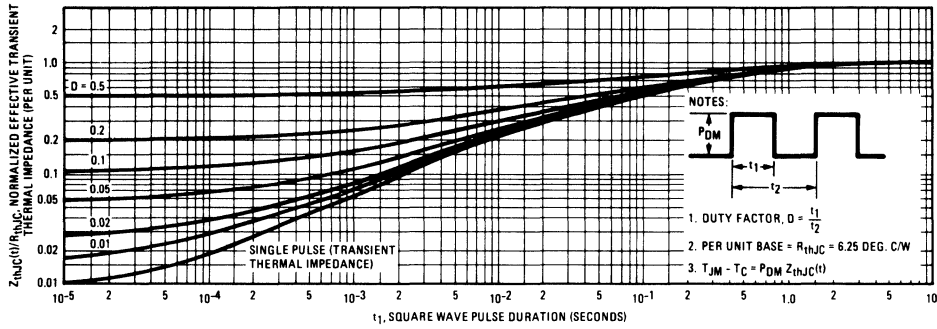


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

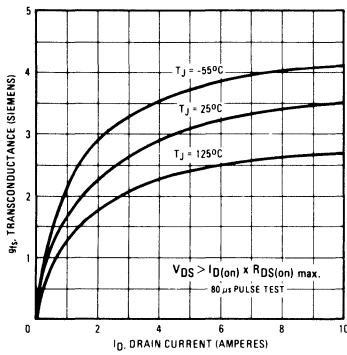


Fig. 7 – Typical Source-Drain Diode Forward Voltage

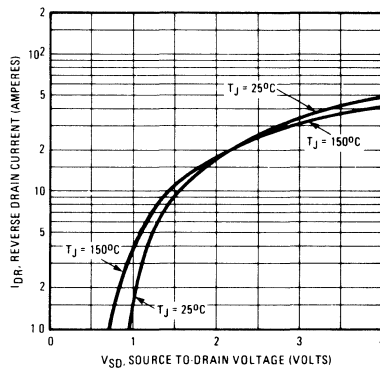


Fig. 8 – Breakdown Voltage Vs. Temperature

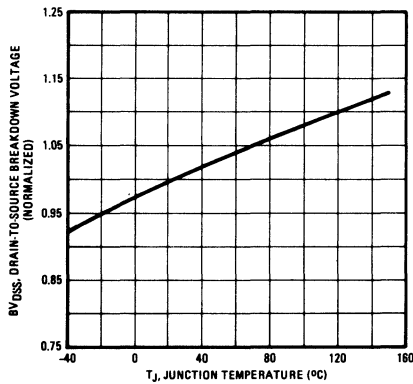


Fig. 9 – Normalized On-Resistance Vs. Temperature

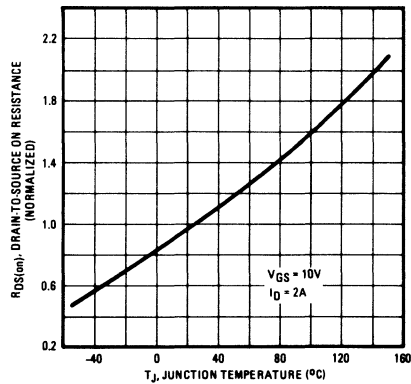


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

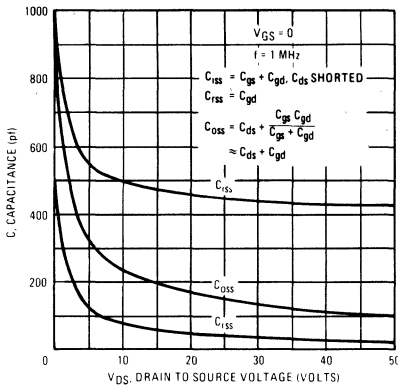


Fig. 12 – Typical On-Resistance Vs. Drain Current

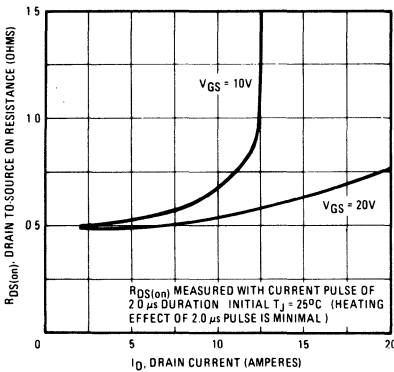


Fig. 11 – Typical Gate Charge vs Gate-to-Source Voltage

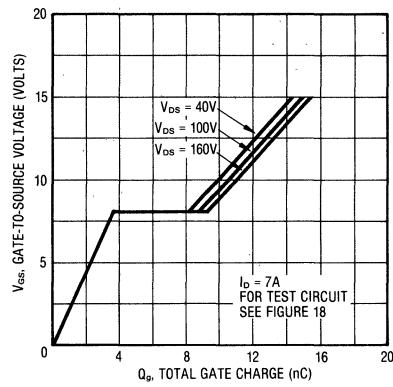


Fig. 13 – Maximum Drain Current vs Case Temperature

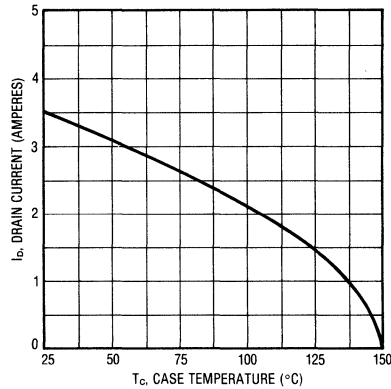


Fig. 14 – Power Vs. Temperature Derating Curve

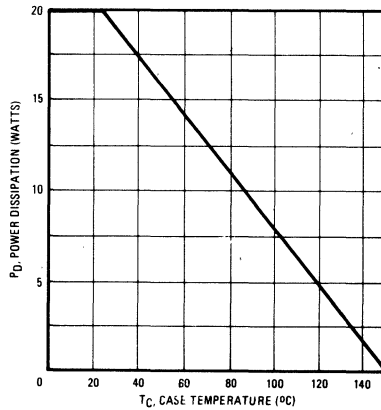


Fig. 15 — Clamped Inductive Test Circuit

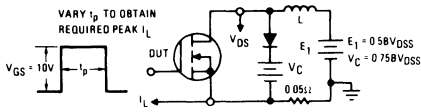


Fig. 16 — Clamped Inductive Waveforms

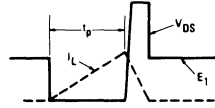


Fig. 17 — Switching Time Test Circuit

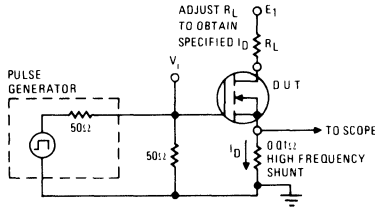
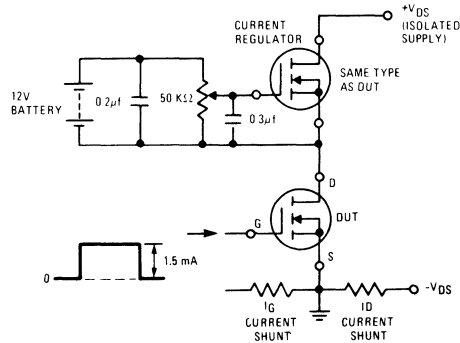


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

2N6791
2N6792

400 Volt, 1.8 Ohm
N-Channel

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

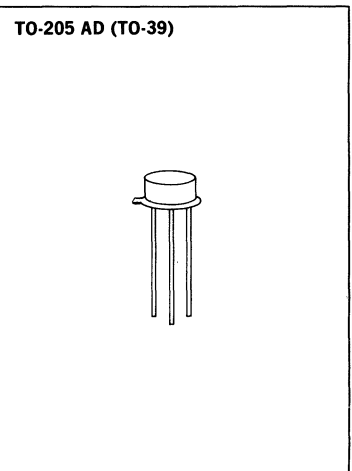
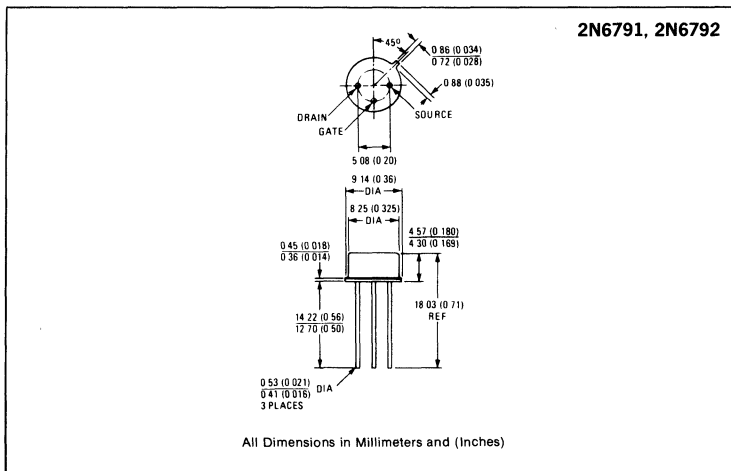
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6791	350V	1.8Ω	2.0A
2N6792	400V	1.8Ω	2.0A

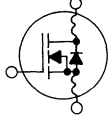
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6791	2N6792		Units
V _{DS} Drain - Source Voltage ①	350*	400*		V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1M Ω) ①	350*	400*		V
I _D @ T _C = 25°C Continuous Drain Current	2.0*	2.0*		A
I _{DM} Pulsed Drain Current ③	10	10		A
V _{GS} Gate - Source Voltage	±20*			V
P _D @ T _C = 25°C Max. Power Dissipation	20* (See Fig. 14)			W
Linear Derating Factor	0.16* (See Fig. 14)			W/K
I _{LM} Inductive Current, Clamped	10	(See Fig. 15 and 16) L = 100 μ H 10		A
T _J Operating Junction and Storage Temperature Range	-55 to 150			°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)			°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6791	350*	—	—	V	V _{GS} = 0V I _D = 1.0mA	
	2N6792	400*	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	μ A	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	2.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.8*	Ω	V _{GS} = 10V, I _D = 1.25A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	4.0*	Ω	V _{GS} = 10V, I _D = 1.25A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	3.6*	V	V _{GS} = 10V, I _D = 2.0A	
g _{fs} Forward Transconductance ②	ALL	1.0*	—	3.0*	S(O)	V _{DS} = 15V, I _D = 1.25A	
C _{iss} Input Capacitance	ALL	200*	—	600*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	40*	—	200*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	5*	—	40*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	40*	ns	V _{DD} = 35V, I _D = 1.25A, Z ₀ = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	35*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	60*	ns		
t _f Fall Time	ALL	—	—	35*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V _{GS} = 10V, I _D = 5.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	6.25*	K/W	Free Air Operation
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	20*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	10	A		
V_{SD}	Diode Forward Voltage ②	ALL	0.6*	—	1.4*	V	$T_C = 25^\circ\text{C}, I_S = 2.0\text{A}, V_{GS} = 0\text{V}$	
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{rr}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

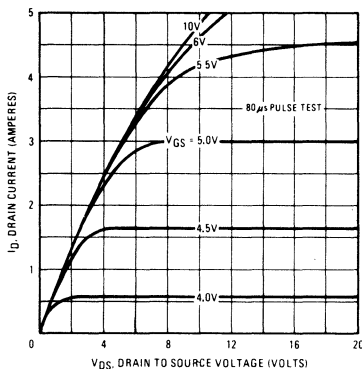


Fig. 2 – Typical Transfer Characteristics

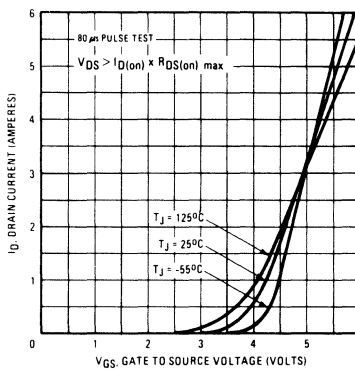


Fig. 3 – Typical Saturation Characteristics

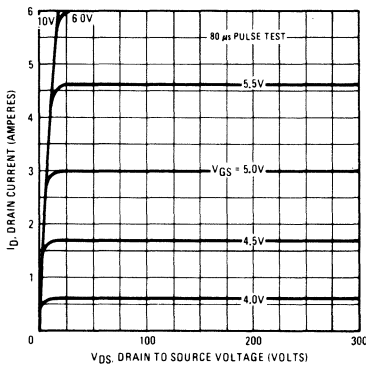


Fig. 4 – Forward Bias Safe Operating Area

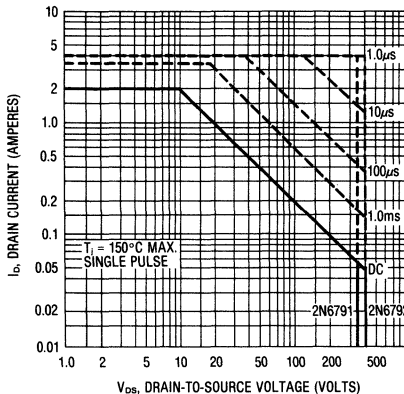


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

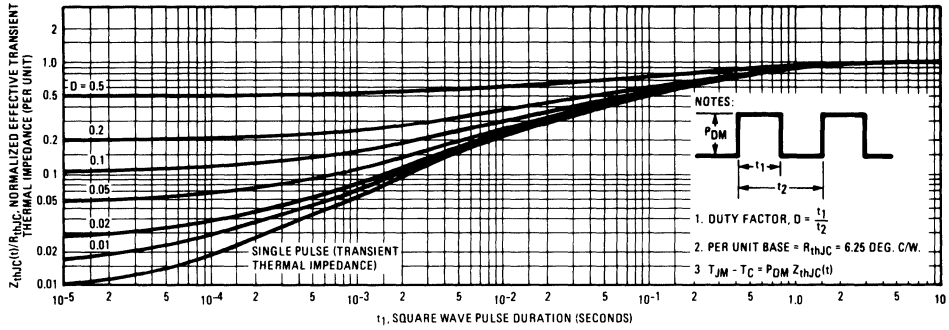


Fig. 6 — Typical Transconductance Vs. Drain Current

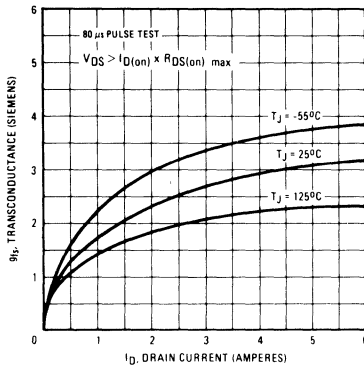


Fig. 8 — Breakdown Voltage Vs. Temperature

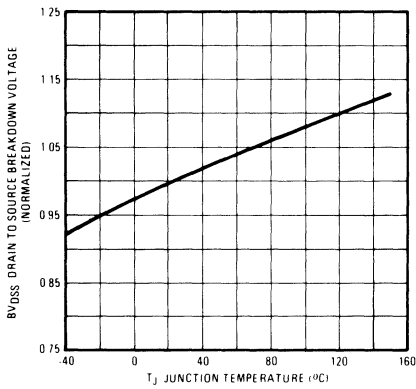


Fig. 7 — Typical Source-Drain Diode Forward Voltage

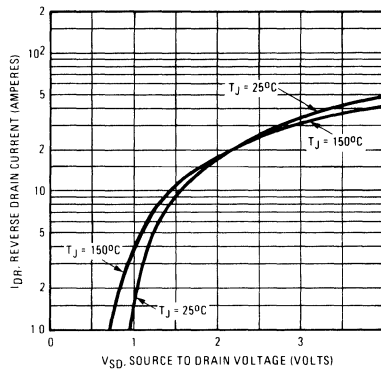


Fig. 9 — Normalized On-Resistance Vs. Temperature

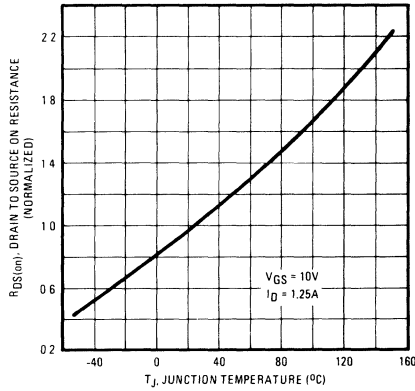


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

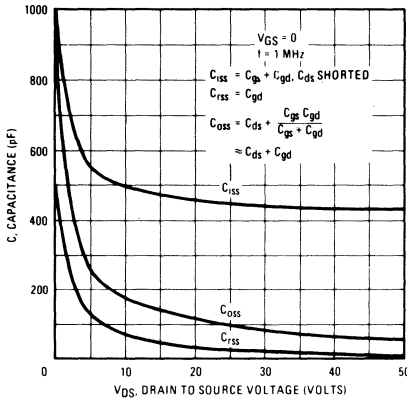


Fig. 12 – Typical On-Resistance Vs. Drain Current

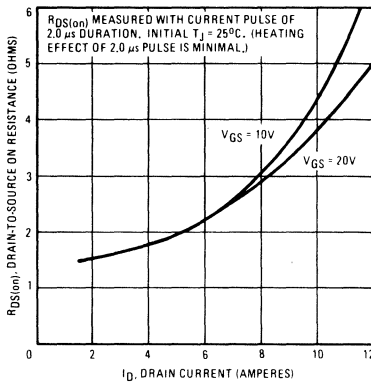


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

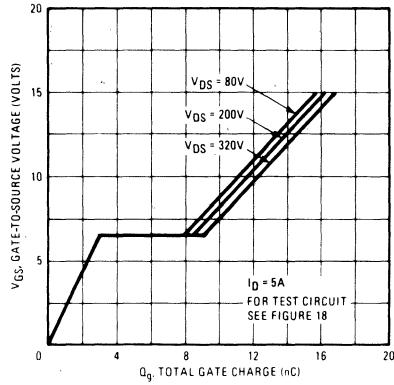


Fig. 13 – Maximum Drain Current Vs. Case Temperature

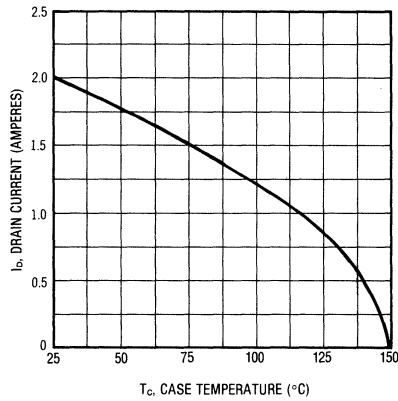


Fig. 14 – Power Vs. Temperature Derating Curve

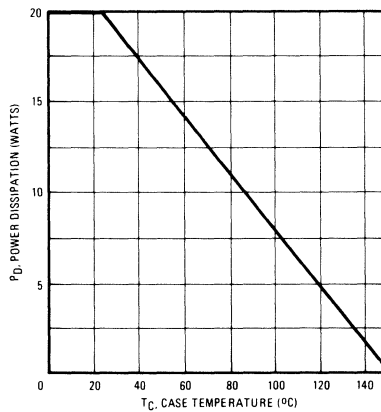


Fig. 15 – Clamped Inductive Test Circuit

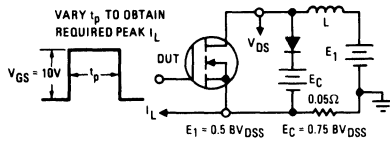


Fig. 16 – Clamped Inductive Waveforms

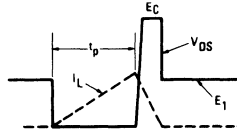


Fig. 17 – Switching Time Test Circuit

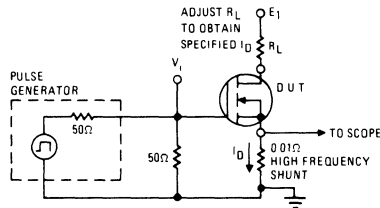
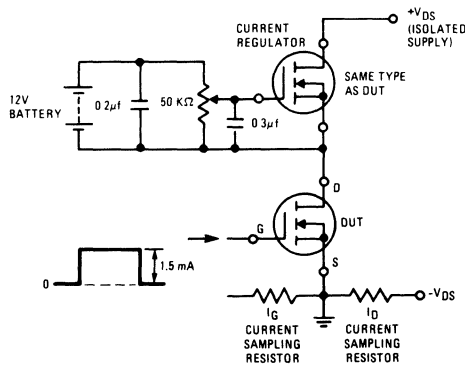


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

2N6793
2N6794

500 Volt, 3.0 Ohm
N-Channel

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

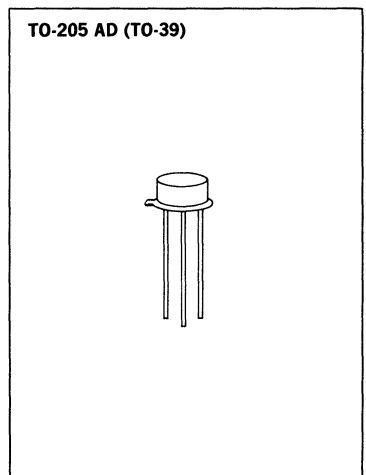
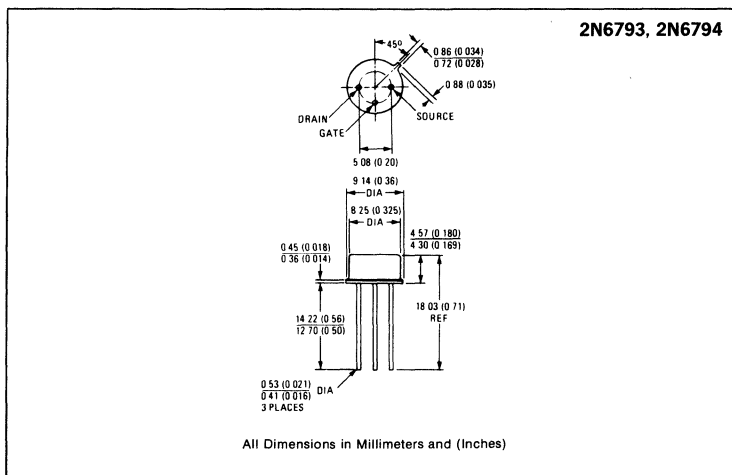
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6793	450V	3.0Ω	1.5A
2N6794	500V	3.0Ω	1.5A

MECHANICAL SPECIFICATIONS

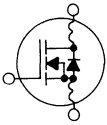


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6793	2N6794	Units
V _{DS} Drain - Source Voltage ①	450*	500*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	450*	500*	V
I _D @ T _C = 25°C Continuous Drain Current	1.5*	1.5*	A
I _{DM} Pulsed Drain Current ③	6.5	6.5	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	20* (See Fig. 14)		W
Linear Derating Factor	0.16* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	6.5	(See Fig. 15 and 16) L = 100μH 6.5	A
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		°C

4

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6793	450*	—	—	V	V _{GS} = 0V	
	2N6794	500*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	1.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	3.0*	Ω	V _{GS} = 10V, I _D = 1.0A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	6.6*	Ω	V _{GS} = 10V, I _D = 1.0A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	4.5*	V	V _{GS} = 10V, I _D = 1.5A	
g _{fs} Forward Transconductance ②	ALL	1.0*	—	3.0*	S(Ω)	V _{DS} = 15V, I _D = 1.0A	
C _{iss} Input Capacitance	ALL	200*	—	600*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	30*	—	150*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	5*	—	40*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	40*	ns	V _{DD} = 225V, I _D = 1.0A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	30*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	60*	ns		
t _f Fall Time	ALL	—	—	30*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V _{GS} = 10V, I _D = 3.0A, V _{DS} = 0.8 Max. Rating, See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature)	
Q _{gs} Gate-Source Charge	ALL	—	5	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

Parameter	Type	Min.	Typ.	Max.	Units	Notes
R _{thJC} Junction-to-Case	ALL	—	—	6.25*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	1.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	6.5	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.6*	—	1.2*	V	$T_C = 25^\circ\text{C}$, $I_S = 1.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 1.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	3.5	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 1.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$.
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values

Fig. 1 – Typical Output Characteristics

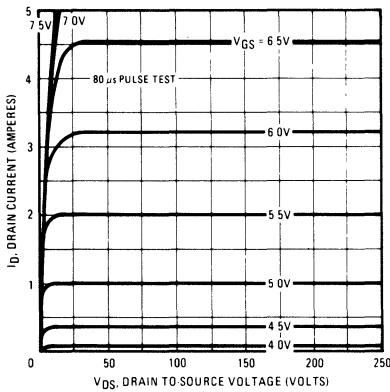


Fig. 2 – Typical Transfer Characteristics

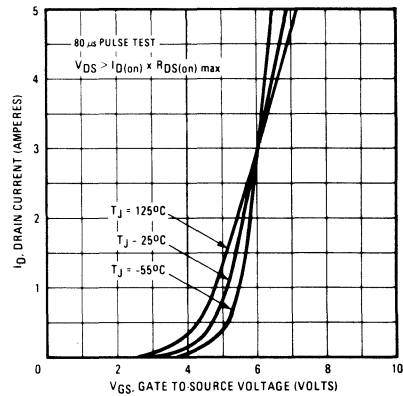


Fig. 3 – Typical Saturation Characteristics

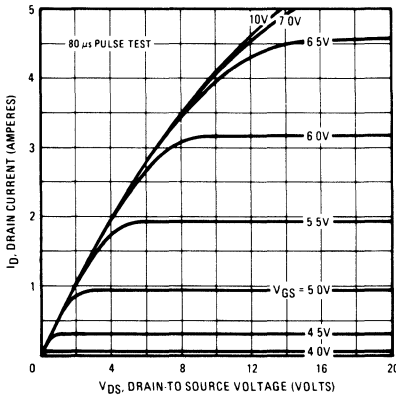


Fig. 4 – Forward Bias Safe Operating Area

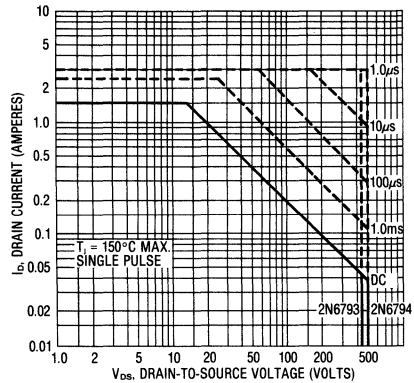


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

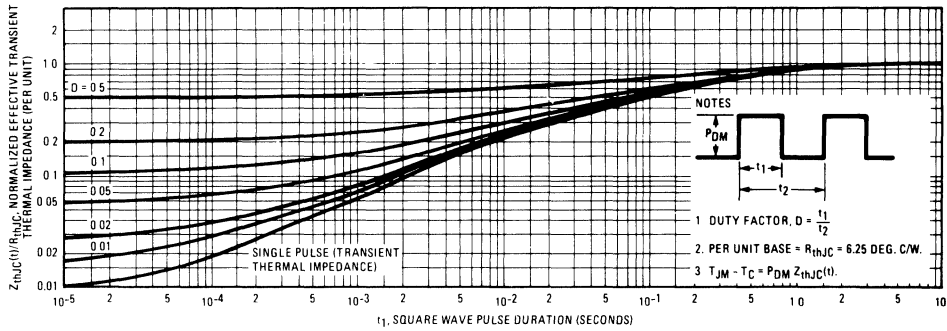


Fig. 6 – Typical Transconductance Vs. Drain Current

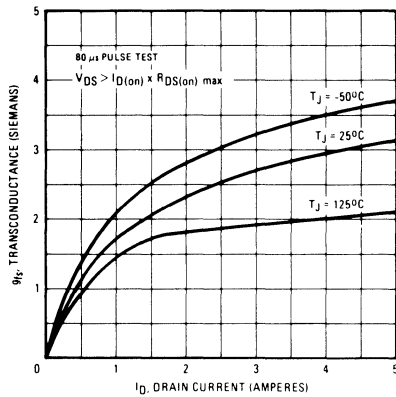


Fig. 7 – Typical Source-Drain Diode Forward Voltage

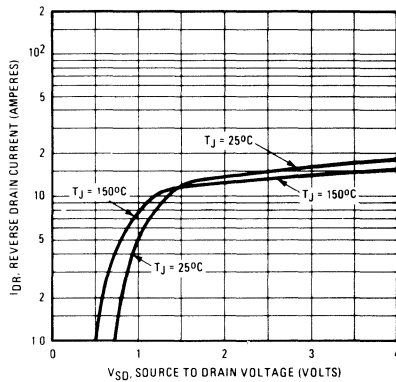


Fig. 8 – Breakdown Voltage Vs. Temperature

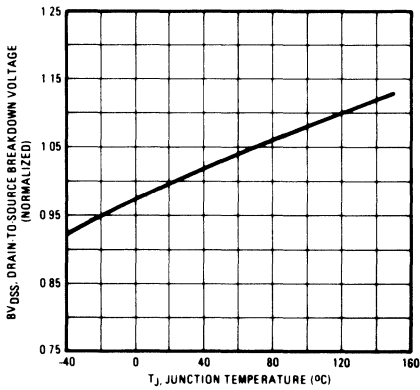


Fig. 9 – Normalized On-Resistance Vs. Temperature

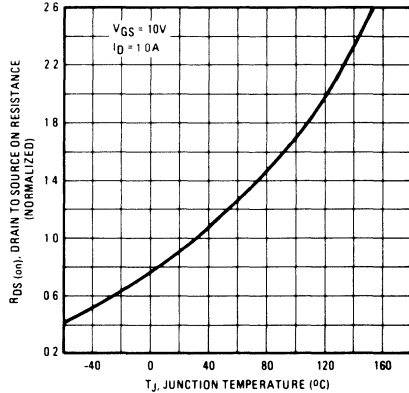


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

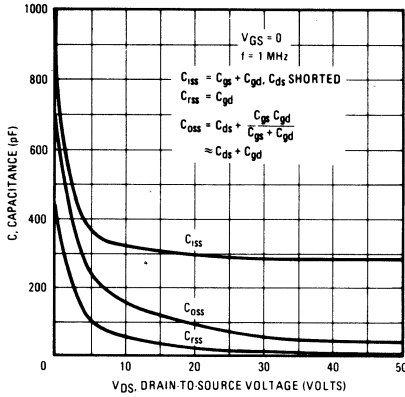


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

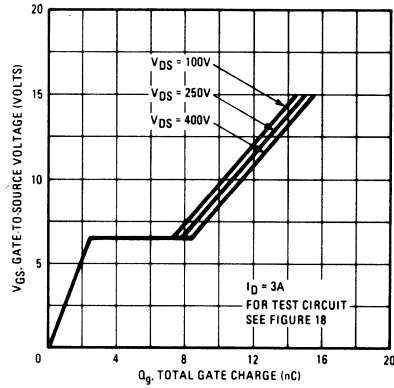


Fig. 12 – Typical On-Resistance Vs. Drain Current

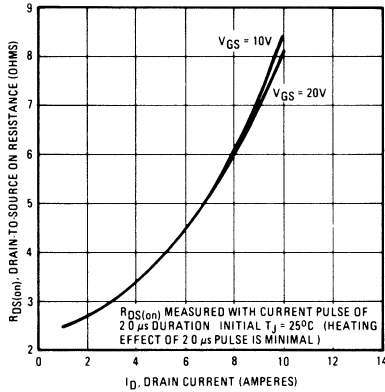


Fig. 13 – Maximum Drain Current Vs. Case Temperature

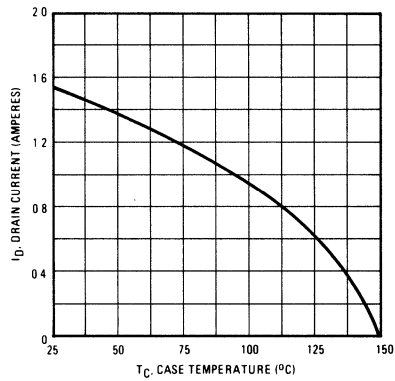


Fig. 14 – Power Vs. Temperature Derating Curve

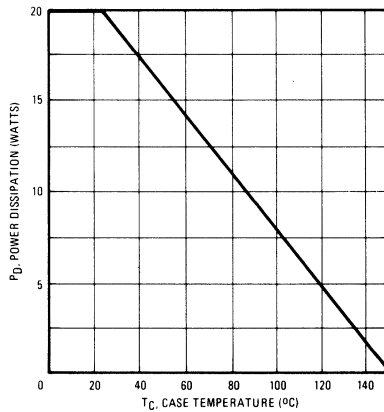


Fig. 15 – Clamped Inductive Test Circuit

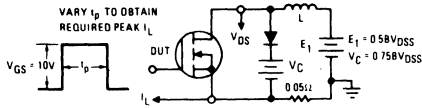


Fig. 16 – Clamped Inductive Waveforms

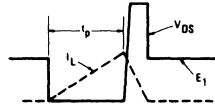


Fig. 17 – Switching Time Test Circuit

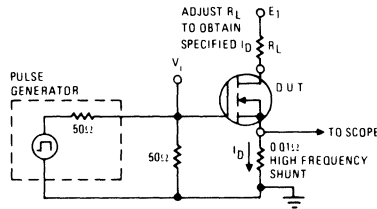
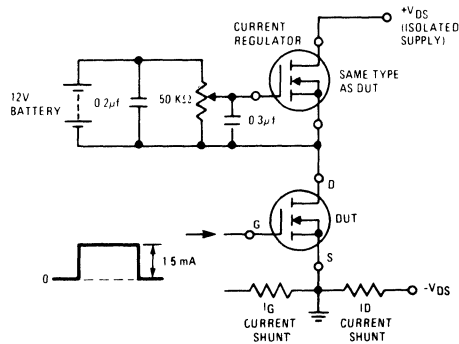


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

2N6795
2N6796

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

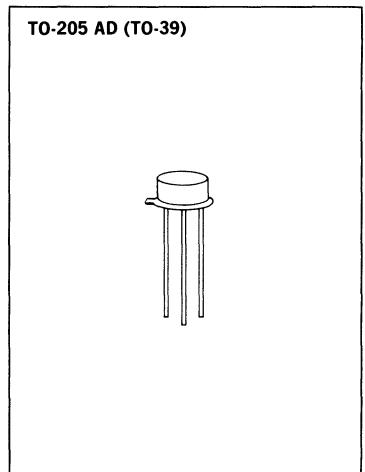
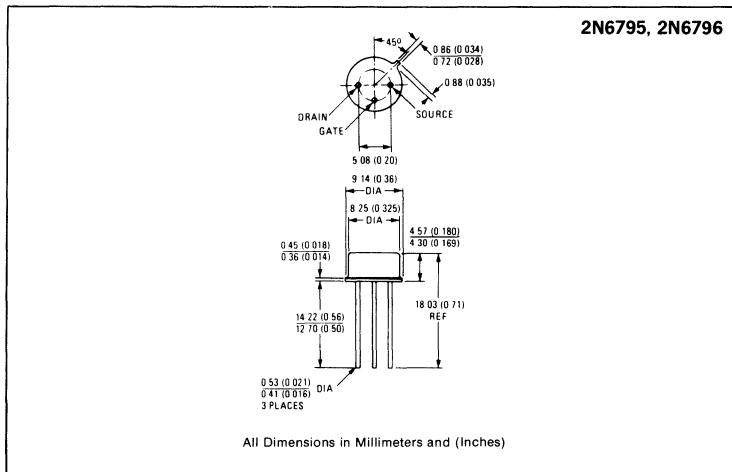
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6795	60V	0.18Ω	8.0A
2N6796	100V	0.18Ω	8.0A

MECHANICAL SPECIFICATIONS

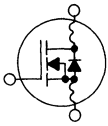


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6795	2N6796	Units
V _{DS} Drain - Source Voltage ①	60*	100*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	60*	100*	V
I _D @ T _C = 25°C Continuous Drain Current	8.0*	8.0*	A
I _{DM} Pulsed Drain Current ③	32	32	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	25* (See Fig. 14)		W
Linear Derating Factor	0.2* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	32	(See Fig. 15 and 16) L = 100μH 32	A
T _J Operating Junction and T _{stg} Storage Temperature Range	-55 to 150		°C
Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		°C

4

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6795	60*	—	—	V	V _{GS} = 0V	
	2N6796	100*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	8.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.18*	Ω	V _{GS} = 10V, I _D = 5.0A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.35*	Ω	V _{GS} = 10V, I _D = 5.0A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	1.56*	V	V _{GS} = 10V, I _D = 8.0A	
g _{fs} Forward Transconductance ②	ALL	3.0*	—	9.0*	S(Ω)	V _{DS} = 15V, I _D = 5.0A	
C _{iss} Input Capacitance	ALL	350*	—	900*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	150*	—	500*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	50*	—	150*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30*	ns		V _{DD} = 30V, I _D = 5.0A, Z _o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
T _r Rise Time	ALL	—	—	75*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	40*	ns		
t _f Fall Time	ALL	—	—	45*	ns	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating, See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC		
Q _{gs} Gate-Source Charge	ALL	—	9	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	5.0*	K/W	Free Air Operation
R _{thJA} Junction-to Ambient	ALL	—	—	175	K/W	

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	8*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.75*	—	1.5*	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	1.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 — Typical Output Characteristics

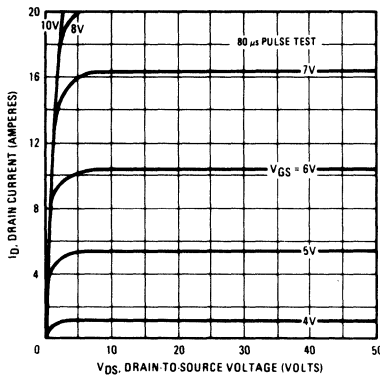


Fig. 2 — Typical Transfer Characteristics

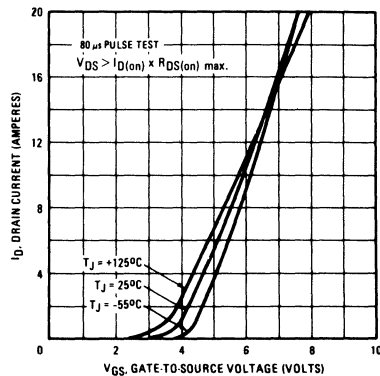


Fig. 3 — Typical Saturation Characteristics

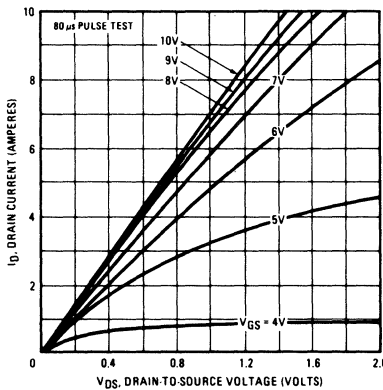


Fig. 4 — Forward Bias Safe Operating Area

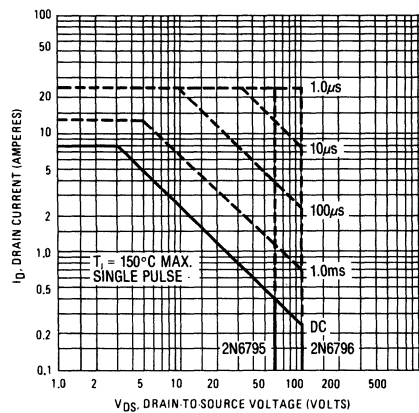


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

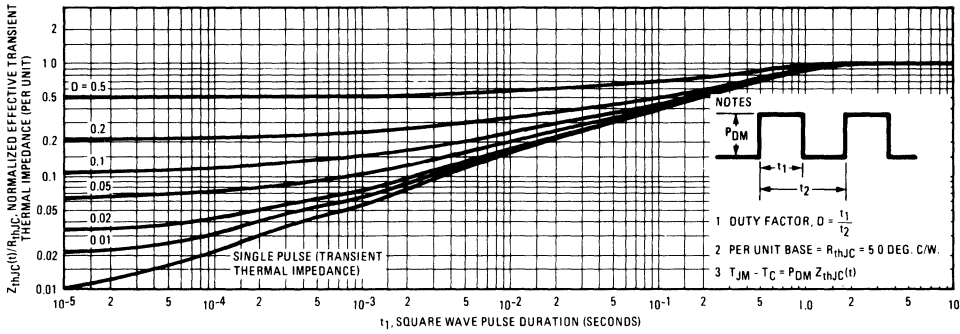


Fig. 6 – Typical Transconductance Vs. Drain Current

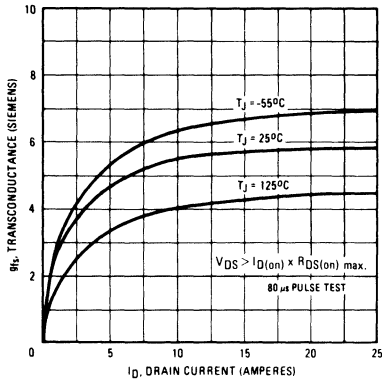


Fig. 7 – Typical Source-Drain Diode Forward Voltage

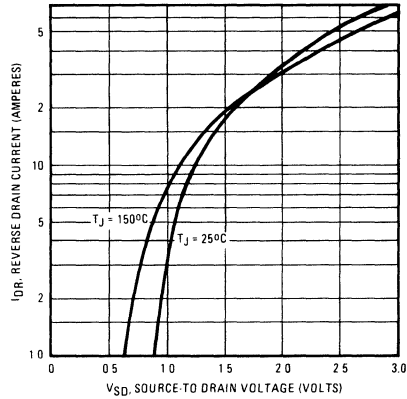


Fig. 8 – Breakdown Voltage Vs. Temperature

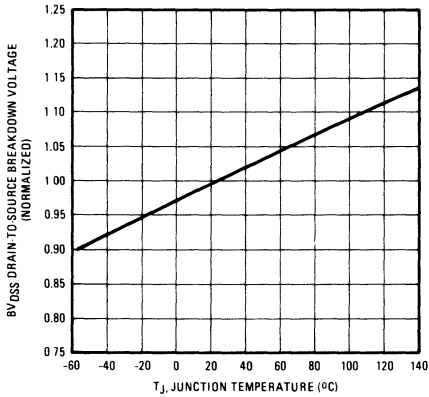


Fig. 9 – Normalized On-Resistance Vs. Temperature

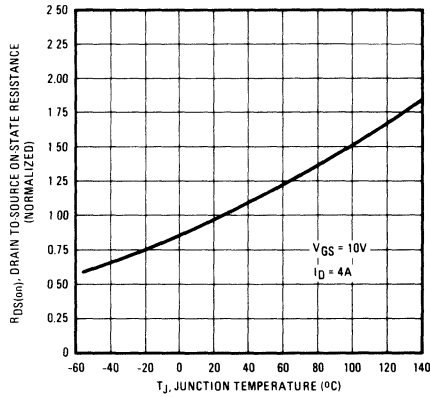


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

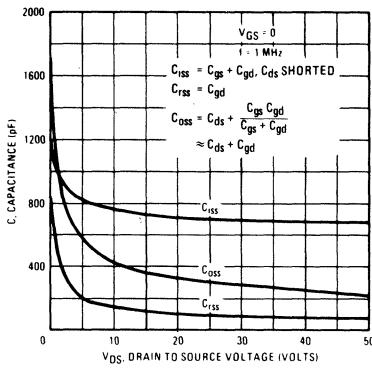


Fig. 12 – Typical On-Resistance Vs. Drain Current

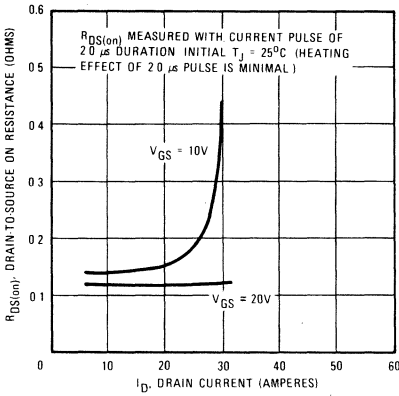


Fig. 14 – Power Vs. Temperature Derating Curve

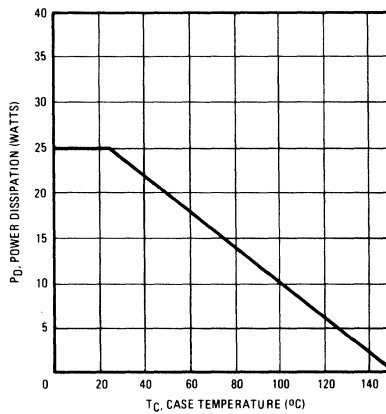


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

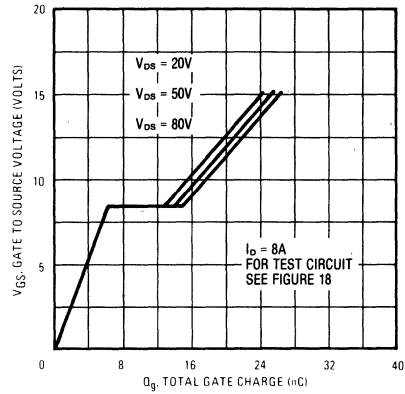


Fig. 13 – Maximum Drain Current Vs. Case Temperature

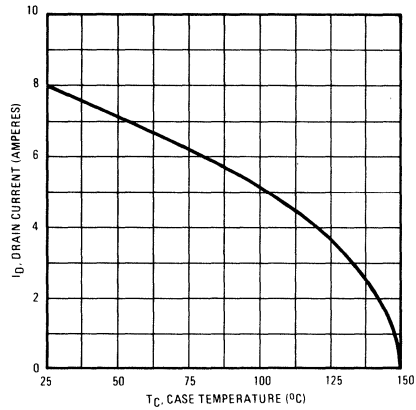


Fig. 15 – Clamped Inductive Test Circuit

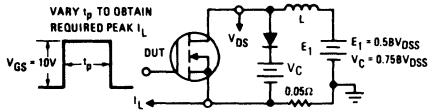


Fig. 16 – Clamped Inductive Waveforms

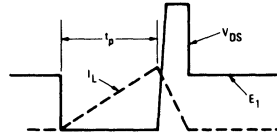


Fig. 17 – Switching Time Test Circuit

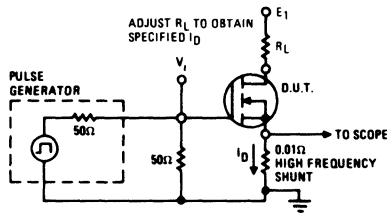
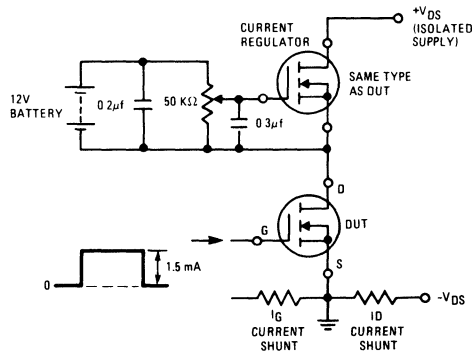


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm
N-Channel

2N6797
2N6798

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

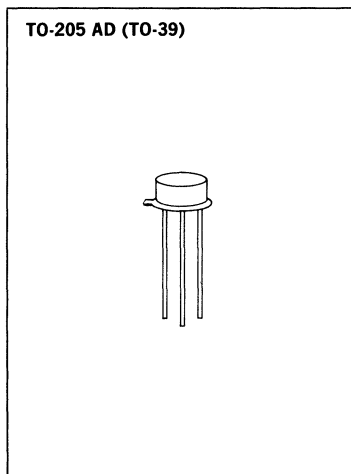
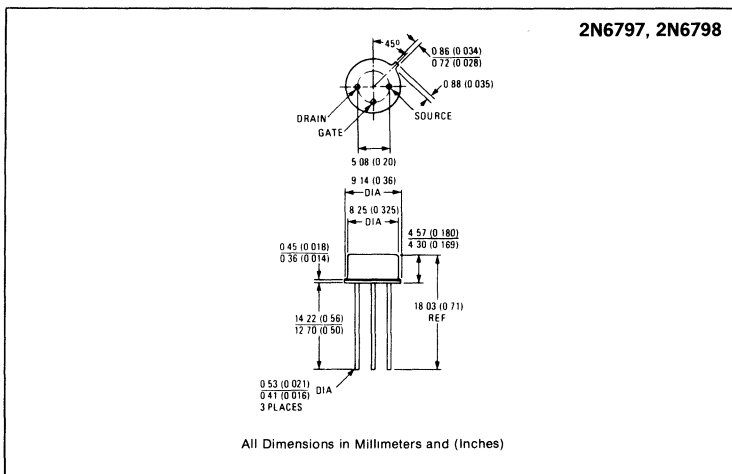
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6797	150V	0.4Ω	5.5A
2N6798	200V	0.4Ω	5.5A

MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	2N6797	2N6798	Units
V _{DS} Drain - Source Voltage ①	150*	200*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	150*	200*	V
I _D @ T _C = 25°C Continuous Drain Current	5.5*	5.5*	A
I _{DM} Pulsed Drain Current ③	22	22	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	25* (See Fig. 14)		W
Linear Derating Factor	0.2* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22		A
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)		°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6797	150*	—	—	V	V _{GS} = 0V I _D = 1.0mA	
	2N6798	200*	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
		—	—	4.0*	mA		
I _{D(on)} On-State Drain Current ②	ALL	5.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.4*	Ω	V _{GS} = 10V, I _D = 3.5A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	0.75*	Ω	V _{GS} = 10V, I _D = 3.5A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	2.2*	V	V _{GS} = 10V, I _D = 5.5A	
g _{fs} Forward Transconductance ②	ALL	2.5*	—	7.5*	S(Ω)	V _{DS} = 15V, I _D = 3.5A	
C _{iss} Input Capacitance	ALL	350*	—	900*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	100*	—	450*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	40*	—	150*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30*	ns	V _{DD} = 77V, I _D = 3.5A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	50*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	50*	ns		
t _f Fall Time	ALL	—	—	40*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	V _{GS} = 10V, I _D = 11A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	10	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances.
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	5.0*	K/W	Free Air Operation
R _{thJA} Junction-to Ambient	ALL	—	—	175	K/W	

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	5.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	22	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.75*	—	1.5*	V	$T_C = 25^\circ\text{C}$, $I_S = 5.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 5.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 5.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 — Typical Output Characteristics

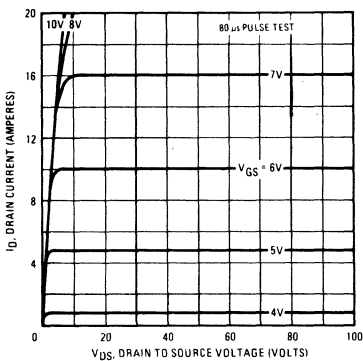


Fig. 2 — Typical Transfer Characteristics

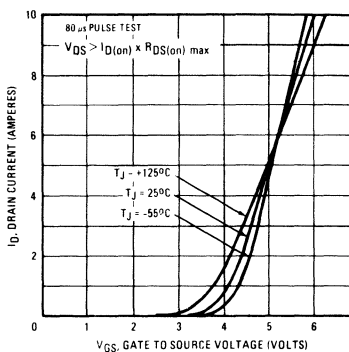


Fig. 3 — Typical Saturation Characteristics

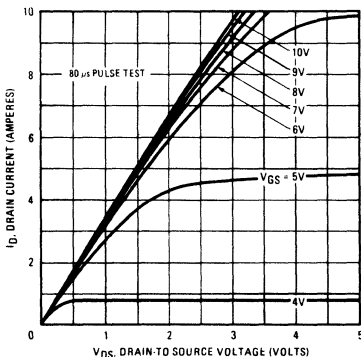


Fig. 4 — Forward Bias Safe Operating Area

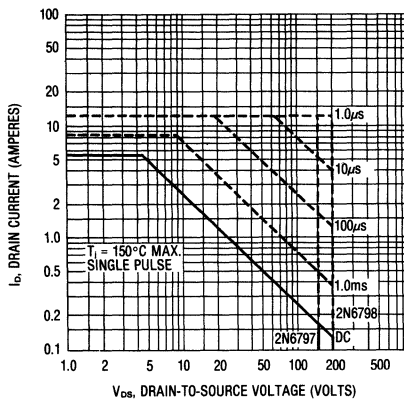


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

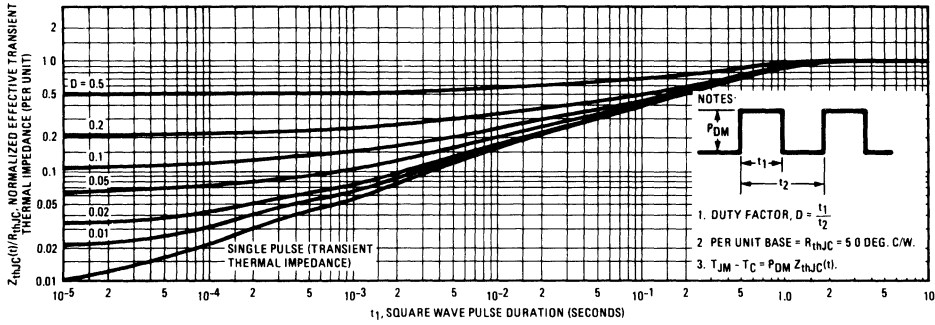


Fig. 6 – Typical Transconductance Vs. Drain Current

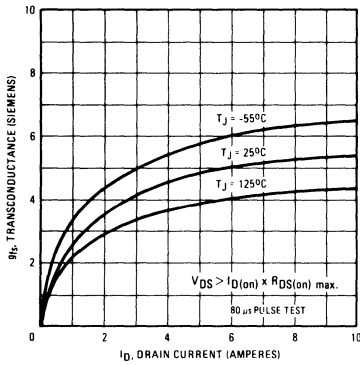


Fig. 7 – Typical Source-Drain Diode Forward Voltage

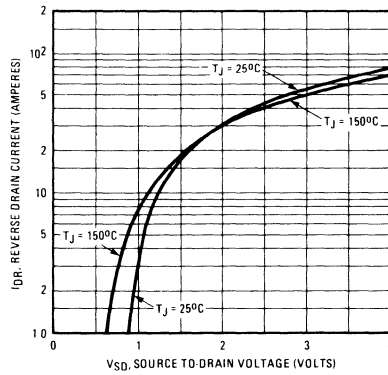


Fig. 8 – Breakdown Voltage Vs. Temperature

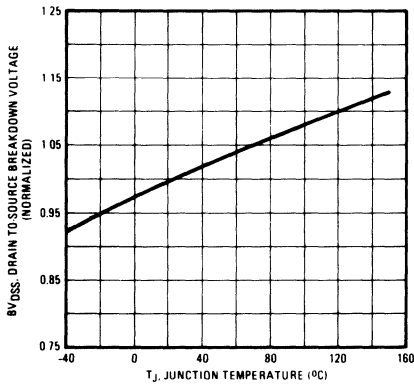


Fig. 9 – Normalized On-Resistance Vs. Temperature

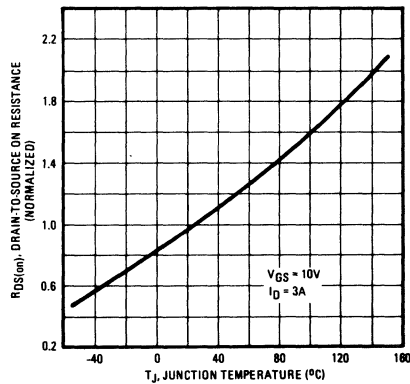


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

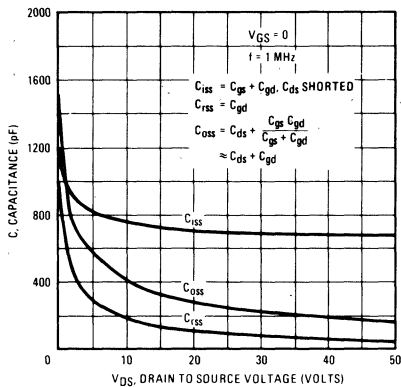


Fig. 12 — Typical On-Resistance Vs. Drain Current

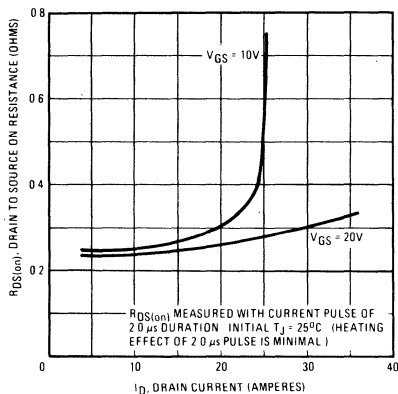


Fig. 11 — Typical Gate Charge vs Gate-to-Source Voltage

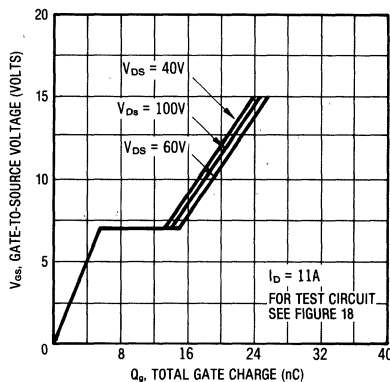


Fig. 13 — Maximum Drain Current vs Case Temperature

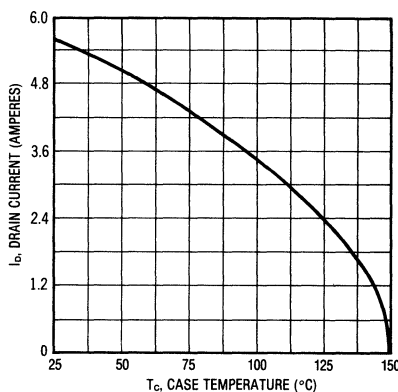


Fig. 14 — Power Vs. Temperature Derating Curve

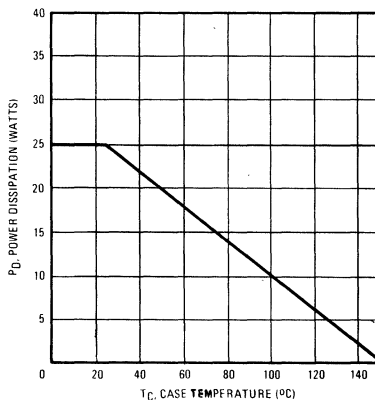


Fig. 15 - Clamped Inductive Test Circuit

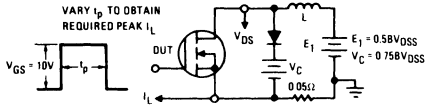
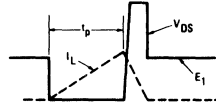


Fig. 16 - Clamped Inductive Waveforms



4

Fig. 17 - Switching Time Test Circuit

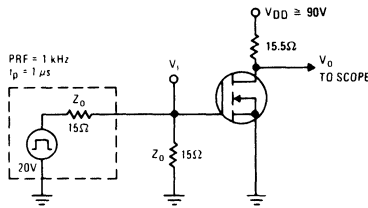
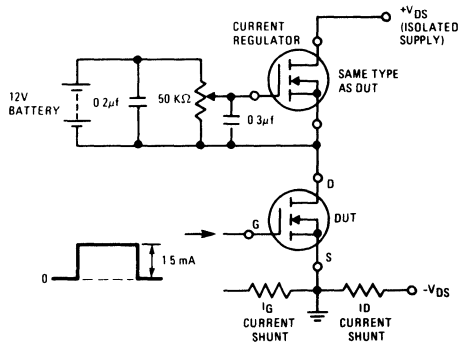


Fig. 18 - Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm
N-Channel

2N6799
2N6800

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

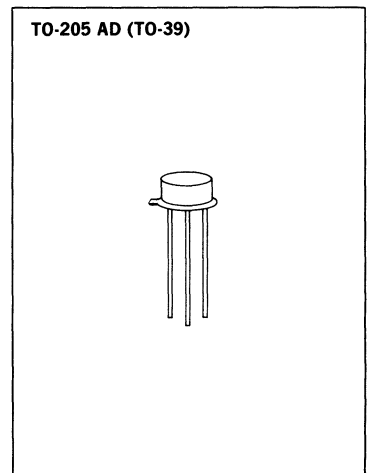
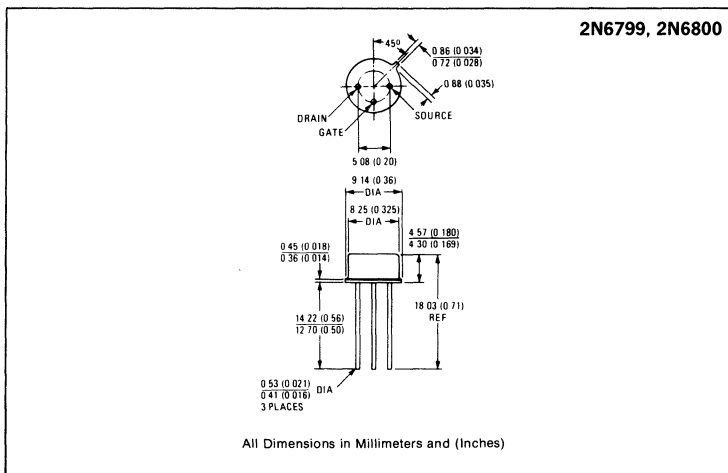
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _D
2N6799	350V	1.0Ω	3.0A
2N6800	400V	1.0Ω	3.0A

MECHANICAL SPECIFICATIONS

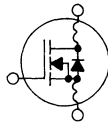


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6799	2N6800	Units
V _{DS} Drain - Source Voltage ①	350*	400*	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1M Ω) ①	350*	400*	V
I _D @ T _C = 25°C Continuous Drain Current	3.0*	3.0*	A
I _{DM} Pulsed Drain Current ③	14	14	A
V _{GS} Gate - Source Voltage	±20*		V
P _D @ T _C = 25°C Max. Power Dissipation	25* (See Fig. 14)		W
Linear Derating Factor	0.20* (See Fig. 14)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100 μ H		A
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)*		°C

4

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6799	350*	—	—	V	V _{GS} = 0V	
	2N6800	400*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	3.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.0*	Ω	V _{GS} = 10V, I _D = 2.0A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	2.4*	Ω	V _{GS} = 10V, I _D = 2.0A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	3.0*	V	V _{GS} = 10V, I _D = 3.0A	
g _{fs} Forward Transconductance ②	ALL	2.0*	—	6.0*	S(Ω)	V _{DS} = 15V, I _D = 2.0A	
C _{iss} Input Capacitance	ALL	350*	—	900*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	50*	—	300*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	20*	—	80*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30*	ns	V _{DD} = 176V, I _D = 2.0A, Z _o = 15 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	35*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	55*	ns		
t _f Fall Time	ALL	—	—	35*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 6.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	11	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	7	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	5.0*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	3.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	14	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.7*	—	1.4*	V	$T_C = 25^\circ\text{C}, I_S = 3.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

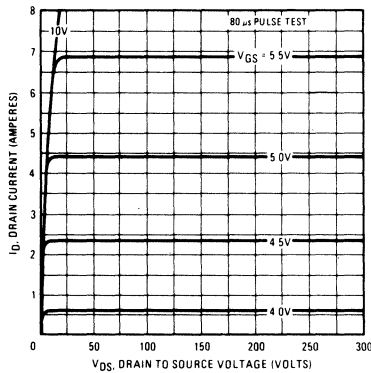


Fig. 2 – Typical Transfer Characteristics

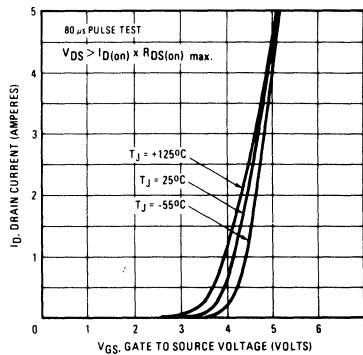


Fig. 3 – Typical Saturation Characteristics

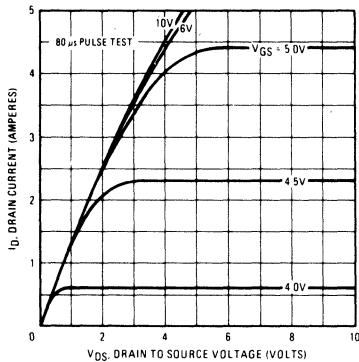


Fig. 4 – Forward Bias Safe Operating Area

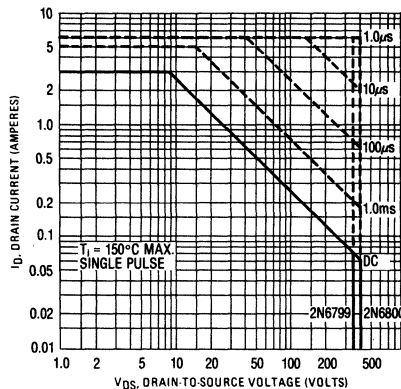
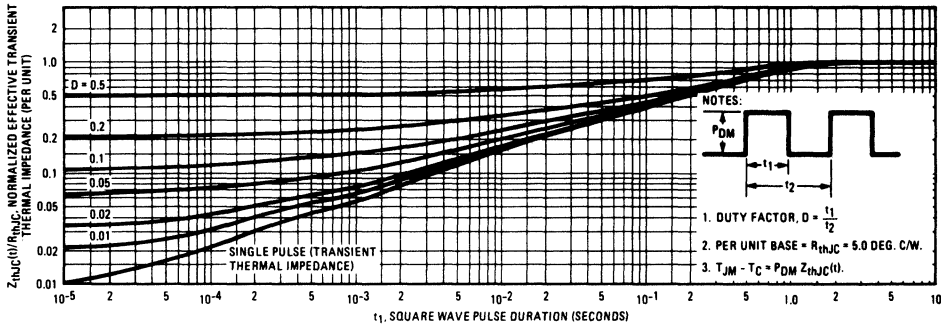


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

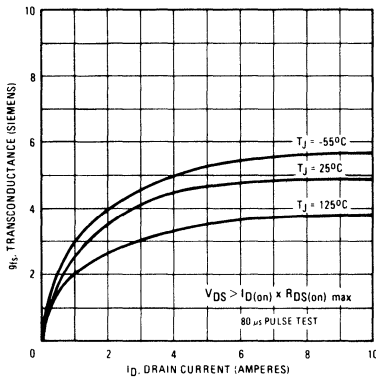


Fig. 7 – Typical Source-Drain Diode Forward Voltage

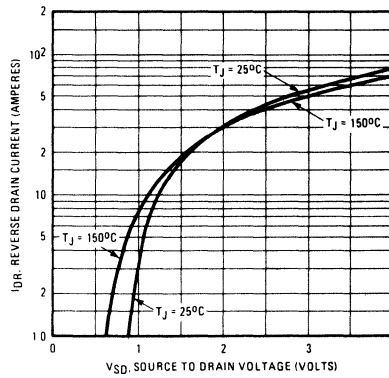


Fig. 8 – Breakdown Voltage Vs. Temperature

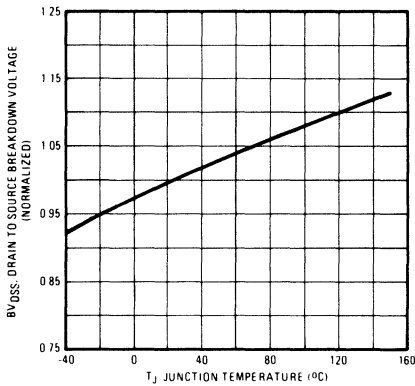


Fig. 9 – Normalized On-Resistance Vs. Temperature

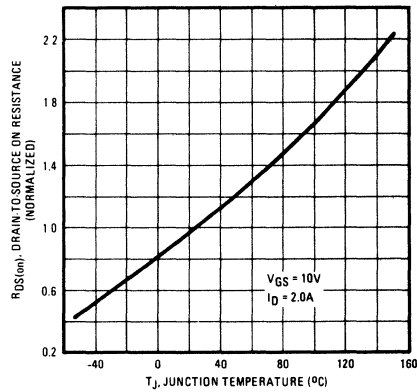


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

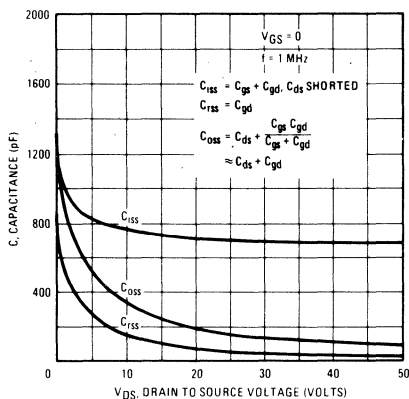


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

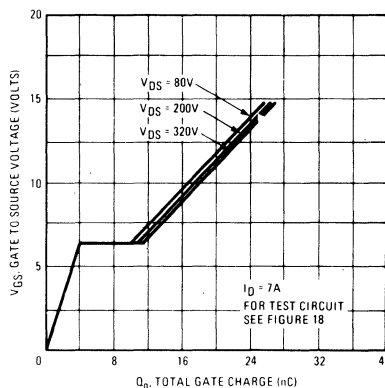


Fig. 12 – Typical On-Resistance Vs. Drain Current

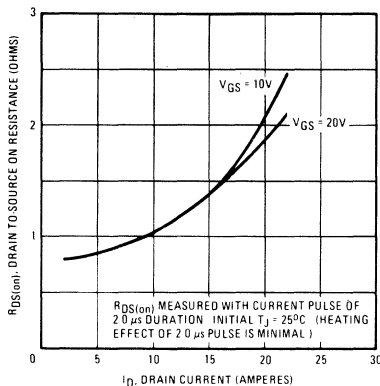


Fig. 13 – Maximum Drain Current Vs. Case Temperature

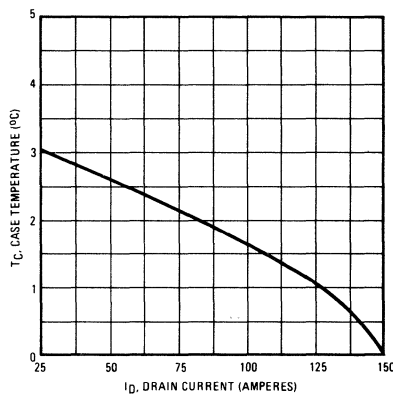


Fig. 14 – Power Vs. Temperature Derating Curve

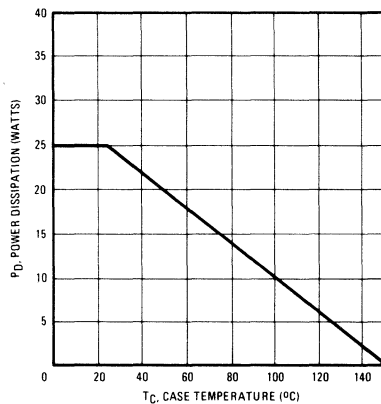


Fig. 15 — Clamped Inductive Test Circuit

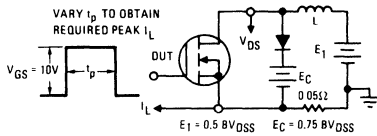


Fig. 16 — Clamped Inductive Waveforms

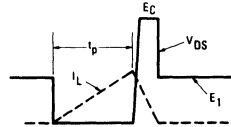


Fig. 17 — Switching Time Test Circuit

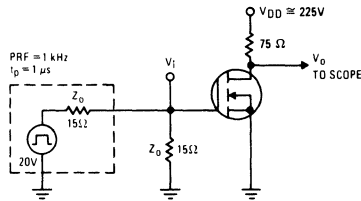
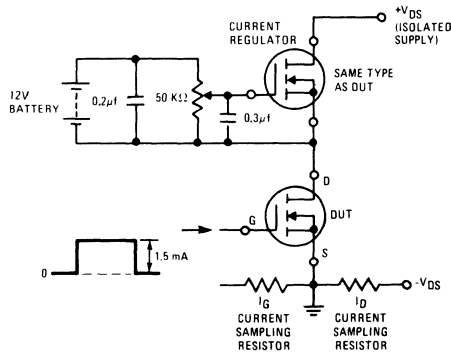


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

2N6801
2N6802

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

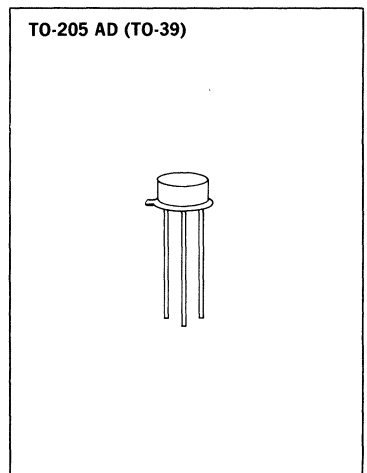
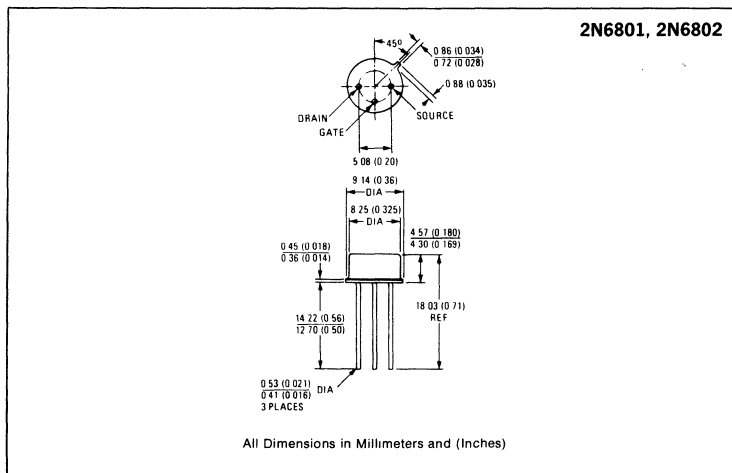
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6801	450V	1.5Ω	2.5A
2N6802	500V	1.5Ω	2.5A

MECHANICAL SPECIFICATIONS

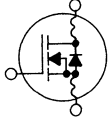


ABSOLUTE MAXIMUM RATINGS

Parameter	2N6801	2N6802		Units
V _{DS} Drain - Source Voltage ①	450*	500*		V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1MΩ) ①	450*	500*		V
I _D @ T _C = 25°C Continuous Drain Current	2.5*	2.5*		A
I _{DM} Pulsed Drain Current ③	11	11		A
V _{GS} Gate - Source Voltage			±20*	V
P _D @ T _C = 25°C Max. Power Dissipation			25* (See Fig. 14)	W
			0.20* (See Fig. 14)	W/K
I _{LM} Inductive Current, Clamped	11	11	(See Fig. 15 and 16) L = 100μH	A
T _J Operating Junction and Storage Temperature Range			-55 to 150	°C
T _{stg} Lead Temperature			300(0.063 in. (1.6mm) from case for 10s)*	°C

4


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	2N6801	450*	—	—	V	V _{GS} = 0V	
	2N6802	500*	—	—	V	I _D = 1.0mA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V _{DS} = V _{GS} , I _D = 1.0mA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100*	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	4.0*	mA	V _{DS} = Max. Rating, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	ALL	2.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	1.5*	Ω	V _{GS} = 10V, I _D = 1.5A, T _C = 25°C	
R _{DS(on)} Static Drain-Source On-State Resistance ②	ALL	—	—	3.5*	Ω	V _{GS} = 10V, I _D = 1.5A, T _C = 125°C	
V _{DS(on)} On-State Drain-Source Voltage ②	ALL	—	—	3.75*	V	V _{GS} = 10V, I _D = 2.5A	
g _{fs} Forward Transconductance ②	ALL	1.5*	—	4.5*	S(Ω)	V _{DS} = 15V, I _D = 1.5A	
C _{iss} Input Capacitance	ALL	350*	—	900*	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	25*	—	200*	pF		
C _{rss} Reverse Transfer Capacitance	ALL	15*	—	60*	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30*	ns	V _{DD} = 225V, I _D = 1.5A, Z _θ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
T _r Rise Time	ALL	—	—	30*	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	55*	ns		
t _f Fall Time	ALL	—	—	30*	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	30	nC	V _{GS} = 10V, I _D = 6.0A, V _{DS} = 0.8 Max. Rating, See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	11	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	11	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	5.0*	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

I_S	Continuous Source Current (Body Diode)	ALL	—	—	2.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	11	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.7*	—	1.4*	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovered Charge	ALL	—	4.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

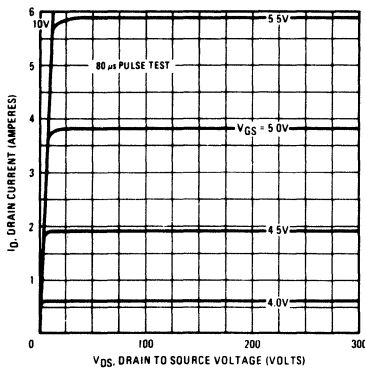


Fig. 2 – Typical Transfer Characteristics

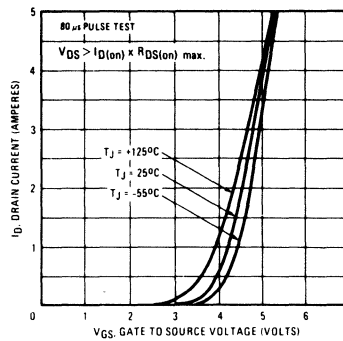


Fig. 3 – Typical Saturation Characteristics

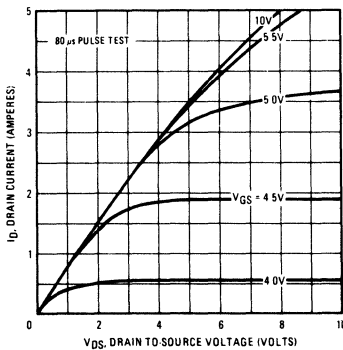


Fig. 4 – Forward Bias Safe Operating Area

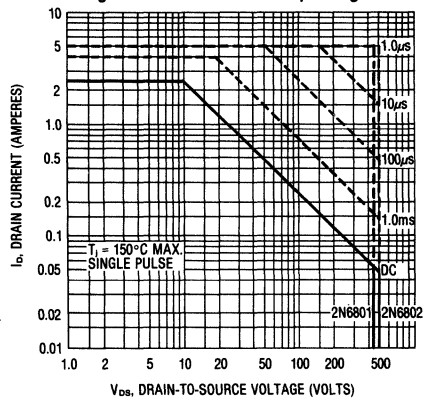
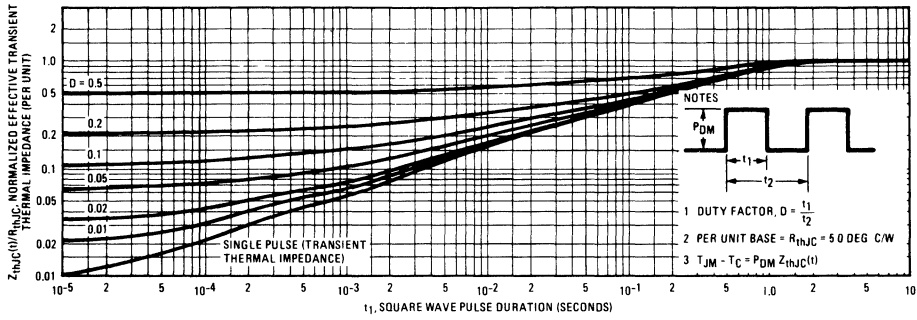


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

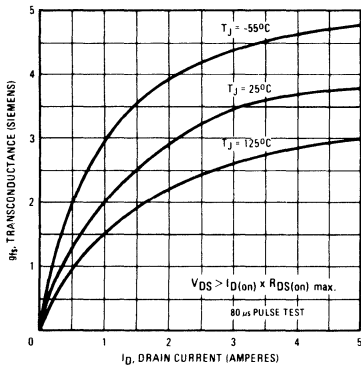


Fig. 7 – Typical Source-Drain Diode Forward Voltage

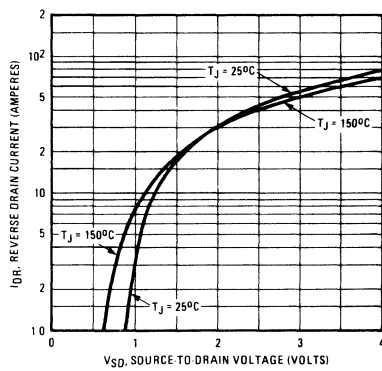


Fig. 8 – Breakdown Voltage Vs. Temperature

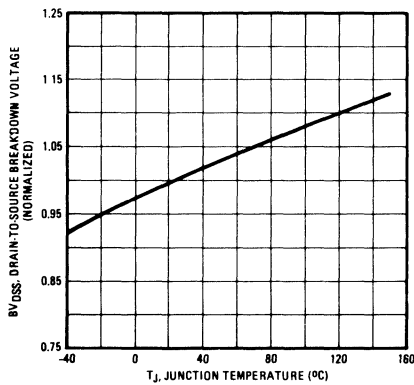


Fig. 9 – Normalized On-Resistance Vs. Temperature

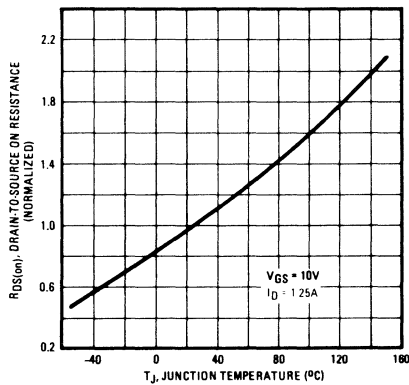


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

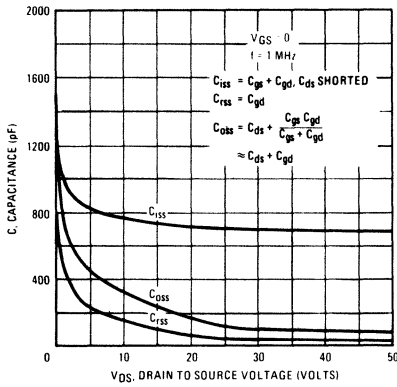


Fig. 12 — Typical On-Resistance Vs. Drain Current

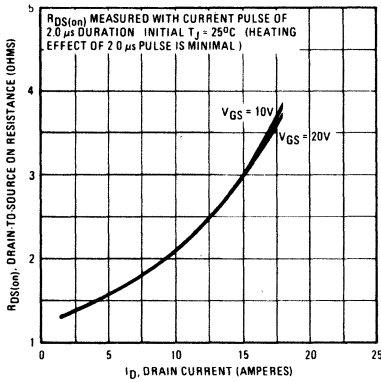


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

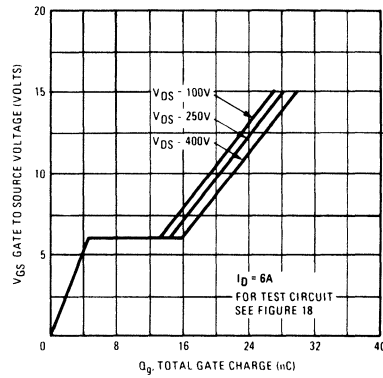


Fig. 13 — Maximum Drain Current Vs. Case Temperature

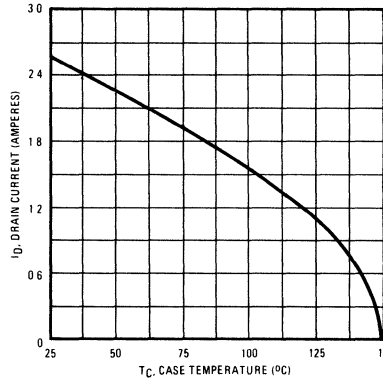


Fig. 14 — Power Vs. Temperature Derating Curve

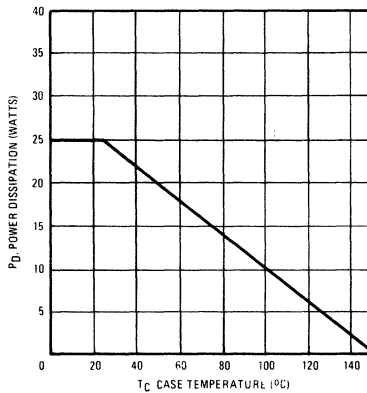


Fig. 15 – Clamped Inductive Test Circuit

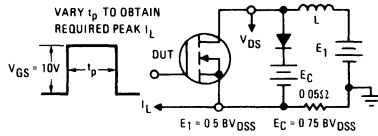


Fig. 16 – Clamped Inductive Waveforms

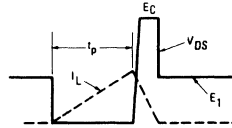


Fig. 17 – Switching Time Test Circuit

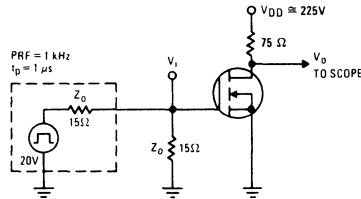
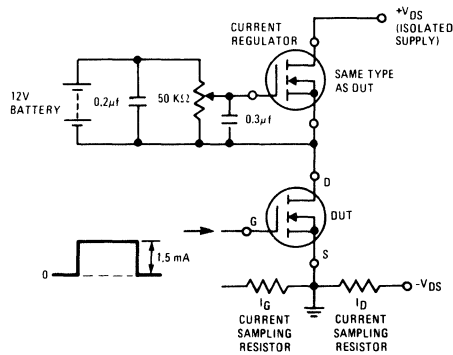


Fig. 18 – Gate Charge Test Circuit



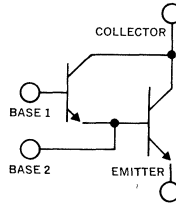
POWER DARLINGTONS

10 Amp, 150V, Planar NPN

U2T101
U2T105
U2T201
U2T205

FEATURES

- High Current Gain: up to 2000 min @ $I_C = 5A$
- Low Saturation Voltage: as low as 1.5V max @ $I_C = 5A$
- High Voltage: up to 150V min V_{CER}
- Monolithic Design Incorporating Multiple-Emitter Techniques
- Triple-Diffused Planar Construction



DESCRIPTION

Unitrode NPN Darlingtons consist of a two transistor circuit on a single monolithic planar chip.

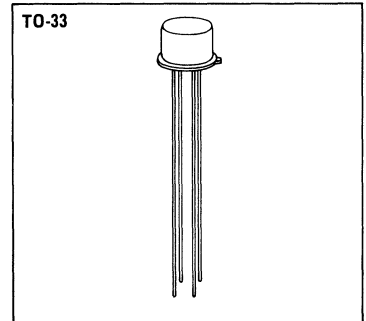
ABSOLUTE MAXIMUM RATINGS

	TO-33		3 PIN TO-66	
	U2T101	U2T105	U2T201	U2T205
Collector-Emitter Voltage	80V	150V	80V	150V
Emitter Base Voltages,				
V_{EB2}	6V	6V	6V	6V
V_{EB1}	12V	12V	12V	12V
D.C. Collector Current	5A	5A	5A	5A
Peak Collector Current	10A	10A	10A	10A
Base 1 Current	0.5A	0.5A	0.5A	0.5A
Power Dissipation				
25°C Ambient	1W	1W	2.5W	2.5W
100°C Case	5W	5W	25W	25W
Thermal Resistance, Junction to Case	20°C/W		4°C/W	
Operating and Storage Temperature Range	-65°C to 200°C		-65°C to 200°C	

MECHANICAL SPECIFICATIONS

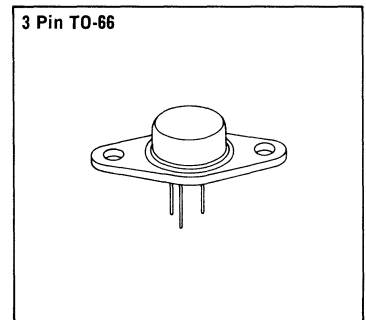
COLLECTOR CONNECTED TO CASE

	ins	mm
A	305-335	7.75-8.51
B	335-370	8.51-9.40
C	240-260	6.10-6.60
D	0.17 ± 0.02 0.01	4.32 ± 0.51 0.25
E	1.5 MIN	38.10 MIN
F	0.18 MAX	0.46 MAX
G	0.31 ± 0.03	0.79 ± 0.08
H	200	1.02
J	100	2.54
K	0.29-0.45	0.74-1.14
L	100	2.54



COLLECTOR CONNECTED TO CASE

	ins	mm
A	250-340	6.35-8.64
B	620 MAX	15.75 MAX
C	0.50-0.75	1.27-1.91
D	0.28-0.34	0.71-0.86
E	3.60 MIN	9.14 MIN
F	9.58-9.62	24.33-24.43
G	1.90-2.10	4.83-5.33
H	1.90-2.10	4.83-5.33
J	3.50 MAX RAD	8.89 MAX RAD
K	5.70-5.90	14.48-14.99
L	1.42-1.52	3.61-3.86
M	1.45 MAX RAD	3.68 MAX RAD



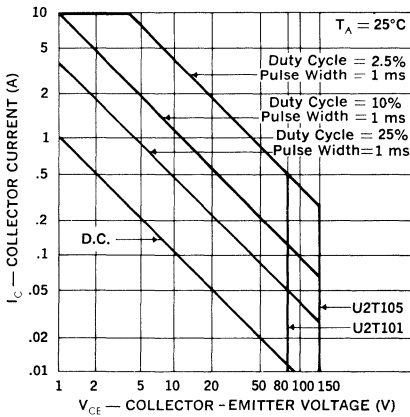
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	U2T101 & U2T201		U2T105 & U2T205		Units	Test Conditions
		Min.	Max.	Min.	Max.		
D.C. Current Gain (Note 1)	h_{FE}	2000	—	1000	—	—	$I_C = 1.0A, V_{CE} = 2V, R_{B2E} = 1K$
D.C. Current Gain (Note 1)	h_{FE}	2000	—	1000	—	—	$I_C = 5A, V_{CE} = 5V, R_{B2E} = 100$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	2.5	V	$I_C = 5A, R_{B2E} = 100$ U2T101, 201: $I_{B1} = 5mA$ U2T105, 205: $I_{B1} = 10mA$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}	80	—	150	—	V	$I_C = 25mA, R_{B1E} = 2.2K, R_{B2E} = 100$
Collector Cutoff Current	I_{CER}	—	1.0	—	1.0	μA	$R_{B1E} = 2.2K, R_{B2E} = 100$ U2T101, 201: $V_{CE} = 80V$ U2T105, 205: $V_{CE} = 150V$
Collector Cutoff Current	I_{CER}	—	1.0	—	1.0	mA	$R_{B1E} = 2.2K, R_{B2E} = 100, T = 150^\circ C$ U2T101, 201: $V_{CE} = 80V$ U2T105, 205: $V_{CE} = 150V$
Collector Capacitance	C_{obo}	—	100	—	100	pf	$V_{CB1} = 10, I_E = 0, f = 1MHz$
A.C. Current Gain	h_{fe}	5	—	5	—	—	$I_C = 1.0A, V_{CE} = 10V, f = 10MHz, R_{B2E} = 100$
Switching Speeds	Delay Time	t_d	100 Typ.	100 Typ.	—	ns	$V_{CC} = 30V,$ $I_C = 5A,$ U2T101, 201: $I_B (on) = I_B (off) = 5mA,$ U2T105, 205: $I_B (on) = I_B (off) = 10mA,$ $R_{B2E} = 100$
	Rise Time	t_r	300 Typ.	400 Typ.	—	ns	
	Storage Time	t_s	600 Typ.	500 Typ.	—	ns	
	Fall Time	t_f	500 Typ.	500 Typ.	—	ns	

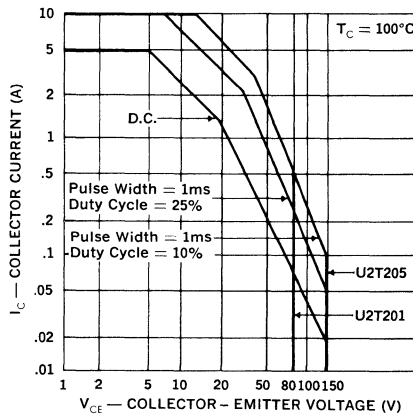
Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.



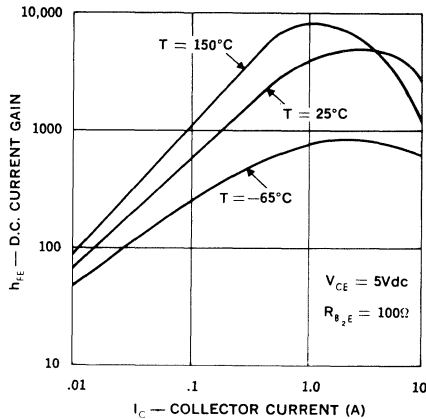
**Maximum Safe Operating Area
U2T101 & 105**



**Maximum Safe Operating Area
U2T201 & 205**



**D.C. Current Gain vs. Collector Current
U2T101, U2T105, U2T201, U2T205**



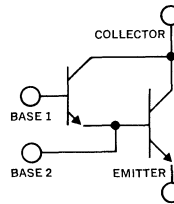
POWER DARLINGTONS

5 Amp, 150V, Planar NPN

U2T301 U2T401
U2T305 U2T405

FEATURES

- High Current Gain: 1000 min. @ $I_C = 2A$
- Low Saturation Voltage: as low as 1.5V max. @ $I_C = 2A$
- High Voltage: up to 150V min. V_{CER}
- Monolithic Design Incorporating Multiple-Emitter Techniques
- Triple-Diffused Planar Construction



DESCRIPTION

Unitrode NPN Darlington consist of a two transistor circuit on a single monolithic planar chip.

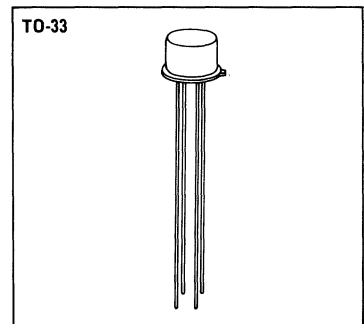
ABSOLUTE MAXIMUM RATINGS

	TO-33		3 PIN TO-66	
	U2T301	U2T305	U2T401	U2T405
Collector-Emitter Voltage	60V	150V	60V	150V
Emitter Base Voltages,				
V_{EB2}	6V	6V	6V	6V
V_{EB1}	12V	12V	12V	12V
D.C. Collector Current	2A	2A	2A	2A
Peak Collector Current	5A	5A	5A	5A
Base 1 Current	0.5A	0.5A	0.5A	0.5A
Power Dissipation				
25°C Ambient	1W	1W	2W	2W
100°C Case	4W	4W	16W	16W
Thermal Resistance				
Junction to Case	25°C/W		6°C/W	
Operating and Storage Temperature Range	-65°C to 200°C		-65°C to 200°C	

MECHANICAL SPECIFICATIONS

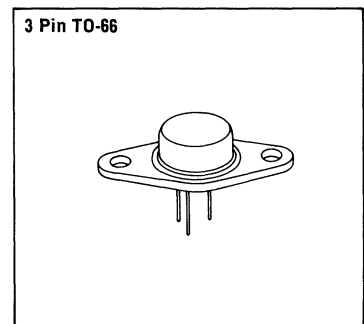
	ins.	mm
A	305-335	7.75-8.51
B	335-370	8.51-9.40
C	240-260	6.10-6.60
D	0.17 ± 0.01	4.32 ± 0.51
E	1.5 MIN	38.10 MIN
F	0.18 MAX	0.46 MAX
G	0.31 ± 0.03	0.79 ± 0.8
H	200	1.02
J	100	2.54
K	0.29-0.45	0.74-1.14
L	100	2.54

COLLECTOR CONNECTED TO CASE



	ins.	mm
A	250-340	6.35-8.64
B	620 MAX	15.75 MAX
C	050-075	1.27-1.91
D	028-034	0.71-0.86
E	350 MIN	9.14 MIN
F	958-962	24.33-24.43
G	190-210	4.83-5.33
H	190-210	4.83-5.33
J	350 MAX RAD	8.89 MAX RAD
K	570-590	14.48-14.99
L	142-152	3.61-3.86
M	145 MAX RAD	3.68 MAX RAD

COLLECTOR CONNECTED TO CASE

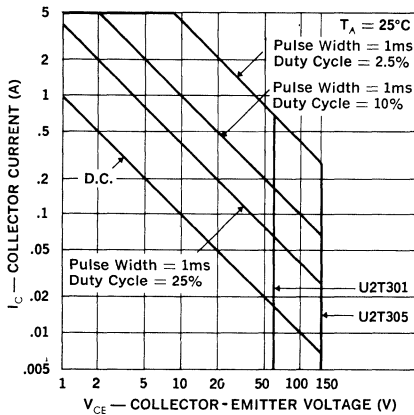


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

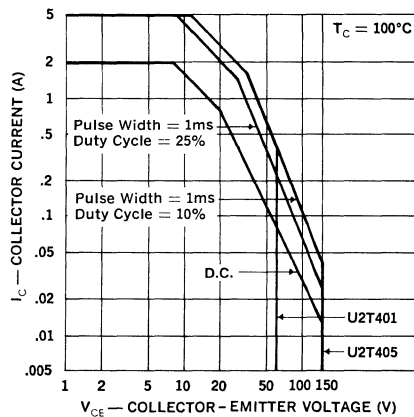
Test	Symbol	U2T301 & U2T401		U2T305 & U2T405		Units	Test Conditions
		Min.	Max.	Min.	Max.		
D.C. Current Gain (Note 1)	h_{FE}	1000	—	1000	—	—	$I_C = 1A, V_{CE} = 2V, R_{B2E} = 1K$
D.C. Current Gain (Note 1)	h_{FE}	1000	—	1000	—	—	$I_C = 2A, V_{CE} = 5V, R_{B2E} = 100$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	2.5	V	$I_C = 2A, R_{B2E} = 100, I_{B1} = 4mA$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}	60	—	150	—	V	$I_C = 25mA, R_{B1E} = 2.2K, R_{B2E} = 100$
Collector Cutoff Current	I_{CER}	—	1.0	—	1.0	μA	$R_{B1E} = 2.2K, R_{B2E} = 100$ U2T301, 401: $V_{CE} = 60V$ U2T305, 405: $V_{CE} = 150V$
Collector Cutoff Current	I_{CER}	—	1.0	—	1.0	mA	$R_{B1E} = 2.2K, R_{B2E} = 100, T = 150^\circ C$ U2T301, 401: $V_{CE} = 60V$ U2T305, 405: $V_{CE} = 150V$
Collector Capacitance	C_{obo}	—	60	—	60	pf	$V_{CB1} = 10V, I_E = 0, f = 1MHz$
A.C. Current Gain	h_{fe}	5	—	5	—	—	$I_C = 0.5A, V_{CE} = 10V, f = 10MHz, R_{B2E} = 100$
Switching Speeds	Delay Time	t_d	100 Typ.	100 Typ.	100 Typ.	ns	$V_{CC} = 30V, I_C = 2A, I_B(ON) = I_B(OFF) = 4mA$ $R_{B2E} = 100$
	Rise Time	t_r	200 Typ.	300 Typ.	300 Typ.	ns	
	Storage Time	t_s	800 Typ.	800 Typ.	800 Typ.	ns	
	Fall Time	t_f	300 Typ.	300 Typ.	300 Typ.	ns	

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

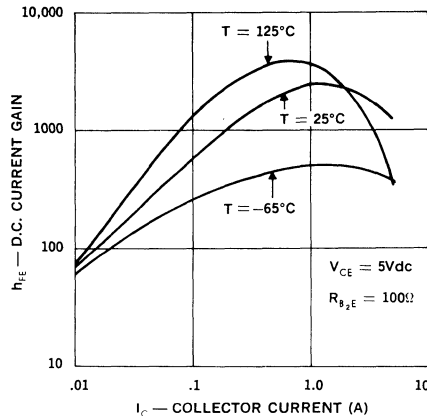
**Maximum Safe Operating Area
U2T301 & 305**



**Maximum Safe Operating Area
U2T401 & 405**



**D.C. Current Gain vs. Collector Current
U2T301, U2T305, U2T401, U2T405**



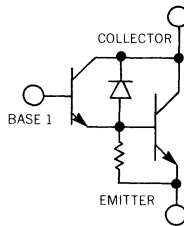
POWER DARLINGTONS

3 Amp, 100V, Planar NPN, Plastic

U2TA506
U2TA508
U2TA510

FEATURES

- High Current Gain: 500 min. @ $I_C = 3A$
- Low Saturation Voltage: as low as 1.5V max. @ $I_C = 3A$
- Economic Plastic Molded Construction

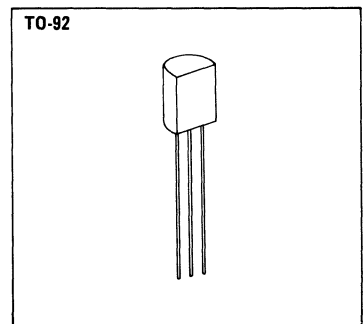
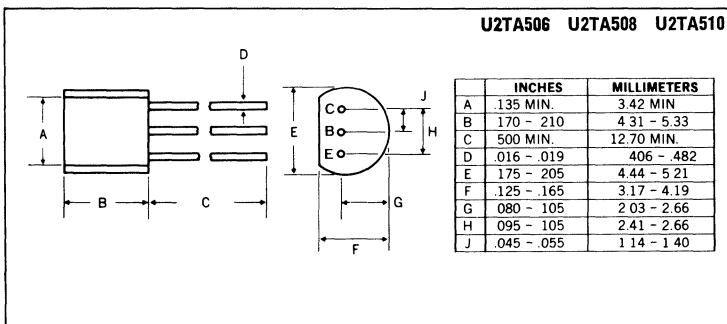


DESCRIPTION

Unitrode NPN Darlington consists of a two transistor circuit on a single monolithic planar chip, including integral bias resistance and protective diode. It is ideally suited for pulse power applications in power supplies, printers, solid state relays and displays.

ABSOLUTE MAXIMUM RATINGS

	U2TA506	U2TA508	U2TA510
Collector-Base Voltage, V_{CBO}	80V	100V	120V
Collector-Emitter Voltage, V_{CEO}	60V	80V	100V
Emitter-Base Voltage, V_{EBO}		5V	
D.C. Collector Current, I_C		.75A	
Peak Collector Current, I_C		5A	
Base Current, I_B		.6A	
Power Dissipation			
25°C Case		2.2W	
25°C Ambient		871mW	
Thermal Resistance, θ_{J-C}		62.5°C/W	
Thermal Resistance, θ_{J-A}		155°C/W	
Storage Temperature Range		-55 to +150°C	
Maximum Junction Temperature		+175°C	

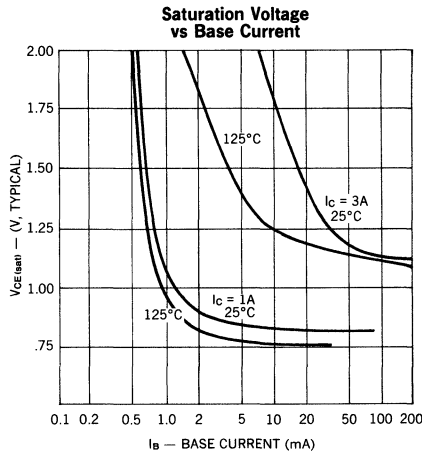
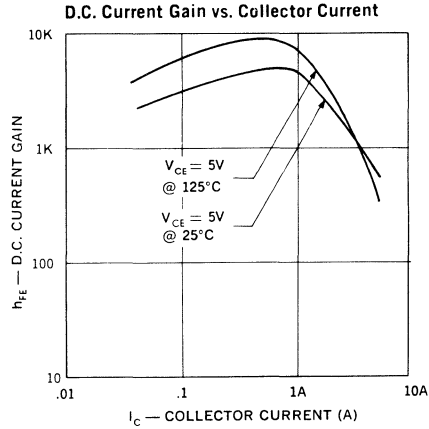
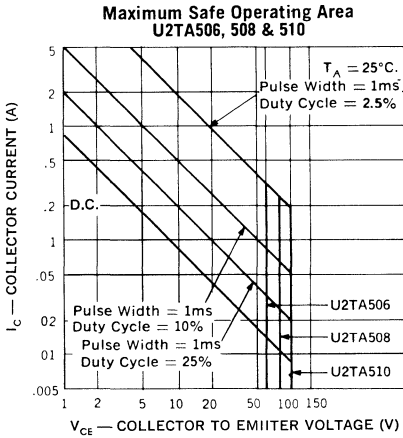


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	1000	—	—	$I_C = 1A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	500	—	—	$I_C = 3A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	300 Typ.		—	$I_C = 5A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	Vdc	$I_C = 3A, I_B = 30mA$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mA$
U2TA506		60	—		
U2TA508		80	—		
U2TA510		100	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μ Adc	$V_{CE} = rating, R = 100\Omega$
Collector-Emitter Cutoff Current	I_{CER}	—	1	mAdc	$V_{CE} = rating, R = 100\Omega, T_A = 125^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μ Adc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	50	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
A.C. Current Gain	h_{fe}	4.0 Typ.		—	$I_C = 1Adc, V_{CE} = 5Vdc, f = 10MHz$
Rise Time	t_r	600 Typ.		ns	$I_C = 2A$
Storage Time	t_s	1500 Typ.		ns	$V_{CC} = rating, I_{B(on)} = I_{B(off)} = 4mA$
Fall Time	t_f	800 Typ.		ns	

Note 1: Pulse width = 300 μ s; duty cycle \leq 2%.

Note 2: For thermal considerations for operating U2TA506, U2TA508 and U2TA510, refer to Application Note U-77.



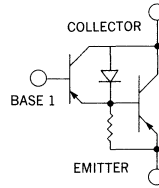
POWER DARLINGTONS

3A, 100V, Planar PNP, Plastic

U2TA606
U2TA608
U2TA610

FEATURES

- High current gain: 500 min @ $I_C = 3A$
- Low saturation voltage: as low as 1.5V max @ $I_C = 3A$
- Economic plastic molded construction



DESCRIPTION

Unitorde PNP Darlingtons consist of two transistor circuits on a single monolithic planar chip, including integral bias resistance. It is ideally suited for pulse applications in power supplies, printers, solid state relays and displays.

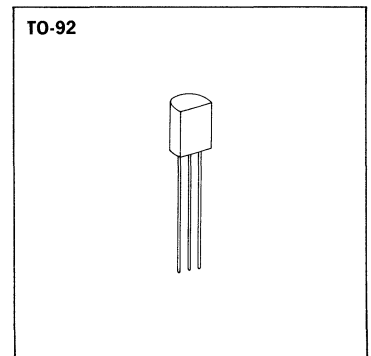
ABSOLUTE MAXIMUM RATINGS

	U2TA606	U2TA608	U2TA610
Collector-Base Voltage, V_{CBO}	80V	100V	120V
Collector-Emitter Voltage, V_{CEO}	60V	80V	100V
Emitter-Base Voltage, V_{EBO}	5V		
D.C. Collector Current, I_C		0.75A	
Peak Collector Current, I_C		5.0A	
Base Current, I_B		0.6A	
Power Dissipation			
25°C Case		2.2W	
25°C Ambient		871mW	
Thermal Resistance, θ_{J-C}		62.5°C/W	
Thermal Resistance, θ_{J-A}		155°C/W	
Storage Temperature Range		-55°C to +150°C	
Maximum Junction Temperature		150°C	

MECHANICAL SPECIFICATIONS

U2TA606 U2TA608 U2TA610

	INCHES	MILLIMETERS
A	.135 MIN.	3.42 MIN.
B	.170 - .210	4.31 - 5.33
C	.500 MIN.	12.70 MIN.
D	.016 - .019	.406 - .482
E	.175 - .205	4.44 - 5.21
F	.125 - .165	3.17 - 4.19
G	.080 - .105	2.03 - 2.66
H	.095 - .105	2.41 - 2.66
J	.045 - .055	1.14 - 1.40

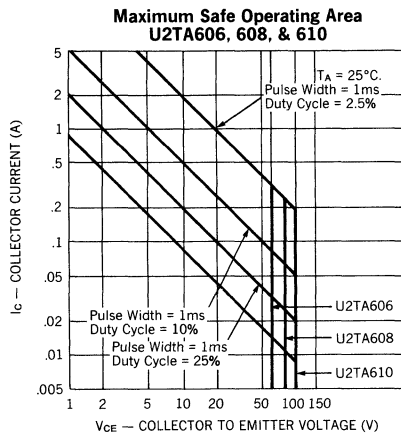
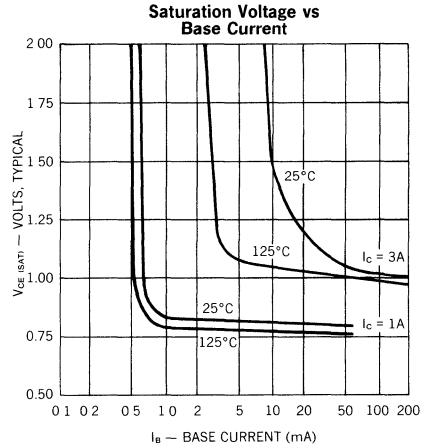
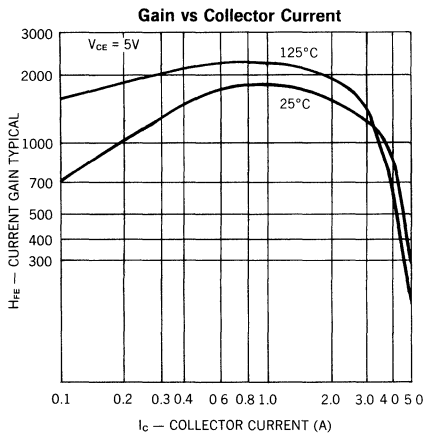


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

TEST	SYMBOL	MIN.	MAX.	UNITS	TEST CONDITIONS
D.C. Current Gain (Note 1)	h_{FE}	1000	—	—	$I_C = -1A, V_{CE} = -5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	500	—	—	$I_C = -3A, V_{CE} = -5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	Vdc	$I_C = -3A, I_B = -30mA$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = -10mAdc$
U2TA606		60	—		
U2TA608		80	—		
U2TA610		100	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μAdc	$V_{CE} = \text{Rating}, R = 100\Omega$
Collector-Emitter Cutoff Current	I_{CER}	—	1	mAdc	$V_{CE} = \text{Rating}, R = 100\Omega, T = 125^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = -5Vdc$
Output Capacitance	C_{ob}	—	50	pF	$V_{CB} = -10Vdc, I_E = 0, f = 1MHz$
A.C. Current Gain	h_{FE}	4.0 Typ.		—	$I_C = -1Adc, V_{CE} = -5Vdc, f = 10MHz$
Rise Time	t_r	600 Typ.		ns	$I_C = -2A$
Storage Time	t_s	1500 Typ.		ns	$V_{CC} = \text{Rating}, I_B(\text{on}) = I_B(\text{off}) = -4mA$
Fall Time	t_f	800 Typ.		ns	

Note 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

Note 2. For thermal considerations for operating U2TA606, U2TA608 and U2TA610, refer to Application Note U-77.



POWER MOSFET TRANSISTORS

100 Volt, 1.5 Ohm
N-Channel

UFNA11
UFNA12

FEATURES

- Designed for High-Speed Switching Applications
- Direct Logic Interface
- No Thermal Runaway or Second Breakdown
- Economical Plastic Molded Construction

DESCRIPTION

Near infinite gain, low on-state impedance and ultra fast switching speeds make the Unitrode POWER MOSFET ideally suited for many high-speed switching applications.

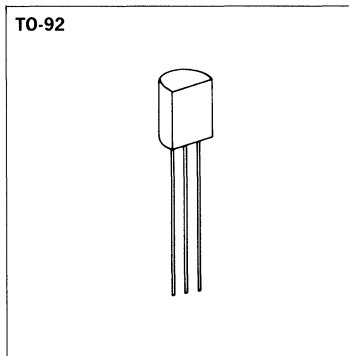
ABSOLUTE MAXIMUM RATINGS

	UFNA11	UFNA12
Drain-Source Voltage, V_{DS}	60V	100V
Drain-Gate Voltage, V_{DG}	60V	100V
Continuous Drain Current, I_D		1.0A
Pulsed Drain Current, I_{DM}		2.0A
Gate-Source Voltage, V_{GS}		$\pm 20V$
Power Dissipation, P_D		
25°C Case		2.4W
25°C Ambient		750mW
Thermal Resistance, θ_{J-C}		62.5°C/W
Thermal Resistance, θ_{J-A}		200°C/W
Operating and Storage Temperature Range		-40°C to +150°C
Maximum Junction Temperature		+175°C

MECHANICAL SPECIFICATIONS

UFNA11 UFNA12

	INCHES	MILLIMETERS
A	.135 MIN.	3.42 MIN.
B	.170 - .210	4.31 - 5.33
C	500 MIN.	12.70 MIN.
D	.016 - .019	.406 - .482
E	.175 - .205	4.44 - 5.21
F	.125 - .165	3.17 - 4.19
G	.080 - .105	2.03 - 2.66
H	.095 - .105	2.41 - 2.66
J	.045 - .055	1.14 - 1.40



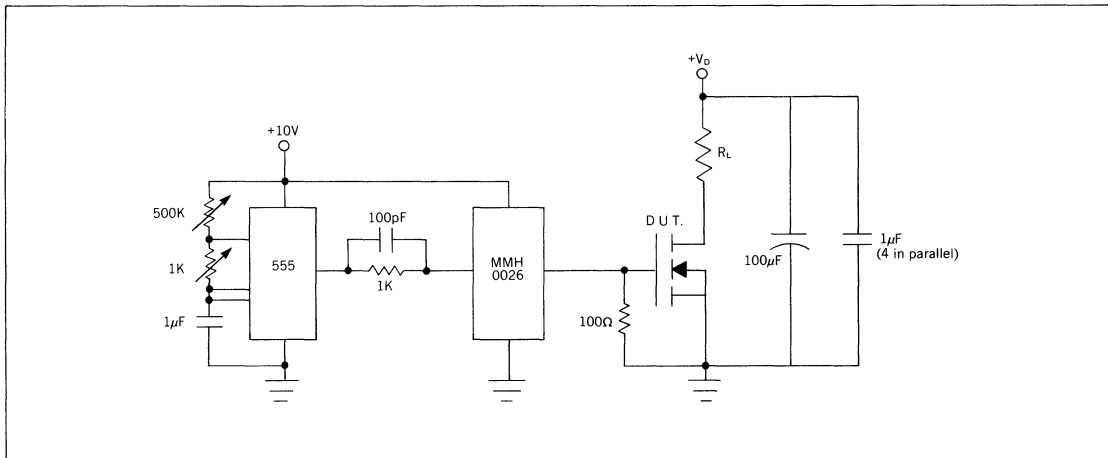
ELECTRICAL SPECIFICATIONS (at 25°C unless otherwise noted)

PARAMETER	SYMBOL	MIN.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage UFNA11 UFNA12	BV_{DSS} BV_{DSS}	60 100	— —	 V	$V_{GS} = 0$ $I_D = 200\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	2.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Gate-Body Leakage	I_{GSS}	—	100	nA	$V_{GS} = 10V, V_{DS} = 0$
Zero Gate Voltage Drain Current	I_{DSS}	—	10	μA	$V_{DS} = 0.8 \text{ Rating}, V_{GS} = 0$
		—	500	μA	$V_{DS} = 0.8 \text{ Rating}, V_{GS} = 0$ $T_J = 125^\circ C$
On-State Drain Current	$I_{D(on)}$	2.0	—	A	$V_{DS} = 25V, V_{GS} = 10V$ (Note 1)
Drain-Source On-State Resistance	$R_{DS(on)}$	—	1.5	Ω	$V_{GS} = 10V, I_D = 1.0A$ (Note 1)
Forward Transconductance	g_{fs}	400	—	$m\Omega$	$V_{DS} = 25V, I_D = 1A$ (Note 1)
Input Capacitance	C_{iss}	—	200	pF	$V_{GS} = 0$ $V_{DS} = 25V$ $f = 1.0MHz$
Output Capacitance	C_{oss}	—	80	pF	
Reverse Transfer Capacitance	C_{rss}	—	40	pF	
Turn-On Delay Time	$t_{d(on)}$	—	10	ns	$V_D \approx .5 \times \text{Rated } V_{DS}$ $I_D = .5A$ $V_{GS(on)} = 10V$ (See Test Circuit Below)
Rise Time	t_r	—	10	ns	
Turn-Off Delay Time	$t_{d(off)}$	—	20	ns	
Fall-Time	t_f	—	20	ns	

Note: 1. Pulse width = 300 μs ; Duty Cycle \leq 2%

4

SWITCHING SPEED CIRCUIT



POWER MOSFET TRANSISTORS

100 Volt, 2.4 Ohm
N-Channel

UFND1Z0
UFND1Z3

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

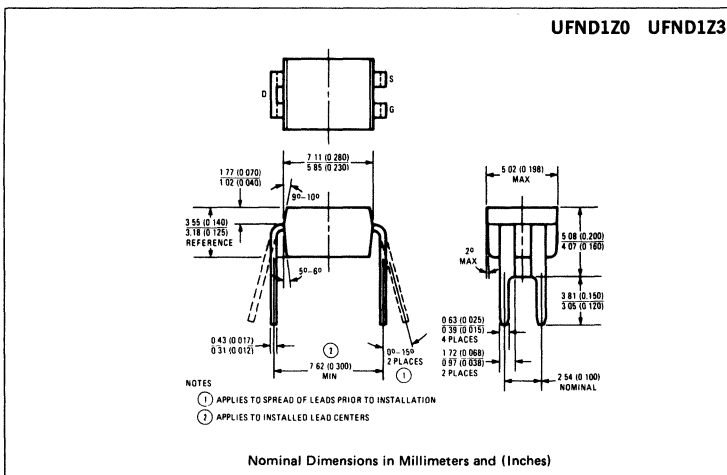
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

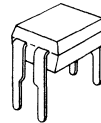
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND1Z0	100V	2.4 Ω	0.5A
UFND1Z3	60V	3.2 Ω	0.4A

MECHANICAL SPECIFICATIONS



DIL-4



ABSOLUTE MAXIMUM RATINGS

Parameter	UFND1Z0	UFND1Z3	Units
V_{DS} Drain - Source Voltage ①	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	0.5	0.4	A
I_{DM} Pulsed Drain Current	4.0	3.2	A
V_{GS} Gate - Source Voltage	± 20		V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	1.0 (See Fig. 13)		W
Linear Derating Factor	0.008 (See Fig. 13)		W/K
I_{LM} Inductive Current, Clamped	(See Fig. 14 and 15) $L = 100\mu\text{H}$		A
T_J T_{stg} Operating Junction and Storage Temperature Range	-55 to 150		$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	UFND1Z0	100	-	-	V	$V_{GS} = 0\text{V}$
	UFND1Z3	60	-	-	V	$I_D = 250\mu\text{A}$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	-	-	500	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	-	-	-500	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	-	-	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$
		-	-	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	UFND1Z0	0.5	-	-	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$
	UFND1Z3	0.4	-	-	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFND1Z0	-	2.2	2.4	Ω	$V_{GS} = 10\text{V}, I_D = 0.25\text{A}$
	UFND1Z3	-	2.8	3.2	Ω	
g_{fs} Forward Transconductance ②	ALL	-	0.35	-	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 0.25\text{A}$
C_{iss} Input Capacitance	ALL	-	50	70	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 9
C_{oss} Output Capacitance	ALL	-	20	30	pF	
C_{rss} Reverse Transfer Capacitance	ALL	-	5.0	10	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	-	10	20	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 0.25\text{A}, Z_0 = 50\Omega$ See Fig. 16
t_r Rise Time	ALL	-	15	25	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	-	15	25	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	-	10	20	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	-	2.0	3.0	nC	$V_{GS} = 10\text{V}, I_D = 1.2\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	-	1.0	-	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	-	1.0	-	nC	
L_D Internal Drain Inductance		-	4.0	-	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
	ALL					
L_S Internal Source Inductance	ALL	-	6.0	-	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJA} Junction-to-Ambient	ALL	-	-	120	K/W	Free Air Operation
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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND1Z0	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFND1Z3	—	—	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND1Z0	—	—	4.0	A	
		UFND1Z3	—	—	3.2	A	
V_{SD}	Diode Forward Voltage ②	UFND1Z0	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 0.5\text{A}, V_{GS} = 0\text{V}$
		UFND1Z3	—	—	1.3	V	$T_C = 25^\circ\text{C}, I_S = 0.4\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	$T_J = 150^\circ\text{C}, I_F = 0.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	$T_J = 150^\circ\text{C}, I_F = 0.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Fig. 1 – Typical Output Characteristics

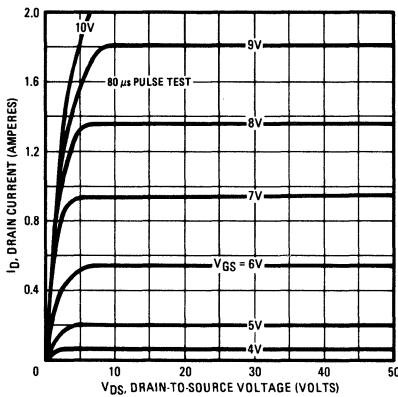


Fig. 2 – Typical Transfer Characteristics

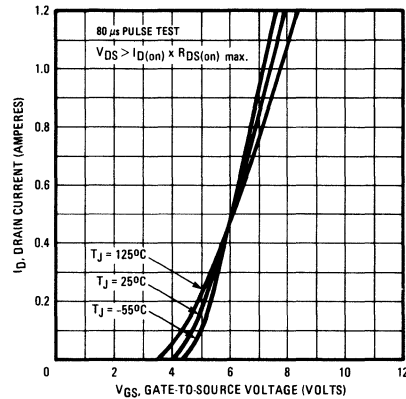


Fig. 3 – Typical Saturation Characteristics

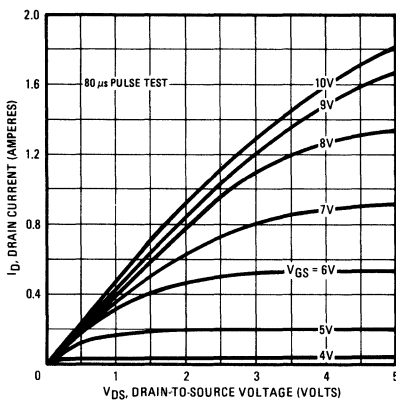


Fig. 4 – Maximum Safe Operating Area

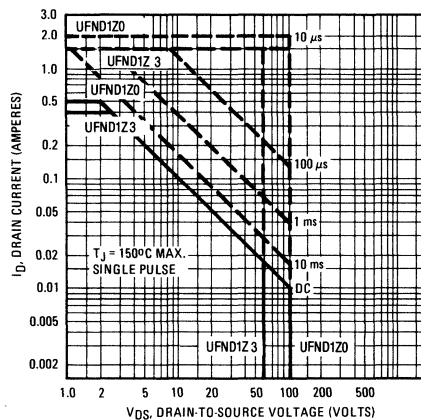


Fig. 5 – Typical Transconductance Vs. Drain Current

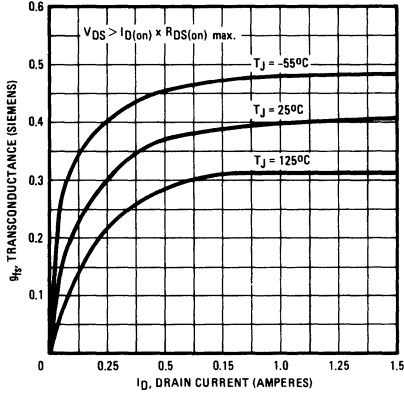


Fig. 6 – Typical Source-Drain Diode Forward Voltage

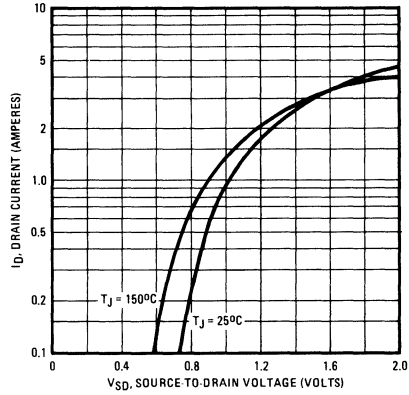


Fig. 7 – Breakdown Voltage Vs. Temperature

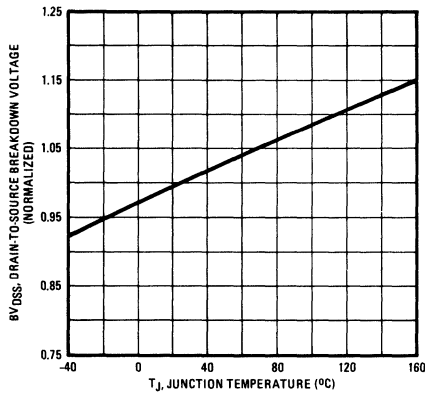


Fig. 8 – Normalized On-Resistance Vs. Temperature

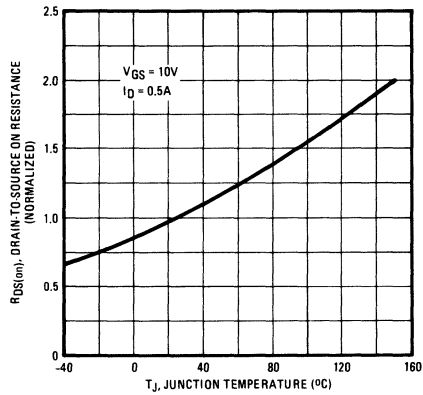


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

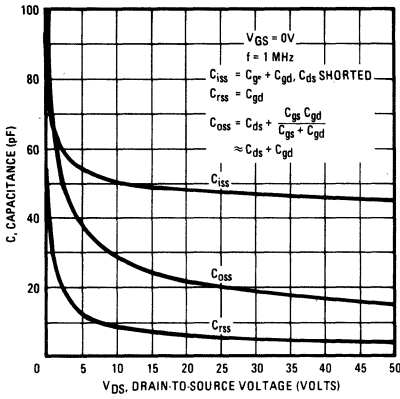


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

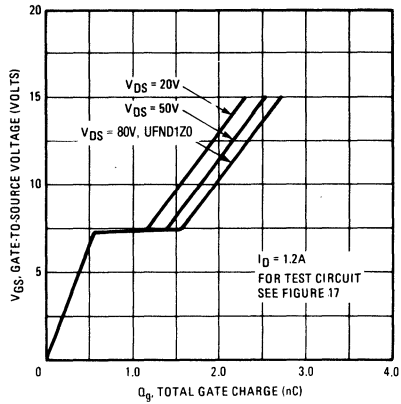


Fig. 11 – Typical On-Resistance Vs. Drain Current

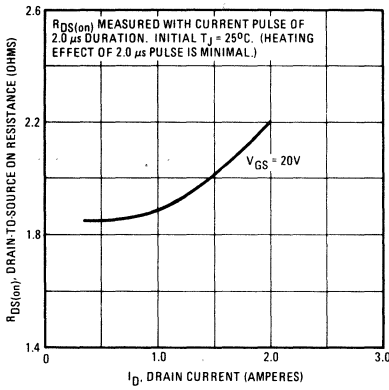


Fig. 12 – Maximum Drain Current Vs. Case Temperature

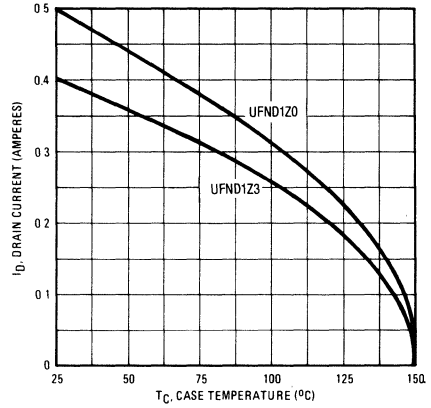


Fig. 13 – Power Vs. Temperature Derating Curve

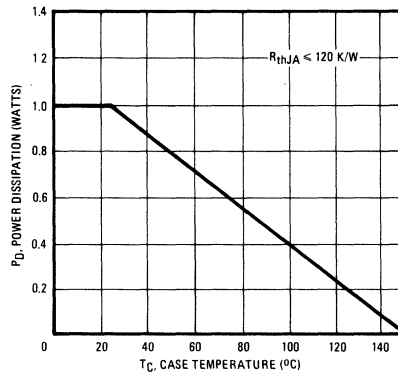


Fig. 14 – Clamped Inductive Test Circuit

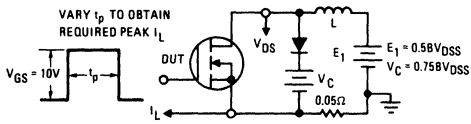


Fig. 15 – Clamped Inductive Waveforms

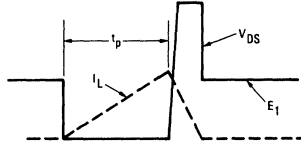


Fig. 16 – Switching Time Test Circuit

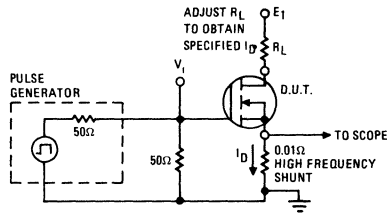
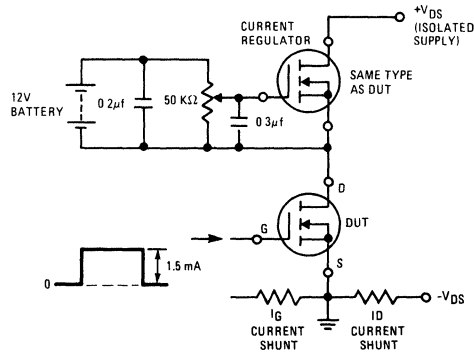


Fig. 17 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.6 Ohm
N-Channel

UFND110
UFND113

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

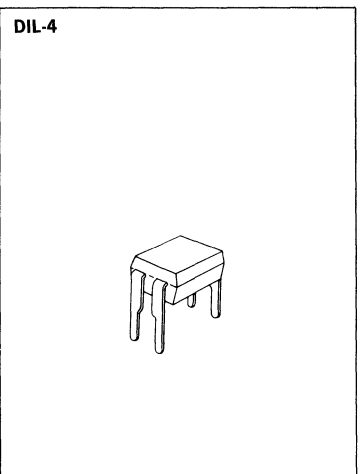
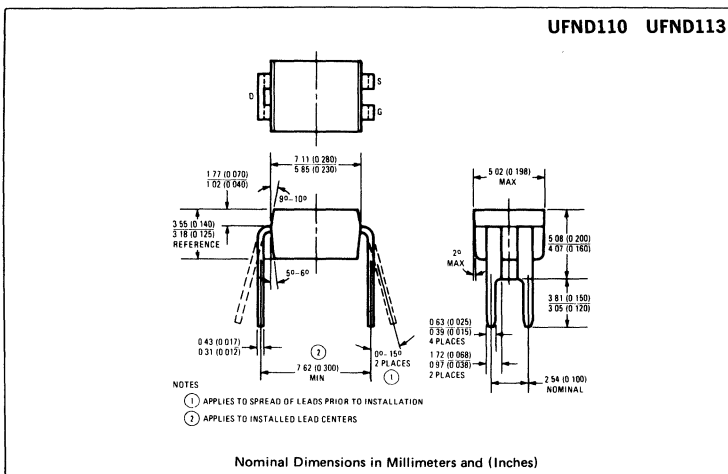
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND110	100V	0.6Ω	1.0A
UFND113	60V	0.8Ω	0.8A

MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFND110	UFND113	Units
V _{DS} Drain - Source Voltage ①	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	1.0	0.8	A
I _{DM} Pulsed Drain Current	8.0	6.4	A
V _{GS} Gate - Source Voltage	± 20		V
P _D @ T _C = 25°C Max. Power Dissipation	1.0 (See Fig. 13)		W
Linear Derating Factor	0.008 (See Fig. 13)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH		A
	8.0	6.4	
T _J T _{stg} Operating Junction and Storage Temperature Range	-55 to 150		°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	UFND110	100	—	—	V	V _{GS} = 0V
	UFND113	60	—	—	V	I _D = 250μA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} ; I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	UFND110	1.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max.; V _{GS} = 10V
	UFND113	0.8	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFND110	—	0.5	0.6	Ω	V _{GS} = 10V, I _D = 0.8A
	UFND113	—	0.6	0.8	Ω	
g _{fs} Forward Transconductance ②	ALL	0.8	1.2	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max.; I _D = 0.8A
C _{iss} Input Capacitance	ALL	—	135	200	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 9
C _{oss} Output Capacitance	ALL	—	80	100	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	20	25	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	10	20	ns	V _{DD} = 0.5 BV _{DSS} ; I _D = 0.8A, Z _o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t _r Rise Time	ALL	—	15	25	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	15	25	ns	
t _f Fall Time	ALL	—	10	20	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.0	nC	V _{GS} = 10V, I _D = 4.0A, V _{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
	ALL	—	2.0	—	nC	
	ALL	—	7.0	—	nC	
L _D Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
	ALL	—	4.0	—	nH	
L _S Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

THERMAL RESISTANCE

R _{thJA} Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation
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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND110	—	—	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFND113	—	—	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND110	—	—	8.0	A	
		UFND113	—	—	6.4	A	
V_{SD}	Diode Forward Voltage ②	UFND110	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 1.0\text{A}, V_{GS} = 0\text{V}$
		UFND112	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 0.8\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Fig. 1 – Typical Output Characteristics

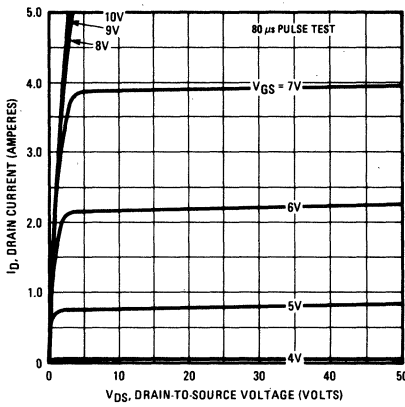


Fig. 2 – Typical Transfer Characteristics

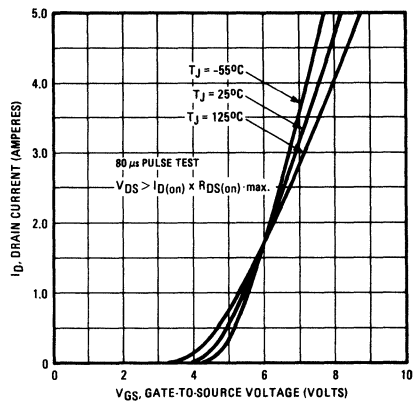


Fig. 3 – Typical Saturation Characteristics

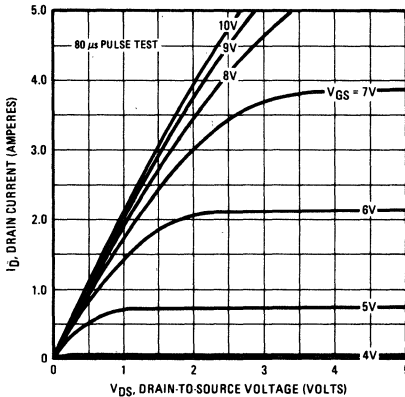


Fig. 4 – Maximum Safe Operating Area

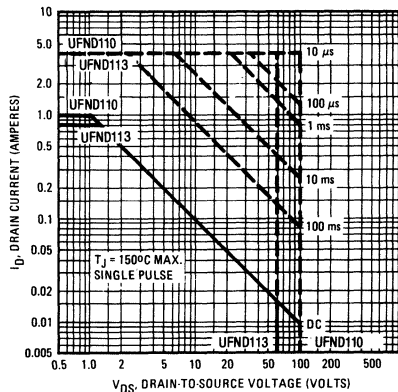


Fig. 5 – Typical Transconductance Vs. Drain Current

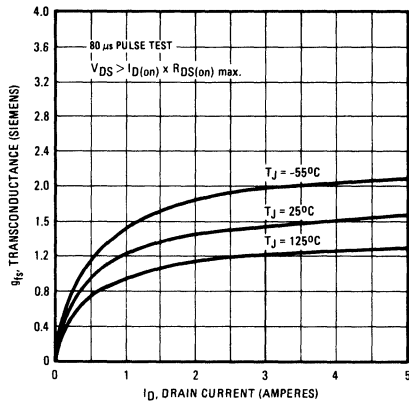


Fig. 6 – Typical Source-Drain Diode Forward Voltage

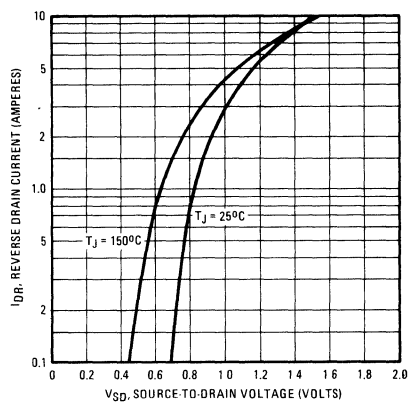


Fig. 7 – Breakdown Voltage Vs. Temperature

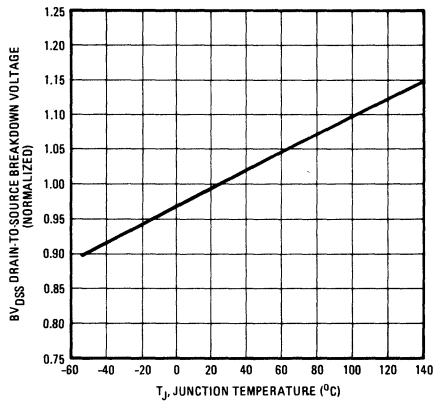


Fig. 8 – Normalized On-Resistance Vs. Temperature

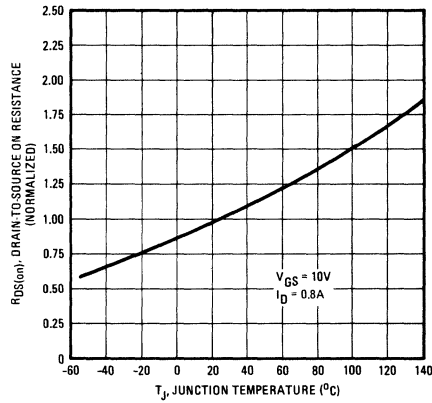


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

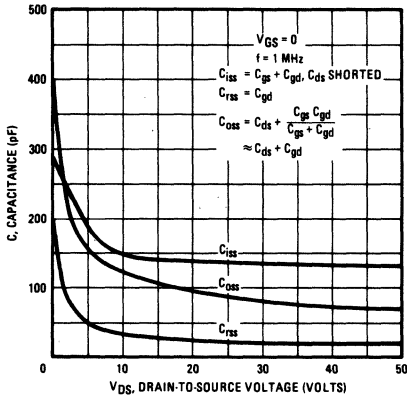


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

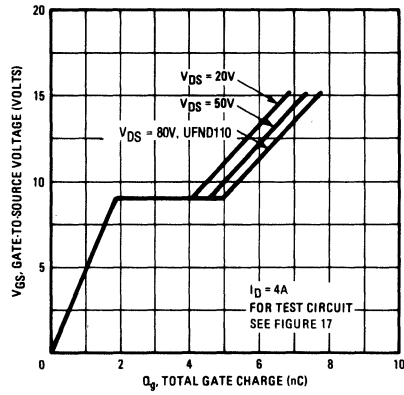


Fig. 11 – Typical On-Resistance Vs. Drain Current

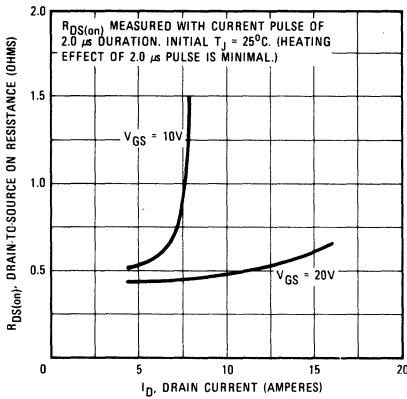


Fig. 12 – Maximum Drain Current Vs. Case Temperature

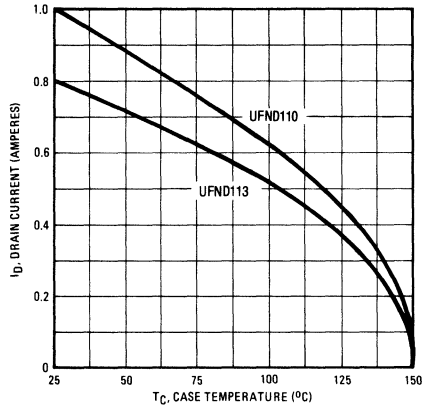


Fig. 13 – Power Vs. Temperature Derating Curve

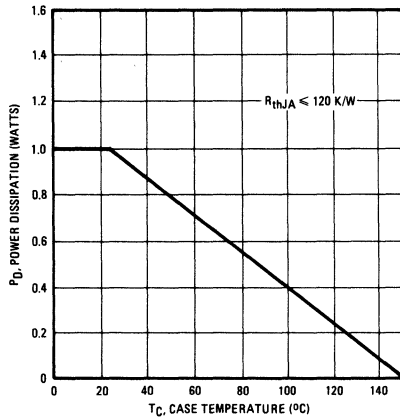


Fig. 14 – Clamped Inductive Test Circuit

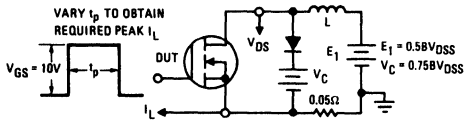


Fig. 15 – Clamped Inductive Waveforms

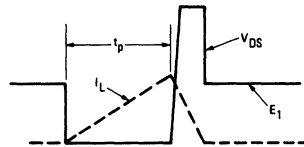


Fig. 16 – Switching Time Test Circuit

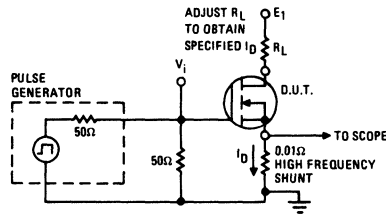
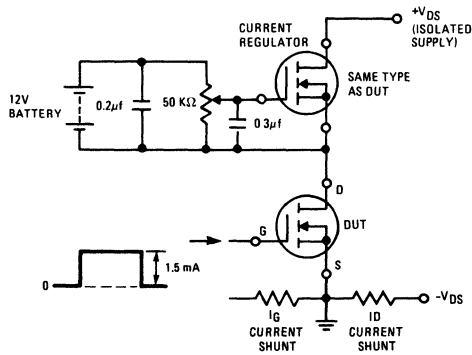


Fig. 17 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm N-Channel

UFND120
UFND123

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

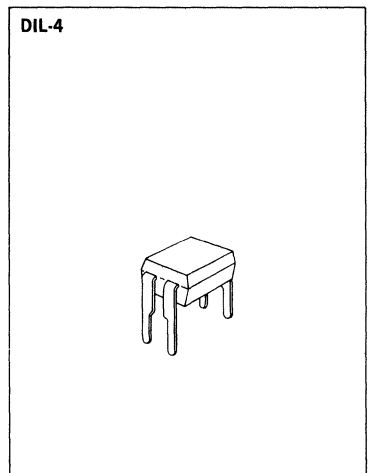
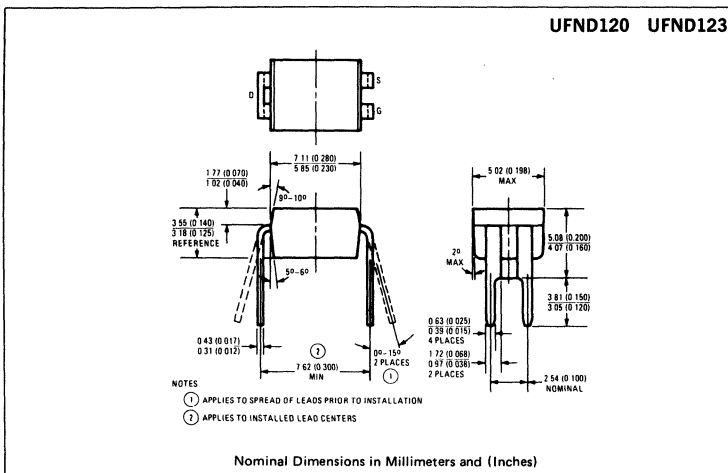
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND120	100V	0.3Ω	1.3A
UFND123	60V	0.4Ω	1.1A

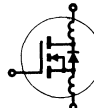
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFND120	UFND123	Units
V_{DS} Drain – Source Voltage ①	100	60	V
V_{DGR} Drain – Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	V
$I_D @ T_A = 25^\circ\text{C}$ Continuous Drain Current	1.3	1.1	A
I_{DM} Pulsed Drain Current	5.2	4.4	A
V_{GS} Gate – Source Voltage	± 20		V
$P_D @ T_A = 25^\circ\text{C}$ Max. Power Dissipation	1.0 (See Fig. 13)		W
Linear Derating Factor	0.008 (See Fig. 13)		W/K
I_{LM} Inductive Current, Clamped	(See Fig. 14 and 15) $L = 100\mu\text{H}$		A
	5.21	4.4	
T_J Operating Junction and Storage Temperature Range	–55 to 150		$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		$^\circ\text{C}$


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain – Source Breakdown Voltage	UFND120	100	–	–	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFND123	60	–	–	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate – Source Leakage Forward	ALL	–	–	500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate – Source Leakage Reverse	ALL	–	–	–500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		–	–	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFND120	1.3	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $V_{GS} = 10\text{V}$	
	UFND123	1.1	–	–	A		
$R_{DS(on)}$ Static Drain – Source On-State Resistance ②	UFND120	–	0.25	0.30	Ω	$V_{GS} = 10\text{V}$, $I_D = 0.6\text{A}$	
	UFND123	–	0.30	0.40	Ω		
g_{fs} Forward Transconductance ②	ALL	0.9	1.0	–	S (③)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $I_D = 0.6\text{A}$	
C_{iss} Input Capacitance	ALL	–	450	600	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 9	
C_{oss} Output Capacitance	ALL	–	200	400	pF		
C_{rfs} Reverse Transfer Capacitance	ALL	–	50	100	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	–	20	40	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 0.6\text{A}$, $Z_\theta = 50\Omega$ See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	–	35	70	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	–	50	100	ns		
t_f Fall Time	ALL	–	35	70	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	$V_{GS} = 10\text{V}$, $I_D = 5.2\text{A}$, $V_{DS} = 0.8$ Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	–	6.0	–	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	–	5.0	–	nC		
L_D Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.	

THERMAL RESISTANCE

Parameter	UFND120	UFND123	Units
R_{thJA} Junction-to-Ambient	ALL	–	120 K/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND120	—	—	1.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
		UFND123	—	—	1.1	A		
I_{SM}	Pulse Source Current (Body Diode)	UFND120	—	—	5.2	A		
		UFND123	—	—	4.4	A		
V_{SD}	Diode Forward Voltage ②	UFND120	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 1.3\text{A}, V_{GS} = 0\text{V}$	
		UFND123	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 1.1\text{A}, V_{GS} = 0\text{V}$	
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.3\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.3\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Fig. 1 — Typical Output Characteristics

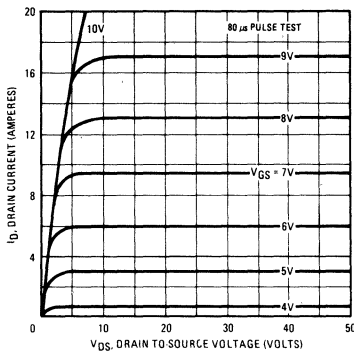


Fig. 2 — Typical Transfer Characteristics

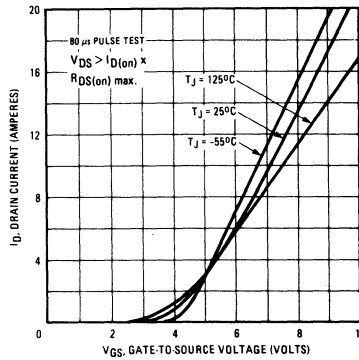


Fig. 3 — Typical Saturation Characteristics

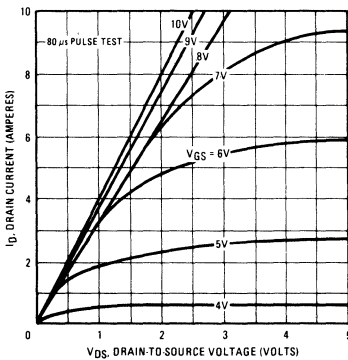


Fig. 4 — Maximum Safe Operating Area

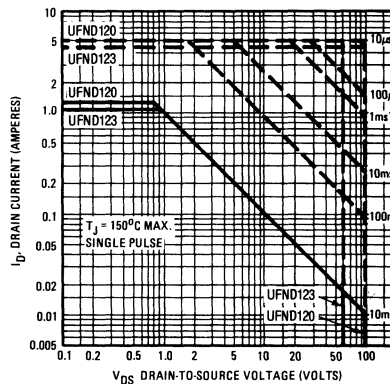


Fig. 5 – Typical Transconductance Vs. Drain Current

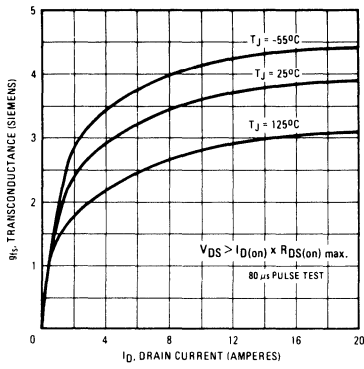


Fig. 6 – Typical Source-Drain Diode Forward Voltage

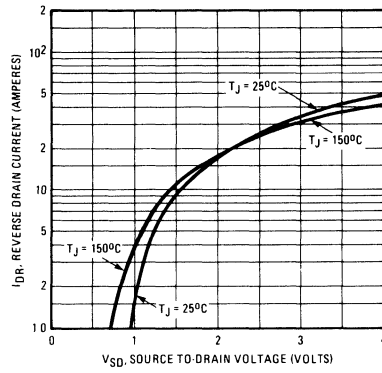


Fig. 7 – Breakdown Voltage Vs. Temperature

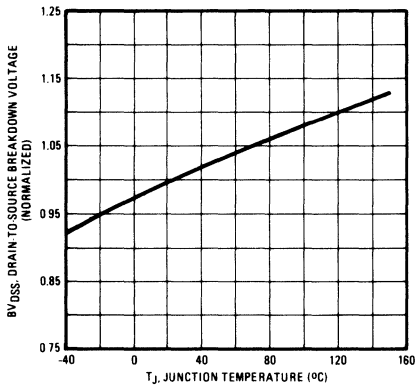


Fig. 8 – Normalized On-Resistance Vs. Temperature

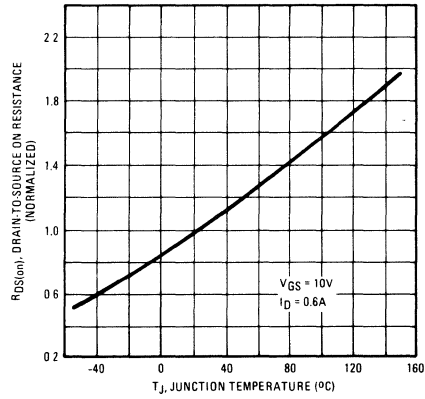


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

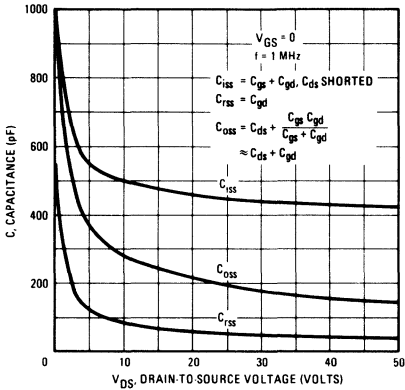


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

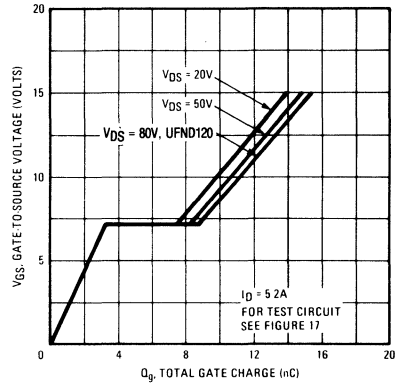


Fig. 11 — Typical On-Resistance Vs. Drain Current

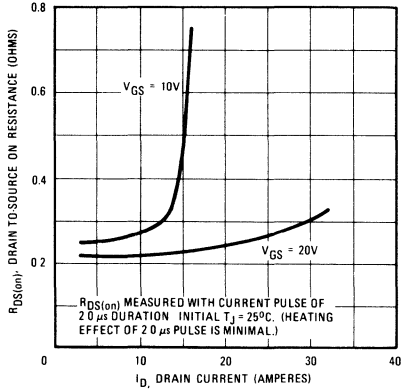


Fig. 12 — Maximum Drain Current Vs. Case Temperature

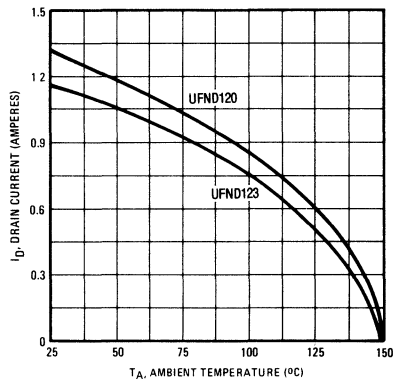


Fig. 13 — Power Vs. Temperature Derating Curve

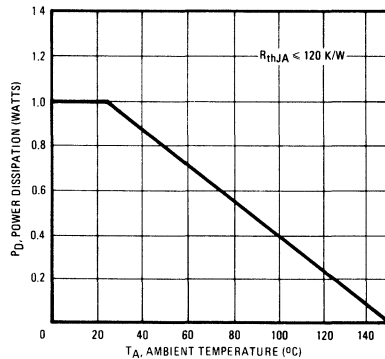


Fig. 14 – Clamped Inductive Test Circuit

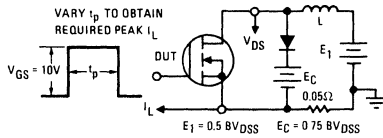


Fig. 15 – Clamped Inductive Waveforms

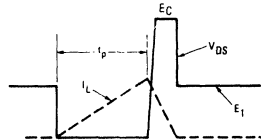


Fig. 16 – Switching Time Test Circuit

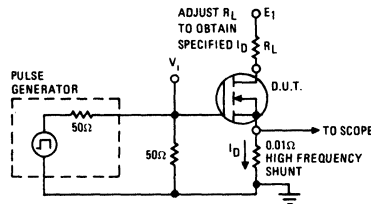
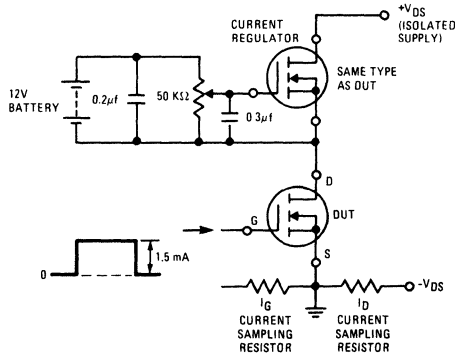


Fig. 17 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

UFND210
UFND213

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

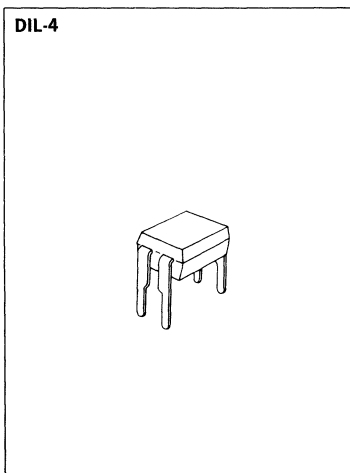
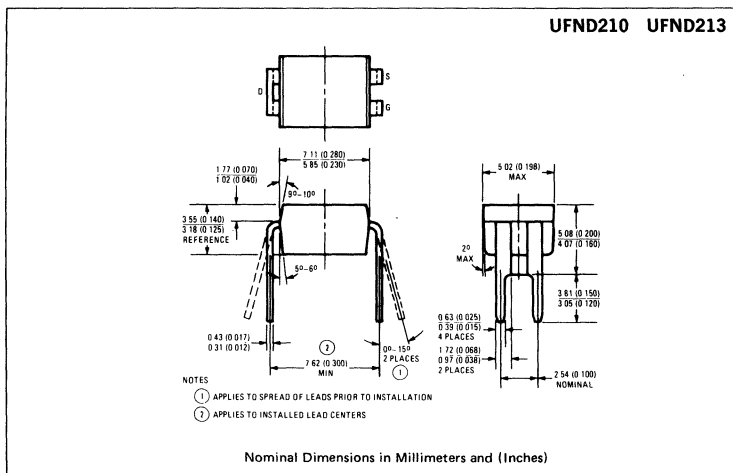
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND210	200V	1.5Ω	0.6A
UFND213	150V	2.4Ω	0.45A

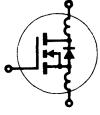
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFND210	UFND213	Units
V _{DS} Drain – Source Voltage ①	200	150	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	V
I _D @ T _A = 25°C Continuous Drain Current	0.6	0.45	A
I _{DM} Pulsed Drain Current	2.5	1.8	A
V _{GS} Gate – Source Voltage	± 20		V
P _D @ T _A = 25°C Max. Power Dissipation	1.0 (See Fig. 13)		W
Linear Derating Factor	0.008 (See Fig. 13)		W/K
I _{LM} Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH		A
	2.5	1.8	
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain – Source Breakdown Voltage	UFND210	200	–	–	V	V _{GS} = 0V	
	UFND213	150	–	–	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	–	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate – Source Leakage Forward	ALL	–	–	500	nA	V _{GS} = 20V	
I _{GSS} Gate – Source Leakage Reverse	ALL	–	–	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		–	–	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFND210	0.6	–	–	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
	UFND213	0.45	–	–	A		
R _{DS(on)} Static Drain – Source On-State Resistance ②	UFND210	–	1.0	1.5	Ω	V _{GS} = 10V, I _D = 0.3A	
	UFND213	–	1.5	2.4	Ω		
g _{fs} Forward Transconductance ②	ALL	0.5	0.8	–	S (Ψ)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 0.3A	
C _{iss} Input Capacitance	ALL	–	135	150	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 9	
C _{oss} Output Capacitance	ALL	–	60	80	pF		
C _{rss} Reverse Transfer Capacitance	ALL	–	16	25	pF		
t _{d(on)} Turn-On Delay Time	ALL	–	8.0	15	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 0.3A, Z _o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	–	15	25	ns		
t _{d(off)} Turn-Off Delay Time	ALL	–	10	15	ns		
t _f Fall Time	ALL	–	8.0	15	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V _{GS} = 10V, I _D = 2.5A, V _{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	–	2.0	–	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC		
L _D Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.	

THERMAL RESISTANCE

Parameter	ALL	Min.	Typ.	Max.	Units	Notes
R _{thJA} Junction-to-Ambient	ALL	–	–	120	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND210	—	—	0.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	
		UFND213	—	—	0.45	A		
I_{SM}	Pulse Source Current (Body Diode)	UFND210	—	—	2.5	A		
		UFND213	—	—	1.8	A		
V_{SD}	Diode Forward Voltage ②	UFND210	—	—	2.0	V		$T_A = 25^\circ\text{C}, I_S = 0.6\text{A}, V_{GS} = 0\text{V}$
		UFND213	—	—	1.8	V		$T_A = 25^\circ\text{C}, I_S = 0.45\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150^\circ\text{C}, I_F = 0.6\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 0.6\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Fig. 1 – Typical Output Characteristics

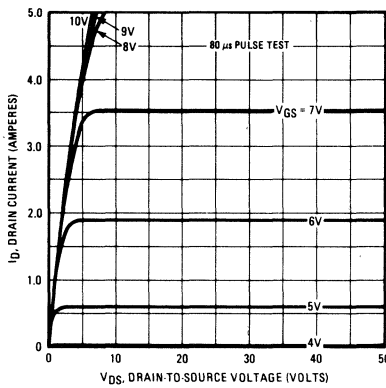


Fig. 2 – Typical Transfer Characteristics

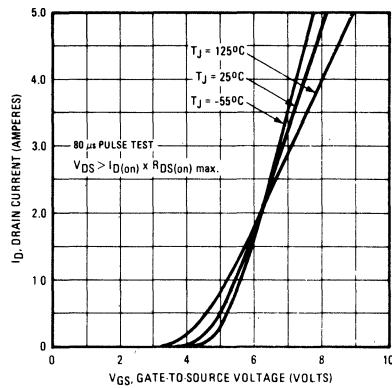


Fig. 3 – Typical Saturation Characteristics

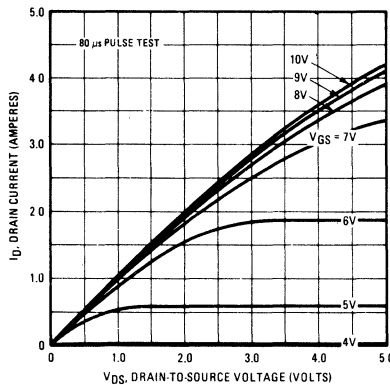


Fig. 4 – Maximum Safe Operating Area

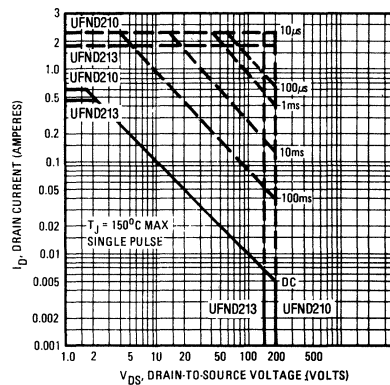


Fig. 5 – Typical Transconductance Vs. Drain Current

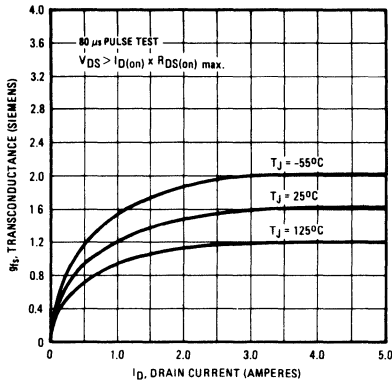


Fig. 6 – Typical Source-Drain Diode Forward Voltage

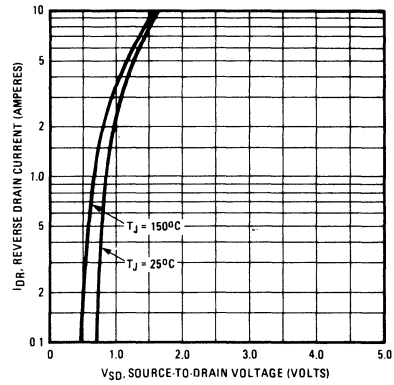


Fig. 7 – Breakdown Voltage Vs. Temperature

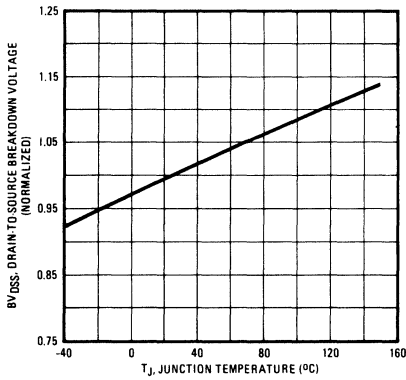


Fig. 8 – Normalized On-Resistance Vs. Temperature

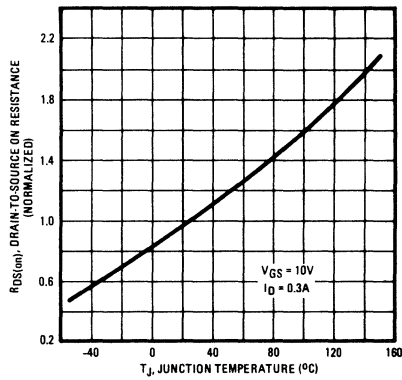


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

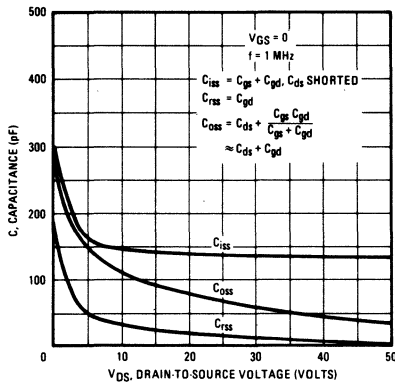


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

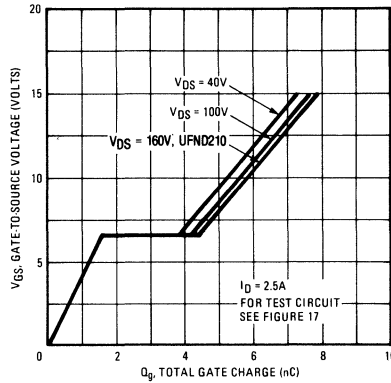


Fig. 11 – Typical On-Resistance Vs. Drain Current

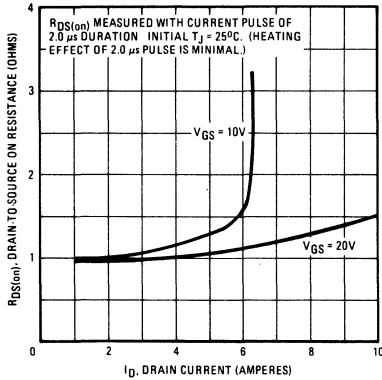


Fig. 12 – Maximum Drain Current Vs. Case Temperature

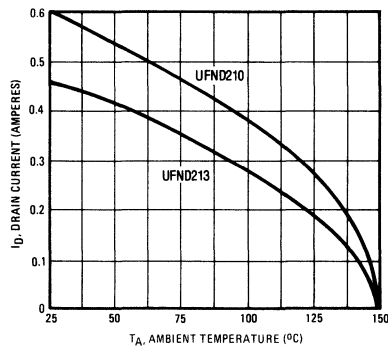


Fig. 13 – Power Vs. Temperature Derating Curve

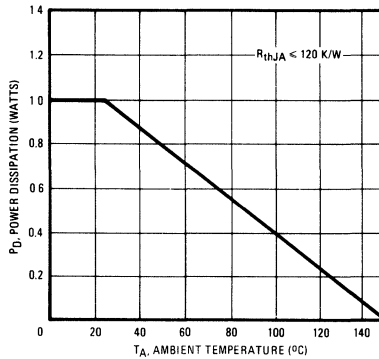


Fig. 14 – Clamped Inductive Test Circuit

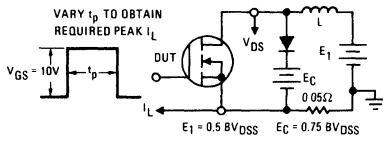


Fig. 15 – Clamped Inductive Waveforms

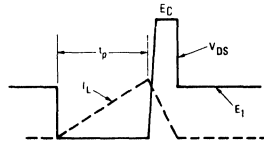


Fig. 16 – Switching Time Test Circuit

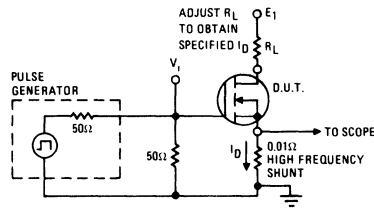
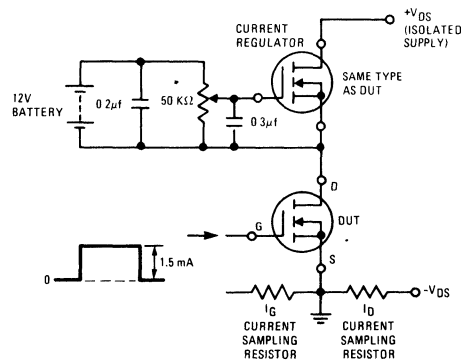


Fig. 17 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.60 Ohm
N-Channel

UFNF110
UFNF111
UFNF112
UFNF113

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

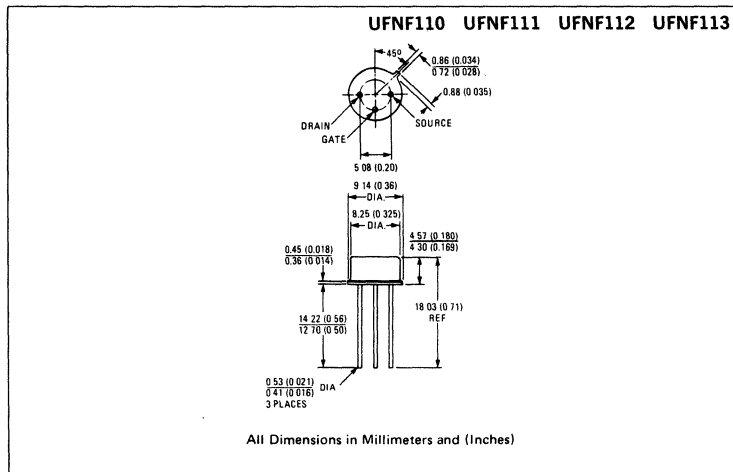
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

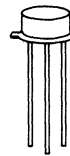
PRODUCT SUMMARY

Part Number	V _{bs}	R _{DS(on)}	I _D
UFNF110	100V	0.6Ω	3.5A
UFNF111	60V	0.6Ω	3.5A
UFNF112	100V	0.8Ω	3.0A
UFNF113	60V	0.8Ω	3.0A

MECHANICAL SPECIFICATIONS



TO-205AD (TO-39)

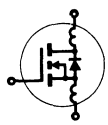


ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF110	UFNF111	UFNF112	UFNF113	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM} Pulsed Drain Current ③	14	14	12	12	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFNF110 UFNF112	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF111 UFNF113	60	—	—	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF110 UFNF111	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFNF112 UFNF113	3.0	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFNF110 UFNF111	—	0.5	0.6	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$	
	UFNF112 UFNF113	—	0.6	0.8	Ω		
g_{fs} Forward Transconductance ②	ALL	1.0	1.5	—	S (①)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 1.5\text{A}$	
C_{iss} Input Capacitance	ALL	—	135	200	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	80	100	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	20	25	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	10	20	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 1.5\text{A}$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	15	25	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	15	25	ns		
t_f Fall Time	ALL	—	10	20	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	$V_{GS} = 10\text{V}$, $I_D = 8.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	2.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	8.33	K/W	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF110	-	-	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF111	-	-	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF110	-	-	14	A	
		UFNF111	-	-	12	A	
V_{SD}	Diode Forward Voltage ②	UFNF110	-	-	2.5	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$
		UFNF111	-	-	2.0	V	
t_{rr}	Reverse Recovery Time	ALL	-	200	-	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	-	1.0	-	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

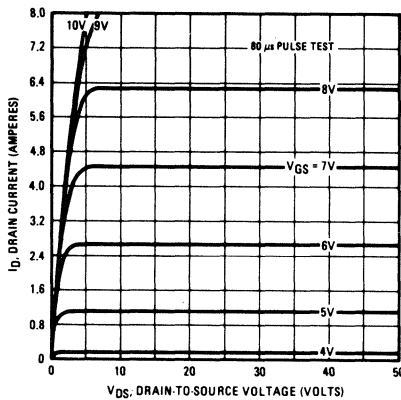


Fig. 2 – Typical Transfer Characteristics

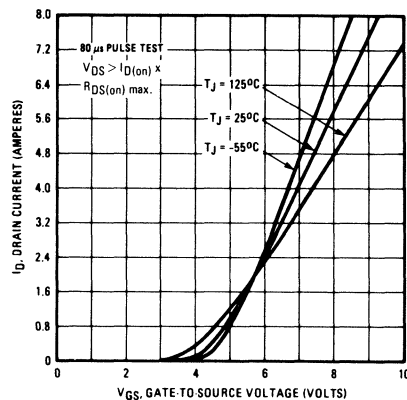


Fig. 3 – Typical Saturation Characteristics

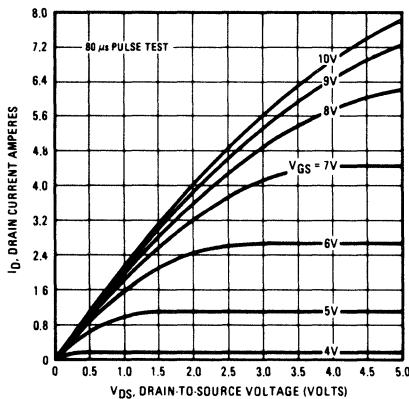


Fig. 4 – Maximum Safe Operating Area

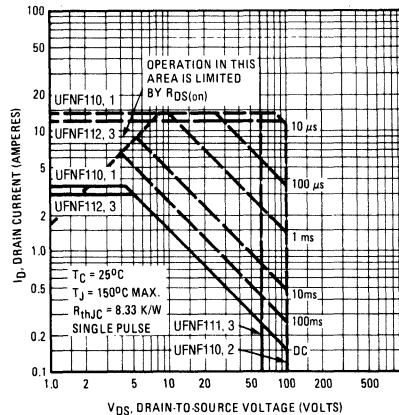
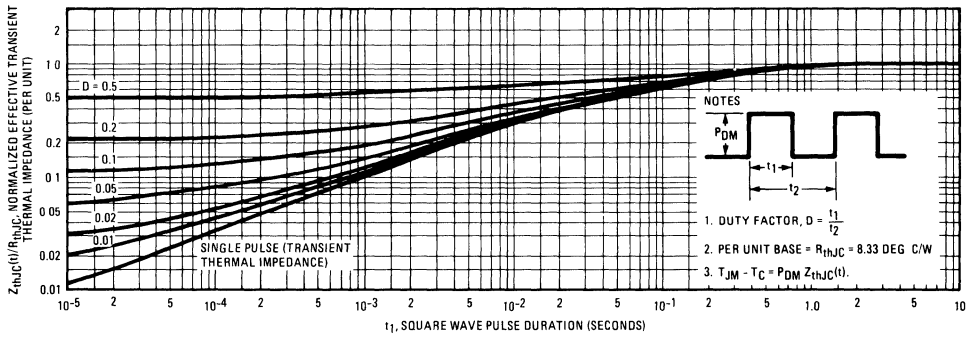


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

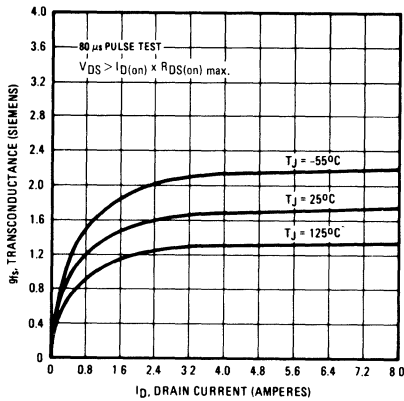


Fig. 7 – Typical Source-Drain Diode Forward Voltage

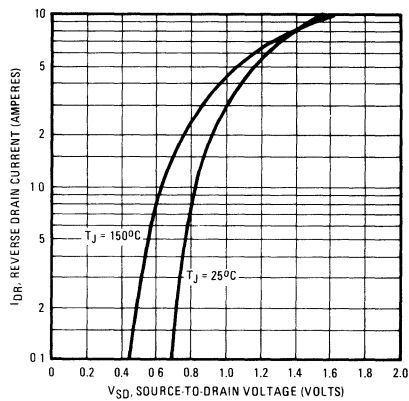


Fig. 8 – Breakdown Voltage Vs. Temperature

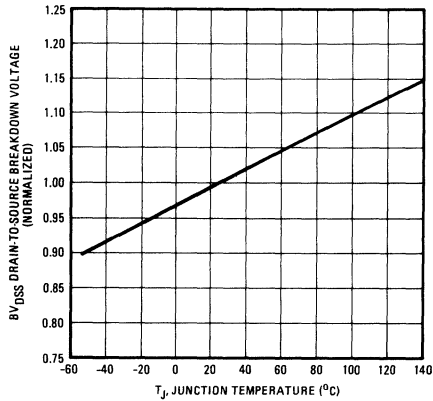


Fig. 9 – Normalized On-Resistance Vs. Temperature

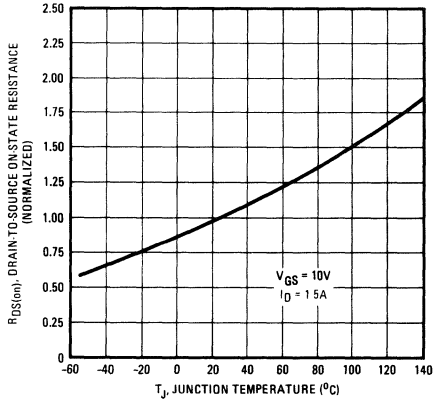


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

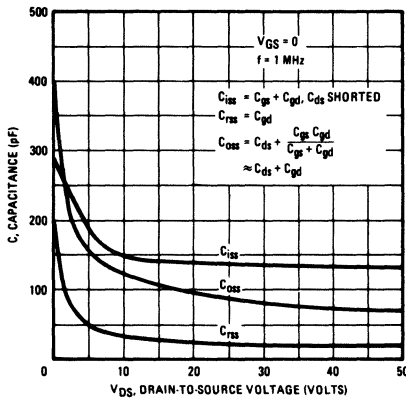


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

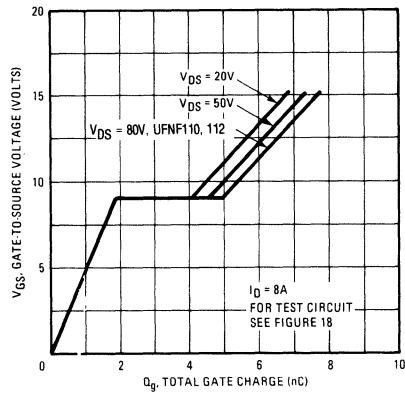


Fig. 12 — Typical On-Resistance Vs. Drain Current

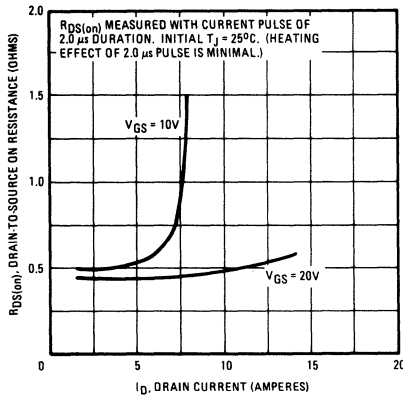


Fig. 13 — Maximum Drain Current Vs. Case Temperature

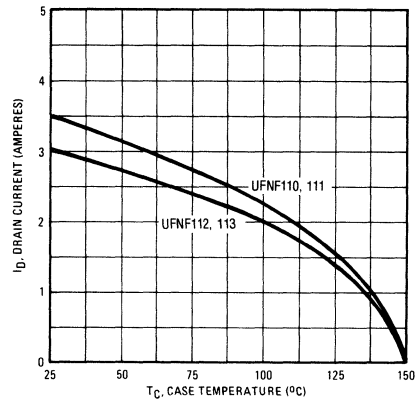


Fig. 14 — Power Vs. Temperature Derating Curve

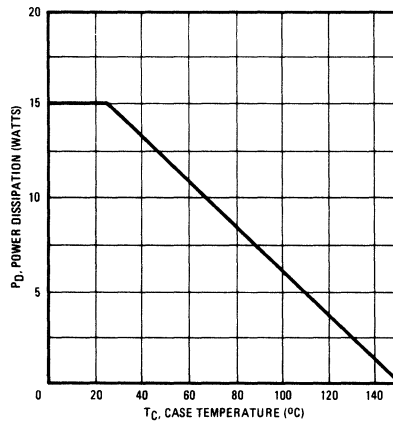


Fig. 15 — Clamped Inductive Test Circuit

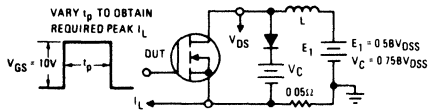


Fig. 16 — Clamped Inductive Waveforms

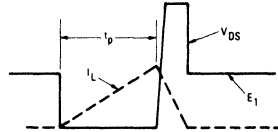


Fig. 17 — Switching Time Test Circuit

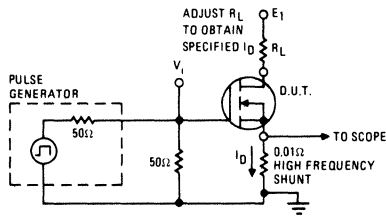
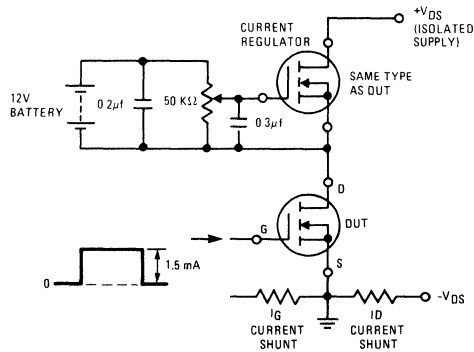


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.30 Ohm
N-Channel

UFNF120
UFNF121
UFNF122
UFNF123

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

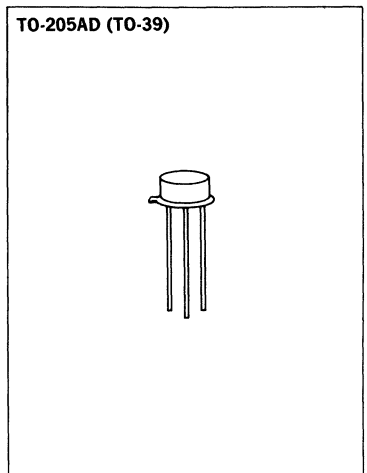
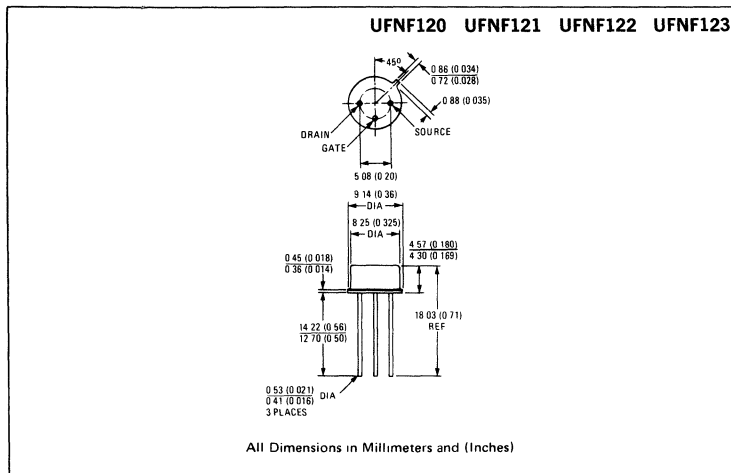
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF120	100V	0.30 Ω	6.0A
UFNF121	60V	0.30 Ω	6.0A
UFNF122	100V	0.40 Ω	5.0A
UFNF123	60V	0.40 Ω	5.0A

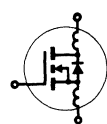
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF120	UFNF121	UFNF122	UFNF123	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	6.0	6.0	5.0	5.0	A
I _{DM} Pulsed Drain Current ③	24	24	20	20	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFNF120 UFNF122	100	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFNF121 UFNF123	60	—	—	V		
	ALL	2.0	—	4.0	V		V _{DS} = V _{GS} , I _D = 250μA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFNF120 UFNF121	6.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
	UFNF122 UFNF123	5.0	—	—	A		
	ALL	—	0.25	0.30	Ω		V _{GS} = 10V, I _D = 3.0A
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFNF120 UFNF121	—	0.25	0.30	Ω	V _{GS} = 10V, I _D = 3.0A	
UFNF122 UFNF123	—	0.30	0.40	Ω			
ALL	1.5	2.9	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 3.0A		
g _{fs} Forward Transconductance ②	ALL	1.5	2.9	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 3.0A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	200	400	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	50	100	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 3.0A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	37	70	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	35	70	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC		V _{GS} = 10V, I _D = 10A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	6.25	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF120	—	—	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF122 UFNF123	—	—	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF120	—	—	24	A	
		UFNF122 UFNF123	—	—	20	A	
V_{SD}	Diode Forward Voltage ②	UFNF120	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 6.0\text{A}, V_{GS} = 0\text{V}$
		UFNF122 UFNF123	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 5.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	$T_J = 150^\circ\text{C}, I_F = 6.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.2	—	μC	$T_J = 150^\circ\text{C}, I_F = 6.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

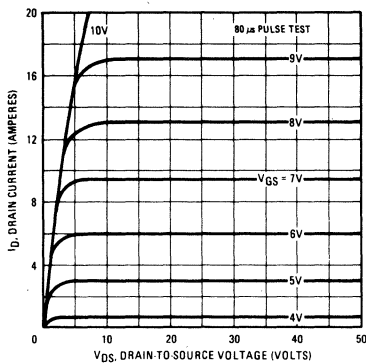


Fig. 3 – Typical Saturation Characteristics

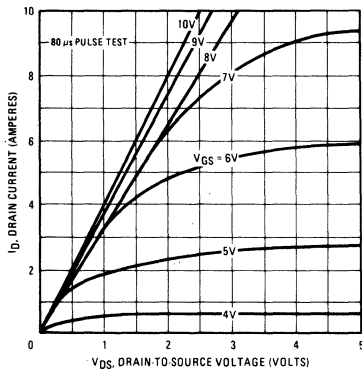


Fig. 2 – Typical Transfer Characteristics

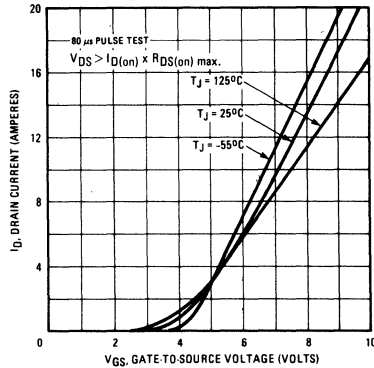


Fig. 4 – Maximum Safe Operating Area

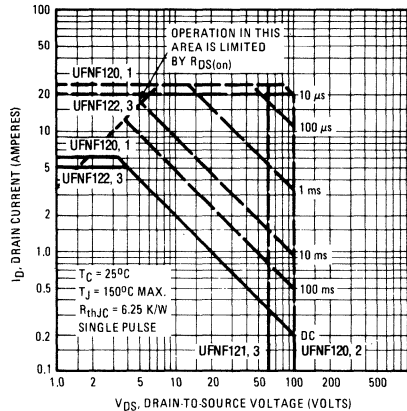


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

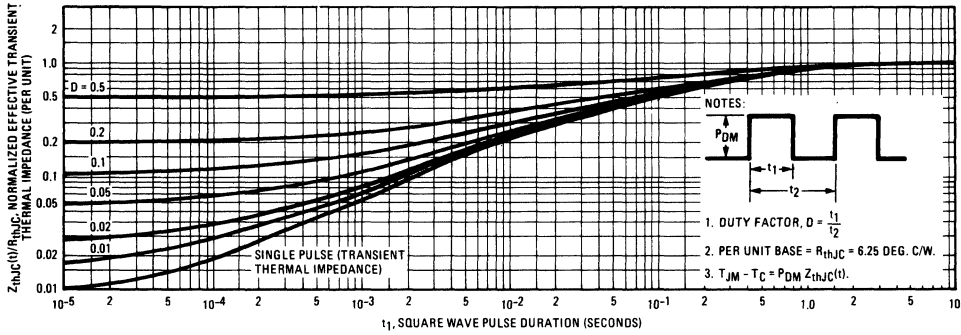


Fig. 6 – Typical Transconductance Vs. Drain Current

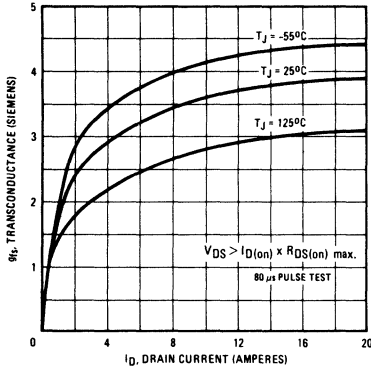


Fig. 7 – Typical Source-Drain Diode Forward Voltage

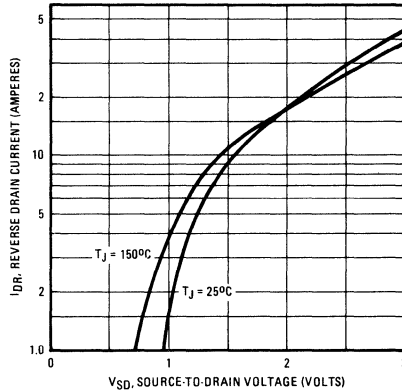


Fig. 8 – Breakdown Voltage Vs. Temperature

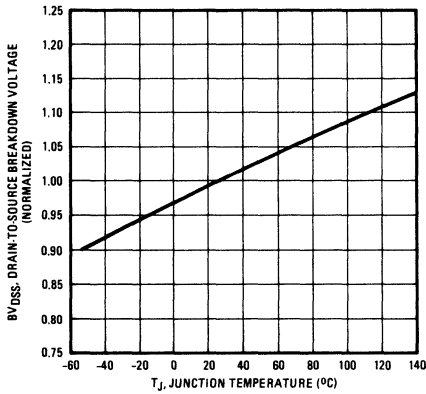


Fig. 9 – Normalized On-Resistance Vs. Temperature

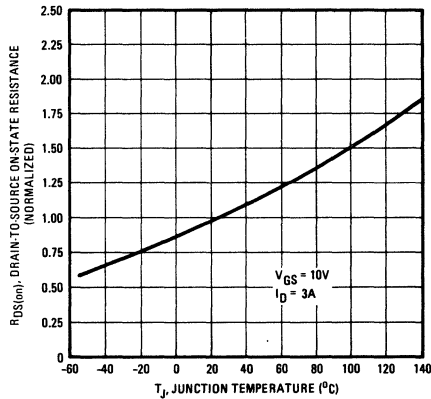


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

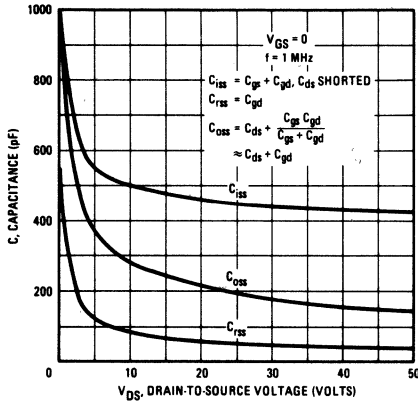


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

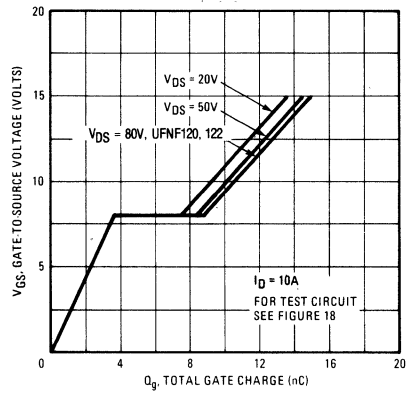


Fig. 12 – Typical On-Resistance Vs. Drain Current

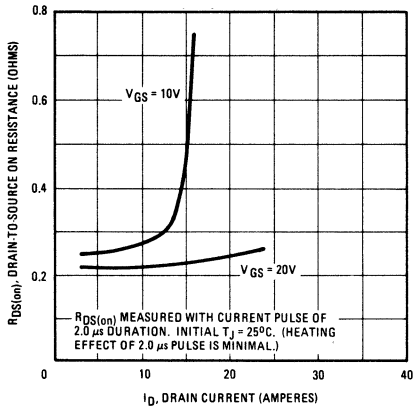


Fig. 13 – Maximum Drain Current Vs. Case Temperature

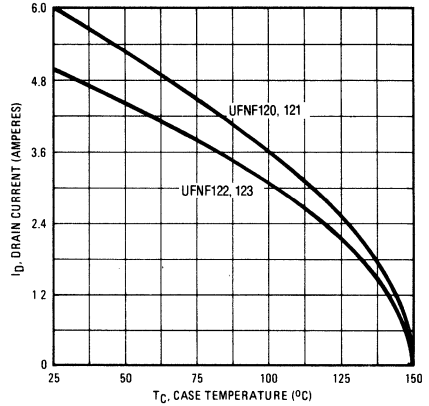


Fig. 14 – Power Vs. Temperature Derating Curve

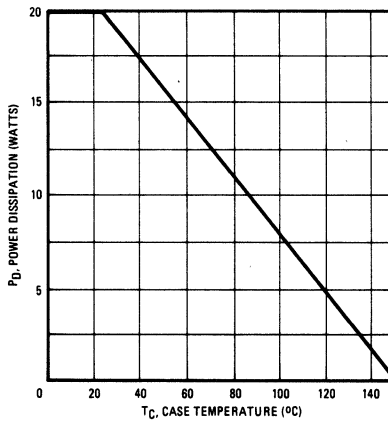


Fig. 15 – Clamped Inductive Test Circuit

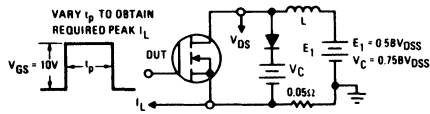


Fig. 16 – Clamped Inductive Waveforms

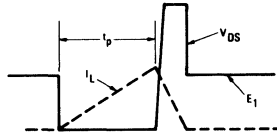


Fig. 17 – Switching Time Test Circuit

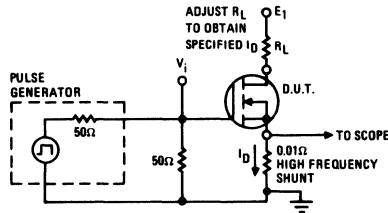
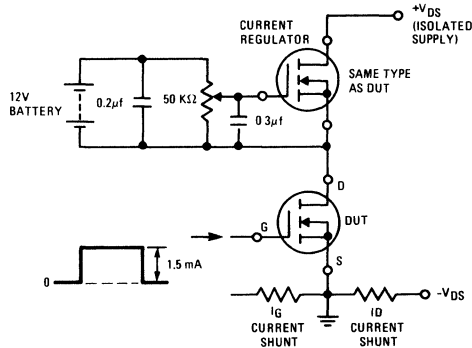


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFNF130
UFNF131
UFNF132
UFNF133

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

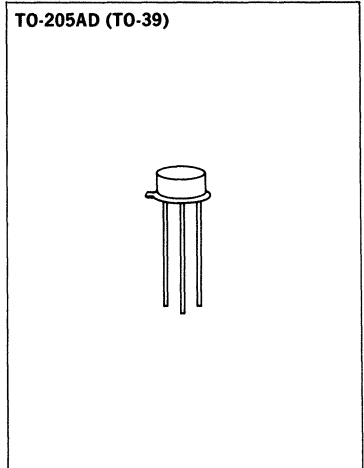
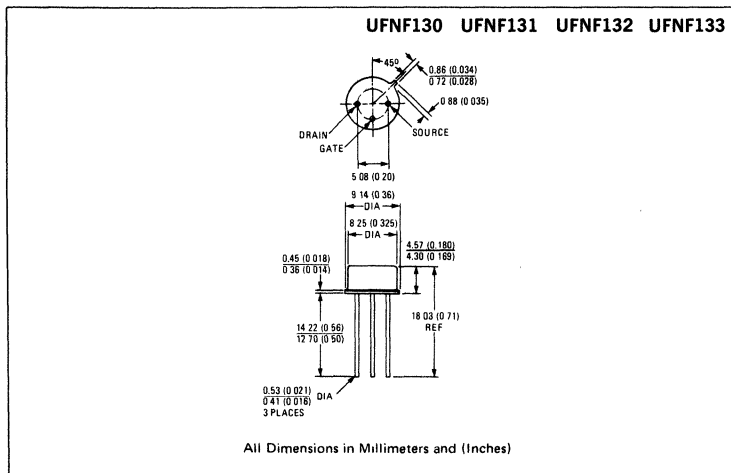
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF130	100V	0.18 Ω	8.0A
UFNF131	60V	0.18 Ω	8.0A
UFNF132	100V	0.25 Ω	7.0A
UFNF133	60V	0.25 Ω	7.0A

MECHANICAL SPECIFICATIONS

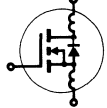


ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF130	UFNF131	UFNF132	UFNF133	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM} Pulsed Drain Current ③	32	32	28	28	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	25 (See Fig. 14)				W
Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFNF130 UFNF132	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF131 UFNF133	60	—	—	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF130 UFNF131	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFNF132 UFNF133	7.0	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFNF130 UFNF131	—	0.14	0.18	Ω	$V_{GS} = 10\text{V}$, $I_D = 4.0\text{A}$	
	UFNF132 UFNF133	—	0.20	0.25	Ω		
g_{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (V)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 4.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	600	800	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$	
C_{oss} Output Capacitance	ALL	—	300	500	pF	See Fig. 10	
C_{rss} Reverse Transfer Capacitance	ALL	—	100	150	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	30	50	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 4.0\text{A}$, $Z_o = 50\Omega$	
t_r Rise Time	ALL	—	80	150	ns	See Fig. 17	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t_f Fall Time	ALL	—	80	150	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	$V_{GS} = 10\text{V}$, $I_D = 18\text{A}$, $V_{DS} = 0.8\text{Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	9.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	5.0	K/W	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF130 UFNF131	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF132 UFNF133	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF130 UFNF131	—	—	32	A	
		UFNF132 UFNF133	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFNF130 UFNF131	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
		UFNF132 UFNF133	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 7.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	f.LL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

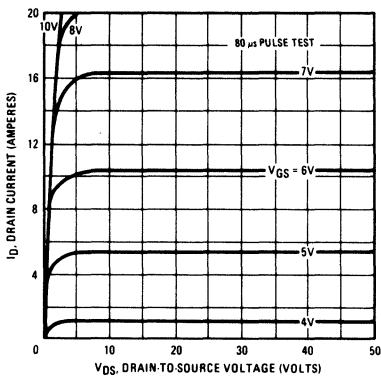


Fig. 2 – Typical Transfer Characteristics

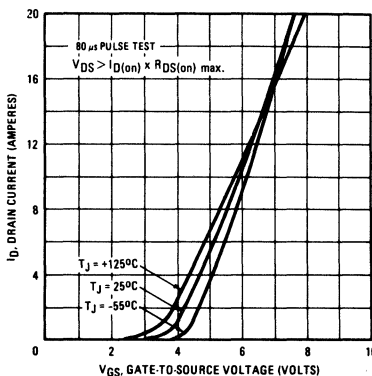


Fig. 3 – Typical Saturation Characteristics

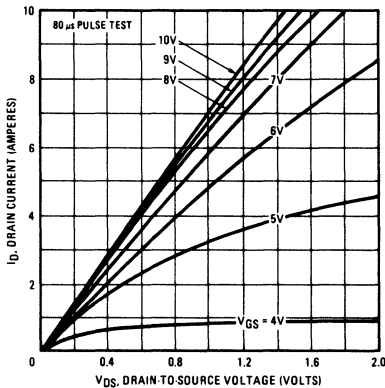


Fig. 4 – Maximum Safe Operating Area

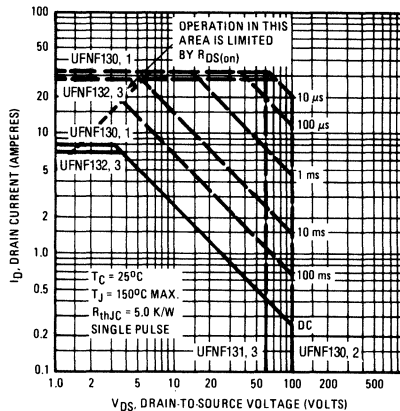


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

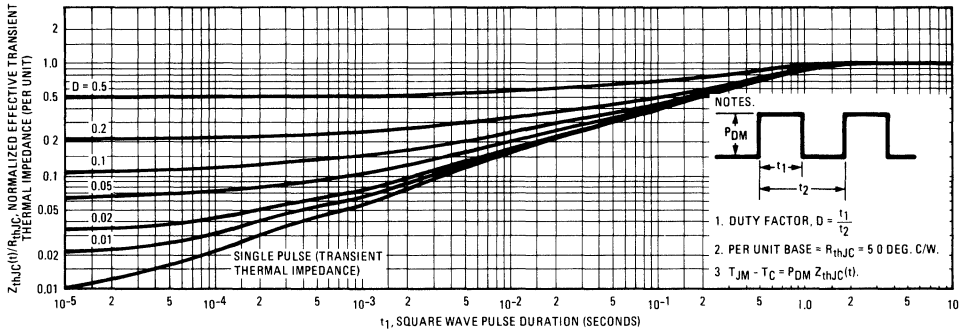


Fig. 6 – Typical Transconductance Vs. Drain Current

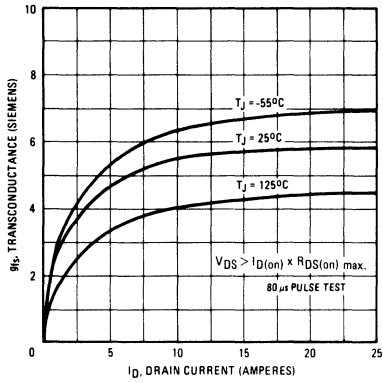


Fig. 8 – Breakdown Voltage Vs. Temperature

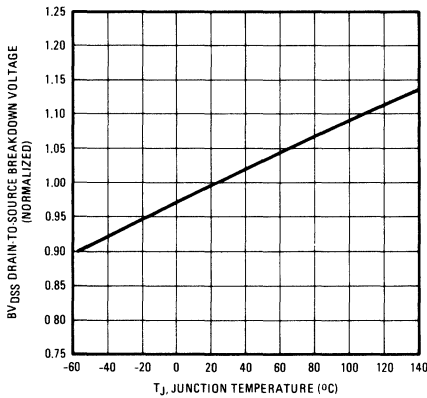


Fig. 7 – Typical Source-Drain Diode Forward Voltage

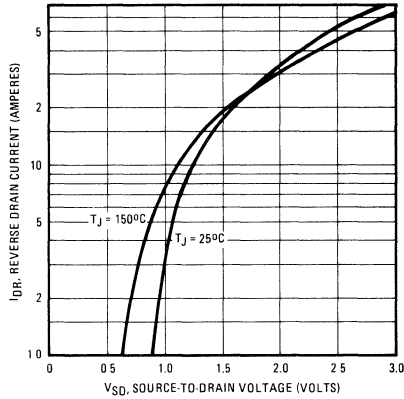


Fig. 9 – Normalized On-Resistance Vs. Temperature

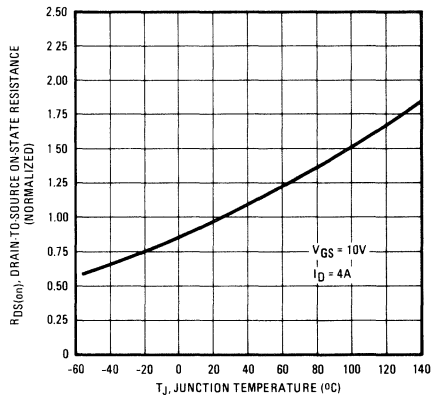


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

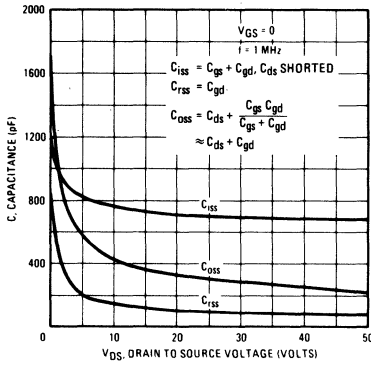


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

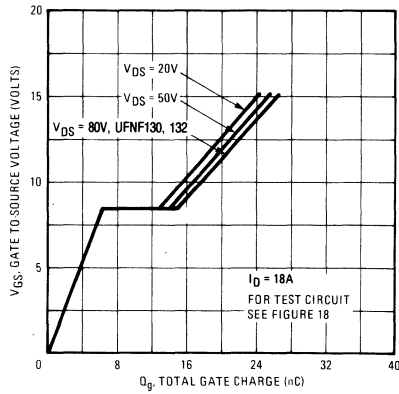


Fig. 12 – Typical On-Resistance Vs. Drain Current

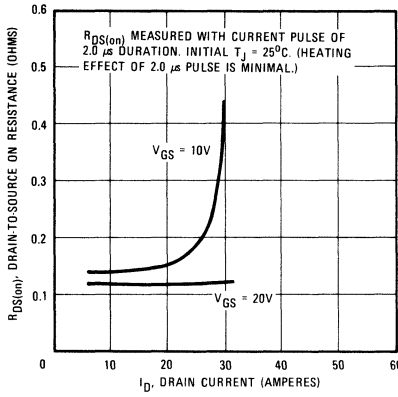


Fig. 13 – Maximum Drain Current Vs. Case Temperature

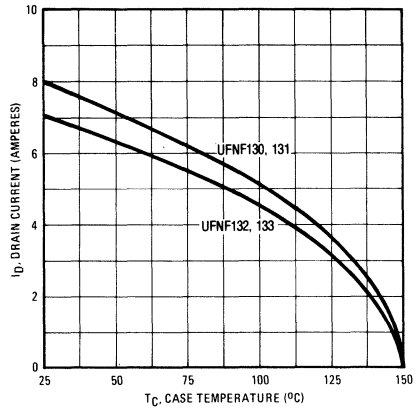


Fig. 14 – Power Vs. Temperature Derating Curve

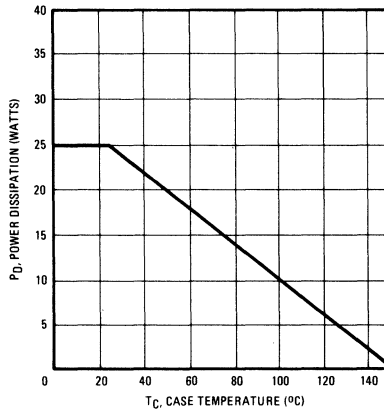


Fig. 15 — Clamped Inductive Test Circuit

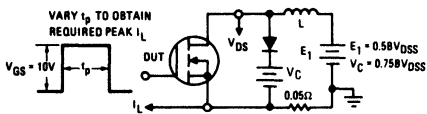


Fig. 16 — Clamped Inductive Waveforms

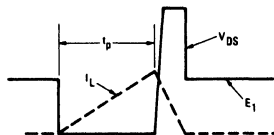


Fig. 17 — Switching Time Test Circuit

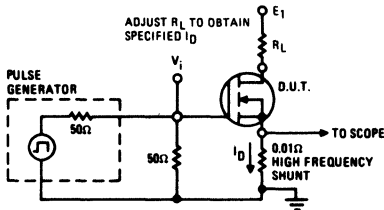
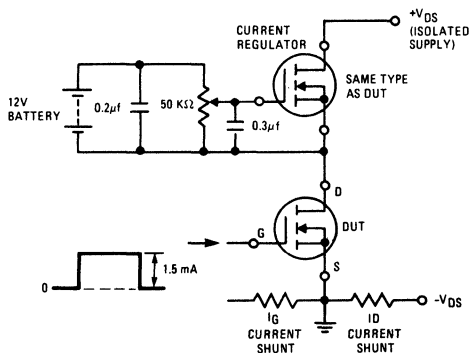


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

UFNF210
UFNF211
UFNF212
UFNF213

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

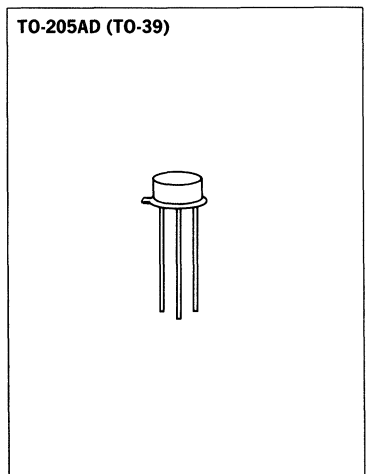
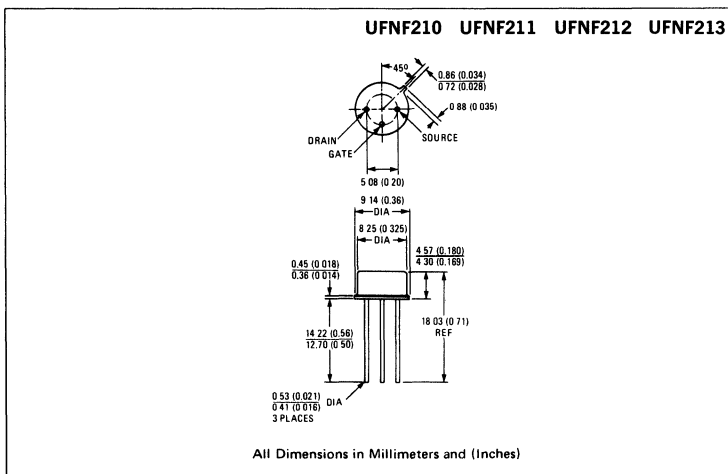
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF210	200V	1.5Ω	2.2A
UFNF211	150V	1.5Ω	2.2A
UFNF212	200V	2.4Ω	1.8A
UFNF213	150V	2.4Ω	1.8A

MECHANICAL SPECIFICATIONS

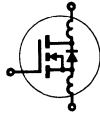


ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF210	UFNF211	UFNF212	UFNF213	Units
V_{DS} Drain – Source Voltage ①	200	150	200	150	V
V_{DGR} Drain – Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	2.2	2.2	1.8	1.8	A
I_{DM} Pulsed Drain Current ③	9.0	9.0	7.5	7.5	A
V_{GS} Gate – Source Voltage					± 20
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain – Source Breakdown Voltage	UFNF210 UFNF212	200	–	–	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF211 UFNF213	150	–	–	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate – Source Leakage Forward	ALL	–	–	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate – Source Leakage Reverse	ALL	–	–	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$ $V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
		–	–	1000	μA		
$I_{D(on)}$ On-State Drain Current ②	UFNF210 UFNF211	2.2	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFNF212 UFNF213	1.8	–	–	A		
$R_{DS(on)}$ Static Drain – Source On-State Resistance ②	UFNF210 UFNF211	–	1.0	1.5	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.25\text{A}$	
	UFNF212 UFNF213	–	1.5	2.4	Ω		
g_{fs} Forward Transconductance ②	ALL	0.8	1.3	–	S (②)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 1.25\text{A}$	
C_{iss} Input Capacitance	ALL	–	135	150	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	–	60	80	pF		
C_{rss} Reverse Transfer Capacitance	ALL	–	16	25	pF		
$t_d(on)$ Turn-On Delay Time	ALL	–	8.0	15	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 1.25\text{A}$, $Z_\theta = 50^\circ\text{C}$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	–	15	25	ns		
$t_d(off)$ Turn-Off Delay Time	ALL	–	10	15	ns		
t_f Fall Time	ALL	–	8.0	15	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	$V_{GS} = 10\text{V}$, $I_D = 4.5\text{A}$, $V_{DS} = 0.8\text{V Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	–	2.0	–	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC		
L_D Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	–	–	8.33	K/W	
R_{thJA} Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S	Continuous Source Current (Body Diode)	UFNF210 UFNF211	—	—	2.2	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF212 UFNF213	—	—	1.8	A	
I _{SM}	Pulse Source Current (Body Diode) ③	UFNF210 UFNF211	—	—	9.0	A	
		UFNF212 UFNF213	—	—	7.5	A	
V _{SD}	Diode Forward Voltage ②	UFNF210 UFNF211	—	—	2.0	V	T _C = 25°C, I _S = 2.2A, V _{GS} = 0V
		UFNF212 UFNF213	—	—	1.8	V	T _C = 25°C, I _S = 1.8A, V _{GS} = 0V
t _{rr}	Reverse Recovery Time	ALL	—	290	—	ns	T _J = 150°C, I _F = 2.2A, dI _F /dt = 100A/μs
Q _{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T _J = 150°C, I _F = 2.2A, dI _F /dt = 100A/μs
t _{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

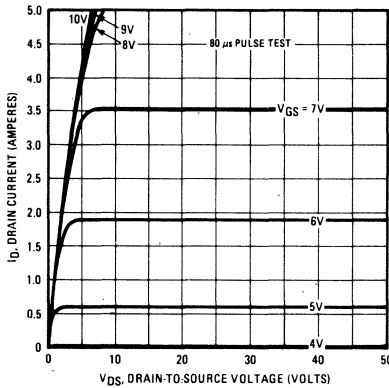


Fig. 2 – Typical Transfer Characteristics

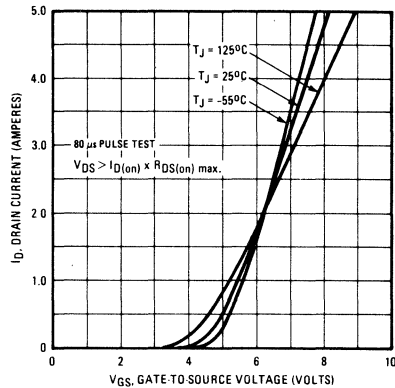


Fig. 3 – Typical Saturation Characteristics

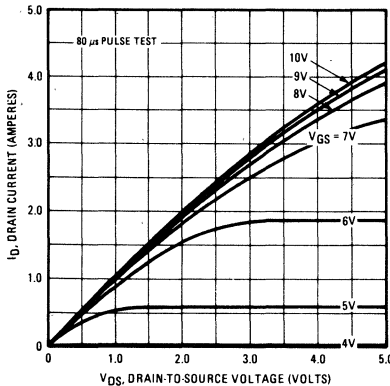


Fig. 4 – Maximum Safe Operating Area

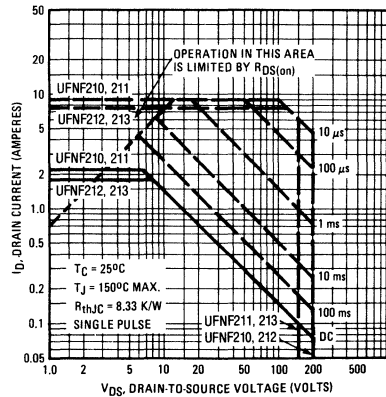


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

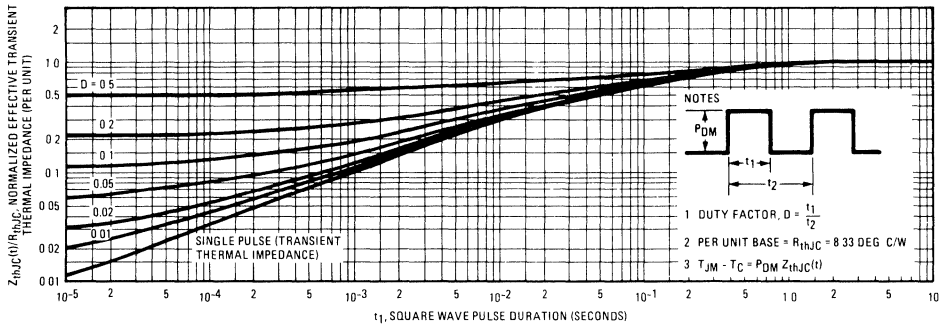


Fig. 6 – Typical Transconductance Vs. Drain Current

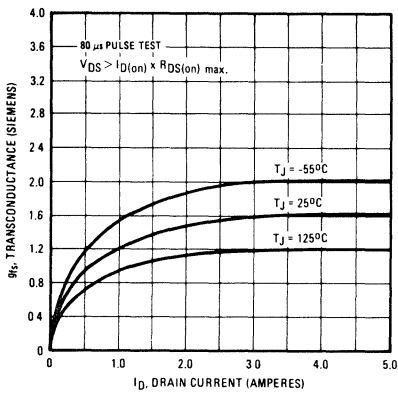


Fig. 7 – Typical Source-Drain Diode Forward Voltage

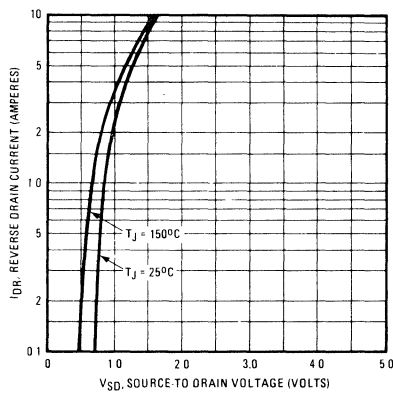


Fig. 8 – Breakdown Voltage Vs. Temperature

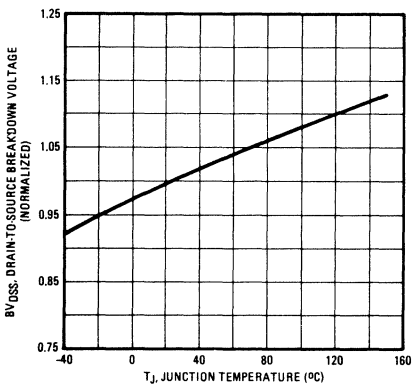


Fig. 9 – Normalized On-Resistance Vs. Temperature

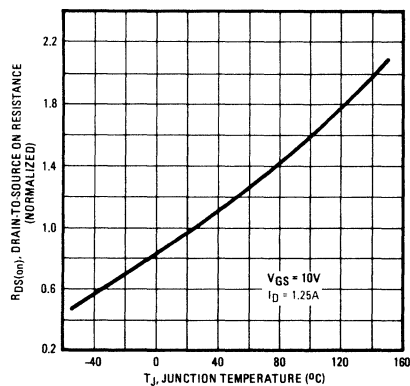


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

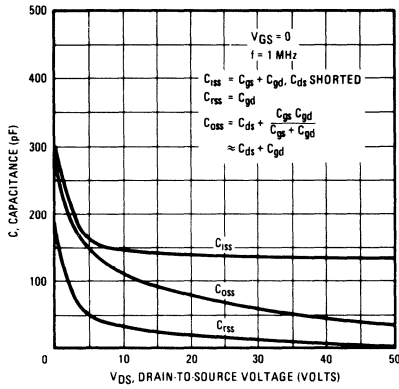


Fig. 12 – Typical On-Resistance Vs. Drain Current

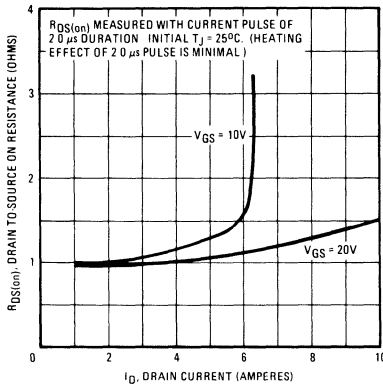


Fig. 14 – Power Vs. Temperature Derating Curve

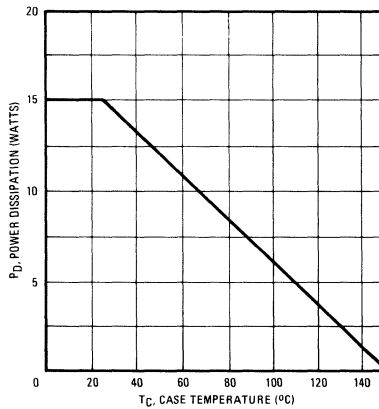


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

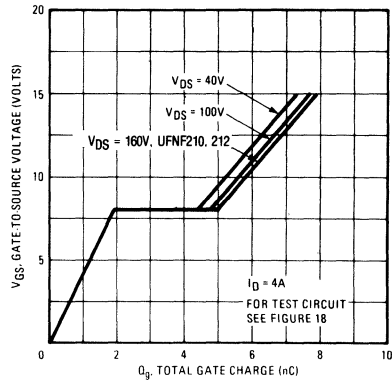


Fig. 13 – Maximum Drain Current Vs. Case Temperature

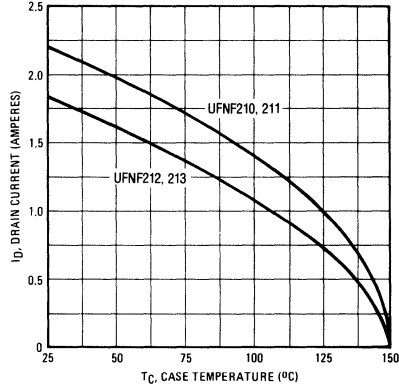


Fig. 15 – Clamped Inductive Test Circuit

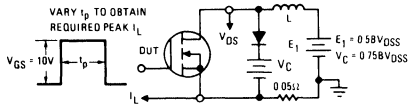


Fig. 16 – Clamped Inductive Waveforms

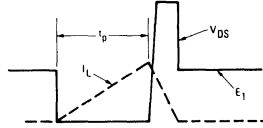


Fig. 17 – Switching Time Test Circuit

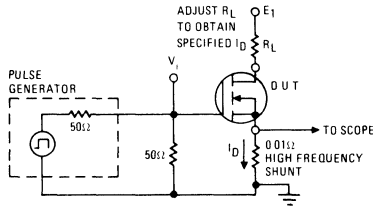
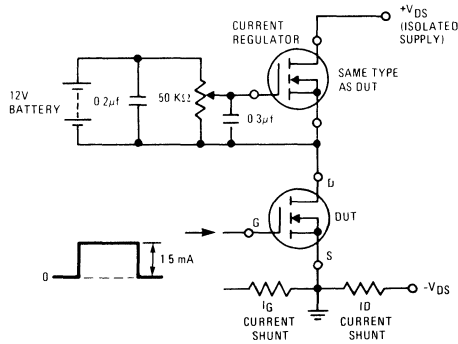


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.8 Ohm
N-Channel

UFNF220
UFNF221
UFNF222
UFNF223

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

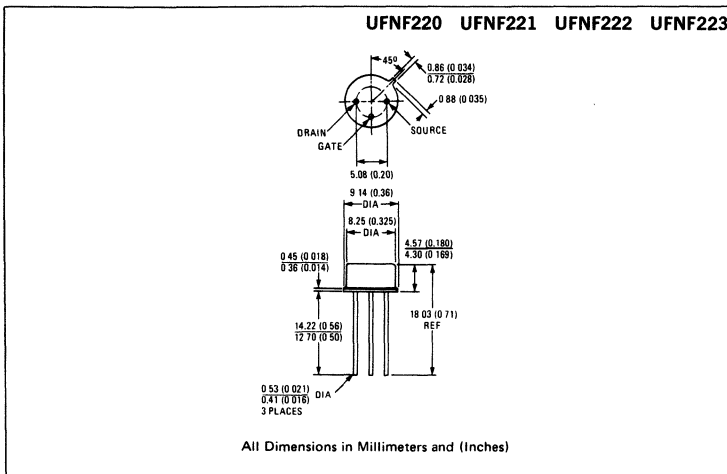
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

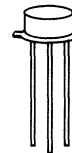
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF220	200V	0.8Ω	3.5A
UFNF221	150V	0.8Ω	3.5A
UFNF222	200V	1.2Ω	3.0A
UFNF223	150V	1.2Ω	3.0A

MECHANICAL SPECIFICATIONS



TO-205AD (TO-39)

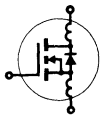


ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF220	UFNF221	UFNF222	UFNF223	Units
V_{DS} Drain – Source Voltage ①	200	150	200	150	V
V_{DGR} Drain – Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM} Pulsed Drain Current ③	14	14	12	12	A
V_{GS} Gate – Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain – Source Breakdown Voltage	UFNF220 UFNF222	200	–	–	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF221 UFNF223	150	–	–	V		
	ALL	–	–	–	–		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate – Source Leakage Forward	ALL	–	–	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate – Source Leakage Reverse	ALL	–	–	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		–	–	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF220 UFNF221	3.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFNF222 UFNF223	3.0	–	–	A		
	ALL	–	–	–	–		
$R_{DS(on)}$ Static Drain – Source On-State Resistance ②	UFNF220 UFNF221	–	0.5	0.8	Ω	$V_{GS} = 10\text{V}$, $I_D = 2.0\text{A}$	
	UFNF222 UFNF223	–	0.8	1.2	Ω		
	ALL	–	–	–	–		
g_{fs} Forward Transconductance ②	ALL	1.5	2.25	–	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 2.0\text{A}$	
C_{iss} Input Capacitance	ALL	–	450	600	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	–	150	300	pF		
C_{rss} Reverse Transfer Capacitance	ALL	–	40	80	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	–	20	40	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 2.0\text{A}$, $Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	–	30	60	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	–	50	100	ns		
t_f Fall Time	ALL	–	30	60	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	$V_{GS} = 10\text{V}$, $I_D = 7.0\text{A}$, $V_{DS} = 0.8\text{V Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	–	5.0	–	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC		
L_D Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	–	–	6.25	K/W	
R_{thJA} Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF220	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF221	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF220	—	—	14	A	
		UFNF221	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	UFNF220	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$
		UFNF221	—	—	2.0	V	
		UFNF222	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

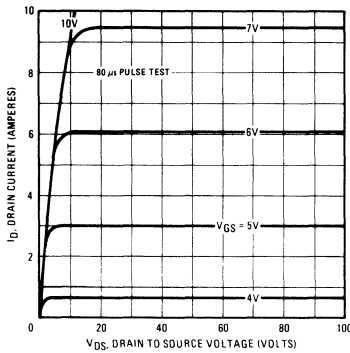


Fig. 2 – Typical Transfer Characteristics

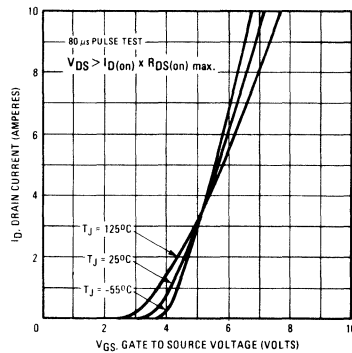


Fig. 3 – Typical Saturation Characteristics

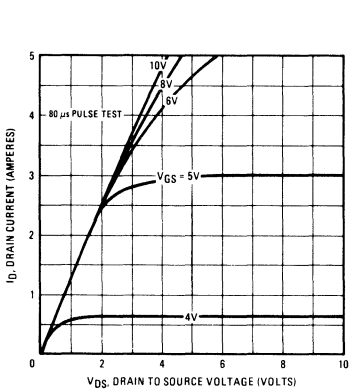


Fig. 4 – Maximum Safe Operating Area

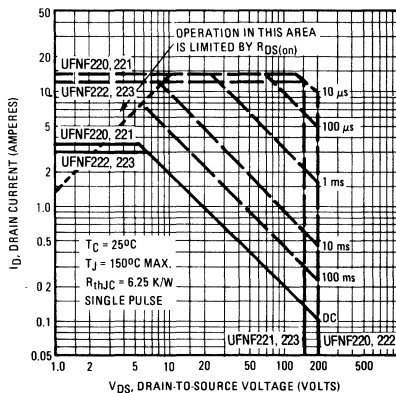


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

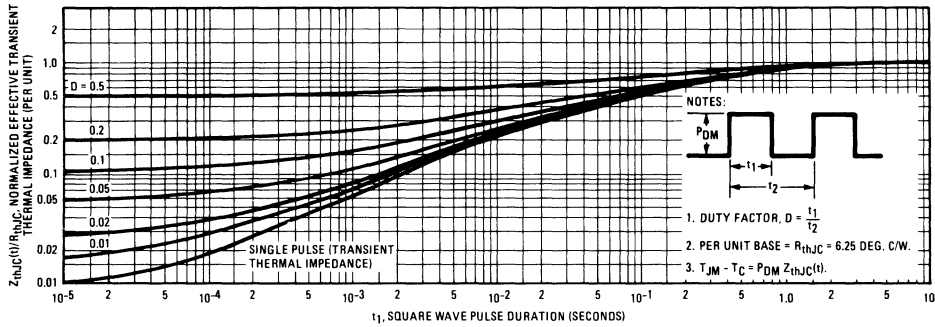


Fig. 6 – Typical Transconductance Vs. Drain Current

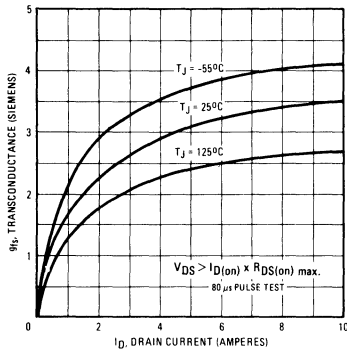


Fig. 7 – Typical Source-Drain Diode Forward Voltage

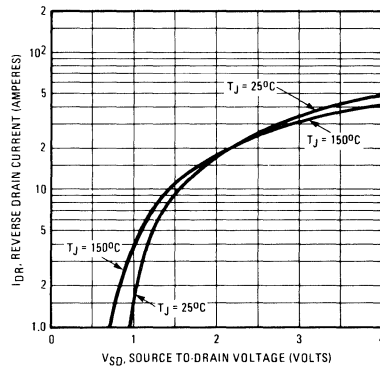


Fig. 8 – Breakdown Voltage Vs. Temperature

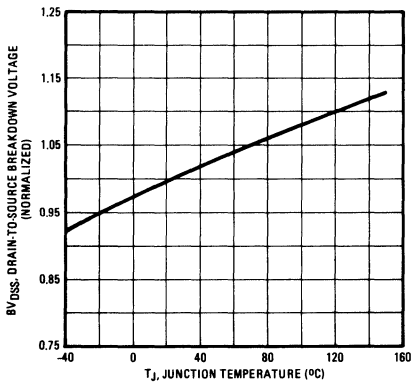


Fig. 9 – Normalized On-Resistance Vs. Temperature

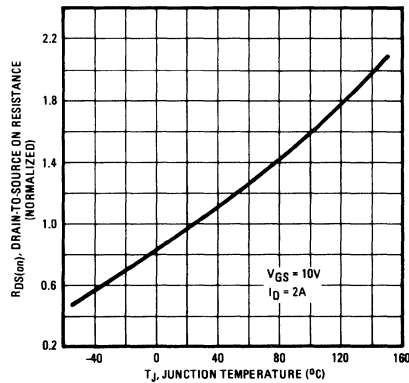


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

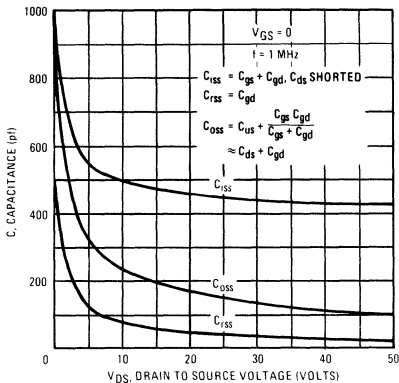


Fig. 12 — Typical On-Resistance Vs. Drain Current

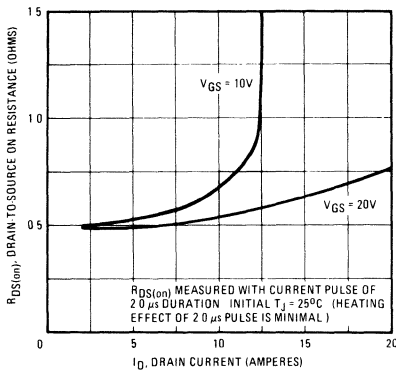


Fig. 14 — Power Vs. Temperature Derating Curve

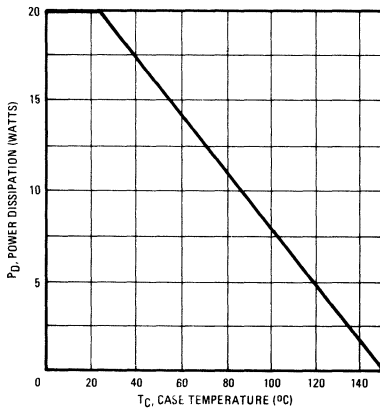


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

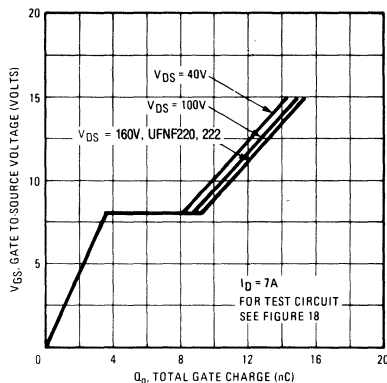


Fig. 13 — Maximum Drain Current Vs. Case Temperature

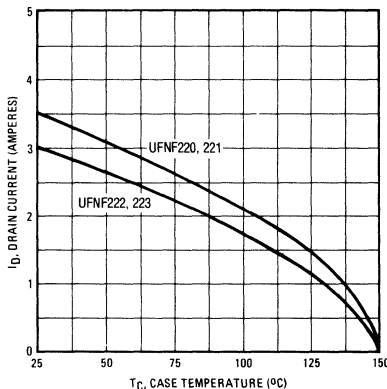


Fig. 15 – Clamped Inductive Test Circuit

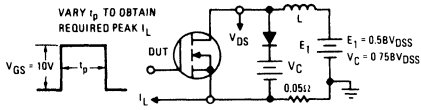
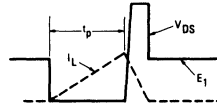


Fig. 16 – Clamped Inductive Waveforms



4

Fig. 17 – Switching Time Test Circuit

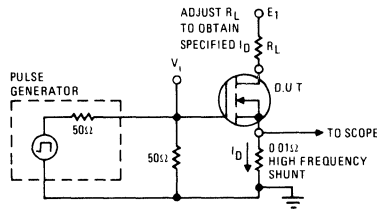
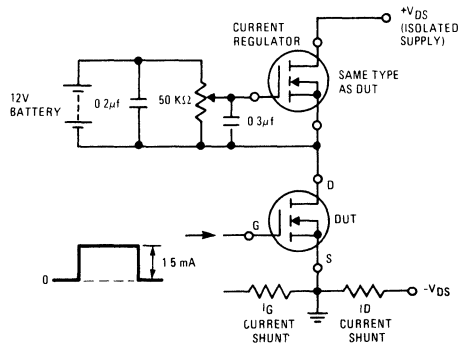


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm
N-Channel

UFNF230
UFNF231
UFNF232
UFNF233

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

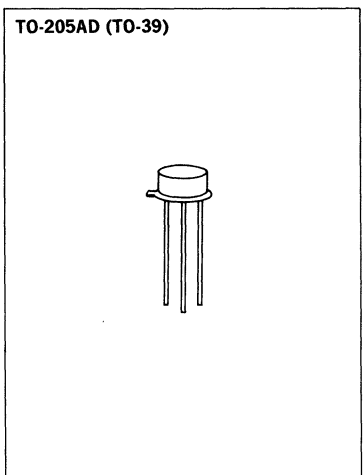
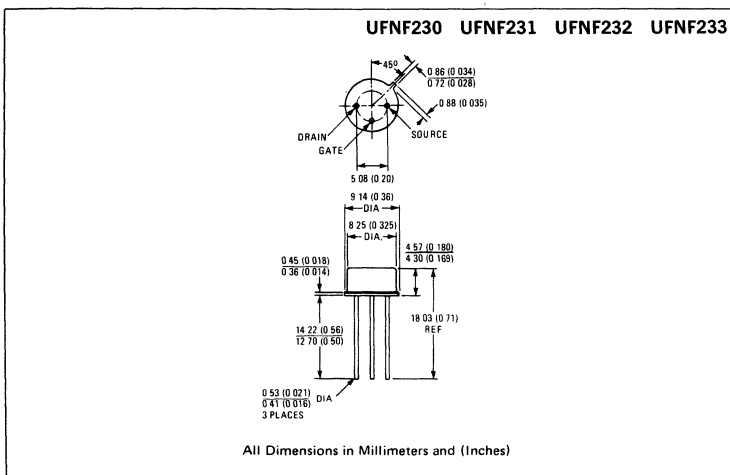
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF230	200V	0.4 Ω	5.5A
UFNF231	150V	0.4 Ω	5.5A
UFNF232	200V	0.6 Ω	4.5A
UFNF233	150V	0.6 Ω	4.5A

MECHANICAL SPECIFICATIONS



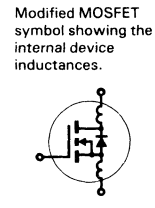


ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF230	UFNF231	UFNF232	UFNF233	Units
V _{DS} Drain – Source Voltage ①	200	150	200	150	V
V _{DGR} Drain – Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	5.5	5.5	4.5	4.5	A
I _{DM} Pulsed Drain Current ③	22	22	18	18	A
V _{GS} Gate – Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	25 (See Fig. 14)				W
Linear Derating Factor	0.2 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	22	22	18	18	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain – Source Breakdown Voltage	UFNF230 UFNF232	200	–	–	V	V _{GS} = 0V
	UFNF231 UFNF233	150	–	–	V	I _D = 250μA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	–	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate – Source Leakage Forward	ALL	–	–	100	nA	V _{GS} = 20V
I _{GSS} Gate – Source Leakage Reverse	ALL	–	–	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		–	–	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	UFNF230 UFNF231	5.5	–	–	A	V _{DS} > I _{D(on)} × R _{DS(on)} max.; V _{GS} = 10V
	UFNF232 UFNF233	4.5	–	–	A	
R _{DS(on)} Static Drain – Source On-State Resistance ②	UFNF230 UFNF231	–	0.25	0.4	Ω	V _{GS} = 10V, I _D = 3.0A
	UFNF232 UFNF233	–	0.4	0.6	Ω	
	ALL	–	–	–	–	
g _{fs} Forward Transconductance ②	ALL	2.5	4.5	–	S (∇)	V _{DS} > I _{D(on)} × R _{DS(on)} max.; I _D = 3.0A
C _{iss} Input Capacitance	ALL	–	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	–	250	450	pF	
C _{rss} Reverse Transfer Capacitance	ALL	–	80	150	pF	
t _{d(on)} Turn-On Delay Time	ALL	–	–	30	ns	V _{DD} = 90V, I _D = 3.0A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _r Rise Time	ALL	–	–	50	ns	
t _{d(off)} Turn-Off Delay Time	ALL	–	–	50	ns	
t _f Fall Time	ALL	–	–	40	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	
Q _{gs} Gate-Source Charge	ALL	–	10	–	nC	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
Q _{gd} Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L _D Internal Drain Inductance	ALL	–	5.0	–	nH	
L _S Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	–	–	5.0	K/W	
R _{thJA} Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF230	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF231	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF230	—	—	22	A	
		UFNF231	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	UFNF230	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 5.5\text{A}, V_{GS} = 0\text{V}$
		UFNF231	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

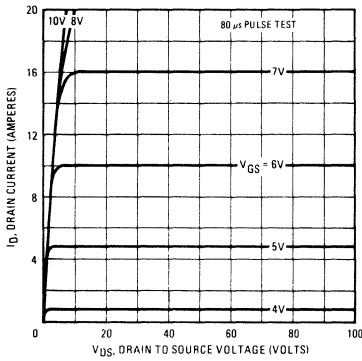


Fig. 2 – Typical Transfer Characteristics

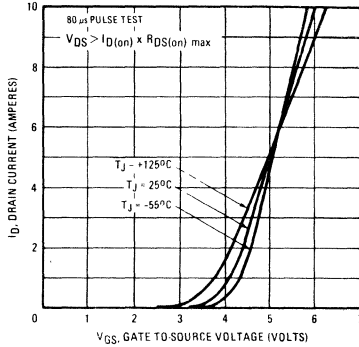


Fig. 3 – Typical Saturation Characteristics

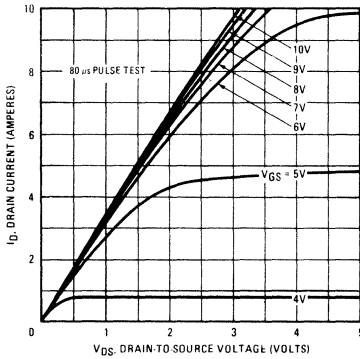


Fig. 4 – Maximum Safe Operating Area

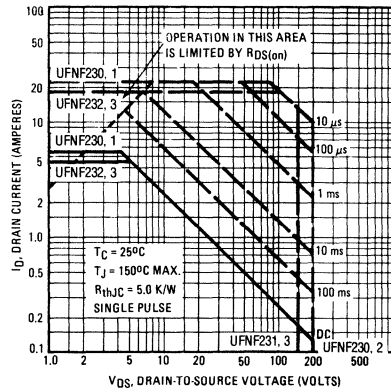
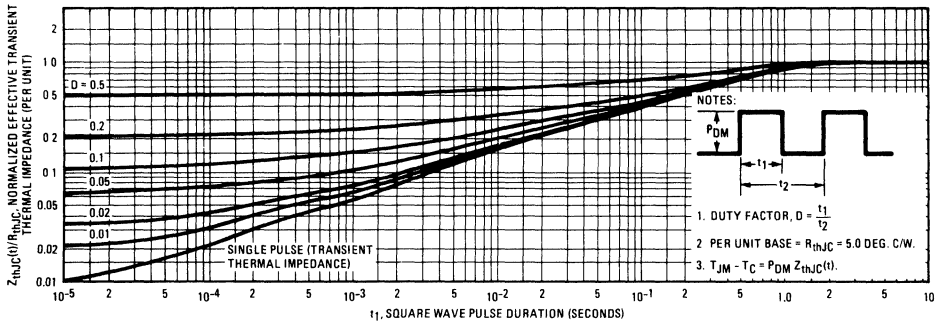


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 — Typical Transconductance Vs. Drain Current

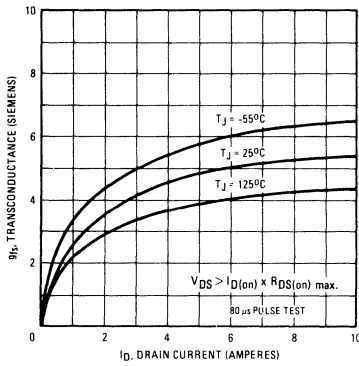


Fig. 7 — Typical Source-Drain Diode Forward Voltage

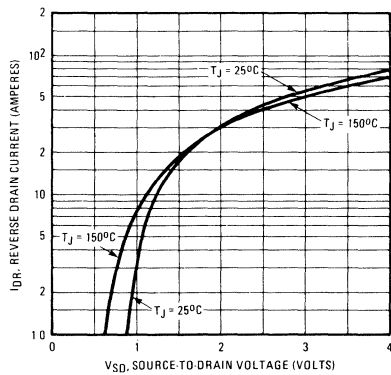


Fig. 8 — Breakdown Voltage Vs. Temperature

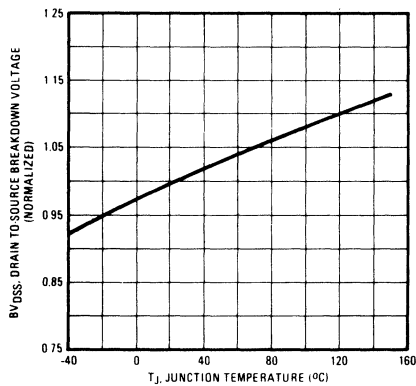


Fig. 9 — Normalized On-Resistance Vs. Temperature

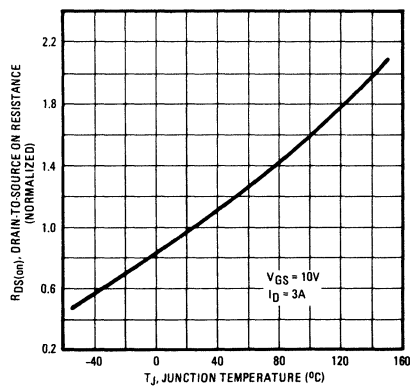


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

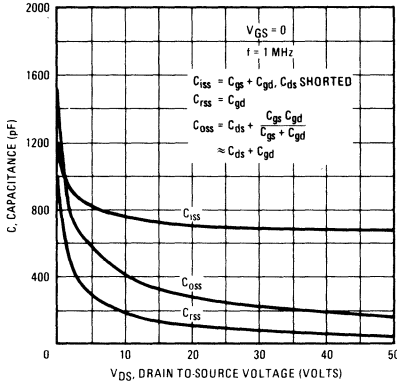


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

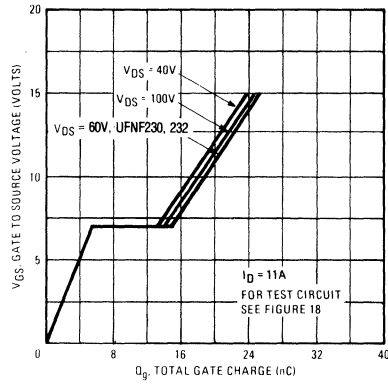


Fig. 12 – Typical On-Resistance Vs. Drain Current

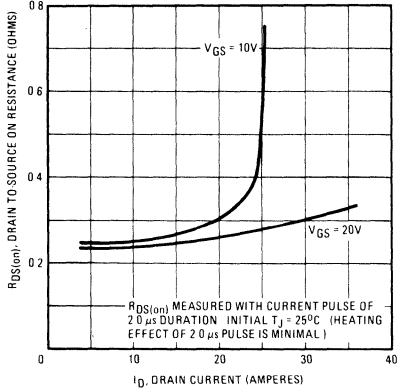


Fig. 13 – Maximum Drain Current Vs. Case Temperature

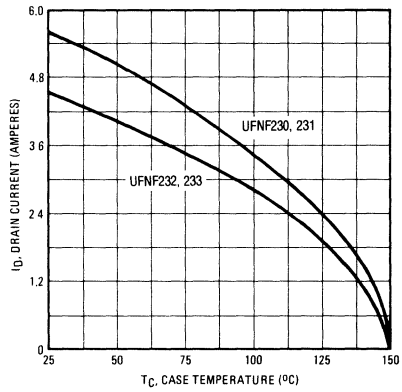


Fig. 14 – Power Vs. Temperature Derating Curve

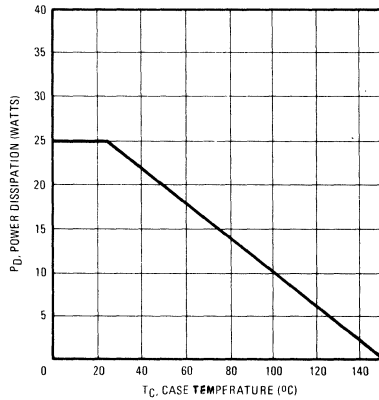


Fig. 15 – Clamped Inductive Test Circuit

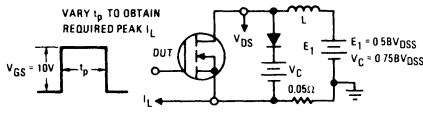
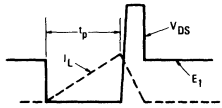


Fig. 16 – Clamped Inductive Waveforms



4

Fig. 17 – Switching Time Test Circuit

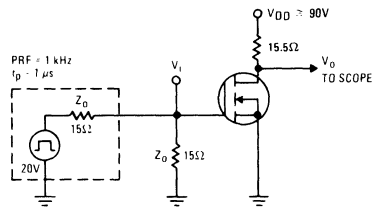
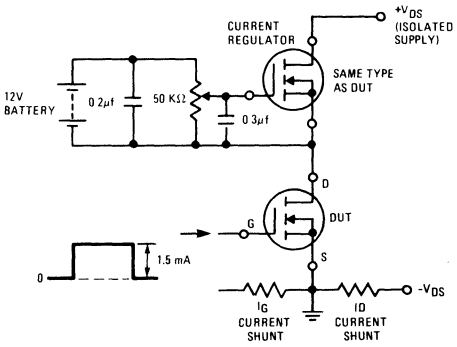


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 3.6 Ohm

UFNF310
UFNF311
UFNF312
UFNF313

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

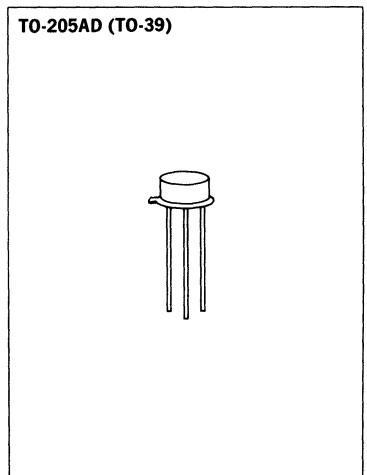
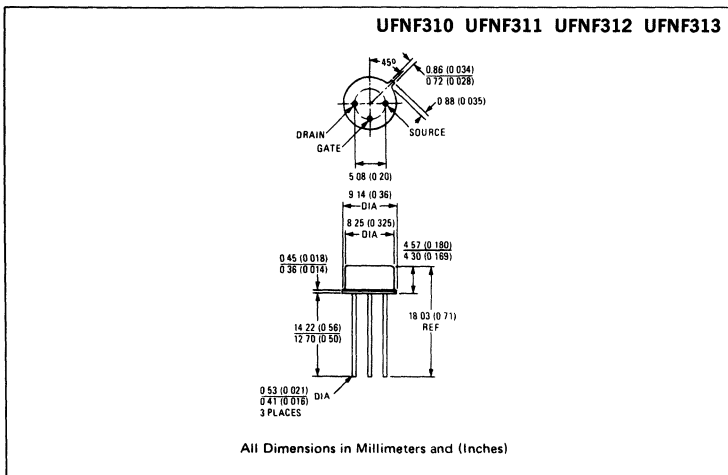
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{ps}	R _{DS(on)}	I _D
UFNF310	400V	3.6Ω	1.35A
UFNF311	350V	3.6Ω	1.35A
UFNF312	400V	5.0Ω	1.15A
UFNF313	350V	5.0Ω	1.15A

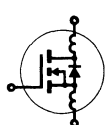
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF310	UFNF311	UFNF312	UFNF313	Units
V_{DS} Drain — Source Voltage ①	400	350	400	350	V
V_{DGR} Drain — Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	1.35	1.35	1.15	1.15	A
I_{DM} Pulsed Drain Current ③	5.5	5.5	4.5	4.5	A
V_{GS} Gate — Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain — Source Breakdown Voltage	UFNF310 UFNF312	400	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$
	UFNF311 UFNF313	350	—	—	V	
	ALL	2.0	—	4.0	V	
I_{GSS} Gate — Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate — Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	UFNF310 UFNF311	1.35	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$
	UFNF312 UFNF313	1.15	—	—	A	
$R_{DS(on)}$ Static Drain — Source On-State Resistance ②	UFNF310 UFNF311	—	3.3	3.6	Ω	$V_{GS} = 10\text{V}$, $I_D = 0.8\text{A}$
	UFNF312 UFNF313	—	3.6	5.0	Ω	
	ALL	0.5	1.2	—	S (μS)	
g_{fs} Forward Transconductance ②	ALL	0.5	1.2	—	S (μS)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 0.8\text{A}$
C_{iss} Input Capacitance	ALL	—	135	150	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	—	35	50	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	8.0	15	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 0.8\text{A}$, $Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f Fall Time	ALL	—	8.0	15	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	
Q_{gs} Gate-Source Charge	ALL	—	3.0	—	nC	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

THERMAL RESISTANCE

Parameter	Units	Value	Notes
R_{thJC} Junction-to-Case	K/W	8.33	
R_{thJA} Junction-to-Ambient	K/W	175	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF310	—	—	1.35	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF311	—	—	1.15	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF310	—	—	5.5	A	
		UFNF311	—	—	4.5	A	
V_{SD}	Diode Forward Voltage ②	UFNF310	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 1.35\text{A}, V_{GS} = 0\text{V}$
		UFNF311	—	—	1.5	V	
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.35\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.35\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

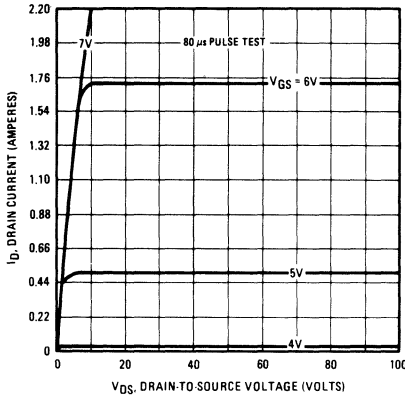


Fig. 2 – Typical Transfer Characteristics

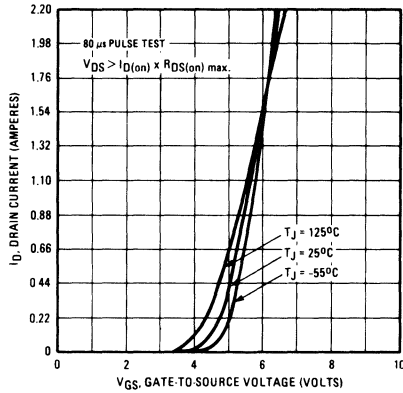


Fig. 3 – Typical Saturation Characteristics

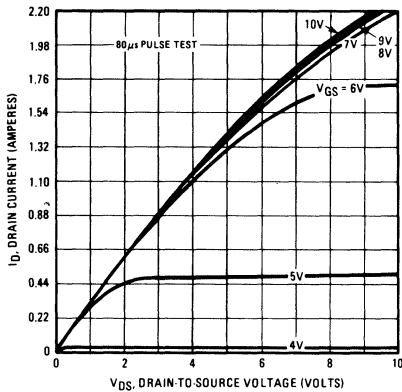


Fig. 4 – Maximum Safe Operating Area

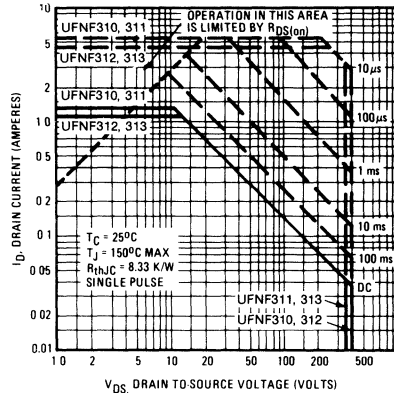
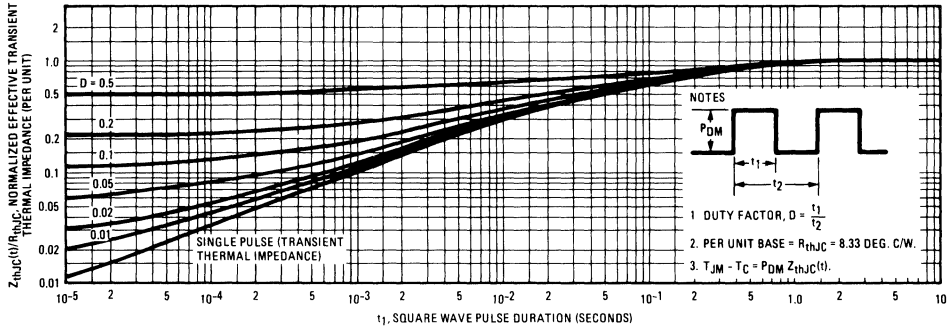


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 — Typical Transconductance Vs. Drain Current

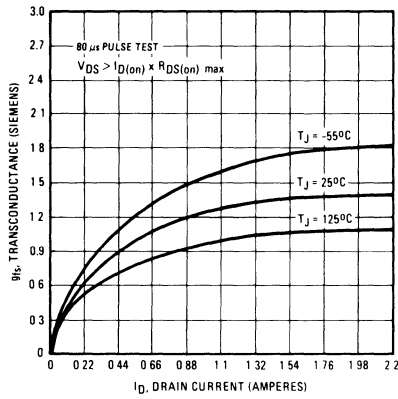


Fig. 7 — Typical Source-Drain Diode Forward Voltage

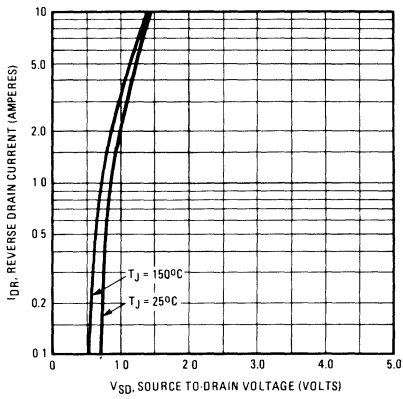


Fig. 8 — Breakdown Voltage Vs. Temperature

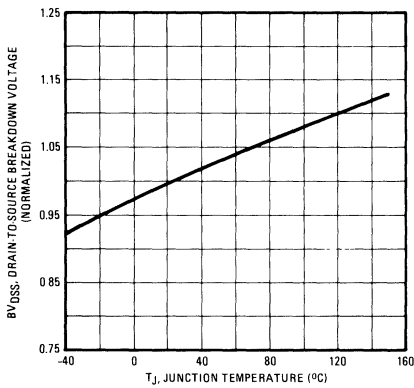


Fig. 9 — Normalized On-Resistance Vs. Temperature

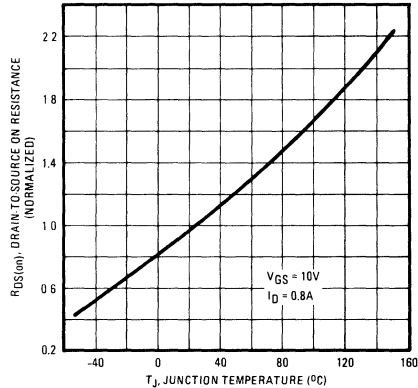


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

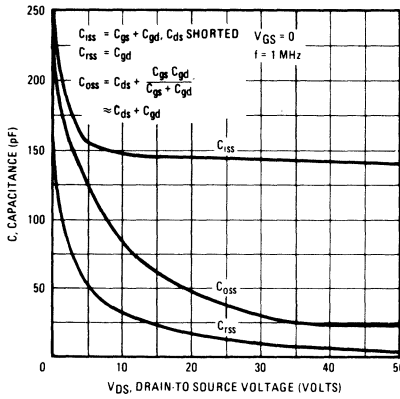


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

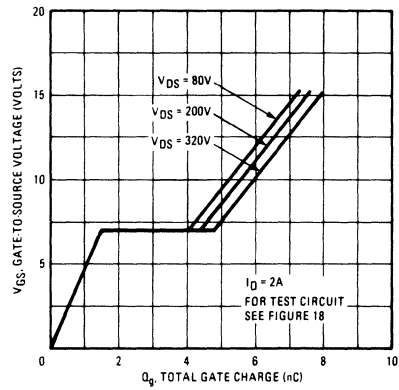


Fig. 12 — Typical On-Resistance Vs. Drain Current

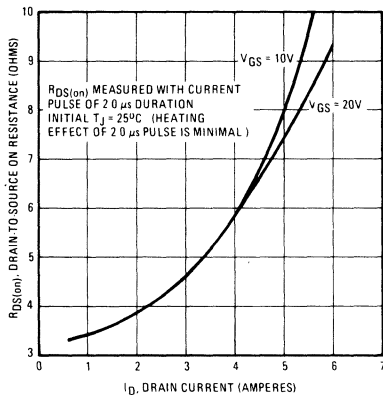


Fig. 13 — Maximum Drain Current Vs. Case Temperature

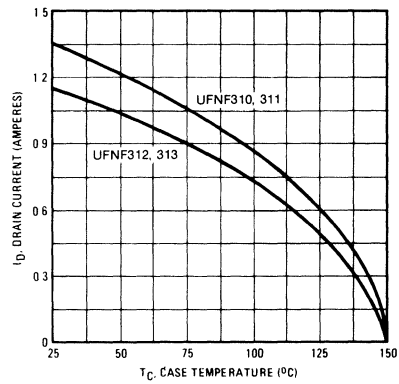


Fig. 14 — Power Vs. Temperature Derating Curve

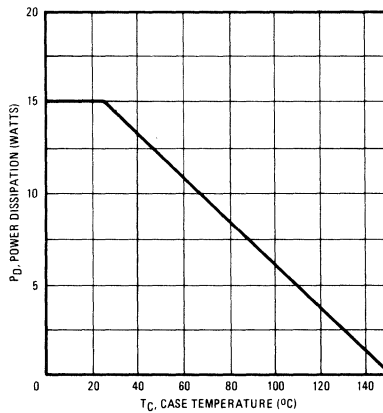


Fig. 15 — Clamped Inductive Test Circuit

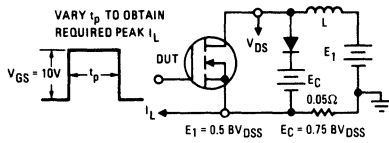


Fig. 16 — Clamped Inductive Waveforms

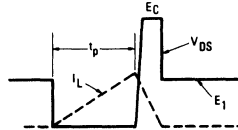


Fig. 17 — Switching Time Test Circuit

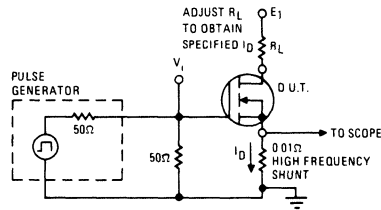
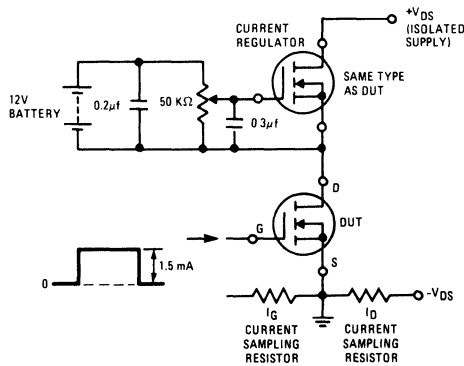


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.8 Ohm

UFNF320
UFNF321
UFNF322
UFNF323

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

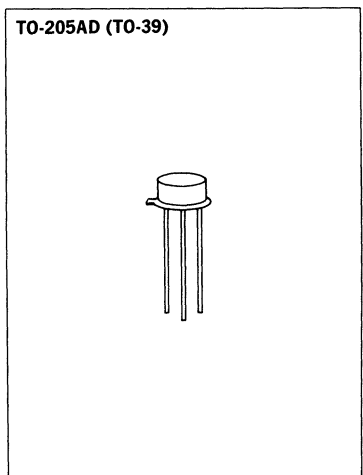
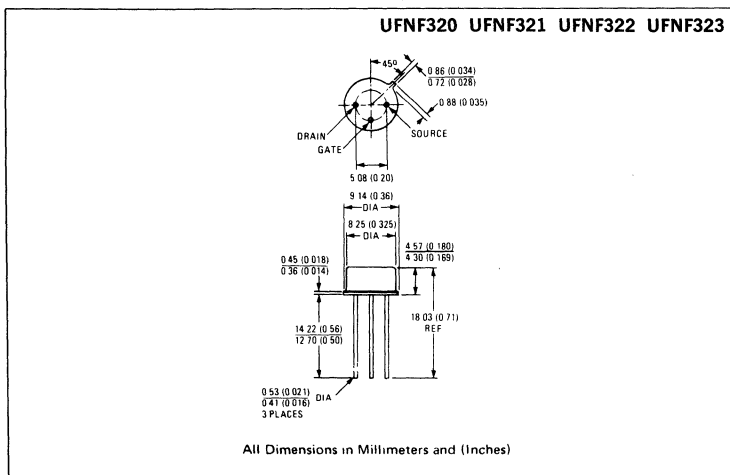
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _D
UFNF320	400V	1.8Ω	2.5A
UFNF321	350V	1.8Ω	2.5A
UFNF322	400V	2.5Ω	2.0A
UFNF323	350V	2.5Ω	2.0A

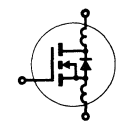
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF320	UFNF321	UFNF322	UFNF323	Units
V_{DS} Drain — Source Voltage ①	400	350	400	350	V
V_{DGR} Drain — Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM} Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS} Gate — Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain — Source Breakdown Voltage	UFNF320 UFNF322	400	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF321 UFNF323	350	—	—	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate — Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate — Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF320 UFNF321	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFNF322 UFNF323	2.0	—	—	A		
$R_{DS(on)}$ Static Drain — Source On-State Resistance ②	UFNF320 UFNF321	—	1.5	1.8	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.25\text{A}$	
	UFNF322 UFNF323	—	1.8	2.5	Ω		
g_{fs} Forward Transconductance ②	ALL	1.0	2.0	—	S (②)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 1.25\text{A}$	
C_{iss} Input Capacitance	ALL	—	450	600	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	100	200	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	20	40	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 2.0\text{A}$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	25	50	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	50	100	ns		
t_f Fall Time	ALL	—	25	50	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	$V_{GS} = 10\text{V}$, $I_D = 5.0\text{A}$, $V_{DS} = 0.8\text{V Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	6.25	K/W	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF320	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF321	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF320	—	—	10	A	
		UFNF321	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFNF320	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
		UFNF321	—	—	1.5	V	
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

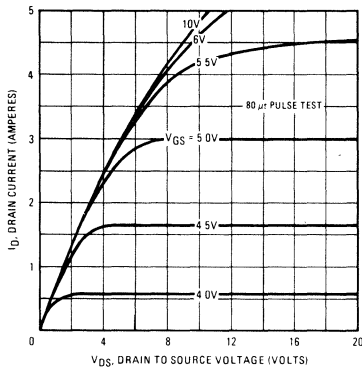


Fig. 2 – Typical Transfer Characteristics

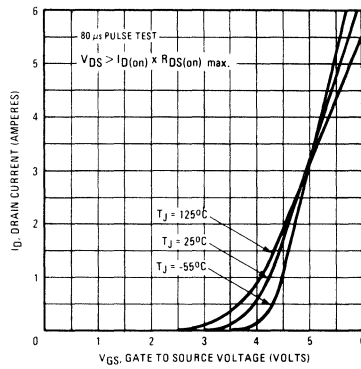


Fig. 3 – Typical Saturation Characteristics

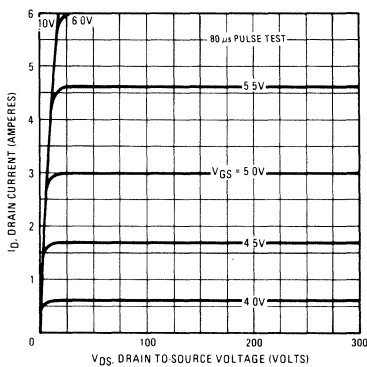


Fig. 4 – Maximum Safe Operating Area

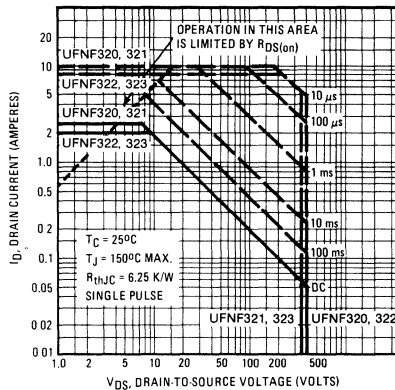
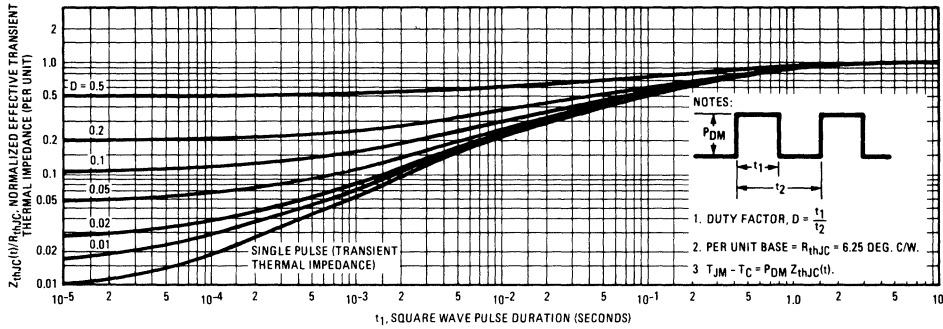


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

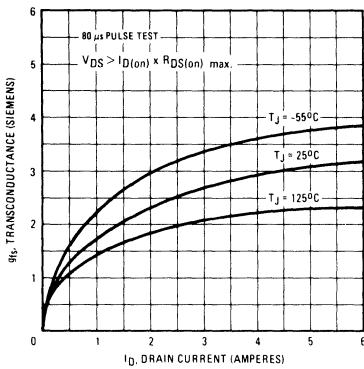


Fig. 7 – Typical Source-Drain Diode Forward Voltage

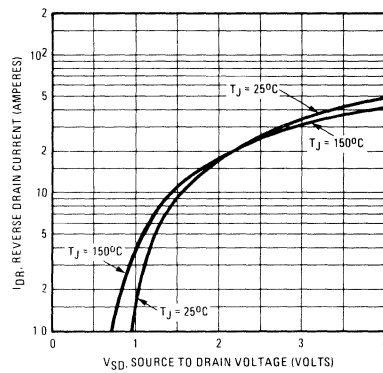


Fig. 8 – Breakdown Voltage Vs. Temperature

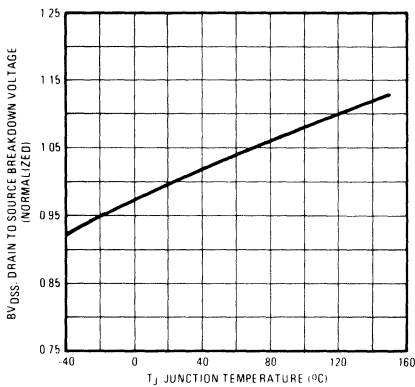


Fig. 9 – Normalized On-Resistance Vs. Temperature

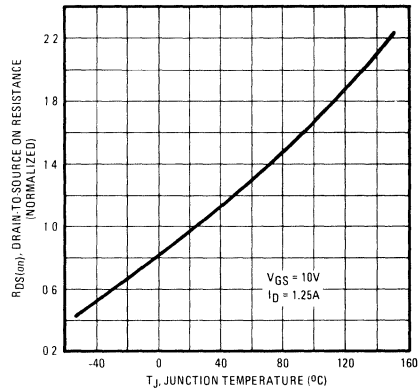


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

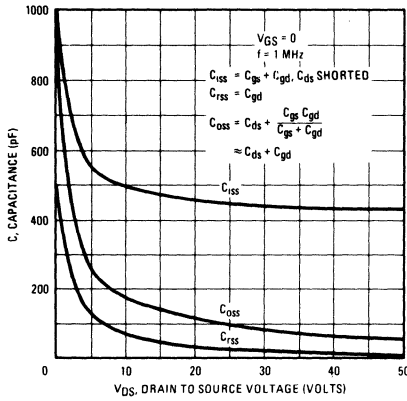


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

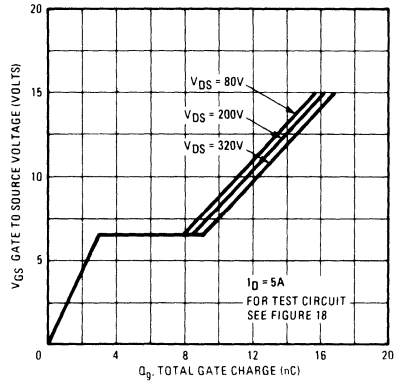


Fig. 12 – Typical On-Resistance Vs. Drain Current

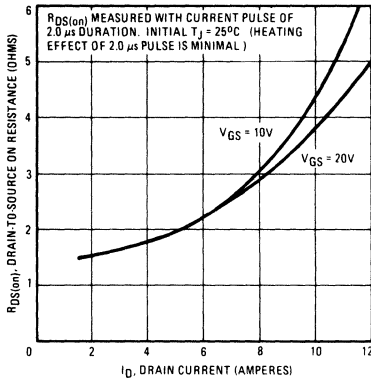


Fig. 13 – Maximum Drain Current Vs. Case Temperature

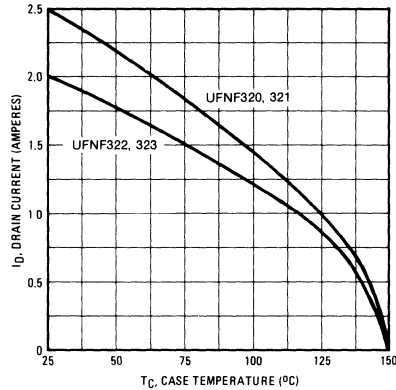


Fig. 14 – Power Vs. Temperature Derating Curve

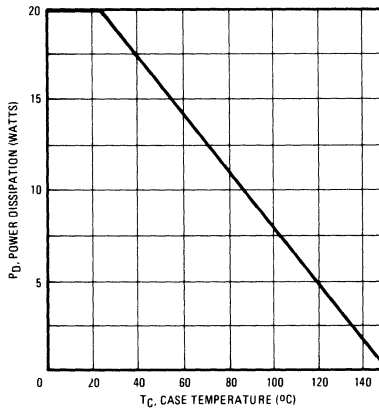


Fig. 15 — Clamped Inductive Test Circuit

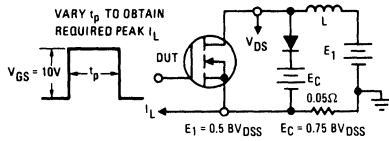


Fig. 16 — Clamped Inductive Waveforms

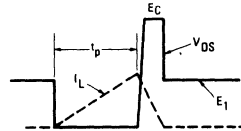


Fig. 17 — Switching Time Test Circuit

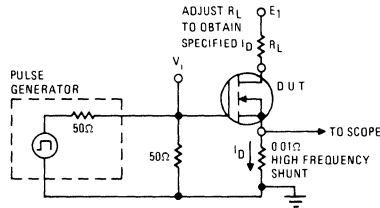
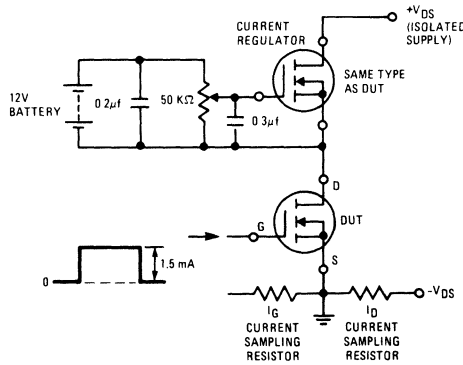


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm

UFNF330
UFNF331
UFNF332
UFNF333

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

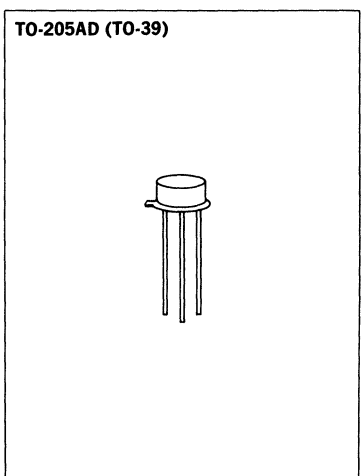
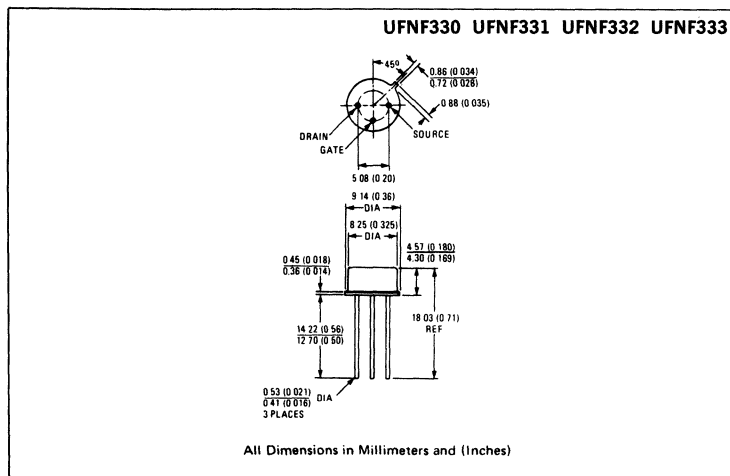
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{ds}	R _{DS(on)}	I _d
UFNF330	400V	1.0Ω	3.5A
UFNF331	350V	1.0Ω	3.5A
UFNF332	400V	1.5Ω	3.0A
UFNF333	350V	1.5Ω	3.0A

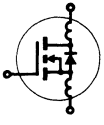
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF330	UFNF331	UFNF332	UFNF333	Units
V _{DS} Drain — Source Voltage ①	400	350	400	350	V
V _{DGR} Drain — Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	3.5	3.5	3.0	3.0	A
I _{DM} Pulsed Drain Current ③	14	14	12	12	A
V _{GS} Gate — Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	25 (See Fig. 14)				W
Linear Derating Factor	0.2 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	14	14	12	12	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ TC = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain — Source Breakdown Voltage	UFNF330	400	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFNF332	—	—	—	—		
	UFNF331 UFNF333	350	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate — Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate — Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFNF330	3.5	—	—	A	V _{DS} > I _{D(on)} × R _{DSON} max., V _{GS} = 10V	
	UFNF331	—	—	—	—		
	UFNF332 UFNF333	3.0	—	—	A		
R _{DSON} Static Drain — Source On-State Resistance ②	UFNF330	—	0.8	1.0	Ω	V _{GS} = 10V, I _D = 2.0A	
	UFNF331	—	—	—	—		
	UFNF332 UFNF333	—	1.0	1.5	Ω		
g _{fs} Forward Transconductance ②	ALL	2.0	3.5	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DSON} max., I _D = 2.0A	
C _{iss} Input Capacitance	ALL	—	700	900	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	150	300	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	40	80	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 175V, I _D = 2.0A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	—	35	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	55	ns		
t _f Fall Time	ALL	—	—	35	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	11	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	5.0	K/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF330	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF332 UFNF333	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF330 UFNF331	—	—	14	A	
		UFNF332 UFNF333	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	UFNF330 UFNF331	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$
		UFNF332 UFNF333	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 3.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

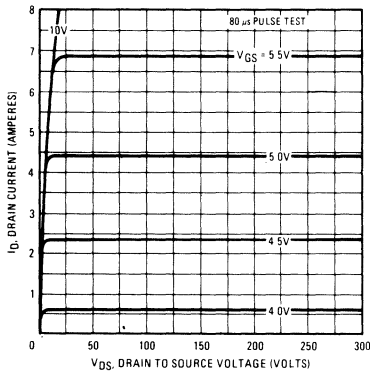


Fig. 2 – Typical Transfer Characteristics

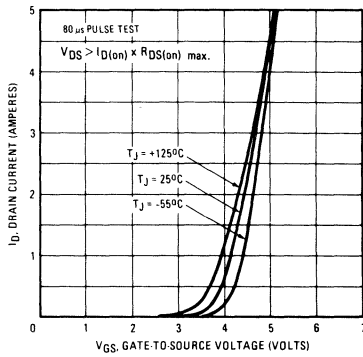


Fig. 3 – Typical Saturation Characteristics

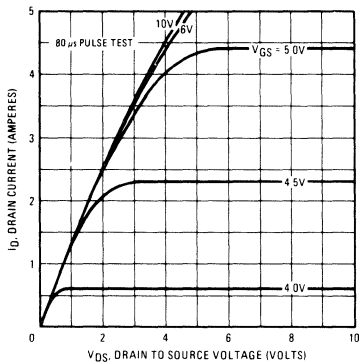


Fig. 4 – Maximum Safe Operating Area

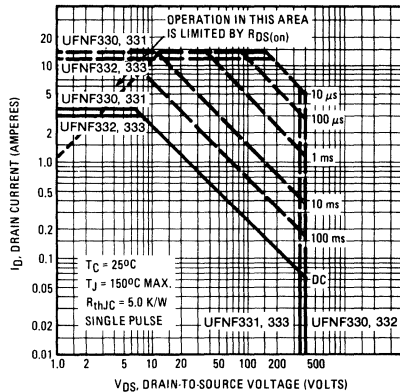
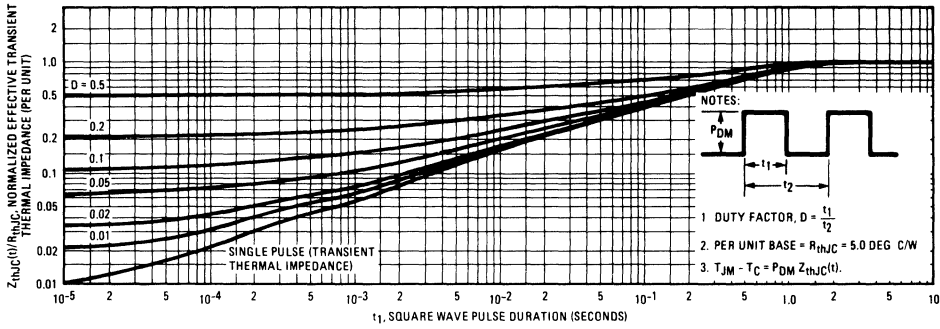


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

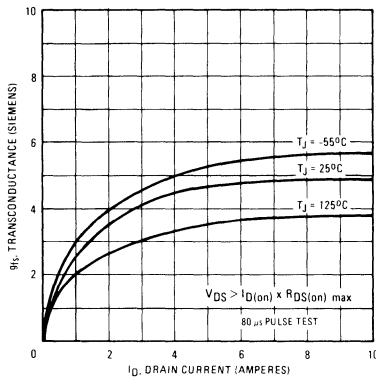


Fig. 7 – Typical Source-Drain Diode Forward Voltage

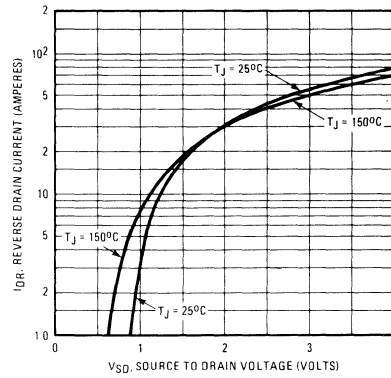


Fig. 8 – Breakdown Voltage Vs. Temperature

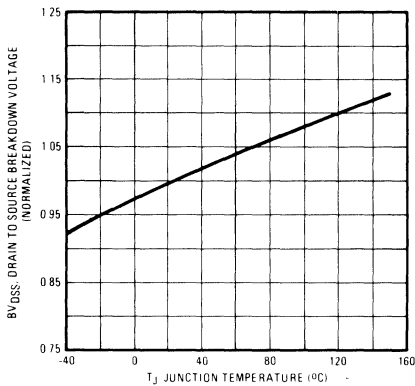


Fig. 9 – Normalized On-Resistance Vs. Temperature

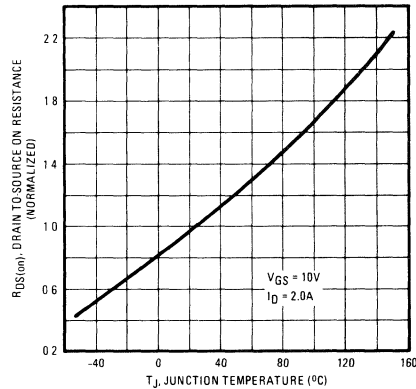


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

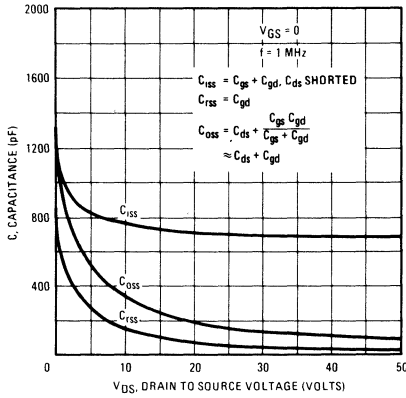


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

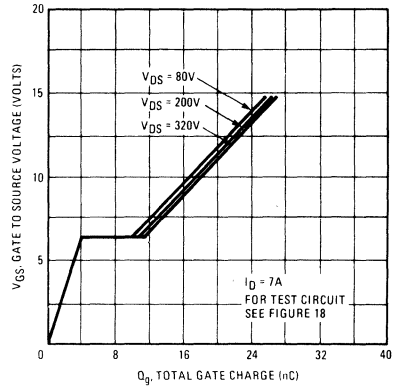


Fig. 12 – Typical On-Resistance Vs. Drain Current

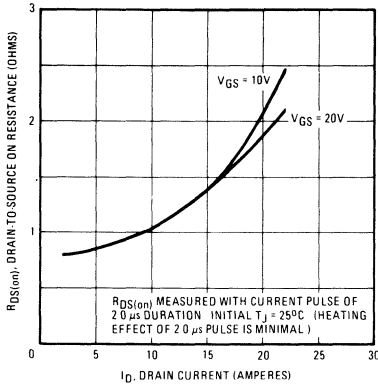


Fig. 13 – Maximum Drain Current Vs. Case Temperature

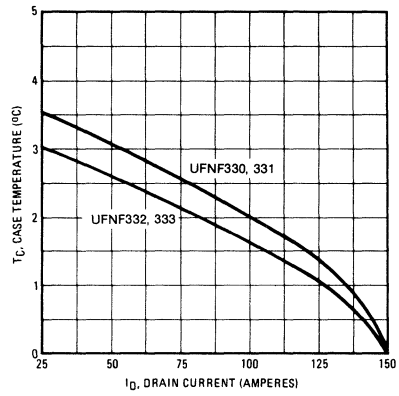


Fig. 14 – Power Vs. Temperature Derating Curve

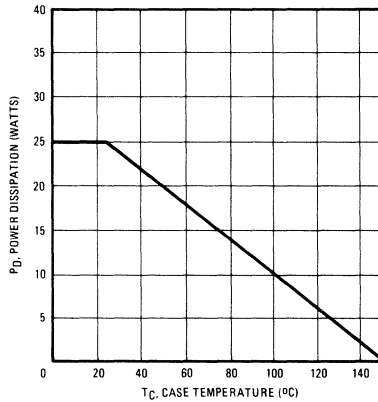


Fig. 15 -- Clamped Inductive Test Circuit

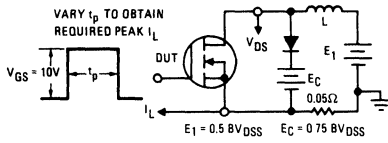


Fig. 16 -- Clamped Inductive Waveforms

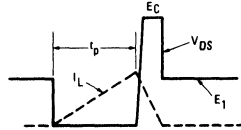


Fig. 17 -- Switching Time Test Circuit

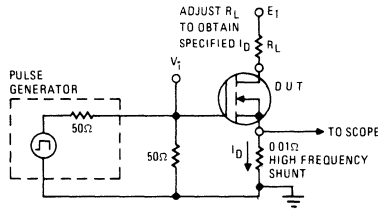
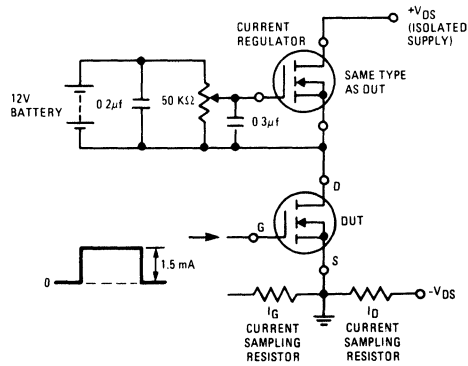


Fig. 18 -- Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 3.0 Ohm

UFNF420
UFNF421
UFNF422
UFNF423

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

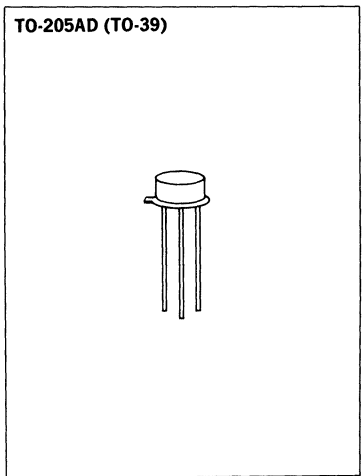
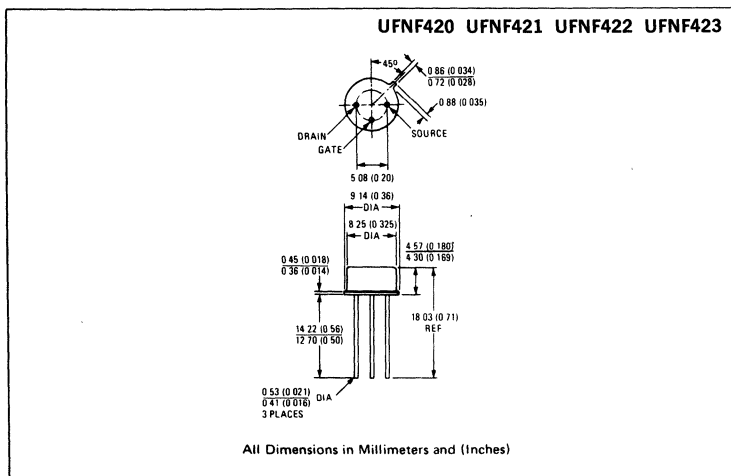
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _D
UFNF420	500V	3.0Ω	1.6A
UFNF421	450V	3.0Ω	1.6A
UFNF422	500V	4.0Ω	1.4A
UFNF423	450V	4.0Ω	1.4A

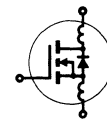
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF420	UFNF421	UFNF422	UFNF423	Units
V_{DS} Drain — Source Voltage ①	500	450	500	450	V
V_{DGR} Drain — Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	1.6	1.6	1.4	1.4	A
I_{DM} Pulsed Drain Current ③	6.5	6.5	5.5	5.5	A
V_{GS} Gate — Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
	6.5	6.5	5.5	5.5	
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain — Source Breakdown Voltage	UFNF420 UFNF422	500	—	—	V	$V_{GS} = 0\text{V}$	
	UFNF421 UFNF423	450	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$; $I_D = 250\mu\text{A}$	
I_{GSS} Gate — Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate — Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$; $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$; $V_{GS} = 0\text{V}$; $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF420 UFNF421	1.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$; $V_{GS} = 10\text{V}$	
	UFNF422 UFNF423	1.4	—	—	A		
$R_{DS(on)}$ Static Drain — Source On-State Resistance ②	UFNF420 UFNF421	—	2.5	3.0	Ω	$V_{GS} = 10\text{V}$; $I_D = 1.0\text{A}$	
	UFNF422 UFNF423	—	3.0	4.0	Ω		
g_{fs} Forward Transconductance ②	ALL	1.0	1.75	—	S (②)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$; $I_D = 1.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	300	400	pF	$V_{GS} = 0\text{V}$; $V_{DS} = 25\text{V}$; $f = 1.0\text{MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	75	150	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	20	40	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	30	60	ns	$V_{DD} = 0.5 BV_{DSS}$; $I_D = 1.0\text{A}$; $Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	25	50	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	30	60	ns		
t_f Fall Time	ALL	—	15	30	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	$V_{GS} = 10\text{V}$; $I_D = 3.0\text{A}$; $V_{DS} = 0.8\text{V}$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	5.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	6.25	K/W	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF420	—	—	1.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFNF421	—	—	1.4	A	
		UFNF422 UFNF423	—	—	1.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF420	—	—	6.5	A	
		UFNF421	—	—	6.5	A	
		UFNF422 UFNF423	—	—	5.5	A	
V_{SD}	Diode Forward Voltage ②	UFNF420	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 1.6\text{A}, V_{GS} = 0\text{V}$
		UFNF421	—	—	1.4	V	
		UFNF422 UFNF423	—	—	1.3	V	
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.6\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.6\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

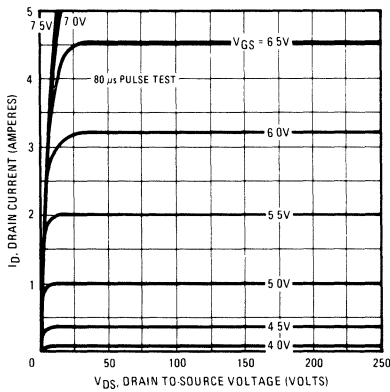


Fig. 2 – Typical Transfer Characteristics

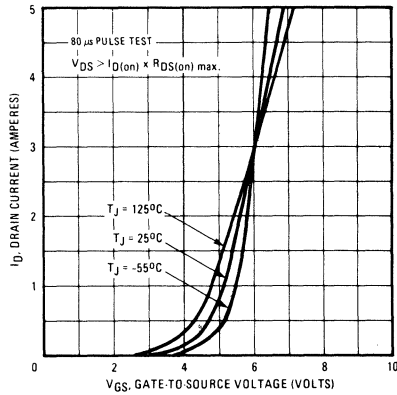


Fig. 3 – Typical Saturation Characteristics

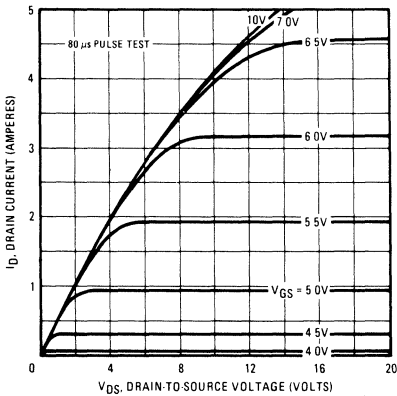


Fig. 4 – Maximum Safe Operating Area

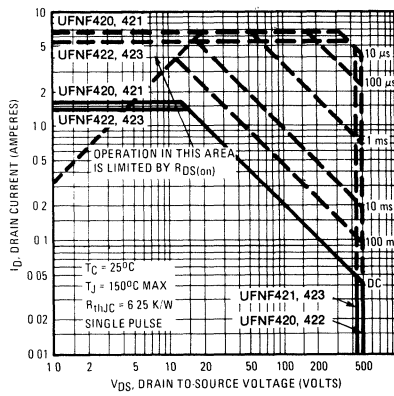


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

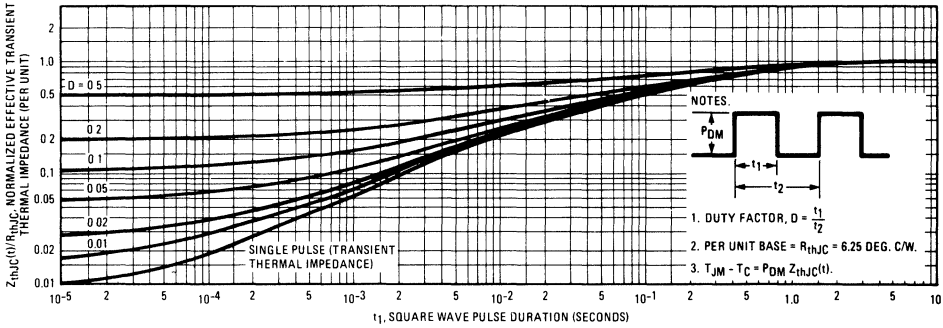


Fig. 6 – Typical Transconductance Vs. Drain Current

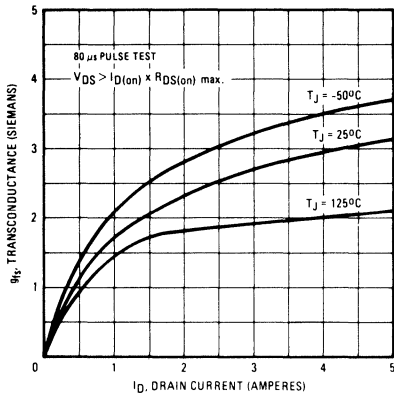


Fig. 7 – Typical Source-Drain Diode Forward Voltage

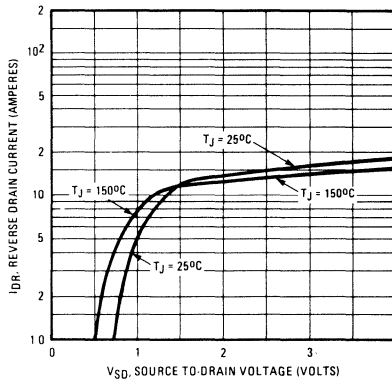


Fig. 8 – Breakdown Voltage Vs. Temperature

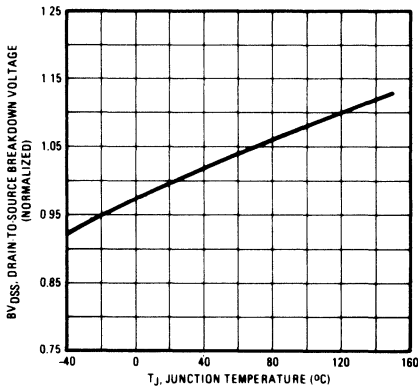


Fig. 9 – Normalized On-Resistance Vs. Temperature

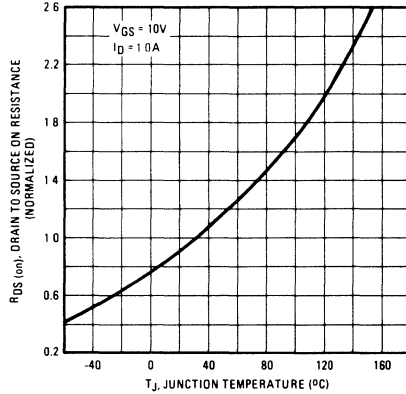


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

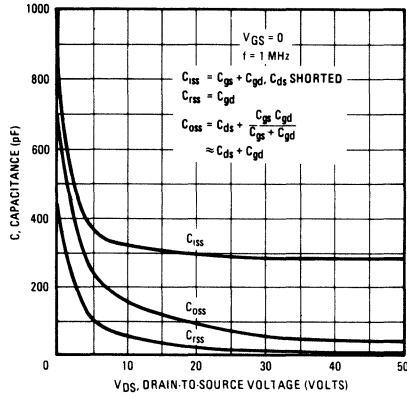


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

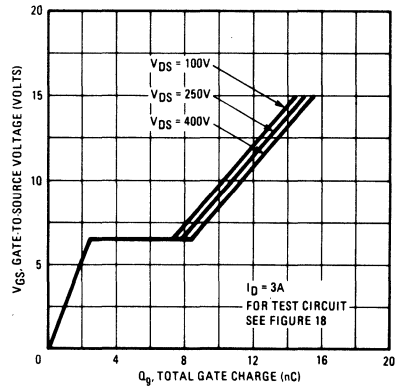


Fig. 12 — Typical On-Resistance Vs. Drain Current

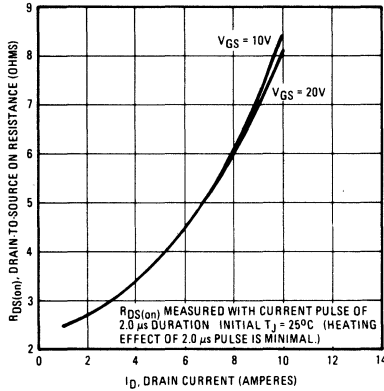


Fig. 13 — Maximum Drain Current Vs. Case Temperature

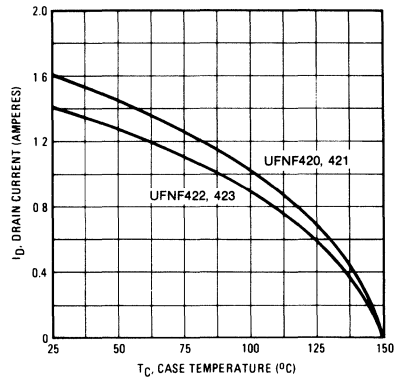


Fig. 14 — Power Vs. Temperature Derating Curve

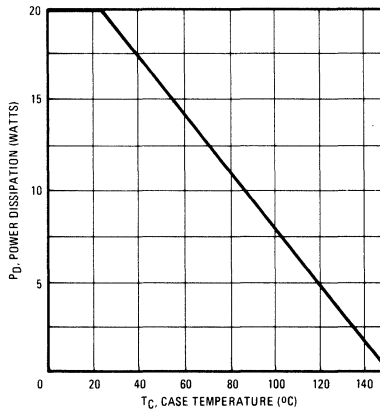


Fig. 15 — Clamped Inductive Test Circuit

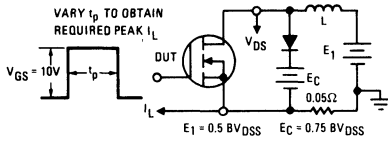


Fig. 16 — Clamped Inductive Waveforms

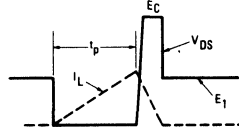


Fig. 17 — Switching Time Test Circuit

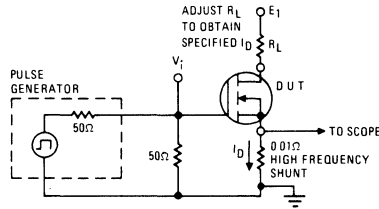
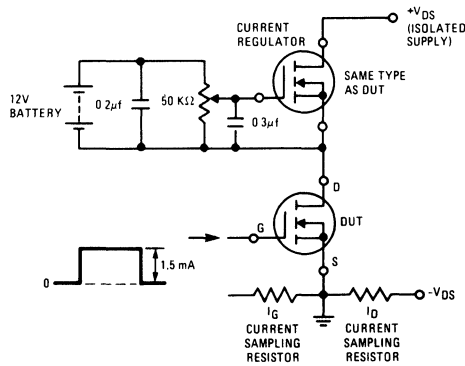


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm N-Channel

UFNF430
UFNF431
UFNF432
UFNF433

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

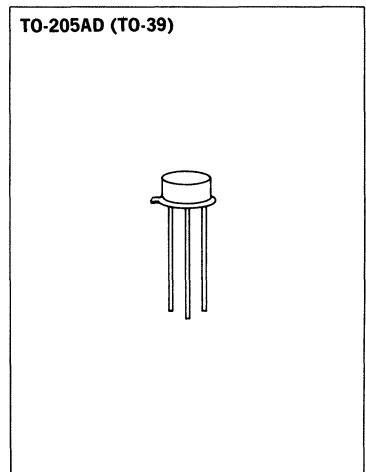
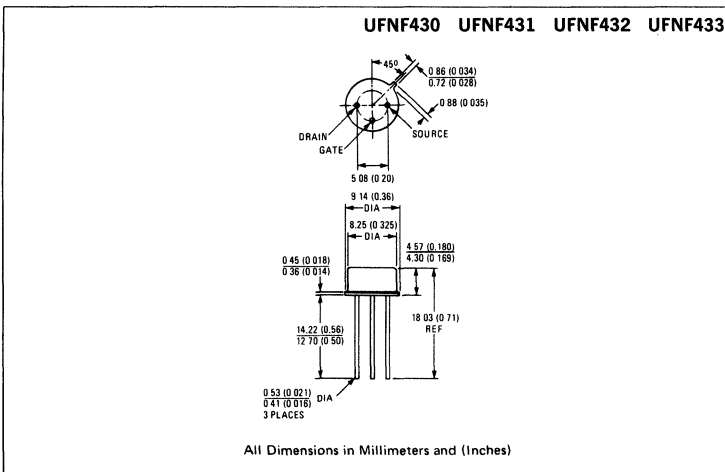
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF430	500V	1.5Ω	2.75A
UFNF431	450V	1.5Ω	2.75A
UFNF432	500V	2.0Ω	2.25A
UFNF433	450V	2.0Ω	2.25A

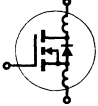
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFNF430	UFNF431	UFNF432	UFNF433	Units
V_{DS} Drain — Source Voltage ①	500	450	500	450	V
V_{DGR} Drain — Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM} Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS} Gate — Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	25 (See Fig. 14)				W
Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
	11	11	9.0	9.0	
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain — Source Breakdown Voltage	UFNF430 UFNF432	500	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFNF431 UFNF433	450	—	—	V		
	ALL	2.0	—	4.0	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	—	—	500	nA	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate — Source Leakage Forward	ALL	—	—	-500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate — Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFNF430 UFNF431	2.75	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, V_{GS} = 10\text{V}$	
	UFNF432 UFNF433	2.25	—	—	A		
	ALL	—	1.3	1.5	Ω		
$R_{DS(on)}$ Static Drain — Source On-State Resistance ②	UFNF430 UFNF431	—	1.3	1.5	Ω	$V_{GS} = 10\text{V}, I_D = 1.5\text{A}$	
	UFNF432 UFNF433	—	1.5	2.0	Ω		
	ALL	1.5	2.5	—	S (ü)		
g_{fs} Forward Transconductance ②	ALL	—	600	800	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$ See Fig. 10	
C_{iss} Input Capacitance	ALL	—	100	200	pF	$V_{DD} = 225\text{V}, I_D = 1.5\text{A}, Z_o = 15\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
C_{oss} Output Capacitance	ALL	—	30	60	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	—	30	ns		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	55	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	—	30	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	30	ns		
t_f Fall Time	ALL	—	—	30	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	30	nC	$V_{GS} = 10\text{V}, I_D = 6.0\text{A}, V_{DS} = 0.8\text{V Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	11	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	11	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	5.0	K/W	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF430 UFNF431	—	—	2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier	
		UFNF432 UFNF433	—	—	2.25	A		
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF430 UFNF431	—	—	11	A		
		UFNF432 UFNF433	—	—	9.0	A		
V_{SD}	Diode Forward Voltage ②	UFNF430 UFNF431	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 2.75\text{A}, V_{GS} = 0\text{V}$	
		UFNF432 UFNF433	—	—	1.3	V		
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.75\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.75\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

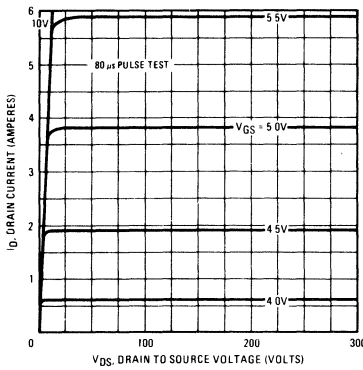


Fig. 2 – Typical Transfer Characteristics

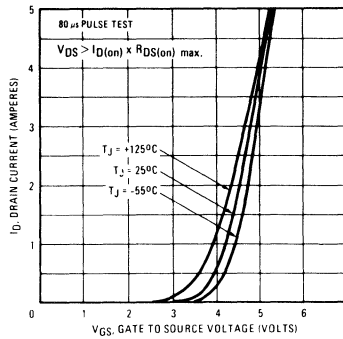


Fig. 3 – Typical Saturation Characteristics

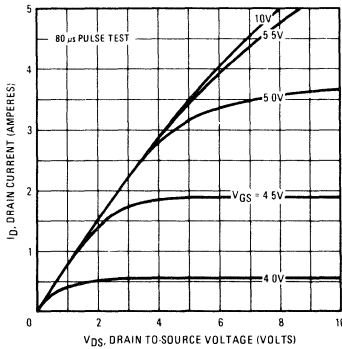


Fig. 4 – Maximum Safe Operating Area

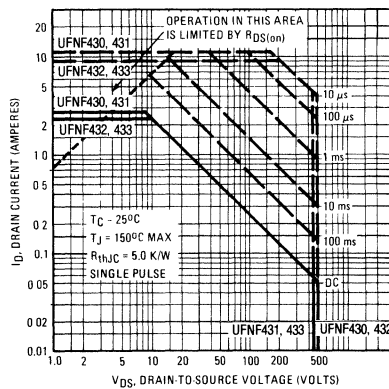
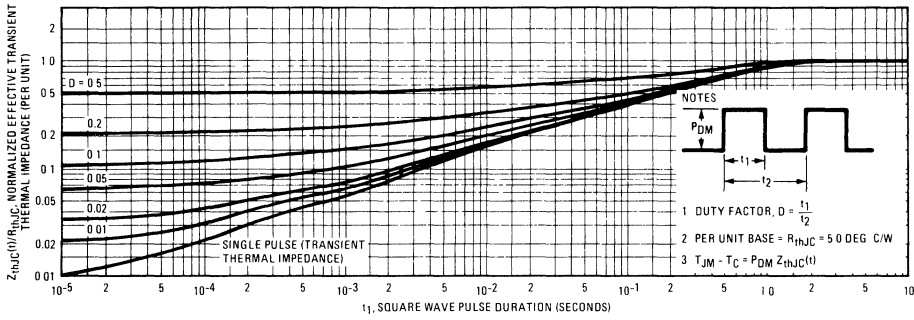


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

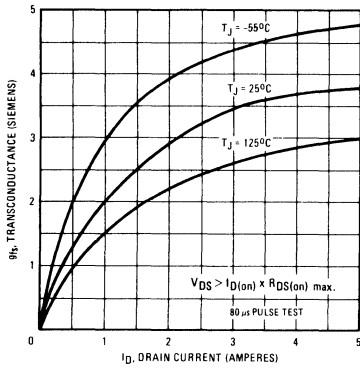


Fig. 7 – Typical Source-Drain Diode Forward Voltage

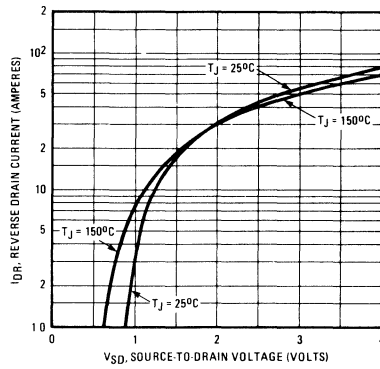


Fig. 8 – Breakdown Voltage Vs. Temperature

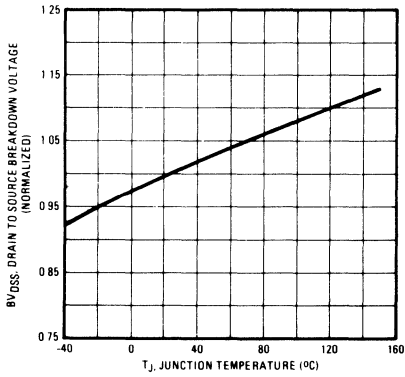


Fig. 9 – Normalized On-Resistance Vs. Temperature

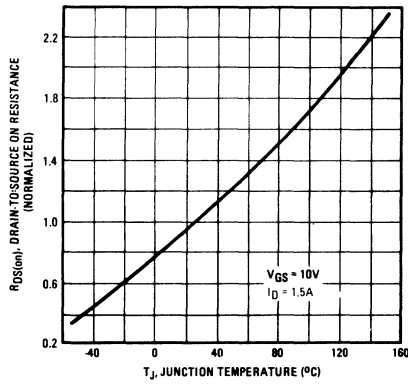


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

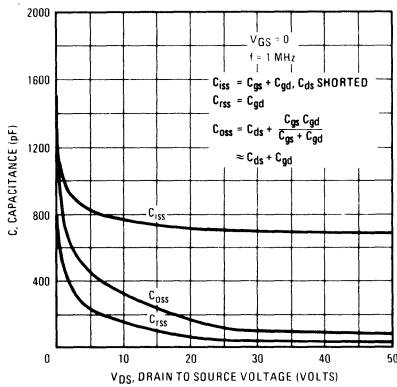


Fig. 12 – Typical On-Resistance Vs. Drain Current

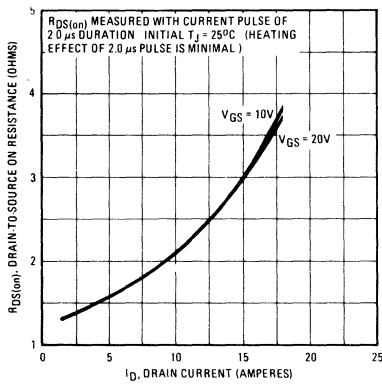


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

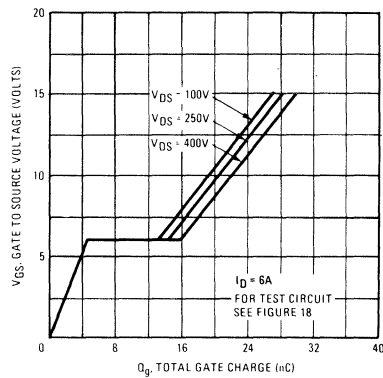


Fig. 13 – Maximum Drain Current Vs. Case Temperature

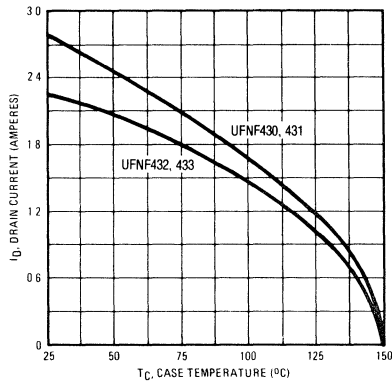


Fig. 14 – Power Vs. Temperature Derating Curve

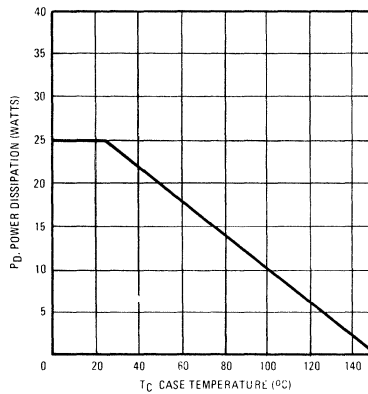


Fig. 15 — Clamped Inductive Test Circuit

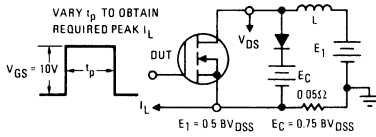


Fig. 16 — Clamped Inductive Waveforms

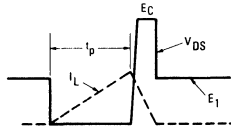


Fig. 17 — Switching Time Test Circuit

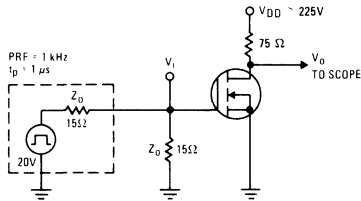
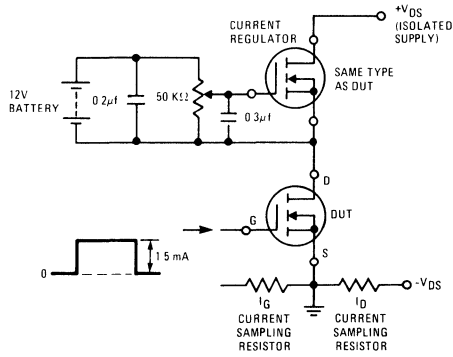


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm N-Channel

UFN120
UFN121
UFN122
UFN123

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

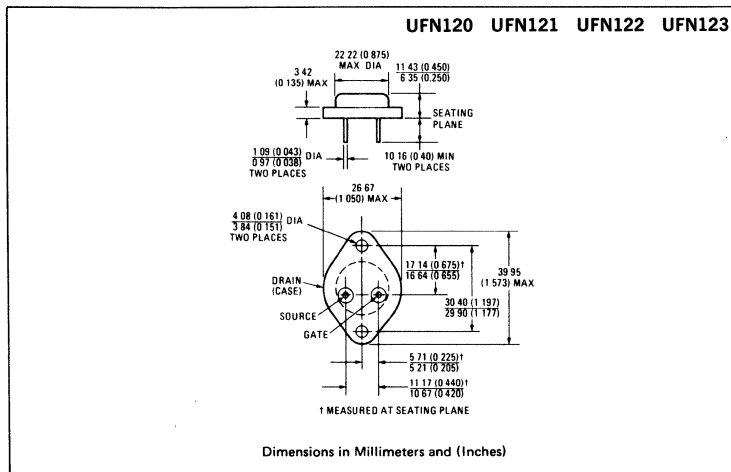
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

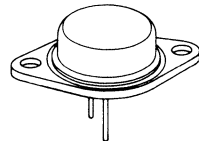
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN120	100V	0.30 Ω	8.0A
UFN121	60V	0.30 Ω	8.0A
UFN122	100V	0.40 Ω	7.0A
UFN123	60V	0.40 Ω	7.0A

MECHANICAL SPECIFICATIONS



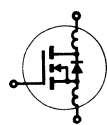
TO-204AA (TO-3)



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN120	UFN121	UFN122	UFN123	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	8.0	8.0	7.0	7.0	A
I _D @ T _C = 100°C Continuous Drain Current	5.0	5.0	4.0	4.0	A
I _{DM} Pulsed Drain Current ③	32	32	28	28	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	32	32	28	28	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN120 UFN122	100	—	—	V	V _{GS} = 0V	
	UFN121 UFN123	60	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN120 UFN121	8.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max.; V _{GS} = 10V	
	UFN122 UFN123	7.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN120 UFN121	—	0.25	0.30	Ω	V _{GS} = 10V, I _D = 4.0A	
	UFN122 UFN123	—	0.30	0.40	Ω		
g _{fs} Forward Transconductance ②	ALL	1.5	2.9	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max.; I _D = 4.0A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz	
C _{oss} Output Capacitance	ALL	—	200	400	pF	See Fig. 10	
C _{rss} Reverse Transfer Capacitance	ALL	—	50	100	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 4.0A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	35	70	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	35	70	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC	V _{GS} = 10V, I _D = 10A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN120	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN121	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN120	—	—	32	A	
		UFN122	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN120	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
		UFN121	—	—	2.3	V	
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

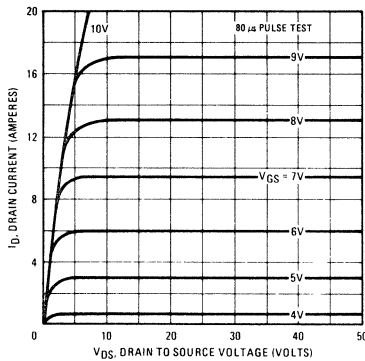


Fig. 2 – Typical Transfer Characteristics

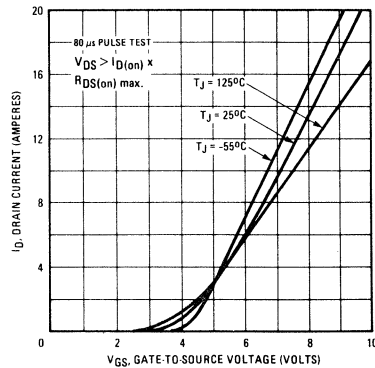


Fig. 3 – Typical Saturation Characteristics

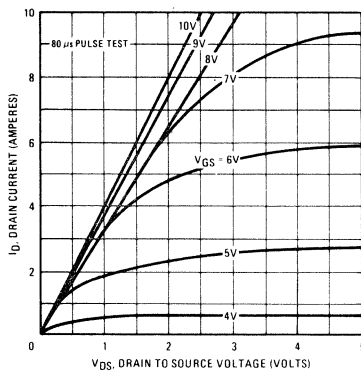


Fig. 4 – Maximum Safe Operating Area

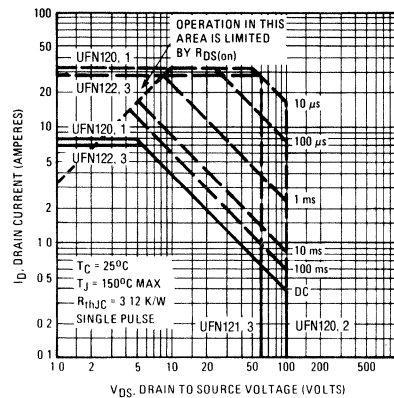
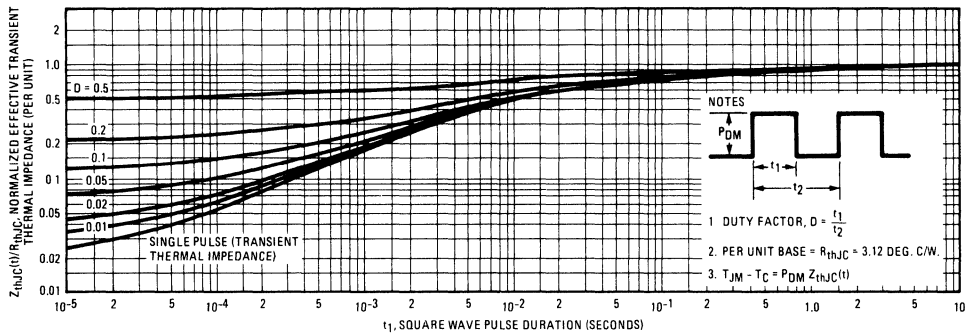


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

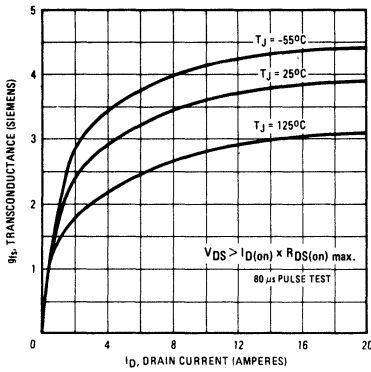


Fig. 7 – Typical Source-Drain Diode Forward Voltage

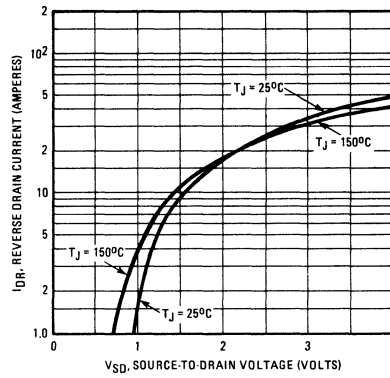


Fig. 8 – Breakdown Voltage Vs. Temperature

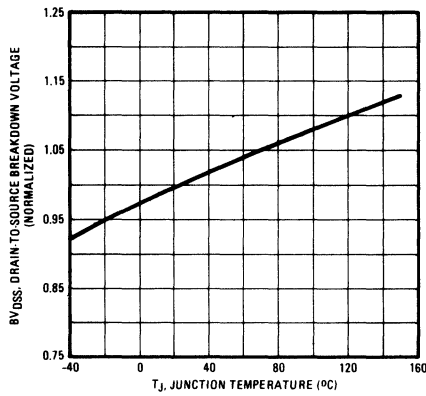


Fig. 9 – Normalized On-Resistance Vs. Temperature

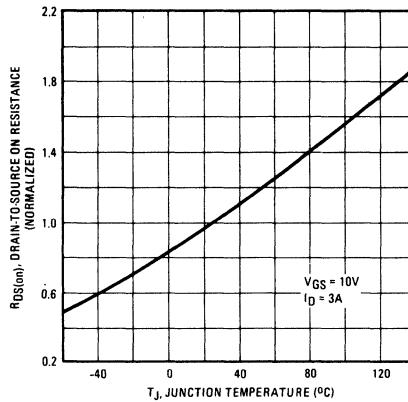


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

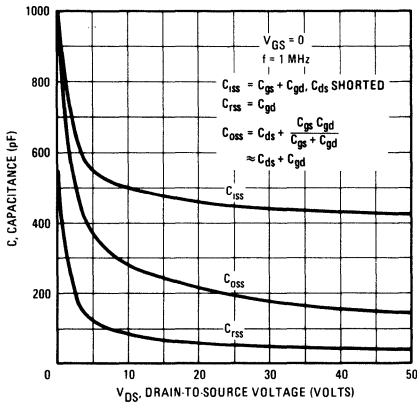


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

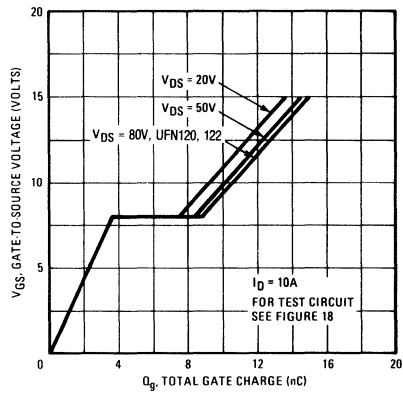


Fig. 12 – Typical On-Resistance Vs. Drain Current

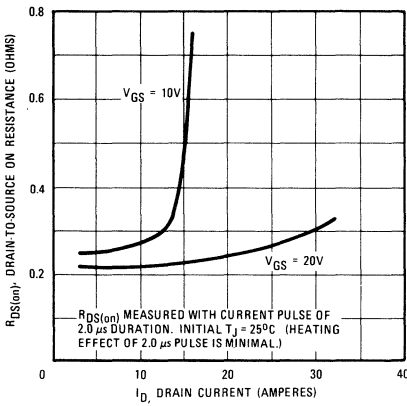


Fig. 13 – Maximum Drain Current Vs. Case Temperature

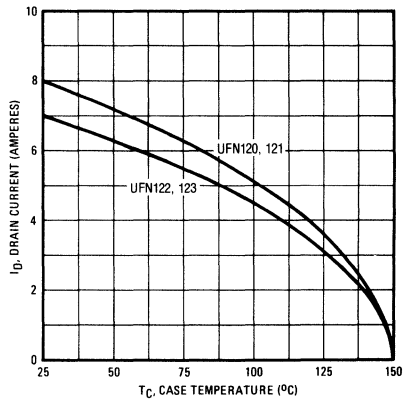


Fig. 14 – Power Vs. Temperature Derating Curve

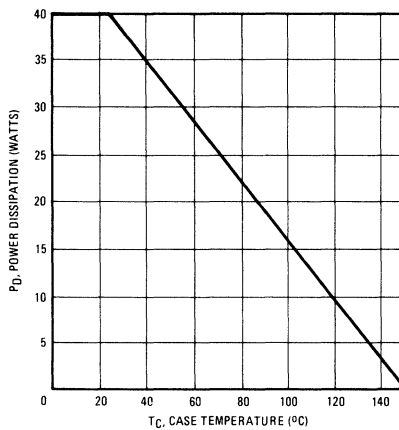


Fig. 15 – Clamped Inductive Test Circuit

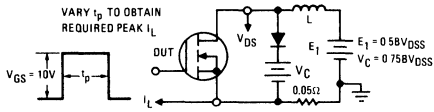


Fig. 16 – Clamped Inductive Waveforms

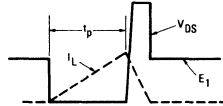


Fig. 17 – Switching Time Test Circuit

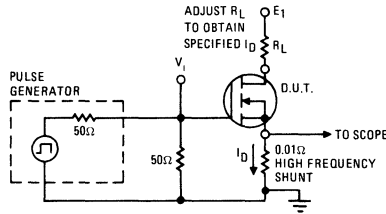
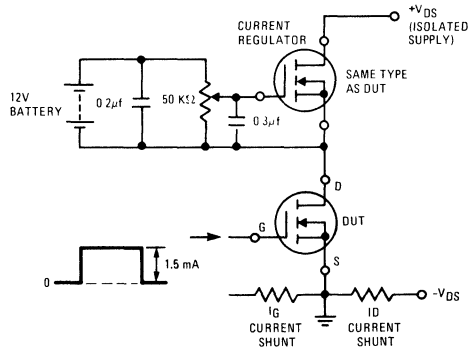


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFN130
UFN131
UFN132
UFN133

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

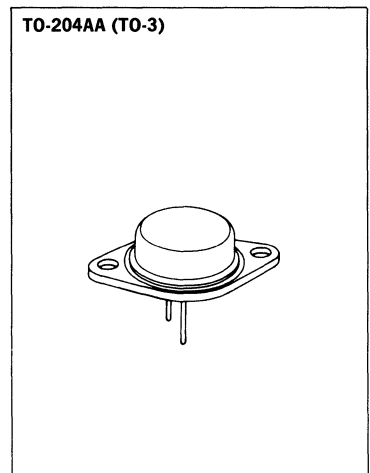
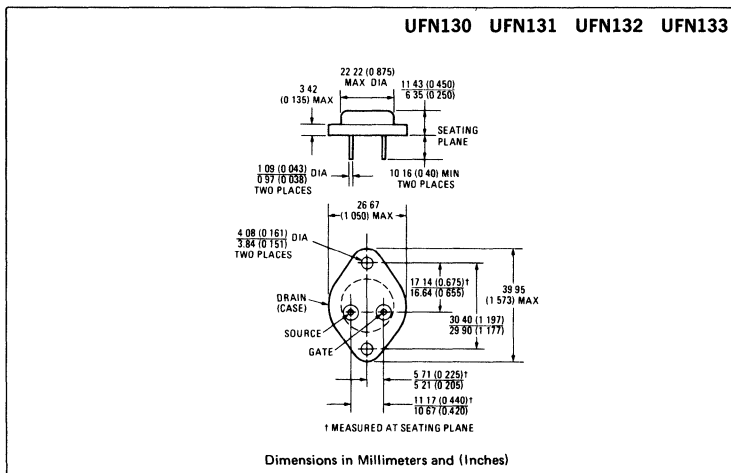
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN130	100V	0.18 Ω	14A
UFN131	60V	0.18 Ω	14A
UFN132	100V	0.25 Ω	12A
UFN133	60V	0.25 Ω	12A

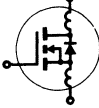
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN130	UFN131	UFN132	UFN133	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	14	14	12	12	A
I _D @ T _C = 100°C Continuous Drain Current	9.0	9.0	8.0	8.0	A
I _{DM} Pulsed Drain Current ③	56	56	48	48	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	56	56	48	48	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN130 UFN132	100	—	—	V	V _{GS} = 0V	
	UFN131 UFN133	60	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN130 UFN131	14	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max.; V _{GS} = 10V	
	UFN132 UFN133	12	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN130 UFN131	—	0.14	0.18	Ω	V _{GS} = 10V, I _D = 8.0A	
	UFN132 UFN133	—	0.20	0.25	Ω		
g _{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max.; I _D = 8.0A	
C _{iss} Input Capacitance	ALL	—	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	300	500	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	100	150	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 36V, I _D = 8.0A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	—	75	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	40	ns		
t _f Fall Time	ALL	—	—	45	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	9.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN130	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN132 UFN133	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN130 UFN131	—	—	56	A	
		UFN132 UFN133	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN130 UFN131	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 14\text{A}, V_{GS} = 0\text{V}$
		UFN132 UFN133	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 12\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

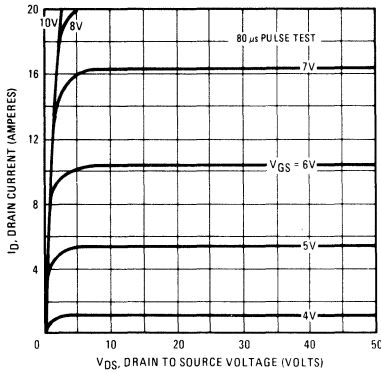


Fig. 2 – Typical Transfer Characteristics

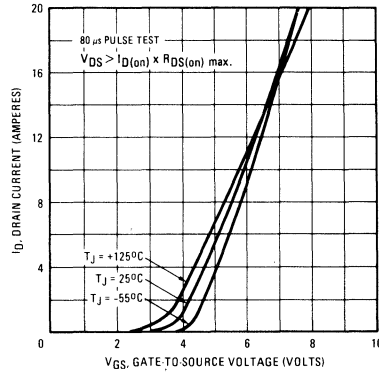


Fig. 3 – Typical Saturation Characteristics

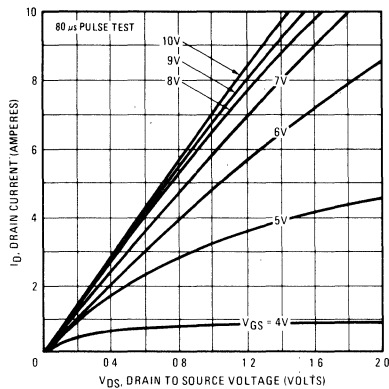


Fig. 4 – Maximum Safe Operating Area

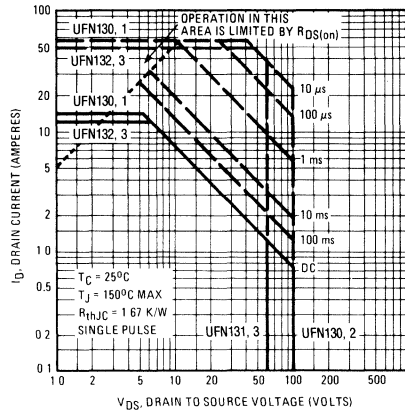
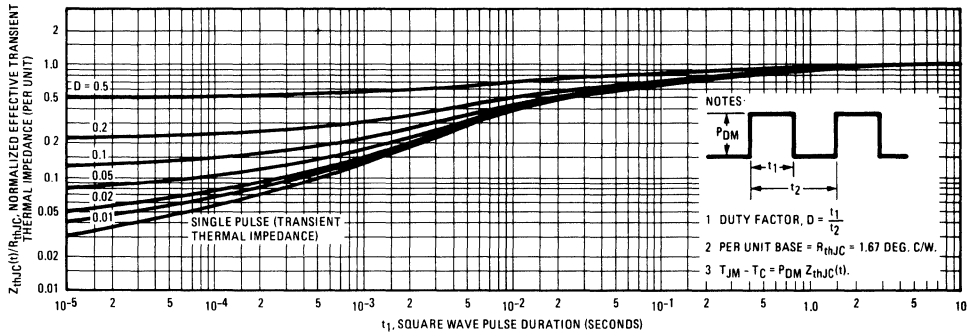


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 — Typical Transconductance Vs. Drain Current

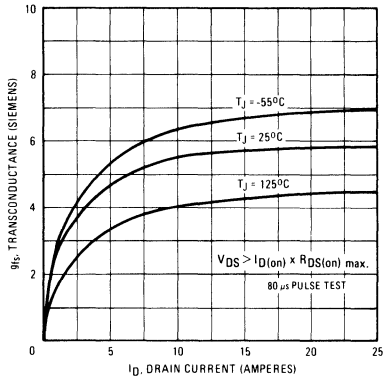


Fig. 7 — Typical Source-Drain Diode Forward Voltage

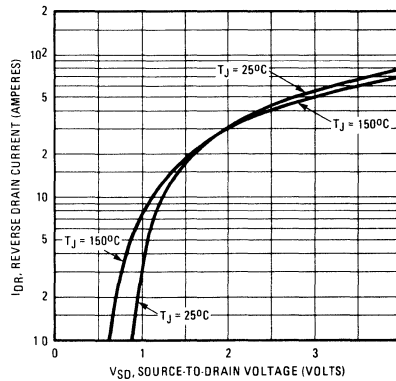


Fig. 8 — Breakdown Voltage Vs. Temperature

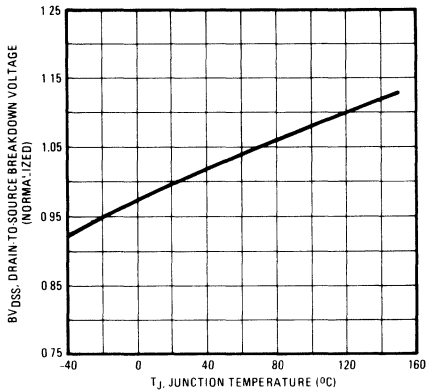


Fig. 9 — Normalized On-Resistance Vs. Temperature

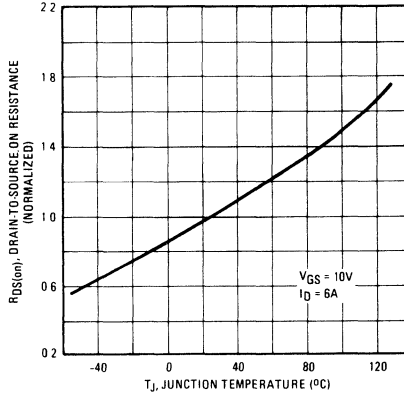


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

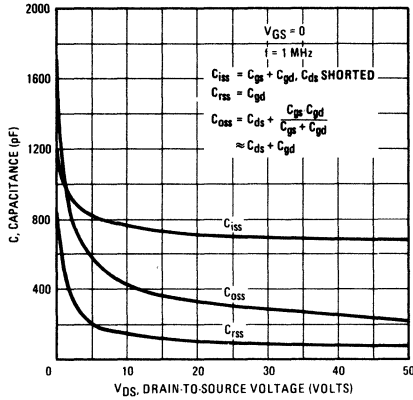


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

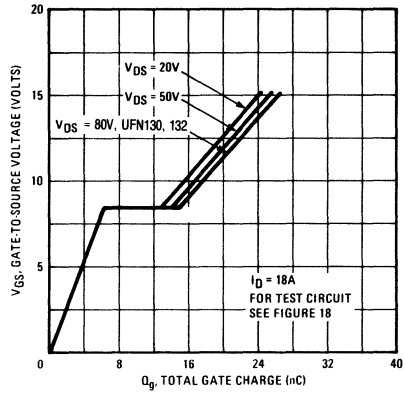


Fig. 12 – Typical On-Resistance Vs. Drain Current

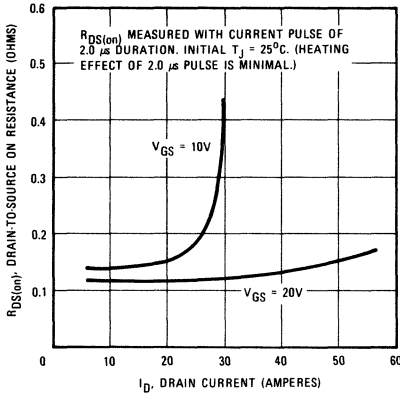


Fig. 13 – Maximum Drain Current Vs. Case Temperature

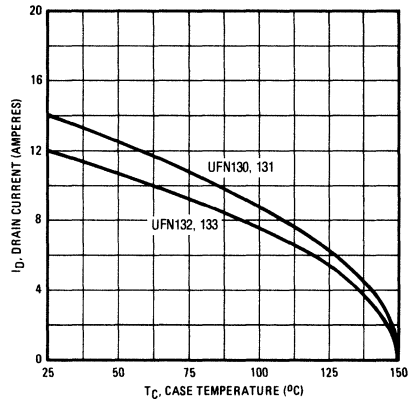


Fig. 14 – Power Vs. Temperature Derating Curve

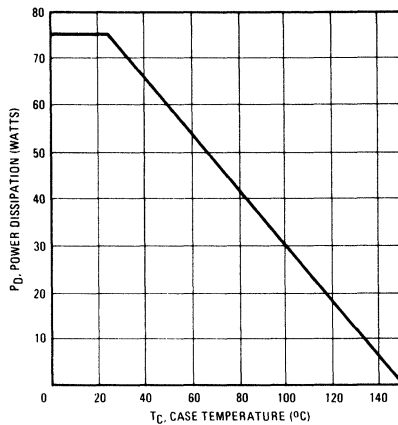


Fig. 15 — Clamped Inductive Test Circuit

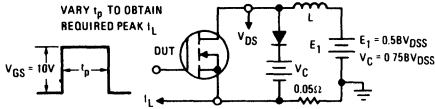


Fig. 16 — Clamped Inductive Waveforms

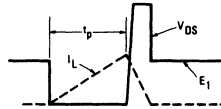


Fig. 17 — Switching Time Test Circuit

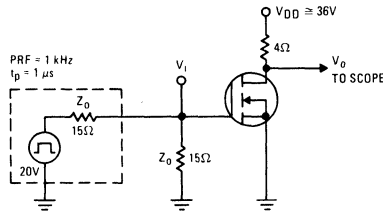
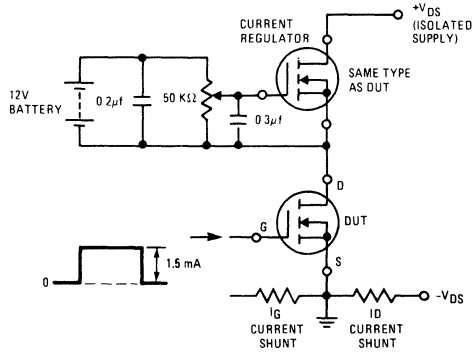


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.085 Ohm
N-Channel

UFN140
UFN141
UFN142
UFN143

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

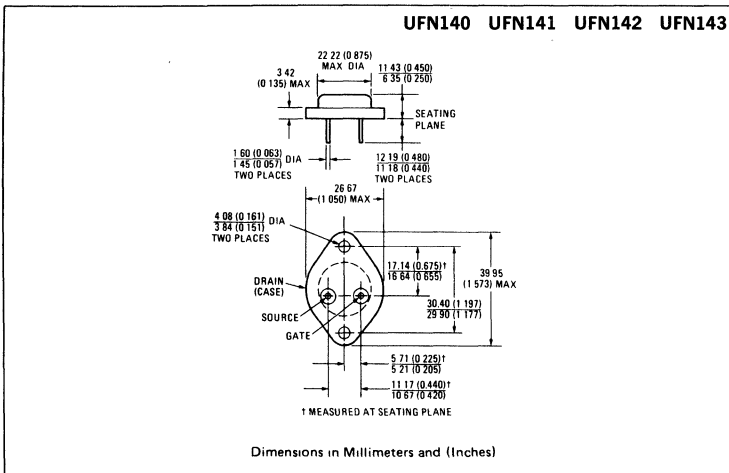
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

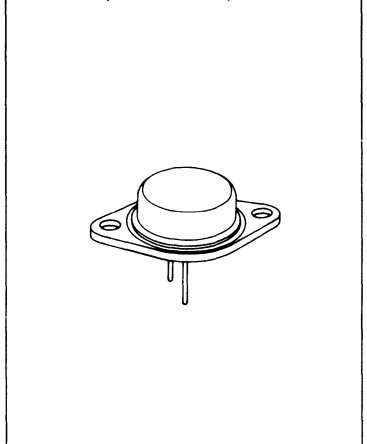
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN140	100V	0.085 Ω	27A
UFN141	60V	0.085 Ω	27A
UFN142	100V	0.11 Ω	24A
UFN143	60V	0.11 Ω	24A

MECHANICAL SPECIFICATIONS



TO-204AE (TO-3 modified)



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN140	UFN141	UFN142	UFN143	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	27	27	24	24	A
I _D @ T _C = 100°C Continuous Drain Current	17	17	15	15	A
I _{DM} Pulsed Drain Current ③	108	108	96	96	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125			(See Fig. 14)	W
		1.0		(See Fig. 14)	W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	108	108	96	96	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN140 UFN142	100	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN141 UFN143	60	—	—	V		
	ALL	2.0	—	4.0	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN140 UFN141	27	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN142 UFN143	24	—	—	A		
	ALL	—	—	—	—		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN140 UFN141	—	0.07	0.085	Ω	V _{GS} = 10V, I _D = 15A	
	UFN142 UFN143	—	0.09	0.11	Ω		
	ALL	—	—	—	—		
g _{fs} Forward Transconductance ②	ALL	6.0	10	—	S/(V)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 15A	
C _{iss} Input Capacitance	ALL	—	1275	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	550	800	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	160	300	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	16	30	ns	V _{DD} = 30V, I _D = 15A, Z _o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	27	60	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	38	80	ns		
t _f Fall Time	ALL	—	14	30	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V _{GS} = 10V, I _D = 34A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	17	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	21	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances.
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN140	-	-	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN141	-	-	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN140	-	-	108	A	
		UFN142	-	-	96	A	
V_{SD}	Diode Forward Voltage ②	UFN140	-	-	2.5	V	$T_C = 25^\circ\text{C}, I_S = 27\text{A}, V_{GS} = 0\text{V}$
		UFN141	-	-	2.3	V	
t_{rr}	Reverse Recovery Time	ALL	-	500	-	ns	$T_J = 150^\circ\text{C}, I_F = 27\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	-	2.9	-	μC	$T_J = 150^\circ\text{C}, I_F = 27\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

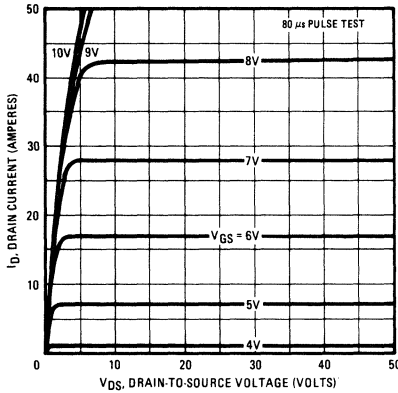


Fig. 2 – Typical Transfer Characteristics

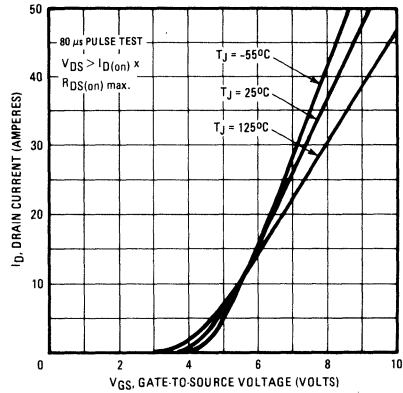


Fig. 3 – Typical Saturation Characteristics

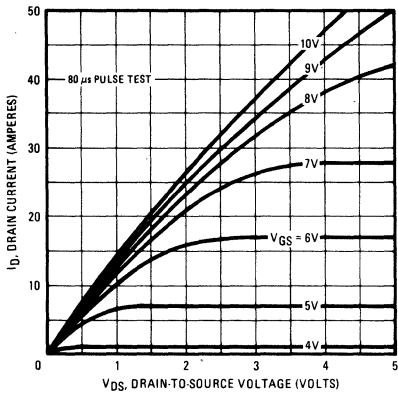


Fig. 4 – Maximum Safe Operating Area

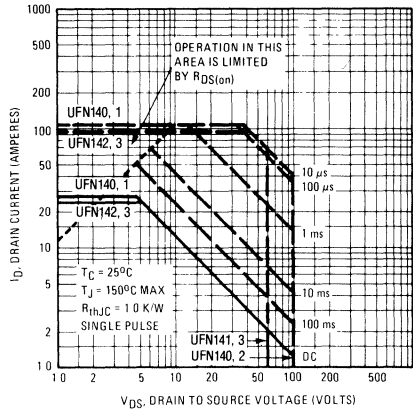
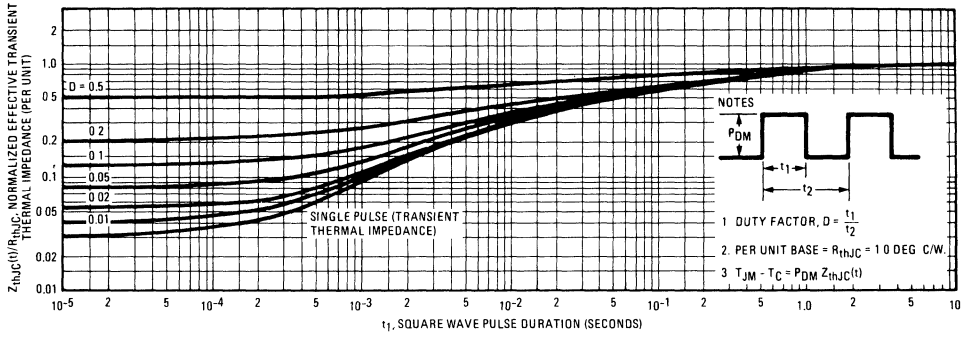


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

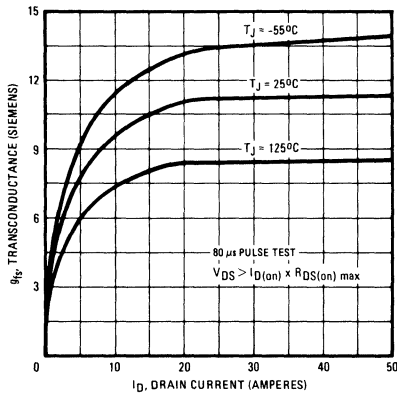


Fig. 7 – Typical Source-Drain Diode Forward Voltage

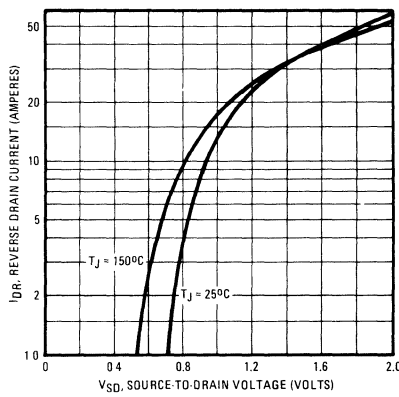


Fig. 8 – Breakdown Voltage Vs. Temperature

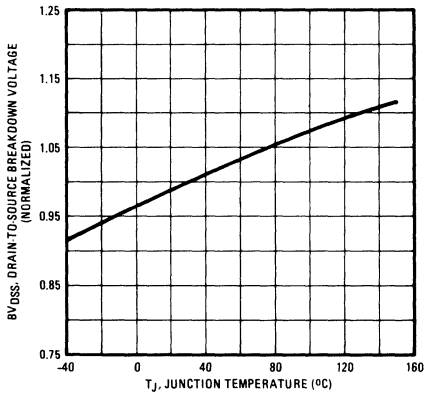


Fig. 9 – Normalized On-Resistance Vs. Temperature

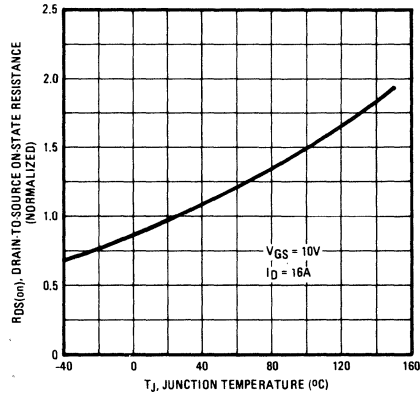


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

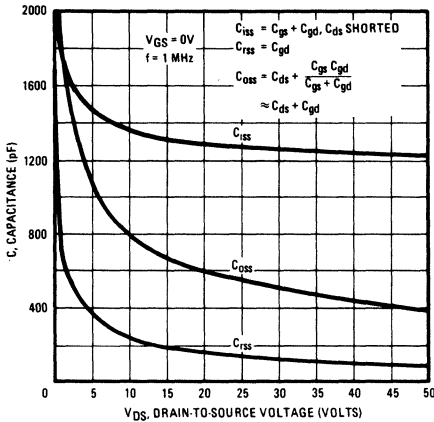


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

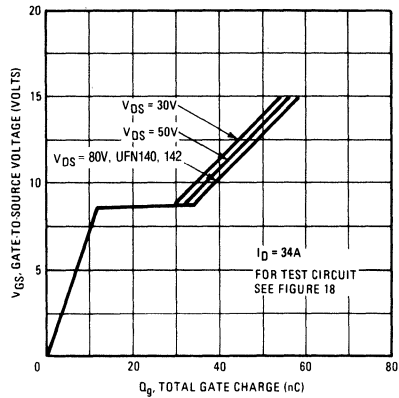


Fig. 12 – Typical On-Resistance Vs. Drain Current

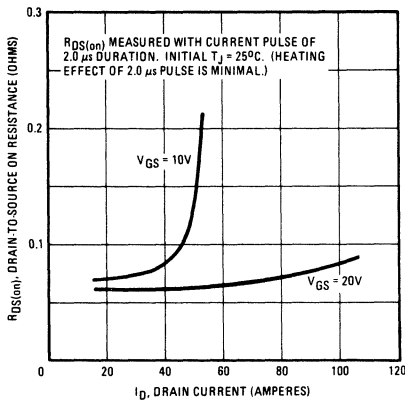


Fig. 13 – Maximum Drain Current Vs. Case Temperature

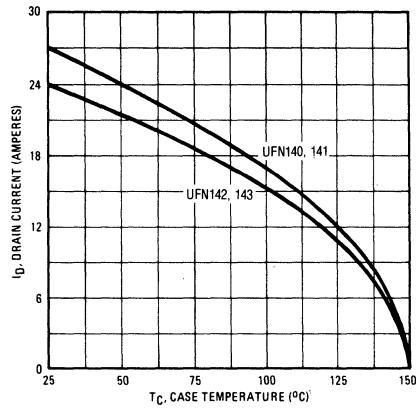


Fig. 14 – Power Vs. Temperature Derating Curve

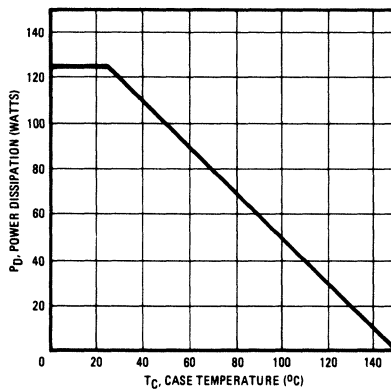


Fig. 15 — Clamped Inductive Test Circuit

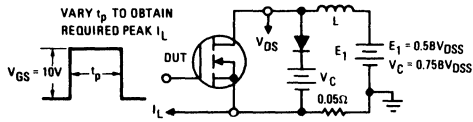


Fig. 16 — Clamped Inductive Waveforms

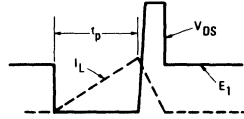


Fig. 17 — Switching Time Test Circuit

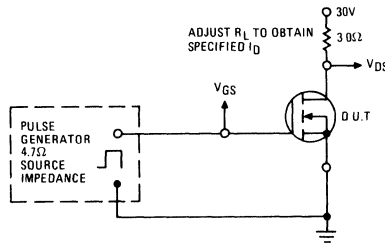
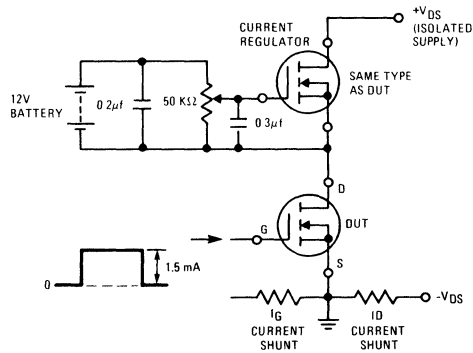


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.055 Ohm
N-Channel

UFN150
UFN151
UFN152
UFN153

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

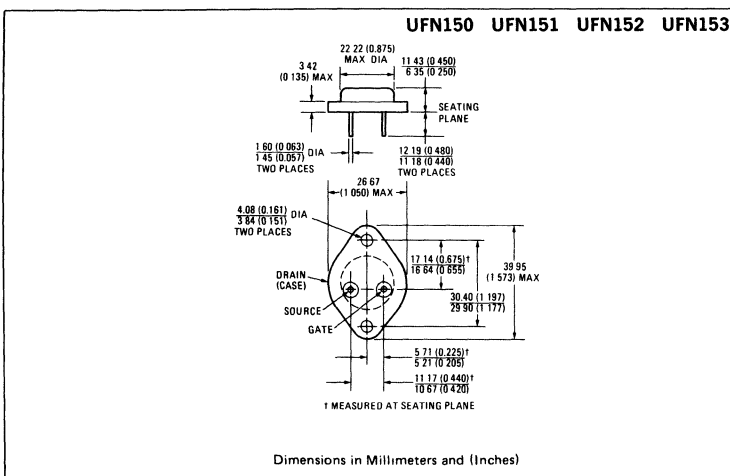
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

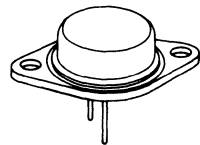
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN150	100V	0.055Ω	40A
UFN151	60V	0.055Ω	40A
UFN152	100V	0.08Ω	33A
UFN153	60V	0.08Ω	33A

MECHANICAL SPECIFICATIONS



TO-204AE (TO-3 modified)

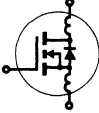


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN150	UFN151	UFN152	UFN153	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	40	40	33	33	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	25	25	20	20	A
I_{DM} Pulsed Drain Current ③	160	160	132	132	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN150 UFN152	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFN151 UFN153	60	—	—	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN150 UFN151	40	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFN152 UFN153	33	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN150 UFN151	—	0.045	0.055	Ω	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$	
	UFN152 UFN153	—	0.06	0.08	Ω		
g_{fs} Forward Transconductance ②	ALL	9.0	11	—	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 20\text{A}$	
C_{iss} Input Capacitance	ALL	—	2000	3000	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	1000	1500	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	350	500	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} = 24\text{V}$, $I_D = 20\text{A}$, $Z_o = 4.7\Omega$ See Figure 17.	
t_r Rise Time	ALL	—	—	100	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	125	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t_f Fall Time	ALL	—	—	100	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	63	120	nC	$V_{GS} = 10\text{V}$, $I_D = 50\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	27	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	36	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	0.83	K/W	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN150	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN151	—	—	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN150	—	—	160	A	
		UFN151	—	—	132	A	
V_{SD}	Diode Forward Voltage ②	UFN150	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 40\text{A}, V_{GS} = 0\text{V}$
		UFN151	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 33\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 40\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.3	—	μC	$T_J = 150^\circ\text{C}, I_F = 40\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

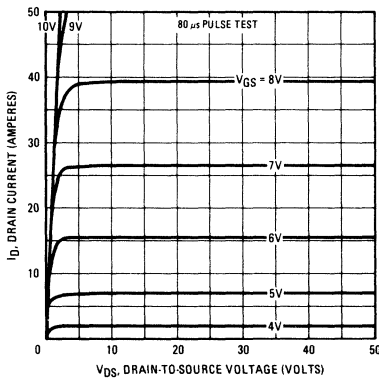


Fig. 2 – Typical Transfer Characteristics

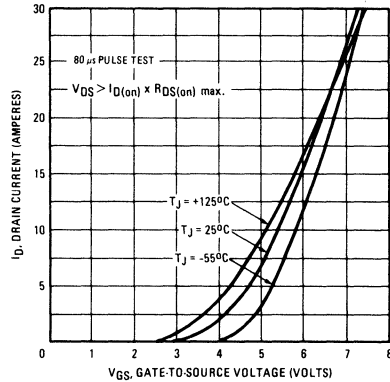


Fig. 3 – Typical Saturation Characteristics

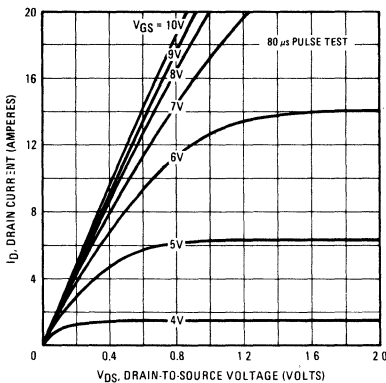


Fig. 4 – Maximum Safe Operating Area

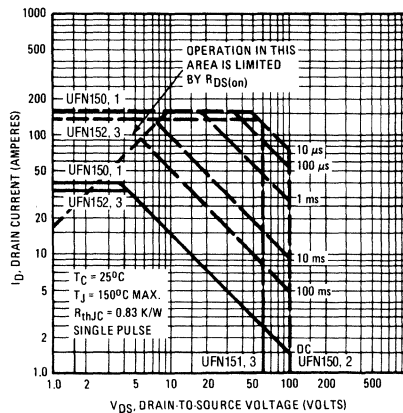


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

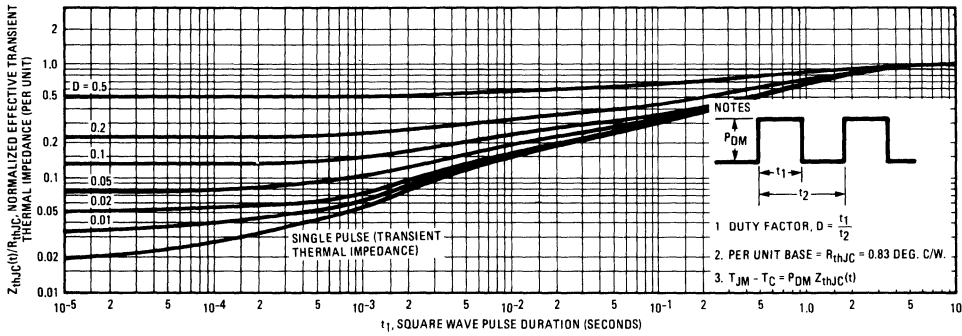


Fig. 6 – Typical Transconductance Vs. Drain Current

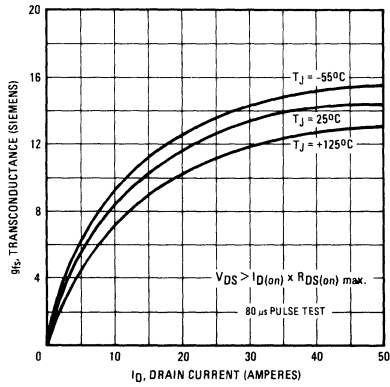


Fig. 7 – Typical Source-Drain Diode Forward Voltage

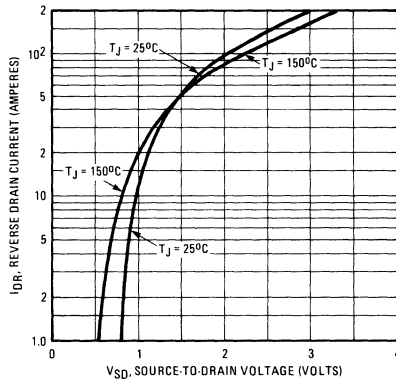


Fig. 8 – Breakdown Voltage Vs. Temperature

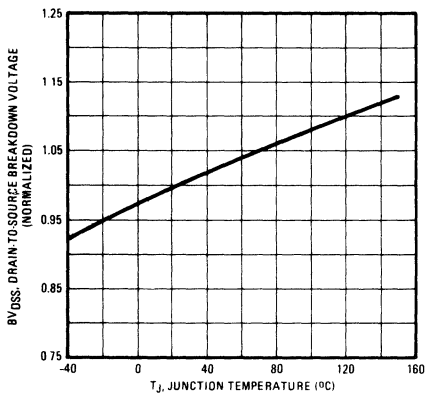


Fig. 9 – Normalized On-Resistance Vs. Temperature

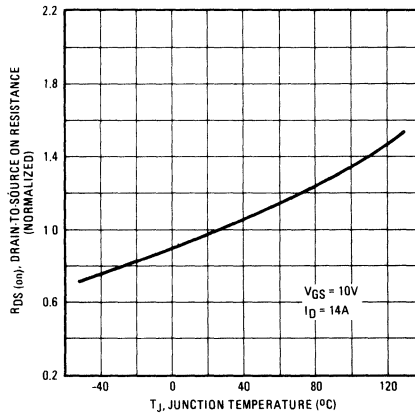


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

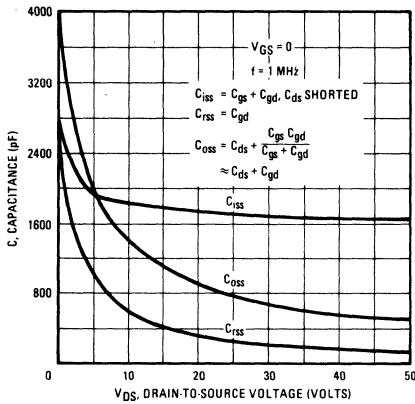


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

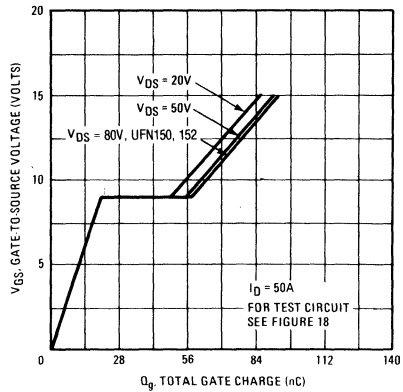


Fig. 12 — Typical On-Resistance Vs. Drain Current

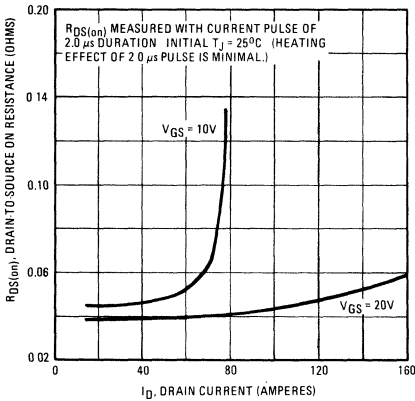


Fig. 13 — Maximum Drain Current Vs. Case Temperature

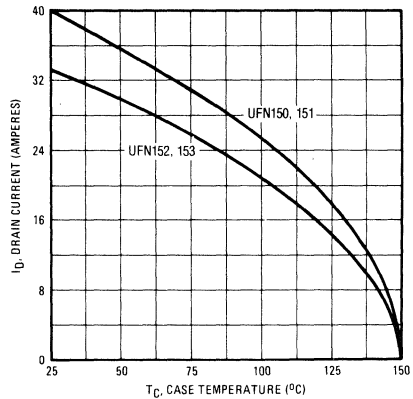


Fig. 14 — Power Vs. Temperature Derating Curve

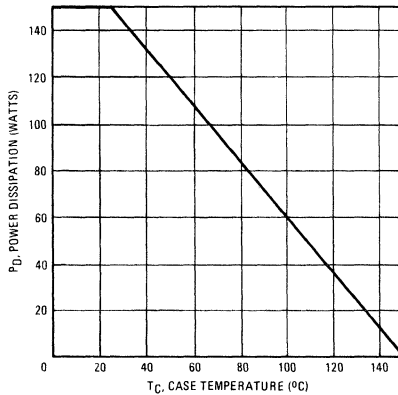


Fig. 15 – Clamped Inductive Test Circuit

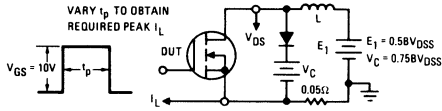


Fig. 16 – Clamped Inductive Waveforms

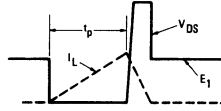


Fig. 17 – Switching Time Test Circuit

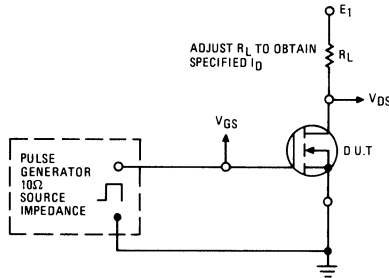
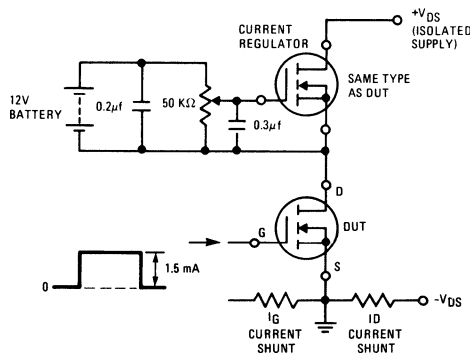


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.8 Ohm
N-Channel

UFN220
UFN221
UFN222
UFN223

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

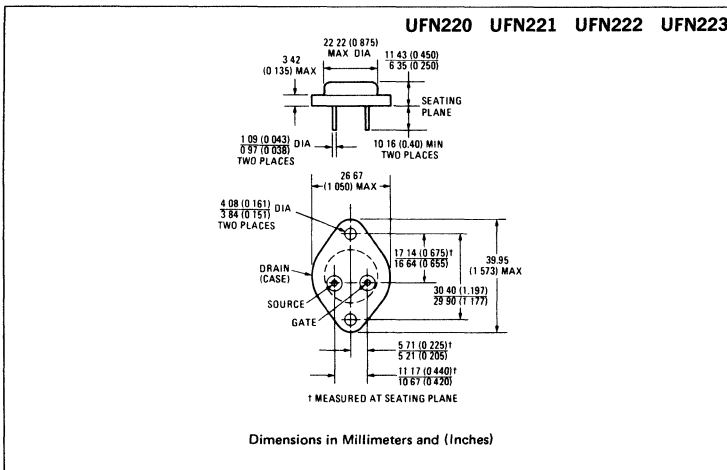
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

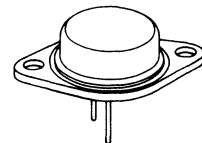
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN220	200V	0.8Ω	5.0A
UFN221	150V	0.8Ω	5.0A
UFN222	200V	1.2Ω	4.0A
UFN223	150V	1.2Ω	4.0A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)

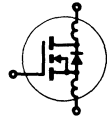


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN220	UFN221	UFN222	UFN223	Units
V _{DS} Drain - Source Voltage ①	200	150	200	150	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	5.0	5.0	4.0	4.0	A
I _D @ T _C = 100°C Continuous Drain Current	3.0	3.0	2.5	2.5	A
I _{DM} Pulsed Drain Current ③	20	20	16	16	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	20	20	16	16	
T _J Operating Junction and Storage Temperature Range	-50 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN220 UFN222	200	—	—	V	V _{GS} = 0V	
	UFN221 UFN223	150	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN220 UFN221	5.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN222 UFN223	4.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN220 UFN221	—	0.5	0.8	Ω	V _{GS} = 10V, I _D = 2.5A	
	UFN222 UFN223	—	0.8	1.2	Ω		
g _{fs} Forward Transconductance ②	ALL	1.3	2.5	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 2.5A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	150	300	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	40	80	pF	V _{DD} = 0.5 BV _{DSS} , I _D = 2.5A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns		
t _r Rise Time	ALL	—	30	60	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	30	60	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V _{GS} = 10V, I _D = 6.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	5.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN220	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN221	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN220	—	—	20	A	
		UFN221	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	UFN220	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 5.0\text{A}, V_{GS} = 0\text{V}$
		UFN221	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150^\circ\text{C}, I_F = 5.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150^\circ\text{C}, I_F = 5.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

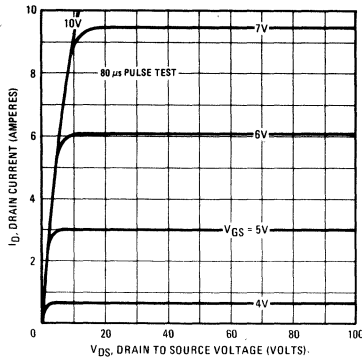


Fig. 2 – Typical Transfer Characteristics

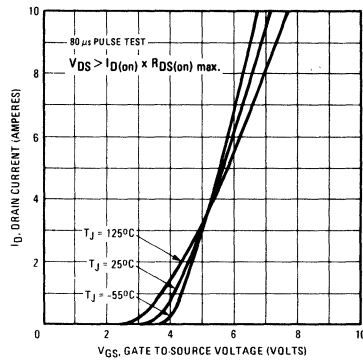


Fig. 3 – Typical Saturation Characteristics

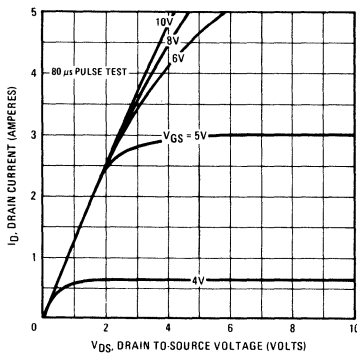


Fig. 4 – Maximum Safe Operating Area

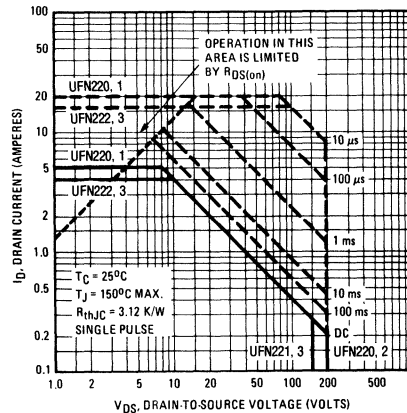
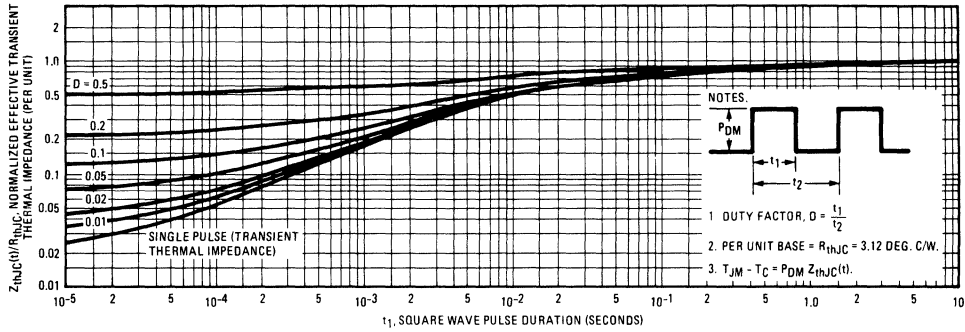


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

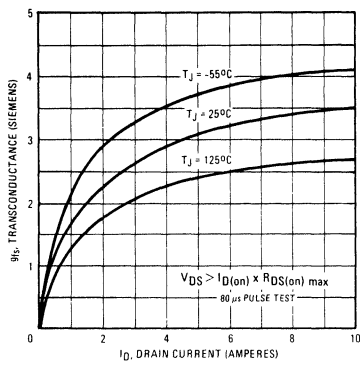


Fig. 7 – Typical Source-Drain Diode Forward Voltage

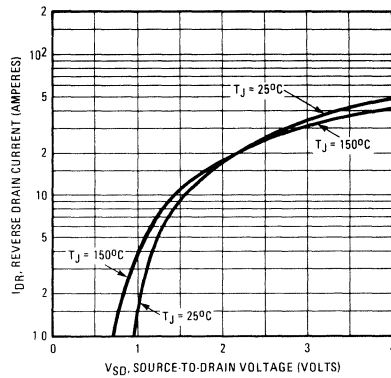


Fig. 8 – Breakdown Voltage Vs. Temperature

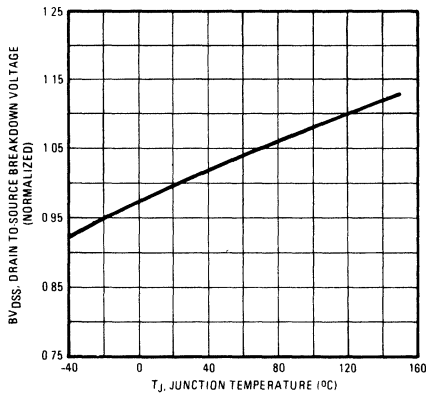


Fig. 9 – Normalized On-Resistance Vs. Temperature

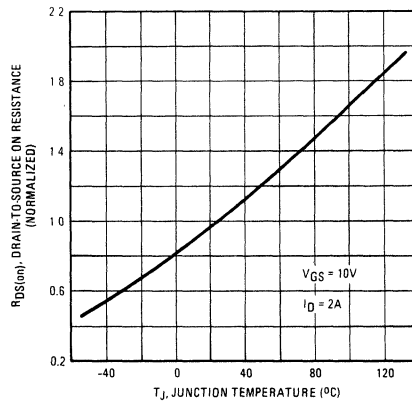


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

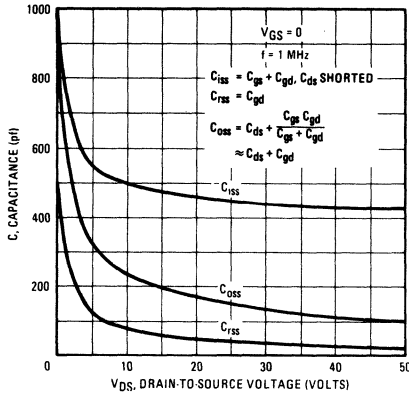


Fig. 12 – Typical On-Resistance Vs. Drain Current

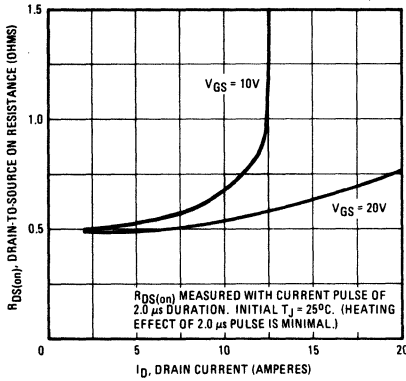


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

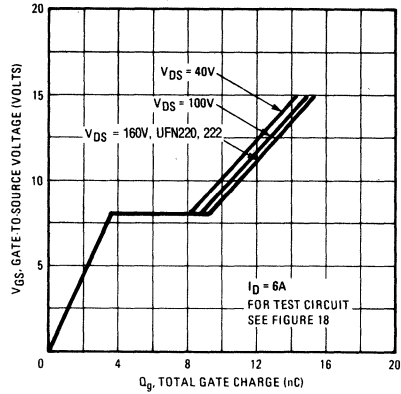


Fig. 13 – Maximum Drain Current Vs. Case Temperature

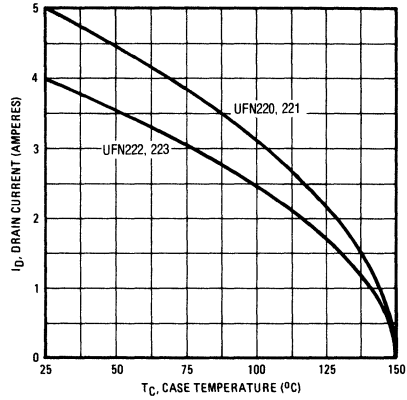


Fig. 14 – Power Vs. Temperature Derating Curve

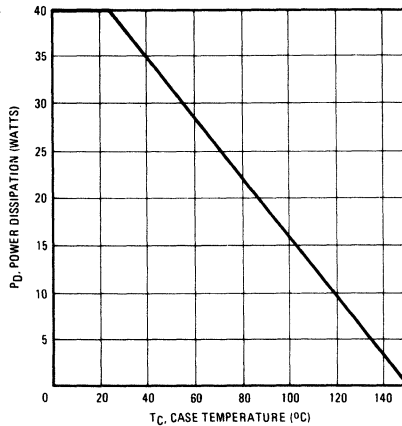


Fig. 15 — Clamped Inductive Test Circuit

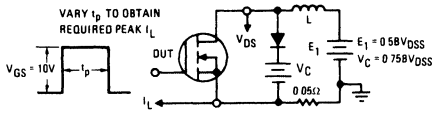


Fig. 16 — Clamped Inductive Waveforms

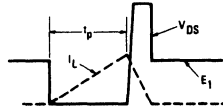


Fig. 17 — Switching Time Test Circuit

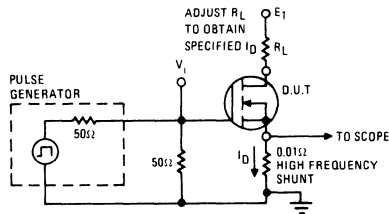
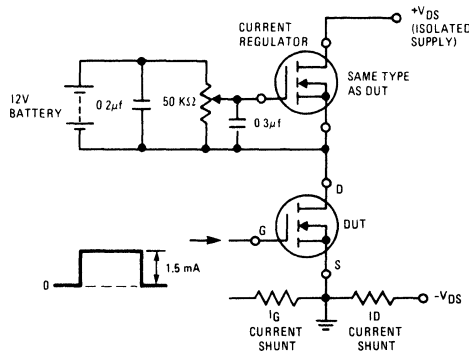


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm
N-Channel

UFN230
UFN231
UFN232
UFN233

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

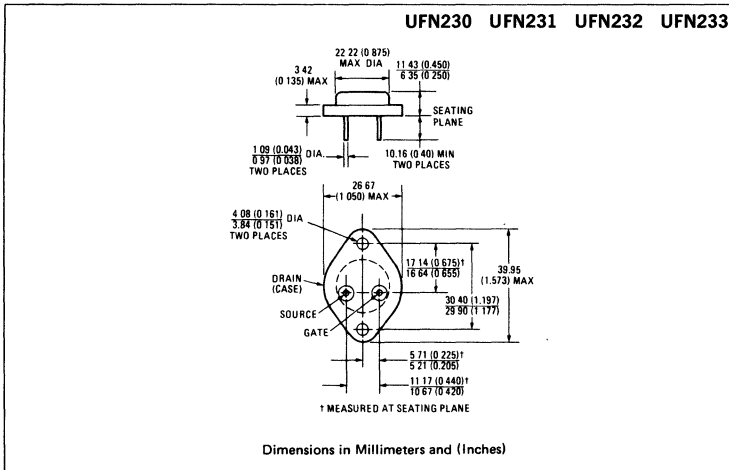
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

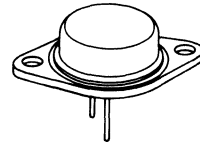
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN230	200V	0.4Ω	9.0A
UFN231	150V	0.4Ω	9.0A
UFN232	200V	0.6Ω	8.0A
UFN233	150V	0.6Ω	8.0A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)

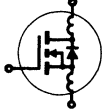


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN230	UFN231	UFN232	UFN233	Units
V_{DS} Drain - Source Voltage ①	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	9.0	9.0	8.0	8.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM} Pulsed Drain Current ③	36	36	32	32	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN230 UFN232	200	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFN231 UFN233	150	—	—	V		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN230 UFN231	9.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFN232 UFN233	8.0	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN230 UFN231	—	0.25	0.4	Ω	$V_{GS} = 10\text{V}$, $I_D = 5.0\text{A}$	
	UFN232 UFN233	—	0.4	0.6	Ω		
g_{fs} Forward Transconductance ②	ALL	3.0	4.8	—	S (f)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 5.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	600	800	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	250	450	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	80	150	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \approx 90\text{V}$, $I_D = 5.0\text{A}$, $Z_o = 15\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	—	50	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	50	ns		
t_f Fall Time	ALL	—	—	40	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	$V_{GS} = 10\text{V}$, $I_D = 12\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	10	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN230	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
		UFN231	—	—	8.0	A		
I_{SM}	Pulse Source Current (Body Diode) ③	UFN230	—	—	36	A		
		UFN231	—	—	32	A		
V_{SD}	Diode Forward Voltage ②	UFN230	—	—	2.0	V		$T_C = 25^\circ\text{C}, I_S = 9.0\text{A}, V_{GS} = 0\text{V}$
		UFN231	—	—	1.8	V		$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

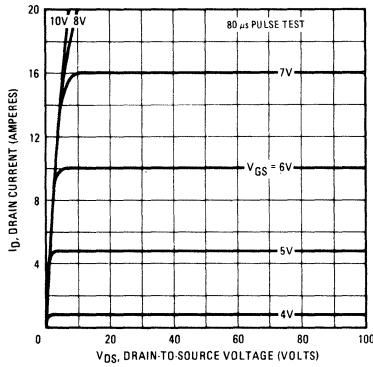


Fig. 2 – Typical Transfer Characteristics

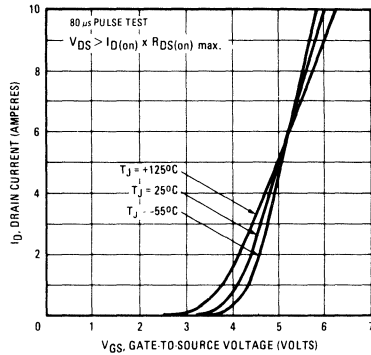


Fig. 3 – Typical Saturation Characteristics

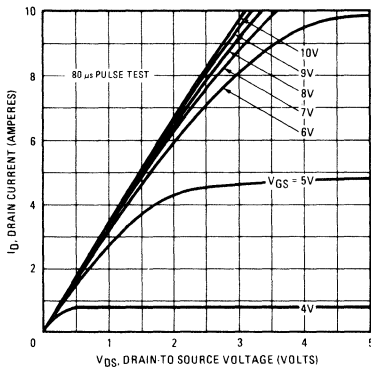


Fig. 4 – Maximum Safe Operating Area

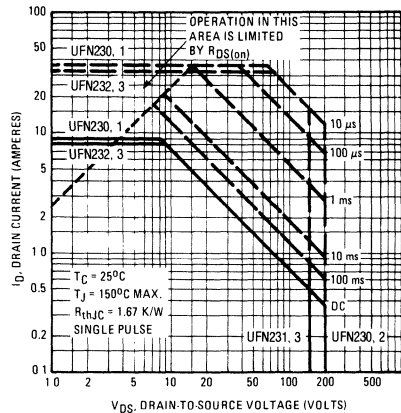
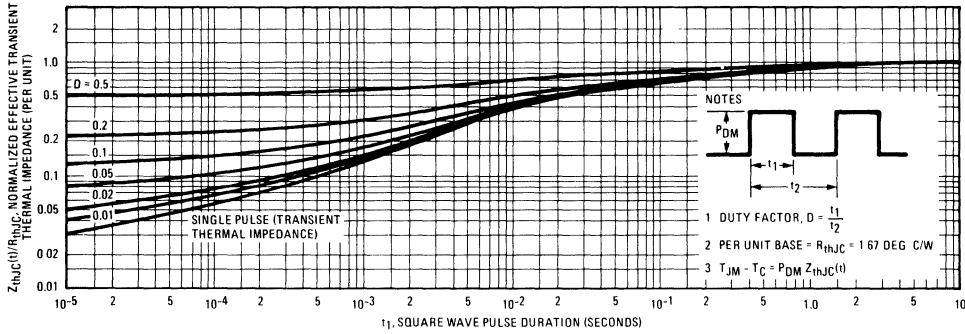


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

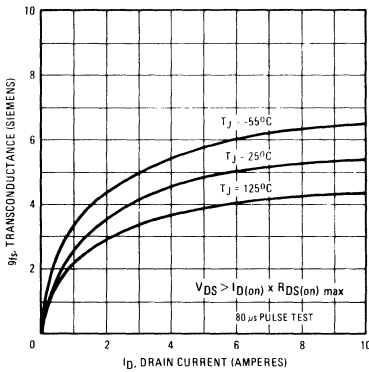


Fig. 7 – Typical Source-Drain Diode Forward Voltage

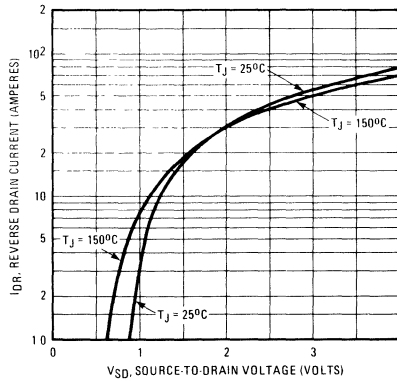


Fig. 8 – Breakdown Voltage Vs. Temperature

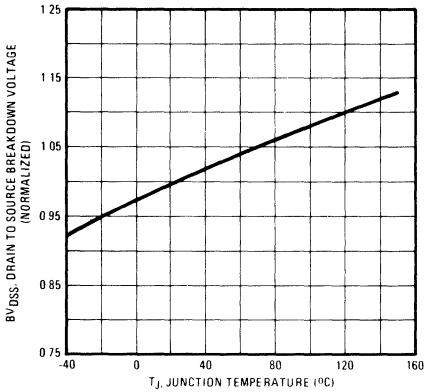


Fig. 9 – Normalized On-Resistance Vs. Temperature

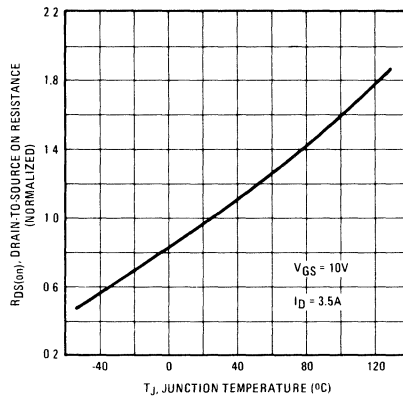


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

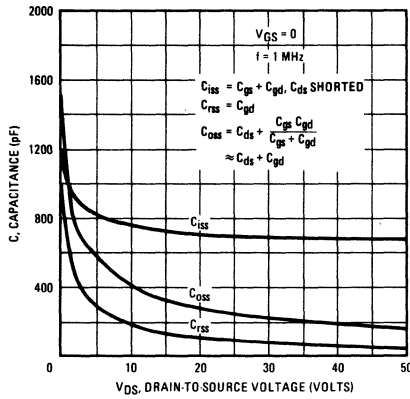


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

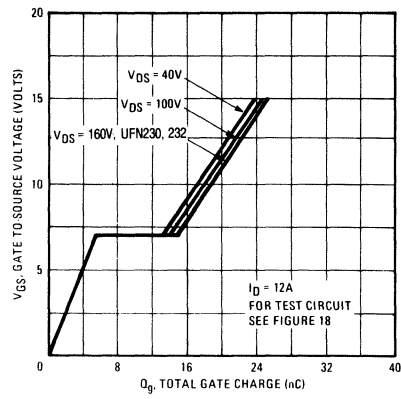


Fig. 12 – Typical On-Resistance Vs. Drain Current

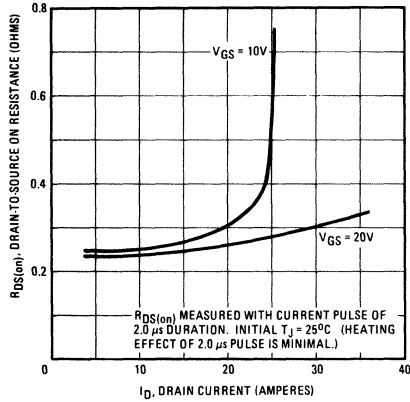


Fig. 13 – Maximum Drain Current Vs. Case Temperature

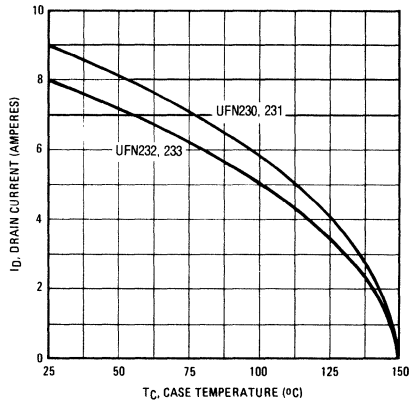


Fig. 14 – Power Vs. Temperature Derating Curve

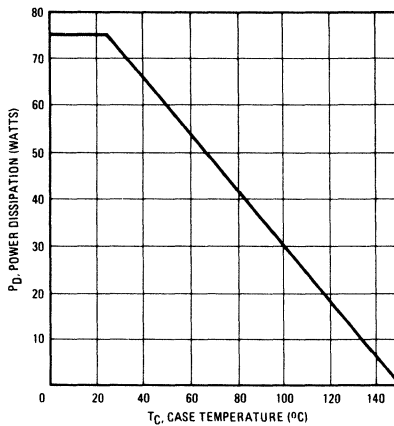


Fig. 15 – Clamped Inductive Test Circuit

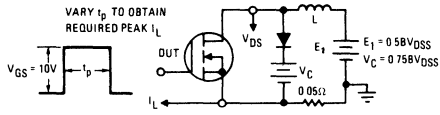


Fig. 16 – Clamped Inductive Waveforms

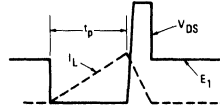


Fig. 17 – Switching Time Test Circuit

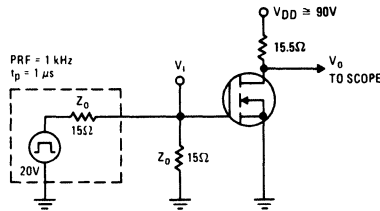
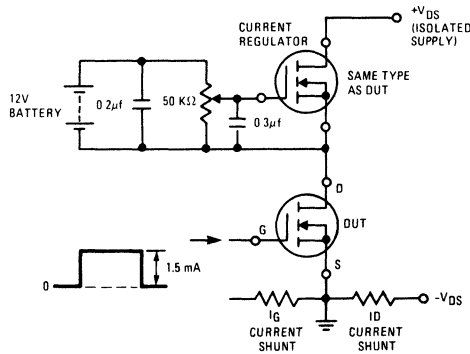


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.2 Ohm
N-Channel

UFN240
UFN241
UFN242
UFN243

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

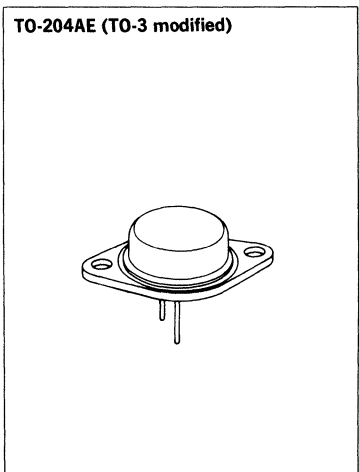
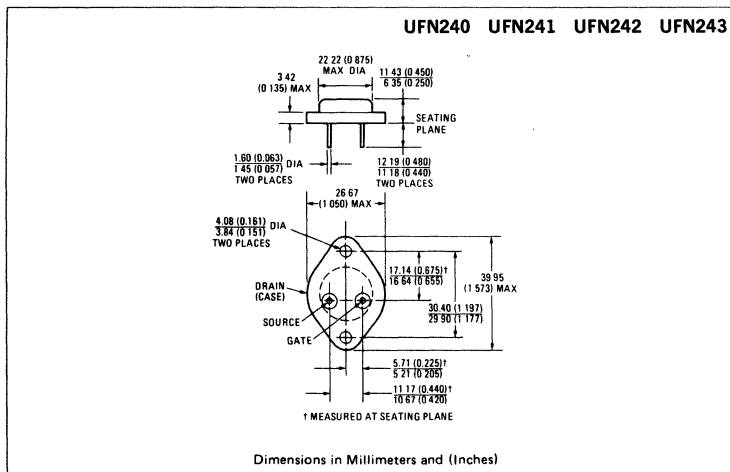
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN240	200V	0.18 Ω	18A
UFN241	150V	0.18 Ω	18A
UFN242	200V	0.22 Ω	16A
UFN243	150V	0.22 Ω	16A

MECHANICAL SPECIFICATIONS

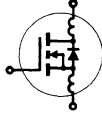


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN240	UFN241	UFN242	UFN243	Units
V_{DS} Drain - Source Voltage ①	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	18	18	16	16	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	11	11	10	10	A
I_{DM} Pulsed Drain Current ③	72	72	64	64	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	72	(See Fig. 15 and 16) L = 100 μ H 72	64	64	A
T_J T_{stg} Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN240 UFN242	200	—	—	V	$V_{GS} = 0\text{V}$	
	UFN241 UFN243	150	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN240 UFN241	18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$	
	UFN242 UFN243	16	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN240 UFN241	—	0.14	0.18	Ω	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	
	UFN242 UFN243	—	0.20	0.22	Ω		
g_{fs} Forward Transconductance ②	ALL	6.0	9.0	—	S (f)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 10\text{A}$	
C_{iss} Input Capacitance	ALL	—	1275	1600	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	500	750	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	160	300	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} = 75\text{V}, I_D = 10\text{A}, Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	27	60	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	40	80	ns		
t_f Fall Time	ALL	—	31	60	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC		$V_{GS} = 10\text{V}, I_D = 22\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	16	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	27	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN240	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN241	—	—	16	A	
		UFN242 UFN243	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN240	—	—	72	A	
		UFN242 UFN243	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	UFN240 UFN241	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 18\text{A}, V_{GS} = 0\text{V}$
		UFN242 UFN243	—	—	1.9	V	$T_C = 25^\circ\text{C}, I_S = 16\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	$T_J = 150^\circ\text{C}, I_F = 18\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 18\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

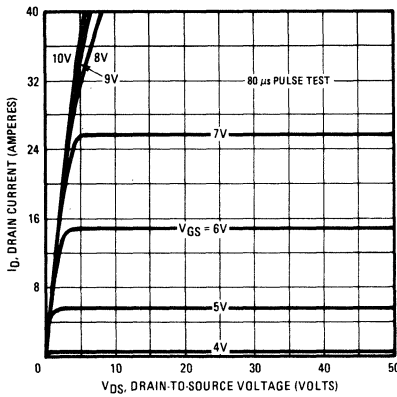


Fig. 2 – Typical Transfer Characteristics

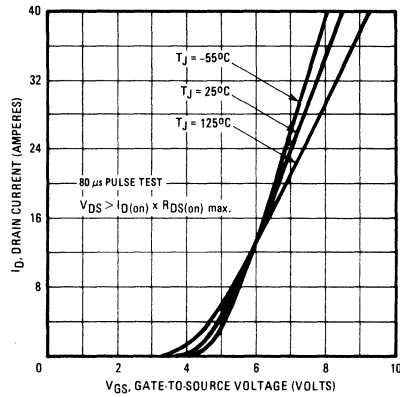


Fig. 3 – Typical Saturation Characteristics

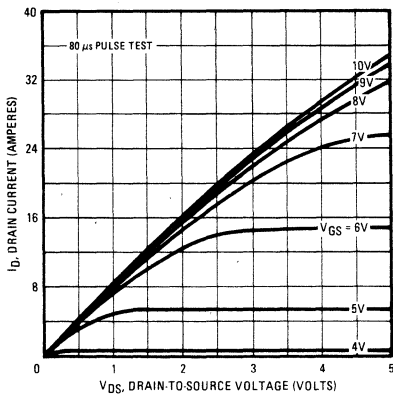


Fig. 4 – Maximum Safe Operating Area

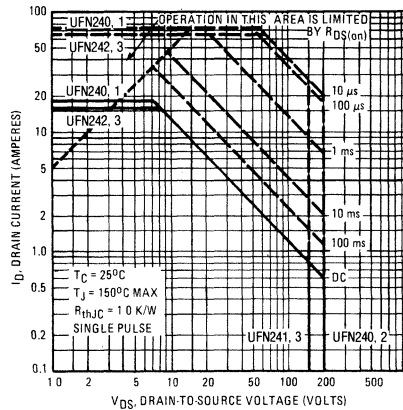


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

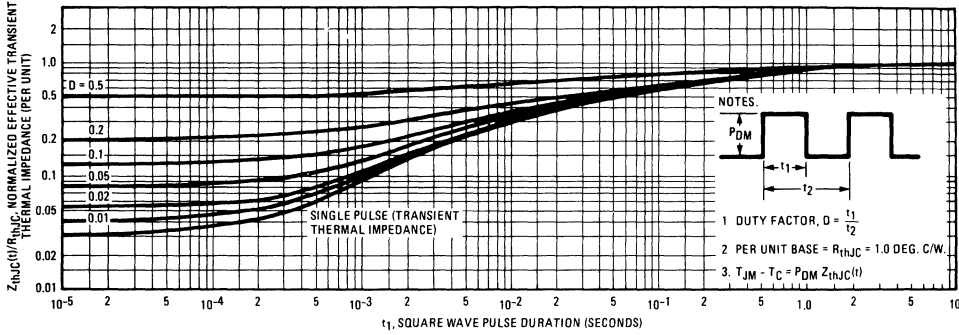


Fig. 6 – Typical Transconductance Vs. Drain Current

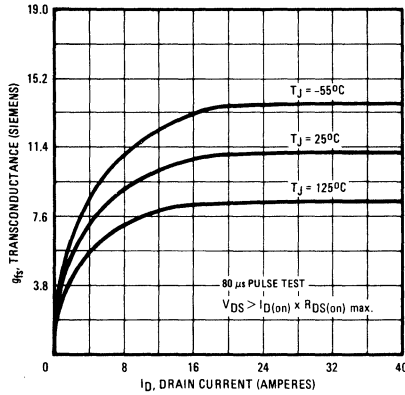


Fig. 7 – Typical Source-Drain Diode Forward Voltage

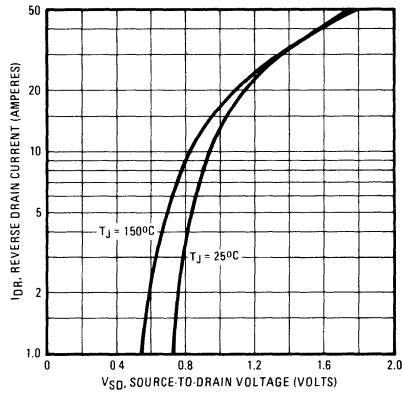


Fig. 8 – Breakdown Voltage Vs. Temperature

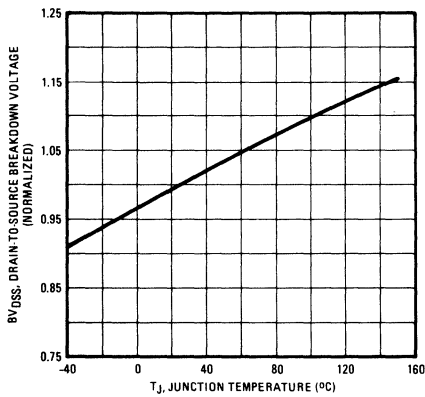


Fig. 9 – Normalized On-Resistance Vs. Temperature

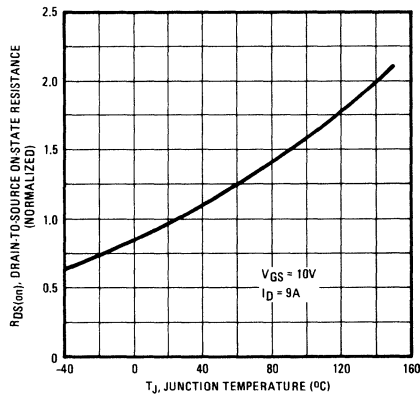


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

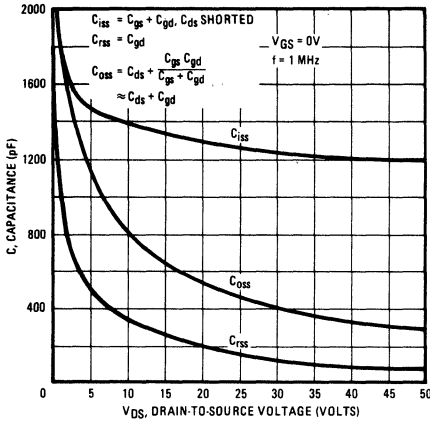


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

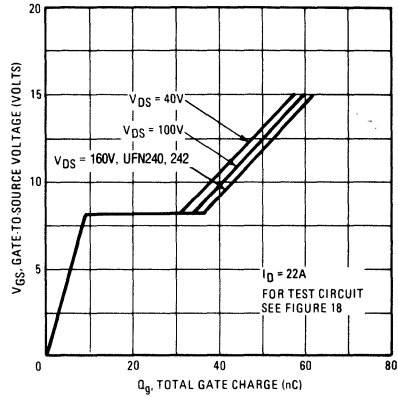


Fig. 12 — Typical On-Resistance Vs. Drain Current

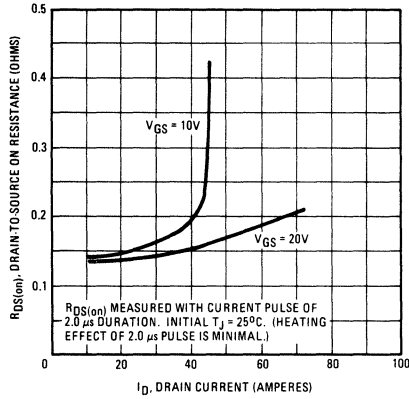


Fig. 13 — Maximum Drain Current Vs. Case Temperature

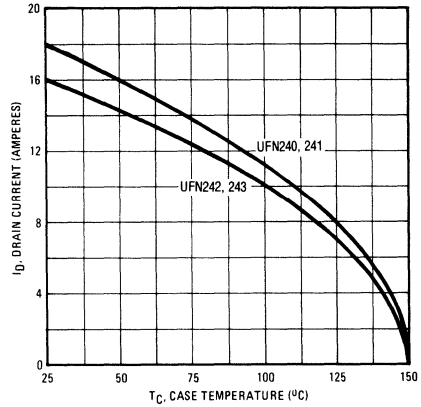


Fig. 14 — Power Vs. Temperature Derating Curve

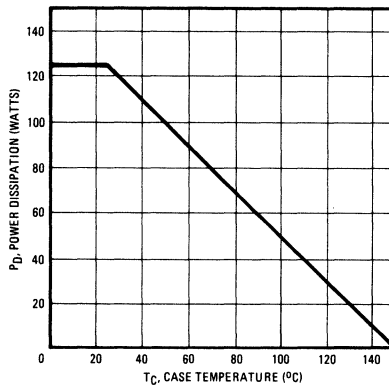


Fig. 15 - Clamped Inductive Test Circuit

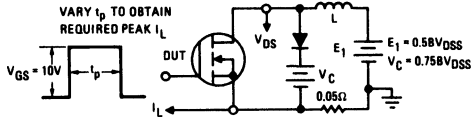


Fig. 16 - Clamped Inductive Waveforms

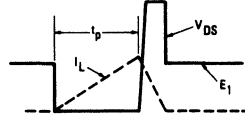


Fig. 17 - Switching Time Test Circuit

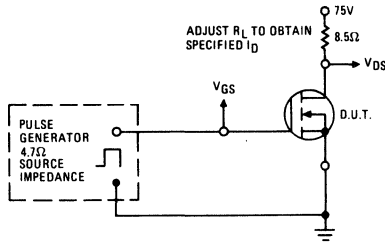
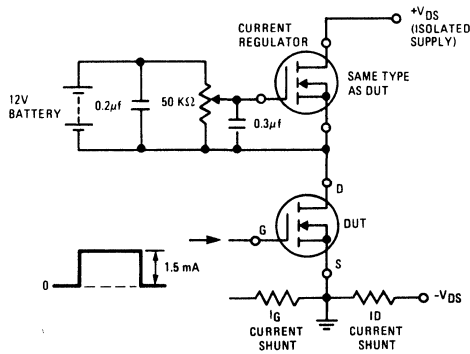


Fig. 18 - Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.085 Ohm
N-Channel

UFN250
UFN251
UFN252
UFN253

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

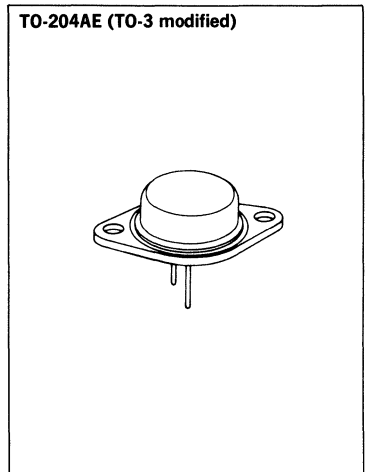
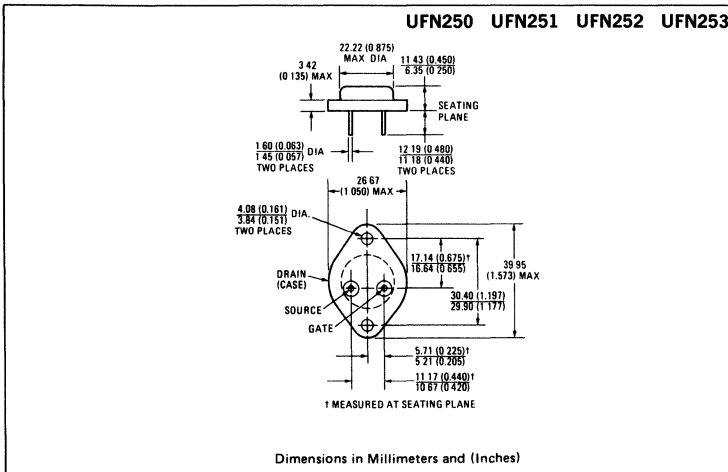
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN250	200V	0.085 Ω	30A
UFN251	150V	0.085 Ω	30A
UFN252	200V	0.120 Ω	25A
UFN253	150V	0.120 Ω	25A

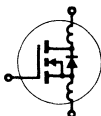
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN250	UFN251	UFN252	UFN253	Units
V _{DS} Drain - Source Voltage ①	200	150	200	150	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	30	30	25	25	A
I _D @ T _C = 100°C Continuous Drain Current	19	19	16	16	A
I _{DM} Pulsed Drain Current ③	120	120	100	100	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	120	120	100	100	°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN250 UFN252	200	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN251 UFN253	150	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN250 UFN251	30	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN252 UFN253	25	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN250 UFN251	—	0.07	0.085	Ω	V _{GS} = 10V, I _D = 16A	
	UFN252 UFN253	—	0.09	0.120	Ω		
g _{fs} Forward Transconductance ②	ALL	8.0	14	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 16A	
C _{iss} Input Capacitance	ALL	—	2000	3000	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	800	1200	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	300	500	pF	V _{DD} = 95V, I _D = 16A, Z _o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _{d(on)} Turn-On Delay Time	ALL	—	—	35	ns		
t _r Rise Time	ALL	—	—	100	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	125	ns		
t _f Fall Time	ALL	—	—	100	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V _{GS} = 10V, I _D = 38A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	37	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	42	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	0.83	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN250	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN251	—	—	25	A	
UFN252	UFN253	—	—	25	A		
I_{SM}	Pulse Source Current (Body Diode) ③	UFN250	—	—	120	A	
		UFN251	—	—	100	A	
UFN252	UFN253	—	—	100	A		
V_{SD}	Diode Forward Voltage ②	UFN250	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 30\text{A}, V_{GS} = 0\text{V}$
		UFN251	—	—	1.8	V	
UFN252	UFN253	—	—	1.8	V	$T_C = 25^\circ\text{C}, I_S = 25\text{A}, V_{GS} = 0\text{V}$	
t_{rr}	Reverse Recovery Time	ALL	—	750	—	ns	$T_J = 150^\circ\text{C}, I_F = 30\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 30\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

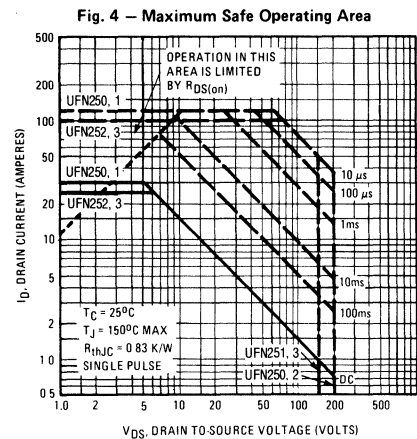
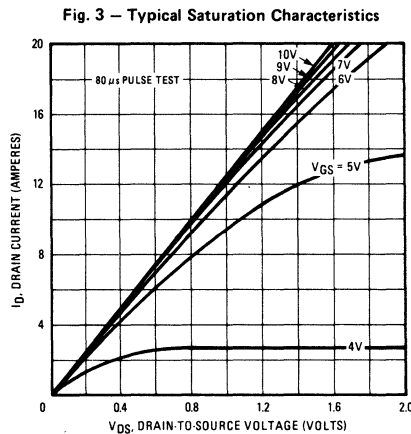
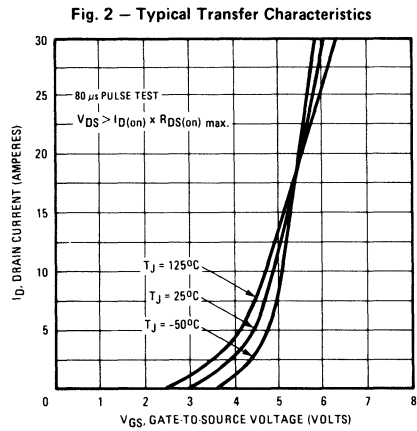
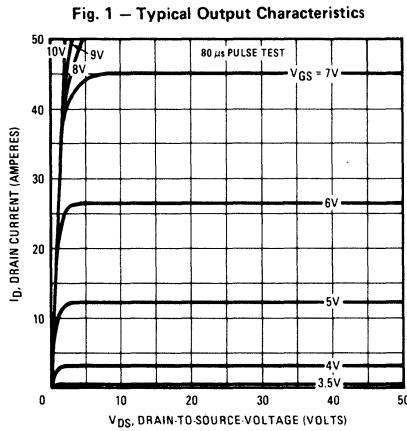


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

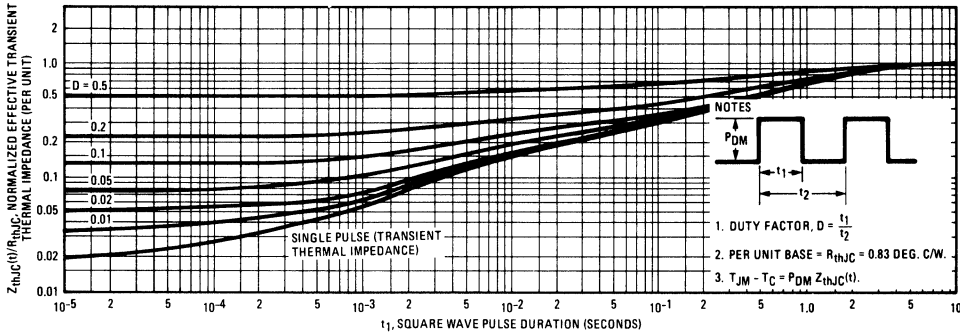


Fig. 6 – Typical Transconductance Vs. Drain Current

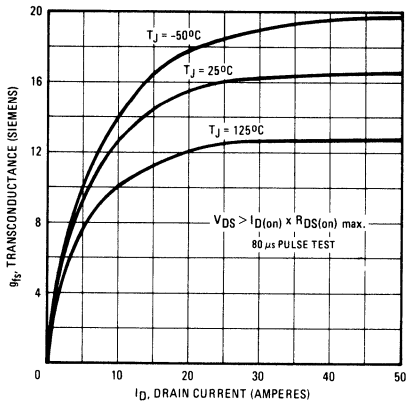


Fig. 7 – Typical Source-Drain Diode Forward Voltage

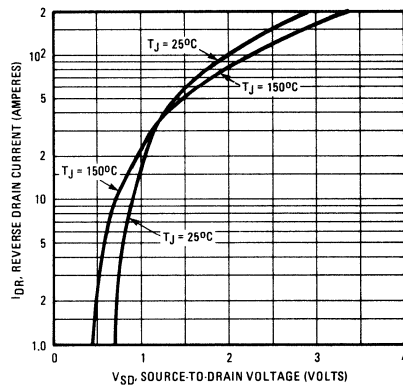


Fig. 8 – Breakdown Voltage Vs. Temperature

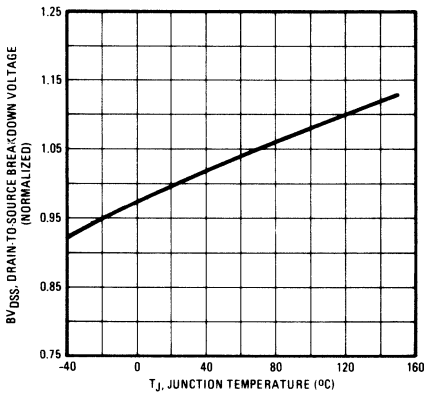


Fig. 9 – Normalized On-Resistance Vs. Temperature

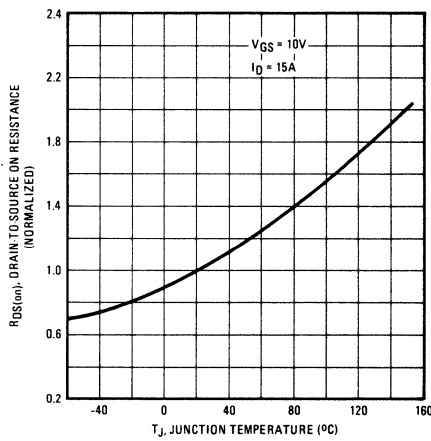


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

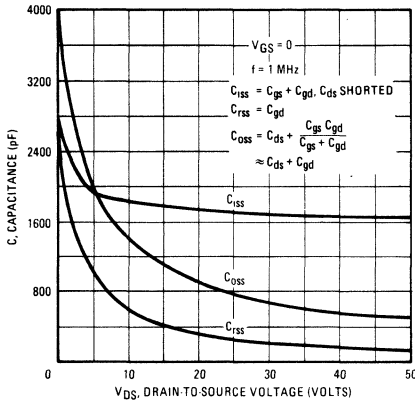


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

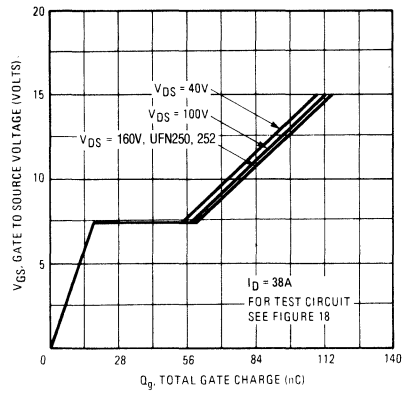


Fig. 12 – Typical On-Resistance Vs. Drain Current

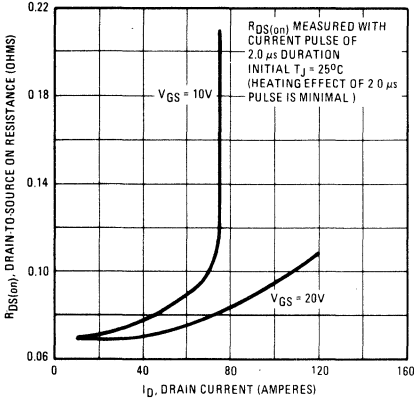


Fig. 13 – Maximum Drain Current Vs. Case Temperature

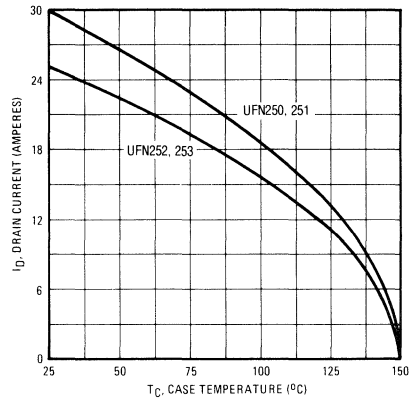


Fig. 14 – Power Vs. Temperature Derating Curve

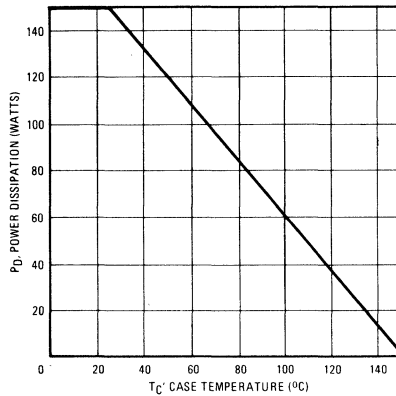


Fig. 15 – Clamped Inductive Test Circuit

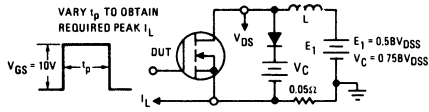


Fig. 16 – Clamped Inductive Waveforms

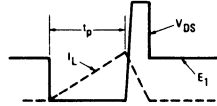


Fig. 17 – Switching Time Test Circuit

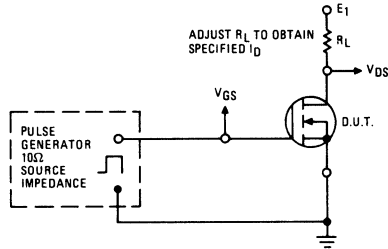
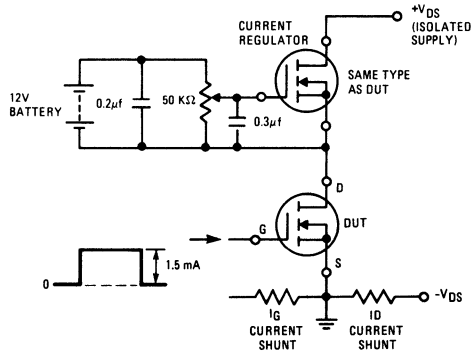


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.8 Ohm N-Channel

UFN320
UFN321
UFN322
UFN323

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

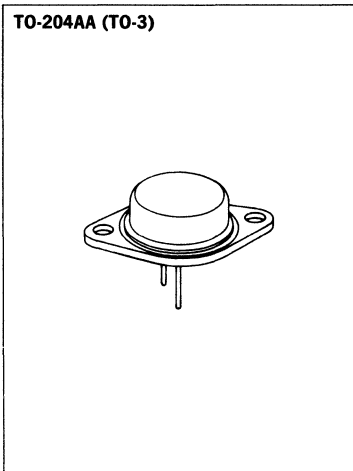
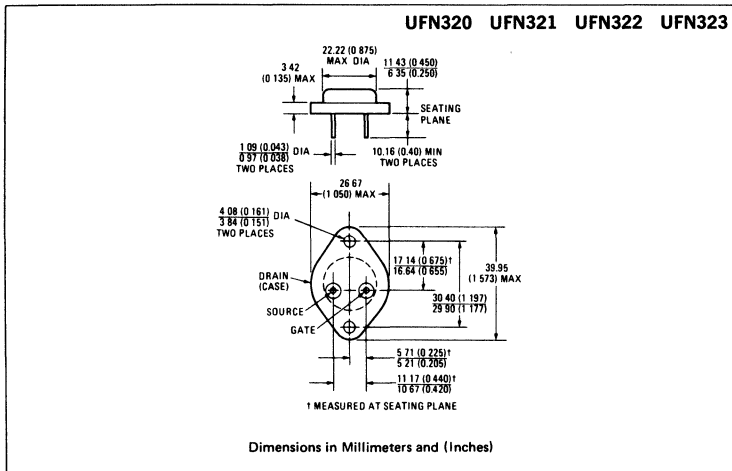
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN320	400V	1.8Ω	3.0A
UFN321	350V	1.8Ω	3.0A
UFN322	400V	2.5Ω	2.5A
UFN323	350V	2.5Ω	2.5A

MECHANICAL SPECIFICATIONS

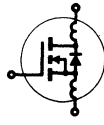


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN320	UFN321	UFN322	UFN323	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	3.0	3.0	2.5	2.5	A
I _D @ T _C = 100°C Continuous Drain Current	2.0	2.0	1.5	1.5	A
I _{DM} Pulsed Drain Current ③	12	12	10	10	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	12	12	10	10	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

4


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN320 UFN322	400	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN321 UFN323	350	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN320 UFN321	3.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN322 UFN323	2.5	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN320 UFN321	—	1.5	1.8	Ω	V _{GS} = 10V, I _D = 1.5A	
	UFN322 UFN323	—	1.8	2.5	Ω		
	—	—	—	—	—		—
g _{fs} Forward Transconductance ②	ALL	1.0	2.0	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 1.5A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	100	200	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	20	40	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 1.5A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	25	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	25	50	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V _{GS} = 10V, I _D = 4.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN320	-	-	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
		UFN321	-	-	2.5	A		
I_{SM}	Pulse Source Current (Body Diode) ③	UFN320	-	-	12	A		
		UFN321	-	-	10	A		
V_{SD}	Diode Forward Voltage ②	UFN320	-	-	1.6	V	$T_C = 25^\circ\text{C}, I_S = 3.0\text{A}, V_{GS} = 0\text{V}$	
		UFN321	-	-	1.5	V		
t_{rr}	Reverse Recovery Time	ALL	-	450	-	ns	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	-	3.1	-	μC	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

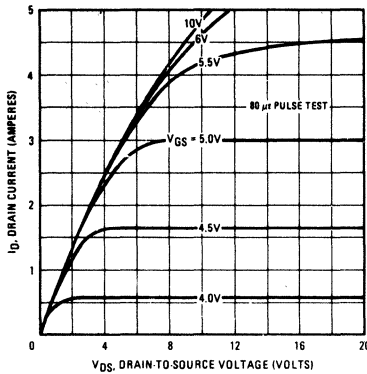


Fig. 2 – Typical Transfer Characteristics

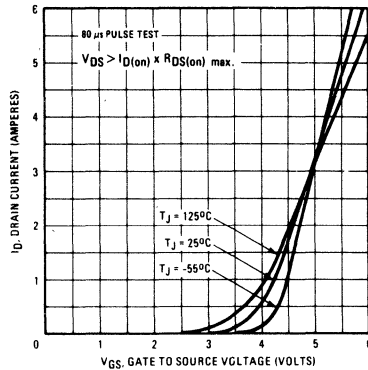


Fig. 3 – Typical Saturation Characteristics

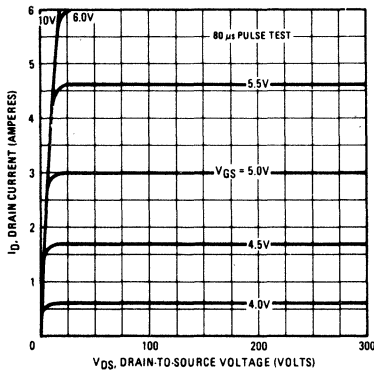


Fig. 4 – Maximum Safe Operating Area

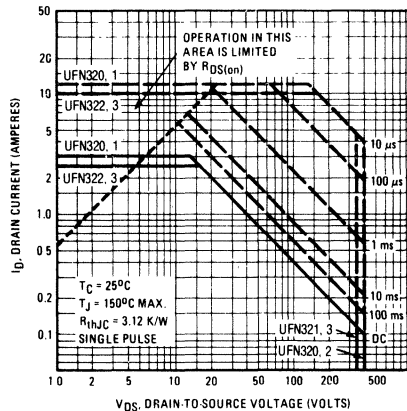
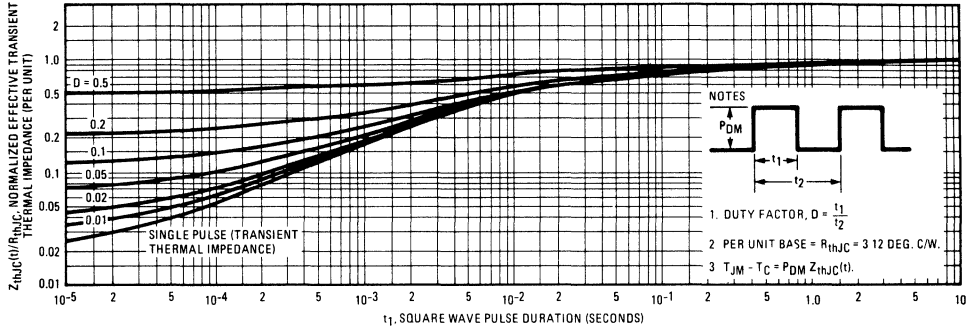


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

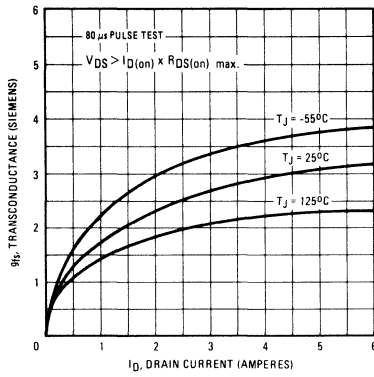


Fig. 7 – Typical Source-Drain Diode Forward Voltage

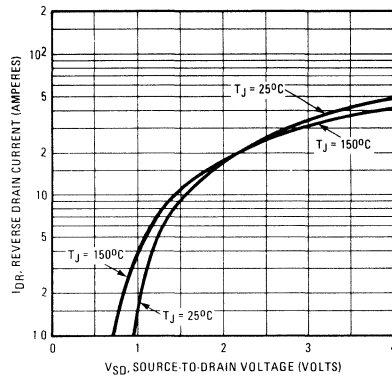


Fig. 8 – Breakdown Voltage Vs. Temperature

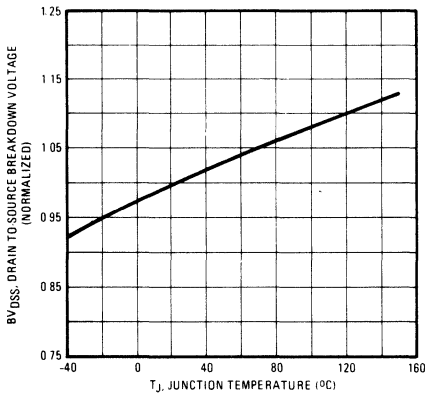


Fig. 9 – Normalized On-Resistance Vs. Temperature

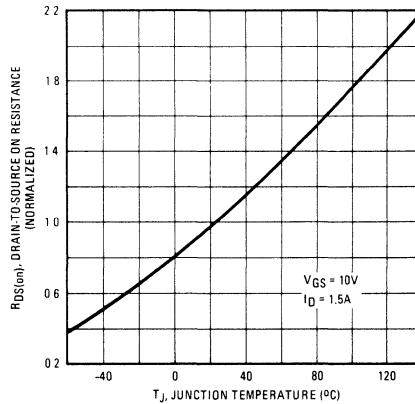


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

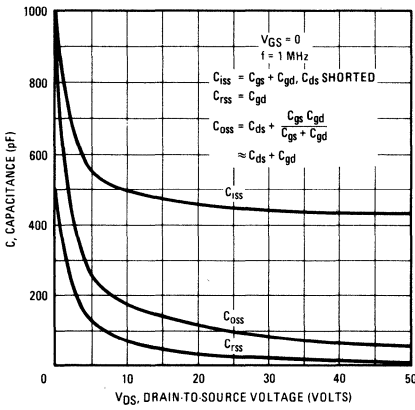


Fig. 12 – Typical On-Resistance Vs. Drain Current

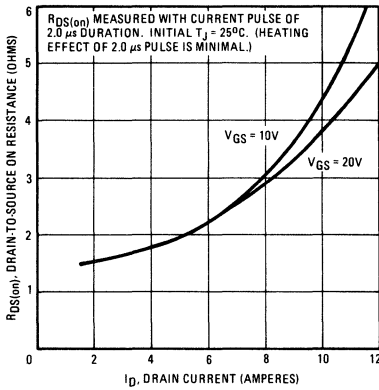


Fig. 14 – Power Vs. Temperature Derating Curve

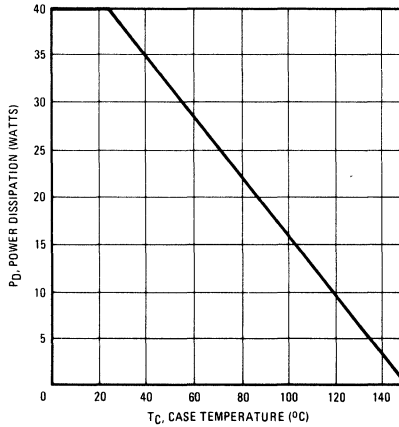


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

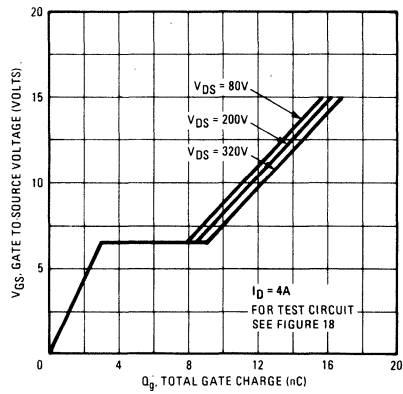


Fig. 13 – Maximum Drain Current Vs. Case Temperature

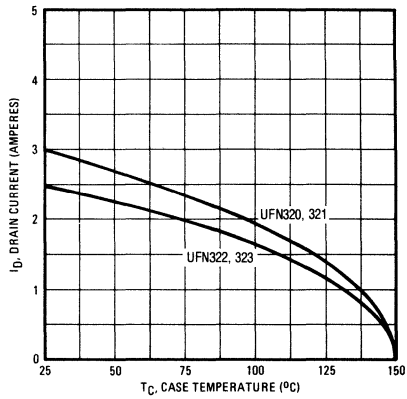


Fig. 15 – Clamped Inductive Test Circuit

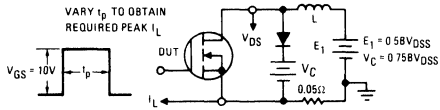


Fig. 16 – Clamped Inductive Waveforms

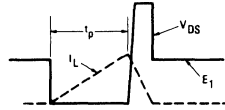


Fig. 17 – Switching Time Test Circuit

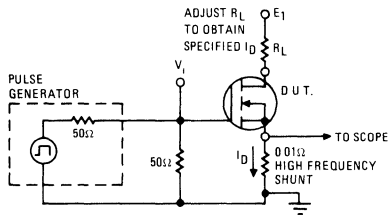
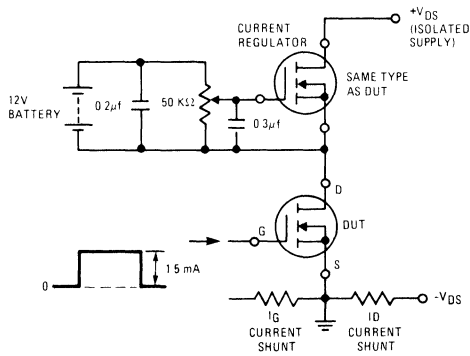


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm
N-Channel

UFN330
UFN331
UFN332
UFN333

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

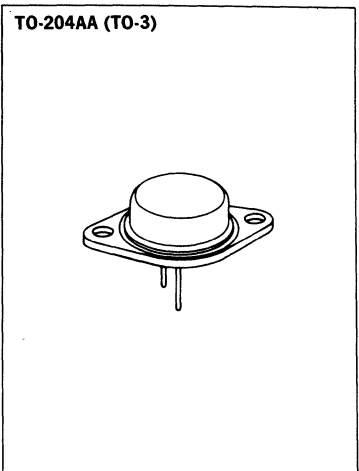
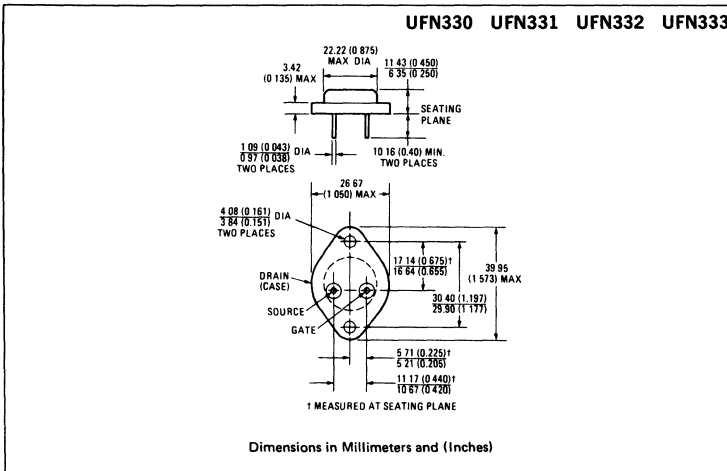
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN330	400V	1.0Ω	5.5A
UFN331	350V	1.0Ω	5.5A
UFN332	400V	1.5Ω	4.5A
UFN333	350V	1.5Ω	4.5A

MECHANICAL SPECIFICATIONS

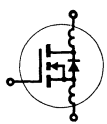


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN330	UFN331	UFN332	UFN333	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	5.5	5.5	4.5	4.5	A
I _D @ T _C = 100°C Continuous Drain Current	3.5	3.5	3.0	3.0	A
I _{DM} Pulsed Drain Current ③	22	22	18	18	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	75				W
Linear Derating Factor	0.6				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

4

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	UFN330 UFN332	400	—	—	V	V _{GS} = 0V I _D = 250μA
	UFN331 UFN333	350	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	UFN330 UFN331	5.5	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on) max.} , V _{GS} = 10V
	UFN332 UFN333	4.5	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN330 UFN331	—	0.8	1.0	Ω	V _{GS} = 10V, I _D = 3.0A
	UFN332 UFN333	—	1.0	1.5	Ω	
g _{fs} Forward Transconductance ②	ALL	3.0	4.0	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on) max.} , I _D = 3.0A
C _{iss} Input Capacitance	ALL	—	700	900	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	150	300	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	40	80	pF	V _{DD} = 175V, I _D = 3.0A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	
t _r Rise Time	ALL	—	—	35	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	—	55	ns	
t _f Fall Time	ALL	—	—	35	ns	V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	
Q _{gs} Gate-Source Charge	ALL	—	11	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN330	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN331	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN330	—	—	22	A	
		UFN331	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	UFN330	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 5.5\text{A}, V_{GS} = 0\text{V}$
		UFN331	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 4.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

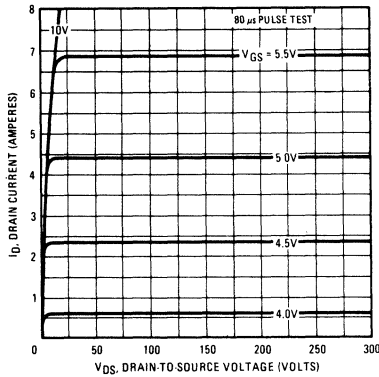


Fig. 2 – Typical Transfer Characteristics

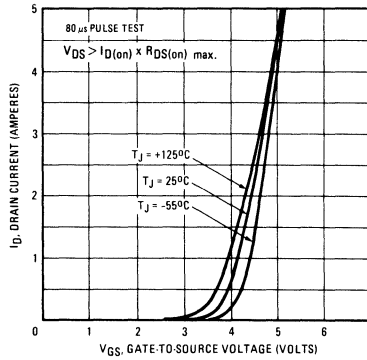


Fig. 3 – Typical Saturation Characteristics

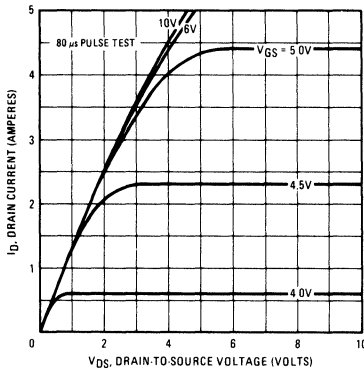


Fig. 4 – Maximum Safe Operating Area

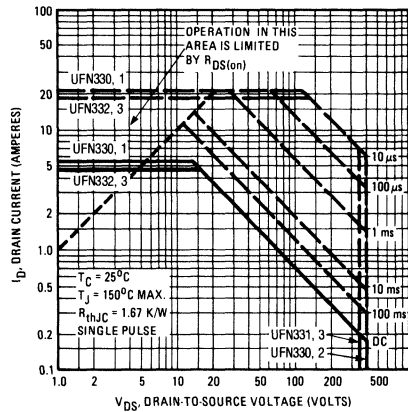


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

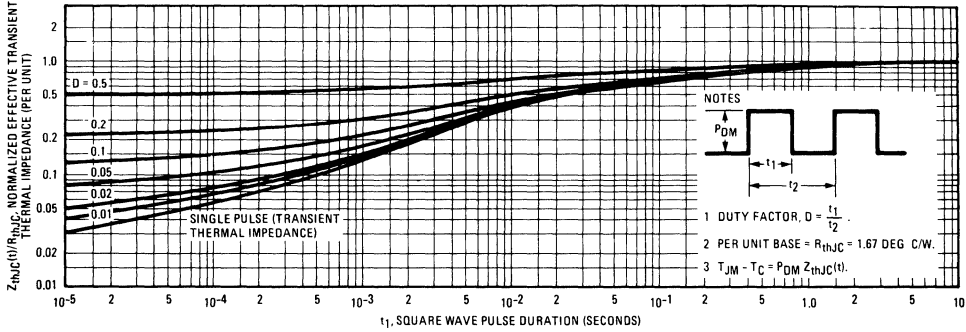


Fig. 6 – Typical Transconductance Vs. Drain Current

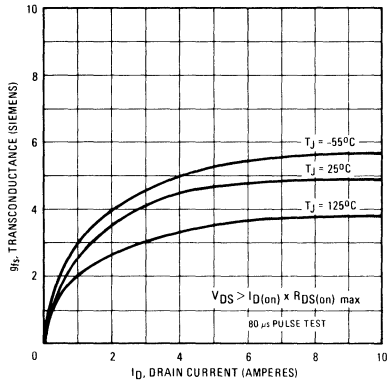


Fig. 7 – Typical Source-Drain Diode Forward Voltage

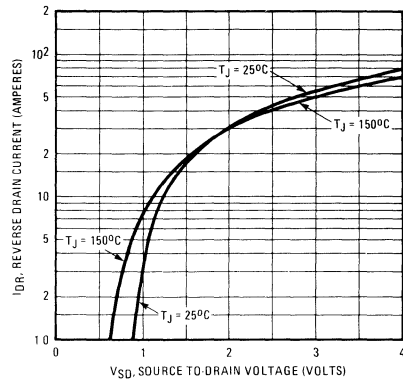


Fig. 8 – Breakdown Voltage Vs. Temperature

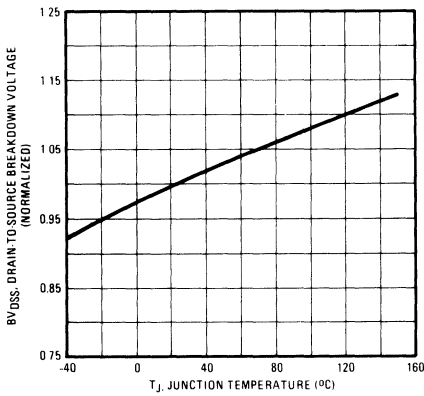


Fig. 9 – Normalized On-Resistance Vs. Temperature

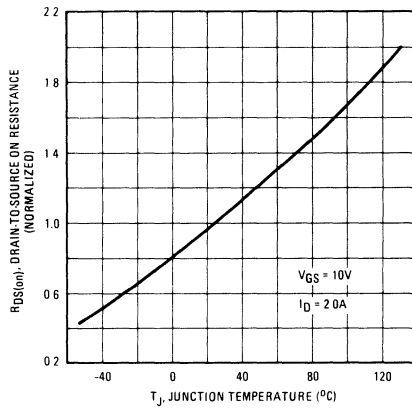


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

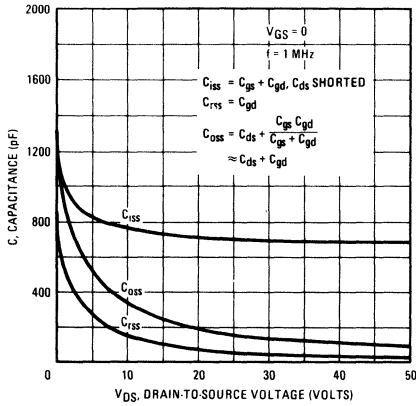


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

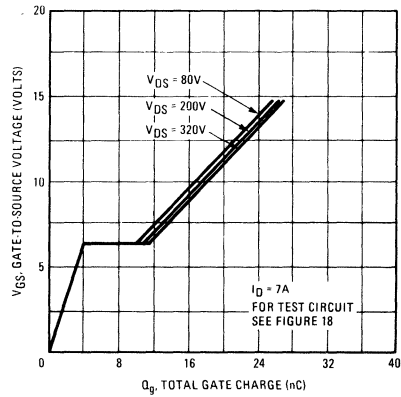


Fig. 12 – Typical On-Resistance Vs. Drain Current

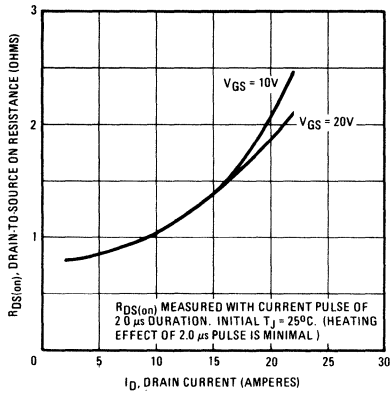


Fig. 13 – Maximum Drain Current Vs. Case Temperature

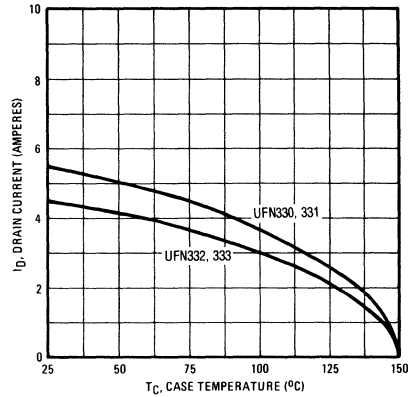


Fig. 14 – Power Vs. Temperature Derating Curve

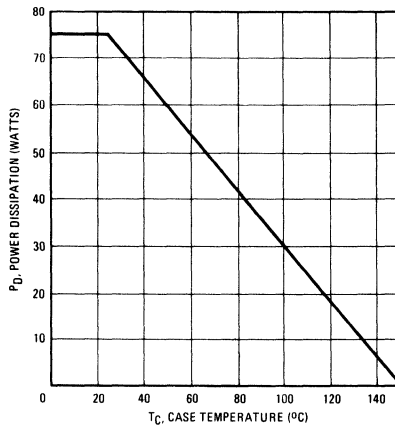


Fig. 15 — Clamped Inductive Test Circuit

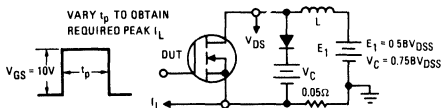


Fig. 16 — Clamped Inductive Waveforms



Fig. 17 — Switching Time Test Circuit

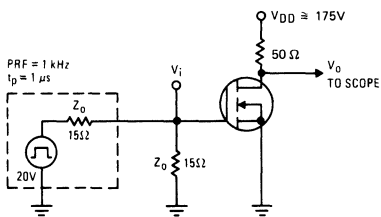
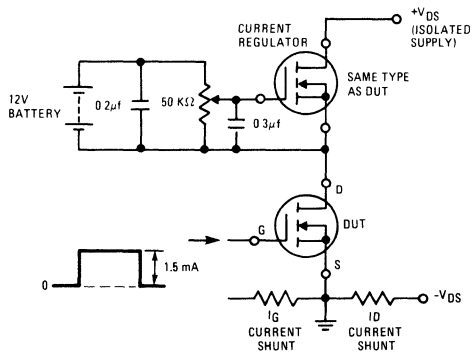


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 0.55 Ohm
N-Channel

UFN340
UFN341
UFN342
UFN343

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

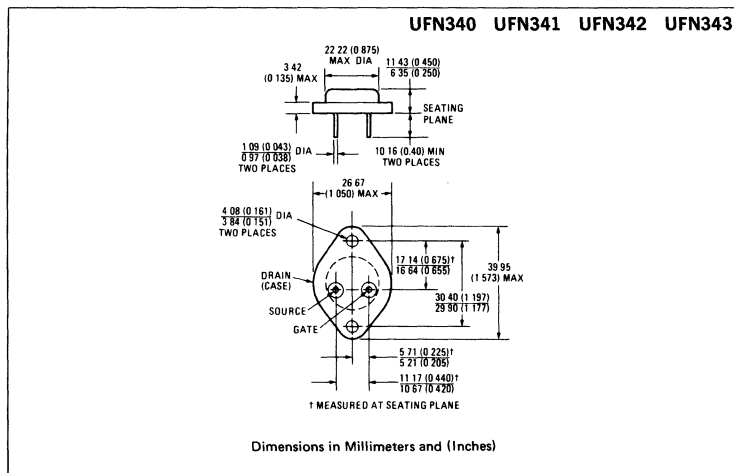
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

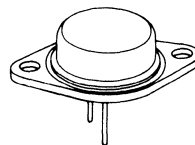
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN340	400V	0.55Ω	10A
UFN341	350V	0.55Ω	10A
UFN342	400V	0.80Ω	8.0A
UFN343	350V	0.80Ω	8.0A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)

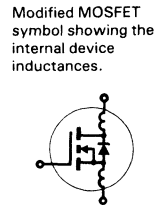


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN340	UFN341	UFN342	UFN343	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	10	10	8.0	8.0	A
I _D @ T _C = 100°C Continuous Drain Current	6.0	6.0	5.0	5.0	A
I _{DM} Pulsed Drain Current ③	40	40	32	32	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	40	40	32	32	
T _J T _{stg} Operating Junction and Storage Temperature Range	-55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	UFN340 UFN342	400	—	—	V	V _{GS} = 0V
	UFN341 UFN343	350	—	—	V	I _D = 250μA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	UFN340 UFN341	10	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V
	UFN342 UFN343	8.0	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN340 UFN341	—	0.47	0.55	Ω	V _{GS} = 10V, I _D = 5.0A
	UFN342 UFN343	—	0.68	0.80	Ω	
g _{fs} Forward Transconductance ②	ALL	4.0	7.0	—	S(Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 5.0A
C _{iSS} Input Capacitance	ALL	—	1250	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	300	450	pF	
C _{rSS} Reverse Transfer Capacitance	ALL	—	80	150	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	17	35	ns	V _{DD} = 175V, I _D = 5.0A, Z _o = 4.7Ω See Fig. 17
t _r Rise Time	ALL	—	5.0	15	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	45	90	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	—	16	35	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	V _{GS} = 10V, I _D = 12A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
	Q _{gs} Gate-Source Charge	ALL	—	18	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	23	—	nC	
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN340	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	
		UFN341	—	—	8.0	A		
I_{SM}	Pulse Source Current (Body Diode) ③	UFN340	—	—	40	A		
		UFN341	—	—	32	A		
V_{SD}	Diode Forward Voltage ②	UFN340	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 10\text{A}, V_{GS} = 0\text{V}$	
		UFN341	—	—	1.9	V		
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 10\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$	
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 10\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.					

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

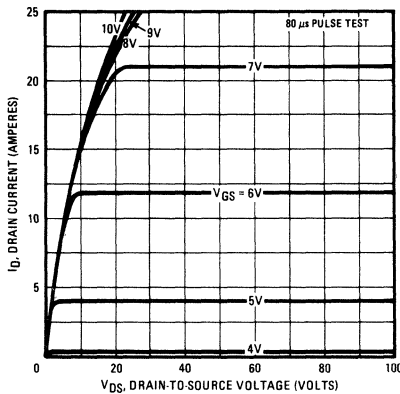


Fig. 2 – Typical Transfer Characteristics

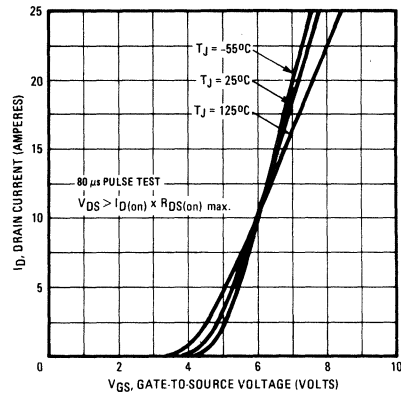


Fig. 3 – Typical Saturation Characteristics

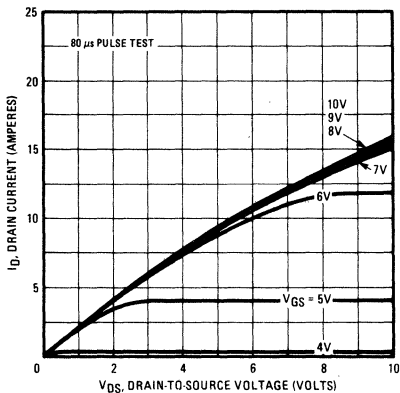


Fig. 4 – Maximum Safe Operating Area

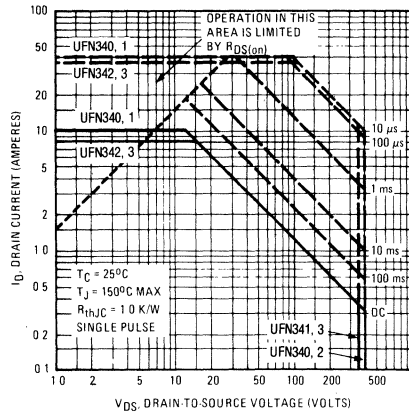
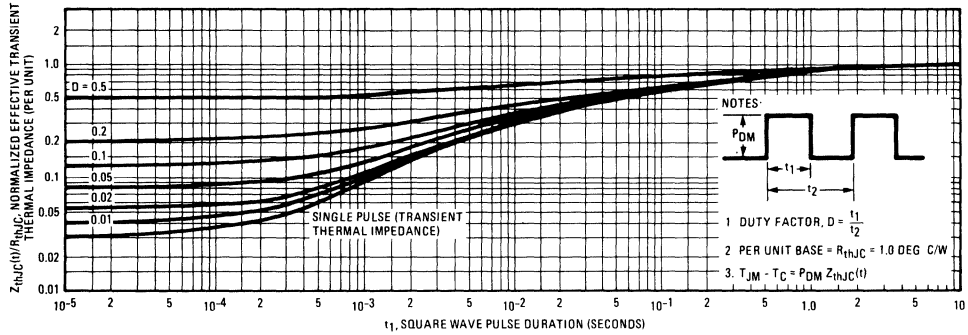


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

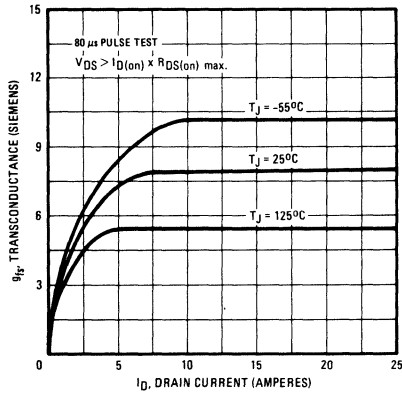


Fig. 7 – Typical Source-Drain Diode Forward Voltage

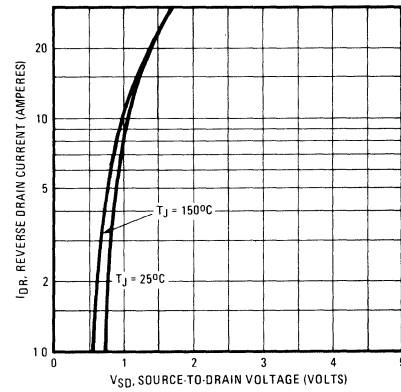


Fig. 8 – Breakdown Voltage Vs. Temperature

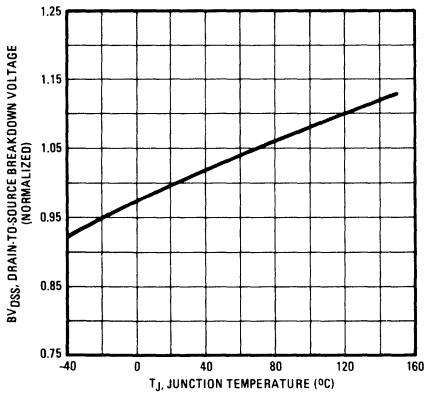


Fig. 9 – Normalized On-Resistance Vs. Temperature

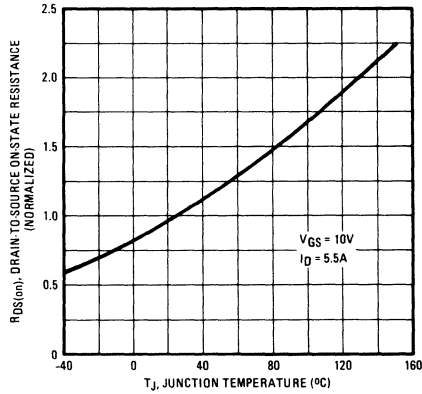


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

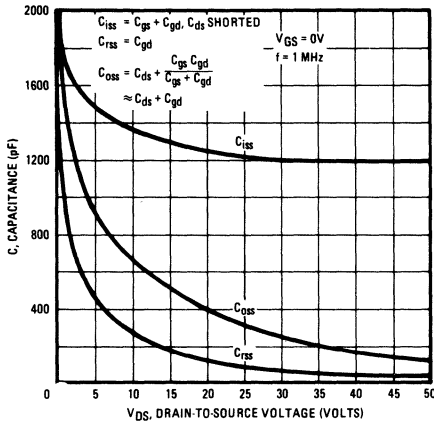


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

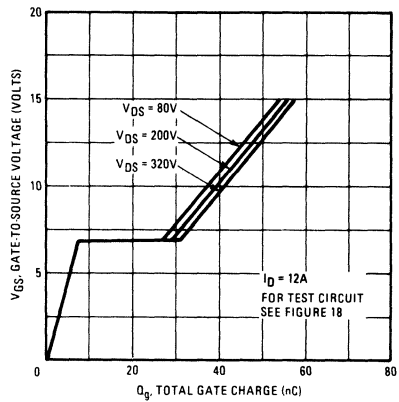


Fig. 12 – Typical On-Resistance Vs. Drain Current

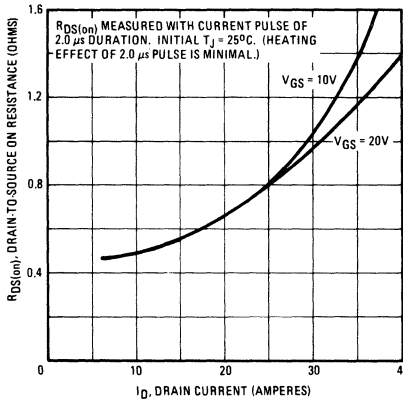


Fig. 13 – Maximum Drain Current Vs. Case Temperature

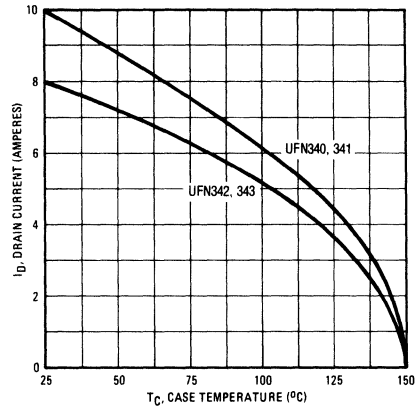


Fig. 14 – Power Vs. Temperature Derating Curve

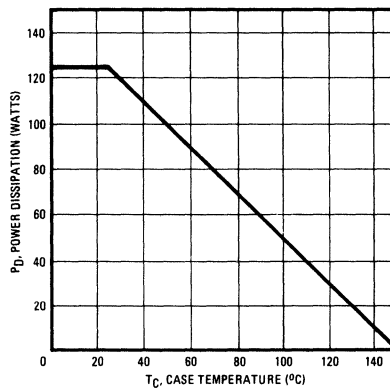


Fig. 15 — Clamped Inductive Test Circuit

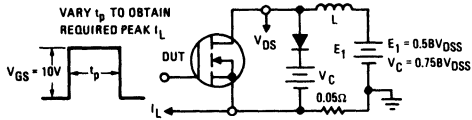


Fig. 16 — Clamped Inductive Waveforms

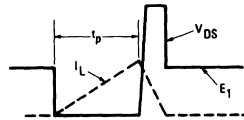


Fig. 17 — Switching Time Test Circuit

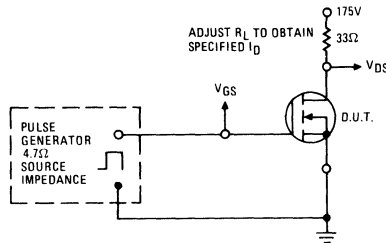
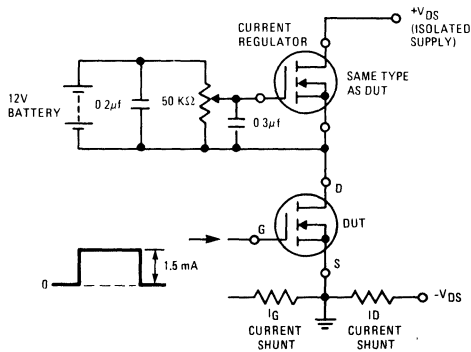


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 0.3 Ohm
N-Channel

UFN350
UFN351
UFN352
UFN353

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

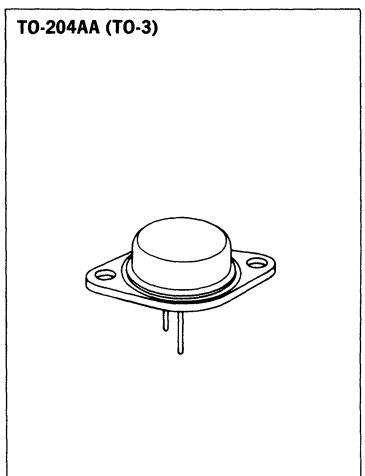
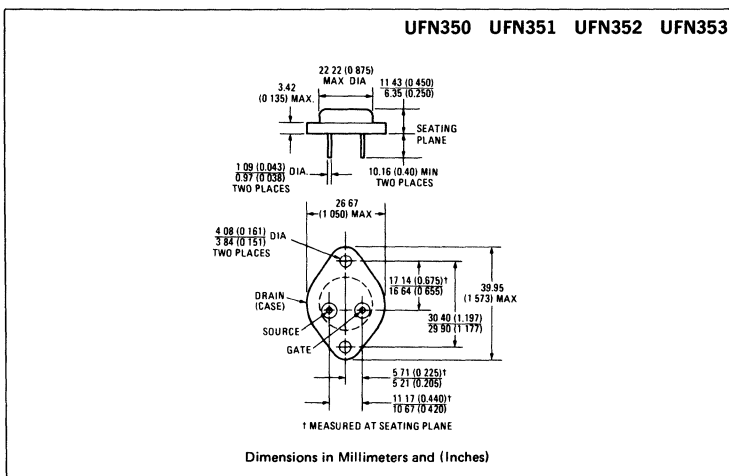
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN350	400V	0.3Ω	15A
UFN351	350V	0.3Ω	15A
UFN352	400V	0.4Ω	13A
UFN353	350V	0.4Ω	13A

MECHANICAL SPECIFICATIONS

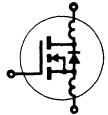


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN350	UFN351	UFN352	UFN353	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	15	15	13	13	A
I _D @ T _C = 100°C Continuous Drain Current	9.0	9.0	8.0	8.0	A
I _{DM} Pulsed Drain Current ③	60	60	52	52	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN350 UFN352	400	—	—	V	V _{GS} = 0V	
	UFN351 UFN353	350	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} ; I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN350 UFN351	15	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max.; V _{GS} = 10V	
	UFN352 UFN353	13	—	—	A		
	—	—	—	—	—		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN350 UFN351	—	0.25	0.3	Ω	V _{GS} = 10V, I _D = 8.0A	
	UFN352 UFN353	—	0.3	0.4	Ω		
	—	—	—	—	—		
g _{fs} Forward Transconductance ②	ALL	8.0	10	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max.; I _D = 8.0A	
C _{iss} Input Capacitance	ALL	—	2000	3000	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	400	600	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	100	200	pF	V _{DD} = 180V, I _D = 8.0A, Z ₀ = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _{d(on)} Turn-On Delay Time	ALL	—	—	35	ns		
t _r Rise Time	ALL	—	—	65	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	150	ns		
t _f Fall Time	ALL	—	—	75	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	38	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	41	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	0.83	K/W	
R _{thCS} Case-to-Sink	ALL	—	—	0.1	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN350	—	—	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN351	—	—	15	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN350	—	—	60	A	
		UFN351	—	—	60	A	
V_{SD}	Diode Forward Voltage ②	UFN350	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 15\text{A}, V_{GS} = 0\text{V}$
		UFN351	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 15\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	UFN350	—	—	1000	ns	$T_J = 150^\circ\text{C}, I_F = 15\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
		UFN351	—	—	1000	ns	
Q_{RR}	Reverse Recovered Charge	ALL	—	6.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 15\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

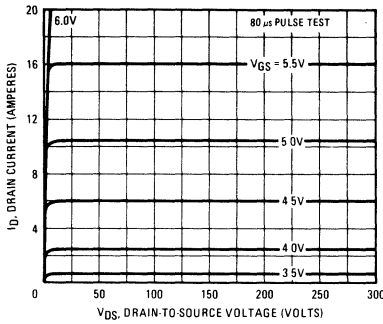


Fig. 3 – Typical Saturation Characteristics

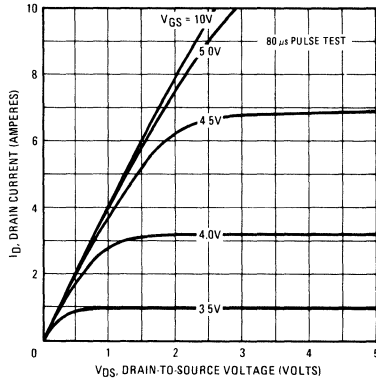


Fig. 2 – Typical Transfer Characteristics

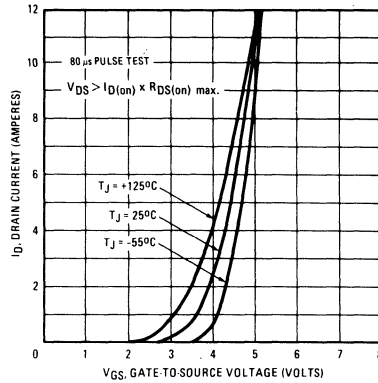


Fig. 4 – Maximum Safe Operating Area

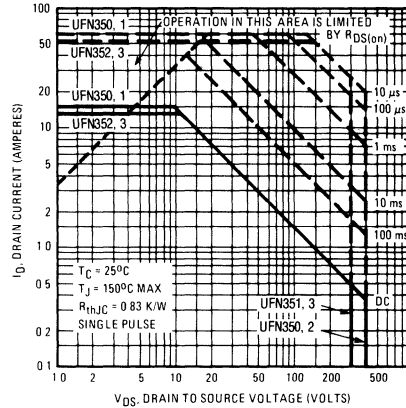
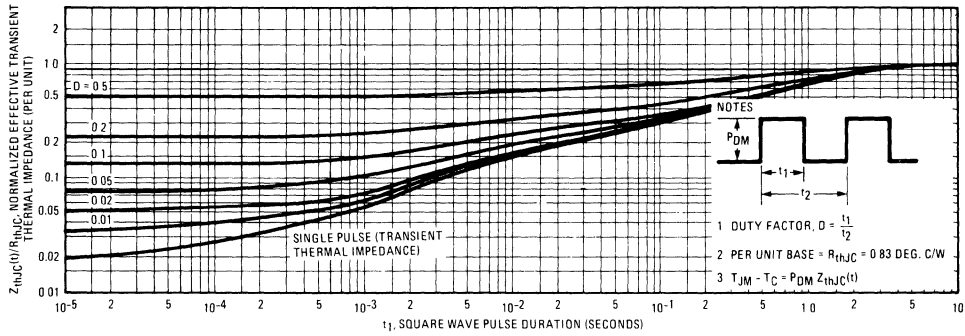


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



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Fig. 6 – Typical Transconductance Vs. Drain Current

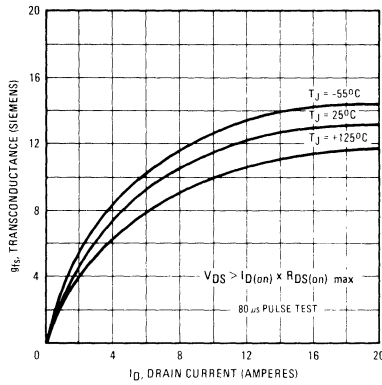


Fig. 7 – Typical Source-Drain Diode Forward Voltage

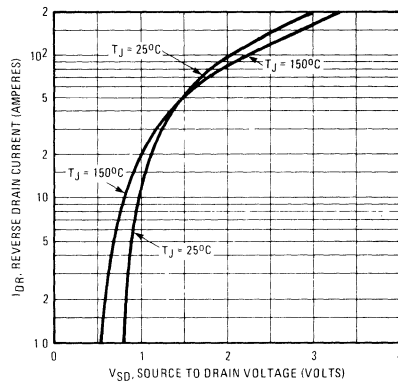


Fig. 8 – Breakdown Voltage Vs. Temperature

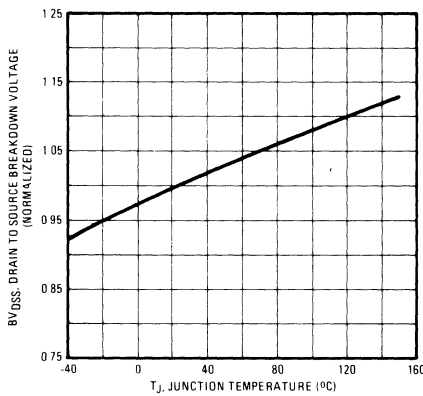


Fig. 9 – Normalized On-Resistance Vs. Temperature

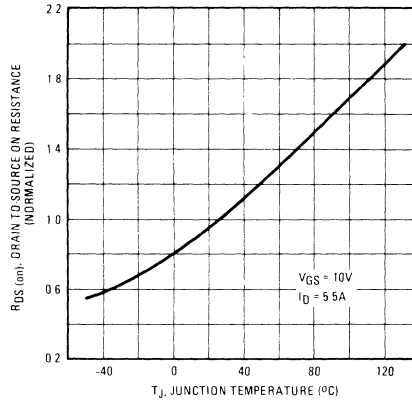


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

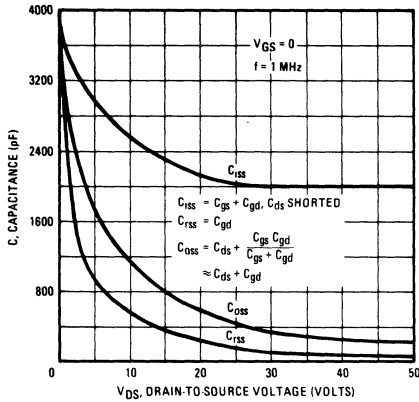


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

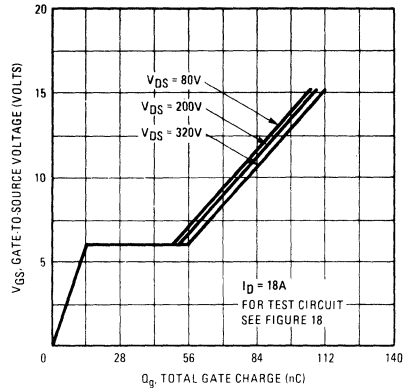


Fig. 12 — Typical On-Resistance Vs. Drain Current

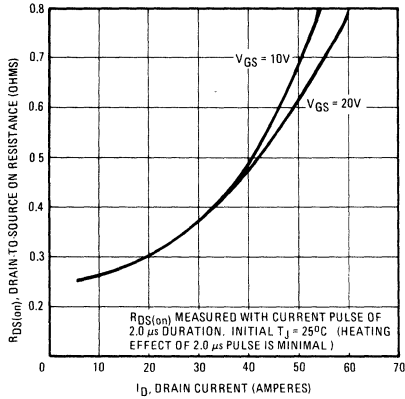


Fig. 13 — Maximum Drain Current Vs. Case Temperature

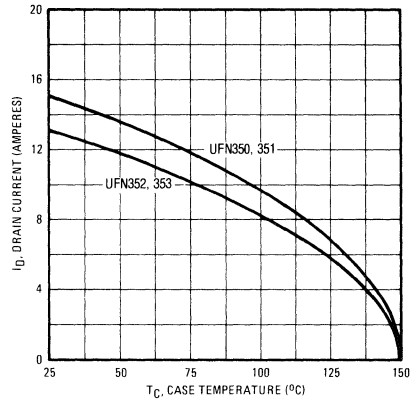


Fig. 14 — Power Vs. Temperature Derating Curve

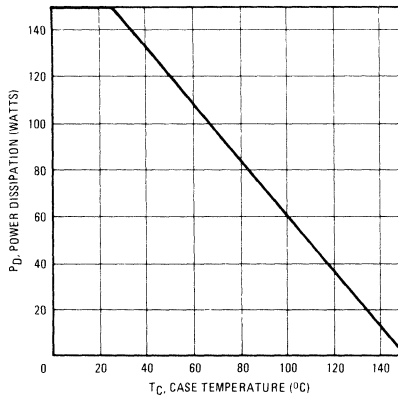


Fig. 15 — Clamped Inductive Test Circuit

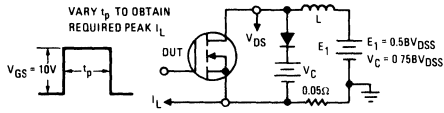
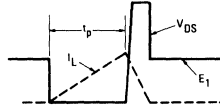


Fig. 16 — Clamped Inductive Waveforms



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Fig. 17 — Switching Time Test Circuit

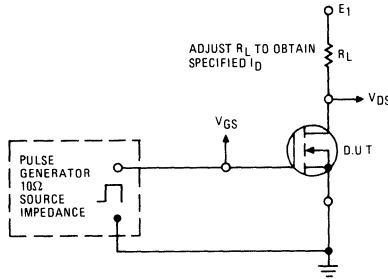
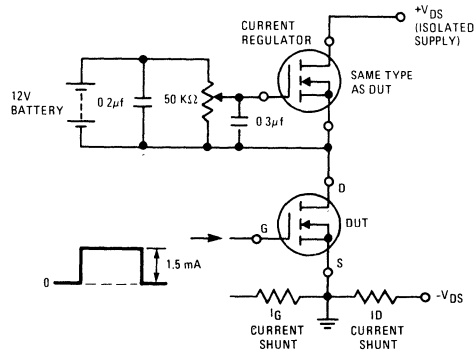


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 3.0 Ohm
N-Channel

UFN420
UFN421
UFN422
UFN423

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

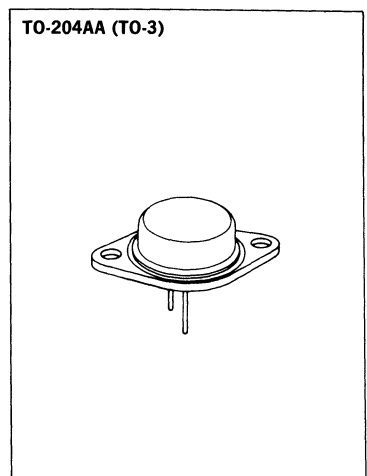
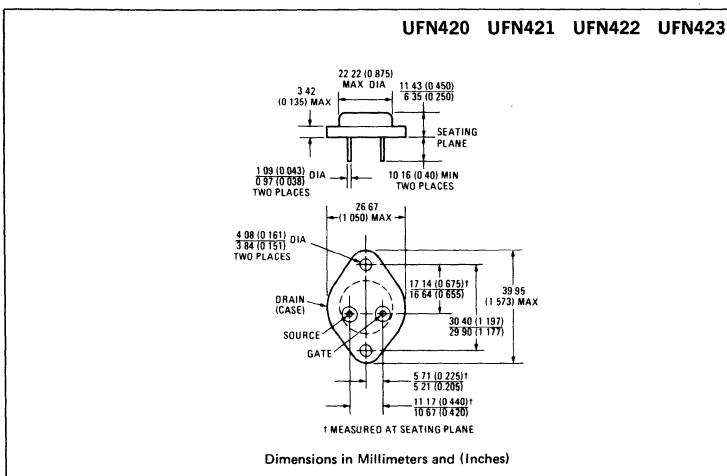
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN420	500V	3.0Ω	2.5A
UFN421	450V	3.0Ω	2.5A
UFN422	500V	4.0Ω	2.0A
UFN423	450V	4.0Ω	2.0A

MECHANICAL SPECIFICATIONS

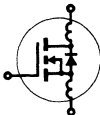


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN420	UFN421	UFN422	UFN423	Units
V _{DS} Drain - Source Voltage ①	500	450	500	450	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	500	450	500	450	V
I _D @ T _C = 25°C Continuous Drain Current	2.5	2.5	2.0	2.0	A
I _D @ T _C = 100°C Continuous Drain Current	1.5	1.5	1.0	1.0	A
I _{DM} Pulsed Drain Current ③	10	10	8.0	8.0	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	10	10	8.0	8.0	
T _J T _{stg} Operating Junction and Storage Temperature Range	-55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

4


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN420 UFN422	500	—	—	V	V _{GS} = 0V	
	UFN421 UFN423	450	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN420 UFN421	2.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN422 UFN423	2.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN420 UFN421	—	2.5	3.0	Ω	V _{GS} = 10V, I _D = 1.0A	
	UFN422 UFN423	—	3.0	4.0	Ω		
g _{fs} Forward Transconductance ②	ALL	1.0	1.75	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 1.0A	
C _{iss} Input Capacitance	ALL	—	300	400	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	75	150	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	20	40	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	30	60	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 1.0A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	25	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	30	60	ns		
t _f Fall Time	ALL	—	15	30	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC		V _{GS} = 10V, I _D = 3.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	5.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN420	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN421	—	—	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN420	—	—	10	A	
		UFN421	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	UFN420	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
		UFN421	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	—	—	—	—	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

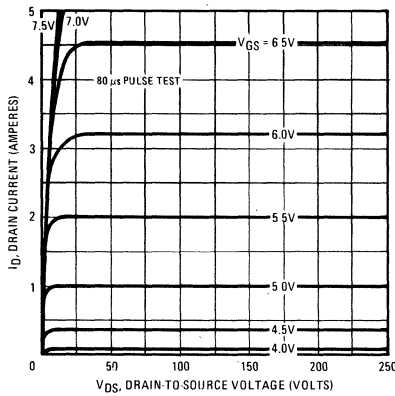


Fig. 2 – Typical Transfer Characteristics

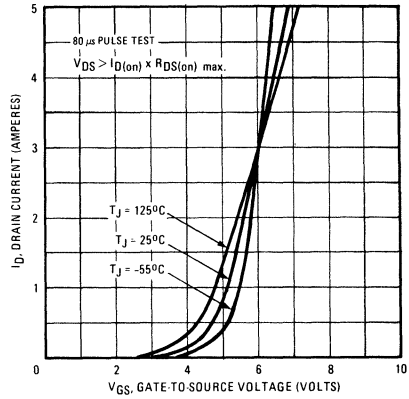


Fig. 3 – Typical Saturation Characteristics

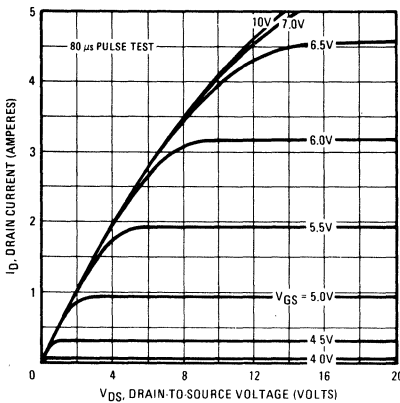


Fig. 4 – Maximum Safe Operating Area

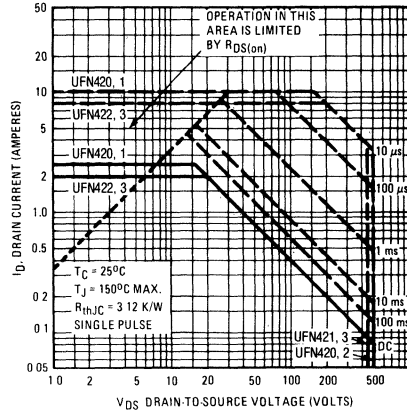


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

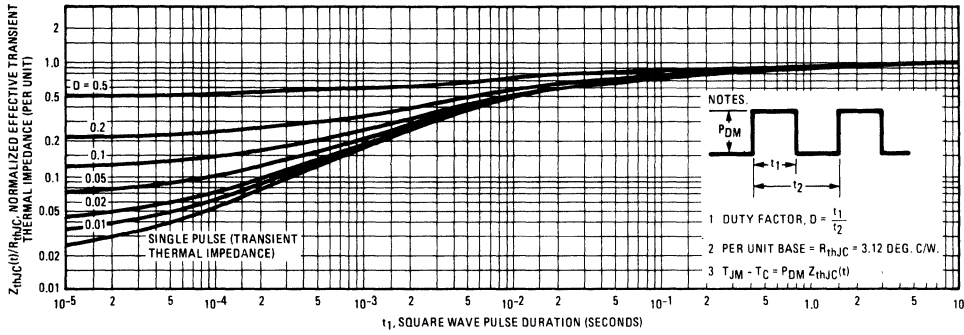


Fig. 6 — Typical Transconductance Vs. Drain Current

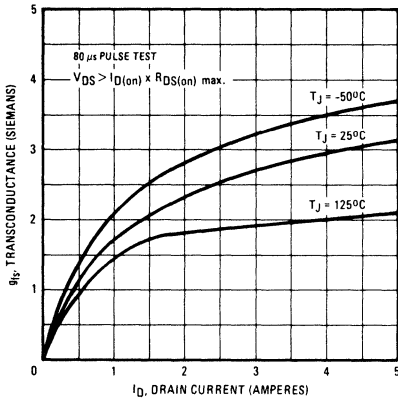


Fig. 7 — Typical Source-Drain Diode Forward Voltage

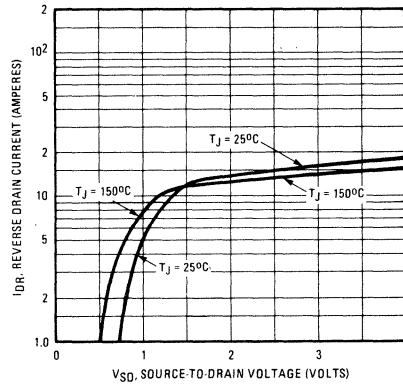


Fig. 8 — Breakdown Voltage Vs. Temperature

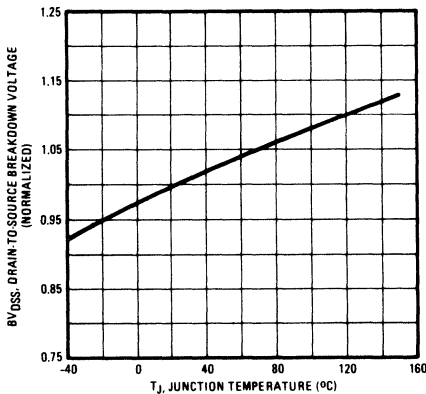


Fig. 9 — Normalized On-Resistance Vs. Temperature

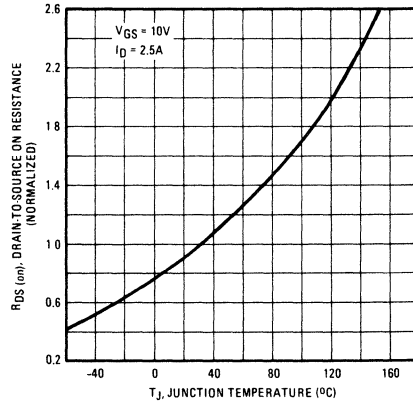


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

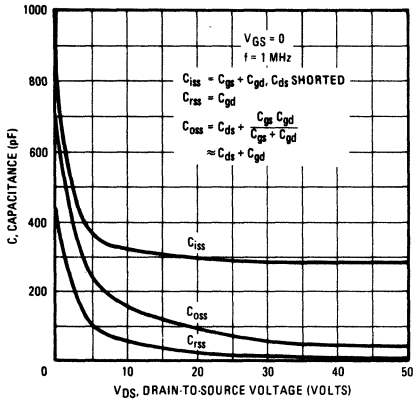


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

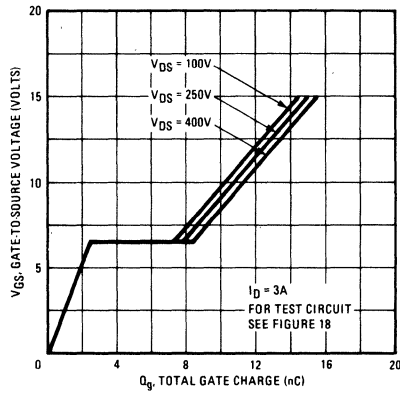


Fig. 12 – Typical On-Resistance Vs. Drain Current

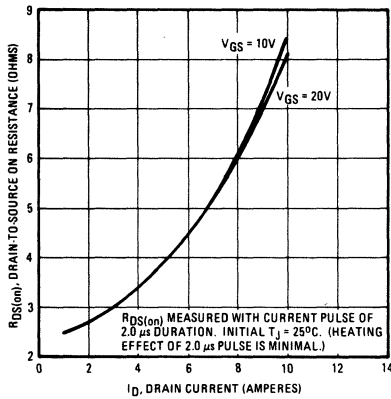


Fig. 13 – Maximum Drain Current Vs. Case Temperature

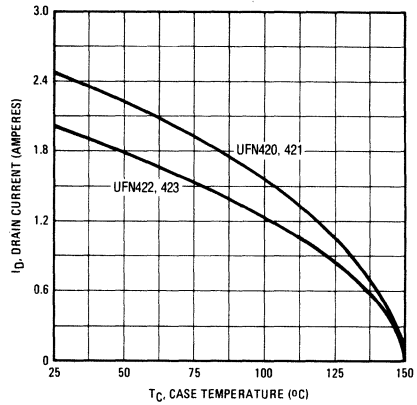


Fig. 14 – Power Vs. Temperature Derating Curve

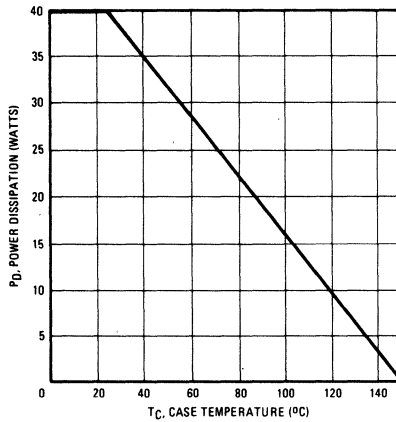


Fig. 15 — Clamped Inductive Test Circuit

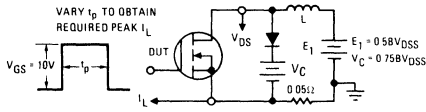


Fig. 16 — Clamped Inductive Waveforms

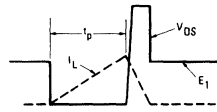


Fig. 17 — Switching Time Test Circuit

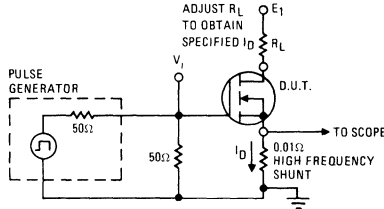
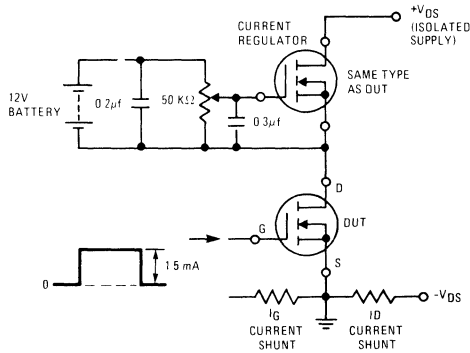


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

UFN430
UFN431
UFN432
UFN433

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

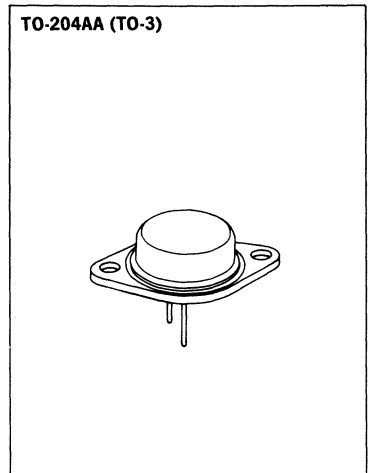
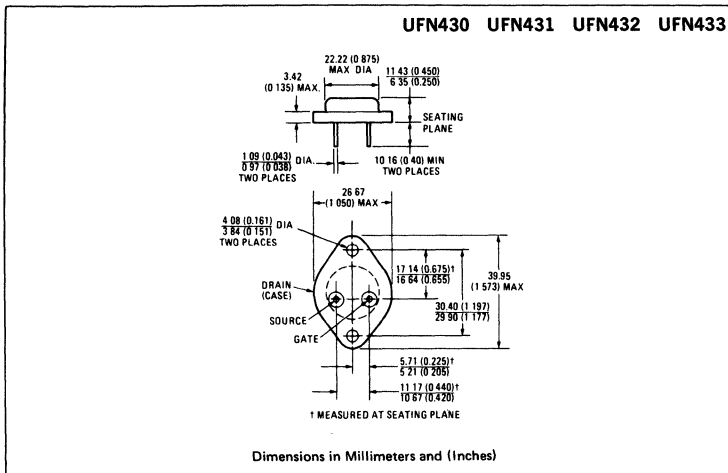
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN430	500V	1.5Ω	4.5A
UFN431	450V	1.5Ω	4.5A
UFN432	500V	2.0Ω	4.0A
UFN433	450V	2.0Ω	4.0A

MECHANICAL SPECIFICATIONS

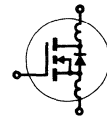


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN430	UFN431	UFN432	UFN433	Units
V_{DS} Drain - Source Voltage ①	500	450	500	450	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	4.5	4.5	4.0	4.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM} Pulsed Drain Current ③	18	18	16	16	A
V_{GS} Gate - Source Voltage					± 20
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation					75 (See Fig. 14)
Linear Derating Factor					0.6 (See Fig. 14)
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range					-55 to 150
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN430 UFN432	500	—	—	V	$V_{GS} = 0\text{V}$	
	UFN431 UFN433	450	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN430 UFN431	4.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFN432 UFN433	4.0	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN430 UFN431	—	1.3	1.5	Ω	$V_{GS} = 10\text{V}$, $I_D = 2.5\text{A}$	
	UFN432 UFN433	—	1.5	2.0	Ω		
g_{fs} Forward Transconductance ②	ALL	2.5	3.2	—	S (③)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 2.5\text{A}$	
C_{iss} Input Capacitance	ALL	—	600	800	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$	
C_{oss} Output Capacitance	ALL	—	100	200	pF	See Fig. 10	
C_{rss} Reverse Transfer Capacitance	ALL	—	30	60	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} = 225\text{V}$, $I_D = 2.5\text{A}$, $Z_0 = 15\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	—	30	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	55	ns		
t_f Fall Time	ALL	—	—	30	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	30	nC	$V_{GS} = 10\text{V}$, $I_D = 6.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	11	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	11	—	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN430	—	—	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN431	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN430	—	—	18	A	
		UFN431	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	UFN430	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 4.5\text{A}, V_{GS} = 0\text{V}$
		UFN431	—	—	1.3	V	$T_C = 25^\circ\text{C}, I_S = 4.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 4.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 4.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

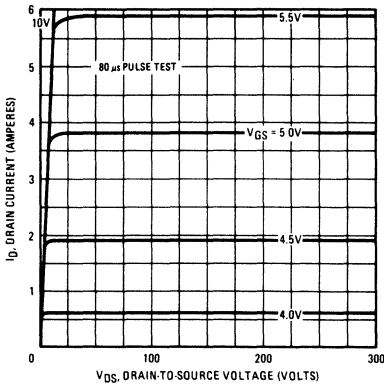


Fig. 2 – Typical Transfer Characteristics

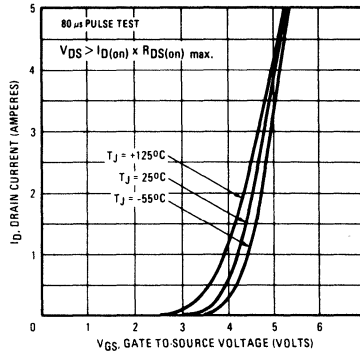


Fig. 3 – Typical Saturation Characteristics

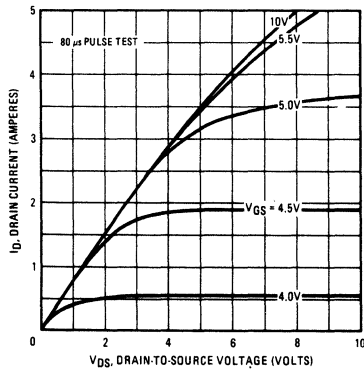


Fig. 4 – Maximum Safe Operating Area

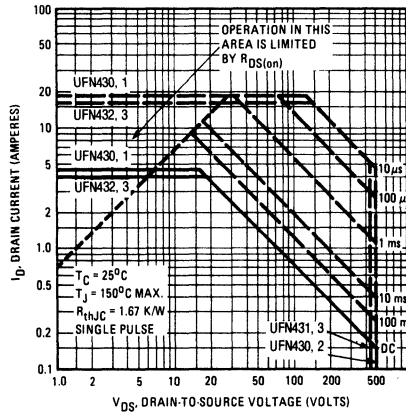
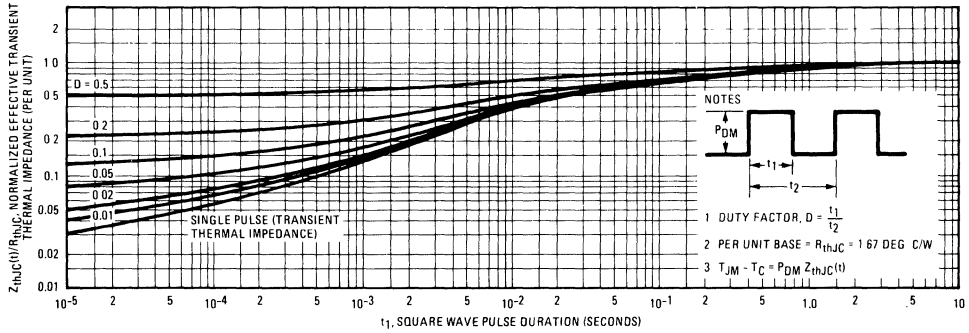


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

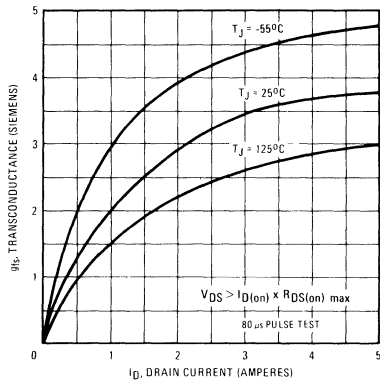


Fig. 7 – Typical Source-Drain Diode Forward Voltage

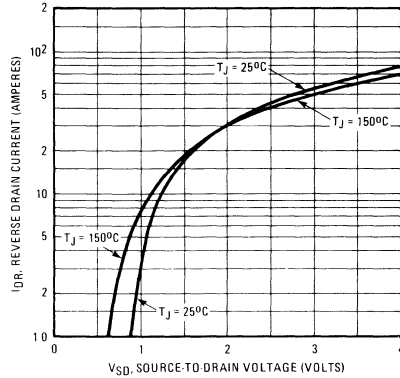


Fig. 8 – Breakdown Voltage Vs. Temperature

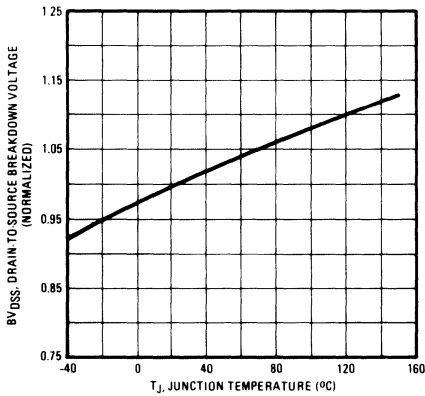


Fig. 9 – Normalized On-Resistance Vs. Temperature

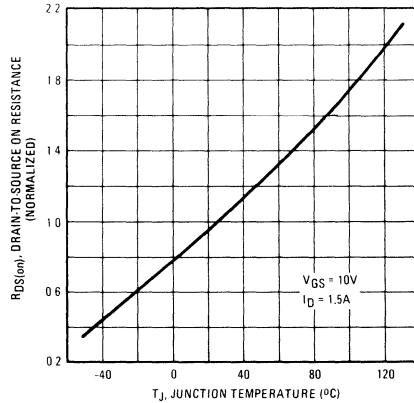


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

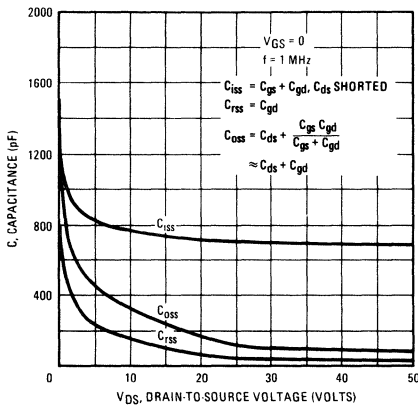


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

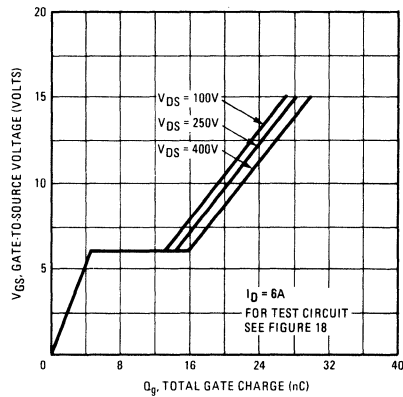


Fig. 12 – Typical On-Resistance Vs. Drain Current

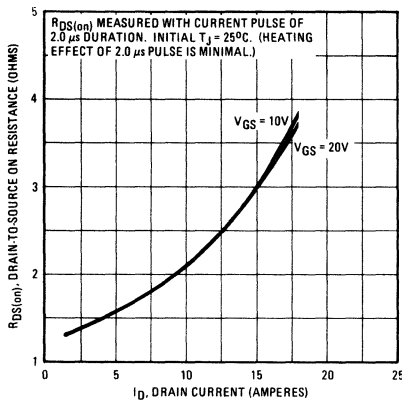


Fig. 13 – Maximum Drain Current Vs. Case Temperature

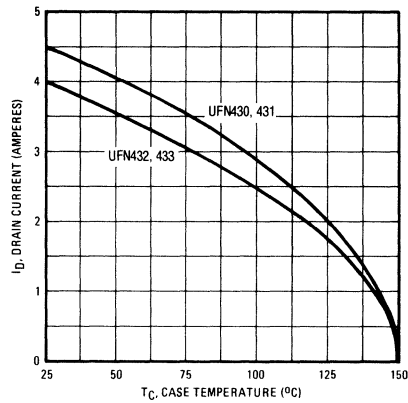


Fig. 14 – Power Vs. Temperature Derating Curve

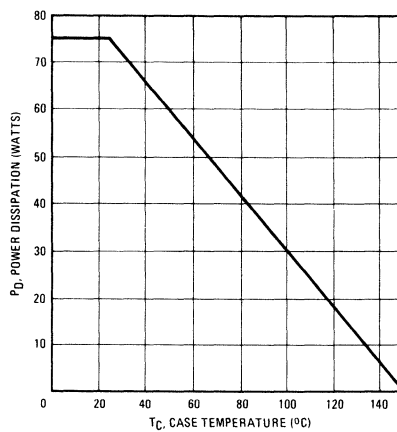


Fig. 15 – Clamped Inductive Test Circuit

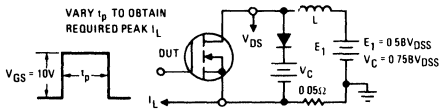


Fig. 16 – Clamped Inductive Waveforms

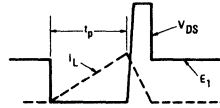


Fig. 17 – Switching Time Test Circuit

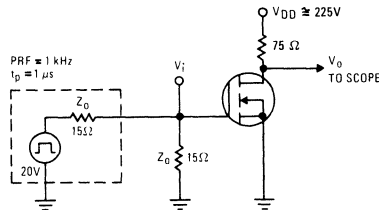
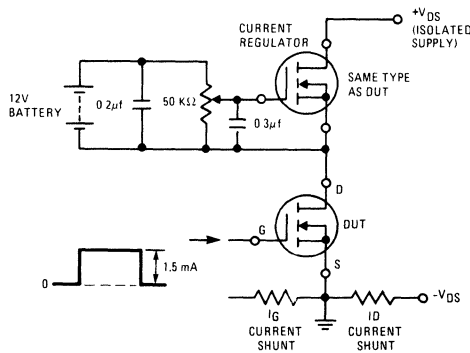


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 0.85 Ohm
N-Channel

UFN440
UFN441
UFN442
UFN443

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

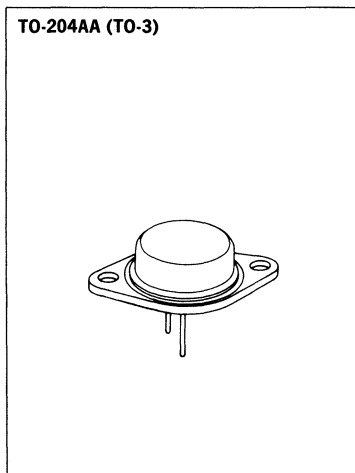
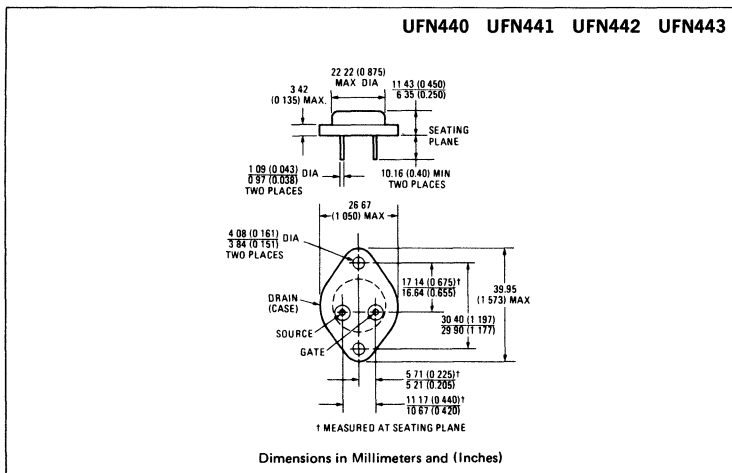
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN440	500V	0.85Ω	8.0A
UFN441	450V	0.85Ω	8.0A
UFN442	500V	1.10Ω	7.0A
UFN443	450V	1.10Ω	7.0A

MECHANICAL SPECIFICATIONS

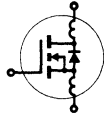


ABSOLUTE MAXIMUM RATINGS

Parameter		UFN440	UFN441	UFN442	UFN443	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$	Max. Power Dissipation	125			(See Fig. 14)	W
	Linear Derating Factor	1.0			(See Fig. 14)	W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4


ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} : Drain - Source Breakdown Voltage	UFN440 UFN442	500	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	UFN441 UFN443	450	—	—	V		
$V_{GS(th)}$: Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} : Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} : Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} : Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$ $V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
		—	—	1000	μA		
$I_{D(on)}$: On-State Drain Current ②	UFN440 UFN441	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFN442 UFN443	7.0	—	—	A		
$R_{DS(on)}$: Static Drain-Source On-State Resistance ②	UFN440 UFN441	—	0.8	0.85	Ω	$V_{GS} = 10\text{V}$, $I_D = 4.0\text{A}$	
	UFN442 UFN443	—	1.0	1.1	Ω		
g_{fs} : Forward Transconductance ②	ALL	4.0	6.5	—	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 4.0\text{A}$	
C_{iss} : Input Capacitance	ALL	—	1225	1600	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} : Output Capacitance	ALL	—	200	350	pF		
C_{rss} : Reverse Transfer Capacitance	ALL	—	85	150	pF		
$t_{d(on)}$: Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} = 200\text{V}$, $I_D = 4.0\text{A}$, $Z_\theta = 4.7\Omega$ See Fig. 17	
t_r : Rise Time	ALL	—	5	15	ns		
$t_{d(off)}$: Turn-Off Delay Time	ALL	—	42	90	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t_f : Fall Time	ALL	—	14	30	ns		
Q_g : Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} : Gate-Source Charge	ALL	—	20	—	nC		
Q_{gd} : Gate-Drain ("Miller") Charge	ALL	—	22	—	nC		
L_D : Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S : Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

Parameter		ALL	—	—	1.0	K/W	
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I _S	Continuous Source Current (Body Diode)	UFN440	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN441	—	—	7.0	A	
		UFN442 UFN443	—	—	7.0	A	
I _{SM}	Pulse Source Current (Body Diode) ③	UFN440	—	—	32	A	
		UFN441	—	—	32	A	
		UFN442 UFN443	—	—	28	A	
V _{SD}	Diode Forward Voltage ②	UFN440 UFN441	—	—	2.0	V	T _C = 25°C, I _S = 8.0A, V _{GS} = 0V
		UFN442 UFN443	—	—	1.9	V	T _C = 25°C, I _S = 7.0A, V _{GS} = 0V
t _{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	T _J = 150°C, I _F = 8.0A, dI _F /dt = 100A/μs
Q _{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	T _J = 150°C, I _F = 8.0A, dI _F /dt = 100A/μs
t _{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

- ① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

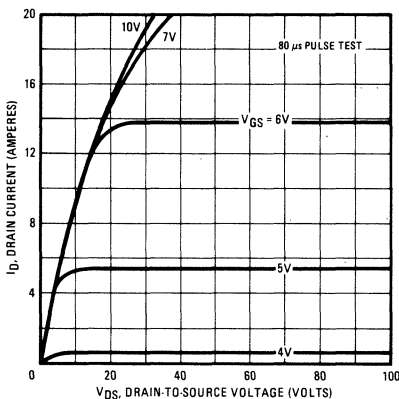


Fig. 2 – Typical Transfer Characteristics

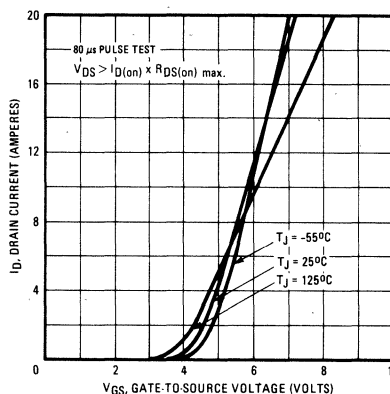


Fig. 3 – Typical Saturation Characteristics

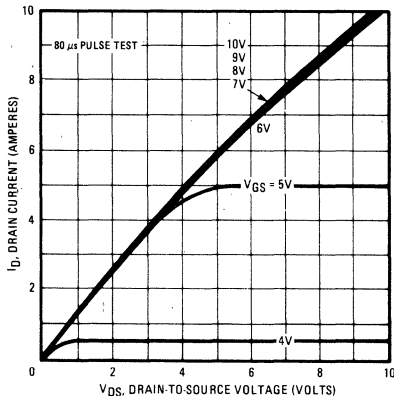


Fig. 4 – Maximum Safe Operating Area

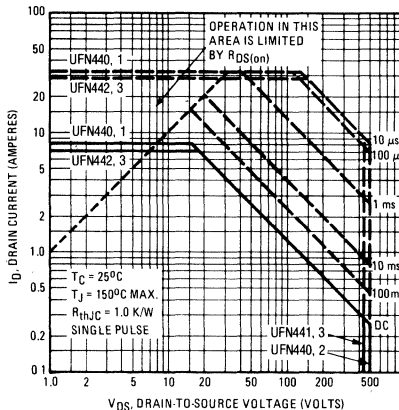


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

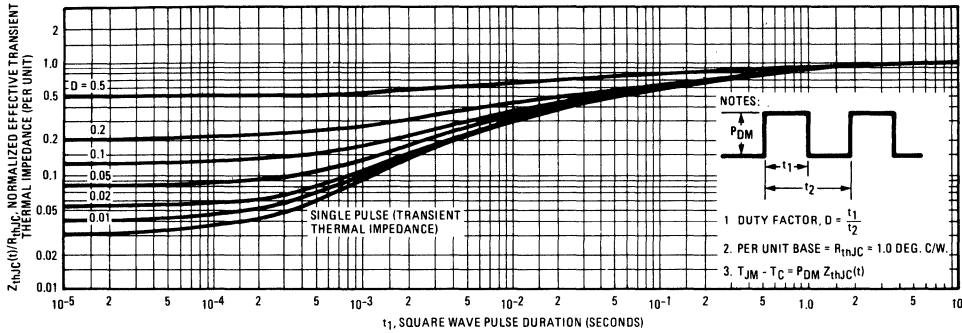


Fig. 6 – Typical Transconductance Vs. Drain Current

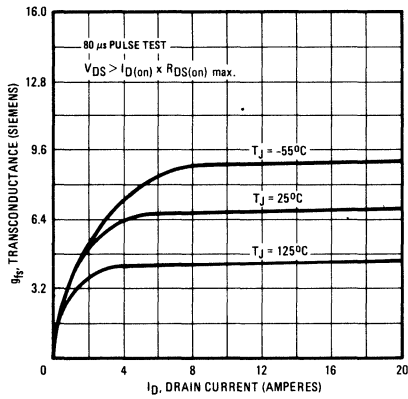


Fig. 7 – Typical Source-Drain Diode Forward Voltage

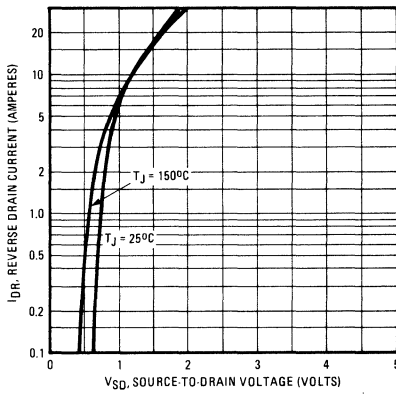


Fig. 8 – Breakdown Voltage Vs. Temperature

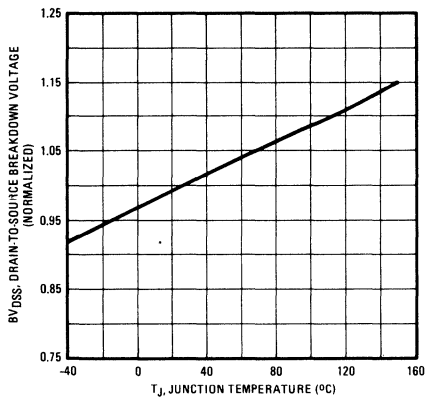


Fig. 9 – Normalized On-Resistance Vs. Temperature

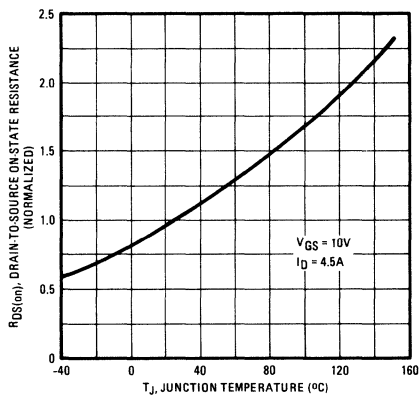


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

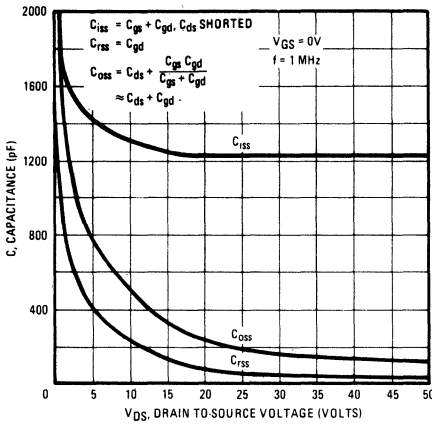


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

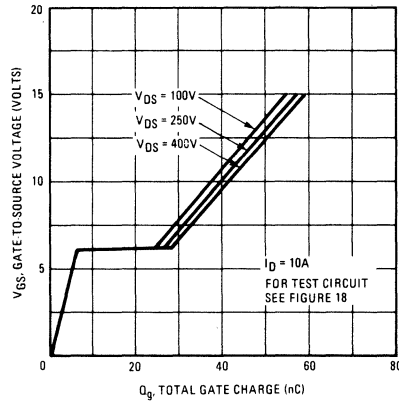


Fig. 12 – Typical On-Resistance Vs. Drain Current

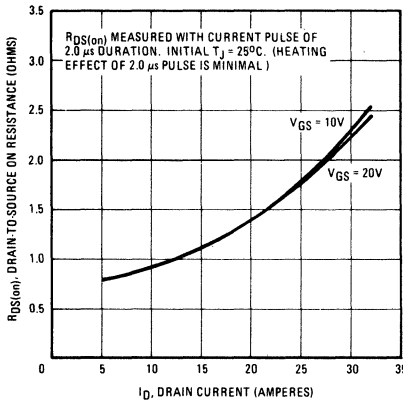


Fig. 13 – Maximum Drain Current Vs. Case Temperature

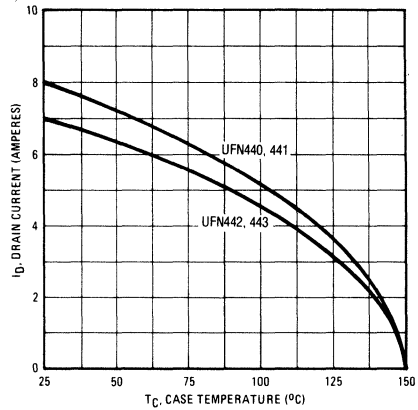


Fig. 14 – Power Vs. Temperature Derating Curve

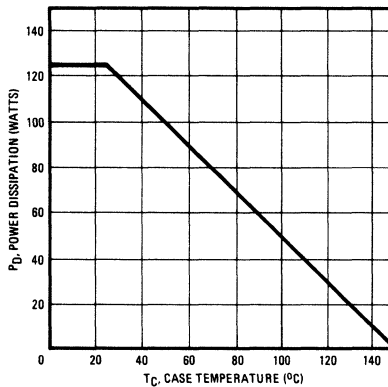


Fig. 15 — Clamped Inductive Test Circuit

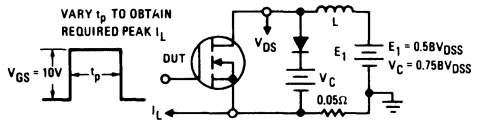


Fig. 16 — Clamped Inductive Waveforms

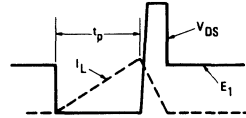


Fig. 17 — Switching Time Test Circuit

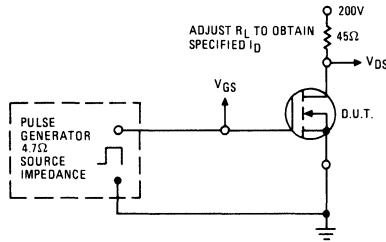
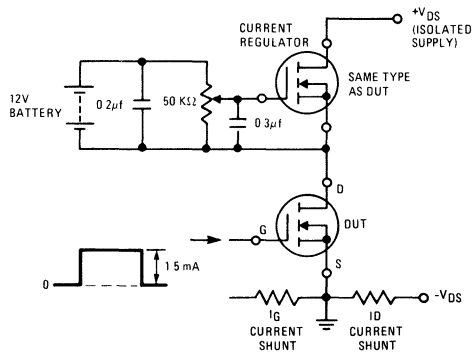


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 0.4 Ohm
N-Channel

UFN450
UFN451
UFN452
UFN453

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

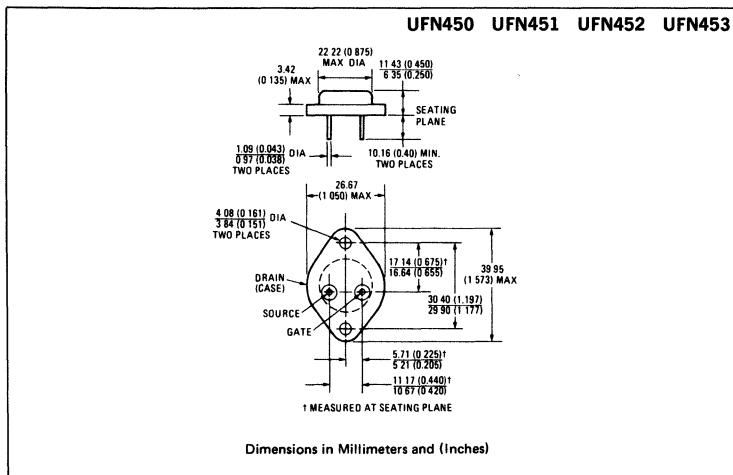
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

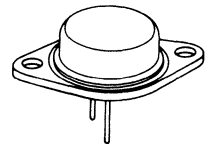
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN450	500V	0.4Ω	13A
UFN451	450V	0.4Ω	13A
UFN452	500V	0.5Ω	12A
UFN453	450V	0.5Ω	12A

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)

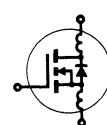


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN450	UFN451	UFN452	UFN453	Units
V _{DS} Drain - Source Voltage ①	500	450	500	450	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	500	450	500	450	V
I _D @ T _C = 25°C Continuous Drain Current	13	13	12	12	A
I _D @ T _C = 100°C Continuous Drain Current	8.0	8.0	7.0	7.0	A
I _{DM} Pulsed Drain Current ③	52	52	48	48	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C



ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN450 UFN452	500	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN451 UFN453	450	—	—	V		
	ALL	—	—	—	—		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN450 UFN451	13	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN452 UFN453	12	—	—	A		
	ALL	—	—	—	—		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN450 UFN451	—	0.3	0.4	Ω	V _{GS} = 10V, I _D = 7.0A	
	UFN452 UFN453	—	0.4	0.5	Ω		
	ALL	—	—	—	—		
g _{fs} Forward Transconductance ②	ALL	6.0	11	—	S(t)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 7.0A	
C _{iss} Input Capacitance	ALL	—	2000	3000	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	400	600	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	100	200	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	35	ns	V _{DD} = 210V, I _D = 7.0A, Z _O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	—	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	150	ns		
t _f Fall Time	ALL	—	—	70	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	120	nC	V _{GS} = 10V, I _D = 16A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	40	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	42	—	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	.83	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN450	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN451	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN450	—	—	52	A	
		UFN451	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN450	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 13\text{A}, V_{GS} = 0\text{V}$
		UFN451	—	—	1.3	V	$T_C = 25^\circ\text{C}, I_S = 12\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	1300	—	ns	$T_J = 150^\circ\text{C}, I_F = 13\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	7.4	—	μC	$T_J = 150^\circ\text{C}, I_F = 13\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

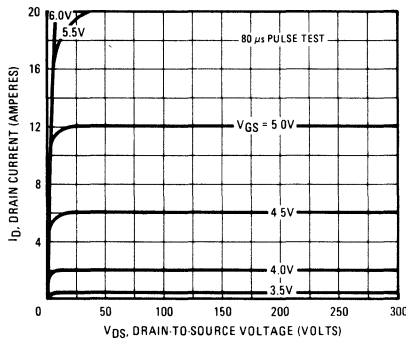


Fig. 3 – Typical Saturation Characteristics

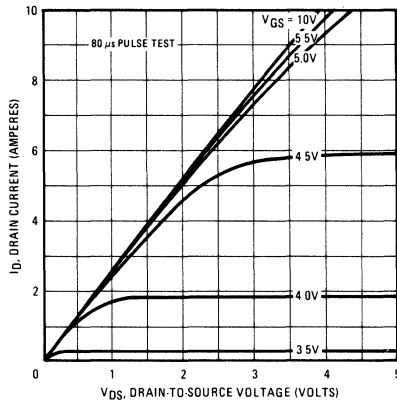


Fig. 2 – Typical Transfer Characteristics

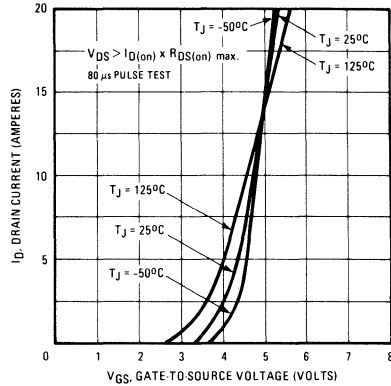


Fig. 4 – Maximum Safe Operating Area

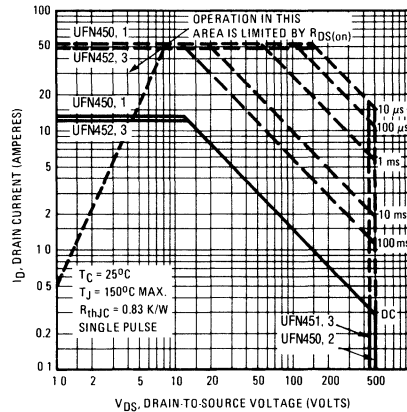


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

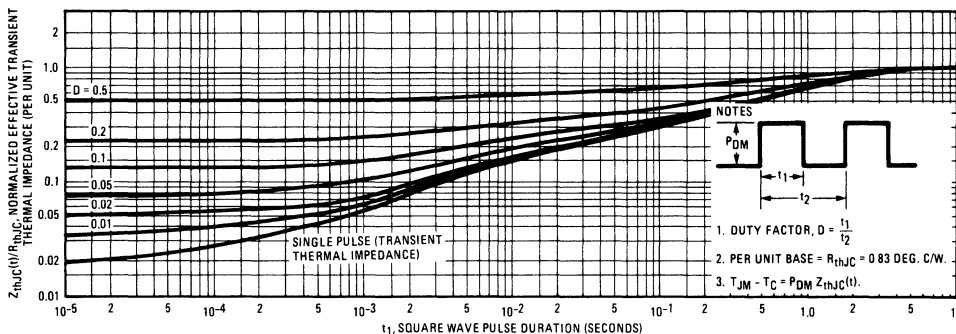


Fig. 6 – Typical Transconductance Vs. Drain Current

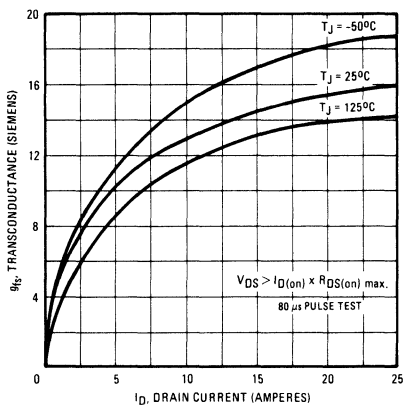


Fig. 7 – Typical Source-Drain Diode Forward Voltage

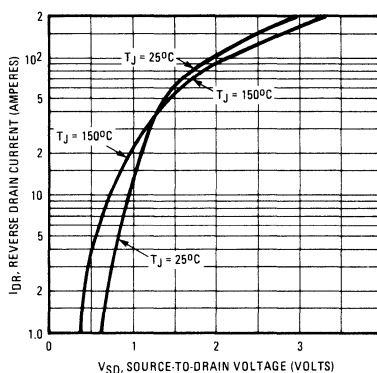


Fig. 8 – Breakdown Voltage Vs. Temperature

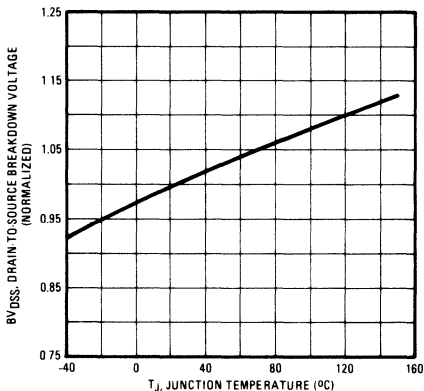


Fig. 9 – Normalized On-Resistance Vs. Temperature

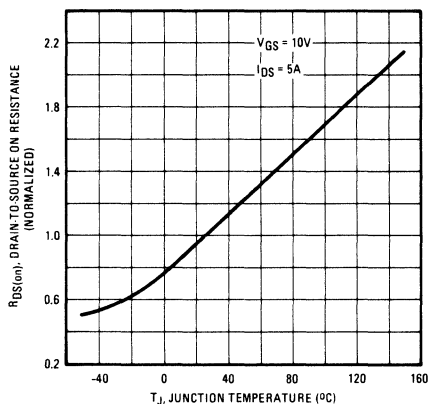


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

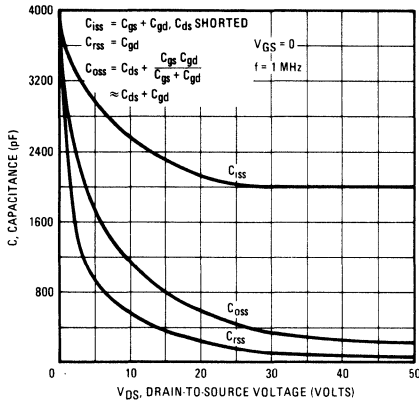


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

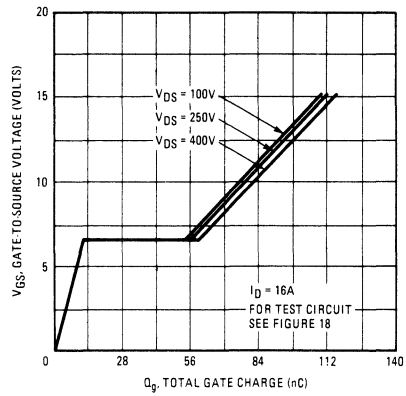


Fig. 12 – Typical On-Resistance Vs. Drain Current

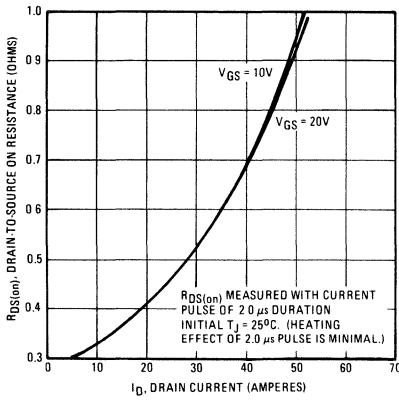


Fig. 13 – Maximum Drain Current Vs. Case Temperature

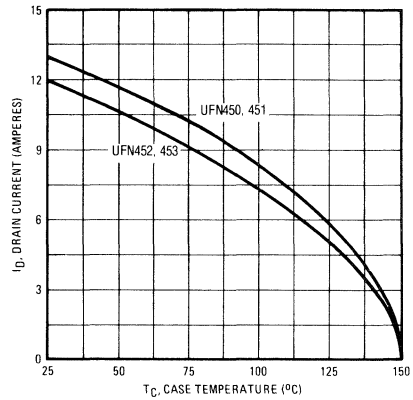


Fig. 14 – Power Vs. Temperature Derating Curve

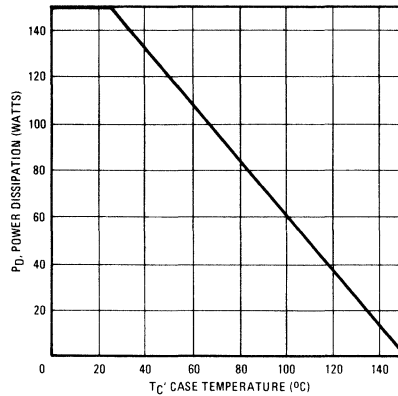


Fig. 15 — Clamped Inductive Test Circuit

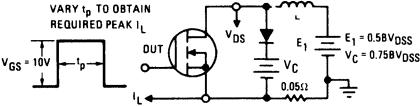
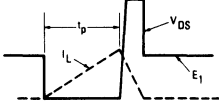


Fig. 16 — Clamped Inductive Waveforms



4

Fig. 17 — Switching Time Test Circuit

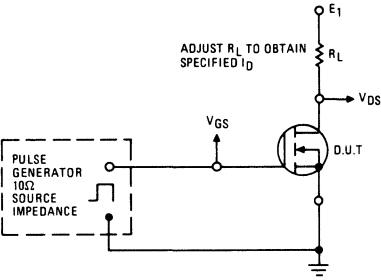
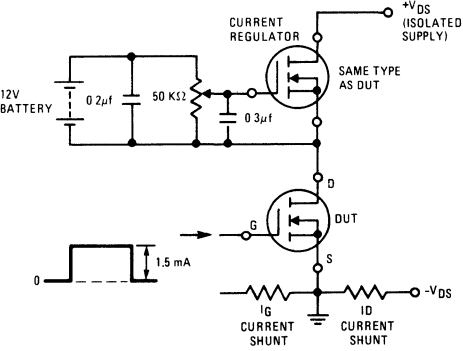


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.6 Ohm
N-Channel

UFN510
UFN511
UFN512
UFN513

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

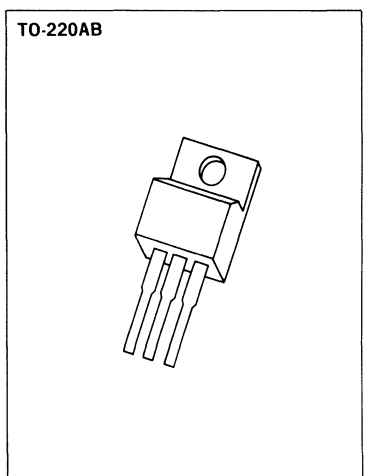
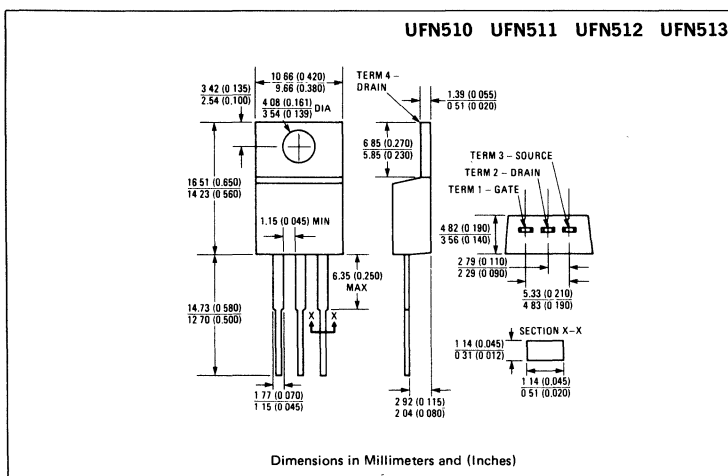
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _D
UFN510	100V	0.6Ω	4.0A
UFN511	60V	0.6Ω	4.0A
UFN512	100V	0.8Ω	3.5A
UFN513	60V	0.8Ω	3.5A

MECHANICAL SPECIFICATIONS

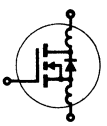


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN510	UFN511	UFN512	UFN513	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	4.0	4.0	3.5	3.5	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM} Pulsed Drain Current ③	16	16	14	14	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN510 UFN512	100	—	—	V	$V_{GS} = 0\text{V}$	
	UFN511 UFN513	60	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN510 UFN511	4.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$	
	UFN512 UFN513	3.5	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN510 UFN511	—	0.5	0.6	Ω	$V_{GS} = 10\text{V}, I_D = 2.0\text{A}$	
	UFN512 UFN513	—	0.6	0.8	Ω		
g_{fs} Forward Transconductance ②	ALL	1.0	1.5	—	S (f)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 2.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	135	150	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	80	100	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	20	25	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	10	20	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 2.0\text{A}, Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	15	25	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	15	25	ns		
t_f Fall Time	ALL	—	10	20	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	$V_{GS} = 10\text{V}, I_D = 8.0\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
		—	2.0	—	nC		
Q_{gs} Gate-Source Charge	ALL	—	2.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN510	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN511	—	—	—	—	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN510	—	—	16	A	
		UFN511	—	—	14	A	
V_{SD}	Diode Forward Voltage ②	UFN510	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 4.0\text{A}, V_{GS} = 0\text{V}$
		UFN511	—	—	—	—	—
t_{rr}	Reverse Recovery Time	UFN510	—	—	230	ns	$T_J = 150^\circ\text{C}, I_F = 4.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
		UFN511	—	—	—	—	
Q_{RR}	Reverse Recovered Charge	ALL	—	1.4	—	μC	$T_J = 150^\circ\text{C}, I_F = 4.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

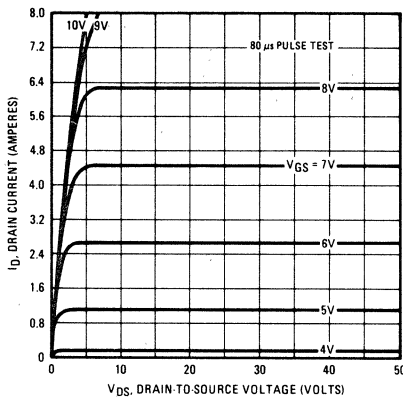


Fig. 2 – Typical Transfer Characteristics

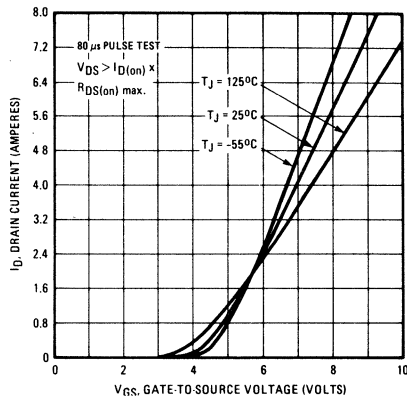


Fig. 3 – Typical Saturation Characteristics

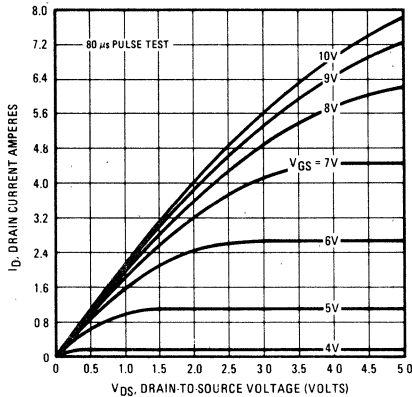


Fig. 4 – Maximum Safe Operating Area

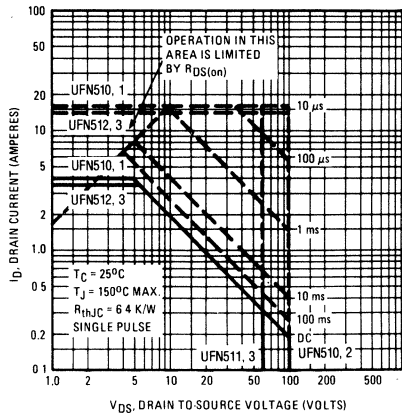
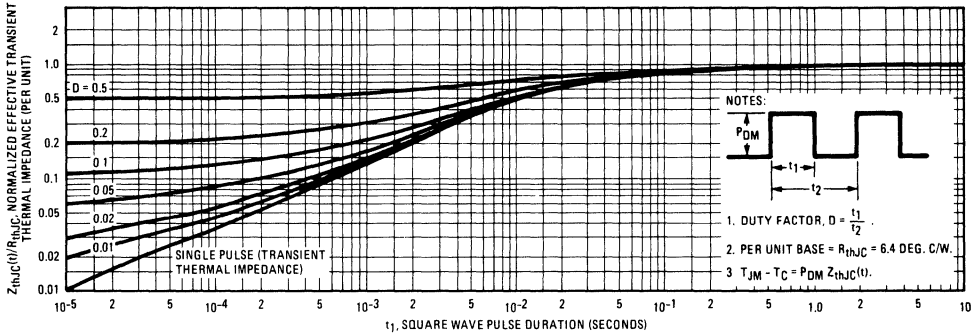


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

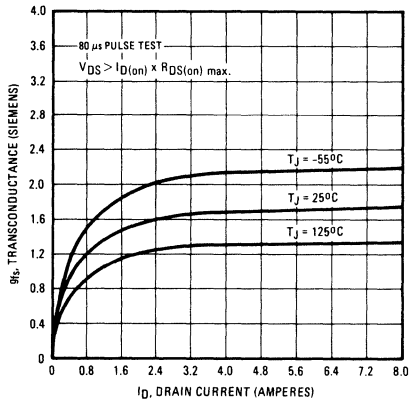


Fig. 7 – Typical Source-Drain Diode Forward Voltage

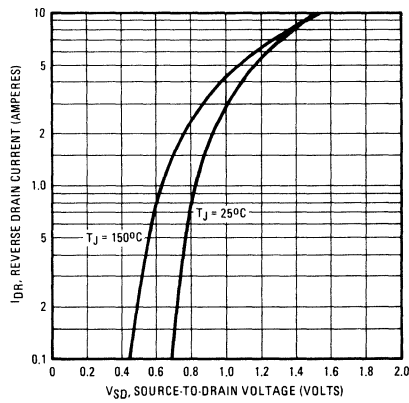


Fig. 8 – Breakdown Voltage Vs. Temperature

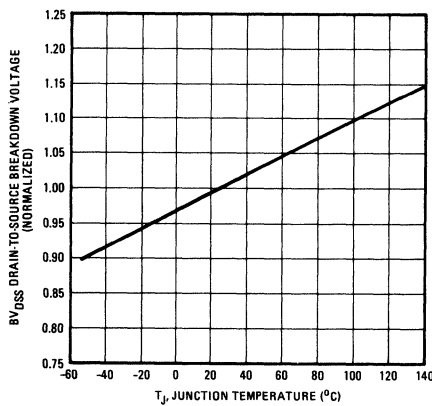


Fig. 9 – Normalized On-Resistance Vs. Temperature

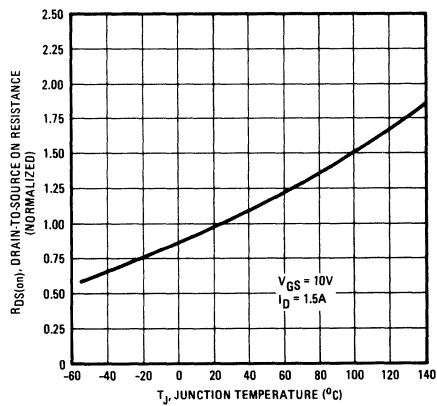


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

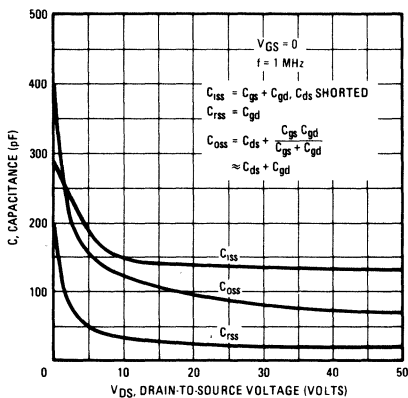


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

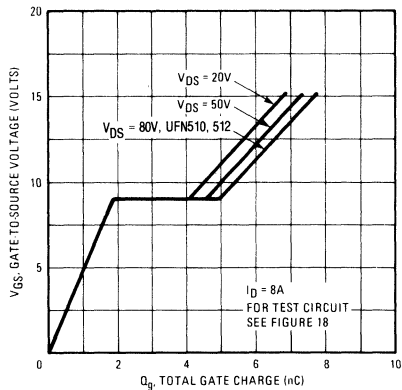


Fig. 12 – Typical On-Resistance Vs. Drain Current

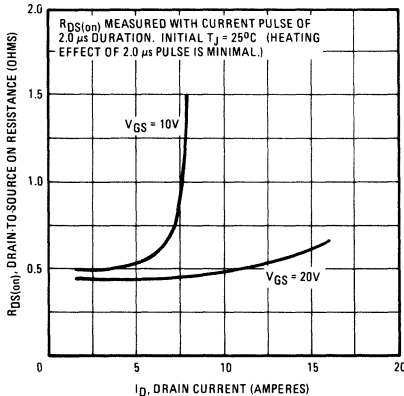


Fig. 13 – Maximum Drain Current Vs. Case Temperature

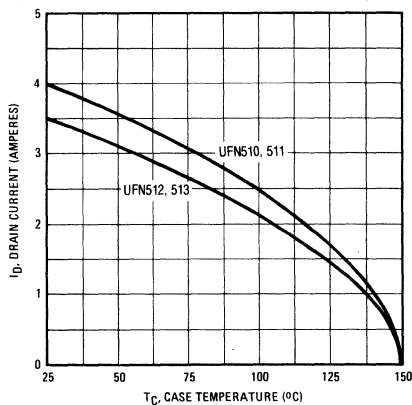


Fig. 14 – Power Vs. Temperature Derating Curve

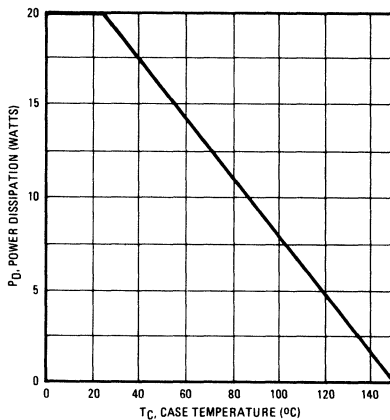


Fig. 15 – Clamped Inductive Test Circuit

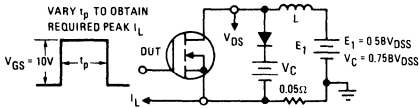


Fig. 16 – Clamped Inductive Waveforms

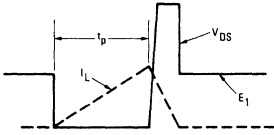


Fig. 17 – Switching Time Test Circuit

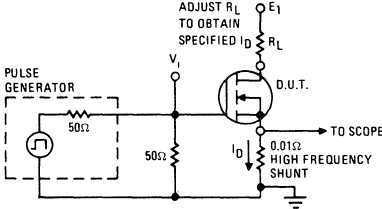
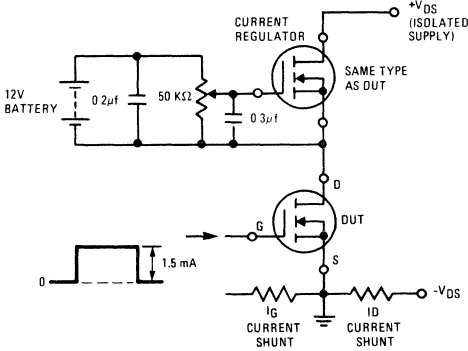


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm
N-Channel

UFN520
UFN521
UFN522
UFN523

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

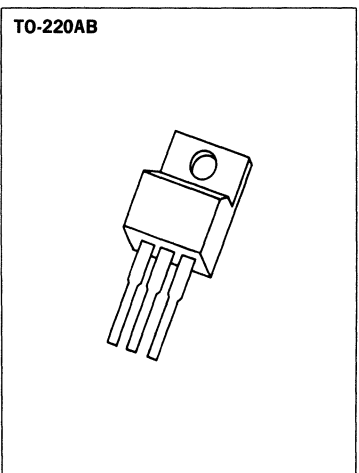
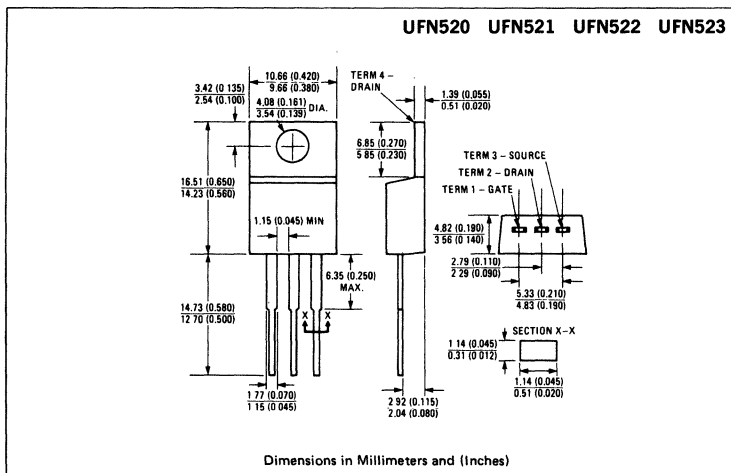
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _p
UFN520	100V	0.30Ω	8.0A
UFN521	60V	0.30Ω	8.0A
UFN522	100V	0.40Ω	7.0A
UFN523	60V	0.40Ω	7.0A

MECHANICAL SPECIFICATIONS

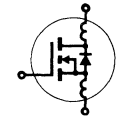


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN520	UFN521	UFN522	UFN523	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	8.0	8.0	7.0	7.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM} Pulsed Drain Current ③	32	32	28	28	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN520 UFN522	100	—	—	V	$V_{GS} = 0\text{V}$	
	UFN521 UFN523	60	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN520 UFN521	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$	
	UFN522 UFN523	7.0	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN520 UFN521	—	0.25	0.30	Ω	$V_{GS} = 10\text{V}, I_D = 4.0\text{A}$	
	UFN522 UFN523	—	0.30	0.40	Ω		
g_{fs} Forward Transconductance ②	ALL	1.5	2.9	—	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 4.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	450	600	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	200	400	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	50	100	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 4.0\text{A}, Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	35	70	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	50	100	ns		
t_f Fall Time	ALL	—	35	70	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC	$V_{GS} = 15\text{V}, I_D = 10\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC		
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN520	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN521	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN520	—	—	32	A	
		UFN522	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN520	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$
		UFN521	—	—	2.3	V	
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

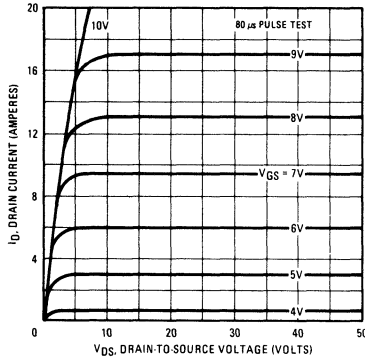


Fig. 2 – Typical Transfer Characteristics

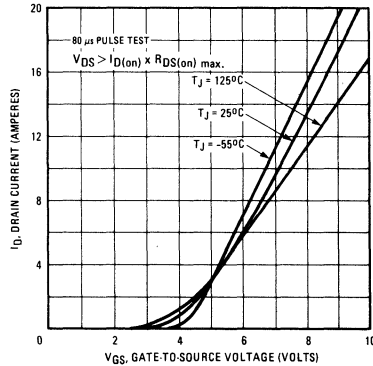


Fig. 3 – Typical Saturation Characteristics

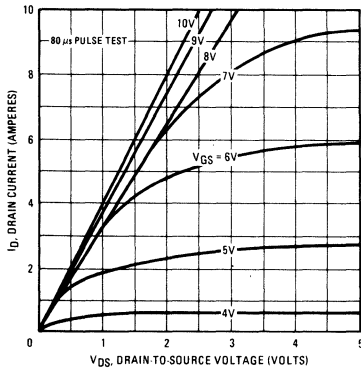


Fig. 4 – Maximum Safe Operating Area

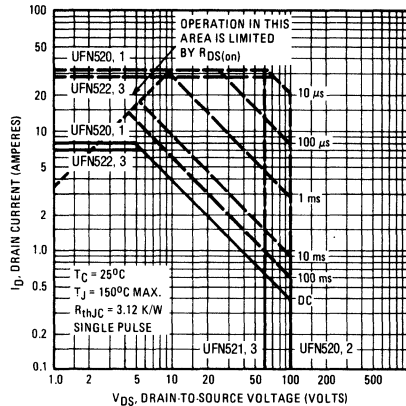


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

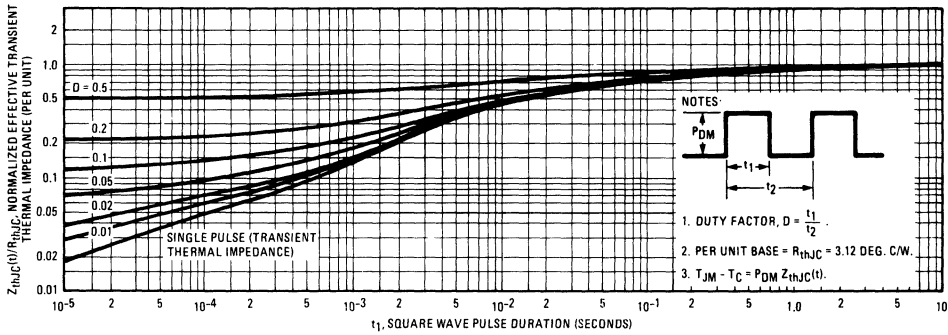


Fig. 6 – Typical Transconductance Vs. Drain Current

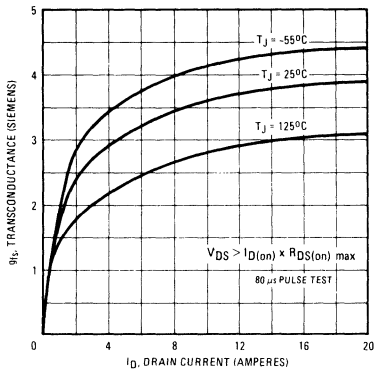


Fig. 7 – Typical Source-Drain Diode Forward Voltage

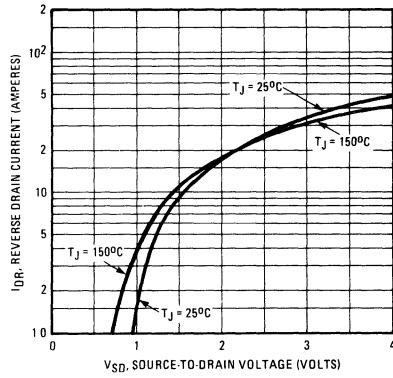


Fig. 8 – Breakdown Voltage Vs. Temperature

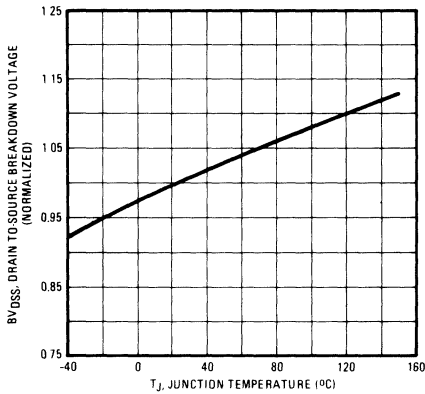


Fig. 9 – Normalized On-Resistance Vs. Temperature

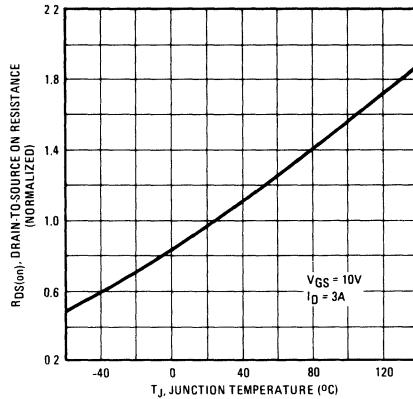


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

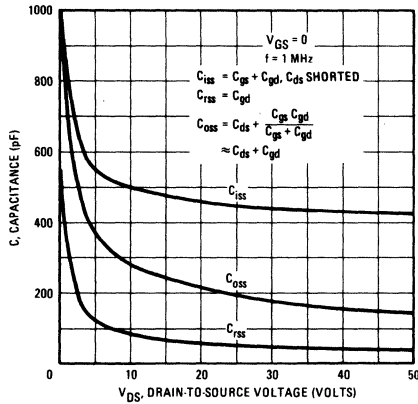


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

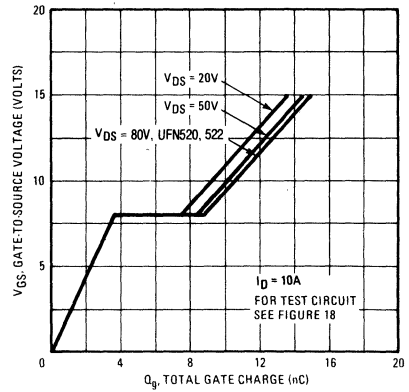


Fig. 12 – Typical On-Resistance Vs. Drain Current

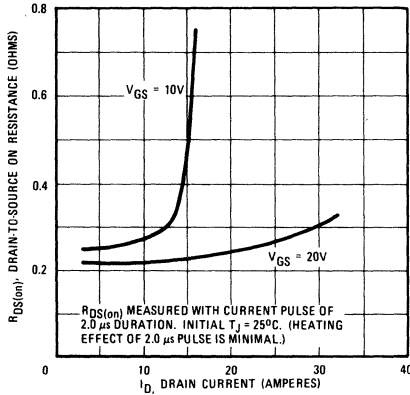


Fig. 13 – Maximum Drain Current Vs. Case Temperature

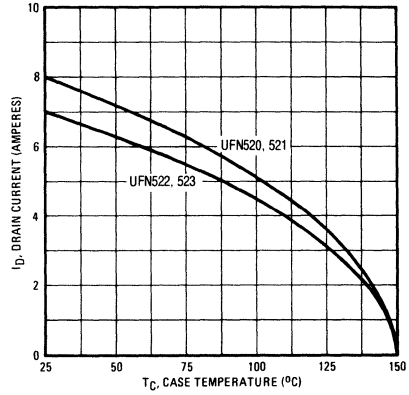


Fig. 14 – Power Vs. Temperature Derating Curve

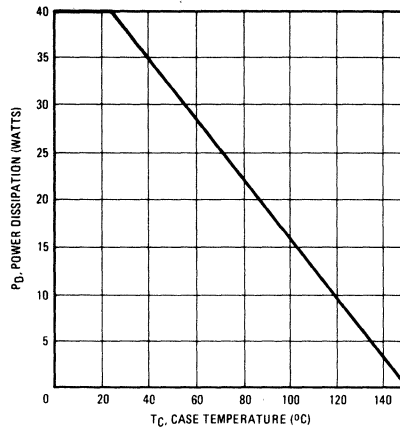


Fig. 15 – Clamped Inductive Test Circuit

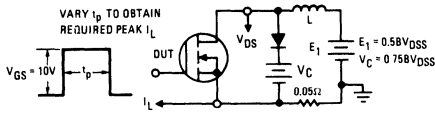
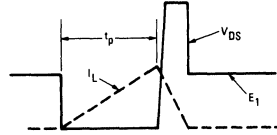


Fig. 16 – Clamped Inductive Waveforms



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Fig. 17 – Switching Time Test Circuit

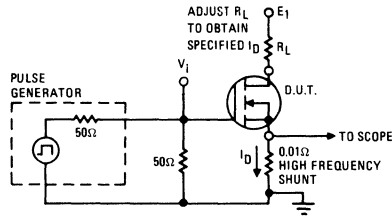
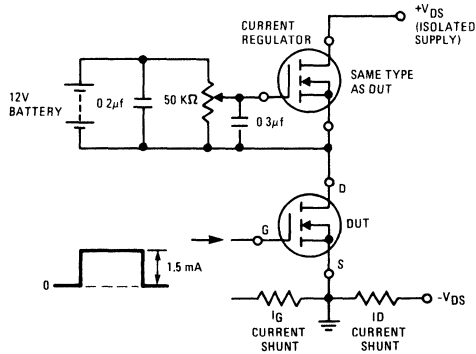


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFN530
UFN531
UFN532
UFN533

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

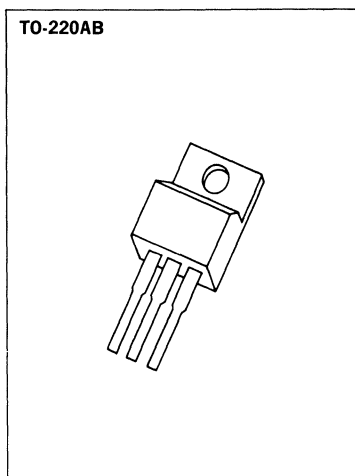
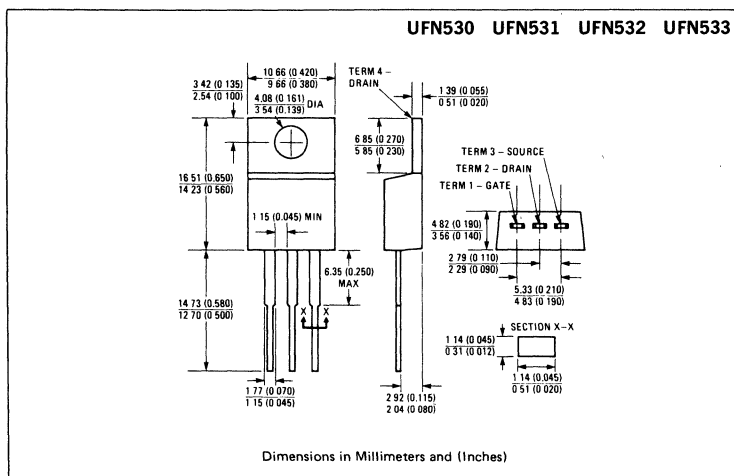
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN530	100V	0.18Ω	14A
UFN531	60V	0.18Ω	14A
UFN532	100V	0.25Ω	12A
UFN533	60V	0.25Ω	12A

MECHANICAL SPECIFICATIONS

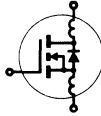


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN530	UFN531	UFN532	UFN533	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	14	14	12	12	A
I _D @ T _C = 100°C Continuous Drain Current	9.0	9.0	8.0	8.0	A
I _{DM} Pulsed Drain Current ③	56	56	48	48	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	56	56	48	48	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C




ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN530 UFN532	100	—	—	V	V _{GS} = 0V	
	UFN531 UFN533	60	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN530 UFN531	14	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max.; V _{GS} = 10V	
	UFN532 UFN533	12	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN530 UFN531	—	0.14	0.18	Ω	V _{GS} = 10V, I _D = 8.0A	
	UFN532 UFN533	—	0.20	0.25	Ω		
g _{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max.; I _D = 8.0A	
C _{iss} Input Capacitance	ALL	—	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	300	500	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	100	150	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 36V, I _D = 8.0A, Z _o = 15Ω	
t _r Rise Time	ALL	—	—	75	ns	See Fig. 17	
t _{d(off)} Turn-Off Delay Time	ALL	—	—	40	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	—	45	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	9.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN530	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN532 UFN533	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN530	—	—	56	A	
		UFN532 UFN533	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN530 UFN531	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 14\text{A}, V_{GS} = 0\text{V}$
		UFN532 UFN533	—	—	2.3	V	
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by junction temperature by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

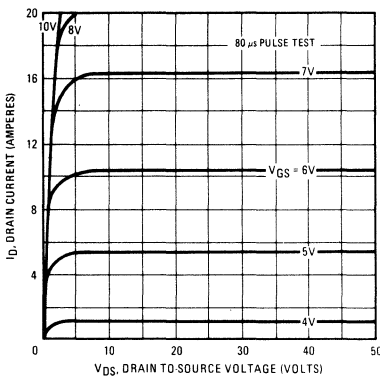


Fig. 2 – Typical Transfer Characteristics

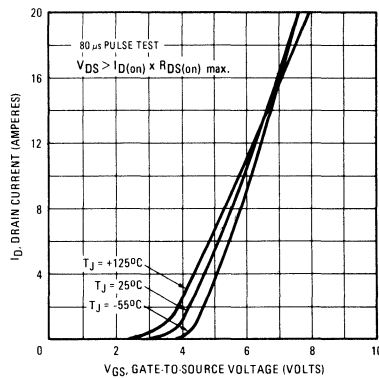


Fig. 3 – Typical Saturation Characteristics

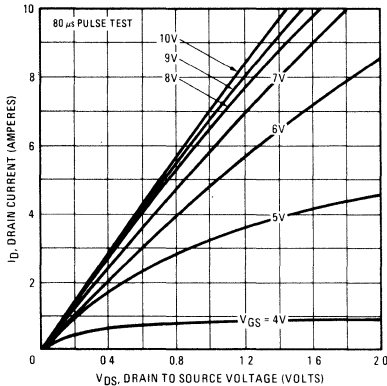


Fig. 4 – Maximum Safe Operating Area

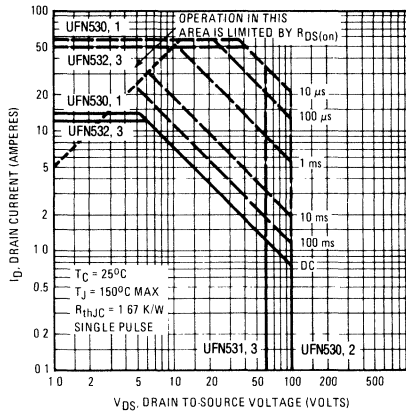
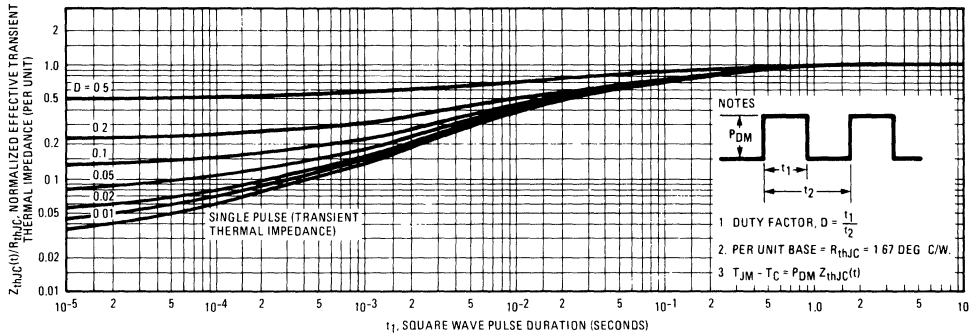


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 — Typical Transconductance Vs. Drain Current

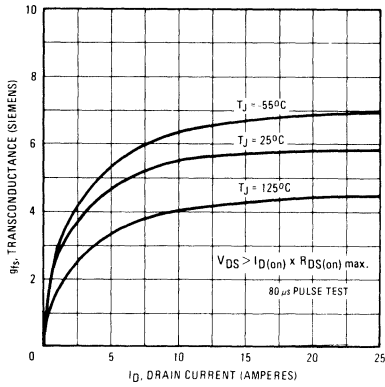


Fig. 7 — Typical Source-Drain Diode Forward Voltage

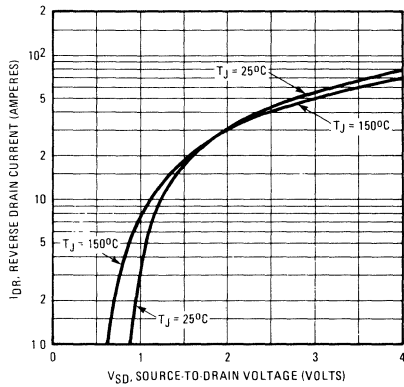


Fig. 8 — Breakdown Voltage Vs. Temperature

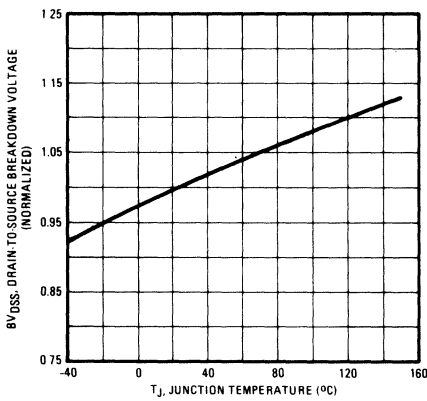


Fig. 9 — Normalized On-Resistance Vs. Temperature

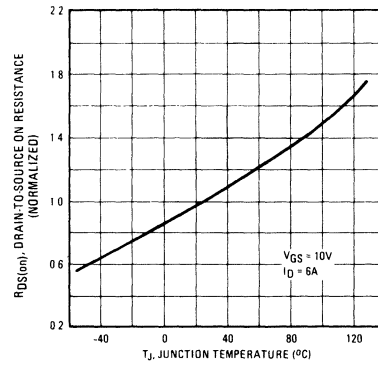


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

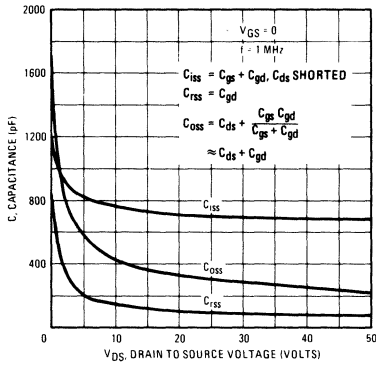


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

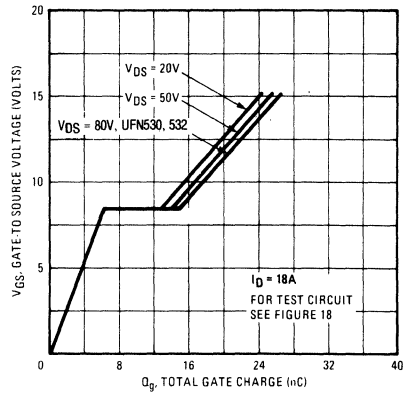


Fig. 12 – Typical On-Resistance Vs. Drain Current

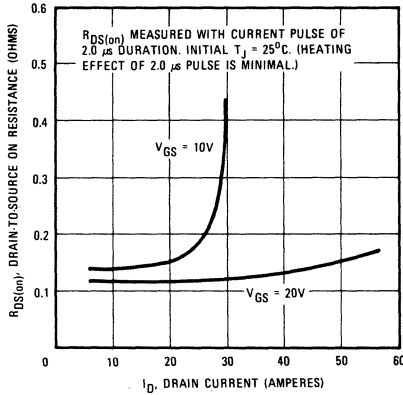


Fig. 13 – Maximum Drain Current Vs. Case Temperature

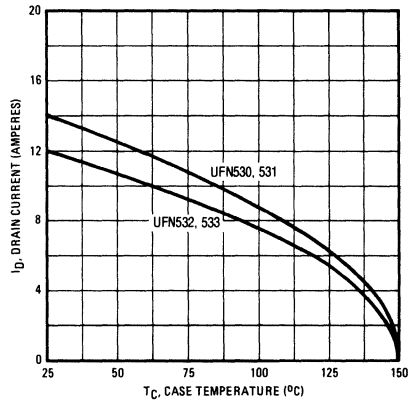


Fig. 14 – Power Vs. Temperature Derating Curve

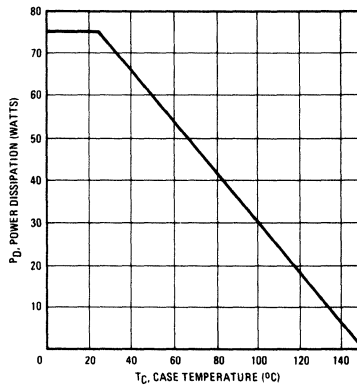


Fig. 15 — Clamped Inductive Test Circuit

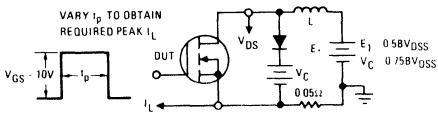


Fig. 16 — Clamped Inductive Waveforms

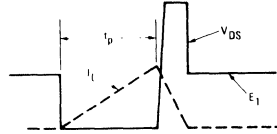


Fig. 17 — Switching Time Test Circuit

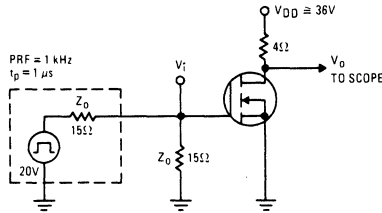
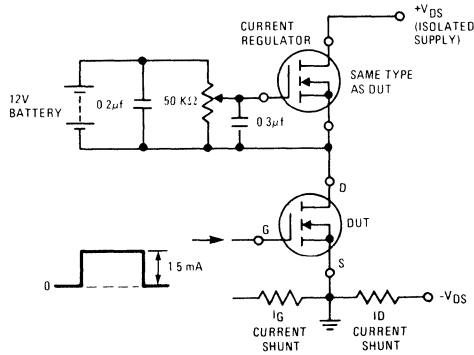


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.085 Ohm N-Channel

UFN540
UFN541
UFN542
UFN543

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

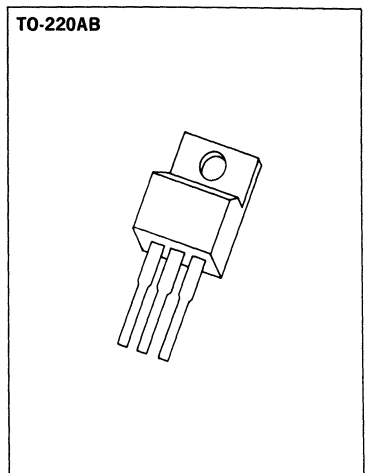
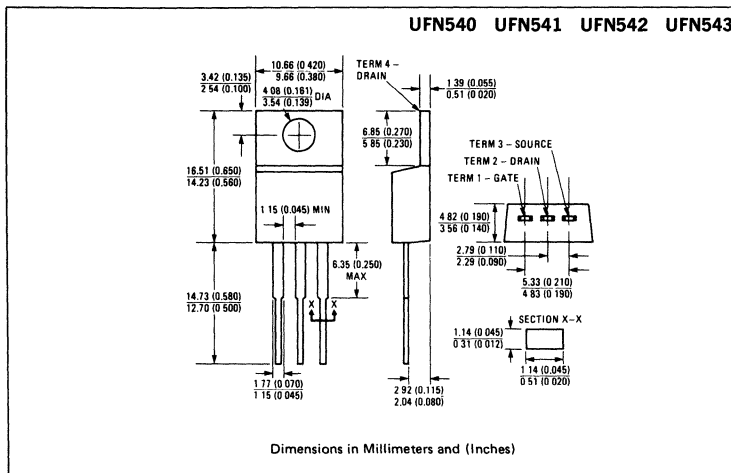
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN540	100V	0.085Ω	27A
UFN541	60V	0.085Ω	27A
UFN542	100V	0.11Ω	24A
UFN543	60V	0.11Ω	24A

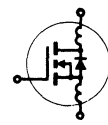
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN540	UFN541	UFN542	UFN543	Units
V _{DS} Drain - Source Voltage ①	100	60	100	60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C Continuous Drain Current	27	27	24	24	A
I _D @ T _C = 100°C Continuous Drain Current	17	17	15	15	A
I _{DM} Pulsed Drain Current ③	108	108	96	96	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125		(See Fig. 14)		W
Linear Derating Factor		1.0		(See Fig. 14) W/K	
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	108	108	96	96	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN540 UFN542	100	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN541 UFN543	60	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
		—	—	1000	μA		
I _{D(on)} On-State Drain Current ②	UFN540 UFN541	27	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
	UFN542 UFN543	24	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN540 UFN541	—	0.07	0.085	Ω	V _{GS} = 10V, I _D = 15A	
	UFN542 UFN543	—	0.09	0.11	Ω		
g _{fs} Forward Transconductance ②	ALL	6.0	10	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 15A	
C _{iss} Input Capacitance	ALL	—	1275	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	550	800	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	160	300	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	16	30	ns	V _{DD} = 30V, I _D = 15A, Z _o = 4.7Ω See Fig. 17	
t _r Rise Time	ALL	—	27	60	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	38	80	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	14	30	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V _{GS} = 10V, I _D = 34A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	17	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	21	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN540 UFN541	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN542 UFN543	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN540 UFN541	—	—	108	A	
		UFN542 UFN543	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	UFN540 UFN541	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 27\text{A}, V_{GS} = 0\text{V}$
		UFN542 UFN543	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 24\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150^\circ\text{C}, I_F = 27\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	$T_J = 150^\circ\text{C}, I_F = 27\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

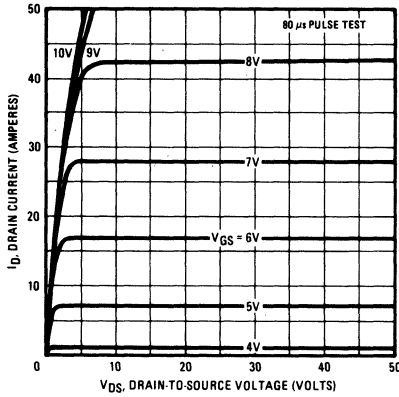


Fig. 2 – Typical Transfer Characteristics

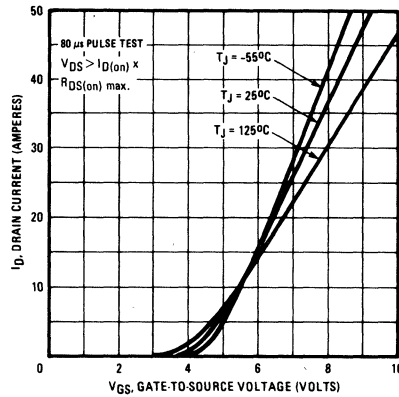


Fig. 3 – Typical Saturation Characteristics

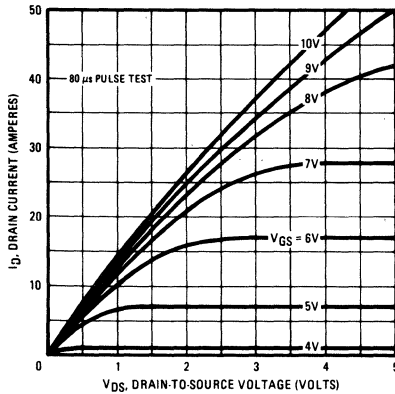


Fig. 4 – Maximum Safe Operating Area

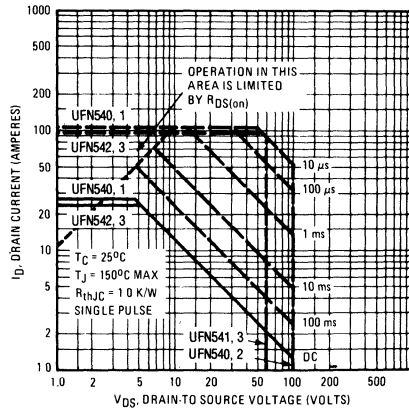


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

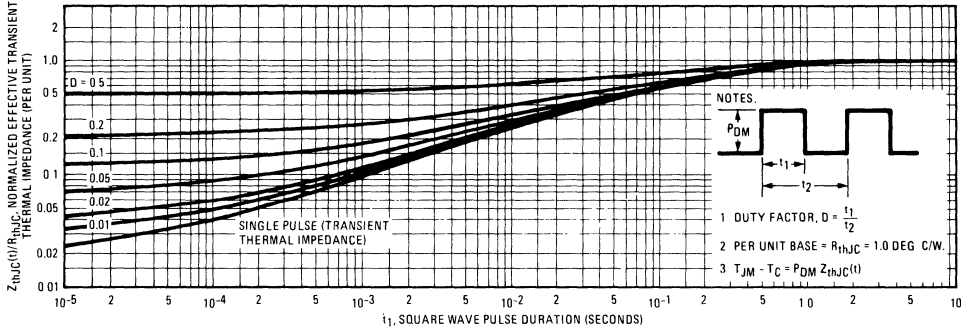


Fig. 6 – Typical Transconductance Vs. Drain Current

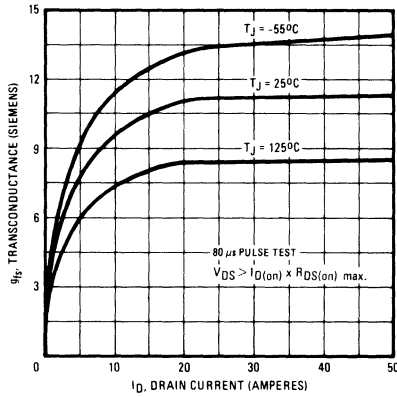


Fig. 7 – Typical Source-Drain Diode Forward Voltage

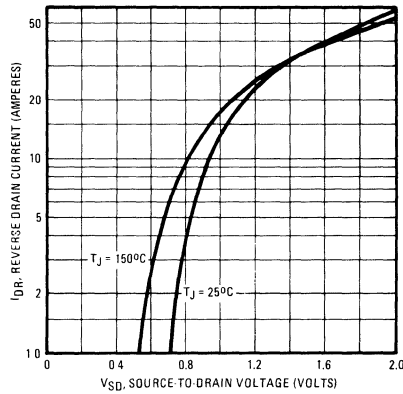


Fig. 8 – Breakdown Voltage Vs. Temperature

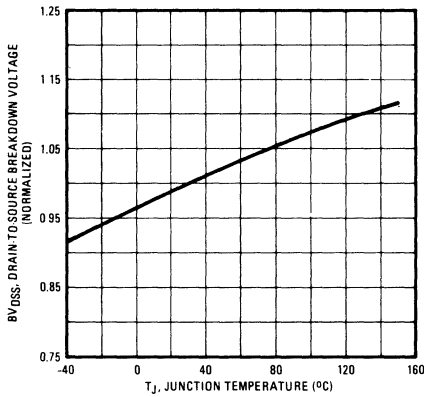


Fig. 9 – Normalized On-Resistance Vs. Temperature

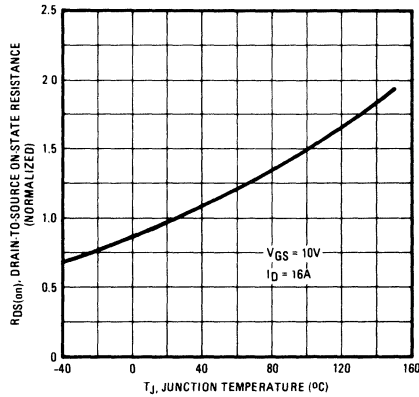


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

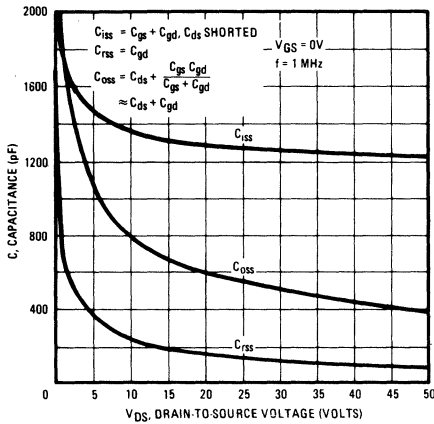


Fig. 12 – Typical On-Resistance Vs. Drain Current

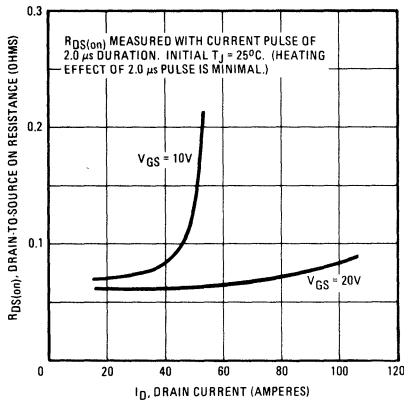


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

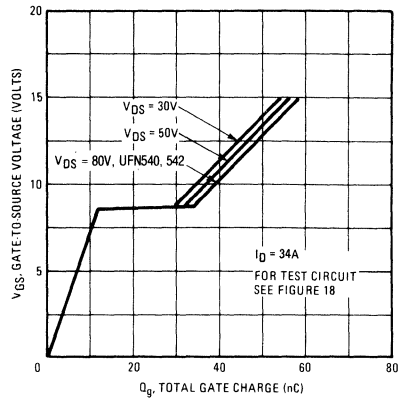


Fig. 13 – Maximum Drain Current Vs. Case Temperature

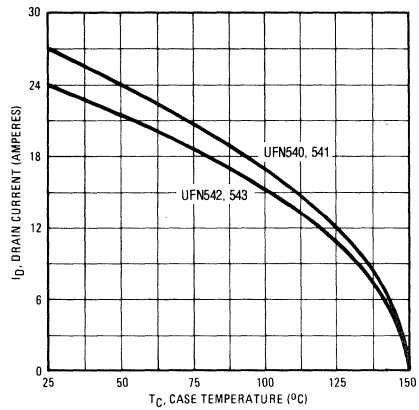


Fig. 14 – Power Vs. Temperature Derating Curve

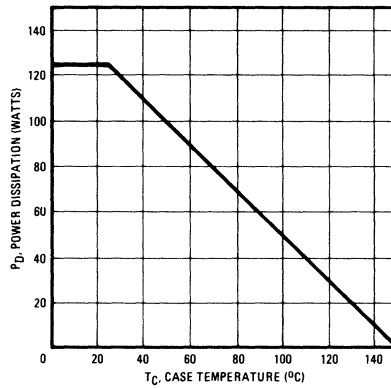


Fig. 15 — Clamped Inductive Test Circuit

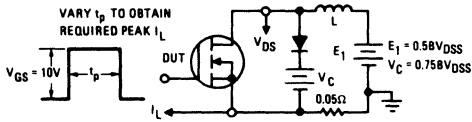


Fig. 16 — Clamped Inductive Waveforms

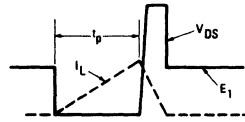


Fig. 17 — Switching Time Test Circuit

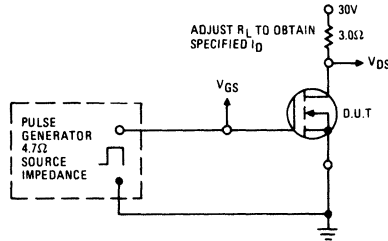
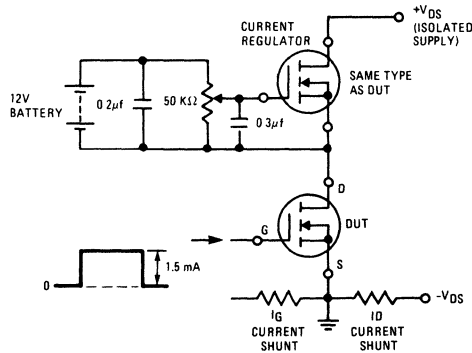


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

UFN610
UFN611
UFN612
UFN613

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

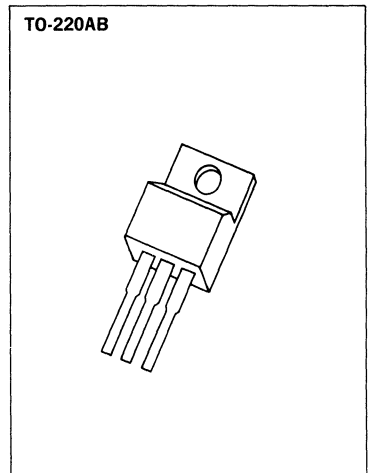
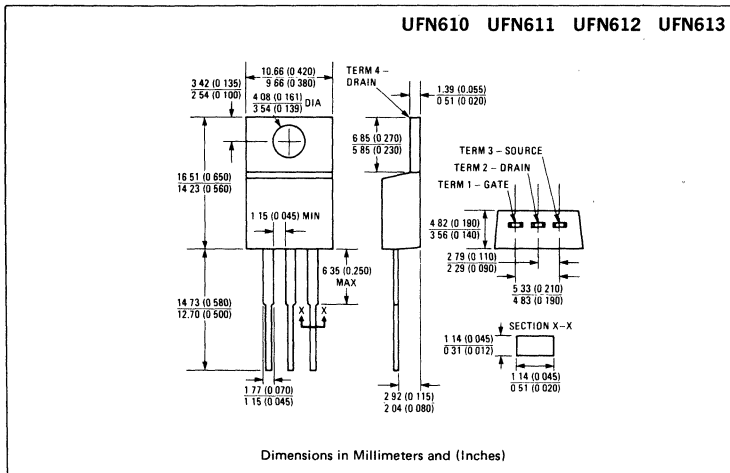
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN610	200V	1.5Ω	2.5A
UFN611	150V	1.5Ω	2.5A
UFN612	200V	2.4Ω	2.0A
UFN613	150V	2.4Ω </td <td>2.0A</td>	2.0A

MECHANICAL SPECIFICATIONS

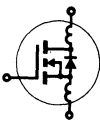


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN610	UFN611	UFN612	UFN613	Units
V _{DS} Drain - Source Voltage ①	200	150	200	150	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	2.5	2.5	2.0	2.0	A
I _D @ T _C = 100°C Continuous Drain Current	1.5	1.5	1.25	1.25	A
I _{DM} Pulsed Drain Current ③	10	10	8.0	8.0	A
V _{GS} Gate - Source Voltage					± 20
P _D @ T _C = 25°C Max. Power Dissipation	20				(See Fig. 14) W
Linear Derating Factor	0.16				(See Fig. 14) W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	10	10	8.0	8.0	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C




ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN610 UFN612	200	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN611 UFN613	150	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate - Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate - Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN610 UFN611	2.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN612 UFN613	2.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN610 UFN611	—	1.0	1.5	Ω	V _{GS} = 10V, I _D = 1.25A	
	UFN612 UFN613	—	1.5	2.4	Ω		
g _{fs} Forward Transconductance ②	ALL	0.8	1.3	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 1.25A	
C _{iss} Input Capacitance	ALL	—	135	150	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	60	80	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	16	25	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	8.0	15	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 1.25A, Z _o = 50Ω See Fig. 17	
t _r Rise Time	ALL	—	15	25	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	10	15	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	8.0	15	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V _{GS} = 10V, I _D = 3.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	2.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	6.4	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN610	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN611	—	—	2.0	A	
		UFN612 UFN613	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN610	—	—	10	A	
		UFN611	—	—	10	A	
		UFN612 UFN613	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFN610 UFN611	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
		UFN612 UFN613	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

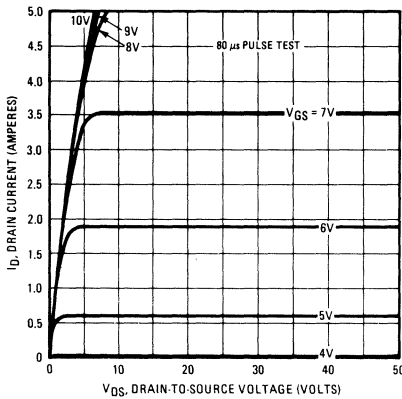


Fig. 2 – Typical Transfer Characteristics

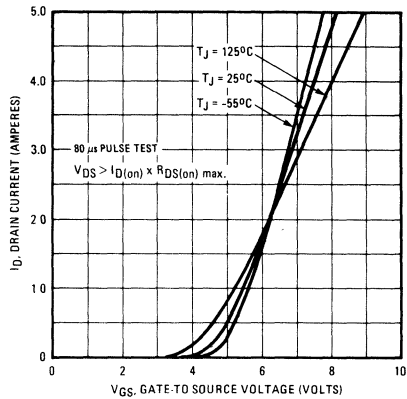


Fig. 3 – Typical Saturation Characteristics

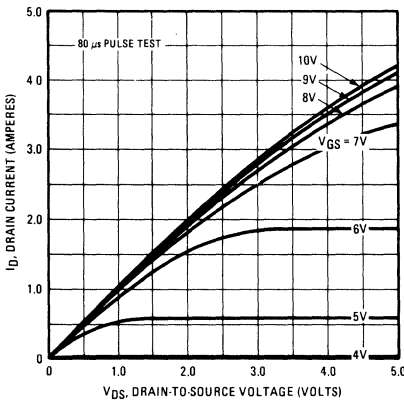


Fig. 4 – Maximum Safe Operating Area

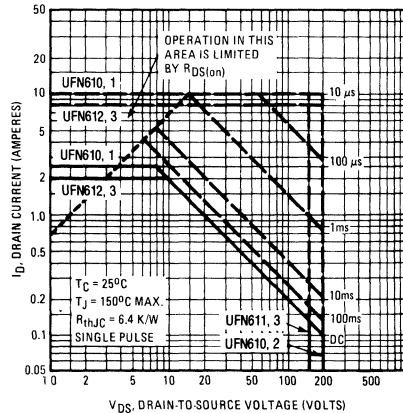
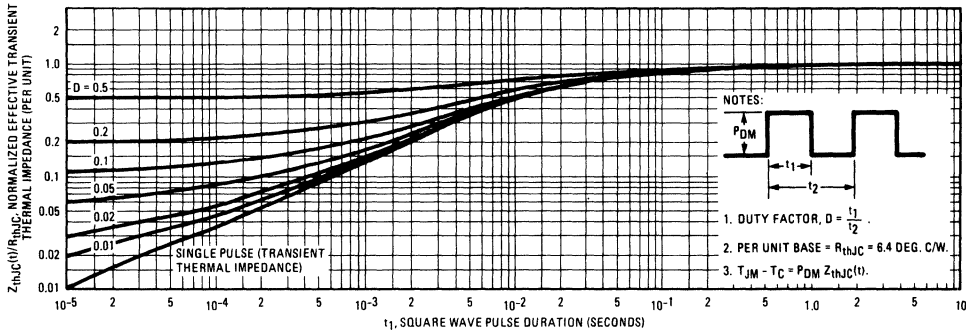


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

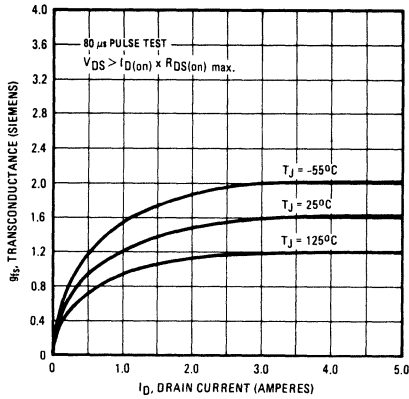


Fig. 7 – Typical Source-Drain Diode Forward Voltage

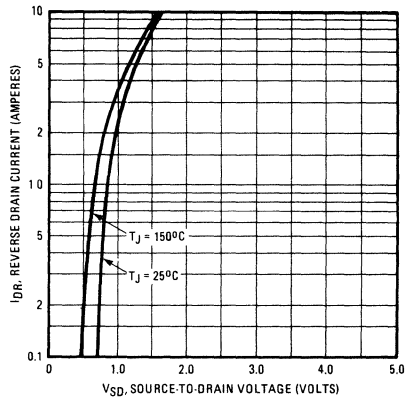


Fig. 8 – Breakdown Voltage Vs. Temperature

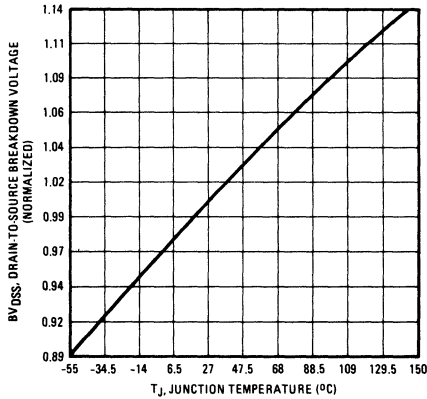


Fig. 9 – Normalized On-Resistance Vs. Temperature

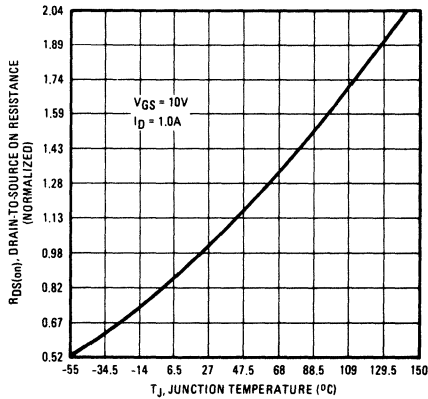


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

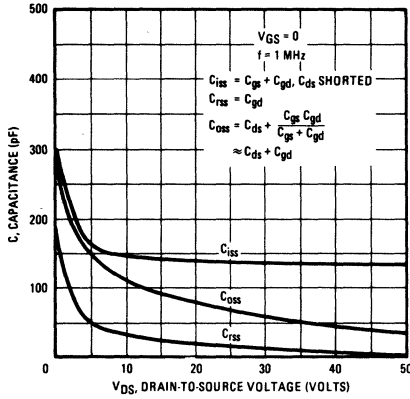


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

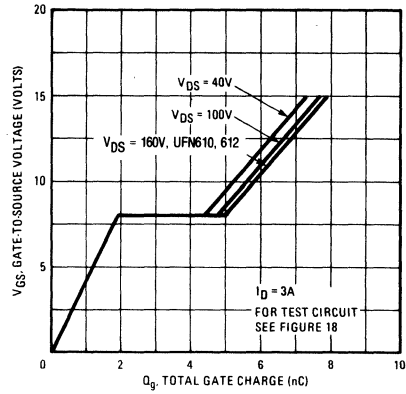


Fig. 12 – Typical On-Resistance Vs. Drain Current

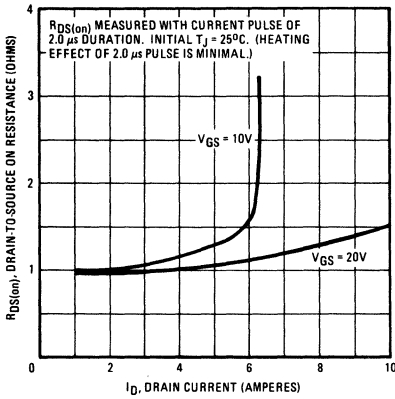


Fig. 13 – Maximum Drain Current Vs. Case Temperature

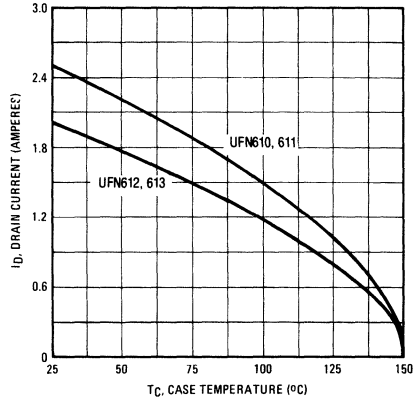


Fig. 14 – Power Vs. Temperature Derating Curve

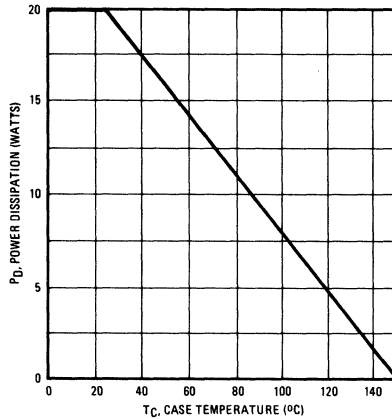


Fig. 15 – Clamped Inductive Test Circuit

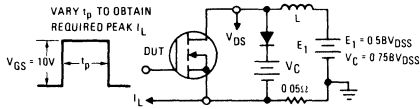


Fig. 16 – Clamped Inductive Waveforms

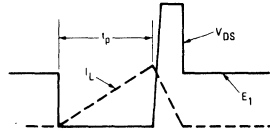


Fig. 17 – Switching Time Test Circuit

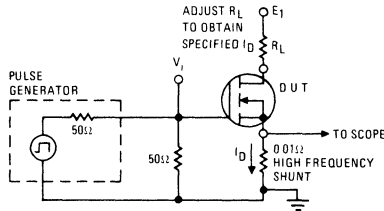
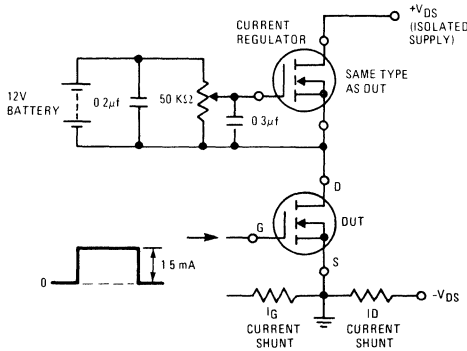


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.8 Ohm
N-Channel

UFN620
UFN621
UFN622
UFN623

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

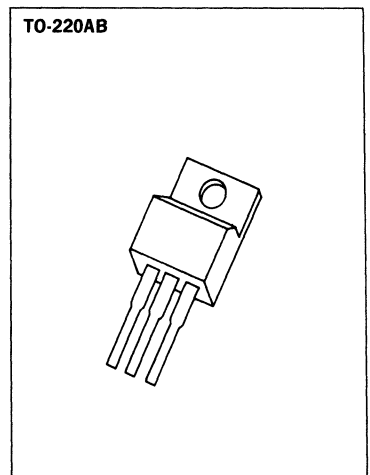
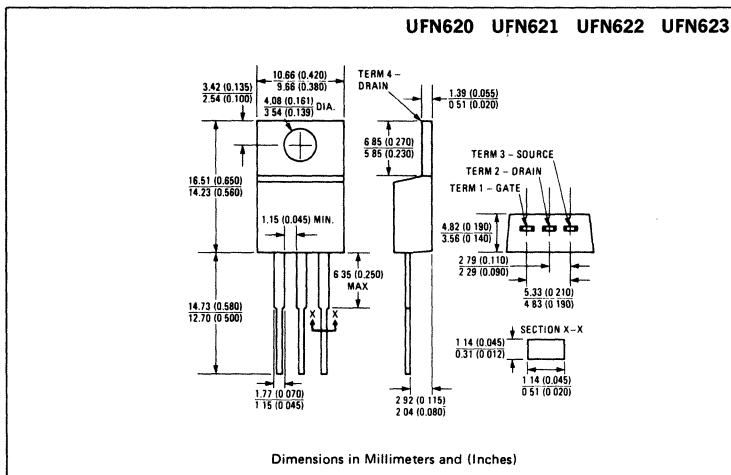
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN620	200V	0.8Ω	5.0A
UFN621	150V	0.8Ω	5.0A
UFN622	200V	1.2Ω	4.0A
UFN623	150V	1.2Ω	4.0A

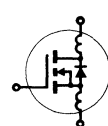
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter		UFN620	UFN621	UFN622	UFN623	Units
V _{DS}	Drain - Source Voltage ①	200	150	200	150	V
V _{DGR}	Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I _D @ T _C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I _{DM}	Pulsed Drain Current ③	20	20	16	16	A
V _{GS}	Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T _J T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN620 UFN622	200	—	—	V	V _{GS} = 0V	
	UFN621 UFN623	150	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN620 UFN621	5.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on) max.} ; V _{GS} = 10V	
	UFN622 UFN623	4.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN620 UFN621	—	0.5	0.8	Ω	V _{GS} = 10V, I _D = 2.5A	
	UFN622 UFN623	—	0.8	1.2	Ω		
g _{fs} Forward Transconductance ②	ALL	1.3	2.5	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on) max.} ; I _D = 2.5A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	150	300	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	40	80	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 2.5 BV _{DSS} ; I _D = 2.5A, Z _o = 50Ω See Fig. 17	
t _r Rise Time	ALL	—	30	60	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	30	60	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V _{GS} = 50V, I _D = 6.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	5.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN620 UFN621	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.			
		UFN622 UFN623	—	—	4.0	A				
I_{SM}	Pulse Source Current (Body Diode) ③	UFN620 UFN621	—	—	20	A				
		UFN622 UFN623	—	—	16	A				
V_{SD}	Diode Forward Voltage ②	UFN620 UFN621	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 5.0\text{A}$, $V_{GS} = 0\text{V}$			
		UFN622 UFN623	—	—	1.4	V		$T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$		
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 5.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$			
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 5.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$			
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.							

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

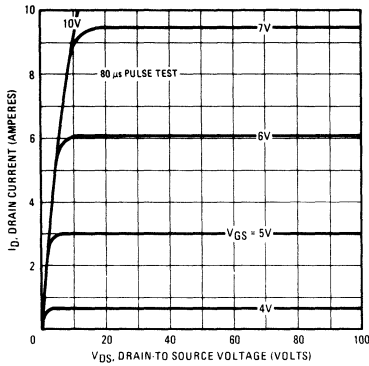


Fig. 2 – Typical Transfer Characteristics

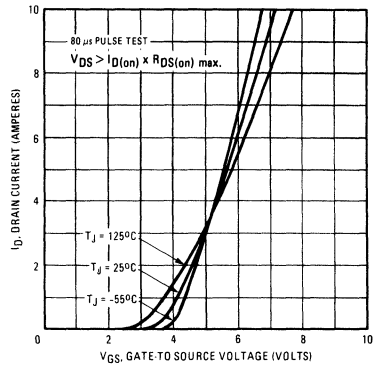


Fig. 3 – Typical Saturation Characteristics

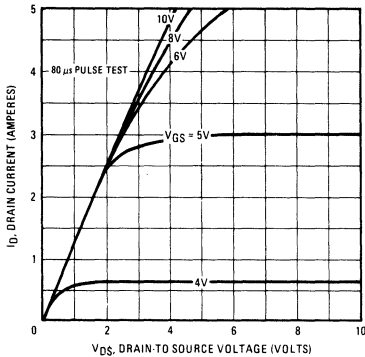


Fig. 4 – Maximum Safe Operating Area

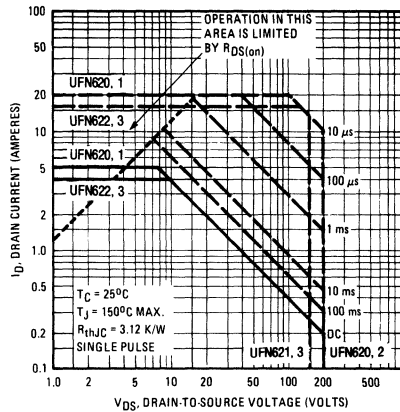


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

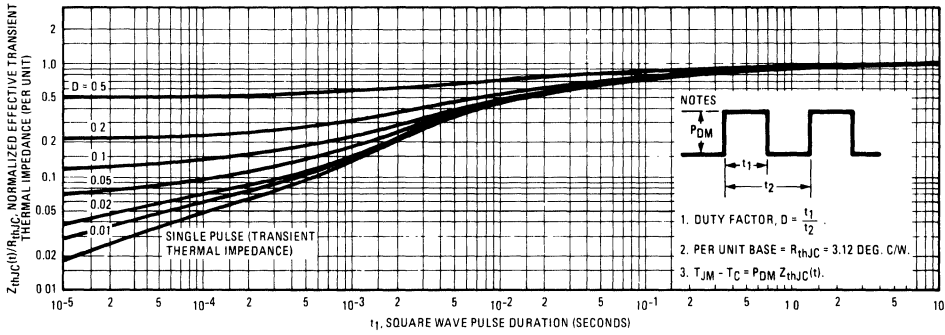


Fig. 6 – Typical Transconductance Vs. Drain Current

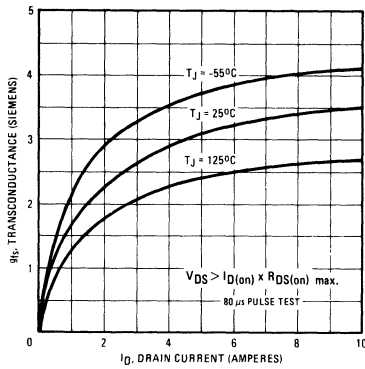


Fig. 7 – Typical Source-Drain Diode Forward Voltage

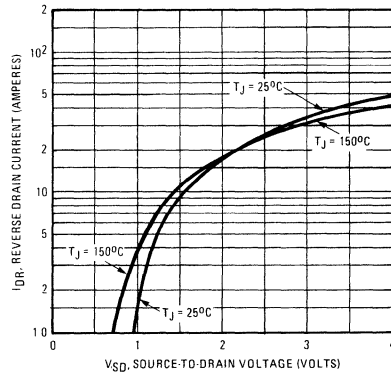


Fig. 8 – Breakdown Voltage Vs. Temperature

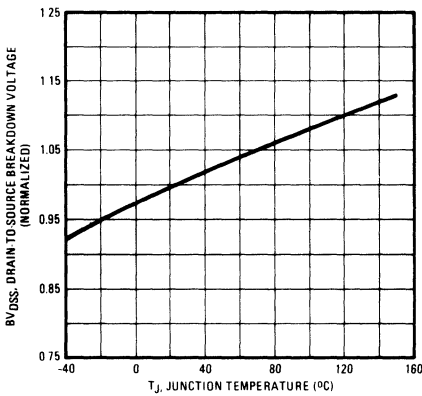


Fig. 9 – Normalized On-Resistance Vs. Temperature

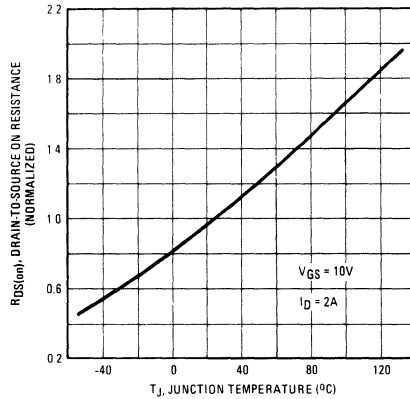


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

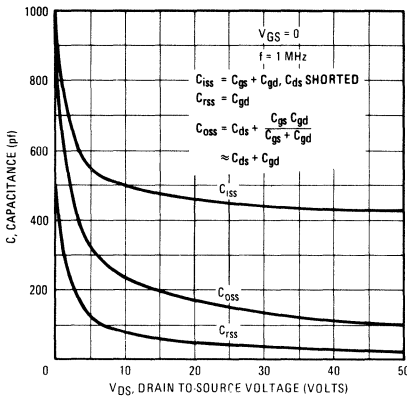


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

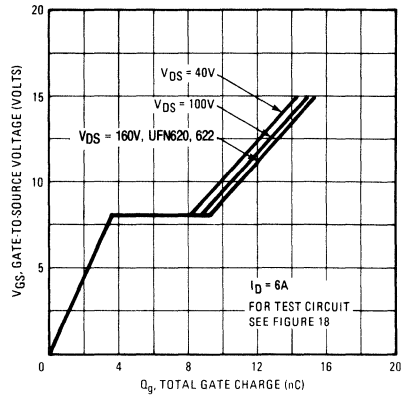


Fig. 12 – Typical On-Resistance Vs. Drain Current

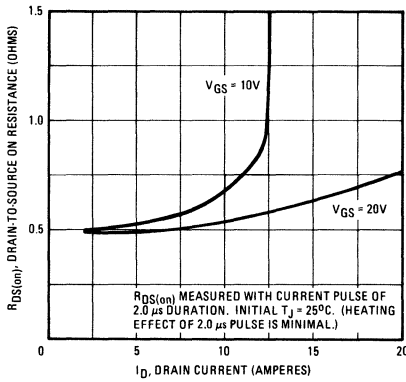


Fig. 13 – Maximum Drain Current Vs. Case Temperature

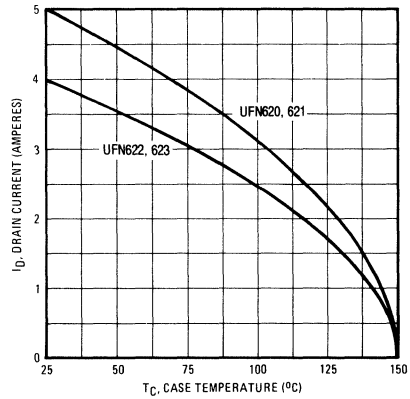


Fig. 14 – Power Vs. Temperature Derating Curve

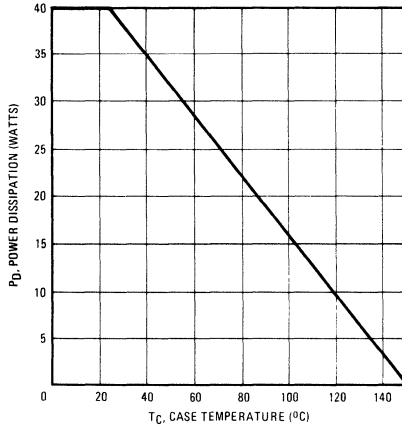


Fig. 15 — Clamped Inductive Test Circuit

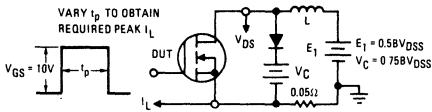


Fig. 16 — Clamped Inductive Waveforms

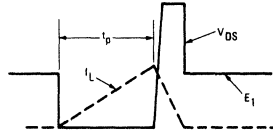


Fig. 17 — Switching Time Test Circuit

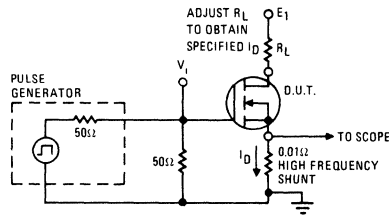
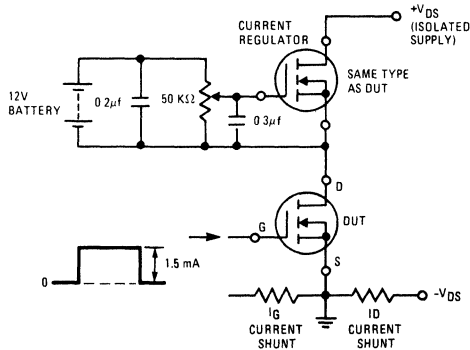


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm N-Channel

UFN630
UFN631
UFN632
UFN633

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

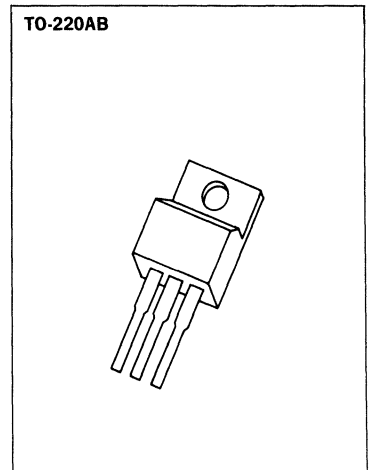
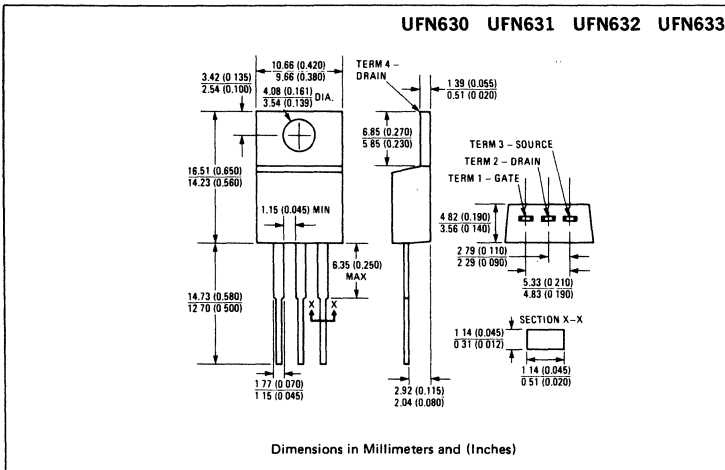
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETs are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN630	200V	0.4 Ω	9.0A
UFN631	150V	0.4 Ω	9.0A
UFN632	200V	0.6 Ω	8.0A
UFN633	150V	0.6 Ω	8.0A

MECHANICAL SPECIFICATIONS

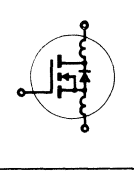


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN630	UFN631	UFN632	UFN633	Units
V _{DS} Drain - Source Voltage ①	200	150	200	150	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	9.0	9.0	8.0	8.0	A
I _D @ T _C = 100°C Continuous Drain Current	6.0	6.0	5.0	5.0	A
I _{DM} Pulsed Drain Current ③	36	36	32	32	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	75			(See Fig. 14)	W
Linear Derating Factor	0.6			(See Fig. 14)	W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	36	36	32	32	
T _J T _{stg} Operating Junction and Storage Temperature Range	-55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C




ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN630 UFN632	200	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN631 UFN633	150	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN630 UFN631	9.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN632 UFN633	8.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN630 UFN631	—	0.25	0.4	Ω	V _{GS} = 10V, I _D = 5.0A	
	UFN632 UFN633	—	0.4	0.6	Ω		
g _{fs} Forward Transconductance ②	ALL	3.0	4.8	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 5.0A	
C _{iss} Input Capacitance	ALL	—	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	250	450	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	80	150	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 90V, I _D = 5.0A, Z _o = 15Ω See Fig. 17	
t _r Rise Time	ALL	—	—	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	50	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	—	40	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	V _{GS} = 10V, I _D = 12A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	10	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN630 UFN631	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.			
		UFN632 UFN633	—	—	8.0	A				
I_{SM}	Pulse Source Current (Body Diode) ③	UFN630 UFN631	—	—	36	A				
		UFN632 UFN633	—	—	32	A				
V_{SD}	Diode Forward Voltage ②	UFN630 UFN631	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 9.0\text{A}, V_{GS} = 0\text{V}$			
		UFN632 UFN633	—	—	1.8	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0\text{V}$			
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$			
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 9.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$			
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.							

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

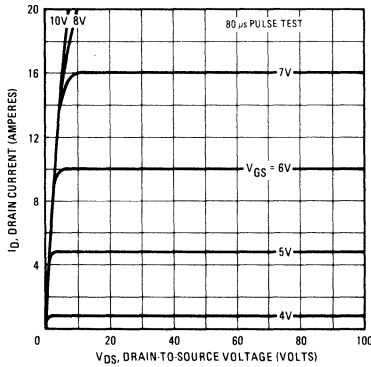


Fig. 2 – Typical Transfer Characteristics

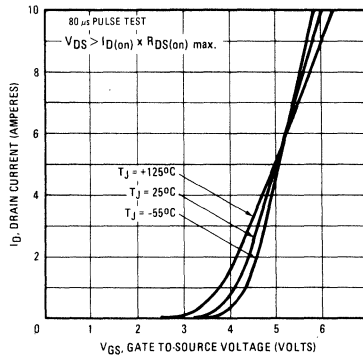


Fig. 3 – Typical Saturation Characteristics

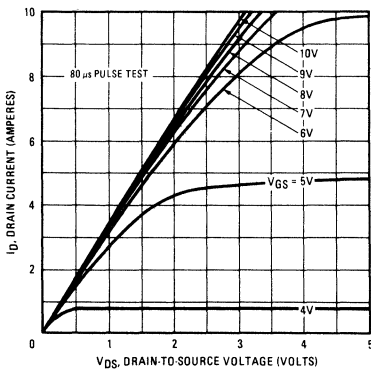


Fig. 4 – Maximum Safe Operating Area

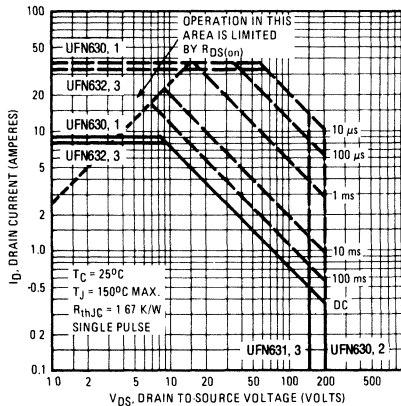
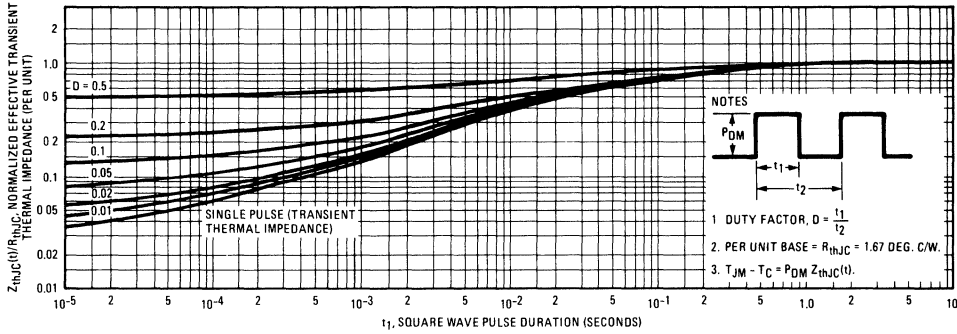


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 — Typical Transconductance Vs. Drain Current

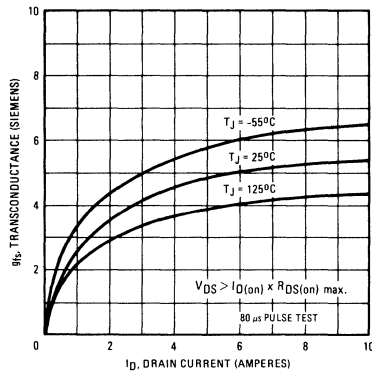


Fig. 7 — Typical Source-Drain Diode Forward Voltage

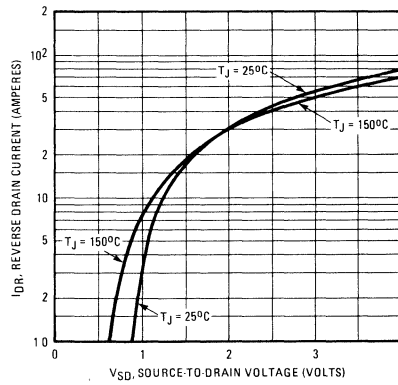


Fig. 8 — Breakdown Voltage Vs. Temperature

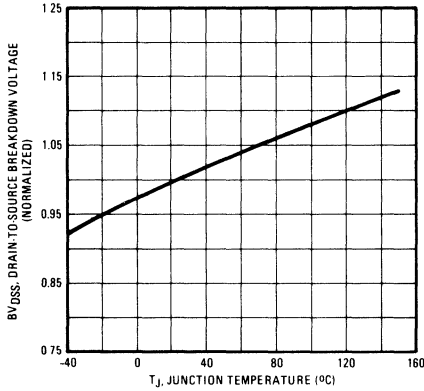


Fig. 9 — Normalized On-Resistance Vs. Temperature

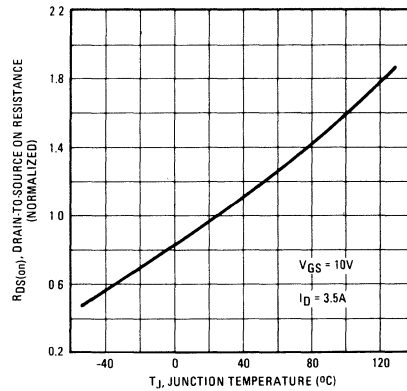


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

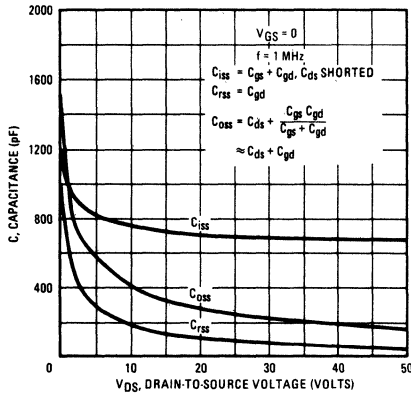


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

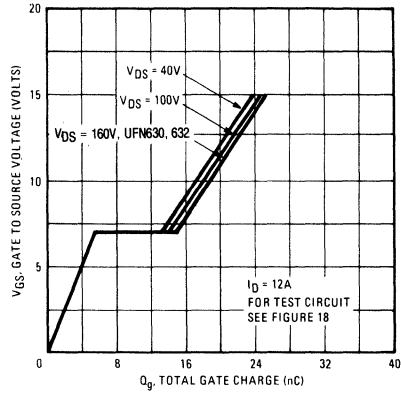


Fig. 12 – Typical On-Resistance Vs. Drain Current

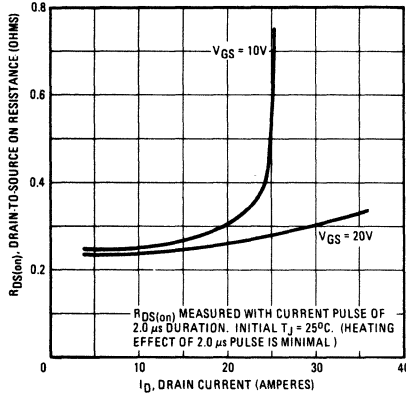


Fig. 13 – Maximum Drain Current Vs. Case Temperature

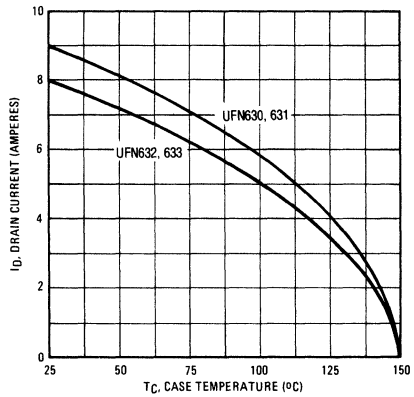


Fig. 14 – Power Vs. Temperature Derating Curve

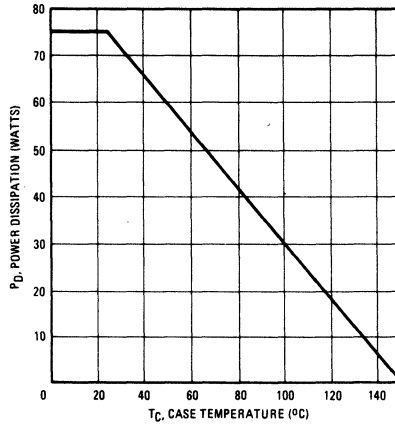


Fig. 15 – Clamped Inductive Test Circuit

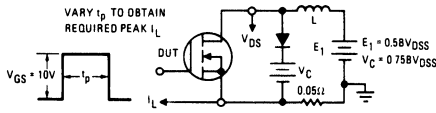


Fig. 16 – Clamped Inductive Waveforms

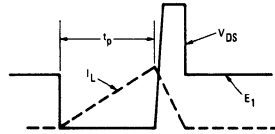


Fig. 17 – Switching Time Test Circuit

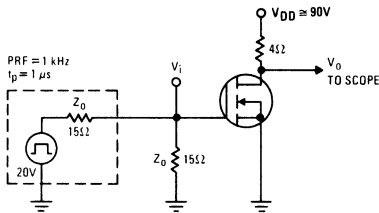
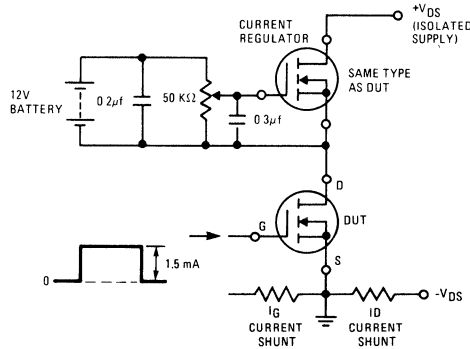


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.2 Ohm N-Channel

UFN640
UFN641
UFN642
UFN643

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

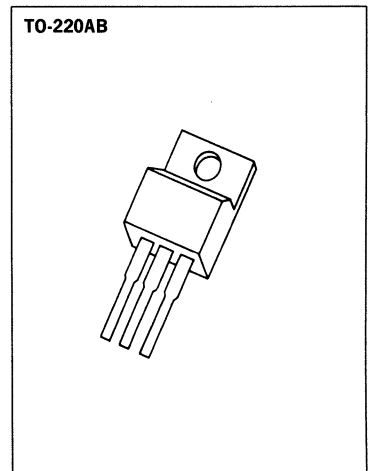
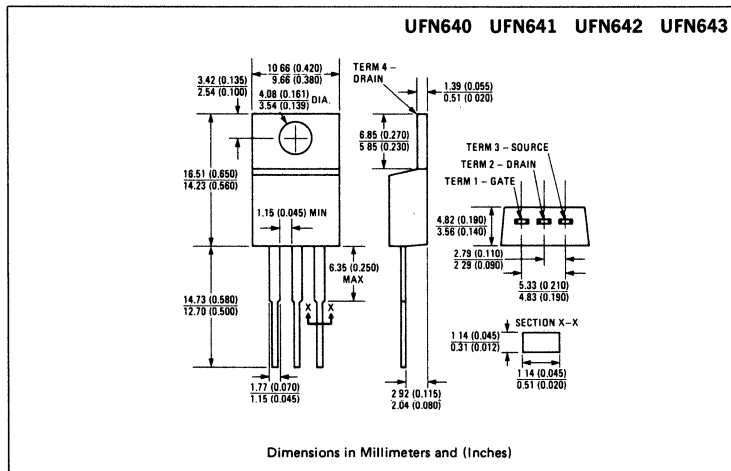
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN640	200V	0.18 Ω	18A
UFN641	150V	0.18 Ω	18A
UFN642	200V	0.22 Ω	16A
UFN643	150V	0.22 Ω	16A

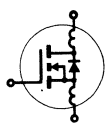
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN640	UFN641	UFN642	UFN643	Units
V _{DS} Drain - Source Voltage ①	200	150	200	150	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	200	150	200	150	V
I _D @ T _C = 25°C Continuous Drain Current	18	18	16	16	A
I _D @ T _C = 100°C Continuous Drain Current	11	11	10	10	A
I _{DM} Pulsed Drain Current ③	72	72	64	64	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125			(See Fig. 14)	W
Linear Derating Factor	1.0			(See Fig. 14)	W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150°C				°C
T _{stg} Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN640 UFN642	200	—	—	V	V _{GS} = 0V	
	UFN641 UFN643	150	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN640 UFN641	18	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN642 UFN643	16	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN640 UFN641	—	0.14	0.18	Ω	V _{GS} = 10V, I _D = 10A	
	UFN642 UFN643	—	0.20	0.22	Ω		
g _{fs} Forward Transconductance ②	ALL	6.0	10	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 10A	
C _{iss} Input Capacitance	ALL	—	1275	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	500	750	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	160	300	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	16	30	ns	V _{DD} = 75V, I _D = 10A, Z ₀ = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	27	60	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	40	80	ns		
t _f Fall Time	ALL	—	31	60	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V _{GS} = 10V, I _D = 22A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	16	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	27	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN640	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN642 UFN643	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN640 UFN641	—	—	72	A	
		UFN642 UFN643	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	UFN640 UFN641	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 18\text{A}, V_{GS} = 0\text{V}$
		UFN642 UFN643	—	—	1.9	V	$T_C = 25^\circ\text{C}, I_S = 16\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	$T_J = 150^\circ\text{C}, I_F = 18\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 18\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

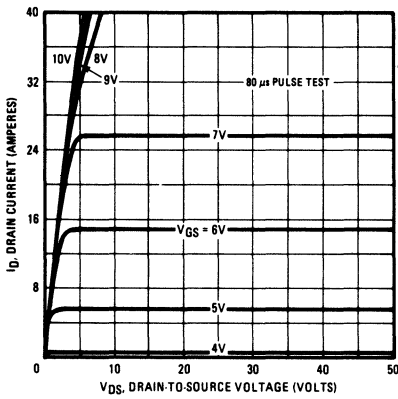


Fig. 2 – Typical Transfer Characteristics

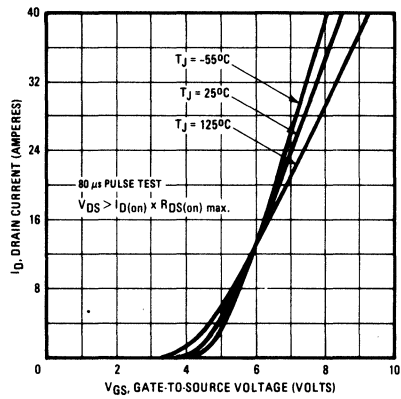


Fig. 3 – Typical Saturation Characteristics

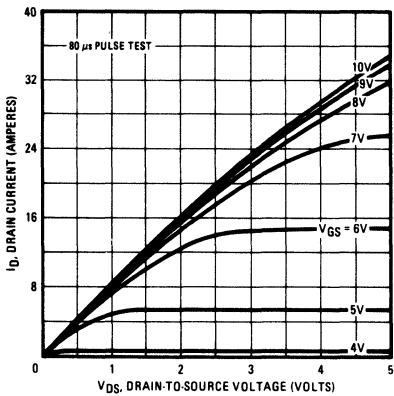


Fig. 4 – Maximum Safe Operating Area

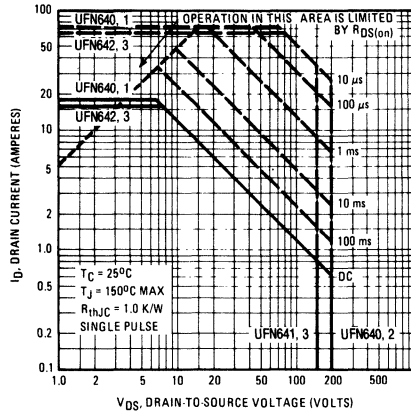
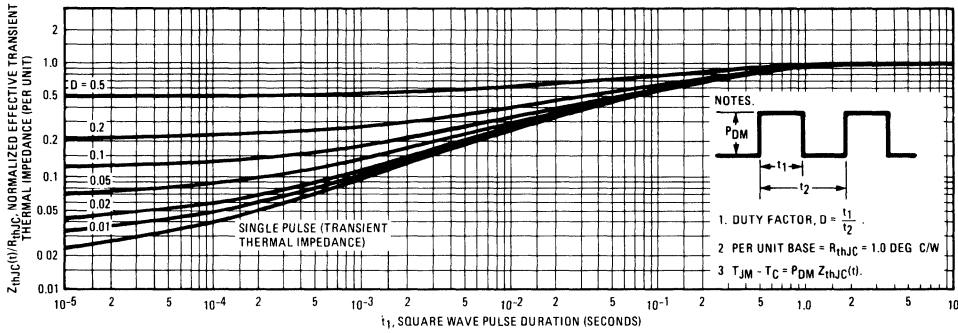


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

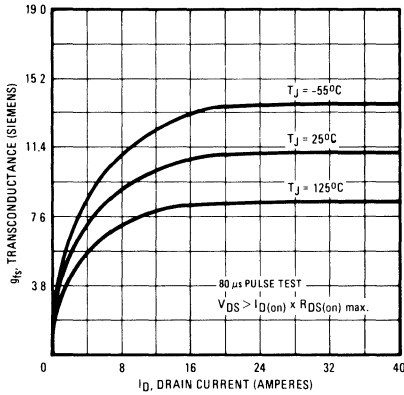


Fig. 7 – Typical Source-Drain Diode Forward Voltage

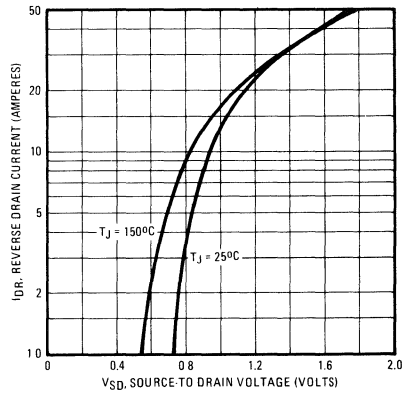


Fig. 8 – Breakdown Voltage Vs. Temperature

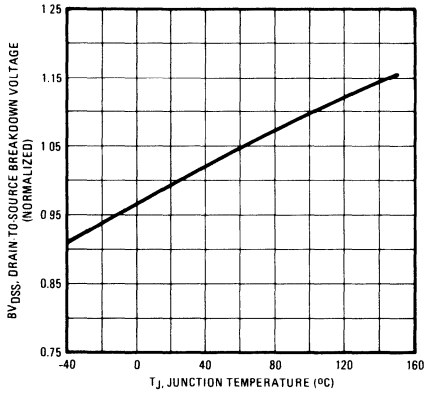


Fig. 9 – Normalized On-Resistance Vs. Temperature

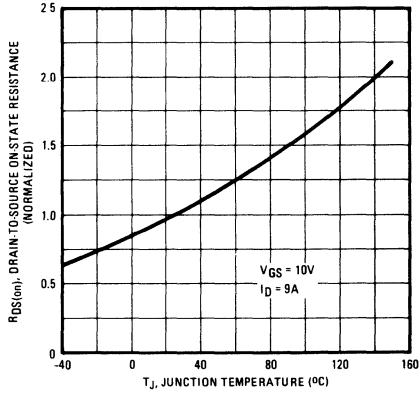


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

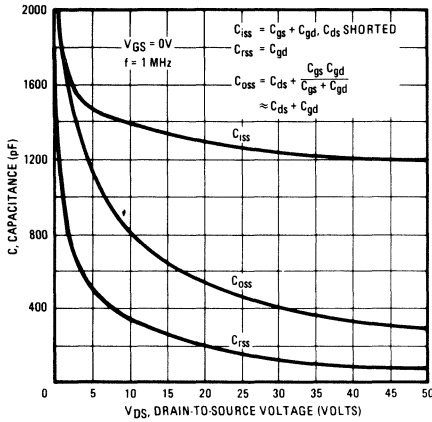


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

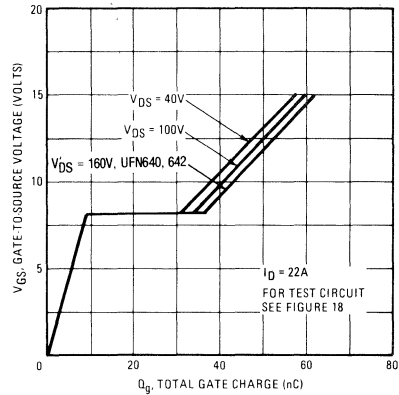


Fig. 12 – Typical On-Resistance Vs. Drain Current

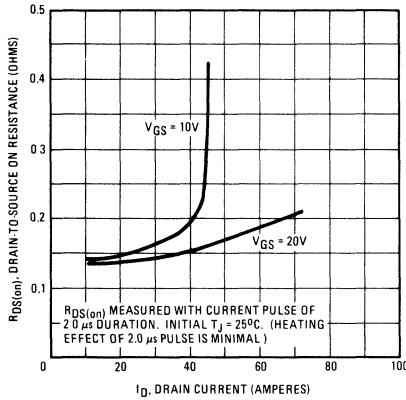


Fig. 13 – Maximum Drain Current Vs. Case Temperature

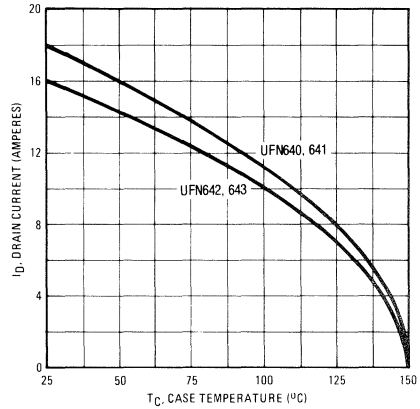


Fig. 14 – Power Vs. Temperature Derating Curve

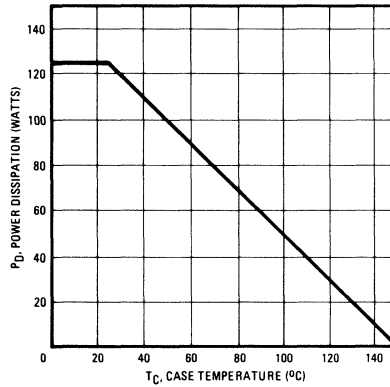


Fig. 15 — Clamped Inductive Test Circuit

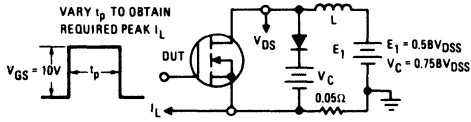


Fig. 16 — Clamped Inductive Waveforms

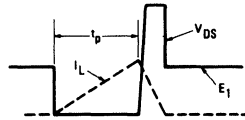


Fig. 17 — Switching Time Test Circuit

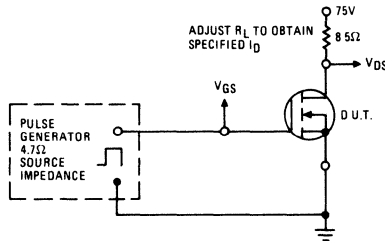
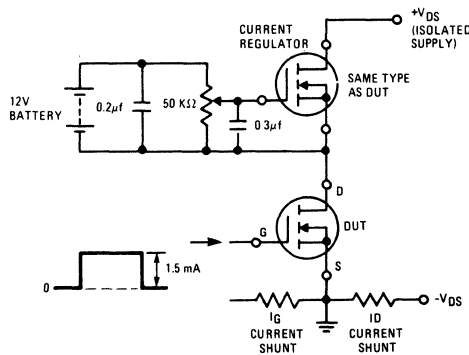


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 3.6 Ohm
N-Channel

UFN710
UFN711
UFN712
UFN713

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

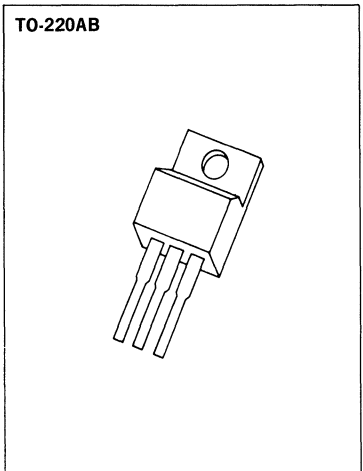
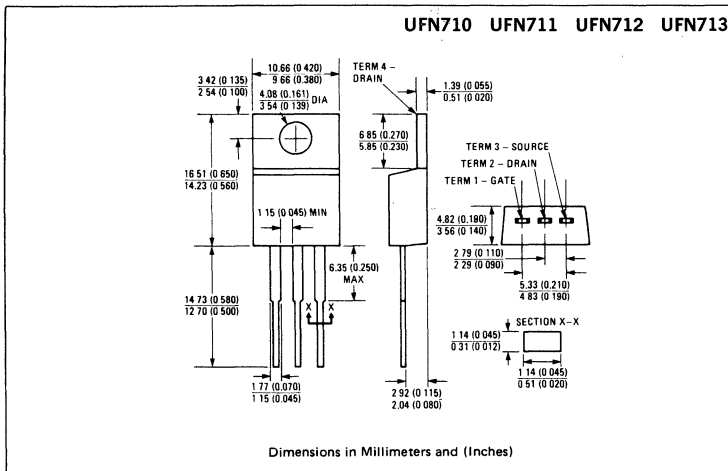
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN710	400V	3.6 Ω	1.5A
UFN711	350V	3.6 Ω	1.5A
UFN712	400V	5.0 Ω	1.3A
UFN713	350V	5.0 Ω	1.3A

MECHANICAL SPECIFICATIONS

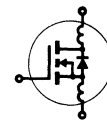


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN710	UFN711	UFN712	UFN713	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	1.5	1.5	1.3	1.3	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM} Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS} Gate - Source Voltage					± 20
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20				(See Fig. 14)
Linear Derating Factor	0.16				(See Fig. 14)
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				
	6.0	6.0	5.0	5.0	A
T_J T_{stg} Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS} Drain - Source Breakdown Voltage	UFN710 UFN712	400	—	—	V	$V_{GS} = 0\text{V}$	
	UFN711 UFN713	350	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	UFN710 UFN711	1.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	UFN712 UFN713	1.3	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN710 UFN711	—	3.3	3.6	Ω	$V_{GS} = 10\text{V}$, $I_D = 0.8\text{A}$	
	UFN712 UFN713	—	3.6	5.0	Ω		
g_{fs} Forward Transconductance ②	ALL	0.5	1.2	—	S (③)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 0.8\text{A}$	
C_{iss} Input Capacitance	ALL	—	135	150	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0 \text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	35	50	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	8.0	15	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 0.8\text{A}$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r Rise Time	ALL	—	10	20	ns		
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	5.0	10	ns		
t_f Fall Time	ALL	—	8.0	15	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	$V_{GS} = 10\text{V}$, $I_D = 2.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	3.0	—	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC		
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN710 UFN711	—	—	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN712 UFN713	—	—	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN710 UFN711	—	—	6.0	A	
		UFN712 UFN713	—	—	5.0	A	
V_{SD}	Diode Forward Voltage ②	UFN710 UFN711	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 1.5\text{A}, V_{GS} = 0\text{V}$
		UFN712 UFN713	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 1.3\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150^\circ\text{C}, I_F = 1.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 1.5\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

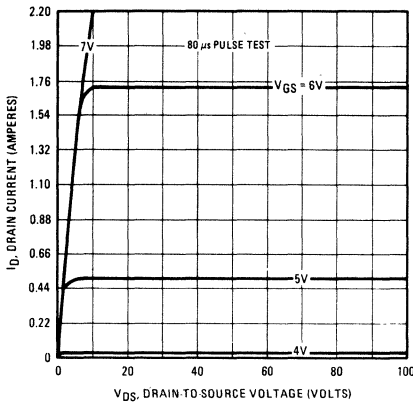


Fig. 2 – Typical Transfer Characteristics

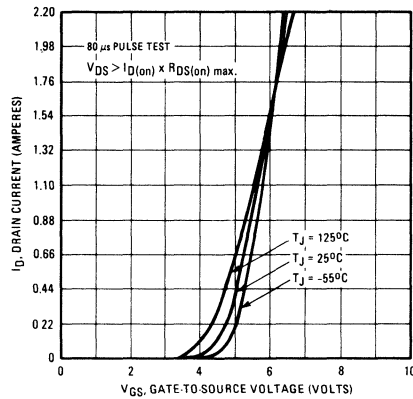


Fig. 3 – Typical Saturation Characteristics

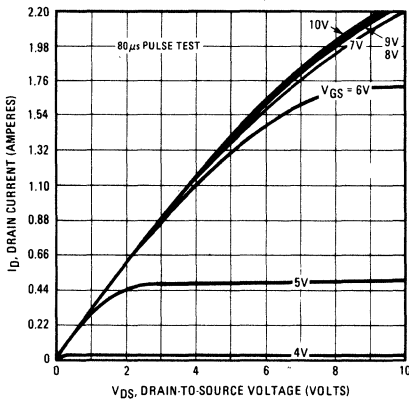


Fig. 4 – Maximum Safe Operating Area

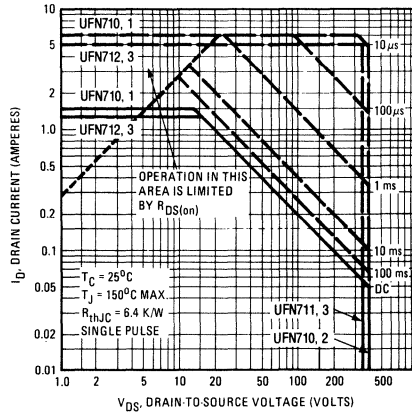


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

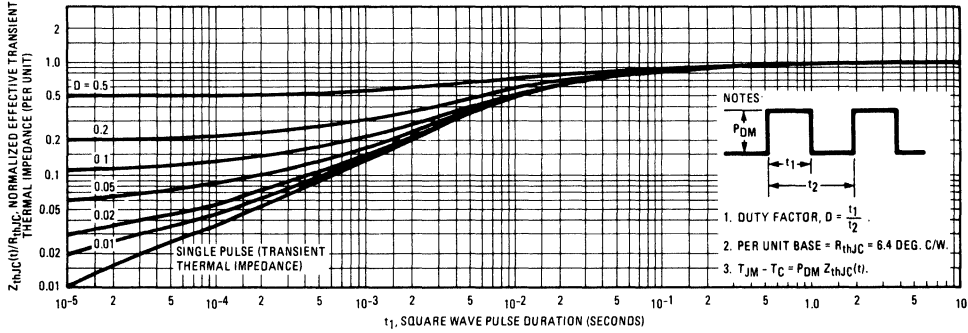


Fig. 6 – Typical Transconductance Vs. Drain Current

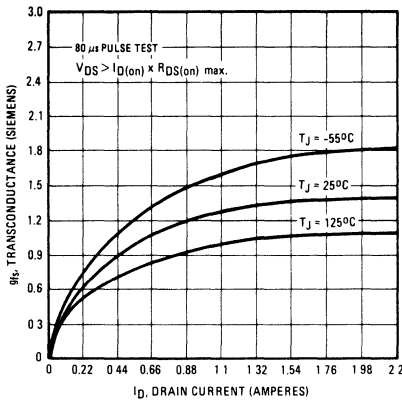


Fig. 7 – Typical Source-Drain Diode Forward Voltage

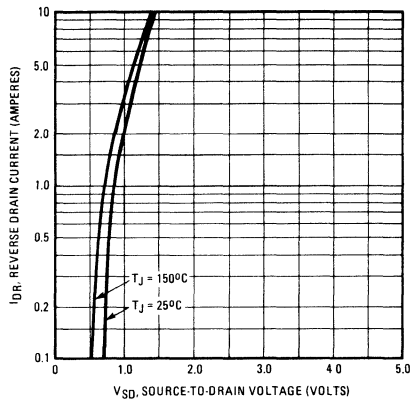


Fig. 8 – Breakdown Voltage Vs. Temperature

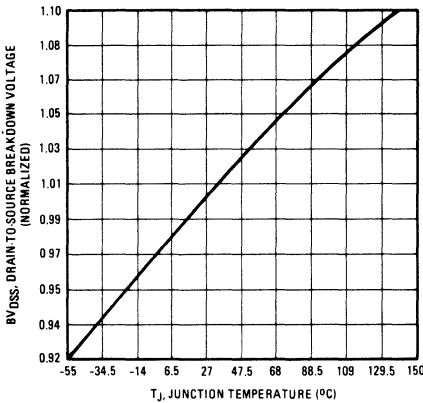


Fig. 9 – Normalized On-Resistance Vs. Temperature

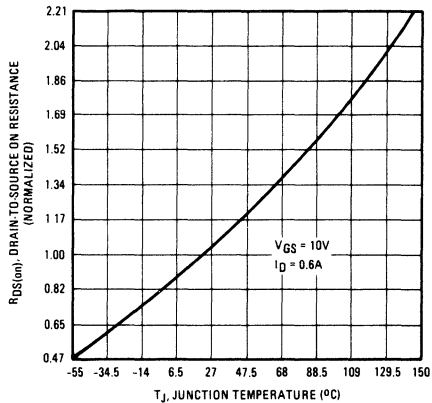


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

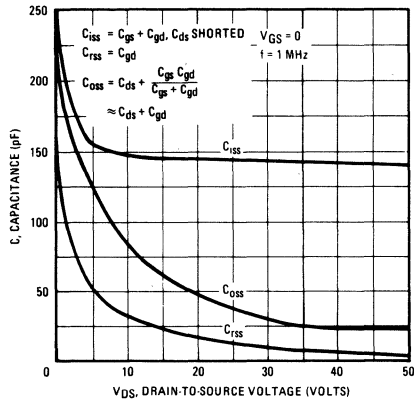


Fig. 12 — Typical On-Resistance Vs. Drain Current

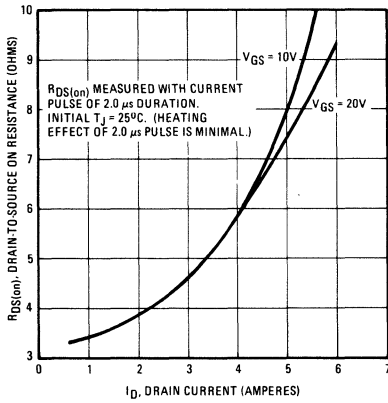


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

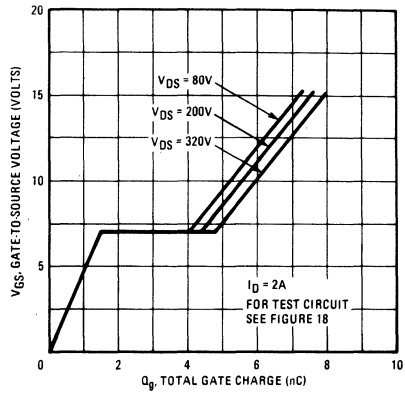


Fig. 13 — Maximum Drain Current Vs. Case Temperature

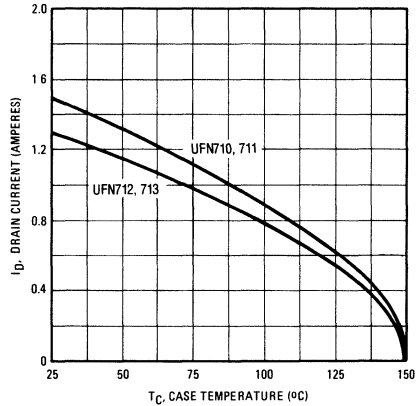


Fig. 14 — Power Vs. Temperature Derating Curve

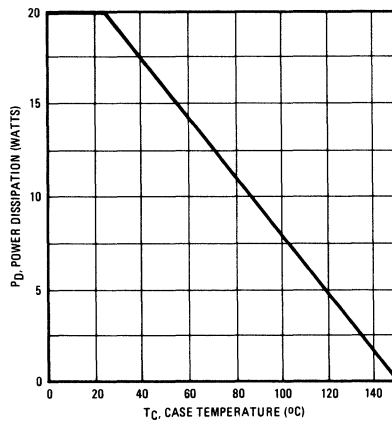


Fig. 15 — Clamped Inductive Test Circuit

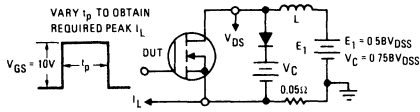


Fig. 16 — Clamped Inductive Waveforms

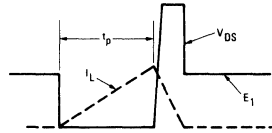


Fig. 17 — Switching Time Test Circuit

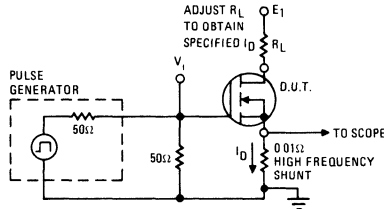
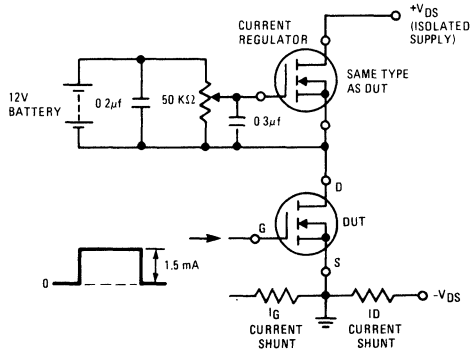


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.8 Ohm
N-Channel

UFN720
UFN721
UFN722
UFN723

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

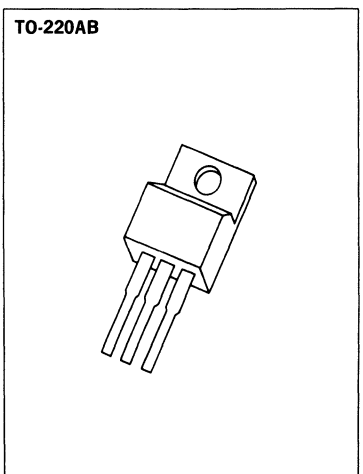
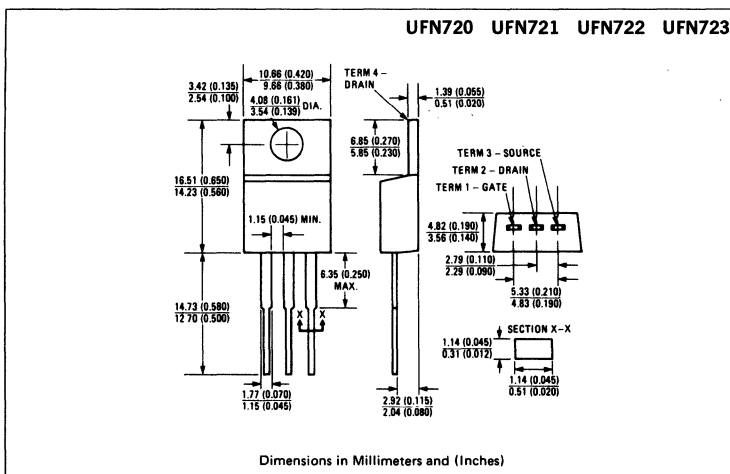
DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance. The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability. These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN720	400V	1.8Ω	3.0A
UFN721	350V	1.8Ω	3.0A
UFN722	400V	2.5Ω	2.5A
UFN723	350V	2.5Ω	2.5A

MECHANICAL SPECIFICATIONS

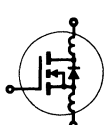


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN720	UFN721	UFN722	UFN723	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	3.0	3.0	2.5	2.5	A
I _D @ T _C = 100°C Continuous Drain Current	2.0	2.0	1.5	1.5	A
I _{DM} Pulsed Drain Current ③	12	12	10	10	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
	12	12	10	10	
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

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ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN720 UFN722	400	—	—	V	V _{GS} = 0V	
	UFN721 UFN723	350	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN720 UFN721	3.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN722 UFN723	2.5	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN720 UFN721	—	1.5	1.8	Ω	V _{GS} = 10V, I _D = 1.5A	
	UFN722 UFN723	—	1.8	2.5	Ω		
g _{fs} Forward Transconductance ②	ALL	1.0	2.0	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 1.5A	
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	100	200	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	20	40	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 1.5A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	25	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	25	50	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V _{GS} = 10V, I _D = 4.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN720 UFN721	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN722 UFN723	—	—	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN720 UFN721	—	—	12	A	
		UFN722 UFN723	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	UFN720 UFN721	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 3.0\text{A}, V_{GS} = 0\text{V}$
		UFN722 UFN723	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

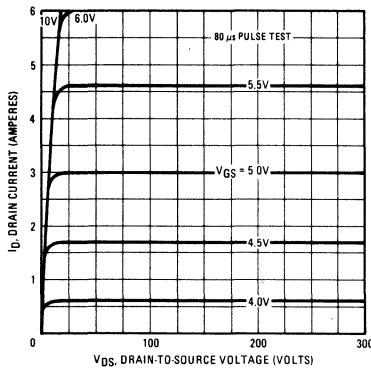


Fig. 2 – Typical Transfer Characteristics

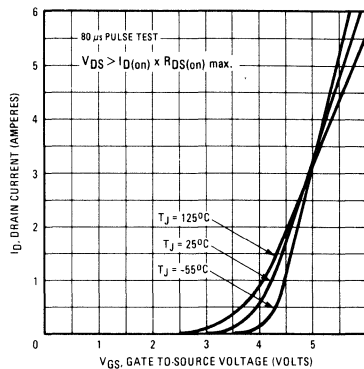


Fig. 3 – Typical Saturation Characteristics

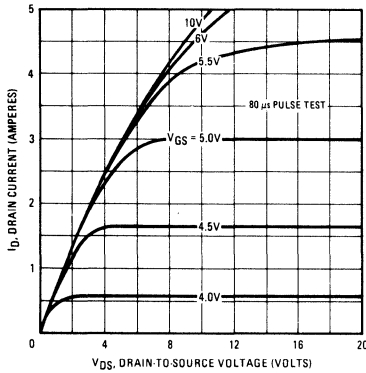


Fig. 4 – Maximum Safe Operating Area

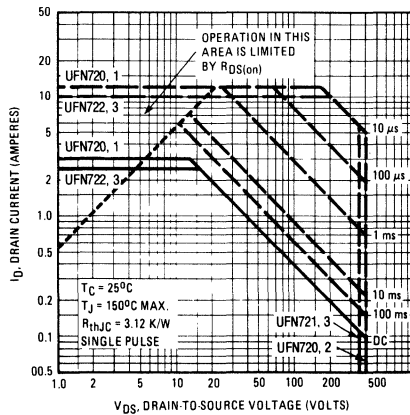
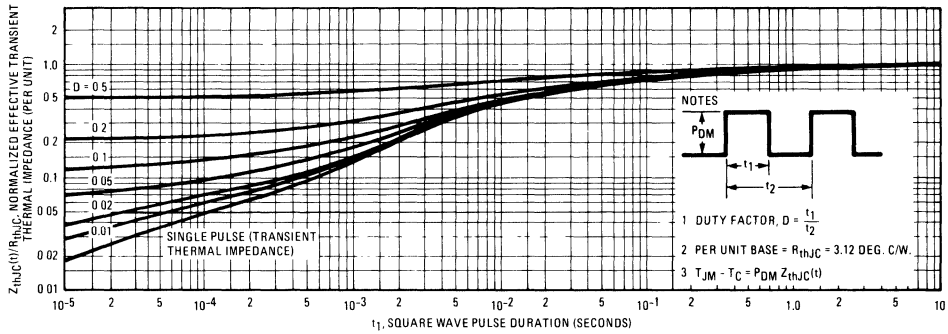


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration



4

Fig. 6 – Typical Transconductance Vs. Drain Current

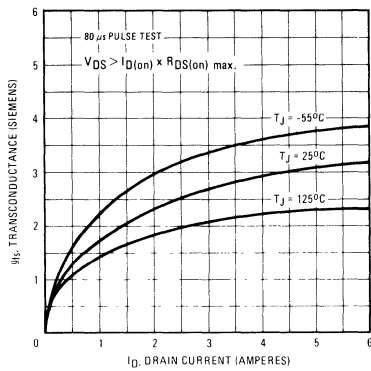


Fig. 7 – Typical Source-Drain Diode Forward Voltage

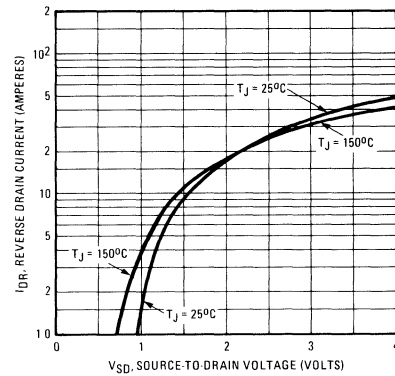


Fig. 8 – Breakdown Voltage Vs. Temperature

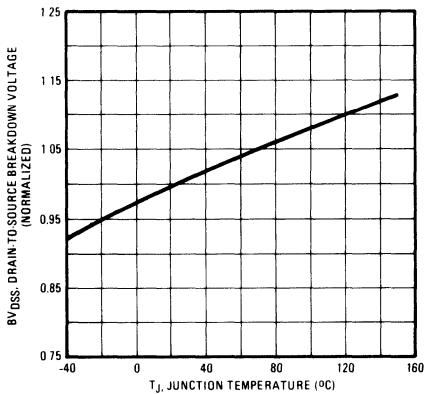


Fig. 9 – Normalized On-Resistance Vs. Temperature

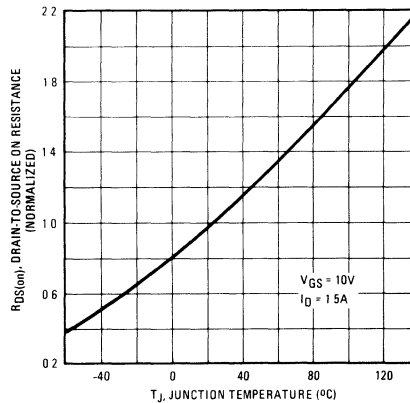


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

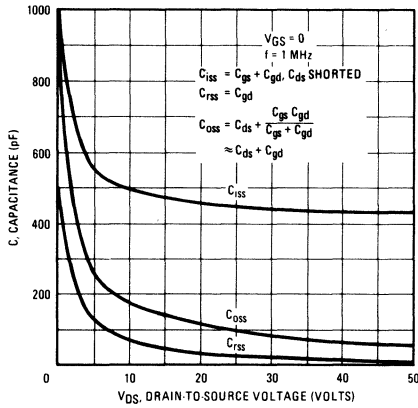


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

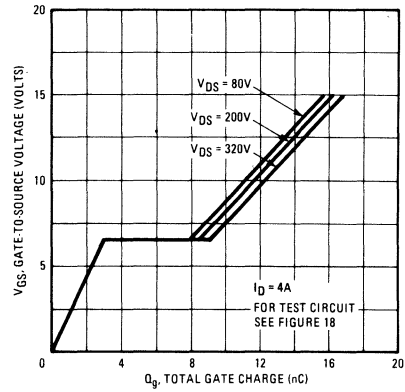


Fig. 12 – Typical On-Resistance Vs. Drain Current

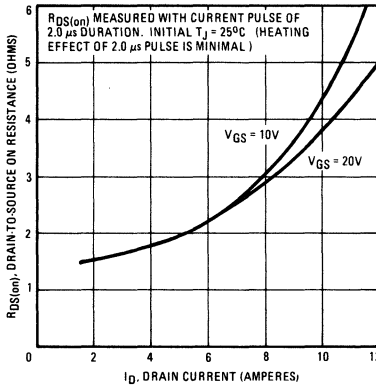


Fig. 13 – Maximum Drain Current Vs. Case Temperature

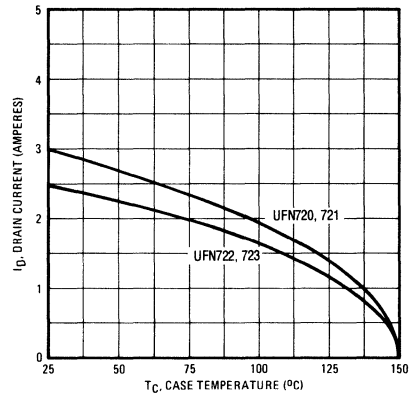


Fig. 14 – Power Vs. Temperature Derating Curve

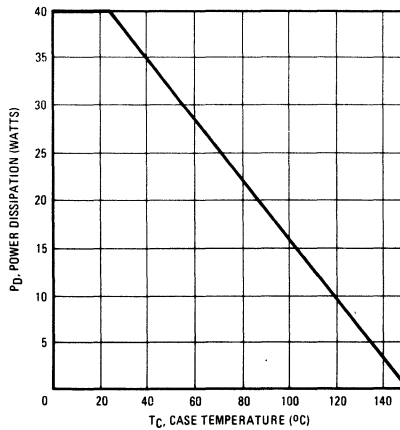


Fig. 15 — Clamped Inductive Test Circuit

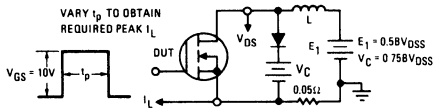


Fig. 16 — Clamped Inductive Waveforms

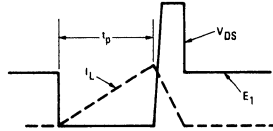


Fig. 17 — Switching Time Test Circuit

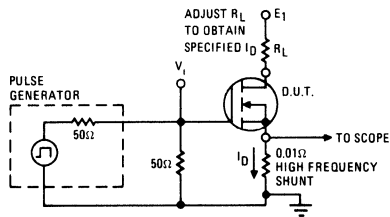
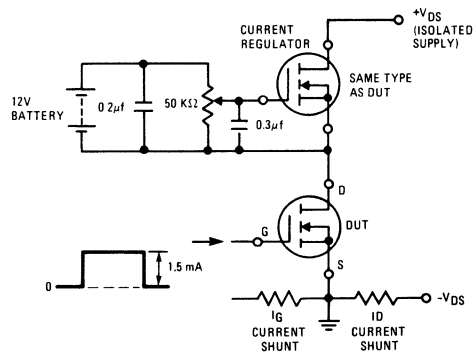


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm N-Channel

UFN730
UFN731
UFN732
UFN733

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

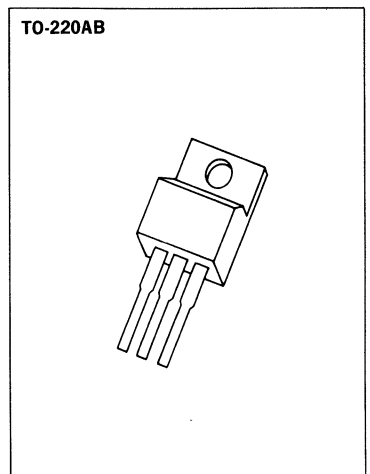
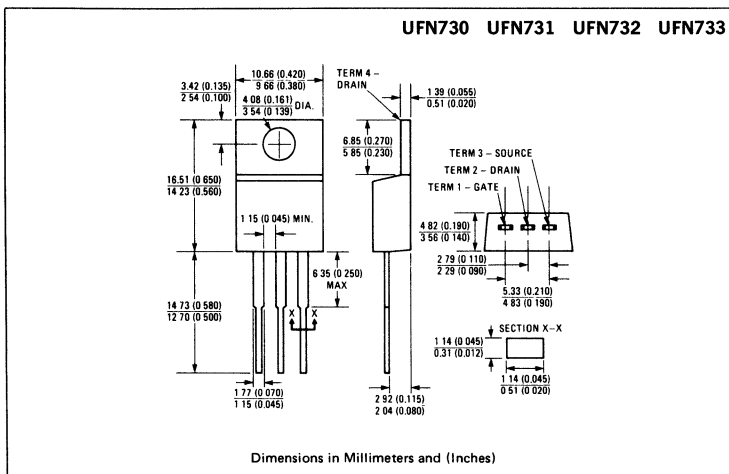
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN730	400V	1.0Ω	5.5A
UFN731	350V	1.0Ω	5.5A
UFN732	400V	1.5Ω	4.5A
UFN733	350V	1.5Ω	4.5A

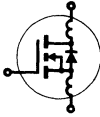
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter		UFN730	UFN731	UFN732	UFN733	Units
V _{DS}	Drain - Source Voltage ①	400	350	400	350	V
V _{DGR}	Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I _D @ T _C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I _{DM}	Pulsed Drain Current ③	22	22	18	18	A
V _{GS}	Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I _{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T _J T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions		
BV _{DSS}	Drain - Source Breakdown Voltage	UFN730 UFN732	400	—	—	V	V _{GS} = 0V	
		UFN731 UFN733	350	—	—	V	I _D = 250μA	
V _{GS(th)}	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
			—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)}	On-State Drain Current ②	UFN730 UFN731	5.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
		UFN732 UFN733	4.5	—	—	A		
R _{DS(on)}	Static Drain-Source On-State Resistance ②	UFN730 UFN731	—	0.8	1.0	Ω	V _{GS} = 10V, I _D = 3.0A	
		UFN732 UFN733	—	1.0	1.5	Ω		
g _{fs}	Forward Transconductance ②	ALL	3.0	4.0	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 3.0A	
C _{iss}	Input Capacitance	ALL	—	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss}	Output Capacitance	ALL	—	150	300	pF		
C _{rss}	Reverse Transfer Capacitance	ALL	—	40	80	pF		
t _{d(on)}	Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 175V, I _D = 3.0A, Z ₀ = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r	Rise Time	ALL	—	—	35	ns		
t _{d(off)}	Turn-Off Delay Time	ALL	—	—	55	ns		
t _f	Fall Time	ALL	—	—	35	ns		
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs}	Gate-Source Charge	ALL	—	11	—	nC		
Q _{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC		
L _D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R _{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN730 UFN731	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN732 UFN733	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN730 UFN731	—	—	22	A	
		UFN732 UFN733	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	UFN730 UFN731	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 5.5\text{A}, V_{GS} = 0\text{V}$
		UFN732 UFN733	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 4.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 5.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $I_S + I_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

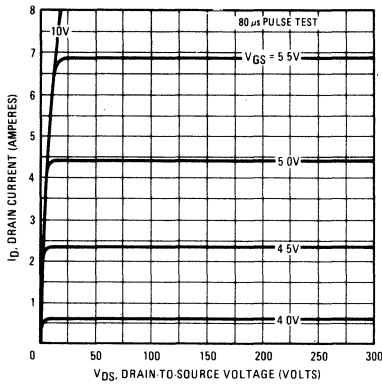


Fig. 2 – Typical Transfer Characteristics

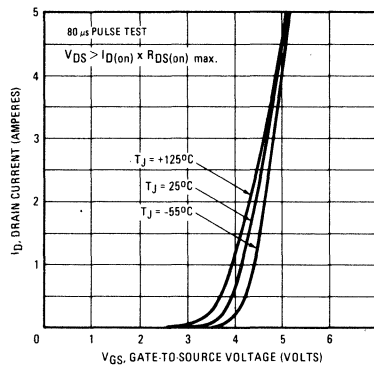


Fig. 3 – Typical Saturation Characteristics

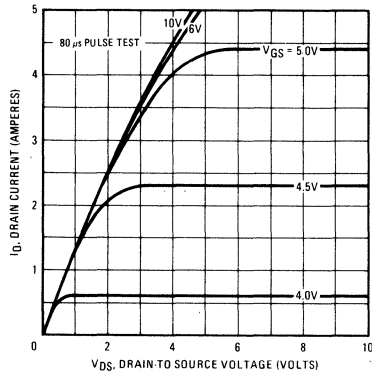


Fig. 4 – Maximum Safe Operating Area

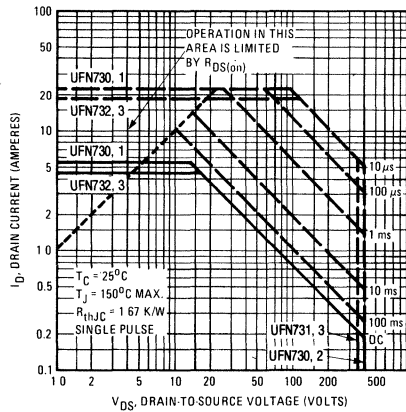


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

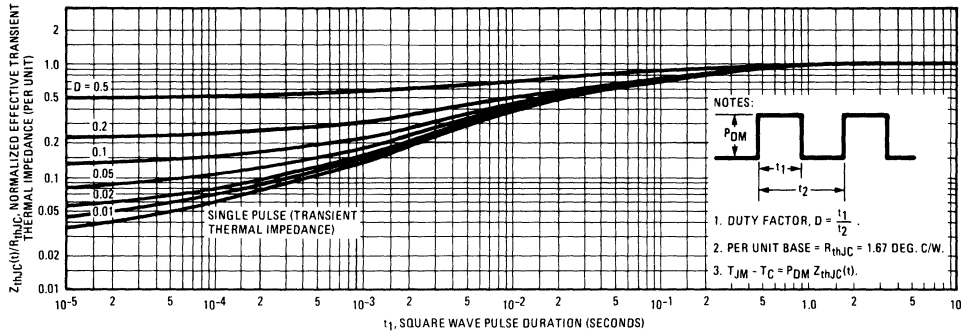


Fig. 6 — Typical Transconductance Vs. Drain Current

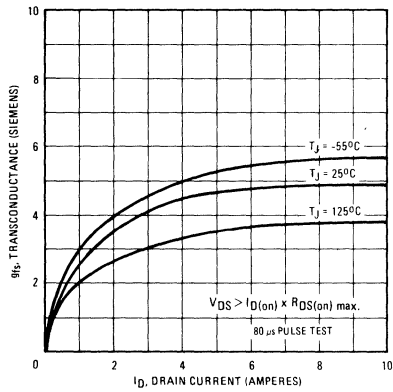


Fig. 7 — Typical Source-Drain Diode Forward Voltage

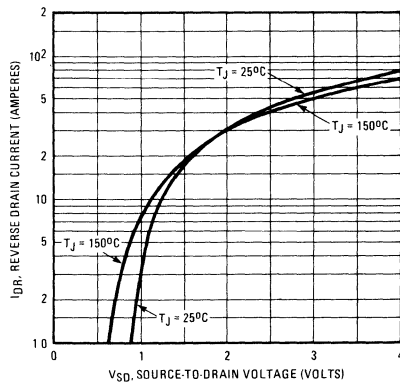


Fig. 8 — Breakdown Voltage Vs. Temperature

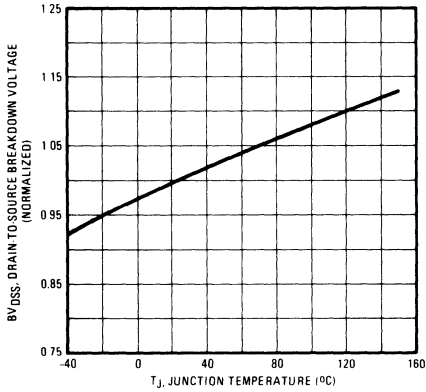


Fig. 9 — Normalized On-Resistance Vs. Temperature

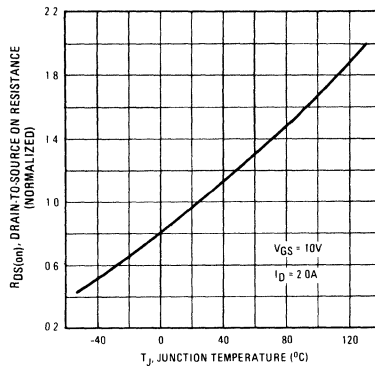


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

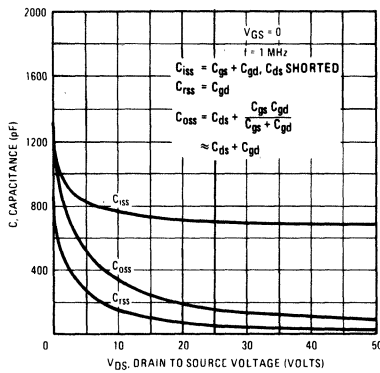


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

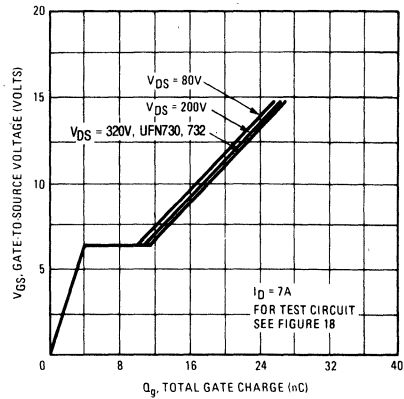


Fig. 12 — Typical On-Resistance Vs. Drain Current

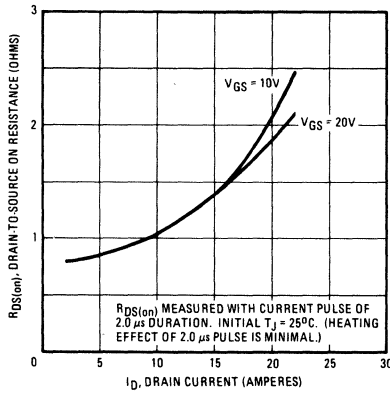


Fig. 13 — Maximum Drain Current Vs. Case Temperature

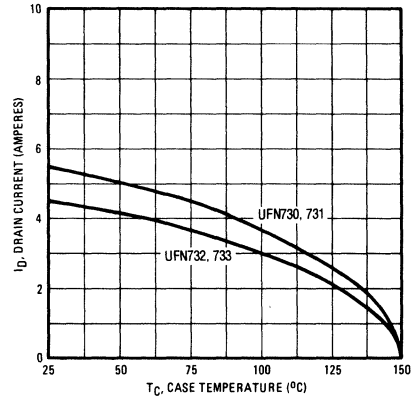


Fig. 14 — Power Vs. Temperature Derating Curve

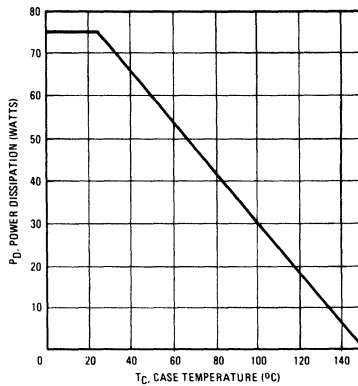


Fig. 15 — Clamped Inductive Test Circuit

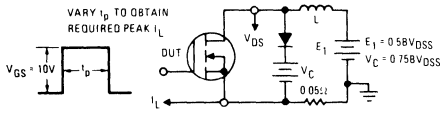


Fig. 16 — Clamped Inductive Waveforms

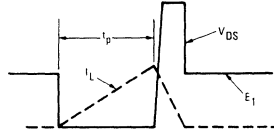


Fig. 17 — Switching Time Test Circuit

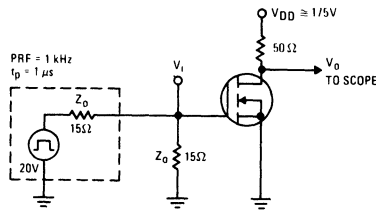
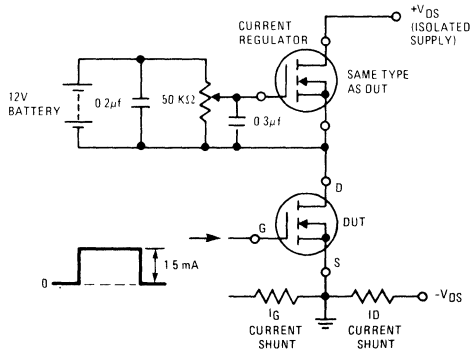


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 0.55 Ohm
N-Channel

UFN740
UFN741
UFN742
UFN743

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

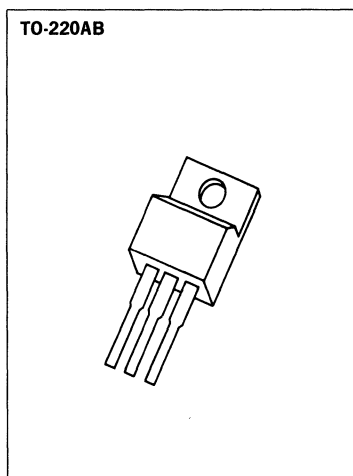
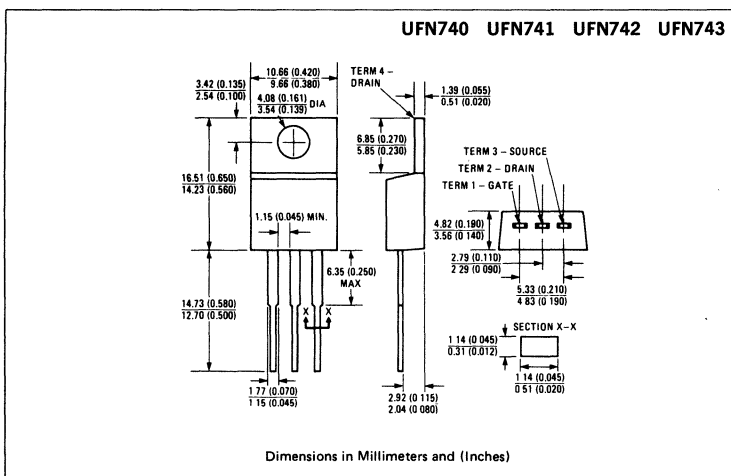
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN740	400V	0.55Ω	10A
UFN741	350V	0.55Ω	10A
UFN742	400V	0.80Ω	8.0A
UFN743	350V	0.80Ω	8.0A

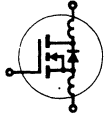
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	UFN740	UFN741	UFN742	UFN743	Units
V _{DS} Drain - Source Voltage ①	400	350	400	350	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	400	350	400	350	V
I _D @ T _C = 25°C Continuous Drain Current	10	10	8.0	8.0	A
I _D @ T _C = 100°C Continuous Drain Current	6.0	6.0	5.0	5.0	A
I _{DM} Pulsed Drain Current ③	40	40	32	32	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	40 (See Fig. 15 and 16) L = 100μH				A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN740 UFN742	400	—	—	V	V _{GS} = 0V	
	UFN741 UFN743	350	—	—	V	I _D = 250μA	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	UFN740 UFN741	10	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V	
	UFN742 UFN743	8.0	—	—	A		
	UFN740 UFN741	—	0.47	0.55	Ω		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN742 UFN743	—	.68	.80	Ω	V _{GS} = 10V, I _D = 5.0A	
	ALL	4.0	7.0	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 5.0A	
C _{iss} Input Capacitance	ALL	—	1250	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	300	450	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	80	150	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	17	35	ns	V _{DD} = 175V, I _D = 5.0A, Z ₀ = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	5.0	15	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	45	90	ns		
t _f Fall Time	ALL	—	16	35	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC		V _{GS} = 10V, I _D = 12A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	18	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	23	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN740	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN741	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN742	—	—	40	A	
		UFN743	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	UFN740	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 10\text{A}, V_{GS} = 0\text{V}$
		UFN741	—	—	1.9	V	
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 10\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 10\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

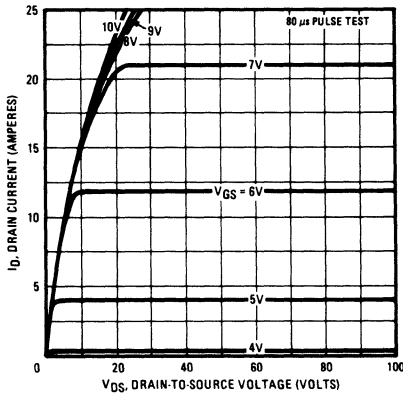


Fig. 2 – Typical Transfer Characteristics

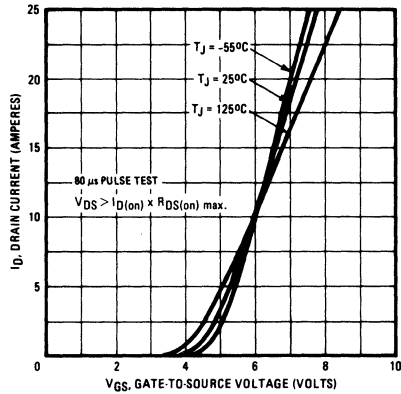


Fig. 3 – Typical Saturation Characteristics

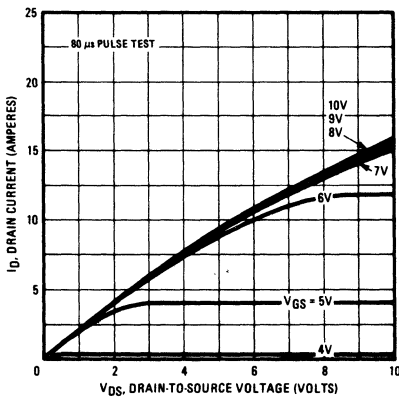


Fig. 4 – Maximum Safe Operating Area

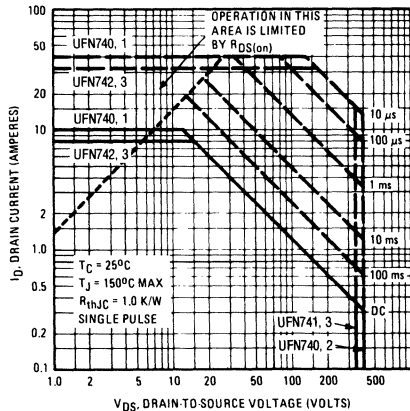


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

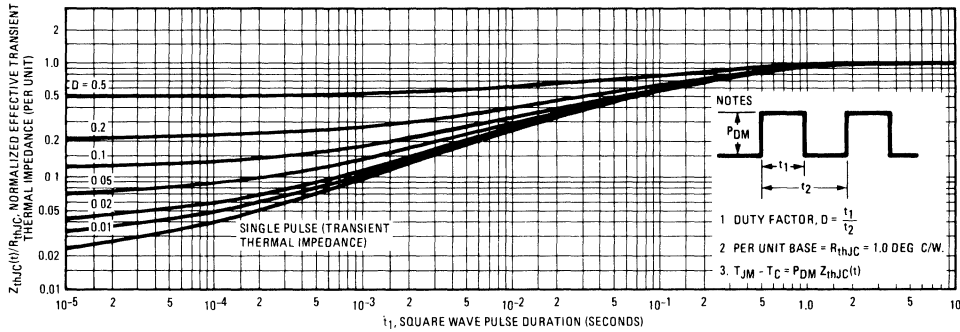


Fig. 6 — Typical Transconductance Vs. Drain Current

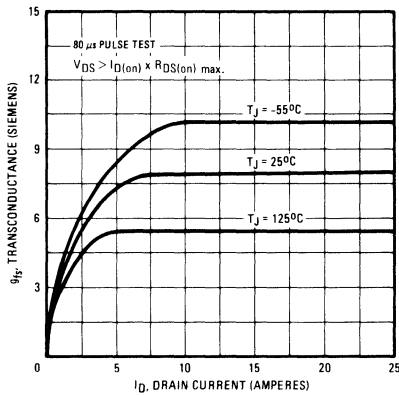


Fig. 7 — Typical Source-Drain Diode Forward Voltage

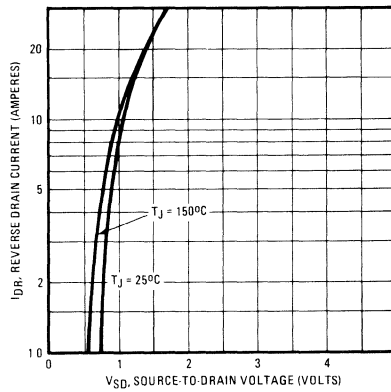


Fig. 8 — Breakdown Voltage Vs. Temperature

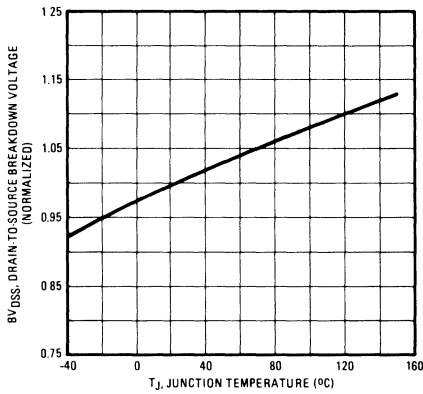


Fig. 9 — Normalized On-Resistance Vs. Temperature

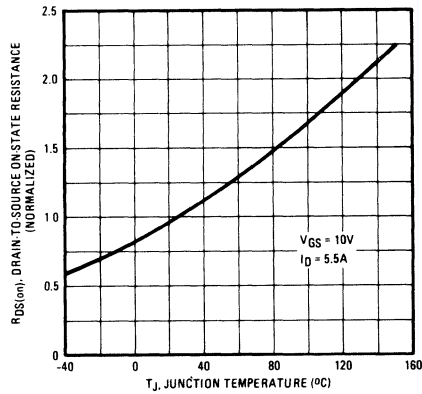


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

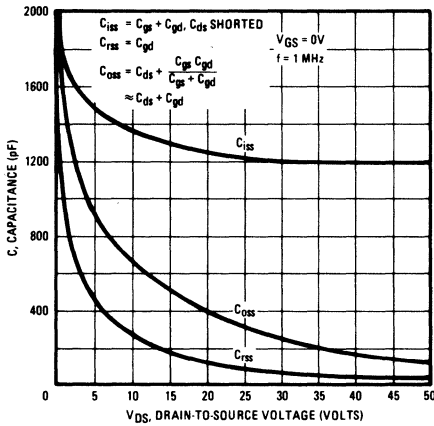


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

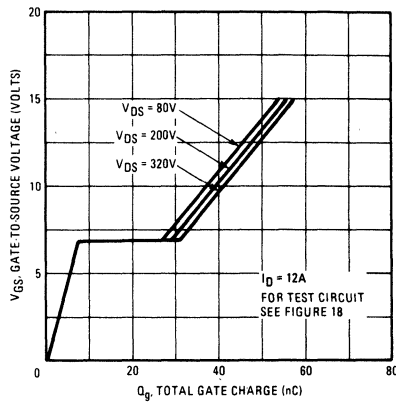


Fig. 12 – Typical On-Resistance Vs. Drain Current

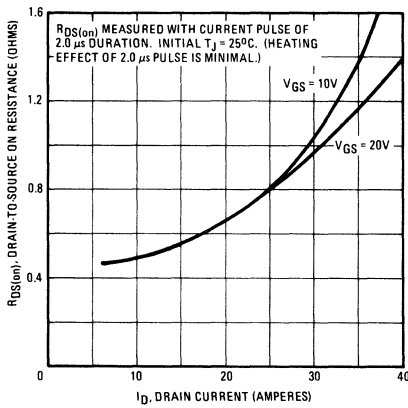


Fig. 13 – Maximum Drain Current Vs. Case Temperature

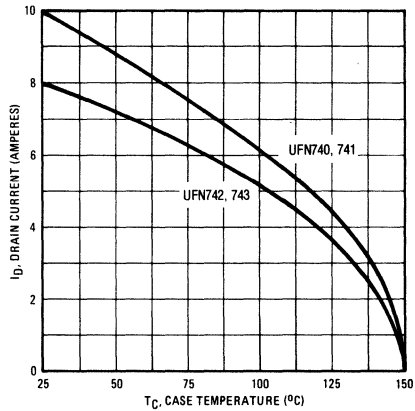


Fig. 14 – Power Vs. Temperature Derating Curve

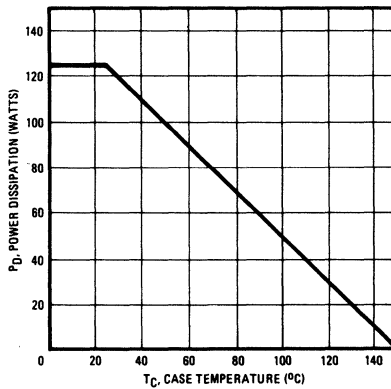


Fig. 15 — Clamped Inductive Test Circuit

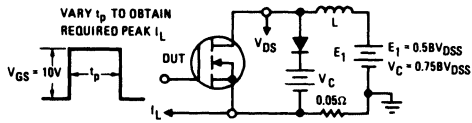


Fig. 16 — Clamped Inductive Waveforms

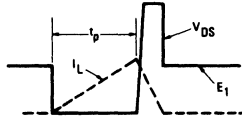


Fig. 17 — Switching Time Test Circuit

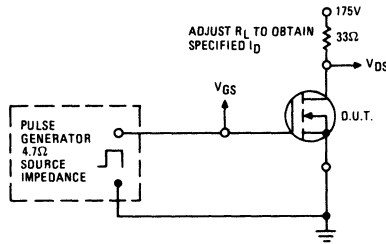
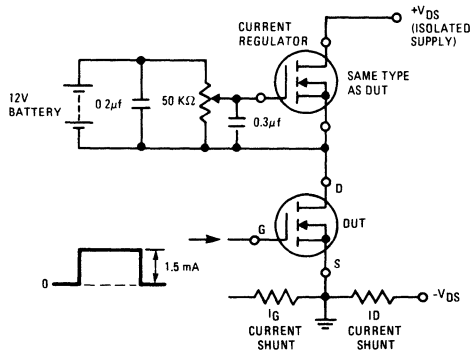


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 3.0 Ohm
N-Channel

UFN820
UFN821
UFN822
UFN823

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

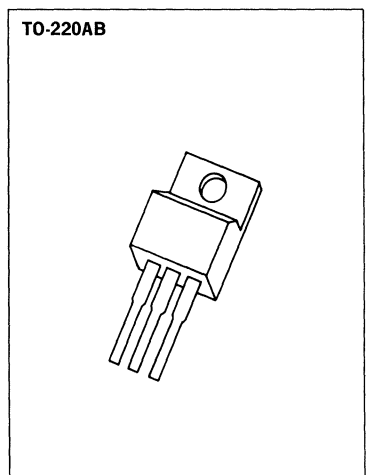
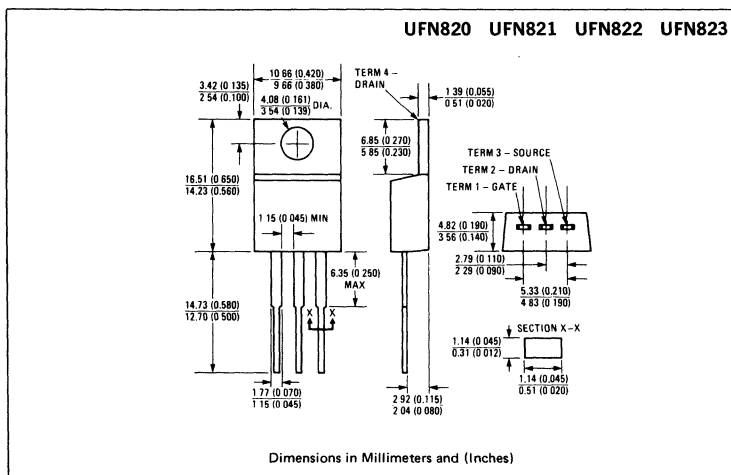
The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN820	500V	3.0Ω	2.5A
UFN821	450V	3.0Ω	2.5A
UFN822	500V	4.0Ω	2.0A
UFN823	450V	4.0Ω	2.0A

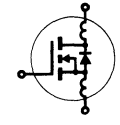
MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter		UFN820	UFN821	UFN822	UFN823	Units
V _{DS}	Drain - Source Voltage ①	500	450	500	450	V
V _{DGR}	Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	500	450	500	450	V
I _D @ T _C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I _D @ T _C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I _{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V _{GS}	Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I _{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T _J T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions		
BV _{DSS}	Drain - Source Breakdown Voltage	UFN820 UFN822	500	—	—	V	V _{GS} = 0V I _D = 250μA	
		UFN821 UFN823	450	—	—	V		
V _{GS(th)}	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
			—	—	1000	μA		
I _{D(on)}	On-State Drain Current ②	UFN820 UFN821	2.5	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
		UFN822 UFN823	2.0	—	—	A		
R _{DS(on)}	Static Drain-Source On-State Resistance ②	UFN820 UFN821	—	2.5	3.0	Ω	V _{GS} = 10V, I _D = 1.0A	
		UFN822 UFN823	—	3.0	4.0	Ω		
		ALL	—	—	—	—		
g _{fs}	Forward Transconductance ②	ALL	1.0	1.75	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 1.0A	
C _{iss}	Input Capacitance	ALL	—	300	400	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss}	Output Capacitance	ALL	—	75	150	pF		
C _{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF		
t _{d(on)}	Turn-On Delay Time	ALL	—	30	60	ns	V _{DD} = 0.5 BV _{DSS} ; I _D = 1.0A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r	Rise Time	ALL	—	25	50	ns		
t _{d(off)}	Turn-Off Delay Time	ALL	—	30	60	ns		
t _f	Fall Time	ALL	—	15	30	ns		
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V _{GS} = 10V, I _D = 3.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs}	Gate-Source Charge	ALL	—	5.0	—	nC		
Q _{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC		
L _D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
			—	4.5	—	nH		
L _S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R _{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased.
R _{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN820	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN822	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN820	—	—	10	A	
		UFN822	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFN820	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 2.5\text{A}, V_{GS} = 0\text{V}$
		UFN822	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 2.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 2.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

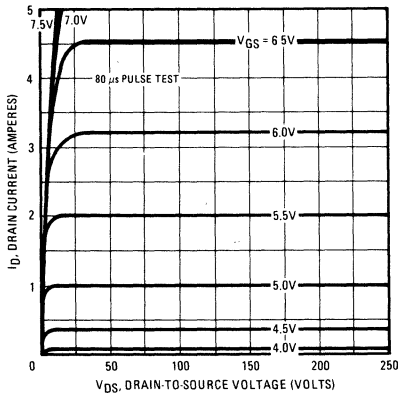


Fig. 2 – Typical Transfer Characteristics

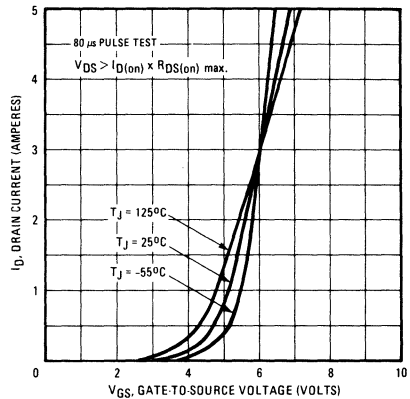


Fig. 3 – Typical Saturation Characteristics

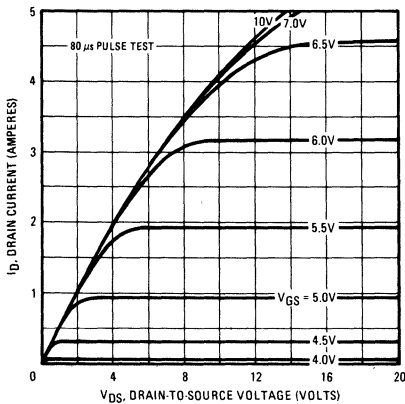


Fig. 4 – Maximum Safe Operating Area

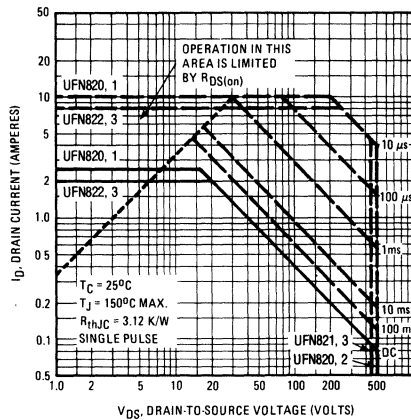


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

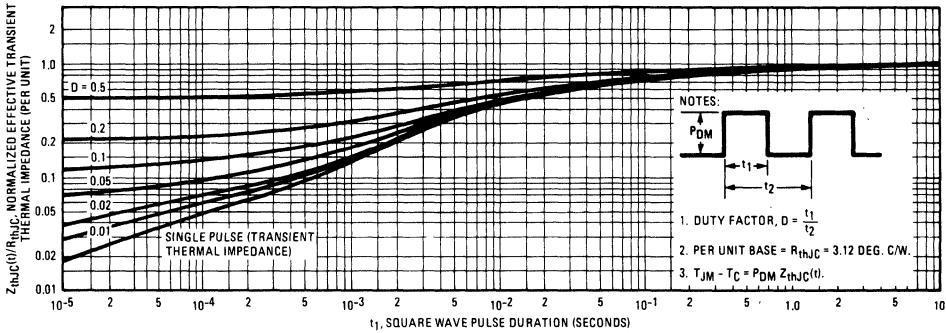


Fig. 6 – Typical Transconductance Vs. Drain Current

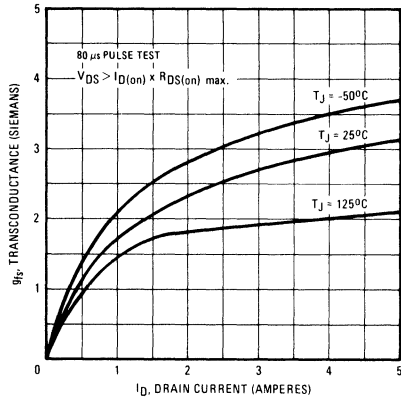


Fig. 8 – Breakdown Voltage Vs. Temperature

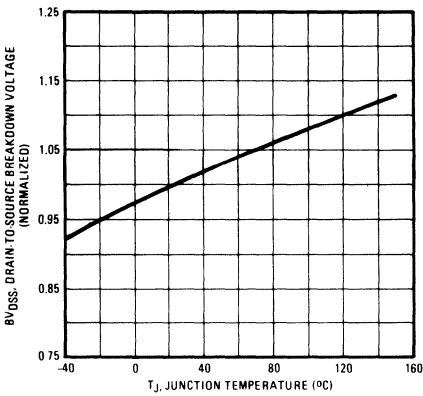


Fig. 7 – Typical Source-Drain Diode Forward Voltage

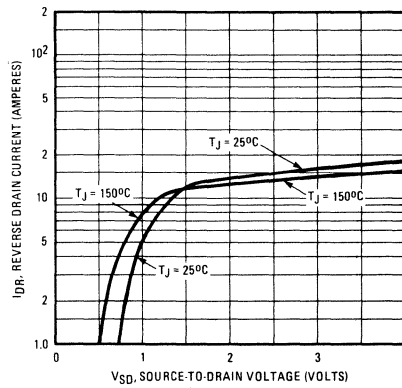


Fig. 9 – Normalized On-Resistance Vs. Temperature

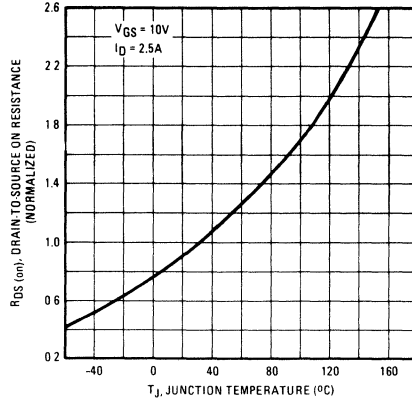


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

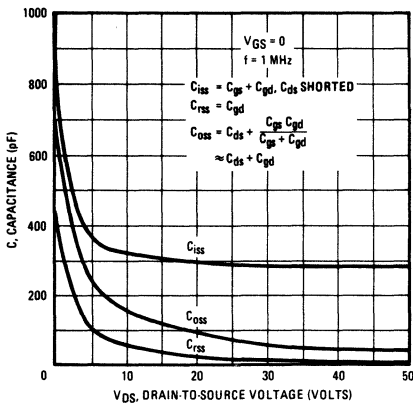


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

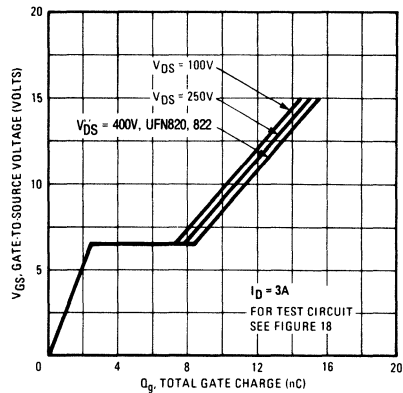


Fig. 12 – Typical On-Resistance Vs. Drain Current

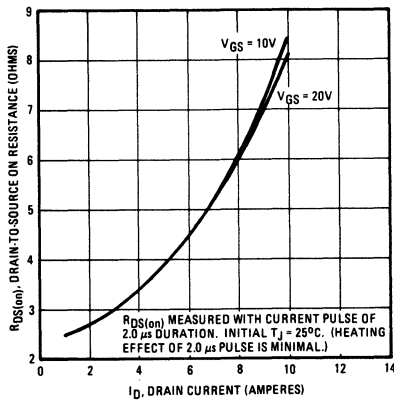


Fig. 13 – Maximum Drain Current Vs. Case Temperature

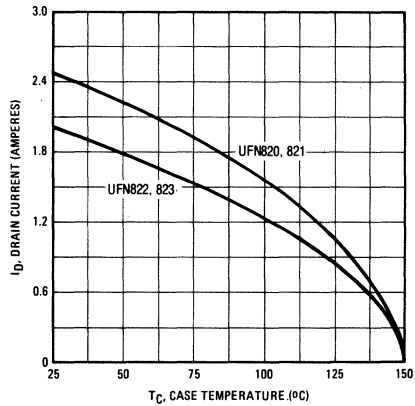


Fig. 14 – Power Vs. Temperature Derating Curve

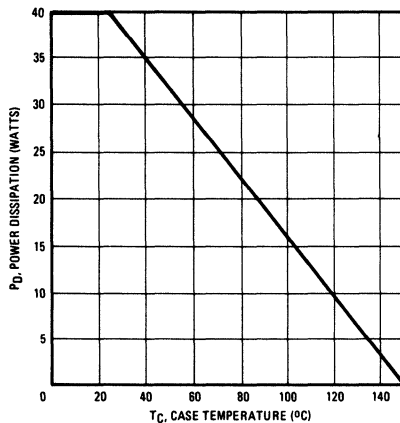


Fig. 15 — Clamped Inductive Test Circuit

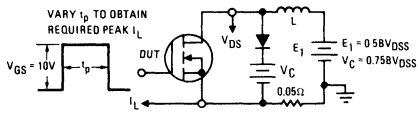


Fig. 16 — Clamped Inductive Waveforms

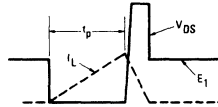


Fig. 17 — Switching Time Test Circuit

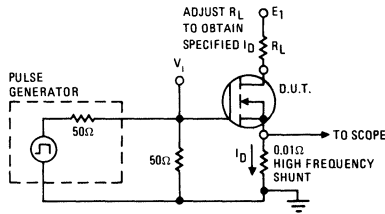
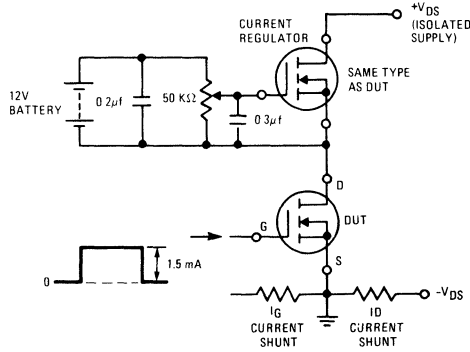


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

UFN830
UFN831
UFN832
UFN833

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

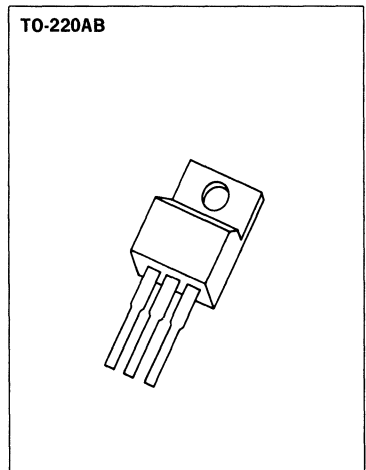
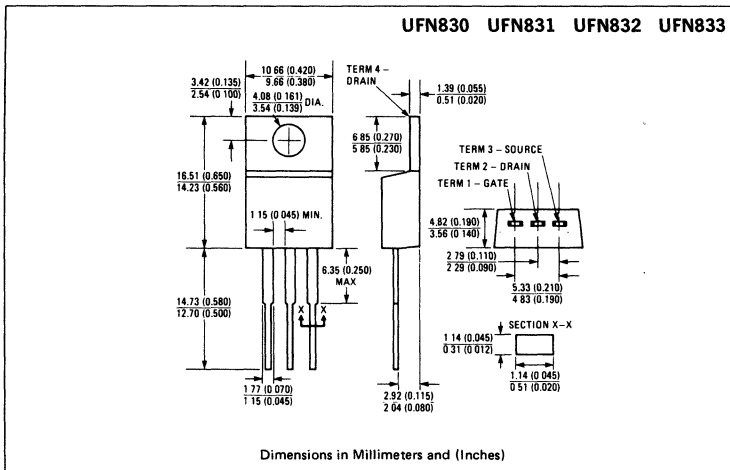
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN830	500V	1.5Ω	4.5A
UFN831	450V	1.5Ω	4.5A
UFN832	500V	2.0Ω	4.0A
UFN833	450V	2.0Ω	4.0A

MECHANICAL SPECIFICATIONS

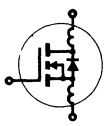


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN830	UFN831	UFN832	UFN833	Units
V_{DS} Drain - Source Voltage ①	500	450	500	450	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 1\text{ M}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	4.5	4.5	4.0	4.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM} Pulsed Drain Current ③	18	18	16	16	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75			(See Fig. 14)	W
Linear Derating Factor	0.6			(See Fig. 14)	W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
	18	18	16	16	
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

4

ELECTRICAL CHARACTERISTICS @ $T_C = 25^\circ\text{C}$ (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	UFN830 UFN832	500	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$
	UFN831 UFN833	450	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$ $V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$
		—	—	1000	μA	
$I_{D(on)}$ On-State Drain Current ②	UFN830 UFN831	4.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$
	UFN832 UFN833	4.0	—	—	A	
	UFN830 UFN831	—	1.3	1.5	Ω	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	UFN832 UFN833	—	1.5	2.0	Ω	$V_{GS} = 10\text{V}$, $I_D = 2.5\text{A}$
	ALL	2.5	3.25	—	S (t)	
g_{fs} Forward Transconductance ②	ALL	—	600	800	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$ See Fig. 10
C_{iss} Input Capacitance	ALL	—	100	200	pF	$V_{DD} = 225\text{V}$, $I_D = 2.5\text{A}$, $Z_o = 15\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
C_{oss} Output Capacitance	ALL	—	30	60	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	—	30	ns	$V_{GS} = 10\text{V}$, $I_D = 6.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	55	ns	
t_r Rise Time	ALL	—	—	30	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	30	ns	
t_f Fall Time	ALL	—	—	30	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	30	nC	
Q_{gs} Gate-Source Charge	ALL	—	11	—	nC	Measured from the contact screw on tab to center of die.
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	11	—	nC	
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
		—	4.5	—	nH	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJC} Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN830 UFN831	—	—	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN832 UFN833	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN830 UFN831	—	—	18	A	
		UFN832 UFN833	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	UFN830 UFN831	—	—	1.6	V	$T_C = 25^\circ\text{C}, I_S = 4.5\text{A}, V_{GS} = 0\text{V}$
		UFN832 UFN833	—	—	1.5	V	$T_C = 25^\circ\text{C}, I_S = 4.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150^\circ\text{C}, I_F = 4.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	$T_J = 150^\circ\text{C}, I_F = 4.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

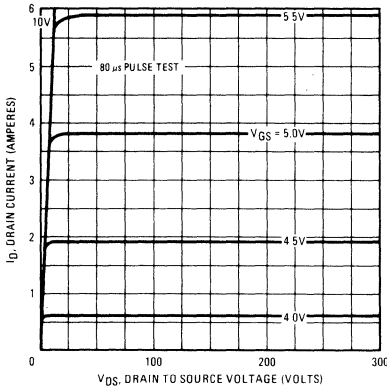


Fig. 2 – Typical Transfer Characteristics

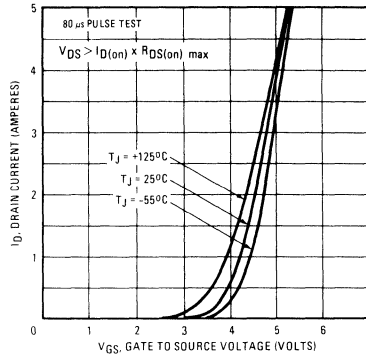


Fig. 3 – Typical Saturation Characteristics

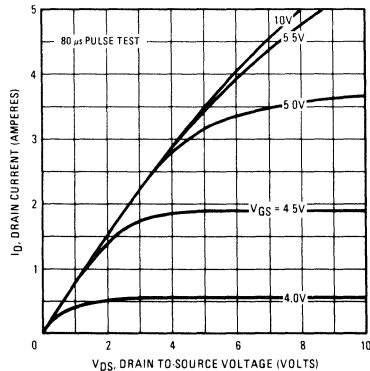


Fig. 4 – Maximum Safe Operating Area

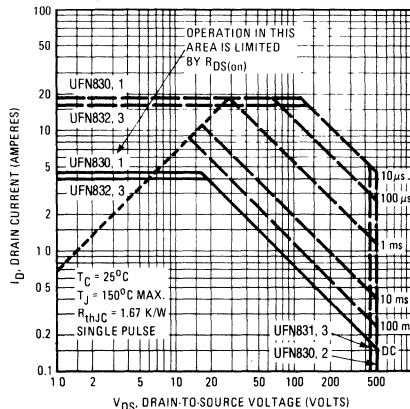


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

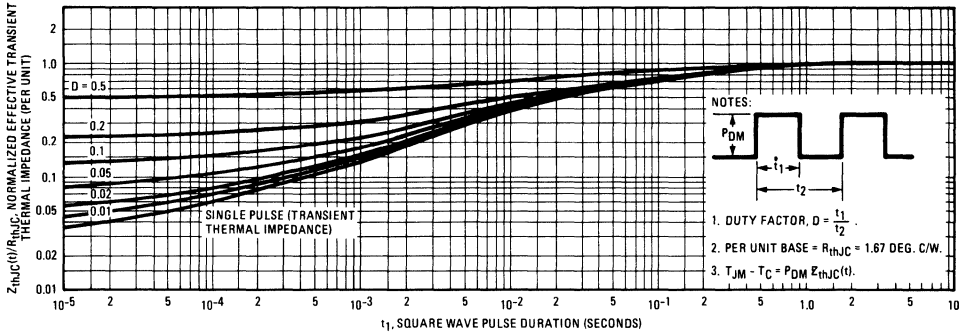


Fig. 6 – Typical Transconductance Vs. Drain Current

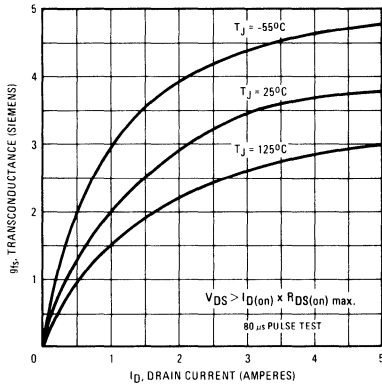


Fig. 7 – Typical Source-Drain Diode Forward Voltage

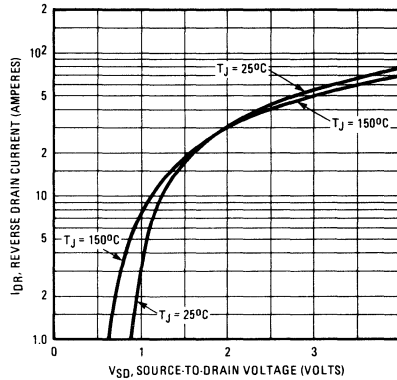


Fig. 8 – Breakdown Voltage Vs. Temperature

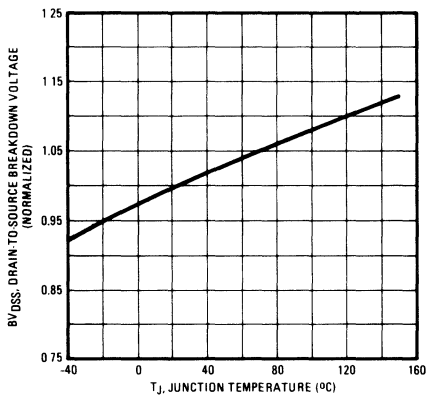


Fig. 9 – Normalized On-Resistance Vs. Temperature

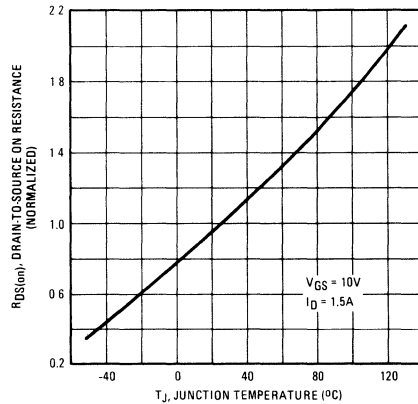


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

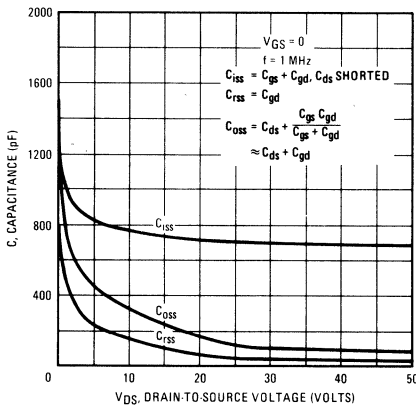


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

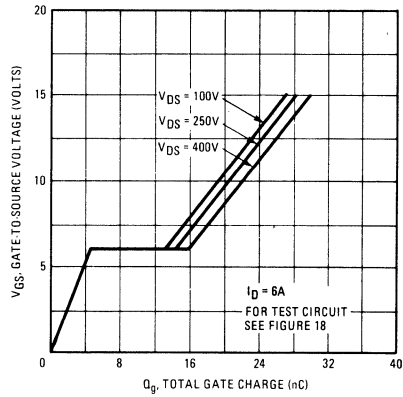


Fig. 12 — Typical On-Resistance Vs. Drain Current

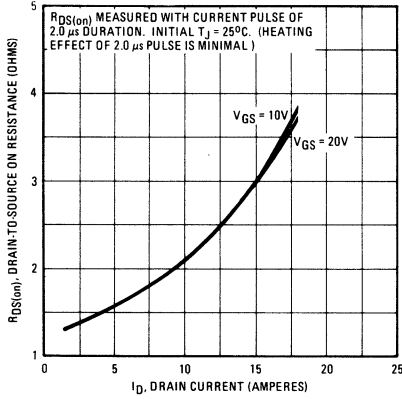


Fig. 13 — Maximum Drain Current Vs. Case Temperature

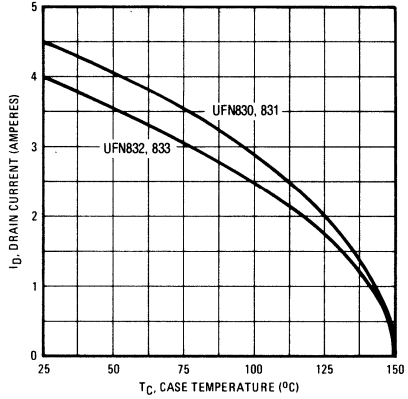


Fig. 14 — Power Vs. Temperature Derating Curve

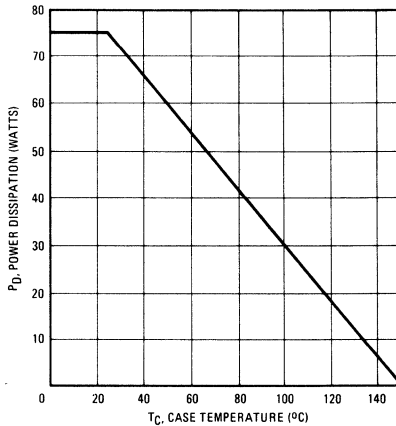


Fig. 15 — Clamped Inductive Test Circuit

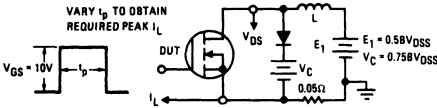


Fig. 16 — Clamped Inductive Waveforms

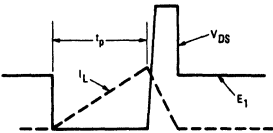


Fig. 17 — Switching Time Test Circuit

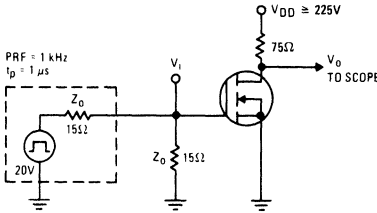
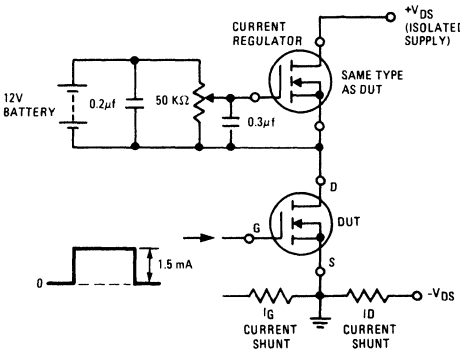


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 0.85 Ohm
N-Channel

UFN840
UFN841
UFN842
UFN843

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitorde power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

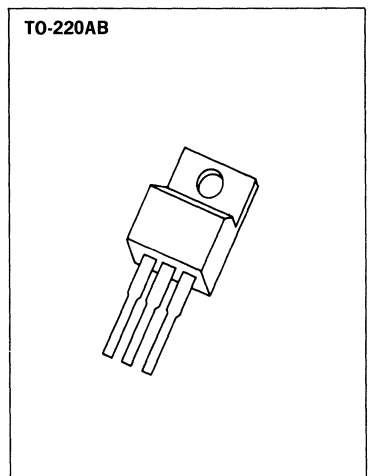
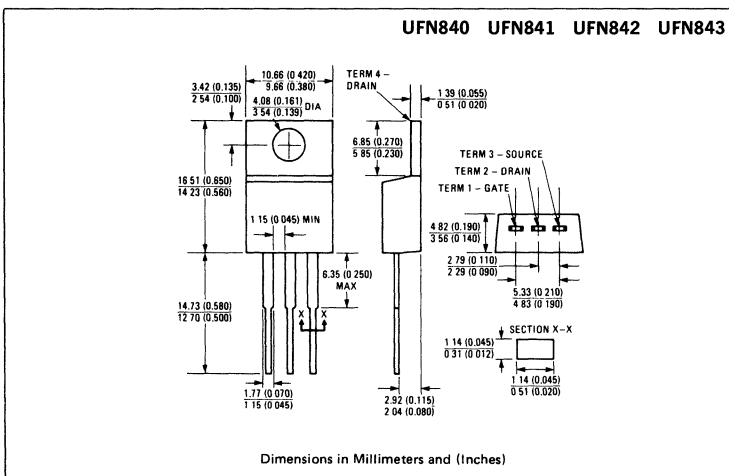
The Unitorde power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN840	500V	0.85Ω	8.0A
UFN841	450V	0.85Ω	8.0A
UFN842	500V	1.10Ω	7.0A
UFN843	450V	1.10Ω	7.0A

MECHANICAL SPECIFICATIONS

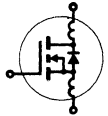


ABSOLUTE MAXIMUM RATINGS

Parameter	UFN840	UFN841	UFN842	UFN843	Units
V _{DS} Drain - Source Voltage ①	500	450	500	450	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 1 MΩ) ①	500	450	500	450	V
I _D @ T _C = 25°C Continuous Drain Current	8.0	8.0	7.0	7.0	A
I _D @ T _C = 100°C Continuous Drain Current	5.0	5.0	4.0	4.0	A
I _{DM} Pulsed Drain Current ③	32	32	28	28	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/K
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
T _J T _{stg} Operating Junction and Storage Temperature Range	-55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

4


ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	UFN840 UFN842	500	—	—	V	V _{GS} = 0V I _D = 250μA	
	UFN841 UFN843	450	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
		—	—	1000	μA		
I _{D(on)} On-State Drain Current ②	UFN840 UFN841	8.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
	UFN842 UFN843	7.0	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	UFN840 UFN841	—	0.8	0.85	Ω	V _{GS} = 10V, I _D = 4.0A	
	UFN842 UFN843	—	1.0	1.1	Ω		
g _{fs} Forward Transconductance ②	ALL	4.0	6.5	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 4.0A	
C _{iss} Input Capacitance	ALL	—	1225	1600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{OSS} Output Capacitance	ALL	—	200	350	pF		
C _{rSS} Reverse Transfer Capacitance	ALL	—	85	150	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	17	35	ns	V _{DD} = 200V, I _D = 4.0A, Z _o = 4.7Ω See Fig. 17	
t _r Rise Time	ALL	—	5	15	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	42	90	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	14	30	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	V _{GS} = 10V, I _D = 10A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	20	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	22	—	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R _{thJC} Junction-to-Case	ALL	—	—	1.0	K/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN840	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		UFN841	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN840	—	—	32	A	
		UFN841	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN840	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 100\text{A}/\mu\text{s}$
		UFN841	—	—	1.9	V	$T_C = 25^\circ\text{C}, I_S = 7.0\text{A}, V_{GS} = 100\text{A}/\mu\text{s}$
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

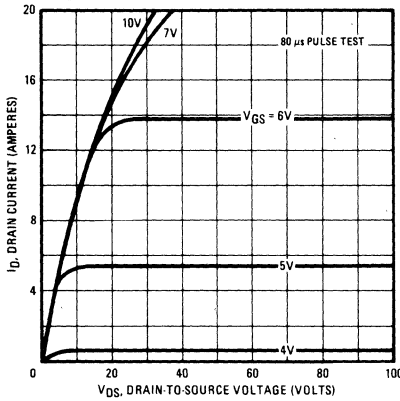


Fig. 2 – Typical Transfer Characteristics

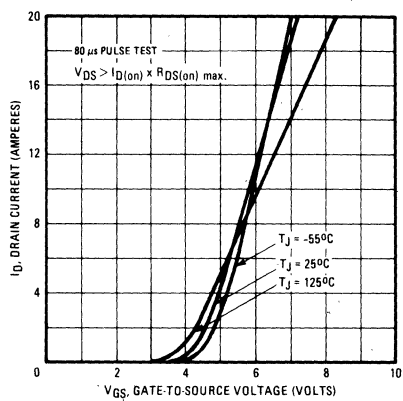


Fig. 3 – Typical Saturation Characteristics

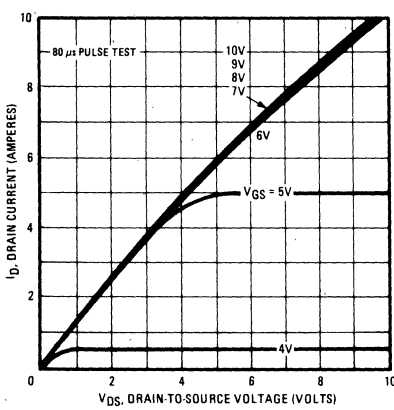


Fig. 4 – Maximum Safe Operating Area

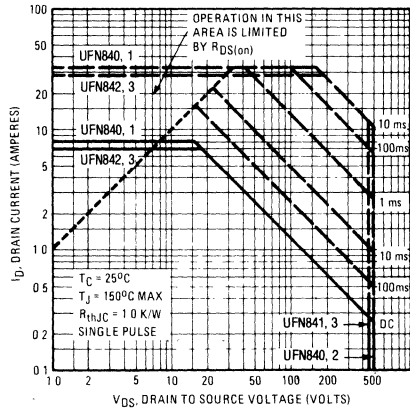


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

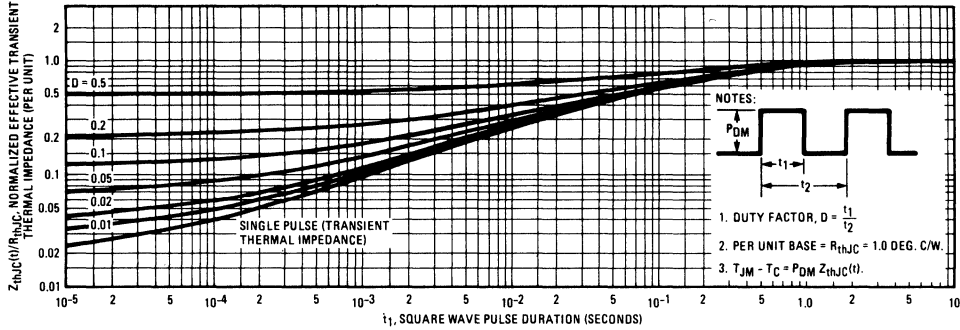


Fig. 6 – Typical Transconductance Vs. Drain Current

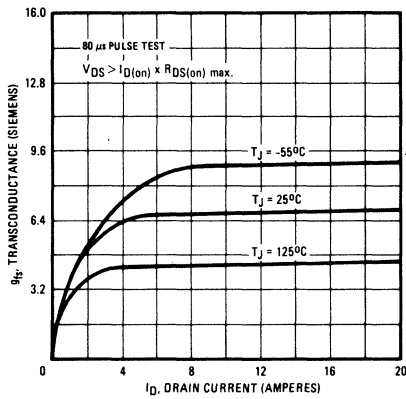


Fig. 7 – Typical Source-Drain Diode Forward Voltage

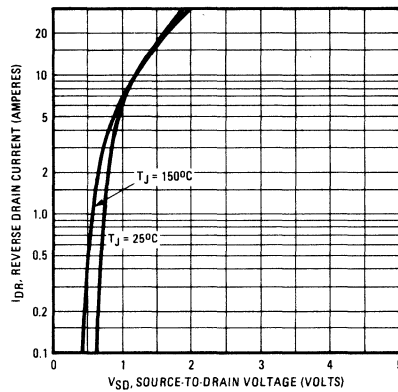


Fig. 8 – Breakdown Voltage Vs. Temperature

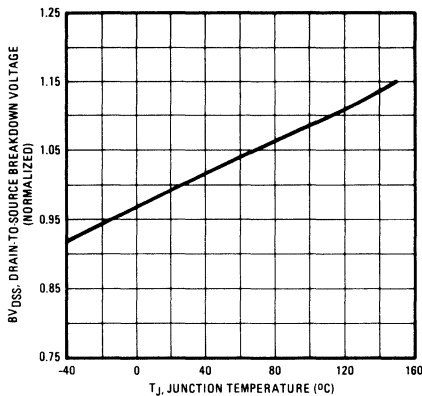


Fig. 9 – Normalized On-Resistance Vs. Temperature

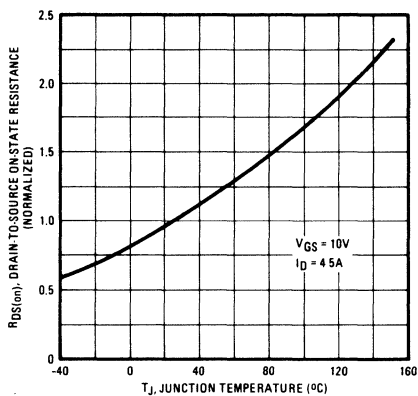


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

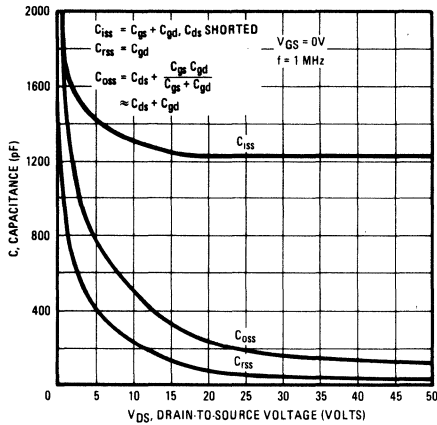


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

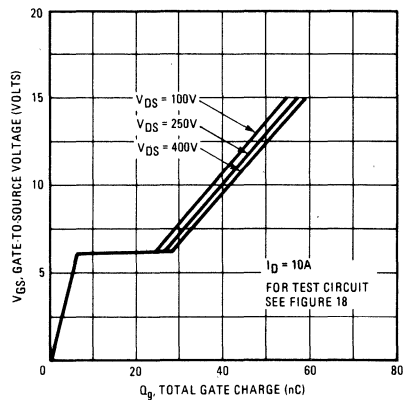


Fig. 12 – Typical On-Resistance Vs. Drain Current

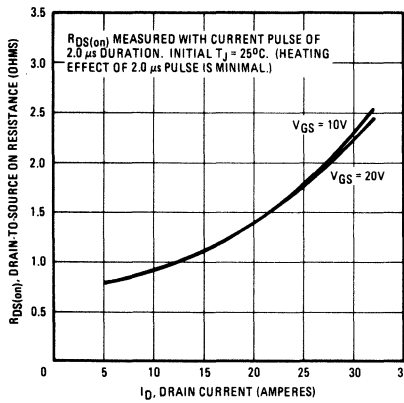


Fig. 13 – Maximum Drain Current Vs. Case Temperature

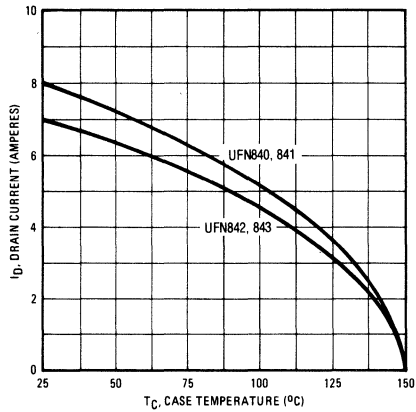


Fig. 14 – Power Vs. Temperature Derating Curve

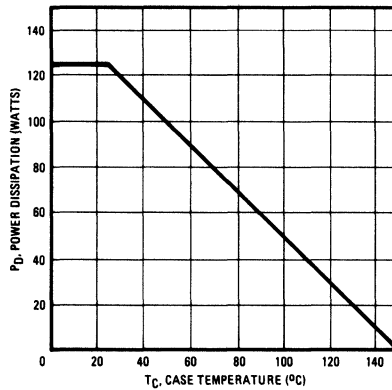


Fig. 15 – Clamped Inductive Test Circuit

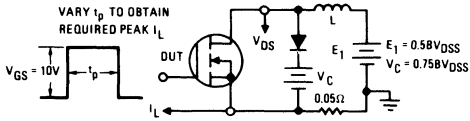
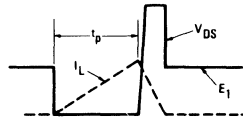


Fig. 16 – Clamped Inductive Waveforms



4

Fig. 17 – Switching Time Test Circuit

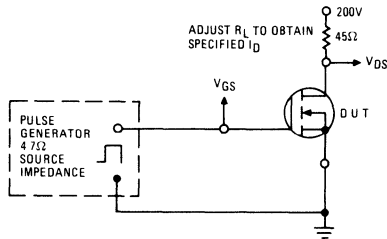
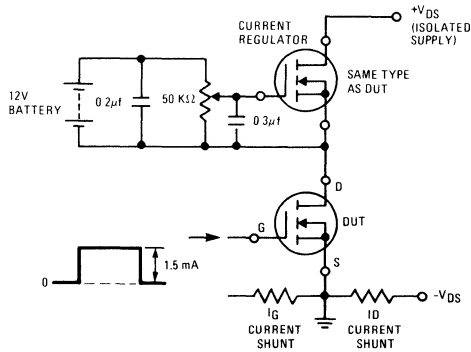


Fig. 18 – Gate Charge Test Circuit



POWER TRANSISTORS

5A, 500V, Fast Switching, High E_{sb}
Silicon NPN Mesa

UMT1006
UMT1007

FEATURES

- Rise Time: $0.4\mu\text{S}$
 - Fall Time: $0.4\mu\text{S}$
 - High Second Breakdown Energy: $540\mu\text{J}$
 - Collector Emitter Voltage: up to 500V
 - Peak Collector Current: 10A
 - Key Parameters characterized at 100°C
- $I_C = 3\text{A}$

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged E_{sb} capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

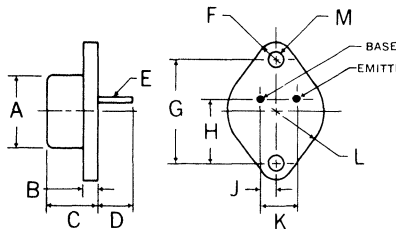
ABSOLUTE MAXIMUM RATINGS

	UMT1006	UMT1007
Collector Emitter Voltage, V_{CEV}	400V	500V
Collector Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter Base Voltage, V_{EBO}	7V	7V
Collector Current, I_C continuous	5A	5A
Collector Current, I_C peak	10A	10A
Base Current, I_B continuous	5A	5A
Power Dissipation, 25°C Case	100W	100W
Derating Factor	$.571\text{W}/^\circ\text{C}$	$.571\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	-65 to 200°C	

MECHANICAL SPECIFICATIONS

NOTE:

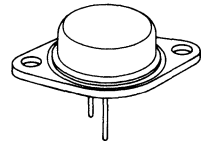
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



UMT1006 UMT1007

	ins.	mm.
A	875 MAX	22.23 MAX.
B	.135 MAX	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN	7.92 MIN
E	.038-0.043 DIA	0.97-1.09 DIA.
F	.188 MAX RAD	4.78 MAX RAD.
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	.525 MAX RAD	13.34 MAX. RAD.
M	.151-.161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)



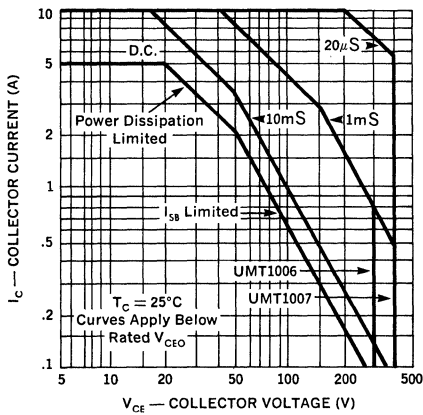
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	UMT1006		UMT1007		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 1.5A, V_{CE} = 2V$
D.C. Current Gain (Note 1)	h_{FE}	7	35	7	35		$I_C = 3.0A, V_{CE} = 2V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 3.0A, I_B = 0.6A$
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2.0	—	2.0	V	$I_C = 3.0A, I_B = 0.6A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 5.0A, I_B = 1.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.4	—	1.4	V	$I_C = 3.0A, I_B = 0.6A$
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.4	—	1.4	V	$I_C = 3.0A, I_B = 0.6A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A, I_B = 0$
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$I_C = 3.0A, L = 180\mu H$ $I_{B1} = I_{B2} = 0.6A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$ $V_{CE} = 500V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	2.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$ $V_{CE} = 500V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 400V, R_{BE} = 50\Omega$ $V_{CE} = 500V, R_{BE} = 50\Omega$
Output Capacitance, Common Base	C_{obo}	50	150	50	150	pF	$V_{CB} = 10V, f = 1\text{ MHz}$
Gain-Bandwidth Product	F_T	6	24	6	24	MHz	$V_{CE} = 10V, I_C = 0.2A, f = 1\text{ MHz}$
Energy Second Breakdown (unclamped)	$E_{s/b}$	540	—	540	—	μJ	$I_C = 3.0A, V_{BE(off)} = 4V$ $L = 120\mu H$ unclamped
Resistive Switching Speeds							
Delay Time	t_d	—	.05	—	.05	μS	$I_C = 3.0A$ $V_{CC} = 200V$ $I_{B1} = I_{B2} = 0.6A$ $V_{BE(off)} = 5V$
Rise Time	t_r	—	0.4	—	0.4		
Storage Time	t_s	—	4.0	—	4.0		
Fall Time	t_f	—	0.4	—	0.4		
Inductive Switching Speeds							
$T_C = 100^\circ C$							
Storage Time	t_s	—	4.0	—	4.0	μS	$I_C = 3.0A, L = 180\mu H$ $I_{B1} = I_{B2} = 0.6A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
Fall Time	t_f	—	0.4	—	0.4		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.75	—	1.75	$^\circ C/W$	

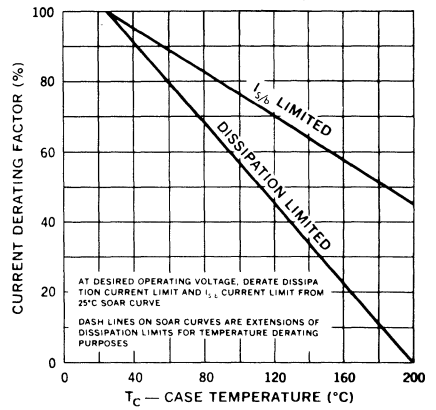
Notes:

- Pulse width = 250 μS ; duty cycle $\leq 1\%$.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

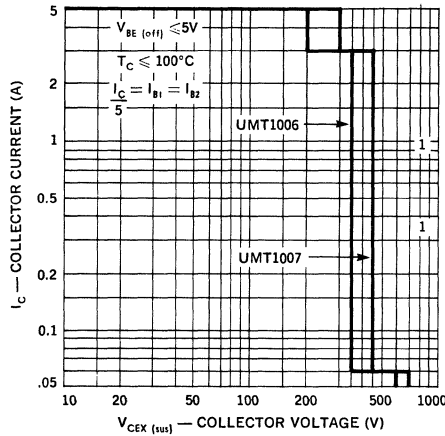
Forward Bias Safe Operating Area



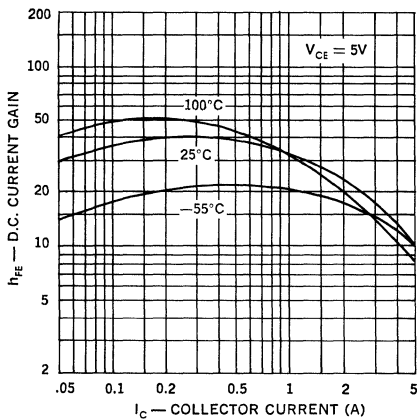
Power Derating



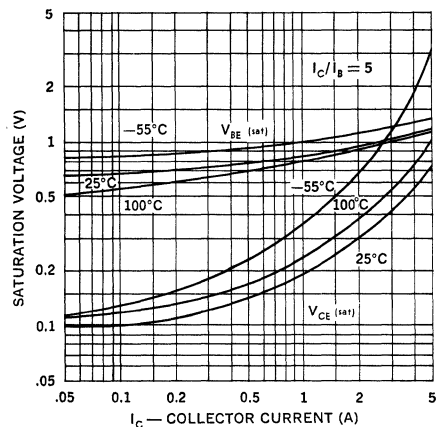
Reverse Biased Safe Operating Area



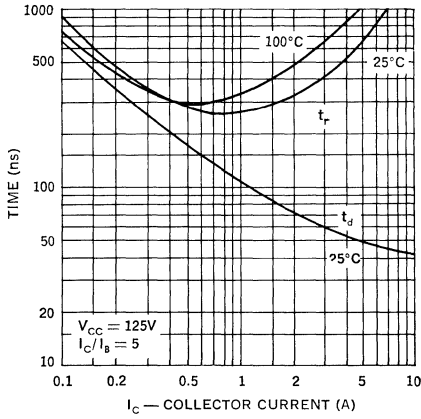
D.C. Current Gain



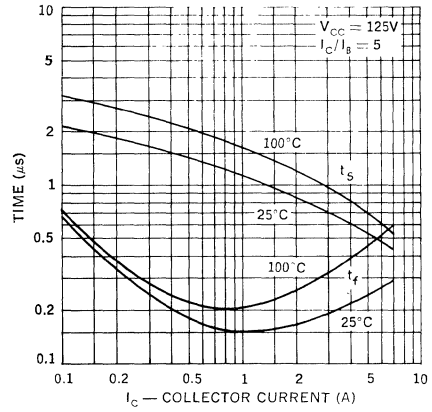
Saturation Voltages



Resistive Turn-On Time

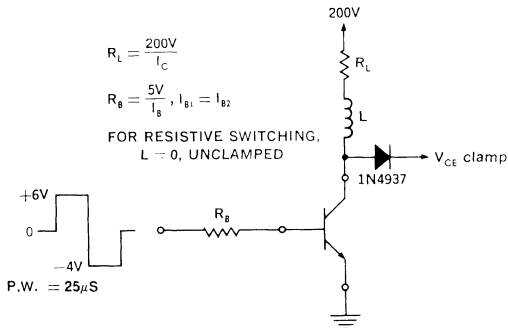


Resistive Turn-Off Time

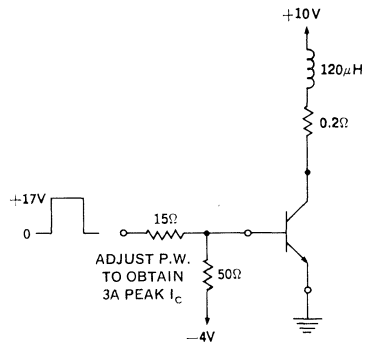


4

Switching Time, $V_{CEX(sus)}$
Test Circuit



$E_{S/b}$ Test Circuit



POWER TRANSISTORS

8 Amp, 500V Fast Switching, High $E_{s/b}$
Silicon NPN Mesa

UMT1008
UMT1009

FEATURES

- Rise Time: $0.4\mu s$ } $I_C = 5A$
- Fall Time: $0.4\mu s$ }
- High Second Breakdown Energy: $1500\mu J$
- Collector Emitter Voltage: up to 500V
- Peak Collector Current: 16A
- Key Parameters characterized at $100^\circ C$

DESCRIPTION

These high voltage triple diffused glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{s/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

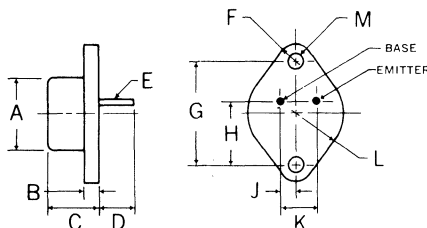
ABSOLUTE MAXIMUM RATINGS

	UMT1008	UMT1009
Collector Emitter Voltage, V_{CEV}	400V	500V
Collector Emitter Voltage, $V_{CEO(SUS)}$	300V	400V
Emitter Base Voltage, V_{EBO}	7V	7V
Collector Current, I_C continuous	8A	8A
Collector Current, I_C peak	16A	16A
Base Current, I_B continuous	8A	8A
Power Dissipation, $25^\circ C$ Case	125W	125W
Derating Factor	.714W/ $^\circ C$.714W/ $^\circ C$
Operating and Storage Temperature Range	-65 to $200^\circ C$	

MECHANICAL SPECIFICATIONS

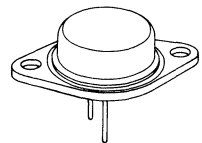
NOTE:

Loads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than $260^\circ C$ for 10 seconds.



	ins.	mm.
A	875 MAX	22.23 MAX
B	135 MAX	3.43 MAX
C	250-450	6.35-11.43
D	312 MIN	7.92 MIN
E	0.38-0.43 DIA	0.97-1.09 DIA
F	188 MAX RAD	4.78 MAX RAD
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX RAD	13.34 MAX RAD
M	151-161 DIA	3.84-4.09 DIA

TO-204AA (TO-3)



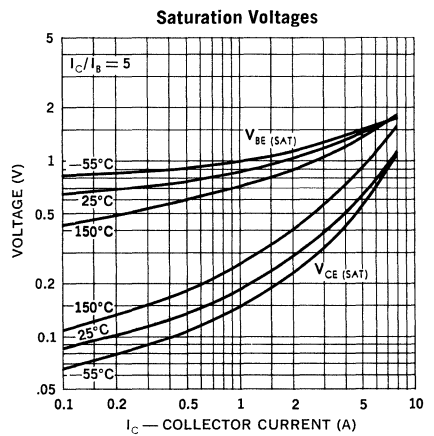
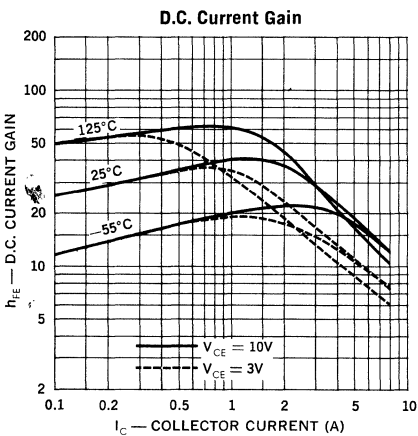
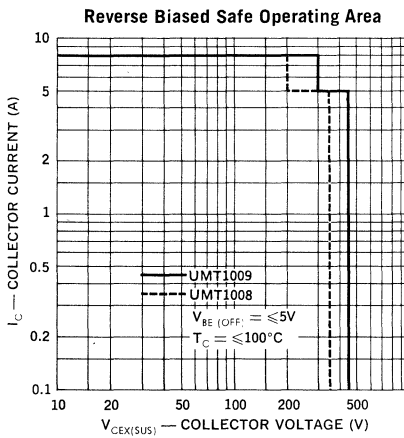
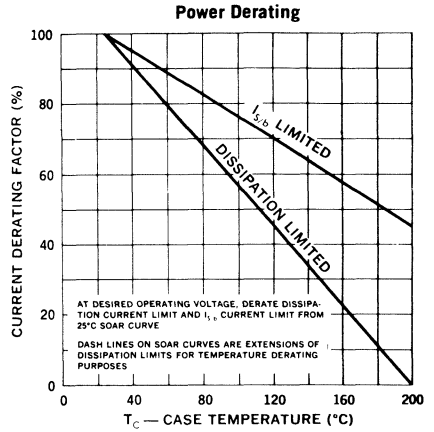
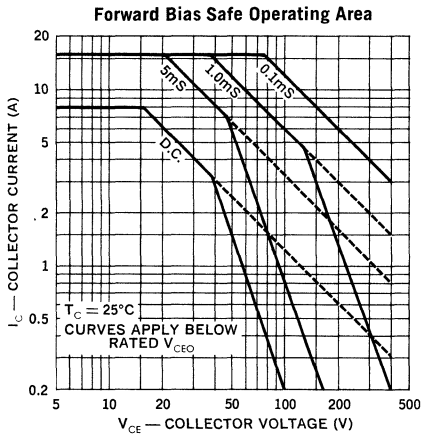
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

4

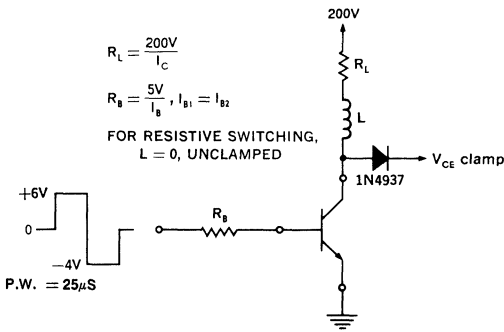
Test	Symbol	UMT1008		UMT1009		Units	Test Conditions	
		MIN.	MAX.	MIN.	MAX.			
D.C. Current Gain (Note 1)	β_{FE}	12	60	12	60		$I_C = 2.5A, V_{CE} = 3V$	
D.C. Current Gain (Note 1)	β_{FE}	7	35	7	35		$I_C = 5.0A, V_{CE} = 3V$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 5.0A, I_B = 1.0A$	
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2.5	—	2.5	V	$I_C = 5.0A, I_B = 1.0A$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 8.0A, I_B = 2.0A$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 5.0A, I_B = 1.0A$	
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 5.0A, I_B = 1.0A$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A$	
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$I_C = 5.0A, L = 180\mu H$ $I_{B1} = I_{B2} = 1A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$	
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$	
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$	
		—	—	—	0.5		$V_{CE} = 500V, V_{BE} = -1.5V$	
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	2.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$	
		—	—	—	2.5		$V_{CE} = 500V, V_{BE} = -1.5V$	
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 400V, R_{BE} = 50\Omega$	
		—	—	—	3.0		$V_{CE} = 500V, R_{BE} = 50\Omega$	
Output Capacitance, Common Base	C_{obo}	100	200	100	200	pF	$V_{CB} = 10V, f = 1\text{ MHz}$	
Gain-Bandwidth Product	F_T	6	30	6	30	MHz	$V_{CE} = 10V, I_C = 0.3A, f = 1\text{ MHz}$	
Energy Second Breakdown (unclamped)	$E_{S/b}$	1500	—	1500	—	μJ	$I_C = 5.0A$ $I_{B1} = 1A$ $L = 120\mu H$ unclamped	
Resistive Switching Speeds	Delay Time	t_d	—	0.1	—	0.1	μS	$I_C = 5.0A$ $V_{CC} = 200V$ $I_{B1} = I_{B2} = 1.0A$ $V_{BE(off)} = 5V$
	Rise Time	t_r	—	0.4	—	0.4		
	Storage Time	t_s	—	4.0	—	4.0		
	Fall Time	t_f	—	0.4	—	0.4		
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	t_s	—	4.0	—	4.0	μS	$I_C = 5.0A, L = 180\mu H$ $I_{B1} = I_{B2} = 1A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
	Fall Time	t_f	—	0.4	—	0.4		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.4	—	1.4	$^\circ C/W$		

Notes:

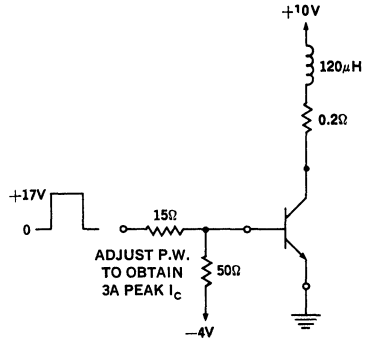
1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.



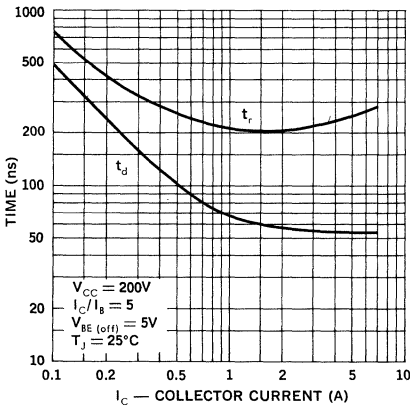
**Switching Time, $V_{CEX(sus)}$
Test Circuit**



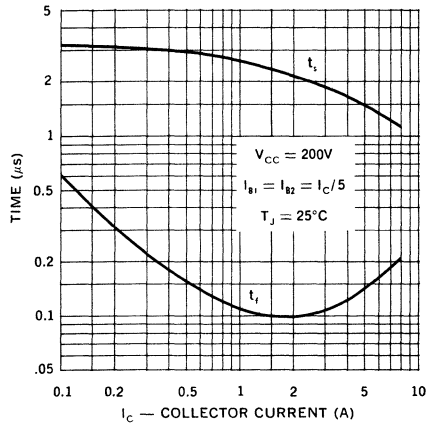
$E_{s/b}$ Test Circuit



Turn-On Time



Turn-Off Time



POWER TRANSISTORS

15A, 500V, Fast Switching, High $E_{S/b}$ Silicon NPN Mesa

UMT1011
UMT1012

FEATURES

- Rise Time: $0.4\mu\text{S}$
 - Fall Time: $0.4\mu\text{S}$
 - High Second Breakdown Energy: $6000\mu\text{J}$
 - Low Saturation Voltage
 - Collector Emitter Voltage: up to 500V
 - Peak Collector Current: 30A
 - Key Parameters characterized at 100°C
- $I_C = 10\text{A}$

DESCRIPTION

These high voltage glass passivated power transistors combine fast switching, low saturation voltage and rugged $E_{S/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, ignition systems and deflection circuits.

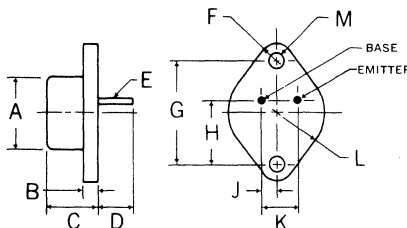
ABSOLUTE MAXIMUM RATINGS

	UMT1011	UMT1012
Collector Emitter Voltage, V_{CEV}	400V	500V
Collector Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter Base Voltage, V_{EBO}	9V	9V
Collector Current, I_C continuous	15A	15A
Collector Current, I_C peak	30A	30A
Base Current, I_B continuous	10A	10A
Power Dissipation, 25°C Case	175W	175W
Derating Factor	1.0W/ $^\circ\text{C}$	1.0W/ $^\circ\text{C}$
Operating and Storage Temperature Range	-65 to 200°C	

MECHANICAL SPECIFICATIONS

NOTE:

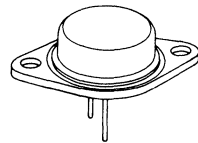
Leads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.



UMT1011 UMT1012

	ins.	mm.
A	875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	312 MIN.	7.92 MIN.
E	.038-.043 DIA	0.97-1.09 DIA
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-675	16.64-17.15
J	205-.225	5.21-5.72
K	420-440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)



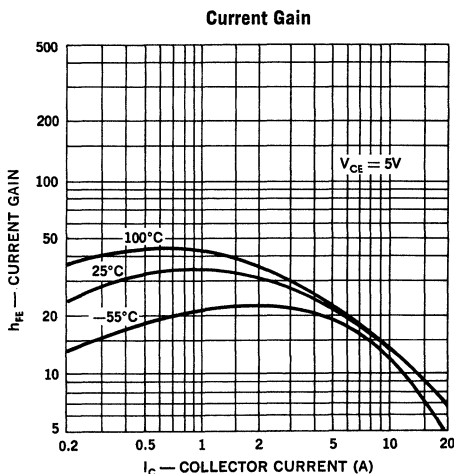
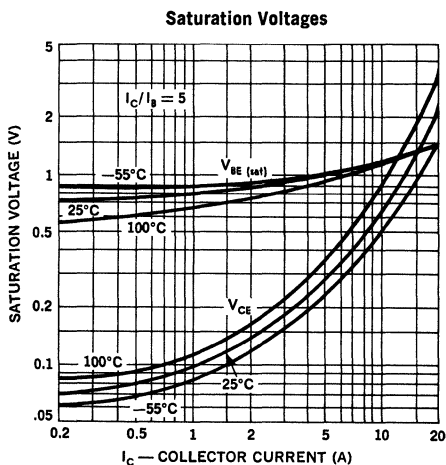
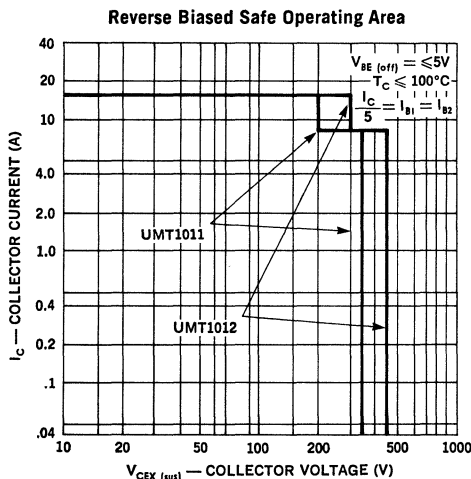
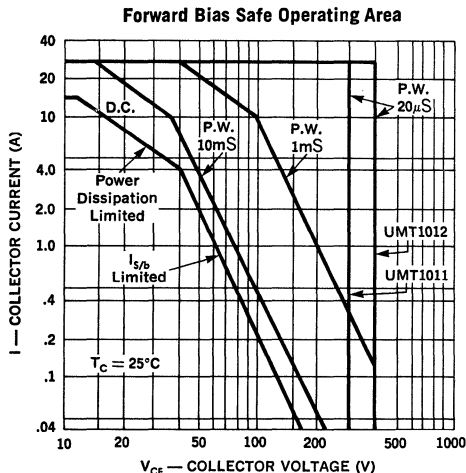
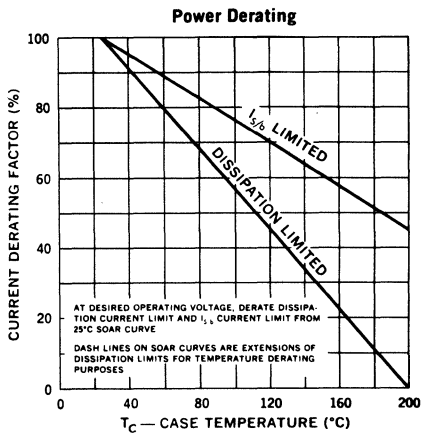
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	UMT1011		UMT1012		Units	Test Conditions	
		MIN.	MAX.	MIN.	MAX.			
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 5.0A, V_{CE} = 2.0V$	
D.C. Current Gain (Note 1)	h_{FE}	6	30	6	30		$I_C = 10A, V_{CE} = 2.0V$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 10A, I_B = 2.0A$	
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	2.0	—	2.0	V	$I_C = 10A, I_B = 2.0A$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	5.0	—	5.0	V	$I_C = 15A, I_B = 3.0A$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 10A, I_B = 2.0A$	
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 10A, I_B = 2.0A$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A, I_B = 0$	
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$I_C = 8.0A, L = 180\mu H$ $I_{B1} = I_{B2} = 2.0A$ $V_{CE \text{ clamp}} = \text{rated } V_{CEX(sus)}$	
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$	
Collector Cutoff Current	I_{CEV}	—	1.0	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$	
		—	—	—	1.0		$V_{CE} = 500V, V_{BE} = -1.5V$	
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	3.0	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$	
		—	—	—	3.0		$V_{CE} = 500V, V_{BE} = -1.5V$	
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 400V, R_{BE} = 50\Omega$	
		—	—	—	3.0		$V_{CE} = 500V, R_{BE} = 50\Omega$	
Output Capacitance, Common Base	C_{obo}	180	360	180	360	pF	$V_{CB} = 10V, f = 1 \text{ MHz}$	
Gain-Bandwidth Product	F_T	6	24	6	24	MHz	$V_{CE} = 10V, I_C = 0.5A, f = 1 \text{ MHz}$	
Energy Second Breakdown (unclamped)	$E_{S/b}$	6000	—	6000	—	μJ	$I_C = 10A, V_{BE(off)} = -4V$ $L = 120\mu H$ unclamped	
Resistive Switching Speeds	Delay Time	t_d	—	.05	—	μS	$I_C = 10A$ $V_{CC} = 200V$ $I_{B1} = I_{B2} = 2.0A$ $V_{BE(off)} = 5V$	
	Rise Time	t_r	—	0.4	—			0.4
	Storage Time	t_s	—	4.0	—			4.0
	Fall Time	t_f	—	0.4	—			0.4
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	t_s	—	4.0	—	μS	$I_C = 10A, L = 180\mu H$ $I_{B1} = I_{B2} = 2.0A$ $V_{CE \text{ clamp}} = \text{rated } V_{CEX(sus)}$	
	Fall Time	t_f	—	0.4	—			0.4
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.0	—	1.0	$^\circ C/W$		

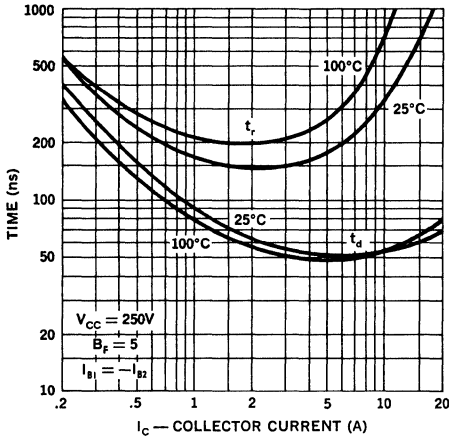
Notes:

1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

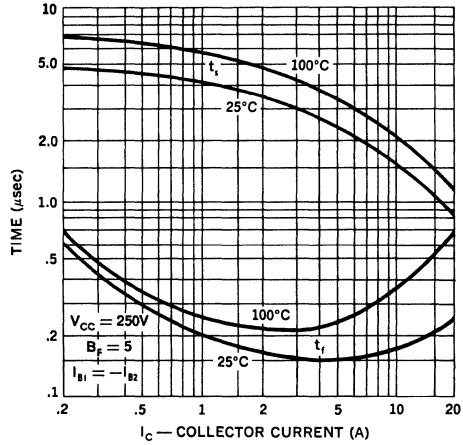




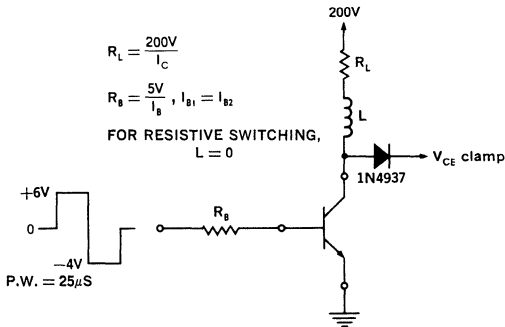
Resistive Turn-On Time



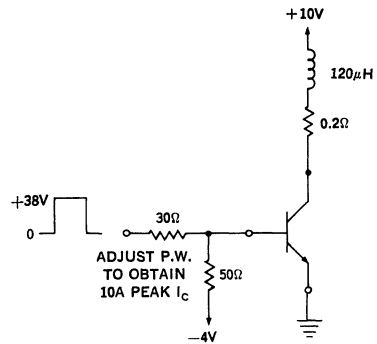
Resistive Turn-Off Time



Switching Time, V_{CEX} (sus) Test Circuit



$E_{s/b}$ Test Circuit



POWER TRANSISTORS

3 Amp, 500V, Fast Switching

Silicon NPN Mesa

UMT1203
UMT1204

FEATURES

- Collector Emitter Voltage: up to 500V
- Peak Collector Current: 5A
- Rise Time: $\leq 1.0\mu s$
- Fall Time: $\leq 0.7\mu s$
- Key Parameters characterized at 100°C
- Economical Plastic Molded Construction

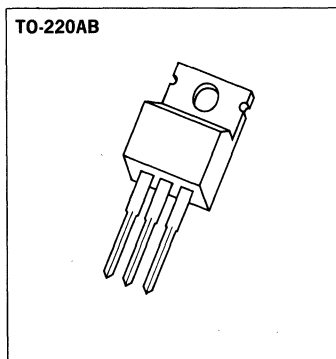
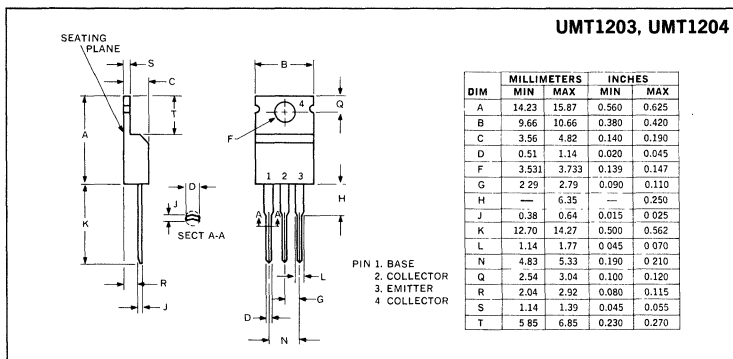
DESCRIPTION

These high voltage triple diffused glass passivated power transistors, in a plastic TO-220AB package, combine fast switching, low saturation voltage and rugged $E_s/4$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, deflection circuits, motor controls and solenoid/relay drivers.

ABSOLUTE MAXIMUM RATINGS

	UMT1203	UMT1204
Collector Emitter Voltage, V_{CEV}	400V	500V
Collector Emitter Voltage, V_{CEO} (sus)	300V	400V
Emitter Base Voltage, V_{EBO}	7V	7V
Collector Current, I_C continuous	3A	3A
Collector Current, I_{CM} peak	5A	5A
Base Current, I_B continuous	1A	1A
Power Dissipation, 25°C Case	40W	40W
Derating Factor	0.32W/°C	0.32W/°C
Operating and Storage Temperature Range	-65 to 150°C	

MECHANICAL SPECIFICATIONS

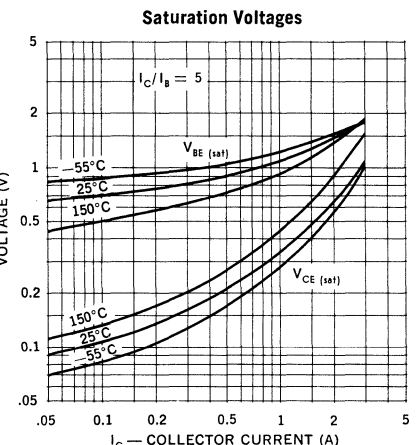
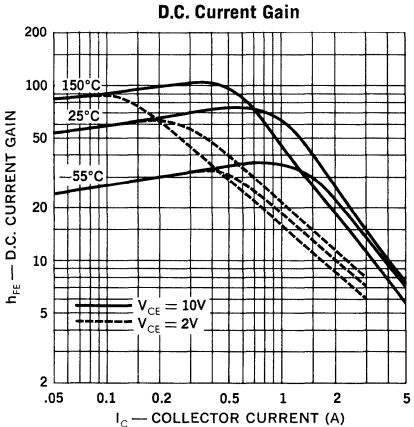
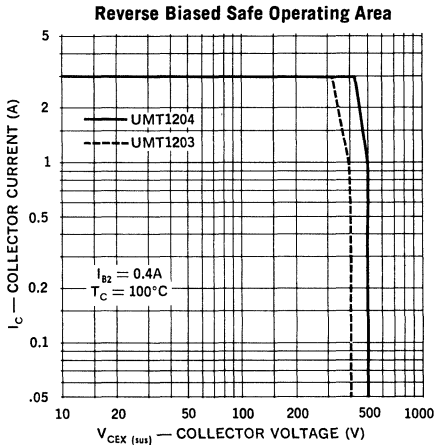
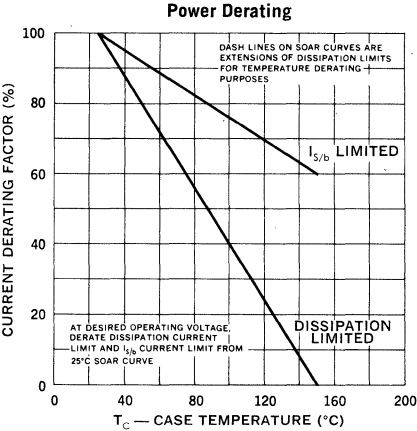
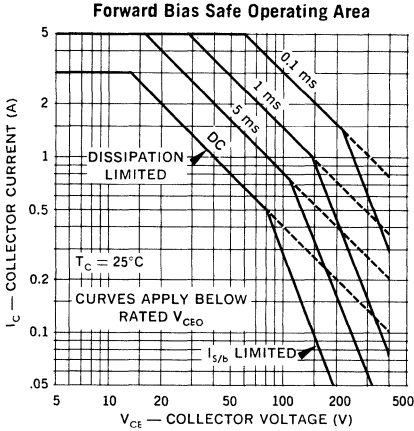


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

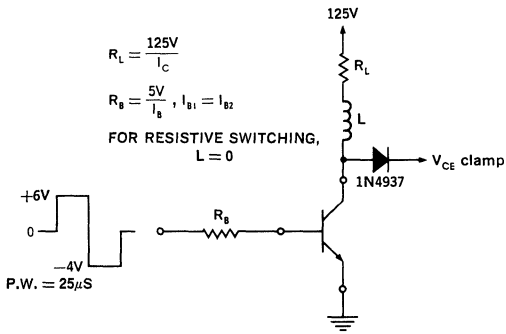
Test	Symbol	UMT1203		UMT1204		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	12	60	12	60		$I_C = 1.0A, V_{CE} = 3V$
D.C. Current Gain (Note 1)	h_{FE}	7	35	7	35		$I_C = 2.0A, V_{CE} = 3V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.2	—	1.2	V	$I_C = 2.0A, I_B = 0.4A$
Collector Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 2.0A, I_B = 0.4A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	3.0	—	3.0	V	$I_C = 3.0A, I_B = 0.75A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.3	—	1.3	V	$I_C = 2.0A, I_B = 0.4A$
Base Saturation Voltage, $T_C = 100^\circ C$ (Note 1)	$V_{BE(sat)}$	—	1.5	—	1.5	V	$I_C = 2.0A, I_B = 0.4A$
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 0.1A$
Collector-Emitter Sustaining Voltage $T_C = 100^\circ C$ (Note 2)	$V_{CEX(sus)}$	350	—	450	—	V	$I_C = 2.0A, L = 500\mu H$ $I_{B1} = I_{B2} = 0.4A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 7V$
Collector Cutoff Current	I_{CEV}	—	0.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	—	—	0.5	mA	$V_{CE} = 500V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	2.5	—	—	mA	$V_{CE} = 400V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	—	—	2.5	mA	$V_{CE} = 500V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	3.0	—	—	mA	$V_{CE} = 400V, R = 50\Omega$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CER}	—	—	—	3.0	mA	$V_{CE} = 500V, R = 50\Omega$
Output Capacitance, Common Base	C_{obo}	35	100	35	100	pF	$V_{CB} = 10V, f = 1\text{ MHz}$
Gain-Bandwidth Product	F_T	6	30	6	30	MHz	$V_{CE} = 10V, I_C = 0.3A, f = 1\text{ MHz}$
Energy Second Breakdown (unclamped)	$E_{S/b}$	80	—	80	—	μJ	$I_C = 2.0A$ $I_{B1} = 0.4A$ $L = 40\mu H$ unclamped
Resistive Switching Speeds							
Delay Time	t_d	—	0.1	—	0.1	μS	$I_C = 2.0A$ $V_{CC} = 200V$ $I_{B1} = I_{B2} = 0.4A$ $V_{BE(off)} = 5V$
Rise Time	t_r	—	1.0	—	1.0		
Storage Time	t_s	—	4.0	—	4.0		
Fall Time	t_f	—	0.7	—	0.7		
Inductive Switching Speeds							
$T_C = 100^\circ C$							
Storage Time	t_s	—	4.0	—	4.0	μS	$I_C = 2.0A, L = 500\mu H$ $I_{B1} = I_{B2} = 0.4A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
Fall Time	t_f	—	0.9	—	0.9		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	3.12	—	3.12	$^\circ C/W$	

Notes:

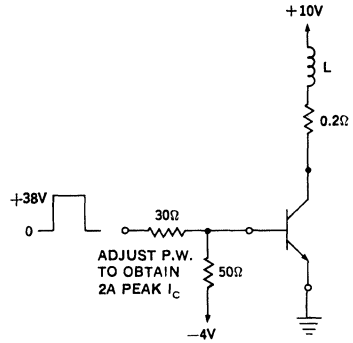
- Pulse width = 250 μS ; duty cycle $\leq 1\%$.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.



Switching Time Test Circuit

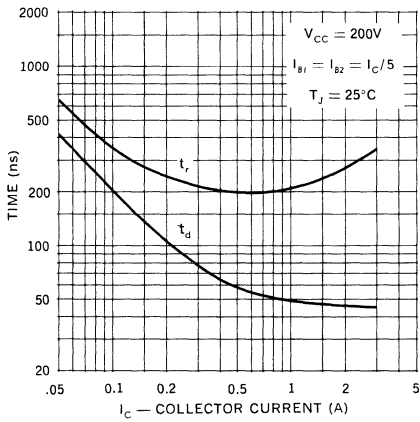


$E_{s/b}$ Test Circuit

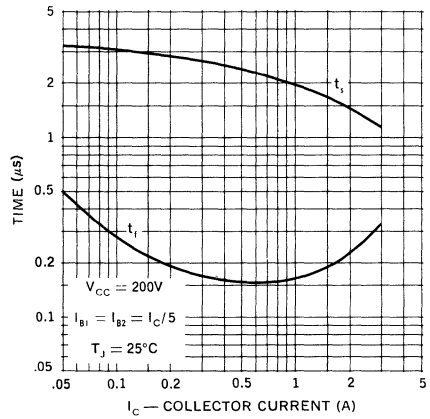


4

Resistive Turn-On Time



Resistive Turn-Off Time



POWER TRANSISTORS

15A, 450V NPN Mesa

UMT2000

FEATURES

- Collector Emitter Voltage: 850V
 - Peak Collector Current: 20A
 - Storage Time $\leq 800\text{ns}$
 - Fall Time $\leq 70\text{ns}$
- } at $I_c = 10\text{A}$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

ABSOLUTE MAXIMUM RATINGS

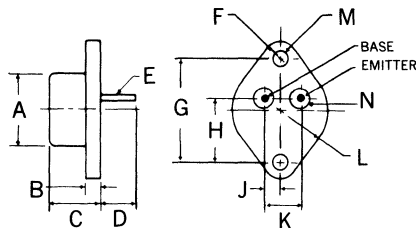
Collector Emitter Voltage, V_{CEV}	850V
Collector Emitter Voltage, $V_{CEO(sus)}$	450V
Emitter Base Voltage, V_{EBO}	6V
Collector Current, I_c continuous	15A
Collector Current, I_{CM} peak (Note 1)	20A
Base Current, I_B continuous	10A
Base Current, I_{BM} peak	15A
Power Dissipation, 25°C Case	175W
100°C Case	100W
above 25°C, derate linearly	1W/°C
Operating and Storage Temperature Range	-65°C to +200°C
Thermal Resistance, Junction to Case, $R_{\theta JC}$	1°C/W

Note: 1. Pulse Test - Pulse Width = 5ms; Duty Cycle $\leq 10\%$

MECHANICAL SPECIFICATIONS

NOTE:

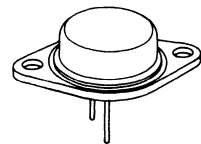
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



UMT2000

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.043 DIA.	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655- .675	16.64- 17.15
J	.205- .225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.
N	.190-.210	4.83-5.33

TO-204AA (TO-3)

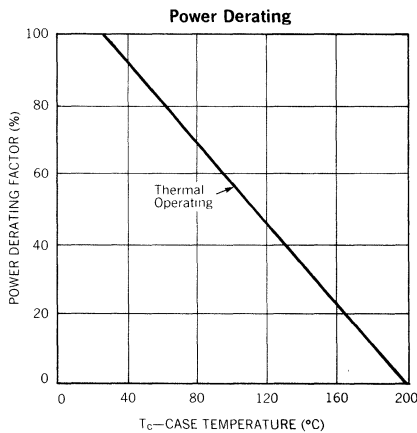
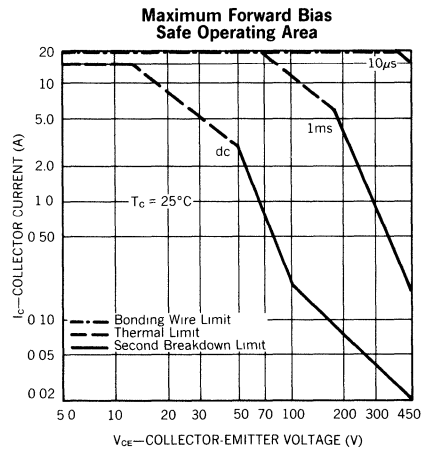
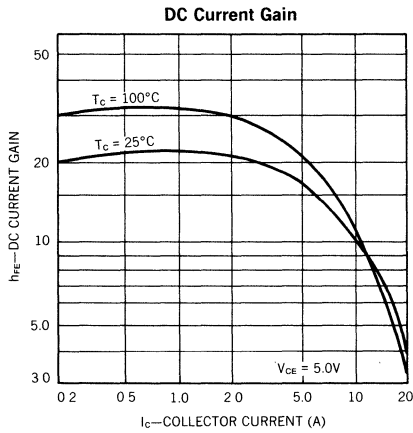
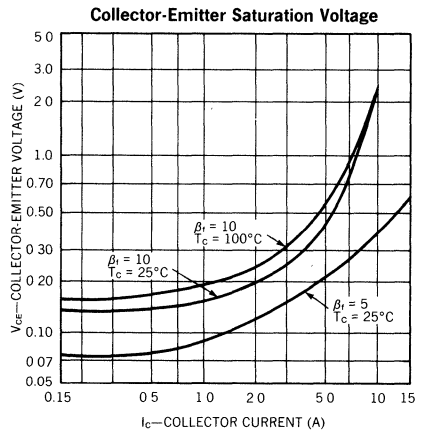
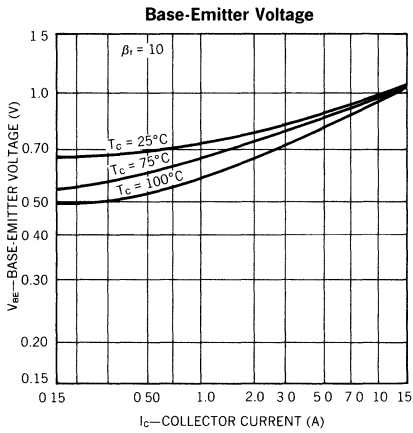


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

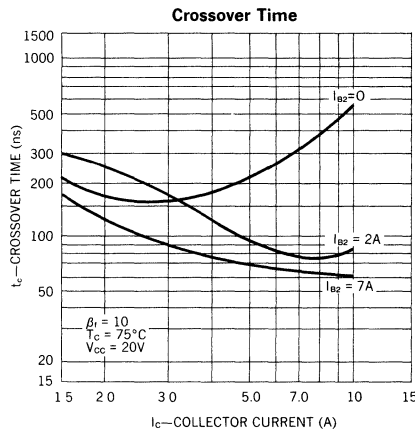
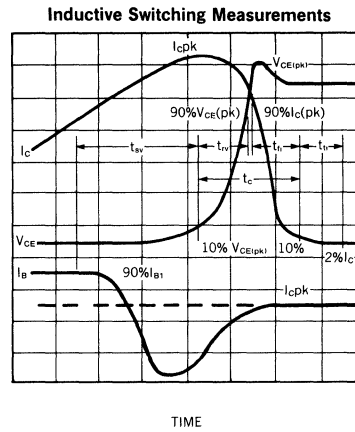
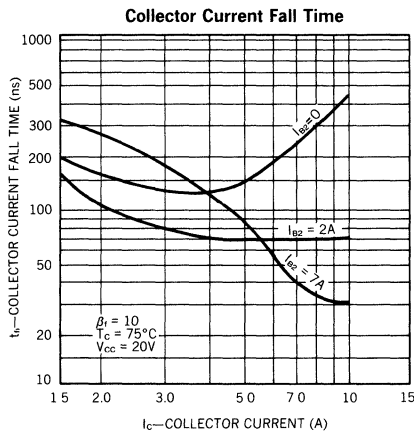
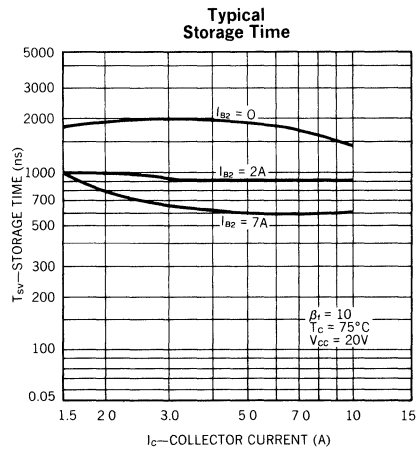
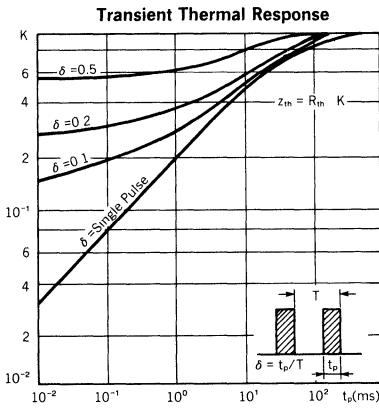
TEST	SYMBOL				UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Off Characteristics						
Collector Emitter Sustaining Voltage	$V_{CE(sus)}$	450	—	—	V	$I_C = 100mA, I_B = 0, L = 10mH$
Collector Cutoff Current	I_{CEV}	—	—	0.25	mA	$V_{CEV} = 850V, V_{BE(off)} = 1.5V$
Collector Cutoff Current $T_C = 100^\circ C$	I_{CEV}	—	—	2.5	mA	$V_{CEV} = 850V, V_{BE(off)} = 1.5V$
Collector Cutoff Current $T_C = 100^\circ C$	I_{CER}	—	—	1.5	mA	$V_{CE} = 850V, R_{BE} = 50\Omega$
Emitter Cutoff Current	I_{EBO}	—	—	1.0	mA	$V_{EB} = 6V, I_C = 0$
On Characteristics (Note 1)						
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	2.5	V	$I_C = 5A, I_B = 0.5A$
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	3.0	V	$I_C = 10A, I_B = 1A$
Collector Emitter Saturation Voltage $T_C = 100^\circ C$	$V_{CE(sat)}$	—	3.0	—	V	$I_C = 10A, I_B = 1A$
Base Emitter Saturation Voltage	$V_{BE(sat)}$	—	—	1.5	V	$I_C = 10A, I_B = 1A$
Base Emitter Saturation Voltage $T_C = 100^\circ C$	$V_{BE(sat)}$	—	1.5	—	V	$I_C = 10A, I_B = 1A$
DC Current Gain	η_{FE}	5.0	—	—		$I_C = 15A, V_{CE} = 5V$
Dynamic Characteristics						
Output Capacitance	C_{obo}	—	—	400	pF	$V_{CB} = 10V, I_E = 0,$ $f_{test} = 1.0kHz$
Switching Characteristics						
Resistive Switching Speeds Turn on Time Storage Time (Note 2) Fall Time (Note 2)	t_{on} t_s t_f	— — —	220 900 150	— — —	ns ns ns	$I_C = 10A$ $V_{CC} = 250V$ $I_{B1} = 1A$ $I_{B2} = 2A, R_B = 1.6\Omega$
Storage Time (Note 2) Fall Time (Note 2)	t_s t_f	— —	500 40	— —	ns ns	$I_C = 10A$ $V_{CC} = 250V$ $I_{B1} = 1A$ $I_{B2} = 2A, R_B = 1.6\Omega$ $V_{BE(off)} = 5V$
Inductive Switching Speeds $T_C = 100^\circ C$ Storage Time Fall Time Crossover Time	t_{sv} t_{fi} t_c	— — —	650 30 50	1500 150 200	ns ns ns	$I_C = 10A$ $I_{B1} = 1A$ $V_{BE(off)} = 5V$ $V_{CE(pk)} = 400V$
$T_C = 150^\circ C$ Storage Time Fall Time Crossover Time	t_{sv} t_{fi} t_c	— — —	850 30 70	— — —	ns ns ns	$I_C = 10A$ $I_{B1} = 1A$ $V_{BE(off)} = 5V$ $V_{CE(pk)} = 400V$

Notes: 1. Pulse Test — Pulse Width = 300 μ s, Duty Cycle < 2%.
2. Pulse Test — Pulse Width = 30 μ s, Duty Cycle < 2%.

TYPICAL DYNAMIC CHARACTERISTICS



TYPICAL DYNAMIC CHARACTERISTICS



POWER TRANSISTORS

30A, 400V, NPN Mesa

UMT2003

FEATURES

- Collector Emitter Voltage: 850V
 - Peak Collector Current: 60A
 - Storage Time $\leq 3\mu\text{s}$
 - Fall Time $\leq 0.8\mu\text{s}$
- } at $I_c = 20A$

DESCRIPTION

These high voltage, multiple layer epitaxial, glass passivated power transistors combine fast switching, low saturation voltage and rugged second-breakdown capability. They are designed for use in off-line power supplies, high voltage inverters and switching regulators.

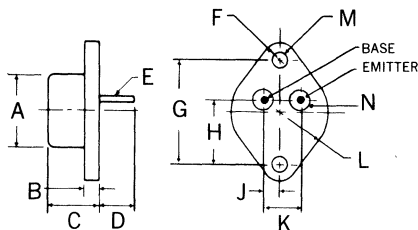
ABSOLUTE MAXIMUM RATINGS

Collector Emitter Voltage, V_{CEV}	850V
Collector Emitter Voltage, $V_{CEO(SUS)}$	400V
Emitter Base Voltage, V_{EBO}	7V
Collector Current, I_c continuous	30A
Collector Current, I_{CM} peak	60A
Base Current, I_b continuous	8A
Base Current, I_{BM} peak	30A
Power Dissipation, 25°C Case	250W
Junction Temperature	+200°C
Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.7°C/W

MECHANICAL SPECIFICATIONS

NOTE:

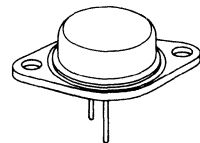
Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



UMT2003

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.043 DIA.	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.057-.063	1.45-1.60 DIA
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA	3.84-4.09 DIA
N	.190-.210	4.83-5.33

TO-204AA (TO-3)

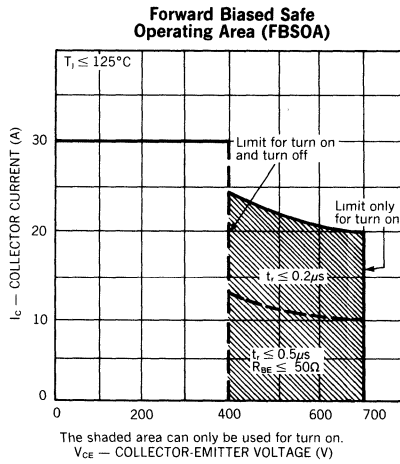
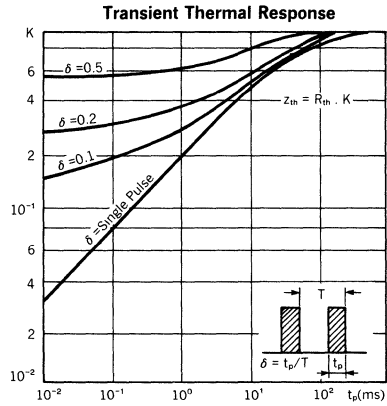
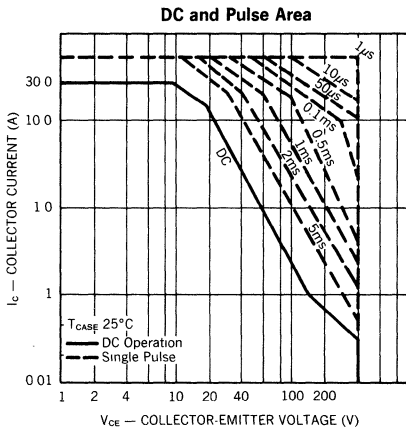


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

TEST	SYMBOL				UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Off Characteristics						
Collector Emitter Sustaining Voltage	$V_{CE(sus)}$	400	—	—	V	$I_C = 0.2A, I_B = 0$ $L = 25mH$
Emitter Base Voltage	V_{EBO}	7	—	30	V	$I_C = 0A, I_B = 0.1A$
Collector Cutoff Current $T_C = 25^\circ C$	I_{CEX}	—	—	0.4	mA	$V_{CE} = V_{CEX}$ $V_{BE} = -2.5V$
Collector Cutoff Current $T_C = 125^\circ C$	I_{CEX}	—	—	4	mA	$V_{CE} = V_{CEX}$ $V_{BE} = -2.5V$
Collector Cutoff Current $T_C = 25^\circ C$	I_{CER}	—	—	1	mA	$V_{CE} = V_{CEX}$ $R_{BE} \leq 5\Omega$
Collector Cutoff Current $T_C = 125^\circ C$	I_{CER}	—	—	8	mA	$V_{CE} = V_{CEX}$ $R_{BE} \leq 5\Omega$
Emitter Cutoff Current	I_{EBO}	—	—	2	mA	$V_{EB} = 5V, I_C = 0$
On Characteristics (Note 1)						
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	1.5	V	$I_C = 20A, I_B = 4A$
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	3.5	V	$I_C = 30A, I_B = 8A$
Base Emitter Saturation	$V_{BE(sat)}$	—	—	1.6	V	$I_C = 20A, I_B = 4A$
Dynamic Characteristics						
Gain-Bandwidth Product	f_T	—	5	—	MHz	$V_{CE} = 10V, I_C = 1A$ $f = 1MHz$
Output Capacitance	C_{obo}	—	500	—	pF	$V_{CE} = 10V, f = 1MHz$
Switching Characteristics						
Resistive Switching Speeds Turn On Time Storage Time Fall Time	t_{on} t_s t_f	— — —	0.55 1.5 0.3	1 3 0.8	μs μs μs	$I_C = 20A$ $V_{CC} = 150V$ $I_{B1} = -I_{B2} = 4A$
Inductive Switching Speeds $T_i = 25^\circ C$ Storage Time Fall Time	t_s t_f	— —	3.5 0.08	— —	μs μs	$I_C = 20A, I_{B(lead)} = 4A$ $L_B = 50\mu H$ $V_{CC} = 300V, -V_{BE} = 5V$
Inductive Switching Speeds $T_i = 100^\circ C$ Storage Time Fall Time	t_s t_f	— —	— —	5 0.4	μs μs	$I_C = 20A, I_{B(lead)} = 4A$ $L_B = 1.5\mu H$ $V_{CC} = 30V, -V_{BE} = 5V$

Note: 1. $t_p = 300\mu s$; duty cycle $\leq 2\%$.





POWER TRANSISTORS

4A, 700V, Fast Switching,
Silicon NPN Mesa

UMT13004
UMT13005

4

FEATURES

- Collector Emitter Voltage: up to 700V
- Peak Collector Current: 8A
- Rise Time: $\leq 7\mu\text{S}$
- Fall Time: $\leq 0.9\mu\text{S}$ } at $I_C = 2\text{A}$
- Key Parameters characterized at 100°C
- Economical Plastic Molded Construction

DESCRIPTION

These high voltage glass passivated power transistors, in a plastic TO-220AB package, combine fast switching, low saturation voltage and rugged $E_{S/B}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, deflection circuits, motor controls and solenoid/relay drivers.

ABSOLUTE MAXIMUM RATINGS

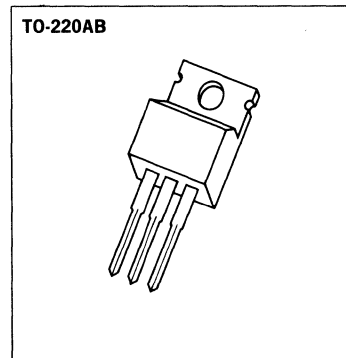
	UMT13004	UMT13005
Collector Emitter Voltage, V_{CEV}	600V	700V
Collector Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter Base Voltage, V_{EBO}	9V	9V
Collector Current, I_C continuous	4A	4A
Collector Current, I_{CM} peak	8A	8A
Base Current, I_B continuous	2A	2A
Power Dissipation, 25°C Case	75W	75W
Derating Factor	0.59W/°C	0.59W/°C
Operating and Storage Temperature Range	-65 to 150°C	

MECHANICAL SPECIFICATIONS

UMT13004, UMT13005

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	UMT13004		UMT13005		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	10	60	10	60		$I_C = 1.0A, V_{CE} = 5V$
D.C. Current Gain (Note 1)	h_{FE}	8	40	8	40		$I_C = 2.0A, V_{CE} = 5V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	.5	—	.5	V	$I_C = 1.0A, I_B = 0.2A$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	0.6	—	0.6	V	$I_C = 2.0A, I_B = 0.5A$
		—	1.0	—	1.0		
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 4.0A, I_B = 1.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.2	—	1.2	V	$I_C = 1.0A, I_B = 0.2A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 2.0A, I_B = 0.5A$
		—	1.5	—	1.5		
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 10mA$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$
Collector Cutoff Current	I_{CEV}	—	1	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$
		—	—	—	1		$V_{CE} = 700V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	5	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$
		—	—	—	5		$V_{CE} = 700V, V_{BE} = -1.5V$
Output Capacitance, Common Base	C_{ob0}	65 typ.		65 typ.		pF	$V_{CB} = 10V, f = 1 MHz$
Gain-Bandwidth Product	F_T	4	—	4	—	MHz	$V_{CE} = 10V, I_C = .5A, f = 1 MHz$
Resistive Switching Speeds	Delay Time	t_d	—	0.1	—	0.1	$I_C = 2.0A$ $V_{CC} = 125V$ $I_{B1} = I_{B2} = 0.4A$ $V_{BE(off)} = 5V, P.W. = 25\mu S$
	Rise Time	t_r	—	0.7	—	0.7	
	Storage Time	t_s	—	3.5	—	3.5	
	Fall Time	t_f	—	0.9	—	0.9	
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	t_s	—	4.0	—	4.0	$I_C = 2.0A, L = 500\mu H$ $I_{B1} = 0.4A, V_{BE(off)} = 5V$ $V_{CE} \text{ clamp} = \text{rated } V_{CE(sus)}$
	Fall Time ($t_{fi} + t_{fv}$)	t_f	—	0.9	—	0.9	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.67	—	1.67	$^\circ C/W$	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	—	62.5	—	62.5	$^\circ C/W$	

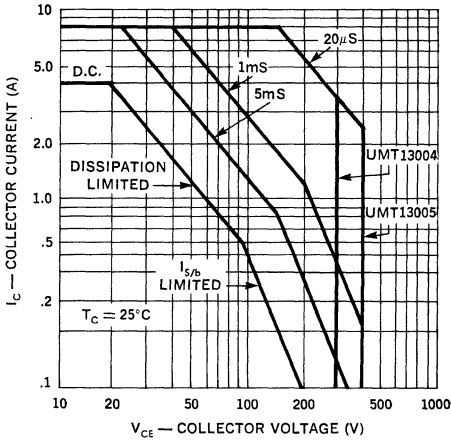
Notes:

- Pulse width = 250 μ S; duty cycle \leq 1%.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length \approx 50 μ S; duty cycle \leq 1%. Voltage clamped at maximum collector-emitter voltage.

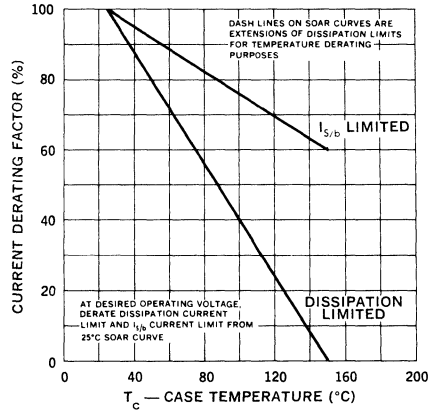
Typical Inductive Load Switching Performance

I_C Amps	T_J $^\circ C$	t_i μS	t_r nS	t_{fi} nS
0.5	25	1.8	180	20
	100	1.2	240	30
1.0	25	1.0	160	21
	100	1.5	220	30
2.0	25	1.2	180	25
	100	1.7	230	35

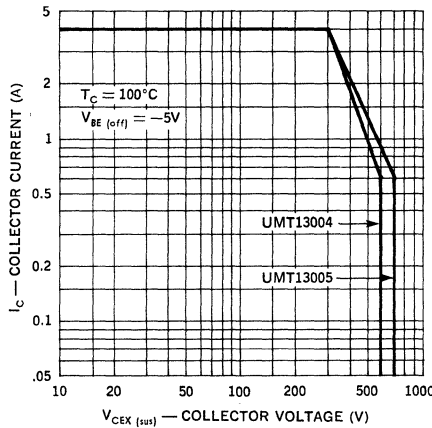
Forward Bias Safe Operating Area



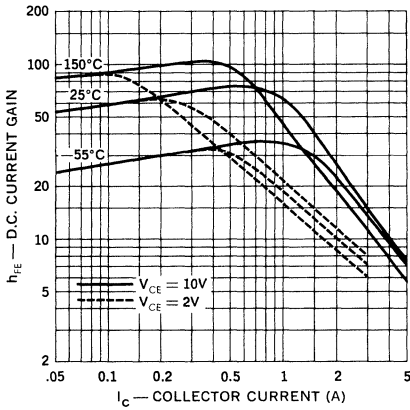
Power Derating



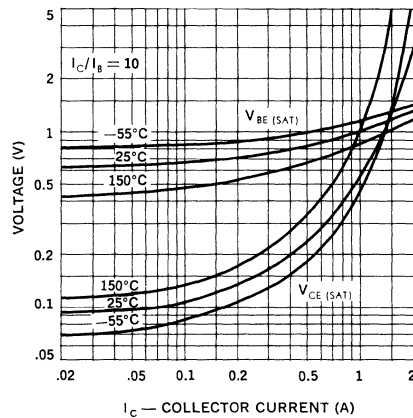
Reverse Biased Safe Operating Area



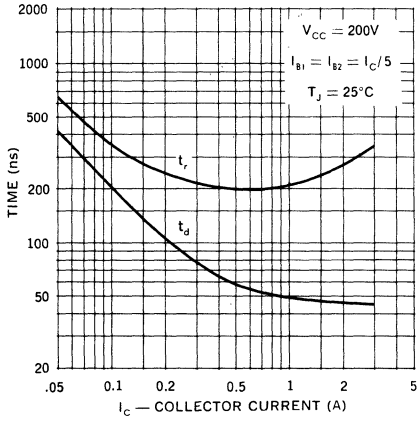
D.C. Current Gain



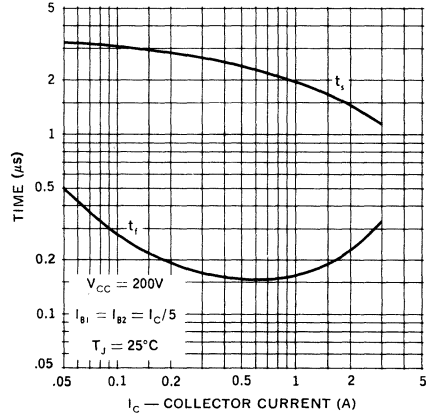
Saturation Voltages



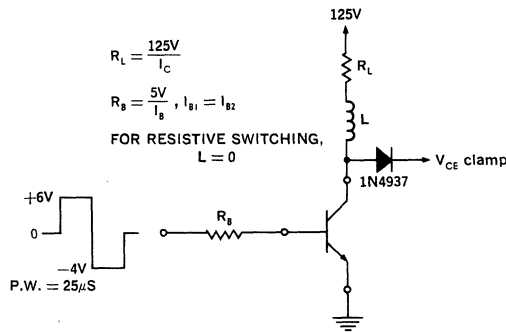
Resistive Turn-On Time



Resistive Turn-Off Time



Switching Time Test Circuit



POWER TRANSISTORS

8A, 700V, Fast Switching,
Silicon NPN Mesa

UMT13006
UMT13007

4

FEATURES

- Collector Emitter Voltage: up to 700V
- Peak Collector Current: 16A
- Rise Time: $\leq 1.0\mu\text{S}$
- Fall Time: $\leq 0.7\mu\text{S}$
- Key Parameters characterized at 100°C
- Economical Plastic Molded Construction

DESCRIPTION

These high voltage glass passivated power transistors, in a plastic TO-220AB package, combine fast switching, low saturation voltage and rugged E_s/I_b capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, deflection circuits, motor controls and solenoid/relay drivers

ABSOLUTE MAXIMUM RATINGS

	UMT13006	UMT13007
Collector Emitter Voltage, V_{CEV}	600V	700V
Collector Emitter Voltage, V_{CEO} (SUS)	300V	400V
Emitter Base Voltage, V_{EBO}	8V	8V
Collector Current, I_C continuous	8A	8A
Collector Current, I_{CM} peak	16A	16A
Base Current, I_B continuous	4A	4A
Power Dissipation, 25°C Case	80W	80W
Derating Factor	0.641W/°C	0.641W/°C
Operating and Storage Temperature Range	-65 to 150°C	

MECHANICAL SPECIFICATIONS

SEATING PLANE

PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

UMT13006, UMT13007

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

TO-220AB

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	UMT13006		UMT13007		Units	Test Conditions
		MIN.	MAX.	MIN.	MAX.		
D.C. Current Gain (Note 1)	h_{FE}	8	40	8	40		$I_C = 2.0A, V_{CE} = 5V$
D.C. Current Gain (Note 1)	h_{FE}	6	30	6	30		$I_C = 5.0A, V_{CE} = 5V$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 2.0A, I_B = 0.4A$
Collector Saturation Voltage (Note 1) $T_C = 25^\circ C$ $T_C = 100^\circ C$	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 5.0A, I_B = 1.0A$
		—	2.0	—	2.0		
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	3.0	—	3.0	V	$I_C = 8.0A, I_B = 2.0A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.2	—	1.2	V	$I_C = 2.0A, I_B = 0.4A$
Base Saturation Voltage (Note 1) $T_C = 25^\circ C$ $T_C = 100^\circ C$	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 5.0A, I_B = 1.0A$
		—	1.5	—	1.5		
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 10mA$
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$
Collector Cutoff Current	I_{CEV}	—	1.0	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$
		—	—	—	1.0		$V_{CE} = 700V, V_{BE} = -1.5V$
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	5	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$
		—	—	—	5		$V_{CE} = 700V, V_{BE} = -1.5V$
Output Capacitance, Common Base	C_{obo}	110 typ.		110 typ.		pF	$V_{CB} = 10V, f = 1 MHz$
Gain-Bandwidth Product	F_T	4	—	4	—	MHz	$V_{CE} = 10V, I_C = 0.5A, f = 1 MHz$
Resistive Switching Speeds	Delay Time	—	0.1	—	0.1	μS	$I_C = 5.0A$ $V_{CC} = 125V$ $I_{B1} = I_{B2} = 1A$ $V_{BE(off)} = 5V$
	Rise Time	—	1.0	—	1.0		
	Storage Time	—	3.0	—	3.0		
	Fall Time	—	0.7	—	0.7		
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	—	2.3	—	2.3	μS	$I_C = 5.0A, V_{BE(off)} = 5V$ $I_{B1} = 1A$ $V_{CE\ clamp} = \text{rated } V_{CE(sus)}$
	Fall Time ($t_{fi} + t_{fv}$)	—	0.7	—	0.7		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.56	—	1.56	$^\circ C/W$	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	—	62.5	—	62.5	$^\circ C/W$	

Notes:

- Pulse width = 250 μS ; duty cycle $\leq 1\%$.
- Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

**Typical
Inductive Load
Switching Performance**

Conditions:

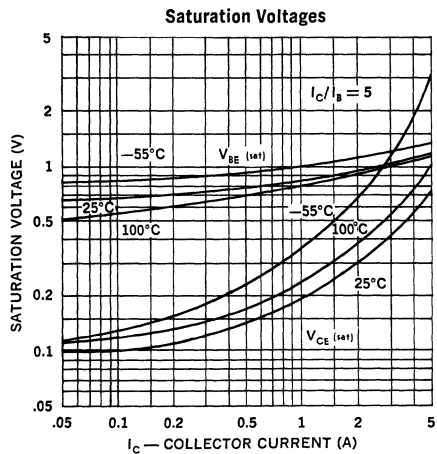
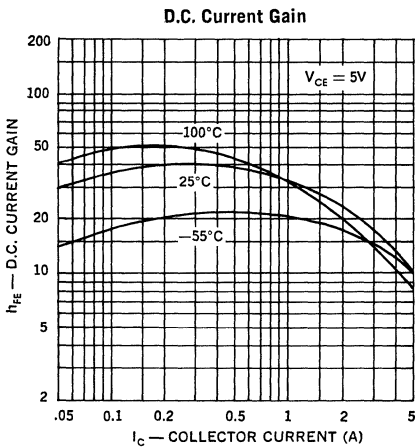
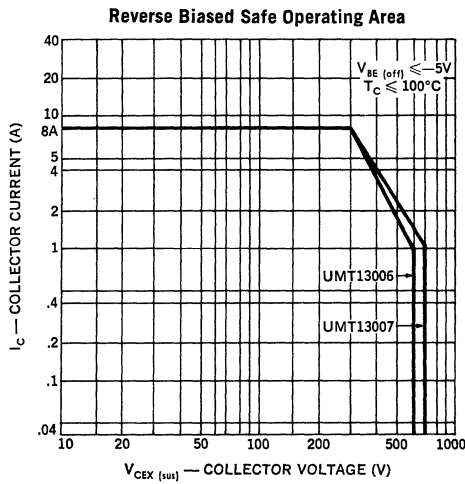
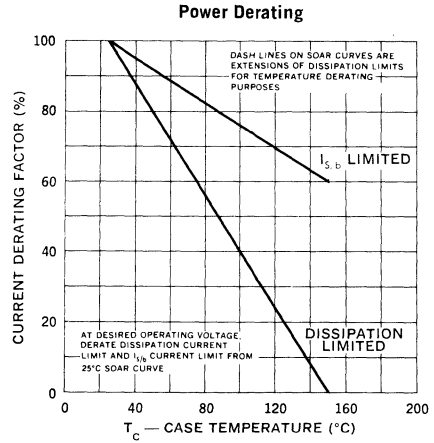
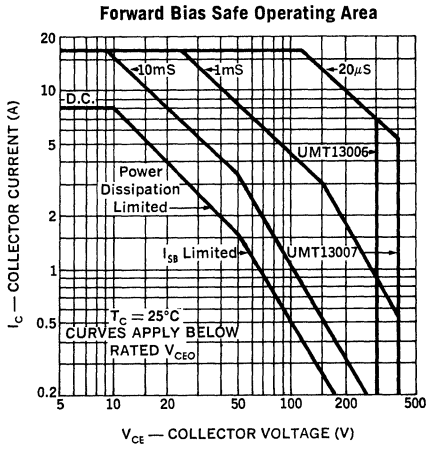
$$\frac{I_C}{I_{B1}} = 5$$

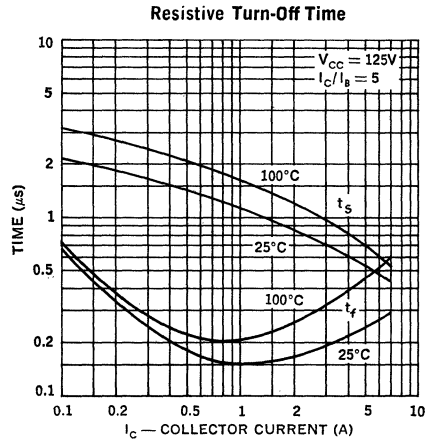
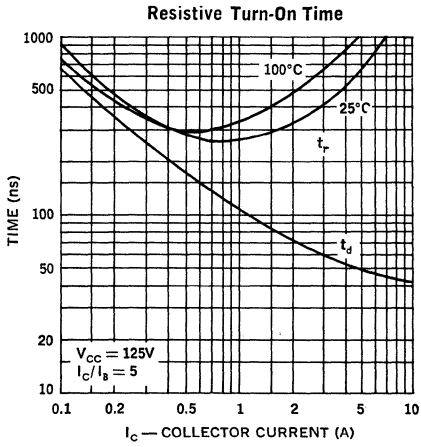
 V_{clamp} at rated $V_{CE(sus)}$

(refer to RBSOA curve)

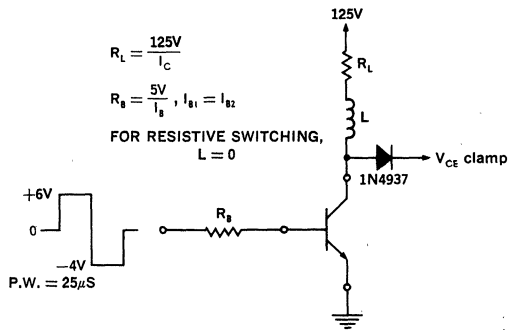
$$V_{BE(off)} = -5V$$

I_C Amps	T_J $^\circ C$	t_s μS	t_{fv} nS	t_{fi} nS
3.0	25	.45	70	10
	100	.575	100	20
5.0	25	.475	25	4
	100	.60	45	10
8.0	25	.525	20	10
	100	.625	45	15





Switching Time Test Circuit



POWER TRANSISTORS

12A, 700V, Fast Switching,
Silicon NPN Mesa

UMT13008
UMT13009

4

FEATURES

- Collector Emitter Voltage: up to 700V
- Peak Collector Current: 24A
- Rise Time: $\leq 1.0\mu\text{S}$
- Fall Time: $\leq 0.7\mu\text{S}$
- Key Parameters characterized at 100°C
- Economical Plastic Molded Construction

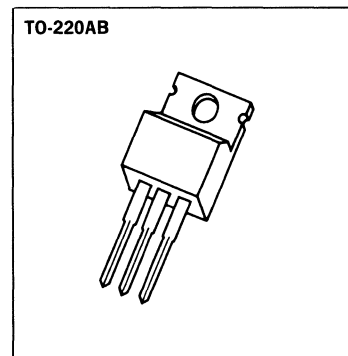
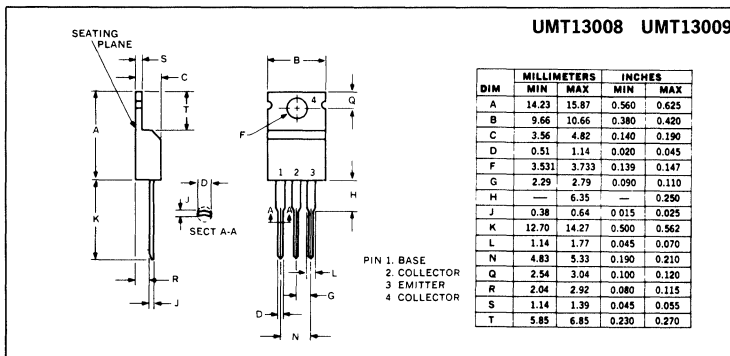
DESCRIPTION

These high voltage glass passivated power transistors, in a plastic TO-220AB package, combine fast switching, low saturation voltage and rugged $E_{S/b}$ capability. They are designed for use in off-line power supplies, high voltage inverters, switching regulators, deflection circuits, motor controls and solenoid/relay drivers.

ABSOLUTE MAXIMUM RATINGS

	UMT13008	UMT13009
Collector Emitter Voltage, V_{CEV}	600V	700V
Collector Emitter Voltage, V_{CEO} (sus)	300V	400V
Emitter Base Voltage, V_{EBO}	9V	9V
Collector Current, I_C continuous	12A	12A
Collector Current, I_{CM} peak	24A	24A
Base Current, I_B continuous	6A	6A
Power Dissipation, 25°C Case	100W	100W
Derating Factor	0.80W/°C	0.80W/°C
Operating and Storage Temperature Range	-65 to 150°C	

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	UMT13008		UMT13009		Units	Test Conditions	
		MIN.	MAX.	MIN.	MAX.			
D.C. Current Gain (Note 1)	h_{FE}	8	40	8	40		$I_C = 5.0A, V_{CE} = 5V$	
D.C. Current Gain (Note 1)	h_{FE}	6	30	6	30		$I_C = 8.0A, V_{CE} = 5V$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 5.0A, I_B = 1.0A$	
Collector Saturation Voltage (Note 1) $T_C = 25^\circ C$ $T_C = 100^\circ C$	$V_{CE(sat)}$	—	1.5	—	1.5	V	$I_C = 8.0A, I_B = 1.6A$	
		—	2.0	—	2.0			
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	3.0	—	3.0	V	$I_C = 12.0A, I_B = 3A$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.2	—	1.2	V	$I_C = 5.0A, I_B = 1.0A$	
Base Saturation Voltage (Note 1) $T_C = 25^\circ C$ $T_C = 100^\circ C$	$V_{BE(sat)}$	—	1.6	—	1.6	V	$I_C = 8.0A, I_B = 1.6A$	
		—	1.5	—	1.5			
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	300	—	400	—	V	$I_C = 10mA$	
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9V$	
Collector Cutoff Current	I_{CEV}	—	1.0	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$	
		—	—	—	1.0		$V_{CE} = 700V, V_{BE} = -1.5V$	
Collector Cutoff Current, $T_C = 100^\circ C$	I_{CEV}	—	5.0	—	—	mA	$V_{CE} = 600V, V_{BE} = -1.5V$	
		—	—	—	5.0		$V_{CE} = 700V, V_{BE} = -1.5V$	
Output Capacitance, Common Base	C_{obo}	180 typ.		180 typ.		pF	$V_{CB} = 10V, f = 1 MHz$	
Gain-Bandwidth Product	F_T	4	—	4	—	MHz	$V_{CE} = 10V, I_C = 0.5A, f = 1 MHz$	
Resistive Switching Speeds	Delay Time	t_d	—	0.1	—	0.1	μS	$I_C = 8.0$ $V_{CC} = 125V$ $I_{B1} = I_{B2} = 1.6A$ $V_{BE(off)} = 5V$
	Rise Time	t_r	—	1.0	—	1.0		
	Storage Time	t_s	—	3.0	—	3.0		
	Fall Time	t_f	—	0.7	—	0.7		
Inductive Switching Speeds $T_C = 100^\circ C$	Storage Time	t_s	—	2.3	—	2.3	μS	$I_C = 8A, V_{BE(off)} = 5V$ $I_{B1} = 1.6A$ $V_{CE\ clamp} = \text{rated } V_{CEX(sus)}$
	Fall Time ($t_{fi} + t_{fv}$)	t_f	—	0.7	—	0.7		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	1.25	—	1.25	$^\circ C/W$		
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	—	62.5	—	62.5	$^\circ C/W$		

Notes:

1. Pulse width = 250 μS ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length $\approx 50\mu S$; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.

Typical Inductive Load Switching Performance

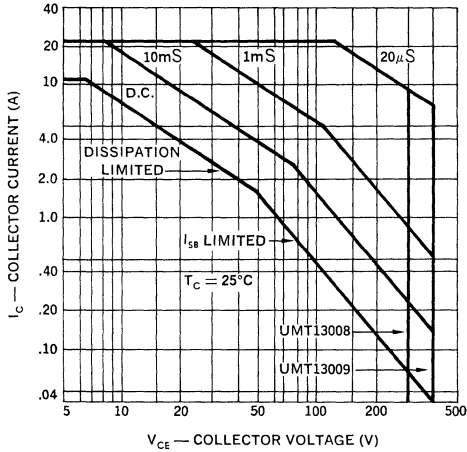
Conditions:

$$\frac{I_C}{I_{B1}} = 5$$

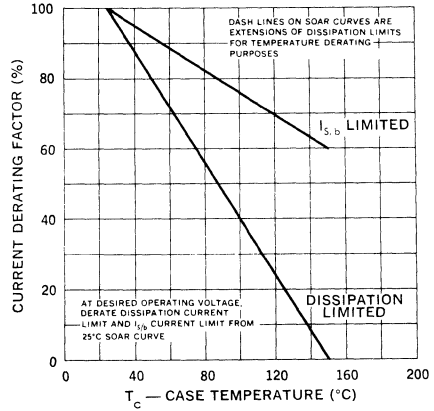
V_{clamp} at rated $V_{CEX(sus)}$
(refer to RBSOA curve)
 $V_{BE(off)} = -5V$

I_C Amps	T_J $^\circ C$	t_s μS	t_{fv} nS	t_{fi} nS
3.0	25	0.5	100	10
	100	0.85	130	14
5.0	25	0.65	40	10
	100	0.90	50	12
8.0	25	0.72	60	12
	100	.092	65	28
12.0	25	.70	70	25
	100	.78	70	110

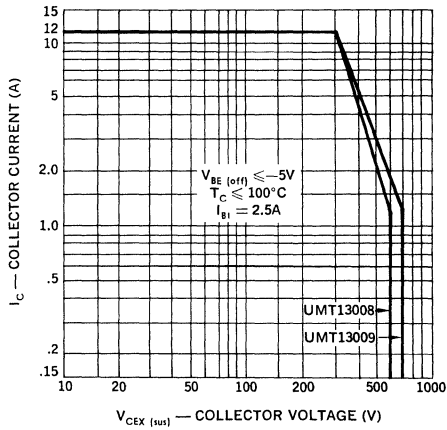
Forward Bias Safe Operating Area



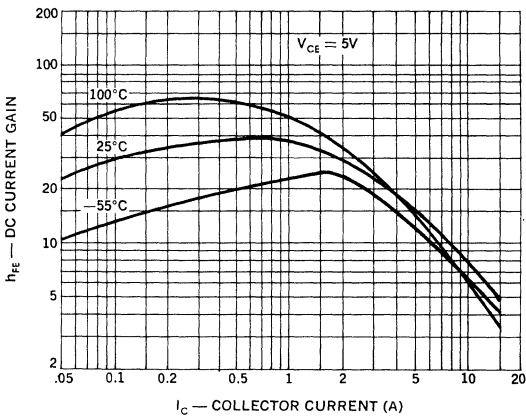
Power Derating



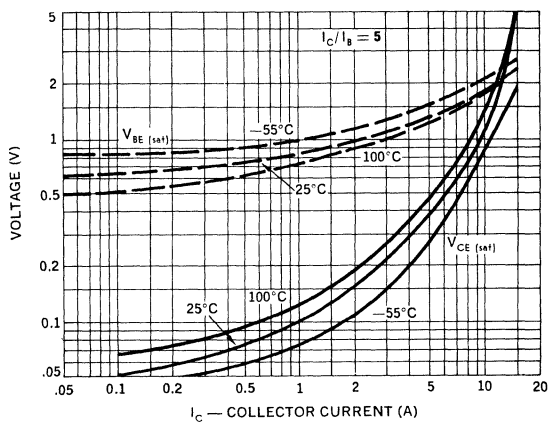
Reverse Biased Safe Operating Area

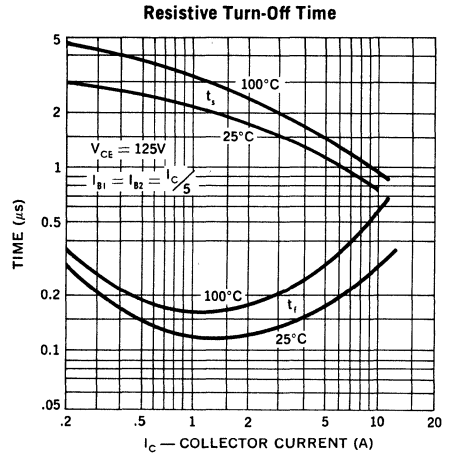
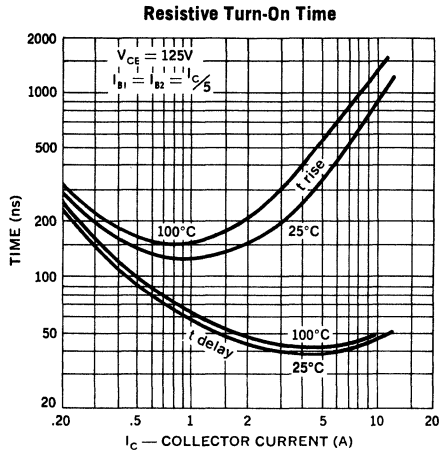


D.C. Current Gain

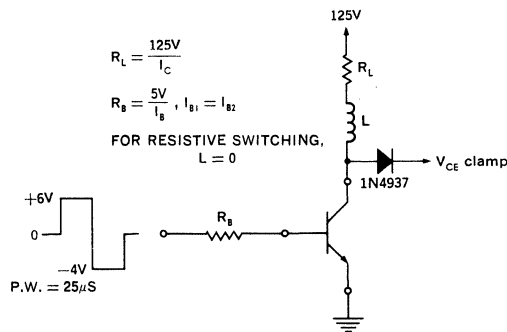


Saturation Voltages





Switching Time Test Circuit



POWER TRANSISTORS

1 Amp, 150V, Planar NPN

UPT111
UPT112
UPT113
UPT114
UPT115

FEATURES

- Collector-Base Voltage: up to 150V
- Peak Collector Current: 2A
- Turn-on Time: 100ns
- Turn-off Time: 250ns

DESCRIPTION

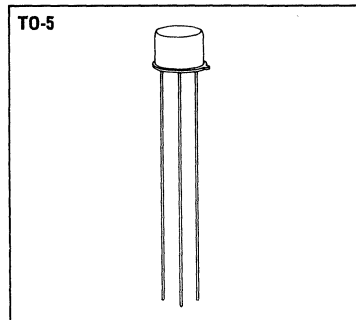
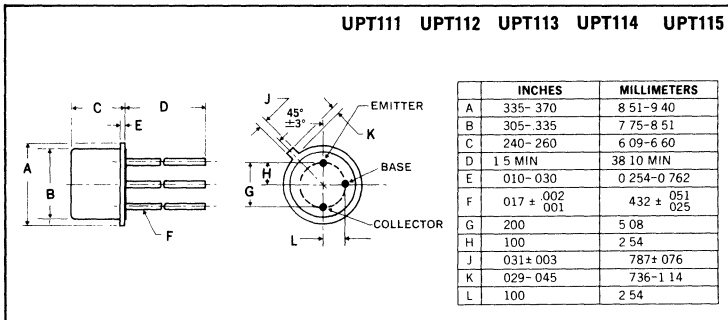
Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply pulse amplifier and similar high efficiency power switching applications.

4

ABSOLUTE MAXIMUM RATINGS

	UPT111	UPT112	UPT113	UPT114	UPT115
Collector-Base Voltage, V_{CBO}	60V	80V	100V	120V	150V
Collector-Emitter Voltage, V_{CEO}	40V	60V	80V	100V	100V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	1A	1A	1A	1A	1A
Peak Collector Current, I_C	2A	2A	2A	2A	2A
Base Current, I_B	0.5A	0.5A	0.5A	0.5A	0.5A
Power Dissipation					
25°C Ambient				.85W	
100°C Case				4W	
Thermal Resistance, θ_{J-C}				25°C/W	
Operating and Storage Temperature Range				-65°C to 200°C	

MECHANICAL SPECIFICATIONS

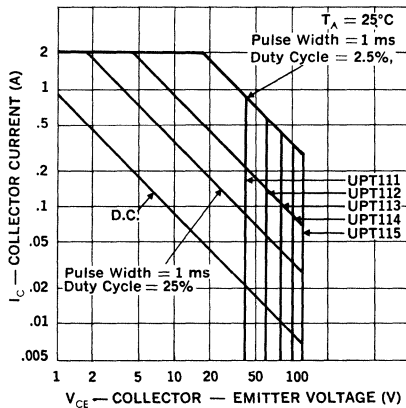


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

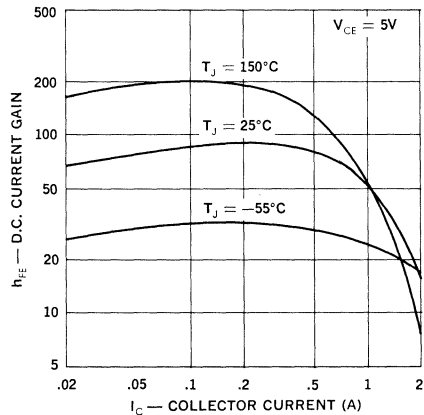
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	30	—	—	$I_C = 0.5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	20	—	—	$I_C = 1A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	15 Typ.		—	$I_C = 2A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = 1A, I_B = 0.1A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.2	Vdc	$I_C = 1A, I_B = 0.1A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}			Vdc	$I_C = 10mAdc; R_{BE} = 100\Omega$
UPT111		60	—		
UPT112		80	—		
UPT113		100	—		
UPT114		120	—		
UPT115		150	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mAdc$
UPT111		40	—		
UPT112		60	—		
UPT113		80	—		
UPT114-5		100	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	40	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	50 Typ.		MHz	$I_C = 0.1Adc, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	100 Typ.	ns	$I_C = 1A$
	Turn-off Time	t_{off}	250 Typ.	ns	

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

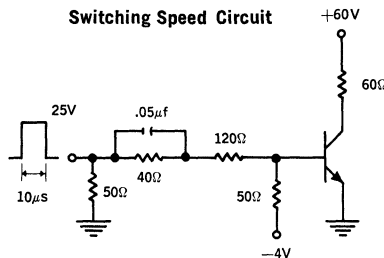
**Maximum Safe Operating Area
UPT111 - 115**



D.C. Current Gain vs. Collector Current



Switching Speed Circuit



POWER TRANSISTORS

2 Amp, 150V, Planar NPN

UPT211
UPT212
UPT213
UPT214
UPT215

FEATURES

- Collector-Base Voltage: up to 150V
- Peak Collector Current: 5A
- Turn-on Time: 130ns
- Turn-off Time: 300ns

DESCRIPTION

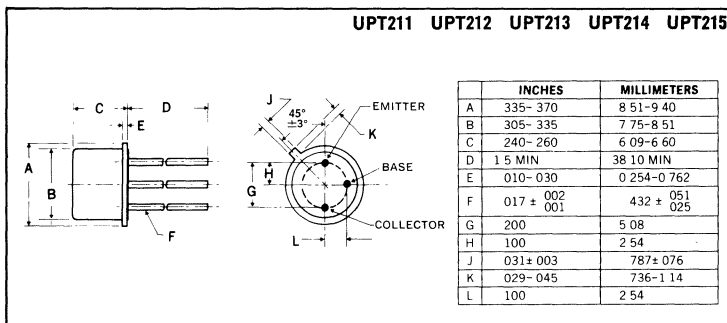
Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply, pulse amplifier and similar high efficiency power switching applications.

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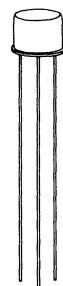
ABSOLUTE MAXIMUM RATINGS

	UPT211	UPT212	UPT213	UPT214	UPT215
Collector-Base Voltage, V_{CBO}	60V	80V	100V	120V	150V
Collector-Emitter Voltage, V_{CEO}	40V	60V	80V	100V	100V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	2A	2A	2A	2A	2A
Peak Collector Current, I_{CP}	5A	5A	5A	5A	5A
Base Current, I_B	1A	1A	1A	1A	1A
Power Dissipation					
25°C Ambient				.85W	
100°C Case				4W	
Thermal Resistance, θ_{J-C}				25°C/W	
Operating and Storage Temperature Range				-65°C to 200°C	

MECHANICAL SPECIFICATIONS



T0-5



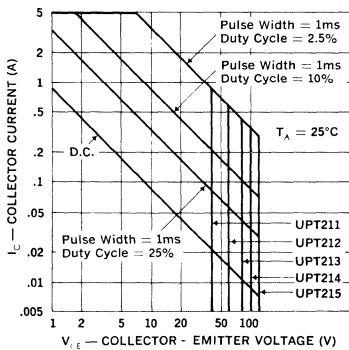
UNITRODE

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

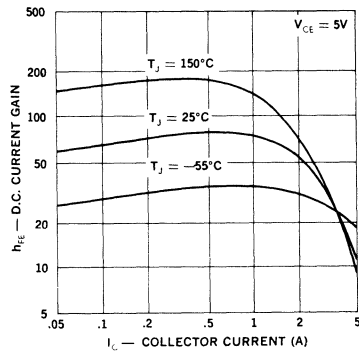
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	30	—	—	$I_C = 0.5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	20	—	—	$I_C = 2A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10 Typ.		—	$I_C = 5A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = 2A, I_B = 0.2A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.2	Vdc	$I_C = 2A, I_B = 0.2A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}			Vdc	$I_C = 10mAdc; R_{BE} = 100\Omega$
UPT211		60	—		
UPT212		80	—		
UPT213		100	—		
UPT214		120	—		
UPT215		150	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mAdc$
UPT211		40	—		
UPT212		60	—		
UPT213		80	—		
UPT214-5		100	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	40	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	70 Typ.		MHz	$I_C = 0.1Adc, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	130 Typ.	ns	$I_C = 2A$
	Turn-off Time	t_{off}	300 Typ.	ns	

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

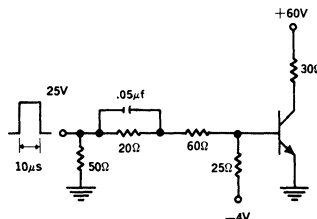
Maximum Safe Operating Area
UPT211-215



D.C. Current Gain vs. Collector Current



Switching Speed Circuit



POWER TRANSISTORS

2 Amp, 400V, Planar NPN

UPT311 UPT321
 UPT312 UPT322
 UPT313 UPT323
 UPT314 UPT324
 UPT315 UPT325

FEATURES

- Collector-Base Voltage: up to 400V
- Peak Collector Current: 3A
- Turn-on Time: 200 ns
- Turn-off Time: 800 ns

DESCRIPTION

Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

4

ABSOLUTE MAXIMUM RATINGS

	UPT311 UPT321	UPT312 UPT322	UPT313 UPT323	UPT314 UPT324	UPT315 UPT325
Collector-Base Voltage, V_{CBO}	200V	250V	300V	350V	400V
Collector-Emitter Voltage, V_{CEO}	150V	200V	250V	300V	300V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	2A	2A	2A	2A	2A
Peak Collector Current, I_{C}	3A	3A	3A	3A	3A
Base Current, I_B	1A	1A	1A	1A	1A
Power Dissipation			UPT311-315	UPT321-325	
25°C Ambient			1W	2W	
100°C Case			10W	16W	
Thermal Resistance, θ_{J-C}			10°C/W	6.7°C/W	
Operating and Storage Temperature Range			-65°C to 200°C	-65°C to 200°C	

MECHANICAL SPECIFICATIONS

UPT311 UPT312 UPT313 UPT314 UPT315

	INCHES	MILLIMETERS
A	335-370	8.51-9.40
B	305-335	7.75-8.51
C	240-260	6.09-6.60
D	1.5 MIN.	38.10 MIN.
E	0.10-0.30	0.254-0.762
F	0.17 ± 0.02 0.001	4.32 ± 0.51 0.025
G	200	5.08
H	100	2.54
J	0.31 ± 0.03	7.87 ± 0.76
K	0.29-0.45	7.36-1.14
L	100	2.54

TO-5

UPT321 UPT322 UPT323 UPT324 UPT325

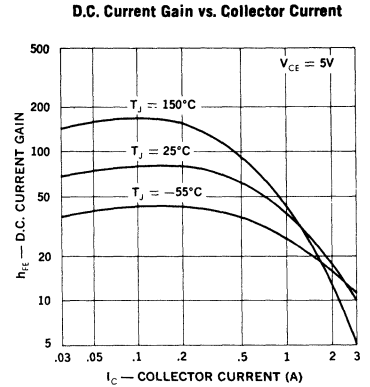
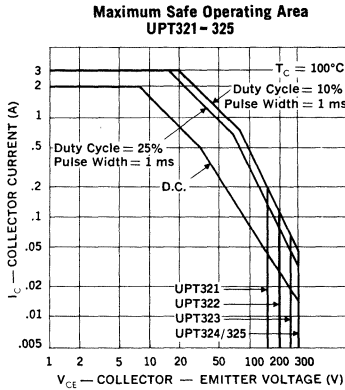
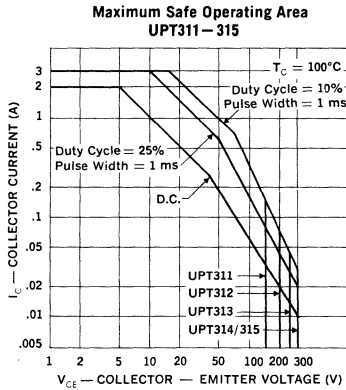
	INCHES	MILLIMETERS
A	620 MAX.	15.75 MAX.
B	.050 - .075	1.27 - 1.90
C	.250 - .340	6.35 - 8.63
D	.360 MIN.	9.14 MIN.
E	.028 - .034 DIA.	.711 - .863
F	.958 - .962	24.33 - 24.43
G	.570 - .590	14.47 - 14.98
H	145 MAX. RAD.	3.68 MAX. RAD.
J	142 - .152 DIA.	3.60 - 3.86 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190 - .210	4.82 - 5.33
M	.093 - .107	2.36 - 2.72

TO-66

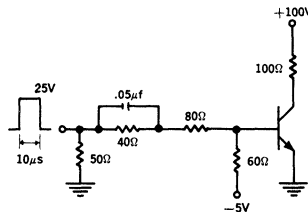
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	30	—	—	$I_C = 0.5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10	—	—	$I_C = 2A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10 Typ.		—	$I_C = 3A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE}(sat)$	—	1.0	Vdc	$I_C = 2A, I_B = 0.4A$
Base Saturation Voltage (Note 1)	$V_{BE}(sat)$	—	1.5	Vdc	$I_C = 2A, I_B = 0.4A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}			Vdc	$I_C = 10mA; R_{BE} = 100\Omega$
UPT311, UPT321		200	—		
UPT312, UPT322		250	—		
UPT313, UPT323		300	—		
UPT314, UPT324		350	—		
UPT315, UPT325		400	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mA$
UPT311, UPT321		150	—		
UPT312, UPT322		200	—		
UPT313, UPT323		250	—		
UPT314-5, UPT324-5		300	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μ Adc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μ Adc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	50	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	40 Typ.		MHz	$I_C = 0.5Adc, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	200 Typ.	ns	$I_C = 1A$
	Turn-off Time	t_{off}	800 Typ.	ns	

Note: 1. Pulse width = 300 μ s; duty cycle \leq 2%.



Switching Speed Circuit



POWER TRANSISTORS

3 Amp, 400V, Planar NPN

UPT521
UPT522
UPT523
UPT524
UPT525

FEATURES

- Collector-Base Voltage: up to 400V
- Peak Collector Current: 5A
- Turn-on Time: 200ns
- Turn-off Time: 900ns

DESCRIPTION

Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

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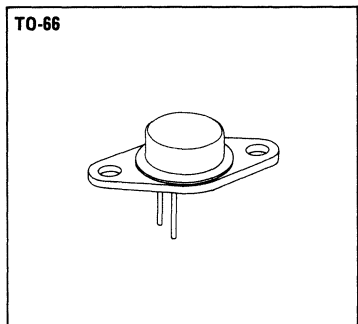
ABSOLUTE MAXIMUM RATINGS

	UPT521	UPT522	UPT523	UPT524	UPT525
Collector-Base Voltage, V_{CBO}	200V	250V	300V	350V	400V
Collector-Emitter Voltage, V_{CEO}	150V	200V	250V	300V	300V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	3A	3A	3A	3A	3A
Peak Collector Current, I_{C}	5A	5A	5A	5A	5A
Base Current, I_B	2A	2A	2A	2A	2A
Power Dissipation					
25°C Ambient			2W		
100°C Case			25W		
Thermal Resistance, θ_{J-C}			4°C/W		
Operating and Storage Temperature Range			-65°C to 200°C		

MECHANICAL SPECIFICATIONS

UPT521 UPT522 UPT523 UPT524 UPT525

	INCHES	MILLIMETERS
A	.620 MAX.	15.75 MAX.
B	.050 - .075	1.27 - 1.90
C	.250 - .340	6.35 - 8.63
D	.350 MIN.	9.14 MIN.
E	.028 - .034 DIA.	.711 - .863
F	.958 - .962	24.33 - 24.43
G	.570 - .590	14.47 - 14.98
H	.145 MAX. RAD.	3.68 MAX. RAD.
J	.142 - .152 DIA.	3.60 - 3.86 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190 - .210	4.82 - 5.33
M	.093 - .107	2.36 - 2.72

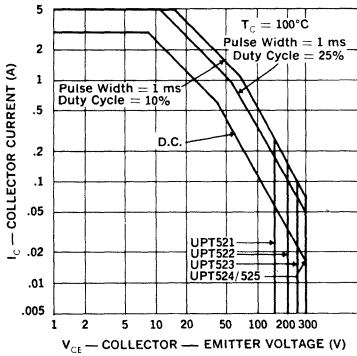


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

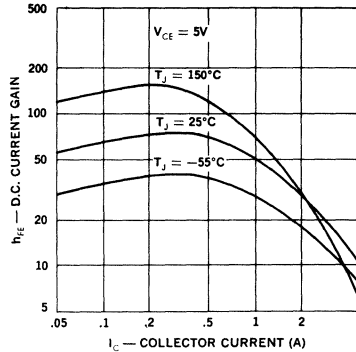
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	25	—	—	$I_C = 1.0A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10	—	—	$I_C = 3A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10 Typ.		—	$I_C = 5A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = 3A, I_B = 0.6A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	Vdc	$I_C = 3A, I_B = 0.6A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}			Vdc	$I_C = 10mA; R_{BE} = 100\Omega$
UPT521		200	—		
UPT522		250	—		
UPT523		300	—		
UPT524		350	—		
UPT525		400	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mA$
UPT521		150	—		
UPT522		200	—		
UPT523		250	—		
UPT524-5		300	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μA	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mA	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μA	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	120	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	30 Typ.		MHz	$I_C = 0.5A, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	200 Typ.	ns	$I_C = 3A$
	Turn-off Time	t_{off}	900 Typ.	ns	

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

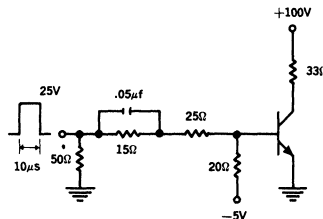
Maximum Safe Operating Area



D.C. Current Gain vs. Collector Current



Switching Speed Circuit



POWER TRANSISTORS

5 Amp, 150V, Planar NPN

UPT611
UPT612
UPT613
UPT614
UPT615

FEATURES

- Collector-Base Voltage: up to 150V
- Peak Collector Current: 10A
- Turn-on Time: 250ns
- Turn-off Time: 550ns

DESCRIPTION

Unitrode power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for power supply, pulse amplifier and similar high efficiency power switching applications.

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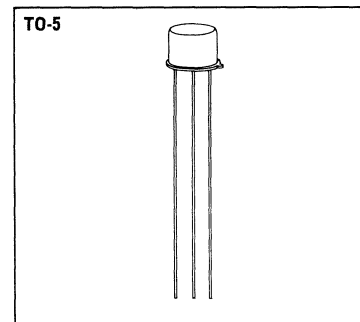
ABSOLUTE MAXIMUM RATINGS

	UPT611	UPT612	UPT613	UPT614	UPT615
Collector-Base Voltage, V_{CB0}	60V	80V	100V	120V	150V
Collector-Emitter Voltage, V_{CEO}	40V	60V	80V	100V	100V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	5A	5A	5A	5A	5A
Peak Collector Current, I_{C}	10A	10A	10A	10A	10A
Base Current, I_b	2A	2A	2A	2A	2A
Power Dissipation					
25°C Ambient			1W		
100°C Case			5W		
Thermal Resistance, θ_{J-C}			20°C/W		
Operating and Storage Temperature Range			-65°C to 200°C		

MECHANICAL SPECIFICATIONS

UPT611 UPT612 UPT613 UPT614 UPT615

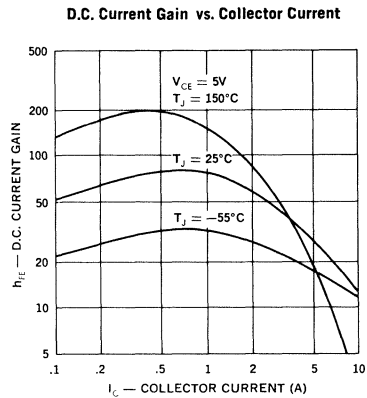
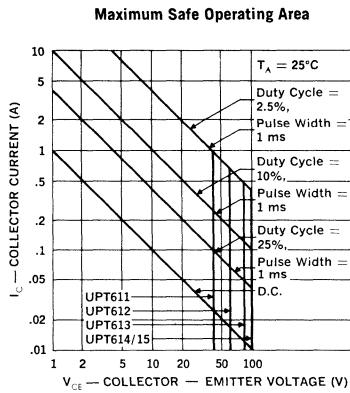
	INCHES	MILLIMETERS
A	.335- .370	8.51-9.40
B	.305- .335	7.75-8.51
C	.240- .260	6.09-6.60
D	1.5 MIN	38.10 MIN.
E	.010- .030	0.254-0.762
F	.017 ± .002 .001	.432 ± .051 .025
G	.200	5.08
H	.100	2.54
J	.031± .003	.787± .076
K	.029- .045	.736-1.14
L	.100	2.54



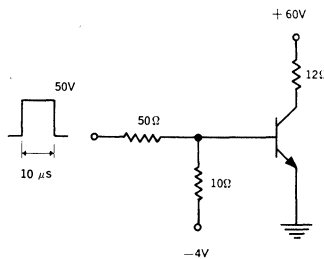
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	30	—	—	$I_C = 1A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	15	—	—	$I_C = 5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	12 Typ.		—	$I_C = 10A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = 5A, I_B = 0.5A$
UPT611-3		—	1.5	Vdc	
UPT614-5		—	1.5	Vdc	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	—	—	$I_C = 5A, I_B = 0.5A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}	—	1.5	Vdc	$I_C = 10mAdc; R_{BE} = 100\Omega$
UPT611		60	—	Vdc	
UPT612		80	—	Vdc	
UPT613		100	—	Vdc	
UPT614		120	—	Vdc	
UPT615		150	—	Vdc	
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}	—	—	Vdc	$I_C = 10mAdc$
UPT611		40	—	Vdc	
UPT612		60	—	Vdc	
UPT613		80	—	Vdc	
UPT614-5		100	—	Vdc	
Collector-Emitter Cutoff Current	I_{CER}	—	10	μ Adc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mAdc	$V_{CE} = \text{rated } BV_{CEO}, R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μ Adc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	120	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	40 Typ.		MHz	$I_C = 0.5Adc, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	250 Typ.	ns	$I_C = 5A$
	Turn-off Time	t_{off}	500 Typ.	ns	

Note: 1. Pulse width = 300 μ s; duty cycle \leq 2%.



Switching Speed Circuit



POWER TRANSISTORS

5 Amp, 400V, Planar NPN

UPT721
UPT722
UPT723
UPT724
UPT725

FEATURES

- Collector-Base Voltage: up to 400V
- Peak Collector Current: 10A
- Turn-on Time: 250ns
- Turn-off Time: 800ns

DESCRIPTION

Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

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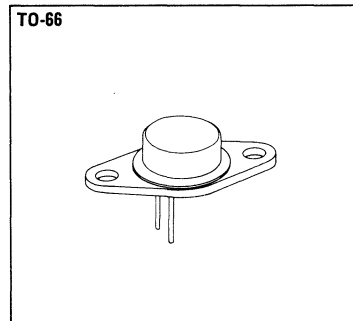
ABSOLUTE MAXIMUM RATINGS

	UPT721	UPT722	UPT723	UPT724	UPT725
Collector-Base Voltage, V_{CBO}	200V	250V	300V	350V	400V
Collector-Emitter Voltage, V_{CEO}	150V	200V	250V	300V	300V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V	5V
D.C. Collector Current, I_C	5A	5A	5A	5A	5A
Peak Collector Current, $I_{C(pk)}$	10A	10A	10A	10A	10A
Base Current, I_B	3A	3A	3A	3A	3A
Power Dissipation					
25°C Ambient				2W	
100°C Case				25W	
Thermal Resistance, θ_{J-C}				4°C/W	
Operating and Storage Temperature Range				-65°C to 200°C	

MECHANICAL SPECIFICATIONS

UPT721 UPT722 UPT723 UPT724 UPT725

	INCHES	MILLIMETERS
A	.620 MAX.	15.75 MAX.
B	.050 - .075	1.27 - 1.90
C	.250 - .340	6.35 - 8.63
D	.360 MIN.	9.14 MIN.
E	.028 - .034 DIA.	.711 - .863
F	.958 - .962	24.33 - 24.43
G	.570 - .590	14.47 - 14.98
H	.145 MAX. RAD.	3.68 MAX. RAD.
J	.142 - .152 DIA.	3.60 - 3.86 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190 - .210	4.82 - 5.33
M	.093 - .107	2.36 - 2.72

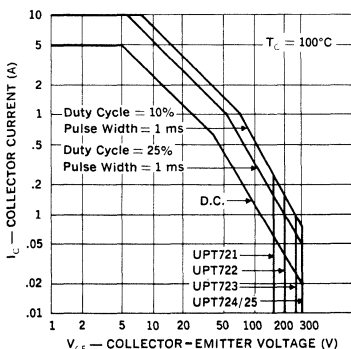


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

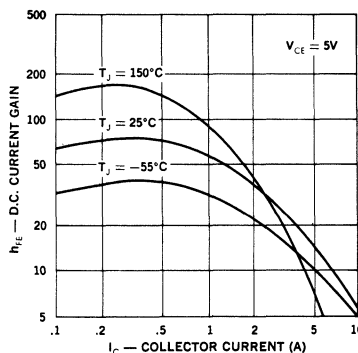
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	25	—	—	$I_C = 1A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	10	—	—	$I_C = 5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	5 Typ.		—	$I_C = 10A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = 5A, I_B = 1A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.8	Vdc	$I_C = 5A, I_B = 1A$
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CER}			Vdc	$I_C = 10mAdc; R_{BE} = 100\Omega$
UPT721		200	—		
UPT722		250	—		
UPT723		300	—		
UPT724		350	—		
UPT725		400	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mAdc$
UPT721		150	—		
UPT722		200	—		
UPT723		250	—		
UPT724-5		300	—		
Collector-Emitter Cutoff Current	I_{CER}	—	10	μAdc	$V_{CE} = \text{rated } BV_{CEO}; R_{BE} = 100\Omega$
Collector-Emitter Cutoff Current, 150°C	I_{CER}	—	1.0	mAdc	$V_{CE} = \text{rated } BV_{CEO}; R_{BE} = 100\Omega, T = 150^\circ C$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	120	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	30 Typ.		MHz	$I_C = 0.5Adc, V_{CE} = 5Vdc, f = 10MHz$
Switching Speeds	Turn-on Time	t_{on}	250 Typ.	ns	$I_C = 5A$
	Turn-off Time	t_{off}	800 Typ.	ns	

Note: 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

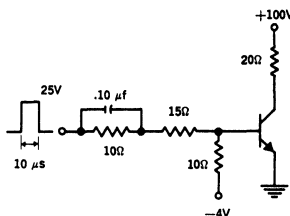
Maximum Safe Operating Area



D.C. Current Gain vs. Collector Current



Switching Speed Circuit



POWER TRANSISTORS

0.5 Amp, 300V, Planar NPN, Plastic

UPTA510
UPTA520
UPTA530

FEATURES

- Designed for High Speed Switching Applications
- Collector-Emitter Voltage: up to 300V
- Peak Collector Current: 1A
- Economical Plastic Molded Construction

DESCRIPTION

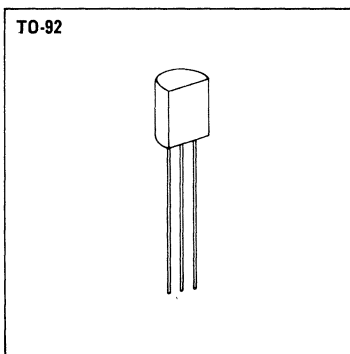
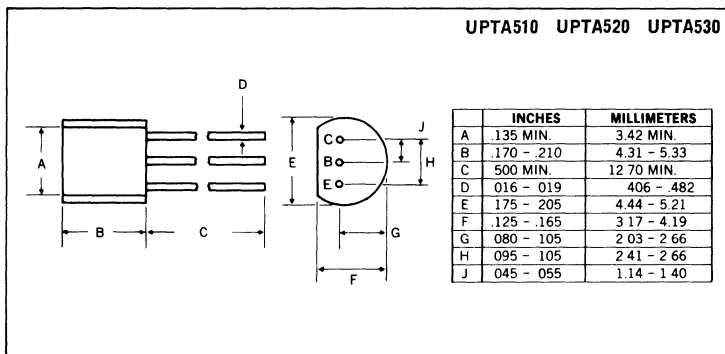
Unitrode high voltage transistors provide a unique combination of low saturation voltage, fast switching, and excellent gain. They are ideally suited for off-line power supply designs and other applications where the increased voltage rating adds to system reliability.

5

ABSOLUTE MAXIMUM RATINGS

	UPTA510	UPTA520	UPTA530
Collector-Base Voltage, V_{CBO}	150V	250V	350V
Collector-Emitter Voltage, V_{CEO}	100V	200V	300V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V
D.C. Collector Current, I_C	.5A	.5A	.5A
Peak Collector Current, I_C	1A	1A	1A
Base Current, I_B	.5A	.5A	.5A
Power Dissipation			
25°C Case	2.4W		
25°C Ambient	750mW		
Thermal Resistance, θ_{J-C}	62.5°C/W		
Thermal Resistance, θ_{J-A}	200°C/W		
Storage Temperature Range	-55°C to +150°C		
Maximum Junction Temperature	+175°C		

MECHANICAL SPECIFICATIONS

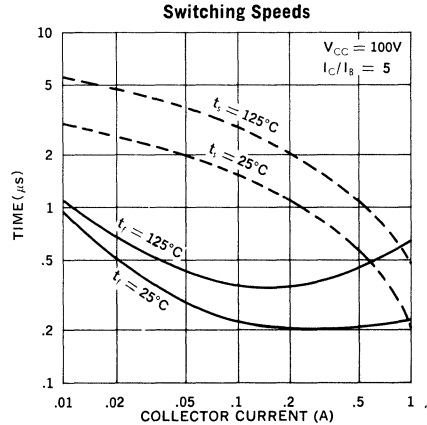
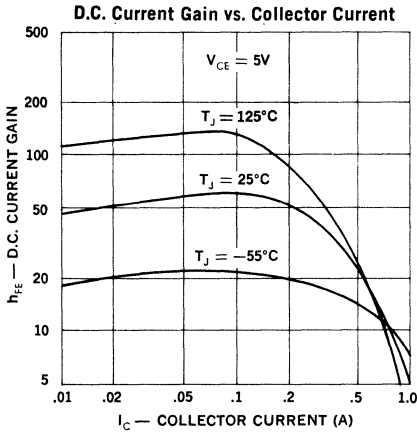


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

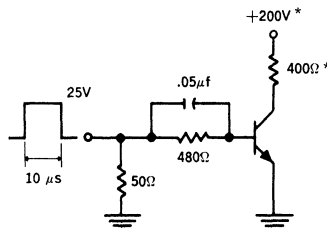
Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	20	—	—	$I_C = .1A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	8	—	—	$I_C = .5A, V_{CE} = 5Vdc$
D.C. Current Gain (Note 1)	h_{FE}	5 Typ.		—	$I_C = 1A, V_{CE} = 5Vdc$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	Vdc	$I_C = .5A, I_B = .1A$
	$V_{CE(sat)}$	—	.5	Vdc	$I_C = .2A, I_B = .02A$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	Vdc	$I_C = .5A, I_B = .1A$
Collector-Base Breakdown Voltage (Note 1)	BV_{CBO}			Vdc	$I_C = 10\mu Adc$
UPTA510		150	—		
UPTA520		250	—		
UPTA530		350	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}			Vdc	$I_C = 10mAdc$
UPTA510		100	—		
UPTA520		200	—		
UPTA530		300	—		
Collector-Emitter Cutoff Current	I_{CES}	—	10	μAdc	$V_{CE} = \text{rated } BV_{CEO}, V_{BE} = 0$
Collector-Emitter Cutoff Current	I_{CES}	—	1	mAdc	$V_{CE} = \text{rated } BV_{CEO}, T = 125^\circ C, V_{BE} = 0$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = 5Vdc$
Output Capacitance	C_{ob}	—	50	pf	$V_{CB} = 10Vdc, I_E = 0, f = 1MHz$
Gain-Bandwidth Product	f_T	15	—	MHz	$I_C = 1Adc, V_{CE} = 5Vdc, f = 10MHz$
Rise Time	t_r	100 Typ.		ns	$I_C = .5A$
Delay Time	t_d	50 Typ.		ns	
Storage Time	t_s	500 Typ.		ns	
Fall Time	t_f	200 Typ.		ns	

Note 1. Pulse width = 300 μs ; duty cycle \leq 2%.

Note 2. For thermal considerations for operating UPTA510, UPTA520 and UPTA530, refer to Application Note U-77.



Switching Speed Circuit



*Note: For UPTA 410/510, $V_{CC} = 100V, R_L = 200\Omega$

POWER TRANSISTORS

0.1 Amp, 500V, Planar NPN, Plastic

UPTB520
UPTB530
UPTB540
UPTB550

4

FEATURES

- Designed for High Speed Switching Applications
- Collector-Emitter Voltage: up to 500V
- Peak Collector Current: to .2A
- Economical Plastic Molded Construction

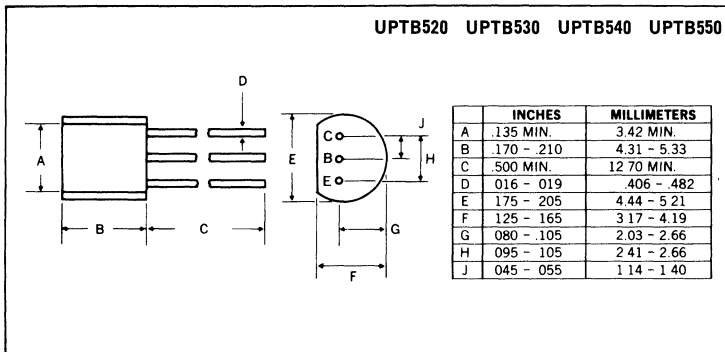
DESCRIPTION

Unitrode high voltage power transistors provide a unique combination of low saturation voltage, high gain and fast switching. They are ideally suited for pulse power applications in power supplies, thermal printers, solid state relays and pulse amplifiers.

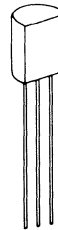
ABSOLUTE MAXIMUM RATINGS

	UPTB520	UPTB530	UPTB540	UPTB550
Collector-Base Voltage, V_{CBO}	250V	350V	450V	550V
Collector-Emitter Voltage, V_{CEO}	200V	300V	400V	500V
Emitter-Base Voltage, V_{EBO}	5V	5V	5V	5V
D.C. Collector Current, I_C	.1A	.1A	.1A	.1A
Peak Collector Current, I_C	.2A	.2A	.2A	.2A
Base Current, I_B	.1A	.1A	.1A	.1A
Power Dissipation				
25°C Case			2.4W	
25°C Ambient			750mW	
Thermal Resistance, θ_{J-C}			62.5°C/W	
Thermal Resistance, θ_{J-A}			200°C/W	
Storage Temperature Range			-55°C to +150°C	
Maximum Junction Temperature			+175°C	

MECHANICAL SPECIFICATIONS



TO-92



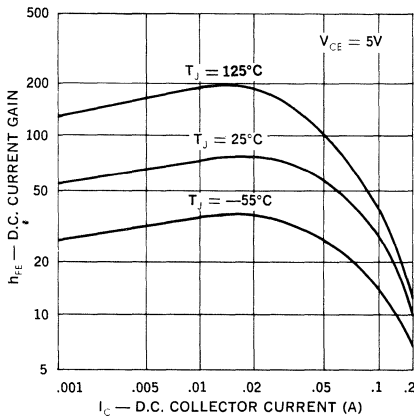
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Max.	Units	Test Conditions
D.C. Current Gain (Note 1)	h_{FE}	20	—	—	$I_C = 25\text{mA}, V_{CE} = 5\text{Vdc}$
D.C. Current Gain (Note 1)	h_{FE}	5	—	—	$I_C = 100\text{mA}, V_{CE} = 5\text{Vdc}$
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.2	Vdc	$I_C = 50\text{mA}, I_B = 10\text{mA}$
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.0	Vdc	$I_C = 20\text{mA}, I_B = 2\text{mA}$
Collector-Base Breakdown Voltage (Note 1)	BV_{CBO}	—	—	Vdc	$I_C = 50\text{mA}, I_B = 10\text{mA}$
(Note 1)					$I_C = 10\mu\text{Adc}$
UPTB520		250	—		
UPTB530		350	—		
UPTB540		450	—		
UPTB550		550	—		
Collector-Emitter Breakdown Voltage (Note 1)	BV_{CEO}	—	—	Vdc	$I_C = 1\text{mAdc}$
UPTB520		200	—		
UPTB530		300	—		
UPTB540		400	—		
UPTB550		500	—		
Collector-Emitter Cutoff Current	I_{CES}	—	10	μAdc	$V_{CE} = \text{rated } BV_{CEO}, V_{BE} = 0$
Collector-Emitter Cutoff Current	I_{CES}	—	1	mAdc	$V_{CE} = \text{rated } BV_{CEO}, T = 125^\circ\text{C}, V_{BE} = 0$
Emitter-Base Cutoff Current	I_{EBO}	—	50	μAdc	$V_{EB} = 5\text{Vdc}$
Output Capacitance	C_{ob}	—	50	pf	$V_{CB} = 10\text{Vdc}, I_E = 0, f = 1\text{MHz}$
Gain-Bandwidth Product	f_T	15	—	MHz	$I_C = 1\text{Adc}, V_{CE} = 5\text{Vdc}, f = 10\text{MHz}$
Rise Time	t_r	—	100 Typ.	ns	$I_C = 100\text{mA}$
Delay Time	t_d	—	50 Typ.	ns	
Storage Time	t_s	—	200 Typ.	ns	
Fall Time	t_f	—	1000 Typ.	ns	

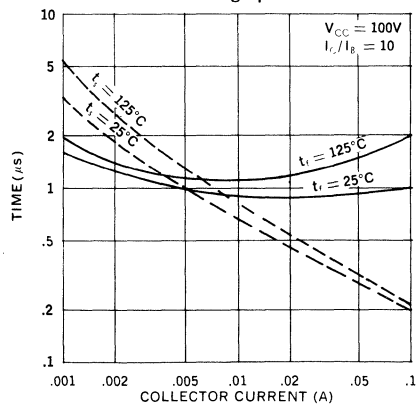
Note 1. Pulse width = 300 μs ; duty cycle $\leq 2\%$.

Note 2. For thermal considerations for operating UPTB520, UPTB530, UPTB540 and UPTB550, refer to Application Note U-77.

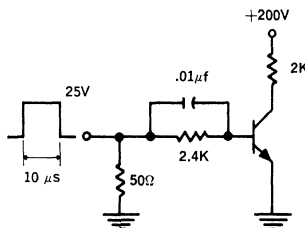
D.C. Current Gain vs. Collector Current

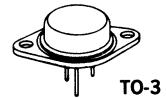
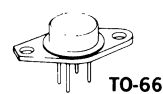


Switching Speeds



Switching Speed Circuit





Type	Output Current, Pk.	Input/Output Voltage	Polarity	Fall Time		On-State Voltage (V) @ (A)	Pkg.
				Volt. (ns)	Cur. (ns)		
PIC600 PIC601 PIC602 PIC610 PIC611 PIC612	5A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	75	150	1.5 @ 2	4 PIN TO-66 (Isolated)
PIC660 PIC661 PIC662 PIC670 PIC671 PIC672	10A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	150 250	250 250	1.5 @ 5	4 PIN TO-66 (Isolated)
PIC625 PIC626 PIC627 PIC635 PIC636 PIC637	15A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	175 300	300 300	1.5 @ 7	4 PIN TO-66 (Isolated)
PIC645 PIC646 PIC647 PIC655 PIC656 PIC657	20A	60 80 100 60 80 100	Pos. Pos. Pos. Neg. Neg. Neg.	150 300	300 300	1.5 @ 7	3 PIN TO-3
PIC730 PIC740	30A	30 40	Pos. Pos.	350	300	1 @ 20	3 PIN TO-3
PIC800 PIC801	8A	350 400	Pos.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)
PIC810 PIC811	8A	350 400	Neg.	200	200	1.5 @ 5	4 PIN TO-66 (Isolated)

5

Type	Description	Key Features	Pkg.
PIC900 B, C, D	5A; 60V, 80V, 100V H-Bridge Hybrid Circuit	<ul style="list-style-type: none"> • Designed and Characterized for Inductive Loads as Stepper Motors, DC Motor Drives, Full Bridge DC Converters • Fast Switching Times with Low (5mA) Drive Current • Electrically Isolated 18-Pin Dip with Integral Heat Spreader • Compatible with Automatic Insertion 	18 Pin DIL with Integral Heat Spreader

POWER INTEGRATED CIRCUIT

Switching Regulator 5 Amp Positive and Negative Power Output Stages

PIC600
PIC601
PIC602
PIC610
PIC611
PIC612

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4.)
- High operating frequency (to > 100kHz) results in smaller inductor-capacitor filter and improved power supply response time
- High operating efficiency: Typical 2A circuit performance —
Rise and Fall time <75ns
Efficiency >85%
- No reverse recovery spike generated by commutating diode (See note 4. and Fig. 2.)
- Electrically isolated, 4-Pin, TO-66 hermetic case

DESCRIPTION

The Unitrode ESP Switching Regulator is a unique hybrid transistor circuit, specifically designed, constructed and specified for use in high current switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode, and empirically determining the optimum drive and bias conditions.

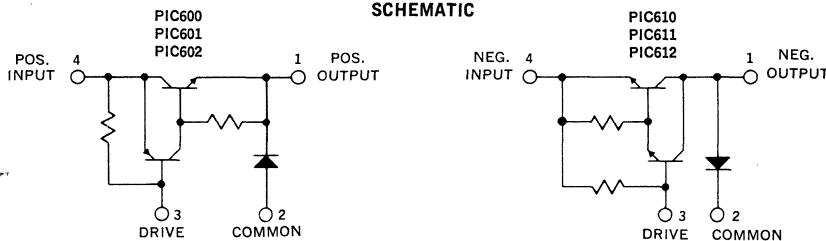
Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitrode PIC600 series, the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC600 series design and packaging, the designer is aided in overcoming two of the most significant

drawbacks to switching regulators: noise generation and slow response time; there is, in fact, no diode reverse recovery spike (see note 4.).

The PIC600 series switching regulators are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of -55°C to $+125^{\circ}\text{C}$. The devices are enclosed in a special 4-pin TO-66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

Application Notes U-68 and U-76 provide a detailed description of the hybrid circuit and design guidance for specific circuit applications.

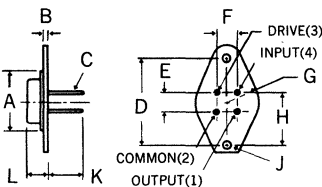
SCHEMATIC



MECHANICAL SPECIFICATIONS

NOTES:

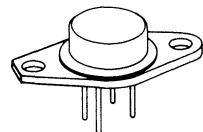
1. Case is electrically isolated.
2. Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



PIC600 PIC601 PIC602 PIC610 PIC611 PIC612

	ins.	mm
A	620 MAX	15.75 MAX
B	050-075	1.27-1.91
C	028-034	0.71-0.86
D	958-962	24.33-24.43
E	190-210	4.83-5.33
F	190-210	4.83-5.33
G	350 MAX RAD	8.89 MAX RAD
H	570-590	14.48-14.99
J	142-152 DIA	3.61-3.86 DIA
K	360 MIN	9.14 MIN
L	250-340	6.35-8.64

4-Pin TO-66



ABSOLUTE MAXIMUM RATINGS

	PIC600	PIC601	PIC602	PIC610	PIC611	PIC612
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive-Input Reverse Voltage, $V_{3,4}$	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	5A	5A	5A	-5A	-5A	-5A
Drive Current, I_3	-0.2A	-0.2A	-0.2A	0.2A	0.2A	0.2A
Thermal Resistance						
Junction to Case, θ_{J-C}				4.0°C/W		
Power Switch				4.0°C/W		
Commutating Diode				4.0°C/W		
Case to Ambient, θ_{C-A}				60.0°C/W		
Operating Temperature Range, T_C				-55°C to +125°C		
Maximum Junction Temperature, T_j				+150°C		
Storage Temperature Range				-65°C to +150°C		



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	PIC600, 601, 602			PIC610, 611, 612			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Current Delay Time	t_{di}	—	20	40	—	20	40	ns	$V_{in} = 25V(-25V)$
Current Rise Time	t_{ri}	—	50	75	—	50	75	ns	$V_{out} = 5V(-5V)$
Voltage Rise Time	t_{rv}	—	30	50	—	30	50	ns	$I_{out} = 2A(-2A)$
Voltage Storage Time	t_{sv}	—	450	—	—	450	—	ns	$I_3 = -20mA(20mA)$ NOTE 5
Voltage Fall Time	t_{fv}	—	50	75	—	50	75	ns	See Figure 2.
Current Fall Time	t_{fi}	—	70	150	—	70	150	ns	See notes 1., 2., 4.
Efficiency (Notes 2. & 4.)	η	—	85	—	—	85	—	%	
On-State Voltage (Note 3.)	$V_{4-(on)}$	—	1.0	1.5	—	-1.0	-1.5	V	$I_4 = 2A(-2A), I_3 = -0.2A(0.2A)$ NOTE 5
On-State Voltage (Note 3.)	$V_{4-1(on)}$	—	2.5	3.5	—	-2.5	-3.5	V	$I_4 = 5A(-5A), I_3 = -0.2A(0.2A)$ NOTE 5
Diode Forward Voltage (Note 3.)	$V_{2-1(on)}$	—	.8	1.0	—	-.8	-1.0	V	$I_2 = 2A(-2A)$
Diode Forward Voltage (Note 3.)	$V_{2-1(on)}$	—	1.0	1.5	—	-1.0	-1.5	V	$I_2 = 5A(-5A)$
Off-State Current	I_{4-1}	—	0.1	10	—	-0.1	-10	μA	$V_4 =$ Rated input voltage
Off-State Current	I_{4-1}	—	10	—	—	-10	—	μA	$V_4 =$ Rated input voltage, $T_A = 100^\circ C$
Diode Reverse Current	I_{1-2}	—	1.0	10	—	-1.0	-10	μA	$V_1 =$ Rated output voltage
Diode Reverse Current	I_{1-2}	—	500	—	—	500	—	μA	$V_1 =$ Rated output voltage, $T_A = 100^\circ C$

NOTES:

- In switching an inductive load, the current will lead the voltage on turn on and lag the voltage on turn-off (see Figure 2.). Therefore, Voltage Delay Time (t_{dv}) $\approx t_{di} + t_{ri}$ and Current Storage Time (t_{si}) $\approx t_{sv} + t_{fv}$.
- The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1., in which the efficiency is measured, is representative of typical operating conditions for the PIC600 switching regulators.
- Pulse test: Duration = 300 μs , Duty Cycle $\leq 2\%$.
- As can be seen from the switching waveforms shown in Figure 2., no reverse of forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
- To insure safe operation I_3 should be $\geq |20mA|$ during T_{ON} . Operation at $I_3 < |20mA|$ can permanently damage device.

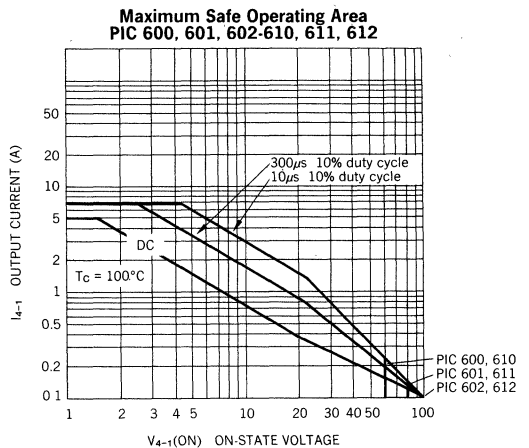
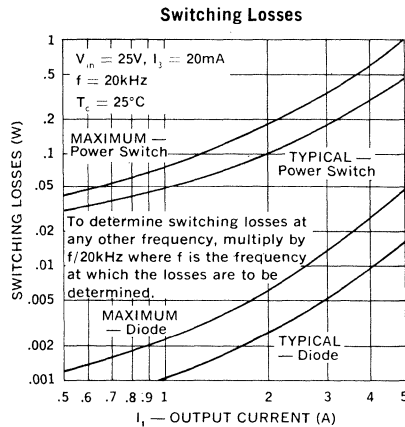
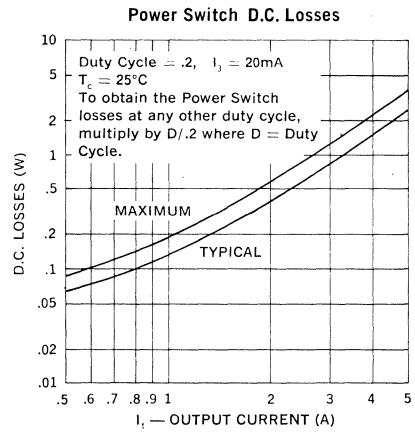
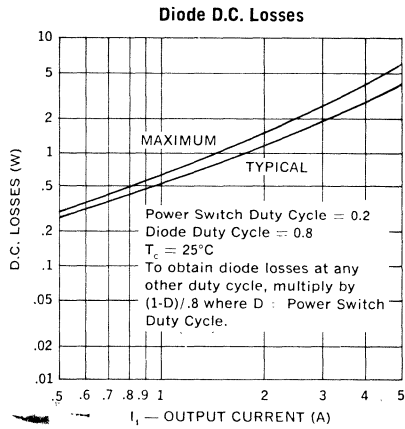
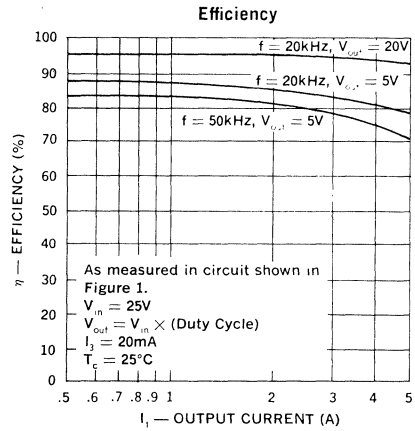
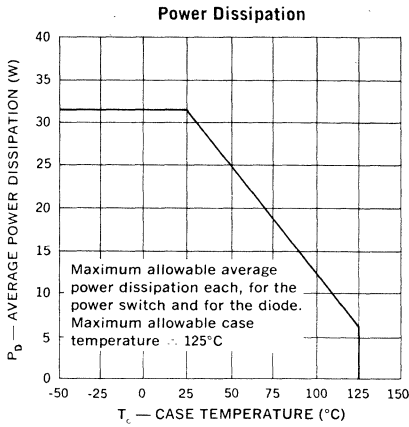
POWER DISSIPATION CONSIDERATIONS

The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.

The switching losses curve presents data for a frequency of 20KHz. To find losses at any other frequency, multiply by $f/20KHz$.

The D.C. losses curve presents data for a duty cycle of .2. To find D.C. losses at any other duty cycle, multiply by $D/.2$ for the power switch and by $(1-D)/.8$ for the diode.

At frequencies much below 10KHz the above method for determining the allowable case or ambient temperature becomes invalid and a detailed transient thermal analysis must be performed. Please see Design Note 6 (DN-6) for further information.



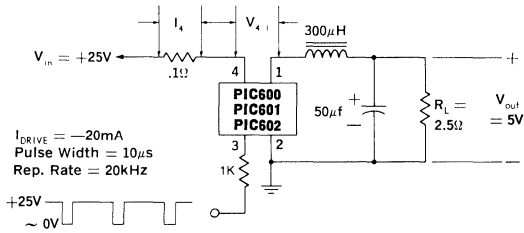


Figure 1. PIC600, 601, 602 Switching Speed Circuit

Note: PIC610, PIC611, PIC612 Test Circuit and waveforms are identical but of opposite polarity ($V_{in} = -25V$, $V_{out} = -5V$, $I_{DRIVE} = +20mA$).

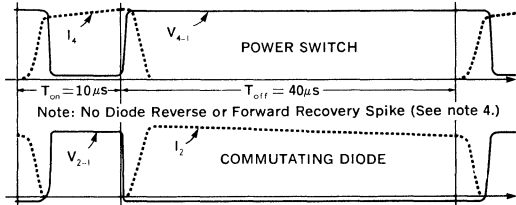
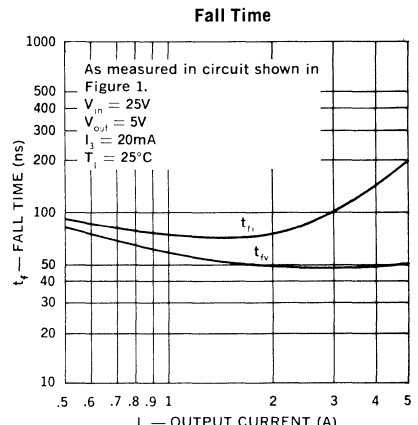
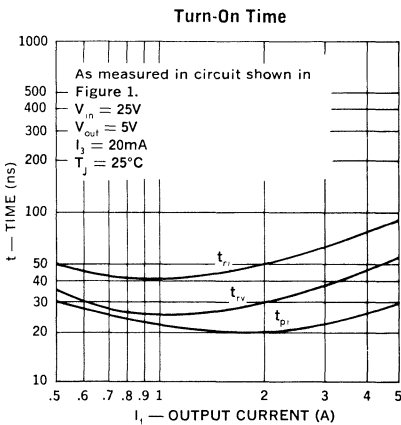
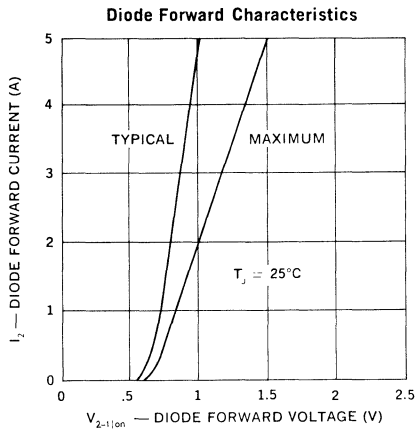
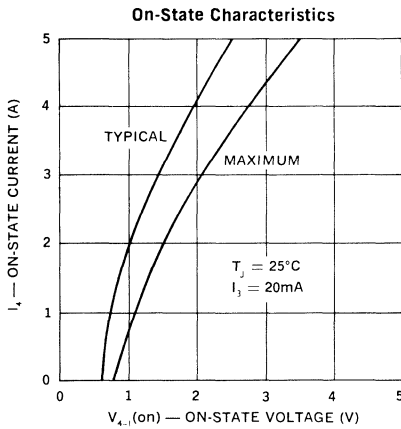


Figure 2. PIC600, PIC601, PIC602 Switching Waveforms



POWER INTEGRATED CIRCUIT

Switching Regulator 15 Amp Positive and Negative Power Output Stages

PIC625
PIC626
PIC627
PIC635
PIC636
PIC637

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4.)
- High operating frequency (to >100kHz) results in smaller inductor-capacitor filter and improved power supply response time
- High operating efficiency: Typical 7A circuit performance —
Rise and Fall time <300 ns
Efficiency >85%
- No reverse recovery spike generated by commutating diode (See note 4. and Fig. 2.)
- Electrically isolated, 4-Pin, TO66 hermetic case

DESCRIPTION

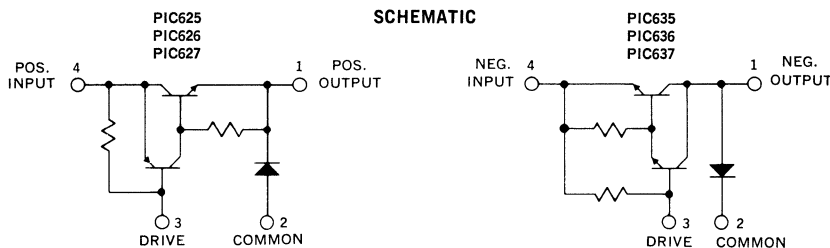
The Unitrode ESP Switching Regulator is a unique hybrid transistor circuit, specifically designed, constructed and specified for use in high current switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode, and empirically determining the optimum drive and bias conditions.

Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitrode PIC600 series the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC600 series design and packaging, the designer is aided in overcoming two of the most

significant drawbacks to switching regulators: noise generation and slow response time; there is, in fact, no diode reverse recovery spike (See note 4.).

The PIC600 series switching regulators are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of -55°C to $+125^{\circ}\text{C}$. The devices are enclosed in a special 4-pin TO66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

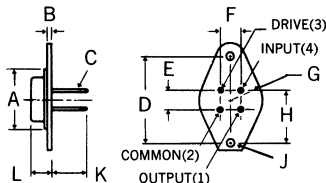
Application Notes U-68 and U-76 provide a detailed description of the hybrid circuit and design guidance for specific circuit applications.



MECHANICAL SPECIFICATIONS

NOTES:

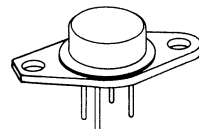
1. Case is electrically isolated.
2. Leads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.



PIC625 PIC626 PIC627 PIC635 PIC636 PIC637

	ins.	mm
A	620 MAX	15.75 MAX
B	050-075	1.27-1.91
C	028-034	0.71-0.86
D	958-962	24.33-24.43
E	190-210	4.83-5.33
F	190-210	4.83-5.33
G	350 MAX RAD	8.89 MAX RAD
H	570-590	14.48-14.99
J	142-152 DIA	3.61-3.86 DIA
K	360 MIN	9.14 MIN
L	250-340	6.35-8.64

4-Pin TO-66



ABSOLUTE MAXIMUM RATINGS

	PIC625	PIC626	PIC627	PIC635	PIC636	PIC637
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5A
Output Current, I_1	15A	15A	15A	-15A	-15A	-15A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch				4.0°C/W		
Commutating Diode				4.0°C/W		
Case to Ambient, θ_{C-A}						
			60.0°C/W			
Operating Temperature Range, T_C						
			-55°C to +125°C			
Maximum Junction Temperature, T_J						
			+150°C			
Storage Temperature Range						
			-65°C to +150°C			



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	PIC625/626/627			PIC635/636/637			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Current Delay Time	t_{di}	—	35	60	—	35	60	ns	$V_{in} = 25V(-25V)$
Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	$V_{out} = 5V(-5V)$
Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	$I_{out} = 7A(-7A)$
Voltage Storage Time	t_{sv}	—	700	—	—	700	—	ns	$I_3 = -30mA(30mA)$ NOTE 5
Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 2
Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See notes 1, 2, 4
Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	1.0	1.5	—	-1.0	-1.5	V	$I_4 = 7A(-7A)$, $I_3 = -.03A(.03A)$ NOTE 5
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	2.5	3.5	—	-2.5	-3.5	V	$I_4 = 15A(-15A)$, $I_3 = -.03A(.03A)$ NOTE 5
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.85	1.25	—	-.85	-1.25	V	$I_2 = 7A(-7A)$
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.95	1.75	—	-.95	-1.75	V	$I_2 = 15A(-15A)$
Off-State Current	I_{4-1}	—	0.1	10	—	-0.1	-10	μA	$V_4 = \text{Rated input voltage}$
Off-State Current	I_{4-1}	—	10	—	—	-10	—	μA	$V_4 = \text{Rated input voltage}$, $T_A = 100^\circ C$
Diode Reverse Current	I_{1-2}	—	1.0	10	—	-1.0	-10	μA	$V_1 = \text{Rated output voltage}$
Diode Reverse Current	I_{1-2}	—	500	—	—	500	—	μA	$V_1 = \text{Rated output voltage}$, $T_A = 100^\circ C$

NOTES:

- In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{pv}) $\cong t_{di} + t_{ri}$ and Current Storage Time (t_{si}) $\cong t_{sv} + t_{fv}$.
- The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the PIC600 series switching regulators.
- Pulse test: Duration = 300 μs , Duty Cycle \leq 2%.
- As can be seen from the switching waveforms shown in Figure 2, no reverse of forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
- To insure safe operation I_3 should be $\geq |30mA|$ during T_{ON} . Operation at $I_3 < |30mA|$ can permanently damage device.

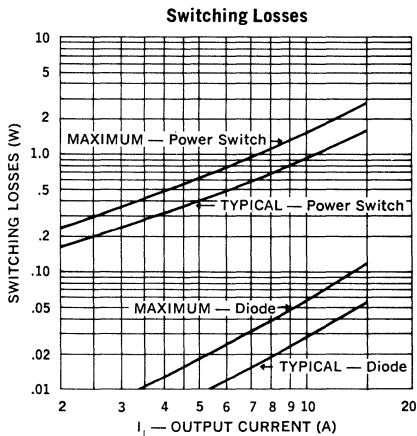
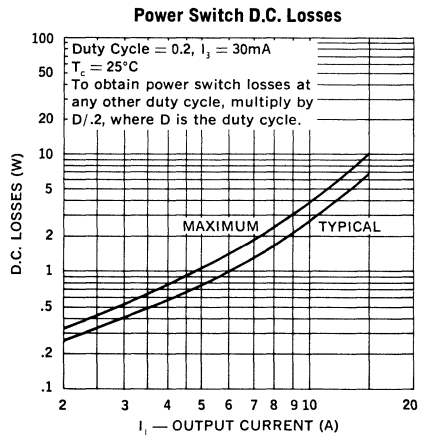
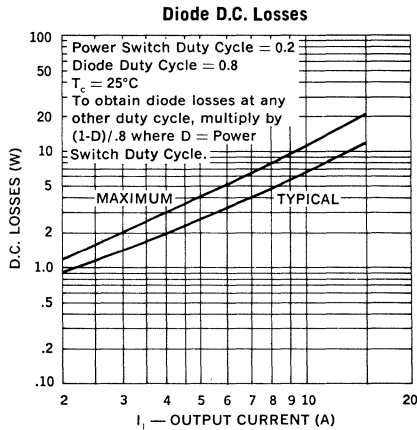
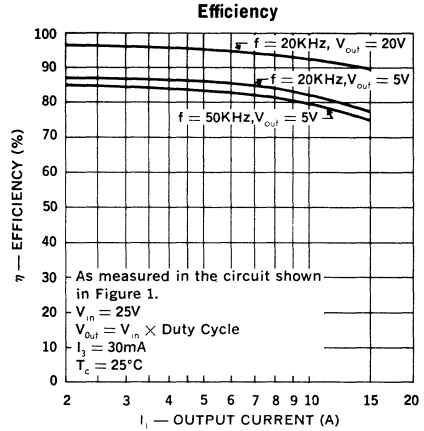
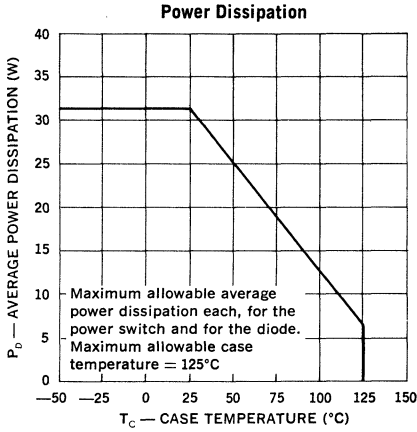
POWER DISSIPATION CONSIDERATIONS

The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.

The switching losses curve presents data for a frequency of 20KHz. To find losses at any other frequency, multiply by $f/20KHz$.

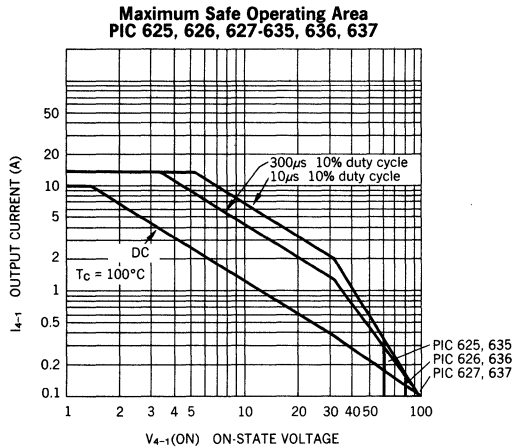
The D.C. losses curve presents data for a duty cycle of .2. To find D.C. losses at any other duty cycle, multiply by $D/.2$ for the power switch and by $(1-D)/.8$ for the diode.

At frequencies much below 10KHz the above method for determining the allowable case or ambient temperature becomes invalid and a detailed transient thermal analysis must be performed. Please see Design Note 6 (DN-6) for further information.



V_{in} = 25V,
I_s = 30mA
f = 20KHz
T_c = 25°C

To determine switching losses at any other frequency, multiply by f/20KHz where f is the frequency at which the losses are to be determined.



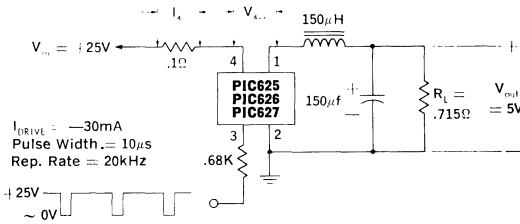


Figure 1. PIC625, 626, 627 Switching Speed Circuit

Note: PIC635, PIC636, PIC637 Circuit and waveforms are identical but of opposite polarity ($V_{in} = -25V$, $V_{out} = -5V$, $I_{DRIVE} = +30mA$.)

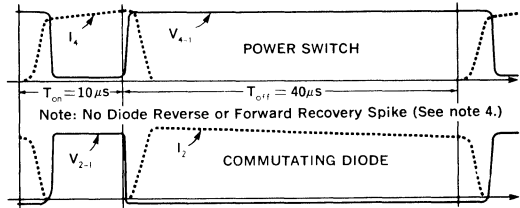
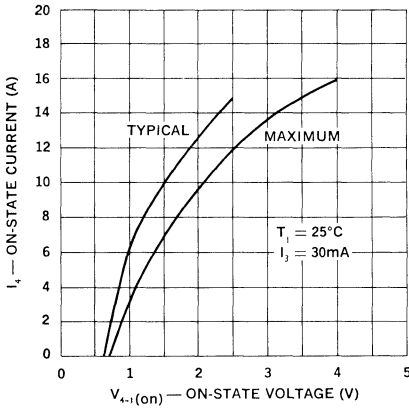
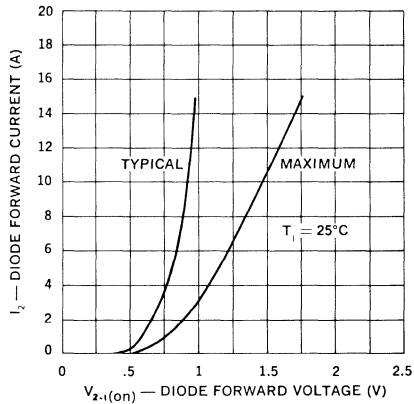


Figure 2. PIC625, 626, 627 Switching Waveforms

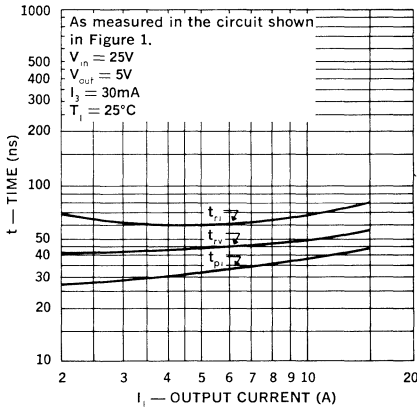
On-State Characteristics



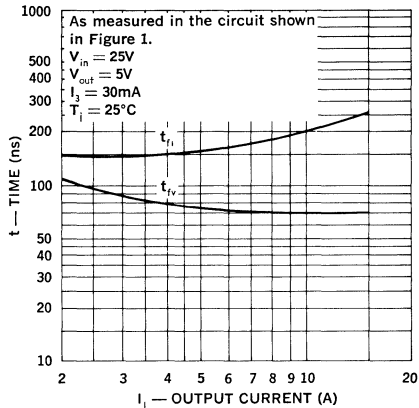
Diode Forward Characteristics



Turn-on Time



Fall Time



POWER INTEGRATED CIRCUIT

Switching Regulator 15 Amp Positive and Negative Power Output Stages

PIC645
 PIC646
 PIC647
 PIC655
 PIC656
 PIC657

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4.)
- High operating frequency (to $>100\text{kHz}$) results in smaller inductor-capacitor filter and improved power supply response time
- High operating efficiency: Typical 7A circuit performance —
 Rise and Fall time $<300\text{ ns}$
 Efficiency $>85\%$
- No reverse recovery spike generated by commutating diode (See note 4. and Fig. 2.)

DESCRIPTION

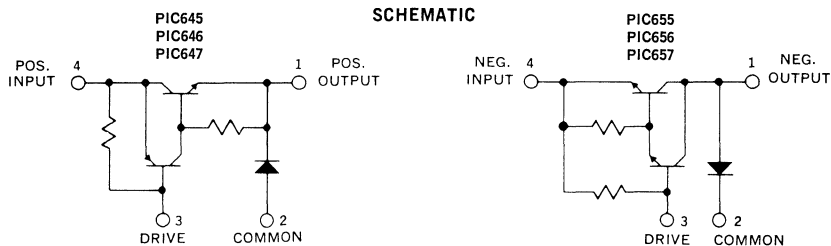
The Unitorde ESP Switching Regulator is a unique hybrid transistor circuit, specifically designed, constructed and specified for use in high current switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode, and empirically determining the optimum drive and bias conditions.

Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitorde PIC600 series the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC600 series design and packaging, the designer is aided in overcoming two of the most

significant drawbacks to switching regulators: noise generation and slow response time; there is, in fact, no diode reverse recovery spike (See note 4.).

The PIC600 series switching regulators are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of -55°C to $+125^{\circ}\text{C}$. The devices are enclosed in a special 3 pin TO-3 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

Application Notes U-68 and U-76 provide a detailed description of the hybrid circuit and design guidance for specific circuit applications.

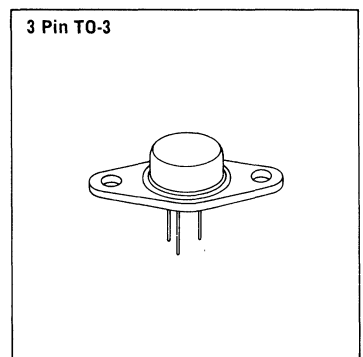


MECHANICAL SPECIFICATIONS

PIC645 PIC646 PIC647 PIC655 PIC656 PIC657

	ins.	mm
A	875 MAX	22.23 MAX
B	.135	3.43
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.205-225	5.21-5.72
F	420-440	10.67-11.18
G	145-165	3.68-4.19
H	395-405	10.03-10.29
J	151-161 DIA	3.84-4.09 DIA
K	188 MAX RAD	4.78 MAX. RAD.
L	525 MAX. RAD	13.34 MAX. RAD
M	708-728	17.98-18.49
N	1.177-1.197	29.90-30.40
P	.038-.043 DIA	.97-1.09 DIA

NOTE:
 Loads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.



ABSOLUTE MAXIMUM RATINGS

	PIC645	PIC646	PIC647	PIC655	PIC656	PIC657
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Continuous Output Current, I_1	15A	15A	15A	-15A	-15A	-15A
Peak Output Current	20A	20A	20A	-20A	-20A	-20A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}				2°C/W		
Power Switch				2°C/W		
Commutating Diode				30.0°C/W		
Case to Ambient, θ_{C-A}						
Operating Temperature Range, T_C				-55°C to +125°C		
Maximum Junction Temperature, T_J				+150°C		
Storage Temperature Range				-65°C to +150°C		

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	PIC645/646/647			PIC655/656/657			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Current Delay Time	t_{di}	—	35	60	—	35	60	ns	$V_{in} = 25V(-25V)$
Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	$V_{out} = 5V(-5V)$
Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	$I_{out} = 7A(-7A)$
Voltage Storage Time	t_{sv}	—	700	—	—	700	—	ns	$I_3 = -30mA(30mA)$ NOTE 5
Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 2
Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See notes 1, 2, 4
Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	1.0	1.5	—	-1.0	-1.5	V	$I_4 = 7A(-7A)$, $I_3 = -.03A(.03A)$ NOTE 5
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	2.5	3.5	—	-2.5	-3.5	V	$I_4 = 15A(-15A)$, $I_3 = -.03A(.03A)$ NOTE 5
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.85	1.25	—	-.85	-1.25	V	$I_2 = 7A(-7A)$
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.95	1.75	—	-.95	-1.75	V	$I_2 = 15A(-15A)$
Off-State Current	I_{4-1}	—	0.1	10	—	-0.1	-10	μA	$V_4 =$ Rated input voltage
Off-State Current	I_{4-1}	—	10	—	—	-10	—	μA	$V_4 =$ Rated input voltage, $T_A = 100^\circ C$
Diode Reverse Current	I_{1-2}	—	1.0	10	—	-1.0	-10	μA	$V_1 =$ Rated output voltage
Diode Reverse Current	I_{1-2}	—	500	—	—	500	—	μA	$V_1 =$ Rated output voltage, $T_A = 100^\circ C$

NOTES:

- In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{pv}) $\cong t_{di} + t_{ri}$ and Current Storage Time (t_{si}) $\cong t_{sv} + t_{fv}$.
- The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the PIC600 series switching regulators.
- Pulse test: Duration = 300 μs , Duty Cycle \leq 2%.
- As can be seen from the switching waveforms shown in Figure 2, no reverse of forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
- To insure safe operation I_3 should be $\geq |30mA|$ during T_{ON} . Operation at $I_3 < |30mA|$ can permanently damage device.

POWER DISSIPATION CONSIDERATIONS

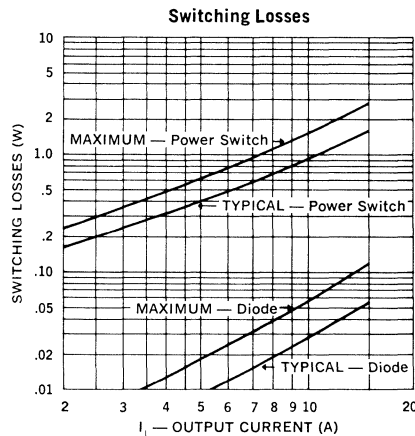
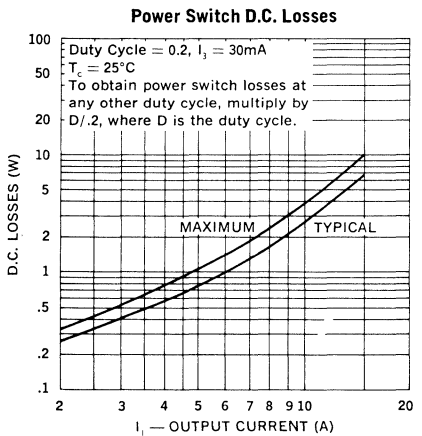
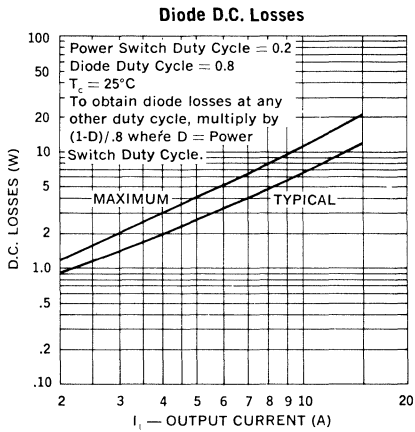
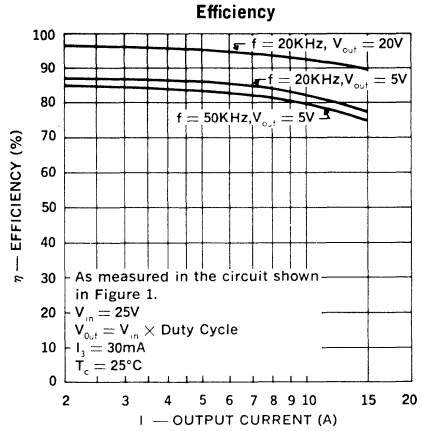
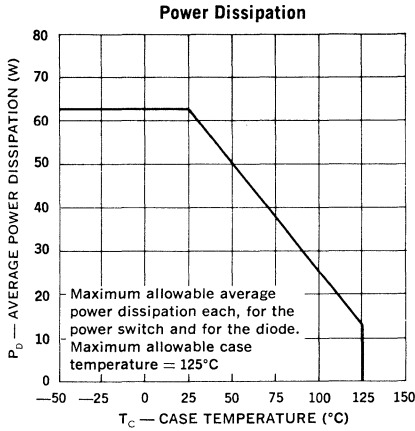
The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.

The switching losses curve presents data for a frequency of 20KHz. To find losses at any other frequency, multiply by $f/20KHz$.

The D.C. losses curve presents data for a duty cycle of .2. To find D.C. losses at any other duty cycle, multiply by $D/.2$ for the power switch and by $(1-D)/.8$ for the diode.

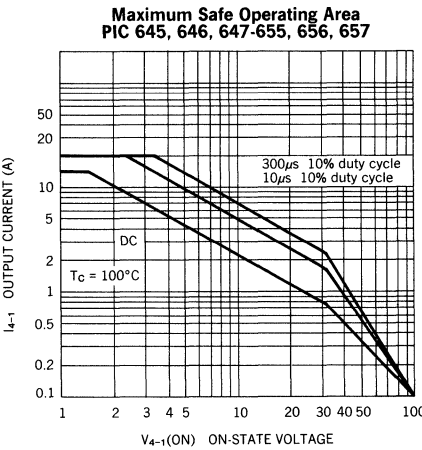
At frequencies much below 10KHz the above method for determining the allowable case or ambient temperature becomes invalid and a detailed transient thermal analysis must be performed. Please see Design Note 6 (DN-6) for further information.





$V_{in} = 25V, I_3 = 30mA$
 $f = 20KHz$
 $T_c = 25^{\circ}C$

To determine switching losses at any other frequency, multiply by $f/20KHz$ where f is the frequency at which the losses are to be determined.



PIC 645 655
 PIC 646 656
 PIC 647 657

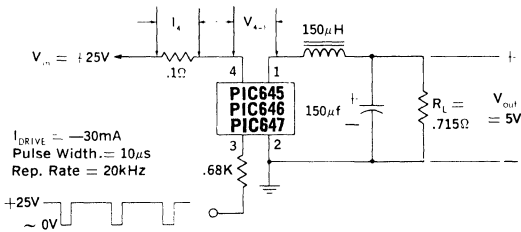


Figure 1. PIC645, 646, 647 Switching Speed Circuit

Note: PIC655, PIC656, PIC657 Circuit and waveforms are identical but of opposite polarity ($V_{in} = -25V$, $V_{out} = -5V$, $I_{DRIVE} = +30mA$.)

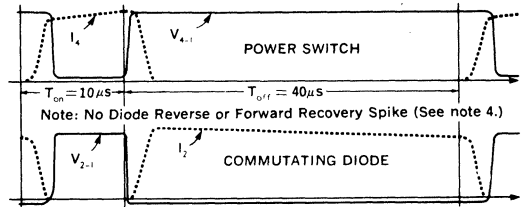
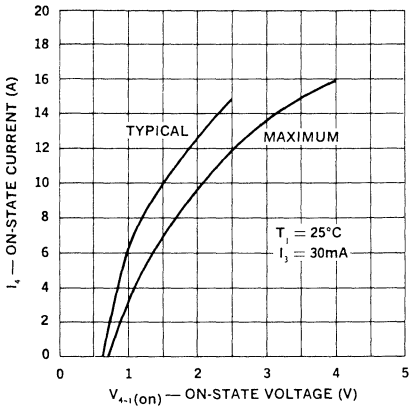


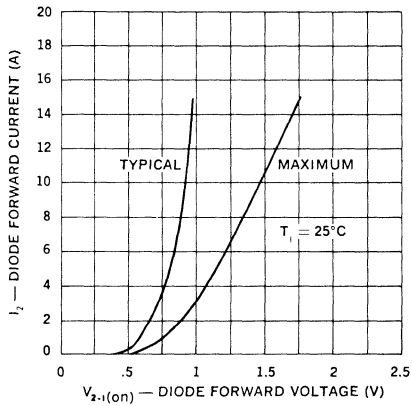
Figure 2. PIC645, 646, 647 Switching Waveforms

5

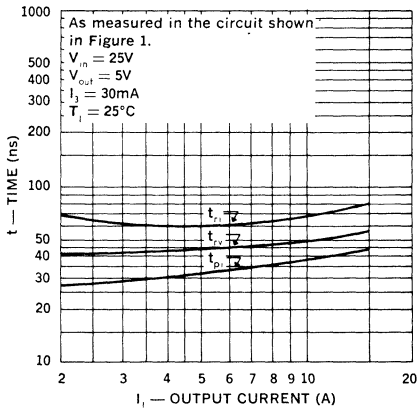
On-State Characteristics



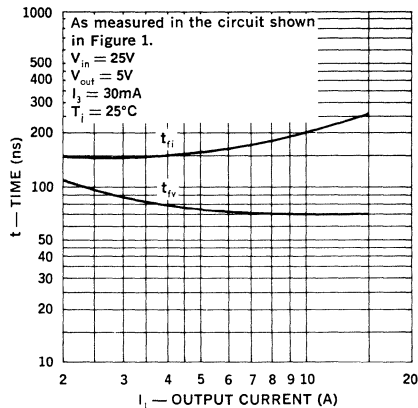
Diode Forward Characteristics



Turn-on Time



Fall Time



POWER INTEGRATED CIRCUIT

Switching Regulator 10 Amp Positive and Negative Power Output Stages

PIC660
PIC661
PIC662
PIC670
PIC671
PIC672

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4.)
- High operating frequency (to >100kHz) results in smaller inductor-capacitor filter and improved power supply response time
- High operating efficiency: Typical 5A circuit performance —
Rise and Fall time <300ns
Efficiency >85%
- No reverse recovery spike generated by commutating diode (See note 4. and Fig. 2.)
- Electrically isolated, 4-Pin, TO-66 hermetic case

DESCRIPTION

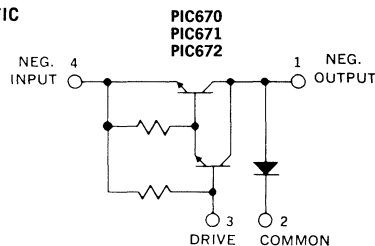
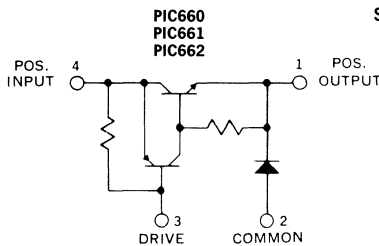
The Unitrode Switching Regulator is a unique hybrid transistor circuit, specifically designed, constructed and specified for use in high current switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode, and empirically determining the optimum drive and bias conditions.

Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitrode PIC600 series the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC600 series design and packaging, the designer is aided in overcoming two of the most

significant drawbacks to switching regulators: noise generation and slow response time; there is, in fact, no diode reverse recovery spike (See note 4.).

The PIC600 series switching regulators are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of -55°C to $+125^{\circ}\text{C}$. The devices are enclosed in a special 4-Pin TO-66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

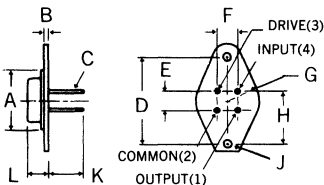
Application Notes U-68 and U-76 provide a detailed description of the hybrid circuit and design guidance for specific circuit applications.



MECHANICAL SPECIFICATIONS

NOTES:

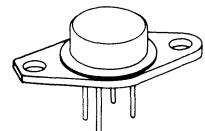
1. Case is electrically isolated.
2. Leads may be soldered to within $\frac{1}{16}$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



PIC660 PIC661 PIC662 PIC670 PIC671 PIC672

	ins.	mm
A	620 MAX	15.75 MAX
B	050-075	1.27-1.91
C	028-034	0.71-0.86
D	958-962	24.33-24.43
E	190-210	4.83-5.33
F	190-210	4.83-5.33
G	350 MAX RAD	8.89 MAX RAD
H	570-590	14.48-14.99
J	142-152 DIA	3.61-3.86 DIA
K	360 MIN	9.14 MIN
L	250-340	6.35-8.64

4-Pin TO-66



ABSOLUTE MAXIMUM RATINGS

	PIC660	PIC661	PIC662	PIC670	PIC671	PIC672
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	10A	10A	10A	-10A	-10A	-10A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch				4.0°C/W		
Commutating Diode				4.0°C/W		
Case to Ambient, θ_{C-A}				60.0°C/W		
Operating Temperature Range, T_C				-55°C to +125°C		
Maximum Junction Temperature, T_J				+150°C		
Storage Temperature Range				-65°C to +150°C		



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	PIC660/661/662			PIC670/671/672			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Current Delay Time	t_{di}	—	35	60	—	35	60	ns	$V_{in} = 25V(-25V)$
Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	$V_{out} = 5V(-5V)$
Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	$I_{out} = 5A(-5A)$
Voltage Storage Time	t_{sv}	—	700	—	—	700	—	ns	$I_3 = -30mA(30mA)$ NOTE 5
Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 2
Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See notes 1, 2, 4
Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	1.0	1.5	—	-1.0	-1.5	V	$I_4 = 5A(-5A), I_3 = -.03A(.03A)$ NOTE 5
On-State Voltage (Note 3)	$V_{4-1(on)}$	—	2.5	3.5	—	-2.5	-3.5	V	$I_4 = 10A(-10A), I_3 = -.03A(.03A)$ NOTE 5
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.85	1.25	—	-.85	-1.25	V	$I_2 = 5A(-5A)$
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	—	.95	1.75	—	-.95	-1.75	V	$I_2 = 10A(-10A)$
Off-State Current	I_{4-1}	—	0.1	10	—	-0.1	-10	μA	$V_4 =$ Rated input voltage
Off-State Current	I_{4-1}	—	10	—	—	-10	—	μA	$V_4 =$ Rated input voltage, $T_A = 100^\circ C$
Diode Reverse Current	I_{1-2}	—	1.0	10	—	-1.0	-10	μA	$V_1 =$ Rated output voltage
Diode Reverse Current	I_{1-2}	—	500	—	—	500	—	μA	$V_1 =$ Rated output voltage, $T_A = 100^\circ C$

NOTES:

1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{dv}) $\cong t_{di} + t_{ri}$ and Current Storage Time (t_{si}) $\cong t_{sv} + t_{fv}$.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the PIC600 series switching regulators.
3. Pulse test: Duration = 300 μs , Duty Cycle \leq 2%.
4. As can be seen from the switching waveforms shown in Figure 2, no reverse of forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
5. To insure safe operation I_3 should be \geq |30mA| during T_{ON} . Operation at $I_3 <$ |30mA| can permanently damage device.

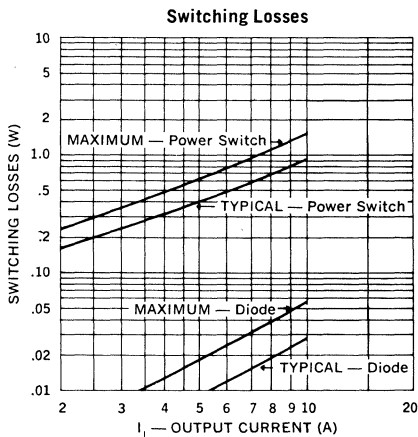
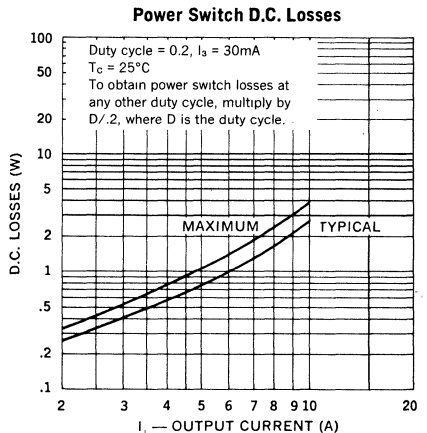
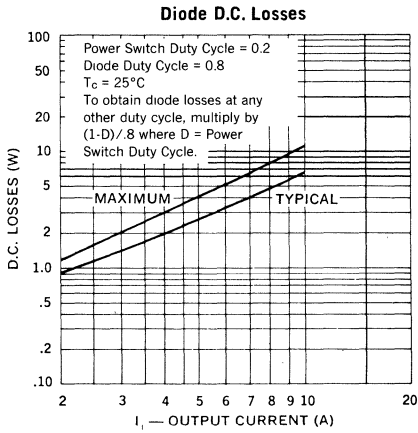
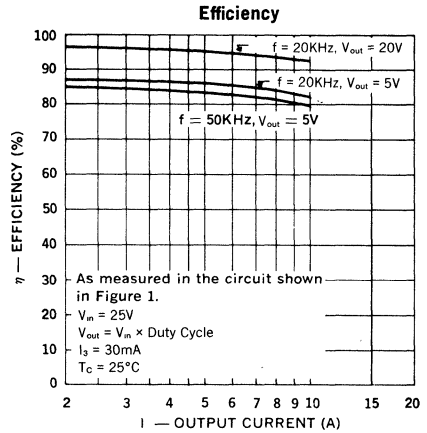
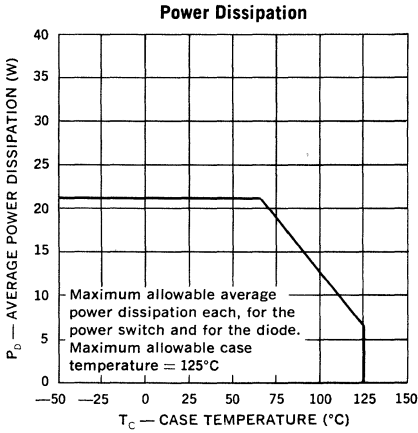
POWER DISSIPATION CONSIDERATIONS

The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.

The switching losses curve presents data for a frequency of 20KHz. To find losses at any other frequency, multiply by $f/20KHz$.

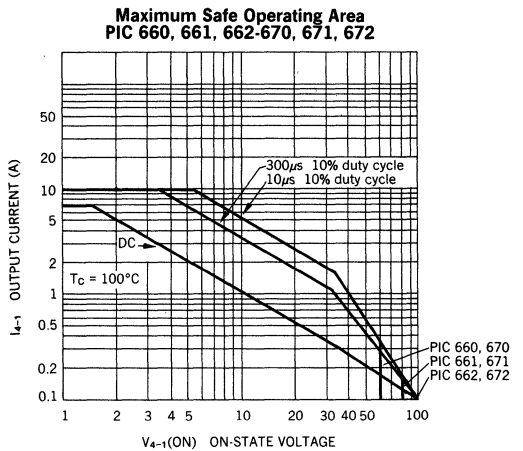
The D.C. losses curve presents data for a duty cycle of .2. To find D.C. losses at any other duty cycle, multiply by $D/.2$ for the power switch and by $(1-D)/.8$ for the diode.

At frequencies much below 10KHz the above method for determining the allowable case or ambient temperature becomes invalid and a detailed transient thermal analysis must be performed. Please see Design Note 6 (DN-6) for further information.



$V_{in} = 25V$, $V_3 = 30mA$
 $f = 20KHz$
 $T_C = 25^{\circ}C$

To determine switching losses at any other frequency, multiply by $f/20KHz$ where f is the frequency at which the losses are to be determined.



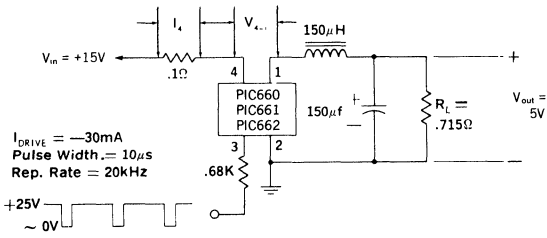


Figure 1. PIC660, 661, 662 Switching Speed Circuit

Note: PIC670, PIC671, PIC672 Circuit and waveforms are identical but of opposite polarity ($V_{in} = -15V$, $V_{out} = -5V$, $I_{DRIVE} = +30mA$.)

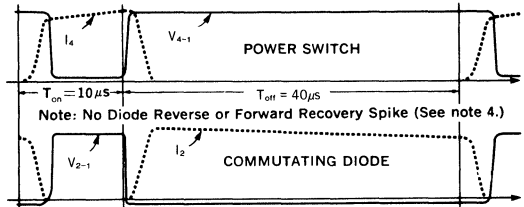
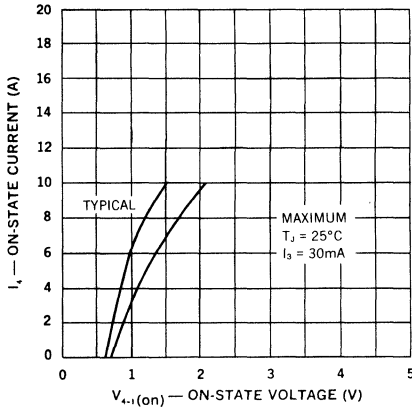


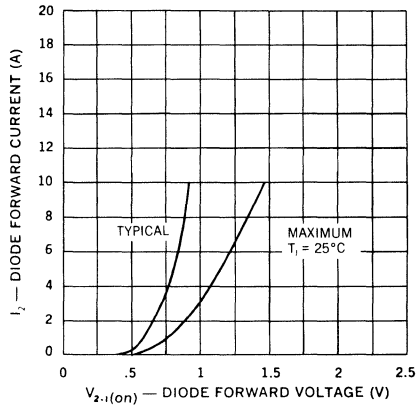
Figure 2. PIC660, 661, 662 Switching Waveforms



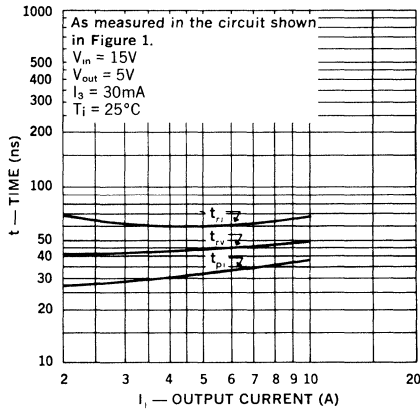
On-State Characteristics



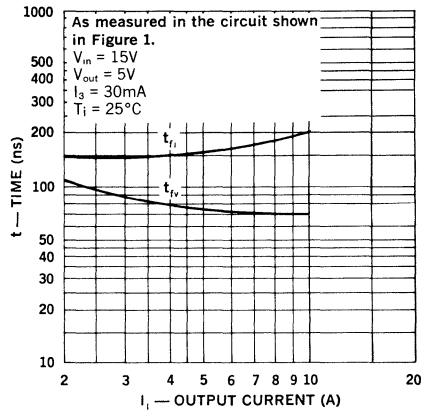
Diode Forward Characteristics



Turn-on Time



Fall Time



POWER INTEGRATED CIRCUIT

Schottky Switching Regulator 30A, 40V

Power Output Stages

PIC730
PIC740

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI
- High operating frequency (to 100kHz) results in smaller inductor-capacitor filter and improved power supply response time
- Low forward drop of Schottky Rectifier:
 $V_F = .6V$ at 20 A
- High Efficiency: 90% typ. @ 15A (see last page)

APPLICATIONS:

High efficiency and high current Buck or Flyback type switching regulator.

DESCRIPTION

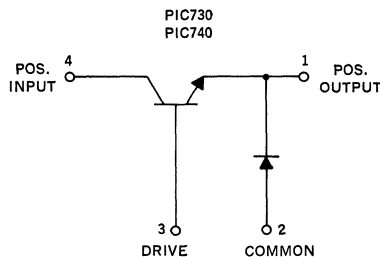
The Unitrode PIC700 series are unique hybrid circuits, specifically designed, constructed and specified for use in high current switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode.

Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitrode PIC700 series the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC700 series design and packaging, the designer is aided in overcoming two of the most

significant drawbacks to switching regulators: noise generation and slow response time.

The PIC700 series switching regulators are completely characterized over their entire operating range of $-55^{\circ}C$ to $+125^{\circ}C$. The devices are enclosed in a special 3 pin TO-3 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

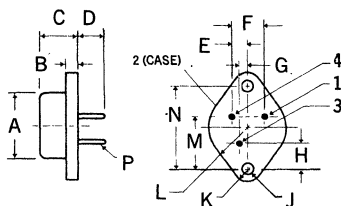
SCHEMATIC



MECHANICAL SPECIFICATIONS

NOTE:

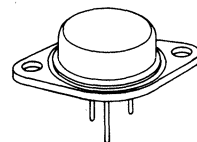
Leads may be soldered to within $1/16$ " of base provided temperature-time exposure is less than $260^{\circ}C$ for 10 seconds.



PIC730 PIC740

	ins.	mm
A	.875 MAX.	22.23 MAX.
B	.135	3.43
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.205-.225	5.21-5.72
F	.420-.440	10.67-11.18
G	.145-.165	3.68-4.19
H	.395-.405	10.03-10.29
J	.151-.161 DIA	3.84-4.09 DIA.
K	.188 MAX. RAD.	4.78 MAX. RAD
L	.525 MAX. RAD.	13.34 MAX. RAD
M	.708-.728	17.98-18.49
N	1.177-1.197	29.90-30.40
P	.038-.043 DIA	.97-1.09 DIA.

3 Pin TO-3



ABSOLUTE MAXIMUM RATINGS

	PIC730	PIC740
Input Voltage	30V	40V
Output Voltage	30V	40V
Drive-Input Reverse Voltage	7V	7V
Continuous Output Current	20A	20A
Peak Output Current	30A	30A
Drive Current	5A	5A
Thermal Resistance		
Junction to Case, θ_{j-c}		
Power Switch	1.0°C/W	
Commutating Diode	2.0°C/W	
Case to Ambient, θ_{c-a}		
Operating Temperature Range, T_C	-55°C to +125°C	
Maximum Junction Temperature, T_J	+150°C	
Storage Temperature Range	-65°C to +150°C	



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

SCHOTTKY RECTIFIER

Test	Symbol	PIC730		PIC740		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
Maximum Instantaneous Reverse Current	I_R	—	50	—	50	mA	$V_R = \text{rated}$, $T_C = 125^\circ\text{C}$ Pulse Width = 300 μs , Duty Cycle = 1 percent
Maximum Instantaneous Forward Voltage	V_F	—	0.6	—	0.6	V	$I_F = 20\text{A}$ $T_C = 125^\circ\text{C}$,

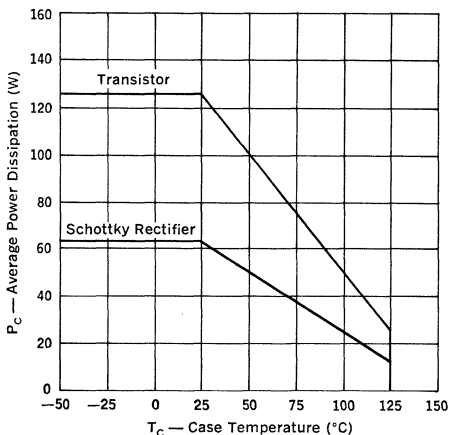
TRANSISTOR

Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 20\text{A}$ $I_B = 2.5\text{A}$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	—	1.5	—	1.5	V	$I_C = 20\text{A}$ $I_B = 2.5\text{A}$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CEO(sus)}$	30	—	40	—	V	$I_C = 100\text{mA}$	
Collector Cut-off Current	I_{CEO}	—	10	—	10	mA	$V_{CE} = 40\text{V}$ P.W. = 300 μs	
Emitter Cut-off Current	I_{EBO}	—	10	—	10	mA	$V_{EB} = 7\text{V}$ P.W. = 300 μs	
Resistive Switching Speed	Rise Storage Fall	t_r	—	500	—	500	nS	$V_{CC} = 30\text{V}$ $I_C = 20\text{A}$ $I_{B1} = I_{B2} = 2.5\text{A}$ $V_{BE(off)} = -4\text{V}$
		t_s	—	1.5	—	1.5	μS	
		t_f	—	250	—	250	nS	
Inductive Switching Speed	Current Fall	t_{ri}	300 TYP.		300 TYP.		nS	$T_J = 100^\circ\text{C}$ $V_{CC} = 30\text{V}$ $I_C = 20\text{A}$ $V_{clamp} = V_{CEO}$ $L = 175\mu\text{H}$ $I_{B1} = I_{B2} = 2.5\text{A}$
	Voltage Fall	t_{fv}	350 TYP.		350 TYP.		nS	

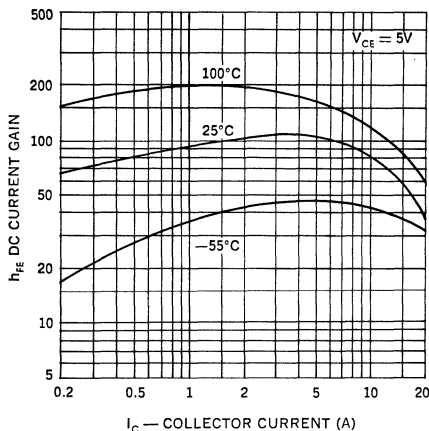
Notes

1. Pulse length=250 μs ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length = 50 μs ; duty cycle $\leq 1\%$.
Voltage clamped at maximum collector-emitter voltage.

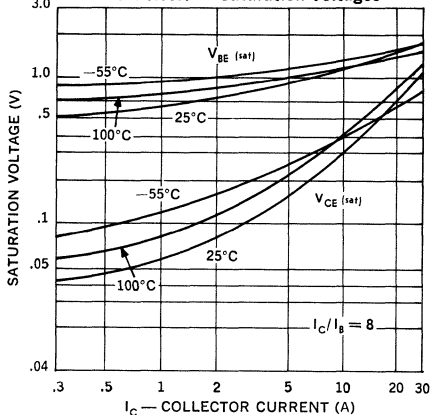
Power Dissipation



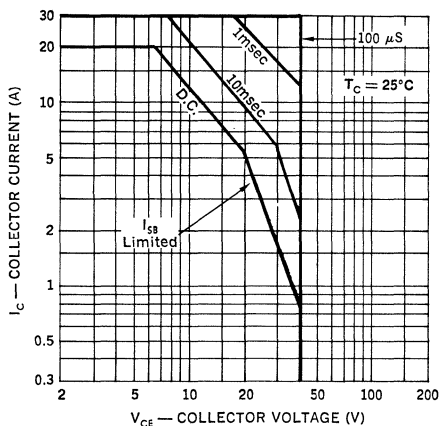
DC Current Gain



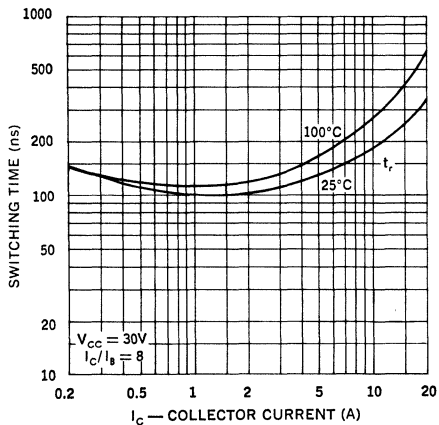
Transistor — Saturation Voltages



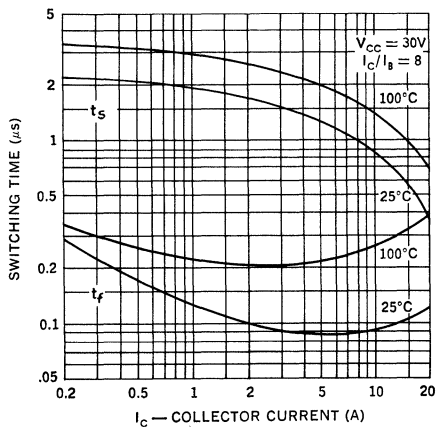
Forward Bias Safe Operating Area



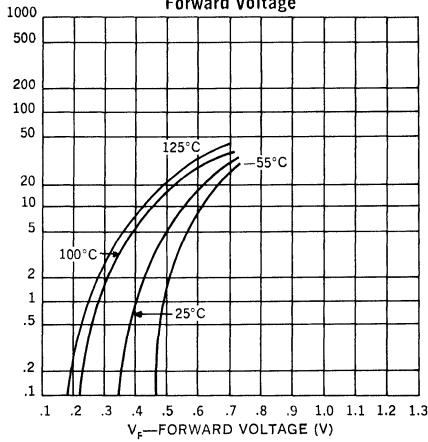
Resistive — Turn-On Time



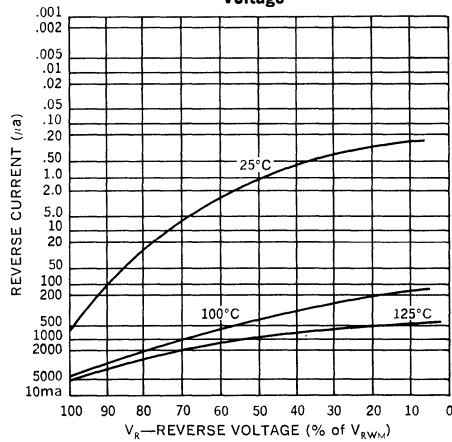
Resistive — Turn-Off Time



Rectifier — Forward Current vs Forward Voltage



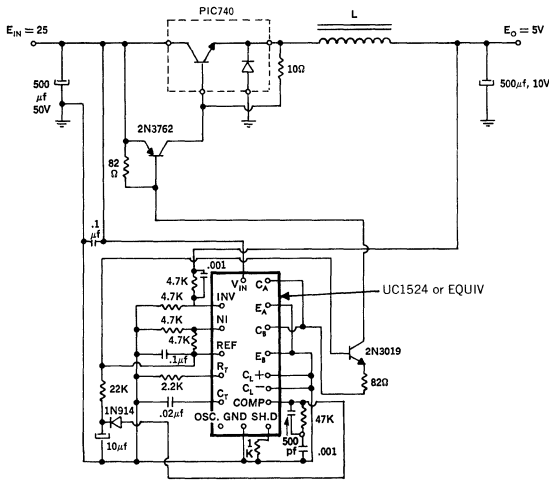
Rectifier — Typical Reverse Current vs Reverse Voltage



5

Possible Circuit Configurations

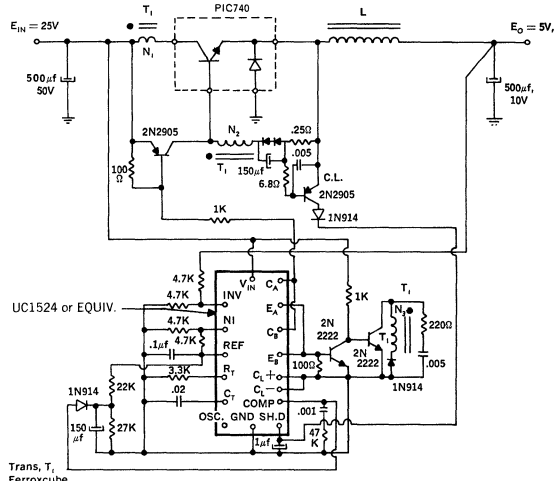
15 AMP SWITCHING REGULATOR
Pass Transistor — Unsaturated-Mode



INDUCTOR L
N = 35 turns
Wire size #18
Arnold A4-17172

Regulation18%
Typ. Efficiency at 15A 85%

15 AMP SWITCHING REGULATOR
Pass Transistor — Saturated-Mode



Trans, T₁, Ferroxcube core, 2616P-3B7
N₁ = 2,
N₂ = 16,
N₃ = 40,

INDUCTOR L
N = 35 turns,
Wire size #18
Arnold A4-17172

Regulation18%
Typ. Efficiency at 15A 90%

Unitrode Corporation makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

POWER INTEGRATED CIRCUIT

Switching Regulator 8A, 400V
Power Output Stages

PIC800
PIC801
PIC810
PIC811

FEATURES

- Designed and characterized for switching regulator applications
- Cost saving design reduces size, improves efficiency, reduces noise and RFI
- High operating frequency (to 100kHz) results in smaller inductor-capacitor filter and improved power supply response time
- High operating efficiency
- Electrically isolated, 4 PIN, TO-66 hermetic case
- Fast reverse recovery time of commutating diode
- Low capacitance between active components and case ($\approx 10\text{pf}$)

APPLICATIONS:

- PIC800/801 – High voltage Buck or Flyback regulator.
PIC810/811 – Single ended half bridge (2 required), Full bridge (4 required), Deflection circuits, DC motor drive.

DESCRIPTION

The Unitrode PIC800 series are power hybrid circuits, specifically designed, constructed and specified for use in high voltage switching regulator applications. The designer is thus relieved of one of the most time consuming, tedious and critical aspects of switching regulator design: choosing the appropriate switching transistors and commutating diode.

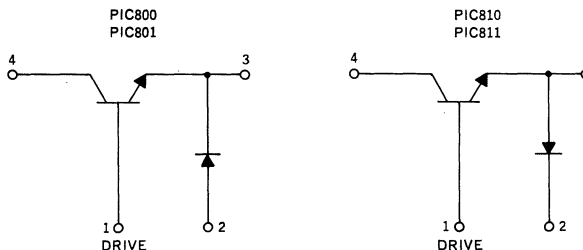
significant drawbacks to switching regulators: noise generation and slow response time; the reverse recovery time of the commutating diode is less than 50 nanoseconds. The capacitance between the active components and the package is about 10 picofarads.

Switching regulators, when compared to conventional regulators, result in significant reductions in size, weight, and internal power losses and a major decrease in overall cost. Using the Unitrode PIC800 series the designer can achieve further improvements in size, weight, efficiency, and costs. At the same time, because of the PIC800 series design and packaging, the designer is aided in overcoming two of the most

PIC800 series are completely characterized over their entire operating range of -55°C to $+125^{\circ}\text{C}$. The devices are enclosed in a special 4-pin TO-66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

Suggested circuit applications are listed on fourth page of this sheet.

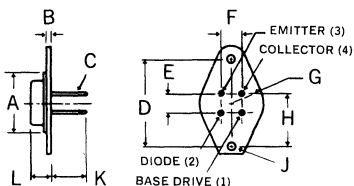
SCHEMATIC



MECHANICAL SPECIFICATIONS

NOTES:

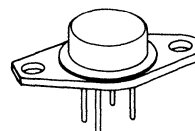
1. Case is electrically isolated.
2. Leads may be soldered to within $1/16$ " of base provided temperature-time exposure is less than 260°C for 10 seconds.



PIC800 PIC801 PIC810 PIC811

	ins.	mm
A	620 MAX	15.75 MAX
B	050-075	1.27-1.91
C	028-034	0.71-0.86
D	958-962	24.33-24.43
E	190-210	4.83-5.33
F	190-210	4.83-5.33
G	350 MAX RAD	8.89 MAX RAD
H	570-590	14.48-14.99
J	142-152 DIA	3.61-3.86 DIA
K	360 MIN	9.14 MIN
L	250-340	6.35-8.64

4-Pin TO-66



ABSOLUTE MAXIMUM RATINGS

PIC800 PIC801 PIC810 PIC811

PIC800-PIC810

PIC801-PIC811

Input Voltage	350V	400V
Output Voltage	350V	400V
Drive-Input Reverse Voltage	5V	5V
Peak Output Current	8A	8A
Continuous Output Current	5A	5A
Drive Current	2A	2A

Thermal Resistance

Junction to Case, θ_{J-C}		
Power Switch		2°C/W
Commutating Diode		3°C/W
Case to Ambient, θ_{C-A}		60.0°C/W
Operating Temperature Range, T_C		-55°C to +125°C
Maximum Junction Temperature, T_J		+150°C
Storage Temperature Range		-65°C to +150°C

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

RECTIFIER

Test	Symbol	PIC800-PIC810		PIC801-PIC811		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
Maximum Inst. Reverse Current $T_J = 25^\circ\text{C}$ $T_J = 100^\circ\text{C}$	I_R	—	20	—	20	μA	$V_R = \text{rated}$, Pulse Width = 300 μs , Duty Cycle = 1 percent
Maximum Forward Voltage $T_J = 25^\circ\text{C}$ $T_J = 100^\circ\text{C}$	V_F	—	1.25	—	1.25	V	$I_F = 3\text{A}$
DC Blocking Voltage	V_R	350	—	400	—	V	Pulse Width = 300 μs , $I_R = 20\mu\text{A}$
Maximum Reverse Recovery Time	t_{rr}	—	50	—	50	nS	$I_F = 1/2\text{A}$, $I_R = 1\text{A}$ $I_{REC} = .25\text{A}$

TRANSISTOR

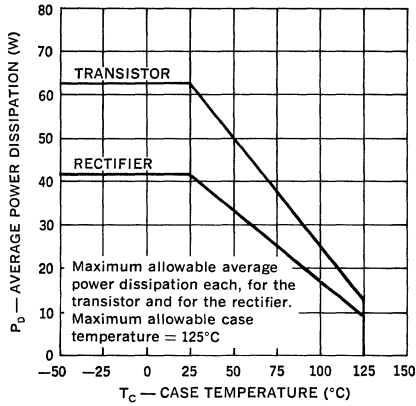
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	1.0	—	1.0	V	$I_C = 2.0\text{A}$, $I_B = 0.4\text{A}$	
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	$T_C = 25^\circ\text{C}$	—	1.5	—	1.5	V	$I_C = 5.0\text{A}$, $I_B = 1.0\text{A}$
		$T_C = 100^\circ\text{C}$	—	2.0	—	2.0		
Collector Saturation Voltage (Note 1)	$V_{CE(sat)}$	—	3.0	—	3.0	V	$I_C = 8.0\text{A}$, $I_B = 2.0\text{A}$	
Base Saturation Voltage	$V_{BE(sat)}$	—	1.2	—	1.2	V	$I_C = 2.0\text{A}$, $I_B = 0.4\text{A}$	
Base Saturation Voltage (Note 1)	$V_{BE(sat)}$	$T_C = 100^\circ\text{C}$	—	1.6	—	1.6	V	$I_C = 5.0\text{A}$, $I_B = 1.0\text{A}$
		$T_C = 25^\circ\text{C}$	—	1.5	—	1.5		
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CE(sus)}$	350	—	400	—	V	$I_C = 10\text{mA}$	
Collector-Emitter Sustaining Voltage (Note 2)	$V_{CE(sus)}$	350	—	400	—	V	$I_C = 3.0\text{A}$, $L = 180\mu\text{H}$ $I_{B1} = I_{B2} = 0.6\text{A}$ $V_{CE \text{ clamp}} = \text{rated } V_{CE(sus)}$	
Emitter-Base Cutoff Current	I_{EBO}	—	1	—	1	mA	$V_{EB} = 9\text{V}$	
Collector Cutoff Current	I_{CEV}	—	1.0	—	1.0	mA	$V_{CE} = 350\text{V}$, $V_{BE} = -1.5\text{V}$ $V_{CE} = 400\text{V}$, $V_{BE} = -1.5\text{V}$	
Collector Cutoff Current, $T_C = 100^\circ\text{C}$	I_{CEV}	—	5	—	5	mA	$V_{CE} = 350\text{V}$, $V_{BE} = -1.5\text{V}$ $V_{CE} = 400\text{V}$, $V_{BE} = -1.5\text{V}$	
Output Capacitance, Common Base	C_{obo}	110	Typ	110	Typ	pF	$V_{CB} = 10\text{V}$, $f = 1\text{MHz}$	
Gain-Bandwidth Product	F_T	4	—	4	—	MHz	$V_{CE} = 10\text{V}$, $I_C = 0.5\text{A}$, $f = 1\text{MHz}$	
Energy Second Breakdown (unclamped)	$E_{S/b}$	180	—	180	—	μJ	$I_C = 3.0\text{A}$, $V_{BE(off)} = 4\text{V}$ $I_{B1} = 0.6\text{A}$ $L = 40\mu\text{H}$ unclamped	
Resistive Switching Speeds	Delay Time	t_d	—	0.1	—	0.1	μs	$I_C = 5.0\text{A}$ $V_{CC} = 125\text{V}$ $I_{B1} = I_{B2} = 1\text{A}$ $V_{BE(off)} = 5\text{V}$
	Rise Time	t_r	—	0.8	—	0.8		
	Storage Time	t_s	—	2.0	—	2.0		
	Fall Time	t_f	—	0.4	—	0.4		
Inductive Switching Speeds $T_C = 100^\circ\text{C}$	Storage Time	t_s	—	2.3	—	2.3	μs	$I_C = 5.0\text{A}$, $V_{BE(off)} = 5\text{V}$ $I_{B1} = I_{B2} = 1\text{A}$ $V_{CE \text{ clamp}} = \text{rated } V_{CE(sus)}$
	Fall Time	t_f	—	0.4	—	0.4		

Notes

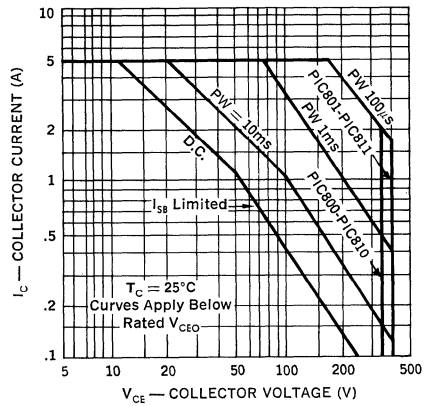
1. Pulse length = 250 μs ; duty cycle $\leq 1\%$.
2. Sustaining Voltage. Measured at a high current point where collector-emitter voltage is lowest. Current pulse length = 50 μs ; duty cycle $\leq 1\%$. Voltage clamped at maximum collector-emitter voltage.



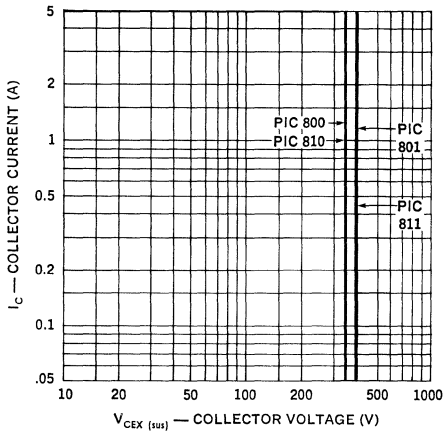
Power Dissipation



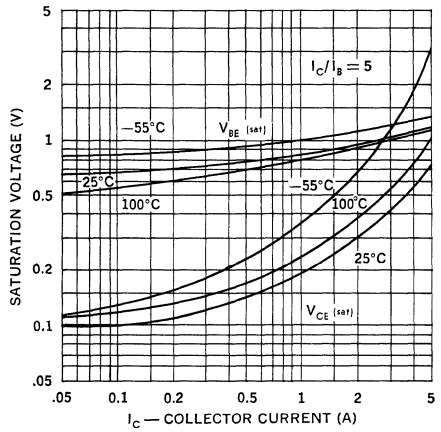
Forward Bias Safe Operating Area



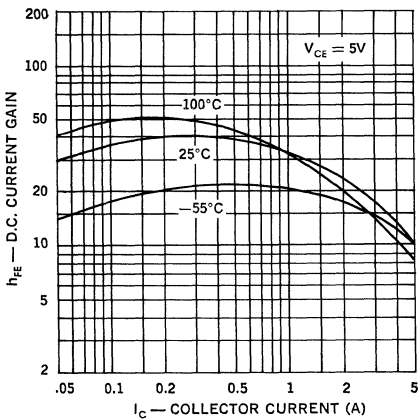
Reverse Biased Safe Operating Area



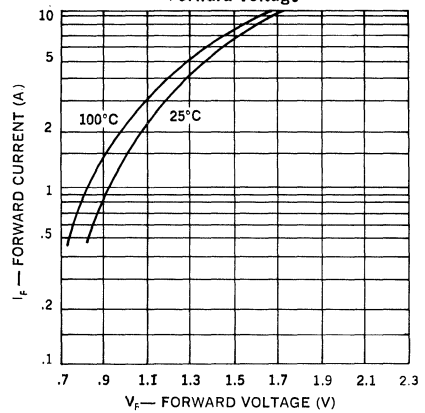
Saturation Voltages



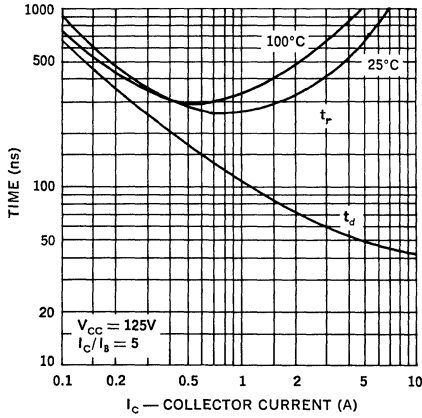
D.C. Current Gain



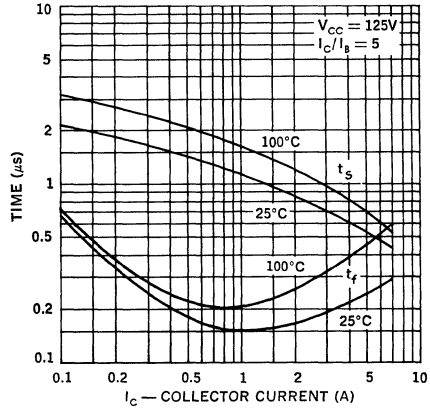
Rectifier — Forward Current vs Forward Voltage



Resistive — Turn-On Time



Resistive — Turn-Off Time



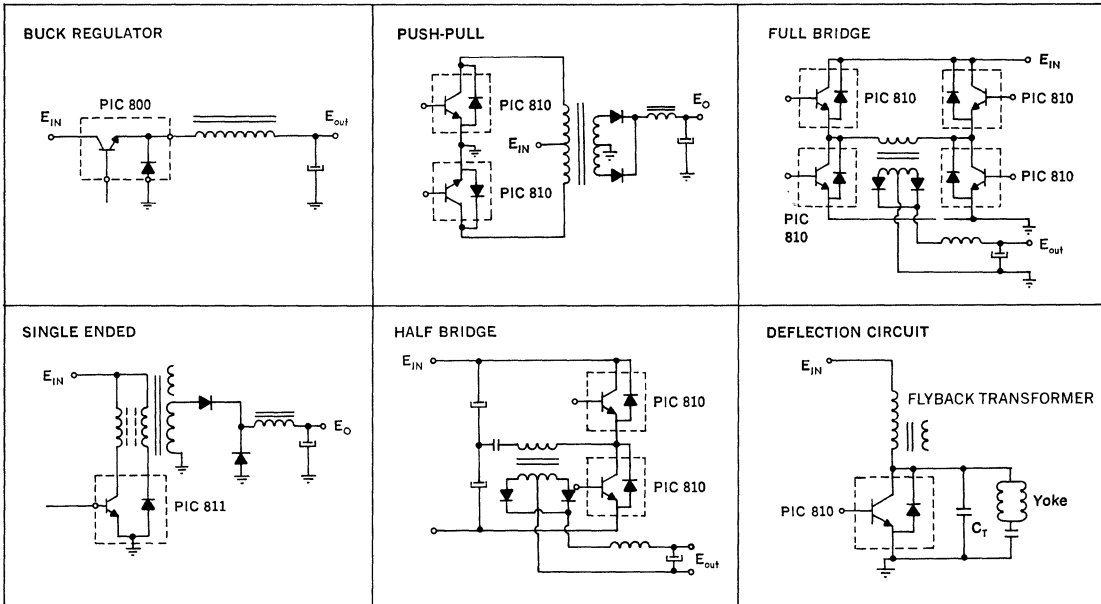
Typical Inductive Switching Times

$$\frac{I_C}{5} = I_{B1} = -I_{B2}, V(\text{clamp}) = 350V$$

$$V_{CC} = 125V$$

Current	Temp.	t_s μS	t_{fv} nS	t_{fi} nS
$I_C = 1A$	25°C	1.2	120	160
	100°C	1.76	140	185
$I_C = 3A$	25°C	.8	100	100
	100°C	1.1	170	130
$I_C = 5A$	25°C	.9	80	100
	100°C	1.0	190	140

APPLICATIONS:



POWER INTEGRATED CIRCUIT

H-Bridge Power Output Stage

5A, 100V

PIC900B
 PIC900C
 PIC900D

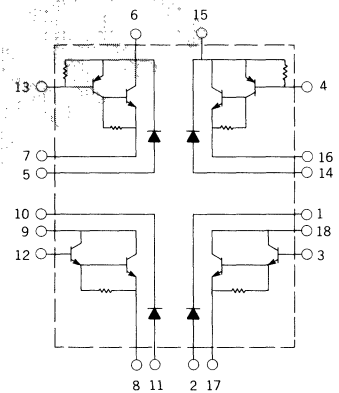
FEATURES

- Designed and characterized for inductive loads such as
 - Stepper Motor Drivers
 - DC Motor Drivers
 - Full Bridge DC Converters
- Fast switching times with low (5mA) drive current
- Electrically isolated 18 pin dual-in-line package with integral heat spreader
- Compatible with automatic insertion

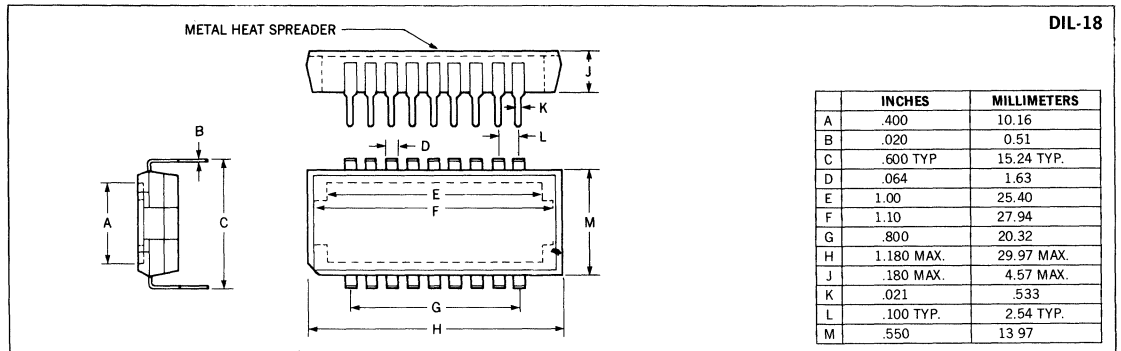
DESCRIPTION

The PIC900 is a unique hybrid circuit specifically designed to simplify construction of bipolar stepper motor controls and fullbridge DC converters. The matched transistors and drivers allow low saturation voltages and consistent thermal response. The low drive current insures compatibility with appropriate driver logic. The hybrid circuit construction utilizes thick-film resistors on an alumina substrate for maximum thermal conductivity and resultant low thermal impedance. All the active elements in the hybrid are fully passivated. Isolation between the active circuit and the metal heat spreader exceeds 3kV.

SCHEMATIC



MECHANICAL SPECIFICATIONS



ABSOLUTE MAXIMUM RATINGS

	PIC900B	PIC900C	PIC900D
Transistor, Collector-Emitter Voltage, V_{CE0}	60V	80V	100V
Transistor, DC Collector Current, I_C		5A	
Diode, DC Blocking Voltage	60V	80V	100V
Diode, Forward DC Current		5A	
Diode, Reverse Recovery Time, t_{rr}		50ns max.	
Thermal Resistance			
Junction to Case, θ_{j-c}			
Power Switch		4.5°C/W	
Clamp Diode		4.5°C/W	
Operating Temperature Range, T_C		-55°C to +125°C	
Maximum Junction Temperature, T_j		+150°C	
Storage Temperature Range		-65°C to +150°C	

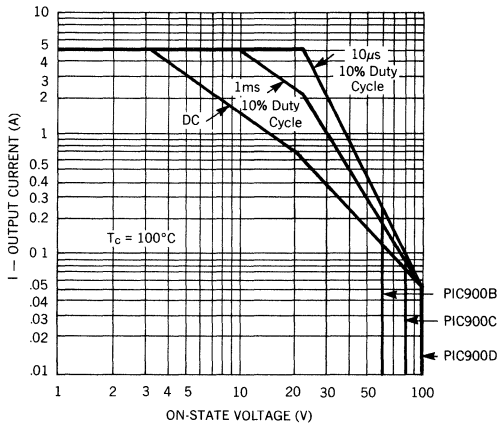


ELECTRICAL CHARACTERISTICS (at 25°C unless noted)

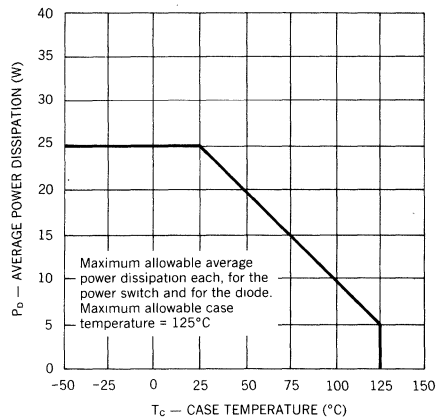
Test	Symbol	PNP Drive			NPN Drive			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
On-State Voltage (Note 1)	V_{CE}	—	1.0	1.5	—	1.0	1.5	V	$I_C = 2A, I_B = -5mA (5mA)$
On-State Voltage (Note 1)	V_{CE}	—	1.2	2.2	—	1.2	2.2	V	$I_C = 5A, I_B = -5mA (5mA)$
Diode Forward Voltage (Note 1)	V_F	—	0.8	1.1	—	0.8	1.1	V	$I_F = 2A$
Diode Forward Voltage (Note 1)	V_F	—	1.0	1.5	—	1.0	1.5	V	$I_F = 5A$
Off-State Current	I_{CEO}	—	0.1	10	—	0.1	10	μA	$V_{CE} = \text{rated voltage}$
Off-State Current	I_{CEO}	—	10	—	—	10	—	μA	$V_{CE} = \text{rated voltage}, T_A = 100^\circ C$
Diode Reverse Current	I_R	—	1.0	10	—	1.0	10	μA	$V_R = \text{rated voltage}$
Diode Reverse Current	I_R	—	500	—	—	500	—	μA	$V_R = \text{rated voltage}, T_A = 100^\circ C$
Current Delay Time	t_{di}	—	90	—	—	90	—	ns	
Current Rise Time	t_{ri}	—	65	150	—	65	150	ns	
Voltage Rise Time	t_{rv}	—	50	100	—	50	100	ns	$V_{CE} = 50V$
Voltage Storage Time	t_{sv}	—	850	1800	—	850	1800	ns	$I_C = 2A$
Voltage Fall Time	t_{fv}	—	500	800	—	500	800	ns	$I_B = 5mA$
Current Fall Time	t_{fi}	—	180	400	—	180	400	ns	

NOTE: 1. Pulse test: duration = 300 μs , duty cycle \leq 2%.

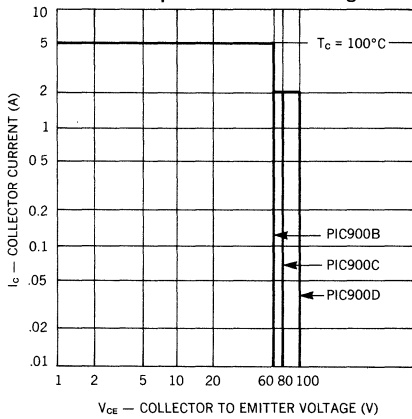
Forward Bias Safe Operating Area



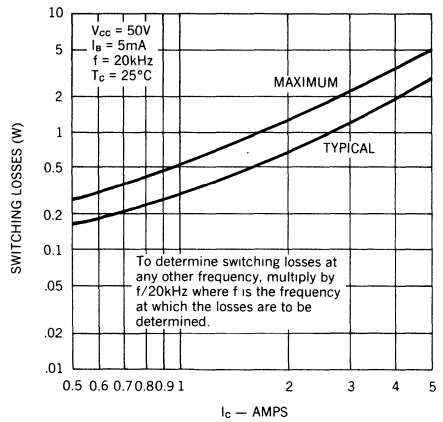
Power Dissipation



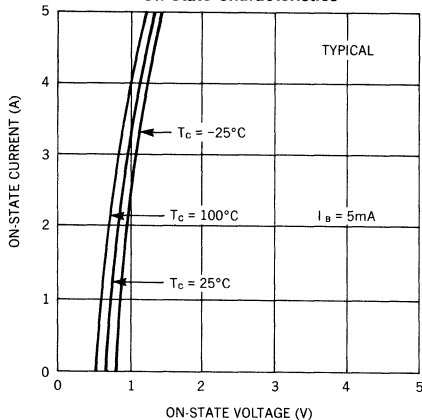
Reverse Bias Safe Operating Area Clamped Inductive Switching



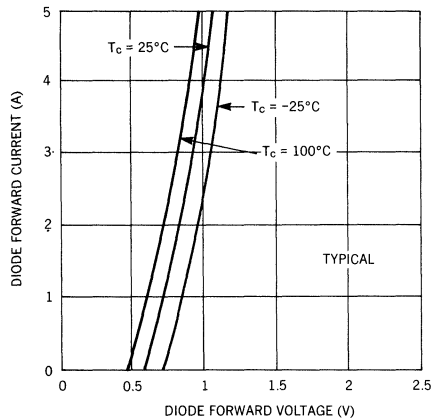
Switching Losses — Single Switch



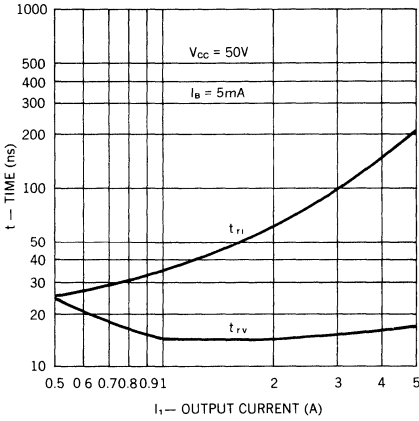
Power Darlington On-State Characteristics



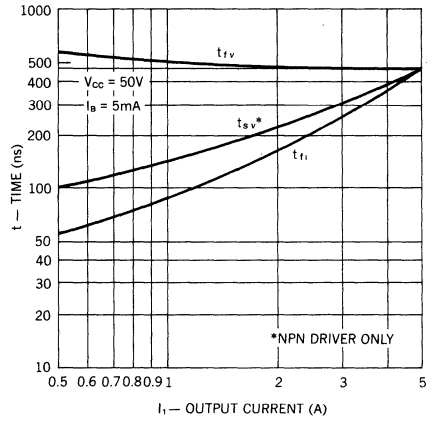
Diode Forward Characteristics



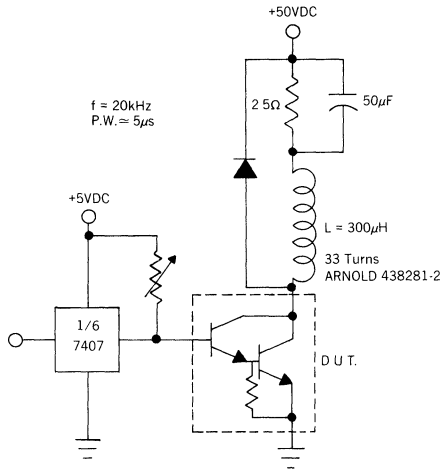
Turn-On Time



Turn-Off Time

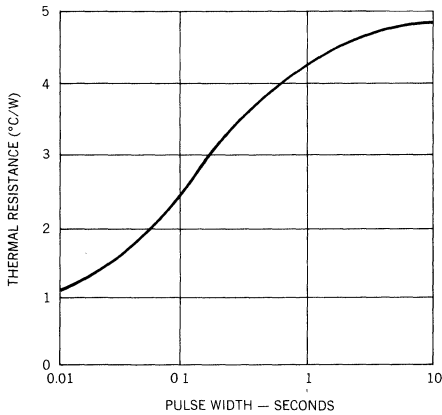


5



Switching Speed Test Circuit

Transient Thermal Impedance Plot



Effective Thermal Impedance

$$\theta_b = R_T \times D + (1-D) r(t + \tau) - r(\tau) + r(t)$$

WHERE:

t = PULSE WIDTH

τ = PERIOD

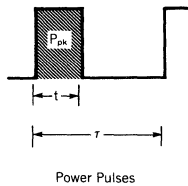
DUTY CYCLE, $D = \frac{t}{\tau}$

PEAK POWER, P_{pk} IS PEAK OF AN EQUIVALENT SQUARE POWER PULSE

$r(t + \tau)$ = TRANSIENT RESISTANCE AT TIME $t + \tau$

$r(t)$ = TRANSIENT THERMAL RESISTANCE AT TIME t

R_T = DC THERMAL RESISTANCE (FROM DATA SHEETS)



If a socket is desired for use during circuit breadboarding, any DIP socket for 24 pins or more will accommodate the 0.6" (15.24mm) row spacing of the DIL-18 package

TYPICAL APPLICATIONS OF THE PIC900

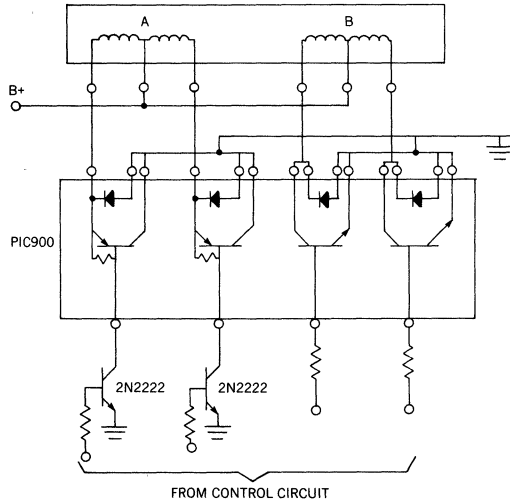
Drive Requirements

The 2N2222 transistors are used to level shift the input signal from ground to the B+ level for the PNP Darlingtonton when required by the application. Almost any small signal transistor of the appropriate voltage rating can be used since it handles only the 5mA (minimum) drive current to the PIC900. Note the use of the current limiting resistor in series with the collector of the 2N2222s where needed.

The drive current spec of 5mA minimum should be observed using worst case design, for applications where minimum current drain is required. Otherwise a 10mA typical value may be used.

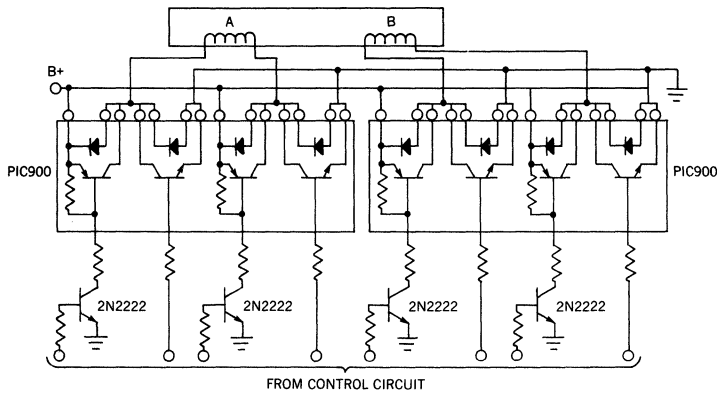
Basic Drive Circuits - Figures 1 and 2

The basic application of the PIC900 to unipolar and bipolar stepper motors is shown in Figures 1 and 2. These are shown as simple L/1R systems.



FROM CONTROL CIRCUIT

Figure 1. Unipolar Drive



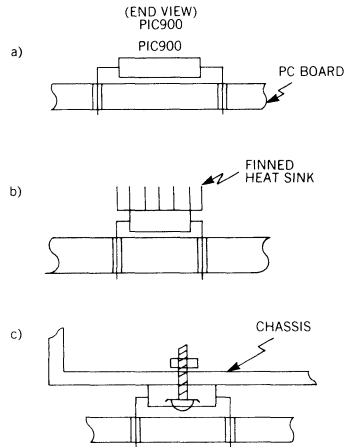
FROM CONTROL CIRCUIT

Figure 2. Bipolar Drive

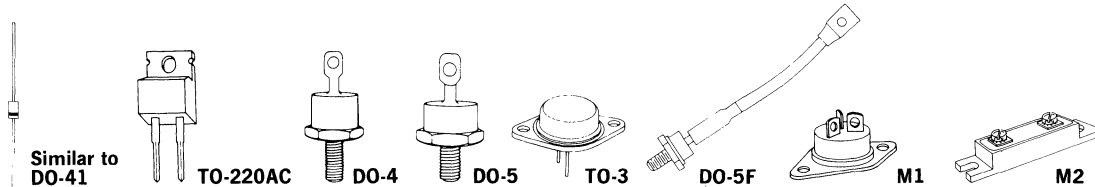
PIC900 Mounting Considerations

The PIC900 is designed to be used with or without additional heat sinking. The PIC900 heat spreader is electrically isolated from the active devices, so a variety of heat sinking methods can be used. Most of the active chips are mounted directly on the copper lead frame to facilitate heat flow through the leads.

- a) PIC900 DIP leads soldered in PC board. Copper leads are designed to pull heat out of chips. Typical mounting for up to 2A average, or up to 5A peak at low duty factor.
- b) PC board mounting by its leads, plus small finned heat sink attached to PIC900 heat spreader using clips, or adhesive.
- c) Heat spreader attached to large heat sink or chassis. Two screws with washers to hold down each end of package.



SCHOTTKY RECTIFIERS



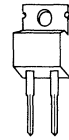
AVERAGE DC OUTPUT CURRENT		1A	1A	3A	6A	8A	12A ¹	12A	16A ²	16A
PEAK REVERSE VOLTAGE	PKG	Similar to DO-41 (ASA)	Similar to DO-41 (ASB)	Similar to DO-201AD	TO-220 PLASTIC (2 LEAD)	TO-220 PLASTIC (2 LEAD)	TO-220 PLASTIC (3 LEAD)	TO-220 PLASTIC (2 LEAD)	TO-220 PLASTIC (3 LEAD)	TO-220 PLASTIC (2 LEAD)
	20V	TYPE V _F I _{FSM}	1N5817 .45 @ 1A 25A	USD1120 .45 @ 1A 50A	1N5820 .475 @ 3A 80A	USD620 .55 @ 6A 150A	USD720 .55 @ 8A 200A	USD620C .65 @ 12A 150A	USD820 .45 @ 12A 200A	USD720C .65 @ 16A 200A
30V	TYPE V _F I _{FSM}	1N5818 .55 @ 1A 25A	USD1130 .475 @ 1A 50A	1N5821 .50 @ 3A 80A						
35V	TYPE V _F I _{FSM}				USD635 .55 @ 6A 150A	USD735 .55 @ 8A 200A	USD635C .65 @ 12A 150A	USD835 .45 @ 12A 200A	USD735C .65 @ 16A 200A	USD935 .50 @ 16A 250A
40V	TYPE V _F I _{FSM}	1N5819 .60 @ 1A 25A	USD1140 .50 @ 1A 50A	1N5822 .525 @ 3A 80A	USD640 .55 @ 6A 150A	USD740 .55 @ 8A 200A	USD640C .65 @ 12A 150A	USD840 .45 @ 12A 200A	USD740C .65 @ 16A 200A	USD940 .50 @ 16A 250A
45V	TYPE V _F I _{FSM}				USD645 .55 @ 6A 150A	USD745 .55 @ 8A 200A	USD645C .65 @ 12A 150A	USD845 .45 @ 12A 200A	USD745C .65 @ 16A 200A	USD945 .50 @ 16A 250A

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AVERAGE DC OUTPUT CURRENT		25A	30A ³	50A	60A	75A	100A	200A
PEAK REVERSE VOLTAGE	PKG	DO-4 STUD	TO-3	DO-5 STUD	DO-5 DO-5F STUD	DO-5 DO-5F STUD	POWER TAB M1	POWER BLOCK M2
	20V	TYPE V _F I _{FSM}		USD320C .6 @ 20A 400A			USD520 .6 @ 60A 1000A	
30V	TYPE V _F I _{FSM}			1N6097 .86 @ 157A 800A				
35V	TYPE V _F I _{FSM}		USD335C .6 @ 20A 400A		USD6035 .6 @ 60A 800A	USD535 .6 @ 60A 1000A		
40V	TYPE V _F I _{FSM}			1N6098 .86 @ 157A 800A			USM140C .775 @ 100A 1000A	USM20040C .745 @ 200A 2000A
45V	TYPE V _F I _{FSM}	1N6391 ⁵	USD345C SD241		1N6392 ⁵ USD6045 SD51 ⁴	USD545	USM145C	USM20045C
50V	TYPE V _F I _{FSM}	.68 @ 50A 600A	.6 @ 20A 400A		.6 @ 60A 800A	.6 @ 60A 1000A	.775 @ 100A 1000A	.745 @ 200A 2000A
50V	TYPE V _F I _{FSM}					USD550 .6 @ 60A 1000A	USM150C .775 @ 100A 1000A	USM20050C .745 @ 200A 2000A

- Center-tap 6A per leg.
- Center-tap 8A per leg.
- Center-tap 15A per leg.
- V_{RRM} @ 25°C is 45V, V_{RRM} @ 150°C is 35V.
- Available as JAN, JANTX, JANTXV.

RECTIFIERS

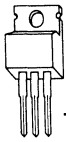


TO-220AC

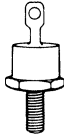
ULTRA-FAST RECOVERY (t_{rr} — 25 to 50ns)

Average D.C. Output Current		1A	2A	2.5A	5A	6A	8A	16A
Package Style		A	A	A	B	B	TO-220AC	TO-220AC
Peak Inverse Voltage	50V	UES1001 .895 @ 1A 25ns		1N5802* UES1101 .895 @ 2A 25ns		1N5807* UES1301 .850 @ 6A 30ns	UES1401 .895 @ 8A 35ns	UES1501 .975 @ 16A 35ns
	75V			1N5803 .895 @ 1A 25ns		1N5808 .850 @ 6A 30ns		
	100V	UES1002 .895 @ 1A 25ns		1N5804* UES1102 .895 @ 2A 25ns		1N5809* UES1302 .850 @ 6A 30ns	UES1402 .895 @ 8A 35ns	UES1502 .975 @ 16A 35ns
	125V			1N5805 .895 @ 1A 25ns		1N5810 .850 @ 6A 30ns		
	150V	UES1003 .895 @ 1A 25ns		1N5806* UES1103 .895 @ 2A 25ns		1N5811* UES1303 .850 @ 6A 30ns	UES1403 .895 @ 8A 35ns	UES1503 .975 @ 16A 35ns
	200V		UES1104 1.15 @ 1A 50ns		UES1304 1.15 @ 3A 50ns			UES1504 .975 @ 16A 35ns
	300V		UES1105 1.15 @ 1A 50ns		UES1305 1.15 @ 3A 50ns			
	400V		UES1106 1.15 @ 1A 50ns		UES1306 1.15 @ 3A 50ns			

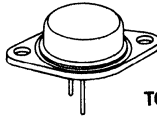
*Available as JAN, JANTX, JANTXV



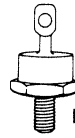
TO-220AB



DO-4



TO-3



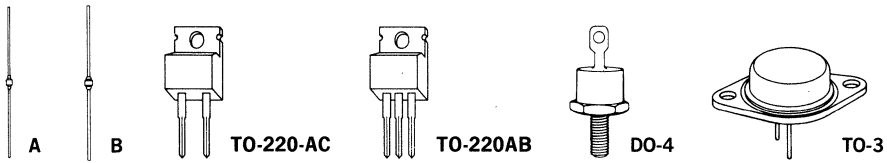
DO-5

ULTRA-FAST RECOVERY (t_r — 25 to 50ns)

Average D.C. Output Current		16A Center-Tap	20A	25A	30A Center-Tap	50A	70A	
Package Style		TO-220AB	DO-4	DO-4	TO-3	DO-5	DO-5	
Peak Inverse Voltage	50V	V_F t_{rr}	UES2401 .895 @ 8A 35ns		1N5812* UES701 .825 @ 25A 35ns	UES2601 .825 @ 15A 35ns	1N6304 UES801 .84 @ 70A 50ns	
	75V	V_F t_{rr}		1N5813 .825 @ 25A 35ns				
	100V	V_F t_{rr}	UES2402 .895 @ 8A 35ns		1N5814* UES702 .825 @ 25A 35ns	UES2602 .825 @ 15A 35ns	1N6305 UES802 .84 @ 70A 50ns	
	125V	V_F t_{rr}		1N5815 .825 @ 25A 35ns				
	150V	V_F t_{rr}	UES2403 .895 @ 8A 35ns		1N5816* UES703 .825 @ 25A 35ns	UES2603 .825 @ 15A 35ns	1N6306 UES803 .84 @ 70A 50ns	
	200V	V_F t_{rr}	UES2404 .895 @ 8A 35ns	UES704 1.15 @ 20A 50ns		UES2604 1.15 @ 15A 50ns	UES804 1.15 @ 50A 50ns	
	300V	V_F t_{rr}		UES705 1.15 @ 20A 50ns		UES2605 1.15 @ 15A 50ns	UES805 1.15 @ 50A 50ns	
	400V	V_F t_{rr}		UES706 1.15 @ 20A 50ns		UES2606 1.15 @ 15A 50ns	UES806 1.15 @ 50A 50ns	

*Available as JAN, JANTX, JANTXV

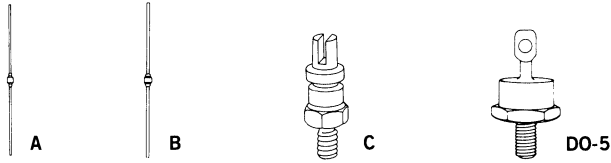
RECTIFIERS



SUPER-FAST RECOVERY (t_{rr} - 75 to 100ns)

Average D.C. Output Current			1A	2A	2A	3A	4A
Package Style			A	A	A	B	B
Peak Inverse Voltage	50V	V_F t_{rr}	UTX105 1.00 @ .5A 75ns	UTX205 1.0V @ 1A 75ns	SES5001 .975 @ 1A 100ns	UTX3105 1V @ 2A 100ns	UTX4105 1V @ 3A 100ns
	100V	V_F t_{rr}	UTX110 1.0V @ .5A 75ns	UTX210 1.0V @ 1A 75ns	SES5002 .975 @ 1A 100ns	UTX3110 1.0V @ 2A 100ns	UTX4110 1.0V @ 3A 100ns
	150V	V_F t_{rr}	UTX115 1.00 @ .5A 75ns	UTX215 1.0V @ 1A 75ns	SES5003 .975 @ 1A 100ns	UTX3115 1.0V @ 2A 100ns	UTX4115 1.0V @ 3A 100ns
	200V	V_F t_{rr}	UTX120 1.00 @ 1A 75ns	UTX220 1.0V @ 1A 75ns		UTX3120 1.0V @ 2A 100ns	UTX4120 1.0V @ 3A 100ns
	250V	V_F t_{rr}	UTX125 1.00 @ .5A 75ns	UTX225 1.0V @ 1A 75ns			

Average D.C. Output Current			5A	8A	16A Center-Tap	16A	20A	25A Center-Tap	60A
Package Style			B	TO-220AB	TO-220AC	TO-220AC	DO-4	TO-3	DO-5
Peak Inverse Voltage	50V	V_F t_{rr}	SES5301 .975 @ 5A 100ns	SES5401 1.025 @ 8A 100ns	SES5401C 1.025 @ 8A 100ns	SES5501 1.025 @ 16A 100ns	SES5701 .83 @ 20A 100ns	SES5601C .83 @ 12.5A 100ns	SES5801 .85 @ 60A 100ns
	100V	V_F t_{rr}	SES5302 .975 @ 5A 100ns	SES5402 1.025 @ 8A 100ns	SES5402C 1.025 @ 8A 100ns	SES5502 1.025 @ 16A 100ns	SES5702 .83 @ 20A 100ns	SES5602C .83 @ 12.5A 100ns	SES5802 .85 @ 60A 100ns
	150V	V_F t_{rr}	SES5303 .975 @ 5A 100ns	SES5403 1.025 @ 8A 100ns	SES5403C 1.025 @ 8A 100ns	SES5503 1.02 @ 16A 100ns	SES5703 .83 @ 20A 100ns	SES5603C .83 @ 12.5A 100ns	SES5803 .85 @ 60A 100ns
	200V	V_F t_{rr}		SES5404 1.025 @ 8A 100ns	SES5404C 1.025 @ 8A 100ns	SES5504 1.02 @ 16A 100ns			



FAST RECOVERY (t_{rr} — 150 to 500ns)

Average D.C. Output Current		1A	1A	2A	3A	3A	4A	6-9A	
Package Style		A	A	A	B	B	B	C	
Peak Inverse Voltage	50V	V_F t_{rr}	UTR01 1.1V @ .5A 250ns		UTR02 1.1V @ 1A 250ns	UTR3305 1.1V @ 3A 250ns	1N5415* 1.5V @ 9A 150ns	UTR4305 1.1V @ 4A 250ns	UTR4405 UTR5405 UTR6405 1.1V @ 6A 300ns
	100V	V_F t_{rr}	UTR11 1.1V @ .5A 250ns		UTR12 1.1V @ 1A 250ns	UTR3310 1.1V @ 3A 250ns	1N5416* 1N5186** 1.5V @ 9A 150ns	UTR4310 1.1V @ 4A 250ns	UTR4410 UTR5410 UTR6410 1.1V @ 6A 300ns
	200V	V_F t_{rr}	UTR21 1.1V @ .5A 250ns	1N4942* 1N5615* 1.3V @ 1A 150ns	UTR22 1.1V @ 1A 250ns	UTR3320 1.1V @ 3A 250ns	1N5417* 1N5187** 1.5V @ 9A 150ns	UTR4320 1.1V @ 4A 250ns	UTR4420 UTR5420 UTR6420 1.1V @ 6A 400ns
	300V	V_F t_{rr}	UTR31 1.1V @ .5A 300ns		UTR32 1.1V @ 1A 300ns				
	400V	V_F t_{rr}	UTR41 1.1V @ .5A 350ns	1N4944* 1N5617* 1.3V @ 1A 150ns	UTR42 1.1V @ 1A 350ns	UTR3340 1.1V @ 3A 300ns	1N5418* 1N5188** 1.5V @ 9A 150ns	UTR4340 1.1V @ 4A 400ns	UTR4440 UTR5440 UTR6440 1.1V @ 6A 500ns
	500V	V_F t_{rr}	UTR51 1.1V @ .5A 400ns		UTR52 1.1V @ 1A 400ns	UTR3350 1.1V @ 3A 350ns	1N5419* 1.5V @ 9A 250ns	UTR4350 1.1V @ 4A 400ns	
	600V	V_F t_{rr}	UTR61 1.1V @ .5A 400ns	1N4946* 1N5619* 1.3V @ 1A 250ns	UTR62 1.1V @ 1A 400ns	UTR3360 1.1V @ 3A 400ns	1N5420* 1N5190** 1.5V @ 9A 400ns	UTR4360 1.1V @ 4A 400ns	

* Available as JAN, JANTX, JANTXV
 ** Available as JAN, JANTX

RECTIFIERS

JAN & JANTX 1N3611-1N3614

Military Approved, 1 Amp,
General Purpose

FEATURES

- Qualified to MIL-S-19500/228
- Continuous Rating: 1A
- Surge Rating: 30A
- PIV: to 800V

DESCRIPTION

This series of MIL approved JAN and JANTX general purpose 1amp rectifiers are useful in many high rel applications.

ABSOLUTE MAXIMUM RATINGS

Peak Reverse Voltage Min.	Reverse Working Voltage	Type
240V	200V	JAN & JANTX 1N3611
480V	400V	JAN & JANTX 1N3612
720V	600V	JAN & JANTX 1N3613
920V	800V	JAN & JANTX 1N3614

Maximum Average D.C. Output Current

@ $T_A = 100^\circ\text{C}$ 1.0A

@ $T_A = 150^\circ\text{C}$ 0.3A

Non-Repetitive Sinusoidal

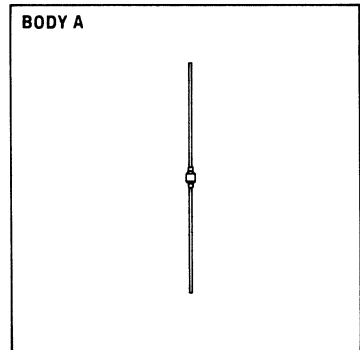
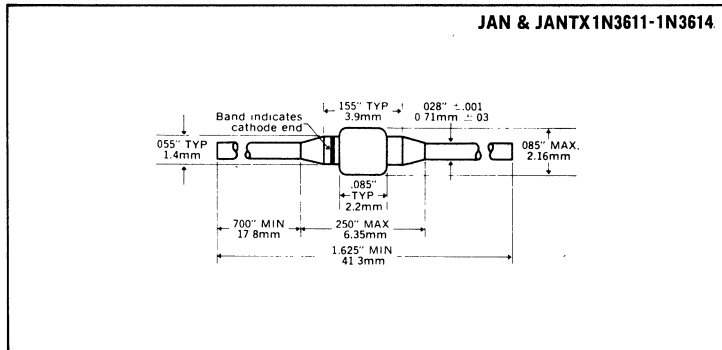
Surge Current (8.3ms) 30A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Thermal Resistance See Lead Temperature Derating Curve

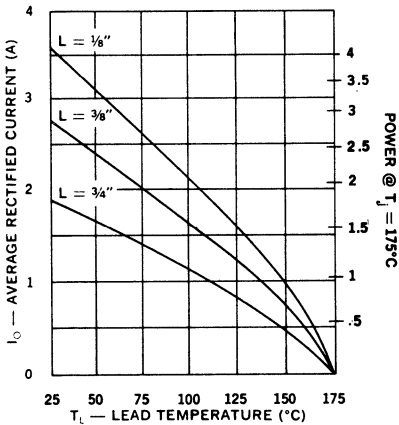
MECHANICAL SPECIFICATIONS



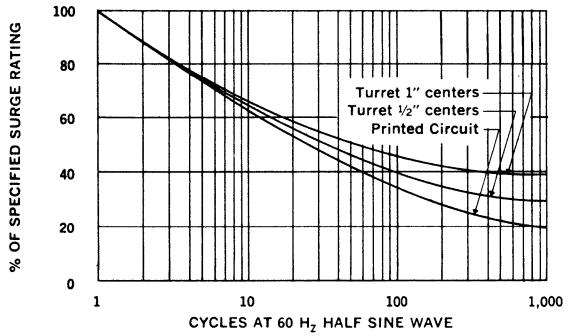
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Reverse D.C. Voltage	Minimum Reverse Breakdown Voltage @ 100 μ A	Peak Forward Voltage		Maximum D.C. Reverse Current at D.C. Voltage	
			Min.	Max.	25°C	150°C
JAN & JANTX 1N3611	200V	240V	0.6V	1.1V(pk) @ 1.0A	1 μ A	300 μ A
JAN & JANTX 1N3612	400V	480V				
JAN & JANTX 1N3613	600V	720V				
JAN & JANTX 1N3614	800V	920V				

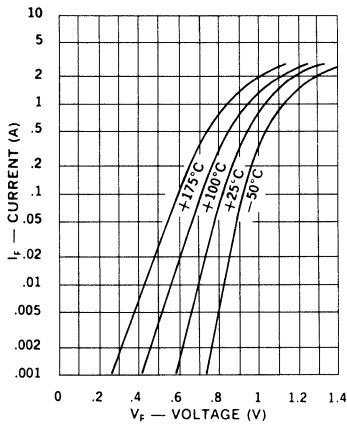
Maximum Current vs Lead Temperature



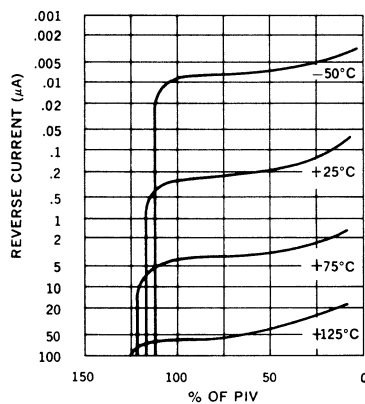
Allowable Forward Surge vs Number of Cycles



Typical Forward Current vs Forward Voltage



Typical Reverse Current vs PIV



6

RECTIFIERS

Military Approved, 1 Amp,
General Purpose

1N4245-1N4249
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/286
- Surge Rating: 25A
- PIV: to 1000 V
- Controlled Avalanche
- No Plastic, Epoxy, Silicone, Oxides, Gases or Solder are used

DESCRIPTION

This series of general purpose power rectifiers are available as JAN, JANTX or JANTXV for many power supply applicatons.

ABSOLUTE MAXIMUM RATINGS

Maximum Reverse Voltage	Type
200V	JAN, JANTX, JANTXV 1N4245
400V	JAN, JANTX, JANTXV 1N4246
600V	JAN, JANTX, JANTXV 1N4247
800V	JAN, JANTX, JANTXV 1N4248
1000V	JAN, JANTX, JANTXV 1N4249

Maximum Average D.C. Output Current

@ $T_A = 100^\circ\text{C}$ 1.0A

@ $T_A = 150^\circ\text{C}$ 0.333A

Non-Repetitive Sinusoidal

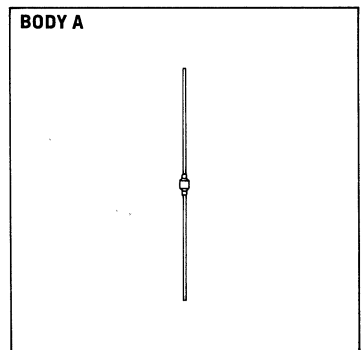
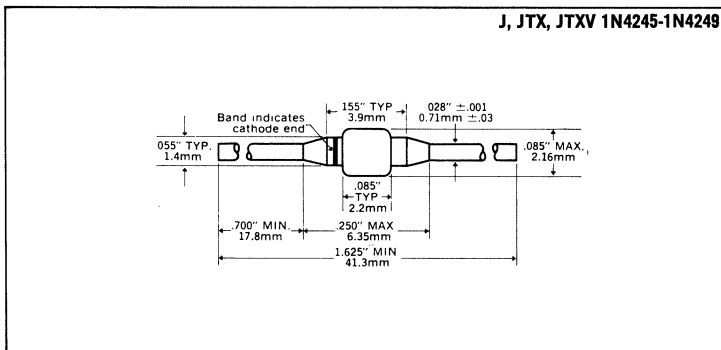
Surge Current 25A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+175^\circ\text{C}$

Thermal Resistance See Lead Temperature Derating Curve

MECHANICAL SPECIFICATIONS

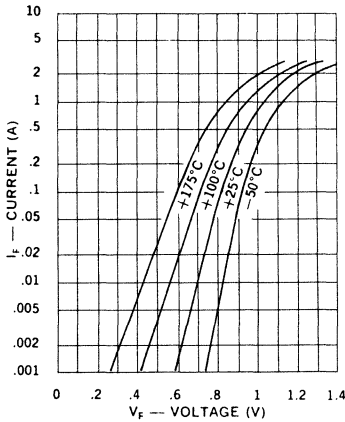


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

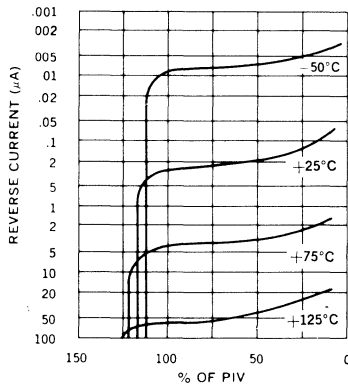
Type	PIV	Minimum Reverse Breakdown Voltage @ 100µA	Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
			Min.	Max.	25°C	150°C	
J, JTX, JTXV 1N4245	200V	240V	0.6V	1.3V(pk) @ 3.0A(pk)	1.0µA	150µA	5.0µs
J, JTX, JTXV 1N4246	400V	480V					
J, JTX, JTXV 1N4247	600V	720V					
J, JTX, JTXV 1N4248	800V	960V					
J, JTX, JTXV 1N4249	1000V	1150V					

*Measured in circuit $I_F = 1/2A$, $I_R = 1.0A$, $I_{REC} = 1/4A$

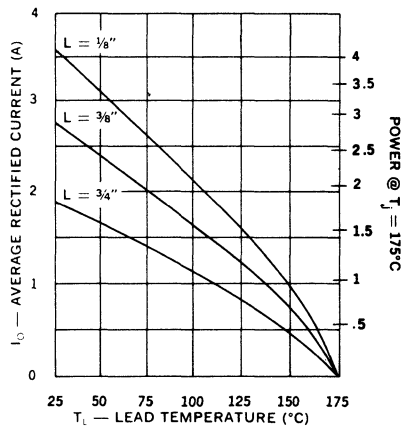
Typical Forward Current vs Forward Voltage



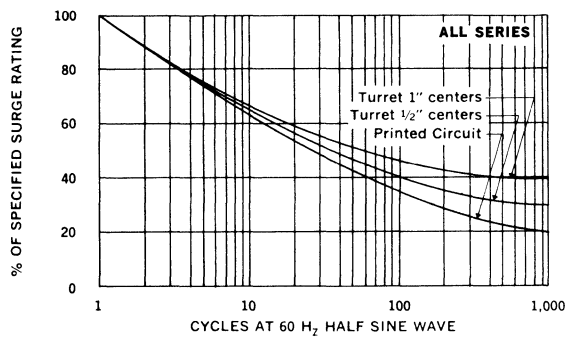
Typical Reverse Current vs PIV



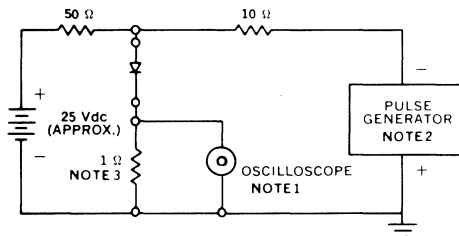
Maximum Current vs Lead Temperature



Allowable Forward Surge vs Number of Cycles



Reverse-Recovery Circuit



NOTES:

- Oscilloscope: Rise time $\leq 3ns$; input impedance = 50Ω.
- Pulse Generator: Rise time $\leq 8ns$; source impedance 10Ω.
- Current viewing resistor, non-inductive, coaxial recommended.



RECTIFIERS

Military Approved, 1 Amp, Fast Recovery

JAN, JANTX, & JANTXV 1N4942
 JAN, JANTX, & JANTXV 1N4944
 JAN, JANTX, & JANTXV 1N4946

FEATURES

- Qualified to MIL-S-19500/359
- Surge Rating: 15A
- PIV: to 600V
- Controlled Avalanche

DESCRIPTION

These fast recovery rectifiers are suitable for use as power devices for many applications. Devices are available as JAN, JANTX or JANTXV.

ABSOLUTE MAXIMUM RATINGS

Maximum Reverse Voltage	Type
200V	JAN, JANTX, & JANTXV 1N4942
400V	JAN, JANTX, & JANTXV 1N4944
600V	JAN, JANTX, & JANTXV 1N4946

Maximum Average D.C. Output Current

@ $T_A = 55^\circ\text{C}$ 1.0A

@ $T_A = 100^\circ\text{C}$ 0.75A

Non-Repetitive Sinusoidal

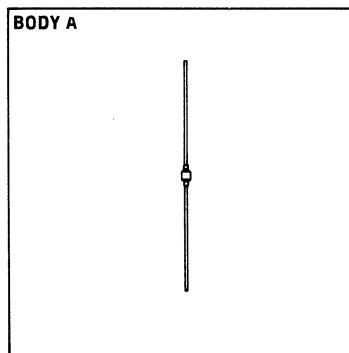
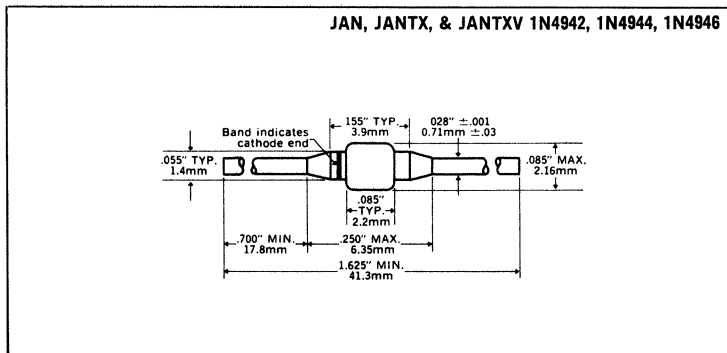
Surge Current (8.3ms) 15A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+175^\circ\text{C}$

Thermal Resistance See Lead Temperature Derating Curve

MECHANICAL SPECIFICATIONS



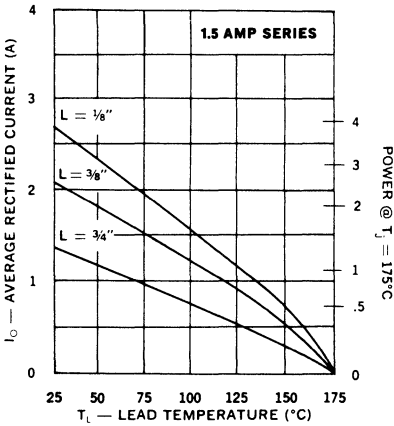
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Minimum Reverse Breakdown Voltage @ 50μA	Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*	Capacitance @ V _R = 12V f = 1MHz
			Min.	Max.	25°C	150°C		
J, JTX, JTXV 1N4942	200V	220V	0.6V @ 1 Adc	1.3Vdc	1.0μA	200μA	150ns	45pf
J, JTX, JTXV 1N4944	400V	440V						
J, JTX, JTXV 1N4946	600V	660V						

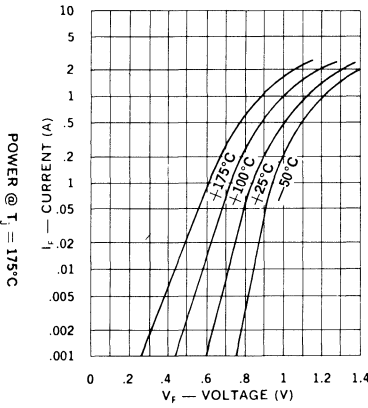
*Measured in circuit I_F = 1/2A, I_R = 1.0A, I_{REC} = 1/4A

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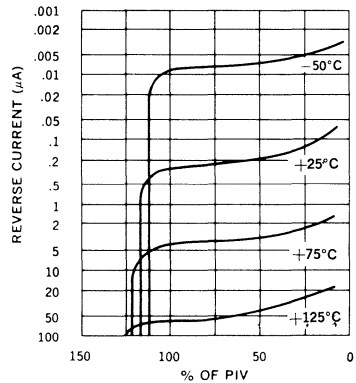
Maximum Current vs Lead Temperature



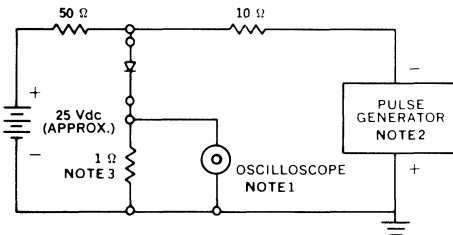
Typical Forward Current vs Forward Voltage



Typical Reverse Current vs PIV

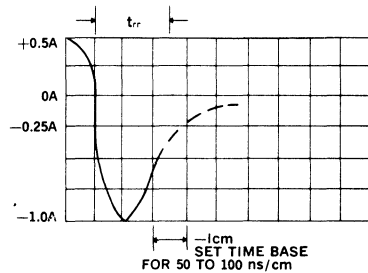


Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
 - Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform.



RECTIFIERS

Military Approved, 3 Amp,
Fast Recovery

1N5186-1N5190
JAN & JANTX

FEATURES

- Continuous Rating: 3A
- Qualified to MIL-S-19500/424
- PIV : to 600V
- Recovery Time: 150ns
- Miniature Size
- Controlled Avalanche

DESCRIPTION

These miniature fast recovery rectifiers permit operation at full power at frequencies as high as 100kHz sine wave. They are qualified to military specification and available as JAN, JANTX or JANTXV.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
100V	JAN & JANTX 1N5186
200V	JAN & JANTX 1N5187
400V	JAN & JANTX 1N5188
600V	JAN & JANTX 1N5190

Maximum Average D.C. Output Current

@ $T_A = 25^\circ\text{C}$ 3.0A

@ $T_A = 150^\circ\text{C}$ 0.7A

Non-Repetitive Sinusoidal

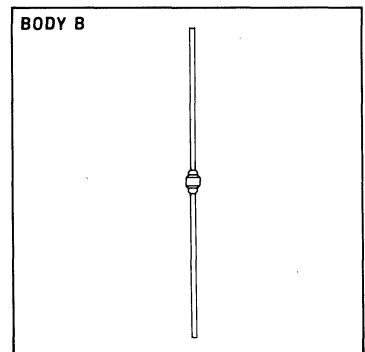
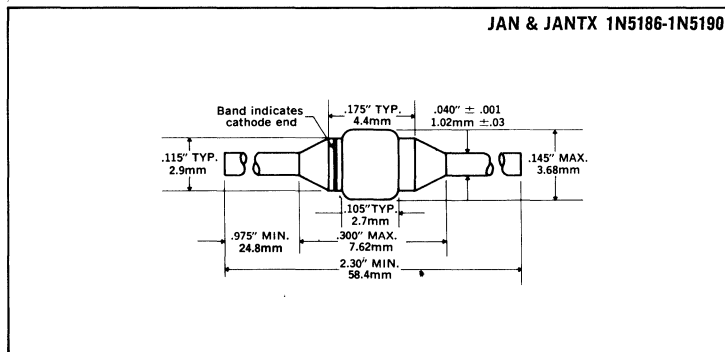
Surge Current (8.3ms) 80A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Thermal Resistance See Lead Temperature Derating Curve

MECHANICAL SPECIFICATIONS

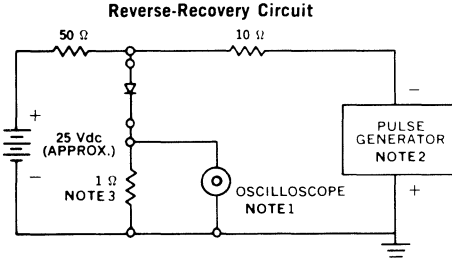
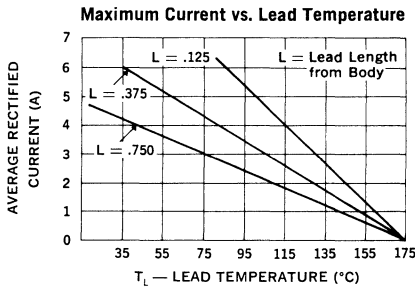


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

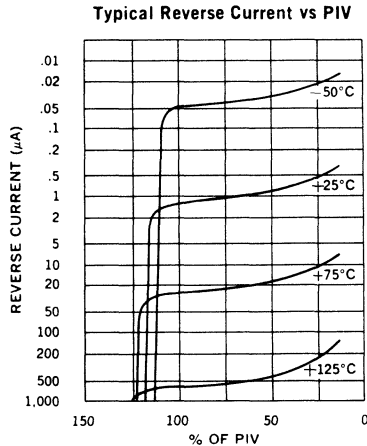
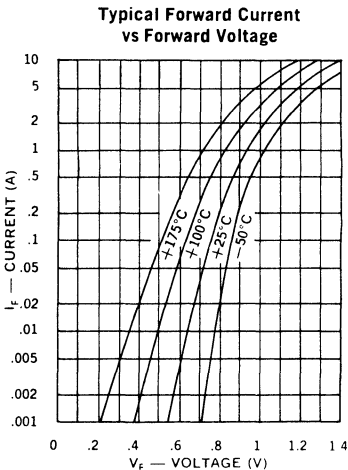
Type	Peak Inverse Voltage	Minimum Reverse Breakdown Voltage @ 100µA	Peak Forward Voltage		Maximum Reverse D.C. Current @ PIV	
			Min.	Max.	25°C	100°C
J, JTX 1N5186	100V	120V	0.9V @ 9A(pk) (8.3ms)	1.5V	2µA	100µA
J, JTX 1N5187	200V	240V				
J, JTX 1N5188	400V	480V				
J, JTX 1N5190	600V	660V				

Type	Reverse Recovery Time*	Capacitance @ V _r = 0V, f = 1MHz	Capacitance @ V _r = 4V, f = 1MHz
J, JTX 1N5186	150ns	300pf	200pf
J, JTX 1N5187	200ns	300pf	170pf
J, JTX 1N5188	250ns	230pf	120pf
J, JTX 1N5190	400ns	180pf	90pf

*Recovery time measured from I_f = 0.5A to I_R = 1.0A, I_{REC} = 0.25A



- NOTES:**
- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
 - Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.



RECTIFIERS

Military Approved, Fast Recovery, 3 Amp

1N5415-1N5420
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/411
- PIV: to 600V
- Controlled Avalanche

DESCRIPTION

This series of devices as designed to meet the need for high speed, power rectifiers in military high-rel power supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
50V	JAN, JANTX, JANTXV 1N5415
100V	JAN, JANTX, JANTXV 1N5416
200V	JAN, JANTX, JANTXV 1N5417
400V	JAN, JANTX, JANTXV 1N5418
500V	JAN, JANTX, JANTXV 1N5419
600V	JAN, JANTX, JANTXV 1N5420

Maximum Average D.C. Output Current

@ $T_A = 55^\circ\text{C}$ 3.0A

@ $T_A = 100^\circ\text{C}$ 2.0A

Non-Repetitive Sinusoidal

Surge Current (8.3ms) 80A

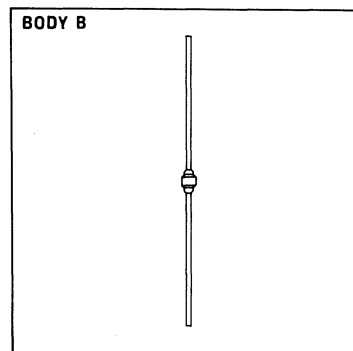
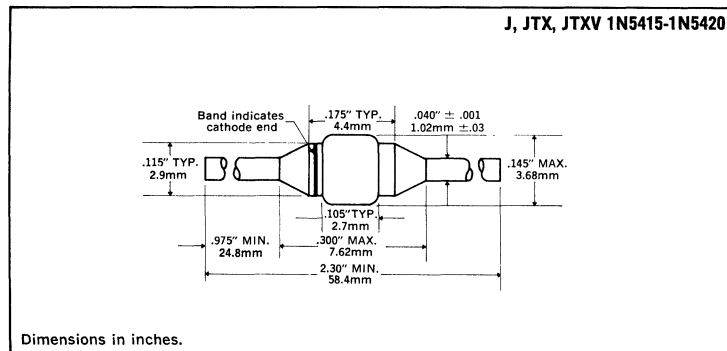
Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Thermal Resistance θ_{JL} @ $L = \frac{3}{8}"$ 20°C/W

See Lead Temperature Derating Curve

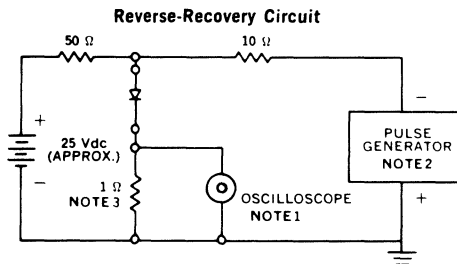
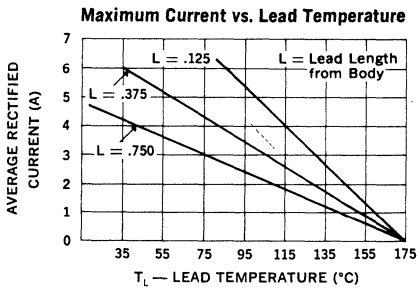
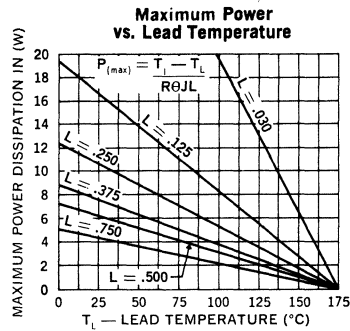
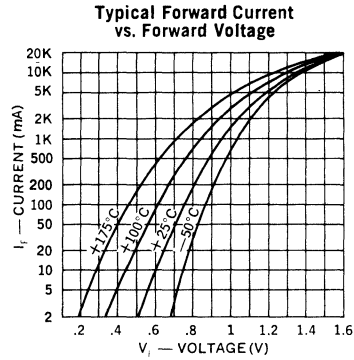
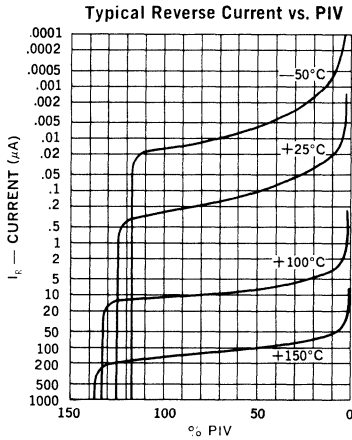
MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Minimum Reverse Breakdown Voltage @ 50μA	Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
			Min.	Max.	25°C	100°C	
J, JTX, JTXV 1N5415	50V	55V	0.6V	1.5V(pk)	1.0μA	20μA	150
J, JTX, JTXV 1N5416	100V	110V					150
J, JTX, JTXV 1N5417	200V	220V					150
J, JTX, JTXV 1N5418	400V	440V					150
J, JTX, JTXV 1N5419	500V	550V					250
J, JTX, JTXV 1N5420	600V	660V					400
							@ 9Adc tp = 300μs

*Measured in circuit $I_F = 0.5 \text{ A}$, $I_R = 1 \text{ A}$, $I_{REC} = 0.25 \text{ A}$.



- NOTES:**
1. Oscilloscope: Rise time $\leq 3\text{ ns}$; input impedance = 50Ω.
 2. Pulse Generator: Rise time $\leq 8\text{ ns}$; source impedance 10Ω.
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

Military Approved, 5 Amp, General Purpose

1N5550-1N5553
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/420A
- Continuous Rating: 5A
- PIV: to 800V
- TX Parts 100% Screened
- Miniature Size
- Controlled Avalanche

DESCRIPTION

This series of military approved rectifiers is useful in many military applications. The 100% screening requirements in the "TX" version combined with the unique Unitrode construction assures the highest degree of reliability.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
200V	JAN, JANTX & JANTXV 1N5550
400V	JAN, JANTX & JANTXV 1N5551
600V	JAN, JANTX & JANTXV 1N5552
800V	JAN, JANTX & JANTXV 1N5553

Maximum Average D.C. Output Current

@ $T_A = 55^\circ\text{C}$ 3.0A

@ $T_L = 55^\circ\text{C}$ 5.0A

Non-Repetitive Sinusoidal

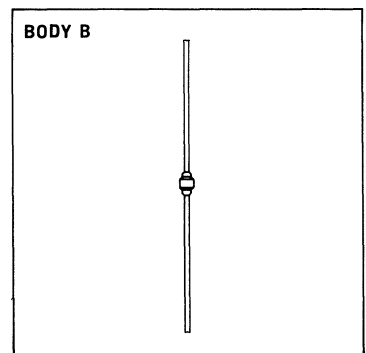
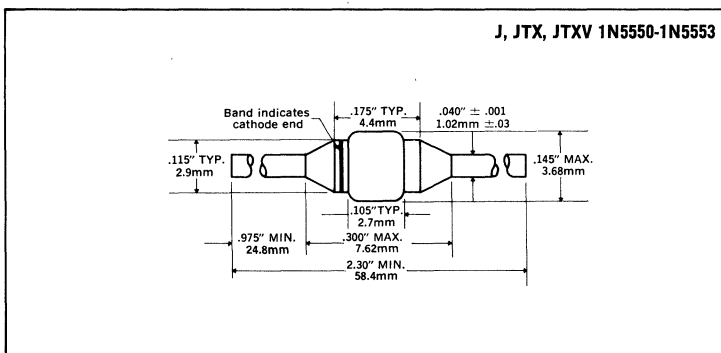
Surge Current (8.3ms) 100A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Thermal Resistance See Lead Temperature Derating Curve

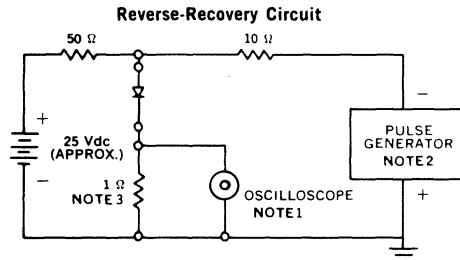
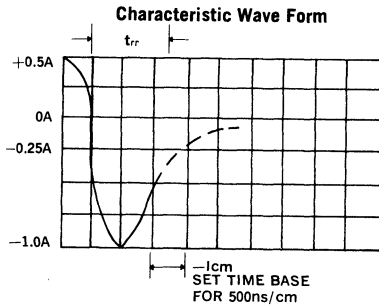
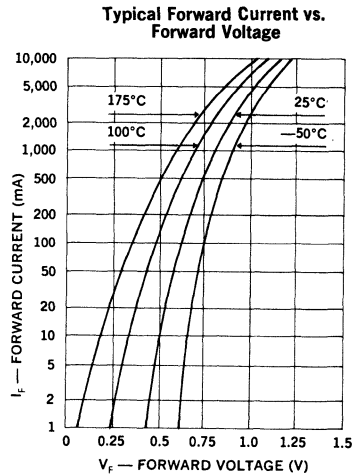
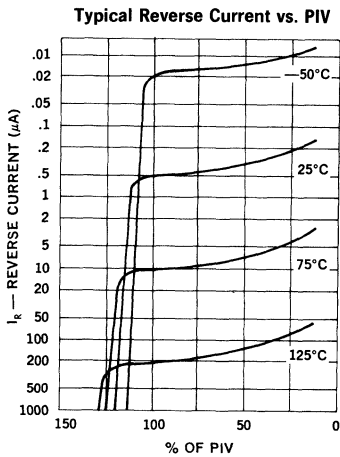
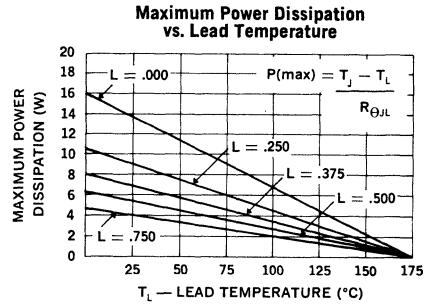
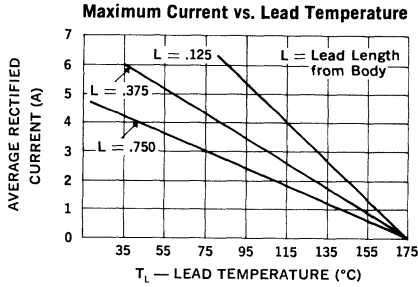
MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Minimum Reverse Breakdown Voltage @ 50µA	Peak Forward Voltage		Maximum Leakage Current @ PIV		Maximum Reverse Recovery Time*
			Min.	Max.	25°C	100°C	
J, JTX, JTXV 1N5550	200V	240V	0.6V @ I _F = 9A(pk) (8.3ms)	1.2V	1.0µA	75µA	2.0µs
J, JTX, JTXV 1N5551	400V	460V					
J, JTX, JTXV 1N5552	600V	660V					
J, JTX, JTXV 1N5553	800V	880V					

*Measured in a test circuit I_F = 0.5A, I_R = 1.0A, I_{REC} = 0.25A



- NOTES:**
- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
 - Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.



RECTIFIERS

Standard Recovery, 1 Amp
Military Approved

1N5614, 1N5616, 1N5618,
1N5620,
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/427
- PIV: to 800V
- Controlled Avalanche

DESCRIPTION

This series of medium power general purpose rectifiers can be used in the most demanding military supplies. Rugged mechanical integrity and tight electrical parameters make them particularly useful.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
200V	JAN, JANTX & JANTXV 1N5614
400V	JAN, JANTX & JANTXV 1N5616
600V	JAN, JANTX & JANTXV 1N5618
800V	JAN, JANTX & JANTXV 1N5620

Maximum Average D.C. Output Current

@ $T_A = 55^\circ\text{C}$ 1.0A

@ $T_A = 100^\circ\text{C}$ 0.75A

Non-Repetitive Sinusoidal

Surge Current (8.3ms) 30A

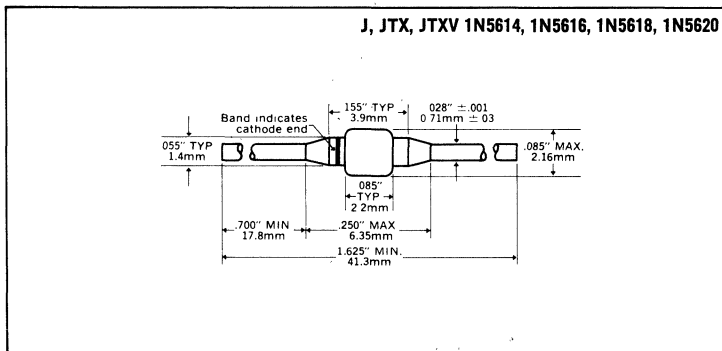
Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

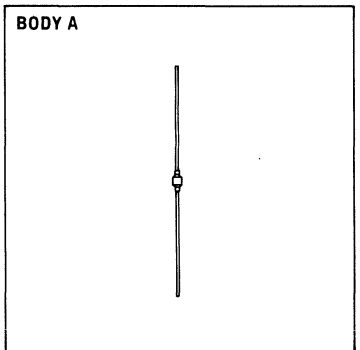
Thermal Resistance θ_{JL} @ $L = 3/8"$ 38°C/W

See Lead Temperature
Derating Curve

MECHANICAL SPECIFICATIONS



BODY A



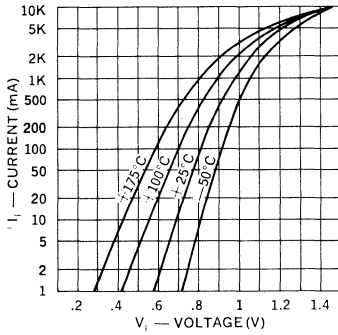
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Minimum Reverse Breakdown Voltage @ 50 μ A	Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
			Min.	Max.	25°C	100°C	
J, JTX, JTXV 1N5614	200V	220V	0.8	1.3V(pk) @ 3.0A tp = 300 μ s	0.5 μ A	25 μ A	2.0 μ s
J, JTX, JTXV 1N5616	400V	440V					
J, JTX, JTXV 1N5618	600V	660V					
J, JTX, JTXV 1N5620	800V	880V					

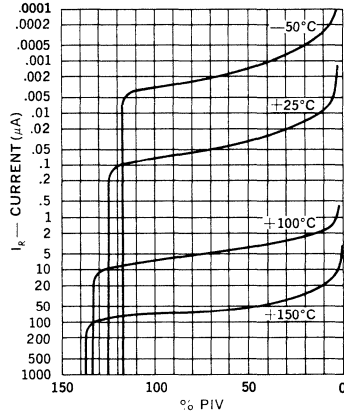
*Measured in Circuit $I_F = \frac{1}{2}A$, $I_R = 1.0A$, $I_{REC} = \frac{1}{4}A$



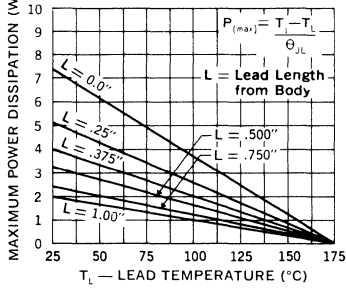
Typical Forward Voltage vs. Forward Current



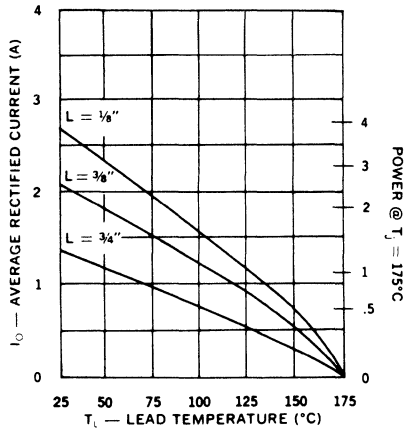
Typical Reverse Current vs. PIV



Maximum Power Dissipation vs. Lead Temperature



Maximum Current vs Lead Temperature



RECTIFIERS

Military Approved, Fast Recovery, 1 Amp

1N5615, 1N5617, 1N5619
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/429
- PIV: to 600V
- Controlled Avalanche

DESCRIPTION

This series of military approved rectifiers is useful in many military applications where fast recovery and medium power are required. The 100% screening requirements in the "TX" version combined with the unique Unitrode construction assures the highest degree of reliability.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
200V	JAN, JANTX, JANTXV 1N5615
400V	JAN, JANTX, JANTXV 1N5617
600V	JAN, JANTX, JANTXV 1N5619

Maximum Average D.C. Output Current

@ $T_A = 55^\circ\text{C}$ 1.0A
 @ $T_A = 100^\circ\text{C}$ 0.75A

Non-Repetitive Sinusoidal

Surge Current (8.3ms) 25A

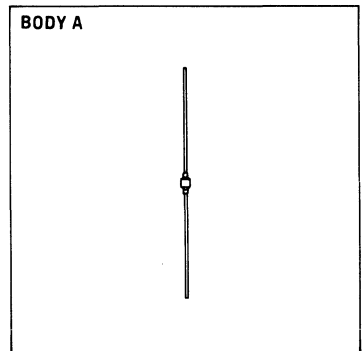
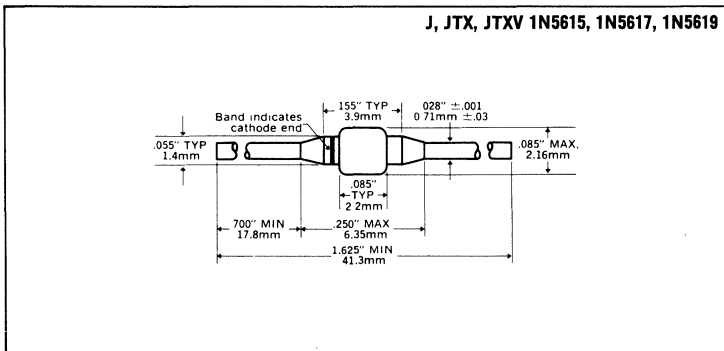
Operating Temperature Range -65°C to $+175^\circ\text{C}$

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Thermal Resistance θ_{JL} 38°C/W

See Lead Temperature
Derating Curve

MECHANICAL SPECIFICATIONS

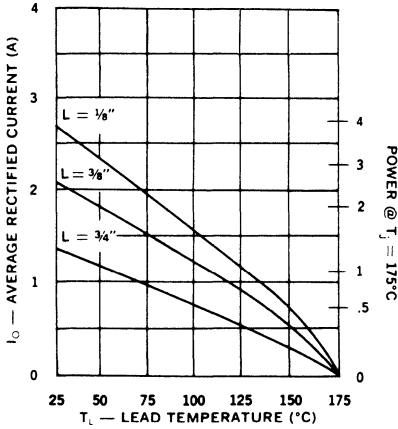


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

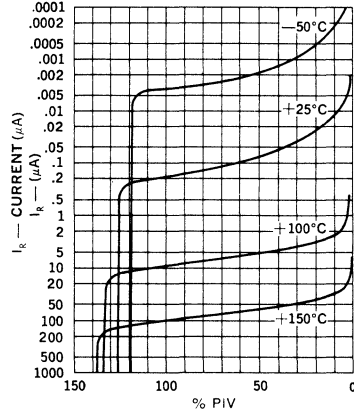
Type	PIV	Minimum Reverse Breakdown Voltage @ 50μA	Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*	Capacitance @ V _r = 12V f = 1MHz
			Min.	Max.	25°C	100°C		
J, JTX, JTXV 1N5615	200V	220V	0.8V	1.6V (pk)	0.5μA	25μA	150ns	45pf
J, JTX, JTXV 1N5617	400V	440V	@ 3.0 Adc tp = 300μs		0.5μA	25μA	150ns	35pf
J, JTX, JTXV 1N5619	600V	660V					250ns	25pf

*Measured in Circuit I_f = 1/2A, I_r = 1A, I_{REC} = 1/4A

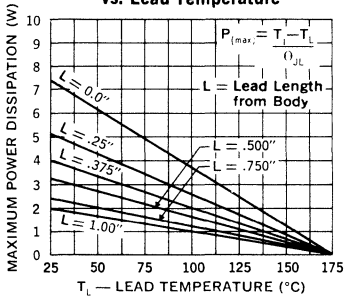
Maximum Current vs Lead Temperature



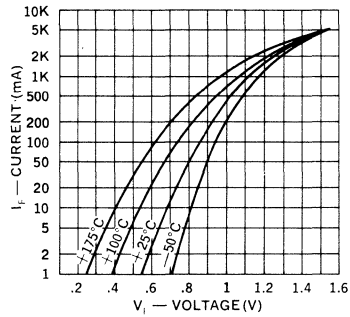
Typical Reverse Current vs. PIV



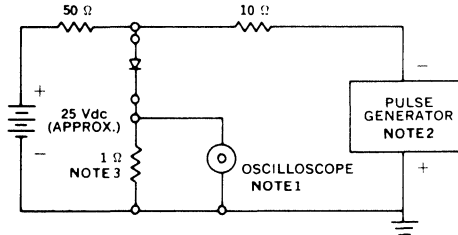
Maximum Power vs. Lead Temperature



Typical Forward Voltage vs. Forward Current



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, ESP, 2.5 Amp to 20 Amp

1N5802-1N5806
1N5807-1N5811
1N5812-1N5816

FEATURES

- Exceptional Efficiency
- Low Forward Voltage
- Extremely Fast Reverse Recovery Time
- Extremely Fast Forward Recovery Time
- High Surge
- Small Size
- Rugged, High Current Termination
- Radiation Tolerant

DESCRIPTION

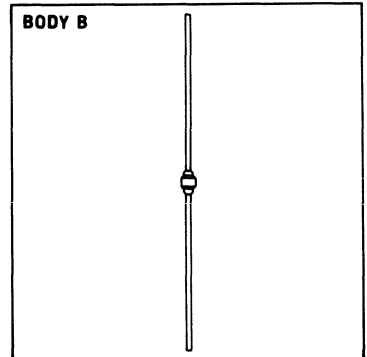
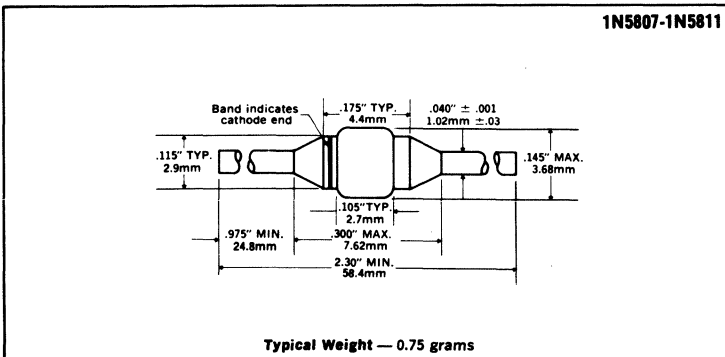
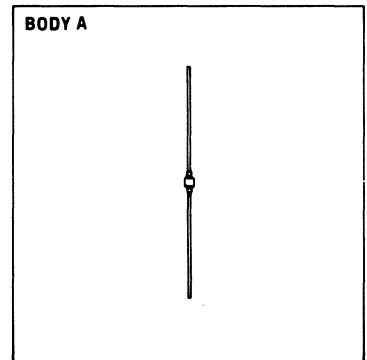
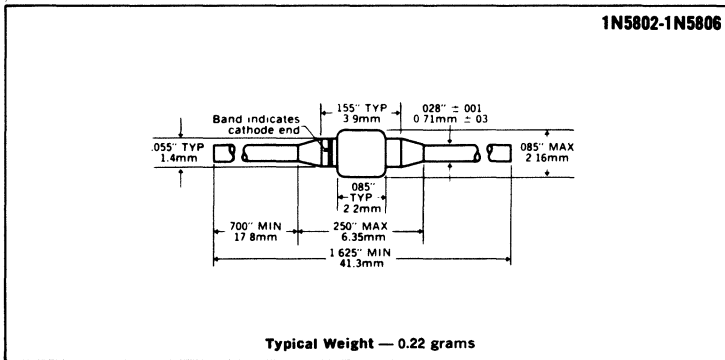
This series of High Efficiency Power Rectifiers allows circuit designers to design high current, high frequency supplies to 500 kHz with very low diode losses. The high forward surge capability makes these devices useful in protective circuits.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	2.5 Amp Series	6 Amp Series	20 Amp Series
50V	1N5802	1N5807	1N5812
75V	1N5803	1N5808	1N5813
100V	1N5804	1N5809	1N5814
125V	1N5805	1N5810	1N5815
150V	1N5806	1N5811	1N5816

Maximum Average D.C. Output Current	2.5 AMP SERIES	6.0 AMP SERIES	20 AMP SERIES
@ $T_L = 75^\circ\text{C}$, $L = \frac{3}{8}"$	2.5A	6.0A	—
@ $T_C = 100^\circ\text{C}$	—	—	20.0A
Non-Repetitive Sinusoidal			
Surge Current (8.3ms)	35A	125A	250A
Operating and Storage Temperature Range	-65°C to +175°C		
Thermal Resistance 2.5A and 6A Series	See Lead Temperature Derating Curve		
20A Series	3.0°C/W		

MECHANICAL SPECIFICATIONS

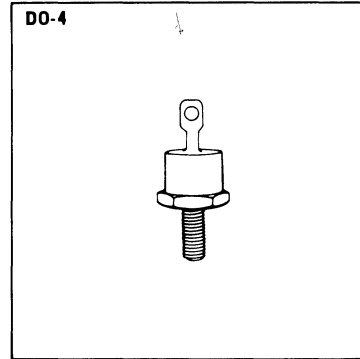


MECHANICAL SPECIFICATIONS

1N5812-1N5816

Part Identification: Type number printed on metal case.
Polarity: Cathode to stud end
Max. Weight: 7.0 Grams
Installation Precautions: Maximum unlubricated stud torque: 10 inch pounds
Thermal Resistance: 3.0°C/W

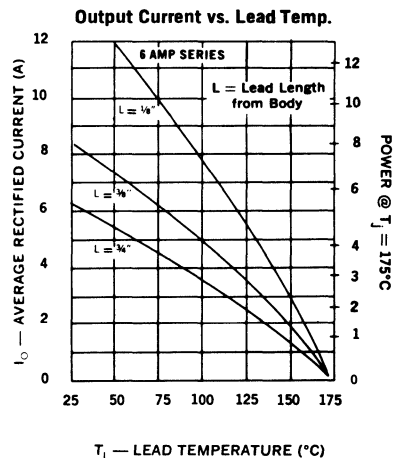
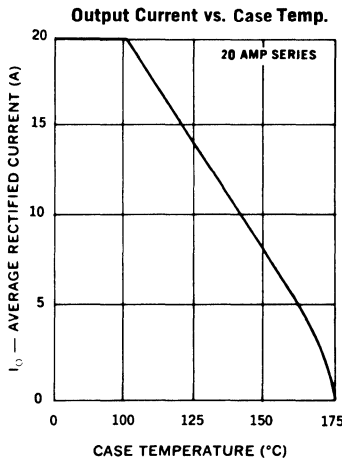
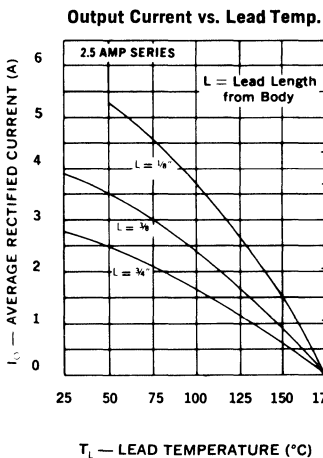
Dimensions in inches.



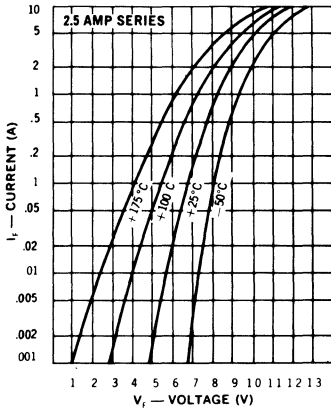
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Maximum Forward Voltage Drop*	Leakage Current @ PIV		Maximum Reverse Recovery Time I_F, I_R, I_{REC}	Typical Forward Recovery Time @ 1A Recover to 1V	Typical Forward Recovery Voltage @ 1A $t_r = 8ns$	Typical Junction Capacitance @ -10V
			25°C	100°C				
1N5802	50V	.875 @ 1A	1 μ A	50 μ A	25ns, 0.5A-0.5A-0.05A	15ns	1.5V	15pf
1N5803	75V							
1N5804	100V							
1N5805	125V							
1N5806	150V							
1N5807	50V	.875 @ 4A	5 μ A	150 μ A	30ns, 1.0-1.0-0.1A	15ns	1.5V	45pf
1N5808	75V							
1N5809	100V							
1N5810	125V							
1N5811	150V							
1N5812	50V	.900 @ 10A	10 μ A	750 μ A	35ns, 1.0-1.0-0.1A	15ns	1.5V	200pf
1N5813	75V							
1N5814	100V							
1N5815	125V							
1N5816	150V							

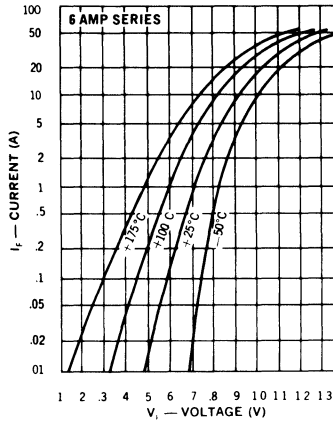
*Pulse width = 250ms



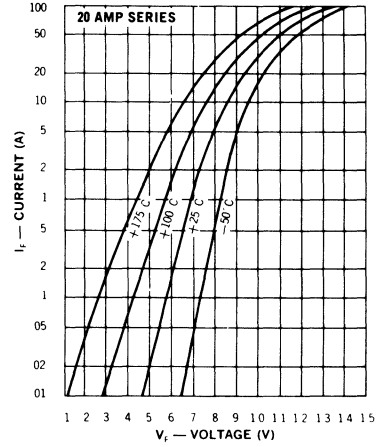
Typical Forward Current vs. Forward Voltage



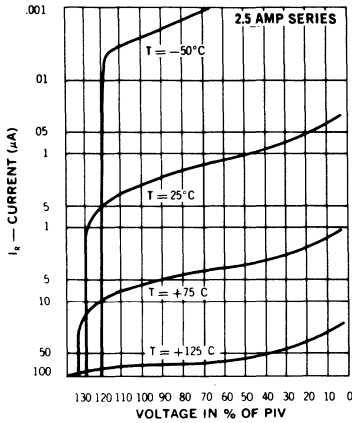
Typical Forward Current vs. Forward Voltage



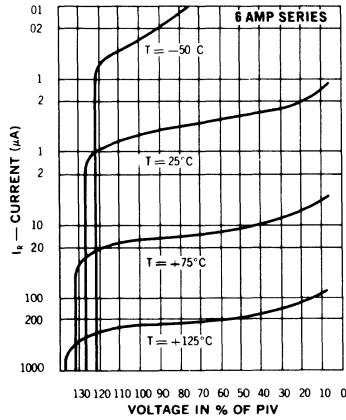
Typical Forward Current vs. Forward Voltage



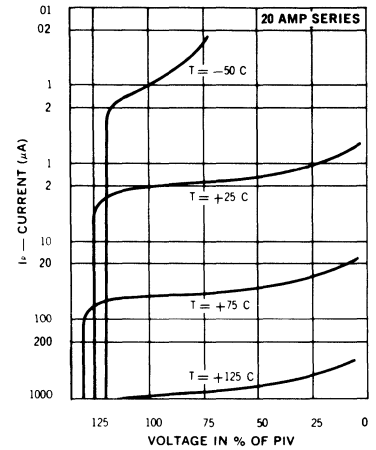
Typical Reverse Current vs. Voltage



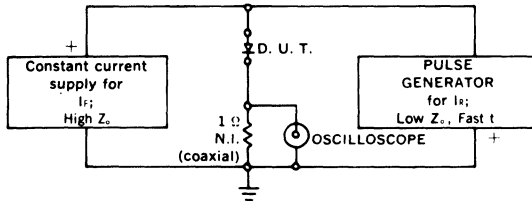
Typical Reverse Current vs. Voltage



Typical Reverse Current vs. Voltage

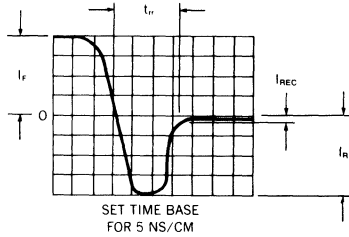


Reverse-Recovery Time Circuit



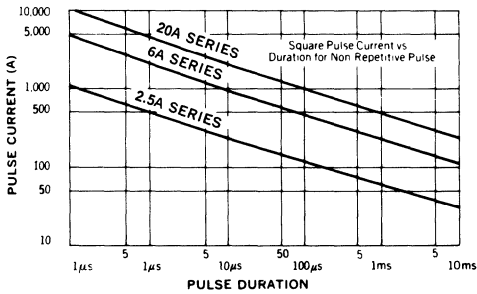
- NOTES:**
1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω .
 2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω .

Characteristic Waveform

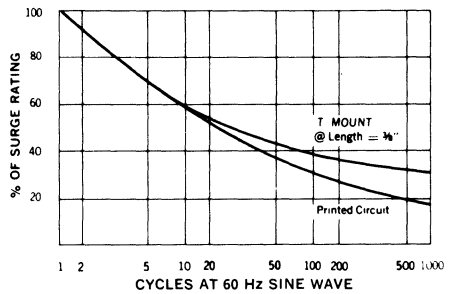


6

Forward Pulse Current vs. Duration



Multiple Surge Current vs. Duration



RECTIFIERS

Military Approved, High Efficiency,
2.5 Amp and 6.0 Amp

1N5802, 1N5804, 1N5806,
1N5807, 1N5809, 1N5811
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/477
- PIV: to 150V
- Low Forward Voltage

DESCRIPTION

This series of high efficiency power rectifiers are particularly applicable to switching regulator power supplies where extremely fast switching and low forward losses are most important.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	2.5A Series	6.A Series
50V	JAN, JANTX & JANTXV 1N5802	JAN, JANTX & JANTXV 1N5807
100V	JAN, JANTX & JANTXV 1N5804	JAN, JANTX & JANTXV 1N5809
150V	JAN, JANTX & JANTXV 1N5806	JAN, JANTX & JANTXV 1N5811

Maximum Average D.C. Output Current

@ $T_L = 75^\circ\text{C}$, $L = \frac{3}{8}"$

@ $T_A = 55^\circ\text{C}$

2.5A SERIES

2.5A

1.0A

6A SERIES

6.0A

3.0A

Non-Repetitive Sinusoidal

Surge Current (8.3ms)

35A

125A

Operating Temperature Range

-65°C to $+175^\circ\text{C}$

Storage Temperature Range

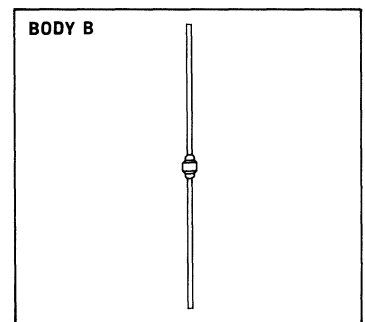
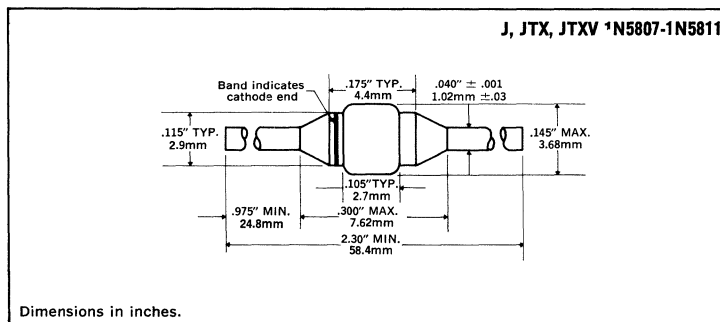
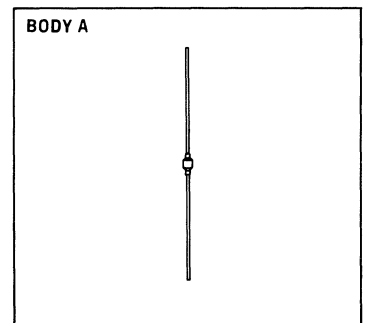
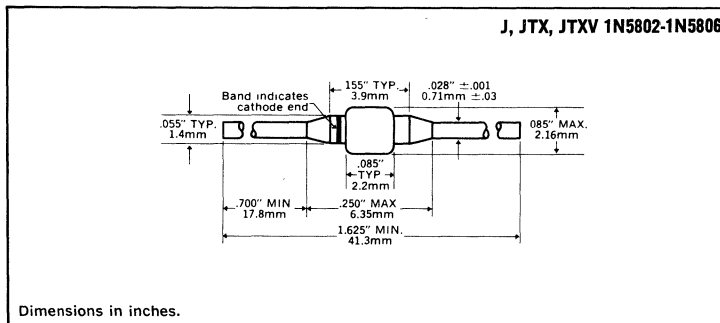
-65°C to $+200^\circ\text{C}$

Thermal Resistance, θ_{JL} @ $L = \frac{3}{4}"$

59°C/W 35.5°C/W

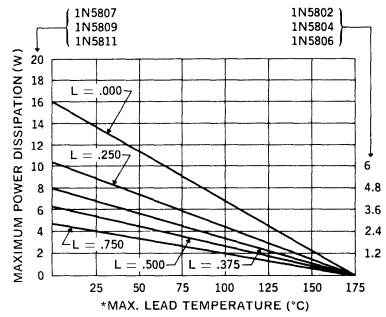
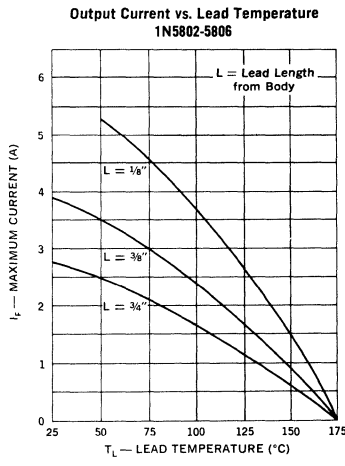
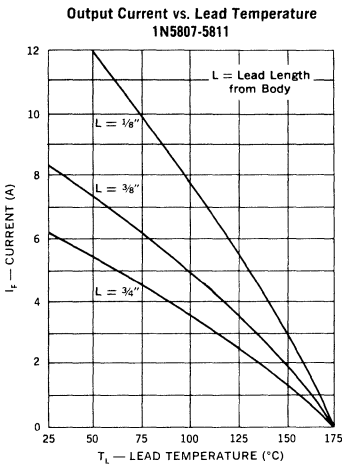
See lead temperature derating curve

MECHANICAL SPECIFICATIONS



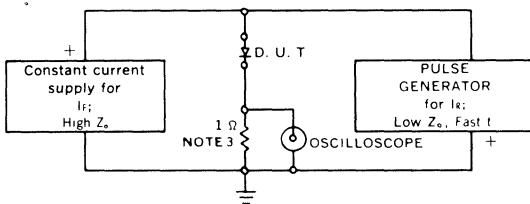
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Minimum Breakdown Voltage @ 100µA	Forward Voltage		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time
			@ 25°C	@ 100°C	25°C	100°C	
J, JTX, JTXV 1N5807	50V	60V	.875V Max. @ 4A (pk)	.8V Max. @ 4A (pk)	5µA	150µA	30ns $I_F = I_R = 1.0A$ $I_{REC} = 0.1A$ $di/dt = 100A/\mu s \text{ min.}$
J, JTX, JTXV 1N5809	100V	110V	.925V Max. @ 6A (pk)				
J, JTX, JTXV 1N5811	150V	160V					
J, JTX, JTXV 1N5802	50V	60V	.875V Max. @ 1A (pk)	.8V Max. @ 1A (pk)	1µA	50µA	25ns $I_F = I_R = 0.5A$ $I_{REC} = 0.05A$ $di/dt = 65A/\mu s \text{ min.}$
J, JTX, JTXV 1N5804	100V	110V	.975V Max. @ 2.5A (pk)				
J, JTX, JTXV 1N5806	150V	160V					

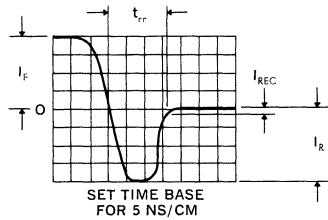


*Maximum lead temperature in °C (T_l) at point "L" from body. (For maximum operating junction temperature of 175°C with equal two-lead conditions.)

Reverse-Recovery Circuit



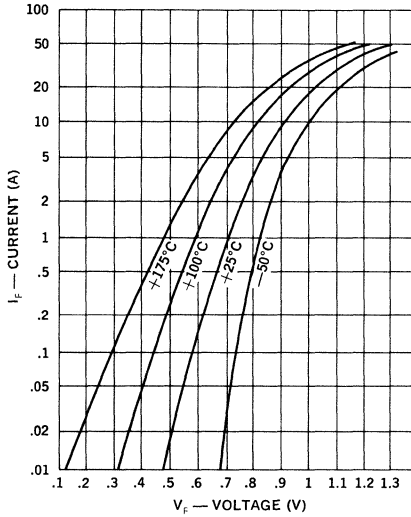
Characteristic Waveform



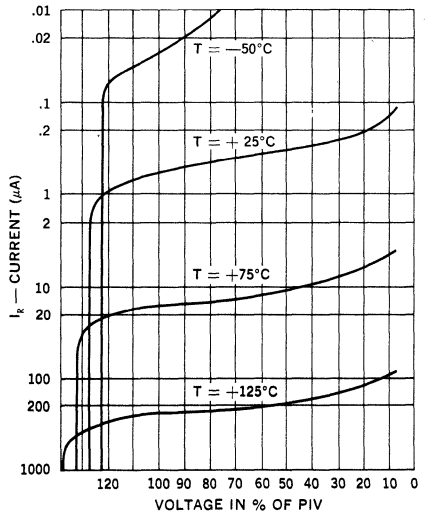
NOTES:

- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
- Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
- Current viewing resistor, non-inductive, coaxial recommended.

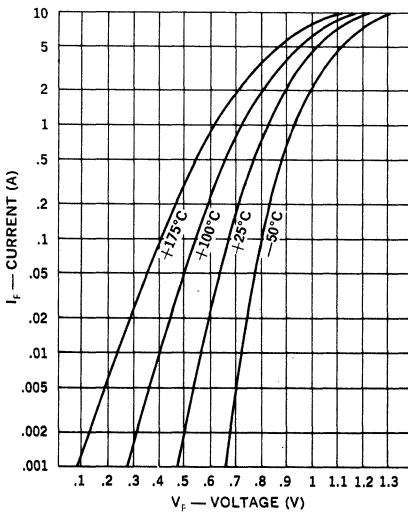
**Typical Forward Current vs. Forward Voltage
JAN & JANTX 1N5807-5811**



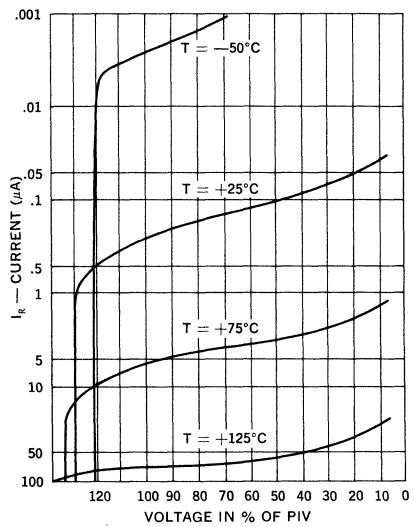
**Typical Reverse Current vs. Voltage
JAN & JANTX 1N5807-5811**



**Typical Forward Current vs. Forward Voltage
JAN & JANTX 1N5802-5806**



**Typical Reverse Current vs. Voltage
JAN & JANTX 1N5802-5806**



RECTIFIERS

Military Approved

High Efficiency, 20 Amp

1N5812, 1N5814, 1N5816
JAN, JANTX & JANTXV

FEATURES

- Qualified to MIL-S-19500/478
- Exceptional Efficiency
- Mechanically Rugged
- Low Thermal Resistance
- JAN, JANTX and JANTXV Available

DESCRIPTION

This series is suited for use as a power rectifier in switching regulator and high frequency inverter/converter and other appropriate equipment circuits where low voltage drop and fast recovery times are important.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
50V	JAN, JANTX, JANTXV 1N5812
100V	JAN, JANTX, JANTXV, 1N5814
150V	JAN, JANTX, JANTXV 1N5816

Maximum Average D.C. Output Current

@ $T_c = 100^\circ\text{C}$ 20A

@ $T_A = 55^\circ\text{C}$ 5A

Non-Repetitive Sinusoidal

Surge Current @ 8.3mSec 400A

Thermal Resistance, Junction to Case 1.5°C/W

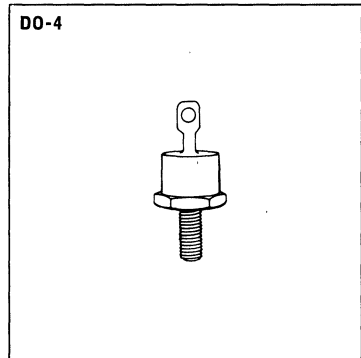
Operating Junction Temperature -65°C to $+175^\circ\text{C}$

Storage Ambient Temperature -65°C to $+200^\circ\text{C}$

MECHANICAL SPECIFICATIONS

J, JTX, JTXV 1N5812, 1N5814, 1N5816

	ins.	mm
A	.078 MAX.	1.98 MAX.
B	$.437 \pm .015$	11.10 ± 0.38
C	405 MAX.	10.29 MAX.
D	800 MAX.	20.32 MAX.
E	$.430 \pm .010$	10.92 ± 0.25
F	250 MAX.	6.35 MAX.
G	424 MAX.	10.77 MAX.
H	.066 MIN. DIA	1.68 MIN. DIA.



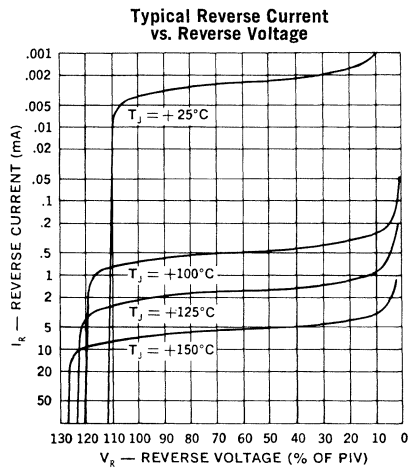
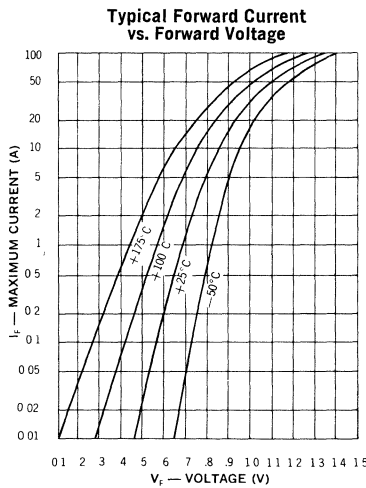
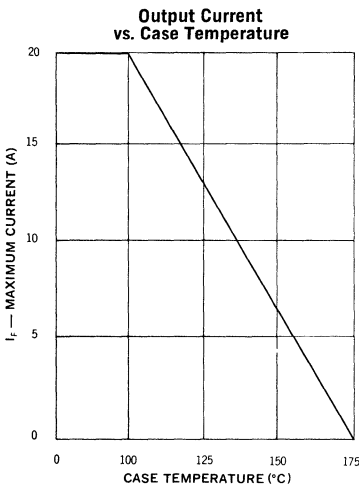
Notes:

1. Polarity is cathode-to-stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 15 inch pounds.
4. Angular orientation of terminal is undefined.

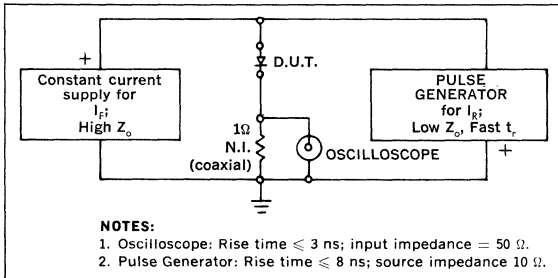
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Minimum Reverse Breakdown Voltage @ 100 μ A	Peak Forward Voltage		Maximum Leakage Current @ PIV	
			@ 10Apk	@ 20Apk	25°C	100°C
J, JTX, JTXV 1N5812	50V	60V				
J, JTX, JTXV 1N5814	100V	110V	.86V MAX.	.95V MAX.	10 μ A	750 μ A
J, JTX, JTXV 1N5816	150V	160V				

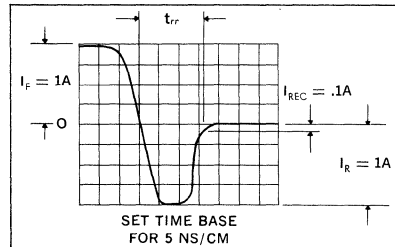
Maximum Reverse Recovery Time @ I_F, I_R, I_{REC}	Maximum Forward Recovery Time @ 1A Recovery to 1V	Maximum Forward Recovery Voltage @ 1A tr = 8nsec	Maximum Junction Capacitance @ -10V
35nsec 1.0A -1.0A -0.1A	15nsec	2.2V	300pf



Reverse-Recovery Time Test Circuit



Characteristic Waveform



POWER SCHOTTKY RECTIFIERS

1A, Up to 40V

1N5817
1N5818
1N5819

FEATURES

- Very Low Forward Voltage
(0.45V max @ 1A for the 1N5817)
- Low Stored Charge, Majority Carrier Conduction
- Economical, Convenient Plastic Package
- Small Size

DESCRIPTION

The 1N5817, 1N5818 and 1N5819 series of Schottky barrier rectifiers are ideally suited for use as rectifiers in low voltage, high frequency inverters, as free wheeling diodes and as polarity protection diodes.

ABSOLUTE MAXIMUM RATINGS*

	1N5817	1N5818	1N5819
Peak Repetitive Reverse Voltage, V_{RRM}	20V	30V	40V
Working Peak Reverse Voltage, V_{RWM}	20V	30V	40V
DC Blocking Voltage, V_R	20V	30V	40V
Non-Repetitive Peak Reverse Voltage, V_{RSM}	24V	36V	48V
RMS Reverse Voltage, $V_{R(RMS)}$	14V	21V	28V
Average Rectified Forward Current, I_o ($V_{R(EQUIV)} \leq 0.2 V_R(DC)$, $T_L = 90^\circ C$, $R_{\theta JA} = 80^\circ C/W$, PC Board Mounting, see Note 1, $T_A = 55^\circ C$)		1.0A	
Ambient Temperature, T_A	85°C	80°C	75°C
Rated $V_R(DC)$, $P_{F(AV)} = 0$, $R_{\theta JA} = 80^\circ C/W$			
Non-Repetitive Peak Surge Current, I_{FSM} (Surge applied at rated load conditions, half-wave, single phase 60Hz, $T_L = 70^\circ C$)		25A (for one cycle)	
Operating and Storage Junction Temperature Range, (Reverse Voltage Applied)		-65°C to +125°C	
Peak Operating Junction Temperature, $T_{J(PK)}$ (Forward Current Applied)		150°C	
Thermal Resistance, Junction to Ambient (Note 1), $R_{\theta JA}$		80°C/W Max.	

* JEDEC registered values.

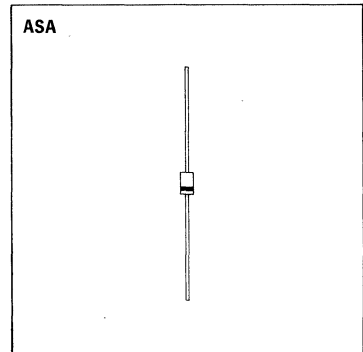
Note 1: Lead Temperature reference is cathode lead $\frac{1}{32}$ " from case.

MECHANICAL SPECIFICATIONS

1N5817 1N5818 1N5819

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.260	4.06	6.60
B	0.110	0.120	2.79	3.05
D	0.030	0.034	0.76	0.86
K	1.0	—	25.4	—

Soldering 220°C, $\frac{1}{16}$ " from case for ten seconds



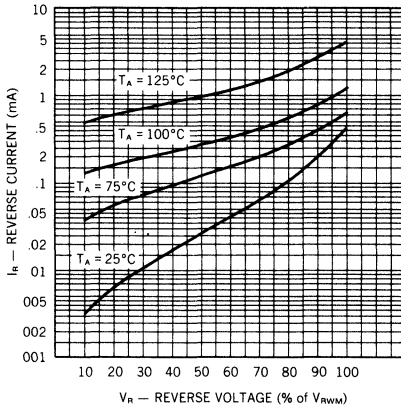
6

ELECTRICAL CHARACTERISTICS (T_L = 25°C unless noted)*

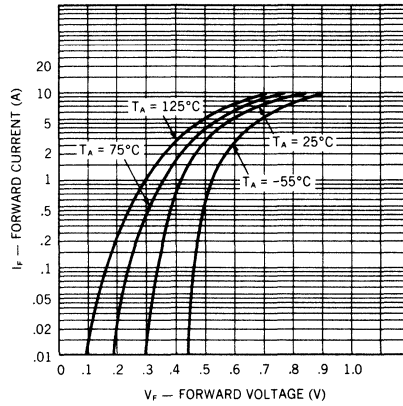
CHARACTERISTIC	SYMBOL	1N5817	1N5818	1N5819	UNITS	CONDITIONS
Maximum Instantaneous Forward Voltage (Note 2)	V _F	0.450	0.550	0.600	V	i _F = 1.0A
		0.750	0.875	0.900	V	i _F = 3.0A
Maximum Instantaneous Reverse Current @ Rated DC Voltage (Note 2)	i _R	1.0	1.0	1.0	mA	T _L = 25°C
		10	10	10	mA	T _L = 100°C

* JEDEC registered values.
 Note 2: Pulse width = 300μs; duty cycle = 2%.

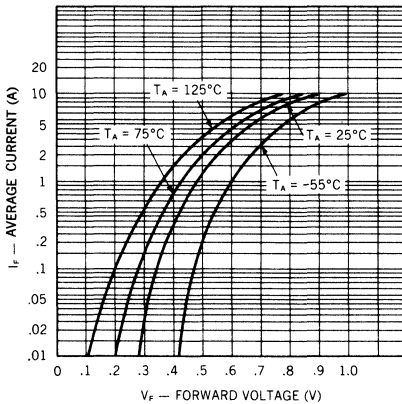
Typical Reverse Current vs Reverse Voltage



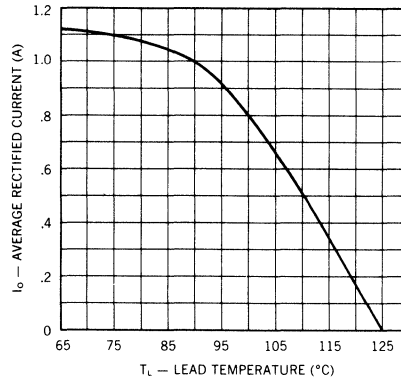
Typical Forward Voltage vs Forward Current (1N5817)



Typical Forward Voltage vs Forward Current (1N5818, 1N5819)



Output Current vs Lead Temperature (L = 3/8")



POWER SCHOTTKY RECTIFIERS

3A, Up to 40V

1N5820
1N5821
1N5822

FEATURES

- Very Low Forward Voltage
(0.475V max @ 3A for the 1N5820)
- Low Stored Charge, Majority Carrier Conduction
- Economical, Convenient Plastic Package
- Small Size

DESCRIPTION

The 1N5820, 1N5821 and 1N5822 series of Schottky barrier rectifiers are ideally suited for use as rectifiers in low voltage, high frequency inverters, as free wheeling diodes and as polarity protection diodes.

ABSOLUTE MAXIMUM RATINGS*

	1N5820	1N5821	1N5822
Peak Repetitive Reverse Voltage, V_{RRM}	20V	30V	40V
Working Peak Reverse Voltage, V_{RWM}	20V	30V	40V
DC Blocking Voltage, V_R	20V	30V	40V
Non-Repetitive Peak Reverse Voltage, V_{RSM}	24V	36V	48V
RMS Reverse Voltage, $V_{R(RMS)}$	14V	21V	28V
Average Rectified Forward Current, I_o ($V_{R(EQUIV)} \leq 0.2 V_R(DC)$, $T_L = 95^\circ C$, $R_{\theta JA} = 28^\circ C/W$, PC Board Mounting, see Note 1, $T_A = 55^\circ C$)		3.0A	
Ambient Temperature, T_A	$90^\circ C$	$85^\circ C$	$80^\circ C$
(Rated $V_R(DC)$, $P_{F(AV)} = 0$, $R_{\theta JA} = 28^\circ C/W$)			
Non-Repetitive Peak Surge Current, I_{FSM} (Surge applied at rated load conditions, half-wave, single phase 60Hz, $T_L = 75^\circ C$)		80A (for one cycle)	
Operating and Storage Junction Temperature Range, (Reverse Voltage Applied)		$-65^\circ C$ to $+125^\circ C$	
Peak Operating Junction Temperature, $T_{J(pk)}$ (Forward Current Applied)		$150^\circ C$	
Thermal Resistance, Junction to Ambient (Note 1), $R_{\theta JA}$		$28^\circ C/W$ Max.	

* JEDEC registered values.

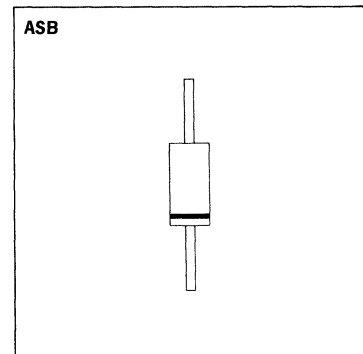
Note 1: Lead Temperature reference is cathode lead $\frac{1}{32}$ " from case.

MECHANICAL SPECIFICATIONS

1N5820 1N5821 1N5822

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.260	4.06	6.60
B	0.110	0.120	2.79	3.05
D	0.030	0.034	0.76	0.86
K	1.0	—	25.4	—

Soldering: $220^\circ C$, $\frac{1}{16}$ " from case for ten seconds



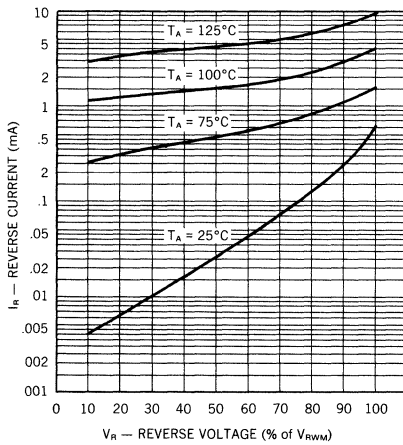
6

ELECTRICAL CHARACTERISTICS ($T_L = 25^\circ\text{C}$ unless noted)*

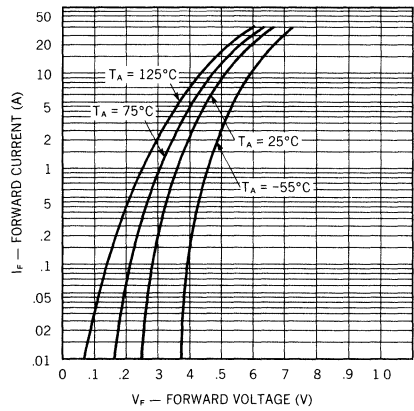
CHARACTERISTIC	SYMBOL	1N5820	1N5821	1N5822	UNITS	CONDITIONS
Maximum Instantaneous Forward Voltage (Note 2)	V_F	0.475	0.500	0.525	V	$i_F = 3.0\text{A}$
		0.850	0.900	0.950	V	$i_F = 9.4\text{A}$
Maximum Instantaneous Reverse Current @ Rated DC Voltage (Note 2)	i_R	2.0	2.0	2.0	mA	$T_L = 25^\circ\text{C}$
		2.0	2.0	2.0	mA	$T_L = 100^\circ\text{C}$

* JEDEC registered values.
 Note 2: Pulse width = 300 μs ; duty cycle = 2%

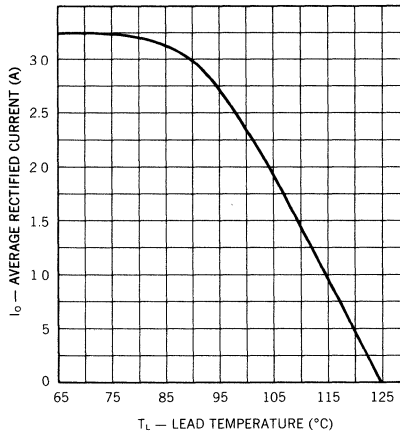
Typical Reverse Current vs Reverse Voltage



Typical Forward Voltage vs Forward Current



Output Current vs Case Temperature ($L = 3/8''$)



POWER SCHOTTKY RECTIFIERS

1N6097
1N6098

50 Amp, 30 and 40 Volts

FEATURES

- Very Low Forward Voltage
- Low Recovered Charge
- Rugged Package Design (DO-5)
- Low Thermal Resistance
- High Surge Current
- Reverse Energy Tested (2A pk)

DESCRIPTION

Unitrode's series of Schottky barrier power rectifiers is ideally suited for output rectifiers and catch diodes in low voltage power supplies. The Unitrode high conductivity design, using a heavy copper top post and 4 point crimp, ensures cool thermal operation and low dynamic impedance. Rugged design absorbs stress that can damage glass-to-metal seal during installation and use.

ABSOLUTE MAXIMUM RATINGS

	1N6097	1N6098
Working Peak Reverse Voltage, V_{RWM}	30V	40V
DC Blocking Voltage, V_R	30V	40V
Repetitive Peak Reverse Voltage, V_{RRM}	30V	40V
Non-repetitive Peak Reverse Voltage, V_{RSM}	36V	48V
Average Rectified Forward Current, I_O	50A ($T_C = 70^\circ C$) 20A ($T_C = 105^\circ C$)	
Non-repetitive Peak Surge Current (8.3 ms), I_{FSM}	800A	
Storage Temperature Range, T_{stg}	-65 to +125°C	
Peak Operating Junction Temperature, $T_{I(pk)}$	+150°C	
Thermal Resistance Junction to Case, $R_{\theta JC}$	1°C/WMax.	

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ C$)

Characteristic	Symbol	Both Types	Units	Conditions
Maximum Instantaneous Reverse Current	I_{RRM}	250	mA	$V_{RWM} = \text{Rated}$, $T_C = 125^\circ C$ Pulse Width = 300 μ s, Duty Cycle ≤ 2 percent
Maximum Reverse Current	I_R	250	mA	$V_R = \text{Rated}$, $T_C = 115^\circ C$
Maximum Instantaneous Forward Voltage	V_{FM}	0.86	V	$I_O = 50A^*$ $T_C = 70^\circ C$
	V_{FM}	0.60	V	$I_F = 10A$ Pulse Width 300 μ s Duty Cycle ≤ 2 percent
Capacitance	C_i	7000	pF	$V_R = 1.0V$

* $I_{FM} = 157A$

MECHANICAL SPECIFICATIONS

1N6097, 1N6098

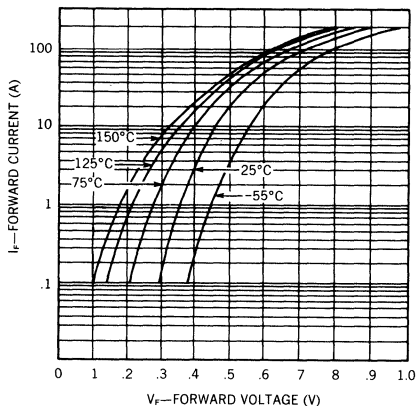
	ins.	mm
A	225 ± .005	5.72 ± 0.13
B	060 MIN	1.52 MIN
C	156 ± .020	3.96 ± 0.51
D	156 MIN FLAT	3.96 MIN FLAT
E	66.7 DIA. MAX	16.94 DIA. MAX
F	090 MAX	2.29 MAX
G	67.7 ± .010	17.20 ± 0.25
H	37.5 MAX	9.53 MAX
J	140 MIN DIA	3.56 MIN DIA
K	1.000 MAX	25.40 MAX
L	450 MAX	11.43 MAX
M	438 ± .015	11.13 ± 0.38
N	078 MAX	1.98 MAX

DO-5

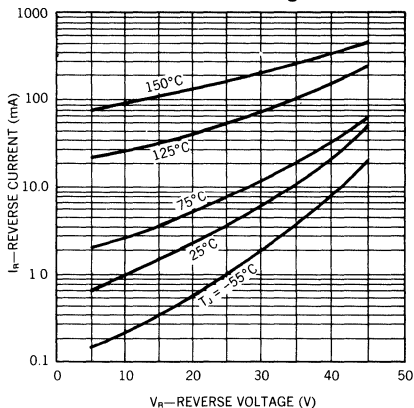
Notes:

1. Cathode is stud.
2. Maximum unlubricated stud torque: 30 inch pounds.
3. Angular orientation of terminal is undefined.
4. Maximum tension (90°) anode terminal 15 pounds for 30 seconds.

Typical Forward Current vs Forward Voltage



Typical Reverse Current vs Reverse Voltage

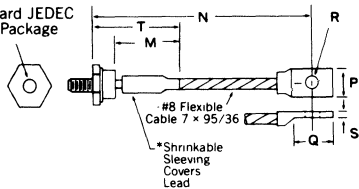


MECHANICAL SPECIFICATIONS

FLEXIBLE TOP LEAD (OPTIONAL)
Add an "F" Suffix to Part Number.

1N6097, 1N6098

Standard JEDEC
DO-5 Package

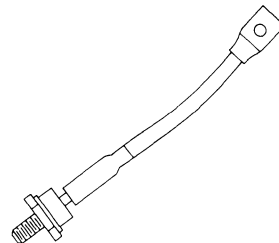


	INCHES	MILLIMETERS
M	718 MAX.	18 24 MAX.
N	4 50 ± 250	114 3 ± 6.35
P	525 MAX.	13.23 MAX.
Q	675 ± 035	17 15 ± 0.89
R	205 ± 005	5 21 ± 0.13
S	.075 ± 010	1 91 ± 0.25
T	1 125 MAX	28 58 MAX

*To 125°C (Ambient)

Note: Consult Factory for Non-standard Lead Lengths

DO-5 with Flexible Lead



RECTIFIERS

High Efficiency, 70A

1N6304—1N6306
JAN, JANTX, JANTXV

FEATURES

- High Continuous Current Rating
- Very Low Forward Voltage
- Very Fast Switching Speeds
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available
- Qualified to MIL-S-19500/550

DESCRIPTION

The 1N6304 Series is specifically designed for operation in power switching circuits operating at frequencies of at least 20KHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, 1N6304	50V
Peak Inverse Voltage, 1N6305	100V
Peak Inverse Voltage, 1N6306	150V
Maximum Average D.C. Output Current at $T_c = 100^\circ\text{C}$	70A
Non-Repetitive Sinusoidal Surge Current 8.3ms	800A
Thermal Resistance, Junction to Case	0.8°C/W
Operating and Storage Temperature Range	-65°C to +175°C
Operating and Storage Temperature Range (JEDEC types)	-55°C to +175°C

POWER CYCLING

These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C, at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS

1N6304-1N6306

	ins.	mm
A	225 ± 005	5 72 ± 0 13
B	060 MIN	1 52 MIN
C	156 ± 020	3 96 ± 0 51
D	156 MIN FLAT	3 96 MIN FLAT
E	667 DIA MAX	16 94 DIA MAX
F	090 MAX	2 29 MAX
G	677 ± 010	17 20 ± 0 25
H	375 MAX	9 53 MAX
J	140 MIN DIA	3 56 MIN DIA
K	1 000 MAX	25 40 MAX
L	450 MAX	11 43 MAX
M	438 ± 015	11 13 ± 0 38
N	078 MAX	1 98 MAX

**DO-203AB
(DO-5)**

Notes:

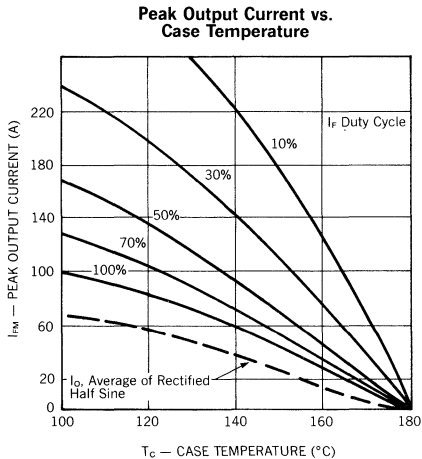
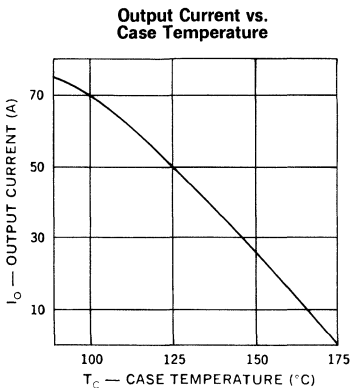
1. Standard polarity is cathode-to-stud.
For reverse polarity (anode-to-stud) add suffix "R", ie. 1N6304R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 20 inch pounds (20 kg. cm).
4. Angular orientation of terminal is undefined.

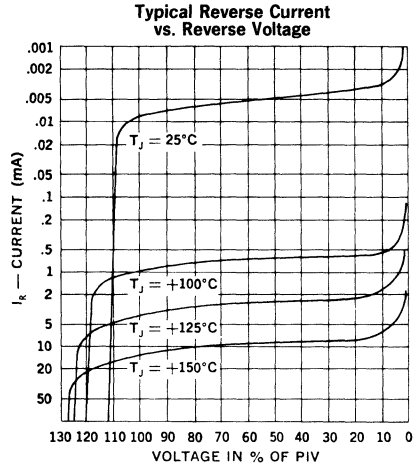
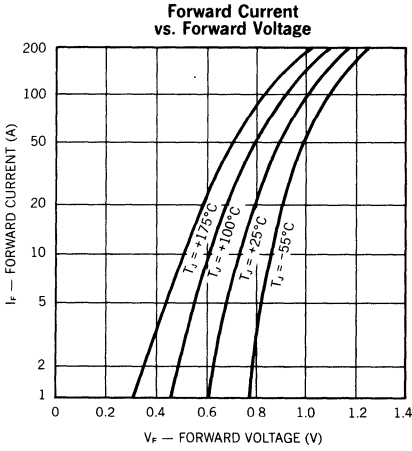
ELECTRICAL SPECIFICATIONS

Type	V _R	Maximum Forward Voltage V _F		Maximum Reverse Current I _R		Maximum Reverse Recovery Time t _{rr}
		T _c = 25°C	T _c = 150°C	T _c = 25°C	T _c = 150°C	
1N6304 1N6305 1N6306	50V 100V 150V	.975V @ 70A t _p = 300μs	.840V @ 70A t _p = 300μs	25μA	30mA	50ns 1A-1A-0.1A
J, JTX, JTXV 1N6304 J, JTX, JTXV 1N6305 J, JTX, JTXV 1N6306	50V 100V 150V	.975V @ 70A t _p = 300μs	.840V @ 70A t _p = 300μs	25μA	30mA	50ns ⁽¹⁾
		1.18V @ 150A t _p = 300μs				60ns ⁽²⁾

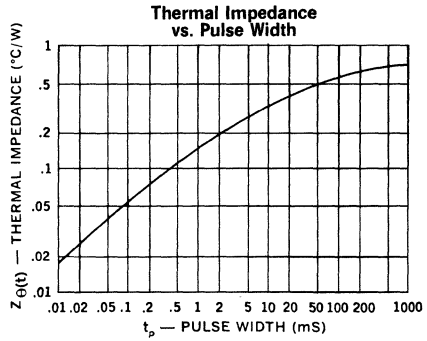
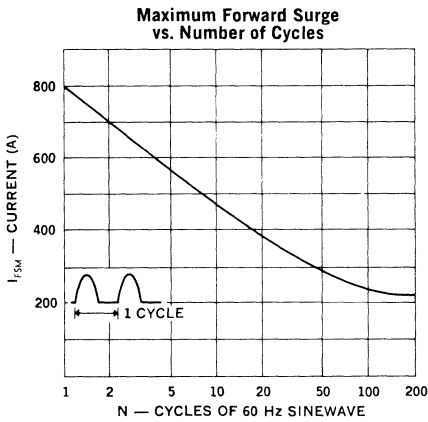
⁽¹⁾ I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A, di/dt = 85A/μs (min.).
⁽²⁾ I_{FM} = 70A, di/dt = 130A/μs.

Type	V _R	Maximum Forward Recovery Time	Maximum Forward Voltage	Maximum Junction Capacitance
J, JTX, JTXV 1N6304 J, JTX, JTXV 1N6305 J, JTX, JTXV 1N6306	50V 100V 150V	15ns I _{FM} = 1A, t _r = 8ns	2.2V I _{FM} = 1A, t _r = 8ns	@ -10V 600pF

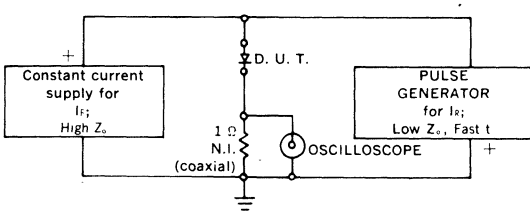




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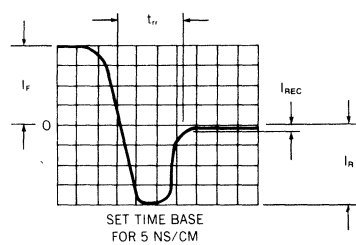


Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω .
 - Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance = 10Ω .
 - Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform



POWER SCHOTTKY RECTIFIERS

50A Pk, 45V

1N6391
JAN, JANTX, JANTXV

FEATURES

- Very Low Forward Voltage
- Low Recovered Charge
- Rugged Package Design (DO-4)
- High Efficiency for Low Voltage Supplies
- 45V Blocking @ Rated T_{jmax}
- 54V Repetitive Surge Voltage
- Qualified to MIL-S-19500/553

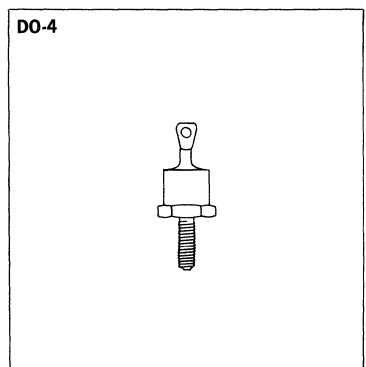
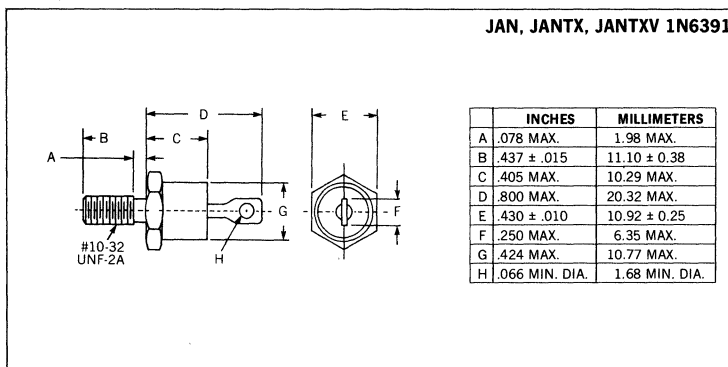
DESCRIPTION

The 1N6391 has a Schottky barrier junction and is ideally suited for output rectifiers and catch diodes in low voltage power supplies. Rugged design absorbs stress that can damage glass-to-metal seal during installation and use.

ABSOLUTE MAXIMUM RATINGS

Working Peak Reverse Voltage, V_{RWM}	45V
DC Blocking Voltage, V_R	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	54V
Average Rectified Forward Current, I_o @ $T_c = 125^\circ C$	25A
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20kHz, 50% Duty Cycle), I_{FRM} @ $T_c = 125^\circ C$	50A
Non-Repetitive Peak Surge Current (8.3ms), I_{FSM}	600A
Peak Reverse Transient Current, I_{RM}	2A
Operating and Storage Temperature Range	$-55^\circ C$ to $+175^\circ C$
Thermal Resistance, Junction to Case, $R_{\theta JC}$	2.0°C/W

MECHANICAL SPECIFICATIONS



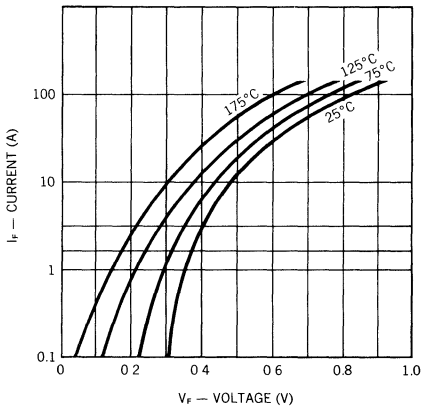
NOTES:

1. Cathode is stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 10 inch pounds.
4. Angular orientation of terminal is undefined.

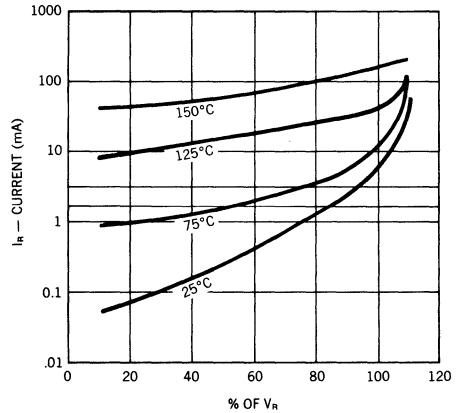
ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C)

Characteristic	Symbol	Limit	Units	Conditions
Maximum Instantaneous Reverse Current	i _R	15	mA	T _C = 25°C, V _R = V _{RWM}
		40	mA	T _C = 125°C
		40	mA	T _C = 175°C Pulse Width = 400μs Duty Cycle = 1%
Maximum Instantaneous Forward Voltage	V _F	0.44	V	i _F = 5A, T _C = 25°C
		0.68	V	i _F = 50A, T _C = 25°C Pulse Width = 300μs Duty Cycle = 1%
Capacitance	C _t	2000	pF	V _R = 5.0V

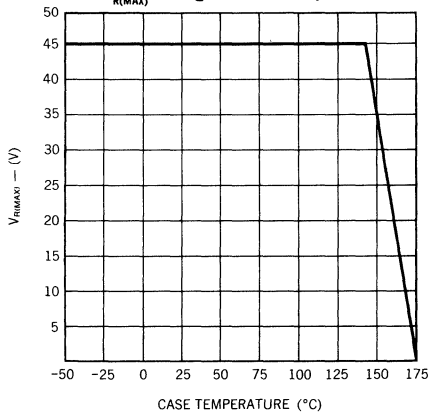
Typical Forward Current vs Forward Voltage



Typical Reverse Current vs Reverse Voltage



V_{R(MAX)} Rating vs Case Temperature



6

POWER SCHOTTKY RECTIFIERS

120A Pk

1N6392
JAN, JANTX, JANTXV

FEATURES

- Very Low Forward Voltage (0.6 at 60A, 125°C)
- Low Recovered Charge
- Rugged Package Design (DO-5)
- High Efficiency for Low Voltage Supplies
- Low Thermal Resistance (1.0°C/W)
- High Surge Current (800A)
- Low Reverse Current (60mA at rated V_R at 125°C)
- Qualified to MIL-S-19500/554

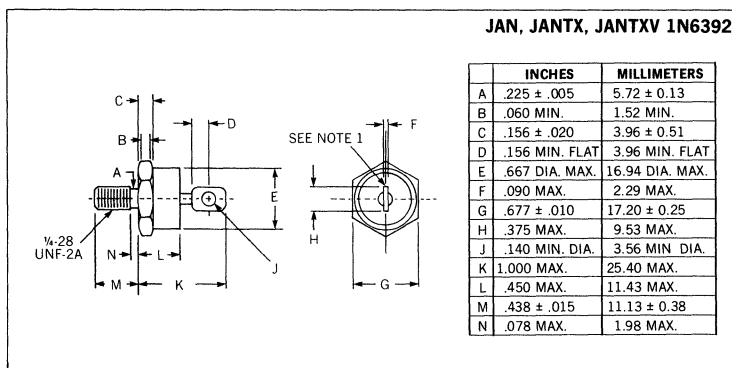
DESCRIPTION

The 1N6392 Schottky barrier power rectifier is ideally suited for output rectifiers and catch diodes in low voltage power supplies. The Unitrode high conductivity design, using a heavy copper top post and 4 point crimp, ensures cool thermal operation and low dynamic impedance. Rugged design absorbs stress that can damage glass-to-metal seal during installation and use.

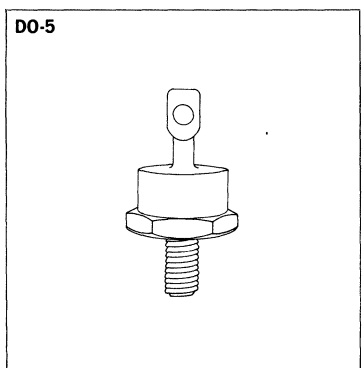
ABSOLUTE MAXIMUM RATINGS

Working Peak Reverse Voltage, V_{RWM}	45V
DC Blocking Voltage, V_R	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	54V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20kHz, 50% Duty Cycle), I_{FRM}	120A (at $T_C = 115^\circ\text{C}$)
Average Rectified Forward Current, I_{FAV}	60A (at $T_C = 115^\circ\text{C}$)
Non-Repetitive Peak Surge Current (8.3ms), I_{FSM}	800A
Peak Reverse Transient Current, I_{RM}	2A
Operating and Storage Temperature Range	-55°C to $+175^\circ\text{C}$
Thermal Resistance, Junction to Case, $R_{\theta JC}$	1.0°C/W

MECHANICAL SPECIFICATIONS



DO-5



NOTES:

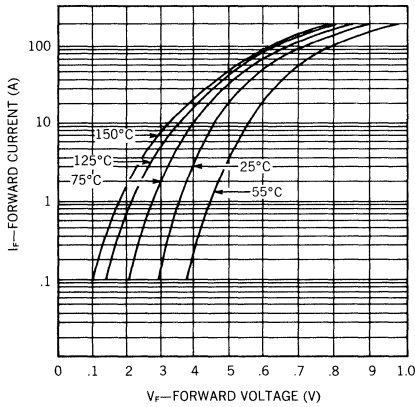
1. Cathode is stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds (35 kg. cm).
4. Angular orientation of terminal is undefined.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C)

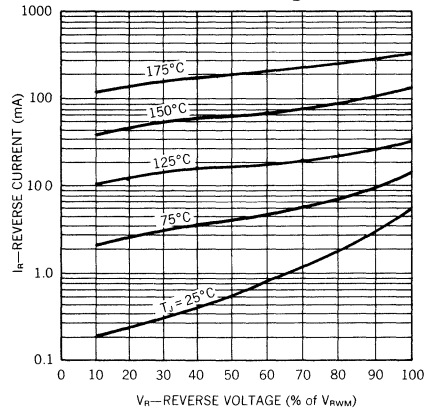
Characteristic	Symbol	Limit	Units	Conditions
Maximum Instantaneous Reverse Current	i _R	20	mA	V _R = V _{RWM} T _C = 125°C T _C = 175°C Pulse Width = 400μs Duty Cycle = 1%
		60	mA	
		600	mA	
Maximum Instantaneous Forward Voltage	V _F	0.47	V	i _F = 10A, T _C = 25°C i _F = 60A, T _C = 25°C i _F = 120A, T _C = 125°C Pulse Width = 300μs Duty Cycle = 1%
		0.68	V	
		0.82	V	
Maximum Capacitance	C _t	3000	pF	V _R = 5.0V

6

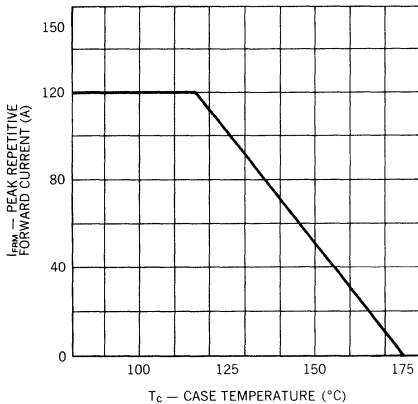
Typical Forward Current vs Forward Voltage



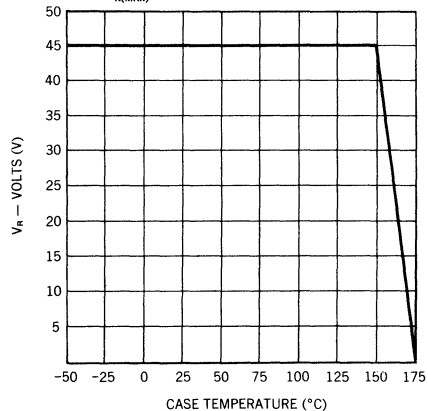
Typical Reverse Current vs Reverse Voltage



Maximum Current vs Case Temperature



V_{R(MAX)} Rating vs Case Temperature



POWER SCHOTTKY RECTIFIERS

SD51

120 Amp Pk, 45V

FEATURES

- Very Low Forward Voltage
- Low Recovered Charge
- Rugged Package Design (DO-5)
- High Efficiency for Low Voltage Supplies
- Available with Flexible Top Lead

DESCRIPTION

The SD51 has a Schottky barrier junction and is ideally suited for output rectifiers and catch diodes in low voltage power supplies. The Unitrode high conductivity design, using a heavy copper top post and a 4 point crimp, ensures cool terminal operation and low dynamic impedance. Rugged design absorbs stress that can damage glass-to-metal seal during installation and use.

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C)

Peak Repetitive Reverse Voltage, V _{RRM}	45V*
Working Peak Reverse Voltage, V _{RWM}	35V*
Peak Repetitive Forward Current (Rated V _R , Square Wave, 20 KHz, 50 percent Duty Cycle), I _{FRM}	120A
Non-repetitive Peak Surge Current (8.3 mS), I _{FSM}	800A
Peak Reverse Transient Current, I _{RM}	2A
Storage Temperature Range, T _{stg}	-55°C to +165°C
Junction Operating Temperature Range, T _j	-55°C to +150°C
Thermal Resistance, Junction-to-Case, R _{θJC}	1.0°C/W

*See curve of V_{RRM} Rating vs Case Temperature

MECHANICAL SPECIFICATIONS

SD51

	ins.	mm
A	.225 ± .005	5.72 ± 0.13
B	060 MIN.	1.52 MIN.
C	156 ± .020	3.96 ± 0.51
D	.156 MIN. FLAT	3.96 MIN. FLAT
E	.667 DIA. MAX.	16.94 DIA. MAX.
F	.090 MAX.	2.29 MAX.
G	.677 ± .010	17.20 ± 0.25
H	.375 MAX.	9.53 MAX.
J	140 MIN. DIA.	3.56 MIN. DIA.
K	1.000 MAX.	25.40 MAX.
L	.450 MAX.	11.43 MAX.
M	.438 ± .015	11.13 ± 0.38
N	.078 MAX.	1.98 MAX.

DO-5

Notes:

1. Cathode is stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds (35 kg. cm).
4. Angular orientation of terminal is undefined.

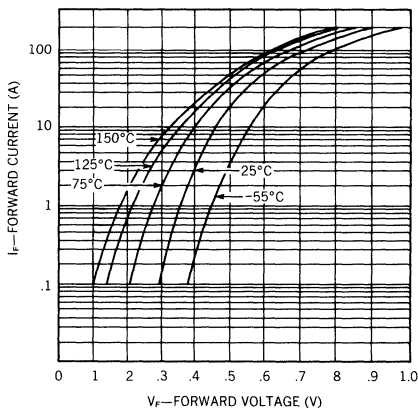
ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$)

Characteristic	Symbol	Limit	Units	Conditions
Maximum Instantaneous Reverse Current	i_R	50 200	mA mA	$T_c = 25^{\circ}C, V_R = 35V$ $T_c = 125^{\circ}C$ Pulse Width = $400\mu S$ Duty Cycle = 1 percent
Maximum Instantaneous Forward Voltage	V_F	0.60	V	$i_F = 60A$ $T_c = 125^{\circ}C$ Pulse Width = $300\mu S$ Duty Cycle = 1 percent
Flexible Top Lead Option	V_F	0.65	V	
Maximum Capacitance	C_T	4000	pF	$V_R = 5.0V$
Maximum Voltage Rate of Change	dv/dt	700	$V/\mu S$	$V_R = 35V$

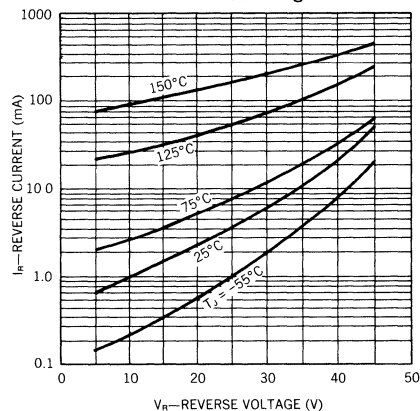
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 V_{RRM} Rating vs Case Temperature

Typical Forward Current vs Forward Voltage



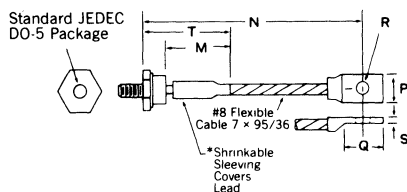
Typical Reverse Current vs Reverse Voltage



MECHANICAL SPECIFICATIONS

FLEXIBLE TOP LEAD (OPTIONAL)
Add an "F" Suffix to Part Number.

SD51F

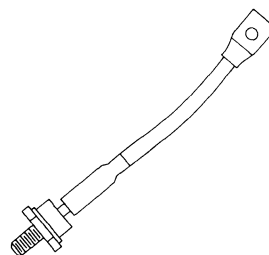


	INCHES	MILLIMETERS
M	.718 MAX	18.24 MAX.
N	$4.50 \pm .250$	114.3 ± 6.35
P	.525 MAX.	13.23 MAX.
Q	$675 \pm .035$	17.15 ± 0.89
R	$205 \pm .005$	5.21 ± 0.13
S	$075 \pm .010$	1.91 ± 0.25
T	1.125 MAX	28.58 MAX

*To 125°C (Ambient)

Note: Consult Factory for Non-standard Lead Lengths.

DO-5 with Flexible Lead



DUAL POWER SCHOTTKY RECTIFIERS

SD241

30 Amp Pk per diode, 45V

FEATURES

- Very Low Forward Voltage
- Low Recovered Charge
- Rugged Packaged Design (TO-3)
- High Efficiency for Low Voltage Supplies
- Dual Schottky Rectifiers in a Single Package

DESCRIPTION

The SD241 has two Schottky barrier junctions arranged in a common cathode configuration and is ideally suited for output rectifiers and catch diodes in low voltage supplies.

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C) Per Diode

Peak Repetitive Reverse Voltage, V _{RRM}	45V*
Working Peak Reverse Voltage, V _{RWM}	35V
Average Rectified Forward Current, I _o	30A
Non-repetitive Peak	
Surge current (8.3 ms), I _{FSM}	400A
Peak Reverse Transient Current, I _{RM}	2A
Storage Temperature Range, T _{stg}	-55°C to +175°C
Junction Operating Temperature Range, T _J	-55°C to +150°C
Package Thermal Resistance, Junction to Case, R _{θJC}	1.4°C/W

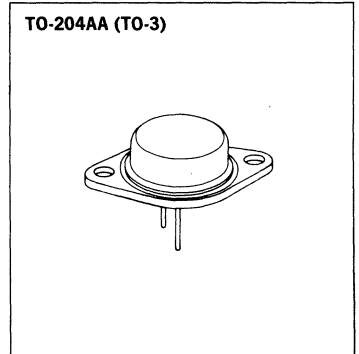
* See curve of V_{RRM} Rating vs Case Temperature.

MECHANICAL SPECIFICATIONS

NOTE:
Leads may be soldered to within 1/16" of base provided temperature-time exposure is less than 260°C for 10 seconds.

SD241

	ins.	mm.
A	.875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-.450	6.35-11.43
D	312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	205-.225	5.21-5.72
K	420-.440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.



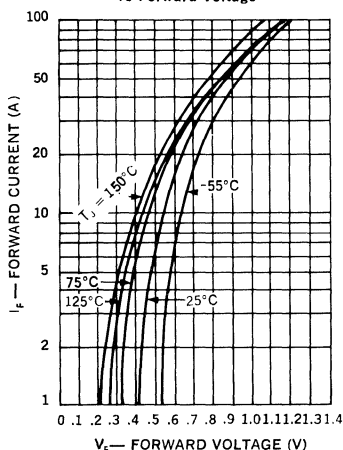
Notes: All metal surfaces tin plated.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$) Per Diode

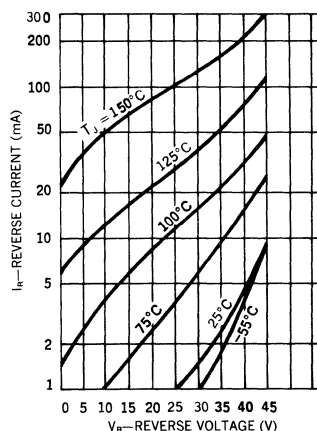
Characteristic	Symbol	Limit	Units	Conditions
Maximum Instantaneous Reverse Current	i_R	25 100	mA mA	$T_C = 25^{\circ}C, V_R = 35V$ $T_C = 125^{\circ}C$ Pulse Width = $400\mu S$ Duty Cycle = 1 percent
Maximum Instantaneous Forward Voltage	V_F	.47	V	$i_F = 10A$ Pulse Width = $300\mu S$ Duty Cycle = 1 percent $T_C = 125^{\circ}C$
		.60	V	$i_F = 20A$ Pulse Width = $300\mu S$ Duty Cycle = 1 percent $T_C = 125^{\circ}C$
Maximum Capacitance	C_i	2000	pF	$V_R = 5.0V$
Maximum Voltage Rate of Change	dv/dt	1000	$v/\mu S$	$v_R = 35V$

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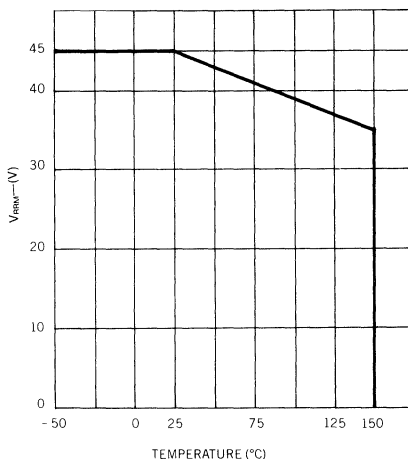
Typical Forward Current vs Forward Voltage



Typical Reverse Current vs Reverse Voltage



VRRM Rating vs Case Temperature



RECTIFIERS

High Efficiency, 2A

SES5001-SES5003

FEATURES

- Fast Recovery Times
- Low Forward Voltage
- Small Size
- Convenient Package

DESCRIPTION

An axial leaded power rectifier useful in many switching applications. Particularly suited where very fast recovery and low forward voltage are required.

ABSOLUTE MAXIMUM RATINGS

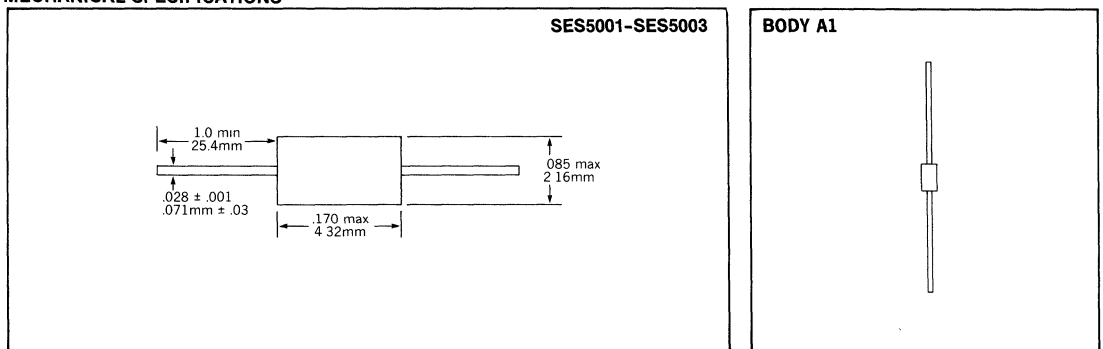
Peak Inverse Voltage, SES5001	50V
Peak Inverse Voltage, SES5002	100V
Peak Inverse Voltage, SES5003	150V
Maximum Average D.C. Output Current at $T_L = 75^\circ\text{C}$, $L = 3/8"$	2A
Non-Repetitive Surge Current at 8.3mS	35A
Thermal Resistance, @ $L = 3/8"$	38°C/W
Operating and Storage Temperature Range	-55°C + 175°C

ELECTRICAL SPECIFICATIONS

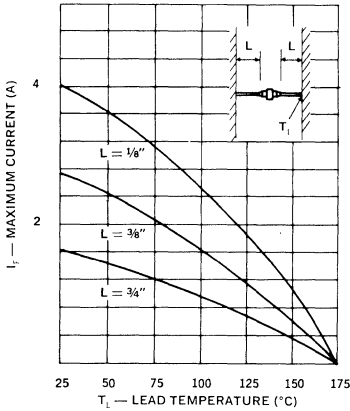
Type	PIV	Maximum Forward Voltage (V_F)		Maximum Reverse Current (I_R)		Maximum Reverse Recovery Time*
		@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$	
SES5001	50V	.975V	.895V			
SES5002	100V	@	@	2 μA	50 μA	100nS
SES5003	150V	1A	1A			

*Measured in circuit $I_F = .5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = .25\text{A}$

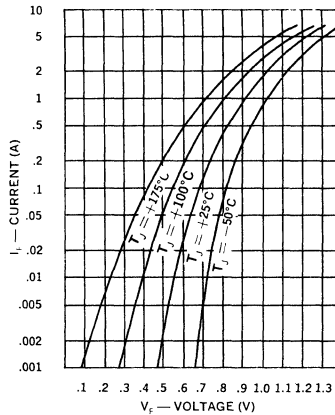
MECHANICAL SPECIFICATIONS



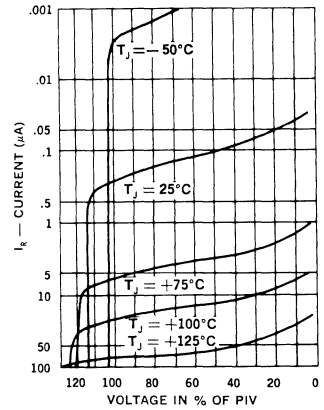
Output Current vs. Lead Temperature



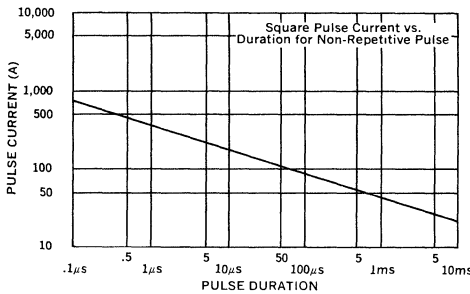
Typical Forward Current vs. Forward Voltage



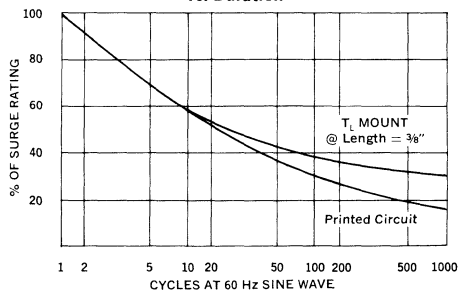
Typical Reverse Current vs. Voltage



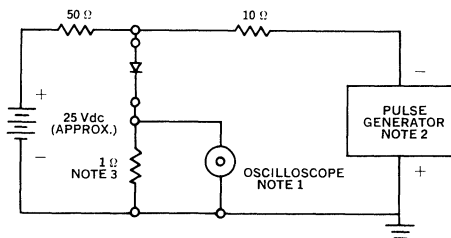
Forward Pulse Current vs. Duration



Multiple Surge Current vs. Duration



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3nS$; input impedance = 50Ω .
2. Pulse Generator: Rise time $\leq 8nS$; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 5A

SES5301-SES5303

FEATURES

- Low Forward Voltage
- Fast Recovery Times
- Small Size
- High Surge

DESCRIPTION

An axial leaded power rectifier useful in many switching applications. Particularly suited where very fast recovery and low forward voltage are required.

ABSOLUTE MAXIMUM RATINGS

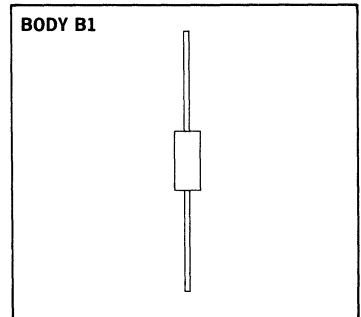
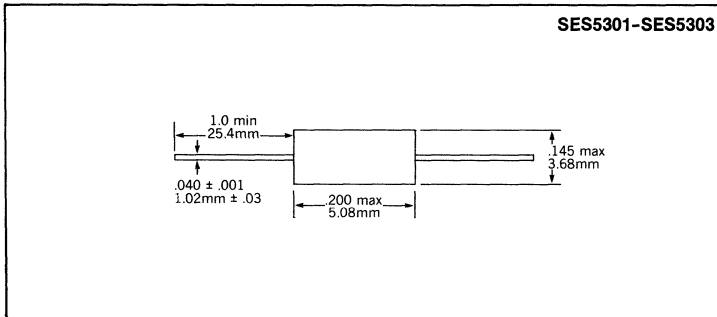
Peak Inverse Voltage, SES5301	50V
Peak Inverse Voltage, SES5302	100V
Peak Inverse Voltage, SES5303	150V
Maximum Average D.C. Output Current at $T_L = 75^\circ\text{C}$, $L = 3/8"$	5A
Non-Repetitive Sinusoidal Surge Current at 8.3mS	110A
Thermal Resistance at $L = 3/8"$	$.20^\circ\text{C/W}$
Operating and Storage Temperature Range	-55°C to $+170^\circ\text{C}$

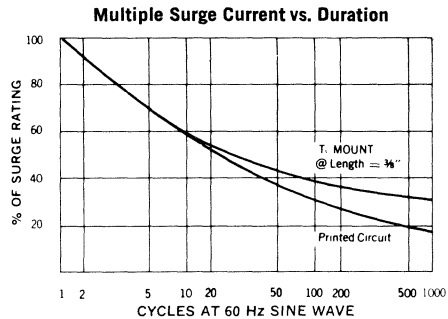
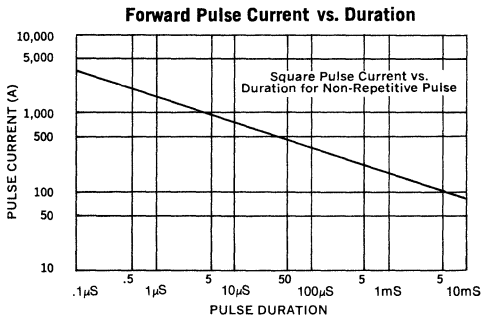
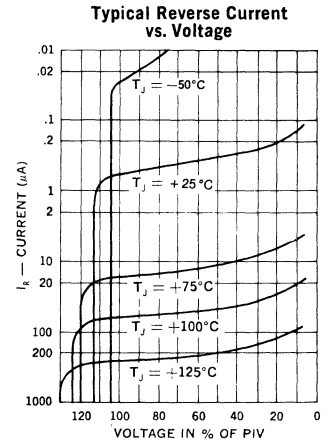
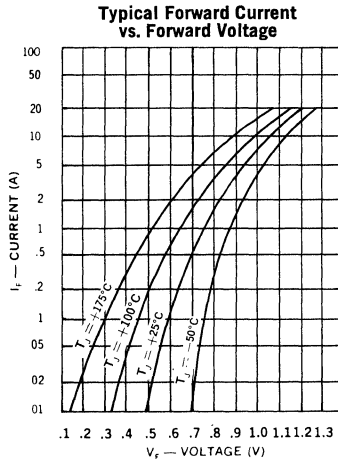
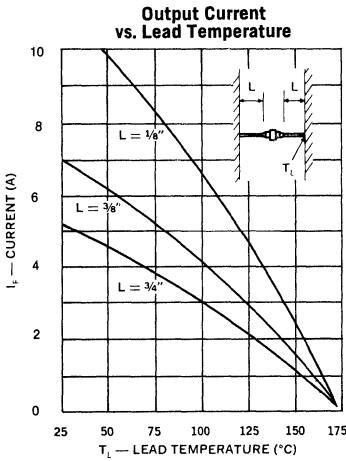
ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$	
SES5301	50V	0.975V	0.895V	5 μA	150 μA	100 ns
SES5302	100V	@	@			
SES5303	150V	5A	5A			

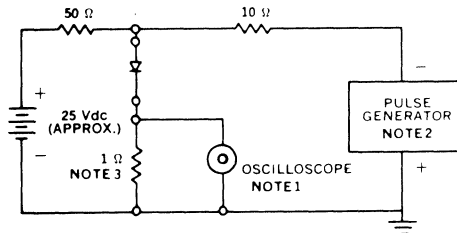
*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = 0.25\text{A}$

MECHANICAL SPECIFICATIONS





Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 nS; input impedance = 50 Ω .
2. Pulse Generator: Rise time ≤ 8 nS; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 8A

SES5401-SES5404

FEATURES

- Low Forward Voltage
- Fast Recovery Times
- Economical, Convenient TO-220 Package
- Low Thermal Resistance
- Mechanically Rugged
- PIV up to 200V

DESCRIPTION

The SES5401 Series, in the economical, convenient TO-220 package, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5401	50V
Peak Inverse Voltage, SES5402	100V
Peak Inverse Voltage, SES5403	150V
Peak Inverse Voltage, SES5404	200V
Maximum Average D.C. Output Current	
@ $T_C = 125^\circ\text{C}$	8.0A
@ $T_A = 25^\circ\text{C}$	3.0A
@ $T_A = 25^\circ\text{C}$ (Note 1)	8.0A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	70A
Thermal Resistance, Junction to Case, θ_{J-C}	2.5°C/W
Thermal Resistance, Junction to Ambient, θ_{J-A}	60°C/W
Operating and Storage Temperature Range	-55°C to +150°C

NOTE 1. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8\text{ns}$
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$		
SES5401	50V	1.025V @ 8A	0.945V @ 8A	5 μA	150 μA 150 μA 150 μA 500 μA	100ns	1.4V
SES5402	100V						
SES5403	150V						
SES5404	200V						

*Measured in circuit $I_F = 0.50\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = 0.25\text{A}$

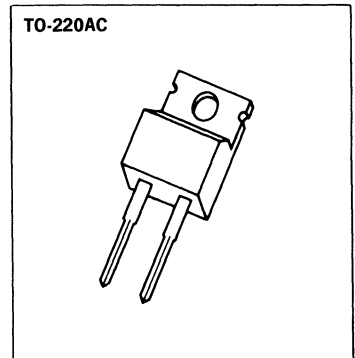
MECHANICAL SPECIFICATIONS

SEATING PLANE

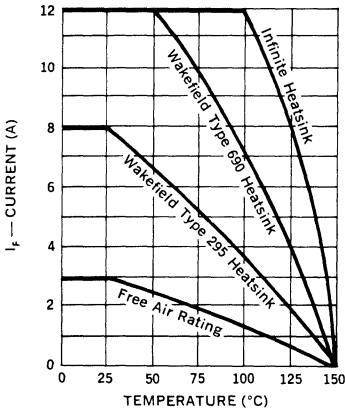
PIN 1. Cathode
2. Anode
Tab is connected to Cathode.

SES5401-SES5404

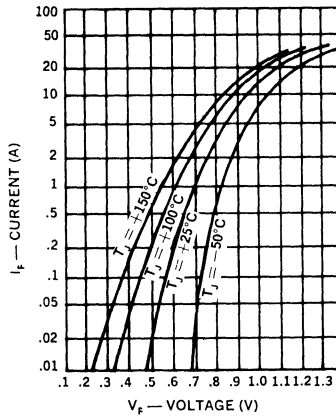
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85



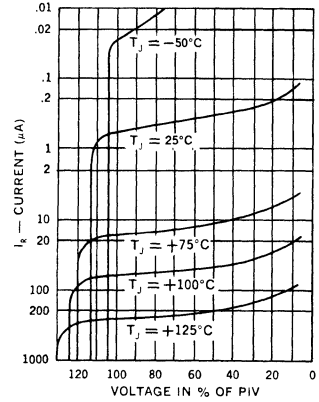
Output Current vs. Temperature



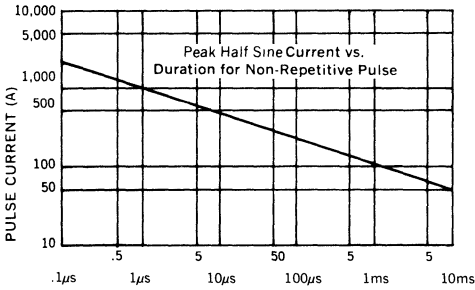
Typical Forward Current vs. Forward Voltage



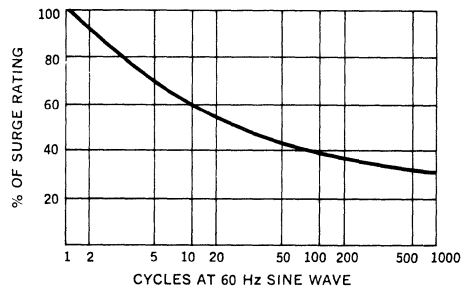
Typical Reverse Current vs. Voltage



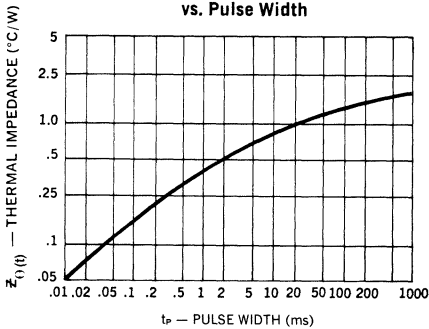
Forward Pulse Current vs. Duration



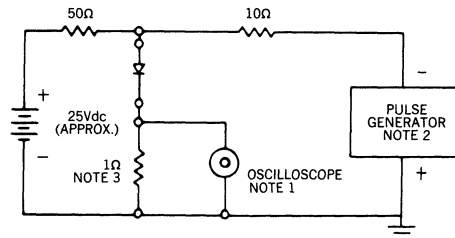
Multiple Surge Current vs. Duration



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω.
2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 16A

SES5501
SES5502
SES5503
SES5504

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Economical, Convenient TO-220 Package
- Low Thermal Resistance
- Mechanically Rugged

DESCRIPTION

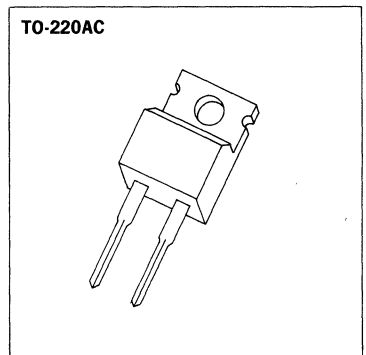
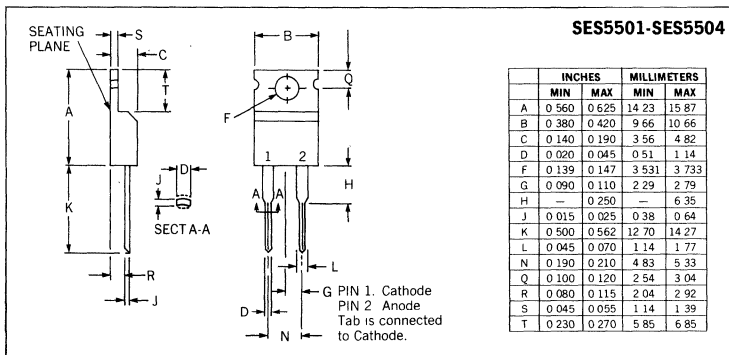
The SES5500 Series, in the economical, convenient TO-220 package, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5501	50V
Peak Inverse Voltage, SES5502	100V
Peak Inverse Voltage, SES5503	150V
Peak Inverse Voltage, SES5504	200V
Maximum Average D.C. Output Current	
@ $T_c = 95^\circ\text{C}$	16A
@ $T_A = 25^\circ\text{C}$	3.3A
@ $T_A = 25^\circ\text{C}$ (Note 1)	9.0A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	250A
Thermal Resistance, Junction to Case, θ_{j-c}	1.5°C/W
Thermal Resistance, Junction to Ambient, θ_{j-a}	60°C/W
Operating and Storage Temperature	-55°C to +150°C

Note: 1. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs Temperature Curve on this data sheet.

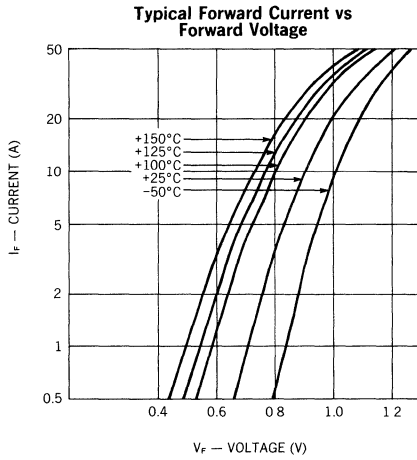
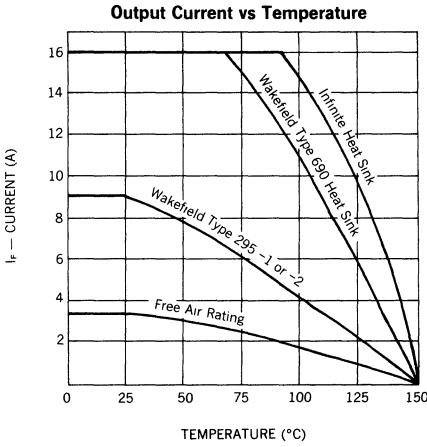
MECHANICAL SPECIFICATIONS



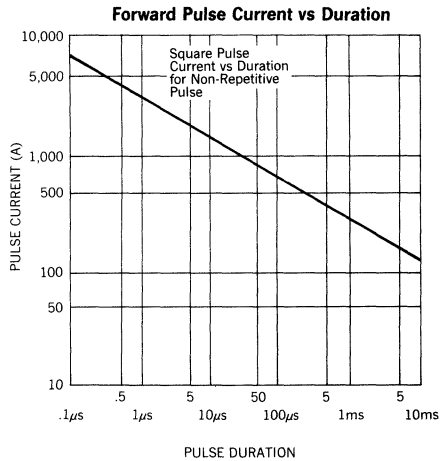
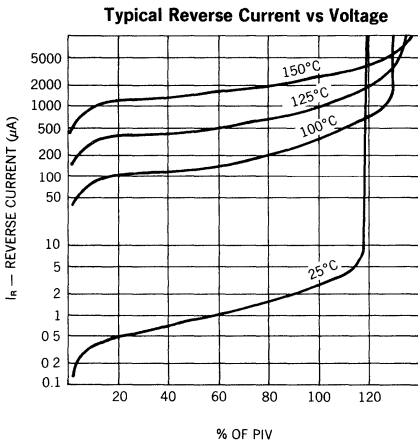
ELECTRICAL SPECIFICATIONS

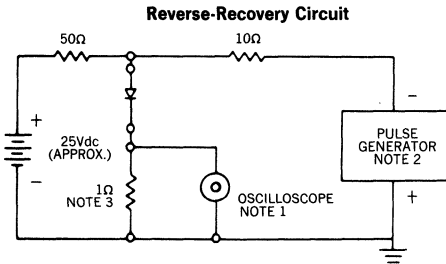
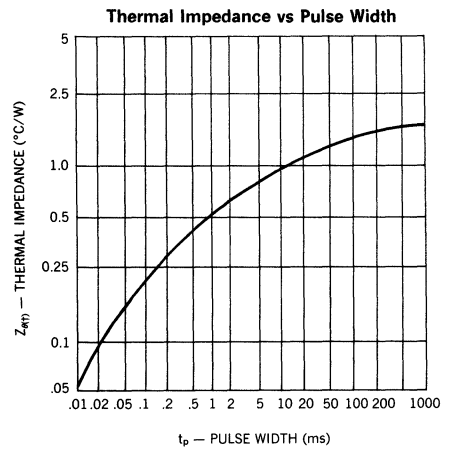
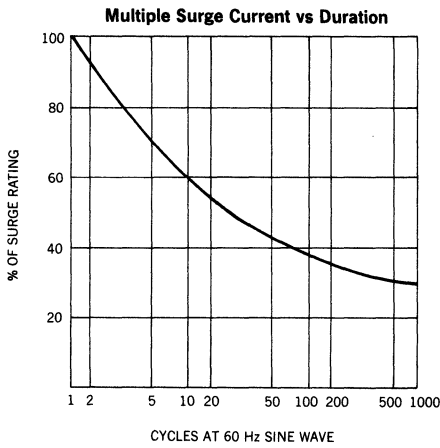
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8ns$
		$T_J = 25^\circ C$	$T_J = 100^\circ C$	$T_J = 25^\circ C$	$T_J = 100^\circ C$		
SES5501	50V	1.025V @ 16A	.945V @ 16A	10 μ A	800 μ A	100ns	2.0V
SES5502	100V						
SES5503	150V						
SES5504	200V						

* Measured in circuit $I_F = 1/2A$, $I_R = 1.0A$, $I_{REC} = 1/4A$



6





- NOTES:**
1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω.
 2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10Ω.
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 16A Center-Tap

SES5401C-SES5404C

FEATURES

- Low Forward Voltage
- Fast Recovery Times
- Economical, Convenient TO-220AB Package
- Low Thermal Resistance
- Mechanically Rugged
- PIV up to 200V

DESCRIPTION

The SES5401C Series in the economical, convenient TO-220AB package, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The series combines two high efficiency devices into one package, simplifying installation, reducing heatsink requirements and the need to purchase matched components.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5401C	50V
Peak Inverse Voltage, SES5402C	100V
Peak Inverse Voltage, SES5403C	150V
Peak Inverse Voltage, SES5404C	200V
Maximum Average D.C. Output Current	
@ $T_C = 125^\circ\text{C}$	16A
@ $T_A = 25^\circ\text{C}$	3A
@ $T_A = 25^\circ\text{C}$ (Note 1)	10A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	70A
Thermal Resistance, Junction to Case, θ_{J-C}	1.75 $^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient, θ_{J-A}	60 $^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$

NOTE 1. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8\text{ns}$
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$		
SES5401C	50V	1.025V @ 8A	0.945V @ 8A	5 μA	150 μA	100ns	1.4V
SES5402C	100V				150 μA		
SES5403C	150V				150 μA		
SES5404C	200V				500 μA		

*Measured in circuit $I_F = 0.50\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = 0.25\text{A}$

MECHANICAL SPECIFICATIONS

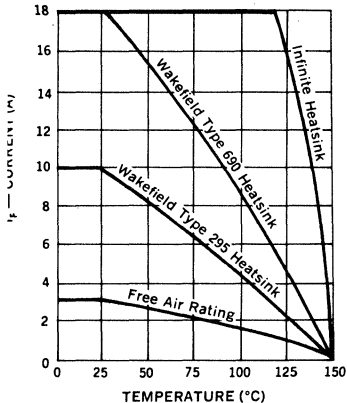
SES5401C-SES5404C

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

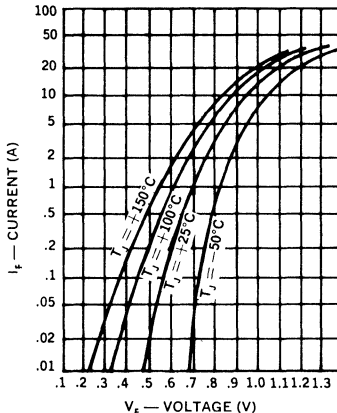
TO-220AB



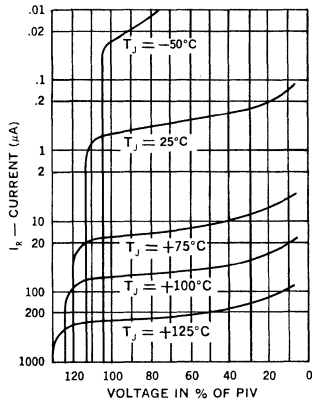
Output Current vs. Temperature



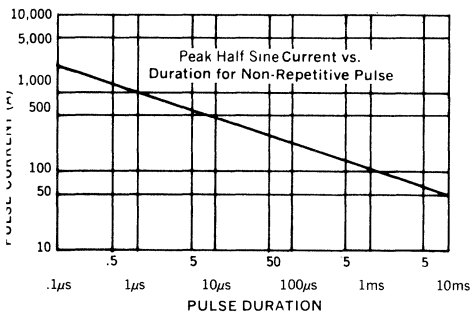
Typical Forward Current vs. Forward Voltage



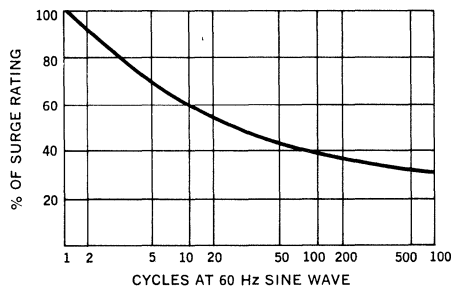
Typical Reverse Current vs. Voltage



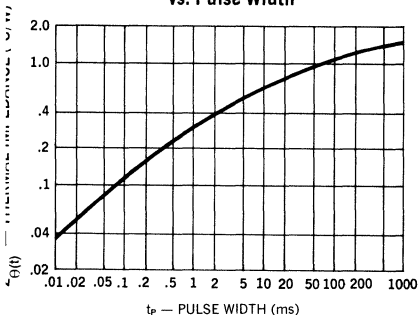
Forward Pulse Current vs. Duration



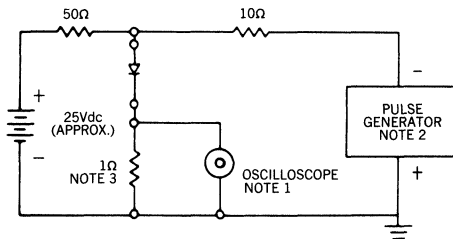
Multiple Surge Current vs. Duration



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3ns$; input impedance = 50 Ω .
2. Pulse Generator: Rise time $\leq 8ns$; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 25A Center-Tap

SES5601C
SES5602C
SES5603C

FEATURES

- Low Forward Voltage
- Fast Switching Speed
- Convenient Package
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged TO-3 Package
- Available as Positive or Negative Center-Tap

DESCRIPTION

The SES, super-fast recovery, rectifiers are specifically designed for operation in power switching circuits. Their super-fast recovery time and very low forward voltage make them particularly efficient in most switching applications.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5601C	50V
Peak Inverse Voltage, SES5602C	100V
Peak Inverse Voltage, SES5603C	150V
Maximum Average D.C. Output Current at $T_C = 100^\circ\text{C}$	25A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	400A
Thermal Resistance, Junction to Case	1°C/W
Operating and Storage Temperature Range	-55°C to +175°C

ELECTRICAL SPECIFICATIONS PER DIODE

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
		$T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$	@ $T_C = 25^\circ\text{C}$	@ $T_C = 125^\circ\text{C}$	
SES5601C	50V	0.990V	0.830V	20 μA	4mA	100nS
SES5602C	100V	@	@			
SES5603C	150V	12.5A $t_p = 300\mu\text{S}$	12.5A $t_p = 300\mu\text{S}$			

*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = 0.25\text{A}$

MECHANICAL SPECIFICATIONS

POSITIVE OUTPUT

CASE

F, M, L, G, H, J, K, E, A, B, C, D

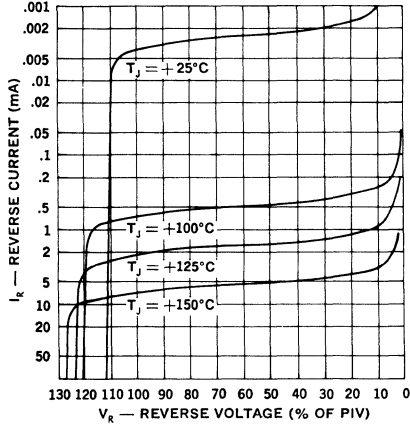
	ins.	mm
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.00-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA (TO-3)

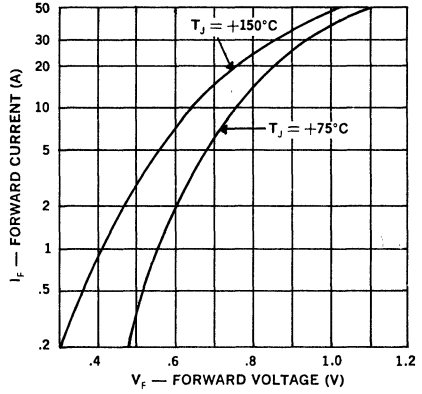
NOTES:

- Standard polarity is positive output.
For reverse polarity (negative output) add suffix "R", i.e. SES5601CR.
- All metal surfaces tin plated.

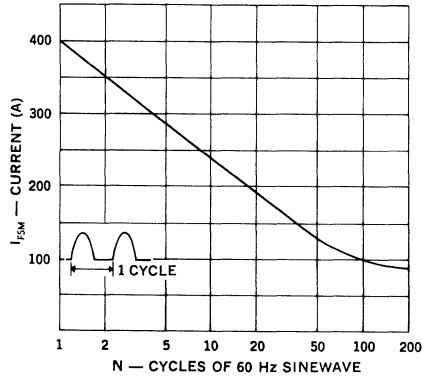
Typical Reverse Current vs. Reverse Voltage



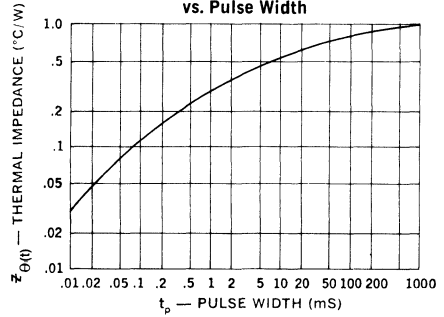
Typical Forward Current vs. Forward Voltage



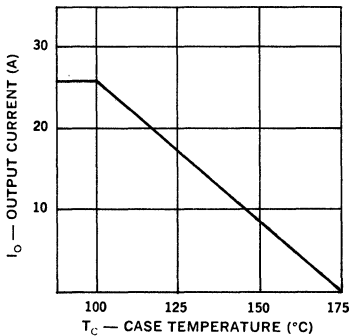
Maximum Forward Surge vs. Number of Cycles



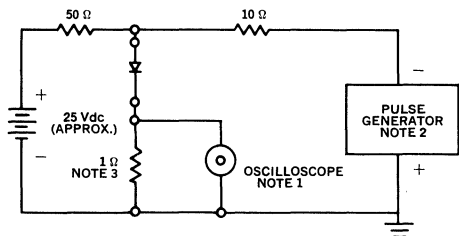
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{nS}$; input impedance = 50Ω .
2. Pulse Generator: Rise time $\leq 8\text{nS}$; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 20A

SES5701
SES5702
SES5703

FEATURES

- Low Forward Voltage
- Fast Switching
- Low Thermal Resistance
- High Surge Capability
- Mechanically Rugged DO-4 Package
- Reverse Polarity Available

DESCRIPTION

The SES, super-fast recovery, rectifiers are specifically designed for operation in power switching circuits. Their super-fast recovery time and very low forward voltage drop make them particularly efficient in most switching applications.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5701	50V
Peak Inverse Voltage, SES5702	100V
Peak Inverse Voltage, SES5703	150V
Maximum Average D.C. Output Current at $T_c = 100^\circ\text{C}$	20A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	400A
Thermal Resistance, Junction to Case	1.5°C/W
Operating and Storage Temperature Range	-55°C to +175°C

6

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
			$T_c = 125^\circ\text{C}$	@ $T_c = 25^\circ\text{C}$	@ $T_c = 125^\circ\text{C}$	
SES5701	50V	.990V	.830			100nS
SES5702	100V	@	@	20μA	4mA	
SES5703	150V	20A $t_p = 300\mu\text{S}$	20A $t_p = 300\mu\text{S}$			

*Measured in circuit $I_F = .5\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = .25\text{A}$

MECHANICAL SPECIFICATIONS

SES5701-SES5703

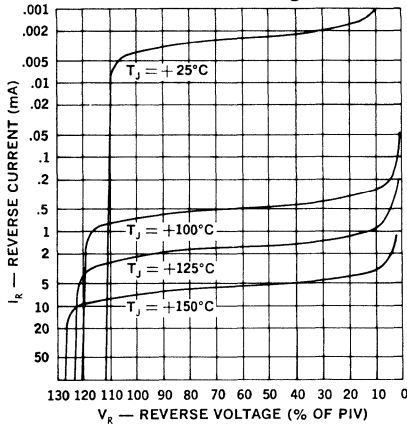
	ins.	mm
A	.078 MAX.	1.98 MAX.
B	$\pm .437 \pm .015$	11.10 ± 0.38
C	.405 MAX.	10.29 MAX.
D	.800 MAX.	20.32 MAX.
E	.424 MAX.	10.77 MAX.
F	.066 MIN. DIA.	1.68 MIN. DIA.
G	.430 $\pm .010$	10.92 ± 0.25
H	.250 MAX.	6.35 MAX.

DO-4

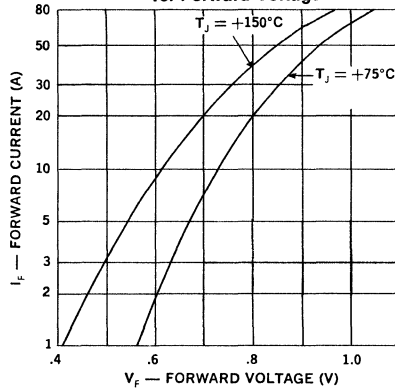
NOTES:

1. Standard polarity is cathode-to-stud.
For reverse Polarity (anode-to-stud) add suffix "R", ie. SES5701R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 10 inch pounds.
4. Angular orientation of terminal is undefined.

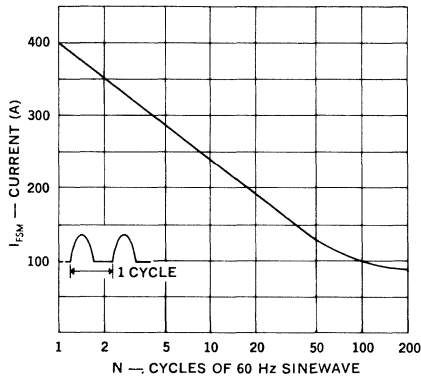
Typical Reverse Current vs. Reverse Voltage



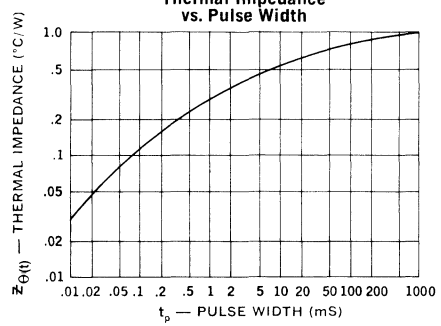
Typical Forward Current vs. Forward Voltage



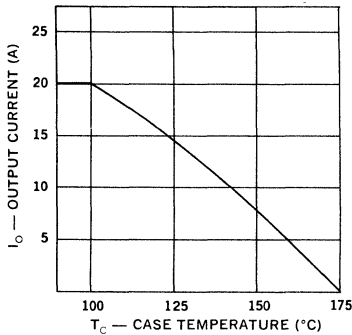
Maximum Forward Surge vs. Number of Cycles



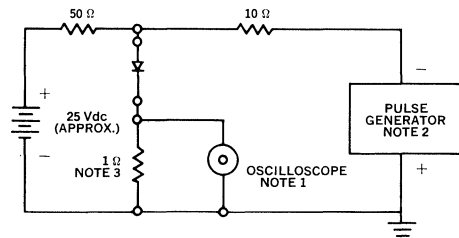
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



- NOTES:**
1. Oscilloscope: Rise time $\leq 3nS$; input impedance = 50 Ω .
 2. Pulse Generator: Rise time $\leq 8nS$; source impedance 10 Ω .
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 60A

SES5801
SES5802
SES5803

FEATURES

- Low Forward Voltage
- Fast Switching Speeds
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged DO-5 Package
- Reverse Polarity Available

DESCRIPTION

The SES, super-fast recovery, rectifiers are specifically designed for operation in power switching circuits. Their super-fast recovery time and very low forward voltage drop make them particularly efficient in most switching applications.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5801	50V
Peak Inverse Voltage, SES5802	100V
Peak Inverse Voltage, SES5803	150V
Maximum Average D.C. Output Current at $T_c = 100^\circ\text{C}$	60A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	800A
Thermal Resistance, Junction to Case	0.8°C/W
Operating and Storage Temperature Range	-55°C to $+175^\circ\text{C}$

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
		$T_c = 25^\circ\text{C}$	$T_c = 150^\circ\text{C}$	@ $T_c = 25^\circ\text{C}$	@ $T_c = 150^\circ\text{C}$	
SES5801 SES5802 SES5803	50V 100V 150V	0.990V @ 60A $t_p = 300\mu\text{s}$	0.850V @ 60A $t_p = 300\mu\text{s}$	25 μA	30mA	100nS

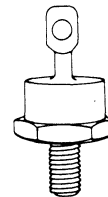
*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = 0.25\text{A}$

MECHANICAL SPECIFICATIONS

SES5801-SES5803

	ins.	mm
A	225 ± .005	5.72 ± 0.13
B	.060 MIN	1.52 MIN.
C	.156 ± .020	3.96 ± 0.51
D	.156 MIN. FLAT	3.96 MIN. FLAT
E	.667 DIA. MAX	16.94 DIA. MAX
F	.090 MAX	2.29 MAX
G	.667 ± .010	16.94 ± 0.25
H	.375	9.53
J	.140 MIN. DIA	3.56 MIN. DIA
K	1.000 MAX	25.40 MAX
L	.450 MAX	11.43 MAX
M	.438 ± .015	11.13 ± 0.38
N	.078 MAX	1.98 MAX.

DO-5

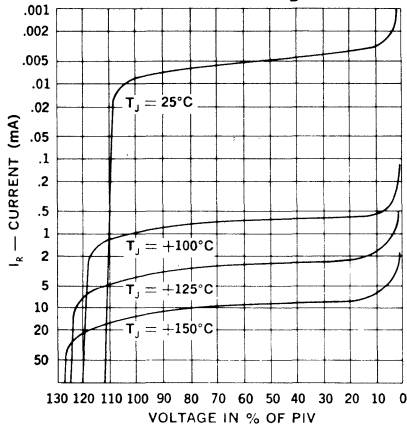


Notes:

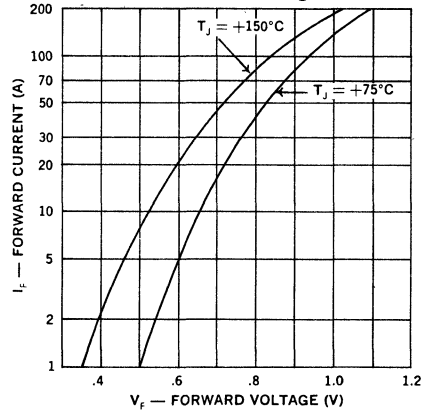
1. Standard polarity is cathode-to-stud.
For reverse polarity (anode-to-stud) add suffix "R", ie. SES5801R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 20 inch pounds.
4. An angular orientation of terminal is undefined.



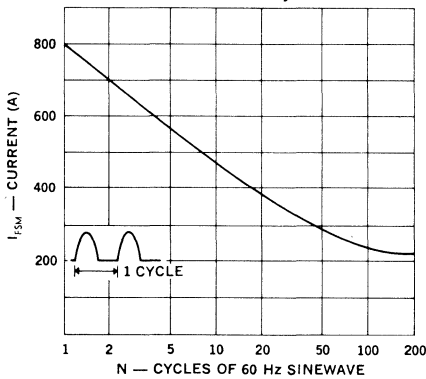
Typical Reverse Current vs. Reverse Voltage



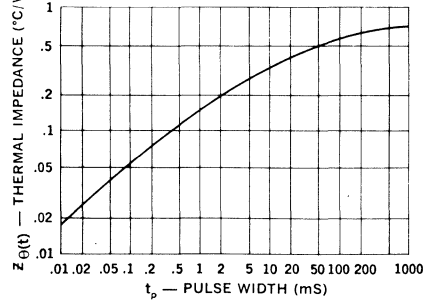
Forward Current vs. Forward Voltage



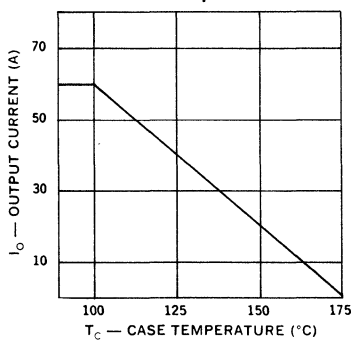
Maximum Forward Surge vs. Number of Cycles



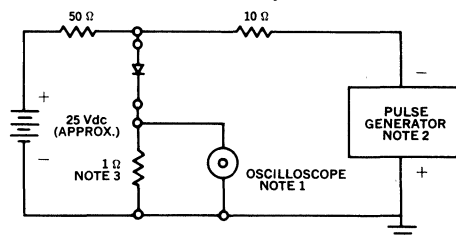
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time $\leq 3\text{nS}$; input impedance = 50Ω.
 - Pulse Generator: Rise time $\leq 8\text{nS}$; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 50 Amp

UES501-UES505

FEATURES

- 50A Continuous Rating at Case Temperature of 125°C
- Exceptional Efficiency
- Low Forward Voltage
- Extremely Fast Reverse Recovery Time
- Extremely Fast Forward Recovery Time
- High Surge
- Radiation Tolerant
- Rugged, High Current Termination

DESCRIPTION:

This series of High Efficiency Power Rectifiers allows circuit designers to design high current, high frequency supplies with very low diode losses. Reverse recovery time is typically 1/10 - 1/100th of equivalent power rectifiers, with even lower forward voltage.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	Type
50V	UES501
75V	UES502
100V	UES503
125V	UES504
150V	UES505

Maximum Average D.C. Output Current

@ $T_C = 125^\circ\text{C}$ 50A

Non-Repetitive Sinusoidal

Surge Current (8.3ms) 600A

Operating Temperature Range -65°C to $+175^\circ\text{C}$

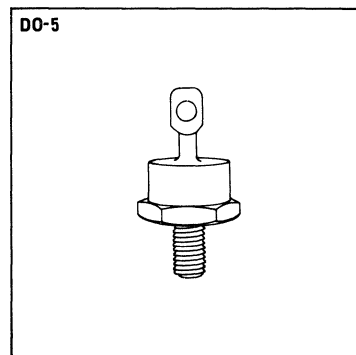
Storage Temperature Range -65°C to $+175^\circ\text{C}$

Thermal Resistance 1°C/W

MECHANICAL SPECIFICATIONS

UES501-UES505

	ins.	mm
A	225 ± .005	5 72 ± 0.13
B	060 MIN	1 52 MIN
C	156 ± .020	3 96 ± 0 51
D	156 MIN FLAT	3 96 MIN FLAT
E	667 DIA MAX	16 94 DIA MAX
F	090 MAX	2 29 MAX
G	677 ± .010	17 20 ± 0 25
H	375 MAX	9 53 MAX
J	140 MIN DIA	3 56 MIN DIA
K	1 000 MAX	25 40 MAX
L	450 MAX	11 43 MAX
M	438 ± .015	11 13 ± 0 38
N	078 MAX	1 98 MAX



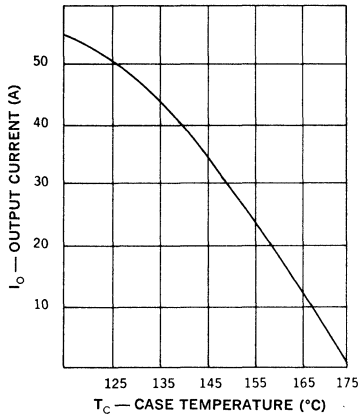
Notes:

1. Angular orientation of terminal is undefined.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds.
4. All dimensions in inches.
5. Polarity is cathode to stud; for anode to stud add suffix "R".

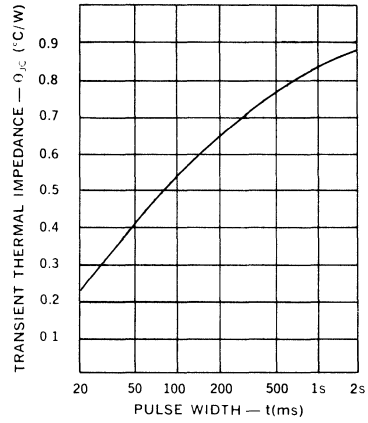
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Maximum Forward Voltage Drop	Maximum Leakage Current		Maximum Reverse Recovery Time $t_{rr} @ I_F = I_R = I_{REC}$
			25°C	125°C	
UES501	50V	.95V @ 50A (pw = 250ms)	25μA	10mA	50ns, 1A-1A-0.5A
UES502	75V				
UES503	100V				
UES504	125V				
UES505	150V				

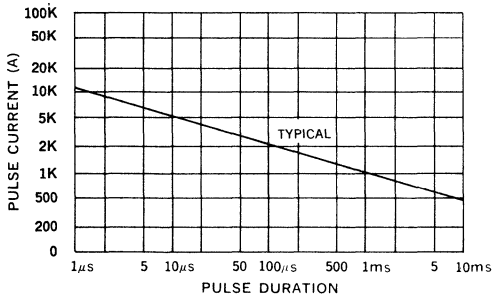
Output Current vs. Case Temp.



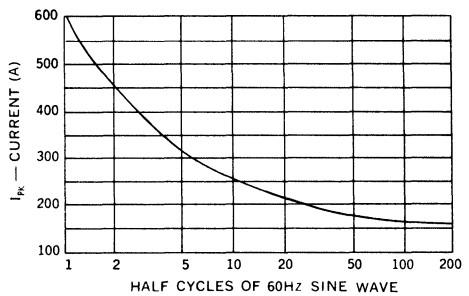
Pulse Thermal Impedance vs. Pulse Width



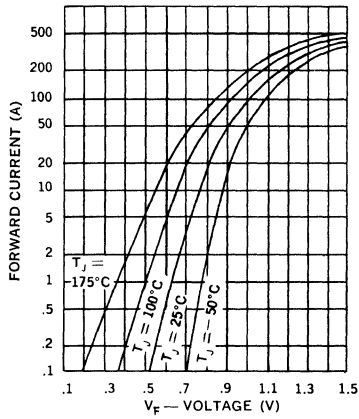
Square Pulse Current vs. Duration for Non-Repetition Square Wave



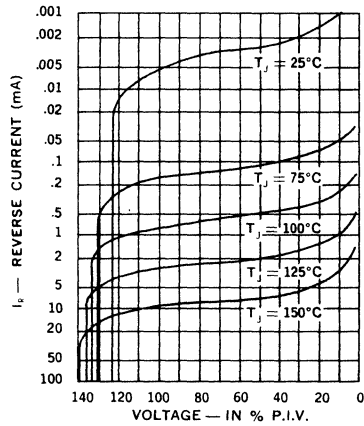
Multiple Surge Current vs. Duration



Typical Forward Current vs. Forward Voltage

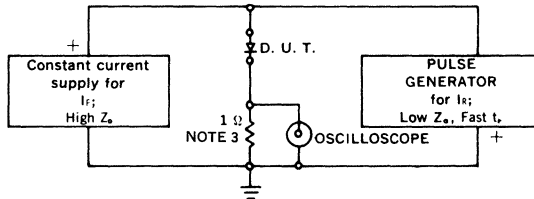


Typical Reverse Current vs. Voltage



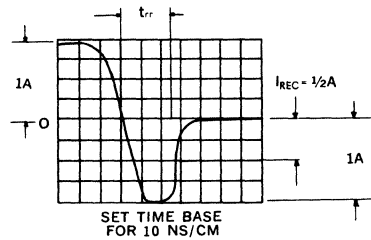
6

Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time $\leq 3\ \text{ns}$; input impedance = $50\ \Omega$.
 - Pulse Generator: Rise time $\leq 8\ \text{ns}$; source impedance $10\ \Omega$.
 - Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform



RECTIFIERS

High Efficiency, 25 A

UES701-UES703

FEATURES

- Low Forward Voltage
- Very Fast Switching
- Low Thermal Resistance
- High Surge Capability
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

Designed to meet the efficiency demand of switching type power supplies, these devices are useful in many switching applications.

The low thermal resistance and forward voltage drop of this series allows the user to replace DO-5 size devices in many applications.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES701	50V
Peak Inverse Voltage, UES702	100V
Peak Inverse Voltage, UES703	150V
Maximum Average D.C. Output Current at $T_C = 100^\circ\text{C}$	25A
Non-Repetitive Sinusoidal Surge Current at 8.3ms	400A
Thermal Resistance, Junction to Case	1.5°C/W
Operating and Storage Temperature Range	-55°C to +175°C

POWER CYCLING

These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C, at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

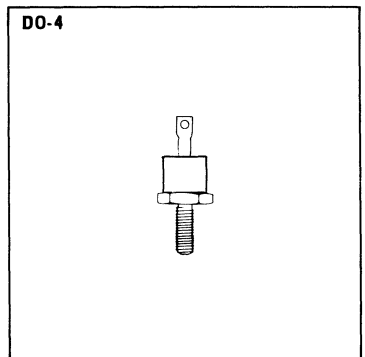
SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS

UES701-UES703

	ins.	mm
A	.078 MAX	1.98 MAX
B	437 ± 015	11.10 ± 0.38
C	405 MAX	10.29 MAX.
D	800 MAX	20.32 MAX.
E	430 ± 010	10.92 ± 0.25
F	250 MAX	6.35 MAX
G	424 MAX	10.77 MAX.
H	066 MIN DIA	1.68 MIN. DIA.



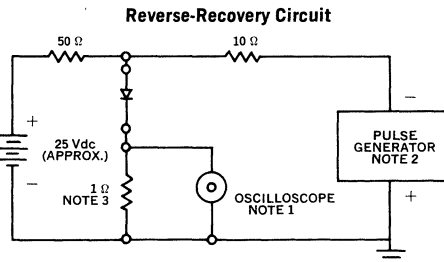
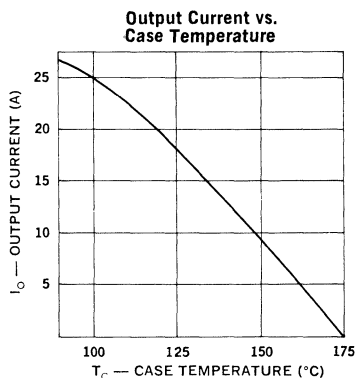
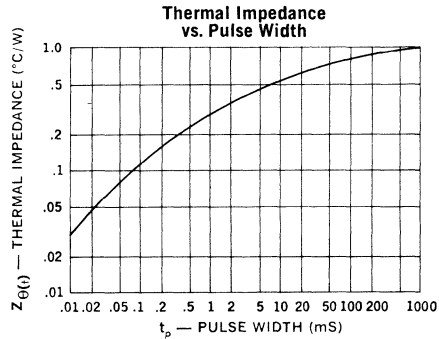
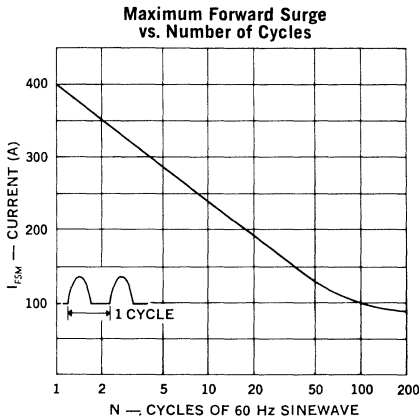
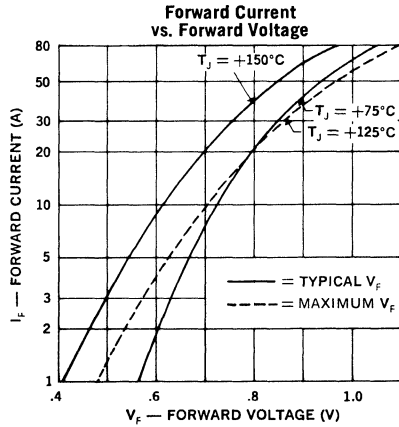
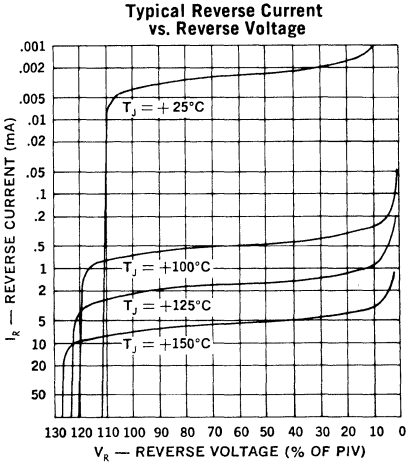
Notes:

1. Standard polarity is cathode-to-stud.
For reverse Polarity (anode-to-stud) add suffix "R", ie. UES701R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 15 inch pounds.
4. Angular orientation of terminal is undefined.

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		T _C = 25°C	T _C = 125°C	T _C = 25°C	T _C = 125°C	
UES701	50V	.950	.825	20μA	4mA	35nS
UES702	100V	@	@			
UES703	150V	25A t _p = 300μS	25A t _p = 300μS			

* Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A



- NOTES:**
- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
 - Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 20A

UES704-UES706

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- Low Thermal Resistance
- High Surge Capability
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

The UES704 series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

The low thermal resistance and forward voltage drop of this series allows the user to replace DO-5 size devices in many applications.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES704	200V
Peak Inverse Voltage, UES705	300V
Peak Inverse Voltage, UES706	400V
Ave. D.C. Output Current, I_o @ $T_c = 100^\circ\text{C}$	20A
Surge Current, 8.3mSec	300A
Thermal Resistance, Junction to Case	1.5°C/W
Operating and Storage Temperature Range	-55°C to +150°C

POWER CYCLING

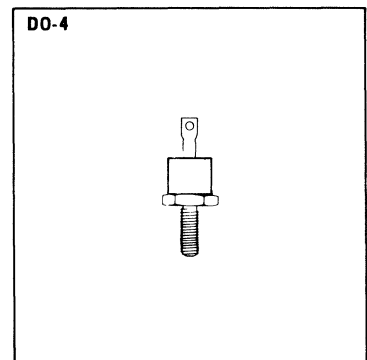
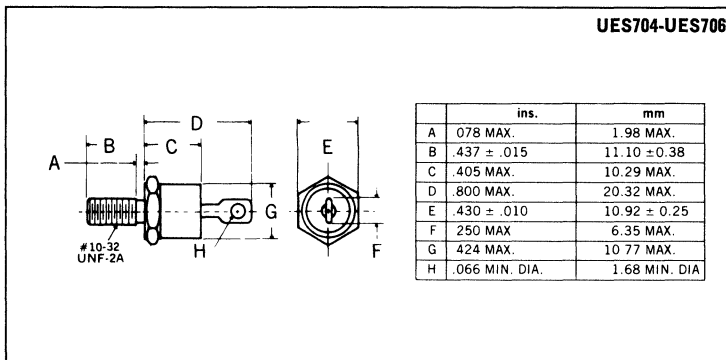
These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C, at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS



Notes:

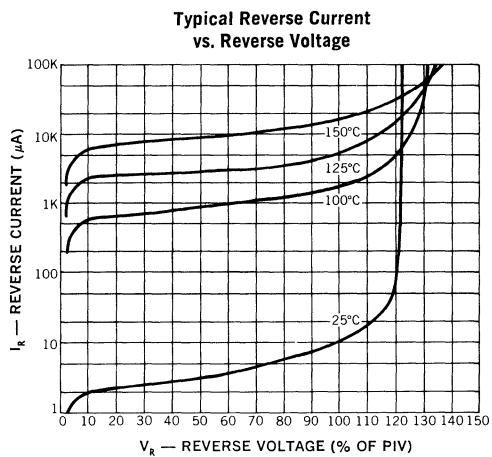
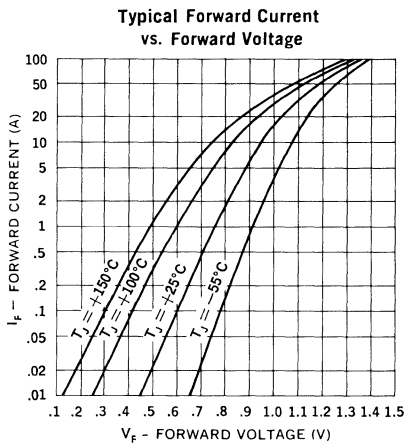
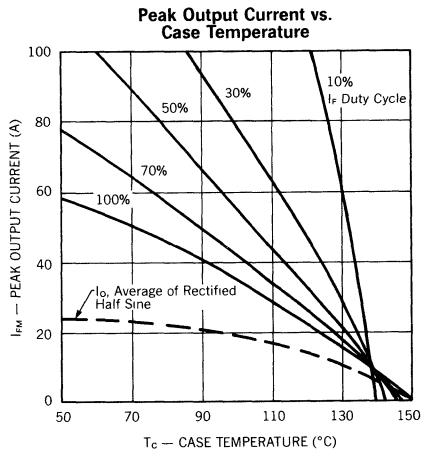
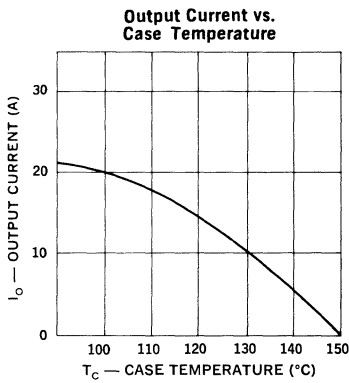
1. Standard polarity is cathode-to-stud.
For reverse Polarity (anode-to-stud) add suffix "R", ie. UES704R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 15 inch pounds.
4. Angular orientation of terminal is undefined.

ELECTRICAL SPECIFICATIONS

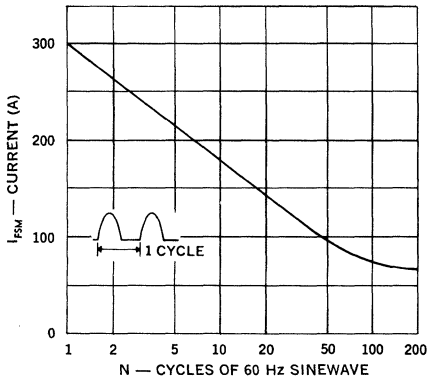
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		T _C = 25°C	T _C = 125°C	T _C = 25°C	T _C = 125°C	
UES704	200V	1.25V	1.15V	50μA	10mA	50nS
UES705	300V	@ 20A	@ 20A			
UES706	400V	t _p = 300μS	t _p = 300μS			

* Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A

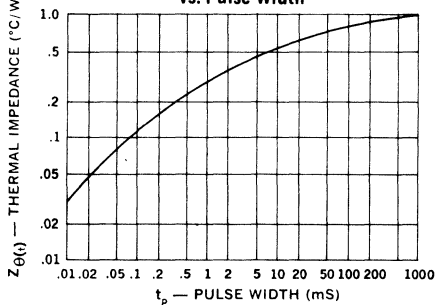
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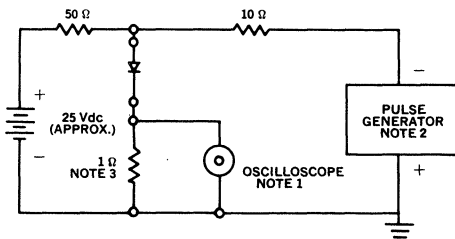
Maximum Forward Surge vs. Number of Cycles



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 70 Amp

UES801-UES803

FEATURES

- High Continuous Current Rating
- Very Low Forward Voltage
- Very Fast Switching Speeds
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available
- Available with Flexible Top Lead

DESCRIPTION

The UES801 Series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES801	50V
Peak Inverse Voltage, UES802	100V
Peak Inverse Voltage, UES803	150V
Maximum Average D.C. Output Current at $T_C = 100^\circ\text{C}$	70A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	800A
Thermal Resistance, Junction to Case	0.8°C/W
Operating and Storage Temperature Range	-55°C to +175°C

POWER CYCLING

These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C, at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

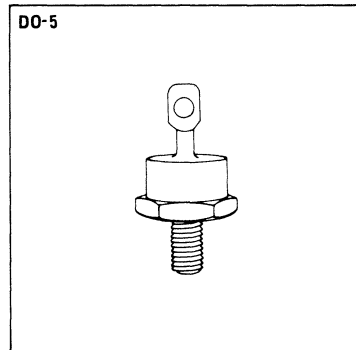
SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS

UES801-UES803

	ins.	mm
A	225 ± .005	5.72 ± 0.13
B	060 MIN	1.52 MIN
C	156 ± .020	3.96 ± 0.51
D	156 MIN FLAT	3.96 MIN FLAT
E	667 DIA MAX	16.94 DIA MAX
F	090 MAX	2.29 MAX
G	677 ± .010	17.20 ± 0.25
H	375 MAX	9.53 MAX
J	140 MIN DIA	3.56 MIN DIA
K	1 000 MAX	25.40 MAX
L	450 MAX	11.43 MAX
M	438 ± .015	11.13 ± 0.38
N	078 MAX	1.98 MAX



Notes:

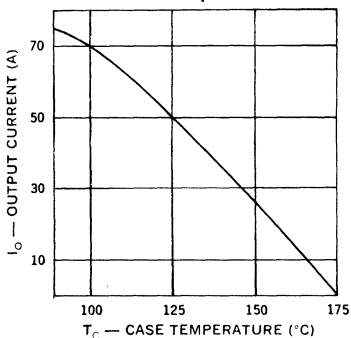
1. Standard polarity is cathode-to-stud.
For reverse polarity (anode-to-stud) add suffix "R", ie. UES801R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 20 inch pounds (20 kg. cm).
4. Angular orientation of terminal is undefined.

ELECTRICAL SPECIFICATIONS

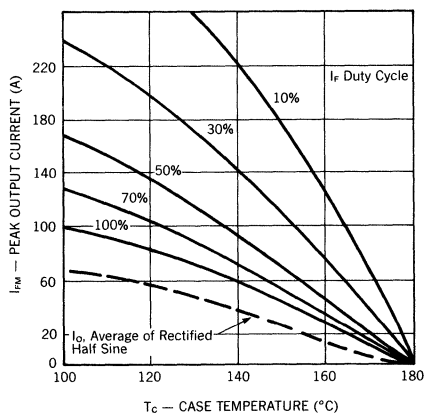
Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		T _C = 25°C	T _C = 150°C	T _C = 25°C	T _C = 150°C	
UES801 UES802 UES803	50V 100V 150V	.975V @ 70A t _p = 300μS	.840V @ 70A t _p = 300μS	25μA	30mA	50nS

Note: Add 0.03 Volts to Max Forward Voltage for Flexible Top Lead Option. * Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A

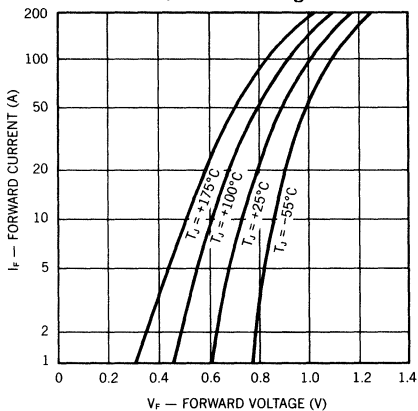
Output Current vs. Case Temperature



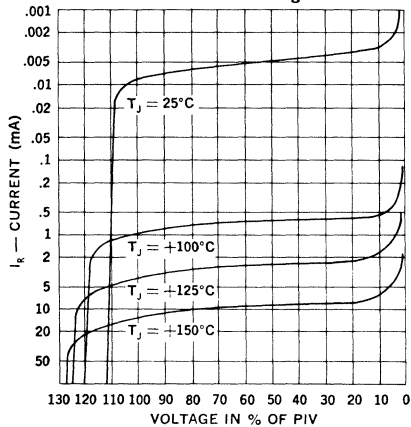
Peak Output Current vs. Case Temperature



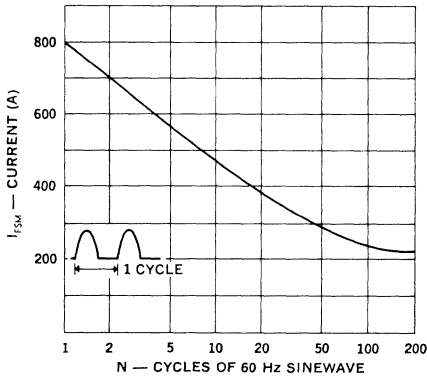
Forward Current vs. Forward Voltage



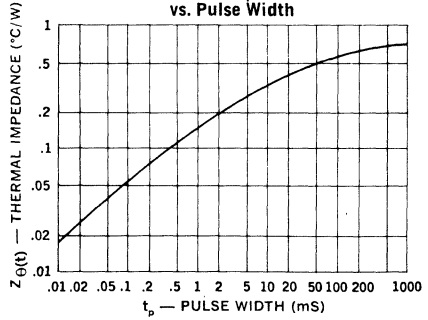
Typical Reverse Current vs. Reverse Voltage



Maximum Forward Surge vs. Number of Cycles

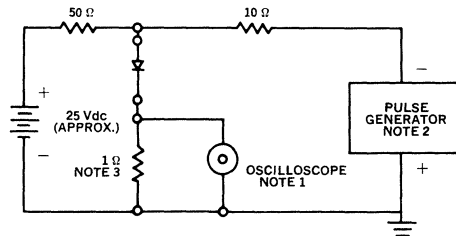


Thermal Impedance vs. Pulse Width



6

Reverse-Recovery Circuit

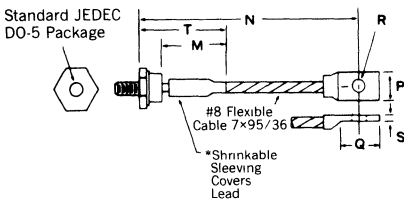


NOTES:

1. Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

MECHANICAL SPECIFICATIONS

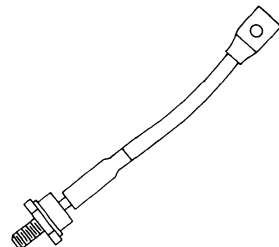
FLEXIBLE TOP LEAD (OPTIONAL)
Add an "F" Suffix to Part Number.



	INCHES	MILLIMETERS
M	.718 MAX.	18.24 MAX.
N	4.50 ± .250	114.3 ± 6.35
P	.525 MAX.	13.23 MAX.
Q	.675 ± .035	17.15 ± 0.89
R	.205 ± .005	5.21 ± 0.13
S	.075 ± .010	1.91 ± 0.25
T	1.125 MAX.	28.58 MAX.

*To 125°C (Ambient)

DO-5 with Flexible Lead



RECTIFIERS

High Efficiency, 50A

UES804-UES806

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

The UES804 is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES804	200V
Peak Inverse Voltage, UES805	300V
Peak Inverse Voltage, UES806	400V
Maximum Average D.C. Output Current @ $T_C = 100^\circ\text{C}$	50A
Surge Current, 8.3mSec	600A
Thermal Resistance, Junction to Case8°C/W
Operating and Storage Temperature Range	-55°C to +150°C

POWER CYCLING

These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C, at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

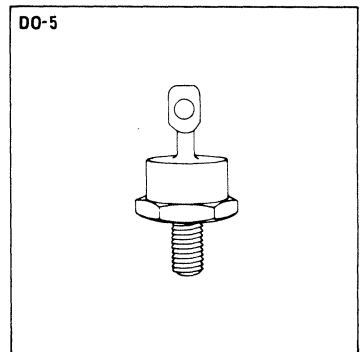
SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS

UES804-UES806

	ins.	mm
A	225 ± 005	5 72 ± 0 13
B	060 MIN	1 52 MIN.
C	156 ± 020	3 96 ± 0 51
D	156 MIN FLAT	3 96 MIN. FLAT
E	667 DIA. MAX	16 94 DIA. MAX
F	090 MAX	2 29 MAX
G	677 ± 010	17 20 ± 0 25
H	375 MAX	9 53 MAX
J	140 MIN. DIA.	3 56 MIN. DIA.
K	1 000 MAX	25 40 MAX
L	450 MAX	11 43 MAX
M	438 ± 015	11 13 ± 0 38
N	078 MAX	1 98 MAX



Notes:

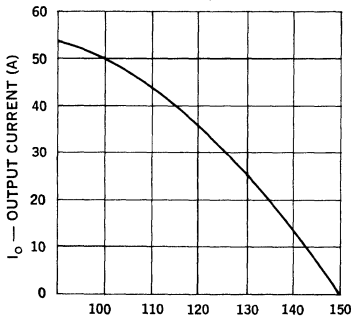
1. Standard polarity is cathode-to-stud.
For reverse polarity (anode-to-stud) add suffix "R", ie. UES804R.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds.
4. Angular orientation of terminal is undefined.

ELECTRICAL SPECIFICATIONS

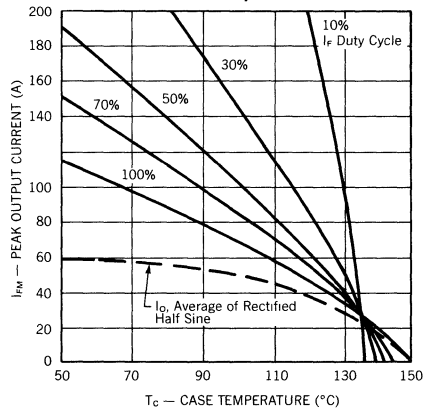
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		T _c = 25°C	T _c = 125°C	T _c = 25°C	T _c = 125°C	
UES804	200V	1.25V	1.15V	70μA	30mA	50nS
UES805	300V	@ I _F = 50A	@ I _F = 50A			
UES806	400V	t _p = 300μS	t _p = 300μS			

* Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A

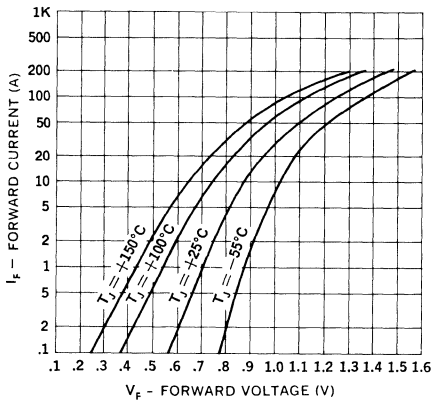
Output Current vs. Case Temperature



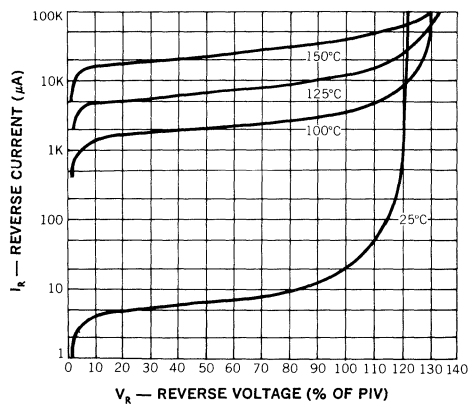
Peak Output Current vs. Case Temperature



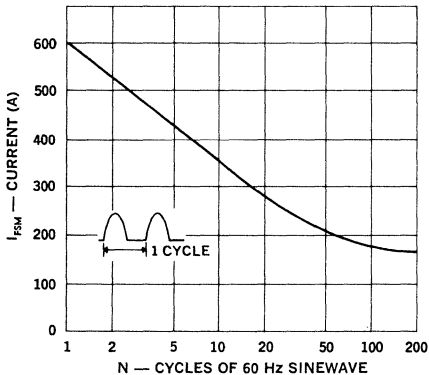
Typical Forward Current vs. Forward Voltage



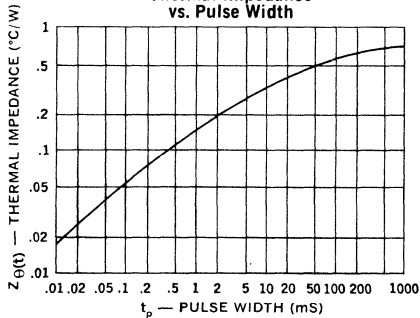
Typical Reverse Current vs. Reverse Voltage



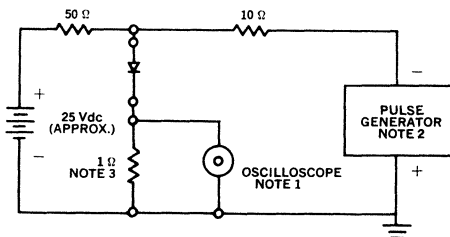
Maximum Forward Surge vs. Number of Cycles



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω .
2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 1A

UES1001-UES1003

FEATURES

- Very Fast Recovery Times
- Very Low Forward Voltage
- Small Size
- Convenient Package

DESCRIPTION

An axial leaded power rectifier useful in many switching applications. Particularly suited where very fast recovery and low forward voltage are required.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1001	50V
Peak Inverse Voltage, UES1002	100V
Peak Inverse Voltage, UES1003	150V
Maximum Average D.C. Output Current at $T_L = 75^\circ\text{C}$, $L = 3/8"$	1A
Non-Repetitive Surge Current at 8.3ms	30A
Thermal Resistance at $L = 3/8"$	$.75^\circ\text{C/W}$
Operating and Storage Temperature Range	$-55^\circ\text{C} + 175^\circ\text{C}$

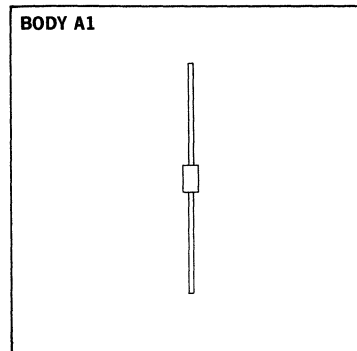
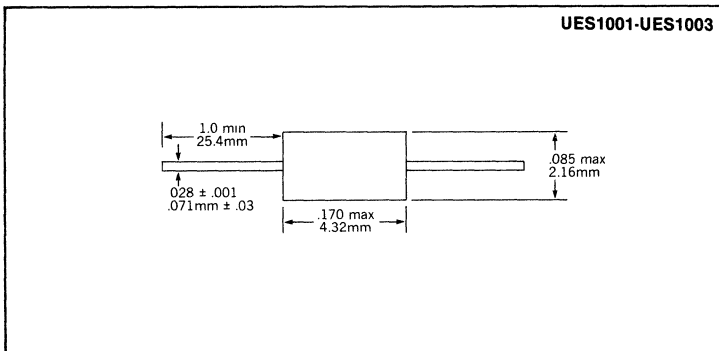
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ELECTRICAL SPECIFICATIONS

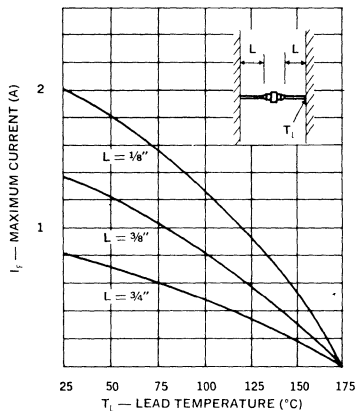
Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$	
UES1001	50V	.975V	.895V			
UES1002	100V	@	@	$2\mu\text{A}$	$50\mu\text{A}$.25nS
UES1003	150V	1A	1A			

*Measured in circuit $I_F = .5\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = .25\text{A}$

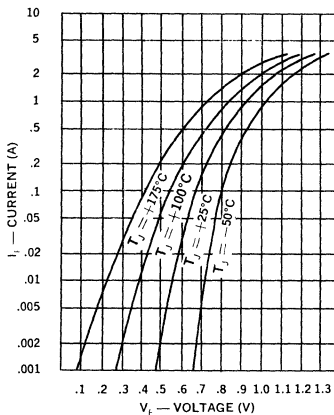
MECHANICAL SPECIFICATIONS



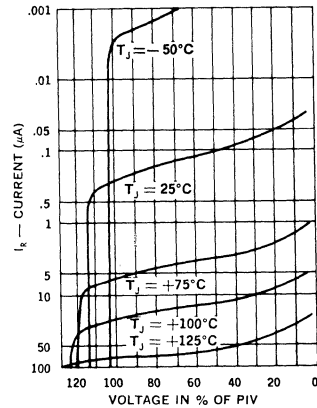
Output Current vs. Lead Temperature



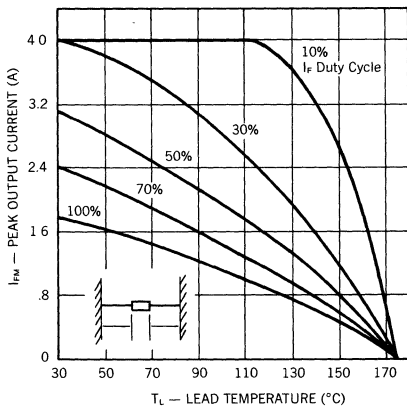
Typical Forward Current vs. Forward Voltage



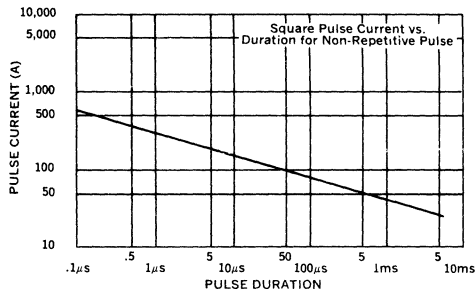
Typical Reverse Current vs. Voltage



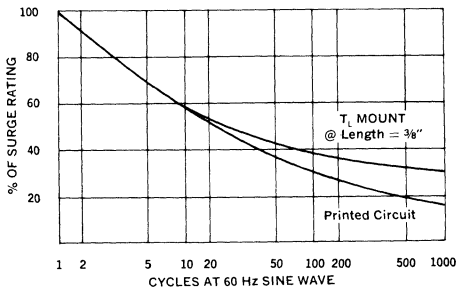
Peak Output Current vs. Lead Temperature



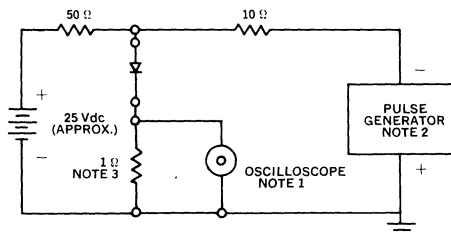
Forward Pulse Current vs. Duration



Multiple Surge Current vs. Duration



Reverse-Recovery Circuit



- NOTES:**
1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = $50\Omega</math>.$
 2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance $10\Omega</math>.$
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 2.5A

UES1101-UES1103

FEATURES

- Very Fast Recovery Times
- Very Low Forward Voltage
- Small Size
- Convenient Package

DESCRIPTION

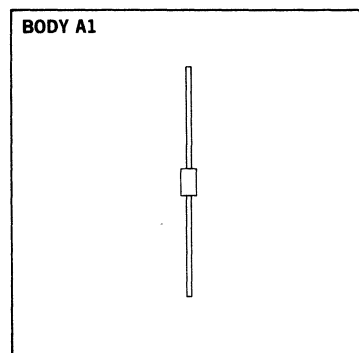
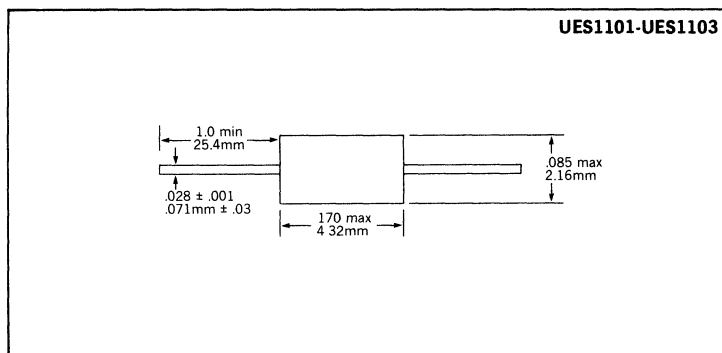
An axial leaded power rectifier useful in many switching applications. Particularly suited where very fast recovery and low forward voltage are required.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1101	50V
Peak Inverse Voltage, UES1102	100V
Peak Inverse Voltage, UES1103	150V
Maximum Average D.C. Output Current at $T_L = 75^\circ\text{C}$, $L = \frac{3}{8}"$	2.5A
Non-Repetitive Surge Current at 8.3 ms	35A
Thermal Resistance at $L = \frac{3}{8}"$	38°C/W
Operating and Storage Temperature Range	-55°C +175°C

MECHANICAL SPECIFICATIONS

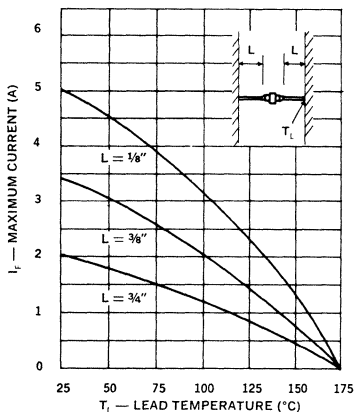


ELECTRICAL SPECIFICATIONS

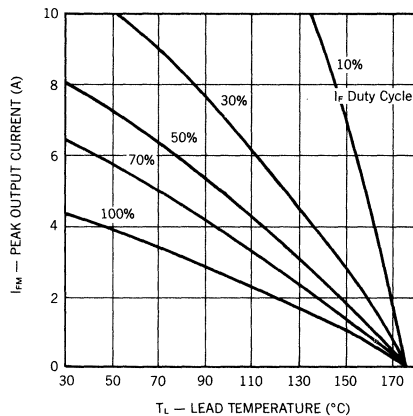
Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		T _J = 25°C	T _J = 100°C	T _J = 25°C	T _J = 100°C	
UES1101	50V	.975V @ 2A	.895V @ 2A	2μA	50μA	25nS
UES1102	100V					
UES1103	150V	tp = 300μS	tp = 300μS			

* Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A

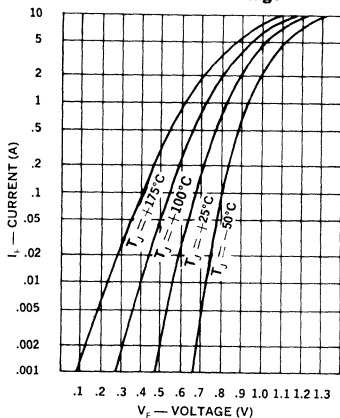
Output Current vs. Lead Temperature



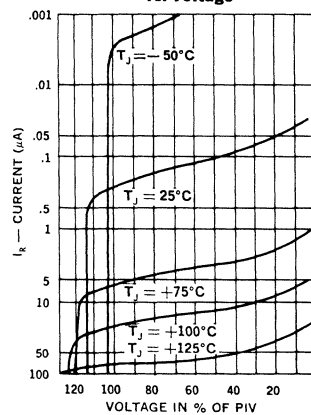
Peak Output Current vs. Lead Temperature



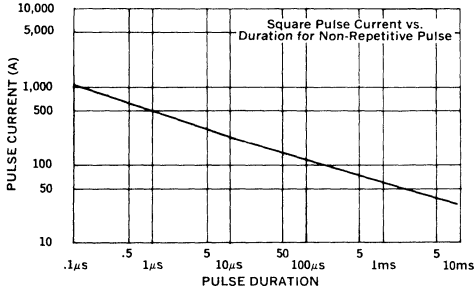
Typical Forward Current vs. Forward Voltage



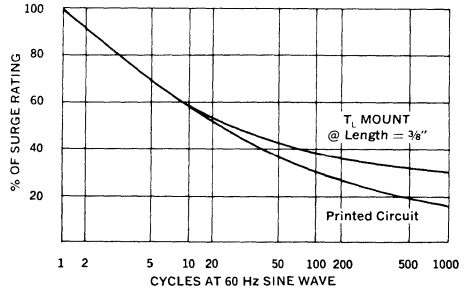
Typical Reverse Current vs. Voltage



Forward Pulse Current vs. Duration

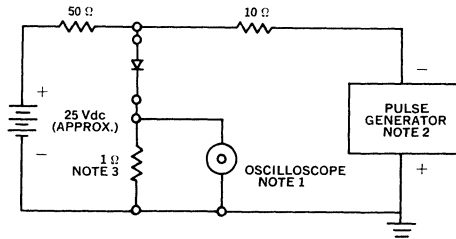


Multiple Surge Current vs. Duration



6

Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω .
2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 2A

UES1104-UES1106

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- Small Size
- Convenient Package

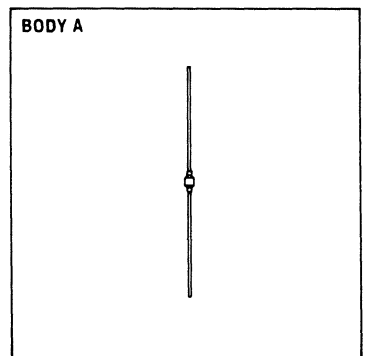
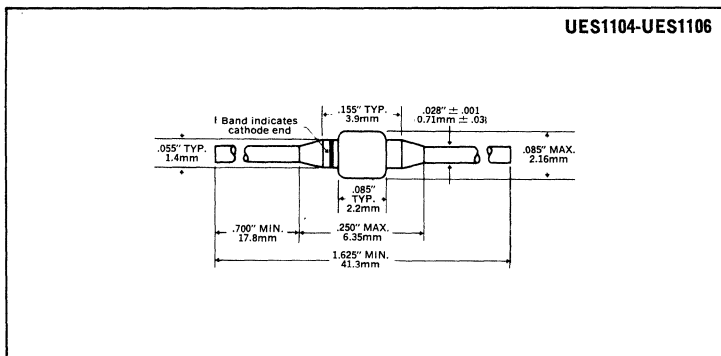
DESCRIPTION

The UES1104 series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1104	200V
Peak Inverse Voltage, UES1105	300V
Peak Inverse Voltage, UES1106	400V
Maximum Average D.C. Output Current, I_o	
@ $T_A = 25^\circ\text{C}$ (Free Air)	1A
@ $T_L = 50^\circ\text{C}$, $L = \frac{3}{16}"$	2A
Surge Current, 8.3mSec	20A
Thermal Resistance @ $L = \frac{3}{16}"$	38°C/W
Operating and Storage Temperature Range	-55°C to +150°C

MECHANICAL SPECIFICATIONS

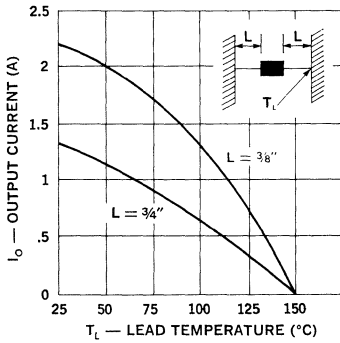


ELECTRICAL SPECIFICATIONS

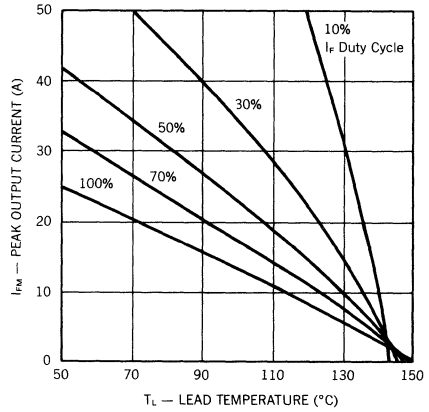
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ PIV, $T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	
UES1104	200V	1.25V @ 1A	1.15V @ 1A	10 μA	200 μA	50nS
UES1105	300V					
UES1106	400V	$t_p = 300\mu\text{S}$	$t_p = 300\mu\text{S}$			

* Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1\text{A}$, $I_{REC} = 0.25\text{A}$

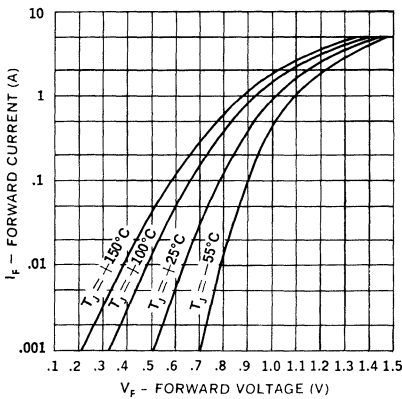
Output Current vs. Lead Temperature



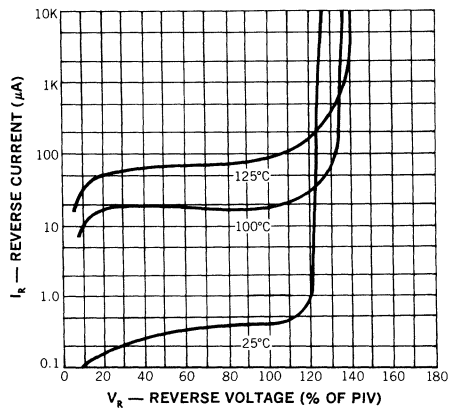
Peak Output Current vs. Lead Temperature



Typical Forward Current vs. Forward Voltage

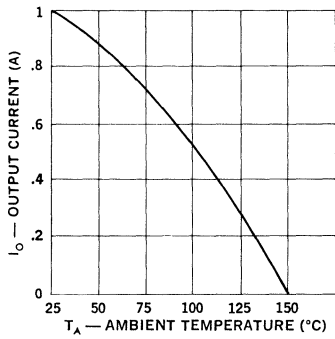


Typical Reverse Current vs. Reverse Voltage

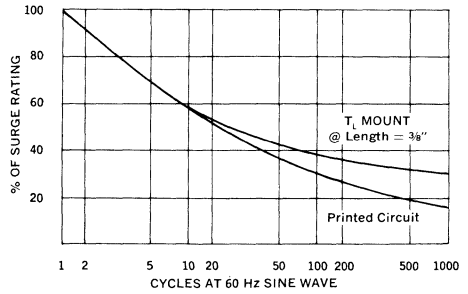


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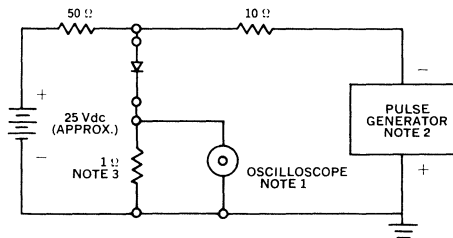
Output Current vs. Ambient Temperature.



Multiple Surge Current vs. Duration



Reverse-Recovery Circuit



- NOTES:**
1. Oscilloscope: Rise time ≤ 3 ns; input impedance $\approx 50\Omega$.
 2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω .
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 6A

UES1301-UES1303

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Small Size
- High Surge

DESCRIPTION

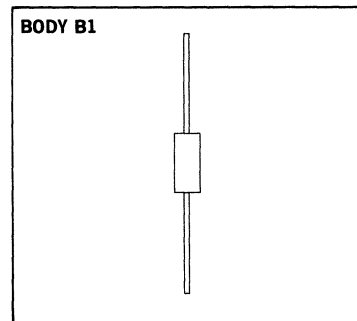
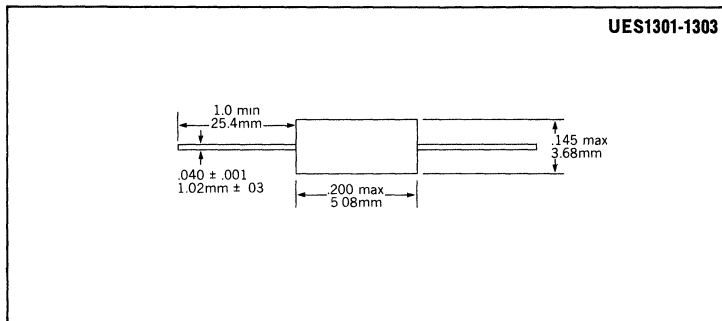
Now power rectifiers in axial leaded package to meet the most demanding switching applications. An industrial product with military reliability.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1301	50V
Peak Inverse Voltage, UES1302	100V
Peak Inverse Voltage, UES1303	150V
Maximum Average D.C. Output Current at $T_L = 75^\circ\text{C}$, $L = \frac{3}{8}"$	6.0A
Non-Repetitive Sinusoidal Surge Current at 8.3ms	125A
Thermal Resistance at $L = \frac{3}{8}"$	20°C/W
Operating and Storage Temperature Range	-55°C to +175°C

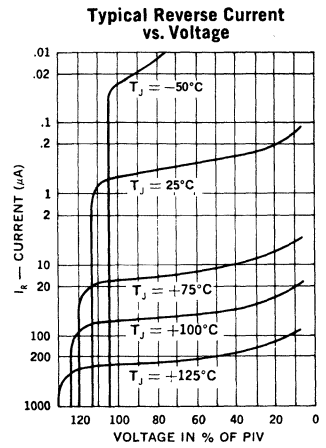
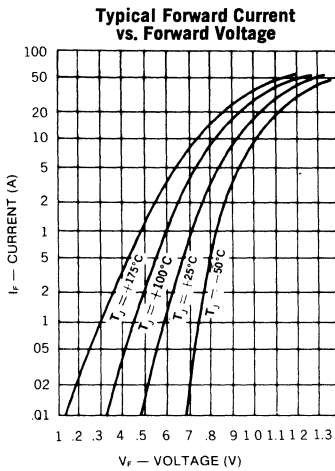
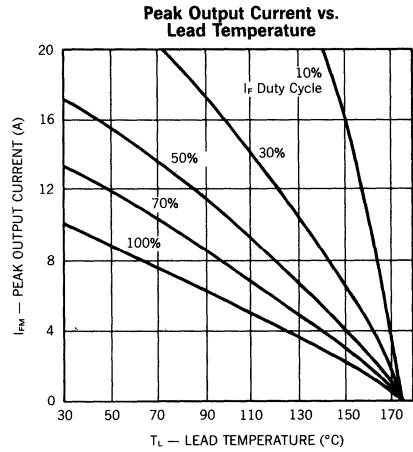
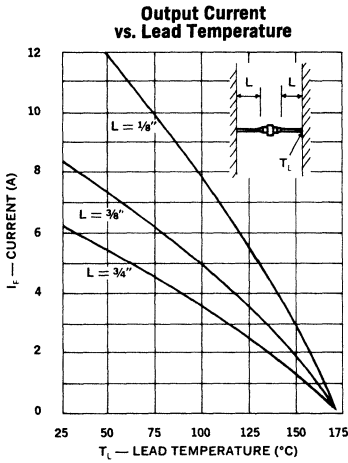
MECHANICAL SPECIFICATIONS



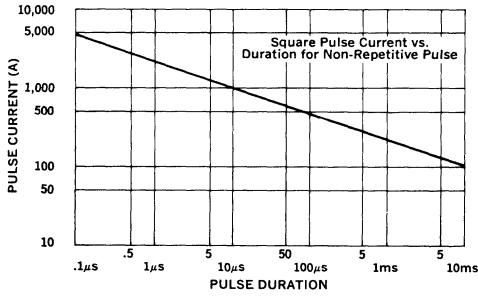
ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		T _J = 25°C	T _J = 100°C	T _J = 25°C	T _J = 100°C	
UES1301	50V	.925V	.850V	5μA	150μA	30nS
UES1302	100V	@ 6A	@ 6A			
UES1303	150V	tp = 300μS	tp = 300μS			

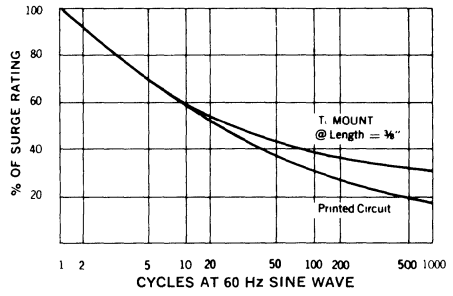
* Measured in circuit I_F = 0.5A, I_R = 1A, I_{REC} = 0.25A



Forward Pulse Current vs. Duration

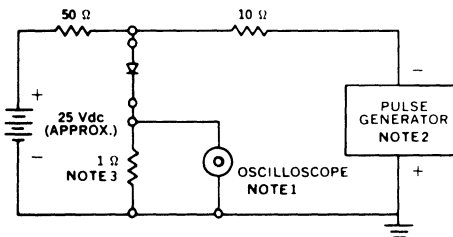


Multiple Surge Current vs. Duration



6

Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 5A

UES1304–UES1306

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- Small Size
- High Surge

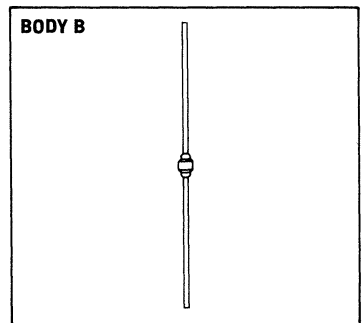
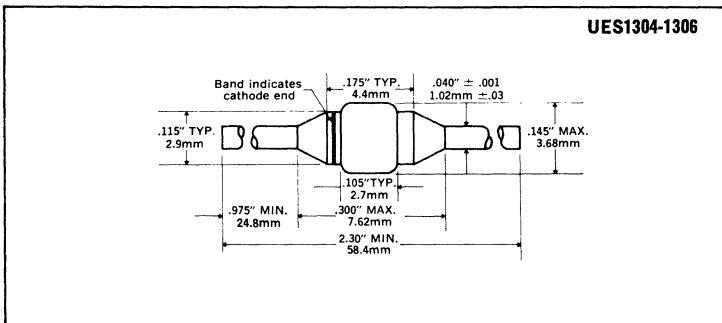
DESCRIPTION

The UES1304 series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1304	200V
Peak Inverse Voltage, UES1305	300V
Peak Inverse Voltage, UES1306	400V
Maximum Average D.C. Output Current, I_o	
@ $T_A = 25^\circ\text{C}$ (Free Air)	3A
@ $T_L = 50^\circ\text{C}$, $L = \frac{3}{8}"$	5A
Surge Current, 8.3mSec	70A
Thermal Resistance @ $L = \frac{3}{8}"$	20°C/W
Operating and Storage Temperature Range	-55°C to +150°C

MECHANICAL SPECIFICATIONS

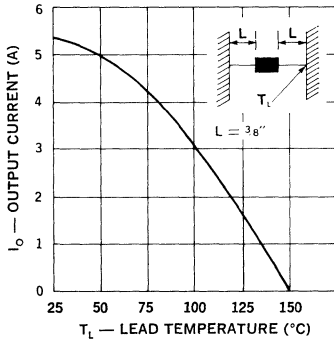


ELECTRICAL SPECIFICATIONS

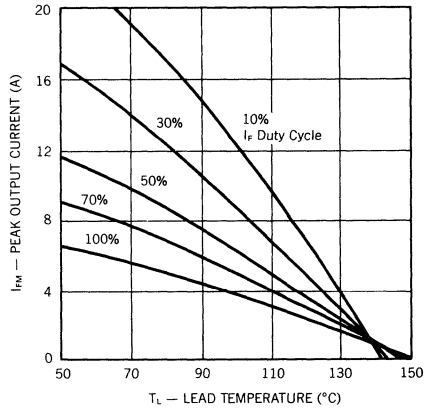
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ PIV, $T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	
UES1304	200V	1.25V	1.15V	$20\mu\text{A}$	$500\mu\text{A}$	50nS
UES1305	300V	@ 3A	@ 3A			
UES1306	400V	$t_p = 300\mu\text{S}$	$t_p = 300\mu\text{S}$			

* Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1\text{A}$, $I_{REC} = 0.25\text{A}$

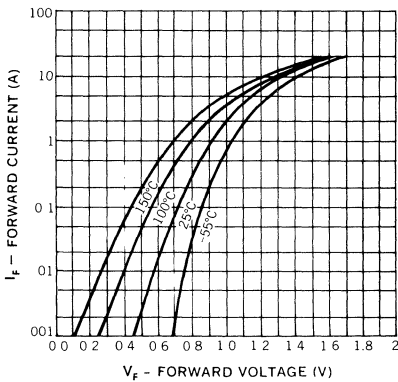
Output Current vs. Lead Temperature



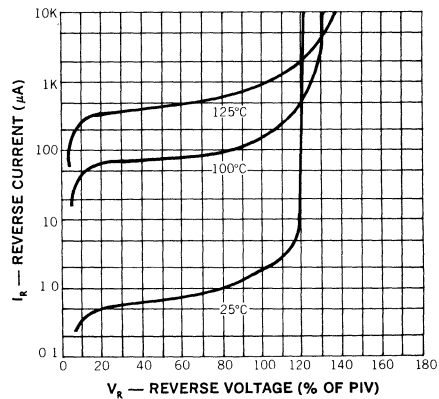
Peak Output Current vs. Lead Temperature



Typical Forward Current vs. Forward Voltage

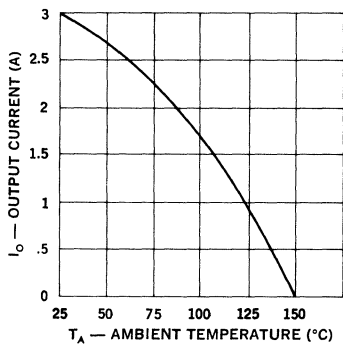


Typical Reverse Current vs. Reverse Voltage

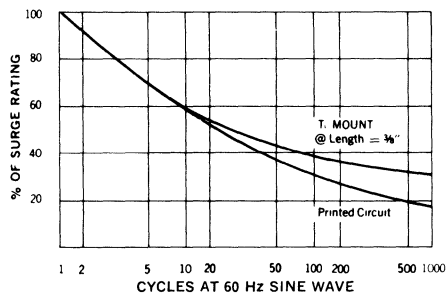


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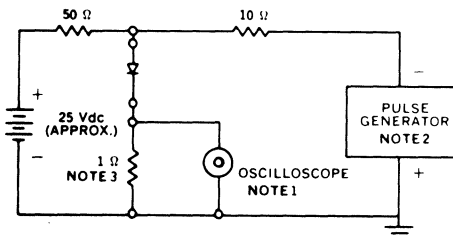
**Output Current vs
Ambient Temperature**



Multiple Surge Current vs. Duration



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 8A

UES1401-UES1404

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Economical, Convenient Plastic Package
- Low Thermal Resistance
- Mechanically Rugged
- PIV up to 200V

DESCRIPTION

The UES1401 Series, in a plastic package similar to the TO-220, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

6

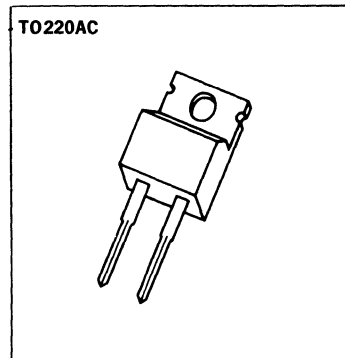
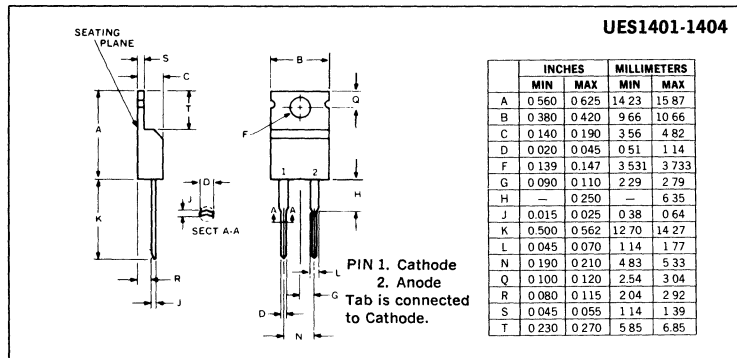
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1401	50V
Peak Inverse Voltage, UES1402	100V
Peak Inverse Voltage, UES1403	150V
Peak Inverse Voltage, UES1404	200V
Maximum Average D.C. Output Current	
@ $T_C = 125^\circ\text{C}$ (Note 1)	8.0A
@ $T_A = 25^\circ\text{C}$	3.0A
@ $T_A = 25^\circ\text{C}$ (Note 2)	8.0A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	80A
Thermal Resistance, Junction to Case, θ_{J-C}	2.5°C/W
Thermal Resistance, Junction to Ambient, θ_{J-A}	60°C/W
Operating and Storage Temperature Range	-55°C to +150°C

Note 1. Above 100°C use the tab for electrical connection.

Note 2. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

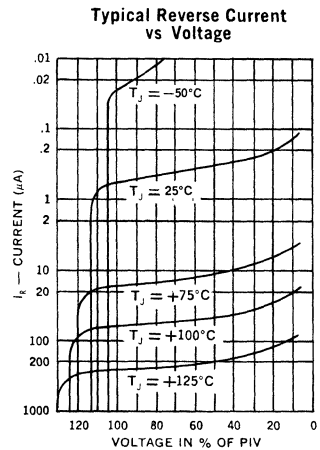
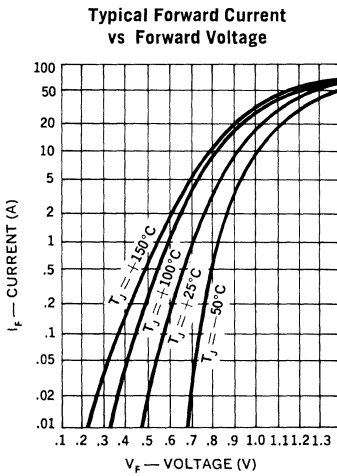
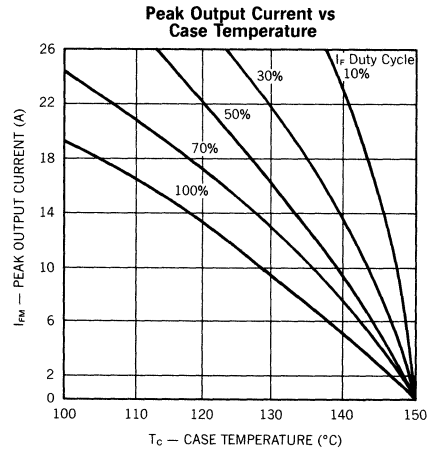
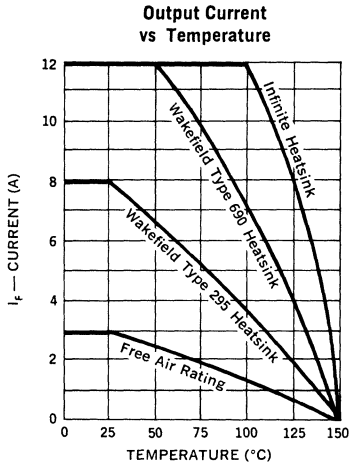
MECHANICAL SPECIFICATIONS



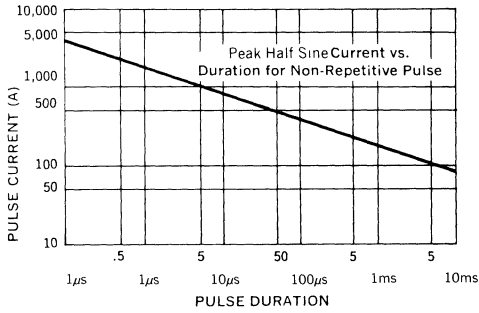
ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8\text{ns}$
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$		
UES1401	50V	0.9V@ 4A	0.8V @ 4A	5 μA	150 μA	35ns	1.4V
UES1402	100V	0.975 @ 8A	0.895 @ 8A		150 μA		
UES1403	150V	0.975 @ 8A $t_p = 300\mu\text{s}$	0.895 @ 8A		150 μA		
UES1404	200V				500 μA		

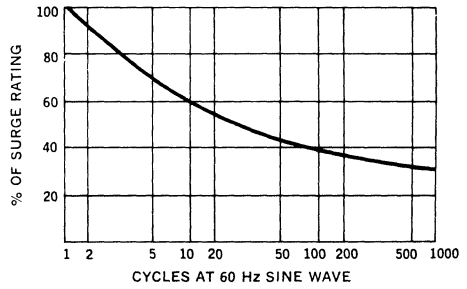
*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = 0.25\text{A}$



Forward Pulse Current vs Duration

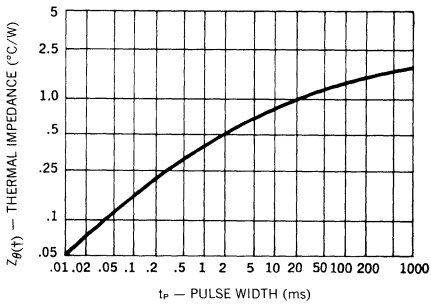


Multiple Surge Current vs Duration

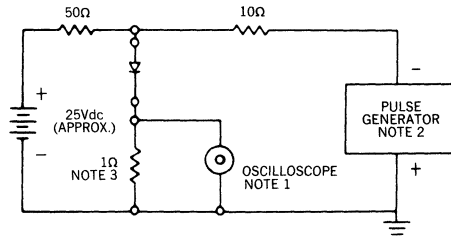


6

Thermal Impedance vs Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50 Ω .
2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 16A

UES1501
UES1502
UES1503
UES1504

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Economical, Convenient TO-220 Package
- Low Thermal Resistance
- Mechanically Rugged

DESCRIPTION

The UES1500 Series, in the economical, convenient TO-220 package, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The very low forward voltage and very fast recovery time make them particularly suited for switching type power supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES1501	50V
Peak Inverse Voltage, UES1502	100V
Peak Inverse Voltage, UES1503	150V
Peak Inverse Voltage, UES1504	200V
Maximum Average D.C. Output Current	
@ $T_C = 100^\circ\text{C}$	16A
@ $T_A = 25^\circ\text{C}$	3.3A
@ $T_A = 25^\circ\text{C}$ (Note 1)	10.0A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	300A
Thermal Resistance, Junction to Case, θ_{j-c}	1.5°C/W
Thermal Resistance, Junction to Ambient, θ_{j-a}	60°C/W
Operating and Storage Temperature	-55°C to +150°C

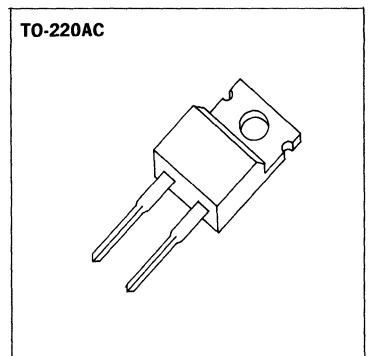
Note: 1. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs Temperature Curve on this data sheet.

MECHANICAL SPECIFICATIONS

UES1501-UES1504

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

PIN 1. Cathode
PIN 2. Anode
Tab is connected to Cathode.

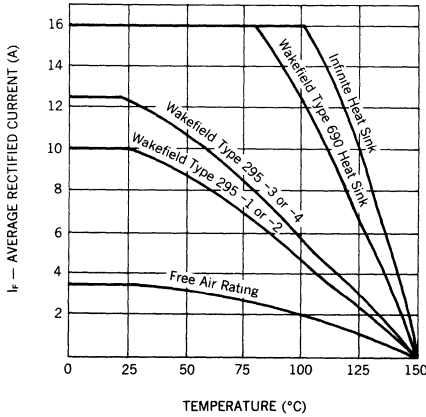


ELECTRICAL SPECIFICATIONS

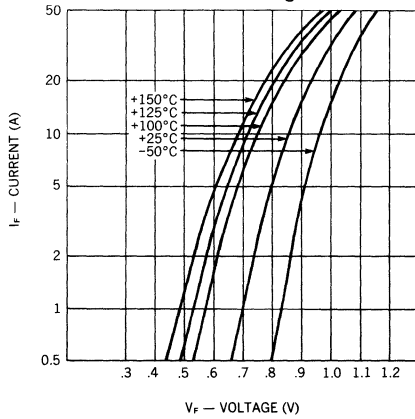
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8\text{ns}$
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$		
UES1501	50V	.975V @ 16A	.895V @ 16A	10 μA	800 μA	35ns	2.0V
UES1502	100V						
UES1503	150V						
UES1504	200V	1.10V @ 32A	1.0V @ 32A				

* Measured in circuit $I_F = 1/2\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = 1/4\text{A}$

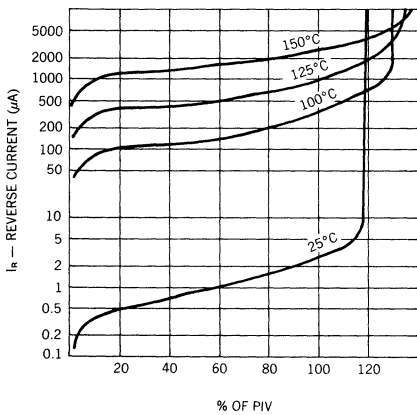
Output Current vs Temperature



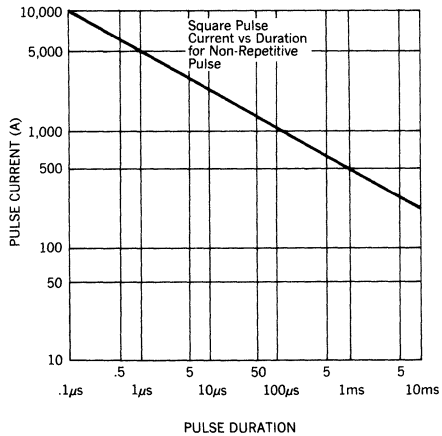
Typical Forward Current vs Forward Voltage



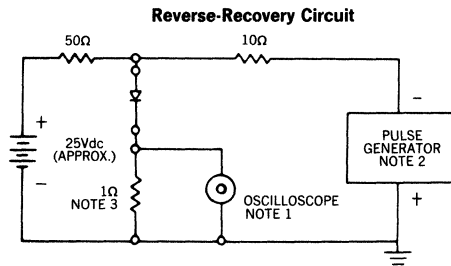
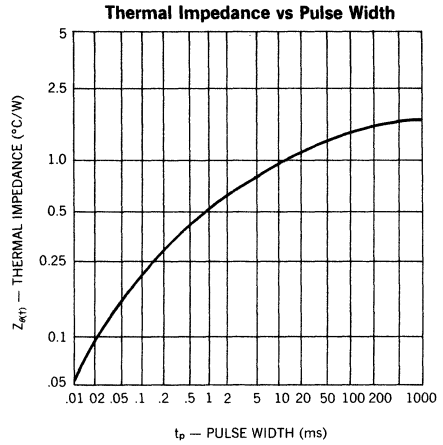
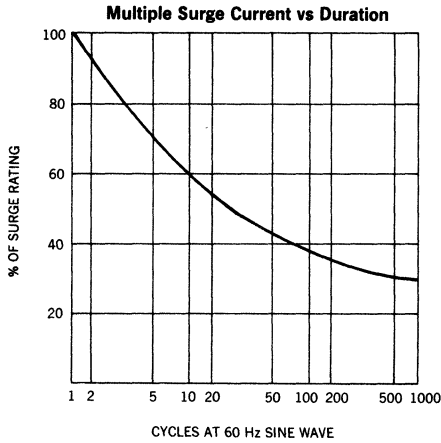
Typical Reverse Current vs Voltage



Forward Pulse Current vs Duration



6



- NOTES:**
1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω .
 2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10Ω .
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 16A Center-Tap

UES2401-UES2404

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Economical, Convenient TO-220AB Package
- Low Thermal Resistance
- Mechanically Rugged
- PIV up to 200V

DESCRIPTION

The UES2401 Series in the economical, convenient TO-220AB package, is specifically designed for operation in power switching circuits to frequencies in excess of 100kHz. The series combines two high efficiency devices into one package, simplifying installation, reducing heatsink requirements and the need to purchase matched components.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2401	50V
Peak Inverse Voltage, UES2402	100V
Peak Inverse Voltage, UES2403	150V
Peak Inverse Voltage, UES2404	200V
Maximum Average D.C. Output Current	
@ $T_c = 125^\circ\text{C}$ (Note 1)	16A
@ $T_A = 25^\circ\text{C}$	3A
@ $T_A = 25^\circ\text{C}$ (Note 2)	10A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	80A
Thermal Resistance, Junction to Case, θ_{j-c}	1.75°C/W
Thermal Resistance, Junction to Ambient, θ_{j-a}	60°C/W
Operating and Storage Temperature Range	-55°C to +150°C

Note 1. Above 8A use the tab for electrical connection.

Note 2. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

MECHANICAL SPECIFICATIONS

UES2401-2404

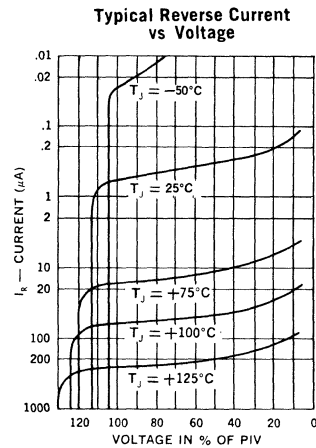
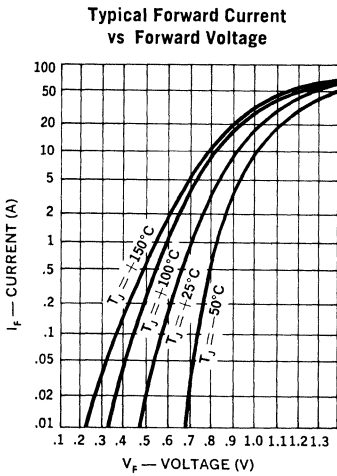
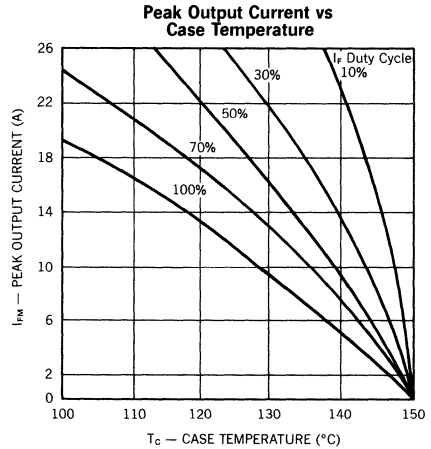
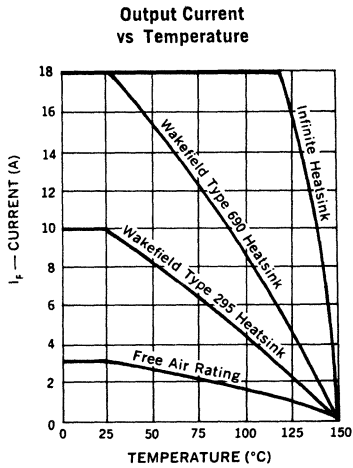
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

TO-220AB

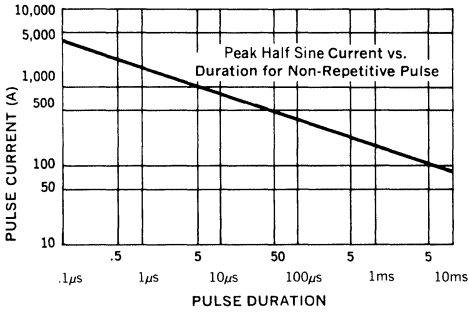
ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8ns$
		$T_J = 25^\circ C$	$T_J = 100^\circ C$	$T_J = 25^\circ C$	$T_J = 100^\circ C$		
UES2401	50V	0.9V @ 4A	0.8V @ 4A	5 μ A	150 μ A	35ns	1.4V
UES2402	100V	0.975 @ 8A	0.895 @ 8A		150 μ A		
UES2403	150V				150 μ A		
UES2404	200V	$t_p = 300\mu s$			500 μ A		

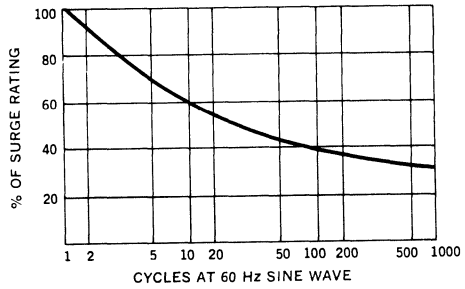
*Measured in circuit $I_F = 0.5A$, $I_R = 1.0A$, $I_{REC} = 0.25A$



Forward Pulse Current vs Duration

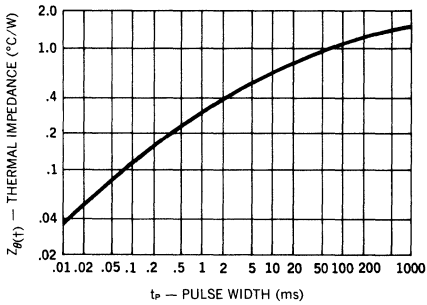


Multiple Surge Current vs Duration

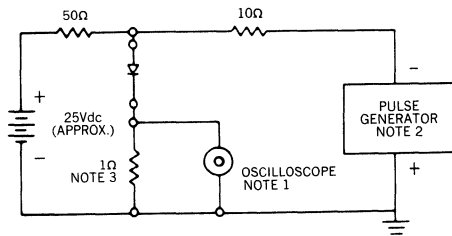


6

Thermal Impedance vs Pulse Width



Reverse-Recovery Circuit



- NOTES:**
1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω.
 2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω.
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 30A Center-Tap

UES2601-UES2603

FEATURES

- Very Low Forward Voltage
- Very Fast Switching Speed
- Convenient Package
- High Surge
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

This series combines two high efficiency devices into one package, simplifying installation, reducing heat sink requirements and the need to purchase matched components.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2601	50V
Peak Inverse Voltage, UES2602	100V
Peak Inverse Voltage, UES2603	150V
Maximum Average D.C. Output Current at $T_c = 100^\circ\text{C}$	30A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	400A
Thermal Resistance, Junction to Case	1°C/W
Operating and Storage Temperature Range	-55°C to $+175^\circ\text{C}$

POWER CYCLING

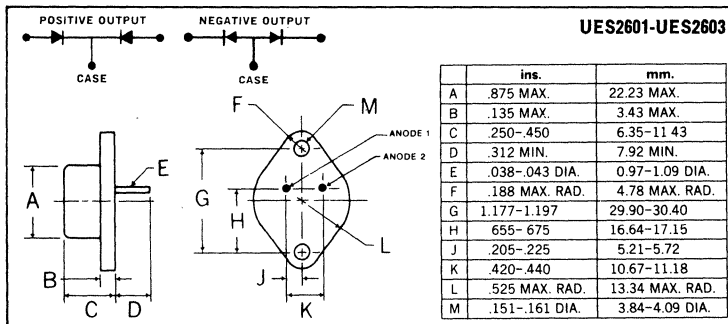
These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C , at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

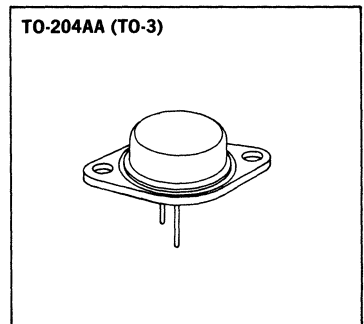
MECHANICAL SPECIFICATIONS



Note:

Standard polarity is positive output.

For reverse polarity (negative output) add suffix "R", ie. UES2601R.

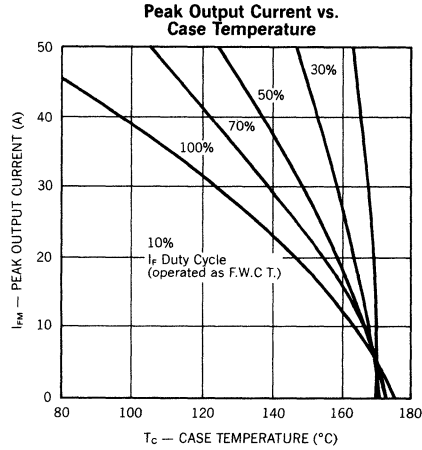
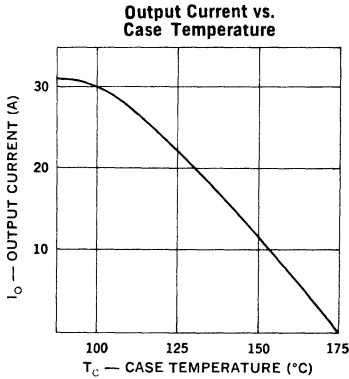


ELECTRICAL SPECIFICATIONS

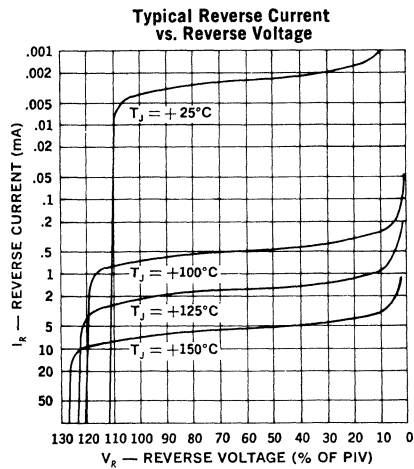
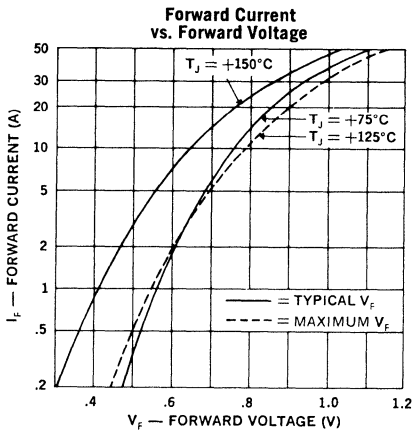
UES2601- UES2603

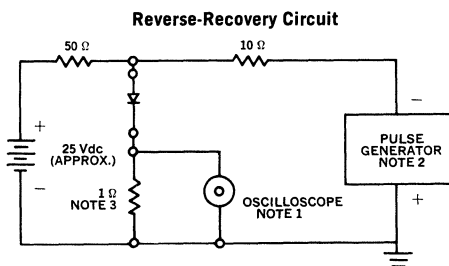
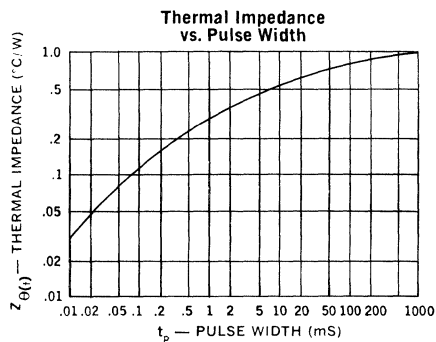
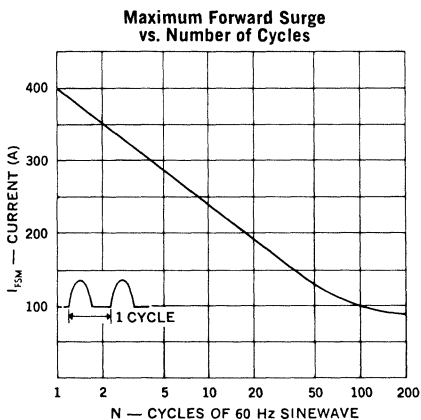
Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		$T_c = 25^\circ\text{C}$	$T_c = 125^\circ\text{C}$	$T_c = 25^\circ\text{C}$	$T_c = 125^\circ\text{C}$	
UES2601 UES2602 UES2603	50V 100V 150V	.930V @ 15A $t_p = 300\mu\text{S}$.825V @ 15A $t_p = 300\mu\text{S}$	$20\mu\text{A}$	4mA	35nS

* Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1\text{A}$, $I_{REC} = 0.25\text{A}$



6





- NOTES:**
1. Oscilloscope; Rise time ≤ 3 ns; input impedance = 50Ω .
 2. Pulse Generator; Rise time ≤ 8 ns; source impedance 10Ω .
 3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 30A Center-Tap

UES2604-UES2606

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- Low Profile Package
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

The UES2604 series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

This series combines two high efficiency devices into one package, simplifying installation, reducing heat sink requirements and the need to purchase matched components.

6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2604	200V
Peak Inverse Voltage, UES2605	300V
Peak Inverse Voltage, UES2606	400V
Maximum Average D.C. Output Current @ $T_c = 100^\circ\text{C}$	30A
Surge Current, 8.3mSec	300A
Thermal Resistance, Junction to Case	1°C/W
Operating and Storage Temperature Range	-55°C to $+150^\circ\text{C}$

POWER CYCLING

These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C , at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

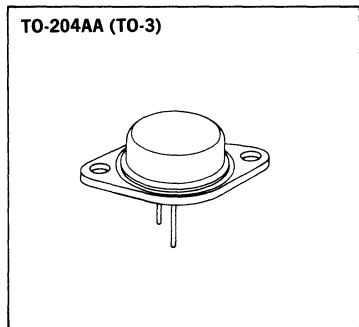
SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS

UES2604-UES2606

	ins.	mm.
A	875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	205-225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX. RAD.	13.34 MAX. RAD.
M	151-161 DIA.	3.84-4.09 DIA.



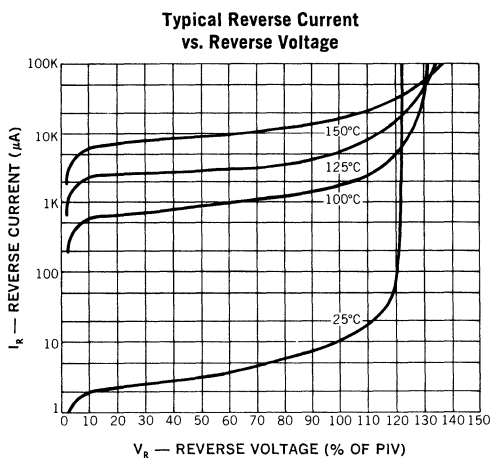
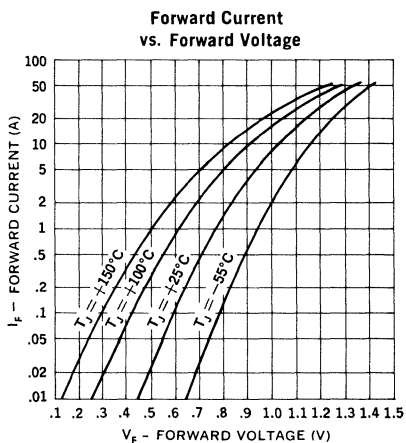
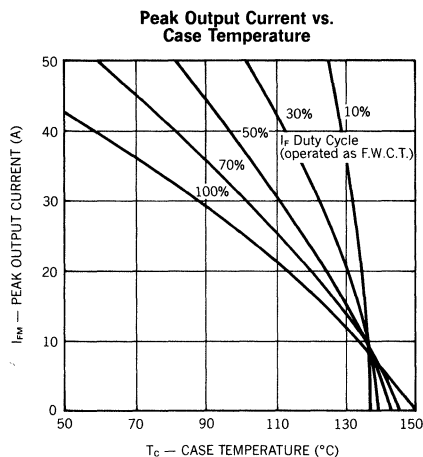
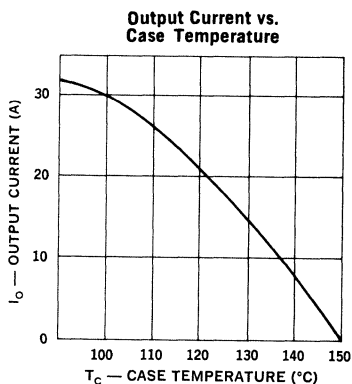
Note:

Standard polarity is positive output.
For reverse polarity (negative output) add suffix "R", ie. UES2604R.

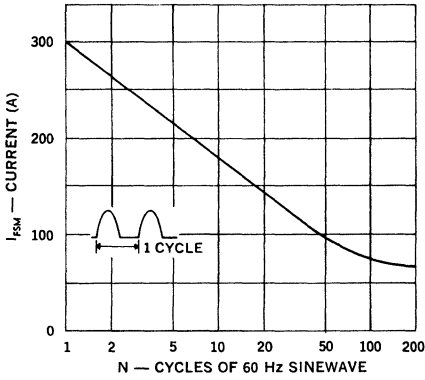
ELECTRICAL SPECIFICATIONS, PER LEG

Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		T _c = 25°C	T _c = 125°C	T _c = 25°C	T _c = 125°C	
UES2604	200V	1.25V	1.15V	50μA	10mA	50nS
UES2605	300V	@ 15A	@ 15A			
UES2606	400V	t _p = 300μS	t _p = 300μS			

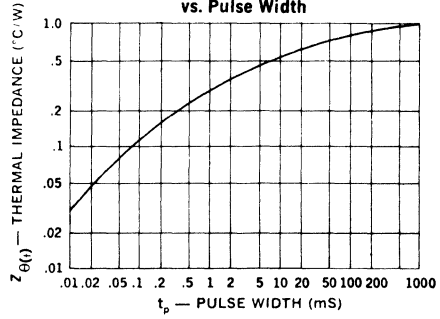
*Measured in circuit I_F = .5A, I_R = 1A, I_{REC} = .25A



Maximum Forward Surge vs. Number of Cycles

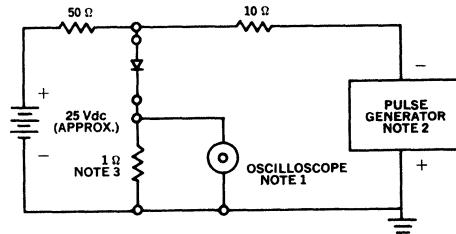


Thermal Impedance vs. Pulse Width



6

Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
2. Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

Radiation Tolerant, 1 Amp-2 Amp

UR105-UR125
UR205-UR225

FEATURES

- Radiation Tolerant: to 10^{16} NVT
- Continuous Rating: to 2A
- Controlled Avalanche
- Surge Rating: to 25A
- Miniature Package

DESCRIPTION

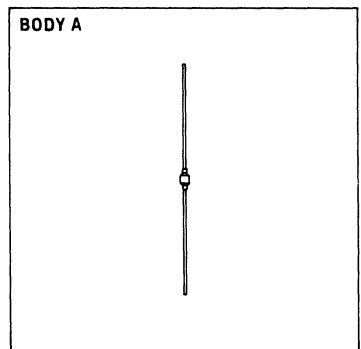
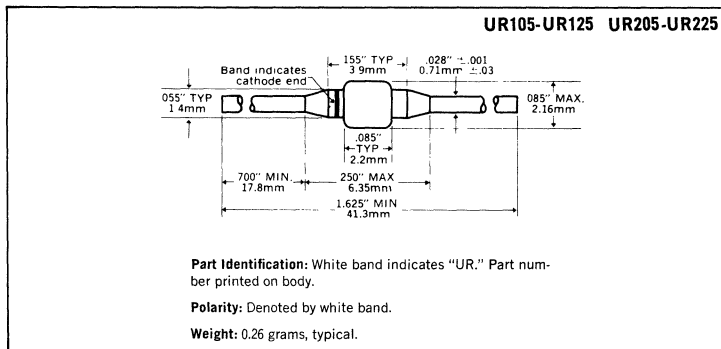
These devices are particularly suited to applications where radiation is present. These units have unique ability to withstand high levels of neutron, gamma and electron radiation.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	1 Amp Series	2 Amp Series
50V	UR105	UR205
100V	UR110	UR210
150V	UR115	UR215
200V	UR120	UR220
250V	UR125	UR225

	1 AMP SERIES	2 AMP SERIES
Maximum Average D.C. Output Current		
@ $T_A = 25^\circ\text{C}$	1A	2A
@ $T_A = 100^\circ\text{C}$	0.5A	1A
Non-Repetitive Sinusoidal		
Surge Current (8.3ms)	20A	25A
Operating Temperature Range	-195°C to +175°C	
Storage Temperature Range	-195°C to +200°C	
Thermal Resistance	See Lead Temperature Derating Curve	

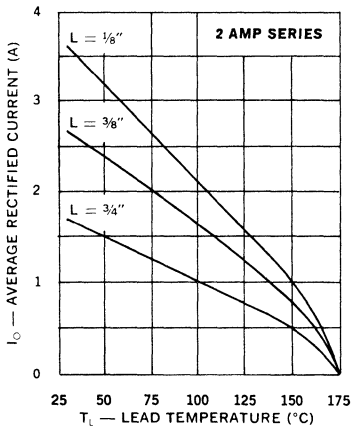
MECHANICAL SPECIFICATIONS



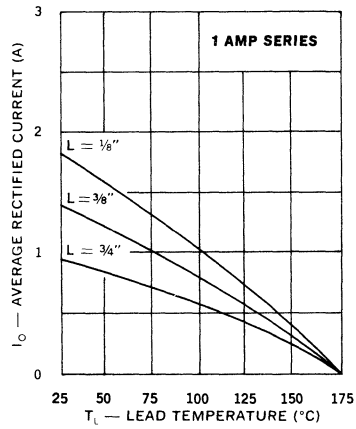
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV		Maximum Radiation Tolerance
			25°C	100°C	
UR205 UR210 UR215 UR220 UR225	50V 100V 150V 200V 250V	1.0V @ 1A	3μA	50μA	10 ¹⁶ NVT 10 ¹⁶ 10 ¹⁵ 10 ¹⁴ 10 ¹⁴
UR105 UR110 UR115 UR120 UR125	50V 100V 150V 200V 250V	1.0V @ 0.5A	3μA	50μA	10 ¹⁶ 10 ¹⁶ 10 ¹⁵ 10 ¹⁴ 10 ¹⁴

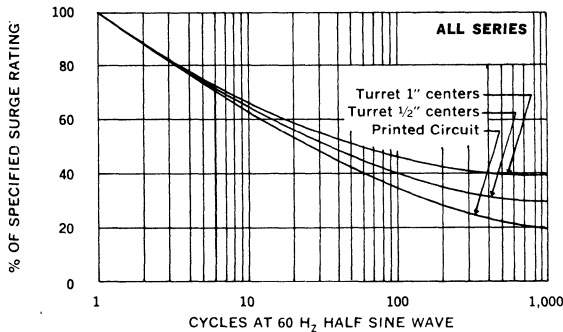
Maximum Current vs Lead Temperature



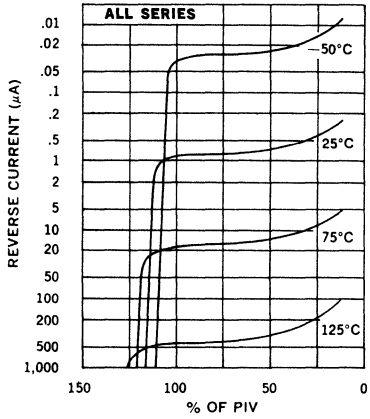
Maximum Current vs Lead Temperature



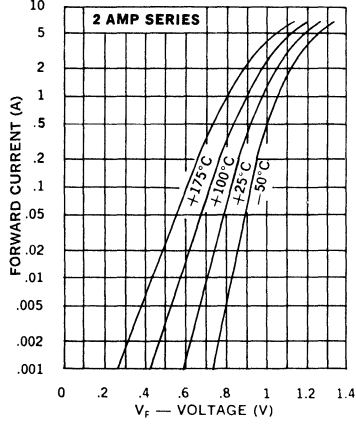
Allowable Forward Surge vs Number of Cycles



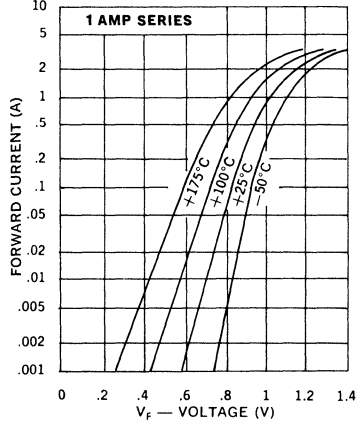
Typical Reverse Current vs PIV



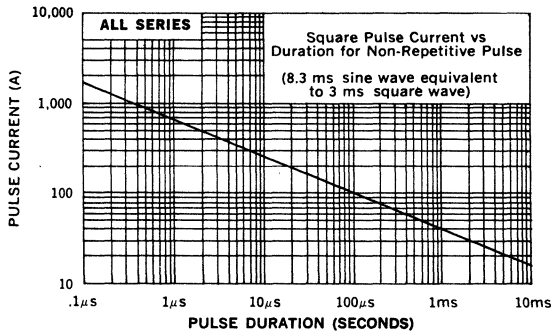
Typical Forward Current vs Forward Voltage



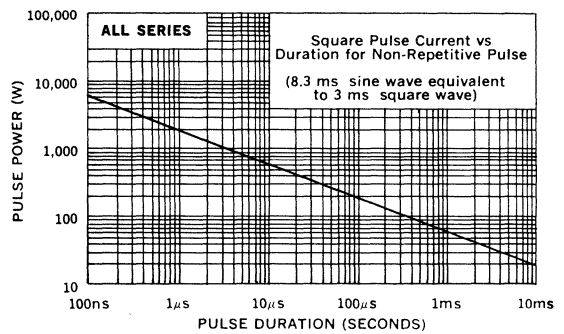
Typical Forward Current vs Forward Voltage



Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



DUAL POWER SCHOTTKY RECTIFIERS

60A Pk, 45V

USD320C
USD335C
USD345C

FEATURES

- Very Low Forward Voltage
- Low Recovered Charge
- Rugged Package Design (TO-3)
- High Efficiency for Low Voltage Supplies
- 45V Blocking @ Rated T_{jmax}
- 50V Repetitive Surge Voltage
- Dual Schottky Rectifier in a Single Package

DESCRIPTION

The USD300C series has two Schottky barriers arranged in a common cathode configuration and is ideally suited for a full wave output rectifier in low voltage switching power supplies.

ABSOLUTE MAXIMUM RATINGS (Total for USD300C Series)

Average Rectified Forward Current, I_o @ $T_c = 100^\circ\text{C}$ 30A

USD320C

USD335C

USD345C

ABSOLUTE MAXIMUM RATINGS (Per Diode)

Working Peak Reverse Voltage V_{RWM} 20V 35V 45V
 DC Blocking Voltage, V_R 20V 35V 45V
 Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM} 24V 42V 54V
 Average Rectified Forward Current, I_o 30A in full wave configuration*
 Non-repetitive Peak
 Surge current (8.3 mS), I_{FSM} 500A
 Peak Reverse Transient Current, I_{RM} 2A
 Storage Temperature Range, T_{stg} -55°C to $+200^\circ\text{C}$.
 Peak Operating Junction Temperature, T_{jmax} 175°C
 Thermal Resistance, Junction to Case, R_{jC} 1.4°C/W

* Each Anode Pin Limited to 18A Average.
 Package Capability 30A Average

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$)

Characteristic	Symbol	Limit	Units	Conditions
Maximum Instantaneous Reverse Current	i_R	10	mA	$T_c = 25^\circ\text{C}$, $V_R = V_{RWM}$ $T_c = 125^\circ\text{C}$ Pulse Width = $400\mu\text{S}$ Duty Cycle = 1 percent
		50	mA	
Maximum Instantaneous Forward Voltage	V_F	0.57	V	$i_F = 10\text{A}$, $T_c = 25^\circ\text{C}$ $i_F = 20\text{A}$, $T_c = 25^\circ\text{C}$ $i_F = 20\text{A}$, $T_c = 125^\circ\text{C}$ Pulse Width = $300\mu\text{S}$ Duty Cycle = 1 percent
		0.66	V	
		0.60	V	
Capacitance	C_t	2000	pF	$V_R = 5.0\text{V}$
Voltage Rate of Change	dv/dt	1000	$v/\mu\text{S}$	$V_R = V_{RWM}$

MECHANICAL SPECIFICATIONS

NOTE:
 Leads may be soldered to within $1/16"$ of base provided temperature-time exposure is less than 260°C for 10 seconds.

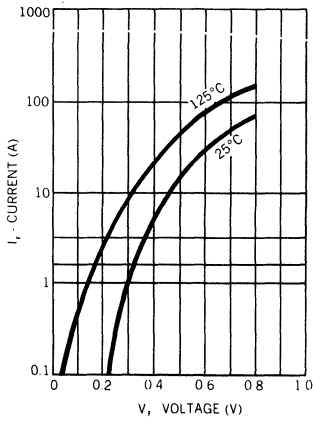
ANODE 2 → ANODE 1
 CASE (CATHODE)

	ins.	mm.
A	875 MAX.	22.23 MAX.
B	135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038- .043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	655-675	16.64-17.15
J	.205-.225	5.21-5.72
K	420-440	10.67-11.18
L	525 MAX. RAD	13.34 MAX. RAD
M	.151-.161 DIA.	3.84-4.09 DIA.

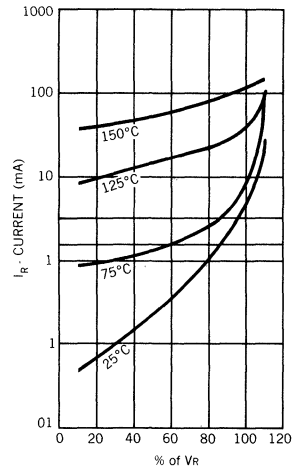
TO-204AA (TO-3)

Notes: All metal surfaces tin plated.

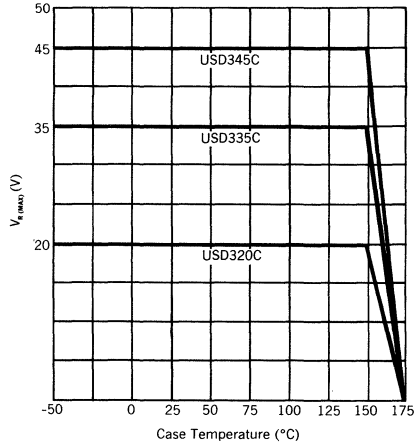
Typical Forward Current vs. Forward Voltage



Typical Reverse Current vs. Reverse Voltage



V_{R(max)} Rating vs. Case Temperature



POWER SCHOTTKY RECTIFIERS

150 Amp Pk, Up to 45V

USD520
USD535
USD545
USD550

FEATURES

- Very Low Forward Voltage (0.6V at 60A, 125°C)
- Low Recovered Charge
- Rugged Package Design (DO-5)
- High Efficiency for Low Voltage Supplies
- Low Thermal Resistance (0.8°C/W)
- High Surge Current (1000A)
- Low Reverse Current (<50mA at rated v_R at 125°C)
- Available with Flexible Top Lead

DESCRIPTION

This series of Schottky barrier power rectifiers is ideally suited for output rectifiers and catch diodes in low voltage power supplies. The Unitorde high conductivity design, using a heavy copper top post and 4 point crimp, ensures cool thermal operation and low dynamic impedance. Rugged design absorbs stress that can damage glass-to-metal seal during installation and use.

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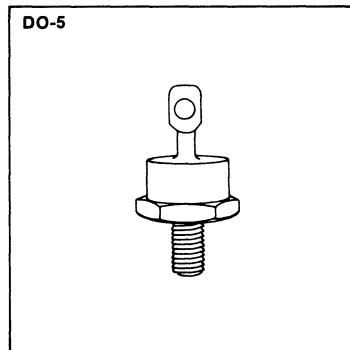
ABSOLUTE MAXIMUM RATINGS

	USD520	USD535	USD545	USD550
Working Peak Reverse Voltage, V_{RWM}	20V	35V	45V	50V
DC Blocking Voltage, V_R	20V	35V	45V	50V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	24V	42V	54V	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz, 50 percent Duty Cycle), I_{FRM}	150A (at $T_c = 115^\circ\text{C}$)			
Average Rectified Forward Current, I_{FAVI}	75A (at $T_c = 115^\circ\text{C}$)			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	1000A			
Peak Reverse Transient Current, I_{RM}	2A			
Storage Temperature Range, T_{SIG}	-55° to +200°C			
Operating Junction Temperature, T_J	+175°C			
Thermal Resistance Junction-to-Case, $R_{\theta JC}$	0.8°C/W			

MECHANICAL SPECIFICATIONS

USD520
USD535
USD545
USD550

	ins.	mm
A	.225 ± .005	5.72 ± 0.13
B	.060 MIN.	1.52 MIN.
C	.156 ± .020	3.96 ± 0.51
D	156 MIN. FLAT	3.96 MIN. FLAT
E	.667 DIA. MAX.	16.94 DIA. MAX.
F	.090 MAX.	2.29 MAX.
G	.677 ± .010	17.20 ± 0.25
H	.375 MAX.	9.53 MAX.
J	140 MIN. DIA.	3.56 MIN. DIA.
K	1.000 MAX.	25.40 MAX.
L	450 MAX.	11.43 MAX.
M	.438 ± .015	11.13 ± 0.38
N	.078 MAX.	1.98 MAX.



Notes:

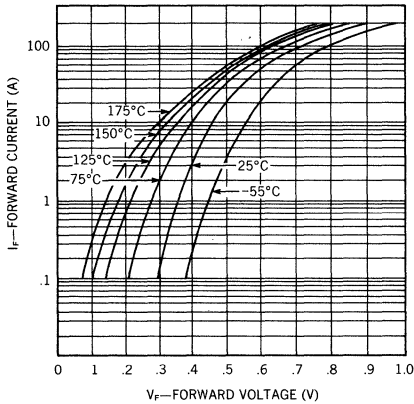
1. Cathode is stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds (35 kg. cm).
4. Angular orientation of terminal is undefined.



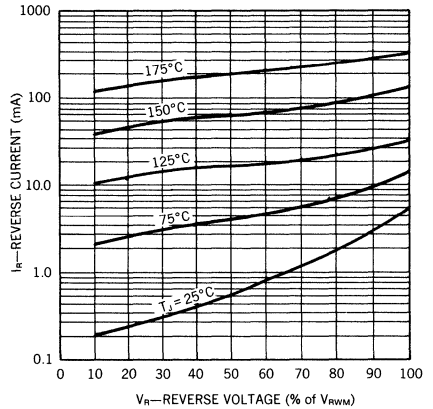
ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C)

Characteristic	Symbol	Limit		Units	Conditions
		USD545	USD550		
Maximum Instantaneous Reverse Current	i_R	20 (50)	20 (75)	mA	$V_R = V_{RWM}$ (T _C = 125°C) Pulse Width = 300μs, Duty Cycle = 1 percent
Maximum Instantaneous Forward Voltage	V_F	0.50		V	$i_F = 10A, T_C = 25°C$
		0.68		V	$i_F = 60A, T_C = 25°C$
		0.60		V	$i_F = 60A, T_C = 25°C$
Flexible Top Lead Option	V_F	(0.63)		V	$i_F = 60A, (T_C = 125°C)$
Maximum Capacitance	C_t	4000		pF	$V_R = 5.0V$
Maximum Voltage Rate of Change	dv/dt	1000		V/μS	$V_R = \text{rated}$

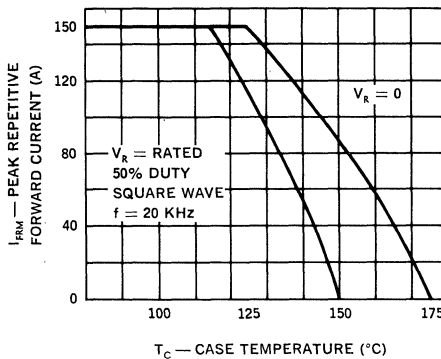
Typical Forward Current vs Forward Voltage



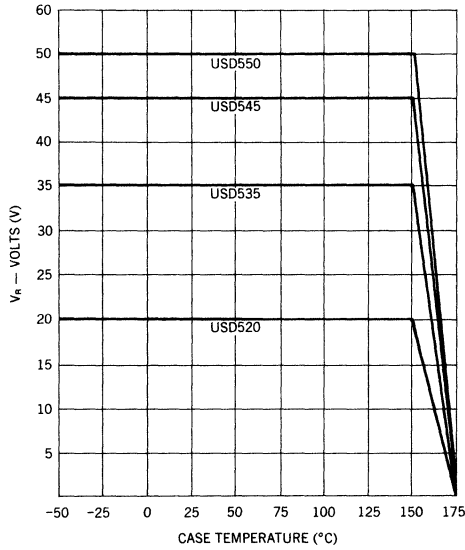
Typical Reverse Current vs Reverse Voltage



Maximum Current vs Case Temperature



$V_{R(MAX)}$ Rating vs Case Temperature



6

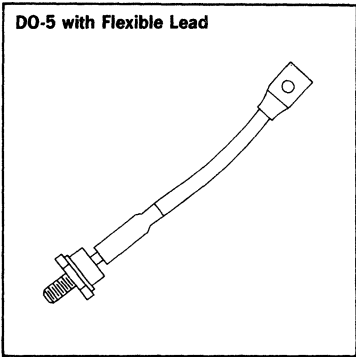
MECHANICAL SPECIFICATIONS

FLEXIBLE TOP LEAD (OPTIONAL)
Add an "F" Suffix to Part Number.

USD520F
USD535F
USD545F
USD550F

	INCHES	MILLIMETERS
M	.718 MAX.	18.24 MAX.
N	4.50 ± .250	114.3 ± 6.35
P	.525 MAX.	13.23 MAX.
Q	.675 ± .035	17.15 ± 0.89
R	.205 ± .005	5.21 ± 0.13
S	.075 ± .010	1.91 ± 0.25
T	1.125 MAX.	28.58 MAX.

*To 125°C (Ambient)



Note: Consult Factory for Non-standard Lead Lengths.

POWER SCHOTTKY RECTIFIERS

150A Pk, 45V

USD545HR2

FEATURES

- Very Low Forward (0.6V at 75A, 125°C)
- High Reverse Surge Voltage (60V)
- Low Recovered Charge
- Rugged Package Design (DO-5)
- High Efficiency for Low Voltage Supplies
- Low Thermal Resistance (0.8° C/W)
- High Surge Current (1000A)
- Low Reverse Current (<50mA at rated V_R at 125°C)
- High Reliability Screening

DESCRIPTION

The USD545 Schottky barrier power rectifier is ideally suited for output rectifiers and catch diodes in low voltage power supplies. Unitorde semiconductors are inherently high-reliability devices; however, for those users who want the ultimate assurance of reliability, we offer the USD545 Schottky with 100% HR-SH screening as described elsewhere within this data sheet.

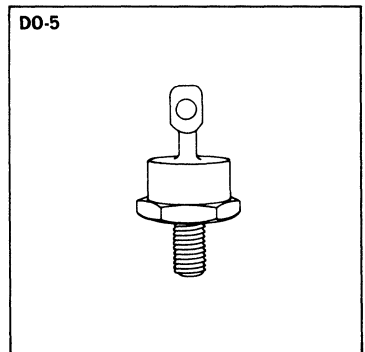
ABSOLUTE MAXIMUM RATINGS

Working Peak Reverse Voltage V_{RWM}	45V
DC Blocking Voltage, V_R	45V
Peak Repetitive Transient Voltage, V_{RSM}	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz, 50 percent Duty Cycle), I_{FRM}	150A (at $T_C = 115^\circ\text{C}$)
Average Rectified Forward Current, $I_{F(AV)}$	75A (at $T_C = 115^\circ\text{C}$)
Non-repetitive Peak Surge Current (8.3mS), I_{FSM}	1000A
Peak Reverse Surge Current, I_{RM}	2A
Storage Temperature Range, T_{Stg}	-55°C to +200°C
Operating Junction Temperature, T_J	+175°C
Thermal Resistance Junction-to-Case, $R_{\theta JC}$	0.8°C/W

MECHANICAL SPECIFICATIONS

USD545HR2

	ins.	mm
A	225 ± 005	5 72 ± 0 13
B	060 MIN	1 52 MIN
C	156 ± 020	3 96 ± 0 51
D	156 MIN FLAT	3 96 MIN FLAT
E	667 DIA MAX	16 94 DIA MAX
F	090 MAX	2 29 MAX
G	677 ± 010	17 20 ± 0 25
H	.375 MAX	9 53 MAX
J	140 MIN DIA	3 56 MIN DIA
K	1 000 MAX	25 40 MAX
L	450 MAX	11 43 MAX
M	438 ± 015	11 13 ± 0 38
N	078 MAX	1 98 MAX



Notes:

1. Cathode is stud.
2. All metal surfaces tin plated.
3. Maximum unlubricated stud torque: 30 inch pounds (35 kg. cm).
4. Angular orientation of terminal is undefined.

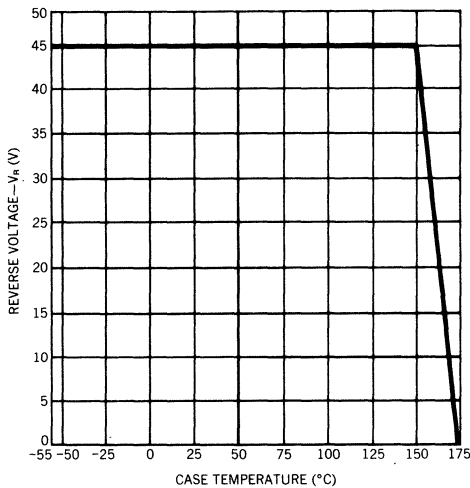
ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C)

Characteristic	Symbol	Max.	Units	Conditions
Maximum Instantaneous Reverse Current	I _R	10 50 175	mA	V _R = 45V T _C = 25°C T _C = 125°C T _C = 150°C Pulse Width = 300μS Duty Cycle = 1 percent
Maximum Instantaneous Forward Current	V _F	0.70 0.60 0.55	V	I _F = 75A T _C = 25°C T _C = 125°C T _C = 150°C Pulse Width = 300μS Duty Cycle = 1 percent
Capacitance	C _t	4000	pF	V _R = 5V
Voltage Rate of Change	dv/dt	1000	V/μS	V _R = 45V
Reverse Energy ⁽¹⁾	E _R	2	A	Duty Cycle ≤ 1 percent

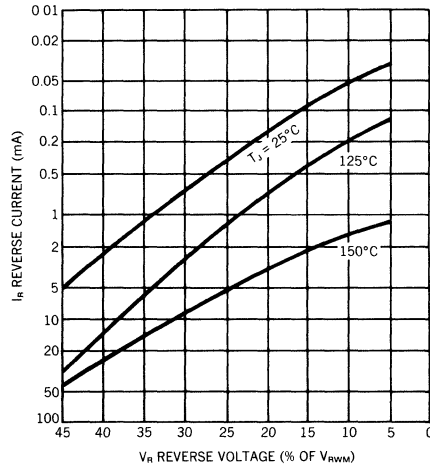
⁽¹⁾ See Reverse Energy Circuit.

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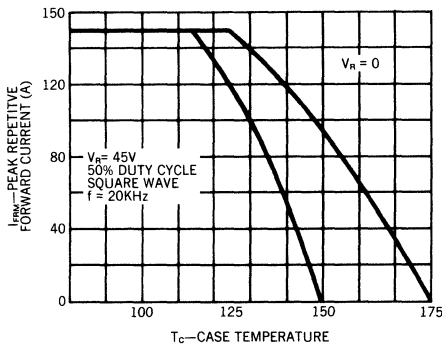
V_{R(MAX)} vs Case Temperature



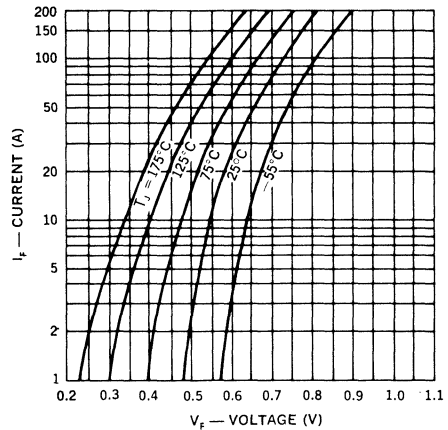
Typical Reverse Current vs Reverse Voltage



Peak Repetitive Forward Current



Typical Forward Current vs. Forward Voltage



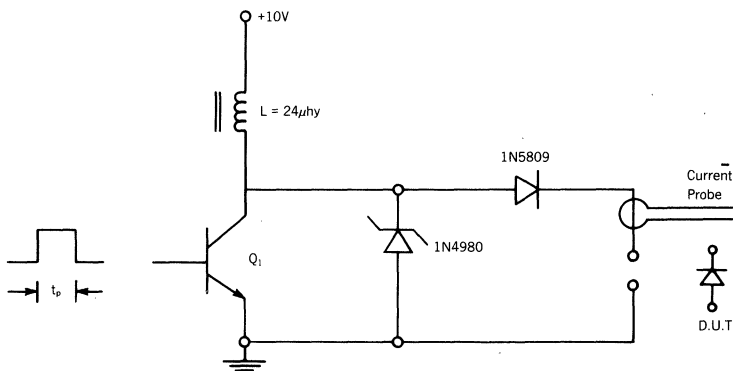
HR-SH

This specification outlines the screening operations to which devices shall be subjected.

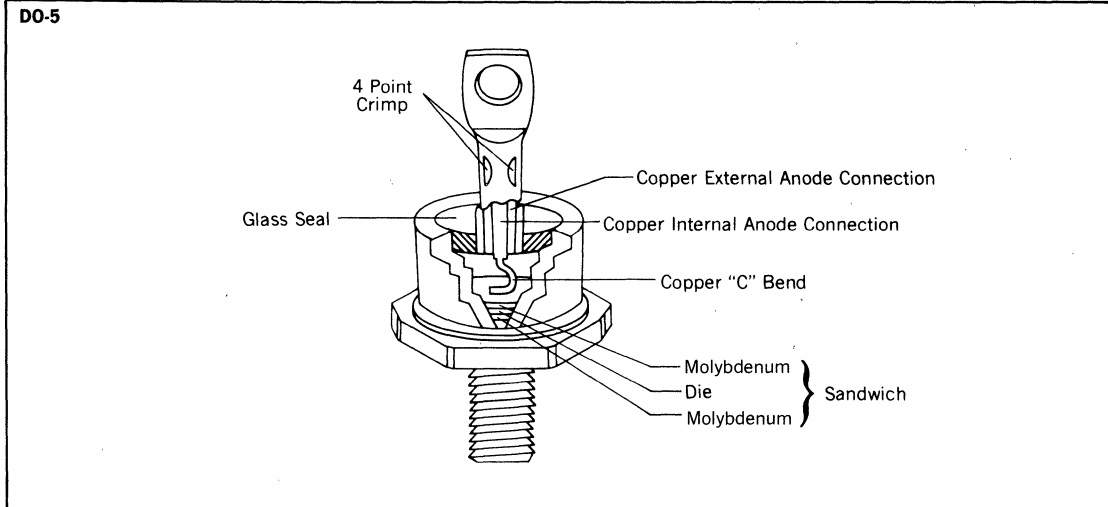
1. ER with peak current of 2A (See Reverse Energy Circuit).
2. Hermetic Seal:

Fine Leak	}	per MIL-STD750 Method 1071
Gross Leak		
3. Thermal Cycling: Ten (10) cycles. Each cycle consists of fifteen (15) minutes at 200°C ambient, transfer immediately to -65°C ambient for fifteen (15) minutes and immediately return to 200°C again.
4. Reverse Bias Operation: 36V shall be applied for one-hundred and sixty-eight (168) hours at 150°C. Temperature is then reduced to 25°C over a period of not less than one (1) hour with full voltage maintained.
5. Electrical Measurements: All parameters shall be measured to insure conformance with specifications. Any parts exceeding specified limits or exhibiting unusual characteristics shall be removed from the lot.

Reverse Energy Circuit



t_p , adjust for desired peak current in D.U.T. when Q turns off.
 Q_1 , must have fall time t_f of 100nS max.



POWER SCHOTTKY RECTIFIERS

12A Pk, up to 45V

USD620
USD635
USD640
USD645

FEATURES

- Very Low Forward Voltage
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Working Voltage @ Rated $T_{j(max)}$

DESCRIPTION

The USD600 series of Schottky power rectifiers is ideally suited for output rectifiers and catch diodes in high frequency low voltage power supplies.

ABSOLUTE MAXIMUM RATINGS

	USD620	USD635	USD640	USD645
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V
DC Blocking Voltage, V_R	20V	35V	40V	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	24V	42V	48V	54V
Average Rectified Forward Current @ $T_C = 115^\circ C$, $I_{F(AV)}$	6A			
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20 KHz, 50% Duty Cycle, @ $T_C = 115^\circ C$), I_{FRM}	12A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	150A			
Peak Reverse Transient Current, I_{RM}	1A			
Operating Junction Temperature, T_j	150°C			
Storage Temperature Range, T_{Stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	3.0°C/W			

6

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ C$)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	5	mA	$V_R = V_{RWM}$ Pulse Width = 400 μ s Duty Cycle = 1 percent
Maximum Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μ s Duty Cycle = 1 percent $T_C = 125^\circ C$
Maximum Instantaneous Forward Voltage	V_F	0.55	V	$i_F = 6A$ $i_F = 12A$ $T_C = 125^\circ C$
		0.65	V	
		0.48 0.60	V	
Capacitance	C_t	1000	pF	$V_R = 5V$
Voltage Rate of Change	dv/dt	1000	V/ μ s	$V_R = V_{RWM}$

MECHANICAL SPECIFICATIONS

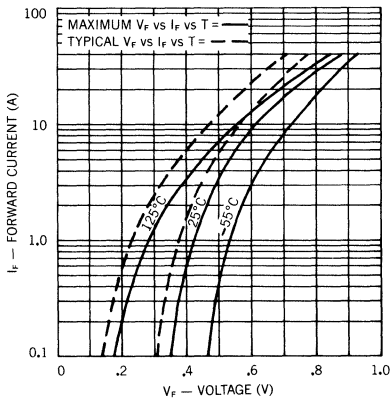
USD600 SERIES

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

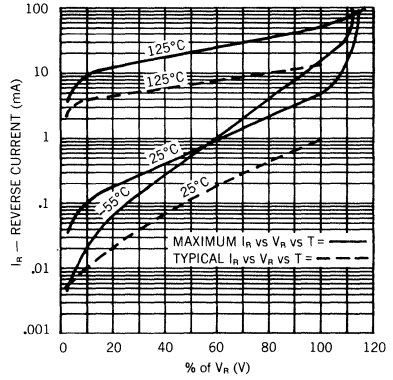
PIN 1. Cathode
2. Anode
Tab is connected to Cathode.

TO-220AC

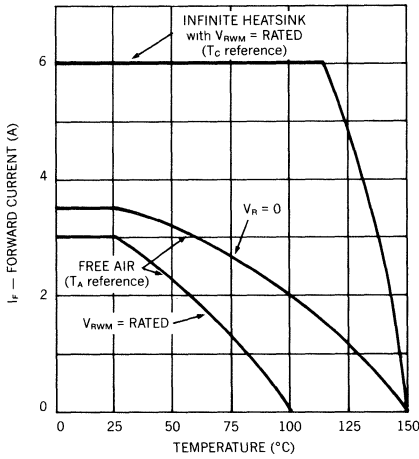
Forward Current vs. Forward Voltage



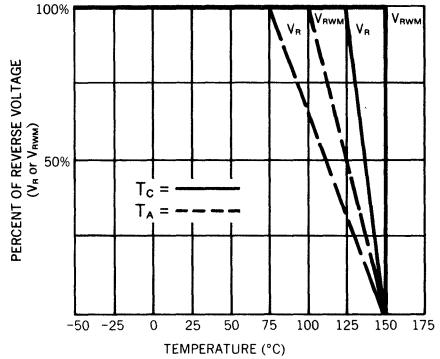
Reverse Current vs. Voltage



Average Forward Current vs. Temperature



V_R Rating vs. Temperature



DUAL POWER SCHOTTKY RECTIFIERS

12A Av, up to 45V

USD620C
USD635C
USD640C
USD645C

FEATURES

- Very Low Forward Voltage
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Working Voltage @ Rated $T_{j(max)}$

DESCRIPTION

The USD600C series of power Schottky rectifiers, in the industry standard TO-220 package, is specifically designed for operation in power switching circuits to frequencies in excess of 100 KHz. The series combines Schottky rectifiers in one convenient package; thus, simplifying installation, reducing heatsink requirements and component parts count.

ABSOLUTE MAXIMUM RATINGS (Per Diode Unless Otherwise Noted)

	USD620C	USD635C	USD640C	USD645C
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V
DC Blocking Voltage, V_R	20V	35V	40V	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	24V	42V	48V	54V
Average Rectified Forward Current @ $T_C = 115^\circ C$, I_o^*	12A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	150A			
Peak Reverse Transient Current, I_{RM}	1A			
Operating Junction Temperature, T_j	150°C			
Storage Temperature Range, T_{Stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	3.0°C/W			

*Full Wave Center-Tap; I_o (AV) 20 KHz Square Wave

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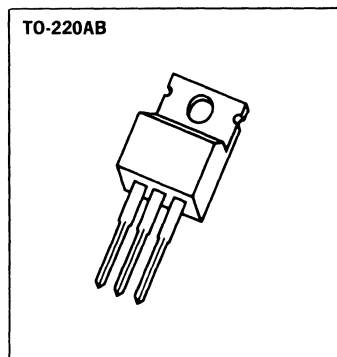
ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ C$) (Per Diode)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	5	mA	$V_R = V_{RWM}$ Pulse Width = 400 μ s Duty Cycle = 1 percent
Maximum Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μ s Duty Cycle = 1 percent $T_C = 125^\circ C$
Maximum Instantaneous Forward Voltage	V_F	0.55	V	$i_F = 6A$ $i_F = 12A$
		0.65	V	
		0.48	V	$i_F = 6A$ $i_F = 12A$ } $T_C = 125^\circ C$
		0.60	V	
Capacitance	C_t	1000	pF	$V_R = 5V$
Voltage Rate of Change	dv/dt	1000	V/ μ s	$V_R = V_{RWM}$

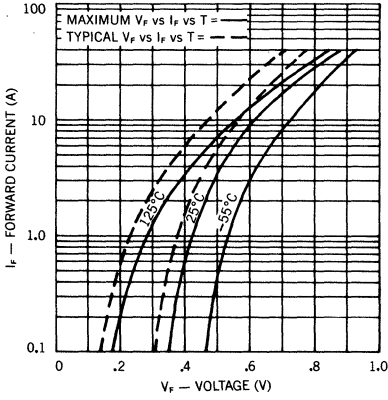
MECHANICAL SPECIFICATIONS

USD600C SERIES

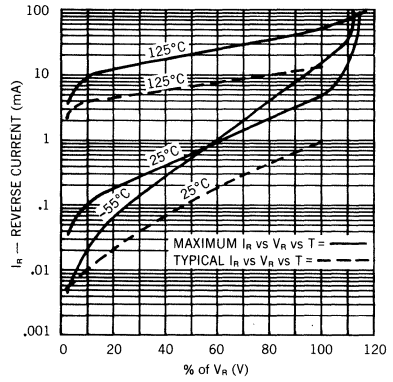
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270



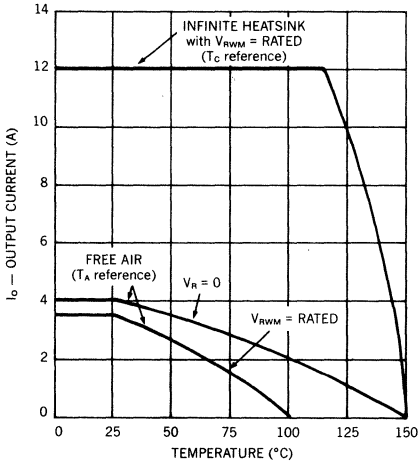
Forward Current vs. Forward Voltage



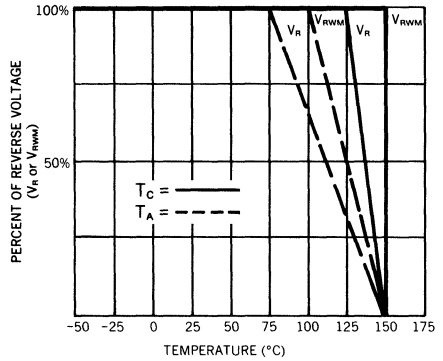
Reverse Current vs. Voltage



Average Output Current vs. Temperature



V_R Rating vs. Temperature



POWER SCHOTTKY RECTIFIERS

16A Pk, up to 45V

USD720
USD735
USD740
USD745

FEATURES

- Very Low Forward Voltage
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Working Voltage @ Rated $T_{j(max)}$

DESCRIPTION

The USD700 series of Schottky power rectifiers is ideally suited for output rectifiers and catch diodes in high frequency low voltage power supplies.

ABSOLUTE MAXIMUM RATINGS

	USD720	USD735	USD740	USD745
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V
DC Blocking Voltage, V_R	20V	35V	40V	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{FRM}	24V	42V	48V	54V
Average Rectified Forward Current @ $T_C = 115^\circ\text{C}$, $I_F (AV)$	8A			
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20 KHz, 50% Duty Cycle, @ $T_C = 115^\circ\text{C}$), I_{FRM}	16A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	200A			
Peak Reverse Transient Current, I_{RM}	1A			
Operating Junction Temperature, T_j	150°C			
Storage Temperature Range, T_{stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	2.8°C/W			

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ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	5	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent
Maximum Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent $T_C = 125^\circ\text{C}$
Maximum Instantaneous Forward Voltage	V_F	0.55	V	$i_F = 8A$ $i_F = 16A$
		0.48 0.60	V	
Capacitance	C_t	1000	pF	$V_R = 5V$
Voltage Rate of Change	dv/dt	1000	V/ μs	$V_R = V_{RWM}$

MECHANICAL SPECIFICATIONS

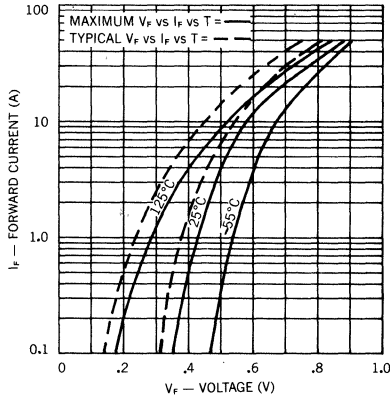
PIN 1. Cathode
2. Anode
Tab is connected to Cathode.

USD700 SERIES

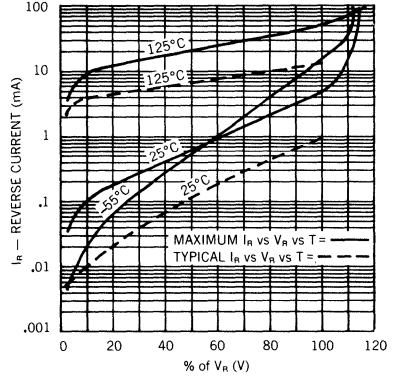
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

TO-220AC

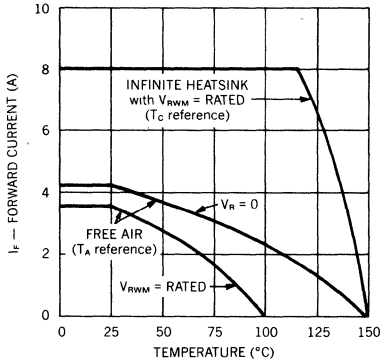
Forward Current vs. Forward Voltage



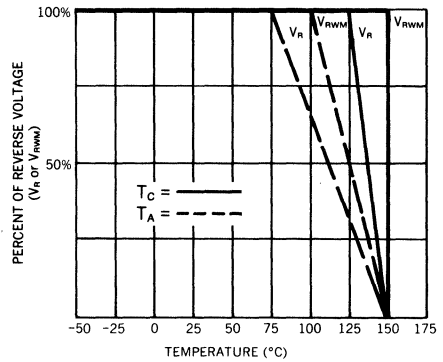
Reverse Current vs. Voltage



Average Forward Current vs. Temperature



V_R Rating vs. Temperature



DUAL POWER SCHOTTKY RECTIFIERS

16A Av, up to 45V

USD720C
USD735C
USD740C
USD745C

FEATURES

- Very Low Forward Voltage
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Working Voltage @ Rated $T_{j(max)}$

DESCRIPTION

The USD700C series of power Schottky rectifiers, in the industry standard TO-220 package, is specifically designed for operation in power switching circuits to frequencies in excess of 100 KHz. The series combines Schottky rectifiers in one convenient package; thus, simplifying installation, reducing heatsink requirements and component parts count.

ABSOLUTE MAXIMUM RATINGS (Per Diode Unless Otherwise Noted)

	USD720C	USD735C	USD740C	USD745C
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V
DC Blocking Voltage, V_R	20V	35V	40V	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RM}	24V	42V	48V	54V
Average Rectified Forward Current @ $T_C = 115^\circ\text{C}$, I_o^*	16A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	200A			
Peak Reverse Transient Current, I_{RM}	1A			
Operating Junction Temperature, T_j	150°C			
Storage Temperature Range, T_{stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	2.8°C/W			

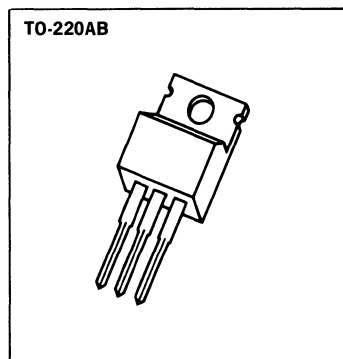
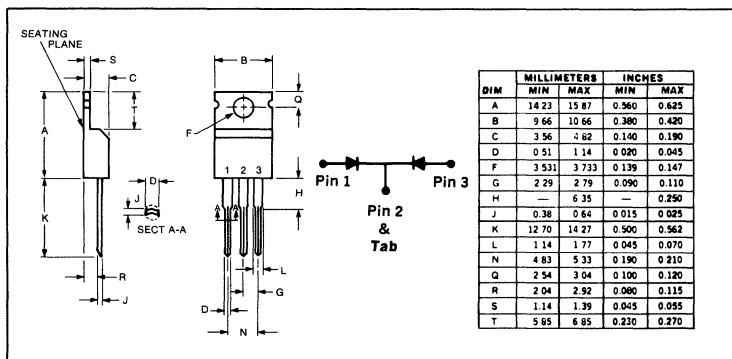
*Full Wave Center-Tap; I_o (AV) 20KHz Square Wave

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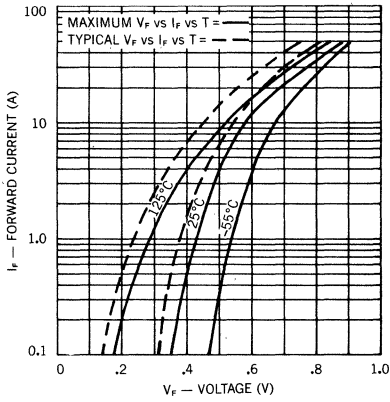
ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$) (Per Diode)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	5	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent
Maximum Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent $T_C = 125^\circ\text{C}$
Maximum Instantaneous Forward Voltage	V_F	0.55	V	$i_F = 8A$ $i_F = 16A$
		0.65	V	
Capacitance	C_t	0.48	pF	$T_C = 125^\circ\text{C}$
		0.60		
Voltage Rate of Change	dv/dt	1000	V/ μs	$V_R = V_{RWM}$

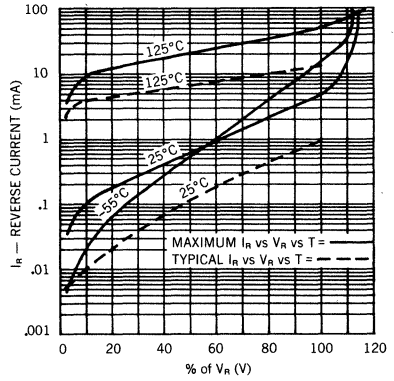
MECHANICAL SPECIFICATIONS



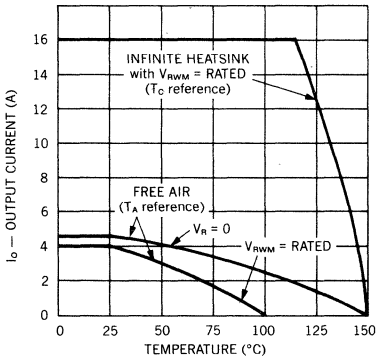
Forward Current vs. Forward Voltage



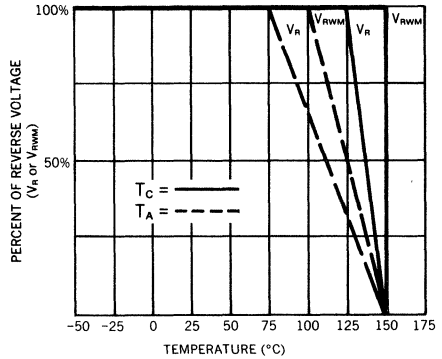
Reverse Current vs. Voltage



Average Output Current vs. Temperature



V_R Rating vs. Temperature



POWER SCHOTTKY RECTIFIERS

24A Pk, up to 45V

USD820
USD835
USD840
USD845

FEATURES

- Very Low Forward Voltage (0.45V max @ 12A)
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Blocking Voltage @ Rated I_{Tmax}

DESCRIPTION

The USD800 series of Schottky barrier power rectifiers is ideally suited for output rectifiers and catch diodes in low voltage power supplies.

ABSOLUTE MAXIMUM RATINGS

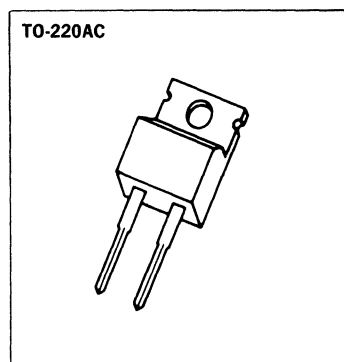
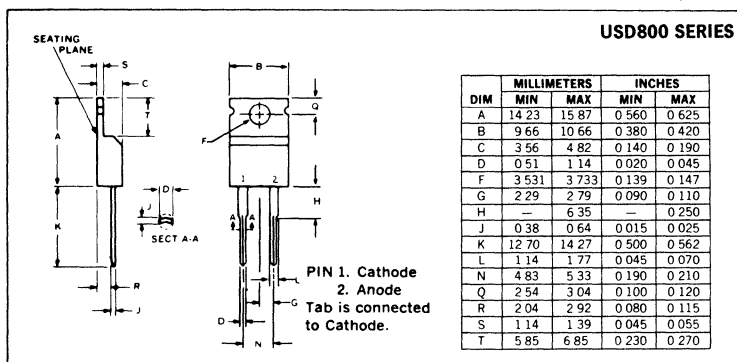
	USD820	USD835	USD840	USD845
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V
DC Blocking Voltage, V_R	20V	35V	40V	45V
Peak Repetitive Surge Voltage, V_{RSM} @ I_{FRM}	24V	42V	48V	54V
Average Rectified Forward Current @ $T_C = 115^\circ\text{C}$, I_o	12A			
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz, 50% Duty Cycle, @ $T_C = 115^\circ\text{C}$), I_{FRM}	24A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	200A			
Peak Reverse Transient Current, I_{RM}	1A			
Operating Junction Temperature, T_J	150°C			
Storage Temperature Range, T_{Stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	2.4°C/W			

6

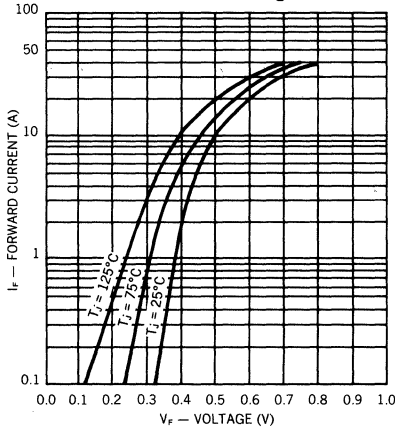
ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	20	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent
Typical Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent $T_C = 125^\circ\text{C}$
Maximum Instantaneous Forward Voltage	V_F	0.59	V	$i_F = 12\text{A}$
		0.51	V	$i_F = 12\text{A}$ $T_C = 125^\circ\text{C}$
Capacitance	C_t	2000	pF	$V_R = 5\text{V}$
Voltage Rate of Change	dv/dt	1000	V/ μs	$V_R = V_{RWM}$

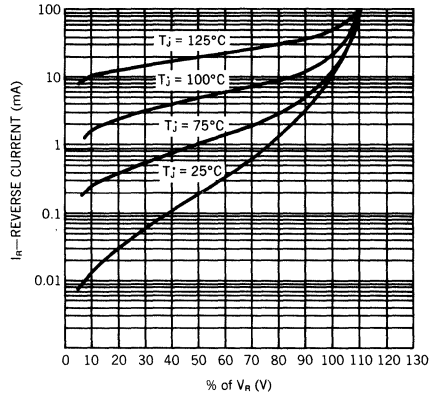
MECHANICAL SPECIFICATIONS



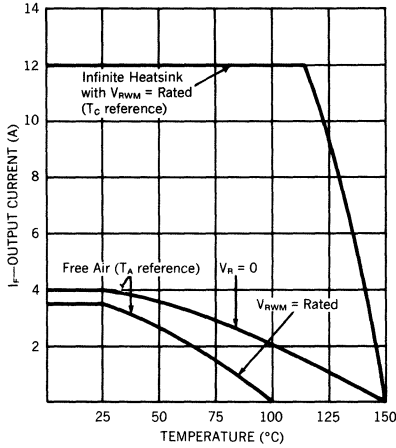
Typical Forward Current vs. Forward Voltage



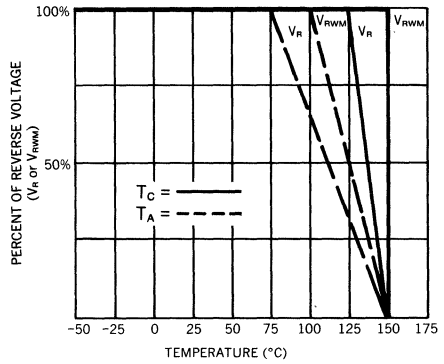
Typical Reverse Current vs. Voltage



Output Current vs. Temperature



V_R Rating vs. Temperature



POWER SCHOTTKY RECTIFIERS

32A Pk, up to 45V

USD920
USD935
USD940
USD945

FEATURES

- Very Low Forward Voltage (0.5V max @ 16A)
- Reverse Transient Capability
- Economical Convenient Plastic Package
- Mechanically Rugged
- 45V Blocking Voltage @ Rated T_{jmax}

DESCRIPTION

The USD900 series of Schottky barrier power rectifiers is ideally suited for output rectifiers and catch diodes in low voltage power supplies.

ABSOLUTE MAXIMUM RATINGS

	USD920	USD935	USD940	USD945
Working Peak Reverse Voltage, V_{RWM}	20V	35V	40V	45V ..
DC Blocking Voltage, V_R	20V	35V	40V	45V ..
Peak Repetitive Surge Voltage, V_{RSM} @ I_{RSM}	24V	42V	48V	54V ..
Average Rectified Forward Current @ $T_C = 115^\circ\text{C}$, I_O	16A			
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz, 50% Duty Cycle, @ $T_C = 115^\circ\text{C}$), I_{FRM}	32A			
Non-repetitive Peak Surge Current (8.3ms), I_{FSM}	250A			
Peak Reverse Transient Current, I_{RM}	2A			
Operating Junction Temperature, T_J	150°C			
Storage Temperature Range, T_{Stg}	-55°C to +150°C			
Thermal Resistance, Junction to Case, $R_{\theta JC}$	2°C/W			

6

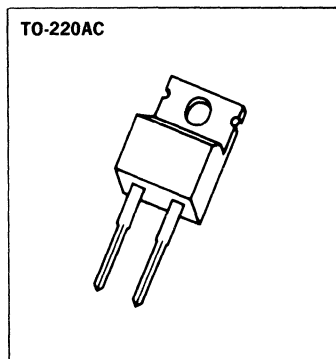
ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	LIMIT	UNITS	CONDITIONS
Maximum Instantaneous Reverse Current	i_R	20	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent
Typical Instantaneous Reverse Current	i_R	50	mA	$V_R = V_{RWM}$ Pulse Width = 400 μs Duty Cycle = 1 percent $T_C = 125^\circ\text{C}$
Maximum Instantaneous Forward Voltage	V_F	0.6	V	$i_F = 16\text{A}$
		0.53	V	$i_F = 16\text{A}$ $T_C = 125^\circ\text{C}$
Capacitance	C_t	2000	pF	$V_R = 5\text{V}$
Voltage Rate of Change	dv/dt	1000	V/ μs	$V_R = V_{RWM}$

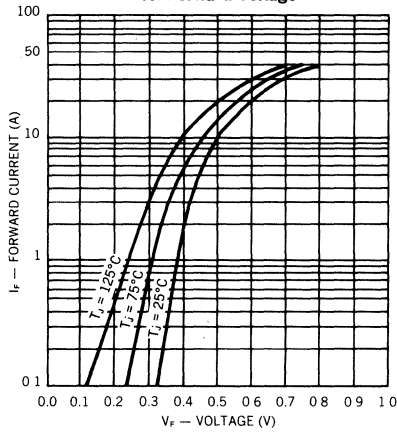
MECHANICAL SPECIFICATIONS

USD900 SERIES

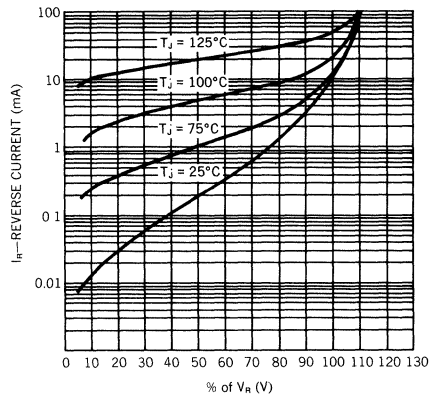
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270



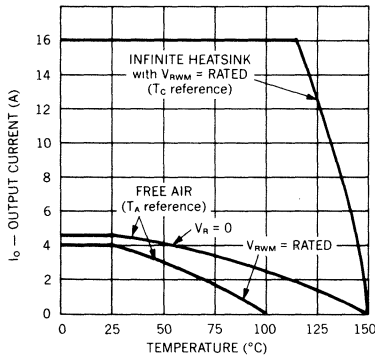
Typical Forward Current vs. Forward Voltage



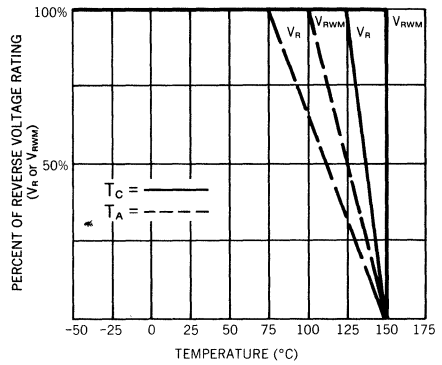
Typical Reverse Current vs. Voltage



Output Current vs. Temperature



V_R Rating vs. Temperature



POWER SCHOTTKY RECTIFIERS

1A, Up to 40V

USD1120

USD1130

USD1140

FEATURES

- Very Low Forward Voltage
(0.45V max @ 1A for the USD1120)
- Low Stored Charge, Majority Carrier Conduction
- Economical, Convenient Plastic Package
- Small Size

DESCRIPTION

The USD1120, USD1130 and USD1140 series of Schottky barrier rectifiers are ideally suited for use as rectifiers in low voltage, high frequency inverters, as free wheeling diodes and as polarity protection diodes.

ABSOLUTE MAXIMUM RATINGS

	USD1120	USD1130	USD1140
Peak Repetitive Reverse Voltage, V_{RRM}	20V	30V	40V
Working Peak Reverse Voltage, V_{RWM}	20V	30V	40V
DC Blocking Voltage, V_R	20V	30V	40V
Non-Repetitive Peak Reverse Voltage, V_{RSM}	24V	36V	48V
RMS Reverse Voltage, $V_{R(RMS)}$	14V	21V	28V
Average Rectified Forward Current, I_o ($V_{R(REQUIV)} \leq 0.2 V_R(DC)$, $T_L = 90^\circ C$, $R_{\theta JA} = 80^\circ C/W$, PC Board Mounting, see Note 1, $T_A = 55^\circ C$)		1.0A	
Ambient Temperature, T_A (Rated $V_R(DC)$, $P_{F(AV)} = 0$, $R_{\theta JA} = 80^\circ C/W$)	85°C	80°C	75°C
Non-Repetitive Peak Surge Current, I_{FSM} (Surge applied at rated load conditions, half-wave, single phase 60Hz, $T_L = 70^\circ C$)		50A (for one cycle)	
Operating and Storage Junction Temperature Range, (Reverse Voltage Applied)		-65°C to +150°C	
Thermal Resistance, Junction to Ambient (Note 1), $R_{\theta JA}$		80°C/W Max.	

Note 1: Lead Temperature reference is cathode lead $\frac{1}{32}$ " from case.

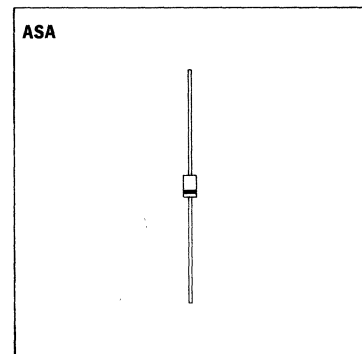
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MECHANICAL SPECIFICATIONS

USD1120 USD1130 USD1140

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.260	4.06	6.60
B	0.110	0.120	2.79	3.05
D	0.030	0.034	0.76	0.86
K	1.0	—	25.4	—

Soldering 220°C, $\frac{1}{16}$ " from case for ten seconds

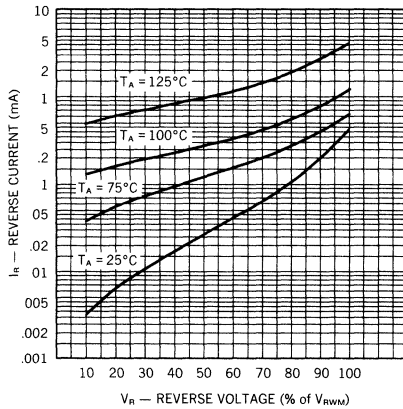


ELECTRICAL SPECIFICATIONS ($T_L = 25^\circ\text{C}$ unless noted)

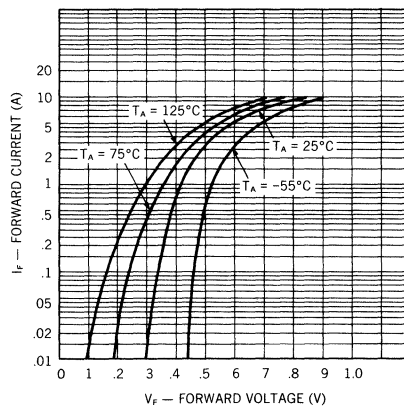
CHARACTERISTIC	SYMBOL	USD1120	USD1130	USD1140	UNITS	CONDITIONS
Maximum Instantaneous Forward Voltage (Note 2)	V_F	0.450	0.475	0.500	V	$i_F = 1.0\text{A}$
		0.600	0.625	0.650	V	$i_F = 3.1\text{A}$
Maximum Instantaneous Reverse Current @ Rated DC Voltage (Note 2)	i_R	1.0	1.0	1.0	mA	$T_L = 25^\circ\text{C}$
		10	10	10	mA	$T_L = 100^\circ\text{C}$

Note 2: Pulse width = 300 μs ; duty cycle = 2%.

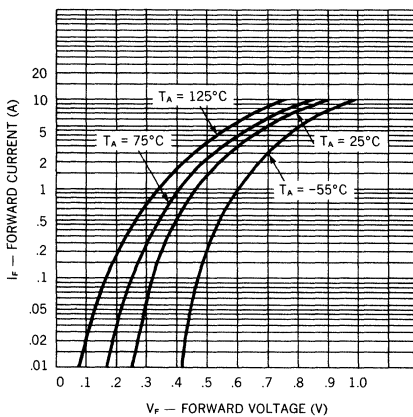
Typical Reverse Current vs Reverse Voltage



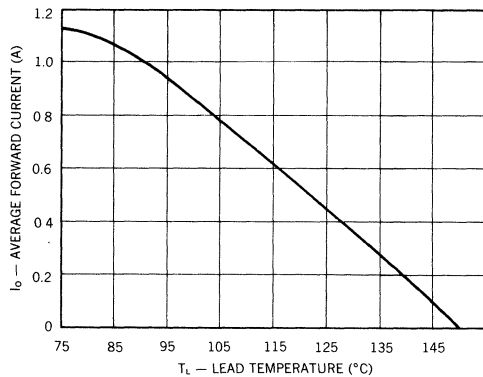
Typical Forward Voltage vs Forward Current (USD1120)



Typical Forward Voltage vs Forward Current (USD1130, USD1140)



Output Current vs Lead Temperature



POWER SCHOTTKY MODULES

100A, Up to 50V

USM140C
USM145C
USM150C
Preliminary

FEATURES

- Low Forward Voltage
- Low Recovered Charge
- High Reverse Transient Capability
- High Surge Current
- High Efficiency for Low Voltage Designs

DESCRIPTION

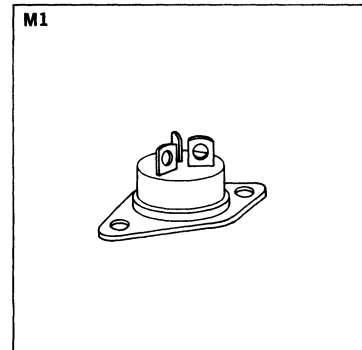
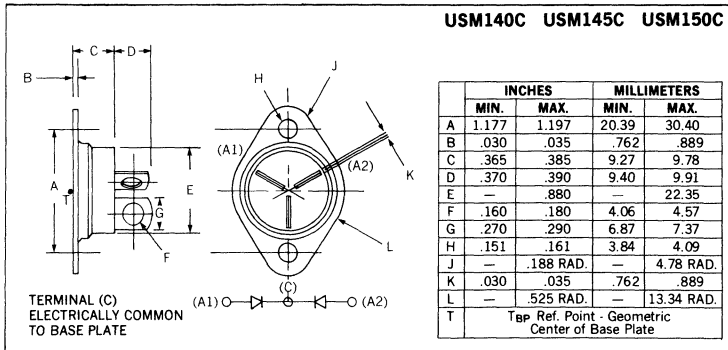
The Unitrode Schottky Module utilizes high current Schottky rectifiers, in a convenient single package, arranged in a common cathode configuration. The combination of low thermal resistance and high conductance terminals makes this device ideally suited for high current full wave center-tap rectification or feed-forward applications.

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ABSOLUTE MAXIMUM RATINGS (per diode unless noted)

	USM140C	USM145C	USM150C
Working Peak Reverse Voltage, V_{RWM}	40V	45V	50V
DC Blocking Voltage, V_R	40V	45V	50V
Peak Repetitive Surge Voltage, V_{RSM}	48V	54V	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz 50 Percent Duty Cycle), I_{FRM}	100A		
Average Rectified Forward Current, I_o	100A (@ $T_c = 115^\circ\text{C}$ Fullwave Configuration)		
Non-repetitive Peak Surge Current, I_{FSM}	1000A		
Peak Reverse Transient Current, I_{RM}	2A		
Storage Temperature Range, T_{STG}	-40°C to $+150^\circ\text{C}$		
Operating Temperature Range, T_J	-40°C to $+175^\circ\text{C}$		
Thermal Resistance, $R_{\theta JBP}$	0.7°C/W per module		

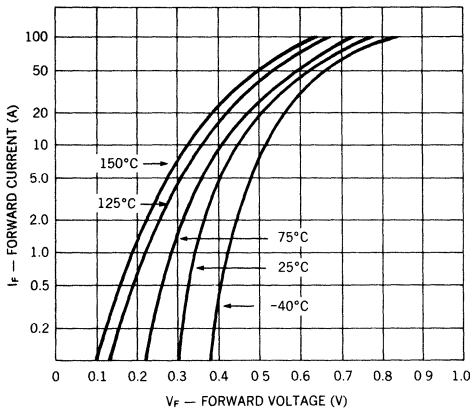
MECHANICAL SPECIFICATIONS



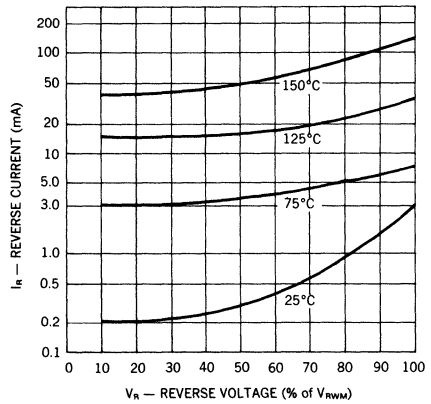
ELECTRICAL CHARACTERISTICS ($T_{BP} = 25^{\circ}C$ unless noted) (Per Diode)

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMIT	UNITS
Maximum Instantaneous Reverse Current	i_R	$V_R = V_{RWM}$ ($T_{BP} = 125^{\circ}C$) Pulsewidth = $400\mu s$ Duty Cycle = 1%	20 (75)	mA
Maximum Instantaneous Forward Voltage	V_F	$I_F = 60A$ ($T_{BP} = 125^{\circ}C$) Pulsewidth = $300\mu s$ Duty Cycle = 1%	.690 (.630)	V
Maximum Instantaneous Forward Voltage	V_F	$I_F = 100A$ ($T_{BP} = 125^{\circ}C$) Pulsewidth = $300\mu s$ Duty Cycle = 1%	.860 (.775)	V
Capacitance	C_t	$V_R = 5V$	3000	pF
Voltage Rate of Change	dv/dt	$V_R = V_{RWM}$	1000	V/ μs
Reverse Energy	I_{RM}	See Reverse Energy Circuit	2	A

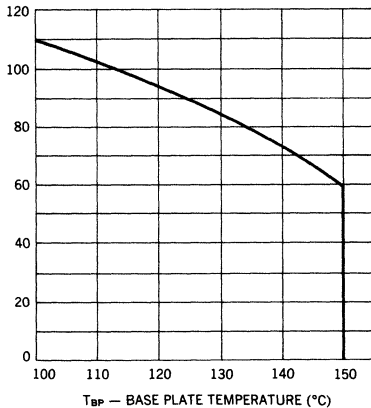
Typical Forward Current vs Forward Voltage



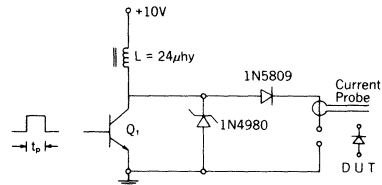
Typical Reverse Current vs Reverse Voltage



Output Current vs Case Temperature



Reverse Energy Circuit



t_p adjust for desired peak current in D.U.T. when Q turns off.
 Q_1 must have fall time t_f of 100ns max.

POWER SCHOTTKY MODULES

200A, Up to 50V

USM20040C
USM20045C
USM20050C
Preliminary

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FEATURES

- Low Forward Voltage
- Low Recovered Charge
- High Reverse Transient Capability
- High Surge Current
- High Efficiency for Low Voltage Designs

DESCRIPTION

The Unitrode Schottky Module utilizes high current Schottky rectifiers, in a convenient single package, arranged in a common cathode configuration. The combination of low thermal resistance and high conductance terminals makes this device ideally suited for higher current full wave center-tap rectification or feed-forward applications.

ABSOLUTE MAXIMUM RATINGS (per diode unless noted)

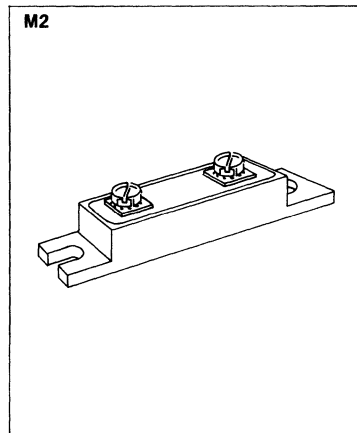
	USM20040C	USM20045C	USM20050C
Working Peak Reverse Voltage, V_{RWM}	40V	45V	50V
DC Blocking Voltage, V_R	40V	45V	50V
Peak Repetitive Surge Voltage, V_{RSM}	48V	54V	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz 50 Percent Duty Cycle), I_{FRM}	200A		
Average Rectified Forward Current, I_O	200A (@ $T_c = 115^\circ\text{C}$ Fullwave Configuration)		
Non-repetitive Peak Surge Current, I_{FSM}	2000A		
Peak Reverse Transient Current, I_{RM}	2A		
Storage Temperature Range, T_{STG}	-40°C to $+175^\circ\text{C}$		
Operating Temperature Range, T_J	-40°C to $+175^\circ\text{C}$		
Thermal Resistance, $R_{\theta JB}$	0.28°C/W per module		
Thermal Resistance, $R_{\theta JBP}$	0.56°C/W per leg		

MECHANICAL SPECIFICATIONS

USM20040C USM20045C USM20050C

Terminal Torque: 50 (Min.) 75 (Max.) lb. — in.
Mounting Base Torque: 30 (Min.) 40 (Max.) lb. — in.

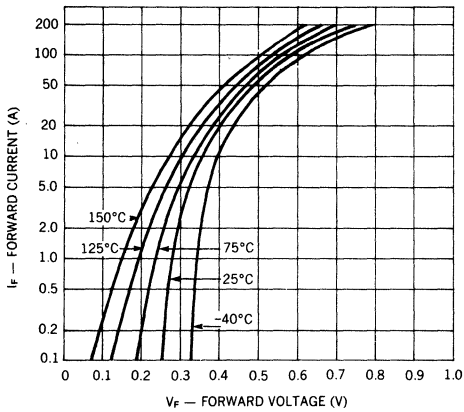
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A		2.63		66.80
B	1.35	1.40	34.29	35.56
C	.70	.80	17.78	20.32
D		.625		15.88
E	3.14	3.16	79.76	80.26
F		3.65		92.71
G	.25	.27	6.35	6.86
H	$\frac{1}{4}$ — 20 UNF With Captive Lockwasher			
T	Top Ref. Point - Geometric Center of Base Plate			



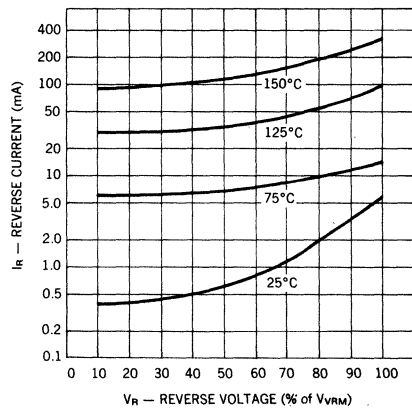
ELECTRICAL CHARACTERISTICS (T_{BP} = 25°C unless noted) (Per Diode)

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMIT		UNITS
			USM20045C	USM20050C	
Maximum Instantaneous Reverse Current	I _R	V _R = V _{RWM} Pulsewidth = 400μs Duty Cycle = 1% (T _{BP} = 125°C)	30 (125)	30 (150)	mA
Maximum Instantaneous Forward Voltage	V _F	I _F = 100A Pulsewidth = 300μs Duty Cycle = 1% (T _{BP} = 125°C)	(575)		V
Maximum Instantaneous Forward Voltage	V _F	I _F = 200A Pulsewidth = 300μs Duty Cycle = 1% (T _{BP} = 125°C)	.800 (.745)		V
Capacitance	C _t	V _R = 5V	6000		pF
Voltage Rate of Change	dv/dt	V _R = V _{RWM}	1000		V/μs
Reverse Energy	I _{RM}	See Reverse Energy Circuit	2		A

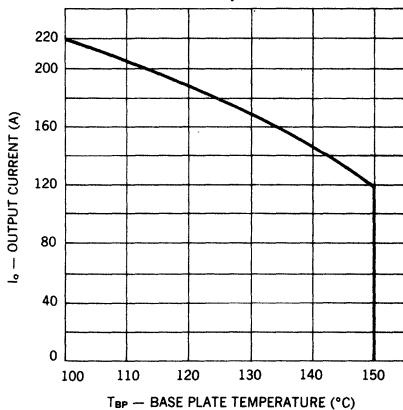
Typical Forward Current vs Forward Voltage



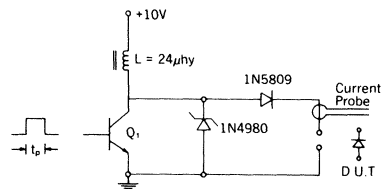
Typical Reverse Current vs Reverse Voltage



Output Current vs Case Temperature



Reverse Energy Circuit



t_p adjust for desired peak current in D.U.T. when Q turns off. Q₁ must have fall time t_f of 100ns max.

RECTIFIERS

Standard Recovery, 1 Amp to 2 Amp

UT236-UT347
 UT249-UT363
 UT251-UT364
 UT261-UT268

FEATURES

- Continuous Rating: to 2A
- Controlled Avalanche
- Surge Rating: to 30A
- PIV: to 1000V
- Miniature Package

DESCRIPTION

These miniature power rectifiers offer the user extreme reliability for high-rel military supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	1 Amp Series	1.25 Amp Series	1.5 Amp Series	2 Amp Series
100V	UT236	UT249	UT251	UT261
200V	UT234	UT242	UT252	UT262
400V	UT235	UT244	UT254	UT264
500V	UT237	UT245	UT255	UT265
600V	UT238	UT247	UT257	UT267
800V	UT361	UT362	UT258	UT268
1000V	UT347	UT363	UT364	

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	1 AMP SERIES	1.25 AMP SERIES	1.5 AMP SERIES	2 AMP SERIES
Maximum Average D.C. Output Current				
@ $T_A = 25^\circ\text{C}$	1.0A	1.25A	1.5A	2.0A
@ $T_A = 100^\circ\text{C}$	0.5A	0.65A	0.75A	1.0A
Non-Repetitive Sinusoidal				
Surge (8.3ms)	20A	20A	25A	30A
Operating Temperature Range	-195°C to +175°C			
Storage Temperature Range	-195°C to +175°C			
Thermal Resistance	See lead temperature derating curve			

MECHANICAL SPECIFICATIONS

UT236-UT347 UT249-UT363 UT251-UT364 UT261-UT268

Part Identification: Orange band indicates "UT." Part number printed on body.

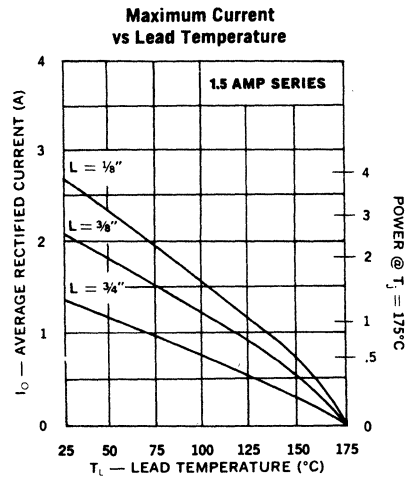
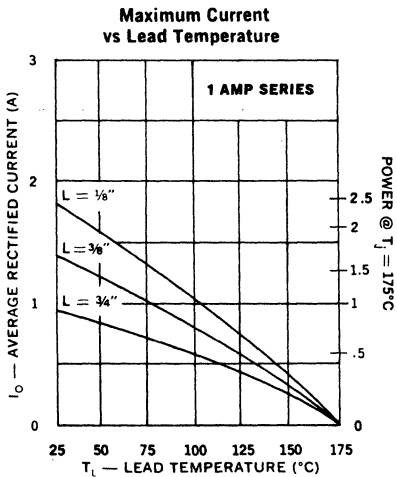
Polarity: Denoted by orange band.

Weight: 0.26 grams, typical.

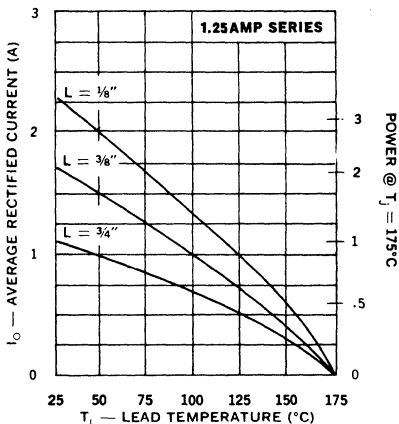
BODY A

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

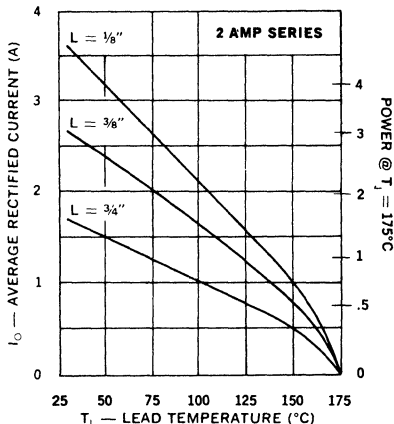
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV	
			25°C	100°C
UT261 UT262 UT264 UT265 UT267 UT268	100V 200V 400V 500V 600V 800V	1V @ 900mA	2μA	75μA
UT251 UT252 UT254 UT255 UT257 UT258 UT364	100V 200V 400V 500V 600V 800V 1000V	1V @ 750mA	2μA	75μA
UT249 UT242 UT244 UT245 UT247 UT362 UT363	100V 200V 400V 500V 600V 800V 1000V	1V @ 500mA	2μA	75μA
UT236 UT234 UT235 UT237 UT238 UT361 UT347	100V 200V 400V 500V 600V 800V 1000V	1V @ 400mA	2μA	75μA



Maximum Current vs Lead Temperature

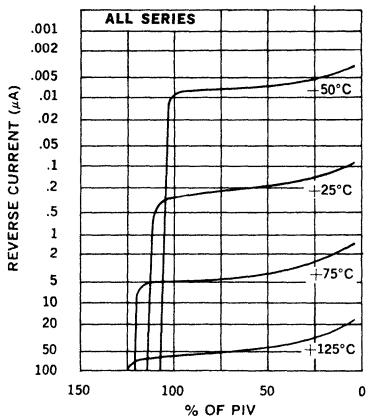


Maximum Current vs Lead Temperature

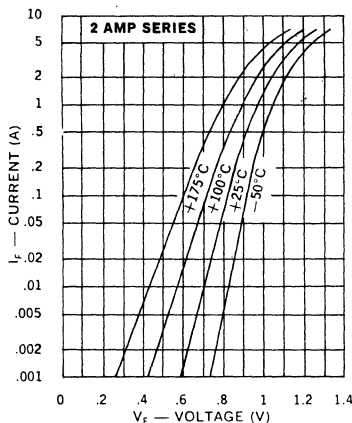


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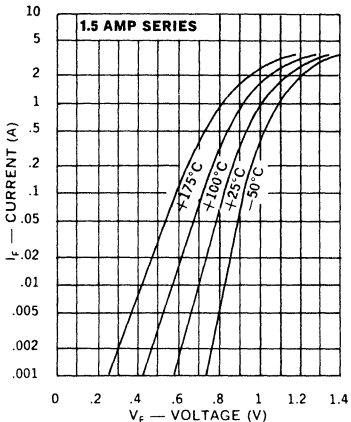
Typical Leakage Current vs. PIV



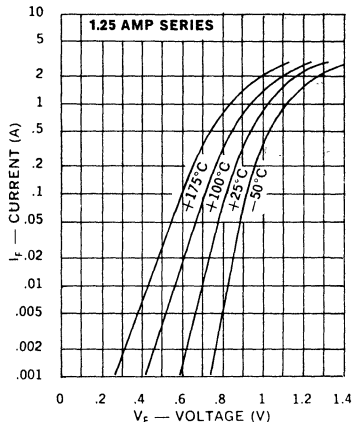
Typical Forward Current vs Forward Voltage



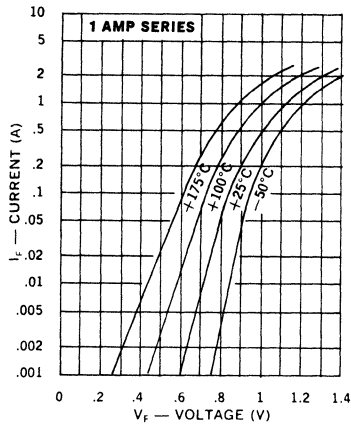
Typical Forward Current vs Forward Voltage



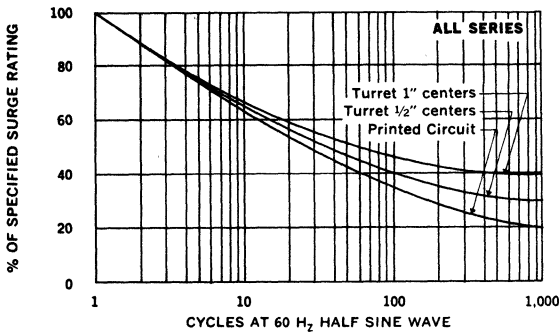
Typical Forward Current vs Forward Voltage



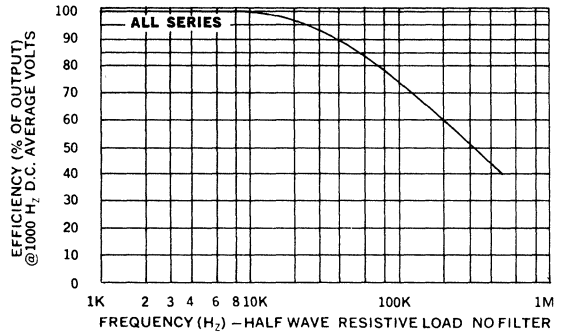
Typical Forward Current vs Forward Voltage



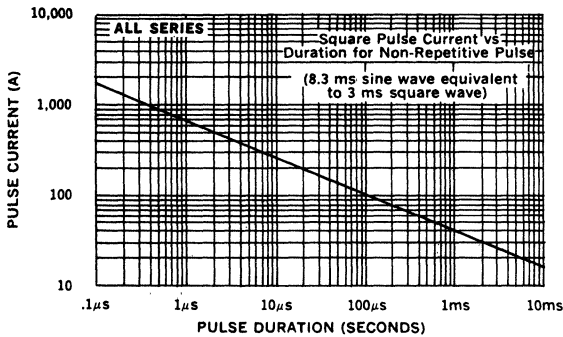
Allowable Forward Surge vs Number of Cycles



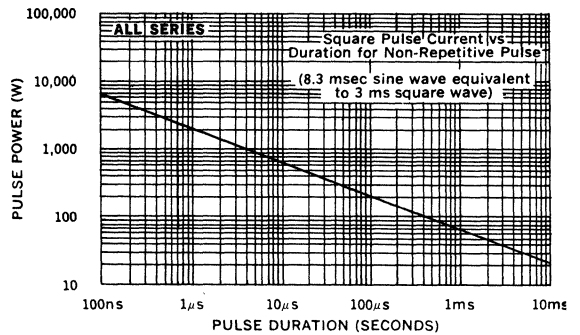
Efficiency vs Frequency at Rated Current (Sine Wave)



Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



RECTIFIERS

Standard Recovery, 2 Amp to 4 Amp

UT2005-UT2060
 UT3005-UT3060
 UT4005-UT4060

FEATURES

- Continuous Rating: to 4A
- Controlled Avalanche
- Surge Rating: to 100A
- PIV: to 600 V
- Miniature Package

DESCRIPTION

High average power and surge capability make these series of devices attractive in many high-rel applications.

All Unitorde rectifiers have a sleeve of pure hard glass fused to the silicon junction. Since the silicon sees only this glass, electrical characteristics are permanently stable. This voidless, monolithic package is totally unaffected by the most severe moisture or temperature testing.

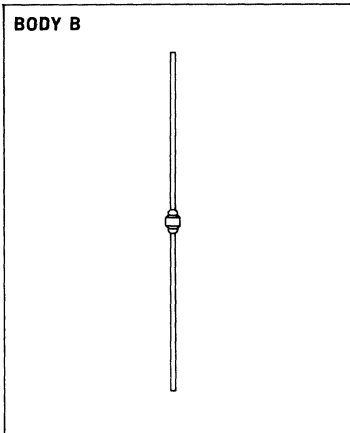
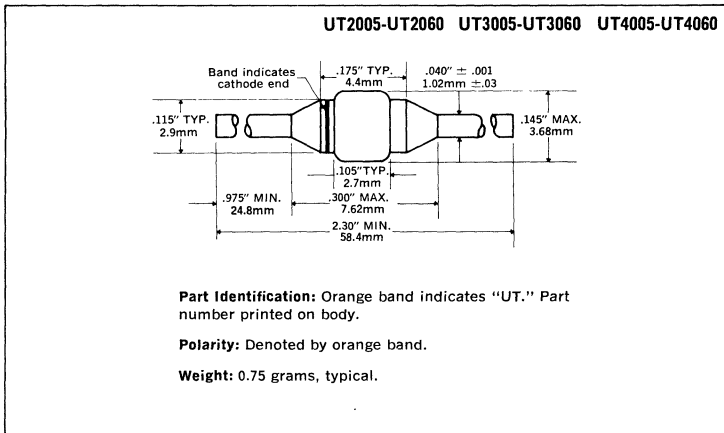
6

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	2 Amp Series	3 Amp Series	4 Amp Series
50V	UT2005	UT3005	UT4005
100V	UT2010	UT3010	UT4010
200V	UT2020	UT3020	UT4020
400V	UT2040	UT3040	UT4040
600V	UT2060	UT3060	UT4060

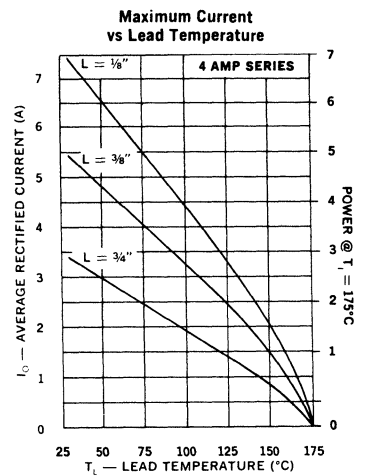
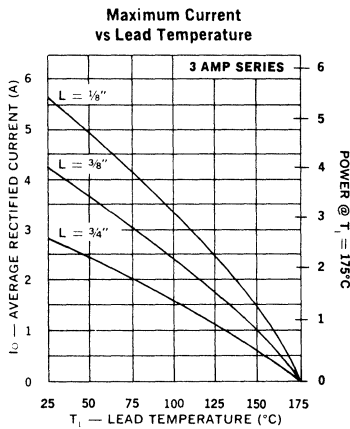
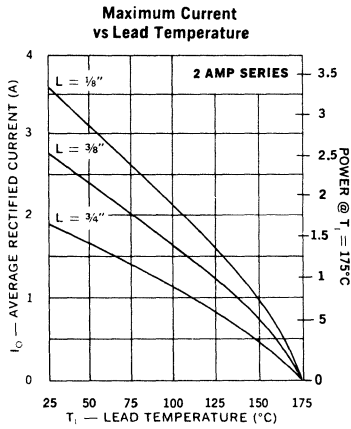
	2 AMP SERIES	3 AMP SERIES	4 AMP SERIES
Maximum Average D.C. Output Current			
@ $T_A = 25^\circ\text{C}$	2.0A	3.0A	4.0A
@ $T_A = 100^\circ\text{C}$	1.0A	1.5A	2.0A
Non-Repetitive Sinusoidal			
Surge Current (8.3ms)	60A	80A	100A
Operating Temperature Range	-195°C to +175°C		
Storage Temperature Range	-195°C to +200°C		
Thermal Resistance	See lead temperature derating curve		

MECHANICAL SPECIFICATIONS

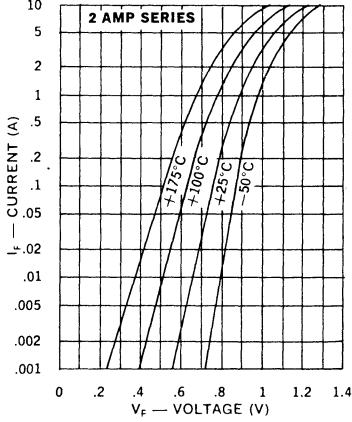


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

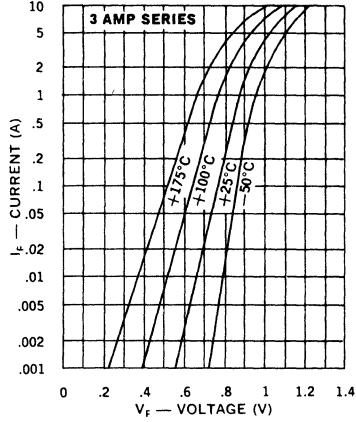
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV	
			25°C	100°C
UT4005 UT4010 UT4020 UT4040 UT4060	50V 100V 200V 400V 600V	1V @ 3A	5μA	100μA
UT3005 UT3010 UT3020 UT3040 UT3060	50V 100V 200V 400V 600V	1V @ 2A	5μA	100μA
UT2005 UT2010 UT2020 UT2040 UT2060	50V 100V 200V 400V 600V	1V @ 1A	5μA	100μA



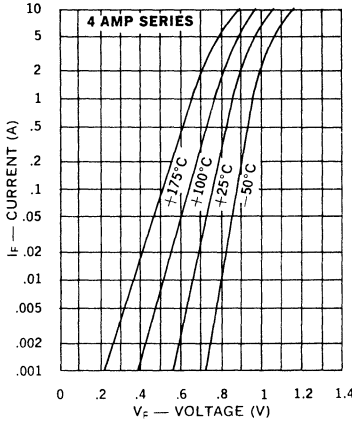
Typical Forward Current vs Forward Voltage



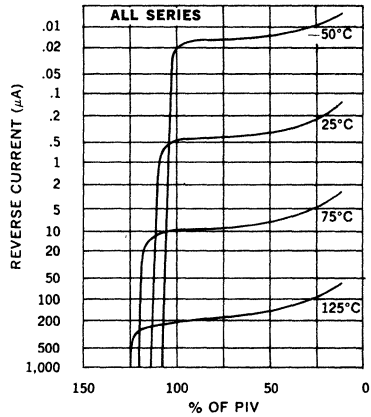
Typical Forward Current vs Forward Voltage

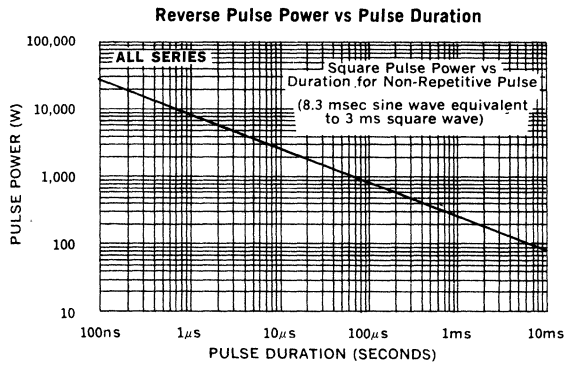
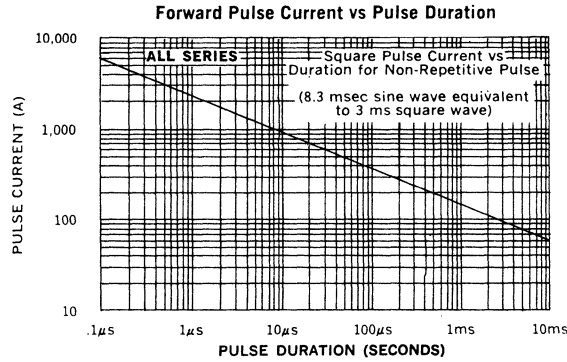
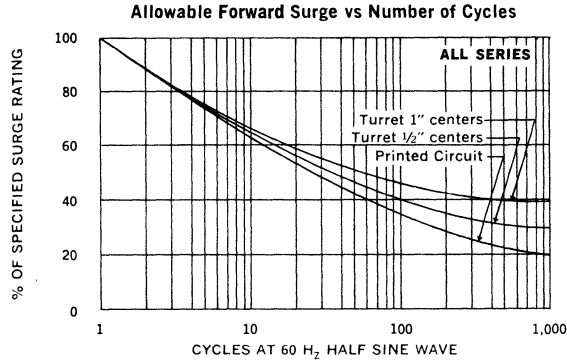


Typical Forward Current vs Forward Voltage



Typical Reverse Current vs PIV





RECTIFIERS

Standard Recovery, 7.5 Amp to 12 Amp

UT5105-UT5160
UT6105-UT6160
UT8105-UT8160

FEATURES

- Rating: 12A
- Controlled Avalanche
- Miniature Package
- Surge Rating: 200A

DESCRIPTION

These series of high current rectifiers offers opportunity for size and weight reduction in high power supplies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	12 Amp Series	9 Amp Series	7.5 Amp Series
50V	UT8105	UT6105	UT5105
100V	UT8110	UT6110	UT5110
200V	UT8120	UT6120	UT5120
400V	UT8140	UT6140	UT5140
600V	UT8160	UT6160	UT5160

	12 AMP SERIES	9 AMP SERIES	7.5 AMP SERIES
Maximum Average D.C. Output Current @ $T_C = 100^\circ\text{C}$	12.0A	9.0A	7.5A
Non-Repetitive Sinusoidal Surge Current (8.3ms)	200A	175A	150A
Operating and Storage Temperature Range	-65°C to +175°C		
Thermal Resistance, Junction to Case	7.5°C/Watt		
Current Derating	See current vs. case temperature curve		

MECHANICAL SPECIFICATIONS

UT5105-UT5160 UT6105-UT6160 UT8105-UT8160

Part Identification: Numerals and polarity letter indicate "UT" type number; e.g., 8105R.

Polarity: Cathode to Stud is standard. Reverse polarity denoted by "R" Suffix.

Finish: Metal parts gold plated per MIL-G-45204, Type II.

Max. Weight: 1.5 grams.

Also available with insulated stud. Reference Design Note-17.

BODY C — Stud Mount

Installation

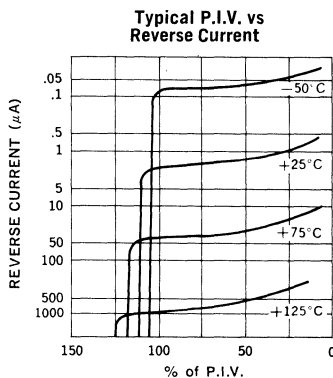
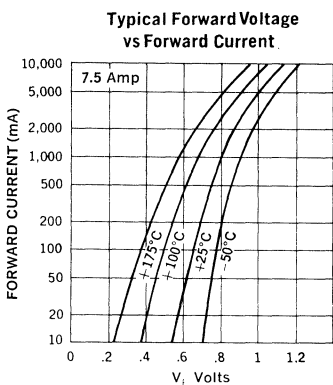
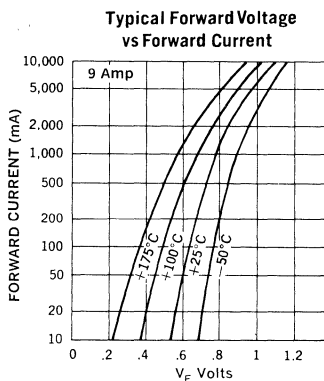
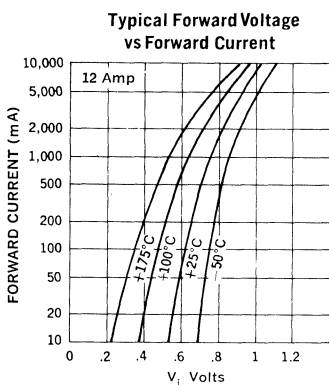
Maximum unlubricated stud torque: 28 inch-ounces.
Insulating hardware supplied.

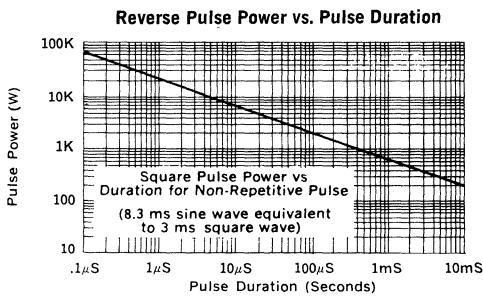
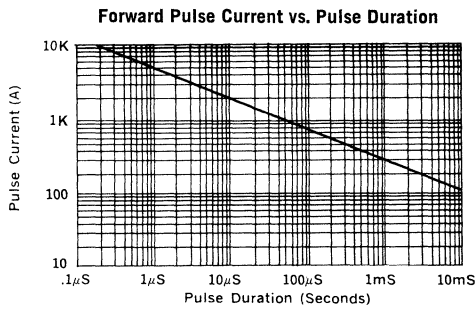
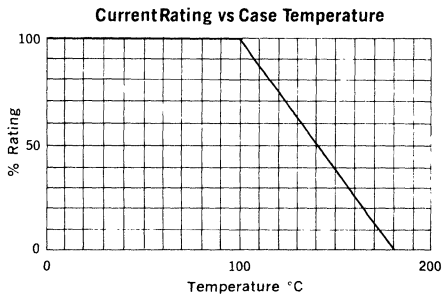
Do not use a screwdriver in the turret slot for installation purposes, or damage may result.

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ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Maximum Forward Voltage	Max. Reverse Current at PIV	
			25°C	100°C
UT8105 UT8110 UT8120 UT8140 UT8160	50V 100V 200V 400V 600V	1V @ 8A	10μA	300μA
UT6105 UT6110 UT6120 UT6140 UT6160	50V 100V 200V 400V 600V	1V @ 6A	10μA	300μA
UT5105 UT5110 UT5120 UT5140 UT5160	50V 100V 200V 400V 600V	1V @ 5A	10μA	300μA





RECTIFIERS

Fast Recovery, 0.5 Amp to 2 Amp

UTR10-UTR60
UTR01-UTR61
UTR02-UTR62

FEATURES

- Continuous Rating: to 2A
- Controlled Avalanche
- Surge Rating: to 25A
- Fast Recovery 40kHz Operation
- PIV: to 600V
- Miniature Package

DESCRIPTION

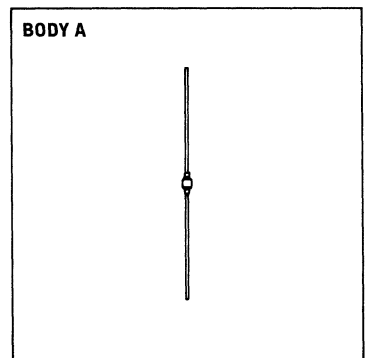
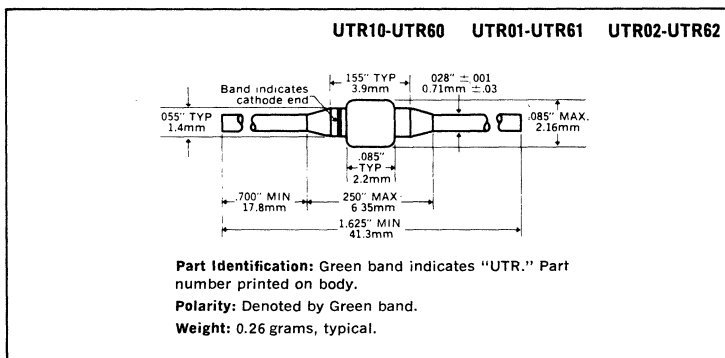
These miniature fast recovery rectifiers permit operation at full frequencies as high as 4JkHz square wave. They have the unique Unitrode Fused in Glass construction.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	½ Amp Series	1 Amp Series	2 Amp Series
50V		UTR01	UTR02
100V	UTR10	UTR11	UTR12
200V	UTR20	UTR21	UTR22
300V	UTR30	UTR31	UTR32
400V	UTR40	UTR41	UTR42
500V	UTR50	UTR51	UTR52
600V	UTR60	UTR61	UTR62

	½ AMP SERIES	1 AMP SERIES	2 AMP SERIES
Maximum Average D.C. Output Current			
@ $T_A = 25^\circ\text{C}$	0.5A	1.0A	2.0A
@ $T_A = 100^\circ\text{C}$	0.25A	0.5A	1.0A
Non-Repetitive Sinusoidal			
Surge Current (8.3ms)	15A	20A	25A
Operating Temperature Range	-195°C to +175°C		
Storage Temperature Range	-195°C to +200°C		
Thermal Resistance	See lead temperature derating curves		

MECHANICAL SPECIFICATIONS

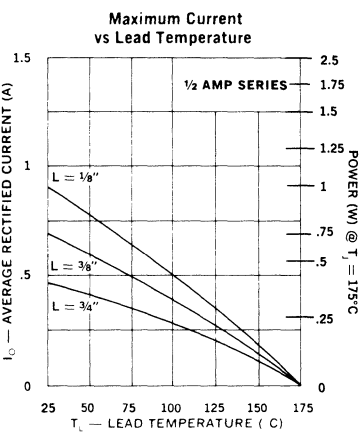
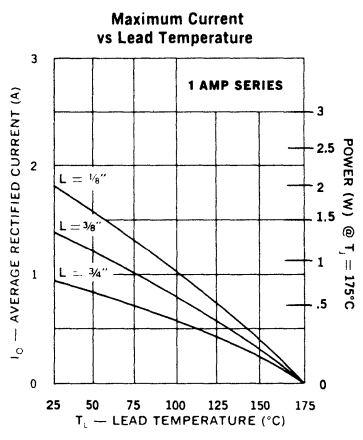
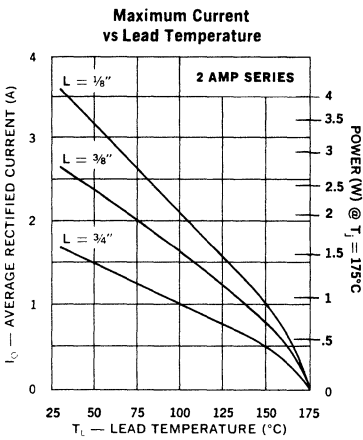


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

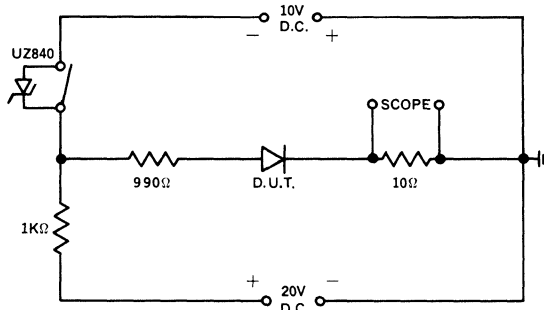
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV		Maximum Reverse Recovery Time*	Maximum Junction Capacitance @ 25°C	
			25°C	100°C		0V	-10V
UTR02	50V	1.1V @ 1000mA	3μA	100μA	250ns	150pf	60pf
UTR12	100V				250ns	100pf	40pf
UTR22	200V				250ns	80pf	32pf
UTR32	300V				300ns	70pf	28pf
UTR42	400V				350ns	60pf	24pf
UTR52	500V				400ns	50pf	20pf
UTR62	600V				400ns	40pf	16pf
UTR01	50V	1.1V @ 500mA	3μA	100μA	250ns	150pf	60pf
UTR11	100V				250ns	100pf	40pf
UTR21	200V				250ns	80pf	32pf
UTR31	300V				300ns	70pf	28pf
UTR41	400V				350ns	60pf	24pf
UTR51	500V				400ns	50pf	20pf
UTR61	600V				400ns	40pf	16pf
UTR10	100V	1.1V @ 200mA	3μA	100μA	250ns	100pf	40pf
UTR20	200V				250ns	80pf	32pf
UTR30	300V				300ns	70pf	28pf
UTR40	400V				350ns	60pf	24pf
UTR50	500V				400ns	50pf	20pf
UTR60	600V				400ns	40pf	16pf



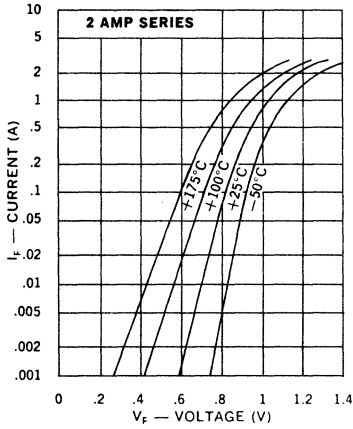
*Recovery time is measured from 10.0mA to 10.0mA recovery to 5.0mA



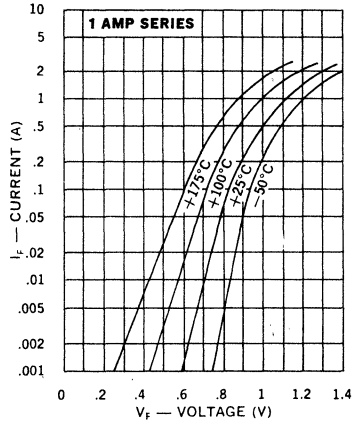
Reverse-Recovery Circuit



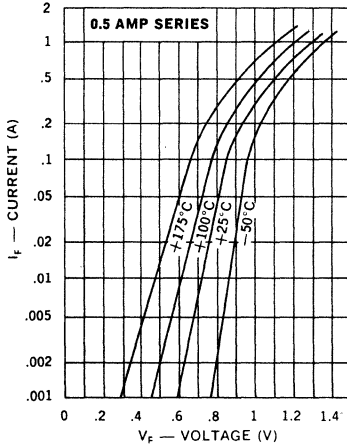
Typical Forward Current vs Forward Voltage



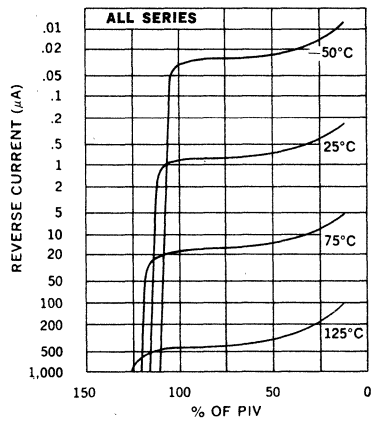
Typical Forward Current vs Forward Voltage



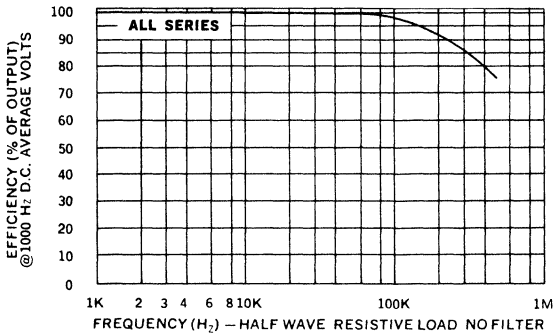
Typical Forward Current vs Forward Voltage



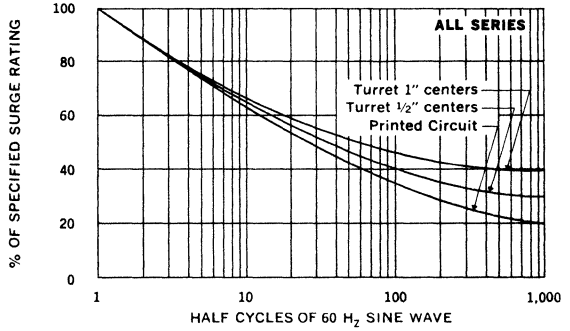
Typical Reverse Current vs PIV



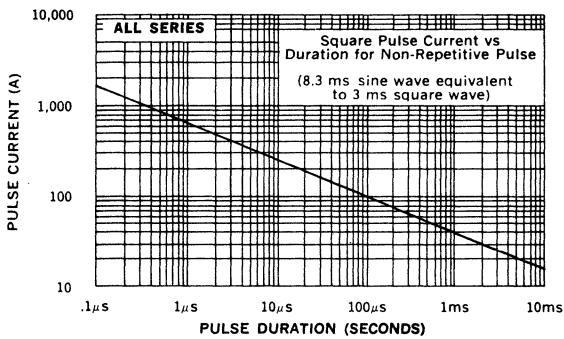
Efficiency vs Frequency at Rated Current (Sine Wave)



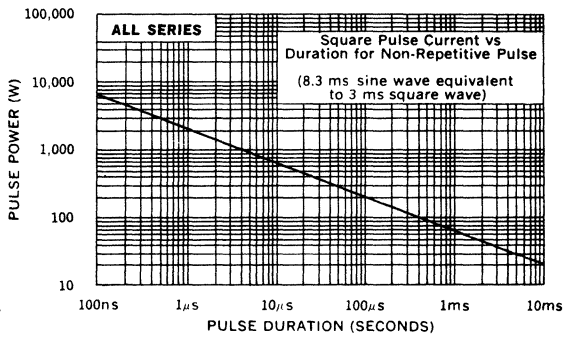
Allowable Forward Surge vs Number of Cycles



Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



RECTIFIERS

Fast Recovery, 2 Amp to 4 Amp

UTR2305-UTR2360
 UTR3305-UTR3360
 UTR4305-UTR4360

FEATURES

- Continuous Rating: to 4A
- Controlled Avalanche
- Surge Rating: to 100A
- PIV: to 600V
- Miniature Package

DESCRIPTION

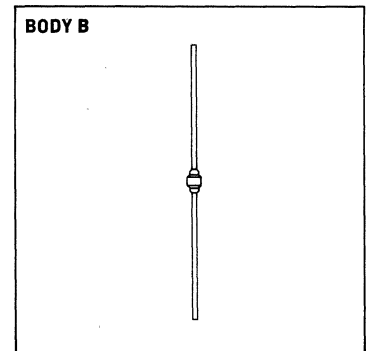
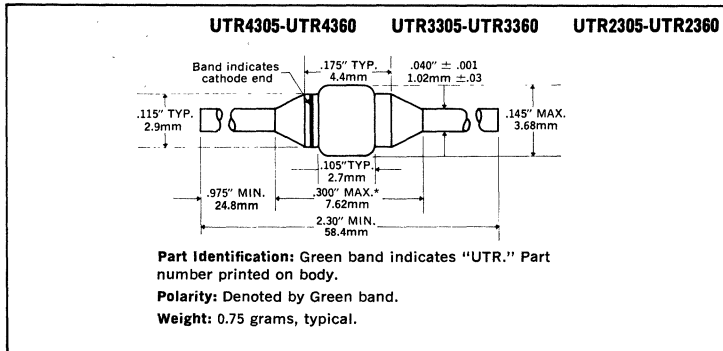
Small size and high surge capability make this series of power switching rectifiers desirable for power supplies where size, weight and reliability are important.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	2 Amp Series	3 Amp Series	4 Amp Series
50V	UTR2305	UTR3305	UTR4305
100V	UTR2310	UTR3310	UTR4310
200V	UTR2320	UTR3320	UTR4320
400V	UTR2340	UTR3340	UTR4340
500V	UTR2350	UTR3350	UTR4350
600V	UTR2360	UTR3360	UTR4360

	2 AMP SERIES	3 AMP SERIES	4 AMP SERIES
Maximum Average D.C. Output Current			
@ $T_A = 25^\circ\text{C}$	2.0A	3.0A	4.0A
@ $T_A = 100^\circ\text{C}$	1.0A	1.5A	2.0A
Non-Repetitive Sinusoidal			
Surge Current (8.3ms)	60A	80A	100A
Operating Temperature Range	-195°C to +175°C		
Storage Temperature Range	-195°C to +200°C		
Thermal Resistance	See lead temperature derating curve		

MECHANICAL SPECIFICATIONS

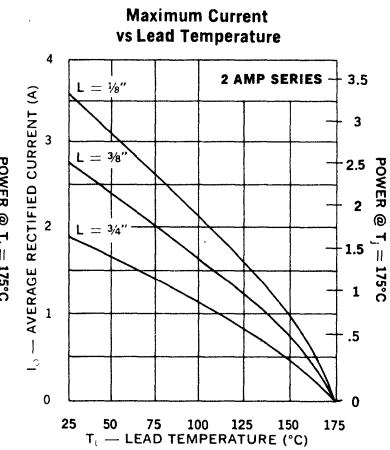
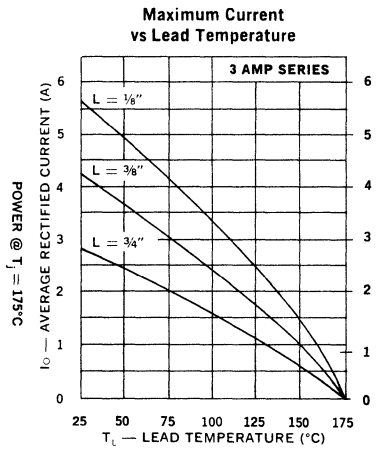
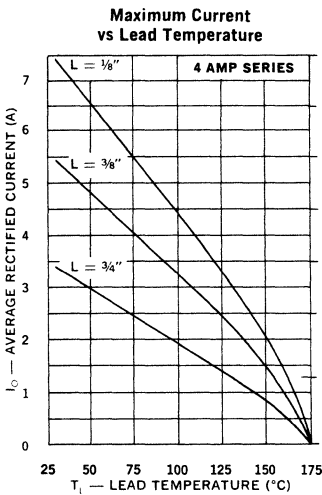


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

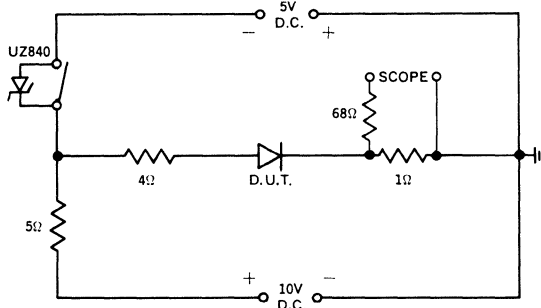
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV		Maximum Reverse Recovery Time*	Maximum Junction Capacitance @ 25°C	
			25°C	100°C		0V	-10V
UTR4305	50V	1.1V @ 4A	5μA	100μA	250ns	600pf	240pf
UTR4310	100V				250ns	400pf	160pf
UTR4320	200V				250ns	320pf	128pf
UTR4340	400V				400ns	240pf	96pf
UTR4350	500V				400ns	200pf	80pf
UTR4360	600V				400ns	160pf	64pf
UTR3305	50V	1.1V @ 3A	5μA	100μA	250ns	600pf	240pf
UTR3310	100V				250ns	400pf	160pf
UTR3320	200V				250ns	320pf	128pf
UTR3340	400V				300ns	240pf	96pf
UTR3350	500V				350ns	200pf	80pf
UTR3360	600V				400ns	160pf	64pf
UTR2305	50V	1.1V @ 2A	5μA	100μA	250ns	600pf	240pf
UTR2310	100V				250ns	400pf	160pf
UTR2320	200V				250ns	320pf	128pf
UTR2340	400V				300ns	240pf	96pf
UTR2350	500V				350ns	200pf	80pf
UTR2360	600V				400ns	160pf	64pf

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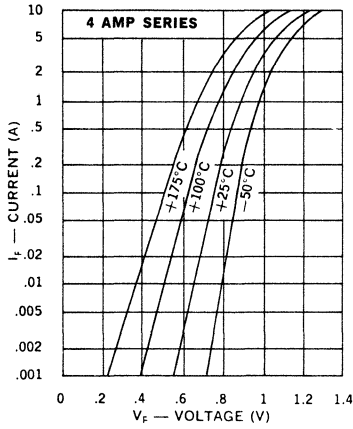
*Recovery time is measured from 1A to 1A recovering to 0.5A.



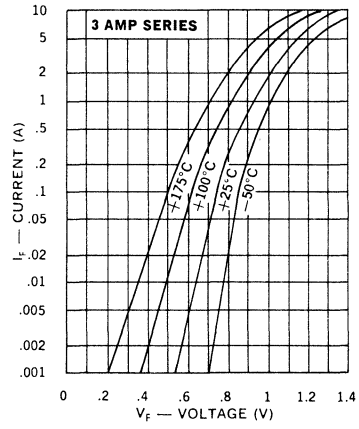
Reverse Recovery Circuit



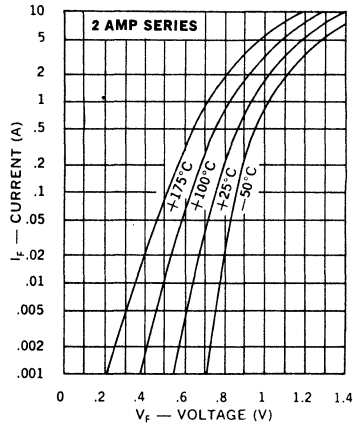
Typical Forward Current vs Forward Voltage



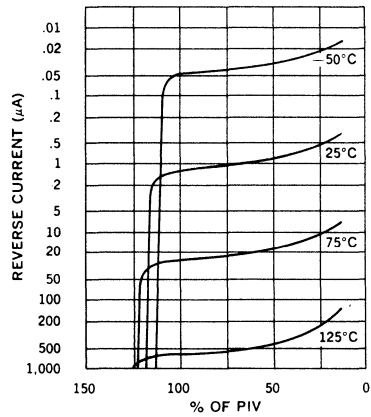
Typical Forward Current vs Forward Voltage



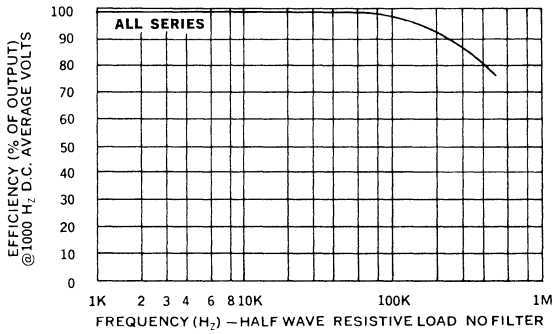
Typical Forward Current vs Forward Voltage



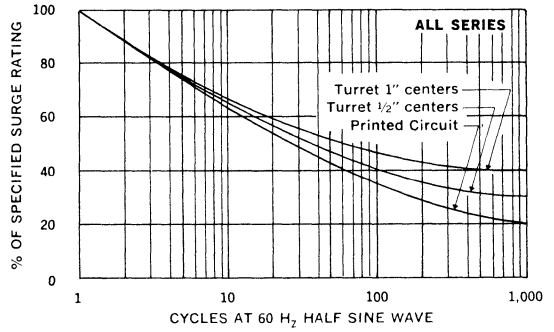
Typical Reverse Current vs PIV



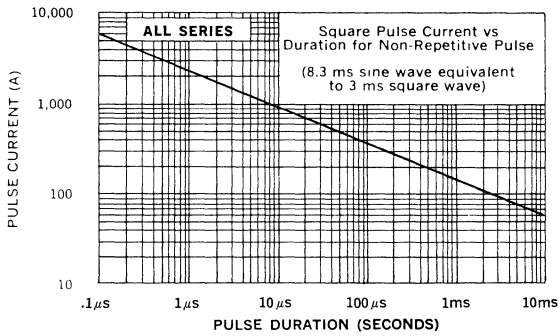
Efficiency vs Frequency at Rated Current (Sine Wave)



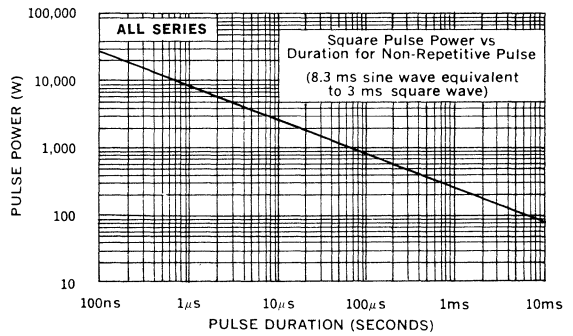
Allowable Forward Surge vs Number of Cycles



Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



RECTIFIERS

Fast Recovery, 6 Amp to 9 Amp

UTR4405-UTR4440
UTR5405-UTR5440
UTR6405-UTR6440

FEATURES

- Continuous Rating: to 9A
- Controlled Avalanche
- Surge Rating: to 150A
- Fast Recovery, 40kHz Operation
- PIV: to 400V
- Miniature Package

DESCRIPTION

The same basic construction as all Unitorde diodes, but using a miniature stud mounting and larger junction area, provides a 9 Amp continuous and 150 Amp surge rating in a package only one fifth the weight and one quarter the volume of conventional types.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	6 Amp Series	7.5 Amp Series	9 Amp Series
50V	UTR4405	UTR5405	UTR6405
100V	UTR4410	UTR5410	UTR6410
200V	UTR4420	UTR5420	UTR6420
400V	UTR4440	UTR5440	UTR6440

	6 AMP SERIES	7.5 AMP SERIES	9.0 AMP SERIES
Maximum Average D.C. Output Current @ $T_C = 100^\circ\text{C}$	6.0A	7.5A	9.0A
Non-Repetitive Sinusoidal Surge Current (8.3ms)	120A	135A	150A
Operating Temperature Range	-195°C to +175°C		
Storage Temperature Range	-195°C to +200°C		
Thermal Resistance	7.5°C/W		

MECHANICAL SPECIFICATIONS

UTR6405-UTR6440 UTR5405-UTR5440 UTR4405-UTR4440

Part Identification: Numerals and polarity letter indicate UTR type number, e.g., UTR 4405.

Polarity: Cathode to Stud is standard. Reverse polarity denoted by "R" suffix.

Finish: Metal parts gold plated per MIL-G-45204, Type II.

Weight: 1.5 grams, typical.

Also available with insulated stud. Reference Design Note-17.

BODY C — Stud Mount

Installation

Maximum unlubricated stud torque: 28 inch-ounces.
Insulating hardware supplied.

Do not use a screwdriver in the turret slot for installation purposes, or damage may result.

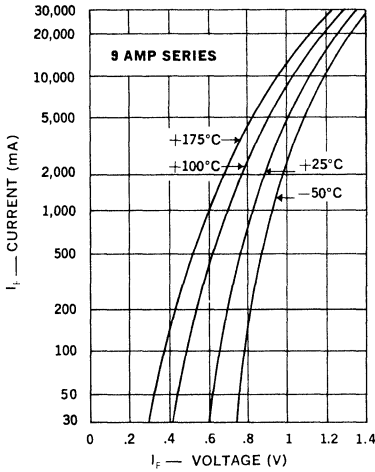
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	PIV	Maximum Forward Voltage Drop	Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*
			25°C	100°C	
UTR6405	50V	1.1V @ 6.0A	10μA	300μA	300ns
UTR6410	100V				300ns
UTR6420	200V				400ns
UTR6440	400V				500ns
UTR5405	50V	1.1V @ 5.0A	10μA	300μA	300ns
UTR5410	100V				300ns
UTR5420	200V				400ns
UTR5440	400V				500ns
UTR4405	50V	1.1V @ 4.0A	10μA	300μA	300ns
UTR4410	100V				300ns
UTR4420	200V				400ns
UTR4440	400V				500ns

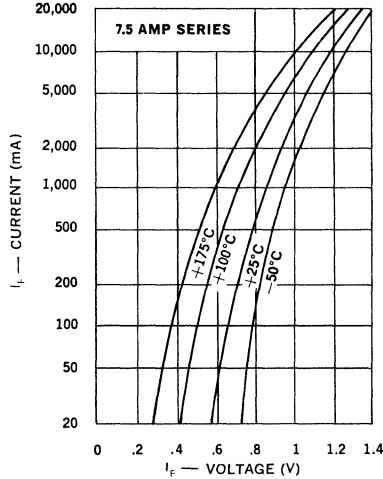
*Recovery time is measured from 1A to 1A, recovering to 0.5A.



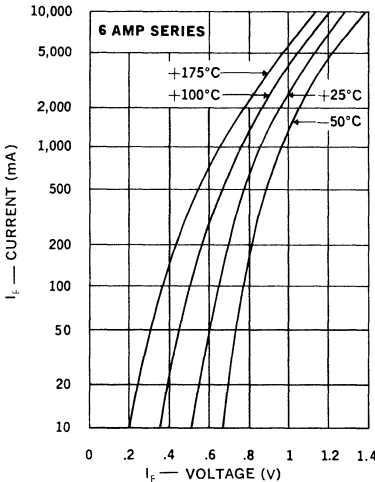
Typical Forward Voltage vs Forward Current



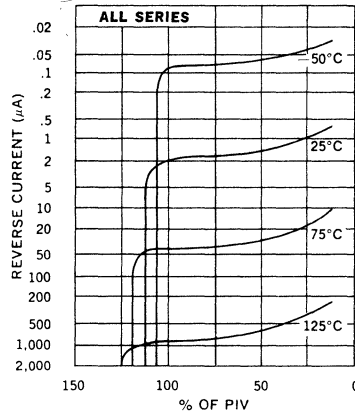
Typical Forward Voltage vs Forward Current



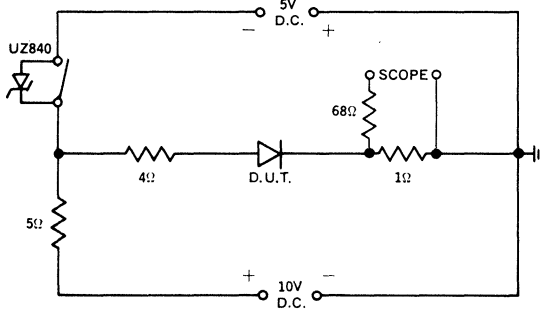
Typical Forward Voltage vs Forward Current



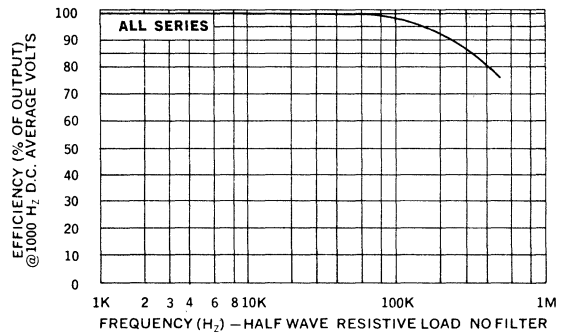
Typical Reverse Current vs PIV



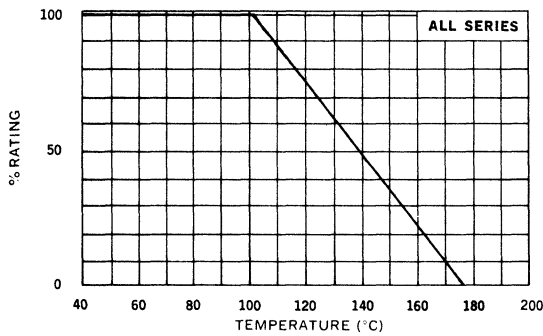
Reverse Recovery Circuit



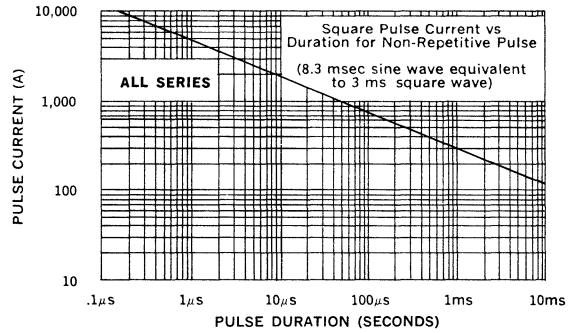
Efficiency vs Frequency at Rated Current (Sine Wave)



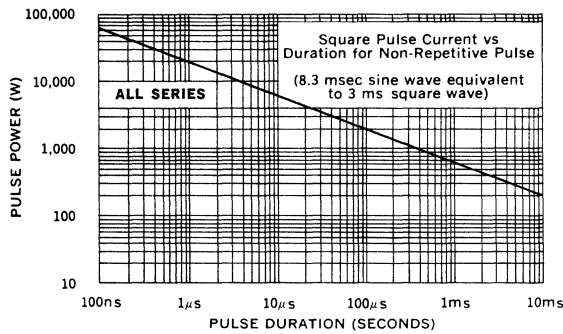
Current Rating vs Case Temperature



Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



RECTIFIERS

Ultra-Fast Recovery, 1 Amp and 2 Amp

UTX105-UTX125
UTX205-UTX225

FEATURES

- Continuous Rating: to 2A
- Controlled Avalanche
- Surge: to 25A
- Recovery Time less than 75ns
- Miniature Package

DESCRIPTION

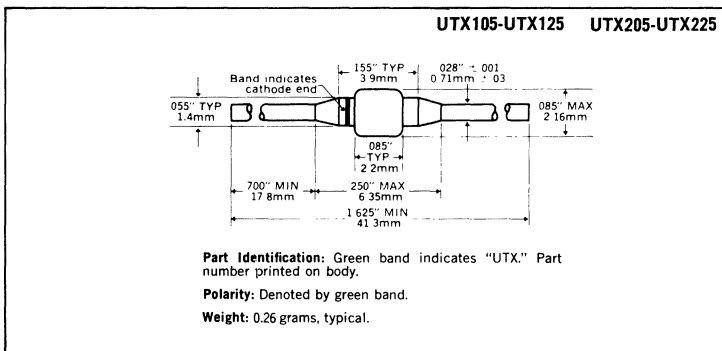
These miniature ultra-fast recovery rectifiers permit operation at full power at frequencies as high as 100kHz square wave. They may be used as half wave rectifiers or as legs of a bridge.

ABSOLUTE MAXIMUM RATINGS

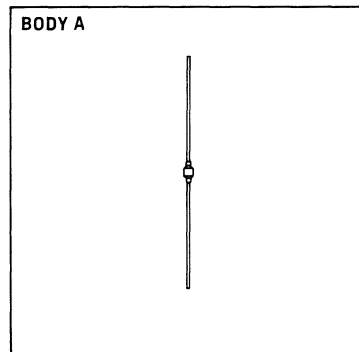
Peak Inverse Voltage	1 Amp Series	2 Amp Series
50V	UTX105	UTX205
100V	UTX110	UTX210
150V	UTX115	UTX215
200V	UTX120	UTX220
250V	UTX125	UTX225

Maximum Average D.C. Output Current	1 AMP SERIES	2 AMP SERIES
@ $T_A = 25^\circ\text{C}$	1.0A	2.0A
@ $T_A = 100^\circ\text{C}$	0.5A	1.0A
Non-Repetitive Sinusoidal		
Surge Current (8.3ms)	20A	25A
Operating Temperature Range	-195°C to +175°C	
Storage Temperature Range	-195°C to +200°C	
Thermal Resistance	See Lead Temperature Derating Curve	

MECHANICAL SPECIFICATIONS



BODY A

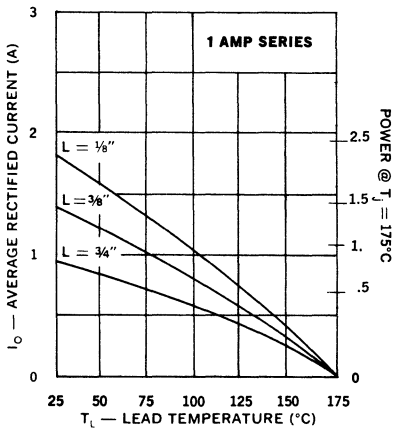


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

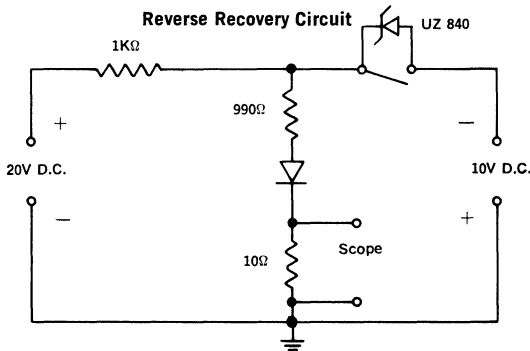
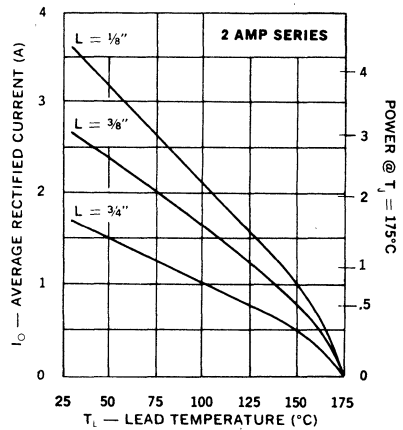
Type	PIV	Maximum Voltage Forward Drop	Leakage Current @ PIV		Max. Reverse Recovery Time*
			25°C	100°C	
UTX 205 UTX 210 UTX 215 UTX 220 UTX 225	50V 100V 150V 200V 250V	1.0V @ 1 Adc	3μA	50μA	75ns
UTX 105 UTX 110 UTX 115 UTX 120 UTX 125	50V 100V 150V 200V 250V	1.0V @ 0.5 Adc	3μA	50μA	75ns

*Recovery time is measured from 10.0mA to 10.0mA recovery to 5.0mA.

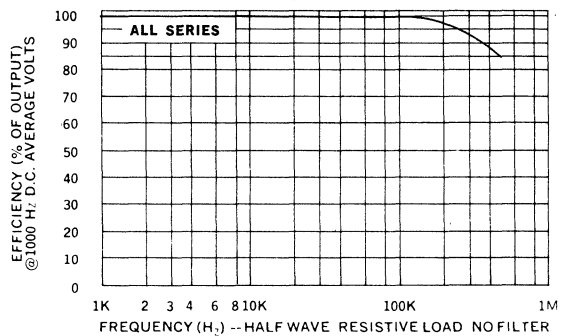
Maximum Current vs Lead Temperature



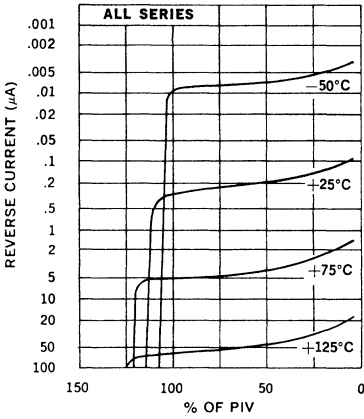
Maximum Current vs Lead Temperature



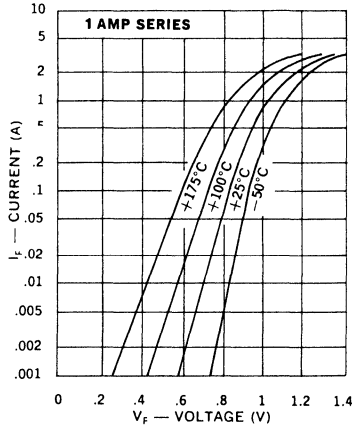
Efficiency vs Frequency at Rated Current (Sine Wave)



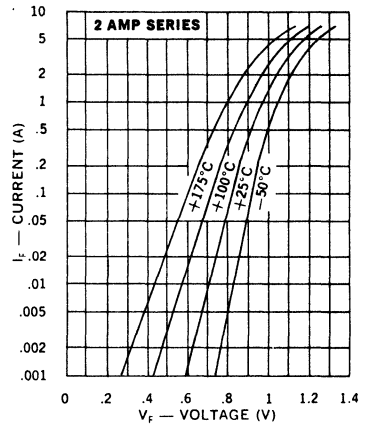
Typical Leakage Current vs. PIV



Typical Forward Current vs Forward Voltage

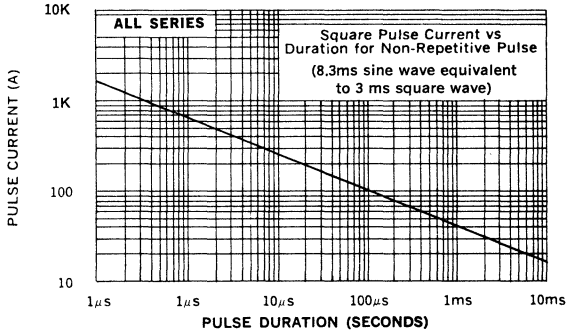


Typical Forward Current vs Forward Voltage

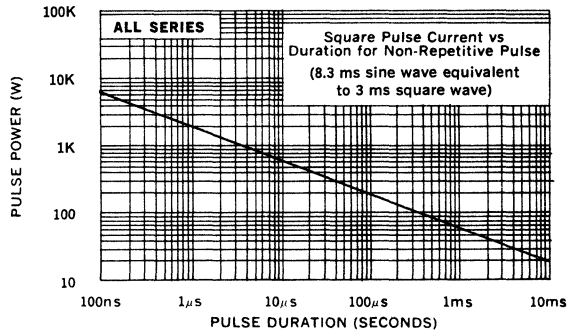


6

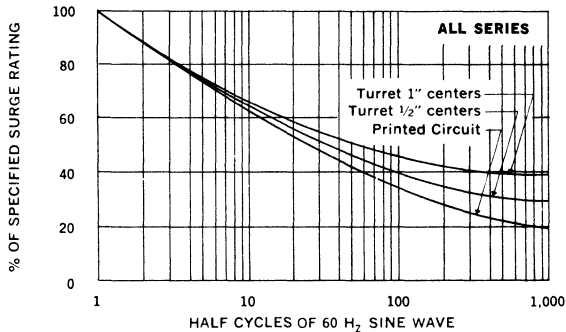
Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



Allowable Forward Surge vs Number of Cycles



RECTIFIERS

Ultra-Fast Recovery, 3 Amp and 4 Amp

UTX 3105-UTX 3120
UTX 4105-UTX 4120

FEATURES

- Continuous Rating: to 4A
- Controlled Avalanche
- Surge: to 80A
- Recovery Time less than 100ns
- Miniature Package

DESCRIPTION

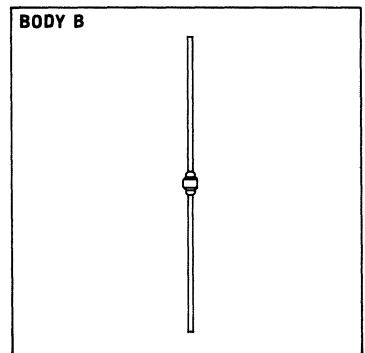
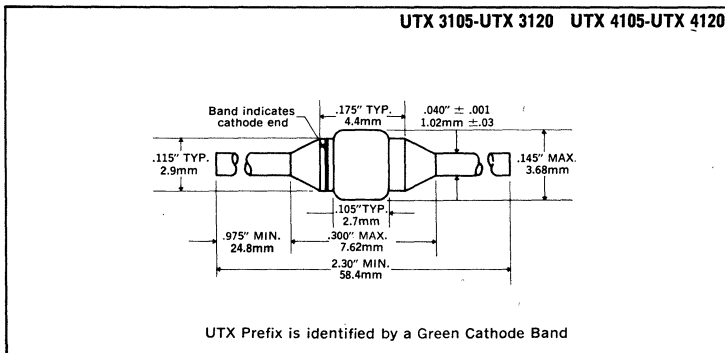
These miniature ultra-fast recovery rectifiers permit operation at full power at frequencies as high as 100kHz square wave. They have the same unique Unitrode construction as the familiar 2 amp UTX series, but are scaled up in size to provide higher continuous and surge current capability.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	3 Amp Series	4 Amp Series
50V	UTX 3105	UTX 4105
100V	UTX 3110	UTX 4110
150V	UTX 3115	UTX 4115
200V	UTX 3120	UTX 4120

	3 AMP SERIES	4 AMP SERIES
Maximum Average D.C. Output Current		
@ $T_A = 25^\circ\text{C}$	3.0A	4.0A
@ $T_A = 100^\circ\text{C}$	1.5A	2.0A
Non-Repetitive Sinusoidal		
Surge Current (8.3ms)	60A	80A
Operating Temperature Range	-195°C to +175°C	
Storage Temperature Range	-195°C to +200°C	
Thermal Resistance	See Lead Temperature Derating Curve	

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

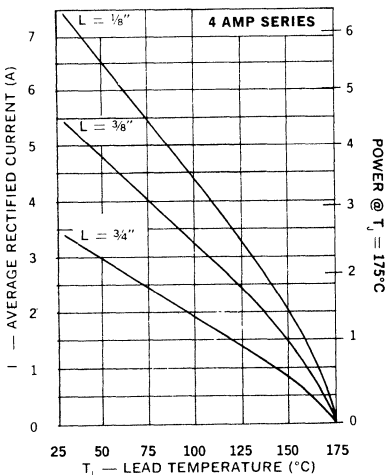
Type	PIV	Maximum Forward Voltage Drop*	Maximum Leakage Current @ PIV		Maximum Reverse Recovery Time**
			25°C	100°C	
UTX 4105	50V	1V @ 3 Adc	5μA	75μA	100ns
UTX 4110	100V				
UTX 4115	150V				
UTX 4120	200V				
UTX 3105	50V	1V @ 2 Adc	5μA	75μA	100ns
UTX 3110	100V				
UTX 3115	150V				
UTX 3120	200V				

*Forward voltage is measured at least 1 second after application of current.

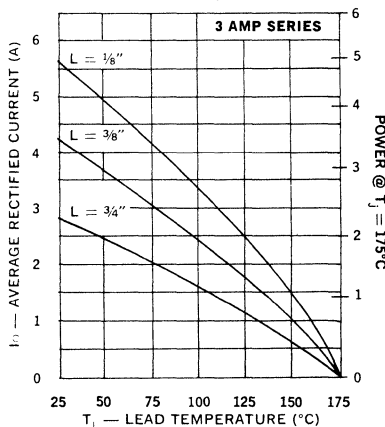
**Recovery time is measured from 1A to 1A recovering to 0.5A.



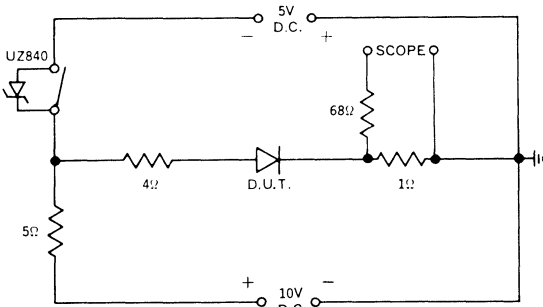
Maximum Current vs Lead Temperature



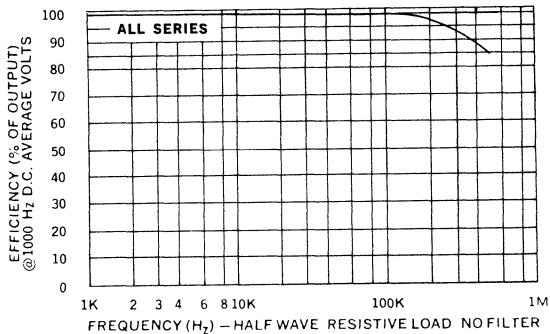
Maximum Current vs Lead Temperature



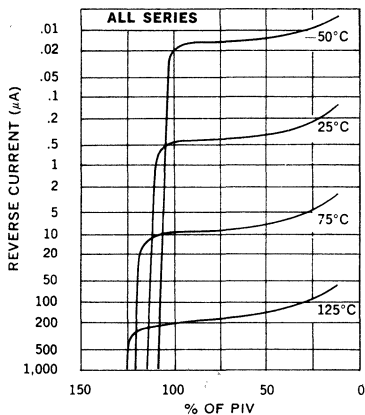
Reverse Recovery Circuit



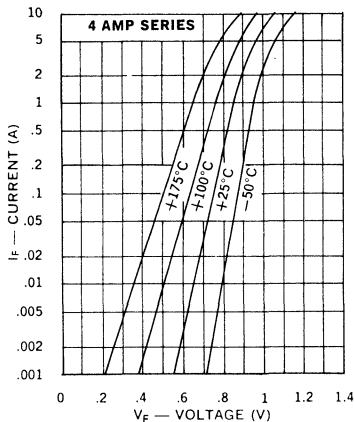
Efficiency vs Frequency at Rated Current (Sine Wave)



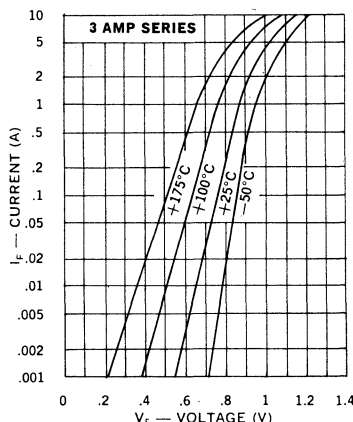
Typical Leakage Current vs PIV



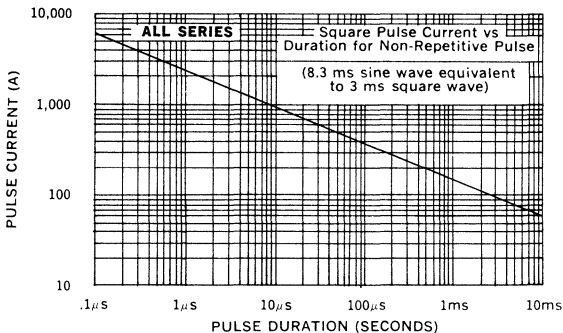
Typical Forward Current vs Forward Voltage



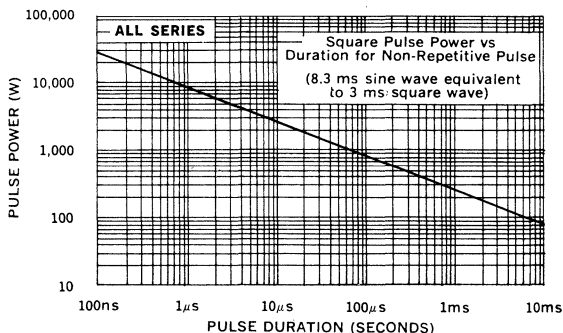
Typical Forward Current vs Forward Voltage



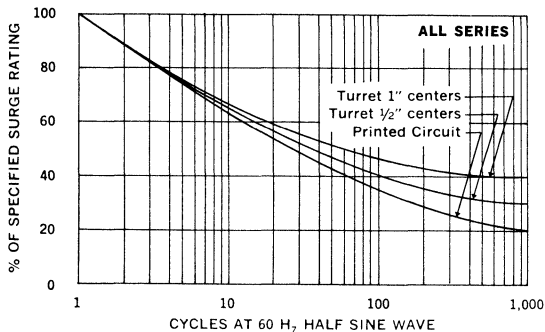
Forward Pulse Current vs Pulse Duration



Reverse Pulse Power vs Pulse Duration



Allowable Forward Surge vs Number of Cycles

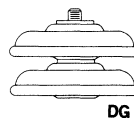
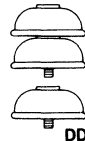
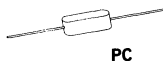


HIGH VOLTAGE RECTIFIERS, RECTIFIER MODULES & MULTIPLIERS

7

HIGH VOLTAGE RECTIFIERS & RECTIFIER MODULES

PRODUCT SELECTION GUIDE

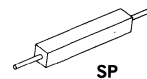
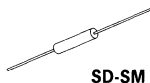


STANDARD RECOVERY

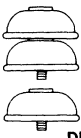
Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT											
	.025-.050A	.050-100A	.100-.250A	.250-.50A	.50-.75A	.75-1A	1-1.5A	1.5-2A	2-2.5A	2.5-5A	5-6A	6-7A
1.0kV			HVE10 SJ HS10 SK 1N3643 SJ			SXS10 SL						
1.2kV							(US12) SA					
1.5kV			HS15 SK HVE15 SJ 1N3644 SJ			SXS15 SL (US15) SA				KXS15 SM		
1.8kV					(US18) SA							
2.0kV			HS20 SK HVE20 SJ 1N3645 SJ		(US20) SA	SXS20 SL				KXS20 SM		
2.5kV			HS25 SK HVE25 SJ 1N3646 SJ		(US25) SB	SXS25 SL	(USB2.5) DH		HVHS 2500 PC	KXS25 SM (UDB2.5) DD	(UDE2.5) DD	(UGE2.5) DG
3.0kV			HS30 SK HVE30 SJ 1N3647 SJ			SXS30 SL (US30) SB				KXS30 SM		
3.5kV				(US35) SC								
4.0kV		HS40 SK HVE40 SJ 1N5181 SJ		(US40) SC	SXS40 SL					KXS40 SM		
4.5kV				(US45A) SD								

Parentheses () designates product using fused-in-glass single chip rectifiers; all others use stacked chips.

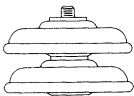
HIGH VOLTAGE RECTIFIERS & RECTIFIER MODULES



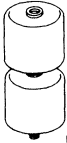
Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT											
	0.50-100A	100-250A	250-50A	.50-.75A	.75-1A	1-1.5A	1.5-2A	2-2.5A	2.5-3A	3-4A	4-5A	5-6A
5.0kV	HS50 SK HVE50 SJ 1N5182 SJ		HVH 5000 PB HVHF 5000 PB (US50A) SD	SXS50 SL (USB5) DH (USS5) DH			(UDA5) DD (UDB5) DD (1N5600)* DE	KXS50 SM HVHS 5000 PC			(UDE5) DG (UGB5) DD	(UGE5) DG (1N5603)* DF
6.0kV			SXS60 SL (US60A) SD			KXS60 SM						
7.0kV			(US70A) SD									
7.5kV	HS75 SK HVF75 SJ 1N5183 SJ		HVH 7500 PB HVHF 7500 PB (USS7.5) DH	(USB7.5) DH		(UDA7.5) DD (UDB7.5) DD		HVHS 7500 PC	(UGB7.5) DG	(UGE7.5) DG		
8.0kV		(US80A) SE	SXS80 SL			KXS80 SM						
10kV	HS100 SK HVE100 SJ 1N5184 SJ	(US100A) SE	HVH 10000 PB HVHF 10000 PB SXS100 SL (USB10) DH (USS10) DH	(688-10) BE	(UDA10) DD * (1N5597) DE	KXS100 SM		HVHS 10000 PC (UGB10) DG				
12kV		(US120A) SE	(688-12) BE									
12.5kV			HVH 12500 PB HVHF 12500 PB					HVHS 12500 PC				



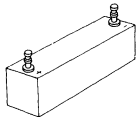
DD DE



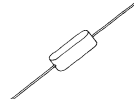
DF, DG



DH



BE



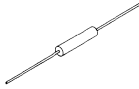
PA PC

STANDARD RECOVERY

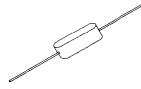
Peak Inverse Voltage	AVERAGE D. C. OUTPUT CURRENT					
	.025-.050A	.050-.100A	.100-.250A	.250-.50A	.50-.75A	2-2.5A
15kV	HVHJ 15K PA		(US150A) SF (USS15) DH	HVH 15000 PB HVHF 15000 PB (688-15) BE	(UDA15) DD	HVHS 15000 PC
17.5kV						HVHS 17500 PC
18kV			(US180A) SF	(688-18) BE		
20kV	HVHJ 20K PA		(US200A) SF	HVH 20000 PB HVHF 20000 PB (688-20) BE		HVHS 20000 PC
22.5kV	HVHJ 22.5K PA					
25kV	HVHJ 25K PA		(688-25) BE	HVH 25000 PB HVHF 25000 PB		
30kV	HVHJ 30K PA					
35kV	HVHJ 35K PA					
37.5kV	HVHJ 37.5K PA					
40kV	HVHJ 40K PA					
45kV	HVHJ 45K PA					
50kV						
60kV						

Parentheses () designates product using fused-in-glass single chip rectifiers; all others use stacked chips.

HIGH VOLTAGE RECTIFIERS & RECTIFIER MODULES



SA-SN

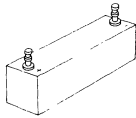


PA-PC

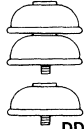
FAST RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT								
	.050-100A	100-250A	250-50A	.50-75A	.75-1.5A	1.5-2A	2-2.5A	2.5-4A	4-6A
1.0kV		HA10* SK HVX10* SJ			SX10* SL				
1.2kV					(USR12) SA				
1.5kV		HA15* SK HVX15 SJ		(USR15) SA	SX15* SL			KX15* SM	
1.8kV				(USR18) SA					
2.0kV		HA20* SK HVX20* SJ		(USR20) SB	SX20* SL			KX20* SM	
2.5kV		HA25* SK HVX25* SJ	HVF 2500 † PB (USR25) SB		SX25* SL (UFB2.5) DH		HVFS 2500 † PC (UDD2.5) DD	KX25* SM	(UDF2.5) DD (UGF2.5) DG
3.0kV		HA30* SK HVX30* SJ	(USR30) SC	SX30* SL			KX30* SM		
3.5kV			(USR35) SC						
4.0kV	HA40* SK HVX40* SJ		(USR40A) SD	SX40* SL			KX40* SM		
4.5kV		(USR45A) SD							
Reverse Recovery Time (Max.)	300ns 250ns*	500ns 250ns*	500ns 250ns†	500ns 250ns*	500ns 250ns*	500ns 250ns	500ns 250ns* 150ns†	250ns*	500ns

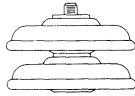
Parentheses () designates product using fused-in-glass single chip rectifiers; all others use stacked chips.



BE



DD



DG



DH

PRODUCT SELECTION GUIDE

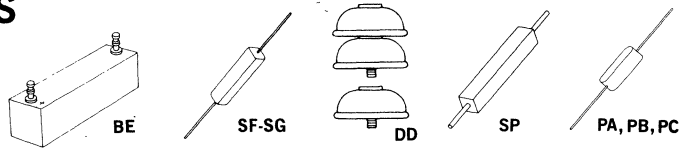
FAST RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT								
	.050-.100A	.100-.250A	.250-.50A	.50-.75A	.75-1A	1-1.5A	1.5-2A	2-2.5A	2.5-4A
5.0kV	HA50 SK MVX50 SJ	(USR50A) SD	HVF 5000† PB (UFS5) DH	SX50* SL (UFB5) DH		(UDC5) DD (UDD5) DD		HVFS 5000† PC KX50* SM	(UDF5) DD (UGD5) DG (UGF5) DG
6.0kV		(USR60A) SD	SX60* SL			KX60* SM			
7.0kV		(USR70A) SE							
7.5kV	HA75 SK HVX75 SJ		HVF 7500† PB (UFB7.5) DH (UFS7.5) DH		(UDC7.5) DD (UDD7.5) DD			HVFS 7500† PC (UGD7.5) DG (UGF7.5) DG	
8.0kV		(USR80A) SE	SX80* SL			KX80* SM			
10kV	HA100 SK HVX100 SJ	(USR100A) SE	HVF 10000† PB SX100* SL (UFS10) DH	(UDC10) DD (688-10R) BE		KX100* SM	(UGD10) DG	HVFS 10000† PC	
12kV		(USR120A) SF	(688-12R) BE						
12.5kV			HVF 12500† PB						HVFS 12500† PC
Reverse Recovery Time (Max.)	250ns	500ns	500ns 250ns* 150ns†	500ns 250ns*	500ns 250ns*	500ns 250ns*	500ns 250ns*	500ns 250ns* 150ns†	500ns

Parentheses () designates product using fused-in-glass single chip rectifiers; all others use stacked chips.



HIGH VOLTAGE RECTIFIERS & RECTIFIER MODULES



FAST RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT					
	025-100A	100-250A	250-75A	75-1.5A	1.5-2A	2-2.5A
15kV	HVJX 15K PA	(USR150A) SF	HVF 15000 [†] PB (UDC15) DD (688-15R) BE			HVFS 15000 PC
17.5kV						HVFS 17500 PC
18kV		(USR180A) SF	(688-18R) BE			
20kV	HVJX 20K PA	(688-20R) BE	HVF 20000 [†] PB			HVFS 20000 PC
22.5kV	HVJX 22.5K PA					
25kV	HVJX 25K PA	(688-25R) BE	HVF 25000 [†] PB			
30kV	HVJX 30K PA					
35kV	HVJX 35K PA					
37.5kV	HVJX 37.5K PA					
40kV	HVJX 40K PA					
45kV	HVJX 45K PA					
50kV						
60kV						
Reverse Recovery Time (Max.)	250ns	500ns	500ns 150ns [†]	250ns	250ns	150ns

Parentheses () designates product using fused-in-glass single chip rectifiers; all others use stacked chips.

CUSTOMER SPECIFICATION SHEET FOR SPECIAL RECTIFIER ASSEMBLIES

Date _____
Company Name _____ Phone _____
Address _____ City _____ State _____
Engineer _____ Ext. _____ Buyer _____ Ext. _____
_____ New Application, _____ Existing Application, Presently Using _____
Quantities to Quote _____

ELECTRICAL REQUIREMENTS

Rectifier Application:

1. Circuit: _____ Half Wave _____ Center Tap _____ Doubler _____ Bridge
2. AC Input: _____ Volts _____ CPS _____ Phase _____ Wave Shape
3. DC Output: _____ Volts _____ Amps At _____ °C
4. Max. Transient Voltage: _____ Volts
5. Max. Fault Current: _____ Amps For _____ Sec.
6. Type of Load _____

Modulator Application:

1. Use _____
2. Peak Voltage _____ V
3. Wave Shape _____
4. Rise or Switching Time _____ Sec.
5. Peak Pulse Current _____ Amps At _____ °C
6. Pulse Duration _____ Sec.
7. Average Current _____ Amps
8. PRF _____ PPS

ENVIRONMENTAL REQUIREMENTS

Operating Medium _____
Operating Temperature Range _____
Storage Temperature Range _____
Other Requirements _____

MECHANICAL REQUIREMENTS

Maximum Size _____
Maximum Weight _____
Terminal Provisions _____
Mounting Provisions _____

7

RECTIFIER ASSEMBLIES

High Voltage Stacks, 1 Amp to 5 Amp,
Military Approved

JAN 1N5597
JAN 1N5600
JAN 1N5603

FEATURES

- Qualified to MIL-S-19500/404A
- PIV: to 10kV
- Surge Ratings: to 200A
- Current Ratings: to 5A
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Modular Package For Easy Stacking

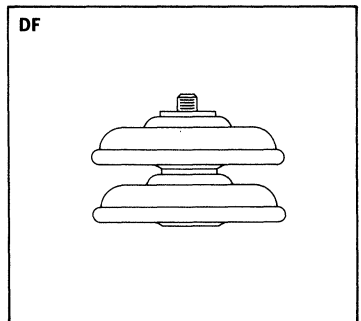
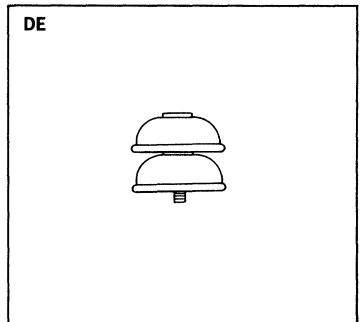
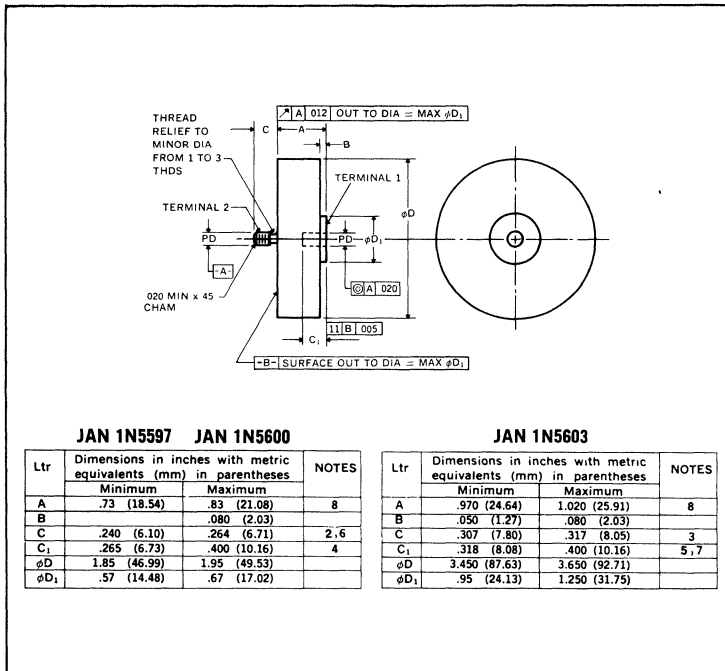
DESCRIPTION

This series of military high-voltage high-current stacks offers the utmost in reliability as required in military system designs. The rectifiers are assembled with diodes which have been subjected to TX type screening tests.

ABSOLUTE MAXIMUM RATINGS

	JAN 1N5597	JAN 1N5600	JAN 1N5603
Peak Inverse Voltage	10kV	5kV	5kV
Maximum Average D.C. Output Current @ $T_C = 75^\circ\text{C}$	1A	2A	5A
Non-Repetitive Sinusoidal Surge (8.3ms) @ $T_C = 75^\circ\text{C}$	30A	80A	200A
Operating and Storage Temperature Range	-65°C to +150°C		

MECHANICAL SPECIFICATIONS



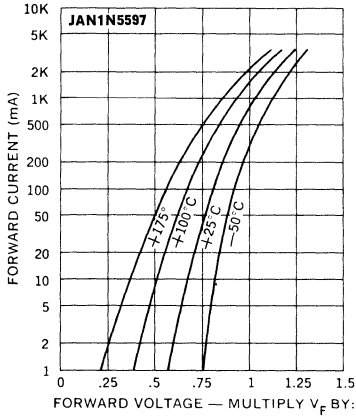
1. All marking shall be on cathode side of module.
2. Threaded stud 1/4-28UNF-2A.
3. Threaded stud 3/8-24UNF-2A.
4. Threaded insert 1/4-28UNF-2B.

5. Threaded insert 3/8-24UNF-2B.
6. Cathode connected to terminal 2.
7. Cathode connected to terminal 1.
8. Module contour within dimension A is not specified.

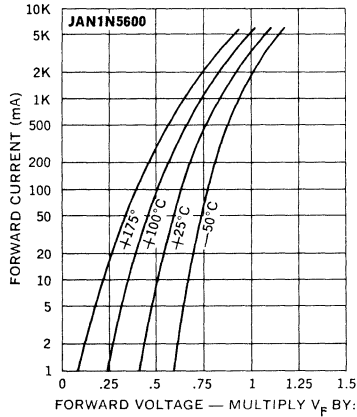
Electrical Specifications (at 25°C unless noted)

Type	PIV kV	Forward Voltage Drop		Maximum Leakage Current @ PIV		Capacitance @ $V_R = 100V$		Maximum Reverse Transient Energy Absorption joules
		Min.	Max.	$T_A = 25^\circ C$	$T_A = 100^\circ C$	Min.	Max.	
				μA	μA			
JAN 1N5597	10	13V @ 1A	19V @ 1A	1	75	5	30	2
JAN 1N5600	5	6V @ 2A	10V @ 2A	5	100	7	30	6
JAN 1N5603	5	6V @ 5A	10V @ 5A	5	100	15	40	12

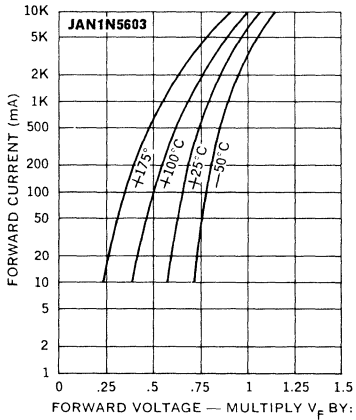
Typical Forward Voltage vs. Forward Current



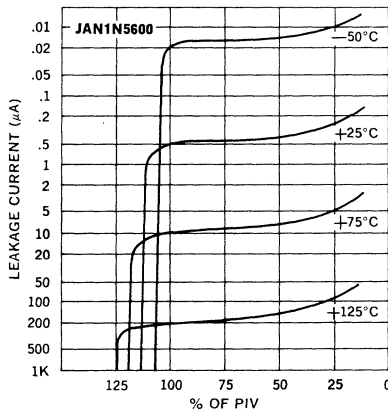
Typical Forward Voltage vs. Forward Current



Typical Forward Voltage vs. Forward Current

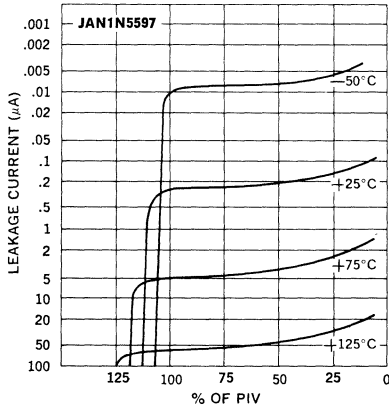


Typical Leakage Current vs. PIV

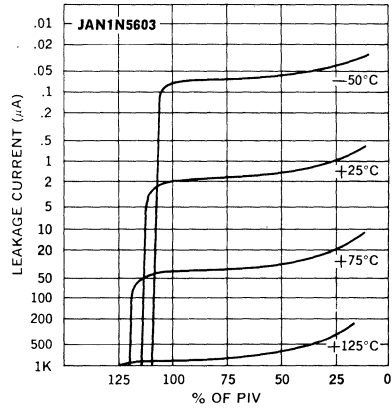


7

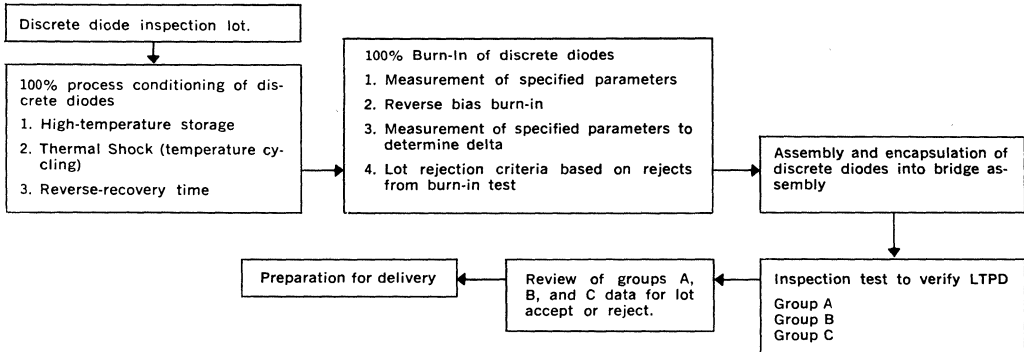
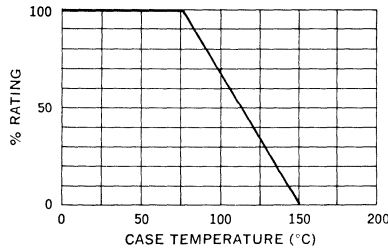
Typical Leakage Current vs. PIV



Typical Leakage Current vs. PIV



Current Derating Curve



RECTIFIER ASSEMBLIES

688 SERIES

High Voltage Stacks,
Standard and Fast Recovery

FEATURES

- PIV: from 10kV to 25kV
- Surge Rating: to 20A
- Recovery Time Available: to 500ns
- Current Ratings: to 0.6A
- Bonded Plate for Maximum Heat Transfer
- Controlled Avalanche Characteristics
- Only Fused-in-Glass Diodes Used

DESCRIPTION

This series of high power stacks has a unique packaging design that provides characteristics not obtainable in conventional molded epoxy packages. This series, therefore, is ideally suited for high-voltage, high-power applications.

7

ABSOLUTE MAXIMUM RATINGS

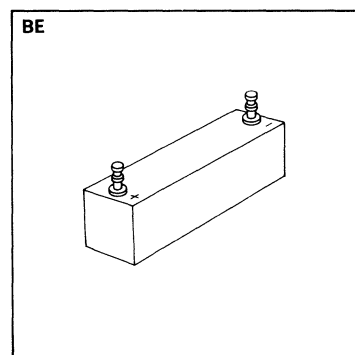
Peak Inverse Voltage 10kV to 25kV
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-repetitive Sinusoidal Surge (8.3ms) 20A
 Operating and Storage Temperature Range -65°C to +150°C
 Thermal Resistance Junction to Ambient 25°C/W
 Junction to Case 10°C/W

688 SERIES

	ins.	mm.
A	1.140 MAX.	28.96 MAX.
B	2.985-3.015	75.82-76.58
C	2.110-2.140	53.59-54.36
D	.740- .770	18.80-19.56
E	.720-.750	18.29-19.05

dd suffix R to denote Fast Recovery version. For example, for recovery time, $t_{rr} = 500\text{ns}$; order 688-10R.

Typical Weight — 2.5 ounces
70 grams



MARKING

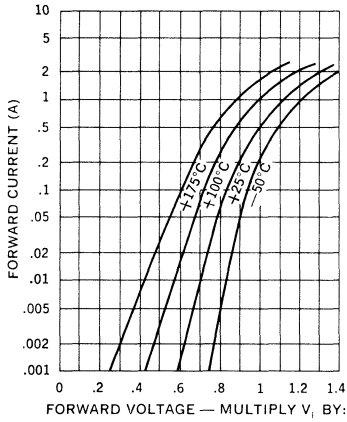
Cathode — Positive Output	+
Anode — Negative	-

Part number is printed on the body.

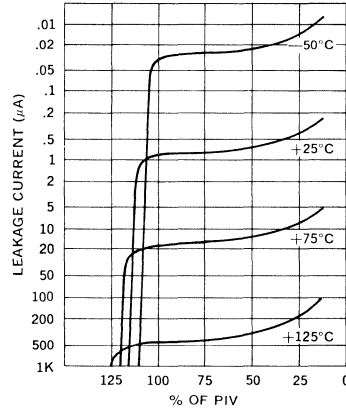
Electrical Specifications (at 25°C unless noted)					Maximum Ratings	
Type	PIV kV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV		Maximum Average D.C. Output Current	
			T _A = 25°C μA	T _A = 100°C μA	T _C = 100°C Amps	
Standard	688-10	10V @ 0.4A	2	100	0.60	
And Fast	688-12	20V @ 0.4A			0.50	
Recovery*	688-15	25V @ 0.4A			0.40	
	688-18	30V @ 0.4A			0.35	
	688-20	34V @ 0.4A			0.30	
	688-25	42V @ 0.4A			0.20	

*Add suffix R to denote Fast Recovery version.

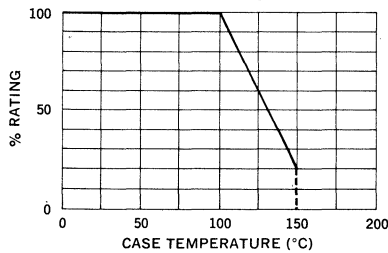
Typical Forward Voltage Per Leg vs. Forward Current



Typical Leakage Current vs. PIV



Current Derating Curve



HIGH VOLTAGE SILICON RECTIFIERS

100-250mA

Fast Recovery, Miniature

HA10-100
HVX10-100

FEATURES

- PIV: From 1.0kV to 10kV
- 250nS Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

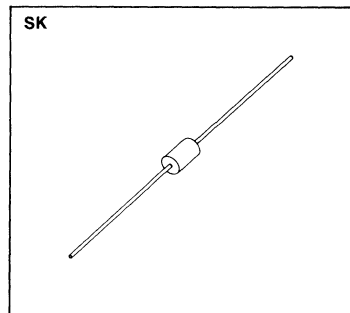
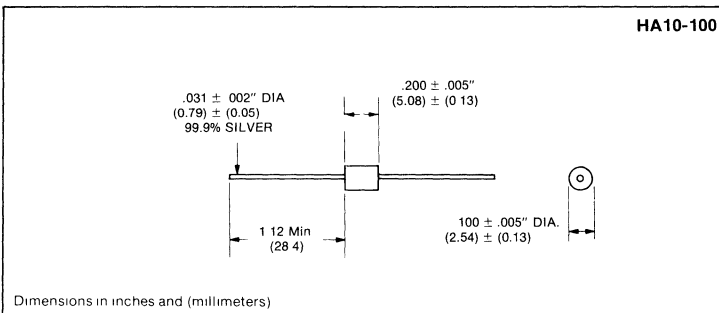
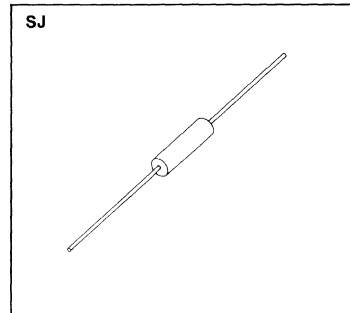
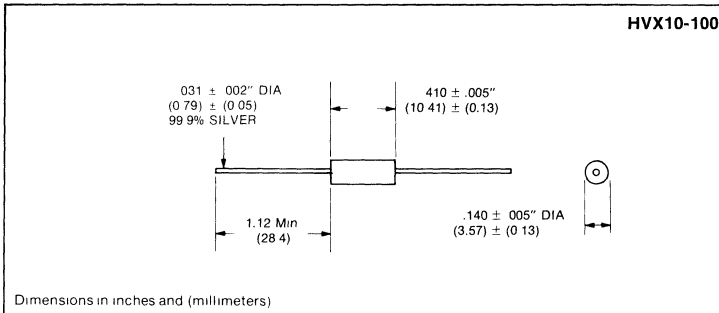
The HVX/HA silicon rectifier series combine a medium rectified current capability and high reliability in a miniature package for commercial, industrial and military applications. The use of cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life. The fast reverse recovery characteristics enhance applications in high frequency power conversion and control circuits.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	1.0kV to 10kV
Maximum Average Rectified Current	See Electrical Specifications
Maximum One Cycle Surge 8.3mS	See Electrical Specifications
Maximum Recurrent Peak Current Surge	See Electrical Specifications
Operating and Storage Temperature Range	-65°C to +150°C

MECHANICAL SPECIFICATIONS

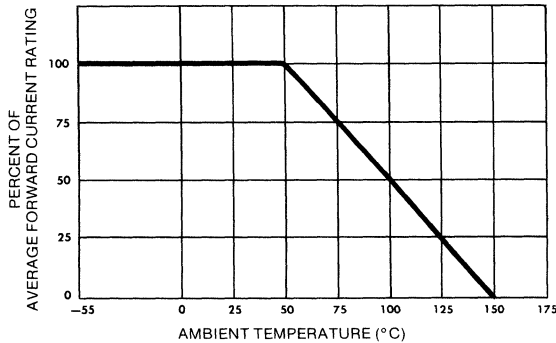


Type	Type	ELECTRICAL SPECIFICATIONS (at 25° C unless noted)					MAXIMUM RATINGS				
		Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ 100mA	Maximum Reverse Recovery Time	Maximum Average Rectified Current†			Maximum Recurrent Peak Current	Maximum One Cycle Surge 8.3mS Surge
		PIV	I_R		V_F	T_{RR}	I_O			I_F	$I_F(\text{surge})$
		V	25° C μA	100° C μA	V	nS	50° C mA	100° C mA	125° C mA	A	A
HVX10	HA10	1000	1	20	5	250	250	125	62.5	2.5	14
HVX15	HA15	1500	1	20	5	250	250	125	62.5	2.5	14
HVX20	HA20	2000	1	20	5	250	250	125	62.5	2.5	14
HVX25	HA25	2500	1	20	5	250	250	125	62.5	2.5	14
HVX30	HA30	3000	1	20	5	250	250	125	62.5	2.5	14
HVX40	HA40	4000	1	20	12	250	100	50	25	1.0	4
HVX50	HA50	5000	1	20	12	250	100	50	25	1.0	4
HVX75	HA75	7500	1	20	12	250	100	50	25	1.0	4
HVX100	HA100	10000	1	20	12	250	100	50	25	1.0	4

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 † The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

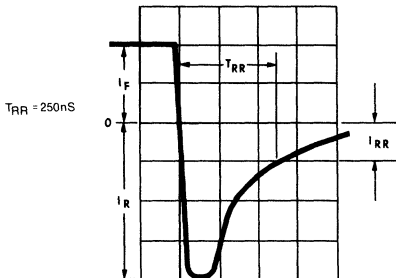
NOTE: Maximum lead temperature for soldering is 250° C, 3/8" (9.5mm) from case for 5 seconds maximum.

MAXIMUM FORWARD CURRENT VS. AMBIENT TEMPERATURE

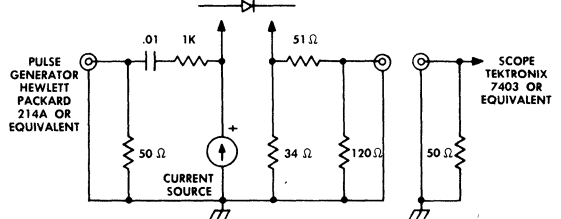


REVERSE RECOVERY TEST CONDITIONS: $I_F = 50 \text{ mA}$, $I_R = 100 \text{ mA}$, $I_{RR} = 25 \text{ mA}$

REVERSE RECOVERY WAVE FORM



REVERSE RECOVERY TEST CIRCUIT



HIGH VOLTAGE SILICON RECTIFIERS

100-250mA

Standard Recovery, Miniature

HS10-100
HVE10-30 (1N3643-47)
HVE40-100 (1N5181-84)

FEATURES

- PIV: From 1.0kV to 10kV
- JEDEC Types
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

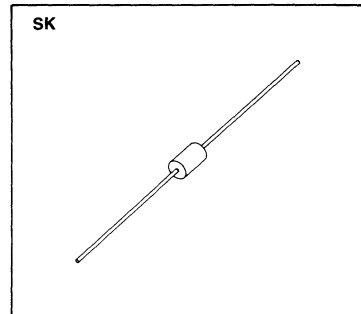
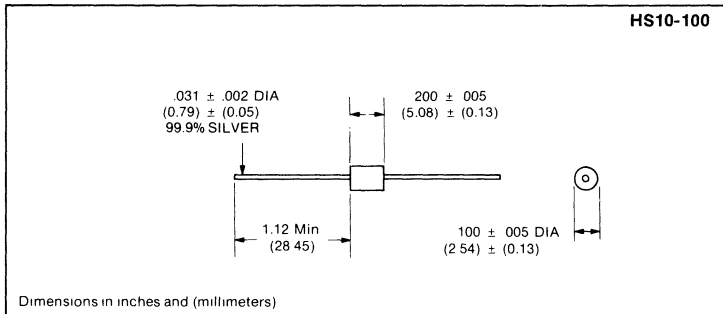
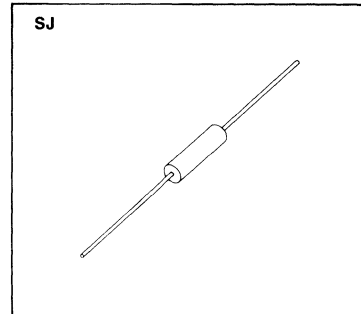
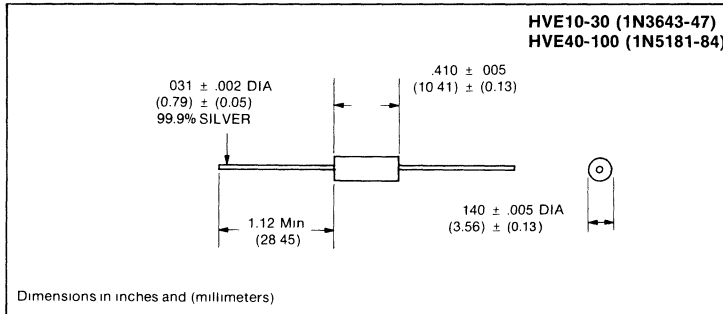
The HVE/HS silicon rectifier series combine a medium average rectified current capability and high reliability in a miniature package for commercial, industrial and military applications. The use of cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life. A 2 microsecond reverse recovery characteristic improves the circuit efficiency of power conversion and control systems.

7

ABSOLUTE MAXIMUM RATINGS

	HS	HVE
Peak Inverse Voltage	1.0kV	10kV
Maximum Average Rectified Current	See Electrical Specifications	
Maximum One Cycle Surge 8.3mS	See Electrical Specifications	
Maximum Recurrent Peak Current Surge	See Electrical Specifications	
Operating and Storage Temperature Range	-65°C to +175°C	

MECHANICAL SPECIFICATIONS

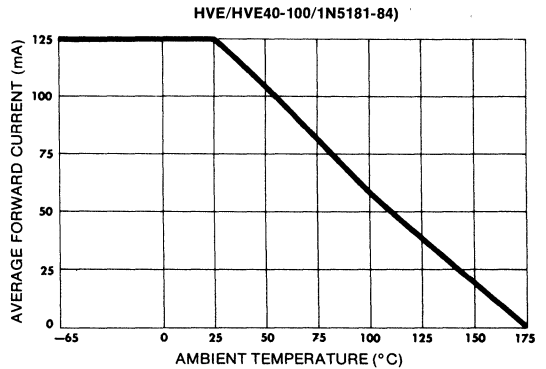
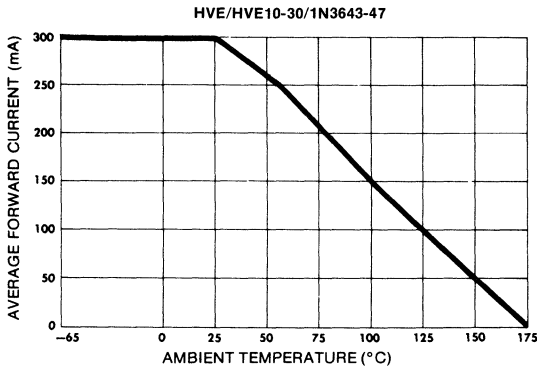


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS					
Maximum Reverse Recovery Time		Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ 100mA Max.	Maximum Average Rectified Current†			Maximum Recurrent Peak Current Surge	Maximum One Cycle Surge 8.3mS
			I _R			I _O				
2μS	2μS	PIV	25°C	100°C	25°C	50°C	100°C	150°C	I _F	I _F (surge)
Type	Type		V	μA	μA	V	mA	mA		
HS10	HVE10 (1N3643)	1000	1	20	3.5	250	150	50	2.5	14
HS15	HVE15 (1N3644)	1500	1	20	3.5	250	150	50	2.5	14
HS20	HVE20 (1N3645)	2000	1	20	3.5	250	150	50	2.5	14
HS25	HVE25 (1N3646)	2500	1	20	3.5	250	150	50	2.5	14
HS30	HVE30 (1N3647)	3000	1	20	3.5	250	150	50	2.5	14
HS40	HVE40 (1N5181)	4000	1	20	10.0	100	60	20	1.0	4
HS50	HVE50 (1N5182)	5000	1	20	10.0	100	60	20	1.0	4
HS75	HVE75 (1N5183)	7500	1	20	10.0	100	60	20	1.0	4
HS100	HVE100 (1N5184)	10000	1	20	10.0	100	60	20	1.0	4

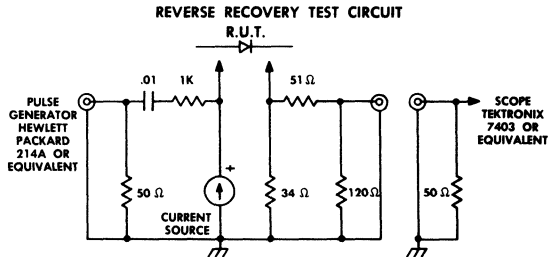
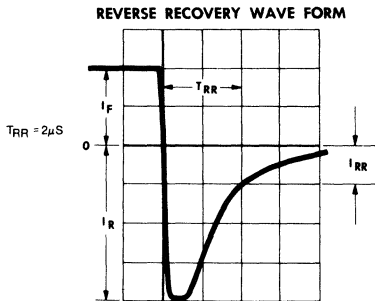
*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.

†The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds maximum.



REVERSE RECOVERY TEST CONDITIONS: I_F = 50 mA, I_R = 100 mA, I_{RR} = 25 mA



HIGH VOLTAGE SILICON RECTIFIERS MULTISTAC

Fast Recovery, High Current

HVF2500-25000

FEATURES

- PIV: From 2.5kV to 25kV
- 150nS Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

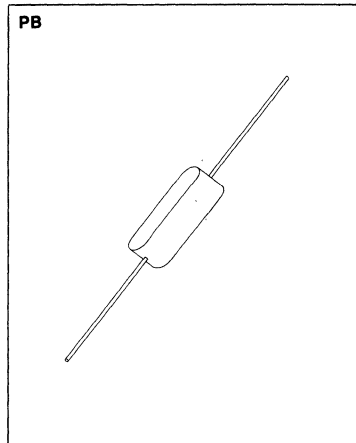
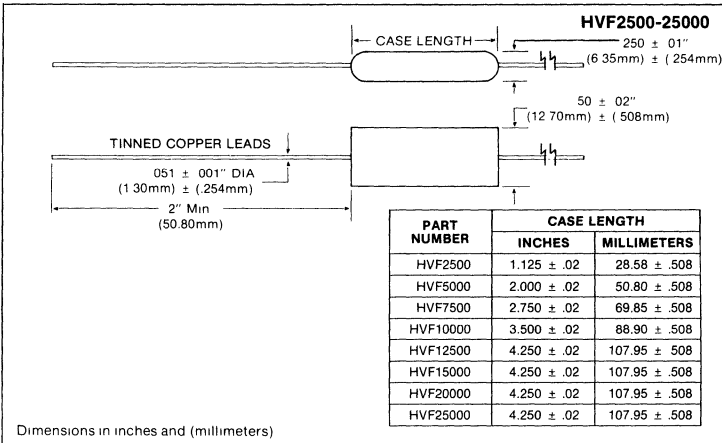
The HVF MULTISTAC high current, high voltage silicon rectifier's convenient size and high power capability meets the reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 2.5kV to 25kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

MECHANICAL SPECIFICATIONS



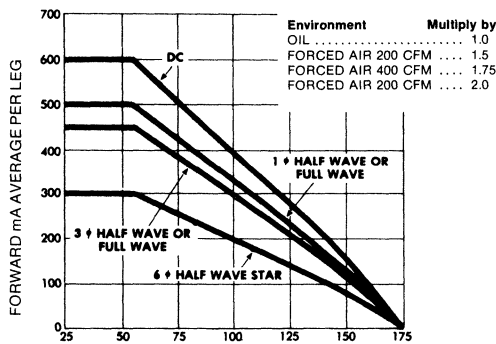
Type	ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O Max.	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
	V	25°C μA	100°C μA	V	nS	55°C A	100°C A	25°C A	100°C A		
HVF2500	2500	0.1	15	5.5	150	.5	.33	40	20	1.125	28.58
HVF5000	5000	0.1	15	11.0	150	.5	.33	40	20	2.000	50.80
HVF7500	7500	0.1	15	16.5	150	.5	.33	40	20	2.750	69.85
HVF10000	10000	0.1	15	22.0	150	.5	.33	40	20	3.500	88.90
HVF12500	12500	0.1	15	27.5	150	.5	.33	40	20	4.250	107.95
HVF15000	15000	0.1	15	33.0	150	.5	.33	40	20	4.250	107.95
HVF20000	20000	0.1	15	38.5	150	.5	.33	40	20	4.250	107.95
HVF25000	25000	0.1	15	44.0	150	.5	.33	40	20	4.250	107.95

* Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.

† The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

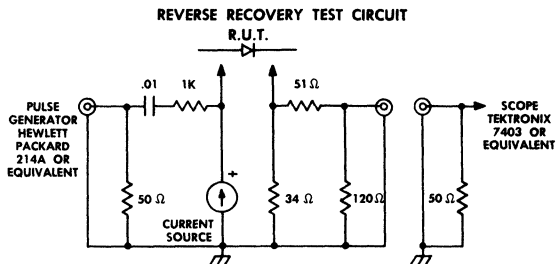
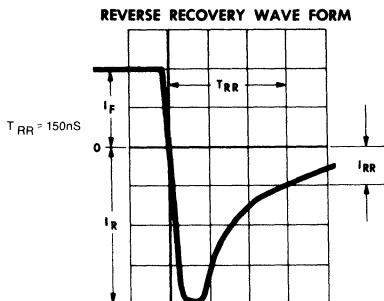
NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.

MAXIMUM FORWARD CURRENT VS. AMBIENT TEMPERATURE



FORWARD CURRENT PER LEG VS. AMBIENT TEMPERATURE (°C)

REVERSE RECOVERY TEST CONDITIONS: I_F = 0.1A, I_R = 0.2A, I_{RR} = 0.05A



Reverse recovery is measured on each rectifier stack prior to manufacture of the assembly

HIGH VOLTAGE SILICON RECTIFIERS

MULTISTAC

Fast Recovery, High Current

HVFS2500-20000

FEATURES

- PIV: From 2.5kV to 20kV
- 150nS Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

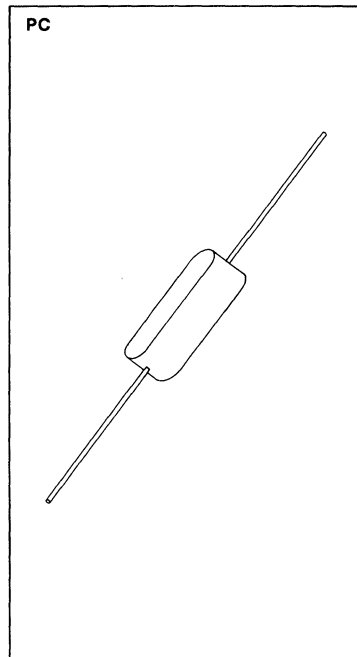
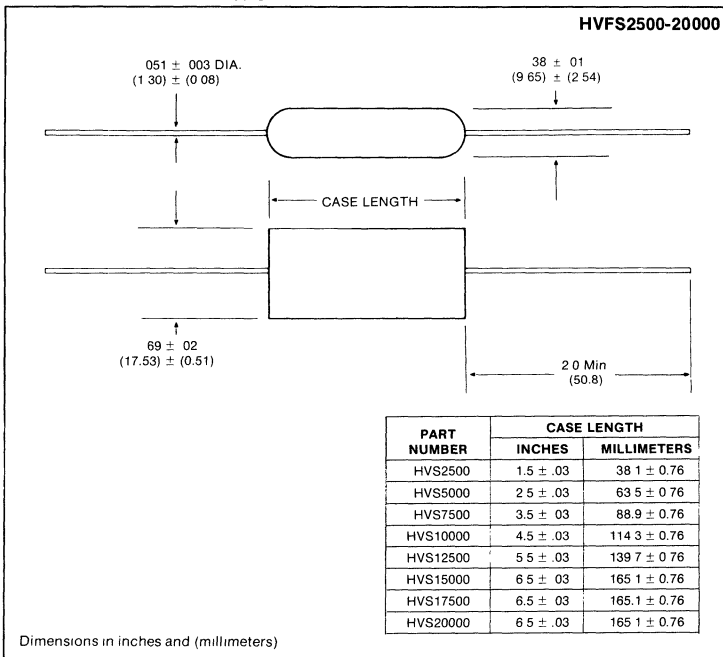
The HVFS MULTISTAC high current, high voltage silicon rectifier's convenient size and high power capability meets the reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 2.5kV to 20kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

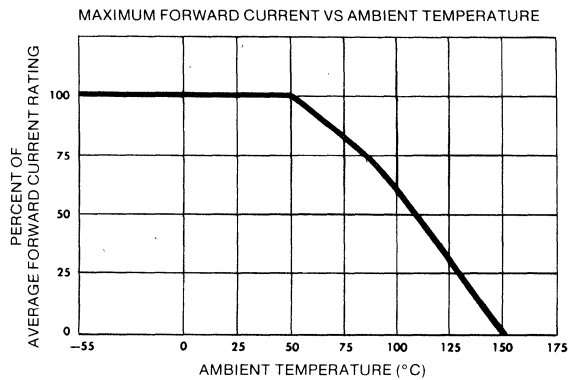
MECHANICAL SPECIFICATIONS



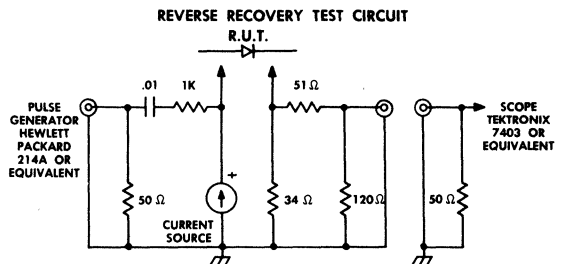
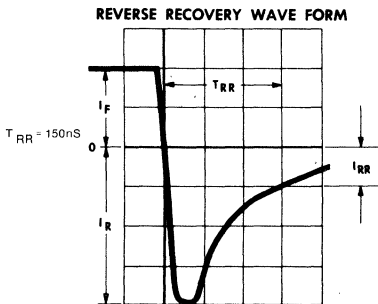
Type	ELECTRICAL SPECIFICATIONS (at 25° C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
		V	25° C			100° C	55° C	100° C	25° C		
	μA	μA	V	nS	A	A	A	A	Ins.	MM	
HVFS2500	2500	10	120	8	150	2.2	1.3	200	100	1.5	38.1
HVFS5000	5000	10	120	16	150	2.2	1.3	200	100	2.5	63.5
HVFS7500	7500	10	120	21	150	2.2	1.3	200	100	3.5	88.9
HVFS10000	10000	10	120	29	150	2.2	1.3	200	100	4.5	114.9
HVFS12500	12500	10	120	36	150	2.2	1.3	200	100	5.5	139.7
HVFS15000	15000	10	120	44	150	2.2	1.3	200	100	6.5	165.1
HVFS17500	17500	10	120	51	150	2.2	1.3	200	100	6.5	165.1
HVFS20000	20000	10	120	58	150	2.2	1.3	200	100	6.5	165.1

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 † The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250° C 3/8" (9.5mm) from case for 5 seconds.



REVERSE RECOVERY TEST CONDITIONS: I_F = 12.5A, I_R = 25A, I_{RR} = 6.25A



HIGH VOLTAGE SILICON RECTIFIERS

MULTISTAC

Standard Recovery

HVH5000-25000

FEATURES

- PIV: From 5kV to 25kV
- 2 μ S Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

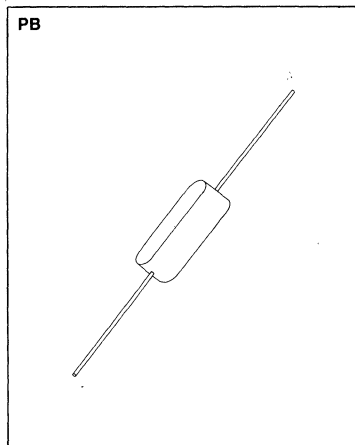
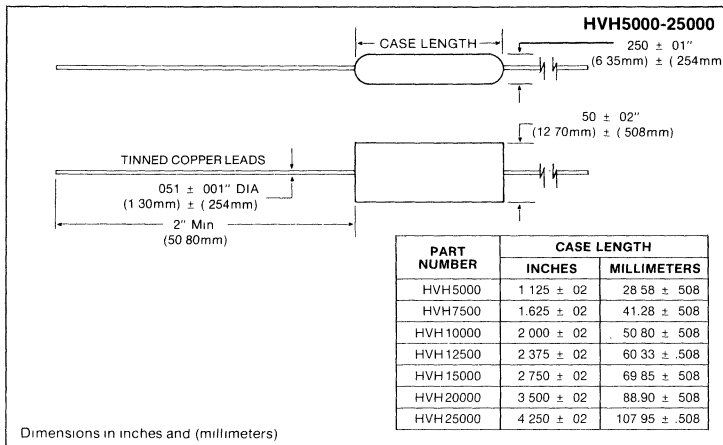
The HVH MULTISTAC silicon rectifier assemblies meet the stringent reliability requirements of commercial, industrial and military users through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life. The 2 microsecond reverse recovery time improves the circuit efficiency of power conversion and control systems.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 5kV to 25kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

MECHANICAL SPECIFICATIONS



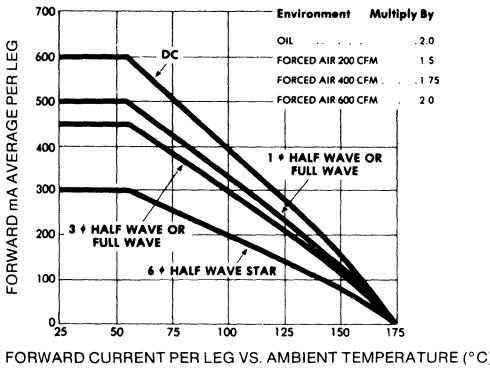
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS				Case Length	
Maximum Reverse Recovery Time	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Average Rectified Current†		Maximum One Cycle Surge			
2μS	PIV	I _R		V _F	I _O		I _F (surge)			
Type	V	25°C	100°C	25°C	55°C	100°C	25°C	100°C		
		μA	μA	V	A	A	A	A	Ins.	MM
HVH 5000	5000	0.1	15	7	.5	.33	60	30	1.125	28.58
HVH 7500	7500	0.1	15	10	.5	.33	60	30	1.625	41.28
HVH10000	10000	0.1	15	14	.5	.33	60	30	2.000	50.80
HVH12500	12500	0.1	15	17	.5	.33	60	30	2.375	60.33
HVH15000	15000	0.1	15	20	.5	.33	60	30	2.750	69.85
HVH20000	20000	0.1	15	27	.5	.33	60	30	3.500	88.90
HVH25000	25000	0.1	15	33	.5	.33	60	30	4.250	107.95

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.

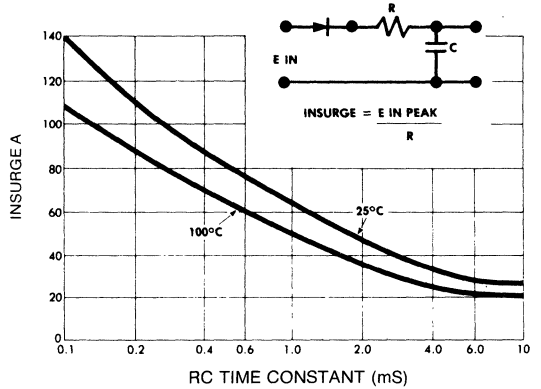
†The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.

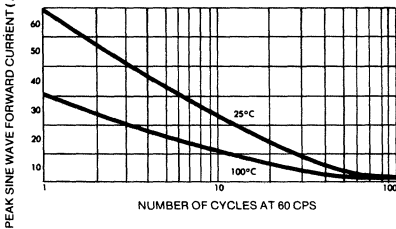
MAXIMUM FORWARD CURRENT VS. AMBIENT TEMPERATURE



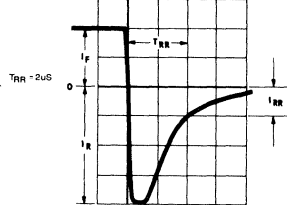
MAXIMUM RATINGS FOR CAPACITY LOADS



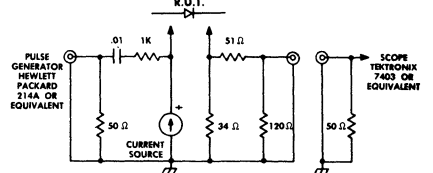
NON-RECURRENT FORWARD CURRENT SURGE CURVE



REVERSE RECOVERY WAVE FORM



REVERSE RECOVERY TEST CIRCUIT



Reverse recovery is measured on each rectifier stack prior to manufacture of the assembly.

HIGH VOLTAGE SILICON RECTIFIERS

MULTISTAC

Standard Recovery, High Current

HVHF5000-25000

FEATURES

- PIV: From 5kV to 25kV
- 1μS Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

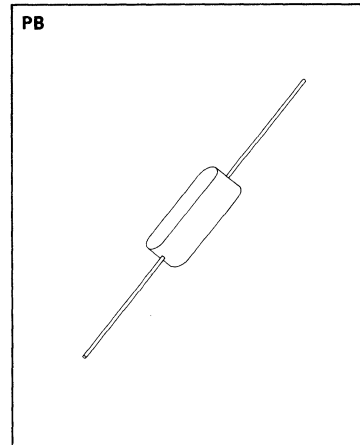
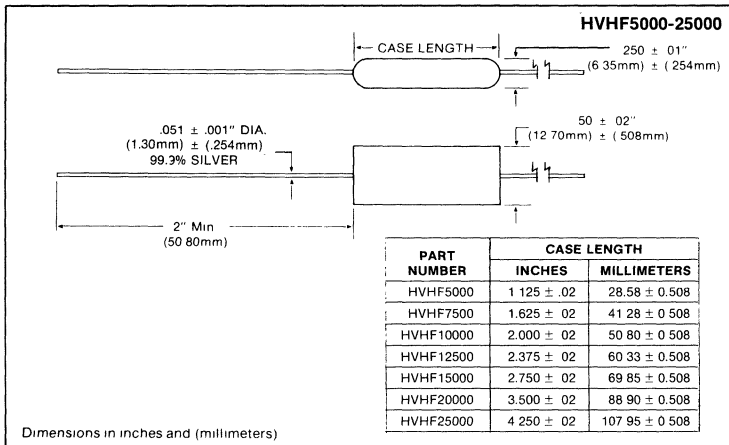
The HVHF MULTISTAC high current, high voltage silicon rectifier's convenient size and high power capability meets the reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 5kV to 25kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

MECHANICAL SPECIFICATIONS

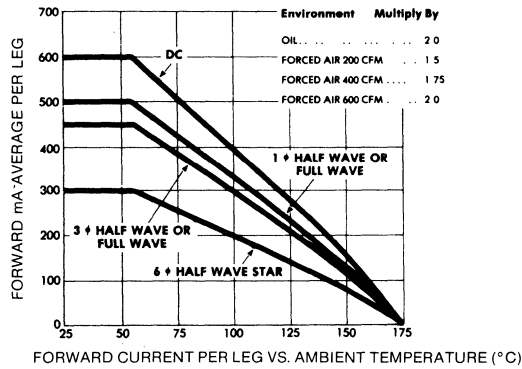


Type	ELECTRICAL SPECIFICATIONS (at 25° C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
	V	25° C	100° C	V	μS	55° C	100° C	25° C	100° C		
		μA	μA			A	A	A	A	Ins.	MM
HVHF5000	5000	0.1	15	7	1	.5	.33	60	30	1.125	28.58
HVHF7500	7500	0.1	15	10	1	.5	.33	60	30	1.625	41.28
HVHF10000	10000	0.1	15	14	1	.5	.33	60	40	2.000	50.80
HVHF12500	12500	0.1	15	17	1	.5	.33	60	40	2.375	60.33
HVHF15000	15000	0.1	15	20	1	.5	.33	60	40	2.750	69.85
HVHF20000	20000	0.1	15	27	1	.5	.33	60	40	3.500	88.90
HVHF25000	25000	0.1	15	33	1	.5	.33	60	40	4.250	107.95

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 †The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

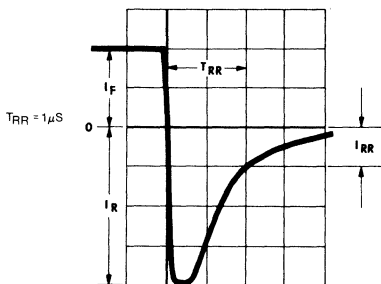
NOTE: Maximum lead temperature for soldering is 250° C 3/8" (9.5mm) from case for 5 seconds.

MAXIMUM FORWARD CURRENT VS. AMBIENT TEMPERATURE

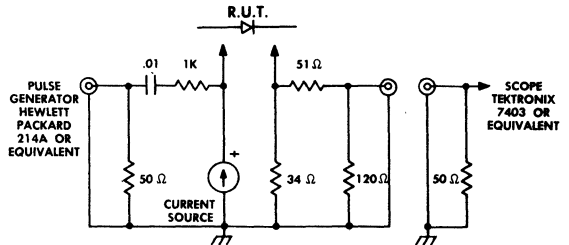


REVERSE RECOVERY TEST CONDITIONS: I_F = 100mA, I_R = 200mA, I_{RR} = 50mA

REVERSE RECOVERY WAVE FORM



REVERSE RECOVERY TEST CIRCUIT



Reverse recovery is measured on each rectifier stack prior to manufacture of the assembly.

HIGH VOLTAGE SILICON RECTIFIERS

HVHJ15K-45K

MULTISTAC

Medium Recovery, Medium Current

FEATURES

- PIV: From 15kV to 45kV
- 2 μ S Reverse Recovery
- High Surge
- Low Reverse Leakage
- Corona Free

DESCRIPTION

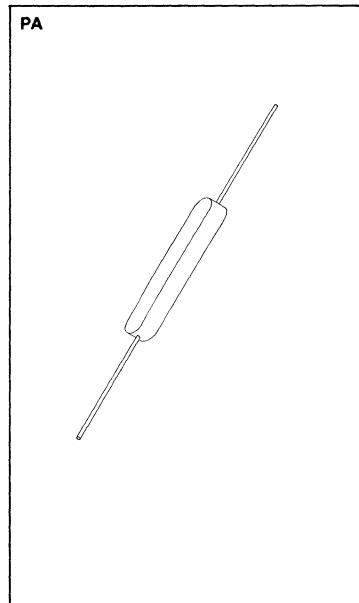
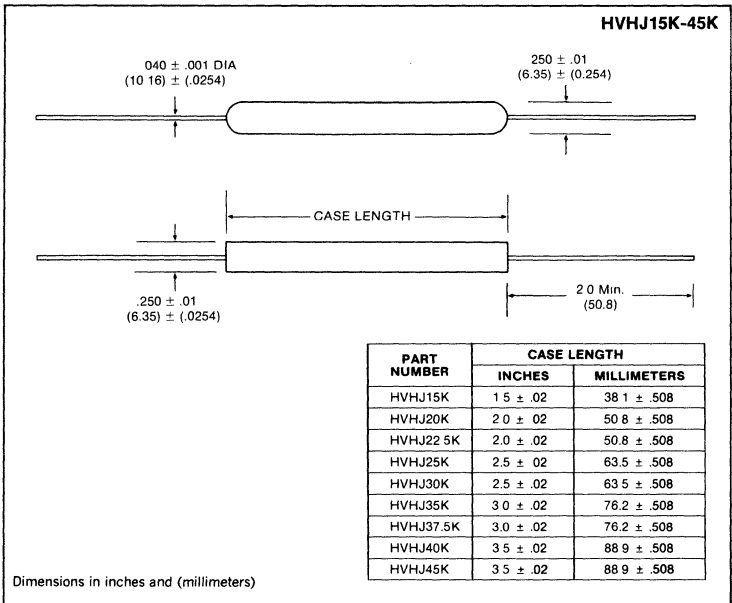
The HVHJ MULTISTAC medium current, high voltage silicon rectifier assembly's small size and high power capability meets the stringent reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 15kV to 45kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

MECHANICAL SPECIFICATIONS

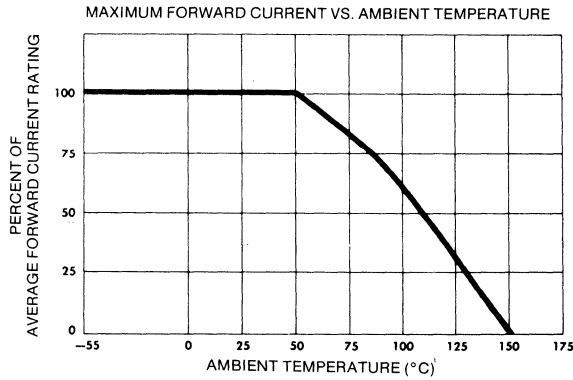


Type	ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
	V	25°C	100°C	V	μS	55°C	100°C	25°C	100°C		
		μA	μA			mA	mA	A	A	Ins.	MM
HVHJ15K	15000	0.1	25	20	2	50	30	5	2.5	1.5	38.1
HVHJ20K	20000	0.1	25	30	2	50	30	5	2.5	2.0	50.8
HVHJ22.5K	22500	0.1	25	30	2	50	30	5	2.5	2.0	50.8
HVHJ25K	25000	0.1	25	40	2	50	30	5	2.5	2.5	63.5
HVHJ30K	30000	0.1	25	40	2	50	30	5	2.5	2.5	63.5
HVHJ35K	35000	0.1	25	50	2	50	30	5	2.5	3.0	76.2
HVHJ37.5K	37500	0.1	25	50	2	50	30	5	2.5	3.0	76.2
HVHJ40K	40000	0.1	25	60	2	50	30	5	2.5	3.5	88.9
HVHJ45K	45000	0.1	25	60	2	50	30	5	2.5	3.5	88.9

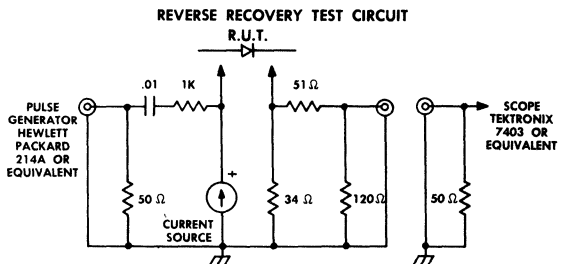
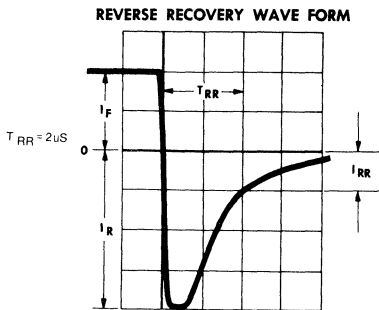
*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.

† The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.



REVERSE RECOVERY TEST CONDITIONS: I_F = 50mA, I_R = 100mA, I_{RR} = 25mA



HIGH VOLTAGE SILICON RECTIFIERS

MULTISTAC

Medium Recovery, High Current

HVHS2500-20000

FEATURES

- PIV: From 2.5kV to 20kV
- 2 μ S Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

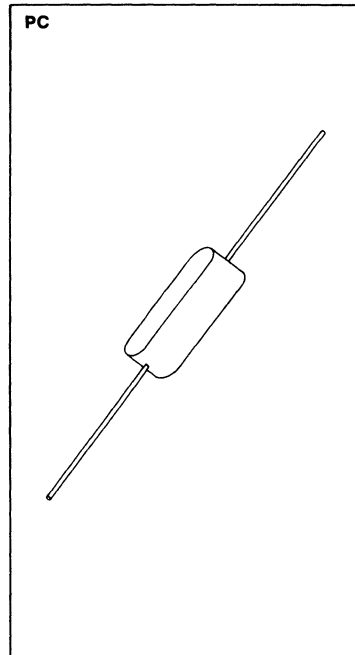
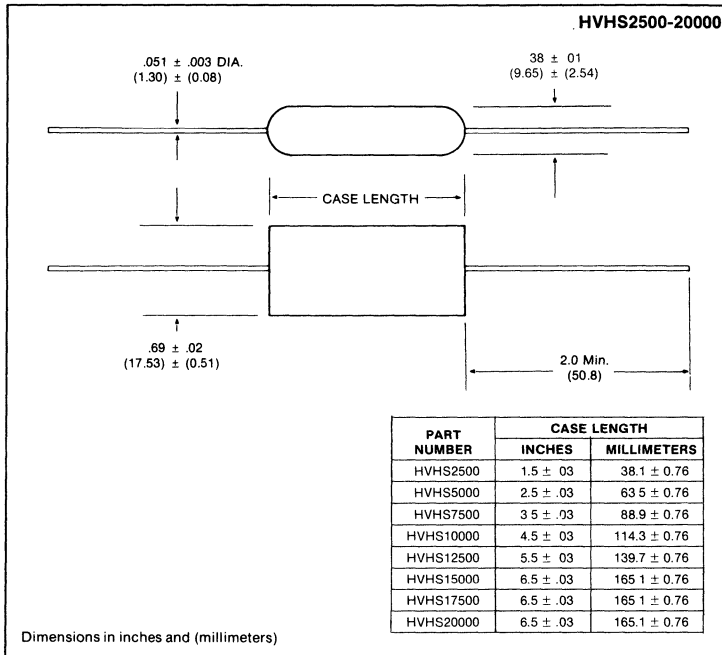
The HVHS MULTISTAC high current, high voltage silicon rectifier's convenient size and high power capability meets the reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 2.5kV to 20kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3 mS See Electrical Specifications
 Operating and Storage Temperature Range -55°C to +150°C

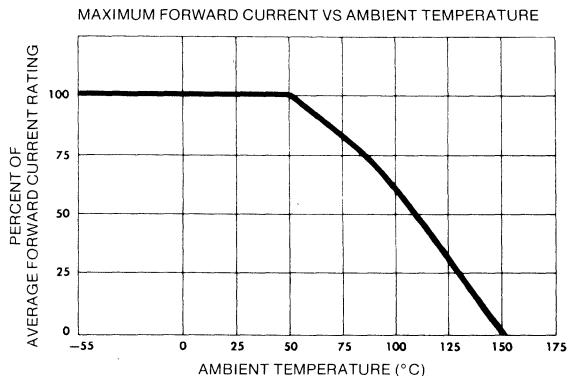
MECHANICAL SPECIFICATIONS



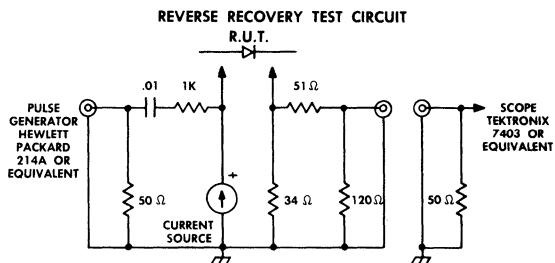
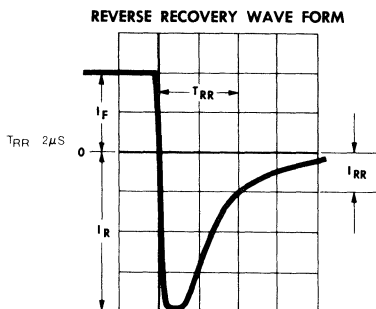
Type	ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
	V	25°C μA	100°C μA	V	μS	55°C A	100°C A	25°C A	100°C A		
HVHS2500	2500	10	120	5	2	2.2	1.3	200	100	1.5	38.1
HVHS5000	5000	10	120	10	2	2.2	1.3	200	100	2.5	63.5
HVHS7500	7500	10	120	15	2	2.2	1.3	200	100	3.5	88.9
HVHS10000	10000	10	120	20	2	2.2	1.3	200	100	4.5	114.9
HVHS12500	12500	10	120	25	2	2.2	1.3	200	100	5.5	139.7
HVHS15000	15000	10	120	30	2	2.2	1.3	200	100	6.5	165.1
HVHS17500	17500	10	120	35	2	2.2	1.3	200	100	6.5	165.1
HVHS20000	20000	10	120	40	2	2.2	1.3	200	100	6.5	165.1

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 † The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.



REVERSE RECOVERY TEST CONDITIONS: I_F = 0.4A, I_R = 0.8A, I_{RR} = 0.2A



Reverse recovery is measured on each rectifier stack prior to manufacture of the assembly

HIGH VOLTAGE SILICON RECTIFIERS

HVJX15K-45K

MULTISTAC

Fast Recovery, Medium Current

FEATURES

- PIV: From 15kV to 45kV
- 200nS Reverse Recovery
- High Surge Current Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

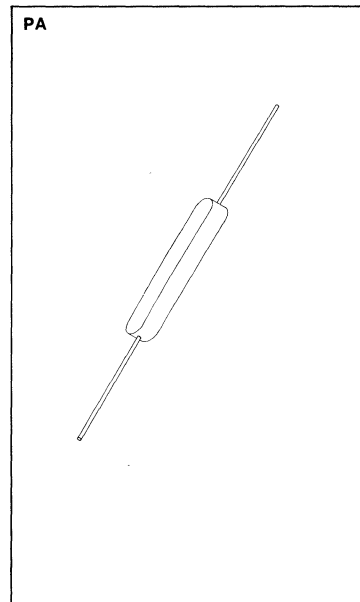
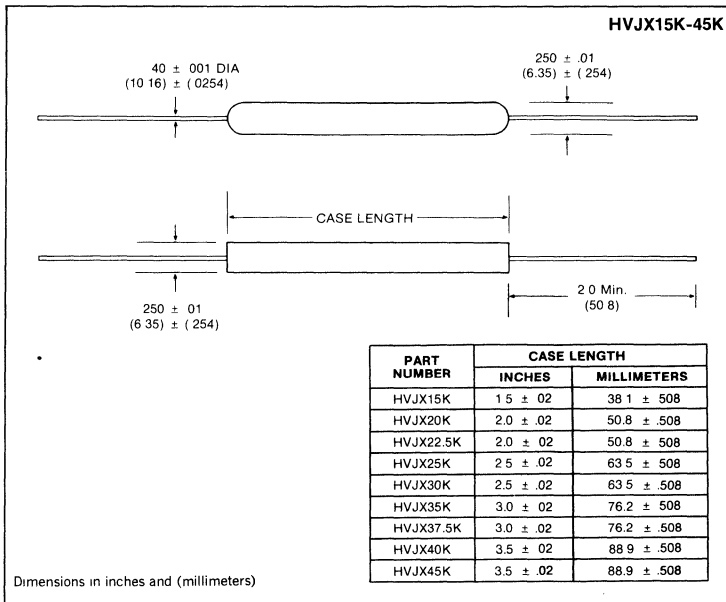
The HVJX MULTISTAC medium current high voltage silicon rectifier assembly's small size and high power capability meets the stringent reliability requirements of commercial, industrial and military applications. Reliability with economy are obtained through the use of proprietary innovations in manufacturing technique. Cylindrical die construction and metallurgical bonds minimize electrical and mechanical stress, contributing to long life.



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 15kV to 45kV
 Maximum Average Rectified Current See Electrical Specifications
 Maximum One Cycle Surge 8.3 mS See Electrical Specifications
 Operating and Storage Temperature Range -55° C to +150° C

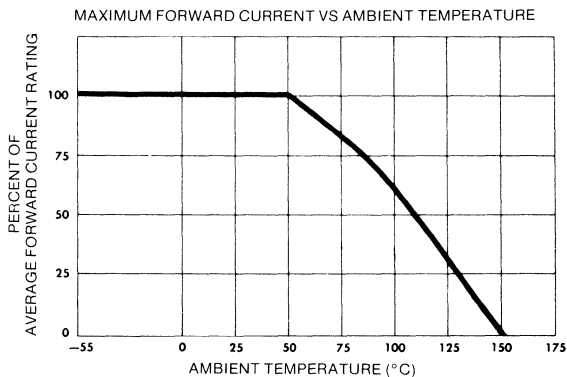
MECHANICAL SPECIFICATIONS



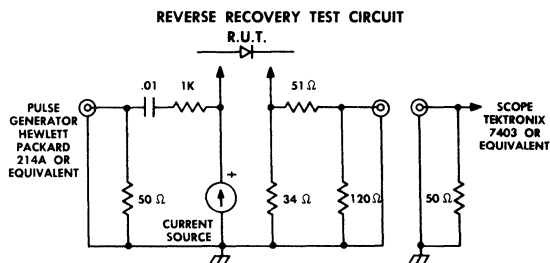
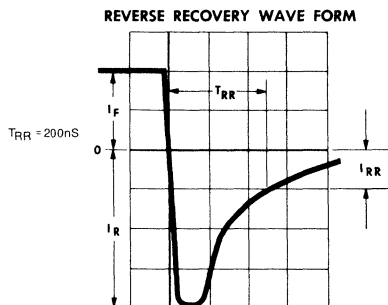
Type	ELECTRICAL SPECIFICATIONS (at 25°C unless noted)					MAXIMUM RATINGS				Case Length	
	Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Reverse Recovery Time	Maximum Average Rectified Current†		Maximum One Cycle Surge 8.3mS			
	PIV	I _R		V _F	T _{RR}	I _O		I _F (surge)			
	V	25°C μA	100°C μA	V	nS	55°C mA	100°C mA	25°C A	100°C A		
HVJX15K	15000	0.1	25	24	200	50	30	5	2.5	1.5	38.1
HVJX20K	20000	0.1	25	36	200	50	30	5	2.5	2.0	50.8
HVJX22.5K	22500	0.1	25	36	200	50	30	5	2.5	2.0	50.8
HVJX25K	25000	0.1	25	48	200	50	30	5	2.5	2.5	63.5
HVJX30K	30000	0.1	25	48	200	50	30	5	2.5	2.5	63.5
HVJX35K	35000	0.1	25	60	200	50	30	5	2.5	3.0	76.2
HVJX37.5K	37500	0.1	25	60	200	50	30	5	2.5	3.0	76.2
HVJX40K	40000	0.1	25	72	200	50	30	5	2.5	3.5	88.9
HVJX45K	45000	0.1	25	72	200	50	30	5	2.5	3.5	88.9

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 † The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.



REVERSE RECOVERY TEST CONDITIONS: I_F = 50mA, I_R = 100mA, I_{RR} = 25mA



HIGH VOLTAGE SILICON RECTIFIERS

KX15-100
KXS15-100

POWERSTACK

1.5 to 3.0A

Very High Current, Miniature

FEATURES

- PIV: From 1.5kV to 10kV
- 1.5 to 3.0A
- 250nS Reverse Recovery
- High Surge Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

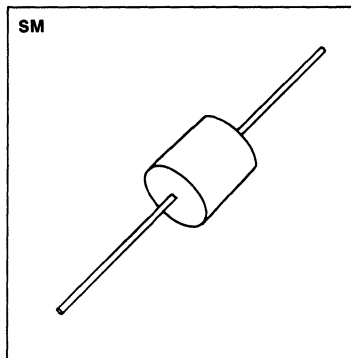
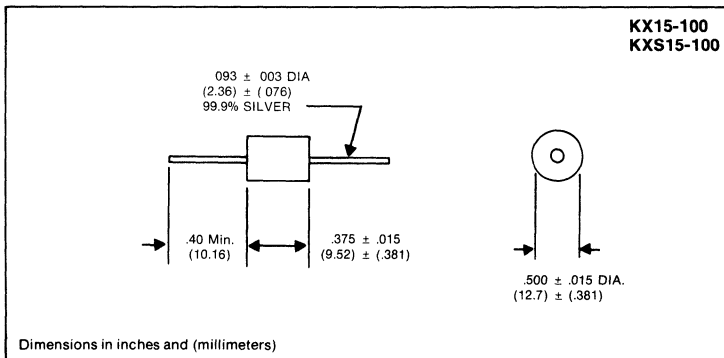
The KX/KXS silicon rectifier series is a unique concept for high current high voltage applications. Matched junction characteristics and low stray capacitance due to metallurgically bonded junctions eliminates the need for external compensation networks. These rectifiers utilize HVD's cylindrical die construction, which minimizes electrical and mechanical stress, insuring long life for commercial, military and industrial applications.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	1.5kV to 10kV
Maximum Average Rectified Current	See Electrical Specifications
Maximum One Cycle Surge 8.3mS	See Electrical Specifications
Operating Temperature Range	-55°C to +150°C
Storage Temperature Range	-55°C to +175°C

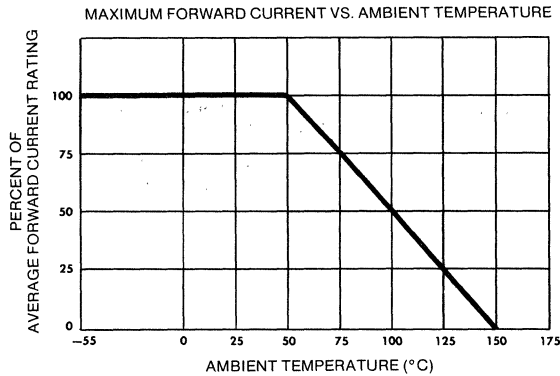
MECHANICAL SPECIFICATIONS



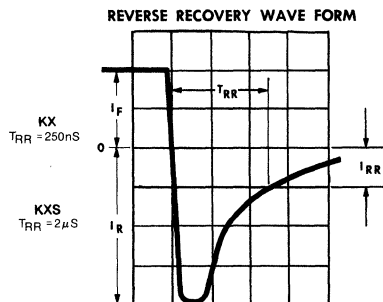
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)						MAXIMUM RATINGS				
Maximum Reverse Recovery Time		Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Average Rectified Current†			Maximum One Cycle Surge 8.3mS	Typical Thermal Impedance‡
250nS	2uS	PIV	I _R		V _F	I _O			I _F (surge)	R _{θJL}
Type	Type	V	25°C	100°C	V	50°C	100°C	120°C	A	°C/Watt
			μA	μA		A	A	A		
KX15	KXS15	1500	2.0	100	5.0	3.00	1.50	.75	200	2.0
KX20	KXS20	2000	2.0	100	5.0	3.00	1.50	.75	200	2.0
KX25	KXS25	2500	2.0	100	5.0	3.00	1.50	.75	200	2.0
KX30	KXS30	3000	2.0	100	7.0	2.20	1.10	.55	150	2.5
KX40	KXS40	4000	2.0	100	7.0	2.20	1.10	.55	150	2.5
KX50	KXS50	5000	2.0	100	7.0	2.20	1.10	.55	150	2.5
KX60	KXS60	6000	2.0	100	11.0	1.50	.75	.37	100	3.0
KX80	KXS80	8000	2.0	100	11.0	1.50	.75	.37	100	3.0
KX100	KXS100	10000	2.0	100	11.0	1.50	.75	.37	100	3.0

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 † The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.
 ‡†† Typical thermal impedance determined with rectifier mounted on infinite heat sinks 0.10" from device body using temperature of center junction and lead temperature adjacent to body.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.



REVERSE RECOVERY TEST CONDITIONS: I_F = 400mA, I_R = 800mA, I_{RR} = 200mA



HIGH VOLTAGE SILICON RECTIFIERS POWERSTACK

400mA-1.0A
High Current, Miniature

SX10-100
SXS10-100

FEATURES

- PIV: From 1kV to 10kV
- 400mA to 1.0A
- 250nS Reverse Recovery
- High Surge Ratings
- Low Reverse Leakage
- Corona Free

DESCRIPTION

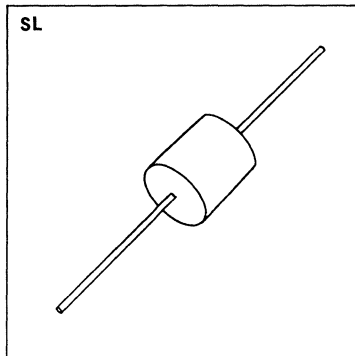
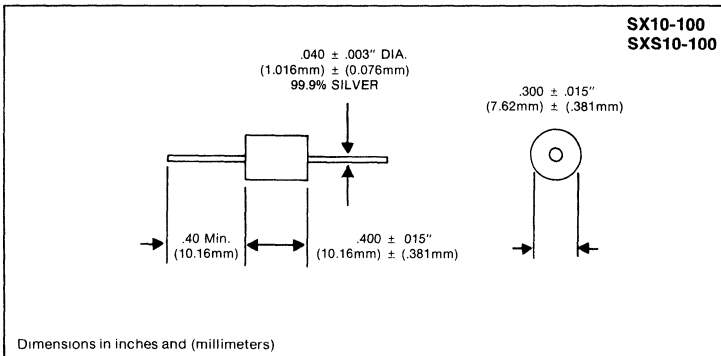
The SX/SXS silicon rectifier series is a unique concept for high current high voltage applications. Matched junction characteristics and low stray capacitance due to metallurgically bonded junctions eliminate the need for external compensation networks. These rectifiers utilize HVD's cylindrical die construction, which minimizes electrical and mechanical stress, insuring long life for commercial, military and industrial applications.



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	1kV to 10kV
Maximum Average Rectified Current	See Electrical Specifications
Maximum One Cycle Surge 8.3mS	See Electrical Specifications
Operating and Storage Temperature Range	-65°C to +150°C

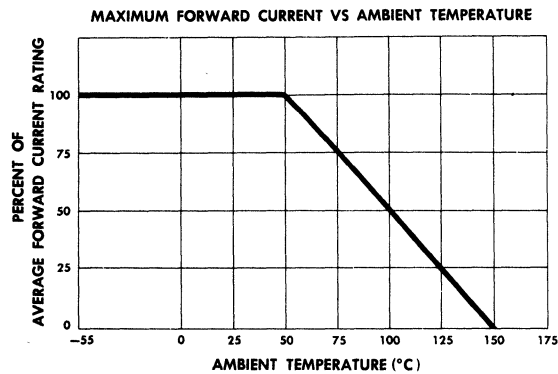
MECHANICAL SPECIFICATIONS



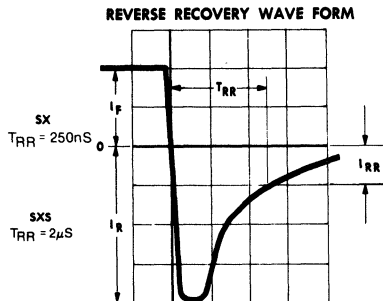
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)						MAXIMUM RATINGS			
Maximum Reverse Recovery Time §		Peak Inverse Voltage*	Maximum Reverse Current @ PIV		Maximum Forward Voltage @ I _O	Maximum Average Rectified Current†			Maximum One Cycle Surge 8.3mS
250nS	2µS	PIV	I _R		V _F	I _O			I _F (surge)
Type	Type	V	25°C µA	100°C µA	25°C V	50°C mA	100°C mA	125°C mA	A
SX10	SXS10	1000	1.0	25	5.5	1000	500	250	60
SX15	SXS15	1500	1.0	25	5.5	1000	500	250	60
SX20	SXS20	2000	1.0	25	5.5	1000	500	250	60
SX25	SXS25	2500	1.0	25	5.5	1000	500	250	60
SX30	SXS30	3000	1.0	25	7.5	600	300	150	40
SX40	SXS40	4000	1.0	25	7.5	600	300	150	40
SX50	SXS50	5000	1.0	25	7.5	600	300	150	40
SX60	SXS60	6000	1.0	25	11.0	400	200	100	25
SX80	SXS80	8000	1.0	25	11.0	400	200	100	25
SX100	SXS100	10000	1.0	25	11.0	400	200	100	25

*Operation and testing of devices over 10,000 V/inch may require re-encapsulation or immersion in a suitable dielectric material.
 †The stated, AVERAGE RECTIFIED CURRENT ratings require no heat sinking, special mounting or forced air across the body of the device.

NOTE: Maximum lead temperature for soldering is 250°C 3/8" (9.5mm) from case for 5 seconds.



Reverse recovery test conditions: I_F = 100mA, I_R = 200mA, I_{RR} = 50mA



RECTIFIER ASSEMBLIES

High Voltage Doorbell® Modules,
Standard and Fast Recovery

UDA, UDB, UDC, UDD ,
UDE, UDF SERIES

FEATURES

- PIV: from 2.5kV to 15kV
- Stackable to 600kV
- Current Ratings: to 7.7A
- Controlled Avalanche Characteristics
- Only Fused-in-Glass Diodes Used
- Recovery Time: to 500ns
- Modular Package For Easy Stacking

DESCRIPTION

This series of high-voltage, high-current stacks that incorporate a unique modular design makes it ideally suited for high power applications such as in radar systems as charger, hold-off and clipper diodes.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage

UDA, UDC Series 5kV to 15kV

UDB, UDD Series 2.5 kV to 7.5kV

UDE, UDF Series 2.5 kV to 5kV

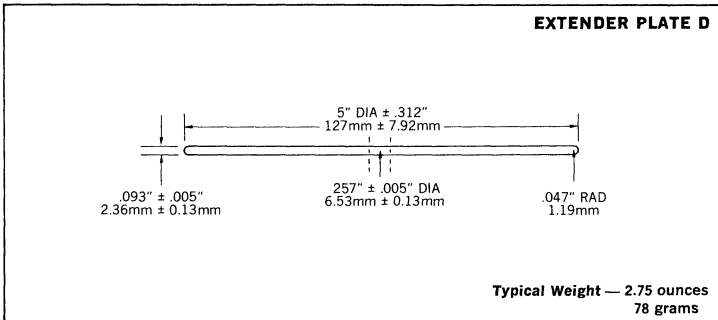
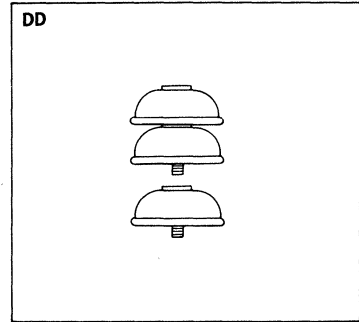
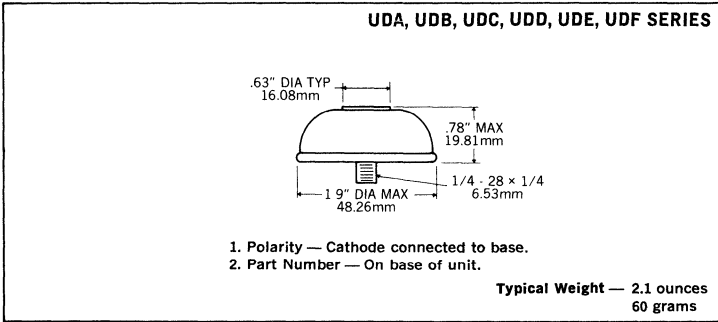
Maximum Average D.C. Output Current See Electrical Specifications

Non-Repitative Sinusoidal Surge (8.3ms) See Electrical Specifications

Operating and Storage Temperature Range -65°C to +150°C



MECHANICAL SPECIFICATIONS



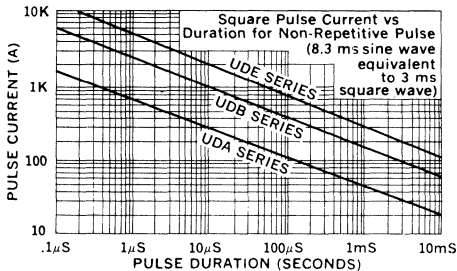
Electrical Specifications (at 25°C unless noted)						Maximum Ratings				
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV	Maximum Reverse Recovery Time	Maximum Average D.C. Output Current			Non-Repetitive Sinusoidal Surge (8.3ms) T _c = 100°C	Maximum Reverse Transient Energy Absorption	
					T _c = 75°C Air	T _c = 60°C Air with Extender Plate**	T _c = 50°C Oil			
Standard Recovery	UDE-2.5	2.5	5V @ 3.00A	10	—	± 6.00	7.00	7.70	200	8
	UDB-2.5	2.5	4V @ 1.50A	5		3.00	3.75	4.25	100	4
	UDE-5	5	10V @ 2.20A	10		± 4.50	5.00	5.50	200	14
	UDB-5	5	8V @ 1.00A	5		2.00	2.50	2.75	100	8
	UDA-5	5	8V @ 0.82A	2		1.65	2.00	2.20	30	1.5
	UDB-7.5	7.5	12V @ 0.70A	5		1.33	1.65	2.00	100	12
	UDA 7.5	7.5	12V @ 0.60A	2		1.25	1.55	1.75	30	2.5
	UDA-10	10	16V @ 0.50A	2		1.00	1.25	1.40	30	3
Fast Recovery	UDA-15	15	25V @ 0.33A	2	0.67	0.80	0.90	30	5	
	UDF-2.5	2.5	6V @ 2.20A	10	4.50	5.00	5.30	150	8	
	UDD-2.5	2.5	6V @ 1.20A	5	2.25	2.80	3.30	80	4	
	UDF-5	5	11V @ 1.60A	10	3.30	4.00	4.40	150	14	
	UDD-5	5	11V @ 0.75A	5	1.50	1.85	2.00	80	8	
	UDC-5	5	10V @ 0.70A	2	1.20	1.50	1.70	25	1.5	
	UDD-7.5	7.5	17V @ 0.50A	5	1.00	1.25	1.50	80	12	
	UDC-7.5	7.5	15V @ 0.50A	2	0.90	1.10	1.25	25	2.5	
UDC-10	10	20V @ 0.37A	2	0.75	0.90	1.00	25	3		
UDC-15	15	30V @ 0.25A	2	0.50	0.60	0.70	25	5		

*Measured in a reverse recovery circuit switching from 1.0A forward to 1.0A reverse current recovering to 0.5A.
 †Measured in a reverse recovery circuit switching from 0.5A forward to 1.0A reverse current recovering to 0.25A.

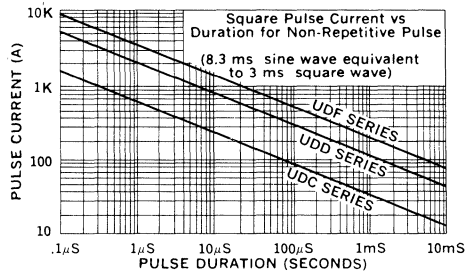
**These ratings are based on using "extender plates" that provide additional surface area to radiate heat. Because of possible corona effects caused by scratches on these plates, extreme care is necessary in their handling and they are not recommended where the working voltage exceeds 7.5KV/module. They should be carefully polished prior to installation.

‡These ratings are based on T_c = 100°C.

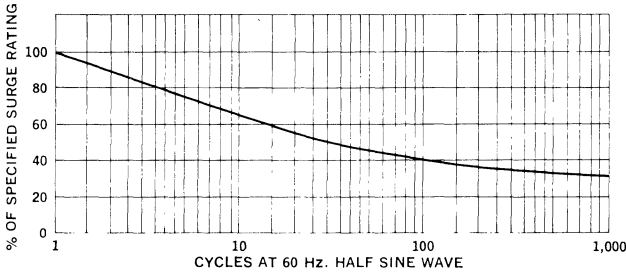
Forward Pulse Current vs. Pulse Duration



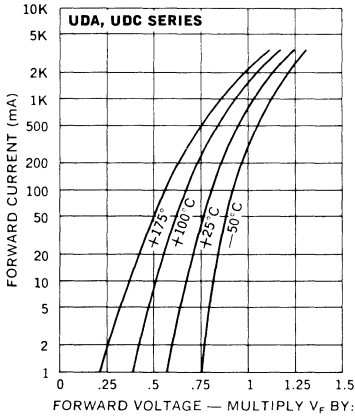
Forward Pulse Current vs. Pulse Duration



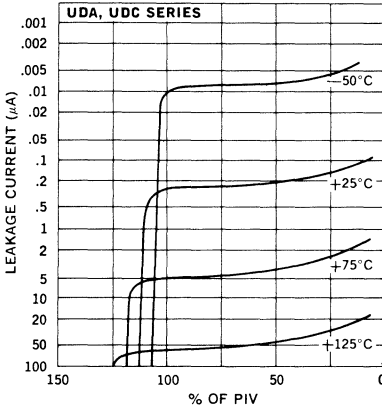
Multiple Surge Rating vs. Duration



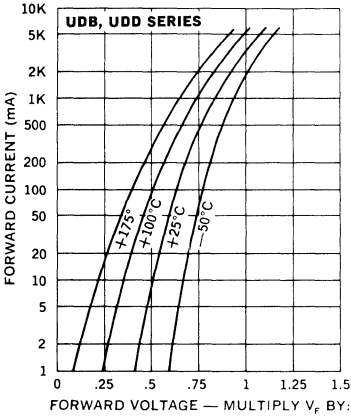
Typical Forward Voltage vs. Forward Current



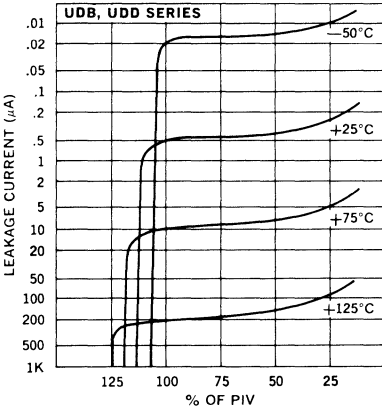
Typical Leakage Current vs. PIV



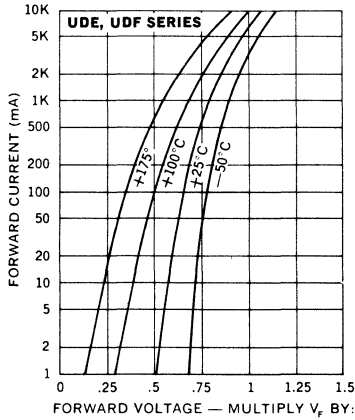
Typical Forward Voltage vs. Forward Current



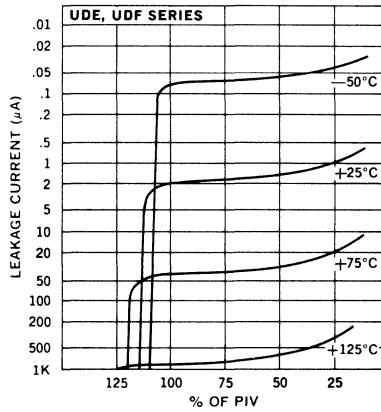
Typical Leakage Current vs. PIV



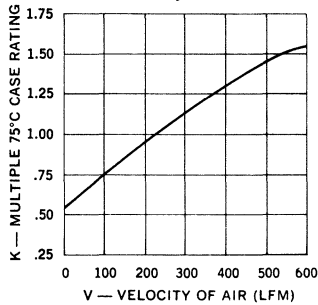
Typical Forward Voltage vs. Forward Current



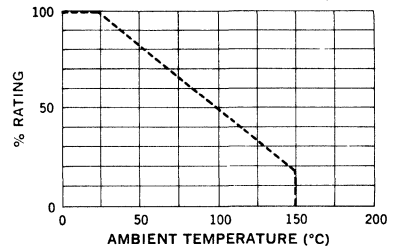
Typical Leakage Current vs. PIV



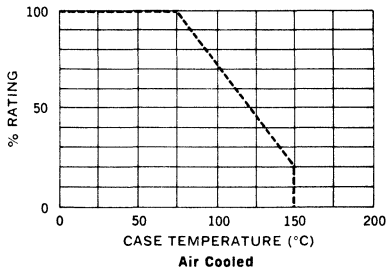
Output Current Ratio vs. Velocity of Air Flow



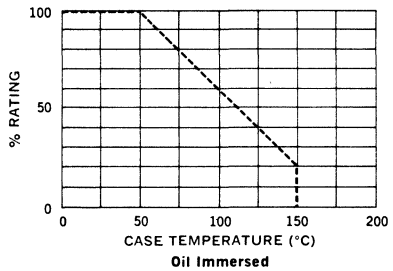
Current Derating Curve



Current Derating Curve



Current Derating Curve



RECTIFIER ASSEMBLIES

UFB, UFS, USB, USS SERIES

High Voltage Stacks,
Standard and Fast Recovery

FEATURES

- Controlled Avalanche Characteristics
- Only Fused-in-Glass Diodes Used
- High Forward and Reverse Surge Capability
- Transfer Molded for Voidless Construction
- Modular for Easy Stacking
- PIV: from 2.5 kV to 15kV
- Recovery Times: to 500ns
- Continuous Ratings: to 2.3A

DESCRIPTION

These assemblies uniquely combine a versatile stackable design with all the requirements for reliable high voltage operation. All modules are suitable for bridge or series operations.

7

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, USS Series 5.0 kV to 15kV
 Peak Inverse Voltage, USB Series 2.5 kV to 10kV
 Peak Inverse Voltage, UFS Series 5.0 kV to 10kV
 Peak Inverse Voltage, UFB Series 2.5 kV to 7.5 kV
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-Repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications
 Operating and Storage Temperature Range -65°C to +150°C

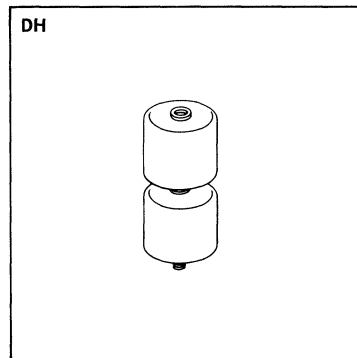
MECHANICAL SPECIFICATIONS

UFB, UFS, USB, USS SERIES

	ins.	mm.
A	.230-.235	5.84-5.97
B	.980-1.10	24.89-27.94
C	.020-.040	0.51-1.02
D	.320-.330	8.13-8.38
E	.97-1.00	24.64-25.40

Typical Weight: USS & UFS Series — 1.0 ounce
 28 grams

USB & UFB Series — 1.1 ounce
 31 grams



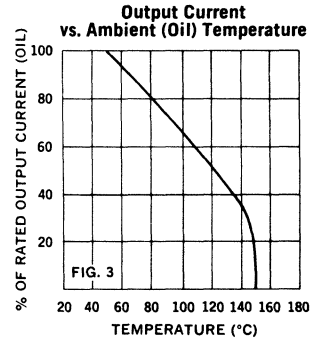
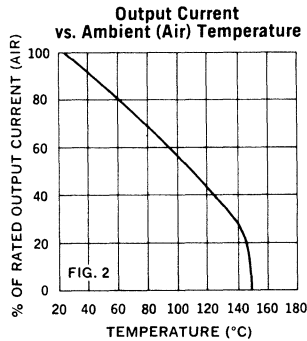
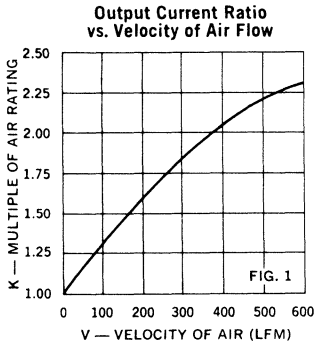
MARKING

Type number marked on unit.

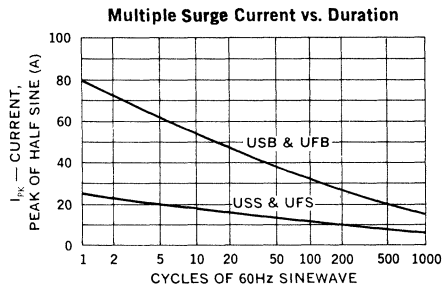
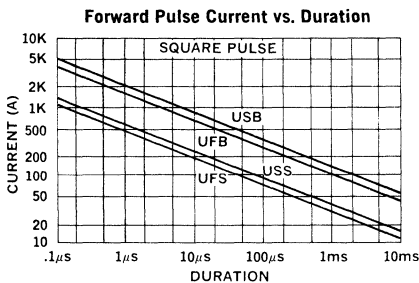
Polarity — Cathode connected to stud.

Electrical Specifications (at 25°C unless noted)						Maximum Ratings			
Type	PIV kV	Maximum Forward Voltage Drop	Leakage Current @ PIV μA	Maximum Reverse Recovery Time ns	Maximum Reverse Transient Energy Absorption joules	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms) Amps	
						T _A = 25°C AIR Amps	T _A = 50°C OIL Amps		
Standard Recovery	USS 5	5.0	9V @ 0.6A	5	—	1.5	0.60	1.1	25
	USS 7.5	7.5	13V @ 0.5A			2.5	0.45	0.91	
	USS 10	10	17V @ 0.3A			3.0	0.35	0.71	
	USS 15	15	25V @ 0.2A			5.0	0.25	0.51	
Standard Recovery	USB 2.5	2.5	5V @ 1.1A	10	—	3.0	1.1	2.3	80
	USB 5	5.0	9V @ 0.7A			6.0	0.68	1.5	
	USB 7.5	7.5	13V @ 0.5A			9.0	0.53	1.2	
	USB 10	10	17V @ 0.4A			12	0.43	1.0	
Fast Recovery	UFS 5	5.0	12V @ 0.5A	5	500* 350†	1.5	0.50	0.90	20
	UFS 7.5	7.5	18V @ 0.4A			2.5	0.38	0.75	
	UFS 10	10	23V @ 0.3A			3.0	0.30	0.58	
Fast Recovery	UFB 2.5	2.5	6V @ 0.9A	10	500* 350†	3.0	0.90	2.0	70
	UFB 5	5.0	12V @ 0.6A			6.0	0.58	1.3	
	UFB 7.5	7.5	18V @ 0.4A			9.0	0.45	1.0	

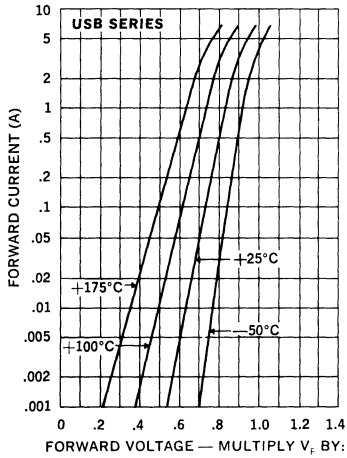
*Measured in a reverse recovery circuit switching from 1A forward to 1A reverse current recovering to 0.5A.
 †Measured in a reverse recovery circuit switching from .5A forward current to 1A reverse current, recovery to .25A.



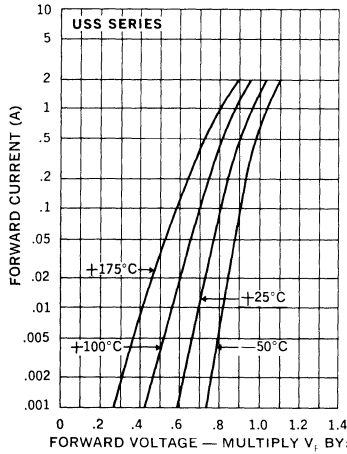
Application example: The rectifier is to be used in a cabinet at 60°C with ambient air moving at 400 LFM. The rating is reduced (Fig. 2) by a factor of 0.81 due to the elevated temperature, but it is enhanced by 2X (Fig. 1) due to the air flow. Hence the DC output current is 0.81 x 2, or 1.6 times the 25°C air rating.



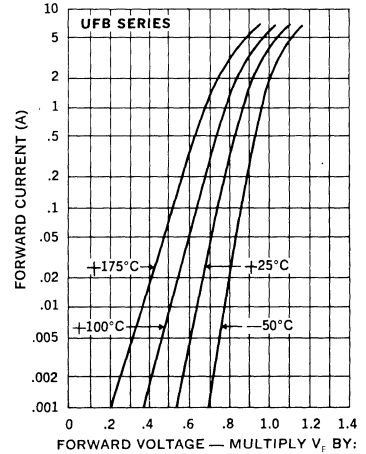
Typical Forward Voltage vs. Forward Current



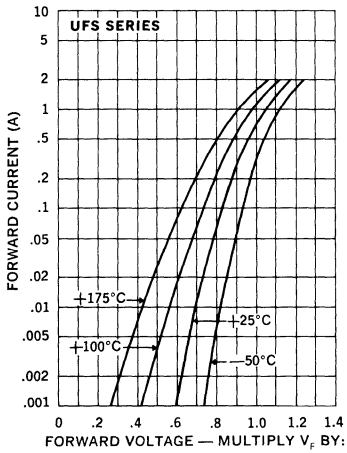
Typical Forward Voltage vs. Forward Current



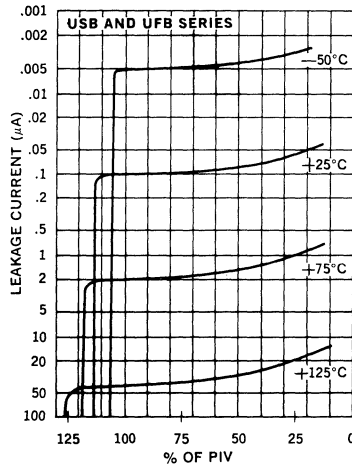
Typical Forward Voltage vs. Forward Current



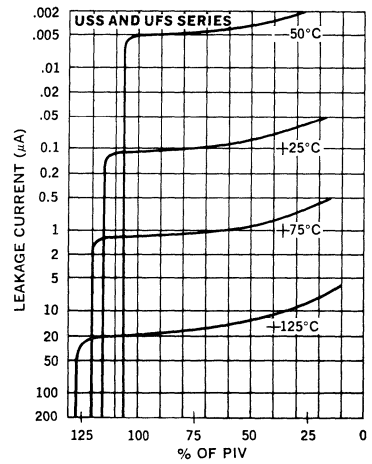
Typical Forward Voltage vs. Forward Current



Typical Leakage Current vs. PIV



Typical Leakage Current vs. PIV



RECTIFIER ASSEMBLIES

UGB, UGD, UGE, UGF SERIES

High Voltage Doorbell® Modules Standard and Fast Recovery

FEATURES

- Current Ratings: to 10A
- PIV: 2.5 kV to 10kV
- Recovery Times: to 500ns
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Stackable to 600kV
- Modular Package for Easy Stacking

DESCRIPTION

This series of high-voltage, high-current stacks that incorporate a unique modular design makes it particularly well-suited for high power applications such as in radar systems as charge, hold-off and clipper diodes.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage

UGB, UGD Series 5kV to 10kV

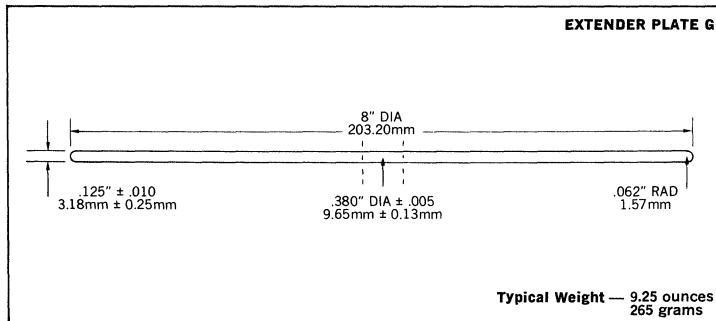
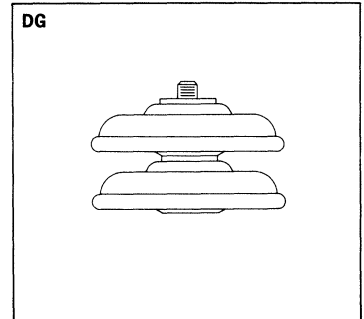
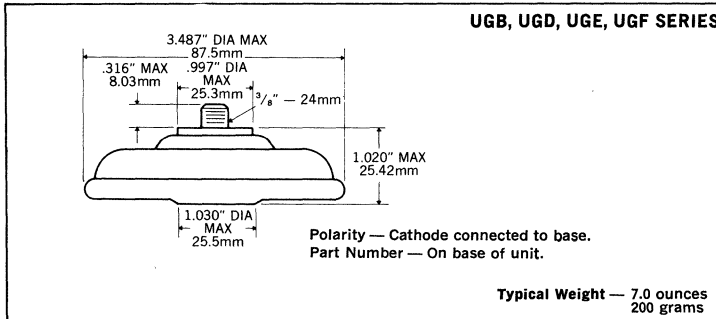
UGS, UGF Series 2.5kV to 7.5kV

Maximum Average D.C. Output Current See Electrical Specifications

Non-repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications

Operating and Storage Temperature Range -65°C to +150°C

MECHANICAL SPECIFICATIONS



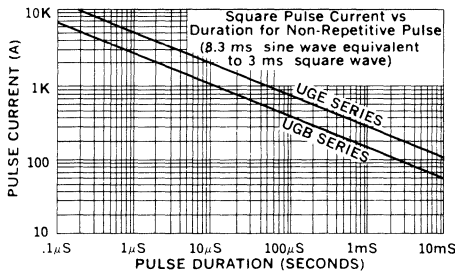
Electrical Specifications (at 25°C unless noted)					Maximum Ratings					
Type	PIV	Maximum Forward Voltage Drop	Maximum Leakage Current @ PIV	Maximum Reverse Recovery Time	Maximum Average D.C. Output Current			Non-repetitive Sinusoidal Surge (8.3ms)	Maximum Reverse Transient Energy Absorption	
					T _c = 75°C Air	T _c = 60°C Air with Extender Plate**	T _c = 50°C Oil			
					Amps	Amps	Amps	T _c = 100°C	joules	
Standard Recovery	UGE-2.5	2.5	5V @ 3.30A	10		6.60	8.25	10.00	200	8
	UGE-5	5	10V @ 2.50A	15		5.00	6.25	7.50	200	14
	UGB-5	5	9V @ 2.20A	5	—	4.40	5.50	6.60	100	7
	UGE-7.5	7.5	13V @ 1.60A	10		3.30	4.10	5.00	200	20
	UGB-7.5	7.5	13V @ 1.50A	5		3.00	3.75	5.00	100	10
	UGB-10	10	17V @ 1.10A	5		2.30	2.85	3.50	100	14
Fast Recovery	UGF-2.5	2.5	6V @ 2.50A	10		5.00	6.25	8.00	150	8
	UGF-5	5	11V @ 1.80A	10		3.75	4.70	6.00	150	14
	UGD-5	5	11V @ 1.60A	5	500*	3.30	4.10	4.80	80	7
	UGF-7.5	7.5	17V @ 1.20A	10	350†	2.50	3.10	4.00	150	20
	UGD-7.5	7.5	17V @ 1.10A	5		2.25	2.80	3.50	80	10
	UGD-10	10	22V @ 0.85A	5		1.75	2.20	2.50	80	14

*Measured in a reverse recovery circuit switching from 1.0A forward to 1.0A reverse current recovering to 0.5A.
 †Measured in a reverse recovery circuit switching from 0.5A forward to 1.0A reverse current recovering to 0.25A.

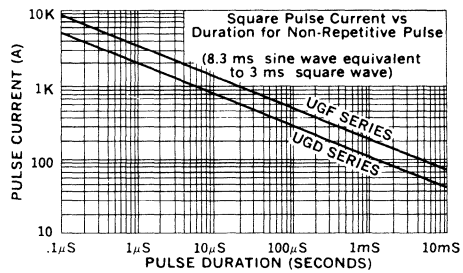
**These ratings are based on using "extender plates" that provide additional surface area to radiate heat. Because of possible corona effects caused by scratches on these plates, extreme care is necessary in their handling and they are not recommended where the working voltage exceeds 7.5KV/module. They should be carefully polished prior to installation.



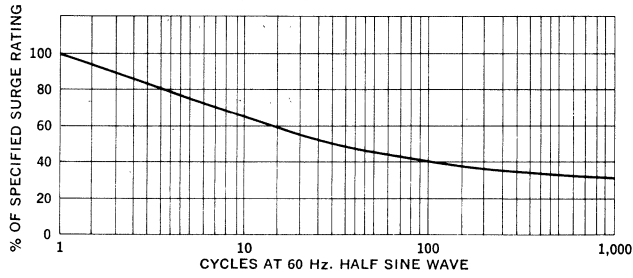
Forward Pulse Current vs. Pulse Duration



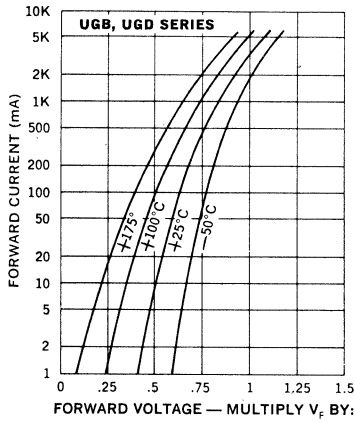
Forward Pulse Current vs. Pulse Duration



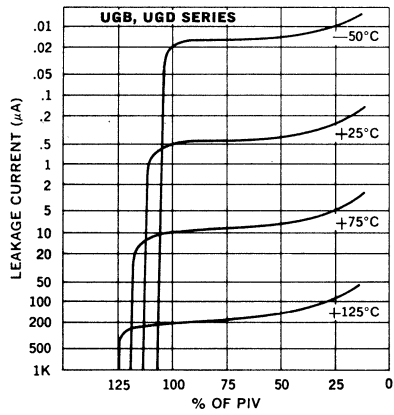
Multiple Surge Rating vs. Duration



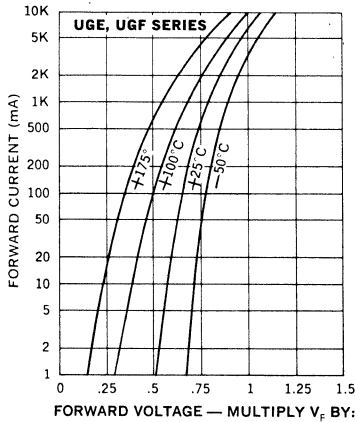
Typical Forward Voltage vs. Forward Current



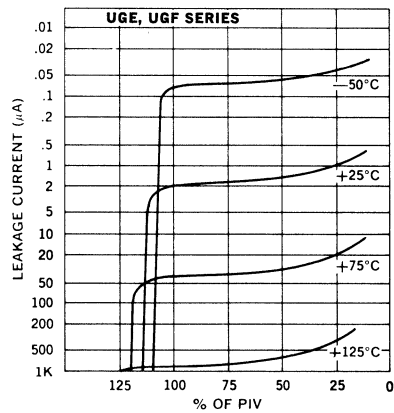
Typical Leakage Current vs. PIV

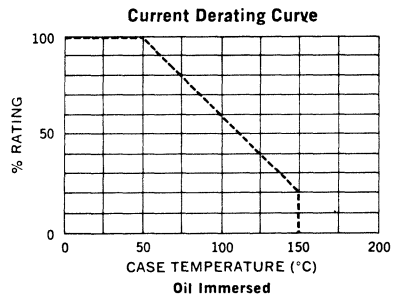
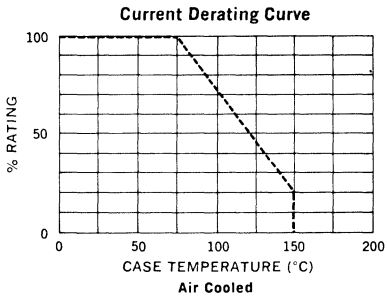
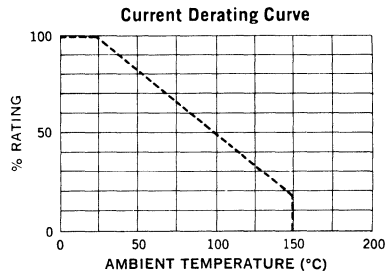
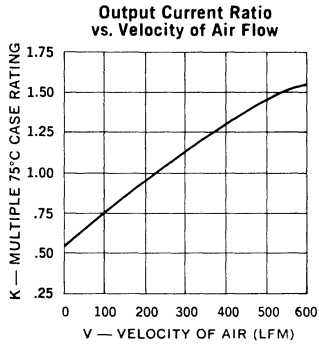


Typical Forward Voltage vs. Forward Current



Typical Leakage Current vs. PIV





RECTIFIER ASSEMBLIES

High Voltage Stacks, .125 Amp to 1 Amp, Standard and Fast Recovery

US12-US200A
USR12-USR180A

FEATURES

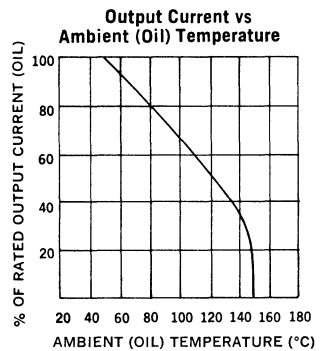
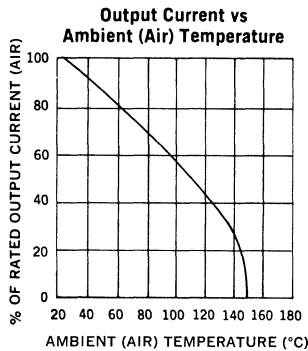
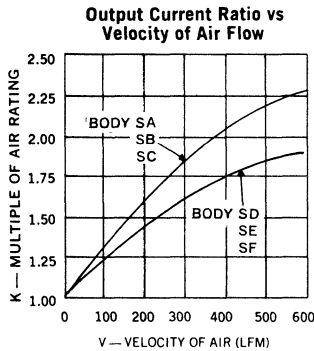
- Controlled Avalanche Characteristics
- Recovery Times: to 500ns
- Transfer Molded for Voidless Encapsulation
- High Forward and Reverse Surge Capability
- PIV: from 1200 to 20,000V
- Only Fused-in-Glass Diodes Used

DESCRIPTION

This series of High Voltage, Medium Current Stacks are assembled from hermetically sealed, controlled avalanche individual diodes. Therefore, they offer the ultimate in reliability for such applications as clipper diodes, back swing diodes and hold-off diodes in pulse modulators.

ABSOLUTE MAXIMUM RATINGS

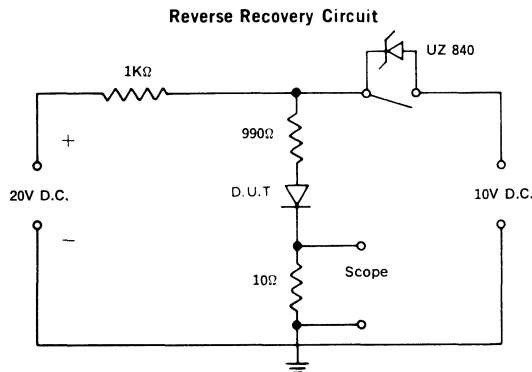
Peak Inverse Voltage	1200 to 20,000V
Maximum Average D.C. Output Current	See Electrical Specifications
Non-Repetitive Sinusoidal Surge (8.3ms)	20A
Operating and Storage Temperature Range	-65°C to +150°C



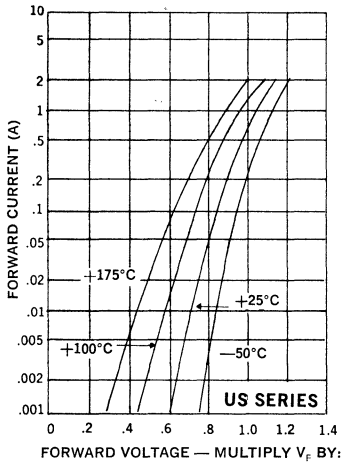
Electrical Specifications (at 25°C unless noted)							Maximum Ratings		
Type	PIV	Maximum Leakage Current at PIV		Maximum Forward Voltage Drop	Maximum Reverse Recovery Time†	Body Size	Max. Avg. D.C. Output Current		
		T _A = 25°C	T _A = 100°C				T _A = 25°C (Air)	T _A = 50°C (Oil)	
	V	μA	μA		ns		mA	mA	
Standard Recovery									
US 12	1200	2	100	2.0V @ 400mA		SA	1000	2500	
US 15	1500	2	100	3.0V @ 400mA	—	SA	800	2000	
US 18	1800	2	100	3.0V @ 400mA		SA	700	1750	
US 20	2000	2	100	4.0V @ 400mA		SA	600	1500	
US 25	2500	2	100	5.0V @ 400mA		SB	600	1500	
US 30	3000	2	100	6.0V @ 400mA	—	SB	500	1250	
US 35	3500	2	100	7.0V @ 200mA		SC	400	1000	
US 40	4000	2	100	7.0V @ 200mA	—	SC	350	850	
US 45A	4500	2	100	8.0V @ 200mA		SD	330	750	
US 50A	5000	2	100	9.0V @ 200mA		SD	330	750	
US 60A	6000	2	100	10.0V @ 200mA	—	SD	300	620	
US 70A	7000	2	100	12.0V @ 200mA		SD	300	620	
US 80A	8000	2	100	14.0V @ 100mA		SE	250	500	
US 100A	10000	2	100	17.0V @ 100mA	—	SE	250	500	
US 120A	12000	2	100	21.0V @ 100mA		SE	200	400	
US 150A	15000	2	100	26.0V @ 100mA		SF	200	400	
US 180A	18000	2	100	31.0V @ 100mA	—	SF	180	360	
US 200A	20000	2	100	34.0V @ 100mA		SF	180	360	
Fast Recovery									
USR 12	1200	5	150	3.3V @ 400mA	500	SA	750	1850	
USR 15	1500	5	150	4.0V @ 400mA	500	SA	600	1500	
USR 20	2000	5	150	5.5V @ 400mA	500	SB	500	1250	
USR 25	2500	5	150	6.6V @ 400mA	500	SB	400	1000	
USR 30	3000	5	150	7.7V @ 400mA	500	SC	400	1000	
USR 35	3500	5	150	8.8V @ 200mA	500	SC	350	850	
USR 40A	4000	5	150	9.9V @ 200mA	500	SD	300	750	
USR 45A	4500	5	150	11.0V @ 100mA	500	SD	250	625	
USR 50A	5000	5	150	13.0V @ 100mA	500	SD	250	625	
USR 60A	6000	5	150	15.4V @ 100mA	500	SD	220	500	
USR 70A	7000	5	150	17.6V @ 100mA	500	SE	220	500	
USR 80A	8000	5	150	20.0V @ 100mA	500	SE	200	400	
USR 100A	10000	5	150	24.0V @ 100mA	500	SE	200	400	
USR 120A	12000	5	150	31.0V @ 100mA	500	SF	150	300	
USR 150A	15000	5	150	33.0V @ 100mA	500	SF	150	300	
USR 180A	18000	5	150	35.0V @ 100mA	500	SF	125	250	



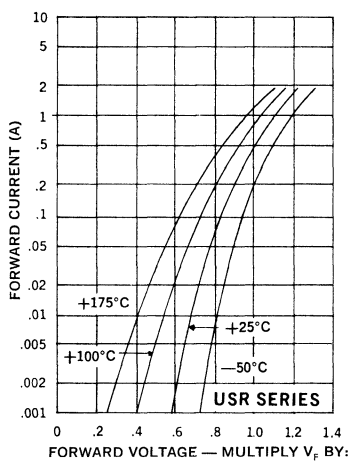
†Measured in a reverse recovery circuit switching from 10mA forward to 10mA reverse current recovering to 5mA.



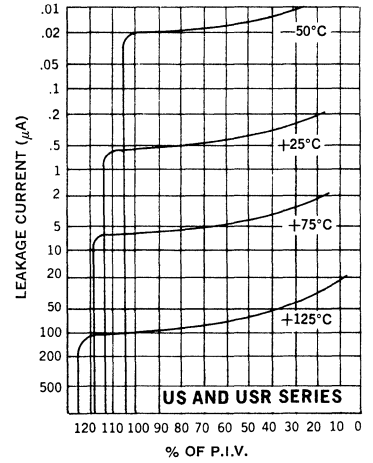
Typical Forward Current vs. Forward Voltage



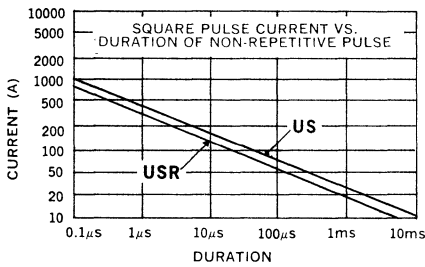
Typical Forward Current vs. Forward Voltage



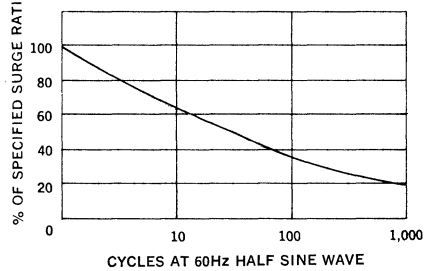
Typical Leakage Current vs. Voltage



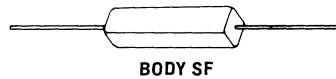
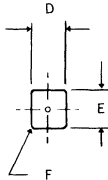
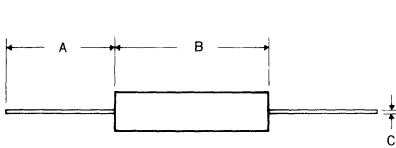
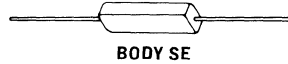
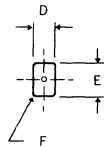
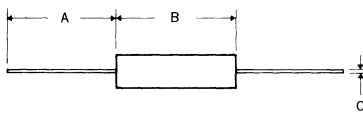
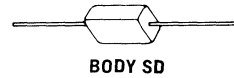
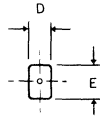
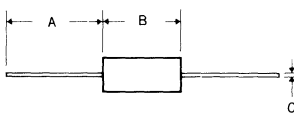
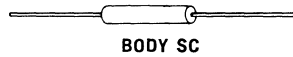
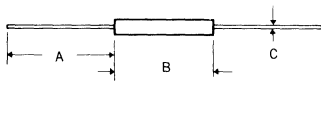
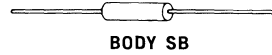
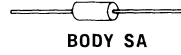
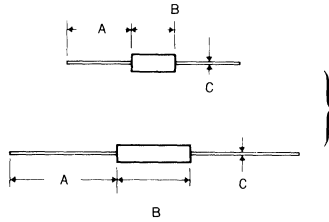
Forward Pulse Current vs Duration



Multiple Forward Surge Rating



MECHANICAL SPECIFICATIONS



7

	SA		SB		SC		SD		SE		SF	
	ins.	mm.	ins.	mm.	ins.	mm.	ins.	mm.	ins.	mm.	ins.	mm.
A	.75 MIN.	19.05 MIN.	1.25 MIN.	31.75 MIN.	1.25 MIN.	31.75 MIN.	1.25 MIN.	31.75 MIN.	1.25 MIN.	31.75 MIN.	1.25 MIN.	31.75 MIN.
B	.50 MAX.	12.70 MAX.	0.85 MAX.	21.59 MAX.	1.125 MAX.	28.58 MAX.	.875 MAX.	22.23 MAX.	1.375 MAX.	34.93 MAX.	1.75 MAX.	44.45 MAX.
C	.028 DIA.	.71 DIA.	.032 DIA.	.81 DIA.	.032 DIA.	.81 DIA.	.032 DIA.	.81 DIA.	.032 DIA.	.81 DIA.	.032 DIA.	.81 DIA.
D	.187 MAX.	4.75 MAX.	.187 MAX.	4.75 MAX.	.187 MAX.	4.75 MAX.	.250 MAX.	6.35 MAX.	.250 MAX.	6.35 MAX.	.400 MAX.	10.16 MAX.
E							.375 MAX.	9.53 MAX.	.375 MAX.	9.53 MAX.	.400 MAX.	10.16 MAX.
F									.078	1.98	.078	1.98

RECTIFIER BRIDGES, DOUBLERS & CENTER-TAPS

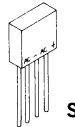
8

RECTIFIER BRIDGES

Single Phase Full-Wave Bridges



HJ, HK, HL, HM,
HN, HO, HP



S



G, GA, GH

STANDARD RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT					
	≅ .25A	.25— .75A	.75— 1.5A	1.5— 2.5A	4— 10A	10— 25A
100V			673-1 G or S	697-1 GA	680-1 NA	679-1 NB SPA25* MC
200V			673-2 G or S	697-2 GA	680-2 NA 469-1** MD	679-2 NB SPB25* MC
300V			673-3 G or S	697-3 GA	680-3 NA	679-3 NB
400V			673-4 G or S	697-4 GA	680-4 NA 469-2** MD	679-4 NB SPC25* MC
500V			673-5 G or S	697-5 GA	680-5 NA	679-5 NB
600V			673-6 G or S	697-6 GA	680-6 NA 469-3** MD	679-6 NB SPD25* MC
1.2kV		673-7 GH				
1.8kV		673-75 HJ				
2.4kV		673-8 HK				
2.5kV						
3.0kV		673-85 HL				
3.6kV	673-9 HM					
4.0kV						
4.2kV	673-10 HN					
4.8kV	673-11 HO					
5.0kV	673-12 HO					
7.5kV						
10kV						
15kV						

*Available as JAN

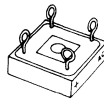
**Available as JAN, JANTX

Parentheses () designates product using stacked chips

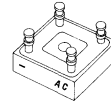
UNITRODE CORPORATION • 5 FORBES ROAD
LEXINGTON, MA 02173 • TEL. (617) 861-6540
TWX (710) 326-6509 • TELEX 95-1064

RECTIFIER BRIDGES

Single Phase Full Wave Bridges



NA, NB



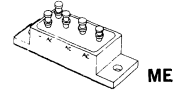
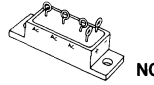
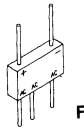
MA, MB, MC, MD

FAST RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT							
	≤ 25A	25—75A	75—1.5A	1.5—2.5A	4—10A	10—25A	25—35A	
50V						803-1 MB	802-1 MA	
100V			676-1 G or S	698-1 GA	684-1 NA	683-1 NB	803-2 MB	802-2 MA
125V						803-3 MB	802-3 MA	
150V						803-4 MB	802-4 MA	
200V			676-2 G or S	698-2 GA	684-2 NA	683-2 NB		
300V			676-3 G or S	698-3 GA	684-3 NA	683-3 NB		
400V			676-4 G or S	698-4 GA	684-4 NA	683-4 NB		
500V			676-5 G or S	698-5 GA	684-5 NA	683-5 NB		
600V			676-6 G or S	698-6 GA	684-6 NA	683-6 NB		
1.2kV		676-12 HJ						
1.8kV		676-18 HK						
2.4kV		676-24 HL						
2.5kV								
3.0kV		676-30 HM						
3.6kV	676-36 HN							
4.0kV								
4.2kV	676-42 HO							
4.8kV	676-48 HP							
5.0kV	676-50 HP							
7.5kV								
10kV								
15kV								
Reverse Recovery Time (max.)	500ns	500ns	500ns	500ns	500ns	500ns	50ns	50ns

Parentheses () designates product using stacked chips

Three Phase Full-Wave Bridge



STANDARD RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT			
	1—3A	4.5—15A	15—25A	
50V				
100V	700-1 F	695-1 NC	678-1 NC	
125V				
150V				
200V	700-2 F	695-2 NC	678-2 NC	483-1* ME
300V	700-3 F	695-3 NC	678-3 NC	
400V	700-4 F	695-4 NC	678-4 NC	483-2* ME
500V	700-5 F	695-5 NC	678-5 NC	
600V	700-6 F	695-6 NC	678-6 NC	483-3* ME
2.5kV				
5.0kV				
7.5kV				
10kV				

FAST RECOVERY

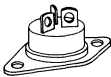
Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT				
	1—3A	4.5—15A	15—25A		25—40A
50V				801-1 ME	800-1 ME
100V	701-1 F	696-1 NC	682-1 NC	801-2 ME	800-2 ME
125V				801-3 ME	800-3 ME
150V				801-4 ME	800-4 ME
200V	701-2 F	696-2 NC	682-2 NC		
300V	701-3 F	696-3 NC	682-3 NC		
400V	701-4 F	696-4 NC	682-4 NC		
500V	701-5 F	696-5 NC	682-5 NC		
600V	701-6 F	696-6 NC	682-6 NC		
2.5kV					
3.0kV					
4.0kV					
5.0kV					
Reverse Recovery Time (max.)	500ns	500ns	500ns	50ns	50ns

* Available as JANTX
 Parentheses () designates product using stacked chips

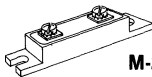
Parentheses () designates product using stacked chips

RECTIFIER BRIDGES

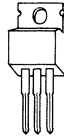
Doublers and Center-Tap Rectifiers



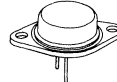
M-1



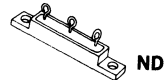
M-2



TO-220AB



TO-3

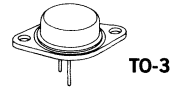
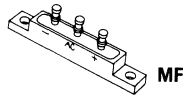
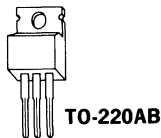
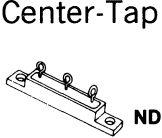


ND

Peak Inverse Voltage Per Leg	SCHOTTKY					STANDARD RECOVERY	
	AVERAGE D.C. OUTPUT CURRENT						
	12A	16A	60A	100A	200A	0—2A	2—15A
20V	USD620C TO-220AB	USD720C TO-220AB	USD320C TO-3				
35V	USD635C TO-220AB	USD735C TO-220AB	USD335C TO-3				
40V	USD640C TO-220AB	USD740C TO-220AB	USD345C SD241 TO-3	USM140C M-1	USM20040C M-2		
45V	USD645C TO-220AB	USD745C TO-220AB		USM145C M-1	USM20045C M-2		
50V				USM150C M-1	USM20050C M-2		
100V							681-1 ND
125V							
150V							
200V							681-2 ND
300V							681-3 ND
400V							681-4 ND
500V							681-5 ND
600V							681-6 ND

RECTIFIER BRIDGES

Doublers and Center-Tap Rectifiers



Peak Inverse Voltage Per Leg	FAST RECOVERY		SUPER FAST RECOVERY		ULTRA-FAST RECOVERY		
	AVERAGE D.C. OUTPUT CURRENT						
	1—2A	2—15A	16A	25A	16A	20A	30A
20V							
35V							
40V							
45V							
50V			SES5401C* TO-220AB	SES5601C* TO-3	UES2401* TO-220AB	804-1 MF	UES2601 TO-3
100V		689-1 ND	SES5402C* TO-220AB	SES5602C* TO-3	UES2402* TO-220AB	804-2 MF	UES2602 TO-3
125V						804-3 MF	
150V			SES5403C* TO-220AB	SES5603C* TO-3	UES2403* TO-220AB	804-4 MF	UES2603 TO-3
200V		689-2 ND	SES5404C* TO-220AB		UES2404* TO-220AB		UES2604 TO-3
300V		689-3 ND					UES2605 TO-3
400V		689-4 ND					UES2606 TO-3
500V		689-5 ND					
600V		689-6 ND					
Reverse Recovery Time (max.)		500ns	100ns	100ns	35ns	50ns	35-50ns

*Center-tap only

Parentheses () designates product using stacked chips

8

RECTIFIER ASSEMBLIES

Single Phase Bridges, 10 Amp, Military Approved

JAN & JANTX 469-1
JAN & JANTX 469-2
JAN & JANTX 469-3

FEATURES

- Qualified to MIL-S-19500/469
- Current Rating: to 10A
- PIV: from 200 to 600V
- Surge Ratings: to 100A
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

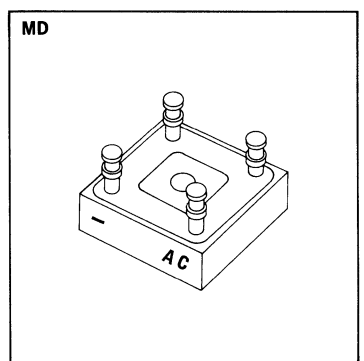
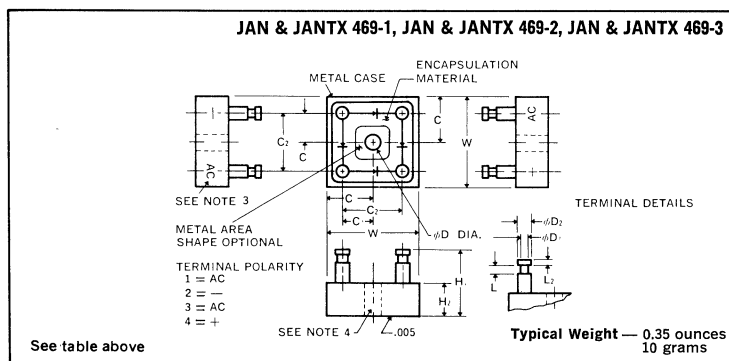
This series of military high-current single-phase bridge offer the utmost in reliability as required in military system designs. The TX series is assembled with diodes which have been subjected to 100% screening tests.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	200 to 600V
Maximum Average D.C. Output Current	
@ $T_C = +55^\circ\text{C}$	10A
@ $T_C = +100^\circ\text{C}$	6A
Non-Repetitive Sinusoidal Surge (8.3ms)	
@ $T_C = +55^\circ\text{C}$	100A
Operating and Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Thermal Resistance Junction to Ambient	$25^\circ\text{C}/\text{W}$
Junction to Case	$5^\circ\text{C}/\text{W}$

Ltr	Dimensions			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
C ₁	.367	.375	9.32	9.53
C ₂	.350	.450	8.89	11.43
C ₃	.175	.225	4.45	5.72
ϕD_1	.139	.149	3.53	3.78
ϕD_2	.091	.101	2.31	2.57
ϕD_3	.066	.076	1.68	1.93
H ₁		.570		14.48
H ₂		.370		9.40
L ₁	.088	.098	2.24	2.49
L ₂	.020	.030	.51	.76
W	.735	.750	18.67	19.05

MECHANICAL SPECIFICATIONS



NOTES:

1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Terminals shall be tinned.
3. Polarity shall be marked on the bridge body adjacent to terminals. Terminal numbers are for reference and do not have to be marked on the bridge; however, terminal (1) shall be indicated by a mechanical index such as a line, flattened corner, etc., visible from the top (terminal surface) of the device.
4. Point at which T_C is read shall be in metal part of a case as shown on drawing.

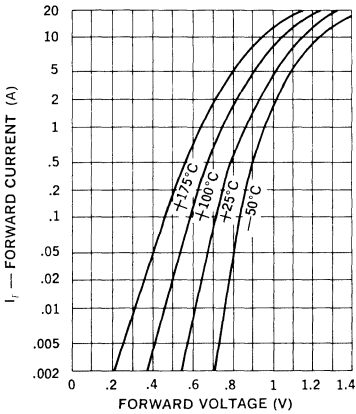
Electrical Specification (at 25°C unless noted)

Type	PIV Per Leg Volts	Minimum Reverse Breakdown Voltage Per Leg @ 50 μ A Volts	Maximum Forward Voltage Drop Per Leg*	Maximum Reverse Recovery Time† μ S	Maximum Leakage Current Per Leg @ PIV	
					T _c = 25°C μ A	T _c = 100°C μ A
JAN & JANTX 469-1	200	240	1.35V @ 15.7A(pk)	2	2	125
JAN & JANTX 469-2	400	460			2	125
JAN & JANTX 469-3	600	660			2	125

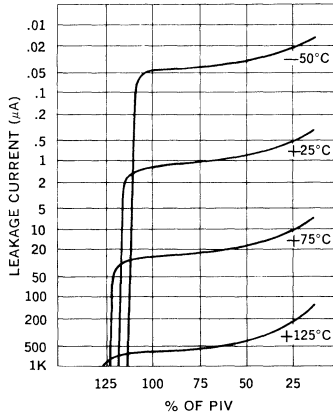
*Maximum forward voltage drop is measured at a pulse width of 8.3ms.

†Measured in a reverse-recovery circuit switching from 0.5A forward to 1.0A reverse current recovering to 0.25A.

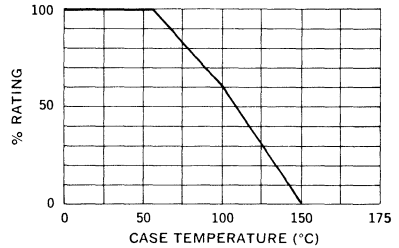
Typical Forward Voltage Per Leg vs. Forward Current



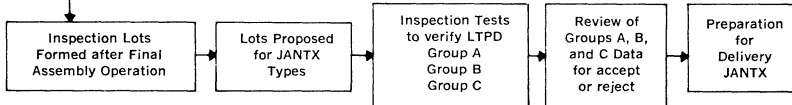
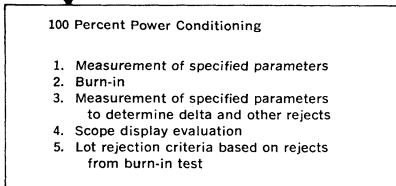
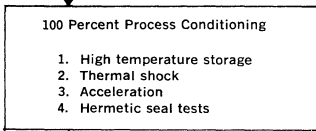
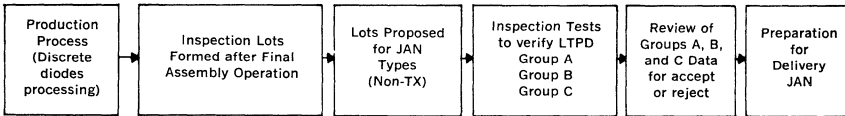
Typical Leakage Current vs. PIV



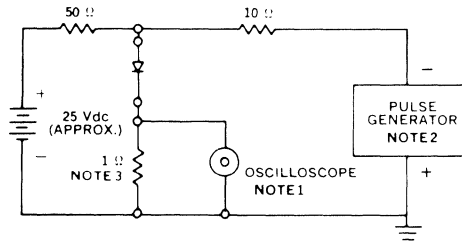
Current Derating Curve



8



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time \leq 3ns; input impedance = 50 Ω .
2. Pulse Generator: Rise time \leq 8ns; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIER ASSEMBLIES

Three Phase Bridges, 25 Amp,
Military Approved

JANTX 483-1
JANTX 483-2
JANTX 483-3

FEATURES

- Qualified to MIL-S-19500/483
- Current Rating: 25A
- PIV: from 200 to 600V
- Surge Ratings: 150A
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

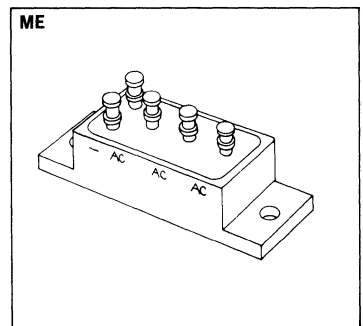
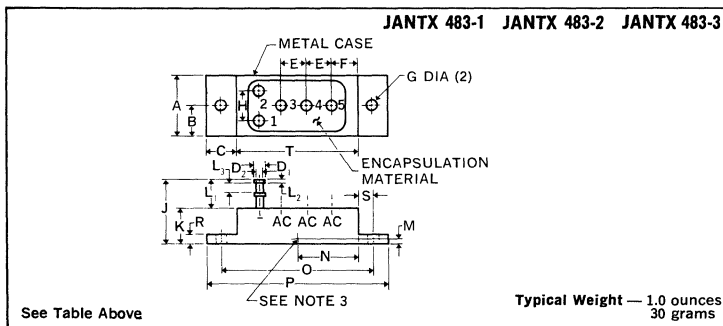
This military high-current three phase bridge series is assembled with diodes which have been subjected to TX type screening tests. This series of bridges offers the utmost in high reliability as normally required in military system design.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	200 to 600V
Maximum Average D.C. Output Current	
@ $T_C = 55^\circ\text{C}$	25A
@ $T_C = 100^\circ\text{C}$	18.5A
Non-Repetitive Sinusoidal Surge (8.3ms)	
@ $T_C = 55^\circ\text{C}$	150A
Operating and Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Thermal Resistance Junction to Ambient	20°C/W
Junction to Case	2.5°C/W

LTR	DIMENSIONS			
	INCH		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.730	.770	18.54	19.56
B	.355	.395	9.02	10.03
C	.355	.395	9.02	10.03
D ₁	.141	.151	3.58	3.84
D ₂	.108	.118	2.74	3.00
E	.355	.395	9.02	10.03
F	.230	.270	5.84	6.86
G	.149	.189	3.78	4.80
H	.355	.395	9.02	10.03
J		.82		20.83
K	.39	.51	9.91	12.95
L ₁	.240	.320	6.10	8.13
L ₂	.015	.030	.38	.76
L ₃	.100	.125	2.54	3.18
M	.040	.060	1.02	1.52
N	.72	.78	18.29	19.81
O	1.84	1.90	46.74	48.26
P	2.22	2.28	56.39	57.91
R	.09	.15	2.29	3.81
S	.168	.208	4.27	5.28
T	1.47	1.53	37.34	38.86

MECHANICAL SPECIFICATIONS



NOTES:

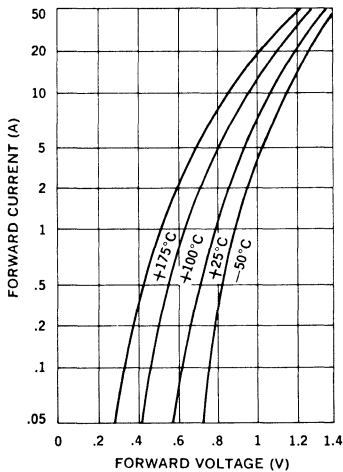
1. Terminals shall be tinned.
2. Polarity shall be marked as shown on drawing.
3. Point at which T_C is read (shall be in metal part of case).

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

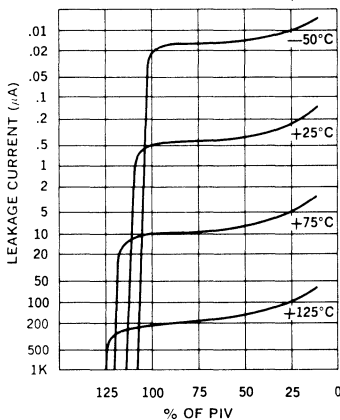
Type	PIV Per Leg	Breakdown Voltage Per Leg @ 50 μ A	Maximum Forward Voltage Drop Per Leg*	Maximum Leakage Current Per Leg @ PIV	
				T _C = 25°C	T _C = 100°C
	Volts	Volts	μ A	μ A	
JANTX 483-1	200	240	1.3V @ 39A (pk)	2	200
JANTX 483-2	400	480			
JANTX 483-3	600	660			

* Maximum forward voltage drop is measured at a pulse width of 8.3ms, duty cycle \leq 2%.

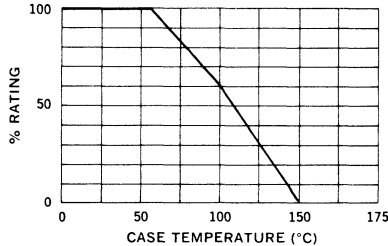
Typical Forward Voltage Per Leg vs. Forward Current



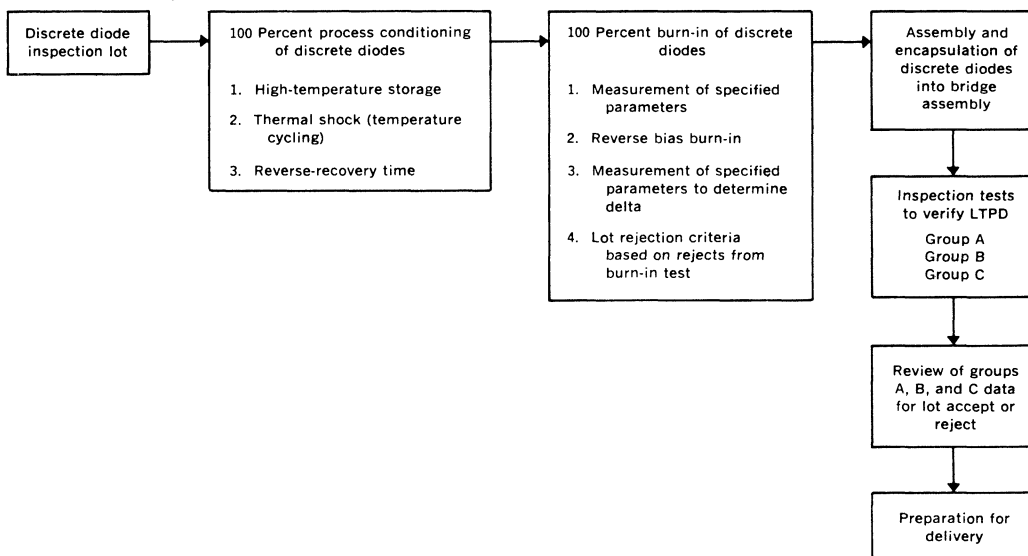
Typical Leakage Current vs. PIV



Current Derating Curve



8



RECTIFIER ASSEMBLIES

673, 676 SERIES

Single Phase Bridges, 1.5Amp,
Standard and Fast Recovery

FEATURES

- Miniature Package
- Surge Ratings: to 25A
- PIV's: from 100 to 600V
- Recovery Times: to 500ns
- Controlled Avalanche Characteristics
- Only Fused-in-Glass Diodes Used

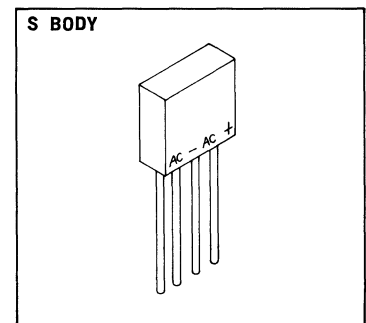
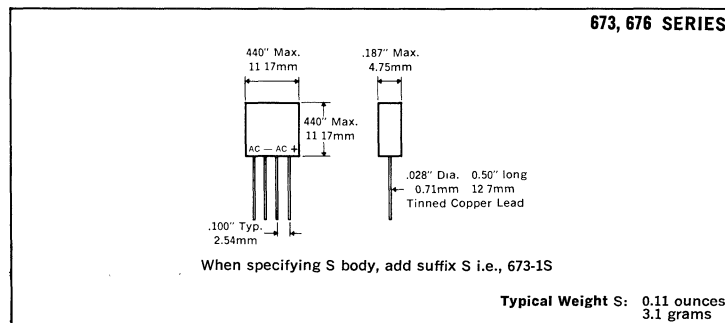
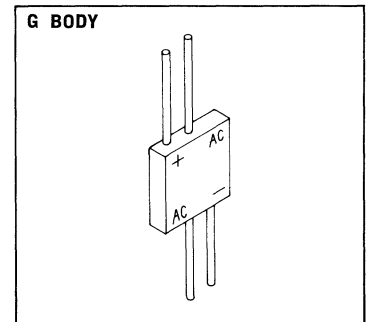
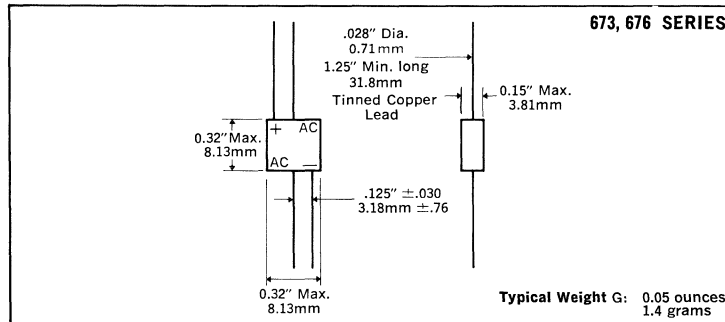
DESCRIPTION

These miniature transfer-molded single-phase power bridges are designed for universal application in power supplies. One basic bridge assembly comes in a choice of lead configurations for mounting in wired chassis or on printed boards.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 100 to 600V
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-Repetitive Sinusoidal Surge (8.3mS) See Electrical Specifications
 Operating and Storage Temperature Range -65°C to +150°C
 Thermal Resistance Junction to Ambient 50°C/W

MECHANICAL SPECIFICATIONS



MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

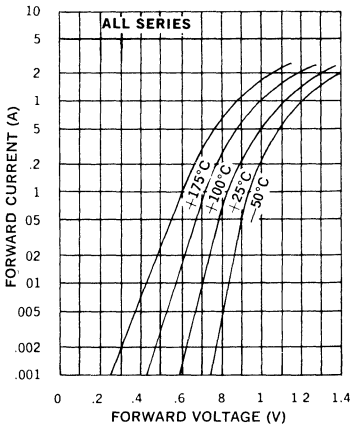
Part number is printed on the body.



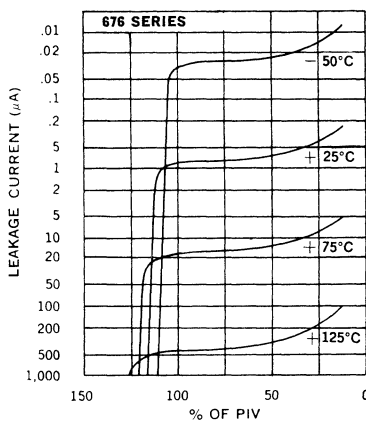
Electrical Specifications (at 25°C unless noted)					Maximum Ratings			
Type	PIV Per Leg	Maximum Forward Drop Per Leg	Leakage Current Per Leg		Maximum Reverse Recovery Time†	Maximum Average D.C. Output Current T _A = 25°C	Non-Repetitive Sinusoidal Surge (8.3mS)	
			T _A = 25°C	T _A = 100°C				
	Volts		μA	μA	ns	Amps	Amps	
Standard Recovery	673-1	100	1.1V @ 1.0A	2	100	—	1.5	25
	673-2	200						
	673-3	300						
	673-4	400						
	673-5	500						
	673-6	600						
Fast Recovery	676-1	100	1.1V @ 0.5A	3	150	500	1.0	20
	676-2	200						
	676-3	300						
	676-4	400						
	676-5	500						
	676-6	600						

†Measured in a reverse recovery circuit switching from 10mA forward to 10mA reverse current recovering to 5mA.

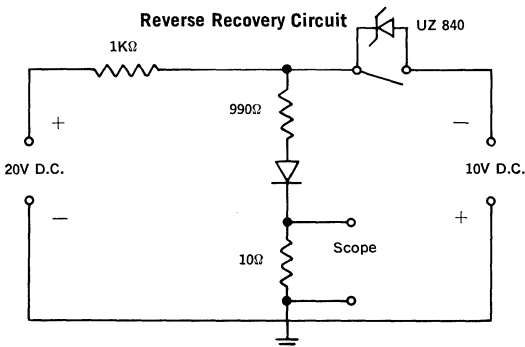
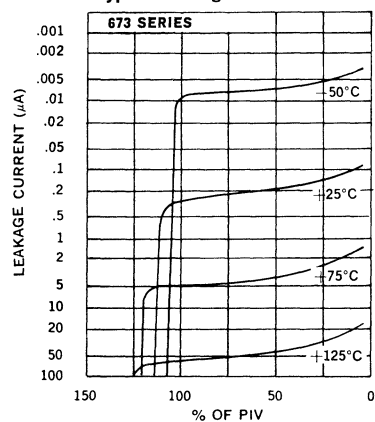
Typical Forward Voltage Per Leg vs. Forward Current



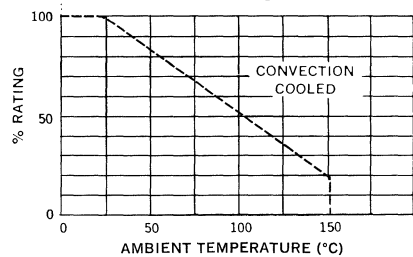
Typical Leakage Current vs. PIV



Typical Leakage Current vs. PIV



Current Derating Curve



RECTIFIER ASSEMBLIES

Single Phase Bridges, High Voltage
0.125-0.6 Amp, Standard and Fast Recovery

673, 676 SERIES
(1200-5000V)

FEATURES

- Miniature High Voltage Bridges
- Continuous Ratings: to 0.6A
- Surge Ratings: to 15A
- PIV's: from 1200 to 5000V
- Recovery Times: to 500ns
- Controlled Avalanche Characteristics
- Only Fused in Glass Diodes Used

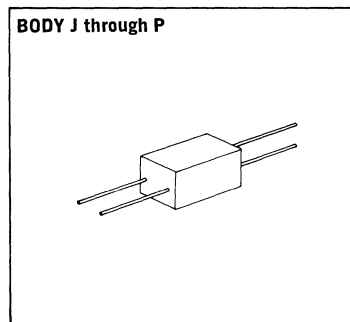
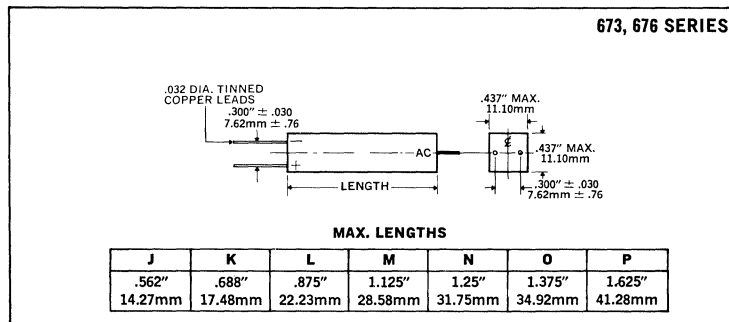
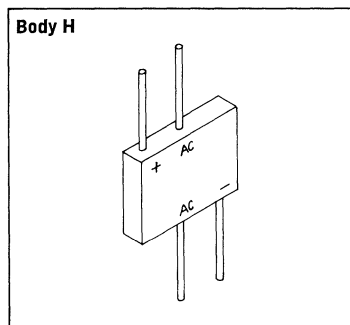
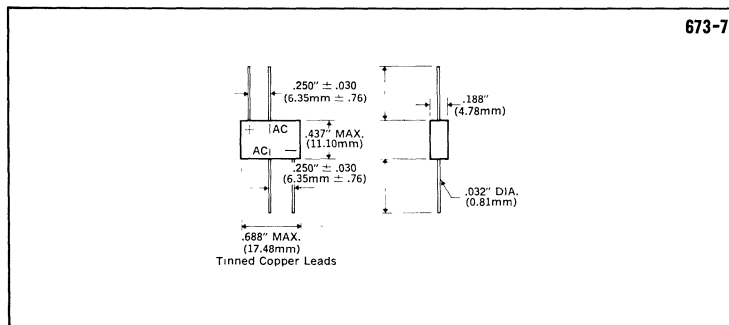
DESCRIPTION

These miniature molded high-voltage single phase bridges are designed for universal application in power supplies. The miniature package is shatterproof and is capable of handling extremes in temperature, vibration and shock. These bridges, therefore are ideally suited for miniaturized, tightly packaged equipment operating in extreme environments.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 1200 to 5000V
Maximum Average D.C. Output Current See Electrical Specifications
Non-repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications
Operating and Storage Temperature Range -65°C to $+150^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient 50°C/W

MECHANICAL SPECIFICATIONS



MARKING

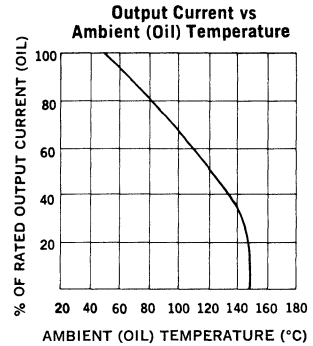
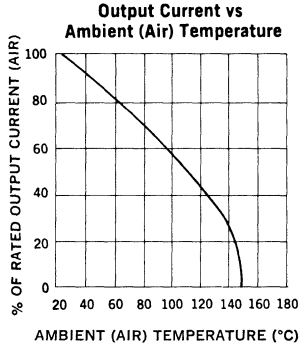
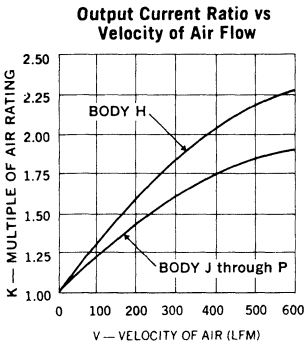
Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative Output	—

Part number is printed on the body.

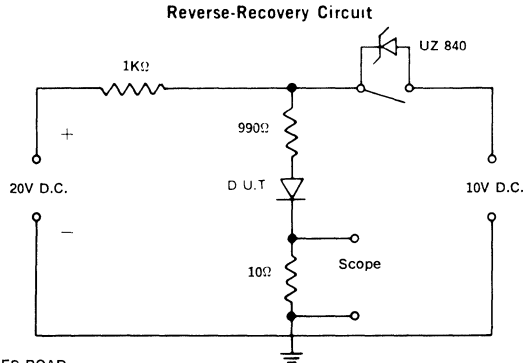


Type		Electrical Specifications at 25°C					Maximum Ratings			
		PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time*	Body Size	Maximum Average D.C. Output Current		Non-repetitive Sinusoidal Surge (8.3ms)
				T _A = 25°C	T _A = 100°C			T _A = 25°C	T _A = 50°C	
				μA	μA			ns	Amps	
Standard Recovery	673-7 673-75 673-8 673-85 673-9 673-10 673-11 673-12	1200 1800 2400 3000 3600 4200 4800 5000	2.2V @ 0.4A 3.3V @ 0.4A 4.4V @ 0.4A 5.5V @ 0.3A 6.6V @ 0.2A 7.7V @ 0.2A 8.8V @ 0.15A 9.0V @ 0.15A	2	100		H J K L M N O J	0.6 0.5 0.4 0.3 0.2 0.18 0.16 0.16	1.5 1.25 1.0 0.75 0.5 0.45 0.4 0.4	15
Fast Recovery	676-12 676-18 676-24 676-30 676-36 676-42 676-48 676-50	1200 1800 2400 3000 3600 4200 4800 5000	3.3V @ 0.3A 4.4V @ 0.2A 5.5V @ 0.2A 7.7V @ 0.2A 8.8V @ 0.15A 9.9V @ 0.15A 11V @ 0.15A 11V @ 0.15A	5	150	500	K L M N O P P	0.4 0.35 0.325 0.25 0.175 0.15 0.135 0.125	1.0 0.85 0.8 0.625 0.425 0.375 0.325 0.3	10

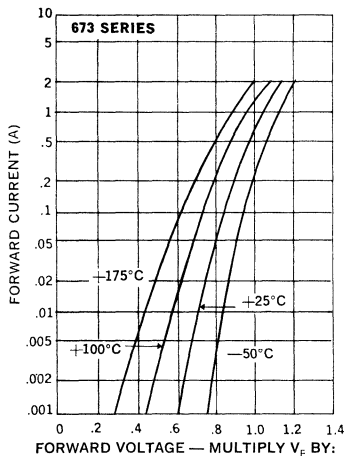
*Measured in a reverse recovery circuit switching from 10mA forward to 10mA reverse current recovering to 5mA.



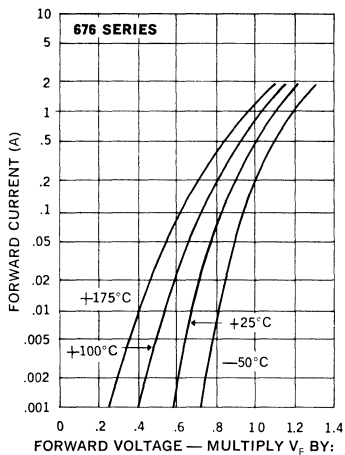
Application example: The rectifier is to be used in a cabinet at 60°C with ambient air moving at 400 LFM. The rating is reduced (Fig. 2) by a factor of 0.81 due to the elevated temperature, but is enhanced by 2.X (Fig. 1) due to the air flow. Hence the DC output current is 0.81 x 2, or 1.6 times the 25°C air rating.



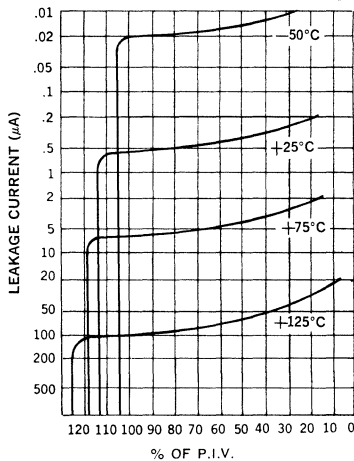
Typical Forward Voltage vs Forward Current



Typical Forward Voltage vs Forward Current



Typical Leakage Current vs. Voltage



RECTIFIER ASSEMBLIES

Three Phase Bridges, 15-25 Amp,
Standard and Fast Recovery Magnum®

678, 682, 695
696 SERIES

FEATURES

- Current Rating: to 25A
- PIVs: from 100 to 600V
- Only Fused-in-Glass Diodes Used
- Recovery Times: to 500ns
- Controlled Avalanche Characteristics
- Surge Ratings: to 150A
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

This series of three phase MAGNUM® bridges offer the ultimate in high current power supply applications. The fast recovery series allows operation at full power at high frequencies (up to 40KHz squarewave), often used in choppers, inverters and converters in aircraft, missiles, etc., equipment.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 100 to 600V
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-Repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications
 Operating and Storage Temperature Range -65°C to +150°C
 Thermal Resistance Junction to Ambient, All Series 20°C/W
 Junction to Case, 678, 682 Series 1.5°C/W
 Junction to Case, 695, 696 Series 3.0°C/W

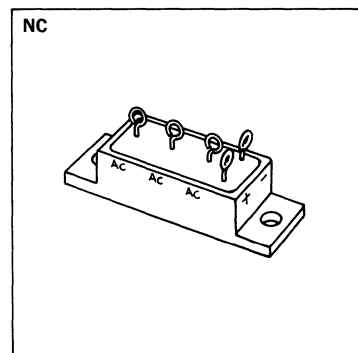
8

MECHANICAL SPECIFICATIONS

678, 682, 695, 696 SERIES

	ins.	mm.
A	.820 MAX.	20.83 MAX.
B	.09 DIA. TYP.	2.29 DIA. TYP.
C	.164-.174 DIA.	4.17-4.42 DIA.
D	.365-.385	9.27-9.78
E	1.870-1.880	47.50-47.75
F	.740-.760	18.80-19.30
G	.370-.390	9.40-9.91
H	.040 TYP	1.02 TYP
J	.486-.506	12.34-12.85
K	.115-.135	2.92-3.43
L	2.240-2.260	56.90-57.40

Typical Weight — 30 grams



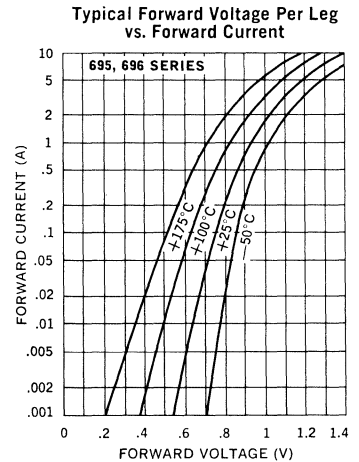
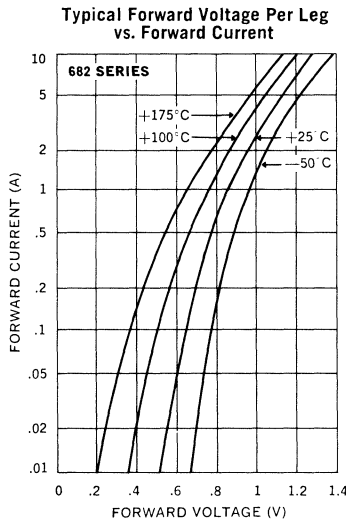
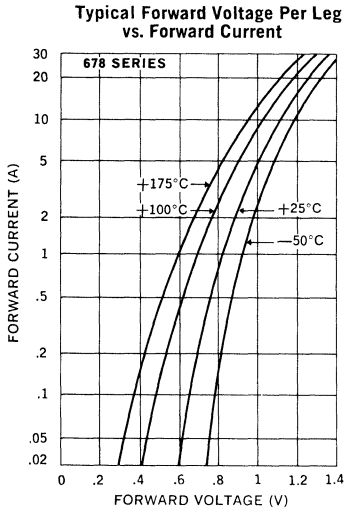
MARKING

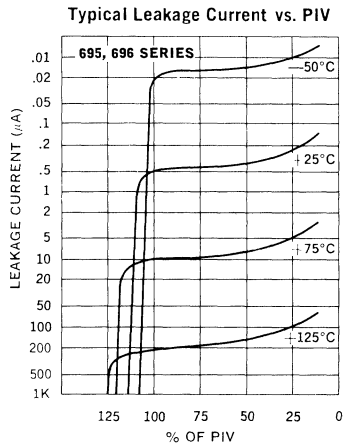
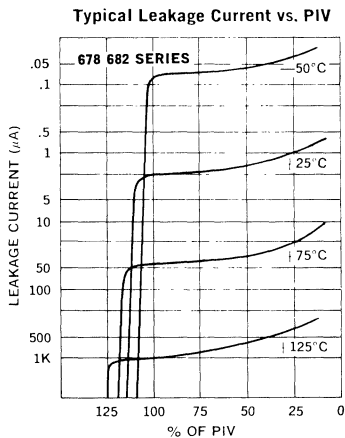
Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

Part number is printed on the body.

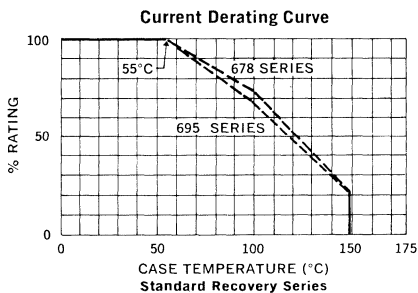
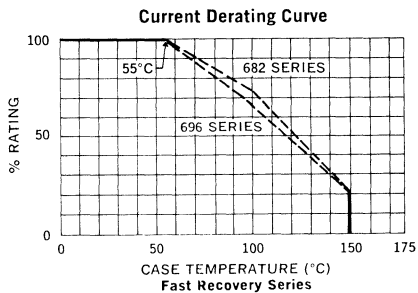
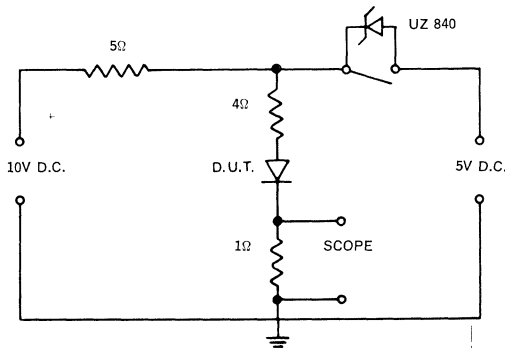
Electrical Specifications (at 25°C unless noted)						Maximum Ratings			
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Maximum Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time*	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms)	
			T _A = 25°C	T _A = 100°C		T _C = 55°C	T _C = 100°C		
			μA	μA		Amps	Amps		Amps
Standard Recovery	678-1 678-2 678-3 678-4 678-5 678-6	100 200 300 400 500 600	1.2V @ 10A	10	200	—	25	18.5	150
Standard Recovery	695-1 695-2 695-3 695-4 695-5 695-6	100 200 300 400 500 600	1.2V @ 2A	5	150	—	15	9	80
Fast Recovery	682-1 682-2 682-3 682-4 682-5 682-6	100 200 300 400 500 600	1.2V @ 6A	10	200	500	20	14	150
Fast Recovery	696-1 696-2 696-3 696-4 696-5 696-6	100 200 300 400 500 600	1.2V @ 2A	5	150	500	15	9	60

*Measured in a reverse recovery circuit switching from 1.0A forward to 1.0A reverse current recovering to 0.5A.





Reverse Recovery Circuit



RECTIFIER ASSEMBLIES

Single Phase Bridges, 10-25 Amp, Standard and Fast Recovery Magnum™

679, 680, 683, 684 SERIES

FEATURES

- Current Ratings: to 25A
- Recovery Time: to 500ns
- PIVs: from 100 to 600V
- Surge Ratings: to 150A
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

This series of single phase MAGNUM™ bridge offers the designer the ultimate in high current power supply applications. The fast recovery series allows operation at full power at high frequencies, up to 40kHz square wave, which is often used in chopper, inverters and converters in aircraft, missiles, etc., equipment.

ABSOLUTE MAXIMUM RATINGS

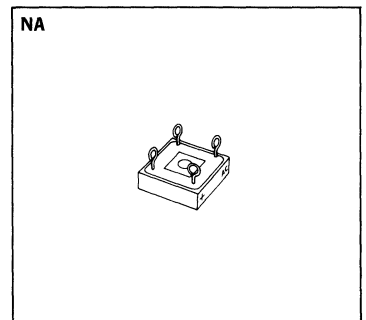
Peak Inverse Voltage	100 to 600V
Maximum Average D.C. Output Current	See Electrical Specifications
Non-Repetitive Sinusoidal Surge (8.3ms)	See Electrical Specifications
Operating and Storage Temperature Range	-65°C to +150°C
Thermal Resistance Junction to Ambient, 679, 683 Series	20°C/W
Junction to Ambient, 680, 684 Series	25°C/W
Junction to Case, 679, 683 Series	2.0°C/W
Junction to Case, 680, 684 Series	4.0°C/W

MECHANICAL SPECIFICATIONS

680, 684 SERIES

	ins.	mm.
A	.240 MAX.	6.10 MAX.
B	.57 MAX.	14.45 MAX.
C	.040 TYP.	1.02 TYP.
D	.750 MAX.	19.05 MAX.
E	.750 MAX.	19.05 MAX.
F	.140 DIA.	3.56 DIA.
G	.09 DIA. TYP.	2.29 DIA. TYP.

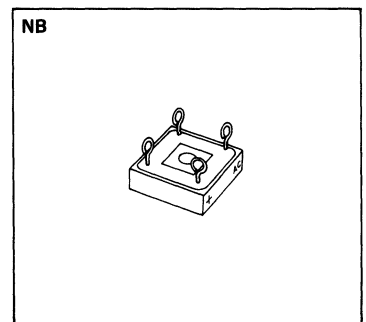
Typical Weight — 0.35 ounces
10 grams



679, 683 SERIES

	ins.	mm.
A	.328 MAX.	8.33 MAX.
B	.750 MAX.	19.05 MAX.
C	.040 TYP.	1.02 TYP.
D	1.125 MAX.	28.58 MAX.
E	.562	14.27
F	1.125 MAX.	28.58 MAX.
G	.193	4.90
H	.562	14.27
J	.500	12.70
K	.09 DIA. TYP.	2.29 DIA. TYP.
L	.062	1.57
M	.062	1.57

Typical Weight — 0.7 ounces
20 grams



MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

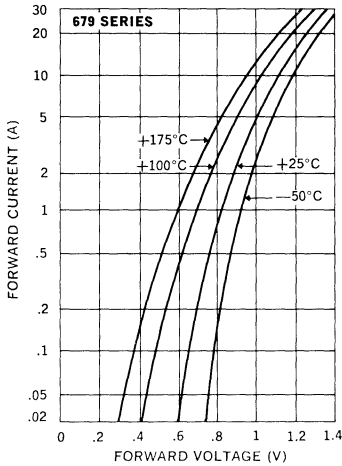
Part number is printed on the body.

Electrical Specifications (at 25°C unless noted)						Maximum Ratings			
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Maximum Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time*	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms)	
			T _A = 25°C	T _A = 100°C		T _C = 55°C	T _C = 100°C		
			Volts	μA		μA	ns	Amps	Amps
Standard Recovery	679-1	100	1.2V @ 10A	10	200	—	25	18.5	150
	679-2	200							
	679-3	300							
	679-4	400							
	679-5	500							
	679-6	600							
Standard Recovery	680-1	100	1.2V @ 2A	2	50	—	10	6	50
	680-2	200							
	680-3	300							
	680-4	400							
	680-5	500							
	680-6	600							
Fast Recovery	683-1	100	1.2V @ 6A	10	200	500	20	14	150
	683-2	200							
	683-3	300							
	683-4	400							
	683-5	500							
	683-6	600							
Fast Recovery	684-1	100	1.2V @ 2A	5	100	500	10	6	50
	684-2	200							
	684-3	300							
	684-4	400							
	684-5	500							
	684-6	600							

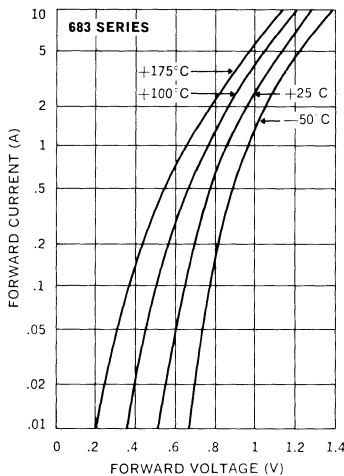
*Measured in a reverse recovery circuit switching from 1.0A forward to 1.0A reverse current recovering to 0.5A.

8

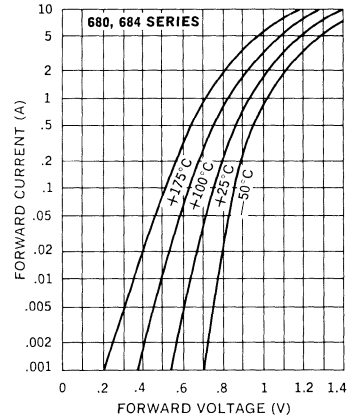
Typical Forward Voltage Per Leg vs. Forward Current



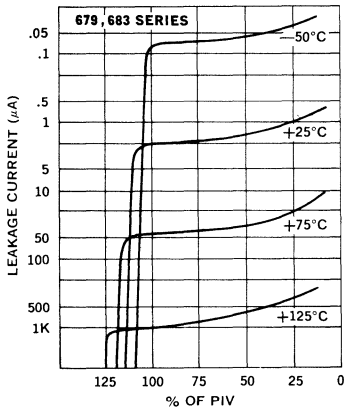
Typical Forward Voltage Per Leg vs. Forward Current



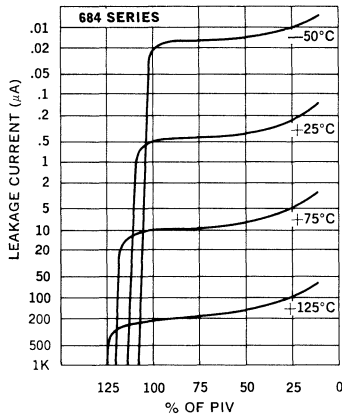
Typical Forward Voltage Per Leg vs. Forward Current



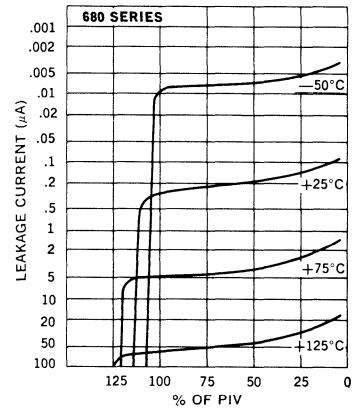
Typical Leakage Current vs. PIV



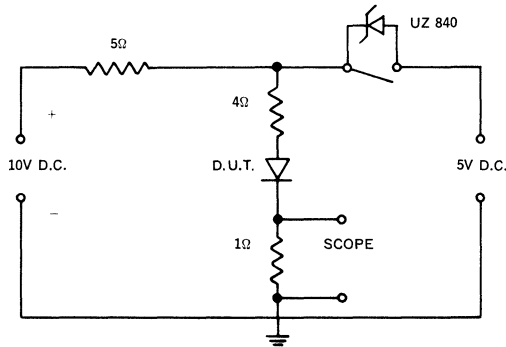
Typical Leakage Current vs. PIV



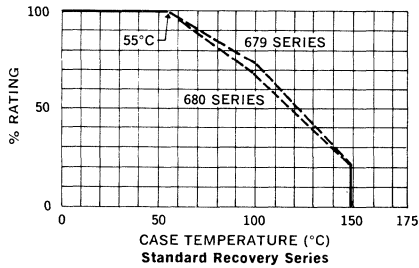
Typical Leakage Current vs. PIV



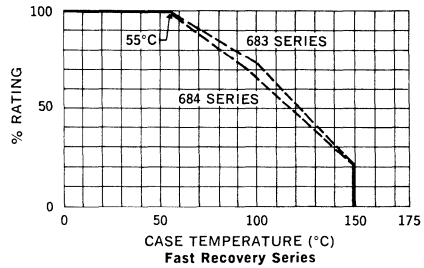
Reverse Recovery Circuit



Current Derating Curve



Current Derating Curve



RECTIFIER ASSEMBLIES

681, 689 SERIES

Doubler and Center Tap, 15 Amp,
Standard and Fast Recovery, Magnum®

FEATURES

- Current Ratings: to 15A
- Aluminum Heat Sink Case, Electrically Insulated
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- PIV: 100 to 600V
- Surge Ratings: to 150A

DESCRIPTION

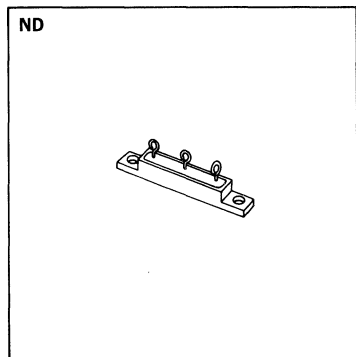
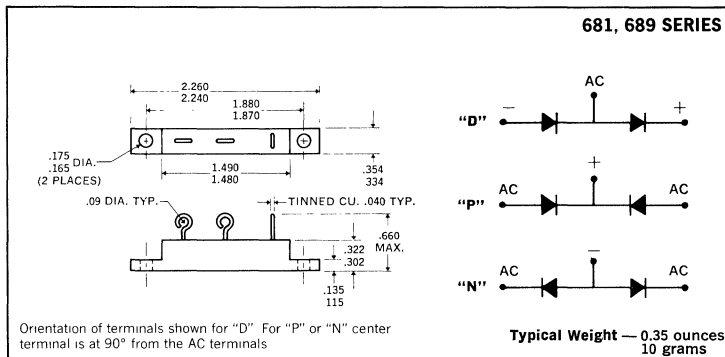
This series of MAGNUM® doublers and center tap rectifiers offers high current and high thermal conductivity needed in high current power supply applications. The MAGNUM® package is virtually indestructible and lends its use to high environmental stresses, as seen in aircraft, missile and satellite equipment.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltages	100 to 600V
Maximum Average D.C. Output Current	
@ $T_C = +55^\circ\text{C}$	15A
@ $T_C = +100^\circ\text{C}$	10A
Non-Repetitive Sinusoidal Surge (8.3ms)	
@ $T_A = +100^\circ\text{C}$	150A
Operating and Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Thermal Resistance	
Junction to Ambient	20°C/W
Junction to Case	6.0°C/W

8

MECHANICAL SPECIFICATIONS



MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

Part number is printed on the body.

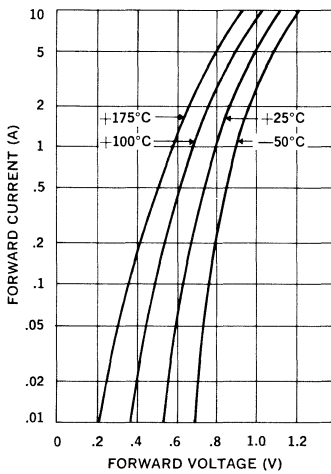
† Add suffix P, N, or D for terminal configuration P, N, or D. For example, for center tap configuration, P, order 681-IP.

Electrical Specifications (at 25°C unless noted)

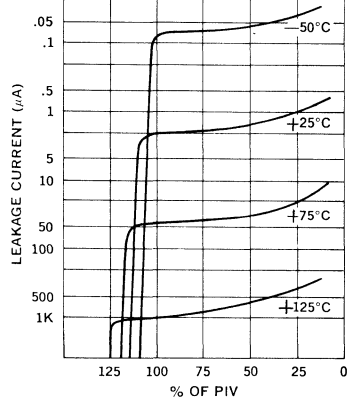
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Maximum Reverse Recovery Time*	Maximum Leakage Current Per Leg @ PIV	
				T _A = 25°C	T _A = 100°C
				Volts	μA
Standard Recovery	681-1	100	1.2V @ 10A	10	200
	681-2	200			
	681-3	300			
	681-4	400			
	681-5	500			
	681-6	600			
Fast Recovery	689-1	100	1.2V @ 10A	500	10
	689-2	200			
	689-3	300			
	689-4	400			
	689-5	500			
	689-6	600			

*Measured in a reverse recovery circuit from 1A forward to 1A reverse current recovery to 0.5A.

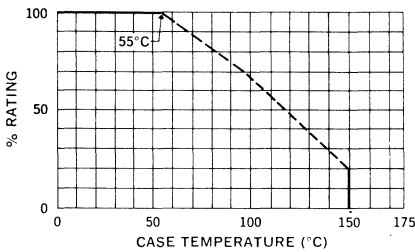
Typical Forward Voltage Per Leg vs. Forward Current



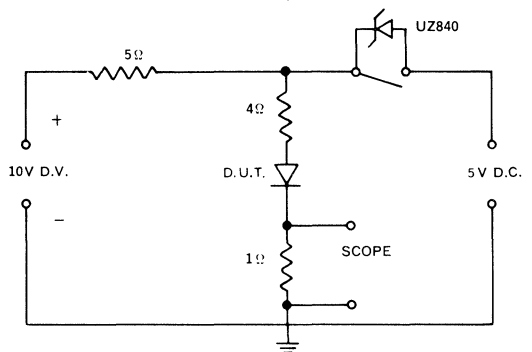
Typical Leakage Current vs. PIV



Current Derating Curve



Reverse-Recovery Circuit



RECTIFIER ASSEMBLIES

697, 698 SERIES

Single Phase Bridges, 7.5 Amp, Standard and Fast Recovery

FEATURES

- Miniature High Current Assemblies
- Continuous Ratings: to 7.5A
- Surge Ratings: to 80A
- PIV's: from 100V to 600V
- Recovery Times: to 500ns
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics

DESCRIPTION

These miniature molded high-current single-phase bridges are designed for universal application in power supplies. One basic bridge fills current requirements up to 7.5A, with PIV's from 100 to 600 volts and recovery times of standard, and 500ns max.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	100 to 600V
Maximum Average D.C. Output Current	See Electrical Specifications
Non-Repetitive Sinusoidal Surge (8.3ms)	See Electrical Specifications
Operating and Storage Temperature Range	-65°C to +150°C
Thermal Resistance Junction to Ambient	32°C/W
Junction to Case	10°C/W

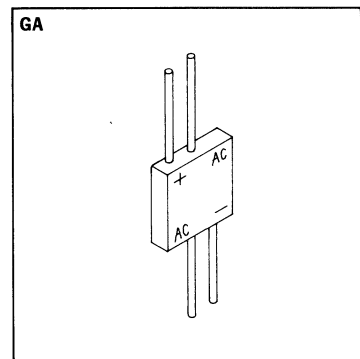
8

MECHANICAL SPECIFICATIONS

697, 698 SERIES

	ins.	mm.
A	0.50±.01	12.70±.25
B	.032 DIA.	0.81 DIA.
C	1.0 MIN.	25.4 MIN.
D	.250 MAX.	6.35 MAX.
E	.150 TYP.	3.81 TYP.
F	0.50±.01	12.70±.25

Typical Weight — 0.14 ounces
4.0 grams



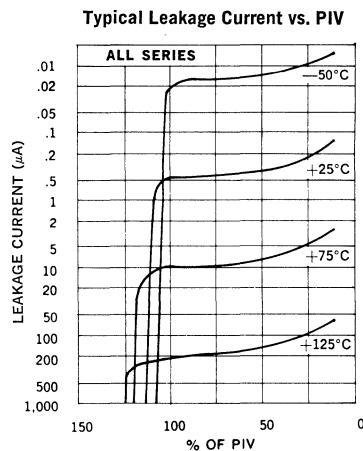
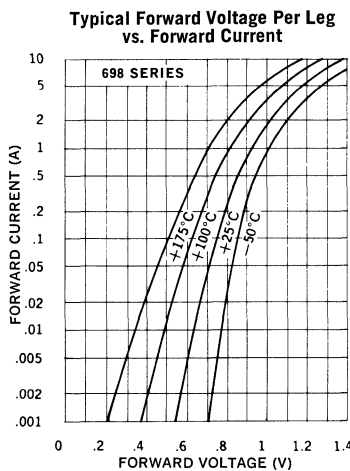
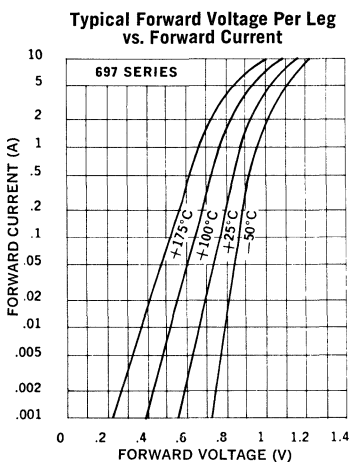
MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

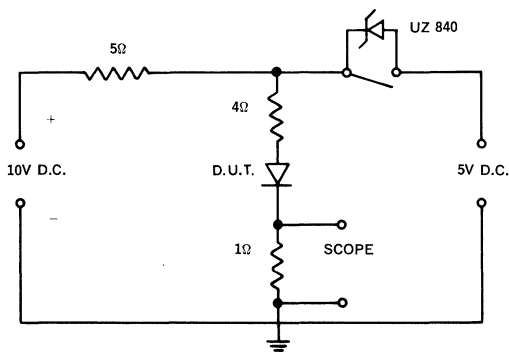
Part number is printed on the body.

Electrical Specifications (at 25°C unless noted)						Maximum Ratings		
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time†	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms)
			T _A = 25°C	T _A = 100°C		T _A = 25°C	T _C = 55°C	
	Volts		µA	µA	ns	Amps	Amps	Amps
Standard Recovery	697-1	100	1.0V @ 2A	5	200	2.5	7.5	80
	697-2	200						
	697-3	300						
	697-4	400						
	697-5	500						
	697-6	600						
Fast Recovery	698-1	100	1.1V @ 2A	5	200	500	2.25	7.0
	698-2	200						
	698-3	300						
	698-4	400						
	698-5	500						
	698-6	600						

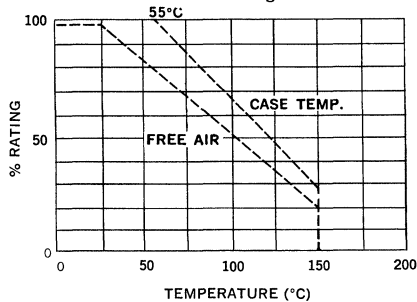
†Measured in a reverse recovery circuit switching from 1A forward to 1A reverse current recovering to .5A.



Reverse Recovery Circuit



Current Derating Curve



RECTIFIER ASSEMBLIES

700, 701 SERIES

Three Phase Bridges, 2.5 Amp, Standard and Fast Recovery

FEATURES

- Miniature Package
- Recovery Time: to 500ns
- Surge Ratings: to 25A
- PIV: from 100 to 600V
- Controlled Avalanche Characteristics
- Only Fused-in-Glass Diodes Used

DESCRIPTION

These miniature transfer-molded high-voltage three-phase power bridges are designed for universal application in power supplies. One basic bridge fills current requirements up to 2.5A, with PIV's from 100 to 600 volts and recovery times of standard and 500ns.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage 100 to 600V
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-Repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications
 Operating and Storage Temperature Range -65°C to +150°C
 Thermal Resistance Junction-to-Ambient 25°C/W

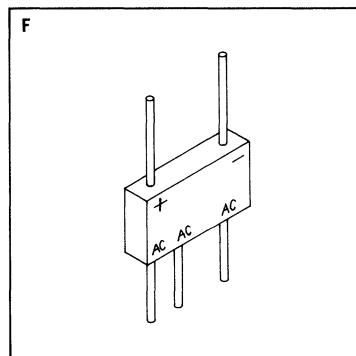
8

MECHANICAL SPECIFICATIONS

700, 701 SERIES

	ins.	mm.
A	.310	7.87
B	.621	15.77
C	.512 REF.	13.0 REF.
D	.460 MAX.	11.68 MAX.
E	.255	6.48
F	1.030 MAX.	26.16 MAX.
G	.220 MAX.	5.59 MAX.
H	.875	22.23
J	.028 DIA.	0.71 DIA.

Typical Weight — 0.12 ounces
3.5 grams



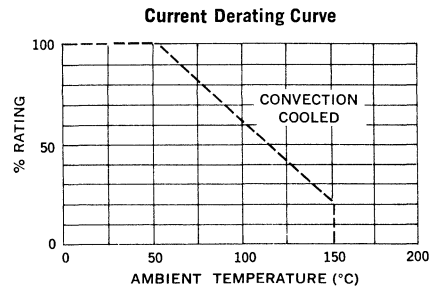
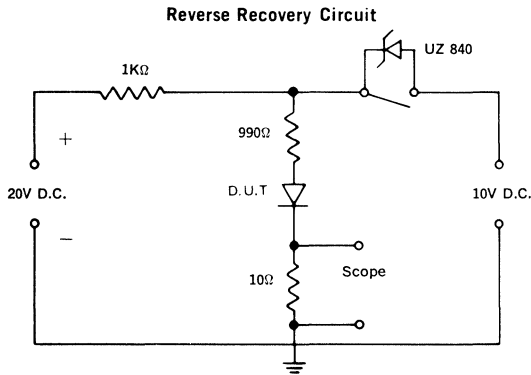
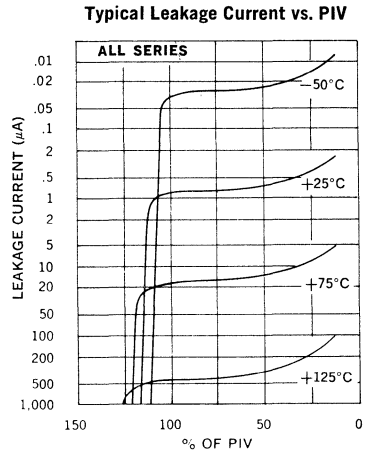
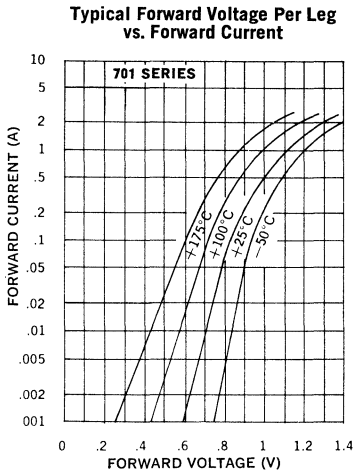
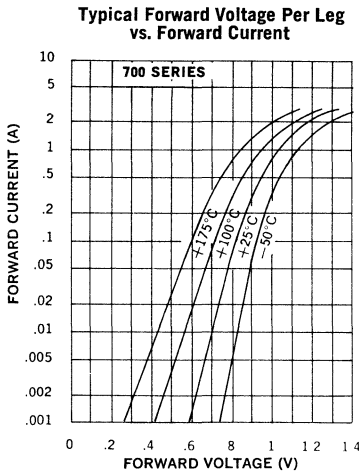
MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

Part number is printed on the body.

Electrical Specifications (at 25°C unless noted)						Maximum Ratings	
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time†	Maximum Average D.C. Output Current	Non-Repetitive Sinusoidal Surge (8.3ms)
			T _A = 25°C	T _A = 100°C		T _A = 55°C	
			µA	µA		ns	Amps
Standard Recovery	700-1	100	1.0V @ 0.5A	2	100	2.5	25
	700-2	200					
	700-3	300					
	700-4	400					
	700-5	500					
	700-6	600					
Fast Recovery	701-1	100	1.1V @ 0.5A	2	100	2.25	20
	701-2	200					
	701-3	300					
	701-4	400					
	701-5	500					
	701-6	600					

†Measured in a reverse recovery circuit switching from 10mA forward to 10mA reverse current recovering to 5mA.



RECTIFIER ASSEMBLIES

Three Phase Bridges, 20-40 Amp,
High Efficiency, ESP

800, 801 SERIES

FEATURES

- Current Ratings: to 40A
- Recovery Time: 50ns
- Surge Ratings: to 250A
- PIVs: from 50 to 150V
- Only Fused-in-Glass Diodes Used
- Exceptionally High Efficiency
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

This series of three phase bridges offers the highest efficiency possible for applications where nothing else will do. The series allows operation at full power at high frequencies.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltages 50 to 150V
 Maximum Average D.C. Output Current See Electrical Specifications
 Non-Repetitive Sinusoidal Surge (8.3ms) See Electrical Specifications
 Operating and Storage Temperature Range -65°C to +150°C
 Thermal Resistance Junction to Ambient, All Series 20°C/W
 Junction to Case, 800 Series 1.5°C/W
 Junction to Case, 801 Series 3.0°C/W

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MECHANICAL SPECIFICATIONS

800, 801 SERIES

	ins.	mm.
A	.740-.760	18.80-19.30
B	2.240-2.260	56.90-57.40
C	.365-.385	9.27-9.78
D	.164-.174 DIA.	4.17-4.42 DIA.
E	.370-.390	9.40-9.91
F	.486-.506	12.34-12.85
G	.115-.135	2.92-3.43
H	1.870-1.880	47.50-47.75
J	.820 MAX.	20.83 MAX.

Typical Weight — 1.0 ounce
30 grams

MARKING

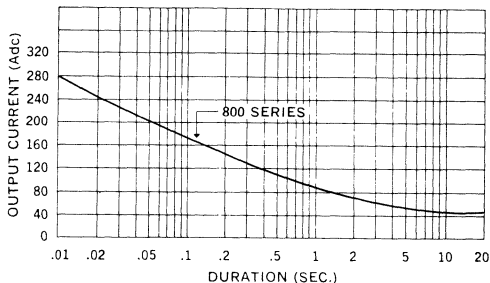
Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

Part number is printed on the body.

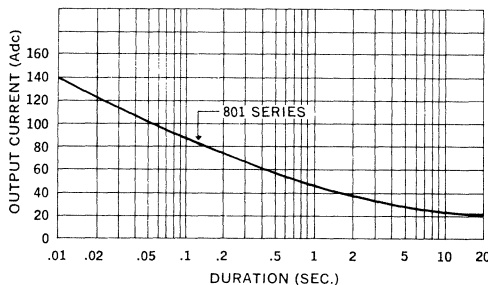
Electrical Specifications (at 25°C unless noted)						Maximum Ratings			
Type	PIV Per Leg	Maximum Forward Voltage Drop Per Leg	Maximum Reverse Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time*	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms)	
			T _A = 25°C	T _A = 100°C		T _C = 55°C	T _C = 100°C		
			μA	μA		Amps	Amps		Amps
ESP Recovery	800-1	50	.95V @ 10A	20	1000	50	40	25	250
	800-2	100							
	800-3	125							
	800-4	150							
ESP Recovery	801-1	50	.95V @ 6A	10	300	50	20	16	125
	801-2	100							
	801-3	125							
	801-4	150							

*Measured in a reverse recovery circuit switching from 1A forward to 1A reverse current recovering to 0.5A.

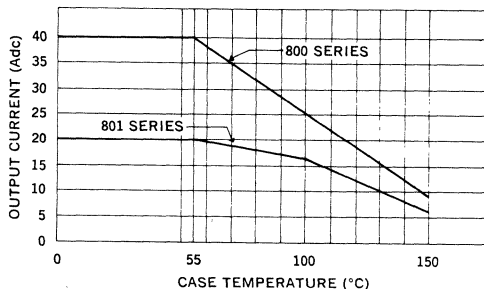
Forward Surge Current vs. Duration

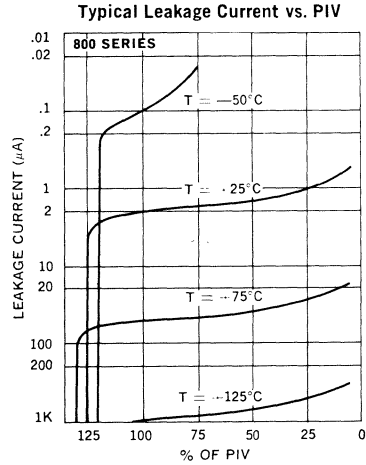
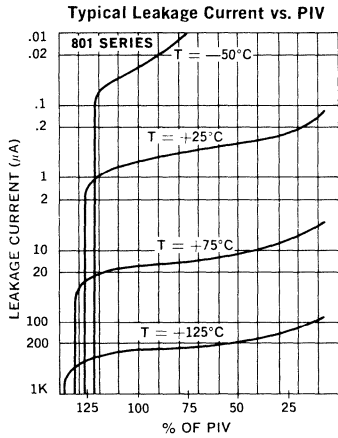
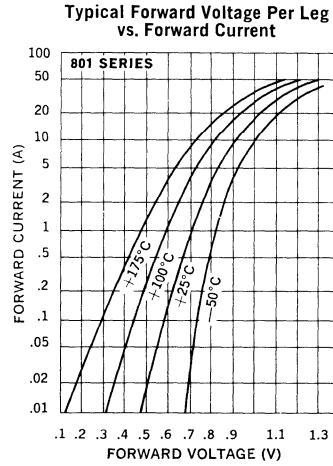
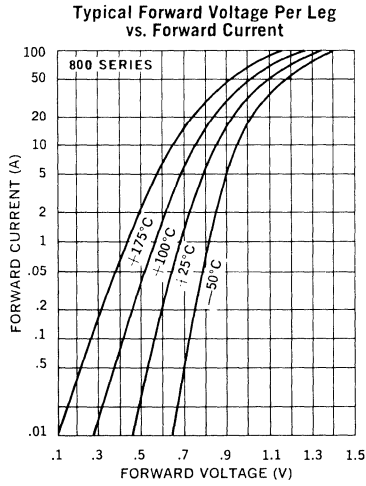


Forward Surge Current vs. Duration



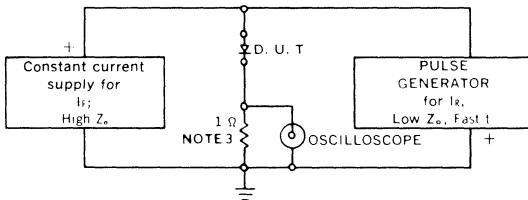
Current Derating Curve





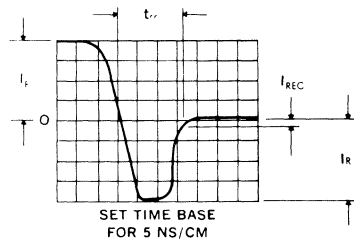
8

Reverse-Recovery Circuit



- NOTES:**
1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω .
 2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω .
 3. Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform



RECTIFIER ASSEMBLIES

802, 803 SERIES

Single Phase Bridges, 20-35 Amp, High Efficiency ESP Series

FEATURES

- Current Ratings: to 35A
- Recovery Time: 50ns
- Surge Ratings: to 250A
- PIVs: from 50 to 150V
- Only Fused-in-Glass Diodes Used
- Exceptional High Efficiency
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

This series of single phase bridges offer the highest efficiency possible for applications where nothing else will do. The series allow operation at full power at very high frequency.

ABSOLUTE MAXIMUM RATINGS

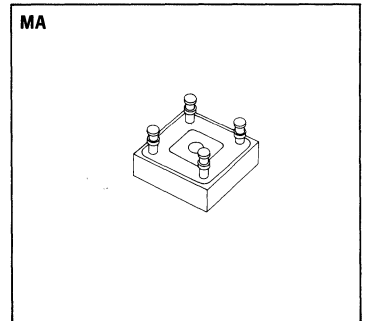
Peak Inverse Voltage	50 to 150V
Maximum Average D.C. Output Current	See Electrical Specifications
Non-Repetitive Sinusoidal Surge (8.3ms)	See Electrical Specifications
Operating and Storage Temperature Range	-65°C to +150°C
Thermal Resistance Junction to Ambient, 802 Series	20°C/W
803 Series	25°C/W
Junction to Case, 802 Series	2.0°C/W
803 Series	4.0°C/W

MECHANICAL SPECIFICATIONS

803 SERIES

	ins.	mm.
A	.735-.755	18.67-19.18
B	.570 MAX.	14.48 MAX.
C	.226-.246	5.74-6.25
D	.735-.755	18.67-19.18
E	.130-.150 DIA.	3.30-3.81

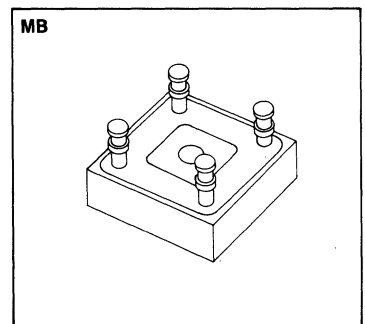
Typical Weight — 0.35 ounces
10 grams



802 SERIES

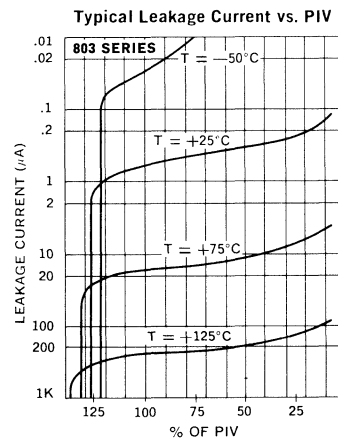
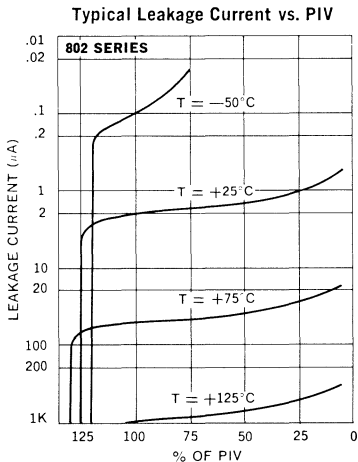
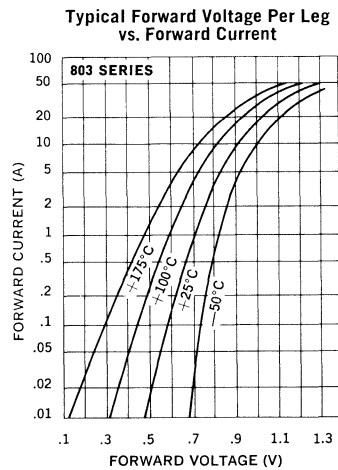
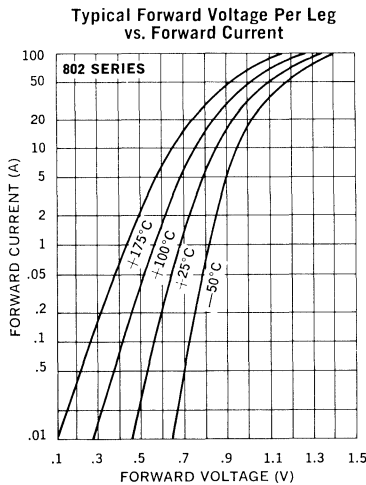
	ins.	mm.
A	.056-.066	1.42-1.68
B	.052-.072	1.32-1.83
C	1.115-1.135	28.32-28.83
D	.552-.572	14.02-14.53
E	.552-.572	14.02-14.53
F	.180-.200 DIA.	4.57-5.08 DIA.
G	.490-.510	12.45-12.95
H	.750 MAX.	19.05 MAX.
J	.302-.322	7.67-8.18
K	1.115-1.135	28.32-28.83

Typical Weight — 0.70 ounces
20 grams



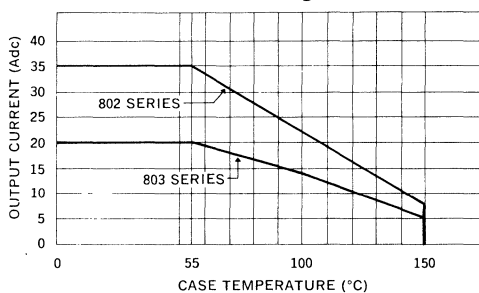
Electrical Specifications (at 25°C unless noted)						Maximum Ratings			
Type	PIV Per Leg Volts	Maximum Forward Voltage Drop Per Leg	Maximum Reverse Leakage Current Per Leg @ PIV		Maximum Reverse Recovery Time*	Maximum Average D.C. Output Current		Non-Repetitive Sinusoidal Surge (8.3ms) I _A = 100°C	
			T _A = 25°C μA	T _A = 100°C μA		T _C = 55°C Amps	T _C = 100°C Amps		
ESP Recovery	802-1	50	.95V @ 10A	20	1000	50	35	22.5	250
	802-2	100							
	802-3	125							
	802-4	150							
ESP Recovery	803-1	50	.95V @ 6A	10	300	50	20	16	125
	803-2	100							
	803-3	125							
	803-4	150							

*Measured in a reverse recovery circuit switching from 1A forward to 1A reverse current recovering to 0.5A.

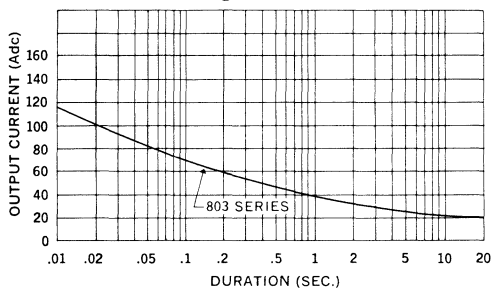


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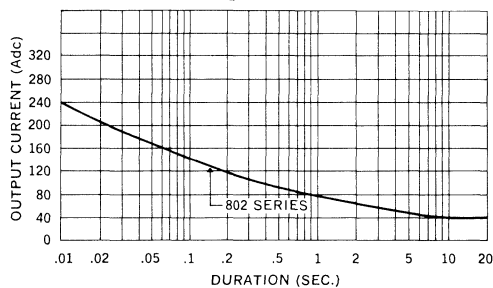
Current Derating Curve



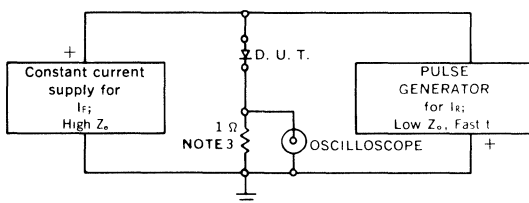
Forward Surge Current vs. Duration



Forward Surge Current vs. Duration



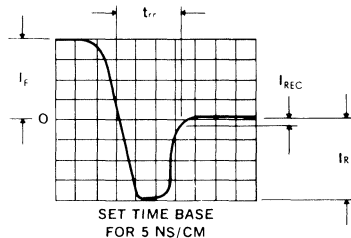
Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time \leq 3ns; input impedance = 50 Ω .
2. Pulse Generator: Rise time \leq 8ns; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform



RECTIFIER ASSEMBLIES

804 SERIES

Doublers and Center Tap, 20 Amp,
High Efficiency, ESP

FEATURES

- Current Rating: to 20A
- Aluminum Heat Sink Case, Electrically Insulated
- Recovery Time: 50ns
- Surge Rating: to 250A
- PIVs: from 50 to 150V
- Only Fused-in-Glass Diodes Used
- Exceptional High Efficiency

DESCRIPTION

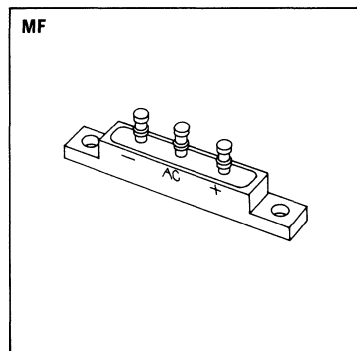
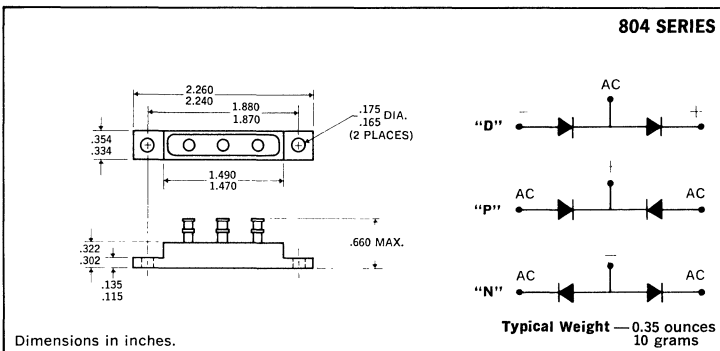
This series of doublers and center tap rectifiers offer the ultimate in high efficiency application. The rectifiers are particularly suited to switching regulator supplies where very fast recovery time and low forward drop are of prime importance.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	50 to 150V
Maximum Average D.C. Output Current	
@ $T_C = +55^\circ\text{C}$	20A
@ $T_C = +100^\circ\text{C}$	14A
Non-Repetitive Sinusoidal Surge (8.3ms)	
@ $T_A = +100^\circ\text{C}$	250A
Operating and Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Thermal Resistance Junction to Ambient	20°C/W
Junction to Case	6.0°C/W

8

MECHANICAL SPECIFICATIONS



MARKING

Alternating Current Input	A.C.
Cathode — Positive Output	+
Anode — Negative	-

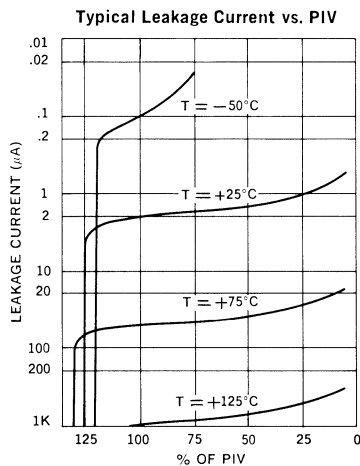
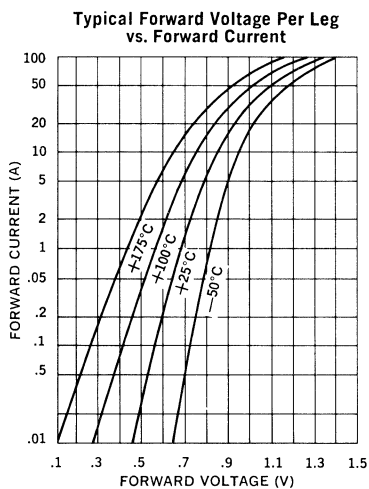
Part number is printed on the body.

† Add suffix P, N, or D for terminal configuration P, N, or D.
For example, for center tap configuration, P, order 804-1P

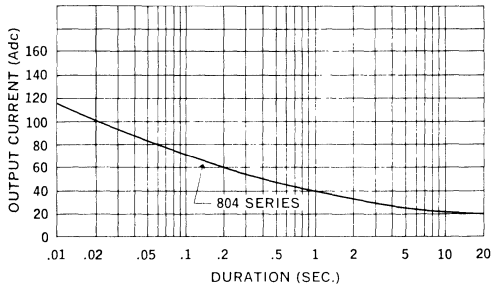
Electrical Specifications (at 25°C unless noted)

Type	PIV Per Leg Volts	Maximum Forward Voltage Drop Per Leg	Maximum Leakage Current (μA) Per Leg @ PIV		Maximum Reverse Recovery Time*
			$T_A = 25^\circ C$	$T_A = 100^\circ C$	
			μA	μA	
ESP 804-1	50	.95V @ 10A	10	500	50
Recovery 804-2	100				
804-3	125				
804-4	150				

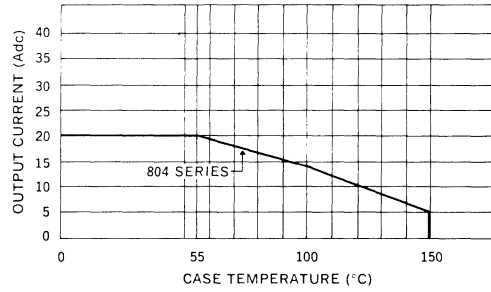
*Measured in a reverse recovery circuit switching from 1A forward to 1A reverse current recovering to 0.5A.



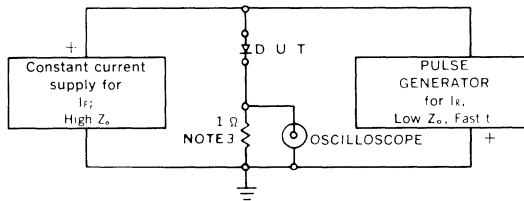
Forward Surge Current vs. Duration



Current Derating Curve



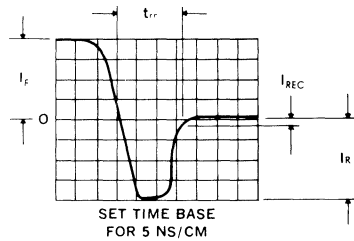
Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time ≤ 3 ns; input impedance = 50Ω .
2. Pulse Generator: Rise time ≤ 8 ns; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

Characteristic Waveform



RECTIFIERS

SES5401C-SES5404C

High Efficiency, 16A Center-Tap

FEATURES

- Low Forward Voltage
- Fast Recovery Times
- Economical, Convenient TO-220AB Package
- Low Thermal Resistance
- Mechanically Rugged

DESCRIPTION

The SES5401C Series in the economical, convenient TO-220AB package, is specifically designed for operation in power switching circuits to frequencies in excess of 100KHz. The series combines two high efficiency devices into one package, simplifying installation, reducing heatsink requirements and the need to purchase matched components.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5401C	50V
Peak Inverse Voltage, SES5402C	100V
Peak Inverse Voltage, SES5403C	150V
Peak Inverse Voltage, SES5404C	200V
Maximum Average D.C. Output Current	
@ $T_C = 125^\circ\text{C}$	16A
@ $T_A = 25^\circ\text{C}$	3A
@ $T_A = 25^\circ\text{C}$ (Note 1)	10A
Non-Repetitive Sinusoidal Surge Current, 8.3mS	70A
Thermal Resistance, Junction to Case, θ_{J-C}	1.75°C/W
Thermal Resistance, Junction to Ambient, θ_{J-A}	60°C/W
Operating and Storage Temperature Range	-55°C to +150°C

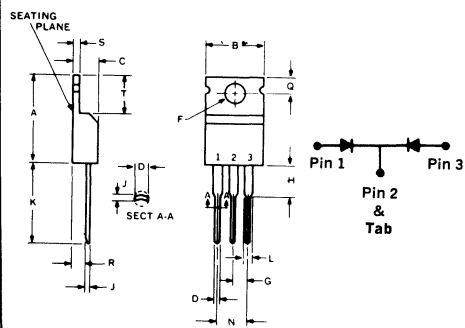
Note 1. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

ELECTRICAL SPECIFICATIONS

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $t_r = 8\text{nS}$
		$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	@ $T_J = 25^\circ\text{C}$	@ $T_J = 100^\circ\text{C}$		
SES5401C	50V			5 μA	150 μA	100nS	1.4V
SES5402C	100V	1.025V @ 8A	0.945V @ 8A				
SES5403C	150V						

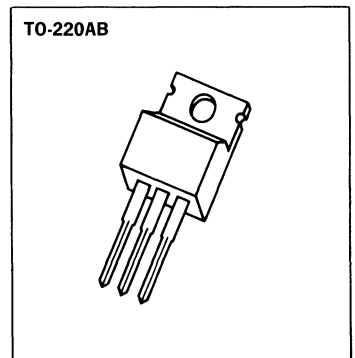
*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{REC} = 0.25\text{A}$

MECHANICAL SPECIFICATIONS

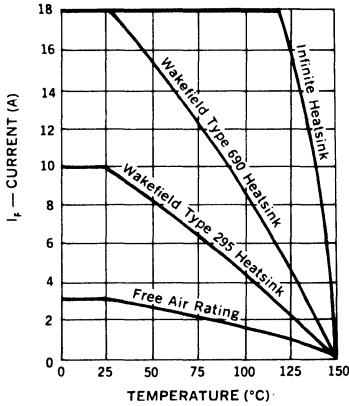


SES5401-SES5404C

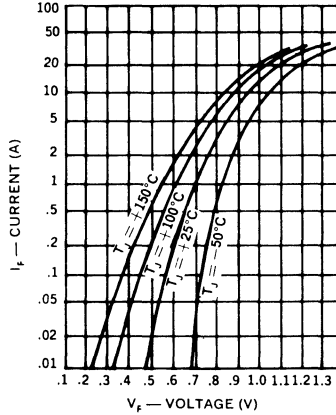
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.42	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.533	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270



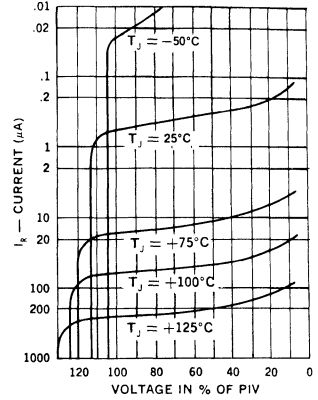
Output Current vs. Temperature



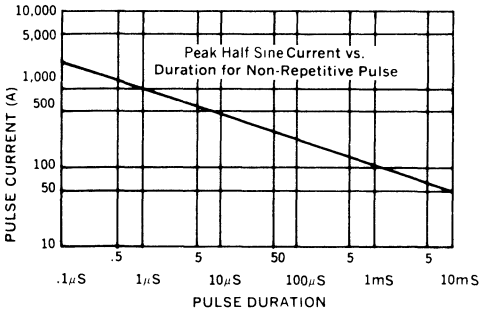
Typical Forward Current vs. Forward Voltage



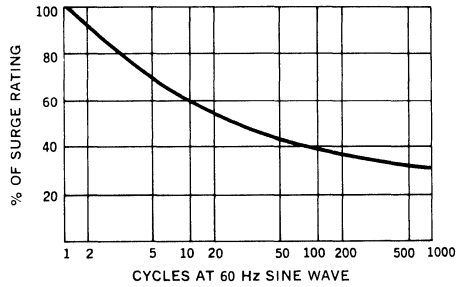
Typical Reverse Current vs. Voltage



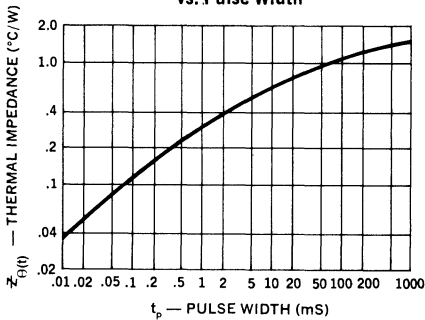
Forward Pulse Current vs. Duration



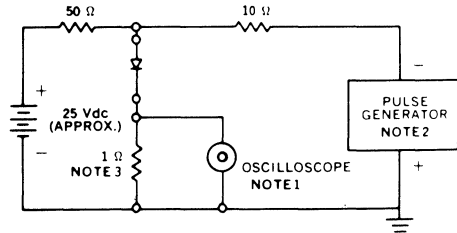
Multiple Surge Current vs. Duration



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50Ω.
2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10Ω.
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 25A Center-Tap

SES5601C
SES5602C
SES5603C

FEATURES

- Low Forward Voltage
- Fast Switching Speed
- Convenient Package
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged TO-3 Package
- Available as Positive or Negative Center-Tap

DESCRIPTION

The SES, super-fast recovery, rectifiers are specifically designed for operation in power switching circuits. Their super-fast recovery time and very low forward voltage make them particularly efficient in most switching applications.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, SES5601C	50V
Peak Inverse Voltage, SES5602C	100V
Peak Inverse Voltage, SES5603C	150V
Maximum Average D.C. Output Current at $T_C = 100^\circ\text{C}$	25A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	400A
Thermal Resistance, Junction to Case	1°C/W
Operating and Storage Temperature Range	-55°C to $+175^\circ\text{C}$

ELECTRICAL SPECIFICATIONS PER DIODE

Type	PIV	Maximum Forward Voltage (V_F) @		Maximum Reverse Current (I_R) @ PIV		Maximum Reverse Recovery Time*
		$T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$	@ $T_C = 25^\circ\text{C}$	@ $T_C = 125^\circ\text{C}$	
SES5601C SES5602C SES5603C	50V 100V 150V	0.990V @ 12.5A $t_p = 300\mu\text{S}$	0.830V @ 12.5A $t_p = 300\mu\text{S}$	20 μA	4mA	100nS

*Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{\text{REC}} = 0.25\text{A}$

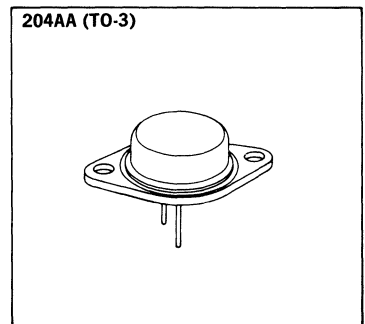
MECHANICAL SPECIFICATIONS

POSITIVE OUTPUT

CASE

SES5601C-SES5603C

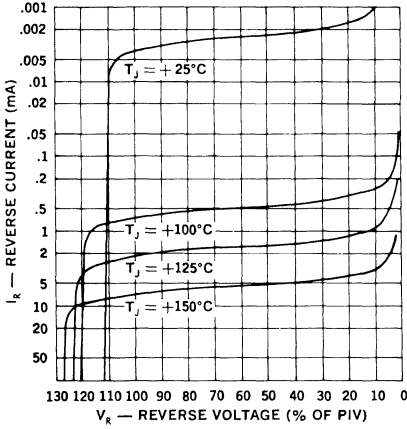
	ins.	mm
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.00-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.



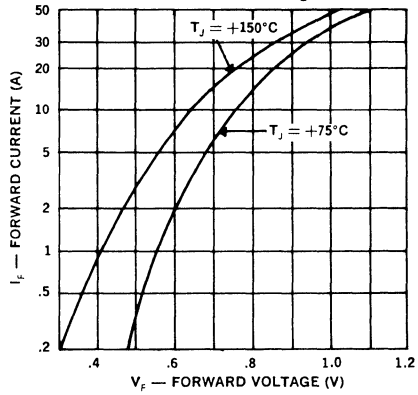
NOTES:

- Standard polarity is positive output.
For reverse polarity (negative output) add suffix "R", ie, SES5601CR.
- All metal surfaces tin plated.

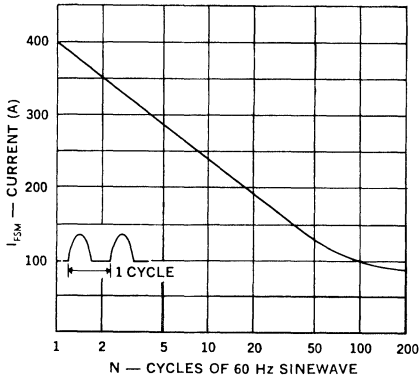
Typical Reverse Current vs. Reverse Voltage



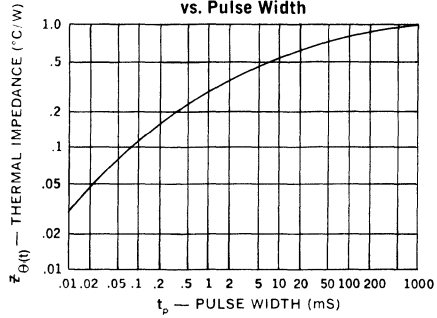
Typical Forward Current vs. Forward Voltage



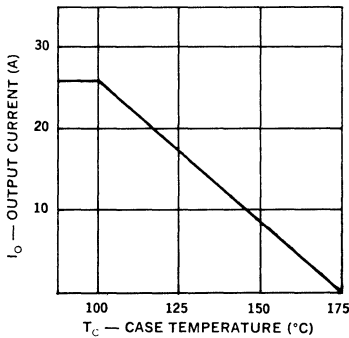
Maximum Forward Surge vs. Number of Cycles



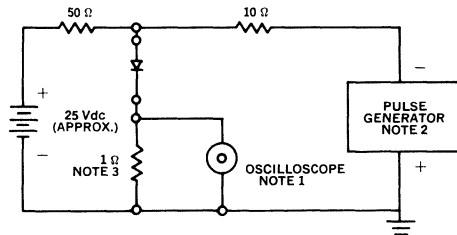
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{nS}$; input impedance = 50Ω .
2. Pulse Generator: Rise time $\leq 8\text{nS}$; source impedance 10Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIER ASSEMBLIES

Single Phase Bridges, 25 Amp,
Military Approved

JAN SPA25
JAN SPB25
JAN SPC25
JAN SPD25

FEATURES

- Qualified to MIL-S-19500/446
- Current Rating: to 25A
- PIV: from 100 to 600V
- Surge Ratings: to 150A
- Only Fused-in-Glass Diodes Used
- Controlled Avalanche Characteristics
- Aluminum Heat Sink Case, Electrically Insulated

DESCRIPTION

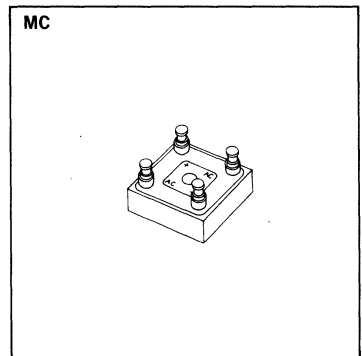
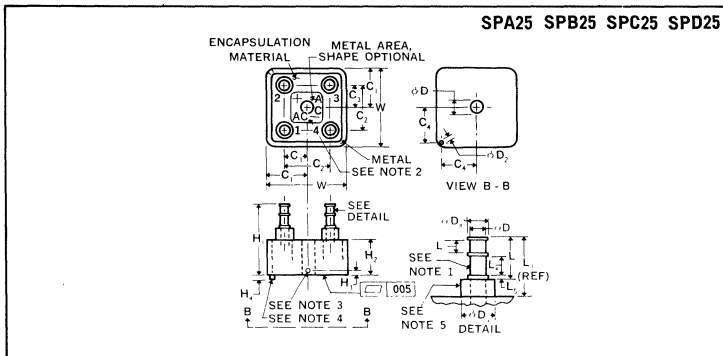
This series of military high-current single-phase bridges offer the utmost in reliability as required in military system designs. This series is assembled with diodes which have been subjected to 100% screening tests.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage	100 to 600V
Maximum Average D.C. Output Current	
@ $T_c = 55^\circ\text{C}$	25A
@ $T_c = 100^\circ\text{C}$	15A
Non-Repetitive Sinusoidal Surge (8.3ms)	
@ $T_c = 55^\circ\text{C}$	150A
Operating and Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Thermal Resistance Junction to Ambient	$20^\circ\text{C}/\text{W}$
Junction to Case	$2.5^\circ\text{C}/\text{W}$

Ltr	Dimensions			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
C ₁	.552	.572	14.02	14.53
C ₂	.624	.760	15.85	19.30
C ₃	.312	.380	7.92	9.65
C ₄	.495	.512	12.57	13.00
ϕD_1	.189	.195	4.80	4.95
ϕD_2	.057	.067	1.45	1.70
ϕD_3	.108	.118	2.74	3.00
ϕD_4	.141	.151	3.58	3.84
ϕD_5	.225	.235	5.72	5.97
H ₁	.669	1.060	17.53	26.92
H ₂	.300	.500	7.62	12.70
H ₃	.040	.060	1.02	1.52
H ₄	.042	.062	1.07	1.57
L ₁	.370	.560	9.40	14.22
L ₂	.307	.365	7.80	9.27
L ₃	.089	.099	2.26	2.49
L ₄	.132	.142	3.35	3.61
L ₅	.026	.036	.66	.91
W	1.104	1.144	28.04	29.06

MECHANICAL SPECIFICATIONS



NOTES:

1. Terminals shall be hot tin dipped or silver plated.
2. Polarity shall be marked on terminal side of device.
3. Point at which T_c is read (must be in metal part of case).
4. Locating pin shall be adjacent to positive terminal.
5. Insulating sleeve shall be alumina (Al_2O_3) or equivalent.

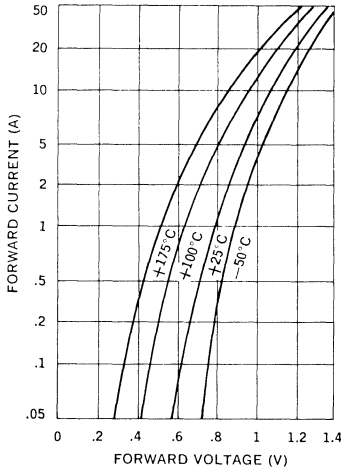
Electrical Specifications (at 25°C unless noted)

Type	PIV Per Leg	Peak Forward Voltage Drop*		Maximum Reverse Recovery Time†	Maximum Leakage Current Per Leg @ PIV	
		Minimum	Maximum		T _C = 25°C	T _C = 100°C
	Volts			μS	μA	μA
JAN SPA25	100	0.9V @ 39A(pk)	1.4V	2	2	150
JAN SPB25	200					
JAN SPC25	400					
JAN SPD25	600					

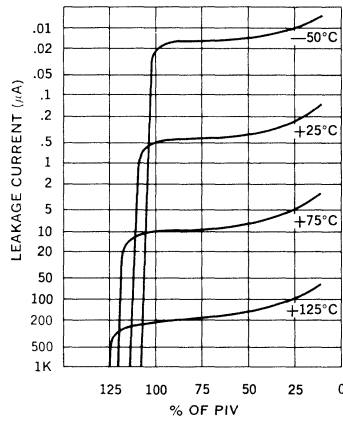
*Peak forward voltage drop is measured at a pulse width of 8.3ms.

†Measured in a reverse recovery circuit switching from 0.5A forward to 1.0A reverse current recovery to 0.5A.

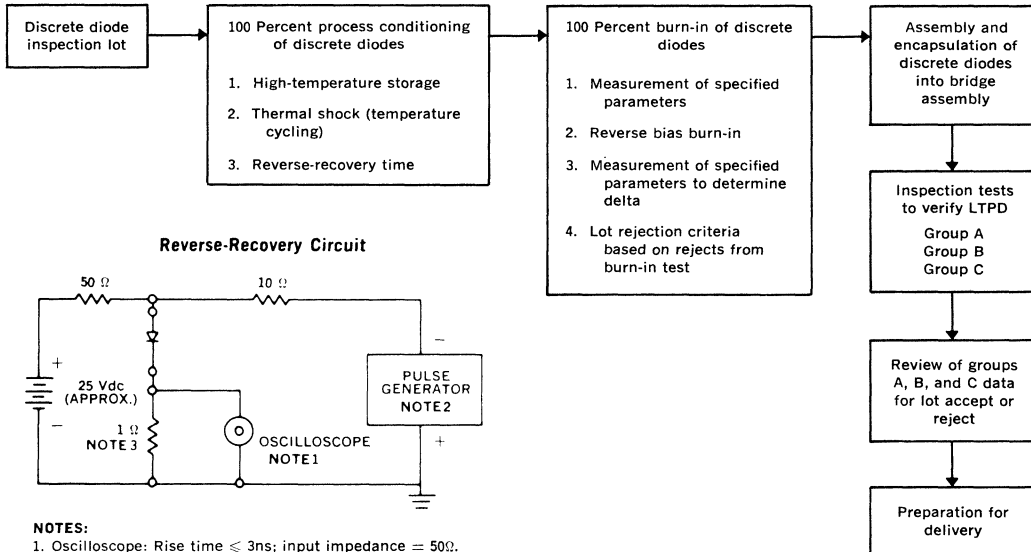
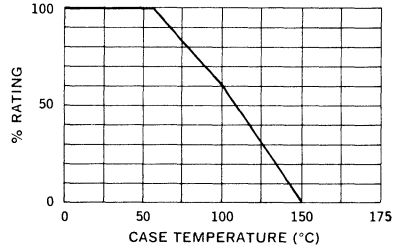
Typical Forward Voltage Per Leg vs. Forward Current



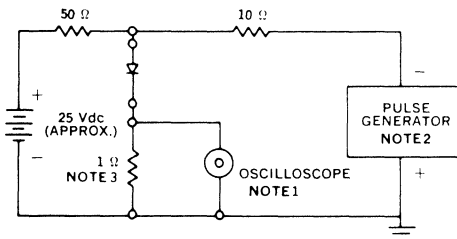
Typical Leakage Current vs. PIV



Current Derating Curve



Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
 - Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
 - Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 16A Center-Tap

UES2401-UES2404

FEATURES

- Very Low Forward Voltage
- Very Fast Recovery Times
- Economical, Convenient TO-220AB Package
- Low Thermal Resistance
- Mechanically Rugged

DESCRIPTION

The UES2401 Series in the economical, convenient TO-220AB package, is specifically designed for operation in power switching circuits to frequencies in excess of 100KHz. The series combines two high efficiency devices into one package, simplifying installation, reducing heatsink requirements and the need to purchase matched components.

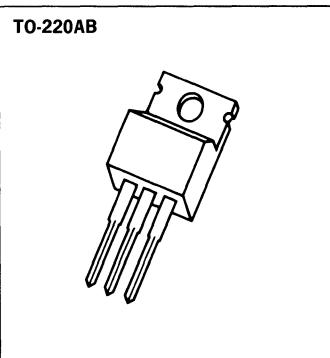
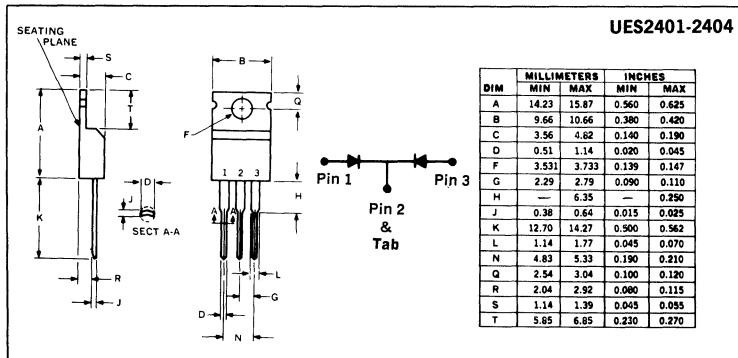
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2401	50V
Peak Inverse Voltage, UES2402	100V
Peak Inverse Voltage, UES2403	150V
Peak Inverse Voltage, UES2404	200V
Maximum Average D.C. Output Current	
@ $T_C = 125^\circ\text{C}$ (Note 1)	16A
@ $T_A = 25^\circ\text{C}$	3A
@ $T_A = 25^\circ\text{C}$ (Note 2)	10A
Non-Repetitive Sinusoidal Surge Current, 8.3ms	80A
Thermal Resistance, Junction to Case, θ_{J-C}	1.75°C/W
Thermal Resistance, Junction to Ambient, θ_{J-A}	60°C/W
Operating and Storage Temperature Range	-55°C to +150°C

Note 1. Above 8A use the tab for electrical connection.

Note 2. Using Wakefield Type 295 heatsink with convection cooling. For more definitive data refer to the Output Current vs. Temperature Curves on this datasheet.

MECHANICAL SPECIFICATIONS

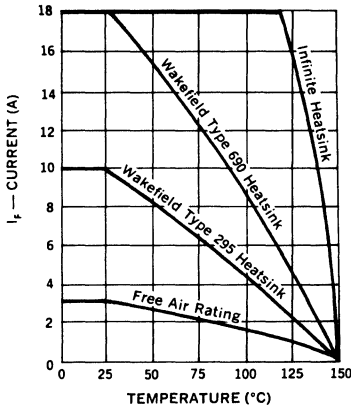


ELECTRICAL SPECIFICATIONS

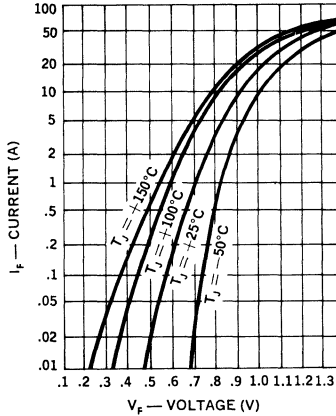
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current @ PIV		Maximum Reverse Recovery Time*	Typical Forward Recovery Voltage @ 1A $T_r = 8nS$
		$T_J = 25^\circ C$	$T_J = 100^\circ C$	$T_J = 25^\circ C$	$T_J = 100^\circ C$		
UES2401	50V	0.9V @ 4A 0.975V @ 8A $t_D = 300\mu S$	0.8V @ 4A 0.895V @ 8A	5 μA	150 μA	35nS	1.4V
UES2402	100V						
UES2403	150V						
UES2404	200V						

*Measured in circuit $I_F = 0.5A$, $I_R = 1.0A$, $I_{REC} = 0.25A$

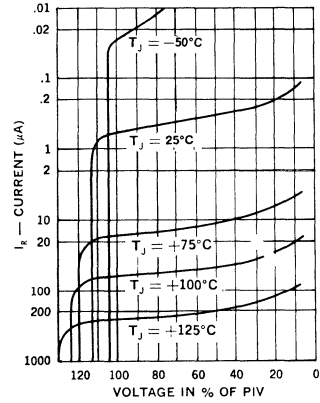
Output Current vs. Temperature



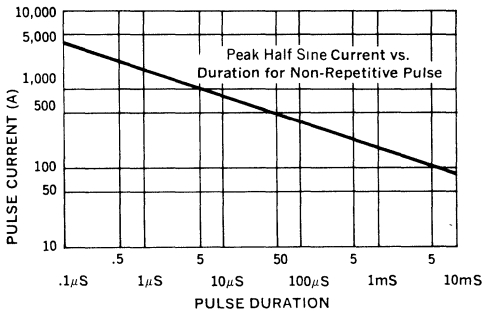
Typical Forward Current vs. Forward Voltage



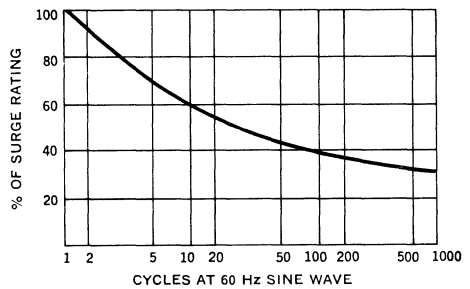
Typical Reverse Current vs. Voltage



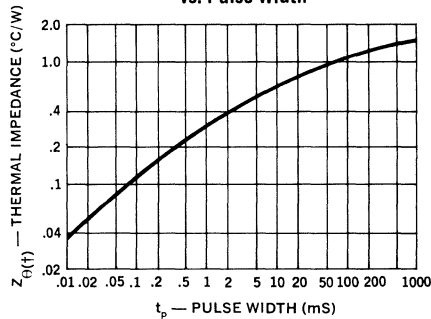
Forward Pulse Current vs. Duration



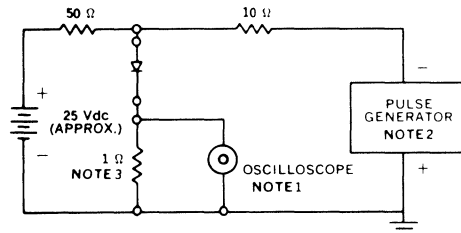
Multiple Surge Current vs. Duration



Thermal Impedance vs. Pulse Width



Reverse-Recovery Circuit



- NOTES:**
- Oscilloscope: Rise time $\leq 3nS$; input impedance = 50 Ω .
 - Pulse Generator: Rise time $\leq 8nS$; source impedance 10 Ω .
 - Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 30A Center-Tap

UES2601-UES2603

FEATURES

- Very Low Forward Voltage
- Very Fast Switching Speed
- Convenient Package
- High Surge
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

This series combines two high efficiency devices into one package, simplifying installation, reducing heat sink requirements and the need to purchase matched components.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2601	50V
Peak Inverse Voltage, UES2602	100V
Peak Inverse Voltage, UES2603	150V
Maximum Average D.C. Output Current at $T_C = 100^\circ\text{C}$	30A
Non-Repetitive Sinusoidal Surge Current 8.3 ms	400A
Thermal Resistance, Junction to Case	1°C/W
Operating and Storage Temperature Range	-55°C to $+175^\circ\text{C}$

POWER CYCLING

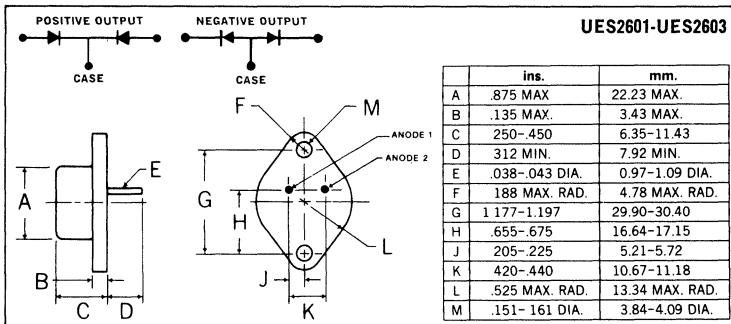
These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C , at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

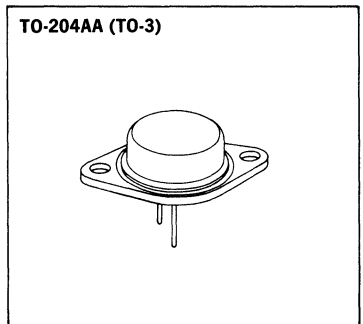
SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS



TO-204AA (TO-3)



Note:

Standard polarity is positive output.

For reverse polarity (negative output) add suffix "R", ie. UES2601R.

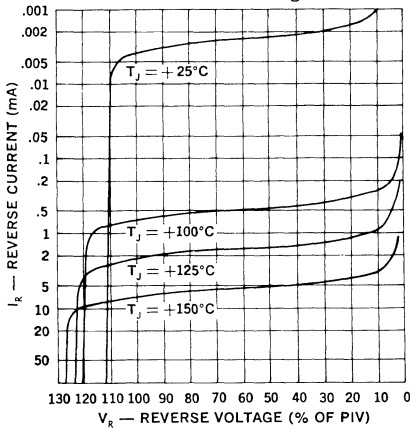
ELECTRICAL SPECIFICATIONS

UES2601- UES2603

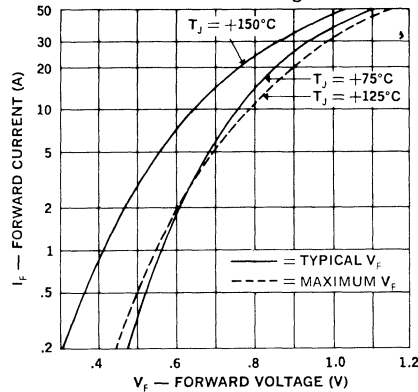
Type	PIV	Maximum Forward Voltage @		Maximum Reverse Current @		Maximum Reverse Recovery Time*
		$T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$	$T_r = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$	
UES2601	50V	.930V @ 15A	.825V @ 15A	20 μA	4mA	35nS
UES2602	100V					
UES2603	150V	$t_p = 300\mu\text{S}$	$t_p = 300\mu\text{S}$			

* Measured in circuit $I_F = 0.5\text{A}$, $I_R = 1\text{A}$, $I_{\text{REC}} = 0.25\text{A}$

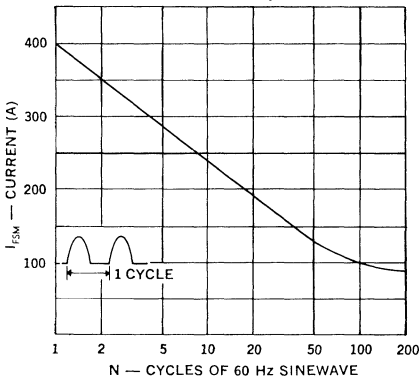
Typical Reverse Current vs. Reverse Voltage



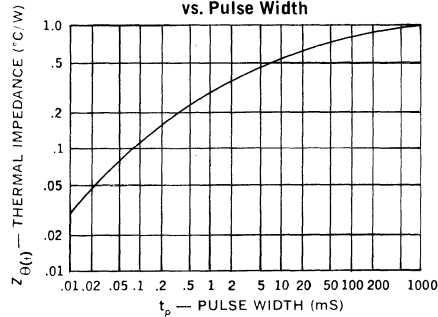
Forward Current vs. Forward Voltage



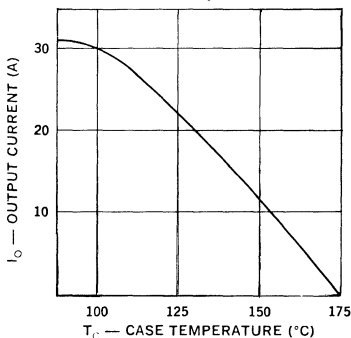
Maximum Forward Surge vs. Number of Cycles



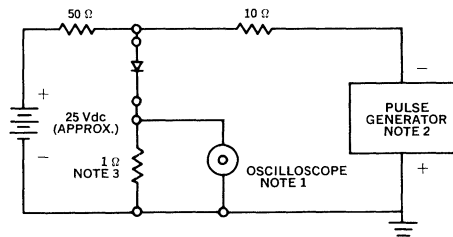
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



NOTES:

1. Oscilloscope: Rise time $\leq 3\text{ns}$; input impedance = 50 Ω .
2. Pulse Generator: Rise time $\leq 8\text{ns}$; source impedance 10 Ω .
3. Current viewing resistor, non-inductive, coaxial recommended.

RECTIFIERS

High Efficiency, 30A Center-Tap

UES2604-UES2606

FEATURES

- Very Low Forward Voltage (1.15V)
- Very Fast Recovery Times (50nSec)
- Low Profile Package
- High Surge Capability
- Low Thermal Resistance
- Mechanically Rugged
- Both Polarities Available

DESCRIPTION

The UES2604 series is specifically designed for operation in power switching circuits operating at frequencies of at least 20 KHz.

This series combines two high efficiency devices into one package, simplifying installation, reducing heat sink requirements and the need to purchase matched components.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage, UES2604	200V
Peak Inverse Voltage, UES2605	300V
Peak Inverse Voltage, UES2606	400V
Maximum Average D.C. Output Current @ $T_c = 100^\circ\text{C}$	30A
Surge Current, 8.3mSec	300A
Thermal Resistance, Junction to Case	$1^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	-55°C to $+150^\circ\text{C}$

POWER CYCLING

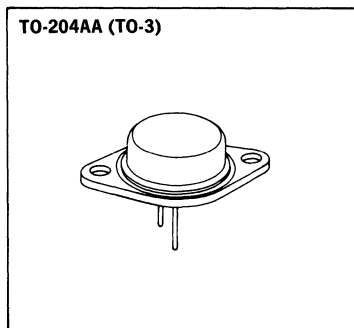
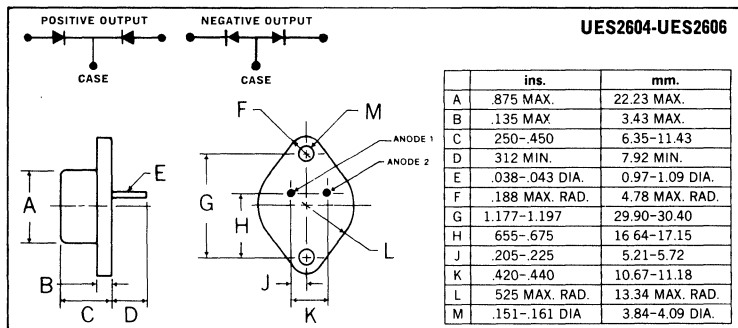
These devices possess the unique ability to pass many thousands of cycles of a stress test designed to evaluate the integrity of the bonding systems used in the construction of power rectifiers.

In this stress test, the case of the device is not heat sunk. Full rated forward current is supplied to force a case temperature increase at least 75°C , at which time, the current is removed and the case allowed to cool. The cycle is repeated a minimum of 5,000 times to simulate equipment being turned on and off. Extended power cycling tests demonstrate a product capability in excess of 25,000 cycles.

SWITCHING CHARACTERISTICS

The switching times of these ultra-fast rectifiers increase relatively little, with temperature or at different currents. Even in severe applications, such as catch diodes for switching regulators and output rectifiers for high frequency square wave inverters, these devices switch many times faster than the fastest associated transistors. Thus, the stresses on and powers dissipated in the switching transistors are substantially less than when using other rectifiers.

MECHANICAL SPECIFICATIONS



Note:

Standard polarity is positive output.

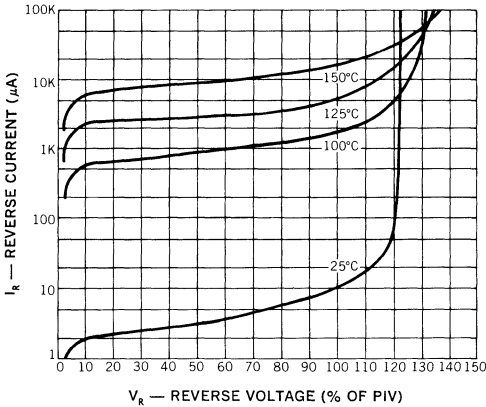
For reverse polarity (negative output) add suffix "R", ie. UES2604R.

ELECTRICAL SPECIFICATIONS, PER LEG

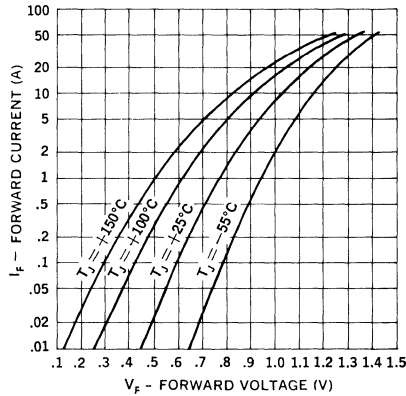
Type	PIV	Maximum Forward Voltage		Maximum Reverse Current		Maximum Reverse Recovery Time*
		T _c = 25°C	T _c = 125°C	T _c = 25°C	T _c = 125°C	
UES2604	200V	1.25V	1.15V	50μA	10mA	50nS
UES2605	300V	@ 15A	@ 15A			
UES2606	400V	t _p = 300μS	t _p = 300μS			

*Measured in circuit I_F = .5A, I_R = 1A, I_{REC} = .25A

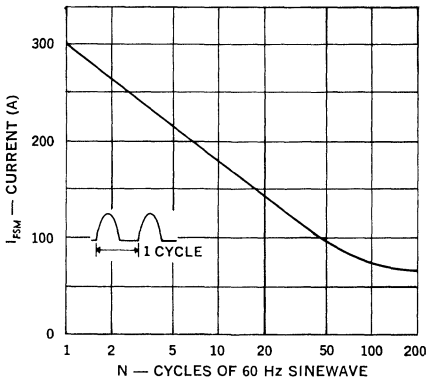
Typical Reverse Current vs. Reverse Voltage



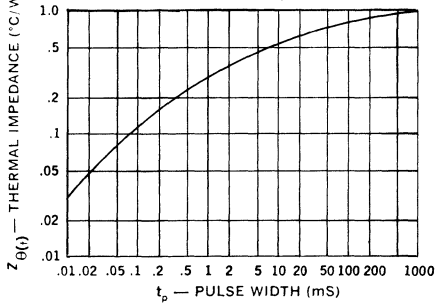
Forward Current vs. Forward Voltage



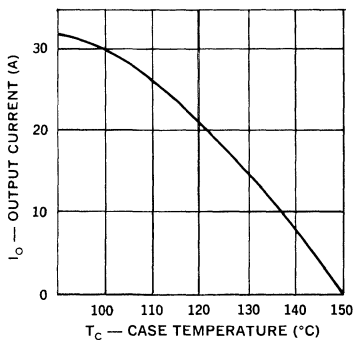
Maximum Forward Surge vs. Number of Cycles



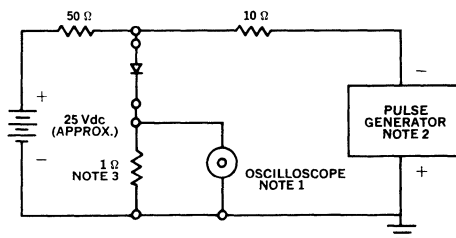
Thermal Impedance vs. Pulse Width



Output Current vs. Case Temperature



Reverse-Recovery Circuit



NOTES:

- Oscilloscope: Rise time ≤ 3ns; input impedance = 50Ω.
- Pulse Generator: Rise time ≤ 8ns; source impedance 10Ω.
- Current viewing resistor, non-inductive, coaxial recommended.



POWER SCHOTTKY MODULES

100A, Up to 50V

USM140C
USM145C
USM150C
Preliminary

FEATURES

- Low Forward Voltage
- Low Recovered Charge
- High Reverse Transient Capability
- High Surge Current
- High Efficiency for Low Voltage Designs

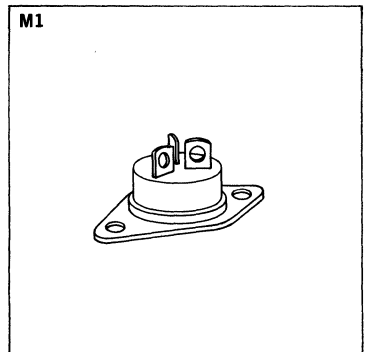
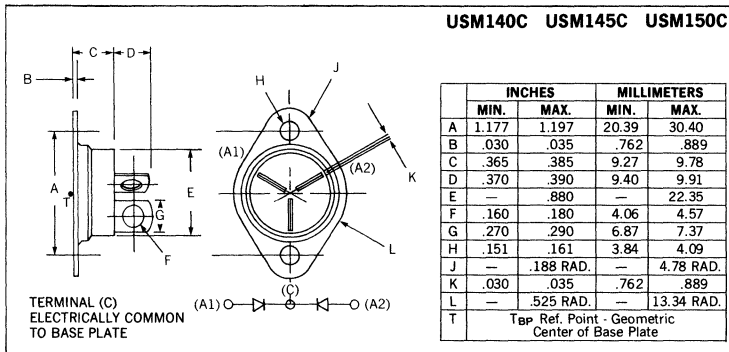
DESCRIPTION

The Unitrode Schottky Module utilizes high current Schottky rectifiers, in a convenient single package, arranged in a common cathode configuration. The combination of low thermal resistance and high conductance terminals makes this device ideally suited for high current full wave center-tap rectification or feed-forward applications.

ABSOLUTE MAXIMUM RATINGS (per diode unless noted)

	USM140C	USM145C	USM150C
Working Peak Reverse Voltage, V_{RWM}	40V	45V	50V
DC Blocking Voltage, V_R	40V	45V	50V
Peak Repetitive Surge Voltage, V_{RSM}	48V	54V	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz 50 Percent Duty Cycle), I_{FRM}	100A		
Average Rectified Forward Current, I_O	100A (@ $T_c = 115^\circ\text{C}$ Fullwave Configuration)		
Non-repetitive Peak Surge Current, I_{FSM}	1000A		
Peak Reverse Transient Current, I_{PRM}	2A		
Storage Temperature Range, T_{STG}	-40°C to +150°C		
Operating Temperature Range, T_J	-40°C to +175°C		
Thermal Resistance, $R_{\theta JB}$	0.7°C/W per module		

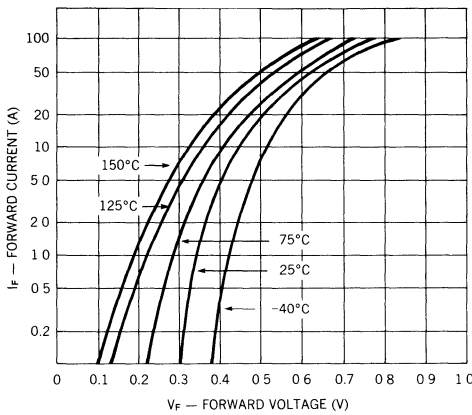
MECHANICAL SPECIFICATIONS



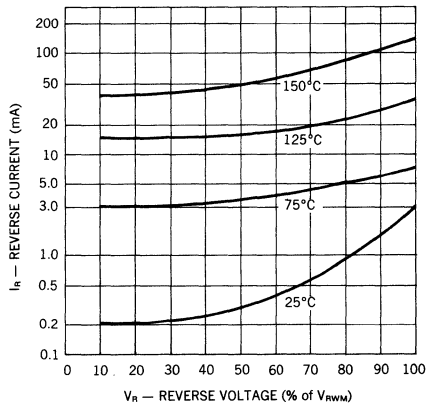
ELECTRICAL CHARACTERISTICS (T_{BP} = 25°C unless noted) (Per Diode)

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMIT	UNITS
Maximum Instantaneous Reverse Current	i _R	V _R = V _{RWM} (T _{BP} = 125°C) Pulsewidth = 400μs Duty Cycle = 1%	20 (75)	mA
Maximum Instantaneous Forward Voltage	V _F	I _F = 60A (T _{BP} = 125°C) Pulsewidth = 300μs Duty Cycle = 1%	.690 (.630)	V
Maximum Instantaneous Forward Voltage	V _F	I _F = 100A (T _{BP} = 125°C) Pulsewidth = 300μs Duty Cycle = 1%	.860 (.775)	V
Capacitance	C _t	V _R = 5V	3000	pF
Voltage Rate of Change	dv/dt	V _R = V _{RWM}	1000	V/μs
Reverse Energy	I _{RM}	See Reverse Energy Circuit	2	A

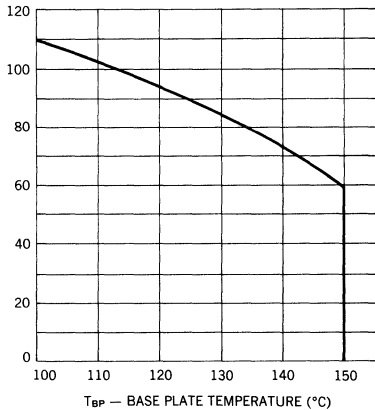
Typical Forward Current vs Forward Voltage



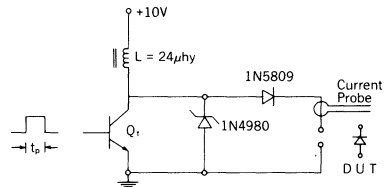
Typical Reverse Current vs Reverse Voltage



Output Current vs Case Temperature



Reverse Energy Circuit



t_p adjust for desired peak current in D.U.T. when Q turns off.
Q₁ must have fall time t_f of 100ns max.

POWER SCHOTTKY MODULES

200A, Up to 50V

USM20040C
 USM20045C
 USM20050C
 Preliminary

FEATURES

- Low Forward Voltage
- Low Recovered Charge
- High Reverse Transient Capability
- High Surge Current
- High Efficiency for Low Voltage Designs

DESCRIPTION

The Unitrode Schottky Module utilizes high current Schottky rectifiers, in a convenient single package, arranged in a common cathode configuration. The combination of low thermal resistance and high conductance terminals makes this device ideally suited for higher current full wave center-tap rectification or feed-forward applications.

ABSOLUTE MAXIMUM RATINGS (per diode unless noted)

	USM20040C	USM20045C	USM20050C
Working Peak Reverse Voltage, V_{RWM}	40V	45V	50V
DC Blocking Voltage, V_R	40V	45V	50V
Peak Repetitive Surge Voltage, V_{RSM}	48V	54V	60V
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20KHz 50 Percent Duty Cycle), I_{FRM}	200A		
Average Rectified Forward Current, I_o	200A (@ $T_c = 115^\circ\text{C}$ Fullwave Configuration)		
Non-repetitive Peak Surge Current, I_{FSM}	2000A		
Peak Reverse Transient Current, I_{RM}	2A		
Storage Temperature Range, T_{STG}	-40°C to $+175^\circ\text{C}$		
Operating Temperature Range, T_J	-40°C to $+175^\circ\text{C}$		
Thermal Resistance, $R_{\theta JB}$	0.28°C/W per module		
Thermal Resistance, $R_{\theta JBP}$	0.56°C/W per leg		

MECHANICAL SPECIFICATIONS

USM20040C USM20045C USM20050C

Terminal Torque: 50 (Min.) 75 (Max.) lb. — in.
 Mounting Base Torque: 30 (Min.) 40 (Max.) lb. — in.

	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A		2.63		66.80
B	1.35	1.40	34.29	35.56
C	.70	.80	17.78	20.32
D		.625		15.88
E	3.14	3.16	79.76	80.26
F		3.65		92.71
G	.25	.27	6.35	6.86
H	$\frac{1}{4}$ — 20 UNF With Captive Lockwasher			
T	Top Ref. Point - Geometric Center of Base Plate			

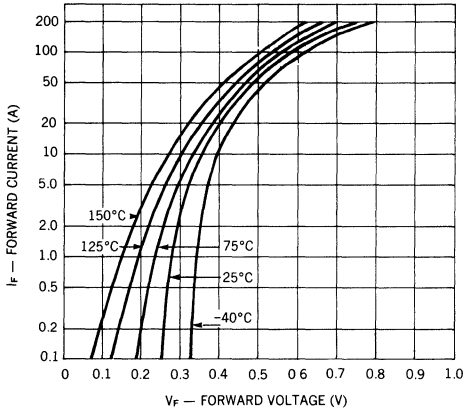
C (ELECTRICALLY COMMON TO BASE PLATE)

M2

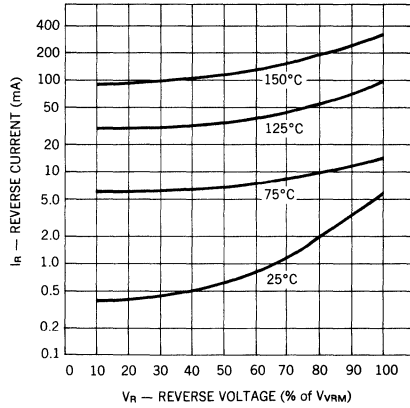
ELECTRICAL CHARACTERISTICS (T_{BP} = 25°C unless noted) (Per Diode)

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMIT		UNITS
			USM20045C	USM20050C	
Maximum Instantaneous Reverse Current	i_R	$V_R = V_{RWM}$ Pulsewidth = 400μs Duty Cycle = 1% (T _{BP} = 125°C)	30 (125)	30 (150)	mA
Maximum Instantaneous Forward Voltage	V_F	$I_F = 100A$ Pulsewidth = 300μs Duty Cycle = 1% (T _{BP} = 125°C)	(.575)		V
Maximum Instantaneous Forward Voltage	V_F	$I_F = 200A$ Pulsewidth = 300μs Duty Cycle = 1% (T _{BP} = 125°C)	.800 (.745)		V
Capacitance	C_t	$V_R = 5V$	6000		pF
Voltage Rate of Change	dv/dt	$V_R = V_{RWM}$	1000		V/μs
Reverse Energy	I_{RM}	See Reverse Energy Circuit	2		A

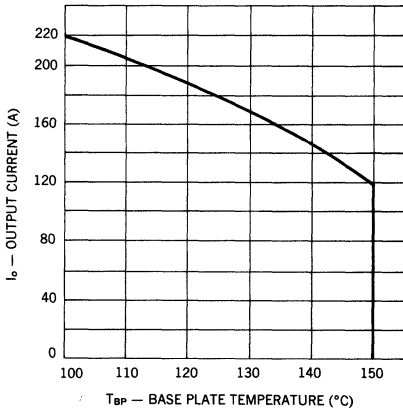
Typical Forward Current vs Forward Voltage



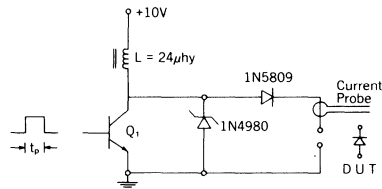
Typical Reverse Current vs Reverse Voltage



Output Current vs Case Temperature



Reverse Energy Circuit



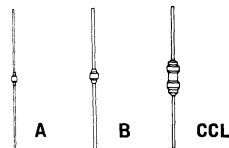
t_p adjust for desired peak current in D.U.T. when Q turns off. Q₁ must have fall time t_f of 100ns max.

POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS

PRODUCT SELECTION GUIDE

Transient Voltage Suppressors

Part No.		Stand-Off Voltage V_R	Min. Breakdown Voltage $BV_{(min)}$ @ 1mA	Max. Peak Pulse Current I_{PP}	Max. Clamping Voltage* V_C @ I_{PP}	Peak Power for 1ms (W)	
		(V)	(V)	(A)	(V)	(W)	
Package Style	A Body	TVS305	5.0	6.0	17	8.7	150
		TVS310	10.0	11.1	8.9	16.8	
		TVS312	12.0	13.8	7.1	21.0	
		TVS315	15.0	16.7	5.9	25	
		TVS318	18.0	20.4	4.9	31	
		TVS324	24.0	28.4	3.6	42	
		TVS328	28.0	30.7	3.2	46	
		TVS348	48.0	54	1.7	82	
		TVS360	60.0	67	1.4	105	
		TVS410	100.0	111	.91	160	
		TVS420	200.0	234	.42	360	
		TVS430	300.0	342	.28	520	
		Package Style	B Body	TVS505	5.0	6.0	
TVS510	10.0			11.1	30.3	16.5	
TVS512	12.0			13.8	23.8	21.0	
TVS515	15.0			16.7	19.8	25.2	
TVS518	18.0			20.4	16.3	30.5	
TVS524	24.0			28.4	11.9	42.0	
TVS528	28.0			30.7	10.7	46.5	
1N6461**	5.0			5.6 @ 25mA	56	9	500
1N6462**	6.0	6.5 @ 20mA	46	11			
1N6463**	12.0	13.6 @ 5mA	22	22.6			
1N6464**	15.0	16.4 @ 5mA	19	26.5			
1N6465**	24.0	27.0 @ 2mA	12	41.4			
1N6466**	30.5	33.0 @ 1mA	11	47.5			
1N6467**	40.3	43.7 @ 1mA	8	63.5			
1N6468**	51.6	54.0 @ 1mA	6	78.5			
CCL Body		1N5610*		33.0	32.0	47.5	1500
		1N5611*		43.7	24.0	63.5	
		1N5612*		54.0	19.0	79.5	
		1N5613*		191.0	5.7	265.0	



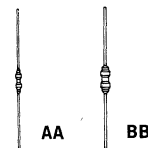
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*Available in JAN & JANTX

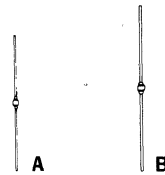
**Available in JAN, JANTX and JANTXV

Bi-directional Zeners

Power		1W	3W	5W
Package Style		AA		BB
Voltage, V (10% Tolerance)	7.5	UDZ8807	UDZ807	UDZ5807
	8.2	UDZ8808	UDZ808	UDZ5808
	9.1	UDZ8809	UDZ809	UDZ5809
	10	UDZ8810	UDZ810	UDZ5810
	12	UDZ8812	UDZ812	UDZ5812
	15	UDZ8815	UDZ815	UDZ5815
	18	UDZ8818	UDZ818	UDZ5818
	20	UDZ8820	UDZ820	UDZ5820
	24	UDZ8824	UDZ824	UDZ5824
	27	UDZ8827	UDZ827	UDZ5827
	30	UDZ8830	UDZ830	UDZ5830
	33	UDZ8833	UDZ833	UDZ5833
36	UDZ8836	UDZ836	UDZ5836	
40	UDZ8840	UDZ840	UDZ5840	
45	UDZ8845	UDZ845	UDZ5845	
60	UDZ8860	UDZ860	UDZ5860	



POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS



POWER ZENERS

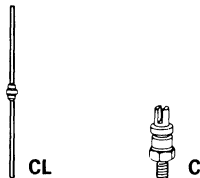
Power	1W	1.5W	3W	3W	5W	5W	6W	10W	
Package Style	A	A	A	A	B	B	CL	C	
VOLTAGE Vz (5% Tolerance)	5.6V						1N5968*		
	6.2V						1N5969*		
	6.8V	UZ8706	1N4461*	1N5063	BZV16C6V8***	UZ4706	1N4954*	UZ7706L	UZ7706
	7.5V	UZ8707	1N4462*	1N5064	BZV16C7V5***	UZ4707	1N4955*	UZ7707L	UZ7707
	8.2V	UZ8708	1N4463*	1N5065	BZV16C8V2***	UZ4708	1N4956*	UZ7708L	UZ7708
	9.1V	UZ8709	1N4464*	1N5066	BZV16C9V1***	UZ4709	1N4957*	UZ7709L	UZ7709
	10V	UZ8710	1N4465*	1N5067	BZV16C10 ***	UZ4710	1N4958*	UZ7710L	UZ7710
	11V	UZ8711	1N4466*	1N5068	BZV16C11***		1N4959*	UZ7711L	UZ7711
	12V	UZ8712	1N4467*	1N4883	BZV16C12***	UZ4712	1N4960*	UZ7712L	UZ7712
	13V	UZ8713	1N4468*	1N5069	BZV16C13***	UZ4713	1N4961*	UZ7713L	UZ7713
	14V	UZ8714		1N5070			1N5118	UZ7714L	UZ7714
	15V	UZ8715	1N4469*	1N5071	BZV16C15***	UZ4715	1N4962*	UZ7715L	UZ7715
	16V	UZ8716	1N4470*	1N5072	BZV16C16***	UZ4716	1N4963*	UZ7716L	UZ7716
	18V	UZ8718	1N4471*	1N5073	BZV16C18***	UZ4718	1N4964*	UZ7718L	UZ7718
	20V	UZ8720	1N4472*	1N4884	BZV16C20***	UZ4720	1N4965*	UZ7720L	UZ7720
	22V	UZ8722	1N4473*	1N5074	BZV16C22***	UZ4722	1N4966*	UZ7722L	UZ7722
	24V	UZ8724	1N4474*	1N5075	BZV16C24***	UZ4724	1N4967*	UZ7724L	UZ7724
	27V	UZ8727	1N4475*	1N5076	BZV16C27***	UZ4727	1N4968*	UZ7727L	UZ7727
	30V	UZ8730	1N4476*	1N5077	BZV16C30***	UZ4730	1N4969*	UZ7730L	1N7730
	33V	UZ8733	1N4477*	1N5078	BZV16C33***	UZ4733	1N4970*	UZ7733L	UZ7733
	36V	UZ8736	1N4478*	1N5079	BZV16C36***	UZ4736	1N4971*	UZ7736L	UZ7736
	39V		1N4479*	1N5080	BZV16C39***	UZ4739	1N4972*		
	40V	UZ8740		1N5081			1N5119	UZ7740L	UZ7740
	43V		1N4480*	1N5082	BZV16C43***	UZ4743	1N4973*		
	45V	UZ8745		1N5083			1N5120	UZ7745L	UZ7745
	47V		1N4481*	1N5084	BZV16C47***	UZ4747	1N4974*		
	50V	UZ8750		1N5085			1N5121	UZ7750L	UZ7750
	51V		1N4482*	1N5086	BZV16C51***	UZ4751	1N4975*		
	56V	UZ8756	1N4483*	1N5087	BZV16C56***	UZ4756	1N4976*	UZ7756L	UZ7756
	60V	UZ8760		1N5088			1N5122	UZ7760L	UZ7760
62V		1N4484*	1N5089	BZV16C62***	UZ4762	1N4977*			
68V		1N4485*	1N5090	BZV16C68***	UZ4768	1N4978*			
PULSE POWER	100W	140W	230W	230W	720W	900W	2000W	2000W	

* Available as JAN, JANTX, & JANTXV

** For 100µs pulse width

† 10% and 20% tolerance also available

*** Pro Electron Diodes 7% tolerance



POWER ZENERS

Power	1W	1.5W	3W	3W	5W	5W	6W	10W
Package Style	A	A	A	A	B	B	CL	C
VOLTAGE V_z (5% Tolerance)	70V	UZ8770		1N5091				
	75V	UZ8775	1N4486*	1N5092	BZV16C75***	UZ4775	1N5123	UZ7770L
	80V	UZ8780		1N5093			1N4979*	UZ7775L
	82V		1N4487*	1N5094	BZV16C82***	UZ4782	1N5124	UZ7780L
	82V			1N5094			1N4980*	
	82V			1N5094			1N5125	UZ7790L
	82V	UZ8790		1N4096				UZ7790
	91V		1N4488*	1N4095	BZV16C91***	UZ4791	1N4981*	
	100V	UZ8110	1N4489*	1N4097	BZV16C100***	UZ4110	1N4982*	UZ7110L
	110V	UZ8111	1N4490*	1N5096		UZ4111	1N4983*	
	120V	UZ8112	1N4491*	1N5097		UZ4112	1N4984*	
	130V	UZ8113	1N4492*	1N5098		UZ4113	1N4985*	
	140V	UZ8114		1N5099				
	150V	UZ8115	1N4493*	1N5098		UZ4115	1N4986*	
	160V	UZ8116	1N4494*	1N5100		UZ4116	1N4987*	
	170V	UZ8117		1N5101			1N5127	
	180V	UZ8118	1N4495*	1N5102		UZ4118	1N4988*	
	190V	UZ8119		1N5103			1N5128	
	200V	UZ8120	1N4496*	1N5104		UZ4120	1N4989*	
	220V			1N5105			1N4990*	
240V			1N5106			1N4991*		
260V			1N5107			1N5129		
270V			1N5108			1N4992*		
280V			1N5109			1N5130		
300V			1N5110			1N4993*		
320V			1N5111			1N5131		
330V			1N5112			1N4994*		
340V			1N5113			1N5132		
360V			1N5114			1N4995*		
380V			1N5115			1N5133		
390V			1N5116			1N4996		
400V			1N5117			1N5134		
PULSE POWER **	100W	140W	230W	230W	720W	900W	2000W	2000W

* Available as JAN, JANTX, & JANTXV
 ** For 100 μ s pulse width
 † 10% and 20% tolerance also available
 *** Pro Electron Diodes 7% tolerance

POWER ZENERS

1.5 Watt, Military

1N4461-1N4496
JAN, JANTX & JANTXV

FEATURES

- 5 Times Greater Surge Rating than JAN1N3016 Series
- Low Reverse Current: to 50nA
- ¼ Size of Conventional 1 Watt Zeners

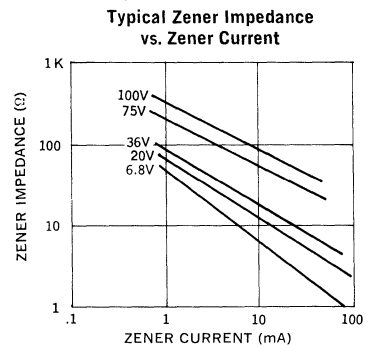
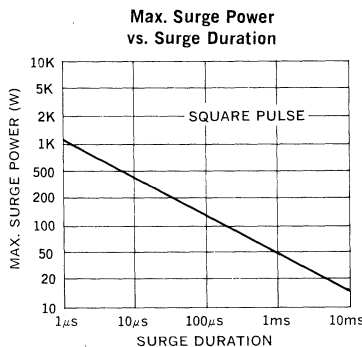
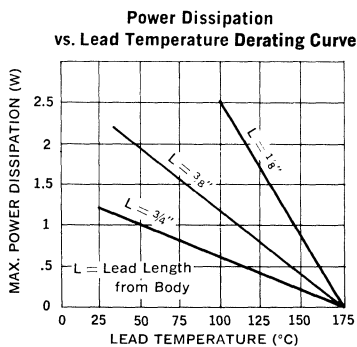
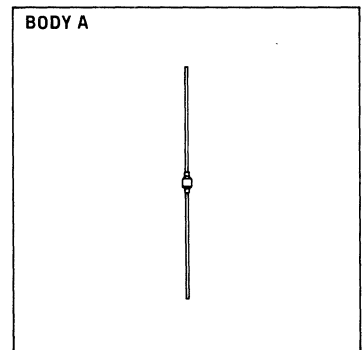
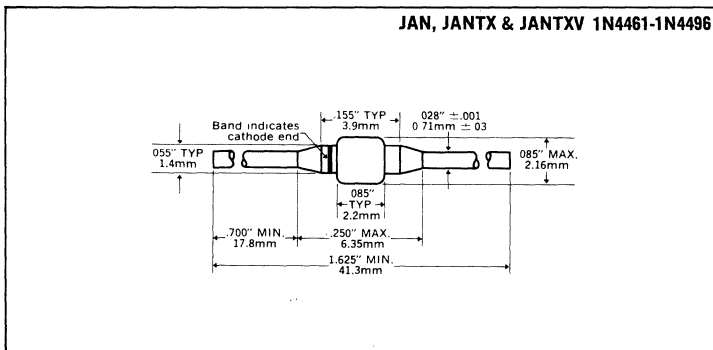
DESCRIPTION

Fused-in-glass, metallurgically bonded
1.5 watt zeners, qualified to MIL-S-19500/406.

ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z	6.8 to 200V
Continuous Current	See Table
Surge Current (8.3ms)	See Table
Surge Power	See Graph
Power	See Lead Temperature Derating Curve
Storage and Operating Temperature	-65°C to +175°C

MECHANICAL SPECIFICATIONS



Type	Electrical Specifications at 25°C								Maximum Ratings	
	Nominal Zener Voltage † V _Z @ I _{ZT}	Test Current I _{ZT}	Max. Zener Impedance ‡			Voltage ** Regulation ΔBV Max	Maximum Reverse Leakage Current		Maximum Cont. Current I _{ZM}	Maximum Surge Current † I _S
			Z _Z @ I _{ZT}	Z _{ZK} @ I _{ZK}	I _{ZK}		I _R @ V _R	V _R		
			Ohms	Ohms	mA		μA	Volts		
±5% Tolerance	Volts	mA	Ohms	Ohms	mA	Volts	μA	Volts	mA	Amps
1N4461	6.8	37	2.5	200	1.0	.30	5.0	4.08	210	5.0
1N4462	7.5	34	2.5	400	.5	.35	1.0	4.50	191	4.5
1N4463	8.2	31	3.0	400	.5	.40	.50	4.92	174	3.9
1N4464	9.1	28	4.0	500	.5	.45	.30	5.46	157	3.4
1N4465	10	25	5.0	500	.25	.50	.30	8.0	143	3.0
1N4466	11	23	6.0	550	.25	.55	.30	8.8	130	2.6
1N4467	12	21	7.0	550	.25	.60	.20	9.6	119	2.4
1N4468	13	19	8.0	550	.25	.65	.10	10.4	110	2.2
1N4469	15	17	9.0	600	.25	.75	.05	12.0	95	1.8
1N4470	16	15.5	10.0	600	.25	.80	.05	12.8	90	1.6
1N4471	18	14	11.0	650	.25	.83	.05	14.4	79	1.4
1N4472	20	12.5	12.0	650	.25	.95	.05	16.0	71	1.2
1N4473	22	11.5	14	650	.25	1.0	.05	17.6	65	1.1
1N4474	24	10.5	16	700	.25	1.1	.05	19.2	60	.90
1N4475	27	9.5	18	700	.25	1.3	.05	21.6	53	.80
1N4476	30	8.5	20	750	.25	1.4	.05	24.0	48	.75
1N4477	33	7.5	25	800	.25	1.5	.05	26.4	43	.66
1N4478	36	7.0	27	850	.25	1.7	.05	28.8	40	.60
1N4479	39	6.5	30	900	.25	1.8	.05	31.2	37	.54
1N4480	43	6.0	40	950	.25	1.9	.05	34.4	33	.48
1N4481	47	5.5	50	1000	.25	2.1	.05	37.6	30	.45
1N4482	51	5.0	60	1100	.25	2.3	.05	40.8	28	.42
1N4483	56	4.5	70	1300	.25	2.5	.05	44.8	26	.39
1N4484	62	4.0	80	1500	.25	2.7	.05	49.6	23	.35
1N4485	68	3.7	100	1700	.25	3.0	.05	54.4	21	.32
1N4486	75	3.3	130	2000	.25	3.3	.05	60.0	19	.29
1N4487	82	3.0	160	2500	.25	3.6	.05	65.6	17	.26
1N4488	91	2.8	200	3000	.25	4.0	.05	72.8	16	.23
1N4489	100	2.5	250	3100	.25	4.4	.25	80.0	14	.20
1N4490	110	2.0	300	4000	.25	5.0	.25	88.0	13	.19
1N4491	120	2.0	400	4500	.25	5.5	.25	96.0	12	.18
1N4492	130	1.9	500	5000	.25	6.0	.25	104	11	.16
1N4493	150	1.7	700	6000	.25	7.0	.25	120	9.5	.14
1N4494	160	1.6	1000	6500	.25	8.0	.25	128	8.9	.12
1N4495	180	1.4	1300	7000	.25	10.0	.25	144	7.9	.10
1N4496	200	1.2	1500	8000	.25	12.0	.25	160	7.2	.08



† All Zener voltages are measured with an automated test set using a 35 millisecond test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

‡ Zener impedance is derived from the 60 cycle AC Voltage created when AC current with RMS value of 10% of DC Zener test current is superimposed on the test current.

** ΔBV is obtained by measuring the voltage change when the test current is changed from 10% to 50% of I_Z max under DC conditions. During this measurement the leads are heat sunk .375 inch from the body and maintained at 25°C.

† Ratings shown are for peak sinusoidal surge current of 8.3 ms duration, non-repetitive. The 8.3 ms square pulse rating is 71% of the value shown. Rating exceeds JEDEC Registered Specification.

POWER ZENERS

5 Watt, Military

1N4954-1N4995
 1N5968-1N5969
 JAN, JANTX & JANTXV
 1N4996

FEATURES

- 2 Times Greater Surge Rating than Conventional 10 Watt Zeners
- Small Physical Size

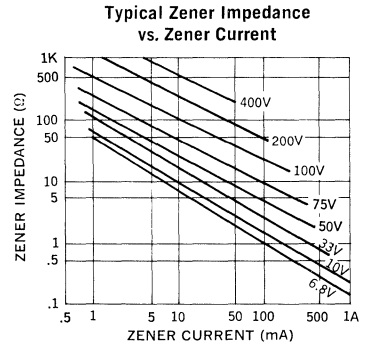
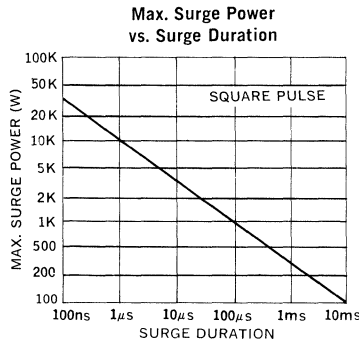
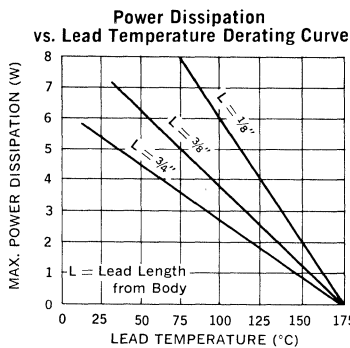
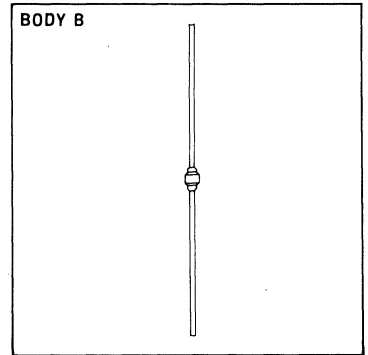
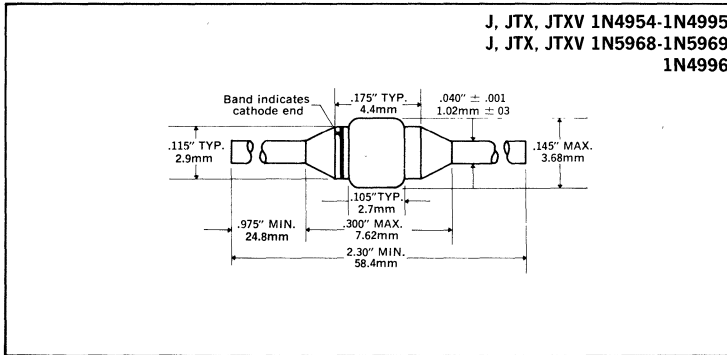
DESCRIPTION

Fused-in-glass, metallurgically-bonded
 5 watt zeners, qualified to MIL-S-19500/356.

ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z 5.6 to 390V
 Continuous Current See Table
 Surge Current (8.3ms) See Table
 Surge Power See Graph
 Power See Lead Temperature Derating Curve
 Storage and Operating Temperature -65°C to $+175^\circ\text{C}$

MECHANICAL SPECIFICATIONS



Electrical Specifications at 25°C										Maximum Ratings	
Type	Nominal Zener Voltage† V _Z @ I _{ZT}	Test Current I _{ZT}	Maximum Zener Impedance §		Voltage Regulation ΔBV §§	Maximum Reverse Leakage Current			Maximum Temperature Coeff. T _C @ I _{ZT}	Maximum Continuous Current★ I _{ZM}	Maximum Surge Current†† I _S
			Z _Z @ I _{ZT}	Z _{ZK} †† @ I _{ZT} = 1mA		I _R ††	I _R	V _R			
±5% Tolerance	Volts	mA	Ohms	Ohms	Volts	μA	Volts	%/°C	mA	Amps	
1N5968*	5.6	220	1.0	400	0.4	5000	5000	4.28	.04	865	20
1N5969*	6.2	220	1.0	1000	0.5	1000	1000	4.74	.04	765	20
1N4954*	6.8	175	1.0	1000	0.7	150	300	5.2	.05	700	40
1N4955*	7.5	175	1.5	800	0.7	100	200	5.7	.06	630	32
1N4956*	8.2	150	1.5	600	0.7	50	100	6.2	.06	580	24
1N4957*	9.1	150	2.0	400	0.7	25	50	6.9	.06	520	22
1N4958*	10.0	125	2.0	125	0.8	25	25	7.6	.07	475	20
1N4959*	11	125	2.5	130	0.8	10	15	8.4	.07	430	19
1N4960*	12	100	2.5	140	0.8	10	10	9.1	.07	395	18
1N4961*	13	100	3.0	145	0.8	10	10	9.9	.08	365	16
1N4962*	15	75	3.5	150	1.0	5	5	11.4	.08	315	12
1N4963*	16	75	3.5	155	1.1	5	5	12.2	.08	294	10
1N4964*	18	65	4.0	160	1.2	5	5	13.7	.085	264	9.0
1N4965*	20	65	4.5	165	1.5	2	2	15.2	.085	237	8.0
1N4966*	22	50	5.0	170	1.8	2	2	16.7	.085	216	7.0
1N4967*	24	50	5.0	175	2.0	2	2	18.2	.090	198	6.5
1N4968*	27	50	6.0	180	2.0	2	2	20.6	.090	176	6.0
1N4969*	30	40	8	190	2.5	2	2	22.8	.090	158	5.5
1N4970*	33	40	10	200	2.8	2	2	25.1	.095	144	5.0
1N4971*	36	30	11	220	3.0	2	2	27.4	.095	132	4.5
1N4972*	39	30	14	230	3.0	2	2	29.7	.095	122	4.0
1N4973*	43	30	20	240	3.3	2	2	32.7	.095	110	3.5
1N4974*	47	25	25	250	3.5	2	2	35.8	.095	100	3.2
1N4975*	51	25	27	270	4.0	2	2	38.8	.095	92	3.0
1N4976*	56	20	35	320	4.4	2	2	42.6	.095	84	2.8
1N4977*	62	20	42	400	5.0	2	2	47.1	.100	76	2.5
1N4978*	68	20	50	500	5.5	2	2	51.7	.100	70	2.2
1N4979*	75	20	55	620	6.0	2	2	56.0	.100	63.0	2.0
1N4980*	82	15	80	720	6.6	2	2	62.2	.100	58.0	1.8
1N4981*	91	15	90	760	7.5	2	2	69.2	.100	52.5	1.6
1N4982*	100	12	110	800	8.0	2	2	76.0	.100	47.5	1.4
1N4983*	110	12	125	1000	9.0	2	2	83.6	.100	43.0	1.2
1N4984*	120	10	170	1150	10	2	2	91.2	.100	39.5	1.00
1N4985*	130	10	190	1250	11	2	2	98.8	.105	36.6	0.80
1N4986*	150	8	330	1500	13	2	2	114.0	.105	31.6	0.75
1N4987*	160	8	350	1650	14	2	2	121.6	.105	29.4	0.70
1N4988*	180	5	450	1750	16	2	2	136.8	.110	26.4	0.60
1N4989*	200	5	500	1850	18	2	2	152	.110	23.6	0.50
1N4990*	220	5	550	2000	19	2	2	167	.115	21.6	0.50
1N4991*	240	5	650	2050	22	2	2	182	.115	19.8	0.40
1N4992*	270	5	800	2100	25	2	2	206	.120	17.5	0.35
1N4993*	300	4	950	2150	28	2	2	228	.120	15.6	0.30
1N4994*	330	4	1175	2200	32	2	2	251	.120	14.4	0.25
1N4995*	360	3	1400	2300	35	2	2	274	.120	13.0	0.22
1N4996	390	3	1800	2500	40	2	2	297	.120	12.0	0.20

* Available as JAN, JANTX & JANTXV.

† All zener voltages are measured with an automated test set using a 35 msec test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§ Zener impedance is derived from the 60-cycle voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

§§ ΔBV is obtained by measuring the voltage change when the test current is changed from 10% to 50% of I_Z max under DC conditions. During this measurement the leads are heat sunk .375 inch from the body and maintained at 25°C.

★ Maximum current based on 5 Watt Rating. See lead temperature derating curves for proper mounting methods.

†† Figures shown are for peak sinusoidal surge current of 8.3 msec duration, non-repetitive. The 8.3 ms square pulse rating is 71% of the value shown.

†† These specifications apply only to JAN and JANTX

POWER ZENERS

Transient Suppressor Diodes

JAN & JANTX 1N5610-1N5613

FEATURES

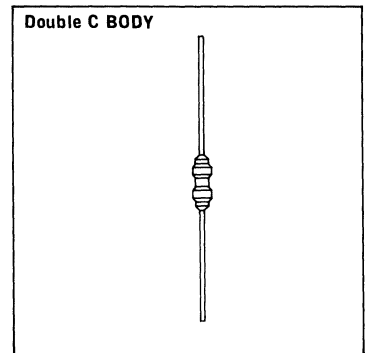
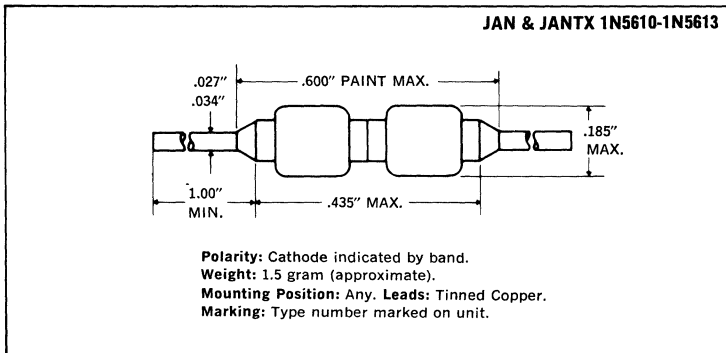
- 1500 Watts for 1ms Pulse Power Capability
- Small Physical Size
- Designed to be Used in Mil-Std-704A Applications

DESCRIPTION

Zener diodes with high surge capability qualified to MIL-S-19500/434.

ABSOLUTE MAXIMUM RATINGS (at 25°C except where otherwise noted)

	1N5610	1N5611	1N5612	1N5613
Zener Voltage		See Electrical Specifications		
Forward Surge Current	200A	200A	200A	200A
Zener Surge Current, at 25°C	32.0A	24.0A	19.0A	5.7A
Surge Current, at 150°C	5.5A	4.8A	3.2A	1.0A
Surge Power		See Graph		
Storage and Operating Temperature		-65°C to +175°C		



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Min. Zener Voltage § Vz @ ImA	Max. Zener Voltage† Vz @ Is		Max. Reverse Leakage Current Ik @ Vr		Max. Forward Voltage‡ @ 100 Amps	Typical Temperature Coefficient
	Volts	Volts	Amps	µA	Volts	Volts	%/°C
1N5610*	33.0	47.5	32.0	5.0	30.5	4.8	.093
1N5611*	43.7	63.5	24.0	5.0	40.3	4.8	.094
1N5612*	54.0	78.5	19.0	5.0	49.0	4.8	.096
1N5613*	191.0	265.0	5.7	5.0	175.0	4.8	.100

Notes: * Available as JAN and JANTX.

§ Duration of applied current ≤ 300ms, duty cycle ≤ 2%.

† Utilizing a pulse which decays exponentially to 50% of the peak value in 1ms. See graph entitled "Pulse Waveform."

‡ Peak Sinusoidal surge current of 8.3ms duration, non-repetitive.

APPLICATIONS

Voltage transients can be suppressed with series elements, shunt elements, or a combination of both. These elements may be passive or active. For low and medium power applications, a series resistor and zener clamp offer several attractive features:

1. Simplicity of design
2. High reliability
3. Fast response time

The 1N5610 series of surge suppressors will suppress the following transients defined by MIL-S-704A without the use of any series limiting resistance beyond that provided by the source:

1. All 600V transients (category #1 on chart below)
2. All 80V transients except those generated by the main voltage regulator (category #2 on chart below)
3. The overvoltage transients generated by the *main voltage regulator* (category #3 on chart below) will also be suppressed by the 1N5610 series if:
 - a. A 20 ohm series limiting resistor is used, or
 - b. No series resistance is used but the zener is protected within 500 µs by using, for example, an SCR crowbar

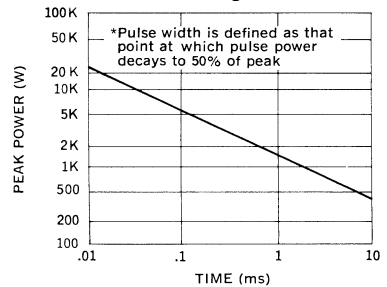
The above statements are based on the source impedances and dv/dt characteristics as given in ARINC* Specification #413. This report entitled "Guidance for Aircraft Electrical Power Utilization and Transient Protection" serves to further define MIL-STD-704A for large aircraft electrical systems.

Category	Source of Transient	Maximum Amplitude	Duration	Min. Source Impedance	dv/dt
1.	Inductive Switching	600 V	≤ 10 µs	50 ohms	
2.	BUS Switching	80 V	≤ 10 ms	15 ohms	
3.	Main Voltage Regulator	80 V	≥ 10 ms	0.2 ohms	50V/ms

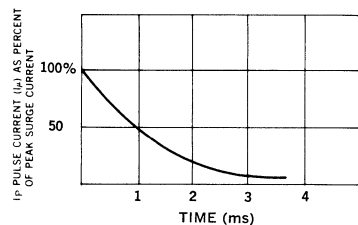
These Surge Suppressors are useful in a variety of other applications where semiconductor devices must function reliably in an environment subject to extremely high but short term surges.

* ARINC stands for Aeronautical Radio, Inc. (Annapolis, Maryland 21401)

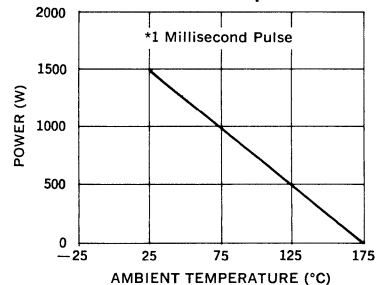
Peak Power Rating vs. Pulse Width*



Pulse Waveform



Peak Power Rating* vs. Ambient Temperature



TRANSIENT VOLTAGE SUPPRESSORS

500W, Military

1N6461-1N6468
JAN, JANTX & JANTXV

FEATURES

- 500W Power Capability for 1ms pulse
- Glass Encapsulated Device
- Clamping Time in Picoseconds

DESCRIPTION

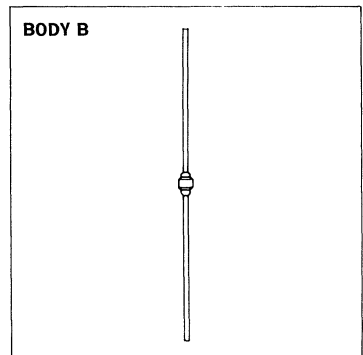
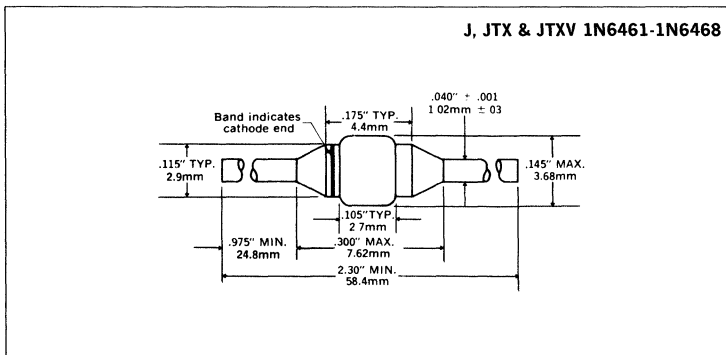
Transient voltage suppressor of noncavity design and qualified to MIL-S-19500/551. Metallurgically bonded for high reliability.

ABSOLUTE MAXIMUM RATINGS @ 25°C

Stand-off Voltage, V_R	5.0V to 51.6V
Peak Pulse Power (1ms)*, P_{PR}	500W
Forward Surge Current @ $t_p = 8.33\text{ms}$, I_{FSM}	80A(pk)
Peak Pulse Current	see table
Breakdown Voltage	see table
Power, Continuous (Derate @ $16.7\text{mW}/^\circ\text{C}$ above $T_A = 25^\circ\text{C}$), P_R	2.5W
Storage Temperature	-55°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+175^\circ\text{C}$

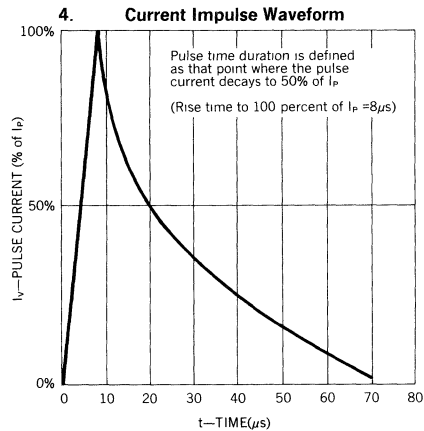
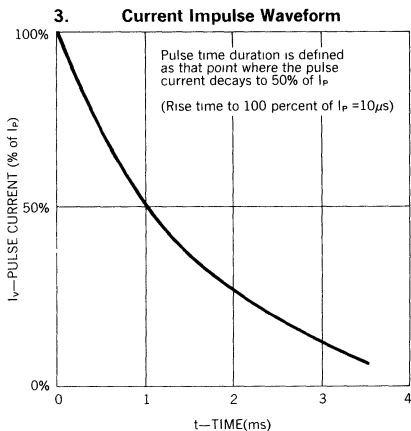
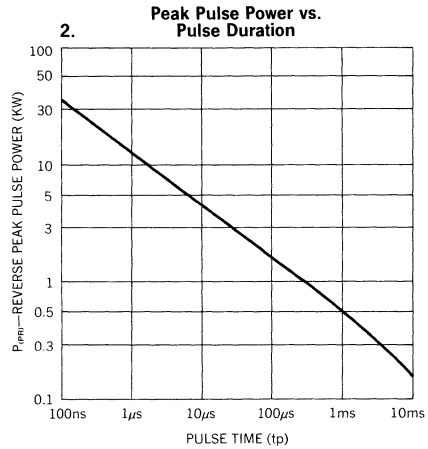
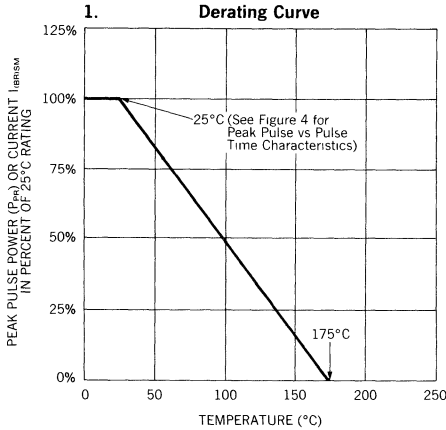
*See Figure 2 for Peak Pulse Power vs. Pulse Duration.

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS @ 25°C

Part No.	Stand-off Voltage V_R	Min. Breakdown Voltage @ I_{BR}	Test Current I_{BR} @ $t_p = 300ms$ Duty Cycle $\leq 2\%$	Max. Leakage Current I_R @ V_R	Max. Peak Pulse Current I_{PP}		Max. Clamping Voltage ($V_{C MAX}$) @ I_{PP} for $t_p = 1ms$	Max. Clamping Voltage @ I_{PP} Inverse Voltage $-V_{C MAX}$ ($t_p = 1ms$)	Max. Temperature Coefficient $\propto V_{(BR)}$
					$t_p = 1ms$ $t_r = 10\mu s$ (Fig. 3)	$t_p = 20\mu s$ $t_r = 8\mu s$ (Fig. 4)			
	V	V	mA	μA	A(pk)	A(pk)	V	V	%/°C
1N6461	5.0	5.6	25	3000	56	315	9.0	-3.5	0.040
1N6462	6.0	6.5	20	2500	46	258	11.0	-3.2	0.040
1N6463	12.0	13.6	5	500	22	125	22.6	-3.8	0.050
1N6464	15.0	16.4	5	500	19	107	26.5	-3.8	0.060
1N6465	24.0	27.0	2	50	12	69	41.4	-3.6	0.084
1N6466	30.5	33.0	1	3	11	63	47.5	-3.6	0.093
1N6467	40.3	43.7	1	2	8	45	63.5	-3.5	0.094
1N6468	51.6	54.0	1	2	6	35	78.5	-3.4	0.096



TRANSIENT VOLTAGE SUPPRESSORS

TVS305-TVS430
TVS505-TVS528

FEATURES

- Up to 500W for 1mS Pulse Power Capability
- Clamping Time in Picoseconds
- Direct Applicability for all popular Microprocessors and IC families
- Metallurgically bonded assembly system to assure long term reliability
- Miniature glass encased hermetically sealed package

DESCRIPTION

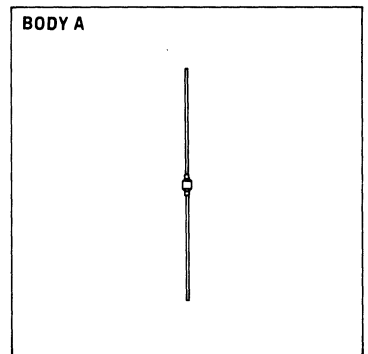
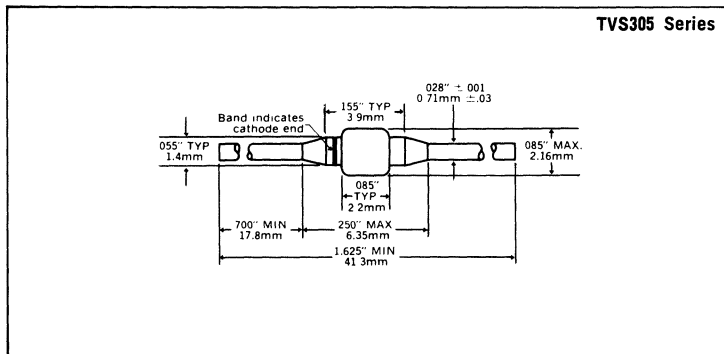
Unitrode's TVS series of transient voltage suppressors feature oxide passivated zener type chips with full-faced metallurgical bonds on both sides to achieve high surge capability and negligible electrical degradation under repeated surge conditions. The series is especially useful in protecting microprocessor, MOS, CMOS, TTL, Schottky TTL, ECL, I²L and linear integrated circuits from spurious transient disturbances.

ABSOLUTE MAXIMUM RATINGS @ 25°C

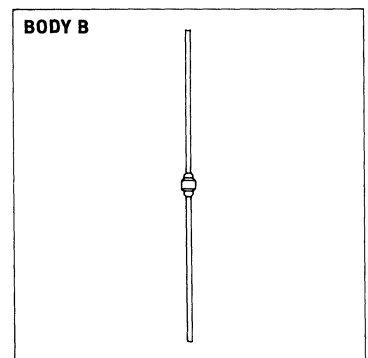
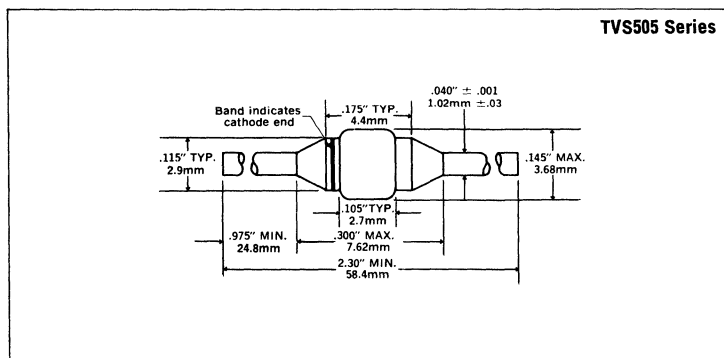
	TVS305-TVS430	TVS505-TVS528
Stand-off Voltage, V _R	5 to 300V	5.0V to 28.0V
Peak Pulse Power (1mS)*	150W	500W
Forward Surge Current (8.3mS half sinewave)	15A	50A
Peak Pulse Current	See Table	See Table
Breakdown Voltage	See Table	See Table
Power, Continuous	3W	5W
Storage and Operating Temperature	-65 to +175°C	-65 to +175°C

*See Figures 3 and 4 for Peak Pulse Power vs Pulse Duration.

MECHANICAL SPECIFICATIONS



MECHANICAL SPECIFICATIONS

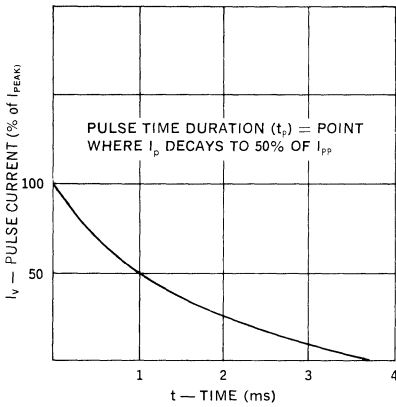


ELECTRICAL SPECIFICATIONS @ 25°C

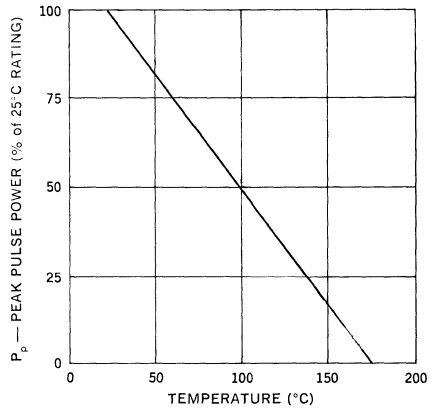
TVS Part No.	Stand-Off Voltage	Min. Breakdown Voltage	Max. Leakage Current	Max. Peak Pulse Current*	Max. Clamping Voltage*	Max. Clamping Voltage*	Max. Clamping Voltage*	
	V_R	$BV_{(min)}$ @ 1mA	I_R @ V_R	I_{PP}	V_C @ I_{PP}	V_C @ 1A	V_C @	
	V	V	μA	A	V	V	5A	10A
TVS305	5.0	6.0	50	17	8.7	—	—	—
TVS310	10.0	11.1	2	8.9	16.8	—	—	—
TVS312	12	13.8	1	7.1	21.0	—	—	—
TVS315	15	16.7	1	5.9	25	—	—	—
TVS318	18	20.4	1	4.9	31	—	—	—
TVS324	24	28.4	1	3.6	42	—	—	—
TVS328	28	30.7	1	3.2	46	—	—	—
TVS348	48	54	1	1.7	82	—	—	—
TVS360	60	67	1	1.4	105	—	—	—
TVS410	100	111	1	.91	160	—	—	—
TVS420	200	234	1	.42	360	—	—	—
TVS430	300	342	1	.28	520	—	—	—
TVS505	5.0	6.0	300	53.7	9.3	7.4	—	7.9
TVS510	10.0	11.1	5	30.3	16.5	13.2	—	14.4
TVS512	12.0	13.8	5	23.8	21.0	16.5	—	18.5
TVS515	15.0	16.7	5	19.8	25.2	19.7	—	22.2
TVS518	18.0	20.4	5	16.3	30.5	23.8	26.0	—
TVS524	24.0	28.4	5	11.9	42.0	32.4	37.0	—
TVS528	28.0	30.7	5	10.7	46.5	35.9	41.0	—

*For 1mS pulse; see Figure 1.

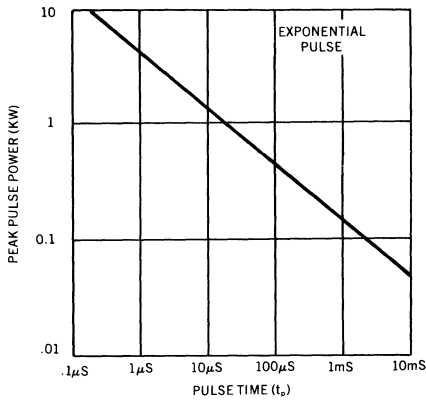
1. Pulse Waveform



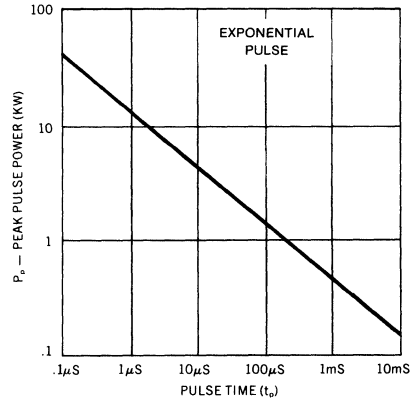
2. Derating Curve



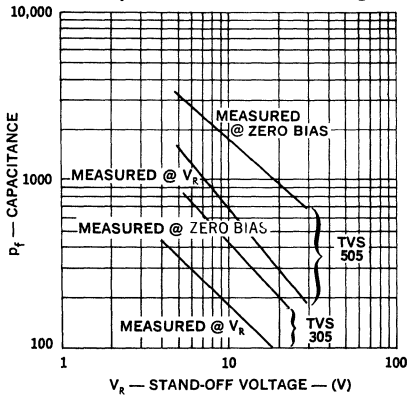
3. Peak Pulse Power vs. Pulse Duration



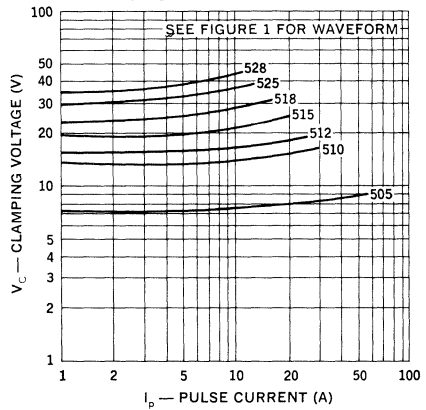
4. Peak Pulse Power vs. Pulse Duration



5. Capacitance vs. Stand-Off Voltage



6. Clamping Voltage vs. Pulse Current



CHOOSING AND SPECIFYING THE PROPER TVS

The following terms are generally used in specifying Transient Voltage Suppressors (TVS):

1. Stand-off Voltage (V_R) is the highest reverse voltage at which the TVS will be non-conducting.
2. Minimum Breakdown Voltage (BV_{min}) is the reverse voltage at which the TVS conducts 1 milli-amp. This is the point where the TVS begins to limit the transient.
3. Maximum Clamping Voltage (V_C max) is the maximum voltage the TVS will allow during a transient "spike."

Figure 7 graphically shows all three terms.

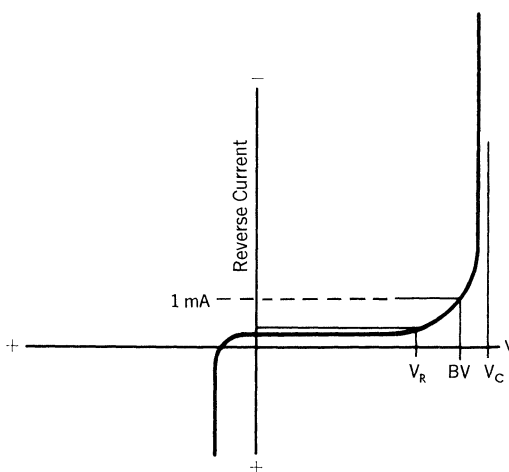


Figure 7

The three most important factors in choosing the appropriate TVS for an application in their order of importance are:

1. Pulse power (P_P) — Choose the TVS series that will handle the Transient Pulse Power. Transient Pulse Power is equal to the clamping voltage (V_C) times the peak pulse current (i_{PP}). The pulse duration vs. pulse power graph on the TVS data sheet can then be used to determine the maximum allowable pulse duration. (Figure 3 or 4).
2. Standoff voltage (V_R) — From the TVS series selected, choose the device with the stand-off voltage equal to or greater than the normal circuit operating voltage.
3. Maximum Clamping Voltage ($V_{C_{MAX}}$) — Determine the clamping voltage of the device chosen for the transient given and be sure it is below the voltage that might damage any components.

For further information see Unitrode Application Note U-79, "Guidelines for Using Transient Voltage Suppressors."

AC POWER ZENERS

1, 3 and 5 Watt Types

UDZ807 SERIES
UDZ5807 SERIES
UDZ8807 SERIES

FEATURES

- Zener Characteristics in Both Directions
- 7.5 to 60V
- High Surge Ratings
- Small Physical Size

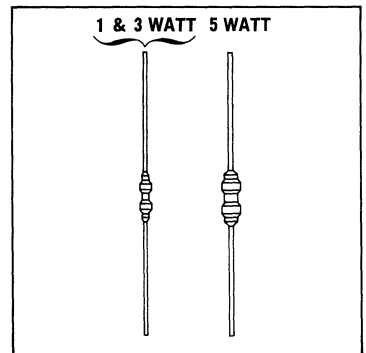
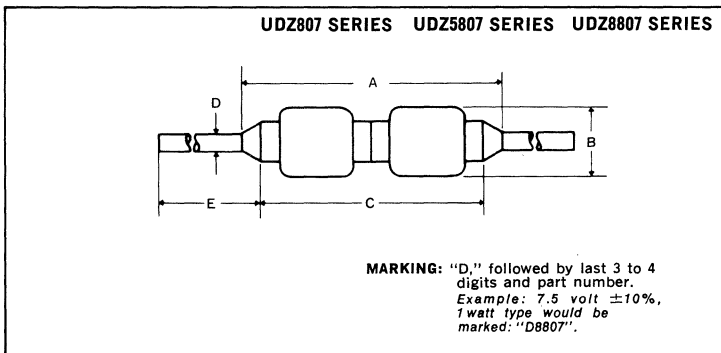
DESCRIPTION

These devices consist of two fused-in-glass zeners brazed cathode to cathode to provide zener action in both directions.

ABSOLUTE MAXIMUM RATINGS

Zener Voltage 7.5 to 60V
 Continuous Current See Tables
 Surge Current (8.3ms) See Tables
 Surge Power See Graph
 Power See Data Sheets for Related Series (UZ8807, UZ807 and UZ5807)
 Storage and Operating Temperature -65°C to +175°C

MECHANICAL SPECIFICATIONS



Dimensions

1 Watt UDZ8807 Series

	ins.	mm
A	450 MAX.	11.43 MAX.
B	.085 MAX.	2.16 MAX.
C	.275 TYP.	6.99 TYP.
D	.028 ± .001	.71 ± .03
E	.700 MIN.	17.78 MIN.

3 Watt UDZ807 Series

	ins.	mm
A	450 MAX.	11.43 MAX.
B	.085 MAX.	2.16 MAX.
C	.275 TYP.	6.99 TYP.
D	.028 ± .001	.71 ± .03
E	.700 MIN.	17.78 MIN.

5 Watt UDZ5807 Series

	ins.	mm
A	500 MAX.	12.70 MAX.
B	.145 MAX.	3.68 MAX.
C	.325 TYP.	8.26 TYP.
D	.040 ± .001	1.02 ± .03
E	.975 MIN.	24.77 MIN.

Type	Electrical Specifications at 25°C						Maximum Ratings**	
	Nominal Zener Voltage † Vz @ IzT	Test Current IzT	Max. Zener Imped § Zz @ IzT	Maximum Leakage @ Reverse Voltage · Current	Reverse Voltage · ±10%	±5%	Maximum Cont. Current IzM	Maximum Surge Current ‡ Is
±10% Tolerance *	Volts	mA	Ohms	µA	Volts	Volts	mA	Amps
1 WATT ZENERS — Specifications apply for both directions.								
UDZ8807	7.5	34	6	50	4.9	5.2	125	5
UDZ8808	8.2	31	7	30	5.4	5.7	115	4.5
UDZ8809	9.1	28	8	10	5.9	6.2	105	3.9
UDZ8810	10	25	8.5	3	6.6	6.9	95	3.37
UDZ8812	12	23	9	1	8.6	9.1	85	2.25
UDZ8815	15	17	14	0.5	10.8	11.4	63	1.65
UDZ8818	18	14	20	0.5	12.9	13.7	52	1.12
UDZ8820	20	12.5	23	0.5	14.4	15.2	47	1.12
UDZ8824	24	10.5	25	0.5	17.3	18.2	40	0.825
UDZ8827	27	9.5	35	0.5	19.4	20.6	35	0.825
UDZ8830	30	8.5	40	0.5	21.6	22.8	31	0.825
UDZ8833	33	7.5	45	0.5	23.7	25.1	28	0.675
UDZ8836	36	7.0	50	0.5	25.9	27.4	26	0.562
UDZ8840	40	6.5	62	0.5	28.8	30.4	24	0.562
UDZ8845	45	6	75	0.5	32.4	34.2	22	0.450
UDZ8860	60	4	125	0.5	43.2	45.6	15	0.337
3 WATT ZENERS — Specifications apply for both directions.								
UDZ807	7.5	75	3	500	4.9	5.2	400	10
UDZ808	8.2	75	4	300	5.4	5.7	360	8
UDZ809	9.1	75	4	200	5.9	6.2	330	7
UDZ810	10	75	5	100	6.6	6.9	300	5
UDZ812	12	65	5	10	8.6	9.1	250	4
UDZ815	15	50	6	10	10.8	11.4	200	3
UDZ818	18	40	8	5	12.9	13.7	170	2
UDZ820	20	40	9	5	14.4	15.2	150	2
UDZ824	24	30	10	5	17.3	18.2	125	1.5
UDZ827	27	25	12	1	19.4	20.6	110	1.5
UDZ830	30	25	15	1	21.6	22.8	100	1.5
UDZ833	33	20	21	1	23.7	25.1	90	1.2
UDZ836	36	20	21	1	25.9	27.4	85	1
UDZ840	40	20	27	1	28.8	30.4	75	1
UDZ845	45	15	37	1	32.4	34.2	65	0.8
UDZ860	60	10	70	1	43.2	45.6	50	0.6



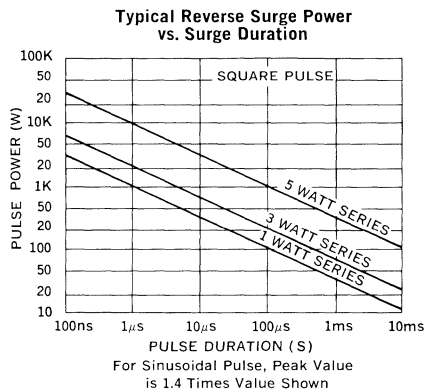
*For ±5% voltage tolerance change the 3rd number from the right from 8 to 7 i.e. UDZ8807 to UDZ8707, etc.

†All zener voltages are measured with an automated test set using a 35ms test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§Zener impedance is derived from the 60-cycle voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

**D.C. Ratings are based on the lead temperature conditions shown in the data sheets covering the UDZ8807, UDZ807, and UDZ5807 series devices. Other conditions will affect the power ratings of all the families except the 1 watt zener family. However, the surge values given apply for any mounting conditions including printed circuit board mounting.

‡Figures shown are for peak sinusoidal surge current of 8.3ms duration using 60 cycle AC. The 8.3ms square pulse rating is 71% of the value shown.



Type	Electrical Specifications at 25°C						Maximum Ratings**	
	Nominal Zener Voltage† V _Z @ I _{ZT}	Test Current I _{ZT}	Max. Zener Imped § Z _Z @ I _{ZT}	Maximum Leakage @ Reverse Voltage Current ±10% ±5%			Maximum Cont. Current I _{ZM}	Maximum Surge Current‡ I _S
±10% Tolerance*	Volts	mA	Ohms	µA	Volts	Volts	mA	Amps
5 WATT ZENERS — Specifications apply for both directions.								
UDZ5807	7.5	175	1.8	500	4.9	5.2	620	40
UDZ5808	8.2	150	1.8	400	5.4	5.7	570	32
UDZ5809	9.1	150	2.5	200	5.9	6.2	510	24
UDZ5810	10	125	2.5	100	6.6	6.9	470	22
UDZ5812	12	100	2.5	50	8.6	9.1	385	18
UDZ5815	15	75	3.5	15	10.8	11.4	300	12
UDZ5818	18	65	4	10	12.9	13.7	255	9
UDZ5820	20	65	4.5	10	14.4	15.2	220	8
UDZ5824	24	50	5	10	17.3	18.2	180	6.5
UDZ5827	27	50	6	10	19.4	20.6	155	6
UDZ5830	30	40	8	10	21.6	22.8	140	5.5
UDZ5833	33	40	10	5	23.7	25.1	130	5
UDZ5836	36	30	11	5	25.9	27.4	120	4.5
UDZ5840	40	30	14	5	28.8	30.4	105	4
UDZ5845	45	30	20	5	32.4	34.2	95	3.5
UDZ5860	60	20	40	5	43.2	45.6	75	2.5

*For ±5% voltage tolerance change the 3rd number from the right from 8 to 7 i.e. UDZ8807 to UDZ8707, etc.

†All zener voltages are measured with an automated test set using a 35ms test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§Zener impedance is derived from the 60-cycle voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

**D.C. Ratings are based on the lead temperature conditions shown in the data sheets covering the UDZ8807, UDZ807, and UDZ5807 series devices. Other conditions will affect the power ratings of all the families except the 1 watt zener family. However, the surge values given apply for any mounting conditions including printed circuit board mounting.

‡Figures shown are for peak sinusoidal surge current of 8.3ms duration using 60 cycle AC. The 8.3ms square pulse rating is 71% of the value shown.

POWER ZENERS

3 Watt

UZ706 SERIES
UZ806 SERIES

FEATURES

- 10 Times Greater Surge Rating than Conventional 1 Watt Types
- Small Physical Size

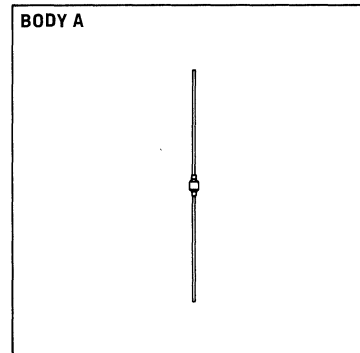
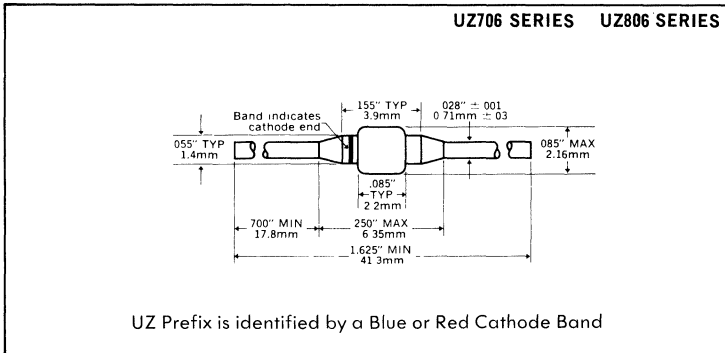
DESCRIPTION

Fused-in-glass metallurgically bonded 3 watt zener diodes.

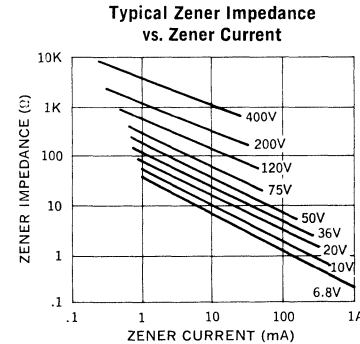
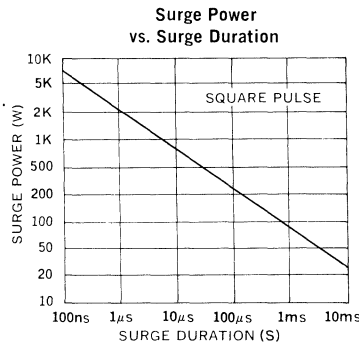
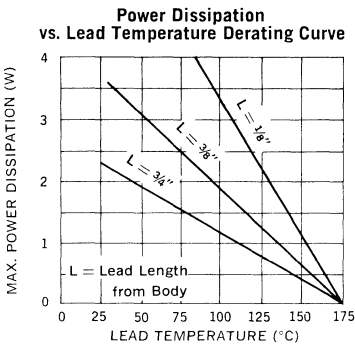
ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z	6.8 to 400V
Continuous Current	See Table
Surge Current (8.3ms)	See Table
Surge Power	See Graph
Power	See Lead Temperature Derating Curve
Storage and Operating Temperature	-65°C to +175°C

MECHANICAL SPECIFICATIONS



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* Type		Electrical Specifications at 25°C							Maximum Ratings	
		Nominal Zener Voltage † $V_Z @ I_{ZT}$	Test Current I_{ZT}	Max. Zener Impedance § $Z_Z @ I_{ZT}$	Maximum Reverse Leakage Current			Typ. Temp. Coefficient $T_C @ I_{ZT}$	Maximum Continuous Current * I_{ZM}	Maximum Surge Current ‡ I_S
					$I_R @ V_R$	± 5% V_R	± 10% V_R			
±5% Tolerance	Jedec** Registration	Volts	mA	Ohms	μA	Volts	Volts	%/°C	mA	Amps
		6.8	75	2	500	5.2	4.9	.04	440	10.0
		7.5	75	2	300	5.7	5.4	.04	400	8.0
		8.2	75	3	200	6.2	5.9	.05	360	7.0
		9.1	75	3	100	6.9	6.6	.05	330	6.0
		10.0	75	4	40	7.6	7.2	.06	300	5.0
		12	65	5	10	9.1	8.6	.07	250	4.0
		13	50	6	10	9.9	9.3	.07	230	4.0
		14	50	6	10	10.6	10.1	.07	210	4.0
		15	50	6	10	11.4	10.8	.07	200	3.0
		16	50	7	5	12.2	11.5	.07	185	3.0
		18	40	8	5	13.7	12.9	.08	170	2.0
		20	40	9	5	15.2	14.4	.08	150	2.0
		22	30	10	5	16.7	15.8	.08	135	2.0
		24	30	10	5	18.2	17.3	.08	125	1.5
		27	25	12	1	20.6	19.4	.09	110	1.5
		30	25	15	1	22.8	21.6	.090	100	1.5
		33	20	21	1	25.1	23.7	.090	90	1.2
		36	20	21	1	27.4	25.9	.090	85	1.0
		40	20	27	1	30.4	28.8	.095	75	1.0
		45	15	37	1	34.2	32.4	.095	65	0.8
		50	15	50	1	38.0	36.0	.095	60	0.8
		56	10	70	1	42.6	40.3	.095	55	0.7
		60	10	70	1	45.7	43.2	.095	50	0.6
		70	10	90	1	53.3	50.5	.095	45	0.6
		75	10	100	1	56.0	54.0	.095	40	0.5
		80	10	115	1	60.8	57.7	.095	35	0.4
		90	8.0	150	1	68.5	64.8	.095	30	0.4
		100	5.0	175	1	76.0	72.0	.100	30	0.4
		110	5.0	250	1	83.6	79.2	.100	25	0.3
		120	5.0	325	1	91.2	86.4	.100	25	0.2
		130	5.0	375	1	98.8	93.6	.100	20	0.20
		140	5.0	550	1	106	101	.100	20	0.20
		150	5.0	650	1	114	108	.100	20	0.20
		160	4.0	700	1	122	115	.100	20	0.15
		170	4.0	750	1	129	122	.100	18	0.15
		180	4.0	850	1	137	129	.100	18	0.10
		190	4.0	900	1	144	137	.100	15	0.10
		200	4.0	950	1	152	144	.100	15	0.10
		220	3.0	1100	1	167	158	.100	15	0.09
		240	3.0	1300	1	182	173	.105	12	0.09
		260	3.0	1500	1	198	187	.105	12	0.08
		280	3.0	1700	1	213	202	.105	10	0.08
		300	3.0	1900	1	228	216	.105	10	0.07
		320	2.0	2100	1	243	230	.105	9	0.07
		340	2.0	2400	1	258	245	.110	9	0.06
		360	2.0	2700	1	274	259	.110	8	0.06
		380	2.0	3000	1	289	274	.110	8	0.06
		400	2.0	3500	1	304	288	.110	7	0.06

* Specify 20% voltage tolerance by changing first numeral of type number from 7 to 9. (UZ709 becomes UZ909) or from 1 to 3 (UZ111 becomes UZ311).

Specify 10% voltage tolerance by changing first numeral of type number from 7 to 8. (UZ709 becomes UZ809) or from 1 to 2 (UZ111 becomes UZ211).

** Jedec registration applies to ±5% tolerance zeners only.

† All zener voltages are measured with an automated test set using a 35 ms test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§ Zener impedance is derived from the 60-cycle AC voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

* Maximum current based on 3 watt rating. See lead temperature derating curves for proper mounting methods.

‡ Figures shown are for a peak sinusoidal surge current of 8.3ms duration using 60 cycle AC. The 8.3ms square pulse rating is 71% of the value shown.

POWER ZENERS

5 Watt, Industrial

UZ4706 SERIES
UZ4806 SERIES

FEATURES

- 2 Times Greater Surge Rating than Plastic Types
- Small Physical Size
- Impervious to Moisture

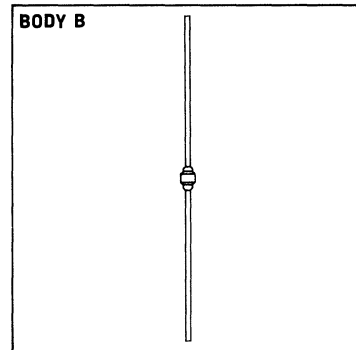
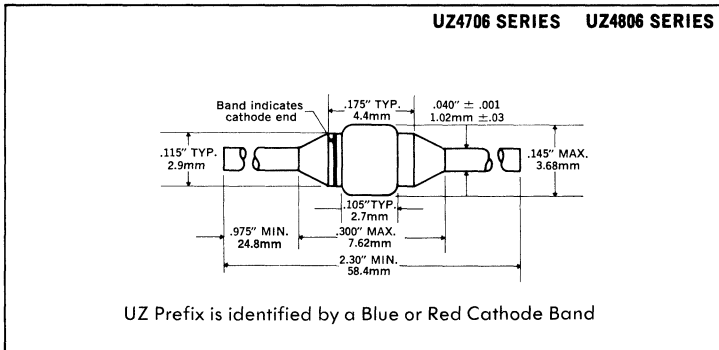
DESCRIPTION

Fused-in-glass 5 watt zeners with the same electrical specs as the 1N5342-1N5388 series.

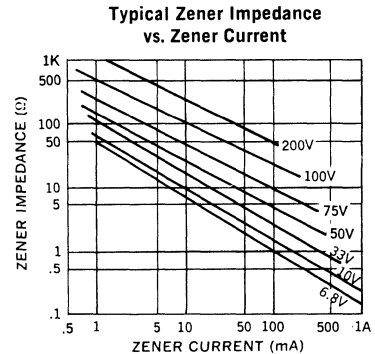
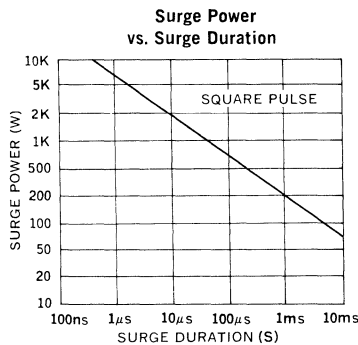
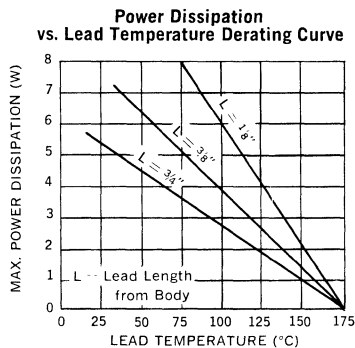
ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z	6.8 to 200V
Continuous Current	See Table
Surge Current (8.3ms)	See Table
Surge Power	See Graph
Power	See Lead Temperature Derating Curve
Storage and Operating Temperature	-65°C to +175°C

MECHANICAL SPECIFICATIONS



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Type		Electrical Specifications at 25°C							Maximum Ratings	
		Nominal Zener Voltage † V _Z @ I _{ZT}	Test Current I _{ZT}	Max. Zener Impedance §		Reverse Voltage			Maximum Cont. Current I _{ZM}	Maximum Surge Current ‡ I _S
				Z _Z @ I _{ZT}	Z _{ZK} @ I _{ZK} = 1mA	Maximum Leakage @ Reverse Voltage Current	Reverse Voltage			
							±10%	±5%		
±5% Tolerance	±10% Tolerance	Volts	mA	Ohms	Ohms	µA	Volts	Volts	mA	Amps
UZ4706	UZ4806	6.8	175	1	1000	500	4.9	5.2	675	32
UZ4707	UZ4807	7.5	175	1.5	800	400	5.4	5.7	620	26.5
UZ4708	UZ4808	8.2	150	1.5	600	200	5.9	6.2	570	19.2
UZ4709	UZ4809	9.1	150	2	400	100	6.6	6.9	510	17.6
UZ4710	UZ4810	10	125	2	125	75	7.2	7.6	470	16
UZ4712	UZ4812	12	100	2.5	140	50	8.6	9.1	385	14.4
UZ4713	UZ4813	13	100	3	145	25	9.3	9.9	350	12.8
UZ4715	UZ4815	15	75	3.5	150	15	10.8	11.4	300	9.6
UZ4716	UZ4816	16	75	3.5	155	10	11.5	12.2	275	8
UZ4718	UZ4818	18	65	4	160	10	12.9	13.7	255	7.2
UZ4720	UZ4820	20	65	4.5	165	10	14.4	15.2	220	6.4
UZ4722	UZ4822	22	50	5	170	10	15.8	16.7	195	5.6
UZ4724	UZ4824	24	50	5	175	10	17.3	18.2	180	5.2
UZ4727	UZ4827	27	50	6	180	10	19.4	20.6	155	4.8
UZ4730	UZ4830	30	40	8	190	10	21.6	22.8	140	4.4
UZ4733	UZ4833	33	40	10	200	5	23.7	25.1	130	4.0
UZ4736	UZ4836	36	30	11	220	5	25.9	27.4	120	3.6
UZ4739	UZ4839	39	30	14	230	5	28.1	29.7	105	3.2
UZ4743	UZ4843	43	30	20	240	5	31	32.7	100	2.8
UZ4747	UZ4847	47	25	25	250	5	33.8	35.8	96	2.6
UZ4751	UZ4851	51	25	27	270	5	36.7	38.8	85	2.4
UZ4756	UZ4856	56	20	35	320	5	40.3	42.6	81	2.2
UZ4762	UZ4862	62	20	42	400	5	44.6	47.1	73	2.0
UZ4768	UZ4868	68	20	50	500	5	49.0	51.7	61	1.8
UZ4775	UZ4875	75	20	55	620	5	54.0	56	60	1.6
UZ4782	UZ4882	82	15	80	720	5	59.0	62.2	55	1.4
UZ4791	UZ4891	91	15	90	760	5	65.5	69.2	50	1.3
UZ4110	UZ4210	100	12	100	800	5	72.0	76.0	45	1.1
UZ4111	UZ4211	110	12	125	1000	5	79.2	83.6	40	1.0
UZ4112	UZ4212	120	10	170	1150	5	86.4	91.2	38	.8
UZ4113	UZ4213	130	10	190	1250	5	93.6	98.8	35	.64
UZ4115	UZ4215	150	8	330	1500	5	108	114.0	31	.60
UZ4116	UZ4216	160	8	350	1650	5	115	121.6	30	.56
UZ4118	UZ4218	180	5	450	1750	5	129	136.8	25	.48
UZ4120	UZ4220	200	5	500	1850	5	144	152.0	22	.40

Maximum V_r @ 1.0 Amp = 1.2 Volts for all types

†All zener voltages are measured with an automated test set using a 35 ms test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§Zener impedance is derived from the 60-cycle voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

‡Figures shown are for peak sinusoidal surge current of 8.3 ms duration using 60 cycle AC. The 8.3ms square pulse rating is 71% of the value shown.

POWER ZENERS

5 Watt

UZ5706 SERIES
UZ5806 SERIES

FEATURES

- 2 Times Greater Surge Rating than Conventional 10 Watt Zeners
- Small Physical Size

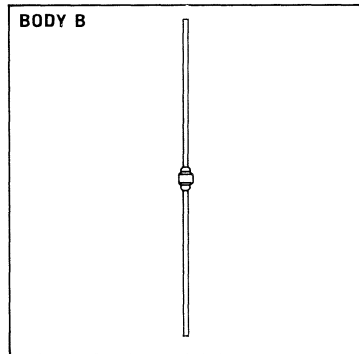
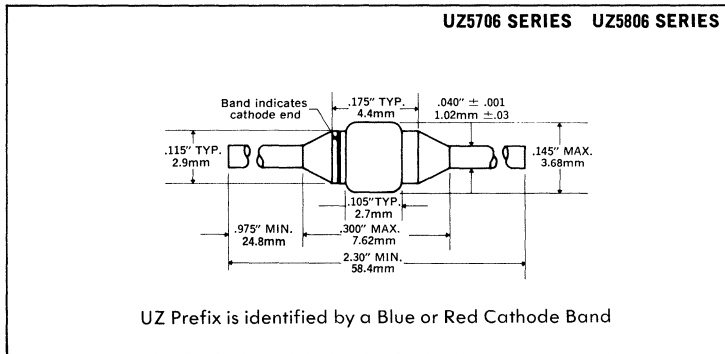
DESCRIPTION

Fused-in-glass, metallurgically-bonded 5 watt zeners.

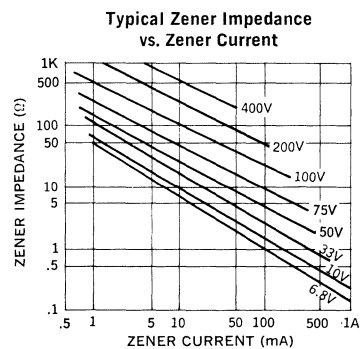
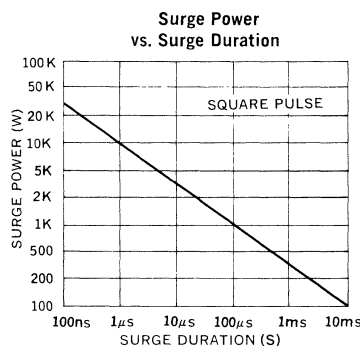
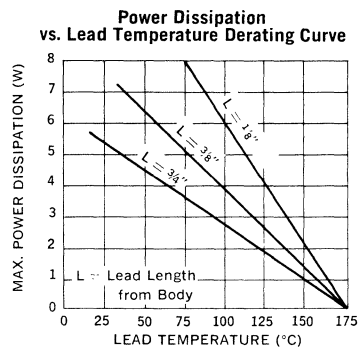
ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z	6.8 to 400V
Continuous Current	See Table
Surge Current (8.3ms)	See Table
Surge Power	See Graph
Power	See Lead Temperature Derating Curve
Storage and Operating Temperature	-65°C to +175°C

MECHANICAL SPECIFICATIONS



9



Type *		Electrical Specifications at 25°C							Maximum Ratings	
		Nominal Zener Voltage † V _Z @ I _{ZT}	Test Current I _{ZT}	Max. Zener Impedance § Z ₂ @ I _{ZT}	Maximum Reverse Leakage Current			Typ. Temp. Coeff. T _C @ I _{ZT}	Maximum Continuous Current * I _{ZM}	Maximum Surge Current ‡ I _S
					I _R	± 5% V _R	± 10% V _R			
±5% Tolerance	±10% Tolerance	Volts	mA	Ohms	µA	Volts	Volts	%/°C	mA	Amps
UZ5706	UZ5806	6.8	175	1.0	500	5.2	4.9	.05	675	40
UZ5707	UZ5807	7.5	175	1.5	400	5.7	5.4	.06	620	32
UZ5708	UZ5808	8.2	150	1.5	200	6.2	5.9	.06	570	24
UZ5709	UZ5809	9.1	150	2.0	100	6.9	6.6	.06	510	20
UZ5710	UZ5810	10.0	125	2.0	75	7.6	7.2	.07	470	20
UZ5712	UZ5812	12	100	2.5	50	9.1	8.6	.07	385	18
UZ5713	UZ5813	13	100	3.0	25	9.9	9.3	.08	350	16
UZ5714	UZ5814	14	100	3.0	20	10.6	10.1	.08	320	14
UZ5715	UZ5815	15	75	3.5	15	11.4	10.8	.08	300	12
UZ5716	UZ5816	16	75	3.5	10	12.2	11.5	.08	275	10
UZ5718	UZ5818	18	65	4.0	10	13.7	12.9	.085	255	9.0
UZ5720	UZ5820	20	65	4.5	10	15.2	14.4	.085	220	8.0
UZ5722	UZ5822	22	50	5.0	10	16.7	15.8	.085	195	7.0
UZ5724	UZ5824	24	50	5.0	10	18.2	17.3	.090	180	6.5
UZ5727	UZ5827	27	50	6.0	10	20.6	19.4	.090	155	6.0
UZ5730	UZ5830	30	40	8	10	22.8	21.6	.09	140	5.5
UZ5733	UZ5833	33	40	10	5	25.1	23.7	.09	130	5.0
UZ5736	UZ5836	36	30	11	5	27.4	25.9	.095	120	4.5
UZ5740	UZ5840	40	30	14	5	30.4	28.8	.095	105	4.0
UZ5745	UZ5845	45	30	20	5	34.2	32.4	.095	95	3.5
UZ5750	UZ5850	50	25	25	5	38.0	36.0	.095	85	3.0
UZ5756	UZ5856	56	20	35	5	42.6	40.3	.095	80	2.8
UZ5760	UZ5860	60	20	40	5	45.7	43.2	.100	75	2.5
UZ5770	UZ5870	70	20	50	5	53.3	50.5	.100	65	2.3
UZ5775	UZ5875	75	15	55	5	56.0	54.0	.100	60	2.0
UZ5780	UZ5880	80	15	80	5	60.8	57.7	.100	55	1.8
UZ5790	UZ5890	90	15	90	5	68.5	64.8	.100	50	1.6
UZ5110	UZ5210	100	10	100	5	76.0	72.0	.100	45	1.4
UZ5111	UZ5211	110	10	125	5	83.6	79.2	.100	40	1.2
UZ5112	UZ5212	120	10	170	5	91.2	86.4	.100	38	1.0
UZ5113	UZ5213	130	10	190	5	98.8	93.6	.105	35	0.80
UZ5114	UZ5214	140	8	230	5	106.0	101.0	.105	33	0.80
UZ5115	UZ5215	150	8	330	5	114.0	108.0	.105	31	0.75
UZ5116	UZ5216	160	8	350	5	122.0	115.0	.105	30	0.70
UZ5117	UZ5217	170	8	380	5	129.0	122.0	.105	27	0.65
UZ5118	UZ5218	180	5	450	5	137	129	.110	25	0.60
UZ5119	UZ5219	190	5	470	5	144	137	.110	24	0.55
UZ5120	UZ5220	200	5	500	5	152	144	.110	22	0.50
UZ5122	UZ5222	220	5	550	5	167	158	.115	20	0.45
UZ5124	UZ5224	240	5	650	5	182	173	.115	18	0.40
UZ5126	UZ5226	260	5	750	5	198	187	.120	17	0.35
UZ5128	UZ5228	280	4	850	5	213	202	.120	16	0.30
UZ5130	UZ5230	300	4	950	5	228	216	.120	15	0.25
UZ5132	UZ5232	320	4	1100	5	243	230	.120	14	0.24
UZ5134	UZ5234	340	4	1200	5	258	245	.120	13	0.23
UZ5136	UZ5236	360	3	1400	5	274	259	.120	12	0.22
UZ5138	UZ5238	380	3	1500	5	289	274	.120	12	0.21
UZ5140	UZ5240	400	3	1800	5	304	288	.120	11	0.20

Temperature Range: Operating and Storage -65°C to +175°C.

* Specify 20% tolerance by changing the second numeral of type number from 8 to 9 (UZ5809 becomes UZ5909) or from 2 to 3 (UZ5211 becomes UZ5311).

† All zener voltages are measured with an automated test set using a 35 millisecond test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§ Zener impedance is derived from the 60-cycle AC voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

* Maximum current based on 5 watt rating. See lead temperature derating curves for proper mounting methods.

‡ Figures shown are for a peak sinusoidal surge current of 8.3ms duration using 60 cycle AC. The 8.3ms square pulse rating is 71% of the value shown.

Several of the above types now have JEDEC 1N type numbers. The following cross-reference table lists the appropriate 1N numbers; specifications are same as above.

JEDEC #	UNITRODE TYPE	JEDEC #	UNITRODE TYPE	JEDEC #	UNITRODE TYPE
1N5118	UZ5714	1N5124	UZ5780	1N5130	UZ5128
1N5119	UZ5740	1N5125	UZ5790	1N5131	UZ5132
1N5120	UZ5745	1N5126	UZ5114	1N5132	UZ5134
1N5121	UZ5750	1N5127	UZ5117	1N5133	UZ5138
1N5122	UZ5760	1N5128	UZ5119	1N5134	UZ5140
1N5123	UZ5770	1N5129	UZ5126		

POWER ZENERS

6 Watt, Military, 10 Watt Military

UZ7706L and UZ7806L SERIES
UZ7706 and UZ7806 SERIES

FEATURES

- High Surge Rating
- Small Physical Size
- Leaded and Stud Packages Available

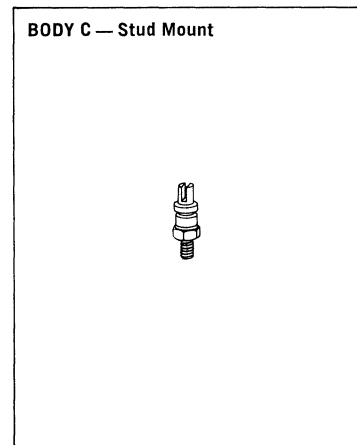
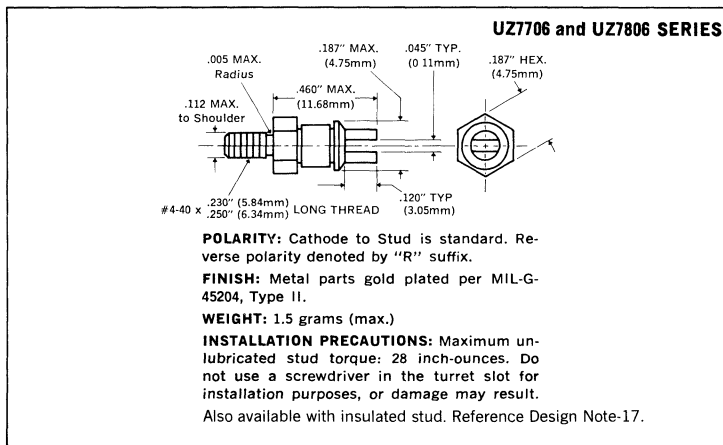
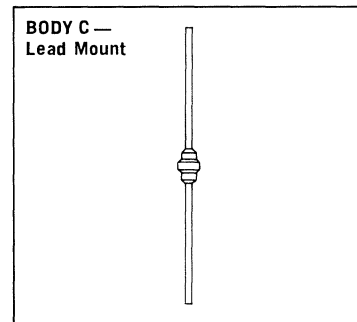
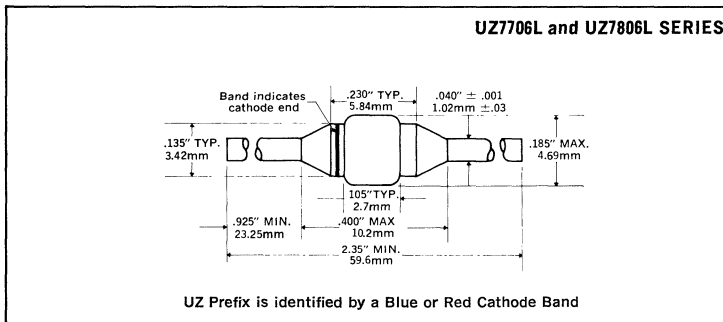
DESCRIPTION

Fused-in-glass, metallurgically bonded
6 watt leaded zeners and 10 watt
stud-type zeners.

ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z	6.8 to 100V
Continuous Current	See Table
Surge Current (8.3ms)	See Table
Surge Power	See Graph
Power	UZ7706L & UZ7806L See Lead Temperature Derating Curve
	UZ7706 & UZ7806 @100°C Case 10W
Storage and Operating Temperature	-65°C to +175°C

MECHANICAL SPECIFICATIONS



Type *		Electrical Specifications at 25°C							Maximum Ratings	
		Nominal Zener Voltage † $V_Z @ I_{ZT}$	Test Current I_{ZT}	Max. Zener Impedance § $Z_Z @ I_{ZT}$	Maximum Reverse Leakage Current			Typ. Temp. Coeff. $T_C @ I_{ZT}$	Maximum Continuous Current ★ I_{ZM}	Maximum Surge Current ‡ I_S
					$I_R @ V_R$	$\pm 5\% V_R$	$\pm 10\% V_R$			
$\pm 5\%$ Tolerance	$\pm 10\%$ Tolerance	Volts	mA	Ohms	μA	Volts	Volts	%/°C	mA	Amps
UZ7706	UZ7806	6.8	350	0.6	1000	5.2	4.9	.04	1350	50
UZ7707	UZ7807	7.5	325	0.7	800	5.7	5.4	.04	1250	41
UZ7708	UZ7808	8.2	300	0.8	200	6.2	5.9	.05	1150	31
UZ7709	UZ7809	9.1	275	1.0	150	6.9	6.6	.05	1020	29
UZ7710	UZ7810	10.0	250	1.0	100	7.6	7.2	.06	950	26
UZ7712	UZ7812	12	200	1.3	75	9.1	8.6	.07	770	23
UZ7713	UZ7813	13	200	1.5	50	9.9	9.3	.07	700	21
UZ7714	UZ7814	14	175	1.5	40	10.6	10.1	.07	640	20
UZ7715	UZ7815	15	150	2.0	30	11.4	10.8	.07	600	17
UZ7716	UZ7816	16	150	2.5	20	12.2	11.5	.07	550	15
UZ7718	UZ7818	18	130	3.5	20	13.7	12.9	.08	500	13
UZ7720	UZ7820	20	120	4.0	20	15.2	14.4	.08	440	12
UZ7722	UZ7822	22	100	4.5	20	16.7	15.8	.08	390	11
UZ7724	UZ7824	24	100	5.0	20	18.2	17.3	.08	360	10
UZ7727	UZ7827	27	90	6.0	20	20.6	19.4	.09	310	9
UZ7730	UZ7830	30	80	8	20	22.8	21.6	.090	280	8.5
UZ7733	UZ7833	33	70	10	10	25.1	23.7	.090	260	7.5
UZ7736	UZ7836	36	60	12	10	27.4	25.9	.090	240	7.0
UZ7740	UZ7840	40	60	15	10	30.4	28.8	.095	210	6.4
UZ7745	UZ7845	45	50	20	10	34.2	32.4	.095	180	5.5
UZ7750	UZ7850	50	50	22	10	38.0	36.0	.095	170	4.6
UZ7756	UZ7856	56	40	30	10	42.6	40.3	.095	160	4.1
UZ7760	UZ7860	60	40	35	10	45.6	43.2	.095	150	3.7
UZ7770	UZ7870	70	35	40	10	53.2	50.4	.095	130	3.3
UZ7775	UZ7875	75	30	45	10	56.0	54.0	.095	120	3.1
UZ7780	UZ7880	80	30	60	10	60.8	57.6	.095	110	2.9
UZ7790	UZ7890	90	25	75	10	68.4	64.8	.095	100	2.6
UZ7710	UZ7210	100	20	90	10	76.0	72.0	.100	90	2.3

Power Rating: Stud Mounted: 10 Watts at 100°C Case derate linearly to zero at 175°C Case.
Lead Mounted: See lead temperature derating curve.
Temperature Range: Operating and storage -65°C to 175°C.

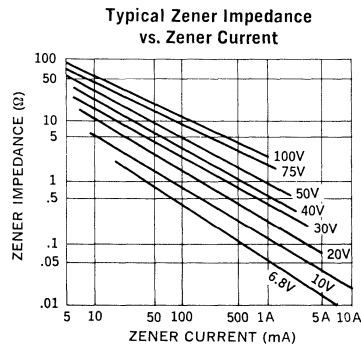
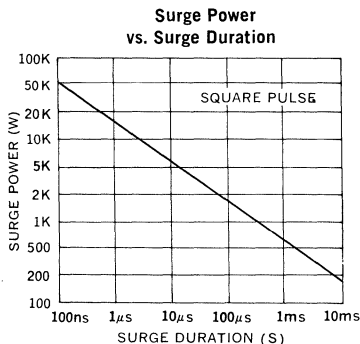
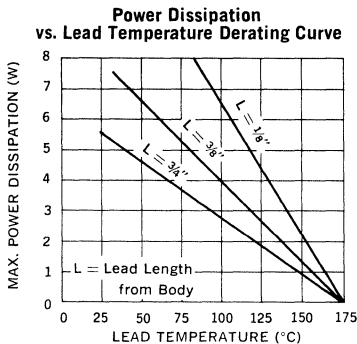
* Specify 20% tolerance by changing the second numeral of type number from 8 to 9 (UZ7809 becomes UZ7909) or from 2 to 3 (UZ7210 becomes UZ7310). Specify leaded version by adding an L suffix (UZ7809 becomes UZ7809L).

† All zener voltages are measured with an automated test set using a 35 msec test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§ Zener impedance is derived from the 60-cycle voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.

★ Ratings Based on 100°C Case temperature; for leaded devices multiply by 0.6.

‡ Figures shown are for a peak sinusoidal surge current of 8.3ms duration, non-repetitive. The 8.3ms square pulse rating is 71% of the value shown



POWER ZENERS

1 Watt, Industrial

UZ8706 SERIES
UZ8806 SERIES

FEATURES

- High Surge Ratings
- A Quarter the Size of Conventional 1 Watt Zeners
- Impervious to Moisture

DESCRIPTION

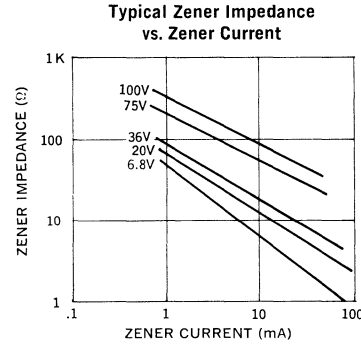
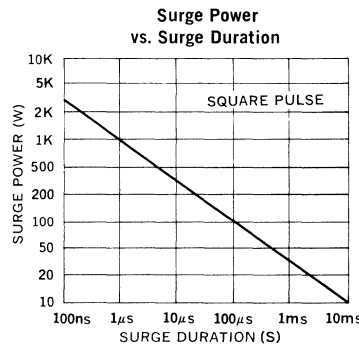
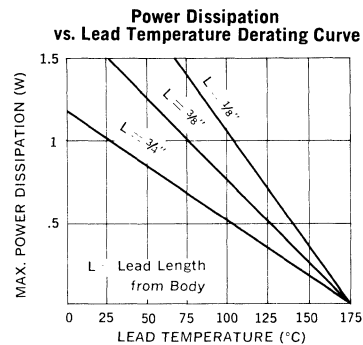
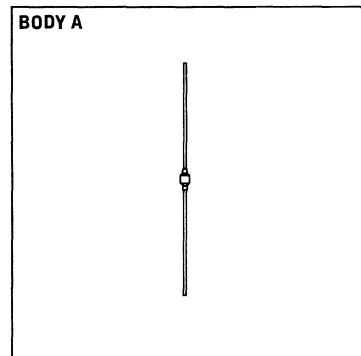
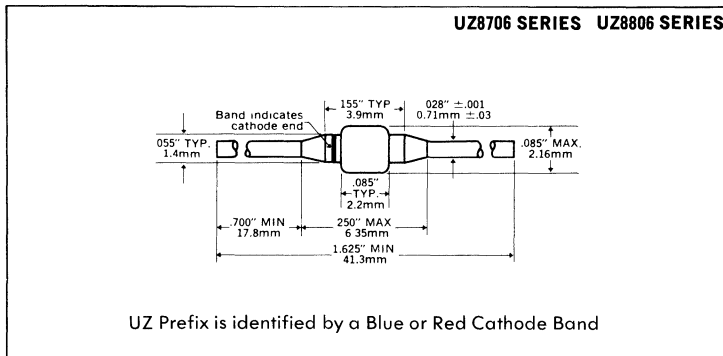
One watt zener diodes, hermetically sealed in glass.

ABSOLUTE MAXIMUM RATINGS

Zener Voltage, V_z 6.8 to 200V
 Continuous Current See Table
 Surge Current (8.3ms) See Table
 Surge Power See Graph
 Power See Lead Temperature Derating Curve
 Storage and Operating Temperature -65°C to $+175^{\circ}\text{C}$

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MECHANICAL SPECIFICATIONS



Type		Electrical Specifications at 25°C							Maximum Ratings	
		Nominal Zener Voltage † V _Z @ I _{ZT}	Test Current I _{ZT}	Max. Zener Impedance § Z _Z @ I _{ZT}	Maximum Reverse Leakage Current			Typ. Temp. Coefficient T.C. @ I _{ZT}	Maximum Continuous Current * I _{ZM}	Maximum Surge Current ‡ I _S
					I _R @ V _R μA	± 5% V _R Volts	± 10% V _R Volts			
± 5% Tolerance	± 10% Tolerance	Volts	mA	Ohms	μA	Volts	Volts	%/°C	mA	Amps
UZ 8706	UZ 8806	6.8	37	3.5	50	5.2	4.9	0.04	140	5.00
UZ 8707	UZ 8807	7.5	34	4.0	30	5.7	5.4	0.04	125	4.50
UZ 8708	UZ 8808	8.2	31	4.5	10	6.2	5.9	0.05	115	3.90
UZ 8709	UZ 8809	9.1	28	5.0	3.0	6.9	6.6	0.05	105	3.37
UZ 8710	UZ 8810	10	25	7.0	2.0	7.6	7.2	0.06	95	2.77
UZ 8712	UZ 8812	12	23	9.0	1.0	9.1	8.6	0.07	85	2.25
UZ 8713	UZ 8813	13	21	10	0.5	9.9	9.3	0.07	80	2.25
UZ 8714	UZ 8814	14	19	12	0.5	10.6	10.1	0.07	74	2.25
UZ 8715	UZ 8815	15	17	14	0.5	11.4	10.8	0.07	63	1.65
UZ 8716	UZ 8816	16	15.5	16	0.5	12.1	11.5	0.07	60	1.65
UZ 8718	UZ 8818	18	14.0	20	0.5	13.7	12.9	0.08	52	1.12
UZ 8720	UZ 8820	20	12.5	22	0.5	15.2	14.4	0.08	47	1.12
UZ 8722	UZ 8820	22	11.5	23	0.5	16.7	15.8	0.08	43	1.12
UZ 8724	UZ 8824	24	10.5	25	0.5	18.2	17.3	0.08	40	0.825
UZ 8727	UZ 8827	27	9.5	35	0.5	20.5	19.4	0.09	35	0.825
UZ 8730	UZ 8830	30	8.5	40	0.5	22.8	21.6	0.09	31	0.825
UZ 8733	UZ 8833	33	7.5	45	0.5	25.1	23.7	0.09	28	0.675
UZ 8736	UZ 8836	36	7.0	50	0.5	27.3	25.9	0.09	26	0.562
UZ 8740	UZ 8840	40	6.5	62	0.5	30.4	28.8	0.095	24	0.562
UZ 8745	UZ 8845	45	6.0	75	0.5	34.2	32.4	0.095	22	0.450
UZ 8750	UZ 8850	50	5.0	85	0.5	38.0	36.0	0.095	20	0.450
UZ 8756	UZ 8856	56	4.5	110	0.5	42.5	40.3	0.095	17	0.390
UZ 8760	UZ 8860	60	4.0	125	0.5	45.6	43.2	0.095	15	0.337
UZ 8770	UZ 8870	70	3.7	150	0.5	53.2	50.4	0.095	14	0.337
UZ 8775	UZ 8875	75	3.3	175	0.5	57.0	54.0	0.095	12	0.277
UZ 8780	UZ 8880	80	3.0	200	0.5	60.8	57.6	0.095	11	0.225
UZ 8790	UZ 8890	90	2.8	250	0.5	68.4	64.8	0.095	10	0.225
UZ 8110	UZ 8210	100	2.5	350	0.5	76.0	72.0	0.10	9.5	0.225
UZ 8111	UZ 8211	110	2.3	450	0.5	83.6	79.2	0.10	8.5	0.165
UZ 8112	UZ 8212	120	2.0	550	0.5	91.2	86.4	0.10	8.0	0.112
UZ 8113	UZ 8213	130	1.9	700	0.5	98.8	93.6	0.10	7.2	0.112
UZ 8114	UZ 8214	140	1.8	850	0.5	106	100	0.10	6.8	0.112
UZ 8115	UZ 8215	150	1.7	1000	0.5	114	108	0.10	6.3	0.112
UZ 8116	UZ 8216	160	1.6	1100	0.5	121	115	0.10	5.9	0.082
UZ 8117	UZ 8217	170	1.5	1200	0.5	129	122	0.10	5.6	0.082
UZ 8118	UZ 8218	180	1.4	1300	0.5	137	129	0.10	5.2	0.056
UZ 8119	UZ 8219	190	1.3	1400	0.5	144	137	0.10	5.0	0.056
UZ 8120	UZ 8220	200	1.2	1500	0.5	152	144	0.10	4.7	0.056

†All zener voltages are measured with an automated test set using a 35 millisecond test time. Longer or shorter test times will have a corresponding effect on the measured value due to heating effects.

§Zener impedance is derived from the 60-cycle AC voltage created when AC current with RMS value of 10% of DC zener test current is superimposed on the test current.




*Ratings are based on free air. T_A is 25°C. For use at 1.5 watts see derating curve.

‡Figures shown are for a peak sinusoidal surge current of 8.3 ms duration using 60 cycle AC. The 8.3 ms square pulse rating is 71% of the value shown.

THYRISTORS (SCRs, PUTs) 10

THYRISTORS (SCRs & PUTs)

PRODUCT SELECTION GUIDE

 TO-18	SCR	V_{DRM} (V)	$I_{T(RMS)}$.5A					
			30		2N3027*	2N3030*	ID100	
			60	AA114	2N3028*	2N3031*	ID101	
			100		2N3029*	2N3032*	ID102	
			150				ID103	
			200	AA116			ID104	
			300	AA110			ID105	
			400	AA111			ID106	
					I_{GT}	200 μ A	200 μ A	200 μ A
		I_H	2mA	5mA	5mA			
 TO-9	SCR	V_{DRM} (V)	$I_{T(RMS)}$ 1.25A					
			30		2N1876	2N1870A**		
			60		2N1877	2N1871A**		
			100		2N1878	2N1872A**		
			150		2N1879	2N1873A		
			200		2N1880	2N1874A**		
					I_{GT}	20 μ A	200 μ A	
					I_H	3mA	5mA	
 TO-39	SCR	V_{DRM} (V)	$I_{T(RMS)}$ 1.6A					
			30			2N2322		
			60	AD100	2N2323A***	2N2323***	ID200	
			100	AD101	2N2324A***	2N2324***	ID201	
			150		2N2325A	2N2325	ID202	
			200	AD102	2N2326A***	2N2326***	ID203	
			300	AD103	2N2328A***	2N2328***	ID300	
			400	AD104		2N2329***	ID301	
					I_{GT}	2 μ A	20 μ A	200 μ A
					I_H	2mA	2mA	3mA

*Available as JAN and JANTX types.

**Available as JAN type.

***Available as JAN, JANTX, JANTXV types.

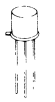
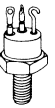
†3mA available from factory

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THYRISTORS (SCRs & PUTs)

PRODUCT SELECTION GUIDE


ULTRAFAST SWITCHING

 TO-18	SCR	V_{DRM} (V)	$I_{T(RMS)}$.4A			
			60V	GA200	GA300	GA200A	GA300A
			100V	GA201	GA301	GA201A	GA301A
			t_{on}	20ns (TYP.)			
			t_q	2.0 μ S			
 TO-59	SCR	V_{DRM} (V)	$I_{T(RMS)}$.6A			
			60V	GB200	GB300	GB200A	GB300A
			100V	GB201	GB301	GB201A	GB301A
			t_{on}	20ns (TYP.)			
			t_q	2.0 μ S			

RADIATION HARDENED SCRs

 TO-18	On-State Current $I_{T(RMS)}$		0.4A
	Package Style		TO-18
	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM} , and REVERSE VOLTAGE, V_{RRM}	30V	GA100
		60V	GA101
		80V	GA102
Key Parameters		I_{GT} (Post 3X10 ¹⁴ NVT) 20mA	
		I_{H} (Post 3X10 ¹⁴ NVT) 30mA	

PUTs — PROGRAMMABLE UNIJUNCTION TRANSISTORS

 TO-18	Peak Recurrent Forward Current		.8A	
	Package Style		TO-18	
	MIN. VALLEY CURRENT, I_V MAX. PEAK POINT CURRENT, I_P	$I_V \equiv 25\mu A @ R_G \equiv 10K$ $I_P \equiv .15\mu A @ R_G \equiv 1Meg$	U13T2	CONSULT FACTORY
		$I_V \equiv 70\mu A @ R_G \equiv 10K$ $I_P \equiv 2\mu A @ R_G \equiv 1Meg$	U13T1	
		$I_V \equiv 1mA @ R_G \equiv 200\Omega$ $I_P \equiv .15\mu A @ R_G \equiv 1Meg$	2N6120	
		$I_V \equiv 1.5mA @ R_G \equiv 200\Omega$ $I_P \equiv 2\mu A @ R_G \equiv 1Meg$	2N6119 2N6137*	
Forward and Reverse Voltage; V_{AKI} , V_{AKR}		40V	100V	

* Available as JAN and JANTX types.

SCRs

1.25 Amp, Planar

2N1870A-2N1874A

FEATURES

- Available as Either "JAN" or Standard Types
- Operating D.C. Current Range: 5 to 1250mA
- Pulse Currents: to 30A
- Voltage Ratings: to 200V
- Maximum Trigger Current: 0.2mA
- Maximum Trigger Voltage: 0.8V
- All Leads Isolated from Case
- Maximum θ_{J-C} : 20°C/W

DESCRIPTION

These are premium PNP controlled switches intended for use in applications requiring a high degree of reliability assurance. The JAN types are specified under MIL-S-19500/198, and are included in MIL-STD-701 as recommended types for military usage.

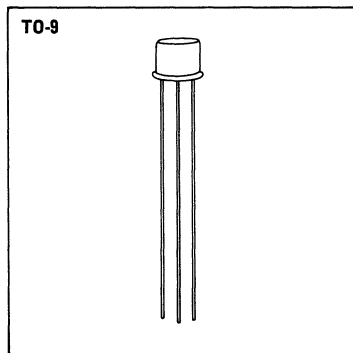
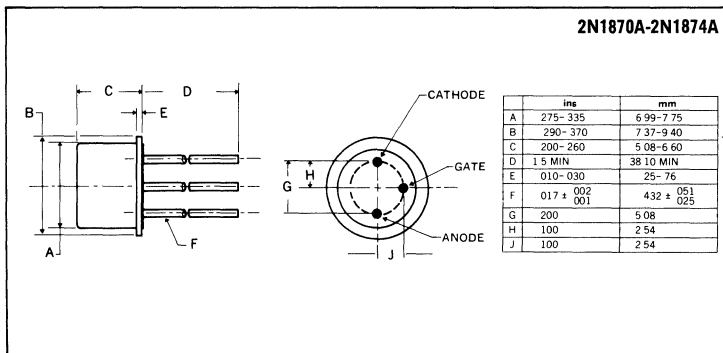
This series is useful in a wide variety of applications including: safety, arming and detonating circuits; timing and programming circuits; protective and warning circuits; driving relays; driving indicator lamps, encoding and decoding circuits; replacing relays, thyatrons, and magamps; servo motor control; pulse generation; plus many others.

ABSOLUTE MAXIMUM RATINGS

	2N1870A JAN2N1870A	2N1871A JAN2N1871A	2N1872A JAN2N1872A	2N1873A	2N1874A JAN2N1874A
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	100V	150V	200V
Repetitive Peak Reverse Voltage, V_{RRM}	30V	60V	100V	150V	200V
D.C. On-State Current, I_T					
100°C Ambient			250mA		
100°C Case			1.25A		
Repetitive Peak On-State Current, I_{TRM}			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}			15A		
Peak Gate Current, I_{GM}			250mA		
Average Gate Current, $I_{G(AV)}$			25mA		
Reverse Gate Voltage, V_{GR}			5V		
Thermal Resistance, Junction to Case, $R\theta_{J-C}$			20°C/W		
Operating and Storage Temperature Range			-65°C to +150°C		

10

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

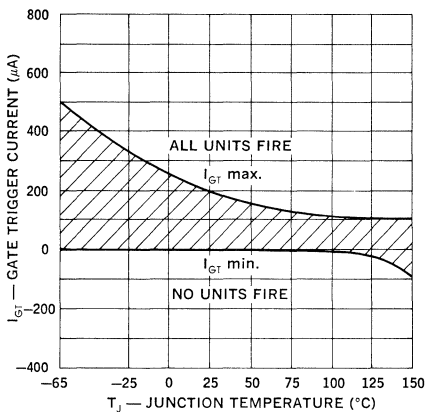
Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Subgroup 1 (Visual and Mechanical)						
Subgroup 2 (25°C Tests)						
Off-State Current	I_{DRM}	—	0.5	10	μA	$R_{GK} = 1K, V_{DRM} = + \text{ Rating}$
Reverse Current	I_{RRM}	—	0.5	10	μA	$R_{GK} = 1K, V_{RRM} = - \text{ Rating}$
Gate Trigger Voltage	V_{GT}	0.4	0.55	0.8	V	$R_{GS} = 100 \text{ ohms}, V_D = 5V$
Gate Trigger Current	I_{GT}	—	30	200	μA	$R_{GS} > 10K \text{ ohms}, V_D = 5V$
On-State Voltage	V_{TM}	—	1.8	2.5	V	$I_{TM} = 2A \text{ (pulse test)}$
Off-State Voltage — Critical of Rise	dv_c/dt	100	—	—	V/ μs	Specified test circuit
Reverse Gate Current	I_{GR}	—	0.5	10	μA	$V_{GRM} = 5V, \text{ anode open}$
Holding Current	I_H	0.3	—	5.0	mA	$I_G = -150\mu A, V_D = 5V$
Subgroup 3 (125°C Tests)						
High Temp. Off-State Current	I_{DRM}	—	15	100	μA	$R_{GK} = 1K, V_{DRM} = + \text{ Rating}$
High Temp. Reverse Current	I_{RRM}	—	15	100	μA	$R_{GK} = 1K, V_{RRM} = - \text{ Rating}$
High Temp. Gate Non-Trigger Voltage	V_{GD}	0.2	—	—	V	$R_{GS} = 100 \text{ ohms}, V_D = 5V$
High Temp. Holding Current	I_H	0.2	—	—	mA	$I_G = -150\mu A, V_D = 5V$
Subgroup 4 (−65°C Tests)						
Low Temp. Gate Trigger Voltage	V_{GT}	—	—	1.0	V	$R_{GK} = 100 \text{ ohms}, V_D = 5V$
Low Temp. Gate Trigger Current	I_{GT}	—	—	500	μA	$R_{GK} > 10K \text{ ohms}, V_D = 5V$
Low Temp. Holding Current	I_H	—	—	15	mA	$I_G = -150\mu A, V_{AA} = 5V$

†All values in this table are JEDEC registered.

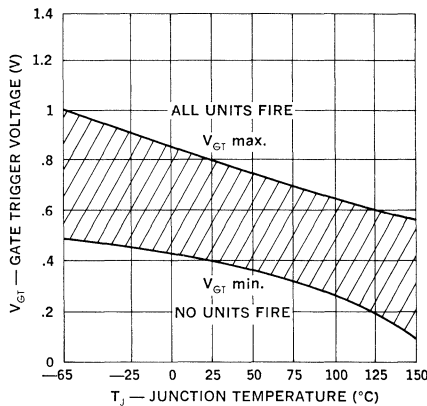
Note: Voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1 K or smaller, or other adequate gate bias is used.

Triggering and Bias Stabilization

1. Gate Trigger Current

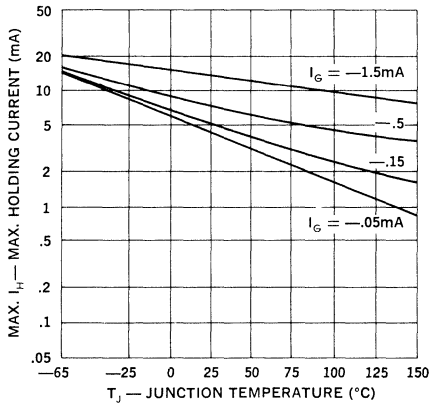


2. Gate Trigger Voltage

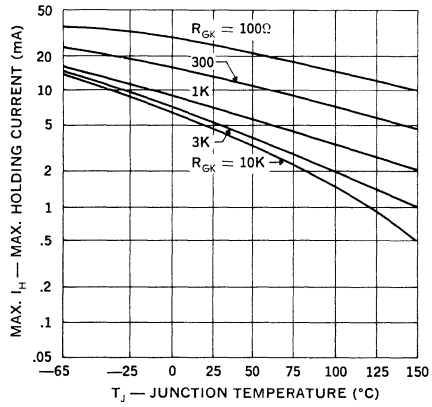


Holding Current

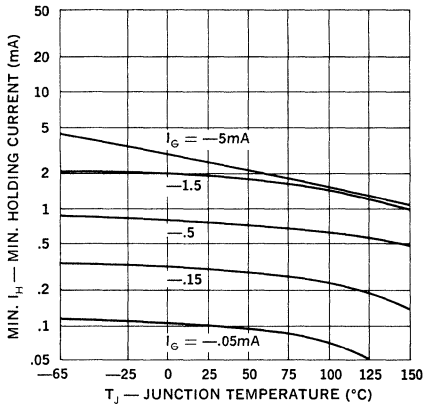
1. Max. Holding Current (Current Bias)



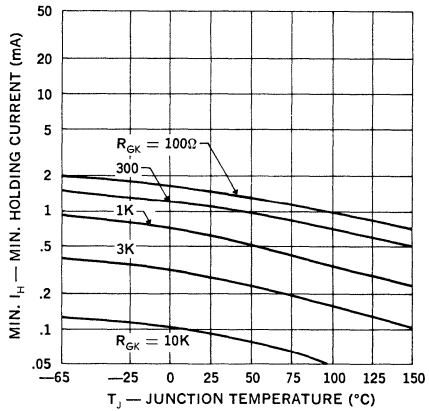
2. Max. Holding Current (Resistor Bias)



3. Min. Holding Current (Current Bias)



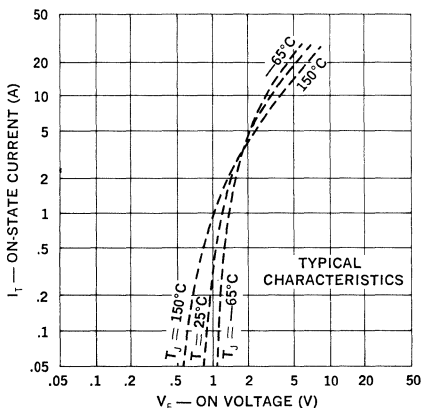
4. Min. Holding Current (Resistor Bias)



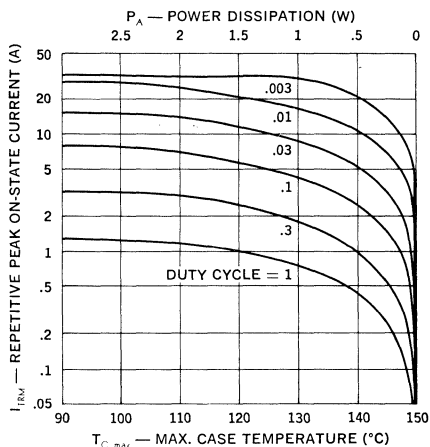
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Current Ratings — Thermal Design

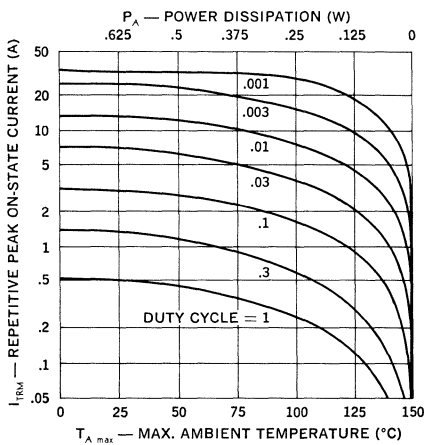
1. On-State Current vs. Voltage



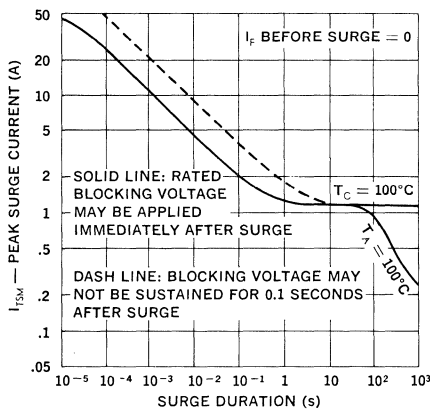
2. Peak Current vs. Case Temperature



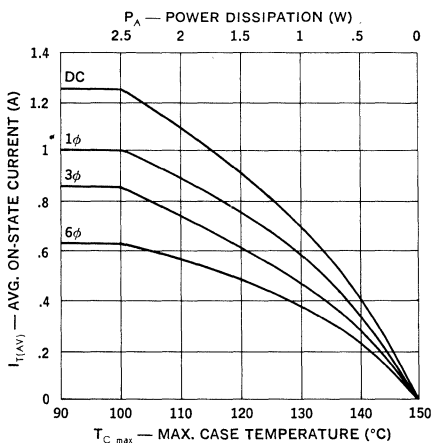
3. Peak Current vs. Ambient Temperature



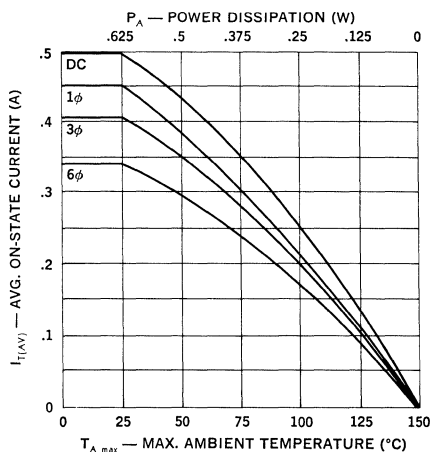
4. Surge Current vs. Time



5. Average Current vs. Case Temperature



6. Average Current vs. Ambient Temperature



SCRs

2N1875-2N1880

1.25 Amp, Planar

FEATURES

- Operating D.C. Current Range: 10-1250mA
- Peak Pulse Current: to 30A
- Maximum Gate Current to Fire: 20 μ A
- Firing Voltage: .52 \pm .08V
- Voltage Ratings: to 200V
- "Turn-on" Time: Typically 0.1 μ s
- Low On Voltage: 2.5V Maximum at 2A

DESCRIPTION

This high sensitivity series, featuring very precise control of triggering characteristics, is particularly useful for timing and time delay circuits, voltage limit detectors, high gain static switching, logic circuits, pulse and sweep generators, and related applications.

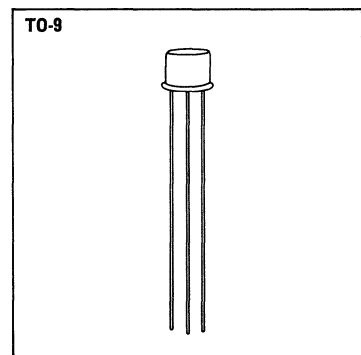
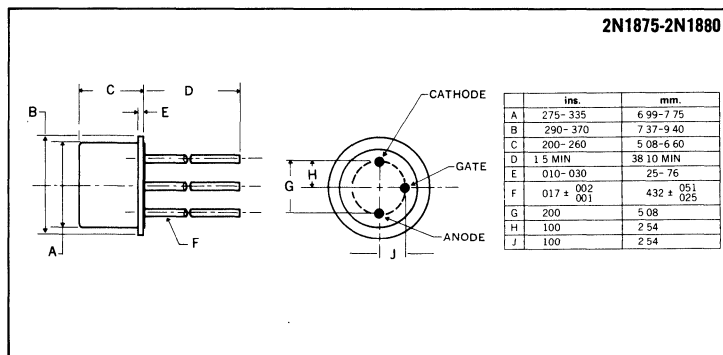
This series is available in a TO-9 package, with all leads isolated from the case, providing a maximum thermal resistance of 20°C/Watt between junction and case.

ABSOLUTE MAXIMUM RATINGS

	2N1875	2N1876	2N1877	2N1878	2N1879	2N1880
Repetitive Peak Off-State Voltage, V_{DRM}	15V	30V	60V	100V	150V	200V
Repetitive Peak Reverse Voltage, V_{RRM}	15V	30V	60V	100V	150V	200V
D.C. On-State Current, I_T						
100°C Ambient						250mA
100°C Case						1.25A
Repetitive Peak On-State Current, I_{TRM}						up to 30A
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}						15A
Peak Gate Current, I_{GM}						250mA
Average Gate Current, $I_{G(AV)}$						25mA
Reverse Gate Voltage, V_{GR}						.5V
Thermal Resistance, Junction to Case, $R\theta_{J-C}$						20°C/W
Operating and Storage Temperature Range						-65°C to +150°C

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MECHANICAL SPECIFICATIONS



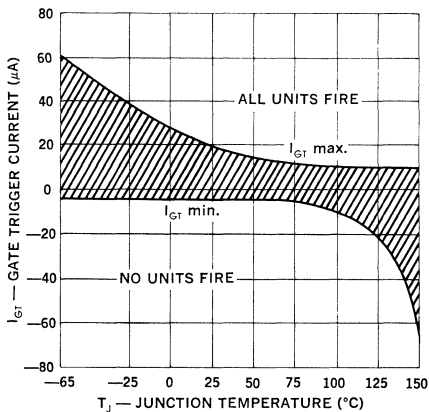
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Subgroup 1 (Visual and Mechanical)						
Subgroup 2 (25°C Tests)						
Off-State Current	I_{DRM}	—	0.5	5	μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K$
Reverse Current	I_{RRM}	—	0.5	10	μA	$V_{RRM} = \text{Rating}$
Reverse Gate Current	I_{GR}	—	0.5	10	μA	$V_{GR} = 2V$
Gate Trigger Current	I_{GT}	—	5	20	μA	$V_D = 5V, R_{GS} = 10K$
Gate Trigger Voltage	V_{GT}	.44	.52	.60	V	$V_D = 5V, R_{GS} = 100\Omega$
Anode Trigger Current (Note 2)	I_{AT}	—	100	—	μA	$V_D = 5V$
On-State Voltage	V_T	0.8	1.8	2.5	V	$I_T = 2A$ (Pulse Test)
Holding Current	I_H	0.3	1.0	3	mA	$I_G = -150\mu A, V_{AA} = 5V$
Subgroup 3 (25°C Tests)						
Turn-on Time	t_{on}	—	0.1	—	μS	$I_G = 20mA$ $I_T = .5A$ $V_D = 30V$ $I_T = .5A, i_R = .5A, R_{GK} = 1K$
Turn-off Time	t_{off}	—	0.5	—	μS	
Gate Trigger — on Pulse Width	$t_{pg(on)}$	—	0.5	—	μS	
Circuit Commutated Turn-off Time	t_q	—	10	—	μS	
Subgroup 4 (125°C Tests)						
High Temp. Off-State Current	I_{DRM}	—	5	20	μA	$V_D = \text{Rating}, R_{GK} = 1K$
High Temp. Reverse Current	I_{RRM}	—	15	100	μA	$V_{RRM} = \text{Rating}$

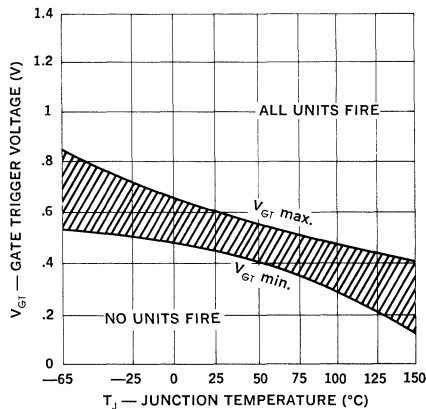
Note 1: Voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used.
2: For a maximum limit of 50 μA , use suffix "—1" and drop "2N". Example: 1877-1.
 † All values in this table are JEDEC registered.

TRIGGERING AND BIAS STABILIZATION

1. Gate Trigger Current



2. Gate Trigger Voltage



SCRs

1 Amp, Planar

2N1881-2N1885

FEATURES

- One Cycle Surge Current: 15A
- Voltage Ratings: to 200V
- Low "On-Voltage": 2V Max. at 1A
- Operation: to 150°C Junction Temperature
- All Leads Isolated for Design Flexibility

DESCRIPTION

These types are useful in AC and DC static switching, proportioning control, relay and thyatron replacement, DC to AC converters, servo motor driving, protective circuits, and related applications.

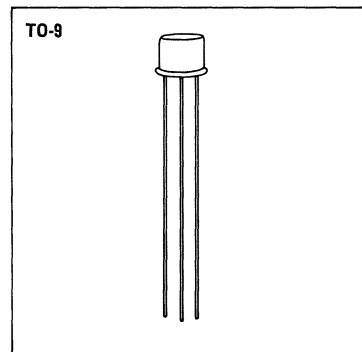
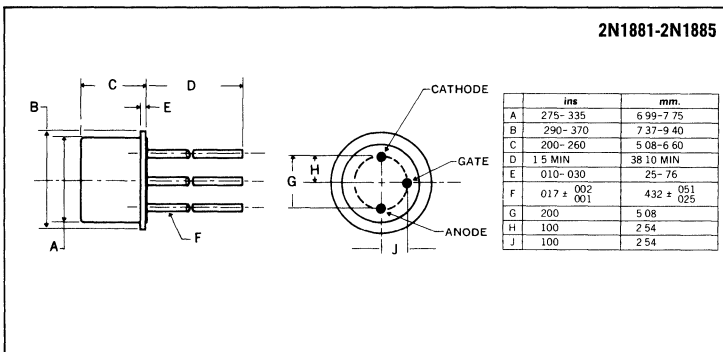
This series is available in a TO-9 package, with all leads isolated from the case, providing a maximum thermal resistance of 20°C/Watt between junction and case.

ABSOLUTE MAXIMUM RATINGS

	2N1881	2N1882	2N1883	2N1884	2N1885
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	100V	150V	200V
Repetitive Peak Reverse Voltage, V_{RRM}	30V	60V	100V	150V	200V
D.C. On-State Current, I_T					
100°C Ambient			250mA		
100°C Case			1.0A		
Repetitive Peak On-State Current, I_{TRM}			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}			15A		
Peak Gate Current, I_{GM}			250mA		
Average Gate Current $I_{G(AV)}$			25mA		
Reverse Gate Voltage, V_{GR}			3V		
Thermal Resistance, Junction to Case, $R_{\theta J-C}$			20°C/W		
Operating and Storage Temperature Range			-65°C to +150°C		

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MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Subgroup 1 (Visual and Mechanical)						
Subgroup 2 (25°C Tests)						
Off-State Current	I_{DRM}	—	0.5	10	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	0.5	10	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Current	I_{GR}	—	0.5	10	μA	$V_{GRM} = 2V$
Gate Trigger Current	I_{GT}	—	0.2	2	mA	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	V_{GT}	0.40	1	2	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	V_T	—	1.5	2	V	$I_T = 1A$ (pulse test)
Holding Current	I_H	—	2	—	mA	$I_G = -150\mu A, V_D = 5V$
Anode Trigger Current	I_{AT}	—	0.5	—	mA	$R_{GS} = 10K, V_D = 5V$
Subgroup 3 (25°C Tests)						
Turn-on Time	t_{on}	—	0.2	—	μS	$I_G = 20mA, I_T = 0.5A, V_D = 30V$
Gate Trigger — on Pulse Width	$t_{pg}(\text{on})$	—	1	—	μS	$I_G = 20mA, I_T = 0.5A, V_D = 30V$
Turn-off Time	t_{off}	—	1	—	μS	$I_T = 1A, I_R = 1A, R_{GK} = 1K$
Circuit Commutated Turn-off Time	t_q	—	10	—	μS	$I_T = 1A, I_R = 1A, R_{GK} = 1K$
Subgroup 3 (125°C Tests)						
High Temp. Off-State Current	I_{DRM}	—	15	200	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	I_{RRM}	—	15	200	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$

† All values in this table are JEDEC registered.

Note: Voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used.

SCRs

1.6 Amp, Planar

2N2322-2N2329
 2N2323A-2N2328A
 2N2323S-2N2329S, J, JTX, JTXV
 2N2323AS-2N2328AS, J, JTX, JTXV

FEATURES

- Available as JAN, JANTX, & JANTXV Types
- JAN Types Available in TO-5
- 1.6A D.C. Current
- Peak Currents: to 30A
- Voltage Ratings: to 400V
- 20 μ A Max. Trigger Current ("A" types)
- 0.6V Max. Trigger Voltage ("A" types)

DESCRIPTION

These are premium thyristor switches intended for use in high performance industrial, military and space applications requiring a high degree of reliability assurance. This series is useful in a wide variety of applications including timing and programming circuits, protective and warning circuits, driving relays, driving indicator lamps, encoding and decoding circuits, replacing relays, thyratrons, and magamps, servo motor control, pulse generation, plus many others. The high surge current rating (15A - 1 cycle) makes this series particularly useful for squib firing.

The following JAN, JANTX and JANTXV types are specified under Mil-S-19500/276A and are included in Mil-STD-701 as recommended types for military usage:

ABSOLUTE MAXIMUM RATINGS

	2N2323 JAN2N2323S JANTX2N2323S JANTXV2N2323S	2N2324 JAN2N2324S JANTX2N2324S JANTXV2N2324S	2N2326 JAN2N2326S JANTX2N2326S JANTXV2N2326S	2N2328 JAN2N2328S JANTX2N2328S JANTXV2N2328S	2N2329 JAN2N2329S JANTX2N2329S JANTXV2N2329S			
Repetitive Peak Off-State Voltage, V_{DRM}	25V	50V	100V	150V	200V	250V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	25V	50V	100V	150V	200V	250V	300V	400V
Non-Repetitive Peak Reverse Voltage, V_{RSM} (< 5ms)	40V	75V	150V	225V	300V	350V	400V	500V
D.C. On-State Current, I_T					300mA			
					80°C Ambient			
					85°C Case			
One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}					1.6A			
Repetitive Peak On-State Current, I_{TM}					15A			
Gate Power Dissipation, P_{GM}					0.1W			
Gate Power Dissipation, $P_{GM(AV)}$					0.01W			
Peak Gate Current, I_{GM}					100mA			
Peak Gate Voltage, Forward and Reverse					6V			
Reverse Gate Current, I_{GR}					3mA			
Storage Temperature Range					-65°C to +150°C			
Operating Temperature Range					-65°C to +125°C			

MECHANICAL SPECIFICATIONS

2N2322-2N2329 2N2323S-2N2328S, J, JTX, JTXV
 2N2323A-2N2328A 2N2323AS-2N2328AS, J, JTX, JTXV

	INCHES	MILLIMETERS
A	.315-.335	8.00-8.51
B	.350-.370	8.89-9.39
C	.240-.260	6.35-6.60
D	.010-.030	0.25-0.76
E	.5 MIN	12.70 MIN
F	.016-.019	.406-.483
G	.190-.210	4.83-5.33
H	.085-.105	2.16-2.67
J	.028-.034	.711-.864
K	.029-.045	.737-1.14
L	.100	2.54

TO-205AD (TO-39)

10

ELECTRICAL SPECIFICATIONS

Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Visual and Mechanical						MIL-STD-750, Method 2071
25°C						
Off-State Current	I_{DRM}	—	0.1	10	μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Reverse Current	I_{RRM}	—	0.1	10	μA	$V_{RRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Gate Trigger Current	I_{GT}	—	2	20	μA	$V_D = 6V, R_L = 100\Omega$
"A" Types		—	50	200	μA	$V_D = 6V, R_L = 100\Omega$
non-"A" Types						
Gate Trigger Voltage	V_{GT}	0.35	0.52	0.60	V	$V_D = 6V, R_{GK} = 2K, R_L = 100\Omega$
"A" Types		0.35	0.55	0.80	V	$V_D = 6V, R_{GK} = 1K, R_L = 100\Omega$
non-"A" Types						
On-State Voltage	V_{TM}	—	2.0	2.2	V	$I_{TM} = 4A$ (pulse test)
Holding Current	I_H	—	0.3	2.0	mA	$V_D = 6V, R_{GK} = 1K$ (2K for "A" Types)
Reverse Gate Current	I_{GR}	—	1	200*	μA	$V_{GR} = 6V$
Delay Time	t_d	—	0.6	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	t_r	—	0.4	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-Off Time	t_q	—	20	—	μs	$I_T = 1A, I_R = 1A, R_{GK} = 1K$
125°C						
Off-State Current	I_{DRM}	—	1	100	μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Reverse Current	I_{RRM}	—	1	100	μA	$V_{RRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Gate Trigger Voltage	V_{GT}	0.1	0.3	—	V	$V_D = \text{Rated } V_D, R_{GK} = 1K$ (2K for "A" Types)
Holding Current	I_H	0.1†	—	—	mA	$V_D = 6V, R_{GK} = 2K$
"A" Types		0.15†	—	—	mA	$V_D = 6V, R_{GK} = 1K$
non-"A" Types						
Off-State Voltage — Critical Rate of Rise	dv/dt	0.7*	—	—	V/ μs	$V_D = \text{Rating}, R_{GK} = 2K$
"A" Types		1.8*	—	—	V/ μs	$V_D = \text{Rating}, R_{GK} = 1K$
non-"A" Types						
–65°C						
Off-State Current	I_{DRM}	—	.05	5.0*	μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Reverse Current	I_{RRM}	—	.05	5.0*	μA	$V_{RRM} = \text{Rating}, R_{GK} = 1K$ (2K for "A" Types)
Gate Trigger Current	I_{GT}	—	50	75	μA	$V_D = 6V, R_L = 100\Omega$
"A" Types		—	100	350	μA	$V_D = 6V, R_L = 100\Omega$
non-"A" Types						
Gate Trigger Voltage	V_{GT}	—	0.7	0.8*	V	$V_D = 6V, R_{GK} = 2K, R_L = 100\Omega$
"A" Types		—	0.75	0.9†	V	$V_D = 6V, R_{GK} = 2K, R_L = 100\Omega$
non-"A" Types		—	1.0	1.0	V	$V_D = 6V, R_{GK} = 1K, R_L = 100\Omega$
Holding Current	I_H	—	—	3.0†	mA	$V_D = 6V, R_{GK} = 1K$ (2K for "A" Types)

* JAN and JANTX Types only.
 † Industrial Types only.

JAN and JANTX Acceptance Tests

100% Screening TX-Types

High Temperature Storage
 Temperature Cycling
 Constant Acceleration
 Fine & Gross Hermetic Seal
 Electrical Test
 Burn-in
 Electrical Test

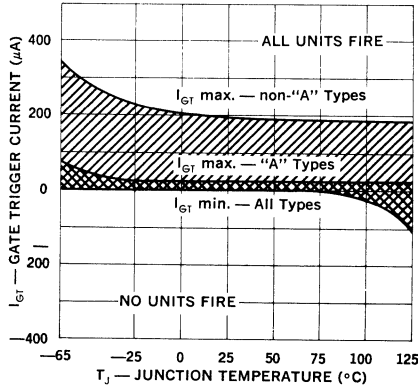
Group B Tests

Subgroup 1 — Reverse Gate Current
 Surge Current
 Non-Repetitive Reverse Voltage
 Subgroup 2 — Low Temp. Reverse Blocking Current
 Low Temp. Forward Blocking Current
 Low Temp. Gate Trigger Voltage
 Low Temp. Gate Trigger Current
 Subgroup 3 — Temperature Cycling
 Thermal Shock
 Moisture Resistance
 Solderability
 Subgroup 4 — Blocking Life Test

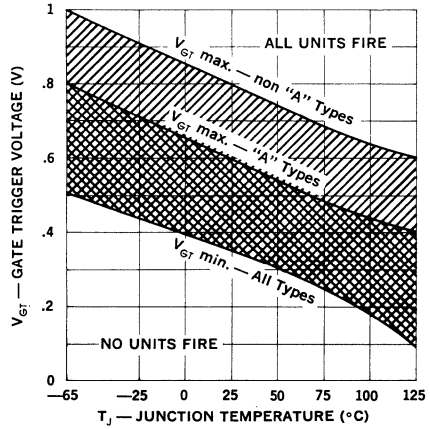
Group C Tests

Subgroup 1 — Physical Dimensions
 Subgroup 2 — Shock
 Constant Acceleration
 Vibration, Variable Frequency
 Subgroup 3 — Barometric Pressure, Reduced
 Subgroup 4 — Salt Atmosphere
 Subgroup 5 — Terminal Strength
 Subgroup 6 — Intermittent Operating Life Test

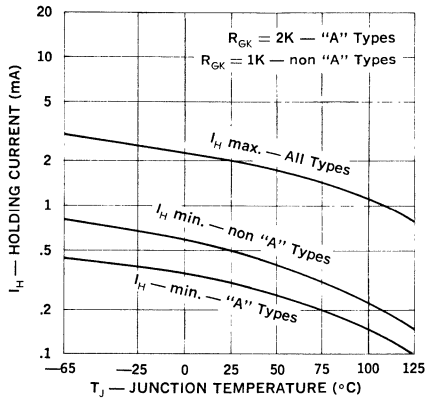
Gate Trigger Current



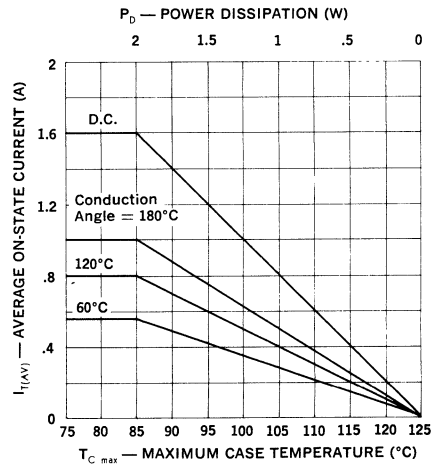
Gate Trigger Voltage



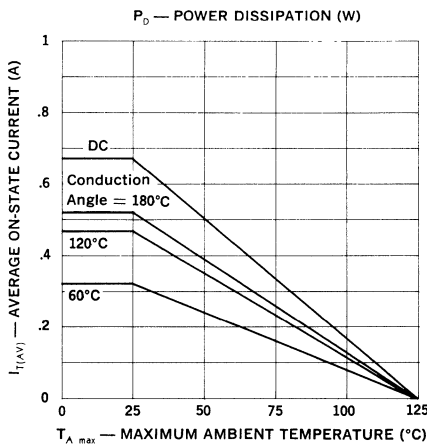
Holding Current



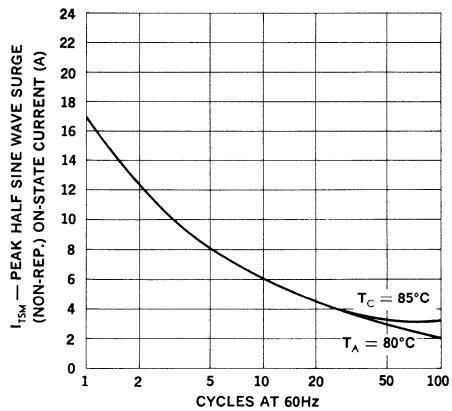
Average Current vs. Case Temperature



Average Current vs. Ambient Temperature



Surge Current



10

SCRs

0.5 Amp, Planar

JAN & JANTX 2N3027-2N3032

FEATURES

- JAN and JANTX Types Available
- Fully Characterized for "Worst Case" Design
- Passivated Planar Construction for Maximum Reliability and Parameter Uniformity
- Low On-State Voltage and Fast Switching at High Current Levels
- Typical Turn-On Time: 0.12 μ s
- Typical Recovery Time: 0.7 μ s
- Pulse Currents: to 30A

DESCRIPTION

The 2N3027 series of planar SCRs (controlled switches) are intended for use in military and space applications requiring a high degree of reliability. They offer a unique combination of extremely fast switching, precise triggering, high pulse power, small size, intrinsic parameter stability, and high radiation tolerance.

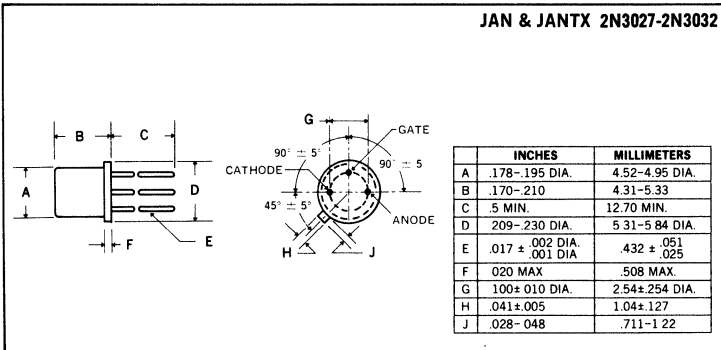
The JAN and JANTX types are specified under MIL-S-19500/419, and are included in MIL-STD-701 as recommended types for military usage.

ABSOLUTE MAXIMUM RATINGS

	JAN & JANTX 2N3027 JAN & JANTX 2N3030	JAN & JANTX 2N3028 JAN & JANTX 2N3031	JAN & JANTX 2N3029 JAN & JANTX 2N3032
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	100V
Repetitive Peak Reverse Voltage, V_{RRM}	30V	60V	100V
D.C. On-State Current, I_T			
100°C Case		500mA	
75°C Ambient		250mA	
Repetitive Peak On-State Current, I_{TRM}		30A	
Surge (Non-Rep.) On-State Current, I_{TSM}			
50ms		5A	
8ms		8A	
Peak Gate Current, I_{GM}		250mA	
Average Gate Current, $I_{G(AV)}$		25mA	
Reverse Gate Voltage		5V	
Reverse Gate Current		3mA	
Storage Temperature Range		-65°C to +20°C	
Operating Temperature Range		-65°C to +150°C	

Note: Blocking voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used. (See section on bias stabilization.)

MECHANICAL SPECIFICATIONS



TO-18



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)
2N3027 — 2N3028 — 2N3029

Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1						
Visual and Mechanical	—	—	—	—	—	MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)						
Off-State Current	I_{DRM}	—	.002	0.1	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	.002	0.1	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	V_{GR}	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	I_{GT}	-5	8	200	μA	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	V_{GT}	.40	.55	.80	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	V_T	0.8	1.2	1.5	V	$i_T = 1A \text{ (pulse test)}$
Holding Current	I_H	0.3	0.7	5.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 3 (25°C Tests)						
Off-State Voltage — Critical Rate of Rise	dv_c/dt	30	60	—	$v/\mu s$	$R_{GK} = 1K, V_D = 30V$
Gate Trigger-on Pulse Width	$t_{pg(ON)}$	—	.07	0.2	μs	$I_G = 10mA, I_T = 1A, V_{DM} = 30V$
Delay Time	t_d	—	.08	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	t_r	—	.04	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	0.7	2.0	μs	$I_T = 1A, i_R = 1A, R_{GK} = 1K$
SUBGROUP 4 (150°C Tests)						
High Temp. Off-State Current	I_{DRM}	—	2	20	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	I_{RRM}	—	20	50	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	V_{GT}	.10	.15	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	I_H	.05	.20	1.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 5 (-65°C Tests)						
Low Temp. Gate Trigger Voltage	V_{GT}	0.6	0.75	1.1	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	I_{GT}	0	150	1.2	mA	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	I_H	0.5	3.5	10	mA	$R_{GK} = 1K, V_D = 5V$

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)
2N3030 — 2N3031 — 2N3032

Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1						
Visual and Mechanical	—	—	—	—	—	MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)						
Off-State Current	I_{DRM}	—	.002	0.1	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	.002	0.1	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	V_{GR}	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	I_{GT}	-5	8	20	μA	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	V_{GT}	0.44	0.6	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	V_T	0.8	1.2	1.5	V	$i_T = 1A \text{ (pulse test)}$
Holding Current	I_H	0.3	1.0	4.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 3 (25°C Tests)						
Off-State Voltage — Critical Rate of Rise	dv_c/dt	30	60	—	$v/\mu s$	$R_{GK} = 1K, V_D = 30V$
Gate Trigger-on Pulse Width	$t_{pg(ON)}$	—	.05	0.1	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Delay Time	t_d	—	0.1	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	t_r	—	.05	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	0.7	2.0	μs	$I_T = 1A, i_R = 1A, R_{GK} = 1K$
SUBGROUP 4 (150°C Tests)						
High Temp. Off-State Current	I_{DRM}	—	2	20	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	I_{RRM}	—	20	50	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	V_{GT}	.10	.15	0.4	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	I_H	.05	.30	2.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 5 (-65°C Tests)						
Low Temp. Gate Trigger Voltage	V_{GT}	0.44	0.8	0.95	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	I_{GT}	0	0.4	0.5	mA	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	I_H	0.5	5.0	8	mA	$R_{GK} = 1K, V_D = 5V$

10

High Reliability Processing

The 2N3027-2N3032 series provides a complete range of high reliability processing from the standard devices that undergo extensive electrical testing, through JAN and JANTX levels. 100% processing, Group B, and Group C tests for JAN and JANTX devices is shown below. For further details, see MIL-S-19500/419(EL).

100% Screening TX-Types

- High Temperature Storage
- Temperature Cycling
- Constant Acceleration
- Fine & Gross Hermetic Seal
- Electrical Test
- Burn-in
- Electrical Test

Group B Tests

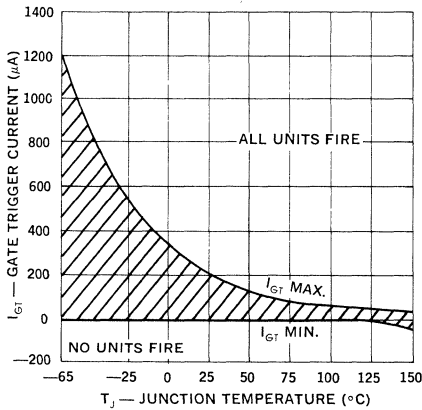
- Subgroup 1 — Physical Dimensions
- Subgroup 2 — Solderability
- Temperature Cycling
- Thermal Shock
- Constant Acceleration
- Moisture Resistance
- Subgroup 3 — Surge Current
- Subgroup 4 — Blocking Life Test
- Subgroup 5 — Storage Life Test
- Subgroup 6 — Operating Life Test

Group C Tests

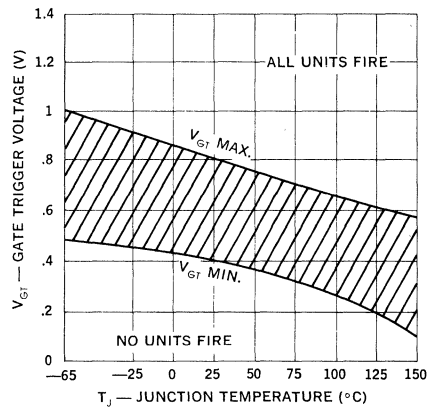
- Subgroup 1 — Shock
- Vibration, Variable Frequency
- Subgroup 2 — Salt Atmosphere
- Subgroup 3 — Terminal Strength
- Subgroup 4 — High Temp. Anode Voltage — Critical rate or rise
- Subgroup 5 — Storage Life Test
- Subgroup 6 — Operating Life Test

TYPICAL CHARACTERISTICS
2N3027 — 2N3028 — 2N3029

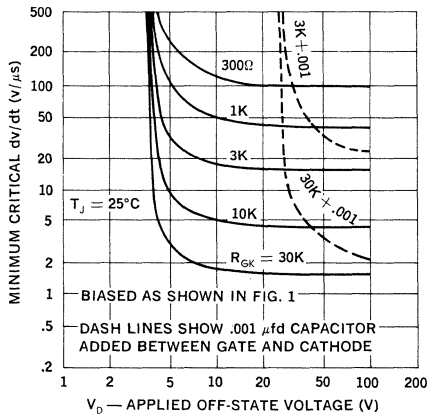
1 Gate Trigger Current



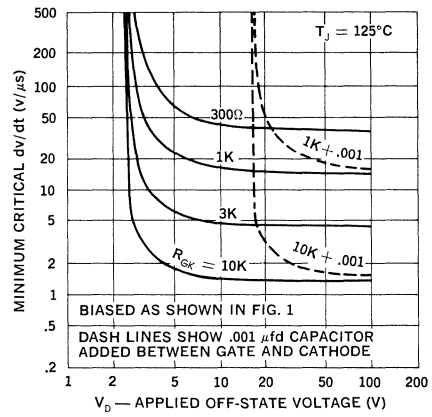
2 Gate Trigger Voltage



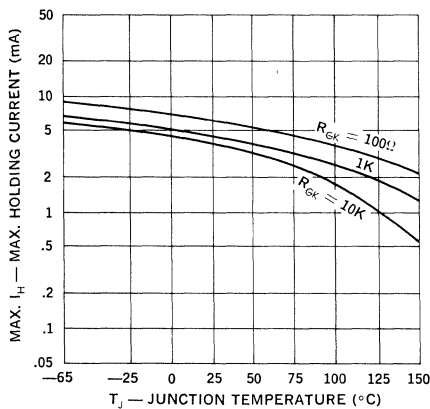
3 Min. Critical dv/dt (25°C — R Bias)



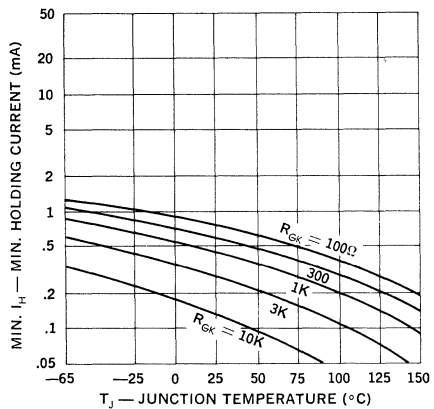
4 Min. Critical dv/dt (125°C — R Bias)



5 Max. Holding Current (Resistor Bias)

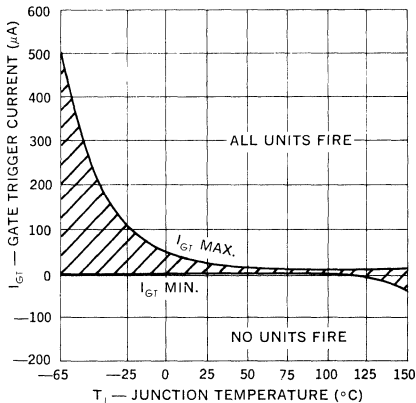


6 Min. Holding Current (Resistor Bias)

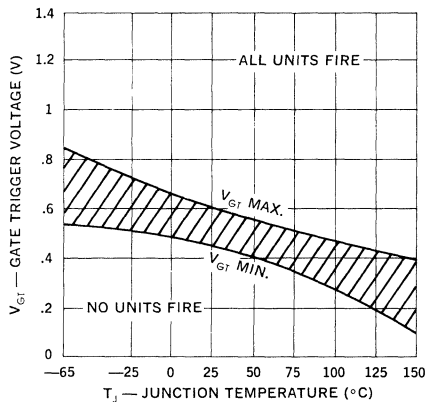


TYPICAL CHARACTERISTICS
2N3030 — 2N3031 — 2N3032

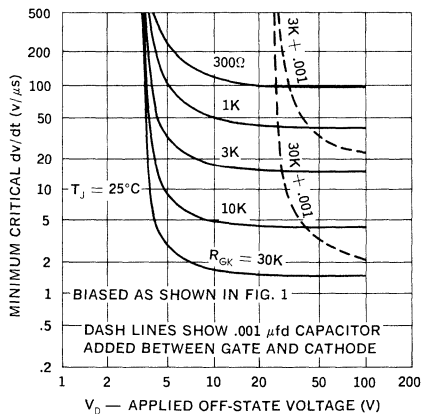
1 Gate Trigger Current



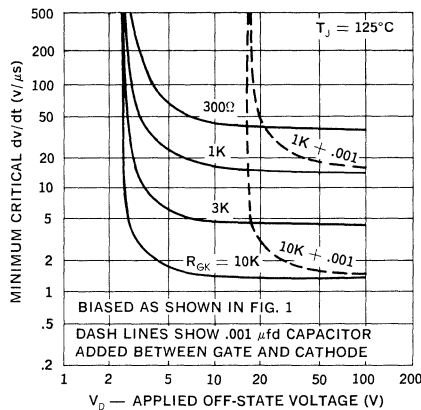
2 Gate Trigger Voltage



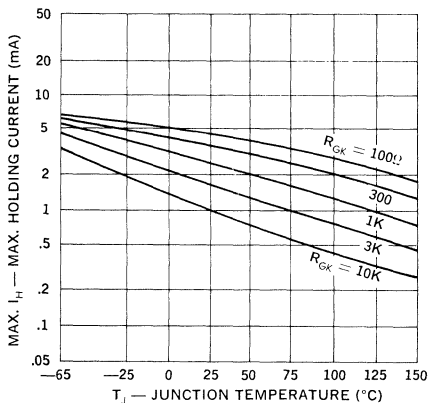
3 Min. Critical dv/dt (25°C — R Bias)



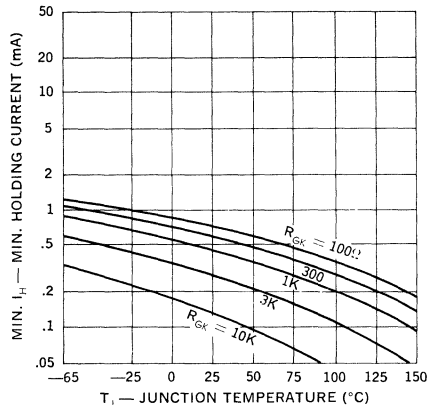
4 Min. Critical dv/dt (125°C — R Bias)



5 Max. Holding Current (Resistor Bias)

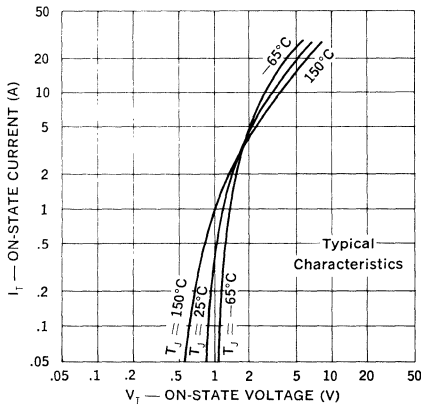


6 Min. Holding Current (Resistor Bias)

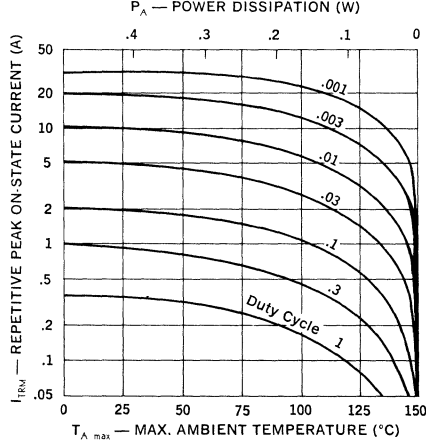


CURRENT RATINGS

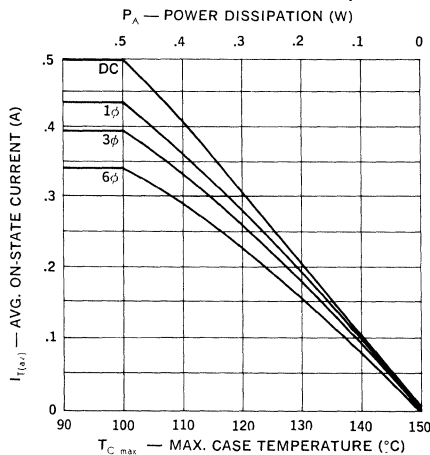
C1 Forward on Current vs. Voltage



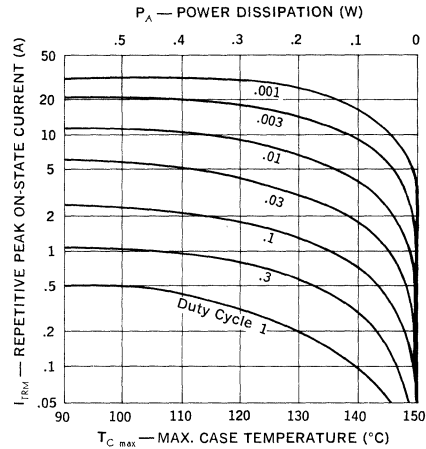
C3 Peak Current vs. Ambient Temperature TO-18 Ratings (see note)



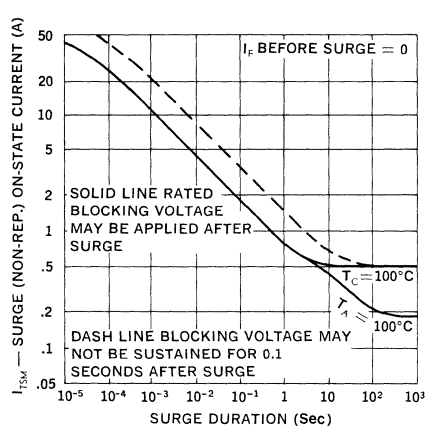
C5 Average Current vs. Case Temperature



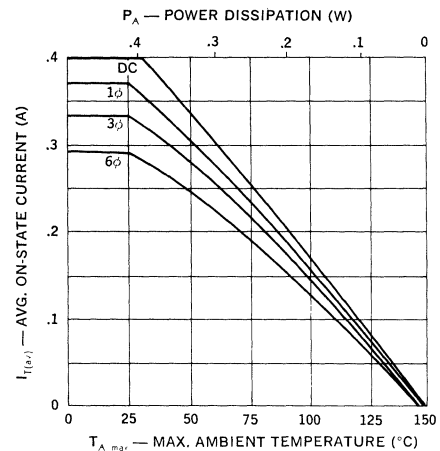
C2 Peak Current vs. Case Temperature



C4 Surge Current vs. Time

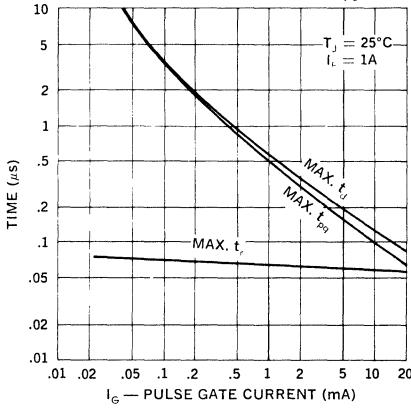


C6 Average Current vs. Ambient Temperature TO-18 Ratings (see note)

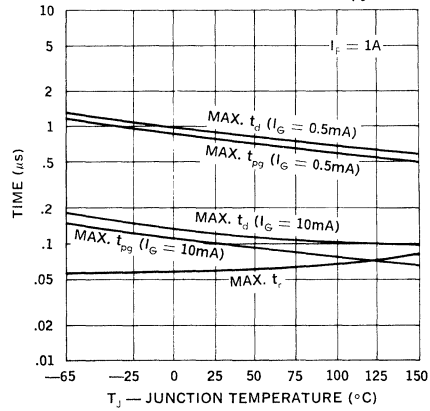


SWITCHING SPEEDS

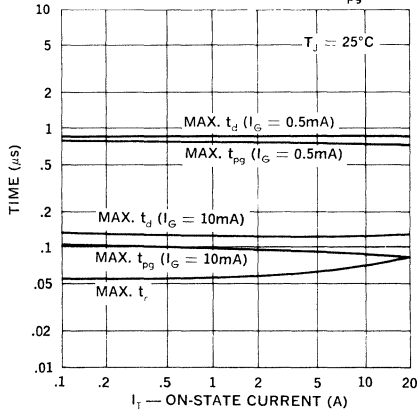
S1 Maximum Delay Time t_d , Rise Time t_r , and Gate Trigger Pulse Width t_{pg} (on)



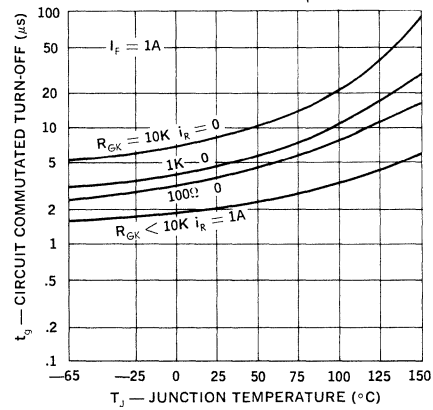
S2 Maximum Delay Time t_d , Rise Time t_r , and Gate Trigger Pulse Width t_{pg} (on)



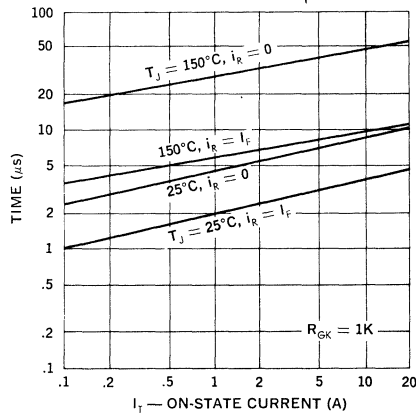
S3 Maximum Delay Time t_d , Rise Time t_r , and Gate Trigger Pulse Width t_{pg} (on)



S4 Maximum Circuit Commutated Turn-off Time t_q



S5 Maximum Circuit Commutated Turn-off Time t_q



10

SCRs

1.6 Amp, Planar

2N5724-2N5728

FEATURES

- Maximum Gate Trigger Current: 20 μ A
- Closely Controlled Gate Trigger Voltage: .44 to .6V
- Operating Current Range: 2mA to 1.6A
- Voltage Ratings: to 400V
- Low On-State Voltage
- Specified for dv/dt and Switching Time

DESCRIPTION

These devices are intended for general purpose usage in Military/aerospace or severe industrial environments. Major design parameters are specified at the temperature extremes, thus permitting worst case design on the basis of guaranteed values. These devices undergo 100% preconditioning, which includes high temperature storage and temperature cycling followed by a fine leak test as a regular part of the manufacturing procedure.

The high voltage types of the 2N5724 series are especially useful as pulse modulator switches in low to medium power pulse modulator applications. Specific parameters such as rise time, delay time, holding current, and recovery time can be selected for optimum performance in a pulse modulator circuit.

ABSOLUTE MAXIMUM RATINGS

	2N5724	2N5725	2N5726	2N5727	2N5728
Repetitive Peak Off-State Voltage, V_{DRM}	60V	100V	200V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	60V	100V	200V	300V	400V
Non-Repetitive Peak Off-State Voltage, V_{DSM}			500V		
D.C. On-State Current, I_T					
75°C Ambient			450mA		
85°C Case			1.6A		
Repetitive Peak On-State Current, I_{TRM}			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}			15A		
Peak Gate Current, I_{GM}			250mA		
Average Gate Current, $I_{G(AV)}$			25mA		
Reverse Gate Current, I_{GR}			3mA		
Reverse Gate Voltage, V_{GR}			6V		
Operating and Storage Temperature Range			-65°C to +150°C		

MECHANICAL SPECIFICATIONS

2N5724-2N5728

	ins.	mm.
A	305-335	7.75-8.51
B	335-370	8.51-9.40
C	240-260	6.35-6.60
D	010-030	.25-.76
E	5 MIN	12.70 MIN
F	017 ± 002 001	4.32 ± 051 025
G	200	5.08
H	100	2.54
J	031 ± 003	7.9 ± 08
K	029-045	7.4-1.14
L	100	2.54

TO-205AD (TO-39)

ELECTRICAL SPECIFICATIONS

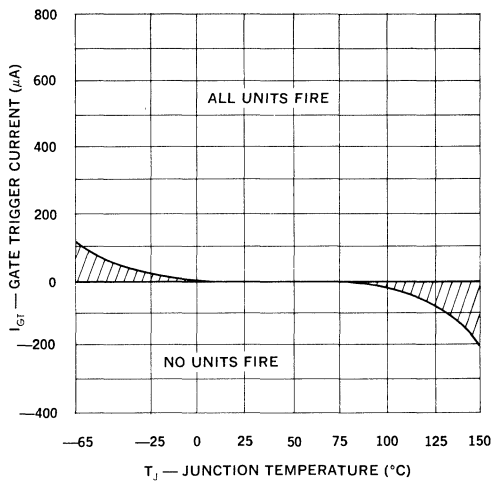
Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1 Visual and Mechanical						
SUBGROUP 2 (25°C TESTS)						
Off-State Current	I_{DRM}	—	.05	0.1	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	.05	0.1	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	V_{GR}	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	I_{GT}	—	2	20	μA	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	V_{GT}	0.44	0.5	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	V_T	—	2.3	2.5	V	$I_T = 5A$ (pulse test)
Holding Current	I_H	0.3	0.8	2.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 3 (25°C TESTS)						
Off-State Voltage — Critical Rate of Rise	dv/dt	100	150	—	$v/\mu S$	$R_{GK} = 1K, V_D = 30V$
Gate Trigger — on Pulse Width	t_{pp} (on)	—	0.1	0.5	μS	$I_G = 10mA, I_T = 1A, V_D = 30V$
Delay Time	t_d	—	0.1	—	μS	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	t_r	—	0.3	—	μS	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	15	30	μS	$I_T = 1A, I_R = 1A, R_{GK} = 1K$
2N5724, 2N5725, 2N5726, 2N5727, 2N5728		—	30	50	μS	
SUBGROUP 4 (150°C TESTS)						
High Temp. Off-State Current	I_{DRM}	—	50	200	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	I_{RRM}	—	80	200	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	V_{GT}	0.10	0.15	—	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	I_H	0.10	0.15	—	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 5 (–65°C TESTS)						
Low Temp. Gate Trigger Voltage	V_{GT}	—	0.7	0.9	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	I_{GT}	—	50	125	μA	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	I_H	—	1.2	3.0	mA	$R_{GK} = 1K, V_D = 5V$

Note 1 See rating curves for full rating information.

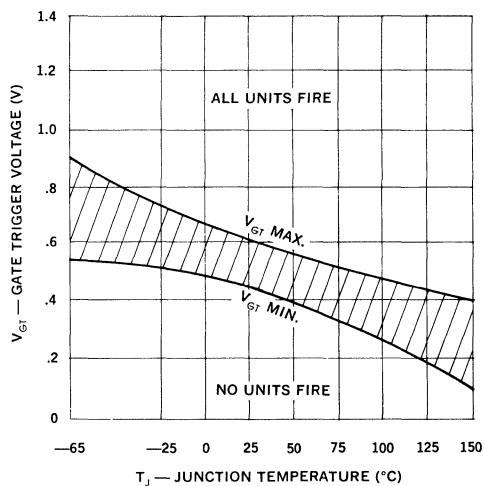
Note 2 Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1K or smaller, or other adequate gate bias is used.

10

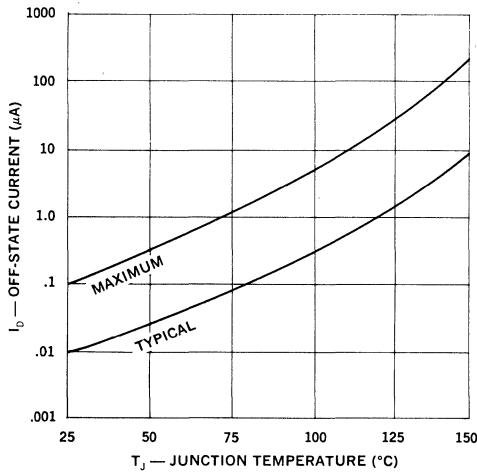
Gate Trigger Current



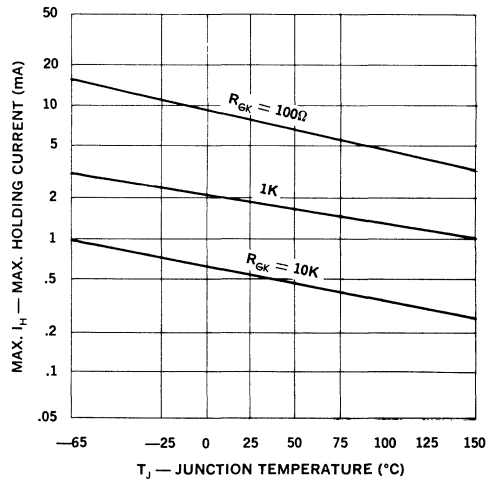
Gate Trigger Voltage



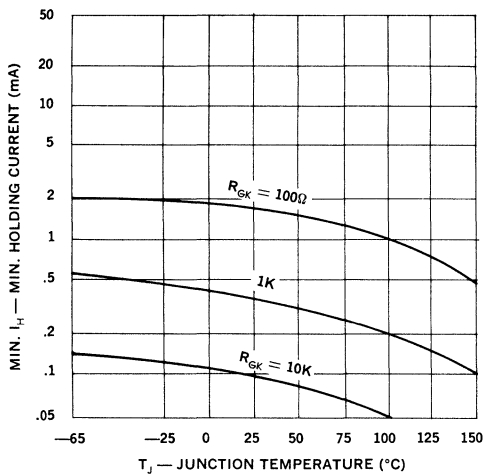
Off-State Current



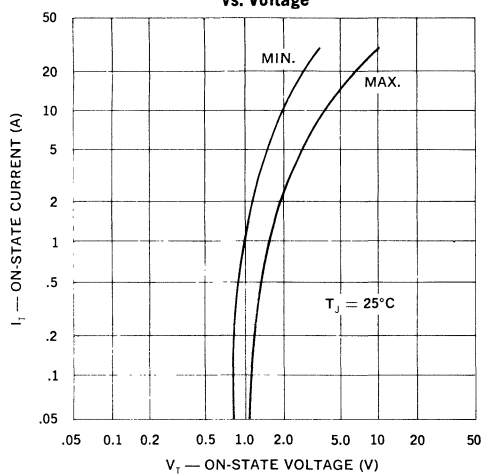
Max. Holding Current

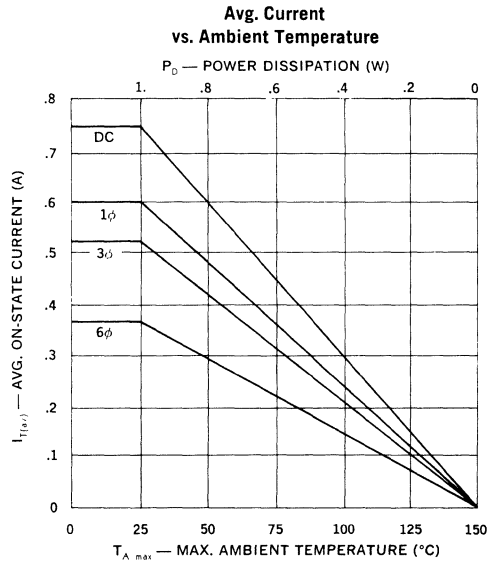
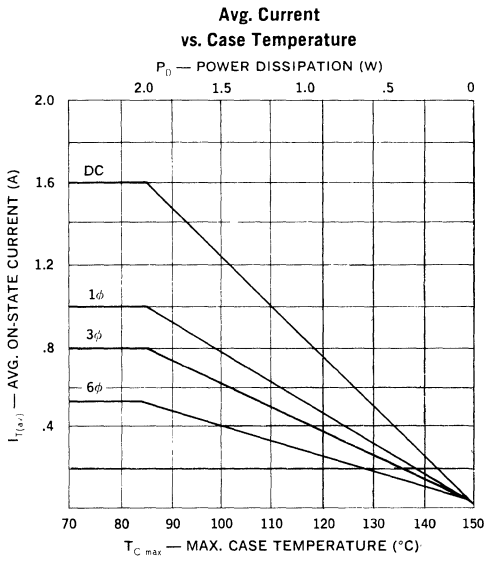


Min. Holding Current



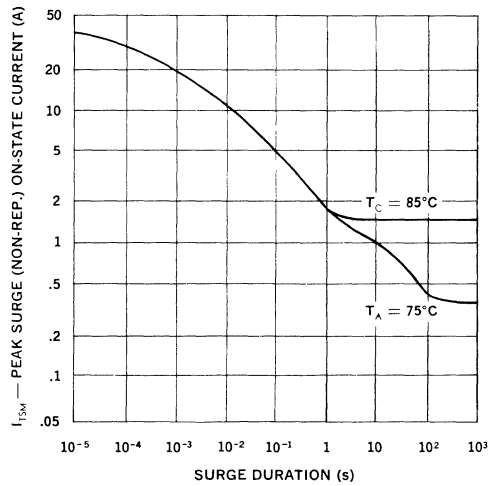
On-State Current vs. Voltage





10

Surge Current



PUTs

2N6119-2N6120

Planar, TO-18, Hermetic

FEATURES

- Hermetically Sealed TO-18 Metal Can
- Programmable η , R_{BB} , I_p and I_v
- Maximum Peak Point Current: 150nA
- Minimum Valley Current to 1.5mA
- Nano-Amp Leakage
- Passivated Planar Construction for Maximum Reliability and Parameter Uniformity

DESCRIPTION

Functionally equivalent to standard unijunction transistors, Unitrode's Programmable Unijunction Transistors offer the distinct advantage of versatile programming. External resistors can be added to meet the designer's needs in programming η , R_{BB} , I_p and I_v functions. This series also features a hermetically sealed TO-18 package for optimum reliability in all environmental conditions. Applications include pulse and timing circuits, SCR trigger circuits, relaxation oscillators and sensing circuits. For additional information see Unitrode Application Note U-66.

ABSOLUTE MAXIMUM RATINGS

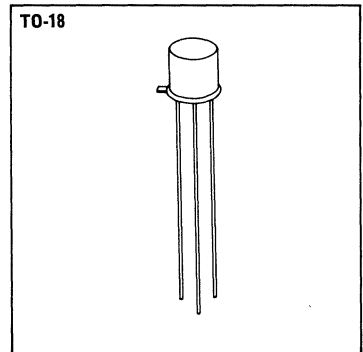
Anode-to-Cathode Voltage, V_{AK}	$\pm 40V$
Gate-to-Cathode Forward Voltage, V_{GK}	40V
Gate-to-Anode Reverse Voltage, V_{GAR}	40V
Gate-to-Cathode Reverse Voltage, V_{GKR}	-5V
Peak Recurrent Forward Current		
10 μ s, 1% Duty Cycle	8A
100 μ s, 1% Duty Cycle	5A
Power Dissipation		
25°C Ambient	400mW
Derating Factor	3.2mW/°C
Storage Temperature	-55°C to +125°C
Operating Temperature Range	-55°C to +125°C

MECHANICAL SPECIFICATIONS

GATE CONNECTED TO CASE

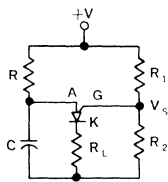
2N6119-2N6120

	INCHES	MILLIMETERS
A	.178-195 DIA.	4.52-4.95 DIA.
B	.170-210	4.31-5.33
C	.5 MIN.	12.70 MIN.
D	.209-230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 DIA .001 DIA	432 ± .051 .025
F	.020 MAX.	.508 MAX.
G	100±.010 DIA.	2.54±.254 DIA.
H	.041±.005	1.04±.127
J	.028-.048	711-1.22

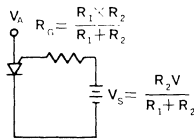


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

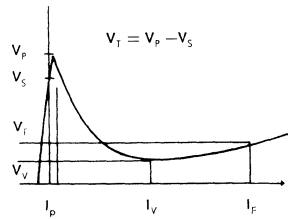
Test	Symbol	Fig.	2N6119		2N6120		Units	Test Conditions
			Min.	Max.	Min.	Max.		
Peak Current	I_P	1	—	5	—	1.0	μA	$R_G = 10k, V_S = 10V$ $R_G = 1 \text{ Meg.}$
Valley Current	I_V	1	70	—	25	—	μA	$R_G = 10k, V_S = 10V$ $R_G = 1 \text{ Meg.}$ $R_G = 200\Omega$
			1.5	—	1.0	—	mA	
Offset Voltage	V_T	1	0.2	0.6	0.2	0.6	V	$R_G = 10k, V_S = 10V$ $R_G = 1 \text{ Meg.}$
			0.2	1.6	0.2	0.6	V	
Gate-to-Anode Leakage	I_{GAO}	2	—	10	—	10	nA	$T = 25^\circ C, V_S = 40V$ $T = 75^\circ C$
			—	100	—	100	nA	
Gate-to-Cathode Leakage	I_{GKS}	3	—	100	—	100	nA	$V_S = 40V$
Forward Voltage	V_F	4	—	1.0	—	1.0	V	$I_F = 50mA$
Pulse Output Voltage	V_o	5	9	—	9	—	V	
Pulse Output Rate of Rise	t_r	5	—	80	—	80	ns	



a) Typical Circuit



b) Equivalent Test Circuit



c) Characteristic Curve

Figure 1

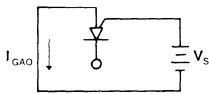


Figure 2

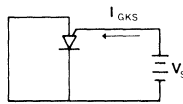


Figure 3

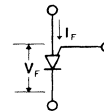


Figure 4

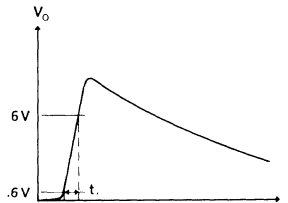
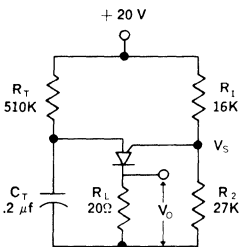
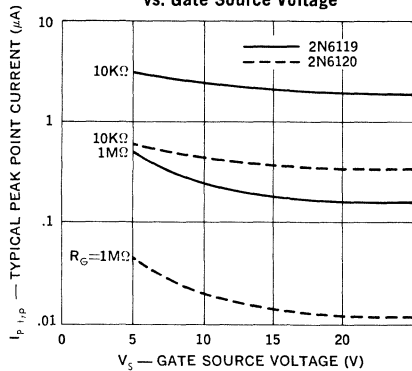


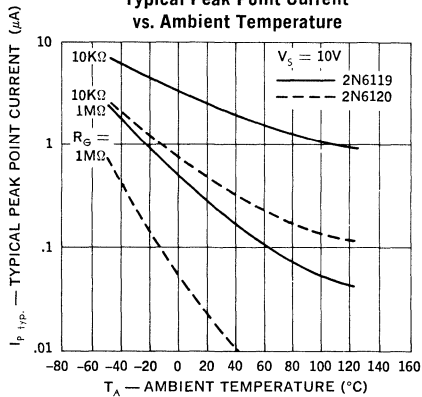
Figure 5

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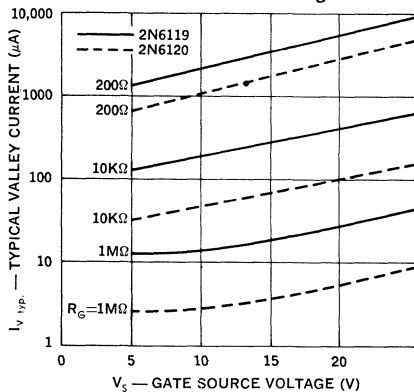
Typical Peak Point Current vs. Gate Source Voltage



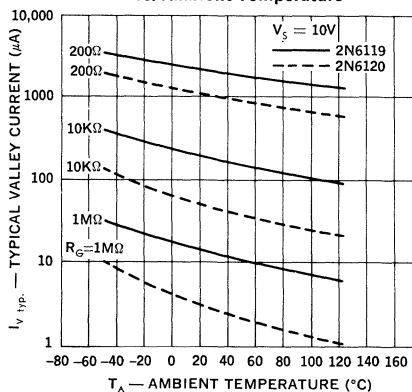
Typical Peak Point Current vs. Ambient Temperature



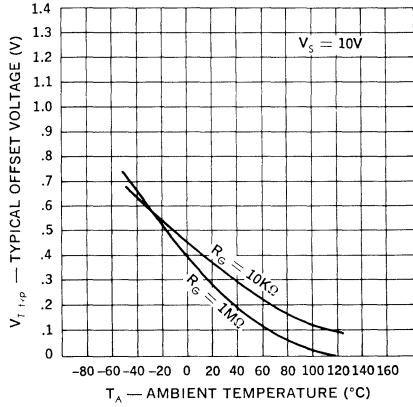
Typical Valley Current vs. Gate Source Voltage



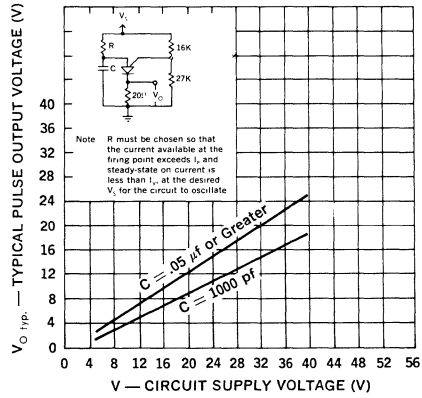
Typical Valley Current vs. Ambient Temperature



Typical Offset Voltage vs. Ambient Temperature

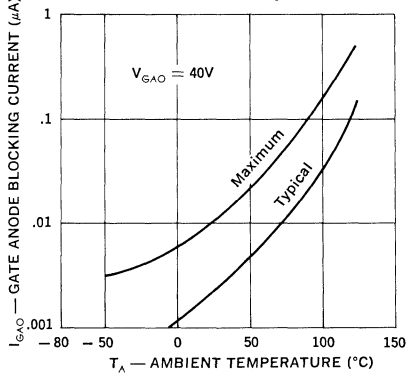


Typical Pulse Output vs. Circuit Supply Voltage

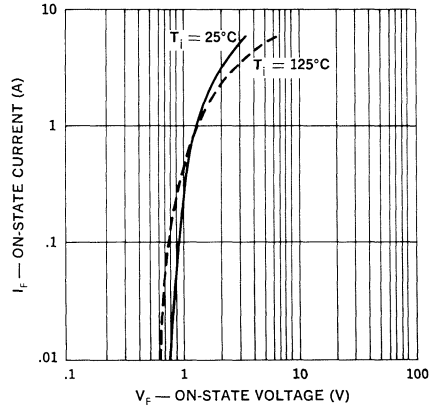


10

Gate-Anode Blocking Current vs. Ambient Temperature



Typical On-State Current vs. Voltage



PUTs

2N6137

Military, Planar, TO-18, Hermetic

FEATURES

- Available as JAN and JANTX types per MIL standard 19500/493
- -55°C to $+125^{\circ}\text{C}$ Temperature Range for Timing and Oscillator Circuits
- $I_r \leq 10\mu\text{A}$ at $T = -55^{\circ}\text{C}$
 $I_v \geq 40\mu\text{A}$ at $T = +125^{\circ}\text{C}$
- Programmable η , R_{BB} , I_p and I_v
- Peak Recurrent Current: of 5A
- Low On-State Voltage Drop
- Hermetically Sealed Metal Case and Planar Passivated Construction for Maximum Reliability and Parameter Stability.

DESCRIPTION

The Programmable Unijunction Transistor is functionally equivalent to a standard unijunction transistor with the advantage that external resistors can be used to program η , R_{BB} , I_p , and I_v , depending upon the designer's needs. The Unitorode device, in addition to allowing programmable versatility, is completely planar passivated and packaged in a TO-18 hermetically sealed package, which offers an order of magnitude improvement in inherent reliability over many similar devices. Applications include pulse and timing circuits, SCR trigger circuits, relaxation oscillators, and sensing circuits. For further application information see Unitorode Application Note U-66.

ABSOLUTE MAXIMUM RATINGS

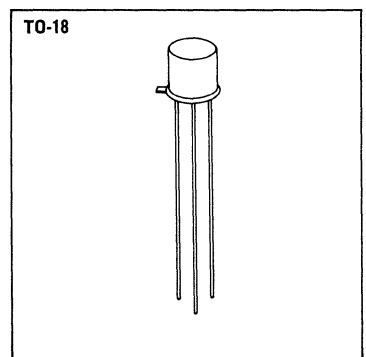
Anode-to-Cathode Forward Voltage, V_{AK}	40V
Anode-to-Cathode Reverse Voltage, V_{AKR}	40V
Gate-to-Cathode Forward Voltage, V_{GK}	40V
Gate-to-Anode Reverse Voltage, V_{GAR}	40V
Gate-to-Cathode Reverse Voltage, V_{GKR}	5V
Peak Recurrent Forward Current, $10\mu\text{s}$ 1% Duty Cycle	5A
Peak Gate Current, I_{GM}	250mA
Average Gate Current, $I_{\text{G(AV)}}$	50mA
Power Dissipation	
25°C Ambient	300mW
Derating Factor	2.4mW/ $^{\circ}\text{C}$
Storage Temperature Range	-55°C to $+125^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$

MECHANICAL SPECIFICATIONS

2N6137

ANODE CONNECTED TO CASE

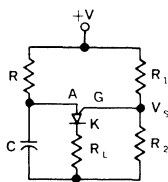
	INCHES	MILLIMETERS
A	.178- .195 DIA.	4.52-4.95 DIA.
B	.170- .210	4.31-5.33
C	5 MIN.	12.70 MIN.
D	.209- .230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 DIA. .001 DIA.	.432 ± .051 .025
F	.020 MAX.	.508 MAX.
G	.100±.010 DIA.	2.54±.254 DIA.
H	.041±.005	1.04±.127
J	.028-.048	.711-1.22



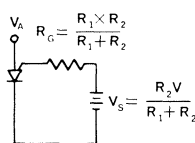
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

Test	Symbol	Figure	Minimum	Typical	Maximum	Units	Test Conditions
SUBGROUP 1 Visual and Mechanical							
SUBGROUP 2							
Gate-anode blocking current	I_{GAO}	2	—	2	10	nA	$V_{GA} = \text{Rating}$
Gate-cathode blocking current	I_{GKS}	3	—	5	100	nA	$V_{GK} = \text{Rating}$
SUBGROUP 3							
Peak-point anode current	I_p	1	—	1 2.5	2 5	μA	$R_G = 1 \text{ Meg} / \left. \begin{array}{l} R_G = 10\text{K} \\ R_G = 10\text{K} \end{array} \right\} V_s = 10\text{V}$
Peak-point offset voltage	V_T	1	0.2 0.2	0.26 0.35	1.6 0.6	V	
Valley-point anode current	I_V	1	— 70 1.5	15 200 2	50 — —	μA μA mA	
SUBGROUP 4							
Forward on-state voltage	V_F	4	—	0.85	1.0	V	$I_F = 50\text{mA}$
Peak pulse voltage	V_O	5	9	12	—	V	
Peak pulse voltage rise time	t_r	5	—	50	80	ns	
SUBGROUP 5							
Gate-anode blocking current (125°C Test)	I_{GAO}	2	—	150	500	nA	$V_{GA} = \text{Rating}$
Valley-point anode current (125°C Test)	I_V	1	40	100	—	μA	$R_G = 10\text{K}, V_s = 10\text{V}$
Peak-point anode current (−55°C Test)	I_p	1	—	7.5	10	μA	$R_G = 10\text{K}, V_s = 10\text{V}$

† All values in table are JEDEC registered



a) Typical Circuit



b) Equivalent Test Circuit

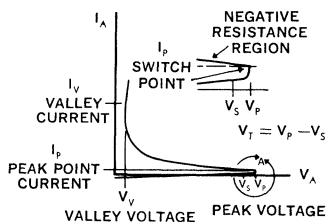


Figure 1

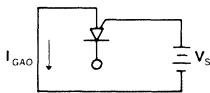


Figure 2

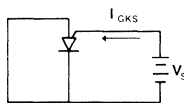


Figure 3

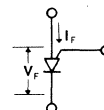


Figure 4

Note: Conditions for oscillation

$$\frac{V_{BB} - V_p}{R} > I_p$$

$$\frac{V_{BB} - V_v}{R} < I_v$$

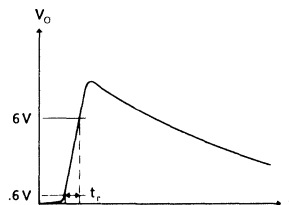
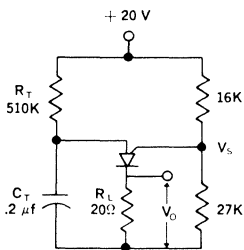
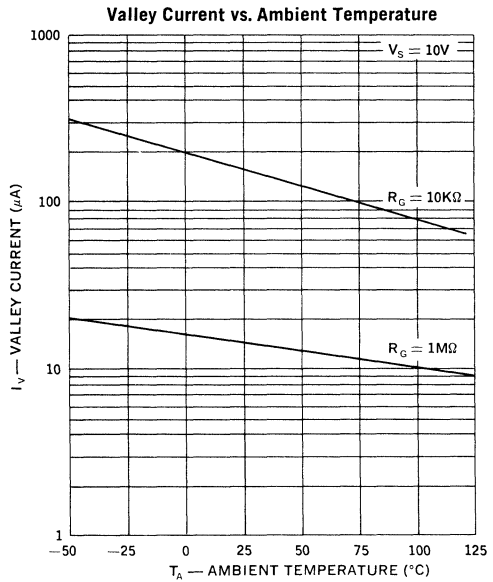
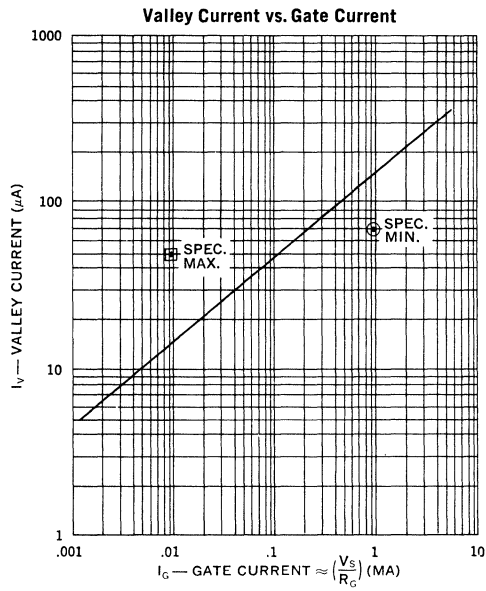
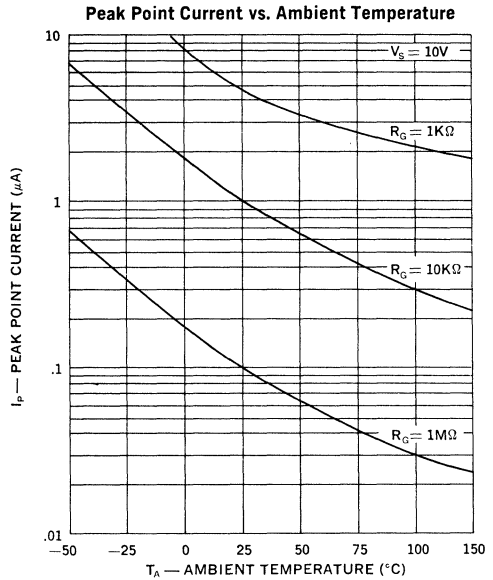
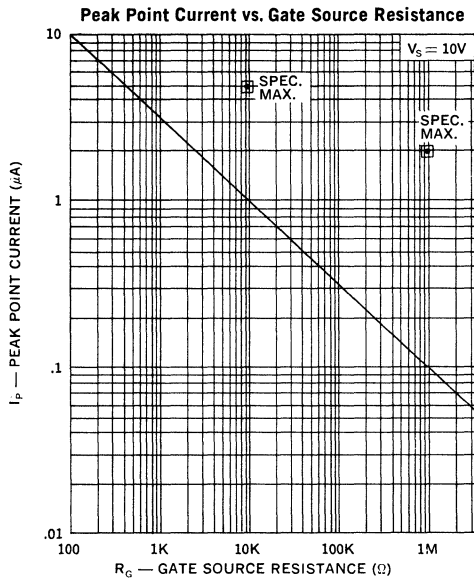
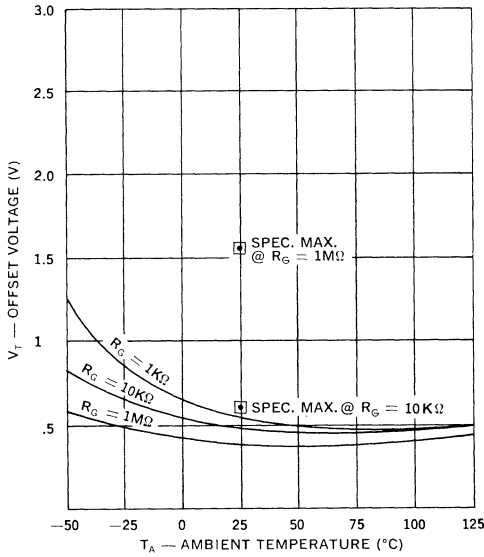


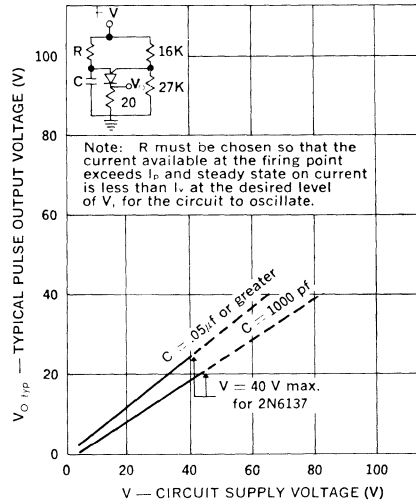
Figure 5



Offset Voltage vs. Ambient Temperature

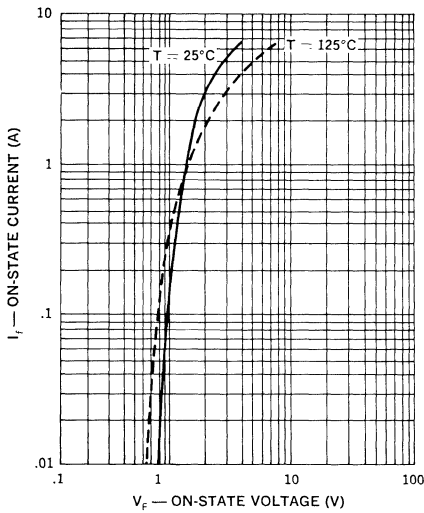


Typical Pulse Output Voltage vs. Circuit Supply Voltage

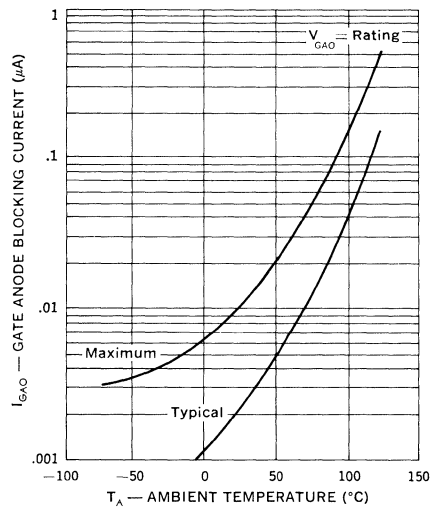


10

Typical Current vs. On-State Voltage



Gate-Anode Blocking Current vs. Ambient Temperature



SCRs

.5A, Planar

AA100-AA104
AA107-AA111
AA114-AA118

FEATURES

- Maximum Gate Trigger Current: 2, 20 or 200 μ A
- Tight Gate Trigger Voltage Range: .44 to .6V
- Voltage Ratings: to 400V
- Specified for dv/dt and Switching Time

DESCRIPTION

This data sheet describes Unitrode's AA Series 0.5A SCRs designed for low-current sensing applications. Units are available in a complete range of blocking voltages from 60 to 400 volts.

The AA100 series offers a maximum gate trigger current of 2.0 microamps making it the most sensitive device of its type. The AA107 series has a maximum I_{GT} of 20 μ A while this parameter is specified at 200 μ A for the AA114 series.

ABSOLUTE MAXIMUM RATINGS

	AA100 AA107 AA114	AA101 AA108 AA115	AA102 AA109 AA116	AA103 AA110 AA117	AA104 AA111 AA118
Repetitive Peak Off-State Voltage, V_{DRM}	60V	100V	200V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	60V	100V	200V	300V	400V
Non-Repetitive Peak Reverse Voltage, V_{RSM}	80V	150V	300V	400V	500V
Non-Repetitive Peak Off-State Voltage, V_{DSM}			500V		
D.C. On-State Current, I_T					
75°C Ambient			250mA		
100°C Case			500mA		
Repetitive Peak On-State Current, I_{TRM}			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}			5A		
Peak Gate Current, I_{GM}			250mA		
Average Gate Current, $I_{G(AV)}$			25mA		
Reverse Gate Voltage V_{GR}			6V		
Operating and Storage Temperature Range			-65°C to +150°C		

MECHANICAL SPECIFICATIONS

AA100-AA104 AA107-AA111 AA114-AA118

	INCHES	MILLIMETERS
A	178-195 DIA	4.52-4.95 DIA
B	170-210	4.31-5.33
C	5 MIN	12.70 MIN
D	209-230 DIA	5.31-5.84 DIA
E	.017 ± .002 DIA .001 DIA.	432 ± .051 .025
F	.020 MAX	508 MAX
G	100±.010 DIA.	2.54±.254 DIA
H	.041±.005	1.04±.127
J	.028-.048	.711-1.22

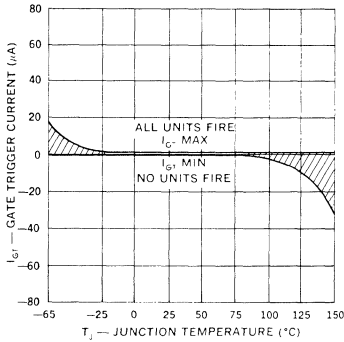
T0-18

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

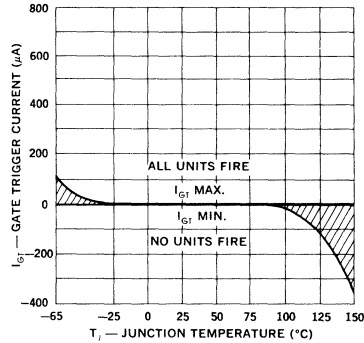
Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1						
Visual & Mechanical						
SUBGROUP 2 (25°C TESTS)						
Off-State Current	I_{DRM}	—	.01	0.1	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$ $R_{GK} = 1K, V_{RRM} = \text{Rating}$ $V_{GR} = 2V$ $R_{GS} = 10K, V_D = 5V$
Reverse Current	I_{RRM}	—	.01	0.1	μA	
Reverse Gate Current	I_{GR}	—	0.1	0.2	μA	
Gate Trigger Current	I_{GT}	—	0.2	2.0	μA	
AA100-104		—	2.0	20	μA	
AA107-111		—	20	200	μA	
AA114-118		—	20	200	μA	
Gate Trigger Voltage	V_{GT}	0.44	0.52	0.60	V	$R_{GS} = 100\Omega, V_D = 5V$ $I_T = 1.0 A (\text{pulse})$ $R_{GK} = 1K$
On-State Voltage	V_T	—	1.1	1.5	V	
Holding Current	I_H	0.3	0.5	2.0	mA	
SUBGROUP 3 (25°C TESTS)						
Off-State Voltage — Critical Rate of Rise	dv/dt	50	100	—	V/ μS	$R_{GK} = 1K, V_D = 30V$ $I_G = 10mA, I_T = 1A, V_D = 30V$ $I_G = 10mA, I_T = 1A, V_D = 30V$ $I_G = 10mA, I_T = 1A, V_D = 30V$ $I_T = 1A, I_R = 1A, R_{GK} = 1K$
Gate Trigger — on Pulse Width	$t_{pg} (\text{on})$	—	0.5	2.0	μS	
Delay Time	t_d	—	0.6	—	μS	
Rise Time	t_r	—	0.4	—	μS	
Circuit Commutated Turn-off Time	t_q	—	20	50	μS	
SUBGROUP 4 (125°C TESTS)						
Off-State Current	I_{DRM}	—	10	20	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$ $R_{GK} = 1K, V_{RRM} = \text{Rating}$ $R_{GS} = 100\Omega, V_D = 5V$ $R_{GK} = 1K$
Reverse Current	I_{RRM}	—	30	100	μA	
Gate Trigger Voltage	V_{GT}	0.15	0.2	—	V	
Holding Current	I_H	0.2	0.4	1.5	mA	

Note: Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1000 ohms or smaller, or other adequate bias is used.

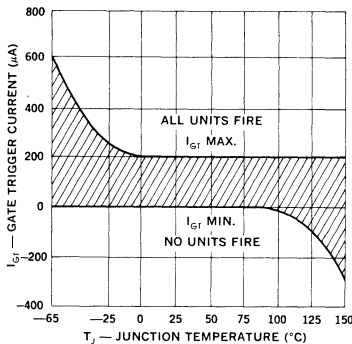
Gate Trigger Current
AA100 Series



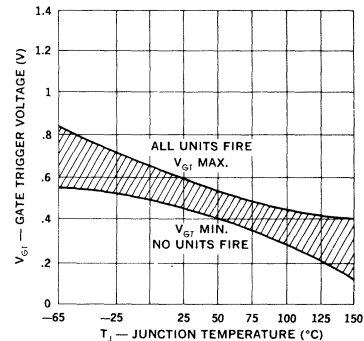
Gate Trigger Current
AA107 Series



Gate Trigger Current
AA114 Series

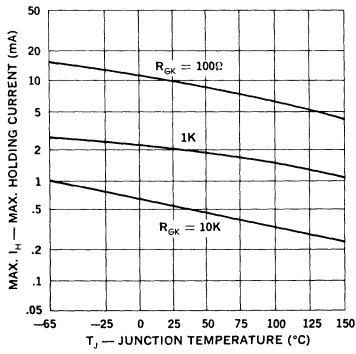


Gate Trigger Voltage

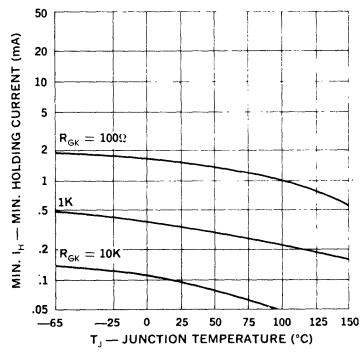


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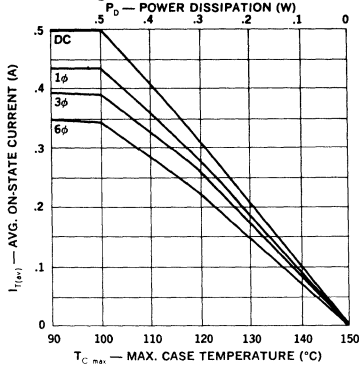
Max. Holding Current



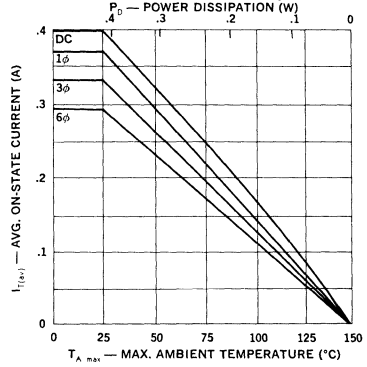
Min. Holding Current



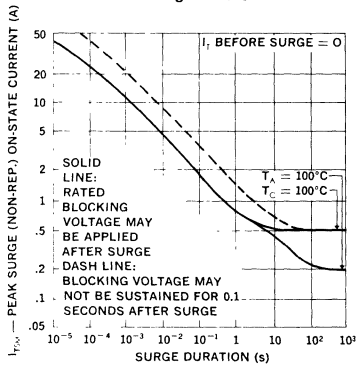
Avg. Current vs. Case Temperature



Avg. Current vs. Ambient Temperature



Surge Current



SCRs

1.6 Amp, Planar

AD100-AD104
AD107-AD111
AD114-AD118

FEATURES

- Maximum Gate Trigger Current: 2, 20 or 200 μ A
- Tight Gate Trigger Voltage Range: .44 to .6V
- Voltage Ratings: to 400V
- Specified for dv/dt and Switching Time

DESCRIPTION

This data sheet describes Unitrode's AD Series 1.6A SCRs designed for medium-current control and sensing applications. Units are available in a complete range of blocking voltages from 60 to 400 volts.

The AD100 series offers a maximum gate trigger current of 2.0 microamps making it the most sensitive device of its type. The AD107 series has a maximum I_{GT} of 20 μ A while this parameter is specified at 200 μ A for the AD114 series.

ABSOLUTE MAXIMUM RATINGS

	AD100 AD107 AD114	AD101 AD108 AD115	AD102 AD109 AD116	AD103 AD110 AD117	AD104 AD111 AD118
Repetitive Peak Off-State Voltage, V_{DRM}	60V	100V	200V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	60V	100V	200V	300V	400V
Non-Repetitive Peak Reverse Voltage, V_{RSM}	80V	150V	300V	400V	500V
Non-Repetitive Peak Off-State Voltage, V_{DSM}			500V		
D.C. On-State Current, I_T					
75°C Ambient			450mA		
85°C Case			1.6A		
Repetitive Peak On-State Current, I_{TRM}			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}			15A		
Peak Gate Current, I_{GM}			250mA		
Average Gate Current, $I_{G(AV)}$			25mA		
Reverse Gate Voltage, V_{GR}			6V		
Operating and Storage Temperature Range			-65°C to +150°C		

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MECHANICAL SPECIFICATIONS

AD100-AD104 AD107-AD111 AD114-AD118

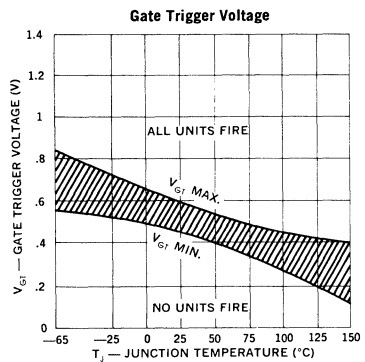
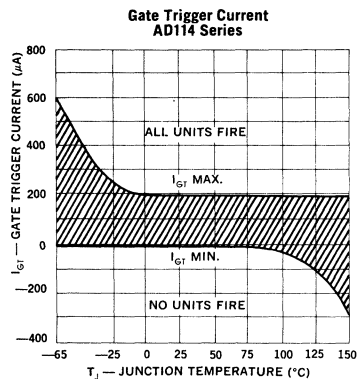
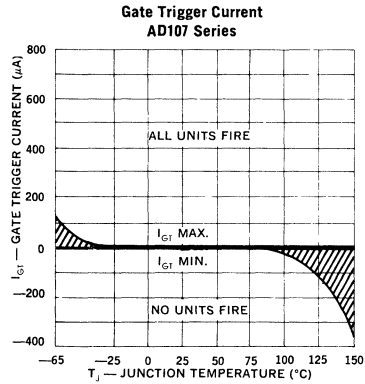
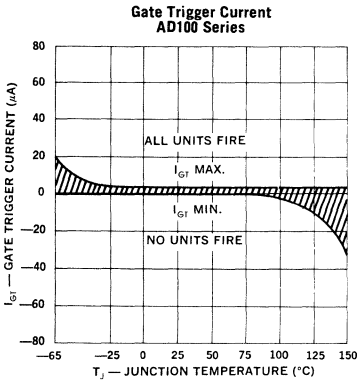
	ins.	mm
A	305-335	7.75-8.51
B	335-370	8.51-9.40
C	240-260	6.35-6.60
D	010-030	25-76
E	5 MIN	12.70 MIN
F	017 ± 002 001	432 ± 051 025
G	200	5.08
H	100	2.54
J	031 ± 003	79 ± 08
K	029-045	74-11.4
L	100	2.54

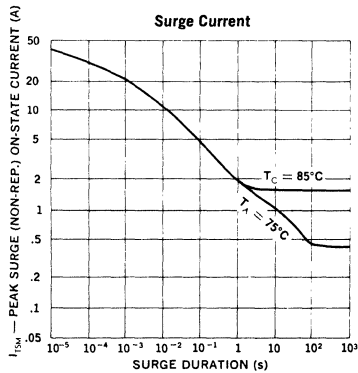
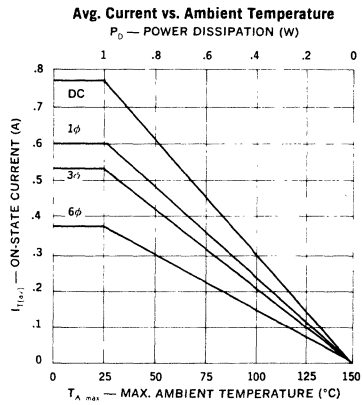
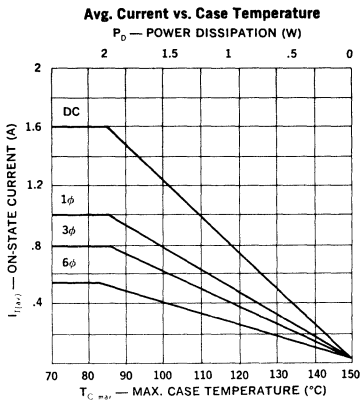
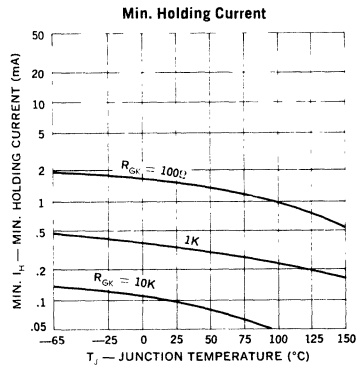
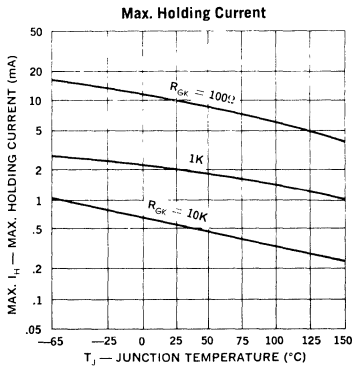
TO-205AD (TO-39)

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1						
Visual & Mechanical						
SUBGROUP 2 (25°C TESTS)						
Off-State Current	I_{DRM}	—	.01	0.1	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	.01	0.1	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Current	I_{GR}	—	0.1	0.2	μA	$V_{GR} = 2V$
Gate Trigger Current	I_{GT}	—	—	—	—	$R_{GS} = 10K, V_D = 5V$
AD100-104		—	0.2	2.0	μA	
AD107-111		—	2.0	20	μA	
AD114-118		—	20	200	μA	
Gate Trigger Voltage	V_{GT}	0.44	0.52	0.60	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	V_T	—	1.1	1.5	V	$I_T = 1.0 \text{ Amp (pulse)}$
Holding Current	I_H	0.3	0.5	2.0	mA	$R_{GK} = 1K$
SUBGROUP 3 (25°C TESTS)						
On-State Voltage-Critical Rate of Rise	dv/dt	50	100	—	V/ μs	$R_{GK} = 1K, V_D = 30V$
Gate Trigger-on Pulse Width	$t_{pg}(\text{on})$	—	0.5	2.0	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Delay Time	t_d	—	0.6	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	t_r	—	0.4	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	t_g	—	20	50	μs	$I_T = 1A, I_R = 1A, R_{GK} = 1K$
SUBGROUP 4 (125°C TESTS)						
Off-State Current	I_{DRM}	—	10	100	μA	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	I_{RRM}	—	30	100	μA	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Gate Trigger Voltage	V_{GT}	0.15	0.2	—	V	$R_{GS} = 100\Omega, V_D = 5V$
Holding Current	I_H	0.2	0.4	1.5	mA	$R_{GK} = 1K$

Note: Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1000 ohms or smaller, or other adequate bias is used.





SCRs

Nuclear Radiation Resistant, Planar

GA100
GA101
GA102

FEATURES

- Optimized for Radiation Resistance
- Fully Characterized for "Worst Case" Design
- Post Radiation Design Limits Specified
- Passivated Planar Construction for Maximum Reliability and Parameter Uniformity
- Pulse Currents: to 30A
- Max. Trigger Current 20mA after 3×10^{14} NVT
- Max. Holding Current 30mA after 3×10^{14} NVT

DESCRIPTION

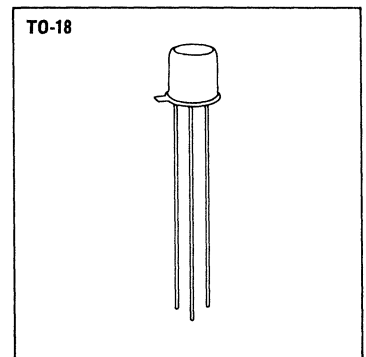
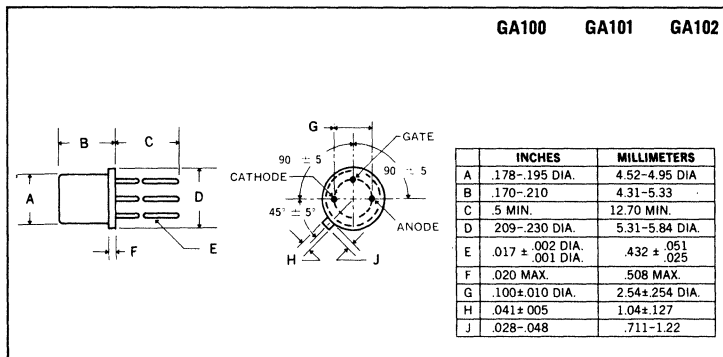
The GA100 Series of Radiation Hard SCR's have been designed to provide significantly greater radiation tolerance than conventional SCR's or Transistors with the same current handling ability. This Series is capable of operation after exposure to 10^{15} NVT.

The radiation resistant characteristics of the GA100 series devices make them particularly desirable for use under radiation environments in squib firing circuits; inverters and converters; pulse generators; relay drivers; and modulator discharge switches.

ABSOLUTE MAXIMUM RATINGS

	GA100	GA101	GA102
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	80V
D.C. On-State Current, I_T			
75°C Ambient		200mA	
100°C Case		400mA	
Repetitive Peak On-State Current, I_{TRM}		up to 30A	
Surge (non-rep.) On-State Current, I_{TSM} (Sq. Pulse-50ms)		5A	
Peak Gate Current, I_{GM}		250mA	
Average Gate Current, $I_{G(AV)}$		25mA	
Reverse Gate Voltage, V_{GR}		5V	
Reverse Gate Current, I_{GR}		3mA	
Storage Temperature Range		-65°C to +200°C	
Operating Temperature Range		-65°C to +150°C	

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Preradiation Limits			Post 3×10^{14} NVT Design Limits		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
SUBGROUP 1 Visual and Mechanical	—	—	—	—	—	—	—	MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)								
Off-State Current	I_{DRM}	—	.005	0.1	—	1.0	μA	$R_{GK} = 220\Omega$, $V_{DRM} = \text{Rating}$
Reverse Gate Current	I_{GR}	—	.01	0.1	—	1.0	μA	$V_{GR} = 2V$
Input Trigger Current (Note 2)	I_{ST}	1.8	2.3	3.5	—	20	mA	$R_{GK} = 220\Omega$, $V_D = 5V$
Gate Trigger Voltage	V_{GT}	0.4	0.5	0.7	—	1.5	V	$R_{GK} = 220\Omega$, $V_D = 5V$
On-State Voltage	V_T	0.8	1.1	1.5	—	3.0	V	$i_T = 1A$ (pulse test)
Holding Current	I_H	0.3	0.7	10	—	30	mA	$R_{GK} = 220\Omega$
SUBGROUP 3 (25°C Tests)								
Off-State Voltage-Critical Rate of Rise	dv_c/dt	20	40	—	—	—	V/ μs	$R_{GK} = 220\Omega$, $V_D = 30V$
Gate Trigger-on Pulse Width	t_{pg} (on)	—	.02	.05	—	0.1	μs	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Delay Time	t_d	—	.02	—	—	—	μs	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Rise Time	t_r	—	.05	—	—	—	μs	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	1.5	2.5	—	1.0	μs	$I_T = 1A$, $i_R = 1A$, $R_{GK} = 220\Omega$
SUBGROUP 4 (125°C Tests)								
High Temp Off-State Current	I_{DRM}	—	10	100	—	100	μA	$R_{GK} = 220\Omega$, $V_{DRM} = \text{Rating}$
High Temp Gate Trigger Voltage	V_{GT}	0.1	.17	—	0.1	—	V	$R_{GK} = 220\Omega$, $V_D = 5V$

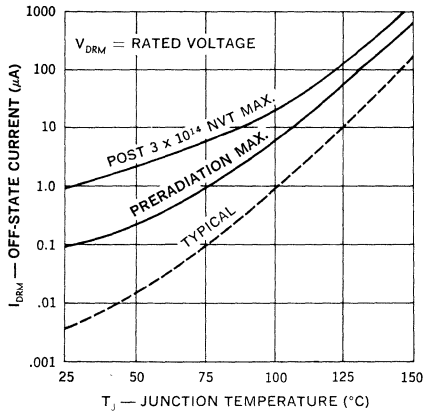
- Notes: 1. Off-State voltage ratings apply over the operating temperature range provided the gate is connected to the cathode through an appropriate resistor, or other adequate bias is used.
2. Total Input Trigger Current, including current required by 220 Ω gate bias resistance.

DESIGN CONSIDERATIONS

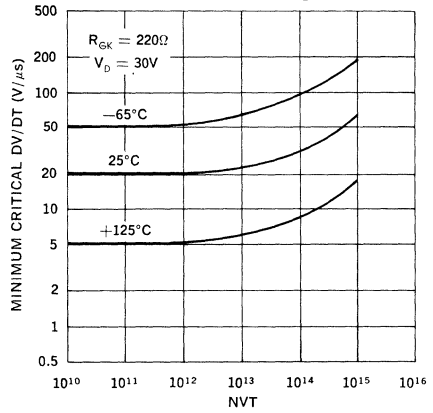
- Curve 1 shows the off-state current, I_{DRM} of the SCR as a function of temperature. I_{DRM} is increased by radiation damage, but is not a design consideration at the recommended gate bias levels.
In order to optimize for radiation tolerance, reverse blocking capability has not been retained as a design feature. Devices with reverse blocking capability can be provided.
- Minimum critical dv/dt levels are defined in Curve 2. The dv/dt capability is improved after radiation because of reduced triggering sensitivity. dv/dt is therefore a design consideration only prior to radiation.
- Curves 3 and 4 show the limits of Gate Trigger Voltage and Total Input Trigger Current prior to radiation. Maximum design limits after a total radiation dosage of 3×10^{14} NVT is also shown. Curves 5 and 6 show the maximum limits of Gate Trigger Voltage and Total Input Trigger Currents as a junction of neutron dosage. The minimum level of Trigger current prior to radiation is established by the shunting effect of a 220 ohm resistor between gate and cathode. After radiation the device is less sensitive and Total Trigger Current will increase to a level relatively independent of the bias resistance. The 220 ohm resistor is recommended since it raises the minimum preradiation trigger current to a level that is closer to the past radiation limit and minimizes the percentage change in this parameter.
- Current ratings shown in Curves 10, 11, and 12 apply after the device has been subjected to 3×10^{14} NVT. Current ratings prior to radiation are greater than the values indicated.
- Gamma radiation produces a reversible ionization (leakage) current within the device which is directly proportional to the Gamma flux level. When the Gamma flux level is in the range of 10 to 100 Roentgens per microsecond for burst durations greater than 1 microsecond, the device will self trigger ON. For the radiation bursts associated with nuclear explosions, the Gamma flux level will invariably cause device triggering at radiation levels significantly below the levels that would produce detectable permanent device damage due to cumulative neutron dosage. In applications where the burst effect triggering cannot be tolerated, it is necessary to reset the device after the radiation burst. Special circuit approaches such as additional SCRs to crowbar or otherwise cancel the output function may be used.

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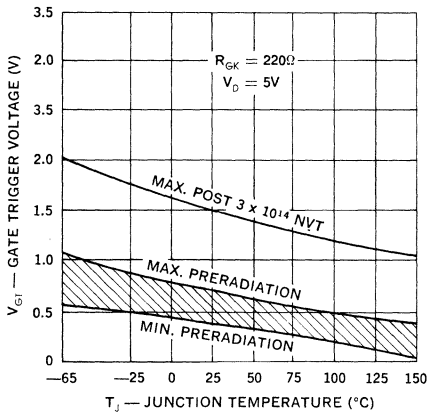
1. Off-State Current



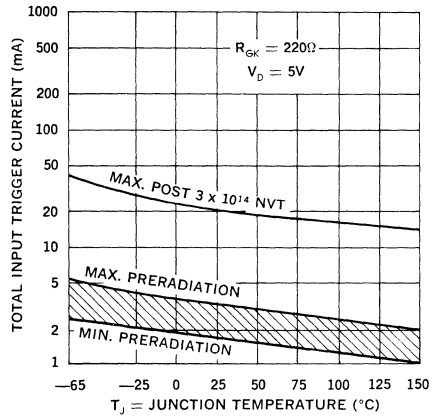
2. Minimum Critical DV/DT vs. Neutron Dosage



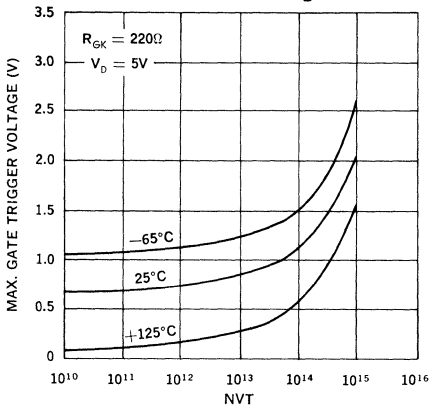
3. Gate Trigger Voltage



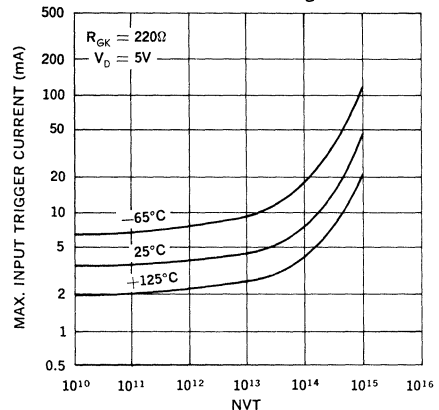
4. Input Trigger Current



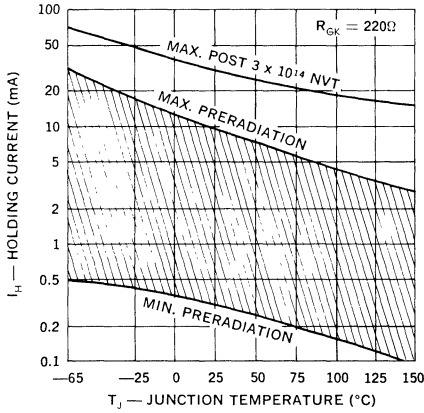
5. Max. Gate Trigger Voltage vs. Neutron Dosage



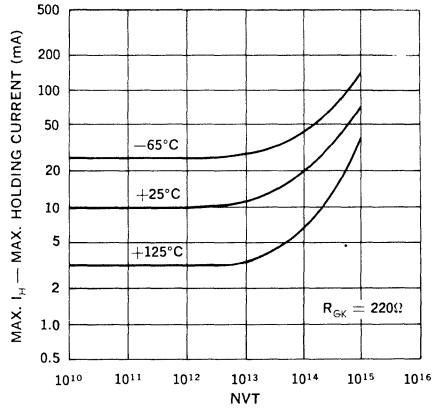
6. Max. Input Trigger Current vs. Neutron Dosage



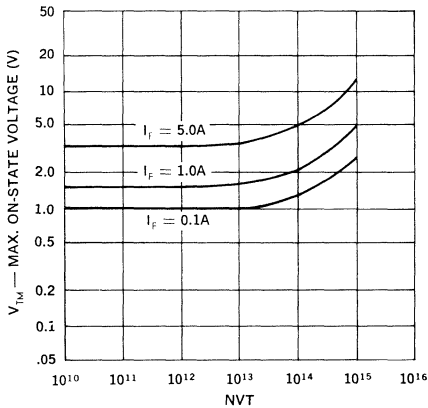
7. Holding Current



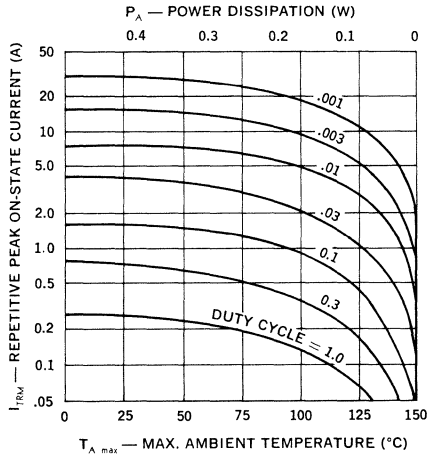
8. Max. Holding Current vs. Neutron Dosage



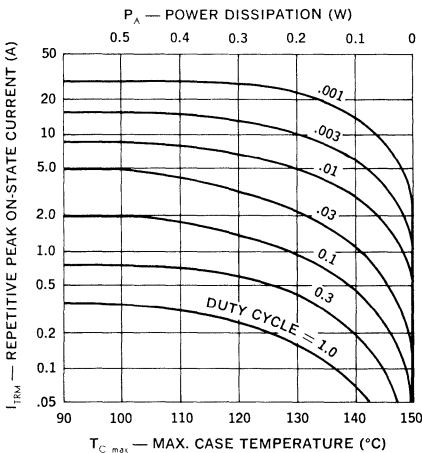
9. Max. On-State Voltage vs. Neutron Dosage



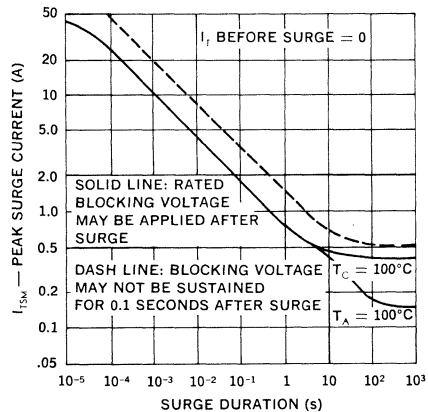
10. Peak Current vs. Ambient Temperature



11. Peak Current vs. Case Temperature



12. Surge Current vs. Time



10

SCRs

Nanosecond Switching, Planar

GA200 GB200
 GA200A GB200A
 GA201 GB201
 GA201A GB201A

FEATURES

- Rise Time: 10ns
- Delay Time: 10ns
- Recovery Time: 0.5 μ s
- Pulse Current: to 100A
- Turn-on with 20ns, 10 mA Gate Pulse

DESCRIPTION

The Unitrode Nanosecond Thyristor Switch combines the turn-on speed of logic level transistors with the high current switching capability inherent in SCRs. With this device engineers can now design circuits capable of switching pulse currents of 1A in less than 10ns or up to 30A in less than 20ns.

The GA/GB200 series is specifically designed for use as switching elements in high speed, low-to-medium power radar pulse modulators. Other applications include switching elements for phased array radars, laser pulse drivers, harmonic wave-form generators, line drivers and high current replacements for avalanche transistors. For applications requiring higher voltage levels, Unitrode has developed several "series string" circuits which allow the series connection of virtually an unlimited number of devices for voltages as high as 2000V with no significant decrease in speed. These circuits are described in Unitrode's Design Note #14.

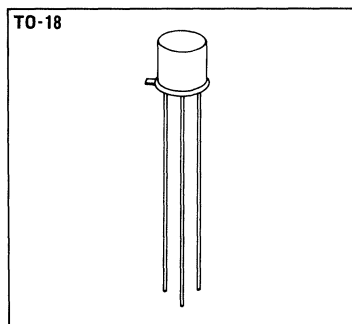
ABSOLUTE MAXIMUM RATINGS

	GA200 GA200A	GA201 GA201A	GB200 GB200A	GB201 GB201A
Repetitive Peak Off-State Voltage, V_{DRM}	60V	100V	60V	100V
Repetitive Peak On-State Current, I_{TRM}	up to 100A		up to 100A	
D.C. On-State Current, I_T				
70°C Ambient	200mA			
70°C Case	400mA		6A	
Peak Gate Current, I_{GM}	250mA		250mA	
Average Gate Current, $I_{G(AV)}$	25mA		50mA	
Reverse Gate Current, I_{GR}	3mA		3mA	
Reverse Gate Voltage, V_{GR}	5V		5V	
Storage Temperature Range	-65°C to +200°C			
Operating Temperature Range	-65°C to +150°C			

MECHANICAL SPECIFICATIONS

GA200 GA200A GA201 GA201A

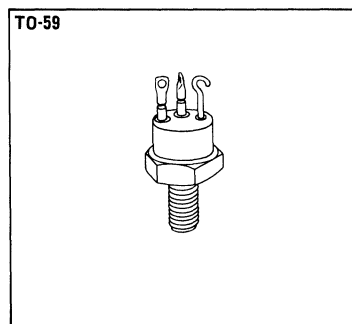
	INCHES	MILLIMETERS
A	.178-.195 DIA	4.52-4.95 DIA.
B	.170-.210	4.31-5.33
C	5 MIN	12.70 MIN
D	.209-.230 DIA	5.31-5.84 DIA.
E	.017 ± .002 DIA .001 DIA	.432 ± .051 .025
F	.020 MAX.	.508 MAX.
G	100± 010 DIA	2.54± 254 DIA
H	041± 005	1.04± 127
J	.028-.048	.711-1.22



GB200 GB200A GB201 GB201A

	INCHES	MILLIMETERS
A	.400-.455	10.16-11.56
B	.090-.150	2.28-3.81
C	.320-.468	8.13-11.88
D	.570-.763	14.48-19.38
E	.318-.380	8.07-9.65
F	.055 ± .010 .015	1.40 ± .254 .381
G	.424-.437	10.77-11.10
H	.185-.215	4.70-5.46

NOTE: Anode connected to case.



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

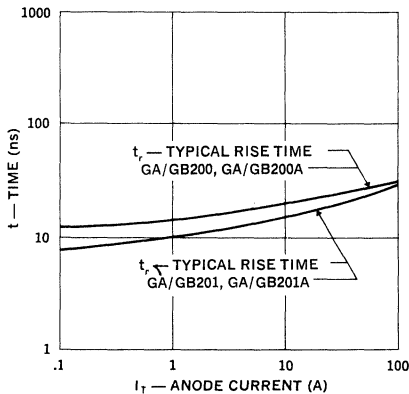
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Delay Time	t_d	—	20	30	ns	$I_G = 20mA, I_T = 1A$ $I_G = 30mA, I_T = 1A$
Rise Time GA200, 200A, GB200, 200A	t_r	—	15	25	ns	$V_D = 60V, I_T = 1A$ (1) $V_D = 60V, I_T = 30A$ (1)
Rise Time GA201, 201A, GB201, 201A	t_r	—	10	20	ns	$V_D = 100V, I_T = 1A$ (1) $V_D = 100V, I_T = 30A$ (1)
Gate Trigger on Pulse Width	$t_{pg(on)}$	—	.02	.05	μs	$I_G = 10mA, I_T = 1A$
Circuit Commutated Turn-off Time GA200, 201, GB200, 201	t_q	—	0.8	2.0	μs	$I_T = 1A, I_R = 1A, R_{EK} = 1K$
GA200A, 201A, GB200A, 201A	t_q	—	0.3	0.5	μs	
Off-State Current	I_{DRM}	—	.01	0.1	μA	$V_{DRM} = \text{Rating}, R_{EK} = 1K$
		—	20	100	μA	$V_{DRM} = \text{Rating}, R_{EK} = 1K,$ $150^\circ C$
Reverse Current	I_{RRM}	—	1.0	10	mA	$V_{RRM} = 30V, R_{EK} = 1K$ (2)
Reverse Gate Current	I_{GR}	—	.01	0.1	mA	$V_{GRM} = 5V$
Gate Trigger Current	I_{GT}	—	10	200	μA	$V_D = 5V, R_{GS} = 10K$
Gate Trigger Voltage	V_{GT}	0.4	.06	0.75	V	$V_D = 5V, R_{GS} = 100\Omega, T = 25^\circ C$
		0.10	0.2	—	V	$T = +150^\circ C$
On-State Voltage	V_T	—	1.1	1.5	V	$I_T = 2A$
Holding Current	I_H	0.3	2.0	5.0	mA	$V_D = 5V, R_{EK} = 1K, T = 25^\circ C$
		0.05	0.2	—	mA	$T = +150^\circ C$
Off-State Voltage-Critical Rate of Rise	dv/dt	20	40	—	V/ μs	$V_D = 30V, R_{EK} = 1K$

Notes: 1. $I_G = 10mA$; Pulse Test, Duty Cycle <1%.

2. Pulse test intended to guarantee reverse anode voltage capability for pulse commutation. Device should not be operated in the Reverse blocking mode on a continuous basis.

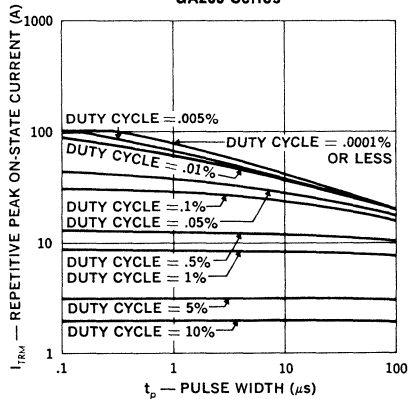
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**Switching Speed (Typical)
GA/GB200 Series**



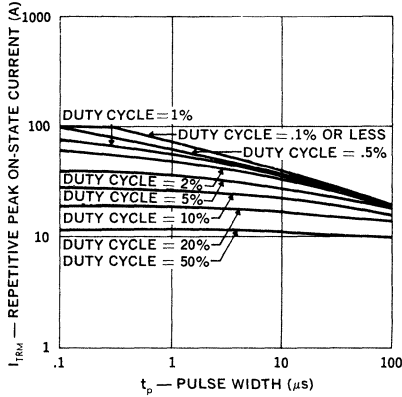
NOTES: 1. $V_D = \text{Rated } V_{DRM}$
2. $T_A = 25^\circ C$
3. $I_G = 20mA$
4. $t_d = 20ns$ TYPICALLY FOR ALL TYPES INDEPENDENT OF ANODE CURRENT

**Peak Current vs. Pulse Width
GA200 Series**



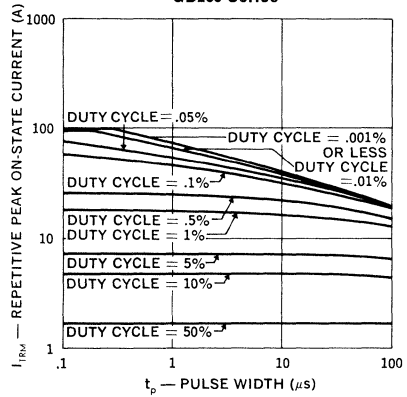
NOTES: 1. DATA BASED ON ON-STATE VOLTAGE GRAPH AT $T_A = 150^\circ C$. BLOCKING VOLTAGE MAY BE APPLIED IMMEDIATELY AFTER TERMINATION OF CURRENT PULSE.
2. $T_A = 75^\circ C$

Peak Current vs. Pulse Width
GB200 Series



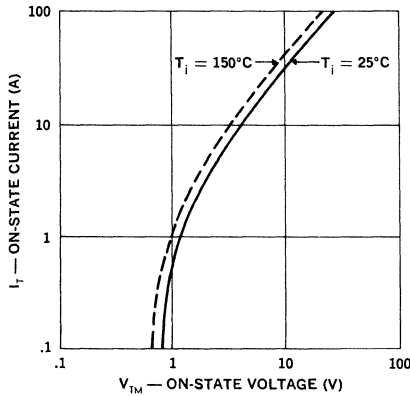
NOTES: 1. DATA BASED ON ON-STATE VOLTAGE GRAPH AT $T_J = 150^\circ\text{C}$. BLOCKING VOLTAGE MAY BE APPLIED IMMEDIATELY AFTER TERMINATION OF CURRENT PULSE.
2. $T_C = 75^\circ\text{C}$

Peak Current vs. Pulse Width
GB200 Series

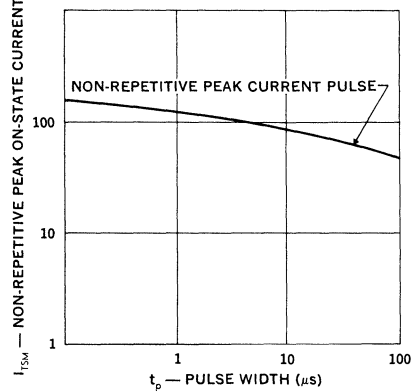


NOTES: 1. DATA BASED ON ON-STATE VOLTAGE GRAPH AT $T_J = 150^\circ\text{C}$. BLOCKING VOLTAGE MAY BE APPLIED IMMEDIATELY AFTER TERMINATION OF CURRENT PULSE.
2. $T_A = 75^\circ\text{C}$

On-State Current vs. Voltage
GA/GB200 Series



Surge Rating Maximum
GA/GB200 Series



NOTES: 1. BLOCKING VOLTAGE MAY NOT BE APPLIED FOR .001 SEC. AFTER TERMINATION OF SURGE PULSE AS JUNCTION TEMPERATURE WILL EXCEED 150°C .
2. $T_C = 75^\circ\text{C}$

SCRs

Commercial Nanosecond Switching Planar

GA300 GB300
 GA300A GB300A
 GA301 GB301
 GA301A GB301A

FEATURES

- Rise Time: 10ns
- Delay Time: 10ns
- Recovery Time: 0.5 μ s
- Pulse Current: to 100A
- Turn-on with 20ns, 10mA gate pulse

DESCRIPTION

Unitrode's Nanosecond Thyristor Switch combines the turn-on speed of logic level transistors with the high current switching capability inherent in SCRs. With this device, engineers can now design circuits capable of switching pulse currents of 1A in less than 10ns or up to 30A in less than 20ns.

The GA300, GB300 Series is specifically designed for use as the switching element in high speed laser diode pulse drivers. Other applications include electronic crowbars, harmonic wave-form generators, line drivers and general purpose replacements for avalanche transistors. For applications requiring higher voltage levels, Unitrode has developed several "series string" circuits which allow the series connection of an unlimited number of devices for voltages as high as 2000V with no significant decrease in speed. These circuits are described in Unitrode's Design Note #14.

ABSOLUTE MAXIMUM RATINGS

	GA300 GA300A	GA301 GA301A	GB300 GB300A	GB301 GB301A
Repetitive Peak Off-State Voltage, V_{DRM}	60V	100V	60V	100V
Repetitive Peak On-State Current, I_{TRM}	up to 100A		up to 100A	
Peak Gate Current, I_{GM}	250mA		250mA	
Average Gate Current, $I_{G(AV)}$	25mA		50mA	
Reverse Gate Current, I_{GR}	3mA		3mA	
Reverse Gate Voltage, V_{GR}	5V		5V	
Storage Temperature Range	-65°C to +150°C			
Operating Temperature Range	0°C to +125°C			

MECHANICAL SPECIFICATIONS

GA300 GA300A GA301 GA301A

	INCHES	MILLIMETERS
A	178-195 DIA	4 52-4 95 DIA
B	170-.210	4 31-5 33
C	.5 MIN.	12.70 MIN
D	209-230 DIA.	5 31-5 84 DIA
E	017 ± .002 DIA 001 DIA	432 ± .051 .025
F	020 MAX	508 MAX
G	100 ± 010 DIA.	2 54 ± 254 DIA
H	041 ± 005	1 04 ± 127
J	028-.048	.711-1 22

TO-18

GB300 GB300A GB301 GB301A

	INCHES	MILLIMETERS
A	400-455	10 16-11 56
B	090-150	2 28-3 81
C	320-468	8 13-11 88
D	570-763	14 48-19 38
E	318-380	8 07-9 65
F	055 ± .010 015	1.40 ± .254 .381
G	424-437	10 77-11 10
H	185-215	4 70-5 46

NOTE: Anode connected to case.

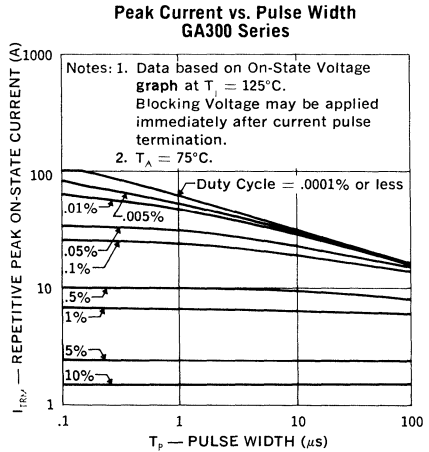
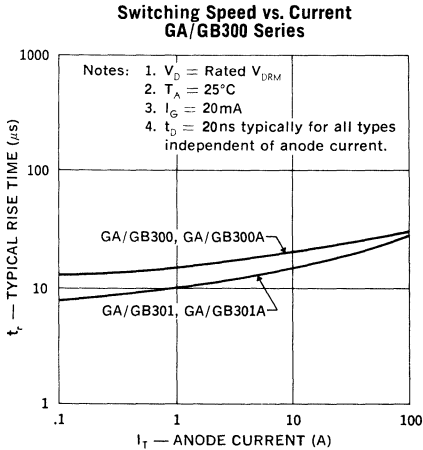
TO-59

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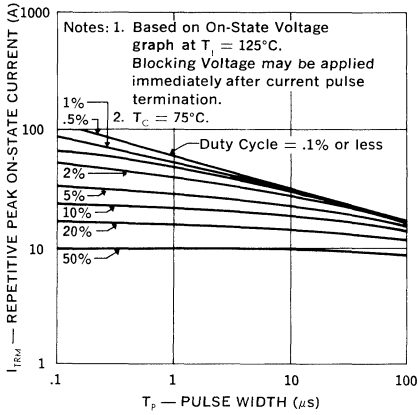
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Delay Time	t_d	—	20 10	30 —	ns	$I_G = 20\text{mA}, I_T = 1\text{A}$ $I_G = 30\text{mA}, I_T = 1\text{A}$
Rise Time (Note 1) GA300, 300A, GB300, 300A	t_r	—	15 25	25 —	ns	$V_D = 60\text{V}, I_T = 1\text{A}$ $V_D = 60\text{V}, I_T = 30\text{A}$ (Note 1)
Rise Time (Note 1) GA301, 301A, GB301, 301A	t_r	—	10 20	20 —	ns	$V_D = 100\text{V}, I_T = 1\text{A}$ $V_D = 100\text{V}, I_T = 30\text{A}$ (Note 1)
Circuit Commutated Turn-off Time GA300, 301, GB300, 301	t_q	—	0.8	2.0	μs	$I_T = 1\text{A}, I_R = 1\text{A}, R_{GK} = 1\text{K}$
GA300A, 301A, GB300A, 301A			0.3	0.5	μs	$I_T = 1\text{A}, I_R = 1\text{A}, R_{GK} = 1\text{K}$
Gate Trigger-on Pulse Width	$t_{pg(on)}$	—	0.02	0.05	μs	$I_G = 10\text{mA}, I_T = 1\text{A}$
Off-state Current	I_{DRM}	—	0.01 20	0.1 100	μA	$V_{DRM} = \text{Rating}, R_{GK} = 1\text{K}, T = 25^\circ\text{C}$ $V_{DRM} = \text{Rating}, R_{GK} = 1\text{K}, T = 125^\circ\text{C}$
Reverse Current (Note 2)	I_{RRM}	—	1.0	10	mA	$V_{RRM} = 30\text{V}, R_{GK} = 1\text{K}$ (Note 2)
Gate Trigger Voltage	V_{GT}	0.4 0.10	0.6	0.75	V	$V_D = 5\text{V}, R_{GS} = 100\Omega, T = 25^\circ\text{C}$
			0.2	—	V	$V_D = 5\text{V}, R_{GS} = 100\Omega, T = 125^\circ\text{C}$
Gate Trigger Current	I_{GT}	—	10	200	μA	$V_D = 5\text{V}, R_{GS} = 10\text{K}$
On-state Voltage	V_T	—	1.1	1.5	V	$I_T = 2\text{A}$
Off-state Voltage — Critical Rate of Rise	dv/dt	15	30	—	V/ μs	$V_D = 30\text{V}, R_{GK} = 1\text{K}$
Reverse Gate Current	I_{GR}	—	0.01	0.1	mA	$V_{GR} = 5\text{V}$
Holding Current	I_H	0.3 0.05	2.0	5.0	mA	$V_D = 5\text{V}, R_{GK} = 1\text{K}, T = 25^\circ\text{C}$
			0.4	—	mA	$V_D = 5\text{V}, R_{GK} = 1\text{K}, T = 125^\circ\text{C}$

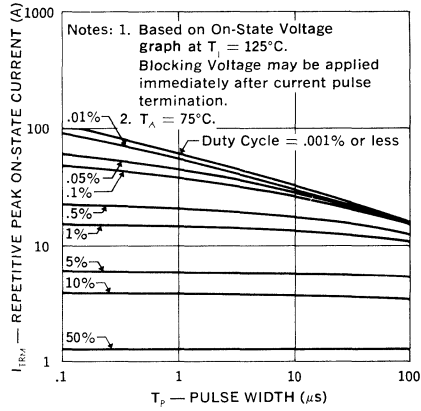
- Notes: 1. $I_G = 10\text{mA}$; Pulse Test, Duty Cycle < 1%.
2. Pulse test intended to guarantee reverse anode voltage capability for pulse commutation. Device should not be operated in the reverse blocking mode on a continuous basis.



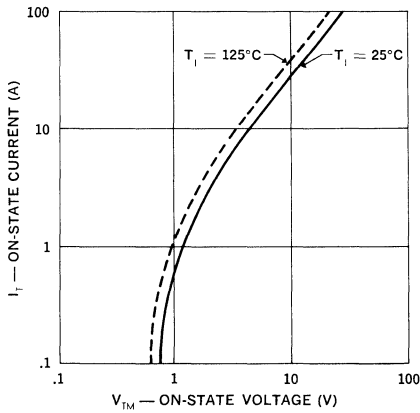
**Peak Current vs. Pulse Width
 GB300 Series**



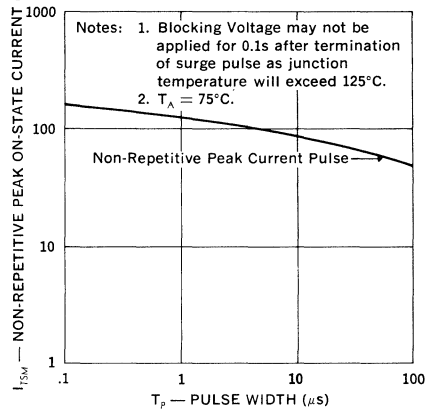
**Peak Current vs. Pulse Width
 GB300 Series**



**On-State Voltage vs. Current
 GA/GB300 Series**



**Surge Rating
 GA/GB300 Series**



SCRs

.5 Amp, Planar

ID100-ID106

FEATURES

- Voltage Ratings: to 400V
- Maximum Gate Trigger Current: 200 μ A
- Hermetically Sealed TO-18 Metal Can
- Planar Passivated Construction

DESCRIPTION

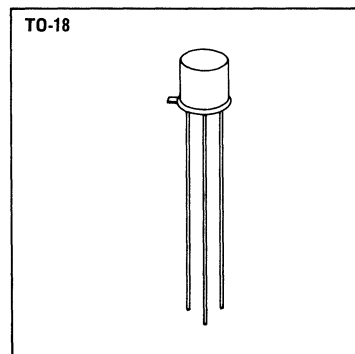
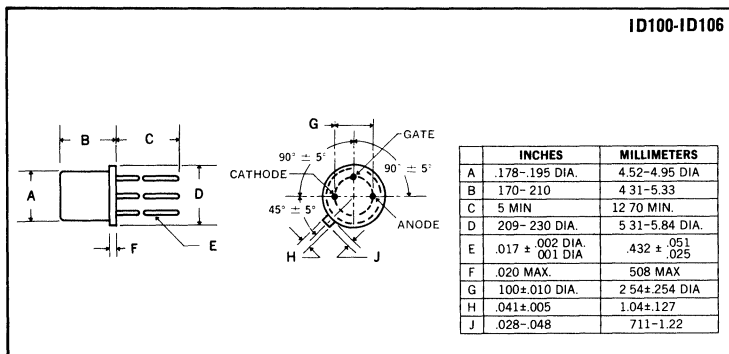
This Data Sheet describes Unitrode's line of hermetically sealed industrial SCRs designed for low-voltage, low-current sensing application. The ID100 Series is packaged in a TO-18 metal case with Unitrode's unique oxide passivated junctions, offering the highest degree of reliability and parameter stability for any device in its price range.

Typical applications include lamp driving, relay driving, sensor, pulse-generating and timing circuits.

ABSOLUTE MAXIMUM RATINGS

	ID100	ID101	ID102	ID103	ID104	ID105	ID106
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	100V	150V	200V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	30V	60V	100V	150V	200V	300V	400V
On-State Current, I_T							
75°C Ambient							250mA
100°C Case							0.5A
Repetitive Peak On-State Current, I_{TRM}							6A
Peak One Cycle Surge (Non-Rep.) On-State Current, I_{TSM}							up to 30A
Peak Gate Current, I_{GM}							250mA
Average Gate Current, $I_{G(AV)}$							25mA
Reverse Gate Voltage, V_{GR}							6V
Storage Temperature Range							-65°C to +150°C
Operating Temperature Range							-65°C to +125°C

MECHANICAL SPECIFICATIONS

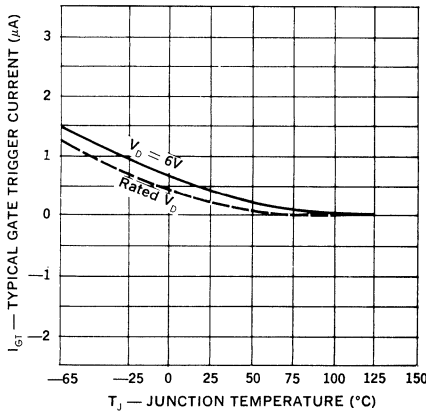


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

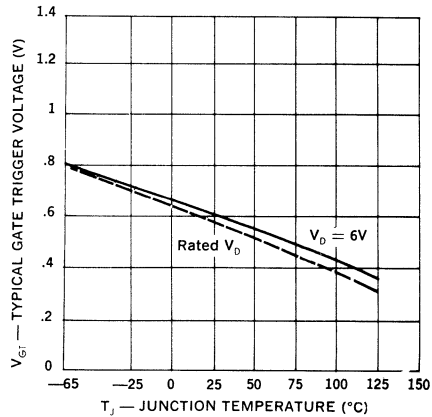
Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
Off-State Current	I_{DRM}	—	5.0 10.0	50 100	μA μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K, T = 125^\circ C, \text{ID100-ID104}$ $V_{DRM} = \text{Rating}, R_{GK} = 1K, T = 125^\circ C, \text{ID105-ID106}$
Reversing Current	I_{RRM}	—	10 15	50 100	μA μA	$V_{RRM} = \text{Rating}, R_{GK} = 1K, T = 125^\circ C, \text{ID100-ID104}$ $V_{RRM} = \text{Rating}, R_{GK} = 1K, T = 125^\circ C, \text{ID105-ID106}$
Gate Trigger Current	I_{GT}	—	5.0 —	200 500	μA μA	$V_D = 5V, R_{GS} = 10K$ $V_D = 5V, R_{GS} = 10K, T = -40^\circ C$
Gate Trigger Voltage	V_{GT}	0.4 0.10	0.55 —	0.8 1.0	V V	$V_D = 5V, R_{GS} = 100\Omega$ $V_D = 5V, R_{GS} = 100\Omega, T = -40^\circ C$ $V_D = 5V, R_{GS} = 100\Omega, T = 125^\circ C$
Peak On-State Voltage	V_{TM}	—	—	1.7	V	$I_{TM} = 1 \text{ Amp Pulse}$
Holding Current	I_H	—	1.0 —	5.0 10.0	mA mA	$R_{GK} = 1K$ $R_{GK} = 1K, T = -40^\circ C$
Turn-on Time	t_{on}	—	0.5	—	μs	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	8.0 15.0	—	μs μs	$I_T = I_R = 1A, R_{GK} = 1K, \text{ID100-ID104}$ $I_T = I_R = 1A, R_{GK} = 1K, \text{ID105-ID106}$

Note: Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1000 ohms or smaller, or other adequate bias is used.

Gate Trigger Current vs. Junction Temp.

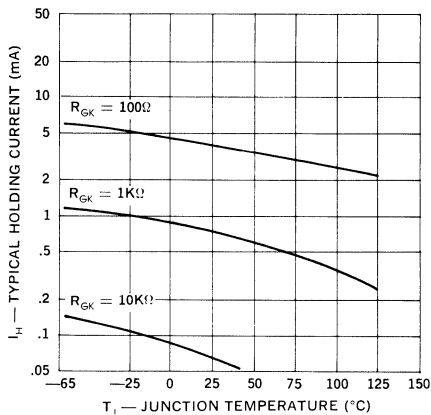


Gate Trigger Voltage vs. Junction Temp.

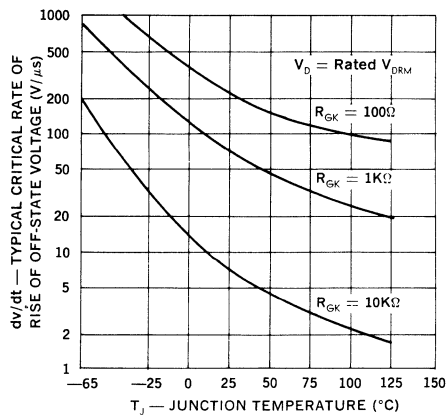


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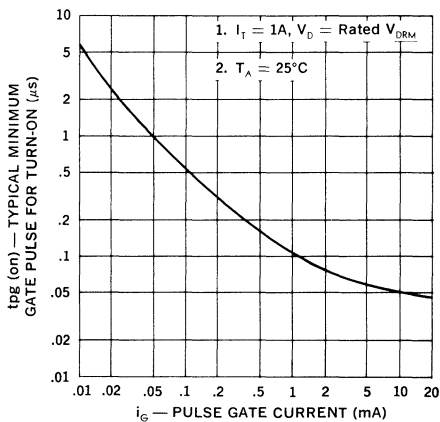
Holding Current vs. Junction Temp.



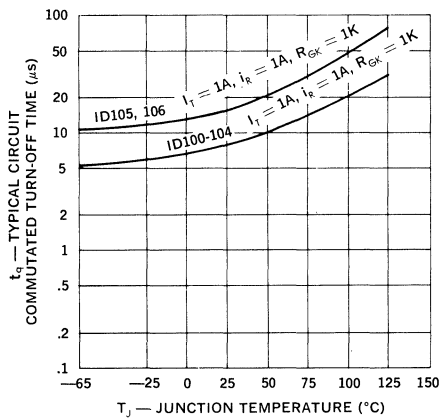
dv/dt vs. Junction Temp.



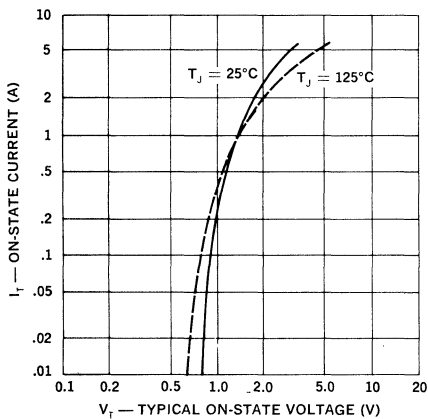
Gate Pulse for Turn-On vs. Pulse Gate Current



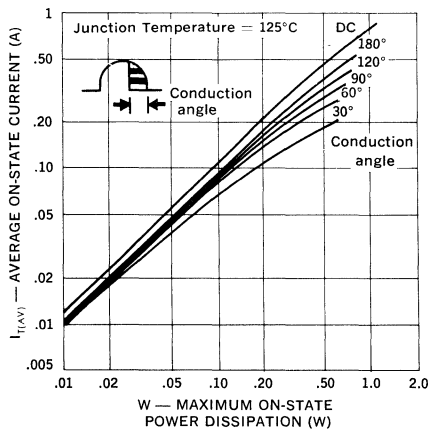
Circuit Commutated Turn-Off Time vs. Junction Temp.



Current vs. On State Voltage



Current vs. Power Dissipation



SCRs

1.6 Amp, Planar

ID200-ID203
ID300-ID301

FEATURES

- Voltage Rating: to 200V
- Max. Gate Trigger Current: 200 μ A
- Hermetically Sealed Metal Can
- Planar Passivated Construction

DESCRIPTION

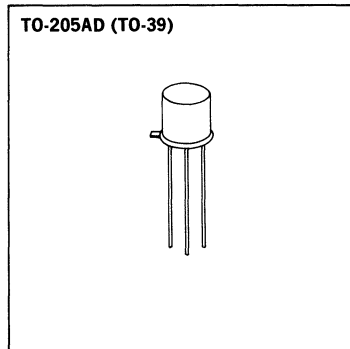
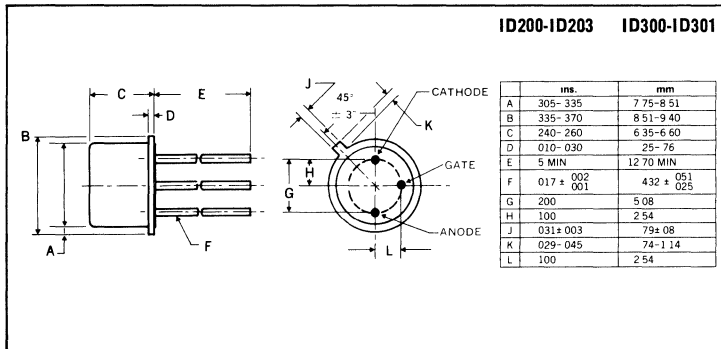
This Data Sheet describes Unitrode's line of hermetically sealed industrial SCRs designed for high-voltage, medium-current control applications. The Series is packaged in a TO-39 metal case with Unitrode's unique oxide passivated junctions to ensure reliability and parameter stability. Typical applications include relay equipment, motor controls, process controllers and pulse generators.

ABSOLUTE MAXIMUM RATINGS

	ID200	ID201	ID202	ID203	ID300	ID301
Repetitive Peak Off-State Voltage, V_{DRM}	50V	100V	150V	200V	300V	400V
Repetitive Peak Reverse Voltage, V_{RRM}	50V	100V	150V	200V	300V	400V
Non-Repetitive Peak Reverse Voltage, V_{RSM} (<5ms)	75V	150V	225V	300V	400V	500V
On-State Current, $I_{T(RMS)}$						
70°C Case					1.6A	
75°C Ambient					450mA	
Peak One Cycle Surge (Non-Repetitive) On-State Current, I_{TSM}					15A	
Repetitive Peak On-State Current, I_{TRM}					up to 30A	
Rate of Rise of On-State Current, di/dt					100A/ μ s	
I^2t (for times > 1.5 ms)					0.83A ² s	
Peak Gate Current, I_{GM}					250mA	
Average Gate Current, $I_{G(AV)}$					25mA	
Reverse Gate Voltage, V_{GR}					6V	
Storage Temperature Range					-65°C to +150°C	
Operating Temperature Range					-40°C to +110°C	

10

MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Off-State Current	I_{DRM}	—	—	10 100	μA μA	$V_{DRM} = \text{Rating}, R_{GK} = 1K, T = 25^\circ C$ $V_{DRM} = \text{Rating}, R_{GK} = 1K, T = 110^\circ C$
Reverse Current	I_{RRM}	—	—	10 100	μA μA	$V_{RRM} = \text{Rating}, R_{GK} = 1K, T = 25^\circ C$ $V_{RRM} = \text{Rating}, R_{GK} = 1K, T = 110^\circ C$
Gate Trigger Current	I_{GT}	—	—	200 500	μA μA	$V_D = 5V, R_{GS} = 10K, T = 25^\circ C$ $V_D = 5V, R_{GS} = 10K, T = -40^\circ C$
On-State Voltage	V_{GT}	0.4 0.5 0.2	0.52 0.7 —	0.8 1.0 —	V V V	$V_D = 5V, R_{GS} = 100\Omega, T = 25^\circ C$ $V_D = 5V, R_{GS} = 100\Omega, T = -40^\circ C$ $V_D = 5V, R_{GS} = 100\Omega, T = 110^\circ C$
Peak On — Voltage	V_{TM}	—	—	2.2	V	$I_T = 4 \text{ Amp Pulse}, T = 25^\circ C$
Holding Current	I_H	0.3 0.4 0.2	0.7 — —	3.0 6.0 —	mA mA mA	$R_{GK} = 1K, T = 25^\circ C$ $R_{GK} = 1K, T = -40^\circ C$ $R_{GK} = 1K, T = 110^\circ C$
Off-State Voltage — Critical Rate of Rise	dv/dt	—	20	—	V/ μs	$V_{DRM} = \text{Rated}, R_{GK} = 1K, T = 110^\circ C$
Turn-on Time	t_{on}	—	1.0	—	μs	$I_G = 10mA, I_T = I_A, V_D = 30V, T = 25^\circ C$
Circuit Commutated Turn-off Time	t_q	—	—	40	μs	$I_T = I_R = 1A, R_{GK} = 1K, T = 25^\circ C$

Note: Blocking voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1000 ohms or smaller, or other adequate bias is used.

PUTs

Planar, TO-18 Hermetic

U13T1-U13T2

FEATURES

- Voltage Ratings: to 100V
- Maximum Peak Current: 150nA
- Valley Current: as low as 25 μ A
- Low Forward Voltage Drop
- Nano-Amp Leakage
- Hermetically Sealed TO-18 Metal Can

DESCRIPTION

The Unitorde hermetically sealed TO-18 metal can series of programmable unijunction transistors feature blocking voltages to 100V, the highest available to designers. These PUTs are functionally equivalent to standard unijunction transistors, with the added advantages of programming versatility. External resistors can be added to program η , R_{BB} , I_p and I_v , depending upon your design requirements. All units are fully planar passivated. This series features a hermetically sealed TO-18 package for optimum reliability in all environmental conditions. Applications include pulse and timing circuits, SCR trigger circuits, relaxation oscillators, and sensing circuits. For further application information see Unitorde's Application Note U-66.

ABSOLUTE MAXIMUM RATINGS

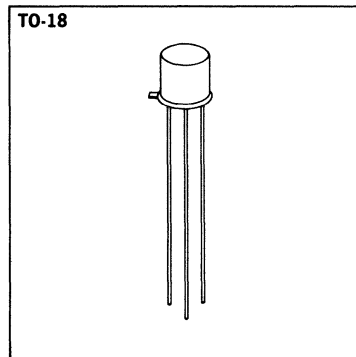
Anode-to-Cathode Forward Voltage, V_{AK}	40V
Anode-to-Cathode Reverse Voltage, V_{AKR}	40V
Gate-to-Cathode Forward Voltage, V_{GK}	40V
Gate-to-Anode Reverse Voltage, V_{GAR}	40V
Gate-to-Cathode Reverse Voltage, V_{GKR}	5V
Peak Recurrent Forward Current	
10 μ s 1% Duty Cycle	8A
100 μ s 1% Duty Cycle	5A
Power Dissipation	
25°C Ambient	400mW
Derating Factor	3.2mW/°C
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +150°C

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MECHANICAL SPECIFICATIONS

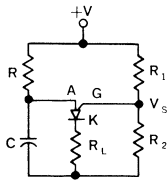
U13T1-U13T2

	INCHES	MILLIMETERS
A	178-195 DIA.	4.52-4.95 DIA.
B	170-210	4.31-5.33
C	5 MIN.	12.70 MIN.
D	209-230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 DIA .001 DIA	.432 ± .051 .025
F	.020 MAX	.508 MAX
G	100 ± .010 DIA.	2.54 ± .254 DIA
H	.041 ± .005	1.04 ± .127
J	028-048	.711-1.22

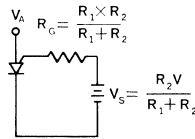


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

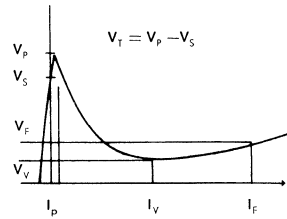
Test	Symbol	Fig.	U13T1		U13T2		Units	Test Conditions
			Min.	Max.	Min.	Max.		
Peak Current	I_p	1	—	5	—	1.0	μA	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
Valley Current	I_v	1	70	—	25	—	μA	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
Offset Voltage	V_T	1	0.2	0.6	0.2	0.6	V	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
Gate-to-Anode Leakage	I_{GAO}	2	—	10	—	10	nA	$T = 25^\circ C, V_s = \text{rating}$ $T = 75^\circ C$
Gate-to-Cathode Leakage	I_{GKS}	3	—	100	—	100	nA	$V_s = \text{rating}$
Forward Voltage	V_F	4	—	1.5	—	1.5	V	$I_F = 50mA$
Pulse Output Voltage	V_o	5	6	—	6	—	V	
Pulse Output Rate of Rise	t_r	5	—	80	—	80	nS	



a) Typical Circuit



b) Equivalent Test Circuit



c) Characteristic Curve

Figure 1

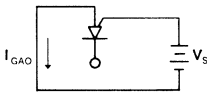


Figure 2

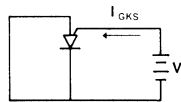


Figure 3

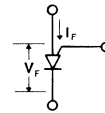


Figure 4

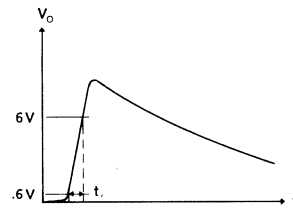
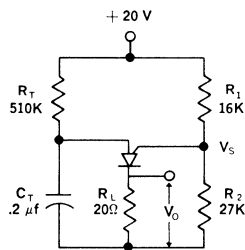


Figure 5

SWITCHING & GENERAL PURPOSE DIODES

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SWITCHING AND GENERAL PURPOSE DIODES

PRODUCT SELECTION GUIDE



SWITCHING

Type	Reverse Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Recovery Time (ns)	Junction Capacitance (pF)
1N4453	30	200	.51-.63 @ 0.1mA		30
1N4154	35	150	1.0 @ 30mA	2	4
1N251*	40	75	1.0 @ 5mA	150	
1N4152	40	150	.49-.52 @ 0.1mA	2	2
1N4450	40	200	.42-.54 @ 0.1mA	4	4
1N4451	40	200	.4-.5 @ 0.1mA	10	6
1N4452	40	200	.42-.54 @ 0.1mA	50	30
1N4444	70	200	.44-.55 @ 0.1mA	7	2
1N3064**	75	75	1.0 @ 10mA	4	2
1N4532***	75	125	1.0 @ 10mA	4	2
1N4534***	75	150	.74-.88 @ 20mA	4	2
1N4151	75	150	1.0 @ 50mA	2	2
1N4153***	75	150	.49-.55 @ 0.1mA	2	2
1N4305	75	150	.5-.575 @ .25mA	2	2
1N4446	75	150	1.0 @ 20mA	4	4
1N4447	75	150	1.0 @ 20mA	4	2
1N4448	75	150	1.0 @ 100mA	4	4
1N4449	75	150	1.0 @ 30mA	4	2
1N3600***	75	200	.54-.62 @ 1mA	4	2.5
1N4149	75	200	1.0 @ 10mA	4	2
1N4150***	75	200	.54-.62 @ 1mA	4	2.5
1N4454***	75	200	1.0 @ 10mA	2	2
1N4500***	80	300	.64-.72 @ 10mA	6	4
1N4607	85	400	1.1 @ 400mA	10	4
1N662*	100	40	1.0 @ 10mA	500	3
1N663*	100	40	1.0 @ 100mA	500	3
1N914**	100	75	1.0 @ 10mA	5	4
1N4531***	100	125	1.0 @ 10mA	5	4
1N4148***	100	200	1.0 @ 10mA	4	4
1N3070**	200	100	1.0 @ 100mA	50	5
1N4938**	200	150	1.0 @ 10mA	50	5

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GENERAL PURPOSE

Type	Reverse Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Recovery Time (ns)	Junction Capacitance (pF)
1N456	30	90	1.0 @ 40mA		
1N457*	70	75	1.0 @ 20mA		
1N483B**	80	200	1.0 @ 100mA		
1N458*	150	55	1.0 @ 7mA		
1N3595***	150	150	.83-1.0 @ 200mA	3μs	2.5
1N459*	200	40	1.0 @ 3mA		
1N643*	200	40	1.0 @ 10mA	300	3
1N485B**	200	200	1.0 @ 100mA		
1N645**	270	400	1.0 @ 400mA		20
1N647**	480	400	1.0 @ 400mA		20

* Available as JAN.
 ** Available as JAN, JANTX.
 *** Available as JAN, JANTX, JANTXV.

COMPUTER DIODE

General Purpose

JAN 1N251

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/188
- Planar Passivated Chip
- DO-7 Package
- Non-JAN Available

DESCRIPTION

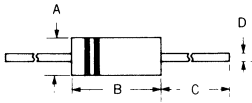
This device is particularly suited to applications where medium speed switching is required. Moisture free stability is ensured through hermetic sealing.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

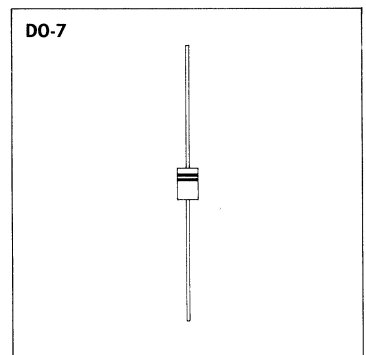
Peak Reverse Voltage	40V
Reverse Working Voltage	30V
Average Rectified Current	75mAdc
Surge Current, 1ms @ 125°C Free Air Temperature	125mA
Continuous Power Dissipation	150mW
Operating Temperature Range	-55°C to +150°C
Storage Temperature Range	-55°C to +150°C

MECHANICAL SPECIFICATIONS

JAN 1N251



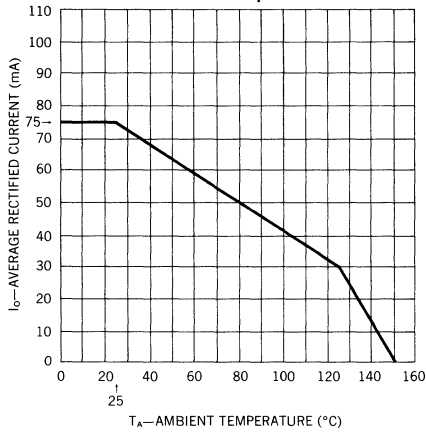
	INCHES	MILLIMETERS
A	.077 - .130	1.96 - 3.30
B	.195 - .300	4.95 - 7.62
C	1.0 - 1.5	25.4 - 38.1
D	.019 - .021	.48 - .53



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Reverse Current	Reverse Current	Reverse Current @ 125°C	Forward Voltage	Reverse Recovery Time
20 μ A @ V _R = 20V	0.1 μ A @ V _R = 10V	10 μ A @ 10V	1V @ I _F = 5mA	150ns @ I _F = 5mA, V _R = 10V R _L = 1K Ω , C _L = 10pf, I _{REC} = 0.5mA

Average Rectified Current vs. Ambient Temperature



DIODE

Low Current

1N456
 JAN 1N457
 JAN 1N458
 JAN 1N459

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/193
- Planar Passivated Chip
- DO-7 Package
- Non-JAN Available

DESCRIPTION

General purpose low current diode with high reliability characteristics

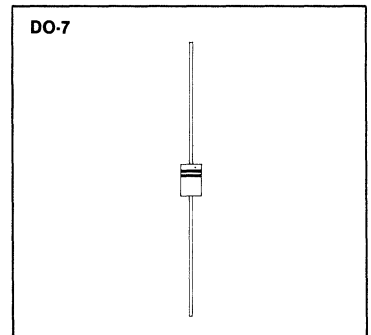
ABSOLUTE MAXIMUM RATINGS, AT 25°C

	1N456	JAN 1N457	JAN 1N458	JAN 1N459
Reverse Working Voltage	.25V	.60V	.125V	.175V
Peak Reverse Voltage	.30V	.70V	.150V	.200V
Average Output Current	.90mA	.75mA	.55mA	.40mA
Surge Current, 8.3mS	700mA	225mA	165mA	120mA
Operating Temperature Range	- 65°C to + 150°C			
Storage Temperature Range	- 65°C to + 200°C			

MECHANICAL SPECIFICATIONS

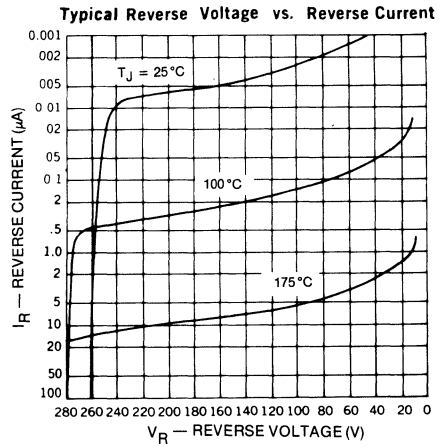
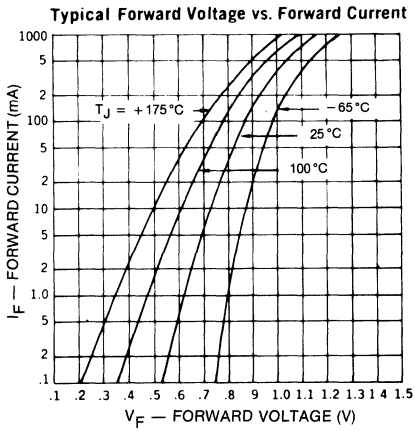
1N456
 JAN 1N457, 1N458, 1N459

	INCHES	MILLIMETERS
A	.085 - .130	2.16 - 3.30
B	.230 - .300	5.84 - 7.62
C	1.0 - 1.5	25.40 - 38.10
D	.018 - .022	46 - 56



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Forward Voltage	Reverse Current	Reverse Current @ T _A = 150°C	Peak Reverse Voltage @ 100μA
1N456	1.0V @ 40mA	25nA @ 25V	5μA @ 25V	30V
1N457, J	1.0V @ 20mA	25nA @ 60V	5μA @ 60V	70V
1N458, J	1.0V @ 7mA	25nA @ 125V	5μA @ 125V	150V
1N459, J	1.0V @ 3mA	25nA @ 175V	5μA @ 175V	200V



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DIODE

General Purpose Low Current

JAN & JANTX 1N483B
JAN & JANTX 1N485B

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/118
- Planar Passivated Chip
- DO-7 Package
- Non-JAN Available

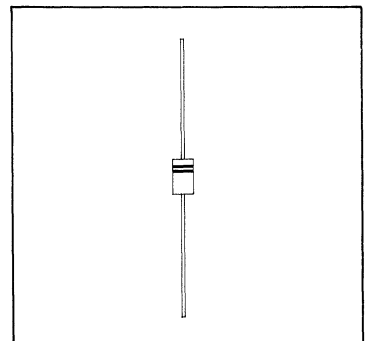
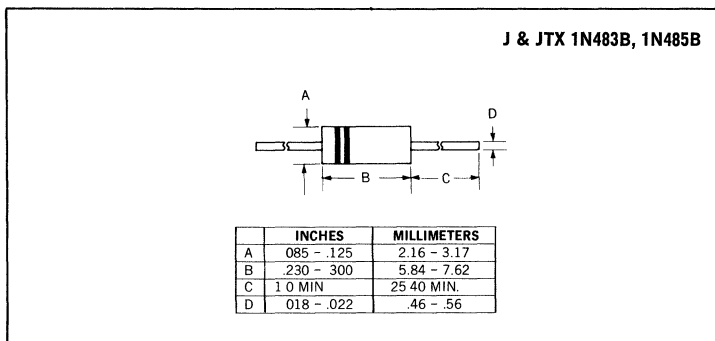
DESCRIPTION

This Series is useful in low current rectifying applications for military, industrial and commercial equipment.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

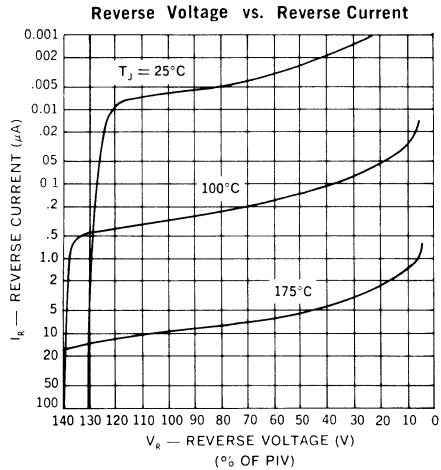
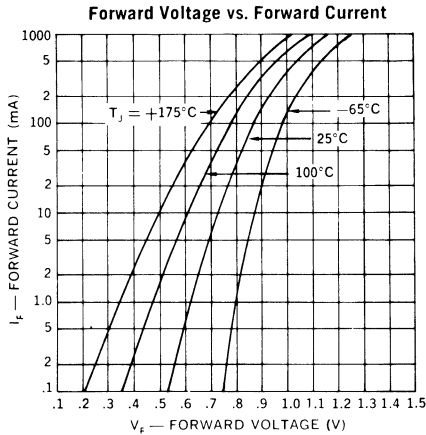
	1N483B	1N485B
Reverse Breakdown Voltage	80V	200V
Peak Working Voltage	70V	180V
Average Output Current @ $T_A = 25^\circ\text{C}$	200mA	
$T_A = 150^\circ\text{C}$	50mA	
Current Derating 1.2 mAdc/°C from 25°C to 150°C and 1.0 mAdc/°C from 150°C to 200°C		
Surge Current, 8.3mSec	2 Amps	
Operating Temperature Range	-65°C to +200°C	
Storage Temperature Range	-65°C to +200°C	

MECHANICAL SPECIFICATIONS

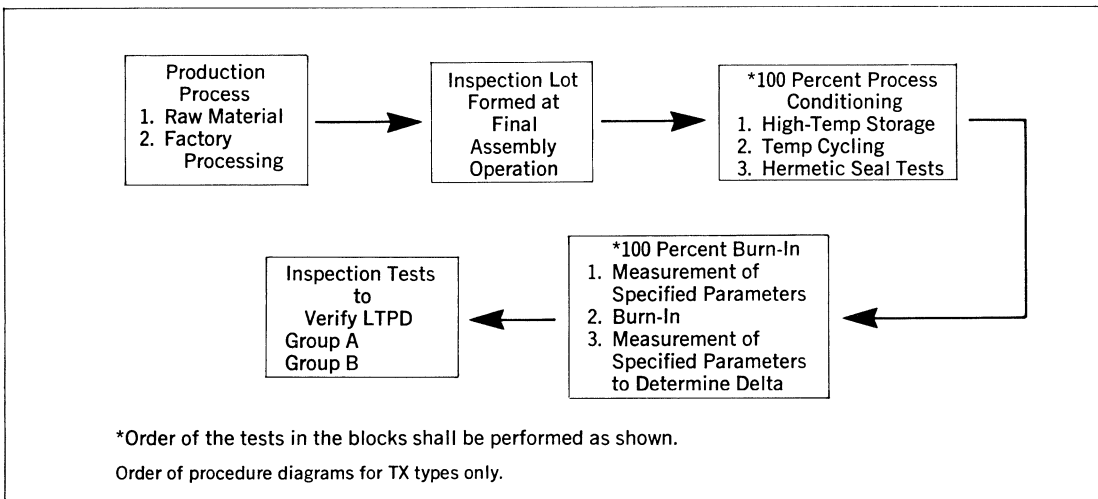


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Reverse Current @ 25°C	Reverse Current @ 25°C	Reverse Current @ 150°C	Forward Voltage @ 100mAdc, 8.5msec dc = 2% MAX.
1N483B	25nA @ 70Vdc	100 μA(pk) @ 80V(pk)	5.0 μA @ 70Vdc	1.0V(pk)
1N485B	25nA @ 180Vdc	100 μA(pk) @ 200V(pk)	5.0 μA @ 180Vdc	



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COMPUTER DIODE

Switching

JAN 1N643
 JAN 1N662
 JAN 1N663

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/256
- Planar Passivated Chip
- DO-7 Package

DESCRIPTION

This device is particularly suited to applications where medium speed switching is required. Moisture free stability is ensured through hermetic sealing.

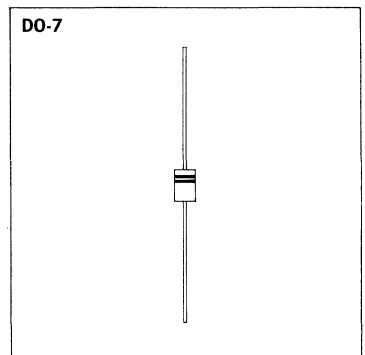
ABSOLUTE MAXIMUM RATINGS, AT 25°C

	1N643	1N662	1N663
Peak Reverse Voltage	200V	100V	100V
Reverse Working Voltage	175V	80V	80V
Average Rectified Current	40mAdc	40mAdc	60mAdc
Surge Current, 8.3ms		500mA	
Operating Temperature Range	-65°C to +150°C		
Storage Temperature Range	-65°C to +175°C		

MECHANICAL SPECIFICATIONS

J 1N643, 1N662, 1N663

	INCHES	MILLIMETERS
A	.077 - .130	1.96 - 3.30
B	.195 - .300	4.95 - 7.62
C	1.0 - 1.5	25.4 - 38.1
D	.019 - .021	.48 - .53



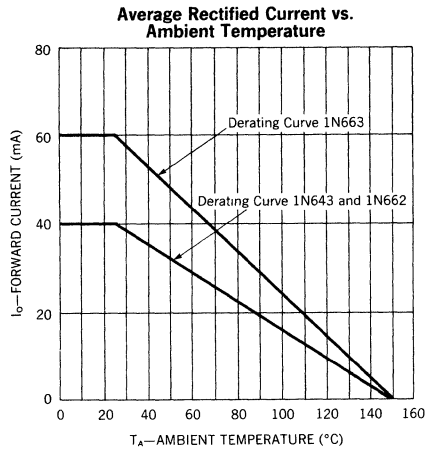
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Maximum Reverse Current @ 25°C	Maximum Reverse Current @ 25°C	Maximum Peak Reverse Current @ 25°C	Maximum Reverse Current @ 100°C	Maximum Reverse Current @ -65°C
1N643	25nAdc @ V _R = 10Vdc	1μAdc @ V _R = 100Vdc	100μA _{PK} @ V _R = 200V _{PK}	15μAdc @ V _R = 100Vdc	1μAdc @ V _R = 100Vdc
1N662	25nAdc @ V _R = 10Vdc	5μAdc @ V _R = 50Vdc	100μA _{PK} @ V _R = 100V _{PK}	100μAdc @ V _R = 50Vdc	5μAdc @ V _R = 50Vdc
1N663	25nAdc @ V _R = 10Vdc	5μAdc @ V _R = 75Vdc	100μA _{PK} @ V _R = 100V _{PK}	50μAdc @ V _R = 75Vdc	5μAdc @ V _R = 75Vdc

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Maximum Forward Voltage @ 25°C	Maximum Forward Voltage @ -65°C	Capacitance	Maximum Reverse Recovery Time
1N643	1.0Vdc @ I _F = 10mA	1.2Vdc @ I _F = 10mA	3pF @ V _R = 175V	300ns @ I _F = 5mA I _R = 17.5mA I _{REC} = 0.2nA
1N662	1.0Vdc @ I _F = 10mA	1.2Vdc @ I _F = 10mA	3pF @ V _R = 80V	500ns @ I _F = 5mA I _R = 17.5mA I _{REC} = 0.4nA
1N662	1.0Vdc @ I _F = 100mA	1.2Vdc @ I _F = 100mA	3pF @ V _R = 80V	500ns @ I _F = 5mA I _R = 17.5mA I _{REC} = 0.4nA

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RECTIFIERS

High Voltage, Low Current

JAN, JANTX 1N645, 1N647
 JAN, JANTX & JANTXV 1N645-1, 1N647-1

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/240
- Planar Passivated Chip
- DO-35 or DO-7 Package
- Non-JAN Available

DESCRIPTION

These devices are useful in general purpose low current applications in high reliability and military equipment.

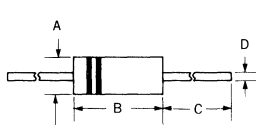
ABSOLUTE MAXIMUM RATINGS, AT 25°C

	1N645 1N645-1	1N647 1N647-1
Reverse Breakdown Voltage	270V	480V
Peak Working Voltage	225V	400V
Average Output Current, 25°C*	400mA	400mA
150°C	150mA	150mA
Surge Current, 8.3ms	5A	5A
Operating Temperature Range	-65°C to +150°C	
Storage Temperature Range	-65°C to +200°C	

*Derate 2.0mA/°C between 25°C and 150°C.

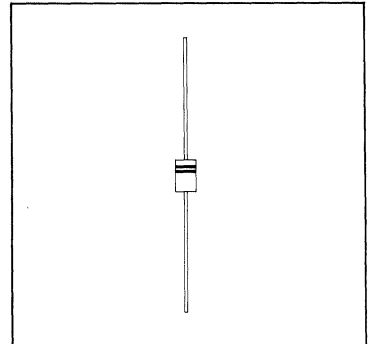
MECHANICAL SPECIFICATIONS

**J, JTX 1N645, 1N647
 J, JTX, & JTXV 1N645-1, 1N647-1**



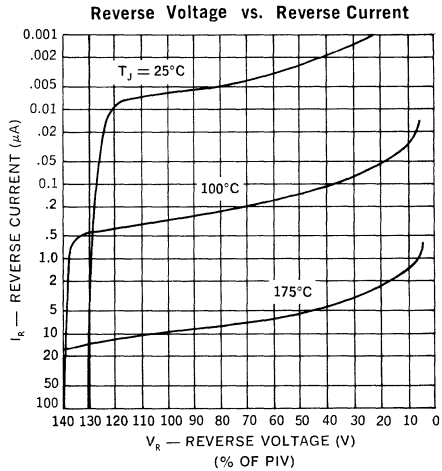
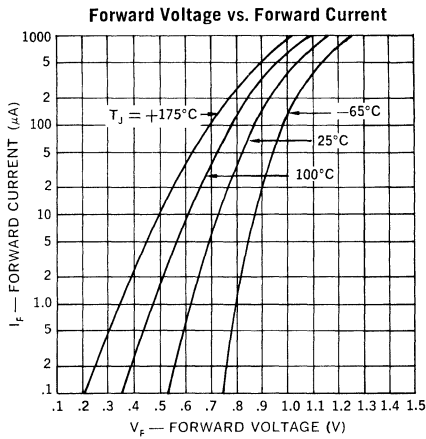
	INCHES	MILLIMETERS
A	.085 - .130	2.16 - 3.30
B	.230 - .300	5.84 - 7.62
C	1.0 MIN.	25.40 MIN.
D	.018 - .022	.46 - .56

	INCHES	MILLIMETERS
A	.055 - .130	1.40 - 3.30
B	.140 - .300	3.55 - 7.62
C	1.0 MIN.	25.40 MIN.
D	.018 - .023	.46 - .58

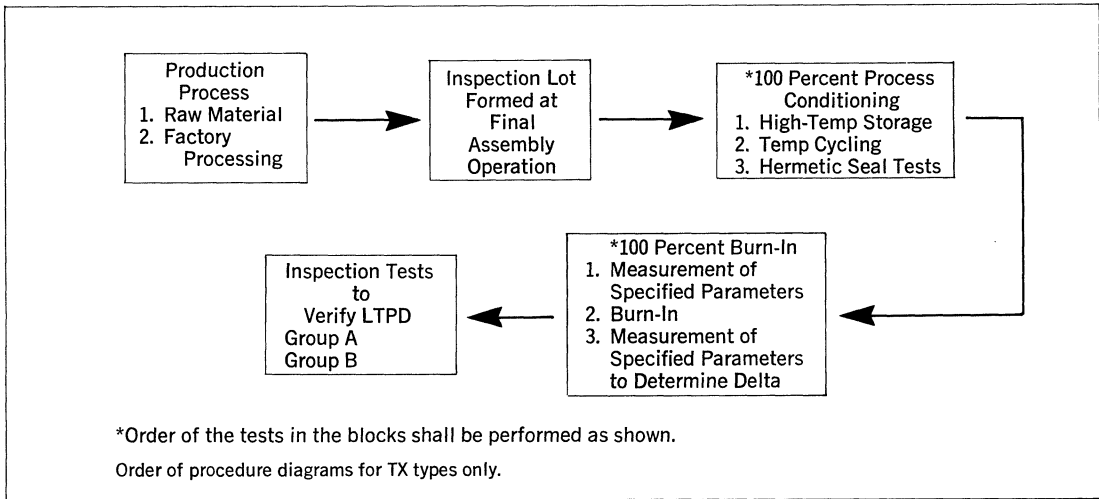


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Reverse Current @ 25°C	Reverse Current @ 50°C	Peak Reverse Current @ 25°C	Average Reverse Current @ 150°C	Forward Voltage @ 25°C	Capacitance
1N645	0.025μA @ 225Vdc	15μAdc @ 225Vdc	100μA (pk) @ 270V (pk)	100μAdc @ 225V (pk)	1.0Vdc @ I _F = 400mAdc 8.3ms	20pF V _R = 4 Vdc f = 1MHz V _{sig} = 50mV
1N645-1	0.050μA @ 225Vdc	25μAdc @ 225Vdc	100μA (pk) @ 270V (pk)	100μAdc @ 225V (pk)		
1N647	0.025μA @ 400Vdc	—	100μA (pk) @ 480V (pk)	100μAdc @ 400V (pk)		
1N647-1	0.050μA @ 400Vdc	—	100μA (pk) @ 480V (pk)	100μAdc @ 400V (pk)		



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COMPUTER DIODE

General Purpose
Switching

JAN, JANTX, 1N914
 JAN, JANTX, JANTXV 1N4148
 JAN, JANTX, JANTXV 1N4148-1
 JAN, JANTX, JANTXV 1N4531

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/116
- Planar Passivated Chip
- DO-34 or DO-35 Package
- Non-JAN Available

DESCRIPTION

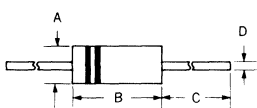
This series is very popular for general purpose switching applications in electronic equipment.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage	100V
Peak Working Voltage	75V
Average Output Current, 1N914	75mAdc
1N4148	200mAdc
1N4148-1	150mAdc
1N4531	125mAdc
Surge Current, 8.3ms	500mA
Operating Temperature Range	-65°C to +175°C
Storage Temperature Range	-65°C to +200°C

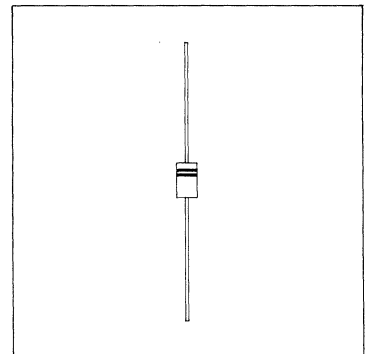
MECHANICAL SPECIFICATIONS

J, JTX 1N914
 J, JTX, JTXV 1N4148
 J, JTX, JTXV 1N4148-1
 J, JTX, JTXV 1N4531



J, JTX & JTXV 1N4531		
	INCHES	MILLIMETERS
A	.045 - .065	1.14 - 1.65
B	.080 - .110	2.032 - 2.79
C	1.0 MIN.	25.40 MIN.
D	.018 - .022	.46 - .56

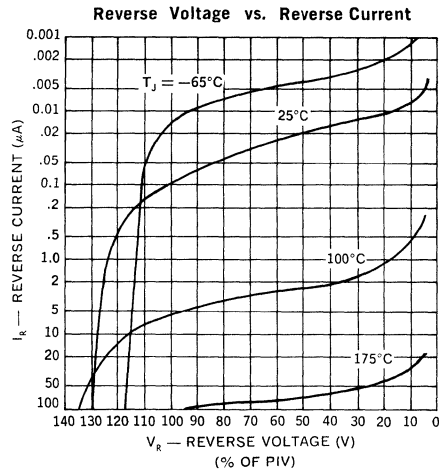
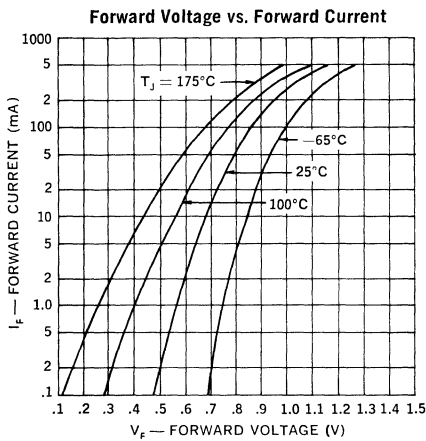
J, JTX 1N914 J, JTX & JTXV 1N4148-1		
	INCHES	MILLIMETERS
A	.056 - .075	1.42 - 1.90
B	.140 - .180	3.55 - 4.57
C	1.0 MIN.	25.40 MIN.
D	.018 - .022	.46 - .56



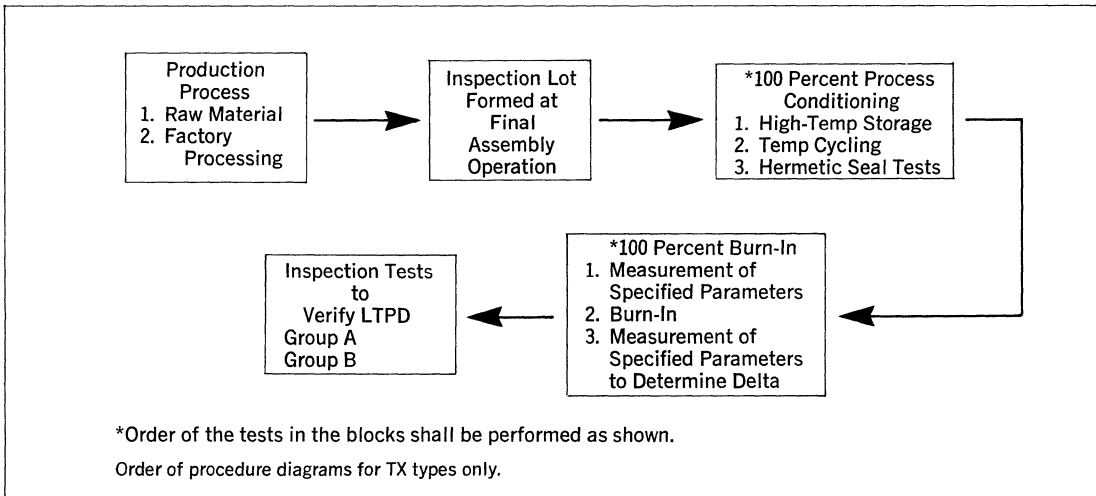
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Reverse Current @ 25°C	Reverse Current @ 25°C	Peak Reverse Current @ 25°C	Reverse Current @ 150°C	Reverse Current @ 150°C
25nAdc @ $V_R = 20Vdc$	5.0 μ Adc @ $V_R = 75Vdc$	100 μ A (pk) @ $V_R = 100V$ (pk)	50 μ Adc @ $V_R = 20Vdc$	100 μ Adc @ $V_R = 75Vdc$

Forward Voltage	Foward Recovery Voltage	Forward Recovery Time	Reverse Recovery Time	Capacitance
1.0Vdc @ $I_F = 10mAdc$	5.0V (pk) @ $I_F = 50mAdc$	20ns @ $I_F = 50mAdc$	5ns @ $I_F = I_R = 10mA$ $R_L = 100$ ohms	4.0 pF @ $V_R = 0V, f = 1$ MHz $v_{sig} = 50mV$ (pk-pk) 2.8 pF @ $V_R = 1.5V, f = 1$ MHz $v_{sig} = 50mV$ (pk-pk)



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COMPUTER DIODE

General Purpose
Switching

JAN & JANTX 1N3064
JAN, JANTX & JANTXV 1N4454
JAN, JANTX & JANTXV 1N4454-1
JAN, JANTX & JANTXV 1N4532

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/144
- Planar Passivated Chip
- DO-7, DO-34 or DO-35 Package
- Non-JAN Available

DESCRIPTION

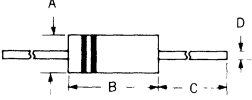
Available in DO-7, DO-34 or DO-35 packages. Unitrode offers high temperature metallurgical bond, making these devices useful in high reliability applications.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage	75V
Peak Working Voltage	50V
Average Output Current, 1N3064	75mA
1N4454,-1	200mA
1N4532	125mA
Surge Current, 1sec, 1N3064	0.5A
1N4454,-1	1A
1N4532	0.5A
Operating Temperature Range	-65°C to +175°C
Storage Temperature Range	-65°C to +200°C

MECHANICAL SPECIFICATIONS

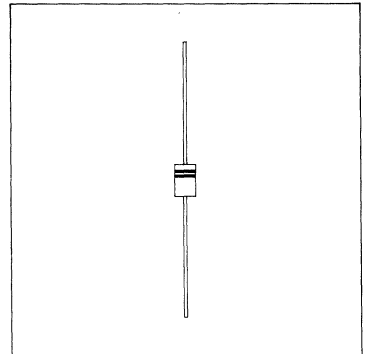
J & JTX 1N3064
J, JTX & JTXV 1N4454 & 1N4454-1
J, JTX & JTXV 1N4532



	INCHES	MILLIMETERS
A	.050 - .075	1.20 - 1.80
B	.085 - .120	2.04 - 2.88
C	1.0 MIN.	24.0 MIN.
D	.018 - .022	.46 - .56

	INCHES	MILLIMETERS
A	.078 - .107	1.98 - 2.72
B	.195 - .300	4.95 - 7.62
C	1.0 MIN.	24.0 MIN.
D	.018 - .022	.46 - .56

	INCHES	MILLIMETERS
A	.056 - .075	1.42 - 1.90
B	.140 - .180	3.55 - 4.57
C	1.0 MIN.	24.0 MIN.
D	.018 - .022	.46 - .56

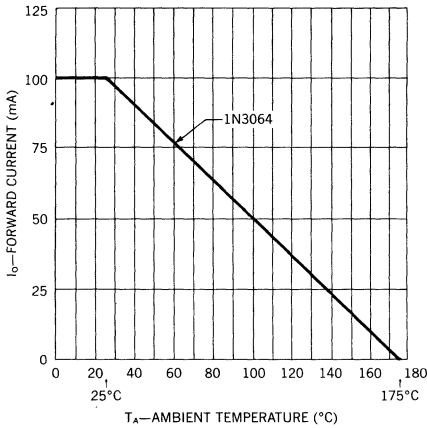


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

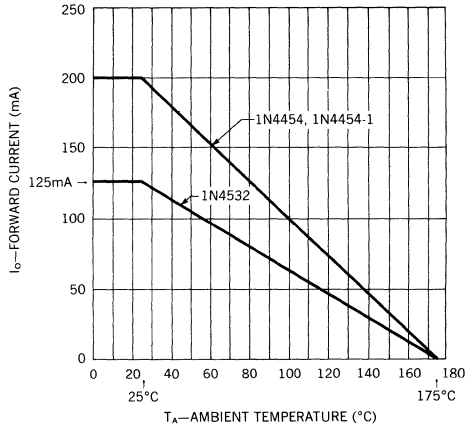
Type	Reverse Current @ 25°C	Reverse Current @ 150°C	Reverse Breakdown Voltage @ -65°C	Reverse Recovery Time	Capacitance
1N3064 1N4454 1N4454-1 1N4532	0.1μAdc @ V _R = 50V	100μAdc @ V _R = 50V	75Vdc @ I _R = 5μAdc	4ns @ I _F = I _R = 10mAdc R _L = 100 ohms c ≤ 3pF	2pF @ V _R = 0 Vdc, f = 1 MHz V _{sig} = 50mV (pk to pk)

Forward Voltage	Forward Recovery Voltage	Forward Recovery Time
1.0Vdc @ I _F = 10mAdc	5.0V (pk) @ I _F = 100mAdc t _r ≤ 0.4ns	30ns I _F = 100mAdc t _r ≤ 0.4ns

Average Rectified Current vs. Ambient Temperature for 1N3064



Average Rectified Current vs. Ambient Temperature for 1N4454,-1 and 1N4532



COMPUTER DIODE

Switching

JAN, JANTX 1N3070
 JAN, JANTX 1N4938

FEATURES

- Double-plug Construction
- Qualified to MIL-S-19500/169
- Available in DO-7 or DO-35 package

DESCRIPTION

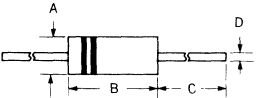
Double-plug construction affords integral positive contact by means of a thermal compression bond. Moisture free stability is ensured through hermetic sealing. The coefficients of thermal expansion of the glass case and the dumet plugs are closely matched. Hot solder dipped leads are standard.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

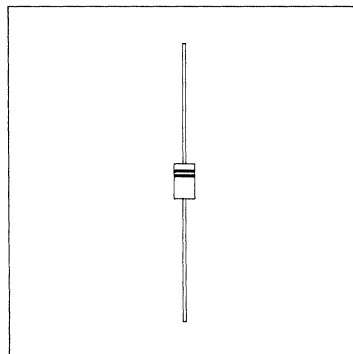
Reverse Breakdown Voltage	200V
Steady-State Forward Current at (or below) 25°C Free Air Temperature	150mA
Peak Surge Current, 1sec	500mA
Peak Surge Current, 1ms	2A
Continuous Power Dissipation at (or below) 25°C Free Air Temperature	250mW
Operating Temperature Range	-65°C to +200°C
Storage Temperature Range	-65°C to +200°C

MECHANICAL SPECIFICATIONS

J, JTX 1N3070
J, JTX 1N4938

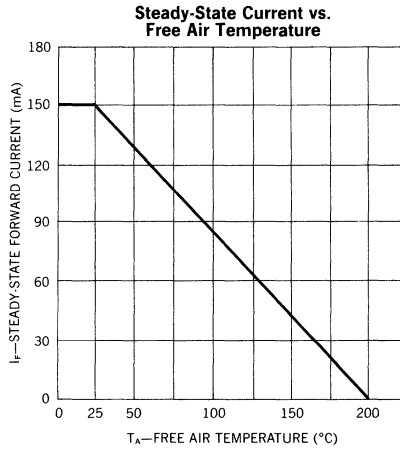


J, JTX 1N4938		J, JTX 1N3070	
	INCHES	MILLIMETERS	
A	0.65 MAX	1.65 MAX	A
B	.155 MAX.	3.94 MAX.	B
C	1.0 MIN	25.4 MIN	C
D	.020	0.51	D



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Maximum Reverse Current		Maximum Forward Voltage	Maximum Capacitance	Maximum Reverse Recovery Time
	@ 25°C	@ 150°C			
1N3070 1N4938	0.1 μ Adc @ 175Vdc	100 μ Adc @ 175Vdc	1Vdc @ $I_F = 100\text{mAdc}$	5pF @ $V_R = 0, f = 1\text{MHz}$	50ns @ $I_F = 30\text{mA}$ $I_R = 30\text{mA}$ $I_{REC} = 1\text{mA}$



COMPUTER DIODE

150 mA, Switching

JAN, JANTX, JANTXV 1N3595

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/241
- Planar Passivated Chip
- DO-7 Package
- Non-JAN Available

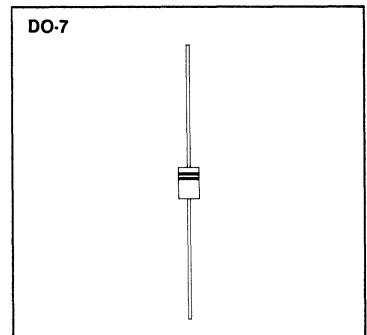
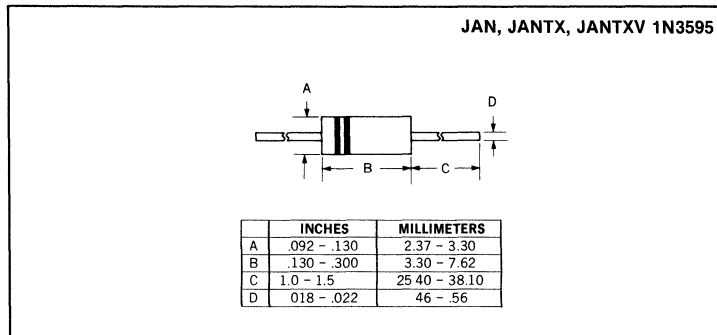
DESCRIPTION

A very useful device for medium current switching applications.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Peak Reverse Voltage	125V
Reverse Breakdown Voltage	150V
Average Output Current	150mA _{dc}
Surge Current, 1S	500mA
1 μ S	4A
Operating Temperature Range	- 65°C to + 150°C
Storage Temperature Range	- 65°C to + 200°C

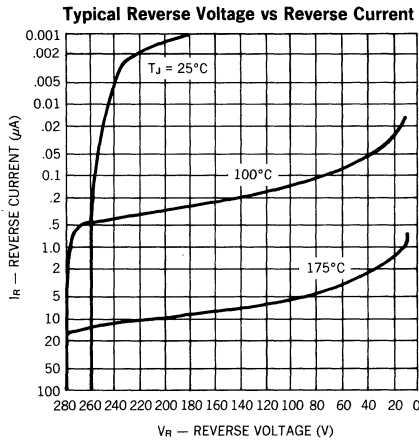
MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Limits	V_{F1} $I_F = 200\text{mA dc}$	V_{F2} $I_F = 100\text{mA dc}$	V_{F3} $I_F = 50\text{mA dc}$	V_{F4} $I_F = 10\text{mA dc}$	V_{F5} $I_F = 5\text{mA dc}$	V_{F6} $I_F = 1\text{mA dc}$
Min	0.83Vdc	0.79Vdc	0.74Vdc	0.65Vdc	0.60Vdc	0.52Vdc
Max	1.00Vdc	0.92Vdc	0.88Vdc	0.80Vdc	0.75Vdc	0.68Vdc

Limits	I_{R1} $V_R = 125\text{V dc}$	I_{R2} $V_R = 30\text{V dc}$ $T_A = 125^\circ\text{C}$	I_{R3} $V_R = 125\text{V dc}$ $T_A = 125^\circ\text{C}$	I_{R4} $V_R = 125\text{V dc}$ $T_A = 150^\circ\text{C}$	C $V_R = 0\text{V dc}$ $f = 1\text{MHz}$	t_{rr} $I_F = 10\text{mA dc}$ $V_R = 35\text{V dc}$
Min	—	—	—	—	—	—
Max	1.0nA dc	0.3 $\mu\text{A dc}$	0.5 $\mu\text{A dc}$	3.0 $\mu\text{A dc}$	8.0pF	3.0 μs



COMPUTER DIODE

200mA

Low Power, Switching

JAN, JANTX & JANTXV 1N3600
 JAN, JANTX & JANTXV 1N4150
 JAN, JANTX & JANTXV 1N4150-1

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/231
- Planar Passivated Chip
- DO-7 or DO-35 Package
- Non-JAN Available

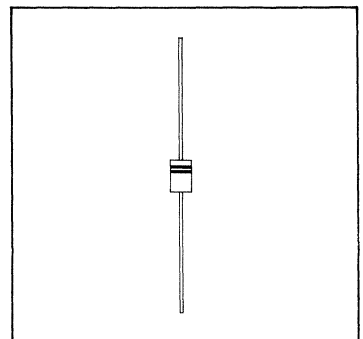
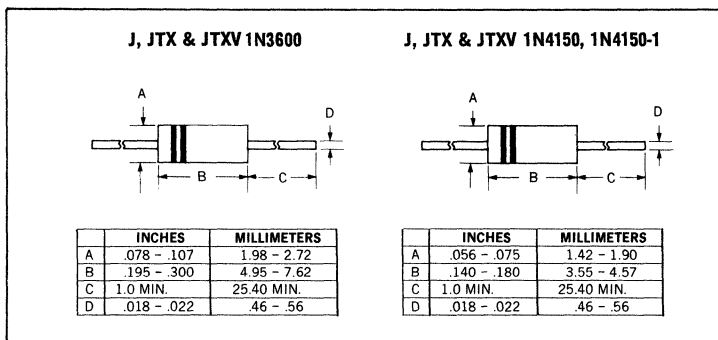
DESCRIPTION

This series of switching diodes is useful in many computer switching applications, for both military and commercial systems.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage	75V
Peak Working Voltage	50V
Average Output Current	200mA
Surge Current (1sec)	0.5A
(1 μ sec)	4.0A
Operating Temperature	-65°C to +175°C
Storage Temperature Range	-65°C to +200°C

MECHANICAL SPECIFICATIONS

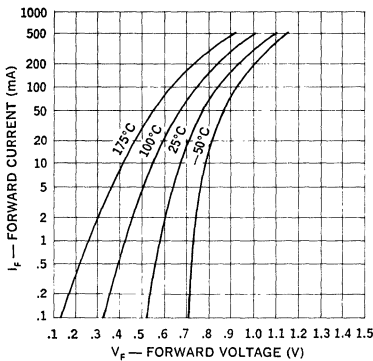


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

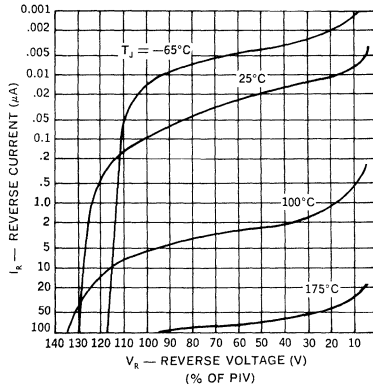
Characteristics	Forward Voltage	Forward Voltage	Forward Voltage	Forward Voltage	Forward Voltage	Reverse Breakdown Voltage
Conditions	V_{F1} $I_F = 1 \text{ mAdc}$	V_{F2} $I_F = 10 \text{ mAdc}$	V_{F3} $I_F = 50 \text{ mAdc}$ (pulse)	V_{F4} $I_F = 100 \text{ mAdc}$ (pulse)	V_{F5} $I_F = 200 \text{ mAdc}$ (pulse)	BV $I_R = 5.0 \text{ }\mu\text{Adc}$
Minimum	0.540 Vdc	0.660 Vdc	0.760 Vdc	0.820 Vdc	0.870 Vdc	75 Vdc
Maximum	0.620 Vdc	0.740 Vdc	0.860 Vdc	0.920 Vdc	1.00 Vdc	—

Characteristics	Reverse Current	Reverse Current	Junction Capacitance	Reverse Recovery Time	Reverse Recovery Time	Forward Recovery Time
Conditions	I_R $V_R = 50 \text{ Vdc}$	I_R $V_R = 50 \text{ Vdc}$ $T_A = 150^\circ\text{C}$	C $V_R = 0$ F = 1 MHz $V_{sig} = 50 \text{ mv (p-p)}$	t_{rr1} $I_F = I_R =$ 10 to 200 mAdc; $R_L = 100 \text{ ohms}$	t_{rr2} $I_F = I_R =$ 200 to 400 mAdc; $R_L = 100 \text{ ohms}$	t_{fr} $I_F = 200 \text{ mAdc};$ $t_p = 100 \text{ nsec};$ $t_r = 0.4 \text{ nsec}$
Maximum	0.1 μAdc	100 μAdc	2.5 pf	4 nsec	6 nsec	10 nsec

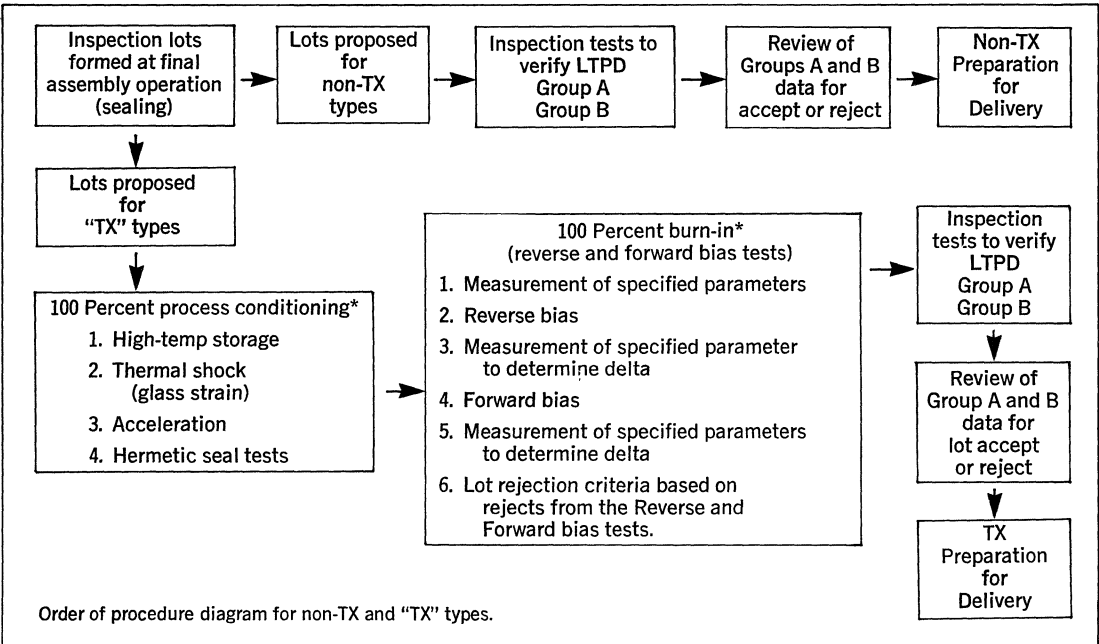
Typical Forward Current vs Voltage



Reverse Voltage vs. Reverse Current



11



COMPUTER DIODE

Switching

1N4149, 1N4151, 1N4154
 1N4446, 1N4447, 1N4448
 1N4449

FEATURES

- Metallurgical Bond
- Planar Passivated
- DO-35

DESCRIPTION

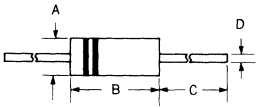
This series offers Metallurgical Bonding and is very popular for general purpose switching applications.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

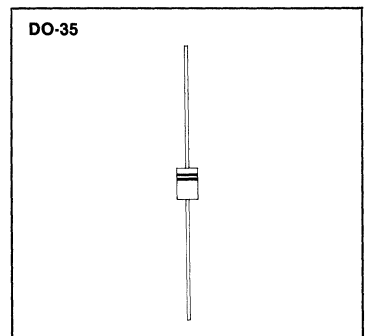
	1N4149	1N4151	1N4154	1N4446	1N4447	1N4448	1N4449
Peak Reverse Voltage	.75V	.75V	.35V	.75V	.75V	.75V	.75V
Average Rectified Current				.200mA			
Surge Current, 8.3 ms				.500mA			
Operating Temperature Range	- 65°C to + 150°C						
Storage Temperature Range	- 65°C to + 200°C						

MECHANICAL SPECIFICATIONS

**1N4149, 1N4151, 1N4154,
 1N4446, 1N4447, 1N4448
 1N4449**

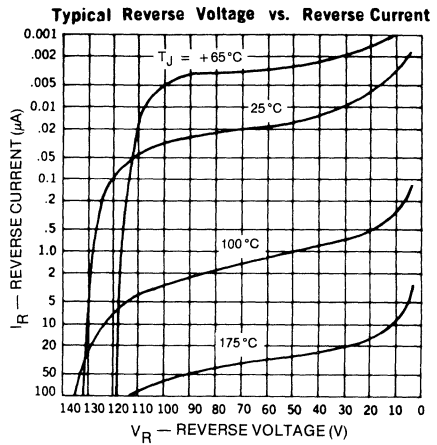
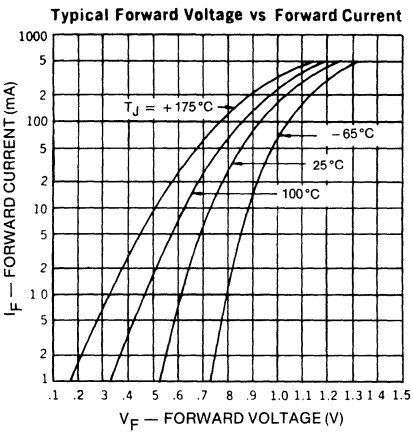


	INCHES	MILLIMETERS
A	.065	1.65
B	.155	3.94
C	1.0 MIN	25.4 MIN.
D	.020	.51



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage	Forward Voltage					Reverse Current V_R nA	Reverse Current @ 150°C V_R μ A	Junction Capacitance @ 0V	Reverse Recovery Time t_{RR}
		@ 10mA	@ 20mA	@ 30mA	@ 50mA	@ 100mA				
1N4149	75	1.0	—	—	—	—	20 25	20 50	4pF	4nS
1N4151	75	—	—	—	1.0	—	50 50	50 50	4pF	2nS
1N4154	35	—	—	1.0	—	—	25 100	25 100	4pF	2nS
1N4446	75	—	1.0	—	—	—	20 25	20 50	4pF	4nS
1N4447	75	—	1.0	—	—	—	20 25	20 50	4pF	4nS
1N4448	75	—	—	—	—	1.0	20 25	20 50	4pF	4nS
1N4449	75	—	—	1.0	—	—	20 25	20 50	2pF	4nS



COMPUTER DIODE

Switching

1N4152, 1N4305, 1N4444

FEATURES

- Metallurgical Bond
- Planar Passivated
- DO-35 Package

DESCRIPTION

This series offers Metallurgical Bonding and is very popular for general purpose switching applications.

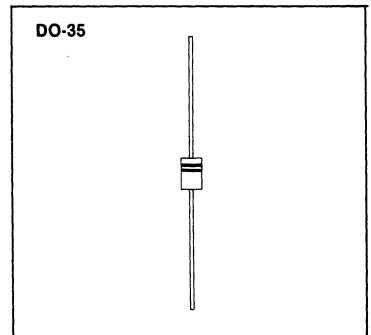
ABSOLUTE MAXIMUM RATINGS, AT 25°C

	1N4152	1N4305	1N4444
Peak Reverse Voltage	40V	75V	70V
Reverse Working Voltage	30V	50V	50V
Average Rectified Current	200mAdc		
Surge Current, 8.3 mS	500mA		
Operating Temperature Range	- 65°C to + 150°C		
Storage Temperature Range	- 65°C to + 200°C		

MECHANICAL SPECIFICATIONS

1N4152, 1N4305, 1N4444

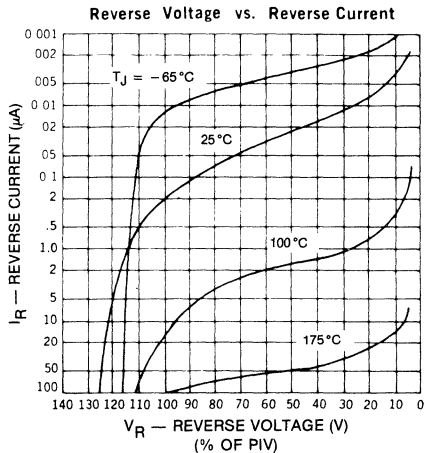
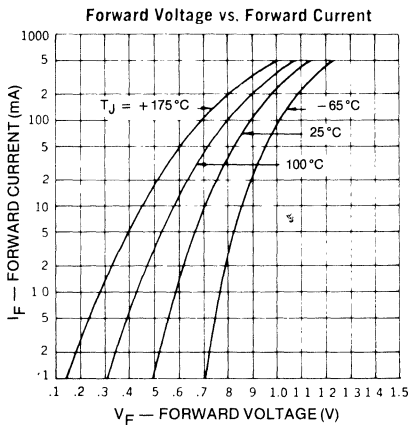
	INCHES	MILLIMETERS
A	.065 MAX.	1.65 MAX.
B	.155 MAX.	3.94 MAX.
C	1.0 MIN.	25.40 MIN.
D	.020	.51



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage (V)	Forward Voltage @ 0.1mA		Forward Voltage @ 0.25mA		Forward Voltage @ 1.0mA		Forward Voltage @ 2.0mA		Forward Voltage @ 10mA		Forward Voltage @ 20mA		Forward Voltage @ 100mA	
		min	max	min	max	min	max	min	max	min	max	min	max	min	max
1N4152	40	0.49	0.55	0.53	0.59	0.59	0.67	0.62	0.70	0.70	0.81	0.74	0.88	—	—
1N4305	75	—	—	0.505	0.575	0.55	0.65	0.61	0.71	0.70	0.85	—	—	—	—
1N4444	70	0.44	0.55	—	—	0.56	0.68	—	—	0.69	0.82	—	—	0.85	1.0

Type	Reverse Current		Reverse Current @ 150°C		Junction Capacitance @ 0V	Reverse Recovery Time t_{rr}
	V_R	(nA)	V_R	μA		
1N4152	30	50	30	50	2pF	2nS
1N4305	50	100	50	100	2pF	2nS
1N4444	50	50	50	50	2pF	7nS



11

COMPUTER DIODE

150mA

Switching Diode

JAN, JANTX & JANTXV 1N4153
 JAN, JANTX & JANTXV 1N4534

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/337
- Planar Passivated Chip
- DO-34 or DO-35 Package
- Non-JAN Available

DESCRIPTION

This device is particularly suited to applications where tightly controlled forward characteristics and fast recovery time are important.

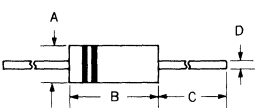
ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage	75V
Peak Working Voltage	50V
Average Output Current*	150mA
Surge Current, 1 μ s	2.0A
Operating Temperature Range	-65°C to +200°C
Storage Temperature Range	-65°C to +200°C

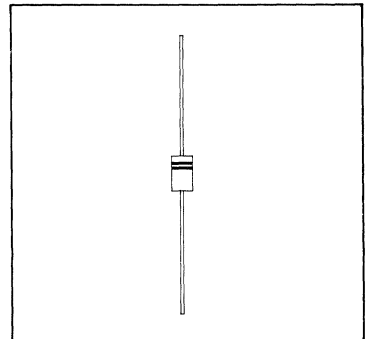
*Derate 0.86mA/c/°C for T_A above 25°C.

MECHANICAL SPECIFICATIONS

J, JTX & JTXV 1N4153
J, JTX & JTXV 1N4534



J, JTX & JTXV 1N4534		J, JTX & JTXV 1N4153	
	INCHES	MILLIMETERS	
A	.050 - .065	1.27 - 1.65	A
B	.080 - .120	2.03 - 3.05	B
C	1.0 - 1.5	25.4 - 38.1	C
D	.018 - .022	.46 - .56	D

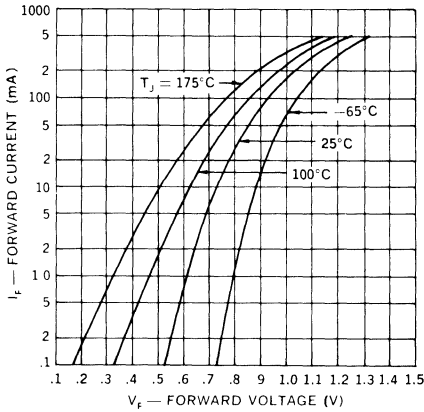


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

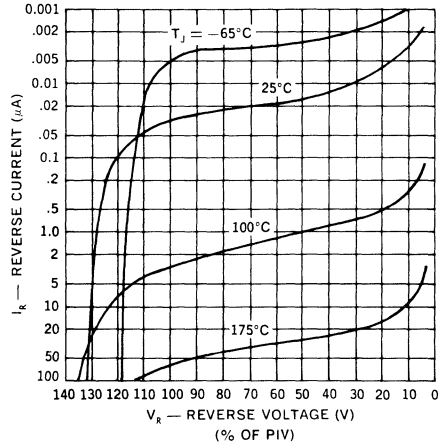
Limit	V_{F1} $I_F = 100 \mu\text{A dc}$	V_{F2} $I_F = 250 \mu\text{A dc}$	V_{F3} $I_F = 1 \text{ mA dc}$	V_{F4} $I_F = 2 \text{ mA dc}$	V_{F5} $I_F = 10 \text{ mA dc}$	V_{F6} $I_F = 20 \text{ mA dc}$
Min	0.490Vdc	0.530Vdc	0.590Vdc	0.620Vdc	0.700Vdc	0.740Vdc
Max	0.550Vdc	0.590Vdc	0.670Vdc	0.700Vdc	0.810Vdc	0.880Vdc

Limit	I_R $V_R = 50\text{V}$	I_{R2} $V_R = 50\text{V}$ $T_A = 150^\circ\text{C}$	C $V_R = 0$ $f = 1\text{MHz}$	t_{rr} $I_F = I_R = 10\text{mA dc}$ $R_L = 100 \text{ ohms}$	Reverse Breakdown Voltage $I_R = 5.0 \mu\text{A dc}$
Min	—	—	—	—	75V
Max	0.05 $\mu\text{A dc}$	50 $\mu\text{A dc}$	2.0pF	4ns	—

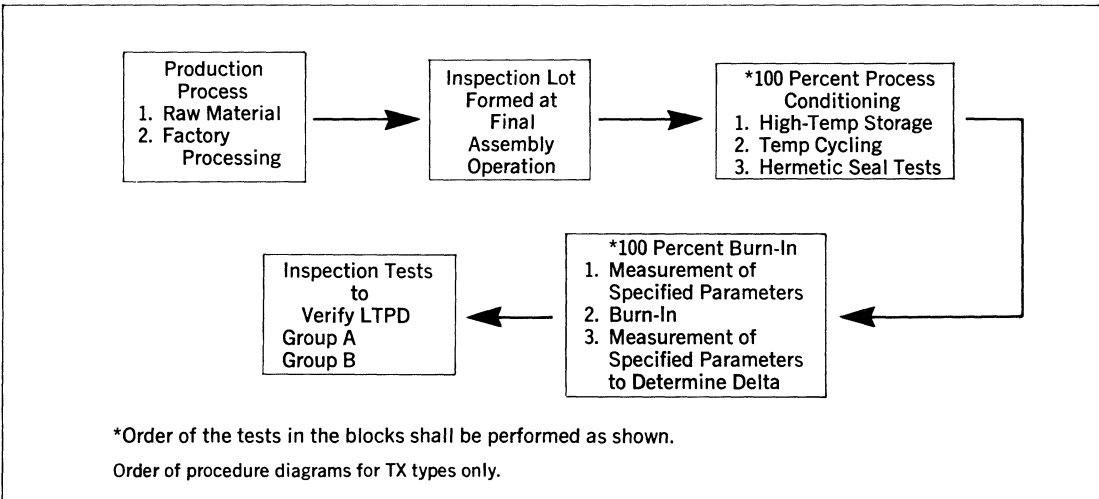
Forward Voltage vs. Forward Current



Reverse Voltage vs. Reverse Current



11



COMPUTER DIODE

Switching

1N4450, 1N4451, 1N4453

FEATURES

- Metallurgical Bond
- Planar Passivated
- DO-35 Package

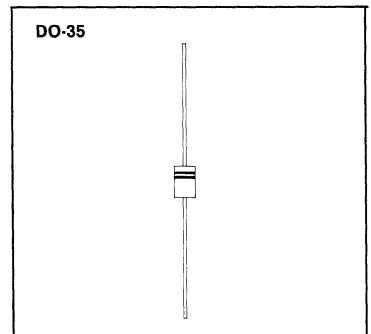
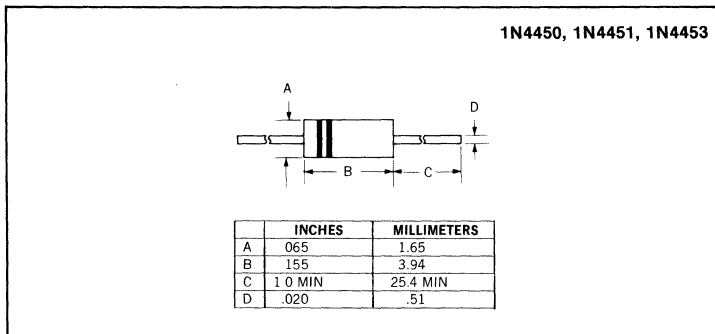
DESCRIPTION

This series offers Metallurgical Bonding and is very popular for general purpose switching applications.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

	1N4450	1N4451	1N4453
Peak Reverse Voltage	40V	40V	30V
Reverse Working Voltage	30V	30V	20V
Average Rectified Current	200mA dc		
Surge Current, 8.3 ms	500mA		
Operating Temperature Range	- 65°C to + 150°C		
Storage Temperature Range	- 65°C to + 200°C		

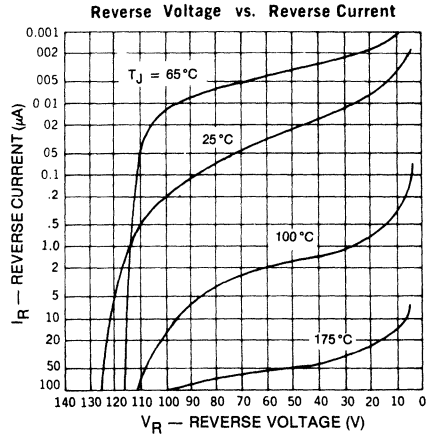
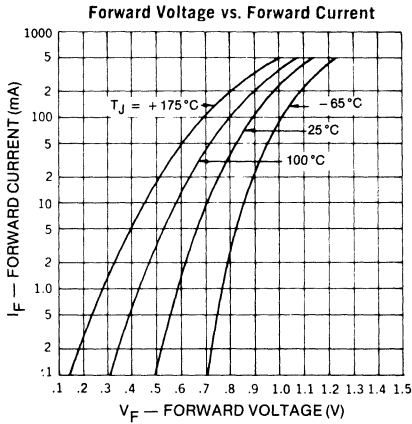
MECHANICAL SPECIFICATIONS



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Type	Peak Inverse Voltage (V)	Forward Voltage @ 0.01mA		Forward Voltage @ 0.1mA		Forward Voltage @ 1.0mA		Forward Voltage @ 10mA		Forward Voltage @ 100mA		Forward Voltage @ 200mA		Forward Voltage @ 300mA	
		min	max	min	max	min	max	min	max	min	max	min	max	min	max
1N4450	40	—	—	0.42	0.54	0.52	0.64	0.64	0.76	0.80	0.96	—	1.0	—	—
1N4451	40	—	—	0.40	0.50	0.51	0.61	0.62	0.72	0.75	0.875	—	—	—	1.0
1N4453	30	0.43	0.55	0.51	0.63	0.60	0.71	0.69	0.80	0.80	0.92	—	—	—	—

Type	Reverse Current		Reverse Current @ 150°C		Junction Capacitance @ 0V	Reverse Recovery Time t_{rr}
	V_R	(nA)	V_R	μA		
1N4450	30	50	30	50	4pF	4nS
1N4451	30	50	30	50	6pF	10nS
1N4453	20	50	20	50	30pF	—



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COMPUTER DIODE

High Conductance

1N4452, 1N4607, 1N4608

FEATURES

- Metallurgical Bond
- Planar Passivated
- High Conductance
- DO-35 Package

DESCRIPTION

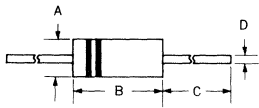
This series offers Metallurgical Bonding and is specifically designed for high conductance switching applications such as core memories.

ABSOLUTE MAXIMUM RATINGS, AT 25 °C

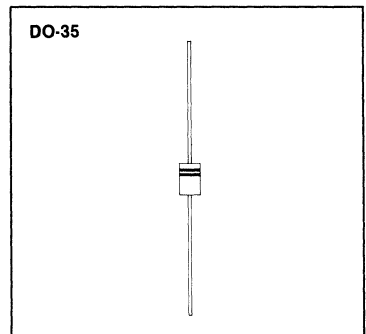
	1N4452	1N4607	1N4608
Peak Reverse Voltage	40V	85V	85V
Reverse Working Voltage	30V	50V	50V
Average Rectified Current	400mAdc		500mAdc
Surge Current, 8.3 mS		1A	
Operating Temperature Range	-65°C to +150°C		
Storage Temperature Range	-65°C to +200°C		

MECHANICAL SPECIFICATIONS

1N4452, 1N4607, 1N4608



	INCHES	MILLIMETERS
A	.065	1.65
B	.155	3.94
C	1.0 MIN.	25.4 MIN
D	.020	.51

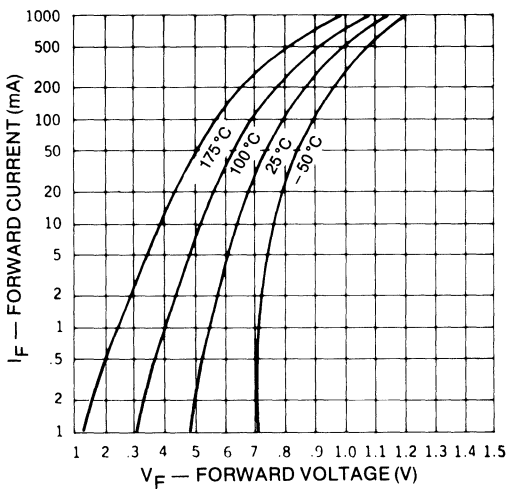


ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

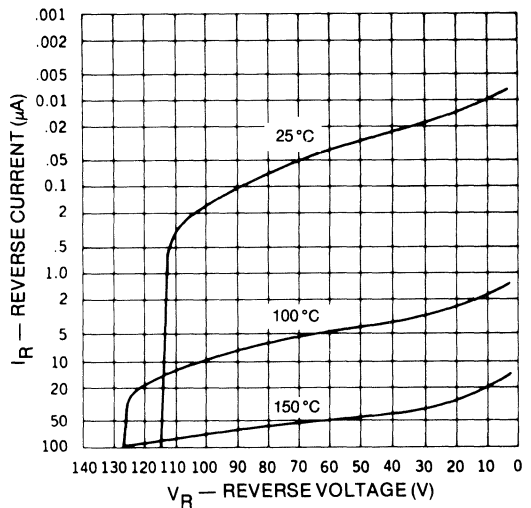
Type	Peak Inverse Voltage	Forward Voltage @ 0.1mA		Forward Voltage @ 1.0mA		Forward Voltage @ 10mA		Forward Voltage @ 100mA		Forward Voltage @ 250mA		Forward Voltage @ 350mA		Forward Voltage @ 400mA		Forward Voltage @ 500mA	
		min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
1N4452	40V	0.42	0.54	0.51	0.62	0.60	0.71	0.71	0.83	—	—	—	—	—	—	—	—
1N4607	85V	0.39	0.50	0.50	0.60	0.61	0.72	0.74	0.87	0.81	0.95	—	1.0	—	1.1	—	—
1N4608	85V	0.39	0.49	0.50	0.60	0.61	0.71	0.74	0.85	0.81	0.93	0.84	0.96	—	—	—	1.1

Type	Forward Voltage @ 600mA		Forward Voltage @ 1000mA		Reverse Current @ 0V		Reverse Current @ 100°C		Reverse Current @ 150°C		Junction Capacitance @ 0V	Reverse Recovery Time t_{rr}
	min	max	min	max	V_R	nA	V_R	μA	V_R	μA		
1N4452	—	1.0	0.90	1.2	30	50	—	—	30	50	—	50nS
1N4607	—	—	—	—	50	100	50	25	—	—	4pF	10nS
1N4608	—	—	—	—	50	100	50	25	—	—	4pF	10nS

Typical Forward Voltage vs Forward Current



Typical Reverse Voltage vs Reverse Current



11

COMPUTER DIODE

500mA
Switching Diode

JAN & JANTX 1N4500

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/403
- Planar Passivated Chip
- DO-35 Package
- Non-JAN Available

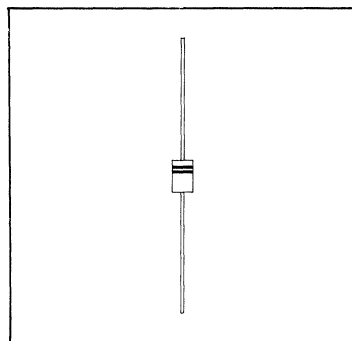
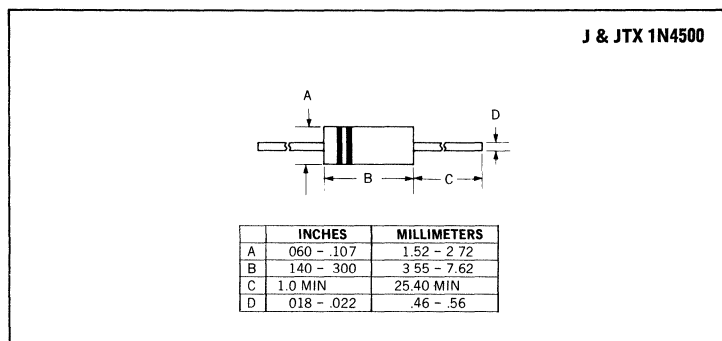
DESCRIPTION

This device is a fast switching, high conductance diode for military, space, high rel and other systems.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage	80Vdc
Peak Working Voltage	75Vpk
Average Output Current	300mA _{dc}
Surge Current, 1sec	0.5A
1 μ sec	4.0A
Operating Temperature Range	-65°C to +175°C
Storage Temperature Range	-65°C to +200°C

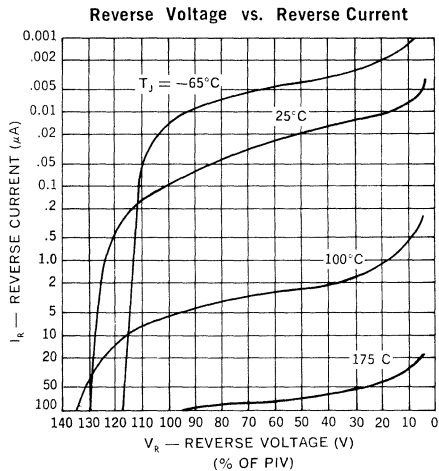
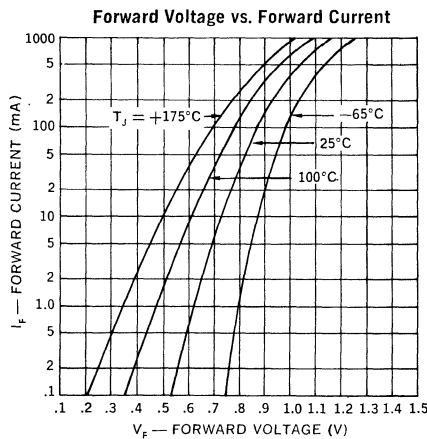
MECHANICAL SPECIFICATIONS



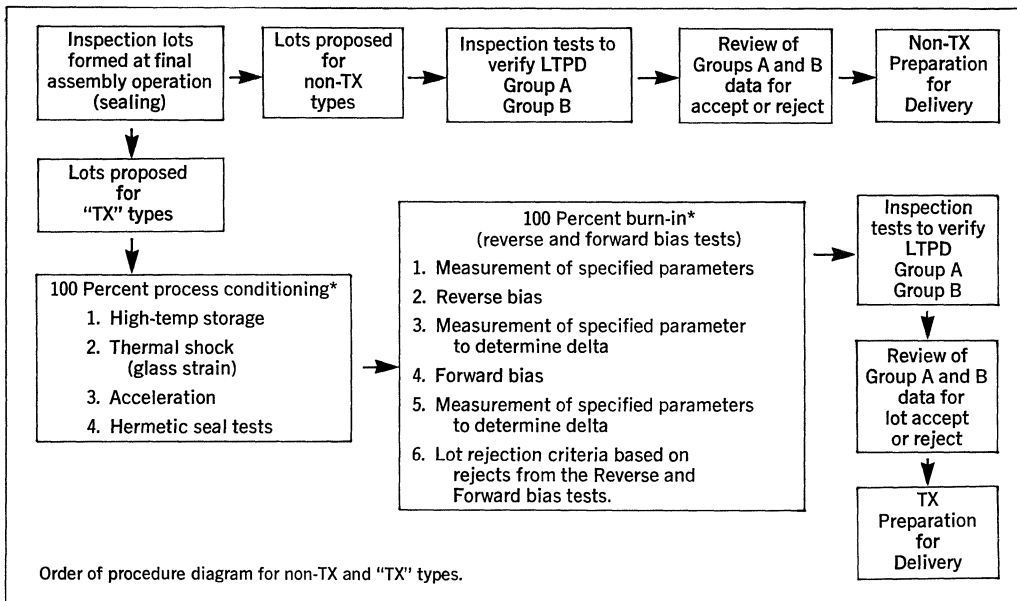
ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Limits	V_{F1} $I_F = 250\mu\text{A}$	V_{F2} $I_F = 1.0\text{mA}$	V_{F3} $I_F = 10\text{mA}$	V_{F4} $I_F = 20\text{mA}$	$V_{F5 1/}$ $I_F = 300\text{mA}$	C $V_R = 0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$ $V_{sig} = 50\text{ mv (p-p)}$
Minimum	mVdc 470	mVdc 520	mVdc 640	mVdc 670	Vdc —	pF —
Maximum	560	600	720	770	1.10	4.0

	I_R $V_R = 75\text{Vdc}$	B_V $I_R = 5\mu\text{A}$	I_R $V_R = 75\text{Vdc}$ $T_A = 150^\circ\text{C}$	t_{rr} $I_F = I_R = 10\text{ mA}$ $R_L = 100\text{ ohms}$
Minimum	nA	Vdc	μA	nsec
Maximum	100	80	100	6.0



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PIN DIODES

PRODUCT SELECTION GUIDE

For applications information, see PIN Diode Designers' Handbook and Catalog (PD-500B)

SWITCHING PIN DIODES

Type	Voltage Rating Range	Capacitance (OV, 1 GHz) C_T max.	Forward Resistance (100mA, 1 GHz) R_S max.	Parallel Resistance (100V, 1 GHz) R_p min.	Average Thermal Resistance θ_A max.	Average Power Dissipation P_A max.	Peak Power Dissipation P_p max.	Carrier Lifetime $I_F = 10mA$ τ min.
	(V)	(pF)	(Ω)	(K Ω)	($^{\circ}C/W$)	(W)	(KW)	(μS)
UM4000	100-1000	3.0	0.5	2	6	25	100	5.0
UM4900	100-600	3.0	0.5	2	4	37	100	5.0
UM6000	100-1000	0.5	1.7	15	25	6	25	1.0
UM6200	100-400	1.1	0.4	10	25	6	10	0.6
UM6600	100-1000	0.4	2.5	10	35	4	13	1.0
UM7000	100-1000	0.9	1.0	10	15	10	60	2.5
UM7100	100-800	1.2	0.6	8	15	10	35	2.0
UM7200	100-400	2.2	0.25	7	15	10	20	1.5

HIGH POWER ATTENUATOR & MODULATOR PIN DIODES

Type	Voltage Ratings Range	Total Capacitance (OV, 1 GHz) C_T max.	RF Resistance (100mA, 1 GHz) R_S max.	RF Resistance (10 μA , 1 GHz) R_S min.	Average Thermal Resistance θ_A max.	Average Power Dissipation P_A max.	Carrier Lifetime $I_F = 10mA$ τ min.
	(V)	(pF)	(Ω)	(Ω)	($^{\circ}C/W$)	(W)	(μS)
UM4300	100-1000	2.2	1.5	1000	8	18	5.0
UM7300	100-1000	0.7	3.0	3000	20	7.5	2.5

GENERAL PURPOSE PIN DIODE

Type	Voltage Rating ($I_R = 10\mu A$)	Total Capacitance (50V, 1MHz) C_T max.	RF Resistance (10 μA , 100 MHz) R_S min.	RF Resistance (20mA, 100 MHz) R_S max.	RF Resistance (100mA, 100MHz) R_S max.	Carrier Lifetime ($I_R = 10mA$) τ min.
	(V)	(pF)	(Ω)	(Ω)	(Ω)	(μS)
1N5767	100	0.4	1000 3000 typ.	8 4 typ.	2.5 1.5 typ.	1

LOW DISTORTION ATTENUATOR PIN DIODES

Type	Voltage Rating $I_R = 10\mu A$	Total Capacitance (OV, 100MHz) C_T max.	RF Resistance (100mA, 100MHz) R_S max.	RF Resistance (10 μA , 100 MHz) R_S max.	Forward Current ($R_S = 75\Omega$ $F = 100MHz$) Typ.	Carrier Lifetime ($I_F = 10mA$) Typ.
	(V)	(pF)	(Ω)	(Ω)	I_F (mA)	τ (μS)
1N5957	100	0.4	3.5	1500	1.0	2
UM9301	75	0.8	3.0	3000	1.1	4

TWO WAY RADIO ANTENNA SWITCHES

Type	Voltage Rating ($I_R = 10\mu A$)	Total Capacitance (OV, 100MHz) C_T max.	RF Resistance (50mA, 100MHz) R_F max.	Transmit Harmonic Distortion $F = 50MHz$ $I = 20mA$	Receive Third Order Distortion (Pin-10mW, 0 Bias) $FA = 50MHz$ $FB = 51MHz$ Max.	Average Power Dissipation P_A Max.
	(V)	(pF)	(Ω)	(dB)	(dB)	(W)
UM9401 and UM9402	50	1.5	1.0	-80	-60	5.5
UM9415	50	4.0	1.0	-80	60	10

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PIN DIODES

PRODUCT SELECTION GUIDE

For applications information, see PIN Diode Designers' Handbook and Catalog (PD-500B)

LOW RESISTANCE ANTENNA SWITCHES

Type	Voltage Rating ($I_R = 10\mu A$)	Total Capacitance (50V, 1MHz)	RF Resistance (10mA, 100MHz)	Forward Bias Third Order IM Distortion $I = 10mA$ $F_a = 43MHz$ $F_b = 44MHz$ max	Reverse Bias Third Order IM Distortion $V = 50V$ $F_a = 43MHz$ $F_b = 44MHz$ max	Average Power Dissipation
	(V)	C_T max (pF)	R_S max (Ω)	(dB)	(dB)	P_A max (W)
UM9701	100	1.8	.8	-90	-90	2.5

MICROSTRIP PACKAGED DIODES

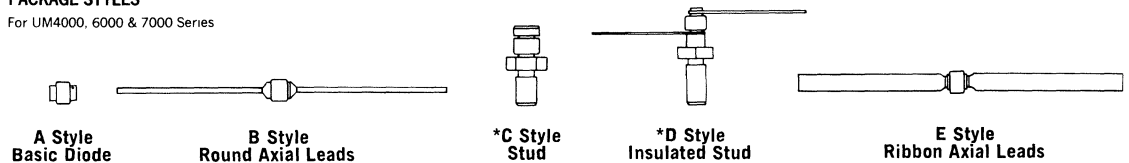
Type	Series Resistance R_S max.	Parallel Resistance R_P min.	Total Capacitance C_T max.	Carrier Lifetime τ min.	Voltage Rating	Forward Voltage V_F typ.
	(Ω)	(K Ω)	(pF)	(μs)	(V)	(V)
UM9601-UM9604	0.6	5	1.2	2.0	100, 400	.85
UM9605-UM9608	1.7	7	0.5	1.0	100, 400	.95

RADIATION DETECTOR

Type	Photocurrent 10^6 Rad (Si), 50V Sec mA min.	Photocurrent Rise Time nS Typ.	Reverse Current 50V μA max.	Capacitance F = 1 MHz, V = 50V pF max.
UM9441	4.0	10	1.0	15

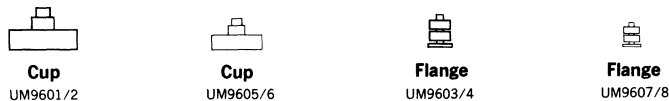
PACKAGE STYLES

For UM4000, 6000 & 7000 Series



*Not available for UM6000, UM6600, UM6200.

For UM9600 Series



Drawings are not actual size.

PIN DIODES

PRODUCT SELECTION GUIDE

For applications information, see PIN Diode Designers' Handbook and Catalog (PD-500B)

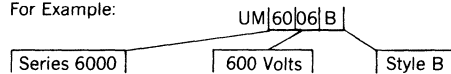
VOLTAGE RATINGS

Series	100V	200V	400V	600V	800V	1000V
UM4000	✓	✓		✓		✓
UM4300	✓	✓		✓		✓
UM4900	✓	✓		✓		
UM6000	✓	✓		✓		✓
UM6200	✓	✓	✓			
UM6600	✓	✓		✓		✓
UM7000	✓	✓		✓		✓
UM7100	✓	✓	✓		✓	
UM7200	✓	✓	✓			
UM7300	✓	✓		✓		✓

ORDERING INFORMATION

Part numbers of Switching and High Power Attenuator PIN diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the voltage rating in hundreds of volts. The remaining letters denote the package style. Reverse polarity is available for C, and D, style and denoted by adding second letter R.

For Example:



PIN DIODE

1N5767 (5082 – 3080)SERIES
1N5957 SERIES

Features

- Useful attenuation from 1 μ A to 100 mA bias.
- Capacitance below 0.4 pF.
- Low distortion in switches and attenuators.
- Rugged Unitrode construction.

Description

The 1N5767 and 1N5957 PIN diodes are based upon low capacitance PIN chips designed with long minority carrier lifetime, and thick intrinsic width. Thus operation as low as 1 MHz is possible with low distortion. Additionally, the low diode capacitance allows useful operation well into the micro-wave frequency range.

The 1N5767 (5082-3080) is a general purpose low power PIN diode designed for both

switch and attenuator applications.

The 1N5957 is primarily used as an attenuator PIN diode and is particularly suitable wherever current controlled, wide dynamic range resistance elements are required. The 1N5957 has also been characterized for the 75 Ω attenuator, commonly employed in CATV systems.

MAXIMUM RATINGS

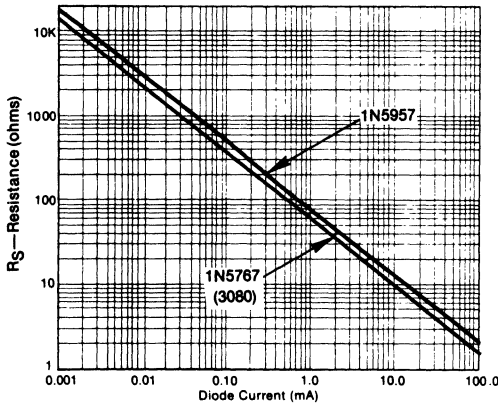
Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	100V
Average Power Dissipation: (25 °C) Free Air (P_A)	400 mW (Derate linearly to 175 °C)
Operating and Storage Temperature Range	– 65 °C to + 175 °C



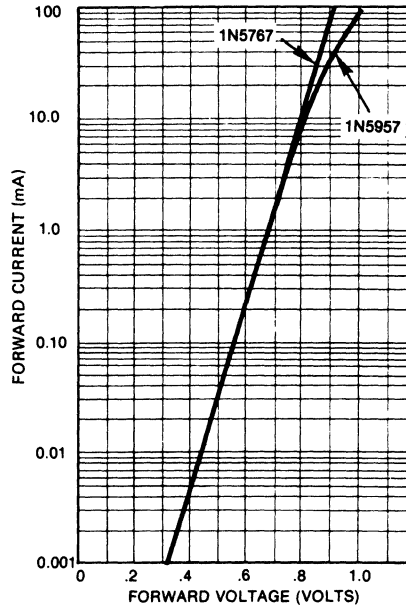
Electrical Specifications (25°C)

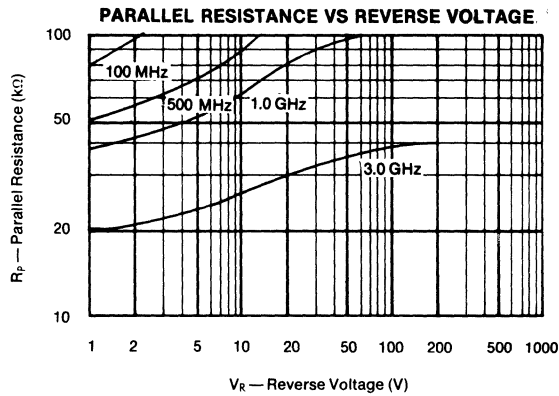
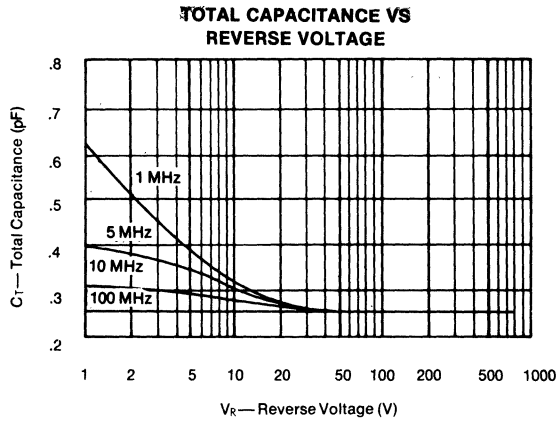
Test	Symbol	1N5767 (5082-3080)	1N5957	Conditions
Total Capacitance (Max)	C_T	0.4 pF	0.4 pF	50V, 1 MHz
Series Resistance	R_S	1000Ω(min) 2000Ω(typ)	1500Ω(min) 3000Ω(typ)	10 μA, 100 MHz
Series Resistance	R_S	8Ω(max) 4Ω(typ)	8Ω(max) 6Ω(typ)	20 mA, 100 MHz
Series Resistance	R_S	2.5Ω(max) 1.5Ω(typ)	3.5Ω(max) 2.0Ω(typ)	100 mA, 100 MHz
Carrier Lifetime (Min)	τ	1.0 μS	1.5(min) 2(typ)	$I_F = 10$ mA
Reverse Current (Max)	I_R	10 μA	10 μA	$V_R =$ Rating
Current for $R_S = 75\Omega$ (typ)	I_{75}	0.7 mA	0.8 mA - 1.2 mA	$R_S = 75\Omega$
Return Loss (typ)	—	30 dB	30 dB	Diode terminates 75Ω line
Second Order Distortion (typ)	—	-40 dB	-50 dB	Bridged tee attenuator atten. = 10 dB
Third Order Distortion (typ)	—	-60 dB	-65 dB	$P_{in} = 50$ dBmV $F_1 = 10$ MHz, $F_2 = 13$ MHz

RESISTANCE
VS FORWARD CURRENT
(TYPICAL)

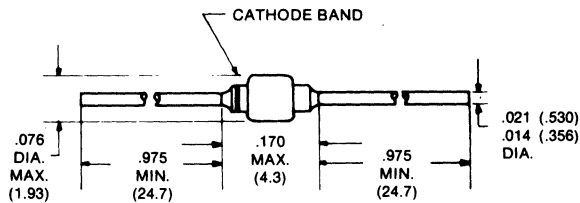


FORWARD VOLTAGE
VS FORWARD CURRENT
(TYPICAL)





MECHANICAL SPECIFICATIONS



Dimensions: Inches (Millimeters)

PIN DIODE

UM4000 SERIES
UM4900 SERIES

Features

- Power dissipation to 37.5W
- Voltage ratings to 1000V
- Series resistance rated at 0.5Ω
- Carrier lifetime greater than $5\mu\text{s}$

Description

The UM4000 and UM4900 series feature high power PIN diodes with long carrier lifetimes and thick I-regions. They are especially suitable for use in low distortion switches and attenuators, in the HF through S band frequencies. While both series are electrically equivalent, the UM4900 series have higher power ratings due to a shorter thermal path between chip and package. High charge storage and long carrier lifetime enable high RF levels to be controlled with relatively low

bias current. Similarly, peak RF voltages can be handled well in excess of applied reverse bias voltage.

Both series have been fully qualified in high power UHF phase shifters and megawatt peak-power duplexers, accumulating thousands of hours of proven performance. Both types have been used in the design of antenna selectors and couplers, where inductive and capacitive elements are switched in and out of filter or cavity networks.

MAXIMUM RATINGS

Average Power Dissipation and Thermal Resistance Ratings

Package	Condition	UM4000		UM4900	
		P_D	θ	P_D	θ
A B&E (Axial Leads)	25°C Pin Temperature	25W	6°C/W	37.5W	4°C/W
	1/2 in. (12.7mm) Overall Length to 25°C Contact	12W	12.5°C/W	12W	12.5°C/W
B&E (Axial Leads)	Free Air	2.5W	—	2.5W	—
C (Studded)	25°C Stud Temperature	25W	6°C/W	37.5W	4°C/W
D (Insulated Stud)	25°C Stud Temperature	18.75W	8°C/W	25W	6°C/W

Peak Power Dissipation Rating

All Packages	1 μs Pulse (Single) at 25 °C Ambient	100 KW
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Operating and Storage Temperature Range: -65°C to +175°C

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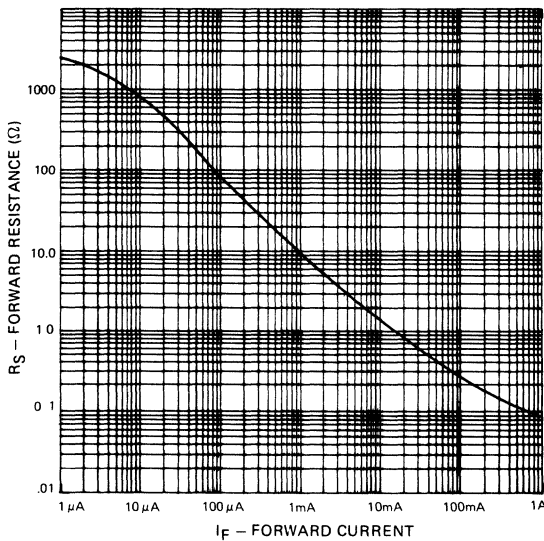
Voltage Ratings (25 °C)

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu$ Amps)	Types	
100	UM4001	UM4901
200	UM4002	UM4902
400	—	—
600	UM4006	UM4906
1000	UM4010	—

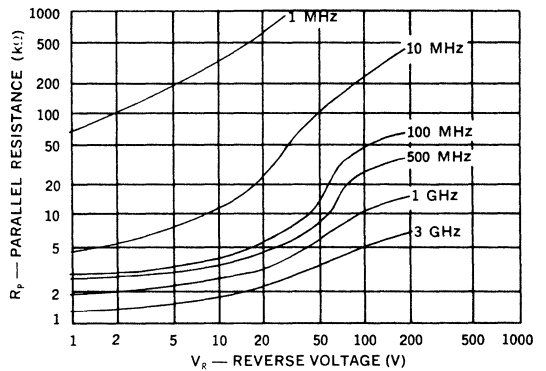
Electrical Specifications (25 °C)

Test	Symbol	UM4000 UM4900	Conditions
Total Capacitance (Max)	C_T	3 pF	0V, 1 GHz
Series Resistance (Max)	R_S	0.5Ω	100 mA, 1 GHz
Parallel Resistance (Min)	R_P	2 KΩ	100V, 1 GHz
Carrier Lifetime (Min)	τ	5μs	$I_F = 10$ mA
Reverse Current (Max)	I_R	10μA	$V_R =$ Rating
I-Region Width (Min)	W	150μm	—

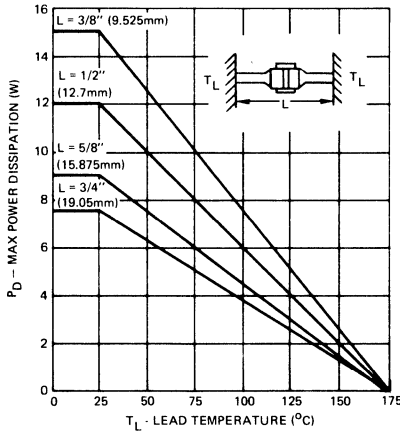
**TYPICAL FORWARD RESISTANCE
VS
FORWARD CURRENT
(F = 100 MHz)**



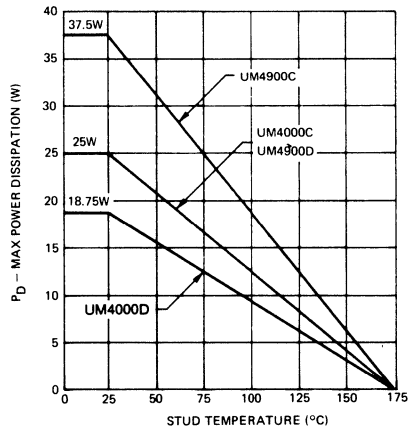
TYPICAL PARALLEL RESISTANCE CHARACTERISTIC



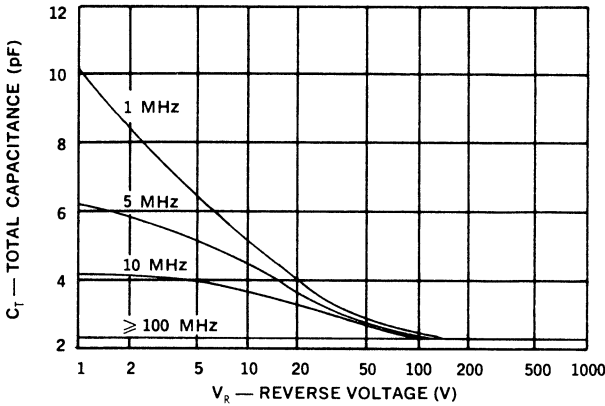
**POWER RATING
AXIAL LEADED DIODE**



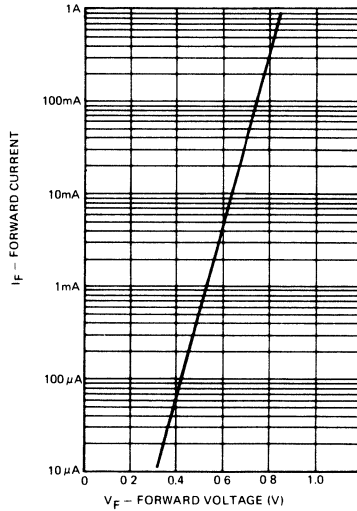
**POWER RATING
STUD MOUNTED DIODES**



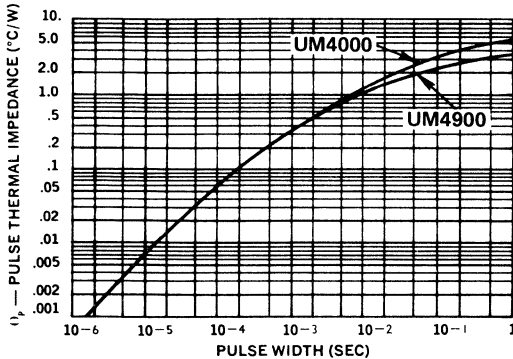
TYPICAL CAPACITANCE CHARACTERISTIC



**DC CHARACTERISTICS
FORWARD VOLTAGE
VS
FORWARD CURRENT (TYPICAL)**



THERMAL IMPEDANCE



ORDERING INSTRUCTIONS

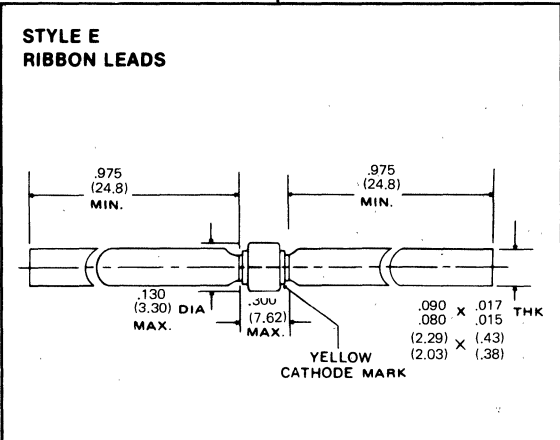
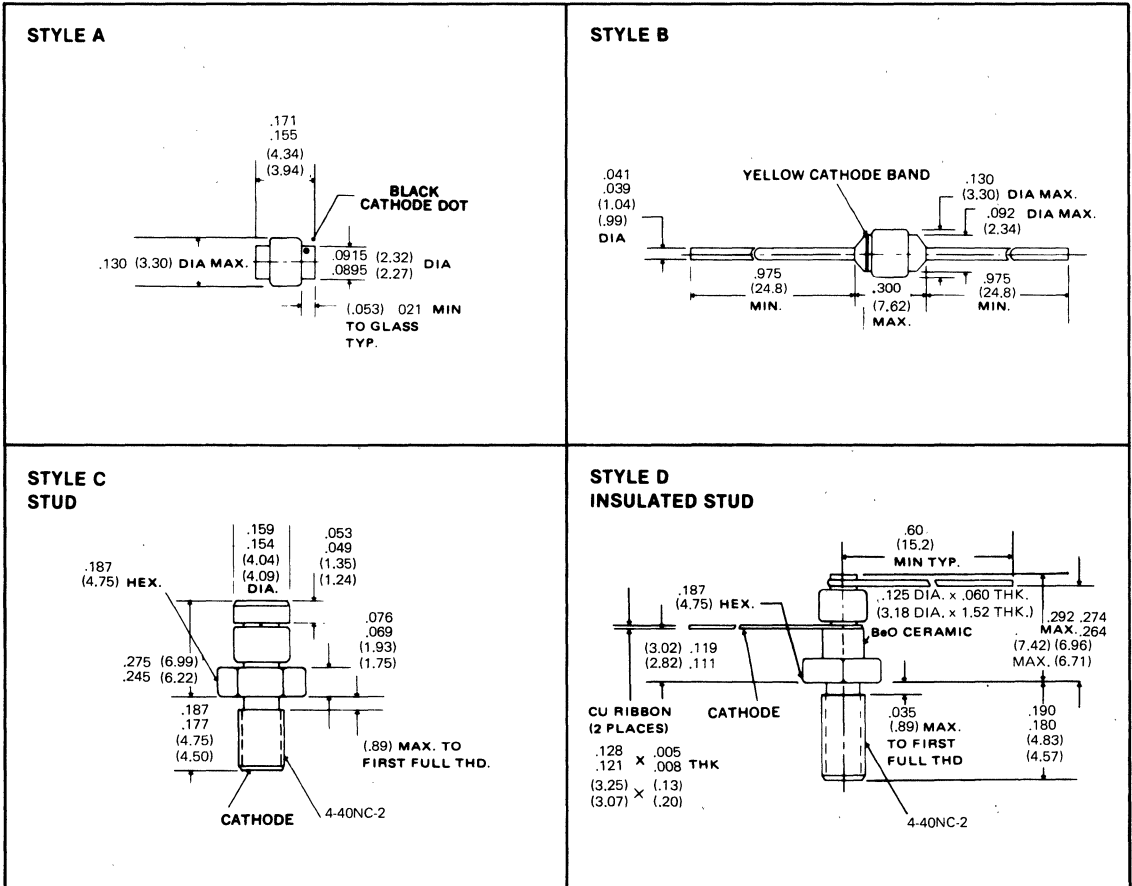
Part numbers of Unitrode PIN Diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the minimum breakdown voltage in hundreds of volts. The remaining letters denote the package style. Reverse polarity (anode large end cap) is available for the C style and denoted by adding second letter R.

For Example: **UM14006CR**
 [Series 4000] [100 Volts] [Style C] [Reverse Polarity]

MECHANICAL SPECIFICATIONS

UM4000 Series

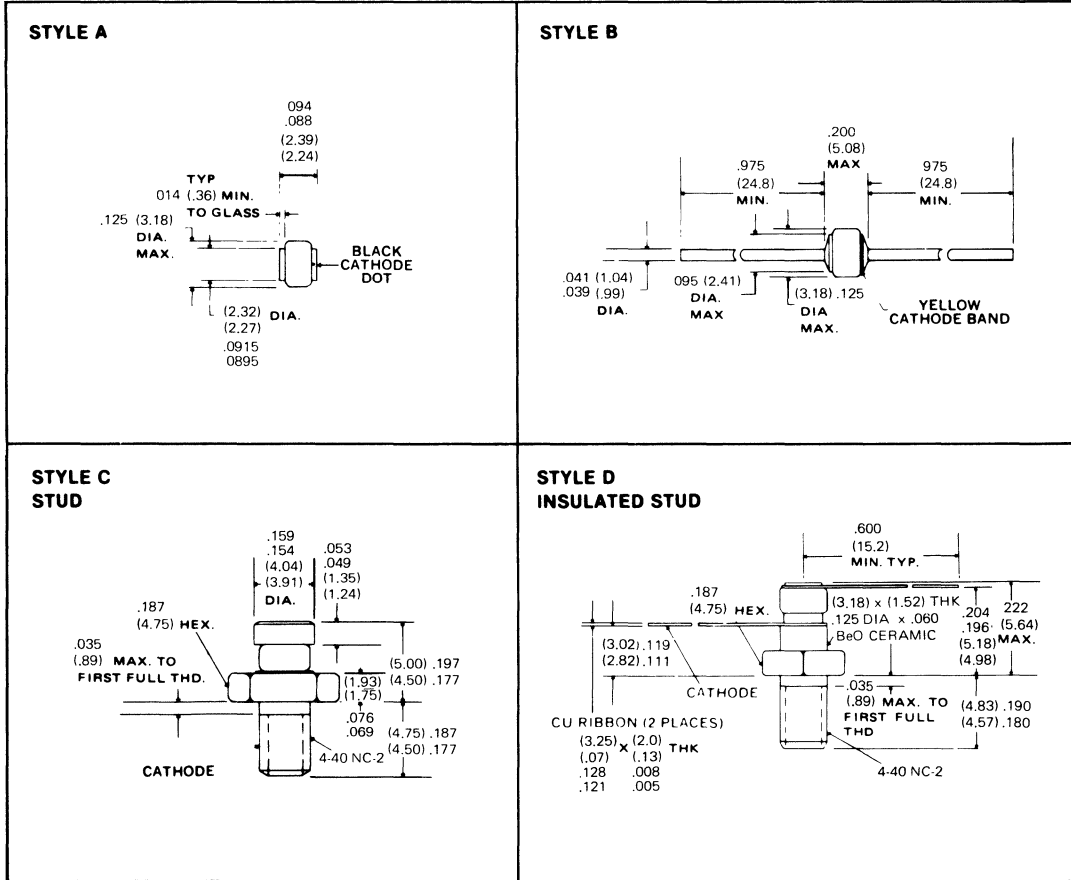
Dimensions — English/Metric



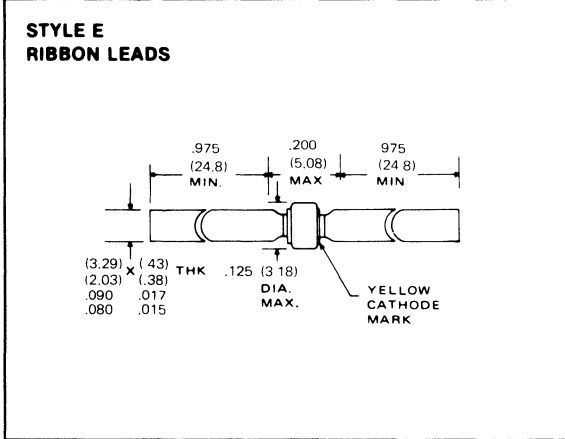
MECHANICAL SPECIFICATIONS (continued)

UM 4900 Series

Dimensions — English/Metric



12



PIN DIODE

UM4300 SERIES

UM7300 SERIES

For Attenuator Applications

Features

- Extremely low distortion performance
- Useful frequency range extends below 500 KHz
- Power dissipation to 20W (UM4300)
- Capacitance as low as 0.7 pF (UM7300)
- Voltage ratings to 1000V

Description

The UM4300 and UM7300 series combine a diode chip of extremely thick intrinsic region with a low thermal resistance construction. This results in diodes uniquely applicable to very low distortion linear attenuators and specialized switching functions. The UM4300 series, with large cross-sectional chip area offers the highest power capability, of the two series. The UM7300 series offers lower capacitance.

Both diode series are intended for use in linear attenuators operating from HF to beyond 1 GHz. Low distortion at low frequencies is a result of transit time frequencies below 5 MHz.

Operated as RF switches, either diode series can be operated at low dc reverse bias voltages, to hold off much higher RF voltage levels.

MAXIMUM RATINGS

Average Power Dissipation and Thermal Resistance Ratings

Package	Condition	UM4300		UM7300	
		P _D	θ	P _D	θ
A	25°C Pin Temperature	20W	7.5°C/W	7.5W	20°C/W
B&E (Axial Leads)	½ in. Total Length to 25°C Contact	10W	15°C/W	4W	37.5°C/W
B&E (Axial Leads)	Free Air	2.5W	—	1.5W	—
C (Studded)	25°C Stud	20W	7.5°C/W	7.5W	20°C/W
D (Insulated Stud)	25°C Stud	15W	10°C/W	6W	25°C/W

Peak Power Dissipation Rating

All packages	1µs Pulse (Single) at 25°C Ambient	500 KW	100 KW
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Operating and Storage Temperature Range: -65°C to +175°C



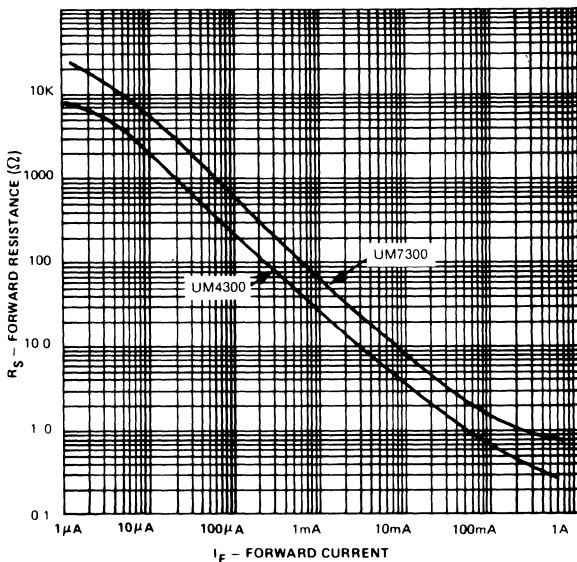
Voltage Ratings (25 °C)

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	Types	
100V	UM4301	UM7301
200V	UM4302	UM7302
600V	UM4306	UM7306
1000V	UM4310	UM7310

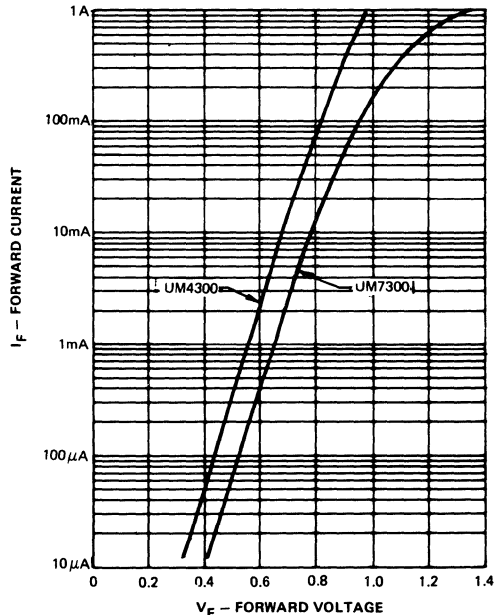
Electrical Specifications (25 °C)

Test	Symbol	UM4300	UM7300	Conditions
Total Capacitance (Max)	C_T	2.2 pF	0.7 pF	0V, 1 GHz
Series Resistance (Max)	R_S	1.5Ω	3.0Ω	100 mA, 1 GHz
Series Resistance (Min)	R_S	1000Ω	3000Ω	10 μA, 100 MHz
Carrier Lifetime (Min)	τ	6μs	4.0μs	$I_F = 10 \text{ mA}$
Leakage Current (Max)	I_R	10μA	10μA	$V_R = \text{Rating}$
I-Region Width (Min)	W	250μm	250μm	—

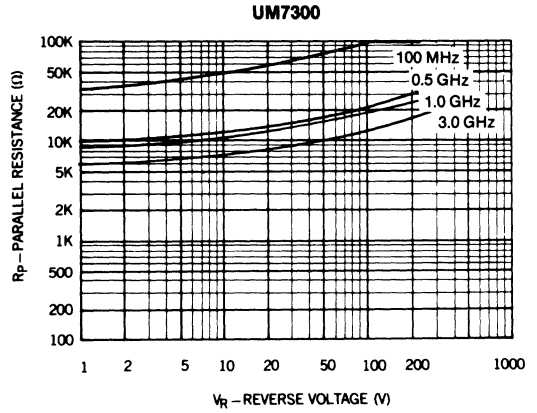
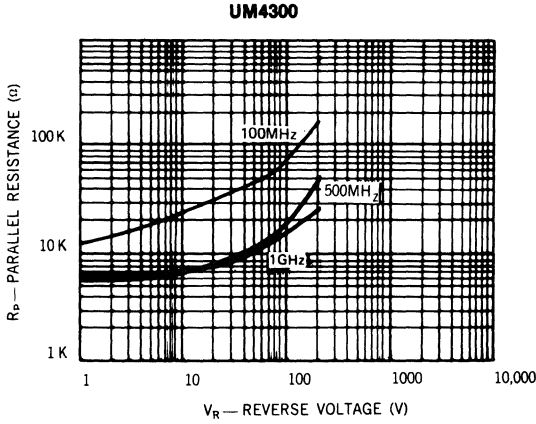
TYPICAL FORWARD RESISTANCE VS FORWARD CURRENT (F = 100 MHz)



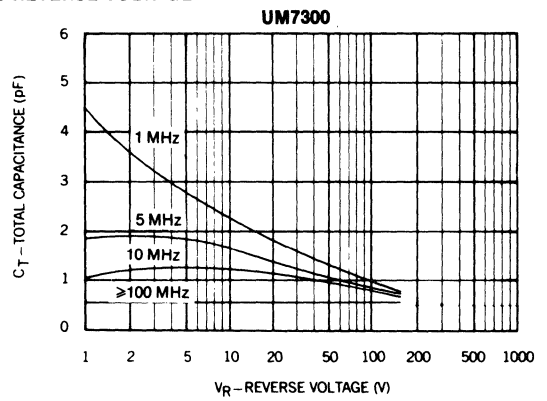
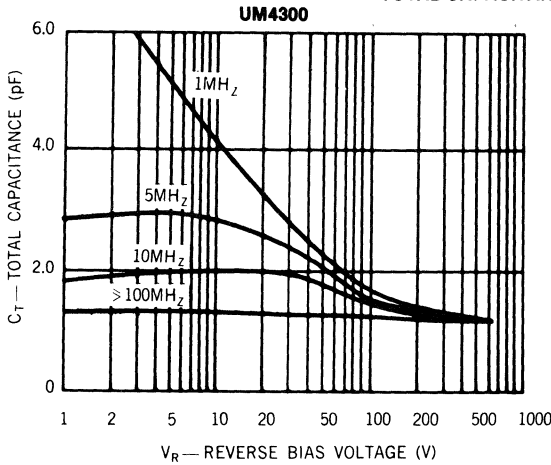
TYPICAL DC CHARACTERISTIC FORWARD VOLTAGE VS FORWARD CURRENT



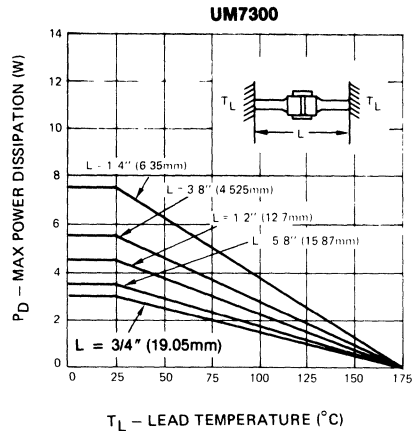
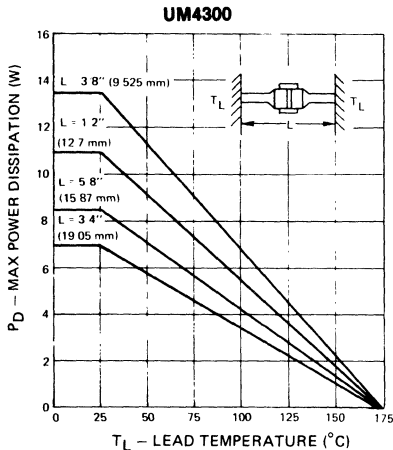
PARALLEL RESISTANCE VS REVERSE VOLTAGE



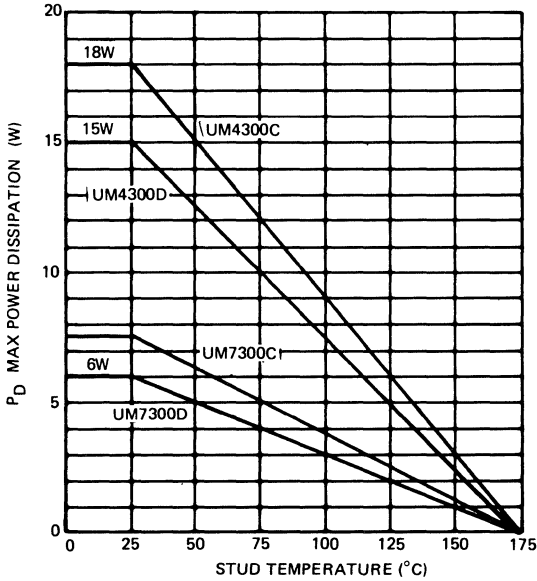
TOTAL CAPACITANCE VS REVERSE VOLTAGE



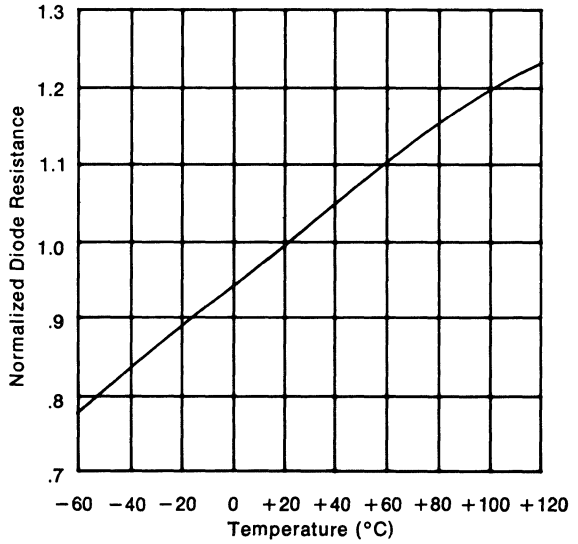
POWER RATING AXIAL LEADED DIODE



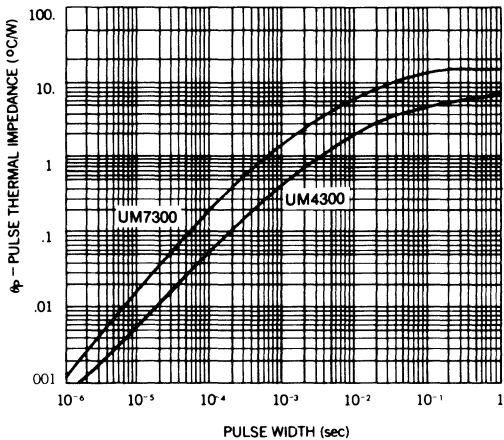
**UM4300/UM7300
POWER RATING
STUD MOUNTED DIODES**



NORMALIZED R_g VS TEMPERATURE



PULSE THERMAL IMPEDANCE VS PULSE WIDTH



ORDERING INSTRUCTIONS

Part numbers of Unitrode PIN Diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the minimum breakdown voltage in hundreds of volts. The remaining letters denote the package style. Reverse polarity (anode on stud end) is available in C or D Styles and denoted by adding second letter R.

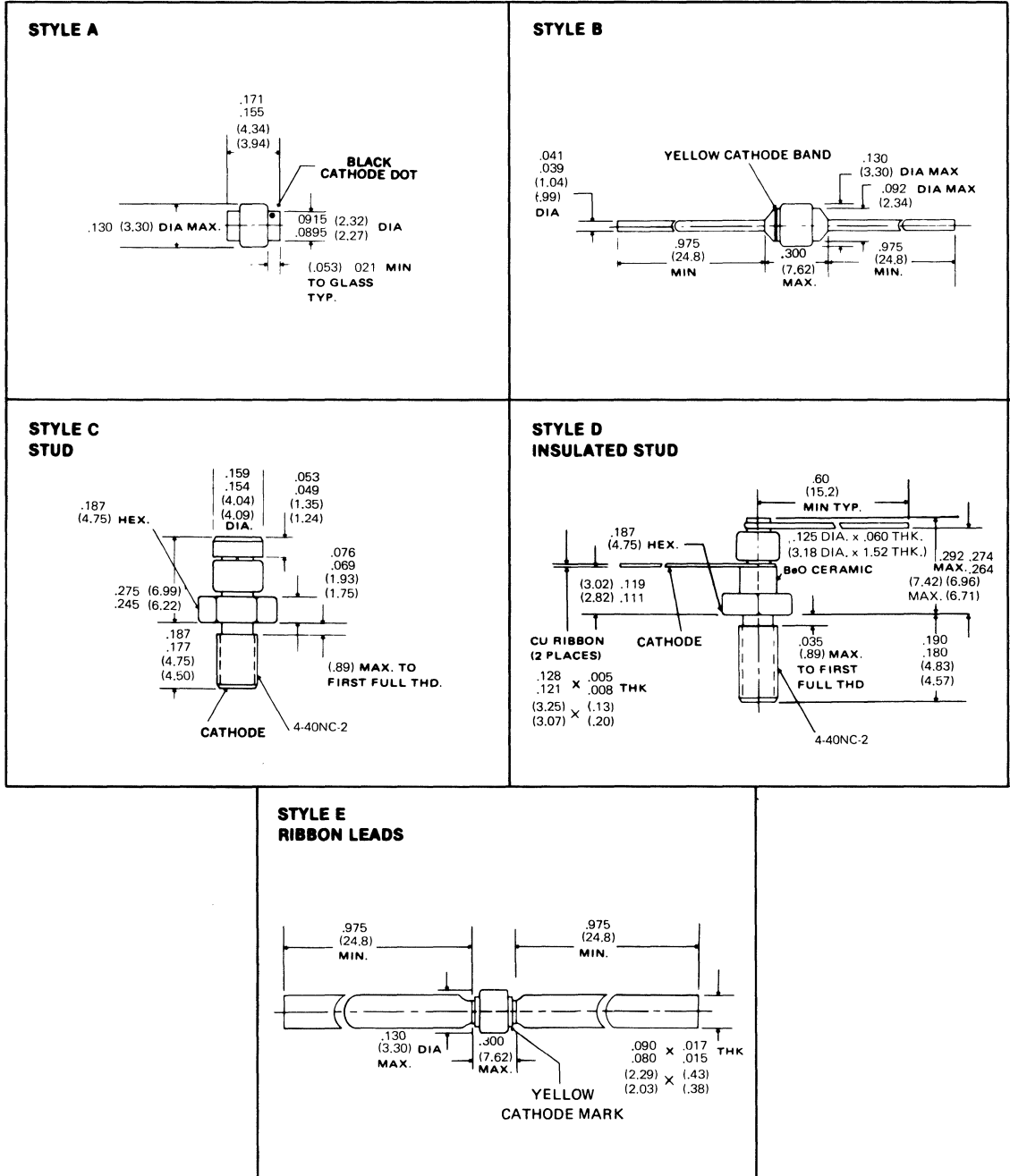
For Example: $UM|73|01|C|$
 Series 7300 | 100 volts | Style C

Reverse polarity available in C style. Part number designated by adding R.

MECHANICAL SPECIFICATIONS

UM4300 SERIES

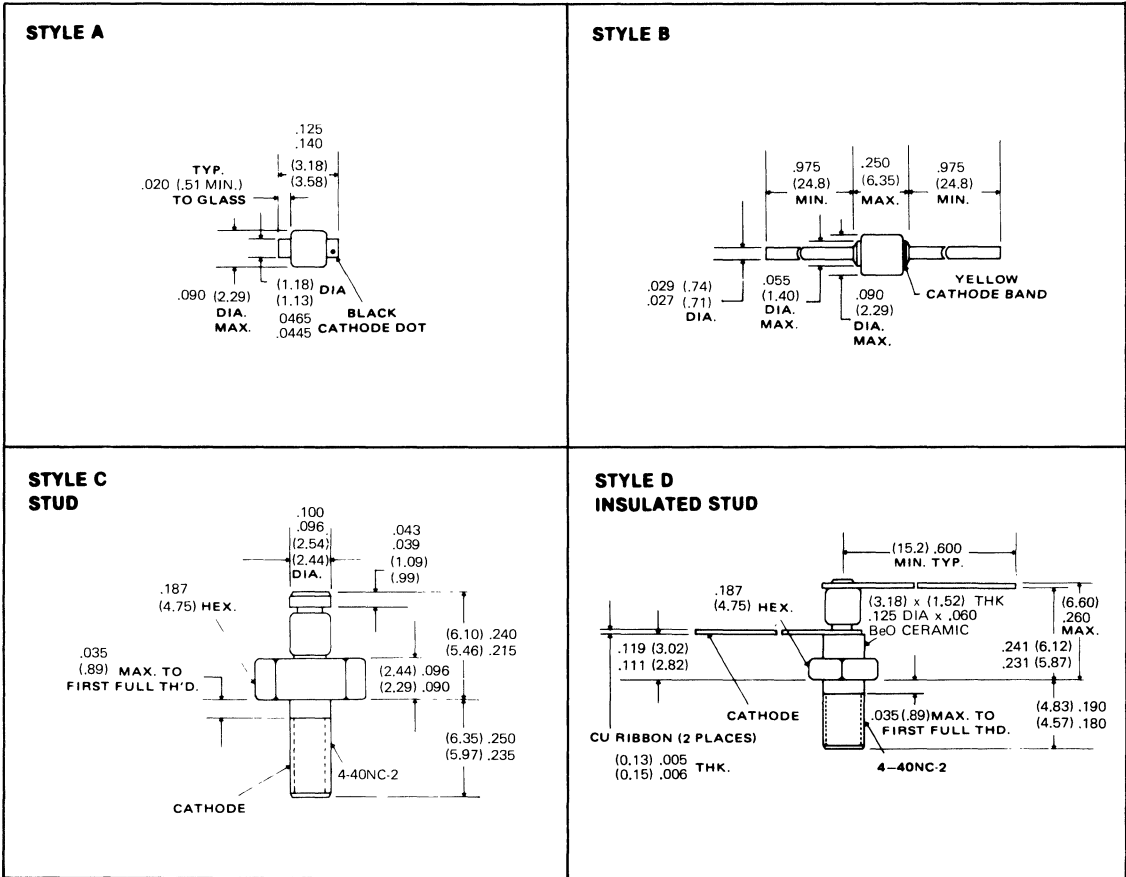
Dimensions — English/Metric



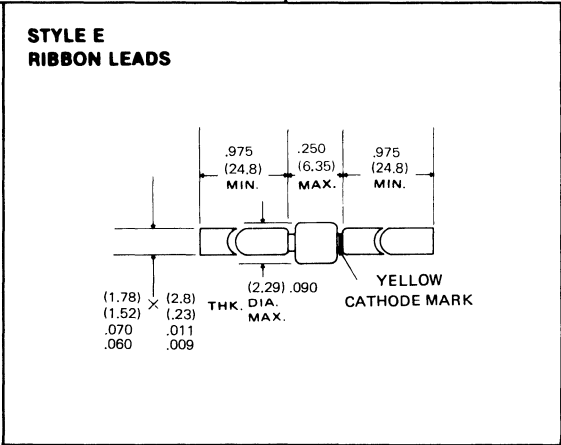
MECHANICAL SPECIFICATIONS (continued)

UM7300 Series

Dimensions — English/Metric



12



PIN DIODE

**UM6000 SERIES
UM6200 SERIES
UM6600 SERIES**

Features

- Capacitance specified as low as 0.4 pF (UM6600)
- Resistance specified as low as 0.4Ω (UM6200)
- Voltage ratings to 1000V
- Power dissipation to 6W

Description

These series of PIN diodes are designed for applications requiring small package size and moderate average power handling capability. The low capacitance of the UM6000 and UM6600 allows them to be used as series switching elements to 1 GHz. The low resistance of the UM6200 is useful in applications where forward bias current must be minimized.

Because of its thick I-region width and long lifetime the UM6000 and UM6600 have been used in distortion sensitive and high peak power applications, including receiver protectors, TACAN, and IFF equipment. Their low capacitance allows them to be useful as attenuator diodes at frequencies greater than 1 GHz. The UM6200 has been used suc-

cessfully in switches in which low insertion loss at low bias current is required.

The "A" style package for this series is the smallest Unitrode PIN diode package. It has been used successfully in many microwave applications using coaxial, microstrip, and stripline techniques at frequencies beyond X-Band. The "B" and "E" style, leaded packages offer the highest available power dissipation for a package this small. They have been used extensively as series switch elements in microstrip circuits. The "C" style package duplicates the physical outline available in conventional ceramic-metal packages but incorporates the many reliability advantages of the Unitrode construction.

MAXIMUM RATINGS

Average Power Dissipation and Thermal Resistance Ratings

Package	Condition	UM6000 UM6200		UM6600	
		P _D	θ	P _D	θ
A&C	25°C Pin Temperature	6W	25°C/W	4W	37.5°C/W
B&E (Axial Leads)	½ in. Total Lead Length to (12.7 mm) to 25°C Contact	2.5W	60°C/W	2.0W	75°C/W
B&E (Axial Leads)	Free Air	0.5W	—	0.5W	—

Peak Power Dissipation Rating

All Packages	1 μs Pulse (Single) at 25°C Ambient	UM6000 - 25 KW UM6200 - 10 KW	UM6600 - 13 KW
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Operating and Storage Temperature Range: -65°C to +175°C



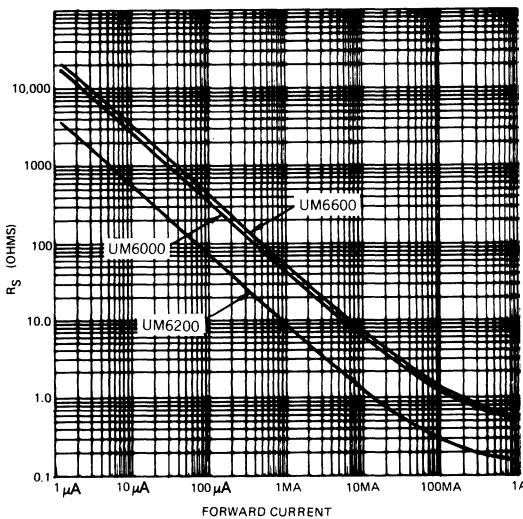
Voltage Ratings (25 °C)

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	Types		
100V	UM6001	UM6201	UM6601
200V	UM6002	UM6202	UM6602
400V	—	UM6204	—
600V	UM6006	—	UM6606
1000V	UM6010	—	UM6610

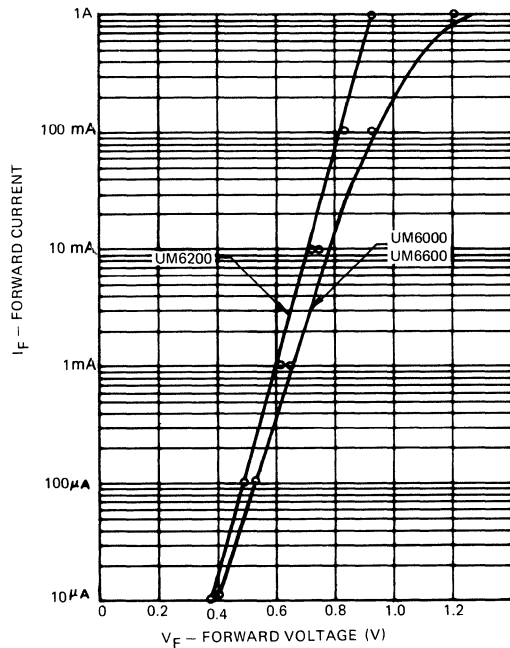
Electrical Specifications (25 °C)

Test	Symbol	UM6600	UM6000	UM6200	Conditions
Total Capacitance (Max)	C_T	0.4 pF	0.5 pF	1.1 pF	0V, 1 GHz
Series Resistance (Max)	R_S	2.5Ω	1.7Ω	0.4Ω	100 mA, 1 GHz
Parallel Resistance (Min)	R_P	10 KΩ	15 KΩ	10 KΩ	100V, 1 GHz
Carrier Lifetime (Min)	τ	1.0 μs	1.0 μs	0.6 μs	$I_F = 10 \text{ mA}$
Reverse Current (Max)	I_R	10 μA	10 μA	10 μA	$V_R = \text{Rating}$
I-Region Width (Min)	W	150 μm	150 μm	40 μm	—

TYPICAL SERIES RESISTANCE VS FORWARD CURRENT (F = 100MHz)

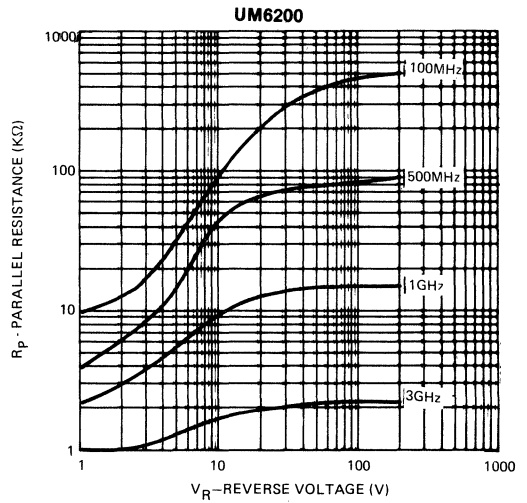
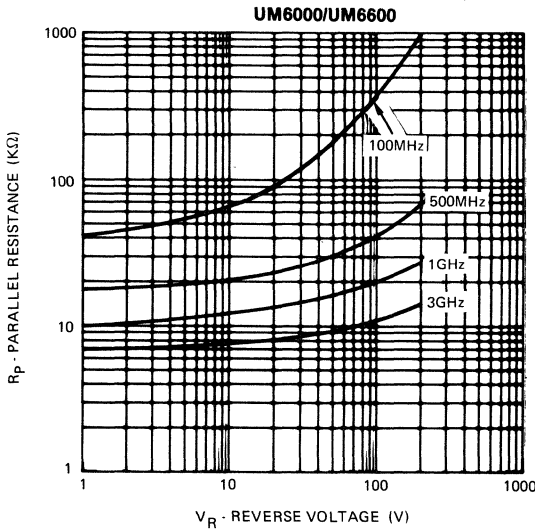


DC CHARACTERISTICS FORWARD VOLTAGE VS CURRENT

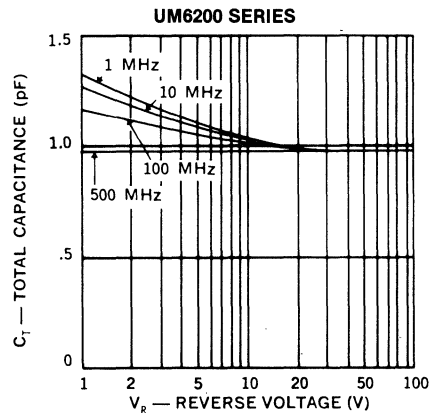
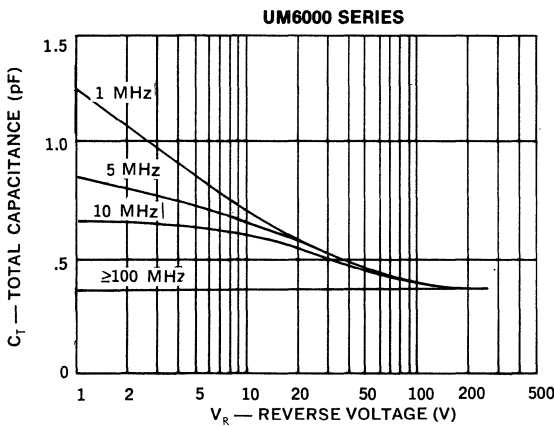


12

TYPICAL R_p VS VOLTAGE & FREQUENCY



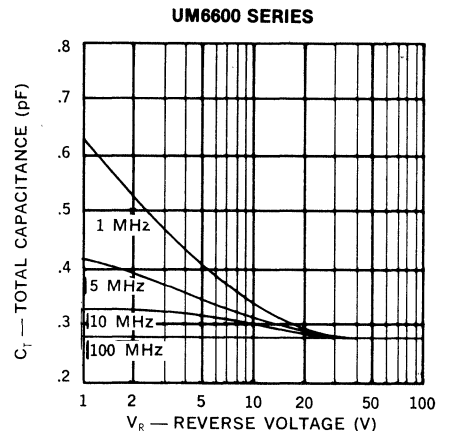
TYPICAL CAPACITANCE VS VOLTAGE AND FREQUENCY



ORDERING INSTRUCTIONS

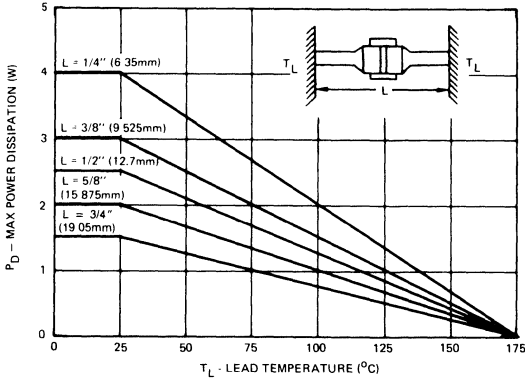
Part numbers of Unitorde PIN diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the minimum breakdown voltage in hundreds of volts. The remaining letters denote the package style. Reverse polarity (anode large end cap) is available for the C style and denoted by adding second letter R.

For Example: **UM 6006 CR**
 [Series 6000] [600 Volts] [Style C|Reverse Polarity]

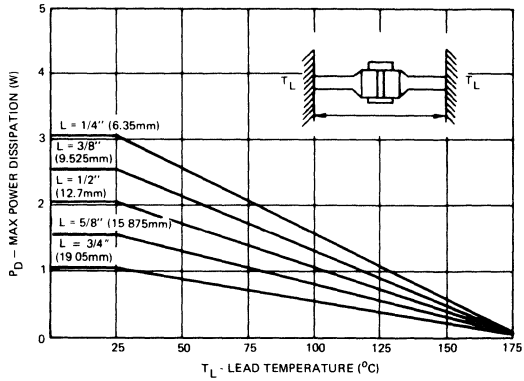


POWER RATING — AXIAL LEADED DIODE

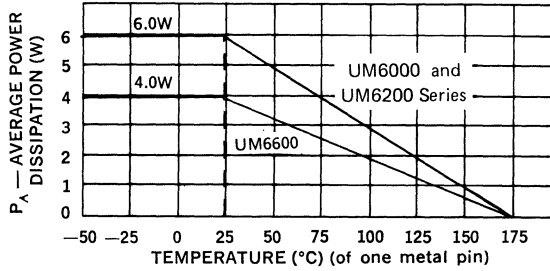
UM6000/UM6200



UM6600

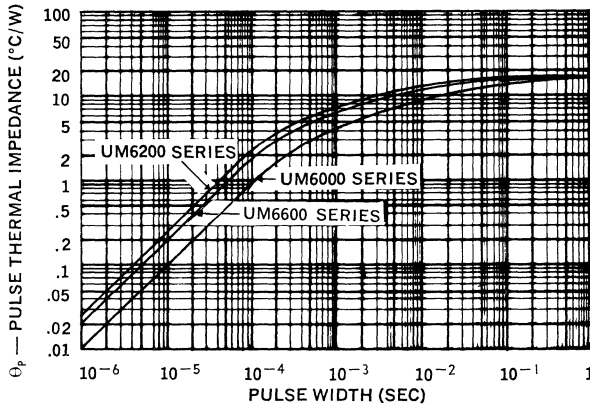


POWER RATING

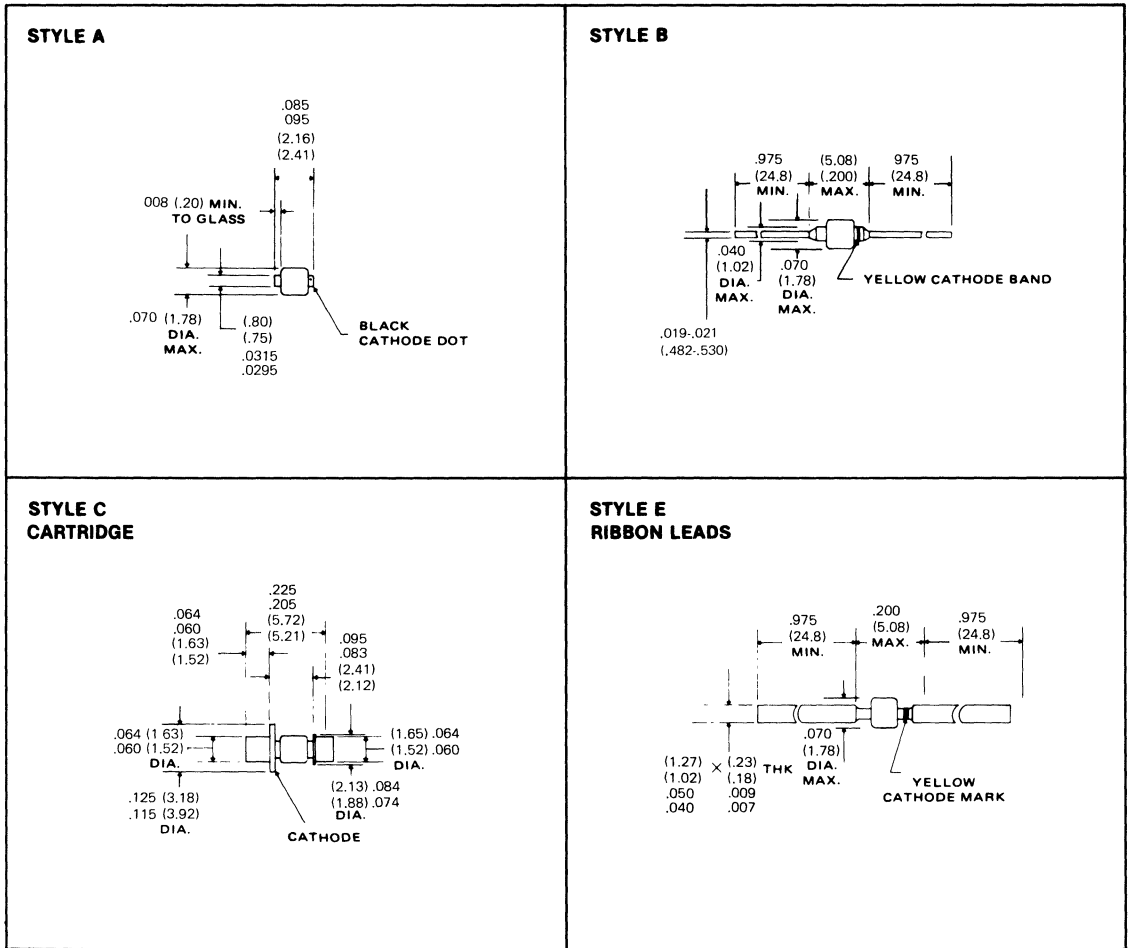


12

PULSE THERMAL IMPEDANCE VS PULSE WIDTH



MECHANICAL SPECIFICATIONS



PIN DIODE

UM7000 SERIES
UM7100 SERIES
UM7200 SERIES

Features

- Voltage ratings to 1000V (UM7000)
- Wide variety of package styles
- Rated average power dissipation to 10W
- Cost effective in volume applications

Description

The UM7000 and UM7100 series offer moderately high power handling in combination with reasonably low levels of both series resistance and capacitance. The UM7200 series offers the lowest series resistance, but the highest capacitance of the group. The differences in specified performance, for

each of the series, results from different l-region thicknesses. The three series have broad applicability in many RF and microwave switch and attenuator circuits. Additionally, the UM7100 in leaded versions, is usually the most cost-effective diode choice in high volume usage.

MAXIMUM RATINGS

Average Power Dissipation and Thermal Resistance Ratings

Package	Condition	P _d	θ
A	25 °C Pin Temperature	10W	15 °C/W
B&E (Axial Leads)	½ in.(12.7 mm) Lead Length to 25 °C Contact	5.5W	27.5 °C/W
B&E (Axial Leads)	Free Air	1.5W	—
C (Studded)	25 °C Stud Temperature	10W	15 °C/W
D (Insulated Stud)	25 °C Stud Temperature	7.5W	20 °C/W

Peak Power Dissipation Rating

All Packages	1 μs Pulse (Single) at 25 °C Ambient	UM7000 - 60 KW UM7100 - 35 KW UM7200 - 20 KW
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Operating and Storage Temperature Range:	- 65 °C to + 175 °C
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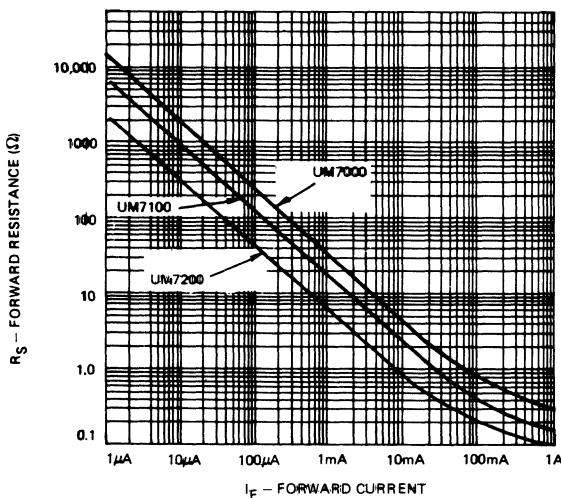
Voltage Ratings (25 °C)

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	Types		
100V	UM7001	UM7101	UM7201
200V	UM7002	UM7102	UM7202
400V	—	UM7104	UM7204
600V	UM7006	—	—
800V	—	UM7108	—
1000V	UM7010	—	—

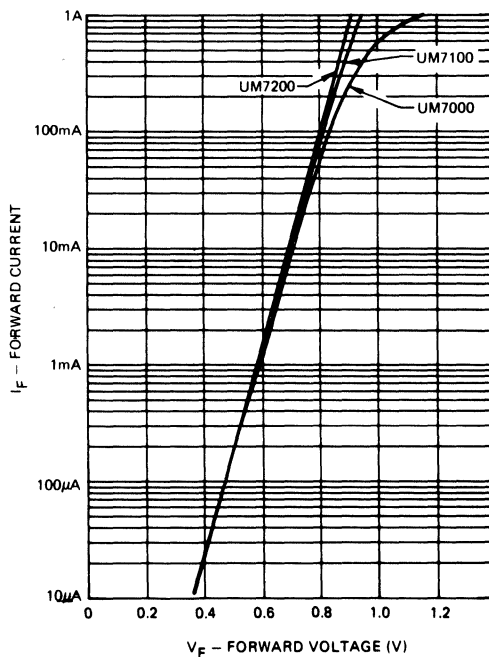
Electrical Specifications (25 °C)

Test	Symbol	UM7000	UM7100	UM7200	Conditions
Total Capacitance (Max)	C_T	0.9 pF	1.2 pF	2.2 pF	0V, 1 GHz
Series Resistance (Max)	R_S	1.0Ω	0.6Ω	0.25Ω	100 mA, 1 GHz
Parallel Resistance (Min)	R_P	10 KΩ	8 KΩ	7 KΩ	100V, 1 GHz
Carrier Lifetime (Min)	τ	2.5 μs	2.0 μs	1.5 μs	$I_F = 10 \text{ mA}$
Reverse Current (Max)	I_R	10 μA	10 μA	10 μA	$V_R = \text{Rating}$
I-Region Width (Min)	W	150 μm	80 μm	40 μm	—

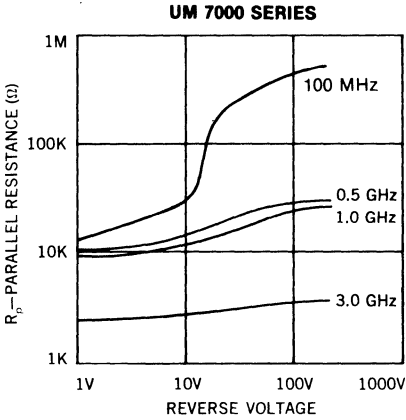
TYPICAL FORWARD RESISTANCE VS FORWARD CURRENT (F = 100 MHz)



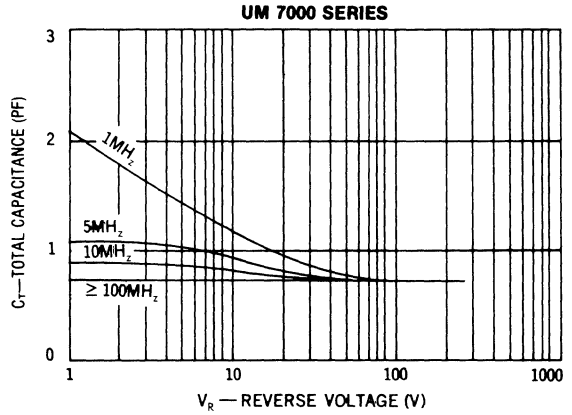
TYPICAL DC CHARACTERISTIC FORWARD VOLTAGE VS FORWARD CURRENT UM7000/UM7100/UM7200



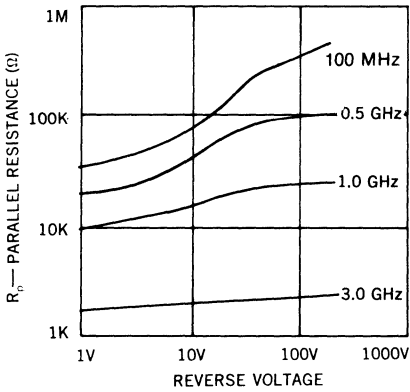
TYPICAL R_p CHARACTERISTIC



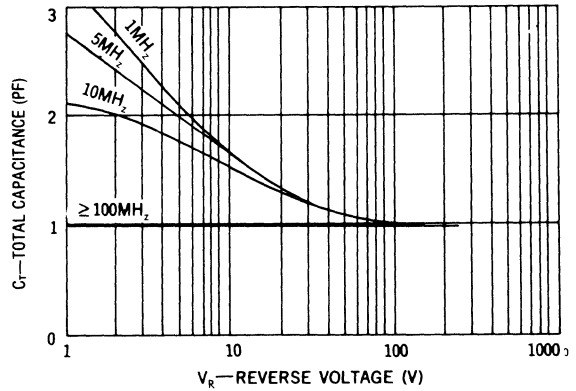
TYPICAL C_T CHARACTERISTIC



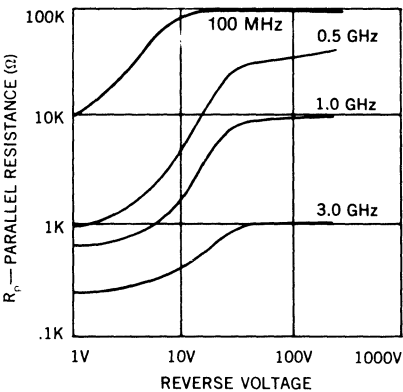
UM7100 SERIES



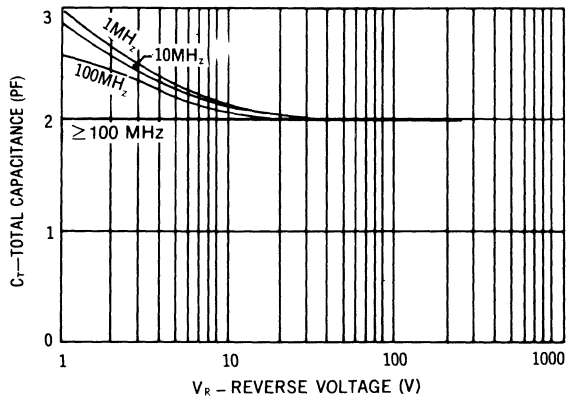
UM 7100 SERIES



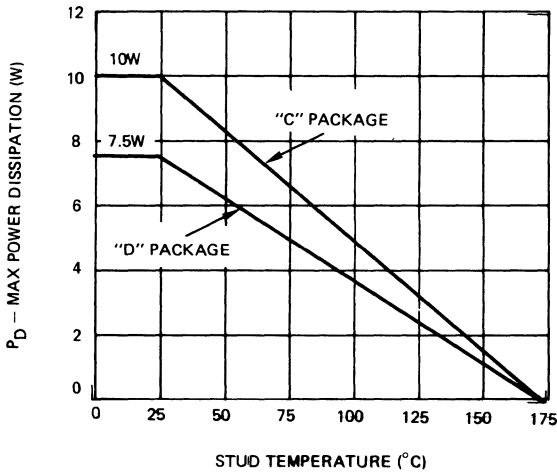
UM 7200 SERIES



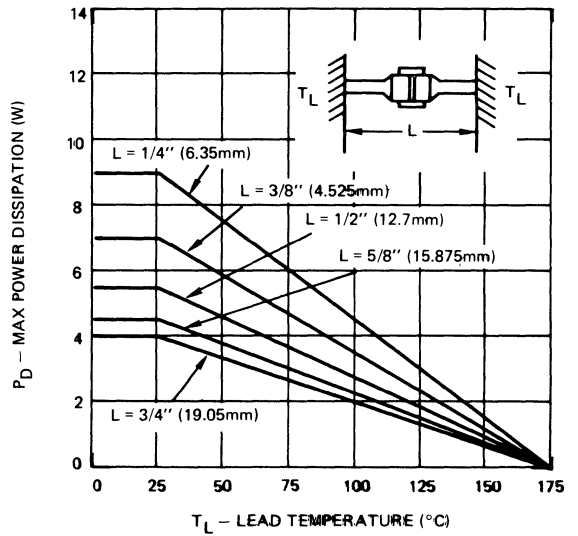
UM 7200 SERIES



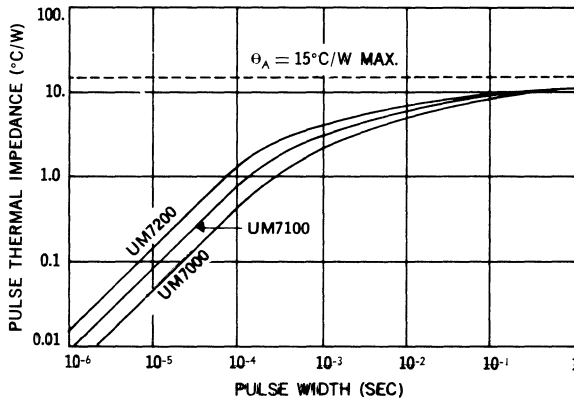
POWER RATING STUD MOUNTED DIODES



POWER RATING — AXIAL LEADED DIODES



PULSE THERMAL IMPEDANCE VS PULSE WIDTH



ORDERING INSTRUCTIONS

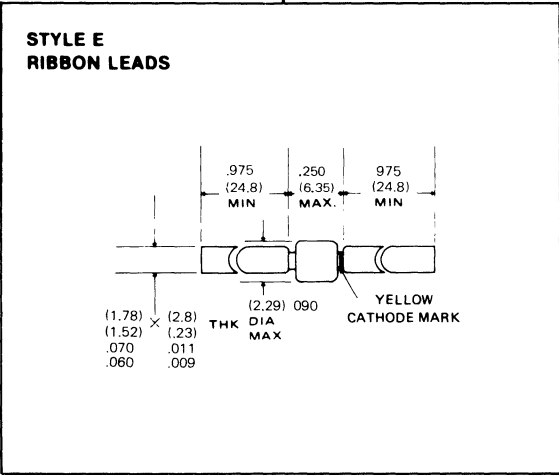
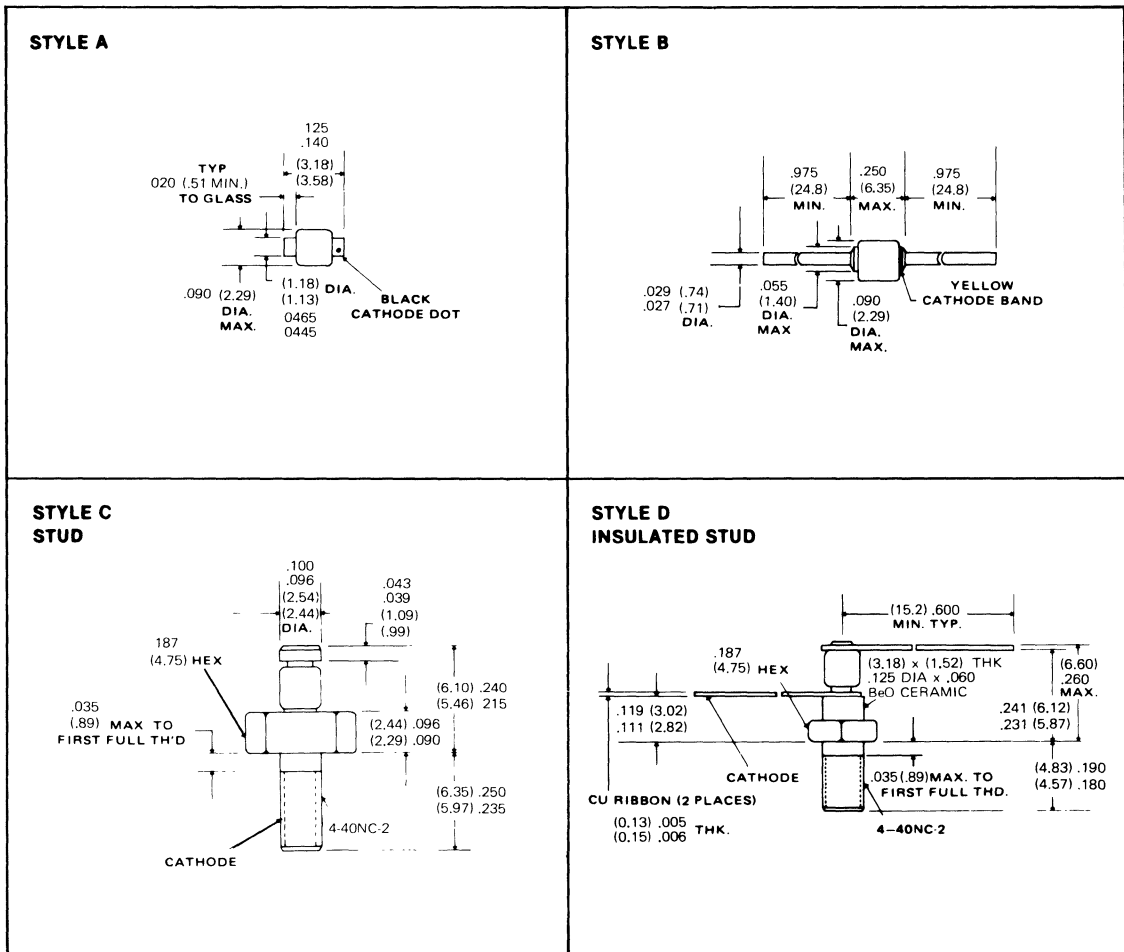
Part numbers of Unitorde PIN Diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the minimum breakdown voltage in hundreds of volts. The remaining letters denote the package style. Reverse polarity (anode on stud end) is available in C or D Styles and denoted by adding second letter R.

For Example: $UM7001C$

Series 7000	100 volts	Style C
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MECHANICAL SPECIFICATIONS

Dimensions — English/Metric



COMMERCIAL ATTENUATOR DIODE

Features

- Specified low distortion
- Low rectification properties at low reverse bias
- Resistance specified at 3 current points
- High reliability fused-in-glass construction

Description

The UM9301 PIN Diode utilizes a special overall chip geometry with an extremely thick intrinsic "I" region, to offer unique capabilities in both RF switch and attenuator applications. Volume production also makes the diode an economical choice suitable for many commercial low power equipments.

The UM9301 has been designed for use in bridged TEE attenuator circuits commonly

utilized for gain and slope control in CATV amplifiers. Low distortion and high dynamic range are characteristic of the diodes' outstanding performance.

The UM9301 is also appropriate for switch applications, when little or no bias voltage is available. Frequent applications occur in portable 12 volt-powered communications equipments, operating at frequencies as low as 2 MHz.

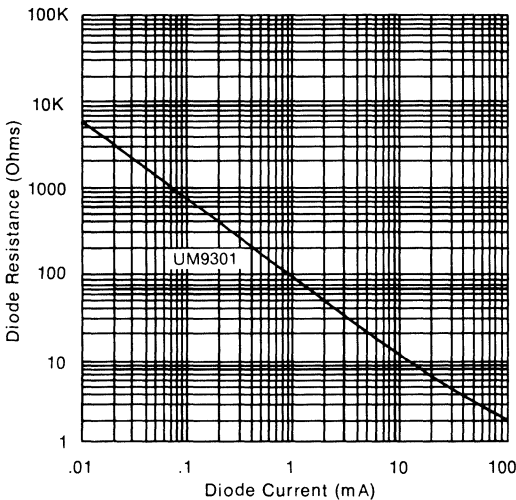
MAXIMUM RATINGS

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	75V
Average Power Dissipation @ (P_A) Leads $\frac{1}{2}$ in. overall to 25°C Contact	1.0W (Derate linearly to 175°C)
Operating and Storage Temperature Range	-65°C to +175°C

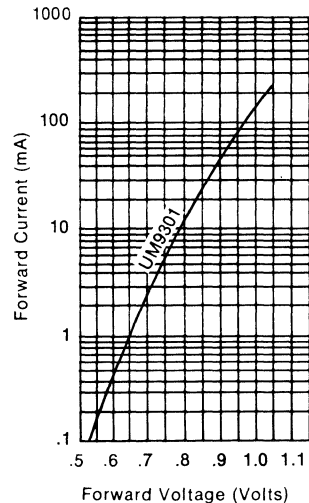
Electrical Specifications (25°C)

Test	Min	Typ	Max	Units	Conditions
Diode Resistance R_s		1.7	3.0	Ω	$I = 100 \text{ mA}, f = 100 \text{ MHz}$
		80	150	Ω	$I = 1 \text{ mA}, f = 100 \text{ MHz}$
	3000	5000		Ω	$I = 0.01 \text{ mA}, f = 100 \text{ MHz}$
Current for $R_s = 75\Omega$	0.5	1.1	2.0	mA	$f = 100 \text{ MHz}$
Capacitance			0.8	pF	$V = 0V, f = 100 \text{ MHz}$
Return Loss	25			dB	Frequency Range: 10 - 300MHz $R_s = 75\Omega @ 100 \text{ MHz}$ Diode Terminates 75Ω line
Second Order Distortion		55	50	- dB	$f_1 = 10 \text{ MHz}, f_2 = 13 \text{ MHz}$ $P = 50 \text{ dBmV}$, See Test Circuit
		70		- dB	$F_1 = 67 \text{ MHz}, F_2 = 77 \text{ MHz}$ $P = 50 \text{ dBmV}$, See Test Circuit
Third Order Distortion		75	65	- dB	$F_1 = 10 \text{ MHz}, F_2 = 13 \text{ MHz}$ $P = 50 \text{ dBmV}$, See Test Circuit
		95		- dB	Triple Beat; 205 + 67 - 77 MHz $P = 50 \text{ dBmV}$, See Test Circuit
Cross Modulation Distortion		75		- dB	12 Channel Test $P = 50 \text{ dBmV}$, See Test Circuit Dix Hills Test Set
Reverse Current			10	μA	$V = 75V$
Carrier Lifetime	4.0			μs	$I = 10 \text{ mA}$

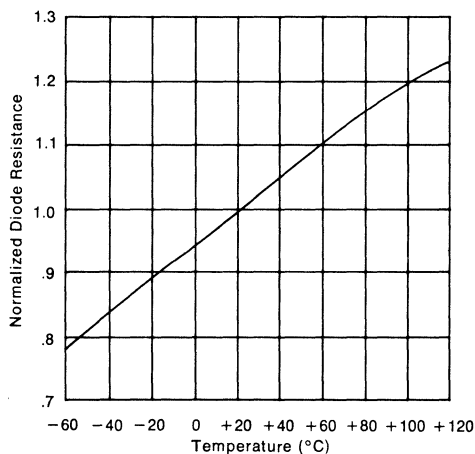
DIODE RESISTANCE VS DIODE CURRENT (TYPICAL)



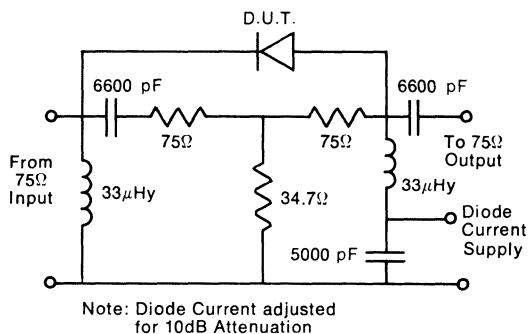
FORWARD CURRENT VS FORWARD VOLTAGE (TYPICAL)



NORMALIZED R_S VS TEMPERATURE

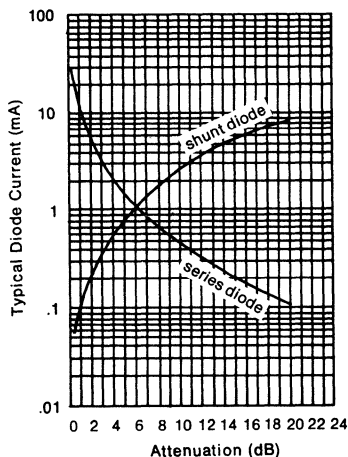


TEST CIRCUIT FOR DISTORTION MEASUREMENTS

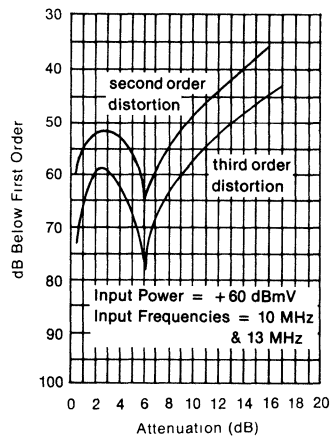


TYPICAL BRIDGED TEE ATTENUATOR PERFORMANCE

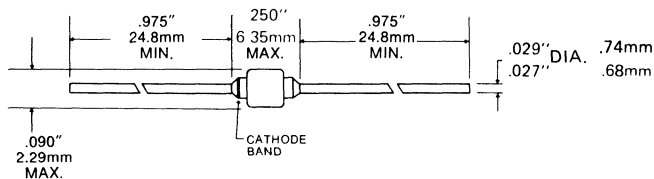
DIODE CURRENT VS ATTENUATION UM9301



DISTORTION ATTENUATION



MECHANICAL SPECIFICATIONS



PIN DIODE

UM9401 SERIES
UM9402 SERIES
UM9415 SERIES

COMMERCIAL TWO-WAY RADIO ANTENNA SWITCH DIODES

Features

- Specified low distortion
- Unitrode ruggedness and reliability
- Low bias current requirements
- Priced for high quantity applications

Description:

Unitrode offers a series of PIN diodes specifically designed and characterized for solid state antenna switches in commercial two-way radios. Antenna switches using the UM9401 and UM9415 series PIN diodes provide high isolation, low loss and low distortion characteristics formerly possible only with electromechanical relay type switches.

The UM9401 and UM9402 diodes can handle above 100W of transmitter power,

while the UM9415 will handle over 1000W. The extensive characterization of these PIN diodes in antenna switch applications has resulted in guaranteed low distortion specifications under transmit and receive conditions. These diodes also feature low forward bias resistance and high zero bias impedance which are required for low loss, high isolation and wide bandwidth antenna switch performance.

MAXIMUM RATINGS

Reverse Voltage (V_R) — Volts ($I_R = 10 \mu A$)	UM9401	UM9402	UM9415
		50V	50V

Average Power Dissipation (P_A)	UM9401	UM9402	UM9415
Leads - 1/2in. Overall to 25 °C	5.5W	—	10W
Heat Sink	—	10W	—
25 °C (Package Flange) Temperature	—	—	—
Free Air	1.5W	—	2.5W

Operating and Storage Temperature Range	UM9401, UM9402, UM9415
	-65 °C to +175 °C

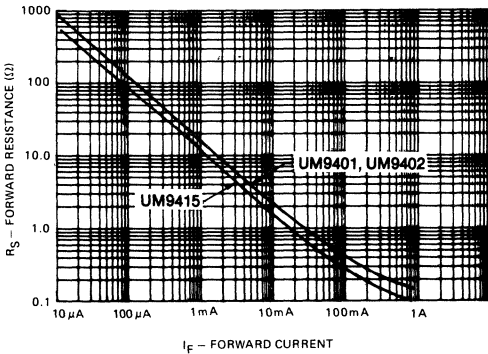
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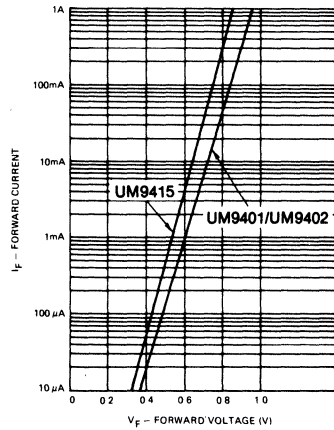
Electrical Specifications (at 25 °C)

Test	Symbol	UM9401/UM9402			UM9415			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Series Resistance	R_S		0.75	1.0		0.75	1.0	Ω	$f = 100\text{MHz}$ typical $I = 50\text{ mA}$
Diode Capacitance	C_T		1.1	1.5			4	pF	$f = 100\text{ MHz}$ $V = 0\text{V}$
Parallel Resistance	R_P	5K	10K		1K	2K		Ω	$f = 100\text{ MHz}$ $V = 0\text{V}$
Carrier Lifetime	τ	1.0	2.0		5			μS	$I = 10\text{ mA}$
Transmit Harmonic Distortion	$\frac{R_{2A}}{A}, \frac{R_{3A}}{A}$			80			80	-dB	$P_{IN} = 50\text{W}$ $f = 50\text{ MHz}, I = 50\text{ mA}$
Receive Third Order Distortion	$\frac{R_{2AB}}{A}$			60			60	-dB	$P_{IN} = 10\text{ mW}, 0\text{V Bias}$ $f_A = 50\text{ MHz}, f_B = 51\text{ MHz}$
Reverse Leakage Current	I_R			10			10	μA	$V = 50\text{V}$
Forward Voltage	V_F			1.0			1.0	V	$I_F = 50\text{ mA}$

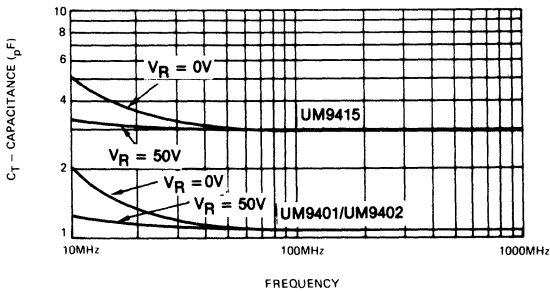
TYPICAL FORWARD RESISTANCE VS FORWARD CURRENT (F = 100 MHz)



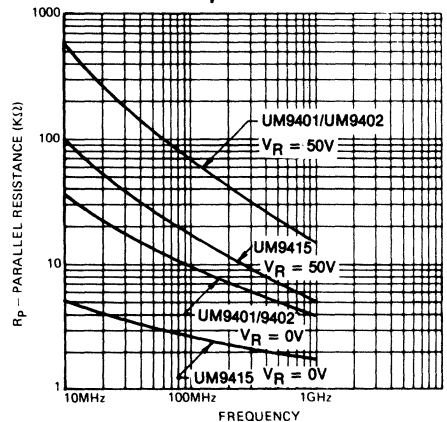
TYPICAL DC CHARACTERISTIC



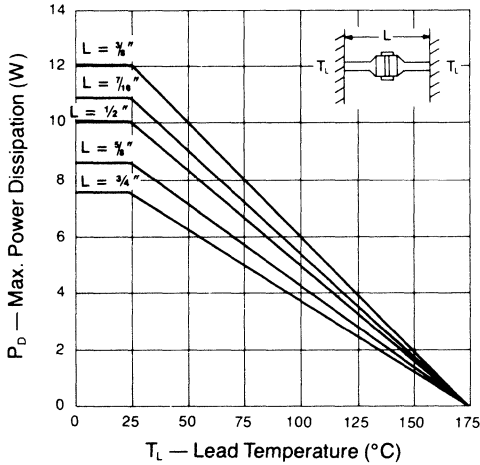
TYPICAL CAPACITANCE CHARACTERISTIC



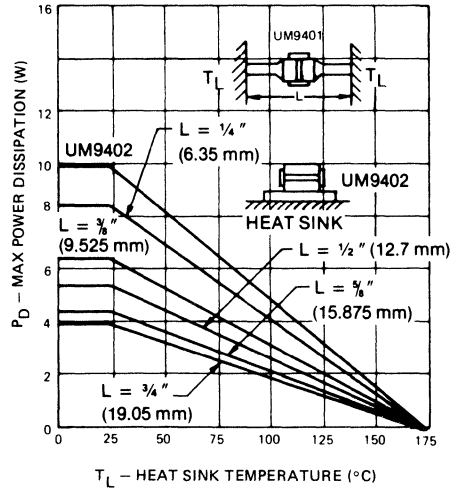
TYPICAL R_P CHARACTERISTICS



POWER RATING
UM9415

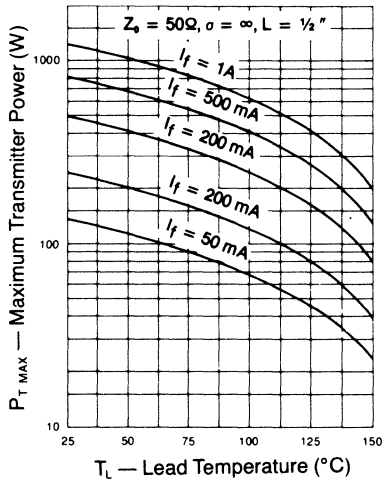


POWER RATING
UM9401/9402

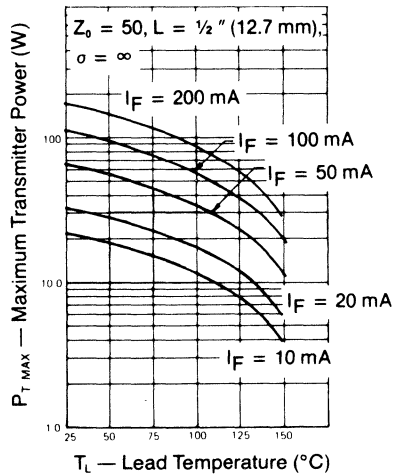


MAXIMUM TRANSMITTER POWER

UM9415



UM9401/UM9402



Maximum Transmitter Power

The maximum CW transmitter power, $P_{T(max)}$, a PIN diode antenna switch can handle depends on the diode resistance, R_S , power dissipation, P_D , antenna SWR, σ , and nominal impedance, Z_0 . The expression relating these parameters is as follows:

$$P_{T(max)} = \frac{P_D \times Z_0}{R_D} \left(\frac{\sigma + 1}{2\sigma} \right)^2 \text{ [Watts]}$$

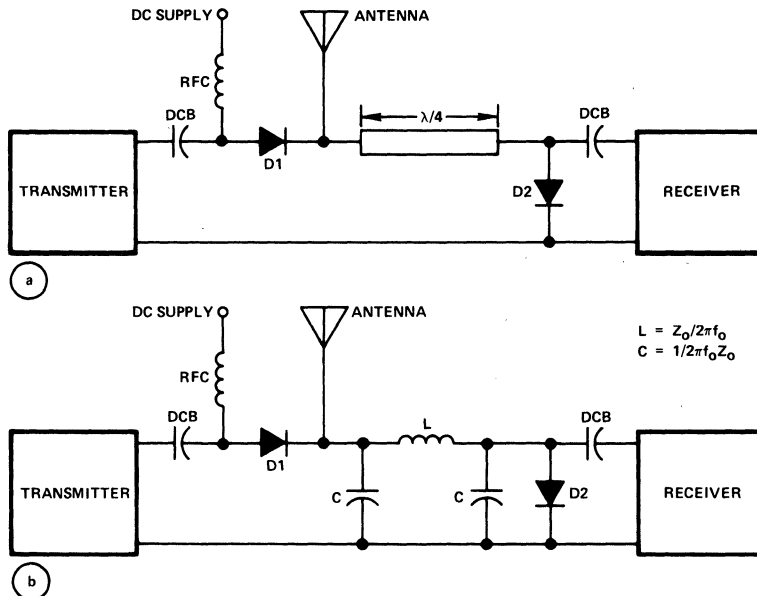
Characteristic curves are shown in the data section which give both the maximum and typical diode resistance, R_S as a function of forward current. The maximum power dissipation rating of the PIN diode depends both on the length of the diode leads and the temperature of the contacts to which the leads are connected. A graph defining the maximum power dissipation at various combinations of overall lead length (L) and lead temperature (T_L) is given in the data section. From these curves and the above equation, the power handling capability of the PIN diode may be computed for a specific application.

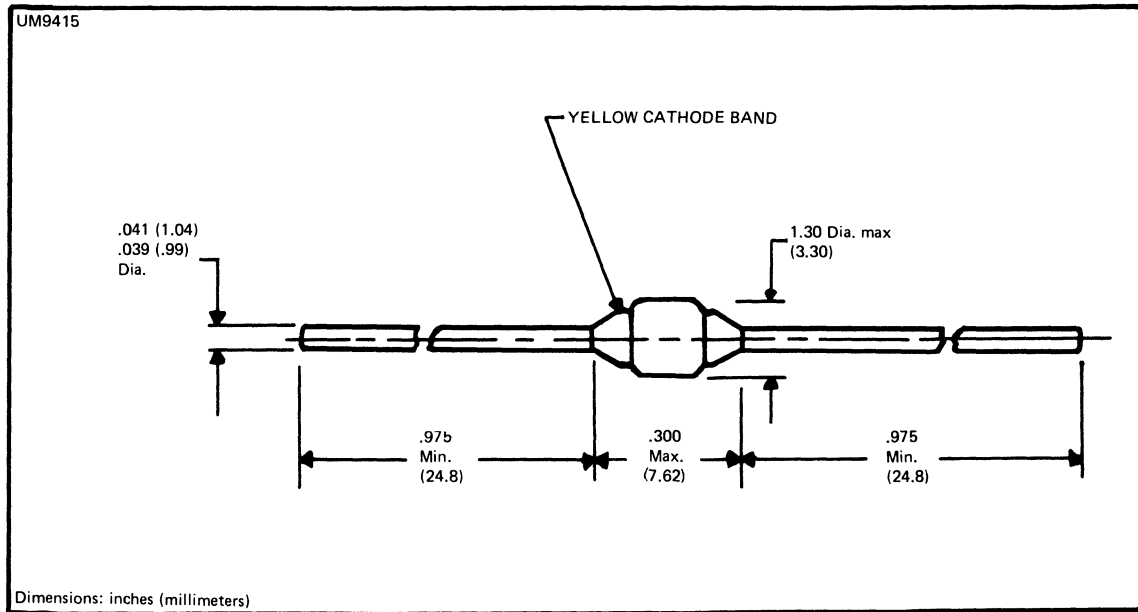
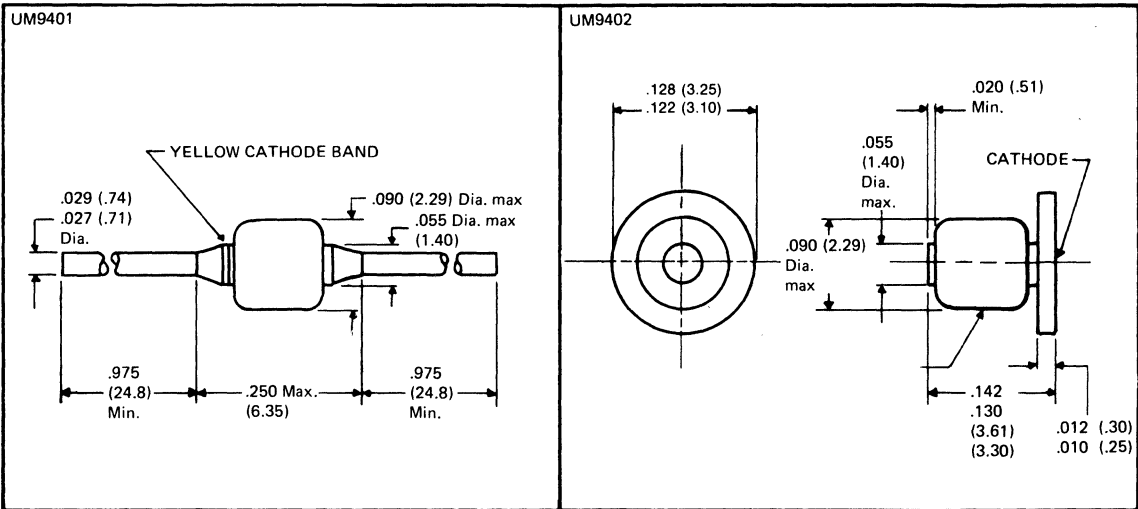
Curves are also presented which show the maximum transmitter power that an antenna

switch using UM9401s and UM9415s can safely handle for various forward currents and lead temperatures. These curves are based on a typical design condition of a 1/2 in. total overall lead length, 50Ω line impedance and a totally mismatched antenna ($\sigma = \infty$). For the case of a perfectly matched antenna, the maximum transmitter power can be increased by a factor of 4.

Design Information

A circuit configuration for a two-way radio antenna switch using PIN diodes consists of a diode placed in series with the transmitter and a shunt diode placed a quarter wavelength from the antenna in the direction of the receiver as shown. For low frequency operation, the quarter wave line may be simulated by lumped elements. Typical performance of antenna switches using PIN diodes forward biased at 100 mA is less than 0.2 dB insertion loss and 30 dB isolation during transmit; at zero bias the receive insertion loss is less than 0.3 dB. This performance is achievable across a ±20% bandwidth at center frequencies ranging from 10 to 500 MHz.





Features

- High Photocurrent Sensitivity
- High Reliability Construction
- Fast Rise Time
- Wide Dynamic Range
- Hardness to Neutron Bombardment
- Low Operating Voltage

Description

Silicon PIN devices are effective detectors of nuclear and electromagnetic radiation. This includes gamma radiation, electrons, and X-rays. The detectors can be used across the temperature range of -55°C to $+175^{\circ}\text{C}$ instead of being restricted to use at low temperatures.

The absorbed radiation produces electron-hole pairs in the space charge region. These charges are swept out by the applied field and result in a current flow proportional to the rate of absorbed radiation.

The Unitrode UM9441 series utilizes high resistivity material and is designed to have a uniform area mesa structure to define the active volume. The current sensitivity of

these devices is proportional only to the I-region volume and is independent of temperature so long as applied voltage exceeds the saturation voltage. This structure also minimizes the effects of permanent damage caused by neutrons and other high energy radiation. Experiments on devices of the UM9441 design show no degradation in gamma sensitivity resulting from a total dose of 10^{14} neutrons/cm² of 1 MeV equivalent.

Package

The UM9441 is an axially leaded device constructed by metallurgically bonding the PIN chip in between two molybdenum refractory pins that are typically 0.125 inches in diameter and 0.050 inches long. Hyper-pure glass is then fused over this bond to form a voidless seal. Leads are then brazed to ends of molybdenum pins. This results in a high-reliability package using materials so well thermally matched that the UM9441 can withstand temperature shock or cycling from -196°C to $+300^{\circ}\text{C}$.

ABSOLUTE MAXIMUM RATINGS

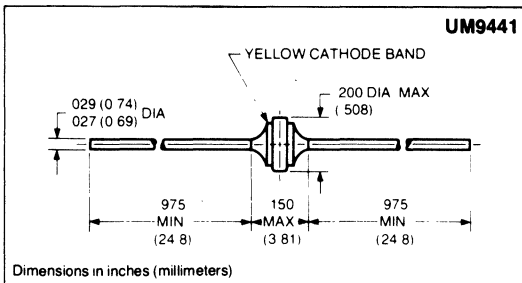
Reverse Voltage 100V

Photocurrent 1A

Storage Temperature . . . -55°C to $+200^{\circ}\text{C}$

Operating Temperature . . -55°C to $+175^{\circ}\text{C}$

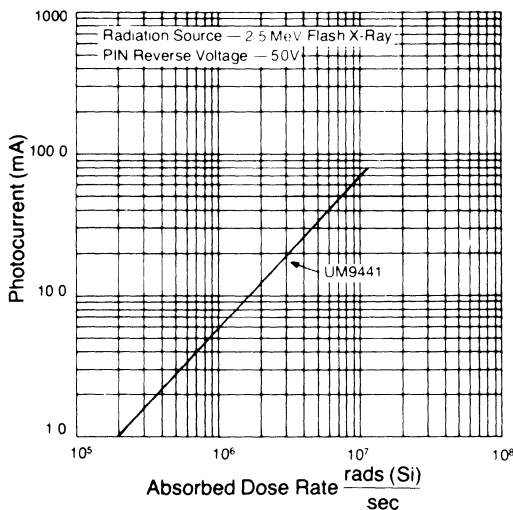
MECHANICAL SPECIFICATIONS



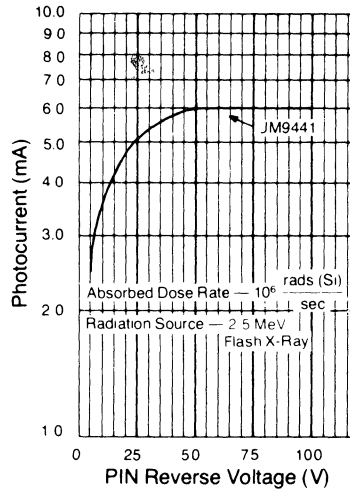
Electrical Specifications (at 25°C)

Test	Min	Typ	Max.	Units	Test Conditions
Photocurrent	4.0	6.0		mA	$V_R = 50V$ $10^6 \frac{\text{rads (Si)}}{\text{sec}}$ 2.5 MeV Flash X-Ray Ion Physics Corp. FX-25
Photocurrent Rise Time (10%-90%)		10		ns	
Capacitance		10	15	pF	$F = 1 \text{ MHz}, V = 50V$
Reverse Current			1.0	μA	$V_R = 50V$
Minority Carrier Lifetime	2.0			μS	$I_f = 10mA$

TYPICAL PHOTOCURRENT SENSITIVITY



TYPICAL VOLTAGE SENSITIVITY



RELIABILITY

The UM9441 is consistent with Unitrode's reputation as a manufacturer of high reliability semiconductors. Unitrode is equipped to perform JAN type testing, base-lining and documental conformance to a wide range of reliability testing. This commitment to reliability has enabled Unitrode to be a qualified supplier of semiconductor devices to many high-reliability programs such as:

- APOLLO
- DRAGON
- HAWK
- MARINER
- MINUTEMAN
- SPRINT
- TRIDENT
- VIKING

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PIN DIODE

UM9601-UM9608

For Microstrip 900MHz Antenna Switches and Microwave Applications

Features

- Low Inductance Shunt Mount Package
- Characterized for Microstrip
- Unitrode Ruggedness and Reliability
- High Power Handling Capability
- Low Bias Current Requirement
- Excellent Distortion Properties
- Cost Effective in High Quantity Applications

Description

The UM9601-UM9608 series of PIN diodes was developed for shunt mount applications in microstrip circuits. Good switch performance is demonstrated at frequencies from UHF to 4GHz and higher. This performance is achieved using discrete low inductance Unitrode PIN diodes assembled with special hardware to permit good electrical and mechanical compatibility with microstrip transmission lines.

Design information is presented for preparation of microstrip circuit boards to accommodate these PIN diodes. A detailed design for a 900MHz quarter-wave antenna switch is given. This switch which employs a low cost UM9401 axial leaded PIN diode in conjunction with a UM9601, performs with 30dB receiver isolation over a 100MHz bandwidth and with transmitter insertion loss of less than 0.4dB. This switch can safely handle transmitter power levels up to 100 watts at infinite antenna SWR.

The Unitrode UM9601 series PIN diodes are constructed using a fused-in-glass process which results in a highly reliable, hermetic package. The process utilizes symmetrical, full faced metallurgical bonds to both surfaces of the silicon chip. This construction greatly minimizes the normal parasitic inductance and capacitance found in conventional glass or ceramic packaged diodes which employ straps, springs or whiskers.

The use of discrete UM9601-UM9608 diodes greatly minimizes handling problems commonly associated with passivated PIN diode chips while maintaining good microwave performance. In addition the power handling capability of the UM9601-UM9608 series is considerably higher than PIN diode chips can provide.

Environmentally, the UM9601-UM9608 series PIN diodes can withstand thermal cycling from -195°C to +300°C and exceed all military environmental specification for shock, vibration, acceleration, and moisture resistance.

Typical Microwave Performance

Frequency	UM9601-UM9604			UM9605-UM9608		
	SPST Insertion Loss 0 Bias	SPST Isolation 100mA	SPNT* Isolation 100mA	SPST Insertion Loss 0 Bias	SPST Isolation 100mA	SPNT* Isolation 100mA
GHz	dB	dB	dB	dB	dB	dB
0.5	0.20	30	36	0.20	25	31
1.0	0.25	26	32	0.20	22	28
1.5	0.35	22	28	0.20	20	26
2.0	0.50	18	24	0.25	17	22
3.0	1.00	15	21	0.25	15	21
4.0	1.50	13	19	0.40	14	20

* Performance based on SPST Measurements
In 0.025" (.635mm) Microstrip Test Circuit.

Note: All dimensions in inches and (millimeters).



Maximum Ratings

	UM9601 - UM9604		UM9605 - UM9608	
	P _D	θ	P _D	θ
Flange at 25° C	7.5W	20° C/W	4W	37.5° C/W
Free Air	1.5W	—	0.5W	—

Reverse Voltage Ratings @ 10 μ A

100V	400V
UM9601	UM9602
UM9603	UM9604
UM9605	UM9606
UM9607	UM9608

Peak Power 1 μ S Single Pulse at 25° C Ambient	25KW	10KW
-----------------------------------------------------------------	------	------

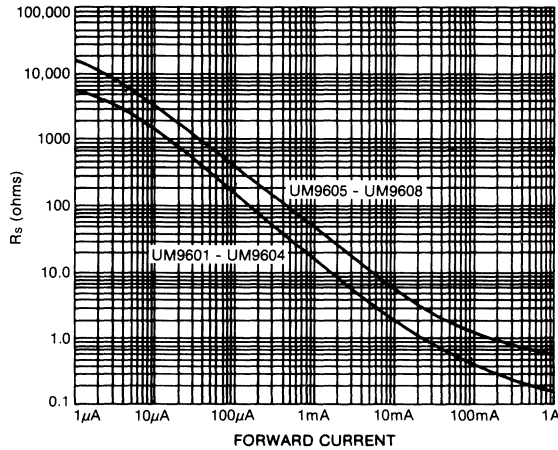
Operating and Storage Temperature	-65° C to +175° C
------------------------------------------	-------------------

Electrical Specifications (at 25° C)

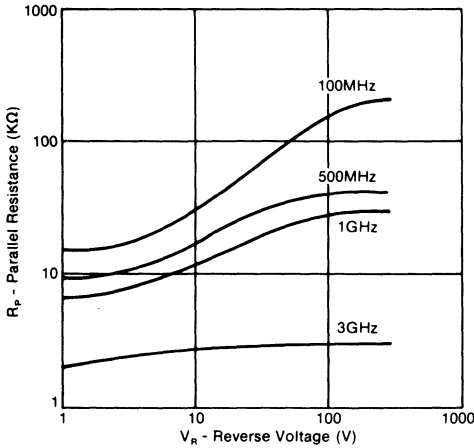
Test	Symbol	UM9601-UM9604			UM9605-UM9608			Units	Condition
		Min	Typ	Max	Min	Typ	Max		
Series Resistance	R _S	—	0.4	0.6	—	1.5	1.7	Ω	I = 100mA F = 1GHz
Parallel Resistance	R _P	5K	—	—	7K	—	—	Ω	Zero Bias F = 1GHz
Total Capacitance	C _T	—	—	1.2	—	—	0.5	pF	Zero Bias F = 1GHz
Carrier Lifetime	τ	2.0	—	—	1.0	—	—	μ S	I _F = 10mA
Forward Voltage	V _F	—	0.85	—	—	0.95	—	V	I _F = 100mA
I-Region Width	W	80	—	—	150	—	—	μ m	

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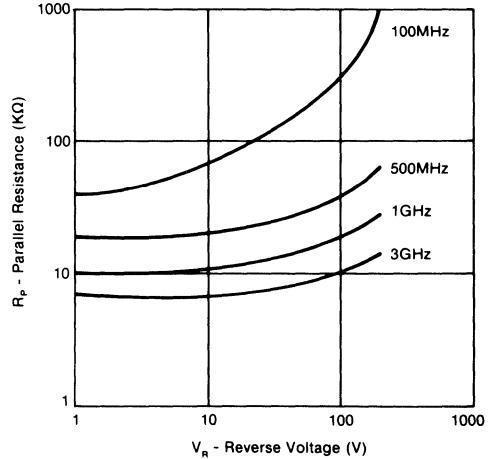
Typical Series Resistance vs Forward Current (F = 100MHz)



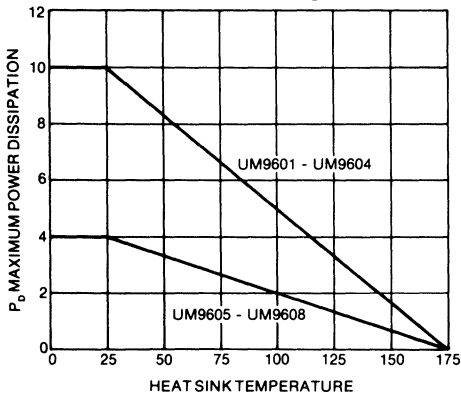
Typical R_p vs Voltage and Frequency UM9601 - UM9604



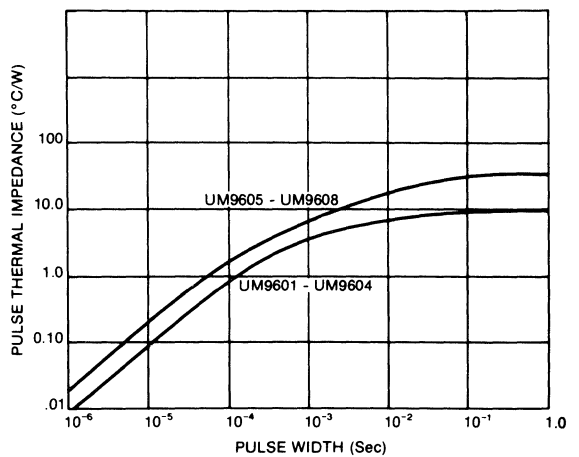
Typical R_p vs Voltage and Frequency UM9605 - UM9608



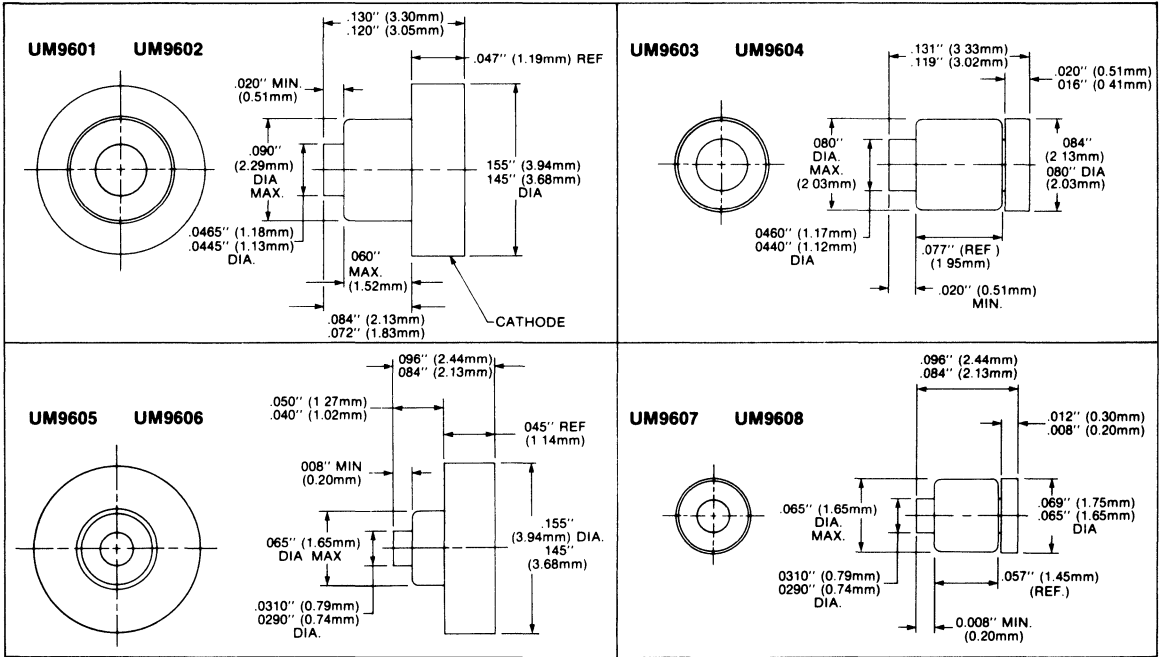
Power Rating



Pulse Thermal Impedance



Mechanical Specifications



Selection Guide

The following chart serves as a general guide for indicating the most likely diode from the series for a given application.

Applications	Recommended Types
1. High isolation switches to 2GHz at low dc drive 2. Quarter-wave antenna switches to 100 watts. 3. Priced for high volume commercial applications.	UM9601 (Affixes to microstrip ground plane.) UM9603 (Affixes to microstrip backing plate.)
High voltage rating version of UM9601 and UM9603 respectively for peak power handling to 3KW.	UM9602, UM9604
1. Low insertion loss switches to 4GHz. 2. Low distortion attenuator applications.	UM9605 (Affixes to microstrip ground plane.) UM9607 (Affixes to microstrip backing plate.)
High voltage version of UM9605 and UM9607 for peak power handling to 10KW.	UM9606, UM9608

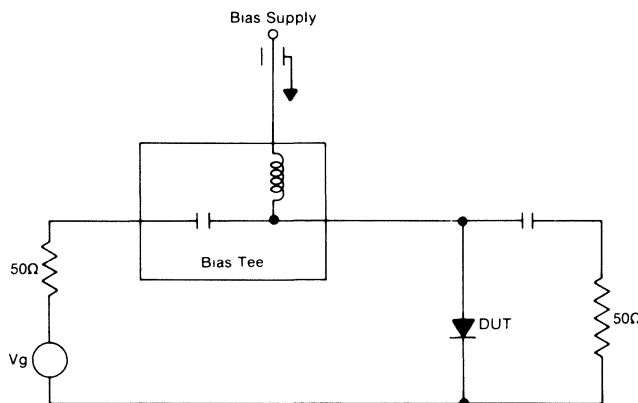
Microwave Characterization

The UM9601-UM9608 series has been designed and characterized as shunt switch elements at frequencies to 4GHz in microstrip circuits. Performance curves are given which demonstrate switch performance in 0.025" (.635mm) alumina microstrip.

The performance data were derived by evaluating externally biased microstrip circuits in which a UM9601 diode was installed. Each circuit consisted of a 1 inch length of 50 ohm nominal impedance 0.025" (.635mm) thick alumina microstrip and two SMA connectors. The data shown include the board and connector loss. Measurements performed using 0.050" (1.27mm) alumina substrates show similar performance at frequencies to 1.5GHz.

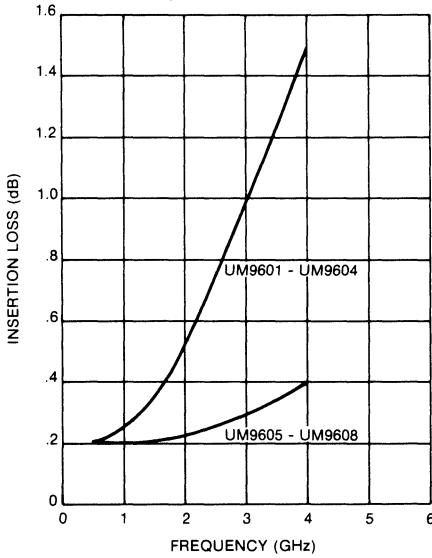
These circuits simulate simple SPST switches. Many designs require multithrow switches. It is important to recognize that a multithrow switch will have 6dB higher isolation than indicated for SPST switches. Also, a multithrow switch using shunt mounted PIN diodes require the diodes be placed a quarter-wavelength from the common port.

A further improvement in switch performance may be achieved by using 2 shunt PIN diodes in each arm spaced a quarter-wavelength from each other. In this case the isolation of each section will be twice the dB value of a SPST switch. The insertion loss due to the diodes should be less than twice the insertion loss of an SPST section due to the transforming effect of the quarter-wave line on the capacitance of a single diode.

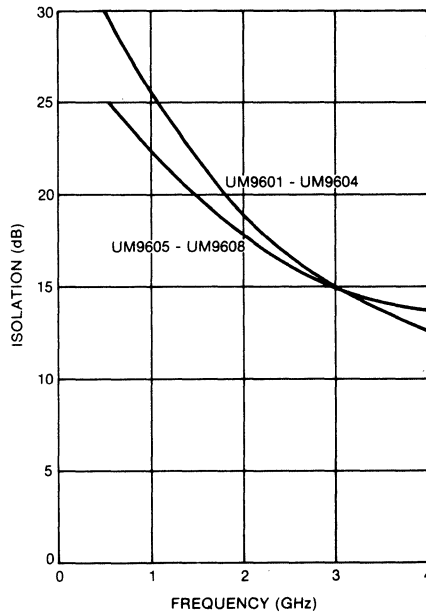


Microwave Test Circuit

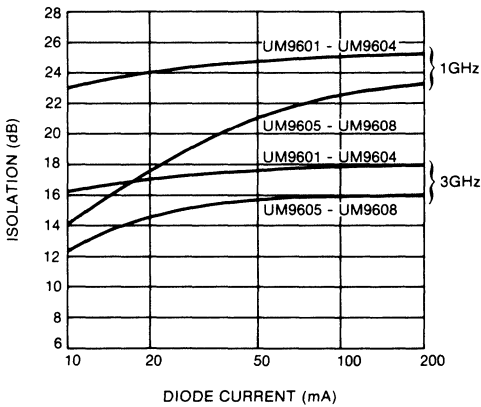
Typical Insertion Loss vs Frequency
0.025" (0.635mm) Alumina Microstrip SPST Switch
Diode at Zero Bias



Typical Isolation vs Frequency
0.025" (0.635mm) Alumina Microstrip SPST Switch
Diode Current = 100mA



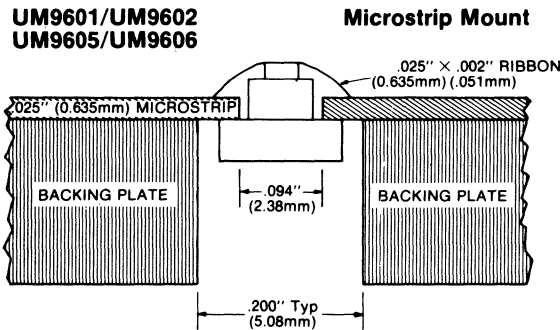
Isolation vs Frequency and Diode Current
0.025" (0.635mm) Alumina Microstrip SPST Switch



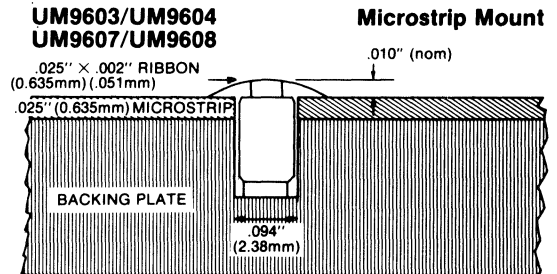
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Installation in Microstrip

The cup type flange on the UM9601, UM9602, UM9605 and UM9606 is designed to be affixed to the ground plane surface of a microstrip board as shown. The UM9603, UM9604, UM9607 and UM9608 were designed to be affixed to a backing plate as shown. It was experimentally determined that at frequencies greater than 2GHz the anode of the diode should be approximately 0.010" (.254mm) above the top surface of the microstrip for lowest insertion loss.



For solder adhesion the microstrip may be heated to solder melting temperature (up to 300°C) with no damage to the diode. Conductive epoxy may also be employed. The thermal resistance of solder mounted UM9601-UM9604 in their test boards was less than 20° C/W; for the UM9605-UM9608 thermal resistance was less than 30° C/W.



Design Example - 900MHz Antenna Switch

An example of a practical circuit design using a UM9601 diode is a quarter-wave antenna switch covering the frequency of 800-900MHz. The circuit design for this switch is shown and was constructed using 0.025" (0.645mm) alumina microstrip.

This antenna switch uses a series mounted diode and a shunt mounted diode. The UM9601 was selected for the shunt mounted device (SPST performance at 1GHz: 0.2dB insertion loss and 25dB isolation) and because it is the lowest cost diode in the UM9601-UM9608 series. A UM9401 axial lead diode was chosen for the series mounted device.

The performance of this switch is displayed in the graphs and in the following table. It should be noted that the loss values are actual measured numbers including losses due to the capacitors, bias networks, connectors as well as the board. In a typical radio application where the antenna switch circuit board is integrated in the same microstrip board that contains transmitter and receiver elements the connector loss is eliminated. This will result in lower overall insertion loss values than indicated here.

The CW power handling capacity is determined by the allowable power dissipation of the series mounted UM9401. Using a gap in the line of 0.190" (4.82mm) and lead soldered attached spacing of 0.250" (0.635mm) the power rating of the UM9401 is 6 watts at a 25° C ambient. This was determined by performing a thermal resistance measurement on the circuit mounted UM9401. The relationship that derives the maximum transmitter power, P_T, is:

$$P_T = \frac{P_{DISS}}{R^S} \cdot Z_o \left(\frac{\sigma + 1}{2\sigma} \right)^2$$

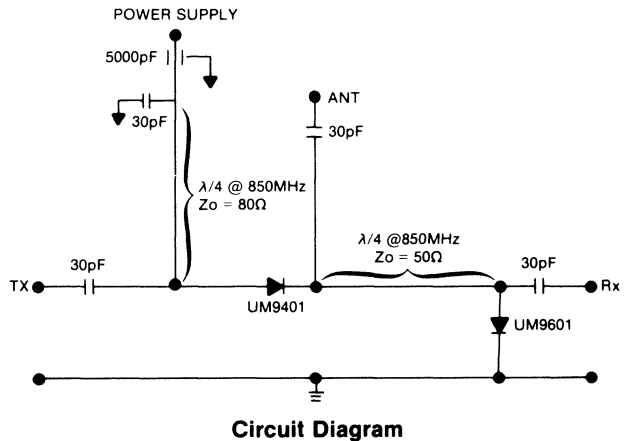
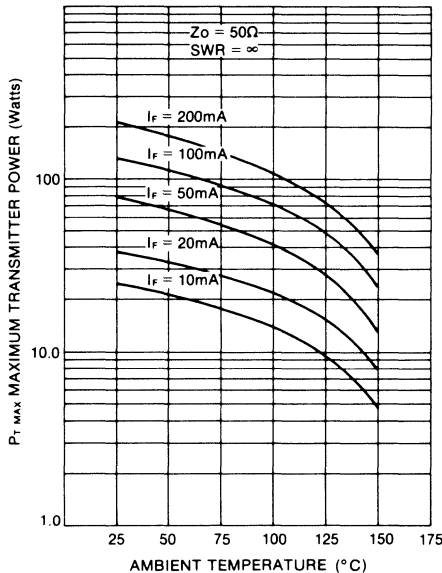
where σ = maximum antenna SWR

Using resistance values for the UM9401 and UM9601 the maximum transmitter power curve is given and shows that this circuit is able to handle 100 watts of transmitter power at 100mA forward biased and totally mismatched antenna at an ambient temperature of 60° C. For a perfectly matched antenna the power handling increases to 400 watts under the same bias and ambient temperature conditions.

Distortion is an important consideration in the selection of a PIN diode antenna switch design. The UM9401 and UM9601 PIN diodes are designed for low distortion applications. The level of distortion produced by this 900MHz antenna switch when operated in the transmit

state (forward bias of 100mA) is expected to be at least 90dB below the carrier for a 50 watt transmitter level. In the receiver state (zero bias) the intermodulation distortion caused by two in-band signals at 0dBm are estimated to be at least 100dB below this level.

Maximum Transmitter Power vs Forward Current for UM9601/UM9401 900MHz Microstrip Antenna Switch



Antenna Switch Performance

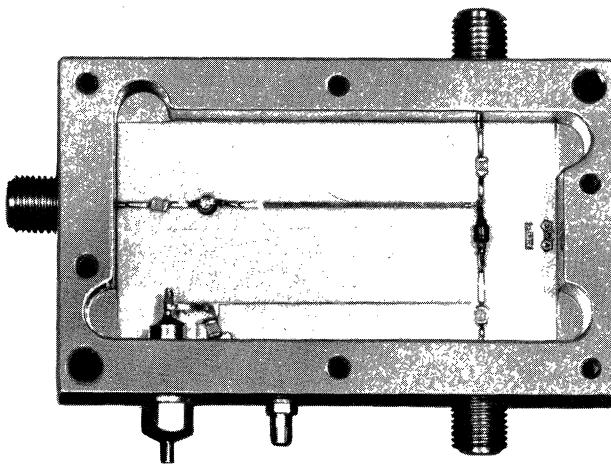
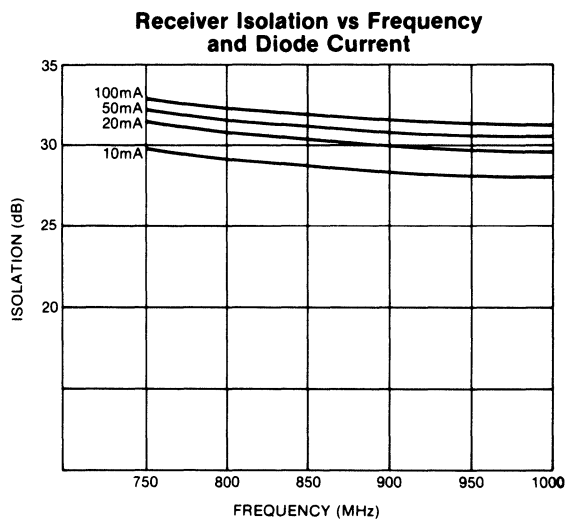
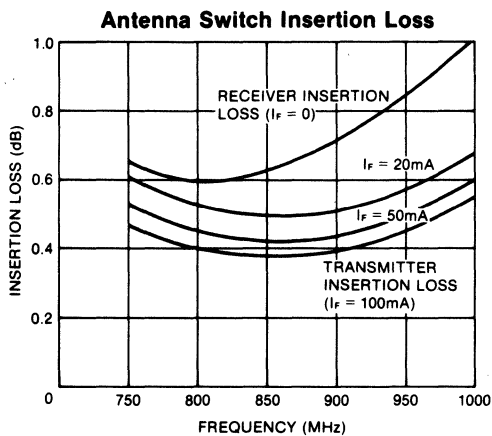
Frequency Range 800-900MHz

I. Transmit State
(I = 100mA, T_A = 60°C)

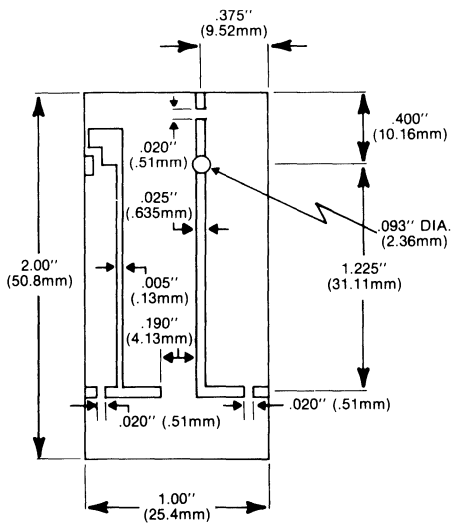
- A. Maximum Transmitter Power - 100 watts (antenna SWR = ∞)
- B. Maximum Transmitter Power - 400 watts (antenna SWR = 1)
- C. Transmitter Insertion Loss - 0.4dB
- D. Receiver Isolation - 31dB
- E. Harmonic Distortion - -90dB (P_T = 100 watts)

II. Receive State
(Zero Bias)

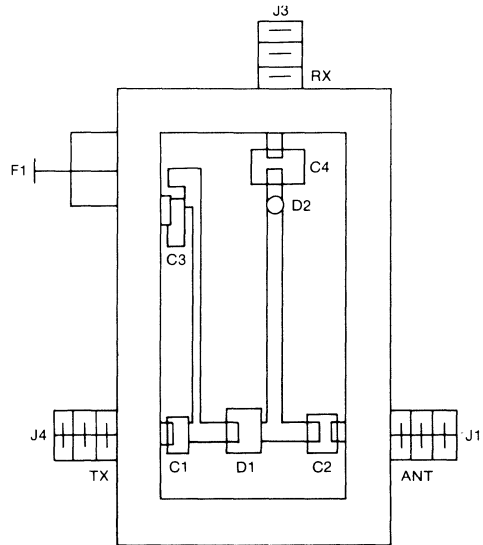
- A. Receiver Insertion Loss - 0.6-0.7dB
- B. Intermodulation Distortion - -100dB
P_{in} = 0dBm



Photograph of 800-900MHz antenna switch test module using UM9401 and UM9601 PIN Diodes. In typical transceiver applications, the antenna switch circuit board is integrated.



Substrate Drawing



Assembly Drawing

Parts List

F1	5000pF Feed through Filter	Erie 1270-016
C1-C4	30pF Chip Capacitor	Vitramon VJ0805A300KF
D1	PIN Diode	Unitrode UM9401
D2	PIN Diode	Unitrode UM9601
J1-J3	SMA Connector	Cablewave 971-028
	Substrate	Vectronics Microwave 79-9081-0401

PIN DIODE

UM9701

Low Resistance, Low Distortion, RF Switching Diode

Features

- Low Forward Resistance
- High Reverse Resistance
- Specified Low Distortion
- High Voltage Capability
- Good Power Handling
- Unitrode Ruggedness and Reliability

Description

The UM9701 PIN diode was designed for low resistance at low forward bias current and low reverse bias capacitance. This unique Unitrode design results in both forward and reverse bias.

These PIN diodes are characterized for low current drain RF and microwave switch applications particularly for digital filter switch designs. The construction and geometry of these devices provide good voltage and power handling capability.

These devices are constructed using a metallurgical full face bond to both surfaces of the silicon chip. A glass enclosure houses this bond in a reliable and hermetic package. The axial leads are attached to the refractory pins and do not touch the glass enclosure.

Environmentally these, and all Unitrode PIN diodes, can withstand thermal cycling from -195°C to $+300^{\circ}\text{C}$ and exceed all military environmental specifications for shock, vibration, acceleration, and moisture resistance.

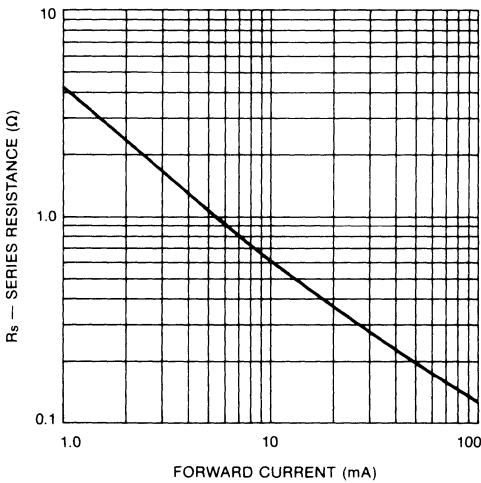
Maximum Ratings

Reverse Voltage	100V
Average Power Dissipation Free Air at 25°C	500mW (Derate linearly to 175°C)
Average Power Dissipation $\frac{1}{2}$ " Total Lead Length to 25°C Contacts	2.5W (Derate linearly to 175°C)
Operating and Storage Temperature	-65°C to $+175^{\circ}\text{C}$

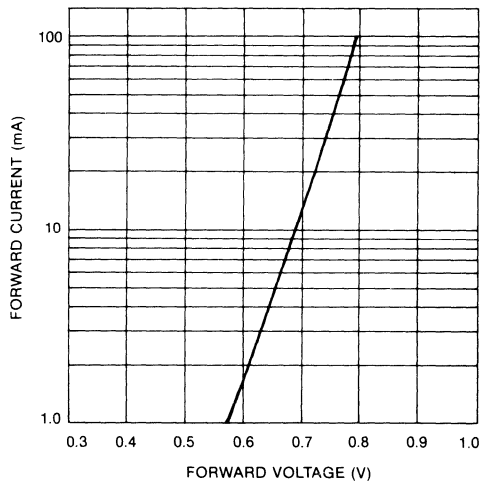
Electrical Specifications

Test	Symbol	UM9701	Condition
Series Resistance (MAX)	R_S	0.8Ω	$F = 100\text{MHz}$, $I = 10\text{mA}$
Total Capacitance (MAX)	C_T	1.8pF	$F = 1\text{MHz}$, $I = 50\text{V}$
Parallel Resistance (MIN)	R_P	$100\text{k}\Omega$	$F = 100\text{MHz}$, $V = 50\text{V}$
Carrier Lifetime (MIN)	τ	$1.5\mu\text{s}$	$I = 10\text{mA}$
Reverse Current (MAX)	I_R	$10\mu\text{A}$	$V = 100\text{V}$
Forward Voltage (MAX)	V_F	0.8V	$I = 10\text{mA}$
Forward Bias Third Order IM Distortion (MAX)	$R \frac{2ab}{a}$	-90dB	$I = 10\text{mA}$ $P_a = P_b = +20\text{dBm}$ $F_a = 43\text{MHz}$, $F_b = 44\text{MHz}$
Reverse Bias Third Order IM Distortion (MAX)	$R \frac{2ab}{a}$	-90dB	$I = 50\text{V}$ $P_a = P_b = +20\text{dBm}$ $F_a = 43\text{MHz}$, $F_b = 44\text{MHz}$

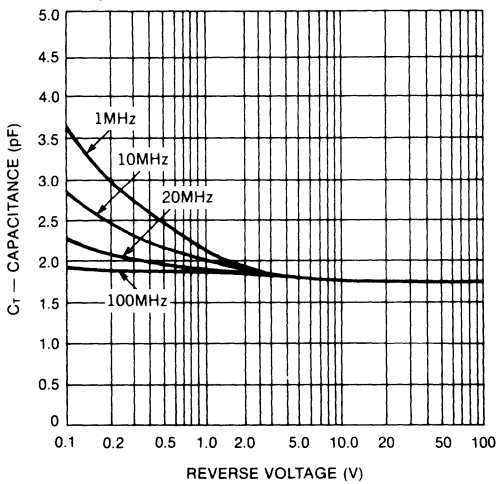
Typical Series Resistance vs Forward Current (F = 100MHz)



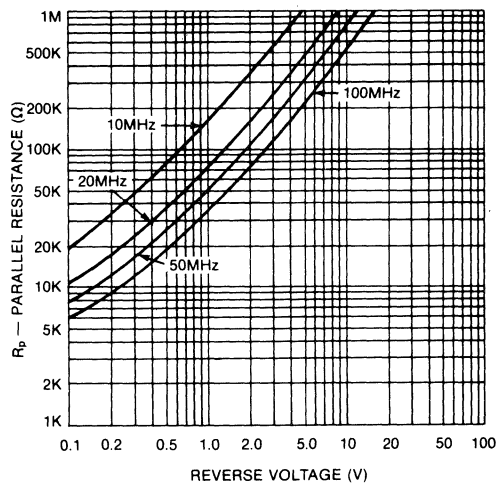
Typical DC Characteristic



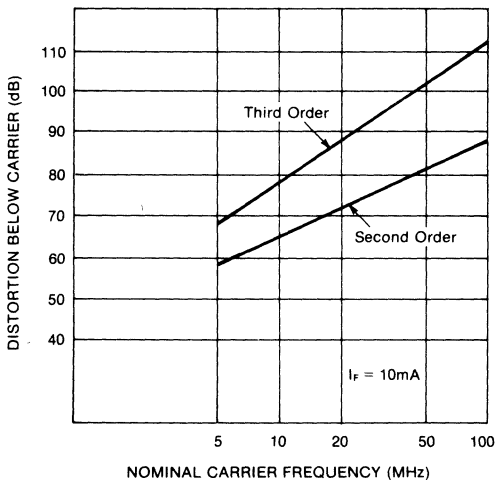
Typical Capacitance Characteristic



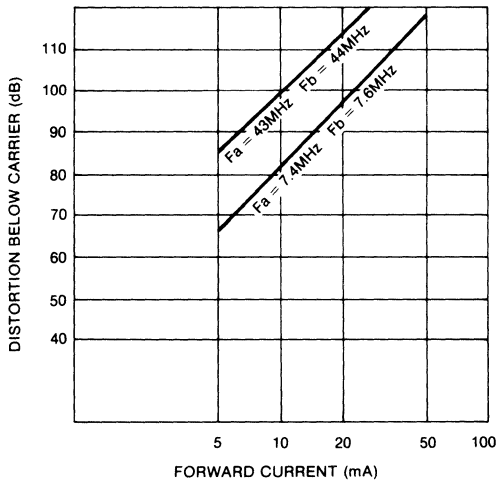
Typical Parallel Resistance Characteristic



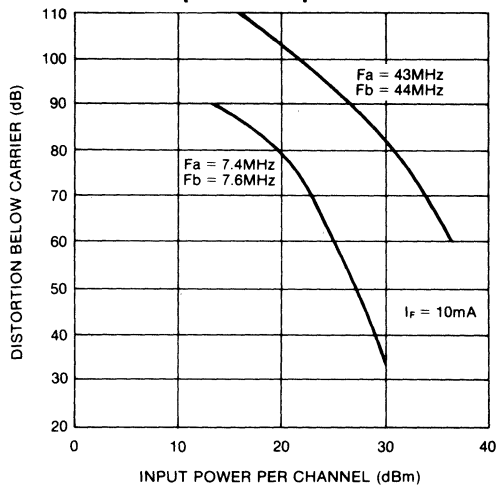
Typical Forward Bias Intermodulation Distortion vs Nominal Carrier Frequency at 20dBm per Channel



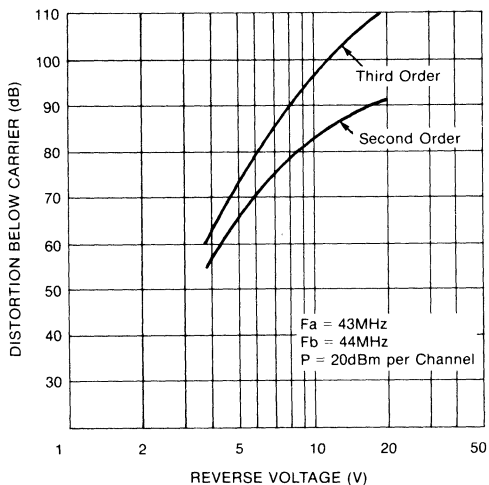
Typical Third Order Intermodulation Distortion ($R \frac{2ab}{a}$) vs Forward Bias Current at 20dBm per Channel



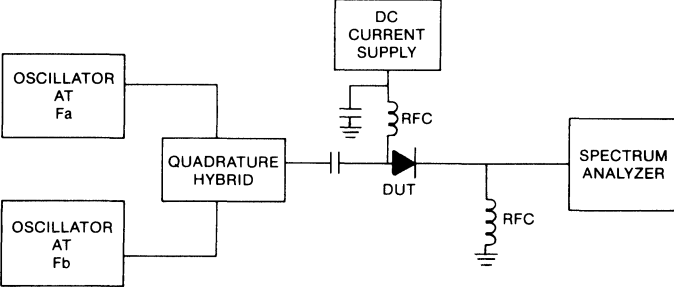
Typical Forward Bias Third Order Intermodulation Distortion ($R \frac{2ab}{a}$) vs Input Power per Channel



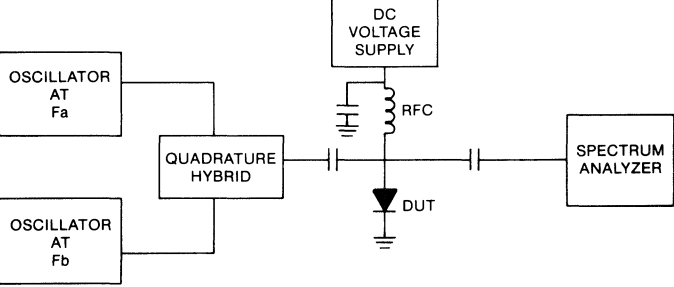
Typical Reverse Bias Intermodulation Distortion



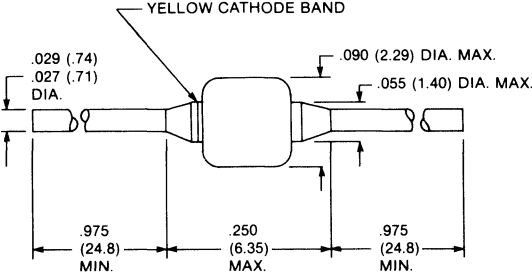
Forward Bias Distortion Test Set

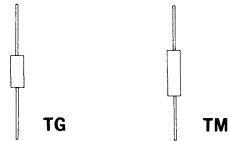


Reverse Bias Distortion Test Set



Mechanical Specifications



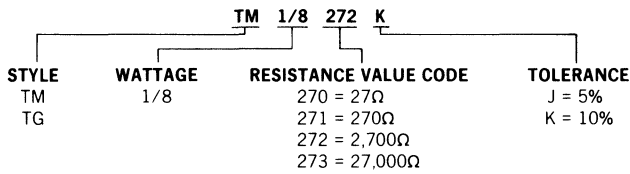


Type	Resistance Range (Ω)	Resistance Rating (R25°C/R125°C)	Tolerance	Package
TG1/8-J	10-10K	0.55±15%	5%	TG
TG1/8-K	10-10K	0.55±15%	10%	TG
TM1/8-J	10-39K	0.55±15%	5%	TM
TM1/8-K	10-39K	0.55±15%	10%	TM

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TYPE NUMBER DESIGNATION

TM1/8272K



SENSISTORS®

Positive – Temperature – Coefficient Silicon Thermistors

TG1/8
TM1/8

FEATURES

- Qualified to MIL-T-23648A
- TG1/8 – Similar to RTH42 (MIL-T-23648A/19)
- TM1/8 – Similar to RTH22 (MIL-T-23648A/9)
- Large Positive Temperature Coefficient $\approx 0.7\%/^{\circ}\text{C}$
- Wide Resistance Value Ranges Available in 5% or 10% Tolerances

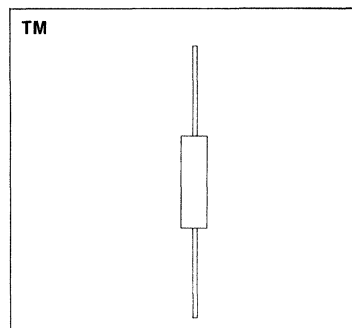
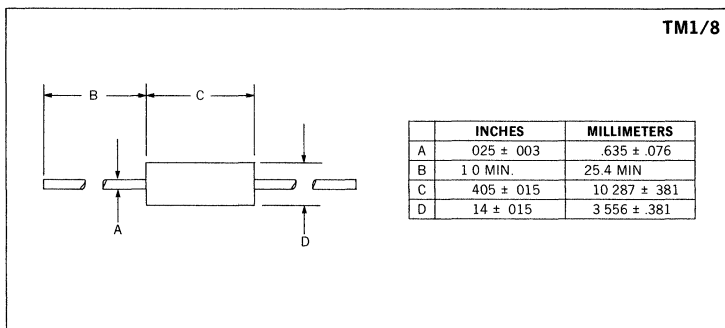
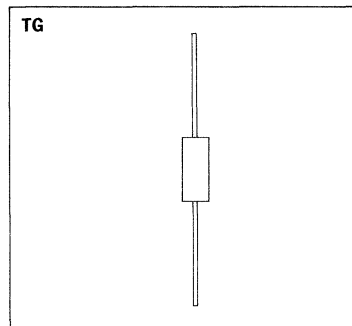
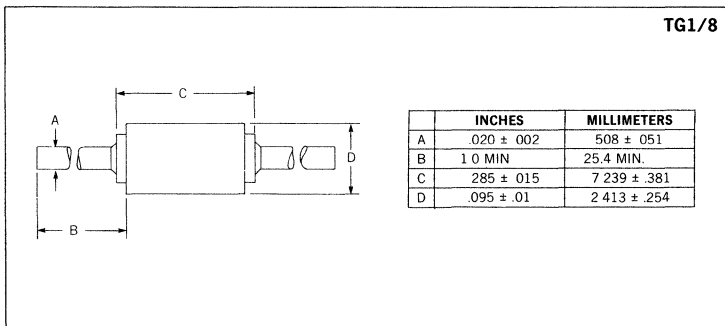
DESCRIPTION

The TG1/8 thermistor is encapsulated in a glass, hermetically sealed package. The TM1/8 thermistor is encapsulated in a molded package. Both have hot solder-dipped leads and are used in temperature sensing and compensation circuits. They meet or exceed all of the requirements of MIL-T-23648A.

ABSOLUTE MAXIMUM RATINGS

	TG1/8	TM1/8
Power Dissipation at (or below) 25°C Free-Air Temperature (See Figure 1).....	300mW.....	500mW
Power Dissipation at (or below) 100°C Free Air Temperature (See Figure 1).....	125mW
Operating Free-Air Temperature Range	-55°C to +125°C ..	
Storage Temperature Range	-65°C to +150°C ..	

MECHANICAL SPECIFICATIONS



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ELECTRICAL AND THERMAL CHARACTERISTICS

TG1/8 TM1/8

Zero Power Resistance Ratio ($R_{25^{\circ}\text{C}}/R_{125^{\circ}\text{C}}$) 0.55 ± 15%
 Thermal Time Constant - Typical 35s
 Thermal Time Constant - Maximum 60s

NOMINAL RESISTANCE AT VARIOUS TEMPERATURES

Standard Zero Power Resistance Value (Ω) at 25°C Free-Air Temperature	Type No.		Resistance (Ω) of Sensistor® at Temperature other than 25°C						
			-55°C	-15°C	0°C	50°C	75°C	100°C	125°C
10	TG1/8	TM1/8	6.15	7.9	8.63	11.6	13.5	15.45	17.5
12	TG1/8	TM1/8	7.38	9.48	10.356	13.92	16.2	18.54	21
15	TG1/8	TM1/8	9.225	11.85	12.945	17.4	20.25	23.175	26.25
18	TG1/8	TM1/8	11.07	14.22	15.534	20.88	24.3	27.81	31.5
22	TG1/8	TM1/8	13.53	17.38	18.986	25.52	29.7	33.99	38.5
27	TG1/8	TM1/8	16.605	21.33	23.301	31.32	36.45	41.715	47.25
33	TG1/8	TM1/8	20.295	26.07	28.479	38.28	44.55	50.985	57.75
39	TG1/8	TM1/8	23.985	30.81	33.657	45.24	52.65	60.255	68.25
47	TG1/8	TM1/8	28.905	37.13	40.561	54.52	63.45	72.615	82.25
50	TG1/8	TM1/8	30.75	39.5	43.15	58	67.5	77.25	87.5
56	TG1/8	TM1/8	34.44	44.24	48.328	64.96	75.6	86.52	98
68	TG1/8	TM1/8	41.82	53.72	58.684	78.88	91.8	105.06	119
82	TG1/8	TM1/8	47.724	63.14	69.454	95.94	112.34	129.888	147.6
100	TG1/8	TM1/8	58.2	77	84.7	117	137	158.4	180
120	TG1/8	TM1/8	69.84	92.4	101.64	140.4	164.4	190.08	216
150	TG1/8	TM1/8	87.3	115.5	127.05	175.5	205.5	237.6	270
180	TG1/8	TM1/8	100.8	135.9	150.84	212.4	252	292.14	334.8
220	TG1/8	TM1/8	123.2	166.1	184.36	259.6	308	357.06	409.2
270	TG1/8	TM1/8	151.2	203.85	226.26	318.6	378	438.21	502.2
330	TG1/8	TM1/8	184.8	249.15	276.54	389.4	462	535.59	613.8
390	TG1/8	TM1/8	218.4	294.45	326.82	460.2	546	632.97	725.4
470	TG1/8	TM1/8	263.2	354.85	393.86	554.2	658	762.81	874.2
500	TG1/8	TM1/8	280	377.5	419	590	700	811.5	930
560	TG1/8	TM1/8	308	414.4	467.6	672	795.2	927.36	1,075.2
680	TG1/8	TM1/8	374	503.2	567.8	816	965.6	1,126.08	1,305.6

13

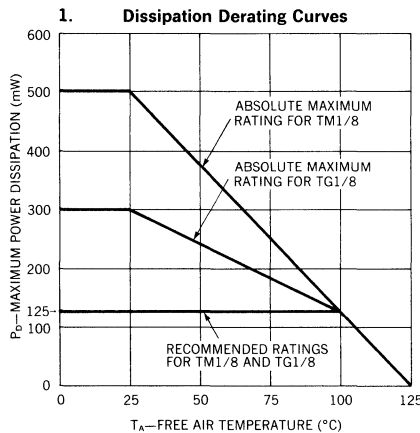
NOMINAL RESISTANCE AT VARIOUS TEMPERATURES

Standard Zero Power Resistance Value (Ω) at 25°C Free-Air Temperature	Type No.		Resistance (Ω) of Sensistor® at Temperature other than 25°C						
			-55°C	-15°C	0°C	50°C	75°C	100°C	125°C
820	TG1/8	TM1/8	451	606.8	684.7	984	1,164.4	1,357.92	1,574.4
1,000	TG1/8	TM1/8	550	740	835	1,200	1,420	1,656	1,920
1,200	TG1/8	TM1/8	660	888	1,002	1,440	1,704	1,987.2	2,304
1,500	TG1/8	—	772.5	1,095	1,237.5	1,845	2,175	2,505	2,940
	—	TM1/8	825	1,110	1,252.5	1,800	2,130	2,484	2,880
1,800	TG1/8	TM1/8	927	1,314	1,485	2,214	2,610	3,006	3,528
2,200	TG1/8	TM1/8	1,133	1,606	1,815	2,706	3,190	3,674	4,312
2,700	TG1/8	TM1/8	1,390.5	1,971	2,227.5	3,321	3,915	4,509	5,292
3,300	TG1/8	TM1/8	1,699.5	2,409	2,722.5	4,059	4,785	5,511	6,468
3,900	TG1/8	TM1/8	2,008.5	2,847	3,217.5	4,797	5,655	6,513	7,644
4,700	TG1/8	TM1/8	2,420.5	3,431	3,877.5	5,781	6,815	7,849	9,212
5,000	TG1/8	TM1/8	2,575	3,650	4,125	6,150	7,250	8,350	9,800
5,600	TG1/8	TM1/8	2,884	4,088	4,620	6,888	8,120	9,352	10,976
6,800	TG1/8	—	3,468	4,964	5,610	8,092	9,520	10,948	12,444
	—	TM1/8	3,502	4,964	5,610	8,364	9,860	11,356	13,328
8,200	TG1/8	—	4,182	5,986	6,765	9,758	11,480	13,202	15,006
	—	TM1/8	4,223	5,986	6,765	10,086	11,890	13,694	16,072
10,000	TG1/8	—	5,100	7,300	8,250	11,900	14,000	16,100	18,300
	—	TM1/8	5,150	7,300	8,250	12,300	14,500	16,700	19,600
12,000	—	TM1/8	6,180	8,760	9,900	14,760	17,400	20,040	23,520
15,000	—	TM1/8	7,215	10,680	12,210	18,150	21,450	25,050	28,500
18,000	—	TM1/8	8,658	12,816	14,652	21,780	25,740	30,060	34,200
22,000	—	TM1/8	10,582	15,664	17,908	26,620	31,460	36,740	41,800
27,000	—	TM1/8	12,987	19,224	21,978	32,670	38,610	45,090	51,300
33,000	—	TM1/8	15,873	23,496	26,862	39,930	47,190	55,110	62,700
39,000	—	TM1/8	18,759	27,768	31,746	47,190	55,770	65,130	74,100

DEVICE TOLERANCE

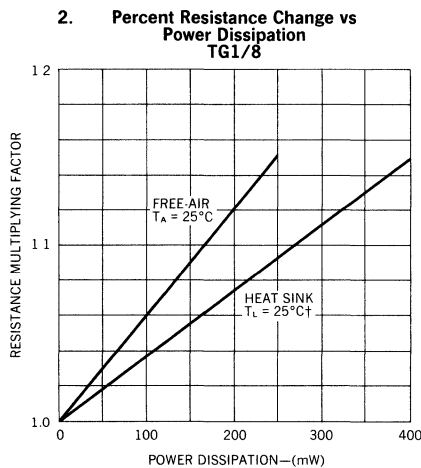
The actual resistance of the thermistor at T/°C may vary from the calculated value by an amount not exceeding the tolerances tabulated below.

Temperature	±5%	±10%
(°C)	(J)	(K)
-55	±15%	±20%
-15	±9%	±14%
0	±7%	±12%
25	±5%	±10%
50	±7%	±12%
75	±9%	±14%
100	±12%	±17%
125	±15%	±20%

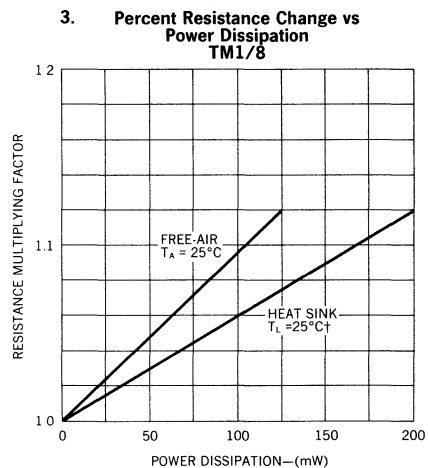


TYPICAL CHARACTERISTICS WITH POWER APPLIED

To determine resistance value with power applied, obtain a multiplying factor from the applicable curve below. The free-air curve is for the condition of heat removal by free-air convection only. The heat sink curve is for the maximum cooling rate condition of a heat sink strap, with leads attached to an infinite heat sink. Actual conditions encountered will be between these two extremes. After selecting an applicable multiplying factor from figure 2 or 3, multiply this by the 25°C zero power resistance. This product is then corrected for the actual ambient temperature by use of the appropriate temperature column in the Nominal Resistance at Various Temperatures table.

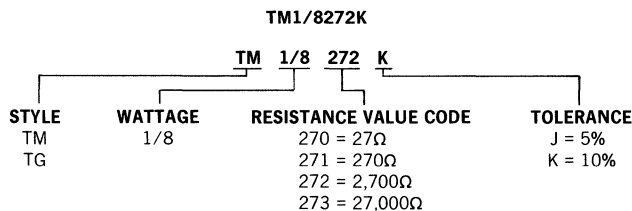


† T_L is lead temperature measured 1/16 inch from the body.



† T_L is lead temperature measured 1/16 inch from the body.

PART NUMBER DESIGNATION



MONOLITHIC CERAMIC CAPACITORS

Facilities and Capabilities

Unitrode, long recognized as a worldwide leader in the design, manufacture and marketing of discrete semiconductor components, has established a comparable position of leadership in the manufacture of Multilayer Ceramic Capacitors.

Since 1973, Unitrode has supplied over one billion *Axial Leaded Multilayer Ceramic Capacitors* to computer, general industrial, and commercial customers. Consequently the Company is recognized as a leading supplier of automatically insertable capacitors for high volume applications.

Our modern facilities in San Diego, California; Methuen, Massachusetts; and Ennis, Ireland are producing both Glass Encapsulated and Hybrid Chip Capacitors to service our domestic and international customers.

Our unique manufacturing and sealing process combined with continual emphasis on quality have earned Unitrode a reputation of setting the highest standards of reliability and performance.

Unitrode's Multilayer Ceramic Capacitors are utilized in numerous and varied applications in such end markets as data processing, consumer electronics, communications/telecommunications, automotive regulators and ignition systems, industrial controls, industrial and medical instrumentation, and military electronics.

The Company's corporate Marketing and Sales headquarters are located in Lexington, Massachusetts. Strategically located Area and Regional Sales Offices backed by a worldwide network of the industry's most qualified team of manufacturers' representatives are prepared to provide any assistance you require to solve your capacitor problems and satisfy your requirements.

General Information

Basic Formula

Capacitors are essentially energy storage devices used in a wide variety of applications in the electronics industry. The most common applications are:

- Pulse circuits
- Timing circuits
- Tuning
- Energy Storage
- By-Pass
- Blocking
- Coupling
- Voltage Suppression
- Arc Suppression

The Multilayer Ceramic Capacitor is a parallel plate capacitor with a ceramic material as the dielectric whose capacitance can be calculated by a formula

$$C = \frac{KAN}{t} \text{ where:}$$

- K = the dielectric constant of the ceramic material utilized.
- A = the area of overlap of the plate electrodes in in²
- N = the number of electrode plates.
- t = thickness of the dielectric material separating the electrode plates in inches.

Classes/Characteristics

Multilayer Ceramic Capacitors are generally divided into Class I and Class II categories:

Class I Ceramics

Capacitors of this dielectric type have a dielectric constant range of 6-100 for the temperature compensated series dielectrics and from 100-500 for an extended TC series. Class I devices are used in applications requiring stability and high Q-factor (low loss) over a temperature range of -55°C to +125°C and exhibit the following characteristics:

- a. Time does not significantly affect capacitance and dissipation factor. No aging.
- b. Capacitance and dissipation factor are not affected by voltage and frequency.
- c. Linear temperature coefficient.
- d. Dissipation factor is typically <0.1% @ 1 MHz.

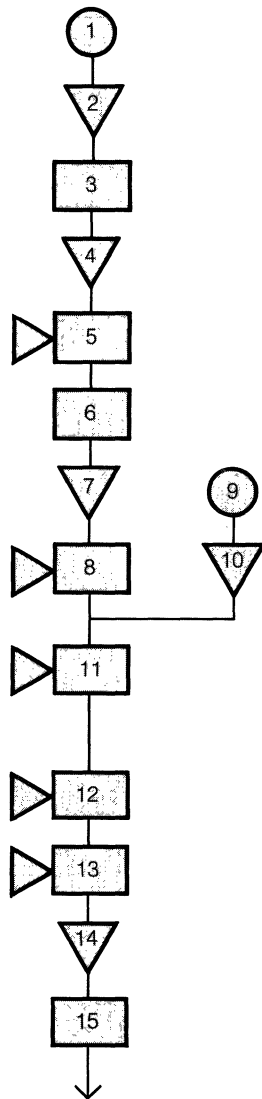
Class II Ceramics

Class II Ceramics are divided into two subgroups, stable and unstable, which are defined by the temperature characteristics. For the stable subgroup, the dielectric constant range is generally 500-3000, and 3000-10000 for the unstable subgroup. BX and X7R dielectrics are examples of the stable subgroup dielectrics. Z5U falls into the unstable subgroup. These higher K dielectrics exhibit non-linear characteristics and less stable properties than the Class I Ceramics, namely:

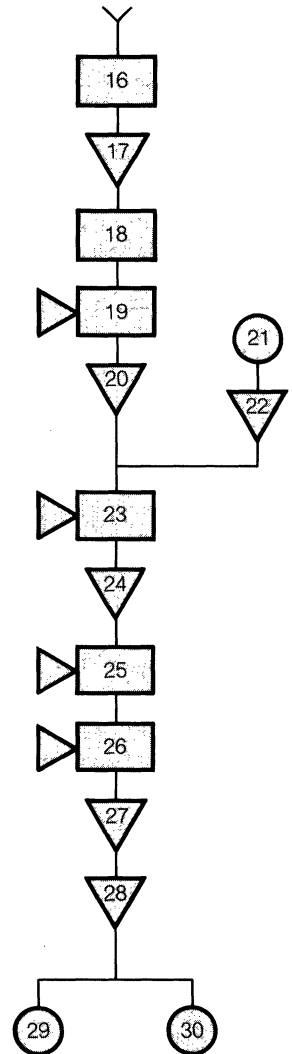
- a. Capacitance and dissipation factor are affected by (1) time (aging), (2) voltage (AC & DC), and (3) frequency.
- b. Non linear T.C.

Class II Ceramic devices are used in by-pass and coupling applications where some degree of electrical instability can be tolerated to achieve higher volumetric efficiency and lower cost.

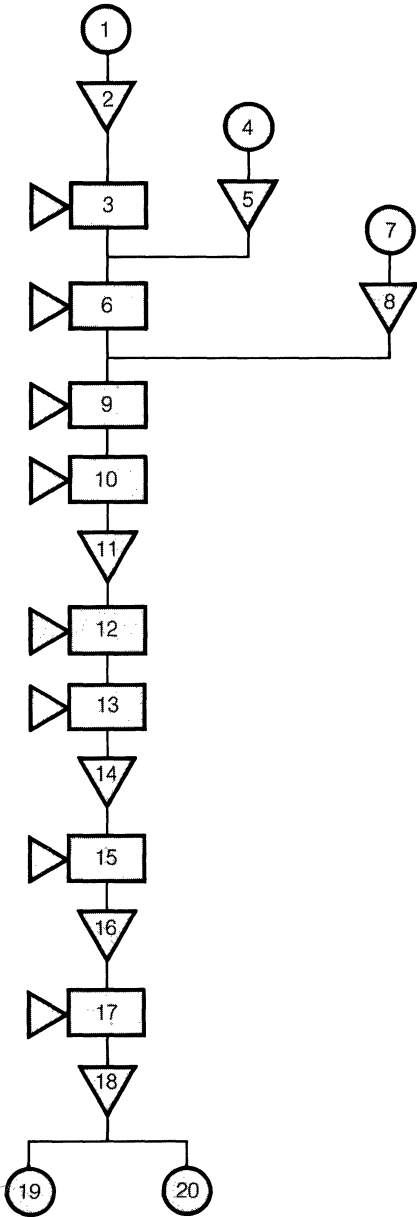
Chip Capacitor Production and Inspection Plan



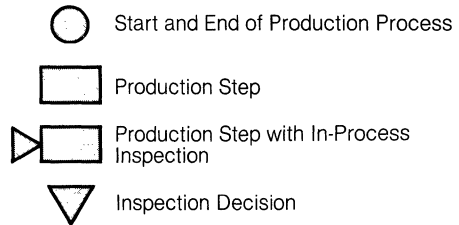
1. Incoming Ceramic and binders
2. Incoming Inspection
3. Mixing Ceramic and Binders
4. QA Sample Inspection
5. Cast
6. Slit
7. Ceramic Film Inspection
8. Block Load
9. Incoming Material—Inks and Screens
10. Incoming Inspection
11. Print
12. Laminate
13. Cut
14. Cut Inspection
15. Dry
16. Tumble
17. Tumble Inspection
18. Bisque Fire
19. Fire
20. Microsection Inspection
21. Incoming Material—Termination Metal
22. Incoming Inspection
23. Termination
24. Termination Inspection
25. Termination Fire
26. Electrical Sort
27. Visual Mechanical Inspection
28. Final QA
29. Chip Storage
30. Transfer for Encapsulation



**Glass Encapsulated Capacitor
Production and Inspection Plan**



1. Incoming Material — Leads
2. Lead Inspection
3. Lead Loading
4. Incoming Material — Glass
5. Glass Inspection
6. Glass Loading
7. Incoming Material — Chips
8. Chip Inspection
9. Chip Loading
10. Sealing
11. Encapsulated Assembly Inspection
12. Lead Plating
13. Electrical Test
14. Electrical Inspection
15. Marking
16. Inspection
17. Reel and Reel Repair
18. Final Q.C.
19. Stock
20. Ship



Test Specifications

Unitrode conducts the following tests on all production lots. The tests are monitored or conducted and controlled by the Quality Assurance Department to assure the specification and test limit integrity is maintained.

CAPACITANCE: Capacitance is checked on 100% of each shipment lot with a final check on an AQL basis. Test conditions for NPO and X7R dielectrics are 1 VRMS \pm .25 VRMS and .3 VRMS for the Z5U.

DISSIPATION FACTOR: This parameter is also checked on a 100% basis. The limits are .1 % for NPO 2.5% for X7R and 3% for Z5U at stated test voltages.

DIELECTRIC WITHSTANDING VOLTAGE: All dielectrics are tested at 250% of rated voltage with charging current limited to 50 mA maximum.

INSULATION RESISTANCE: Capacitors are tested to an AQL level at rated voltage for a maximum two minute charging time. All dielectrics are required to meet 100,000 megohms or 1000 megohm microfarads whichever is the lesser of the two.

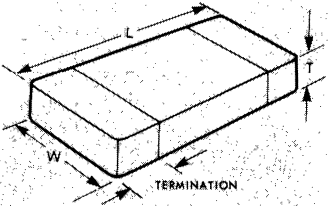
All above specifications are at room temperature and humidity. Specific details are given for each dielectric on pages 9 through 11 under Dielectric Characteristics Information Section.

HIGH RELIABILITY: All Unitrode product is manufactured to meet or exceed MIL-C-55681, MIL-C-11015 and MIL-C-39014 and Unitrode is prepared to offer for a nominal charge, units screened to the following specifications:

Test	MIL-STD-202 Method	Condition	Test Conditions
Burn-In	108	A	200% of rated voltage @ + 125°C for NPO and X7R dielectrics. 150% of rated voltage @ + 85°C for Z5U dielectric; for 96 hours.
Dielectric Withstanding Voltage	301	—	250% of rated voltage for NPO, X7R and Z5U dielectric with charging current limited to 50 mA.
Insulation Resistance	302	—	Rated voltage applied for 2 minutes maximum.
Thermal Shock	107	B	Exposure at temperature extremes for 30 minutes.
Capacitance	305	—	NPO and X7R dielectrics; 1 VRMS \pm .25 VRMS @ 1 KHz. Z5U dielectric; .3 VRMS @ 1 KHz.
Dissipation Factor	305	—	NPO and X7R dielectrics; 1 VRMS \pm .25 VRMS @ 1 KHz. Z5U dielectric; .3 VRMS @ 1 KHz.

**Unitrode Monolithic
Ceramic Capacitor Chips**

NPO (COG) Characteristics



Performance Specifications

MIL Specifications:
Meets or exceeds applicable portions of MIL-C-55681

Insulation Resistance:
Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Flash Test:
2.5 x WVDC

Life Test:
2 x WVDC @ +125°C, 1000 hours.

Temperature Range:
-55°C to +125°C

Temperature Coefficient:
0 ±30 PPM/°C

Dissipation Factor:
.1% max. @ 1 KHz

Capacitance Tolerance:
C (±.25pF, 1pF-10pF), D (±.5pF, 1pF-10pF), F (±1%), G (±2%), J (±5%), K (±10%), M (±20%)

- *All L&W values ±.010 (.254)
- **All termination measurements ±.010 (.254) except .010 (.254) value which is ±.005 (.127)

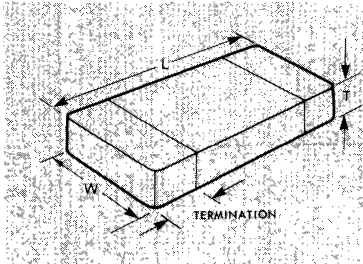
Extended value available

SIZE	1	2	3	4	5	6	7	8	9	24	
L	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.100 ins. 2.54 (mm)	.150 ins. 3.81 (mm)	.125 ins. 3.18 (mm)	.180 ins. 4.57 (mm)	.180 ins. 4.57 (mm)	.175 ins. 4.45 (mm)	.250 ins. 6.35 (mm)	.090 ins. 2.28 (mm)	
W	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.095 ins. 2.41 (mm)	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.125 ins. 3.18 (mm)	.225 ins. 5.72 (mm)	.070 ins. 1.77 (mm)	
T. MAX	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	
** Termination	.010 ins. .254 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	EIA
Capacitance pF	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	Capacitance Code
10											100
12											120
15											150
18											180
22											220
27											270
33											330
39											390
47											470
56											560
68											680
82											820
100											101
120											121
150											151
180											181
220											221
270											271
330											331
390											391
470											471
560											561
680											681
820											821
1000											102
1200											122
1500											152
1800											182
2200											222
2700											272
3300											332
3900											392
4700											472
5600											562
6800											682
8200											822
.0100 mF											103
.0120											123
.0150											153
.0180											183
.0220											223
.0270											273
.0330											333
.0390											393
.0470											473
.0560											563

How To Order

SIZE CODE	D VOLTAGE	103 VALUE	K TOLERANCE	P TERMINATION MATERIAL	N TEMPERATURE CHARAC- TERISTIC
1 050 x 040	C 25VDC	Capacitance Value in pF (EIA Code)	C ± 25pF (1pF-10pF)	A Ag	N NPO
2 080 x 050	D 50VDC		D ± 5pF (1pF-10pF)	B PdAg	B BX
3 100 x 050	E 100VDC		F ± 1%	C Solder Coat (604 Ag STANDARD)	X X7R
4 150 x 050	F 200VDC		G ± 2%		Z Z5U
5 125 x 095			J ± 5%		
6 180 x 050			K ± 10%		
7 180 x 080			M ± 20%		
8 175 x 125					
9 250 x 225					

X7R (BX) Characteristics



Performance Specifications

MIL Specifications:

Meets or exceeds applicable portions of MIL-C-55681

Insulation Resistance:

Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Flash Test:

2.5 × WVDC

Life Test:

2 × WVDC @ 125°C, 1000 hours.

Temperature Range:

-55°C to +125°C

Temperature Coefficient:

±15%

Dissipation Factor:

2.5% max. @ 1 KHz, 25°C, 1 VRMS

Capacitance Tolerances and Codes:

K (±10%), M (±20%) Z (+80%, -20%), V (GMV) Consult Factory for J (±5%) Tolerance

* All L&W values ±.010 (.254)

** All termination measurements ±.010 (.254) except .010 (.254) value which is ±.005 (.127)

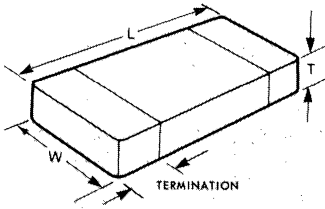
Extended value available

SIZE	1	2	3	4	5	6	7	8	9	24	
L	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.100 ins. 2.54 (mm)	.150 ins. 3.81 (mm)	.125 ins. 3.18 (mm)	.180 ins. 4.57 (mm)	.180 ins. 4.57 (mm)	.175 ins. 4.45 (mm)	.250 ins. 6.35 (mm)	.090 ins. 2.28 (mm)	
W	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.095 ins. 2.41 (mm)	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.125 ins. 3.18 (mm)	.225 ins. 5.72 (mm)	.070 ins. 1.77 (mm)	
T. MAX	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	
** Termination	.010 ins. .254 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	EIA
Capacitance	pF	Volts	Volts	Volts	Volts	Volts	Volts	Volts	Volts	Volts	Capacitance
	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	25 50 100	Code
100											101
120											121
150											151
180											181
220											221
270											271
330											331
390											391
470											471
560											561
680											681
820											821
1000											102
1200											122
1500											152
1800											182
2200											222
2700											272
3300											332
3900											392
4700											472
5600											562
6800											682
8200											822
.0100 mF											103
.0120											123
.0150											153
.0180											183
.0220											223
.0270											273
.0330											333
.0390											393
.0470											473
.0560											563
.0680											683
.0820											823
.1000											104
.1200											124
.1500											154
.1800											184
.2200											224
.2700											274
.3300											334
.3900											394
.4700											474
.5600											564
.6800											684
.8200											824
1.000											105
1.200											125
1.5											155

How To Order

SIZE CODE	D VOLTAGE	103 VALUE	K TOLERANCE	P TERMINATION MATERIAL	N TEMPERATURE CHARACTERISTIC
1 050 x 040	C 25VDC	Capacitance Value in pF (EIA Code)	C ± 25pF (1pF-10pF)	A Ag	N NPO
2 080 x 050	D 50VDC		D ± 5pF (1pF-10pF)	B PdAg	B BX
3 100 x 050	E 100VDC		F ± 1%	C Solder Coat (604 Ag STANDARD)	X X7R
4 150 x 050	F 200VDC		G ± 2%		Z Z5U
5 125 x 095			J ± 5%		
6 180 x 050			K ± 10%		
7 180 x 080			M ± 20%		
8 175 x 125					
9 250 x 225					

Z5U Characteristics (General Purpose)



Performance Specifications

MIL Specifications:

Meets or exceeds applicable portions of MIL-C-55681

Insulation Resistance:

Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Flash Test:

2.5 x WVDC

Life Test:

2 x WVDC @ 85°C.

Temperature Range:

+10°C to +85°C

Temperature Coefficient:

+22%

-56%

Dissipation Factor:

3.0% max. @ 1 KHz, 25°C, .3 VRMS

Capacitance Tolerances and Codes:

M (±20%) Z (+80%, -20%), V (GMV)

*All L&W values ±.010 (.254)

**All termination measurements ±.010 (.254) except .010 (.254) value which is ±.005 (.127)

SIZE	1	2	3	4	5	6	7	8	9	24	
L	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.100 ins. 2.54 (mm)	.150 ins. 3.81 (mm)	.125 ins. 3.18 (mm)	.180 ins. 4.57 (mm)	.180 ins. 4.57 (mm)	.175 ins. 4.45 (mm)	.250 ins. 6.35 (mm)	.090 ins. 2.28 (mm)	
W	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.095 ins. 2.41 (mm)	.050 ins. 1.27 (mm)	.080 ins. 2.03 (mm)	.125 ins. 3.18 (mm)	.225 ins. 5.72 (mm)	.070 ins. 1.77 (mm)	
T. MAX	.040 ins. 1.016 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.050 ins. 1.27 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	.060 ins. 1.52 (mm)	
Termination	.010 ins. .254 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	.020 ins. .508 (mm)	EIA
Capacitance pF	Volts 25 50 100	Volts 25 50 100	Volts 25 15 100	Volts 25 50 100	Volts 25 50 100	Volts 25 50 100	Volts 25 50 100	Volts 25 50 100	Volts 25 50 100	Volts 25 50 100	Capacitance Code
1000											102
1200											122
1500											152
1800											182
2200											222
2700											272
3300											332
3900											392
4700											472
5600											562
6800											682
8200											822
.0100 mF											103
.0120											123
.0150											153
.0180											183
.0220											223
.0270											273
.0330											333
.0390											393
.0470											473
.0560											563
.0680											683
.0820											823
.1000											104
.1200											124
.1500											154
.1800											184
.2200											224
.2700											274
.3300											334
.3900											394
.4700											474
.5600											564
.6800											684
.8200											824
1.000											105
1.200											125
1.500											155
1.800											185
2.200											225
2.700											275
3.300											335
3.900											395

How To Order

SIZE CODE	D VOLTAGE	103 VALUE	K TOLERANCE	P TERMINATION MATERIAL	N TEMPERATURE CHARACTERISTIC
1 050 x 040	C 25VDC	Capacitance	C ± 25pF (1pF-10pF)	A Ag	N NPO
2 080 x 050	D 50VDC	Value in pF	D ± 5pF (1pF-10pF)	B PdAg	B BX
3 100 x 050	E 100VDC	(EIA Code)	F ± 1%	C Solder Coat	X X7R
4 150 x 050	F 200VDC		G ± 2%	(604 Ag STANDARD)	Z Z5U
5 125 x 095			J ± 5%		
6 180 x 050			K ± 10%		
7 180 x 080			M ± 20%		
8 175 x 125					
9 250 x 225					

Chip Capacitor Tape and Reel Information

General

Table 1 indicates the chip size/capacitance value range of chips available in tape and reel packaging. The 8 mm wide cardboard carrier tape is supplied on 7 inch diameter reels. Each reel contains approximately 3000 devices.

Table 1

EIA SIZE CODE	L	W	T MAX	CAP VALUE RANGE		
				NPO 100 WVDC	XTR 50 WVDC	Z5U 50 WVDC
0504	.050 ± .010 (1.27 ± 0.25)	.040 ± .010 (1.02 ± 0.25)	.030 (0.76)	1.0pf 180pf	100pf 390pf	1000pf .015MF
0805	.080 ± .010 (2.03 ± 0.25)	.050 ± .010 (1.27 ± 0.25)	.050 (1.27)	1.0pf 390pf	100pf .015MF	1000pf .047MF
1005	.100 ± .010 (2.54 ± 0.25)	.050 ± .010 (1.27 ± 0.25)	.060 (1.52)	1.0pf 820pf	100pf .027MF	1000pf .082MF
1206	.126 ± .010 (3.2 ± 0.25)	.063 ± .010 (1.6 ± 0.25)	.050 (1.27)	47pf 1800pf	820pf .056MF	3300pf .15MF
1210	.125 ± .010 (3.18 ± 0.25)	.095 ± .010 (2.41 ± 0.25)	.065 (1.65)	100pf 2200pf	3900pf .082MF	4700pf .33MF
1505	.150 ± .010 (3.81 ± 0.25)	.050 ± .010 (1.27 ± 0.25)	.065 (1.63)	39pf 1200pf	560pf .039MF	1000pf .15MF

Reel Dimensions and Carrier Tape Dimensions

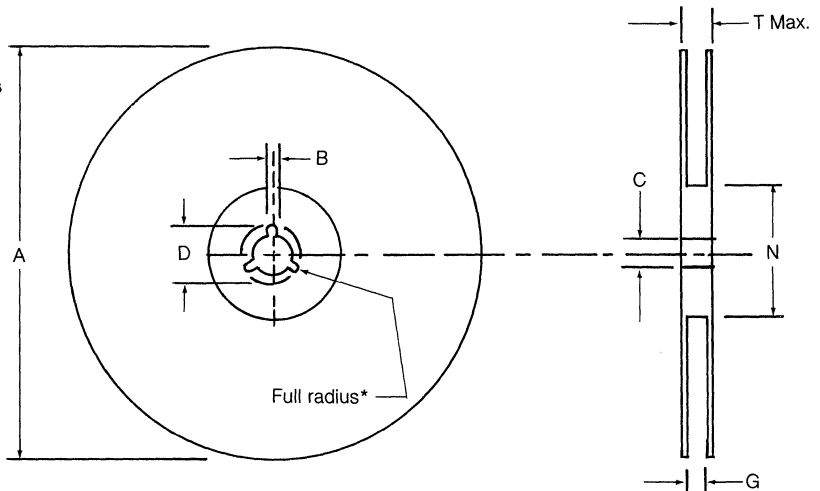


Table 2

A	B	C	D	N	G	T
178 ± 2.0 (7.00 ± 0.079)	2.0 (0.079)	13 ± 0.5 (0.512 ± 0.020)	20.2 MIN. (0.795 MIN.)	50 MIN. (1.969 MIN.)	10.0 ± 1.5 0.394 ± 0.059	14.9 (0.587)
Metric dimensions will govern. English measurements rounded and for reference only. Options subject to agreement between vendor and user.						

Carrier Dimensions

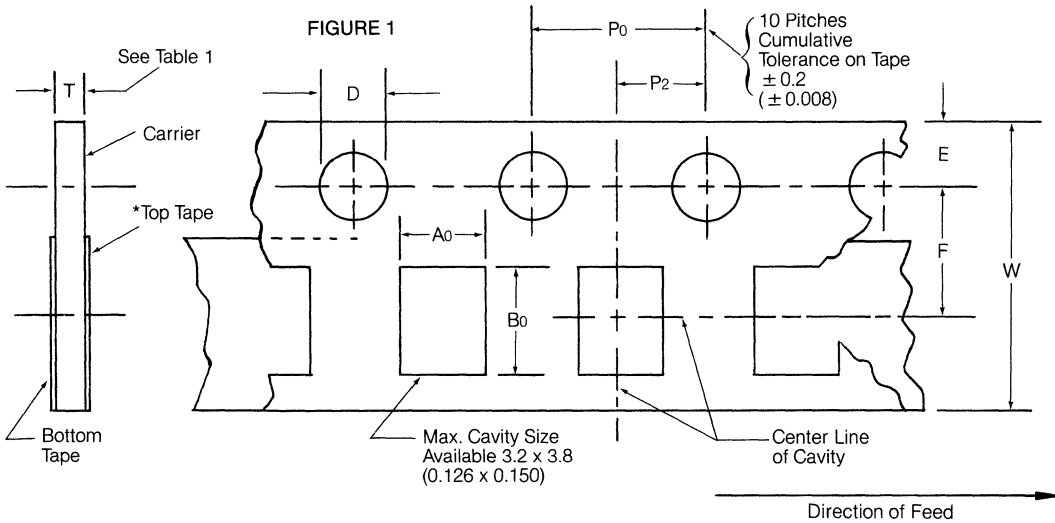


Table 3

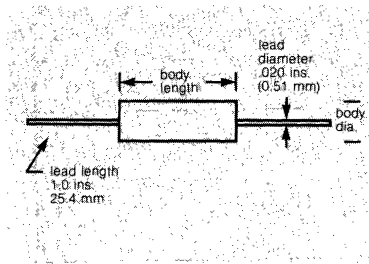
W	F	E	P ₂	P ₀	D	A ₀ , B ₀	T
8.0 ± 0.2 (0.315 ± 0.008)	* 3.5 ± 0.05 (0.138 ± 0.002)	1.75 ± 0.05 (0.069 ± 0.002)	2.0 ± 0.05 (0.079 ± 0.002)	4.0 ± 0.1 (0.157 ± 0.004)	1.5 ^{+0.1} _{-0.0} (0.059 ^{+0.004} _{-0.000})	See Note: 1	NO. 1 - 0.94 (0.037) NO. 2 - 1.19 (0.047)

Metric dimensions will govern.
 English measurements rounded and for reference only.
 Options subject to agreement between vendor and user.

NOTE: 1 A₀ & B₀ are determined by maximum specified length and width of components plus 0.4 ± 0.2 (0.016 ± 0.008), plus the additional requirements that components not be allowed to rotate more than 20° within the cavity clearance or whichever condition occurs first.

Unitrode Monolithic Ceramic Axial Lead Glass Capacitors

NPO (COG) Characteristics



Performance Specifications

MIL Specifications:

Meets or exceeds applicable portions of MIL-C-11015 and MIL-C-39014.

Insulation Resistance:

Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Dielectric Strength:

2.5 × WVDC

Life Test:

2 × WVDC @ 125°C, 1000 hours.

Lead Material:

Tinned Copper Clad Steel

Temperature Range:

-55°C to +125°C

Temperature Coefficient:

0 ±30 PPM/°C

Dissipation Factor:

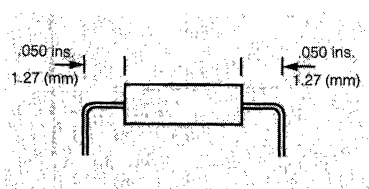
0.1 % max. at 1 MHz @ 1 VRMS (≤100pF)
1 KHz @ 1 VRMS (>100pF)

Capacitance Tolerance:

F (±1%), G (±2%), J (±5%),
K (±10%), M (±20%)

PACKAGE	B	C	D	E	F	EIA Code
Body Length (max.)	.170 ins. 4.32 (mm)	.200 ins. 5.08 (mm)	.260 ins. 6.60 (mm)	.300 ins. 7.62 (mm)	.400 ins. 10.16 (mm)	
Body Dia. (max.)	.100 ins. 2.54 (mm)	.100 ins. 2.54 (mm)	.100 ins. 2.54 (mm)	.110 ins. 2.79 (mm)	.150 ins. 3.81 (mm)	
Capacitance pF	Voltage 50 100 200	Voltage 50 100 200	Voltage 50 100 200	Voltage 50 100 200	Voltage 50 100 200	
10						100
12						120
15						150
18						180
22						220
27						270
33						330
39						390
47						470
56						560
68						680
82						820
100						101
120						121
150						151
180						181
220						221
270						271
330						331
390						391
470						471
560						561
680						681
820						821
1000						102
1200						122
1500						152
1800						182
2200						222
2700						272
3300						332
3900						392
4700						472
5600						562
6800						682
8200						822
.01 mF						103

Guidelines for Automatic Insertion:

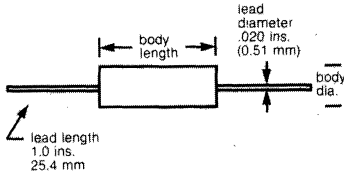


How To Order

STYLE	PACKAGE	EIA CAPACITANCE CODE	TOLERANCE	VOLTAGE	TEMPERATURE CHARACTERISTIC
CG	A 170 x 075 B 170 x 100 C 200 x 100 D 260 x 100 E 300 x 110 F 400 x 150 G 300 x 150	Capacitance Value in pF	F ± 1% G ± 2% J ± 5% K ± 10% M ± 20% Z ± 80% -20% V GMV	C 25V D 50V E 100V F 200V	N NPO X X7R Z Z5U

*Consult factory for values and voltages

X7R (BX) Characteristics



Performance Specifications

MIL Specifications:

Meets or exceeds applicable portions of MIL-C-11015 and MIL-C-39014.

Insulation Resistance:

Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Dielectric Strength:

2.5 × WVDC

Life Test:

2 × WVDC @ 125°C, 1000 hours.

Lead Material:

Tinned Copper Clad Steel

Temperature Range:

-55°C to +125°C

Temperature Coefficient:

±15%

Dissipation Factor:

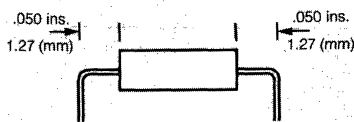
2.5% @ 1 KHz @ 1 VRMS

Capacitance Tolerance:

K (±10%), M (±20%) Consult Factory for J (±5%) Tolerance

PACKAGE	A	B	C	D	E	F	EIA Capacitance Code
Body Length (max):	.170 ins. 4.32 (mm)	.170 ins. 4.32 (mm)	.200 ins. 5.08 (mm)	.260 ins. 6.60 (mm)	.300 ins. 7.62 (mm)	.400 ins. 10.16 (mm)	
Body Dia. (max):	.075 ins. 1.91 (mm)	.100 ins. 2.54 (mm)	.100 ins. 2.54 (mm)	.100 ins. 2.54 (mm)	.110 ins. 2.79 (mm)	.150 ins. 3.81 (mm)	
Capacitance pF	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	
100							101
120							121
150							151
180							181
220							221
270							271
330							331
390							391
470							471
560							561
680							681
820							821
1000							102
1200							122
1500							152
1800							182
2200							222
2700							272
3300							332
3900							392
4700							472
5600							562
6800							682
8200							822
.01 mF							103
.012							123
.015							153
.018							183
.022							223
.027							273
.033							333
.039							393
.047							473
.056							563
.068							683
.082							823
.10							104
.12							124
.15							154
.18							184
.22							224
.27							274

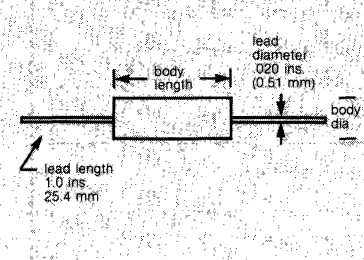
Guidelines for Automatic Insertion:



How To Order

STYLE	PACKAGE	EIA CAPACITANCE CODE	TOLERANCE	VOLTAGE	TEMPERATURE CHARACTERISTIC
CG	A 170 x 075 B 170 x 100 C 200 x 100 D 260 x 100 E 300 x 110 F 400 x 150 G 300 x 150	Capacitance Value pF	F ± 1% G ± 2% J ± 5% K ± 10% M ± 20% Z ± 80%, -20% V GMV	C 25V D 50V E 100V F 200V	N NPO X X7R Z Z5U

**Z5U Characteristics
(General Purpose)**



Performance Specifications

Insulation Resistance:
Minimum 100,000 megohms or 1,000 megohm microfarads, whichever is less, with rated voltage applied, @ 25°C (see curve for other temperatures).

Dielectric Strength:
2.5 × WVDC below .5 mfd; 2.0 × WVDC .5 mfd and above

Life Test:
2 × WVDC @ 85°C, 1000 hours.

Lead Material:
Tinned Copper Clad Steel

Temperature Range:
+10°C to +85°C

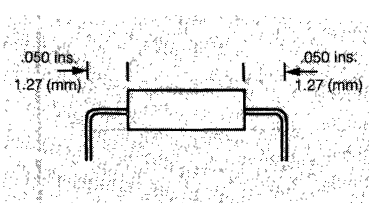
Temperature Coefficient:
+22, -56%

Dissipation Factor:
3.0% max. at 1 KHz., 25°C, @ .3 VRMS

Capacitance Tolerance:
M (±20%), Z (+80%, -20%), GMV (+100%, -0%).

PACKAGE	A	B	C	E	F	EIA Capacitance Code
Body Length (max.)	.170 ins. 4.32 (mm)	.170 ins. 4.32 (mm)	.200 ins. 5.08 (mm)	.300 ins. 7.62 (mm)	.400 ins. 10.16 (mm)	
Body Dia. (max.)	.075 ins. 1.91 (mm)	.100 ins. 2.54 (mm)	.100 ins. 2.54 (mm)	.110 ins. 2.79 (mm)	.150 ins. 3.81 (mm)	
Capacitance pF	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	Voltage 25 50 100	
1000						102
1200						122
1500						152
1800						182
2200						222
2700						272
3300						332
3900						392
4700						472
5600						562
6800						682
8200						822
.01 mF						103
.012						123
.015						153
.018						183
.022						223
.027						273
.033						333
.039						393
.047						473
.056						563
.068						683
.082						823
.10						104
.12						124
.15						154
.18						184
.22						224
.27						274
.33						334
.39						394
.47						474
.56						564
.68						684
.82						824
1.0						105

Guidelines for Automatic Insertion:



How To Order

STYLE	PACKAGE	EIA CAPACITANCE CODE	TOLERANCE	VOLTAGE	TEMPERATURE CHARACTERISTIC
CG	A 170 x 075 B 170 x 100 C 200 x 100 D 260 x 100 E 300 x 110 F 400 x 150 *G 300 x 150	Capacitance Value in pF	F ± 1% G ± 2% J ± 5% K ± 10% M ± 20% Z + 80% - 20% V GMV	C 25V D 50V E 100V F 200V	N NPO X X7R Z Z5U

*Consult factory for values and voltages

APPLICATION AND DESIGN DATA

SUBJECT	PAGE	SUBJECT	PAGE
LINEAR INTEGRATED CIRCUITS		POWER HYBRIDS & MODULES	
A Second Generation — IC Switch Mode Controller Optimized for High Frequency Power Mosfet Drive (U-89)	15-137	Switching Regulator Design Guide (U-68A)	15-13
The UC1524A Integrated PWM Control Circuit Provides New Performance Levels for an Old Standard (U-90)	15-148	Flyback and Boost Switching Power Supplies (U-76)	15-46
Applying the UC1840 to Provide Total Control for Low-Cost, Primary-Referenced Switching Power Systems (U-91)	15-160	Detecting Impending Core Saturation in Switched-Mode Power Converters (U-81)	15-68
A New Integrated Circuit for Current-Mode Control (U-93)	15-170	Hybrid Circuits for Low Voltage Switched-Mode Converters (U-82)	15-76
The UC1901 Simplifies the Problem of Isolated Feedback in Switching Regulators (U-94)	15-179	Hybrid Circuits for Off-Line Switching Power Supplies (U-84)	15-89
A Simple Isolation Amplifier Using the UC1901 (DN-19)	15-240	Minimizing Storage Time When Using Unitorde Switching Regulator Power Output Circuits (DN-3)	15-215
PIN DIODES		Avoiding Spurious Oscillation When Using Unitorde Switching Regulator Power Output Circuits (DN-4)	15-216
Pin Diode Designers' Handbook & Catalog (PD500B)	*	Operating the Switching Regulator Output Circuit at Low Frequencies (DN-6)	15-220
POWER TRANSISTORS & DARLINGTONS		A 350 Watt Switching Regulated Output Power Supply for Multiple Outputs Utilizing Unitorde Semiconductor Components (DN-8)	15-224
Power Darlingtons as Switching Devices (U-70B)	*	THYRISTORS (SCRs & PUTs)	
The Unitorde monolithic power Darlington is characterized and compared with other switching methods. Unique advantages are discussed and basic circuits for many modern applications are shown.		Programmable Unijunction Transistors (U-66)	15-5
Thermal Design Considerations for Operating Unitorde's TO-92 Transistors and Darlingtons in Pulsed-Power Applications (U-77)	15-55	Incorporate Active Inrush Current Limiting to Improve Reliability and Efficiency of Power Supplies (U-83)	15-85
500W, 200kHz Off-Line Power Supply Using Power MOSFETs (U-87)	15-115	Squib-Firing Circuit Provides for Reliable Firing, from Low Level Inputs (DN-10)	15-230
Design Considerations for Power MOSFET Gate Drive Circuitry (U-88)	15-121	Combined AC-DC Load Control Simplifies SCR Reset (DN-11)	15-232
Proportional Base Drive of Bipolar Power Transistors in Switching Power Supplies (D1)	15-191	Turn-off Method for SCRs Minimizes Effect of DV/DT (DN-13)	15-234
How to Safely Check Sustaining Voltage on Power Transistors (DN-5)	15-217	Nanosecond SCR Switch for Reliable High Current Pulse Generators and Modulators (DN-14)	15-236
RECTIFIERS		Nanosecond SCR Switch for Laser Diode Pulse Driver (DN-15)	15-238
The Importance of Rectifier Characteristics in Switching Power Supply Design (U-73A)	15-35	TRANSIENT VOLTAGE SUPPRESSORS/ZENERS	
Design Guide - Power Schottky Rectifiers in a Switching Regulator (U-85)	15-99	Guidelines for Using Transient Voltage Suppressors (U-79)	15-59
RECTIFIER ASSEMBLIES, HIGH VOLTAGE RECTIFIERS		Determining the Change in Zener Voltage when the Current is Changed (DN-1A)	15-214
Doorbell® High Voltage Stacking (N-136B)	*	DESIGN REVIEW	
Self-stacking rectifier modules are described and shown in numerous applications. Examples of circuits and mounting configurations are given.		250 Watt Off-Line Forward Converter Design Review (T1)	15-198
Doorbell® Tube Replacement (N-130B)	*		
The advantages of using rectifier modules to replace tubes are discussed. Case histories are noted and advice is given relating to module selection and installation. Pertinent ratings and other information is presented in tabular form, and outlines are shown for standard caps and bases.			

*Does not appear in Databook.

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PROGRAMMABLE UNIJUNCTION TRANSISTORS

INTRODUCTION

The Programmable Unijunction Transistor is today's preferred device for low cost timing circuits, oscillators, sensing circuits, and a wide range of other applications where a variable voltage level threshold is desired. This note describes the principle of operation of the PUT, its electrical characteristics, and its various applications.

PRINCIPLE OF OPERATION

The PUT is a three-terminal device as shown in the schematic representation, Fig. 1a. The anode voltage V_A and the gate voltage V_G are measured with respect to the cathode (k). The corresponding anode, gate and cathode currents are given respectively by I_A , I_G , and I_K . The most general usage of a PUT involves an external gate resistor R_G as shown in Fig. 1a. Hence, the voltage generally referred to in characterizing PUT's is the applied voltage V_S rather than the gate voltage V_G which is less than V_S by the voltage drop across R_G .

The theory of operation of the PUT can perhaps be best understood by considering that it is a four-layer (PNPN) device, as is a silicon-controlled rectifier (SCR). The basic PUT structure is shown in Fig. 1b, in which it is noted that the gate is adjacent the anode, in contrast to an SCR in which the gate lead is adjacent the cathode. As shown in Fig. 1c, the PUT, has a two-transistor analogy, which is similar to that used to explain the operation of an SCR, except that the gate connection is common to the PNP base and the NPN collector. Regenerative switching occurs when the sum of the alpha's dynamically approach unity. The net result is that when the anode voltage exceeds the gate voltage by an amount equal to the emitter to base drop of the PNP transistor, the positive feedback drops the anode-cathode voltage and presents a negative resistance.

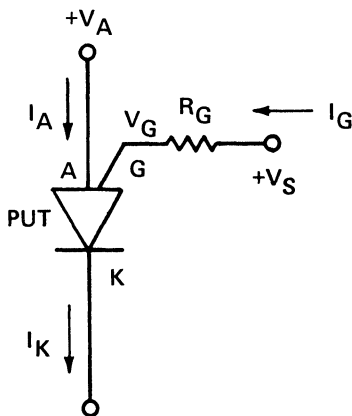


Figure 1a. PUT Parameters

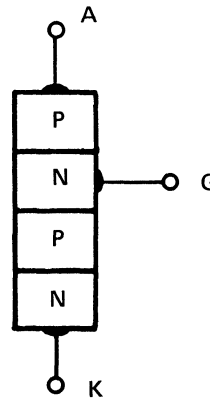


Figure 1b. PUT Structure

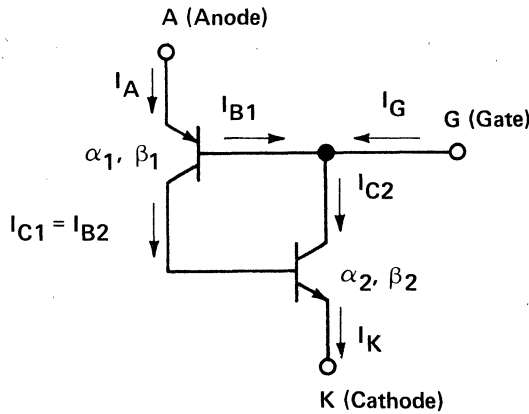


Figure 1c. Two Transistor Analogy

ANODE CHARACTERISTIC

The PUT, together with R_G as shown in Fig. 1a, exhibits a negative resistance characteristic illustrated in Fig. 2 for a fixed value of V_S and R_G . For anode voltages less than the peak voltage V_P at which a current I_{GA} flows. (Region I), a positive incremental resistance results. For anode currents above the valley current I_V , which occurs at the valley voltage V_V (Region III) a positive incremental resistance also occurs. However, for anode currents between the peak point current I_P and the valley current I_V (Region II) the incremental resistance is negative. This region is unstable and forms the basis for use in oscillator circuits. With V_A less than V_S forward anode current flows. At the peak current point, I_P where V_A exceeds V_P the PUT will regeneratively switch to its low impedance state: anode current increases rapidly to a level limited by external load resistance. The PUT will remain on this "ON STATE" until the anode current is reduced to a level below the valley current, I_V . At this point the PUT returns to its blocking or "OFF STATE", because operation in the negative region is unstable. Operation in the region between I_P and I_V will be covered in detail.

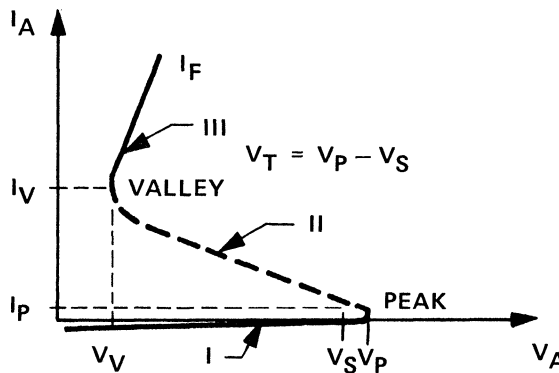


Figure 2. PUT Characteristics

ADVANTAGES

The primary advantage of the PUT over the UJT is the programmability of operating parameters such as peak point current (I_P), valley current (I_V), and offset voltage (V_T), which is defined as

$$V_T = V_P - V_S \tag{1}$$

These are easily programmed over a range by the choice of circuit components. Shown in Fig. 3 are the relationships between I_P and I_V vs stand off voltage (V_S) and gate source impedance (R_G). As observed from Fig. 3, operation at higher voltages allow a greater spread between I_P and I_V . The significance of this becomes apparent in applications where the negative resistance (Region II, Fig. 2) must be large and must remain relatively broad over a temperature range.

Other advantages of the PUT over the UJT are:

1. Lower current drain through R_1 and R_2 ; the UJT required several milliamperes of current, The PUT micro amperes of current.
2. Lower peak point current of the PUT allows use of larger R_T (timing resistor) therefore, the C_T may be smaller for the same time delay hence, lower in cost. Lower capacitance values also result in lower leakage current and lower temperature coefficient.
3. Higher efficiency is available due to greater energy transfer from the capacitor to the load. The on state voltage (V_F) is considerably lower for a PUT than for a UJT.
4. High or low operating voltages may be used; V_S as low as 2V or greater than 40V will operate the PUT.
5. The PUT has an overall extended operating range due to programmability of I_P and I_V .
6. Greater uniformity of triggering point. Stand off ratio η is not determined by manufacturing tolerance.

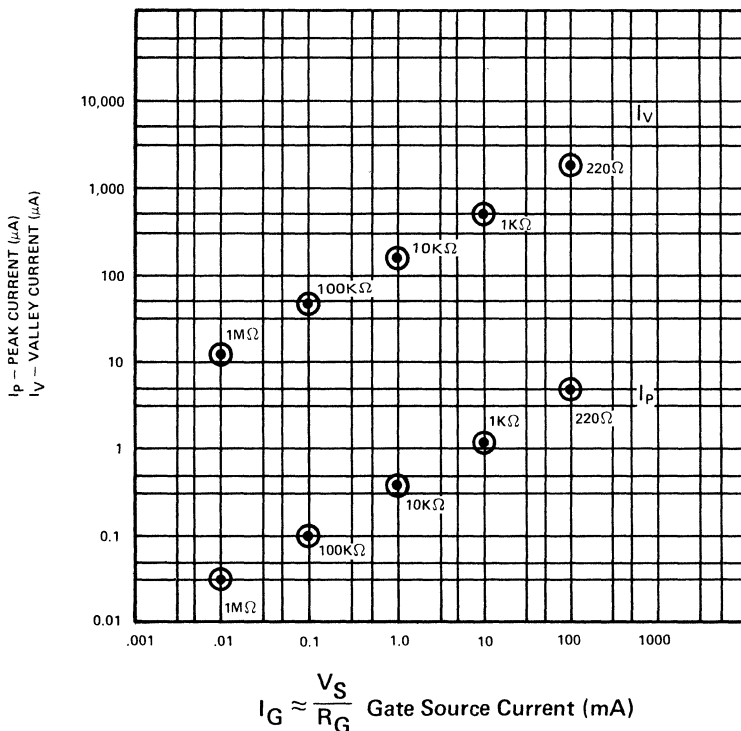


Figure 3.

BASIC PUT OSCILLATOR

An analysis of the basic PUT oscillator demonstrates the inter-relationship of parameters. From Fig. 4b, the voltage V_a changes at a rate determined by the $R_t C_t$ charging path. When the PUT is operating in Region I, the anode voltage is given by

$$V_a = V_{BB} (1 - e^{-t/R_t C_t}) \quad (2)$$

The standoff voltage is related to the supply voltage V_{BB}

$$V_S = \eta V_{BB} \quad (3)$$

where

$$\eta = \frac{R_1}{R_1 + R_2} \quad (4)$$

Triggering is accomplished when the voltage on the capacitor reaches the standoff voltage V_S ; plus the offset voltage V_T , i.e.

$$V_{BB} (1 - e^{-t/R_t C_t}) - V_T = \eta V_{BB} \quad (5)$$

The switching time occurs at

$$t = R_t C_t \ln \left(\frac{1}{1 - \eta \frac{V_{BB} + V_T}{V_{BB}}} \right) \quad (6)$$

V_T varies only slightly with temperature having a temperature coefficient of about 2.5 mv/°C.

Advantages of the PUT over the UJT are readily observed by comparing their operation in a simple relaxation oscillator circuit. Figure 4a shows a typical UJT oscillator with the simplified UJT model. In the off state the resistance ratio at the intersection of r_1 and r_2 is a fixed value represented by η (intrinsic stand off ratio). This ratio which determines the device triggering voltage is established in the manufacturing process by the resistance of the silicon material and the diode contact. Manufacturing tolerance result in values of η which typically range in value from about 0.4 to 0.9. Replacing the UJT with a PUT results in stable operation in any given circuit (Fig. 4b). The parameter stand-off ratio η is now established exclusively by setting the value of R_2 and R_1 and remains relatively temperature stable. I_p and I_V are controlled by gate source resistance R_g and stand off voltage V_S (Fig. 3). A detailed discussion of the PUT oscillator will be given.

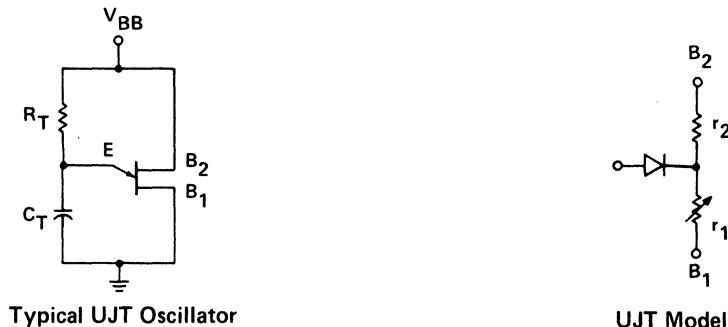
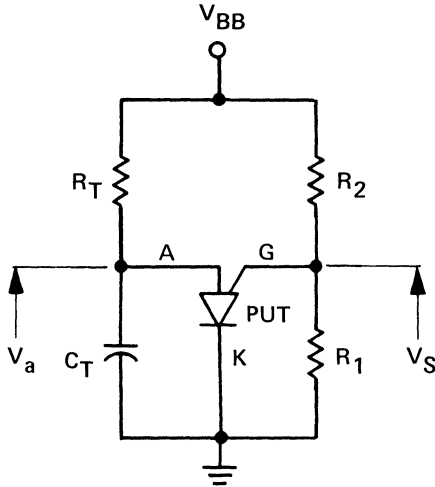


Figure 4a.



$$\eta = \frac{R_1}{R_1 + R_2} \quad \text{Standoff Ratio}$$

$$V_S = \eta V_{BB} \quad \text{Standoff Voltage}$$

$$V_T = V_P - V_S \quad \text{Offset Voltage}$$

$$R_G = \frac{R_1 R_2}{R_1 + R_2} \quad \text{Gate Source Resistance} \quad (7)$$

Fig. 4b

CONDITIONS FOR OSCILLATION

Switching on takes place at the peak point (I_P) switching off requires that current through the PUT be less than the valley current (I_V). Therefore, the load line must intersect the characteristic curve in the negative resistance region Fig. 5 and must be above the I_P point.

CONDITION FOR SUSTAINED OSCILLATION

$$\frac{V_{BB} - V_P}{R_T} (\text{max}) > I_P (\text{max}) \quad \text{This condition insures current levels greater than the } I_P \quad (8)$$

$$\frac{V_{BB} - V_V}{R_T} < I_V \quad \text{This condition insures current levels lower than the } I_V \quad (9)$$

$$1 - \eta \gg \frac{V_T}{V_{BB}} \quad \text{This condition insures more stable operation.} \quad (10)$$

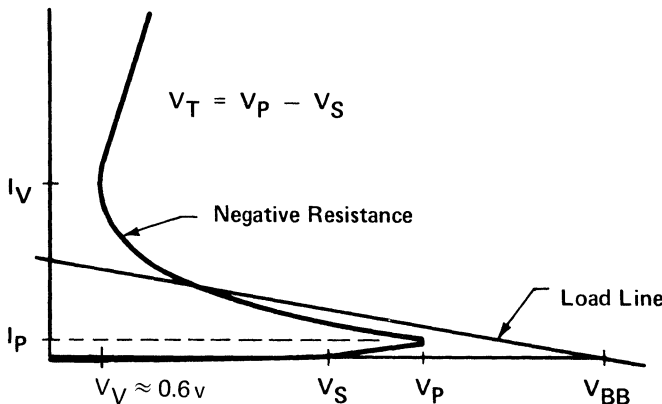


Figure 5. Offset Voltage

CONDITIONS FOR ONE SHOT OPERATION

$$\frac{V_{BB} - V_P}{R_T} > I_P (\text{max}) \quad \frac{V_{BB} - V_V}{R_T} > I_V$$

must be satisfied. Since the load current is in the positive resistance region, the PUT will LATCH on and remain on.

PUT OFFSET COMPENSATION

In order to compensate for offset voltage (V_T) temperature shift, a diode D_1 forward biased through R_D may be used Fig. 6. The value of R_D is selected by:

$$R_D = \frac{V_{BB}}{I_P (\text{max})}$$

A diode having a forward voltage temperature characteristic similar to the offset voltage temperature coefficient (TC) would provide optimum compensation.

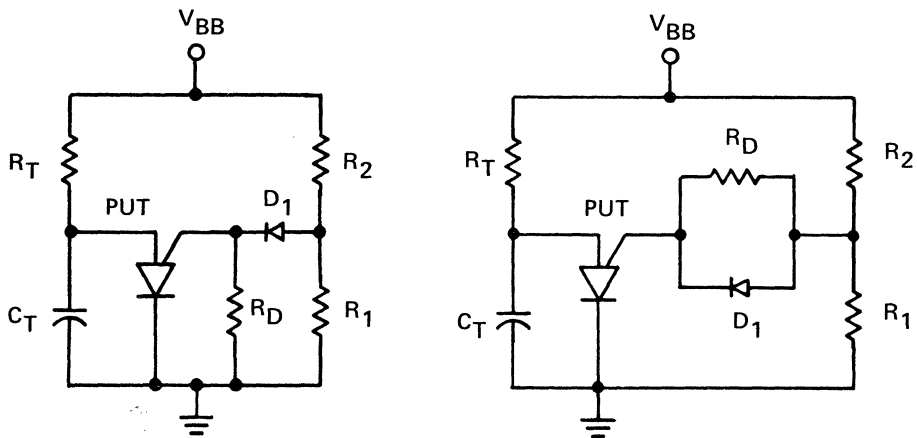


Figure 6. Offset Compensation Methods

TUNABLE FREQUENCY OSCILLATORS

Variable oscillator circuits which include active elements for discharging the timing capacitor C_T are shown in Fig. 7. A second method is given as in Fig. 8.

FREQUENCY RANGE
40 Hz to 65 kHz

OUTPUT PULSE
Rise time ~ 200 nsec.
Pulse width ~ 10 μ sec.
Recovery time < 200 nsec.

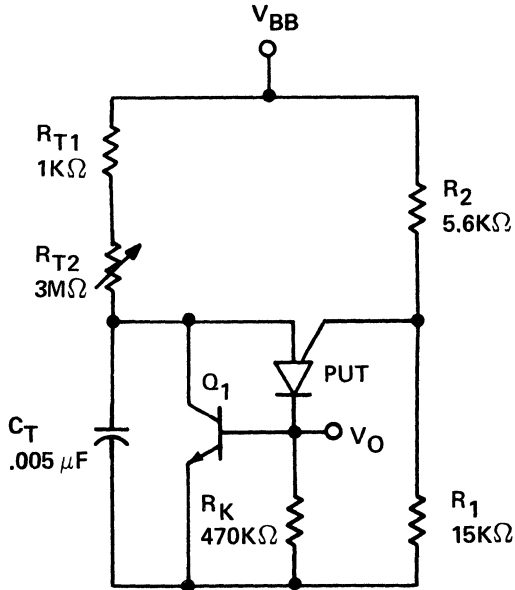


Fig. 7

FREQUENCY RANGE
40 Hz to 40 kHz

OUTPUT PULSE
Width ~ 5 μ sec.

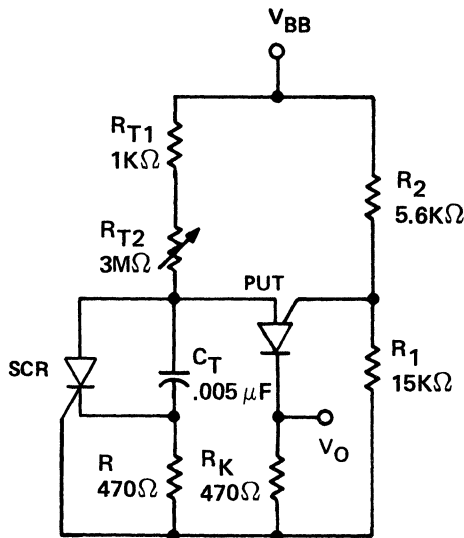


Fig. 8

DESIGN EXAMPLE

A relaxation oscillator. A trigger generator is needed to provide a pulse of energy.

The required repetition rate is 1000 pulses per second. A power source of 20 Vdc is available.

- Step 1 Select the value of R_1 and R_2 based on I_p , I_V requirements. For $R_G = 10K\Omega$, (Fig. 3) $R_1 \sim 27K\Omega$, $R_2 \sim 16K\Omega$ this will give an η of ~ 0.63 . (Equations 7 and 4).
- Step 2 From Fig. 9 with T given as 0.001 sec and η of 0.63. $R_t C_t = 0.001$, $T/R_t C_t = 1$ @ $\eta = 0.63$.
- Step 3 The condition for sustained oscillation must be satisfied (equations 8 and 9) hence, $275K < R_t < 1.4$ meg (using spec values for a 2N6027).
- Step 4 The value of capacitance is chosen by considering the rise time and energy required. Since $R_t C_t = 0.001$ the C_t range is $0.0007 < C_t < 0.0036\mu fd$. Choose a standard value of capacitance and resistance. For example, $C_t = 0.002\mu fd$ and $R_t = 470K\Omega$ (Standard Value).

For this example $R_t = 470K\Omega$, $C_t = 0.002\mu fd$. A cathode resistance of 20Ω will provide a pulse of current of 130 ma with a pulse width of 300 nsec.

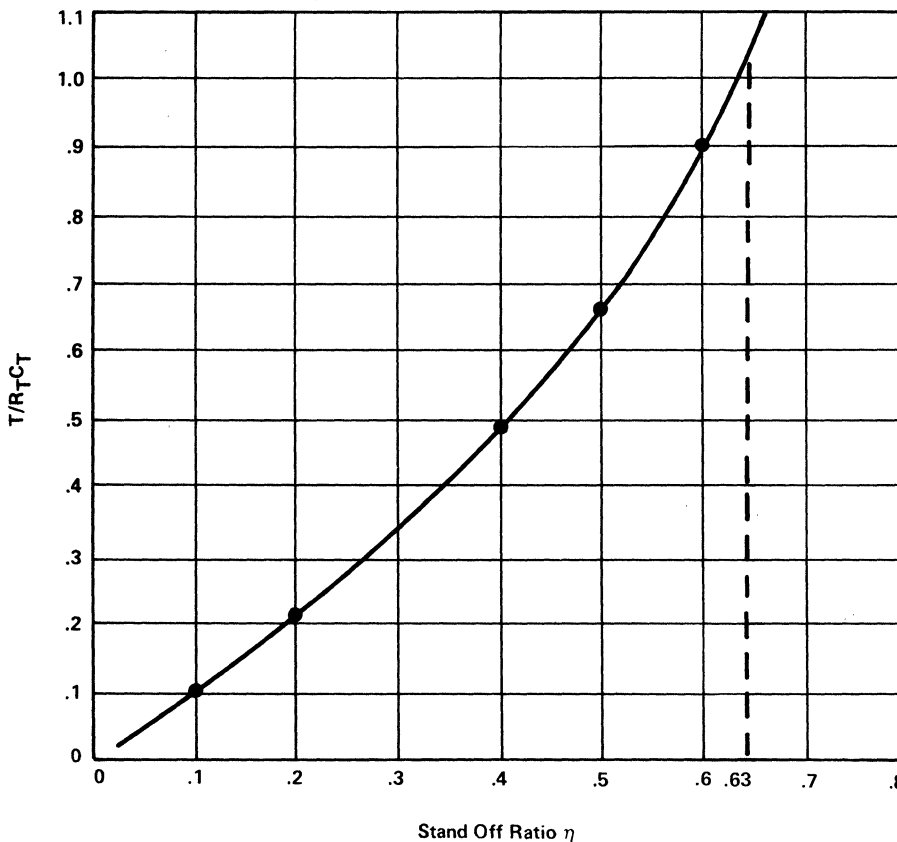


Fig. 9

SWITCHING REGULATOR DESIGN GUIDE

I. The Advantages of the Switching Regulator

Unlike conventional "dissipative" series or shunt regulators, in which the power-regulating transistor operates in a continuous-conduction mode, dissipating large amounts of power at high load currents – especially when the input-output voltage difference is large – the switching regulator has high efficiency under all input and output conditions. Furthermore, since the power-transistor "switch" is always either cut off or saturated (except for a very brief transition between those two states), the switching regulator can achieve good regulation despite large changes in input voltage, and maintains high efficiency over wide ranges in load current.

Because the switching regulator regulates by varying the ON-OFF duty cycle of the power-transistor switch, and the switching frequency can be made very much higher than the line frequency, the filtering elements used in the power supply can be made small, lightweight, low in cost, and very efficient – i.e., with almost negligible power losses. It is possible to drive the switching regulator with very poorly filtered DC (in fact, in high-power applications, three-phase rectification *without* filtering of any kind is often used to develop the input DC from the power line), thereby eliminating large and expensive line-frequency filtering elements.

Finally, it is possible to design switching regulators with excellent load-transient properties, so that step increases of load current cause relatively small instantaneous changes in output voltage, recovery from which is essentially completed in a few hundred microseconds.

The switching regulator has become increasingly popular in new-equipment designs, not only in aerospace and defense applications, but in computers,

industrial process control systems, instrumentation, and communication.

Compared to the dissipative regulator, the switching regulator does have some disadvantages which preclude its use in some applications. The primary power source delivers current to the switching regulator in pulses which, for efficiency reasons, have short rise and fall times. In those applications where a significant series impedance appears between the supply and the regulator, the rapid changes in current can generate considerable noise. This problem can be reduced by reducing the series impedance, increasing the switching time, or by filtering the input to the regulator.

A second problem of the switching regulator, compared to the dissipative regulator, is its response time to rapid changes in load current. The switching regulator will reach a new equilibrium only when the average inductor current reaches its new steady-state value. In order to make this time short, it is advantageous to use low inductor values, or else to use a large difference between the input and output voltage.

Improved circuits for controlling switching regulators have been developed at Unitrode, thereby eliminating some earlier design constraints and optimizing the performance attainable with available hardware. These new circuits permit taking full advantage of the economy and efficiency of the Unitrode PIC600 Series Hybrid Power Switch.

The design approach used herein is believed to be original, and to be clearly superior to earlier methods of calculating the key parameters and designing the power inductor . . . yielding explicit, accurate results in significantly less time than the approximate equations in common use.

II. The Switching Regulator Described and Characterized

The basic configuration of a switching regulator is shown in Figure 1. It accepts a DC voltage input, E_{in} , and regulates a DC output voltage, E_o , despite variations in E_{in} and load current. Although the static regulation, dynamic regulation, and ripple rejection of this type of regulator cannot be as easily optimized as they can in a continuous (so-called "dissipative") series regulator, its efficiency, power density (Watts output per cubic inch) and economy are all markedly superior to the series regulator . . . particularly for low-voltage, high-current supplies. Unlike a series regulator, it maintains high efficiency with high input voltages. Switching regulators can thus be employed with high efficiency to derive low voltage outputs from a high voltage unregulated supply.

All of these advantages derive from the method of regulating the output voltage: *by varying the duty cycle of a power-transistor switch*, rather than varying the voltage drop across a power transistor operating in the linear mode. Because the switch (Q1 in Figure 1) is always in the saturated state when it is conducting, and is otherwise completely non-conducting (except for a brief commutation time between the ON and OFF states), the power dissipated in the regulator is much lower than it would be in a series regulator for the same input and output conditions.

The basic switching regulator circuit functions as follows:

The control circuit causes transistor switch, Q1, to switch on and off at a predetermined frequency, f . During the time that Q1 is on, t_{on} , the input voltage, E_{in} , is applied to the input of the LC filter, causing current i_1 to increase. When Q1 is off, the energy stored in the inductor, L, maintains current flow to the

load, circulating through "catch" diode D1. The input of the LC filter is now at zero Volts, i_1 decreases to its original value and the cycle repeats.

The output voltage, E_o , will equal the time average of the voltage at the input of the LC filter:

$$E_o = E_{in} t_{on}/\tau$$

where: $\tau = 1/f$

The control circuit senses and regulates E_o by controlling the duty cycle, $\alpha = t_{on}/\tau$. If E_{in} increases, the control circuit will cause a corresponding reduction in the duty cycle, α , so as to maintain a constant E_o .

$$E_o = \alpha E_{in}$$

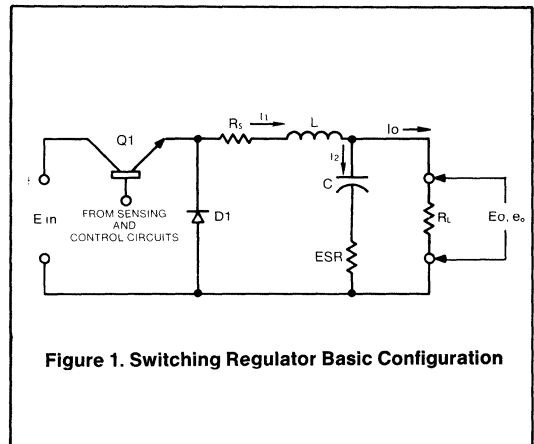
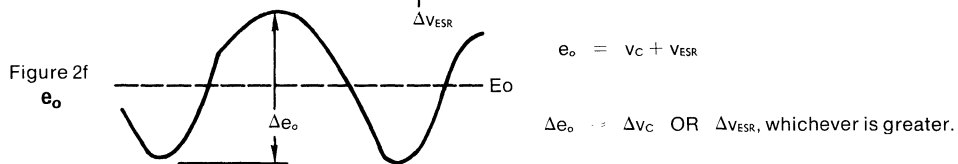
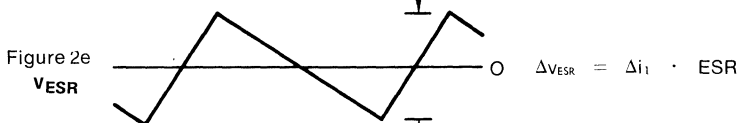
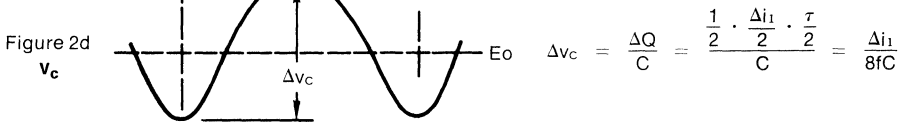
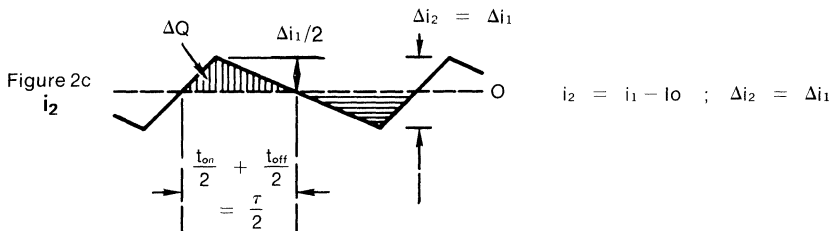
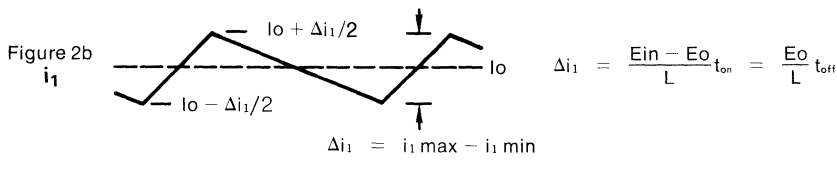
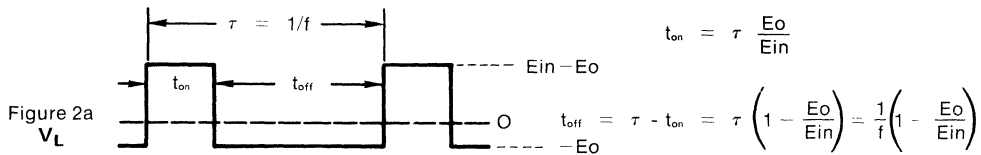


Figure 1. Switching Regulator Basic Configuration



NOTE: See Appendix A for rigorous analysis and justification

Figure 2. Switching Regulator Waveforms

Figure 2 shows some of the important waveforms and equations which define the operation of the switching regulator power circuit. The following discussion is based on several simplifying assumptions which are explained and justified or corrected in Appendix A. The most significant assumptions are to neglect the saturation voltage of Q1, the forward drop of D1, and the series loss resistance, R_s , of the inductor, L.

Figure 2a shows the voltage across inductor, L, which equals $(E_{in} - E_o)$ during t_{on} and $(-E_o)$ during t_{off} . Under equilibrium conditions, when output load current, I_o , is constant, the average voltage across L must, by definition, equal zero.

Figure 2b shows the current i_1 through the inductor. Under equilibrium output current conditions, the increase in current during t_{on} , Δi_1 , must equal the decrease in current during t_{off} . The average value of i_1 equals the output current, I_o .

Figure 2c shows current i_2 through the capacitor, which is equal to $(i_1 - I_o)$. The average value of $i_2 = 0$, and $\Delta i_2 = \Delta i_1$. Current i_2 causes a ripple voltage to appear at the output. The output ripple voltage, e_o , has two components, a capacitive component, v_C , and a resistive component, v_{ESR} , caused by the equivalent series resistance of the capacitor.

Figure 2d shows the capacitive component, v_C , of the ripple voltage, which is the time integral of the capacitor current, i_2 . Note that v_C is the integral of a triangular wave, and is not sinusoidal. Also note that v_C is in "quadrature" with i_2 , in the sense that v_C min and v_C max occur at times A and B, midway in the t_{on} and t_{off} intervals, when i_2 is zero. The total charge, ΔQ flowing into C is computed graphically by finding the area of the triangular current waveform between time A and time B (Area = $\frac{1}{2} bh$; $\Delta Q = \frac{1}{2} \times \tau/2 \times \Delta i_2/2$). The

peak to peak capacitive ripple component $\Delta v_C = \Delta Q/C = \Delta i_1/8fC$. (The factor $8f$ for a triangular current waveform is comparable to $2\pi f$ for a sinusoidal input current.)

Figure 2e shows the resistive component, v_{ESR} , of the ripple voltage which simply equals $i_2 \times ESR$, and is in phase with i_2 .

Figure 2f, the total output ripple voltage, e_o , is the sum of the waveforms in Figures 2d and 2e. Note that since v_C and v_{ESR} are in quadrature, the greater of these two components dominates, and for all practical purposes the peak to peak output ripple voltage, Δe_o , is equal to either Δv_C or Δv_{ESR} whichever is greater.

The magnitude of v_{ESR} in comparison with v_C shown in these waveforms is not exaggerated. Indeed, when designing a switching regulator to operate at frequencies greater than 20 kHz in order to achieve small size and low cost in the L and C filter elements, the ESR of the capacitor usually dominates completely. Even when high quality capacitors (low ESR) are employed, it is usually necessary to use a larger capacitance value than would otherwise be required in order to realize the ESR required to achieve the ripple objective of the design.

With conventional free running switching regulator control circuits, capacitor ESR also causes very significant departure from the design frequency, which can result in large ripple magnitude, inductor saturation, and switching transistor failure. In the circuits developed at Unitrode and presented in the next section, the frequency-variation effect caused by ESR is effectively eliminated, leaving only the ripple consideration.

Detailed design considerations for switching regulator power circuits are contained in Section IV.

III. Applications Circuits for Switching Regulators

The design and performance of conventional switching regulators are usually dominated by the ESR of the output capacitor. However, in the group of circuits described in this section, the following parametric relationships and circuit characteristics are easily and economically attained:

- The switching frequency may be selected and established at the optimum value for the switching components, and *will be independent of the value of the ESR of the output capacitor.*
- The value of t_{off} is held relatively constant, over wide ranges of load current and input voltage, and independent of the ESR of the output capacitor. Constant t_{off} results in constant ripple current and output ripple voltage.
- Settable overcurrent limiting is provided, thereby protecting both the load and the switching transistors under all conditions, and preventing saturation of the power inductor during the startup transient period, thereby minimizing startup overshoot.
- The overcurrent limiting circuit is significantly lower in dissipation than conventional current-limit-feedback arrangements.
- The drive current to the power output (switch) stage is regulated to a pre-determined value, for best efficiency and optimum switching speed. Drive current is automatically increased at low temperatures and decreased at high temperatures, thereby maintaining optimum drive conditions for the power switch.

Note that, although the use of this circuit approach permits essentially constant " t_{off} " operation even with capacitors having relatively high ESR, the output ripple voltage is increased by high ESR. (If the ripple developed across ESR is significantly larger than that developed across C, then the ripple is essentially proportional to ESR.)

Not all of the circuits that follow have all of the virtues listed above, but the exceptions will be noted. Figure

3 typifies this family of regulators. It is shown implemented by the popular LM305 regulator IC, and a Unitrode Series PIC600 Hybrid Power Switch, comprising a quasi-Darlington switching transistor, a fast recovery catch diode, and transistor bias resistors, all matched for optimum efficiency and switching speed (up to 100 kHz without derating). The configuration of Figure 3 is a *positive* output regulator, with performance characteristics as follows:

$$E_{in} = 20 \text{ to } 40\text{V}$$

$$E_o = 5\text{V} \pm 1\%$$

$$\Delta e_o = 100 \text{ mV p-p (2\% p-p ripple)}$$

$$I_o = 2 \text{ to } 10\text{A}$$

$$I_{sc} = 12\text{A}$$

$$\text{Regulation versus } E_{in} (20 \text{ to } 40\text{V}) < 25 \text{ mV}$$

Transient Recovery Time for step change in load current from 2A to 10A, or 10A to 2A < 150 μsec .

$$f = 50 \text{ kHz nominal}$$

$$\text{Efficiency} > 70\%$$

The circuit of Figure 3 operates in the fixed-off-time mode; hence, output ripple is independent of input voltage over wide ranges. In this circuit, two feedback signal paths are provided:

- *DC Feedback.* A fraction of the DC output voltage, E_o , is fed back to the inverting input of the LM305 through voltage divider R1, R2. The DC voltage at the inverting input is compared to a reference voltage (approximately 1.8V) within the LM305, and the LM305 regulates E_o so that the voltage fed back to the inverting input is essentially equal to the built in reference voltage. The R1, R2 divider ratio therefore establishes the level of the DC output voltage, E_o . Resistor R5 improves output voltage regulation versus input voltage changes by feeding a small compensating voltage proportional to the input voltage into the inverting input of the LM305.

- **AC Feedback.** Capacitor C1 feeds back an AC voltage waveform to the inverting input of the LM305. This voltage is proportional to the output ripple voltage plus the AC voltage developed across R_1 , $\Delta e_o + \Delta v_{R_1}$.

Capacitor C2 feeds back an AC voltage to the non-inverting input of the LM305. This voltage is proportional to the output ripple voltage plus the AC voltage across R_3 , $\Delta e_o + v_{R_3}$.

When the circuit values are properly established, the same fraction of Δe_o is fed back to both inverting and non-inverting inputs, thereby effectively cancelling. The operation of the switching regulator is thus rendered independent of the output ripple voltage developed across the C or ESR of the output capacitor.

Since the Δe_o components cancel each other, the LM305 essentially compares Δv_{R_1} at the inverting input to Δv_{R_3} at the non-inverting input. Voltage Δv_{R_3} is a rectangular waveform with a peak-to-peak amplitude equal to $I_{\text{drive}} \times R_3$, where I_{drive} is the base drive to the hybrid switching transistor provided by the LM305, and Δv_{R_1} is a triangular waveform with a peak-to-peak amplitude equal to $\Delta i_1 \times R_1$, where Δi_1 is the ripple current through inductor L. When the drive current is on, Δv_{R_3} is at its peak positive amplitude. As i_1 increases, v_{R_1} increases proportionately. When the positive amplitude of Δv_{R_1} reaches Δv_{R_3} , this causes the LM305 to switch off the drive current, Δv_{R_3} immediately drops to its peak negative amplitude, and i_1 starts to fall. When Δv_{R_1} reaches a negative amplitude equal to Δv_{R_3} , the LM305 switches the drive current back on, and the process repeats. In this manner, the LM305 controls the power switch so that Δi_1 is fixed. Since $t_{\text{off}} = \Delta i_1 \times L / E_o$, with fixed values of L and E_o , t_{off} is fixed and independent of changes in E_{in} or capacitor C or ESR values.

R_4 , connected between pins 1 and 8 of the LM305, establishes the desired level of base drive for the PIC600 Series Hybrid Power Switch, and determines the hysteresis voltage across R_3 .

Current-limiting action is provided by transistor Q1, the collector of which is connected to the "gate" or "inhibit" terminal of the LM305 (pin 7). When the load current is normal, Q1 is cut off and pin 7 floats; but when the voltage drop across R_1 increases to a value greater than the sum of V_{BE} (Q1) and v_{R_3} , Q1 turns on, cutting off the drive current from the LM305 and, ultimately, the power switch. This cutoff action is made to "latch" by the fact that, with the drive cut off, v_{R_3} disappears. This keeps Q1 on, until the current through R_1 drops significantly – enough to make the voltage drop across R_1 fall below the V_{BE} of Q1.

The current through R_1 , following such an overload cutoff action, falls linearly at the rate of E_o/L . When Q1 is cut off, drive current is restored. The circuit will then continue to switch on and off at a frequency comparable to normal operation, with the average current limited at the design limit, and power dissipation held to safe values.

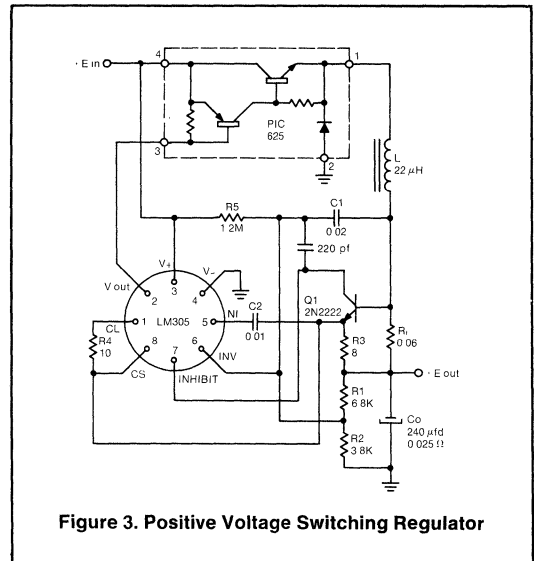
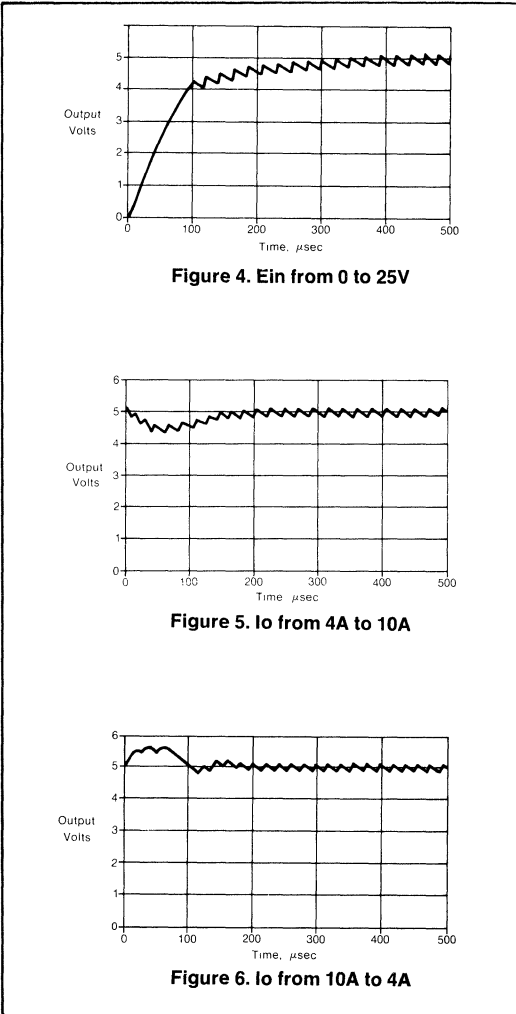


Figure 3. Positive Voltage Switching Regulator

Transient response of the switching regulator of Figure 3 is shown in Figures 4, 5, and 6.



It is usually necessary to employ a noise filtering capacitor across the input of any switching regulator. This functions to prevent the steep waveform of the

rectangular current pulse associated with the power switch turning on and off from propagating into the Ein supply line. The capacitance value required is a function of the impedance characteristics of the Ein supply and intervening wiring. Watch out for underdamped resonance with the inductance of the input wiring, or transient induced ringing may occur. The input capacitor must have short leads, and the ground side should preferably be connected directly to the ground side of the output filter capacitor.

A 10A negative voltage switching regulator, utilizing an LM304 and PIC600 series, is shown in Figure 7.

A reference voltage is determined by resistor R1 and R2. The error amplifier controls the output voltage at twice the voltage across R2. Diode D1 is used to ensure a potential difference of less than 2V at the unregulated input (pin 5) with respect to the reference supply (pin 3). (If the unregulated supply terminal gets more than 2V positive with respect to reference supply, the collector isolation junction of transistor Q6 of LM304 becomes forward biased and disrupts the reference.)

Current limiting is achieved, in Figure 7, by means of reducing the reference voltage to ground with the help of transistor Q1 and resistor R8, instead of turning off the base drive to the power output switch as in Figure 3.

The functions of the rest of the components and the operation of the switching regulator are the same as described for Figure 3.

A positive switching regulator using a μ A723 is shown in Figure 8.

The basic performance and circuit operation is the same as Figure 3.

The circuit shown in Figure 9 is a high voltage positive switching regulator. Because the LM305 (like almost all IC regulators) cannot be operated at supply voltage in excess of 40V, this circuit uses a fraction of Ein as a power supply for the IC circuit by means of zener diode and current limiting resistor R9. The voltage isolation between LM305 and power switch, and the regulated base drive to the power switch are provided by transistor Q2.

APPLICATION NOTE

The basic operation of the circuit and design approach is the same as that of a low voltage positive switching regulator.

The circuit shown in Figure 10 is a negative high voltage switching regulator.

This circuit is similar to the low voltage negative switching regulator with a minor modification. Transistor Q2, resistor R10 and R11 are all used to provide regulated base drive to the power output stage and also to provide the voltage isolation between power output stage and LM305. The resistor R9 is used to limit current through zener diode under steady state and startup conditions.

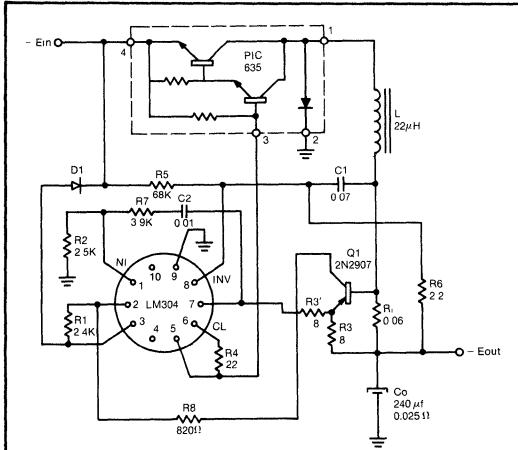


Figure 7. Negative Voltage Switching Regulator

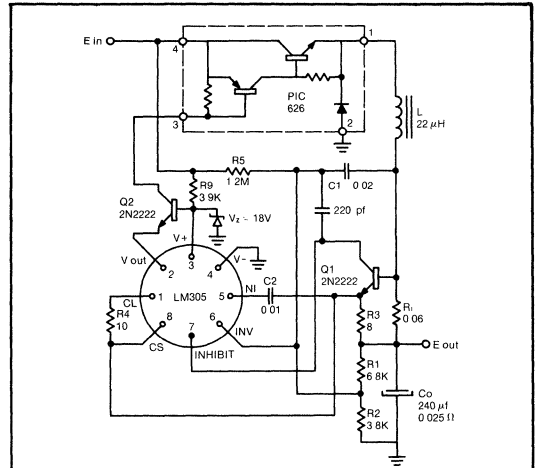


Figure 9. High Voltage Positive Switching Regulator

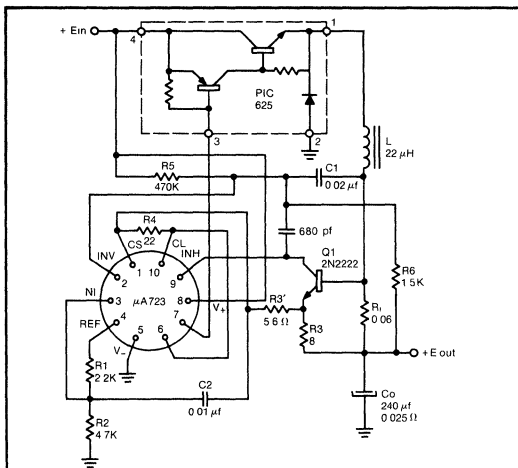


Figure 8. Positive Voltage Switching Regulator

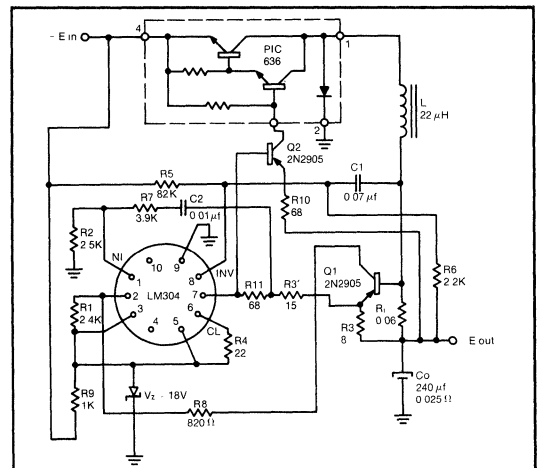


Figure 10. High Voltage Negative Switching Regulator

IV. Designing the Power Circuit

In designing a switching regulator power supply, the following parameters will normally be predefined. Specific values shown for each parameter will be used as the basis for a design example:

E_o	=	5V Output Voltage
Δe_o	=	100 mV Output Ripple Voltage, Peak to Peak
$I_o \text{ max}$	=	10A Output Current, Full Load
$I_o \text{ min}$	=	2A Output Current, Minimum Load
$E_{in \text{ max}}$	=	40V Input Voltage, Maximum
$E_{in \text{ min}}$	=	20V Input Voltage, Minimum

The first step in the design is to decide on the operating frequency of the switching regulator. No concrete rules can be given for this decision.

High frequency operation is distinctly advantageous in that the cost, weight and volume of both L and C filter elements are reduced. However, above the frequency where the capacitor ESR exceeds its capacitive reactance, no further reduction in capacitor size or cost will occur. This frequency, in the range of 1-50 kHz, depends upon the "quality" of the capacitor in terms of ESR. Above this frequency, the inductor will continue to diminish in size and cost, although when the inductor reaches a very small size, cost will level off.

Operation above 20 kHz is desirable to eliminate the possibility of audio noise.

The main factor limiting high frequency operation is the drop in efficiency caused by switching losses in the power switching transistor and "catch" diode. The higher cost of these fast switching semiconductors required to operate efficiently at high frequencies must be weighed against the reduced cost, size and weight of the L and C components to arrive at the optimum frequency for any specific application. It may be desirable to work the design through at several frequencies in order to make a decision.

In the specific application defined at the beginning of this section, the power output ($E_o \times I_o \text{ max}$) is 50W.

Referring to the specification for the Unitrode PIC 625/635 Hybrid Power Switch, the DC losses (Transistor V_{CEsat} , Diode V_F) under the conditions of this application amount to 10W. The following tabulation shows the switching losses and overall efficiency at several frequencies.

Frequency	1 kHz	20 kHz	50 kHz	100 kHz
Power output	50	50	50	50
DC losses	10	10	10	10
Switching losses	0.05	1	2.5	5
Total power input	60.05	61	62.5	65
Realizable efficiency	83.3%	82%	80%	77%

For our example, we will choose a frequency of 50 kHz, even though the efficiency is not significantly reduced at 100 kHz. At 100 kHz most currently available tantalum and aluminum electrolytic capacitors begin to exhibit series inductance.

Transistors and diodes which do not have the fast switching capabilities of the PIC 625/635 will become efficiency limited at much lower frequencies. Note that in this specific application, a dissipative regulator design will incur power losses in the series transistor of 350W, resulting in an efficiency of 12.5 percent!

The control circuits shown in the previous section control the on-off switching periods by sensing and controlling the ripple current, ΔI_L , through the inductor L. This mode of operation results in a constant ripple current and (assuming E_o and L are fixed) constant off time, t_{off} , independent of input voltage. The relationship between t_{off} , f, E_o , and E_{in} is as follows (from Figure 2a):

$$t_{off} = (1 - E_o/E_{in}) / f$$

With t_{off} and E_o fixed by the control circuit, f will change when E_{in} changes, and f will be maximum when E_{in} is maximum. In our specific example,

$$\begin{aligned} f \text{ max} &= 50 \text{ kHz} \\ E_{in \text{ max}} &= 40 \text{ V} \\ E_o &= 5 \text{ V} \end{aligned}$$

so that:

$$t_{off} = (1 - 5/40) / 50,000 = 17.5 \mu\text{sec}$$

Now, with t_{off} fixed at 17.5 μsec , if E_{in} changes to $E_{in\ min} = 20V$,

$$f_{min} = \frac{(1 - E_o/E_{in})}{t_{off}} = \frac{(1 - 5/20)}{17.5 \times 10^{-6}} = 43 \text{ kHz}$$

The fact that the frequency changes slightly with E_{in} is really not important, as stated earlier, because constant t_{off} operation results in more constant output ripple than constant frequency operation.

Having determined (or assumed) the maximum operating frequency and calculated t_{off} , we next proceed to find specific values for L and C. L and C together form a low pass filter which reduces the rectangular waveform at the filter input to a DC output voltage, E_o , with a small amount of ripple, Δe_o , superimposed. To achieve a specified Δe_o requires a specific LC product, independent of load current. Theoretically, this LC product can be achieved with any L/C ratio – small L and large C, or large L and small C (or very large L and no C at all, using instead the load resistance R_L as one element of an L/R filter). There are, however, several practical economic and performance considerations that apply to selecting specific L and C values.

It is favorable to push in the direction of small L and large C for the following reasons:

1. Under the power and frequency ranges commonly encountered in switching regulator circuits, it costs more to store energy in an inductor than in a capacitor. Also, an inductor will have considerably greater weight and volume than a capacitor with equal energy storage capacity. Small L and large C, within the limits defined below, will usually result in the lowest cost, weight and size design.
2. Small L and large C results in low "surge impedance" of the filter, hence better transient behavior with step changes in load current.

3. Losses in a practical inductor are higher than in a capacitor with equal energy storage capacity (assuming low ESR). This again argues for small L, large C.

One major objection to a low L/C ratio is that it causes large and sometimes intolerable overshoot in input current and output voltage on startup, when the circuit is first energized. Input current overshoot can saturate the inductor and destroy the switching transistor. The current limiting feature of the applications circuits shown in Section III effectively controls the startup transient, thereby protecting all components and minimizing voltage overshoot. With current limiting, this problem is eliminated and no longer pertains to the selection of L and C values.

Referring to Figure 2b and its associated equations, the peak-to-peak ripple current through the inductor, Δi_L , is inversely proportional to the inductance, L. As L is made smaller, Δi_L increases. Maximum limits on Δi_L determine how small L is permitted to be, as follows:

1. The instantaneous current through L ranges between a maximum of $I_o + \Delta i_L/2$ and a minimum of $I_o - \Delta i_L/2$. If $\Delta i_L/2$ is permitted to become larger than I_o , the minimum inductor current becomes a negative value. This is impossible, since neither the switching transistor nor the "catch" diode will conduct. Therefore, the switching regulator goes into a discontinuous mode of operation which is perfectly safe, but the frequency changes considerably and regulation with output current changes becomes relatively poor. The worst case consideration to insure that discontinuous operation does not occur is to make $\Delta i_L/2$ equal to the *minimum* load output current, $I_{o\ min}$, or $\Delta i_L = 2 I_{o\ min}$.

It is not practical to apply this criterion if $I_{o\ min}$ is very small ($<0.05 I_{o\ max}$) because Δi_L would then be very small, forcing an impractically large L value. In applications

where $I_{o \text{ min}}$ is very small, there are two alternatives: (a) raise $I_{o \text{ min}}$ by preloading the supply, or (b) make $\Delta I_1 = 2(0.05 I_{o \text{ max}}) = 0.1 I_{o \text{ max}}$ realizing that when I_o becomes less than $0.05 I_{o \text{ max}}$, the discontinuous mode will occur.

- The maximum peak current is equal to the full load current, $I_{o \text{ max}} + \Delta I_1/2$. As L is decreased, the corresponding increase in ΔI_1 will begin to cause a significant increase in the maximum peak current. Since the inductor must be designed not to saturate at the maximum peak current, this begins to negate the cost, size and weight advantages of making the L value smaller. Higher peak currents will have an adverse effect on efficiency and transistor drive requirements, and may require transistor and "catch" diodes with higher current ratings (and higher cost). It is, therefore, recommended that $\Delta I_1/2$ be no greater than $0.25 I_{o \text{ max}}$, which will limit the maximum peak current to $1.25 I_{o \text{ max}}$, or $\Delta I_1 \text{ max} = 0.5 I_{o \text{ max}}$.

In summary:

$\Delta I_1 = 2 I_{o \text{ min}}$, within the following somewhat arbitrary limits:

$$\Delta I_1 \text{ min} = 0.1 I_{o \text{ max}}$$

$$\Delta I_1 \text{ max} = 0.5 I_{o \text{ max}}$$

In our example, $I_{o \text{ min}} = 2\text{A}$, $I_{o \text{ max}} = 10\text{A}$. Calculating $\Delta I_1 = 2 I_{o \text{ min}} = 4\text{A}$, which is acceptable since $\Delta I_1 \text{ max} = 0.5 \times 10\text{A} = 5\text{A}$, and $\Delta I_1 \text{ min} = 0.1 \times 10\text{A} = 1\text{A}$.

Now that t_{off} and ΔI_1 have been determined, L can be calculated as follows:

$$L = \frac{E_o \times t_{\text{off}}}{\Delta I_1} = \frac{5 \times 17.5 \times 10^{-6}}{4} = 21.9 \mu\text{H}$$

The final step is to determine the requirements for the capacitor C and ESR values which will result in the desired output ripple voltage, Δe_o . Since the two components of Δe_o : Δv_C and Δv_{ESR} , are in "quadrature", we can consider each component separately, with a worst case error of less than 20 percent when both components are equal. This much error is highly unlikely, since the ESR component usually dominates completely when operating at high frequencies.

From Figure 2d:

$$C = \frac{\Delta I_1}{8f \Delta v_C}$$

note that C varies inversely with f . In order to achieve Δv_C less than the desired maximum Δe_o , the minimum value for C must be determined at the lowest frequency, f_{min} , calculated previously.

$$\begin{aligned} C \text{ min} &= \frac{\Delta I_1}{8f_{\text{min}} \Delta e_o \text{ max}} \\ &= \frac{4}{8 \times 43 \times 10^3 \times 100 \times 10^{-3}} \\ &= 114 \mu\text{F} \end{aligned}$$

From Figure 2e:

$$\begin{aligned} \text{ESR max} &= \frac{\Delta v_{\text{ESR}}}{\Delta I_1} = \frac{\Delta e_o \text{ max}}{\Delta I_1} \\ &= \frac{100 \times 10^{-3}}{4} \\ &= 0.025 \Omega \end{aligned}$$

With high frequency operation, capacitor ESR usually dominates, forcing the use of a C value much greater than $C \text{ min}$ in order not to exceed ESR max .

Subsequent sections deal with designing the inductor and selecting the capacitor and other components of the switching regulator.

V. Design of the Power Inductor

This simplified nomographic method facilitates selecting the smallest core that will achieve the desired characteristics of the power inductor. This procedure is useful in selecting the proper core and determining wire size, number of turns, copper losses, and temperature rise. It also permits investigating the effects of change in assumed initial conditions and in "trimming" the design.

A detailed analysis of this inductor design procedure is contained in Appendix B.

Tables 1 and 2 give core parameters for a variety of commonly used ferrite pot cores and Mo-Permalloy toroids. (Note: There is no significance to the selection of manufacturers, nor is any intended. Many manufacturers make roughly equivalent cores in these sizes, with similar magnetic properties.)

Ferrite and Mo-Permalloy powder are excellent core materials for the switching regulator inductor. Since the rms AC current through the inductor is small compared to the DC current, AC losses in the winding and core losses will be negligible compared with DC winding losses.

Selection of the proper core for a specific application is a process concerned with two factors: (1) The core must provide the desired inductance without saturating magnetically at the maximum peak overload current, i_1 max. In this respect each core has a specific $(LI^2)_{sat}$ energy storage capability. (2) The core must have a window area for the winding which admits the number of turns necessary to obtain the required inductance with a wire size which will result in acceptable DC losses in the winding at the full load output current, I_o . Each core has a specific $(LI^2)_{diss}$ capability that will result in a specific power loss or temperature rise.

The significant core parameters are primarily core size and the magnetic gap in series with the flux path. Consider a very small (for the application) ferrite pot core with no air gap. The effective permeability, μ_{eff} , will be very large because there is no gap. Relatively few turns will be required to achieve the desired inductance, and the power loss at I_o will be small, but the core cannot store the required energy $L(i_1 \text{ max})^2$ without saturating. If we introduce a gap into this core, the energy storage capability increases (the extra energy is actually stored in the gap, not in the ferrite material). However, the gap causes the effective permeability to drop, which requires more turns of finer wire to achieve the desired inductance. If the core is

too small, as the gap is increased to the point required to achieve the necessary energy storage capability without saturating, the DC resistance of the increased number of turns of finer wire has increased to the point where the power dissipation and temperature rise is too great. This conflict is resolved by going to a larger core with appropriate gap.

To facilitate core selection, Tables 1 and 2 contain tabulated values of $(LI^2)_{sat}$ energy storage capability (saturation limited) and $(LI^2)_{25C}$ capability (based on power dissipation resulting in 25°C temperature rise). These values have been calculated for various size cores with different gaps, by methods described in Appendix B. Also given in the tables are the power dissipation corresponding to a 25°C rise for each core size, and the effective window area for the winding, A_w' . Tabulated A_L values relate to different gaps. (A_L is the inductance index at a particular gap setting – defined as the inductance in mH for 1000 turns.)

The optimum cores for switching regulator inductor applications generally have quite large gaps, and consequent relatively low A_L values. This is fortuitous, since the core properties are then dependent mostly on the gap itself, and variations in the magnetic materials of the core are swamped out, resulting in excellent stability and linearity. Note, however, that in the ferrite pot core table, many of the lower A_L values are not supplied as stock items by the manufacturer, and the desired gap must be ground to size on a special order basis.

Mo-Permalloy powder cores are effectively "gapped" by the manufacturer by means of varying the amount of non-magnetic binder that holds the Mo-Permalloy particles together within the core, and by the size and shape of the Mo-Permalloy particles. Thus, the "gap" is actually distributed throughout the core material. These cores are supplied with many different A_L values in each size.

One of the main advantages of ferrite pot cores and ferrite E-I cores (not tabulated, but worth considering) is that the winding is easily formed on a bobbin which is subsequently assembled within the two-piece core assembly. Ferrite toroids are not recommended because of the practical difficulty of introducing a gap. Mo-Permalloy toroids are not as convenient to wind, but this is not a serious problem as most switching regulator inductor designs require few turns of relatively heavy wire.

Example of Inductor Design

The example shown below will illustrate the method of solution, as drawn on the nomograph of Figure 11.

Given:

$$\begin{aligned} L &= 21.9 \mu\text{H} \\ I_o &= 10\text{A} \\ I_1 \text{ max} &= 14\text{A (current limited)} \\ E_o \times I_o &= 50\text{W (output of regulator)} \end{aligned}$$

Copper losses not to exceed 1% of output power, and temperature rise of inductor not to exceed 25°C.

Step 1: Draw line ① from $I_o = 10\text{A}$ on the "I" scale, to 0.0219 mH (21.9 μH) on the "L" scale through the " LI^2 " scale. Note that $LI_o^2 = 2.19$ millijoules.

Step 2: Draw line ② from $I_1 \text{ max} = 14\text{A}$ on the "I" scale to the 0.0219 mH on the "L" scale through the " LI^2 " scale. Note that $L(I_1 \text{ max})^2 = 4.3$ millijoules.

Step 3: Find the smallest core in Tables 1 or 2 that has $(LI^2)_{25C}$ capability greater than LI_o^2 defined in step 1, and $(LI^2)_{\text{sat}}$ capability greater than $L(I_1 \text{ max})^2$ defined in step 2. This appears to be a 2616-3B7 pot core with $A_L = 160$ from Table 1, or an A-291061-2 toroid from Table 2.

Step 4: Actual temperature rise of the core and power loss can be calculated as follows:

Temperature rise of pot core;

$$\begin{aligned} \text{Actual } \Delta T &= 25^\circ\text{C} \frac{LI_o^2 \text{ (step 1)}}{(LI^2)_{25C} \text{ from core table}} \\ &= 25^\circ\text{C} \times \frac{2.19}{2.288} \\ &= 24^\circ\text{C} \end{aligned}$$

Power loss in inductor;

$$\begin{aligned} \text{Actual } P_w &= P_{25C} \times \frac{LI_o^2}{(LI^2)_{25C}} \\ &= 0.547 \times \frac{2.19}{2.288} \text{ W} \\ &= 0.524\text{W} \end{aligned}$$

Actual power loss in the inductor as a percentage of the power output of the switching regulator is:

$$\frac{P_w \times 100\%}{E_o \times I_o} = \frac{0.524 \times 100\%}{50} = 1.05\%$$

If power losses are not acceptable, then select a core with higher $(LI^2)_{25C}$ capability.

Step 5: In the nomogram, draw line ③ from 0.0219 mH on the "L" scale through $A_L = 160$ on " A_L " scale to the "N" scale. Note that 12 turns are required to obtain the desired inductance.

Step 6: Enter the $A_w' = 0.193$ from the table for the core selected on the " A_w " scale. Draw ④ from "N" scale where $N = 12$ through $A_w' = 0.193$ to the "wire size" scale. From this scale, note that wire size is AWG 15.2. Select the next highest integer, AWG 16, in order to fit within the available window area. This will result in a slight increase in power loss and temperature rise.

The same procedure applies if a toroid is selected instead of a pot core.

If both the LI_o^2 and $L(I_1 \text{ max})^2$ values calculated in steps 1 and 2 are less than the appropriate limiting (LI^2) values for the core selected, it is suggested that the L value of the application be increased until one or the other of the core limits is reached. This will permit reduction of ΔI_1 , and reduce the requirements of the output capacitor.

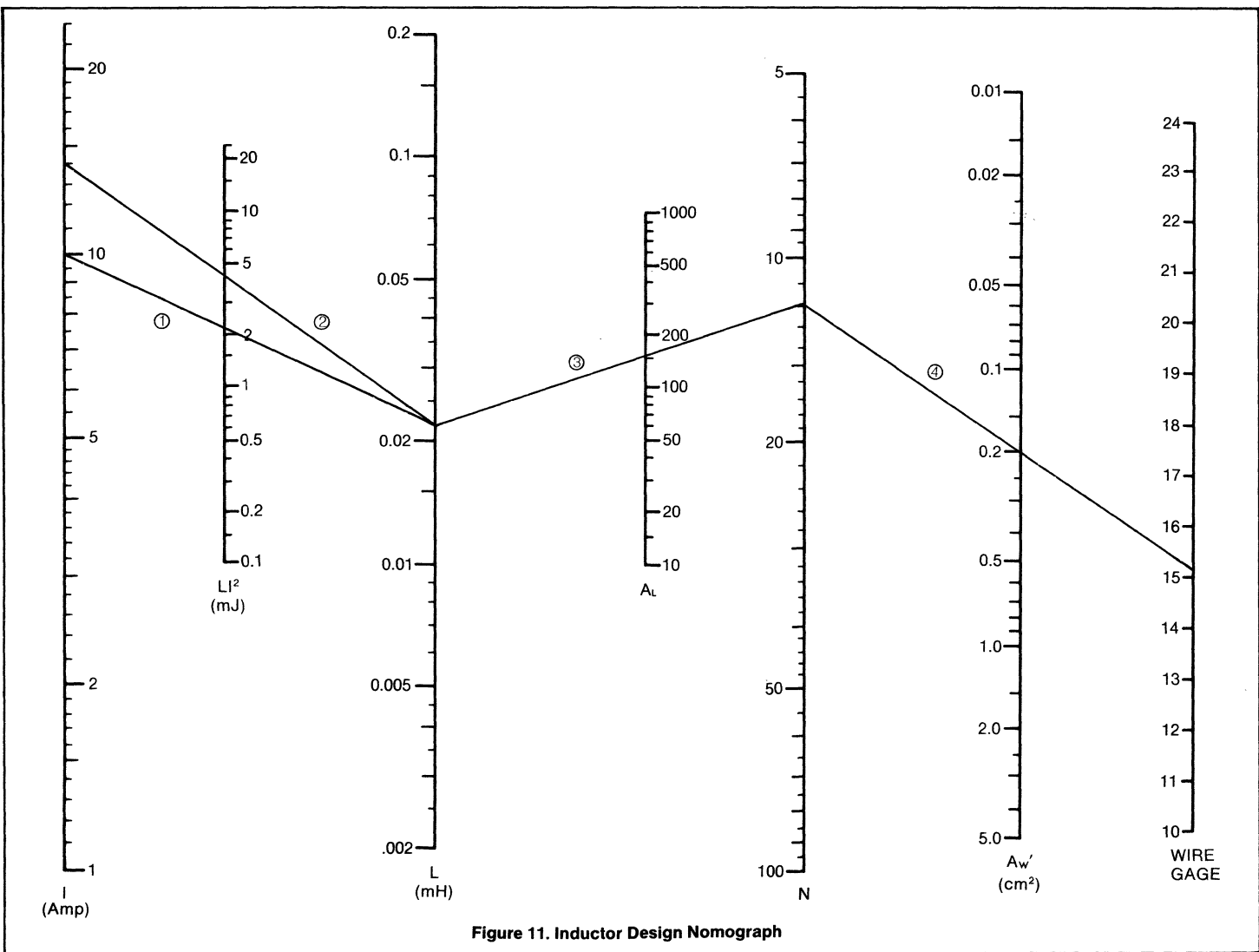


Figure 11. Inductor Design Nomograph

Table 1. Ferrite Pot Cores

Ferroxcube Part No.	Dimensions (inches)		Power Dissipation 25°C rise (watts)	Window Area 0.65 A _w (cm ²)	Inductor Index	Saturation Limit (mJ)	Dissipation Limit 25°C rise (mJ)
	(OD)	(HT)	(P _{25C})	(A _w)	(A _i)	((LI ²) _{sat})	((LI ²) _{25C})
1107-A100-3B7	0.445	0.264	0.100	0.034	100	0.200	0.077
1107-A160-3B7	0.445	0.264	0.100	0.034	160	0.144	0.124
1408-A100-3B7	0.559	0.334	0.158	0.063	100	0.490	0.180
1408-A160-3B7	0.559	0.334	0.158	0.063	160	0.324	0.288
1811-A160-3B7	0.716	0.428	0.259	0.122	160	1.02	0.719
2213-A160-3B7	0.858	0.538	0.358	0.193	160	2.12	1.32
2616- * -3B7	1.024	0.640	0.547	0.263	160*	5.06	2.29
2616-A250-3B7	1.024	0.640	0.547	0.263	250	3.24	3.58
3019- * -3B7	1.201	0.754	0.754	0.382	200*	8.57	4.90
3622- * -3B7	1.418	0.880	1.04	0.486	200*	18.4	7.21
4229- * -3B7	1.697	1.16	1.60	0.910	200*	31.8	17.9

* Indicates not stock item. Gap must be ground to obtain desired A_i.

Table 2. Mo-Permalloy Toroids

Arnold Part No.	Dimensions (inches)		Power Dissipation 25°C rise (watts)	Window Area 0.5 A _w (cm ²)	Inductor Index	Saturation Limit (mJ)	Dissipation Limit 25°C rise (mJ)
	(OD)	(HT)	(P _{25C})	(A _w)	(A _i)	((LI ²) _{sat})	((LI ²) _{25C})
A-307032-2	0.425	0.180	0.072	0.082	32	0.180	0.065
A-051027-2	0.530	0.217	0.125	0.192	27	0.296	0.199
A-189043-2	0.710	0.280	0.209	0.319	43	0.782	0.659
A-059043-2	0.930	0.330	0.346	0.703	43	1.55	2.06
A-894075-2	1.09	0.472	0.520	0.781	75	3.40	4.32
A-291061-2	1.33	0.457	0.708	1.47	61	4.54	8.97
A-298028-2	1.33	0.457	0.708	1.47	28	9.90	4.12
A-085035-2	1.60	0.605	1.04	2.14	35	20.1	8.65
A-087059-2	1.875	0.745	1.48	2.14	59	40.2	16.0

1. Power Switching Components

Voltage ratings of the power switching transistor and catch diode must be greater than the maximum input voltage, E_{in} , including any transient voltages that may appear at the input of the switching regulator. Low transistor $V_{CE\ sat}$ and diode V_F at full load output current are important considerations to maintain high efficiency (Ref efficiency calculations – Appendix A).

Fast switching diodes and transistors are required to maintain good efficiency in high frequency switching regulators. Transistor switching losses become significant when combined rise time plus fall time exceeds approximately $0.025 \times \tau$. Thus, for 50 kHz operation, $t_r + t_f$ should be approximately 0.5 μ sec or less. Transistor delay and storage times do not affect efficiency, but cause delays in turn on and turn off resulting in lowering the frequency of operation and increasing ripple. Combined $t_d + t_s$ should be less than $0.05 \times \tau$.

Unitrode manufactures a broad variety of fast switching power transistors and Darlingtons, which are listed in the Power Transistor & Darlington Product Selection Guide. Their combinational high voltage, high current, low saturation voltage and medium to fast switching characteristics make them ideal for this application.

The diode reverse recovery time must be no more than about half the current rise time through the transistor. If this requirement is not met, large amplitude reverse recovery current spikes will be drawn from the input power supply causing severe EMI problems. Large transient currents through the transistor may cause degradation or second breakdown. Referring to Figure 1, Section II, during the time that the transistor is off, the catch diode is conducting the output current, I_o , and the transistor V_{CE} equals E_{in} . When base drive is applied to the transistor to turn it on, current through the transistor rises from 0 to I_o . During this current rise time interval, t_{r1} , the diode remains in forward conduction, but the diode current declines from I_o to 0, since the inductor maintains the total current at a constant value equal to I_o . If the diode has recovered at the end of the t_{r1} interval, the voltage across the transistor will start to decrease and the diode will go into the reverse direction. This period of time is the transistor voltage rise time interval, t_{rv} , which is terminated when the transistor V_{CE} reaches $V_{CE\ sat}$ and the diode V_R reaches E_{in} . If the diode has *not* recovered at the end of the t_{r1} interval, it will remain a low impedance instead of proceeding smoothly into the reverse direction. Transistor current will increase well above I_o until the diode

recovers, pulling the additional current through the diode in the reverse direction.

This problem has probably caused more grief in switching regulator applications than any other, and almost completely dominates diode selection. Diode switching losses will be completely negligible if the diode is fast enough to minimize the recovery problem, i.e., two to three times faster than the transistor turn-on rate.

Unitrode UES rectifiers, listed in the Rectifier Product Selection Guide, are uniquely suited to this type of application. With low forward drop and typical recovery time of 20 nsec from forward currents as high as 50A, they cause no discernible recovery spike when used in conjunction with Unitrode's medium frequency switching transistors.

Unitrode PIC600 Hybrid Power Switches summarized in the Switching Regulator Power Circuits Product Selection Guide combine in a single package the UES rectifier and power switching transistor with its associated drive transistor and bias resistors. Power transistor, drive transistor and rectifier are matched to optimize switching speeds and $V_{CE\ sat}$. Available in NPN and PNP versions, the PIC600 series can operate at 50 kHz with only 2.5 percent loss of efficiency compared with operation at lower frequencies. Significant reduction of EMI can be achieved because of the reduction of circuit wiring.

2. Output Filter Capacitor.

The most difficult component selection problem for high frequency switching regulator applications is to find and specify an output capacitor with suitably low ESR. Most tantalum and aluminum electrolytic capacitor types do not have ESR specifications (probably because ESR is not very good). In some cases, the dissipation factor, DF, is given in the specification. However, DF is usually specified at 60 Hz, which is more indicative of effective *parallel* resistance, and is virtually useless in determining ESR. When DF is specified at 1 kHz or higher, it may be used to determine ESR:

$$ESR = DF (\%) \times 0.01 \times X_C = \frac{DF (\%) \times 0.01}{2\pi f C}$$

The power circuit design example given in Section IV requires an output capacitor with C_{min} of 114 μ fd and ESR_{max} of 0.025 Ω . The capacitor which comes closest to meeting this requirement (after a limited search) is solid tantalum, Mallory THF, 120 μ fd @ 10V. This capacitor has a max DF of 8% at 1 kHz, which defines $ESR_{max} = 0.106\Omega$. ESR is typically 0.05 Ω . Two of

these capacitors in parallel are required, based on typical ESR, to achieve an ESR of 0.025Ω ; four in parallel are required, based on ESR_{max} of the capacitor. The aluminum electrolytic which comes closest (again based on a limited search) is the Sprague 672D series, $1000\ \mu\text{fd}$ @ 12V , which has an ESR_{max} of 0.065Ω @ $50\ \text{kHz}$. Typical ESR is 0.025Ω . In either case, a much larger C value is required in order to achieve the desired ESR. This does have the advantage of reducing transient voltage changes with sudden changes in load current.

It is worth noting again that with the control circuits shown in Section III (unlike conventional switching regulator control circuits), the operating frequency will remain relatively constant, regardless of ESR, although the output ripple voltage will vary directly with ESR. In some cases, it may be economically advantageous to increase the value of L (and the size and cost of the inductor) in order to reduce ripple current, $\Delta i_1 = \Delta i_2$, and thereby increase the ESR_{max} requirement.

In addition to considering the C and ESR values and appropriate voltage derating for the application, most capacitors have maximum RMS ripple current or max RMS ripple voltage ratings which should not be exceeded. Actual RMS ripple current and voltage in the application can be calculated as follows:

$$\Delta e_{o,RMS} = \Delta e_o \text{ p-p} / 3.0$$

$$\Delta i_{RMS} = \Delta i_1 \text{ p-p} / 3.5$$

In the design example of Section IV, $\Delta e_{o,RMS} = 0.033\text{V}$, which is less than the 0.05V max ripple rating of the 10V Mallory THF capacitor, and $\Delta i_{RMS} = 1.14\text{A}$, which is less than the 2.47A max ripple current rating of the $1000\ \mu\text{fd}$, 12V Sprague 672D capacitor.

Series inductance of the capacitor is usually not significant compared to ESR at frequencies below $100\ \text{kHz}$. However, inductance can become dominant if good wiring practices are not followed. Specifically, the ground side of the catch diode should be returned directly and as close as possible to the ground side of the capacitor, and capacitor lead length including circuit wiring on both sides of the capacitor should be minimized.

3. Control Amplifier and Reference.

Control circuits for switching regulators can be designed around IC operational amplifiers and separate voltage references, or around low power voltage regulator IC's which have built-in references. Voltage regulator IC's such as the LM304, LM305, and $\mu\text{A}723$ have the added advantage that the output current they provide to drive the power switching transistor can be caused to diminish at higher temperatures, which conforms to the transistor drive requirements vs. temperature and helps to maintain optimum switching speeds over a range of temperatures. Amplifiers used in the control circuit should be uncompensated in order to obtain fast switching speeds, otherwise the delay times introduced will result in lower frequency operation and larger ripple amplitudes, and may cause circuit instability.

Appendix A Analysis of Power Circuit

The design equations for the switching regulator power circuit used throughout this design guide were based on several simplifying assumptions, which will now be dealt with.

The simplified equations neglected the effect of "catch" diode forward drop, V_F , transistor saturation voltage, V_{sat} , and the IR drops in the inductor and current sensing resistor, $I_o R_x$. If a design is implemented using the values of L , C , ESR, and Δi derived from the simplified equations, then t_{on} , t_{off} , f , and Δe_o will differ from the design values because of the effect of the simplifying assumptions as follows, from Figure 2b:

Simplified :

$$\Delta i_1 = \frac{(E_{in} - E_o)t_{on}}{L} \quad (1)$$

Exact :

$$\Delta i_1 = \frac{(E_{in} - E_o - V_{sat} - I_o R_x)t_{on}'}{L} \quad (2)$$

Simplified :

$$\Delta i_1 = \frac{E_o t_{off}}{L} \quad (3)$$

Exact :

$$\Delta i_1 = \frac{(E_o + V_D + I_o R_x)t_{off}'}{L} \quad (4)$$

Note that Δi_1 is fixed, because the control circuit controls this value directly. Instead of the original design values of t_{on} and t_{off} , actual values t_{on}' and t_{off}' will be observed. Since Δi_1 is fixed, we can equate Equations (1) to (2) and (3) to (4):

$$\frac{t_{on}'}{t_{on}} = \frac{(E_{in} - E_o)}{(E_{in} - E_o - V_{sat} - I_o R_x)} \quad \text{and}$$

$$\frac{t_{off}'}{t_{off}} = \frac{E_o}{E_o + V_D + I_o R_x}$$

Although the actual t_{off}' is less than the assumed t_{off} , t_{on}' is greater than the assumed t_{on} , so that their net effect on the operating frequency is reduced. In the worst case, when E_o is small (5V) and E_{in} is high (50V), the actual frequency will be 25 percent higher than the original assumed frequency, resulting in a very slight drop in efficiency. Output ripple component Δv_C will be smaller because of the higher frequency, and Δv_{ESR} will not change because Δi_1 is fixed. Component tolerances will result in larger deviations than those caused by the use of the simplified equations.

The only other assumption that could have possible significance is that the transistor switching times are negligible at the highest frequency of operation. The validity of this assumption is normally assured by selecting appropriate devices (see Section VI). This also applies to the speed of the control circuit. If delay time through the control circuit in addition to transistor turn-on and turn-off times is significant with respect to the total period, τ , the consequent delay in turning the power circuit on and off will cause a proportional increase in Δi_1 and Δe_o , and a proportional decrease in frequency.

Efficiency Calculations: The efficiency of a switching regulator depends upon the factors given in the following equation:

$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%$$

$$= \frac{E_o \times I_o}{E_o \times I_o + P_T + P_D + p_T + p_D + P_L + P_I + p_C + P_C}$$

Note that the worst case for each factor does not necessarily occur under the same conditions.

1. *DC Losses – Transistor.* (Worst case when E_{in} is lowest because t_{on} is largest.)

$$P_T = V_{\text{CEsat}} \times I_o \times \frac{t_{\text{on}}}{\tau}$$

where: $\frac{t_{\text{on}}}{\tau} = \frac{E_o}{E_{\text{in}}}$

2. *DC Losses – Diode.* (Worst case when E_{in} is highest.)

$$P_D = V_F \times I_o \times \frac{t_{\text{off}}}{\tau}$$

where: $\frac{t_{\text{off}}}{\tau} = 1 - \frac{E_o}{E_{\text{in}}}$

3. *Switching Losses – Transistor.* (Worst case when E_{in} is high. $t_d + t_s$ do not contribute to power losses.)

$$p_T = E_{\text{in}} \times I_o \frac{t_r + t_f}{2\tau}$$

where: $t_r = t_{rv} + t_{ri}$, $t_f = t_{fv} + t_{fi}$

4. *Switching Losses – Diode.*

This is a very complex calculation if diode recovery time is not much smaller than the transistor rise time, because the diode will short-circuit the power supply prior to turn-off, affecting the transistor dissipation, possibly causing second breakdown, and generating intolerable EMI. By using a diode whose recovery time is not more than half the transistor rise time, all these problems become negligible.

5. *DC Losses – Inductor.* (AC losses are negligible when ΔI_1 is small compared to I_o .)

$$P_L = I_o^2 \times R_s$$

where: R_s is equal to effective series resistance of inductor.

6. *DC Losses – Current Sense Resistor.* (AC losses negligible when ΔI_1 is small compared to I_o .)

$$p_r = I_o^2 \times R_i$$

7. *AC Losses – Capacitor.* (Usually negligible.)

$$p_C = \frac{\Delta I_1^2}{12} \times \text{ESR}$$

8. *Control Circuit Losses.* (Base drive to switching transistor is dominant, but usually negligible.)

$$P_C = E_{\text{in}} \times I_b \times \frac{t_{\text{on}}}{\tau} = E_o \times I_b$$

where: $\frac{t_{\text{on}}}{\tau} = \frac{E_o}{E_{\text{in}}}$

Appendix B

Analysis of Power Inductor Design

This appendix describes the methods used to develop the core tables given in Section V and the nomographic method for design of the power inductor. Core parameters for any cores not listed in the tables can be derived from the equations given.

The following equations provide the basis for this design approach. Equation (1a) defines the value of inductance, L, in terms of basic core parameters and the total number of turns, N, wound on the core:

$$L = N^2 \times 0.4\pi \mu \frac{A_e}{\ell_e} \times 10^{-5} \quad \text{mH} \quad (1a)$$

where: μ = effective permeability of core
 ℓ_e = effective magnetic path length – cm
 A_e = effective magnetic cross section – cm²

For most standard cores, the above calculation has been simplified by listing the compound parameter A_L , called the "inductor index", as follows:

$$L = N^2 A_L \times 10^{-6} \quad \text{mH} \quad (1b)$$

where: $A_L = 0.4\pi \mu \frac{A_e}{\ell_e} \times 10$ mH for 1000 turns

Multiplying both sides of Equation (1b) by I²,

$$LI^2 = (NI)^2 A_L \times 10^{-6} \quad \text{millijoules} \quad (2)$$

Core Saturation Limits.

Any specific core has a maximum ampere-turn, NI, capability limited by magnetic saturation of the core material. (NI)_{sat} is listed in some core catalogs, in which case the maximum (LI²)_{sat} capability of the core can be calculated from Equation (2). (NI)_{sat} is related to the saturation flux density, B_{sat}, as follows:

$$(NI)_{\text{sat}} = 10 \frac{B_{\text{sat}} A_e}{A_L} \quad \text{ampere-turns} \quad (3)$$

Substituting Equation (3) into (2),

$$(LI^2)_{\text{sat}} = \frac{B_{\text{sat}}^2 A_e^2 \times 10^{-4}}{A_L} \quad \text{millijoules} \quad (4)$$

Values of (LI²)_{sat} are given for each core represented in Tables 1 and 2 of Section III. Equation (2) or (4) was employed, using values for either B_{sat} or NI which would result in a reduction of A_L (and L) of 20 percent under maximum overload conditions, according to the core manufacturer's data. The core selected for an application must have an (LI²)_{sat} value greater than L(i₁ max)² to insure that the core will not saturate under maximum peak overload current conditions.

Power Dissipation and Temperature Rise Limits.

In switching regulator applications, the AC current component is small compared to the DC current through the power inductor. Power dissipation in the inductor is almost entirely DC losses in the winding. DC resistance of the winding, R_s, is calculated from the following:

$$R_s = \rho \frac{\ell_w}{A_x} N \quad \text{ohms} \quad (5)$$

where: ℓ_w = mean length of turn – cm
 A_x = effective area of wire – cm²
 ρ = resistivity of wire – Ω -cm

Core geometry provides a certain window area, A_w , for the winding, but only a fraction of this area can be occupied by the actual conductor. The *effective* window area, A_w' is taken as 0.5 A_w for toroids, and 0.65 A_w for pot cores. This allows for wasted area of uniformly wound round wire with HF insulation, allows for the fact that the central fourth of the window area of a toroid cannot practically be filled, and allows for a single section bobbin in the case of the pot core. The number of turns, area of wire, and effective window area of a fully wound core are related by:

$$A_x = \frac{A_w'}{N} \text{ cm}^2 \quad (6)$$

Substituting Equation (6) into (5):

$$R_s = \rho \frac{\ell_w}{A_w'} N^2 \quad \text{ohms} \quad (7)$$

Multiplying both sides of Equation (7) by I^2 , the power dissipation in the winding, P_L , is:

$$P_L = I^2 R_s = I^2 \rho \frac{\ell_w}{A_w'} N^2 \quad \text{Watts} \quad (8)$$

Substituting for N from Equation (1b), and rearranging:

$$LI^2 = P_L \frac{A_s A_w'}{\rho \ell_w} \times 10^{-6} \quad \text{millijoules} \quad (9)$$

Equation (9) shows that the LI^2 capability is directly related to, and is limited by the maximum permissible power dissipation. Using a value for P_L that will result in a 25°C rise in the temperature of the inductor, values of $(LI^2)_{25C}$ are calculated for each core in Tables 1 and 2 of Section III. For these calculations, resistivity, ρ , is assumed to be $1.9 \times 10^{-6} \Omega$ -cm, the resistivity of copper wire at 65°C. The power dissipation that will result in a 25°C rise is calculated and tabulated for each core as follows:

$$\Delta T = 850 \frac{P_L}{A_s} \quad ^\circ\text{C} \quad (10)$$

where: ΔT = temperature rise
 A_s = surface area of inductor – cm²

The factor 850 in the above equation represents a temperature rise of 850°C for 1W power dissipation from 1 cm² surface area, empirically determined for natural convection cooling. The surface area, A_s , used in the calculation is taken as the top and sides of the inductor, ignoring the mounted bottom surface. Substituting a temperature rise of 25°C:

$$P_{25C} = \frac{25 \times A_s}{850} \quad \text{Watts} \quad (11)$$

Appendix C

Analysis of Application Circuits

The design equations for the critical components and operating parameters of Figure 3, Section III, are given below, for the following design objectives:

$$\begin{aligned} E_o &= +5V \\ \Delta e_o &= 100 \text{ mV p-p} \\ E_{in} &= 20V \text{ min, } 40V \text{ max} \\ I_o &= 2A \text{ min, } 10A \text{ max} \\ \text{Current Limit} &= 14A \text{ max peak} \end{aligned}$$

Using the procedure described in Section IV, the following parameters were established:

$$\begin{aligned} f &= 50 \text{ kHz (nominal)} \\ t_{off} &= 17.5 \mu\text{sec} \\ L &= 22 \mu\text{H} \\ C &= 120 \mu\text{F min} \\ \text{ESR of capacitor} &= 0.025 \Omega \text{ max} \\ \Delta i_1 &= 4A \end{aligned}$$

From the manufacturer's design data for the LM305, we know that: the internal reference voltage, V_{ref} , is 1.8V, nominal; the impedance of the inverting input is very high; the threshold level of the drive-current-limiting circuit is 0.30V; and the impedance of the non-inverting input (R_{in}) is 2.4K, nominal.

From the Unitorde data for the PIC625 Hybrid Power Switch, the drive current (I_{drive}) required for $I_o = 10A$ is 30 mA. The V_{BE} of Q1 is taken as 0.6V.

First, we may calculate the values R_1 and R_2 of the output divider. We will make the effective parallel resistance of R_1 and R_2 equal to 2.4K, so that the impedance at the inverting input will be approximately the same as the noninverting input of the LM305:

$$\begin{aligned} \frac{R_2}{R_1 + R_2} &= \frac{V_{ref}}{E_o} = \frac{1.8}{5} \\ \frac{R_1 R_2}{R_1 + R_2} &= R_{in} = 2.4K \end{aligned}$$

The resulting values are $R_1 = 6.8K$, $R_2 = 3.8K$. R_2 may be trimmed for precise setting of E_o .

C_1 and C_2 function to provide negative and positive AC feedback, and should be large enough to result in small losses to the AC signals. Assuming that $R_{in} = (R_1 \times R_2)/(R_1 + R_2)$, the value of C_1 should be twice the value of C_2 , so that the negative feedback will be dominant over positive feedback at all frequencies, thereby ensuring circuit stability. The following relationships satisfy these conditions:

$$C_2 \cong \frac{1}{R_{in} \times f} \quad ; \quad C_1 = 2 \times C_2$$

where: f = the nominal switching frequency.

These equations are satisfied by $C_2 \approx 0.01 \mu\text{F}$ and $C_1 = 0.02 \mu\text{F}$. Making C_1 and C_2 too large will have an adverse effect on transient recovery time of the switching regulator.

R_4 is calculated from the threshold voltage of the LM305 drive current limiting circuit and the required base drive current.

$$R_4 = \frac{V_{\text{threshold}}}{I_{\text{drive}}} = \frac{0.3V}{0.03A} = 10\Omega$$

Current sampling resistor R_i is determined by the desired short circuit current limit and the V_{BE} of Q1. As described in Section III, under *current overload conditions*, current i_1 ranges between two values. The maximum instantaneous overload current is defined by: $i_1 \times R_i = V_{BE} + V_{R_3}$. The minimum instantaneous overload current is defined by: $i_1 \times R_i = V_{BE}$.

Since Δi_1 has been previously defined as 4A p-p, if we assume a minimum value of 10A for i_1 under overload conditions, then the maximum peak overload value for i_1 will be 14A, and the average value of $i_1 = I_o$ under overload conditions is 12A.

$$R_i = \frac{V_{BE}}{i_1 (\text{min overload})} = \frac{0.6V}{10A} = 0.06\Omega$$

Power dissipation in R_i will be 6W under full load conditions, and 8.64W under overload conditions.

R_3 determines Δi_1 under overload conditions as well as for normal operation of the switching regulator:

$$\begin{aligned} R_3 \times I_{\text{drive}} &= R_i \times \Delta i_1 \\ R_3 &= \frac{R_i \times \Delta i_1}{I_{\text{drive}}} = \frac{0.06 \times 4}{0.030} = 8\Omega \end{aligned}$$

The value of R_5 is determined empirically to optimize regulation versus changes in E_{in} . With R_5 omitted, E_o changes approximately 70 mV when E_{in} is changed from 20V to 40V. With $R_5 = 1.2 \text{ M}\Omega$, the change in E_o is reduced to less than 25 mV.

THE IMPORTANCE OF RECTIFIER CHARACTERISTICS IN SWITCHING POWER SUPPLY DESIGN

With the increasing interest in switching regulated power supplies designers have directed much of their effort to selecting transistors with low switching losses and adequate power handling capability. While recognizing that they must use fast recovery rectifiers, less attention has been given to "how fast" or "what type of recovery characteristic" is desired. More detailed knowledge of rectifier behavior allows determination of the magnitude of increased losses and stress on the transistor by the non-ideal diode. By choosing the best available rectifier, transistor stress can be minimal, thereby resulting in higher reliability. Other benefits are:

- A. Improved power supply efficiency
- B. Lower noise
- C. Lower cost and/or
- D. Smaller size and weight

The performance of fast rectifiers in the most popular switching circuits is discussed below.

"Switcher" inputs use available DC voltages, or rectifiers directly off the AC line. This DC "input" is converted by semiconductor switches operating at high frequency in circuits such as buck, flyback or boost regulators and in pulse-width-modulated or square wave inverters.

Inverter output rectifiers and regulator "catch" diodes are subject to unusual stresses due to the fast switching rates and very low impedance seen by the diode during the reverse transient (diode turn-off) and a momentary high impedance during diode turn-on.

These new square wave switching supplies are limited in efficiency and frequency by transistor stress and switching losses, some of which is due to diode switching characteristics. Faster transistors and diodes are helping to increase efficiency and/or frequency. At low output voltages, and lower frequency the DC characteristics ($V_{CE(sat)}$ and V_F) have the major influence on efficiency. However, as frequency and/or input voltage increase the switching characteristics become increasingly important.

BUCK REGULATOR ANALYSIS

Ideal Diode — For better understanding consider the buck regulator and resulting waveforms, using an *ideal* diode and assuming linear current rise and fall in the power transistor during switching. Similar considerations apply to other types of switching regulator circuits.

The transistor "on" time, t controls the conversion such that,

$$(1) V_o = \frac{t}{\tau} V_i$$

where τ is the period. t is determined by the control circuit which senses output voltage and controls transistor base drive.

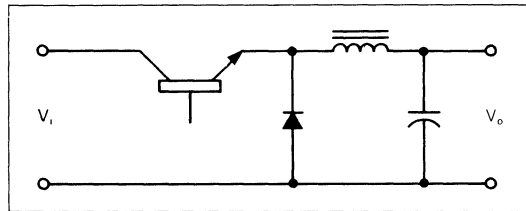


Figure 1a

In this regulator the inductor current is essentially constant as it flows alternately through the transistor or "catch" diode. The sum of the transistor current and diode current must always equal the current in the inductor, which cannot change instantaneously.

At t_0 the diode is conducting inductor current while the transistor is blocking the input voltage.

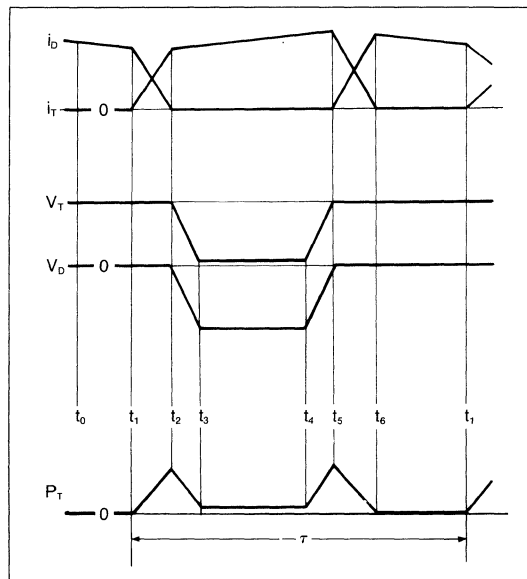


Figure 1b

t_1 to t_2 is the current rise time t_{ri} of the transistor. Since inductor current is not changing, the diode current must decrease. The forward biased diode maintains full input voltage across the transistor.

At t_2 the transistor is conducting all the inductor current so the diode turns off and voltage across the transistor

starts to decrease toward $V_{CE(sat)}$.

t_2 to t_3 is the voltage rise time, t_{rv} of the transistor.

From t_3 to t_4 the transistor is saturated and conducting the inductor current i_L .

At t_4 the transistor starts to turn off and V_{CE} increases.

t_4 to t_5 is the voltage fall time t_{fv} of the transistor. During this time the transistor must conduct the entire inductor current because the diode is still reverse biased. At t_5 the diode is forward biased and the transistor is blocking the full input voltage. Diode current starts to increase and the transistor current decreases, the sum equalling i_L .

t_5 to t_6 is the current fall time t_{fi} of the transistor. Diode current increases in a complementary manner. From t_6 to t_1 the transistor is off and the diode is conducting all the inductor current.

To simplify the illustration assume the inductor current constant and equal to I_o . Transistor dissipation P_T is the sum of transient switching and DC losses. Neglecting losses due to DC leakages, which are generally negligible:

$$(2) P_T = \frac{V_i I_o}{2} \left(\frac{t_{ri} + t_{rv} + t_{fv} + t_{fi}}{\tau} \right) + \frac{V_{CE(sat)} I_o (t_4 - t_3)}{\tau}$$

$$(3) P_T = \frac{I_o}{\tau} \left\{ \frac{V_i}{2} (t_{ri} + t_{rv} + t_{fv} + t_{fi}) + V_{CE(sat)} (t_4 - t_3) \right\}$$

Practical diode — Now consider how the non-ideal diode with reverse recovery, junction capacitance, forward recovery and DC loss affects the circuit of Figure 1a.

In Figure 1c the solid lines are the waveforms using a practical diode in a buck regulator circuit. Comparing them with the dotted lines of the ideal diode previously considered we see three significant differences during transient switching and one during DC conduction:

1. The peak collector current increases (above I_o) during a period of high dissipation t_2 to t_2' .
2. Rise times t_{ri} and t_{rv} are increased. $(t_2' - t_1) > (t_2 - t_1)$ and $(t_3' - t_2') > (t_3 - t_2)$.
3. Maximum collector voltage peaks up above V_i briefly at t_5 .
4. The diode has DC loss (from t_6 to t_1) and switching loss (principally from t_2' to t_3').

From the P_T curve of Figure 1c it is obvious that transistor power dissipation increases above that of (3) due to the "real" diode, — see the hatched regions.

The magnitude of these detrimental factors depends on the choice of rectifier. Before considering losses more fully let us examine the switching periods in greater detail.

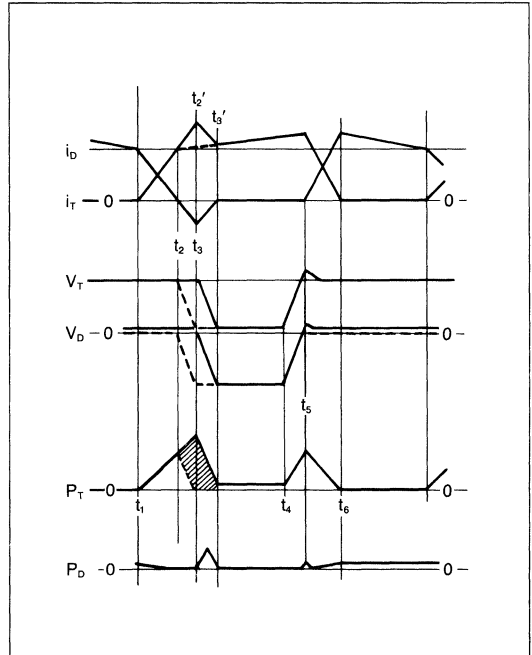


Figure 1c

TRANSISTOR TURN-ON BEHAVIOR

The transistor "turn-on transient", when the diode is switching from forward conduction to reverse blocking, results in the following transistor and diode waveforms:

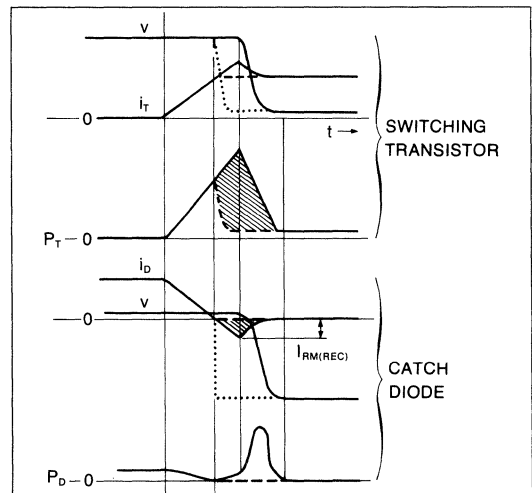


Figure 2

Dashed lines show what the current and power would be if the diode were ideal to the extent of having no reverse recovery time or junction capacitance. (Dotted

lines show the voltage for the ideal diode case.) The reverse diode current caused by diode capacitance and recovered charge is shown by the cross hatched area of the i_D curve. The transistor must conduct this reverse diode current as well as the inductor current. The grey area represents additional transistor dissipation due solely to the diode recovered charge and capacitance.

Faster switching transistors will not necessarily result in reduced switching losses. Unless a diode with recovery time 2 or 3 times faster than the transistor current rise time is used, a faster transistor will increase the peak recovery current in the diode and thus increase overall switching losses. Furthermore, a diode with a "soft" recovery characteristic will cause more dissipation than an "abrupt" type with the same peak recovery current. The relationship of recovery characteristic to switching rate is discussed in Appendix B. With many switching transistors now available a 200 nS fast-recovery rectifier will have a peak recovery current $I_{RM(REC)}$ greater than shown in the i_D waveform of Figure 2, where it is about $\frac{1}{3}$ of the forward current. This rather modest additional collector current (of 33% above that limited by an ideal diode) can cause increased transistor power dissipation of 100 to 150% during the turn-on period. Other serious problems can occur from high peak currents, such as noise transients in the line, the transistor coming-out of saturation and forward-biased second breakdown.

Rectifiers are now available with recovery characteristics to keep these problems minimal. Their use is required for a switching supply of maximum reliability and efficiency.

TRANSISTOR TURN-OFF BEHAVIOR:

When the transistor turns off, the diode turn-on characteristic usually has little effect on power dissipation but may cause voltage spiking, with resulting noise and the

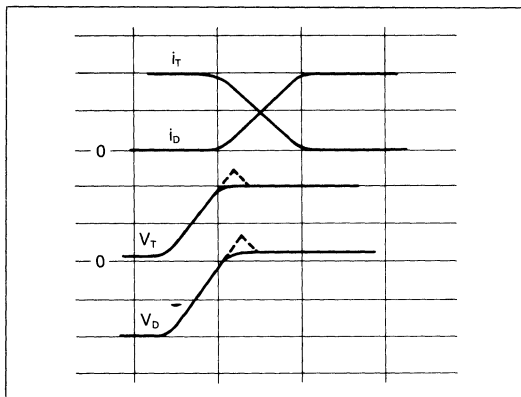


Figure 3

possibility of exceeding the transistor voltage ratings. Diode characteristics and conditions under which these transients occur are discussed in Appendix C. The voltage spike is due to the forward recovery characteristic and, when present, will occur as shown (dotted) in Figure 3. To correct it a snubber (series RC across the diode) may be needed. However, the choice of an optimum diode will minimize or eliminate this need.

POWER LOSSES IN THE SEMICONDUCTOR DEVICES

DC Losses in the buck regulator occur alternately when the diode is forward conducting and when the transistor is turned on. Referring to Figure 1 these intervals are t_6 to t_1 and t_3 to t_4 respectively. During *either* interval the dissipation is independent of input voltage, V_i , or output voltage, V_o , depending only on load current and device voltage drop. *Total circuit DC losses* are a function of V_o/V_i because a) this ratio relates to "on" time and b) transistor $V_{CE(sat)}$ will probably not equal diode V_F . Neglecting switching intervals the dissipation due to DC losses is:

$$(4) P_{DC} = V_F I_o \frac{V_i - V_o}{V_i} + V_{CE(sat)} I_o \frac{V_o}{V_i}$$

Loss of efficiency due to DC losses is greatest when V_o is low, with diode loss being more significant when V_i is relatively high and transistor loss dominating when V_i is close to V_o .

Transient (switching) losses in the regulator vary considerably with voltage, being highest at "high line" V_i (see Eq. 3). Furthermore, high voltage transistors and rectifiers generally have longer switching times than low voltage types. Speed and "recovery characteristic" (see Appendix B), and consequently losses, can vary greatly between different device types and manufacturing processes. A relationship for calculating approximate transient dissipation of practical devices during the transistor turn-on interval is given in Appendix B. The other component (turn-off interval) can be similarly developed but it is not significantly affected by diode selection. However, when transistors and/or drive techniques are chosen for shorter fall times overall losses are reduced *and* the benefits of optimum diode selection become more significant. Proper diode (and transistor) selection is important in all switching supplies, but the higher the voltage (and frequency) the more significant will be the effect of selection on switching losses.

OTHER SWITCHING CIRCUITS

The pulse-width-modulated inverter (PWM) supply (Figure 4a) has much in common with the buck regulator. Output rectifiers also perform the catch diode function. Current waveforms are shown in Figure 4b,

with overshoot due to diode reverse recovery and capacitance. Here again slow diodes cause additional transistor stress, usually not reduced significantly by transformer impedance. Leakage reactance will often require the use of a snubber, to protect the transistor.

Transistor "on" time t and the turns-ratio control the conversion such that

$$(5) V_o = \frac{2t \cdot N_s}{\tau \cdot N_p} V_i$$

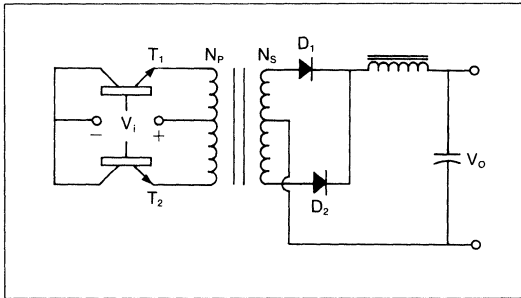


Figure 4a

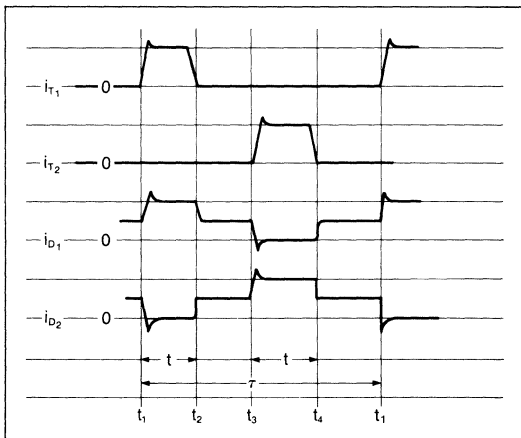


Figure 4b

From t_1 to t_2 transistor T_1 and diode D_1 conduct, with diode current equal to inductor current i_L .

At t_2 the transistor turns off and the inductor "pulls" i_L equally through D_1 and D_2 .

At t_3 transistor T_2 turns on, driving full i_L through D_2 and causing D_1 to be reversed biased. D_2 current is increased by the recovery current of D_1 , and T_2 current also increases proportionally.

From t_4 to t_1 , both transistors are again off and at t_1 the events of t_3 occur on the opposite device pair.

One difference between the inverter and the regulator is that here the DC diode losses are more significant

because they (D_1 and/or D_2) are conducting the full cycle regardless of V_i to V_o ratio. Another difference is that here the diode recovery is from half, rather than full, load current.

The square wave inverter can be considered, in terms of device operation, a special case of the PWM where $2t$ approaches τ . Regulation is achieved by varying V_i .

EMI, RFI, NOISE —

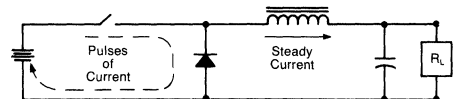
Given any inductance in a circuit "loop" of wiring, a rapid current change will generate a voltage transient, $V = L di/dt$, and the energy in such a transient will vary with the square of the current, $E = \frac{1}{2}LI^2$. The interference and voltage spiking will be easier to filter if the energy is low and has predominantly high frequency components.

We can establish a priority of factors for reducing EMI:

1. $I_{RM(REC)}$ should be as low as possible, — accomplish by diode selection (see Appendix B and Fig. 7).
2. L (circuit loop) should be minimum, — accomplish by layout and interconnect geometry. (See Fig. 5).
3. Use a "soft recovery" diode (See Appendix B). However, this is an item of possible trade-off since such a device may have longer t_{rr} , higher $I_{RM(REC)}$ and, thus, create much higher switching loss.

An ultra-fast device with moderate recovery (vs. abrupt or soft) will often be the best choice.

REDUCE EMI BY LOWERING CIRCUIT WIRING INDUCTANCE:



Low L needed in loop shown in grey. Avoid ground loop noise by returning input capacitor directly to diode.

Figure 5a

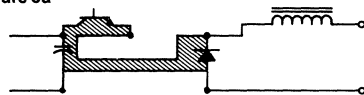


Figure 5b

SELECTING THE BEST SWITCHING RECTIFIER

Ratings and characteristics have different priorities and significance when they are to be applied to these power switching circuits. Selection should be based on the following:

1. **Peak inverse voltage, PIV** of "catch" diodes must at least equal the highest input voltage, while PIV of center-tap output rectifiers must be at least twice the maximum output voltage in a square wave inverter and much greater in the pulse width modulated inverter. More significant perhaps are the transient voltages in practical fast switching circuits partly due to wiring inductance and rectifier's own recovery. Unless these are intentionally clipped, damped, or "designed out" it is advisable to use a safety factor of 2 or 3. PIV selected

should apply over a range from lowest ambient to the highest expected junction temperature.

2. Reverse recovery time t_{rr} must be much lower than the rise time of the transistor with which it will be used, — preferably by at least 3 times when measured at conditions similar to circuit operation. Selection is complicated because rectifiers are normally specified at conditions less severe than in power switching circuits. Furthermore, correlation between test conditions is not always the same (see Table I of Appendix B).

Following preliminary selection from available data the devices should be compared in a circuit developing the highest current, junction temperature and rate of current switching ($- di/dt$) expected.

The desired goal is to minimize peak recovery current $I_{RM(REC)}$ and switching loss. Note that these are the same order of magnitude with Schottky rectifiers (due to high capacitance, principally) as with the fastest PN rectifiers. The figures below illustrate these points. Figure 6 shows the variation of peak current with switching rate, using the Unitrode UES 801 in a special test circuit. Figure 7 shows the difference in $I_{RM(REC)}$ and t_{rr} when representative fast recovery DO-5 devices are measured in a JEDEC test circuit at different temperatures. In Figure 8 the incremental collector current (the peak value in excess of 30 A) for a 30 A buck regulator using 50, 100, and 200 nS catch diodes is plotted as a function of transistor rise time (and resulting di/dt). Figures 9a, b, and c show the loss of efficiency due to transistor turn-on dissipation as a function of operating frequency, with 3 transistor rise times and 3 diode recovery times, in a regulator operated with 40 V in and 10 V out. Similar figures can be developed for other conditions using the model and assumptions in Appendix B.

3. Forward voltage should be as low as possible to optimize efficiency, especially for inverter output rectifiers and regulators with high V_i/V_o ratios. Loss of efficiency due to V_F is most significant at low output voltages. Figure 10, which relates this loss to device choice over the range of available forward voltages, applies to output rectifiers of inverter supplies with popular output voltages.

Schottky rectifiers have the lowest V_F and are therefore widely used as output rectifiers for 5 V supplies. Their limitations in PIV, transient voltage capability and temperature must be considered when applying them in other applications.

Selection should be based on conditions where losses are most significant, — at rated supply output current and anticipated junction temperature. The approximate range of V_F , at rated current and 25°C, as well as at more typical operating conditions, is shown in Figure 11 for representative fast rectifier types. Note that the

Unitrode UES series is closest to the Schottky, especially at expected operating conditions.

4. Maximum average rectified output current at maximum expected case or ambient temperature must always be considered. Note however, that standard current rating is based on a half sine waveform. These square wave applications at average current equal to this rating will usually dissipate somewhat lower power, and, thus, be used conservatively. However, regulators with $V_i \leq 1.5 V_o$ should use a catch diode with a higher rating than the average current it conducts at full load.

5. Peak voltage $V_{F(DYN)}$ during forward recovery will be of significance when using transistors with fast fall times at close to the V_{CE} rating. This is further discussed in Appendix C. See Table II for typical performance of representative devices. At lower values of di/dt the peak voltages will be lower.

6. Surge current (8.3 mS) is not of great significance because transistor saturation limits fault current. If the power supply is designed to provide rapid charging of a large output capacitor the "overload" requirement for the charge time (perhaps 0.1 to 2 seconds or so) must be considered.

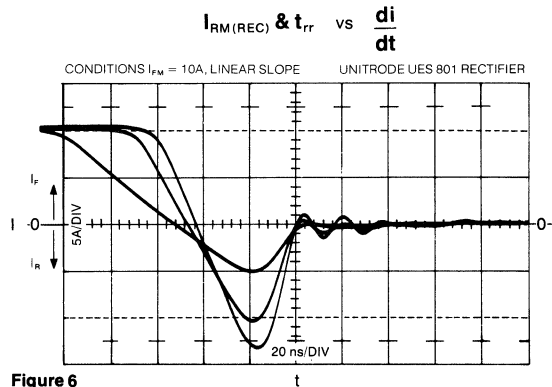


Figure 6

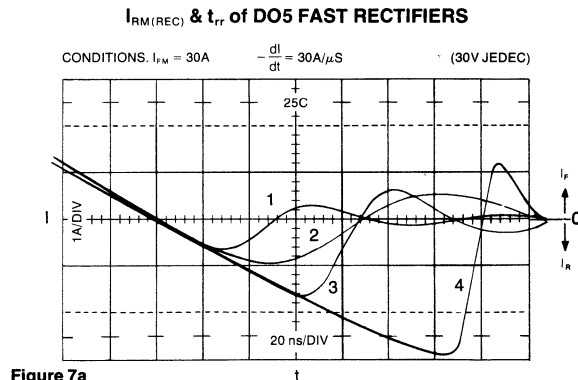


Figure 7a

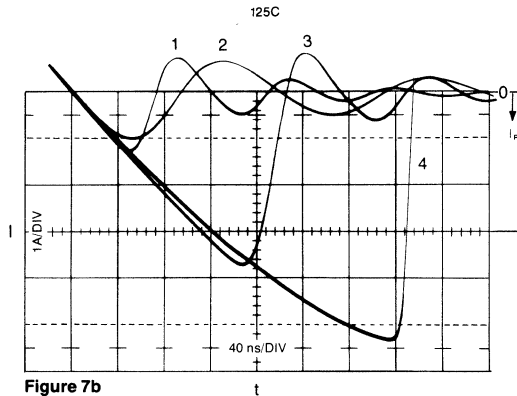


Figure 7b

DEVICE TYPE	I _{RM(REC)}		t _{rr}		t _{rr} MAX. At Low Current Cond'ns.
	25°C (A)	125°C (A)	25°C (nS)	125°C (nS)	
1	0.6	1.3	50	72	50
2	1.0	1.0	86	95	—
3	1.7	3.7	86	185	100
4	2.9	5.4	142	296	200

- 1 Unitorde UES 803
- 2 Schottky rectifier.
- 3 100nS rectifier.
- 4 200nS rectifier.

Figure 7c

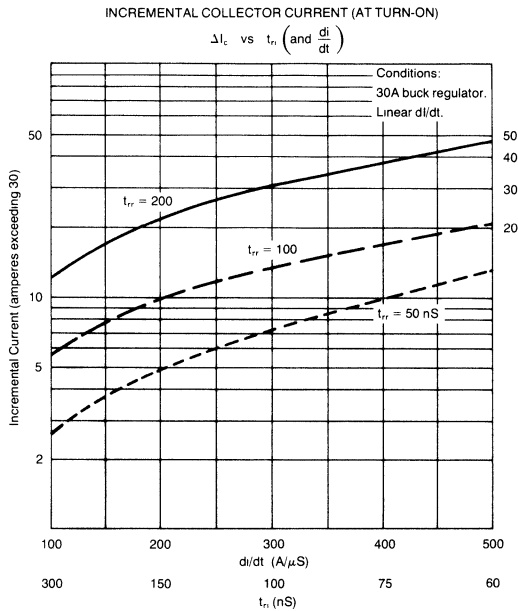
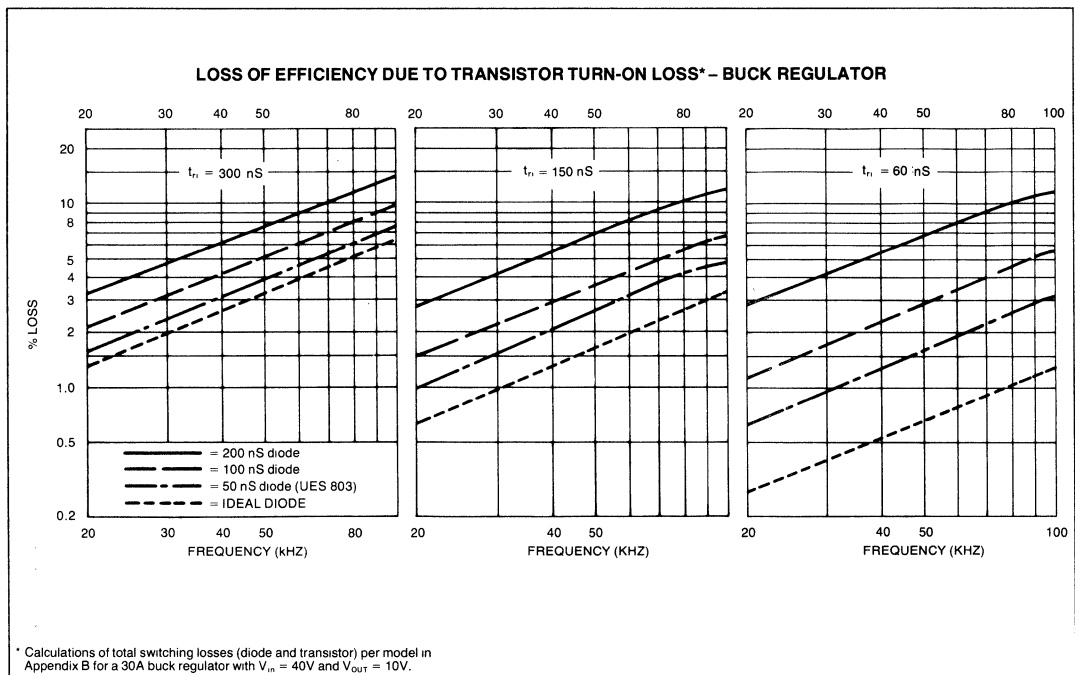


Figure 8



* Calculations of total switching losses (diode and transistor) per model in Appendix B for a 30A buck regulator with V_{in} = 40V and V_{out} = 10V.

Figure 9

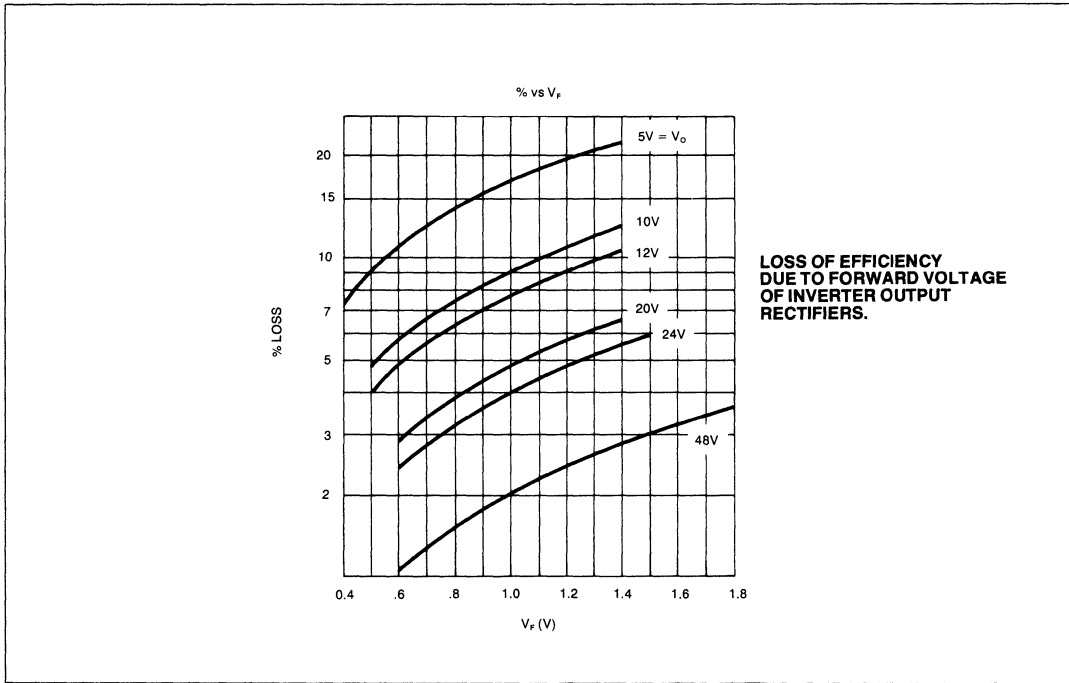


Figure 10

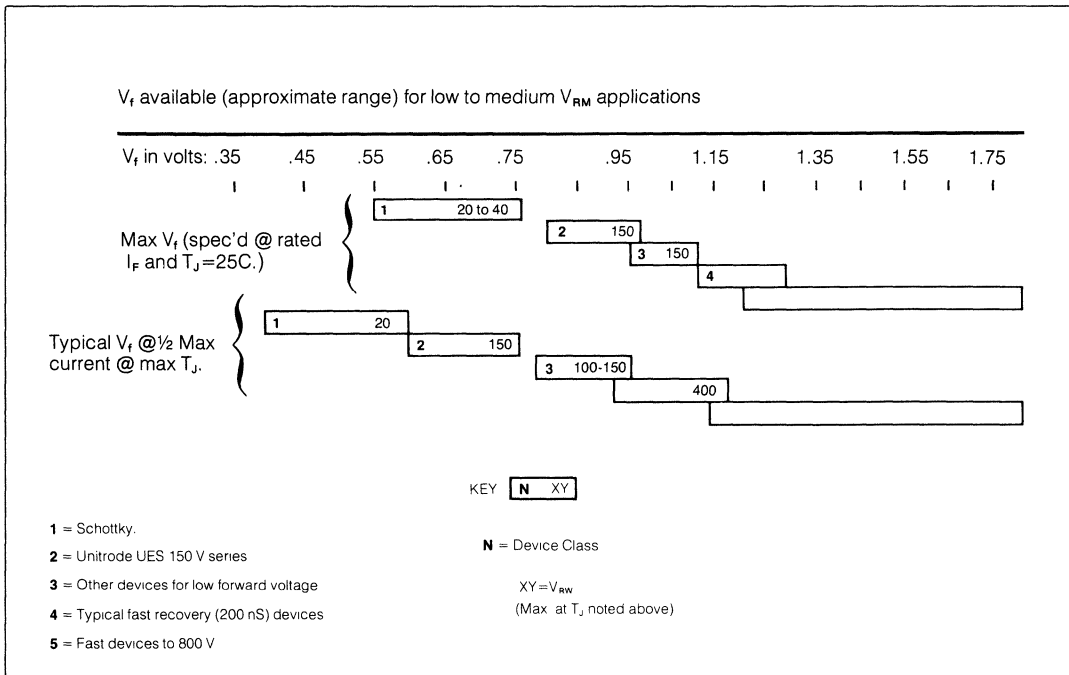
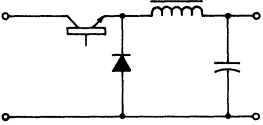
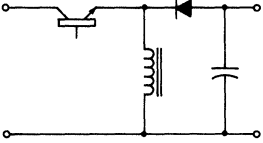
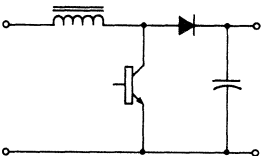
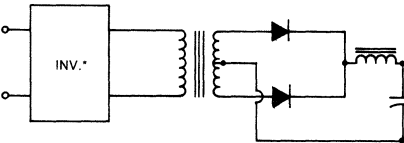
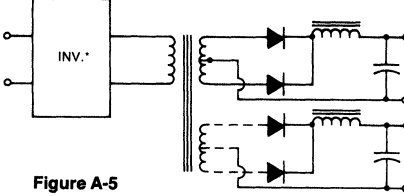


Figure 11

Appendix A "Off-Line" Supplies

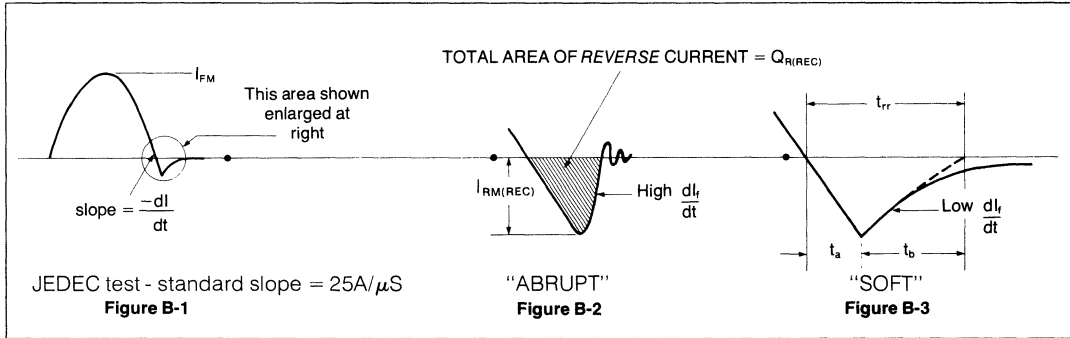
BASIC CIRCUIT	TYPE	FEATURES
<p>FROM RECTIFIED, OFF-LINE (OR OTHER D.C.) SOURCE</p>  <p>Figure A-1</p>	<p>a) Buck Regulator</p>	<p>$V_o < V_{in}$. Output non-isolated. Easy to filter output. Noisy input.</p>
 <p>Figure A-2</p>	<p>b) Flyback Regulator</p>	<p>V_o opposite polarity from V_{in}. (Unless isolated). Output can be isolated. Output can be stepped up to HV. Noisy input and output.</p>
 <p>Figure A-3</p>	<p>c) Boost Regulator</p>	<p>$V_o > V_{in}$. Output non-isolated. Hard to filter output. Quiet input.</p>
 <p>Figure A-4</p>	<p>d) PWM (Variable Duty Cycle) Inverter.</p>	<p>Used with single V_o, - also common for lab supplies. Provides isolation. Does not need separate catch diode, - rectifiers serve this function, possibly with small HV diodes in primary for magnetizing current.</p>
<p>INPUT FROM a, b, or c.</p>  <p>Figure A-5</p>	<p>e) Square Wave Inverter (50% Duty)</p>	<p>Regulation provided by previous input. Regulates one of (possible) multiple outputs. Uses high transistor count. Provides isolation. Does not need separate catch diode, - rectifiers serve this function, possibly with small HV diodes in primary for magnetizing current.</p>

(*) INV. = Bridge, center-tap, or half-bridge inverter.

Appendix B

Reverse Recovery Behavior and Dissipation

1. Waveforms and definition of terms:



2. Discussion of Variables:

Any PN junction diode operating in the forward direction contains stored charge in the form of excess minority carriers. The amount of stored charge is proportional to the forward current level.

The diode or rectifier in a switching regulator is switched from forward conduction to reverse at a specific ramp rate ($-di/dt$) determined by the external circuit, usually by the turn-on time of the associated switching transistor. During the first portion of the reverse recovery period, t_a , charge stored in the diode is able to provide more current than the circuit demands, so that the device appears to be a short circuit. Transition from t_a to t_b occurs when stored charge has been depleted to the point where it can no longer supply the increasing current demanded by the circuit. The device becomes a high impedance and during t_b the reverse voltage is permitted to increase. Reverse current, no longer circuit determined, dwindles as excess stored charge depletes to zero. Stored charge is depleted by the reverse current flow and also by recombination within the device.

At ($-di/dt$) rates which are slow relative to the rate of recombination of the specific device relatively little stored charge is swept out. Recovery time, t_{rr} is determined mainly by the recombination rate, independent of ($-di/dt$). Peak reverse recovery current $I_{RM(REC)}$, and total charge associated with reverse current, $Q_{R(REC)}$ are almost directly proportional to ($-di/dt$) (Region I, Figure B-4). The recovery characteristic with slow ($-di/dt$) rates tends to be soft.

When the ($-di/dt$) rate is fast compared to recombination rate (transistor turn-on faster than diode recovery time), t_{rr} decreases as $-di/dt$ increases, because more of the available stored charge is swept out sooner,

leaving little to be depleted by recombination. As ($-di/dt$) increases, peak recovery current increases and can become much greater than the original forward current level. However, $Q_{R(REC)}$ levels off as ($-di/dt$) increases because it can only approach but not exceed the total stored charge which is a function of the original forward current level (Region II, Figure B-4).

Higher voltage devices have poorer recovery characteristics because they require thicker regions of higher resistivity, resulting in greater volume of stored charge and longer recombination rates.

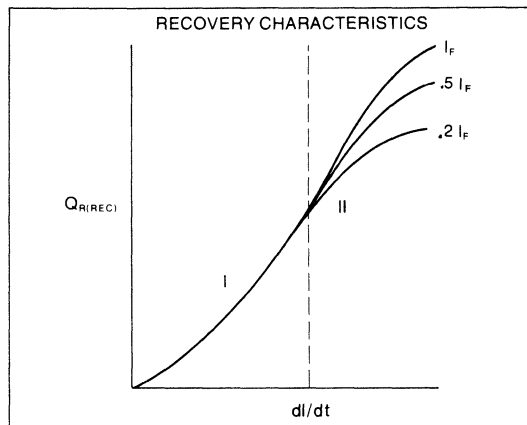


Figure B-4

With a given I_F and di/dt the $Q_{R(REC)}$, $I_{RM(REC)}$, and t_{rr} all increase with temperature. Recovery characteristic changes as well (generally becoming more abrupt if reverse current is not circuit limited, and softer if limited). Furthermore, $Q_{R(REC)}$ increases and recovery generally softens if higher circuit voltage is applied to a given diode.

3. Comparison of devices at popular test conditions:

Table I, below, shows measured t_{rr} values (in nanoseconds) using ultra-fast and fast recovery DO-5 rectifiers.

I_c (A)	I_m (A)	$-di/dt$ (A/ μ S)	T (°C)	$I_{RM(REC)}$ (t_{rr} Measured to (A))	UNITRODE UES803	MANUFACTURER			
						B	C	D	E
0.5	1.0	step	25	0.25	38	50	42	—	—
1.0	1.0	step	25	0.10	45	75	50	63	120
1.0	1.0	step	125	0.10	60	90	122	135	300
(85V JEDEC circuit)									
30	—	30	25	0	75	120	85	105	150
30	—	30	125	0	100	150	140	210	300
30	—	100	25	0	45	72	66	92	—
30	—	100	125	0	65	114	106	160	—
MAX t_{rr} per manufacturer's stated condition					50	50 to 100			200

Table I

4. Turn-on switching losses, assuming linear V and I transitions:

With an ideal diode, switching losses are entirely in the transistor as follows (from Eq. 2).

$$(B1) P_{(t_{ri})} = V_{in} \cdot \frac{I_c}{2} \cdot \frac{t_{ri}}{\tau}$$

$$(B2) P_{(t_{rv})} = \frac{V_{in}}{2} \cdot I_c \cdot \frac{t_{rv}}{\tau}$$

$$(B3) P_{(t_a)} = V_{in} \left(I_c + \frac{I_{RM(REC)}}{2} \right) \frac{t_a}{\tau}$$

$$(B4) t_a = t_{ri} \left(\frac{I_{RM(REC)}}{I_c} \right)$$

$$(B5) P_{(t_a)} = V_{in} \left(I_c + \frac{I_{RM(REC)}}{2} \right) \left(\frac{t_{ri}}{\tau} \cdot \frac{I_{RM(REC)}}{I_c} \right)$$

$$(B6) P_{(t_b)} = V_{in} \cdot I_{RM(REC)} \left(1 + \frac{I_{RM(REC)}}{2I_c} \right) \frac{t_{ri}}{\tau}$$

A practical diode with finite t_{rr} and $I_{RM(REC)}$ will cause *additional* switching losses as follows:

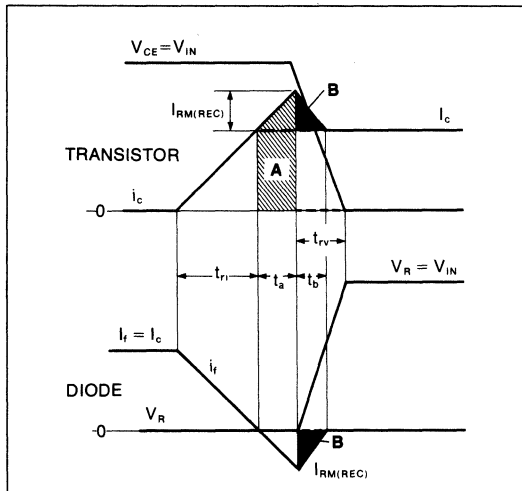


Figure B-5

Diode recovery time component t_a effectively increases transistor rise time, and delays the voltage transition, t_{rv} . During time t_a , the diode conducts reverse current but remains a low impedance. Transistor V_{CE} remains equal to V_{in} while collector current continues to rise above I_c to $I_c + I_{RM(REC)}$. The entire amount of charge shown in shaded area A results in increased switching loss in the *transistor only* (increase in diode loss is negligible):

If diode $I_{RM(REC)}$ is half of I_c (1.5:1 current overshoot in transistor) total transistor switching losses during current turn-on ($t_{ri} + t_a$) will be 2.25 times greater than with an ideal diode (Eq. B1).

During diode recovery time component t_b , the diode continues to conduct reverse current, but becomes a high impedance, permitting the transistor voltage transition, t_{rv} , to take place. Diode reverse current during t_b causes increased switching losses in the transistor and/or the diode. It is difficult to quantify these losses in the diode and transistor separately, since transistor V_{CE} is decreasing and diode V_R is increasing during all or part of period t_b . However, the total increase in losses in both diode and transistor during t_b is:

$$(B7) P_{(t_b)} = V_{in} \cdot \frac{I_{RM(REC)}}{2} \cdot \frac{t_b}{\tau}$$

$$\text{(area B)} = \frac{I_{RM(REC)}}{2} \cdot t_b$$

Note: $P_{(t_b)}$ loss is in *addition* to the ideal diode case transistor losses, $P_{(t_{rv})}$ (Eq. B2). With a very fast diode, t_b will be much shorter than t_{rv} , and most of the $P_{(t_b)}$ loss will occur in the transistor, although it will be negligible. With a slow diode, where t_b is much longer than t_{rv} , $P_{(t_b)}$ loss will be significant and will occur mostly in the diode.

$P_{(t_a)}$ is usually much greater than $P_{(t_b)}$. Since all of $P_{(t_a)}$ is dissipated in the transistor, it can be seen that most of the increased switching losses caused by diode reverse recovery are borne by the switching transistor, not by the rectifier.

Appendix C

Forward Recovery Behavior and Characterization

When used in some circuits, any diode may exhibit the phenomenon known as forward recovery. Under these conditions, the device has an impedance which, for a short time after initial application of forward current, is higher than its normal "on" value. The magnitude and duration of this transient impedance will depend on circuit conditions and device design, varying from no effect in many circuits to a few microseconds in the worst case. When present, the effect is generally less with fast-recovery rectifiers, and much less with "computer-type" switching diodes.

Circuits with very fast current rise time, in the direction of forward conduction, will allow this phenomenon to appear. Generally, these will be low-inductance circuits which allow the current to rise from zero to rated forward current in less than the reverse recovery time for fast stud-mounted rectifiers, and in less than $0.1 \times t_{rr}$ for lead mounted fast devices.

When such a source has a high voltage, of at least 10 times V_F , the forward recovery phenomenon exhibits an initial higher-than-steady-state forward voltage. The rise time of current is not limited by the diode and the

peak voltage decays to the specified measurement level in the "forward recovery time" t_{fr} . The peak voltage $V_{F(DYN)}$ will be strongly influenced by the current rise time di/dt , and current I_F .

When a fast-rise source has an open circuit (compliance) voltage of less than several times the diode V_F , the forward recovery phenomenon may exhibit a delay in the rise of forward current. In this case the peak diode voltage is limited by the source, and the "turn-on" time is the rise time to 90% of I_F .

A comparison of the Unitrode UES 803 with a typical 200 nS rectifier is shown in Table II below.

Test Condition	Unitrode UES 803		DO5 200 nS	
	$V_{F(DYN)}$ (v)	t_{fr} (nS)	$V_{F(DYN)}$ (v)	t_{fr} (nS)
I_F to 1A in 8 nS	1.2	20	12	300
I_F to 1A in 125nS and continuing to 50A with $t_r = 10\mu S$	0.9	—	2.8	350

Table II

FLYBACK AND BOOST SWITCHING REGULATOR DESIGN GUIDE

Section One — Flyback Regulator

I. Definition

The flyback switching regulator described in this application note accepts a DC voltage input and provides a regulated output voltage of opposite polarity. This method of conversion, compared to a conventional DC to DC converter, provides advantages of high efficiency, low cost, circuit simplicity, and a rather wide, easily selectable choice of the regulated output voltage. The switching transistor is not stressed to second breakdown in either the forward or reverse bias modes. Thus, it provides a reliable method of converting the input voltage. The disadvantage of the flyback switching regulator described here is that it provides no isolation and requires a large output filter capacitor. Primary usage of this type of regulator is in low current and/or high voltage applications.

II. Design Approaches to Flyback Regulator

The principal difference between a flyback regulator and a buck regulator (Ref. Unitorde Design Guide U-68) is the manner in which energy is transferred to the output capacitor. In a buck regulator, energy is provided continuously, while in a flyback regulator, energy is pumped in a discontinuous fashion. The flyback regulator can be operated in two modes.

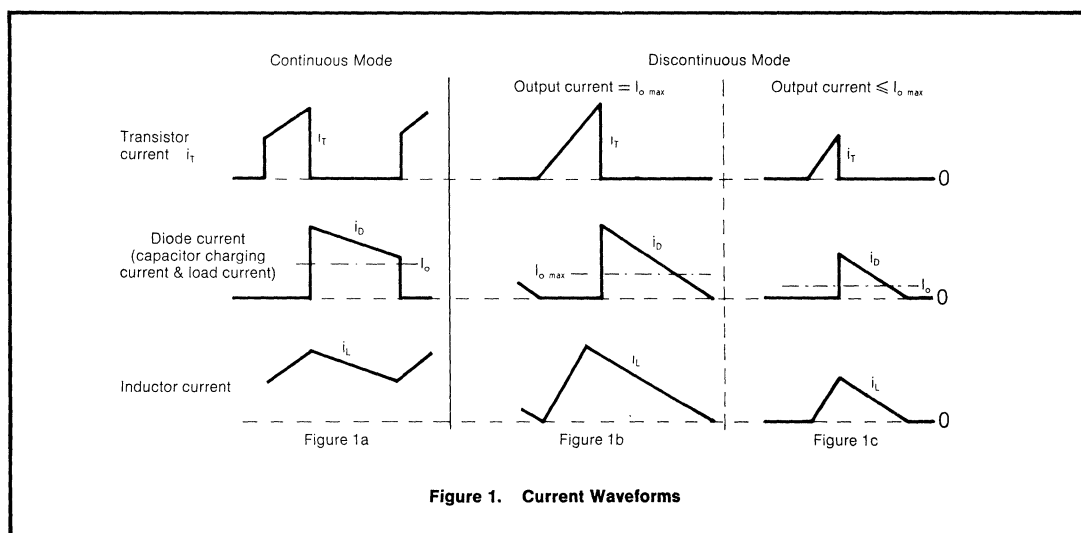
A. Continuous Mode (see Figure 1a)

In this mode of operation, a large inductor is required to insure that the inductor current never goes to zero. Although the current through the inductor flows continuously, the charging current to the filter capacitor is in the form of discontinuous current pulses. This large peak-to-peak current waveform requires a much larger filter capacitor than the buck regulator. Component cost is higher than with the discontinuous mode of operation because of the large inductance required, and transient response is worse.

B. Discontinuous Mode (see Figure 1b, 1c)

In this mode, the regulator is designed such that at maximum output load current and minimum input voltage, the transistor starts conducting as soon as the catch diode stops conducting. At a lower output current or higher input voltage there is a dead time when neither device conducts.

The output voltage can be regulated by varying the duty cycle of the transistor switch.



III. The Flyback Switching Regulator Described and Characterized

The basic circuit configuration and generalized current waveforms are shown in Figure 2. When transistor Q_1 is turned on, the supply voltage, E_{IN} , is applied across power inductor L . The current through the inductor rises linearly to a peak current level I_p :

$$I_p = \frac{E_{IN} \times t_r}{L} \dots \dots \dots A.$$

This results in an energy transfer from the input supply to the power inductor:

$$W = \frac{1}{2} L I_p^2 \dots \dots \dots B.$$

When the transistor turns off, a voltage is induced across inductor L which forces the current to flow through diode D_1 . All of the energy stored in the inductor is transferred to the output capacitor and load R_L , and the inductor current diminishes linearly from I_p to zero according to the relationship:

$$I_p = \frac{E_o \times t_b}{L} \dots \dots \dots C.$$

The power delivered to the load is equal to the peak energy stored in the inductor times the number of pump cycles per second:

$$P_{out} = E_o \times I_o = \frac{1}{2} L I_p^2 \times f \dots \dots \dots D.$$

The voltage induced in the inductor is such that E_o is opposite in polarity from E_{IN} . The relationship between E_o and E_{IN} is established by combining equations A and C, eliminating I_p and L :

$$\frac{E_o}{E_{IN}} = \frac{t_r}{t_b} \dots \dots \dots E.$$

DC output current I_o is equal to the average current through the diode:

$$I_o = \frac{I_p}{2} \times \frac{t_b}{\tau} = \frac{I_p}{2} \times t_b \times f$$

The output voltage can be regulated by operating at a fixed frequency and varying the transistor on time, t_r . However, because of the inherent "pumping" action of the flyback regulator, the output voltage diminishes while the switching transistor is on, and

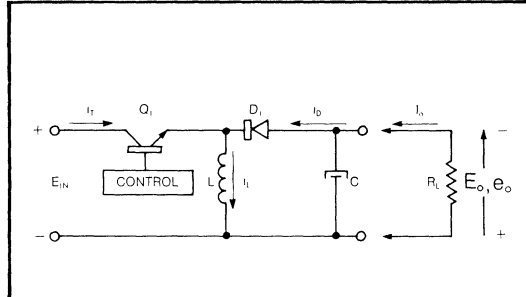


Figure 2a. Flyback Switching Regulator

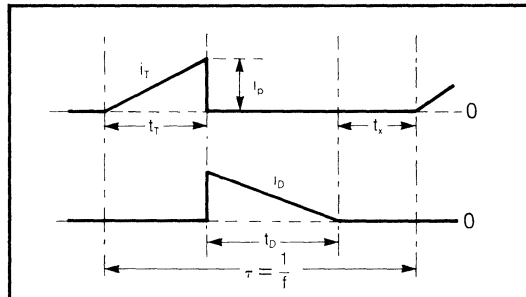


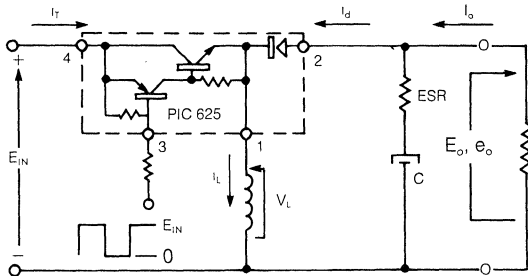
Figure 2b. Generalized Current Waveforms of a Flyback Switching Regulator

increases when the transistor is off. This characteristic makes it difficult to control on a fixed frequency basis.

The simplest approach to controlling the flyback regulator in the discontinuous mode is to establish a fixed peak current through the inductor, which determines a fixed diode conduction time, t_b . Frequency then varies directly with output current, and transistor on-time varies inversely with input voltage. This is the approach used in this application note, resulting in a simple and economical control circuit.

IV. Worst Case Design Conditions

Design equations based on the fixed peak current mode of operation are shown in Figure 3. The worst case condition exists when input voltage is low while output current is at maximum. Under these worst case conditions, frequency is maximum and t_r is zero because the pass transistor turns on as soon as diode stops conducting.

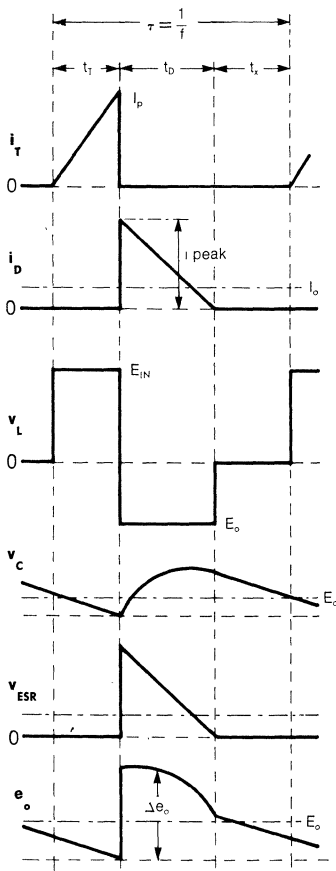


GIVEN:

- $E_{IN (min)}$
- E_o
- $I_o (max)$
- f_{max}
- Δe_o

WORST CASE:

- $E_{IN} = E_{IN (min)}$
- $I_o = I_o (max)$
- $t_s = 0$



$$I_p = 2 I_o (max) (E_o / E_{IN (min)} + 1) = \text{constant}$$

$$t_D = \frac{1}{f_{max} (E_o / E_{IN (min)} + 1)} = \text{constant}$$

$$L = \frac{t_D \times E_o}{I_p} = \frac{t_T \times E_{IN}}{I_p}$$

$$f = \frac{1}{T} = f_{max} \frac{I_o}{I_o (max)}$$

$$C_{min} = \frac{I_p \times t_D}{2 \Delta e_o}$$

(worst case $I_o \rightarrow 0$)

$$ESR_{max} = \frac{\Delta e_o}{I_p}$$

Figure 3. Flyback Regulator

V. Circuit Design and Description

In designing a flyback switching regulator power supply, the following parameters will normally be predefined. Numerical values are given and computed for the example shown in Figure 4.

- $E_o = 5V$ output
- $\Delta e_o = 100\text{ mV}$ output ripple voltage peak to peak
- $I_o\text{max} = 2.5A$
- $E_{IN\text{min}} = 9V$ (minimum)
- $E_{IN\text{max}} = 15V$ (maximum)

Since the output voltage is derived from pulses of

current, it is desirable to keep the operating frequency as high as possible in order to obtain small size and lower cost of the filter inductor and capacitor. However, above 5-10 kHz, capacitor impedance is usually dominated by its equivalent series resistance, ESR, rather than C value. Since the ESR remains essentially constant regardless of operating frequency, operation at higher frequencies does not enable the size and cost of the capacitor to be further reduced.

Also, at higher frequencies, transistor switching losses become significant. Thus, a maximum operating frequency of 25 kHz is chosen for this design.

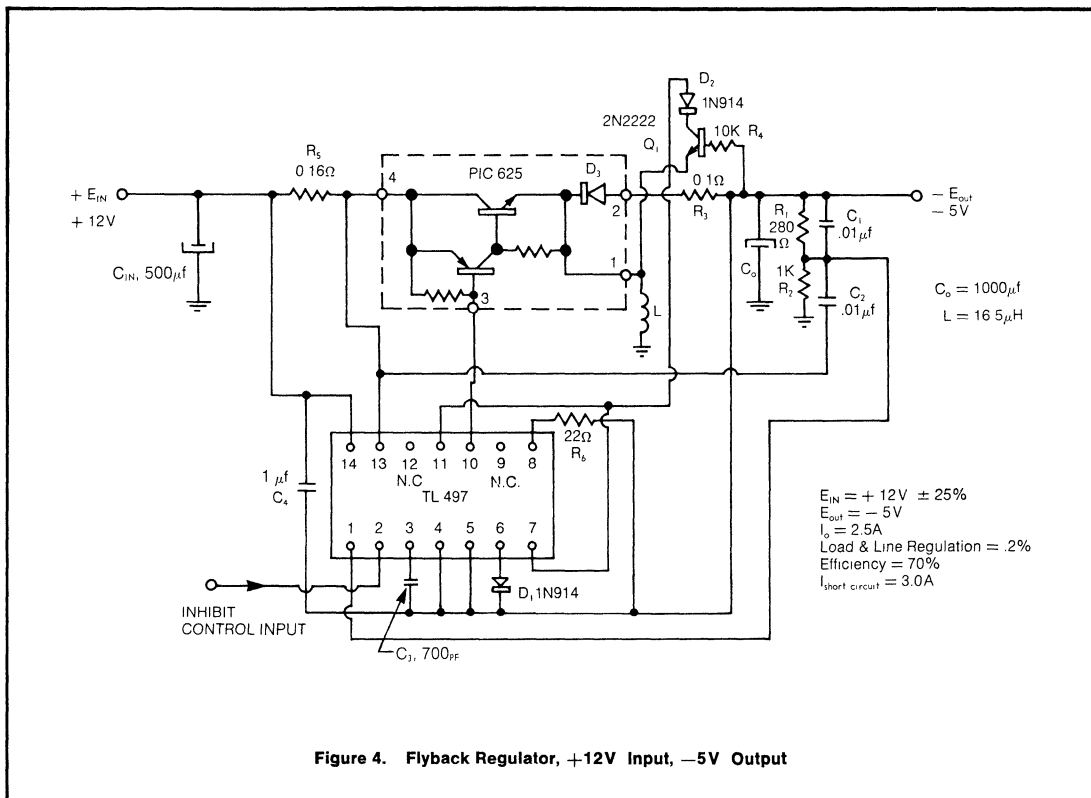


Figure 4. Flyback Regulator, +12V Input, -5V Output

Referring to Figure 3, the design calculations are:

$$I_p = 2 I_{o,max} (E_o/E_{INmin} + 1) = 2 \times 2.5 (5/9 + 1) \\ = 7.8A \text{ (constant)}$$

$$t_D = \frac{1}{f_{max} (E_o/E_{INmin} + 1)} = \frac{1}{25 \times 10^3 (5/9 + 1)} \\ = 25.7 \mu s \text{ (constant)}$$

$$L = \frac{t_D \times E_o}{I_p} = \frac{25.7 \times 10^{-6} \times 5}{7.8} \\ = 16.47 \mu H$$

$$C_{min} = \frac{I_p \times t_D}{2 \Delta e_o} = \frac{7.8 \times 25.7 \times 10^{-6}}{2 \times 0.1} \\ = 1002 \mu F$$

$$ESR_{max} = \frac{\Delta e_o}{I_p} = \frac{0.1}{7.8} = 0.0128 \Omega$$

The operating frequency will change in proportion to load current, I_o :

$$f = f_{max} \times \frac{I_o}{I_{o,max}}$$

The PIC625 hybrid power output stage incorporates a fast PNP quasi-darlington switching transistor and UES catch diode. The quasi-darlington switch requires 30 mA of drive current. This drive current is provided with diode D_1 and Resistor R_6 in conjunction with the Integrated circuit TL497. (Refer to Figure 4)

$$I_{DRIVE} = \frac{V_{DE}}{R_6} = \frac{0.65}{R_6} \\ \therefore R_6 = 22 \Omega$$

The output voltage is preset by divider network R_1 and R_2 , according to the relationship:

$$E_o = \left[1 + \frac{R_2}{R_1} \right] V_{REF}$$

where $V_{REF} = 1.22V$. Assuming a nominal value for $R_2 = 1K$, then:

$$R_1 = 320 \Omega$$

R_1 may be trimmed to obtain the precise output voltage.

The TL497 control circuit operates in the current limiting mode under normal operating condition. Thus, the peak current value, I_p , is determined by the current limiting resistor R_5 . Capacitor C_3 is required to prevent the TL497 from terminating the transistor on-time prematurely. This causes an $8 \mu s$ delay, once over-current is detected at the short circuit sense input (pin 13 of TL497) before the transistor switch turns off. The delay time is the time required to charge capacitor C_3 to the predetermined voltage level before drive current to the pass transistor is removed. The current limit threshold voltage is about 1.2 volts.

$$R_5 = \frac{1.2V}{I_p} \\ = \frac{1.2}{7.8A} \\ = 0.153 \Omega$$

The function of transistor Q_1 , diode D_3 and resistor R_3 and R_4 is to provide short circuit protection. The transistor Q_1 prevents turn-on of the pass transistor as long as the catch diode continues to conduct. Thus, it limits the maximum current and operating frequency under short circuit conditions. D_2 and R_4 providing voltage isolation to transistor Q_1 .

C_2 is required for circuit stabilization; capacitor C_1 provides AC coupling of ripple voltage to the control circuit. C_{IN} and C_o are filter capacitors.

Unitrode Switching Regulator Design Guide U-68 covers the design of a buck regulator, and contains a section on power inductor design which is applicable to the flyback and boost regulators.

Section Two – Boost Switching Regulator

The boost switching regulator is described briefly in this application note. It accepts a DC voltage input and provides a regulated output voltage which must be greater than input voltage.

The basic circuit configuration of a boost regulator is shown in Figure 5. When the transistor switch is turned on, the supply voltage E_{IN} is applied across power inductor L . The diode is reverse biased by voltage E_o . Energy is transferred from the input supply to the power inductor. When the transistor is turned off, the energy stored in the inductor L induces a voltage such that the diode conducts and transfers the energy to the load and the output capacitor. In addition to the energy stored in the inductor, additional energy is transferred from the input directly to the output during the diode conduction time.

This pumping action, similar to the flyback regulator, also makes it desirable to operate the boost regulator in the discontinuous mode with a fixed peak current through the inductor. However, unlike the flyback regulator, in the boost regulator the diode

conduction time is not fixed, but varies according to the input voltage:

$$t_b = \frac{L I_p}{E_o - E_{IN}}$$

Output voltage is regulated by controlling the duty cycle:

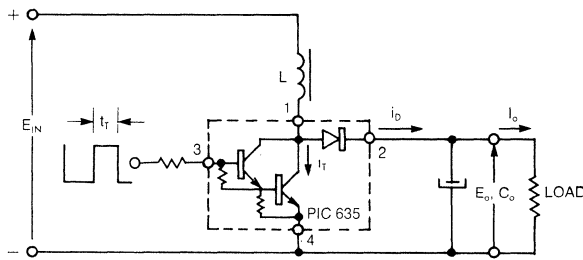
$$\frac{E_o}{E_{IN}} = \frac{t_t}{t_b} + 1$$

Since the ripple voltage across the output capacitor is directly proportional to diode conduction time, t_b , capacitor requirements are determined by the maximum t_b :

$$t_b \text{ max} = \frac{L I_p}{E_o - E_{IN}(\text{max})}$$

The Figure 6 is a complete schematic diagram of a boost switching regulator. It accepts +12V of DC input voltage and provides regulated +24V of output voltage.

The design procedure and circuit description is similar to the flyback switching regulator.

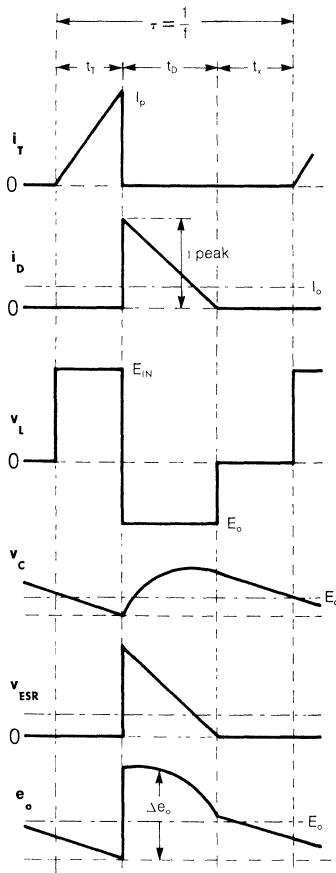


GIVEN:

- $E_{IN(max)}$
- $E_{IN(min)}$
- E_o
- $I_o(max)$
- $f_{(max)}$
- Δe_o

WORST CASE:

- $E_{IN} = E_{IN(min)}$
- $I_o = I_o(max)$
- $t_r = 0$



$$I_p = 2 I_o(max) (E_o/E_{IN(min)}) = \text{constant}$$

$$t_{D(min)} = \frac{1}{f_{max} (E_o/E_{IN(min)})}$$

$$L = \frac{t_{D(min)} (E_o - E_{IN(min)})}{I_p}$$

$$f = \frac{1}{\tau} = f_{max} \frac{I_o}{I_o(max)} \times \frac{E_o - E_{IN}}{E_o - E_{IN(min)}}$$

$$C_{min} = \frac{I_p \times t_{D(max)}}{2 \Delta e_o}$$

(worst case $I_o \rightarrow 0$)

$$ESR_{max} = \frac{\Delta e_o}{I_p}$$

Figure 5. Boost Regulator

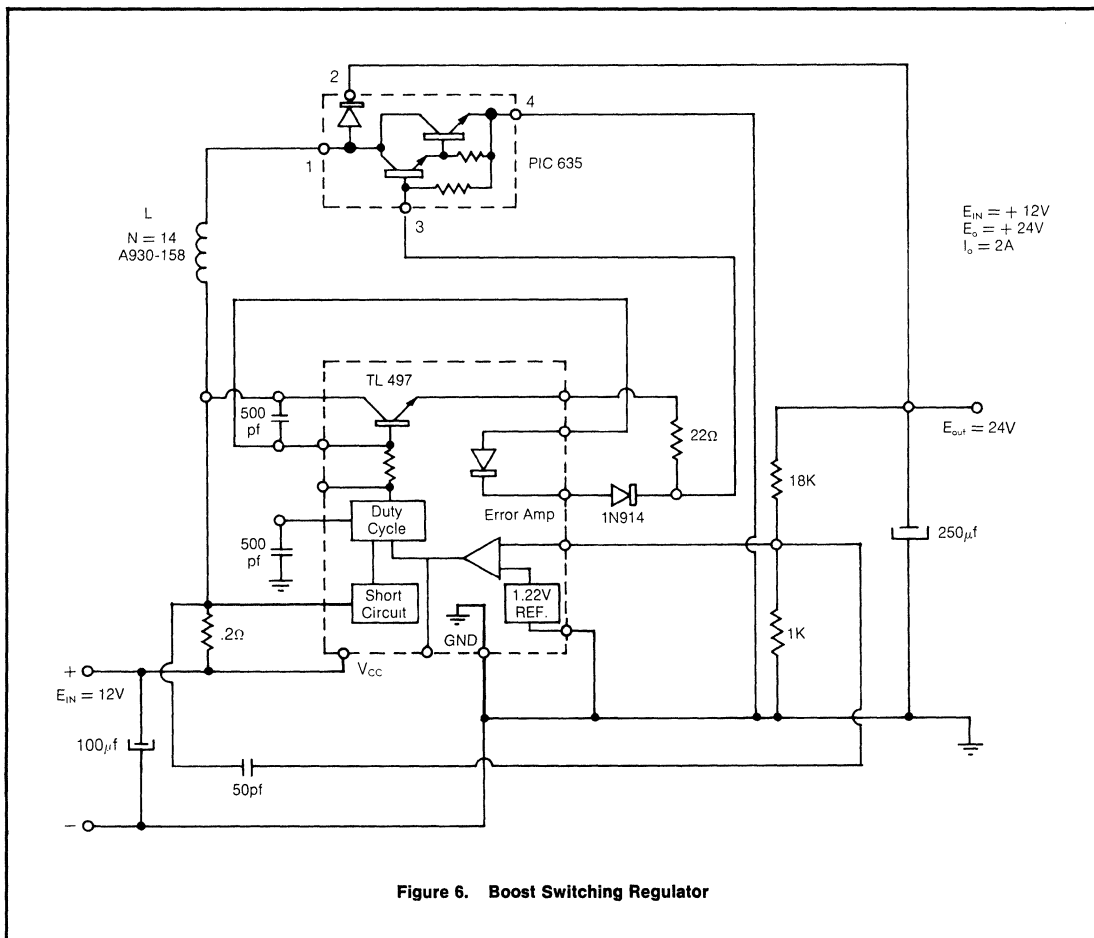


Figure 6. Boost Switching Regulator

Appendix A – Derivation of Design Equations

The basic circuit configuration of the flyback switching regulator is shown in Figure 3. Assuming a fixed value of peak current, I_p , and output volts, E_o , the following equations are evident:

$$E_{IN} t_T = E_o t_D = I_p \times L \dots\dots\dots 1.$$

$$t_T = t_D \times E_o / E_{IN} \dots\dots\dots 1a.$$

$$\tau = t_T + t_D + t_X = 1/f \dots\dots\dots 2.$$

Worst case $\tau = \tau_{min}$, $f = f_{max}$, $t_X = 0$, $E_{IN} = E_{IN min}$.
Substituting Equation 1a:

$$\tau_{min} = \frac{1}{f_{max}} = t_D (E_o / E_{IN min} + 1) \dots\dots\dots 2a.$$

$$\therefore t_D = \frac{1}{f_{max} (E_o / E_{IN min} + 1)} \dots\dots\dots 2b.$$

Since in Equation 1, E_o , I_p and L are all constant values for a given application, t_D is also a constant value.

By inspection of Figure 3 output current waveforms:

$$I_o = \frac{I_p}{2} \times \frac{t_D}{\tau} = \frac{I_p}{2} \times t_D \times f \dots\dots\dots 3.$$

Taking worst case conditions and substituting Equation 2b:

$$I_o max = \frac{I_p}{2} \times f_{max} \times \frac{1}{f_{max} (E_o / E_{IN max} + 1)} \dots\dots\dots 3a.$$

$$\therefore I_p = 2 I_o max (E_o / E_{IN max} + 1) \dots\dots\dots 3b.$$

Rearranging Equation 1:

$$L = \frac{t_D \times E_o}{I_p} \dots\dots\dots 1b.$$

The ripple voltage, Δv_c , across the output filter capacitor:

$$\Delta v_c = \frac{\Delta Q}{C} \dots\dots\dots 4.$$

The worst case net charge into the capacitor is equal to the area under the diode current waveform

$$\Delta Q_{max} = \frac{I_p \times t_D}{2} \dots\dots\dots 4a.$$

Substituting into Equation 4 and rearranging:

$$\therefore C_{min} = \frac{I_p \times t_D}{2 \Delta e_o} \dots\dots\dots 4b.$$

The ripple voltage, v_{ESR} across the capacitor series resistance, ESR.

$$v_{ESR} = I_p \times ESR \dots\dots\dots 5.$$

$$\therefore ESR_{max} = \frac{\Delta e_o}{I_p} \dots\dots\dots 5a.$$

The frequency, f , will vary as a function of load current. Rearranging Equation 3:

$$\frac{I_o}{f} = \frac{I_p}{2} \times t_D = I_o max / f_{max} \dots\dots\dots 6.$$

$$\therefore f = f_{max} \times \frac{I_o}{I_o max} \dots\dots\dots 6a.$$

and

$$f_{min} = f_{max} \times \frac{I_o min}{I_o max}$$

THERMAL DESIGN CONSIDERATIONS FOR OPERATING UNITRODE'S TO-92 TRANSISTORS AND DARLINGTONS IN PULSED-POWER APPLICATIONS

Introduction

Unitrode's power Darlington's (U2TA506, U2TA508, U2TA510, U2TA606, U2TA608, U2TA610) and power transistors (UPTA510, UPTA520, UPTA530 and UPTB520, UPTB530, UPTB540, UPTB550) in economical TO-92 plastic packages are ideally suited for use in pulsed power applications, such as lamp driving or printer driving where the inrush or pulse drive current can be as high as several amperes. When compared with transistors or Darlington's in conventional power packages, the Unitrode TO-92 devices offer cost savings of 50% or more, take up significantly less board space, and lend themselves to tape and reeling and automatic insertion. They also offer the advantage of a maximum operating junction temperature ($T_{J(max)}$) of 175°C versus 150°C or 125°C for other plastic packaged devices.

Thermal considerations are of prime concern when the TO-92 power transistors and Darlington's are used in pulsed power applications. This Design Guide provides a method for determining the junction temperature and maximum allowable peak power dissipation for the U2TA506, U2TA606 and the UPTA510 and UPTB520 series when they are operated at frequencies of 10kHz or less, where the switching losses are negligible and can be ignored. This method is valid for the vast majority of pulse applications.

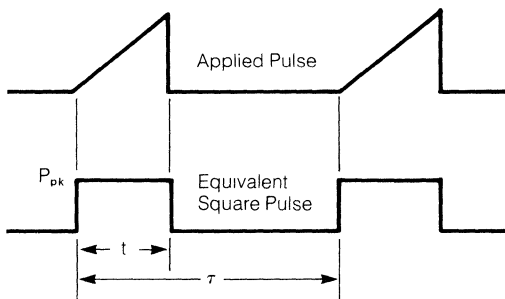
Thermal Analysis

A detailed transient thermal analysis is required to determine the peak junction temperature and maximum allowable power dissipation since the junctions of the transistor or Darlington are subjected to temperature excursions due to the applied, periodic power pulses.

A) Effective Pulsed Thermal Impedance

The effective pulsed thermal impedance (Θ_p) of a device subjected to a periodic train of power pulses can be calculated as follows:

$$\Theta_p = (\Theta_{j-A})(D) + (1-D)(r(t+\tau)) - r(\tau) + r(t) \dots \dots (1)$$



- Where: t = pulse width
- τ = period
- D = t/τ (Duty Cycle)
- $r(t+\tau)$ = transient thermal impedance at time $t + \tau$
- $r(t)$ = transient thermal impedance at time t
- Θ_{j-A} = DC junction to ambient thermal impedance
- P_{pk} = The peak power of a square power pulse with equivalent energy to that of the actual power pulse.

Figure 1. Power Pulses

The DC junction to ambient thermal impedance (Θ_{j-A}) is 200°C/W maximum for the UPTA510 and UPTB520 series and is 155°C/W maximum for the U2TA506 and U2TA606 series.

The transient thermal impedance for the U2TA506, U2TA606 and the UPTA510 and UPTB520 series can be obtained from the curves presented in Figure 2:

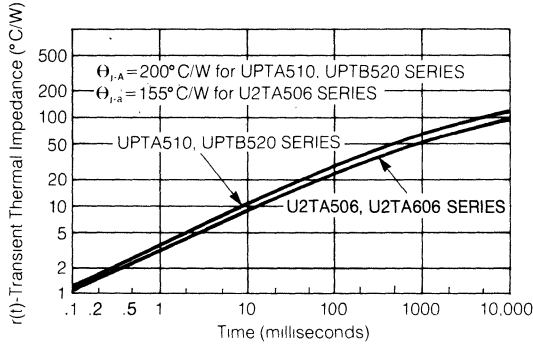


Figure 2. Junction to Ambient Transient Thermal Impedance

B) Peak Junction Temperature

The peak junction temperature of a device subjected to a periodic train of power pulses can be calculated using the previously derived effective pulsed thermal impedance as follows:

$$T_{j(\text{peak})} = T_{\text{Ambient}} + (P_{\text{pk}})(\Theta_p) \dots\dots\dots (2)$$

In the case of a single shot pulse the term for Θ_p reduces to $\Theta_p = r(t)$

and the equation used to calculate peak junction temperature becomes

$$T_{j(\text{peak})} = T_{\text{Ambient}} + (P_{\text{pk}})(r(t)) \dots\dots\dots (3)$$

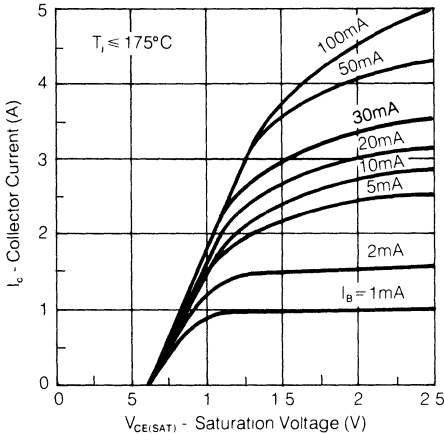


Figure 3. U2TA506 and U2TA606 Series. Maximum Saturation Voltage vs. Collector Current

Allowable Peak Power Dissipation

The allowable peak power dissipation can be derived from the following equation:

$$P_{\text{pk(max)}} = \frac{T_{j(\text{max})} - T_{\text{Ambient}}}{\Theta_p} \dots\dots\dots (4)$$

Where $T_{j(\text{max})}$ is the maximum allowable junction temperature. For the U2TA506, U2TA606, UPTA510 and UPTB520 series the maximum junction temperature is 175°C.

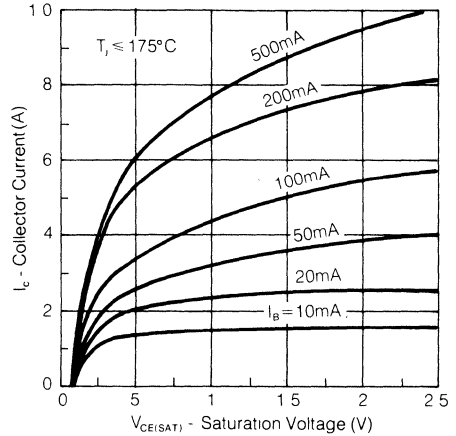


Figure 4. UPTA510 Series. Maximum Saturation Voltage vs. Collector Current

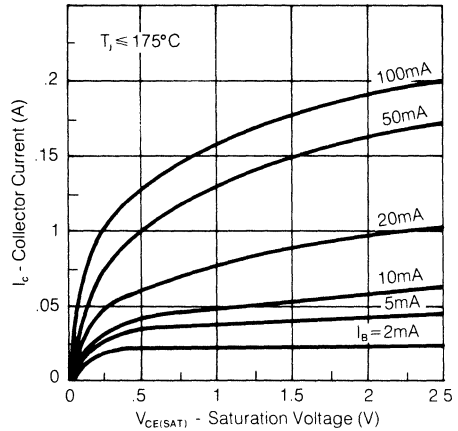


Figure 5. UPTB520 Series Maximum Saturation Voltage vs. Collector Current

Peak Power

The peak power can be expressed as follows:

$$P_{pk} = (V_{CE(SAT)})(I_{pk}) + (V_{BE(SAT)})(I_B) \dots \dots \dots (5)$$

Where I_{pk} is the peak collector current of a square pulse of current equivalent to the applied current pulse, $V_{CE(SAT)}$ is the transistor or Darlington saturation voltage at I_{pk} , $V_{BE(SAT)}$ is the base-to-emitter saturation voltage and I_B is the base current. Figures 3, 4, and 5 are plots of $V_{CE(SAT)}$ for the U2TA506, U2TA606, UPTA510 and UPTB520 series Darlington and transistors. Figures 6 and 7 are plots of the $V_{BE(SAT)}$. These curves can be used in determining P_{pk} .

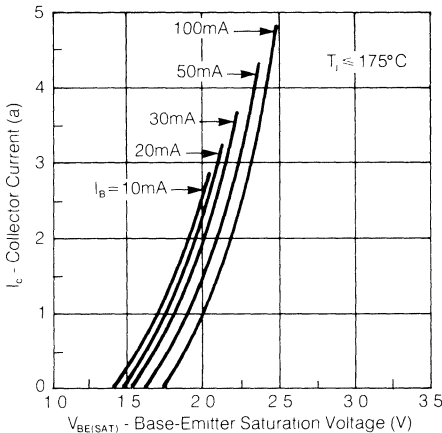


Figure 6. U2TA506 and U2TA606 Series Maximum Base to Emitter Saturation Voltage vs. Collector Current

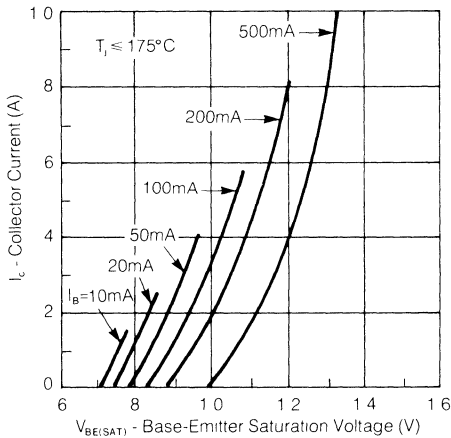


Figure 7. UPTA510, UPTB520 Series. Maximum Base to Emitter Saturation Voltage vs. Collector Current

Design Examples

1. An incandescent lamp is controlled by a U2TA506 Darlington operating from a 12V battery. When switched on the lamp draws an inrush current of 3A which decays exponentially to a steady-state value of 300mA. The time constant of the inrush current is 50 milliseconds and the worst case ambient temperature is 55°C. The Darlington's base drive is 30mA dc.

Problem:

Calculate the peak junction temperature due to the inrush pulse and the steady-state junction temperature.

Solution:

The inrush current can be approximated by a square wave of 3A peak and 50 milliseconds duration. The equivalent square pulse of current will have the same energy as the exponential pulse if the $V_{CE(SAT)}$ of the Darlington is assumed to remain constant. Since the $V_{CE(SAT)}$ will actually drop as the inrush current exponentially decays, the result obtained from using the square wave approximation will be conservative.

Using equations (3) and (5)

$$T_{j(peak)} = T_{Ambient} + (P_{pk})(r(t)) \dots \dots \dots (3)$$

Where: $T_{Ambient} = 55^\circ\text{C}$

$$r(t) = r(50\text{mSec}) = 17.5^\circ\text{C/W (from Figure 2)}$$

$$P_{pk} = (V_{CE(SAT)})(I_{pk}) + (V_{BE(SAT)})(I_B) \dots \dots \dots (5)$$

$$= (1.5\text{V})(3\text{A}) + (2.15\text{V})(30\text{mA})$$

(from Figures 3 and 6)

$$= 4.56\text{W}$$

Therefore:

$$T_{j(peak)} = 55^\circ\text{C} + (4.56\text{W})(17.5^\circ\text{C/W}) = 135^\circ\text{C}$$

Since 135°C is 40°C less than the maximum operating junction temperature for the U2TA506 ($T_{j(max)} = 175^\circ\text{C}$), the Darlington is operating well within its rating.

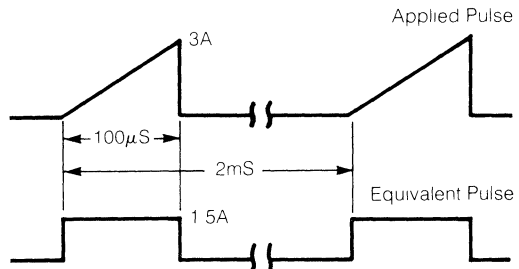
The Steady-state junction temperature can be determined as follows:

$$T_{j(ss)} = (P_{(ss)})(\Theta_{j-A}) + T_{Ambient}$$

$$= ((.3\text{A})(73\text{V}) + (.03\text{A})(1.60\text{V}))(155^\circ\text{C/W}) + 55^\circ\text{C}$$

$$= 96^\circ\text{C}$$

2. A U2TA508 is used to drive a solenoid load in an impact printer. The collector current waveform is as shown below along with the equivalent square pulse:



15

The Darlington is switching in a clamped mode so the energy stored in the solenoid inductance during the on-time is dissipated in the clamp and not in the Darlington. The maximum ambient temperature is 80°C and the base drive current is 20mA.

Problem:

Find the worst case junction temperature and determine if it is within the maximum rating of the U2TA608.

Solution:

Use equation (1) to determine Θ_p

$$\Theta_p = (\Theta_{JA})(D) + (1-D)(r(t+\tau)) - r(\tau) + r(t) \dots\dots\dots(1)$$

$\Theta_{JA} = 155^\circ\text{C/W}$ (from Figure 2)

$$D = \frac{.1\text{mSec}}{2\text{mSec}} = .05$$

$$r(t+\tau) = r(2.1\text{mSec}) = 4.2^\circ\text{C/W}$$
 (from Figure 2)

$$r(\tau) = r(2\text{mSec}) = 4.1^\circ\text{C/W}$$
 (from Figure 2)

$$r(t) = r(.1\text{mSec}) = 1.1^\circ\text{C/W}$$
 (from Figure 2)

Therefore:

$$\begin{aligned} \Theta_p &= (155^\circ\text{C/W})(.05) + (.95)(4.2^\circ\text{C/W}) - 4.1^\circ\text{C/W} \\ &\quad + 1.1^\circ\text{C/W} \\ &= 8.75^\circ\text{C/W} \end{aligned}$$

Using equation (5)

$$P_{pk} = (V_{CE(SAT)})(I_{pk}) + (V_{BE(SAT)})(I_b) \dots\dots\dots(5)$$

$$I_{pk} = 1.5\text{A}$$

$$V_{CE(SAT)} = 2\text{V}$$
 (from Figure 3)

(The $V_{CE(SAT)}$ value at 3A was chosen to give a conservative answer. If T_j is found to be greater than 175°C it may be necessary to recompute using a closer approximation of the actual $V_{CE(SAT)}$ which varies as the current increases from 0 to 3A.)

$$I_b = 20\text{mA}$$

$$V_{BE(SAT)} = 2.1\text{V}$$
 (from Figure 6)

(Again the $V_{BE(SAT)}$ value at 3A was chosen to give a conservative result.)

Therefore:

$$P_{pk} = (2\text{V})(1.5\text{A}) + (2.1\text{V})(.02\text{A}) = 3.04\text{W}$$

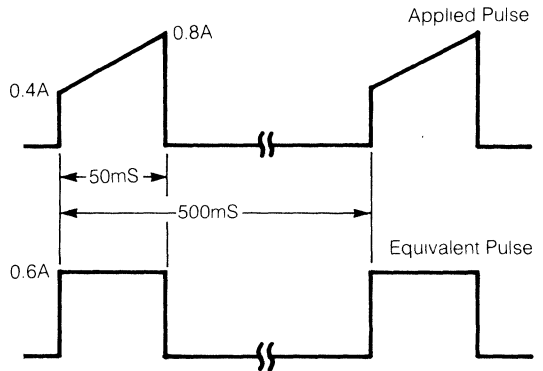
Now T_j can be determined from equation (2)

$$T_j = T_{\text{ambient}} + (P_{pk})(\Theta_p) \dots\dots\dots(2)$$

$$= 80^\circ\text{C} + (3.04\text{W})(8.75^\circ\text{C/W}) = 107^\circ\text{C}$$

This is well within the maximum rating of 175°C for the U2TA608.

3. A UPTA530 is used to drive a high voltage DC motor in a display application the current waveform as is shown below:



The base drive is 200 mA and the worst case ambient temperature is 65°C.

Problem:

Determine the junction temperature to insure it is within the maximum rating of 175°C for the UPTA530.

Solution:

Using Equation (1)

$$\begin{aligned} \Theta_p &= (200^\circ\text{C/W})(.1) + (.9)(52^\circ\text{C/W}) - 50^\circ\text{C/W} + 21^\circ\text{C/W} \\ &= 37.8^\circ\text{C/W} \end{aligned}$$

From equation (5) and Figures 4 and 7.

$$P_{pk} = (2.3\text{V})(.6\text{A}) + (1.2\text{V})(.2\text{A}) = 1.6\text{W}$$

(Again $V_{CE(SAT)}$ and $V_{BE(SAT)}$ values at .8A rather than .6A were used to insure a conservative answer).

Therefore, from equation (2)

$$T_j = 65^\circ\text{C} + (1.6\text{W})(37.8^\circ\text{C/W}) = 126^\circ\text{C}$$

It becomes readily apparent from these examples that Unitrode's TO-92 transistors and Darlington's can be operated with significant safety margin in a wide variety of pulsed-power applications.

GUIDELINES FOR USING TRANSIENT VOLTAGE SUPPRESSORS

1.0 Introduction

During transient periods, system voltages and currents are often many times greater than their steady-state values. These transients must be considered in overall electronic systems design to insure required circuit performance and reliability both during and after the transient.

Transients may result from a variety of causes. The most common of these are: normal switching operations (power supply turn-on and turn-off cycles), routine AC line fluctuations, or abrupt circuit disturbances (faults, load switching, voltage dips, magnetic coupling by electro-mechanical devices, lightning surges, etc.). Voltage transients are a major cause of component failures in semiconductors. Random high voltage transient spikes can permanently damage these voltage sensitive devices and disrupt proper system operation. Catastrophic power supply conditions should not necessarily be the designer's prime concern, since lower level transients can cause improper operation of a system even though no component failures are caused. Normal power supply on-off cycles have the potential of emitting spikes with sufficient energy to destroy an entire semiconductor device chain. Any surviving devices are also suspect. Trouble shooting, isolating, and replacing damaged devices is time consuming and costly; especially when performed in the field.

Unitrode's TVS305 and TVS505 series of transient voltage suppressors (TVS) offer the designer significant price/performance advantages over other protection methods. Their miniature size permits simple "close-in" installation in applications where circuit boards are dispersed throughout one or more electronic racks. Dispersed usage aids system trouble shooting and affords transient voltage protection where internal system disturbances such as those caused by inductive load switching could occur.

In spite of their small size, the TVS305 and TVS505 suppressor series can dissipate 500 watts and 150 watts (respectively) of peak pulse power for 1 millisecond. Response time to transients is just about instantaneous — about 1×10^{-12} seconds. These devices perform to their data sheet specifications without significant degradation throughout their

operating life. Unitrode has performed full power pulse life tests for 100,000 pulses with negligible change in characteristics. These devices are suitable for almost any equipment and environment.

2.0 Choosing the Correct Transient Voltage Suppressor for the Application

Certain critical terms must be defined before any discussion of "how to" choose the correct TVS.

1. Stand-Off Voltage (V_R) is the highest reverse voltage at which the TVS will be non-conducting.
2. Min. Breakdown Voltage (BV_{min}) is the reverse voltage at which the TVS conducts 1 mA. This is the point where the TVS becomes a low impedance path for the transient.
3. Max. Clamping Voltage (V_{Cmax}) is the maximum voltage drop across the TVS while it is subjected to the peak pulse current, usually for 1mS.

Figure 1 graphically shows all three terms.

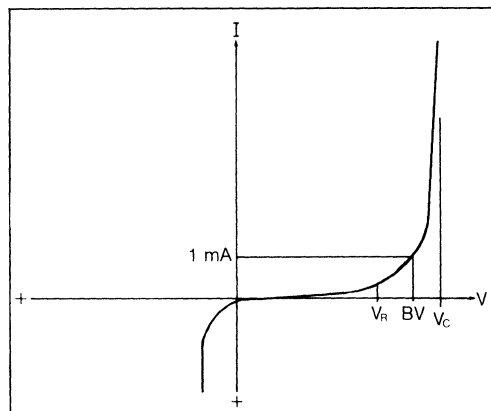


Figure 1 — TVS Characteristics

2.1 Determining Pulse Power Levels

Since a zener TVS has an almost constant clamping voltage throughout a transient pulse, the transient pulse power (P_p) equals the peak pulse current (I_{pp}) multiplied by the clamping voltage (V_c).

$$P_p = V_c \times I_{pp}$$

2.2 Choosing the Appropriate Transient Voltage Suppressor

The three most important factors in choosing the appropriate TVS for your application, in their order of importance are:

1. Pulse power (P_p) — Choose the TVS series that will handle the Transient Pulse Power. To determine Transient Pulse Power use the simple equation in section 2.1. If I_{pp} is not known or measurable, it can be calculated — see Sections 3 and 4. The pulse duration vs. pulse power graph on the Unitorde TVS305/TVS505 data sheet can then be used to determine the TVS series that will handle the transient. This graph for the TVS505 series is shown in Figure 2.

2. Stand-off voltage (V_R) — From the TVS series selected, choose the device with the stand-off voltage equal to or greater than your normal circuit operating voltage. This insures that the TVS will draw a negligible amount of current from the circuit during normal circuit operation. The electrical specifications for the TVS505 series are shown in Figure 3.
3. Maximum Clamping Voltage (V_{Cmax}) — Determine the clamping voltage of the device chosen for the transient given and be sure it is below the voltage that might damage any components in the protected circuit. See Figure 3.

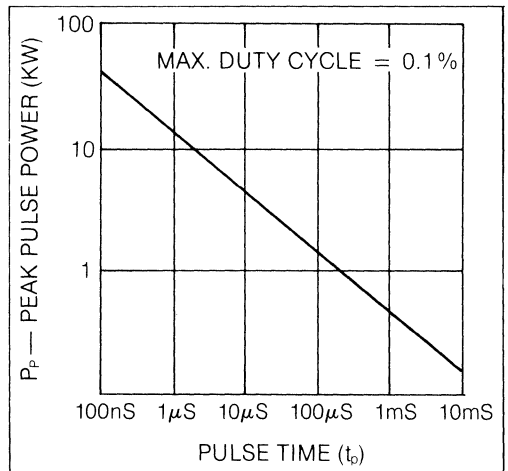


Figure 2 — Peak Pulse Power vs. Pulse Duration

TVS Part No.	Stand-off Voltage V_R	Min. Breakdown Voltage $BV_{(min)} @ 1mA$	Max. Leakage Current $I_R @ V_R$	Max. Clamping Voltage $V_C @ 1A$	Max. Clamping Voltage $V_C @$		Max. Peak Pulse Current I_{pp}	Max. Clamping Voltage $V_C @ I_{pp}$
					5A	10A		
	V	V	μA	V	V		A	V
TVS505	5.0	6.0	300	7.4		7.9	53.7	9.3
TVS510	10.0	11.1	5	13.2		14.4	30.3	16.5
TVS512	12.0	13.8	5	16.5		18.5	23.8	21.0
TVS515	15.0	16.7	5	19.7		22.2	19.8	25.2
TVS518	18.0	20.4	5	23.8	26.0		16.3	30.5
TVS524	24.0	28.4	5	32.4	37.0		11.9	42.0
TVS528	28.0	30.7	5	35.9	41.0		10.7	46.5

Figure 3 — Electrical Specifications @ 25°C

If the actual pulse power and pulse width are different from those listed on the data sheet, the clamping voltage can be calculated. The actual calculation method is beyond the scope of this note. Instead, we offer a graphical approximation using Figure 4. The approximation is based on the ratio of the actual and rated pulse power.

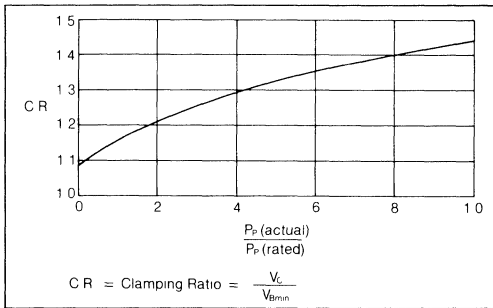


Figure 4 — Graphical Approximation for the Clamping Ratio

The procedure is as follows:

- a. Calculate P_p (actual) $\approx 1.3BV_{min} I_{pp}$.
- b. For P_p (rated) use value from TVS data sheet curve (See Fig. 2 for example).
- c. Calculate P_p (actual)/ P_p (rated).
- d. Use Fig. 4 to find corresponding value of C.R.
- e. Calculate $V_c = C.R. \times BV_{min}$.

2.3 Installation Considerations

1. Locate the TVS as close to the device or circuit to be protected as possible.
2. Minimize the "common path" through the TVS to minimize voltage spikes produced by fast risetime transients in lead and wiring stray inductance. See Figure 5.

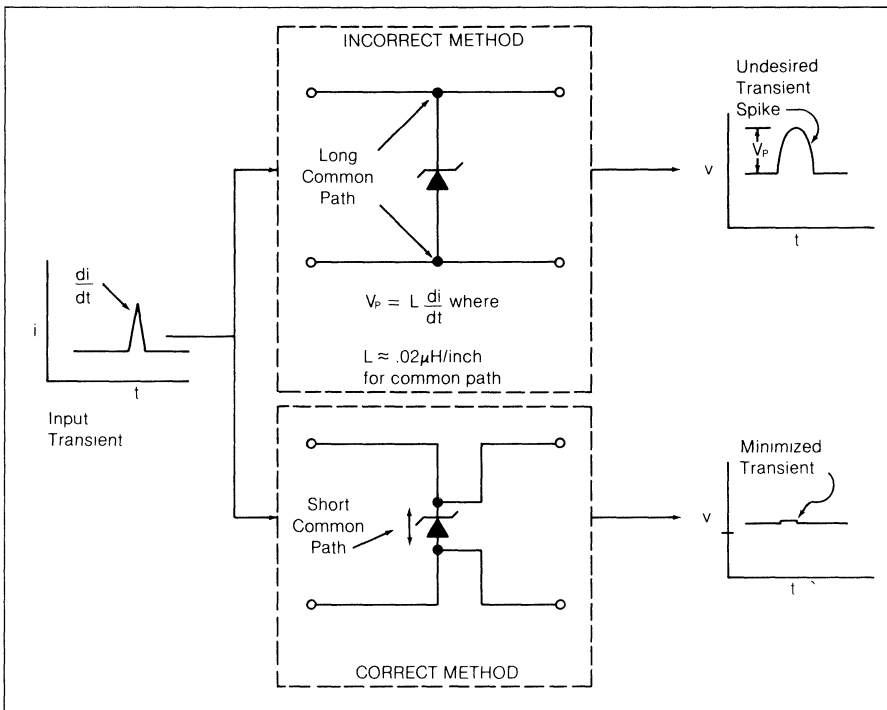


Figure 5 — Minimizing the Common Path

3.0 Transient Levels and Waveforms

3.1 Voltage, Current and Power Levels

Since TVS tests and specs may be written in terms of voltage, current or power levels, the relationships are shown in Figure 6 for (a) field conditions and (b) test conditions.

In addition to the magnitude of the voltage, current or power, the waveform or pulse width should be specified, as shown in Figure 7, for example.

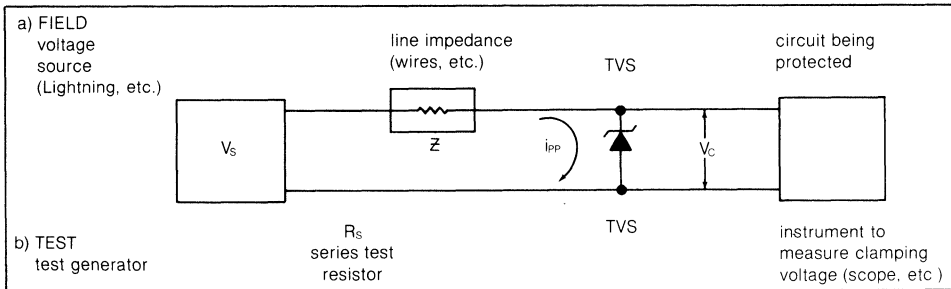


Figure 6 — Equivalent Circuit for Field and Test Conditions

3.2 Typical Transient Levels

Martzloff and Hahn in their paper on transients on 120 volt power lines* produced this table showing the surges recorded at a number of different locations

over a two year period. The table indicates two primary causes of transients; load switching within the house and lightning storms.

Table 1*
Detailed Analysis of Recorded Surges

House	Most Severe Surge			Most Frequent Surge			Average Surges per Hour	Remarks
	Type†	Crest (volts)	Duration (μs or cycles)	1.5mHz Type†	Crest (volts)	Duration (μs or cycles)		
1	A-1.5	700	10 μs	A-1.5	300	10 μs	0.07	fluorescent light switching
2	A-2.0	750	20 μs	A-2.0	500	20 μs	0.14	
3	B-0.5	600	1 cycle	B-0.5	300	1 cycle	0.05	
4	B-0.5	400	2 cycles	B-0.5	300	2 cycles	0.2	10 total
5	C	640	5 μs	too few to show typical				
6	B-0.3	400	1 cycle	B-0.3	250	1 cycle	0.01	lightning storm
7	B-1	1800	1 cycle	B-1.0	800	1 cycle	0.03	
8	C	1200	10 μs	B-0.5	300	4 cycles	0.1	oil burner
9	B-0.25	1500	1 cycle	same as most severe			0.2	
10	B-0.25	2500	1 cycle	B-0.25	2000	1 cycle	0.4	oil burner
11	B-0.2	1500	1 cycle	same as most severe			0.15	water pump
12	B-0.2	1700	1 cycle	B-0.2	1400	1 cycle	0.06	oil burner
13	B-0.1	350	1 cycle	too few to show typical			4 total	house next to 12
14	C	800	15 μs	—	—	—	1 total	lightning
15	B-0.25	800	3 cycles	B-0.25	600	3 cycles	0.05	rural area
16	B-0.15	400	15 μs	B-0.13	200	30 μs	0.4	surges
Street pole	B-0.5	5600	4 cycles	B-0.3	1000	1 cycle	0.1	lightning stroke nearby
Hospital	C	2700	9 μs	C	900	5 μs	0.1	lightning storm
Hospital	B-0.3	1100	1 cycle	too few to show typical			4 total	
Dept store	B-0.5	300	1 cycle	B-0.5	300	1 cycle	0.5	
Street pole	B-0.2	1400	4 cycles	B-0.2	600	4 cycles	0.07	lightning storm

*Reprinted from *Surge Voltages in Residential and Industrial Power Circuits* by Francois D. Martzloff, Member, IEEE, and Gerald J. Hahn. Reprinted by permission from *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-89, No. 6, July/August 1970, pp. 1049-1056. Copyright 1970, by the Institute of Electrical and Electronics Engineers, Inc. Printed in U.S.A.

3.3 Commonly Used Test Waveforms

1. The $10 \times 1000\mu\text{S}$ Test Waveform used by many TVS manufacturers, also by incoming inspection departments of users, represents some commonly encountered transients. (See Figure 7).
2. The IEEE Standard (ANSI C 37.90a — 1974) for surge withstand capability. (See Figure 8).

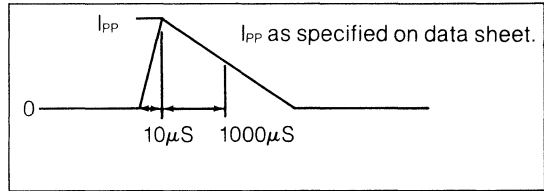


Figure 7 — Commonly Used Test Waveform

3.4 Surge Testing

Figure 9 shows a typical test set used to produce an exponentially decaying current pulse of 1mS to 50% down. ($10 \times 1000\mu\text{S}$). The 1mS waveform is used by many manufacturers to test and characterize their TVS devices for pulse power and clamping voltage.

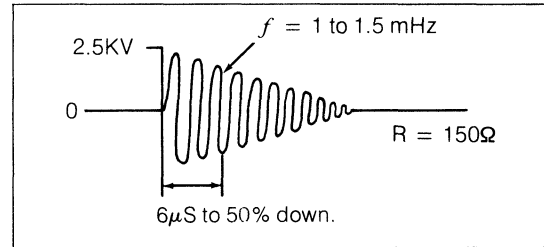


Figure 8 — More Complex Standard Waveform

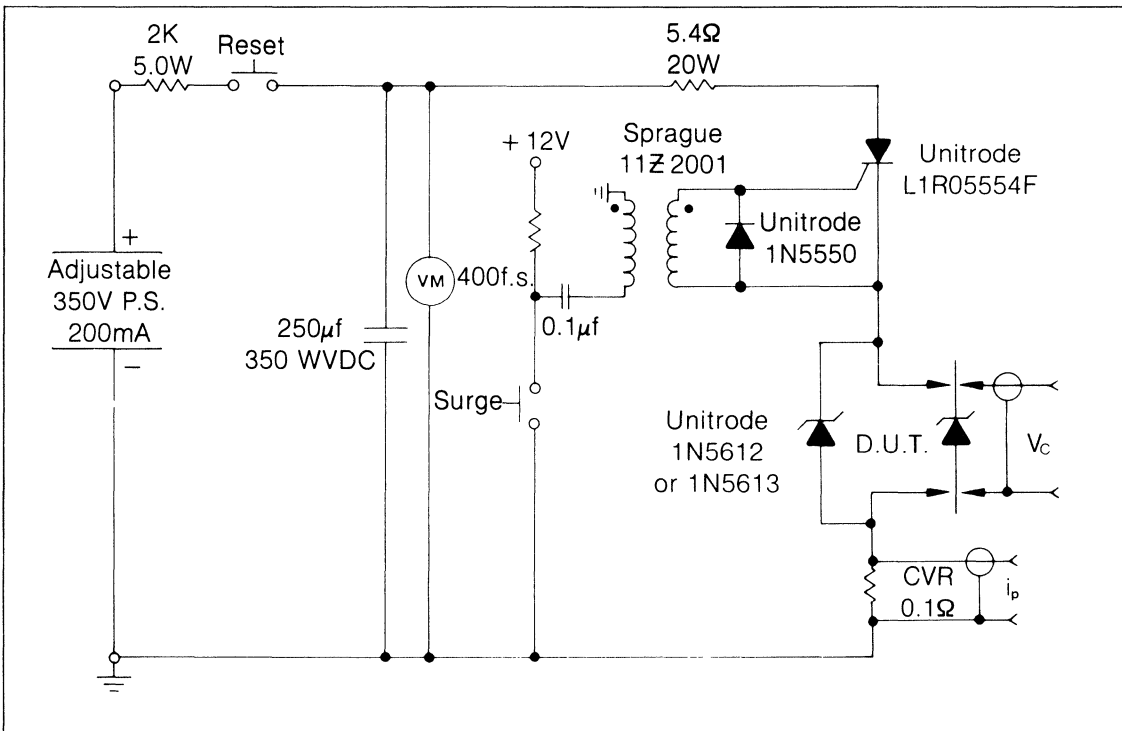


Figure 9 — Suggested Set-up for Surge Testing

4.0 Examples

4.1 Relay and Solenoid Applications

When the energy stored in the coil inductance of a relay or solenoid is released it can damage contacts or drive transistors. It can also produce EMI interference. A TVS used as shown in Figure 10 will provide reliable operation.

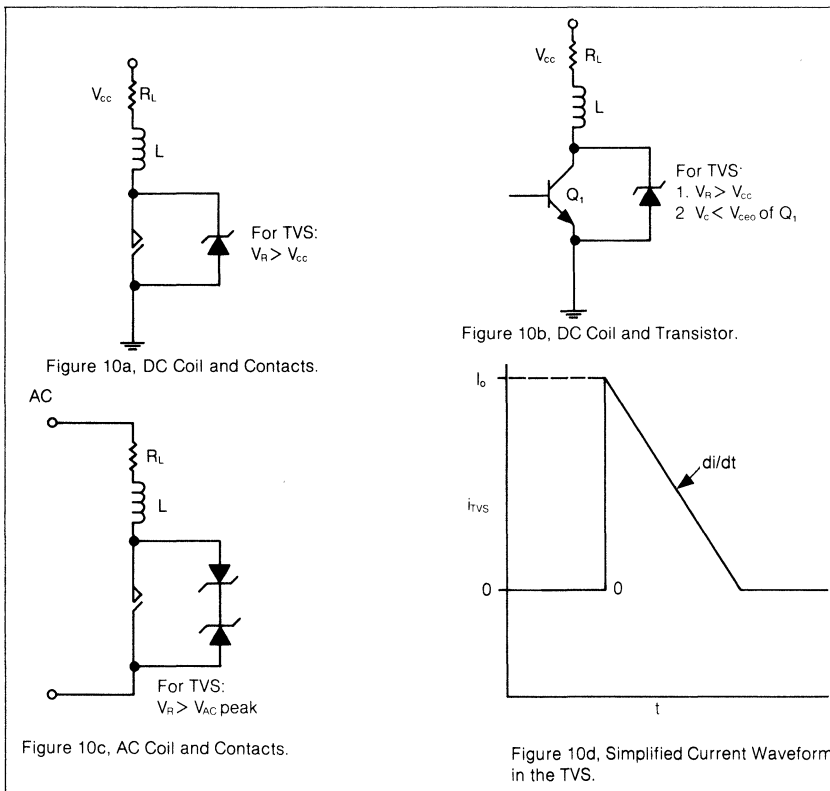
Just before the switch opens, the initial inductor current $I_0 = \frac{V_{cc}}{R_L}$.

This is the worst case (maximum) current and assumes the switch was closed long enough for the circuit to reach steady-state.

After the contacts switch at $t = 0$, $e = -L \frac{di}{dt}$, and when using a TVS the change in coil current, $\frac{di}{dt} = \frac{V_c}{L}$. Referring to Figure 10d, $t_1 = \frac{I_0}{di/dt} = \frac{V_{cc}/R_L}{V_c/L} = \frac{V_{cc}L}{R_L V_c}$. Note that the higher the V_c of the TVS, the shorter the current decay time.

In order to select the proper TVS, determine:

1. Peak pulse power $P_p = I_p \times V_c$, where $I_p = I_0$.
2. Pulse time t_p (@ 50% down point of i_{TVS}) = $\frac{t_1}{2}$.
3. These values of P_p and t_p are used with graphs of pulse power vs. pulse duration provided on the TVS305 and TVS505 data sheet to select proper device. See example in Figure 2.



NOTE: In some cases, because of accessibility, the TVS must be located across the coil; in that case a diode should be used in series with the TVS, connected back to back as shown in Figure 11.

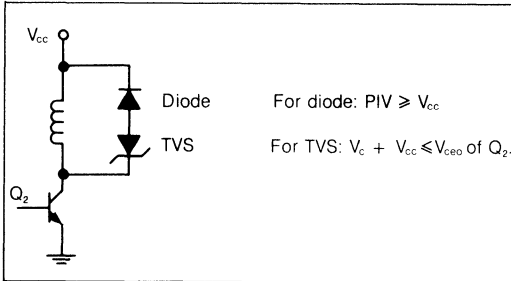


Figure 11 — Using TVS Across Coil

Sample Calculations:

For example, using the circuit of Figure 10a, and sample values of:

$$V_{cc} = 14V, L = 1mH, \text{ and } R_L = 2\Omega;$$

For $V_{cc} = 14V$, the next higher V_{R1} is 15V. (Note that $V_c = 22.2V$ at 10A).

$$\text{STEP 1: } I_o = \frac{V_{cc}}{R_L} = \frac{14V}{2\Omega} = 7A$$

$$P_p = I_o \times V_c = 7.0A \times 22.2V = 155W$$

$$\text{STEP 2: } t_1 = \frac{V_{cc}/R_L}{V_c/L} = \frac{14/2}{22.2/10^{-3}} = 0.32mS$$

$$\text{so } t_p = \frac{0.32mS}{2} = 0.16mS = 160\mu S$$

STEP 3: From Figure 2, P_{pmax} for $t_p = 160\mu S$ is 1200W, which is well above the circuit value of 155W.

4.2 Protecting Switching Power Supplies

The designer needs to protect against:

1. Load transients
2. Line transients
3. Internally generated transients including those produced by internal faults or failures.

Transients can produce failures because of their own high energy level; and also they can cause improper operation and component failure.

Figure 12 shows a simplified schematic of a typical switching power supply.

Referring to Figure 12, the TVS devices shown protect the following circuit components:

1. the rectifiers.
2. the HV switching transistors.
3. the output rectifiers.
4. the control circuitry.

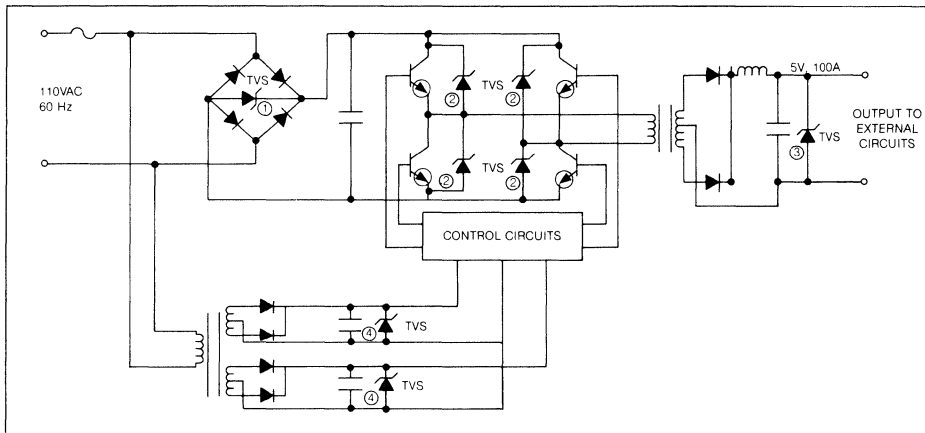


Figure 12 — Typical Switching Power Supply

4.3 Protecting Microprocessor Based Systems

While most microprocessor and IC semiconductor manufacturers design some form of diode-resistive input clamping network on the chip itself, transient voltage protection offered is very minimal — on the order of a few watts of pulse power. Manufacturers are also reluctant to make device performance and reliability claims when power supply operation

extends beyond the maximum rated level of the individual device for even relatively short durations such as those that may be encountered during on-off transitions. Therefore, there is a need for some external protective device to suppress voltage transients, as shown in Figure 13.

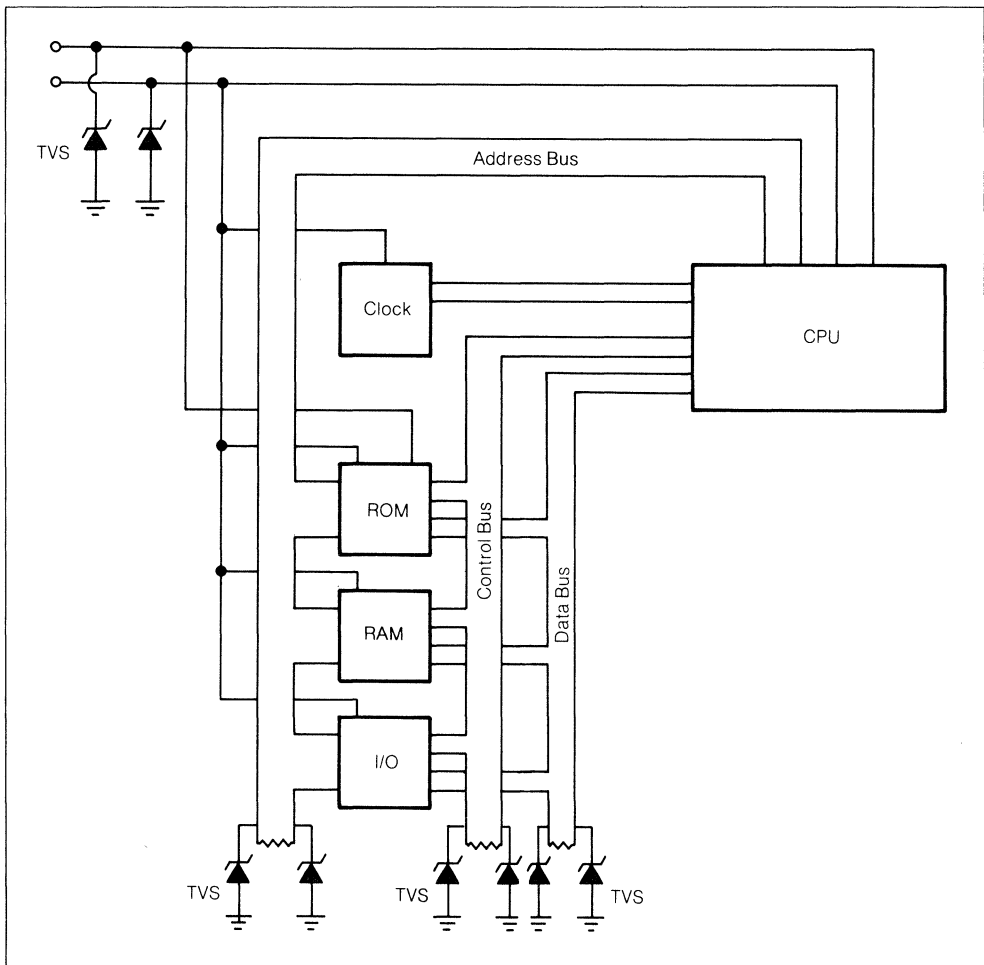


Figure 13 — Protecting Microprocessors

5.0 Alternative Protection Devices

Other protective devices such as MOVs, spark gaps, and crowbars have one common disadvantage when compared to zener TVS products; the response time is from nanoseconds to as much as tens of microseconds as compared to 1 pS for an avalanche zener diode. Even 50nS is long enough to allow a transient to destroy the small junctions used in most integrated circuits, logic, fast transistors, etc.

In circuits where transient pulses are fairly common, device degradation becomes a significant problem.

TVS products do not significantly degrade even after 100,000 transients.

In many cases, the zener TVS and one of the alternative devices can complement each other. For example, when used with an SCR crowbar, the zener TVS will keep the voltage during a transient to an acceptable level until the crowbar, which may take 10 μ S to short the line, can protect the load circuits, and in the case of a heavy transient protect the smaller TVS as well.

DETECTING IMPENDING CORE SATURATION IN SWITCHED-MODE POWER CONVERTERS

ABSTRACT

A new low cost concept termed "mismatched flux" has been developed which not only prevents impending saturation of the core but also provides symmetrical switching current in power switches in Pulse Width Modulation switched-mode converters except at low flux density. The detecting signal is obtained by mismatching the flux in the outer legs of an E-E core configuration.

INTRODUCTION

Opposite polarity power pulses are applied to the power transformer in a PWM converter to transfer power from the primary to the secondary windings. The volt-second integral of these pulses averaged over one or more cycles should be zero to avoid any problems with transformer core saturation.

In practice, however, imbalance occurs due to non-ideal characteristics of power switches, mainly the switching times (including storage and delay times) and saturation voltage. Even though the imbalance in the pulse width of the drive current provided by a PWM control circuit is very small compared to power switches, it can drive the core into saturation.

Core saturation in PWM switched-mode converters can cause problems such as secondary breakdown in switching transistors, excessive voltage and current stress on the rectifiers, and EMI problems.

The unique circuit described in this paper develops voltages proportional to the flux density in the core. When the maximum flux densities at the end of the positive and negative cycles in the core are not the same, unequal voltages are produced during the positive and negative cycles. These voltages are fed back to the PWM control circuit which adjusts the widths of its output pulses until the amplitudes of these two voltages are equal.

This technique, which can be applied in push-pull converters as well as bridge type converters, prevents core saturation and provides symmetrical primary current during the positive and negative cycles. It allows the most efficient use of the power transformer. In a buck type regulator, the current limiting function can be performed with this same technique.

THE UNBALANCED PWM CONVERTER

Figure 1 shows the typical push-pull converter and its associated current and voltage waveforms. Due to the difference in switching times and $V_{CE(SAT)}$ of transistors Q_1 and Q_2 , the transformer core is driven into saturation. The volt-seconds applied by

transistor Q_2 is higher than Q_1 as shown in Figure 1d, even though the secondary current is the same during on-times of transistors Q_1 and Q_2 .

Three important observations can be made from these figures:

1. Information concerning the magnitude of the imbalance of the flux can be derived by examining the current in the rectifier diodes (Figures 1e and 1f) during the dead-band period.
2. The slopes of the primary currents when Q_1 and Q_2 are conducting are not the same.
3. The familiar equation $I_{C1}/I_{D1}=N_2/N_1$ is not applicable when the flux density in the transformer is not symmetrical during the positive and negative half-cycle.

Under normal operating conditions and during dead-band period, the path for the current flowing in the output inductor L is provided by diodes D_1 and D_2 . The inductor current is divided between these two diodes. The magnetizing current I_{MS} flows in the entire secondary winding. Note that the magnitude of I_{MS} remains the same during the entire dead-band period because the voltage across the secondary winding is zero. The overall result is that one diode conducts more current than the other diode. The current flowing in these diodes is:

$$i_{D1} = \frac{i_L}{2} + I_{MS} \quad \text{Current in Rectifier Diode } D_1 \quad (1)$$

$$i_{D2} = \frac{i_L}{2} - I_{MS} \quad \text{Current in Rectifier Diode } D_2 \quad (2)$$

Subtracting i_{D1} from i_{D2} and rearranging

$$I_{MS} = \frac{i_{D1} - i_{D2}}{2} \quad (3)$$

Thus, the current flowing in diode D_1 and D_2 allows us to determine the exact amount of imbalance in the flux density during the positive and negative half-cycles. Figure 1g, which is calculated from diode current D_1 and D_2 , shows the operating flux density of a core in only the 1st quadrant of a B-H curve.

When transistor Q_1 or Q_2 turns on, this magnetizing current is reflected back into the primary winding according to the equation:

$$I_{PM} = \frac{2(N_2)}{N_1} I_{MS} \quad (4)$$

The dotted line in Figures 1c and 1d shows the reflected current in the primary winding. Since the flux density is not symmetrical around zero in the B-H curve, the collector current in Transistor Q₁ is lower than in Transistor Q₂. When the magnetizing current (dotted line in Figure 1c) is added to the actual measured collector current (solid line) in Transistor Q₁, it will produce a linear slope compared to the rounded slope of the measured collector current. The equation

$$\frac{I'_{c1}}{I_{D1}} = \frac{N_2}{N_1} \quad (5)$$

will hold true, where I'c₁ is equal to the magnetizing current reflected into the primary winding plus the actual measured collector current I_{c1}. Similarly, when Transistor Q₂ turns on, the transformer transfers energy from the input power source to the secondary. Some energy is also stored in the core due to the unsymmetrical flux density in the core. The magnetizing current (current level above dotted line in Figure 1d) is subtracted from the measured collector current.

The equation

$$\frac{I'_{c2}}{I_{D2}} = \frac{N_2}{N_1} \quad (6)$$

will hold true, where I_{c2} is equal to the actual measured collector current minus the magnetizing current reflected into the primary winding.

The imbalance in volt-seconds causes the flux density to drift towards one side of the hysteresis loop. This causes an imbalance in the collector currents of the transistor switches. The imbalance in volt-seconds will be compensated, to some extent, by an adjustment in the collector currents of the two transistor switches. As the collector current decreases the storage time increases and V_{CE(SAT)} decreases as shown in Figures 2 and 3. This effectively increases the volt-seconds. The I_R drop in the primary winding also helps to balance the volt-seconds in the transformer. These collector currents will vary until the proper volt-second balance is obtained in the transformer. If no corrective scheme is provided to balance current in the switch, the following disadvantages are present:

1. The required current ratings of the transistors and rectifiers must be increased.
2. The V_{CE(SAT)} losses will be increased. Furthermore switching losses will be even higher, especially in high voltage power converters.

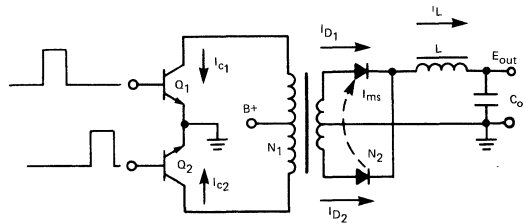


Figure 1a.

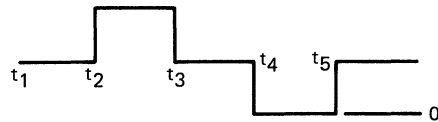


Figure 1b. Voltage Waveform at Collector of Q₂.

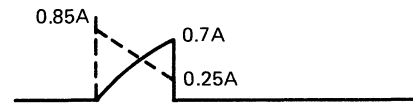


Figure 1c. I_{c1} Current Flowing in Transistor Q₁.

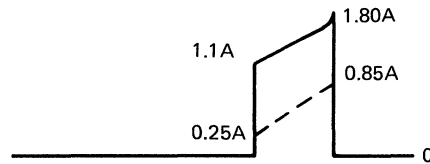


Figure 1d. I_{c2} Current Flowing in Transistor Q₂.

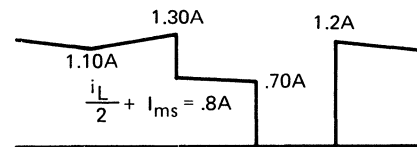


Figure 1e. Load Current in I_{D1}.

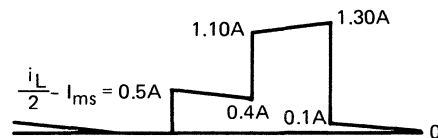


Figure 1f. Load Current in I_{D2}.

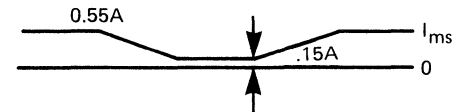


Figure 1g. Magnetizing Current in Secondary.

Figure 1. Gallery of Waveforms of a Push Pull P.W.M. Switching Regulator

3. Losses in the core increase as a function of the square of the maximum operating flux density. As the core temperature goes up, the losses in the core also increase, thus, the potential exists for thermal runaway in the core.
4. The leakage inductance is proportional to the maximum operating flux density. The imbalance causes high leakage inductance, and excess voltage stress across the transistor and rectifier.
5. If the core goes into saturation, it creates excessive current in the power switches, can result in forward bias second breakdown, clamped reverse bias second breakdown, and increased radiated and conducted EMI.

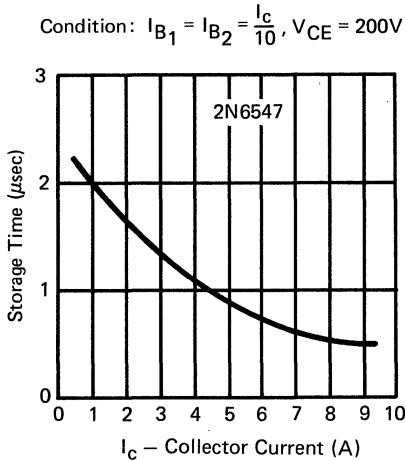


Figure 2. Storage Time vs Collector Current

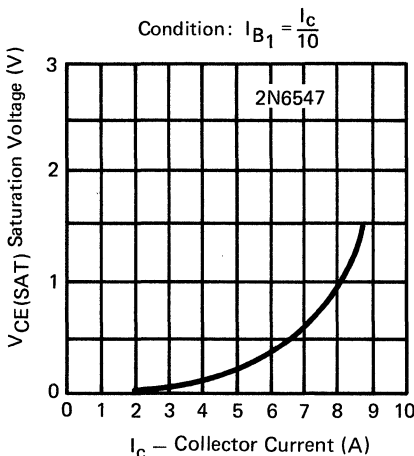


Figure 3. $V_{CE(SAT)}$ vs Collector Current

BASIC PRINCIPLE

An air gap in the E-E core can be used to prevent core saturation in PWM converters. The air gap reduces residual flux density in a square loop transformer and prevents core saturation during the start-up condition. However when there is a volt-second imbalance, the air gap does not prevent core saturation.

If the air gap is placed in only one of the outer legs of an E-E or EC core configuration, as shown in Figure 4a, then it allows a means of detecting core saturation, and by using this signal, to provide symmetrical flux swing in the core.

The primary winding and secondary winding are placed in the center leg of the E-E core, while the auxiliary winding is placed in the outer leg which contains the air gap.

The peak output voltage of the auxiliary winding is detected with Diode D_1 , D_2 and Capacitor C_1 . The Resistor R_1 in parallel with Capacitor C_1 provides the reset for another cycle by discharging the capacitor. The voltage developed across R_1 and C_1 is proportional to the maximum rate of change in flux at the instant when the transistor switch turns on.

The total amount of flux passing through the outer leg with the air gap is inversely proportional to the magnetic length of the opposite side of the leg. As the flux density in the center leg increases, a larger and larger area of the core at the point where the two E cores meet on the opposite side of the leg will become saturated. Note that only the edge of the core will saturate, while the rest of the core (leg with no air gap) will not saturate. As it saturates further, the reluctance of this leg increases, thus its effective magnetic length increases. This phenomenon forces more flux into the leg which has the air gap.

The voltage developed in the auxiliary winding is expressed by Faraday's Law:

$$V = N \left[\frac{d\Phi_2}{dt} \right] \times 10^{-8} \quad (7)$$

Where N is the number of turns. Thus the magnitude of developed voltage will depend upon the rate of change in flux with respect to time. Since the air gap is in only one leg of the E-E core, the term $|d\Phi_2/dt|$ changes continuously and depends upon the flux density in the center leg. Thus the output voltage from the auxiliary winding also varies with respect to time.

The same results can be obtained with using a core as shown in Figure 4b. The advantage of using this core is that the leakage inductance will be less compared with the previous technique.

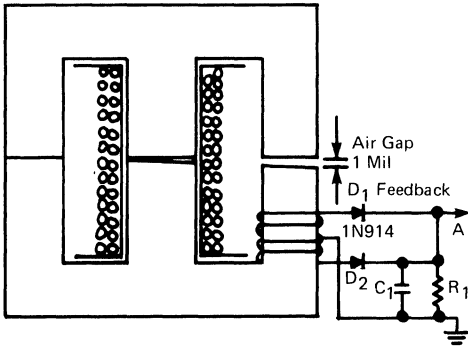


Figure 4a. Air Gap in Only One Leg of E-E Core

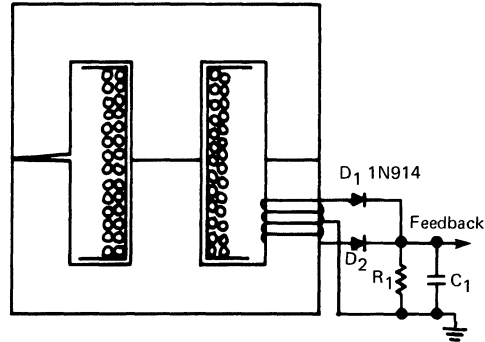


Figure 4b. Tapered Air Gap in One of the Outer Legs of the E-E Core

Figure 5 shows the B-H curve (solid line) of an E-E core with an air gap in only one leg. It lies between the E-E core with an equal air gap in both sides of the outer legs and a core with no air gap. From this figure it is obvious that $|d\Phi/dt|$ changes with the flux density and is a non linear function. Figure 6 shows variation in inductance with magneto-motive forces.

be accomplished by gating the output voltage of the auxiliary winding with a pulse width of a few microseconds.

Figures 7 through 9 show the voltage developed in the auxiliary winding at different values of the magnetizing current. The magnetizing current is directly proportional to the maximum flux level for a given transformer. In these waveforms the initial flux density is set at zero and the allowed flux swing is in the 1st quadrant only. The magnitude of the error signal (when the transistor switch turns on) is the same in all three figures since $d\Phi_2/dt$ is the same. As the magnetizing current increases, the developed error signal due to $d\Phi_2/dt$ in the winding around the outer leg (with the air gap) also increases because $d\Phi_2/dt$ increases with flux density. From the shape of the collector current it is obvious that the core is not saturated.

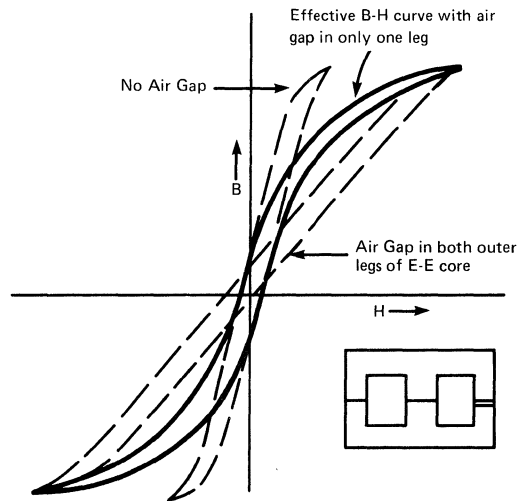


Figure 5. Effects on Hysteresis Curve with Air Gap in Only One Leg of E-E Core

Figure 10 shows the voltage developed across Resistor R_1 from the auxiliary winding and also the current in the two transistors I_{C1} and I_{C2} . The current waveforms show that there is no symmetry in the flux of the core. Figure 11 shows the same output voltage peak detected by paralleling Capacitor C_1 across Resistor R_1 . The voltages developed are not symmetrical during the alternative half period of the cycle. Figure 12 shows that when the developed voltage is fed back to the control circuit, it produces flux symmetry in the core. This can be seen by the equal magnitude of the collector currents.

The initial amplitude of the voltage from the auxiliary winding (after the transistor turns on) can be used to further improve performance. This can

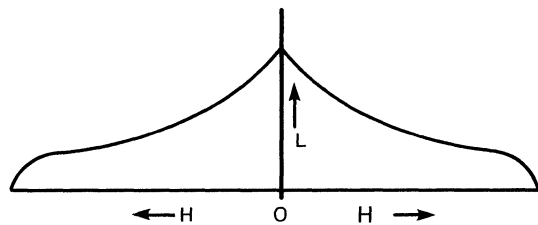


Figure 6. Inductance vs Magnetomotive Force

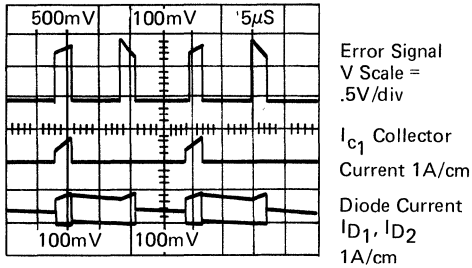


Figure 9. Error Signal Developed at Magnetizing Current = 700 mA

CLOSING THE LOOP

The developed voltage across R_1 and C_1 is fed back to the control circuit (UC3524).

This voltage can be fed into the control circuit in one of three ways:

1. AC coupled into the output of the error amplifier. Since this amplifier is a trans-conductance design, the output has very high impedance (approximately $5 M\Omega$). The feedback signal from the auxiliary winding is modulated at this point with the output voltage of the error amplifier. The output pulse width is corrected to provide symmetry as well as to prevent core saturation.

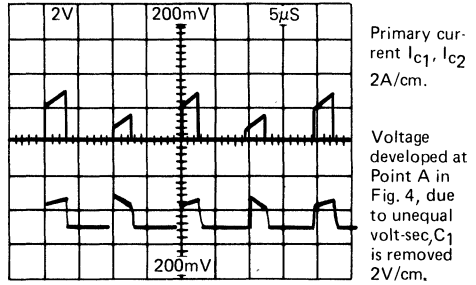


Figure 10. Without a Feedback

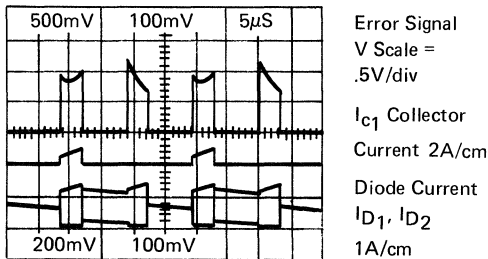


Figure 11. Without a Feedback

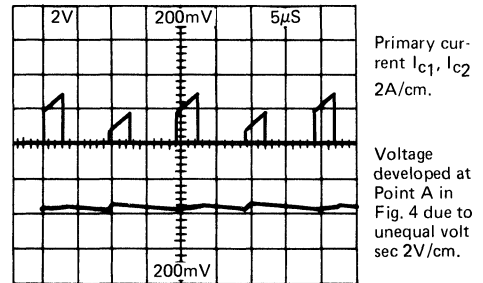


Figure 12. With a Closed Loop

2. Into the non-inverting input. This can be achieved by (a) lifting up 4.7K from ground in the NI circuit, (b) adding 100Ω in series with 4.7K and the other side of 100Ω returning to ground, and (c) adding a feedback signal at the junction of the 100Ω and 4.7K resistors. The peak to peak amplitude of the signal fed into the NI input has to be less than the output ripple voltage fed into the INV input. Feeding signals in the NI or INV inputs will provide flux symmetry in only DC conditions.
3. Feeding the signal at the INV input. This requires an opposite polarity signal, which can be obtained by reversing the diodes in

Figure 4. The modifications required to change the circuit are the same as listed above. Also in this case the peak to peak amplitude of the signal fed into the INV input has to be lower than the peak to peak output ripple voltage fed into the INV input.

To obtain adequate signal at very low input voltages may require a low V_F diode.

PWM PUSH-PULL CONVERTER

A complete schematic of the PWM Push-Pull Converter using this technique is shown in Figure 13. The power switch is a Unitrode hybrid circuit, the PIC636, which is housed in a 4 pin electrically isolated TO-66 package. It provides the advantages of low RFI and ease in heat sinking due to the electrically isolated package. Constant base drive is provided by small signal transistors (2N2905). The output rectifier is a center tap TO-220 fast recovery (35nS) rectifier. The control chip is a UC3524 PWM voltage regulator. The soft start function is performed at the NI input by allowing the reference voltage to come up slowly when the input power supply is turned on. The feedback signal from the auxiliary winding is fed into the compensation terminal (output of the error amplifier) with Resistors R_2 , R_3 and Capacitor C_2 . The steady state and transient response of the circuit was evaluated: it provides flux symmetry and prevents core saturation under these conditions.

HALF BRIDGE CONVERTER

The method described in this paper can be used for half bridge configurations as shown in Figure 14. It does not require a low ESR, high voltage capacitor in series with the primary of the transformer. The DC balance is provided by Capacitors C_1 and C_2 . Thus, this technique offers a low cost solution in preventing core saturation and in providing flux symmetry.

BUCK REGULATOR

In a buck regulator, the method described here can be used to provide the current limiting function without a current sense resistor.

The circuit shown in Figure 15 is a high performance buck regulator. It utilizes the Unitrode power hybrid switching regulator circuit, PIC625. The high performance transistor chip and fast recovery (20nS) rectifier diode are mounted in an electrically isolated 4 pin TO-66 package. The control circuit is a Unitrode Corp. PWM voltage regulator chip. The inductor L utilizes the equal E-E core configuration with unequal air gaps in the side legs. The main winding is placed on the center leg while the two auxiliary windings are wound on the outer legs. The output voltage from these auxiliary windings are compared using Transistor Q_3 . The magnitude of the current limiting is adjusted with Resistor R_1 . When the current in the hybrid circuit, PIC625, exceeds the set current

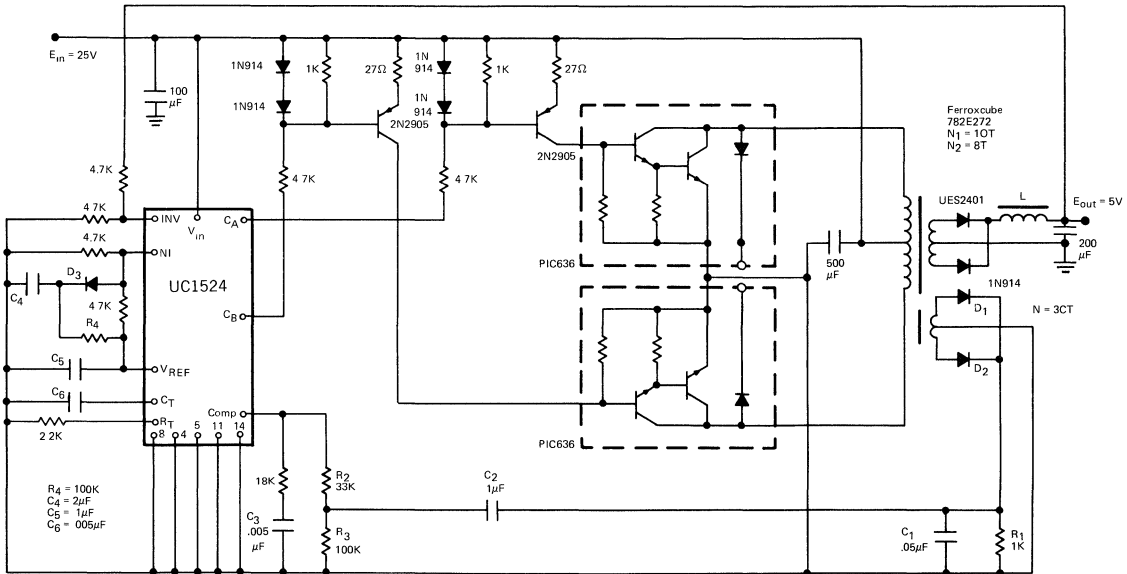


Figure 13. PWM Push-Pull Converter

limit, Q_3 turns on and the voltage developed across C_1 and R_2 is fed into transistor switches Q_1 and Q_2 . The transistor Q_2 removes the drive current from the PIC625 instantaneously. It provides protection during the transient condition. The transistor switch Q_1 provides the function of current foldback by discharging the soft start capacitor C_2 . The transient response of this circuit is shown in Figure 16. The current in the switching transistor during short circuit and normal operation mode is shown in Figure 17.

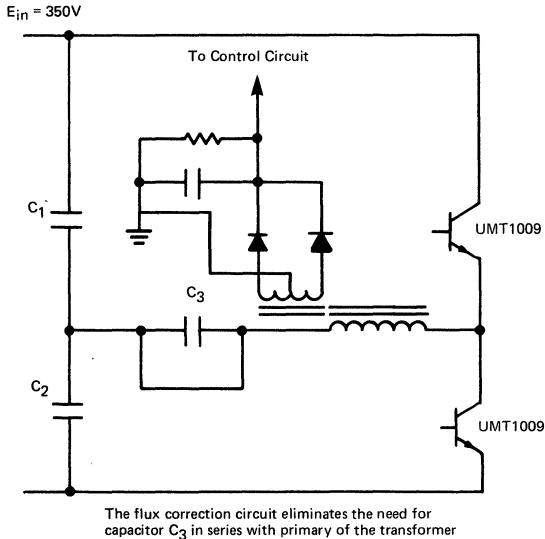


Figure 14. Half Bridge Converter

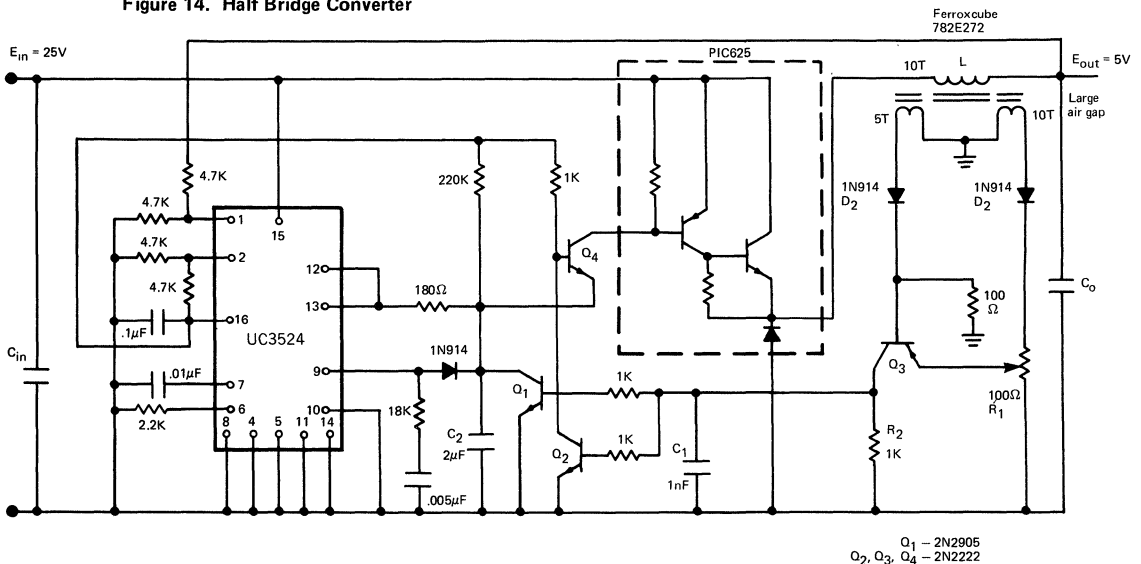


Figure 15. High Performance Buck-Type Switching Regulator

CONCLUSION

The low cost circuit described in this paper prevents core saturation due to unsymmetrical flux, and provides equal collector current in the transistor switch and in the rectifier diodes. The power dissipation of these switches is kept in balance.

Further advantages of this approach are:

1. a. In a push-pull converter, the need for an inductor is eliminated, thus, the size, cost and weight are reduced.
- b. Transient response time is improved.
2. In a bridge type converter, a capacitor (low ESR, high voltage) in series with the primary of the power transformer is not required. (In conventional designs even with this capacitor, there exists a danger that the core can be driven into saturation under transient conditions).
3. In a buck type converter, it allows the current limiting function to be performed without a current sense resistor, thus improving the performance.
4. Storage time and $V_{CE(SAT)}$ matching of the transistor switches are not required.
5. More efficient use of the transformer, allowing smaller, lower cost magnetics is achieved.
6. In an off-line converter, isolation is maintained.

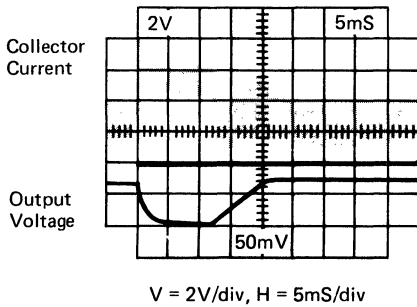


Figure 16.
Collector currents for step change
in load from 1A to 5A, to 1A.

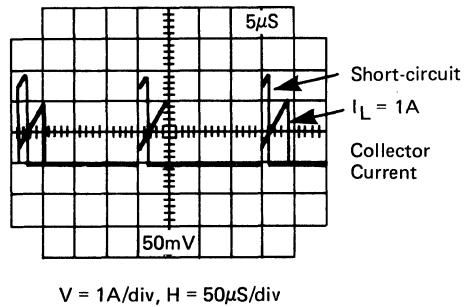


Figure 17.
Collector currents, $I_L = 1A$ and under
short circuit conditions.

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1. Walter J. Hirschberg, "A New PWM Control Technique That Eliminates Transformer Unbalance Problems in Power Converters", ACDC Electronics Powercon 6, 1979.
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HYBRID CIRCUITS FOR LOW VOLTAGE SWITCHED-MODE CONVERTERS

ABSTRACT

Hybrid circuits offer many advantages over the conventional discrete approach in switched-mode converters. This paper deals with the construction of the hybrid circuit and its thermal considerations. It examines the efficiency of a buck regulator employing a saturated transistor versus the optimized darlington configuration. Also considered are the effects of reverse recovery of the rectifier and base spreading resistance of the transistor on the efficiency of a switching regulator. Finally, applications of standard hybrid circuits for switched-mode converters are discussed.

I. INTRODUCTION

Recently a rapid increase in the use of hybrid circuits in switched-mode power converters is evident due to their inherent advantages. Some of these advantages are: dc and high frequency electrical isolation, ease in heat sinking multiple power components within the single hybrid package, reduced stray parasitics, and finally, lower overall cost compared to the discrete approach.

The hybrid circuit approach requires careful consideration of thermal design for maximum reliability and proper selection of silicon chips for best electrical performance. This paper provides an overview of the construction of a typical power hybrid switching regulator circuit and its thermal design considerations. Also considered are the effects of the reverse recovery time of the rectifier and the base spreading resistance r_{BB} of the power switching transistor on the efficiency of the switching regulator. Applications and advantages are also discussed for types of hybrid circuits which are designed for low voltage applications and other types designed for "off-line" switched mode converters.

II. CONSTRUCTION

The power hybrid circuit PIC600 is the power output stage of a buck type switching regulator as shown in Figure 1. It consists of a high speed darlington-connected transistor pair, a commutating diode and two thick film biasing resistors. These components are housed in a 4 pin electrically isolated TO-66 package.

The manufacturing procedure for these devices is divided into two stages. First, a BeO substrate is chosen because of its excellent thermal conductivity, -- 70% as good as copper. The interconnection paths, pad areas for the wire bonds and the thick film resistors are screen

printed onto the BeO substrate and then fired in high temperature furnaces. For optimum performance, the tolerances of the thick film resistors are maintained within 10% of their design values. The semiconductor devices used in the circuit are all silicon planar passivated devices and are gold eutectic mounted. Aluminum ultrasonic wire bonding is used for interconnections.

In the second stage the BeO substrate is soft soldered to the header for good heat transfer. A copper slug is interfaced between the BeO substrate and nickel plated steel header. The copper slug is used to relieve mechanical stress between the BeO substrate and the header and to provide heat spreading resulting in lower thermal resistance.

III. THERMAL CONSIDERATIONS

The design of the power hybrid circuit requires careful consideration to optimize important thermal requirements; thermal cycling, resistance, and partitioning. To obtain maximum thermal resistance, overlapping heat flow should be avoided. As shown in Figure 2, heat flow from silicon chips #2 and #3 overlaps, thus reducing the thermal capability. No overlapping heat flow occurs from chip #1.

Thermal resistance of the package can be calculated by the formula:

$$R_T = \rho \frac{t}{A}$$

where t is the thickness of material through which heat flows, ρ is the thermal resistivity of the material and A is the average area through which heat flows.

In making a conservative calculation, it is assumed that heat flux diverges at approximately a 45° angle for all the materials except the copper slug (62.5°) due to high conductivity.

The thermal resistance calculation of a hybrid circuit is shown in Figure 2. The copper slug between the BeO and header reduces the thermal resistance of the package (by about .32°C/W) by spreading the heat flow through a large area of the steel header.

This calculation assumes that no voids are present at the interfaces.

IV. COMPONENT AND CIRCUIT SELECTION

Achieving maximum efficiency in a buck-type regulator requires proper selection of electrical characteristics of the transistor switch and catch diode. Optimum efficiency can be obtained with a

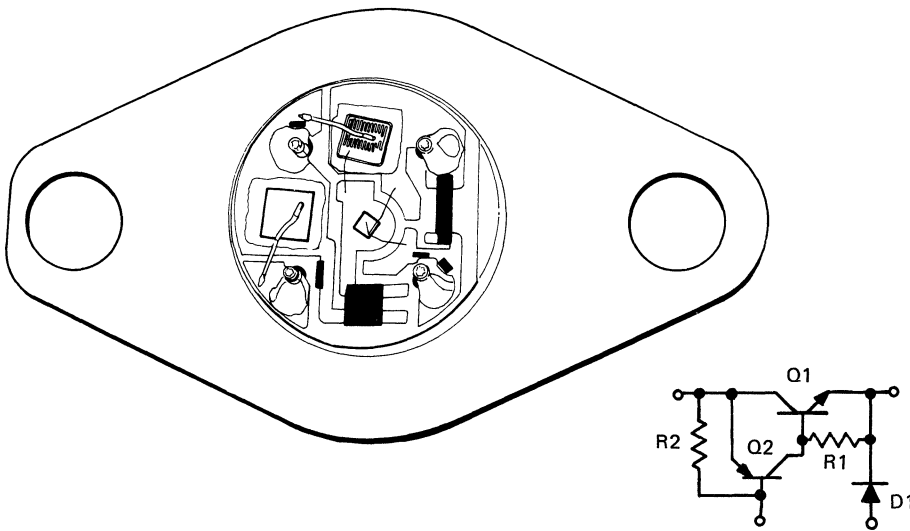
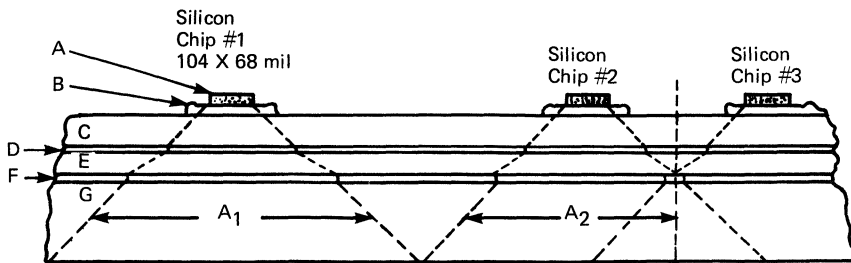


Figure 1. Unitrode power hybrid circuit (PIC600)



DEFINITION:

Material	Temp. Coef. 10 ⁻⁶ °C	ρ Rest. °C-in/W	t Thickness in mils	R _T * of PIC625
A - Silicon	4.2	.303	5	.214
B - Si Au Eut.	14	.182	3	.0718
C - BeO	6	.152	20	.249
D - Solder	23	.8	.4	.187
E - Copper	16	.104	10	.04614
F - Solder	23	.8	3	.0836
G - Steel	11	.884	65	1.043
			Total	1.8954

*R_T = $\rho \left(\frac{t}{A} \right)$

Figure 2. Heat Flux Line in a Hybrid Circuit

Schottky rectifier because it has lower forward drop than most PN junction devices. The Schottky rectifier is a majority carrier device and has zero reverse recovery time. However, the Schottky's high junction capacitance (10 times greater than PN junction devices) produces the same effect as the t_{rr} of PN junction devices. Junction capacitance does not change appreciably with temperature, so the effective reverse recovery time remains the same with respect to temperature. Since commercially available Schottky rectifiers have only a 45V PIV rating, the absolute maximum input voltage of the buck type regulator is limited to only 45V.

Ultra fast PN junction devices are available with the same effective reverse recovery as Schottky rectifiers with a higher (up to 400V) PIV capability. The somewhat higher forward drop of the PN junction devices does not degrade efficiency at higher voltages.

The way in which a device recovers from forward conduction is also important. In high voltage (>1000V) power supplies, it is desirable to have abrupt reverse recovery time for optimum efficiency. In low voltage, high current power supplies a soft reverse recovery rectifier is better suited from the RFI viewpoint.

Figure 3 shows the effect of a diode recovery time on transistor power dissipation. The reverse recovery time of the catch diode requires the transistor to conduct higher peak current for a longer

duration in the active region. This significantly increases RFI and also increases the power dissipation in the transistor, and may cause second breakdown.

For reliable circuit operation, t_{rr} should be much less than the current rise time of the transistor. This ensures minimum current overshoot in the transistor and also minimizes the amount of time the transistor spends in the active region during turn-on, resulting in lower power dissipation and increased efficiency. However, to obtain maximum efficiency, all switching times, (including current rise time) should be as fast as possible. The rectifier should be selected such that its t_{rr} is one third or less of the current rise time of the transistor. In switching regulator applications, it is also essential that the storage and fall times be as low as possible.

When turn-off is achieved without the assistance of I_{B2} , it is important that the power output transistor have the following characteristics for best performance:

1. Larger emitter periphery area with a triple diffused or double diffused epitaxial construction to provide lowest effective collector series resistance to prevent forward biasing of the collector-base junction.
2. The base spreading resistance, $r_{BB'}$, of the device should be lower than the external biasing resistor. This will provide low storage time and fast fall time.

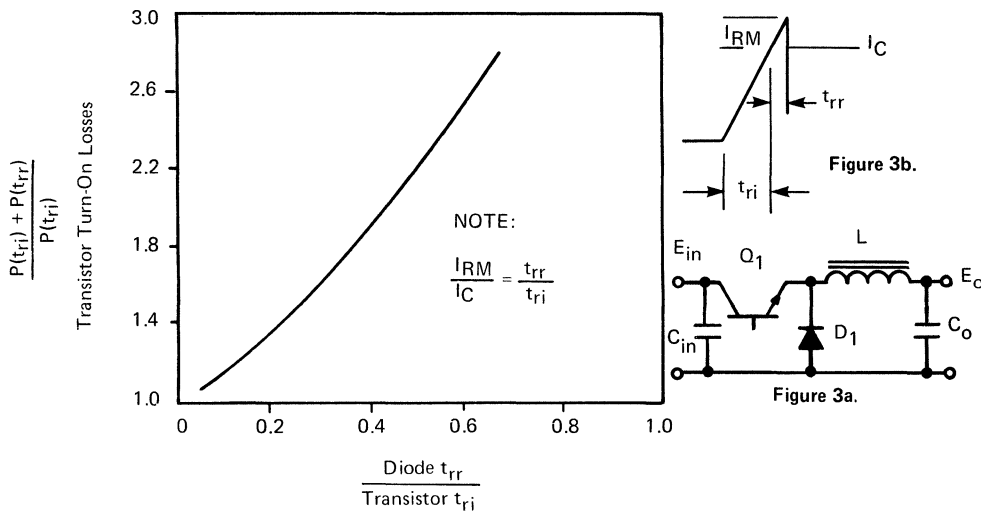


Figure 3. Importance of Reverse Recovery Time of a Rectifier

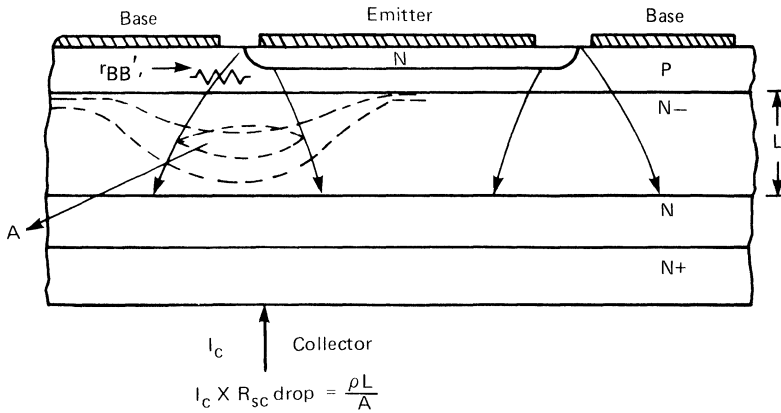


Figure 4. Effect of $r_{BB'}$ on Switching Times and Dynamic Saturation

The resistor turn-on biasing method works satisfactory up to 10A for a low voltage device without affecting the efficiency of the switching regulator. Another advantage of the resistive turn-off circuit is that it limits current crowding during turn-off thus increasing the reliability of the circuit. Since the driver transistor operates in a saturated mode, the device should have a high gain-bandwidth product to minimize overall storage time.

The hybrid circuit PIC600 consists of two transistors connected in a darlington configuration.

The internal biasing resistors of these transistors are sufficient for fast turn-off without requiring any I_{B2} .

The table shown in Figure 5 compares the efficiency of a saturated transistor (2N4150) versus the hybrid darlington as the switching element in a 50 kHz buck regulator. In each case, the output device has the same size silicon chip.

Pass Transistor	Power Losses (Watts) $T_j = 25^\circ\text{C}$	Efficiency	
		$\frac{E_o}{E_{in}} = 0.5$	$\frac{E_o}{E_{in}} = 0.2$
2N4150 (Saturated)	D.C. Losses	84.79%	81.66%
	Switching Losses		
	Drive Losses		
	Diode Losses		
PIC625 (Darlington)	D.C. Losses	82.8%	81.69%
	Switching Losses		
	Drive Losses		
	Diode Losses		

Conditions: $f = 50\text{KHz}$
 $E_o = 5\text{V}$
 $I_o = 7\text{A}$
 Same size output device for both cases.

Figure 5. Comparison Between Saturated and Darlington Pass Transistors in a Buck Type Switching Regulator

In the saturated transistor approach, the transistor is driven with a forced Beta of 5 during turn-on and turn-off. However, in the darlington configuration, no turn-off base drive is employed. Typical measured switching times and saturation voltages are used to calculate losses.

From the table in Figure 5, it is evident that the hybrid darlington approach provides best results in terms of efficiency when the ratio between the output and input voltage is less than 0.25. In a darlington configuration, if the output device is kept out of saturation, then the rise, fall and storage times will be reduced compared with the saturated transistor. Even at higher output/input voltage ratios the loss in efficiency because of higher $V_{CE(SAT)}$ is minimal compared to the complexity and cost of a drive circuit required for a saturated transistor.

The plot in Figure 6 shows dc power dissipation of a PIC625 at various duty cycles and temperatures. The efficiency of the regulator depends heavily upon output voltage. Switching losses of the PIC625 under conditions shown in Figure 6 are:

- 25°C — 0.875W
- 55°C — 0.525W
- 125°C — 1.476W

V. APPLICATIONS

Different applications of power hybrid circuits are discussed in this section.

Low Voltage Hybrid Circuits (<100V)

Some applications of low voltage hybrid circuits are: low and high current positive and negative buck-type regulators, bidirectional motor driver circuits, PWM push-pull and half bridge converters. Each is discussed briefly as follows:

a. Buck Type Switching Regulator

The schematic of the low cost, free running buck switching regulator is shown in Figure 7. When the output voltage is lower than the reference voltage, transistor Q₂ is on and provides the base drive to the power hybrid circuit PIC600. The current in inductor L₁ increases linearly and continues to charge the output capacitor C_o. When the output voltage exceeds the zener voltage of diode D₁ (plus some fixed fraction of V_{BE} of transistor Q₂) transistor Q₂ turns on and removes base drive current from transistor Q₁ and hybrid circuit PIC600. Resistor R₆ and capacitor C₁ are used to provide fast switching times. The output voltage is trimmed with resistor R₃.

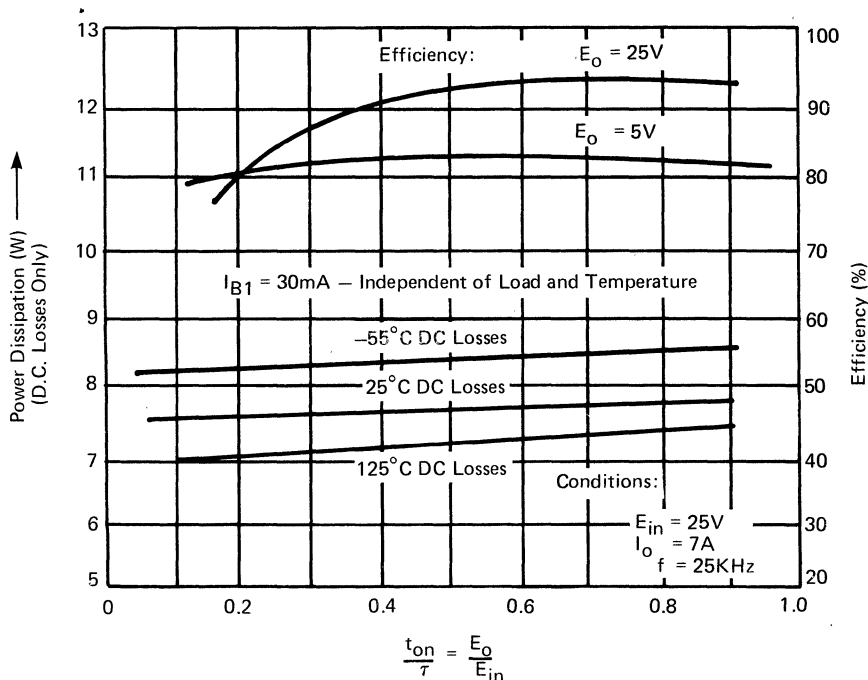


Figure 6. Losses and Efficiency — PIC625

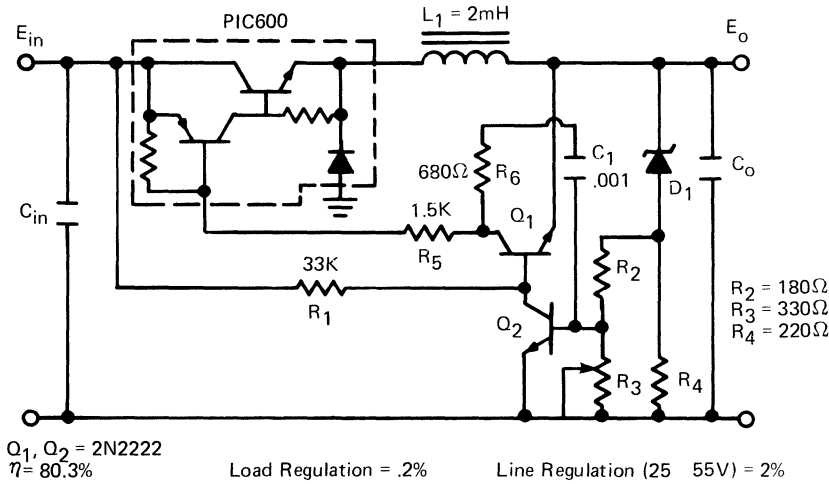


Figure 7. Low Cost Buck Regulator

b. High Frequency Switching Regulator

Low voltage hybrid circuits can be operated as high as 250 kHz due to their fast switching times. When these devices are used above 100 kHz, the storage time of the driver transistor must be reduced. This can be done by using a Baker clamp with resistor R_1 and diode D_1 as shown in Figure 8.

The advantages of operating a buck regulator at higher frequencies are:

- Lower filter cost
- Reduced size and weight
- Improved transient response
- Output ripple voltage less dependent upon ESR of capacitor
- Simpler EMI and RFI filtering

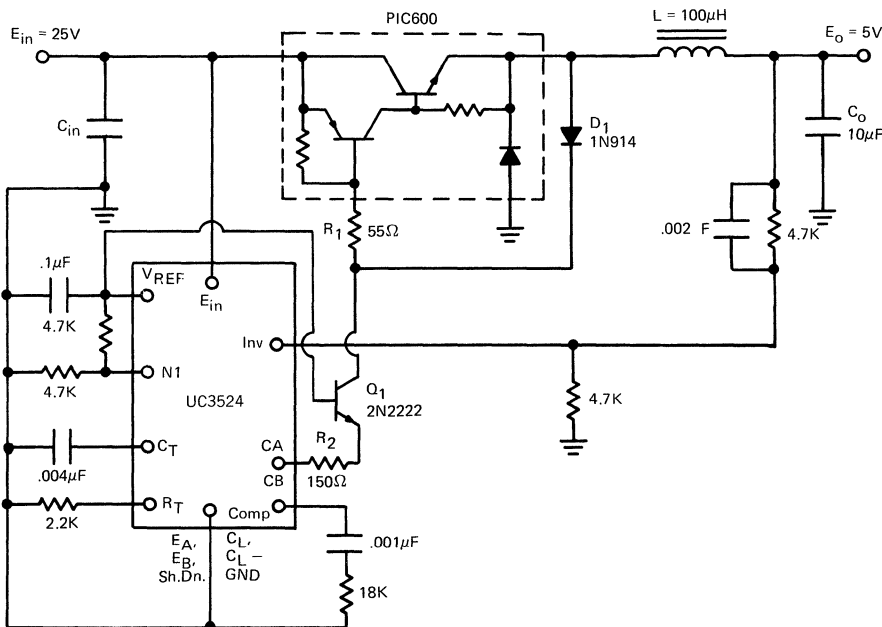


Figure 8. Operating a PWM Buck Regulator Above 100KHz

c) Extending Output Current Capability up to 20A

The output current capability of a buck regulator can be extended by (1) paralleling the output devices as shown in Figure 9 and (2) the use of a high current device as shown in Figure 10.

The advantages of paralleling output devices are that it allows the device to operate with a relatively simple drive circuit and provides simplicity of heat sinking. On the other hand, proper current sharing during the on-time period and turn-off time is required. The circuit shown in Figure 9 provides the circuit technique to do just that. The only drawback is that it requires a dead-band period which must be greater than $0.1L$, where L is the inductance value of the common mode choke L_1 .

Another method is to use high current devices like the PIC740, a power output hybrid circuit. It consists of a 25A power output transistor and Schottky rectifier. The device is housed in a 3 pin TO-3 package with copper-core pins. The heat generation is kept to a minimum by using the Schottky rectifier and copper-core pins which allow the use of the TO-3 package for 25A buck type regulators. The limitation of these devices is that the maximum input voltage is only 40V. These devices can be used in high efficiency, high current buck switching

regulators. In high current applications, careful consideration should be given to the drive circuit when the output device of the PIC740 is operated in the saturated mode. An increase of up to 5% in efficiency compared to the darlington can be realized at 15A output current.

PWM Push-Pull Converter

The circuit schematic shown in Figure 11 is a width modulated push-pull converter. It utilizes the Unitorde PIC636 power hybrid circuit.

Flux symmetry⁵ in the transformer core is provided by introducing an air gap in only one leg of the EE core configuration. The voltage developed across resistor R_1 and capacitor C_1 is proportional to the flux density in the center leg of the EE core. This developed voltage is fed back into the control circuit at the output of the error amplifier. The output pulsewidth is corrected by the developed voltage across C_1 and R_1 , providing flux symmetry in the power transformer.

Bidirectional Motor Drive Circuit

These power hybrid circuits can be employed to drive inductive loads, such as DC motors, stepper motors, and hammer drivers. Small inductors L_1 and L_2 limit cross-conduction current during switching times of the two hybrid circuits. The excellent switching properties of the hybrid circuit allow the circuit to be operated with high efficiency up to 100 kHz, improving transient response of the circuit.

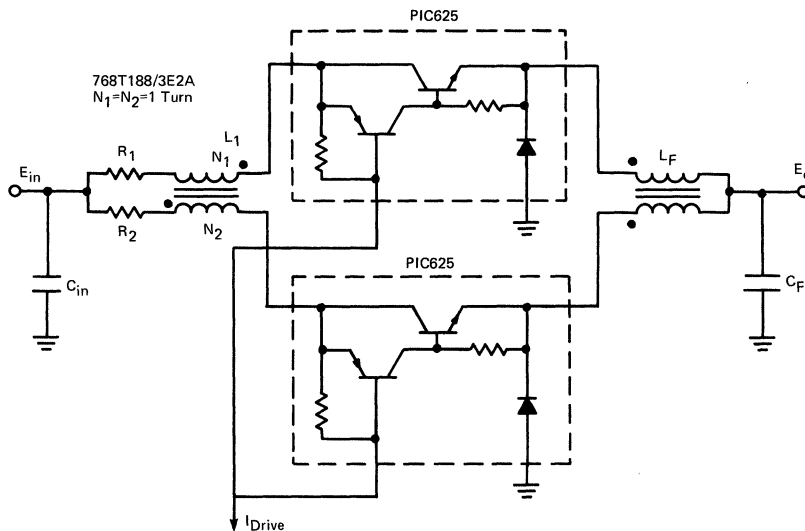


Figure 9. Current Sharing with a Common Mode Choke

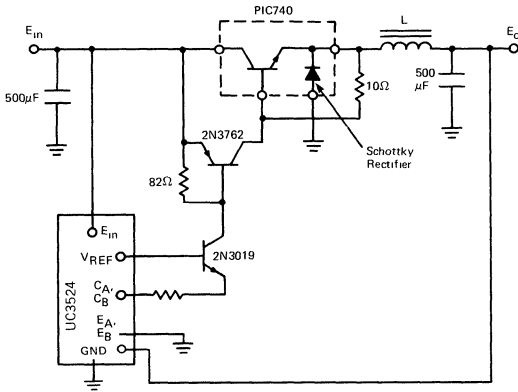


Figure 10. Simplified Schematic of 20A Buck Type High Efficiency Switching Regulator

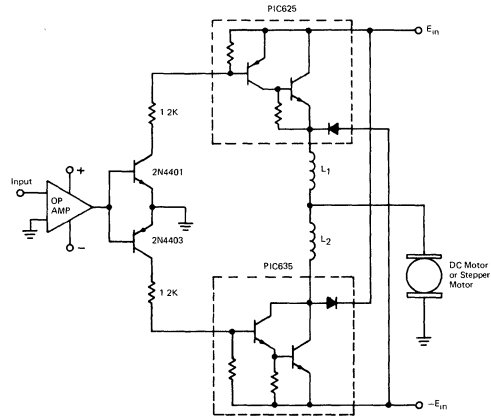


Figure 12. Bidirectional Motor Drive Circuit

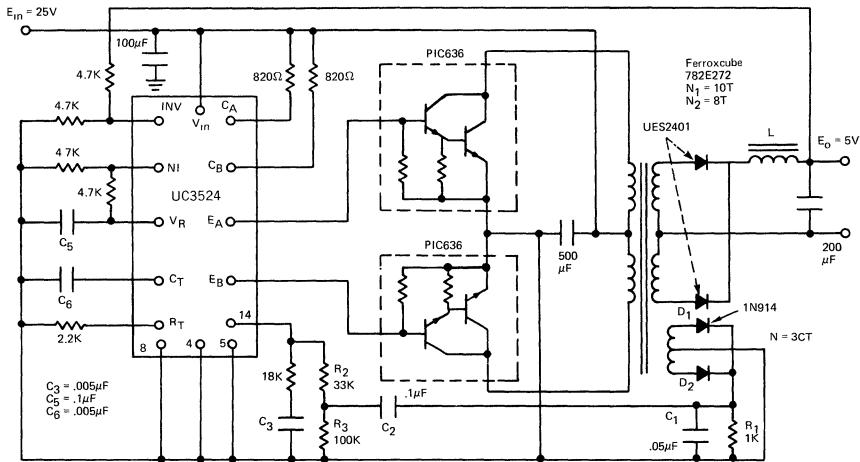


Figure 11. PWM Push-Pull Converter

VI. CONCLUSION

A wide variety of power hybrid circuits in standard packages for switched-mode converter applications have been developed by Unitrode. Power components were carefully selected for optimum electrical performance. In many instances these hybrid circuits not only provide superior electrical performance but also reduce the overall cost of the power supply by reducing production labor and repair cost.

INCORPORATE ACTIVE INRUSH CURRENT LIMITING TO IMPROVE RELIABILITY AND EFFICIENCY OF POWER SUPPLIES

Active inrush-current limiters—unlike fuses and circuit breakers—prevent dangerous situations instead of only reacting to them. Apply limiting techniques, and you need not employ extra-hefty rectifiers just to ensure rectifier survival during turn on.

The input filter capacitor employed in many power-supply designs creates a potential problem—high inrush current. Fortunately, though, adding a few extra components can prevent inrush current and its associated circuit damage.

How does the input capacitor cause such problems? Intentionally chosen for high storage capacity and low equivalent series resistance (ESR), it behaves like a nearly perfect short circuit when the supply first turns on. The resulting short-duration peak inrush current can reach levels much greater than the tolerable single-cycle ratings of the supply's semiconductor rectifiers (thus destroying them) and still not contain sufficient total energy to open protective fuses or circuit breakers. Additionally, the supply's rapidly rising voltage and current levels could cause dv/dt- or di/dt-sensitive devices in neighboring hardware to fail or malfunction.

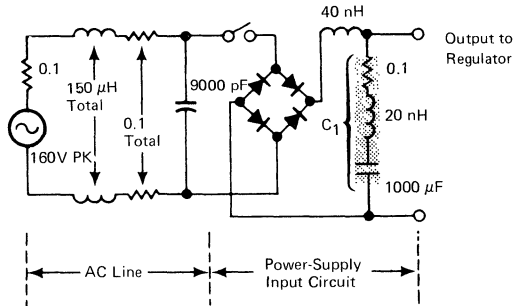
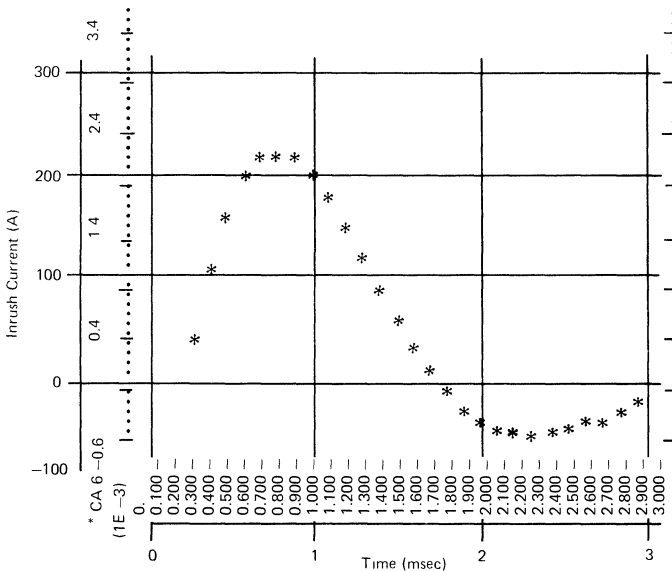


Figure 1. Based upon this generalized model, analysis indicates the inrush-current problem's magnitude. Chosen for its low ESR, the input filter capacitor (C_1) behaves like a nearly perfect short circuit when the supply first turns on.



ECAP
TRANSIENT ANALYSIS

```

C
B1      N(0,1), R = .1
B2      N(1,2), L = 150E - 6
B3      N(2,3), R = .1
B4      N(3,0), C = 7000E - 12
B5      N(3,4), R = .001
B6      N(4,5), L = 40E - 9
B7      N(5,6), R = .1
B8      N(6,7), L = 10E - 6
B9      N(7,0), C = 1000E - 6
E1      (1), 0, 0, 0, 160
TIME STEP = 100E - 6
FINISH TIME = 3E - 3
1ERROR = 1
PRINT NV, CA
PLOT, (SCALED), CA(6)
BINARY, NV, CA
    
```

Figure 2. Peaks greater than 200A are predicted by ECAP for the circuit model shown in Figure 1.

Turn on an analysis before you turn on a power supply

Computer analysis proves useful

To appreciate the inrush-current problem, consider an estimate of its magnitude before examining possible control techniques. Figure 1 depicts a model of the ac-input and rectifier/filter sections for a typical power supply. Although shown in a straight off-the-power-mains configuration, the model should be valid for any other design with the same output-power capability.

An ECAP computer analysis performed for this circuit assumed worst-case conditions: switch closure at 160V (peak voltage). The results (Figure 3) of a typical design. The current pulse's high level and short duration could generate severe, localized hot spots in rectifier junctions or cause false triggering of rate-sensitive devices elsewhere in the circuit.

A standard approach to current limiting is depicted in Figure 4a—a resistor. It's simple, reliable and easy to design in, but efficient it isn't. At any current level, it dissipates power that would otherwise be available to the load. The resistor does perform a surge-current-limiting function, however.

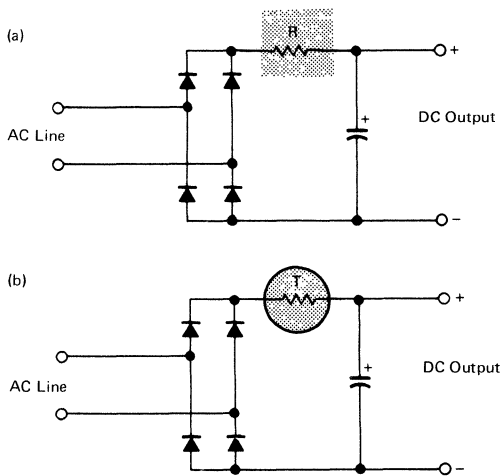


Figure 4. Two common methods of inrush limiting employ either a resistor (a) or a thermistor (b). But if the resistor is large enough to effectively control surge currents, it also significantly reduces efficiency. The thermistor, while more efficient, offers little protection during dropout recovery because of its long thermal time constant.

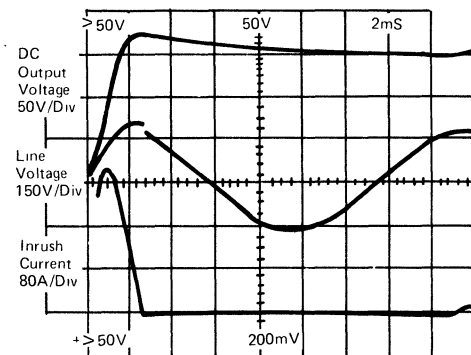
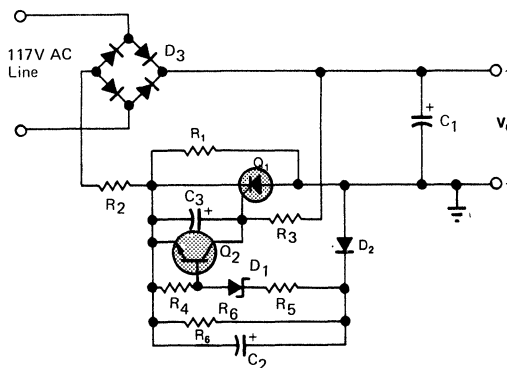


Figure 3. Measured inrush current appears close to that predicted in Figure 2. This large current inrush could cause junction hot spots and generate troublesome EMI.

Alternatively, a thermistor-controlled current limiter (Figure 4b) alleviates the resistor's efficiency problems to some extent, but it aggravates the dropout-recovery problem. The same cold-to-hot resistance variation that permits turn-on current limiting and high efficiency at low operating currents fails in dropout-recovery situations: The thermistor's long thermal time constant prohibits fast recovery.



NOTES

R1: 3, 5W	C1: 1000 μ F	Q1: L2R06254
R2: 0.2, 10W	C2: 10 μ F	Q2: UPT312
R3: 3k, 5W	C3: 2 μ F	
R4: 1k	D1: UZ4715	
R5: 1k, 2W	D2: 1N4245	
R6: 2k	D3: UT680-4	

Figure 5. SCR soft starting bypasses the current-limiting resistor (R_1) only when the peak-detected voltage across Q_1 drops below the zener breakdown, i.e., when C_1 becomes almost fully charged through R_1 .

SCR spells efficiency

In view of resistor and thermistor drawbacks, active soft-start designs offer a best-of-both-worlds solution—effective inrush limiting, fast recovery and high operating efficiency. This type of circuit, shown in Figure 5, essentially incorporates a current-limiting resistor (R_1) and a bypass switch (Q_1). At turn on, Q_1 is OFF, and the surge current (I_S) develops a voltage across R_1 . This voltage is peak detected by D_2 and stored in C_2 . When the voltage exceeds D_1 's zener breakdown—an event that should occur almost instantaneously— Q_2 turns on, disabling Q_1 's gate-triggering network (R_3C_3). As the power supply's filter capacitor C_1 charges up, the inrush peaks diminish until the detected $I_S R_1$ voltage falls below D_1 's zener breakdown. Q_2 then turns off, and the R_3C_3 network charges up and fires Q_1 , bypassing R_1 .

This circuit recovers rapidly enough to limit inrush currents that could occur as a result of even short line dropouts. When the ac input voltage goes to zero, the voltage across Q_1 also goes to zero, and Q_1 turns off. When the input voltage reappears, Q_2 keeps Q_1 's gate circuit OFF until R_1 has allowed C_1 to become almost fully charged.

Figure 6 graphically depicts this design's inrush-limiting ability. Note how the $I_S R_1$ voltage level (upper trace) tracks the diminishing inrush-current pulses (lower trace) for the first three cycles. At the 17-msec point (slightly after the third current pulse), the peak detected voltage has dropped below the zener breakdown point, and Q_1 switches on, bypassing R_1 . Then R_2 limits inrush currents.

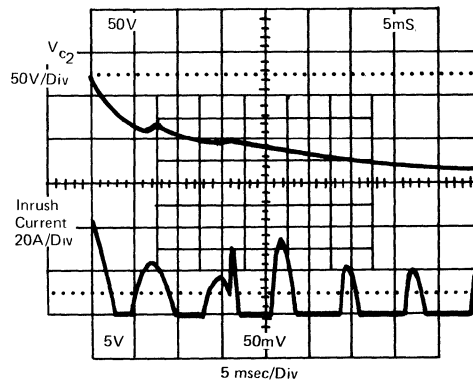


Figure 6. Inrush-current pulses of decreasing magnitude (bottom trace) lower the SCR's hold-off voltage (upper trace). After 17 msec, the SCR fires.

After determining your design's maximum continuous dc output current (I_O) and inrush limit (I_S), you can select an appropriate SCR. (The major SCR considerations are the peak repetitive blocking voltages and the maximum average plus peak current levels.) Typical SCRs exhibit a gate-turn-on voltage (V_{GT}) of about 0.6V; typical power-supply circuits exhibit a di/dt of about $1A/\mu\text{sec}$ —two quantities required for calculating the values of the other critical components:

$$R_1 = \sqrt{2V_{AC}/I_S}$$

$$R_2 = P_{R_2}/I_O^2$$

$$V_Z = I_S R_2$$

$$C_3 \geq (2\sqrt{2} V_{AC} V_Z) / (R_3 V_{GT} R_1 (di/dt)).$$

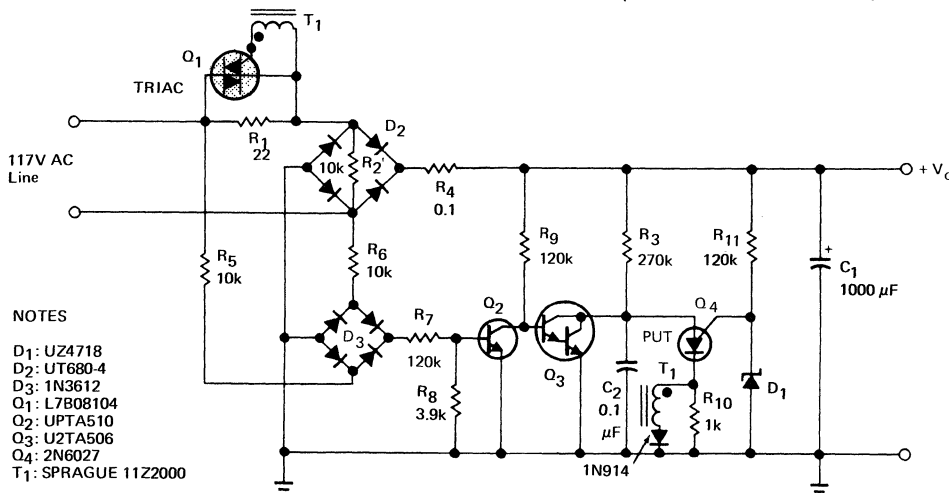


Figure 7. Phase controlling a triac limits inrush-current pulses' amplitude and duration. Cycle-by-cycle triggering — handled by the PUT comparator — ensures instant recovery from line dropouts.

Switch out the limiting resistor when the inrush is over

In the second equation, specify PR_2 as the maximum power your requirements allow across R_2 .

Another effective inrush-current limiter is the phase-controlled triac design shown in Figure 7, which operates by controlling the conduction time of the current surges. Initially, the dc voltage (V_O) across C_1 builds up slowly because of R_1 's current-limiting action. This dc voltage helps establish a reference (via R_{11} and zener diode D_1) for the programmable unijunction transistor (PUT) Q_4 and charges the phase-control timing capacitor C_2 (via R_3). The PUT fires when its trigger point is reached, turning the triac on. Thus, when V_O is initially low, C_2 charges slowly, and the triac triggers on late in the half cycle. As V_O rises Q_1 turns on earlier in each cycle until nearly 100% conduction is achieved.

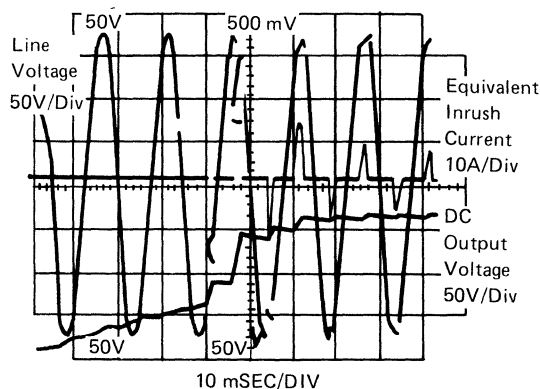


Figure 8. Triac conduction follows the gradually increasing dc output voltage, decreasing the would-be inrush current. When the output voltage reaches design level, the triac is bypassing the current limiter nearly 100% of the time.

The remaining circuit components (D_3 , Q_2 , Q_3 , etc) discharge timing capacitor C_2 on each half cycle, thereby assuring cycle-by-cycle current limiting and fast recovery from dropouts. Figure 8 depicts the relationship between the ac input voltage, the dc output voltage and the varying conduction angle of the triac.

HYBRID CIRCUITS FOR OFF-LINE SWITCHING POWER SUPPLIES

1. Introduction

Hybrid circuits offer many advantages over the conventional discrete approach for switching power supplies, which has resulted in a rapid increase in their use. These advantages include ease in heat sinking multiple power components, while maintaining DC and high frequency isolation, reduced stray parasitics and lower overall cost. This application note discusses one of the hybrid circuits built by Unitrode, its components and construction, and two applications in detail, a Forward Converter and a Half-Bridge Converter.

2. "Off Line" Hybrid Circuits

2.1 Advantages

The Unitrode PIC800 series are "Off Line" hybrid circuits consisting of a high voltage power transistor and a fast recovery diode mounted in a 4 pin electrically isolated TO-66 package. The following advantages can be derived by using these power hybrid circuits:

- a) Reduced EMI because of
 1. Lower capacitance (10pF instead of 100pF) between the case and active components compared to the conventional TO-66 package, and
 2. faster recovery time of the rectifier (less than 40nSec).
 3. the close proximity of the diode and transistor chip; this also results in reduced ringing.
- b) Heat sinking is simple because the package is isolated; devices can be mounted on the same heat sink without any precautions regarding isolation up to 800V.
- c) Components are matched for better performance.

2.2 Components

In a high voltage "off line" hybrid circuit a large portion of the power dissipation in the transistor is due to switching losses. The PIC800 series hybrid circuits utilize a Unitrode high voltage transistor which has been computer optimized for fast

switching speeds. This optimization and the specially interdigitated structure result in lower r_{bb} ' and uniform current injection. The PIC800's rectifier diode, a gold-doped epitaxial device, was chosen for a typical reverse recovery time of 20nSec. This is less than one-third of the transistor's current rise time, to minimize transistor switching dissipation and the generation of spikes and RFI. These power hybrid circuits have the capability of switching up to 8A at 400V and are designed for such applications as high voltage buck type regulators, bridge circuits, forward converters, deflection circuits and DC motor drives.

Type	Peak Output Current	Input/Output Voltage	Polarity	Fall Time Voltage (nS)	Fall Time Current (nS)	On-State Voltage $V_{CE(sat)}$ (V)	Package
PIC800 PIC801	8A	350 400	Pos	200	200	1.5 μ A 5	4 PIN TO-66 (Isolated)
PIC810 PIC811	8A	350 400	Neg	200	200	1.5 μ A 5	4 PIN TO-66 (Isolated)

FIG. 1a - PIC800 Series Hybrid Circuits

TYPICAL INDUCTIVE SWITCHING TIMES				CONDITIONS	
Current	Temp	t_s μ S	t_{fv} nS	t_r nS	$I_C = I_{BI} = I_{B2}$
$I_C = 5A$	25°C	.9	80	100	$V_{CC} = 125V$ $V_{(clamp)} = 350V$
	100°C	1.0	190	140	

FIG. 1b - Unitrode Transistor Switching Times

2.3 Construction

The PIC800 series hybrid circuit is shown in Figure 2. It combines a transistor and a commutating diode in a 4 pin electrically isolated TO-66 package.

Berillium oxide (BEO) is used for the substrate because of its excellent thermal conductivity, 70% as good as copper. The interconnection paths and pad areas for the wire bonds are screen printed on the BEO substrate and fired in high temperature furnaces. The semiconductor devices used in the circuit are gold eutectic mounted, and aluminum ultrasonic wire bonding is used for interconnections.

The BEO substrate is soldered to the nickel plated steel header with a copper slug between them. The copper slug relieves mechanical stress between the BEO substrate and the header, and provides heat spreading for lower thermal resistance.

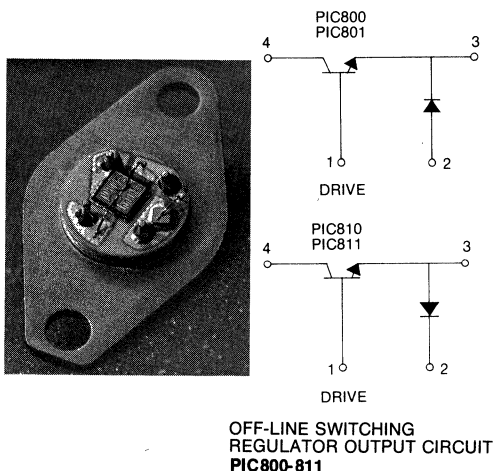


Figure 2. PIC800 hybrid circuit

3. Off-Line Forward Converter Application

This section discusses the design for an off-line Forward PWM Converter, 50 watts total to multiple outputs. The design employs such features as soft start, current limiting and protection from output short circuits. The Forward Converter design uses one PIC811 hybrid circuit. The power output transformer uses a demagnetizing winding to prevent core saturation, as does the base drive transformer. The PWM control circuit uses a UC3524 regulator chip. Proportional base drive reduces the power transistor

storage time, and an RC snubber limits the turn-off power dissipation.

Section 4 of this application note discusses the design for an off-line half-bridge converter.

Other Unitrode application notes discuss the design of buck, boost, flyback and H-bridge type switching power supplies. (Application Notes U68A, U80, U76 and Design Note DN-8).

3.1 Description of Functional Circuits (see Fig. 3.3)

Current limiting is performed by measuring the collector current of the power transistor Q1 and cutting off the base drive of Q1 instantaneously. Resistor R6 measures the emitter current in Q1; when the voltage developed across R6 becomes greater than V_{BE} of Q4 (0.7V), Q4 turns on and diverts Q1's base current.

Soft start capacitor C11 is at zero volts when the power supply is turned on, and CR26 keeps pin 9 at 0.7V more positive than the voltage on C11, which is being charged slowly by R13.

The maximum pulse width is set by potentiometer R12 and CR24. Storage time of the power transistor Q1 is reduced by using proportional base current drive and by providing large base turn-off current, using transformer T3 and the associated combination of diodes.

3.2 Specs:

Input – 95 to 135V, 60Hz

Outputs – 5V @ 3A, ±15V @ 1A

Regulation – Line: 0.2% for specified AC input.
 – Load (20% to 100%): 5V output, 0.3%; ±15V output, 3%.

Ripple & Noise – 50mV peak to peak for ±15V outputs, 100mV for 5V output.

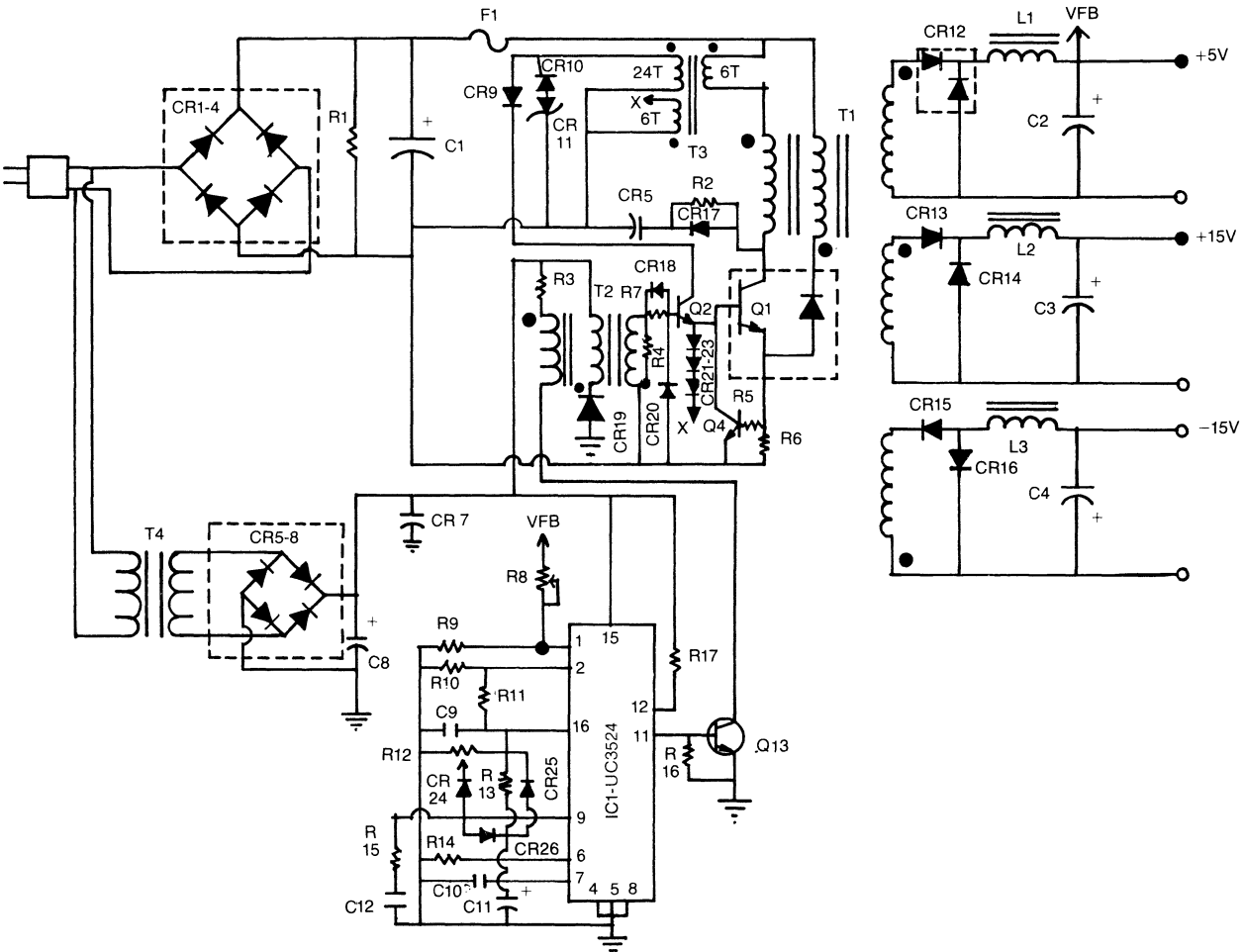
Frequency – 30KHz

Efficiency – 78%

Features:

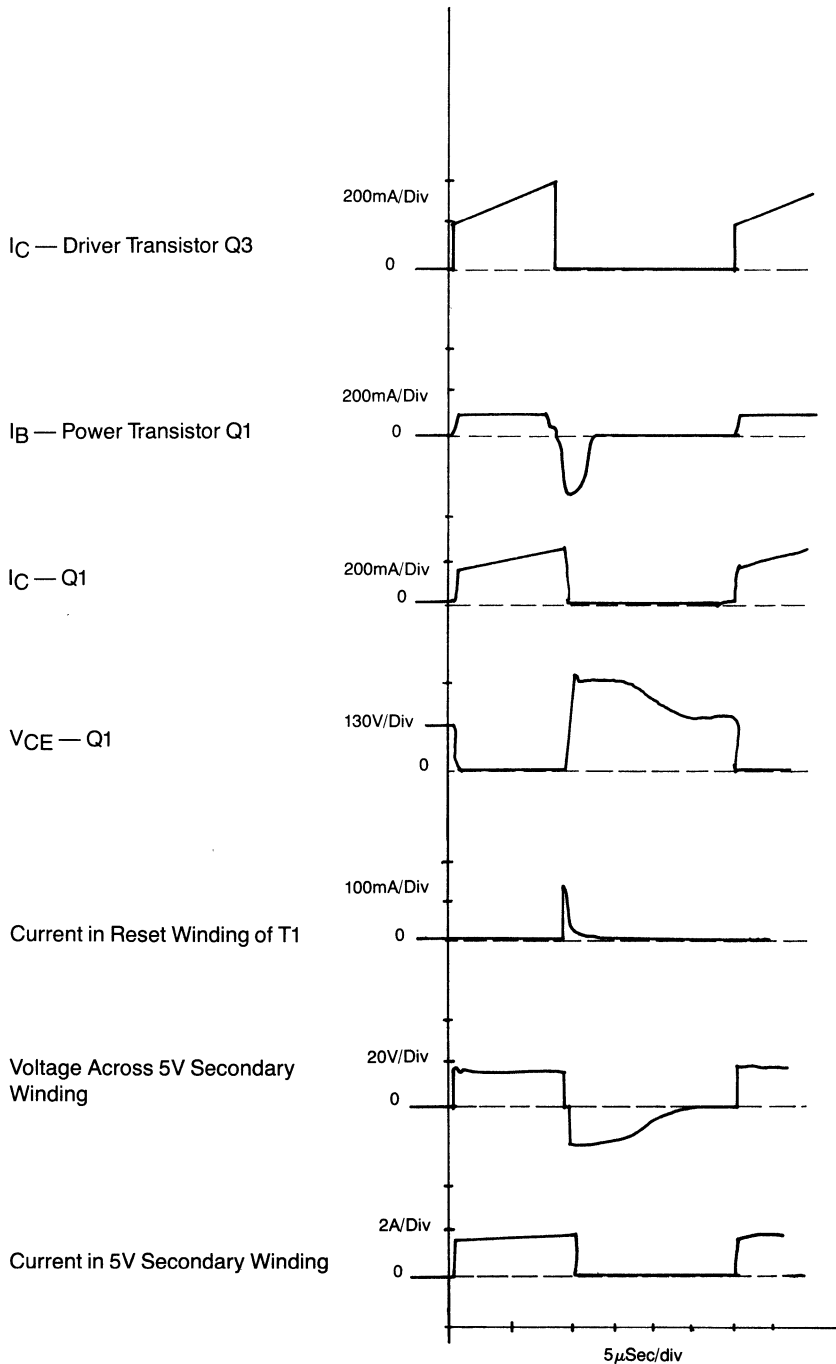
Short circuit protected

Soft Start



3.3 Schematic of Forward Converter

3.4 Waveforms



3.5 Power Transformer Design for Forward Converter

Use an EC-41-3C8 EE core (Ferroxcube).

$$N_p(\text{min}) = \frac{E_{in}(\text{high}) \times 10^8}{2f B_{\text{max}} A_e} = \frac{140\sqrt{2} \times 10^8}{2 \times 25\text{K} \times 3.3\text{K} \times 1.21} = 101 \text{ Turns (min)} \quad (1)$$

$$i_{\text{pri}} = \frac{P_o/V_{in}}{D.F. \times \text{Eff.}} = \frac{50\text{W}/165\text{V}}{0.45 \times 0.8} = 0.84\text{A}$$

For 15% current ramp in primary, $I_m = 0.15 \times 0.84\text{A} = 0.14\text{A}$

$$L_m = E_{in}(\text{high})/(di/dt) = 135\text{V}\sqrt{2}/(0.14/15\mu\text{S}) = 20\text{mH} \quad (2)$$

$$N_p(\text{min}) = \left(\frac{L_m \times 10^9}{A^2}\right)^{0.5} = \left(\frac{20 \times 10^6}{2800}\right)^{0.5} = 84 \text{ turns (min)} \quad (3)$$

From (1) and (3) use 120 turns.

Current density in primary; design for 3000A/sq. in. (max) (4)
 0.84/3000A/sq. in. = .00028 sq. in. (min)
 AWG#24 = .00032 sq. in.
 $A_w = 2.5(A_p \times N_p) \times 2 = 2.5(.00032 \times 120) \times 2 = 0.17 \text{ sq. in. needed.}$
 EC-41 has $A_w = 0.21 \text{ sq. in. available on bobbin.}$

For the 5V winding:

$$\frac{N_p}{N_s}(\text{max}) = \frac{E_{in}(\text{low}) - V_{CE(\text{SAT})}}{2(E_o + V_f + V_{RS})} = \frac{90\sqrt{2} - 1}{2(5 + 0.7 + 0.1)} = 10.9 \text{ (max); use 9:1 Turns Ratio.}$$

For the 15V Winding:

$$\frac{N_p}{N_s}(\text{max}) = \frac{90\sqrt{2} - 1}{2(15 + 0.7 + 0.1)} = 4.3:1 \text{ (max); use 4:1}$$

3.6 Parts List – 50W Forward Converter

IC1 – UC3524

Q1 – PIC811

Q2-3 – 2N2222

Q4 – UPT212

CR1-4 – 697-4

CR5-8 – 673-1

CR9 – UES1101

CR10 – UES1101

CR11 – UZ707

CR12 – UES2401

CR13-14 – UES1304

CR15-16 – UES1304

CR17 – UES1306

CR18 – UES1101

CR19 – UES1304

CR20 – UES1101

CR21-23 – UES1101

CR24-26 – 1N914

TI-4 – See Magnetics Sheet

LI-3 – See Magnetics Sheet

F1 – 2A AGC

C1 – 600μF, 250VDC

C2 – 5000μF, 10VDC

C3 – 1000μF, 25VDC

C4 – 1000μF, 25VDC

C5 – .001μF, 1KV disc ceramic

C7 – 47μF, 35V

C8 – 500μF, 50VDC

C9 – 0.1μF, 50V

C10 – .005μF, 50V disc

C11 – 100μF, 50VDC

C12 – .01μF, 50VDC disc

R1 – 27K, 2W

R2 – 2.2K, 2W

R3 – 27

R4 – 27

R5 – 47

R6 – 0.5

R7 – 33

R8 – 20K pot

R9 – 4.7K

R10 – 4.7K

R11 – 4.7K

R12 – 1K pot

R13 – 100K

R14 – 3.9K

R15 – 22K

R16 – 100

R17 – 330

3.7 Magnetic Components

T1 – Power Transformer

Core: EC-41-3C8 Core & Bobbin, Ferroxcube

120T	120T	13T	30T	30T
#24 AWG	#30 AWG	#20AWG	#20AWG	#20AWG
(PRI)	(RESET CORE)	(5V SEC)	(15V SEC)	(-15VSEC)

T2 – Base Drive Transformer

Core: 376 B/U 250-3C8 (UI Core), Ferroxcube

60T	60T	15T
#27 AWG	#30 AWG	#24 AWG
(PRI)	(RESET CORE)	(SEC)

T3 – Current Transformer

Core: 846T250-3C8, Ferroxcube

6T	6T	24T
#18 AWG	#18 AWG	#24 AWG
(PRI)	(SEC)	(SEC)

T4 – Isolation Transformer

Stancor PPC-2, 115V/15V, 0.1A

L1 – 5V Output Inductor

Core: 1F31-3C8, Ferroxcube

40T	6 mil air gap in each of the 2 legs.
#18 AWG	L1 = 600 μ H

L2 & L3, 15V Output Inductor

Core: 1F31-3C8, Ferroxcube L3 = L2 = 1.3mH

74T	6 mil air gap in each of the legs.
#18 AWG	

4. Off-Line Half-Bridge Converter Application

This portion of the application note discusses the design for an off-line half-bridge PWM converter supplying 100 watts to multiple outputs. Features include soft start and current limiting, and the PWM control circuit uses the UC3524 chip.

Proportional base drive and a special base drive circuit are used to reduce transistor storage time.

4.1 Circuit Description (see Fig. 4.3)

The half-bridge type circuit was chosen for the 100 watt converter design, along with the PIC810 hybrid and fairly simple circuits. The half bridge circuit keeps the transistors' collector voltage, including inductive spikes, from exceeding the DC bus voltage, and the series capacitor C6 prevents core saturation. The base drive circuit is designed to minimize transistor storage time by essentially shorting the primary of the driver transformer T1 during transistor dead-time, providing a low impedance path for I_{B2} of the transistors. This is accomplished by turning on both Q21 and Q22 during the dead-band period. In addition proportional base drive is used.

Soft start capacitor C26 is at zero volts when the power supply is turned on, and CR24 keeps pin 9 at 0.7V more positive than the voltage on C26, which is being charged slowly by R27. The maximum pulse width is set by potentiometer R26 and CR23.

4.2 Specs for Half-Bridge Converter

Input – 95V to 135V, 60Hz

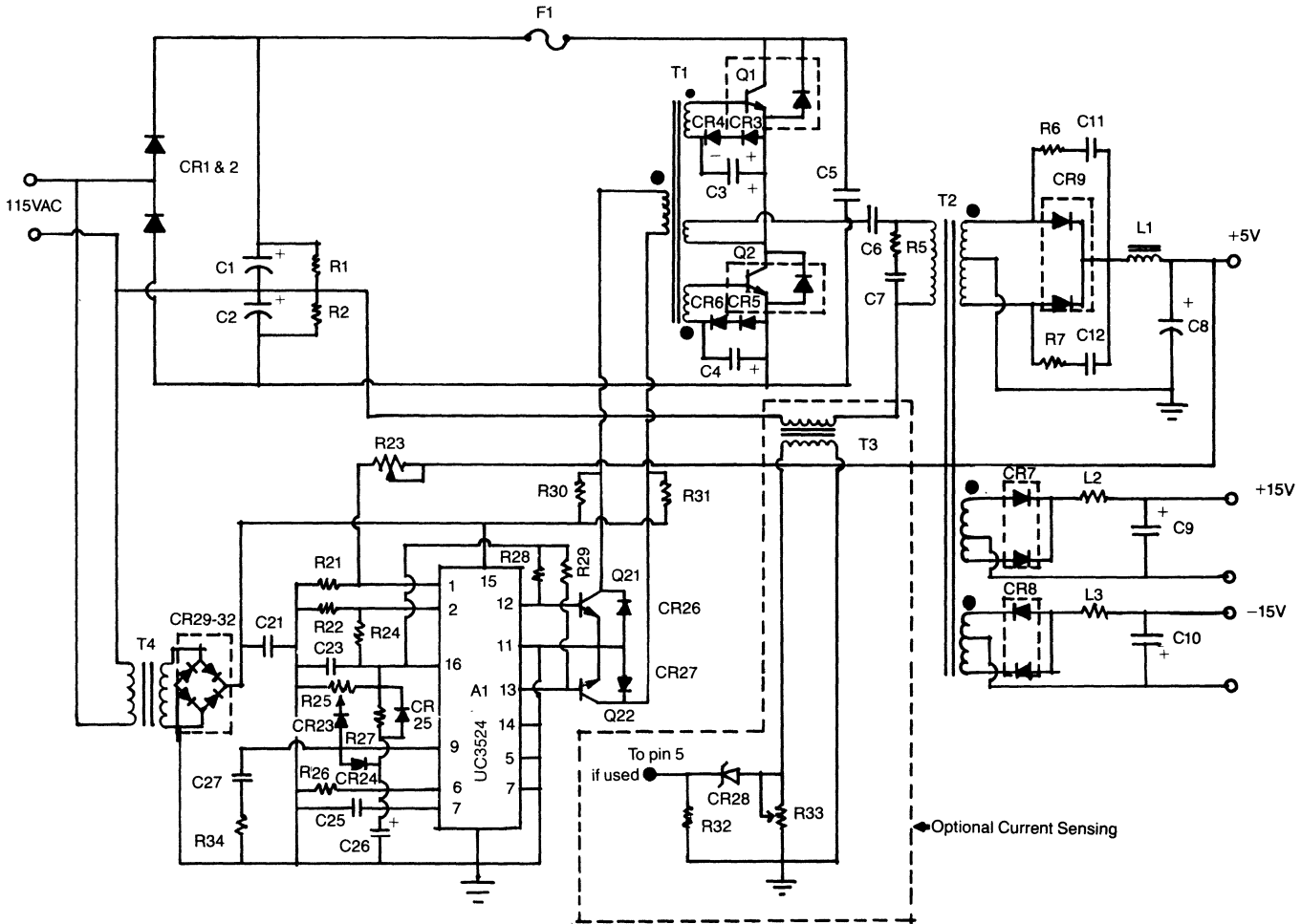
Outputs – 5V @ 15A, $\pm 15V$ @ 1A

Regulation – Line: 0.3% for specified AC input
Load (20% to 100%): 5V output, 0.5%; $\pm 15V$, 2%.

Ripple and Noise – 5V output, 80mV peak to peak.
– $\pm 15V$ output, 20mV peak to peak.

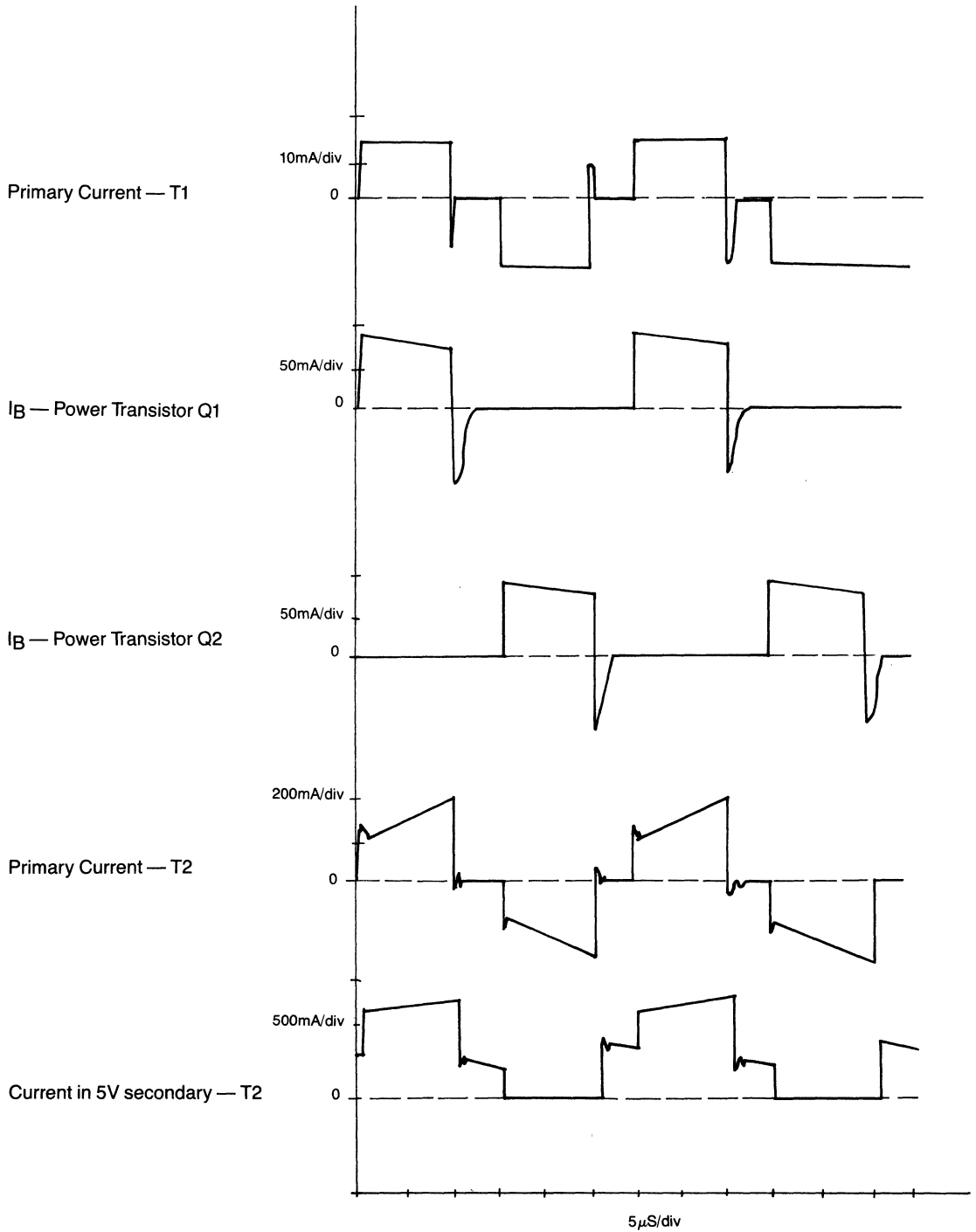
Frequency – 30KHz

Efficiency – 80%



4.3 Schematic of 100W Off-Line Half-Bridge Converter

4.4 Typical Waveforms for Half-Bridge Converter



4.5 Power Transformer Design for Half-Bridge

Use EC35-3C8 core and bobbin (E-E configuration)

$$\begin{aligned} N_p(\text{min}) &= \frac{E_{in}(\text{max}) \times 10^8}{4f B_{\text{max}} A_e} \\ &= \frac{135\sqrt{2} \times 10^8}{4 \times 30\text{K} \times 3.3\text{K} \times 0.843} \\ &= 57 \text{ turns (min)}. \end{aligned}$$

$$i_{\text{pri}} = \frac{P_o/V_{in}}{\text{DF} \times \text{Eff.}} = \frac{100/165}{0.5 \times 0.8} = 1.52\text{A}$$

For 25% current ramp in primary:

$$I_m = 0.25 \times i_{\text{pri}} = 0.25 \times 1.52 = 0.38\text{A}$$

$$L_m = \frac{E_{in}(\text{max})}{I_m/\text{ton}} = \frac{135\sqrt{2}}{(0.38/12\mu\text{S})} = 5.9\text{mH}$$

$$\begin{aligned} N_p(\text{min}) &= \left(\frac{L_m \times 10^9}{A_L} \right)^{0.5} = \left(\frac{5.9 \times 10^6}{1500} \right)^{0.5} \\ &= 63 \text{ turns (min)} \end{aligned}$$

For the 5V winding:

$$\begin{aligned} \frac{N_p(\text{max})}{N_s} &= \frac{E_{in}(\text{min}) - V_{CE(\text{SAT})}}{E_o + V_F + V_{RS}} \times \frac{T - 2T_{\text{db}}}{T} \\ &= \frac{90\sqrt{2} - 1}{5 + 0.8 + 0.4} \times \frac{33 - 2}{33} \\ &= 19.1 \text{ (max)} \end{aligned}$$

63T/19.1 = 3.3T; use 4 turns

For the 15V winding:

$$\frac{N_p(\text{max})}{N_s} = \frac{90\sqrt{2} - 1}{15 + 0.8 + 0.4} \times \frac{33 - 2}{33} = 7.3 \text{ (max)}$$

19.1/7.3 = 2.62, $2.62 \times 4T = 10.48T$; use 11 turns.

For primary use $4 \times 18 = 72$ turns.

Design for current density of 3000A/sq. in. (max).

$A_p(\text{min}) = i_{\text{pri}}/\text{max density} = 1.52/3000 = .00050$ sq. in; use #22 AWG = .00050 sq. in.

$AW = 2.5(A_p \times N_p) \times 2 = 2.5(.00050 \times 72) \times 2 = 0.17$ sq. in. needed. EC35 bobbin has 0.16 sq. in. available. (The first factor of 2.5 is for efficiency of using winding area, the second 2 is for equal primary and secondary winding area).

4.6 Inductor for 5V Output

Selecting an inductor core can be done by first calculating the $A_e A_c$ product (magnetic core area \times window winding area) from the known requirements, and then choosing an inductor with an $A_e A_c$ product that is equal or larger.

Using MPP (Magnetics Inc) core material;

$$A_e A_c = \frac{(100/k) (L I_{\text{max}} A_t) \times 10^8}{B_{\text{max}}}$$

Where k is usable winding area of core in %, and A_t is cross sectional area of wire in sq. cm.

$$\begin{aligned} &= \frac{(100/75) (70\mu \times 15 \times 0.033) \times 10^8}{2000} \\ &= 2.09 \text{ cm}^4 \text{ needed} \end{aligned}$$

Referring to the manufacturer's data sheet, the 55543-A2 core has an $A_e A_c = 0.67 \times 3.1 = 2.1 \text{ cm}^4$, which is sufficient.

$$\begin{aligned} (A_t &= 15\text{A}/3000\text{A/sq. in.} = .005 \text{ sq. in.} \\ &= .033 \text{ sq. cm}) \end{aligned}$$

$$\begin{aligned} \text{Then } N &= 1000\sqrt{L/L_{1000}} = 1000\sqrt{70\mu\text{H}/305\text{mH}} \\ &= 15 \text{ Turns} \end{aligned}$$

4.7 Magnetics:

Driver Transformer T1

Core: Ferroxcube 2213 P3B7

(1-2) 75 turns, #26 wire

(3-4) (4-5) 12 turns, Bifilar, #24 wire

(6-7) 2 turns, #19 wire

Power Transformer T2

Core: Ferroxcube EC35-3C8 (E-E)

(1-2) 72 turns, #22 wire

(3-4) (4-5) 4 turns, Bifilar, #16

(6-7) (7-8) 11 turns, Bifilar, #18

(9-10) (10-11) 11 turns, Bifilar, #18

Current Transformer T3

Core: Magnetics, Inc. #52056-ID

(1-2) 1 turn, primary winding through core.

(3-4) 34 turns, #24 wire

Filter Inductors

L1

Core: Magnetics, 55543-A2

15 Turns, #12 AWG

L2, L3

Core: Ferroxcube 1F31-3C8

74 turns, #18 AWG

*4.8 Electrical Parts List**Semiconductors*

A1 – UC3524
 Q1, Q2 – PIC810
 Q21, Q22 – UPT212

CR1, CR2 – 1N5551
 CR3,4,5,6 – 1N4001
 CR7,8 – UES2401
 CR9 – SD241
 CR21-27 – SES5001
 CR28 – 1N4461
 CR29-32 –673-1 Bridge

Resistors

R1, R2 – 10K, 2W
 R5 – 3 Ω , 5W
 R6, R7 – 6.8 Ω , 2W
 R21, R22, R24 – 5.1K
 R25 – 1K, $\frac{3}{4}$ W, Trim Pot
 R28, R29 – 510 Ω , $\frac{1}{2}$ W, 5%*
 R30, R31 – 1K Ω
 R32 – 1K
 R33 – 200 Ω , $\frac{3}{4}$ W, Trim Pot
 R34 – 20K
 R27 – 100K
 R26 – 3.9K
 R23 – 20K Trimpot

*Adjust for symmetrical base pulses.

All resistors $\frac{1}{2}$ W, 5% unless otherwise noted.

Capacitors

C1, C2 – 430 μ F, 200V
 C3, C4 – 22 μ F, 6V
 C5, C6 – 2 μ F, 400V
 C7 – 0.001 μ F, 1KV
 C8 – 5000 μ F, 10V
 C9, C10 – 1000 μ F, 25V
 C11, C12 – 0.1 μ F, 100V
 C23 – 0.1 μ F, 25V
 C27 – 0.1 μ F, 100V
 C25 – .005 μ F, 100V
 C26 – 100 μ F, 12V
 C21 – 500 μ F, 25V

Magnetics

L1, L2, L3 – Filter Chokes
 T1 – Driver Transformer
 T2 – Power Transformer
 T3 – Current Transformer
 T4 – Stancor PPC-2, 115V/15V, 0.1A

Other

F1 Fuse – 2A-3AG

DESIGN GUIDE — POWER SCHOTTKY RECTIFIERS IN A SWITCHING REGULATOR

1. Introduction

Present technology is stimulating the development of more efficient power supplies. The switching regulated power supply is fast becoming the most popular type especially in industrial and military applications because it offers higher efficiency than a linear power supply.

Schottky rectifiers are widely used in switched-mode converters due to their inherently lower forward voltage characteristics compared with PN junction devices. Losses in the power supply are reduced considerably by the use of Schottky rectifiers, resulting in increased efficiency, improved reliability, and reduced size, weight and cost of the switched-mode converter.

In a +5V T²L logic power supply, the efficiency of a switched-mode converter is reduced 11 to 15% due to rectifier losses. The trend is for information processing circuits to be operated at even lower voltages, making the forward characteristic of a Schottky rectifier even more important.

Since the Schottky rectifier is a majority carrier device, there is no reverse recovery characteristic caused by minority carrier storage when the devices switch from forward conduction to the blocking state. However, due to the large junction capacitance, Schottky rectifiers will exhibit reverse recovery time like a fast PN junction rectifier.

This application note describes, in brief, the theory of Schottky rectifiers and compares Schottky rectifier characteristics using different barrier metals and their effects on switching regulator efficiency.

The discussion also covers the parasitic elements in the Schottky rectifier and considers the effects of these elements in switched-mode converters. Design rules are derived for optimum snubber networks to protect against transient voltages and minimize RFI. Guidelines are provided for selecting the proper Schottky rectifier for different types of switched-mode converters.

2. Basic Structure

The basic construction of a Schottky rectifier is shown in Figure 1. The starting material is a heavily doped N⁺ silicon wafer on which an N-type epitaxial layer is deposited. The resistivity of this layer determines the reverse blocking voltage capability of the rectifier. The Schottky barrier is formed by depositing a metal layer on the N-type epitaxial layer, and the junction formed between the metal and the semiconductor is an abrupt junction.

The most commonly used barrier metals or alloys are chromium, platinum, nickel platinum, molybdenum tungsten. A performance comparison of different barrier metals is summarized in Table 1. The chromium barrier provides low forward voltage with a very high leakage current. However, the tungsten barrier provides low leakage current with high forward voltage. Since efficiency is a major consideration in switched-mode converters, the nickel platinum barrier provides the best choice due to its low forward drop with a minimum of leakage current.

3. Theory And Discussion of Parasitic Elements in a Schottky Rectifier

The energy bands of a metal and semiconductor separated by a vacuum are shown in Figure 2a. This system is not in equilibrium. However, if an electrical connection is made between the semiconductor and metal, charge is allowed to flow from the semiconductor to the metal. Equilibrium will be established and the Fermi levels will become aligned.

When intimate contact is made between the metal and semiconductor, Figure 2b, the Fermi levels will line up and there will be an accumulation of positive charges at the surface of the semiconductor. A barrier will exist for electron flow from the metal to semiconductor and the barrier height will be the difference between the work function of the metal and the semiconductor.

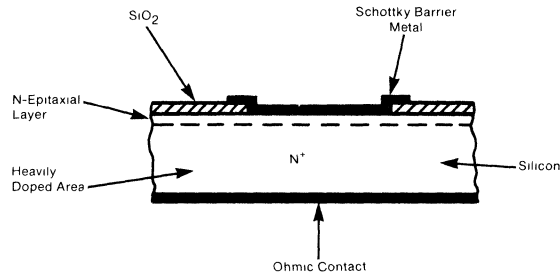


Figure 1 - Cross-Section of a Schottky Barrier Power Rectifier

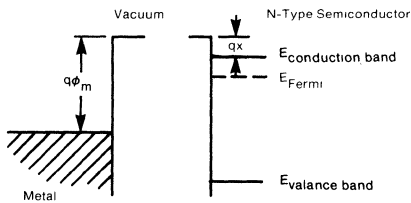


Figure 2a

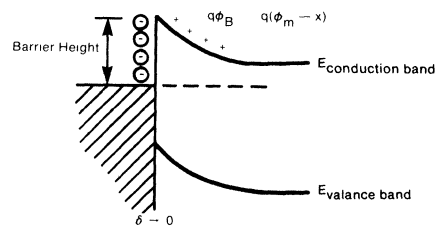


Figure 2b

Figure 2 - Energy Band Diagram of Metal Semiconductor Contact

TABLE 1 — PERFORMANCE COMPARISON OF DIFFERENT BARRIERS

SPECIFICATIONS			POWER LOST IN EACH RECTIFIER		
METAL BARRIER	V _F @ 20A (V) 125° C**	V _F @ 100A (V) 125° C**	LEAKAGE CURRENT (mA) 125° C**	LOSSES DUE TO LEAKAGE (W)*	V _F LOSSES @ 100A (W)*
Chromium	0.35	0.78	280	1.80	33.20
Molybedeum	0.45	0.75	65	0.46	34.07
Platinum	0.51	0.80	10	0.071	35.23
Ni-Platinum	0.433	0.73	30	0.2145	32.70
Tungsten	0.51	0.82	10	0.071	36.79

* Power dissipation calculations are based on 125° C operating junction temperature and a high line input voltage for an off-line PWM converter.

** V_F voltages are for 160 mil² die.

3.1 Forward Biased Junction

When the barrier or a junction is forward biased, the energy level of the conduction band in the semiconductor is raised, which allows electrons to flow into the metal as shown in Figure 3a. A small barrier does remain, but the electron energy distribution is sufficient to overcome this remaining barrier. Increased forward bias will overcome the barrier and current flow will be limited only by the series resistance of the device. Most of the forward drop at high current occurs in the high resistivity epitaxial layer which determines the reverse blocking voltage capability.

Schottky rectifier forward drop can be expressed by the following equation:

$$V_F = \frac{\Phi}{q} + \frac{KT}{q} \ln \left(\frac{I_F}{A \times RT^2} \right) + \frac{I_F \cdot \rho \cdot d}{A} \quad (3.1)$$

+ Voltage drop in ohmic contact of package

Where: I_F = Forward current (A)

A = Barrier area (cm²)

$\frac{KT}{q}$ = 0.026 at room temperature

Φ = Barrier height - e_v

ρ = Resistivity of epitaxial layer (Ω-cm)

d = Thickness of epitaxial layer (cm)

R = Richardson constant

T = Absolute temperature (°K)

The term [I_F · ρ · (d/A)] in the above equation is the forward drop in the high resistivity epitaxial layer and it is a significant portion of the forward drop at high current levels.

Since holes cannot exist in the metal, none can be injected into it. As a result, conduction is entirely due to electrons. This eliminates the minority carrier related reverse recovery time.

3.2 Reverse Biased Junction

When the device is reverse biased, the conduction band in the semiconductor is lowered by the applied reverse biased voltage as shown in Figure 3b. For any conduction to occur, electrons must surmount the potential barrier created at the metal-semiconductor junction. Some electrons in the metal gain sufficient thermal energy from the lattice structure to overcome the barrier while others are able to tunnel through the barrier. This leakage current is temperature dependent.

3.3 Junction Capacitance

The barrier metal and uniformly doped N-type epitaxial layer create an abrupt junction. This results in at least 5 times higher junction capacitance when compared with similar slightly graded ultra-fast PN junction devices. The depletion capacitance of a Schottky rectifier under reverse biased conditions can be expressed by the equation:

$$C = A \cdot \sqrt{\frac{(43 \cdot 10^{-6})N_D}{V_R + 0.6 + (KT/q)}} \quad (3.2)$$

Where: N_D = Carrier concentration of an epitaxial layer

$\frac{KT}{q}$ = 0.026 at room temperature

V_R = Applied reverse biased voltage

As can be seen from the equation, the junction capacitance is inversely proportional to the square root of the applied reverse voltage and is practically independent of temperature at reverse voltages greater than 1V. When the device switches from forward biased condition to the reverse blocking state, current is required to charge the depletion capacitance. The time required to charge up capacitance is determined by the circuit impedance. This charging current has the same effect as the reverse recovery current of a Unitorde fast recovery "UES" PN junction rectifier!

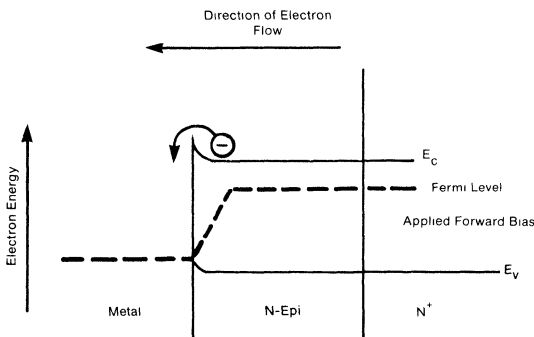


Figure 3a - Rectifier — Forward Biased

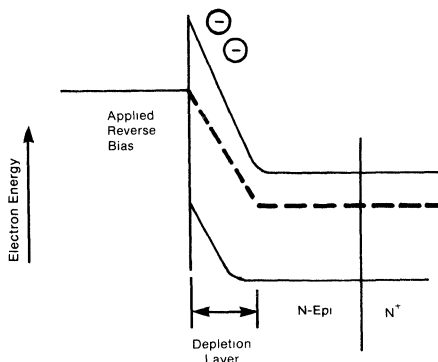


Figure 3b - Rectifier — Reverse Biased

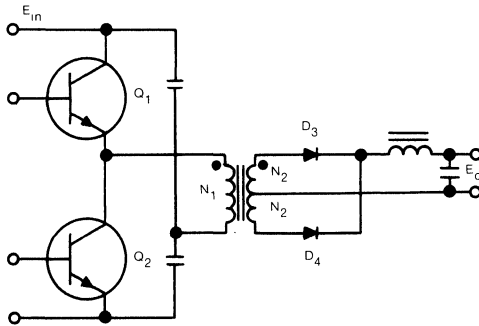
In a switched-mode converter, the apparent reverse recovery time is determined by the leakage inductance of the transformer and the junction capacitance of the Schottky rectifier. Since capacitance does not vary with temperature, the apparent recovery time and current overshoot remain constant with temperature. Ringing resonance of leakage inductance and Schottky capacitance can cause voltage overshoot. In a high frequency switched-mode converter where the transformer is designed with very low leakage inductance, careful consideration must be given in selecting the Schottky rectifier because of dv/dt limitations.

4. Applications of a Schottky Rectifier in Switched-Mode Converters

The simplified power output stage of a half-bridge switched-mode converter is shown in Figure 4a. When switching transistors Q_1 and Q_2 are in the "off" condition, diodes D_3 and D_4 conduct in the forward direction to provide a current path for inductor L_1 . Each diode carries half of the load current. When transistor Q_1 turns on, current in diode D_3 starts to change from half the load current to full load current, while current in diode D_4 starts to change from half the load current into the "off" condition. Current transition time in the rectifier will depend on the current rise time of the transistor and the leakage inductance of power transformer T_2 . When current in rectifier D_3 increases to full load current, current in rectifier D_4 decreases to zero.

Since a Schottky rectifier is a majority carrier device, it should turn off instantaneously. However, because of the larger junction capacitance of the Schottky rectifier compared with PN junction devices, transistor Q_1 supplies additional current to the secondary winding to charge up this larger junction capacitance. Note that the junction capacitance of the Schottky rectifier varies with reverse bias voltage as shown in Figure 5. Also the capacitance is five times that of equivalent PN junction devices.

As current is increased, the voltage across the junction capacitance of the rectifiers builds up toward the full reverse blocking state. The primary current will be higher than the output load current divided by the transformer turns ratio. During this period, energy is stored in the leakage inductance due to the excessive current on the primary side. As the



- $\frac{N_1}{N_2}$ = N, transformer turns ratio
- R_{PW} = Series resistance of primary windings
- R_{SW} = Series resistance of one half secondary winding
- L = Leakage inductance of transformer
- C_{PW} = Primary windings distributed capacitance
- C_{SW} = One half secondary winding capacitance
- C_{ob} = Output capacitance of switching transistor
- C_j = Junction capacitance of rectifier

Figure 4a - Typical Half-Bridge PWM Switching Converter

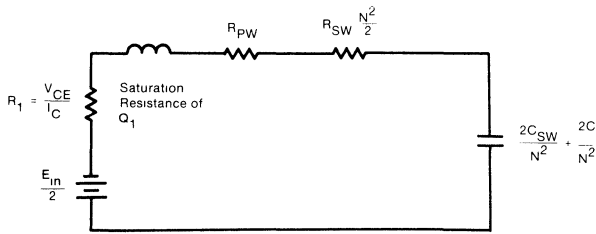


Figure 4b - Equivalent Circuit During Charging of a Junction Capacitance of a Schottky

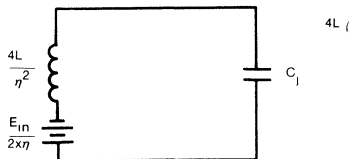


Figure 4c - Simplified Equivalent Circuit Referred Back to Secondary Side

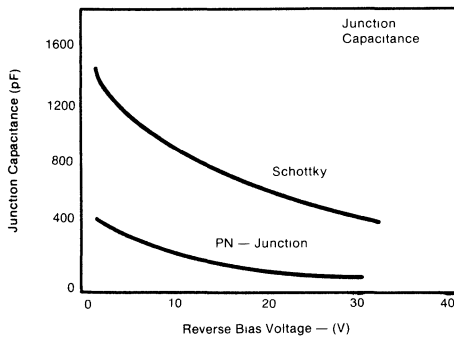


Figure 5 - Comparison of Junction Capacitance ultra-fast PN-Junction vs. Comparable Schottky Rectifier

voltage across the rectifier reaches full switching voltage, energy stored in the leakage inductance continues to charge up the junction capacitance of the rectifier above the switching voltage reflected back in the secondary. These voltages can force the device into the breakdown region if the proper snubber circuit is not employed.

4.1 Snubber Network Design

The equivalent circuit referred back to the primary side when the junction capacitance is charging up is shown in Figure 4b. The junction capacitance of the Schottky and the leakage inductance of transformer T₂ form a resonant circuit. The winding resistances, R_{PW} and R_{SW}, and saturation resistance, R₁, provide very little damping to this LC tuned circuit. Therefore, its effect on damping can be neglected. The interwinding capacitance of the power transformer is much lower than the junction capacitance of the Schottky rectifier and may be neglected. The simplified circuit referred back to the secondary side is shown in Figure 4c.

Since Schottkys are prone to excessive heating and possible damage in the breakdown mode, a proper snubber is required. The design of the snubber network minimizes voltage spikes and snubber losses. The snubber network also helps to reduce conducted and radiated RFI.

The optimum snubber network should be designed on the basis of critical damping of the LC tuned circuit and limiting the maximum excursion of the voltage below the PIV ratings of the rectifier.

Shown below is the LC tuned circuit with resistor R_{snb} paralleled across the junction capacitance of the Schottky rectifier for a critically damped condition.

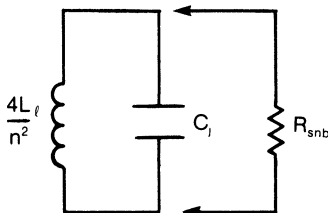


Figure 6 - Damping Resistor R_{snb} Added Across the LC Tuned Circuit for Critical Damping

The loaded Q_L should be 0.5 for a critically damped case to prevent any ringing of the voltage and to provide minimum losses in the snubber resistor. LC tuned circuits will have only real roots. Loaded Q_L can be described by the equation:

$$Q_L = 0.5 = \frac{R_{snb}}{X_L} \tag{4.1}$$

Where: $X_L = j\omega L$

$$\begin{aligned} \therefore R_{snb} &= 0.5 \cdot \omega \cdot L \\ &= 0.5 \left(\frac{1}{\sqrt{(4L_l/n^2)C_1}} \right) \left(\frac{4L_l}{n^2} \right) \\ R_{snb} &= \frac{1}{n} \sqrt{\frac{L_l}{C_1}} \end{aligned} \tag{4.2}$$

Where: C₁ = Junction capacitance of rectifier
L_l = Leakage inductance of power transformer

A capacitor is required in series with the resistor in order to block the dc voltage present. The blocking capacitor should be at least ten times the rectifier junction capacitance:

$$C_{snb} = 10(C_1) \tag{4.3}$$

To transfer the power effectively from the input power source to the output load, the time constant (R_{snb} x C_{snb}) should at at most one-tenth the minimum pulse width of the switched-mode converter. This occurs at maximum input voltage. Therefore:

$$R_{snb} \cdot C_{snb} \leq \frac{(1/20)}{f} (E_{in_{min}}/E_{in_{max}}) \tag{4.4}$$

Where: f is the operating frequency of the switching regulator.

The power dissipation in the snubber resistor R_{snb} can be calculated by the equation:

For Half-Bridge:

$$P_{R_{snb}} = \frac{1}{2} C_{snb} \left[\frac{E_{in_{max}}}{n} \right]^2 \cdot f \tag{4.5}$$

For Push-Pull for Full-Bridge:

$$P_{R_{snb}} = \frac{1}{2} C_{snb} \left[\frac{2(E_{in_{max}})}{n} \right]^2 \cdot f \quad (4.6)$$

Where: $E_{in_{max}}$ = Maximum input voltage
 n = Primary to secondary turns ratio of power transformer

Every inch of wire represents 20 nanohenries of inductance. When the output current is high, the energy stored in the lead and package inductance in the secondary circuit can generate high voltage spikes across the rectifier during reverse recovery time. To reduce these spikes, two snubber networks are required. One should be placed across each Schottky rectifier as shown in Figure 7 below.

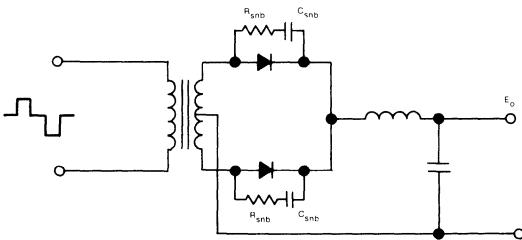


Figure 7 - High Current Outputs

For low current outputs, the snubber network can be connected across the secondary winding as shown in Figure 8.

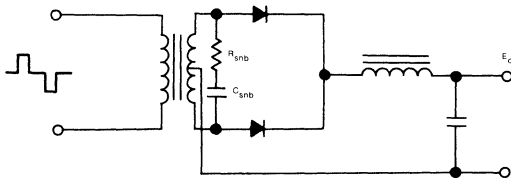


Figure 8 - Low Current Outputs

4.2 Reverse Recovery Time and Overshoot Current, $I_{RM(REC)}$

Reverse recovery time is defined as the time required to change a rectifier from the forward conduction state to the reverse blocking state. Although a Schottky rectifier is a majority carrier device, it takes

time to "recover" because of its high junction capacitance. In a switched-mode converter, reverse recovery time is, to a large extent, determined by the parasitic leakage inductance of the transformer which resonates with the junction capacitance of the Schottky rectifier. Design equations for reverse recovery time and current overshoot can be derived as shown below.

Reverse Recovery Time:

From basic equations of an LC tuned circuit:

$$\omega = \sqrt{\frac{1}{LC}}$$

Substituting $f = 1/\tau$ and rearranging:

$$\tau = 2\pi\sqrt{LC}$$

Since $\tau/2 = t_{rr}$ by definition:

$$t_{rr} = \pi\sqrt{LC} \quad (4.7)$$

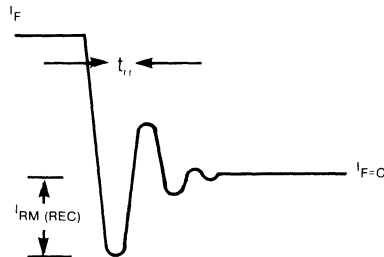


Figure 9 - Reverse Recovery Time of a Rectifier

Assuming the rise time of the transistor is much faster than t_{rr} of the rectifier, and substituting $L_l =$ leakage inductance of the transformer and $C_j =$ junction capacitance of the Schottky rectifier. Neglecting the interwinding capacitance of the transformer, the reverse recovery time (when no snubber network is employed across the rectifier) can be calculated by the equation:

t_{rr} , due to junction capacitance:

$$t_{rr} = \frac{2\pi}{n} \sqrt{L_l(C_j)} \quad (4.8)$$

Where: n = Primary to secondary turns ratio

The ringing frequency can be calculated by the equation:

$$f = \frac{n}{4\pi\sqrt{L_l(C_T)}} \quad (4.9)$$

From the characteristic impedance of the LC tuned circuit, overshoot current, I_{RM} , in the Schottky rectifier can be calculated by:

$$I_{RM(REC)} = \frac{E_{in}}{2} \sqrt{\frac{C_j}{L_l}} \quad (4.10)$$

4.3 Practical Example

A detailed diagram of a 150W, multiple output switching regulated power supply is shown in Figure 10. The power supply is designed to operate with a line input voltage of 117V ac, 60 Hz or 220V ac, 50 Hz. The regulated output voltages are +5V @ 1A, +12V @ 1.2A, -12V @ 1A and -5V @ 1A. The output voltage is regulated by power switching hybrid circuits Q_1 and Q_2 which are housed in four pin electrically isolated packages.

Since the case is electrically isolated from the active devices, it provides the following advantages:

- lower conducted and radiated RFI
- ease in mounting — two devices can be mounted on the same heat sink.

The selected switching transistor provides fast switching time (<100ns) and the diode in the hybrid circuit provides low reverse recovery (<50ns) and forward recovery time. The proportional base current to the switching transistor is supplied by the current transformer T_1 .

One of the output voltages (+5V) is regulated with a pulse width modulated (PWM) control chip Unitrode's UC3524. The auxiliary voltage to power the control circuit should be electrically isolated from the line voltage. Conventionally, the 60 Hz transformer is utilized to provide isolation and the transformer output voltage is rectified and regulated to supply bias voltage to the control circuit. Transistors, Q_3 and Q_4 , provide a low cost approach in developing bias voltage for the control circuit without the use of a 60 Hz transformer. The operation of the circuit is described in detail below.

When the 117V ac input line voltage is applied to the switched-mode converter, capacitors C_1 and C_2

charge up to full input voltage. Meanwhile capacitor C_T charges up slowly through resistor R_T . When the voltage across C_T reaches the anode-gate voltage of the programmable unijunction transistor Q_4 , it will turn on and dump the stored charge from capacitor C_T into one of the proportional base drive windings of the transformer T_1 . The polarity of the windings is such that it will turn on only transistor Q_2 , transferring energy from input capacitor C_2 into the output capacitor C_3 (isolated from the input line) through power transformer T_2 . The control circuit LM3524 starts to switch transistor Q_2 . At the instant when transistor Q_2 turns on, capacitor C_T will be isolated from current transformer T_1 with the help of transistor Q_3 . The programmable unijunction transistor Q_4 now remains off. The capacitor C_3 is now continuously charging up through the secondary winding of the transformer.

The output circuit of the switched-mode converter utilizes coupled inductor L_1 to provide better tracking among all the output voltages, improve transient response and reduce the minimum loading requirement. Coupled inductor L_2 (which is not in the control loop) maintains the sawtooth current in the +5V winding of L_1 (which is in the control loop) providing stability in the control circuit.

Calculations of Snubber Network:

In the 150W switching regulator shown in Figure 10, first calculate the current overshoot $I_{RM(REC)}$, the ringing frequency and the apparent reverse recovery time without the snubber network. Then determine the resistor and capacitor values (for critically damped case) of the network across the Schottky rectifier.

Given: L_l , Leakage inductance of power transformer = 22 μ H

C_j , Junction capacitance of Schottky = 850pF

f , Operating frequency = 30 KHz

n , Primary to secondary turns ratio = 14

E_{inmin}/E_{inmax} , Ratio of maximum input voltage to minimum input voltage = 400/200 = 2

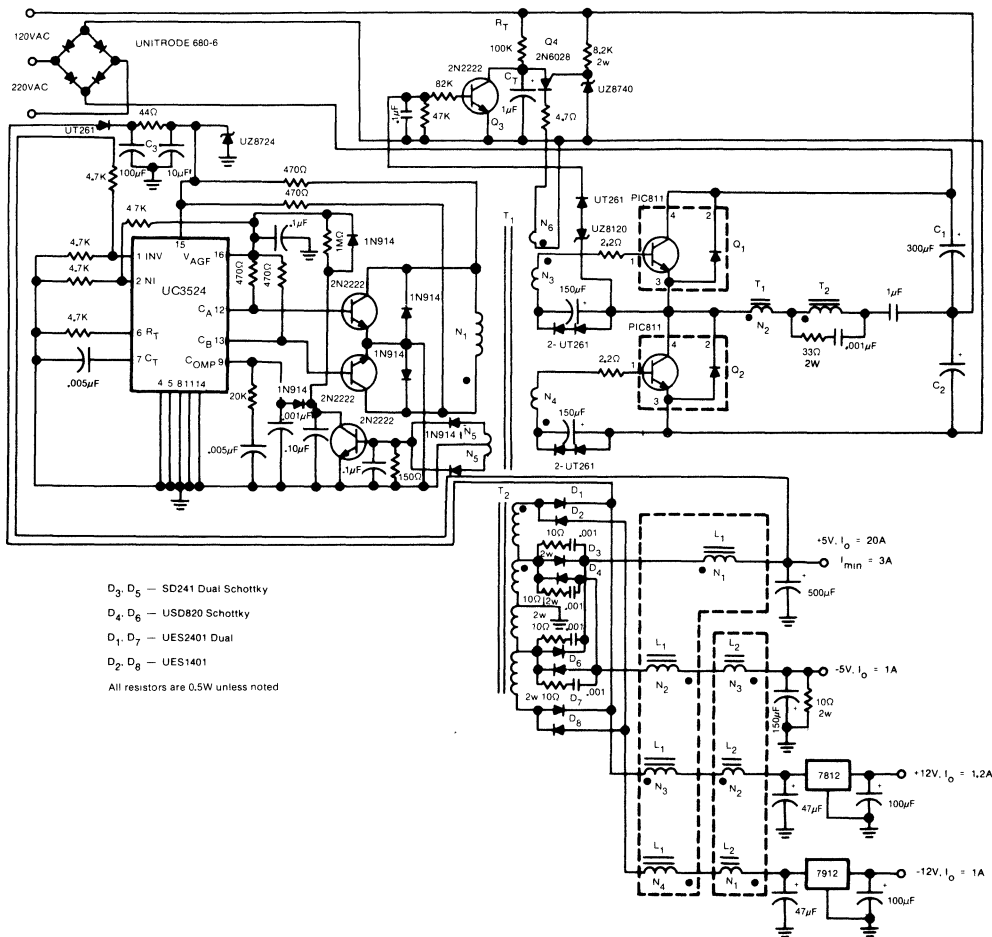


Figure 10 - 150 Watt Multiple Output "OFF Line" Switched-Mode Converter

Solution:

Current overshoot, $I_{RM(REC)}$, from Equation 4.10:

$$\begin{aligned} I_{RM(REC)} &= \frac{E_{in}}{2} \sqrt{\frac{C_j}{L_\ell}} \\ &= \frac{320V}{2} \sqrt{\frac{850 \times 10^{-12}}{22 \times 10^{-6}}} \\ &= 1A \end{aligned}$$

The ringing frequency from equation 4.9:

$$\begin{aligned} f &= \frac{n}{4\pi \sqrt{L_\ell (C_j)}} \\ &= \frac{14}{4\pi \sqrt{(22 \times 10^{-6}) (850 \times 10^{-12})}} \\ &= 8.1 \text{ MHz} \end{aligned}$$

The apparent reverse recovery time from equation 4.8:

$$\begin{aligned} t_{rr} &= \frac{2\pi}{n} \sqrt{C_j (L_\ell)} \\ &= \frac{2\pi}{14} \sqrt{(850 \times 10^{-12}) (22 \times 10^{-6})} \\ &= 67\text{ns} \end{aligned}$$

The value of the snubber resistor from Equation 4.2:

$$\begin{aligned} R_{snb} &= \frac{1}{n} \sqrt{\frac{L_\ell}{C_j}} \\ &= \frac{1}{14} \sqrt{\frac{22 \times 10^{-6}}{850 \times 10^{-12}}} \\ &= 10.9\Omega \end{aligned}$$

The value of the snubber capacitor from Equation 4.3:

$$\begin{aligned} C_{snb} &= 10(C_j) \\ &= 10(850 \times 10^{-12}) \\ &= 0.01\mu\text{F} \end{aligned}$$

The power dissipation in snubber resistor, R_{snb} , from Equation 4.5:

$$\begin{aligned} PR_{snb} &= \frac{1}{2} C_{snb} \left[\frac{E_{in_{max}}}{n} \right]^2 \cdot f \\ &= \frac{1}{2} (0.01 \times 10^{-6}) \left[\frac{400}{14} \right]^2 \cdot 30 \times 10^3 \\ &= 0.121W \end{aligned}$$

∴ The snubber resistor R_{snb} should have at least 0.5W rating.

The criteria for the snubber network should satisfy the conditions below:

$$R_{snb} (C_{snb}) \leq \frac{1}{20f} \left[\frac{E_{in_{min}}}{E_{in_{max}}} \right]$$

$$10\Omega (0.01 \times 10^{-6}) \leq \frac{1}{20(30 \times 10^3)} \cdot \frac{1}{2}$$

$$0.1\mu\text{s} \leq 0.993\mu\text{s}$$

The voltage across the Schottky rectifier with and without the snubber network in a 150W off-line switched-mode converter is shown in Figures 11a and 11b. Note that the voltage across the Schottky rectifier with a snubber network has no voltage overshoot. Thus, it prevents failure of the Schottky due to large voltage transients during transistor turn-on. The ringing frequency is about 10 MHz without the snubber and is close to calculated values.

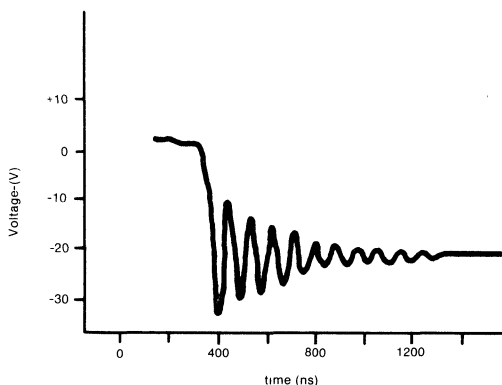


Figure 11a - Voltage Across Rectifier Without Snubber Network

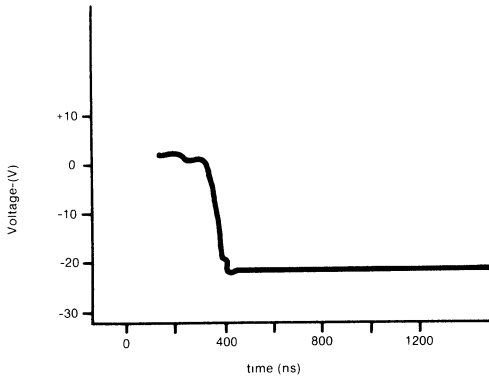


Figure 11b - Voltage Across Rectifier With Snubber Network
10Ω - 0.1μF

4.4 Thermal Stability Considerations

The reverse leakage current of a Schottky rectifier is much higher than PN junction devices because of the Schottky's lower barrier height. The magnitude of this leakage current doubles approximately every ten degrees Centigrade. Since it is temperature sensitive, the thermal stability of the system should be checked over to avoid thermal runaway. In a PWM switched-mode converter (i.e. push-pull, half-bridge, etc.) the rectifier can be operated at 50% duty cycle in the reverse blocking state while the remaining 50% of the time it will operate in the forward conduction mode under worst case conditions. However, forward drop is also a temperature sensitive parameter and this should also be considered when thermal stability calculations are made.

The criteria for thermal stability is defined as: "the rate of change in power pumped into a device with respect to temperature (dP_{in}/dt) should be less than the rate of change in power removed (in the applicable thermal environment) in the form of heat from the device with respect to temperature (dP_{out}/dt)".

In a switched-mode converter, the power dissipated in the device and the power removed can be expressed by:

$$V_R \cdot \frac{I_L(\tau - t_{on})}{\tau} + I_F \cdot V_F \cdot \frac{t_{on}}{\tau} \leq \frac{T_J - T_A}{R_{\theta J-A}} \quad (4.11)$$

- Where: V_R = Applied reverse voltage
- I_L = Leakage current at temperature
- t_{on} = Rectifier on-time

τ = 1/f, where f is the operating frequency

I_F = Forward current

V_F = Forward voltage at forward current (at temperature)

T_J = Junction temperature

Since both I_L and V_F are temperature sensitive parameters, we can express I_L and V_F as functions of temperature in the above equation for thermal stability and obtain:

$$\left\{ \frac{(\tau - t_{on})}{\tau} \cdot V_R \cdot I_o \cdot 2^{\frac{(T_J - T_A)}{y}} \right\} + \left\{ I_F \cdot \frac{t_{on}}{\tau} \cdot [V_{F0} + X(T_J - T_A)] \right\} \leq \frac{T_J - T_A}{R_{\theta J-A}} \quad [4.12]$$

Where: I_o = Leakage current at room temperature

V_{F0} = Forward voltage drop at room temperature

x = Temperature coefficient for forward voltage at operating current

y = Temperature difference for which leakage current doubles.

Differentiating the above equation:

$$\frac{(\tau - t_{on})}{\tau} \cdot V_R \cdot I_o \cdot 2^{\frac{(T_J - T_A)}{y}} \cdot \frac{1}{y} \cdot \ln 2 + I_F \cdot \frac{t_{on}}{\tau} \cdot X \leq \frac{1}{R_{\theta J-A}} \quad [4.13]$$

Defining I_o · 2 ^{$\frac{(T_J - T_A)}{y}$} as the critical current, I_{R(crit)} at maximum temperature, and solving for I_{R(crit)} we obtain:

$$I_{R(crit)} \leq y \left[\frac{(\tau/R_{\theta J-A}) - I_F \cdot t_{on} \cdot X}{.693 (\tau - t_{on}) V_R} \right] \quad [4.14]$$

Design Example

In the practical example previously discussed, the maximum reverse voltage across the rectifiers is 30V. Each rectifier is mounted on a heat sink. The

thermal resistance of the heat sink is 1°C/W . The Schottky rectifier, SD241, has a maximum thermal resistance of 1.4°C/W from case to junction. Its reverse leakage current doubles every ten degrees Centigrade, while the forward voltage at $I_f=20\text{A}$ decreased by $1\text{mV}/^\circ\text{C}$ as the junction temperature increases. The designer desires to limit the maximum operating junction temperature of the Schottky rectifier to 125°C under worst case conditions

Calculate the maximum reverse leakage current allowed for these rectifiers at 125°C to prevent thermal instability

Calculation:

$$\begin{aligned} R_{\theta JA} &= (R_{\theta H} + R_{\theta J-C})^\circ\text{C/W} \\ &= 1^\circ\text{C/W} + 1.4^\circ\text{C/W} \\ &= 2.4^\circ\text{C/W} \\ t_{\text{on}} &= 16.6\mu\text{s} \\ t_{\text{off}} &= 16.6\mu\text{s} \\ \tau = t_{\text{on}} + t_{\text{off}} &= 33.2\mu\text{s} \end{aligned}$$

Using equation 4.14:

$$I_{R(\text{crit})} \leq 10^\circ\text{C} \times \left[\frac{(33.2 \times 10^{-6}) / (2.4^\circ\text{C/W}) - (20\text{A}) (16.6 \times 10^{-6}) (-1 \times 10^{-3}\text{V})}{.693(33.2 \times 10^{-6} \text{sec} - 16.6 \times 10^{-6}) (30\text{V})} \right] \leq 410\text{mA}$$

From the SD241 specification, the maximum reverse leakage current at 125°C is 100mA ; therefore this system will be thermally stable.

4.5 Paralleling Rectifiers

When the output current required is greater than the maximum rated forward current of commercial rectifiers, it becomes necessary to parallel the devices. In some instances, it may be preferable to parallel devices even when a single device of higher current ratings is available. The advantages of paralleling these devices are:

- 1) Heat is easier to remove when compared to a single device with a higher current rating because the heat is spread between two or more devices.
- 2) The transformer is easier to wind since the wire size is smaller, using a separate winding for each rectifier.

- 3) Smaller chip size will have less chance of voids in the chip bond to the package, thus, the reliability of the system is improved.

The disadvantage of paralleling rectifiers is that some kind of circuit technique is required to share the current among the paralleled devices. If the current is not shared equally, the junction temperature of the device which conducts the higher current will increase. The forward voltage of the device will decrease due to its increased temperature and will conduct an even larger share of the load current. If adequate matching is not provided, this regenerative process continues; and if not checked in time, the junction temperature will exceed the maximum rating and the device will be damaged.

In switched-mode converter applications, current sharing can be accomplished by using separate windings for each rectifier and by matching forward drops. The series resistance of each winding acts as a current ballasting impedance.

5. Guidelines for Selecting the Schottky Rectifier in Pulse Width Mode (PWM) Switched-Mode Converter Applications

The minimum required dc blocking voltage of the Schottky rectifier and its maximum power dissipation can be calculated for different types of switched-mode power supplies summarized in Tables II and III. After calculating the maximum power dissipation, the designer can determine the required thermal resistance of the rectifier and the heat sink using the equation:

$$R_{\theta H} + R_{\theta JC} = \frac{T_{j\text{max}} - T_{\text{Amax}}}{P_{\text{max}}} \quad [5.1]$$

Where: $R_{\theta JC}$ = Thermal resistance of rectifier
 $R_{\theta H}$ = Thermal resistance of heat sink
 $T_{j\text{max}}$ = Maximum operating junction temperature of device
 T_{Amax} = Maximum ambient temperature

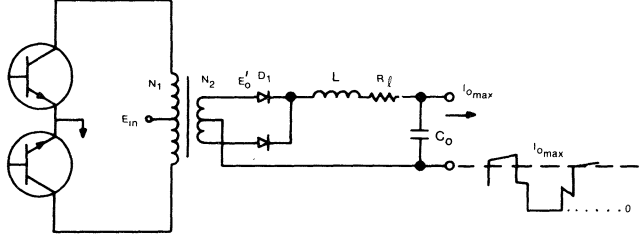
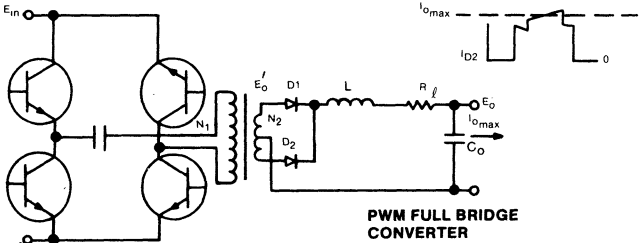
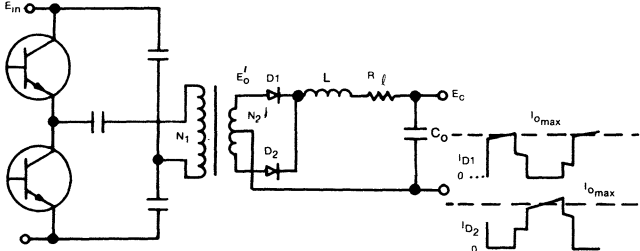
When calculations are made for maximum power dissipation in a rectifier, the voltage drop V_F and leakage current I_R should be taken at the maximum operating junction temperature.

During start up and for step changes in the output load current, the voltage across the rectifier should be limited to below its maximum dc blocking voltage to avoid failures due to transient voltage across the Schottky.

TABLE 1 — GUIDELINES FOR DETERMINING THE RATING OF A RECTIFIER IN A PWM SWITCHED-MODE CONVERTER

TYPES OF SWITCHING REGULATORS	OUTPUT VOLTAGE	STEADY STATE — POWER DISSIPATION IN RECTIFIERS	MINIMUM DC BLOCKING VOLTAGE REQUIRED
<p>BUCK REGULATOR</p>	$E_o = E_{in} \times \frac{t_{on}}{T}$ $E_o \approx E_{in} \times \frac{t_{on}}{T}$	<p>Power dissipation in Diode D₁ due to forward conduction:</p> $P_{D1F} = I_{o_{max}} \times V_F \cdot \frac{E_{in_{max}} - E_o}{E_{in_{max}}}$ <p>Power dissipation due to leakage current, I_R:</p> $P_{D1R} \leq I_R \times E_o \cdot I_R @ E_{in_{max}}$	<p>For Diode D₁:</p> $1.2 \times E_{in_{max}}$
<p>PUSH-PULL CONVERTER (50% Duty Cycle)</p>	$E_o' = E_o + V_F$ $E_o = E_{in} \times \frac{N_2}{N_1}$	<p>Power dissipation in Rectifier D₁ or D₂ due to forward conduction:</p> $P_{D1F} \text{ or } P_{D2F} = \frac{I_{o_{max}} \times V_F}{2}$ <p>Power dissipation due to leakage current, I_R:</p> $P_{D1R} \text{ or } P_{D2R} = 2.0 \times E_{in_{max}} \times \frac{N_2}{N_1} \times I_R$	<p>For D₁ or D₂:</p> $2.4 (E_{in_{max}}) \times \frac{N_2}{N_1}$
<p>PWM FORWARD CONVERTER</p>	$E_o' = E_o + V_F + I_{o_{max}} \times R$ $E_o = E_{in_{min}} \times \frac{N_3}{N_1 + N_2}$ <p>Where:</p> <p>E_o = dc Output Voltage</p> <p>E_o' = Output of Secondary Winding When D₁ is conducting</p>	<p>Power dissipation due to forward conduction in Rectifier D₁:</p> $P_{D1F} = I_{o_{max}} \times V_F \cdot \frac{N_1}{N_1 + N_2}$ <p>Power dissipation in Rectifier D₂:</p> $P_{D2F} = I_{o_{max}} \times V_F \left[1 - \frac{N_1}{N_1 + N_2} \cdot \frac{E_{in_{max}}}{E_{in_{min}}} \right]$ <p>Power dissipation due to reverse leakage current:</p> $P_{D1R} = E_{in_{min}} \cdot I_R \cdot \frac{N_3}{N_1 + N_2}$ $P_{D2R} = I_R \times \frac{N_3}{N_1 + N_2} \times E_{in_{min}}$	<p>For D₁:</p> $1.2 \times E_{in_{max}} \times \frac{N_3}{N_2}$ <p>For D₂:</p> $1.2 \frac{E_{in_{max}} \times N_3}{N_1}$

TABLE II

TYPES OF SWITCHING REGULATORS	OUTPUT VOLTAGE	STEADY STATE — POWER DISSIPATION IN RECTIFIERS	MINIMUM DC BLOCKING VOLTAGE REQUIRED
<p style="text-align: center;">PWM PUSH-PULL CONVERTER</p>  <p style="text-align: center;">PWM FULL BRIDGE CONVERTER</p> 	$E_o = E_o + V_F + I_{o_{max}} \times R_l$ $E_o = E_{in_{min}} \times \frac{N_2}{N_1}$ <p>For Push-Pull and Full Bridge</p>	<p>Power dissipation in Rectifier D₁ or D₂ due to forward conduction</p> $P_{D1F} \text{ or } P_{D2F} = \frac{I_{o_{max}} \times (V_F @ I_{o_{max}})}{2} \times \frac{E_{in_{min}}}{E_{in_{max}}}$ $+ \frac{I_{o_{max}} \times (V_F @ I_{o_{max}})}{2} \times \frac{E_{in_{max}} - E_{in_{min}}}{E_{max}}$ <p>Power dissipation due to leakage current</p> $P_{D1R} \text{ or } P_{D2R} = I_R (E_{in_{min}}) (N_1/N_2)$ <p>NOTE $I_R @ 2(E_o + V_F + I_{o_{max}} \times R_l) \times \frac{E_{in_{max}}}{E_{in_{min}}}$</p>	<p>For D₁ or D₂.</p> $2.4 (E_o + V_F + R \times I_{o_{max}}) \times \frac{E_{in_{max}}}{E_{in_{min}}}$
<p style="text-align: center;">PWM HALF-BRIDGE CONVERTER</p> 	$E_o = E_o + V_F \times I_{o_{max}} \times R_l$ $E_o = \frac{E_{in_{min}}}{2} \times \frac{N_2}{N_1}$ <p>For Half-Bridge</p>	<p style="text-align: center;">SAME AS ABOVE</p>	<p style="text-align: center;">SAME AS ABOVE</p>

6 Conclusion

Complete design guidelines for Schottky rectifiers used in switched-mode converters have been provided. The Schottky, when compared to a fast PN junction rectifier, offers the advantages of lower forward voltage and a faster reverse recovery time which is independent of temperature. Efficiency is improved at least 3 to 5% when Schottky rectifiers are used in place of PN junction devices for power rectification in switched-mode converters. Schottky rectifiers are available with a maximum reverse blocking voltage up to only 50 to 60V. Thus, applications of Schottky devices are limited to low output voltages (+5V) in PWM switched-mode converters (except for buck type and 50% duty cycle converters). When the rectifier requires voltage blocking capability of greater than 60V, fast PN junction devices like UES800 series rectifier offers the optimum choice without sacrificing speed and forward voltage.

SCHOTTKY RECTIFIERS

AVERAGE DC OUTPUT CURRENT		6A	8A	12A ¹	12A	16A ²	16A	25A	30A	50A	60A ³	60A	75A
PEAK REVERSE VOLTAGE	PACKAGE	TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (3-LEAD)	TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (3-LEAD)	TO-220 PLASTIC (2-LEAD)	DO-4 STUD	DO-4 STUD	DO-5 STUD	TO-3	DO-5 DO-SF STUD	DO-5 DO-SF STUD
	20V	TYPE V _F I _{FSM}	USD620 55 @ 6A 150A	USD720 55 @ 8A 200A	USD620C 65 @ 12A 150A	USD820 45 @ 12A 200A	USD720C 65 @ 16A 200A	USD920 50 @ 16A 250A		USD420 55 @ 30A 600A		USD320 6 @ 20A 400A	
30V	TYPE V _F I _{FSM}							1N6095 86 @ 78A 400A		1N6097 86 @ 157A 800A			
35V	TYPE V _F I _{FSM}	USD635 55 @ 6A 150A	USD735 55 @ 8A 200A	USD635C 65 @ 12A 150A	USD835 45 @ 12A 200A	USD735C 65 @ 16A 200A	USD935 50 @ 16A 250A		USD435 55 @ 30A 600A		USD335C 6 @ 20A 400A		USD535 6 @ 60A 1000A
40V	TYPE V _F I _{FSM}	USD640 55 @ 6A 150A	USD740 55 @ 8A 200A	USD640C 65 @ 12A 150A	USD840 45 @ 12A 200A	USD740C 65 @ 16A 200A	USD940 50 @ 16A 250A	1N6096 86 @ 78A 400A		1N6098 86 @ 157A 800A			
45V	TYPE V _F I _{FSM}	USD645 55 @ 6A 150A	USD745 55 @ 8A 200A	USD645C 65 @ 12A 150A	USD845 45 @ 12A 200A	USD745C 65 @ 16A 200A	USD945 50 @ 16A 250A		USD445 SD41 ² 55 @ 30A 600A		USD345C SD241 6 @ 20A 400A	SD51 ⁴ 6 @ 60A 800A	USD545 6 @ 60A 1000A

1 CENTER-TAP 6A PER LEG

2 CENTER-TAP, 8A PER LEG

3 CENTER-TAP, 30A PER LEG

4 V_R AT 25° C IS 45V, V_R AT 150° C IS 35V

500W, 200kHz OFF-LINE POWER SUPPLY USING POWER MOSFETS

Introduction

The power supply design discussed in this application note uses a fairly common, straight-forward circuit. It is the judicious selection of the components used, and careful layout of the circuit, which gives it its performance. As the operating frequency of switching power supplies continues to increase above 100kHz, attention to high frequency considerations is a necessity. A knowledge of component and circuit parasitics is essential as well as an understanding of RLC circuits and transient response, particularly LC resonant tank circuits. Because of the resonance of parasitic circuit and component inductance and capacitance at these high frequencies, the use of damping and snubbing techniques becomes increasingly important.

In the off-line converters some of these high frequency problem areas are aggravated by the large turns ratio of the step-down transformer, particularly for low voltage (5V) outputs. The use of Schottky rectifiers with their 5 to 10 times larger junction capacitance than PN junction rectifiers can cause additional difficulty with the design. At 200kHz these problems are manageable by careful component selection and circuit layout.

Specifications

Input - 115V or 220V \pm 15%, 50Hz or 60Hz

Output - 5V @ 100A

Regulation - Line: 0.4%

Load: 0.5% (10% to 100% load)

Ripple: 100mV peak to peak

Frequency - 200kHz

Efficiency - 75% minimum

Circuit Description

The schematic and parts list of a 500W switching power supply are shown in Figure 9. The description of the circuit is as follows. The input rectifier bridge is arranged for connection either to the 117 or the 220V AC line. The circuit uses a pair of Unitrode UFN441 power MOSFETs in a half-bridge configuration. The MOSFET gates are driven directly from a UC3525A control chip output through step down and isolation transformer T₁. The UC3525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of

T₁. This provides the fast, high current turn-on and turn-off pulses needed for the MOSFET gates. In addition, the two ends of the primary winding are shorted to ground during deadtime, which prevents accidental turn-on of an output transistor by transients. Note that the current supplied by the UC3525A output drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors R₃ and R₄, with series blocking capacitors C₁₆ and C₁₇, minimize ringing of the MOSFET gate capacitance with the inductance of T₁ and lead inductance; particularly during deadtime. In this design, where the gates are driven directly from the control chip via the gate drive transformer at 200kHz, it is necessary to use a small heat sink for the control chip. A Thermalloy #6007 is sufficient.

The output transformer uses a small E-E core, Ferroxcube EC52-3C8, operated at 1000 Gauss peak to reduce core loss at 200kHz. The primary is wound in 2 layers, 7 turns per layer, 2 #16 AWG wires in parallel. The secondaries are wound between the 2 primary layers to reduce leakage inductance, and are made of copper strap 10 mils thick by 0.8 inches wide, one turn on each side of the centertap.

Ringing of the primary winding, at a frequency of approximately 4MHz due to leakage inductance resonating with the output capacitance of the MOSFETS, is controlled by damping resistor R₁₈ and blocking capacitor C₄.

Reverse voltage across Schottky rectifiers CR₁ to CR₄, due to ringing (at approximately 20MHz) of the LC circuit comprised of the Schottky rectifier capacitance with the leakage inductance of the transformer (transformed to the secondary by the square of the turns ratio), is controlled by damping resistors R₇ to R₁₀ with blocking capacitors C₁₀ to C₁₃.

The output filter capacitor C₅ is comprised of three 5 μ F, 100V polypropylene capacitors in parallel. These are TRW type 35, with an ESR of 12 milliohms each. The inductor is made with a Ferroxcube IF30-3C8 core, wound with 4 turns of 5 #12 AWG wires in parallel.

Current limiting is done with current transformer T₃

in the return lead of the transformer primary. The signal is rectified, threshold sensed and adjusted, and is fed to the shutdown terminal pin 10 of the UC3525A control chip.

Performance

A curve of efficiency versus power output is shown in Figure 8. Note that the efficiency decreases for increasing power output. This is primarily due to resistive losses, other than the Schottky rectifier losses, such as the $R_{DS(on)}$ losses of the MOSFETs and the copper losses of the output transformer and filter inductor. The switching losses of the MOSFETs are low; the measured current rise and fall times were 10ns and 20ns, respectively.

When compared to a 25kHz switcher, the transient response of this circuit can be improved by a factor over 8 times since the LC output filter resonant frequency can be increased by this amount. There is an additional improvement factor, since polypropylene capacitors rather than electrolytic are used for 200kHz operation. The value of capacitance can be reduced considerably, because of the improved ESR. However, in order to realize the improved frequency response, careful attention to control circuit layout and shielding is important to minimize parasitic capacitance and inductance. The use of a ground plane is a necessity.

A dramatic reduction of the size of several major components is evident when comparing this 200kHz, 500W switcher to a 25kHz switcher. The power transformer, output filter inductor, and output filter capacitor are about half the volume, and the drive circuits for the MOSFETs are considerably smaller than the drive circuits for bipolars at 25kHz. The auxiliary power supply is half the size. The parts count is less, primarily due to the reduced parts count of the drive circuits.

Design Considerations

The choice of operating frequency and the decision to use MOSFETs or bipolars depends upon a number of factors, including the required power output level, size, weight, cost, etc., and a rapidly changing technology which includes circuit topology, new components, control chips and high frequency techniques.

There are some major advantages that are obtainable by using MOSFETs in place of bipolars, other than those associated with higher operating frequency. One of these is in the area of potential gate drive circuits. In the power supply described in this application note, the power MOSFET gates are driven directly by the control chip through a small

step down isolation transformer.

The feedback loop compensation is comprised of an RC network at the error amplifier of the UC3525A. The resonant frequency of the LC output filter is approximately 40kHz. Closing the loop at 0dB at 100kHz, this network adds two zeros (phase lead) at approximately one half the LC resonant frequency, and gives a 40° phase margin up to 100kHz.

Do's and Don'ts of High Frequency Switchers

For the control chip circuit, the use of a ground plane construction is recommended. A double sided PC board, with one side used for the ground plane, is preferable. If a single sided board is used, use as much copper area as possible for the ground plane. Keep traces fairly wide to reduce inductance. The judicious use of a few wire jumps to reduce trace length is helpful.

Power MOSFET gate drive circuits do not have to supply a continuous large current drive. MOSFET gates do require fairly large, fast current pulses to change the gate voltage rapidly because of the composite gate capacitance, including the Miller effect capacitance. This means that the gate drive circuit and transformer should be designed to minimize lead inductance by reducing loop areas to a minimum. Remember that each inch of wire adds about 20 nanohenries of inductance. Using fairly large diameter wires twisted together helps, as well as designing the layout to reduce lead lengths to a minimum.

The use of copper strapping in place of round wire is also helpful in reducing inductance. Use two closely spaced parallel strips if possible. Circuit by-passing with small high frequency capacitors is important, especially around the control chip circuit area. By-passing the fairly large electrolytic input energy storage capacitors is helpful, if the by-pass capacitors are located physically at the junction of the MOSFETs and the primary of the output transformer, as shown on the schematic.

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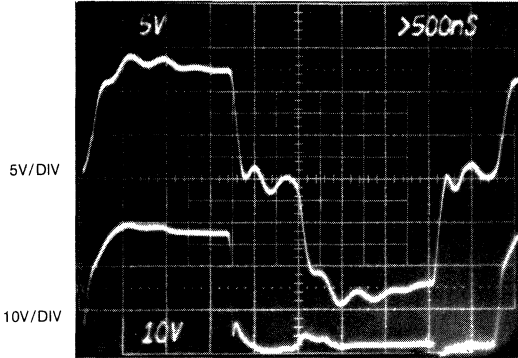
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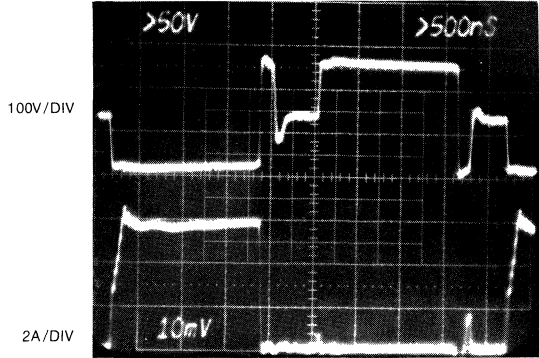
MOSFET Gate Drive Circuitry," Unitrode Switching Power Supply Design Seminar Manual, Spring 1982.

WAVEFORMS AT $I_o = 100A$



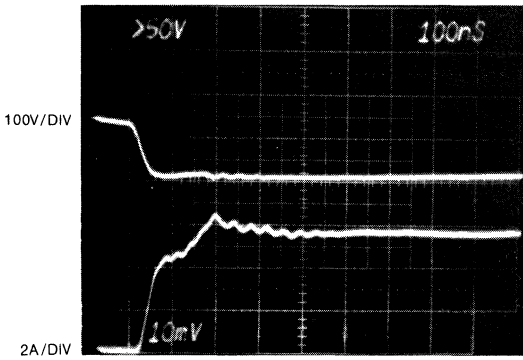
UPPER — V_{gs} OF Q_2
 LOWER — V_{out} OF PIN 14, UC3525A
 500ns/DIV

FIGURE 1. GATE DRIVE



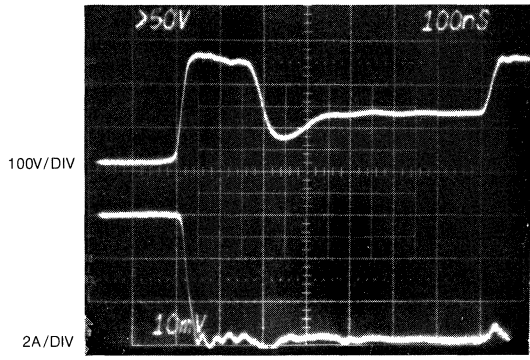
UPPER — V_{ds} OF Q_2
 LOWER — I_o OF Q_2
 500ns/DIV

FIGURE 2. MOSFET SWITCHING



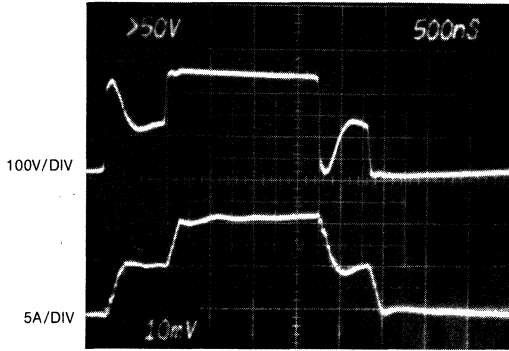
UPPER — V_{ds} OF Q_2
 LOWER — I_o OF Q_2
 100ns/DIV

FIGURE 3. RISE TIME



UPPER — V_{ds} OF Q_2
 LOWER — I_o OF Q_2
 100ns/DIV

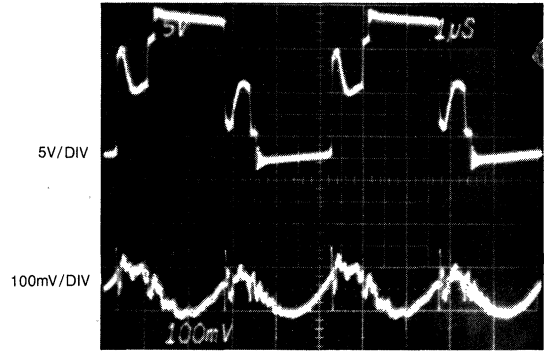
FIGURE 4. FALL TIME



500ns/DIV

UPPER — $V_{PRIMARY}$
LOWER — $I_{PRIMARY}$

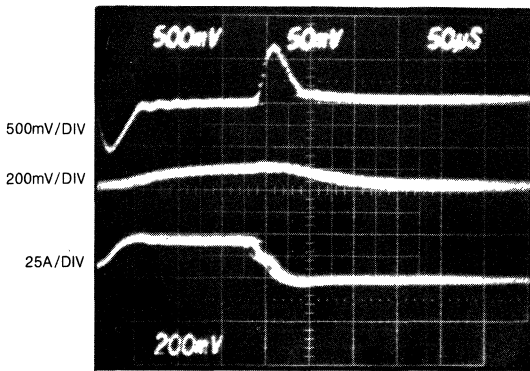
FIGURE 5. TRANSFORMER PRIMARY WAVEFORMS



1µs/DIV

UPPER — XFMR SEC VOLTAGE
LOWER — OUTPUT RIPPLE

FIGURE 6. TRANSFORMER SECONDARY VOLTAGE, AND OUTPUT RIPPLE



50µs/DIV

UPPER — 5V OUTPUT
MIDDLE — ERROR AMPLIFIER OUTPUT
LOWER — LOAD CURRENT

FIGURE 7. TRANSIENT RESPONSE, 25A LOAD CHANGE (LARGE SIGNAL CHANGE)

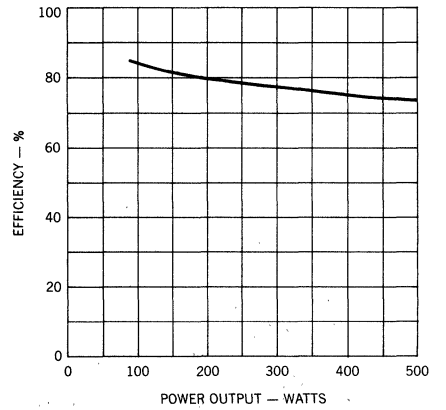


FIGURE 8. EFFICIENCY VS POWER OUTPUT

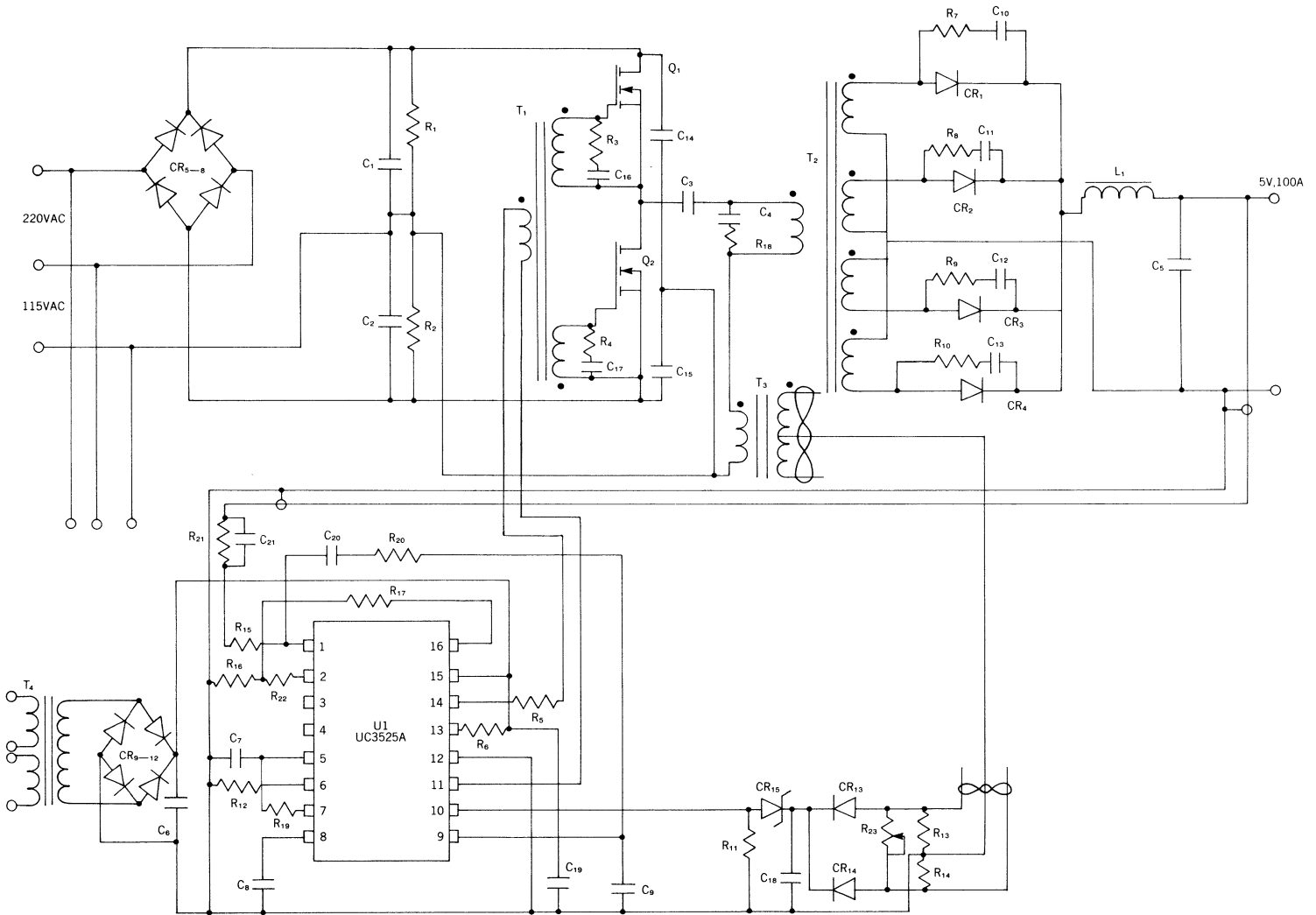


FIGURE 9. SCHEMATIC OF 500W, 200kHz HALF-BRIDGE POWER SUPPLY

15-119

Parts List

U ₁	UC3525A	R ₁₂	3.3K
Q ₁ , Q ₂	UFN441	R ₁₃ , R ₁₄	220Ω
CR ₁ -CR ₄	USD545	R ₁₅	10K
CR ₅ -CR ₈	680-4 (Unitorde)	R ₁₆	10K
CR ₉ -CR ₁₂	673-1 (Unitorde)	R ₁₇	51Ω
CR ₁₃ , CR ₁₄	UES1003	R ₁₈	50Ω, 4W
CR ₁₅	TVS310	R ₁₉	10Ω
C ₁ , C ₂	600μF, 250V	R ₂₀	27K
C ₃	1μF, 400V	R ₂₁	24K
C ₄	500pF, 1kV	R ₂₂	33K
C ₅	3x5μF, 100V (polypropy.)	T ₁	Core, Ferrox 486T250-3C8 Pri, 14T #22AWG Sec (2) 7T #22AWG
C ₆	500μF, 50V	T ₂	Core, Ferrox EC52-3C8 Pri, 14T, 2 layers, 2 #16 AWG in parallel. Sec, (2), each 2T, C.T., copper strap 0.01" x 0.8" see text.
C ₇	1000pF, 50V	T ₃	Core, Ferrox 486T250-3C8 Pri, 1T Sec, 20 turns CT #22AWG
C ₈	1μF, 50V	T ₄	220/117V, 25V, 0.15A
C ₉	50pF, 50V	L ₁	Core, Ferrox IF30-3C8, 4 turns, 5 #12AWG in parallel.
C ₁₀ -C ₁₃	0.02μF, 50V		
C ₁₄ , C ₁₅	1μF, 200V		
C ₁₆ , C ₁₇	.002, μF, 50V		
C ₁₈	0.2, μF, 50V		
C ₁₉	0.1, μF, 50V		
C ₂₀	300pF, 50V		
C ₂₁	220pF, 50V		
R ₁ , R ₂	33K, 2W		
R ₃ , R ₄	47Ω		
R ₅	10Ω, 1/2W		
R ₆	4.7Ω		
R ₇ -R ₁₀	3.9Ω, 1/2W		
R ₁₁	10K		

DESIGN CONSIDERATIONS FOR POWER MOSFET GATE DRIVE CIRCUITRY

1. Introduction

The power MOSFET promises exciting performance advantages over the more conventional bipolar transistor. However, much attention must be given to gate drive techniques to take full advantage of MOSFET characteristics. This application note develops simple, high performance gate drive circuits.

This application note also provides design engineers with a basic understanding of the relationship between parasitic elements and switching times. In addition, a circuit is developed which controls the switching time of the power MOSFET to reduce rectifier reverse recovery spikes; thus, reducing RFI and switching loss.

2. Features

The power MOSFET is becoming more and more popular in many applications due to its inherent features, such as:

2.a. Extremely Fast Switching Characteristics.

A power MOSFET is capable of switching rapidly because it is a majority carrier device. The speed at which it can switch depends upon the rate at which gate charge is supplied or removed by the gate driving source. In a practical application the MOSFET can be made to switch in less than 10 nanoseconds. This feature allows operation at higher frequencies than with bipolar devices, resulting in improved electrical performance (transient response), reduced size and cost of the magnetic components, and decreased weight of the overall system.

Other advantages derived from fast switching times are:

- The losses in the snubber circuit, if employed, are minimized.
- Switching times are independent of load and temperature variation. The variation in the frequency spectrum of conducted RFI is minimized.
- The cross-conduction problem in a switched-mode converter (half bridge, full bridge, push-pull) is reduced because power MOSFETs have no storage time.
- The problem of core saturation due to asymmetrical volt-seconds in circuits using a transformer is minimized because the major cause of this effect, differences in storage time is negligible for MOSFETs.
- If a voltage feed-forward control is being used, the nonlinearity introduced by the storage time of the switching device is eliminated, thus reducing the gain requirement of the error amplifier.

2.b. High Gate Input Impedance.

The gate input impedance is a high resistance shunted by a capacitance. At high frequencies the capacitance completely dominates. This fact allows the design of a simple and efficient gate drive circuit.

2.c. No Forward or Reverse Biased Second Breakdown.

Because of the positive temperature co-efficient of channel resistance, power MOSFETs do not have forward or reverse biased second breakdown characteristics like bipolar devices. Thus power MOSFETs improve the overall reliability of systems. Snubber networks for turn-off load line shaping may be smaller and often eliminated. This reduces circuit complexity and cost. The voltage spikes due to stray inductance can be limited by simply controlling the switching times in many applications.

2.d. Integral Diode.

There is a built-in diode across the source to drain. The reverse recovery time of the diode depends upon the drain to source breakdown voltage. Low voltage (100V) devices have reverse recovery times as low as 200 nanoseconds, while high voltage devices (400-500V) have recovery times of about 600-700 nanoseconds. When a high speed diode is not required, the internal diode can be used effectively for free wheeling voltage damping. However, long recovery times might hinder the performance of the circuit in some applications, so this effect must be considered.

2.e. Current Sharing Capability

Since the channel resistance of a power MOSFET has a positive temperature co-efficient many devices can be paralleled with much less special design attention than with bipolar transistors. The power output capability can, thus, be extended.

The Undesirable Features of the Power MOSFET are:

2.f. Temperature Dependence of Saturation Resistance.

The saturation resistance ($R_{DS(on)}$) increases with temperature. It doubles approximately every 110°C. Thus, power dissipation will increase as the junction temperature increases. Consideration of the thermal stability of the system is required if a major part of the power losses occur in the on-state mode.

(In a bipolar transistor "off line" converter, most of the power losses are due to switching. The switching losses increase with temperature, usually doubling every 100°C. In this respect, power MOSFETs will be more thermally stable than bipolar transistors, as switching the times of a power MOSFET do not change with temperature.)

2.g. Silicon Chip Area.

The silicon chip area of a power MOSFET is about 50% larger than an equivalent bipolar transistor. This has some impact on the cost of the device.

3. Construction

The cross section of an N-channel vertical DMOS (double-diffused MOS) is shown in Figure 3.1. Sections of this structure affecting gate drive are discussed in the following sections.

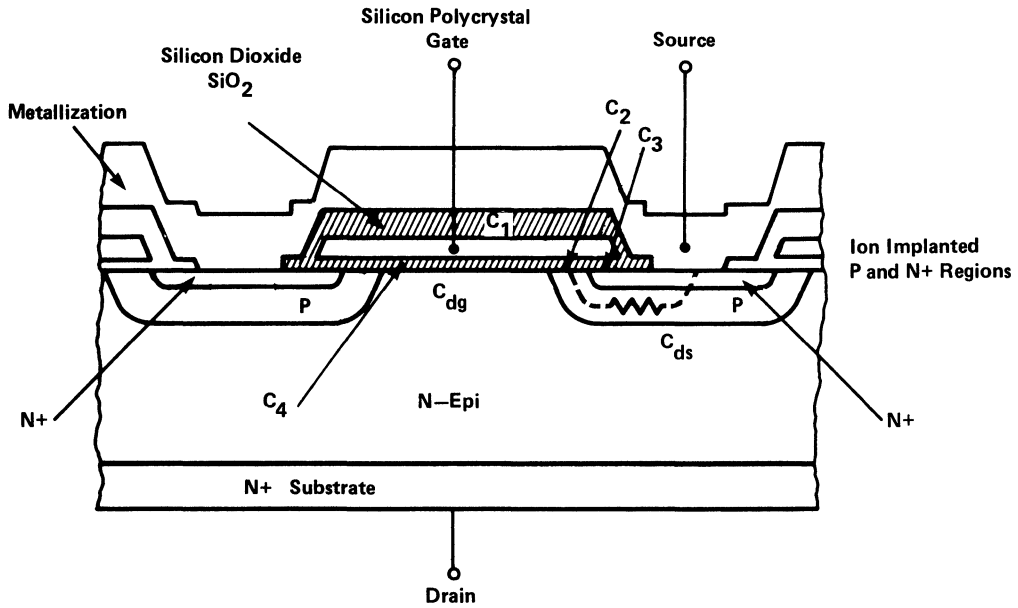


Figure 3.1 The Power MOSFET Physical Structure

4. Parasitic Elements and Switching

Since MOSFETs are majority carrier devices, they are theoretically capable of switching in picoseconds. In practical devices, however, parasitic elements adversely affect switching capability. MOSFET parasitic capacitances are shown in Figure 4.1.

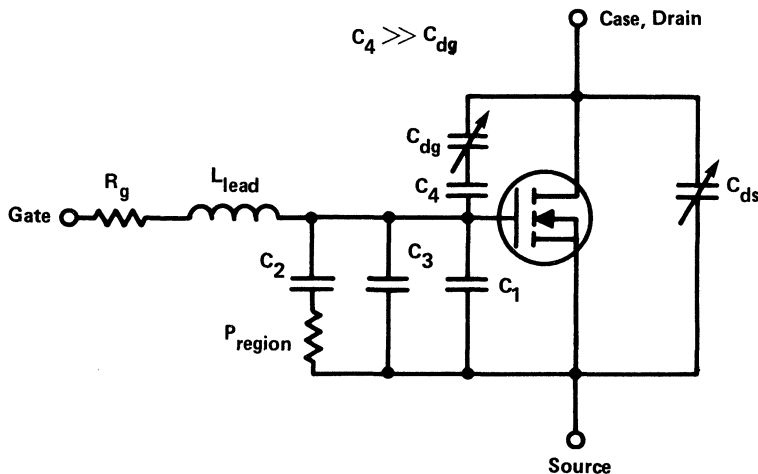


Figure 4.1 Power MOSFET Parasitic Capacitance

The thickness and area of SiO_2 dielectric material between gate and source determines the value of the gate capacitance. In the off-state, the total gate-to-source capacitance is composed of a) capacitance C_3 between the gate and the heavily doped N+ source region, b) capacitance C_2 between the gate and the moderately doped P region and c) capacitance C_1 between the gate and the source metallization on the top of the gate (C_1 is much less than capacitances C_3 and C_2 and can be neglected). The gate capacitance is practically independent of gate voltage, as shown in Figure 4.2.

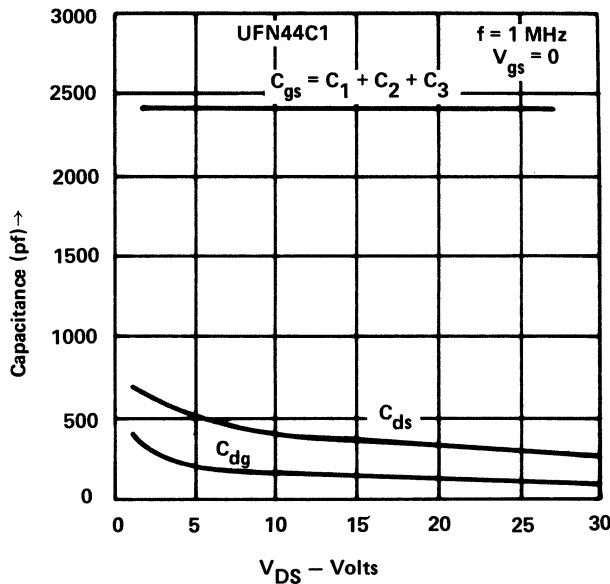


Figure 4.2 Capacitance Vs. Drain to Source Voltage

The Miller effect capacitance between drain and gate consists of a series combination of a space charge capacitance C_{dg} due to a depletion layer in the N-region and the dielectric capacitance C_4 between the N-region and the gate, as shown in Figure 3.1. The capacitance C_{dg} is a function of drain voltage (as shown in Figure 4.2), while dielectric capacitance C_4 is independent of the voltage. These drain capacitances effectively increase the input gate capacitance during switching transitions.

The capacitance C_{ds} between drain and source is a depletion capacitance and does not have a major effect on the switching behaviour of the device. It can be neglected in the switching analysis.

The turn-on and turn-off characteristics of a power MOSFET are shown in Figure 4.3.

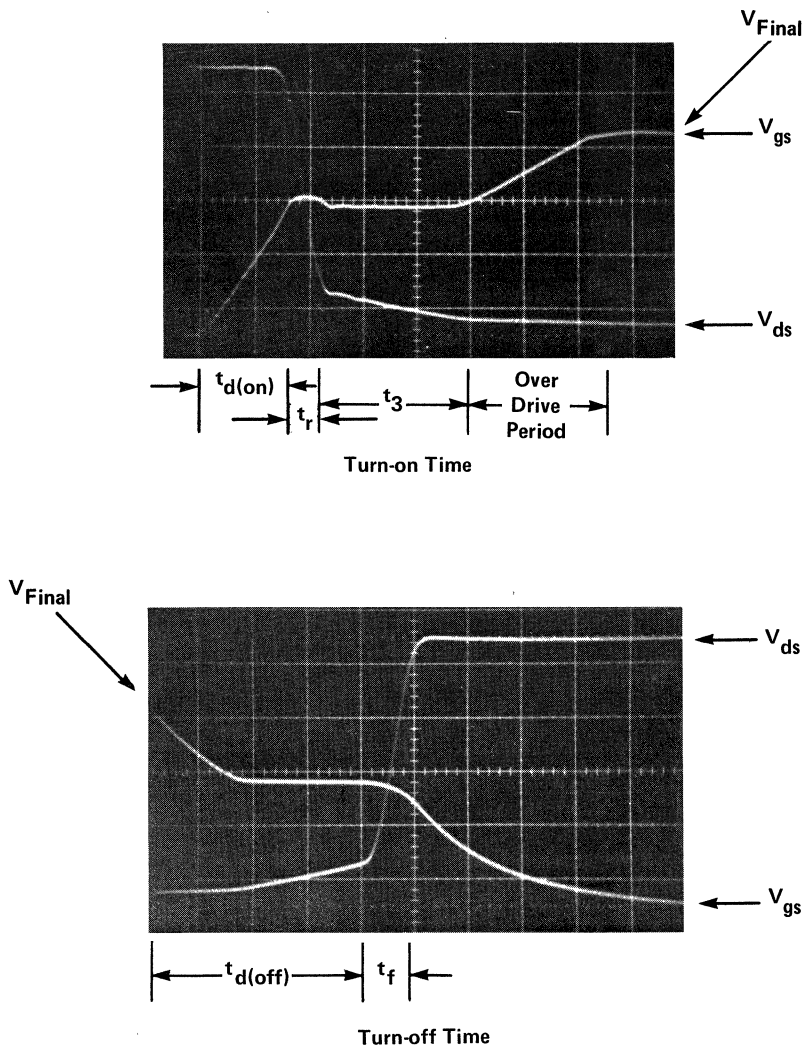


Figure 4.3 Power MOSFET Switching Waveforms

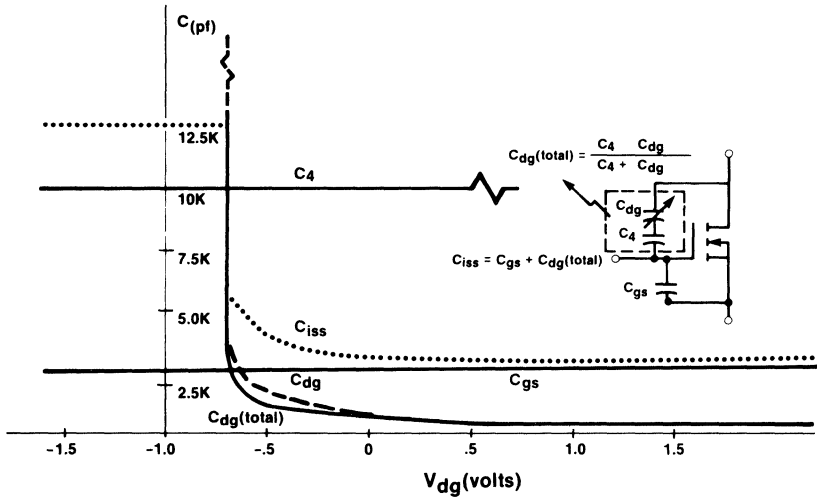


Figure 4.4A C vs V_{dg} - Static Case Expanded

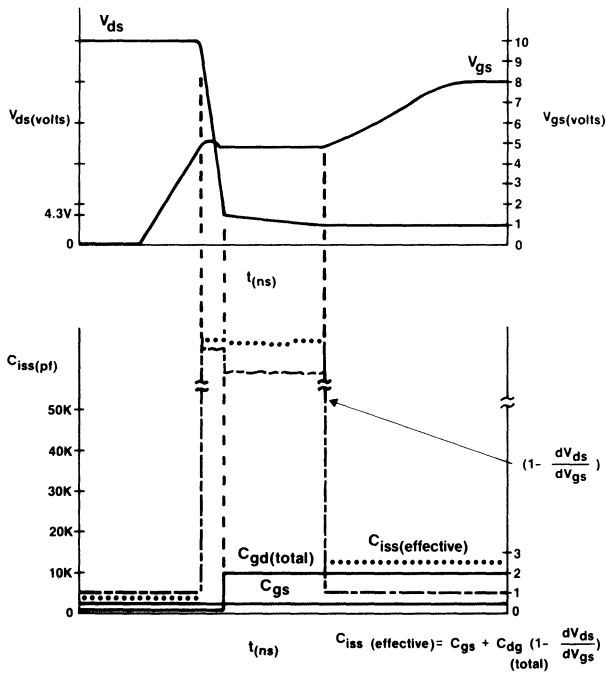


Figure 4.4B C vs t - Dynamic Case

Figure 4.4 Input Capacitance and Conditions at Turn-on

4.a. Turn-on Delay Time – $t_{d(on)}$

The effective gate input capacitance during this period is a parallel combination of capacitor C_1 , C_2 and C_3 . While the gate voltage builds up toward the gate threshold voltage, the drain voltage remains the same.

4.b. Rise Time – t_r

When the drain voltage starts to drop, during current rise time the effective gate capacitance increases significantly due to the Miller effect capacitance (C_{dg}), which absorbs nearly all the gate drive current. The rise time of the drain current is inversely proportional to the gate drive current supplied, and transition rise time can be controlled accurately by controlling the gate current, a feature particularly useful to reduce current overshoot due to rectifier reverse recovery. Since the magnitude of the gate and drain capacitances are determined by the structure of the device, they are very consistent from device to device and are temperature independent. This allows optimization of snubber network designs.

4.c. Dynamic Saturation – t_3

During this period, which follows the rise time; the drain voltage drops below the gate voltage. An inversion layer is established underneath the entire gate in the N- drain region. The gate capacitance is equal to the dielectric capacitance and is independent of voltage bias. At this point, the total drain to gate capacitance changes abruptly to a very high value. This can be seen in the gate voltage waveform of Figure 4.3 where effective gate capacitance is in the order of 50,000 pf and no further increase in gate voltage is noticed.

4.d. Overdrive Period

The input gate capacitance is approximately twice the value expected from Figure 4.2 during over-drive conditions, as can be seen by comparing the slopes of the gate voltage during the period $t_{d(on)}$ and overdrive (see Figure 4.3). This is because C_{gs} is measured with a greater voltage across the drain to source terminals than is present during this period.

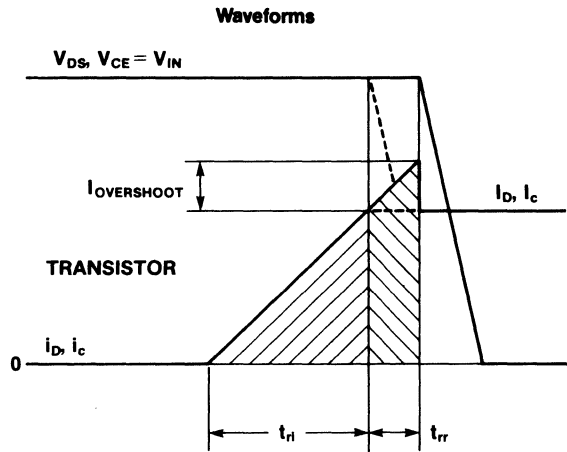
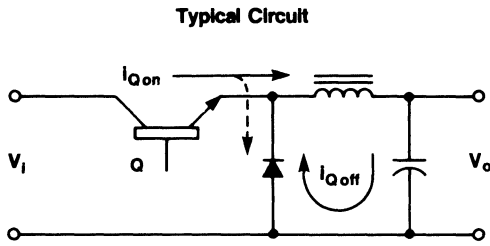
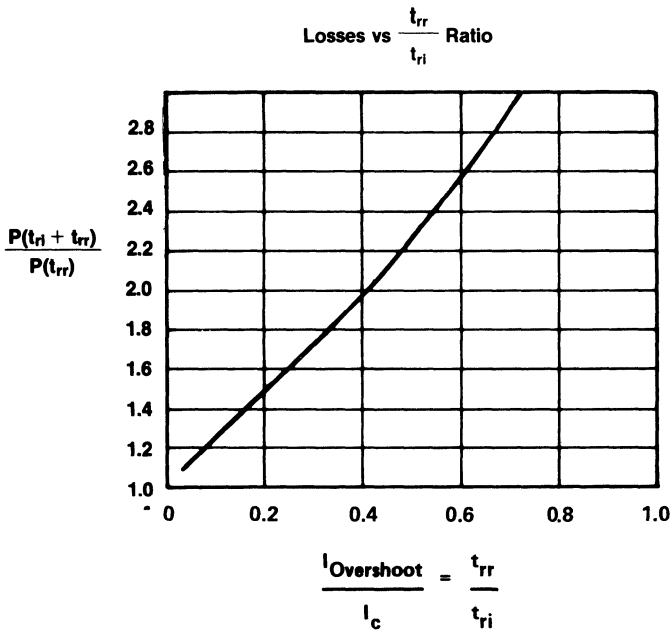


Figure 5.1A Transistor Current During Turn-On



Example: $V_{CE} = 100V$, $I_c = 6A$, $t_{rl} = 100ns$

t_{rr} (ns)	I_{PK} (A)	P_{AV} (W/Cycle)	E (μJ)
0	6	300	30
30	7.8	390	51
50	9	450	68
100	12	600	12

$$\frac{I_{Overshoot}}{I_c} = \frac{t_{rr}}{t_{rl}}$$

Figure 5.1B Effect of Reverse Recovery on Losses

Figure 5.1 Importance of Current Rise Time in a Transistor and Reverse Recovery in a Rectifier

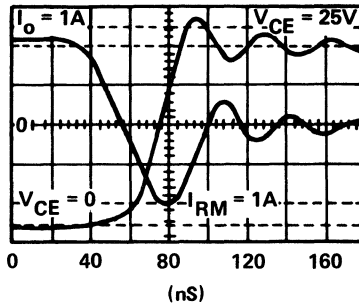


Figure 5.2A Schottky Rectifier (SD41)

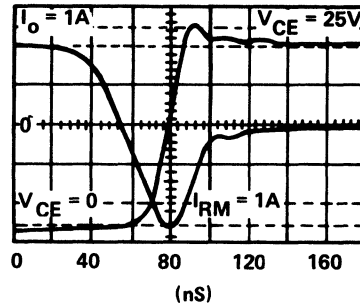


Figure 5.2B Ultra-fast PN Junction (UES701)

Figure 5.2 Reverse Recovery of Fast Rectifiers

5. Drive Circuit Considerations

The power MOSFET is a charge driven device, and the switching times can be controlled by the external circuit rather than by the device itself. In a buck switching regulator application (or similarly behaving circuit), the rise time of a power MOSFET may be controlled to prevent excessive current spikes and power dissipation due to rectifier reverse recovery. Current spikes also produce unwanted ringing and RFI in the circuit. The relationship between reverse recovery time, current rise time and power dissipation in the power MOSFET is shown in Figure 5.1. The fastest available power PN junction rectifiers have recovery times on the order of 20 ns. To minimize the recovery current spikes, the current rise time of the power MOSFET should be made at least 3 times slower than the reverse recovery of the rectifier. Even though Schottky rectifiers are majority carrier devices, they have about the same effective reverse recovery time as very fast PN junction diodes due to high junction capacitance, as shown in Figure 5.2. In transformer coupled switching regulators, leakage inductance will reduce the large current spikes to some extent depending upon the transformer design.

During turn-off time, voltage spikes will occur as a result of energy stored in the stray inductance of the drain circuit during the preceding on-time. The magnitude of these spikes directly depends upon the speed with which the device is turned off and upon lead inductance in the drain circuit. A snubber network in the drain may be required to limit these voltage spikes. The turn-off power dissipation can be optimized with a fast turn-off time along with the use of a snubber circuit.

The drive circuit described in this section allows control of the rise time in a power MOSFET during turn-on while providing fast turn-off.

5.a. Low Cost Gate Drive Circuit

A low cost power MOSFET gate drive circuit with isolation for off-line applications is shown in Figure 5.3. The circuit provides a controlled rate of increasing drain current to minimize spikes due to the reverse recovery of the output rectifier. The rise time of the power MOSFET is controlled by supplying a linearly increasing gate voltage. The relatively large capacitor C_1 (as compared with C_{gs}) is placed in parallel with the gate and source to minimize the effect of variations of C_{dg} on the switching characteristic of the device. C_1 also prevents spurious oscillations due to high frequency voltage feedback from C_{dg} . C_1 is charged with a constant current from the drive circuit, providing linearly increasing voltage at the gate of power MOSFET, Q_2 . The rise time of the MOSFET depends on the rate at which capacitor C_1 charges. The drive circuit described provides a rise time of around 70 ns and current fall time of about 40 ns.

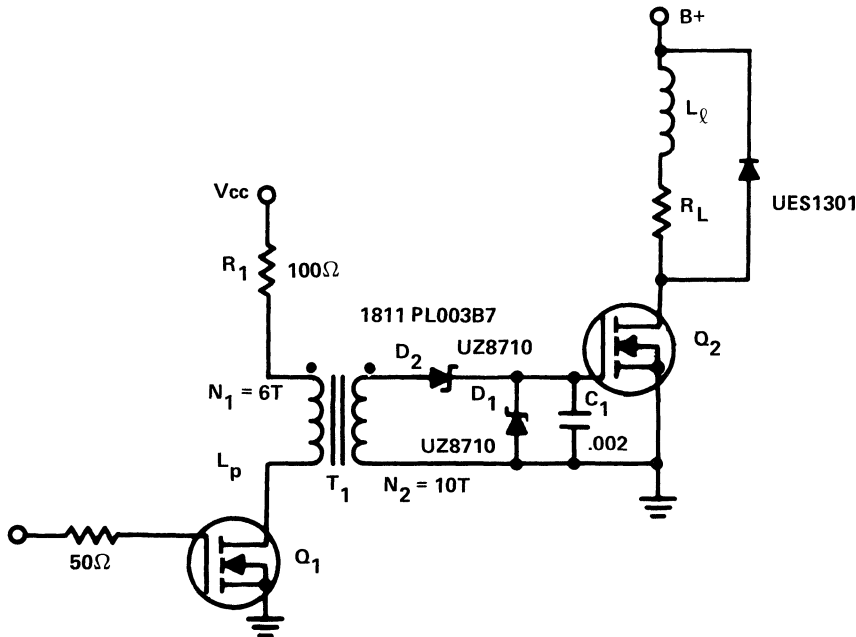


Figure 5.3 Low Cost Gate Drive Circuit with Isolation

The operation of the circuit can be described as follows: When drive transistor Q_1 turns on, the current transformer provides constant drive current into the secondary circuit. The constant drive current is determined by resistor R_1 and will charge capacitor C_1 linearly through diode D_2 . Zener diode D_1 limits Q_2 gate to source voltage. When the voltage across the secondary winding drops due to primary time constant L_p/R_1 , the zener diode D_2 becomes reverse biased and prevents the discharge of capacitor C_1 . While transistor Q_1 is on, the energy will be stored in the transformer core. When transistor Q_1 subsequently turns off, current will flow in the secondary side due to energy stored in the core of transformer T_1 . The amount of energy stored must be greater than that stored in the capacitor C_1 in order to ensure complete discharge of the capacitor.

Capacitor C_1 discharges through zener diode D_2 . Diode D_1 prevents any negative voltage swing across gate to source and provides a current path for discharge of the secondary inductance.

The circuit shown in Figure 5.4 improves the fall time compared to the previous circuit. The operation of the circuit is the same as that described above except during turn off. During Q_1 turn-off, capacitor C_1 discharges through winding N_3 and diode D_2 . The discharge current will be 4 times greater than in the previous circuit because the current now flows through only one quarter of the winding, while the ampere-turns remain unchanged. Diode D_1 prevents current flow from the winding N_2 during turn off.

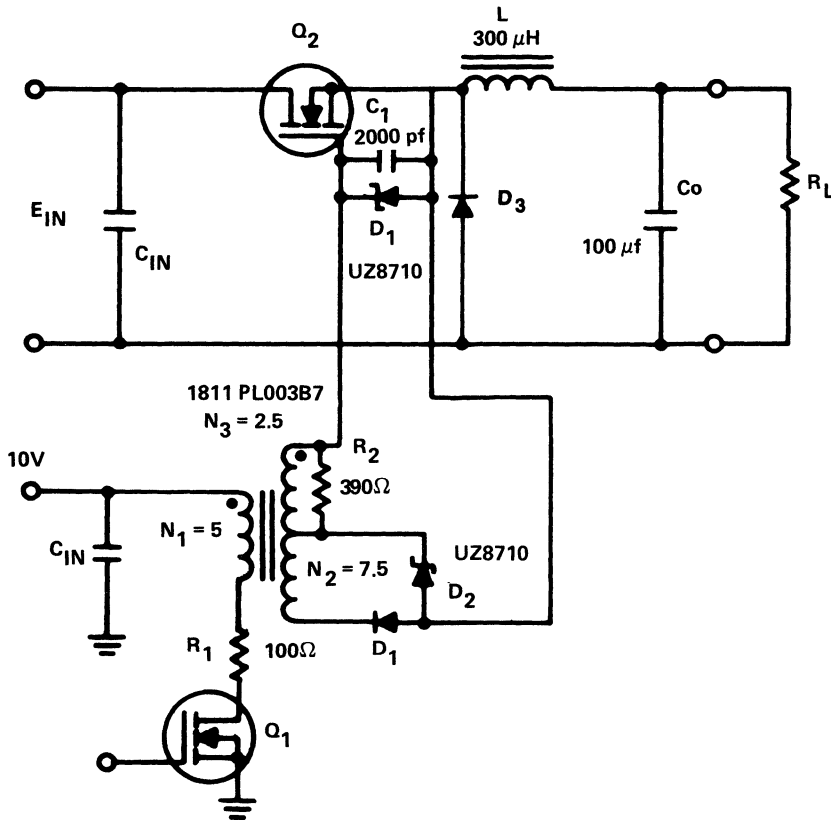


Figure 5.4 Fall Time Enhancement Drive Circuit

5.b. Pulse Drive Circuit

In some applications, as in a line driver, it is essential that power MOSFETs switch rapidly both during turn-on and turn-off. The drive circuit shown in Figure 5.5 provides these fast switching times while conserving drive power from the low voltage supply. The circuit is capable of switching a device with a high (2500 pf) gate input capacitance in 12 to 15 nanoseconds. During off time, low impedance is maintained across gate to source. This prevents turn-on of the power MOSFET due to dv/dt or noise at the drain terminal. The drive circuit can be operated from 1KHz to 100 KHz without any changes. For low cost, it utilizes an inexpensive ferrite bead as a current transformer.

The drive circuit operates from a 25V power supply. The transformer is driven by a Unitrode UC1524A pulse width modulator control chip. With Q_3 off when the output transistor of the UC1524A turns on, the voltage V_{C_1} is impressed across the primary of current transformer T_1 . The energy stored in the capacitor C_1 is, thereby, transferred to the T_1 secondary. Secondary current flows through capacitor C_2 , winding N_2 , diode D_3 , diode D_4 , small signal MOSFET Q_2 and back to capacitor C_2 . The secondary current discharges the initially charged capacitor C_2 . MOSFET Q_2 turns off when the voltage across C_2 drops below the gate threshold voltage of Q_2 . The negative voltage across the gate to source of Q_2 is clamped to a safe value by diode D_1 . Now the secondary current starts to flow into the input gate capacitance of the output power MOSFET Q_3 . When the gate voltage reaches the gate threshold voltage, Q_3 will begin to turn on. The gate voltage will continue to rise until the current transformer saturates and the current in the secondary ceases. The voltage across winding N_2 drops to zero. Charge stored in the gate capacitance of Q_3 is maintained because diode D_4 is back biased by the resulting gate voltage. The rate at which the gate capacitance discharges depends upon the leakage current of D_4 and the I_{DSS} of Q_2 .

For $1.0 \mu A$ total leakage current, it will require about 25 milliseconds to discharge a device with a 2500 pf input capacitance.

When the output transistor of the UC1524A turns off, the magnetizing energy stored in the current transformer is transferred by current flow to the secondary circuit. The current will flow in the loop which consists of diode D_2 , winding N_2 , and capacitance C_2 in parallel with the input capacitance of Q_2 . When the voltage on the gate reaches the threshold voltage, Q_2 turns on and discharges the gate capacitance of Q_3 with a low impedance, resulting in fast turn-off.

Capacitor C_2 remains charged because it has no discharge path. This keeps Q_2 on and Q_3 is held off. This prevents turn-on of Q_3 due to any dv/dt present at the drain terminal of Q_3 , which is particularly useful in PWM half-bridge switching regulator circuits.

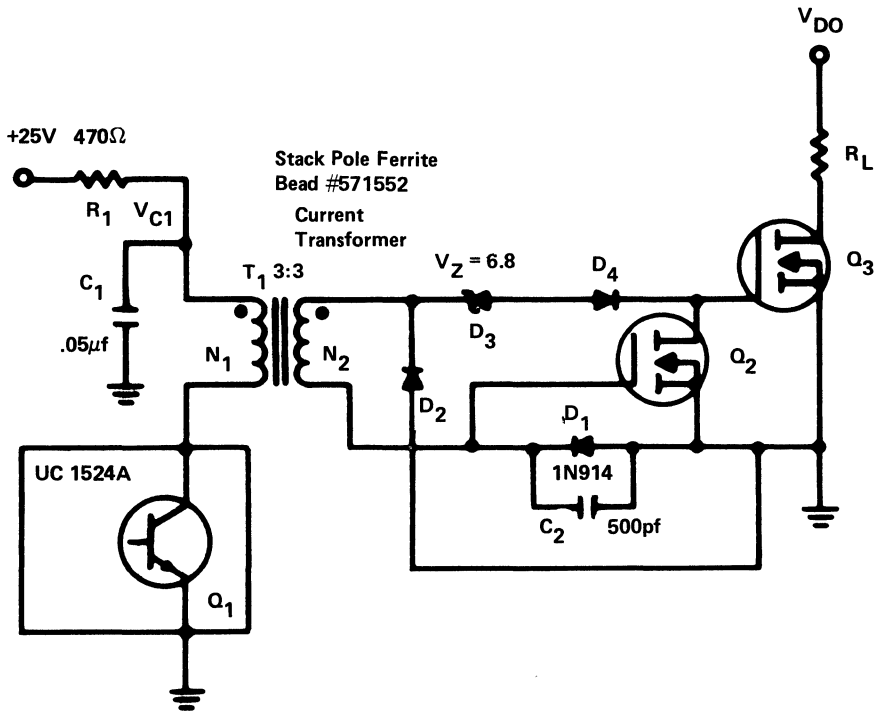
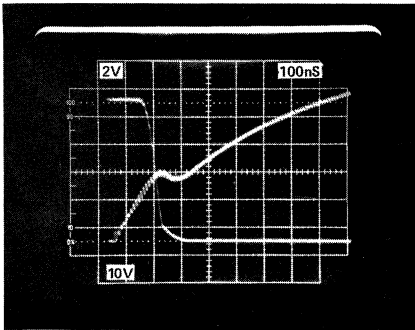


Figure 5.5 Pulse Drive Circuit

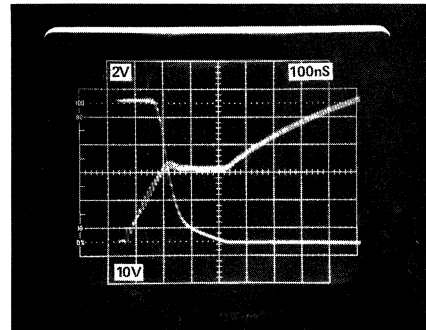
The power drawn from the drive circuit power supply is minimized by using this current pulse drive circuit, especially when operating at a low frequency for fast switching applications.

The switching times of a Unitrode power MOSFET are compared with those of a competitive device in Figure 5.6. The circuit described above was used. The devices have the same voltage and current ratings and comparable $R_{DS(on)}$. The Unitrode UFN44C1 switches faster, due to its 20 percent lower gate-to-drain and gate-to-source capacitances, than the competitive device.

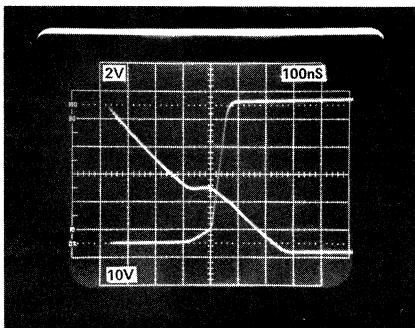


Unitrode UFN44C1

– Turn-on Time –

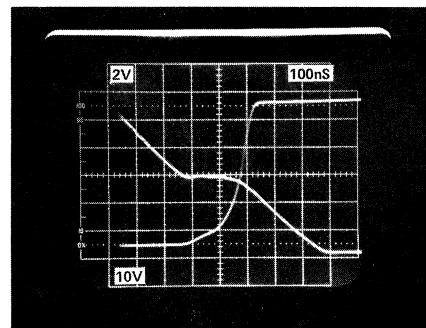


Competitive Device



Unitrode UFN44C1

– Turn-off Time –



Competitive Device

**Figure 5.6 Switching Times of Unitrode UFN44C1 Power MOSFET vs
Competitive Device with Same Voltage and Current Ratings**

Conclusion

The use of power MOSFETs in switching regulated power supplies is advantageous due to their fast switching capability with simple drive circuits. The overall system cost can be further reduced by operating these power MOSFETs at a high frequency. The reliability of the switching power supply is improved due to lack of forward or reverse bias second breakdown in the device and due to reduced parts count.

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOSFET DRIVE

Introduction

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced (it is available from Unitrode as the UC1524). Although this device, as well as the MC3420 and TL494 which followed it, contained all the basic control elements required for switching regulator design; practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical power FETs which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs. In order to be able to take full advantage of the speed

capabilities of power FETs, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the UC1525A, and its complimentary output version, the UC1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Integrating More Power Supply Functions

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in *Figure 1*, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp

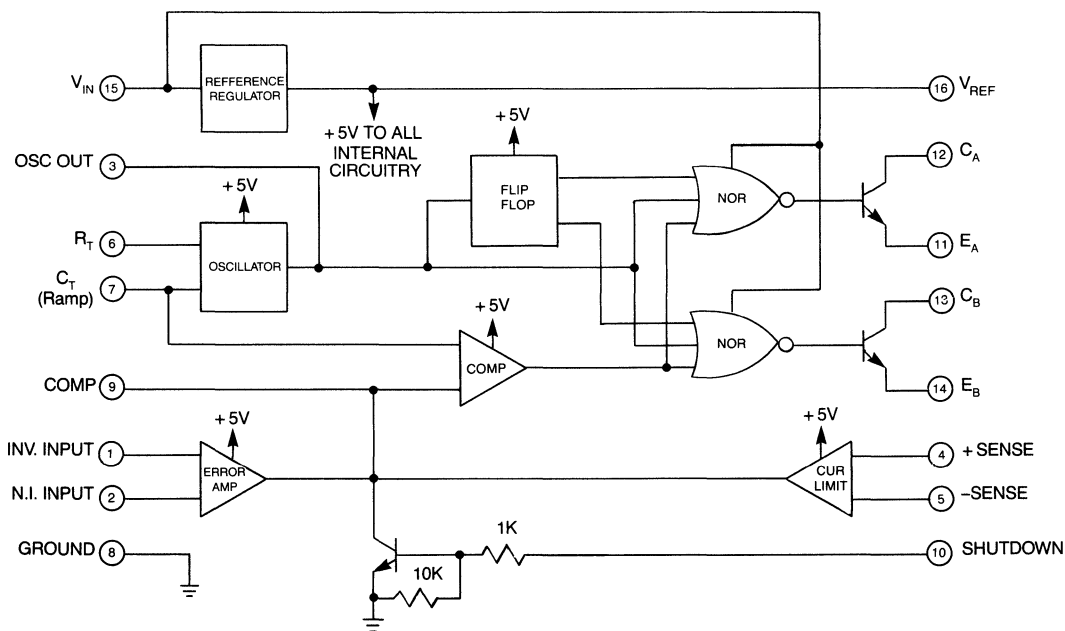


Figure 1. The UC1524 Regulating PWM Block Diagram. This design was the first complete IC control chip for switch mode power supplies.

waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the UC1525A is shown in Figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the

UC1525A device defined by an output configuration which is high during the ON pulse, and the UC 1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the UC1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

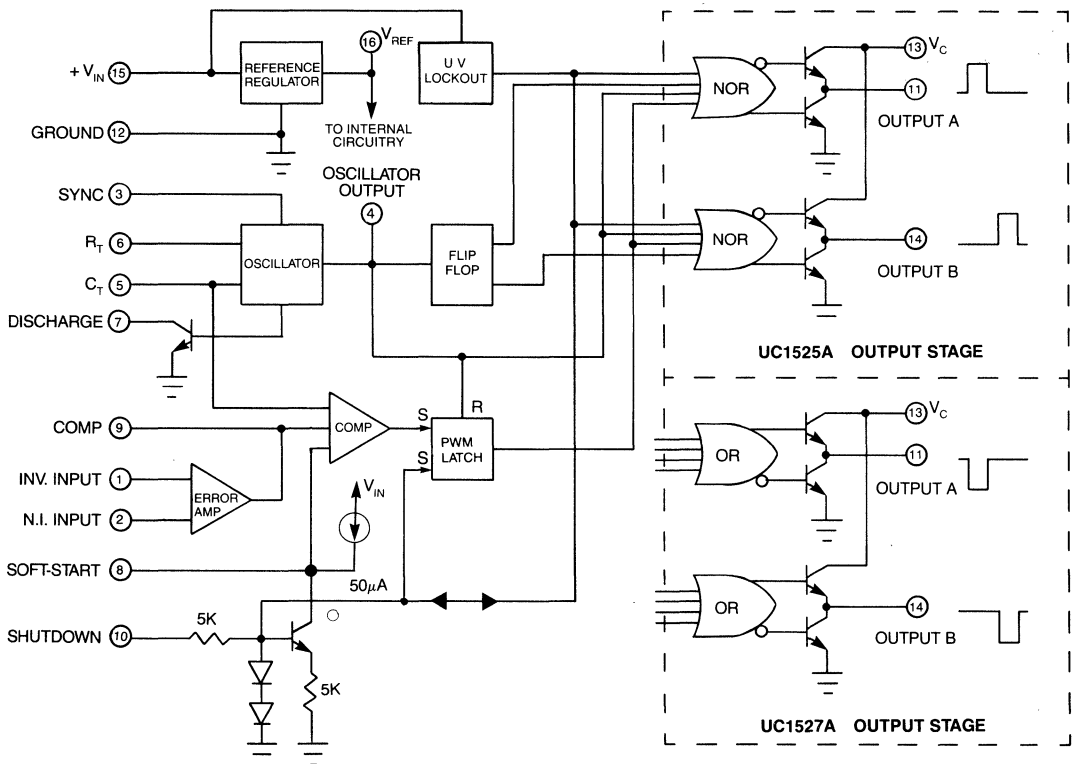


Figure 2. The UC1525A family represents a "second generation" of IC controllers.

“Totem-Pole” Output Stage

One of the most significant benefits in using the UC1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the UC1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or FET. The circuit schematic of one of the two output stages contained within the device is shown in Figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C . Note that V_C is a separate terminal from the V_{IN} supply to the rest of the device. This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_{IN} , the output cannot rise higher than approximately $1\frac{1}{2}$ volts below V_{IN} .

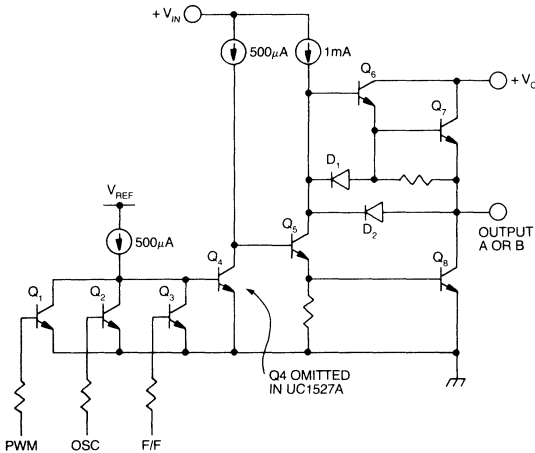


Figure 3. One of two power output stages contained within the UC1525A which conduct alternately due to the internal flip-flop.

During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at V_C is shown in Figure 4. This transient will normally be decoupled from the rest of

the control power by a 0.1mfd capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

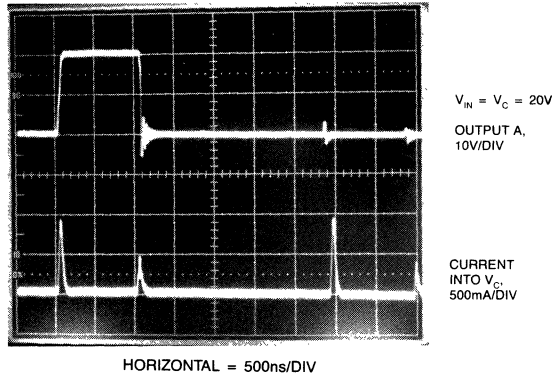


Figure 4. Current “spiking” on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

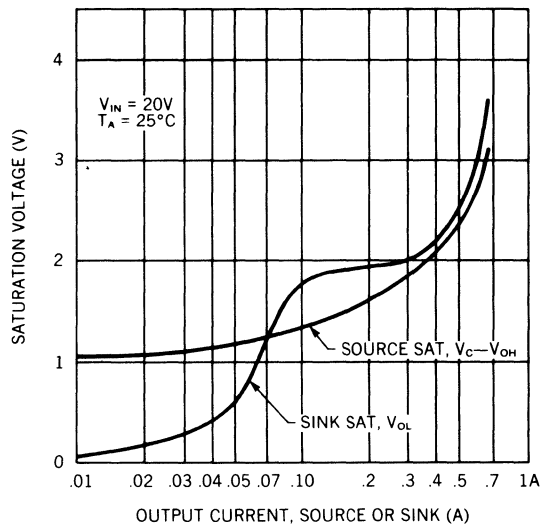


Figure 5. The output saturation characteristics of the UC1525A provide both high drive current and low hold-off voltage.

The output saturation characteristics of this stage are shown in *Figure 5*. The source transistor, Q_7 , is a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400mA under the assumption that $V_{IN} \geq V_{CC}$. The sink transistor, Q_8 , however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8 . With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

A typical output configuration for a push-pull, bipolar transistor power stage is shown in *Figure 6*. With a steady state base drive current from the UC1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the UC1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1 . With the values given, the output current and voltage waveforms are

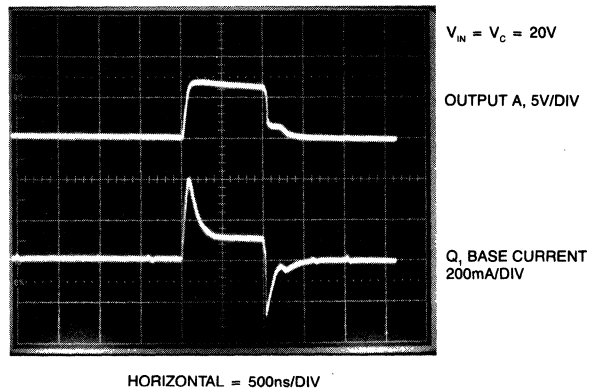


Figure 7. Base current waveforms (Figure 6 circuit) show the enhanced turn-on and turn-off current possible with the UC1525A.

shown in *Figure 7* for a one microsecond pulse. If power FETs are used for the output switches as shown in *Figure 8*, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the FET.

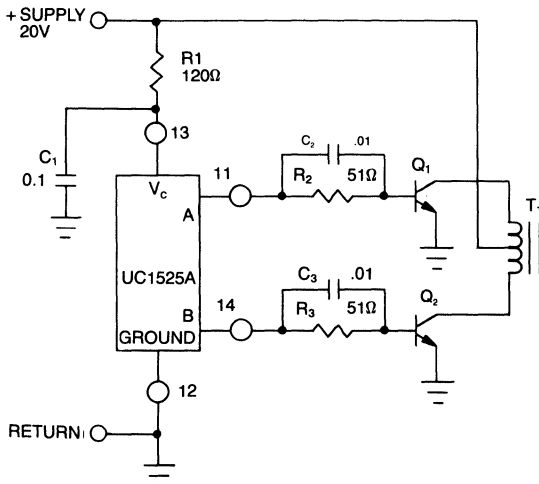


Figure 6. A typical push-pull converter power stage using external bipolar power transistor switches.

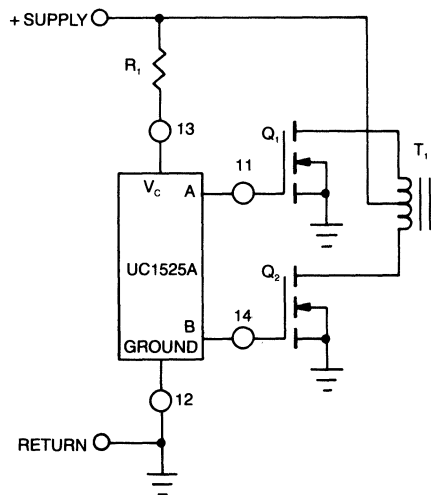


Figure 8. Replacing bipolar transistors with POWER MOSFETs provides even greater simplicity due to the low driving impedances of the UC1525A in each transition.

Push-pull direct transformer drive is also particularly advantageous with UC1525A as shown in Figure 9. A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for 1/2 bridge and full bridge switching. The configuration of Figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the UC1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

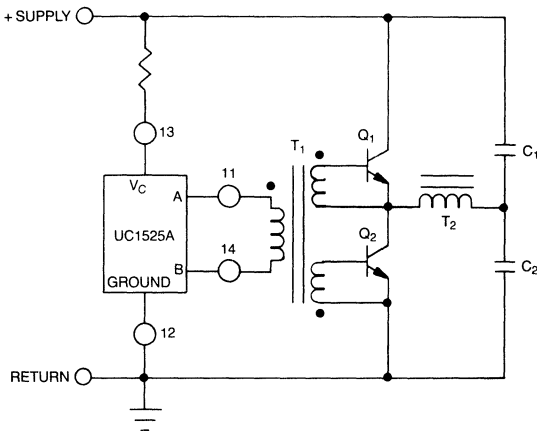


Figure 9. The UC1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary centertap.

A useful single-ended configuration, typical of buck regulators, is shown in Figure 10. Here the UC1525A outputs are grounded and the PWM signal is taken from the Vc terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

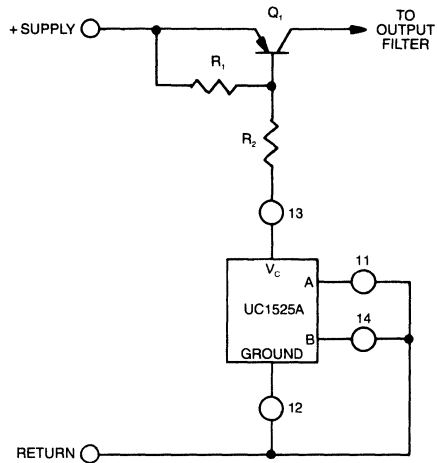


Figure 10. A single-ended, ground-referenced power stage for a flyback or boost regulator.

Controlling Power Supply Start-Up

Although the advantages of the UC1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the UC1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2 1/2V of supply voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining UC1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100% duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50µA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in Figure 11.

Q₃ and Q₄ are the output gates normally driven by the oscillator through D₂ to provide output blanking between pulses. (One of these transistors is shown as Q₂ in Figure 3.) At low supply voltages, Q₂ conducts with base drive from the 20μA current source. Q₂ provides three functions. First, current through R₄ activates the output gates with minimum voltage drop. Second, current through R₅ activates the shutdown transistor Q₅ holding the soft-start capacitor, C_{SS}, discharged. Third, R₂ provides a small bucking voltage across R₃ for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q₁, that transistor turns on. This turns off Q₂, activating the outputs and allowing C_{SS} to begin to charge from the internal 50μA current source. The time to reach approximately 50% duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\mu\text{A}} \right) C_{SS}$$

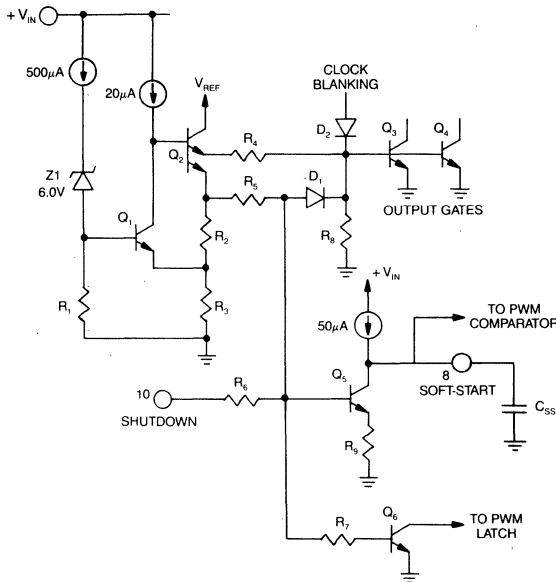


Figure 11. The internal power turn-on, soft-start, and shutdown circuitry of the UC1525A.

Power Supply Shutdown

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the UC1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to Figure 11, the base of Q₅ is turned on by a signal which is clamped to approximately 1.4V by the action of D₁ and the V_{BE} of gates Q₃ and Q₄. This holds the outputs off and keeps C_{SS} discharged by Q₅ which, with R₉, becomes a 100μA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D₁. Second, the PWM latch is set by Q₆ so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q₅ is activated commencing a 100μA discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than 1/3 of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start. Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

Regulating PWM Performance Improvements

The UC1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to 5.1V ± 1% during manufacture, eliminating the need for adjusting potentiometers in most applications.

Error Amplifier: The UC1525A uses the same basic transconductance amplifier as the UC1524 with an important difference: it is powered by V_{IN} rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An

important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the UC1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The UC1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the UC1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the UC1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple UC1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of *Figure 12* for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8 , which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2 . The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D . As long as C_T is discharging, the clock output is high, blanking the outputs. Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T (.07R_T + 3R_D)}$$

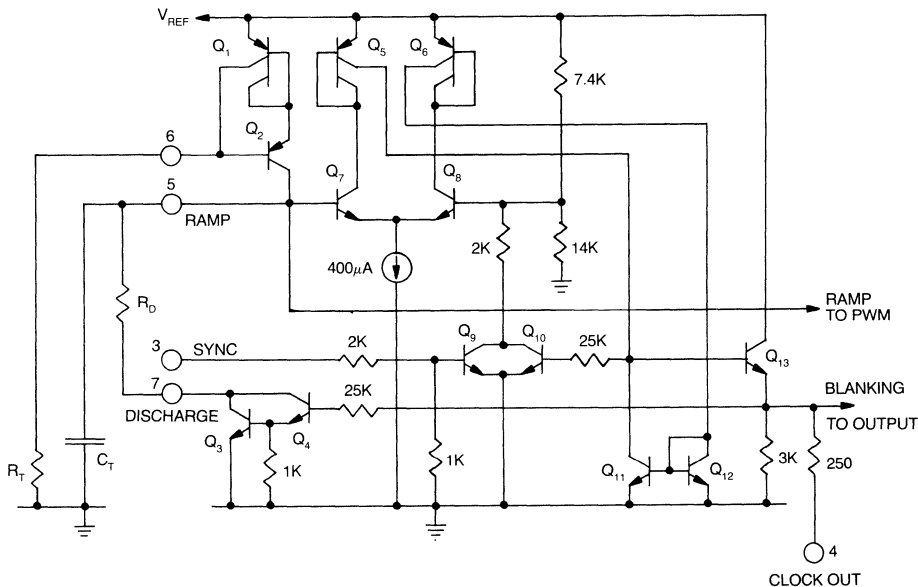


Figure 12. A simplified schematic of the UC1525A's oscillator circuitry.

External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9 , lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple UC1525A devices together, one need only to define a master with the correct $R_T C_T$ time constant, connect its output pin to the slave sync pins, and set each slave $R_T C_T$ for a time constant 10–20% longer than the master.

A 200 Watt, Off-Line, Forward Converter

The ease of interfacing the UC3525A into a practical power supply system can be illustrated by the off-line, power converter shown in *Figure 13*. This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a SG723 or LM305. One other undefined block in *Figure 13* is the auxiliary power supply which supplies the low voltage, low current bias supply for the UC1525A and the drive for Q_1 , the power switch. The choice of the UFN44C2 POWER MOSFET

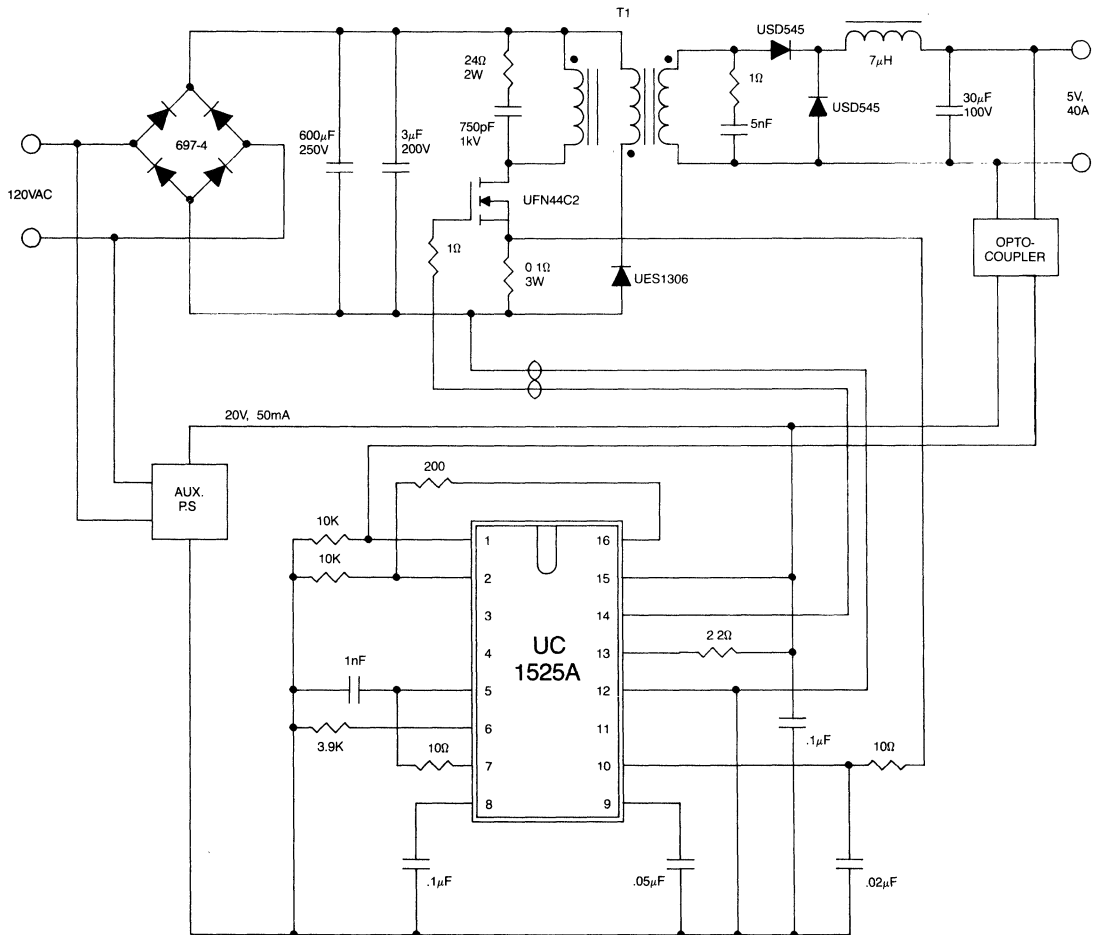


Figure 13. 200W, Off-Line Forward Converter.

for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150kHz which is accomplished by running the UC1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the .05 μ F capacitor on pin 9.

The totem-pole output of the UC1525A is used to advantage to drive Q₁ by providing a 400mA peak current to charge and discharge the MOSFET's gate capacitance while keeping overall power dissipation low. Waveform

photographs of this operation are shown in *Figure 14*.

When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected. Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in UFN44C2 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the UC1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

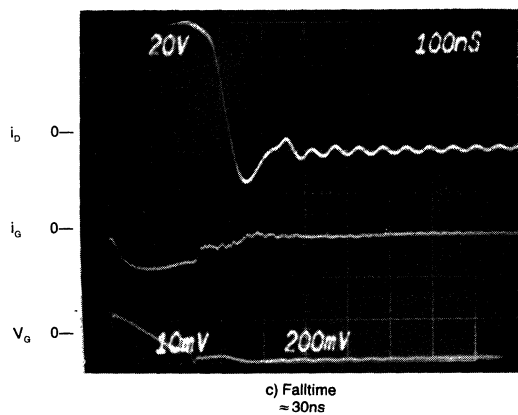
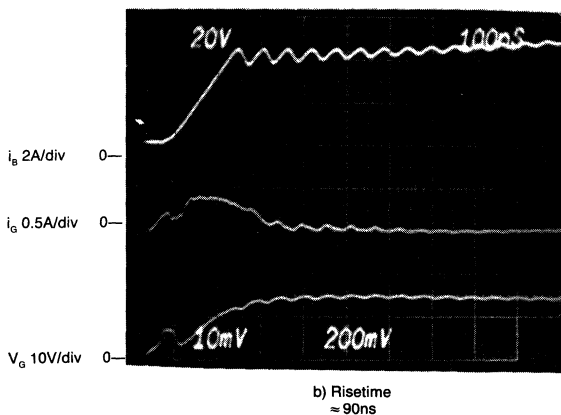
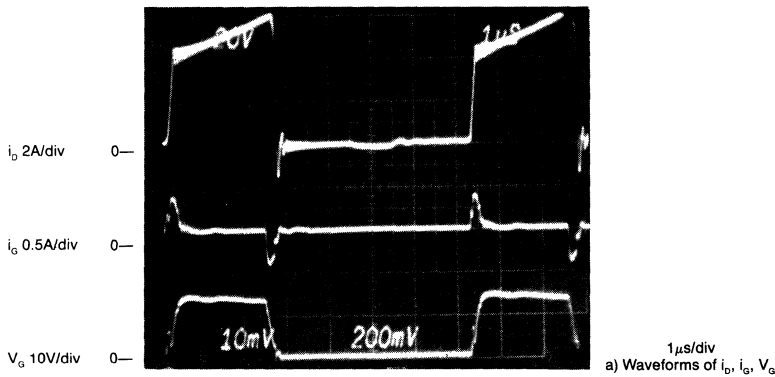


Figure 14. Current and voltage waveforms for the 200W, Off-Line Forward Converter with a UC1525A direct driven MOSFET Power switch. (Operating frequency is 150kHz with output current equal to 40A.)

Transformer Winding Data

500 Watt, 100kHz, Off-Line, Half-Bridge Converter

T1 Core: Ferrox 486T250-3C8

Pri: 14T #22AWG

Sec (2): 7T #22AWG

T2 Core: Ferrox EC52-3C8 (EE)

Pri: 14T, 2 layers, 2 #16 AWG in parallel

Sec (2): each 2T, C.T., copper strap .01" x .8"

T3 Core: Ferrox 486T250-3C8

Pri: 1T

Sec: 20T, C.T. #22AWG

T4 117V/220V, 25V, 0.15A, 50-60Hz

L1 Core: Ferrox IF30-3C8

4 turns, 5 #12AWG in parallel

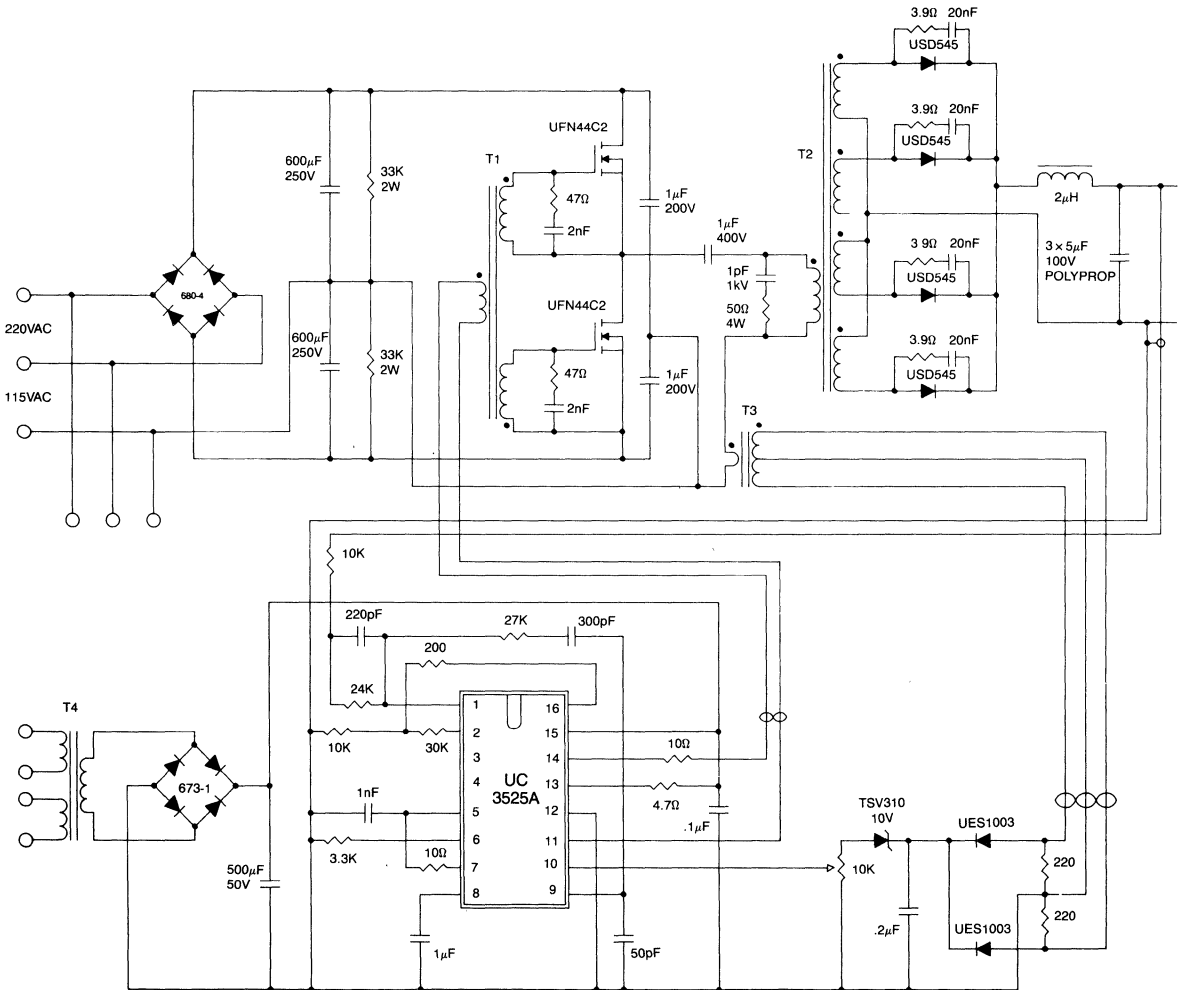


Figure 15. 500W, 100kHz Half-Bridge Schematic.

500 Watt, Off-Line, Half-Bridge Converter

The circuit shown in *Figure 15* uses a pair of Unitrode UFN44C2 POWER MOSFETs in a half-bridge configuration with the UC1525A chip referenced to the secondary side of the power transformer. The MOSFET gates are driven directly from the control chip output through step down and isolation transformer T₁. The UC1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T₁. This provides the fast, high current turn-on and turn-off pulses needed for the MOSFET gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the UC1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T₁ minimize ringing due to the MOSFET gate capacitance and the inductance of T₁ and lead inductance, particularly during deadtime.

Deadtime for the UC1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the MOSFETs have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

Current limiting is provided by current transformer T₃ in series with the primary of the power transformer T₂. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the UC1525A.

Waveforms of the converter are shown in the scope photos of *Figure 16*. Current rise and fall times are 20ns and 10ns. For additional details on this design, see Unitrode Application Note U-87, a 500W, 200kHz Off-Line Power Supply using POWER MOSFETs.

Improved Performance; Less Complexity

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the UC1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

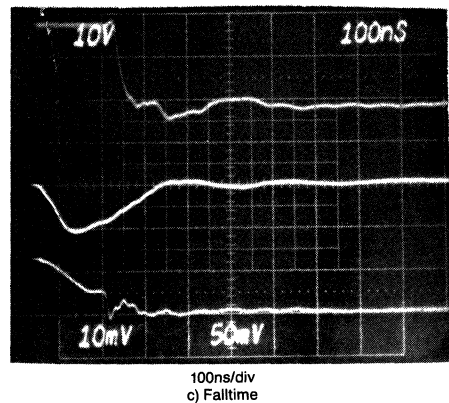
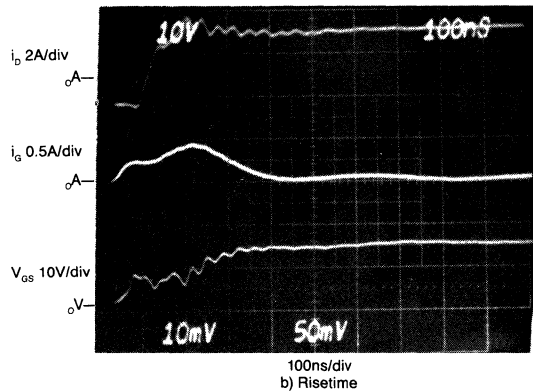
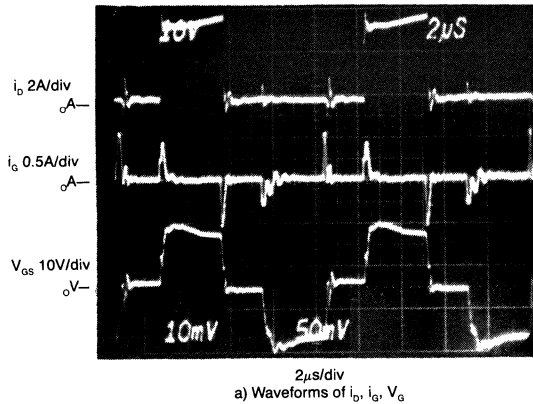


Figure 16. Performance waveforms for the Half-Bridge, 500W, 100kHz Converter with output current of 80A.

THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

Introduction

The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real world of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of

fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that design engineers still preferred the 1524 for its wide versatility and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. Thus, Unitrode undertook this task. The result is the UC1524A.

The UC1524A PWM Controller

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In

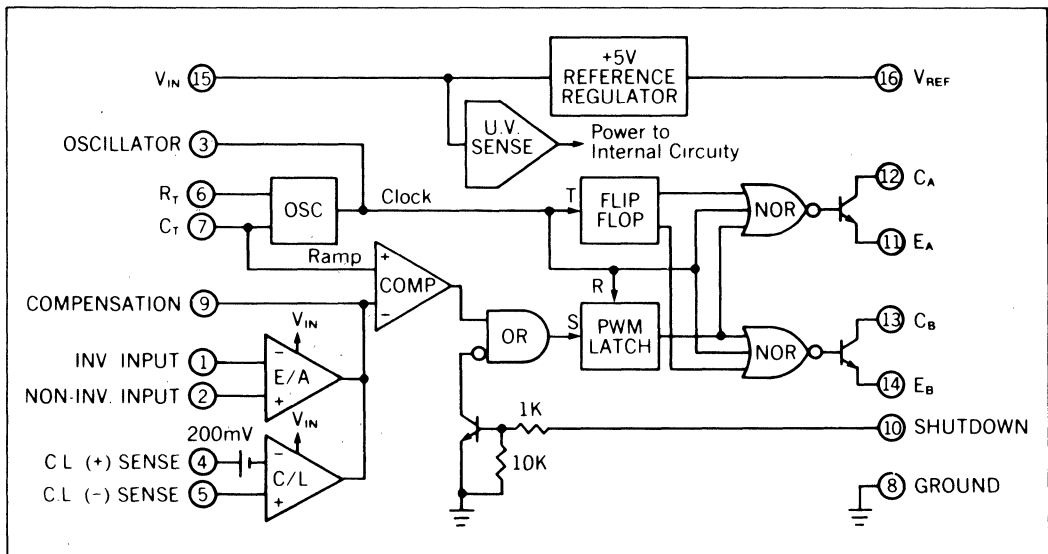


FIGURE 1 — The UC1524A Block Diagram Follows the Same Architecture As the UC1524 But With Several Significant Differences.

this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be a cost advantage in using the UC1524A in new designs. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to $\pm 1\%$ accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds directly to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500kHz and is easier to synchronize with an external clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

Internal Power Turn-on Circuit

The under-voltage lockout and turn-on hysteresis circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_{IN} rises above 2V, R_2 begins to

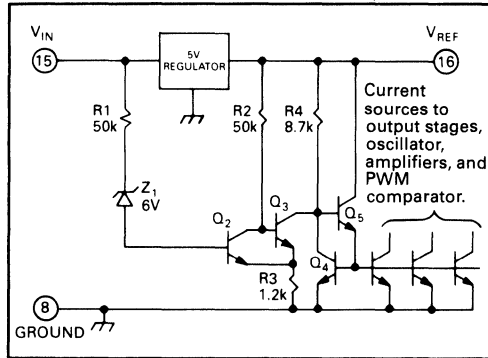


FIGURE 2 — The Under-Voltage Lockout and Power Turn-On Circuitry within the UC1524A.

conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3 , developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4 , a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode Z_1 begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3 , the voltage across R_3 drops, providing positive feed-

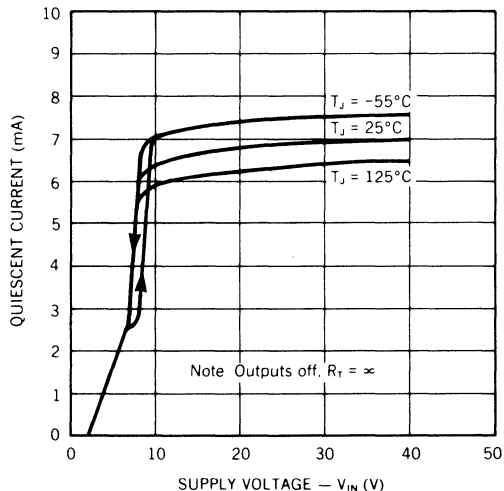


FIGURE 3 — Supply Current for the UC1524A vs. Input Voltage.

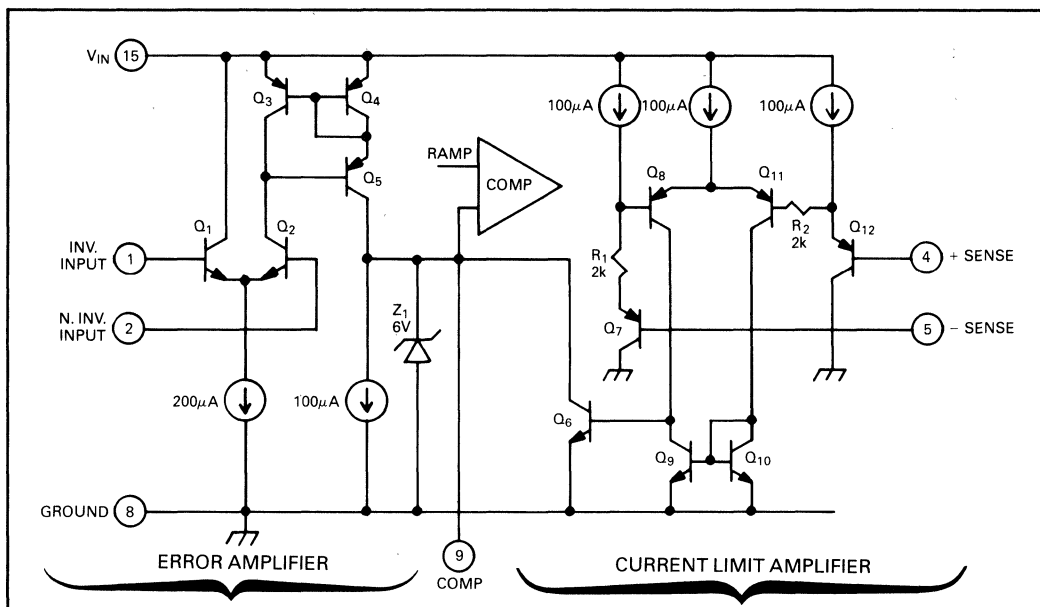


FIGURE 4 — Voltage and Current Sensing Amplifiers Have a Common Output at the Input to the PWM Comparator.

back. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

A New Current Limit Amplifier

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5 , must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524A with one exception: it is now powered by V_{IN} instead of V_{REF} , so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1 , is used on the

output to keep the input level to the PWM comparator below 6 volts.

The error amplifier's output can be considered a $100\mu\text{A}$ current source or sink (0 - $200\mu\text{A}$ source with $100\mu\text{A}$ constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q_6 through Q_{12} . Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within $-2V$ of V_{IN} . Its threshold, or offset, of 200mV is established by the $100\mu\text{A}$ current source through R_1 , with R_2 added to null out the effect of any base current from Q_8 .

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to

error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100µA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

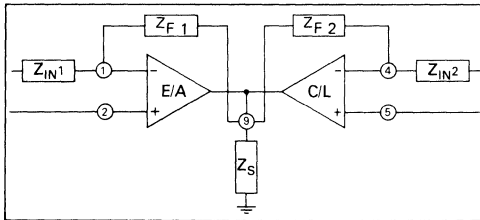


FIGURE 5 — Various Compensation Options Which Are Possible When Both Amplifiers Are Operated in the Linear Mode.

An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R₁ is made 100k, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin 10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of -2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

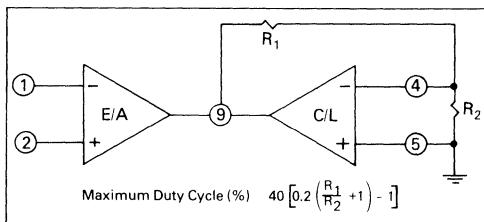


FIGURE 6 — The Fixed 200mV Threshold of the Current Limit Amplifier Can Be Multiplied to Form a Duty-Cycle Clamp or Dead-Band Control.

PWM Comparator and Latch

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to blank the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

There are several significant advantages to this circuit. First, the latch completely eliminates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossings of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance of this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

Higher Power Output Switches

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirements, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds

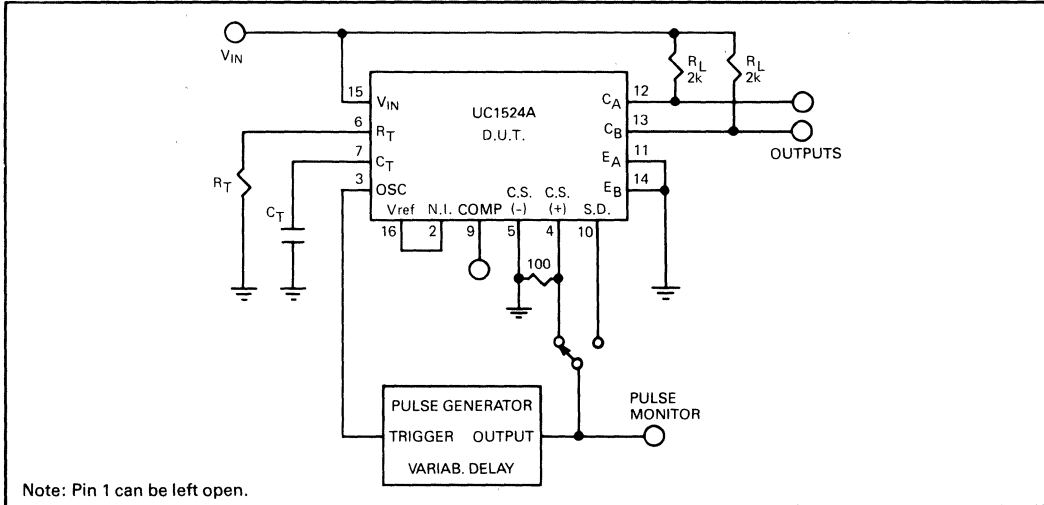


FIGURE 7 — Evaluating the Turn-off Delays of the UC1524A with the Aid of a Triggerable Pulse Generator With Variable Delay.

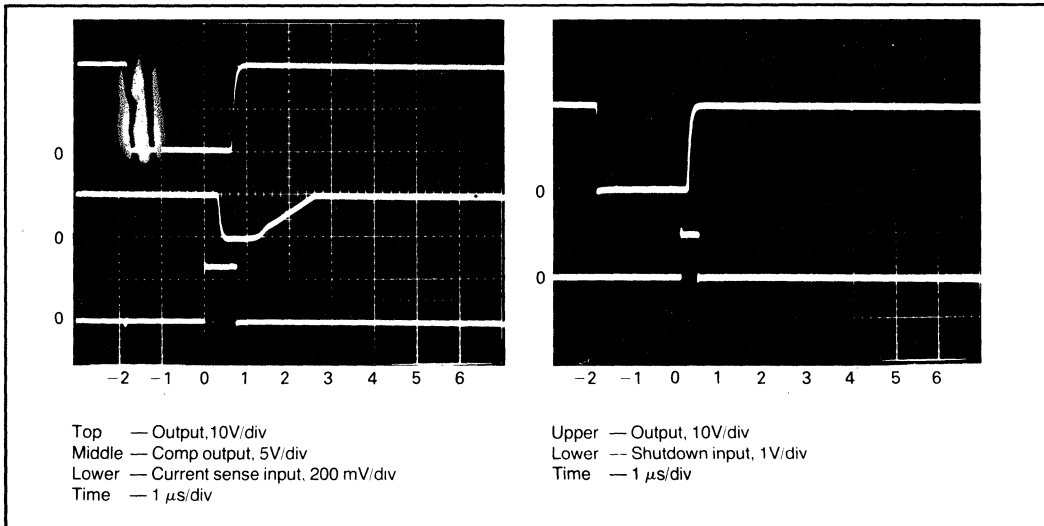


FIGURE 8 — Typical Turn-off Response From Both the Current Sense and Shutdown Inputs.

somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay. Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful config-

uration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1 , is capacitively coupled to saturate an external transistor, Q_2 , greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3 . Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

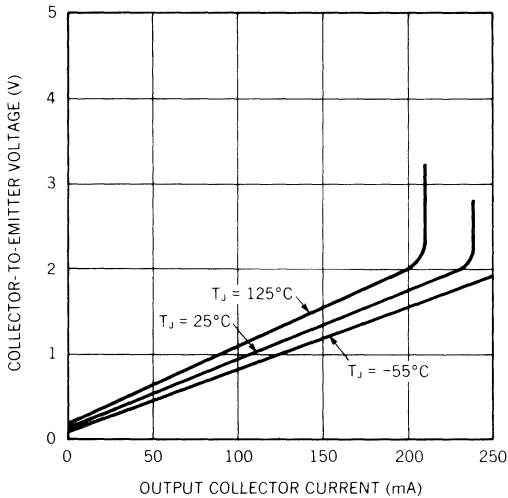


FIGURE 9 — Output Saturation Characteristics for Each of the UC1524A's Outputs.

Frequency Synchronization

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2 . Without this component, a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5 . The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10} , momentarily reducing the threshold of comparator Q_8 - Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

As with the 1524, synchronization to an external clock should be done with the $R_T C_T$ time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the components. For synchronizing multiple UC1524A devices, all R_T , C_T , and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1 kohm minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF} . This technique is quite accurate due to the accuracy of V_{REF} and the 100 μ A fixed current available from the amplifier.

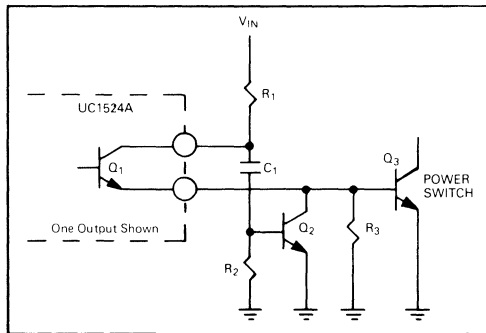


FIGURE 10 — The addition of C_1 and Q_2 Uses the Collector Signal of the UC1524A to Generate an Enhanced Turn-off Command for Q_3

A Simple Buck Regulator Circuit

The application of Figure 12 demonstrates the utility of the UC1524A used with a Unitrode PIC600 hybrid switch. This combination greatly simplifies the design of switching regulators, since the only other active device required is a small-signal 2N2222 which serves to provide a constant drive current to the output switch, regardless of the input voltage level. With the UC1524A, current sensing does not have to be done in the ground line, but will still function when the regulator output is shorted to ground.

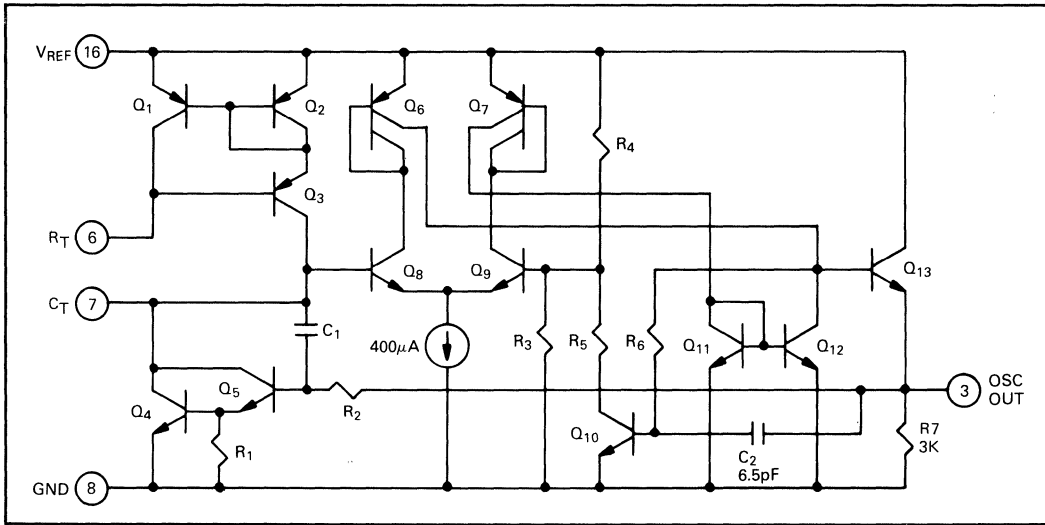


FIGURE 11 — The Oscillator Circuit of the UC1524A Allows Both High Frequency Operation and Ease of External Synchronization.

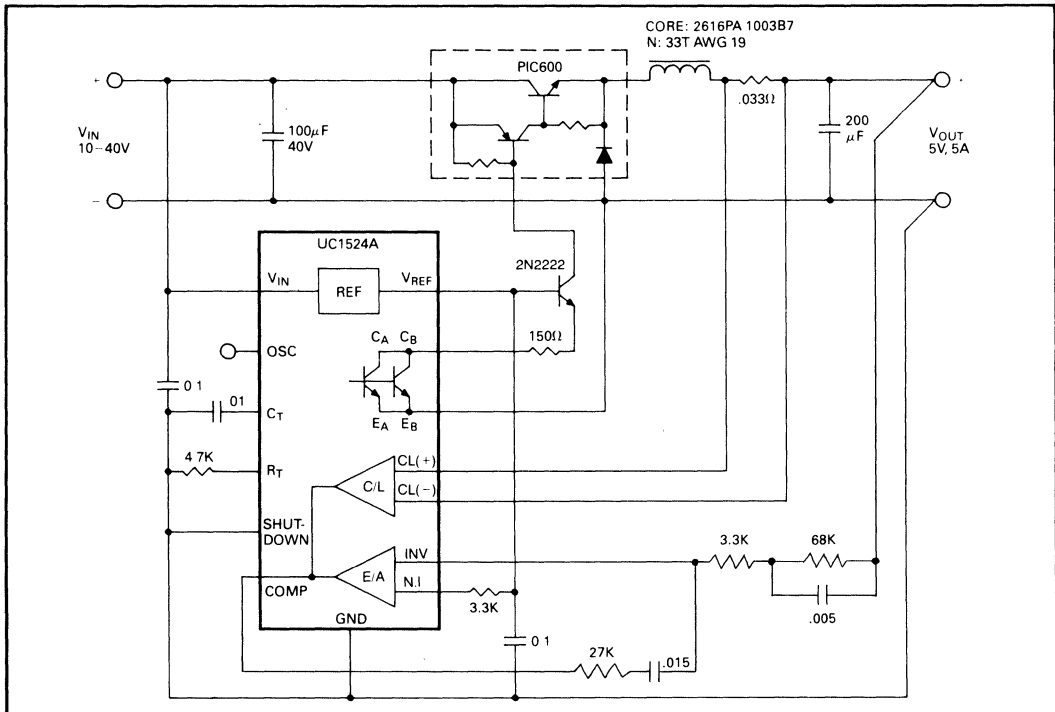


FIGURE 12 — The UC1524A Combines With the PIC 600 Hybrid Switch to Form A Simple But Powerful Buck Regulator.

The waveforms of Figure 13 demonstrate the performance of the current limiting comparator, showing that from the onset of current limiting to a complete short circuit, the peak input current increases from 5.2A to only 5.9A.

A Complete DC-DC Converter with the UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical

4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 14 uses a push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28:7 turns ratio in the transformer, a 5V, ¾A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 15.

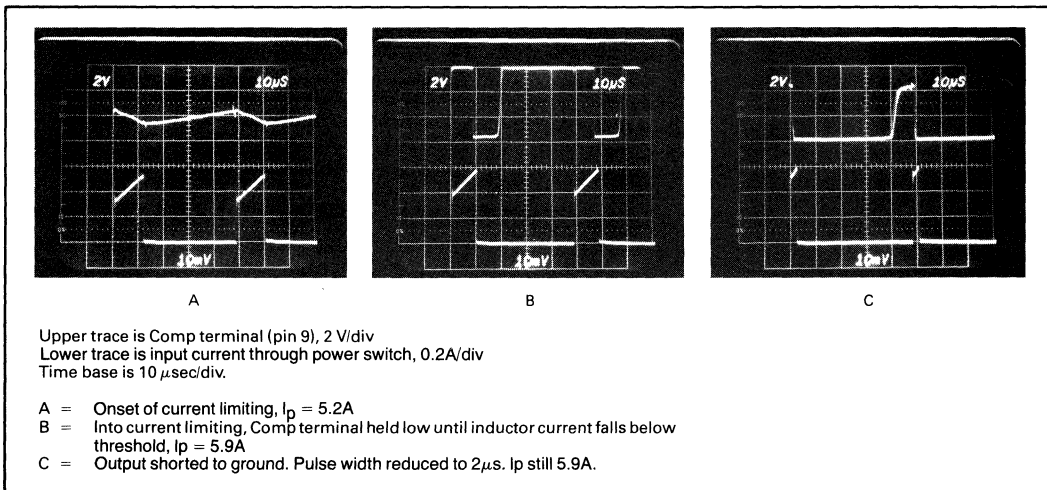


FIGURE 13 — Performance Data for Figure 14's Regulator Shows the Tight Control of Peak Current, Even Under Shorted Output Conditions.

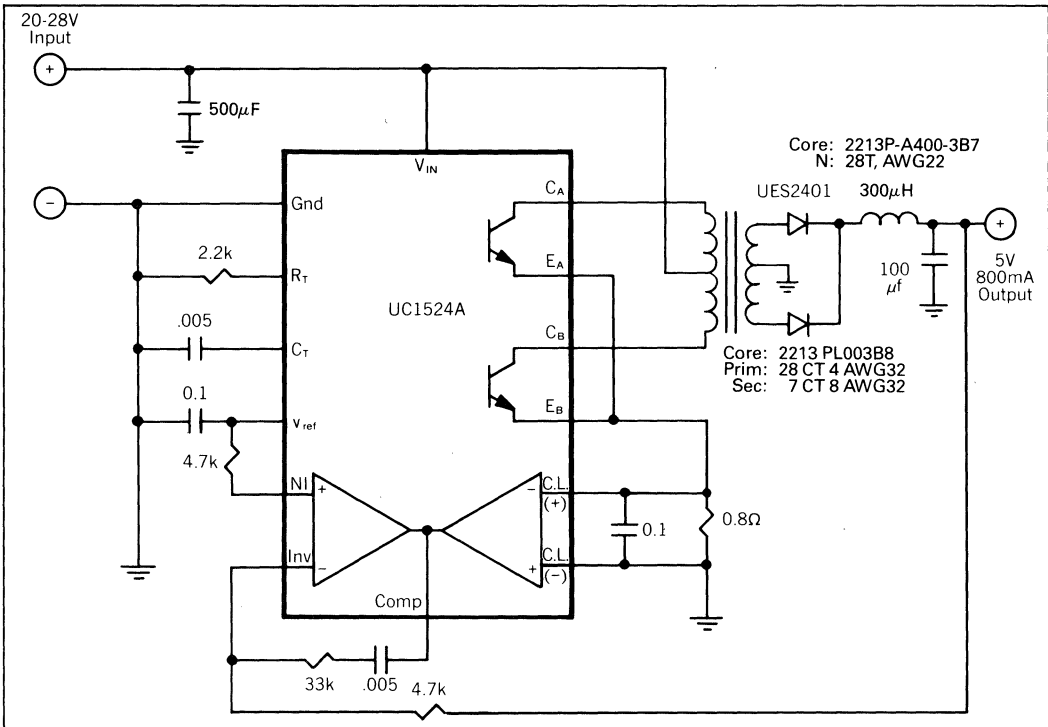
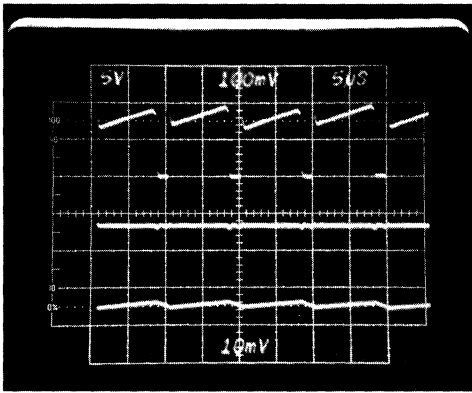
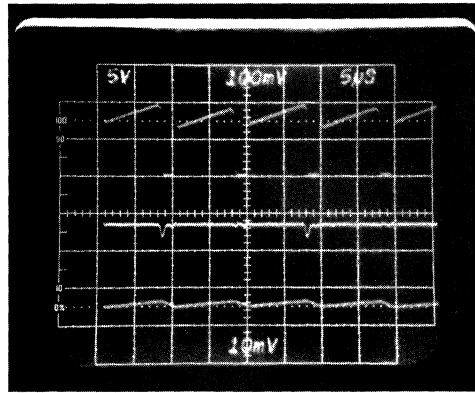


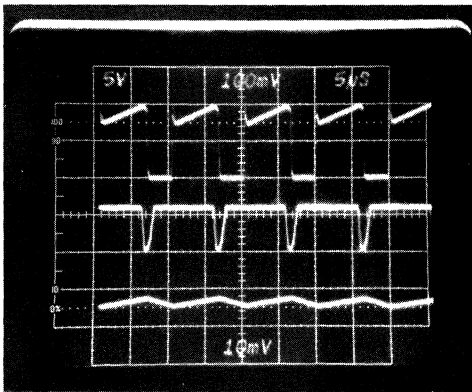
FIGURE 14 — With Higher Output Voltage Capability, the UC1524A can Implement a Complete 4 Watt DC to DC Converter with no Additional Switching Transistors.



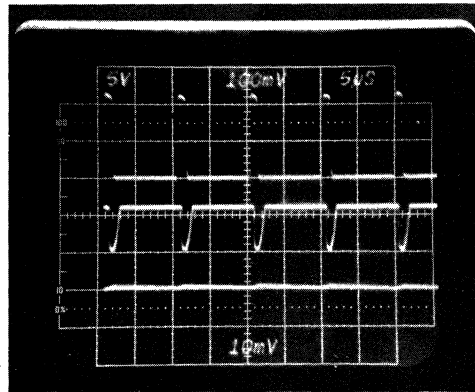
Circuit Under Normal Load



Circuit at Threshold of Current Limiting



Circuit Under Full Current Limit



Circuit Under Short Circuit Conditions

FIGURE 15 — Operating waveforms for the PWM DC-DC converter (Figure 14)

- Upper trace** = Primary current at 0.1 A/division
- Middle trace** = Pin 9 voltage at 5V/division
- Lower trace** = Load current at 0.5A/division
- Time base** = 5 μ s/division

An Off-line Forward Converter

For low to medium power applications, a single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 16 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating

drive power coming from winding N₂. The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C₂ with only approximately 8mA required through R₁.

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency by means of the 2N2222 transistor and transformer T₂. With every switching cycle, the output voltage is transferred from N₁ to N₂ where it is peak detected to generate a primary-referenced signal to drive the PWM error amplifier. Diode D₂ is used to temperature compensate for the loss in the rectifier, D₁ and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D₃

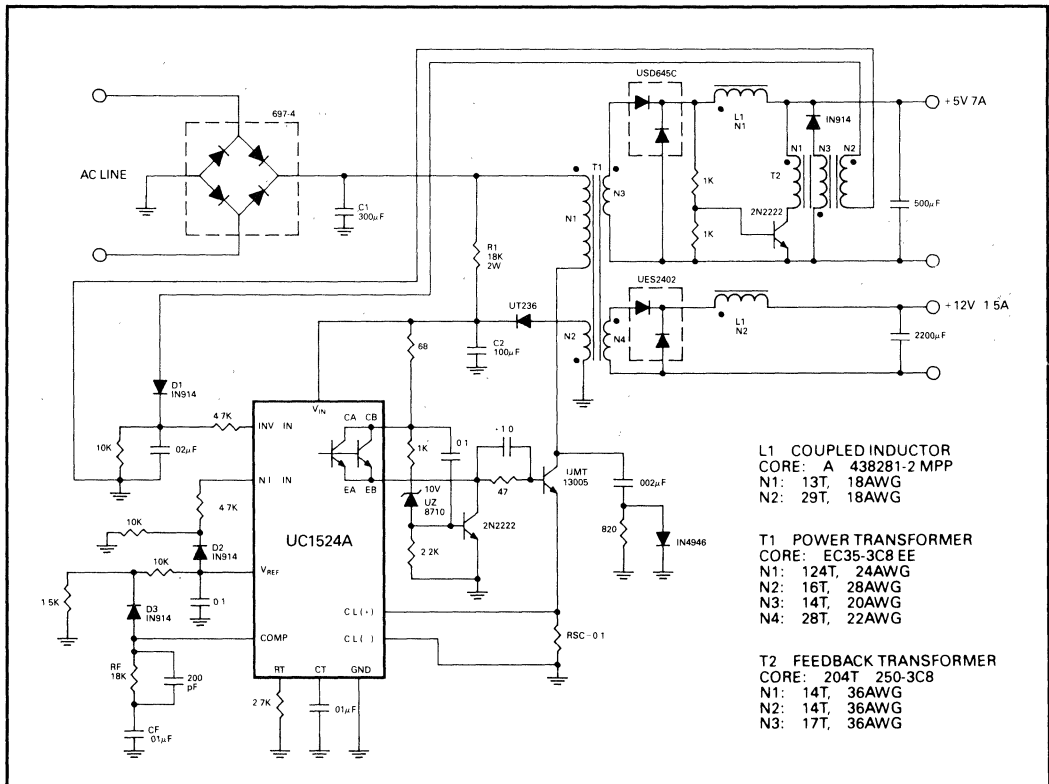


FIGURE 16 — This 50W Off-Line Forward Converter Features Both High Efficiency and Good Regulation while Maintaining Input-Output Isolation.

and the 10k - 1.5k divider from V_{REF} . This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the UMT13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the $1\mu\text{f}$ base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 17. Operating at 40kHz, this regulator provides an isolated 50W of power with an efficiency of 83%, a high degree of regulation, and fast overload protection.

Conclusion

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement: providing greater performance and versatility while reducing system costs.

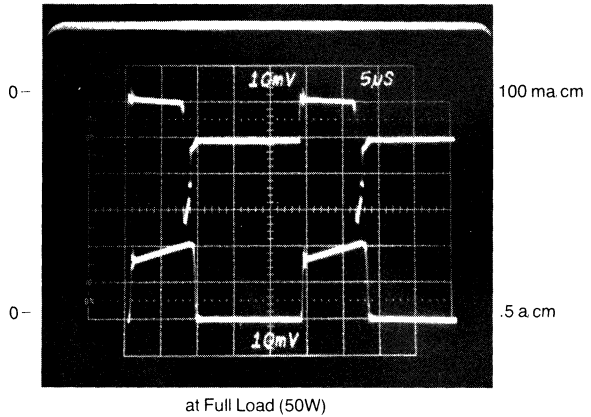


FIGURE 17 — Base Current (Upper Trace) and Collector Current for the UMT 13005 of Figure 16. The Time Base is $5\mu\text{s}$ per Division.

APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW COST, PRIMARY REFERENCED SWITCHING POWER SYSTEMS

1. Introduction

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the

control and power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

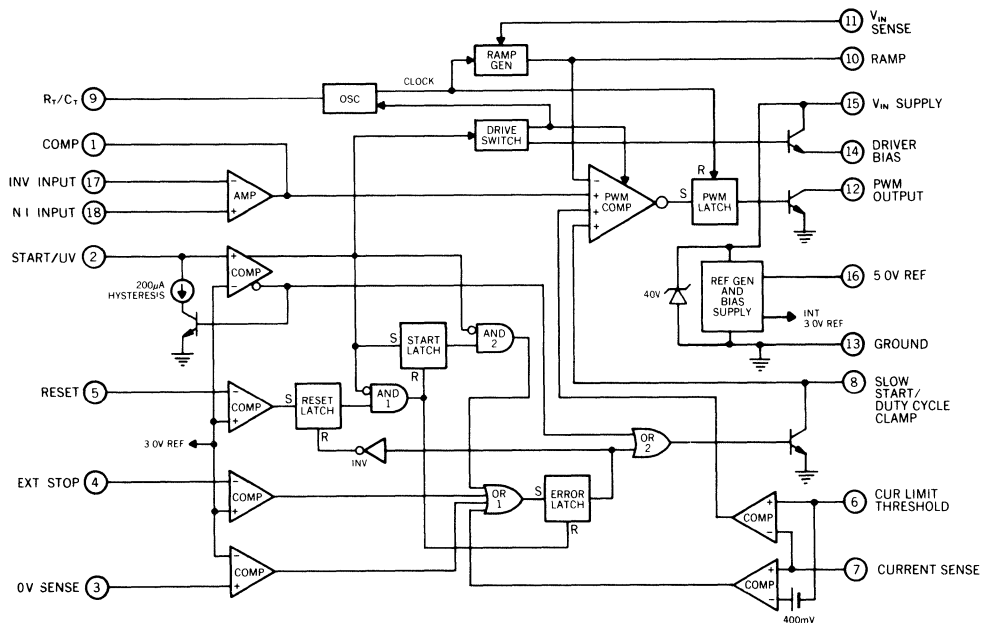


FIGURE 1. THE OVERALL BLOCK DIAGRAM OF THE UC1840, AN INTEGRATED CIRCUIT OPTIMIZED FOR PRIMARY-SIDE CONTROL OF OFF-LINE SWITCHING POWER SUPPLIES

2. The UC1840 Controller

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

- (1) Fixed-frequency operation set by user-selected components
- (2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control
- (3) A drive switch for low current start-up of the high-voltage line
- (4) A precision reference generator with internal over-voltage protection
- (5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart
- (6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch

- (7) Logic control for pulse-commandable or DC power sequencing

For an understanding of how these individual blocks work together in a typical, medium-power, flyback power supply, reference should be made to Figure 2 and the functional description which follows.

3. UC1840 Functional Description

3.1 Power Sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, V_c , to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

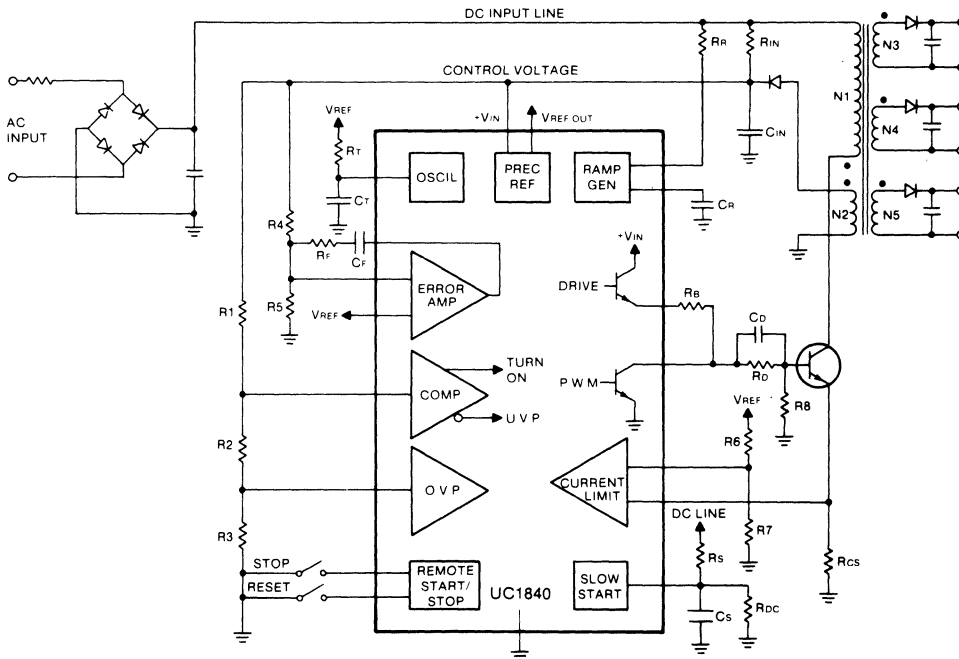


FIGURE 2. A FULLY PROTECTED, ISOLATED FLYBACK POWER SUPPLY CAN BE IMPLEMENTED WITH THE UC1840, A HIGH-VOLTAGE POWER SWITCH, THE TRANSFORMER, AND A SMALL HANDFUL OF PASSIVE COMPONENTS.

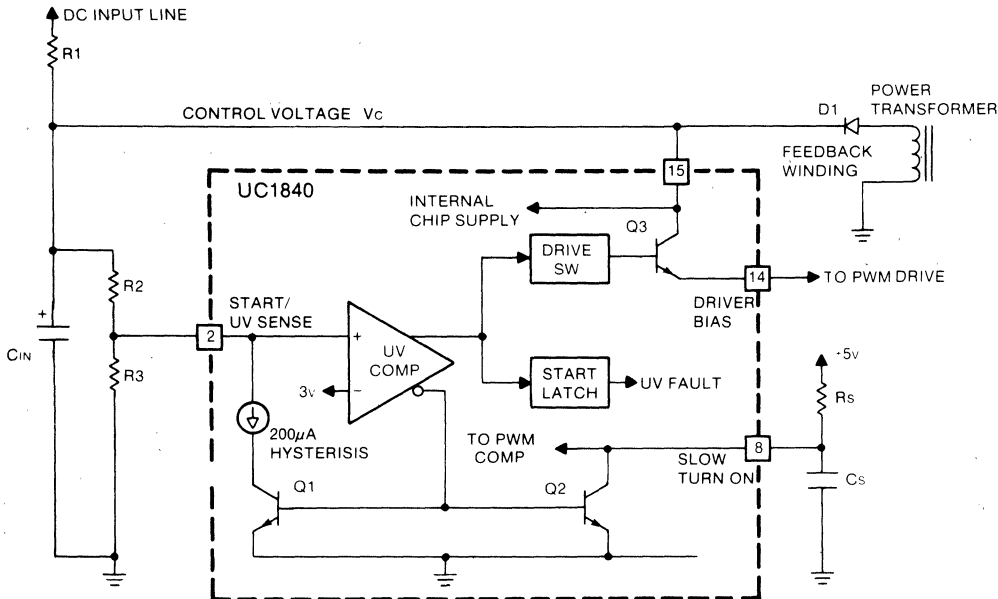


FIGURE 3. THE UC1840'S START CIRCUITRY REQUIRES LOW STARTING CURRENT FROM THE DC INPUT LINE WITH NORMAL OPERATING CURRENT SUPPLIED FROM A LOW-VOLTAGE FEEDBACK WINDING ON THE POWER TRANSFORMER

- (1) While the control voltage, V_c , is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:
 - (a) A $200\mu\text{A}$ hysteresis current is flowing into pin 2 through R_1 causing an added drop across R_2 .
 - (b) The drive switch is holding the Driver Bias transistor, Q_3 , OFF. This insures that the only current required through R_1 is the start-up current of the UC1840, plus external dividers (R_2, R_3, R_s , etc.).
 - (c) The Slow Turn-on transistor, Q_2 , is ON, holding pin 8 and C_s low.
 - (d) The Start Latch keeps the under-voltage signal from being defined as a fault.

- (2) The start level is defined by:

$$V_c(\text{start}) = 3 \left(\frac{R_2 + R_3}{R_3} \right) + 0.2 R_2.$$

When V_c rises to this level, the Start/UV

Comparator then does the following:

- (a) Turns off Q_1 , eliminating the $200\mu\text{A}$ hysteresis current. This allows the voltage on V_c to drop before reaching the under-voltage fault level defined by:

$$V_c(\text{U.V. fault}) = 3 \left(\frac{R_2 + R_3}{R_3} \right)$$
 - (b) Sets the Start Latch to monitor for an under-voltage fault.
 - (c) Activates Q_3 providing Driver Bias to the power switch, pulling the added current out of C_{in} .
 - (d) Turns off Q_2 allowing for programmed slow turn-on defined by R_s and C_s .
- (3) A normal start-up occurs with the control voltage, V_c , following the path shown in Figure 4. If the power supply does not start, V_c will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon

the status of the Reset terminal as defined under Fault Sequencing (Para. 3.4.2). If start-up does not occur because of some fault in the Driver Bias line, Vc will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp Vc to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

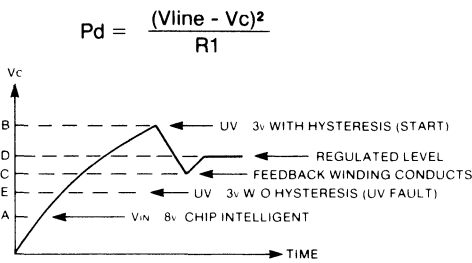


FIGURE 4 UNDER A NORMAL TURN-ON, THE SUPPLY VOLTAGE TO THE UC1840, Vc, WOULD RISE LIGHTLY LOADED TO THE START LEVEL, FALL UNDER THE TURN-ON LOAD, AND THEN REGULATE AT SOME INTERMEDIATE LEVEL

If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

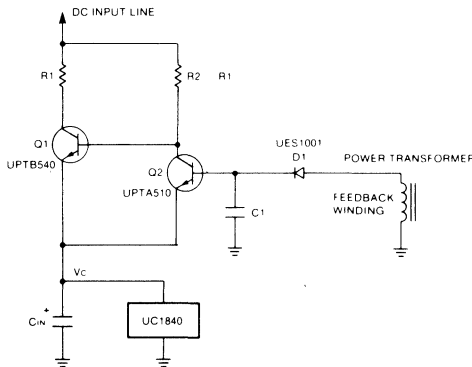


FIGURE 5. THE ADDITION OF Q1 AND Q2 CAN ELIMINATE THE STEADY-STATE CURRENT THROUGH R1 AFTER TURN-ON. Q2 IS SELECTED TO PASS ALL CONTROL CURRENT THROUGH ITS BASE-EMITTER JUNCTION.

3.2 Slow Turn-on Circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

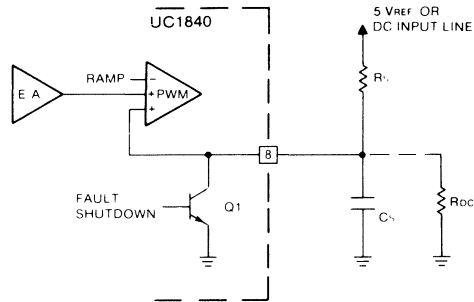


FIGURE 6 PIN 8 ON THE UC1840 CAN BE USED FOR BOTH SLOW TURN-ON AND DUTY-CYCLE LIMITING AS WELL AS A PWM SHUTDOWN PORT

When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of Cs and a charging source, such as Rs, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for Vc to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding Rdc to ground. If Rs is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line—for constant volt-second operation—then the clamp voltage on pin 8 must also vary. This is readily accomplished by connecting Rs to the DC input line. The divider voltage:

$$V_{Pin\ 8} = \left(\frac{R_{dc}}{R_s + R_{dc}} \right) V_{DC\ input}$$

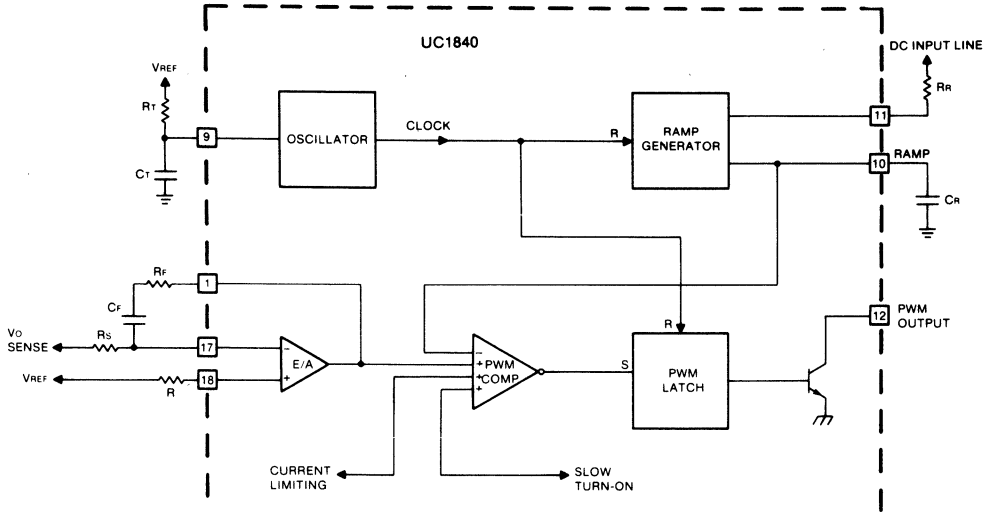


FIGURE 7. THE PULSE-WIDTH MODULATOR WITHIN THE UC1840 SEPARATES THE RAMP FUNCTION FROM THE FIXED-FREQUENCY OSCILLATOR.

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

3.3 PWM Control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

3.3.1 Oscillator

A constant clock frequency is established by connecting R_t from pin 9 to the 5V reference and C_t from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_t C_t}$$

where the value of R_t can range from 1kΩ to 100kΩ and C_t from 300pF to 0.1μF. The best temperature coefficients occur with C_t in the range of 1000 to 3000pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R_1 and C_1 are selected to provide a 0.5V, 200ns pulse across the 51Ω resistor, and R_t and C_t define a frequency slightly lower than the synchronizing source.

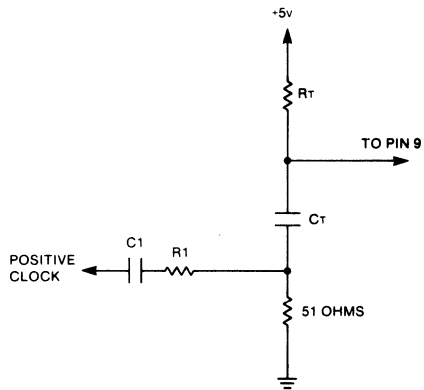


FIGURE 8. SYNCHRONIZATION TO AN EXTERNAL TIME BASE CAN BE ACCOMPLISHED BY ADDING A 51Ω RESISTOR IN SERIES WITH C_t .

To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

3.3.2. Ramp Generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

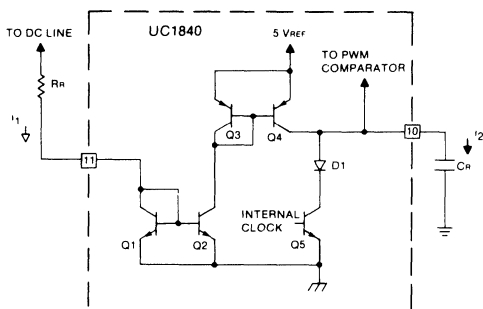


FIGURE 9. CURRENT MIRRORS Q1-Q4 ARE USED TO MAKE THE RAMP CHARGING CURRENT i_2 , LINEARLY PROPORTIONAL TO THE DC INPUT LINE

The NPN and PNP current mirrors provide a charging current to C_r of:

$$i_2 = i_1 = \frac{V_{line} - 0.7V}{R_r} \approx \frac{V_{line}}{R_r}$$

The current mirrors are useful over a current range of $1\mu A$ to $1mA$, but optimum tracking occurs between $30\mu A$ and $300\mu A$. Since the voltage across Q_1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{line}}{R_r C_r}$$

The peak voltage across C_r is clamped to approximately $4.2V$ while the valley, or low voltage, is determined by the on-voltage of the discharge network, D_1 and Q_5 . This is typically $0.7V$.

If line sensing is not required, R_r should be connected to the $5V$ reference for constant ramp slope.

3.3.3 Error Amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The $1k\Omega$ output resistor, R_o , is used both for short circuit protection and to limit the peak output voltage to less than $4.0V$ so it cannot rise above the clamped ramp waveform. At sink currents less than $300\mu A$, the low output level will be within $200mV$ of ground but it rises to $1V$ at higher current levels.

The input common mode range is from $1V$ to within $2V$ of the input supply voltage, V_{in} , and thus either input can be connected directly to the $5V$ reference.

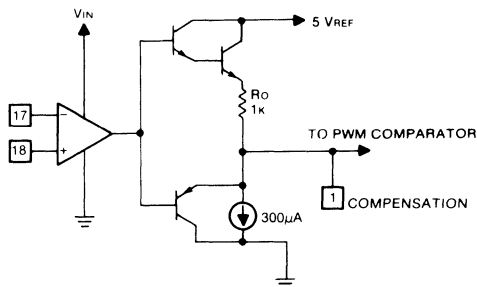


FIGURE 10. THE OUTPUT OF THE ERROR AMPLIFIER OPERATES CLASS A TO $300\mu A$, BUT CAN SOURCE AND SINK MORE THAN $1mA$ FOR FAST RESPONSE

The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under $1V/\mu s$.

3.3.4 PWM Comparator and Latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100% . The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

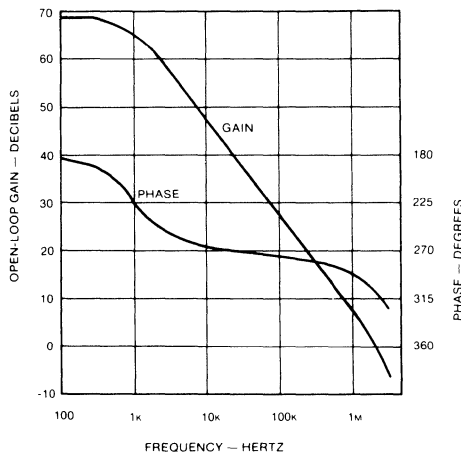


FIGURE 11. THE UC1840 ERROR AMPLIFIER HAS A DC GAIN OF $67db$, A $2MEGAHERTZ$ BANDWIDTH, AND PHASE MARGIN OF APPROXIMATELY 45°

3.3.5 PWM Output Stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages ($V_{in} < 3V$), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between $V_{in} = 3V$ and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying ($V_{in} - 2V$) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4—narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several

different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high-speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

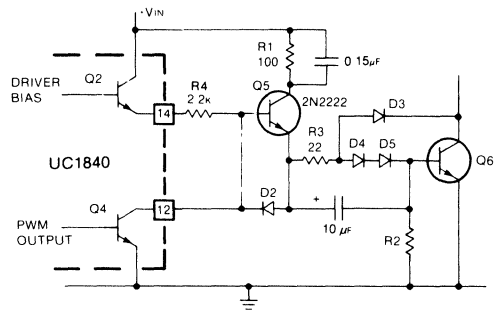


FIGURE 13. ADDING Q5 AS A SWITCHED, DRIVE-BOOST TRANSISTOR PROVIDES ADDED BASE DRIVE FOR Q6 WHILE REDUCING THE STEADY-STATE CURRENT THROUGH BOTH Q2 AND Q4.

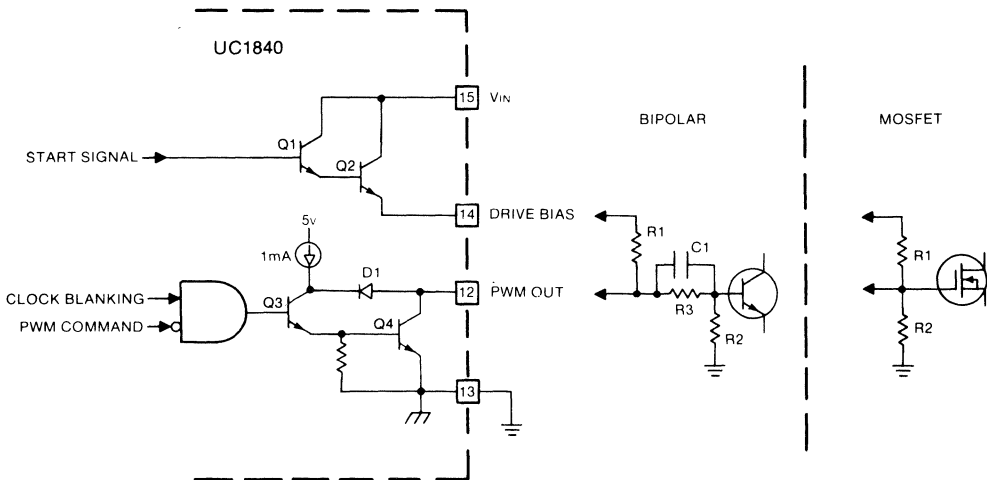


FIGURE 12. INTERFACING THE UC1840 PWM OUTPUT STAGE TO EITHER BIPOLAR OR POWER MOSFET SWITCHES.

Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

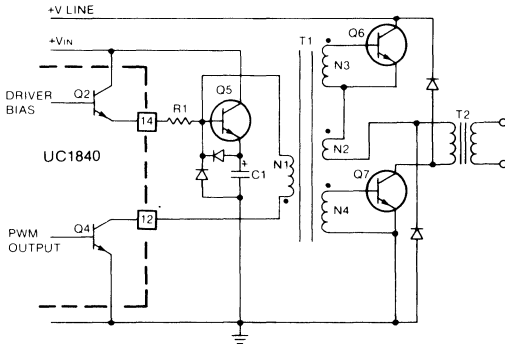


FIGURE 14 INTERFACING THE UC1840 SINGLE PWM OUTPUT TO A TWO-TRANSISTOR OFF-LINE FORWARD CONVERTER WHICH USES PROPORTIONAL BASE DRIVE.

3.4 Fault Protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

3.4.1 Current Limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by Rsc reaches a threshold defined by divider R1, R2, and the 5V reference. Since Vc is intended to track the supply's output voltage, the addition of a resistor from pin 6 to Vc will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset

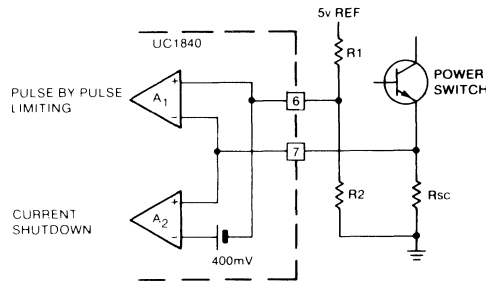


FIGURE 15. CURRENT LIMITING AND OVERCURRENT SHUTDOWN ARE IMPLEMENTED WITH COMPARATORS OF DIFFERENT THRESHOLDS AND A SINGLE CURRENT SENSE RESISTOR.

voltage, it is activated when the voltage across Rsc equals that across R2. Comparator A2, with an offset voltage of 400mV, will activate for over-current shutdown when the voltage across Rsc rises to 400mV higher than the voltage across R2. Since the input bias to both comparators is less than 5 μ A, a low-pass filter for noise rejection may be inserted between Rsc and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

3.4.2 Fault Sequencing

The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

- (1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2
- (2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3
- (3) A voltage of less than 3V on the Ext. Stop terminal, pin 4
- (4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400mV

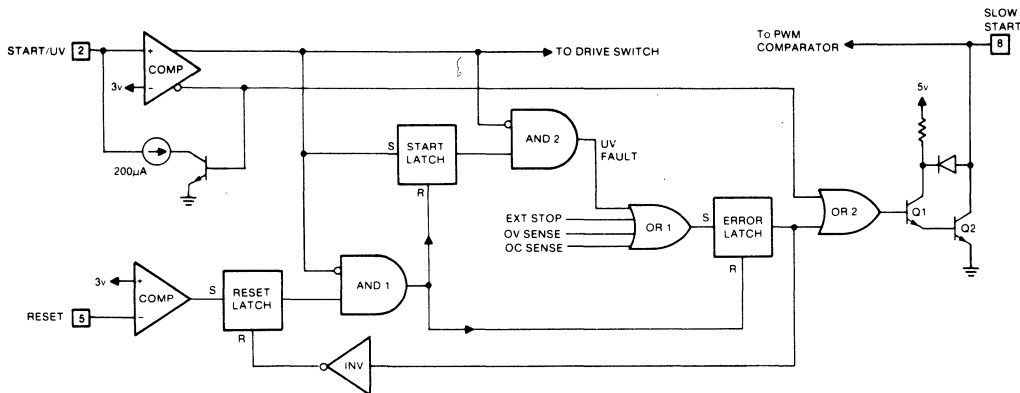


FIGURE 16. FAULT SEQUENCE LOGIC IS DESIGNED TO INSURE A COMPLETE SHUTDOWN AND FULLY CONTROLLED RESTART UPON ANY OF FOUR POSSIBLE FAULT CONDITIONS.

Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than $2\mu\text{A}$ of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are:

- (1) Latch off and require a recycle of input voltage to restart
- (2) Continuously attempt to restart
- (3) Attempt some number of restarts and then latch off
- (4) Latch off and await a momentary reset pulse to restart

To examine the operation of the Reset Latch; note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of

the Error Latch, the Reset Latch is free to take the state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch, re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a con-

start driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

4. Conclusion

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.

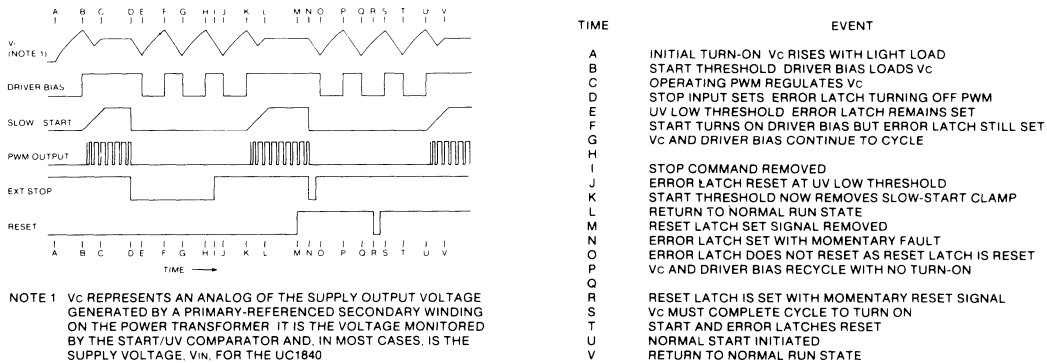


FIGURE 17. THE INTERRELATIONSHIP BETWEEN THE FUNCTIONS CONTROLLED BY THE FAULT SEQUENCE LOGIC IS ILLUSTRATED WITH BOTH STATIC AND PULSE COMMANDS ON THE EXT. STOP AND RESET TERMINALS.

A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977⁽¹⁾ and has seen rapid development by many authors to date.⁽²⁻⁶⁾ In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

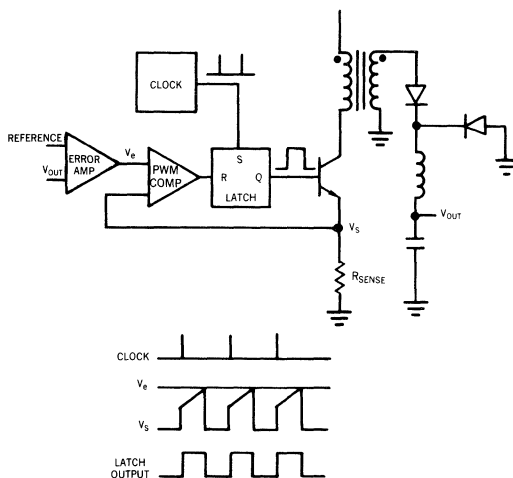


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e , is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e , instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

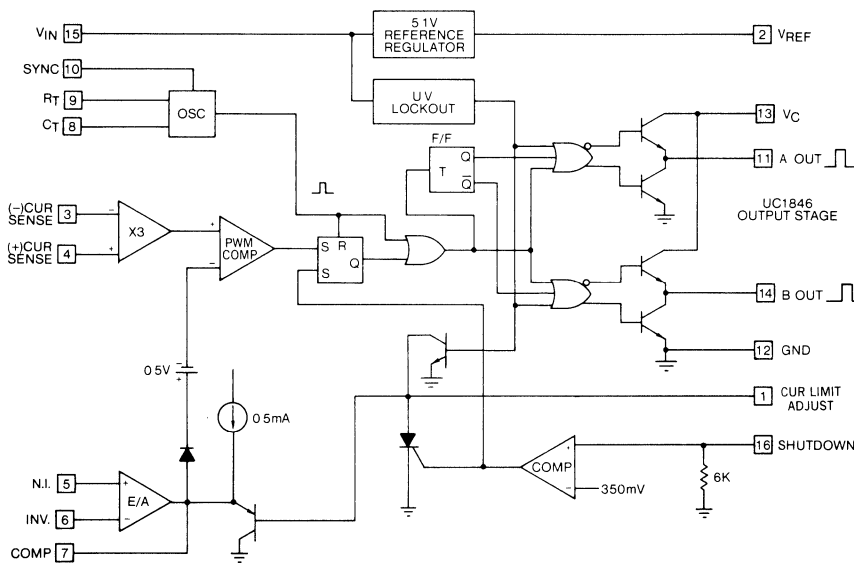


FIGURE 2 UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A $\pm 1\%$, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz.
- An error amplifier with common mode range from ground to $V_{cc}-2V$.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.

- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

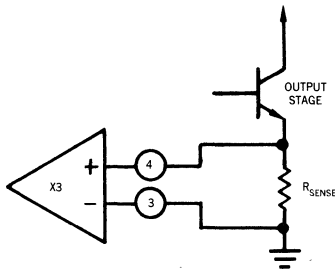
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

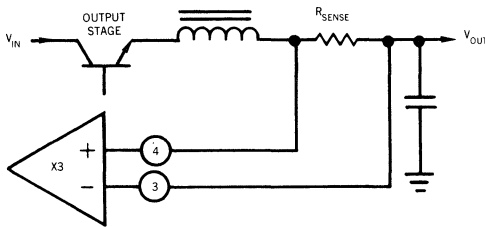
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

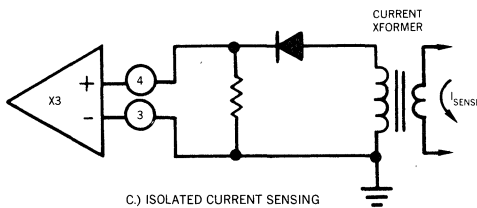
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A) RESISTIVE SENSING WITH GROUND REFERENCE



B) RESISTIVE SENSING ABOVE GROUND



C) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in

series with the input is generally all that is required to reduce the spike to an acceptable level.

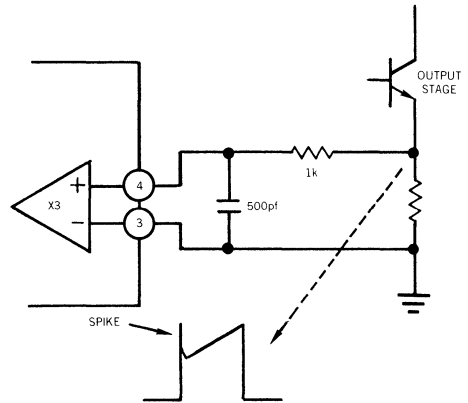


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow ($f_t = 2\text{MHz}$) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1MHz.

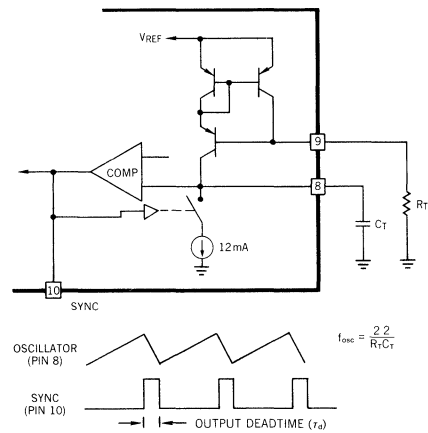


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

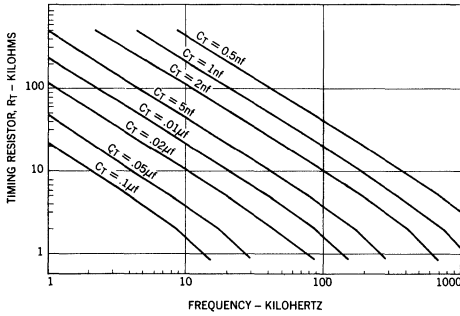


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau_d = 145 C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)} \right] \quad (2)$$

For large values of R_T :

$$\tau_d = 145 C_T \quad (3)$$

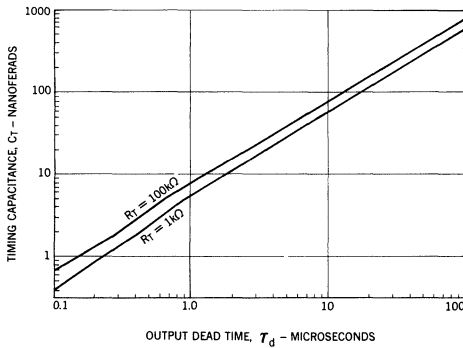


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

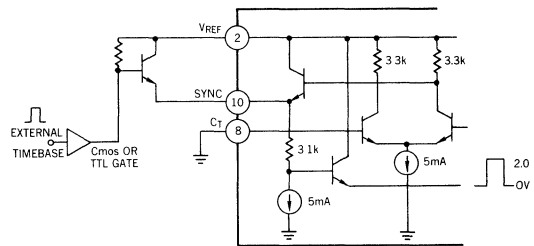


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2 , to set a pre-determined voltage at pin 1.

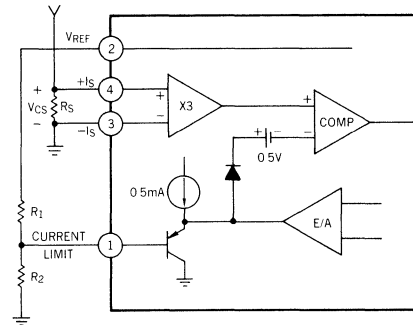


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1 , acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1} - 0.5V$. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{R_2 (V_{REF}) - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

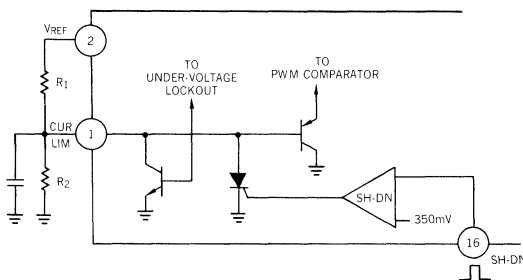


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H , of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5k Ω , Q_1 will discharge any capacitance, C_s , on pin 1 to ground and commutate the output latch, allowing C_s to recharge. If R_1 is chosen less than 2.5k Ω , Q_1 will discharge C_s and remain in the latched state until power is externally cycled off. In either case, C_s is required only if a soft-start or soft-restart function is desired.

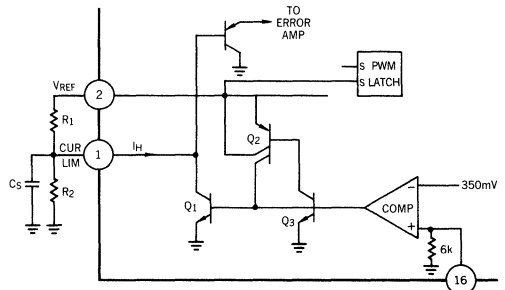


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

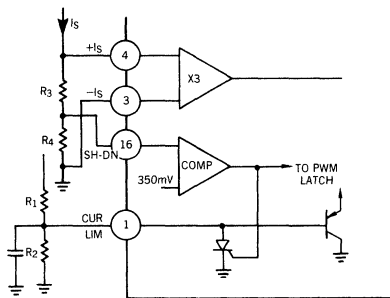


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency⁽⁵⁾. Therefore, a pole-zero combination has been

placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation⁽⁴⁻⁶⁾. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

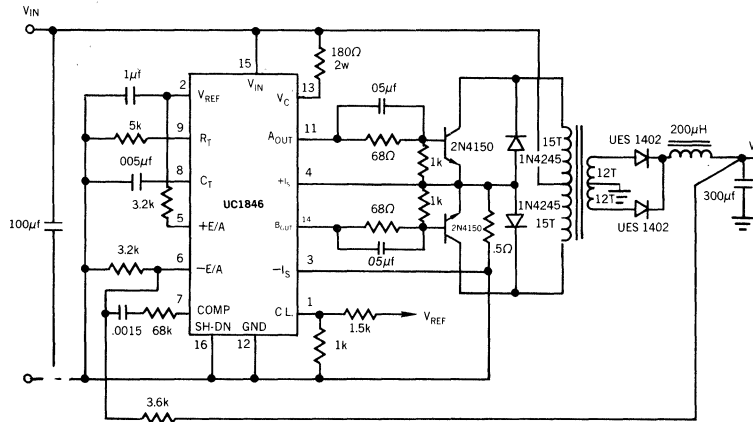
It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF} , -E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

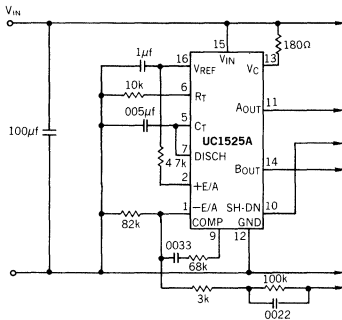
Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A — with identical output

transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

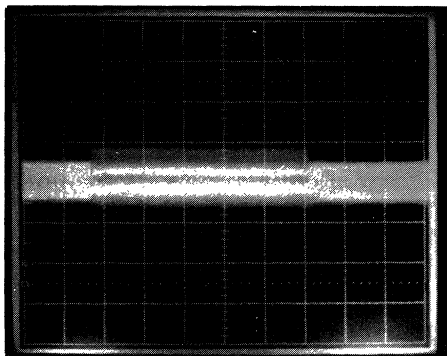


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR

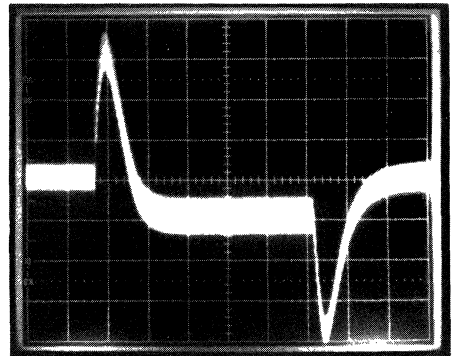


(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A)



(B)

t = 2ms/DIV
 OUTPUT RESPONSE
 50mV/DIV

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 AND (B) UC1525A CONVERTERS

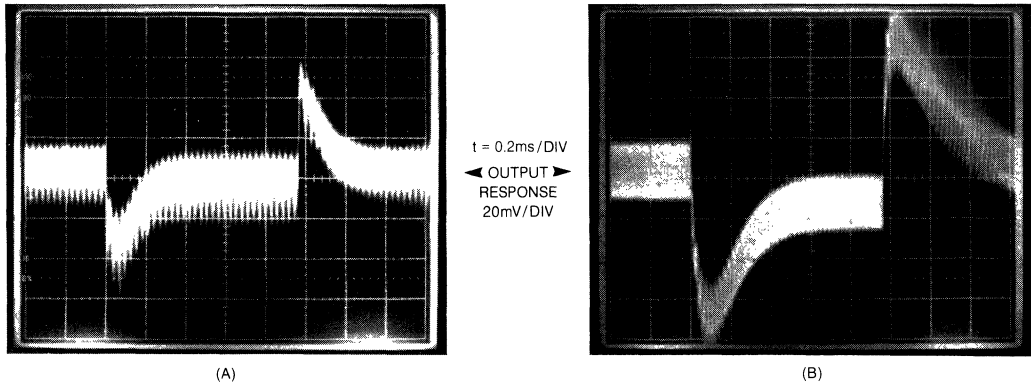


FIGURE 15. RESPONSE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

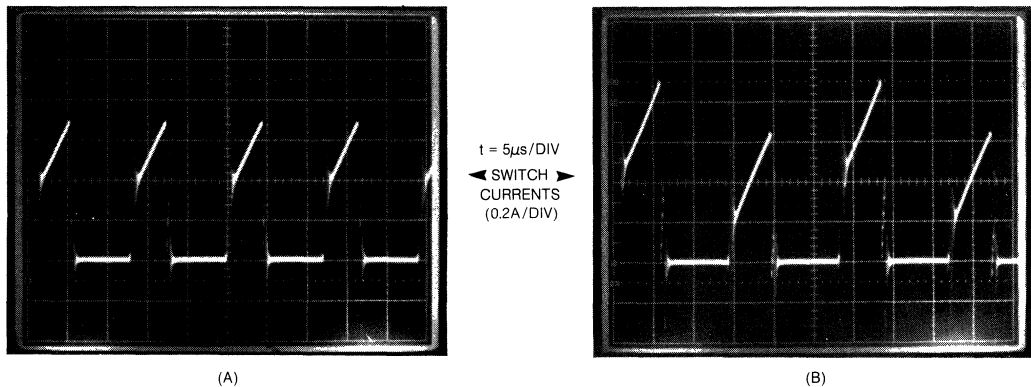


FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular

design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counterparts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worst case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, opto-couplers suffer from poor initial tolerance and sta-

bility. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

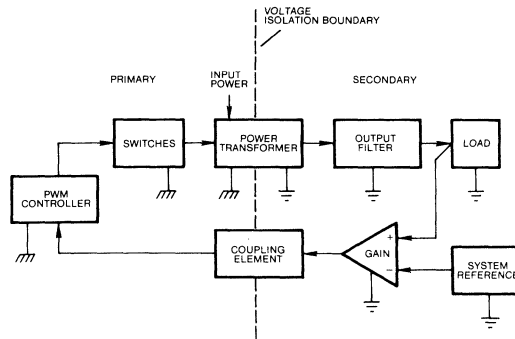


FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best understood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

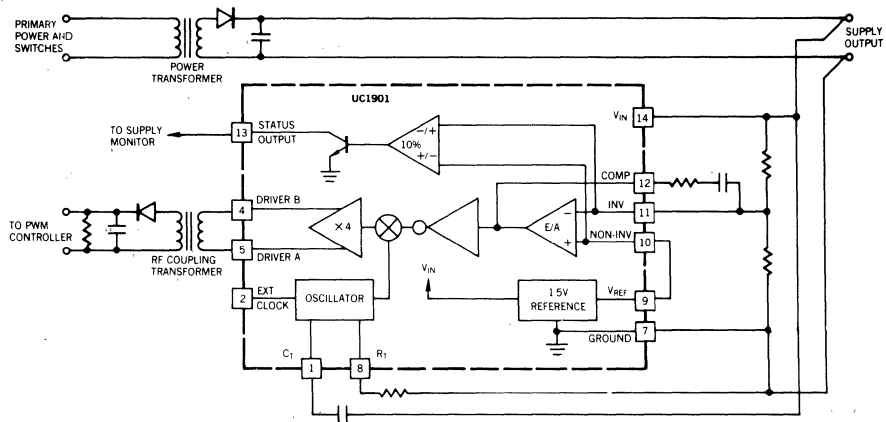


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

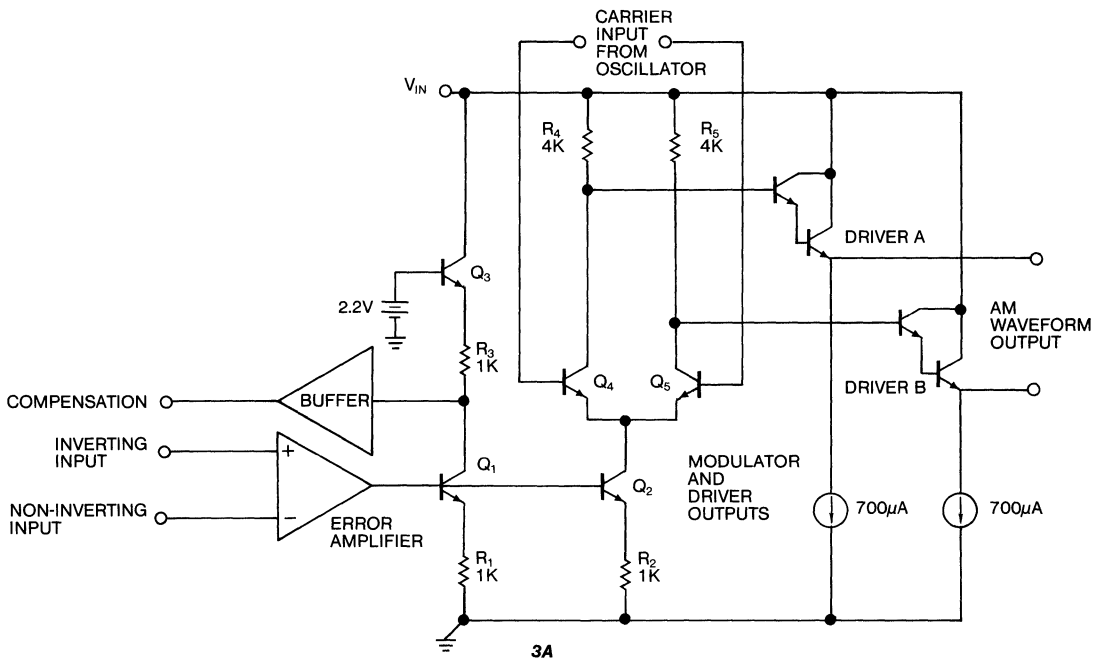


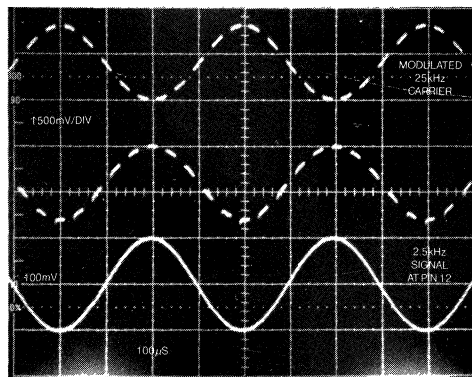
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward convert-



3B

ers are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q₁ and Q₂, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q₁. Since Q₂ sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q₁. The collector current of Q₂ feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R₄ (or R₅) and R₂ results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

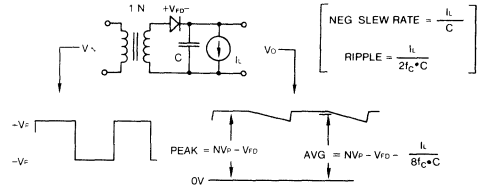


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

$$(1) \quad L_M \geq \frac{V_P}{4f_c I_P}$$

- Where:
- L_M = the magnetizing inductance,
 - V_P = the peak carrier voltage across transformer inputs,
 - f_c = the UC1901 operating frequency,
 - I_P = the bias current of the UC1901 drivers.

As an example, consider the case where V_P is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1 mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

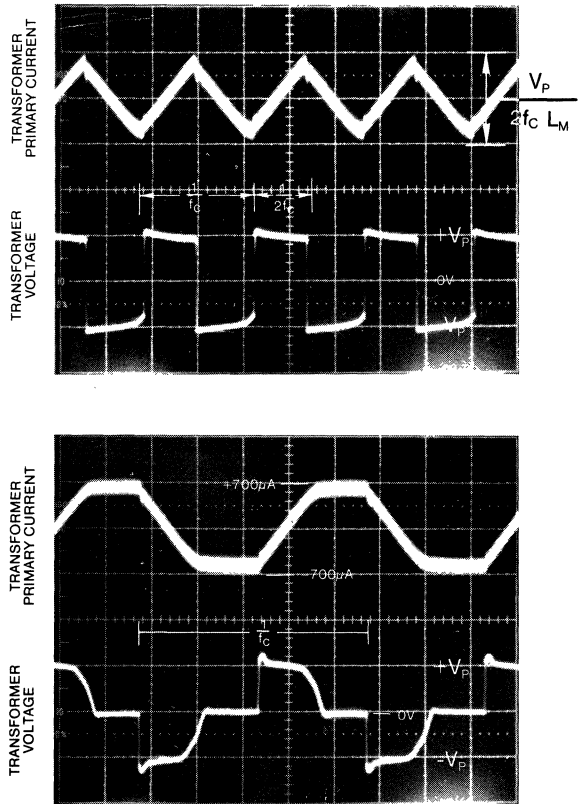


FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P , is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the >50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T , typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T 's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1 - Q_4 , diodes D_1 and D_2 , and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T . The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt .

When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} , and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2 .

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of $10k\Omega$. A desired operating frequency is obtained by choosing the correct value for C_T . As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \quad f_{osc} = \frac{1.24}{R_T C_T}$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

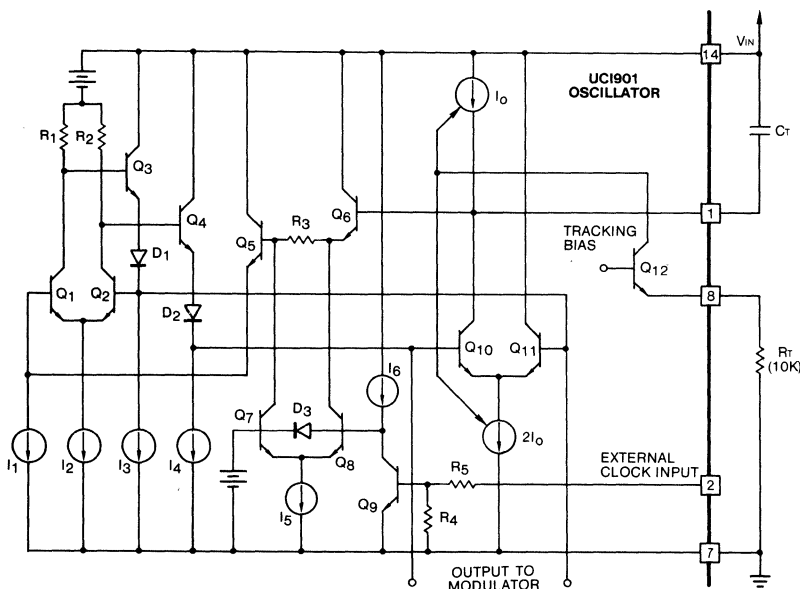


FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

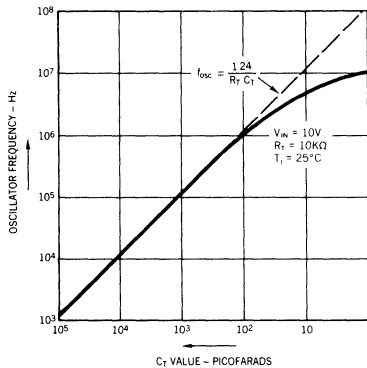


FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-riden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the

latched comparator via the input device Q_9 , and the differential pair Q_7 and Q_8 . As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2 . When the supply output

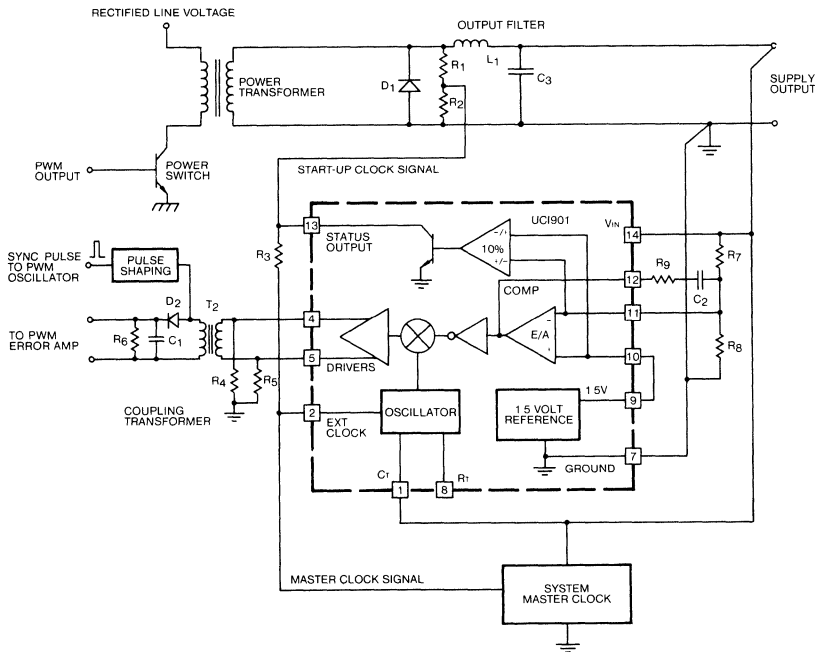


FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

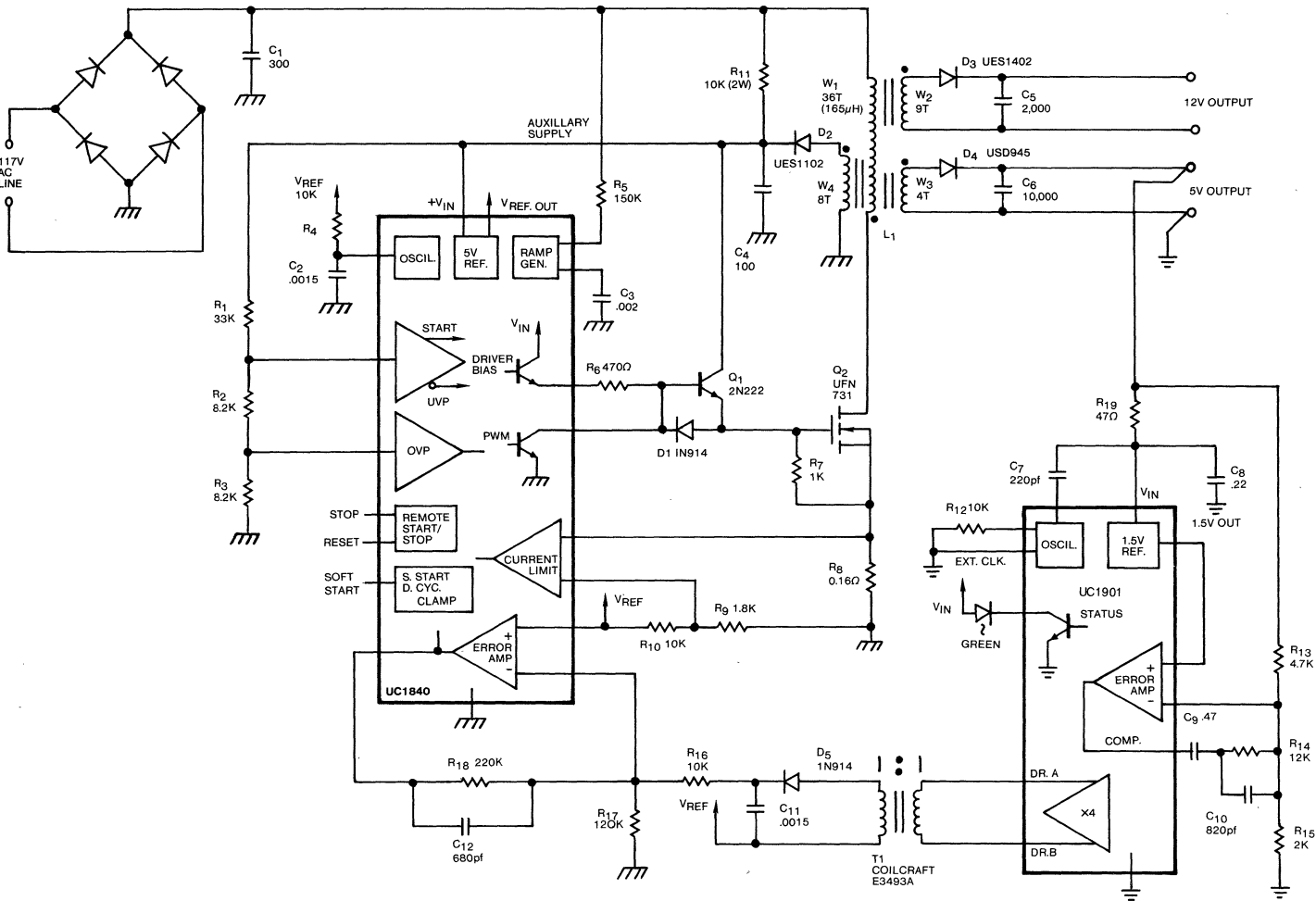


FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (< 150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ± 2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ± 5 percent with ± 6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11} . Once the supply is up and running W_4 , the auxiliary winding on L_1 , provides power to the controller and the switch drive circuitry. The primary

winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT} , to, V_C , the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3) \quad \frac{V_{OUT}}{V_C}(s) = \frac{V_{IN}}{V_R} \sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

- V_{IN} = level of the rectified line voltage,
- V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,
- T_P = One period of the switching frequency,
- L_M = Magnetizing inductance of the primary winding,
- C_F = A total effective output filter capacitor,

- R_L = The total effective load, (assumed resistive),
- R_S = ESR of the filter capacitor,
- s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L , and the input voltage, V_{IN} . This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3 . Scaling the ramp slope is the same as scaling V_{in} , the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \quad V_R = \frac{V_{IN} T_P}{R_5 C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequen-

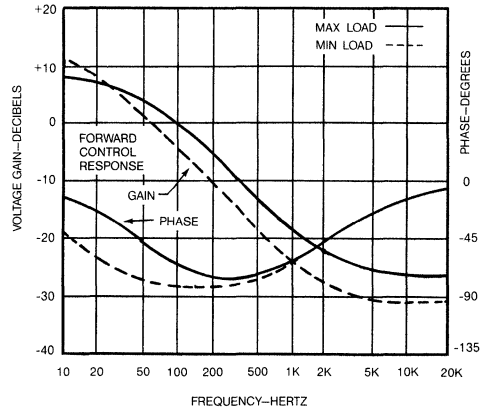


FIGURE 10: Closing the Feedback Loop is Preceded by the Characterization of the Converter's Forward Small Signal Transfer Function.

cy. No mid-band zeros or lead-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedance of the 12V supply will be determined by IR losses, the dynamic impedance of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedance is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilloscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass ($< 15\text{kHz}$) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedance of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the $2000\mu\text{F}$ value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedance. This agrees well with actual measurements of the 12V output's load regulation.

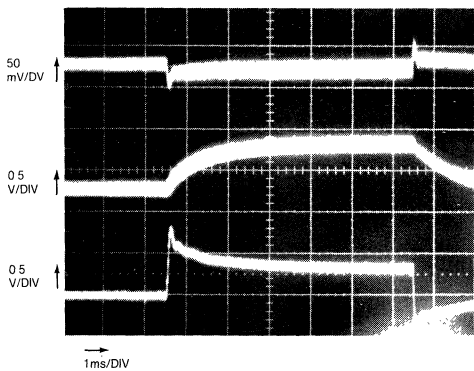


FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only $475\mu\text{A}$ per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is $50\mu\text{A}$, set by the 0.5V operating level and R_{16} . The peak to peak detector ripple, at 500kHz, across the $.0015\mu\text{F}$ holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

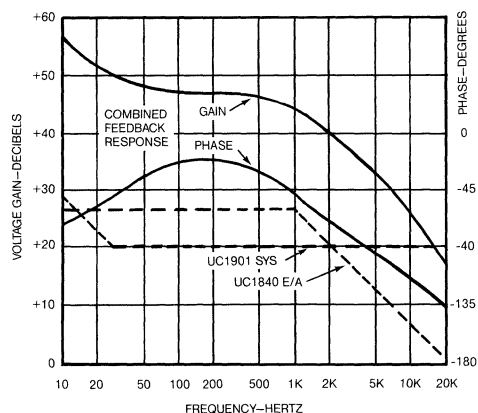


FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. Too much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

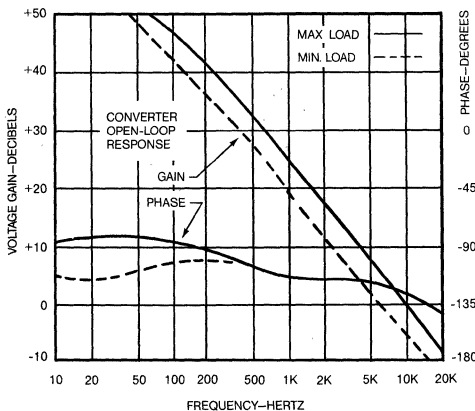


FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of $> 50^\circ$.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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PROPORTIONAL BASE DRIVE OF BIPOLAR POWER TRANSISTORS IN SWITCHING POWER SUPPLIES

Proportional base drive is a simple and effective method of achieving improved performance with high voltage bipolar power switching transistors in off-line applications. As shown in Figure 1, a current transformer provides regenerative base drive current whose amplitude is proportional to the collector current being switched. The drive current ratio is established by the turns ratio of the collector and base windings.

The proportional drive method may be employed with any power switching circuit topology. Advantages over conventional fixed base current drive methods include:

1. Fixed base drive current must be large enough to handle the full load (or short-circuit load) collector current. Under lightly loaded conditions, the switching transistors are severely overdriven, resulting in long storage and fall times and more difficult turn-off. Proportional drive provides optimal performance under varying load current conditions.
2. Proportional base drive requires less drive power from the control circuit. During the "on" time of the switching transistor, base drive is provided regeneratively from the collector circuit through the current transformer. The control drive circuit is not required to provide sustaining base drive current. It must only provide short pulses of drive current to initiate turn-on and turn-off. The amplitude of these drive current pulses can easily be made large enough to obtain good switching performance from high voltage bipolar devices in off-line applications.

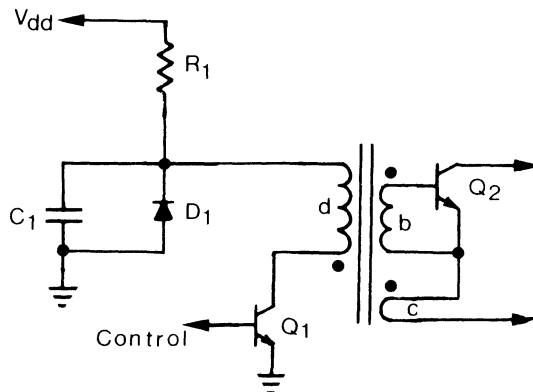


Figure 1. Proportional Base Drive Circuit

Referring to Figures 1 and 2, when driver transistor Q_1 is on, power switch Q_2 is off. Magnetizing current I_{d1} in the control drive winding N_d approaches a steady-state value equal to the drive circuit supply voltage V_{dd} divided by R_1 . Capacitor C_1 is discharged and there is zero voltage across all windings of T_1 .

When the output of the control circuit turns on, driver Q_1 turns off and primary current I_{d1} must cease. Energy stored in T_1 causes the voltage at the dotted ends of all windings to flyback in the positive direction. I_{d1} multiplied by turns ratio N_d/N_b becomes I_{b1} , the turn-on base drive current pulse to Q_2 .

Collector current I_c starting to flow in winding N_c causes a regenerative increase in base drive to Q_2 until it is switched fully on. The final value of I_c induces a proportional base drive current, I_b , according to the turns ratio N_b/N_c .

During the time that Q_2 is on and Q_1 is off, capacitor C_1 charges through R_1 to supply voltage V_{dd} . At the end of this "on" period, driver transistor Q_1 is turned on again, applying the voltage on capacitor C_1 to the drive transformer primary. This drives the voltage on the base of Q_2 sharply negative. The turn-off base current pulse, I_{b2} , can be made larger than Q_2 collector current, resulting in very rapid turn-off of Q_2 .

After Q_2 is off and I_{b2} ceases, any remaining voltage on C_1 across the drive transformer primary helps to rebuild the magnetizing current. Diode D_1 prevents the possibility of any underdamped ringing from driving the upper end of N_d negative. At the end of the "off" period, magnetizing current I_{d1} has been re-established and the cycle repeats.

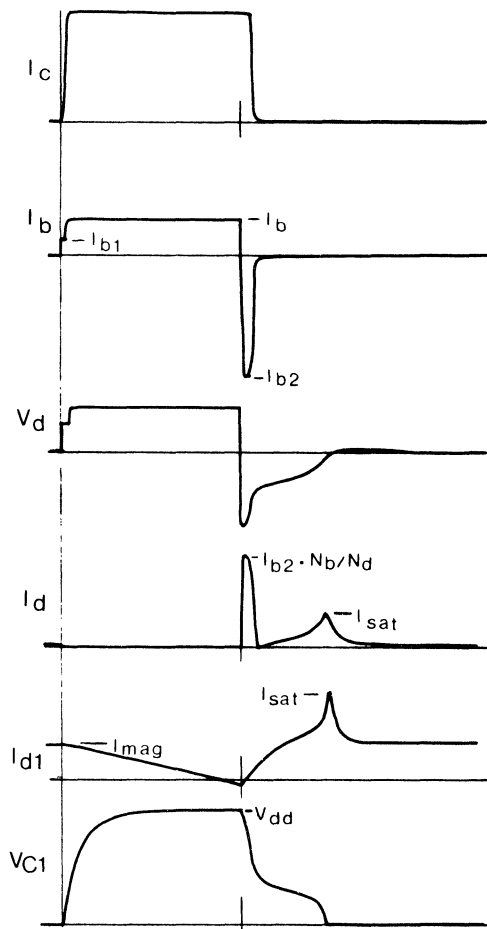


Figure 2. Waveforms

It is quite feasible to operate high voltage bipolar transistors at frequencies above 50 KHz with reasonable efficiency because of the large amplitude base drive pulses obtainable with this method. However, the circuit of Figure 1, as just described, is not capable of operation at frequencies above a few kilohertz. This is because capacitor C must charge to V_{dd} during the "on" period of Q_2 , and the R_1C_1 charging time constant is far too long for this to be accomplished at 50 KHz.

This problem is solved by the addition of a rapid recharge circuit as shown in Figure 3. During the time that Q_2 is on and Q_1 is off, current through R_1 is multiplied by the current gain of Q_3 , which significantly reduces the charging time of C_1 . When Q_1 turns on, C_1 discharges through D_2 . The base-emitter of Q_3 is reverse biased, holding it off during the entire Q_2 "off" time.

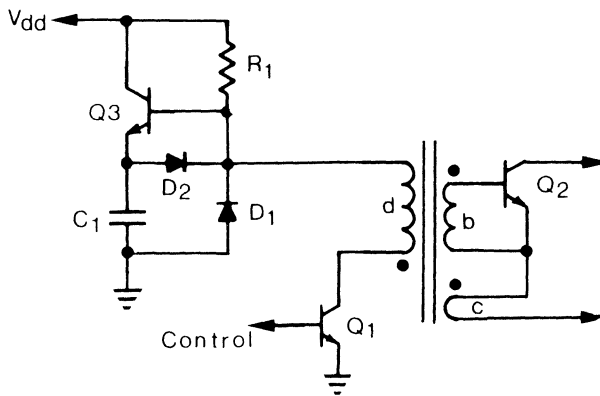


Figure 3. Improved Proportional Base Drive Circuit

DESIGN PROCEDURE:

Application parameter values must be defined, including drive requirements for the power switching transistors:

I_c	Maximum collector current
I_{b1}	Initial turn-on base drive current
I_c/I_b	Sustaining proportional base drive ratio
I_{b2}	Turn-off base drive current at max. I_c
V_{bb2}	Turn-off base drive source voltage at max. I_c
t_2	Maximum transistor turn-off time
V_{dd}	Drive circuit supply voltage
f	Operating frequency

Drive transformer base/collector turns ratio is equal to the desired proportional base drive ratio:

$$N_b/N_c = I_c/I_b \quad (1)$$

Drive transformer driver/base turns ratio is established by the desired turn-off base source voltage and the drive circuit supply voltage, minus 1 volt diode drop:

$$N_d/N_b = (V_{dd}-1)/V_{bb2} \quad (2)$$

When Q_1 turns off, primary magnetizing current, I_{d1} , transferred to the base winding must provide the required turn-on base drive, I_{b1} .

$$I_{d1} = I_{b1}/(N_d/N_b) \quad (3)$$

The R_1 value required to obtain this magnetizing current is:

$$R_1 = V_{dd}/I_{d1} \quad (4)$$

During initial turn-off, driver primary current I_{d2} must absorb the proportional base drive current and transformer magnetizing current I_{d1} in addition to the turn-off base drive current:

$$I_{d2} = \frac{I_{b2} + I_a/(N_b/N_c)}{(N_d/N_b)} + I_{d1} \quad (5)$$

Capacitor C_1 is designed to supply the worst-case energy required to turn off Q_2 :

$$W = \frac{1}{2} C_1 (V_{dd}-1)^2 = (V_{dd}-1) I_{d2} t_2$$

$$C_1 = \frac{2 I_{d2} t_2}{V_{dd}-1} \quad (6)$$

When Q_2 is operated at very low duty cycle (such as immediately after a sudden decrease in load current), C_1 may not have time to fully charge to V_{dd} during the very short "on" time, in spite of the assistance provided by Q_3 . This will probably not be a problem, because Q_2 will also not have time to store much charge and will be much easier to turn off. The time required for Q_2 to reach equilibrium charge storage is comparable to the time required to remove this charge during turn-off. The C_1 charging time constant (reduced according to the gain, H_{fe} , of Q_3) will generally be adequate if it is less than 1/2 the Q_2 turn off time, t_2 .

$$TC_1 = R_1 C_1 / H_{fe} \quad (7)$$

DRIVE TRANSFORMER DESIGN:

Turns ratios for the drive transformer were established in equations (1) and (2). Only certain integral number of turns are permissible for each winding. For example, if N_d/N_c is 25, the permissible number of drive winding turns are 25, 50, 75, etc., corresponding to 1, 2, and 3 collector turns.

Winding I^2R losses are usually negligible. The drive transformer design is based on the following two considerations:

1. Magnetizing current I_{b1} is required for initial turn-on of the power switching transistor. During the time Q_2 is on, the magnetizing current will decrease due to voltage V_{be} across the base winding. The magnetizing current must not be allowed to decrease to less than zero, or it will cause premature turnoff under light load conditions by overcoming the small proportional drive current I_b . Referred to the primary, the drive winding inductance must be large enough to prevent I_{d1} (Equation 3) from reaching zero with voltage $V_{be}(N_d/N_b)$ during the longest possible "on" time (usually half the switching period, $1/2f$):

2. Under light load conditions, relatively little charge is required to turn off Q_2 . C_1 will then have substantial voltage remaining which will be applied to the drive winding during the remainder of the "off" period. This will cause the magnetizing current (and its associated energy storage) to become much larger than desired. The problem is solved by designing the drive winding to saturate at a current level slightly greater than the desired value of magnetizing current, I_{d1} . This will result in dumping any excess energy remaining in C_1 and establishing a consistent starting point on the B-H characteristic at the beginning of each "on" period.

Figure 4 shows the B-H characteristic of the core as seen from the drive winding. For the vertical axis, B times core area A_e and N_d equals $\int V_d dt$ (Faraday's Law). For the horizontal axis, H times effective core length, l , and divided by N_d equals the magnetizing current I_d , (Ampere's Law). The characteristic slope equals the drive winding inductance, L_d , and the area to the left equals the energy stored.

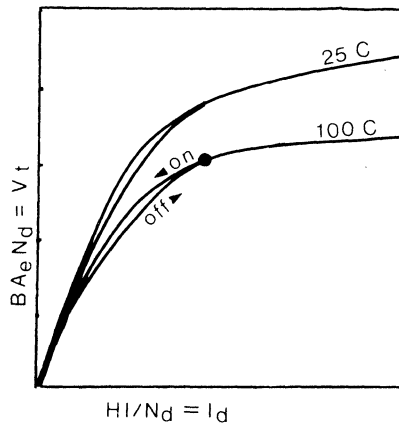


Figure 4.

The operating point shown will satisfy the two requirements above if it exceeds I_{d1} on the horizontal axis and if it exceeds $V_{be}(N_d/N_b)/2f$ on the vertical axis under worst case conditions at high temperature. Procedurally, use Faraday's Law with B close to saturation at high temperature and with the area, A_e , of the core selected. Solve for N_d :

$$\frac{V_{be}(N_d/N_b)}{2f} = B A_e N_d \quad (8)$$

Use the smallest permissible N_d equal to or greater than the value calculated above. An N_d value larger than the calculated amount simply means that the change in flux density will be less than the maximum permitted.

Next, use Ampere's law with a value for H corresponding to the B value chosen before, the smallest permissible N_d from above, and I equal to I_{d1} . Solve for the magnetic path length, l .

$$N_d I_{d1} = H l \quad (9)$$

Compare the actual l_e value for the core selected with the value calculated above. If the actual l_e of the core is significantly larger than the calculated l , it will be necessary to use either a smaller core, or use a larger permissible number of turns, N_d . Otherwise, the operating point will not be close enough to saturation, and the B and H levels will both be too low to prevent the magnetizing current from becoming negative at the end of the "off" period.

If the actual core l_e is smaller than the calculated l , the core will be too heavily saturated, and will not store enough energy to provide the desired I_{b1} . Either go to a larger core, or introduce a small gap, l_g , according to the relationship:

$$l = (l_e + \mu_a l_g), \quad \text{where } \mu_a = B/H \quad (10)$$

Driving Two Transistors. Two power switching transistors are often used in series in order to halve their high voltage V_{ce} rating requirements. It is usually desirable to drive these two transistors from a single drive circuit. This can be accomplished by means of two identical base windings in the transformer. N_b/N_c must be halved and N_d/N_b doubled from the values calculated in Eq. (1) and (2) because the total base current is twice as much as with a single transistor.

As shown in Figure 5, it is also necessary to add a small amount of resistance in series with each base in order to ensure current sharing. A resistor which drops 0.5 volts at maximum sustaining base drive, I_b , should be adequate. The added resistance does not affect the calculation of N_d in Equation (8) because its voltage drop is negligible compared to V_{be} under light load conditions, when the sustaining base drive is small. However, during turn-off, each series base resistor must be shunted by a

small diode. Otherwise, a very large V_{bb2} value would be required in order to pull the desired I_{b2} out of each base. The forward drop of this diode must be added to the V_{bb2} requirement in Equation (2).

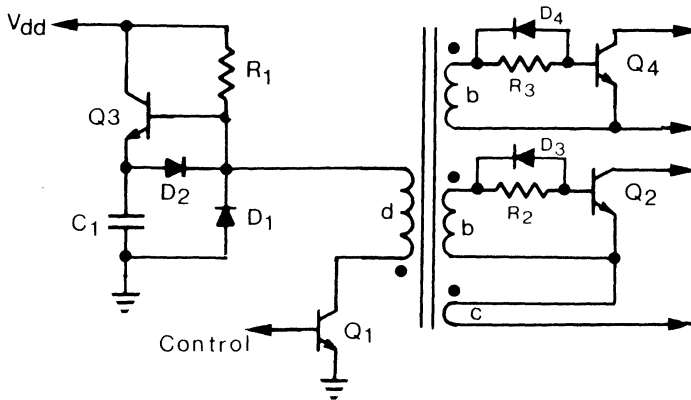


Figure 5. Two-Transistor Driver

Line-side vs Output-side Control Circuit. The base and collector windings of the drive transformer are normally on the input, or line side, of the power supply. When the control/driver circuits are located on the output side of the supply, high voltage insulation is required between the drive winding and the base and collector windings. This high voltage insulation, usually greater than 3000 volts, will impair the coupling between line-side and output-side windings. This results in high leakage inductance, causing voltage spikes during turn-on and turn-off which may necessitate additional snubbing or clamping the drive transistor collector and the power switching transistor base.

When the control and driver circuits are located on the line side, the drive transformer does not require high voltage insulation. Leakage reactance can be made almost negligible, especially if multifilar windings are employed.

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250 WATT OFF-LINE FORWARD CONVERTER DESIGN REVIEW

by

Raoji Patel

This paper gives a practical example of the design of an off-line switching power supply with forward converter topology. Topics include transformer and filter inductor design, proportional base drive, component selection, output filter design, and closing the control loop using the new Unitrode UC1524A control circuit.

POWER SUPPLY SPECIFICATIONS:

TOPOLOGY: Forward Converter with Proportional Base Drive

LINE INPUT: 117 Volts \pm 15% (99-135V), 60Hz
230 Volts \pm 15% (195-265V), 50Hz

OUTPUT: Voltage: 5 Volts
Current: 5 to 50 Amperes
Current Limit: 60 Amperes Short Circuit
Ripple Voltage: 100mV p-p maximum
Line Regulation: \pm 1%
Load Regulation: \pm 1%

OTHER FEATURES: Efficiency: 75%
Line Isolation: 3750 Volts
Switching Frequency: 40KHz

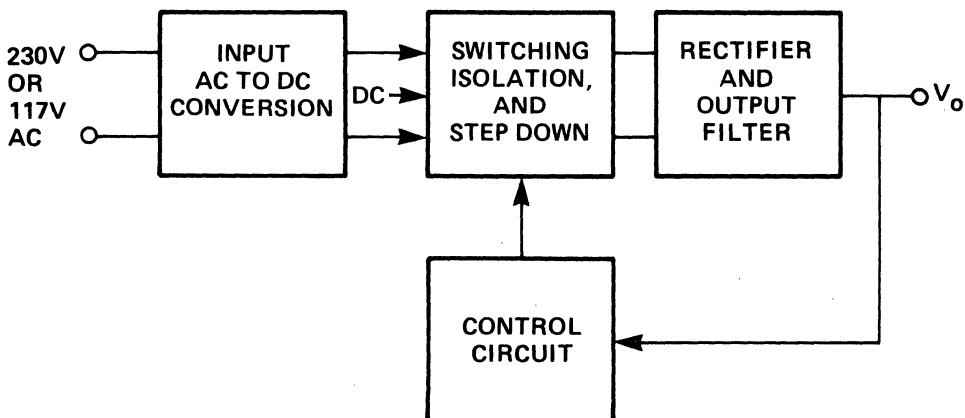


Figure 1. Block Diagram of the Switching Power Supply

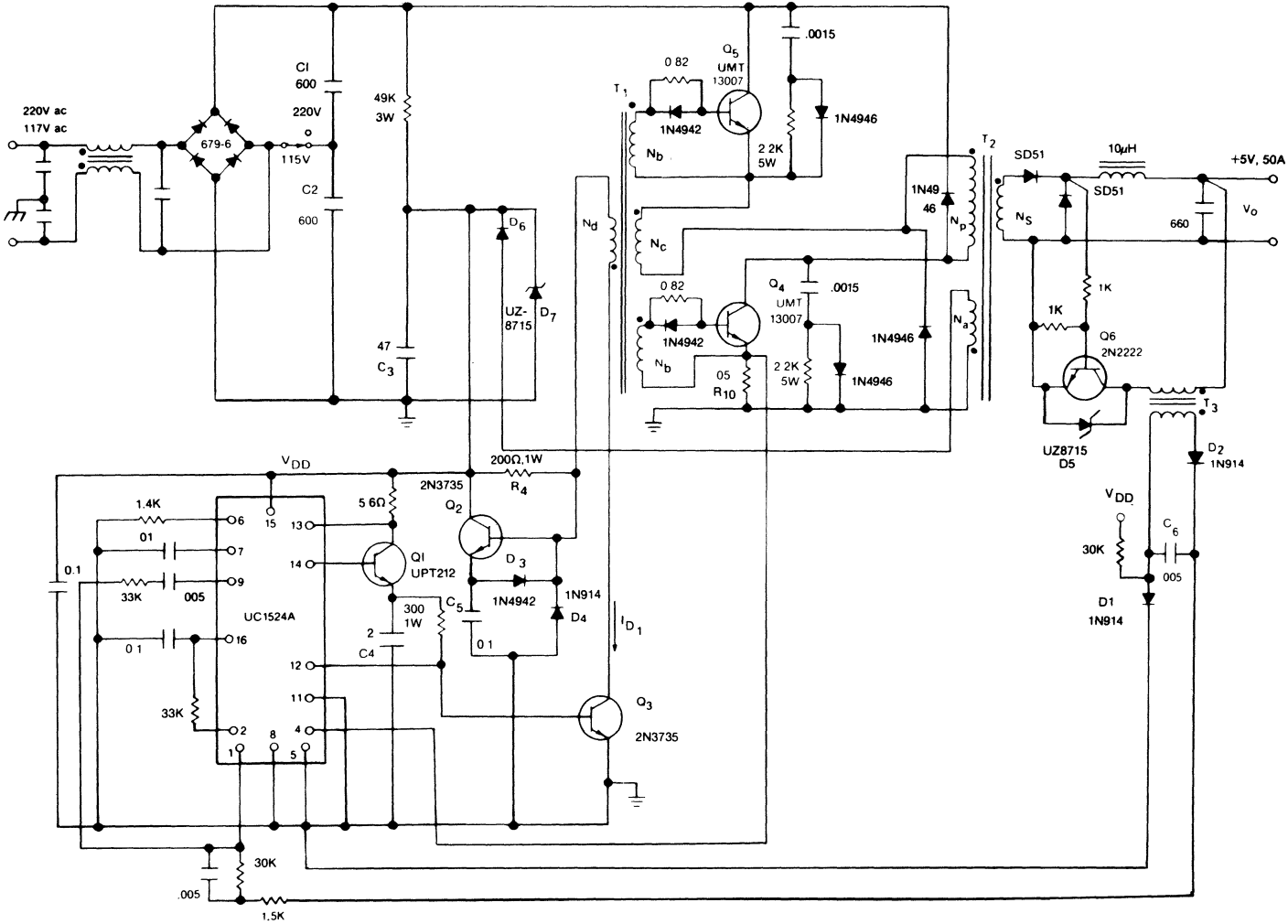


Figure 2. Complete 250 Watt Switching Power Supply

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THE COMPLETE POWER SUPPLY CIRCUIT

The complete 250 watt switching power supply schematic is given in Figure 2. This supply meets all of the specification requirements defined on page 1.

LINE INPUT AC TO DC CONVERSION

The input rectifier/filter section converts the AC line voltage into a crudely filtered and unregulated DC voltage, V_{in} , which powers the downstream switching regulator. The input section is configured as a full-wave bridge when operating from the 230 volt line, and as a voltage doubler when operated from 117 volts. This provides approximately the same V_{in} range (200-380 volts) for the switching regulator with either line voltage. Minimum input voltage, V_{min} , is 200 volts at low line.

The design of the input section is covered extensively in Section I1 of the Design Reference Addenda at the end of this book. The power input required in this application equals power output (250W) divided by efficiency (75%), or 333 watts. Circuit values for this application can be obtained by multiplying the 100 watt input values given in Table I of Section I1 by $P_{in}/100 = 3.33$, using the worst case voltage doubler configuration:

$$C_1 = C_2 = 3.33(160) = 533 \mu F \quad (\text{use } 600 \mu F) \quad (1)$$

$$I_{chg} = 3.33(1.126) = 3.75 \text{ Amps RMS AC} \quad (2)$$

The switching regulator draws 40 KHz rectangular current pulses which discharge the input capacitors. Peak discharge current, i_{dis} , occurs at V_{min} when the duty cycle, D , is maximum (50%):

$$i_{dis} = P_{in}/(V_{min}D) = 333/(200 \cdot .5) = 3.33 \text{ A peak} \quad (3)$$

The RMS AC component of the discharge current, I_{dis} , which flows through the input capacitors at worst case 50% duty cycle is:

$$I_{dis} = (i_{dis})/2 = 3.33/2 = 1.67 \text{ Amps RMS AC} \quad (4)$$

The total RMS AC current rating required for the input capacitors is calculated from Equation 8 of Section I1:

$$I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} = \sqrt{3.75^2 + 1.67^2} \quad (5)$$

SWITCHING CIRCUIT TOPOLOGY

The two transistor forward converter configuration shown in Figure 3 was used in this 250 watt switching power supply for the following reasons:

1. Transistor voltage ratings are half the voltage required in a comparable single transistor circuit (400V vs. 800V). Only 1/4 the silicon chip area is required for the same current rating, and the switching speeds will be twice as fast.
2. The snubber networks are for load line shaping only and are not required to absorb all the energy stored in the transformer leakage reactance. Instead, clamp diodes D_5 and D_6 conserve most of this energy by returning it to the input, improving the efficiency.
3. Closed-loop stability is easier to achieve than with a flyback converter because there is no right half plane zero.
4. Filter capacitor requirements are much less severe than in boost or flyback converters because of the output filter inductor.
5. Transformer construction is simplified because there is no need for a clamp winding (N_a is used for the auxiliary supply).
6. Reliability is improved because faster transistors result in reduced switching losses, and each transistor dissipates only one half of these reduced losses.

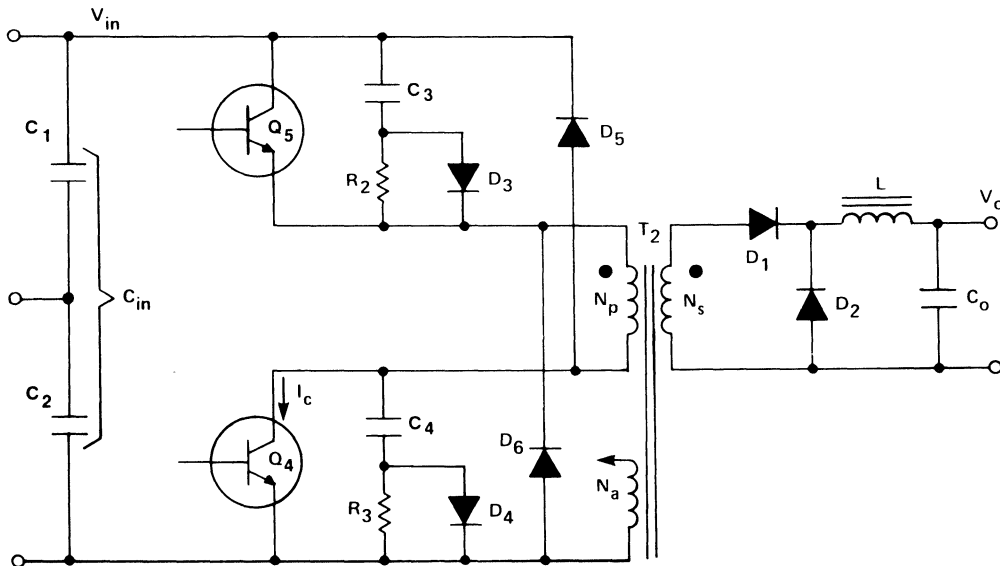


Figure 3. Two Transistor Forward Converter

Disadvantages of this topology are:

1. Two transistors are required instead of one (but cost may be less).
2. Restricted to less than 50% duty cycle to permit core reset. This results in poorer transformer utilization.
3. Added cost of filter inductor, which is not required for the flyback converter.

SPECIFYING THE SWITCHING TRANSISTORS

Maximum peak primary current flowing through the transistors, I_{CM} , is the same as i_{dis} from Equation 3, or 3.33 A.

The transistors should have good $V_{CE(sat)}$ and switching speeds at a collector current of at least 4.0 amperes, which includes an allowance for unusual conditions such as short circuit current. (Disregard spec sheet "maximum current ratings" which are inflated for competitive marketing reasons, and focus on the specified test conditions.)

The collector voltage rating must be greater than maximum V_{in} , or 380 volts in this application. Conservatively, this should be the BV_{CEO} rating, but with careful load line shaping to make certain the transistor is completely off before voltage is applied, a less conservative designer might specify BV_{CEX} greater than $V_{in(max)}$.

The UMT13007 satisfies the above requirements, with BV_{CEO} of 400V, $V_{CE(sat)}$ less than 2.0V at 5A, and worst case fall time of 400ns under the proportional base drive conditions provided.

SNUBBER NETWORK DESIGN

The turn-off snubber networks shown across each transistor in Figure 3 provide shaping of the load line to ensure that it remains below the reverse bias safe operating area (RBSOA) of the transistors. Capacitors C_3 and C_4 accomplish this by holding the voltage across each transistor low during current turn-off. The snubber capacitors thus absorb the turn-off transition energy that otherwise would have been dissipated in the transistors (see Figure 4).

$$C_3 = C_4 = \frac{I_{CM} t_f}{2 V_{in(max)}} \quad (6)$$

$$= \frac{3.33 \times .4 \times 10^{-6}}{2 \times 380} = .00175 \mu F \quad (\text{use } .0015 \mu F)$$

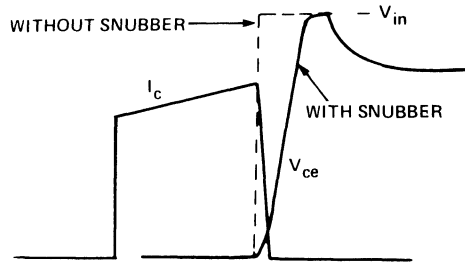


Figure 4. Effect of Snubber Network on Turn-Off Characteristic

Resistors R_2 and R_3 are designed to discharge the snubber capacitors with a discharge time constant of one-half the minimum on time, $t_{on(min)}$.

$$t_{on(min)} = \frac{D(max) V_{in(min)}}{f V_{in(max)}} = \frac{0.5}{40,000} \frac{200}{380} = 6.58 \mu s \quad (7)$$

$$R_2 = R_3 = \frac{t_{on(min)}}{2C_3} = \frac{6.58 \times 10^{-6}}{2 \times 1.5 \times 10^{-9}} = 2.2K$$

Maximum power dissipation in each resistor:

$$\begin{aligned} PR_2 = PR_3 &= \frac{1}{2} C_2 V_{in(max)}^2 f \\ &= \frac{1.5 \times 10^{-9}}{2} \times 380^2 \times 40,000 = 4.3 \text{ watts} \end{aligned} \quad (8)$$

POWER TRANSFORMER DESIGN

The design of the 40KHz inverter transformer is detailed in Appendix A. A primary to secondary turns ratio of 148/9, or 15.33, ensures that 5 volts output is provided with minimum V_{in} of 200 volts at 50% duty cycle, including voltage drops in rectifiers, transistors and windings.

Transformer winding N_B is used to provide an auxiliary supply to power the control and base drive circuits. This makes good use of the energy stored in the transformer primary inductance.

15

OUTPUT FILTER DESIGN

The output filter and its associated waveforms are shown in Figure 5. The filter inductor calculation is based on the maximum "off" time:

$$D(min) = D(max) \frac{V_{in(min)}}{V_{in(max)}} = 0.5 \frac{200}{380} = .263 \quad (9)$$

$$t_{off(max)} = \frac{1-D(min)}{f} = \frac{1-.263}{40,000} = 18.4 \mu s \quad (10)$$

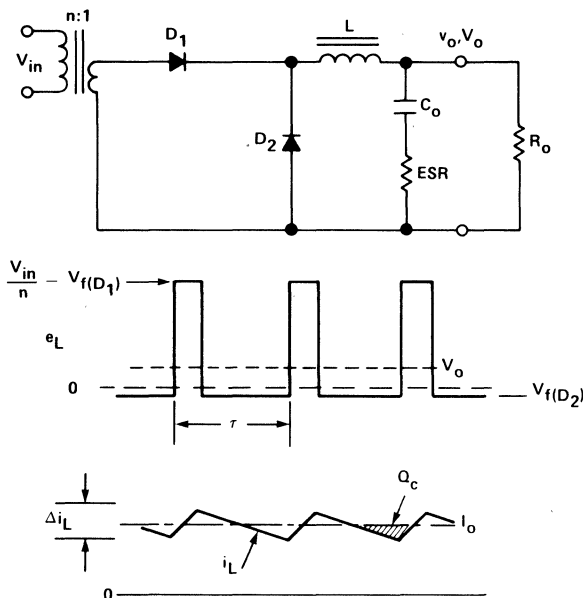


Figure 5. Output Power Filter Design

The inductance required to prevent discontinuous mode operation depends upon the minimum load current:

$$\Delta I_L(\max) = 2I_o(\min) = 2 \times 5 = 10A \quad (11)$$

$$L = \frac{(V_o + V_f)t_{off}(\max)}{\Delta I_L(\max)} = \frac{(5 + 0.6)18.35}{10} = 10 \mu H \quad (12)$$

The capacitance required to achieve the output ripple voltage specification of 0.1 volts is:

$$C_o = \frac{1}{2} \frac{\Delta I_L(\max)}{2} \frac{1}{2f} \frac{1}{v_o} = \frac{10}{8 \times 40,000 \times 0.1} = 312 \mu F \quad (13)$$

The maximum ESR of the capacitor is:

$$ESR = v_o / \Delta I_L(\max) = 0.1 / 10 = .01 \Omega \quad (14)$$

To obtain the necessary ESR requires a capacitor much larger than the 312 microfarads calculated. This design will use three 220 microfarad solid tantalum capacitors, Mallory THF227M010P1G, in parallel. A single 14,000 microfarad aluminum electrolytic capacitor, Mallory CG0143M10R2C3PL could also be used.

With the tantalum capacitor, the resonant frequency of the filter is 2KHz. With the aluminum electrolytic, the resonant frequency is reduced to 425Hz, changing the closed-loop design.

CLOSING THE CONTROL LOOP

The Unitorde UC1524A is used for the control circuit. It has additional features such as pulse by pulse current limiting and high current and voltage output capability (200mA, 60V) compared with the SG1524. The UC1524A reference is trimmed to +/- 1% which makes it possible to avoid using a voltage-setting potentiometer in many instances.

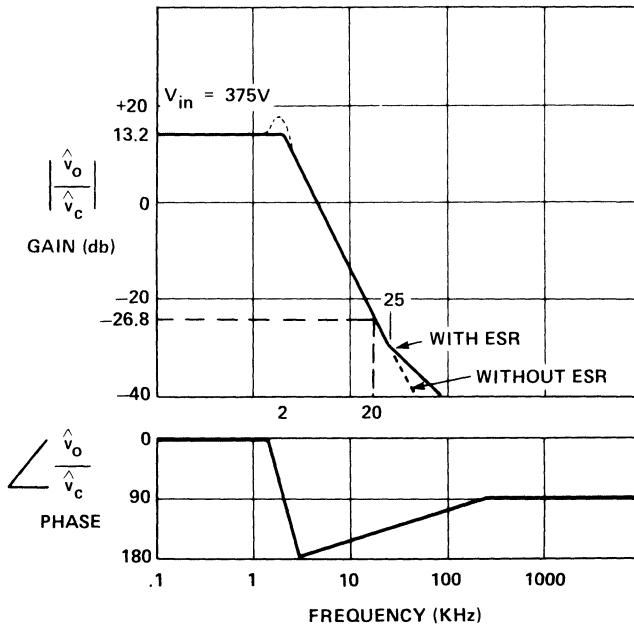
The control to output transfer function, dV_o/dV_c , shown in Figure 6, includes the cascaded gain of the sawtooth modulator within the UC1524A control IC, the power switching circuit, and the output filter characteristic, $H_e(s)$.

In the control IC, a control voltage V_c is compared with sawtooth ramp voltage V_s (2.5 volts) to establish the drive pulse width to the power switches. For the forward converter, only one of the two alternating outputs of the UC1524A is used so as to limit the duty cycle to 50% maximum and allow for transformer core reset:

$$D = 0.5V_c/V_s = 0.5V_c/2.5 = V_c/5 \tag{15}$$

The forward converter is a member of the buck regulator family. Transformer turns ratio $n = 16.44$:

$$V_o = \frac{V_{in} D}{n} = \frac{V_{in} V_c}{n 2V_s} \tag{16}$$



**Figure 6. Control to Output Transfer Function
LC Filter and Modulator**

The low frequency control to output transfer characteristic is obtained by differentiating with respect to V_c :

$$\frac{\partial V_o}{\partial V_c} = \frac{V_{in}}{n \cdot 2V_s} = \frac{380}{15.33 \times 5} = 4.95 = 13.2 \text{ db} \quad (17)$$

Note that gain is greatest at maximum V_{in} . The overall control to output transfer characteristic including the filter is:

$$\frac{\partial V_o}{\partial V_c} = \frac{V_{in}}{n \cdot 2V_s} H_e(s) \quad (18)$$

The filter introduces a two-pole characteristic at its resonant frequency (2 KHz). Above resonance, the gain drops 40db per decade, and the phase shift becomes -180 degrees. Combined with the -180 degree phase shift of the feedback network, this will cause instability and oscillations unless compensated.

Closing the loop involves feeding back the error voltage from the output terminal of the supply (\hat{V}_o) to the IC control voltage port (\hat{V}_c) through the UC1524A error amplifier. The approach taken is to make the gain of the feedback network such that the overall loop gain crosses zero db (with adequate phase margin) at one half the switching frequency.

As shown in Figure 6, control to output gain is 13.2db at low frequencies, rolling off above 2KHz at -40db per decade, so that at 20 KHz the control to output gain is 13.2 - 40, or -26.8db. For overall loop gain of zero, the feedback network gain must be made +26.8 db at 20 KHz.

From 20KHz down to 2Kz, there is a net single zero in the feedback network which cancels one of the two filter poles and reduces the phase shift in this region to -270 degrees.

Below the filter resonant frequency the two filter poles are gone. However, the resonant frequency may be less than 2KHz because of plus tolerances on the filter capacitor. The feedback network is therefore designed to transition from a net single zero to a single pole at 1KHz, half the resonant frequency.

Figure 7 shows the gain and phase plot of the error amplifier and the overall feedback loop. Figure 8 shows the specific feedback network used to achieve this result.

The high frequency error amplifier gain is set by R_2 and R_3 . An R_3 value of 33K is chosen to minimize amplifier loading:

$$A_{v1} = R_3/R_2 = 26.8\text{db} = 21.9 \quad (19)$$

$$R_2 = R_3/A_{v1} = 33000/21.9 = 1500 \Omega$$

The required error amplifier gain at 1KHz is:

$$A_{v2} = A_{v1} \times 1\text{KHz}/20\text{KHz} = 21.9 \times 1/20 = 1.095 \text{ (0.8db)} \quad (20)$$

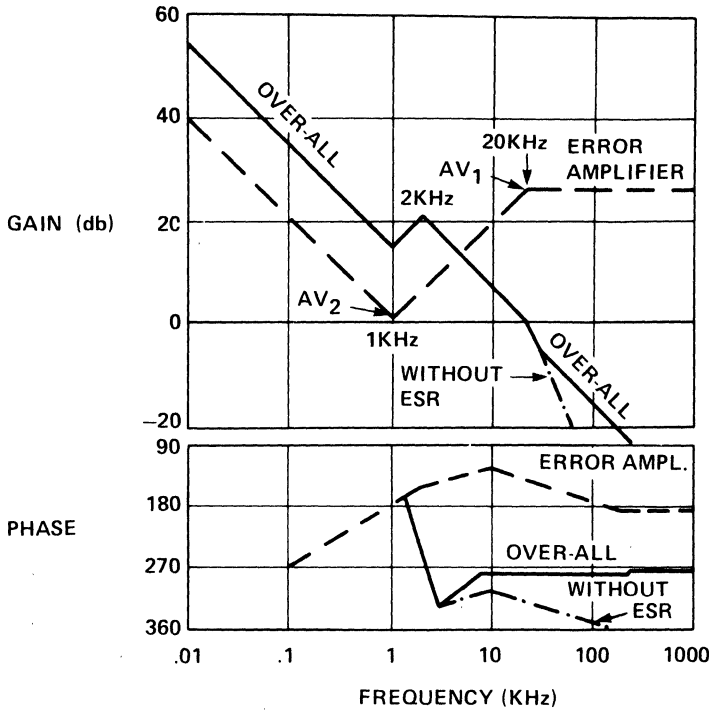


Figure 7. Open Loop Gain and Phase Plot

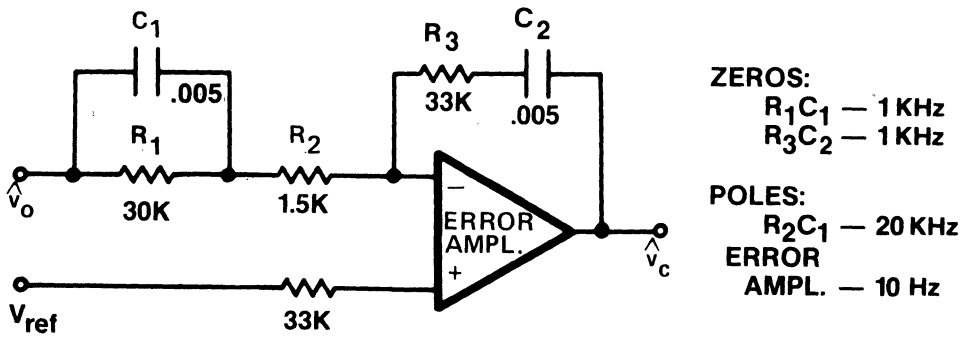


Figure 8. Error Amplifier with Compensation

The gain at 1KHz is determined by R_1 , R_2 and R_3 :

$$A_{v2} = R_3 / (R_1 + R_2) = 33K / (R_1 + 1500) = 1.095 \quad (21)$$

$$R_1 = 28.6K \quad (\text{use } 30K)$$

The two zeros at 1 KHz which changes the feedback network from a net single zero to single pole are equal to:

$$f_1 = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_3 C_2} = 1 \text{ KHz} \quad (22)$$

$$C_1 = .0053 \mu\text{F}, \quad C_2 = .0048 \mu\text{F}$$

C_1 and R_1 in parallel with R_2 result in an additional pole at 20KHz. This flattens the error amplifier gain above 20 KHz. The overall phase shift will gradually increase toward 360 degrees, but it doesn't matter because the overall gain is less than one.

An additional pole occurs below 10 Hz. This is the inherent single-pole characteristic of the error amplifier's 5 megohm output impedance loaded by feedback capacitor C_2 .

PROPORTIONAL BASE DRIVE

In Figure 2, transistors Q_2 and Q_3 and base drive transformer T_1 provide proportional drive to the bases of power switching transistors Q_4 and Q_5 . The proportional base drive technique provides excellent performance from high voltage bipolar transistors. It provides large base current pulses for fast turn-on and turn-off, but with modest drive power requirements. Sustaining base drive is provided regeneratively from a collector current winding on the drive transformer. The transistors are never overdriven, even under light load conditions, since the sustaining base drive is proportional to the collector current. Design considerations for the proportional base drive technique are given in Section D1 in the design section at the back of this book.

Referring to the circuit of Figure 2, when Q_3 is on, R_4 establishes 75 mA magnetizing current in drive winding N_d of T_1 . When Q_3 turns off, the energy stored in T_1 drives 150 mA into the base of each transistor. Collector current starting to flow in N_c provides sustaining base drive. With I_c of 3.33 A under full load conditions, an additional 667 mA of drive is provided to each base.

While Q_3 is off, capacitor C_5 charges through Q_2 in less than 1 microsecond. Then, when Q_3 turns back on, C_5 provides a negative base drive pulse of -1.5 A to each transistor, achieving turn-off in less than 1 microsecond.

Drive transformer T_1 has a drive winding inductance of 0.7 mH and is designed to saturate at 75 mA. High voltage insulation is not required because all windings are on the line side of the supply.

Core: Ferroxcube 1107P-L00-3B7 Pot Core
 N_d : 20 turns AWG34
 N_b : 5 turns AWG28x2 (2 wires, one for each base)
 N_c : 2 turns 5xAWG28 (5 wires paralleled)

AUXILIARY POWER SUPPLY

A 15 volt auxiliary supply powers the control and driver circuits, obtaining its energy from capacitor C₃. Flyback energy is normally provided by T₂ through winding N_a and D₆ to maintain the charge on C₃ every switching cycle. However, at initial power-up it is necessary to provide separate means to activate the V_{DD} supply. Otherwise, the control and driver circuits could not become functional and the supply could not start to switch.

The unique under-voltage lockout feature of the UC1524A facilitates this technique. All of its internal circuits are disabled (except the reference) until the V_{DD} voltage reaches 8 volts. This holds the standby current to less than 4mA until the 8 volt threshold is reached, and permits C₃ to be initially charged through R₁ from the unregulated input. Enough energy is stored in C₃ to operate the control/drive circuits for several switching cycles, until flyback energy from winding N_a can take over and maintain the voltage on C₃.

It is also necessary to eliminate base drive to Q₃ during initial power-up, otherwise Q₃ will draw current through R₄ which will prevent C₃ from initially charging. This is accomplished by transistor Q₁ which disconnects base drive source capacitor C₄. When the UC1524A becomes active, its second output turns Q₁ on periodically to charge C₄.

The amount of energy stored in the power transformer is twice the drive/control circuit requirements. Excess energy is dumped into 15 volt zener diode D₇ which establishes the V_{DD} supply voltage at that level. This also provides a constant clamp voltage across the switching transistors, regardless of line voltage. With good coupling between N_a and primary winding N_p, it may be possible to eliminate clamp diodes D₁₂ and D₁₃.

OUTPUT VOLTAGE SENSE AND OVERCURRENT SENSE

A small, inexpensive transformer, T₃, couples the output voltage to the line side control circuit with high voltage isolation. The transformer is wound on a Ferroxcube 204-T250-3E2A ferrite toroidal core. Primary and secondary windings are both 14 turns AWG32.

During the time the power switching transistors are on, Q₆ is on, applying V_O to the primary of T₃. Through D₂, this provides a real-time feedback voltage to the control circuit across C₆. When Q₆ is off, D₅ clamps the flyback voltage to 15 volts. Core reset is accomplished well before the end of the "off" time, since the "off" time of the forward converter is always more than 50%. All transformer windings then go to zero volts, establishing a DC coupling level. D₁ in series with the ground return compensates for the forward voltage drop and temperature coefficient of D₂.

Pulse by pulse current limiting is set by sense resistor R10. Primary current is limited to 4A, corresponding to 62A load current.

Transient response of the switching supply is shown in Figure 9 with changes in load from 20A to 60A and back to 20A. This behavior is a large signal phenomenon. It doesn't matter how fast the control loop is, it is temporarily driven into the bounds because the load change is much larger than the output filter inductor current can accommodate in one cycle. Nevertheless, recovery is smooth and there is no evidence of ringing or oscillations, demonstrating the stability of the control loop. Step changes in load current that are small enough for the control loop to remain functional are barely noticeable at the output.

Transient response can be improved by reducing the filter inductor and increasing the filter capacitor size, but this will increase the minimum load current required to keep the inductor current from becoming discontinuous.

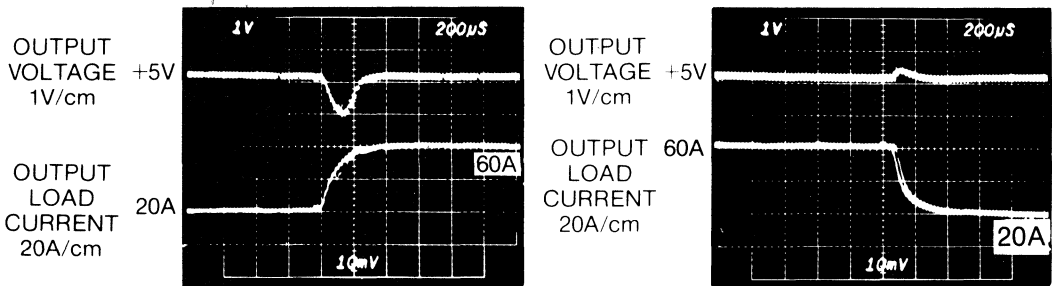


Figure 9. Step Change in Output Load

APPENDIX A DESIGN OF THE POWER TRANSFORMER AND FILTER INDUCTOR

The design procedure used herein is defined in Design Reference Section M5. Symbols, definitions and various core and wire data are given in Reference Sections M1, M2, and M3. Equation references are to Section M5.

Flux Density Excursion

In this forward converter application, the flux excursion is entirely within the first quadrant of the B-H characteristic, from zero flux density toward saturation. With simple duty cycle control, using the UC1524A control IC, it is possible to have nearly twice the normal volt-seconds, $V_{in(max)}t_{on(max)}$, during startup or after a large step increase in load current. This means that the flux density cannot be permitted to go more than half way toward saturation under normal conditions or the core will saturate under transient conditions.

Saturation flux density for 3C8 power ferrite material is greater than 0.3 Tesla (3000 Gauss), allowing a ΔB of 0.15 T (0 to 0.15 T) in this application. (With volt-second control, available in the UC1840 control IC, a ΔB of 0.3 T would be permissible, significantly reducing the transformer size.)

Core Selection

The core area product, AP, requirements in this application are calculated using Equation 1 and Table I of Section M5 with power input of 333 watts and frequency of 40 KHz.

$$AP = A_w A_e = \left(\frac{11.1 P_{in}}{K \Delta B f} \right)^{1.143} = \left(\frac{11.1 \cdot 333}{0.141 \cdot 0.15 \cdot 40,000} \right)^{1.143} = 5.4 \text{ cm}^4$$

This equation is based on the assumptions that the windings occupy 40% of the window area, the primary and secondary windings are of equal area, and the windings are operated at a current density that will result in a temperature rise of 30°C with natural convection cooling.

From Table I, Section M1, the EC52 core with an AP of 5.71 cm⁴ is the obvious choice.

Designing the Windings

The minimum number of primary turns required to support the volt-seconds required for normal operation is calculated from Equation 2 of Section M5:

$$N_p(\min) > \frac{5000 V_{in}(\min)}{\Delta B A_e f} > \frac{5000 \cdot 200}{0.15 \cdot 1.83 \cdot 40,000} > 91 \text{ turns}$$

From Equation 3, the primary to secondary turns ratio is:

$$n = \frac{N_p}{N_s} = \frac{0.9 D [V_{in}(\min) - V_{CE}(\text{sat})]}{V_o + V_F} = \frac{0.45(200 - 2)}{5 + 0.8} = 15.36$$

Secondary turns from Equation 4:

$$N_s = \text{Integer}(N_p/n) = \text{Integer}(91/15.36) = 6 \text{ turns}$$

Recalculate the primary turns:

$$N_p = 6 \times 15.36 = 92 \text{ turns}$$

RMS primary current from Equation 6:

$$I_p = I_{in}(\max)/K_t = \frac{P_{in}(\max)}{V_{in}(\min) K_t} = \frac{333}{200 \cdot 0.71} = 2.34 \text{ A}$$

From Equation 7, the maximum current density for this size core is:

$$J_{\max} = 450 A P^{-.125} = 450(5.71)^{-.125} = 362 \text{ } \Omega/\text{cm}^2$$

The minimum primary wire area, A_{xp} , is:

$$A_{xp} = I_p(\max)/J_{\max} = 2.34/362 = .0065 \text{ cm}^2$$

From the Wire Table in Section M2 under 'AREA, Copper', AWG 19 is appropriate.

The maximum RMS secondary current, I_s , occurs at 50% duty cycle:

$$I_s(\max) = I_o(\max)/1.414 = 50/1.414 = 35.3 \text{ A}$$

Minimum secondary wire area, A_{xs} , is:

$$A_{xs} = I_s(\max)/J_{\max} = 35.3/362 = .0975 \text{ cm}^2$$

From the Wire Table, this calls for AWG 7 to 8. Ten AWG 18 wires in parallel will carry the required secondary current and provide a smooth winding with less leakage inductance and acceptable eddy current losses. Copper strip 2.5x.04 cm could also be used.

The number of turns required for the auxiliary winding is:

$$N_a = \frac{V_{dd} N_p}{V_{in}(\min)} = \frac{15 \cdot 92}{200} = 7 \text{ turns}$$

This will provide enough volt-seconds during flyback to reset the core (back to zero flux density) at 50% maximum duty cycle. AWG 32 wire is adequate to carry the V_{dd} supply current. This winding should be tightly coupled to the primary.

Double-check the wire fit in the window (neglect N_g). The total copper area of all windings should be less than 40% of the total window area of the core ($0.40 \times 3.12 = 1.25 \text{ cm}^2$ max).

$$A_w' > N_p A_{xp} + N_s A_{xs} = 92(.0065) + 6 \times 10(.00823) = 1.09 \text{ cm}^2$$

Calculate Losses and Temperature Rise

The total losses in the windings is calculated from Equation 12. The mean length per turn, l_t , for the EC52 core is 7.3 cm, and AWG 19 wire is .000353 Ω/cm from the Wire Table at 100°C.

$$P_w = 2 I_p^2 N_p l_t (\Omega/\text{cm}) = 2(2.34)^2 \times 92 \times 7.3 \times .000353 = 2.59 \text{ watts}$$

The total core losses for 3C8 ferrite are obtained from Figure 1 in Section M3. The flux density axis of this graph assumes the transformer is operating with a symmetrical flux swing about the origin. The forward converter operates asymmetrically, so enter the graph with $\Delta B/2$, or .075 T. The resulting 0.1 W/cm³ must be multiplied by the core volume to obtain the total core loss, P_c .

$$P_c = .01 \times 18.7 = .187 \text{ watts}$$

Total transformer losses are:

$$P_t = P_w + P_c = 2.59 + .187 = 2.78 \text{ watts}$$

The temperature rise of the core for natural convection cooling is calculated from Equation 14:

$$\Delta\theta = \frac{850 P_t}{A_s} = \frac{850(2.78)}{91} = 25.9^\circ\text{C}$$

Summarizing the transformer design:

Core: Ferroxcube EC52, 3C8 Ferrite E-E core
 N_p: 92 turns AWG19
 N_a: 7 turns AWG32
 N_s: 6 turns 10xAWG18 (10 wires paralleled)

The primary and auxiliary windings are tightly coupled. The secondary is insulated with 2mil mylar tape to provide 3750 volt line isolation capability.

Filter Inductor Design

The design of the filter inductor is covered extensively in Unitrode Application Note U68A, in the Unitrode Databook. Using this approach, the inductor design is summarized as follows:

Core: Ferroxcube 4229-3C8 Ferrite Pot Core
 Winding: 7 turns 10xAWG17 (10 wires paralleled)
 Losses: 2.2 watts
 Temperature Rise: 35°C

DETERMINING THE CHANGE IN ZENER VOLTAGE WHEN THE CURRENT IS CHANGED

A common question concerning zener diodes is "what will be the zener voltage at a current different from the current now specified?"

The difficulty is that the impedance of a zener is not a constant, and changes with the current, so the zener voltage is a non-linear function of current.

Here is a useful equation that gives a good approximation to the change in zener voltage when the current is changed from one value to another value.

$$\Delta V_z \cong k_z \ln\left(\frac{I_2}{I_1}\right)$$

where $k_z = I_z \times Z_z$ and I_z is chosen approximately midway between I_1 and I_2

The equation does not include the effect of pulse or dc-heating on the zener voltage. If appreciable junction heating is involved the thermal model must also be used.

Here is an example of how the equation is used.

Question: If the voltage of a UZ5733 is specified as 33V at 40mA, what will be its voltage when measured at 5mA?

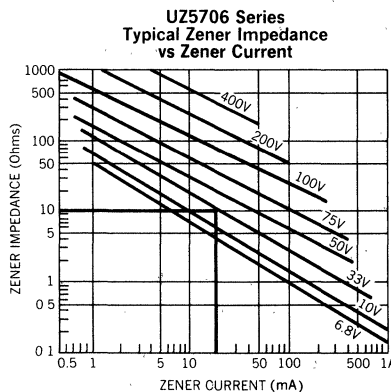
Using the graph of Z_z versus I_z on the data sheet for this device, and choosing a value of I_z at 20mA,

$$Z_z = 10\Omega$$

$$\text{So } k_z = I_z \times Z_z = 20\text{mA} \times 10\Omega = 0.20\text{V}$$

$$\Delta V_z \cong k_z \ln\left(\frac{I_2}{I_1}\right) = 0.20 \times \ln\left(\frac{5\text{mA}}{40\text{mA}}\right) = 0.20 \times \ln(0.125) = 0.20\text{V} (-2.08) = -0.42\text{V}$$

Thus the zener voltage at 5mA will be $33\text{V} - 0.42\text{V} = 32.6\text{V}$

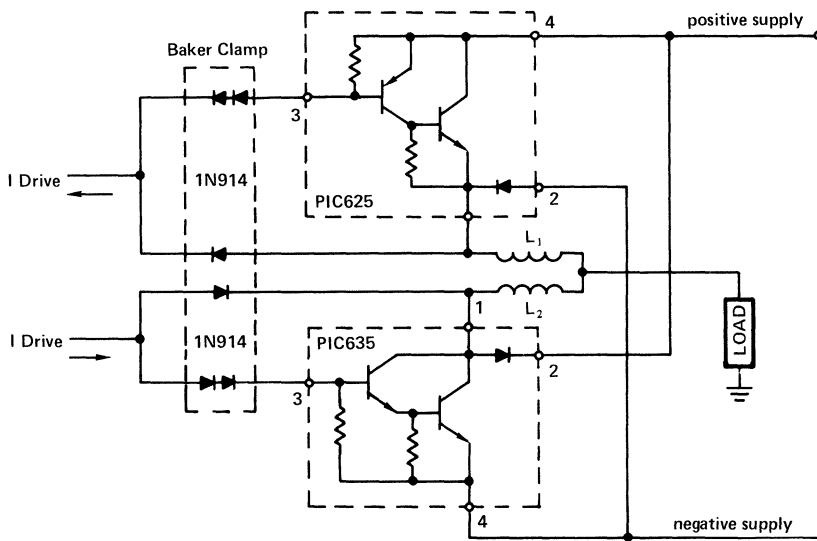


MINIMIZING STORAGE TIME WHEN USING UNITRODE SWITCHING REGULATOR POWER OUTPUT CIRCUITS (PIC600 SERIES)

In some applications (such as a reversing motor drive, for example: stepper motor) where storage time is an important consideration in the design, the normal storage time of PIC600 series (approximately 600ns) can be reduced to acceptable level.

At lower output currents, the excess storage time is a result of the driver stage operating well under saturation, while at higher output currents it is a result of the output transistor operating into quasi-saturation region.

The storage time can be reduced to less than 100ns by utilizing a Baker Clamp technique as shown in the circuit below:



The Baker Clamp will increase the $V_{CE(sat)}$ losses but this disadvantage will be more than offset by the improved switching speed.

The Baker Clamp circuit varies the drive current of the PIC600 series for optimum switching speed at any given load current. The drive current required to the Baker Clamp can be unregulated, as long as it is greater than 30mA.

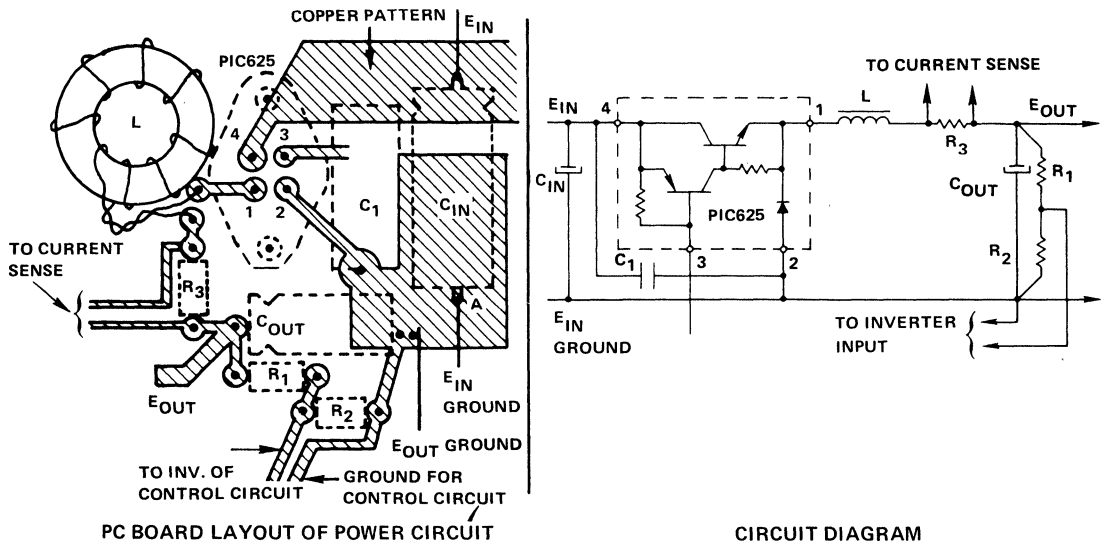
The small value of the inductor L_1 and L_2 (5 to 10 μ H) stops cross conduction during the switching of PIC600 series.

AVOIDING SPURIOUS OSCILLATION WHEN USING UNITRODE SWITCHING REGULATOR POWER OUTPUT CIRCUITS (PIC600 SERIES)

Avoid spurious oscillation due to ground loops and RFI when using a Unitrode Switching Regulator Power Output Circuit (PIC600 Series) in a switching regulator.

The Unitrode switching regulator power output stage (PIC600 Series) is a high frequency fast switching device. Its control circuitry must also operate at high frequency and high gain. Therefore, it is necessary to avoid any ground loops and RFI for stable circuit operation.

The high frequency roll-off of the control circuit should be adjusted properly with a compensation network. The typical layout of the power circuit is shown in the figure below.



Capacitor C_1 ($0.2 \mu f$) reduces the RFI generated due to the reverse recovery current spike of the catch diode, and should be physically located near pin 4 and pin 2 of the PIC625. The capacitor should be a high frequency by-pass capacitor, such as Polystyrene.

The current sense resistor R_3 should be a non-inductive (carbon) type. The current sense signal should be picked up right across this resistor.

If the switching regulator is operated at the higher end of the input voltage, the inductor should be shielded with an electrostatic shield, grounded to Point A. The case of PIC625 should also be connected to Point A.

HOW TO SAFELY CHECK SUSTAINING VOLTAGE ON POWER TRANSISTORS

One of the most important parameters for any power transistor, particularly in switching applications with inductive loads, is the sustaining voltage. Many manufacturers specify only open base sustaining voltage ($V_{CEO(SUS)}$) at a low current level (10 to 200mA); and, even where sustaining voltage with resistive bias ($V_{CER(SUS)}$) or voltage bias ($V_{CEX(SUS)}$) is specified on a data sheet, the chances are that it will not be specified under the exact conditions that will be required by a specific application. Because of this, many designers select a transistor based on its $V_{CEO(SUS)}$ rating, since V_{CER} or V_{CEX} will always be greater than V_{CEO} (see Figure 1 for a graphical explanation of the relationship among V_{CEO} , V_{CER} and V_{CEX}).

By choosing a transistor based upon its V_{CEO} rating, the designer may be using a higher voltage device than necessary. If he could determine the voltage under the actual conditions of his application, it is possible that a lower voltage device could be used, resulting in considerable cost savings. Figure 2 presents a test circuit that can be used to safely measure sustaining voltage under any bias condition at collector currents up to 5A.

PLEASE NOTE: SUSTAINING VOLTAGE SHOULD NEVER BE READ ON A CURVE TRACER, EVEN AT LOW CURRENT LEVELS, SINCE POWER RATING OR REVERSE-BIASED SECOND-BREAKDOWN RATING ($E_{S/b}$) MAY BE EXCEEDED, RESULTING IN PERMANENT DAMAGE TO THE TRANSISTOR.

The test circuit of Figure 2 may also be used to check a transistor's $E_{S/b}$ rating if the zener clamp is removed. $E_{S/b}$, under a specified bias condition of R_{BB} and V_{BB} , is related to collector current and inductance as follows:

$$E_{S/b} \text{ (joules)} \cong 1/2Li^2$$

Where i is the peak collector current flowing at the time the transistor is turned-off.

It should be noted, however, that the transistor is not protected without the zener clamp, and the device may be damaged or destroyed if it does not meet its $E_{S/b}$ rating.

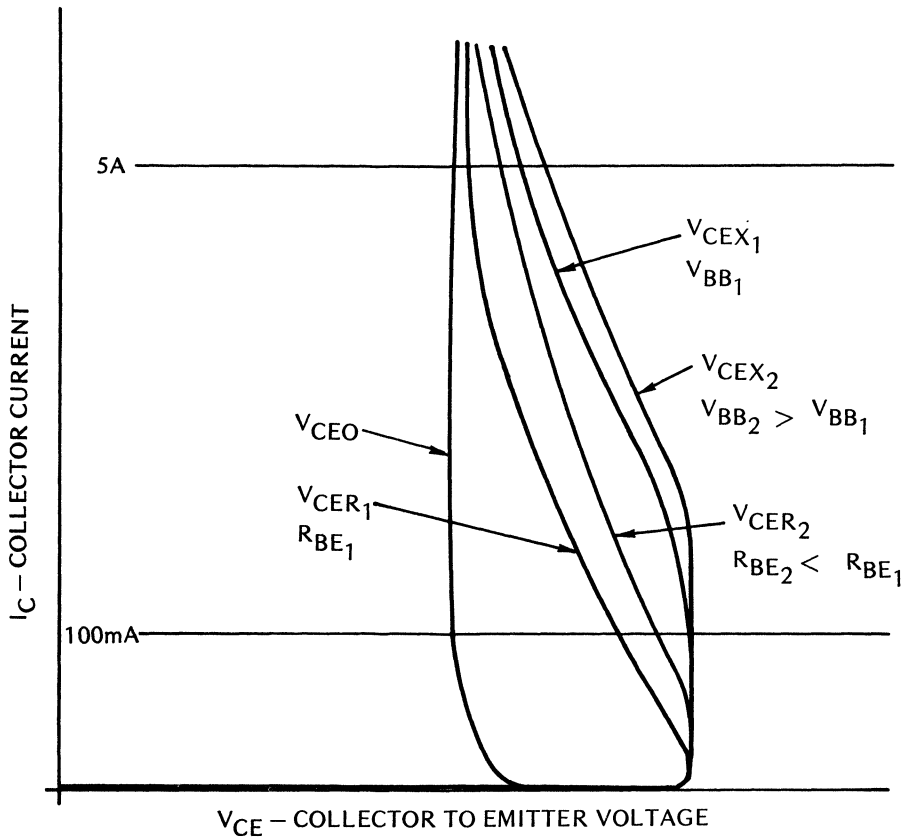
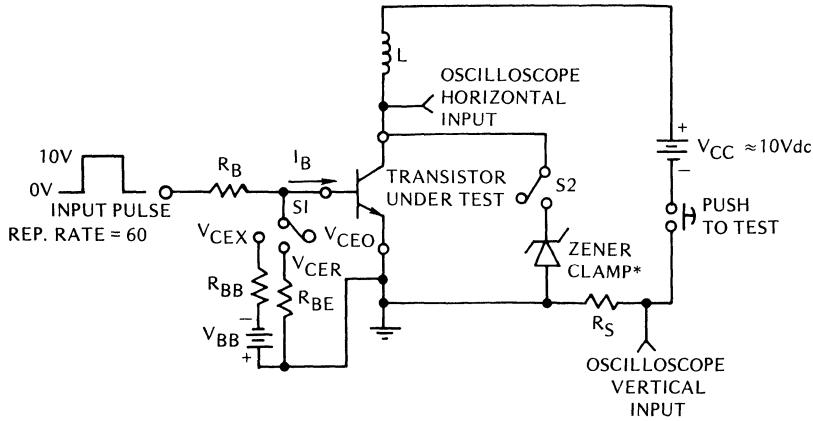


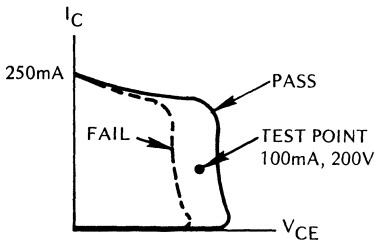
Fig. 1. Relationship among $V_{CEO}(SUS)$, $V_{CER}(SUS)$, $V_{CEX}(SUS)$
(Not to Scale)



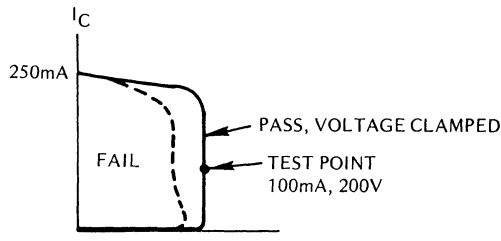
*ZENER CLAMP VOLTAGE SHOULD BE EQUAL TO THE MINIMUM SPECIFIED VALUE OF THE V_{CEO} , V_{CER} OR V_{CEX} VOLTAGE BEING CHECKED.

VOLTAGE RATING (V_{CEO} , V_{CER} , V_{CEX})	TEST CURRENT (I_C) ¹	INDUCTOR (L)	CURRENT SENSE (R_S)	I_B	INPUT PULSE WIDTH
≤80V	≤50mA	50mH	10Ω	0.1(I_C)	350μSec
	50mA–200mA	20mH	5Ω	0.1(I_C)	525μSec
	200mA–1.0A	2mH	1Ω	0.1(I_C)	250μSec
	1.0A–5.0A	0.5mH	0.2Ω	0.1(I_C)	325μSec
80V–200V	≤50mA	100mH	10Ω	0.1(I_C)	800μSec
	50mA–200mA	40mH	5Ω	0.1(I_C)	1.0mSec
	200mA–1.0A	4mH	1Ω	0.1(I_C)	550μSec
	1.0A–5.0A	1mH	0.2Ω	0.2(I_C)	650μSec
≥200V	≤50mA	200mH	10Ω	0.1(I_C)	1.5mSec
	50mA–200mA	80mH	5Ω	0.1(I_C)	2.0mSec
	200mA–1.0A	10mH	1Ω	0.2(I_C)	1.25mSec
	1.0A–5.0A	2mH	0.2Ω	0.2(I_C)	1.25mSec

1. THE ZENER CLAMP SHOULD ALWAYS BE USED WHEN TESTING AT COLLECTOR CURRENT VALUES ABOVE 200mA SINCE THE REVERSE-BIASED SECOND-BREAKDOWN ($E_{S/b}$) RATING OF THE TRANSISTOR UNDER TEST MAY BE EXCEEDED.



REPRESENTATIVE SCOPE TRACE FOR UNCLAMPED TEST AT $I_C = 100mA$



REPRESENTATIVE SCOPE TRACE FOR CLAMPED TEST AT $I_C = 100mA$

Fig. 2. Test Circuit for $V_{CEO}(SUS)$, $V_{CER}(SUS)$, $V_{CEX}(SUS)$

**OPERATING THE SWITCHING REGULATOR OUTPUT CIRCUIT
(PIC600 SERIES) AT LOW FREQUENCIES**

The Unitrode switching regulator power output circuit consists basically of a power transistor switch and a catch diode. The appropriate data sheets in the Unitrode Semiconductor Databook provide the necessary information for determining junction temperature and power dissipation at frequencies above 10 kHz.

This Design Note provides a method for determining the junction temperature and maximum allowable power dissipation for the transistor switch and catch diode when the switching regulator is operated at frequencies under 10 kHz, where the switching losses are negligible and can be safely ignored.

The method of determining safe power dissipation requires a detailed transient thermal analysis, since the junctions of the transistor and diode are subjected to temperature excursions due to the applied pulse power.

When the device is subjected to a train of periodical power pulses, the maximum power dissipation and junction temperature can be calculated from the effective pulse thermal resistance (θ_p) as follows:

$$\theta_p = R_T \times D + (1-D) r(t + \tau) - r(\tau) + r(t)$$

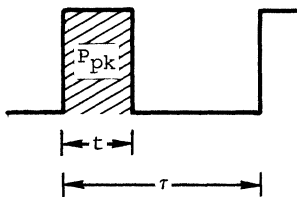


Figure 1. Power Pulses

where: t = pulse width

τ = period

Duty cycle $D = \frac{t}{\tau}$

Peak Power, P_{pk} is peak of an equivalent square power pulse

$r(t + \tau)$ = transient resistance at time $t + \tau$

$r(t)$ = transient thermal resistance at time t

R_T = DC thermal resistance (from data sheets)

1. Calculating the Junction Temperatures (Pulse Train)

A. Power Transistor Switch

The peak junction temperature of the transistor switch under repetitive peak power pulse conditions is calculated as follows:

$$T_{j(\text{peak})} = T_{\text{CASE}} + P_{\text{pk}} \times \theta_p$$

$$T_{j(\text{peak})} = T_{\text{CASE}} + V_{\text{CE}} \times I_{\text{C}} \times \left[R_{\text{T}} \frac{t_{\text{T}}}{\tau} + \left(1 - \frac{t_{\text{T}}}{\tau} \right) \times r(t_{\text{T}} + \tau) - r(\tau) + r(t_{\text{T}}) \right]$$

The transient thermal impedances $r(t_{\text{T}} + \tau)$, $r(\tau)$, $r(t_{\text{T}})$ are obtained from the transient thermal impedance plot for the transistor (see Figure 2),

t_{T} = transistor on-time

B. Catch Diode

The peak junction temperature of the catch diode under repetitive peak power pulse condition is calculated as follows:

$$T_{j(\text{peak})} = T_{\text{CASE}} + I_{\text{F}} \times V_{\text{F}} \left[R_{\text{T}} \times \frac{t_{\text{D}}}{\tau} + \left(1 - \frac{t_{\text{D}}}{\tau} \right) r(t_{\text{D}} + \tau) - r(\tau) + r(t_{\text{D}}) \right]$$

where:

$$t_D = \text{diode on-time}$$

The Transient thermal impedances $r(t_D + \tau)$, $r(\tau)$, $r(t_D)$, are obtained from the transient thermal impedance plot for the catch diode (see Figure 2).

C. Power Dissipation

The maximum allowable power dissipation in either the transistor or the diode is determined by the maximum junction temperature of 150°C:

$$P_{pk(max)} = \frac{150^\circ\text{C} - T_{CASE}}{\theta_p}$$

2. Calculating the Junction Temperature (Single Shot Power Pulse)

For a non-repetitive power pulse, the rise of junction temperature can be calculated as follows:

$$T_j = P_{pk} \times r(t) + T_{CASE}$$

For a pulse with less than 100 millisecc, the case temperature is assumed to remain at ambient temperature.

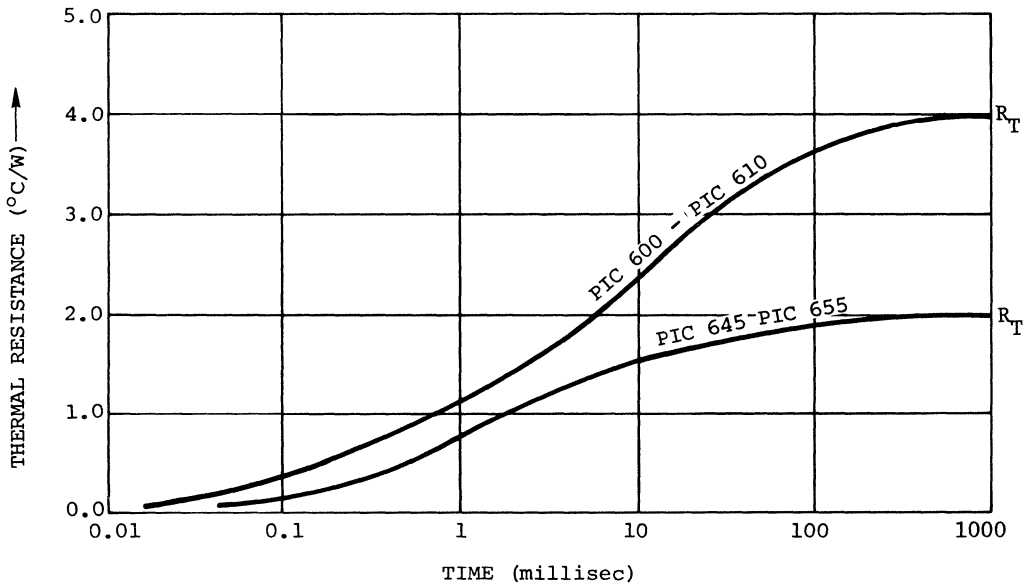


Figure 2. Transient Thermal Resistance - Power Transistor or Catch Diode

A 350 WATT SWITCHING REGULATED OUTPUT POWER SUPPLY FOR MULTIPLE OUTPUTS UTILIZING UNITRODE SEMICONDUCTOR COMPONENTS

There are many ways a switching power supply can be designed to obtain regulated output voltages. When multiple outputs are desired, such as ± 5 volts and ± 12 volts, the circuit described below provides the basis for an efficient, economical, and reliable power supply. It consists of a pulse width modulated buck regulator and a synchronized "H" (full bridge) inverter, each leg of which operates at 50% duty cycle. The block diagram of the power supply is shown in Figure 1.

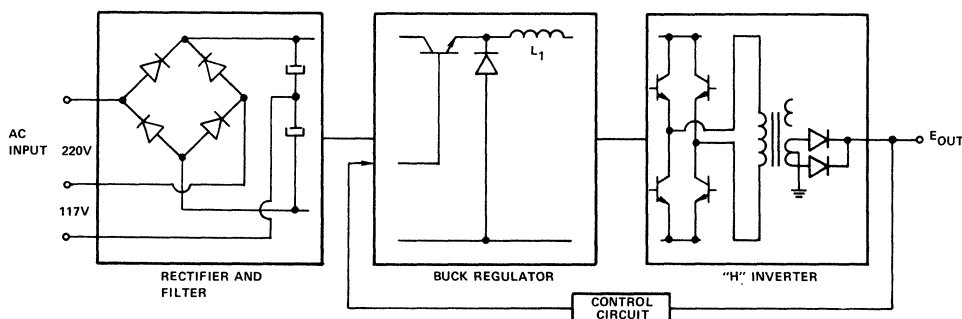


Figure 1. Block Diagram

The advantages of this design approach are as follows:

1. Numerous inductors (normally needed when pulse-width modulating an inverter) are not required. No filter inductor is required in the output which lowers costs. Minimum load bleeder resistors are not needed, thus improving efficiency and excessive heat generation. These features result from the "H" inverter operating at 100% duty cycle.
2. A high voltage, low ESR capacitor in series with the power transformer is not required. The problem of excessive collector current in an "H" inverter stage due to "walking of core flux" on a saturated B-H curve is eliminated.
3. There is no possibility of high current or forward-biased second breakdown in the inverter bridge transistors when they are simultaneously on during switching periods. The "cross-current" is limited by the inductor, L_1 , (the buck regulator acts as a constant current source) which increases reliability. Furthermore, the transistors are in saturation during cross conduction again improving efficiency, and reducing heat generation.

4. Only one high voltage switching transistor is required for either 110 or 220V input.
5. There is no possibility of forward-biased second breakdown in the bridge transistor during initial turn-on (“start-up”).
6. No expensive high voltage filter capacitor is needed. Filtering is achieved with a low voltage output capacitor.

Description of the Circuit:

The buck regulator, “H” inverter and control circuit is described in brief in this section. The detailed schematic of the circuit is shown in Figure 2.

A. Buck Regulator:

The output stage of a buck regulator consists of a Unitrode Barrier transistor™ UMT1009 and a fast recovery (50 nanoseconds) high voltage catch diode, the Unitrode UES1306. The buck regulator is operated at 50 kHz, twice the operating frequency of the “H” inverter, with very low switching losses. Operating the buck regulator at higher frequency reduces the cost of the filtering inductor, L_1 .

The output voltage is regulated in this stage by employing a pulse-width modulation technique using a UC1524. The output of the filter inductor is clamped below the BV_{CEO} of transistors used in an “H” bridge with a Unitrode zener diode UZ4212. This diode absorbs the energy stored in inductor L_1 during the period when energy is not coupled into the secondary due to the leakage inductance of power transformer T_3 . Notice that there is no output filter capacitor in the buck regulator. This design feature limits excessive cross conduction collector current in the transistors of the “H” inverter.

The base drive current to the pass transistor is provided with a unique transformer coupled drive circuit. It provides base drive current up to 100% duty cycle if required. Furthermore, a small amount of energy stored in a ferrite bead in the base drive circuit provides assistance in turning off the high voltage pass transistor.

B. “H” Inverter:

The “H” inverter operates at 25 kHz, with a 50% duty cycle in each leg, synchronized with the buck regulator. It utilizes four low voltage 2N6354 transistors. Low voltage transistors offer low $V_{CE(SAT)}$, high gain and fast switching times. Due to high gain, the base drive current required is low.

The switching losses are kept to a minimum by switching the transistors when inductor, L_1 , current is at a minimum. The storage time of the transistor is kept to a minimum by reducing the base drive just prior to transistor turn-off. (The base drive current is highest when transistor is turned on and reducing linearly.)

The diodes $D_1 - D_4$ provide the path for magnetizing current at lower output current as well as the path for energy stored in the leakage inductance of the power output transformer.

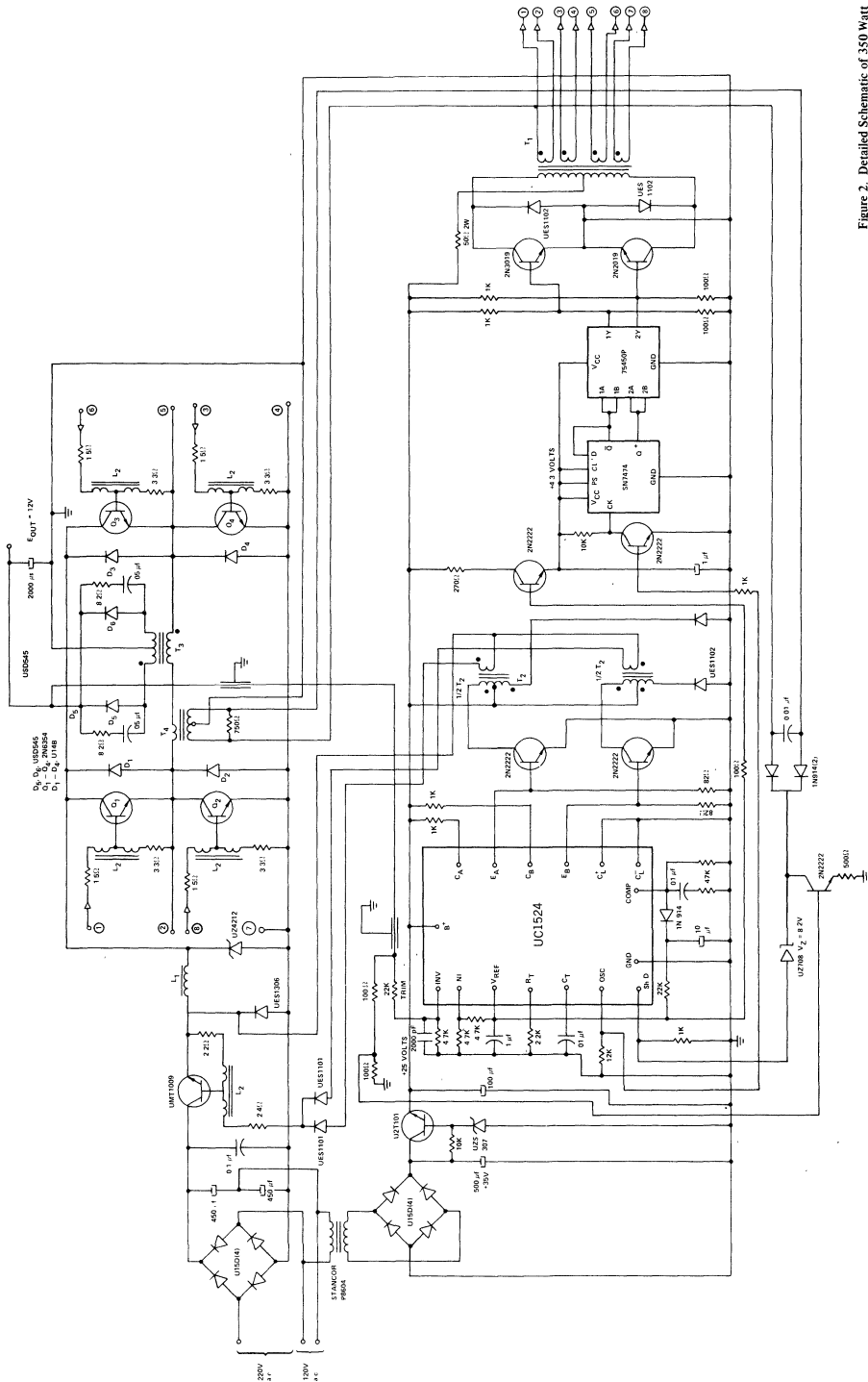


Figure 2. Detailed Schematic of 350 Watt Switching Regulated Output Power Supply

Current limiting is obtained with a current transformer. The level of the current limit is maintained constant regardless of temperature by effectively using two diodes in series with an 8.2 volt zener (Z_2) UZ708. Only one driver transformer is used for all four transistors. The transistor turn-on and turn-off is enhanced with a ferrite bead in the drive circuit.

The output is rectified with Unitrode USD545 Schottky Rectifiers which provide the advantages of low V_F at high current and minimum change in leakage current with temperature. The snubber network across the Schottky diodes prevent reverse bias breakdown from the large voltage spikes due to leakage inductance in the power transformer, and reduces RFI.

C. Control and Drive Circuits:

The regulation function is achieved with a UC1524 P.W.M. monolithic integrated circuit. The synchronizing pulses from the integrated circuit drive the D-Flip Flop, SN7474. The output of this D-Flip Flop drives the logic circuit 75450P which provides drive current to low cost 2N3019 NPN transistors. Line isolation is maintained with a driver transformer.

The control circuit (UC1524) is inhibited in a slow start mode to prevent large current and voltage transients.

The circuit described herein provides conversion efficiency up to 85%. This design approach achieves an efficient and economical switching-regulated power supply when multiple outputs are desired. The output filter capacitor is smaller in size because each leg of the "H" inverter operates at 50% duty cycle.

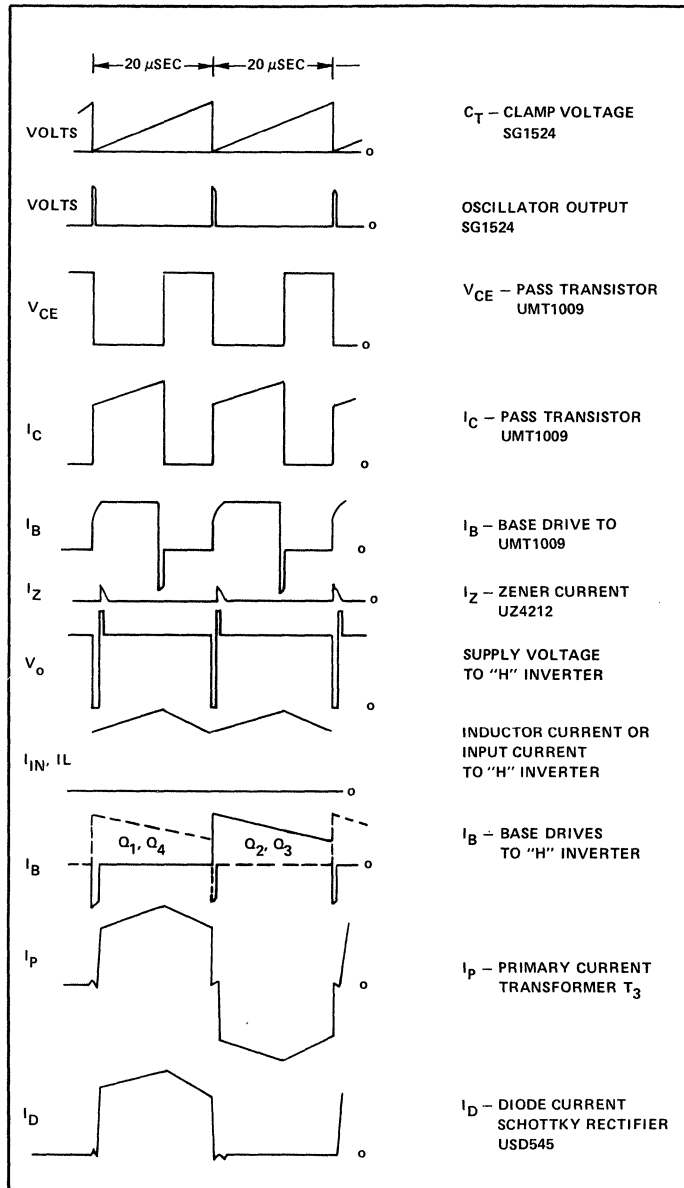




Figure 3. Basic Waveforms

TRANSFORMER AND INDUCTOR DETAILS

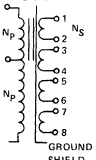
L₁. Filter Inductor;

core: Ferroxcube IF-19
 N = 198 turns, wire size AWG #16
 Air gap = 0.2 inches

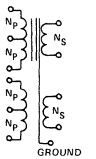
L₂. Ferrite Bead;

core: Stackpole #57-1552 Ferrite Bead
 N₁ = 2 turns, wire size #32
 N₂ = 2 turns, wire size #32

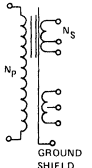
T₁. "H" Inverter Driver Transformer;

core: Ferroxcube 376U250-3C8, 376UB250-3C8
 N_P = 90 turns, wire size AWG #32
 N_S = 15 turns, wire size AWG #32


T₂. Buck Regulator Driver Transformer;

core: Ferroxcube 78E272-3C8, 782B272-3C8
 N_P = 90 turns, wire size AWG #34
 N_S = 15 turns, wire size AWG #28
 Two transformers wound on same core, over outside legs of E-I core.

T₃. Power Output Transformer;

core: Ferroxcube EC-52
 N_P = 32 turns, wire size #16
 N_S = 4 turns, wire size #26, 36 wires twisted together
 NOTE: Secondary is designed for +12 volts output. For multiple output total copper area of secondary should be 0.30 x Total Window Area.

T₄. Current Transformer;

core: Ferroxcube 376U250-3C8, 376B250-3C8
 N_P = 2 turns, wire size AWG #16
 N_S = 60 turns, wire size AWG #32

NOTE: The information presented in this bulletin is believed to be accurate and reliable. However, no responsibility is assumed by Unitrode Corporation for its use.

Unitrode Corporation makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

SQUIB-FIRING CIRCUIT PROVIDES FOR RELIABLE FIRING, FROM LOW LEVEL INPUTS

The design of reliable squib-firing circuitry often presents particular problems. Squib functions are typically quite critical, and the initial triggering source for these systems is, by nature, usually minute.

Conventional transistor squib-firing circuits usually require several gain stages, together with a power transistor to handle the squib-firing current. Mechanical squib switches, on the other hand, cannot be operated repetitively to allow for complete testing of the device and associated circuitry during check-out.

The high sensitivity planar Silicon Controlled Rectifier (SCR) can be triggered directly from low-level input circuitry, with significant reduction in circuit complexity and size. Reliability is thus considerably enhanced.

The unique characteristics of the planar SCR have resulted in wide usage of this semiconductor component in squib-firing circuits for rocket engine ignition, detonation, and explosive bolt applications. Compared with conventional transistor techniques or mechanical squib switches, this proven approach has significant reliability advantages, with circuit simplicity, size reduction, mechanical ruggedness and elimination of electrical contacts.

An SCR, with surge current ratings at 100°C of 5 amperes-50 milliseconds or 20 amperes-1 millisecond can easily handle the current required for firing most squibs. Input circuits can be designed to trigger reliably at levels below 100 microamperes and 1.0 Volt, making the SCR particularly well-suited for direct drive from low level control logic circuits and simple RC time delay networks. In addition, the bistable properties of the SCR enable it to be triggered on by a pulse input—remaining in the “ON” state until reset. This inherent “memory” is frequently used to advantage in arming circuits.

Two circuits typical of squib firing applications are shown in Figures 1 and 2. Both will operate from -65°C to over 125°C.

In Figure 1, Capacitor C_1 is charged to +28 Volts through R_1 and stores energy for firing the squib. A positive pulse of 1 mA applied to the gate of SCR₁ will cause it to conduct, discharging C_1 into the squib load X_1 . With the load in the cathode circuit, the cathode rises immediately to +28 Volts as soon as the SCR is triggered on. Diode D_1 decouples the gate from the gate trigger source, allowing the gate to rise in potential along with the cathode so that the negative gate-to-cathode voltage rating is not exceeded. This circuit will reset itself after test firing, since the available current through R_1 is less than the holding current of the SCR. After C_1 has been discharged, the SCR automatically turns off—allowing C_1 to recharge.

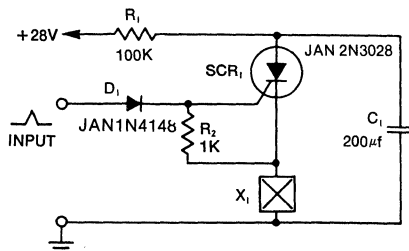


FIGURE 1

In Figure 2, energy for firing the squib is supplied directly from the +28 Volt supply. Caution must be exercised when arming this type of circuit. If anode voltage is applied too rapidly, the SCR may fire. This dv/dt effect acts through the SCR anode-gate capacitance (15 pf), which couples current to the SCR gate (in proportion to anode dv/dt). The effect is negligible if dv/dt is under 1 Volt/ μs —as in Figure 1, where it is limited by the charging of C_1 . Faster rates of rise can be safely handled by increasing the SCR gate bias.

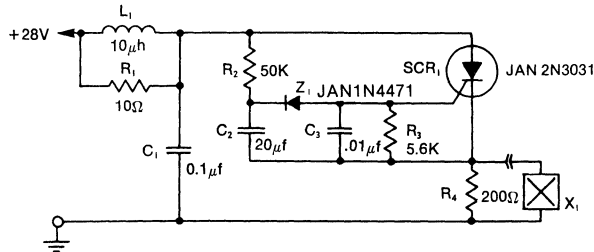


FIGURE 2

In Figure 2, the LRC input network limits the anode dv/dt to a safe value—below 30 Volts/ μs . R_1 provides critical damping to prevent voltage overshoot. While a simple RC filter section could be used, the high current required by the squib would dictate a small value of resistance and a much larger capacitor. Resistor R_3 provides DC bias stabilization, while C_3 provides stiff gate bias during the transient interval when anode voltage is applied.

In this circuit the SCR is fired one second after arming by means of the simple $R_2 C_2 Z_1$ time delay network. R_4 provides a load for the SCR for testing the circuit with the squib disconnected—limiting the current to a level well within the continuous rating of the SCR. The circuit can be reset by opening the +28 Volt supply and then re-arming.

COMBINED AC-DC LOAD CONTROL SIMPLIFIES SCR RESET

Silicon Controlled Rectifiers (SCRs) are finding increased use in a wide variety of control circuit and power switching applications. They offer an economical way to achieve high switching gain, efficiency and blocking voltage.

When the inherent memory or "latching" feature is not desired, AC anode supply is often used, allowing the SCR to turn off automatically upon removal of the gate control signal. With an AC anode supply, an additional benefit is derived—the SCR doubles in function as a rectifying element. Thus, it is possible to operate DC loads directly from an AC power source, often eliminating the need for separate bulky and expensive DC power sources.

When SCR latching action is desired, DC anode supply is commonly employed. Here, however, reset can be a problem, since "brute force" reset techniques must normally be used. This involves an additional switching element, to either open or shunt the load voltage, and current from the SCR.

The circuit of Figure 1 retains the advantages of operating loads directly from an AC power source. Latching action is provided with no need for brute force reset techniques. The DC source needs to provide only a few milliamperes of SCR holding current, since load power is drawn from the AC source.

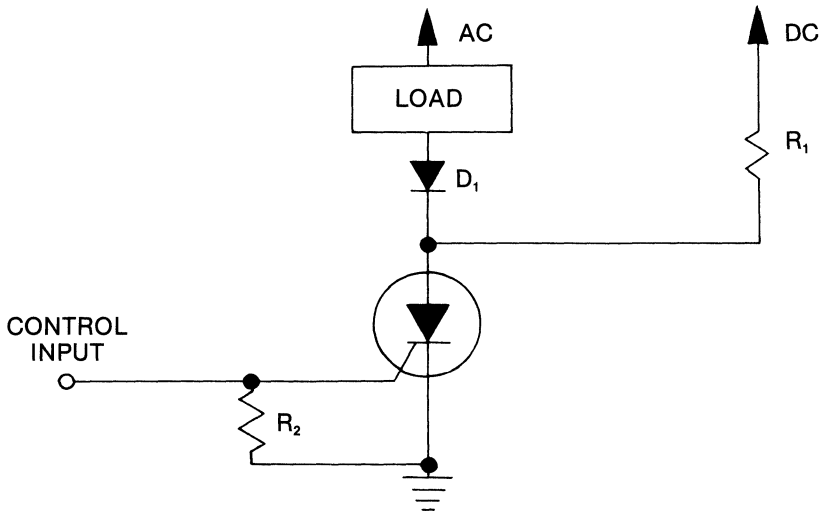


FIGURE 1

When the SCR is on, a half-wave rectified voltage waveform is applied to the load. During each positive half-cycle of the AC source, diode (or rectifier) D_1 and the SCR conduct the load current as well as the DC holding current provided through R_1 . During each negative half-cycle, D_1 blocks the negative voltage from the AC supply, allowing the SCR to remain in conduction. Resistive loads such as heaters and incandescent lamps are driven satisfactorily with the half-wave rectified output of this circuit. DC loads that are less tolerant of this waveform can easily be operated by using shunt capacitors or other filtering methods. Shunt free-wheeling diodes should be employed across inductive loads.

Reset is simply accomplished by interrupting the holding current provided from the DC supply through R_1 . The reset interval must, of course, be longer than one half-cycle of the AC line frequency, or it must be timed to occur during the negative half-cycle, since load current will keep the SCR latched on during the entire positive half-cycle. The reset interval must exceed the device gate recovery time which ranges from less than $0.5 \mu\text{s}$ for the higher speed SCRs to $50 \mu\text{s}$ for the slower SCRs.

The DC supply voltage level is not critical and can be less than equal to, or greater than the peak AC supply voltage. When it is less than the peak AC, however, D_1 will conduct for a portion of each half-cycle when the SCR is off, causing a current pulse to flow from the AC to the DC supply through R_1 .

D_1 must have a blocking voltage capability greater than the sum of the peak AC voltage plus the DC supply voltage. The SCR voltage rating must be at least equal to the peak AC or DC supply voltage, whichever of these is greater.

When many identical or similar circuits are used in a single system (as in a band of SCR incandescent lamp drivers), multiple reset is easily accomplished by simultaneously interrupting the DC source and resetting all circuits connected to that source.

TURN-OFF METHOD FOR SCRs MINIMIZES EFFECT OF DV/DT

SCRs can be turned off by reducing the magnitude of the anode current to a level below that of the holding current, either by opening the anode circuit or by driving the anode negative. Forward blocking voltage cannot be reapplied until after the minority carrier charge stored in the device as a result of previous forward conduction has been dissipated to a level that can be controlled by the gate bias, otherwise the SCR will self-trigger on again.

In addition, even after the SCRs have recovered, reapplication of anode supply voltage may cause self-triggering due to dv/dt .

Self-triggering of a SCR due to dv/dt is caused by a capacitive current equal to the product of the anode-gate (C_{AG}) capacitance of the SCR and the rate of rise (dv/dt) of applied anode voltage. Sensitivity of a SCR to dv/dt effects can be controlled by the use of a gate-cathode resistor or a current bias. The SCR will self-trigger only if the capacitive current is too large to be controlled by the bias resistor. The smaller the bias resistor, the higher will be the critical rate of rise of anode voltage. However, if the anode-gate capacitance is fully charged before the supply voltage is reapplied across the SCR, the device will be immune to dv/dt effects.

A simple SCR switching circuit is shown in Figure 1. When switch S1 (which can be a relay or a transistor) is in the closed position, the SCR will fire upon the application of a gate trigger pulse of the appropriate magnitude and duration. Switch S1, when opened, will turn off the SCR. After switch S1 is opened, the anode-gate capacitance will charge through the load resistor and the 100K between gate and ground. When the SCR has recovered, S1 can be closed, and no capacitive current will flow since C_{AG} is already charged to the full anode supply voltage.

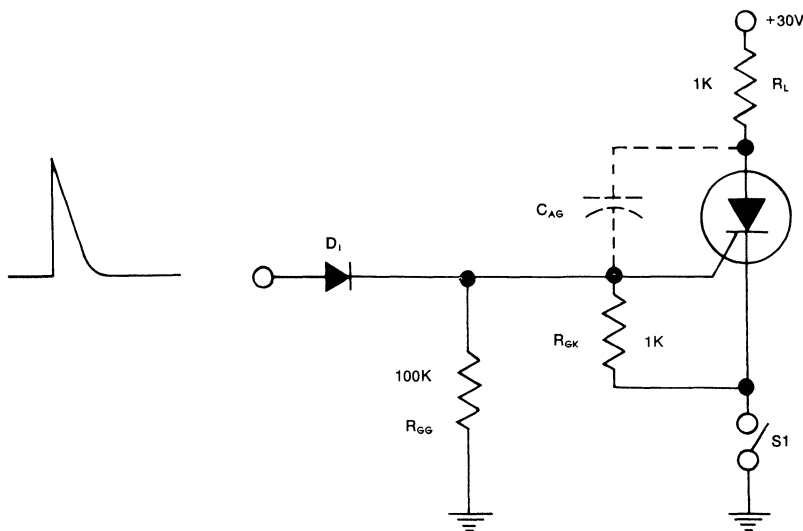


FIGURE 1

When the cathode circuit of a conducting SCR is initially opened, a large reverse gate current can flow which may damage the gate-cathode junction of the device. Reverse gate current should be limited to 3 ma for safe operation of most SCRs. The bias resistors shown in Figure 1 accomplish this objective, while affording bias stabilization over the operating temperature range. Bias resistor R_{GK} removes all of the internally supplied gate current out through the gate terminal. Under this condition, the internal gate current cannot flow across the gate junction; the device is cut-off, and self-triggering cannot occur. If R_{GK} was connected to the ground side of the switch, when the switch opened the reverse gate current would be about 15 mA — far exceeding the maximum reverse current rating for most SCRs. R_{GG} takes over from R_{GK} when the switch is opened, limiting the reverse gate current to less than 0.3 mA. Diode D_I decouples the gate trigger source from the SCR when the cathode switch is opened. This prevents a low impedance supply from drawing excessive reverse gate current.

For the situation where the anode supply voltage may be subjected to transient pulses or voltage spikes, a small capacitor C_{GK} , connected in parallel with R_{GK} will absorb the transient charging current. If we assume C_{AG} is 100 pf then a C_{GK} of 0.002 μ f will form a 20:1 voltage divider requiring a 10V pulse on the anode to result in the required 0.5V (at 25°C) to trigger the SCR.

NANOSECOND SCR SWITCH FOR RELIABLE HIGH CURRENT PULSE GENERATORS AND MODULATORS

The design of reliable modulator and pulse generator circuitry often presents the design engineer with seemingly conflicting requirements. In order to obtain fast rise times, "hard tubes" or hydrogen thyratrons are often used. This results in a large system which consumes considerable power and has relatively low conversion efficiency. Reliability, jitter, and stability are also common problems in these systems.

To improve reliability, as well as decrease standby power consumption and improve conversion efficiency, semiconductor devices are a natural choice. However, at the voltage and current levels most often encountered in these applications, conventional semiconductors are usually too slow.

The nanosecond SCR switch developed by Unitrode allows the designer to upgrade high current, high voltage modulator and pulse generator circuitry. A single device (GA201 or GA301*) is capable of operating in circuits with supply voltages up to 100 Volts DC and pulsed load currents in excess of 50 Amperes. It can be triggered directly from logic level signals (1 Volt, 200 microamps) and exhibits a rise time of less than 10 nanoseconds to 1 Ampere with only 10 milliamps of drive signal. Single switches operated in this mode can be used as high current replacements for avalanche transistors, modulators, and harmonic wave form generators.

Special circuitry has been developed to apply these nanosecond switches in applications where supply voltages exceed the forward blocking capability of a single device. The simplest of these is shown in Figure 1.

The 1 meg-ohm resistors act as a voltage-sharing network to insure that no single device is overvoltaged because of unequal leakage currents. Turn-on is accomplished by applying a trigger signal to the primary of the pulse transformer, T1. The capacitor, which has been charged to the supply voltage through R_C , discharges through R_L , and the string of SCRs. This circuit is useful until the number of stages used requires a pulse transformer that becomes objectionably bulky. Beyond that point the circuit of Figure 2 or 3 is used.

Figure 2 illustrates an approach that uses a pulse transformer to trigger only part of the string, while the rest of the devices in the string are supplied with gate drive through the zener diodes. With a supply voltage of 360 Volts DC, a 95 Volt $\pm 5\%$ zener diode across each SCR in the string prevents unequal voltage distribution. When SCR₃ and SCR₄ are triggered, 360 Volts appear across SCR₁ and SCR₂ causing zener diodes Z₁ and Z₂ to conduct. Since D₁ and D₂ are back-biased, the current must flow through the gate-to-cathode junctions of SCR₁ and SCR₂, thus driving them on. Up to eight stages can be stacked in this manner using a pulse transformer to drive only the bottom two SCRs in the string. Driving three SCRs with a pulse transformer allows stacking sixteen stages, which can switch a 1440 Volt load using a pulse transformer that needs to have a dielectric isolation rating of less than 300 Volts.

Figure 3 uses no pulse transformer and can be extended to virtually any number of stages. When SCR₁ is triggered, the cathode of SCR₂ drops from +100 to essentially 0 Volts. Capacitor C₁ discharges into the gate of SCR₂, causing it to conduct, and this process is repeated for SCR₃ and SCR₄. This circuit has the added feature of providing negative bias to the SCRs during recharge of the load in order to minimize the effect of dv/dt . As the voltage rises on the anode of SCR₄, current flows through the path consisting of C₄, R₄, C₃, R₃, C₂, R₂, etc. This provides negative bias for the gate-to-cathode junctions of the SCR in the string, making them less sensitive to dv/dt triggering. This allows the use of rapid recharge circuits which permits operation at higher repetition rates. Either resonant recharge or active (SCR) rapid recharge techniques may be used with these circuits.

*GA201 recommended for military, GA301 for commercial applications.

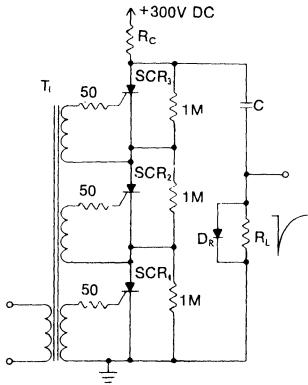


FIGURE 1

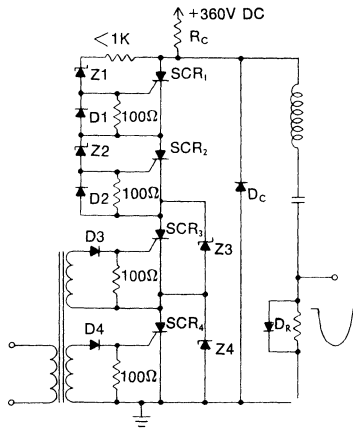


FIGURE 2

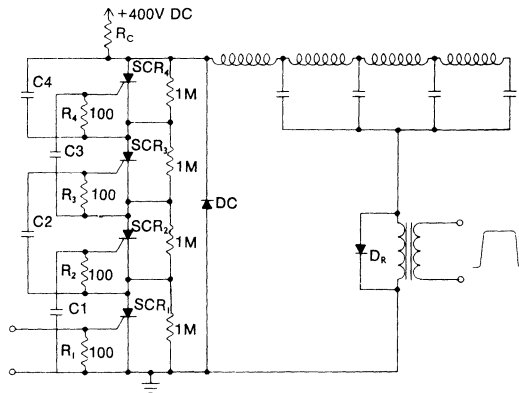


FIGURE 3

If the energy storage element(s) and load consist only of R and C components, the charging resistor must be large enough to limit the DC current to a value less than the minimum holding current of the SCRs in the string. When the load contains an inductive component, as is usually the case in modulator circuits, the network can be designed to "ring" in order to reverse-bias the SCR string momentarily, permitting the SCRs to regain their forward blocking capability even though R_c allows more than the minimum holding current to flow. Diode D_R may be used in all circuits so that the recharge current will not flow through the output element. In Figures 2 and 3, D_R shunts the reverse "ringing" current around the output element. Diode D_C must be used in circuits that contain inductive elements to protect the string from being excessively back-biased due to circuit ringing.

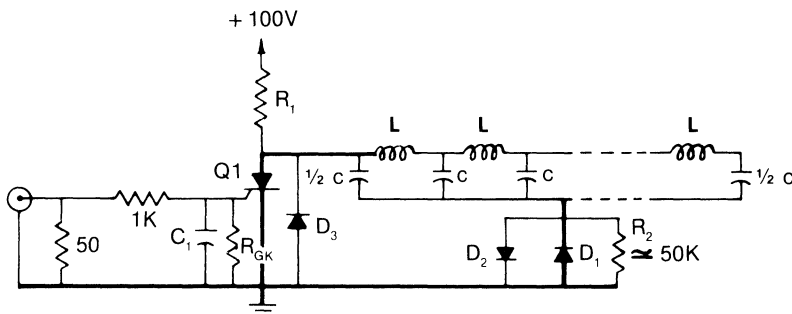
NANOSECOND SCR FOR LASER DIODE PULSE DRIVER

The use of pulsed gallium-arsenide lasers requires a reliable high speed, high current switch to drive these devices. In the past the only solid state devices that could be used in this application were avalanche transistors and fast medium power transistors. Avalanche transistors presented reliability problems, while the standard medium power transistors available were too slow. The GA200 series "Nanosecond SCR" with a rise time capability of 10 nsec to 1 Amp or 20 nsec to 30 Amps provides a solution to both the reliability and the speed problems and appears to be ideal for this type of application.

The circuit shown in Figure 1 utilizes a GA201 device along with a lumped constant delay line to generate the desired square current pulse. For simplicity, a single capacitor could be used instead of the delay line. The delay line, however, has the advantage of producing a square pulse that provides sharp turn-off, which limits the excess power dissipation that would occur in the laser diode if the pulse fell exponentially. The impedance of the delay line ($= \sqrt{L/C}$) is chosen to produce a slight mismatch, which produces overshoot on the trailing edge of the pulse. This overshoot acts as a reverse bias on the anode of the SCR, assisting in turning it off. A typical value for the delay line impedance would be 1 to 2 ohms, which approximates the impedance of the load formed by the SCR and laser diode in series. The time duration of the pulse ($= \sqrt{L/C}$ per section) can be made as short as desired with a value of 50 to 100 nsec being typical.

With the SCR in the off state, the delay line will charge to the supply voltage (100 Volts with GA201). A gate current at the input of as little as 200 μ A will trigger the SCR. The delay line will then discharge, producing a square current pulse through the gallium-arsenide laser diode. R_1 and R_{GK} are chosen so that the current, after the delay line discharges, will be less than the holding current of the GA201 ($= 3$ mA with $R_{GK} = 100$ ohms.) C_1 should be about .001 μ f and is necessary to prevent false triggering through noise or through dv/dt commutation. D_2 provides a charging path for the delay line, while $R_2 \cong 50K$ provides a stable ground reference. Diode D_3 insures that the reverse breakover voltage of the GA201 will not be exceeded during the turn-off period.

The forward current level will depend upon the total impedance of the GA201 and the laser diode and the charging voltage used. With a 100 Volt device and a practical minimum circuit impedance of about 1 ohm, it is possible to develop peak currents of up to 100 Amps. (See Figure 2 for Time vs Current curve for GA200/GB200 Series.) Pulse of 60 Amps with rise times of approximately 30 nsec have actually been achieved. For improved performance at high current levels, the SCRs may be operated in parallel or in series. Parallel operation is achieved by providing equal series resistors to the gates of the devices and driving them from the same source. By overdriving the gates with 50 to 100 mA, simultaneous turn-on is guaranteed. Parallel operation results in lower forward voltage drop and faster rise time at high current levels. Series stringing techniques can be used in circuits with a higher total impedance where higher voltages are needed to obtain the desired current levels. For a description of series operation see Design Note 14.



Q1—GA201/GB201, GA301/GB301

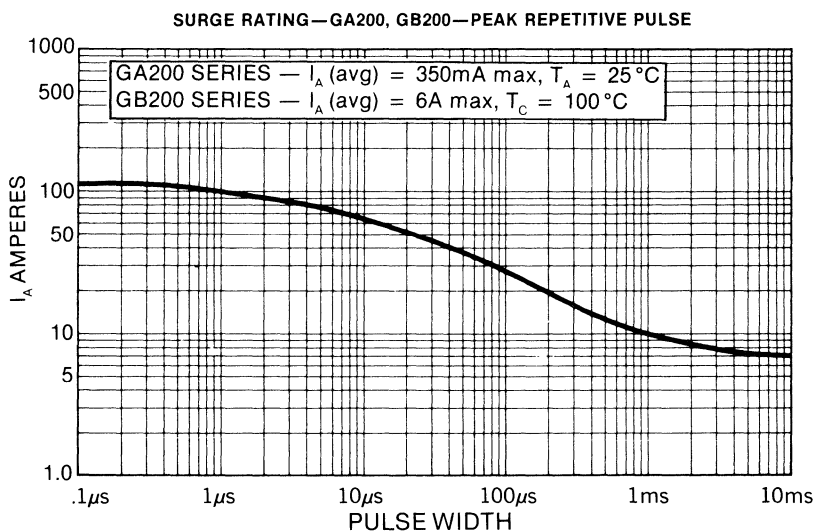
D₁—Gallium-Arsenide Laser Diode

D₂—JAN 1N5802 or 1N5807* (Alternative: UES1101 or UES1301)

D₃—JAN 1N5804 or 1N5809* (Alternative: UES1102 or UES1302)

Note: Heavy lines indicate braided connections for reduced inductance and resistance.

Figure 1



Note: For MIL and high Rel series applications, use GA/GB 200/201 and JAN Diodes.

For high rep rate (high average current), use GB series with 1N5809 or UES1302 rectifiers.

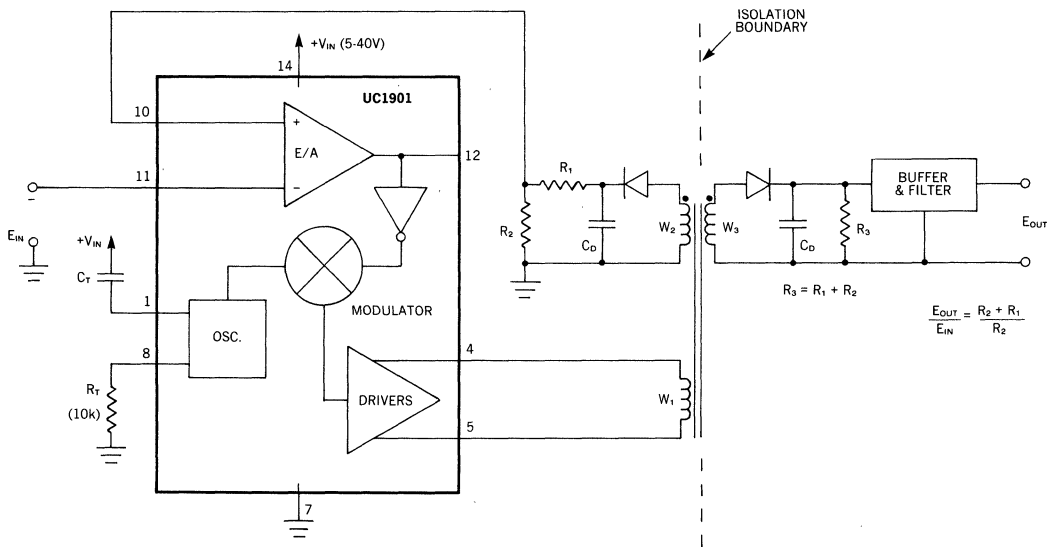
GA300 and UES series are intended for commercial applications.

Figure 2

A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal AC, transfer functions can be established across the isolation boundary.



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W_2 and W_3) on a small signal transformer. The demodulated signal from winding W_2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W_3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost

HR201 HI-REL SCREENING

Unitrode semiconductors are inherently high-reliability devices, manufactured with a quality control system that complies to MIL-Q-9858A. Some users, however, want the ultimate assurance of reliability.

In addition to those devices qualified and tested to JANTX and JANTXV specifications we can supply our broad product line of hermetically sealed devices screened to various requirements.

For discrete semiconductor devices we can screen to Table II of MIL-S-19500. Our linear integrated circuits can be screened to MIL-STD-883 METHOD 5004.6. Our switching regulator (PIC) series is not covered by a MIL specification and for this series we recommend our own UL101 or UL102 screening program. This includes:

1. Hermetic Seal: Fine and Gross leaks MIL-STD-750 Method 1071.
2. High Temperature Storage, MIL-STD-750 Method 1032.1.
3. Temperature Cycling, MIL-STD-202 Method 107.

4. Reverse Bias Clamp Test, $V_{CE0} = \text{Rated } V_{IN}$, $I_C = 5A$, $f = 25\text{KHz}$, $E_{OUT} = 5V$, $T_C = 25^\circ\text{C}$.
5. Power Stress, $T_C = 125^\circ\text{C}$, $P = 2.0W$, $t = 40 \text{ hrs.}$
6. High Temperature Reverse Bias, $T_A = 125^\circ\text{C}$, $t = 16 \text{ hrs.}$, $V_r = 80\%$ of rating.

For applications where full MIL-S-19500 Table II is not required we have our own screening specifications as follows:

PRODUCT	SPECIFICATION	SPECIFICATION WITH DELTA'S
Rectifiers	HR201	HR201-D
Zeners	HR201Z	HR201Z-D
Surge Suppressors	HR201S	HR201S-D
Transistors	HR201T	HR201T-D

MOUNTING AND THERMAL CONSIDERATIONS

TO-220 Package

The leads of the TO-220 transistors, SCRs, rectifiers and Schottky diodes may be formed, but they are not intended to be flexible or ductile enough for unrestrained lead wrapping.

The TO-220 is generally considered as the economic replacement for the TO-66 power package. Unlike the TO-66, the leads of the TO-220 may be formed if the following considerations are met.

The figures show the typical device and hardware recommended. Several typical configurations of lead forming are illustrated.

The advantages of mounting the flange to the printed circuit board is that improved thermal heat transfer allows operating at higher levels of power dissipation. The individual specification sheets give the safe operating area as a function of a case temperature.

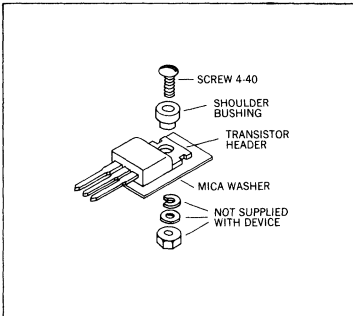


Figure A. Device and Hardware for Insulated Mounting.

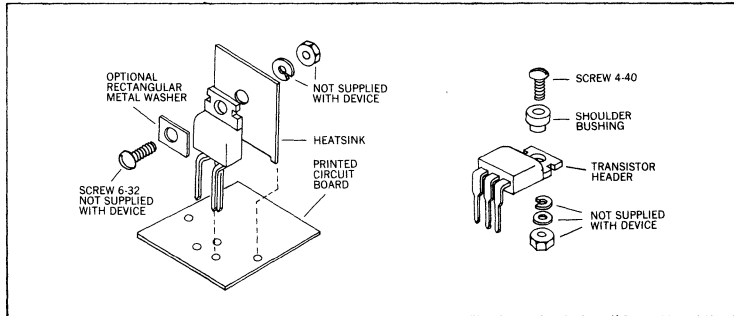


Figure B. Two Alternative Configurations for Axial Strain Relief and Electrical Isolation.

BENDING THE LEADS

Whenever the leads of the T-220 are to be formed, whether by a special fixture or by the use of long-nosed pliers, several important considerations must be followed. Internal damage to the device or lead damage may result if any or all of these precautions are not considered.

1. Minimum bend distance between the plastic body and the bend is $\frac{1}{8}$ inch.
2. The minimum radius of the bend is $\frac{1}{16}$ inch.
3. Avoid repeating bending at the same flexure point.
4. Whenever possible, use one of the lead forming configurations which relieve strain induced by mechanical or thermal loads.
5. Leads should not be bent greater than 90 degrees.
6. Avoid axial pulling or bending that would induce axial strain. The maximum axial component is 4 pounds.

7. Forming fixtures or pliers should not touch the plastic case because axial strain of $\approx .005$ " could cause irreversible internal damage.
8. The leads must be fully restrained during the lead forming operation to prevent relative movement between the body and the leads.

SOLDERING INTO THE CIRCUIT

The leads on the TO-220 are solderable; however, there are a few precautions that must be observed.

1. Soldering temperature must not exceed 270°C.
2. Maximum soldering temperature must not be applied for more than 5 seconds.
3. Maximum soldering temperature should not be applied closer than $\frac{1}{8}$ inch from the plastic body of the device.

MOUNTING THE FLANGE

Flange mounting is recommended for maximum power handling applications. A 6-32 machine screw is recommended. Eyeletting (hollow rivet) is acceptable if care is taken not to distort the flange. For insulated mount, a 4-40 screw and a shoulder bushing is recommended (see figure). Suggested material for bushings are: Diallphthalate, fiber-glass-filled nylon, or fiber-glass-filled polycarbonate. Note unfilled nylon should be avoided. The flange should not be directly soldered because the use of lead-tin could produce temperatures in excess of the maximum storage temperature. See the individual specification for the device.

Check list and summary for flange mounting:

1. Use recommended hardware.

2. Always fasten the flange prior to lead soldering.
3. Do not allow the forming tool to come in contact with the plastic body.
4. Maximum mounting torque is 8 inch-pounds.
5. Avoid modifying the flange by machining and do not use oversized screws.
6. Provide axial and transverse strain relief of the leads.
7. Use recommended insulation bushings. Avoid materials that exhibit hot-creep problems.

Thermal Considerations TO-220 Power Transistors

Thermal Resistance, Case to Ambient;
 Free Air, No Heatsink 60°C/W typical
 Thermal Capacitance
 of Package 4.8 watt-seconds/°C
 Thermal Time Constant 305 seconds

Device Type	I _C A		Power Dissipation W	Power Derating mW°C	Thermal Resistance Junction Case °C/W
	Continuous	Peak			
UMT/MJE 13004 UMT/MJE 13005	4	8	75	600	1.67
UMT/MJE 13006 UMT/MJE 13007	8	16	80	640	1.56
UMT/MJE 13008 UMT/MJE 13009	12	24	100	800	1.25
UFN732	4.5	18	75	600	1.67
UFN742	8.0	32	125	1000	1.00

Note: When using a 2 mil MICA washer for electrical isolation, add 0.4°C/W to heatsink thermal resistance.

Thermal joint compound should be used at the interface of the TO-220 flange and the heatsink to which it is attached.

Consider a TO-220 power transistor with a thermal resistance junction to case of 1.25°C/W. The junction temperature produced depends upon the mounting conditions and power dissipation in the circuit.

The table below shows junction temperature resulting from 50W of dissipation when mounted on an infinite heatsink at 25°C with different methods of interfacing.

Interface Condition Between Case and Heatsink	Thermal Resistance Case-Heatsink °C/W	Junction Temperature °C
Assumed direct, ideal metallic contact (no interference)	0.0	87.5
1 mil air gap*	1.2	147.5
Thermal compound; Tab screw torqued at 8 inch-pound	0.09	92
2 mil mica washer with thermal compound applied to both surfaces; tab screw torqued at 8 inch pound	0.58	116.5

* A film of air one mil in length has the thermal resistance of ≈ 1.2°C/W.

When using a small heat sink in free air one must consider the additional thermal resistance of the heat sink to ambient and operate at an appropriate power level. For example with an

18°C/W rated sink and thermal compound as above the device will have a junction temperature of 122°C when operating at 5W in an ambient of 25°C free air.

THERMAL DESIGN CONSIDERATIONS FOR LEADED DEVICES

For Lead Mounted Rectifiers and Zeners, for 5 types of mounting.

Determining The Power Rating for Your Application.

The information given in this section is presented for straight-forward use by the designer. The value given in this table is $R_{\theta JA}$, the "Total" thermal resistance of the diode and mounting together, no other graphs or tables are needed.

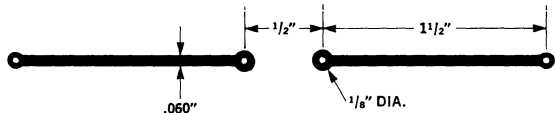
$$P_{max} = \frac{T_{Jmax} - T_{Amb}}{R_{\theta JA}}$$

Where: P_{max} is the maximum power that can be dissipated in the device reliably. T_{Jmax} is the maximum of the operating temperature range, usually 175°C, unless derated for a military or hi rel application.

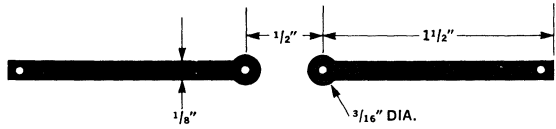
T_{Amb} is the max temp that the ambient reference (air below the device) will reach during operation.

Alternately,

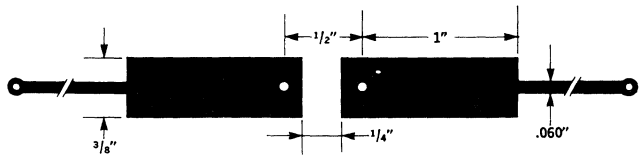
Junction Temp Rise = $PR_{\theta JA}$



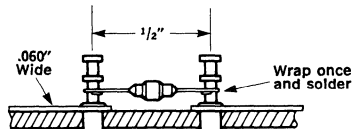
TYPE 1 PC BOARD, LIGHT



TYPE 2 PC BOARD, MEDIUM



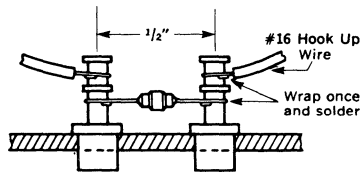
TYPE 3 PC BOARD, HEAVY



.060 Epoxy Glass
.060" dia. x 3/8" high

Terminals are per MS 17122-7

TYPE 4 PC BOARD WITH CHESSMEN TERMINALS



.060 Epoxy Glass
.125" dia. x 1/2" high

Terminals are per MS 17122-8

TYPE 5 TERMINALS AND HOOK-UP WIRES

R _{θJA} Total Thermal Resistance in Degrees C/Watt					
Type	Mounting Type				
	1	2	3	4	5
1N3611-3614	105	92	75	97	65
1N4245-4249	105	92	75	97	65
1N4461-4489	105	92	75	97	65
1N4736-4764	140	127	110	132	100
1N4942-4946	98	85	68	90	58
1N4954-4996	75	62	45	67	35
1N5063-5117	94	81	64	86	54
1N5186-5189	75	62	45	67	35
1N5186-5190	72	59	42	64	32
1N5550-5553	75	62	45	67	35
1N5614-5622	93	80	63	85	53
1N5802-5806	94	81	64	86	54
1N5807-5811	75	62	45	67	35
TVS 505-528	75	62	45	67	35
UES1101-1106	94	81	64	86	54
UES1301-1306	75	62	45	67	35
UR105-125	142	129	112	134	102
UR205-225	98	85	68	90	58
UT236-347	127	114	97	119	87
UT249-363	110	97	80	102	70
UT251-364	105	92	75	97	65
UT261-268	98	85	68	90	58
UT2005-2060	97	84	67	89	57
UT3005-3060	85	72	55	77	45
UT4005-4060	80	67	50	73	40
UTR01-61	127	114	97	119	87
UTR02-62	98	85	68	90	58
UTR10-60	176	163	146	168	136
UTR2305-2360	97	84	67	89	57
UTR3305-3360	85	72	55	77	45
UTR4305-4360	80	67	50	72	40
UTX105-125	142	129	112	134	102
UTX205-225	98	85	68	90	58
UTX3105-3120	85	72	55	77	45
UTX4105-4120	80	67	50	72	40
UZ706-140	94	81	64	86	54
UZ4706-4120	75	62	45	67	35
UZ5706-5140	75	62	45	67	35
UZ7706L-7710L	73	60	43	65	33
UZ8706-8120	140	127	110	132	100
UZS 306-440	94	81	64	86	54

LEAD MATERIALS

Unitrode offers a wide choice of lead materials for soldering or welding because the leads are attached to the pins outside the glass seal. Since the leads do not pass through a glass-to-metal seal, there is no need to match the thermal coefficient of expansion of the leads to the glass.

Solderable Leads — Silver plated copper meets the solderability requirements of MIL-STD 202C Method 208A.

Solid silver leads meeting the requirements of MIL-S-13282 Grade A are available on special order.

Weldable Leads — Three types are available to meet the welding requirements of MIL-STD-1276A. The pure grade A nickle leads meet the requirements of type N-1. The gold-plated nickle leads meet the requirements of type N-2. Gold-plating is in accordance with MIL-G-45204, Type 1.

The copper leads (tin-coated) are the standard lead materials. These leads meet the requirements of type C. Types N-2 and C are solderable as well as weldable.

The following table lists standard lead lengths and materials. Weights of the diodes with various leads are also shown. In the event other lead materials are required, please consult Unitrode.

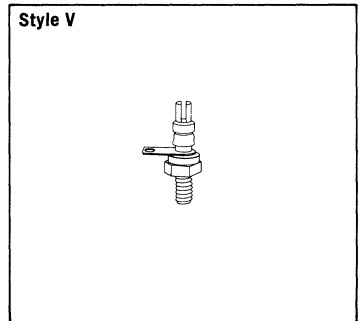
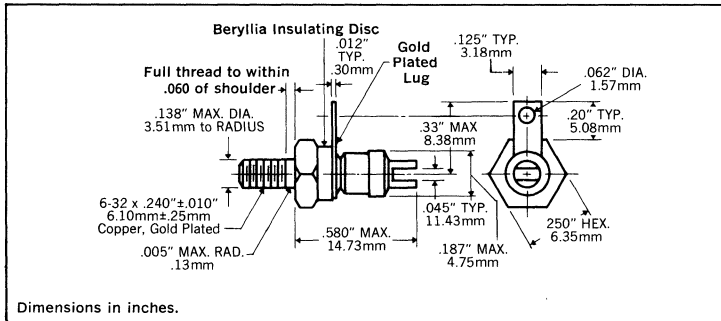
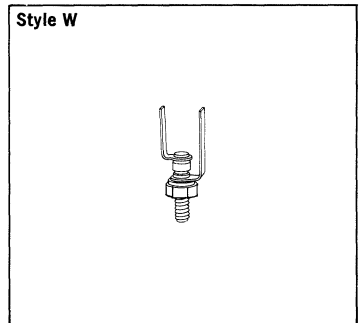
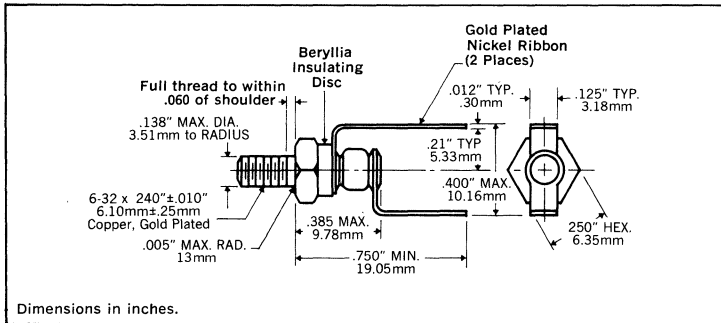
Body	Material	Usage	Lead				Suffix Letter	Typical Weight Body Plus Leads (mg)
			Length		Dia			
			ins	mm	ins	mm		
.030	Silver plated Copper	Solderable	1.0	25.4	.020	.51	None	—
	Silver plated dumet	Solderable or weldable	1.0	25.4	.014	.36	*	—
A .045	Silver plated Copper	Solderable	1.0	25.4	.028	.71	H	260
	Silver	Solderable	0.7	1.24	.028	.71	M	215
	Copper, tinned (standard)	Solderable or weldable	1.0	25.4	.028	.71	None	260
B .090 and C .125	Silver plated Copper	Solderable	1.0	25.4	.040	1.02	J	740
	Silver	Solderable	1.0	25.4	.040	1.02	P	740
	Copper, tinned (standard)	Solderable or weldable	1.0	25.4	.040	1.02	None	740

* Available on 1N5767 and 1N5957 only.

INSULATED STUD PACKAGES

Unitrode's three stud-mounted devices, 10W high-surge zener diodes, 12A standard recovery rectifiers, and 9A fast-recovery rectifiers, are also available as shown here with insulated studs having the same high ratings as the standard non-insulated devices.

MECHANICAL SPECIFICATIONS



Part Identification: Style W: Part number printed on ribbon lead. Style V: Part number printed on body. Numerals are unique and indicate 10W Zener Series (UZ), 12A rectifier series (UT), or 9A fast-recovery rectifier series (UTR).

Polarity: Cathode to stud end.

Max. Weight: Styles W & V: 2.3 grams.

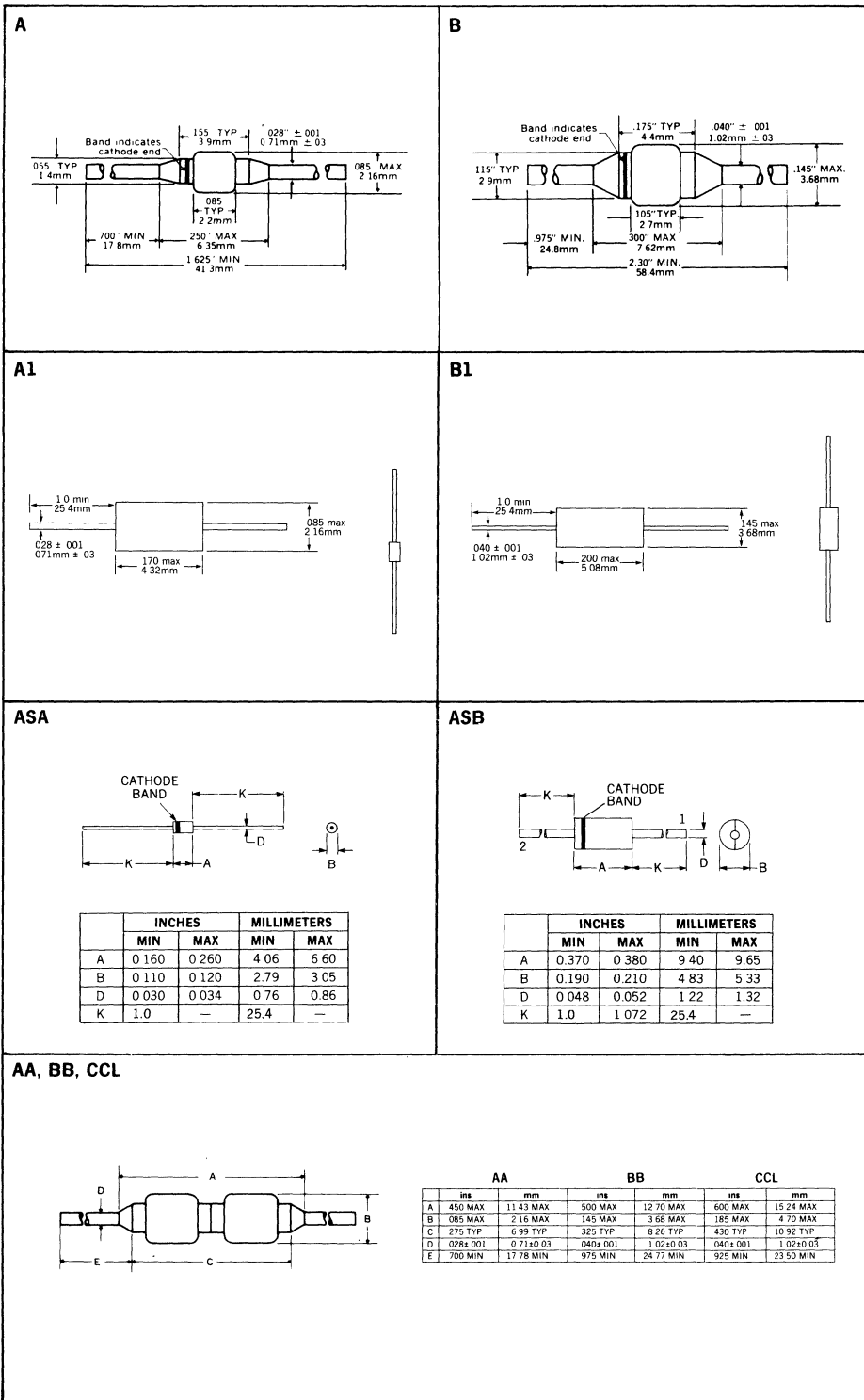
Installation Precautions: Maximum unlubricated stud torque: 36 inch-ounces.

Note: Do not use a screwdriver in turret slot for installation purposes, or damage may result.

ORDERING INFORMATION

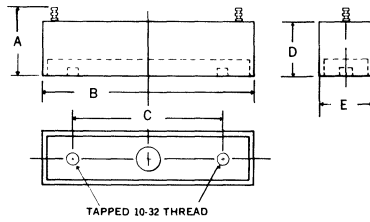
The type numbers that apply to the standard studs also apply to the insulated studs with the addition of suffix W or V for style W or V (see outline drawings). For example, to specify insulated stud style W for a 6.8V zener, order UZ7806W; for a 50V 12A rectifier, order UT8105W; and for a 100V 9A fast-recovery rectifier, order UTR6410W.

MECHANICAL SPECIFICATIONS



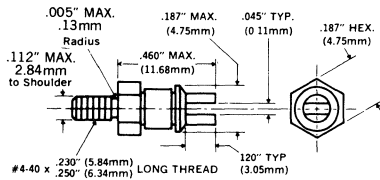
MECHANICAL SPECIFICATIONS

BE

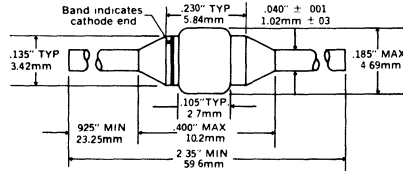


	ins.	mm.
A	1.140 MAX.	28.96 MAX.
B	2.985-3.015	75.82-76.58
C	2.110-2.140	53.59-54.36
D	.740-.770	18.80-19.56
E	.720-.750	18.29-19.05

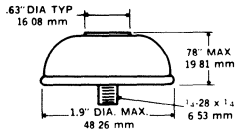
C



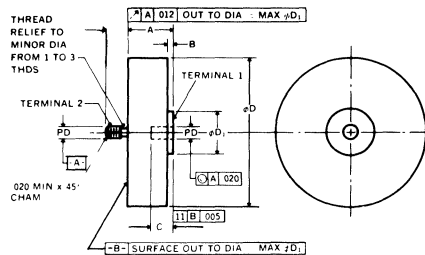
CL



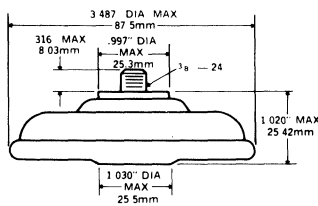
DD



DE, DF



DG



DE

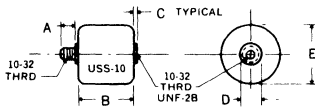
Ltr	Dimensions in inches with metric equivalents (mm) in parentheses		NOTES
	Minimum	Maximum	
A	.73 (18.54)	.83 (21.08)	8
B		.080 (2.03)	
C	.240 (6.10)	.264 (6.71)	2, 6
C ₁	.265 (6.73)	.400 (10.16)	4
øD	1.85 (46.99)	1.95 (49.53)	
øD ₁	.57 (14.48)	.67 (17.02)	

DF

Ltr	Dimensions in inches with metric equivalents (mm) in parentheses		NOTES
	Minimum	Maximum	
A	.970 (24.64)	1.020 (25.91)	8
B	.650 (16.27)	.680 (17.28)	
C	.307 (7.80)	.317 (8.05)	3
C ₁	.318 (8.08)	.400 (10.16)	5, 7
øD	3.450 (87.63)	3.650 (92.71)	
øD ₁	.95 (24.13)	1.250 (31.75)	

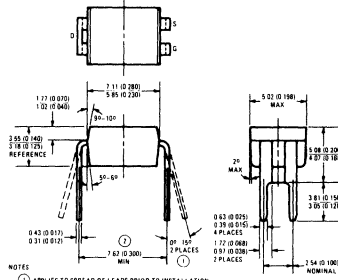
MECHANICAL SPECIFICATIONS

DH



	ins.	mm.
A	.230-.235	5.84-5.97
B	.980-1.10	24.89-27.94
C	.020-.040	0.51-1.02
D	.320-.330	8.13-8.38
E	.97-1.00	24.64-25.40

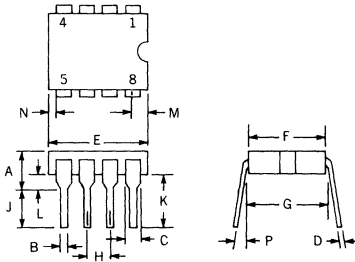
DIL-4



NOTES
 ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
 ② APPLIES TO INSTALLED LEAD CENTERS

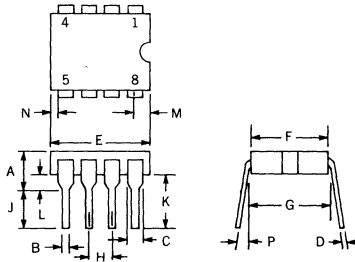
Nominal Dimensions in Millimeters and (Inches)

DIL-8 J



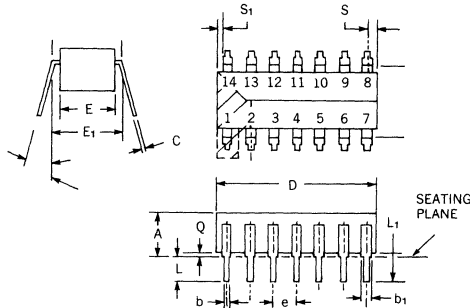
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	.200	—	5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.015	0.20	0.38
E	—	.390	—	9.91
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150	—	3.81	—
L	.015	.060	0.38	1.52
M	—	.045	—	1.14
N	.005	—	0.13	—
P	0°	15°	0°	15°

DIL-8 N



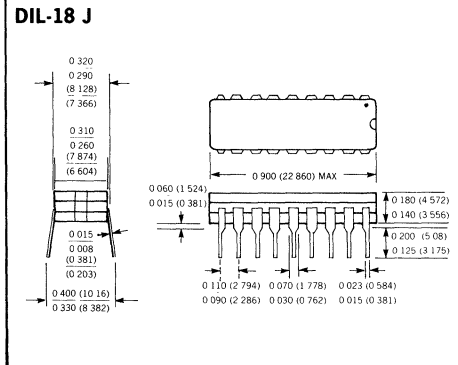
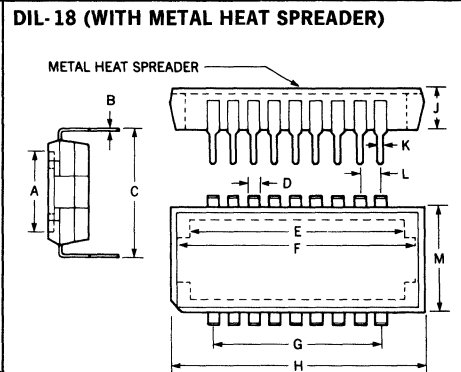
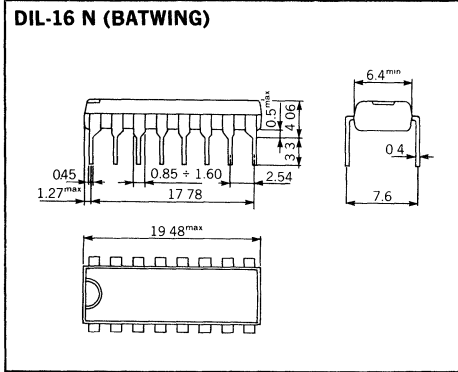
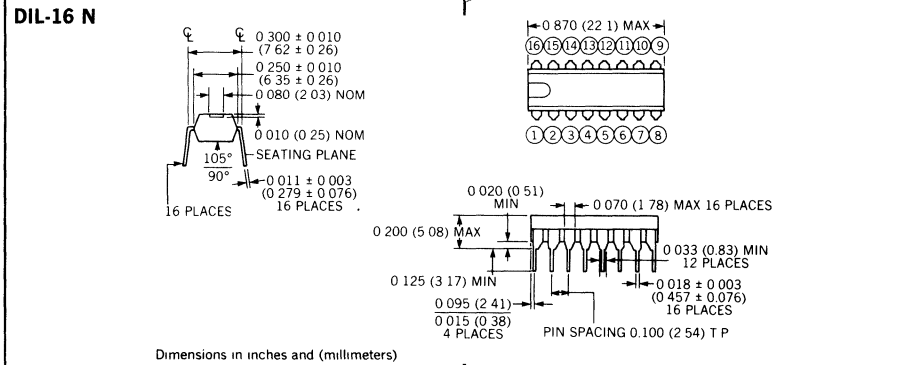
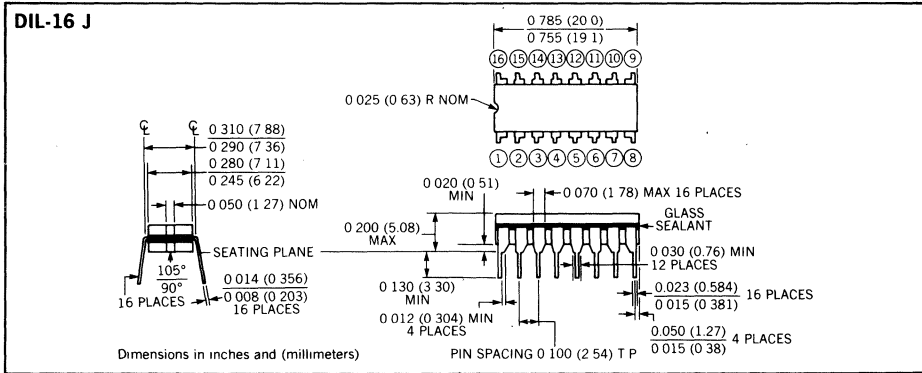
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.115	.125	2.92	3.17
B	.015	.021	0.38	0.53
C	.030	.070	0.76	1.78
D	.010	.015	0.25	0.38
E	.360	.400	9.14	10.16
F	.240	.260	6.09	6.60
G	.290	.310	7.37	7.87
H	.090	.110	2.29	2.79
J	.120	.135	3.05	3.43
K	.140	.165	3.56	4.18
L	.020	.030	0.51	0.75
M	.025	.050	0.64	1.27
N	.005	—	0.13	—
P	0°	15°	0°	15°

DIL-14 N



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	.200	—	5.08	—
b	.014	.023	0.36	0.58	8
b ₁	.030	.070	0.76	1.78	2, 8
c	.008	.015	0.20	0.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
E ₁	.290	.320	7.37	8.13	7
E ₂	.100	—	2.54	—	—
E ₃	.050	—	1.27	—	—
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	—
L ₁	.150	—	3.81	—	—
Q	.015	.060	0.38	1.52	3
Q ₁	.020	—	0.51	—	—
S	—	.098	—	2.49	6
S ₁	.005	—	0.13	—	6
S ₂	.005	—	0.13	—	—

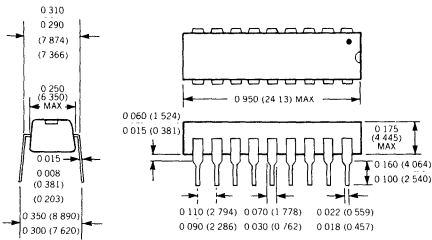
MECHANICAL SPECIFICATIONS



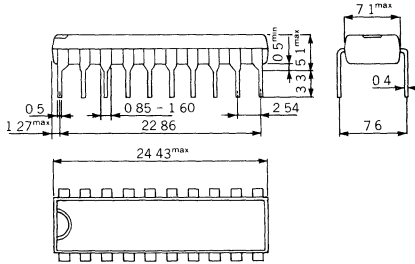
	INCHES	MILLIMETERS
A	.400	10.16
B	.020	0.51
C	.600 TYP.	15.24 TYP.
D	.064	1.63
E	1.00	25.40
F	1.10	27.94
G	.800	20.32
H	1.180 MAX.	29.97 MAX.
J	1.180 MAX.	4.57 MAX.
K	.021	.533
L	.100 TYP.	2.54 TYP.
M	.550	13.97

MECHANICAL SPECIFICATIONS

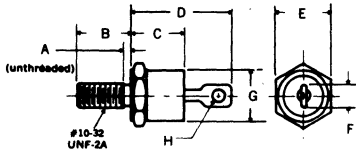
DIL-18 N



DIL-20 N

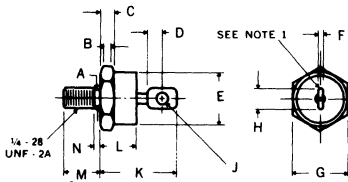


DO-4



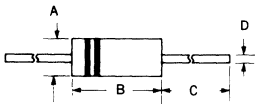
	ins.	mm.
A	.078 MAX.	1.98 MAX.
B	.437±.015	11.10±0.38
C	.405 MAX.	10.29 MAX.
D	.800 MAX.	20.32 MAX.
E	.430±.010	10.92±0.25
F	.250 MAX.	6.35 MAX.
G	.424 MAX.	10.77 MAX.
H	.066 MIN. DIA.	1.68 MIN. DIA.

DO-5



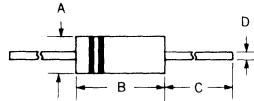
	ins.	mm.
A	.225±.005	5.72±0.13
B	.060 MIN. DIA.	1.52 MIN. DIA.
C	.156±.020	3.96±0.51
D	.156 MIN. FLAT	3.96 MIN. FLAT
E	.667 DIA. MAX.	16.94 DIA. MAX.
F	.090 MAX.	2.29 MAX.
G	.667±.010	17.20±0.25
H	.375 MAX.	9.53 MAX.
J	.140 MIN. DIA.	3.56 MIN. DIA.
K	1.000 MAX.	25.40 MAX.
L	.450 MAX.	11.43 MAX.
M	.438±.015	11.13±0.38
N	.078 MAX.	1.98 MAX.

DO-7



	ins.	mm.
A	.078-1.07	1.98-2.72
B	.195-300	4.95-7.62
C	1.0 MIN.	25.40 MIN.
D	.018-.022	0.46-0.56

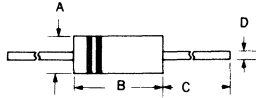
DO-34



	INCHES	MILLIMETERS
A	.050 - .065	1.27 - 1.65
B	.080 - .120	2.03 - 3.05
C	1.0 - 1.5	25.4 - 38.1
D	.018 - .022	.46 - .56

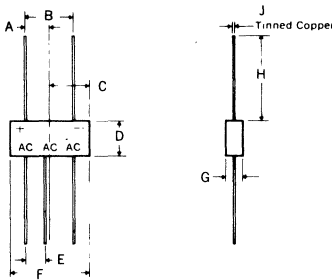
MECHANICAL SPECIFICATIONS

DO-35



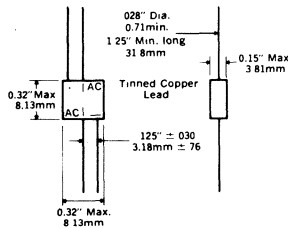
	ins.	mm.
A	.056-.075	1.42-1.91
B	.140-.180	3.56-4.57
C	1.0 MIN.	25.40 MIN.
D	.018-.022	0.46-0.56

F

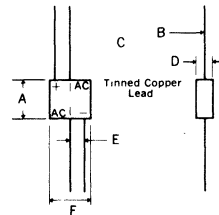


	ins.	mm.
A	.310	7.87
B	.621	15.77
C	.512 REF.	13.0 REF.
D	.460 MAX.	11.68 MAX.
E	.255	6.48
F	1.030 MAX.	26.16 MAX.
G	.220 MAX.	5.59 MAX.
H	.875	22.23
J	.028 DIA.	0.71 DIA.

G

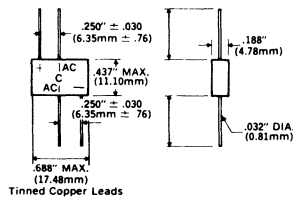


GA

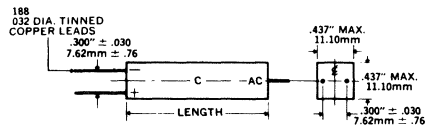


	ins.	mm.
A	0.50 ± 0.1	12.70 ± 2.5
B	.032 DIA	0.81 DIA
C	1.0 MIN	25.4 MIN
D	250 MAX	6.35 MAX
E	150 TYP	3.81 TYP
F	0.50 ± 0.1	12.70 ± 2.5

GH



HJ, HK, HL, HM, HN, HO, HP

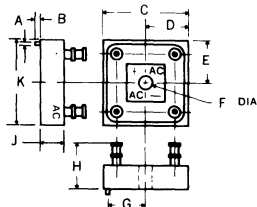


MAX. LENGTHS

J	K	L	M	N	O	P
.562"	.688"	.875"	1.125"	1.25"	1.375"	1.625"
14.27mm	17.48mm	22.23mm	28.58mm	31.75mm	34.92mm	41.28mm

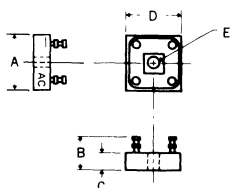
MECHANICAL SPECIFICATIONS

MA



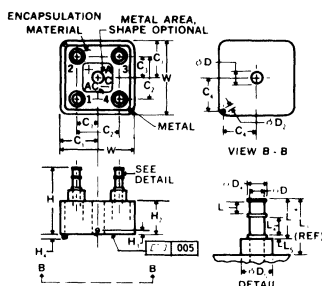
	ins.	mm.
A	.056-.066	1.42-1.68
B	.052-.072	1.32-1.83
C	1.115-1.135	28.32-28.83
D	.552-.572	14.02-14.53
E	.552-.572	14.02-14.53
F	180-200 DIA	4.57-5.08 DIA
G	.490-.510	12.45-12.95
H	.750 MAX.	19.05 MAX
J	.302-.322	7.67-8.18
K	1.115-1.135	28.32-28.83

MB



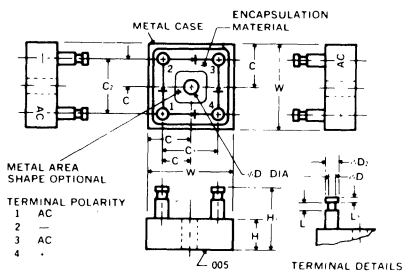
	ins.	mm.
A	.735-.755	18.67-19.18
B	.570 MAX.	14.48 MAX.
C	.226-.246	5.74-6.25
D	.735-.755	18.67-19.18
E	.130-.150 DIA.	3.30-3.81

MC



Ltr	Dimensions			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
C ₁	.552	.572	14.02	14.53
C ₂	.624	.760	15.85	19.30
C ₃	.312	.380	7.92	9.65
C ₄	.495	.512	12.57	13.00
φD	.189	.195	4.80	4.95
φD ₂	.057	.067	1.45	1.70
φD ₁	.108	.118	2.74	3.00
φD ₄	.141	.151	3.58	3.84
φD ₅	.225	.235	5.72	5.97
H	.669	1.060	17.53	26.92
H ₂	.300	.500	7.62	12.70
H ₁	.040	.060	1.02	1.52
H ₄	.042	.062	1.07	1.57
L	.370	.560	9.40	14.22
L ₂	.307	.365	7.80	9.27
L ₁	.089	.099	2.26	2.49
L ₄	.132	.142	3.35	3.61
L ₅	.026	.036	.66	.91
W	1.104	1.144	28.04	29.06

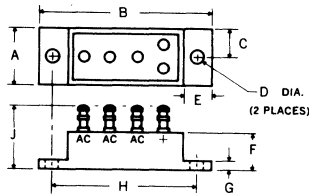
MD



Ltr	Dimensions			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
C ₁	.367	.375	9.32	9.53
C ₂	.350	.450	8.89	11.43
C ₃	.175	.225	4.45	5.72
φD	.139	.149	3.53	3.78
φD ₂	.091	.101	2.31	2.57
φD ₁	.066	.076	1.68	1.93
H ₁		.570		14.48
H ₂		.370		9.40
L ₁	.088	.098	2.24	2.49
L ₂	.020	.030	.51	.76
W	.735	.750	18.67	19.05

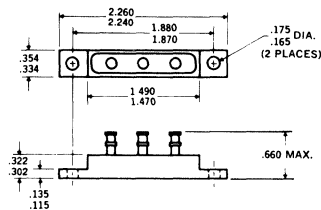
MECHANICAL SPECIFICATIONS

ME

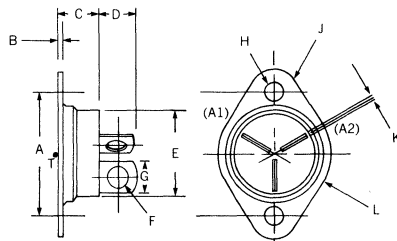


	ins.	mm.
A	.740-.760	18.80-19.30
B	2.240-2.260	56.90-57.40
C	.365-.385	9.27-9.78
D	.164-.174 DIA.	4.17-4.42 DIA.
E	.370-.390	9.40-9.91
F	.486-.506	12.34-12.85
G	.115-.135	2.92-3.43
H	1.870-1.880	47.50-47.75
J	.820 MAX.	20.83 MAX.

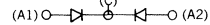
MF



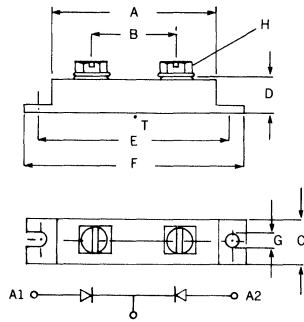
M1



TERMINAL (C)
ELECTRICALLY COMMON
TO BASE PLATE



M2

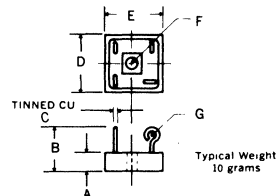


C (ELECTRICALLY COMMON
TO BASE PLATE)

Terminal Torque: 50 (Min.) 75 (Max.) lb. — in.
Mounting Base Torque: 30 (Min.) 40 (Max.) lb. — in.

	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A		2.63		66.80
B	1.35	1.40	34.29	35.56
C	.70	.80	17.78	20.32
D		.625		15.88
E	3.14	3.16	79.76	80.26
F		3.65		92.71
G	.25	.27	6.35	6.86
H	1/4 — 20 UNF With Captive Lockwasher			
T	Top Ref. Point - Geometric Center of Base Plate			

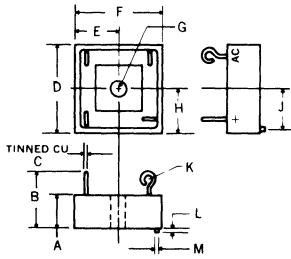
NA



	ins.	mm.
A	240 MAX.	61.0 MAX.
B	57 MAX.	14.45 MAX.
C	040 TYP.	1.02 TYP.
D	750 MAX.	19.05 MAX.
E	750 MAX.	19.05 MAX.
F	140 DIA.	3.56 DIA.
G	09 DIA TYP.	2.29 DIA TYP.

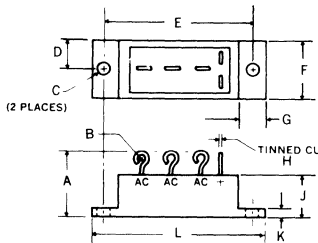
MECHANICAL SPECIFICATIONS

NB



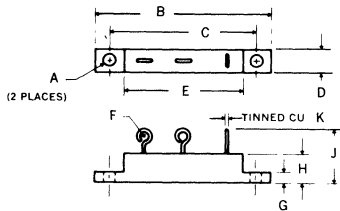
	ins.	mm.
A	.328 MAX.	8.33 MAX.
B	.750 MAX.	19.05 MAX.
C	.040 TYP.	1.02 TYP.
D	1.125 MAX.	28.58 MAX.
E	.562	14.27
F	1.125 MAX.	28.58 MAX.
G	.193	4.90
H	.562	14.27
J	.500	12.70
K	.09 DIA. TYP.	2.29 DIA. TYP.
L	.062	1.57
M	.062	1.57

NC



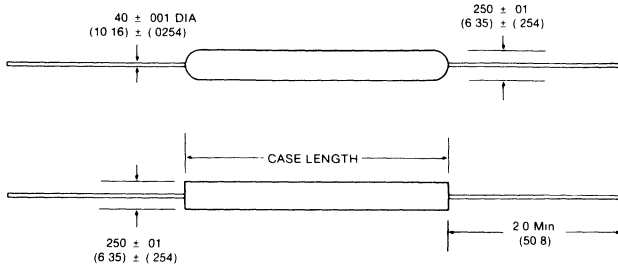
	ins.	mm.
A	.820 MAX.	20.83 MAX.
B	.09 DIA. TYP.	2.29 DIA. TYP.
C	.164-.174 DIA.	4.17-4.42 DIA.
D	.365-.385	9.27-9.78
E	1.870-1.880	47.50-47.75
F	.740-.760	18.80-19.30
G	.370-.390	9.40-9.91
H	.040 TYP.	1.02 TYP.
J	.486-.506	12.34-12.85
K	.115-.135	2.92-3.43
L	2.240-2.260	56.90-57.40

ND



	ins.	mm.
A	.165-.175 DIA.	4.19-4.45 DIA.
B	2.240-2.260	56.90-57.40
C	1.870-1.880	47.50-47.75
D	.334-.354	8.48-8.99
E	1.480-1.490	37.59-37.85
F	.09 DIA. TYP.	2.29 DIA. TYP.
G	.115-.135	2.29-3.43
H	.302-.322	7.67-8.18
J	.660 MAX.	16.76 MAX.
K	.040 TYP.	1.02 TYP.

PA

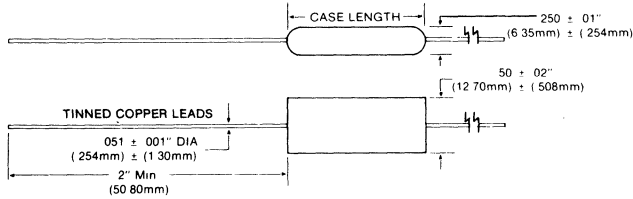


CASE LENGTH	
ins.	MM
1.5 ± .02	38.1 ± .508
2.0 ± .02	50.8 ± .508
2.5 ± .02	63.5 ± .508
3.0 ± .02	76.2 ± .508
3.5 ± .02	88.9 ± .508

Dimensions in inches and (millimeters)

MECHANICAL SPECIFICATIONS

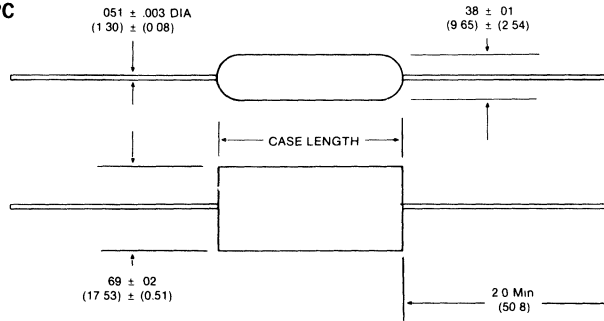
PB



CASE LENGTH		
Ins.	MM	
1.125 ± .02	28.58 ± .508	
1.625 ± .02	41.28 ± .508	
2.000 ± .02	50.80 ± .508	
2.375 ± .02	60.33 ± .508	
2.750 ± .02	69.80 ± .508	
3.500 ± .02	88.90 ± .508	
4.250 ± .02	107.95 ± .508	

Dimensions in inches and (millimeters)

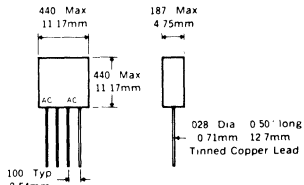
PC



CASE LENGTH		
Ins.	MM	
1.5 ± .03	38.10 ± 0.76	
2.5 ± .03	63.50 ± 0.76	
3.5 ± .03	88.90 ± 0.76	
4.5 ± .03	114.30 ± 0.76	
5.5 ± .03	139.70 ± 0.76	
6.5 ± .03	165.10 ± 0.76	

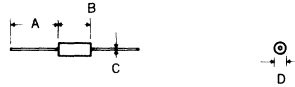
Dimensions in inches and (millimeters)

S



Dimensions in inches and millimeters

SA



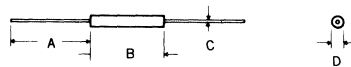
	ins.	mm.
A	.75 MIN.	19.05 MIN.
B	.50 MAX.	12.70 MAX.
C	.028 DIA.	.71 DIA.
D	.187 MAX.	4.75 MAX.

SB



	ins.	mm.
A	1.25 MIN.	31.75 MIN.
B	0.85 MAX.	21.59 MAX.
C	.032 DIA.	.81 DIA.
D	.187 MAX.	4.75 MAX.

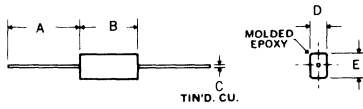
SC



	ins.	mm.
A	1.25 MIN.	31.75 MIN.
B	1.125 MAX.	28.58 MAX.
C	.032 DIA.	.81 DIA.
D	.187 MAX.	4.75 MAX.

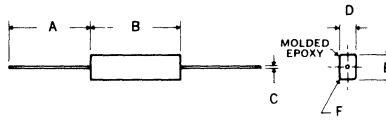
MECHANICAL SPECIFICATIONS

SD



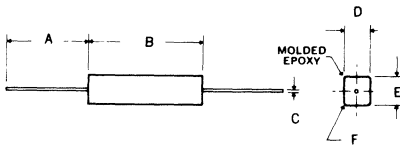
	ins.	mm.
A	1.25 MIN.	31.75 MIN.
B	.875 MAX.	22.23 MAX.
C	.032 DIA.	.81 DIA.
D	.250 MAX.	6.35 MAX.
E	.375 MAX.	9.53 MAX.

SE



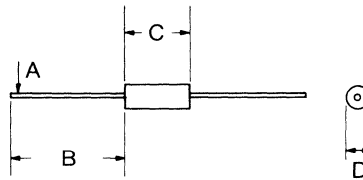
	ins.	mm.
A	1.25 MIN.	31.75 MIN.
B	1.375 MAX.	34.93 MAX.
C	.032 DIA.	.81 DIA.
D	.250 MAX.	6.35 MAX.
E	.375 MAX.	9.53 MAX.
F	.078	1.98

SF



	ins.	mm.
A	1.25 MIN.	31.75 MIN.
B	1.75 MAX.	44.45 MAX.
C	.032 DIA.	.81 DIA.
D	.400 MAX.	10.16 MAX.
E	.400 MAX.	10.16 MAX.
F	.078	1.98 MAX.

SJ, SK, SL, SM, SN

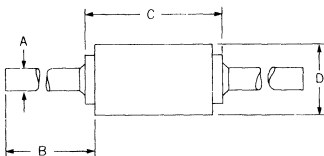


Dimensions in inches and (millimeters)

	SJ		SK	
	ins.	MM	ins.	MM
A	0.31 ± .002	0.79 ± 0.05	0.31 ± .002	0.79 ± 0.05
B	1.12	28.4	1.12	28.4
C	0.410 ± .005	10.41 ± 0.13	0.200 ± .005	5.08 ± 0.13
D	0.140 ± .005	3.57 ± 0.13	0.100 ± .005	2.54 ± 0.13

	SL		SM		SN	
	ins.	MM	ins.	MM	ins.	MM
A	0.040 ± .003	1.016 ± 0.076	0.093 ± .003	2.36 ± 0.076	0.020 ± .001	0.51 ± 0.03
B	.40	10.16	.40	10.16	.60	15.24
C	0.400 ± .015	10.16 ± .381	0.375 ± .015	9.52 ± .381	1.500 ± .015	38.1 ± .381
D	0.300 ± .015	7.62 ± .381	0.500 ± .015	12.7 ± .381	0.235 ± .005	5.97 ± 0.13

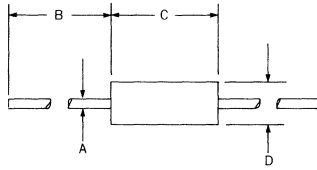
TG



	INCHES	MILLIMETERS
A	0.020 ± .002	508 ± .051
B	1.0 MIN	25.4 MIN
C	2.85 ± .015	7.239 ± .381
D	0.095 ± .01	2.413 ± .254

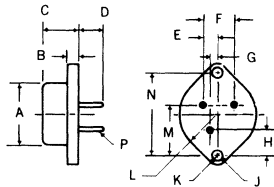
MECHANICAL SPECIFICATIONS

TM



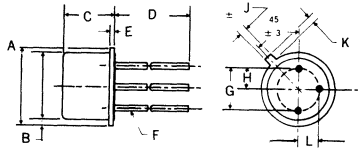
	INCHES	MILLIMETERS
A	025 ± 003	635 ± 076
B	1 0 MIN	25 4 MIN
C	405 ± 015	10 287 ± 381
D	14 ± 015	3 556 ± 381

TO-3 (3 PIN) (See TO-204AA for 2 PIN TO-3)



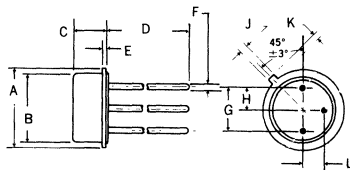
	ins.	mm.
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	250-450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.205-.225	5.21-5.72
F	.420-.440	10.67-11.18
G	.145-.165	3.68-4.19
H	.395-.405	10.03-10.29
J	.151-.161 DIA.	3.84-4.09 DIA.
K	.188 MAX. RAD.	4.78 MAX. RAD.
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.708-.728	17.98-18.49
N	1.177-1.197	29.90-30.40
P	.038-.043 DIA.	0.97-1.09 DIA.

TO-5



	ins.	mm.
A	.335-.370	8.51-9.40
B	.305-.335	7.75-8.51
C	.240-.260	6.09-6.60
D	1.5 MIN.	38.10 MIN.
E	.010-.030	.254-.762
F	.017 ± $\frac{.002}{.001}$.432 ± $\frac{.051}{.025}$
G	.200	5.08
H	.100	2.54
J	.028-.034	.711-.864
K	.029-.045	.736-1.14
L	.100	2.54

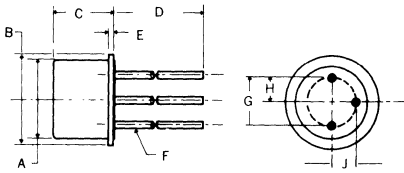
TO-5 Pancake



	ins.	mm.
A	.335-.370	8.51-9.40
B	.305-.335	7.75-8.51
C	.165-.185	4.19-4.70
D	1.5 MIN.	38.10 MIN.
E	.010-.030	.254-.762
F	.017 ± $\frac{.002}{.001}$.432 ± $\frac{.051}{.025}$
G	.200	5.08
H	.100	2.54
J	.028-.034	.711-.864
K	.029-.045	.736-1.14
L	.100	2.54

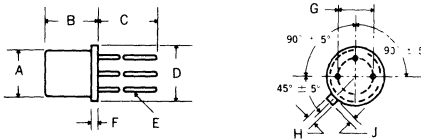
MECHANICAL SPECIFICATIONS

TO-9



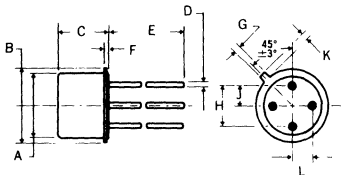
	ins.	mm
A	275-335	6.99-7.75
B	290-370	7.37-9.40
C	200-260	5.08-6.60
D	1.5 MIN.	38.10 MIN.
E	.010-.030	.25-76
F	.017 ± .002 .001	432 ± .051 .025
G	200	5.08
H	100	2.54
J	100	2.54

TO-18



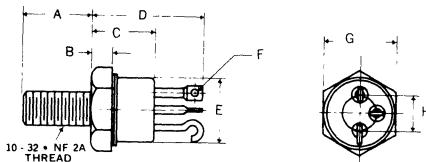
	INCHES	MILLIMETERS
A	.178-.195 DIA.	4.52-4.95 DIA.
B	.170-.210	4.31-5.33
C	.5 MIN.	12.70 MIN.
D	.209-.230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 .001 DIA.	432 ± .051 .025
F	.020 MAX.	.508 MAX.
G	.100 ± .010 DIA.	2.54 ± .254 DIA.
H	.041 ± .005	1.04 ± .127
J	.028-.048	.711-1.22

TO-33



	ins.	mm
A	305-335	7.75-8.51
B	.335-.370	8.51-9.40
C	.240-.260	6.10-6.60
D	.017 ± .002 .001	0.43 ± .05 .03
E	1.5 MIN.	38.10 MIN.
F	.018 MAX.	0.46 MAX.
G	.031 ± .003	0.79 ± .08
H	200	1.02
J	.100	2.54
K	.029-.045	0.74-1.14
L	.100	2.54

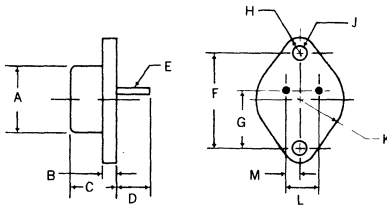
TO-59



	INCHES	MILLIMETERS
A	.400-.455	10.16-11.56
B	.090-.150	2.28-3.81
C	.320-.468	8.13-11.88
D	.570-.763	14.48-19.38
E	.318-.380	8.07-9.65
F	.055 ± .010 .015	1.40 ± .254 .381
G	.424-.437	10.77-11.10
H	.185-.215	4.70-5.46

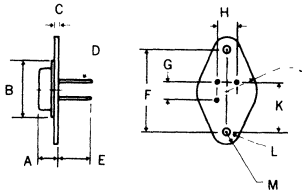
MECHANICAL SPECIFICATIONS

TO-66



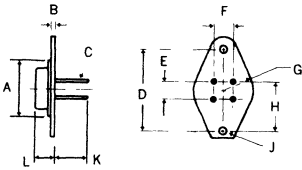
	ins.	mm.
A	.620 MAX.	15.75 MAX.
B	.050-.075	1.27-1.90
C	.250-.340	6.35-8.63
D	.360 MIN.	9.14 MIN.
E	.028-.034 DIA.	.711-0.863
F	.958-.962	24.33-24.43
G	.570-.590	14.47-14.98
H	.145 MAX. RAD.	3.68 MAX. RAD.
J	.142-.152 DIA.	3.60-.386 DIA.
K	.350 MAX. RAD.	8.89 MAX. RAD.
L	.190-.210	4.82-5.33
M	.093-.107	2.36-2.72

TO-66 (3 PIN)



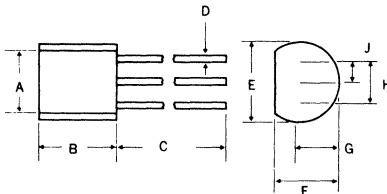
	ins.	mm.
A	.250-.340	6.35-8.64
B	.620 MAX.	15.75 MAX.
C	.050-.075	1.27-1.91
D	.028-.034	0.71-0.86
E	.360 MIN.	9.14 MIN.
F	.958-.962	24.33-24.43
G	.190-.210	4.83-5.33
H	.190-.210	4.83-5.33
J	.350 MAX. RAD.	8.89 MAX. RAD.
K	.570-.590	14.48-14.99
L	.142-.152	3.61-3.86
M	.145 MAX. RAD.	3.68 MAX. RAD.

TO-66 (4 PIN)



	ins.	mm.
A	.620 MAX.	15.75 MAX.
B	.050-.075	1.27-1.91
C	.028-.034	0.71-0.86
D	.958-.962	24.33-24.43
E	.190-.210	4.82-5.33
F	.190-.210	4.82-5.33
G	.350 MAX. RAD.	8.89 MAX. RAD.
H	.570-.590	14.48-14.99
J	.142-.152 DIA.	3.61-3.86 DIA.
K	.360 MIN.	9.14 MIN.
L	.250-.340	6.35-8.64

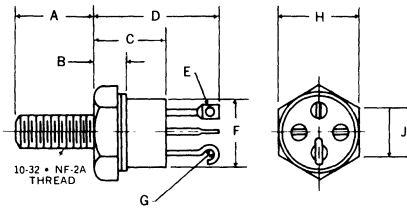
TO-92



	ins.	mm.
A	.135 MIN.	3.42 MIN.
B	.170-.210	4.31-5.33
C	.500 MIN.	12.70 MIN.
D	.016-.019	.406-.482
E	.175-.205	4.44-5.21
F	.125-.165	3.17-4.19
G	.080-.105	2.03-2.66
H	.095-.105	2.41-2.66
J	.045-.055	1.14-1.40

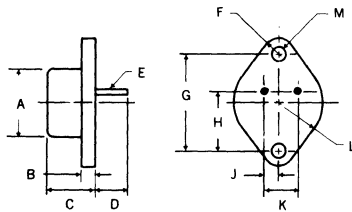
MECHANICAL SPECIFICATIONS

TO-111



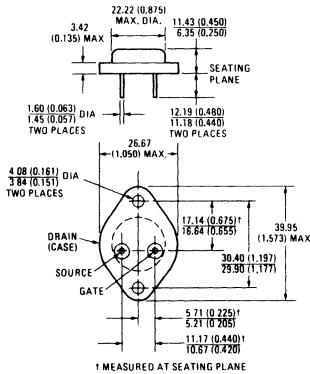
	ins.	mm.
A	.400-.455	10.16-11.55
B	.090-.250	2.28-6.35
C	.320-.468	8.13-11.88
D	.570-.763	14.48-19.38
E	.065-.090	1.65-2.28
F	.313-.318	7.95-8.07
G	.070-.090	1.77-2.28
H	.423-.438	10.74-11.12
J	.135-.215	3.43-5.46

TO-204AA (TO-3)

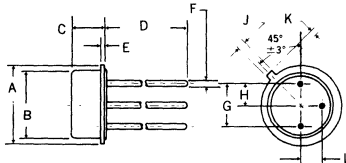


	ins.	mm.
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA. *	0.97-1.09 DIA. *
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AE (TO-3 MODIFIED)



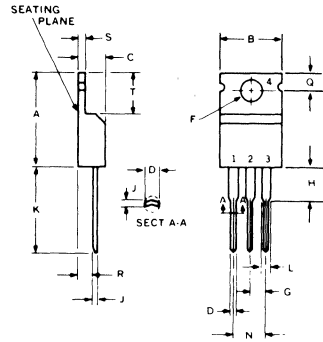
TO-205AD (TO-39)



	ins.	mm.
A	.350-.370	8.89-9.39
B	.315-.335	8.00-8.51
C	.240-.260	6.35-6.60
D	.010-.030	.25-.76
E	.5 MIN.	12.70 MIN.
F	.017 ± .002 .001	.432 ± .051 .025
G	.200	5.08
H	.100	2.54
J	.031 ± .003	.79 ± .08
K	.029-.045	.74-1.14
L	.100	2.54

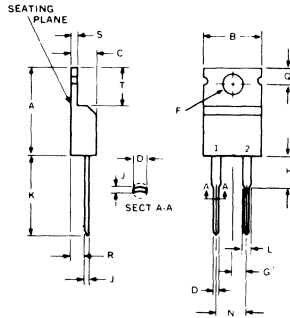
MECHANICAL SPECIFICATIONS

TO-220AB



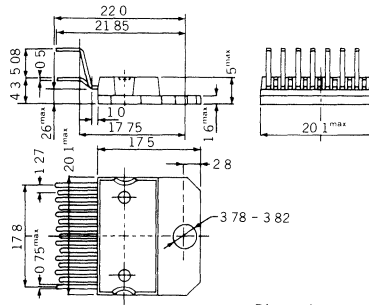
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

TO-220AC



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	—	6.35	—	0.250
J	0.38	0.64	0.015	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

V (15 PIN SIP)



Dimensions in millimeters

UNITRODE REGIONAL OFFICES

Eastern Area Office, Door 8 — Lakeside Office Park, North Avenue, Wakefield, MA 01880, Tel. (617) 245-3010, TWX 710-348-1733
Metropolitan New York Office, 150 Broadhollow Road, Suite 210A, Melville, NY 11747, Tel. (516) 271-3110, 11, TWX 510-226-6997
Southeast Office, 8001 North Dale Mabry Highway, Suite 801D, Tampa, FL 33614, Tel. (813) 932-5807, TWX 810-876-0886
Mid-America Area Office, 121 South Wilke Road, Suite 103, Arlington Heights, IL 60005, Tel. (312) 394-5240, TWX 910-233-0168
South Central Office, 13999 Goldmark, Suite 460, Dallas, TX 75240, Tel. (214) 231-8700, TWX 910-867-4738
North Central Office, 3131 S. Dixie Drive, Suite 507, Dayton, OH 45439, Tel. (513) 294-1364, TWX 810-450-2645
Western Area Office, 5530 Corbin Avenue, Suite 328, Tarzana, CA 91356, Tel. (818) 705-8085, TWX 910-494-5964
Southwest Office, 15011 Parkway Loop, Suite F, Tustin, CA 92680, Tel. (714) 730-1077, TWX 910-595-1999
Northwest Office, 2444 Moorpark Avenue, Suite 314, San Jose, CA 95128, Tel. (408) 294-4210, TWX 910-338-0126

DOMESTIC REPRESENTATIVES

ALABAMA

Conley & Associates, Inc.
 Huntsville
 205-882-0316

ARIZONA

Compass Mktg. & Sales, Inc.
 Phoenix
 602-266-5400

ARKANSAS

See Texas

CALIFORNIA — NORTHERN

I² Inc.
 Santa Clara
 408-988-3400

CALIFORNIA — SOUTHERN

Centaur Corp.
 Irvine
 714-261-2123

Centaur Corp.
 San Diego
 619-571-7871

Centaur Corp.
 Woodland Hills
 818-704-1655

COLORADO

Component Sales, Inc.
 Denver
 303-759-1666

CONNECTICUT

Kanan Associates
 Yalesville
 203-265-2404

DELAWARE

See Pennsylvania-Eastern

DISTRICT OF COLUMBIA

See Maryland

FLORIDA

Conley & Associates, Inc.
 Oviedo
 305-365-3283

Conley & Associates, Inc.
 Boca Raton
 305-395-6108

Conley & Associates, Inc.
 Tampa
 813-885-7658

GEORGIA

Conley & Associates, Inc.
 Doraville
 404-447-6992

IDAHO

See Washington

ILLINOIS — NORTHERN

Oasis Sales Corp.
 Elk Grove Village
 312-640-1850

ILLINOIS — SOUTHERN

See Missouri

INDIANA

Shamrock Associates
 Carmel
 317-848-5265

IOWA

See Minnesota

KANSAS

Rush & West Associates
 Olathe
 913-764-2700

KENTUCKY

See Ohio

LOUISIANA

See Texas

MAINE

See Massachusetts

MARYLAND

New Era Sales, Inc.
 Severna Park
 301-544-4100

MASSACHUSETTS

Kanan Associates
 Reading
 617-944-8484

Byrne Associates, (DEC only)
 Maynard
 617-897-3131

MICHIGAN

Miltimore Sales, Inc.
 Novi
 313-349-0260

Miltimore Sales, Inc.
 Grand Rapids
 616-942-9721

MINNESOTA

Aldridge Associates
 Eden Prairie
 612-944-8433

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