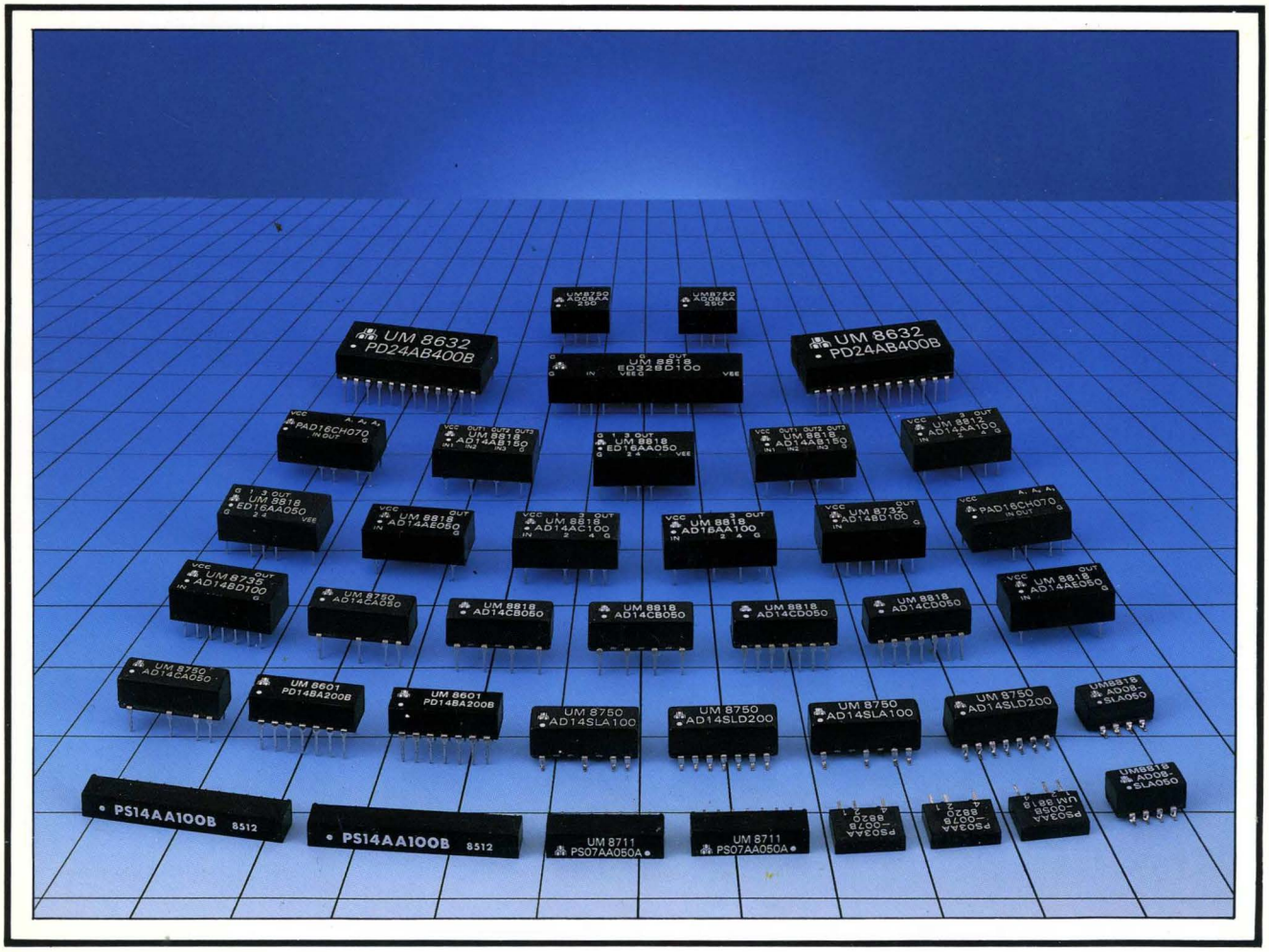
UNIVERSAL
MICROELECTRONICS

DELAY LINES



DELAY LINE

1. ACTIVE DELAY LINES:

MEASURING TECHNIQUES OF ACTIVE DELAY LINE. 1

(1) TTL COMPATIBLE

(2) ECL COMPATIBLE

(3) PROGRAMMABLE DELAY LINES

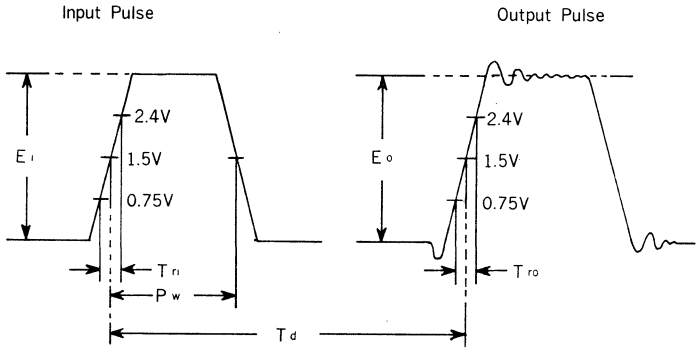
(4) SURFACE MOUNTING DELAY LINES

2. PASSIVE DELAY LINES:

MEASURING TECHNIQUES OF PASSIVE DELAY LINE. 18

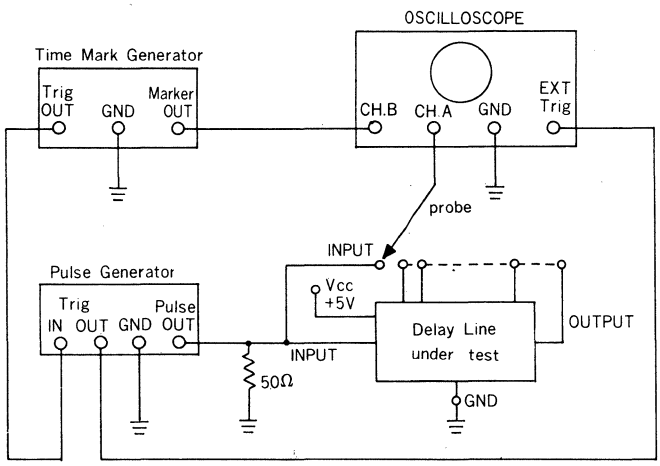
MEASURING TECHNIQUES OF ACTIVE DELAY LINE.

● WAVEFORM AND PARAMETER DEFINITIONS

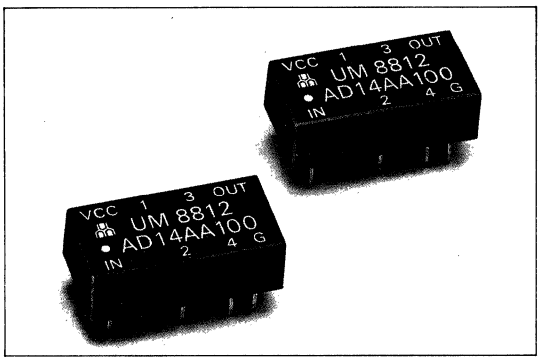


E_i — Input Pulse Voltage
E_o — Output Pulse Voltage
T_d — Delay Time Between The 1.5 V Level of The Leading Edges
T_{ri} — Input Rise Time
T_{ro} — Output Rise Time
P_w — Pulse Width of Input Pulse

● TEST CIRCUIT



AD14AA SERIES: 14-PIN DIL 5-TAP EQUALLY-SPACED



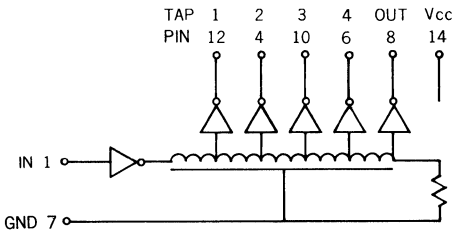
FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Fits in Standard 14-pin DIL
- Operating Temperature Range: 0℃ to +70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: –2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

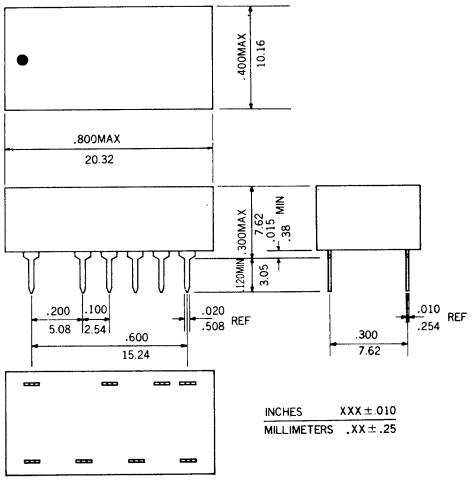
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

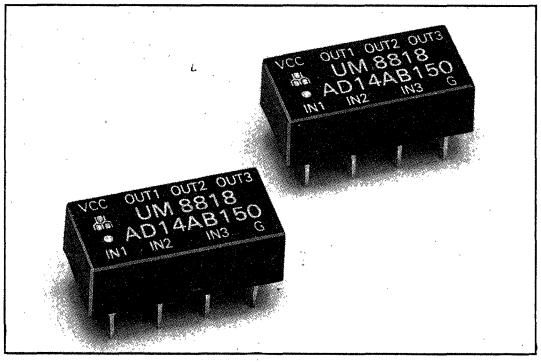
Pulse Voltage: 3.2V
Rise Time: 3.0ns
Supply Current: 60mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD14AA025	25±2	5±2	4
AD14AA050	50	10±2	4
AD14AA075	75	15±2	4
AD14AA100	100	20±3	4
AD14AA125	125	25±3	4
AD14AA150	150	30±3	4
AD14AA175	175	35±3	4
AD14AA200	200	40±3	4
AD14AA250	250	50±3.5	4
AD14AA300	300	60±4	4
AD14AA400	400	80±4	4
AD14AA500	500	100±5	4

(1) Delays. measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD14AB SERIES: 14-PIN DIL TRIPLE



FEATURES:

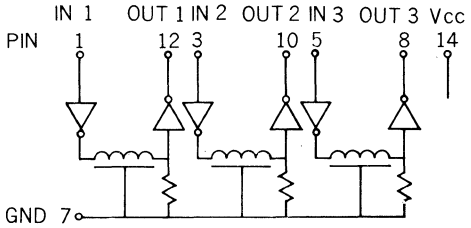
- TTL and DTL Compatible
- 3 Independent Equal Delays
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (delays or pin layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	−2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max.

All measurements made at Vcc=5.0V, 25°C

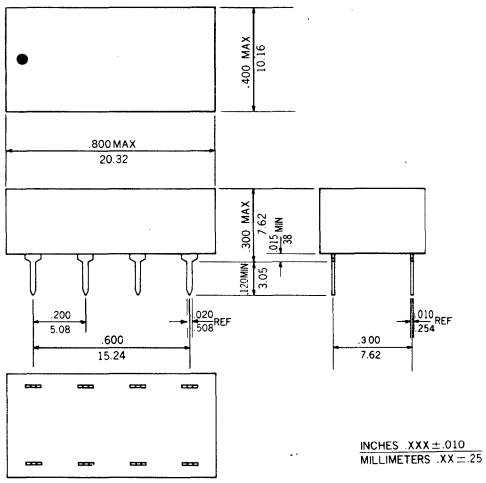
PACKAGE DIMENSIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

CIRCUIT AND PIN CONNECTIONS:



INPUT TEST CONDITIONS

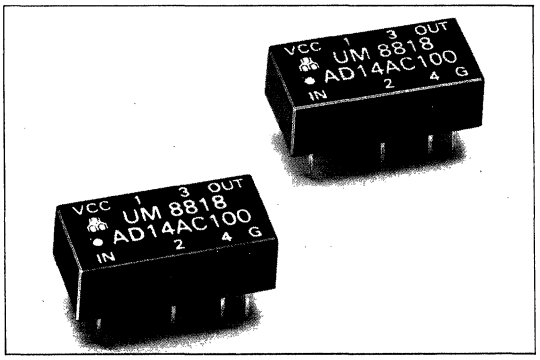
Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	60mA typical
Pulse Width:	min.100% of total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	DELAY TIME(1) ±5%(ns)	RISE TIME(2) ns max.
AD14AB005	5±1.5	3
AD14AB010	10±1.5	3
AD14AB020	20±1.5	3
AD14AB025	25±1.5	3
AD14AB030	30±2.0	3
AD14AB040	40±2.5	3
AD14AB050	50	3
AD14AB060	60	4
AD14AB070	70	4
AD14AB075	75	4
AD14AB080	80	4
AD14AB090	90	4
AD14AB100	100	4
AD14AB125	125	4
AD14AB150	150	4
AD14AB200	200	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD14AC SERIES: 14-PIN DIL 5-TAP FOR DYNAMIC RAM



FEATURES:

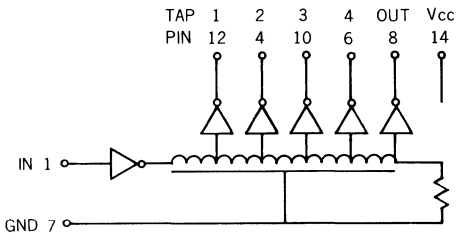
- TTL and DTL Compatible
- Specifically Designed for Dynamic RAM Timing
- 5 Taps
- Used with Multiplex Address RAMS
- Operating Temperature Range: 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	-2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max

All measurements made at Vcc=5.0V, 25°C

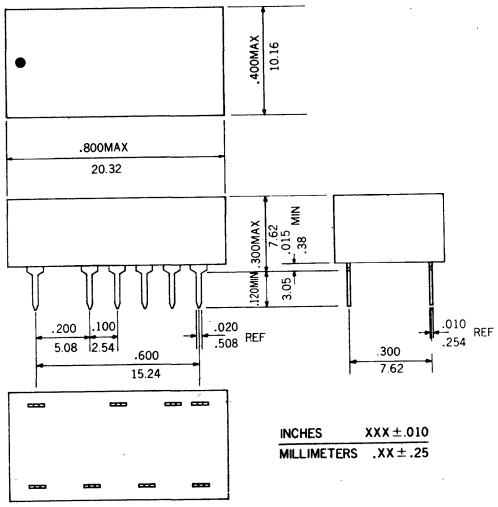
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

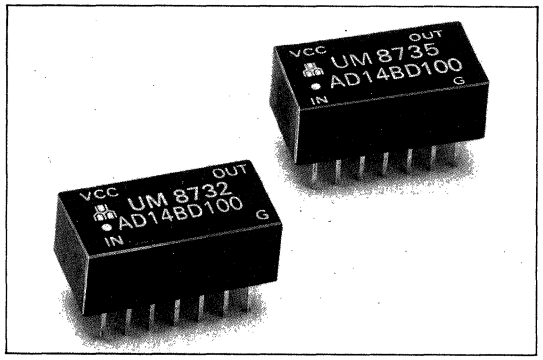
Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	60 mA typical
Pulse Width:	min. of 100% total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

UM PART NO.	TOTAL DELAY TAP1	TAP2	AT EACH TAP TAP3	TAP4	±5%(ns)(1) OUTPUT	RISE TIME(2) ns max.
AD14AC340	25±5	45±5	160	185	340	4
AD14AC400	30±5	80±5	220	250	400	4
AD14AC440	40±5	100	265	290	440	4
AD14AC515	85±5	140	320	345	515	5

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD14BD SERIES: 14-PIN DIL 10-TAP EQUALLY-SPACED



FEATURES:

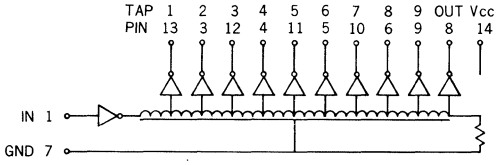
- Compatible with TTL Circuits
- 10 Equally-Spaced Delay Taps
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	-2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max

All measurements made at Vcc=5.0V, 25°C

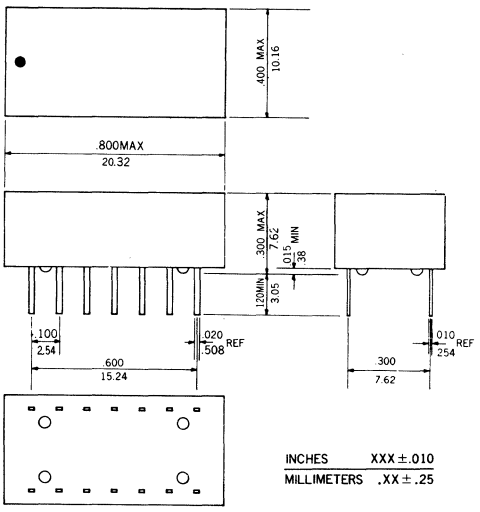
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
:20 TTL loads/ unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

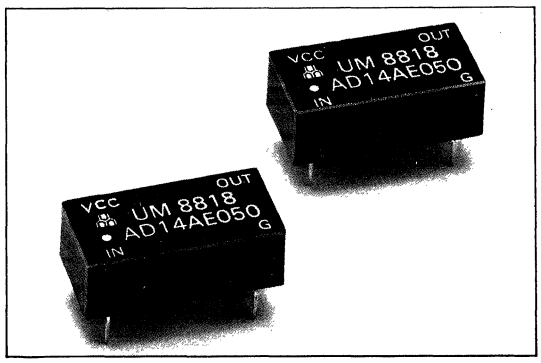
Pulse Voltage:	3.2V
Rise Time:	3.0ns
Supply Current:	120 mA typical
Pulse Width:	min 100% of total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns±10%	RISE TIME(2) ns max.
AD14BD050	50	5±2	4
AD14BD100	100	10±2	4
AD14BD150	150	15±2	4
AD14BD200	200	20±3	4
AD14BD250	250	25±3	4
AD14BD300	300	30	5
AD14BD350	350	35	5
AD14BD400	400	40	5
AD14BD450	450	45	5
AD14BD500	500	50	5
AD14BDA00	1000	100	5

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD14AE SERIES: 14-PIN DIL-SINGLE OUTPUT



FEATURES:

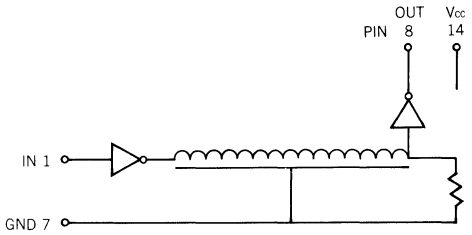
- TTL and DTL Compatible
- Single Output 14-pin DIL
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (delays or pin layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Votage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	-2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max.

All measurements made at Vcc=5.0V, 25℃

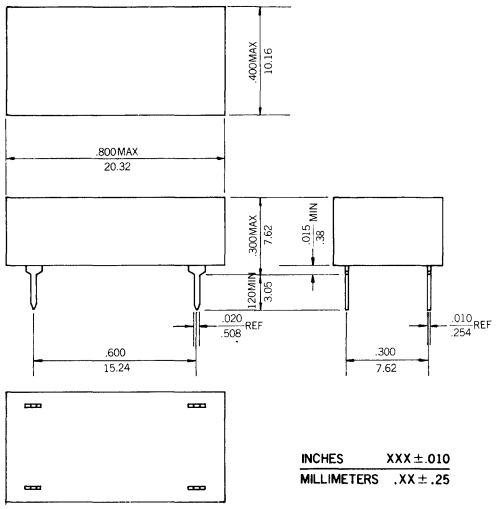
CIRCUIT CONFIGURATION:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

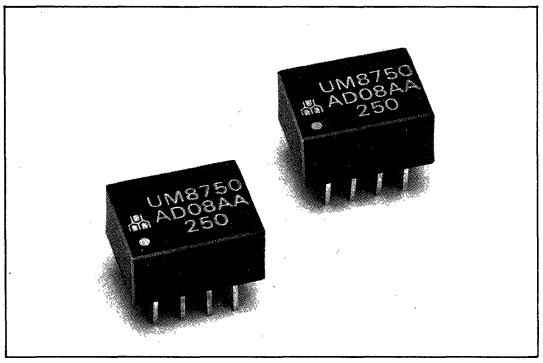
Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	60 mA typical
Pulse Width:	min. 100% of total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY (1)(3)ns	RISE TIME (2)ns max.	PART NUMBER	TOTAL DELAY (1)(3)ns	RISE TIME (2)ns max.
AD14AE010	10	4	AD14AE125	125	4
AD14AE020	20	4	AD14AE150	150	4
AD14AE030	30	4	AD14AE175	175	4
AD14AE040	40	4	AD14AE200	200	4
AD14AE050	50	4	AD14AE250	250	4
AD14AE060	60	4	AD14AE300	300	4
AD14AE070	70	4	AD14AE350	350	4
AD14AE080	80	4	AD14AE400	400	4
AD14AE090	90	4	AD14AE450	450	4
AD14AE100	100	4	AD14AE500	500	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.
(3) ±5% or ±2ns which is greater.

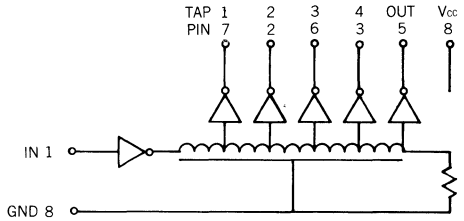
AD08AA SERIES: 8-PIN DIL 5-TAP EQUALLY-SPACED



FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (Delays or Pin Layouts) Available upon Request

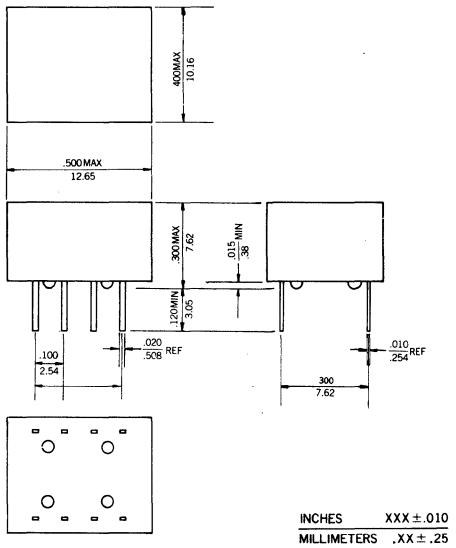
CIRCUIT CONFIGURATION:



ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: –2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

PACKAGE DIMENSIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

INPUT TEST CONDITIONS

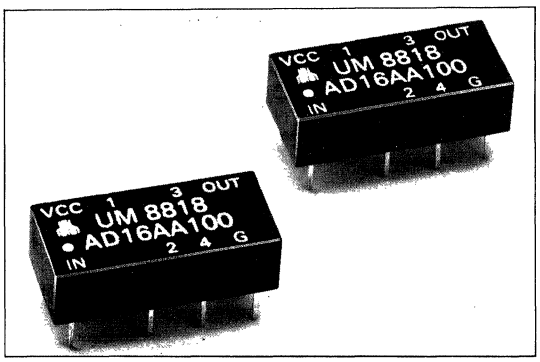
Pulse Voltage: 3.2 V
Rise Time: 3.0 ns
Supply Current: 60 mA typical
Pulse Width: min. of 100% total delay
Duty Cycle: 33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1)(3) ns	TAP DELAY(1)(3) ns	RISE TIME ns max
AD08AA025	25	5	4
AD08AA050	50	10	4
AD08AA100	100	20	4
AD08AA150	150	30	4
AD08AA200	200	40	4
AD08AA250	250	50	4
AD08AA300	300	60	4
AD08AA350	350	70	4
AD08AA400	400	80	4
AD08AA450	450	90	4
AD08AA500	500	100	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.
(3) ±5% or ±2ns which is greater.

AD16AA SERIES: 16-PIN DIL 5-TAP EQUALLY-SPACED



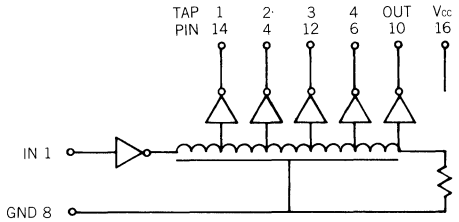
FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Fits in Standard 16-pin DIL
- Operating Temperature Range: 0℃ to+70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: –2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

CIRCUIT AND PIN CONNECTIONS:



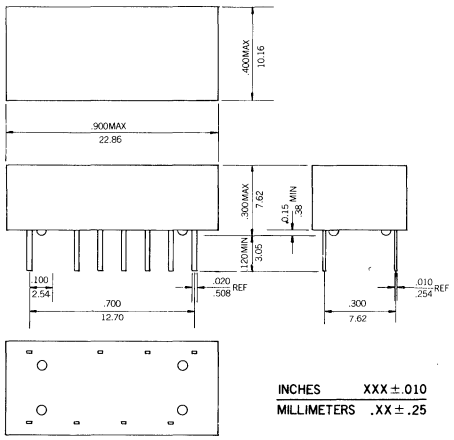
FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

INPUT TEST CONDITIONS

Pulse Voltage: 3.2V
Rise Time: 3.0ns
Supply Current: 60mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

PACKAGE DIMENSIONS:

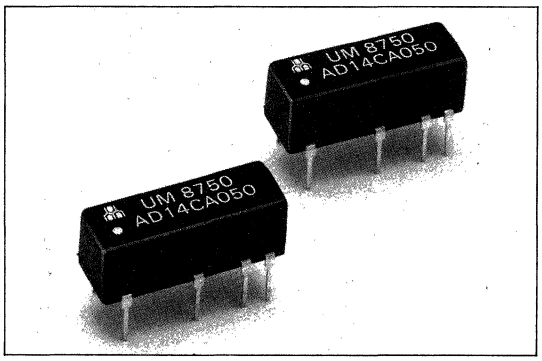


ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD16AA025	25±2	5±2	4
AD16AA050	50	10±2	4
AD16AA075	75	15±2	4
AD16AA100	100	20±3	4
AD16AA125	125	25±3	4
AD16AA150	150	30±3	4
AD16AA175	175	35±3	4
AD16AA200	200	40±3	4
AD16AA250	250	50±3.5	4
AD16AA300	300	60±4	4
AD16AA400	400	80±4	4
AD16AA500	500	100±5	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from .75V to 2.4V with no loads.

AD14CA SERIES: 14-PIN DIP 5-TAP AUTO INSERTABLE



FEATURES:

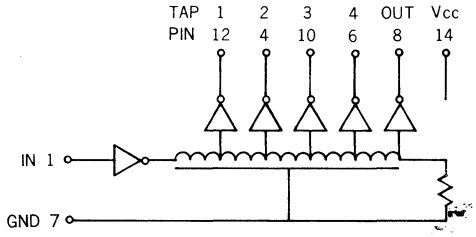
- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	−2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max.

All measurements made at Vcc=5.0V, 25°C

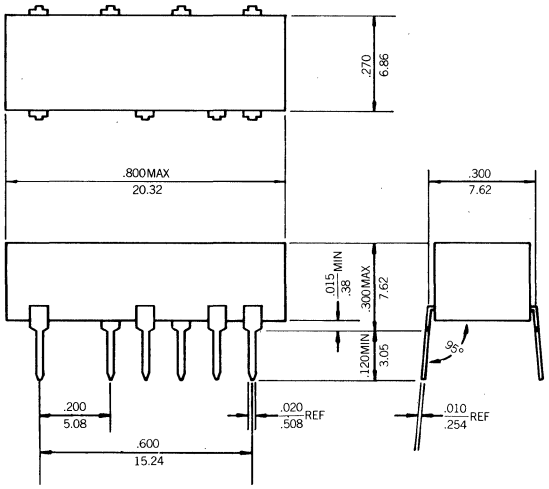
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INCHES XXX±.010
MILLIMETERS .XX±.25

INPUT TEST CONDITIONS

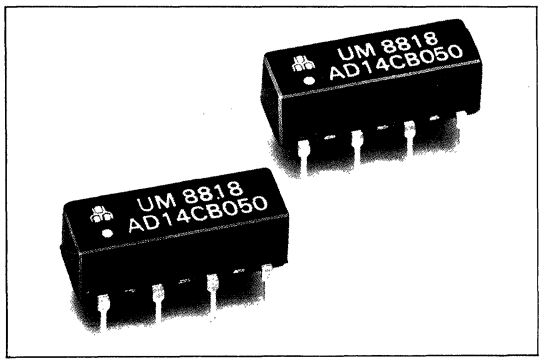
Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	60 mA typical
Pulse Width:	min. of 100% total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD14CA025	25±2	5±2	4
AD14CA050	50	10±2	4
AD14CA075	75	15±2	4
AD14CA100	100	20±3	4
AD14CA125	125	25±3	4
AD14CA150	150	30±3	4
AD14CA175	175	35±3	4
AD14CA200	200	40±3	4
AD14CA250	250	50±3.5	4
AD14CA300	300	60±4	4
AD14CA400	400	80±4	4
AD14CA500	500	100±5	4

(1) Delays. measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD14CB SERIES: 14-PIN DIP 3 INDEPENDENT AUTO INSERTABLE



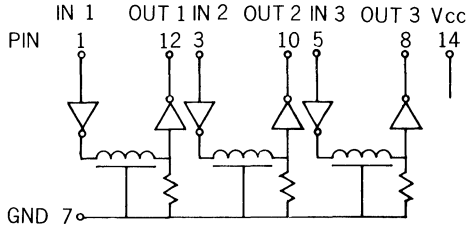
FEATURES:

- Compatible with TTL Circuits
- 3. Independent Equally Delays
- Operating Temperature Range: 0℃ to+70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: -2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

CIRCUIT AND PIN CONNECTIONS:



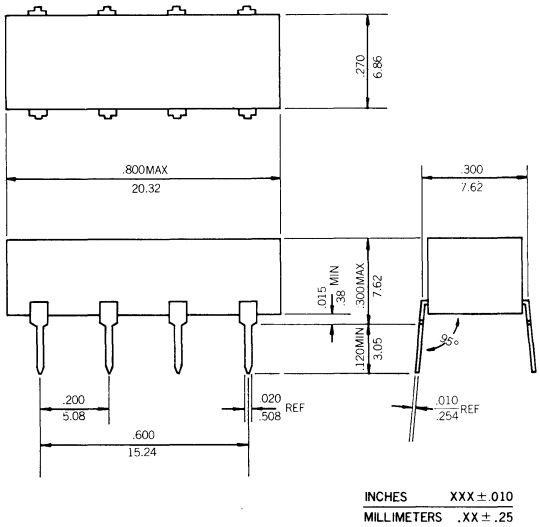
FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

INPUT TEST CONDITIONS

Pulse Voltage: 3.2 V
Rise Time: 3.0 ns
Supply Current: 60 mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

PACKAGE DIMENSIONS:

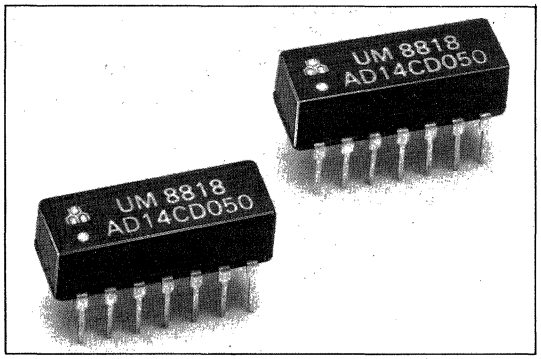


ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD14CB025	25±2	5±2	4
AD14CB050	50	10±2	4
AD14CB075	75	15±2	4
AD14CB100	100	20±3	4
AD14CB125	125	25±3	4
AD14CB150	150	30±3	4
AD14CB175	175	35±3	4
AD14CB200	200	40±3	4
AD14CB250	250	50±3.5	4
AD14CB300	300	60±4	4
AD14CB400	400	80±4	4
AD14CB500	500	100±5	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from .75V to 2.4V with no loads.

AD14CD SERIES: 14-PIN DIP 10-TAP AUTO INSERTABLE



FEATURES:

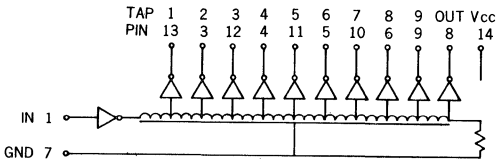
- Compatible with TTL Circuits
- 10 Equally-Spaced Delay Taps
- Operating Temperature Range: 0°C to +70°C
- Custom Designs (Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Input Current:	−2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max.

All measurements made at Vcc=5.0V, 25°C

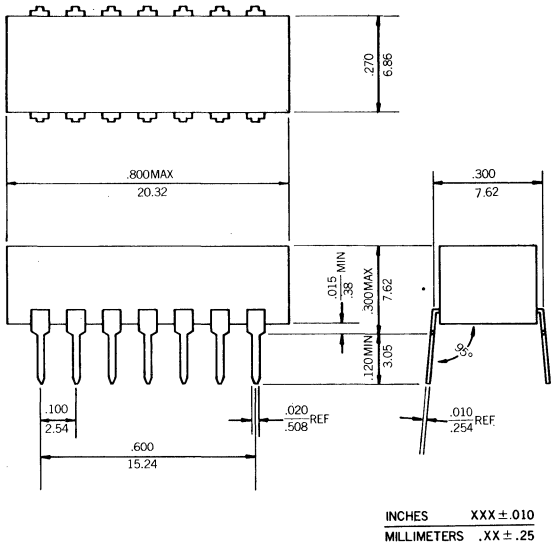
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

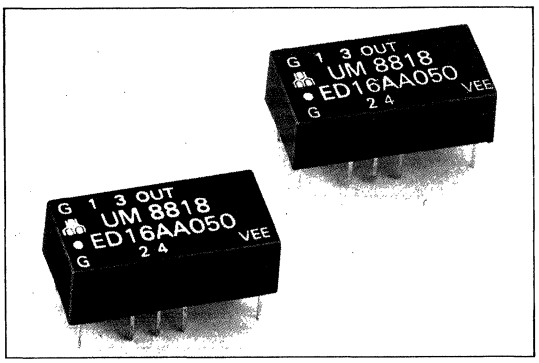
Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	120 mA typical
Pulse Width:	min. 100% of total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns±10%	RISE TIME(2) ns max.
AD14CD050	50	5±2	4
AD14CD100	100	10±2	4
AD14CD150	150	15±2	4
AD14CD200	200	20±3	4
AD14CD250	250	25±3	4
AD14CD300	300	30	5
AD14CD350	350	35	5
AD14CD400	400	40	5
AD14CD450	450	45	5
AD14CD500	500	50	5

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

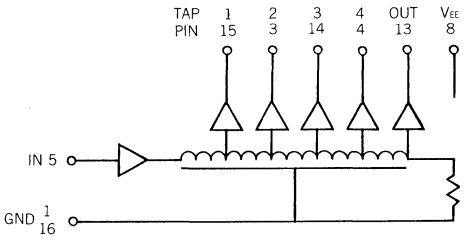
ED16AA SERIES: 16-PIN DIL 5-TAP EQUALLY-SPACED



FEATURES:

- Input and Output ECL Buffered
- 5 Equally-Spaced Delay Taps
- Fits in Standard 16-pin DIL
- Operating Temperature Range: −30°C TO +85°C
- Custom Design (Delays or pin Layouts) Available Upon Request

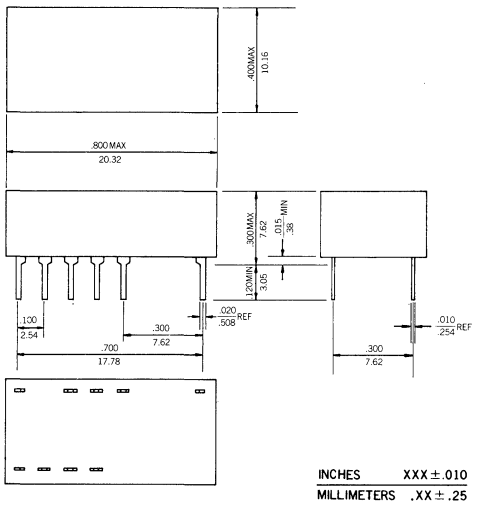
CIRCUIT AND PIN CONNECTIONS:



ELECTRICAL CHARACTERISTICS

Supply Voltage V_{EE}: −5.2±0.25 VDC
Logic 1 Input Voltage: −0.96 V min
Input Current: .26 mA max
Logic 0 Input Voltage: −1.65 V max
Input Current: .5 μA max
All Measurements Made at V_{CC} = −5.2V, 25°C

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

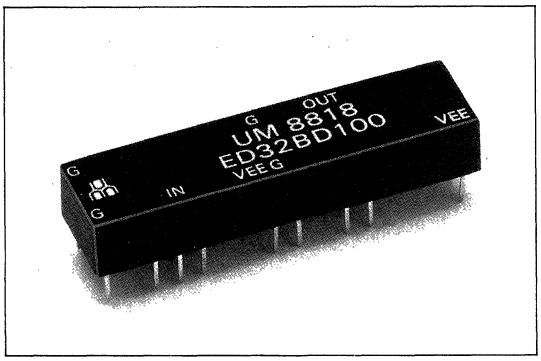
Pulse Voltage : 1V (−.75V to −1.75V)
Rise Time : 3.0 ns
Supply Current: 60mA typical
Pulse Width : min. 100% of total delay
Duty Cycle : 33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY (2)ns	TAP DELAY ns	RISE TIME(3) ns max
ED16AA010	10	2± .4	4
ED16AA020	20	4± .5	4
ED16AA025	25	5±1.0	4
ED16AA050	50	10±2.0	4
ED16AA075	75	15±2.0	4
ED16AA100	100	20±2.0	4
ED16AA150	150	30±2.0	4
ED16AA200	200	40±2.0	4
ED16AA250	250	50±2.5	4
ED16AA300	300	60±3.0	5
ED16AA400	400	80±4.0	5
ED16AA500	500	100±5.0	5

(1) Timedelay measurements referenced to 1st tap.
(2) ±5% or ±2ns which is greater.
(3)Risetime measured from 20% to 80% with loads.

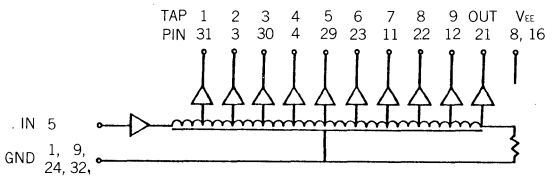
ED32BD SERIES: 32-PIN DIP 10-TAP EQUALLY-SPACED



FEATURES:

- Input and Output ECL Buffered
- 10 Equally-Spaced Delay Taps
- PC Board Economy Achieved.
- Operating Temperature Range: −30°C to +85°C
- Custom Design (Delays or pin Layouts) Available upon Request

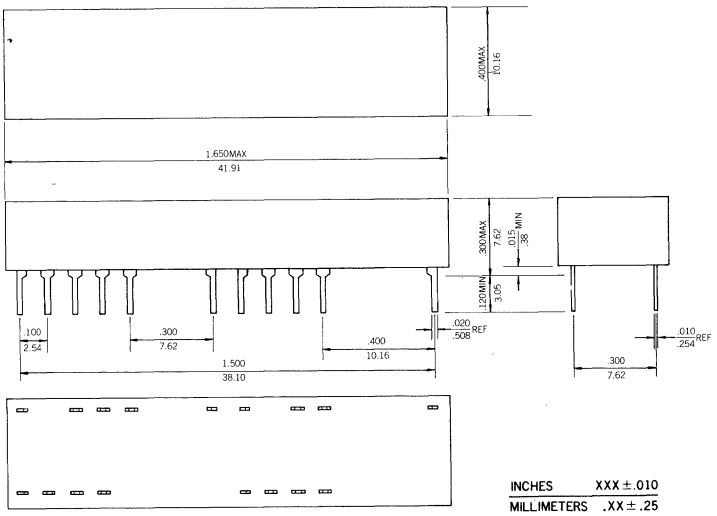
CIRCUIT CONFIGURATION



ELECTRICAL CHARACTERISTICS

Supply Voltage V_{EE}: −5.2±0.25 VDC
Logic 1 Input Voltage: −0.96 V min
Input Current: .26 mA max
Logic 0 Input Voltage: −1.65 V max
Input Current: .5 μA max
All Measurements Made at V_{CC} = −5.2V, 25°C

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

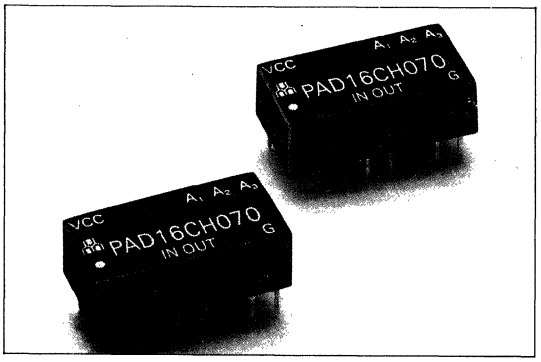
Pulse Voltage : 1V (−.75V to −1.75V)
Rise Time: 3.0ns
Supply Current: 120mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY (2)ns	TAP DELAY ns	RISE TIME(3) ns max
ED32BD030	30	3 ± .5	4
ED32BD050	50	5 ±1.0	4
ED32BD075	75	7.5±1.5	4
ED32BD100	100	10 ±2.0	4
ED32BD150	150	15 ±2.0	4
ED32BD200	200	20 ±2.0	4
ED32BD250	250	25 ±2.0	4
ED32BD300	300	30 ±2.0	5
ED32BD400	400	40 ±2.0	5
ED32BD500	500	50 ±2.5	5
ED32BD750	750	75 ±4.1	5
ED32BDA00	1000	100 ±5.0	5

(1) Timedelay measurements referenced to 1st tap.
(2) ±5% or ±2ns which is greater.
(3)Risetime measured from 20% to 80% with loads.

PAD16CH SERIES: 16-PIN DIL PROGRAMMABLE, 3 BIT, 8 DELAY STEPS, TTL COMPATIBLE



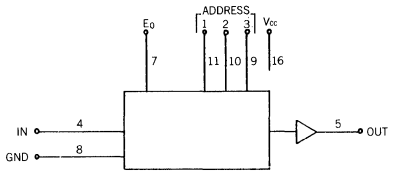
FEATURES

- Digitally Programmable in 8 Delay Steps
- Delay Increments of 1/2 ns Thru 70 ns
- Fits in Standard 16-pin DIL
- Operating Temperature Range: 0°C to + 70°C
- Output Fully TTL Interfaced
- Output Pulse Polarity Same as Input.

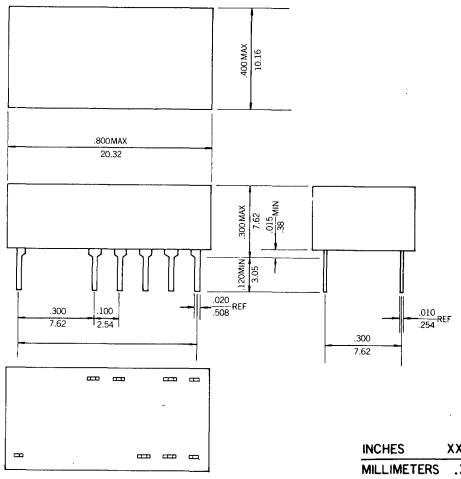
ELECTRICAL CHARACTERISTICS

Supply Voltage V_{CC}: 5.0 ± 0.25 VDC
Logic 1 Input Voltage: 2.0 V min
Input Current: 50 μA max
Logic 0 Input Voltage: 0.8 V max
Input Current: −2.0 mA max
Logic 1 Output Voltage: 2.4V min
Logic 0 Output Current: 0.5 V max
Inherent Delay: 7 NS ± 1 NS
Propagation Delay: Address to Output: 12 ns Typical
Enable to Output: 12 ns Typical
All Measurements Made at V_{CC} = 5.0V, 25°C

CIRCUIT CONFIGURATION:



PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

Pulse Voltage:	3.2 V
Rise Time:	3.0 ns
Supply Current:	60 mA typical
Pulse Width:	min. of 100% total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

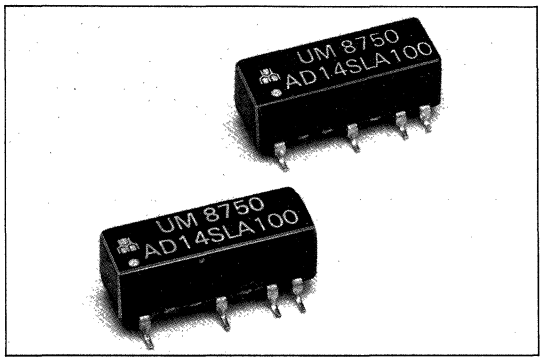
PART NO.	DELAY ns min	DELAY ns max	DELAY PER STEP ns	TOLERANCE PER STEP ns
PAD16CH007	7±1	14	1± .5	± .8
PAD16CH014	7±1	21	2± .6	±1.2
PAD16CH021	7±1	28	3± .7	±1.6
PAD16CH028	7±1	35	4± .8	±1.8
PAD16CH035	7±1	42	5±1.0	±2.0
PAD16CH042	7±1	49	6±1.2	±2.4
PAD16CH049	7±1	56	7±1.4	±2.8
PAD16CH056	7±1	63	8±1.6	±3.2
PAD16CH063	7±1	70	9±1.8	±3.6
PAD16CH070	7±1	77	10±2.0	±4.0

TRUTH TABLE

ENABLE	ADDRESS(BIT NO.) 3	2	1	DELAY OUT
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1				

1=High
0=Low
=Don't care
T_0=Reference or Inherent delay of circuit
T_1 to T_7=Multiplier of Incremenatal delay.

AD14SLA SERIES: 14-PIN 5-TAP SURFACE MOUNTING, L LEAD



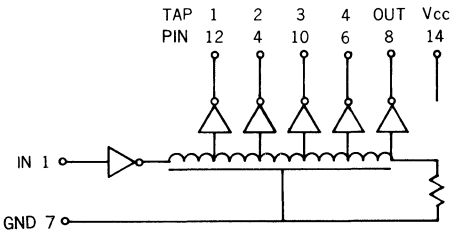
FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Surface Mount L Lead Package
- Operating Temperature Range: 0℃ to+70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

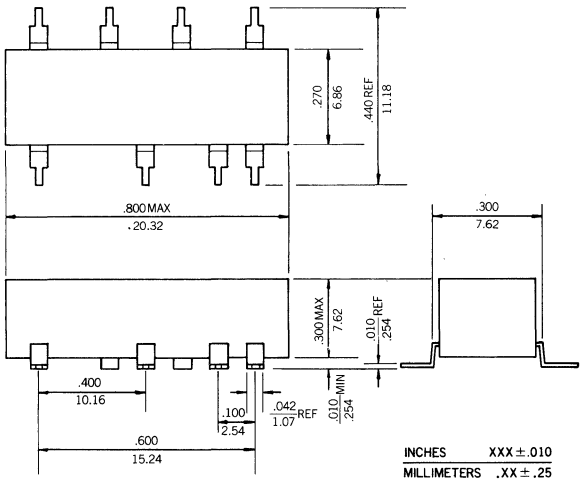
ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: –2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

CIRCUIT AND PIN CONNECTIONS:



PACKAGE DIMENSIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

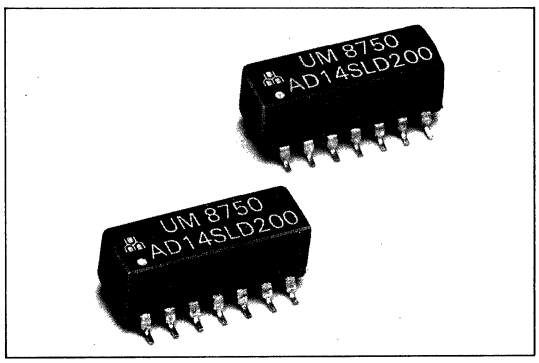
INPUT TEST CONDITIONS

Pulse Voltage: 3.2V
Rise Time: 3.0ns
Supply Current: 60mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD14SLA025	25±2	5±2	4
AD14SLA050	50	10±2	4
AD14SLA075	75	15±2	4
AD14SLA100	100	20±3	4
AD14SLA125	125	25±3	4
AD14SLA150	150	30±3	4
AD14SLA175	175	35±3	4
AD14SLA200	200	40±3	4
AD14SLA250	250	50±3.5	4
AD14SLA300	300	60±4	4
AD14SLA400	400	80±4	4
AD14SLA500	500	100±5	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from .75V to 2.4V with no loads.

AD14SLD SERIES: 14-PIN 10-TAP SURFACE MOUNTING, L LEAD



FEATURES:

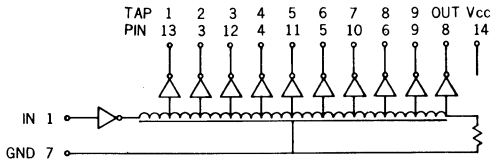
- Compatible with TTL Circuits
- 10 Equally-Spaced Delay Taps
- Surface Mount L Lead Package
- Operating Temperature Range: 0℃ to +70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Votage Vcc:	5.0±0.25 VDC
Logic 1 Input Voltage:	2.0V min.
Logic 1 Input Current:	50μA max.
Logic 0 Input Voltage:	0.8V max.
Logic 0 Input Current:	-2.0mA max.
Logic 1 Output Voltage:	2.4V min.
Logic 0 Output Voltage:	0.5V max.

All measurements made at Vcc=5.0V, 25℃

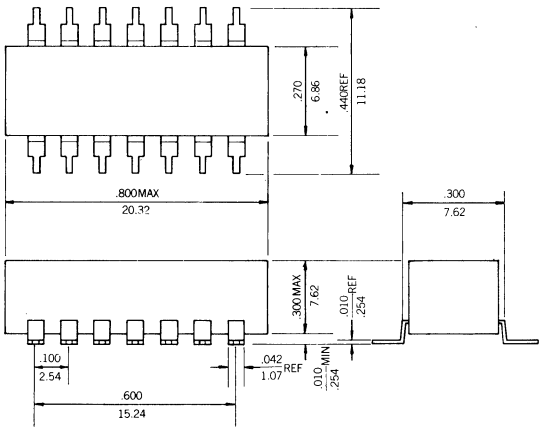
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output:	10 TTL loads/tap max.
	20 TTL loads/unit max.
Logic 1 Output:	20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INCHES XXX±.010
MILLIMETERS .XX±.25

INPUT TEST CONDITIONS

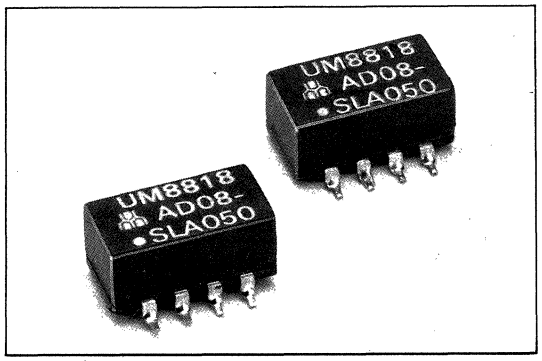
Pulse Voltage:	3.2V
Rise Time:	3.0ns
Supply Current:	120mA typical
Pulse Width:	min. 100% of total delay
Duty Cycle:	33% or less

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns±10%	RISE TIME(2) ns max.
AD14SLD050	50	5±2	4
AD14SLD100	100	10±2	4
AD14SLD150	150	15±2	4
AD14SLD200	200	20±3	4
AD14SLD250	250	25±3	4
AD14SLD300	300	30	5
AD14SLD350	350	35	5
AD14SLD400	400	40	5
AD14SLD450	450	45	5
AD14SLD500	500	50	5

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

AD08SLA SERIES: 8-PIN 5-TAP SURFACE MOUNTING, L LEAD



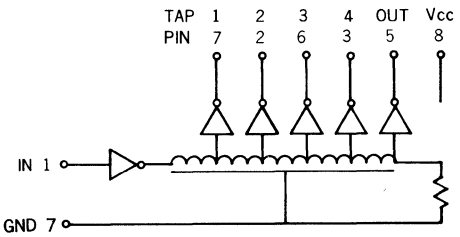
FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Surface Mount L Lead Package
- Operating Temperature Range: 0℃ to +70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: -2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

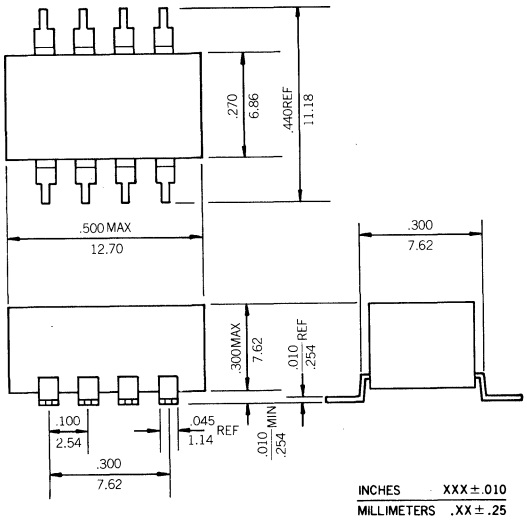
CIRCUIT AND PIN CONNECTIONS:



FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

PACKAGE DIMENSIONS:



INPUT TEST CONDITIONS

Pulse Voltage: 3.2 V
Rise Time: 3.0 ns
Supply Current: 60 mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

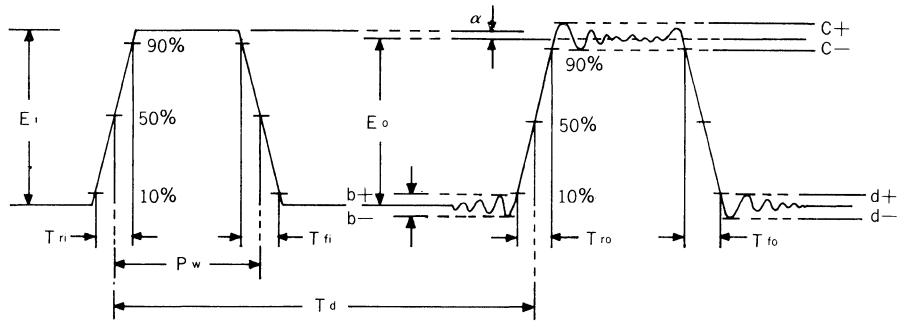
ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY(1) ns±5%	TAP DELAY(1) ns	RISE TIME(2) ns max.
AD08SLA025	25±2	5±2	4
AD08SLA050	50	10±2	4
AD08SLA075	75	15±2	4
AD08SLA100	100	20±3	4
AD08SLA125	125	25±3	4
AD08SLA150	150	30±3	4
AD08SLA175	175	35±3	4
AD08SLA200	200	40±3	4
AD08SLA250	250	50±3.5	4

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

MEASURING TECHNIQUES OF PASSIVE DELAY LINE.

● WAVEFORM AND PARAMETER DEFINITIONS



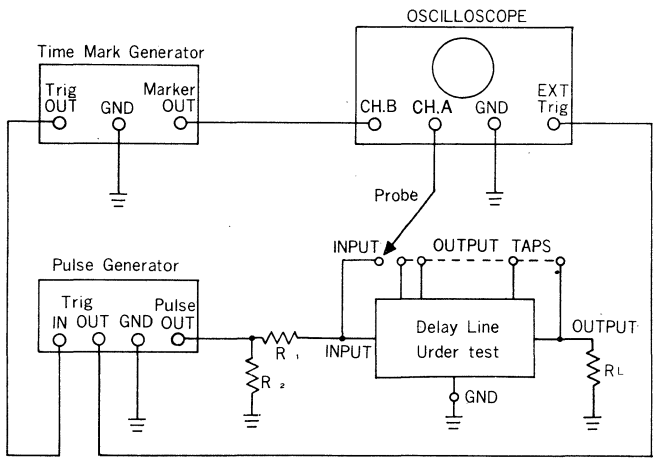
E_i — Input Pulse Voltage
E_o — Output Pulse Voltage
T_d — Delay Time
T_{ri} — Input Rise Time
T_{ro} — Output Rise Time
T_r — Delay Line Rise Time $T_r = \sqrt{T_{ro}^2 - T_{ri}^2}$

Z_o — Characteristic Impedance
P_w — Input Pulse Width
T_{fi} — Input Fall Time
T_{fo} — Output Fall Time
α — % Attenuation $= \frac{E_i - E_o}{E_i} \times 100\%$
S — % Distortion $= \frac{|b| \text{ or } |c| \text{ or } |d|}{E_o} \times 100\%$

● MEASUREMENT CONDITION

$E_i = 3.0V$
$P_w = 3 \times T_d$
Period $= 4 \times P_w$

● TEST CIRCUIT



Input Matching Resistances

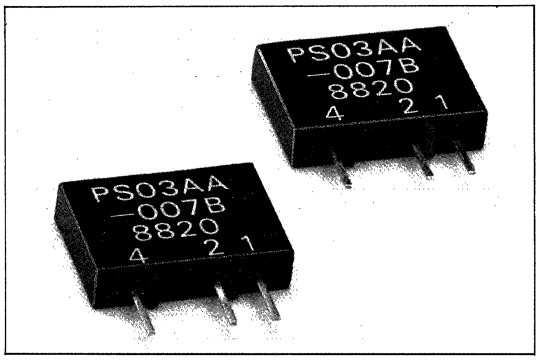
$R_1 = \sqrt{Z_o (Z_o - 50)}$

$R_2 = 50\sqrt{Z_o / (Z_o - 50)}$

Terminating Resistance

$R_L = Z_o$

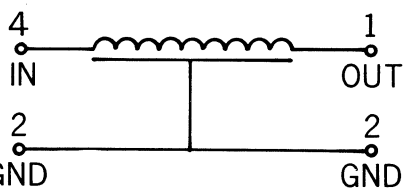
PS03AA SERIES: 3-PIN SIP-SINGLE OUTPUT



FEATURES:

- 3-pin SIP Package
- Compatible with ECL and TTL Circuits
- Small Size
- Other Delays Available upon Request

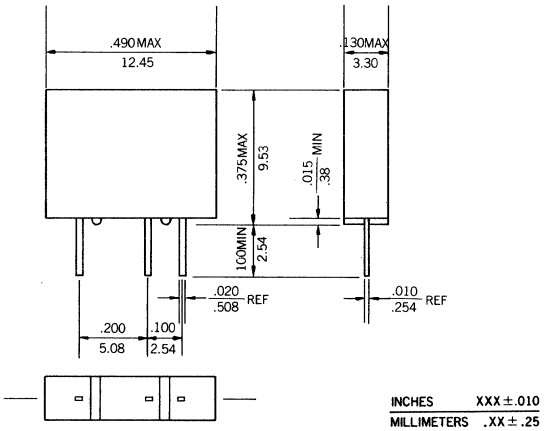
CIRCUIT CONFIGURATION:



GENERAL SPECIFICATIONS:

Total Delay:1 to 10 ns
Distortion:±10% max.
Characteristic Impedance: 100 ohms (±10%)
Temperature Coefficient: 100 ppm/°C max.
Operating Temperature Range:0°C to +70°C
Storage Temperature Range:-55°C to +125°C
Insulation Resistance: 1000 megohms min.
50VDC, +25°C

PACKAGE DIMENSIONS:



PART NUMBER SYSTEM:

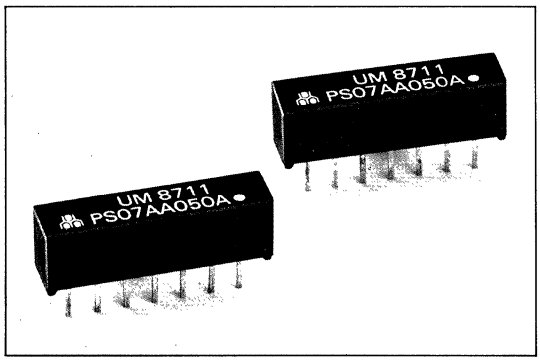
PS03AA 005 B

- B — Characteristic Impedance in ohm
  B=100 ohms
- 005 — Total Delay in ns
  For example:005=5 ns
- PS03AA — Basic Series
  Passive delay line SIP 3 pins

ELECTRICAL SPECIFICATIONS:

PART NO.	IMPEDANCE Zo±10%(Ω)	TOTAL DELAY Td (ns)	RISE TIME Tr max. (ns)	ATTENUATION max. (%)
PS03AA001B	100	1.0±0.2	3.0	2
PS03AA002B	100	2.0±0.4	3.0	2
PS03AA003B	100	3.0±0.5	3.0	2
PS03AA004B	100	4.0±0.5	3.5	2
PS03AA005B	100	5.0±0.5	3.5	2
PS03AA006B	100	6.0±0.5	3.5	2
PS03AA007B	100	7.0±0.5	4.0	2
PS03AA008B	100	8.0±0.5	4.0	2
PS03AA009B	100	9.0±0.5	4.5	2
PS03AA010B	100	10.0±0.5	4.5	2

PS07 SERIES: 7-PIN SIP 5-TAP EQUALLY-SPACED



FEATURES:

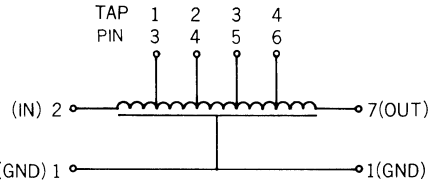
- 7-Pin SIP Package
- 5 Equally-Spaced Delay Taps
- Optional Internal Termination
- Other Delays Available upon Request

GENERAL SPECIFICATIONS:

Total Delay: 10 to 100ns
Tap Delays: 20% increments
Characteristic Impedance: 50 to 100 ohms (±10%)
Distortion: ±10% max.
Temperature Coefficient of Delay: 200 ppm/℃ max.
Operating Temperature Range: 0℃ to +70℃
Storage Temperature Range: −55℃ to +125℃
Insulation Resistance: 1000 megohms min.
50VDC, 25℃

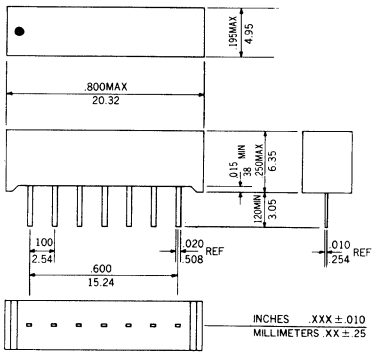
CIRCUIT CONFIGURATION AND PIN CONNECTIONS:

Circuit A



PACKAGE DIMENSIONS:

Package A



PART NUMBER SYSTEM:

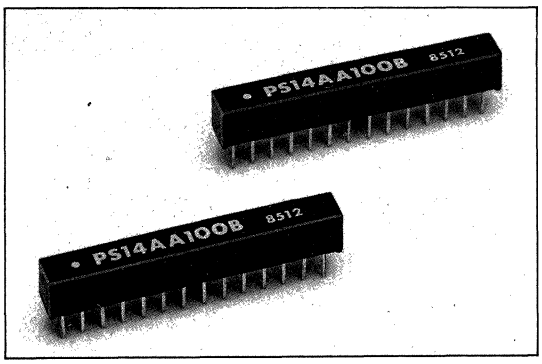
PS07 A A 100 B

- B — Characteristic Impedance in ohm
  A=50 ohms B=100 ohms
- 100 — Delay Time in ns
  For examples: 100=100ns
  050=50ns
- A — Circuit Configuration - See schematics Above
  circuit A is standard, other pin connections
  are available upon request
- A — Package Dimensions
  Package A is standard
- PS07 — Basic Series Number
  Passive Delay Line, SIP 7 pins

ELECTRICAL SPECIFICATIONS:

PART NO.	IMPEDANCE Zo±10%(Ω)	TOTAL DELAY TIME ±5%(ns)	TAP DELAY (ns)	RISE TIME Tr max. (ns)	ATTENUATION max. (%)
PS07AA010A	50	10	2.0±0.5	4.0	5.0
PS07AA020A	50	20	4.0±2.0	6.0	5.0
PS07AA030A	50	30	6.0±3.0	9.0	5.0
PS07AA040A	50	40	8.0±3.0	12.0	5.0
PS07AA050A	50	50	10.0±3.0	15.0	5.0
PS07AA100A	50	100	20±3.0	30.0	6.0
PS07AA010B	100	10	2.0±0.5	4.0	5.0
PS07AA020B	100	20	4.0±2.0	6.0	5.0
PS07AA030B	100	30	6.0±3.0	9.0	5.0
PS07AA040B	100	40	8.0±3.0	11.0	5.0
PS07AA050B	100	50	10.0±3.0	14.0	5.0
PS07AA100B	100	100	20±3.0	28.0	6.0

PS14 SERIES: 14-PIN SIP 10-TAP EQUALLY-SPACED



FEATURES:

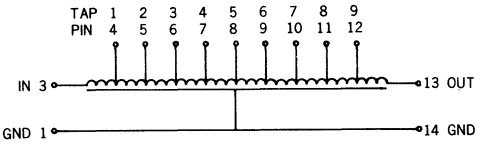
- 14-pin SIP Package
- 10 Equally-Spaced Delay Taps
- Low Output Distortion
- Other Delays Available upon Request

GENERAL SPECIFICATIONS:

Total Delay: 10 to 250 ns
Tap Delays: 10% increments
Characteristic Impedance: 50 ohms (±10%)
Distortion: ±10% max.
Temperature Coefficient of Delay: 100ppm/℃ max.
Operating Temperature: 0℃ to +70℃
Storage Temperature Range: −55℃ to +125℃
Insulation Resistance: 1000 megohms min.
50VDC, 25℃

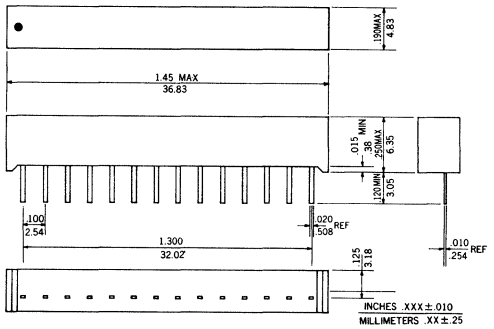
CIRCUIT CONFIGURATION AND PIN CONNECTIONS:

Circuit A



PACKAGE DIMENSIONS:

Package A



PART NUMBER SYSTEM:

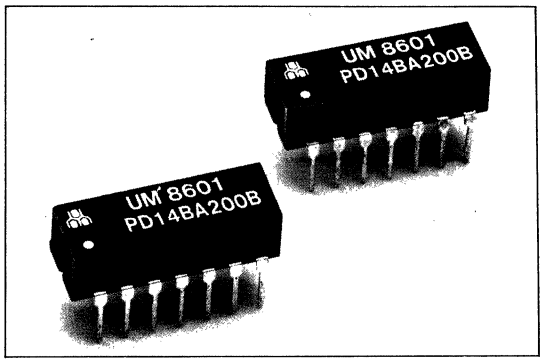
PS14 A A 100 A

- Characteristic Impedance in ohm
  A=50 ohms
- Total Delay Time in ns
  For examples: 050=50 ns
  100=100 ns
- Circuit Configuration-See schematics Above, circuit A is standard, other pin connections are available upon request
- Package Dimensions
  Package A is standard
- Basic Series
  Passive delay line, SIP 14 pins

STANDARD RATINGS:

PART NO.	IMPEDANCE Zo±10%(Ω)	TOTAL DELAY td±5%(ns)	TAP DELAY (ns)	RISE TIME tr max. (ns)	ATTENUATION max (%)
PS14AA010A	50	10±1	1±0.5	2.5	5
PS14AA020A	50	20±2	2±0.5	4	5
PS14AA030A	50	30±2	3±1	6	5
PS14AA040A	50	40	4±2	8	5
PS14AA050A	50	50	5±2	9	5
PS14AA100A	50	100	10±3	18	6
PS14AA150A	50	150	15±3	28	8
PS14AA200A	50	200	20±3	38	10
PS14AA250A	50	250	25±3	45	12

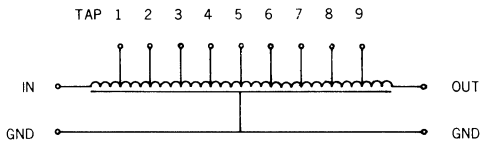
PD14 SERIES: 14-PIN DIP 10-TAP EQUALLY-SPACED



FEATURES:

- Standard 14-pin DIP Package
- 10 Equally-Spaced Delay Taps
- Compatible with TTL and DTL
- Custom Designs Available upon Request.

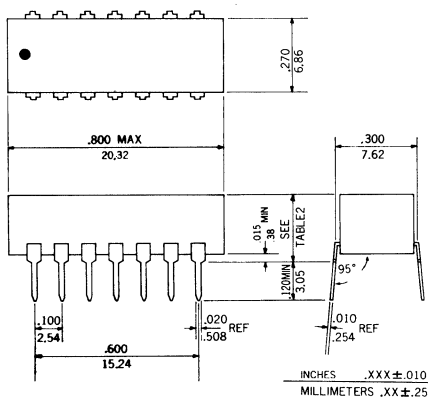
CIRCUIT CONFIGURATION AND PIN CONNECTIONS:



GENERAL SPECIFICATIONS:

Total Delay: 10 to 1000 ns.
Tap Delay: 10% increments standard (other increments available upon request).
Rise Time: 20% max. of total delay
Characteristic Impedance: 50 to 500 ohms (±10%)
Distortion: ±10% max.
Temperature Coefficient of Delay: 100ppm/°C max.
Operating Temperature Range: 0°C to +70°C
Storage Temperature Range: −55°C to +125°C
Insulation Resistance: 1000 megohms min. 50VDC, +25°C
Dielectric Strength: 50VDC

PACKAGE DIMENSIONS:



PART NUMBER SYSTEM:

PD14 A A 050 A

- A — Characteristic Impedance in ohm A=50 ohms B=100 ohms C=200 ohms D=300 ohms.
- 050 — Total Delay in ns. For examples: 050=50ns 125=125ns.
- A — Circuit Configuration and Pin Connections. See schematics Above , circuit A to F are standard(see Table 1), other pin connections are available upon request
- A — Mounting Height of Package (see Table 2)
- PD14 — Basic Series Number Passive delay line, DIP 14 pins

TABLE 1 - PIN CONNECTIONS

Circuit	IN	Tap1	Tap2	Tap3	Tap4	Tap5	Tap6	Tap7	Tap8	Tap9	OUT	GND
A	2	3	4	5	6	7,8	9	10	11	12	13	1,14
B	14	2	12	3	11	4	5	10	6	9	7	1,8
C	1	13	2	12	3	11	5	10	6	9	7	8,14
D	6	5	4	3	2	1	13	12	11	10	9	7,8
E	1	2	3	4	5	6	12	11	10	9	8	7
F	1	13	2	12	3	11	4	10	5	9	6	7

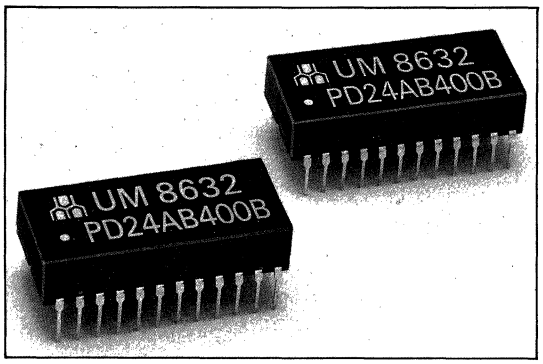
TABLE 2-MOUNTING HEIGHT

Code	Dimension (max.)
A	.300 in(7.62mm)
B	.250 in(6.35mm)
C	.200 in(5.08mm)

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY Td(ns)±5%	Td/TAP (ns)	RISE TIME Tr(ns) max.	ATTENUATION(%) PER IMPEDANCE 50	100	200
PD14XX010X	10±1	1±0.5	3.0	3	5	
PD14XX020X	20	2±0.5	5.0	3	5	5
PD14XX030X	30	3±1	7.0	3	5	5
PD14XX040X	40	4±2.0	8.0	3	5	5
PD14XX050X	50	5±2.0	10.0	3	5	5
PD14XX100X	100	10±3	20.0	3	5	5
PD14XX150X	150	15±3	30.0	3	5	6
PD14XX200X	200	20±3	40.0	4	5	6
PD14XX250X	250	25±3	50.0	4	5	6
PD14XX300X	300	30±3	60.0		6	8
PD14XX400X	400	40±4	80.0		7	8
PD14XX500X	500	50±5	100.0		8	10
PD14XXA00X	1000	100±10	200.0		10	20

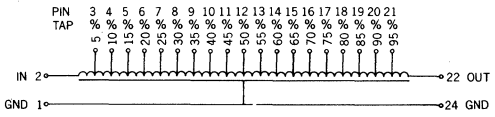
PD24 SERIES: 24-PIN DIP 20-TAP EQUALLY-SPACED



FEATURES:

- TTL and DTL Compatible
- 20 Equally-Spaced Delay Taps
- Standard 24-pin DIP Package
- Custom Designs Available upon Request

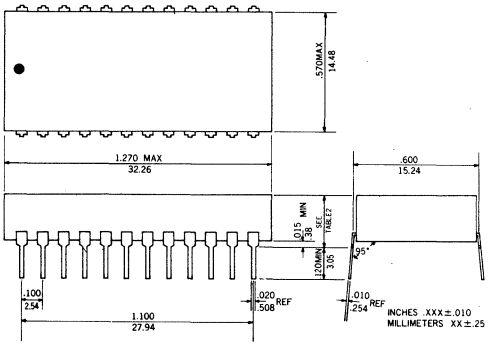
CIRCUIT CONFIGURATION AND PIN CONNECTIONS:



GENERAL SPECIFICATIONS:

Total Delay: 20 to 1000 ns
Tap Delays: 5% increments of total delay
Characteristic Impedance: 50 to 200 ohms (±10%)
Distortion: ±10% max.
Temperature Coefficient of Delay: 100 ppm/℃ max.
Operating Temperature Range: 0℃ to +70℃
Storage Temperature Range: −55℃ to +125℃
Insulation Resistance: 1000 megohms min.
50VDC, +25℃
Dielectric Strength: 50VDC

PACKAGE DIMENSIONS:



PART NUMBER SYSTEM:

PD24 A A 200 B

- B — Characteristic Impedance in ohm
  A=50 ohms B=100 ohms C=200 ohms
- 200 — Total Delay in ns
  For examples: 200=200ns
  A00=1000ns
- A — Circuit Configuration and Pin Connections (see Table 1)
- A — Mounting Height of Package (see Table 2)
- PD24 — Basic Series Number
  Passive delay line, DIP 24 Pins

TABLE 1-PIN CONNECTIONS

Circuit	IN	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Tap 10	Tap 11	Tap 12	Tap 13	Tap 14	Tap 15	Tap 16	Tap 17	Tap 18	Tap 19	OUT	GND
A	2	3	4	5	6	7	8	9	10	11	12	14	15	16	17	18	19	20	21	22	23	1,24
B	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23	12
C	1	2	3	4	5	6	7	8	9	10	11	14	15	16	17	18	19	20	21	22	23	12,24
E	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	1,24

TABLE 2- MOUNTING HEIGHT

Code	in inches	in mm
A	.325	8.26
B	.300	7.62
C	.275	6.99

ELECTRICAL SPECIFICATIONS:

PART NO.	TOTAL DELAY Td(ns)±5%	TAP DELAY (ns)	RISE TIME Tr(ns) max.	ATTENUATION(%) PER IMPEDANCE 50	100	TYPICAL (ohm) 200
PD24XX020X	20±2	1±0.5	3	5	5	6
PD24XX040X	40	2±0.5	4	5	5	8
PD24XX060X	60	3±1	6	6	6	8
PD24XX080X	80	4±2	8	6	6	8
PD24XX100X	100	5±2	10	6	8	8
PD24XX200X	200	10±3	20	8	8	8
PD24XX300X	300	15±3	30	8	8	8
PD24XX400X	400	20±3	40	8	8	10
PD24XX500X	500	25±3	50	8	8	10
PD24XXA00X	1000	50±5	100	10	10	10

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