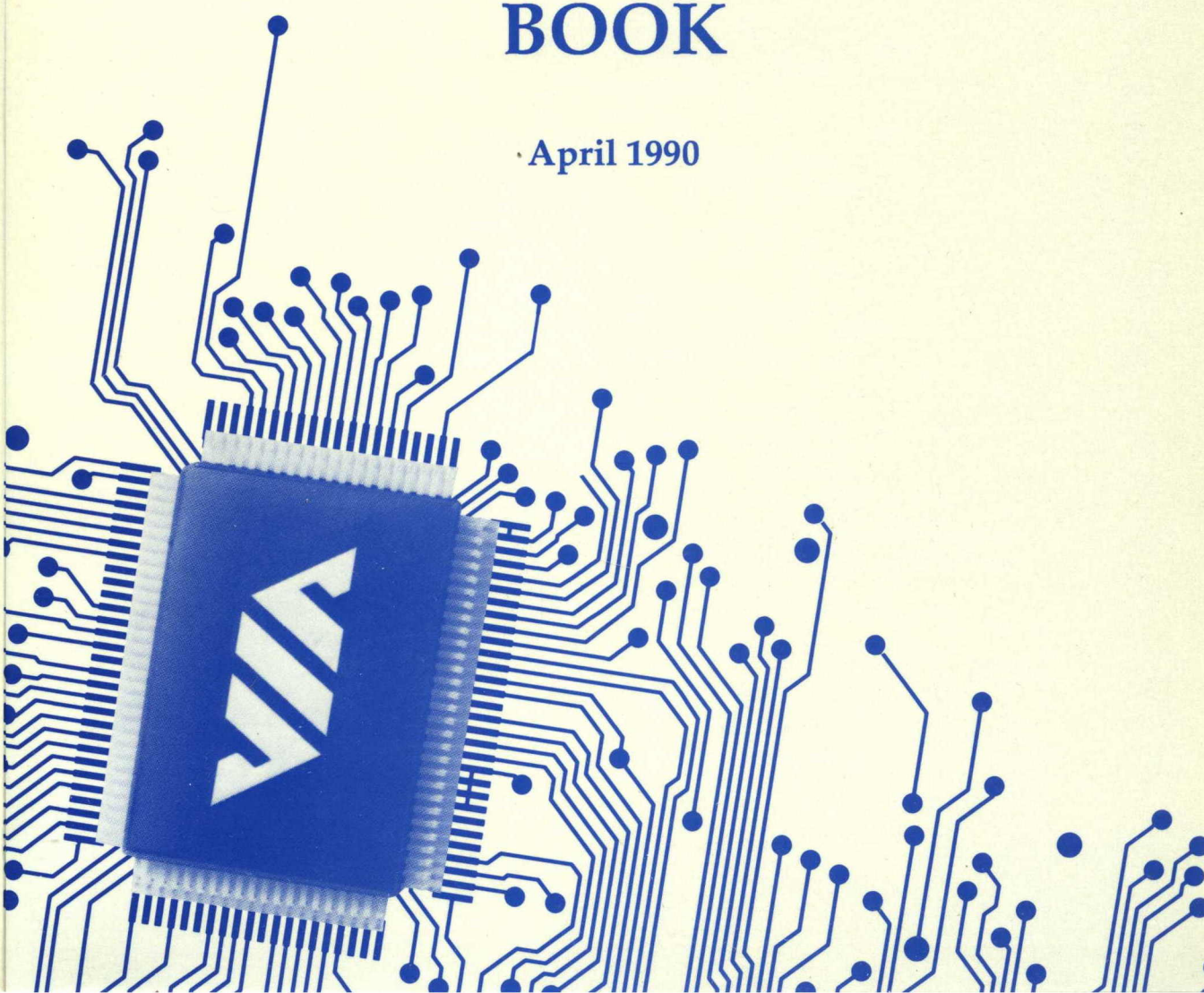
Technologies, Inc.

# DATA BOOK

April 1990



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ADVANCE
Advanced datasheets provide specifications for products which are not yet complete or fully characterized. They provide design target information for customer planning purposes. The word ADVANCE is marked below the part number on the upper right hand corner of the cover page.

PRELIMINARY
Preliminary datasheets provide typical specifications only pending completion of device characterization. The word PRELIMINARY is marked below the part number on the upper right hand corner of the cover page.

# VIA TECHNOLOGIES DATA BOOK

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# INTRODUCTION TO VIA

VIA Technologies, Inc., founded in 1987, and headquartered in Sunnyvale, California, designs and develops high performance computer chip sets for desktop personal computers, workstations and laptops. "Chip Sets" include all the circuitry required to implement the computer motherboard except RAM, ROM, CPU and co-processors.

## FLEXSET PRODUCTS

VIA Technologies' current products include both proprietary and alternate source IBM-compatible PC/AT system logic devices. At the forefront of VIA Technologies' IC product offering is the FlexSet, a new and proprietary family of PC/AT system logic chips based on a unique universal chip set concept. VIA Technologies-based PCs share the same core logic throughout the entire PC spectrum requiring only a single "personalized memory controller" to implement each new system. In addition to very low motherboard IC count, this modular approach provides a significant breakthrough in manufacturing cost, inventory management, and time to market.

VIA Technologies products offer flexibility, high density, and enhanced performance across the entire PC/AT system spectrum. Utilizing proven, state-of-the-art bipolar and CMOS processes, our customers are able to achieve low system costs in both procurement and manufacturing. Because VIA Technologies utilizes advanced semi-custom design tools and processes, we can also rapidly modify existing products to provide a completely customized chip set for the high volume customer.

## UNIVERSAL PRODUCTS

Universal Products can be designed into any PC/AT system. Customer benefits include high system integration and design flexibility, which results in overall system price/performance improvements.

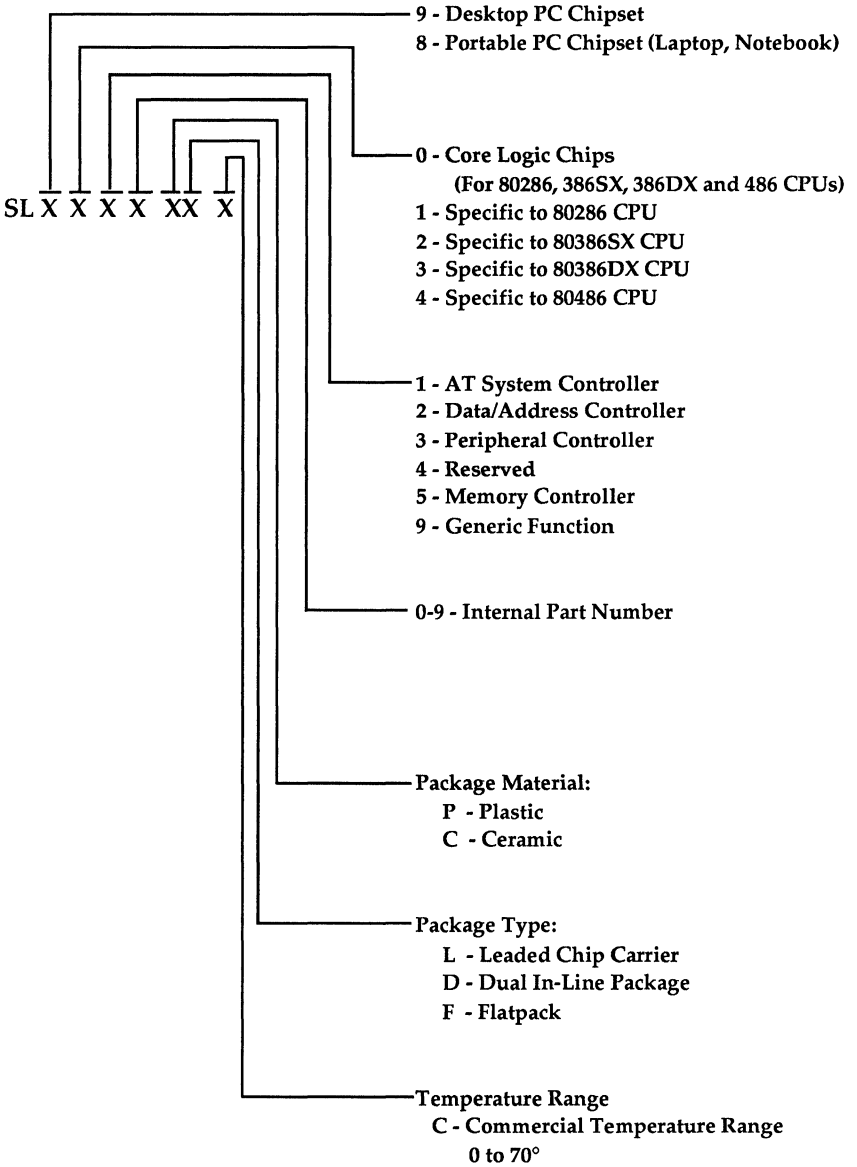
Our current Universal Product line includes the SL9030 Integrated Peripheral Controller, the SL9090/A Universal PC/AT Clock Chip and the SL9095 Laptop Power Management Unit.

## DESIGN SERVICES

VIA also offers standard and custom motherboard design services to accelerate our customer's time to market. Current evaluation board products are included in this data book. For other board design services and products, please contact your sales representative or contact VIA directly.

## ORDERING and PACKAGING INFORMATION

### Part Number Scheme



# FlexSet

# Products

## FEATURES

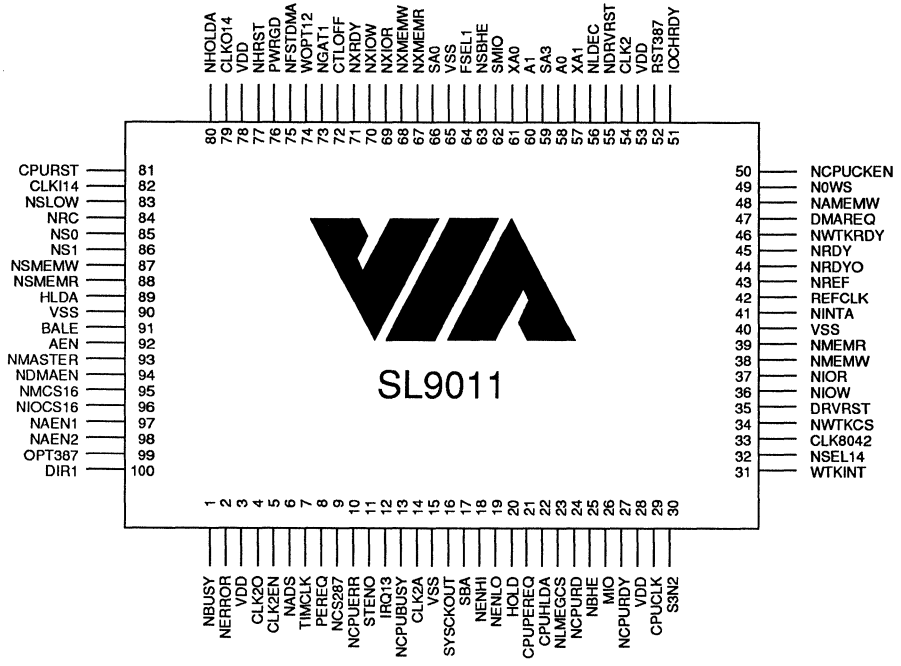
- AT System Control Logic.
- Supports 80286, 80386SX (P9), or 80386DX-based Designs.
- Up to 25 MHz Performance.
- Clock Switching and Reset Logic.
- Programmable Wait States for 8 Bit AT Cycles.
- Generates all Essential Clock Signals for PC's.
- Synchronous Options.
- Refresh/DMA Arbitration.
- Numerical Coprocessor Support for 80287, 80387SX, 80387DX and Weitek Coprocessor.
- Ready Generation Logic.
- Generates Data, Address, Direction and Enable Controls.
- Advanced ALE Generation.
- Advance CMOS Technology.
- 100 pin Flatpack.

## DESCRIPTION

The SL9011 System Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system control logic.

The SL9011 is part of the Core AT Logic that implements the system logic which is common to the microprocessors 80286, 80386SX and 80386DX. Up to 25 MHz performance is supported. In addition to the SL9011, the Core AT Logic chips consists of the SL9020 Data Controller, the SL9025 Address Controller, the SL9030 Integrated Peripheral Controller and the SL9X50/1 Memory Controller.

## PINOUT


SL9011
1 NBUSY
2 NERROR
3 VDD
4 CLK2O
5 CLK2EN
6 NADS
7 TIMCLK
8 PEREQ
9 NCS287
10 NCPUERR
11 STENO
12 IRQ13
13 NCPUBUSY
14 CLK2A
15 VSS
16 SYSCKOUT
17 SBA
18 NENHI
19 NENLO
20 HOLD
21 CPUPEREQ
22 CPUHLDA
23 NLMEGCS
24 NCPURD
25 NBHE
26 MIO
27 NCPURDY
28 VDD
29 CPUCLK
30 S3N2
31 WTKINT
32 NSEL14
33 CLK8042
34 NWTKCS
35 DRVRST
36 NIOW
37 NIOR
38 NMEMW
39 NMEMR
40 VSS
41 NINTA
42 REFCLK
43 NREF
44 NRDYO
45 NRDY
46 NWTKRDY
47 DMAREQ
48 NAMEMW
49 N0WS
50 NCPUCKEN
51 IOCHRDY
52 RST387
53 VDD
54 CLK2
55 NDRVRST
56 NLDEC
57 XA1
58 A0
59 SA3
60 A1
61 XA0
62 SMIO
63 NSBHE
64 FSEL1
65 VSS
66 SA0
67 NXMEMR
68 NXMEMW
69 NXIOR
70 NXIOW
71 NXRDY
72 CTLOFF
73 NGAT1
74 WOPT12
75 NFSTDMA
76 PWRGD
77 NHRST
78 VDD
79 CLKOT14
80 NHOLDA
81 CPURST
82 CLKI14
83 NSLOW
84 NRC
85 NS0
86 NS1
87 NSMEMW
88 NSMEMR
89 HLDA
90 VSS
91 BALE
92 AEN
93 NMASTER
94 NDMAEN
95 NMCS16
96 NIOCS16
97 NAEN1
98 NAEN2
99 OPT387
100 DIR1

## DESCRIPTION (Cont'd.)

The SL9011 provides the AT System Control Logic. It generates all the major clocks for an AT compatible system design along with the command and control signals for both the system and peripheral busses. It interfaces with the CPU to determine the type of the bus cycle to execute, and generates the CPU READY signal. The SL9011 System Controller contains logic to make conversions between 16-bit and 8-bit data accesses. It also generates the control signals necessary for the 80287, 80387SX and 80387DX Numeric Processors.

The SL9011 controls all bus activity and provides arbitration between the CPU, DMA, External Master devices and the Refresh logic. It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

SL9011 operates in four basic modes. First and most common, is the CPU mode. This mode is active any time CPUHLDA is low.

The other modes can only be active when CPUHLDA is high. These modes are DMA mode, External Master Mode, or Refresh Mode. If the inputs NAEN1 or NAEN2 are active, the SL9011 is in DMA mode and the command bus is driven from the inputs on the peripheral bus.

### FUNCTIONAL DESCRIPTION

The SL9011 AT System Controller consists of the following sub-modules as illustrated in the Block Diagram.

1. 80X87 Logic
2. Refresh Logic
3. Ready
4. 82288 Bus Controller
5. Reset Logic
6. FSel Logic
7. Bus Conversion Control Logic
8. Clock Control and Clock Generation

The SL9011 PC/AT Compatible System Controller functionally replaces an 82C288 Bus Controller and an 82C84A Clock Generator and Driver.

## 80X87 LOGIC

The 80X87 Logic supplies all the necessary glue logic to support the Intel 80287, 80387SX or 80387DX NPX and the Weitek 3167. The NPX I/O port address is 00F8 through 00FF, RST387 (from SL9025) is effected by an IO write to 00F1. The system signals SA0, SA3, MIO, NIOW, RESET and the SL9025 signal NCS287 are anded together to initiate a NPX reset. Reset logic will hold 387RST true and IOCHRDY false until the appropriate number of CPUCLK cycles have elapsed. The NPX output signal NBUSY is clocked into a "D" register by the NPX output NERROR. The register output is STENO, status enable. STENO is used to gate NPX output PEREQ into CPUPEREQ, as well as input WTKINT into IRQ13. STENO also gates either NBUSY or TIMCLK into NCPUBUSY, as determined by the input OPT387. STENO is true if NBUSY is false when the NPX asserts NERROR. If NBUSY is true when NERRROR is asserted, STENO is latched false and must then be cleared by an I/O write to 00F0.

NPX input NERROR is continuously gated into NCPUERR following the first NADS or NS1 after a CPURST.

## REFRESH LOGIC

The refresh circuitry provides logic to perform the following five functions:

1. Provide REFCLK
2. Provide NMEMR
3. Hold off REFCLK and NMEMR with IOCHRDY
4. Drive NREF
5. Request a CPU hold

A refresh cycle is initiated when the input REFREQ is toggled low to high, causing the request to be latched. DMACLK relatches the request and causes a CPUHOLD request. The relatched request is again latched with SYSCLK. This latched output is anded with HLDA and used to drive NREF. NREF starts the State Machine which performs the following functions in order:

1. Enable REFCLK
2. Generate NMEMR
3. Hold for IOCHRDY
4. Reset Refresh
5. Stop

External refresh request logic may be utilized by tying REFREQ high, and connecting the NREF I/O pin to the external devices request pin. If an SL9030 IPC is used, the refresh line is called NREFRESH.

## READY

The READY circuitry provides the basic function of oring peripheral and memory ready signals and passing them on to the CPU. Additionally, through the selection of the WOPT12 input, MEM/IO wait states may be added to IOCHRDY. See Table 1. IOCHRDY will extend any bus I/O, memory or refresh operation.

READY, Cont'd.

The three ready signals: NREAD0 from the NPX, NWTKRDY from the Weitek NPX, and NRDY from the memory controller, are ored together and gated out directly to NCPURDY. The SLOT signal N0WS is latched by CPUCLK, gated with NCNVRDY (no conversion in progress) relatched with NSYSCLK, then gated out to NCPURDY. The signal IOCHRDY from the SLOT bus is gated with the internal signals 1WS, CNVRDY and wait state counter outputs, such that the wait states per Table 1 are inserted. Delayed IOCHRDY is then latched by SYSCKOUT, relatched by CPUCLK, gated with internal conversion signals, latched by NSYSCKOUT and gated out to NCPURDY.

| WOPT12 | 16 BIT | 8BIT |
|---|---|---|
| 0 | 2 | 6 |
| 1 | 1 | 4 |

Table 1

82288 BUS CONTROLLER

The 82288 Support Logic and 82288 work together to effect a system solution that is 82288 compatible.

Support logic uses the input signals S3N2 and MIO to distinguish between 386 or 286 operation. Inputs NS0, NS1 and MIO are decoded to product the basic outputs NINTA, NIOW, NIOR, NMEMW and NMEMR. NMCS16, XRDY, NDCONV, and ALE are used to generate CMDLY. The inputs HLDA and MASTER are used to generate AEN and disable the outputs for DMA operation.

RESET LOGIC

There are three Reset inputs and three Reset outputs. Two Reset functions are served, I/O and CPU.

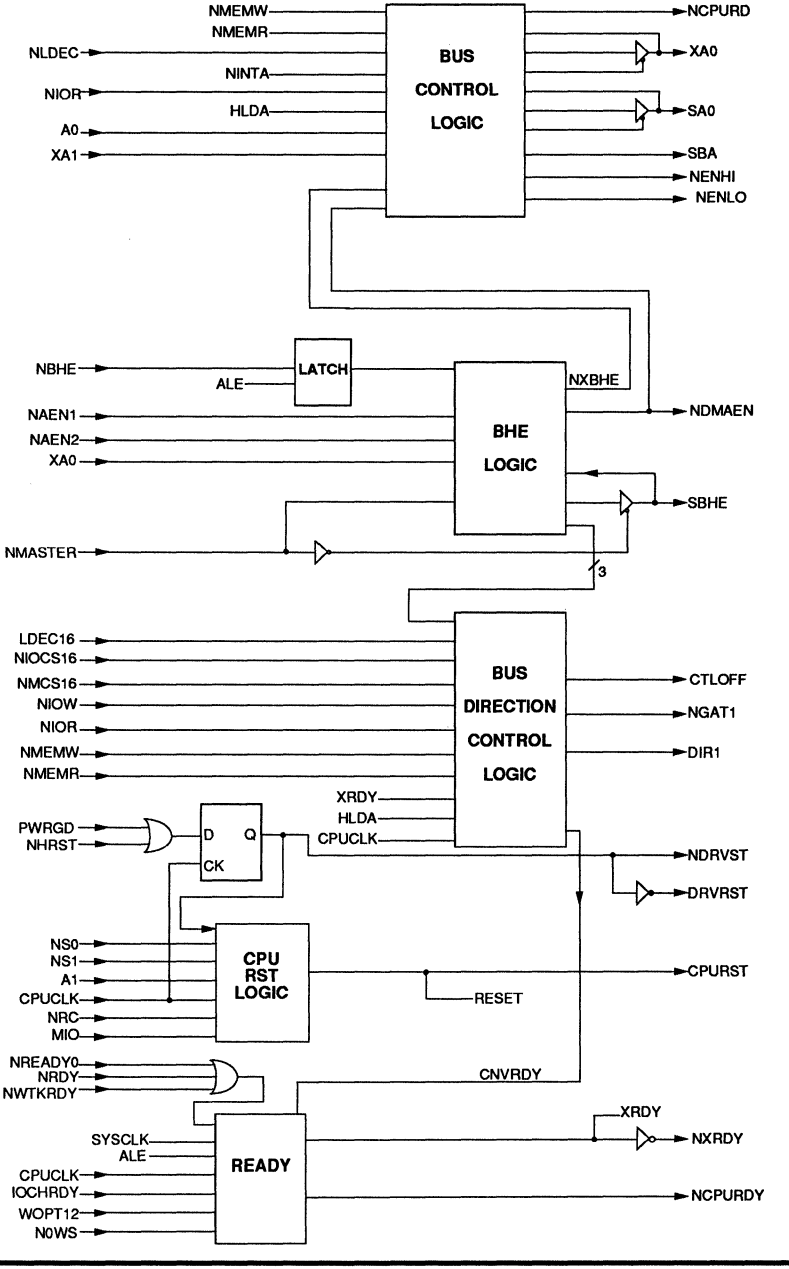
To effect a I/O Reset, inputs PWRGD and NHRST are ored and latched by CPUCLK. The latched output drives NDRVRST and its compliment, DRVRST. These signals are used to reset the slot I/O and keyboard controller. NHRST is a schmidt input and this may be driven with a mechanical switch.

To effect a CPU Reset, the inputs PWRGD and NHRST are ored and latched by CPUCLK. The latched signal is ored with NRC and conditioned with the CPU signals MIO NS0, NS1 and A1 such that the output signal CPURST is driven true synchronously with CPUCLK and is negated to meet the hold and release requirements of the processor.

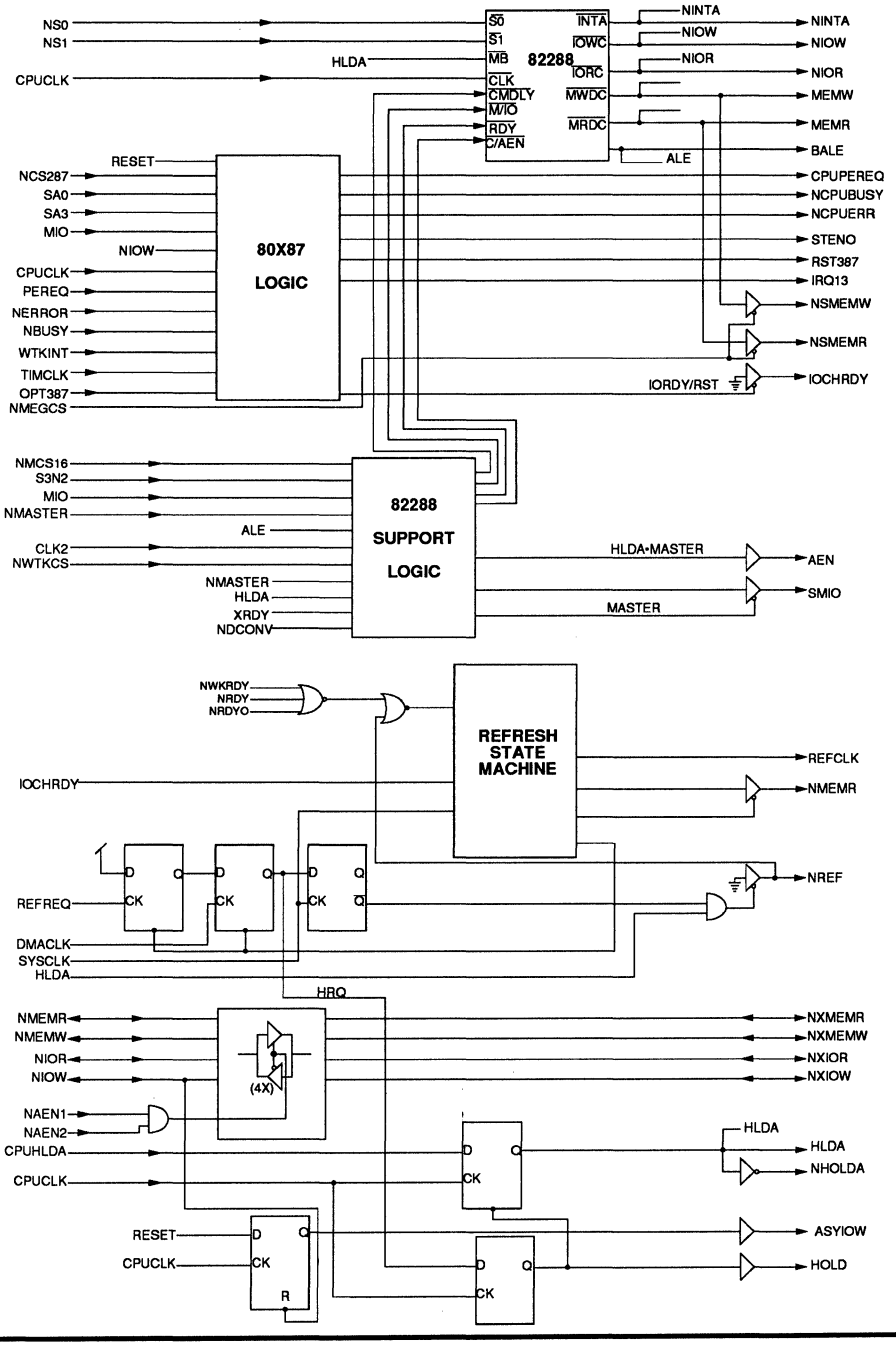
FSEL LOGIC

FSel 1 output is used to drive the FSel Pin on SL9090A. When FSel1=0, the clock CPUCLK slows to 16MHz. When FSel1=1, the clock is selected fast (Reference the 9090A spec). When NFSTDMA is negated, NMASTER or NDMAEN (BUSMASTER or 8 or 16 bit DMA) will clock FSel1=0, and NS0 or NS1 (IO/MEM READ, IO/MEM WRITE) will reset FSel1=0. FSel1 will be set =1 by NADS or Reset. When NFSTDMA is asserted, NDMAEN and NMASTER have no affect on FSel1. NS0 and NS1 Reset FSel1=0 as above, and asserting NADS, RESET or HLDA will set FSel1=1.

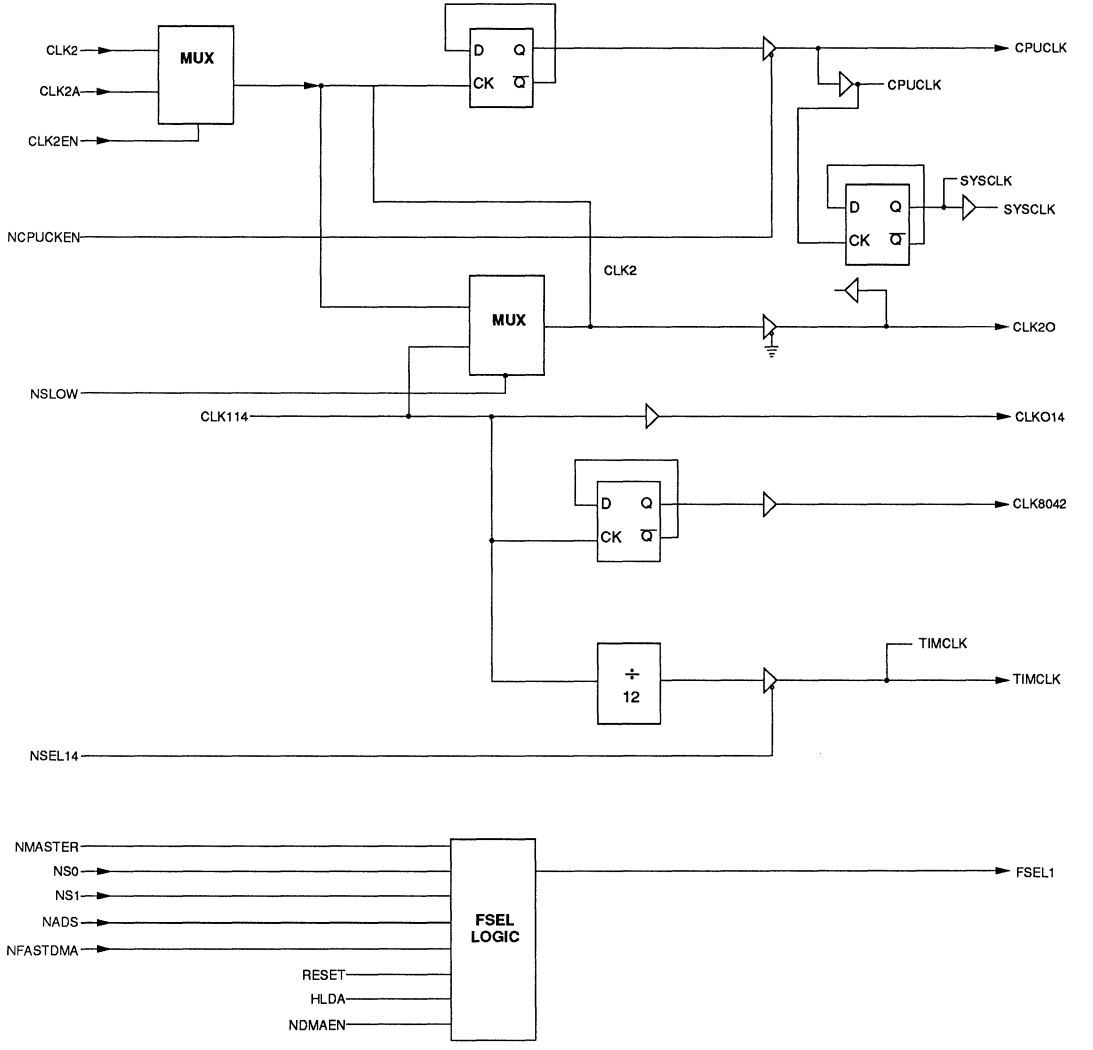
## BLOCK DIAGRAM SL9011



## BLOCK DIAGRAM SL9011, cont'd.



## BLOCK DIAGRAM SL9011, cont'd.



## BUS CONVERSION CONTROL LOGIC

A State Machine for controlling the conversion between 16-bit data accesses from the CPU to 8-bit peripherals is contained in the SL9011. The state machine will generate the control signals DIR1, NGAT1 and CTLOFF to the SL9020 Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to high, and then perform read/write operations for the high data byte.

SL9011 also generates NGAT1 and DIR1 during 8-bit DMA cycles to route the lower byte on the system data bus to or from the high or low byte of the on-board memory.

## CLOCK CONTROL AND CLOCK GENERATION

The SL9011 receives CLK2, CLK2A, and CLKI14 and uses them to generate CLKO14, CPUCLK, CLK8042, CLK2O, TIMCLK and SYSCKOUT. CLK2EN allows for switching between CLK2 and CLK2A. NCPUCKEN and NSEL14 also allow for CPUCLK and TIMCLK to be input externally. CLK2EN and NSLOW can be switched dynamically. SYSCKOUT is synchronized with NADS.

| CLK2EN | NSLOW | CLK2O |
|---|---|---|
| X | 0 | 14 MHz |
| X | 0 | 14 MHz |
| 0 | 1 | CLK2 |
| 1 | 1 | CLK2A |

**Table 2**

## PIN DESCRIPTION SL9011

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A0,1 | 58,60 | I | Local bus least significant address inputs. A0-A1 are generated from CPU BE0-BE3. A0 is used to generate CPURST for shutdown cycle. |
| AEN | 92 | O | DMA Address Enable. When LOW, enables data buffers between XD Bus and SD Bus. It is HIGH during DMA cycles. It is used to drive SLOT AEN and the SL9025 Buffer Control. |
| BALE | 91 | O | Buffered Address Latch Enable. Directly drives AT SLOT signal BALE. |
| CLK2 | 54 | I | TTL Level input from oscillator or clock chip. Has twice the frequency of the CPU clock. It is used to clock 82288 support logic. |
| CLK2A | 14 | I | Input from oscillator. |
| CLK2EN | 5 | I | Clock 2 Enable. Jumper input. When LOW CLK2A is input. When HIGH CLK2 is input. |
| CLK2O | 4 | O | Clock 2 Out. This pin is always output enabled. Depending on jumper combinations [CLK2EN], [NSLOW], CLK2O can be either CLK2, CLK2A or 14MHz. |
| CLK8042 | 33 | O | CLK8042 is CLKI14 divided by two. |
| CLKI14 | 82 | I | Clock In 14 MHz. 14 MHz being input from oscillator. |
| CLKO14 | 79 | O | Clock Out 14 MHz. 14 MHz clock output from the chip. |
| CPUCLK | 29 | I/O | CPU Clock. It is half the frequency of CLK2 or CLK2A. Internally generated output or input from Clock Chip. |
| CPUHLDA | 22 | I | CPU Hold Acknowledge. It is active HIGH when a Bus cycle is granted in response to hold request (HOLD). It is used to generate HLDA and NHOLDA, as well as reset HOLD. |
| CPUPEREQ | 21 | O | CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU. |
| CPURST | 81 | O | Reset Signal to the CPU is an active HIGH output. It is generated in response to any one of the following signals: NHRST, PWRGD and NRC. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| CTLOFF | 72 | O | Control Output Flag. Rising edge clocks data from SD[7:0] to D [7:0] latches during Bus-conversion cycles. Connects directly to the SL9020 pin CTLOFF. |
| DIR1 | 100 | O | Direction 1. Controls data transfer direction between SD[7:0] and SD[15:8] in the SL9020 Data Controller. NGAT1 must be asserted. It is used during data conversions (8bit SLOT Read/Writes). |
| DMAREQ | 47 | I | DMA Request is asserted HIGH to request a DMA cycle. It initiates hold request (HOLD) to the CPU for a DMA cycle to begin. |
| DRVRST | 35 | O | Device Reset is an active HIGH output. When asserted it resets the AT System and the SL9350 Memory Controller. Directly drives the AT SLOT signal DRVRST. |
| FSEL1 | 64 | O | Frequency Select 1. Jumper output. When asserted LOW (when SL9011 is used with SL9090A), SYSCKOUT is slowed down to 8MHz. |
| HLDA | 89 | O | Hold Acknowledge is an active HIGH output to the SL9X5X Memory Controller. When asserted it indicates that CPU has released its control on the local bus in favor of another bus master device (DMA external master). It is generated by resynchronizing CPUHLDA with CPUCLK. |
| HOLD | 20 | O | Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU. |
| IOCHRDY | 51 | I/O | I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT I/O or AT memory cycles. It is used to generate NCPURDY. It is an output during NPX reset cycle. |
| IRQ13 | 12 | O | Interrupt Request 13 is an active HIGH output which indicates an interrupt from the numeric coprocessor. It connects to the SL9030 pin IRQ13. |
| MIO | 26 | I | Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle. It is used to synchronize Reset, drive SMIO, and enable 80X87 operations. |
| NADS | 6 | I | Address Status is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NAEN1,2 | 97,98 | I | DMA Enable 1,2 are active LOW inputs from the SL9030. When NAEN1 is asserted LOW it indicates an 8-bit DMA cycle. When NAEN2 is asserted LOW it indicates a 16-bit DMA cycle. When both are HIGH it indicates that a non-DMA device owns the system's bus controls. They can not be LOW at the same time. They are used to generate direction control signals NSBHE, SBA, NENHI and NENLO. |
| NAMEMW | 48 | I | Advance Memory Write is an active LOW input. It is asserted for local memory write cycles. It is used to enable CPU HOLD. |
| NBHE | 25 | I | Byte High Enable is an active LOW input signal which indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is used to generate NENHI. |
| NBUSY | 1 | I | Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate busy signal to the CPU, NCPUBUSY. |
| NCPUBUSY | 13 | O | CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY. |
| NCPUCKEN | 50 | I | CPU Clock Enable. Jumper input. When LOW CPUCLK is an output. When HIGH CPUCLK is an input. |
| NCPUERR | 10 | O | CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU. |
| NCPURD | 24 | O | CPU Read is an active LOW output to the SL9020 that sets the direction of data between D0-D15 and SD0-SD15. When asserted, the direction is from SD to D. |
| NCPURDY | 27 | O | CPU Ready is an active LOW output which goes to CPU's ready input. When asserted, CPU terminates its current bus cycle. IC or S memory, I/O and NPX Ready signals. |
| NCS287 | 9 | I | NPX Chip Select is an active LOW input which is asserted for I/O port addresses 00F0 through 00FF. It is connected to the SL9025 Address Controller pin NCS287. |
| NDMAEN | 94 | O | DMA Enable is an active LOW output to the SL9025 Address Controller. When asserted it indicates a DMA cycle is in progress; either 8-bit or 16-bit. It gates XA1-XA16 onto SA1-SA16 for a DMA operation. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NDRVRST | 55 | O | Device Reset is an active LOW output. It is the compliment of DRVRST. It is used to reset the SL9025 Address Controller. |
| NENHI | 18 | O | Enable High byte to the SL9020 Data Controller, is asserted LOW to enable HIGH byte data transfer between D Bus and SD Bus. |
| NENLO | 19 | O | Enable Low byte to the SL9020 Data Controller, is asserted LOW to enable LOW byte data transfers between D Bus and SD Bus. |
| NERROR | 2 | I | NPX Error is an active LOW input from 80X87. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR. |
| NFSTDMA | 75 | I | Fast DMA. Jumper input. When LOW slows down I/O, and external memory access only. SYSCLK is at one half of CPUCLK. When HIGH SYSCLK slows down for I/O, and external memory, DMA and NMASTER. |
| NGAT1 | 73 | O | Gate 1 is asserted LOW to enable the data buffer between HIGH byte and LOW byte of SD Bus. It is used in bus conversion cycles to assemble 8 bit bytes into 16 bit words in the SL9020 Data Controller. |
| NHOLDA | 80 | O | When asserted NHOLDA indicates that CPU has released its buses and controls on the local bus in favor of another bus master device (DMA/External Master). It is used by the SL9025 to gate SA1-SA16 into A1-A16 during DMA. It is the compliment of HLDA. |
| NHRST | 77 | I | Forcing Hardware Reset LOW generates a systems reset (CPURST, DRVRST and NDRVRST). It is a schmidt input and may be connected to a mechanical switch. |
| NIOCS16 | 96 | I/O | Input/Output Chip select 16 is an active LOW input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGAT1. |
| NINTA | 41 | O | Interrupt Acknowledge is an active LOW output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during an interrupt acknowledge cycle. |
| NIOR | 37 | I/O | Input/Output Read is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NIOW | 36 | I/O | Input/Output Write is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle. It is used for 80X87 support. |
| NLDEC | 56 | I | Local Decode is an active LOW input for the SL9X5X. When active it indicates a local memory transfer. It is used to determine NCPURD direction. |
| NLMEGCS | 23 | I | Lower 1 Meg Chip Select is an active LOW, when asserted it indicated that lower 1 meg memory is being selected. It is used to tri-state enable NSMEMR and NSMEMW. |
| NMASTER | 93 | I | External Master is an active LOW input from the AT bus. When asserted, indicates that an external master device is currently active. |
| NMCS16 | 95 | I | Memory Chip Select 16 is an active LOW input from the AT bus. When asserted indicates a 16 bit memory cycle. When HIGH it implies an 8-bit memory transfer. It is used to control NGAT1. |
| NMEMR | 39 | I/O | Memory Read is an active LOW bi-directional pin on the AT System bus. It is an output during CPU, DMA and refresh cycles. It is an input when an external master is active on the AT bus. |
| NMEMW | 38 | I/O | Memory Write is an active LOW bi-directional pin on the AT System bus. It is an output during CPU and DMA cycles. It is an input when an external master is active on the AT bus. |
| N0WS | 49 | I | Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle, at the first Tc 02 (286) or T2 02 (386). |
| NRC | 84 | I | External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURST. It may come from a debounced switch. |
| NRDYO | 44 | I | Ready O is an active LOW input from the NPX to terminate an NPX bus cycle. It generates an NCPURDY. |
| NRDY | 45 | I | Ready is an active LOW input. It is asserted for 32-bit local memory cycles and 16-bit ROM cycles for 386 based systems. For 386SX or 286 it is asserted for 16-bit local memory cycles and 16-bit ROM cycles. It generates an NCPURDY. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NREF | 43 | I/O | Refresh is an active LOW bi-directional pin. It is input at all other times. It connects to the SL9350 pin NREFRESH and to the SL9030 pin NREFRESH. |
| NS0,1 | 85,86 | I | Status1,0 are active LOW inputs from the memory controller. They are used by the system to determine the type of bus cycle. (Write, Read, Idle or INTA). |
| NSBHE | 63 | I/O | Byte High Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle. |
| NSEL14 | 32 | I | Select 14. Jumper input. When LOW [TIMCLK] is output. When HIGH [TIMCLK] is input. |
| NSLOW | 83 | I | Jumper input. When LOW selects 14 MHz and outputs that as [CLK2O]. When HIGH it outputs [CLK2] or [CLK2A] as [CLK2O]. |
| NSMEMR | 88 | O | System Memory Read is an active LOW tri-state output for the AT bus. It is an output for CPU, DMA and refresh cycles. It goes to tri-state when lower 1 meg memory is accessed. |
| NSMEMW | 87 | O | System Memory Write is an active LOW tri-state output for the AT bus. It is an output for CPU and DMA cycles. It goes tri-state when lower 1 meg memory is accessed. |
| NWTKCS | 34 | I | Weitek Chip Select is an active LOW input. When asserted it disables AT bus controller to allow NPX enough time to complete an NPX bus cycle. It connects to the NPX pin - MCS. |
| NWTKRDY | 46 | I | Weitek Ready is an active LOW input to terminate an NPX bus cycle. It is used to generate NCPURDY. |
| NXIOR | 69 | I/O | Peripheral Bus Input/Output Read is an active LOW bi-directional pin. It is an output for CPU, refresh and external master cycles. It is an input for DMA cycles. |
| NXIOW | 70 | I/O | Peripheral Bus Input/Output Write is an active LOW bi-directional pin. It is an output for CPU, refresh and external master cycles. It is an input for DMA cycles. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NXMEMR | 67 | I/O | Peripheral Bus Memory Read is an active LOW input for DMA cycles. It is used to generate NSMEMR and NMEMR signals during DMA cycles. All other operations (CPU memory read, Refresh, MASTER) will output NMEMR on this line. |
| NXMEMW | 68 | I/O | Peripheral Bus Memory Write is an active LOW output for CPU, refresh and external master cycles. It is an input for DMA cycles. |
| NXRDY | 71 | O | Ready is an active LOW output to the SL9025 Address Controller. When asserted it indicates termination of a CPU/SLOT bus cycle. It also resets AT's bus cycle state machine. |
| OPT387 | 99 | I | Option 387 is a jumper select input. When HIGH, allows the NPX NBUSY to pass through to NCPUBUSY. Else TIMCLK appears on NCPUBUSY. |
| PEREQ | 8 | I | NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from it's data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated. |
| PWRGD | 76 | I | Power Good is an active HIGH input from the power supply. Negating it will cause NDRVRST, DRVRST and CPURST to assert. |
| REFCLK | 42 | O | Refresh Clock is an active LOW output asserted during refresh cycle for three SYSCKOUT cycles. It drives the SL9025 pin NREF1. |
| RST387 | 52 | O | Reset 387 is an active HIGH output. It is asserted when I/O port 00F1 is written onto. The signal is active for 96 CPUCLK cycles. |
| S3N2 | 30 | I | 386/286 Mode Select. It is a jumper option. It is HIGH for 386DX or 386SX based systems and LOW for 286 based systems. |
| SA0 | 66 | I/O | System Bus Address 0-bit. It is a bi-directional pin. It is an output for CPU, Refresh and DMA operations, and an input for Master operation. It is used for 80X87 support. |
| SA3 | 59 | I | System Bus Address 3-bit. It is used for 80X87 support. |
| SBA | 17 | O | Select Data Buffer Data. This signal drives the SL9020 Data Controller. When HIGH it selects latched SD Bus LOW byte data during bus conversions cycles. When HIGH, unlatched SD Bus LOW byte data will pass onto D Bus. |

## PIN DESCRIPTION SL9011 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SMIO | 62 | I/O | Memory Input/Output for the System Bus. When HIGH it indicates a memory cycle. When LOW it indicates an I/O cycle. Tri-stated when master is asserted. This signal is not normally used in an AT. |
| STENO | 11 | O | Status Enable is an active HIGH output. This pin serves as a chip select for the 80X87. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state. |
| SYSCKOUT | 16 | O | System Clock Out is a free running system clock generated by dividing CPUCLK by 2. It uses NADS to synchronize itself to the CPUCLK upon power up during the first CPU cycle. Odd numbers of wait states will also cause SYSCKOUT to resynchronize in subsequent cycles. |
| TIMCLK | 7 | I/O | 1.19 MHz Timer Clock is an input from the clock chip, or internally generated timer clock being output. |
| VDD | 3,28,53,78 | - | +5V. Power. |
| VSS | 15,40,65,90 | - | 0V. Ground. |
| WOPT12 | 74 | I | Wait State Option 1,2 is a jumper option. When HIGH it allows 1 wait state for 16-bit memory/IO and 4 wait states for 8-bit memory/IO cycles. When LOW it allows 2 wait states for 16-bit memory/IO and 6 wait states for 8-bit memory/IO cycles. |
| WTKINT | 31 | I | Weitek Interrupt is an active HIGH input which asserts IRQ13. It connects directly to NPX pin INTR. |
| XA0 | 61 | I/O | Peripheral Bus Address Line 0 is a bi-directional pin. It is an output for CPU, refresh and external master cycles and an input for DMA cycles. It is gated onto the SA Bus during DMA operation. |
| XA1 | 57 | I | Peripheral Bus Address Line 1 is an input used in generating NENLO and NENHI. It must be tied LOW for 386SX based systems. |

## ABSOLUT MAXIMUM RATINGS SL9011 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current *note 2 | $I_{OS}$ | -40 | +40 | mA |
| Output Current *note 3 | $I_{OS}$ | -40 | +80 | mA |
| Output Current *note 4 | $I_{OS}$ | -60 | +120 | mA |
| Output Current *note 5 | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All other outputs.
3. NINTA, NDRVRST, CPURST, SYSCKOUT, CLK2O, CPUCLK.
4. NMEMR/W, NIOR/W, NXMEMR/W, NXIOR/W, NSMEMW/R, HLDA, BALE, AEN, IOCHRDY, NREF, SMIO, NSBHE, XA0, SA0 .
5. DRVRST.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9011

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state* |
| Output High Voltage for Normal Output (IOL = 3.2 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 8 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 12 mA) | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output (IOL = 24 mA) | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output (IOL = 3.2 mA) | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output (IOL = 8 mA) | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output (IOL = 12 mA) | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output (IOL = 24mA) | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for Normal Input | VIH | 2.2 | | V | |
| Input Low Voltage for Normal Input | VIL | | 0.8 | V | |
| Input High Voltage for CMOS Input | VIH | 0.7VDD | | V | |
| Input Low Voltage for CMOS Input | VIL | 0.3VDD | | V | |
| Input Leakage Current | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD |

NOTES:

* VIH = VDD, VIL = Vss

| | |
|---|---|
| DRVRST | = 24mA |
| NMEMR/W, NIOR/W, NXMEMR/W, NXIOR/W, NSMEMW/R, HLDA, BALE, AEN, IOCHRDY, NREF, SMIO, NSBHE, XA0, SA0 | = 12mA |
| NINTA, NDRVRST, CPURST, SYSCKOUT, CLK2O, CPUCLK | = 8mA |
| ALL OTHER OUTPUTS | = 3.2 mA |

## AC CHARACTERISTICS SL9011

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| t1 | CLK2 Period | 25 | - | ns |
| t2 | CLK2 High Duration | 7 | - | ns |
| t2a | CLK2 Low Duration | 7 | - | ns |
| t3 | CPUCLK Period | 50 | - | ns |
| t4 | CPUCLK High Duration | 14 | - | ns |
| t4a | CPUCLK Low Duration | 14 | - | ns |
| t5 | CPUCLK Falling Edge to SYSCKOUT (High to Low) | - | 9.5 | ns |
| t5a | CPUCLK Falling Edge to SYSCKOUT (Low to High) | - | 9.5 | ns |
| t6 | CLK2 High to NADVALE (Low) | - | 4.0 | ns |
| t6a | CLK2 High to NADVALE (High) | - | 4.0 | ns |
| t7 | NS0,1 Set-up time to CPUCLK Falling Edge | 7.0 | - | ns |
| t8 | CPUCLK Falling Edge to BALE (Low to High) | - | 7.5 | ns |
| t8a | CPUCLK Falling Edge to BALE (High to Low) | - | 7.5 | ns |
| t9 | N0WS Set-up time to CPUCLK Rising Edge | 5.7 | - | ns |
| t10 | CPUCLK Falling Edge to NMEMW (High to Low) | - | 16.7 | ns |
| t10a | CPUCLK Falling Edge to NMEMW (Low to High) | - | 16.7 | ns |
| t11 | SYSCKOUT Falling Edge to NCPURDY (High to Low) | - | 6.0 | ns |
| t11a | CLK2 Rising Edge to NCPURDY (Low to High) | - | 15.5 | ns |
| t12 | NMCS16 Set-up time to CPUCLK Rising Edge | 7.5 | - | ns |
| t13 | IOCHRDY Set-up time to SYSCKOUT Rising Edge | 10 | - | ns |
| t13a | IOCHRDY Hold Time to SYSCKOUT Rising Edge | 5 | - | ns |
| t14 | NIOCS16 Set-up time to CPUCLK Rising Edge | 7.5 | - | ns |
| t15 | PWRGD Set-up time to CPUCLK Rising Edge | 6.0 | - | ns |
| t15a | NHRST Set-up time to CPUCLK Rising Edge | 6.0 | - | ns |
| t16 | CPUCLK Rising Edge to CPURST (High) | - | 12.0 | ns |
| t16a | CPUCLK Rising Edge to CPURST (Low) | - | 12.0 | ns |
| t17 | CPUCLK Rising Edge to RST387 (High) | - | 9.0 | ns |
| t17a | CPUCLK Rising Edge to RST387 (Low) | - | 9.0 | ns |
| t18 | WTKINT to IRQ13 (Low to High) | - | 5.0 | ns |
| t18a | WTKINT to IRQ13 (High to Low) | - | 5.0 | ns |
| t19 | CLK2 Rising Edge to SMIO (High to Low) | - | 15.5 | ns |
| t19a | CLK2 Rising Edge to SMIO (Low to High) | - | 16.0 | ns |
| t20 | CLK2 Rising Edge to NSBHE (High to Low) | - | 18.5 | ns |
| t20a | CLK2 Rising Edge to NSBHE (Low to High) | - | 19.0 | ns |
| t21 | CLK2 Rising Edge to SA0 (High to Low) | - | 18.5 | ns |
| t21a | CLK2 Rising Edge to SA0 (Low to High) | - | 19.0 | ns |
| t22 | NADS Set-up time to CLK2 Rising Edge | 9.0 | - | ns |
| t23 | DMAREQ Set-up time to CPUCLK Rising Edge | 3.0 | - | ns |
| t24 | REFREQ Set-up time to CPUCLK Rising Edge | 3.0 | - | ns |

## AC CHARACTERISTICs SL9011 (Cont'd.)

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| t25 | CPUCLK Rising Edge to NREF (Low to High) | - | 20.0 | ns |
| t25a | CPUCLK Rising Edge to NREF (High to Low) | - | 20.0 | ns |
| t26 | NREF Set-up time to CPUCLK Rising Edge | 5.0 | - | ns |
| t27 | CPUCLK Rising Edge to NXRDY (High to Low) | - | 15.0 | ns |
| t27a | CPUCLK Rising Edge to NXRDY (Low to High) | - | 15.0 | ns |
| t28 | CPUCLK Falling Edge to CTLOFF (Low to High) | - | 10.0 | ns |
| t28a | CPUCLK Falling Edge to CTLOFF (High to Low) | - | 10.0 | ns |
| t29 | NWTKCS Set-up time to CPUCLK Rising Edge | 5.0 | - | ns |
| t30 | CPUCLK Falling Edge to NGAT1 (High to Low) | - | 30.0 | ns |
| t30a | CPUCLK Falling Edge to NGAT1 (Low to High) | - | 30.0 | ns |
| t31 | CPUCLK Falling Edge to DIR1 (High to Low) | - | 27.0 | ns |
| t31a | CPUCLK Falling Edge to DIR1 (Low to High) | - | 27.0 | ns |
| t32 | CPUCLK Falling Edge to NINTA (High to Low) | - | 14.0 | ns |
| t32a | CPUCLK Falling Edge to NINTA (Low to High) | - | 14.0 | ns |
| t33 | CPUHLDA Set-up time to CPUCLK Falling Edge | 6.0 | - | ns |
| t34 | CPUCLK Falling Edge to NSMEMW (High to Low) | - | 19.0 | ns |
| t34a | CPUCLK Falling Edge to NSMEMW (Low to High) | - | 19.0 | ns |
| t35 | CPUCLK Falling Edge to NSMEMR (High to Low) | - | 20.0 | ns |
| t35a | CPUCLK Falling Edge to NSMEMR (Low to High) | - | 20.0 | ns |
| t36 | CPUCLK Falling Edge to ASYIOW (High to Low) | - | 10.0 | ns |
| t36a | CPUCLK Falling Edge to ASYIOW (Low to High) | - | 10.0 | ns |
| t37 | CPUCLK Falling Edge to HLDA (Low to High) | - | 6.0 | ns |
| t37a | CPUCLK Falling Edge to HLDA (High to Low) | - | 6.0 | ns |
| t38 | CPUCLK Falling Edge to NHOLDA (High to Low) | - | 6.6 | ns |
| t38a | CPUCLK Falling Edge to NHOLDA (Low to High) | - | 6.6 | ns |
| t39 | CPUCLK Rising Edge to DRVRST (Low to High) | - | 11.0 | ns |
| t39a | CPUCLK Rising Edge to DRVRST (High to Low) | - | 11.0 | ns |
| t40 | CPUCLK Rising Edge to NDRVRST (High to Low) | - | 12.0 | ns |
| t40a | CPUCLK Rising Edge to NDRVRST (Low to High) | - | 12.0 | ns |
| t41 | CPUCLK Rising Edge to NCPURD (High to Low) | - | 22.0 | ns |
| t41a | CPUCLK Rising Edge to NCPURD (Low to High) | - | 22.0 | ns |
| t42 | CPUCLK Rising Edge to SBA (High to Low) | - | 12.0 | ns |
| t42a | CPUCLK Rising Edge to SBA (Low to High) | - | 12.0 | ns |
| t43 | CPUCLK Rising Edge to NENHI (High to Low) | - | 18.0 | ns |
| t43a | CPUCLK Rising Edge to NENHI (Low to High) | - | 18.0 | ns |

## AC CHARACTERISTICS SL9011 (Cont'd.)

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| t44 | CPUCLK Rising Edge to NENLO (High to Low) | - | 20.0 | ns |
| t44a | CPUCLK Rising Edge to NENLO (Low to High) | - | 20.0 | ns |
| t45 | SYSCKOUT Rising Edge to REFCLK (High to Low) | - | 12.0 | ns |
| t45a | SYSCKOUT Rising Edge to REFCLK (Low to High) | - | 12.0 | ns |
| t46 | NLMEGCS asserted Low to NSMEMW enable | - | 7.0 | ns |
| t46a | NLMEGCS asserted High to NSMEMW Tri-state | - | 8.5 | ns |
| t47 | NLMEGCS asserted Low to NSMEMR enable | - | 7.0 | ns |
| t47a | NLMEGCS asserted High to NSMEMR Tri-state | - | 8.5 | ns |
| t48 | NMASTER asserted Low to AEN (Low to High) | - | 6.5 | ns |
| t48a | NMASTER asserted High to AEN (High to Low) | - | 6.5 | ns |
| t49 | NAEN1 asserted Low to NDMAEN (High to Low) | - | 6.0 | ns |
| t49a | NAEN1 asserted High to NDMAEN (Low to High) | - | 6.0 | ns |
| t50 | NAEN2 asserted Low to NDMAEN (High to Low) | - | 6.0 | ns |
| t50a | NAEN2 asserted High to NDMAEN (Low to High) | - | 6.0 | ns |
| t51 | SA0 to XA0 delay (High to Low) | - | 10.0 | ns |
| t51a | SA0 to XA0 delay (Low to High) | - | 10.0 | ns |
| t52 | XA0 to NSBHE delay (High to Low) | - | 12.0 | ns |
| t52a | XA0 to NSBHE delay (Low to High) | - | 12.0 | ns |
| t53 | NBUSY to NCPUBUSY delay (High to Low) | - | 8.0 | ns |
| t53a | NBUSY to NCPUBUSY delay (Low to High) | - | 8.0 | ns |
| t54 | PEREQ to CPUPEREQ delay (Low to High) | - | 7.0 | ns |
| t54a | PEREQ to CPUPEREQ delay (High to Low) | - | 7.0 | ns |
| t55 | NERROR to NCPUERR delay (High to Low) | - | 7.0 | ns |
| t55a | NERROR to NCPUERR delay (Low to High) | - | 7.0 | ns |
| t56 | NERROR Rising Edge to STENO (High to Low) | - | 10.0 | ns |
| t57 | NCS287 asserted Low to STENO delay (Low to High) | - | 17.0 | ns |
| t58 | NRDYO asserted Low to NCPURDY (High to Low) | - | 6.4 | ns |
| t58a | NRDYO asserted High to NCPURDY (Low to High) | - | 6.4 | ns |
| t59 | NRDY asserted Low to NCPURDY (High to Low) | - | 7.0 | ns |
| t59a | NRDY asserted High to NCPURDY (Low to High) | - | 7.0 | ns |
| t60 | NWTKRDY asserted Low to NCPURDY (High to Low) | - | 7.0 | ns |
| t60a | NWTKRDY asserted High to NCPURDY (Low to High) | - | 7.0 | ns |

## AC TIMING DIAGRAMS SL9011

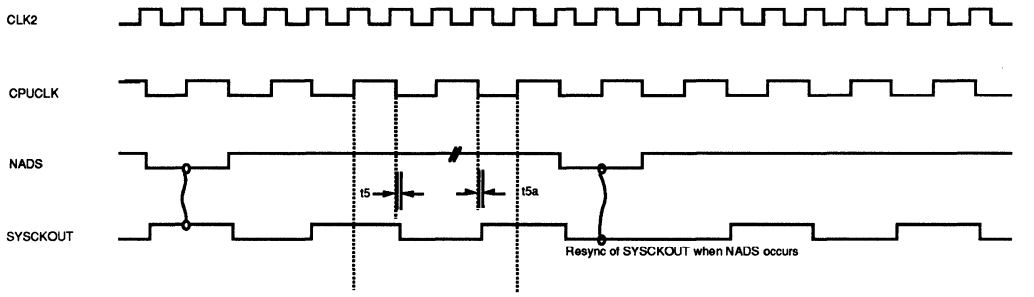
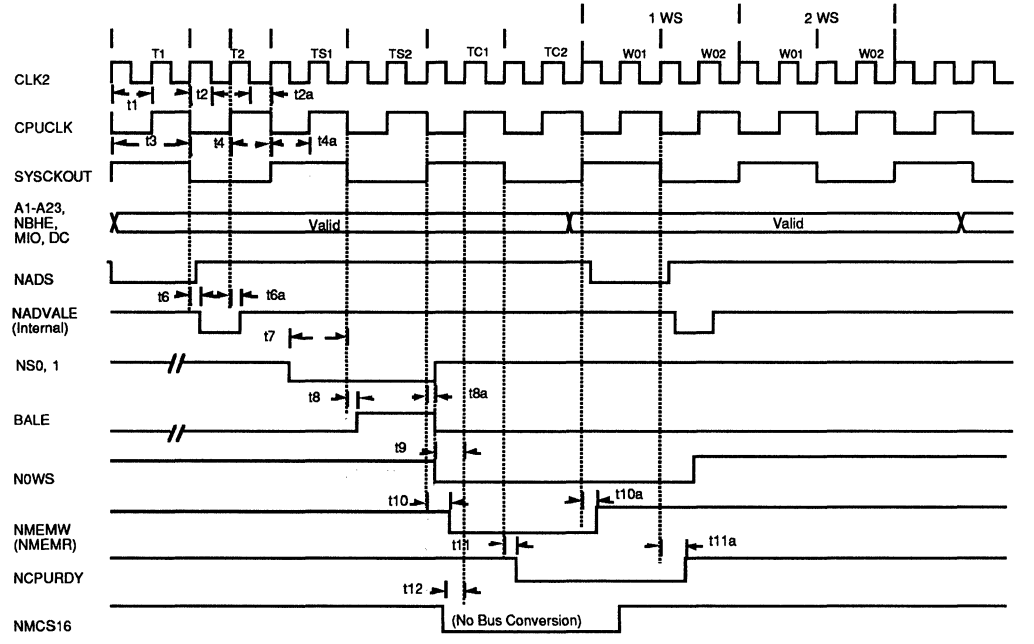



Figure 1. SYSKOUT and DMACLK Relationships with CPUCLK SYSCKOUT Synchronization with the Assertion of NADS




NOTES:

1. N0WS active setup to CPUCLK rising edge is to ensure AT (ISA) 0 wait state cycle.
2. NADVALE is internal to SL9011.
3. NMCS16 setup ensures that no Bus conversion cycle takes place.
4. NMEMR delay from CPUCLK falling edge is same as NMEMW (t10, t10a).
5. NMCS16 or NIOCS16 is not latched inside SL9011. It is sampled every rising edge of CPUCLK and must stay asserted for the duration of the ISA Bus cycle.
6. CMD DELAY is asserted for all 8 or 16 bit I/O cycles and 8 bit memory cycles.

Figure 2. 16 Bit External Memory Cycle, 0 Wait State Non-Pipelined

## AC TIMING DIAGRAMS SL9011

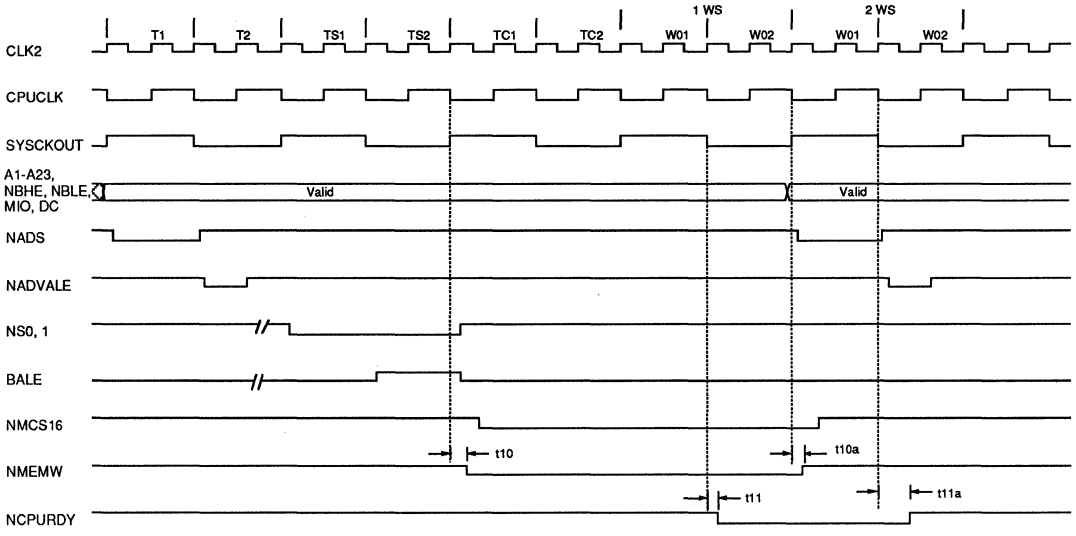



Figure 3. 16-Bit External Memory Cycle, 1 Wait State Non-Pipelined

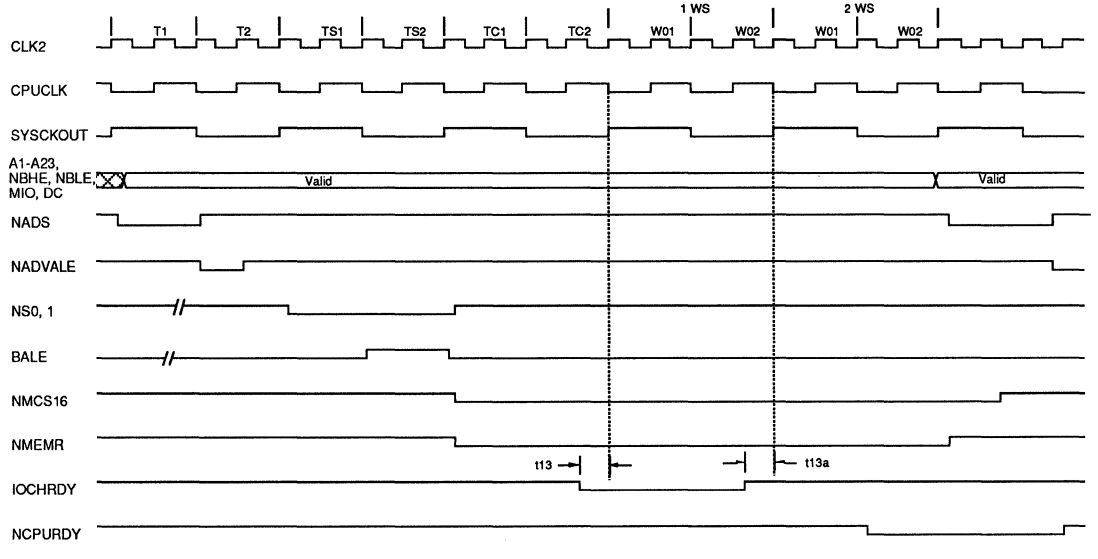



Figure 4. 16-Bit External Memory Cycle, 2 Wait State Using IOCHRDY to Extend the Cycle Non-Pipelined

## AC TIMING DIAGRAMS SL9011

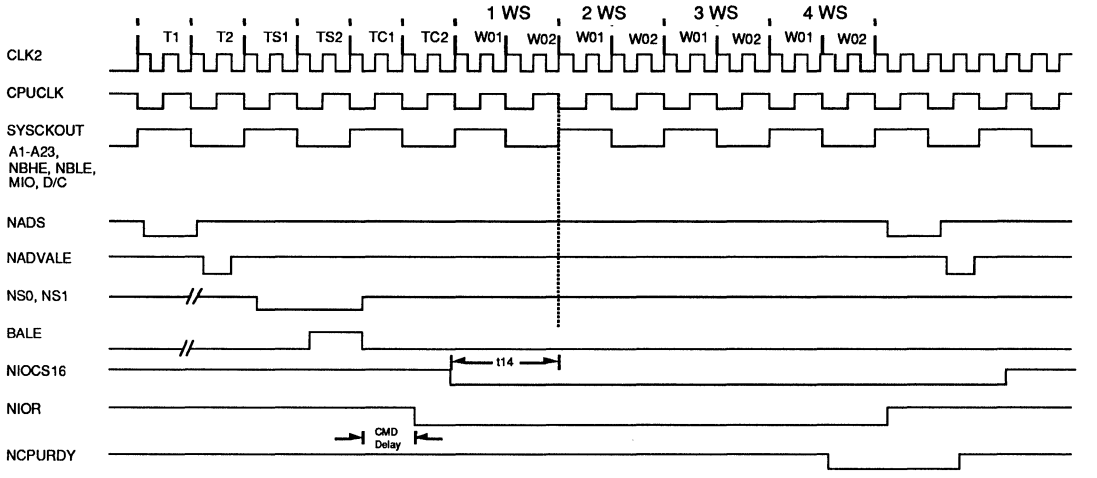



Figure 5. 16-Bit External I/O Cycle with 4 Wait States Non-Pipelined

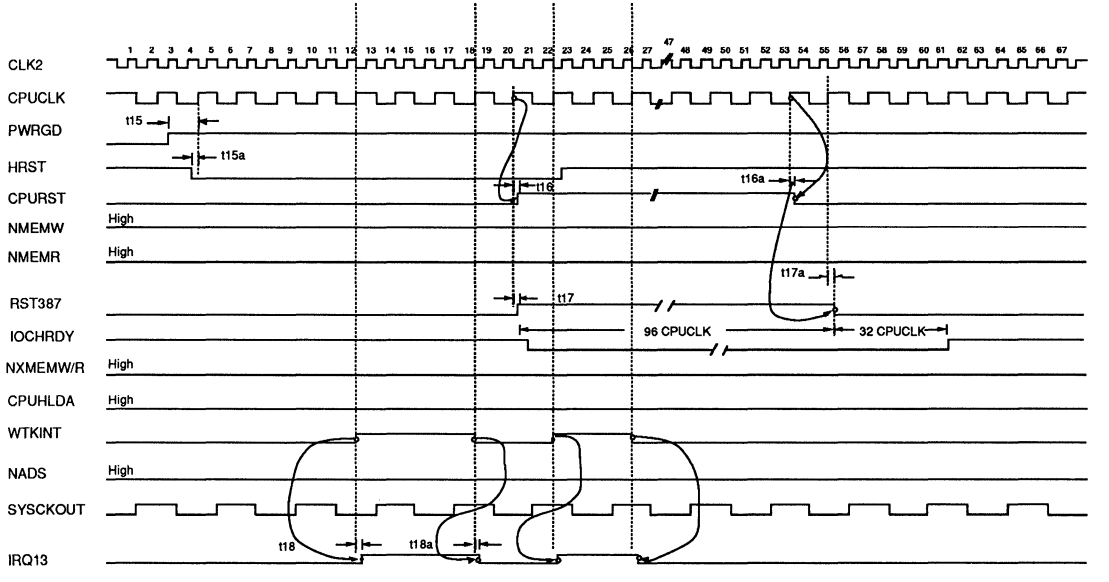



Figure 6. RESET, CPURST, DMACKOUT, SYSCKOUT TIMINGS WTKINT AND IRQ13 RELATIONSHIP

## AC TIMING DIAGRAMS SL9011

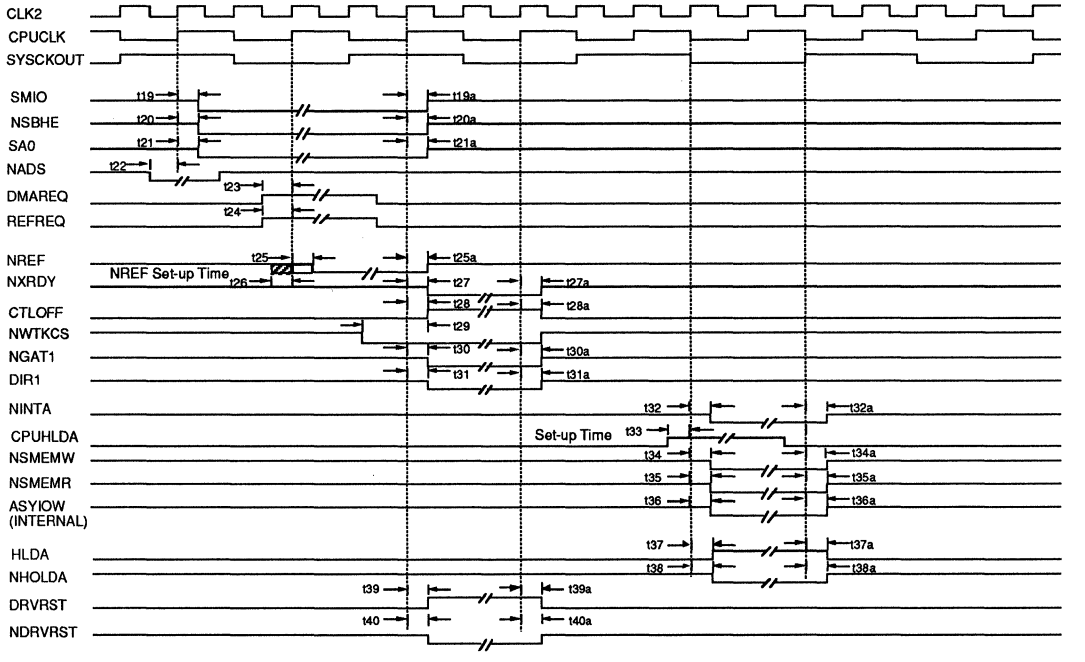



Figure 7. Set-Up Times and Output Signal Delays from CLK2 or CPUCLK

## AC TIMING DIAGRAMS SL9011

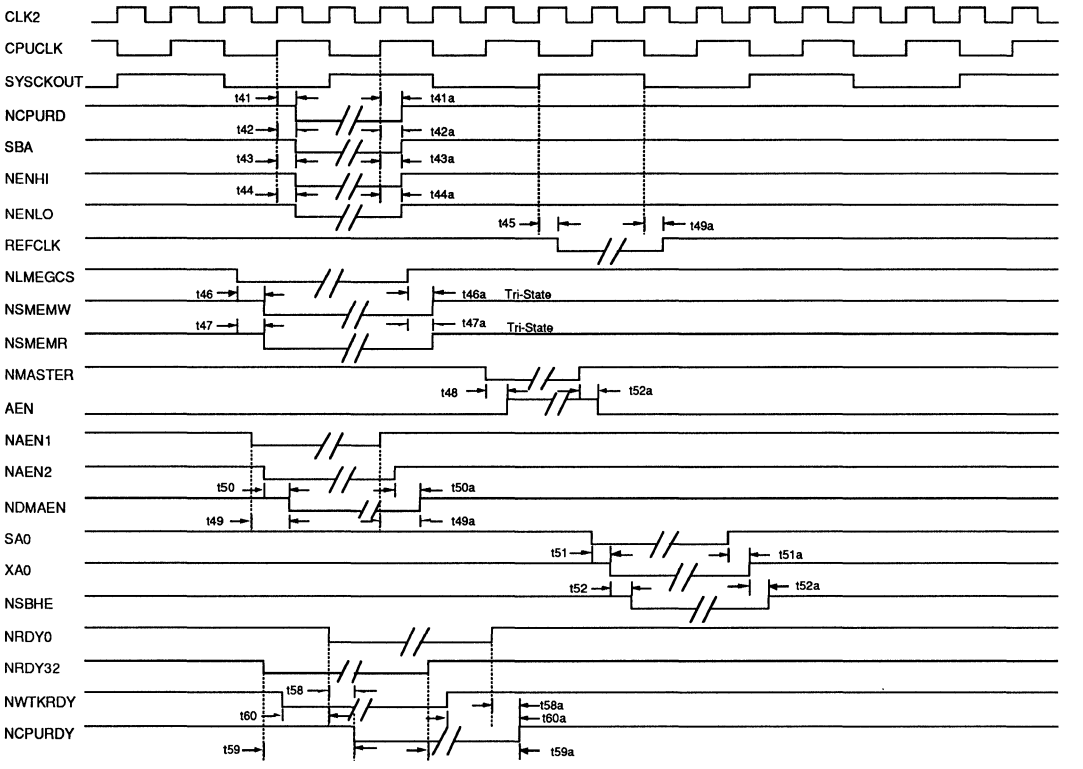



Figure 8. Output Signal Delays from CPUCLK and NCPURDY Delays

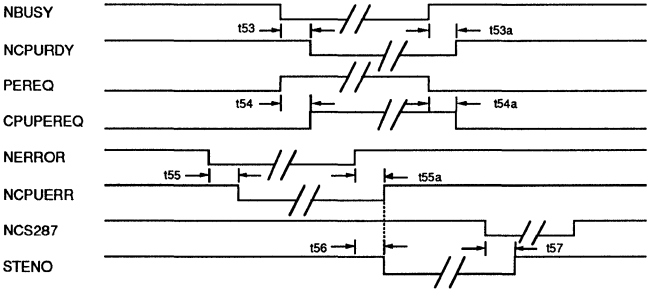
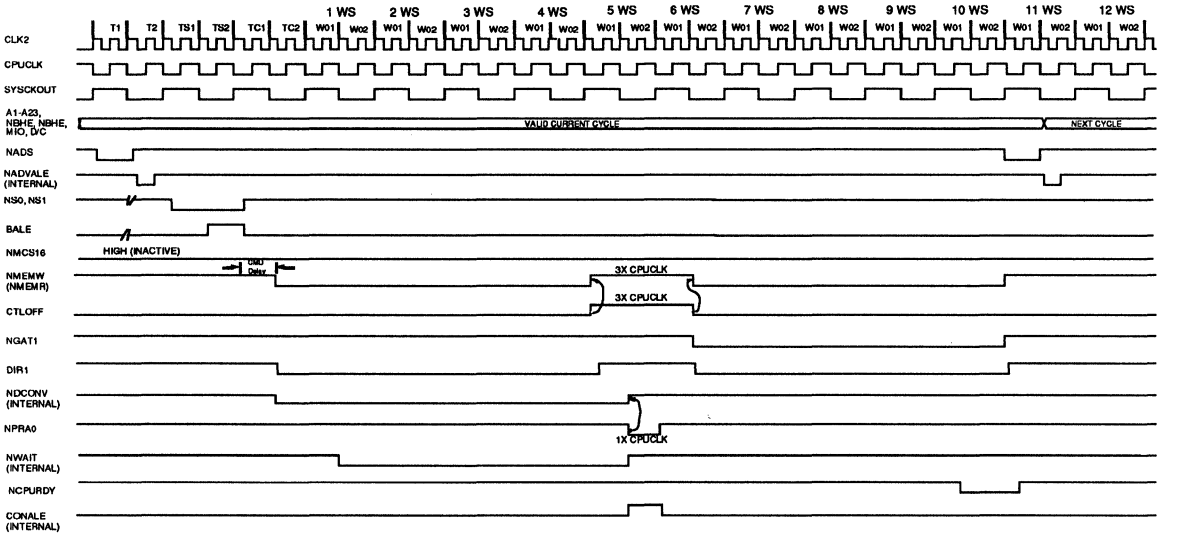



Figure 9. NPX Cycle Input to Output Signal Delays

## AC TIMING DIAGRAMS SL9011




NOTES:
1. NPRA0 changes SA0 from logical 0 to logical 1.
2. CTLOFF and NWAIT keep NCPURDY deasserted.
3. CONALE resets the wait state state machine.
4. NGAT1 and DIR1 transfer data from SD[15:8] to SD[7:0]. NENLO=1.

**Figure 10. 8 Bit External Memory Bus Conversion Cycles (non-pipelined)**

## FEATURES

- **Supports 80286, 80386SX, 80386DX, and 80486-based AT Designs.**
- **Data In to Data Out: 15 ns.**
- **24 mA Output Buffers for SD Bus.**
- **Includes MD, SD & XD Buffers.**
- **16 bit Data Path can be Used as Low or High Buffer.**
- **Two SL9020 are Used in Tandem to Support 32 bit Data Bus.**
- **Low to High byte Transfer.**
- **Latches Provided for Cache Designs.**
- **Fast Memory to CPU Data Path.**
- **Advance CMOS Technology.**
- **100 pin Flatpack.**

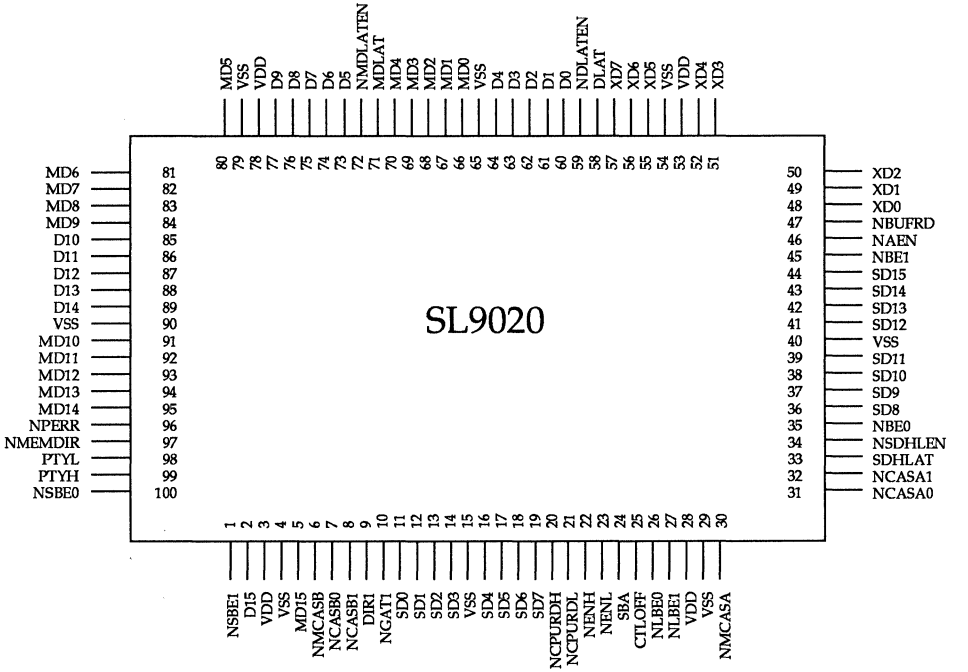
## DESCRIPTION

The SL9020 Data Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9020 is part of the Core AT Logic chips that implement the system logic which is common to all microprocessors such as 80286, 80386SX, 80386DX and 80486-based PC/AT designs and supports up to 25 MHz performance. In addition to the SL9020, the Core AT Logic chips consists of the SL9011 System Controller, the SL9025 Address Controller, the SL9030 Integrated Peripheral Controller and the SL9X5X Memory Controller.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

## PINOUT


SL9020
1 NSBE1
2 D15
3 VDD
4 VSS
5 MD15
6 NMCASB
7 NCASB0
8 NCASB1
9 DIR1
10 NGAT1
11 SD0
12 SD1
13 SD2
14 SD3
15 VSS
16 SD4
17 SD5
18 SD6
19 SD7
20 NCPURDH
21 NCPURDL
22 NENH
23 NENL
24 SBA
25 CTLOFF
26 NLBE0
27 NLBE1
28 VDD
29 VSS
30 NMCASA
31 NCASA0
32 NCASA1
33 SDHLAT
34 NSDHLEN
35 NBE0
36 SD8
37 SD9
38 SD10
39 SD11
40 VSS
41 SD12
42 SD13
43 SD14
44 SD15
45 NBE1
46 NAEN
47 NBUFRD
48 XD0
49 XD1
50 XD2
51 XD3
52 XD4
53 VDD
54 VSS
55 XD5
56 XD6
57 XD7
58 DLAT
59 NDLATEN
60 D0
61 D1
62 D2
63 D3
64 D4
65 VSS
66 MD0
67 MD1
68 MD2
69 MD3
70 MD4
71 MDLAT
72 NMDLATEN
73 D5
74 D6
75 D7
76 D8
77 D9
78 VDD
79 VSS
80 MD5
81 MD6
82 MD7
83 MD8
84 MD9
85 D10
86 D11
87 D12
88 D13
89 D14
90 VSS
91 MD10
92 MD11
93 MD12
94 MD13
95 MD14
96 NPERR
97 NMEMDIR
98 PTYL
99 PTYH
100 NSBE0

## DESCRIPTION (Cont'd.)

The SL9020 provides the data buffer latches and drivers for a 16-bit data path for PC/AT using 80286 and 80386SX type processor. Two SL9020 can be used to construct a 32-bit data path for PC/AT's using an 80386DX microprocessor.

Control logic and drivers for the chip includes CPU Data Bus (D Bus), Memory Data Bus (MD Bus), System Data Bus (SD Bus) and Peripheral Data Bus (XD Bus). The SL9020 also performs parity generation/checking, low to high byte transfer on SD Bus and drivers for low and high byte Column Address Strobes (CAS) for two independent memory banks. Latched CPU Byte enable (BHE0 & BHE1) are also provided.

All Data bus outputs are capable of high drive (12-24mA) and have fast rise & fall times of 5ns.

Latches are also provided on D to MD, MD to D, and SD to D paths.

### MD/D LOW BYTE BUFFER/LATCH

Data is transferred from MD0-7 to D0-7 or D0-7 to MD0-7 Bus via the MD/D low byte buffer/latch. The transfer direction is set MD to D by asserting NMEMDIR low. Deasserting NMEMDIR sets transfer directions D to MD. NSBE0 enables the MD or D bus low byte output buffers, and hence must be asserted to allow data to be driven onto the selected bus.

Transparent input data latches are provided on both D0-D7 and MD0-MD7 busses. Asserting DLAT high enables D0-D7 data to pass through latches. Deasserting DLAT latches D0-D7 data. Latched D0-D7 data or D0-D7 data is selected by asserting/deasserting NDLATEN. Similarly, asserting MDLAT high enables MD0-MD7 data to pass through latches. Deasserting MDLAT latches D0-D7 data. Latched MD0-MD7 data or MD0-MD7 data is selected by asserting/deasserting NMDLATEN.

### MD/D HIGH BYTE BUFFER/LATCH

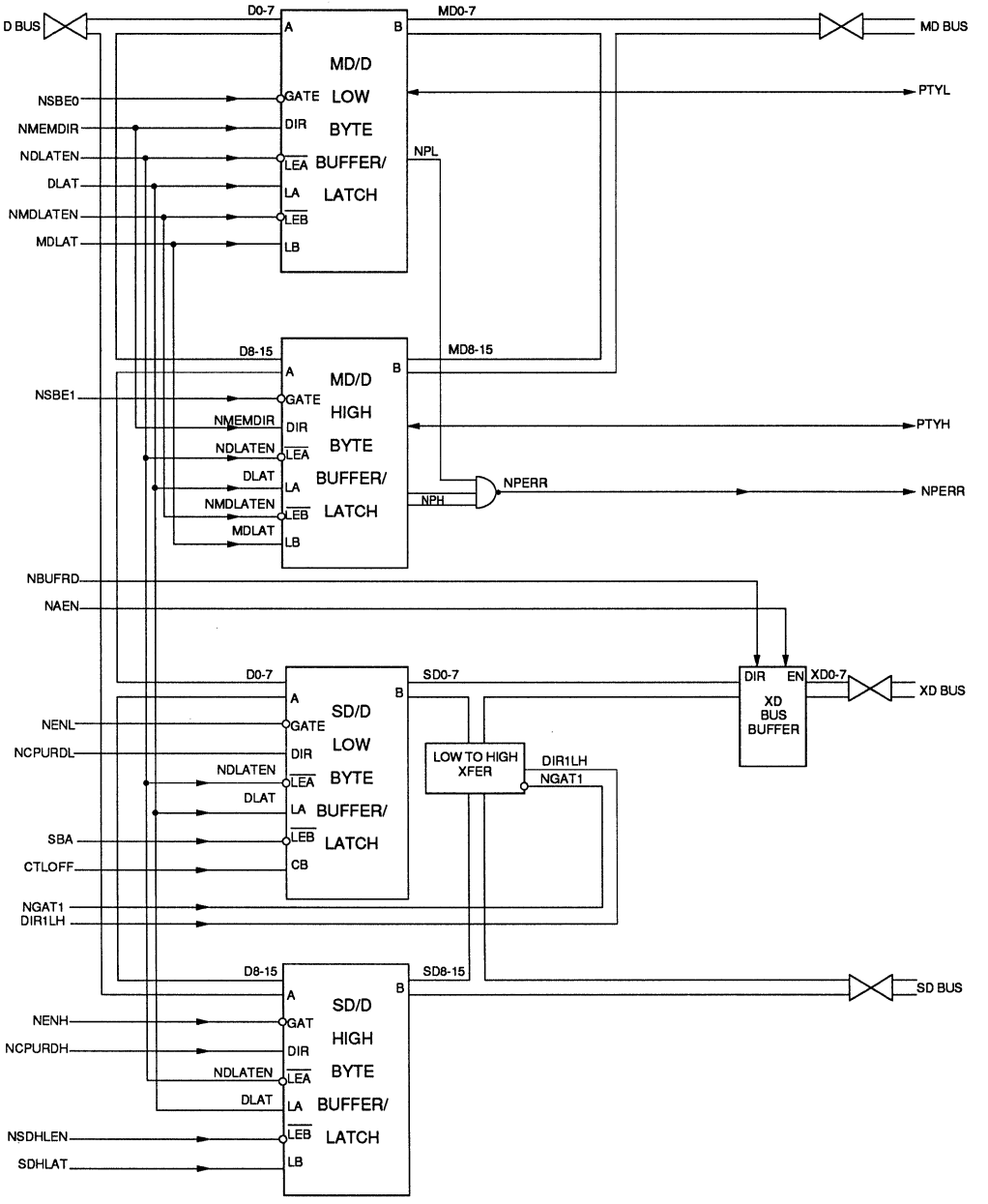
Data is transferred from the MD8-MD15 bus to the D8-D15 bus or from the D8-D15 bus to the MD8-MD15 bus via the MD/D high byte buffer/latch. Both direction (NMEMDIR) and latch controls (DLAT, NDLATEN, MDLAT, NMDLATEN) operate on high byte identically as they would on low byte. Reference MD/D low byte buffer latch. NSBE1 enables the MD or D bus high byte output buffers.

### SD/D LOW BYTE BUFFER/LATCH

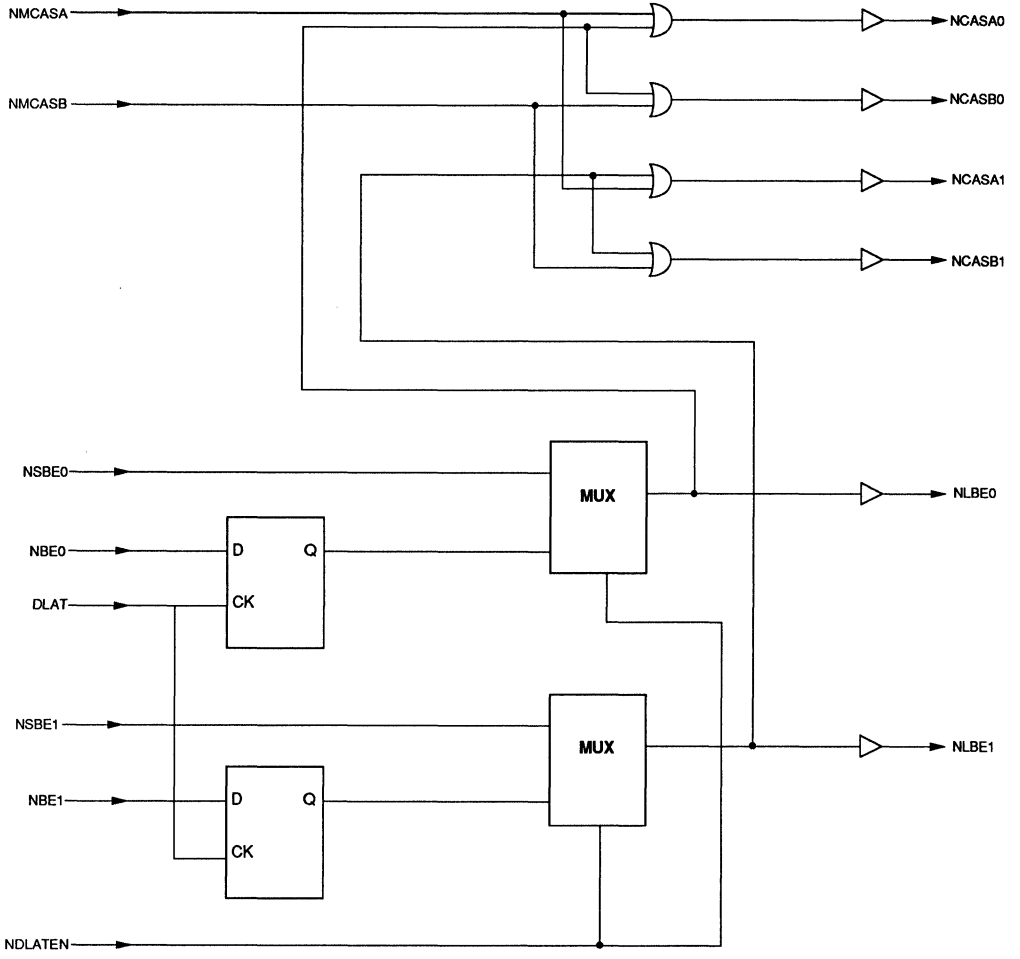
Data is transferred from SD0-SD7 bus to D0-D7 bus or from D0-D7 bus to SD0-SD7 bus via the SD/D low byte buffer/latch. The transfer direction is set SD to D by asserting NCPURDL low. Deasserting NCPURDL sets transfer direction D to SD. NENL enables the SD or D bus low byte output buffers, and hence must be asserted low to allow data to be driven onto the selected bus.

Input data latches are provided on both D0-D7 and SD0-SD7 busses. Asserting DLAT high enables D0-D7 data to pass though latches. Deasserting DLAT latches D0-D7 data. Latched D0-D7 data or D0-D7 data is selected by asserting/deasserting NDLATEN. Similarly, the low to high edge of CTLOFF latches SD0-SD7 data. Latched SD0-SD7 data or SD0-SD7 data is selected by asserting/negating SBA.

## BLOCK DIAGRAM SL9020



## BLOCK DIAGRAM SL9020 (Cont'd.)




**CAS Buffer Logic**

### SD/D HIGH BYTE BUFFER/LATCH

Data is transferred from SD8-SD15 Bus to D8-D15 Bus or from D8-D15 Bus to SD8-SD15 Bus via the SD/D high byte buffer/latch. The transfer direction is set SD to D by asserting NCPURDH low. Deasserting NCPURDH sets transfer direction D to SD. NENH enables the SD or D bus high byte output buffers, and hence must be asserted low to allow data to be driven onto the selected bus.

Input data latches are provided on both D8-D15 and SD8-SD15 busses. Asserting DLAT high enables D8-D15 data to pass through latches. Deasserting DLAT latches D8-D15 data. Latched D8-D15 data or D8-D15 data is selected by asserting/deasserting NDLATEN. The low to high edge of SDHLAT latches SD8-SD15 data. Latched SD8-SD15 data or SD8-SD15 data is selected by negating/asserting NSDHLEN.

### SD LOW BYTE TO SD HIGH BYTE TRANSFER

Low byte to high byte SD bus transfers (byte to word) are effected through the SD low byte to high byte transfer logic, asserting DIR1LH directs SD0-SD7 onto SD8-SD15. Asserting NGAT1 enables the SD buffers. If DIR1LH is deasserted, transfer will occur from high byte to low byte.

### XD BUS BUFFER

Data is transferred from XD0-XD7 bus to SD0-SD7 bus or from SD0-SD7 bus to XD0-XD7 bus via the XD bus buffer. The transfer direction is set XD to SD bus by asserting NBUFRD low. Deasserting NBUFRD sets direction of transfer SD to XD bus. NAEN enables the XD or SD bus buffers and hence must be asserted low to allow data to be driven onto the selected bus.

### CAS BUFFER LOGIC

The CAS Buffer Logic "demultiplexes" the NMCASA and NMCASB inputs from the memory controller, generating 24ma drive CAS lines for 2 Banks (A and B) high byte and low byte: NCASA0, NCASB0, NCASA1, NCASB1. Inputs NSBE0, NSBE1, NBE0, NBE1, NDLATEN, NMCASA and NMCASB are inputs to the CAS logic. NDLATEN, when asserted low, selects NBE0/NBE1 latched outputs to gate out NCASX0/NCASX1. NDLATEN is also used to gate NSBE0/NSBE1 or NBE0-NBE1 (latched with rising DLAT) into the outputs NLBE0/NLBE1. When NDLATEN is asserted low, it selects latched NBE0/NBE1 for outputs.

### PARITY GENERATION/CHECK

The parity generation and checking logic is included within the low and high byte buffer/latches. Even parity is checked looking at MD0-MD7 and PTYL for the high byte, and looking at MD8-MD15 and PTYH for the high byte. The low byte/high byte parity check outputs NPL and NPH are gated with NBE0 and NBE1 respectively and logically ored together with NMDIRIN to produce the parity error output NPERR. Parity is generated during write cycles when NMEMDIR is negated high. The low byte output PTYL, is even parity generated from D0 through D7. Similarly, the high byte output, PTYH, is even parity generated from D8 through D15.

## PIN DESCRIPTION SL9020

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| CTLOFF | 25 | I/O | Rising edge clocks data from SD [7:0] to D[7:0] latches during Bus-conversion cycles. |
| D0-D15 | 60,61,62,63,64<br>73,74,75,76,77<br>85,86,87,88,89,2 | I/O | 16 Bit local data Bus. |
| DIR1 | 9 | I | Direction 1. When asserted HIGH, directs data from SD[7:0] to SD[15:8]. DIR1 is enabled by NGAT1. |
| DLAT | 58 | I | Latches local bus data when Pulled LOW. Should be left un-connected for non-cache-based designs. Latches NBE0, NBE1. |
| MD0-MD15 | 66,67,68,69,70<br>80,81,82,83,84<br>91,92,93,94,95,5 | I/O | 16 Bit Memory data Bus. |
| MDLAT | 71 | I | Latches MD Bus data when pulled LOW. Should be left un-connected for non-cache-based designs. |
| NAEN | 46 | I | Asserting NAEN LOW enables data buffers between XD Bus & SD Bus. |
| NBE0,1 | 35,45 | I | Active LOW Byte Enable signals. Inputs to BE0/BE1 latch for CAS demultiplexing. Not normally used in an AT structure, should be pulled-up. |
| NBUFRD | 47 | I | Direction control for XD Bus Buffer. When asserted LOW, transfer is from XD to SD. |
| NCASA0 | 31 | O | CAS for bank A LS byte. |
| NCASA1 | 32 | O | CAS for bank A MS byte. |
| NCASB0 | 7 | O | CAS for bank B LS byte. |
| NCASB1 | 8 | O | CAS for bank B MS byte. |
| NCPURDH | 20 | I | HIGH byte direction control between D Bus and SD Bus. When LOW, direction is from SD Bus to D Bus. |
| NCPURDL | 21 | I | LOW Byte direction control between D Bus and SD bus. When LOW, direction is from SD Bus to D Bus. |

## PIN DESCRIPTION SL9020 (Cont'd)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NDLATEN | 59 | I | Data Latch Enable. Selects latched D Bus/D Bus data when LOW/HIGH. It also selects NBE0,1 or NSBE0,1 for use in demultiplexing CAS inputs. Should be left un-connected for non-cache-based designs. |
| NENH | 22 | I | Active LOW. HIGH Byte data transfer enable between D Bus and SD Bus from SL9011 System Controller. |
| NENL | 23 | I | Active LOW. LOW Byte data transfer enable between D Bus and SD Bus from SL9011 System Controller. |
| NGAT1 | 10 | I | When LOW, enables byte transfer between SD Bus' LOW and HIGH bytes. |
| NLBE0,1 | 26,27 | O | Latched Byte enable outputs. When NDLATEN is asserted, the latched inputs NBE0/NBE1 (latched by LOW to HIGH transition on DLAT) are buffered out on NLBE0/NBLE1. When NDLATEN is negated, the inputs NSBE0/NSBE1 are buffered out on NLBE0/NLBE1. |
| NMCASA | 30 | I | Memory Column Address Strobe from SL9X50. Active LOW for DMA or CPU Memory Cycles for Bank A. Used to generate NCASA0,1 signals. |
| NMCASB | 6 | I | Memory Column Address Strobe from SL9X50. Active LOW for DMA or CPU Memory Cycles for Bank B. Used to generate NCASB0,1 signals. |
| NMDLATEN | 72 | I | Memory data latch enable. Selects latched MD Bus data when asserted LOW. Should be left un-connected for non-cache-based designs. |
| NMEMDIR | 97 | I | Data transfer direction between D Bus and MD Bus. When LOW, data path is from MD Bus to D Bus. (Read) |
| NPERR | 96 | O | When LOW it indicates Parity Error on the LOW or the HIGH Byte. Active on read cycles only. |
| NSBE0,1 | 100,1 | I | Byte Enables. Asserting NSBE0/1 enables LOW/HIGH byte MD or D Bus Buffers. |
| NSDHLEN | 34 | I | Selects latched/unlatched SD data. When LOW it selects unlatched data from SD Bus. |

## PIN DESCRIPTION SL9020 (Cont'd)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| PTYL,H | 98,99 | I/O | Parity Data Bus for LOW and HIGH bytes. Parity is generated for write cycles. Parity is checked for read cycles. Direction is controlled by NMEMDIR. |
| SBA | 24 | I | Select Data Buffers from the SL9011 System Controller. When HIGH it selects latched data from SD [7:0] to D [7:0]. When LOW it selects unlatched data from SD [7:0] to D [7:0]. |
| SD0-SD15 | 11,12,13,14<br>16,17,18,19<br>36,37,38,39<br>41,42,43,44 | I/O | 16 Bit I/O channel Data Bus. |
| SDHLAT | 33 | I | SLOT Data Latch Strobe. A LOW to HIGH transition latches data from SD[15:8]. |
| VDD | 3,28,53,78 | - | +5V Power. |
| VSS | 4,15,29,40<br>54,65,79,90 | - | 0V Ground. |
| XD0-XD7 | 48,49,50,51<br>52,55,56,57 | I/O | 8 Bit peripheral Data Bus. |

## ABSOLUT MAXIMUM RATINGS SL9020 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current *note 2 | $I_{OS}$ | -40 | +40 | mA |
| Output Current *note 3 | $I_{OS}$ | -40 | +80 | mA |
| Output Current *note 4 | $I_{OS}$ | -60 | +120 | mA |
| Output Current *note 5 | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All other outputs.
3. XD0-XD15.
4. MD0-MD15, D0-D15.
5. SD0-SD15,NCASA,B,02,13.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9020

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state* |
| Output High Voltage for Normal Output (IOL = 3.2 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 8 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 12 mA) | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output (IOL = 24 mA) | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output (IOL = 3.2 mA) | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output (IOL = 8 mA) | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output (IOL = 12 mA) | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output (IOL = 24mA) | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for TTL Input | VIH | 2.2 | | V | |
| Input Low Voltage for TTL Input | VIL | | 0.8 | V | |
| Input High Voltage for CMOS Input | VIH | 0.7VDD | | V | |
| Input Low Voltage for CMOS Input | VIL | | 0.3VDD | V | |
| Input Leakage Current | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = VSS |

NOTES:

* VIH = VDD, VIL = Vss

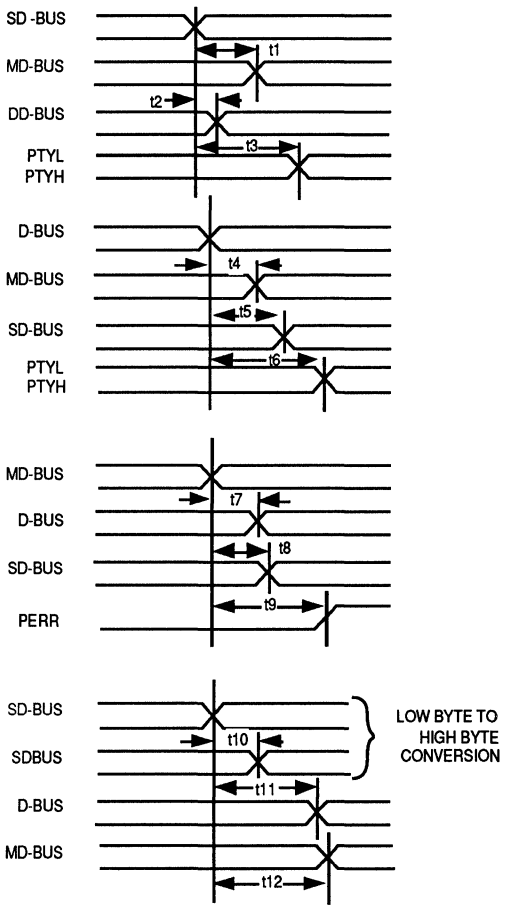
| | |
|---|---|
| SD0-SD15,NCASA,B,02,13 | = 24mA buffers (typical) |
| MD0-MD15, D0-D15 | = 12mA buffers |
| XD0-XD15 | = 8mA buffers |
| All other outputs | = 3.2 mA buffers |

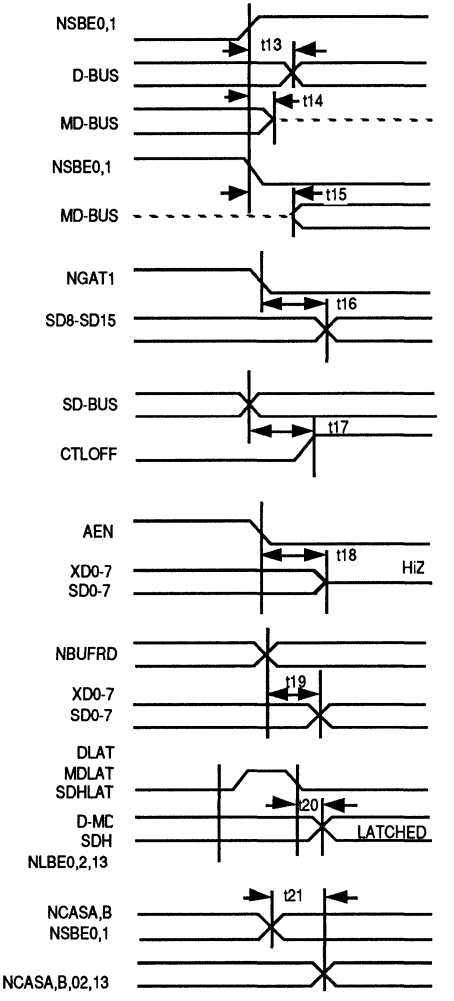
## AC CHARACTERISTICS SL9020

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| SYMBOL | DESCRIPTION | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| t1 | System Data Bus to Memory Bus Delay | 8 | 17 | ns |
| t2 | System Data Bus to CPU Data Bus Delay | 8 | 17 | ns |
| t3 | System Data Bus to Parity Bits Output | 10 | 30 | ns |
| t4 | CPU Data Bus to Memory Data Bus Delay | 8 | 15 | ns |
| t5 | CPU Data Bus to System Data Bus Delay | 8 | 20 | ns |
| t6 | CPU Data Bus to Parity Bits PTYL,H Output | 10 | 30 | ns |
| t7 | Memory Data Bus to CPU Data Bus Delay | 8 | 15 | ns |
| t8 | Memory Data Bus to System Data Bus Delay | 8 | 20 | ns |
| t9 | Memory Data Bus to Parity Error Output | 10 | 24 | ns |
| t10 | System Data Bus Low Byte to High Byte Conversion | 8 | 20 | ns |
| t11 | System Bus to CPU Data Bus Hi-Lo Byte Conversion | 8 | 30 | ns |
| t12 | System Bus to Mem Data Bus Hi-Lo Byte Conversion | 8 | 30 | ns |
| t13 | NSBE0,1 to CPU Data Bus Delay | 8 | 29 | ns |
| t14 | NSBE0,1 to Memory Data Bus Hi-Z | 8 | 26 | ns |
| t15 | NSBE0,1 to Memory Data Bus Valid | 8 | 29 | ns |
| t16 | NGAT1 to SD8-SD15 Delay | -- | 29 | ns |
| t17 | SD Bus to CTLOFF setup time | 10 | - | ns |
| t18 | AEN to XD,SD Hi-Z | 8 | 20 | ns |
| t19 | NBUFRD to XD,SD Valid | 8 | 20 | ns |
| t20 | DLAT, MDLAT, SDHLAT to Latched Data | 8 | 20 | ns |
| t21 | NCASA,B or NSBE0,1 to NCASA02,13 or NCASB02,13 | 8 | 15 | ns |

## AC TIMING DIAGRAMS SL9020



## FEATURES

- **Supports 80286, 80386SX (P9), 80386DX, and 80486-based AT Designs.**
- **Address In to Address Out: 15 ns.**
- **Up to 25 MHz Performance.**
- **24 mA Buffers.**
- **Include SA & XA Buffers.**
- **Includes XD to XA Transfer Latches.**
- **Provides Refresh for 256K, 1M or 4Mbit DRAM Chips.**
- **Includes Port B, I/O Decode and NMI Logic.**
- **Advanced CMOS Technology.**
- **100 pin Flatpack.**

## DESCRIPTION

The SL9025 Address Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

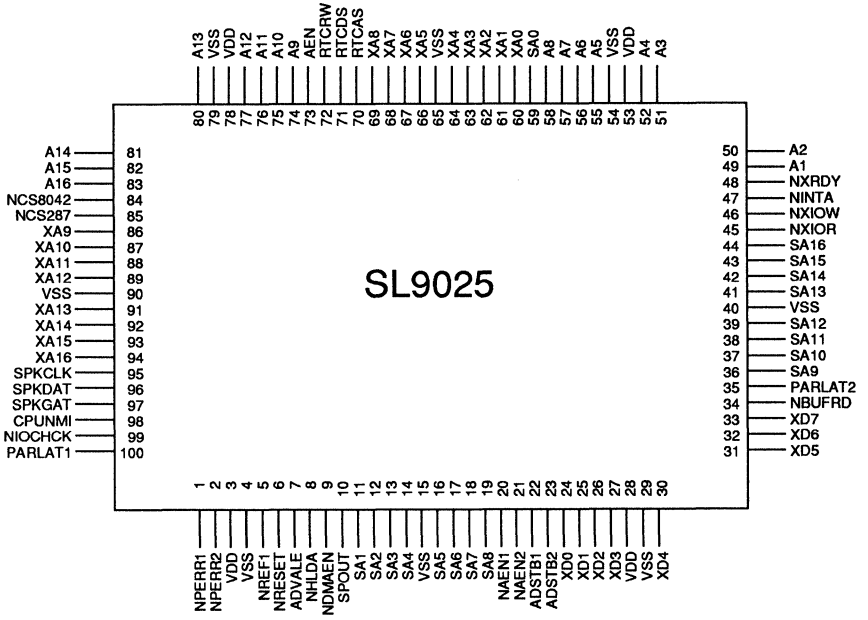
The SL9025 is part of the Core AT Logic chips that implement the system logic common to 80286, 80386SX, 80386DX and 80486-based PC/AT designs. It supports up to 25 MHz performance. In addition to the SL9025, the Core AT Logic chips consists of the SL9011 System Controller, the SL9020 Data Controller, the SL9030 Integrated Peripheral Controller and the 9X5X Memory Controller.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

SL9025 is a general purpose address controller for PC/AT. It can be used with 16 or 32 bit CPUs including 80286, 80386SX, 80386DX or 80486. The device includes all necessary latches, buffers, and drivers for CPU Address Bus (A-Bus), System Address Bus (SA-Bus), and Peripheral Address Bus (XA-Bus). In addition, Port-B, NMI, Parity Latch and I/O Decode Logic as well as Refresh for 256K, 1M or 4M DRAMs is provided. Optional XD to XA transfer latches are also provided.

High drive buffers (12mA-24mA) are provided for full PC/AT compatibility.

## PINOUT


SL9025
A14 81
A15 82
A16 83
NCS8042 84
NCS287 85
XA9 86
XA10 87
XA11 88
XA12 89
VSS 90
XA13 91
XA14 92
XA15 93
XA16 94
SPKCLK 95
SPKDAT 96
SPKGAT 97
CPUNMI 98
NIOCHCK 99
PARLAT1 100
50 A2
49 A1
48 NXRDY
47 NINTA
46 NXIOW
45 NXIOR
44 SA16
43 SA15
42 SA14
41 SA13
40 VSS
39 SA12
38 SA11
37 SA10
36 SA9
35 PARLAT2
34 NBUFRD
33 XD7
32 XD6
31 XD5
80 A13
79 VSS
78 VDD
77 A12
76 A11
75 A10
74 A9
73 AEN
72 RTCRW
71 RTCDS
70 RTCAS
69 XA8
68 XA7
67 XA6
66 XA5
65 VSS
64 XA4
63 XA3
62 XA2
61 XA1
60 XA0
59 SA0
58 A8
57 A7
56 A6
55 A5
54 VSS
53 VDD
52 A4
51 A3
1 NPERR1
2 NPERR2
3 VDD
4 VSS
5 NREF1
6 NRESET
7 ADVALE
8 NHLDA
9 NDMAEN
10 SPOUT
11 SA1
12 SA2
13 SA3
14 SA4
15 VSS
16 SA5
17 SA6
18 SA7
19 SA8
20 NAEN1
21 NAEN2
22 ADSTB1
23 ADSTB2
24 XD0
25 XD1
26 XD2
27 XD3
28 VDD
29 VSS
30 XD4

PORT B AND NMI LOGIC

Port "B" at I/O address 64H is fully IBM compatible. Read/Write bit definitions are as shown below in Table 1.

| BIT | R | W |
|---|---|---|
| 0 | Speaker Gate | Speaker Gate |
| 1 | Speaker Data | Speaker Data |
| 2 | XD2 | Reset Parity Latch |
| 3 | XD3 | Reset I/O Chck Latch |
| 4 | REFRESH 0 | XD4 |
| 5 | Speaker Clock | XD5 |
| 6 | I/O Channel Check | XD6 |
| 7 | Parity Error | NMI Enable |

**Table 1**

Parity error signals NPERR1 and NPERR2 are logically ored together and latched by a low to high transition on PARLAT1 or PARLAT2 inputs. The parity latch is held reset by writing a 1 to Bit 2. Parity error inputs on Port B Bit 7.

I/O channel check (NIOCHCK) is latched on a low transition, and is held clear by writing a 1 to Bit 3. It is input on Bit 6.

Latched parity error and I/O channel check are ored together and gated out with write Bit 7 to produce a CPUNMI (CPU non-maskable interrupt).

DMA

8237 compatible DMA support logic is comprised of two 8 Bit latches and two 8 Bit multiplexers. Reference the DMA section of the Block Diagram.

A low to high transition on ADSTB1 latches 8 Bit DMA most significant address byte from XD Bus into XD8 latch. Likewise, a low to high transition on ADSTB2 latches 16 Bit DMA most significant address byte from SD bus into SD16 latch.

If the transfer is an 8 Bit DMA, input NAEN1 is asserted causing the DMA Mux to switch SD8 latch data onto the SA Bus Mux and the A Bus Mux. If the transfer is a 16 Bit DMA, input NAEN2 is asserted causing the DMA Mux to switch SD16 latch data onto the S Bus Mux and the A Bus Mux.

## I/O DECODE LOGIC

The I/O decode logic provides the chip selects and strobes for the NPX, NMI, Port B, Keyboard Controller and the RTC. Reference the I/O Decode Logic portion of the Block Diagram. The direction enable signal NBUFRD, used by the SL9020 Data Controller, is also provided.

Input SPOUT is used to gate NXIOR onto NBUFRD. Address inputs XA0, 4, 5, 6, 7, 8, 9 and AEN are selectively used to decode the external selects NCS287 and NCS8042, the strobes RTCAS, RTCDS, RTCRW and NBUFRD, as well as the internal strobes NMICK, PBRD and PBWT. Input NXIOR strobes NBUFRD, RTCDS and PBRD. The input NXIOW strobes NMICK, RTCRW and PBWR. NXRDY qualifies NMICK and the output RTCAS.

## BUS MULTIPLEXERS/DIRECTION CONTROL

The bus multiplexers and direction control logic provides the necessary gating and arbitration to:

1. The XA and SA Bus with system address during CPU I/O and memory operations
2. DMA address during DMA transfers
3. Refresh address to A and SA Buses at Refresh time

The direction control logic uses the inputs NHLDA, NDMAEN, NAEN1, NAEN2 and NREF1 to generate the I/O internal Mux selection and output buffer enable signals; X TO S, X TO A, S TO A, S TO X, A TO X, XR TO S, NENA, NENS, NENXL, NENXH. Refer to Table 2 for the allowed transfer directions.

## REFRESH COUNTER/MULTIPLEXER

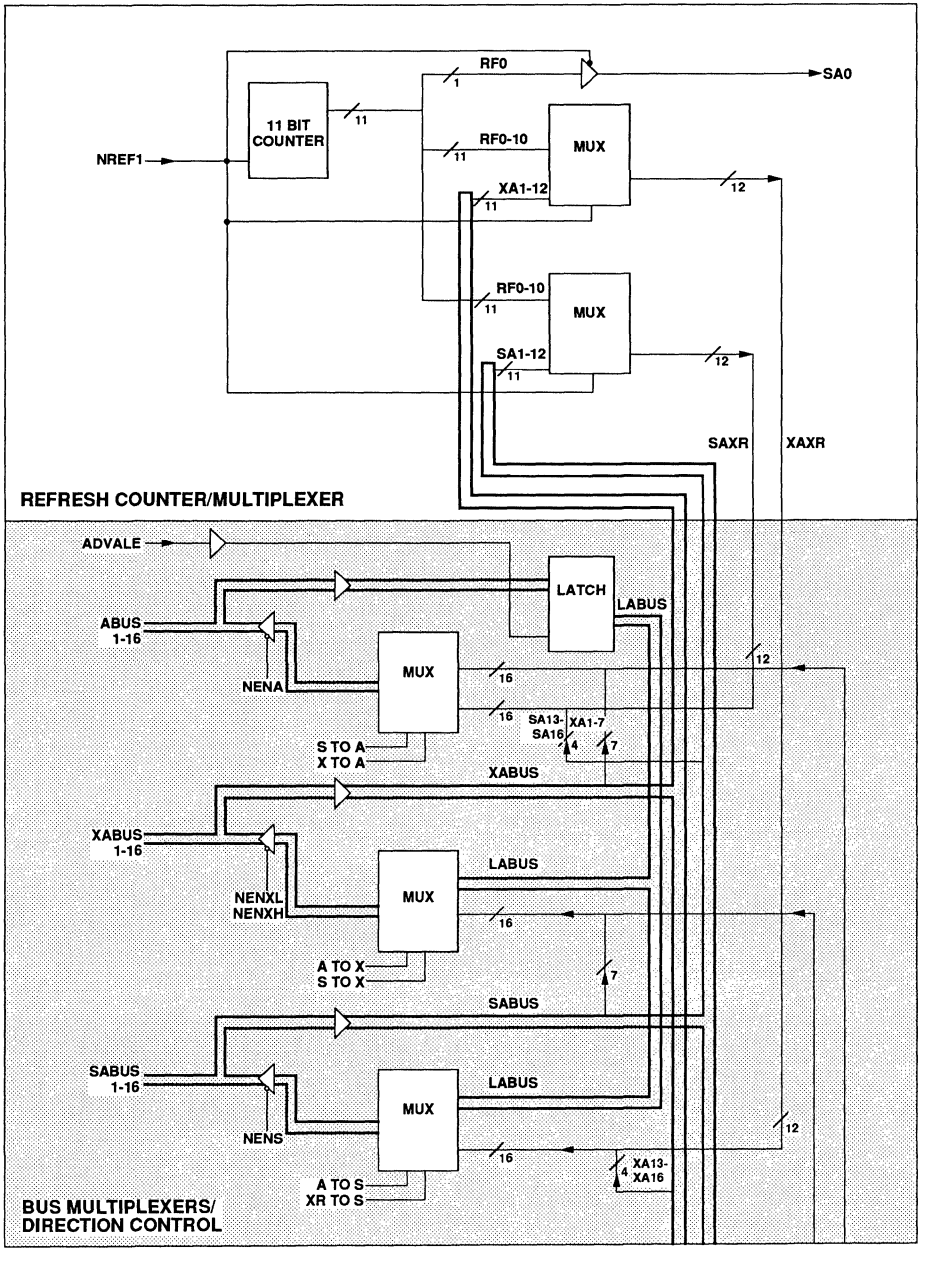
The Refresh Counter/Multiplexer consists of an eleven bit Counter and two 12 Bit Multiplexers.

When NREF1 is true, the 11 Bit Counter is advanced, and the output address is Muxed and enabled onto the A Bus and SA Bus.

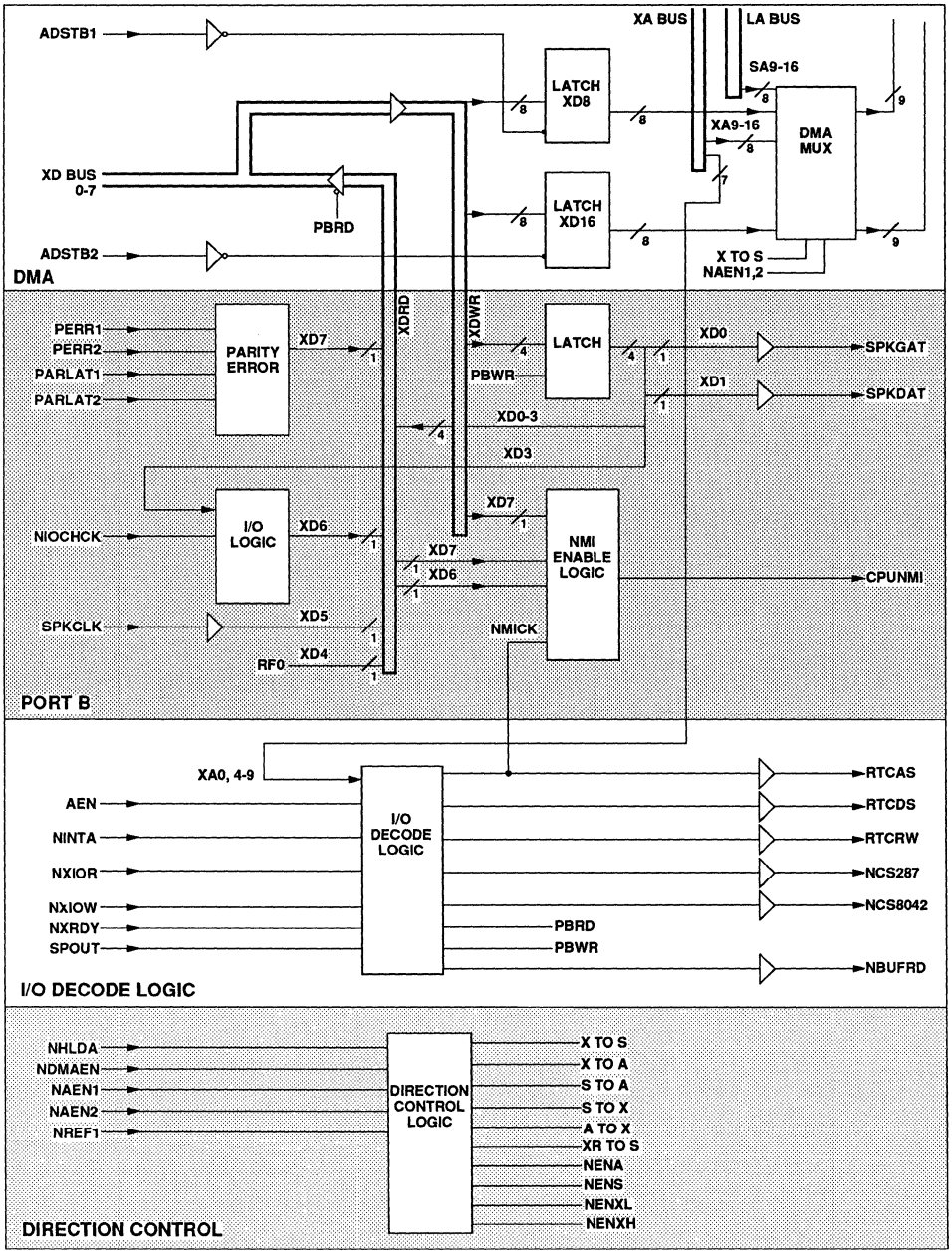
| SYSTEM FUNCTION | NHLDA | NDMAEN | AEN1,2 | REF1 | NAENA | NENS | NENXL | NENXH | S TO A | A TO S | XR TO S | X TO S | S TO X | X TO A | A TO X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| I/O REFR | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| LOC REFR | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| CPU R/W | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

**Table 2**

## BLOCK DIAGRAM SL9025



## BLOCK DIAGRAM SL9025 (Conf'd)



## PIN DESCRIPTION SL9025

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A1-A16 | 49,50,51,52, 55,56,57,58, 74,75,76,77, 80,81,82,83 | I/O | CPU Address Bus. |
| ADSTB1,2 | 22,23 | I | Address Strobes to latch XD data from DMA controllers to XA Bus. ADSTB1 is active for 8-bit DMA transfers while ADSTB2 is active for 16-bit DMA transfers. Tied HIGH if the SL9030 Integrated Peripheral Controller is used. |
| ADVALE | 7 | I | Advance Address Latch Enable from memory controller. It latches local bus address for the system bus on the LOW to HIGH transition. |
| AEN | 73 | I | Address Enable, HIGH for DMA cycles. Prevents DMA from accessing on-board peripherals. When LOW, enables data buffers between XD Bus and SD Bus. |
| CPUNMI | 98 | O | CPU Non-Maskable Interrupt, generated from PERR or IOCHCK. Output to 80X86. |
| NAEN1,2 | 20,21 | I | Address Enable 1 and 2, from discrete DMA controller. Assertion allows DMA XD data to tie to XA Bus. Tied HIGH if the SL9030 Integrated Peripheral Controller is used. |
| NBUFRD | 34 | O | Direction control for data buffer between SD Bus and XD Bus. Drives the SL9025 Data Controller signal NBUFRD. |
| NCS287 | 85 | O | Active LOW Numeric Processor Chip Select to NXP. |
| NCS8042 | 84 | O | Active LOW Keyboard Controller Chip Select to 8042. |
| NDMAEN | 9 | I | DMA Enable from the SL9011 System Controller. When LOW, indicates a DMA cycle: XA1-XA16 is gated onto SA1-SA16. |
| NHLDA | 8 | I | Hold Acknowledge. When asserted by CPU, indicates that the CPU has released the bus. It is used to direction address bits 1-16 to/from A Bus/SA Bus. |
| NINTA | 47 | I | Interrupt Acknowledge from the SL9011 System Controller. It is used to gate NBUFRD. |
| NIOCHCK | 99 | I | I/O Channel Check. Active LOW signal from the AT bus. When LOW it indicates an I/O channel fault. |

## PIN DESCRIPTION SL9025 (Cont'd)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NPERR1,2 | 1,2 | I | Parity Error from lower and upper 16 bit RAM, from the SL9020 Data Controller. |
| NREF1 | 5 | I | Refresh cycle clock from SL9011 pin REFCLK. It is used to clock RAM Row Address during Refresh. |
| NRESET | 6 | I | Systems Reset. Active LOW, from the SL9011 System Controller. |
| NXIOR | 45 | I | X Bus I/O Read. |
| NXIOW | 46 | I | X Bus I/O Write. |
| NXRDY | 48 | I | X Ready from the SL9011 System Controller. When LOW, indicates a peripheral bus cycle termination. (End of T2 data phase.) It is used to qualify RTCAS. |
| PARLAT1,2 | 100,35 | I | Parity error is latched on rising edge of either PARLAT1 or PARLAT2 while the other is LOW. Connects to 9X5X pins NBMR and NCAS. |
| RTCAS | 70 | O | Active HIGH Real Time Clock Address Strobe to RTC. |
| RTCDS | 71 | O | Active HIGH Real Time Clock Data Strobe to RTC. |
| RTCRW | 72 | O | Active HIGH Real Time Clock Read Cycle/Write Cycle input to RTC. |
| SA0 | 59 | O | System Bus Address A0. |
| SA1-SA16 | 11,12,13,14, 16,17,18,19, 36,37,38,39, 41,42,43,44 | 1/O | System Address Bus. |
| SPKCLK | 95 | I | Speaker Clock from the SL9030 Integrated Peripheral Controller. |
| SPKDAT | 96 | O | Speaker Data active HIGH output used to gate the timer tone signal to the speaker. |
| SPKGAT | 97 | O | Speaker Gate. Enables timer tone signal to the speaker. |
| SPOUT | 10 | I | Serial Parallel port decode. Usually tied LOW. A logical 1 in will enable NBUFRD during NXIOR. |
| VDD | 3,28,53,78 | - | +5V. Power. |

## PIN DESCRIPTION SL9025 (Cont'd)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| VSS | 4,15,29,40, 54,65,79,90 | - | 0V. Ground. |
| XA0 | 60 | I | Peripheral Bus Address A0. |
| XA1-XA16 | 61,62,63,64, 66,67,68,69, 86,87,88,89, 91,92,93,94 | I/O | Peripheral Address Bus. |
| XD0-XD7 | 24,25,26,27, 30,31,32,33 | I/O | Peripheral Data Bus. |

## ABSOLUT MAXIMUM RATINGS SL9025 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current *note 2 | $I_{OS}$ | -40 | +40 | mA |
| Output Current *note 3 | $I_{OS}$ | -40 | +80 | mA |
| Output Current *note 4 | $I_{OS}$ | -60 | +120 | mA |
| Output Current *note 5 | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All others.
3. A1-A16.
4. XA1-XA16.
5. SA0-SA16.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9025

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state* |
| Output High Voltage for Normal Output (IOL = 3.2 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 8 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 12 mA) | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output (IOL = 24 mA) | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output (IOL = 3.2 mA) | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output (IOL = 8 mA) | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output (IOL = 12 mA) | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output (IOL = 24mA) | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for Normal Input | VIH | 2.2 | | V | |
| Input Low Voltage for Normal Input | VIL | | 0.8 | V | |
| Input High Voltage for CMOS Input | VIH | 0.7VDD | | V | |
| Input Low Voltage for CMOS Input | VIL | | 0.3VDD | V | |
| Input Leakage Current | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = Vss |

NOTES:

* VIH = VDD, VIL = Vss

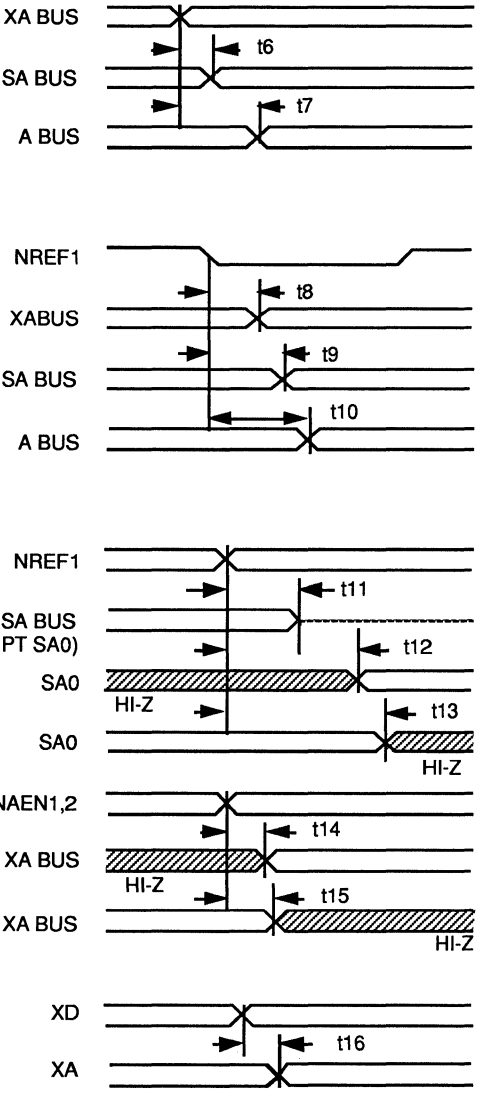
| | | |
|---|---|---|
| SA0-SA16 | = 24mA buffers | (typical) |
| XA1-XA16 | = 12mA buffers | |
| A1-A16 | = 8mA buffers | |
| All others | = 3.2 mA buffers | |

## AC CHARACTERISTICS SL9025

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| SYMBOL | DESCRIPTION | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| t1 | ADVALE to System Address Bus Delay | 8 | 20 | ns |
| t2 | ADVALE to Peripheral Address Bus Delay (XA Bus) | 8 | 20 | ns |
| t4 | System Address Bus to Peripheral Address Bus Delay (XA Bus) | 8 | 15 | ns |
| t5 | System Address Bus to CPU Address Bus Delay | 8 | 15 | ns |
| t6 | Peripheral Address Bus to System Address Bus Delay | 8 | 15 | ns |
| t7 | Peripheral Address Bus to CPU Address Bus Delay | 8 | 15 | ns |
| t8 | NREF1 Active to Peripheral Address Bus Valid Delay | 8 | 40 | ns |
| t9 | NREF1 Active to System Address Bus Delay | 8 | 40 | ns |
| t10 | NREF1 Active to Memory Address Bus Delay | 8 | 40 | ns |
| t11 | NREF1 In-Active to System Address Bus Hi-Z Delay | 8 | 20 | ns |
| t12 | NREF1 to SA0 Valid Delay | 6 | 15 | ns |
| t13 | NREF1 to SA0 Hi-Z Delay | 6 | 15 | ns |
| t14 | NAEN1,2 to Peripheral Address Bus Valid Delay | 6 | 15 | ns |
| t15 | NAEN1,2 to Peripheral Address Bus Hi-Z Delay | 6 | 15 | ns |
| t16 | Peripheral Data Bus to Peripheral Address Bus Delay | 8 | 20 | ns |

## AC TIMING DIAGRAMS SL9025



## FEATURES

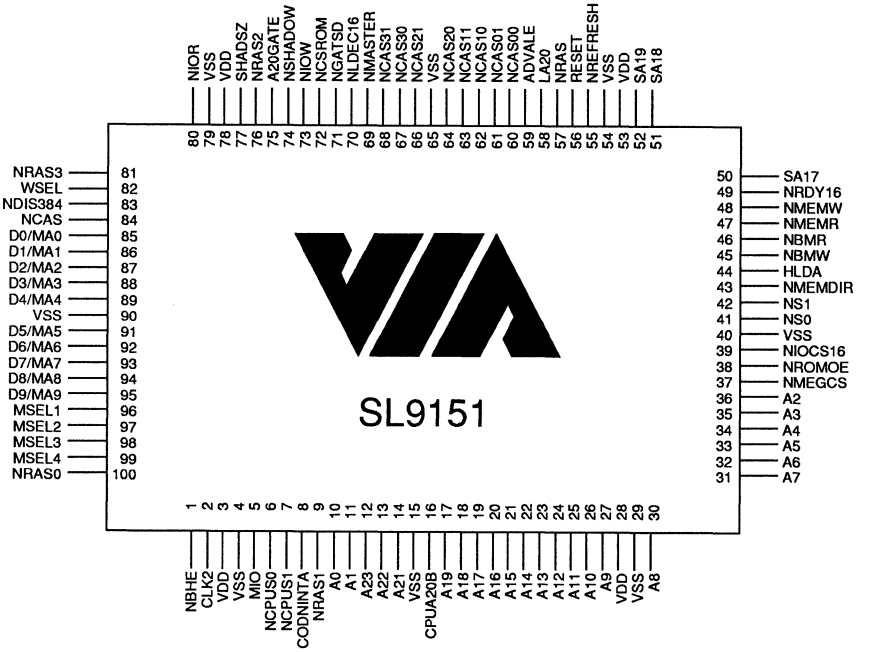
- Supports 80286 based designs.
- 16, 20 or 25 MHz Options.
- Enhanced Fast Page Mode/Page Interleave DRAM Controller.
- Hardware support for EMS LIM 4.0 standard and EEMS.
- Supports up to 8 M byte of on board memory.
- Programmable Shadow RAM feature of 128K or 256K.
- Programmable 2 or 4 way Memory Interleaving Option.
- Programmable Wait State Options.
- Can use 256K x 1, 256K x 4, and 1 M x 1 DRAMs or a mix.
- Supports 120ns and 80ns DRAMs at 16 MHz, 80ns and 60ns at 20 MHz and 60ns and 40ns at 25MHz.
- Programmable Registers for changing switch settings.
- Selectable Wait States for Slower DRAMs.
- Selectable remapping of 640K - 1 M RAM to top of the address space.
- Advanced CMOS Technology.
- 100 pin Flatpack.

## DESCRIPTION

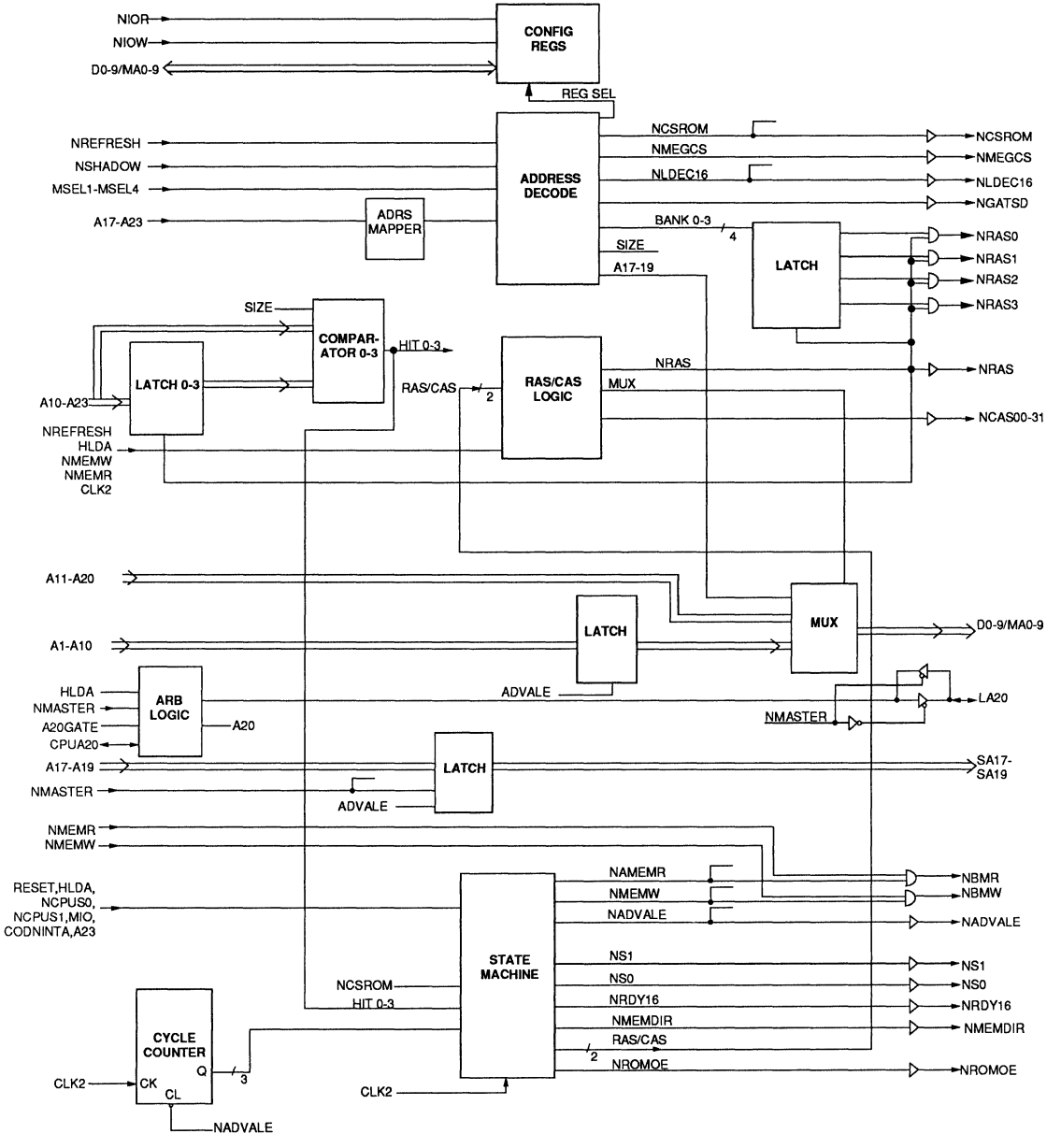
The SL9151 Memory Controller is a second generation integration of the most popular 80286 system level features. Both EMS LIM 4.0 and EEMS are now available on the chip. Programmable registers are available for controlling 2 or 4 way memory interleave options. In addition, earlier features have been expanded and optimized for higher performance.

The SL9151, along with the SL925X and SL935X provide complete PC/AT solutions by utilizing the same core logic chips. It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

## PINOUT


NIOR 80
VSS 79
VDD 78
SHADSZ 77
NRAS2 76
A20GATE 75
NSHADOW 74
NIOW 73
NCSROM 72
NGATSD 71
NLDEC16 70
NMASTER 69
NCAS31 68
NCAS30 67
NCAS21 66
VSS 65
NCAS20 64
NCAS11 63
NCAS10 62
NCAS01 61
NCAS00 60
ADVALE 59
LA20 58
NRAS 57
RESET 56
NREFRESH 55
VSS 54
VDD 53
SA19 52
SA18 51
NRAS3 81
WSEL 82
NDIS384 83
NCAS 84
D0/MA0 85
D1/MA1 86
D2/MA2 87
D3/MA3 88
D4/MA4 89
VSS 90
D5/MA5 91
D6/MA6 92
D7/MA7 93
D8/MA8 94
D9/MA9 95
MSEL1 96
MSEL2 97
MSEL3 98
MSEL4 99
NRAS0 100
50 SA17
49 NRDY16
48 NMEMW
47 NMEMR
46 NBMR
45 NBMW
44 HLDA
43 NMEMDIR
42 NS1
41 NS0
40 VSS
39 NIOCS16
38 NROMOE
37 NMEGCS
36 A2
35 A3
34 A4
33 A5
32 A6
31 A7
SL9151
1 NBHE
2 CLK2
3 VDD
4 VSS
5 MIO
6 NCPUS0
7 NCPUS1
8 CODNINTA
9 NRAS1
10 A0
11 A1
12 A23
13 A22
14 A21
15 VSS
16 CPUA20B
17 A19
18 A18
19 A17
20 A16
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
27 A9
28 VDD
29 VSS
30 A8

## BLOCK DIAGRAM SL9151



## DESCRIPTION

### ROM/RAM DECODE

The device provides all necessary circuitry to decode on board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column or Fast Page DRAMs.

The system can be configured for 512K Bytes to 8M Bytes. The bank selection code & sizes are as follows:

| Total On Board Memory | Memory in Each Bank | | | | Switch Selection | | | | Operation Mode |
|---|---|---|---|---|---|---|---|---|---|
| | Bank3 | Bank2 | Bank1 | Bank0 | Msel4 | Msel3 | Msel2 | Msel1 | |
| 512K | | | | 512K | 0 | 0 | 0 | 0 | Non Interleaved |
| 1M | | | 512K | 512K | 0 | 0 | 0 | 1 | Non Interleaved |
| 1.5M | | 512K | 512K | 512K | 0 | 0 | 1 | 0 | Non Interleaved |
| 2M | 512K | 512K | 512K | 512K | 0 | 0 | 1 | 1 | Non Interleaved |
| 3M | | 2M | 512K | 512K | 0 | 1 | 1 | 0 | Non Interleaved |
| 5M | 2M | 2M | 512K | 512K | 0 | 1 | 1 | 1 | Non Interleaved |
| 2M | | | | 2M | 1 | 1 | 0 | 0 | Non Interleaved |
| 4M | | | 2M | 2M | 1 | 1 | 0 | 1 | Non Interleaved |
| 6M | | 2M | 2M | 2M | 1 | 1 | 1 | 0 | Non Interleaved |
| 8M | 2M | 2M | 2M | 2M | 1 | 1 | 1 | 1 | Non Interleaved |
| | | | | | | | | | Interleaved: |
| 1M | | | 512K | 512K | 1 | 0 | 0 | 0 | 2 Way |
| 2M | 512K | 512K | 512K | 512K | 1 | 0 | 0 | 1 | 4 Way |
| 4M | | | 2M | 2M | 1 | 0 | 1 | 0 | 2 Way |
| 8M | 2M | 2M | 2M | 2M | 1 | 0 | 1 | 1 | 4 Way |

**Table 1**

When NDIS384 input is tied low, the 384K remap to the top of the memory space is disabled.

When CPU accesses the memory for the first time, the controller runs a page miss memory cycle and asserts RAS and CAS low at appropriate times (Fig. 1). RAS is left low, CAS is returned high at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with previous value stored in the register. If a match (hit) is detected, then the RAS is held low and CAS is strobed immediately. If a mismatch (miss) is detected then RAS is brought high for 3 CLK2 cycles before reasserting low, and new row address is stored in the row address register. The controller will now run an 0/2 or 1/3 wait state memory cycle depending on the switch setting WSEL1 (Fig. 1, Fig. 2).

Page is automatically sized to 2KB if any 256K DRAMs are used and to 4KB if only 1M DRAMs are used.

CPU Addresses A11-A20 are passed onto MA0-9 as latched row addresses whereas A1-A10 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. NRAS, MUXSEL (internal), and NCAS00-31 are separated by one CLK2 period as shown in the timing diagram (fig.1). This latching of column addresses allows the use of static column DRAMs as well.

## ROM/RAM CONTROL

SL9151 provides all the circuitry needed to generate RAM/ROM controls. Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS00-31), RAM Read/Write (NBMR, NBMW) ready for 16 bit on board RAM read/write (NRDY16) and non on-board memory/IO cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

| MIO | CODNINTA | CPUNS0 | CPUNS1 | ADDRESS | CYCLE TYPE |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | _____ | MEM CODE READ |
| 1 | 0 | 0 | 0 | _____ | HALT/SHUTDOWN |
| 1 | 1 | 1 | 0 | _____ | MEM DATA READ |
| 1 | 1 | 0 | 1 | _____ | MEM DATA WRITE |
| 0 | 0 | 0 | 0 | _____ | INTA |
| 0 | 1 | 1 | 0 | _____ | I/O DATA READ |
| 0 | 1 | 0 | 1 | _____ | I/O DATA WRITE |

**Table 2**

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 16 bit memory miss can be set using the following table.

| CPU SPEED | WSEL1 | WAIT STATES | | MEMORY SPEED (NS) |
|---|---|---|---|---|
| | | Page Miss | Page Hit | |
| 16 | 1 | 3 | 1 | 120 |
| | 0 | 2 | 0 | 80 |
| 20 | 1 | 3 | 1 | 80 |
| | 0 | 2 | 0 | 60 |
| 25 | 1 | 3 | 1 | 60 |
| | 0 | 2 | 0 | 40 |

**Table 3**

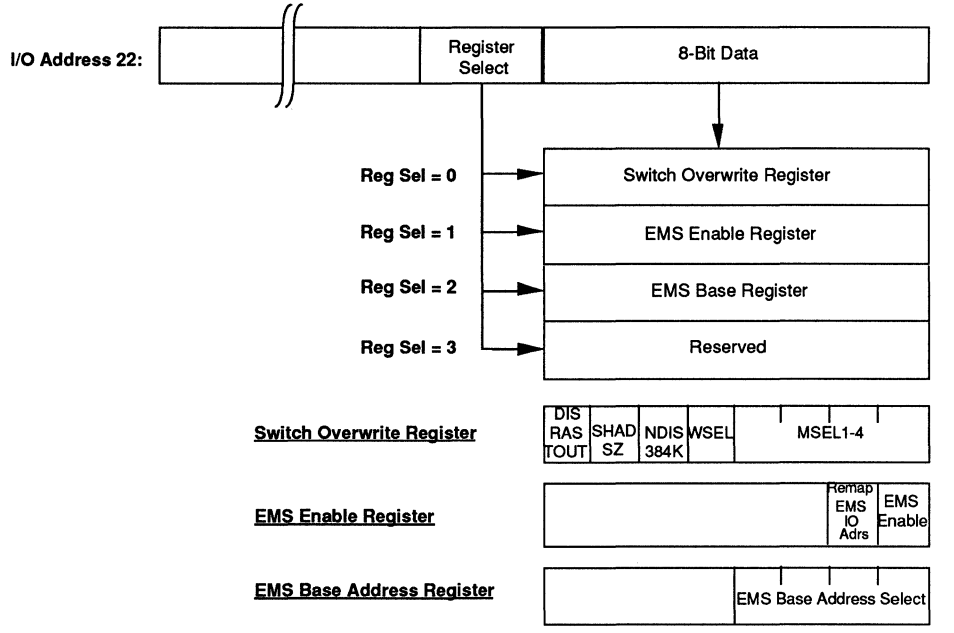
ROM controls, NCSROM and NROMOE, are asserted low at appropriate time when address 0E0000h-0FFFFFh or FE0000h-FFFFFFh is decoded during a memory cycle. The timing relationship is shown in the timing diagram. If Shadow RAM option is used by strapping NSHADOW pin low, the subsequent ROM code reads will be treated as RAM reads and ROM controls are disabled. BIOS customization is required to activate this option at boot time. NSHADOW option only affects the 128K/256K region immediately below 1 Meg, depending on the state of SHADSZ pin.

## REFRESH

The SL9151 provides support for DRAM refresh. During refresh NRAS0-3 are deasserted and then asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by SL9025 Address Controller are passed from A Bus to MA Bus.

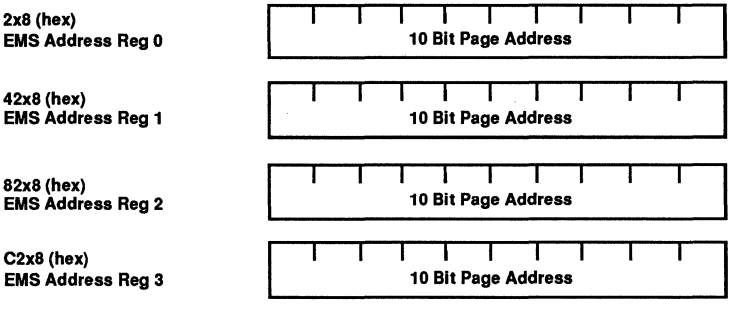
## INTERNAL REGISTERS

16 Bit I/O write to address 22 writes a byte of data to one of 4 registers as selected by Data Bits 8 and 9.



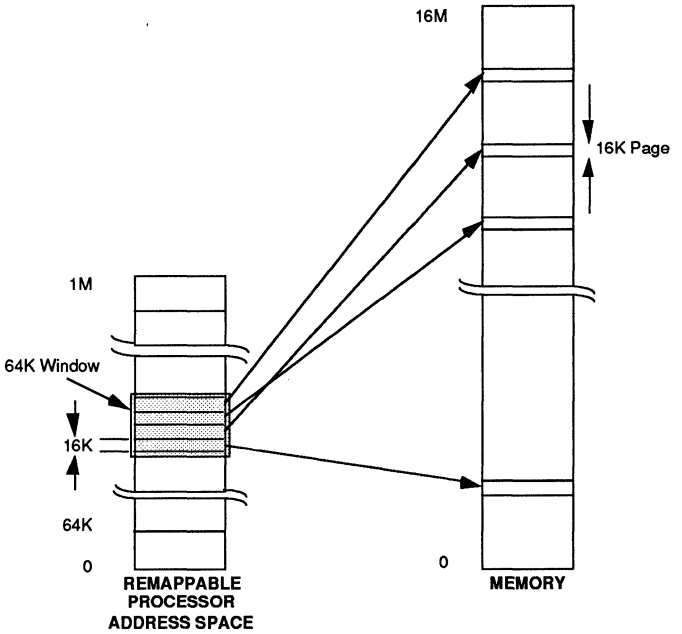

There are 4 EMS address registers of 10 bits width each, at the addresses: 2x8, 42x8, 82x8 and C2x8. X is 0 or 1 as defined by EMS Enable Register Bit 1. They each contain the Page Address for EMS Remapped Page.

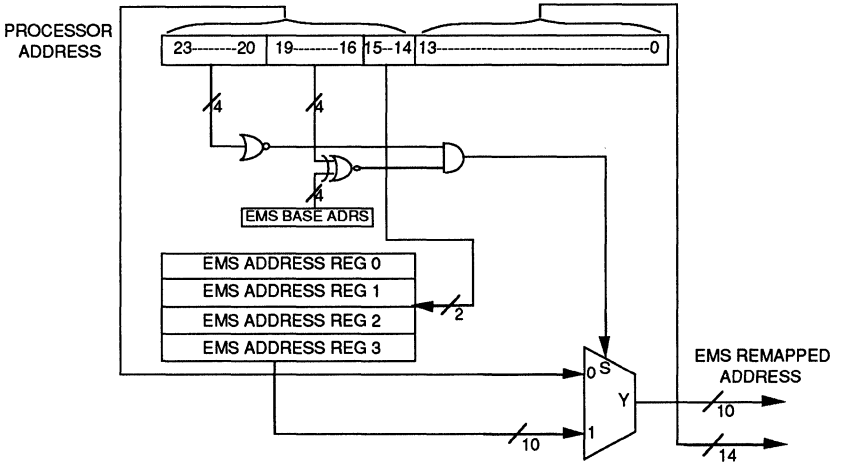
The remapping is shown in the diagrams.



## EMS REMAPPING

EMS Base Address can be set to any 64K boundary in the first 1 Meg address space of the processor. Then four 16K pages above that (base-address) can be mapped to any 16K boundary in the 16 Meg space.



## PIN DESCRIPTION SL9151

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A1-A16 | 11,36,35,34, 33,32,31,30, 27,26,25,24, 23,22,21,20 | I | CPU Address Bus. |
| A17-A23 | 19,18,17,14, 13,12 | I | CPU Address Bus. |
| A20GATE | 75 | I | CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH. |
| ADVALE | 59 | O | Advanced Address Latch Enable. It latches local bus address for the system bus. |
| CLK2 | 2 | I | CLK2 from SL9011 System Controller. CPU should get inverted CLK2. |
| CODNINTA | 8 | I | CPU status signal. |
| CPUA20B | 16 | I/O | CPU Address 20 or LA20. |
| D0-9/MA0-9 | 85,86,87,88, 89,91,92,93, 94,95 | I/O | DRAM address bus. Data Bus for writing to the programmable registers for EMS and option select registers. |
| HLDA | 44 | I | Asserted to signal that the CPU has relinquished control of the bus to the requesting device. |
| LA20 | 58 | I/O | Decoded 20-bit address bit used to generate address decode for 1 M RAMs. |
| MIO | 5 | I | CPU Output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is used to generate memory and I/O signals for the system. |
| MSEL1-4 | 96,97,98,99 | I | On-board DRAM memory size and type select. Internally pulled down. See Table 1. |
| NBMR | 46 | O | Buffered Memory Read signal. |
| NBMW | 45 | O | Buffered Memory Write signal. |
| NCAS | 84 | O | Logical Or of all CAS00-31 signals. |
| NCAS00,01, 10, 11,20, 21 30, 31 | 60-64, 66-68 | O | Memory Column Address Strobe. Asserted LOW when either CPU or DMA is accessing the memory. |

## PIN DESCRIPTION SL9151 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NCPUS0,1 | 6,7 | I | CPU status signal. |
| NCSROM | 72 | O | LOW assert Read Only Memory Chip select. |
| NDIS384 | 83 | I | Optional Disable for 684K - 1M [384K] remap. When LOW disables remap. |
| NGATSD | 71 | O | Control for an external data buffer used for writing from XD Bus to XD/MA inputs only during I/O write cycles. This signal may be used to enable a 74245 type device. When LOW the 74245 may enable this data. |
| NIOCS16 | 39 | I/O | 16 Bit I/O cycle indication. |
| NIOR | 80 | I/O | Input/Output Read is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle. |
| NIOW | 73 | I/O | Input/Output Write is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle. |
| NSHADOW | 74 | I | Selectable Option for Shadow RAMs. When LOW enables Shadow RAM feature. |
| NLDEC16 | 70 | O | Decode for on-board high speed 16-bit RAM. |
| NMASTER | 69 | I | Asserted when an external device has control of the AT Bus. |
| NMEGCS | 37 | O | Decode for lower 1M of RAM. |
| NMEMDIR | 43 | O | Direction select between D Bus and MD Bus. Read when LOW, generated by SL9011 System Controller. |
| NMEMR | 47 | I | LOW assert Memory Read signal from SL9011 System Controller. |
| NMEMW | 48 | I | LOW assert Memory Write signal from SL9011 System Controller. |
| NRAS | 57 | O | LOW assert Row Address Strobe. |
| NRAS0-3 | 100,9,76,81 | O | Row Address Strobes for Banks 0, 1, 2 and 3 for the on-board memory. Asserted LOW during CPU or DMA cycle for memory access. |

## PIN DESCRIPTION SL9151 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NRDY16 | 49 | O | Asserted LOW to signal the end of 16 bit on board memory cycle. |
| NREFRESH | 55 | I | On-board RAM refresh signal. |
| NROMOE | 38 | O | Enables ROM Output during ROM read cycles. |
| NS0,1 | 41,42 | O | 80286 compatible status signals for the SL9011 System Controller. |
| RESET | 56 | I | Active HIGH reset from system controller. |
| SA17,18,19 | 50,51,52 | O | System Address Bus. |
| SHADSZ | 77 | I | Selects Shadow Memory Size. 0 = 128K. 1 = 256K. |
| WSEL | 82 | I | Wait-state Select Options. Internally pulled up. See Table 3. |
| VDD | 3,28,53,78 | - | +5V. Power. |
| VSS | 4,15,29,40, 54,65,79,90 | - | 0V. Ground. |

## AC TIMING DIAGRAMS SL9151

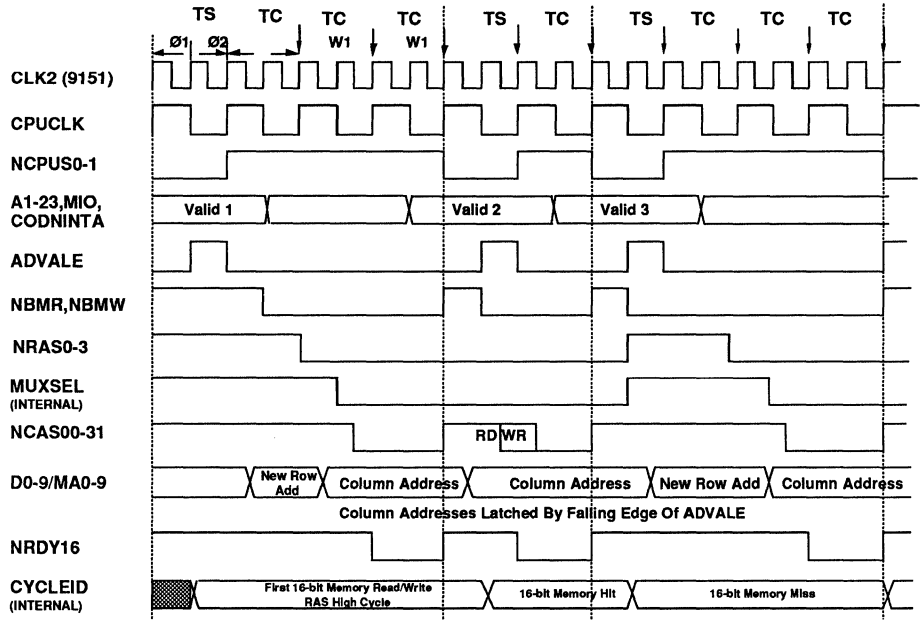



Fig. 1 16 Bit On Board/Local Memory Cycles Timing Diagram

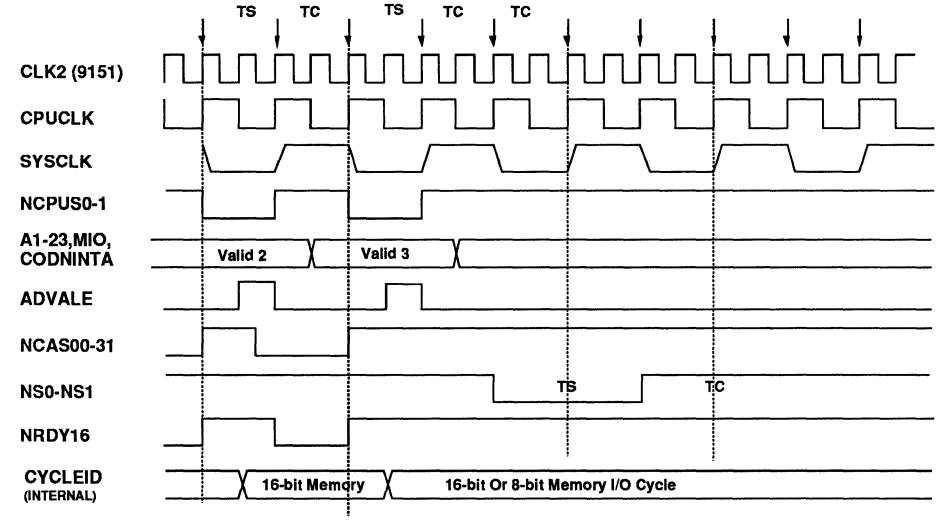



Fig. 2 Timing Diagram for I/O and Off Board Memory Cycles

## AC TIMING DIAGRAMS SL9151

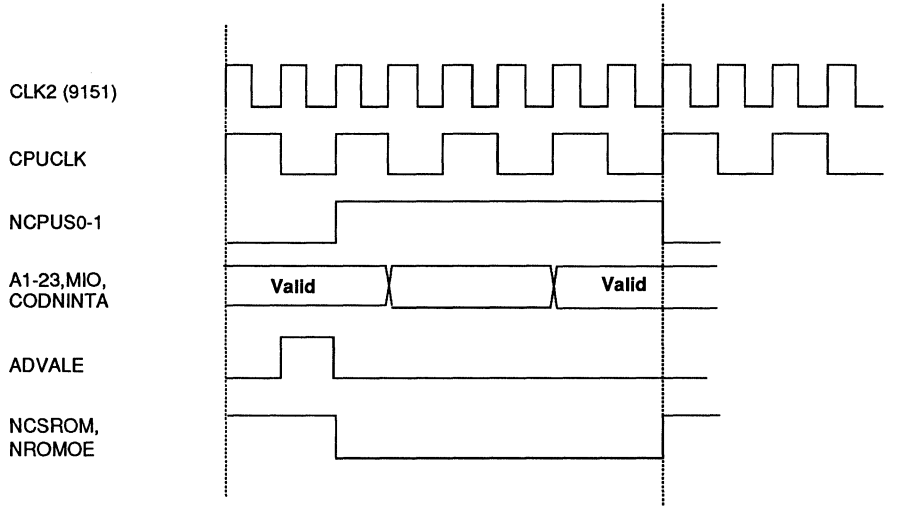



Fig. 3. ROM Cycle

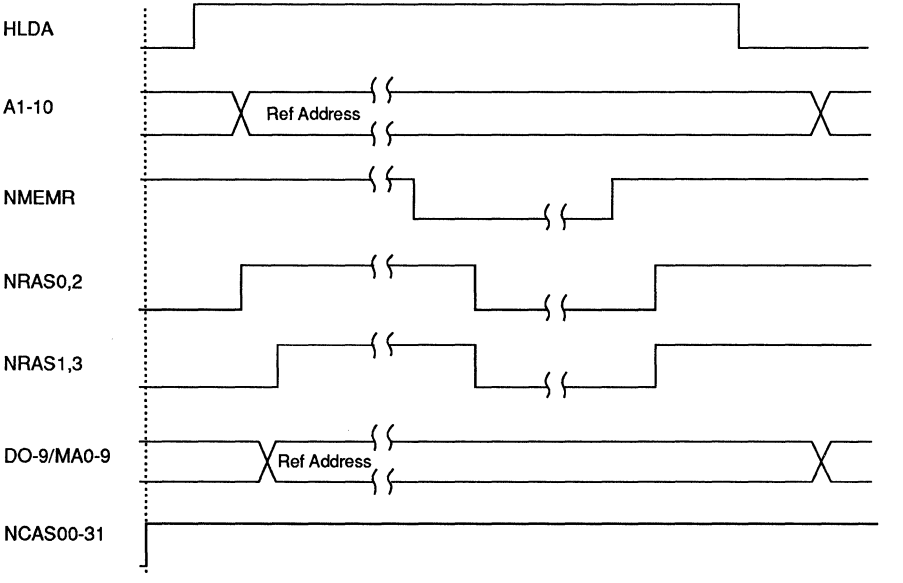



Fig. 4. Refresh Cycle

## ABSOLUT MAXIMUM RATINGS SL9151 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current | $I_{OS}$ | -40 | +40 | mA |
| Output Current | $I_{OS}$ | -40 | +80 | mA |
| Output Current | $I_{OS}$ | -60 | +120 | mA |
| Output Current | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9151

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state* |
| Output High Voltage for Normal Output (IOL = 3.2 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 8 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 12 mA) | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output (IOL = 24 mA) | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output (IOL = 3.2 mA) | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output (IOL = 8 mA) | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output (IOL = 12 mA) | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output (IOL = 24mA) | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for Normal Input | VIH | 2.2 | --- | V | |
| Input Low Voltage for Normal Input | VIL | --- | 0.8 | V | |
| Input High Voltage for CMOS Input | VIH | 0.7VDD | | V | |
| Input Low Voltage for CMOS Input | VIL | --- | 0.3VDD | V | |
| Input Leakage Current | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = Vss |

NOTES:

* VIH = VDD, VIL = Vss

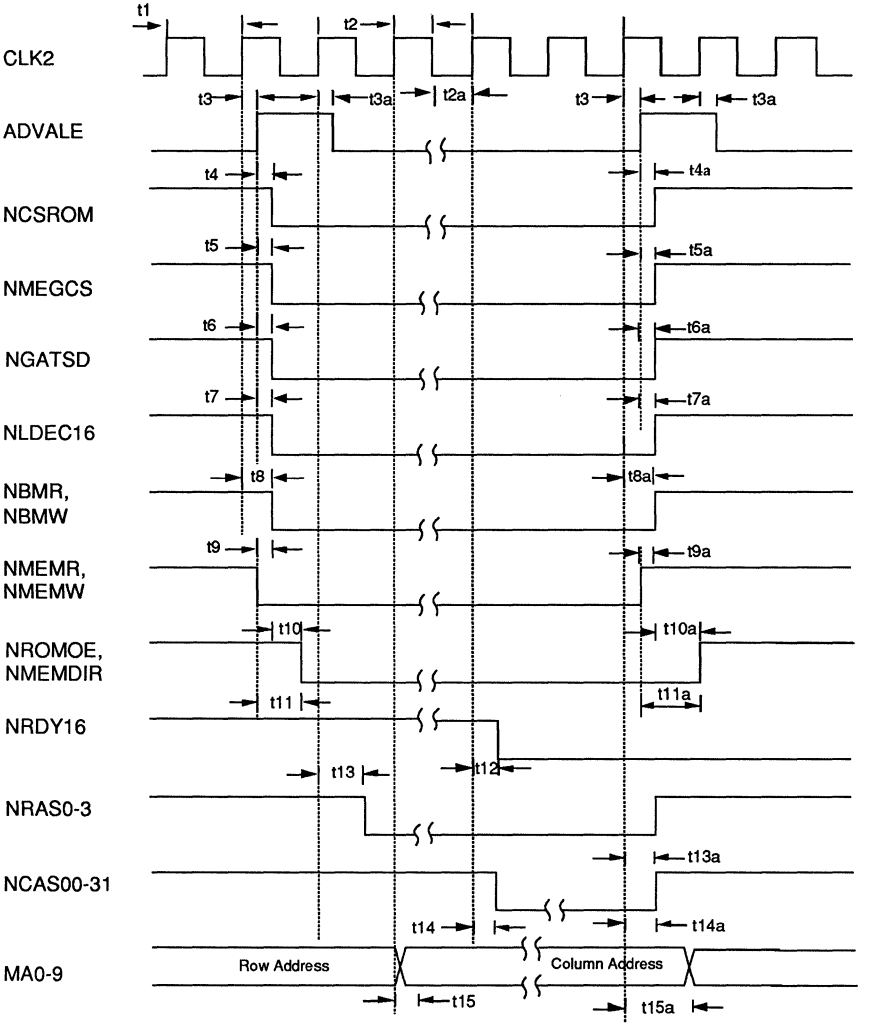
| | | |
|---|---|---|
| RAS0-RAS3, NBMR, NBMW, SA17-SA19 | = 24 mA | (typical) |
| LA17-LA23, MA0-MA9 | = 12 mA | |
| A1-A16, A17-A23 | = 8 mA | |

## AC CHARACTERISTICS SL9151

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| SYMBOL | DESCRIPTION | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| t1 | CLK2 Period | 25 | - | ns |
| t2 | CLK2 High Duration | 7 | - | ns |
| t2a | CLK2 Low Duration | 7 | - | ns |
| t3 | CLK2 to ADVALE (Low to High) | 5 | 20 | ns |
| t3a | CLK2 to ADVALE (High to Low) | 5 | 20 | ns |
| t4 | ADVALE to NCSROM (High to Low) | 5 | 15 | ns |
| t4a | ADVALE to NCSROM (Low to High) | 5 | 15 | ns |
| t5 | ADVALE to NMEGCS (High to Low) | 5 | 15 | ns |
| t5a | ADVALE to NMEGCS (Low to High) | 5 | 15 | ns |
| t6 | ADVALE to NGATSD (High to Low) | 5 | 15 | ns |
| t6a | ADVALE to NGATSD (Low to High) | 5 | 15 | ns |
| t7 | ADVALE to NLDEC16 (High to Low) | 5 | 15 | ns |
| t7a | ADVALE to NLDEC16 (Low to High) | 5 | 15 | ns |
| t8 | CLK2 to NBMR, NBMW (High to Low) | 5 | 12 | ns |
| t8a | CLK2 to NBMR, NBMW (Low to High) | 5 | 12 | ns |
| t9 | NMEMR, NMEMW to NBMR, NBMW (High to Low) | 5 | 10 | ns |
| t9a | NMEMR,NMEMW to NBMR, NBMW (Low to High) | 5 | 10 | ns |
| t10 | NBMR to NROMOE (High to Low) | 0 | 12 | ns |
| t10a | NBMR to NROMOE (Low to High) | 0 | 12 | ns |
| t11 | NMEMR to NROMOE (High to Low) | 5 | 15 | ns |
| t11a | NMEMR to NROMOE (Low to High) | 5 | 15 | ns |
| t12 | CLK2 to NRDY16 | 5 | 12 | ns |
| t13 | CLK2 to NRAS0-NRAS3 (High to Low) | 5 | 12 | ns |
| t13a | CLK2 to NRAS0-NRAS3 (Low to High) | 5 | 12 | ns |
| t14 | CLK2 to NCAS00-31 (High to Low) | 5 | 12 | ns |
| t14a | CLK2 to NCAS00-31 (Low to High) | 5 | 12 | ns |
| t15 | CLK2 to MA0-MA9 Delay | 5 | 15 | ns |

## AC TIMING DIAGRAMS SL9151



## FEATURES

- **Supports 80386SX based AT Designs.**
- **Up to 20 MHz Performance.**
- **Enhanced Fast Page Mode DRAM Controller.**
- **Supports 8 M byte of On-Board Memory.**
- **Shadow RAM Feature.**
- **Programmable Wait State Options.**
- **Can use 256K or 1 Meg DRAMs or a mix.**
- **Supports 100 ns DRAMs at 16 MHz and 80 ns at 20 MHz.**
- **Selectable Wait State Option for Faster DRAMs.**
- **Switchable remapping of 640K - 1 M RAM to the Top of the Address Space.**
- **Advanced CMOS Technology.**
- **100 pin Flatpack.**

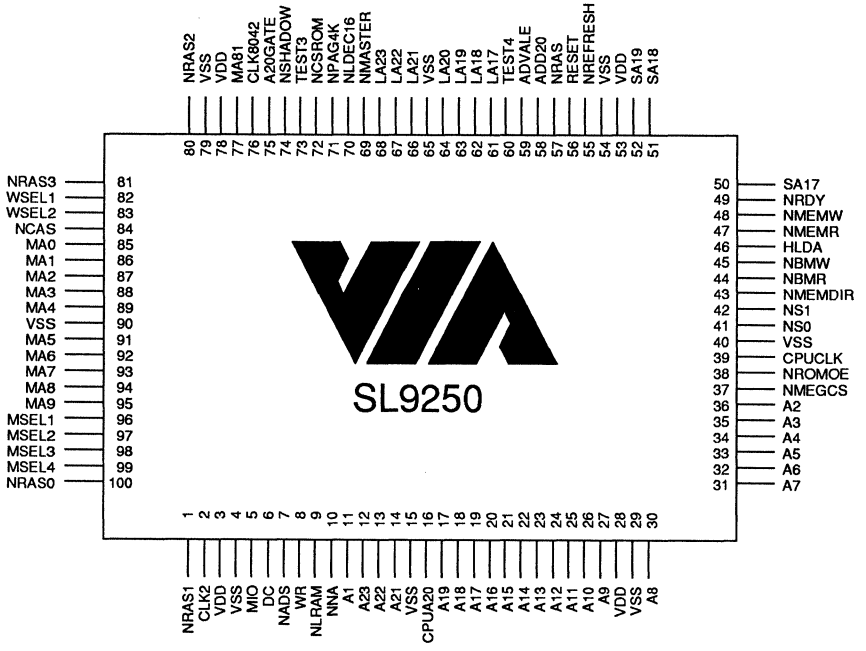
## DESCRIPTION

The SL9250 Memory Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9250 is part of the Personalized AT Logic chipset that implements the Page Mode Memory Control functions which is specific to the 80386SX based PC/AT design and supports up to 20 MHz performance. Other members of the Personalized AT Logic chips include the SL9151 Page Interleave Memory Controller and the SL9350 Page Mode Memory Controller that are specific to 80286 and 80386DX-based PC/AT designs respectively.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

## PINOUT


NRAS2 80
VSS 79
VDD 78
MA81 77
CLK8042 76
A20GATE 75
NSHADOW 74
TEST3 73
NCSROM 72
NPAG4K 71
NLDEC16 70
NMASTER 69
LA23 68
LA22 67
LA21 66
VSS 65
LA20 64
LA19 63
LA18 62
LA17 61
TEST4 60
ADVALE 59
ADD20 58
NRAS 57
RESET 56
NREFRESH 55
VSS 54
VDD 53
SA19 52
SA18 51
NRAS3 81
WSEL1 82
WSEL2 83
NCAS 84
MA0 85
MA1 86
MA2 87
MA3 88
MA4 89
VSS 90
MA5 91
MA6 92
MA7 93
MA8 94
MA9 95
MSEL1 96
MSEL2 97
MSEL3 98
MSEL4 99
NRAS0 100
50 SA17
49 NRDY
48 NMEMW
47 NMEMR
46 HLDA
45 NBMW
44 NBMR
43 NMEMDIR
42 NS1
41 NS0
40 VSS
39 CPUCLK
38 NROMOE
37 NMEGCS
36 A2
35 A3
34 A4
33 A5
32 A6
31 A7
1 NRAS1
2 CLK2
3 VDD
4 VSS
5 MIO
6 DC
7 NADS
8 WR
9 NLRAM
10 NNA
11 A1
12 A23
13 A22
14 A21
15 VSS
16 CPUA20
17 A19
18 A18
19 A17
20 A16
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
27 A9
28 VDD
29 VSS
30 A8
SL9250

## ROM /RAM DECODE

The device provides all necessary circuitry to decode on-board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column DRAMs.

The system can be configured for 512K Bytes to 16M Bytes. The bank selection code & sizes are as follows:

| Msel4 | Msel3 | Msel2 | Msel1 | RAS0/CAS0 | RAS1/CAS1 | RAS2/CAS2 | RAS3/CAS3 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0-640/1M-1M+384K | | | | |
| 0 | 0 | 0 | 1 | 0-640/2M-2M+384K | 1M-2M | | | |
| 0 | 0 | 1 | 0 | 0-640/3M-3M+384K | 1M-2M | 2M-3M | | |
| 0 | 0 | 1 | 1 | 0-640/4M-4M+384K | 1M-2M | 2M-3M | 3M-4M | |
| 0 | 1 | 0 | 0 | 0-640/1M-1M+384K | | | | 256K DRAMs |
| 0 | 1 | 0 | 1 | 0-640/2M-2M+384K | 1M-2M | | | 1M DRAMs |
| 0 | 1 | 1 | 0 | 0-640/6M-6M+384K | 1M-2M | 2M-6M | | |
| 0 | 1 | 1 | 1 | 0-640/10M-10M+384K | 1M-2M | 2M-6M | 6M-10M | |
| 1 | 1 | 0 | 0 | 0-640/1M-4M/4M-4M+384K | | | | |
| 1 | 1 | 0 | 1 | 0-640/1M-4M/8M-8M+384K | 4M-8M | | | |
| 1 | 1 | 1 | 0 | 0-640/1M-4M/12M-12M+384K | 4M-8M | 8M-12M | | |
| 1 | 1 | 1 | 1 | 0-640/1M-4M | 4M-8M | 8M-12M | 12M-16M | |

**Table 1**

When Test3 input is tied low, the 384K Re-map to the top of the memory space is disabled.

The page size is 2KB if any 256K DRAMs are used and 4KB if only 1M DRAMs are used, by tying NPAG4K High (256K) or Low (1Meg).

When CPU accesses the memory for the first time, the controller runs a one wait state memory cycle and asserts RAS & CAS low at appropriate times (Table 1). RAS is kept asserted while the CAS is deasserted at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with the previous value stored in the register. If a match (hit) is detected, the RAS is held low and CAS is strobed immediately after ADVALE goes low for read cycles, and for write cycles, CAS is asserted 1 CPUCLK later. If a mismatch (miss) is detected then RAS is pulled high for 3 CLK2 cycles before being reasserted and new row address is stored in the row address register. The controller will now run a 1 or 2 wait state memory cycle depending on the switch setting WSEL1 and WSEL2 (Table 3).

CPU Addresses A11-A21 and A1 are passed onto MA0-9 as unlatched row addresses whereas A2-A11 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. RAS, MUX, and CAS are separated by one CLK2 period as shown in the timing diagram. This latching of column addresses allows use of static column DRAMs as well.

## BLOCK DIAGRAM SL9250

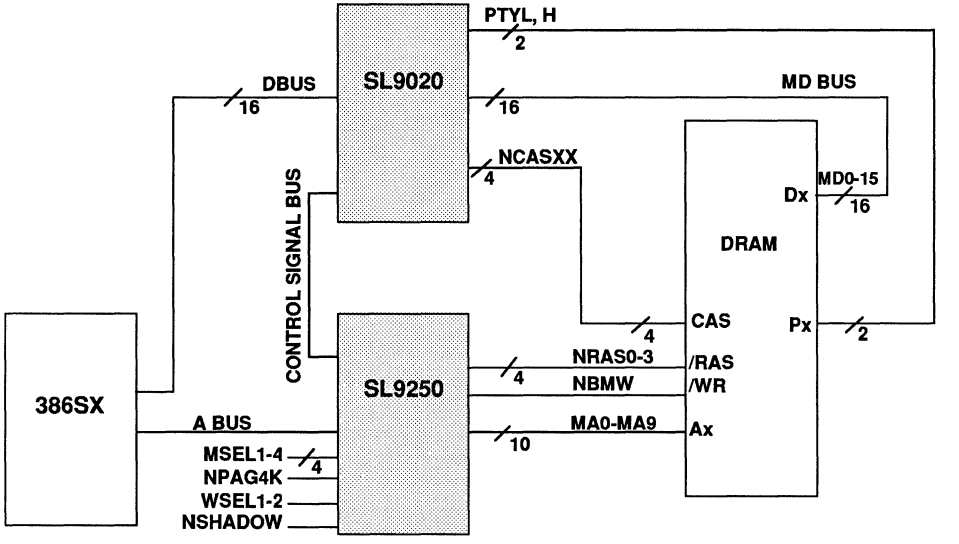



Fig. 1 386SX RAM BLOCK DIAGRAM

ROM/ RAM CONTROL (Cont'd.)

The SL9250 Memory Controller provides all the circuitry needed to generate RAM/ROM controls. RAM controls for Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS), RAM Read Write (NBMW, NBMR), Ready from 16 bit on board RAM read write (NRDY), next CPU address (NNA), and non on-board memory cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

| MIO | DC | WR | ADDRESS | CYCLE TYPE |
|---|---|---|---|---|
| 1 | 0 | 0 | | MEM CODE READ |
| 1 | 0 | 1 | 2/0 | HALT/SHUTDOWN |
| 1 | 1 | 0 | | MEM DATA READ |
| 1 | 1 | 1 | | MEM DATA WRITE |
| 0 | 0 | 0 | | INTA |
| 0 | 0 | 1 | | NOT POSSIBLE |
| 0 | 1 | 0 | | I/O DATA READ |
| 0 | 1 | 1 | | I/O DATA WRITE |

**Table 2**

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 16 bit, on board, memory miss can be set using the following table.

| CPU SPEED | WSEL1 | WSEL2 | WAIT STATES READ | WAIT STATES WRITE | MEMORY SPEED (ns) |
|---|---|---|---|---|---|
| 16 | 0 | 0 | 2 | 2 | -10 |
| | 1 | 0 | 2 | 1 | -10* |
| | 1 | 1 | 1 | 1 | -8* |
| 20 | 0 | 0 | 2 | 2 | -8 |
| | 1 | 0 | 2 | 1 | -8* |
| | 1 | 1 | 1 | 1 | -6* |

* Page Mode CAS write time ≤ 1 CLK2 period.

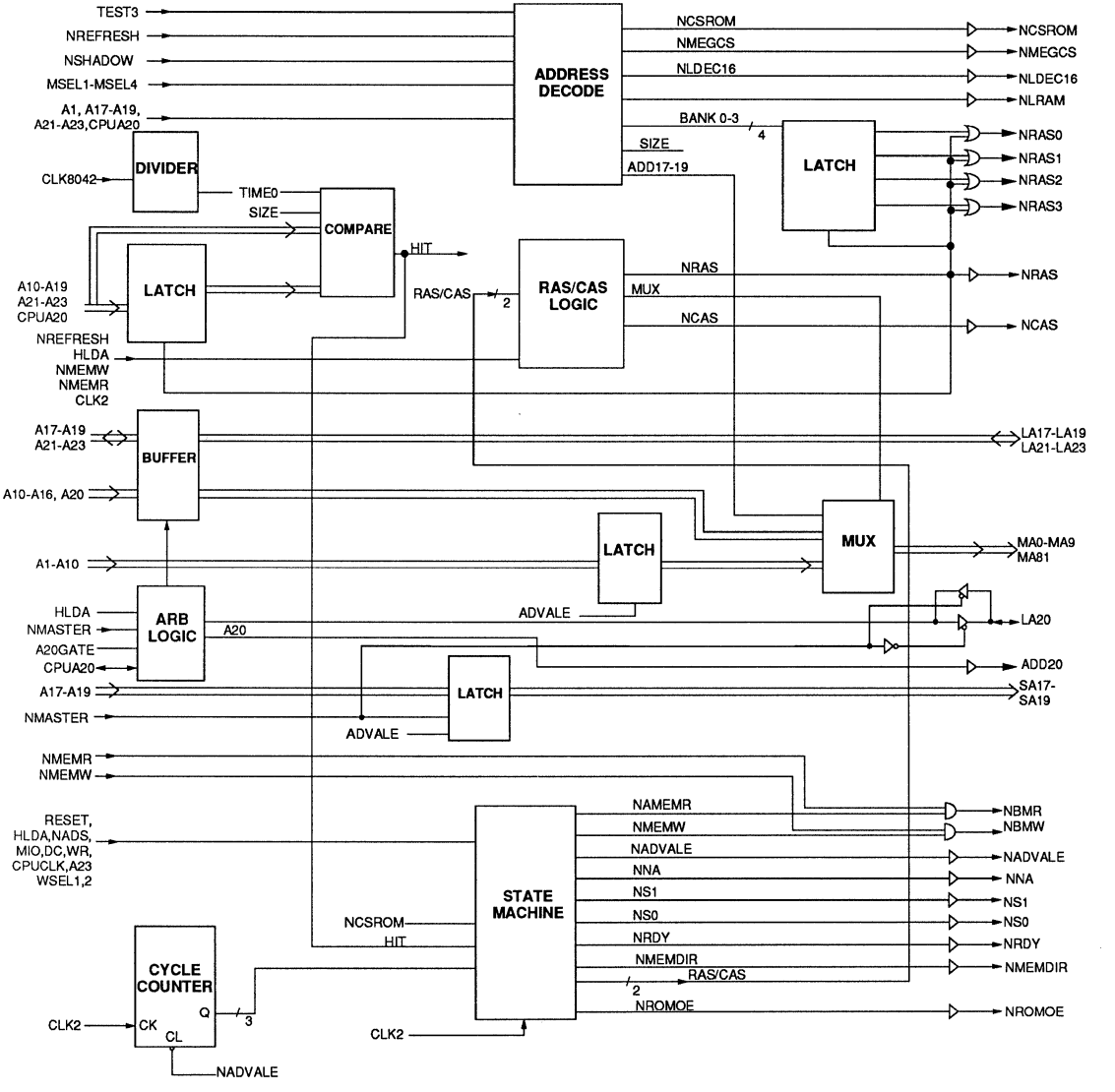
**Table 3**

ROM controls NCSROM & NROMOE are asserted low at appropriate time when address 0E0000h-0FFFFFh (low) or FE0000h-FFFFFFh (high) is decoded during a memory cycle. The timing relationship is shown in the timing diagram. These will be disabled if Shadow RAM option is used. When Shadow RAM option is used by pulling NSHADOW pin low, the ROM code is copied in the corresponding RAM location by BIOS, and the subsequent ROM code reads will be decoded as RAM reads & will be much faster. BIOS can be customized to activate this option at boot. The NSHADOW option affects the 128K region immediately below 1 Meg.

REFRESH SUPPORT

The SL9250 provides support for DRAM refresh. During refresh NRAS0-3 are asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by the SL9025 Address Controller is passed from A Bus to MA Bus.

## BLOCK DIAGRAM SL9250



RAM

System RAM is added as shown in Fig. 1. 16 Bit memory data is connected to the MD Bus. Memory data flow is from/to the MD Bus and to/from Dbus via the SL9020 Data Controller. Parity data is generated and checked in the SL9020 through parity byte bits PTYL and PTYH. The SL9020's output memory CAS strobes are: NCASA02, NCASA13, NCASB02, NCASB13.

RAM address is passed or latched internally in the SL9250 as necessary from A Bus to memory MA Bus (10 Bit). The MA Bus features 12ma drive capability. The SL9250 provides 24ma direct drive lines for memory RAS (NRAS0-NRAS3) as well as memory Write (NBMW). Eleven signals are output by the SL9250 to facilitate system control during RAM transfers. Their function and destination are covered in Table 4.

| SIGNAL | DESTINATION | FUNCTION |
|---|---|---|
| ADVALE | SL9025 Address Controller | Used to latch the 386SX address bus A1-A16 to the system address bus SA1-SA16. |
| | Internal | Used to latch the 386SX address bus A17-A19 to the system address bus SA17-SA19. Transfers and latches 10 Bit CAS address (MA0-MA9) and NLDEC16. Clears cycle counter. |
| NBMR | SL9025 Address Controller | Trailing edge used to latch parity error. |
| NBMW | SL9011 System Controller | Used to gate CPURST and drive WE for RAM. |
| NCAS | SL9020 Data Controller | Used to gate SL9020 CAS output drivers: CASLA, CASLB, CASHA and CASHB. Trailing edge used to latch parity error. |
| NMEMDIR | SL9020 Data Controller | Sets MDBUS/DBUS direction. HI = D→MD |
| NLDEC16 | SL9011 System Controller | Indicates a local RAM/ROM decode. |
| MEGCS | SL9011 System Controller | Indicates a local RAM/ROM decode less than 1Meg address. |
| NRDY | SL9011 System Controller | Indicates the memory is ready with data. |
| NNA | 386SX | Pipeline request to 386SX. |
| NS0-NS1 | SL9011 System Controller | 286 compatible status signal indicating a Read, Write, interrupt acknowledge or idle state. |

**Table 4. SL9250 Control Signal Function**

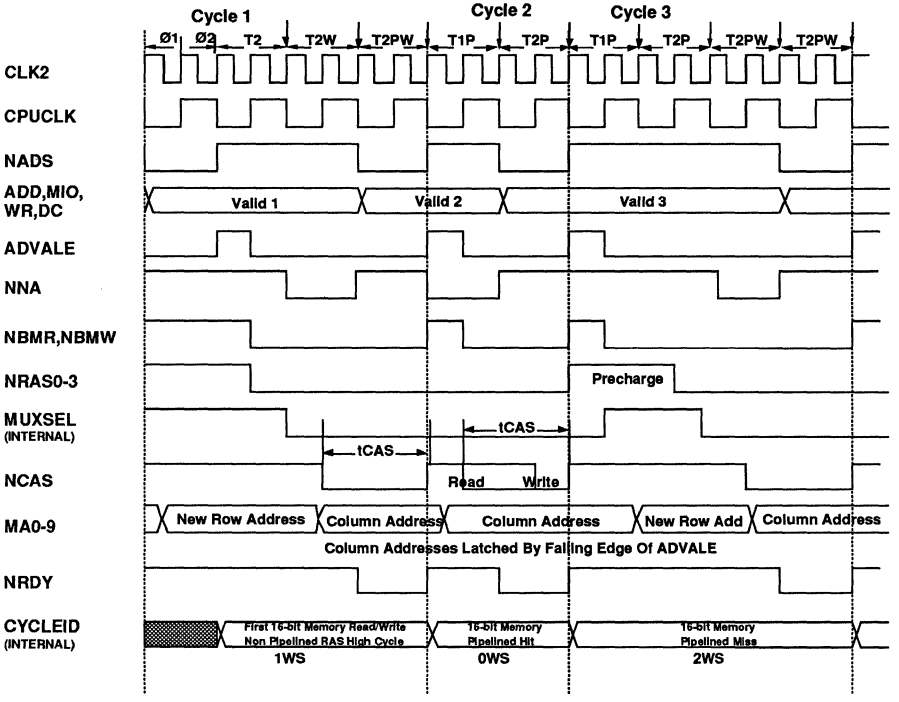



Fig. 2 On-Board Memory Timing Diagram

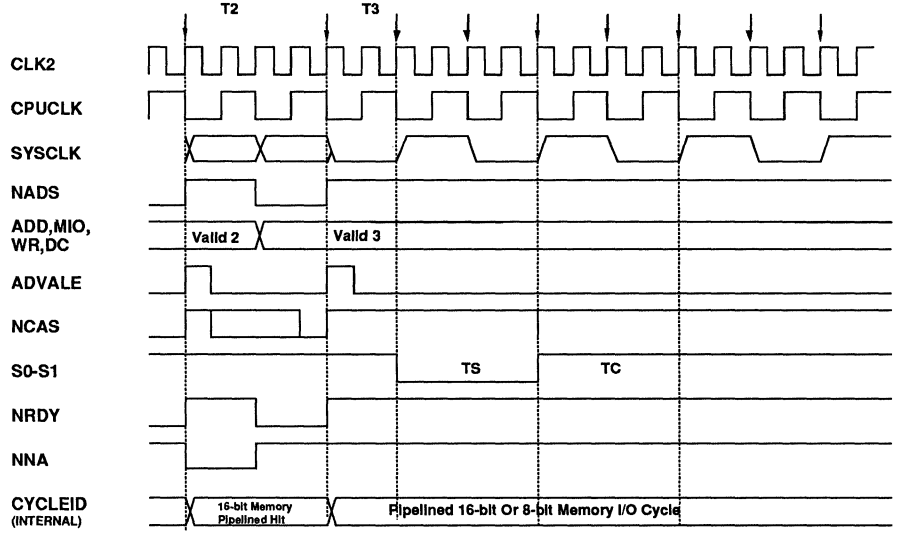



Fig. 3 Off-Board Memory Timing Diagram

RAM (Cont'd)

A local memory cycle (cycle1 in Fig.2), begins during T1 when the 386SX asserts NADS, MIO, and DC. SL9250 output NLDEC16 asserts, indicating a memory decode within the range specified by memory select jumpers MSEL1-MSEL4, as shown in Table 1. If the present address is within the lower 1 meg range, then MEGCS will also assert at this time. "ROW" addresses A11-A19 and CPUA20 are passed directly through the SL9250 into MA0-MA9. ADVALE is asserted during 01 (Phase 1, CPUCLK low) of T2. If the cycle is a Write, the start of T2 02 (Phase 2) brings NBMW valid, thus setting RAM WE. At this time, a RAS line will assert (NRAS0-NRAS3) strobing the MA0-MA9 address into the appropriate bank. ADVALE negates at 02, latching A1 through A10 in the SL9250. T2W 01 enables latched column address on MA0-MA9, and sets NNA to the 386SX requesting the next cycle to be pipelined. T2W 02 asserts NCAS to the SL9020 Data Controller, where the appropriate CAS line CASLA, LB, HA or HB is asserted, thus strobing the RAM column address and enabling RAM data output. NRDY to CPU (via SL9011) asserts at T2PW, signaling CPU to latch RAM data at end of T2PW 02. NADS also asserts, indicating a valid pipeline cycle in response to the previous NNA. T2WP 02 ends with CPUCLK dropping low, finishing the first cycle: NBMW, NCAS, NRDY and NADS negate, RAM data latches in the 386SX CPU.

The next cycle, (cycle 2 in Fig. 3), T1P, asserts ADVALE, which enables a new column address on MA1-MA9. NNA is asserted, requesting the next cycle to be pipelined. AT T1P 02 advale negates, latching column addresses, asserts NBMR or NBMW as appropriate, and NCAS. NCAS assertion gives rise to the assertion of the appropriate RAM CAS line CASLA, LB, HA, or HB. T2P 01 negates NNA and asserts NRDY, signaling a page hit. The 386SX asserts NADS indicating a new pipeline cycle. T2P 02 end latches RAM data in the 386SX and negates NADS.

Cycle 3 begins in state T1P01 with NADS, NBMW, NRDY, NBUS, NNA NCAS and NRAS negated. ADVALE is asserted. Since NRAS is negated, a page miss is indicated. 02 negates ADVALE, asserts NBMW, and sets internal muxsel high. The mux is now driving a new row address on MA0-MA9. T2P 02 asserts the appropriate NRAS0-NRAS3 strobe, latching DRAM row address. T2P02 end drops internal muxsel, presenting as new column address on MA0-MA9. T2PW02 negates NCAS, thus strobing a new column address into DRAM and enabling DRAM output. The second wait state T2PW01 asserts NRDY. Data for cycle 3 will then be latched in the CPU at the end of 02.

ROM

System ROM is enabled from 0E0000H to 0FFFFFH, or from FE0000H to FFFFFFH. Two wait states are forced for any ROM access. If shadowing is selected, by asserting NSHADOW high on SL9250, NROMOE and NCSROM signals are not asserted during the 386SX Read cycle and a RAM cycle is started instead.

System ROM is added as shown in Fig.4. 16 Bit ROM data out is connected to the MD Bus. 15 Bit ROM address input is connected directly to the 386SX A Bus. ROM enable signals OE and CE are connected to the SL9250 output signals NROMOE and NCSROM. Data path is from MD Bus to 386SX D Bus via the SL9020 Data Controller.

A Read cycle is started when the 386SX asserts MIO, D/C and NADS. The "cycle" is latched internally on the rising edge of CLK2, when CPUCLK is high and a valid ROM address is on A1, A17-A19, A21-A23, and CPUA20. NCSROM is first asserted when a valid ROM address is decoded at T1A. When CPUCLK goes low and CLK2 rises high, (T2A), NBUS16 is asserted for the duration of CPUCLK low, indicating to the 386SX a 16 bit cycle. Next CLK0, CPUCLK goes high and CLK2 rising high (T2B), NROMOE asserts, thus enabling ROM outputs. NMEMDIR asserts at this time, as well, signaling the SL9020 Data Controller to switch the memory data path from MDBus to DBus. After 2 wait states, on CLK2 rising high at T2W2B, NRDY asserts, signaling the SL9011 Controller that data is ready. The SL9011 drops NCPURDY, the CPU latches Bus data, and enters the second 16 Bit cycle by negating BE0, BE1, and NADS at T12 A. The second cycle repeats as the first. After the last ROM access, a valid ROM address will not be decoded and thus NCSROM, NROMOE, and NMEMDIR will be negated in T1 A.

## BLOCK DIAGRAM SL9250

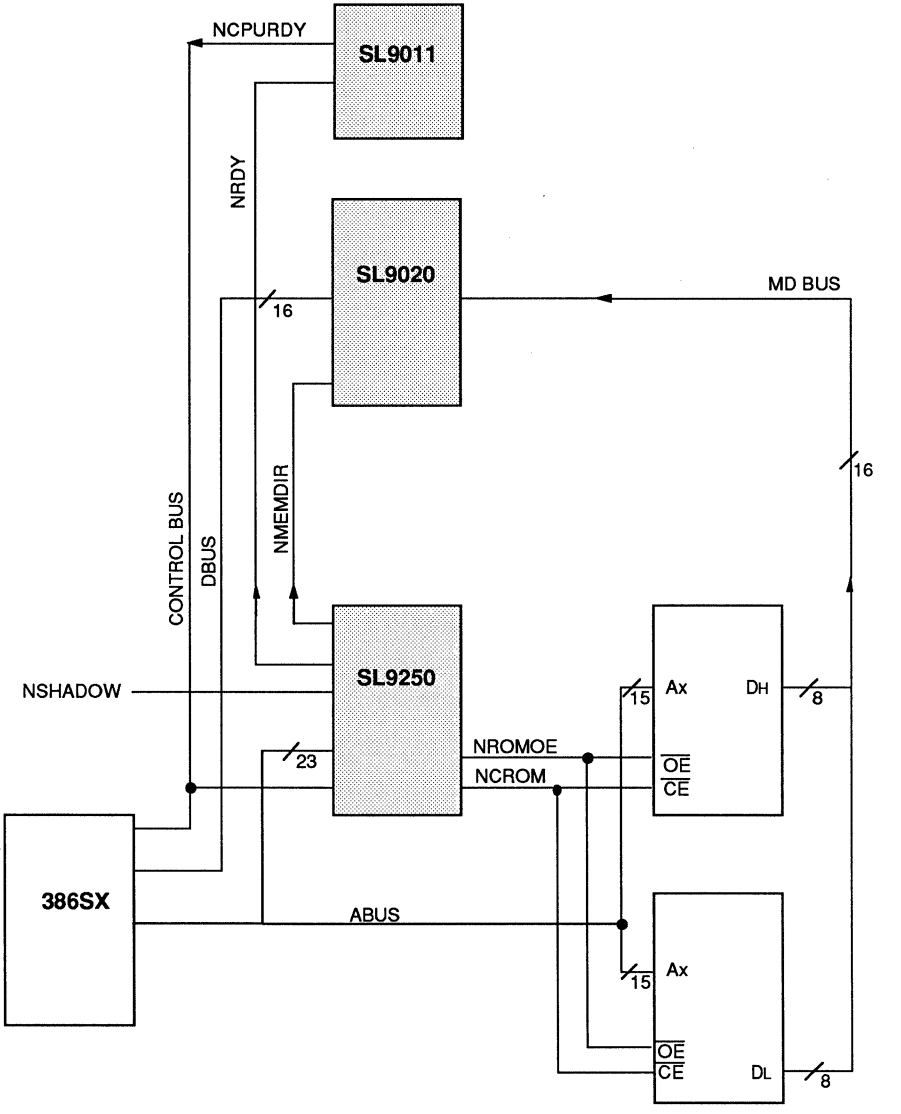



**Fig. 4 386SX ROM BLOCK DIAGRAM**

## AC TIMING DIAGRAMS SL9250

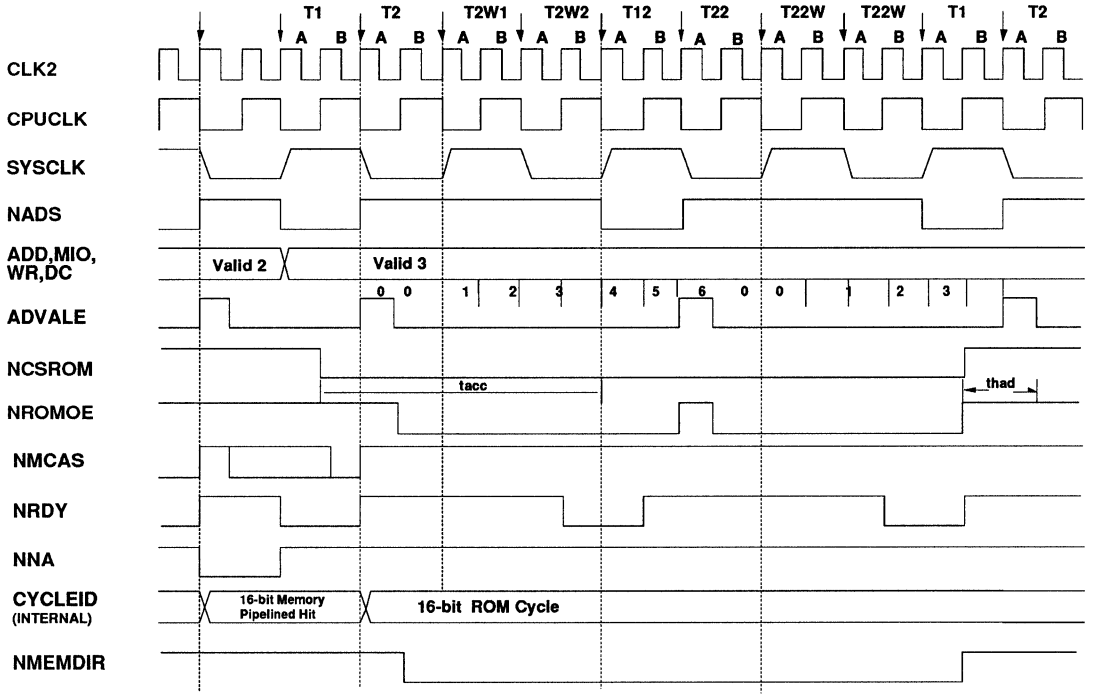



Fig. 5 Timing Diagram for BIOS ROM cycle (16-bit memory)

## PIN DESCRIPTION SL9250

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A1-A16 | 11,36,35,34,33, 32,31,30,27, 26,25,24,23, 22,21,20 | I | CPU Address Bus. |
| A17-A19 A21-23 | 19,18,17, 14,13,12 | I/O | CPU Address Bus. |
| A20GATE | 75 | I | CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH. |
| ADD20 | 58 | O | Decoded 20-bit address bit used to generate address decode for 1 M RAMs. |
| ADVALE | 59 | O | Advanced Address Latch Enable from memory controller. It latches local bus address for the system bus. |
| CLK2 | 2 | I | Input Clock used to clock internal state machine. It is 2 times the frequency of the CPUCLK. |
| CLK8042 | 76 | I | 7 MHz clock input. It is used to internally generate a RAS time out. (Page mode.) |
| CPUA20 | 16 | I/O | CPU Address Bus. |
| CPUCLK | 39 | I | Input Clock simulating 386SX internal clock. It is CLK1 divided by two. |
| DC | 6 | I | CPU Status Signal. Differentiates between Data and Control instructions. |
| HLDA | 46 | I | CPU Output Signal, asserted to signal that the CPU has relinquished control of the bus to the requesting device: MASTER or DMA. It is used to tri-state SLOT addresses during master. |
| LA17-LA23 | 61,62,63,64, 66,67,68 | I/O | Local address bus. Directly drives AT-SLOT signals LA17-LA23. |
| MA0-MA9 | 85,86,87,88, 89,91,92,93, 94,95 | O | RAM Address Bus Output. Directly drives DRAM address inputs. |
| MA81 | 77 | O | RAM Address pin for 1M RAMs. Used in place of MA8 for 1M DRAMs. |

## PIN DESCRIPTION SL9250 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| MIO | 5 | I | CPU output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is being used by the state machine to generate memory and I/O signals for the system. |
| MSEL1-4 | 96,97,98,99 | I | On-board Fast RAM memory size and type select. They are set as indicated in Table 1. The setting will determine the appropriate RAS and CAS outputs. Internally pulled down. |
| NADS | 7 | I | CPU output control signal, asserted when Address Bus outputs are valid. |
| NBMR | 44 | O | Buffered Memory Read signal. Used to latch addresses in the SL9025 Address Controller chip. |
| NBMW | 45 | O | Buffered Memory Write signal. Used to directly drive DRAM write input. |
| NCSROM | 72 | O | LOW assert ROM Chip Select. Connects directly to system ROM CS. |
| NLDEC16 | 70 | O | Decode signal for on-board local HIGH-speed RAM. Indicates a local DRAM transfer is in process. |
| NLRAM | 9 | O | Decode for on-board external HIGH speed 16 Bit RAM. |
| NMASTER | 69 | I | Asserted when an external device has control of the AT Bus at slot card output. Used to set address direction from SLOT to system. |
| NCAS | 84 | O | Memory column address strobe. Asserted when either CPU or DMA is accessing the memory. Used to drive SL9020 NCAS input. |
| NMEGCS | 37 | O | Select Decode for lower 1M of memory. Used to drive SL9011 NMEGCS input. |
| NMEMDIR | 43 | O | Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input. |
| NMEMR | 47 | I | Read Memory command from SL9011/SLOT. |

## PIN DESCRIPTION SL9250 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NMEMW | 48 | I | Write Memory command from SL9011/SLOT. |
| NNA | 10 | O | CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle. |
| NPAG4K | 71 | I | Active LOW Page size = 4K option; when 1M DRAMs are used. Left HIGH for 256Ks or mixes. |
| NRAS | 57 | O | LOW assert Row address strobe. Not used in normal operation. |
| NRAS0-3 | 100,1,80,81 | O | Row address strobes for Banks 0,1,2 & 3 for the on-board memory. Generated during CPU or DMA cycle for memory access. Used to directly drive DRAM RAS inputs. |
| NRDY | 49 | O | Asserted one clock cycle after NNA is asserted at the end of a local memory cycle. Used to signal SL9011 that data is ready. |
| NREFRESH | 55 | I | On-board RAM refresh signal. Generated from REFREQ input. |
| NROM0E | 38 | O | Enables ROM output during ROM read cycles. Connects directly to ROMOE pin. |
| NS0,1 | 41,42 | O | 80286 compatible status signals for the AT System Controller SL9011. |
| NSHADOW | 74 | I | Selectable option for Shadow RAMs. LOW enables Shadow RAM feature. |
| RESET | 56 | I | Active HIGH Reset from system controller. |
| SA17-19 | 50,51,52 | O | System Address Bus. |
| TEST3 | 73 | I | Optional disable for 684K - 1M [384K] remap. |
| TEST4 | 60 | I | Test Pin - Not connected. |
| VDD | 3,28,53,78 | - | +5V. Power. |
| VSS | 4,15,29,40, 54,65,79,90 | - | 0V. Ground. |
| WR | 8 | I | CPU output control signal Write. |
| WSEL1,2 | 82,83 | I | Wait-state Select options. Refer to Table 3 for proper setting. Internally pulled up. |

## AC TIMING DIAGRAMS SL9250

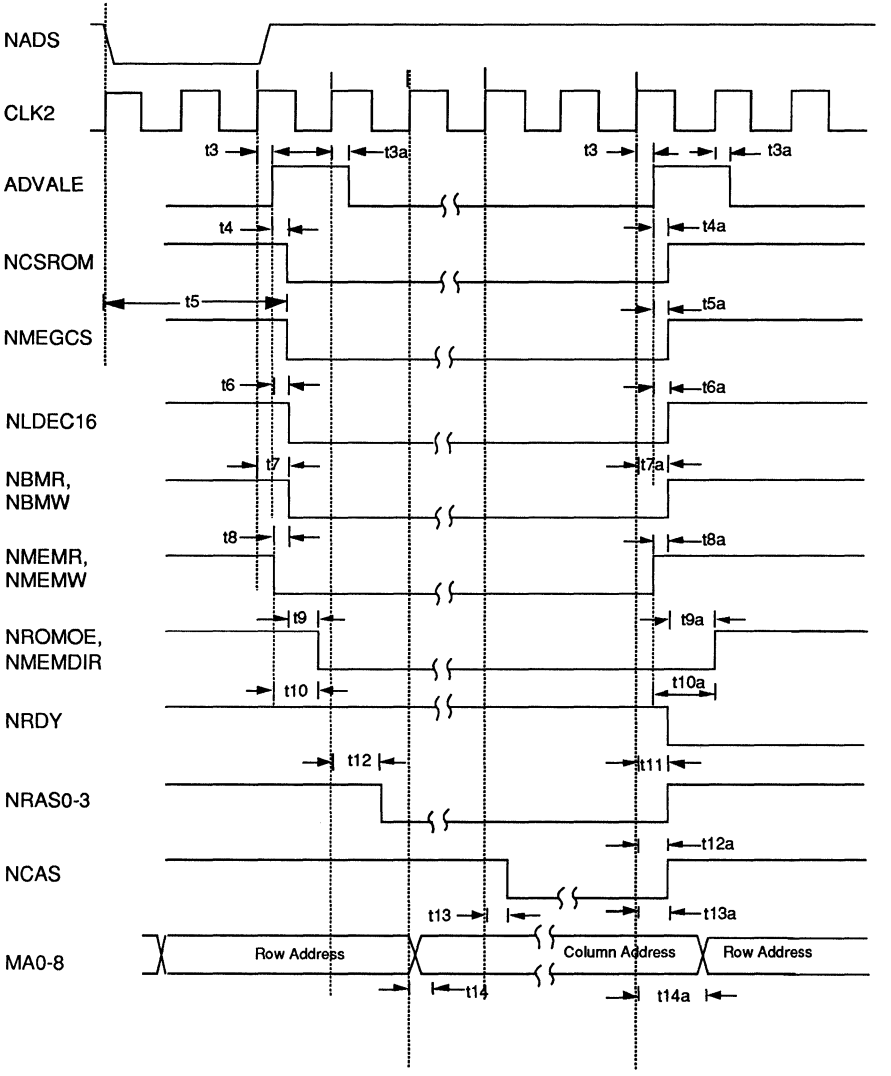



**Fig. 6 Set-up and Hold Times**

## ABSOLUT MAXIMUM RATINGS SL9250 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current *note 2 | $I_{OS}$ | -40 | +40 | mA |
| Output Current *note 3 | $I_{OS}$ | -40 | +80 | mA |
| Output Current *note 4 | $I_{OS}$ | -60 | +120 | mA |
| Output Current *note 5 | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NROMOE, NS0, NS1.
3. A1, A17 - A19, A21-23, CPUA20.
4. ADD20, MA0-MA9, MA81, LA17 - LA23, NRAS, SA17 - SA19.
5. NBMW, NRAS0 - NRAS3.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9250

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | TBD | TBD | mA | 20 MHz |
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state |
| Output High Voltage *note 1 | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output *note 2 | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output NBMW, NRAS0-NRAS3 | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output *note 3 | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output A1, A17-A19, A21-23, CPUA20 | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output *note 4 | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output NBMW, NRAS0-NRAS3 | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for All Inputs | VIH | 2.2 | | V | |
| Input Low Voltage for All Inputs | VIL | | 0.8 | V | |
| Input Leakage Current *note 5 | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current, Tri-state *note 6 | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = Vss |
| Input Current, Pull-up *note 7 | IILU | -335 | -204 | µA | VI = .4V |
| Input Current, Pull-up *note 8 | IIHU | -135 | -124 | µA | VI = 2.4V |
| Input Current, Pull-up MSEL1-MSEL4 | IILD | TBD | 26 | µA | VI = .4V |
| Input Current, Pull-up MSEL1-MSEL4 | IIHD | 14 | 106 | µA | VI = 2.4V |

NOTES:
1. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, A1, A17-A19, A21-23, CPUA20
2. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
3. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1
4. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
5. A1-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, NREFRESH, RESET, WR
6. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
7. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2
8. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2

## AC CHARACTERISTICS SL9250

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| SYMBOL | DESCRIPTION | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| t1 | CLK2 Period | 25 | - | ns |
| t2 | CLK2 High Duration | 7 | - | ns |
| t2a | CLK2 Low Duration | 7 | - | ns |
| t3 | CLK2 to ADVALE (Low to High) | 5 | 20 | ns |
| t3a | CLK2 to ADVALE (High to Low) | 5 | 20 | ns |
| t4 | ADVALE to NCSROM (High to Low) | 5 | 15 | ns |
| t4a | ADVALE to NCSROM (Low to High) | 5 | 15 | ns |
| t5 | NADS to NMEGCS (High to Low) | 5 | 15 | ns |
| t5a | NADS to NMEGCS (Low to High) | 5 | 15 | ns |
| t6 | ADVALE to NLDEC16 (High to Low) | 5 | 15 | ns |
| t6a | ADVALE to NLDEC16 (Low to High) | 5 | 15 | ns |
| t7 | CLK2 to NBMR, NBMW (High to Low) | 5 | 12 | ns |
| t7a | CLK2 to NBMR, NBMW (Low to High) | 5 | 12 | ns |
| t8 | NMEMR, NMEMW to NBMR, NBMW (High to Low) | 5 | 10 | ns |
| t8a | NMEMR,NMEMW to NBMR, NBMW (Low to High) | 5 | 10 | ns |
| t9 | NBMR to NROMOE (High to Low) | 0 | 12 | ns |
| t9a | NBMR to NROMOE (Low to High) | 0 | 12 | ns |
| t10 | NMEMR to NROMOE (High to Low) | 5 | 15 | ns |
| t10a | NMEMR to NROMOE (Low to High) | 5 | 15 | ns |
| t11 | CLK2 to NRDY | 5 | 12 | ns |
| t12 | CLK2 to NRAS0-NRAS3 (High to Low) | 5 | 12 | ns |
| t12a | CLK2 to NRAS0-NRAS3 (Low to High) | 5 | 12 | ns |
| t13 | CLK2 to NCAS (High to Low) | 5 | 12 | ns |
| t13a | CLK2 to NCAS (Low to High) | 5 | 12 | ns |
| t14 | CLK2 to MA0-MA8 Delay | 5 | 15 | ns |

(TA = 25 ° C, VDD = V1 = 5V, fo = 1MHz)

| PARAMETERS | SYMBOL | MIN. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | --- | 16 | Pf | note 1 |
| Input Pin Capacitance | CIN | --- | TBD | Pf | note 2 |
| Output Pin Capacitance | COUT | --- | 16 | Pf | note 3 |
| Output Pin Capacitance | COUT | --- | 18 | Pf | note 4 |
| I/O Pin Capacitance | CI/O | --- | 16 | Pf | note 5 |
| I/O Pin Capacitance | CI/O | --- | 23 | Pf | note 6 |

NOTES:
1. A2-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, REFRESH, RESET, WR
2. NSHADOW, MSEL1-MSEL4, NPAG4K, TEST 3, TEST 4, WSEL1, WSEL2
3. ADVALE, ADD20, MA0-MA9, MA81, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NRAS, NROMOE, NS0, NS1
4. NBMW, NRAS0-NRAS3
5. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
6. NBMW, NRAS0-NRAS3

FEATURES

- Supports 80386SX based AT Designs.
- Up to 25 MHz Performance.
- Enhanced Fast Page Mode/Page Interleave.
- Supports 8 M bytes of on Board Memory.
- Shadow RAM Feature
  - 16K granularity
  - 8 remap options
  - System, video, LAN BIOS
- Programmable Memory Options
  - ROM chip select in 16K granularity
  - Wait states for 16 Bit ROM
  - Hit wait states (0-3)
  - Miss wait states (1-4)
  - RAS and CAS precharge
- Programmable Memory Partitioning
  - Disable (on board) memory to 0K in 128K resolution
  - 512 X 512 split
  - Memory backfill
- Can use 256K x 1, 1 M x 1 and 256K x 4 DRAMs or a mix.
- Staggered RAS Refresh.
- Supports Pipeline and Non-Pipeline Modes.
- Fast Gate A20 and Fast Reset.
- Backward Compatible to SL9250.
- Advanced, Low Power CMOS Technology for Laptops.
- 100 pin Flatpack.

## DESCRIPTION

The SL9251 Memory Controller supports PC/AT systems based on Intel's 80386SX microprocessor. It is a member of VIA's FlexSet family which utilizes the same core logic across the entire PC/AT spectrum. The SL9251 is backward compatible with existing memory controllers for the 80386SX (SL9250). Boards designed using the SL9250 can be used with the new SL9251 without modifications and with existing BIOS. In order to take advantage of the SL9251's many new programmable features, minor board modification and a modified BIOS is required for enhanced performance.

The SL9251 offers the advanced memory control functions and features needed to develop high performance PC/AT systems without using external TTL Logic. The SL9251 supports two-way and 4-way page interleave mode for 80386SX based designs. The Page interleave option can be enabled or disabled using the configuration registers. All memory banks which are interleaved use the same type of memory. Designers can enable the staggered RAS option during refresh, which minimizes power surge. Both pipeline and non-pipeline modes are supported by enabling or disabling the next address controls, and providing ready at the correct time.

### RAM & ROM OPTIONS

The programmable RAM options supported by the SL9251, offer a very high level of design flexibility to the PC/AT system designer. DRAM page 'HIT' wait states are programmable from 0 to 3, and the DRAM page 'MISS' wait states are programmable from 1 to 4. This allows systems designers to design PC/AT systems capable of handling a wide range of DRAM speeds with wide variety of CPU speeds including 33 MHz Cache based systems. The 'MISS' wait states for write operation can be programmed to one less than the Read cycle. A minimum of one wait state is forced if a 'MISS' cycle is detected. The RAS precharge time is also programmable, typically a multiple of the CLK2 (2 to 5). Start of CAS can be independently programmed for HIT, read MISS and write MISS cycles. RAS to address is programmable in steps and 1/2 CLK2 increments.

In addition to the RAM, programming options for ROM are also supported. ROM chip select is programmable in 16K granularity. For ROM, 1 to 10 programmable wait states are supported.

### REMAP

In order to enhance the system and video performance, the SL9251 has been designed to support advanced shadow RAM features. The memory address space from '00A0000' to 00FFFFF' can be shadowed in 16K granularity, for system, video, LAN and other types of BIOS. This memory space is write protected in 16K granularity. The chip also supports Read/Write for local RAM using the 'backfill' option. By disabling the local RAM, the SL9251 allows system designers to Read and Write to the system bus. The local memory from 0 to 640K can be disabled with 128K granularity. The SL9251 offers many memory remap options which are listed in Table 1.

DESCRIPTION (cont'd.)

**Table 1. Remap Options**

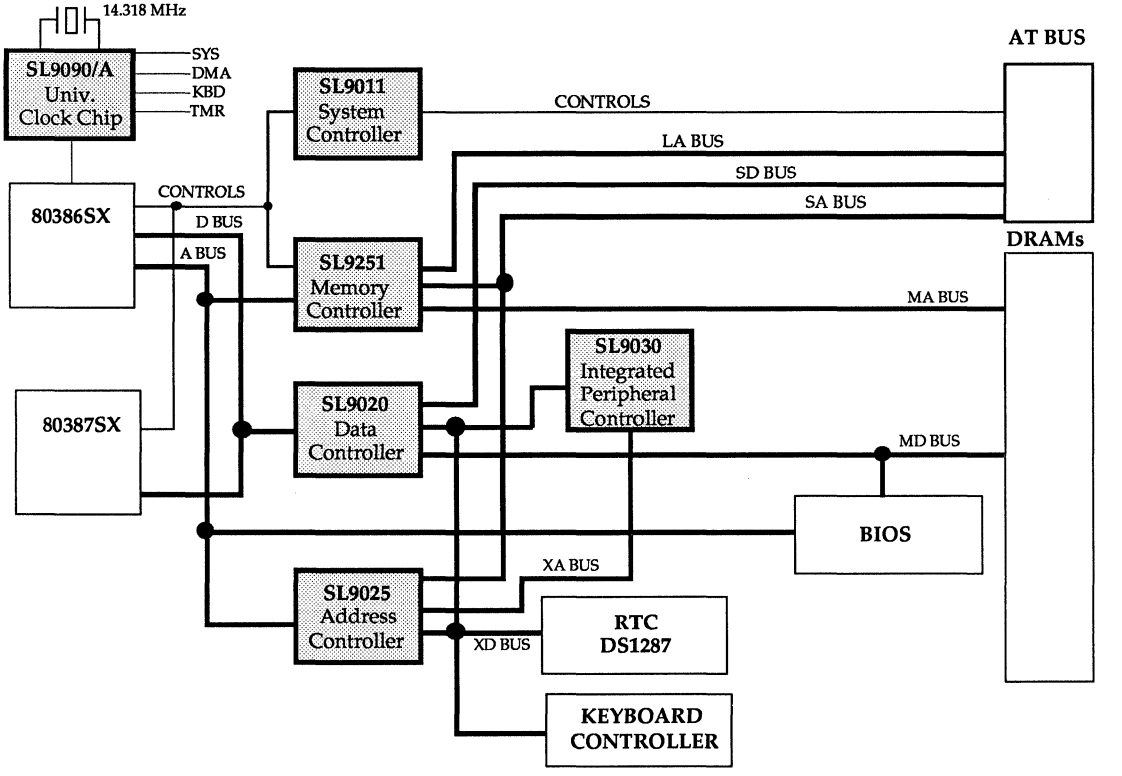
| |
|---|
| NO REMAP |
| 512K (512 X 512 SPLIT) |
| 128K (384K - 256K (SYSROM + ALL OPTION ROM) |
| 256K (384K - 128K LOCAL ROM) |
| 288K (384K - LOCAL SYS ROM + VIDEO ROM) |
| 320K (384K - 64K LOCAL ROM) |
| 352K (384K - 32K LOCAL ROM) |
| 384K REMAPPED FULLY. (NO SHADOW) |

ADDITIONAL FEATURES

OS/2 performance is enhanced significantly by using the Fast GATEA20 and Fast CPU Reset features offered by the SL9251. Port 92, defined in the IBM PS/2 technical manual, is used to provide faster performance.

Configuration registers are used to program these features during the system set up.

The SL9251 is available in a 100 pin plastic flat pack. It has been designed using advanced 1.2 micron double layer metal CMOS technology.




**FlexAT/386SX System Block Diagram**

# SL9350
# 80386DX Page Mode Memory Controller
PRELIMINARY

## FEATURES

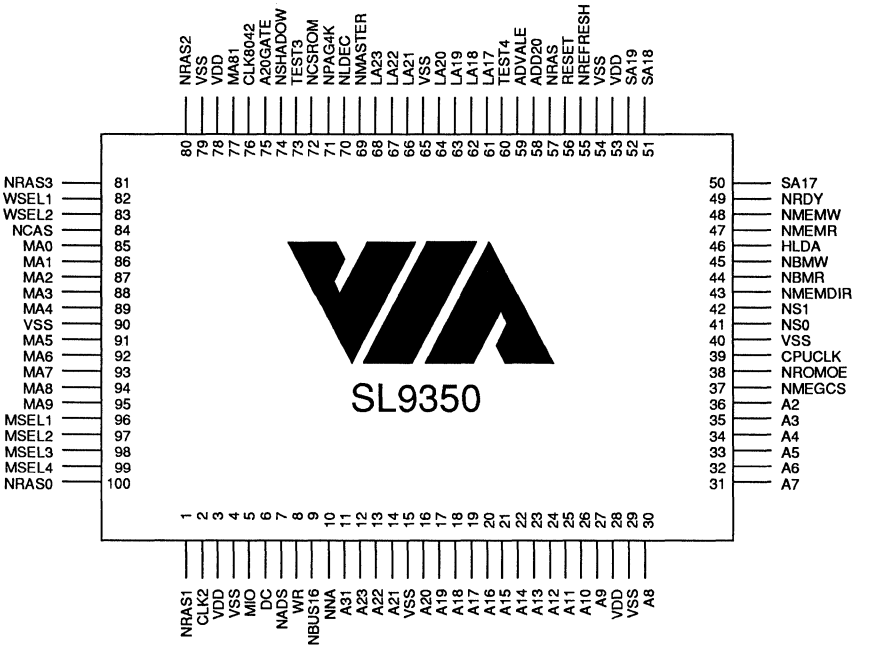
- Supports 80386DX based AT Designs.
- Up to 25 MHz Performance.
- Enhanced Fast Page Mode DRAM Controller.
- Supports 16 M byte of on Board Memory.
- Shadow RAM Feature.
- Programmable Wait State Options.
- Can use 256K or 1 Meg DRAMs or a mix.
- Supports 100 ns DRAMs at 16 MHz and 80 ns at 20 MHz.
- Selectable Wait State Option for Faster DRAMs.
- Switchable remapping of 640K - 1 M RAM to Top of the Address Space.
- Advanced CMOS Technology.
- 100 pin Flatpack.

## DESCRIPTION

The SL9350 Memory Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9350 is part of the Personalized AT Logic chips that implements the Page Mode Memory Control functions which is specific to the 80386DX based PC/AT design and supports up to 25 MHz performance. Other members of the Personalized AT Logic chips include Page Interleave Memory Controller SL9151 and Page Mode Memory Controller SL9250 that are specific to 80286 and 80386SX-based PC/AT designs respectively.
It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

## PINOUT


NRAS2 80
VSS 79
VDD 78
MA81 77
CLK8042 76
A20GATE 75
NSHADOW 74
TEST3 73
NCSROM 72
NPAG4K 71
NLDEC 70
NMASTER 69
LA23 68
LA22 67
LA21 66
VSS 65
LA20 64
LA19 63
LA18 62
LA17 61
TEST4 60
ADVALE 59
ADD20 58
NRAS 57
RESET 56
NREFRESH 55
VSS 54
VDD 53
SA19 52
SA18 51
NRAS3 81
WSEL1 82
WSEL2 83
NCAS 84
MA0 85
MA1 86
MA2 87
MA3 88
MA4 89
VSS 90
MA5 91
MA6 92
MA7 93
MA8 94
MA9 95
MSEL1 96
MSEL2 97
MSEL3 98
MSEL4 99
NRAS0 100
50 SA17
49 NRDY
48 NMEMW
47 NMEMR
46 HLDA
45 NBMW
44 NBMR
43 NMEMDIR
42 NS1
41 NS0
40 VSS
39 CPUCLK
38 NROMOE
37 NMEGCS
36 A2
35 A3
34 A4
33 A5
32 A6
31 A7
SL9350
1 NRAS1
2 CLK2
3 VDD
4 VSS
5 MIO
6 DC
7 NADS
8 WR
9 NBUS16
10 NNA
11 A31
12 A23
13 A22
14 A21
15 VSS
16 A20
17 A19
18 A18
19 A17
20 A16
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
27 A9
28 VDD
29 VSS
30 A8

## ROM /RAM DECODE

The device provides all necessary circuitry to decode on board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column DRAMs.

The system can be configured for 512K Bytes to 16M Bytes. The bank selection code & sizes are as follows:

| Msel4 | Msel3 | Msel2 | Msel1 | RAS0/CAS0 | RAS1/CAS1 | RAS2/CAS2 | RAS3/CAS3 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0-640/1M-1M+384K | | | | |
| 0 | 0 | 0 | 1 | 0-640/2M-2M+384K | 1M-2M | | | |
| 0 | 0 | 1 | 0 | 0-640/3M-3M+384K | 1M-2M | 2M-3M | | |
| 0 | 0 | 1 | 1 | 0-640/4M-4M+384K | 1M-2M | 2M-3M | 3M-4M | |
| 0 | 1 | 0 | 0 | 0-640/1M-1M+384K | | | | 256K DRAMs |
| 0 | 1 | 0 | 1 | 0-640/2M-2M+384K | 1M-2M | | | 1M DRAMs |
| 0 | 1 | 1 | 0 | 0-640/6M-6M+384K | 1M-2M | 2M-6M | | |
| 0 | 1 | 1 | 1 | 0-640/10M-10M+384K | 1M-2M | 2M-6M | 6M-10M | |
| 1 | 1 | 0 | 0 | 0-640/1M-4M/4M-4M+384K | | | | |
| 1 | 1 | 0 | 1 | 0-640/1M-4M/8M-8M+384K | 4M-8M | | | |
| 1 | 1 | 1 | 0 | 0-640/1M-4M/12M-12M+384K | 4M-8M | 8M-12M | | |
| 1 | 1 | 1 | 1 | 0-640/1M-4M | 4M-8M | 8M-12M | 12M-16M | |

**Table 1**

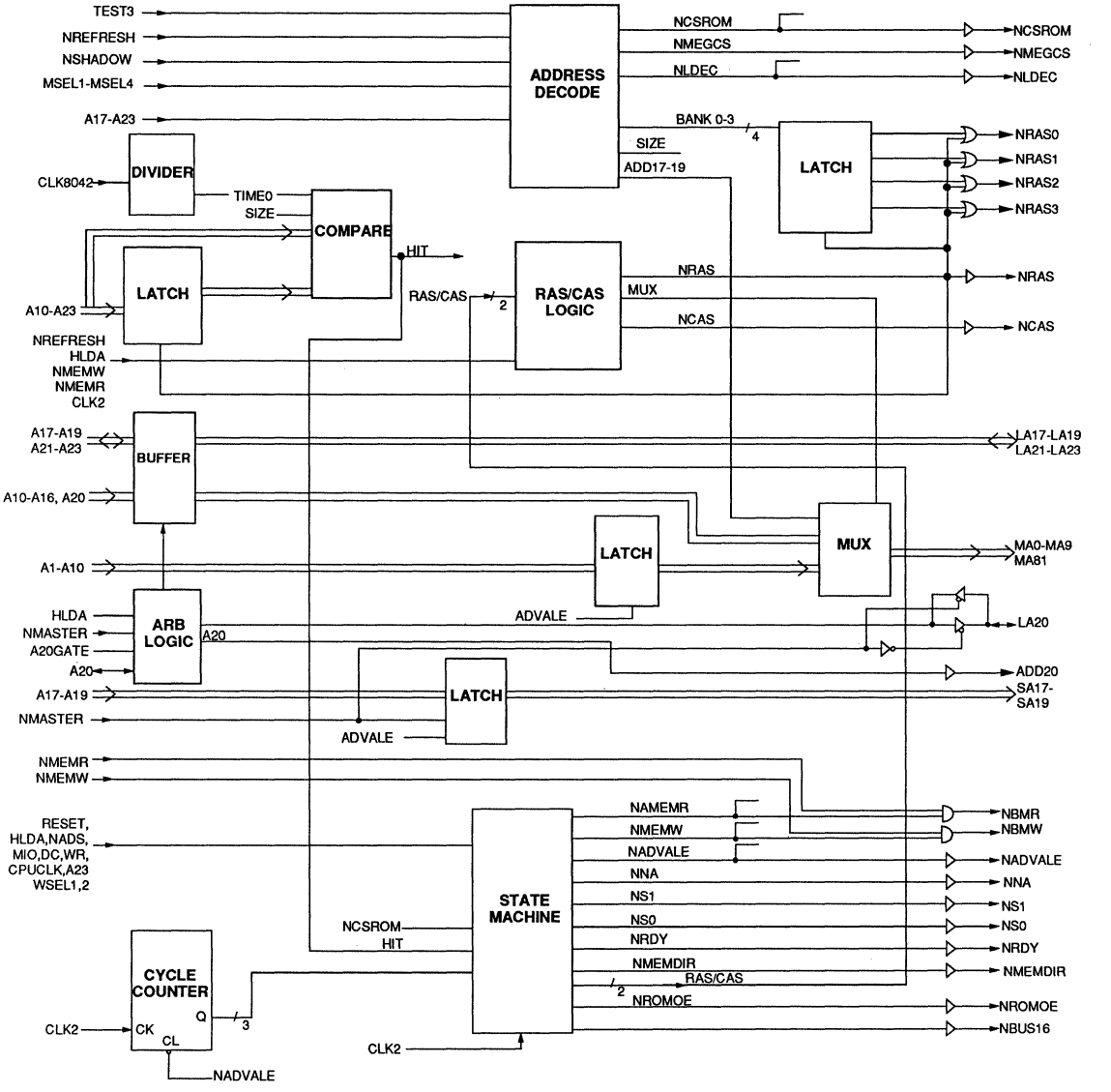
When Test3 input is tied low, the 384K Re-map to the top of the memory space is disabled.

Page is sized to 2KB if any 256K DRAMs are used and to 4KB if only 1M DRAMs are used, by tying NPAG4K High (256K) or Low (1Meg).

When CPU accesses the memory for the first time, the controller runs a one wait state memory cycle and asserts RAS & CAS low at appropriate times (Table 1). RAS is left low, CAS is returned high at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with previous value stored in the register. If a match (hit) is detected, then the RAS is held low and CAS is strobed immediately after ADVALE goes low for read cycles, and for write cycles, CAS is asserted 1 CPUCLK later. If a mismatch (miss) is detected then RAS is pulled high for 3 CLK2 cycles before reasserting low, and new row address is stored in the row address register. The controller will now run a 1 or 2 wait state memory cycle depending on the switch setting WSEL1 and WSEL2 (Table 3).

CPU Addresses A11-A21, A31 are passed onto MA0-9 as unlatched row addresses whereas A2-A11 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. RAS, MUX, and CAS are separated by one CLK2 period as shown in the timing diagram. This latching of column addresses allows use of static column DRAMs as well.

## BLOCK DIAGRAM SL9350



ROM/ RAM CONTROL (Cont'd.)

The SL9350 Memory Controller provides all the circuitry needed to generate RAM/ROM controls. RAM controls for Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS), RAM Read Write (NBMW, NBMR), Ready from 32 bit on board RAM read write (NRDY), next CPU address (NNA), and non on-board memory cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

| MIO | DC | WR | ADDRESS | CYCLE TYPE |
|---|---|---|---|---|
| 1 | 0 | 0 | | MEM CODE READ |
| 1 | 0 | 1 | 2/0 | HALT/SHUTDOWN |
| 1 | 1 | 0 | | MEM DATA READ |
| 1 | 1 | 1 | | MEM DATA WRITE |
| 0 | 0 | 0 | | INTA |
| 0 | 0 | 1 | | NOT POSSIBLE |
| 0 | 1 | 0 | | I/O DATA READ |
| 0 | 1 | 1 | | I/O DATA WRITE |

**Table 2**

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 32 bit, on board, memory miss can be set using the following table.

| CPU SPEED | WSEL1 | WSEL2 | WAIT STATES READ | WAIT STATES WRITE | MEMORY SPEED (ns) |
|---|---|---|---|---|---|
| 16 | 0 | 0 | 2 | 2 | -10 |
| | 1 | 0 | 2 | 1 | -10* |
| | 1 | 1 | 1 | 1 | -8* |
| 20 | 0 | 0 | 2 | 2 | -8 |
| | 1 | 0 | 2 | 1 | -8* |
| | 1 | 1 | 1 | 1 | -6* |

* Page Mode CAS write time ≤ 1 CLK2 period.

**Table 3**

ROM controls NCSROM & NROMOE are asserted low at appropriate time when address 0E0000h-0FFFFFh (low) or FE0000h-FFFFFFh (high) is decoded during a memory cycle. The timing relationship is shown in the timing diagram. These will be disabled if Shadow RAM option is used. When Shadow RAM option is used by pulling NSHADOW pin low, the ROM code is copied in the corresponding RAM location by BIOS and the subsequent ROM code reads will be decoded as RAM reads and will be much faster. BIOS can be customized to activate this option at boot. The NSHADOW option affects the 128K region immediately below 1 Meg.

REFRESH SUPPORT

The SL9350 provides support for DRAM refresh. During refresh NRAS0-3 are asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by the SL9025 Address Controller is passed from A Bus to MA Bus.

## BLOCK DIAGRAM SL9350

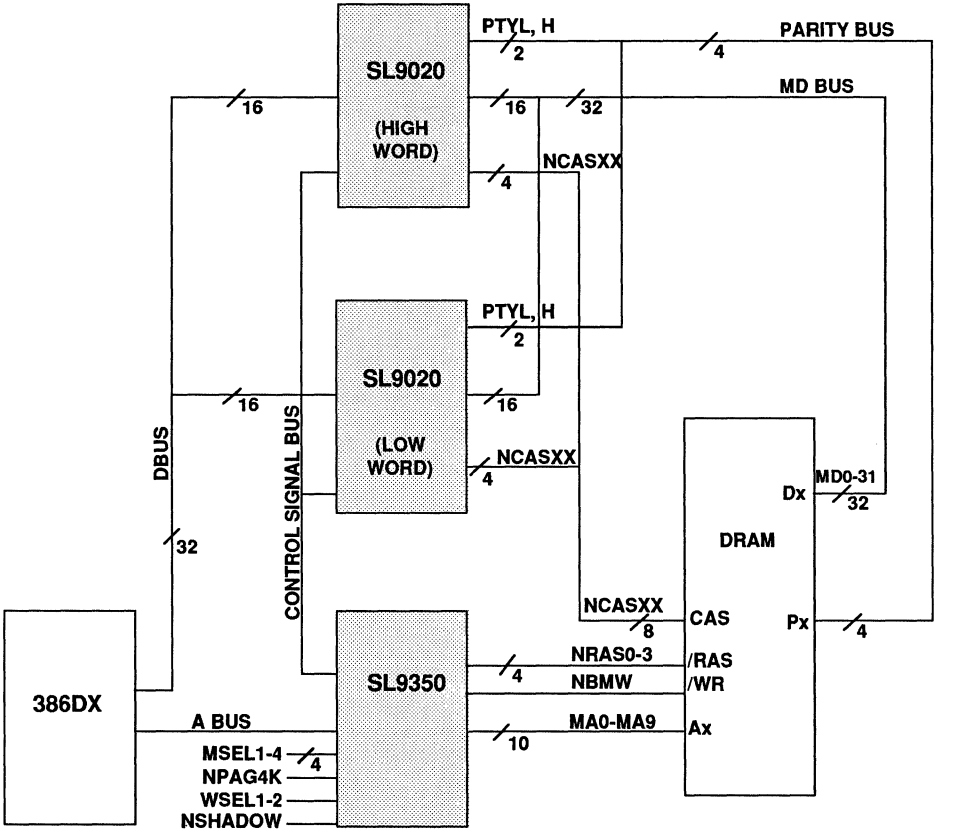



Fig. 1 386DX RAM BLOCK DIAGRAM

## RAM

System RAM is added as shown in Fig. 1. 32 Bit memory data is connected to the MD Bus. Memory data flow is from/to the MD Bus and to/from Dbus via two each SL9020 (high word and low word) Data Controllers. Parity data is generated and checked in the SL9020 through parity byte bits PTYL and PTYH. The SL9020's output memory CAS strobes are: NCASA02, NCASA13, NCASB02, NCASB13.

RAM address is passed or latched internally in the SL9350 as necessary from A Bus to memory MA Bus (10 Bit). The MA Bus features 12ma drive capability. The SL9350 provides 24ma direct drive lines for memory RAS (NRAS0-NRAS3) as well as memory Write (NBMW). Eleven signals are output by the SL9350 to facilitate system control during RAM transfers. Their function and destination are covered in Table 4.

| SIGNAL | DESTINATION | FUNCTION |
|---|---|---|
| ADVALE | SL9025 Address Controller | Used to latch the 386 address bus A1-A16 to the system address bus SA1-SA16. |
| | Internal | Used to latch the 386 address bus A17-A19 to the system address bus SA17-SA19. Transfers and latches 10 Bit CAS address (MA0-MA9) and NLDEC. Clears cycle counter. |
| NBMR | SL9025 Address Controller | Trailing edge used to latch parity error. |
| NBMW | SL9011 System Controller | Used to gate CPURST. |
| NCAS | SL9020 Data Controller | Used to gate SL9020 CAS output drivers: CASLA, CASLB, CASHA and CASHB. Trailing edge used to latch parity error. |
| NMEMDIR | SL9020 Data Controller | Sets MDBUS/DBUS direction. HI = D→MD |
| NLDEC | SL9011 System Controller | Indicates a local RAM/ROM decode. |
| MEGCS | SL9011 System Controller | Indicates a local RAM/ROM decode less than 1Meg address. |
| NRDY | SL9011 System Controller | Indicates the memory is ready with data. |
| NNA | 386 | Pipeline request to 386. |
| NS0-NS1 | SL9011 System Controller | 286 compatible status signal indicating a Read, Write, interrupt acknowledge or idle state. |

**Table 4. SL9350 Control Signal Function**

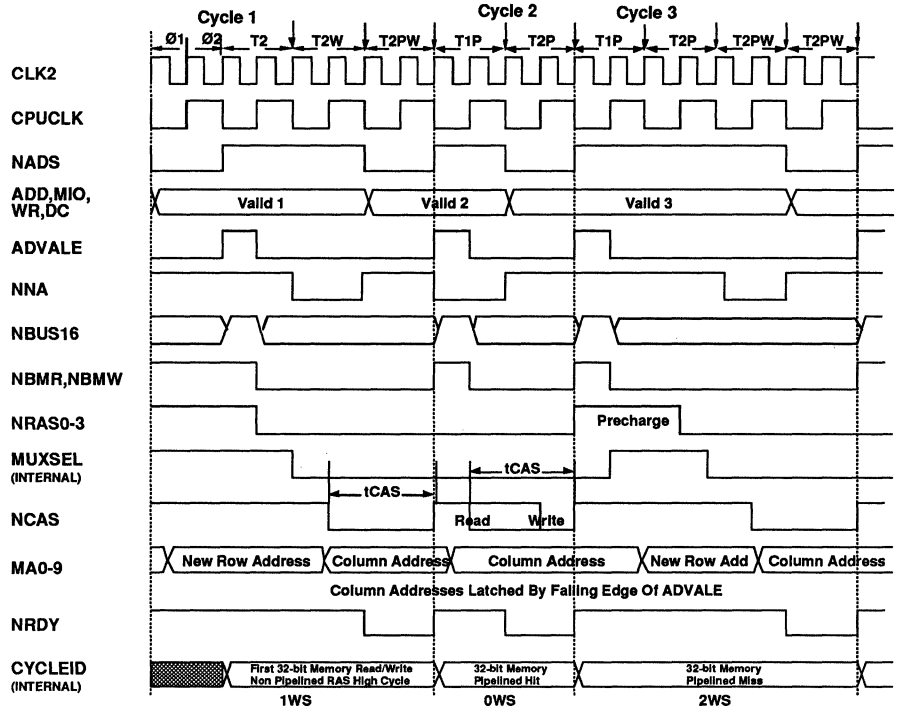



Fig. 2 32-Bit Memory (On Board) Timing Diagram

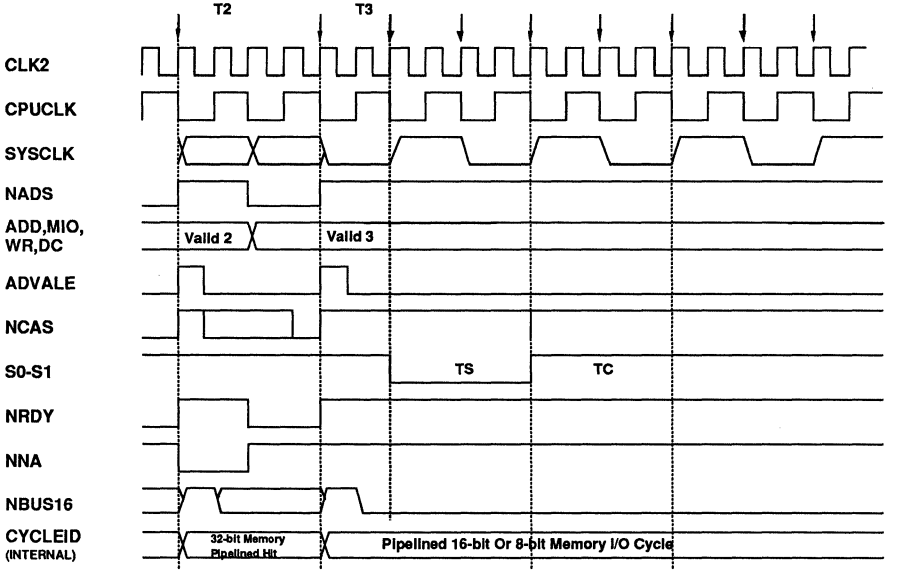



Fig. 3 Timing Diagram for Non 32-Bit Cycles

RAM (Cont'd)

A local memory cycle (cycle1 in Fig.2), begins during T1 when the 386 asserts NADS, MIO, and DC. SL9350 output NLDEC asserts, indicating a memory decode within the range specified by memory select jumpers Msel1-Msel4, as shown in Table 1. If the present address is within the lower 1 meg range, then MEGCS will also assert at this time. "ROW" addresses A11 through A20 are passed directly through the SL9350 into MA0-MA9. ADVALE is asserted during 01 (Phase 1, CPUCLK low) of T2. If the cycle is a Write, the start of T2 02 (Phase 2) brings NBMW valid, thus setting RAM WE. At this time, a RAS line will assert (NRAS0-NRAS3) strobing the MA0-MA9 address into the appropriate bank. ADVALE negates at 02, latching A1 through A10 in the SL9350. T2W 01 enables latched column address on MA0-MA9, and sets NNA to the 386 requesting the next cycle to be pipelined. T2W 02 asserts NCAS to the SL9020 Data Controllers, where the appropriate CAS line CASLA, LB, HA or HB is asserted, thus strobing the RAM column address and enabling RAM data output. NRDY to CPU (via SL9011) asserts at T2PW, signaling CPU to latch RAM data at end of T2PW 02. NADS also asserts, indicating a valid pipeline cycle in response to the previous NNA. T2WP 02 ends with CPUCLK dropping low, finishing the first cycle: NBMW, NCAS NRDY, and NADS negate, RAM data latches in the 386 CPU.

The next cycle, (cycle 2 in Fig. 3), T1P, asserts ADVALE, which enables a new column address on MA1-MA9. NNA is asserted, requesting the next cycle to be pipelined. AT T1P 02 advale negates, latching column addresses, asserts NBMR or NBMW as appropriate, and NCAS. NCAS assertion gives rise to the assertion of the appropriate RAM CAS line CASLA, LB, HA, or HB. T2P 01 negates NNA and asserts NRDY, signaling a page hit. The 386 asserts NADS indicating a new pipeline cycle. T2P 02 end latches RAM data in the 386 and negates NADS.

Cycle 3 begins in state T1P01 with NADS, NBMW, NRDY, NBUS, NNA NCAS and NRAS negated. ADVALE is asserted. Since NRAS is negated, a page miss is indicated. 02 negates ADVALE, asserts NBMW, and sets internal muxsel high. The mux is now driving a new row address on MA0-MA9. T2P 02 asserts the appropriate NRAS0-NRAS3 strobe, latching DRAM row address. T2P02 end drops internal muxsel, presenting as new column address on MA0-MA9. T2PW02 negates NCAS, thus strobing a new column address into DRAM and enabling DRAM output. The second wait state T2PW01 drops NRDY. Data for cycle 3 will then be latched in the CPU at the end of 02.

ROM

System ROM is enabled from 0E0000H to 0FFFFFH, or from FE0000H to FFFFFFH. 2 wait states are forced for any ROM access. If shadowing is selected, by asserting NSHADOW high on SL9350, then NROMOE and NCSROM signals are not asserted during the 386 Read cycle, and a RAM cycle is started instead.

System ROM is added as shown in Fig.4. 16 Bit ROM data out is connected to the MD Bus. 15 Bit ROM address input is connected directly to the 386 A Bus. Rom enable signals OE and CE are connected to the SL9350 output signals NROMOE and NCSROM. Data path is from MD Bus to 386D Bus via the SL9020 Data Controller. (Low word)

A Read cycle is started when the 386 asserts MIO, D/C and NADS. The "cycle" is latched internally on the rising edge of CLK2, when CPUCLK is high and a valid ROM address is on A17-A23 and A31. NCSROM is first asserted when a valid ROM address is decoded at T1A. When CPUCLK goes low and CLK2 rises high, (T2A), NBUS16 is asserted for the duration of CPUCLK low, indicating to the 386 a 16 bit cycle. Next CLK0, CPUCLK goes high and CLK2 rising high (T2B), NROMOE asserts, thus enabling ROM outputs. NMEMDIR asserts at this time, as well, signaling the SL9020 Data Controller to switch the memory data path from MDBus to DBus. After 2 wait states, on CLK2 rising high at T2W2B, NRDY asserts, signaling the SL9011 Controller that data is ready. The SL9011 drops NCPURDY, the CPU latches Bus data, and enters the second 16 Bit cycle by negating BE0, BE1, and NADS at T12 A. The second cycle repeats as the first. After the last ROM access, a valid ROM address will not be decoded and thus NCSROM, NRDMOE, and NMEMDIR will be negated in T1 A.

## BLOCK DIAGRAM SL9350

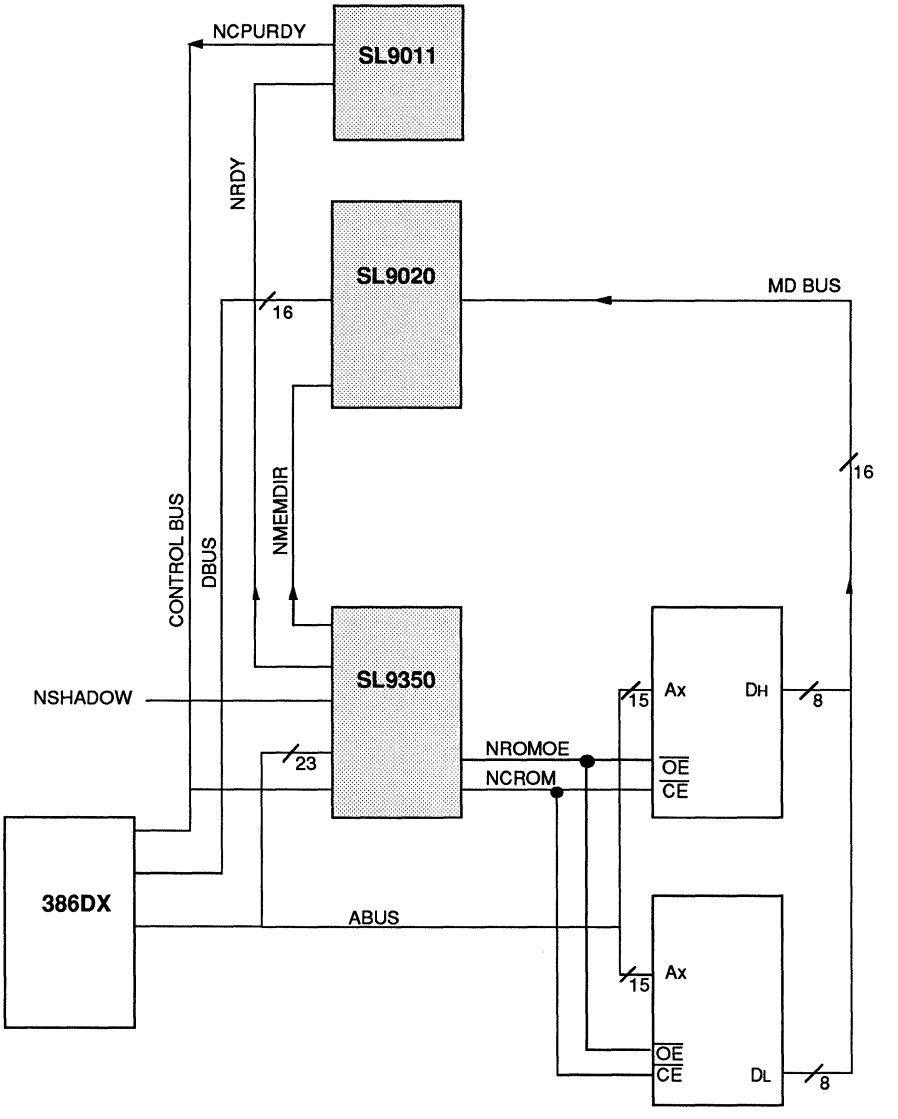



**Fig. 4 386DX ROM BLOCK DIAGRAM**

## AC TIMING DIAGRAMS SL9350

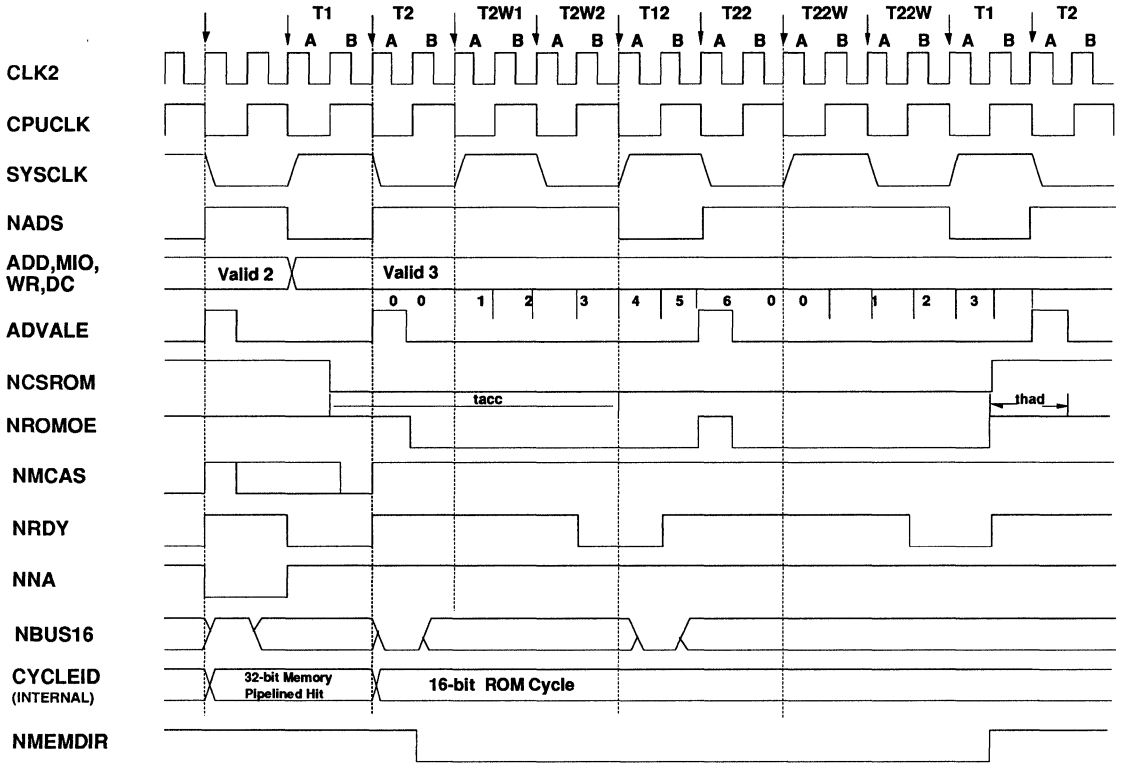



Fig. 5 Timing Diagram for BIOS ROM cycle (16-bit memory)

## PIN DESCRIPTION SL9350

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A2-A16 | 36,35,34,33, 32,31,30,27, 26,25,24,23, 22,21,20 | I | CPU Address Bus. |
| A17-A23 | 19,18,17,16, 14,13,12 | I/O | CPU Address Bus. |
| A31 | 11 | I/O | CPU Address Bus. |
| A20GATE | 75 | I | CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH. |
| ADD20 | 58 | O | Decoded 20-bit address bit used to generate address decode for 1 M RAMs. |
| ADVALE | 59 | O | Advanced Address Latch Enable from memory controller. It latches local bus address for the system bus. |
| CLK2 | 2 | I | Input Clock used to clock internal state machine. It is 2 times the frequency of the CPUCLK. |
| CLK8042 | 76 | I | 7 MHz clock input. It is used to internally generate a RAS time out. (Page mode.) |
| CPUCLK | 39 | I | Input Clock simulating 386 internal clock. It is CLK1 divided by two. |
| DC | 6 | I | CPU Status Signal. Differentiates between Data and Control instructions. |
| HLDA | 46 | I | CPU Output Signal, asserted to signal that the CPU has relinquished control of the bus to the device requesting MASTER or DMA. It is used to tri-state SLOT addresses during master. |
| LA17-LA23 | 61,62,63,64, 66,67,68 | I/O | Local address bus. Directly drives AT-SLOT signals LA17-LA23. |
| MA0-MA9 | 85,86,87,88, 89,91,92,93, 94,95 | O | RAM Address Bus Output. Directly drives DRAM address inputs. |
| MA81 | 77 | O | RAM Address pin for 1M RAMs. Used in place of MA8 for 1M DRAMs. |

## PIN DESCRIPTION SL9350 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| MIO | 5 | I | CPU output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is being used by the state machine to generate memory and I/O signals for the system. |
| MSEL1-4 | 96,97,98,99 | I | On-board Fast RAM memory size and type select. They are set as indicated in Table 1. The setting will determine the appropriate RAS and CAS outputs. Internally pulled down. |
| NADS | 7 | I | CPU output control signal, asserted when Address Bus outputs are valid. |
| NBMR | 44 | O | Buffered Memory Read signal. Used to latch addresses in the SL9025 Address Controller chip. |
| NBMW | 45 | O | Buffered Memory Write signal. Used to directly drive DRAM write input. |
| NBUS16 | 9 | O | CPU control input signal, Bus size 16. Activates 16-bit data bus operation; data is transferred on the lower 16 bits of the data bus and an extra cycle is provided for transfers of more than 16 bits. |
| NCSROM | 72 | O | LOW assert ROM Chip Select. Connects directly to system ROM CS. |
| NLDEC | 70 | O | Decode signal for on-board local HIGH-speed RAM. Indicates a local DRAM transfer is in process. |
| NMASTER | 69 | I | Asserted when an external device has control of the AT Bus at slot card output. Used to set address direction from SLOT to system. |
| NCAS | 84 | O | Memory column address strobe. Asserted when either CPU or DMA is accessing the memory. Used to drive SL9020 NCAS input. |
| NMEGCS | 37 | O | Select Decode for lower 1M of memory. Used to drive SL9011 NMEGCS input. |
| NMEMDIR | 43 | O | Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input. |
| NMEMR | 47 | I | Read Memory command from SL9011/SLOT. |

## PIN DESCRIPTION SL9350 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NMEMW | 48 | I | Write Memory command from SL9011/SLOT. |
| NNA | 10 | O | CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle. |
| NPAG4K | 71 | I | Active LOW Page size = 4K option; when 1M DRAMs are used. Left HIGH for 256Ks or mixes. |
| NRAS | 57 | O | LOW assert Row address strobe. Not used in normal operation. |
| NRAS0-3 | 100,1,80,81 | O | Row address strobes for Banks 0,1,2 & 3 for the on-board memory. Generated during CPU or DMA cycle for memory access. Used to directly drive DRAM RAS inputs. |
| NRDY | 49 | O | Asserted one clock cycle after NNA is asserted at the end of a local memory cycle. Used to signal SL9011 that data is ready. |
| NREFRESH | 55 | I | On-board RAM refresh signal. Generated from REFREQ input. |
| NROM0E | 38 | O | Enables ROM output during ROM read cycles. Connects directly to ROMOE pin. |
| NS0,1 | 41,42 | O | 80286 compatible status signals for the AT System Controller SL9011. |
| NSHADOW | 74 | I | Selectable option for Shadow RAMs. LOW enables Shadow RAM feature. |
| RESET | 56 | I | Active HIGH Reset from system controller. |
| SA17-19 | 50,51,52 | O | System Address Bus. |
| TEST3 | 73 | I | Optional disable for 684K - 1M [384K] remap. |
| TEST4 | 60 | I | Test Pin - Not connected. |
| VDD | 3,28,53,78 | - | +5V. Power. |
| VSS | 4,15,29,40, 54,65,79,90 | - | 0V. Ground. |
| WR | 8 | I | CPU output control signal Write. |
| WSEL1,2 | 82,83 | I | Wait-state Select options. Refer to Table 3 for proper setting. Internally pulled up. |

## AC TIMING DIAGRAMS SL9350

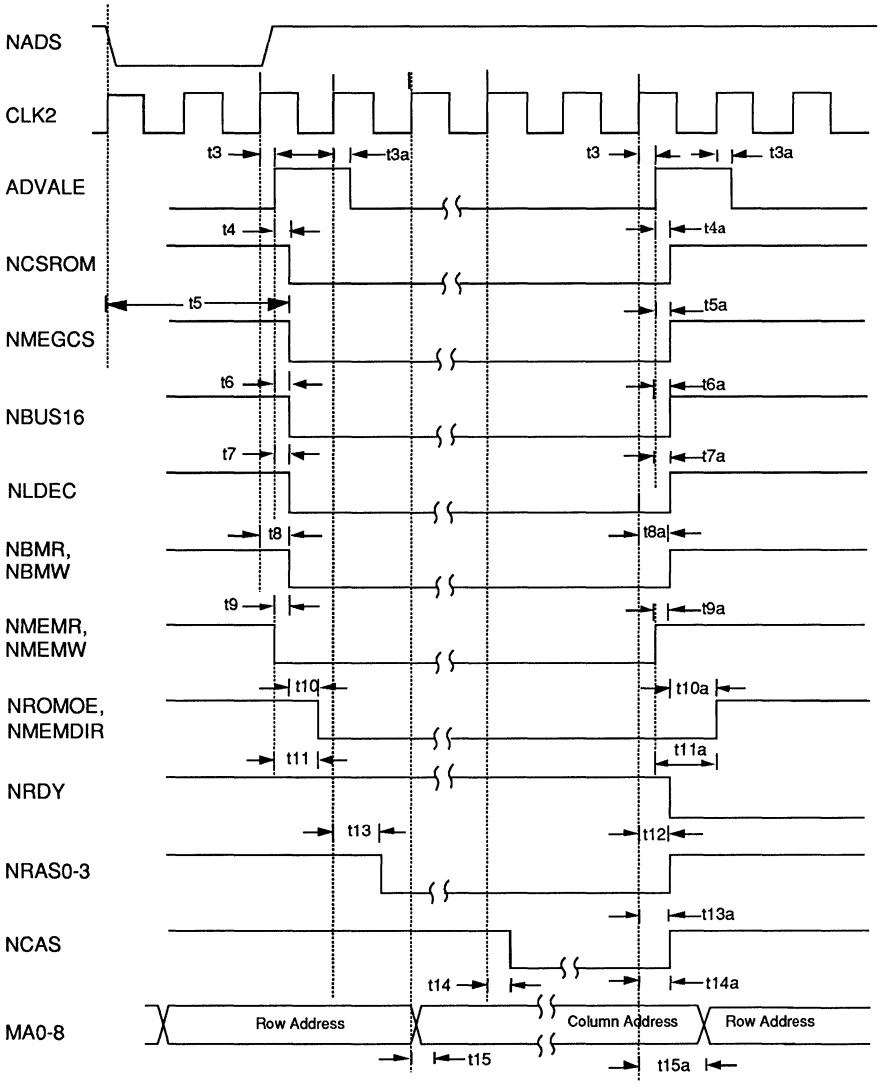



Fig. 6 Set-up and Hold Times

## ABSOLUT MAXIMUM RATINGS SL9350 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current *note 2 | $I_{OS}$ | -40 | +40 | mA |
| Output Current *note 3 | $I_{OS}$ | -40 | +80 | mA |
| Output Current *note 4 | $I_{OS}$ | -60 | +120 | mA |
| Output Current *note 5 | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NNA, NRDY, NROMOE, NS0, NS1.
3. A17 - A23, A31.
4. ADD20, MA0-MA9, MA81, LA17 - LA23, NRAS, SA17 - SA19.
5. NBMW, NRAS0 - NRAS3.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9350

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | TBD | TBD | mA | 20 MHz |
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state |
| Output High Voltage *note 1 | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output *note 2 | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output NBMW, NRAS0-NRAS3 | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output *note 3 | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output A17-A23, A31 | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output *note 4 | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output NBMW, NRAS0-NRAS3 | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for All Inputs | VIH | 2.2 | | V | |
| Input Low Voltage for All Inputs | VIL | | 0.8 | V | |
| Input Leakage Current *note 5 | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current, Tristate *note 6 | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = VSS |
| Input Current, Pull-up *note 7 | IILU | -33.5 | -204 | µA | VI = .4V |
| Input Current, Pull-up *note 8 | IIHU | -13.5 | -124 | µA | VI = 2.4V |
| Input Current, Pull-down MSEL1-MSEL4 | IILD | 4 | 26 | µA | VI = .4V |
| Input Current, Pull-down MSEL1-MSEL4 | IIHD | 14 | 106 | µA | VI = 2.4V |

NOTES:
1. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, A17-A23, A31
2. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
3. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1
4. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
5. A2-A16, A20 GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, NREFRESH, RESET, WR
6. A17-A23, A31, LA17-LA23, SA17-SA19
7. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2
8. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2

## AC CHARACTERISTICS SL9350

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| SYMBOL | DESCRIPTION | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| t1 | CLK2 Period | 25 | - | ns |
| t2 | CLK2 High Duration | 7 | - | ns |
| t2a | CLK2 Low Duration | 7 | - | ns |
| t3 | CLK2 to ADVALE (Low to High) | 5 | 20 | ns |
| t3a | CLK2 to ADVALE (High to Low) | 5 | 20 | ns |
| t4 | ADVALE to NCSROM (High to Low) | 5 | 15 | ns |
| t4a | ADVALE to NCSROM (Low to High) | 5 | 15 | ns |
| t5 | NADS to NMEGCS (High to Low) | 5 | 15 | ns |
| t5a | NADS to NMEGCS (Low to High) | 5 | 15 | ns |
| t6 | ADVALE to NBUS16 (High to Low) | 5 | 15 | ns |
| t6a | ADVALE to NBUS16(Low to High) | 5 | 15 | ns |
| t7 | ADVALE to NLDEC (High to Low) | 5 | 15 | ns |
| t7a | ADVALE to NLDEC (Low to High) | 5 | 15 | ns |
| t8 | CLK2 to NBMR, NBMW (High to Low) | 5 | 12 | ns |
| t8a | CLK2 to NBMR, NBMW (Low to High) | 5 | 12 | ns |
| t9 | NMEMR, NMEMW to NBMR, NBMW (High to Low) | 5 | 10 | ns |
| t9a | NMEMR,NMEMW to NBMR, NBMW (Low to High) | 5 | 10 | ns |
| t10 | NBMR to NROMOE (High to Low) | 0 | 12 | ns |
| t10a | NBMR to NROMOE (Low to High) | 0 | 12 | ns |
| t11 | NMEMR to NROMOE (High to Low) | 5 | 15 | ns |
| t11a | NMEMR to NROMOE (Low to High) | 5 | 15 | ns |
| t12 | CLK2 to NRDY | 5 | 12 | ns |
| t13 | CLK2 to NRAS0-NRAS3 (High to Low) | 5 | 12 | ns |
| t13a | CLK2 to NRAS0-NRAS3 (Low to High) | 5 | 12 | ns |
| t14 | CLK2 to NCAS (High to Low) | 5 | 12 | ns |
| t14a | CLK2 to NCAS (Low to High) | 5 | 12 | ns |
| t15 | CLK2 to MA0-MA8 Delay | 5 | 15 | ns |

(TA = 25 ° C, VDD = V1 = 5V, fo = 1MHz)

| PARAMETERS | SYMBOL | MIN. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | --- | 16 | Pf | note 1 |
| Input Pin Capacitance | CIN | --- | TBD | Pf | note 2 |
| Output Pin Capacitance | COUT | --- | 16 | Pf | note 3 |
| Output Pin Capacitance | COUT | --- | 18 | Pf | note 4 |
| I/O Pin Capacitance | CI/O | --- | 16 | Pf | note 5 |
| I/O Pin Capacitance | CI/O | --- | 23 | Pf | note 6 |

NOTES:
1. A2-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, REFRESH, RESET, WR
2. NSHADOW, MSEL1-MSEL4, NPAG4K, TEST 3, TEST 4, WSEL1, WSEL2
3. ADVALE, ADD20, MA0-MA9, MA81, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NNA, NRDY, NRAS, NROMOE, NS0, NS1
4. NBMW, NRAS0-NRAS3
5. A17-A23, A31, LA17-LA23, SA17-SA19
6. NBMW, NRAS0-NRAS3

FEATURES

- Supports 80386DX based AT Designs.
- Up to 33 MHz Performance with Cache Based Systems.
- Enhanced Fast Page Mode/Page Interleave.
- Supports 16 M bytes of on Board Memory.
- Shadow RAM Feature
  - 16K granularity
  - 8 remap options
  - System, video, LAN BIOS
- Programmable Memory Options
  - ROM chip select in 16K granularity
  - Wait states for 16 Bit ROM
  - Hit wait states (0-3)
  - Miss wait states (1-4)
  - RAS and CAS precharge
- Programmable Memory Partitioning
  - Disable (on board) memory to 0K in 128K resolution
  - 512 X 512 split
  - Memory backfill
- Can use 256K x 1, 1 M x 1 and 256K x 4 DRAMs or a mix.
- Staggered RAS Refresh.
- Supports Pipeline and Non-Pipeline Modes.
- Fast Gate A20 and Fast Reset.
- Backward Compatible to SL9350.
- Advanced, Low Power CMOS Technology for Laptops.
- 100 pin Flatpack.

## DESCRIPTION

The SL9351 Memory Controller supports PC/AT systems based on Intel's 80386DX microprocessor. It is a member of VIA's FlexSet family which utilizes the same core logic across the entire PC/AT spectrum. The SL9351 is backward compatible with existing memory controllers for the 80386DX (SL9350). Boards designed using the SL9350 can be used with the new SL9351 without modifications and with existing BIOS. In order to take advantage of the SL9351's many new programmable features, minor board modification and a modified BIOS is required for enhanced performance.

The SL9351 offers the advanced memory control functions and features needed to develop high performance PC/AT systems without using external TTL Logic. The SL9351 supports two-way page interleave mode for 80386DX based designs. The Page interleave option can be enabled or disabled using the configuration registers. All memory banks which are interleaved use the same type of memory. Designers can enable the staggered RAS option during refresh, which minimizes power surge. Both pipeline and non-pipeline modes are supported by enabling or disabling the next address controls, and providing ready at the correct time.

### RAM & ROM OPTIONS

The programmable RAM options supported by the SL9351, offer a very high level of design flexibility to the PC/AT system designer. DRAM page 'HIT' wait states are programmable from 0 to 3, and the DRAM page 'MISS' wait states are programmable from 1 to 4. This allows systems designers to design PC/AT systems capable of handling a wide range of DRAM speeds with wide variety of CPU speeds including 33 MHz Cache based systems. The 'MISS' wait states for write operation can be programmed to one less than the Read cycle. A minimum of one wait state is forced if a 'MISS' cycle is detected. The RAS precharge time is also programmable, typically a multiple of the CLK2 (2 to 5). Start of CAS can be independently programmed for HIT, read MISS and write MISS cycles. RAS to address is programmable in steps and 1/2 CLK2 increments.

In addition to the RAM, programming options for ROM are also supported. ROM chip select is programmable in 16K granularity. For ROM, 1 to 10 programmable wait states are supported.

### REMAP

In order to enhance the system and video performance, the SL9351 has been designed to support advanced shadow RAM features. The memory address space from '00A0000' to 00FFFFF' can be shadowed in 16K granularity, for system, video, LAN and other types of BIOS. This memory space is write protected in 16K granularity. The chip also supports Read/Write for local RAM using the 'backfill' option. By disabling the local RAM, the SL9351 allows system designers to Read and Write to the system bus. The local memory from 0 to 640K can be disabled with 128K granularity. The SL9351 offers many memory remap options which are listed in Table 1.

DESCRIPTION (cont'd.)

**Table 1. Remap Options**

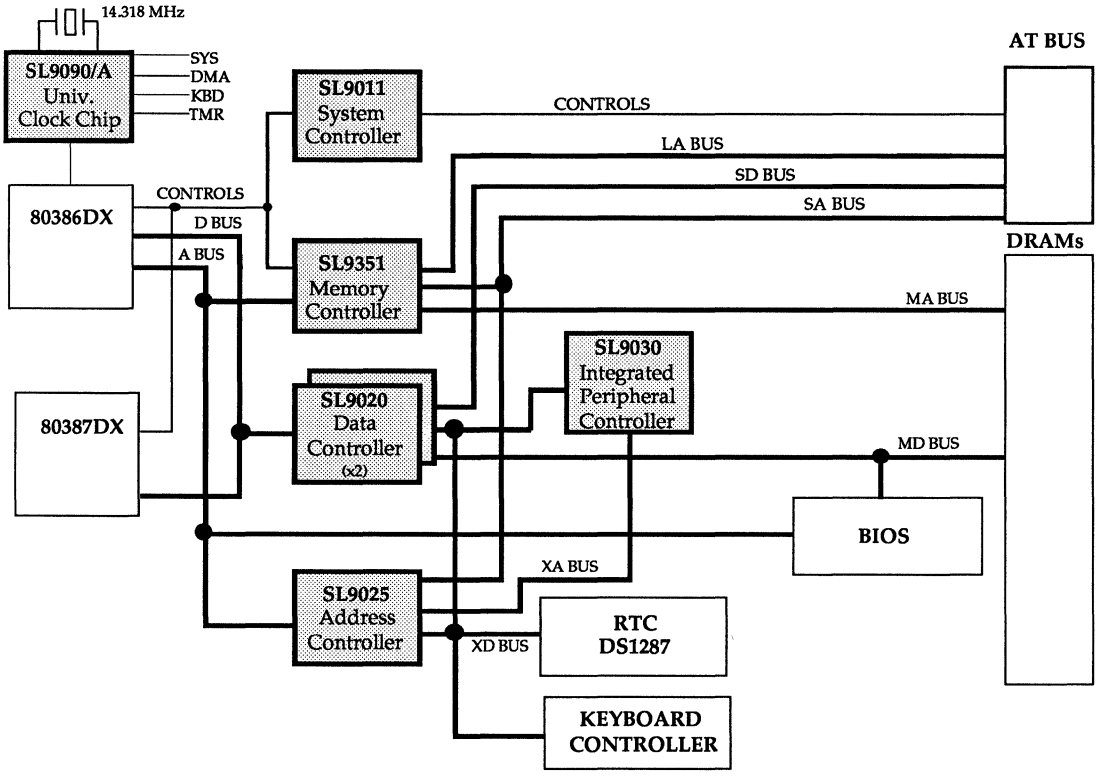
| |
|---|
| NO REMAP |
| 512K (512 X 512 SPLIT) |
| 128K (384K - 256K (SYSROM + ALL OPTION ROM) |
| 256K (384K - 128K LOCAL ROM) |
| 288K (384K - LOCAL SYS ROM + VIDEO ROM) |
| 320K (384K - 64K LOCAL ROM) |
| 352K (384K - 32K LOCAL ROM) |
| 384K REMAPPED FULLY. (NO SHADOW) |

ADDITIONAL FEATURES

OS/2 performance is enhanced significantly by using the Fast GATEA20 and Fast CPU Reset features offered by the SL9351. Port 92, defined in the IBM PS/2 technical manual, is used to provide faster performance.

Configuration registers are used to program these features during the system set up.

The SL9351 is available in a 100 pin plastic flat pack. It has been designed using advanced 1.2 micron double layer metal CMOS technology.




**FlexAT/386DX System Block Diagram**

# Universal

# Products

## FEATURES

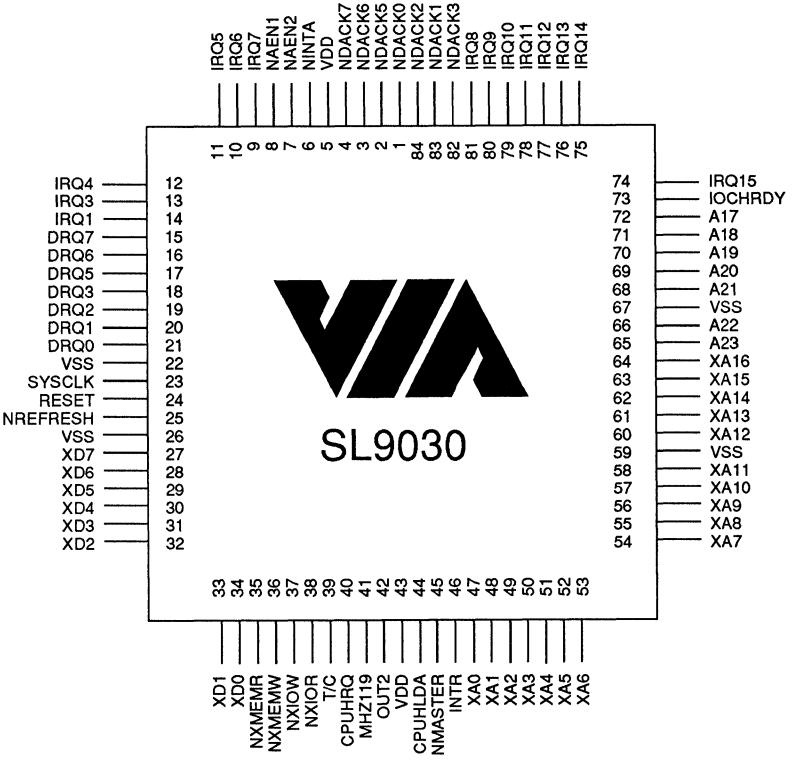
- **Pin to Pin Replacement for VLSI VL82C100.**
- **IBM PC/AT Compatible.**
- **Replaces 22 Logic Devices.**
- **Supports up to 20 MHz System Clock.**
- **Seven DMA Channels.**
- **14 External Interrupt Requests.**
- **Three Programmable Timer/Counter Channels.**
- **Compatible with all VIA FlexSet Chipsets.**
- **Designed in 1.2 micron CMOS Process.**
- **JEDEC - Standard 84-pin PLCC.**

## DESCRIPTION

The SL9030 Integrated Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS373 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and other less-complex TTL devices. The SL9030 provides 24 address bits for 16M bytes of DMA address space. It also interfaces directly to the CPU to handle all interrupts. Arbitration between refresh and DMA hold requests are performed by the SL9030.

The device is manufactured with an advanced high-performance 1.2 micron CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The SL9030 is part of the PC/AT-compatible FlexSet chip sets from VIA Technologies.

## PINOUT


IRQ5 11
IRQ6 10
IRQ7 9
NAEN1 8
NAEN2 7
NINTA 6
VDD 5
NDACK7 4
NDACK6 3
NDACK5 2
NDACK0 1
NDACK2 84
NDACK1 83
NDACK3 82
IRQ8 81
IRQ9 80
IRQ10 79
IRQ11 78
IRQ12 77
IRQ13 76
IRQ14 75
IRQ4 12
IRQ3 13
IRQ1 14
DRQ7 15
DRQ6 16
DRQ5 17
DRQ3 18
DRQ2 19
DRQ1 20
DRQ0 21
VSS 22
SYSCLK 23
RESET 24
NREFRESH 25
VSS 26
XD7 27
XD6 28
XD5 29
XD4 30
XD3 31
XD2 32
74 IRQ15
73 IOCHRDY
72 A17
71 A18
70 A19
69 A20
68 A21
67 VSS
66 A22
65 A23
64 XA16
63 XA15
62 XA14
61 XA13
60 XA12
59 VSS
58 XA11
57 XA10
56 XA9
55 XA8
54 XA7
SL9030
33 XD1
34 XD0
35 NXMEMR
36 NXMEMW
37 NXIOW
38 NXIOR
39 T/C
40 CPUHRQ
41 MHZ119
42 OUT2
43 VDD
44 CPUHLDA
45 NMASTER
46 INTR
47 XA0
48 XA1
49 XA2
50 XA3
51 XA4
52 XA5
53 XA6

## FUNCTIONAL DESCRIPTION

The SL9030 Integrated Peripheral Controller integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer and a 74LS612 equivalent along with support logic onto a single chip. The peripheral controller will replace all of the logic on the X bus of an AT-compatible design except the KeyboardController and Real Time Clock.

The SL9030 consists of five major subsections. The megacell chip select subsection decodes the signals MASTER, CPUHLDA, and the address bus XA0-XA9. This decoder is used to generate the chip select signals for each of the megacells within the SL9030.

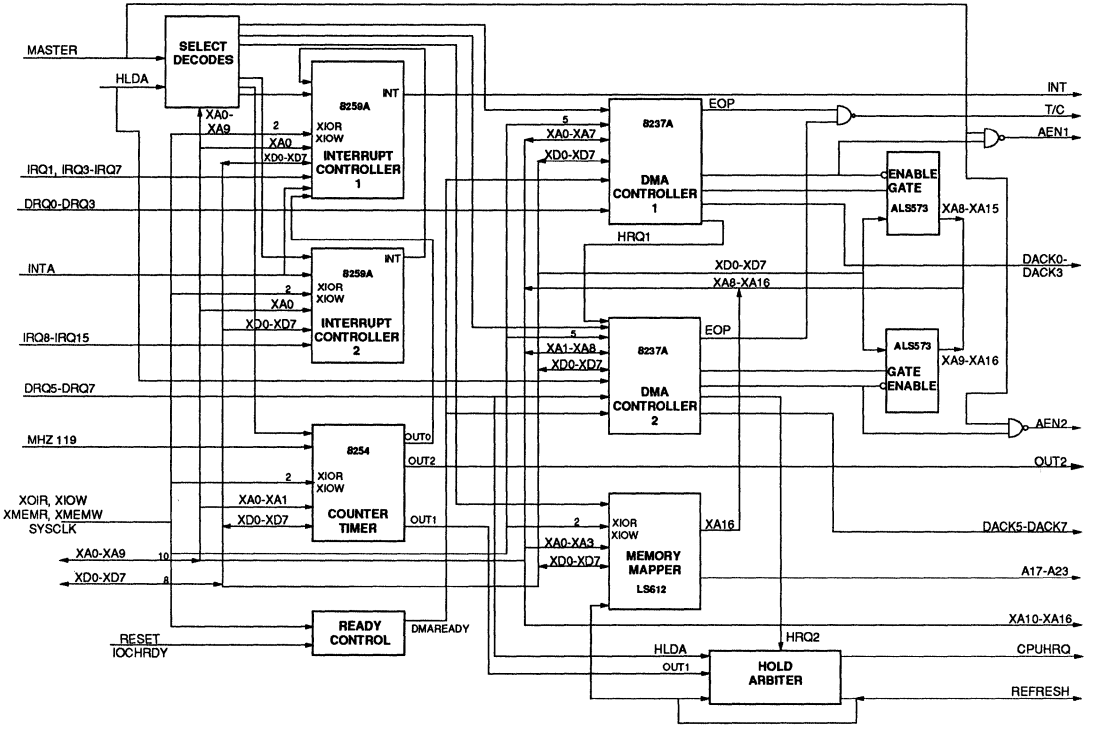
The DMA subsection consists of two 8237 megacells, two 8 bit latches to hold the middle range address bits during a DMA cycle and a 74LS612 equivalent megacell to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to force all DMA cycles to have one wait state inserted and additional logic to delay the leading edge of the XMEMR signal for one DMA clock cycle. These functions are used to maintain AT-compatibility. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8 bit I/O adapters and the other three are used for 16 bit I/O adapters. All channels are capable of addressing all memory locations in a 16 megabyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to accept 14 possible interrupt sources.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters are clocked at a 1.19 MHz rate. Gate inputs to counter 0 and 1 are always enabled (tied high). Gate 2 is connected to the Q output of a flip-flop. The D input of this flip-flop is bit 0 of the X Data and is clocked by port B write decode. The output of Counter 0 is routed to the interrupt controller subsection to be used as interrupt request 0. The output from Counter 1 is routed to the hold request arbiter to initiate refresh cycles. Counter 2's output is available as an external pin.

The hold request arbiter and refresh subsection is used to arbitrate between a possible hold request from the DMA subsection or Counter 1 of the counter/timer subsection. This block of logic also controls the REFRESH output signal.

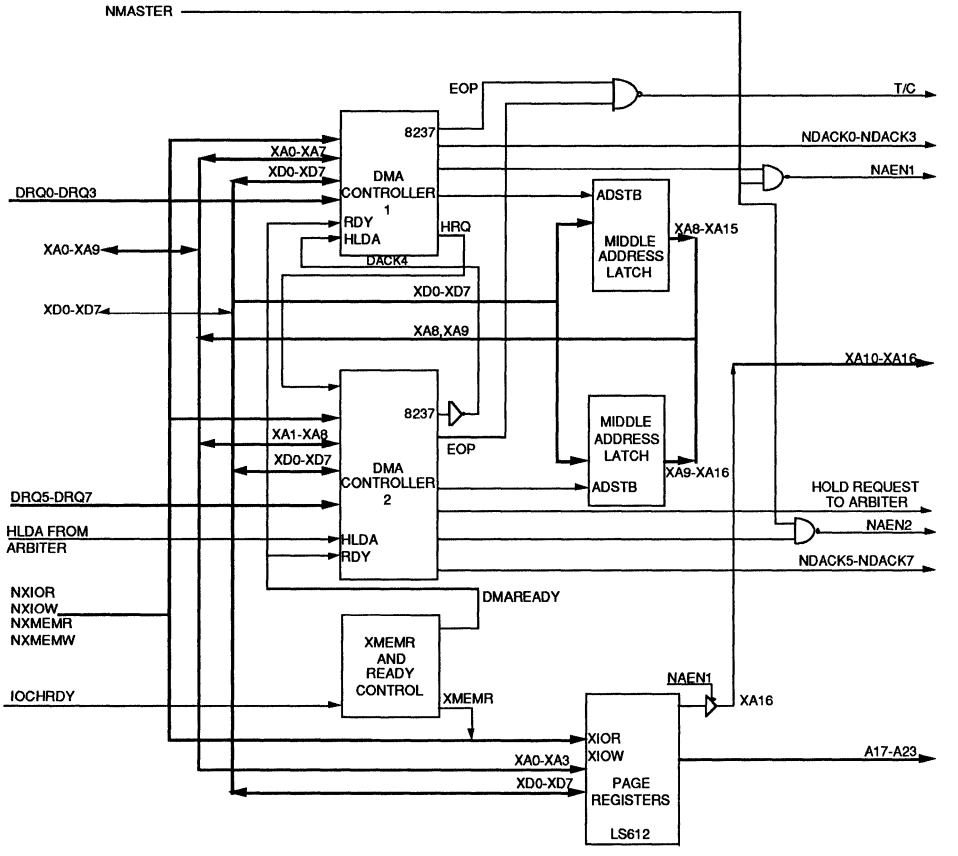
## BLOCK DIAGRAM SL9030



## DMA SUBSECTION

The DMA subsection controls DMA transfers between an I/O channel and on-board or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller will drive all 24 address bits for a total addressing capability of 16 megabytes, and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237 compatible, internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus and the function of a 74LS612 memory mapper is provided to generate the upper address bits.

**Fig. 1 DMA Subsection**



## DMA CONTROLLERS

The SL9030 supports seven DMA channels using two 8237 equivalent megacells capable of running at a 5 MHz DMA clock (10 MHz SYSCLK) rate. DMA Controller 1 contains channels 0 through 3. These channels support 8 bit I/O adapters. Channels 0 through 3 are used to transfer data between 8 bit peripherals and 8 or 16 bit memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data up to a maximum of 64 kilobytes per page.

DMA Controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16 bit I/O adapters to transfer data between 16 bit I/O adapters and 16 bit system memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data up to a maximum of 128 kilobytes per page. Channels 5, 6, and 7 are meant to transfer 16 bit words only and cannot address single bytes in system memory.

The 8237 can assume seven separate states, each composed of one full clock period. State 1 (S1) is the idle state. It is entered when the 8237 has no valid DMA requests pending, at the end of a DMA transfer sequence or when a reset or master clear has occurred.

State 0 (S0) is the first state of a DMA service. The 8237 has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the processor will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. Wait States (SW) are inserted when more time is needed to complete a transfer.

The system clock to the SL9030 may be stopped when the DMA controllers are in the S1 state and the Refresh signal from the SL9030 is not used.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored.

## MEGACELL CHIP SELECTS

Address bits XA0-XA9 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

For all the address decodes shown, the chip selects are disabled if both CPUHLDA and MASTER are high. The address decode at address 061 hex goes to a single flip-flop used to clock in the value of TMGAT2 in an AT-compatible design. This flip-flop will clock in the value of XD0 on the rising edge of XIOW whenever that address decode is valid. The output of the flip-flop is used to gate counter 2 in the 8254 megacell. This is the only bit of Port B that is decoded by the SL9030 and it cannot be read externally. The entire Port B is decoded in the SL9025 of the FlexSet. Bit 0 is duplicated in the SL9030 only to save an input pin.

**Table 1. Address Decode for Megacell Selects**

| XA9 | XA8 | XA7 | XA6 | XA5 | XA4 | XA3 | XA2 | XA1 | XA0 | Address Range | Megacell Selected |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | 000-01F | DMA Controller 1 (8237) |
| 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | 020-03F | Int. Controller 1 (8259) |
| 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | 040-05F | Counter/Timer (8254) |
| 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 1 | 061 | Port B (TMGAT2) |
| 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | 080-09F | DMA Page Reg. |
| 0 | 0 | 1 | 0 | 1 | X | X | X | X | X | 0A0-0BF | (74LS612) |
| 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | 0C0-0DF | Int. Controller 2 (8259) |

## DMA CONTROLLER REGISTERS

The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA 2 are for the 16 bit DMA channels and DMA 1 corresponds to the 8 bit channels. When writing to a channel's address or word count register the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16 bit registers. The value on the Xdata bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the Clear Byte Pointer Flip-Flop command. After this command the first read/write to an address or word count register will read/write to the low byte of the 16 bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count register will read/write to the high byte of the 16 bit register and the byte pointer flip-flop will toggle back to a zero.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DRQ and DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DRQ signals active high and the DACK signals active low.

When programming the 16 bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16 bit channels is the number of 16 bit words to be transferred, not the number of bytes as is the case for the 8 bit channels. It is recommended that all internal locations, especially the mode register, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

## MIDDLE ADDRESS BIT LATCHES

The middle address bits of the 24 bit address range are held in two sets of 8 bit registers, one register for each DMA controller. The DMA controller will drive the value to be loaded onto the data bus and then issue an address strobe signal to latch the data bus value into these register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8 bit address increments across the 8 bit subpage boundary during block transfers. These registers cannot be written to or read externally. They are loaded only from the address strobe signals from the megacells and the outputs go only to the XA8-XA16 pins.

## Table 2. DMA Controller Registers Addresses

| Hex Address | | Register Function |
|---|---|---|
| DMA2 | DMA1 | |
| 0C0 | 000 | Channel 0 Base and Current Address Register |
| 0C2 | 001 | Channel 0 Base and Current Word Count Register |
| 0C4 | 002 | Channel 1 Base and Current Address Register |
| 0C6 | 003 | Channel 1 Base and Current Word Count Register |
| 0C8 | 004 | Channel 2 Base and Current Address Register |
| 0CA | 005 | Channel 2 Base and Current Word Count Register |
| 0CC | 006 | Channel 3 Base and Current Address Register |
| 0CE | 007 | Channel 3 Base and Current Word Count Register |
| 0D0 | 008 | Read Status Register/Write Command Register |
| 0D2 | 009 | Write Request Register |
| 0D4 | 00A | Write Single Mask Register Bit |
| 0D6 | 00B | Write Mode Register |
| 0D8 | 00C | Clear Byte Pointer Flip-Flop |
| 0DA | 00D | Read Temporary Register/Write Master Clear |
| 0DC | 00E | Clear Mask Register |
| 0DE | 00F | Write All Mask Register Bits |

### PAGE REGISTERS

The equivalent of a 74LS612 is used in the SL9030 to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8 bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16 bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 eight bit registers in the 74LS612 megacell. The page registers are in the I/O address space as shown.

| Page Register | Hex I/O Address |
|---|---|
| DMA channel 0 | 087 |
| DMA channel 1 | 083 |
| DMA channel 2 | 081 |
| DMA channel 3 | 082 |
| DMA channel 5 | 08B |
| DMA channel 6 | 089 |
| DMA channel 7 | 08A |
| Refresh | 08F |

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080 and 08F that are not shown, are not used by the DMA channels but can be read or written to by the CPU. Address 08F is used to drive a value onto the upper address bits A17-A23 of the CPU's address bus during a refresh cycle.

## Table 3. Address Source Generation

| Outputs from 74LS612 Page Registers | Outputs from Middle Address Latches | Address Outputs from 8237 | 8 Bit DMA Address Bits | 16 Bit DMA Address Bits |
|---|---|---|---|---|
| M7 | | | A23 | A23 |
| M6 | | | A22 | A22 |
| M5 | | | A21 | A21 |
| M4 | | | A20 | A20 |
| M3 | | | A19 | A19 |
| M2 | | | A18 | A18 |
| M1 | | | A17 | A17 |
| M0 | | | XA16 | |
| | D7 | | XA15 | XA16 |
| | D6 | | XA14 | XA15 |
| | D5 | | XA13 | XA14 |
| | D4 | | XA12 | XA13 |
| | D3 | | XA11 | XA12 |
| | D2 | | XA10 | XA11 |
| | D1 | | XA9 | XA10 |
| | D0 | | XA8 | XA9 |
| | | A7 | XA7 | XA8 |
| | | A6 | XA6 | XA7 |
| | | A5 | XA5 | XA6 |
| | | A4 | XA4 | XA5 |
| | | A3 | XA3 | XA4 |
| | | A2 | XA2 | XA3 |
| | | A1 | XA1 | XA2 |
| | | A0 | XA0 | XA1 |
| | | LOW | | XA0 |

### ADDRESS GENERATION

The DMA addresses are setup such that there is an upper address portion, used to select a specific page, a middle address portion, used to select a block within the page, and a lower address portion.

The upper address portion is generated by the page register, in the 74LS612 equivalent megacell. The page registers for each channel must be setup by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8 bit channels (channels 0 through 3) and 128 kilobytes for 16 bit channels (channels 5, 6, and 7). The DMA page register values are output on A17-A23 and XA16 for 8 bit channels, and A17-A23 for 16 bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block of boundary. Block sizes are 256 bytes for 8 bit channels (channels 0 through 3) and 512 bytes for 16 bit channels (channels 5, 6, and 7). This middle address portion is output by the 8237 megacells onto the data bus during state S1. The internal middle address bit latches will latch in this value. The middle address bit latches are output on XA8-XA15 for 8 bit channels, and XA9-XA16 for 16 bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on XA0-XA7 for 8 bit channels, and XA1-XA8 for 16 bit channels. XA0 is forced low during 16 bit DMA operations.

Table 3 is shown to illustrate the source for all address bits during both 8 and 16 bit transfers.

## READY CONTROL

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. To maintain an AT-compatible design, the SL9030 ready control logic forces one wait state on every DMA transfer. The external signal IOCHRDY goes into the ready control logic to extend transfer cycles longer than one wait state if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock during the forced wait state. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time before the second phase of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4 (see timing diagrams).

## XMEMR DELAY

To maintain an AT-compatible design, the SL9030 inserts a DMA clock cycle delay in the falling edge of the XMEMR signal. XMEMR will go low one DMA clock (two SYSCLKs) later than the MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time as the MEMR signal from the megacell goes high.

## EXTERNAL CASCADING

An external DMA controller or bus master can be attached to an AT-compatible design through the DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channel's DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the seven channels is programmed in cascade mode and that channel is acknowledged the DMA controller will not drive the data bus, the command signals, or the XA address bus. However, the upper address bits A17-A23 will be driven with the value programmed into the page register for the channel programmed in cascade mode.

An external device can become a bus master and control the system address, data, and command buses in much the same manner. One of the DMA channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's DACK line goes active, the external device can then pull the MASTER signal low to force the system buses to a high impedance state. As in the DMA controller cascading, the SL9030 will not drive the X buses while the cascaded channels DACK signal is active. Also, the SL9030 will force the upper address bits A17-A23 to a high impedance state while MASTER is held low.

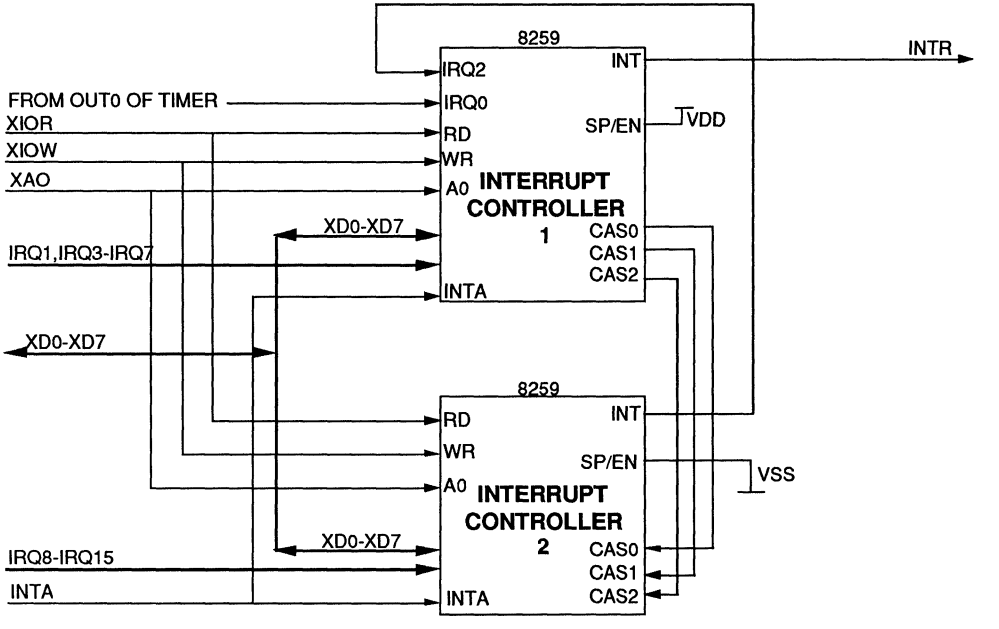
INTERRUPT CONTROLLER SUBSECTION

The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally through IRQ2 and IRQ0 is internally connected to a OUT0 of the 8254 counter/timer megacell. This allows a total of 14 external interrupt request.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the INTA pulses from the CPU. On the first INTA cycle the cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded in the SL9030, they should always be programmed to operate in the cascade mode.

**Fig. 2. Interrupt Controller Subsection**



INTERRUPT CONTROLLER INTERNAL REGISTERS

The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 4 shows the correct addressing for each of the 8259 registers. Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW0) can be written at any time after initialization.

In the standard 8259 megacell ICW3 is optional. But since the two 8259's in this chip are cascaded together, they should always be programmed in cascade mode and ICW3 will always be needed.

When reading at address 020 or 0A0 hex, the register read will depend on how Operation Control Word 3 was setup prior to the read.

## Table 4. Write Operations

| Hex Address | | XD4 | XD3 | Register Function |
|---|---|---|---|---|
| INT1 | INT2 | | | |
| 020 | 0A0 | 1 | X | Write ICW1 |
| 021 | 0A1 | X | X | Write ICW2 |
| 021 | 0A1 | X | X | Write ICW3 |
| 021 | 0A1 | X | X | Write ICW4 (If needed) |
| 021 | 0A1 | X | X | Write OCW1 |
| 020 | 0A0 | 0 | 0 | Write OCW2 |
| 020 | 0A0 | 0 | 1 | Write OCW3 |

## Table 5. Read Operations

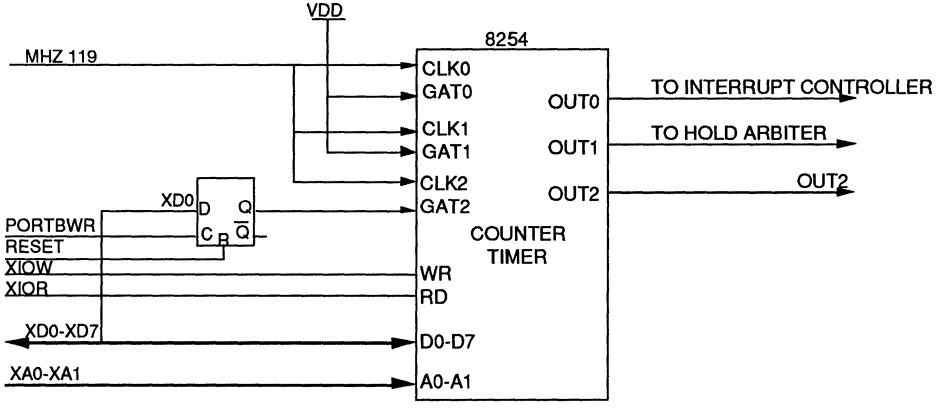
| Hex Address | | Register Function |
|---|---|---|
| INT1 | INT2 | |
| 020 | 0A0 | Interrupt Request Reg., In-Service Reg., or Poll Command |
| 021 | 0A1 | Interrupt Mask Register |

## TIMER/COUNTER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in the diagram. The clocks for each of the three internal counters are tied to the single input pin MHz 119. The gate inputs of Counters 0 and 1 are tied high to enable those Counters at all times. The gate input of Counter 2 is tied to the output of a flip-flop inside the SL9030. This flip-flop will clock in the value on XD0 during an I/O write to Port B. The output of the flip-flop is used to gate Counter 2 in the 8254 megacell on and off.

Only one of the 8254 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of interrupt controller 1. Counter 1's output goes to the hold request arbiter and refresh subsection to initiate a refresh cycle. Finally, Counter 2's output goes directly to the output pin OUT2.

**Fig. 3. Timer/Counter Subsection**




## TIMER/COUNTER INTERNAL REGISTERS

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 6 shows the correct addressing for each of the 8254 registers.

The write control word at address 043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

## Table 6. Timer/Counter Registers

| Hex Address | XIOR | XIOW | Register Function |
|---|---|---|---|
| 040 | 1 | 0 | Write Initial Count to Counter 0 |
| 040 | 0 | 1 | Read Latched Count or Status from Counter 0 |
| 041 | 1 | 0 | Write Intitial Count to Counter 1 |
| 041 | 0 | 1 | Read Latched Count or Status from Counter 1 |
| 042 | 1 | 0 | Write Intital Count to Counter 2 |
| 042 | 0 | 1 | Read Latched Count or Status from Counter 2 |
| 043 | 1 | 0 | Write Control Word |
| 043 | 0 | 1 | No Operation |

### HOLD REQUEST ARBITER AND REFRESH SUBSECTION

The hold request arbiter and refresh subsection is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 issues a hold request or when the output of counter 1 in the 8254 megacell makes a low to high transition. To provide equal weight to these two possible sources for a hold request, the hold request from the DMA controller is sampled on the rising edge of the internal DMA clock and the request from the counter/timer is sampled on the falling edge of the internal DMA clock. The request which is clocked in first will be granted by the arbiter and the other request inhibited until the first request is finished.

At the end of a hold request form either source the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the CPUHRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the CPUHRQ signal and return control back to the CPU.

In the case of the DMA controller's hold request winning in the arbiter, the arbiter will assert the CPUHRQ output and wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause a hold acknowledge to be sent to the DMA controller. When the DMA controller is finished it will negate its hold request signal to the arbiter. The arbiter will then switch to a REFRESH cycle, if a hold request is pending from the 8254 counter/timer, or negate the CPUHRQ line and return control to the CPU.

In the case of a refresh cycle winning the arbitration, the CPUHRQ output will be asserted and the arbiter subsection will wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause the SL9030 to pull the REFRESH pin low. REFRESH will remain low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK the REFRESH pin will go to a high impedance state enabling it to be pulled up by an external resistor, and the CPUHRQ signal will be negated. If the hold request arbiter has a hold request from the DMA controller pending on the fourth rising edge of SYSCLK cycle (see waveforms). The hold request arbiter will then acknowledge the hold request of the DMA controller.

Refresh cycles can be extended by an external source by forcing the IOCHRDY input low a setup time before the third rising edge of SYSCLK. REFRESH will remain low until IOCHRDY is returned high.

The pin REFRESH is a bidirectional open drain I/O pin and requires an external pull-up. It can also be used as an input if a refresh cycle is to be initiated from an external source.

## PIN DESCRIPTION SL9030

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A17-A21<br>A22, A23 | 72-68<br>66, 65 | O | CPU Address Bus Bits (A17 - 23) are connected to the CPU's address but and are driven from the LS612 memory mapper any time CPUHLDA is active (HIGH) and NMASTER is inactive (HIGH). They are in a three-state condition during all other times. |
| CPUHLDA | 44 | I | CPU Hold Acknowledge is an input from the CPU and indicates that it is acknowledging the hold request and is no longer driving the system bus. It indicated that the SL9030 can now drive the address and control buses. |
| CPUHRQ | 40 | O | CPU Hold Request output is the hold request to the CPU and is used to request control of the system bus. It can be issued by a request from the DMA controllers or the timer when it is time for a refresh cycle. |
| DRQO-DRQ3<br>DRQ5-DRQ7 | 21-18<br>17-15 | I | Input signals, DMA Request Bits 0-3, 5-7, are the individual asynchronous requests for DMA service connected to the 8237 megacell. DRQ0 through DRQ3 supports transfers form 8 bit I/O adapters to/from 8 or 16 bit system memory. DRQ5 through DRQ7 support transfers form 16 bit I/O adapters to/from 16 bit system memory. DRQ4 is not available as it is used to cascade the two DMA controllers together. |
| INTR | 46 | O | Interrupt Request is an output used to interrupt the CPU and is generated whenever a valid IRQ is received. |
| NINTA | 6 | I | Interrupt Acknowledge is an input used to enable the 8259 interrupt controllers to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU. |
| IOCHRDY | 73 | I | I/O Channel Ready is an input used to extend the memory read and write pulses from the 8237 to accommodate slow external devices. |
| IRQ1, IRQ3-IRQ7<br>IRQ8-IRQ15 | 14, 13-9,<br>81-74 | I | Interrupt Request bits 1, 3-7, 8-15 are asynchronous interrupt request inputs to the 8259 megacells. IRQ2 and IRQ0 are not available as inputs to the chip. IRQ2 is used to cascade the two 8259's together and IRQ0 is connected to the out0 signal of the 8254 counter. |
| MHZ119 | 41 | I | This is the 1.19 MHz clock input for the 8254 counter. |
| NAEN1 | 8 | O | Address Enable 1 is an active LOW signal. It indicates when DMA Controller 1 is enabling addresses onto the peripheral address bus for a DMA transfer. |

## PIN DESCRIPTION SL9030 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NAEN2 | 7 | O | Address Enable 2 is an active LOW signal. It indicates when DMA Controller 2 is enabling addresses onto the peripheral address bus for a DMA transfer. |
| NDACK0-NDACK3<br>NDACK5-NDACK7 | 1, 83, 84, 82<br>2-4 | O | DMA Acknowledge Bits 0-3, 5-7 output signals are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is programmable and is set to active LOW on reset. |
| NMASTER | 45 | I | Master - An external device will pull this input LOW to disable the DMA controllers to gain access to the system bus. It indicates an I/O device controls the system buses. |
| NREFRESH | 25 | I/O | The Refresh I/O signal will be pulled LOW by the SL9030 whenever the 8254 counter 1 issues a CPUHRQ to the CPU and a hold acknowledge is received from the CPU. It is used internally to select a location in the memory mapper which drives the upper address bus A17-A23. Refresh can also be used as an input if the refresh timing is to come from a source other than the 8254 channel 1 counter. Refresh is an open drain output capable of sinking 20 mA and requires an external pull-up resistor. |
| NXIOR | 38 | I/O | I/O Read is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times. |
| NXIOW | 37 | I/O | I/O Write is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times. |
| NXMEMR | 35 | O | Memory Read is a three-state output which will be active during a DMA cycle. |
| NXMEMW | 36 | I/O | Memory Write is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times. In the input mode XMEMW is used to enable the hold request arbiter after an interrupt acknowledge cycle. |
| OUT2 | 42 | O | Out 2 is the output of counter 2 in the 8254 megacell. |
| RESET | 24 | I | Reset is an active HIGH input used to clear the DMA controller and hold request arbiter. |

## PIN DESCRIPTION SL9030 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SYSCLK | 23 | I | System Clock Input. This pin is divided by two internally to generate DMACLK for the 8237 DMA controllers. It is also used in the hold request arbiter. SYSCLK can be driven at a frequency of up to 20 MHz. |
| T/C | 39 | O | Terminal Count indicates one of the DMA channel's terminal count has been reached. |
| VDD | 5, 43 | | System Power : 5 V. |
| VSS | 22, 26, 59, 67 | | System Ground. |
| XA0-XA9 | 47-56 | I/0 | Peripheral Address bus Bits 0-9 are bidirectional pins. They are outputs during DMA cycles and are inputs all other times. As inputs they are used to generate chip selects for the 82XX megacells. |
| XA10, XA11<br>XA12-XA16 | 57, 58<br>60-64 | O | The seven most significant address bits on the XA bus (XA10-16) are three-state outputs only. They actively drive the XA bus during DMA cycles. |
| XD0-XD7 | 34-27 | I/O | Peripheral Data Bus Bits 0-7. The eight least significant data bits on the XD bus are bidirectional. |

## ABSOLUT MAXIMUM RATINGS SL9030 *note 1

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -.5 | 6.0 | V |
| Input Voltage | $V_I$ | -.5 | $V_{DD}$+.5 | V |
| Output Voltage | $V_O$ | -.5 | $V_{DD}$+.5 | V |
| Output Current | $I_{OS}$ | -40 | +40 | mA |
| Output Current | $I_{OS}$ | -40 | +80 | mA |
| Output Current | $I_{OS}$ | -60 | +120 | mA |
| Output Current | $I_{OS}$ | -90 | +180 | mA |
| Storage Temp. | $T_{STL}$ | -40 | +125 | °C |
| Storage Temp. | $T_{BIOS}$ | -25 | +85 | °C |

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Temperature | $T_A$ | 0 | 70 | °C |

## DC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Output High Voltage | VOH | 3.0 | | V | IOH = 4mA |
| Output Low Voltage | VOL1 | | 0.4 | V | IOL = 20 mA, NREFRESH |
| Output Low Voltage | VOL2 | | 0.4 | V | IOL = 4 mA, All Other Pins |
| Input High Voltage | VIH | 2.2 | VDD+.5 | V | TTL |
| Input Low Voltage | VIL | -0.5 | 0.8 | V | TTL |
| Output Capacitance | CO | | 10 | pF | |
| Input Capacitance | CI | | 10 | pF | |
| Input/Output Capacitance | CIO | | 10 | pF | |
| Three-state Leakage Current | IO2H | | 10 | mA | VOH = VDD |
| | IO2L | -10 | | mA | VOL = GND |
| Input Leakage Current | ILI | -10 | 10 | µA | All Inputs |
| Power Supply Current | ICC | | 30 | mA | Note |

NOTE:
VIN = VDD or GND, VDD = 5.25V, ouputs unloaded

ABSOLUTE MAXIMUM RATINGS:

| | |
|---|---|
| Ambient Operating Temperature | QC = 0°C to +70C<br>QI = -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Supply Voltage to Ground Potential | -0.5V to +7.0V |
| Applied Input Voltage | -0.5V to VDD to .5V |
| Power Dissipation | 500 mW |

## AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

| Symbol | Description | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| tSET3 | DRQ to SYSCLK High Setup Time | 0 | - | ns | 1 |
| tD10 | CPUHRQ Valid from SYSCLK High Delay Time | - | 60 | ns | |
| tSET4 | CPUHLDA to SYSCLK High Setup Time | 25 | - | ns | |
| tD11 | NAEN1 Valid from SYSCLK High Delay Time | - | 75 | ns | |
| tD12 | NDACK Valid from SYSCLK High Delay Time | - | 90 | ns | |
| tD13 | XD Bus Valid from SYSCLK High Delay Time | - | 100 | ns | |
| tD14 | XD Bus Active to Float Delay from SYSCLK High | - | 55 | ns | |
| tD15 | A17-A23 Float to Active from CPUHLDA High Delay Time | - | 35 | ns | |
| tD16 | Upper Address Bits Valid from SYSCLK High Delay Time | - | 110 | ns | 2 |
| tD17 | A17-A23 Active to Float from CPUHLDA Low Delay Time | - | 25 | ns | |
| tD18 | Middle Address Bits Valid from SYSCLK High Delay Time | - | 110 | ns | 3 |
| tD19 | Lower Address Bits Valid from SYSCLK High Delay Time | - | 85 | ns | 4 |
| tD20 | XA Address Bus Active to Float from SYSCLK High Delay Time | - | 60 | ns | 7 |
| tD21 | NREAD and NWRITE Active from SYSCLK High Delay Time | - | 75 | ns | |
| tD22 | NREAD and NWRITE Valid from SYSCLK High Delay Time | - | 80 | ns | |
| tD23 | NREAD and NWRITE Float from SYSCLK High Delay Time | - | 60 | ns | 7 |
| tD24 | T/C Valid from SYSCLK High Delay Time | - | 85 | ns | 7 |
| tHD2 | XA Address From NREAD or NWRITE | 2 TCY -50 | - | ns | TCY=SYSCLK cycle time |
| tD25 | NAEN2 Valid from SYSCLK High Delay Time | - | 75 | ns | |
| tD26 | NAEN2 High from SYSCLK High | - | 125 | ns | |
| tD27 | XA Address Bus Float from SYSCLK High Delay Time | - | 120 | ns | 8 |
| tD28 | NREAD or NWRITE Float from SYSCLK High Delay Time | - | 120 | ns | 8 |
| tD29 | NREAD or NWRITE Float from NREAD or NWRITE High at end of DMA Cycle | 5 | - | ns | 8 |
| tSET5 | IOCHRDY Valid to SYSCLK High Setup Time | 15 | - | ns | |
| tHD3 | IOCHRDY from SYSCLK High Hold Time | 5 | - | ns | |
| tD30 | A17-A23 Float from NMASTER Low Delay Time | - | 25 | ns | |
| tD31 | A17-A23 Float from NMASTER High Delay Time | - | 40 | ns | |
| tD32 | NREFRESH Low from CPUHLDA High Delay Time | - | 50 | ns | |
| tD33 | NREFRESH Inactive from SYSCLK High Delay Time | - | 50 | ns | 5 |
| tSET6 | NREFRESH Low to SYSCLK High Setup Time | 20 | - | ns | 6 |
| tD34 | A17-A23 Valid from NREFRESH Valid Delay Time | - | 80 | ns | |
| t35 | SYSCLK Cycle Time | 50 | - | ns | |
| tPW55 | SYSCLK Pulse Width Low | 20 | - | ns | |
| tPW56 | SYSCLK Pulse Width High | 20 | - | ns | |
| t36 | SYSCLK Rise/Fall Time | - | 7 | ns | |

NOTES:
1. The DRQ signals are asynchronous inputs. Setup times are shown to assure recognition at a specific clock edge for testing.
2. Upper address bits are defined as A17-A23 for 16 bit DMA cycles, and A17-A23 plus XA16 for 8 bit DMA cycles.
3. Middle address bits are defined as XA9-XA16 for 16 bit DMA cycles and XA8-XA15 for 8 bit DMA cycles.
4. Lower address bits are defined as XA0-XA8 for 16 bit DMA cycles and XA0-XA7 for 8 bit DMA cycles.
5. NREFRESH is an open drain output. This specification is the time until the output is in an inactive state. Rise time of the external signal will depend on the external pull-up value and capacitive load.
6. When used as an input, NREFRESH is an asynchronous signal.
7. 8 Bit Cycles Only.
8. 16 Bit Cycles Only.

## AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| tRW | NXIOR or NXIOW Pulse Width Low | 150 | - | ns |
| tSET1 | XA Address Valid to NXIOR or NXIOW Low Setup Time | 25 | - | ns |
| tHD1 | XA Address from NXIOR or NXIOW High Hold Time | 15 | - | ns |
| tD1 | XD Data Valid Delay from NXIOR Low | - | 100 | ns |
| tD2 | XD Data Float Delay from NXIOR High | - | 60 | ns |
| tSET2 | XD Data Valid to NXIOW High Setup Time | 100 | - | ns |
| tHD2 | XD Data Valid from NXIOW High Hold Time | 10 | - | ns |
| tRST | RESET Pulse Width High | 200 | - | ns |
| t1 | RESET Inactive to first NXIOR or NXIOW Command | 200 | - | ns |
| t2 | Comand Recovery Time Between Successive NXIOR or NXIOW Pulses | 200 | - | ns |

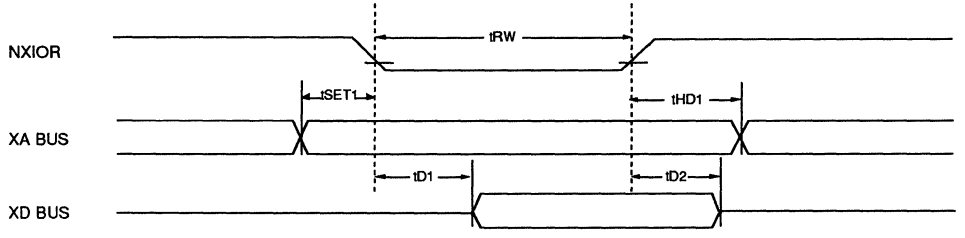



Fig. 4. READ TIMING

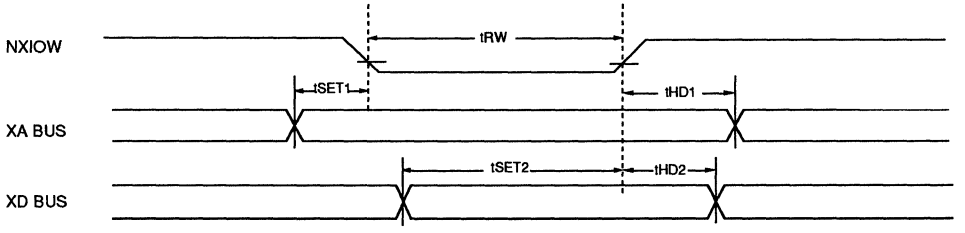



Fig. 5. WRITE TIMING

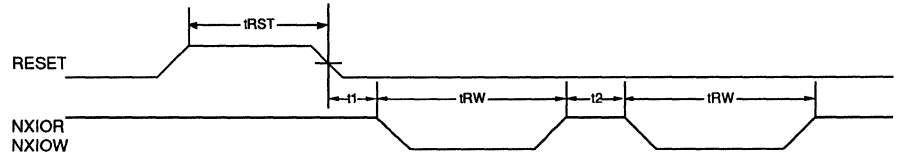



Fig. 6. COMMAND AND RESET TIMING

## AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

| Symbol | Description | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| tPW1 | Interrupt Request Pulse Width Low | 90 | - | ns | |
| tD3 | Interrupt Output Delay | 130 | - | ns | |
| tPW2 | NINTA Pulse Width Low | 180 | - | ns | |
| tD4 | End of NINTA Pulse to next NINTA Pulse | 180 | - | ns | |
| tD5 | XD Data Valid Delay from NINTA Low | - | 110 | ns | 1 |
| tD6 | XD Data Float Delay from NINTA High | 0 | 45 | ns | 2 |
| tPW3 | MHz 119 Clock Pulse Widht High | 50 | - | ns | |
| tPW4 | MHz 119 Clock Pulse Width Low | 50 | - | ns | |
| tD7 | MHz 119 Clock Rise/Fall Time | - | 20 | ns | |
| tD8 | OUT2 Valid from NXIOW High Delay Time when writing to Counter 2 Mode Register or TMGATE2 in Port B | - | 100 | ns | |
| tD9 | Out2 Valid from MHz 119 Low Delay Time | - | 100 | ns | |

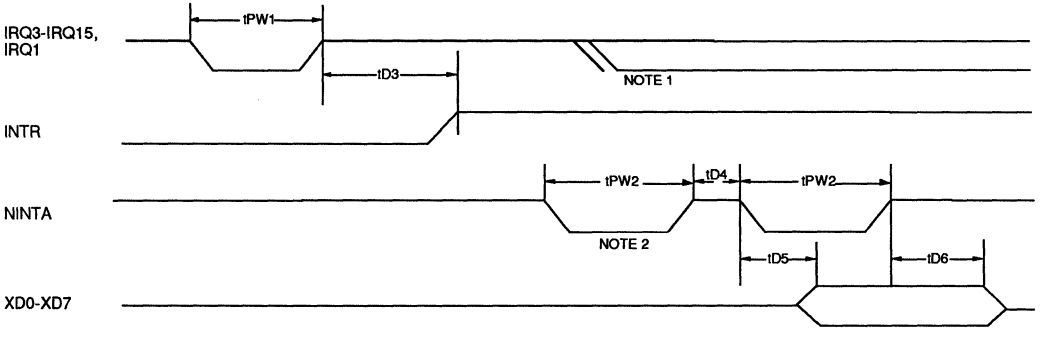



Fig. 7. INTERRUPT TIMING

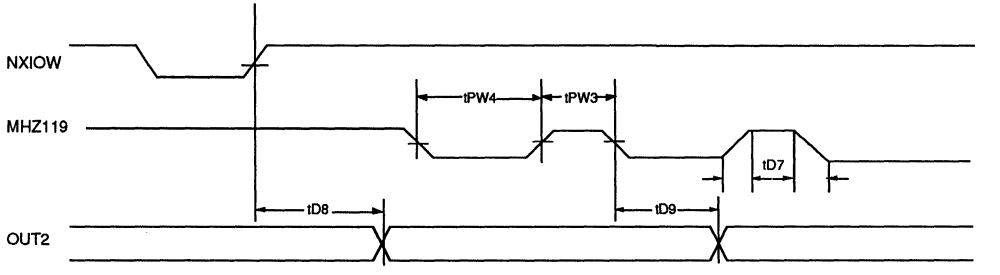



Fig. 8. TIMER/COUNTER TIMING

NOTES: 1. IRQ must remain HIGH until first NINTA pulse
2. Cascade priority is resolved on this NINTA cycle.

## AC TIMING DIAGRAMS SL9030

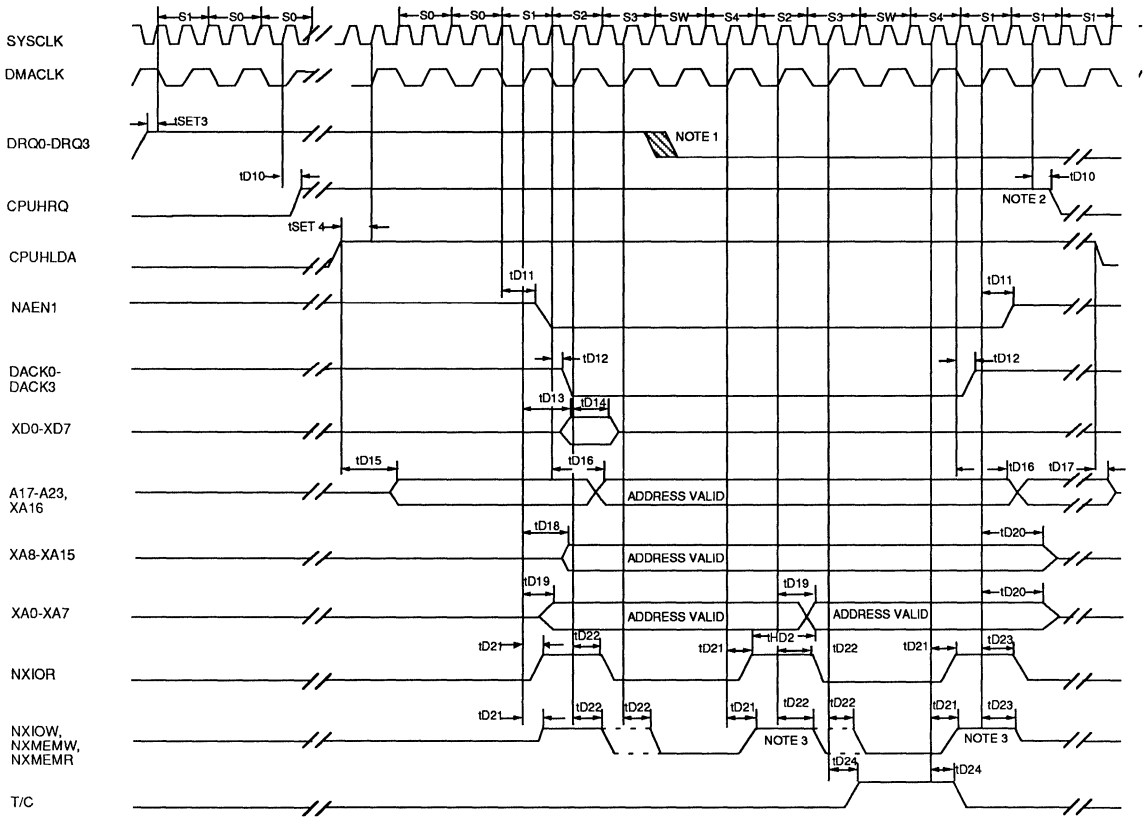



Figure 9. 8 BIT DMA TIMING

NOTES:
1. DRQ should be held active until NDACK is returned.
2. The falling edge of CPUHRQ could occur one clock cycle earlier or later depending on how many bytes are transferred.
3. The first high to low transition shown here is for extended NXIOW and NXMEMW. The second high to low transition shown is for NXMEMR and late write on NXIOW and NXMEMW.

## AC TIMING DIAGRAMS SL9030

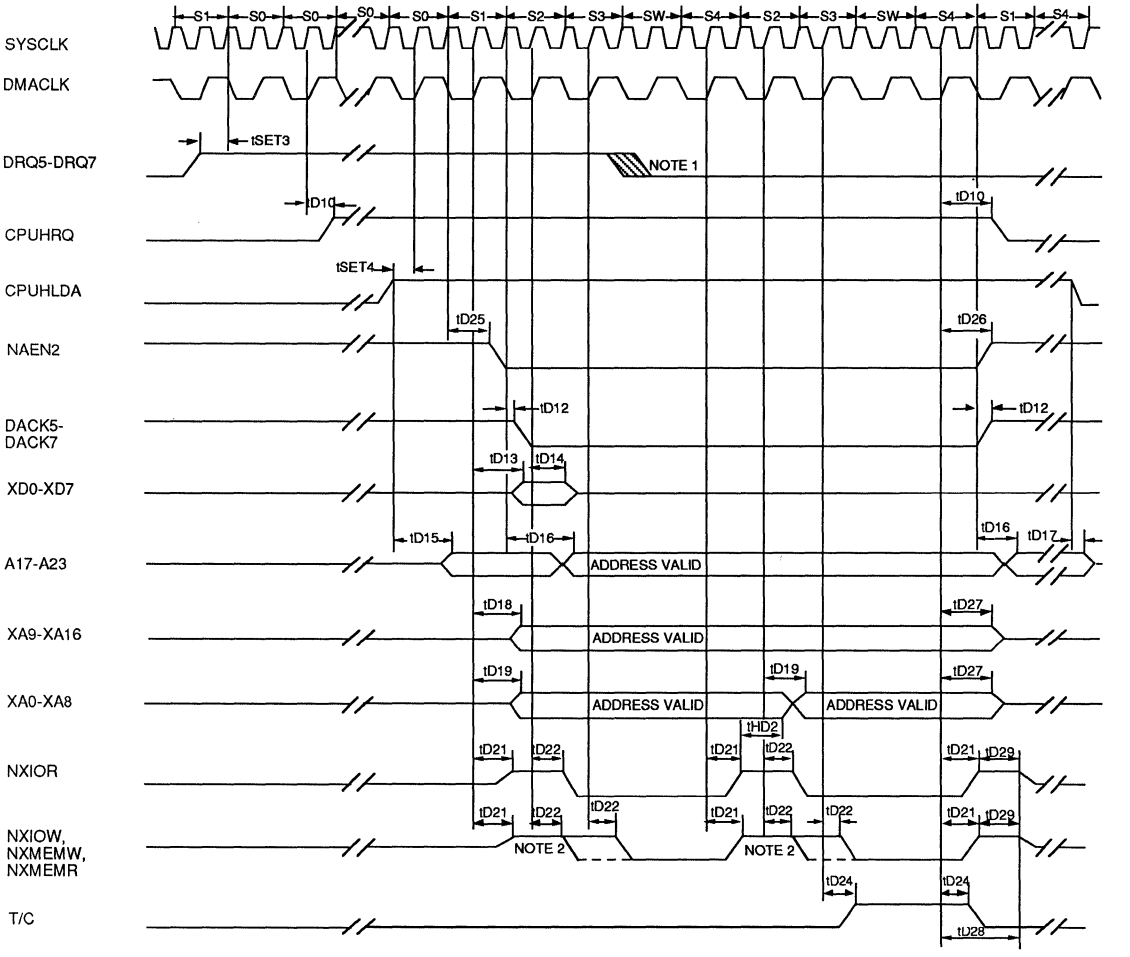



Figure 10. 16 BIT DMA TIMING

**NOTES:**
1. DRQ should be held active until NDACK is returned.
2. The first high to low transition shown here is for extended NXIOW and NXMEMW. The second high to low transition shown is for NXMEMR and late write on NXIOW and NXMEMW.

## AC TIMING DIAGRAMS SL9030

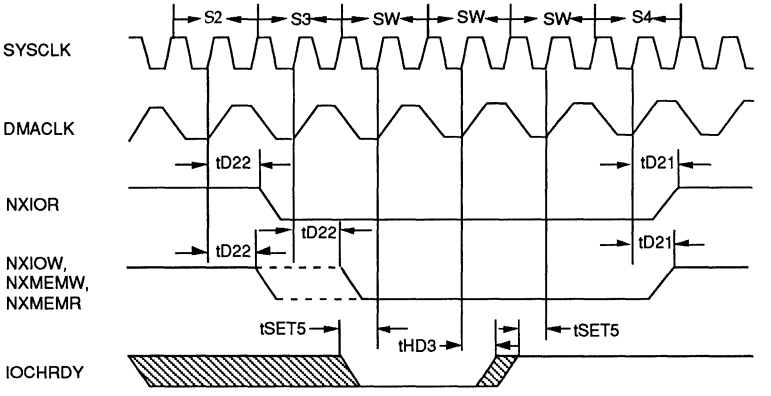



Figure 11. IOCHRDY TIMING

NOTE: The first wait state is inserted by internal circuitry in the SL9030 for all DMA cycles. Any additional wait states must by inserted using IOCHRDY.

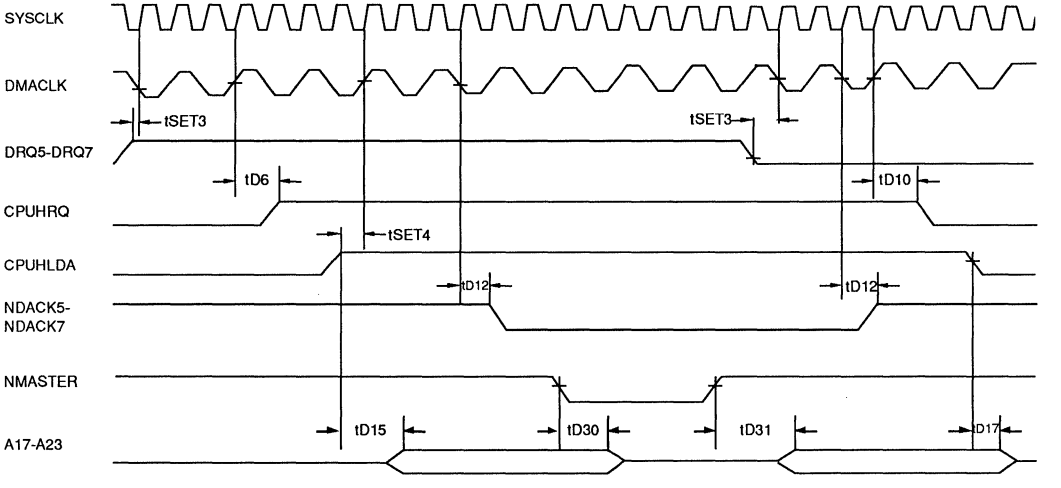



Figure 12. NMASTER TIMING

NOTES:
1. The DMA channel used for requesting control of the bus by a new bus master must be programmed in cascade mode. The new master should not pull NMASTER low until it has received the corresponding NDACK signal.
2. The timing shown is assuming one of the 16 bit DMAchannels is used. There will be extra cycles between DRQ and CPUHRQ before and after the request cycle when using an 8 bit DMA channel. These extra cycles are caused by the cascade delay from the slave 8237 through the master 8237.

## AC TIMING DIAGRAMS SL9030

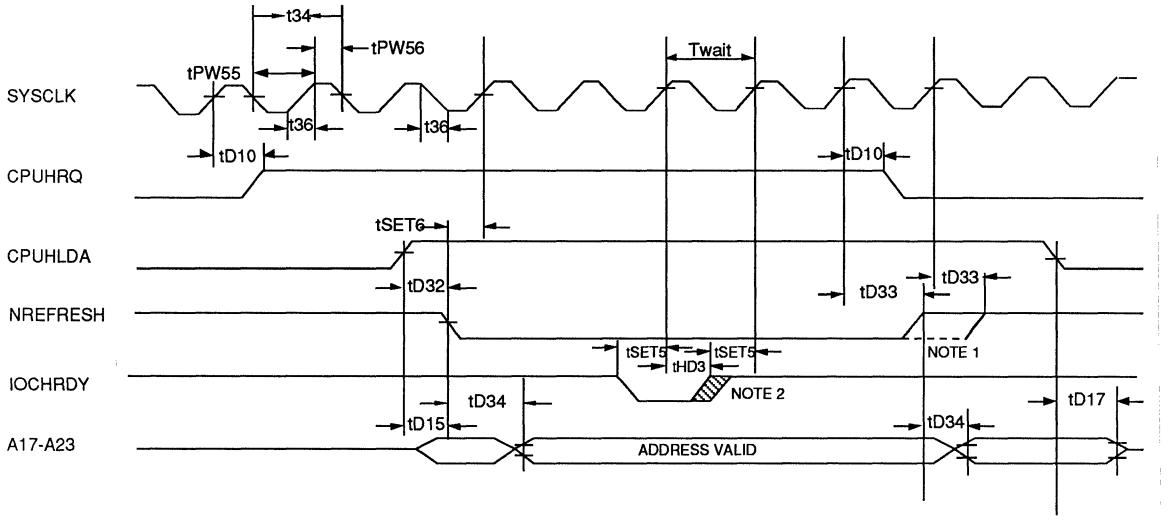
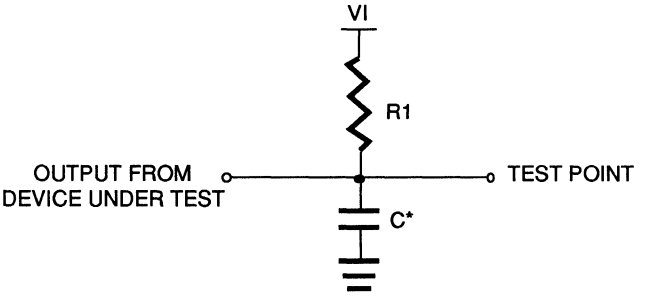



Figure 13. NREFRESH TIMING

NOTES:
1. A refresh pulse is normally three SYSCLK cycles long (with no wait states). Refresh pulses will be four SYSCLK cycles if a hold request is pending from the DMA controllers.
2. REFRESH cycles can be extended by inserting wait states using IOCHRDY.

## AC TIMING DIAGRAMS SL9030

FIG. 14 A.C. TEST CIRCUITS

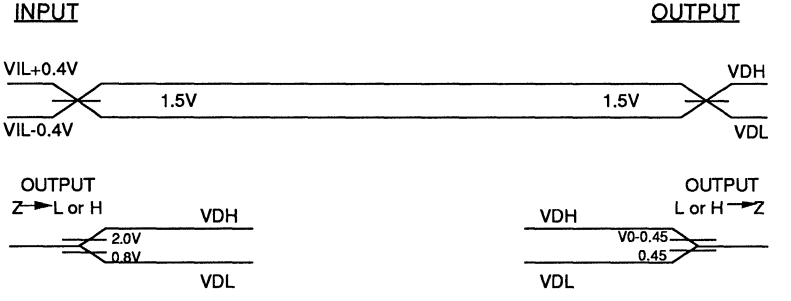



* Includes STRAY and JIG capacitance

**TEST CONDITION DEFINITION TABLE**

| PINS | VI | R1 | C1 |
|---|---|---|---|
| All Outputs Except EOP | 1.7V | 520 | 100pF |
| EOP | VCC | 1.6K | 50pF |

FIG. 15 A.C. TESTING INPUT, OUTPUT




A.C. Testing: All A.C. Parameters tested as per test circuits. Input RISE and FALL times are driven at Ins/V.

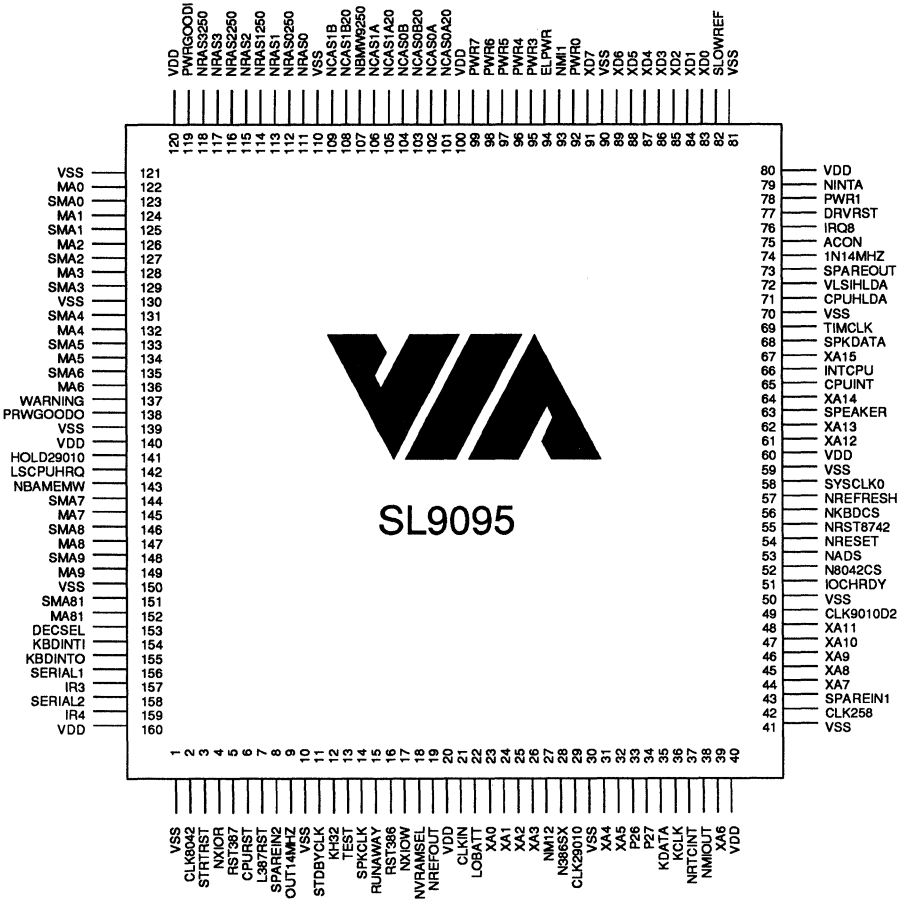
## FEATURES

- **Supports 80286, 80386SX, 80386DX, and 80486 Page Mode or Cache-based Laptop designs.**
- **IBM PC/AT Compatible.**
- **Software Programmable Power Management Unit. Provides Individual On/Off Control.**
- **Compatible with all CPU Clock Rates.**
- **Supports Suspend and Resume Modes.**
- **Auto Power On Capability.**
- **Supports Slow Refresh DRAMs.**
- **Sleep Mode.**
- **Generates all the necessary PC/AT Clock Signals.**
- **Advanced CMOS Technology.**
- **160 pin Plastic Flatpack.**

## DESCRIPTION

The SL9095 is an integrated CMOS Power Mangement Unit (PMU) which minimizes the power consumption and maximizes the battery life in laptop designs. The PMU is a single chip addition to the FlexSet PC/AT core logic chip set. The FlexSet provides all of the core logic required for any Intel microprocessor based designs (80286, 80386SX, 80386DX and 80486). This approach provides minimum chip count, low power dissipation, low cost and maximizes upward design compatibility.

## PINOUT


SL9095
VDD 120
PWRGOODI 119
NRAS3250 118
NRAS3 117
NRAS2250 116
NRAS2 115
NRAS1250 114
NRAS1 113
NRAS0250 112
NRAS0 111
VSS 110
NCAS1B 109
NCAS1B20 108
NBMW9250 107
NCAS1A 106
NCAS1A20 105
NCAS0B 104
NCAS0B20 103
NCAS0A 102
NCAS0A20 101
VDD 100
PWR7 99
PWR6 98
PWR5 97
PWR4 96
PWR3 95
ELPWR 94
NMI1 93
PWR0 92
XD7 91
VSS 90
XD6 89
XD5 88
XD4 87
XD3 86
XD2 85
XD1 84
XD0 83
SLOWREF 82
VSS 81
VSS 121
MA0 122
SMA0 123
MA1 124
SMA1 125
MA2 126
SMA2 127
MA3 128
SMA3 129
VSS 130
SMA4 131
MA4 132
SMA5 133
MA5 134
SMA6 135
MA6 136
WARNING 137
PRWGOODO 138
VSS 139
VDD 140
HOLD29010 141
LSCPUHRQ 142
NBAMEMW 143
SMA7 144
MA7 145
SMA8 146
MA8 147
SMA9 148
MA9 149
VSS 150
SMA81 151
MA81 152
DECSEL 153
KBDINTI 154
KBDINTO 155
SERIAL1 156
IR3 157
SERIAL2 158
IR4 159
VDD 160
80 VDD
79 NINTA
78 PWR1
77 DRVRST
76 IRQ8
75 ACON
74 1N14MHZ
73 SPAREOUT
72 VLSIHLDA
71 CPUHLDA
70 VSS
69 TIMCLK
68 SPKDATA
67 XA15
66 INTCPU
65 CPUINT
64 XA14
63 SPEAKER
62 XA13
61 XA12
60 VDD
59 VSS
58 SYSCLK0
57 NREFRESH
56 NKBDCS
55 NRST8742
54 NRESET
53 NADS
52 N8042CS
51 IOCHRDY
50 VSS
49 CLK9010D2
48 XA11
47 XA10
46 XA9
45 XA8
44 XA7
43 SPAREIN1
42 CLK258
41 VSS
1 VSS
2 CLK6042
3 STRTRST
4 NXIOR
5 RST387
6 CPURST
7 L387RST
8 SPAREIN2
9 OUT14MHZ
10 VSS
11 STDBYCLK
12 KH32
13 TEST
14 SPKCLK
15 RUNAWAY
16 RST386
17 NXIOW
18 NVRAMSEL
19 NREFOUT
20 VDD
21 CLKIN
22 LOBATT
23 XA0
24 XA1
25 XA2
26 XA3
27 NM12
28 N386SX
29 CLK29010
30 VSS
31 XA4
32 XA5
33 P26
34 P27
35 KDATA
36 KCLK
37 NRTCINT
38 NMIOUT
39 XA6
40 VDD

## GENERAL OPERATION

The SL9095 Power Management Unit supports three modes of operation, sleep mode, auto power off and suspend/resume. As an option, slow refresh DRAMs can be used to further reduce power during these various power down modes.

### SLEEP MODE:

When the CPU is not executing a program or I/O operation and waiting for a keyboard input, a programmable counter is initialized in the PMU. If an interrupt does not occur within the programmed time limit (2 seconds to 8 minutes), the PMU will initiate a sleep mode. During sleep mode, the Real Time Clock interrupt is blocked, the CPU is halted and the clock is stopped for the 80286 and SL9011 PC/AT System Controller. Power is turned off for the SL9025 Address Controller, SL9250 Memory Controller, SL9020 Data Controller, EPROM, RS232C, EL or LCD display and SCSI Hard Disk Controller. The clock is slowed down for 80386SX and 80386DX, such that the CPU consumes a minimum amount of power. Following a keyboard entry, the power is turned back on and the CPU resumes execution . The memory is refreshed by the Power Management Unit while in the sleep mode. At the next keyboard entry, mouse or modem interrupt the PMU initiates "auto power on" allowing the CPU to continue at the same step where it was previously halted.

### AUTO POWER OFF:

The Power Management Unit provides a programmable timeout counter to monitor the activity of a power hungry device. For example, the power to a electro-luminescent display can be automatically shut off if "no activity" has been detected for the programmed interval.

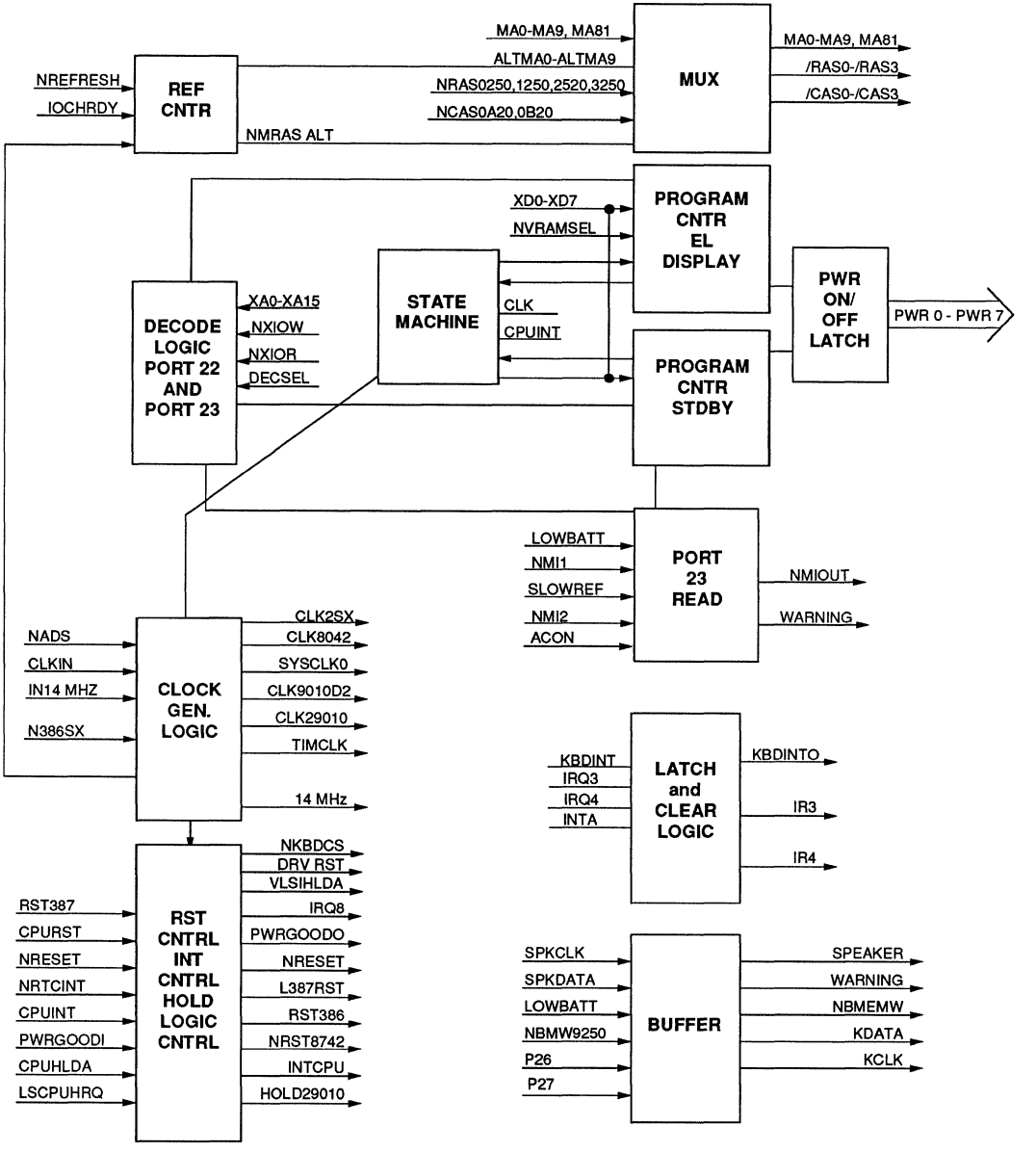
### SUSPEND / RESUME:

The Suspend / Resume feature is a system option that enables a user to turn the system off (suspend) and save the current application. When power is turned back on (resume), the application continues from the point where it was suspended. The contents of all registers are stored in the battery backed up memory space or disk when power is turned off. If they were copied to disk, they will get copied back to the registers when power is turned back on. In order to accomplish this, all registers are read / writeable. During the power off sequence, if the resume option is enabled, BIOS is required to set check sum flags in memory. When the power is turned on again, the BIOS should always check the flags to see whether the data stored in the memory was valid while the system was in standby. If the flags are not valid then the BIOS will start the system as a cold start. The BIOS software must implement the suspend/resume feature for the PMU to operate.

### SLOW REFRESH OPTION:

In order to use slow refresh DRAMs, the status bit on port 23 must be switched high. During power up, the system BIOS will check this status bit and set the SL9030 IPC refresh parameters.

## BLOCK DIAGRAM SL9095



## BLOCK DIAGRAM DESCRIPTION

1. REFRESH COUNTER: Generates refresh addresses during standby. Address generation during normal operations is handled by the SL9250.

2. MUX: Multiplexes memory addresses from the memory controller and the SL9095 refresh counter depending on the operating mode. DRAM selection should comprehend a small additional delay from MUX.

3. PROGRAMMABLE COUNTER, EL DISPLAY: Controls power supply and timing for an EL or LCD display.

4. PROGRAMMABLE STANDBY: Controls power supply and timing on power pins P0-P7.

5. STATE MACHINE: Generates the timing to control the programmable counters.

6. PORT 23 READ: Controls all status signals for machine operability.

7. CLOCK GENERATOR LOGIC: Generates all clocks required for PC/AT by using two oscillators.

8. RESET CONTROLLER: Generates all reset signals to ensure device operation during standby.

9. LATCH and CLEAR LOGIC: Latches keyboard, modem and mouse interrupts during standby.

## PIN DESCRIPTION SL9095

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| ACON | 75 | I | Active HIGH it indicates that the AC switch is ON. |
| CLKIN | 21 | I | Clock Input from an oscillator. It's frequency is twice that of the processor speed. |
| CLK258 | 42 | O | Clock Output for the CPU. It's frequency is twice that of the processor speed and it is connected to the CPU. |
| CLK29010 | 29 | O | Clock output for the PC/AT System Controller. It's frequency is twice that of the CPU speed and it is connected to the PC/AT SL9011 System Controller. |
| CLK8042 | 2 | O | 7MHz Keyboard Controller clock which is half the frequency of IN14MHZ frequency. |
| CLK9010D2 | 49 | O | Clock output for the PC/AT SL9011 System Controller. It's frequency is equal to the frequency of the internal processor clock. |
| CPUHLDA | 71 | I | CPU hold acknowledge input. It is active HIGH when a bus cycle is granted in response to a hold request. |
| CPUINT | 65 | I | Active HIGH, interrupt from the Interrupt Controller, when asserted, will wake up the system from Sleep Mode. |
| CPURST | 6 | I | Active High from Sleep Mode. CPU reset signal input from the PC/AT System Controller SL9011. |
| DECSEL | 153 | I | This signal selects the port address for the SL9095 PMU. A HIGH maps the PMU SL9095 at port 22 and 23. A LOW maps the PMU SL9095 at port A4EA and A4EB. |
| DRVRST | 77 | O | The DRIVE RESET is an active HIGH output. This signal is not generated in STDBY. When active, it resets the system. |
| ELPWR | 94 | I | Display Power. |
| HOLD29010 | 141 | O | This is the CPU Hold Request output. It is used to request control of the system bus. |
| IOCHRDY | 51 | I | The I/O Channel Ready is an active HIGH input from the AT bus. When active LOW, it indicates a not ready condition. |

## PIN DESCRIPTION SL9095 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| IN14MHZ | 74 | I | The CLK inputs from an oscillator are used to generate the clock signals OSC(14 MHz) , OSC/12 (TIMCLK) and the keyboard clock (CLK8042). |
| INTCPU | 66 | O | The INTCPU6 is an output used to interrupt the CPU. It is active HIGH. |
| IR3 | 157 | O | This is the interrupt request output to the SL9030 Integrated Peripheral Controller. This active HIGH serial port2 interrupt request signal is latched in STANDBY. |
| IR4 | 159 | O | This active HIGH interrupt request output to the SL9030 Integrated Peripheral Controller is latched in STANDBY. |
| IRQ8 | 76 | O | Interrupt request output for the Real Time Clock interrupt. |
| KBDINTI | 154 | I | Active HIGH Keyboard Interrupt from Keyboard Controller 8742. |
| KBDINTO | 155 | O | Active HIGH Keyboard Interrupt output to the SL9030 Integrated Peripheral Controller is latched in STANDBY. |
| KCLK | 36 | O | Buffered Keyboard Clock output. |
| KDATA | 35 | O | Buffered Keyboard Data output. |
| KH32 | 12 | I | This is the time base for the STANDBY counter. The clock is divided by 64K to generate STDBY CLK. |
| LOWBATT | 22 | I | A LOW signal on this input indicates that the battery is getting weak and needs to be recharged. |
| LSCPUHRQ | 142 | I | Active HIGH HOLDREQUEST input from the SL9030 Integrated Peripheral Controller. |
| L387RST | 7 | O | This output is latched RST387 and is not asserted when going into or coming out of STANDBY. It is connected to 80387SX coprocessor and it is active HIGH. |
| MA0 - MA9 | 122, 124, 126, 128, 132, 134, 136, 145, 147, 149 | O | This is the RAM address bus. |

## PIN DESCRIPTION SL9095 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| MA81 | 152 | O | This is the RAM address select pin for 1M DRAMs. |
| NADS | 53 | I | The address status is an input generated by the CPU. When asserted it indicates the start of a new cycle. |
| NBAMEMW | 143 | O | The Buffered Memory Write signal is active LOW. |
| NBMW9250 | 107 | I | The Memory Write input from the Memory Controller is active LOW. |
| NCAS0A,1A | 102, 106 | O | CAS0 and CAS1 for bank A is active LOW. |
| NCAS0A20, 1A20 | 101, 105 | I | CAS0 and CAS1 inputs from the SL9020 Data Controller for bank A is active LOW. |
| NCAS0B, 1B | 104, 109 | O | CAS0 and CAS1 for bank B is active LOW. |
| NCAS0B20, 1B20 | 103, 108 | I | CAS0 and CAS1 inputs from the SL9020 Data Controller for bank B is active LOW. |
| NINTA | 79 | I | The interrupt acknowledge is an active LOW input from the PC/AT SL9011 System Controller. |
| NKBDCS | 56 | O | This active LOW signal is asserted to select the Keyboard Controller 8742. |
| NMI1 | 93 | I | This is a Non Maskable Interrupt input from the PC/AT SL9011 System Controller. |
| NMI2 | 27 | I | This pin can be used for any NMI source in order to generate NMI, e.g. power failure. It is active HIGH. |
| NMIOUT | 38 | O | NMI output connected to the CPU. It is active HIGH. |
| NRAS0-3 | 111, 113, 115, 117 | O | Row address strobes for Banks 0, 1, 2 and 3 for the on board memory generated during the CPU or DMA cycles for memory access. It is active LOW. |
| NRAS0250-<br>NRAS3250 | 112, 114, 116, 118 | I | Row address strobes from the Memory Controller are active LOW. |
| NREFOUT | 19 | O | This active LOW signal is used to generate a refresh cycle for the DRAMs. This signal is not generated in the STANDBY wake up period. |

## PIN DESCRIPTION SL9095 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| NREFRESH | 57 | I | Active LOW from the SL9030 Integrated Peripheral Controller. When asserted it indicates the DRAM refresh cycle. |
| NRESET | 54 | I | The NRESET is active LOW from the PC/AT SL9011 System Controller. |
| NRST8742 | 55 | O | Active LOW Reset to 8742. |
| NRTCINT | 37 | I | This is the Real Time Clock input. |
| NVRAMSEL | 18 | I | This activates the ELPWR control pin. This will go HIGH for ELPWR to shutoff if Electroluminescence display is not accessed for the programmed time. |
| NXIOR | 4 | I | The peripheral bus input read is active LOW. |
| NXIOW | 17 | I | The peripheral bus output write is active LOW. |
| N386SX | 28 | I | This indicates if the CPU is 80286, 80386SX, or 80386DX. A LOW indicates a 80386SX or 80836DX. |
| N8042CS | 52 | I | This is the input signal from the SL9025 Address Controller. It is latched in STANDBY and active LOW. |
| OUT14MHZ | 9 | O | This Output has a buffered clock with the same frequency as the input IN14MHZ frequency. |
| PWRGOODI | 119 | I | The PWRGOODI is an active HIGH input from the power supply. |
| PWRGOODO | 138 | O | The PWRGOODO is an active HIGH output that generates the reset after STANDBY. |
| PWR0, PWR3-PWR7 | 92, 95 - 99 | O | These outputs control the power supply of different device. They are active LOW in STANDBY. When active HIGH it indicates that the power is ON. |
| PWR1 | 78 | O | This output controls the power on a device. It is active LOW in STANDBY. When active HIGH it indicates that the power is ON. |
| P26 | 33 | I | This is the keyboard data input from the Keyboard Controller 8742. |
| P27 | 34 | I | This is the keyboard data input from the Keyboard Controller 8742. |

## PIN DESCRIPTION SL9095 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| RST386 | 16 | O | This is the CPU reset signal. It is not generated in STANDBY and it is active HIGH. |
| RST387 | 5 | I | This input is active HIGH from the PC/AT SL9011 System Controller. |
| RUNAWAY | 15 | O | This output is generated if the CPU does not wake up after the sleep mode. |
| SERIAL 1 | 156 | I | This is the interrupt from the first serial port. |
| SERIAL 2 | 158 | I | This is the interrupt from the second serial port. |
| SLOWREF | 82 | I | Slow refresh DRAM.<br>1: Indicates that slow refresh DRAMs are used.<br>0: Indicates that regular DRAMs are used. |
| SMA0 - SMA9 | 123, 125, 127, 129, 131, 133, 135, 144, 146, 148 | I | RAM address bus inputs from the SL9X5X Memory Controller. |
| SMA81 | 151 | I | RAM address select input from the SL9X5X Memory Controller. |
| SPAREIN1 | 43 | I | Spare input of the NAND Gate. |
| SPAREIN2 | 8 | I | Spare input of the NAND Gate. |
| SPAREOUT | 73 | O | Spare output of the NAND Gate. |
| SPEAKER | 63 | O | This output is connected to the speaker. |
| SPKCLK | 14 | I | This CLK is used to generate an alarm. |
| SPKDATA | 68 | I | This is used with the SPKCLK to generate the speaker alarm. |
| STDBYCLK | 11 | O | This clock runs the programmable STDBY counter. (2 seconds) |
| STRTRST | 3 | I | This should be tied to VDD. This signal is used in simulation. |
| SYSCLK0 | 58 | O | System clock out is a free running system clock generated by dividing CPUCLK by 2. It is conditioned by the NADS signal. |

## PIN DESCRIPTION SL9095 (Cont'd.)

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| TEST | 13 | I | This signal is used to test the counters in simulation. This signal should be tied to VDD. |
| TIMCLK | 69 | O | This output has a buffered clock with a frequency 1/ 12th that of IN14MHZ (pin 74) frequency. |
| VDD | 20, 40, 60, 80, 100, 120, 140, 160 | | +5V, Power. |
| VLSIHLDA | 72 | O | Active HIGH output which indicates that a bus cycle is granted in response to HOLD REQUEST. |
| VSS | 1, 10,30, 41, 50 59, 70, 81, 90, 110, 121, 130, 139, 150 | | 0V, Ground. |
| WARNING | 137 | O | This signal indicates low battery warning through either the speaker or LED. |
| XA0-XA15 | 23-26, 31, 32, 39, 44-48, 61, 62, 64, 67 | I | Peripheral address bus inputs from the Address Controller SL9025. |
| XD0-XD7 | 83-89, 91 | I/O | Peripheral Data Bus. |

## DC CHARACTERISTICS SL9095

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Power Supply Current | IDDS | 0 | 100 | µA | Steady state* |
| Output High Voltage for Normal Output (IOL = 3.2 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 8 mA) | VOH | 4.0 | VDD | V | IOH = - 2 mA |
| Output High Voltage for Driver Output (IOL = 12 mA) | VOH | 4.0 | VDD | V | IOH = - 4 mA |
| Output High Voltage for Driver Output (IOL = 24 mA) | VOH | 4.0 | VDD | V | IOH = - 8 mA |
| Output Low Voltage for Normal Output (IOL = 3.2 mA) | VOL | Vss | 0.4 | V | IOL = 3.2 mA |
| Output Low Voltage for Driver Output (IOL = 8 mA) | VOL | Vss | 0.4 | V | IOL = 8 mA |
| Output Low Voltage for Driver Output (IOL = 12 mA) | VOL | Vss | 0.4 | V | IOL = 12.0 mA |
| Output Low Voltage for Driver Output (IOL = 24mA) | VOL | Vss | 0.5 | V | IOL = 24.0 mA |
| Input High Voltage for Normal Input | VIH | 2.2 | | V | |
| Input Low Voltage for Normal Input | VIL | | 0.8 | V | |
| Input High Voltage for CMOS Input | VIH | 0.7VDD | | V | |
| Input Low Voltage for CMOS Input | VIL | 0.3VDD | | V | |
| Input Leakage Current | ILI | -10 | 10 | µA | VI = 0 - VDD |
| Input Leakage Current | ILZ | -10 | 10 | µA | Tri-state VI = 0 - VDD |
| Input Pull-up/Down Resistor | RP | 25 | 100 | KΩ | VIH = VDD<br>VIL = VS |

NOTES:

* VIH = VDD, VIL = Vss

NRAS0 - NRAS3 = 24mA

CLK8042, OUT14MHz, MA0 - MA9, MA81
CLK29010, UDATA, KCLK, CLK2SX, CLK10D2
WARNING, TIMCLK, PWR0, ELPWR, PWR3-7, NCAS0A-NCAS1B = 12mA

RST386, LRST387, DRVRST, NRST8742 = 8mA

ALL OTHER OUTPUT = 3.2 mA

## AC CHARACTERISTICS SL9095

(TA = 0° C to 70 ° C, VDD = 5V ± 5%)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| t1 | CLK2 to CPUCLK (low to high) | 1.1 | 3.8 | ns |
| t2 | CLK2 to CPUCLK (high to low) | 1.1 | 3 | ns |
| t3 | CLK10D2 to SYSCLK (high to low) | 3 | 5 | ns |
| t4 | CLK10D2 to SYSCLK (low to high) | 2 | 5 | ns |
| t5 | NRAS0250-3250 to NRAS0-3 (high to low) | | 24 | ns |
| t6 | NRAS0250-3250 to NRAS0-3 (low to high) | | 16 | ns |
| t7 | NCAS(0A-1B) 9020 TO NCAS0A-1B (high to low) | | 14 | ns |
| t8 | NCAS(0A-1B) 9020 to NCAS0A-1B (low to high) | | 18 | ns |
| t9 | SMA0-SMA9 to MA0-MA9 Delay | | 18 | ns |
| t10 | CLK2SX to 386RST (high to low) | 4 | 18 | ns |
| t11 | CLK2SX to L387RST (low to high) | 4 | 18 | ns |
| t12 | CLK2SX to NDRVRST (low to high) | 4 | 15 | ns |
| t13 | CLK2SX to NRST8742 (low to high) | 4 | 15 | ns |
| t14 | SYSCLK to PERHLDA (low to high) | 4 | 10 | ns |
| t15 | LSCPUHRQ to HOLD29010 (low to high) | | 14 | ns |
| t16 | LSCPUHRQ to HOLD9010 (high to low) | | 16 | ns |
| t17 | P26 to KCLK (low to high) | | 14 | ns |
| t18 | P26 to KCLK (high to low) | | 16 | ns |
| t19 | P27 to KDATA (low to high) | | 14 | ns |
| t20 | P27 to KDATA (high to low) | | 16 | ns |
| t21 | NBMW9250 to NBAMEMW (high to low) | | 18 | ns |
| t22 | NBMW9250 to NBAMEMW (low to high) | | 14 | ns |
| t23 | CLK Period | 25 | | ns |
| t24 | CLK High Duration | 7 | | ns |
| t25 | CLK Low Duration | 7 | | ns |
| t26 | XD0-XD7 Hold Time | 8 | 20 | ns |

## CONFIGURATION REGISTERS

The following registers are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O Port 22H, followed by the Data Information to I/O Port 23H. If the DEC SEL Pin is low, the I/O Port Address changes from Port 22H to Port A4EAH and from Port 23H to Port A4EBH.

INDEX: 02H - EL Counter Register or Backlit Power Register. (WRITE)

This register holds the counter value to turn off the DC-AC converter for the EL or to turn off the LCD Power and Backlit Power in case an LCD Display is being used.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| EL CNT7 | EL CNT6 | EL CNT5 | EL CNT4 | EL CNT3 | EL CNT2 | EL CNT1 | EL CNT0 |

| BIT | FUNCTION |
|---|---|
| 7-0 | COUNTER VALUE (0-255)<br>D0 = 1 Specifies 2 second Interval<br>D0-7 = FF Specifies 8 Min. and 32 Secs. Intervals |

INDEX: 03H - Standy Counter Register. (WRITE)

This register holds the counter value to turn off the PWR0-PWR7 signals when the system goes in stand-by.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| STDBY CNT7 | | | | | | | STDBY CNT0 |

| BIT | FUNCTION |
|---|---|
| 7-0 | COUNTER VALUE (0-255)<br>D0 = 1 Specifies 2 second Interval<br>D0-7 = FF Specifies 8 Min. and 32 Secs. Intervals |

## CONFIGURATION REGISTERS

INDEX: 00 - Power Control Register. (WRITE)

This register holds the value of each power pin.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PWR 7 | | | | | | | PWR 0 |

| BIT | FUNCTION | |
|---|---|---|
| 0 | D0 = 0 | PWR0 =OFF = 0 |
| | D0 = 1 | PWR0 = ON = 1 |
| 1 | D1 = 0 | PWR1 = OFF = 0 |
| | D1 = 1 | PWR1 = ON = 1 |
| 2 | D2 = 0 | DISPWR0 = OFF = 0 |
| | D2 = 1 | DISPWR1 = ON = 1 |
| 3 | D3 = 0 | PWR3 = OFF = 0 |
| | D3 = 1 | PWR3 = ON = 1 |
| 4 | D4 = 0 | PWR4 = OFF = 1 |
| | D4 = 1 | PWR4 = ON = 1 |
| 5 | D5 = 0 | PWR5 = OFF = 0 |
| | D5 = 1 | PWR5 = ON = 1 |
| 6 | D6 = 0 | PWR6 = OFF = 0 |
| | D6 = 1 | PWR6 = ON = 1 |
| 7 | D7 = 0 | PWR7 = OFF = 0 |
| | D7 = 1 | PWR7 = ON = 1 |

## CONFIGURATION REGISTERS

INDEX: 01H - Start Count Register. (WRITE)

This register holds the value to start the count to turn off power pin PWR0-PWR7 in STANDBY.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| TXD7 | TXD6 | TXD5 | TXD4 | TXD3 | TXD2 | TXD1 | TXD0 |

| | | |
|---|---|---|
| 0 | D0 = 1 | Starts down counting of EL Display or LCD Display counter register. DISPWR. |
| | DO = 0 | No Down Count. DISP PWR = ON |
| 1 | D1 = 1 | Starts down counting of stand-by counter. PWR0-PWR7 are turned off when counter reaches 0. |
| | D1 = 0 | No DWN Counter. POWER = ON. |
| 2 | D2 = TXD2 | SPARE. |
| 3 | D3 = TXD3 = NBLOCK | |
| | D3 = 1 | Blocks the HOLD request to SL9010. (HOLD29010). When the Processor goes to HALT. |
| 4 | D4 = TXD4 = 1 | PWR4 Pin will not be turned off in standby. PWR4 = 1 |
| | D4 = TXD4=0 | PWR4 Pin will be turned off in standby. PWR4 = 0. |
| 5 | D5 = TXD5 = 1 | PWR5 Pin will not be turned off in standby. PWR5 = 1 |
| | D5 = TXD5 = 0 | PWR5 Pin will be turned off in standby. |
| 6 | D6 = TXD6 = 1 | PWR6 Pin will not be turned off in standby. |
| | D6 = TXD6 = 0 | PWR6 Pin will be turned off in standby. |
| 7 | D7 = TXD7 = 1 | PWR7 Pin will not be turned off in standby. |
| | D7 = TXD7 = 0 | PWR7 Pin turned off in standby. |

## CONFIGURATION REGISTERS

INDEX: 01H - Status Register. (READ)

This register holds the status of several pins.

| XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |
|---|---|---|---|---|---|---|---|

**XD0 = 1** **NMI2 is On. ( Nonmaskable Interrupt)X**

**XD1 = 2** **Slow Refresh DRAMs are used.**

**XD2 =** **Space.**

**XD3=** **Space.**

**XD4=1** **AC Power On.**

**XD5=0** **Battery Low.**

**XD6=1** **EL Display Power is On.**

**XD7=1** **Power 3 Pin is On (Hard Disk).**

## AC TIMING DIAGRAMS SL9095

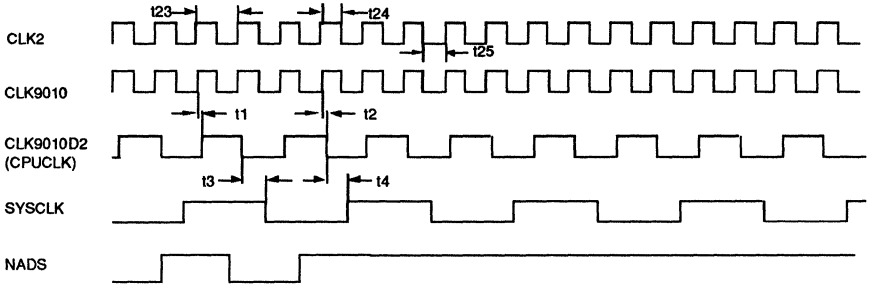



FIG. 1 CLK DURATION AND DELAYS FROM CLK2 OR CPUCLK.

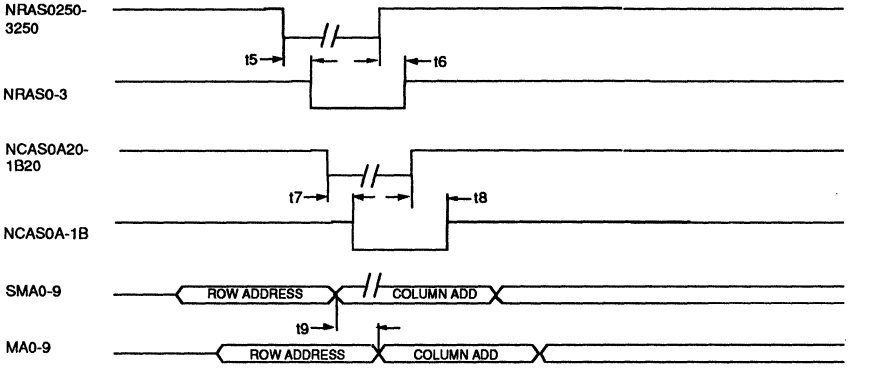



FIG. 2 OUTPUT SIGNAL DELAYS FROM INPUTS.

## AC TIMING DIAGRAMS SL9095

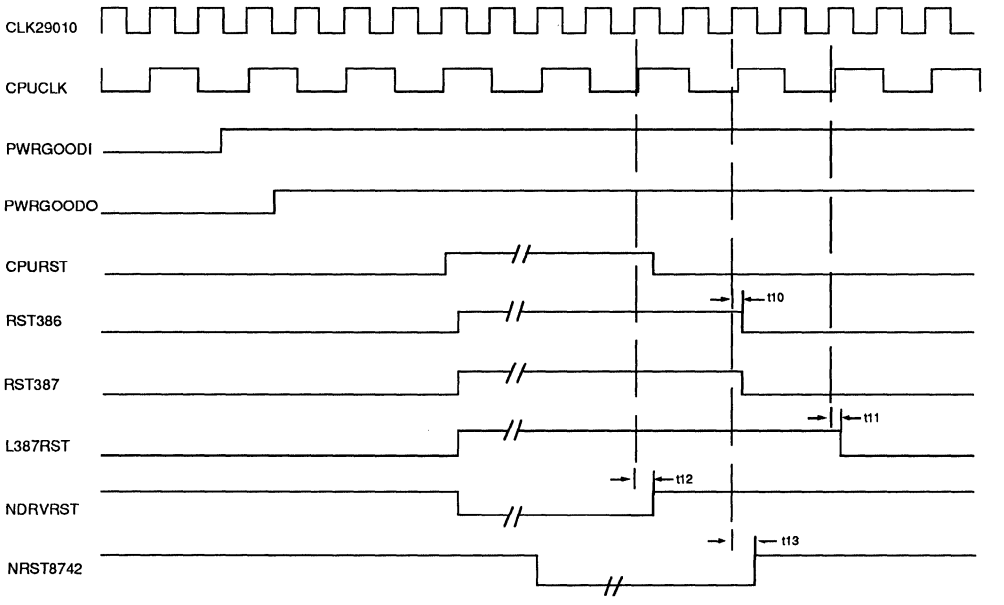



FIG. 3 RST386, L387RST andNRST8742 DELAYS FROM INPUTS AND CPUCLK

## AC TIMING DIAGRAMS SL9095

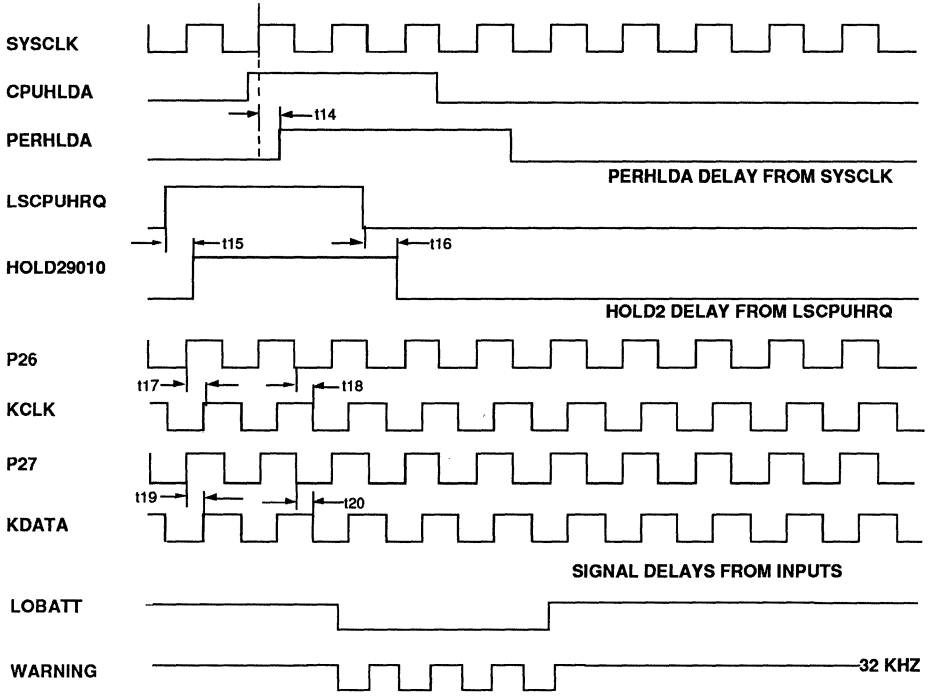



FIG. 4 WARNING SIGNAL TO SPEAKER

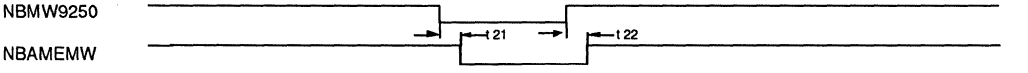



FIG. 5 NBAMEMW SIGNAL DELAYS FROM INPUT NBMW9250.

## AC TIMING DIAGRAMS SL9095

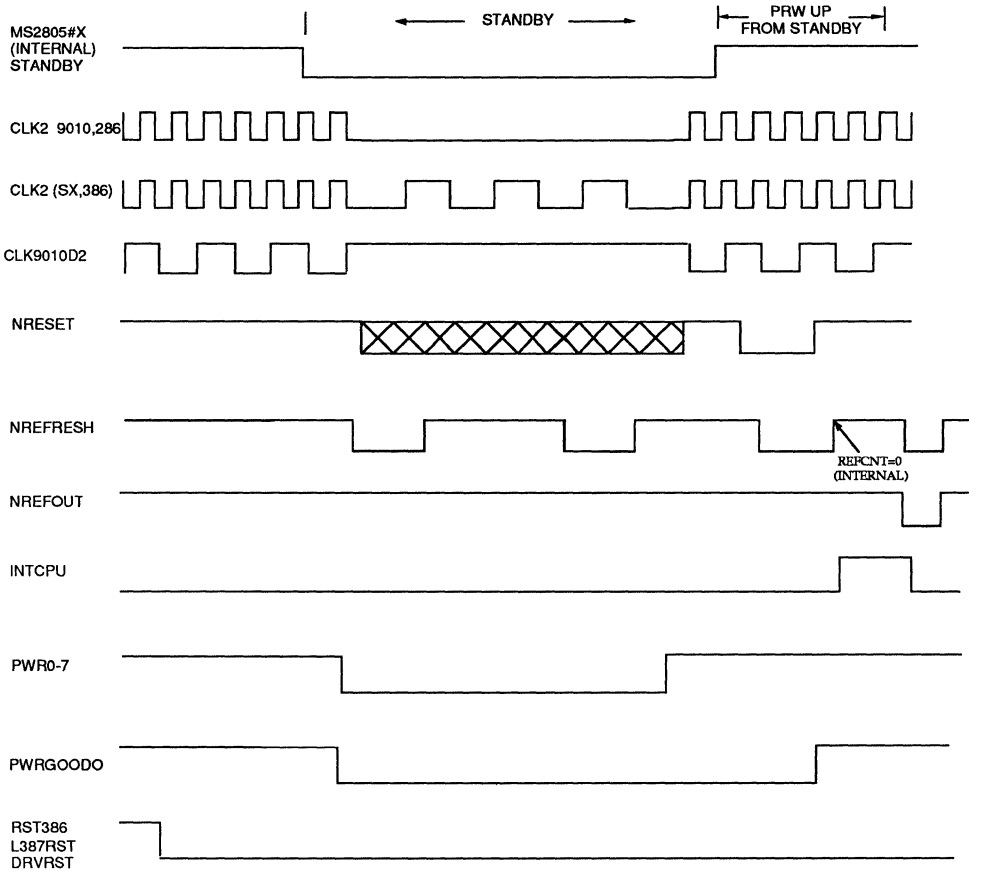



FIG. 6 STANDBY CYCLE TIMINGS

## AC TIMING DIAGRAMS SL9095

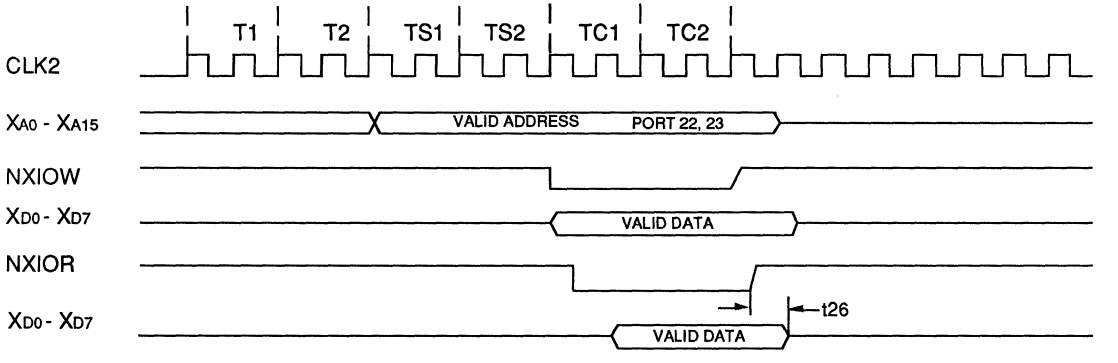
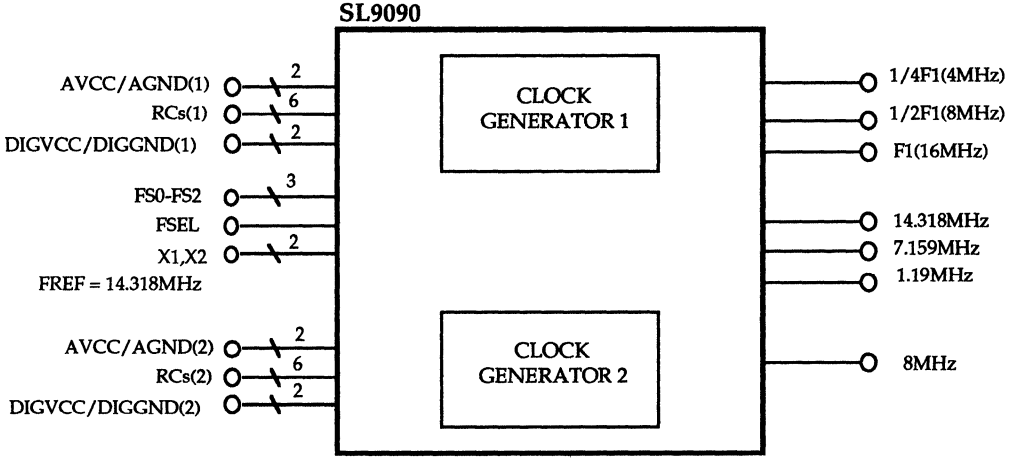



FIG. 7 EXTERNAL I/O CYCLE.

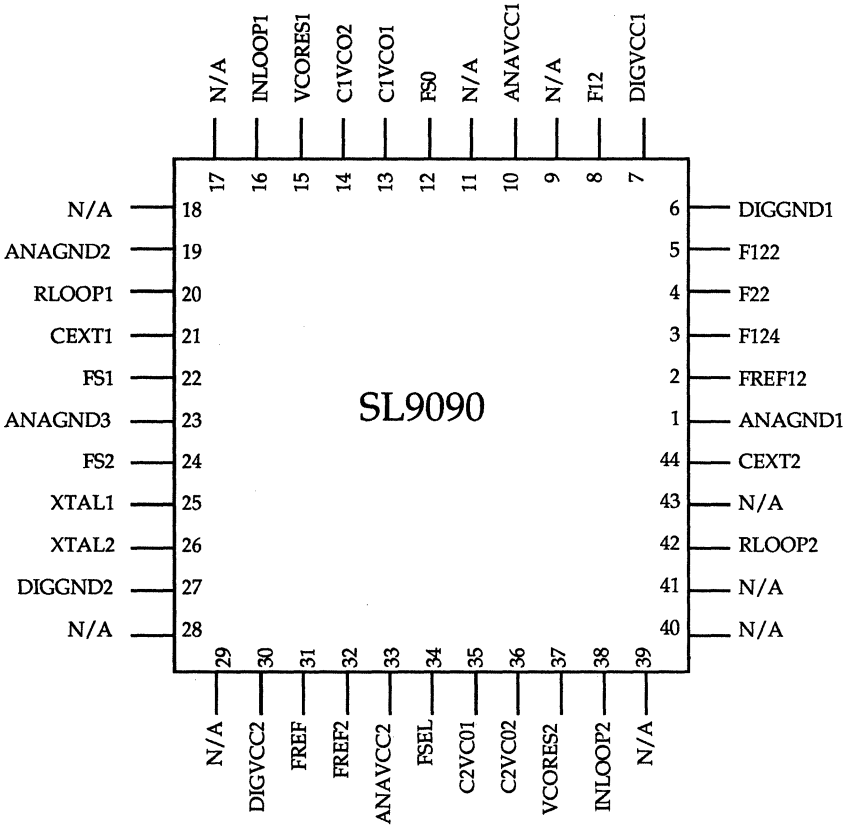
## FEATURES

- Generates all Essential Clock Signals for P.C.'s.
- Supports 8086/8088/80286/80386SX/80386-based designs.
- Clock Options of 60, 50, 48, 40, or 32 MHz and Others.
- Requires Only One Crystal and Few RC Components.
- Two Independent Clock Generators.
- Glitch Free Switching for both Clock Generators.
- All Outputs Capable of 8 mA Drive.
- Advanced Bipolar Technology.
- 40 Pin Plastic Dip, or 44 Pin PLCC.

## FUNCTIONAL BLOCK DIAGRAM



## PINOUT


SL9090
1 ANAGND1
2 FREF12
3 F124
4 F22
5 F122
6 DIGGND1
7 DIGVCC1
8 F12
9 N/A
10 ANAVCC1
11 N/A
12 FS0
13 C1VCO1
14 C1VCO2
15 VCORES1
16 INLOOP1
17 N/A
18 N/A
19 ANAGND2
20 RLOOP1
21 CEXT1
22 FS1
23 ANAGND3
24 FS2
25 XTAL1
26 XTAL2
27 DIGGND2
28 N/A
29 N/A
30 DIGVCC2
31 FREF
32 FREF2
33 ANAVCC2
34 FSEL
35 C2VC01
36 C2VC02
37 VCORES2
38 INLOOP2
39 N/A
40 N/A
41 N/A
42 RLOOP2
43 N/A
44 CEXT2

## DESCRIPTION

The SL9090 is a Universal Clock Chip capable of generating all essential clock signals that are used in a typical P.C. design. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs. The outputs of this clock chip are programmable through the keyboard and also by jumper settings. Clock options of 60 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz and their multiples are available, in order to give flexibility to the user.

Frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. FSEL is used to control the system I/O bus clock. During a CPU cycle the FSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the FSEL goes low and fixed frequencies of 16 MHz, 8 MHz and 4 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). Designer have an option to run the system I/O clock at half the CPU clock as well. This is achieved by connecting the FSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the FSEL signal to be controlled through the keyboard by pressing "CTL ALT +" or "CTL ALT-".

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. This frequency is divided by 2 internally and 7.159 MHz is supplied to the output through the FREF2 pin for the keyboard controller. The FREF12 pin has an output of 1.19 MHz and is used by the timer1 (8254) in the peripheral controller for refresh. All outputs are capable of 8mA drive.

The SL9090 consists of two independent Voltage controlled Oscillators (VCOs) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9090. This reference frequency is fed into the phase sensitive detectors to differentiate the difference in phase between the reference frequency being generated by the VCOs. This becomes an input to the charge pumps which in turn generates a signal to sink or source the charge. This signal is buffered by the buffer amplifiers between the charge pumps and the VCOs. The output from the VCOs are divided to generate the appropriate outputs.

The SL9090 is designed, using advanced Bipolar technology and is available in a 44 pin PLCC. It requires only one crystal (14.3 MHz) and a few RC components to generate all the essential clocks that are required for a P.C. design. As there is only one crystal on the system board, the Electro Magnetic Radiation is reduced significantly facilitating FCC approval. This makes the SL9090 an ideal low cost solution with capabilities for universal applications.

## PIN DESCRIPTION

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| ANAGND1,2,3 | 1,19,23 | - | Analog Ground. |
| ANAVCC1,2 | 10,33 | - | Analog VCC +5/12V for Clock generator 1,2. |
| C1VCO1,2 | 13,14 | I | VCO capacitor pin 1, 2 for Clock generator 1. |
| C2VCO1,2 | 35,36 | I | VCO capacitor pin 1, 2 for Clock generator2. |
| CEXT1,2 | 21,44 | I | Charge pump pin for Clock generator 1,2. |
| DIGGND1,2 | 6,27 | - | Digital Ground. |
| DIGVCC1,2 | 7,30 | - | Digital +5V supply. |
| F22 | 4 | O | 8 MHz output. |
| F12 | 8 | O | FREQ 1 or 16 MHz output. |
| F122 | 5 | O | FREQ 1 / 2 or 8 MHz output. |
| F124 | 3 | O | FREQ 1 / 4 or 4 MHz output. |
| FREF | 31 | O | 14.318 MHz output. |
| FREF2 | 32 | O | 7.159 MHz output (Timer clock). |
| FREF12 | 2 | O | 1.19 MHz output (Keyboard clock). |
| FS0-FS2 | 12,22,24 | I | Frequency Select LSB-MSB (from Keyboard or Jumpers). |
| FSEL | 34 | I | Frequency Select input (Dynamic). |
| INLOOP1,2 | 16,38 | I | Loop filter resistor pin 1 for Clock generator 1,2. |
| N.C. | 9,11,17,18,28, 29,39,40,41,43 | - | No Connect. |
| RLOOP1,2 | 20,42 | I | Loop filter resistor pin 2 for Clock generator 1,2. |
| VCORES1,2 | 15,37 | I | Center frequency resistor for Clock generator 1,2. |
| XTAL1,2 | 25,26 | X1,X2 | Crystal oscillator pin 1,2. |

## FREQUENCY SELECT CODES

| PIN NAME | FSEL | FS2 | FS1 | FS0 | F12 | F122 | F124 | F2 | F22 | |
|---|---|---|---|---|---|---|---|---|---|---|
| PIN No. | 34 | 24 | 22 | 12 | 8 | 5 | 3 | - | 4 | |
| FUNCTION | | | | | (F1,F2) | $\frac{(F1,F2)}{2}$ | $\frac{(F1,F2)}{4}$ | (F2) | $\frac{(F2)}{2}$ | UNIT |
| | 1 | 0 | 0 | 0 | 48 | 24 | 12 | 16 | 8 | MHz |
| | 1 | 0 | 0 | 1 | 50 | 25 | 12.5 | 16 | 8 | MHz |
| | 1 | 0 | 1 | 0 | 60 | 30 | 15 | 16 | 8 | MHz |
| | 1 | 0 | 1 | 1 | 19.2 | 9.6 | 4.8 | 16 | 8 | MHz |
| | 1 | 1 | 0 | 0 | 32 | 16 | 8 | 16 | 8 | MHz |
| | 1 | 1 | 0 | 1 | 40 | 20 | 10 | 16 | 8 | MHz |
| | 0 | X | X | X | 16 | 8 | 4 | 16 | 8 | MHz |

| PIN NAME | FREF | FREF2 | FREF12 | |
|---|---|---|---|---|
| PIN No. | 31 | 32 | 2 | |
| FUNCTION | (FREF) | $\frac{(FREF)}{2}$ | $\frac{(FREF)}{12}$ | UNIT |
| | 14.318 | 7.159 | 1.19 | MHz |

NOTES:

1. FS0, FS1, FS2, & FSEL can all be switched dynamically.
2. FSEL switching response time is less than 2X F1 clock cycles.
3. FS0, FS1 & FS2 switch occurs within 1 μs to 10% of selected frequency.

## DC CHARACTERISTICS SL9090

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| Parameters | Symbol | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Low Level Input Voltage | VIL | 0 | 0.8 | V | |
| Low Level Input Current | IIL | | -0.6 | mA | Vin = 0.4V |
| High Level Input Voltage | VIH | 2.0 | 5.25 | V | |
| High Level Input Current | IIH | | 10 | mA | Vin = DIGVCC |
| Low Level Output Voltage | VOL1 | | 0.5 | V | Iol = 3mA |
| High Level Output Voltage | VOH1 | 2.4 | | V | Ioh = -400 µA |
| Low Level Output Voltage (low power TTL) | VOL2 | | 0.5 | V | Iol = 8mA |
| High Level Out Voltage (low power TTL) | VOH2 | 2.4 | | V | Ioh = -400µA |
| Supply Current | ICC | | 140 | mA | |

NOTES

1. Thermal resistance of package = 66 °C/W.
2. Calculated worst case tpd factor = 1.81.
3. Calculated max junction temp = 117° C.

## AC CHARACTERISTICS

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

XTAL1, XTAL2, Crystal frequency.....14.318 MHz

F12, F122 Duty Cycle.....45:55 - 55:45
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

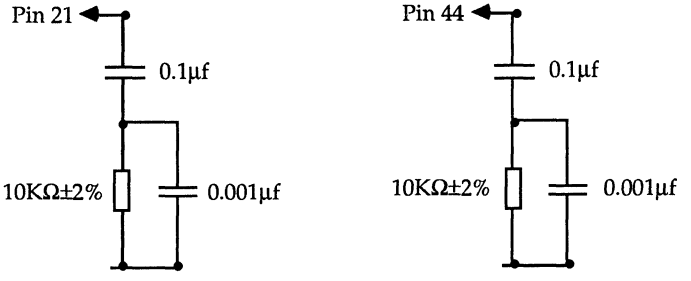
F2, F22, FREF, FREF2, FREF12 duty Cycle.....40:60 - 60:40
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

Settling time from change of FS1, FS2, FS3.....1uS to +/- 10% of defined frequency.
(300uS to lock.)

## EXTERNAL COMPONENTS

| Description | Name | Clo ck Generator 1 | Clock Generator 2 |
|---|---|---|---|
| Shunt Regulator | (RSHUNT) | 100Ω±2% | 100Ω±2% |
| Center frequency resistor | (VCORES) | 2.2KΩ±1% | No Connect |
| Loop filter resistor | (RLOOP - INLOOP) | 1.8KΩ±1% | 1.8KΩ±1% |
| VCO Capacitor | (CVCO1 - CVCO2) | 10pf±0.5pf | 10pf±0.5pf |

Charge Pump Components (CEXT) Connected as follows:



# SL9090A UNIVERSAL PC/AT CLOCK CHIP

PRELIMINARY

## FEATURES

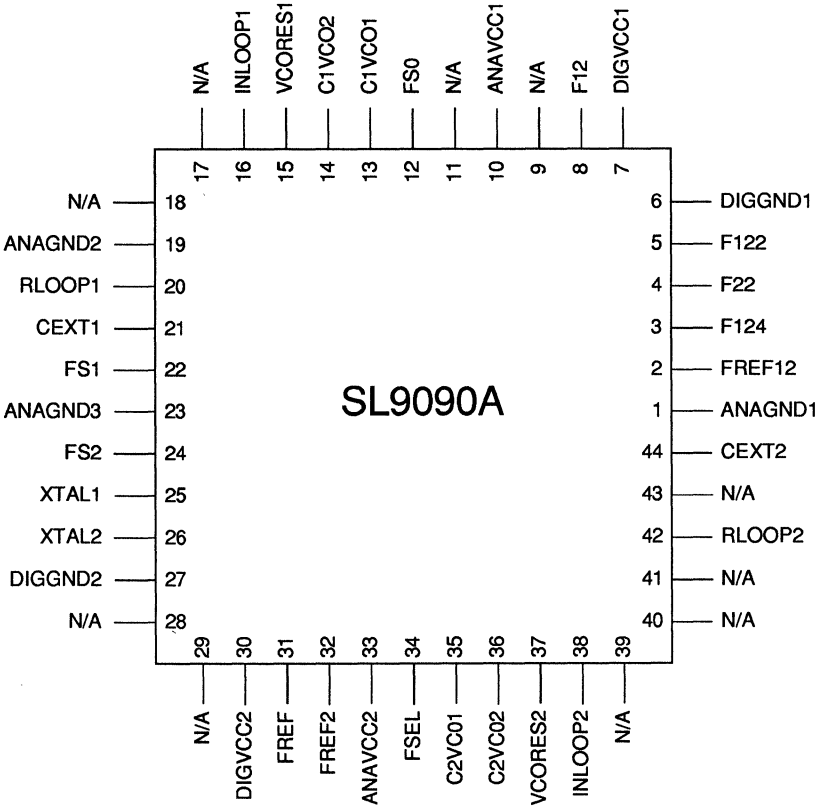
- **Generates all Essential Clock Signals for P.C.'s.**
- **Supports 8086/8088/80286/80386SX/80386DX/80486-based designs.**
- **Clock Options of 66, 50, 48, 40, 32, 24 MHz and Others.**
- **Facilitates FCC approval by reducing EMR.**
- **Requires Only One Crystal and a Few RC Components.**
- **Two Independent Clock Generators.**
- **Glitch Free Switching for both Clock Generators.**
- **All Outputs Capable of 8 mA Drive.**
- **Advanced Bipolar Technology.**
- **44 Pin PLCC.**

## DESCRIPTION SL9090A

The SL9090A is a Universal Clock Chip capable of generating all essential clock signals that are used in a typical P.C. design. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs. The outputs of this clock chip are programmable through the keyboard and also by jumper settings. Clock options of 66 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz and 24 MHz. Multiples are available, giving flexibility to the user.

Frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. FSEL is used to control the system I/O bus clock. During a CPU cycle the FSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the FSEL goes low and fixed frequencies of 32 MHz, 16 MHz and 8 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pin F124 guaranties the add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock, by connecting the FSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the FSEL signal to be controlled through the keyboard by pressing "CTL ALT +" or "CTL ALT-".

## PINOUT


SL9090A
1 ANAGND1
2 FREF12
3 F124
4 F22
5 F122
6 DIGGND1
7 DIGVCC1
8 F12
9 N/A
10 ANAVCC1
11 N/A
12 FS0
13 C1VCO1
14 C1VCO2
15 VCORES1
16 INLOOP1
17 N/A
18 N/A
19 ANAGND2
20 RLOOP1
21 CEXT1
22 FS1
23 ANAGND3
24 FS2
25 XTAL1
26 XTAL2
27 DIGGND2
28 N/A
29 N/A
30 DIGVCC2
31 FREF
32 FREF2
33 ANAVCC2
34 FSEL
35 C2VC01
36 C2VC02
37 VCORES2
38 INLOOP2
39 N/A
40 N/A
41 N/A
42 RLOOP2
43 N/A
44 CEXT2

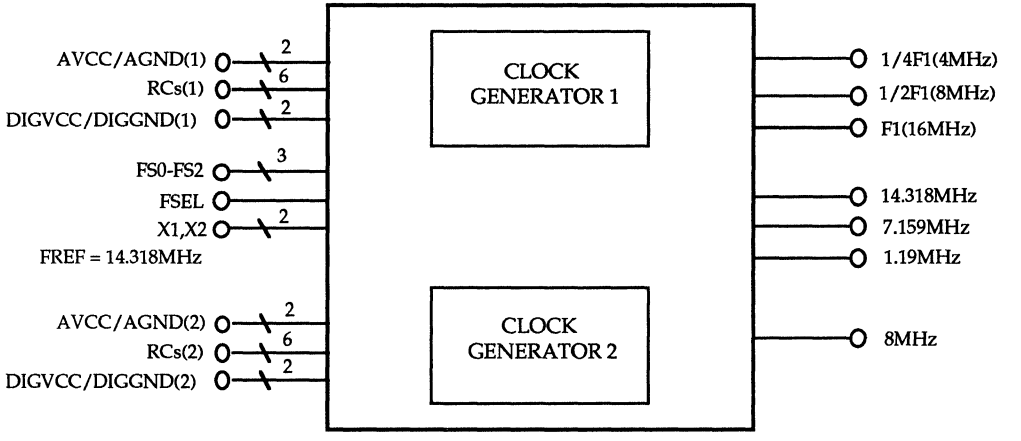
## DESCRIPTION (Cont'd)

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. This frequency is divided by 2 internally and 7.159 MHz is supplied to the output through the FREF2 pin for the keyboard controller. The FREF12 pin has an output of 1.19 MHz and is used by the timer1 (8254) in the peripheral controller for refresh. All outputs are capable of 8mA drive.

The SL9090A consists of two independent Voltage Controlled Oscillators (VCOs) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9090A. Phase difference between this reference frequency and that generated by the VCOs are tracked by phase sensitive detectors. This becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCOs. The output from the VCOs are divided to generate the appropriate outputs.

The SL9090A is designed, using advanced Bipolar technology and is available in a 44 pin PLCC. It requires only one crystal (14.3 MHz) and a few RC components to generate all the essential clocks that are required for a P.C. design. As there is only one crystal on the system board, the Electro Magnetic Radiation is reduced significantly facilitating FCC approval. This makes the SL9090A an ideal low cost solution with capabilities for universal applications.

## FUNCTIONAL BLOCK DIAGRAM SL9090A



## PIN DESCRIPTION

| SYMBOL | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| ANAGND1,2,3 | 1,19,23 | - | Analog Ground. |
| ANAVCC1,2 | 10,33 | - | Analog VCC for Clock generator 1,2. |
| C1VCO1,2 | 13,14 | I | VCO capacitor pin 1, 2 for Clock generator 1. |
| C2VCO1,2 | 35,36 | I | VCO capacitor pin 1, 2 for Clock generator2. |
| CEXT1,2 | 21,44 | I | Charge pump pin for Clock generator 1,2. |
| DIGGND1,2 | 6,27 | - | Digital Ground. |
| DIGVCC1,2 | 7,30 | - | Digital +5V supply. |
| F22 | 4 | O | 16 MHz output. |
| F12 | 8 | O | F1 or F2 (32 MHz) output. |
| F122 | 5 | O | F1/2 or F2 (16 MHz) output. |
| F124 | 3 | O | F1/4 or F2 (8 MHz) output. |
| FREF | 31 | O | 14.318 MHz output. |
| FREF2 | 32 | O | 7.159 MHz output (Timer clock). |
| FREF12 | 2 | O | 1.19 MHz output (Keyboard clock). |
| FS0-FS2 | 12,22,24 | I | Frequency Select (from Keyboard or Jumpers) as shown in Table 1. |
| FSEL | 34 | I | Frequency Select input (Dynamic). When FSEL is 1, F1 is selected. When it is 0, F2 is selected. |
| INLOOP1,2 | 16,38 | I | Loop filter resistor pin 1 for Clock generator 1,2. |
| N/C | 9,11,17,18,28, 29,39,40,41,43 | - | No Connection. |
| RLOOP1,2 | 20,42 | I | Loop filter resistor pin 2 for Clock generator 1,2. |
| VCORES1,2 | 15,37 | I | Center frequency resistor for Clock generator 1,2. |
| XTAL1,2 | 25,26 | X1,X2 | Crystal oscillator pin 1,2. |

## FREQUENCY SELECT CODES

| PIN NAME | FSEL | FS2 | FS1 | FS0 | F12 | F122 | F124 | F2 | F22 | |
|---|---|---|---|---|---|---|---|---|---|---|
| PIN No. | 34 | 24 | 22 | 12 | 8 | 5 | 3 | - | 4 | |
| FUNCTION | | | | | (F1,F2) | $\frac{(F1,F2)}{2}$ | $\frac{(F1,F2)}{4}$ | (F2) | $\frac{(F2)}{2}$ | UNIT |
| | 1 | 0 | 0 | 0 | 48 | 24 | 12 | 32 | 16 | MHz |
| | 1 | 0 | 0 | 1 | 50 | 25 | 12.5 | 32 | 16 | MHz |
| | 1 | 0 | 1 | 0 | 24 | 12 | 6 | 32 | 16 | MHz |
| | 1 | 0 | 1 | 1 | 66 | 33 | 16.5 | 32 | 16 | MHz |
| | 1 | 1 | 0 | 0 | 32 | 16 | 8 | 32 | 16 | MHz |
| | 1 | 1 | 0 | 1 | 40 | 20 | 10 | 32 | 16 | MHz |
| | 0 | X | X | X | 32 | 16 | 8 | 32 | 16 | MHz |

Table 1

| PIN NAME | FREF | FREF2 | FREF12 | |
|---|---|---|---|---|
| PIN No. | 31 | 32 | 2 | |
| FUNCTION | (FREF) | $\frac{(FREF)}{2}$ | $\frac{(FREF)}{12}$ | UNIT |
| | 14.318 | 7.159 | 1.19 | MHz |

Table 2

NOTES:

1. FS0, FS1, FS2, & FSEL can all be switched dynamically.
2. FSEL switching response time is less than 2X F1 clock cycles.
3. FS0, FS1 & FS2 switch occurs within 1 μs to 10% of selected frequency.

## DC CHARACTERISTICS SL9090A

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

| Parameters | Symbol | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Low Level Input Voltage | VIL (TTL) | 0 | 0.8 | V | |
| Low Level Input Current | IIL (TTL) | | -0.6 | mA | Vin = 0.4V |
| High Level Input Voltage | VIH (TTL) | 2.0 | 5.25 | V | |
| High Level Input Current | IIH (TTL) | | 10 | mA | Vin = DIGVCC |
| Low Level Output Voltage | VOL1 (TTL) | | 0.5 | V | Iol = 8mA |
| High Level Output Voltage | VOH1 (TTL) | 2.4 | | V | Ioh = -400 µA |
| Low Level Output Voltage (Low power TTL) | VOL2 (FREF) | | 0.5 | V | Iol = 16mA |
| High Level Output Voltage (Low power TTL) | VOH2 (FREF) | 2.4 | | V | Ioh = -2mA |
| Supply Current | ICC | 140 | 210 | mA | All pins floating |

NOTES

1. Thermal resistance of package = 66° C/W.
2. Calculated worst case tpd factor = 1° 81.
3. Calculated max junction temp = 117° C.

## AC CHARACTERISTICS SL9090A

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

XTAL1, XTAL2, Crystal frequency.....14.318 MHz

F12, F122 Duty Cycle.....43:57 - 57:43
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

F2, F22, FREF, FREF2, FREF12 duty Cycle.....40:60 - 60:40
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

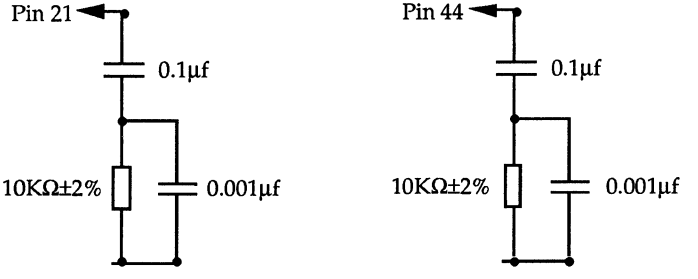
Settling time from change of FS1, FS2, FS3.....1uS to +/- 10% of defined frequency.
(300uS to lock.)

## EXTERNAL COMPONENTS

| Description | Name | Clock Generator 1 | Clock Generator 2 |
|---|---|---|---|
| Shunt Regulator | (RSHUNT) | 100Ω±2% | 100Ω±2% |
| Center frequency resistor | (VCORES) | 3.0K±1% | 3.0K |
| Loop filter resistor | (RLOOP - INLOOP) | 820Ω±1% | 1.6K±1% |
| VCO Capacitor | (CVCO1 - CVCO2) | 10pf±0.5pf | 10pf±0.5pf |

Table 3

Charge Pump Components (CEXT) Connected as follows:



## APPLICATION INFORMATION

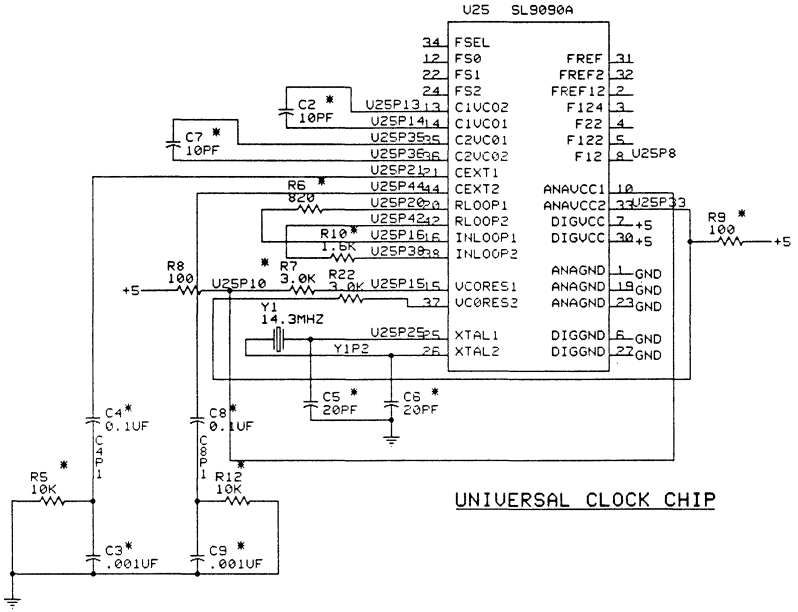


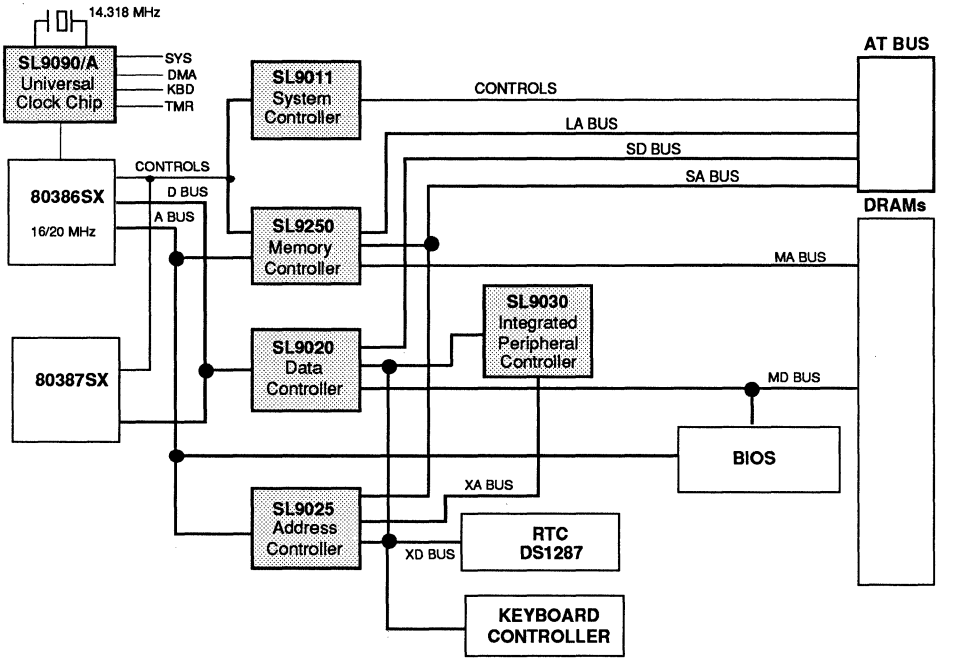

**Fig. 1**

# Evaluation

# Products

## FEATURES

- 80386SX based PC/AT Motherboard Design.
- 16 / 20 MHz, Fast Page Mode.
- 100% IBM PC/AT Compatible.
- VIA FlexSet Chips.
- 80387SX Numeric Coprocessor Support.
- AMI, Award, Phoenix or Quadtel BIOS.
- Switchable Shadow RAM Feature.
- 512K (Min) to 8M (Max) On Board Memory.
- Uses SIMMs 256Kx1, 256Kx4 and 1Mx1 DRAMs or a Mix.
- Works with Page Mode or Static Column DRAMs.
- Selectable Wait States for Slower DRAMs. 100 ns DRAMs for 16 MHz Operation and 80 ns DRAMs for 20 MHz Operation.
- Provide 640Kb / 384Kb Memory Configuration.
- Switchable Clock Speed using Hardware or Keyboard Controls.
- I/O Bus Decoupling to Ensure Compatibility at All Speeds.
- Keyboard Lock, Turbo and Power On LED connectors.
- Speaker and Keyboard Connectors.
- 8 Expansion Slots: 6) 16-bit Slots; 2) 8-bit Slots.
- Baby AT Size (8.5 X 13 inches); 4 Layer P.C. Board.




## FlexAT/386SXP Block Diagram

SL9011 System Controller: The SL9011 integrates all the PC/AT System control logic including clock switching and reset logic. It also contains a programmable wait state and command delay for external memory and I/O commands.

SL9020 Data Controller: The SL9020 provides a fast Data In to Data Out throughput time of 15ns with 24mA buffers for the MD, SD and XD busses for the 16 bit data bus.

SL9025 Address Controller: The SL9025 provides a fast Address In to Address Out Time of 15 ns, with 24 ma buffers for SA and XA busses. It also has the necessary refresh for 256 Kb and/or 1Mb DRAMs.

SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design except the keyboard controller and RTC. It is fully compatible with the VLSI 82C100.

SL9250 Page Mode Memory Controller: The SL9250 supports up to 8M on board memory with any combination of 256K X 1, 256K X 4 or 1M X 1 DRAM. It also includes a built in shadow RAM feature.

SL9090/A Universal PC/AT Clock: The SL9090/A generates all the essential PC/AT clock signals using only one 14.3 MHz crystal. Output frequencies form 16 to 66 MHz are programmable and designed to be switched dynamically.

## DESCRIPTION

**CLOCK SWITCHING**

VIA's unique clocking scheme allows an user to upgrade a 16 MHz system to 20 MHz by simply changing the jumper pin on J1. In addition, dynamic switching from 16 MHz or 20 MHz to 8 MHz, during an I/O cycle, is provided through hardware or keyboard control on J3.

**SELECTABLE WAIT STATES**

VIA's FlexAT/386SXP is a page mode memory design. All memory accesses within a 2K/4K page provides a zero wait state operation.

For the highest performance, use the wait state option where both the memory read and write miss results in 1 wait state operation. Proper DRAM for this option is 100 ns for 16 MHz and 80 ns for 20 MHz.

On board memory wait states are programmable (SW1) to allow usage of slower DRAMs. For example a 20 MHz system can operate using 2 wait states using 100 ns DRAMs and a 16 MHz system with 120 ns DRAMs.

**MEMORY TYPE AND SIZE**

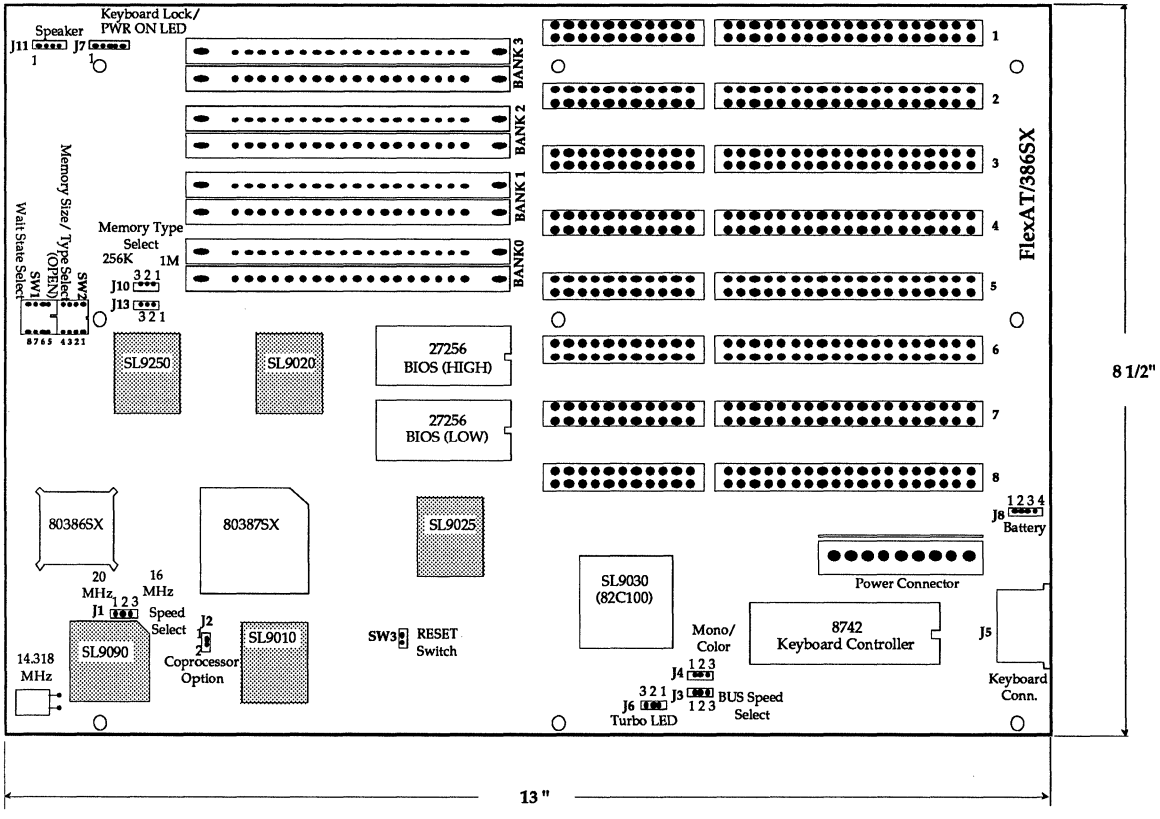
All 4 banks can use 256K or 1M DRAMs. Refresh and address decoding are provided for various memory types and mixes by On Board Jumbers J10, J13 and SW2.

Using 256K DRAMs the banks can be selectively populated to get 512K, 1M, 1.5M, or 2M total on board memory. Using 1M chips will give 2M, 4M, 6M, or 8M total memory. A mix can also be used. 384Kb of memory space between 640K and 1M is remapped at the top of the total memory space.

**SHADOW RAM FEATURE**

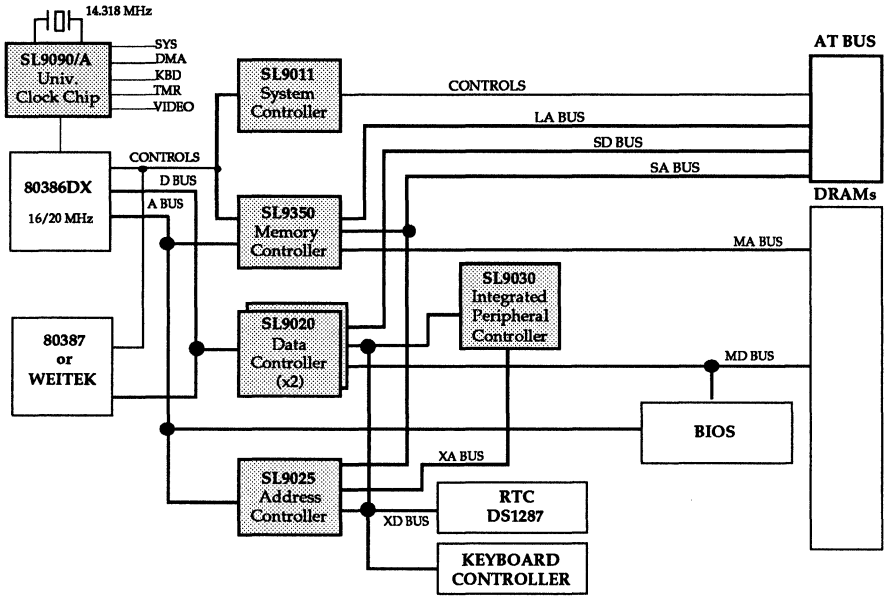
128K of memory space (ROM) just below 1M is remapped into RAM to provide the shadow RAM option. This feature is operational only with a BIOS designed for shadow RAM operations. Switch SW1-(6) labelled KSH will enable shadow RAM when switch is on and visa versa. Once SW1-(6) is set, the shadow RAM is keyboard controlled.

# VIA Technologies 80386SX-based PC/AT design



## FEATURES

- 80386DX based PC/AT Motherboard Design.
- 16 / 20 MHz, Fast Page Mode.
- 100% IBM PC/AT Compatible.
- VIA FlexSet™ Chips.
- 80387DX or Weitek Numeric Coprocessor Support.
- AMI, Phoenix, Award or Quadtel BIOS.
- Switchable Shadow RAM Feature.
- 1M (Min) to 16M (Max) On Board Memory.
- Uses either 256Kb or 1M DRAM SIMMs or a Mix.
- Uses either Page Mode or Static Column DRAMs.
- Selectable Wait States for Slower DRAMs. 100 ns DRAMs for 16 MHz and 80 ns DRAMs for 20 MHz Operation.
- 640Kb / 384Kb Memory Configuration.
- Switchable Clock Speed using Hardware or Keyboard Controls.
- I/O Bus Decoupling to Ensure Compatibility at All Speeds.
- Keyboard Lock, Turbo and Power On LED Connectors.
- Speaker and Keyboard Connectors.
- 8 Expansion Slots; 6) 16-bit Slots and 2) 8-bit Slots.
- Baby AT Size (8.5 X 13 inches) 6 Layer PC Board.




## FlexAT/386DXP™ Block Diagram

SL9011 System Controller: The SL9011 integrates all the PC/AT System control logic including clock switching and reset logic. It also contains a programmable wait state and command delay for external memory and I/O commands.

SL9020 Data Controller: The SL9020 provides a fast data in to data out throughput time of 15ns with 24mA buffers, with latches, for the MD, SD and XD busses. An 80386DX based system, 32 bit data bus, uses two SL9020 data controllers.

SL9025 Address Controller: The SL9025 provides a fast address in to address out throughput time of 15 ns with 24 ma buffers for SA and XA busses. It also provides the neccessary refresh for 256 Kb and/or 1Mb DRAMs.

SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design except the keyboard controller and RTC. It is fully compatible with the VLSI 82C100.

SL9350 Page Mode Memory Controller: The SL9350 supports up to 16M on board memory with any combination of 256K X 1, 256K X 4 or 1M X 1 DRAM. It also includes a built in shadow RAM feature.

SL9090/A Universal PC/AT Clock: The SL9090/A generates all the essential PC/AT clock signals using only one 14.3 MHz crystal. Output frequencies form 16 to 66 MHz are programmable and designed to be switched dynamically.

## DESCRIPTION

**CLOCK SWITCHING**

VIA's unique clocking scheme allows the user to upgrade from a 16 MHz to a 20 MHz or to 25 MHz system by simply changing the jumper selections on J17, J22 and J23. In addition, dynamic switching from selected bus operating frequency to 8MHz during an I/O cycle is provided through hardware or keyboard control on J11.

**SELECTABLE WAIT STATES**

VIA's FlexAT/386DXP is a page mode memory design. All memory accesses within the same 2Kb/4Kb page result in zero wait state operation.

For highest performance, use the wait state option where both the memory read and the write miss result in 1 wait state operation. Proper DRAM selection for this mode is 80 ns for 16 MHz or 60ns for 20 MHz.

For lower costs systems, on board memory wait states are programmable (SW1) to allow usage of slower DRAMs. For example, a 20 MHz system can operate with 2 wait states when using 80ns DRAMs or 100ns for 16 MHz.

**MEMORY TYPE AND SIZE**

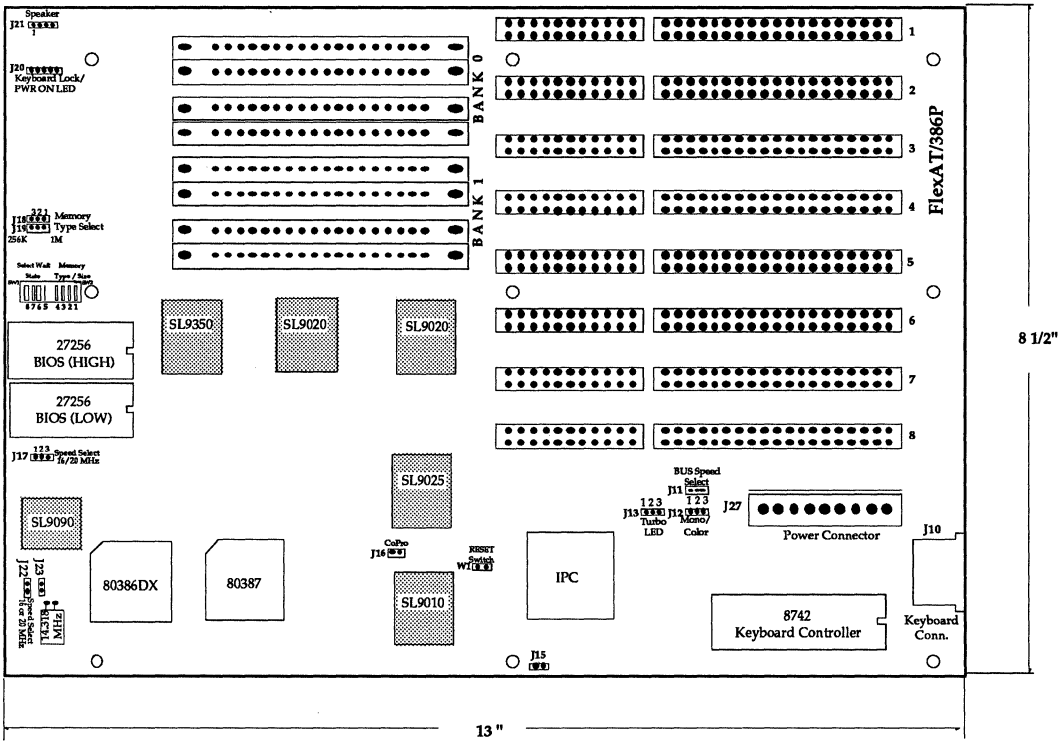
Both banks can use 256Kb or 1M DRAMs. Refresh and address decoding is provided for various memory types and mixes by on board jumpers J18, J19 and SW2.

Using 256K DRAMs the banks can be selectively populated to get 1M or 2M total on board memory. Using 1M chips will give 4M or 8M total memory. The 384Kb of memory space between 640Kb and 1M is remapped at the top of the total memory space.

**SHADOW RAM FEATURE**

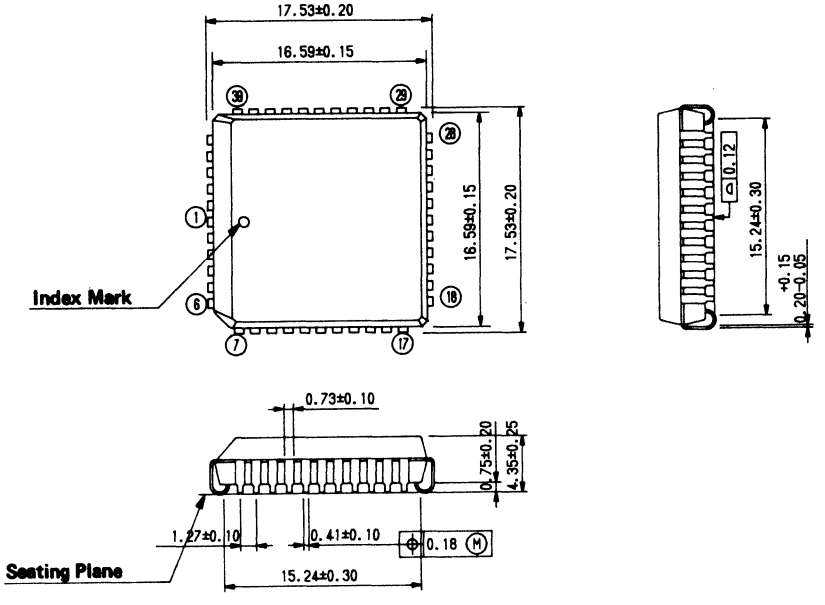
128Kb of memory space (ROM) just below 1M is remapped into RAM to provide shadow RAM option. This can also be disabled.

# VIA Technologies 80386DXP PC/AT Evaluation Board



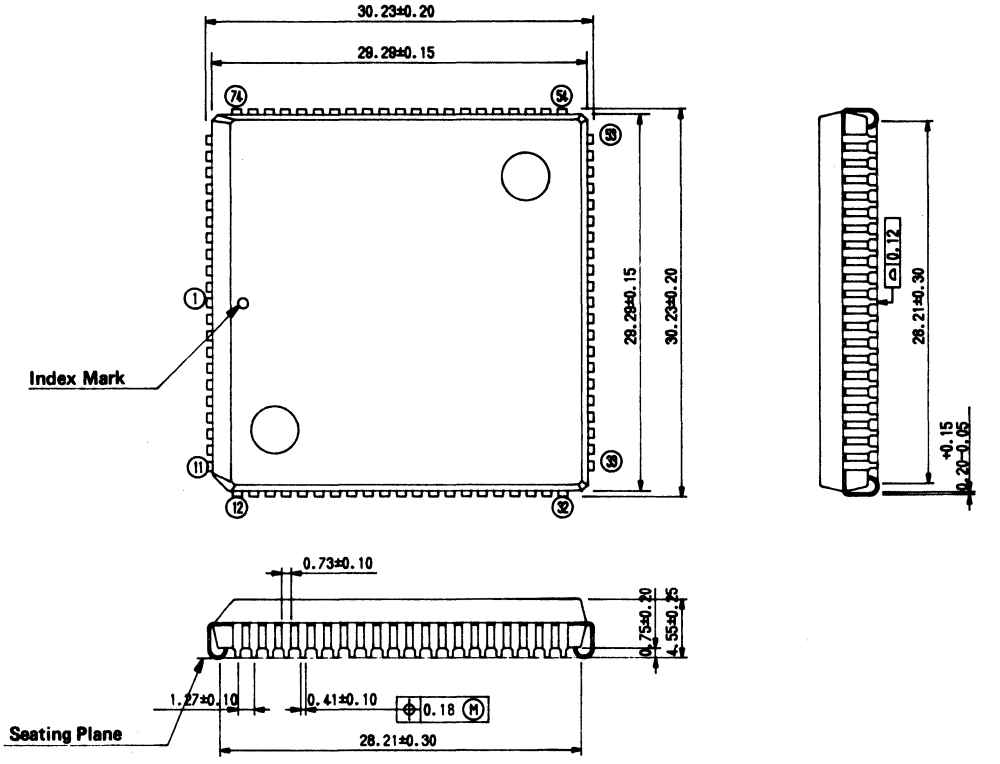
PACKAGE OUTLINES

# 44-Pin Plastic Leaded Chip Carrier



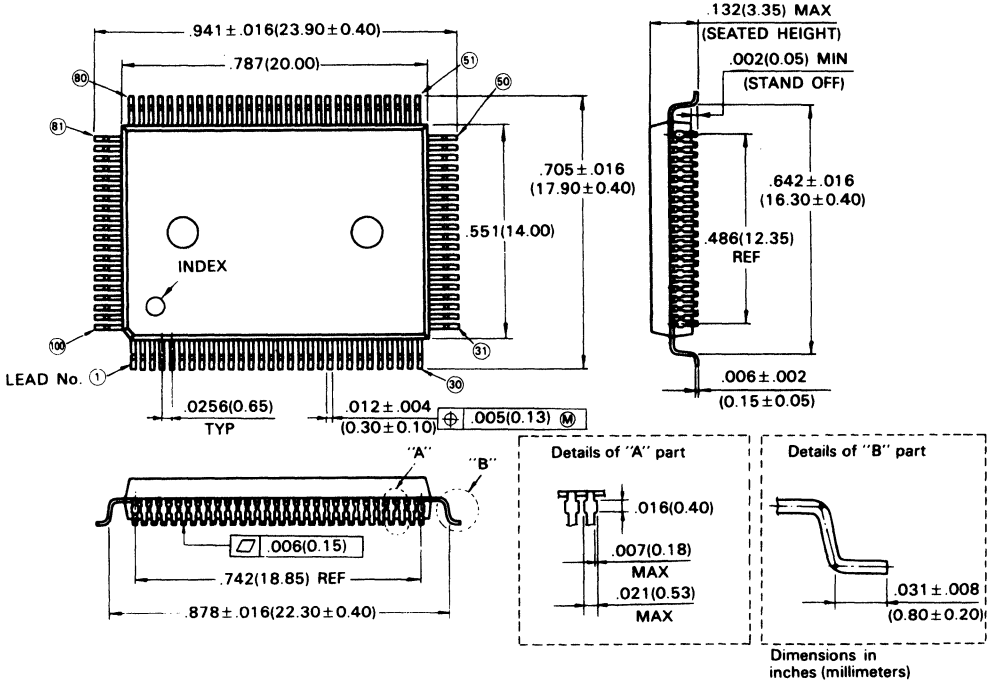
PACKAGE OUTLINES, Cont'd

# 84-Pin Plastic Leaded Chip Carrier



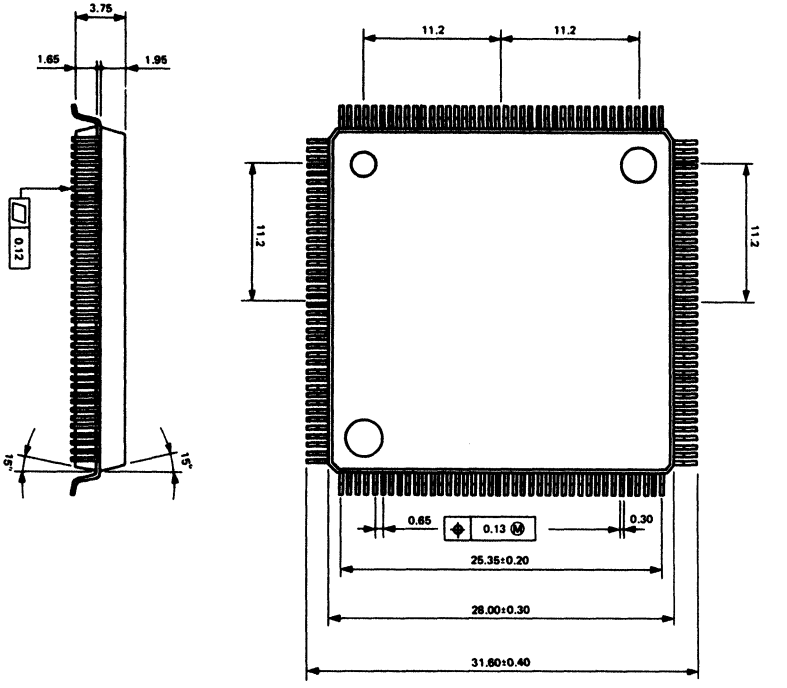
PACKAGE OUTLINES, Cont'd

# 100-Pin Plastic Flatpack



PACKAGE OUTLINES, Cont'd

# 160-Pin Plastic Flatpack



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