UNIVERSAL PC/AT CLOCK CHIP
SL9090A

PRELIMINARY

FEATURES

- Generates all Essential Clock Signals for P.C.'s.
- Supports 8086/8088/80286/80386SX/80386DX/80486-based designs.
- Clock Options of 66, 50, 48, 40, 32, 24 MHz and Others.
- Facilitates FCC approval by reducing EMR.
- Requires Only One Crystal and a Few RC Components.
- Two Independent Clock Generators.
- Glitch Free Switching for both Clock Generators.
- All Outputs Capable of 8 mA Drive.
- Advanced Bipolar Technology.

DESCRIPTION SL9090A

The SL9090A is a Universal Clock Chip capable of generating all essential clock signals that are used in a typical P.C. design. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs. The outputs of this clock chip are programmable through the keyboard and also by jumper settings. Clock options of 66 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz 24 MHz and their multiples are available, giving flexibility to the user.

Frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. FSEL is used to control the system I/O bus clock. During a CPU cycle the FSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the FSEL goes low and fixed frequencies of 32 MHz, 16 MHz and 8 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pin F124 guaranties the add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock, by connecting the FSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the FSEL signal to be controlled through the keyboard by pressing "CTL ALT +" or "CTL ALT-".

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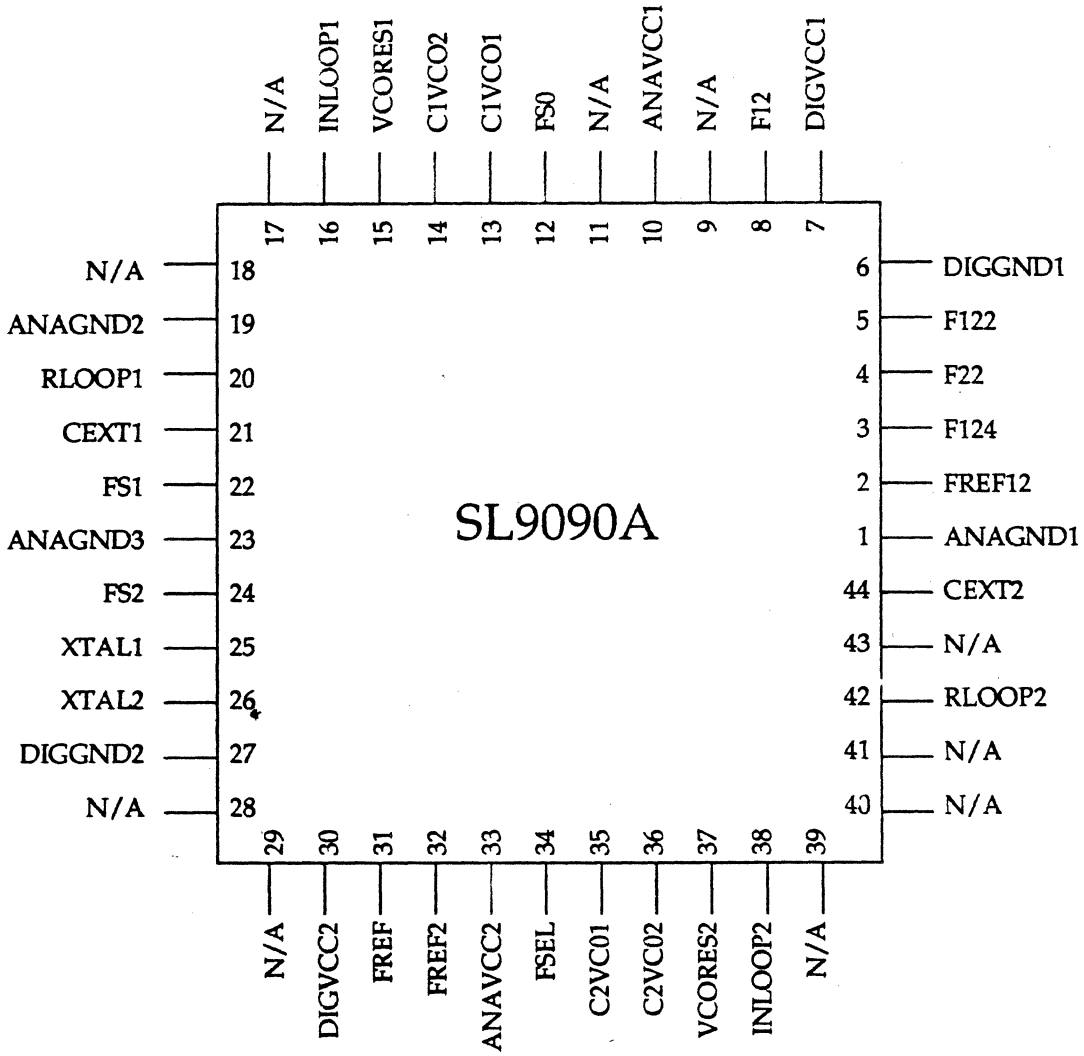
PINOUT


SL9090A
1 ANAGND1
2 FREF12
3 F124
4 F22
5 F122
6 DIGGND1
7 DIGVCC1
8 F12
9 N/A
10 ANAVCC1
11 N/A
12 FS0
13 C1VCO1
14 C1VCO2
15 VCORES1
16 INLOOP1
17 N/A
18 N/A
19 ANAGND2
20 RLOOP1
21 CEXT1
22 FS1
23 ANAGND3
24 FS2
25 XTAL1
26 XTAL2
27 DIGGND2
28 N/A
29 N/A
30 DIGVCC2
31 FREF
32 FREF2
33 ANAVCC2
34 FSEL
35 C2VC01
36 C2VC02
37 VCORES2
38 INLOOP2
39 N/A
40 N/A
41 N/A
42 RLOOP2
43 N/A
44 CEXT2

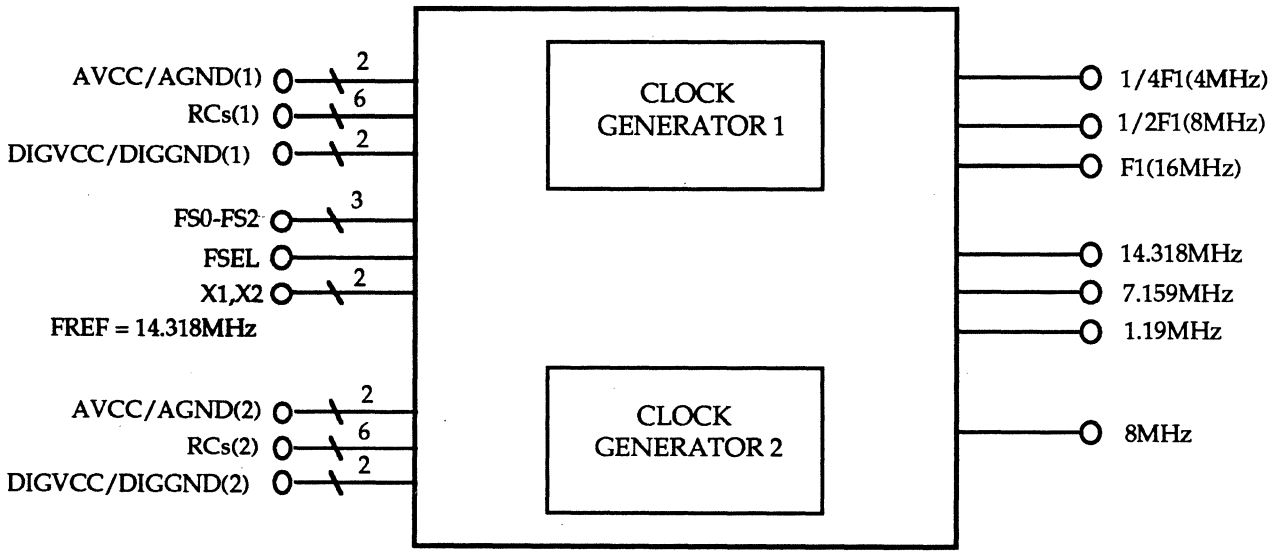
DESCRIPTION (Cont'd)

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. This frequency is divided by 2 internally and 7.159 MHz is supplied to the output through the FREF2 pin for the keyboard controller. The FREF12 pin has an output of 1.19 MHz and is used by the timer1 (8254) in the peripheral controller for refresh. All outputs are capable of 8mA drive.

The SL9090A consists of two independent Voltage controlled Oscillators (VCOs) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9090A. Phase difference between this reference frequency and that generated by the VCOs are tracked by phase sensitive detectors. This becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCOs. The output from the VCOs are divided to generate the appropriate outputs.

The SL9090A is designed, using advanced Bipolar technology and is available in a 44 pin PLCC. It requires only one crystal (14.3 MHz) and a few RC components to generate all the essential clocks that are required for a P.C. design. As there is only one crystal on the system board, the Electro Magnetic Radiation is reduced significantly facilitating FCC approval. This makes the SL9090A an ideal low cost solution with capabilities for universal applications.

FUNCTIONAL BLOCK DIAGRAM SL9090A



PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
ANAGND1,2,3	1,19,23	-	Analog Ground.
ANAVCC1,2	10,33	-	Analog VCC for Clock generator 1,2.
C1VCO1,2	13,14	I	VCO capacitor pin 1, 2 for Clock generator 1.
C2VCO1,2	35,36	I	VCO capacitor pin 1, 2 for Clock generator2.
CEXT1,2	21,44	I	Charge pump pin for Clock generator 1,2.
DIGGND1,2	6,27	-	Digital Ground.
DIGVCC1,2	7,30	-	Digital +5V supply.
F22	4	O	16 MHz output.
F12	8	O	F1 or F2 (32 MHz) output.
F122	5	O	F1/2 or F2 (16 MHz) output.
F124	3	O	F1/4 or F2 (8 MHz) output.
FREF	31	O	14.318 MHz output.
FREF2	32	O	7.159 MHz output (Keyboard clock).
FREF12	2	O	1.19 MHz output (Timer clock).
FS0-FS2	12,22,24	I	Frequency Select (from Keyboard or Jumpers) as shown in Table 1.
FSEL	34	I	Frequency Select input (Dynamic). When FSEL is 1, F1 is selected. When it is 0, F2 is selected.
INLOOP1,2	16,38	I	Loop filter resistor pin 1 for Clock generator 1,2.
N/C	9,11,17,18,28, 29,39,40,41,43	-	No Connection.
RLOOP1,2	20,42	I	Loop filter resistor pin 2 for Clock generator 1,2.
VCORES1,2	15,37	I	Center frequency resistor for Clock generator 1,2.
XTAL1,2	25,26	X1,X2	Crystal oscillator pin 1,2.

FREQUENCY SELECT CODES

PIN NAME	FSEL	FS2	FS1	FS0	F12	F122	F124	F2	F22	
PIN No.	34	24	22	12	8	5	3	-	4	
FUNCTION					(F1,F2)	$\frac{(F1,F2)}{2}$	$\frac{(F1,F2)}{4}$	(F2)	$\frac{(F2)}{2}$	UNIT
	1	0	0	0	48	24	12	32	16	MHz
	1	0	0	1	50	25	12.5	32	16	MHz
	1	0	1	0	24	12	6	32	16	MHz
	1	0	1	1	66	33	16.5	32	16	MHz
	1	1	0	0	32	16	8	32	16	MHz
	1	1	0	1	40	20	10	32	16	MHz
	0	X	X	X	32	16	8	32	16	MHz

Table 1

PIN NAME	FREF	FREF2	FREF12	
PIN No.	31	32	2	
FUNCTION	(FREF)	$\frac{(FREF)}{2}$	$\frac{(FREF)}{12}$	UNIT
	14.318	7.159	1.19	MHz

Table 2

NOTES:

1. FS0, FS1, FS2, & FSEL can all be switched dynamically.
2. FSEL switching response time is less than 2X F1 clock cycles.
3. FS0, FS1 & FS2 switch occurs within 1 µs to 10% of selected frequency.

DC CHARACTERISTICS SL9090A

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Parameters	Symbol	Min.	Max.	Units	Conditions
Low Level Input Voltage	VIL (TTL)	0	0.8	V	
Low Level Input Current	IIL (TTL)		-0.6	mA	Vin = 0.4V
High Level Input Voltage	VIH (TTL)	2.0	5.25	V	
High Level Input Current	IIH (TTL)		10	mA	Vin = DIGVCC
Low Level Output Voltage	VOL1 (TTL)		0.5	V	Iol = 8mA
High Level Output Voltage	VOH1 (TTL)	2.4		V	Ioh = -400 µA
Low Level Output Voltage (Low power TTL)	VOL2 (FREF)		0.5	V	Iol = 16mA
High Level Output Voltage (Low power TTL)	VOH2 (FREF)	2.4		V	Ioh = -2mA
Supply Current	ICC	140	210	mA	All pins floating

NOTES

1. Thermal resistance of package = 66° C/W.
2. Calculated worst case tpd factor = 1° 81.
3. Calculated max junction temp = 117° C.

AC CHARACTERISTICS SL9090A

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

XTAL1, XTAL2, Crystal frequency.....14.318 MHz

F12, F122 Duty Cycle.....43:57 - 57:43
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

F2, F22, FREF, FREF2, FREF12 duty Cycle.....40:60 - 60:40
(Load 2 LSTTL inputs, External resistor may be required to achieve duty cycle close to 50%.)

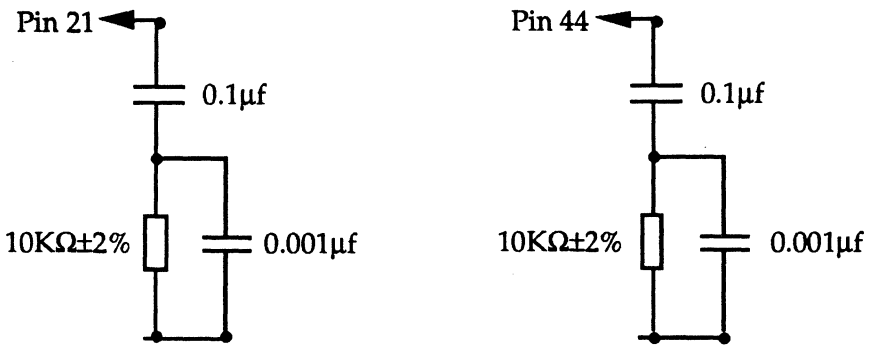
Settling time from change of FS1, FS2, FS3.....1uS to +/- 10% of defined frequency.
(300uS to lock.)

EXTERNAL COMPONENTS

Description	Name	Clock Generator 1	Clock Generator 2
Shunt Regulator	(RSHUNT)	100Ω±2%	100Ω±2%
Center frequency resistor	(VCORES)	3.0K±1%	3.0K
Loop filter resistor	(RLOOP - INLOOP)	820Ω±1%	1.6K±1%
VCO Capacitor	(CVCO1 - CVCO2)	10pf±0.5pf	10pf±0.5pf

Table 3

Charge Pump Components (CEXT) Connected as follows:



APPLICATION INFORMATION

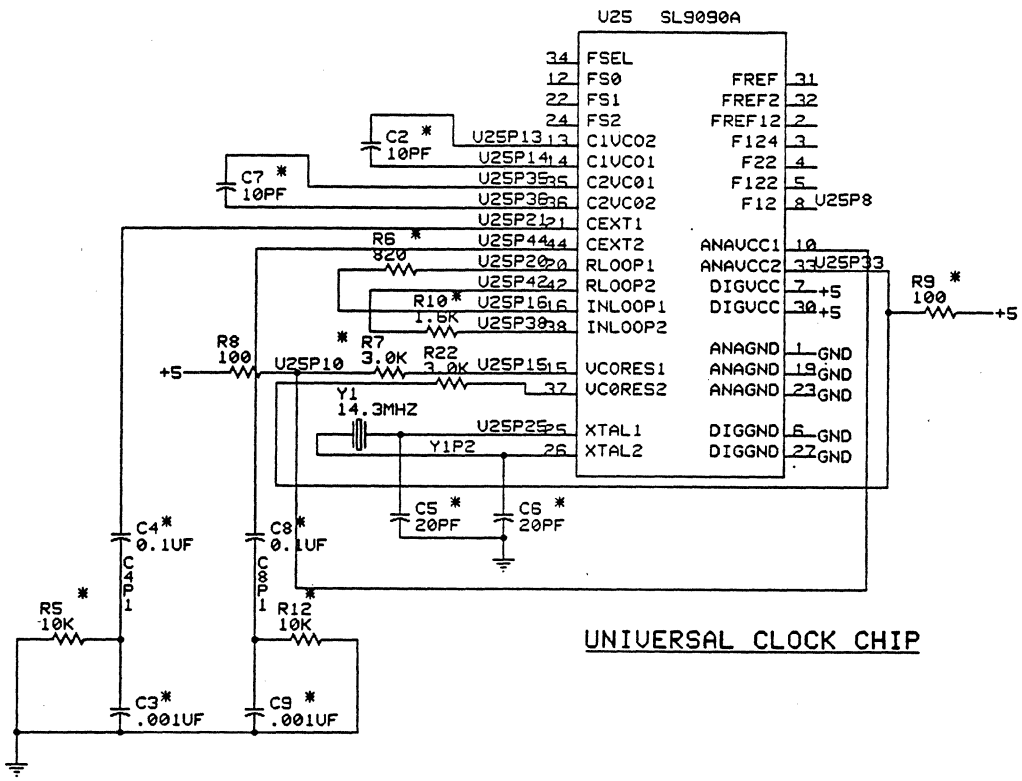


Fig. 1

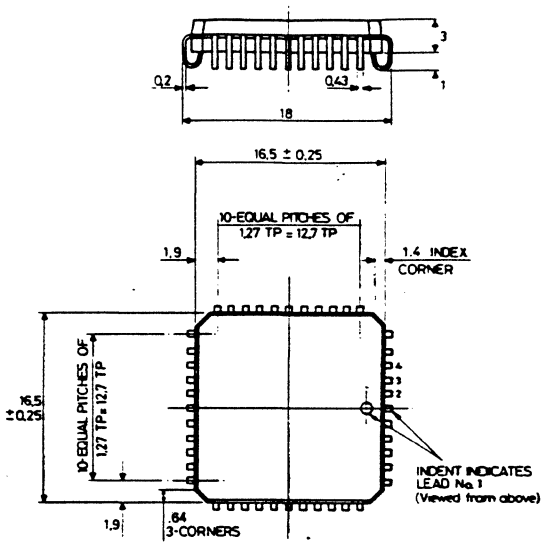
UNIVERSAL PC/AT CLOCK CHIP

SL9090A

PRELIMINARY

Package Information

44 Pin Plastic Leadless Chip Carrier



ORDERING INFORMATION

Device Type:
SL9090A

Package Type:
PL- Plastic LCC

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL9090A XX X

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