SL9092
SYSTEM CLOCK CHIP

PRELIMINARY

FEATURES

- Generates all Essential Clock Signals for All-In-One Motherboards and Laptops.
- Supports 8086/8088/80286/80386SX/80386DX/80486-based Designs.
- Frequency Options of 66, 64, 50, 48, 40, 32, 24 MHz and Others.
- Integrates Floppy Drive, Serial Port and Keyboard Controller Clocks On-chip.
- Single Crystal Expedites FCC Approvals by Reducing EMR.
- Two Independent Clock Generators.
- Fast Rise and Fall Times.
- Glitch Free Switching for Both Clock Generators.
- Extremely Stable Frequencies.
- Switchable Clock Rates, Even After Board Manufacturing.
- One Percent Duty Cycle Tolerance.
- All Outputs Capable of 12 mA Drive.
- Advanced Low Power CMOS Technology.
- 44 Pin PLCC.

May, 1991
4.053191

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Sunnyvale, CA 94086

DESCRIPTION SL9092

The SL9092 is a universal System Clock Chip capable of generating all essential clock signals that are used in typical PC and Notebook designs. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs. The CPUCLK outputs of this clock chip are programmable through the keyboard or by jumper settings. Clock options of 66 MHz, 64 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz, and 24 MHz are available, as well as the resultant frequencies from dividing these signals by 2 or 4, giving optimal flexibility to the user.

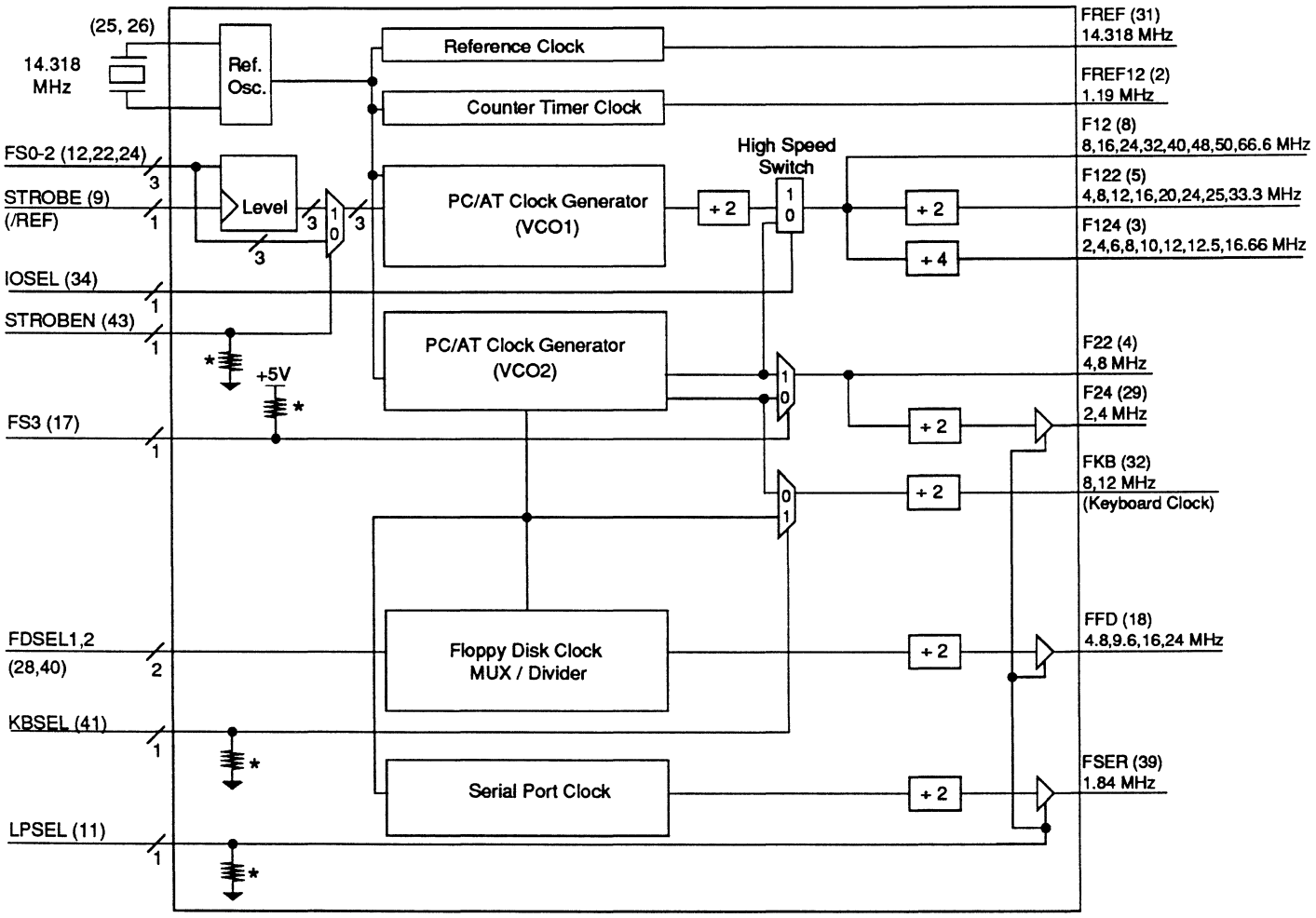
CPU frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. IOSEL is used to control the system I/O bus clock. During a CPU cycle the IOSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the IOSEL goes low and fixed frequencies of 16 MHz, 8 MHz and 4 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pin F124 guarantees add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock by connecting the IOSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the IOSEL signal to be controlled through the keyboard.

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. The FREF12 pin has an output of 1.19 MHz and is used by Timer 1 (8254) in the peripheral controller for refresh. All outputs are capable of 12mA drive.

The SL9092 consists of two independent Voltage Controlled Oscillators (VCO's) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9092. Phase differences between this reference frequency and that generated by the VCO's are tracked by phase sensitive detectors. The phase difference becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCO's. The output from the VCO's are divided to generate the appropriate outputs.

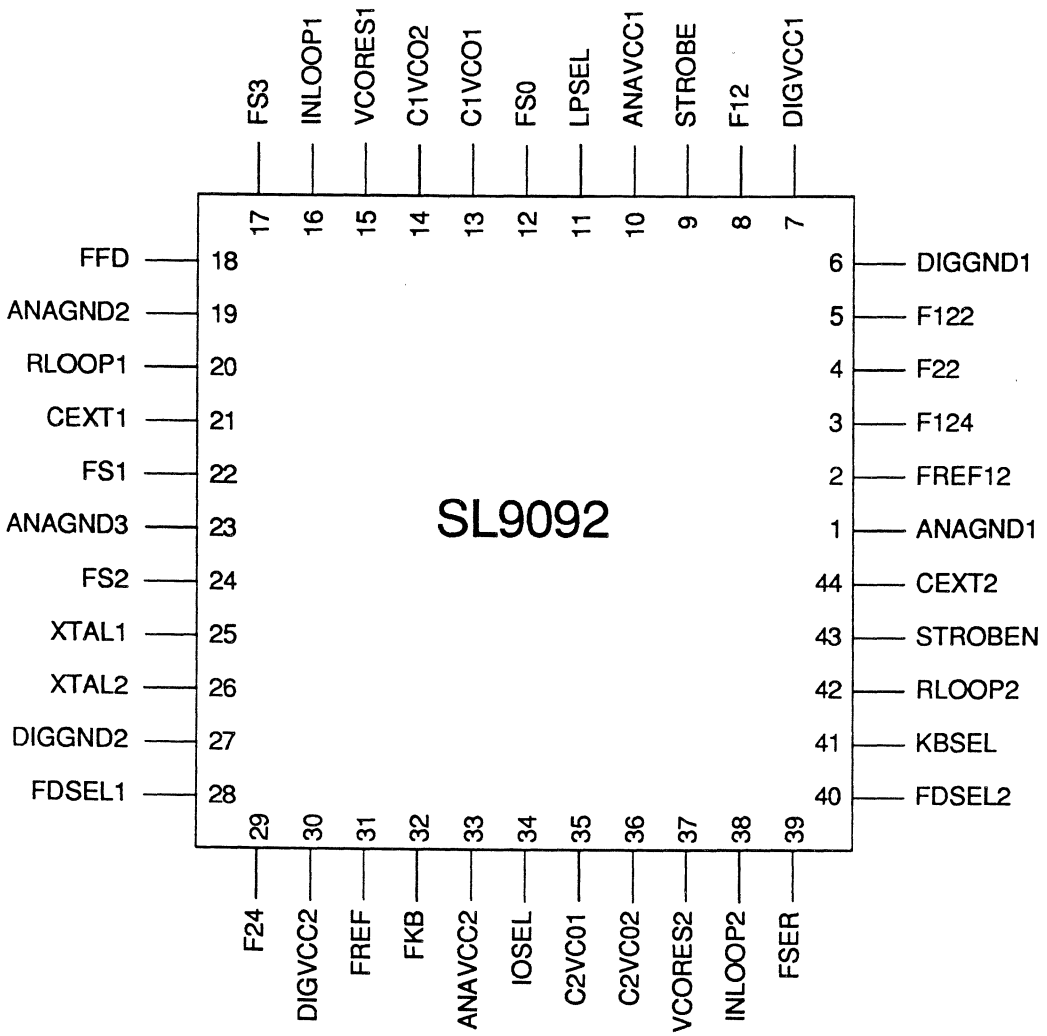
The SL9092 is designed using advanced CMOS technology and is available in a 44 pin PLCC. It requires only one crystal (14.318 MHz) and a few RC components to generate all the essential clocks that are required for PC and Notebook designs. As there is only one crystal on the system board, Electro Magnetic Radiation (EMR) is reduced significantly, facilitating FCC approval. This makes the SL9092 an ideal low cost solution with capabilities for universal system applications.

BLOCK DIAGRAM SL9092



* Pulled Up/Down in Pin Description

PINOUT


SL9092
1 ANAGND1
2 FREF12
3 F124
4 F22
5 F122
6 DIGGND1
7 DIGVCC1
8 F12
9 STROBE
10 ANAVCC1
11 LPSEL
12 FS0
13 C1VCO1
14 C1VCO2
15 VCORES1
16 INLOOP1
17 FS3
18 FFD
19 ANAGND2
20 RLOOP1
21 CEXT1
22 FS1
23 ANAGND3
24 FS2
25 XTAL1
26 XTAL2
27 DIGGND2
28 FDSEL1
29 F24
30 DIGVCC2
31 FREF
32 FKB
33 ANAVCC2
34 IOSEL
35 C2VC01
36 C2VC02
37 VCORES2
38 INLOOP2
39 FSER
40 FDSEL2
41 KBSEL
42 RLOOP2
43 STROBEN
44 CEXT2

SL9092 PIN DESCRIPTIONS

SYMBOL	PIN	TYPE	DESCRIPTION
ANAGND1,2,3	1,19,23	-	Analog Ground.
ANAVCC1,2	10,33	-	Analog VCC for Clock generator 1,2.
C1VCO1,2	13,14	I	VCO capacitor pin 1, 2 for Clock generator 1.
C2VCO1,2	35,36	I	VCO capacitor pin 1, 2 for Clock generator2.
CEXT1,2	21,44	I	Charge pump pin for Clock generator 1,2.
DIGGND1,2	6,27	-	Digital Ground.
DIGVCC1,2	7,30	-	Digital +5V supply.
F12	8	O	F1 (24, 40, 48, 50, 64, 66 MHz) if IOSEL = 1. F2 (8,16 MHz) if IOSEL = 0.
F122	5	O	F12 divide by 2.
F124	3	O	F12 divide by 4.
F22	4	O	4 or 8 MHz output.
F24	29	O	F22 frequency divide by 2.
FFD	18	O	Floppy disk frequencies 4.8, 9.6, 16, or 24 MHz available at this pin depending on FDSEL1 and FDSEL2.
FREF	31	O	14.318 MHz output for ATbus video clock.
FKB	32	O	8 or 12 MHz output (Keyboard clock).
FREF12	2	O	1.19 MHz output (Timer clock).
FS0-FS2	12,22,24	I	Frequency Select (from Keyboard or Jumpers) as shown in Table 1.
FS3	17	I	Selects F22 frequency to be 16 or 8 MHz.
FDSEL 1, 2	28, 40	I	Floppy disk frequency select pins.
KBSEL	41	I	Keyboard clock frequency select pin. 8 MHz selected when low, 12 MHz when high.
IOSEL	34	I	Frequency Select input used for input/output operations (Dynamic). When IOSEL is 1, F1 is selected. When it is 0, F2 is selected.

SL9092 PIN DESCRIPTIONS Cont'd

SYMBOL	PIN	TYPE	DESCRIPTION
FSER	39	O	Serial Port frequency: 1.8461 MHz.
INLOOP1,2	16,38	I	Loop filter resistor pin 1 for Clock generator 1,2. Both pins should also be tied to ground through .001µF capacitors.
LPSEL	11	I	Low power input. Forces loop 2, Floppy and Serial Clocks to be disabled when low.
RLOOP1,2	20,42	I	Loop filter resistor pin 2 for Clock generator 1,2.
STROBE	9	I	Refresh strobe pin.
STROBEN	43	I	Enable pin for the strobe. Strobe latch in picture when high, bypassed when low.
VCORES1,2	15,37	I	Center frequency resistor for Clock generator 1,2.
XTAL1,2	25,26	X1,X2	Crystal oscillator pin 1,2.

FS0 (12)	FS1 (22)	FS2 (24)	FS3 (17)	IOSEL (34)	F12 (8)	F122 (5)	F124 (3)
0	0	0	X	1	48 MHz	24 MHz	12 MHz
0	0	1	X	1	50 MHz	25 MHz	12.5 MHz
0	1	0	X	1	24 MHz	12 MHz	6 MHz
0	1	1	X	1	66 MHz	33 MHz	16.5 MHz
1	0	0	X	1	32 MHz	16 MHz	8 MHz
1	0	1	X	1	40 MHz	20 MHz	10 MHz
1	1	0	X	1	64 MHz	32 MHz	16 MHz
1	1	1	X	1	32 MHz	16 MHz	8 MHz
X	X	X	1	0	16 MHz	8 MHz	4 MHz
X	X	X	0	0	8 MHz	4 MHz	2 MHz

Table 1 CPU Clock Outputs/Selection

FS3 (17)	F22 (4)	F24* (29)
1	8 MHz	4 MHz
0	4 MHz	2 MHz

*Output can be disabled using LPSEL input.

Table 2 I/O Clock Frequency Selection

FDSEL1 (28)	FDSEL2 (40)	FFD* (18)
0	0	4.8 MHz
0	1	9.6 MHz
1	0	16 MHz
1	1	24 MHz

*Output can be disabled using LPSEL input.

Table 3 Floppy Disk Frequency Selection

KBSEL (41)	FKB (32)
0	8 MHz
1	12 MHz

Table 4 Keyboard Frequency Selection

FREF (31)	FREF12 (2)	FSER* (39)
14.318 MHz	1.19 MHz	1.8461 MHz

*Output can be disabled using LPSEL input.

Table 5 Reference Frequencies

DC CHARACTERISTICS SL9092

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Parameters	Symbol	Min.	Max.	Units	Conditions
Low Level Input Voltage	VIL		0.8	V	
Input Current	IIL		±1	µA	
High Level Input Voltage	VIH	2.0		V	
Low Level Output Voltage	VOL1		0.4	V	IDL = 12 mA
High Level Output Voltage	VOH1	2.4			IOH = 12 mA
Low Level Output Voltage (Low power TTL)	VOL2		0.4		
High Level Output Voltage (Low power TTL)	VOH2	2.4			
Supply Current					
Oper	ICC		2	mA	Per MHz
Quiscent			5	µA	Inputs @ Vss or VDD

NOTES

1. Thermal resistance of package = 66° C/W.
2. Calculated worst case tpd factor = 1° 81.
3. Calculated max junction temp = 117° C.

AC CHARACTERISTICS SL9092

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

XTAL1, XTAL2, Crystal frequency.....14.318 MHz

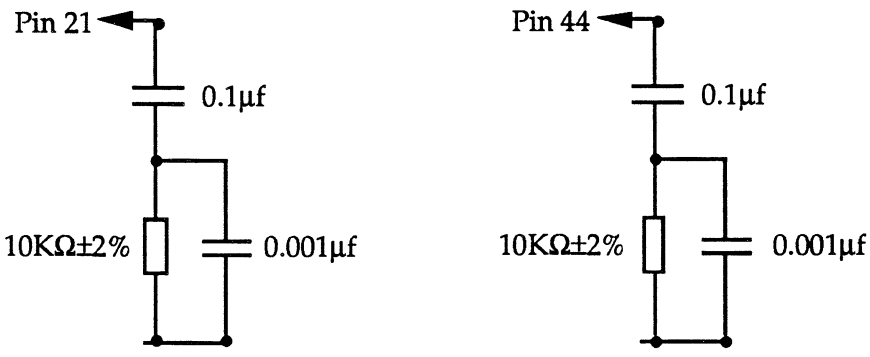
Duty Cycle (All Clock Outputs).....50% ± 1%
(Load 4 LSTTL inputs.)

Settling time from change of FS1, FS2, FS3.....1uS to +/- 10% of defined frequency.
(1ms to lock.)

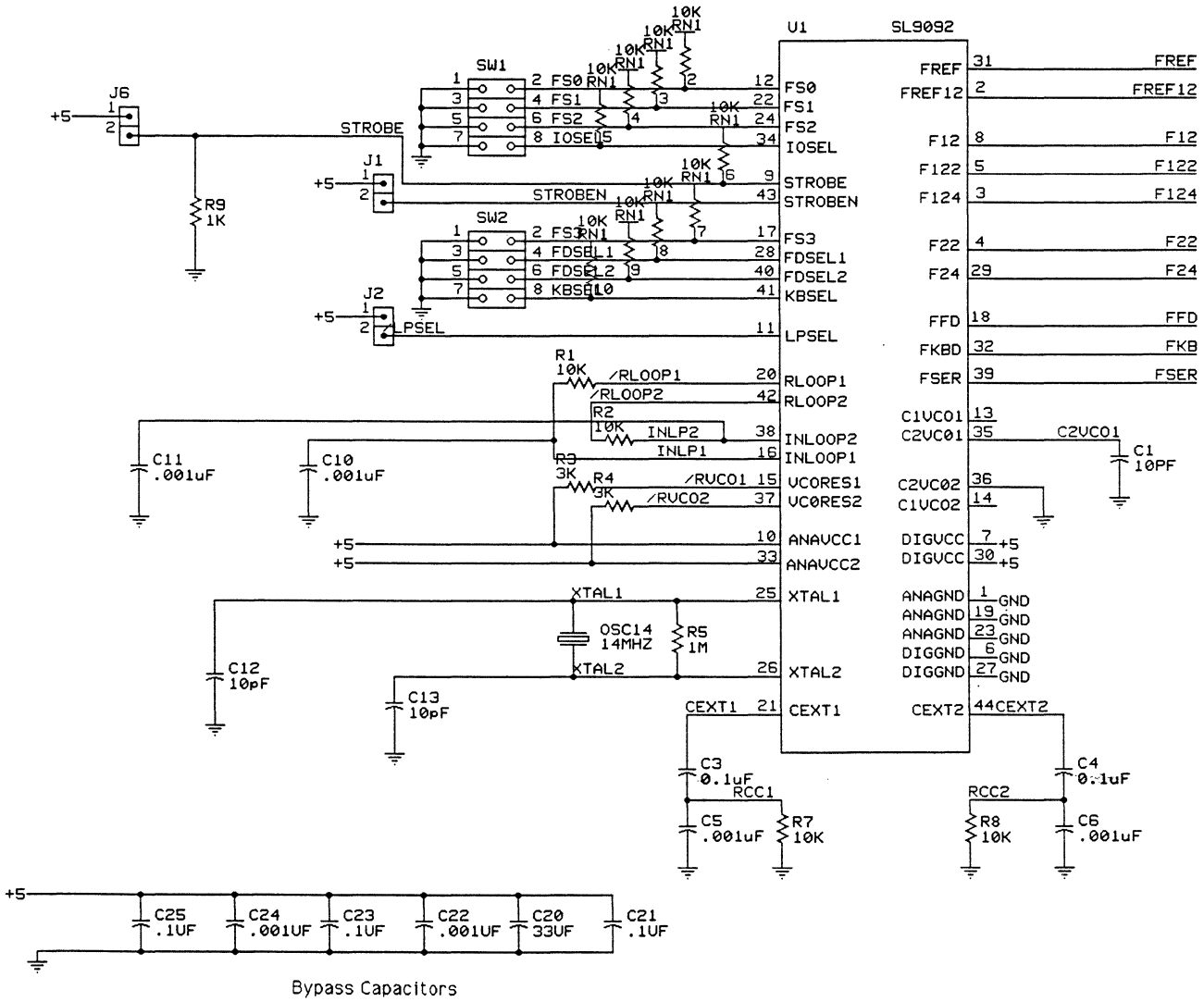
EXTERNAL COMPONENTS

Description	Name	Clock Generator 1	Clock Generator 2
Center Frequency Resistor	(VCORES)	3kΩ	3kΩ
Loop Filter Resistor	(RLOOP - INLOOP)	10kΩ	10kΩ
VCO Capacitor	C2VCO1	-	10PF

Charge Pump Components (CEXT) Connected as follows:



APPLICATION INFORMATION



Clock Circuit Connection Schematic

SL9092
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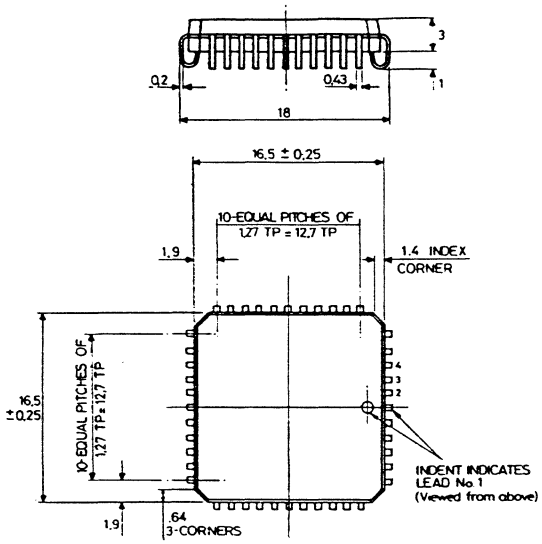
Package Information

44 Pin Plastic Leadless Chip Carrier



ORDERING INFORMATION

Device Type:
SL9092

Package Type:
PL- Plastic LCC

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL9092 XX X

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March, 1991

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