Technologies, Inc.

PRODUCT OVERVIEW

September, 1990

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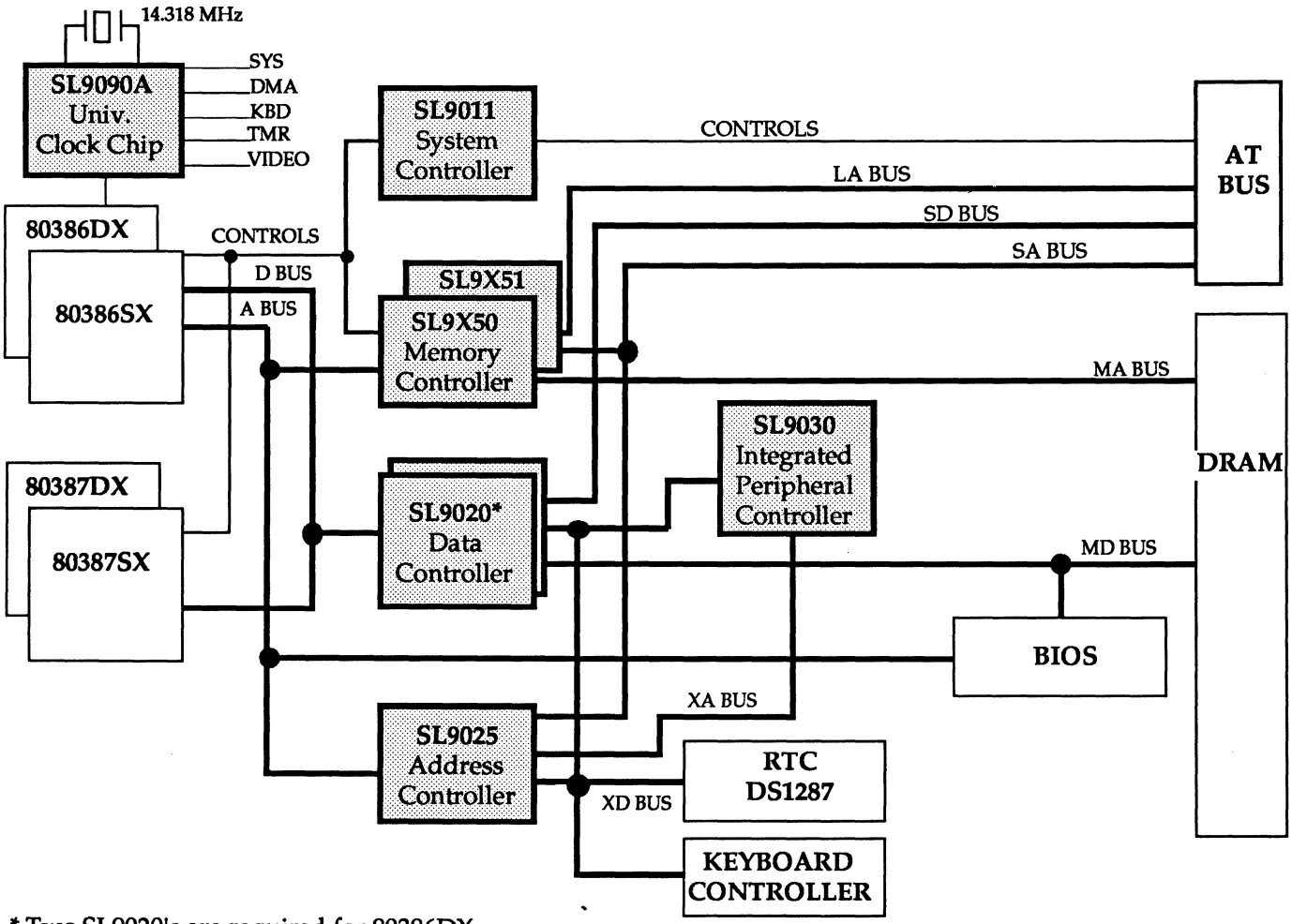
VIA Technologies
Product Overview

Flex I Products

The Flex I 100% PC/AT compatible chip set includes all of the core logic for 80386DX or 80386SX PC/AT systems. The Flex I chip set consists of the SL9011 System Controller, the SL9020 Data Controller*, the SL9025 Address Controller and the SL9X5X Memory Controller.

Detailed information on the Flex I chip set may be found in our April, 1990 Data Book. To obtain the Data Book, just call a sales representative in your area or contact VIA directly at 800-621-CHIP.



* Two SL9020's are required for 80386DX

Flex I Block Diagram

Flex II

Products

FEATURES

- 100% PC/AT Compatible.
- Up to 20 MHz Performance.
- ISA Bus Control Logic.
  - Synchronous or Asynchronous System Control Operation.
  - Programmable Command Delays.
  - Numerical Co-processor Support.
  - Programmable Wait States for Local and Off-board Cycles.
  - Fast Gate A20 and Fast Reset.
- Memory Control Logic
  - Enhanced Page Mode/2-Way Word and Multi-Page Interleave.
  - Supports up to 16M bytes of On-Board Memory.
  - Shadow RAM Feature for System, Video, LAN BIOS.
  - Can use 4M, 1M and 256K DRAMs or a mix.
  - Staggered RAS Refresh.
- Programmable Memory Options
  - User Selectable 8 or 16 bit ROM with Selectable wait states.
  - Selectable Hit (0-3) and Miss (1-4) wait states for DRAM access.
  - 512 X 512 Split.
  - Disable (On Board) Memory to 0K in 128K Resolution.
  - Memory Backfill.
  - EMS LIM 4.0 Mapping Registers
    - Up to 4 Sets of 4 Registers
    - Each Set Maps 64K Boundry
    - Each Register Maps 16K anywhere above 1M Memory
- Testability Features.
- Advanced, Low Power CMOS Technology for Laptops.
- 160 Pin Flatpack.

DESCRIPTION

VIA's System and Memory Controller SL9252, has the logic for the System Control, Memory Control, Data Control and chip select for some of the peripherals used in an AT system. The device is fully configurable via software. No external hardware jumpers are needed to utilize its features. Default values are provided to boot any system configuration. On reset, BIOS routines are used to program the device, transparent to the user, to utilize its special features.

Four configuration registers in the System Control Logic control the AT bus and peripheral bus operations. Synchronous and asynchronous bus operations are supported. In synchronous mode, bus clock is derived from the processor's CLK2. In asynchronous mode, it is derived from an independent external bus clock pin.

Support for page mode and non-page mode operation with non-interleave or word/multi-page interleave, along with programmable memory timing, allow the system designer to get maximum performance for the chosen DRAMs. High drive for RAS, CAS, memory address, and write lines are provided to connect SL9252 directly to a large DRAM memory array without external buffering. In addition, CAS for all the banks in non-interleave and 2-way interleave are provided to reduce external gates.

Shadowing features are supported in 16K granularity from 640K to 1M. Remap options allow shadowing of eight different combinations of top of memory, Local ROM, and Video ROM to 640K to 1M region.

VIA's System and Memory Controller, SL9252, can be used with VIA's SL9020 Data Controller, or with discrete latches and buffers. Data direction and enable signals for the data controller are provided for both modes of operation.

SL9252 provides decoding for Real Time Clock and Keyboard Controller, thus avoiding external decoding gates. In addition, Port B logic, PS/2 Compatible Port 92 for fast reset, and A20GATE provide the necessary logic support for a one-chip solution.

The SL9252 is logically divided into four blocks:

1. System Control Logic
2. Memory Control Logic
3. Data Control Logic.
4. Peripheral Control Logic

1. System Control Logic

The System Control Logic is divided into eight sections:

a. Clock and Reset Control
b. Hold Logic
c. Bus Control Logic
d. Coprocessor Interface
e. Ready Logic
f. Refresh Counter Logic
g. Byte Enable Generation
h. PS/2 Compatible Port 92

2. Memory Control Logic

The Memory Control Logic is logically divided into six sections:

a. Address Decode
b. HIT/MISS Detection
c. RAS/CAS Logic
d. Memory Address Generation
e. Next Address and Ready Logic
f. ROM Data Conversion Logic

3. Data Control Logic

The three major blocks of the Data Control Logic are:

a. Bus Enable Logic
b. Bus Direction and Data Conversion Logic
c. High Byte Enable Logic

4. Peripheral Control Logic

The Peripheral Control Logic provides logic for the following:

a. Peripheral Address Decoding
b. Port B Logic

BLOCK DIAGRAM SL9252

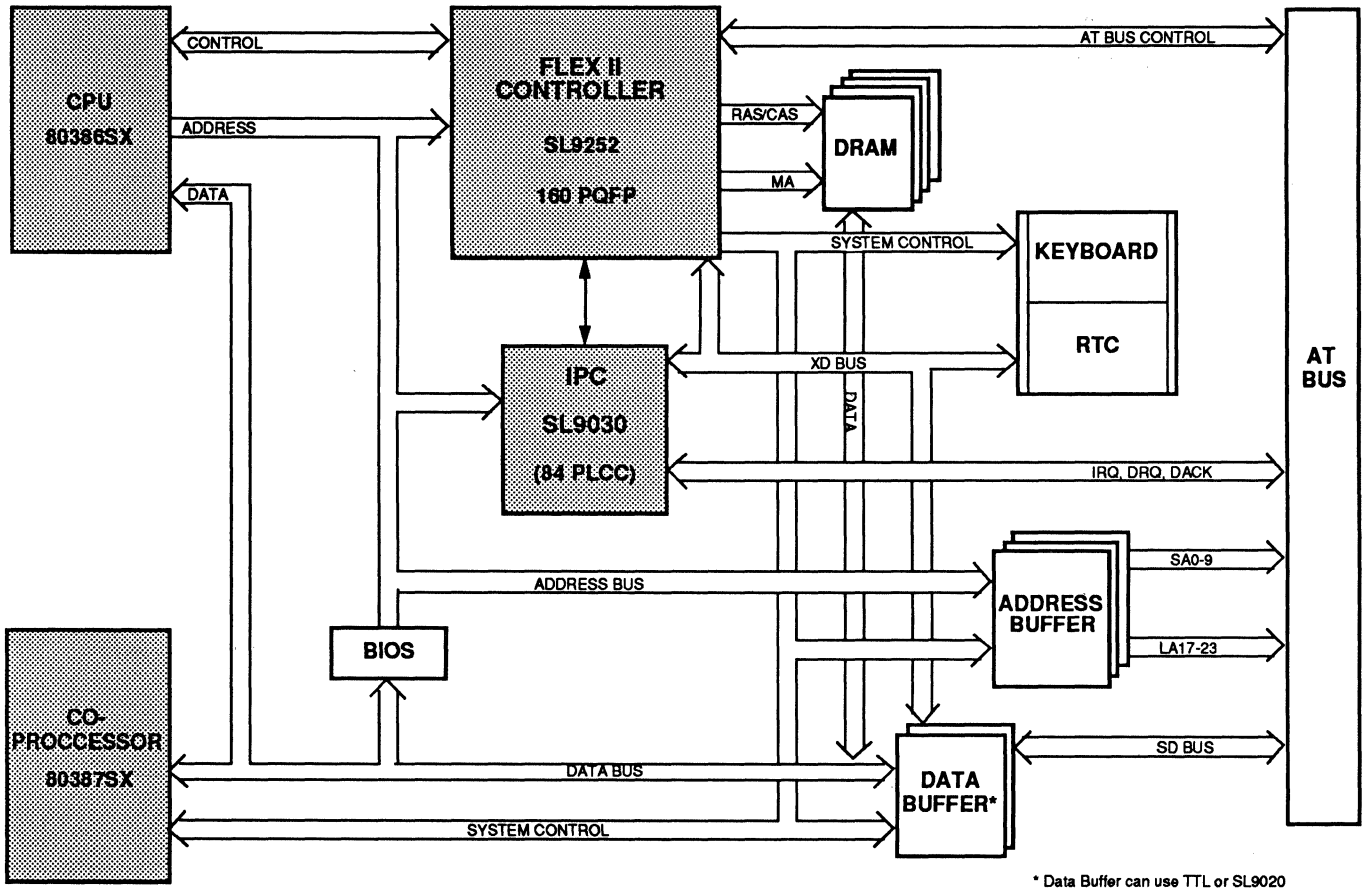


Fig. 1. Block Diagram for 80386SX CPU Board

FEATURES

- 100% PC/AT Compatible.
- Up to 20 MHz Performance.
- ISA Bus Control Logic.
  - Synchronous or Asynchronous System Control Operation.
  - Programmable Command Delays.
  - Numerical Co-processor Support.
  - Programmable Wait States for Local and Off-board Cycles.
  - Fast Gate A20 and Fast Reset.
  - IOCHRDY Timeout.
- Memory Control Logic
  - Enhanced Page Mode/2-Way Word and Multi-Page Interleave.
  - Supports up to 64M bytes of On-Board Memory.
  - Shadow RAM Feature for System, Video, LAN BIOS.
  - Can use 4M, 1M and 256K DRAMs or a mix.
  - Staggered RAS Refresh.
- Programmable Memory Options
  - User Selectable 8 or 16 bit ROM with Selectable wait states.
  - Selectable Hit (0-3) and Miss (1-4) wait states for DRAM access.
  - Mapping of Logical Banks to Physical Banks.
  - 512 X 512 Split.
  - Disable (On Board) Memory to 0K in 128K Resolution.
  - Memory Backfill.
  - EMS LIM 4.0 Mapping Registers
    - Up to 4 Sets of 4 Registers
    - Each Set Maps 64K Boundry
    - Each Register Maps 16K anywhere above 1M Memory
- Testability Features.
- Advanced, Low Power CMOS Technology for Laptops.
- 160 Pin Flatpack.

DESCRIPTION

VIA's System and Memory Controller SL9352, has the logic for the System Control, Memory Control, Data Control and chip select for some of the peripherals used in an AT system. The device is fully configurable via software. No external hardware jumpers are needed to utilize its features. Default values are provided to boot any system configuration. On reset, BIOS routines are used to program the device, transparent to the user, to utilize its special features.

Four configuration registers in the System Control Logic control the AT bus and peripheral bus operations. Synchronous and asynchronous bus operations are supported. In synchronous mode, bus clock is derived from the processor's CLK2. In asynchronous mode, it is derived from an independent external bus clock pin.

Support for page mode and non-page mode operation with non-interleave or word/multi-page interleave, along with programmable memory timing, allow the system designer to get maximum performance for the chosen DRAMs. High drive for RAS, CAS, memory address, and write lines are provided to connect SL9352 directly to a large DRAM memory array without external buffering. In addition, CAS for all the banks in non-interleave and 2-way interleave are provided to reduce external gates.

Shadowing features are supported in 16K granularity from 640K to 1M. Remap options allow shadowing of eight different combinations of top of memory, Local and Video ROM to 640K to 1M region.

VIA's System and Memory Controller, SL9352, can be used with two of VIA's SL9020 Data Controllers, or with discrete latches and buffers. Data direction and enable signals for the data controller are provided for both modes of operation.

SL9352 provides decoding for Real Time Clock and Keyboard Controller, thus avoiding external decoding gates. In addition, Port B logic, PS/2 Compatible Port 92 for fast reset, and A20GATE provide the necessary logic support for a one-chip solution.

The SL9352 is logically divided into four blocks:

1. System Control Logic
2. Memory Control Logic
3. Data Control Logic.
4. Peripheral Control Logic

1. System Control Logic

The System Control Logic is divided into eight sections:

a. Clock and Reset Control
b. Hold Logic
c. Bus Control Logic
d. Coprocessor Interface
e. Ready Logic
f. Refresh Counter Logic
g. Byte Enable Generation
h. Bus Size 16 Logic
i. PS/2 Compatible Port 92

2. Memory Control Logic

The Memory Control Logic is logically divided into six sections:

a. Address Decode
b. HIT/MISS Detection
c. RAS/CAS Logic
d. Memory Address Generation
e. Next Address and Ready Logic
f. ROM Data Conversion Logic

3. Data Control Logic

The three major blocks of the Data Control Logic are:

a. Bus Enable Logic
b. Bus Direction and Data Conversion Logic
c. High Byte Enable Logic

4. Peripheral Control Logic

The Peripheral Control Logic provides logic for the following:

a. Peripheral Address Decoding
b. Port B Logic

BLOCK DIAGRAM SL9352

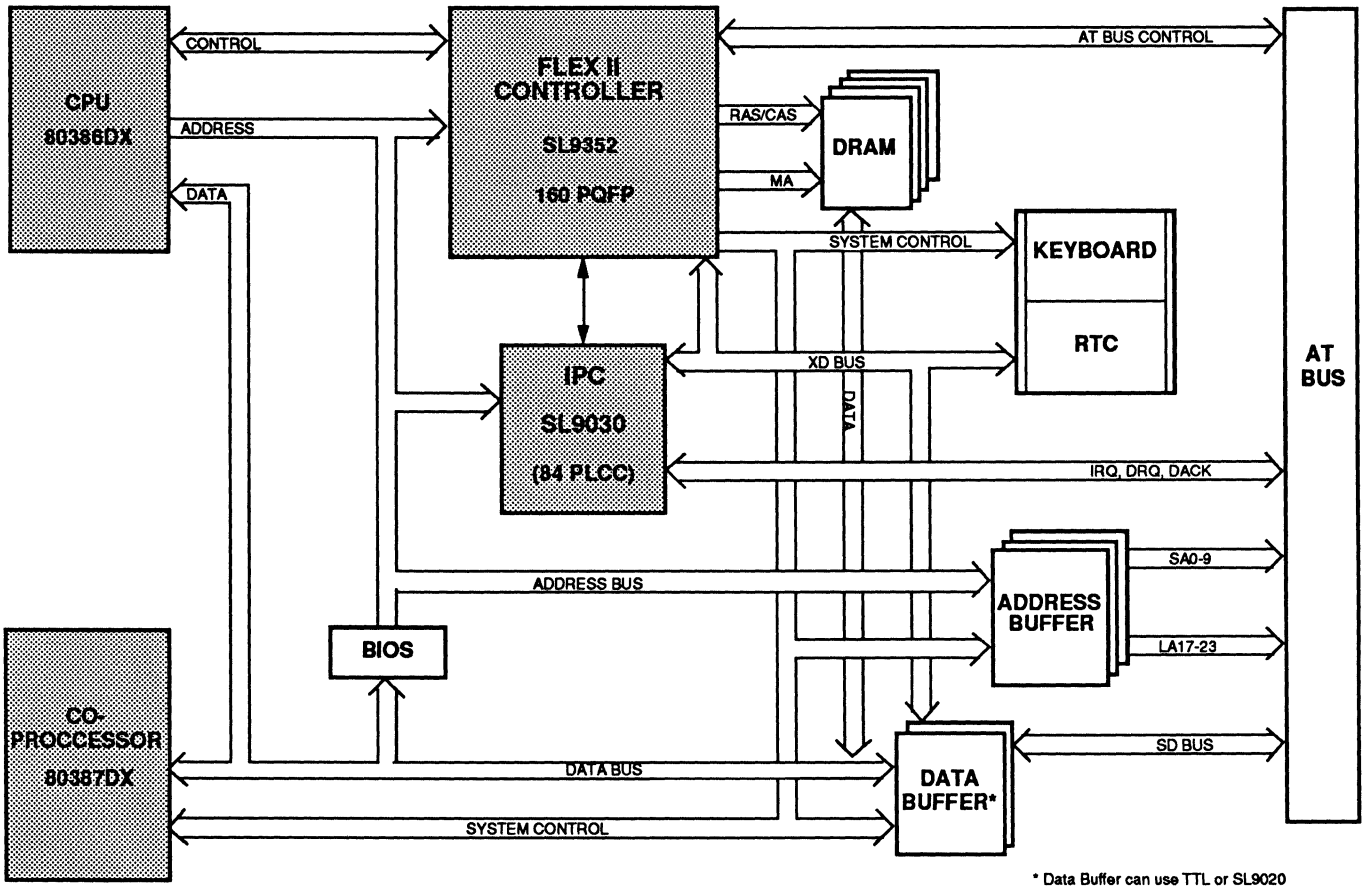


Fig. 1. Block Diagram for 80386DX CPU Board

Universal

Products

FEATURES

- **Generates all Essential Clock Signals for P.C.'s.**
- **Supports 8086/8088/80286/80386SX/80386DX/80486-based designs.**
- **Clock Options of 66, 50, 48, 40, 32, 24 MHz and Others.**
- **Facilitates FCC approval by reducing EMR.**
- **Requires Only One Crystal and a Few RC Components.**
- **Two Independent Clock Generators.**
- **Glitch Free Switching for both Clock Generators.**
- **All Outputs Capable of 8 mA Drive.**
- **Advanced Bipolar Technology.**
- **44 Pin PLCC.**

DESCRIPTION SL9090A

The SL9090A is a Universal Clock Chip capable of generating all essential clock signals that are used in a typical P.C. design. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs. The outputs of this clock chip are programmable through the keyboard and also by jumper settings. Clock options of 66 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz and 24 MHz. Multiples are available, giving flexibility to the user.

Frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. FSEL is used to control the system I/O bus clock. During a CPU cycle the FSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the FSEL goes low and fixed frequencies of 32 MHz, 16 MHz and 8 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pin F124 guaranties the add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock, by connecting the FSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the FSEL signal to be controlled through the keyboard by pressing "CTL ALT +" or "CTL ALT-".

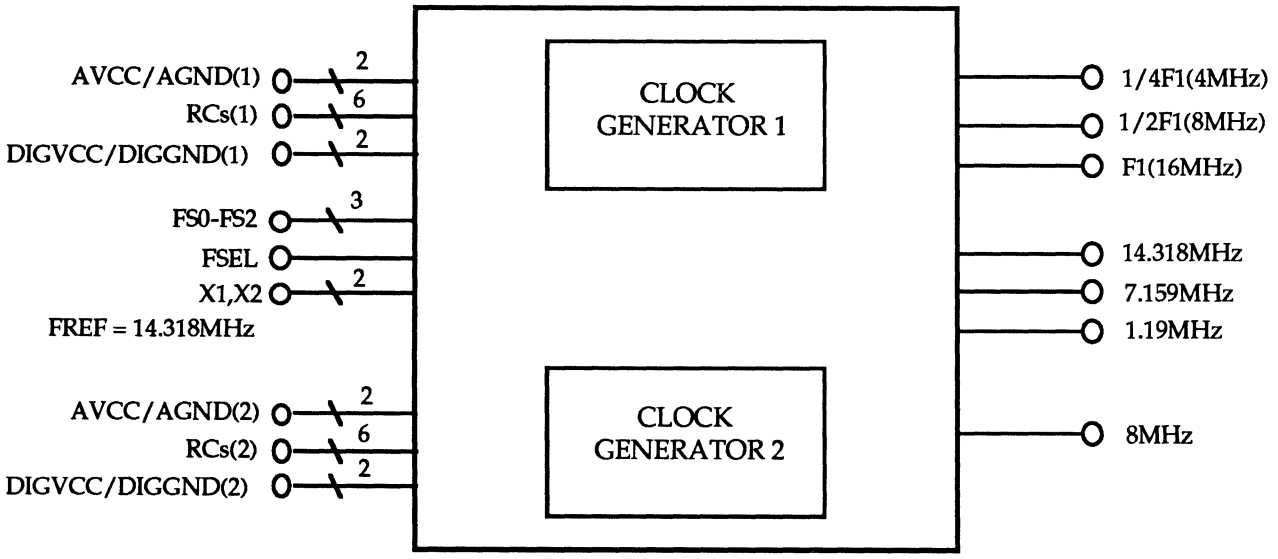
DESCRIPTION (Cont'd)

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. This frequency is divided by 2 internally and 7.159 MHz is supplied to the output through the FREF2 pin for the keyboard controller. The FREF12 pin has an output of 1.19 MHz and is used by the Timer 1 (8254) in the peripheral controller for refresh. All outputs are capable of 8mA drive.

The SL9090A consists of two independent Voltage Controlled Oscillators (VCO's) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9090A. Phase difference between this reference frequency and that generated by the VCO's are tracked by phase sensitive detectors. This becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCO's. The output from the VCO's are divided to generate the appropriate outputs.

The SL9090A is designed, using advanced Bipolar technology and is available in a 44 pin PLCC. It requires only one crystal (14.3 MHz) and a few RC components to generate all the essential clocks that are required for a PC design. As there is only one crystal on the system board, the Electro Magnetic Radiation (EMR) is reduced significantly facilitating FCC approval. This makes the SL9090A an ideal low cost solution with capabilities for universal applications.

FUNCTIONAL BLOCK DIAGRAM SL9090A



FEATURES

- **Generates all Essential Clock Signals for All-In-One Motherboards and Laptops.**
- **Supports 8086/8088/80286/80386SX/80386DX/80486-based Designs.**
- **CPU Clock Options of 66, 64, 50, 48, 40, 32, 24 MHz and Others.**
- **Integrates Floppy Drive, Serial Port and Keyboard Controller Clocks On-chip.**
- **Single Crystal Expedites FCC Approvals by Reducing EMR.**
- **Two Independent Clock Generators.**
- **Glitch Free Switching for both Clock Generators.**
- **Switchable Clock Rates, Even After Board Manufacturing.**
- **All Outputs Capable of 8 mA Drive.**
- **Advanced Low Power CMOS Technology.**
- **44 Pin PLCC.**

DESCRIPTION

The SL9092 is a universal System Clock Chip capable of generating all essential clock signals that are used in typical PC and Laptop designs. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 micropro-cessor based designs. The CPUCLK outputs of this clock chip are programmable through the keyboard or by jumper settings. Clock options of 66 MHz, 64 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz, and 24 MHz are available, as well as the resultant frequencies from dividing these signals by 2 or 4, giving optimal flexibility to the user.

CPU frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. IOSEL is used to control the system I/O bus clock. During a CPU cycle the IOSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the IOSEL goes low and fixed frequencies of 32 MHz, 16 MHz and 8 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pin F124 guarantees add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock by connecting the IOSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the IOSEL signal to be controlled through the keyboard.

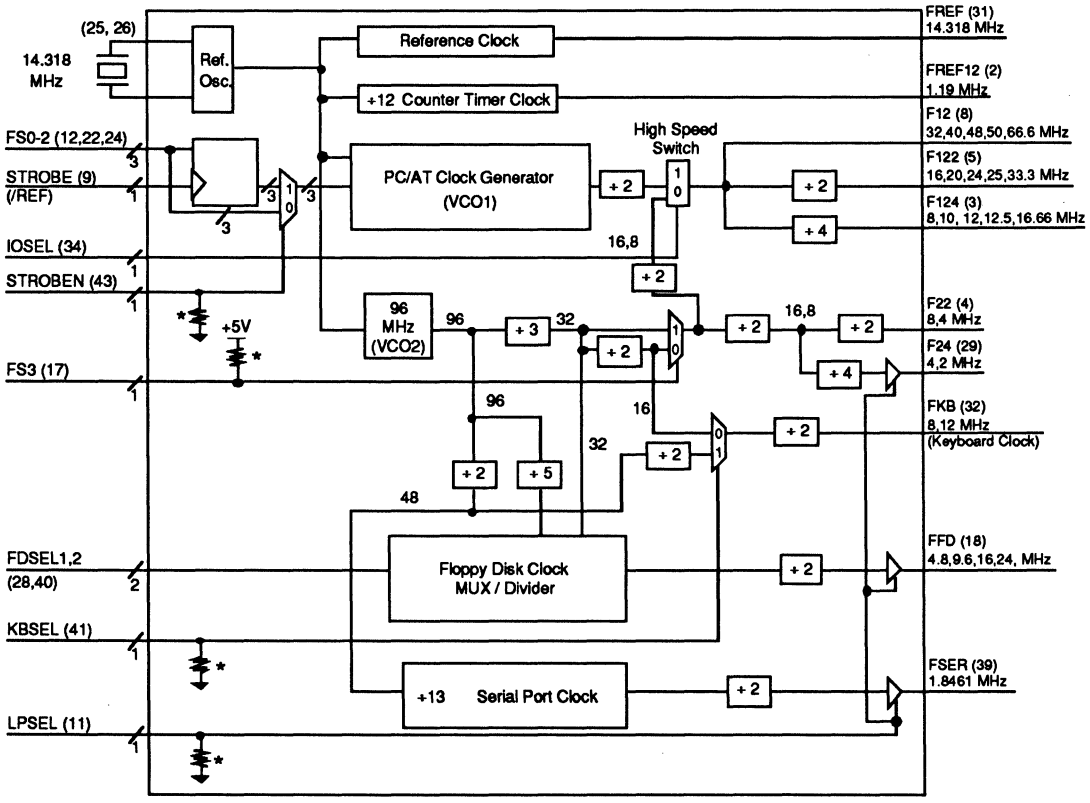
DESCRIPTION (Cont'd)

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. This frequency is divided by 2 internally and 7.159 MHz is supplied to the output through the FKB pin for the keyboard controller. The FREF12 pin has an output of 1.19 MHz and is used by Timer 1 (8254) in the peripheral controller for refresh. All outputs are capable of 8mA drive.

The SL9092 consists of two independent Voltage Controlled Oscillators (VCO's) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9092. Phase differences between this reference frequency and that generated by the VCO's are tracked by phase sensitive detectors. The phase difference becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCO's. The output from the VCO's are divided to generate the appropriate outputs.

The SL9092 is designed using advanced CMOS technology and is available in a 44 pin PLCC. It requires only one crystal (14.3 MHz) and a few RC components to generate all the essential clocks that are required for PC and Laptop designs. As there is only one crystal on the system board, Electro Magnetic Radiation (EMR) is reduced significantly, facilitating FCC approval. This makes the SL9092 an ideal low cost solution with capabilities for universal system applications.

BLOCK DIAGRAM SL9092



*Pulled Up/Down in Pin Description

FEATURES

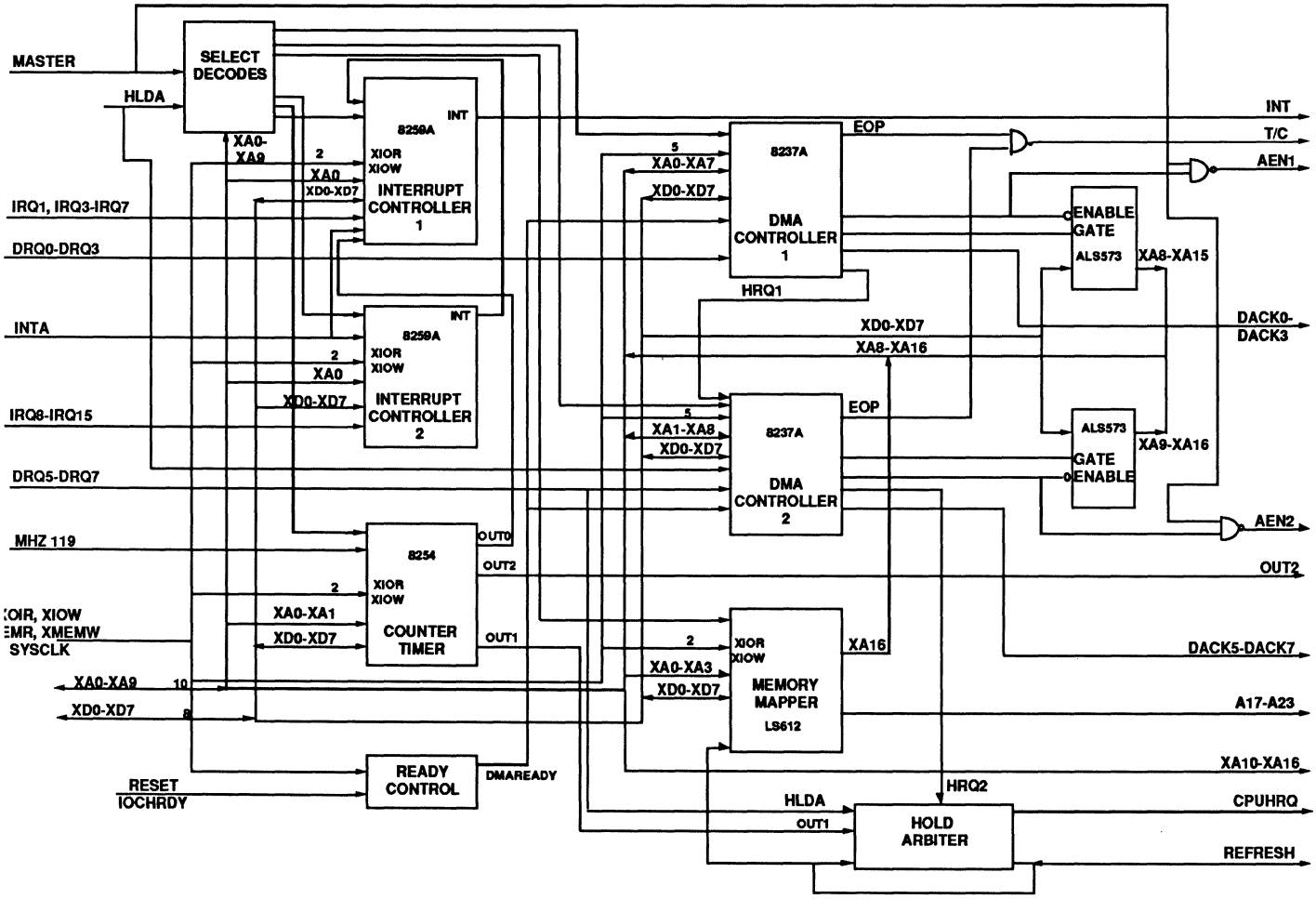
- **Pin to Pin Replacement for VLSI VL82C100.**
- **IBM PC/AT Compatible.**
- **Replaces 22 Logic Devices.**
- **Supports up to 20 MHz System Clock.**
- **Seven DMA Channels.**
- **14 External Interrupt Requests.**
- **Three Programmable Timer/Counter Channels.**
- **Compatible with all VIA FlexSet Chipsets.**
- **Designed in 1.2 micron CMOS Process.**
- **JEDEC - Standard 84-pin PLCC.**

DESCRIPTION

The SL9030 Integrated Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS373 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and other less-complex TTL devices. The SL9030 provides 24 address bits for 16M bytes of DMA address space. It also interfaces directly to the CPU to handle all interrupts. Arbitration between refresh and DMA hold requests are performed by the SL9030.

The device is manufactured with an advanced high-performance 1.2 micron CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The SL9030 is part of the PC/AT-compatible FlexSet chip sets from VIA Technologies.

BLOCK DIAGRAM SL9030



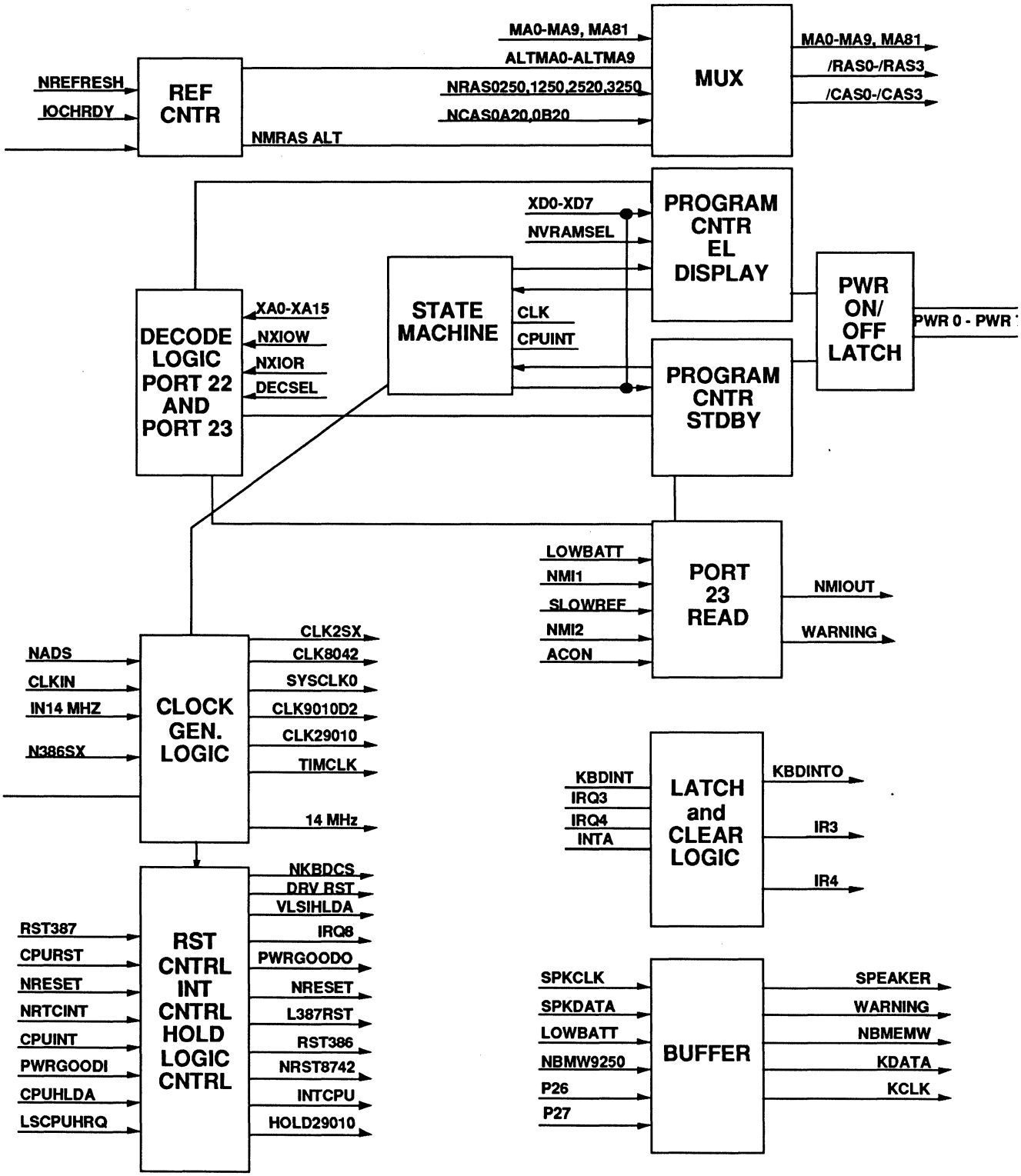
FEATURES

- **Supports 80286, 80386SX, 80386DX, and 80486 Page Mode or Cache-based Laptop designs.**
- **IBM PC/AT Compatible.**
- **Software Programmable Power Management Unit. Provides Individual On/Off Control.**
- **Compatible with all CPU Clock Rates.**
- **Supports Suspend and Resume Modes.**
- **Auto Power On Capability.**
- **Supports Slow Refresh DRAMs.**
- **Sleep Mode.**
- **Generates all the necessary PC/AT Clock Signals.**
- **Advanced CMOS Technology.**
- **160 pin Plastic Flatpack.**

DESCRIPTION

The SL9095 is an integrated CMOS Power Mangement Unit (PMU) which minimizes the power consumption and maximizes the battery life in laptop designs. The PMU is a single chip addition to the FlexSet PC/AT core logic chip set. The FlexSet provides all of the core logic required for any Intel microprocessor based designs (80286, 80386SX, 80386DX and 80486). This approach provides minimum chip count, low power dissipation, low cost and maximizes upward design compatibility.

BLOCK DIAGRAM SL9095

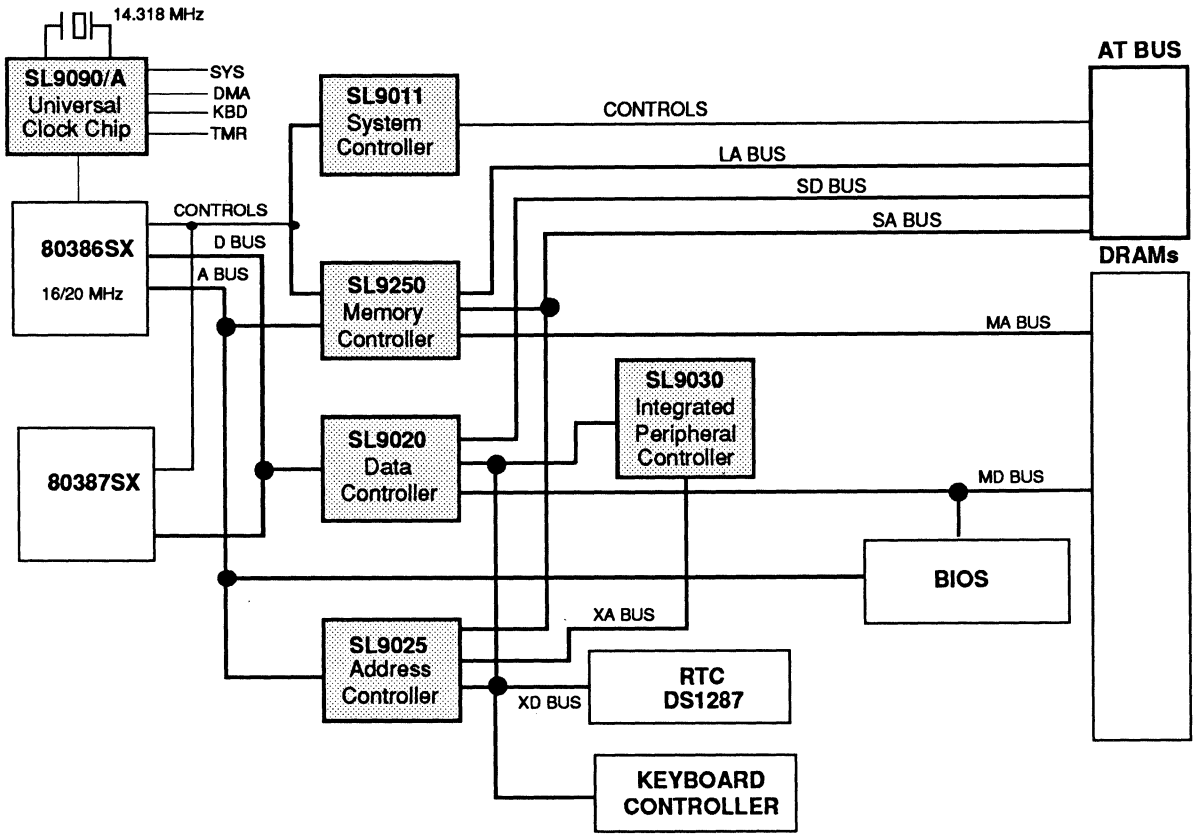


Support

Products

FEATURES

- 80386SX based PC/AT Motherboard Design.
- 16 / 20 MHz, Fast Page Mode.
- 100% IBM PC/AT Compatible.
- VIA FlexSet Chips.
- 80387SX Numeric Coprocessor Support.
- AMI, Award, Phoenix or Quadtel BIOS.
- Switchable Shadow RAM Feature.
- 512K (Min) to 8M (Max) On Board Memory.
- Uses SIMMs 256Kx1, 256Kx4 and 1Mx1 DRAMs or a Mix.
- Works with Page Mode or Static Column DRAMs.
- Selectable Wait States for Slower DRAMs. 100 ns DRAMs for 16 MHz Operation and 80 ns DRAMs for 20 MHz Operation.
- Provide 640Kb / 384Kb Memory Configuration.
- Switchable Clock Speed using Hardware or Keyboard Controls.
- I/O Bus Decoupling to Ensure Compatibility at All Speeds.
- Keyboard Lock, Turbo and Power On LED connectors.
- Speaker and Keyboard Connectors.
- 8 Expansion Slots: 6) 16-bit Slots; 2) 8-bit Slots.
- Baby AT Size (8.5 X 13 inches); 4 Layer PC Board.



Flex I / 386SXP Block Diagram

SL9011 System Controller: The SL9011 integrates all the PC/AT System control logic including clock switching and reset logic. It also contains a programmable wait state and command delay for external memory and I/O commands.

SL9020 Data Controller: The SL9020 provides a fast Data In to Data Out throughput time of 15ns with 24mA buffers for the MD, SD and XD busses for the 16 bit data bus.

SL9025 Address Controller: The SL9025 provides a fast Address In to Address Out Time of 15 ns, with 24 ma buffers for SA and XA busses. It also has the necessary refresh for 256 Kb and/or 1Mb DRAMs.

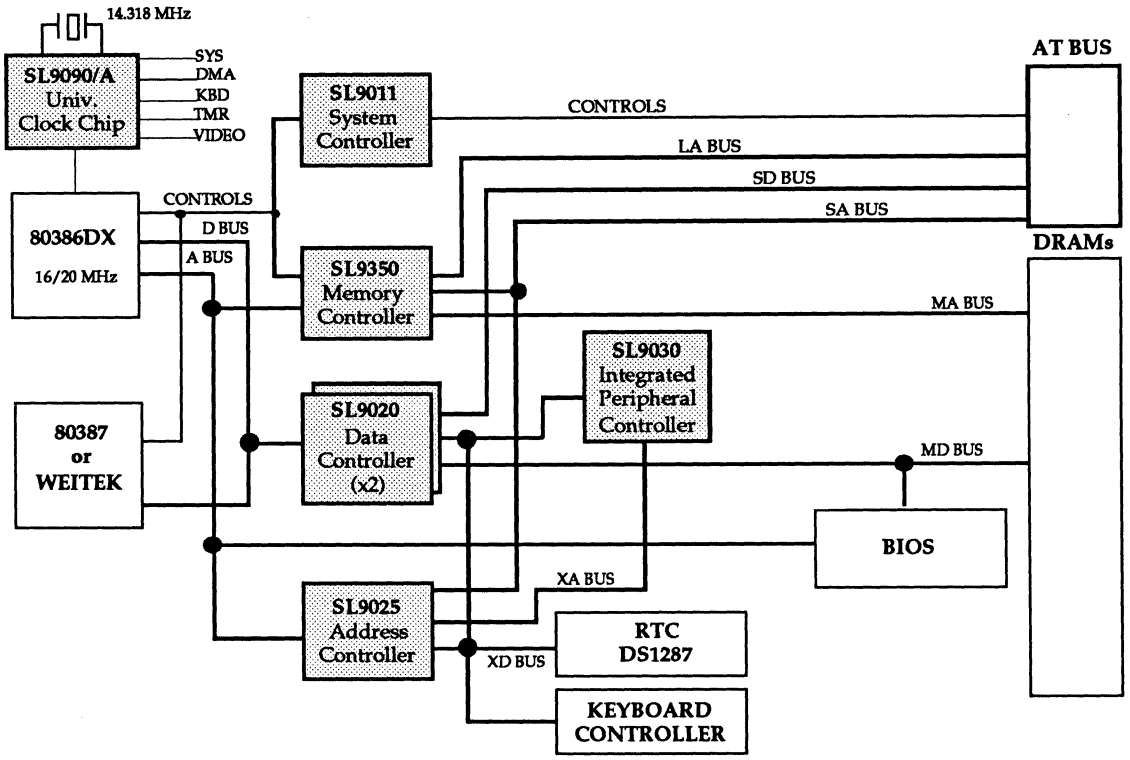
SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design except the keyboard controller and RTC. It is fully compatible with the VLSI 82C100.

SL9250 Page Mode Memory Controller: The SL9250 supports up to 8M on board memory with any combination of 256K X 1, 256K X 4 or 1M X 1 DRAM. It also includes a built in shadow RAM feature.

SL9090/A Universal PC/AT Clock: The SL9090/A generates all the essential PC/AT clock signals using only one 14.3 MHz crystal. Output frequencies form 16 to 66 MHz are programmable and designed to be switched dynamically.

FEATURES

- 80386DX based PC/AT Motherboard Design.
- 16 / 20 MHz, Fast Page Mode.
- 100% IBM PC/AT Compatible.
- VIA FlexSet™ Chips.
- 80387DX or Weitek Numeric Coprocessor Support.
- AMI, Phoenix, Award or Quadtel BIOS.
- Switchable Shadow RAM Feature.
- 1M (Min) to 16M (Max) On Board Memory.
- Uses either 256Kb or 1M DRAM SIMMs or a Mix.
- Uses either Page Mode or Static Column DRAMs.
- Selectable Wait States for Slower DRAMs. 100 ns DRAMs for 16 MHz and 80 ns DRAMs for 20 MHz Operation.
- 640Kb / 384Kb Memory Configuration.
- Switchable Clock Speed using Hardware or Keyboard Controls.
- I/O Bus Decoupling to Ensure Compatibility at All Speeds.
- Keyboard Lock, Turbo and Power On LED Connectors.
- Speaker and Keyboard Connectors.
- 8 Expansion Slots; 6) 16-bit Slots and 2) 8-bit Slots.
- Baby AT Size (8.5 X 13 inches) 6 Layer PC Board.



Flex II / 386DXP™ Block Diagram

SL9011 System Controller: The SL9011 integrates all the PC/AT System control logic including clock switching and reset logic. It also contains a programmable wait state and command delay for external memory and I/O commands.

SL9020 Data Controller: The SL9020 provides a fast data in to data out throughput time of 15ns with 24mA buffers, with latches, for the MD, SD and XD busses. An 80386DX based system, 32 bit data bus, uses two SL9020 data controllers.

SL9025 Address Controller: The SL9025 provides a fast address in to address out throughput time of 15 ns with 24 ma buffers for SA and XA busses. It also provides the neccessary refresh for 256 Kb and/or 1Mb DRAMs.

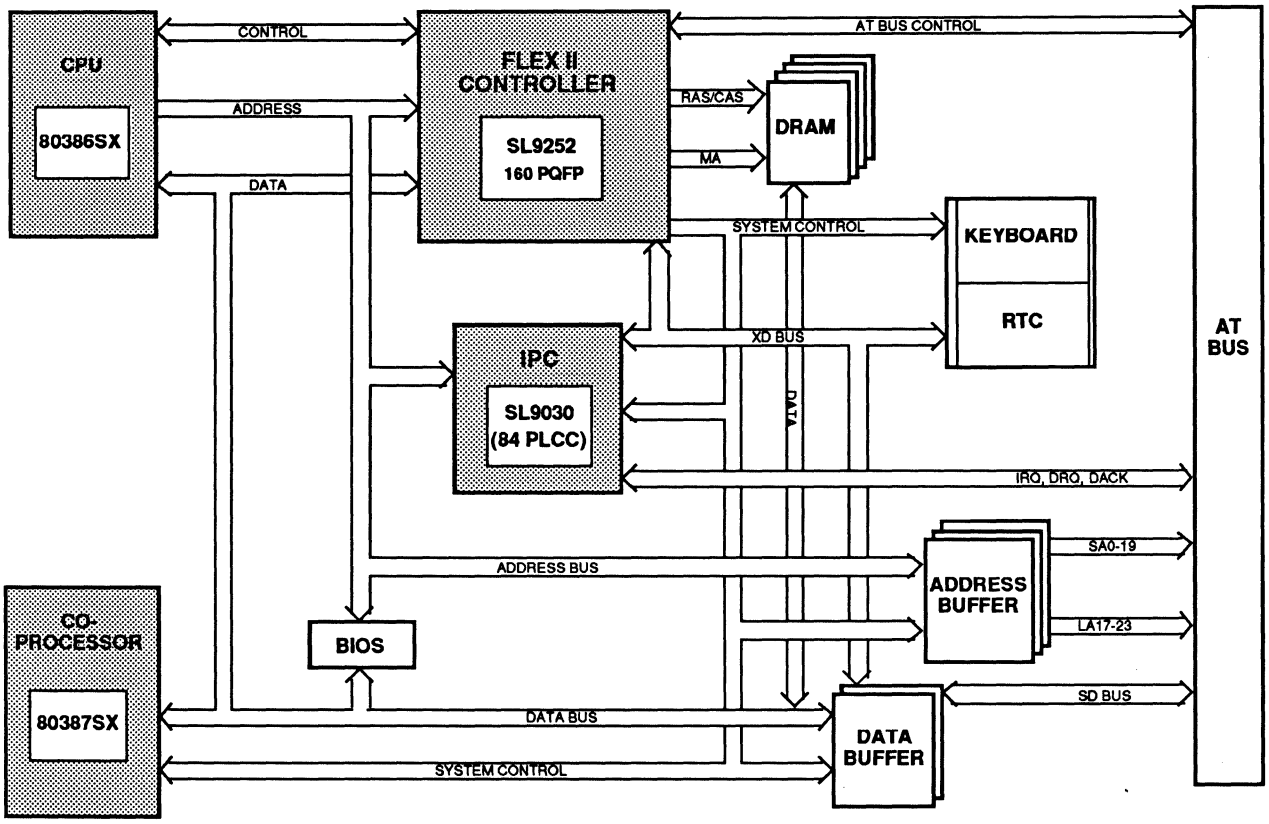
SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design except the keyboard controller and RTC. It is fully compatible with the VLSI 82C100.

SL9350 Page Mode Memory Controller: The SL9350 supports up to 16M on board memory with any combination of 256K X 1, 256K X 4 or 1M X 1 DRAM. It also includes a built in shadow RAM feature.

SL9090/A Universal PC/AT Clock: The SL9090/A generates all the essential PC/AT clock signals using only one 14.3 MHz crystal. Output frequencies form 16 to 66 MHz are programmable and designed to be switched dynamically.

FEATURES

- 100% IBM PC/AT Compatible.
- 80386SX Based PC/AT Motherboard Design.
- 16/20 MHz, Operation.
- Baby AT Form Factor (8.5 X 13 inches).
- 4 Layer Board.
- 7 Expansion Slots (3 8-bit Slots and 4 16-bit Slots).
- Speaker and Keyboard Connectors.
- Turbo and Power-on LED Connectors.
- 80387SX Numeric Coprocessor Support.
- Single Chip BIOS Support.
- Uses 256K, 1M and 4M DRAM's.
- Supports Intermixing of different size DRAM's.
- 512K (minimum) to 16M (maximum) On-board Memory.
- 4 Banks of Memory.
- Supports Page Mode and 2 or 4 Way Page Interleave Memory Access.
- Disable (on-board) Memory to 0K in 128K Resolution.
- Programmable Memory Remap.
- Programmable BIOS and Video Shadow RAM.
- Programmable Read and Write Wait States.
- Programmable Hit (0-3) and Miss (1-4) Wait States for DRAM Access.



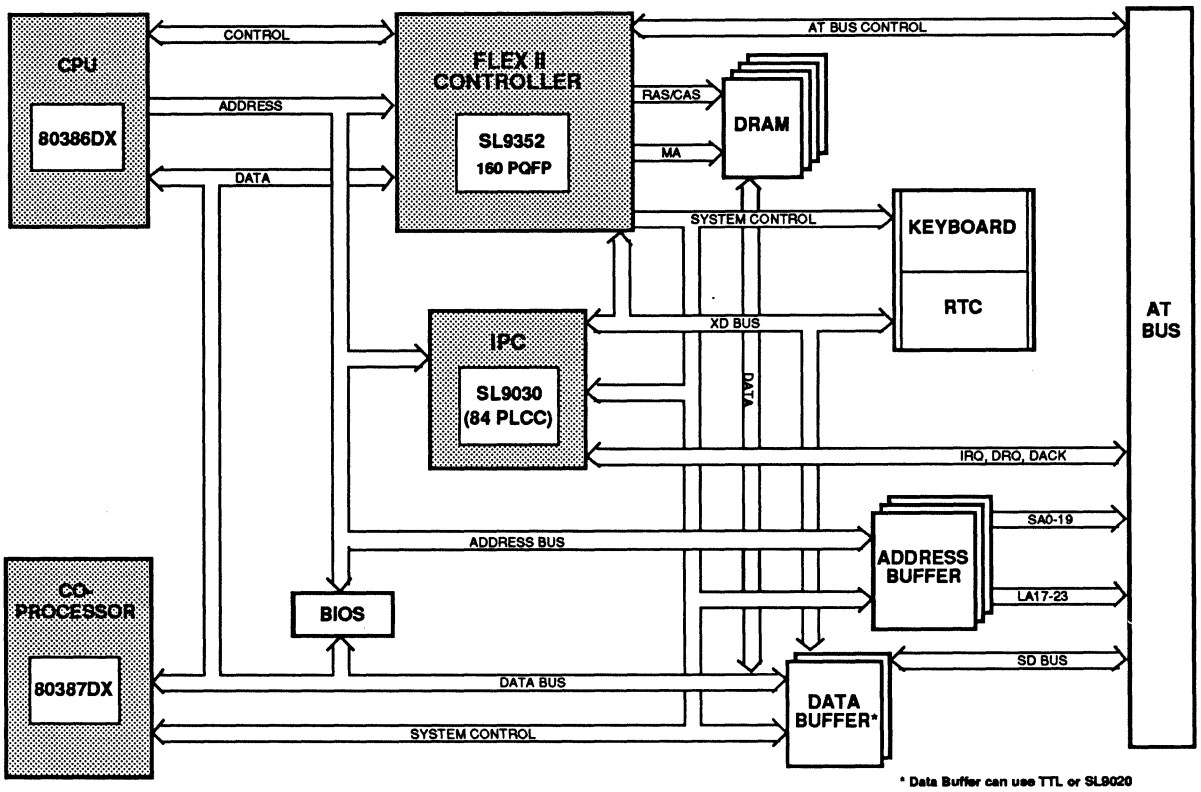
FLEX II / 386SXP BLOCK DIAGRAM

SL9252 System and Memory Controller: The SL9252 is a member of VIA's Flex II product line. It efficiently integrates all the PC/AT System control logic along with the Page Mode memory functions specific to the 80386SX PC/AT design. It can support 16M of memory using 256K, 1M or 4M DRAMs. All wait states are programmable for memory and I/O commands. It supports upto 20 MHz performance and offers enhanced features such as remap, staggered RAS, support for EMS LIM 4.0, synchronous or asynchronous system control operation and memory backfill.

SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design except the keyboard controller and RTC. It is fully compatible with the VLSI 82C100. It has two 82C374 Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper and other less-complex TTL devices. It provides 24 address bits for 16M bytes of DMA address space and can be interfaced directly to the CPU to handle all interrupts. It can also perform arbitration between refresh and DMA hold requests.

FEATURES

- 100% IBM PC/AT Compatible.
- 80386DX Based PC/AT Motherboard Design.
- 20/25 MHz, Operation.
- Baby AT Form Factor (8.5 X 13 inches).
- 4 Layer Board.
- 7 Expansion Slots (3 8-bit Slots and 4 16-bit Slots).
- Speaker and Keyboard Connectors.
- Turbo and Power-on LED Connectors.
- 80387DX Numeric Coprocessor Support.
- Single Chip BIOS Support.
- Uses 256K, 1M and 4M DRAM's.
- Supports Intermixing of different size DRAM's.
- 1M (minimum) to 16M (maximum) On-board Memory.
- 4 Banks of Memory.
- Supports Page Mode and 2 Way Page Interleave Memory Access.
- Disable (on-board) Memory to 0K in 128K Resolution.
- Programmable Memory Remap.
- Programmable BIOS and Video Shadow RAM.
- Programmable Read and Write Wait States.
- Programmable Hit (0-3) and Miss (1-4) Wait States for DRAM Access.



Flex II / 386DX™ Block Diagram

SL9352 System and Memory Controller: The SL9352 is a member of VIA's Flex II product line. It efficiently integrates all the PC/AT System control logic with the Page Mode/Page Interleave memory control functions specific to the 80386DX PC/AT design. It can support 64M of memory using 256K, 1M or 4M DRAMs. All wait states are programmable for memory and I/O commands. It supports up to 20MHz performance and offers enhanced features like Remap, staggered RAS, support for EMS LIM 4.0, Synchronous or Asynchronous system control operation and memory Backfill.

SL9030 Integrated Peripheral Controller: The SL9030 replaces 22 logic devices on the X Bus portion of an AT-Compatible design (keyboard controller and RTC are not replaced). It is fully compatible with the VLSI 82C100. It has two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper and other less-complex TTL devices. It also provides 24 address bits for 16M bytes of DMA address space and can be interfaced directly with the CPU to handle all interrupts. It can also perform arbitration between refresh and DMA hold requests.

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