Data Sheet

VL210

USB 3.0 Hub Controller

1 Port USB3.0 and 3 Ports USB2.0

March 31, 2014

Revision 0.80

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Revision History

Revision No.	Draft Date	History	Initial
0.56	Dec. 16. 2013	Preliminary Engineering Draft Release.	TS
0.60	Jan. 13. 2014	Updated Feature List to reflect ACA Charging Support	TS
0.80	**Mar. 31. 2014**	**Correct the typo.** **Correct the TID.**	**AY**

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Product Feature

VL210: Super-Speed USB Hub Controller – 1 Port USB3.0 and 3 Ports USB2.0

- **USB 3.0 Compliant**
  - Compliant to Universal Serial Bus 3.0 Specification Rev 1.0, including Hub errata
  - Compliant to Universal Serial Bus Specification Revision 2.0
  - Supports simultaneous Super-speed(SS), high-speed (HS), full-speed (FS) traffic, and low-speed (LS) traffic
  - Four down-stream ports, one up-stream port
  - In-house USB PHY employs advanced CMOS process for low power consumption
  - Supports USB Low-Power States such as Ux states and Selective Suspend

- **Full Sideband Signal Support**
  - Supports either individual mode or gang mode operation for power enable and over current detection on down-stream ports
  - Supports LED status indicators with automatic or manual control via GPIO per down-stream port
  - 2x GPIO, reserved for special functions

- **Comprehensive USB Battery Charging Support**
  - Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
  - Adds Support for Vendor Specific Charging Modes eg. Apple, RIM, etc.
  - Supports YD/T 1591-2009
  - Supports “Sleep Charging” (DCP + Apple Mode)
  - Supports charging across all down-stream ports, depending on configuration
  - Supports charging on upstream port to USB Host via USB Battery Charging ACA Configuration

- **Physical**
  - QFN 48L green package (6x6x0.85 mm)

- **Certification (TBD)**
  - Earned USB 2.0 USB-IF certification
  - Earned USB 3.0 USB-IF certification TID# 330000050
  - Passed Windows HCK Logo for Windows 8, RT

- **Applications**
  - Standalone USB hub.
  - Desktop/Notebook motherboard on-board hub
  - Desktop front panel hub
  - Notebook/Ultrabook Docking Station / Port Replicator
  - USB hub compound device with keyboard, mouse, display, etc.

- **Platform and Operating System Support**
  - Standalone USB hub
  - Desktop/Notebook motherboard on-board hub
  - Desktop front panel hub
  - Notebook/Ultrabook Docking Station / Port Replicator
  - USB hub compound device with keyboard, mouse, display, etc

- **Misc**
  - Optimized for Low Power consumption
  - Integrated 5V to 3.3V LDO and 5V to 1.2V Switching Regulators
  - 3.3 V and 1.2 V power supply
  - PLL embedded with external 25MHz crystal
  - Support external SPI flash for firmware upgrade

VL210 System Overview

VIA Lab's VL210 is a 4th generation advanced USB 3.0 Hub controller featuring a simplified port configuration. VL210 features four downstream ports: a single USB 3.0 and three USB 2.0 ports, each with comprehensive USB Charging without the need for external charger ICs. The VL210 employs an advanced CMOS process for greatly reduced power consumption and fully supports USB power management and low-power states. The custom in-house USB PHY gives VL210 excellent signal integrity characteristics under a variety of channel conditions and now supports improved USB EMI profile support including the new 2.4GHz Radio Friendly mode. VL210 features a highly flexible firmware architecture, providing a framework for custom functions as well as advanced feature support in addition to in-field updates.

VL210 hub devices work under Windows, Mac OS X, and various Linux kernels without additional drivers. Since USB 3.0 hubs do not require additional drivers, VL210 is also compatible with non-x86 devices and platforms that support USB hub functions such as smart phones, tablets, and set-top boxes. It is well suited for all USB hub applications such as stand-alone USB hubs, Notebook/Ultrabook docking stations/port-replicators, desktop PC front panel, 2-in-1 convertible Tablets, and USB hub compound devices.

With well-planned pinout and a high level of integration, VL210 based devices enjoy easy layout and simplified BOM. Full sideband signal pins are available for showing power enable, over current, GPIO, and LED status control. The SPI interface supports external EEPROM/Flash ROM which can be updated over USB. VL210 is available in QFN 48L package (6x6x0.85 mm).

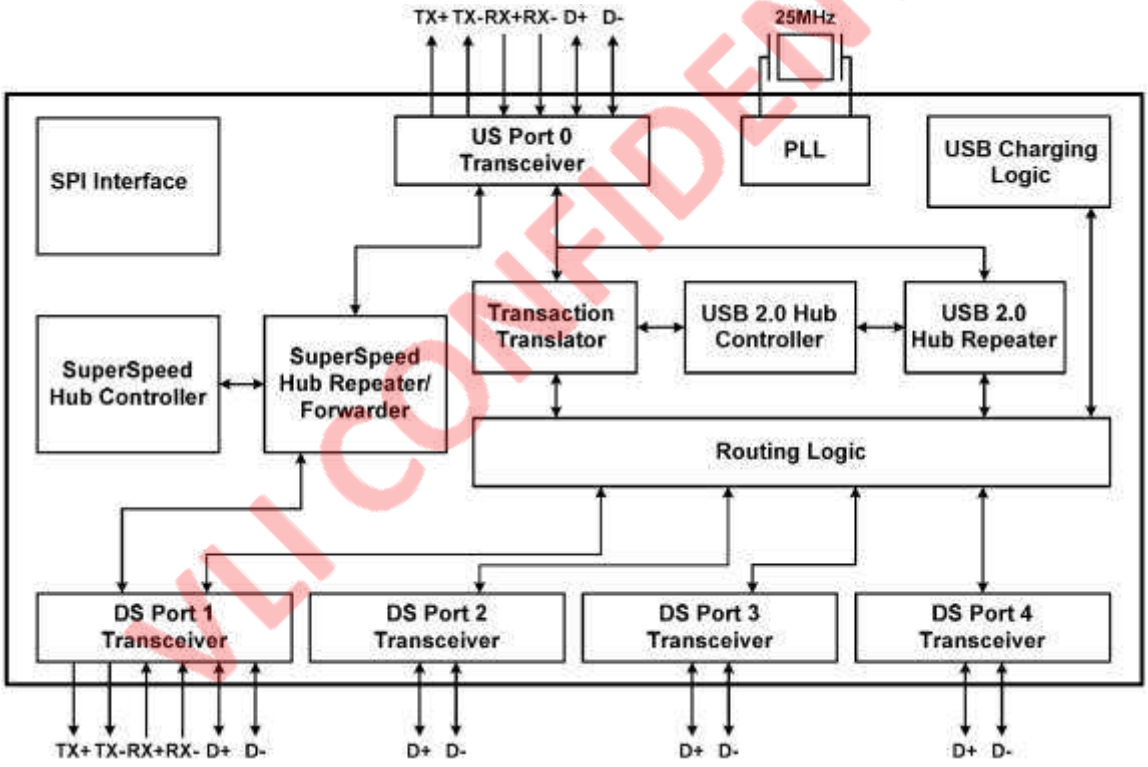


Figure 1 – VL210 Block Diagram

Rapid Charging over USB in Detail

3 Concepts of Rapid Charging over USB:

(1) **Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.** The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.0 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 1000mA to 2000mA.

(2) **It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine the Rapid Charging capabilities of the Host/Hub port it is connected to.** Since Rapid Charging over USB allows charging at rates in excess of USB spec, this detection mechanism is necessary to ensure safe and reliable operation, and can prevent situations where a device requests more current than what a host/hub port can supply. Also, this implies that Rapid Charging will only occur when both Host/Hub and Device supports it.

(3) **The rate at which a device charges is dependant upon the device.** This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port

This is a typical USB 2.0 or USB 3.0 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.0 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.0 modes.

CDP – Charging Downstream Port

CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

DCP – Dedicated Charging Port

DCP is defined in the USB Battery Charging Specification 1.2 and has been in use on an unofficial basis prior to the official USB Battery Charging Specification. DCP is a dedicated charging mode, so when a device is charging under DCP, regular USB operations such as data transfer to the device are not supported.

Special Modes

Various vendors such as Apple, RIM, Motorola, etc. may employ different detection mechanisms compared to other USB devices and thus, may enter Rapid Charging under the previously mentioned charging modes. VL811+ supports an auto detection mechanism that provides charging for the majority of devices.

Pinout

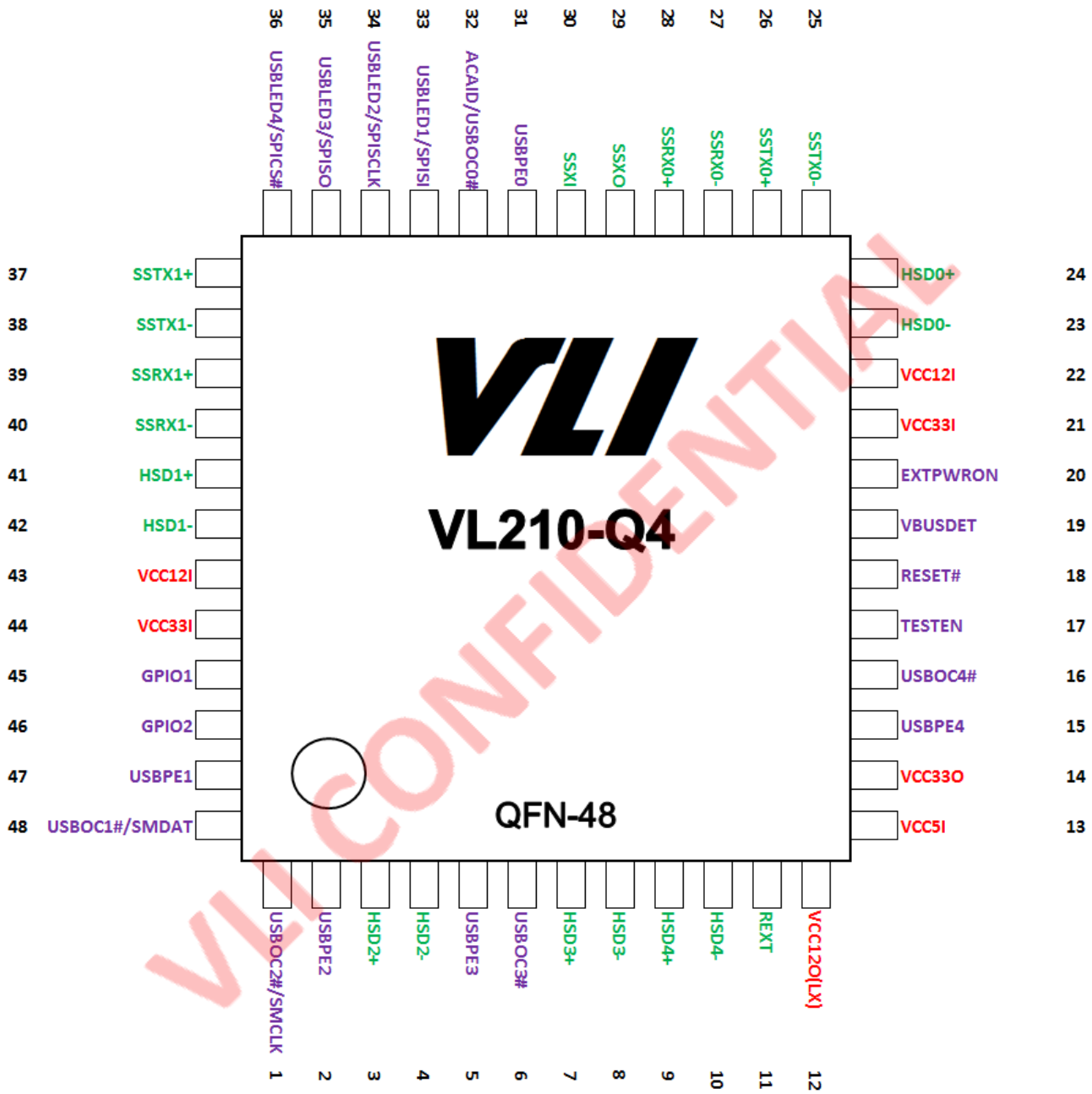


Figure 2 – VL210-Q4 QFN-48 Package Pin Diagram

Pin List

Pin	Pin Name
1	USBOC2#/SMCLK
2	USBPE2
3	HSD2+
4	HSD2-
5	USBPE3
6	USBOC3#
7	HSD3+
8	HSD3-
9	HSD4+
10	HSD4-
11	REXT
12	VCC12O(LX)
13	VCC5I
14	VCC33O
15	USBPE4
16	USBOC4#
17	TESTEN
18	RESET#
19	VBUSDET
20	EXTPWRON
21	VCC33I
22	VCC12I
23	HSD0-
24	HSD0+

Pin	Pin Name
25	SSTX0-
26	SSTX0+
27	SSRX0-
28	SSRX0+
29	SSXO
30	SSXI
31	USBPE0
32	ACAID/USBOC0#
33	USBLED1/SPISI
34	USBLED2/SPISCLK
35	USBLED3/SPISO
36	USBLED4/SPICS#
37	SSTX1+
38	SSTX1-
39	SSRX1+
40	SSRX1-
41	HSD1+
42	HSD1-
43	VCC12I
44	VCC33I
45	GPIO1
46	GPIO2
47	USBPE1
48	USBOC1#/SMDAT

Table 1 – VL210 QFN-48 Package Pin List

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.0 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	26		USB 3.0 UP Port Differential Transmit Data +
SSTX0-	25		USB 3.0 UP Port Differential Transmit Data -
SSRX0+	28		USB 3.0 UP Port Differential Receive Data +
SSRX0-	27		USB 3.0 UP Port Differential Receive Data -
SSTX1+	37		USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	38		USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	39		USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	40		USB 3.0 DP1 Port Differential Receive Data -

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	24		USB 2.0 UP Bus Data Plus (D+)
HSD0-	23		USB 2.0 UP Bus Data Minus (D–)
HSD1+	41		USB 2.0 DP1 Bus Data Plus (D+)
HSD1-	42		USB 2.0 DP1 Bus Data Minus (D–)
HSD2+	3		USB 2.0 DP2 Bus Data Plus (D+)
HSD2-	4		USB 2.0 DP2 Bus Data Minus (D–)
HSD3+	7		USB 2.0 DP3 Bus Data Plus (D+)
HSD3-	8		USB 2.0 DP3 Bus Data Minus (D–)
HSD4+	9		USB 2.0 DP4 Bus Data Plus (D+)
HSD4-	10		USB 2.0 DP4 Bus Data Minus (D–)

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	30		25M crystal input
SSXO	29		25M crystal output
REXT	11		Connect to reference resistor

Power and Ground

Pin Name	Pin #	I/O	Signal Description
VCC12I	22	PWR	1.2V Core power
VCC33I	21,44	PWR	3.3V Core power
VCC5I	13	PWR	5-3.3V LDO Input, 5-1.2V Regulator Input
VCC33O	14	PWR	3.3V LDO Output
VCC12I	43	PWR	5-1.2V Feedback, 1.2V Input
VCC12O(LX)	12	PWR	5-1.2V Regulator Output

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	17	I	Test Mode Enable Do not connect for normal operation. Internal pull down. Low: Normal mode. High: Test mode.

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBLED1/SPISI	33	O	DP1 LED Indicator and SPISI share pin. For LED, output high when active and external 100Kohm pull low required.
USBLED2/SPICLK	34	O	DP2 LED Indicator / SPISCLK share pin. For LED, output high when active and external 100Kohm pull low required.
USBLED3/SPISO	35	O	DP3 LED Indicator and SPISO share pin. For LED, output high when active and external 100Kohm pull low required.
USBLED4/SPICS#	36	O	DP4 LED Indicator / SPICS# share pin. For LED, output high when active and external 100Kohm pull low required.
USBPE1	47	O	DP1 Power Enable. Low: Port Power On. High: Port Power Off.
USBPE2	2	O	DP2 Power Enable. Low: Port Power On. High: Port Power Off.
USBPE3	5	O	DP3 Power Enable. Low: Port Power On. High: Port Power Off.
USBPE4	15	O	DP3 Power Enable. Low: Port Power On. High: Port Power Off.
ACAID/USBOC0#	32	I/O	UP Over Current Detect Low: Port Over Current High: Port Power Normal
USBOC1#/SMDAT	48	I/O	DP1 Over Current Detect Low: Port Over Current High: Port Power Normal SMBus data for debug only. It is not a standard SMBus interface. Open Drain
USBOC2#/SMCLK	1	I/O	DP2 Over Current Detect Low: Port Over Current High: Port Power Normal SMBus clock for debug only. It is not a standard SMBus interface. Open Drain
USBOC3#	6	I	DP3 Over Current Detect Low: Port Over Current High: Port Power Normal
USBOC4#	16	I	DP4 Over Current Detect Low: Port Over Current High: Port Power Normal
EXTPWRON	20	I	Upstream Port VBUS Detection for Upstream port plug-in
RESET#	18	I	System Reset Low: Reset High: Normal Operation
VBUSDET	19	I	5V USB VBus Presence Detect
GPIO1	45	I/O	GPIO Pin reserved for special function
GPIO2	46	I/O	GPIO Pin reserved for special function

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{33}	3.3V Power Supply Voltage	-0.5	3.63	V	—
V_{12}	1.2V Input Voltage	-0.5	1.26	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{jc}	Thermal resistance between junction and case	● For 4-layer PCB: 9.1 ● For 2-layer PCB: 11.3		°C/W	2L & 4L PCB definitions follow JESD51-7
θ_{ja}	Thermal resistance between junction and ambient	● For 4-layer PCB: 21.8 ● For 2-layer PCB: 56.8		°C/W	
P_D	Max Power Dissipation	—	1.0 0.6	W	Q8P 4-Port Q4S 2-Port

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	70	°C	—
T_j	Junction Temperature	0	125	°C	—
V_{33}	3.3V Power Supply Voltage	3.0	3.6	V	—
V_{10}	1.2V Input Voltage	1.14	1.26	V	1.2 Nominal
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.0	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	µA	$0<V_i<V_{33}$
I_{OZ}	Tristate Leakage Current	—	+/-20	µA	$0<V_o<V_{33}$

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW data for VL210. Timing guidelines are provided to assist in selection of appropriate and compatible SPI flash. To ensure SPI flash suitability, not only should the timing requirements conform to the provided guidelines, but actual testing with VL811+ should also be done.

Symbol	Parameters	Condition	Value	Unit
f_{CT}	Clock Frequency for fast read mode(*)	Max value must larger than	15	MHz
f_C	Clock Frequency for read mode	Max value must larger than	15	MHz
t_{RI}	Input Rise time	Max value must larger than	5	ns
t_{FI}	Input Fall time	Max value must larger than	5	ns
t_{CKH}	SCK High Time	Min value must smaller than	20	ns
t_{CKL}	SCK Low Time	Min value must smaller than	20	ns
t_{CEH}	CE# High Time	Min value must smaller than	100	ns
t_{CS}	CE# Setup Time	Min value must smaller than	20	ns
t_{CH}	CE# Holde Time	Min value must smaller than	100	ns
t_{DS}	Data In Setup Tiime	Min value must smaller than	20	ns
t_{DH}	Data In Hold Time	Min value must smaller than	20	ns
t_{HS}	Hold Setup Time	Not Utilized		
t_{HD}	Hold Time	Not Utilized		
t_V	Output Valid	Max value must smaller than	20	ns
t_{OH}	Output Hold Time Normal Mode	Not Utilized		
t_{LZ}	Hold to Output Low Z	Not Utilized		
t_{HZ}	Hold to Output High Z	Not Utilized		
t_{DIS}	Output Disable Time	Not Utilized		
t_{EC}	Erase Time	Max value must smaller than	100	ms
t_{PP}	Page Program Time	Max value must smaller than	100	ms
t_{VCS}	Vcc Setup Time	Min value must smaller than	1	ms
t_w	Write Status Register Time (Flash bit)	Max value must smaller than	100	ms

*Fast read mode must be supported.

SERIAL INPUT/OUTPUT TIMING (1)

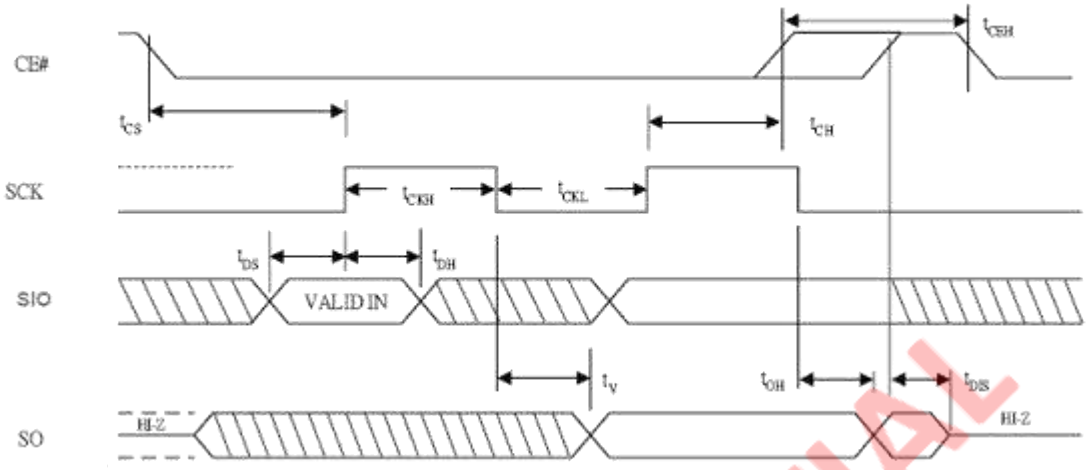


Figure 3 - Illustration of SPI Flash Interface Timing – (1)

HOLD TIMING

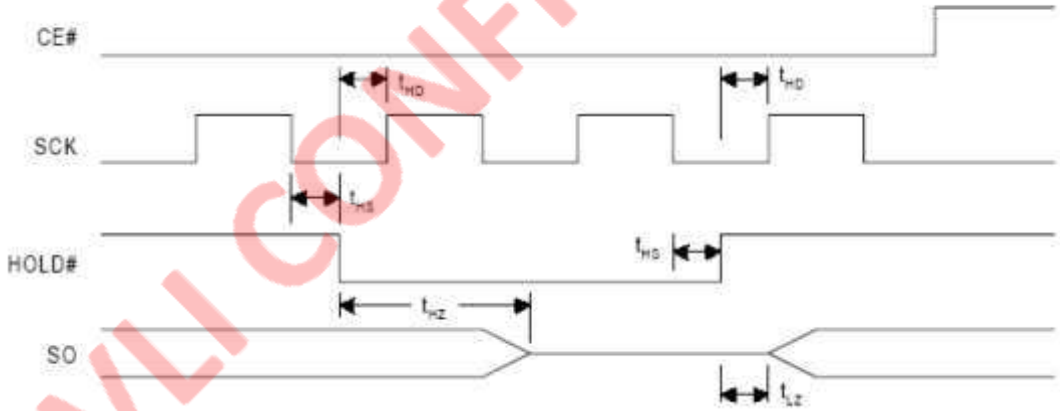
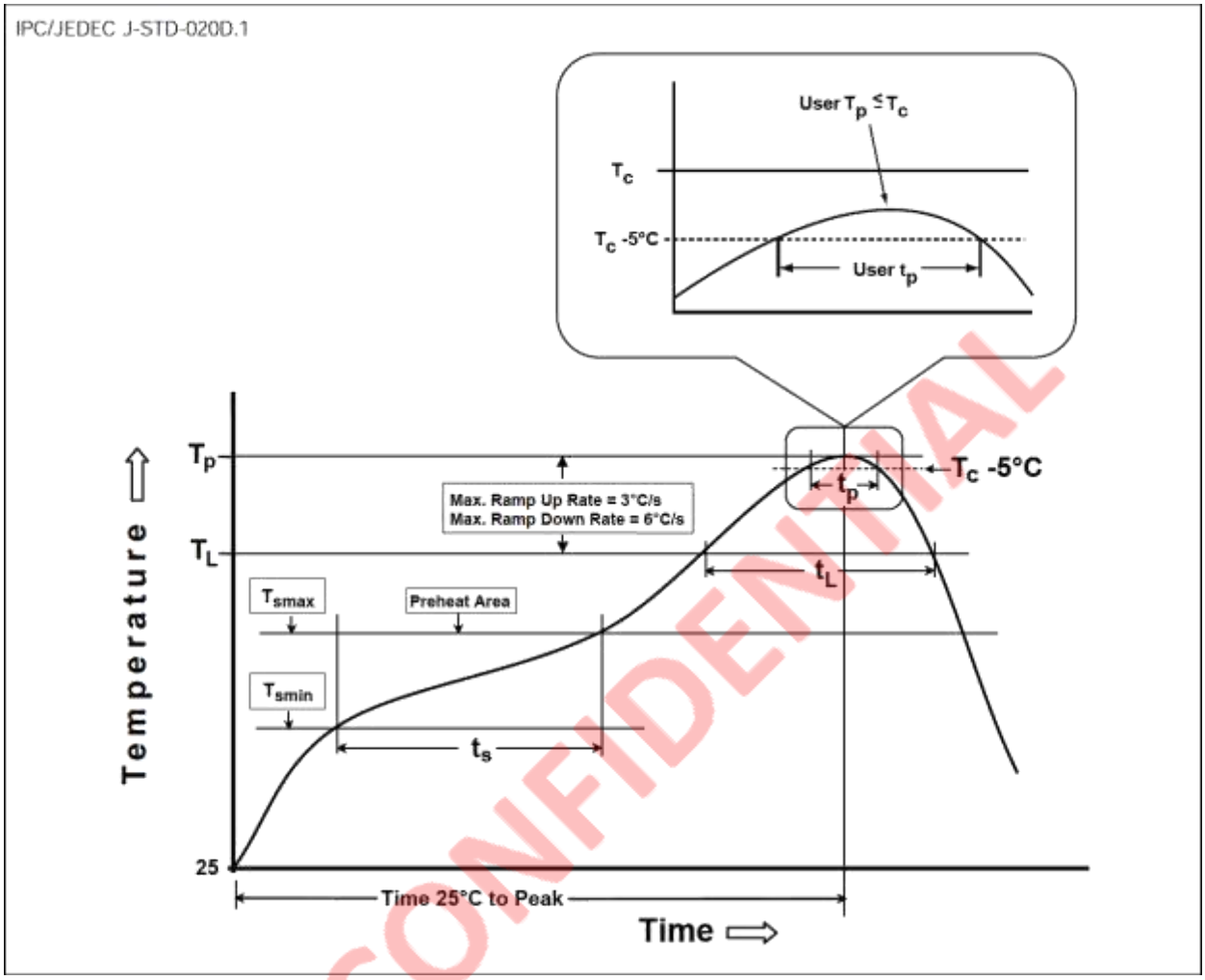


Figure 4 - Illustration of SPI Flash Interface Timing – (2)

General Reflow Profile Guidelines



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	225 °C	250 °C
Classification temperature (T_c)	230 °C	255 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

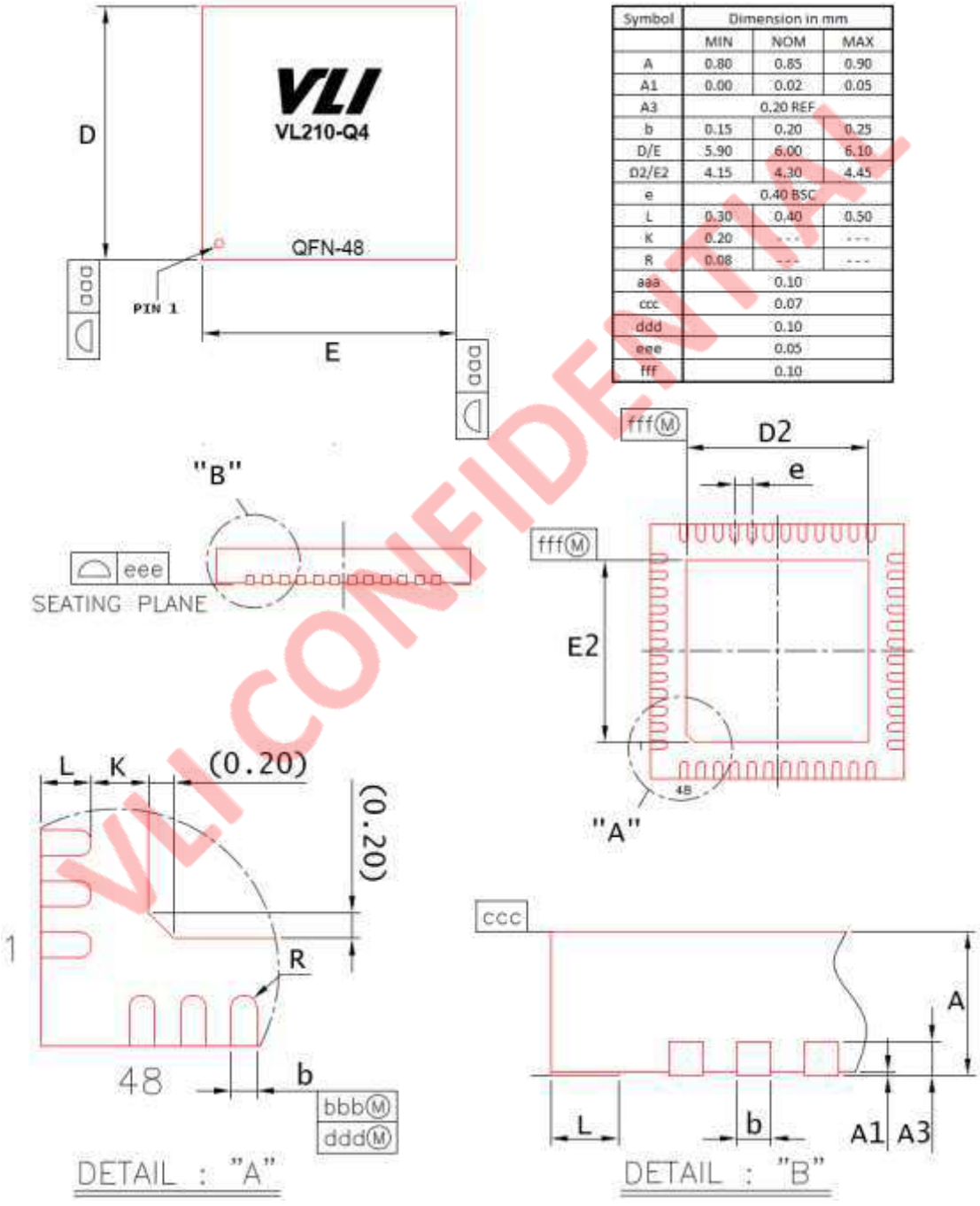
Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug).

Figure 5 - Reflow

Package Mechanical Specifications (QFN-48)

Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	255	°C
Max Time within 5°C of Tp	30	seconds



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	5.90	6.00	6.10
D2/E2	4.15	4.30	4.45
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.08	---	---
aaa		0.10	
ccc		0.07	
ddd		0.10	
eee		0.05	
fff		0.10	

Figure 6 - Mechanical Specification: QFN-48 6x6x0.85 mm Package

Package Top Side Marking & Ordering Information

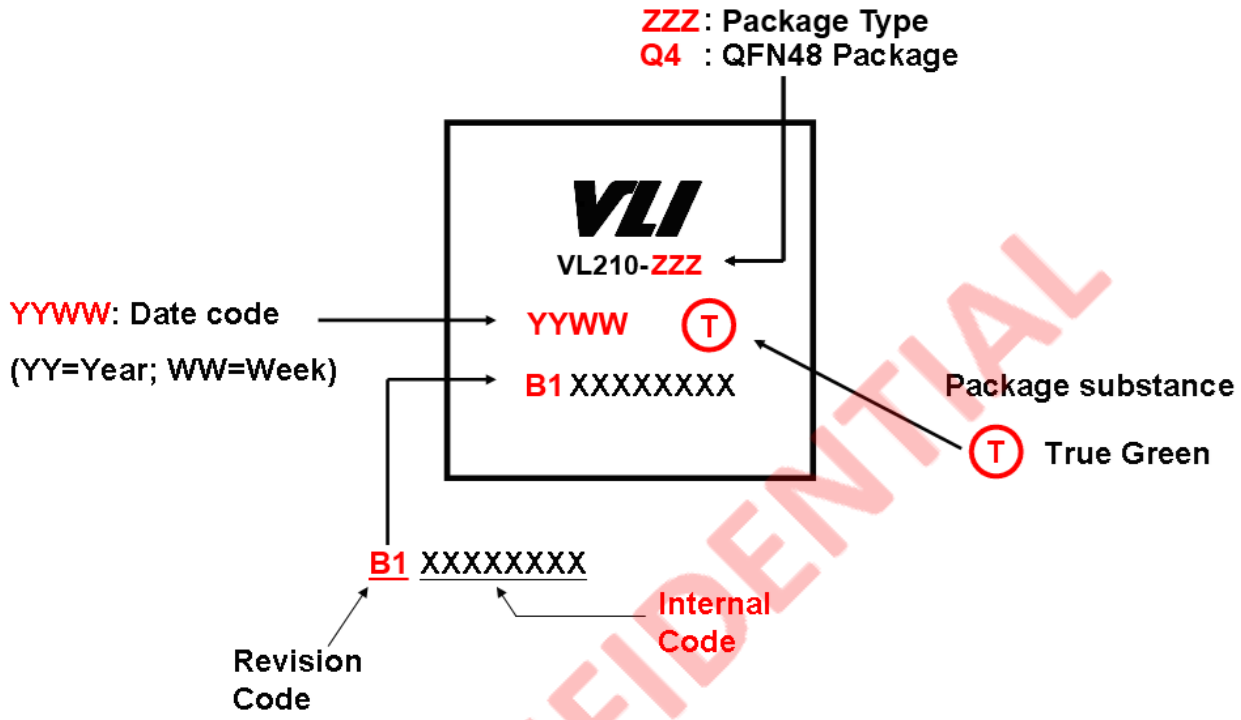


Figure 7 - Package Top Side Marking

Ordering Information	Description	Package Type
VL210-Q4	1SS 3HS Hub: 1x USB 3.0 & 3x USB 2.0	QFN48 6x6 mm

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