Data Sheet

VT1613

2-Channel AC'97 Codec

Revision 1.0
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	12/6/04	Initial external release	JM

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VT1613

2-Channel AC'97 Codec

PRODUCT FEATURES

- **AC'97 V2.3 Audio Codec**
  - Fully compliant with AC'97 Specification, Revision 2.3
- **High Audio Quality**
  - Variable sampling rate converters
  - 16-bit independent rate ADC architecture
  - 18-bit independent rate DAC architecture
  - Integrated Headphone Amps with mute at Front outputs.
- **Various Output Format**
  - 96KHz DAC for 2 channels
  - 48KHz ADC
  - Integrated S/PDIF TX with 96K, 48K, 44.1K and 32KHz support
  - Integrated S/PDIF RX with 48K, 44.1K and 32KHz support
- **Added-on Function**
  - 1 integrated MIC biasing transistors
  - Add 1.5dB analog gin boost to the headphone Amplifier
  - 2 Microphones
  - Add GPIO interrupt capability
  - 1 GPIO pin
  - Direct-Play feature: Play CD through OP Amp of Front Channels
    - Analog and Digital power state to select direct-play mode or normal mode
    - Play CD during PC power off
- **Power**
  - EAPD pin support
  - Integrated Vref_out power down feature
  - Integrated Clean-ON™ Power-up de-Pop
  - SNR exceeds 90dB
  - Low power consumption mode
  - 3.3V or 5V analog, 3.3V digital power supply
- **Package**
  - Pin compatible with VT1612A 2-Channel AC'97 Codec
  - 48-Pin LQFP Package

OVERVIEW

VIA Technologies' VT1613 18-bit audio codec conforms to the AC'97 Specification, Revision 2.3 and S/PDIF Input / Output specifications. The VT1613 integrates Sample Rate Converters on all channels. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems.

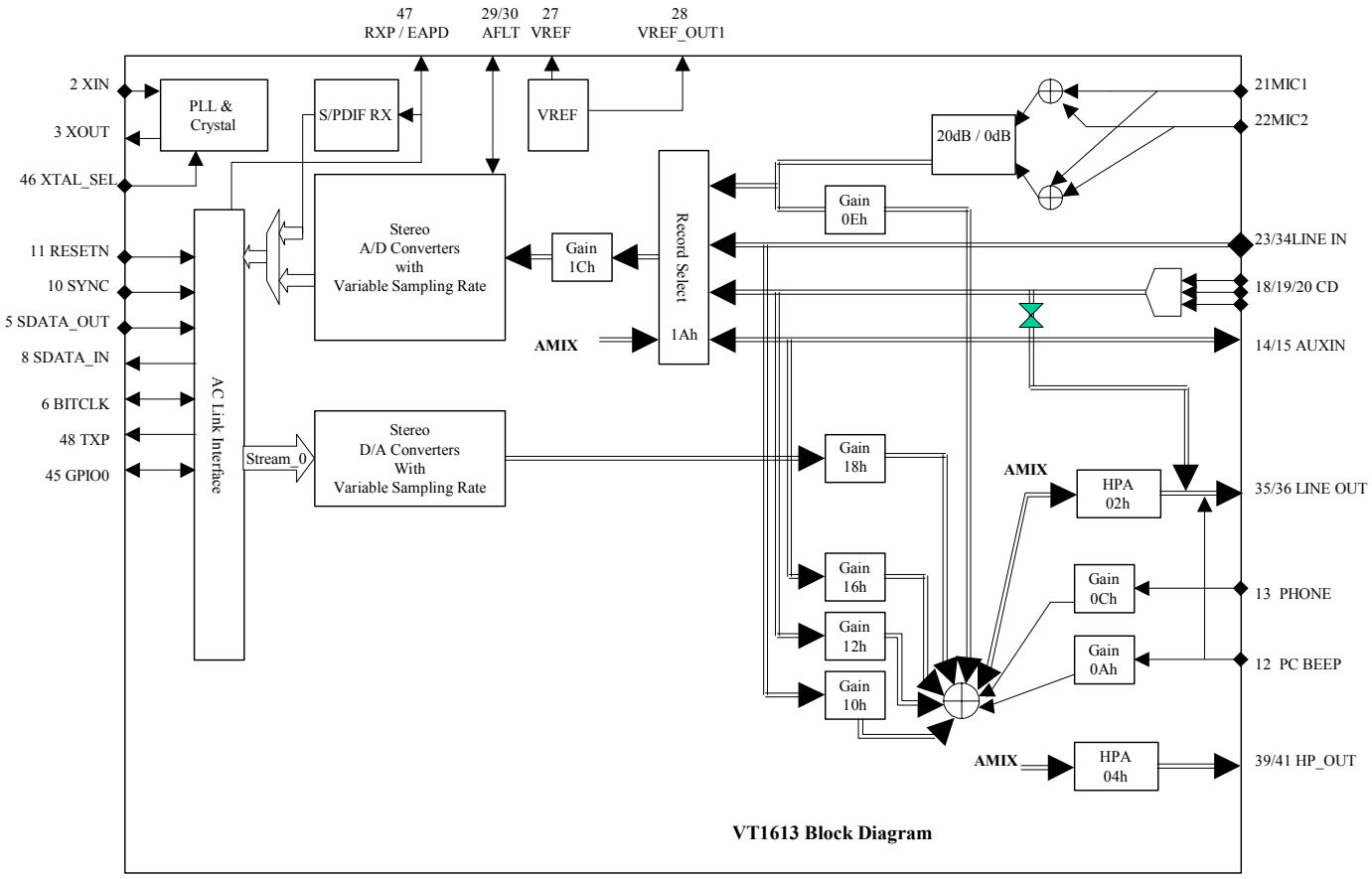


Figure 1. Functional Block Diagram

Pin Diagram

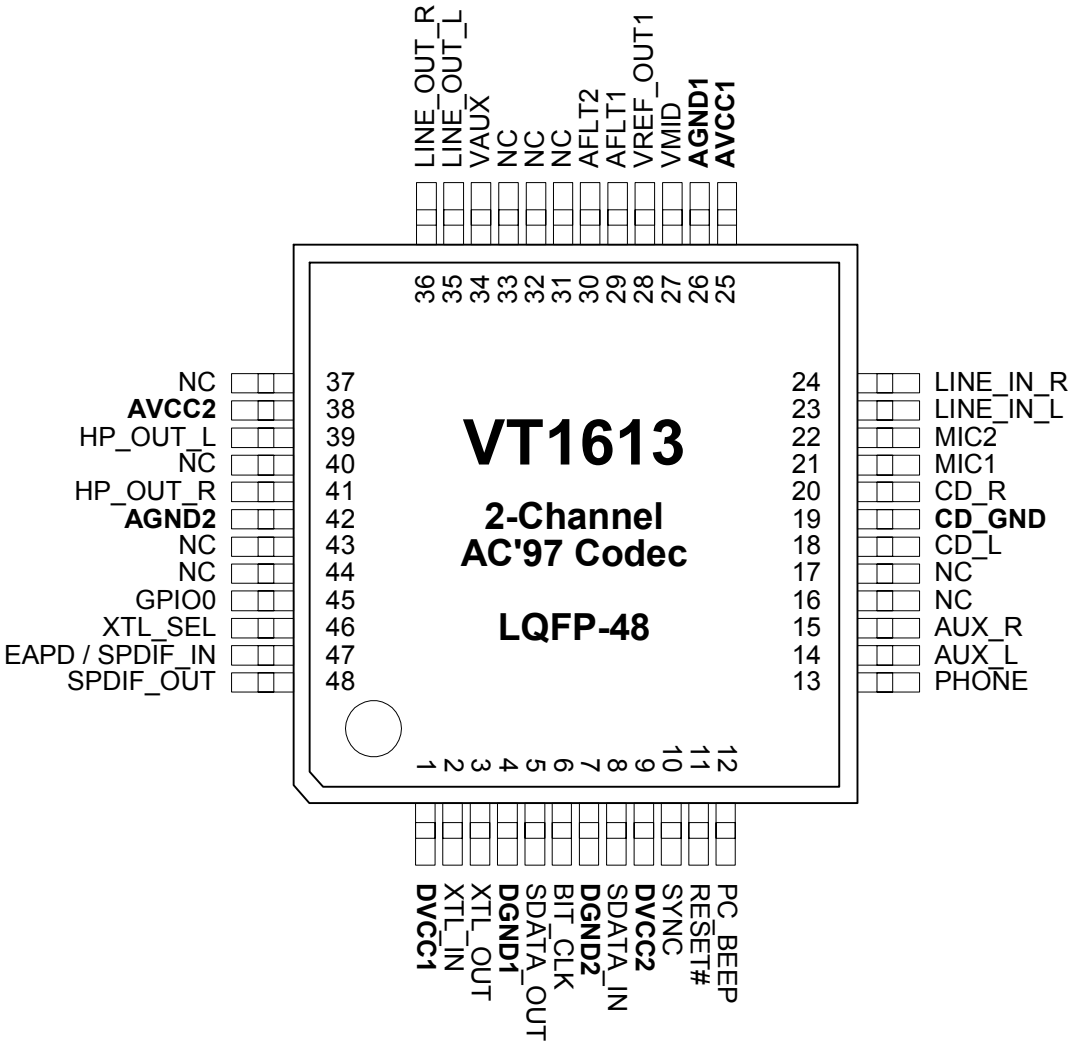


Figure 2. VT1613 Pin Diagram (Top View)

Pin List

Table 1. Pin List (Listed by Pin Name)

Pin#	Pin Name	Type	Pin#	Pin Name	Type
29	AFLT1	O	21	MIC1	I
30	AFLT2	O	22	MIC2	I
26	**AGND1**	**P**	16-17, 31-33, 37, 40, 43-44	NC	—
42	**AGND2**	**P**	12	PCBEEP	I
14	AUX_L	I	13	PHONE	I
15	AUX_R	I	11	RESET#	I
25	**AVCC1**	**P**	8	SDATA_IN	IO
38	**AVCC2**	**P**	5	SDATA_OUT	IO
6	BIT_CLK	IO	48	SPDIF_OUT	O
19	CD_GND	I	10	SYNC	IO
18	CD_L	I	34	VAUX	I
20	CD_R	I	27	VMID	I
4	**DGND1**	**P**	28	VREF_OUT1	O
7	**DGND2**	**P**	2	XTL_IN	I
1	**DVCC1**	**P**	3	XTL_OUT	O
9	**DVCC2**	**P**	46	XTL_SEL	IO
47	EAPD / SPDIF_IN	IO			
45	GPIO0	IO			
39	HP_OUT_L	O			
41	HP_OUT_R	O			
23	LINE_IN_L	I			
24	LINE_IN_R	I			
35	LINE_OUT_L	O			
36	LINE_OUT_R	O			

Note: I = Input, O = Output, P = Power / Ground, A = Analog

Pin Descriptions

Table 2. Pin Descriptions

Pin #	Pin Name	Type	Description
1	**DVCC1**	P	Digital Supply Voltage, 3.3V only
2	**XTL_IN**	I	24.576 MHz Crystal or 24.576M/14.318MHz clock input
3	**XTL_OUT**	O	24.576 MHz Crystal
4	**DGND1**	P	Digital Ground
5	**SDATA_OUT**	IO	AC'97 Serial Data Input Stream
6	**BIT_CLK**	IO	12.288 MHz Serial Data Clock (Internal pulled low).
7	**DGND2**	P	Digital Ground
8	**SDATA_IN**	IO	AC'97 Output Stream (Internal pulled low).
9	**DVCC2**	P	Digital Supply Voltage, 3.3V only
10	**SYNC**	IO	48 KHz Fixed Rate Sync Pulse / LRCLK
11	**RESET#**	I	AC'97 Master Reset
12	**PC_BEEP**	I	PC Speaker Beep Pass Through
13	**PHONE**	I	Telephony Subsystem Speakerphone
14	**AUX_L**	IO	Auxiliary Audio Left Channel / Surround Back Left Output
15	**AUX_R**	IO	Auxiliary Audio Right Channel / Surround Back Right Output
16-17	NC	—	No Connect
18	**CD_L**	I	CD Audio Left Channel
19	**CD_GND**	I	CD Audio Analog Ground
20	**CD_R**	I	CD Audio Right Channel
21	**MIC1**	I	Desktop Microphone
22	**MIC2**	I	Second Microphone
23	**LINE_IN_L**	I	Line In Left Channel
24	**LINE_IN_R**	I	Line In Right Channel
25	**AVCC1**	P	Analog Supply Voltage, 5V or 3.3V
26	**AGND1**	P	Analog Ground
27	**VMID**	I	Mixer Reference Voltage
28	**VREF_OUT1**	O	Reference Voltage Output
29	**AFLT1**	O	Left Channel Anti-Aliasing Filter Capacitor
30	**AFLT2**	O	Right Channel Anti-Aliasing Filter Capacitor
31-33	NC	—	No Connect
34	**VAUX**	I	Power-off CD enable
35	**LINE_OUT_L**	O	Line Out Left Channel (with built-in HP driver)
36	**LINE_OUT_R**	O	Line Out Right Channel (with built-in HP driver)
37	NC	—	No Connect
38	**AVCC2**	P	Analog Supply Voltage, 5V or 3.3V
39	**HP_OUT_L**	O	HP Out Left Channel
40	NC	—	No Connect
41	**HP_OUT_R**	O	HP Out Right Channel
42	**AGND2**	P	Analog Ground
43-44	NC	—	No Connect
45	**GPIO0**	IO	GPIO0 (Internal pulled high)
46	**XTL_SEL**	IO	Crystal Selection (Internal pulled high)
47	**EAPD / SPDIF_IN**	IO	External Power Amplifier Power Down (Internal pulled high) / SPDIF input
48	**SPDIF_OUT**	O	PCM/Non-Audio Sony/Philips Digital I/F Output (Internal pulled high)

REGISTERS

Register Overview

The following tables summarize all on-chip registers.

Table 3. Register Map

Index	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset	—	—	—	—	—	—	—	ID8	—	ID6	—	—	—	—	—	—
02h	Stereo Output Volume	Mute	—	—	ML4	ML3	ML2	ML1	ML0	—	—	—	MR4	MR3	MR2	MR1	MR0
04h	HP Stereo Output Volume	Mute	—	—	ML4	ML3	ML2	ML1	ML0	—	—	—	MR4	MR3	MR2	MR1	MR0
0Ah	PC Beep Volume	Mute	—	—	—	—	—	—	—	—	—	—	PV3	PV2	PV1	PV0	—
0Ch	Phone Volume	Mute	—	—	—	—	—	—	—	—	—	—	GN4	GN3	GN2	GN1	GN0
0Eh	Mic In Volume	Mute	—	—	GL4	GL3	GL2	GL1	GL0	Mute	20dB	—	GN4	GN3	GN2	GN1	GN0
10h	Line In Volume	Mute	—	—	GL4	GL3	GL2	GL1	GL0	—	—	—	GR4	GR3	GR2	GR1	GR0
12h	CD In Volume	Mute	—	—	GL4	GL3	GL2	GL1	GL0	—	—	—	GR4	GR3	GR2	GR1	GR0
16h	Aux In Volume	Mute	—	—	GL4	GL3	GL2	GL1	GL0	—	—	—	GR4	GR3	GR2	GR1	GR0
18h	PCM Out volume	Mute	—	—	GL4	GL3	GL2	GL1	GL0	—	—	—	GR4	GR3	GR2	GR1	GR0
1Ah	Record Select	—	—	—	—	—	SL2	SL1	SL0	—	—	—	—	—	SR2	SR1	SR0
1Ch	Record Gain	Mute	—	—	—	GL3	GL2	GL1	GL0	—	—	—	—	GR3	GR2	GR1	GR0
20h	General Purpose	—	—	—	—	DRSS1	DRSS0	—	MS	LPBK	—	—	—	—	—	—	—
24h	Audio Int. & Paging	I4	I3	I2	—	I0	—	—	—	—	—	—	—	PG3	PG2	PG1	PG0
26h	Power Down & Status	EAPD	—	PR5	PR4	PR3	PR2	PR1	PR0	—	—	—	—	REF	ANL	DAC	ADC
28h	Extended Audio ID	—	—	—	—	REV1	REV0	—	—	—	—	—	—	—	SPDIF	DRA	VRA
2Ah	Ext. Audio Stat / Control	VCFG	—	—	—	—	SPCV	—	—	—	—	SSA1	SSA0	—	SPDIF	DRA	VRA
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
3Ah	S/PDIF Control	V	DRS	SSR1	SSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/PCM	PRO
5Ah	Vendor Reserved Register	D15	AROMT	DROMT	—	—	BPDC	—	—	INIT	D2AL	—	—	IB1	IB0	EQADC	EQDAC
5Ch	Vendor Reserved Register	VRPD1	BIST	—	—	—	—	—	—	HPE1	—	HPE0	—	—	STMIC	—	SMD
62h	PCI SVID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0
64h	PCI SID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0
66h	S/PDIF RX Status	L	CC6	CC5	CC4	CC4	CC2	CC1	CC0	Mode1	Mode0	Pre2	Pre1	Pre0	COPY	/PCM	PRO
68h	S/PDIF RX Status	Invalid	Lock	Ca1	Ca0	Fs3	Fs2	Fs1	Fs0	Cn3	Cn2	Cn1	Cn0	Sn3	Sn2	Sn1	Sn0
6Ah	S/PDIF RX Control	En	D14	D13	D12	D11	—	D9	D8	—	—	—	—	—	—	D1	SCMS
6Ch	DAC Slot Mapping	FD3	FD2	FD1	FD0	—	—	—	—	—	—	—	—	—	—	—	—

Index	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6Eh	ADC Slot Mapping	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MV
70h	ADC / SPDIF RX Left Peak	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
74h	PLL Setting / Debugging	DAOVF	ADOVF	—	—	—	CLK22M	BOUT	BIN	XIN	TEST2	RDY2	EN2	CS	BYP	RDY1	EN1
76h	Miscellaneous	—	—	MS2R	MS1R	—	—	MS2L	MS1L	L8ITP	CD2SP	TADC	TDAC	—	GDAC	FRONT	—
78h	GPIO Control	GSI	GOS	—	—	—	—	—	GW0	—	—	—	GP0	—	—	—	GC0
7Ah	GPIO Status	—	—	—	—	—	—	—	GIS0	GO0	—	—	—	—	—	—	GI0
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Register Descriptions

The register tables in this section also document the power-on default value ("Default") and access type ("Acc") for each register. All offset and default values are shown in hexadecimal unless otherwise indicated. Access type definitions used are RW (Read / Write), RO (Read / Only), "—" for reserved used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Reset

Index: 00h **Default Value: 0140h / 0140h**

The Reset register is used to configure the hardware to a known state or to read the ID code of the part. ID8 and ID6 are set to 1b to report that the ADC and DAC are 18-bit resolution respectively. Writing data to this register will set all the mixer registers to their default values. For detailed description of the bits set to 0b, please refer to AC'97 Rev. 2.3 spec.

Bit	Attr.	Description
15:9	RO	-Reserved-
8	RO	**18-bit ADC**
7	RO	-Reserved-
6	RO	**18-bit DAC**
5:0	RO	-Reserved-

Stereo Output Control

Index: 02h **Default Value: 8000h / 0000h**

Bit	Attr.	Description
15	RW	**Stereo Output Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Master Output (Left Channel) Volume Control** These five bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Master Output (Right Channel) Volume Control** These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels.

Headphone Stereo Output Control

Index: 04h **Default Value: 8000h / 0000h**

Bit	Attr.	Description
15	RW	**Stereo Output Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Master Output (Left Channel) Volume Control** These five bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Master Output (Right Channel) Volume Control** These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels.

Table 4. Stereo Output Attenuation

	M4	M3	M2	M1	M0	Level (dB)
0	0	0	0	0	0	0.0
1	0	0	0	0	1	-1.5
2	0	0	0	1	0	-3.0
3	0	0	0	1	1	-4.5
4	0	0	1	0	0	-6.0
5	0	0	1	0	1	-7.5
..	..	..	..	..	..	..
..	..	..	..	..	..	..
28	1	1	1	0	0	-42.0
29	1	1	1	0	1	-43.5
30	1	1	1	1	0	-45.0
31	1	1	1	1	1	-46.5

PC Beep Input Volume Control

Index: 0Ah **Default Value: 8000h / 8000h**

Bit	Attr.	Description
15	RW	**PC Beep Input Mute Control** 0: Normal 1: Mute
14:5	RO	-Reserved-
4:1	RW	**PC Beep Input Volume Control** These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[4:1] = 0h. Even though the default of the input volume control is mute, as long as RESET# is active, PC Beep will be passively routed to the line outputs.
0	RO	-Reserved-

Phone Input Volume Control

Index: 0Ch **Default Value: 8008h / 8008h**

Bit	Attr.	Description
15	RW	**Phone Input Mute Control** 0: Normal 1: Mute
14:5	RO	-Reserved-
4:0	RW	**Phone Input Volume Control** These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

MIC Input Volume Control

Index: 0Eh **Default Value: 8808h / 8808h**

Bit	Attr.	Description
15	RW	**MIC Input Mute Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Left Channel Gain Control** These five bits select the gain applied to the LEFT channel of the MIC Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Those bits and bit 7 are only active if STMIC in register 5Ch is set to 1.
7	RW	0: Normal 1: Mute
6	RW	**MIC Boost Control** 0: Fixed 20dB gain disabled 1: Fixed 20dB gain enabled
5	RO	-Reserved-
4:0	RW	**Mic Input Volume Control** These five bits select the gain applied to the Mic Input signal. The gain is programmable from - 34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

Line Input Volume Control

Index: 10h **Default Value: 8808h / 8808h**

Bit	Attr.	Description
15	RW	**Line Input Mute Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Left Channel Gain Control** These five bits select the gain applied to the left channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Right Channel Gain Control** These five bits select the gain applied to the right channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

CD Input Volume Control

Index: 12h **Default Value: 8808h / 8808h**

Bit	Attr.	Description
15	RW	**CD Input Mute Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Left Channel Gain Control** These five bits select the gain applied to the left channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Right Channel Gain Control** These five bits select the gain applied to the right channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

Auxiliary Input Volume Control

Index: 16h **Default Value: 8808h / 8808h**

Bit	Attr.	Description
15	RW	**Auxiliary Input Mute Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Left Channel Gain Control** These five bits select the gain applied to the left channel of the AUX input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Right Channel Gain Control** These five bits select the gain applied to the right channel of the AUX input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

PCM Output Volume Control

Index: 18h **Default Value: 8808h / 0808h**

Bit	Attr.	Description
15	RW	**PCM Output Mute Control** 0: Normal 1: Mute
14:13	RO	-Reserved-
12:8	RW	**Left Channel Gain Control** These five bits select the gain applied to the left channel of the PCM output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.
7:5	RO	-Reserved-
4:0	RW	**Right Channel Gain Control** These five bits select the gain applied to the right channel of the PCM output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels.

Table 5. Stereo Output Attenuation

	G4	G3	G2	G1	G0	Level (dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

Record Select Control

Index: 1Ah **Default Value: 0000h / 0404h**

Bit	Attr.	Description
15:11	RO	-Reserved-
10:8	RW	**Record Source Select (Left Channel) (SL[2:0])** These bits determine the record source for the left channel. **SL2 SL1 SL0 Left Record Source** 0 0 0 MIC 0 0 1 CD (L) 0 1 0 reserved 0 1 1 Aux In (L) 1 0 0 Line In (L) 1 0 1 Stereo Mix (L) 1 1 0 Mono Mix 1 1 1 Phone
7:3	RO	-Reserved-
2:0	RW	**Record Source Select (Right Channel) SR[2:0]** These bits determine the record source for the right channel **SR2 SR1 SR0 Right Record Source** 0 0 0 MIC 0 0 1 CD (R) 0 1 0 reserved 0 1 1 Aux In (R) 1 0 0 Line In (R) 1 0 1 Stereo Mix (R) 1 1 0 Mono Mix 1 1 1 Phone

Record Gain Control

Index: 1Ch **Default Value: 8000h / 0000h**

Bit	Attr.	Description
15	RO	**Record Mute Control** 0: Normal 1: Mute
14:12	RO	-Reserved-
11:8	RW	**Record Gain Control (Left Channel)** These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.
7:4	RO	-Reserved-
3:0	RW	**Record Gain Control (Right Channel)** These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GR[3:0] = 0h.

General Purpose

Index: 20h **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15:12	RO	-Reserved-
11:10	RW	**Double Rate Slot Select (DRSS[1:0])** 00: PCM L, R n+1 data is on slots 10,11 01: PCM L, R n+1 data is on slots 7, 8
9	RO	-Reserved-
8	RW	**MS** (MIC Select)
7	RW	**Loopback Mode** 0: DAC/ADC Loopback disabled 1: DAC/ADC Loopback enabled
6:0	RO	-Reserved-

Audio Interrupt and Paging Mechanism

Index: 24h **Default Value: 0001h / 0001h**

Bit	Attr.	Description
15	RW	**Interrupt Status** 0 Interrupt is cleared 1: Interrupt was generated Interrupt event is cleared by writing a 1 to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the AC link will follow this bit change when interrupt enable (I0) is un-masked. If this bit is set, one or both of I3 or I2 must be set to indicate the interrupt cause.
14:13	RO	**Interrupt Cause** I [2]= 0 - Reserved I [3]= 0 - GPIO status change did not cause interrupt (default) 1: GPIO status change caused interrupt. These bits will indicate the cause(s) of an interrupt. This information should be used to service the correct interrupting event(s). If the Interrupt Status (bit I4) is set, one or both of these bits must be set to indicate the interrupt cause. Hardware must reset these bits back to zero when the Interrupt Status bit is cleared.
12	RO	-Reserved-
11	RW	**Interrupt Enable** 0: Interrupt generation is masked 1: Interrupt generation is un-masked Software should not un-mask the interrupt unless ensured by the AC ’97 controller that no conflict is possible with modem slot 12- GPI functionality. AC ’97 2.2. Compliant controllers will not likely support audio codec interrupt infrastructure.
10:4	RO	-Reserved-
3:0	RW	**Page Selector** 0h: Vendor Specific 1h: Page ID 01(see correspondent definition register 60h-6Fh) 2h-Fh – Reserved Pages This register is used to select a descriptor of 16 word pages between registers 60h. to 6Fh. A value of 0h is used to select vendor specific space to maintain compatibility With AC ’97 2.2 vendor specific registers. System software can determine implemented pages by writing the page number and reading the value back. If the value read back does not match the value written, the page is not implemented. All implemented pages must be in consecutive. (i.e., page 2h cannot be implemented without page 1h)

Power Down and Status

Index: 26h **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15	RW	**Enable Amplifier Power Down** The signal polarity at pin 47, EAPD is identical to bit description 0: External Power Amplifier active 1: Powerdown External Power Amplifier
14	RW	-Reserved-
13:8	RO	**Power Down Mode Bits PR[5:0]** These read/write bits are used to control the power down states of the VT1613. Each power down function bit is enabled by setting the respective bit high. When either PR2 or PR3 is 1, the analog mixer circuit is powered down. Particularly, PR5 has no effect unless PR0, PR1 and PR4 are all set to "1". This implies that the codec can be woken up by a warm reset, because warm reset clears PR4, which in turn disables the function of PR5. The register bit, however will not be cleared by a warm reset. The power down modes controlled by each bit is described in the table below. **Bit Function** PR0 ADC and Mux Powerdown PR1 DAC Powerdown PR2 Mixer Powerdown (VREF on) PR3 Mixer Powerdown (VREF off) PR4 AC-Link Powerdown (BIT_CLK off) PR5 Internal Clock Disabled
7:4	RO	-Reserved-
3	RO	1: Vref at normal level
2	RO	1: Analog circuit (mixer, volume control…etc) ready
1	RO	1: DAC ready to accept data
0	RO	1: ADC ready to transmit data

Note: Bit[3:0] are status bits. These bits are used to monitor the readiness of some sections of the VT1613. Reading a "1" from any of these bits would be an indication of "ready" status.

Table 6. Power Down Control Mapping Table

	ADC	DAC	Mixer	Vref	AC-Link	Internal Clock	EAPD	HP Amp 1	HP Amp 1
PR0	PD								
PR1		PD							
PR2			PD					PD	PD
PR3	PD	PD	PD	PD				PD	PD
PR4	PD	PD			PD				
PR5	PD	PD			PD	PD			
PR7							High		
5C[7]									PD
5C[5]								PD	

Extended Audio ID

Index: 28h **Default Value: 097Ch**

Bit	Attr.	Description
15:12	RO	-Reserved-
11:10	RO	**AC'97 Revision ID** REV[1:0]=10 indicates Codec is AC '97 revision 2.3 compliant.
9:3	RO	-Reserved-
2	RO	**Sony/Philips Digital Audio Interface** 1: Feature implemented in compliance to "S/PDIF Output for AC '97, Rev 1.0"
1	RO	**Double Rate PCM Audio** 1: Feature implemented in compliance to AC '97 2.2 Appendix A
0	RO	**Variable Sampling Rate PCM Audio** 1: Feature implemented in compliance to AC '97 2.2 Appendix A

Extended Audio Status/Control

Index: 2Ah **Default Value: 3830h**

Bit	Attr.	Description
15	RW	**S/PDIF Valid Configuration (VCFG)** Determines S/PDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF "Validity" flag, which is bit 28 transmitted in each S/PDIF sub-frame.
14:11	RO	-Reserved-
10	RO	**S/PDIF Configuration Valid** 0: S/PDIF configuration (SPSA, SSR, DAC rate, DRS) invalid (not supported) 1: S/PDIF configuration (SPSA, SSR, DAC rate, DRS) valid (supported)
9:6	RO	-Reserved-
5:4	RW	**S/PDIF Slot Assignment** These bits determine the S/PDIF data source from AC-link slot selection. The default state reflects the pervasive design feature of common AC'97 digital controllers supporting slots 3 & 4. 00: AC-link slots 3 & 4 (front stereo pair) 01: AC-link slots 7 & 8 (surround pair) 10: AC-link slots 6 & 9 (LFE & Center pair) 11: AC-link slots 10 &11 (default):
3	RO	-Reserved-
2	RW	**Sony/Philips Digital Audio Interface** 0: The S/PDIF transmitter is off by default 1: Set this bit to turn on the S/PDIF transmitter.
1	RW	**Double Rate Mode Control** 0: Disable 1: Enable Double-Rate Audio mode in which data from PCM L and PCM R in output slots 3 and 4 is used in conjunction with PCM L (n+1) and PCM R (n+1) data, to provide DAC streams at twice the sample rate designated by the PCM Front Sample Rate Control Register.
0	RW	**Variable Sampling Rate Mode control** 0: Fixed 48 KHz sampling rate 1: Enable VSR

Table 7. SPDIF Validity and Configuration Mapping Table

V Index 3A[15]	VCFG Index 2A[15]	S/PDIF Channel Status Bit 28	S/PDIF Data Bit
0	**0**	**0**: if valid data is available to transfer **1**: if no valid data is available to transfer	Valid data, or repeat the previous data if no valid data is available
0	**1**	**0**	Valid data, or 24'b0 if no valid data available
1	**0**	**1**	Repeat the previous data
1	**1**	**1**	24'b0

PCM Front , Surround and Center DAC Sample Rate

Index: 2Ch **Default Value: BB80h / BB80h (fixed)**

Bit	Attr.	Description
15:0	RW	**Main stereo + Center or all DAC Sample Rate (in Hz)** 16-bit unsigned value representing the sample rate. The default value is 48 KHz (48000 = BB80h). This register controls all eight DAC output rate providing a sample accurate synchronization among the channels. Registers 2Eh and 30h are read only and always reflect the setting in register 2Ch when read back. The value is reset to BB80h if VRA bit in register 2A is cleared to 0.

PCM ADC Sample Rate

Index: 32h **Default Value: BB80h / BB80h (fixed)**

Bit	Attr.	Description
15:0	RW	**ADC Sample Rate (in Hz)** 16-bit unsigned value representing the sample rate. The default value is 48 KHz (48000 = BB80h). The value is reset to BB80h if VRA bit in register 2A is cleared to 0.

Valid Sampling Rate	Value in Registers
48K	BB80h
44.1K	AC44h
32K	7D00h
24K	5DC0h
22.05K	5622h
16K	3E80h
12K	2EE0h
11.025K	2B11h
8K	1F40h

Note: When a sampling rate value programmed is not supported, the hardware will choose a rate that's close to the desired rate. The driver should always read back the register content to see if the programmed rate is supported.

Also, in I2S mode, the sampling rates are fixed at 48K (BB80h).

S/PDIF Control

Index: 3Ah **Default Value: 2000h / 2000h**

This read / write register controls the S/PDIF functionality. The register manages the bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written when the S/PDIF transmitter is disabled (SPDIF bit at 2Ah_2 is "0"). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

Bit	Attr.	Description
15	RW	**Validity (V)** This bit affects the "Validity flag", bit[28] transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the VCFG bit in the Extended Audio Status and Control register. The behavior of the transmitter is defined in the definition of the Extended Audio Status and Control Register (Index 2Ah)
14	RW	**Double Rate S/PDIF** When DRS is enabled "1" and SPSA is configured {"01", "10", or "11"} the S/PDIF transmitter uses AC-link slots 3&4 + {7&8, 6&9, or 10&11} to supply data at Fs = 96 kHz. *Note: Double rate S/PDIF should only be enabled if register 6E[15:12] = 3'b0011, that is, the front L/R jack is plugged into pin 35/36.*
13:12	RW	**S/PDIF Sample Rate** 00: 44.1KHz 01: 10: 48KHz (default) 11 32KHz
11	RW	**Generation Level** Programmed according to IEC standards.
10:4	RW	**Category Code** Programmed according to IEC standards.
3	RW	**Preemphasis** 0: Default is no Preemphasis. 1: Indicates filter preemphasis is 50/15µs.
2	RW	**Copyright** 0: Copyright is not asserted (default). 1: Indicates copyright is asserted.
1	RW	**Non-Audio Samples** 0: Indicates samples are linear PCM suitable for direct conversion to audio playback. . 1: Set this bit for transmitting non-PCM audio samples such as AC-3.
0	RW	**Professional** 0: Indicates Consumer mode (default). 1: Set Professional mode. Set this bit in conjunction with /PCM bit (above) for AC-3.

Vendor Reserved

Index: 5Ah **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15	RW	**In AC'97 mode, this bit is fixed at 0.** **In I2S mode, this bit is readable / writable.** 0: I2S data format 1: Left Justified data format
14	RW	**ADC ROM Test Mode** 0: Normal 1: Enable ADC ROM test mode
13	RW	**DAC ROM Test Mode** 0: Normal 1: Enable DAC ROM test mode
12:11	RO	-Reserved-
10	RW	**ADC DC-offset Removal Control** The default setting of "0" ensures that the circuit is disabled at power up. When set to "1", the DC-offset cancellation circuit will be enabled. This helps to maximize recording quality by removing white noise. The transfer function of this digital high-pass filter is: $H(z) = (1-Z^{-1}) / (1-0.9995Z^{-1})$
9:8	RW	-Reserved-
7	RW	**RAM Test Mode Initialization** When this bit is set to 1, the internal RAM address will be updated every BITCLK cycle, and the storage elements in ALU and sigma-delta circuits are reset to 0. This is for testing only and should not be set during normal operation.
6	RW	**D2A Loopback Test Mode** When this bit is set to 1, the DAC sigma delta output is routed back to the ADC sigma-delta input. This is for testing only and should not be set during normal operation.
5:4	RO	-Reserved-
3:2	RW	**Analog Current Setting Bits** Normally these bits should be left at default when analog operating at 5V supply. The four possible settings adjust the power consumption of the analog section. The power-up default 00b sets the codec for the best overall analog performance at 5V. At 3.3V analog supply, 10b should be set for the lowest power instead of default 00b. This mode is desirable for system designs with limited power budget such as battery operated portable devices. Setting to 11b puts the codec to its best A- A mixer performance overall. 00: Normal (1X) 01: Reduced (4/5 X) 10: Power Miser (2/3 X) 11: Enhanced (4/3 X)
1	RW	**ADC Left / Right Data Comparison** Used together with D2AL bit for test mode. If this bit is read 1, it means the left and right channels from the ADC have exactly the same data.
0	RW	**DAC Left / Right Data Comparison** Used together with D2AL bit for test mode. If this bit is read 1, it means the left and right channels from the DAC sigma-delta output have exactly the same data.

Vendor Reserved

Index: 5Ch **Default Value: 00A9h / 00A9h**

Bit	Attr.	Description
15	RW	**Vrefout1 Power Down** 0: Vrefout1 enabled 1: Vrefout1 power down
14	RW	**BIST Enable** 0: Normal 1: This bit has to be set to 1 before any test mode bits are enabled
13:8	RO	-Reserved-
7	RW	0: Normal function. The enhanced headphone amplifiers at pin 39/41 are enabled 1: The enhanced headphone amplifier at pin 39/41 are disabled
6	RO	-Reserved-
5	RW	0: Normal function. The enhanced headphone amplifiers at pin 35/36 are enabled 1: The enhanced headphone amplifier at pin 35/36 are disabled
4:3	RO	-Reserved-
2	RW	**Stereo MIC Volume Control** 0: Mono MIC volume control in regsiter 0Eh. Bit[12:8] in register 0Eh should be cleared to 0 1: 1: Bit [12:8] of register 0Eh controls the left channel of MIC, and bit[4:0] of register 0Eh controls the right channel of MIC.
1	RO	-Reserved-
0	RW	**Soft-Mute Disable** 0: Soft-mute is enabled 1: Soft-mute is disabled

ADC Peak Meter

Index: 70h **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15:0	RW	**Peak Meter Data for left channel** The data reflect the peak value of the ADC / SPDIF RX left channel. The data is reset to 0 after each read.
7:0	RW	**Peak Meter Data for right channel** The data reflect the peak value of the ADC / SPDIF RX right channel. The data is reset to 0 after each read.

PLL Setting

Index: 74h **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15	RO	**DAC Digital Filter Overflow Bit.** Cleared by Rx. 5A[7]
14	RO	**ADC Digital Filter Overflow Bit.** Cleared by Rx. 5A[7]
13:11	RO	-Reserved-
10	RW	22.5792MHz is driven from GPI[2] pin for testing when set to 1
9:8	RW	-Reserved- (BITCLK test mode)
7	RW	**XIN Source Available** 0: XIN pin has no input 1: XIN pin has either 14.318MHz or 24.576MHz input. Software can write a 0 to clear this register before reading. In the case when BITCLK is driven by the audio controller and XIN has no input, the sampling rate of 32K, 16K and 8K cannot be supported because they require 24.576MHz clock source.
6	RW	**Test PLL2** 1: The output of PLL2 is sent out through SDATA_IN pin for measurement
5	RO	**PLL2 Ready** 1: Indicates PLL2 ready
4	RW	**PLL2 Enable** 0: Disable PLL2 1: Enable 12.288M ~ 22.5792M PLL. PLL2 needs to be enabled if the sampling rate is 44.1K, 22.05K or 11.025KHz
3	RW	**PLL Bypass Control Select** 0: Hardware Control 1: Software Control
2	RW	**SW Control PLL Bypass** 1: Bypass PLL1
1	RO	**PLL Ready** 1: Indicates PLL1 ready
0	RO	**PLL1 Enable** 0: Indicates that Pin 46 is pulled high or floating. It reflects 14.318M ~ 24.576M PLL Bypass. 1: Enable 14.318M ~ 24.576M PLL.

Note: Both PLL are disabled in I2S mode.

Miscellaneous

Index: 76h **Default Value: 1182h / 1182h**

Bit	Attr.	Description
15:14	RO	-Reserved-
13	RW	**MIC2 to right channel Control** 0: Disabled 1: Enabled *Note: This bit is set to 1 if Rx20[8] is 1 for backward compatibility*
12	RW	**MIC1 to right channel Control** 0: Disabled 1: Enabled (default) *Note: This bit is set to 0 if Rx 20[8] is 1 for backward compatibility*
11:10	RO	-Reserved-
9	RW	**MIC2 to left channel Control** 0: Disabled 1: Enabled *Note: This bit is set to 1 if Rx20[8] is 1 for backward compatibility*
8	RW	**MIC1 to left channel Control** 0: Disabled 1: Enabled (default) *Note: This bit is set to 0 if Rx20[8] is 1 for backward compatibility*
7	RW	**Test Mode** 0: Disable 8X interpolation 1: Normal mode
6	RW	**CD input to S/PDIF out** 0: S/PDIF output data comes from SDATA_OUT 1: S/PDIF output data comes from ADC
5	RW	**Test ADC Mode** 0: Normal mode 1: The 4 bits from the analog sigma-delta output of the front left channel is sent out through pin 45 to 48
4	RW	**Test DAC Mode** 0: Normal mode 1: The 3-bit digital sigma-delta output is input from pin 46 to 48
3	RO	-Reserved-
2	RW	**Test DAC Mode** 0: Normal mode 1: The 3-bit digital sigma-delta output is sent out from pin 46 to 48
1	RW	**When bit 2 above is set to 1, bit 1 is used to select which DAC output is selected.** 0: Surround left DAC data is sent out from pin 46 to 48 1: Front left DAC data is sent out from pin 46 to 48
0	RO	-Reserved-

GPIO Control

Index: 78h **Default Value: 0070h / 0070h**

Bit	Attr.	Description
15	RW	**GPIO Interrupt Status Indication in SDATA_IN** 0: The status of GPIO and its valid tag are not indicated in SDATA_IN. 1: The status of GPIO and its valid tag are indicated in SDATA_IN.
14	RW	**GPIO output select** 0: GPIO output is controlled by Rx7A[7]. 1: GPIO output is controlled by SDATA_OUT Slot12 bit4.
13:9	RO	-Reserved-
8	RW	**GPIO Pin interrupt enable when GPIO is used as input (GW[0])** 0: Disable 1: Enable
7:5	RO	-Reserved-
4	RW	**GPIO Interrupt Polarity** 0: Low to High transition 1: High to Low transition
3:1	RO	-Reserved-
0	RW	**GPIO Pin Configuration** 0: GPIO_0 pin is used as input 1: GPIO_0 pin is used as output

GPIO Status

Index: 7Ah **Default Value: 0070h / 0070h**

Bit	Attr.	Description
15:9	RO	-Reserved-
8	RO	**GPIO Input Status (When GPIO is used as input)** 0: GPIO[n] is driven low 1: GPIO[n] is driven high
7	RW	**GPIO Output Control** 0: Drive GPIO low 1: Drive GPIO high
6:1	RO	-Reserved-
0	RWC	**GPIO Interrupt Status (When GPIO is used as input)** 0: No GPIO interrupt 1: GPIO interrupt Write 1 to clear this status bit.

Vendor Identification

Index: 7Ch **Default Value: 5649h / 5649h**

Bit	Attr.	Description
15:0	RO	The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the VT1613. The Vendor ID Code (in ASCII format) is equal to “VIA”, where: F[7:0] Upper Byte (Index 7Ch) D[15:8] = V S[7:0] Lower Byte (Index 7Ch) D[7:0] = I T[15:8] Upper Byte (Index 7Eh) D[15:8] = A

Revision Identification

Index: 7Eh **Default Value: 4120h / 4120h**

Bit	Attr.	Description
15:0	RO	The upper byte of this register is used in conjunction with index register 7Ch to make up the Vendor ID code for the VT1613. The lower byte identifies VT1613 and its revision code. T[15:8]: See description in Vendor Identification Register. REV[7:0] Revision ID "20" : VT1613 identification and revision number

Vendor Defined Register (Page ID = 00h)

S/PDIF RX Channel Status

Index: 66h **Default Value: X000h / X000h**

Bit	Attr.	Description
15	RO	**Generation Level**
14:8	RO	**Category Code**
7:6	RO	**Mode[1:0]**
5:3	RO	**Preemphasis**
2	RO	**Copyright**
1	RO	**Non-Audio Samples**
0	RO	**Professional Mode**

S/PDIF RX Channel Status

Index: 68h **Default Value: X000h / X000h**

Bit	Attr.	Description
15	RO	**Invalid Status** 0: Data X and Y are valid 1: At least one of data X or Y is invalid
14	RO	**Lock Status** 0: S/PDIF RX unlocked 1: S/PDIF RX locked
13:12	RO	**Clock Accuracy**
11:8	RO	**Sample Frequency in channel status** 0000: 44.1KHz 0010: 48 KHz 0011: 32 KHz Others: reserved
7:4	RO	**Channel Number**
3:0	RO	**Source Number**

Table 8. Channel Status Bit from S/PDIF RX in Consumer Mode

0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Pro	/PCM	COPY	Pre0	Pre1	Pre2	Mode0	Mode1
8	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CC0	CC1	CC2	CC3	CC4	CC5	CC6	Level
16	**17**	**18**	**19**	**20**	**21**	**22**	**23**
Sn0	Sn1	Sn2	Sn3	Cn0	Cn1	Cn2	Cn3
24	**25**	**26**	**27**	**28**	**29**	**30**	**31**
Fs0	Fs1	Fs2	Fs3	Ca0	Ca1	0	0

S/PDIF RX Control

Index: 6Ah **Default Value: 0000h / 0000h (fixed)**

Bit	Attr.	Description
15	RW	**S/PDIF RX Enable** 0: Disable 1: Enable When S/PDIF RX is enabled, pin 47 becomes input mode for S/PDIF RX, and EAPD function is not available.
14	RW	**S/PDIF RX Monitoring** 0: Disable 1: S/PDIF RX data is added to PCM data and sent to DAC. Note: The DAC output may not sound correctly in this mode because the S/PDIF RX rate is not synchronous with the PCM rate, and the mixed data may be clipped.
13	RW	**S/PDIF TX to S/PDIF RX Internal Loopback** (for testing only) 0: Disable 1: Enable
12	RW	**SDATA_IN Source Select** 0: SDATA_IN is from ADC data 1: SDATA_IN is from S/PDIF RX data
11	RW	**S/PDIF RX Monitoring** 0: Disable 1: S/PDIF RX data is added to PCM data and sent to DAC. Note: The DAC output may not sound correctly in this mode because the S/PDIF RX rate is not synchronous with the PCM rate, and the mixed data may be clipped.
10	RW	-Reserved- (S/PDIF RX Test mode for debug only)
9:8	R	**S/PDIF RX Test Mode. RX Rate Decode Result.** 00: 44.1K 10: 48K 11: 32K
7:2	RW	-Reserved- (S/PDIF RX test mode for bi-phase and preamble decode)
1	RW	**RX Signal Monitoring** 0: Normal 1: The S/PDIF RX signal seen by the RX circuit is sent out from pin 45 (GPIO 0)
0	RW	**Clear S/PDIF TX Data for SCMS** 0: Normal 1: Clear S/PDIF TX data to 0 if the data is marked as invalid

Extended Codec Registers (Page ID = 01h)

PCI SVID

Index: 62h **Default Value: FFFFh / FFFFh**

Bit	Attr.	Description
15:0	RW	**PCI Sub System Vendor ID** This field provides the PCI Sub System Vendor ID of the Audio or Modem Sub Assembly Vendor (i.e., CNR manufacturer, Motherboard Vendor). This is NOT the codec vendor PCI Vendor ID, nor is it the AC '97 controller PCI Vendor ID. If not implemented this register is read only and must return value of 0x0h when read. If the register is implemented and data is not available it should return FFFFh.

PCI SID

Index: 64h **Default Value: FFFFh / FFFFh**

Bit	Attr.	Description
15:0	RW	**PCI Vendor ID** This field provides the PCI Sub System ID of the Audio or Modem Sub Assembly (i.e., CNR Model, Motherboard SKU). This is NOT the codec vendor PCI ID, nor is it the AC '97 controller PCI ID. Information in this field must be available for AC '97 controller reads when codec ready is asserted in AC link. If not implemented this register is read only and must return value of 0x0h when read. If the register is implemented and data is not available it should return FFFFh.

DAC Slot Mapping

Index: 6Ch **Default Value: 376Ah / 376Ah**

Bit	Attr.	Description
15:12	RW	**Front Channel DAC Slot Mapping Control** Control the mapping of the 1st DAC pair (generally the front speakers and headphone), which defaults to slots 3 and 4.
11:0	RO	-Reserved-

ADC Slot Mapping

Index: 6Eh **Default Value: 0000h / 0000h**

Bit	Attr.	Description
15:1	RO	-Reserved-
0	RO	**Mapping Valid** Indicates that the values programmed into page offsets 6Ch are valid.

ELECTRICAL SPECIFICATIONS

Digital DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit
DV_{dd}	Digital Power Supply	3.135	3.3	3.465	V
V_{IN}	Input Voltage Range	-0.3		DV_{CC} + 0.3	V
V_{IL}	Input Low Voltage			0.35 x DV_{dd}	V
V_{IH}	Input High Voltage	0.65 x DV_{dd}			V
V_{OH}	Output High Voltage	0.9 x DV_{dd}			V
V_{OL}	Output Low Voltage			0.1 x DV_{dd}	V
	Input Leakage Current (AC-Link inputs)	-10		10	uA
	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10		10	uA
	Input / Output Pin Capacitance			7.5	pF

Analog Performance Characteristics

Analog Input

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage				
Line Inputs		1.0		Vrms
Miscellaneous Inputs with 20dB Gain		0.1		
Miscellaneous inputs with 0dB Gain		1		
Input Impedance	10			Kohm
Input Capacitance		7.5		pF

Analog Output

Parameter	Min	Typ	Max	Unit
Full Scale Output Voltage				
Line Output		10		Vrms
Headphone Output			1.41	
Analog S/N				
CD to LINE_OUT		90		dB
Other to LINE_OUT		90		
Analog Frequency Response	20		20000	Hz
Vrefout		2.25~2.75		V

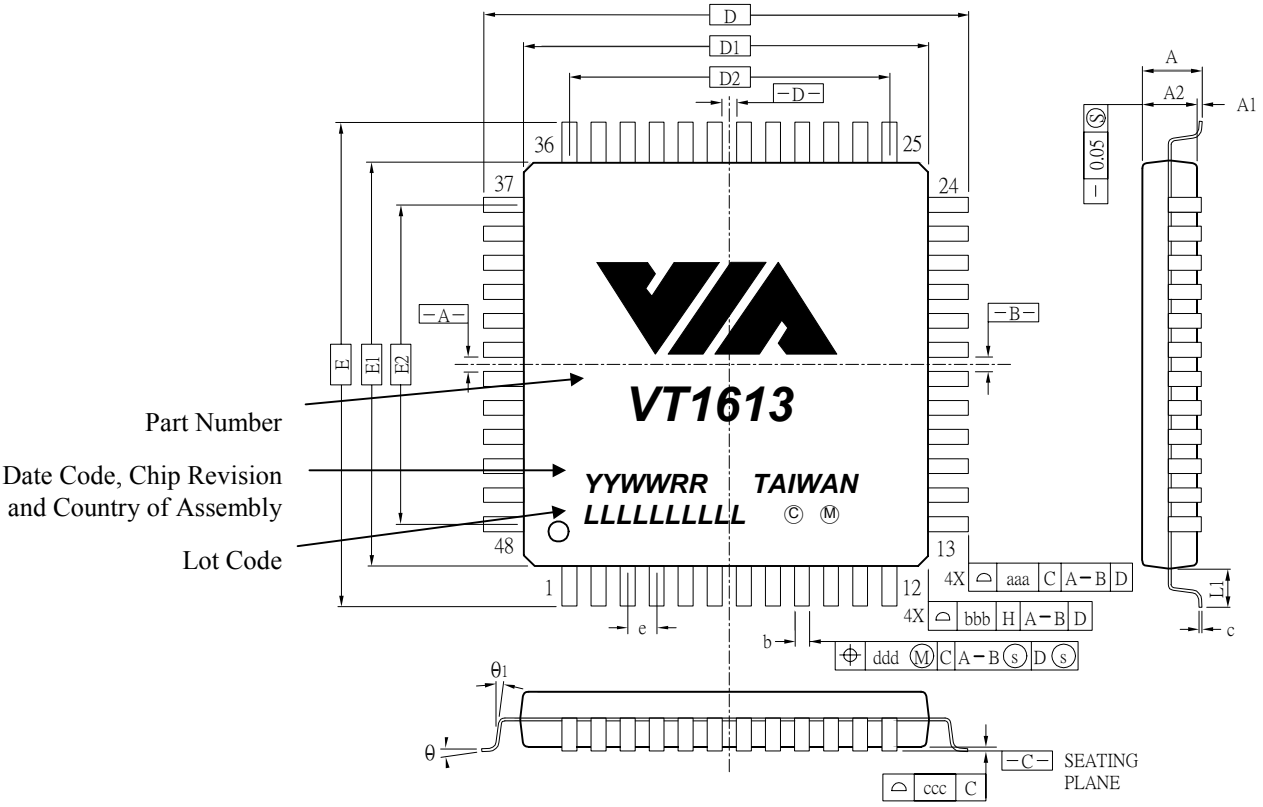
ADC Converters

Parameter	Min	Typ	Max	Unit
Digital S/N	75	80		dB
Total Harmonic Distortion			0.02	%
Frequency Response	20		19.200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

DAC Converters

Parameter	Min	Typ	Max	Unit
Digital S/N				
D/A (Front 2 channels)	85	90		dB
Total Harmonic Distortion				
Line Output			0.02	%
Headphone Output			1.0	
Frequency Response	20		19.200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Crosstalk between Input Channels			-70	dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

MECHANICAL SPECIFICATIONS



CONTROL DIMENSIONS ARE IN MILLIMETERS.

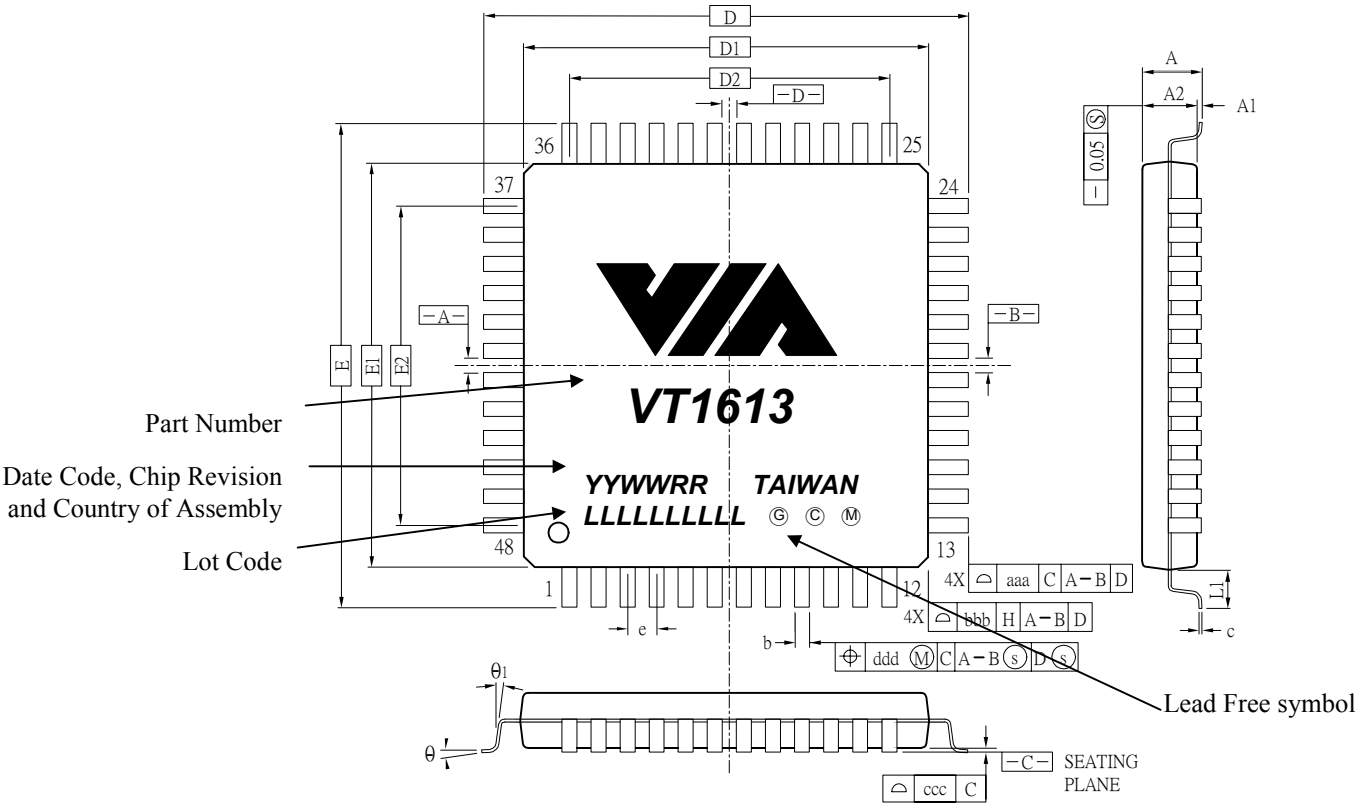
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 3. Mechanical Specification – 48-Pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 4. Mechanical Specification for Lead Free – 48-Pin LQFP