Data Sheet

VT1708B

High Definition Audio Codec

Preliminary Revision 1.0
January 6, 2009

VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: 886-2-2218-5452
FAX: 886-2-2218-5453
Home page: http://www.via.com.tw

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: 510-683-3300
FAX: 510-683-3301 or 510-687-4654
Home Page: http://www.viatech.com

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VT1708B
High Definition Audio Codec

PRODUCT FEATURES

- **High Definition Audio Codec**
  - Intel High Definition Audio Specification Rev.1.0 Compliant
- **High Audio Quality**
  - Exceeds Microsoft Windows Logo Program (WLP) Requirements
  - High-performance ADCs with 98 dB SNR, DACs with 95 dB SNR
- **Various Output Format**
  - 4 Stereo DACs Output Pairs supporting 16/24-bit, 48/ 96/ 192/ 44.1/ 88.2 kHz sample rate
  - 2 Stereo ADCs supporting 16/24-bit, 44.1/ 48/ 96/ 192 kHz sample rate
  - 16/24-bit S/PDIF TX supports 48/ 96 / 44.1/ 88.2 kHz sample rate
  - 16/24-bit S/PDIF RX supports 32/ 48/ 96/ 44.1/ 88.2 kHz sample rate
- **Others**
  - HPF In ADC Path for DC Removal
  - Two Jack Detection Pins
  - Two GPO and Two GPI Pins for Customized Use
- **Power Supply**
  - Digital: 3.3V
  - Analog: 5V
  - Supports External Amplifier Power Down (EPAD)
  - Power Management and Enhanced Power Saving Features
- **Package**
  - Available in 48-Pin LQFP Lead-Free Package
- **Applications**
  - Desktop PCs
  - Laptop PCs

OVERVIEW

The VIA VT1708B is a quality High Definition Audio Codec designed for desktop and laptop PCs. It conforms to Intel High Definition Audio Specification Rev. 1.0 and delivers excellent audio performance that exceeds Microsoft Windows Logo Program (WLP) Requirements. VT1708B supports 98-dB ADC SNR and 95-dB DAC SNR. VT1708B features four 16-, 24-bit stereo digital-to-analog converter (DAC) output-pair channels, supporting audio sampling rates of 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, 88.2 kHz, and two 16-, 24-bit stereo analog-to-digital converter (ADC) channels, supporting audio sampling rates of 44.1 kHz, 48 kHz, 96 kHz, and 192 kHz. VT1708B is capable of supporting various audio output stream formats.

VT1708B also features the 16-, 24-bit S/PDIF TX that supports sampling rates of 48 kHz, 96 kHz, 44.1 kHz, and 88.2 kHz, and the 16-, 24-bit S/PDIF RX that supports sampling rates of 32 kHz, 48 kHz, 96 kHz, 44.1 kHz, and 88.2 kHz. In addition, VT1708B features high-pass-filter (HPF) in analog-to-digital converter (ADC) path for removing DC offset signals. The two Jack Detection pins allow to sense if an audio device is plugged in. VT1708B provides two general-purpose-output (GPO) pins and two general-purpose-input (GPI) pins for customized configurations. VT1708B is available in the 48-Pin LQFP lead-free and RoHS compliant package. Figure 1 shows the functional block diagram of VT1708B High Definition Audio Codec.

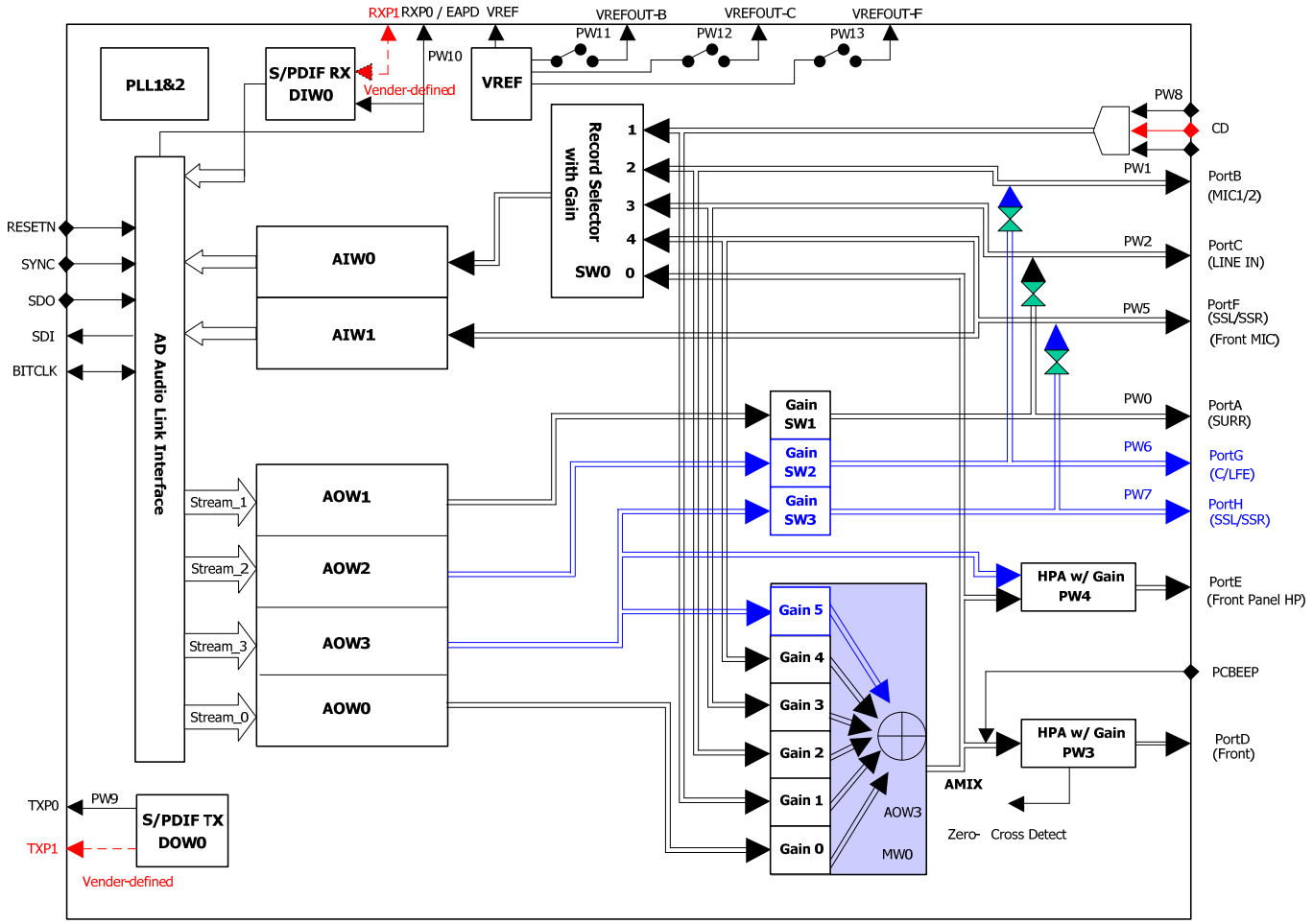

Figure 1. VT1708B Functional Block Diagram

Pin Diagram

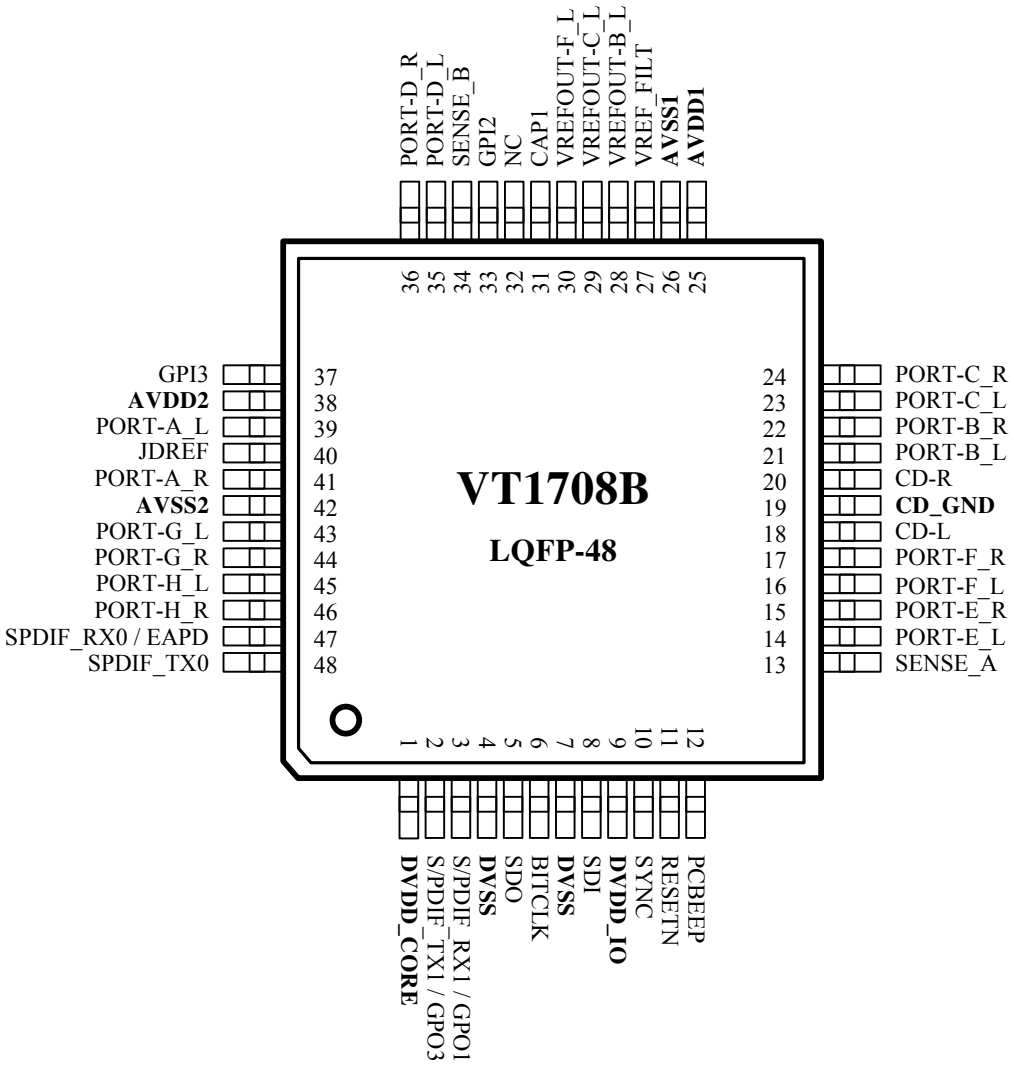

Figure 2. VT1708B Pin Diagram

Pin List

Table 1. Pin List (Listed by Pin Name)

Pin#	Pin Name	Pin#	Pin Name
25	**AVDD1**	35	PORT-D_L
38	**AVDD2**	36	PORT-D_R
26	**AVSS1**	14	PORT-E_L
42	**AVSS2**	15	PORT-E_R
6	BITCLK	16	PORT-F_L
31	CAP1	17	PORT-F_R
19	**CD_GND**	43	PORT-G_L
18	CD-L	44	PORT-G_R
20	CD-R	45	PORT-H_L
1	**DVDD_CORE**	46	PORT-H_R
9	**DVDD_IO**	11	RESETN
4	**DVSS**	47	S/PDIF_RX0 / EAPD
7	**DVSS**	3	S/PDIF_RX1 / GPO1
33	GPI2	48	S/PDIF_TX0
37	GPI3	2	S/PDIF_TX1 / GPO3
40	JDREF	8	SDI
32	NC	5	SDO
12	PCBEEP	13	SENSE_A
39	PORT-A_L	34	SENSE_B
41	PORT-A_R	10	SYNC
21	PORT-B_L	27	VREF_FILT
22	PORT-B_R	28	VREFOUT-B_L
23	PORT-C_L	29	VREFOUT-C_L
24	PORT-C_R	30	VREFOUT-F_L

Note: I = Input, O = Output, A = Analog, B = Bi-directional, P = Power / Ground

Pin Descriptions

Table 2. Pin Descriptions

Digital I/O Pins			
Signal Name	**Pin#**	**I/O**	**Signal Description**
SDO	5	I	Serial data input from controller
BITCLK	6	I	24 MHz bit clock from controller
SDI	8	I/O	Serial data output to controller
SYNC	10	I	Sample SYNC from controller
RESETN	11	I	Hardware reset from controller
S/PDIF_RX0 / EAPD	47	I/O	S/PDIF input / External Amplifier power-down
S/PDIF_RX1 / GPO1	3	I/O	S/PDIF input / General Purpose Output
S/PDIF_TX0	48	O	S/PDIF output
S/PDIF_TX1/ GPO3	2	O	S/PDIF output / General Purpose Output
GPI2 **GPI3**	33 37	I	General Purpose Input

Analog I/O Pins			
Signal Name	**Pin#**	**I/O**	**Signal Description**
SENSE_A	13	I	Jack detect pin 1
SENSE_B	34	I	Jack detect pin 2
PORT-A_L	39	I/O	Analog I/O. Default is output for Back-Surround out Left
PORT-A_R	41	I/O	Analog I/O. Default is output for Back-Surround out Right
PORT-B_L	21	I/O	Analog I/O. Default is input for MIC1 Left
PORT-B_R	22	I/O	Analog I/O. Default is input for MIC1 Right
PORT-C_L	23	I/O	Analog I/O. Default is input for Line-in Left
PORT-C_R	24	I/O	Analog I/O. Default is input for Line-in Right
PORT-D_L	35	I/O	Analog I/O. Default is output for Line-out Left
PORT-D_R	36	I/O	Analog I/O. Default is output for Line-out Right
PORT-E_L	14	O	Analog Output for front panel HP out left
PORT-E_R	15	O	Analog Output for front panel HP out right
PORT-F_L	16	I/O	Analog I/O. Default is input for front MIC
PORT-F_R	17	I/O	Analog I/O. Default is input for front MIC
PORT-G_L	43	I/O	Analog I/O. Default is output for Center
PORT-G_R	44	I/O	Analog I/O. Default is output for LFE
PORT-H_L	45	I/O	Analog I/O. Default is output for Side-Surround out Left
PORT-H_R	46	I/O	Analog I/O. Default is output for Side-Surround out Right
CD-L	18	I	CD input left channel
CD-R	20	I	CD input right channel
PCBEEP	12	I	PC beep signal input
VREF_FILT	27	I/O	Reference voltage capacitor
VREFOUT-B_L	28	O	Reference voltage output for port B
VREFOUT-C_L	29	O	Reference voltage output for port C
VREFOUT-F_L	30	O	Reference voltage output for port F
CAP1	31	I/O	Optional capacitor for ADC reference
JDREF	40	I	External resistor for jack detect circuit

HIGH DEFINITION AUDIO LINK PROTOCOL

Link Signaling

The link protocol defines the digital serial interface that connects High Definition Audio codec to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24MHz BITCLK and is purely isochronous without any flow control.

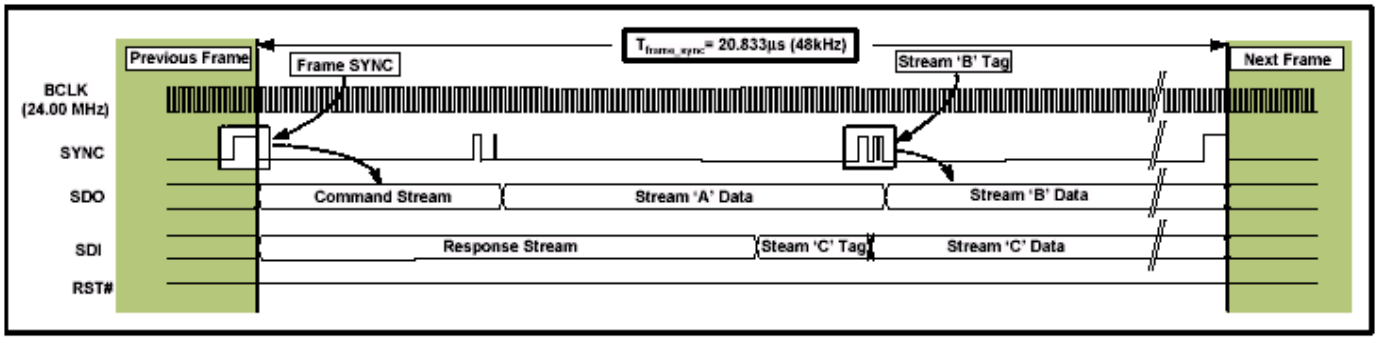

Figure 3. High Definition Audio Link Conceptual View

Signal Definitions

Table 3. Link Signal Description

Signal Name	Source	Type	Description
BITCLK	Controller	I	24 MHz clock
SYNC	Controller	I	Global 48 kHz Frame Sync and outbound tag signal
SDO	Controller	I	Bussed serial data output from controller
SDI	Codec & controller	I/O	Point-to-point serial data. Controller has a weak pull down
RESETN	Controller	I	Global active low reset signal

BITCLK is the 24 MHz clock sourced from the controller and connecting to all codec on the link.

SYNC marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codec on the link.

SDO is driven by the controller to all codec on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

SDI is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared to SDO, data is single pumped with respect to only the rising edge of BITCLK. The controller is required to implement weak pull-down on all SDI signals.

RESETN is sourced from the controller and connects to all codec on the link. Assertion of RESETN results installation link interface logic being reset to default power on state.

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3 and so forth.

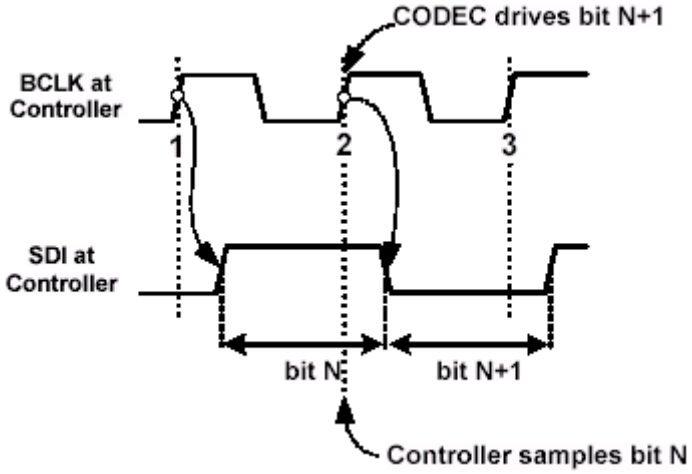

Figure 6. SDI Timing Relative to BITCLK

Signaling Topology

The following diagram shows a typical system with one controller and its associated codec.

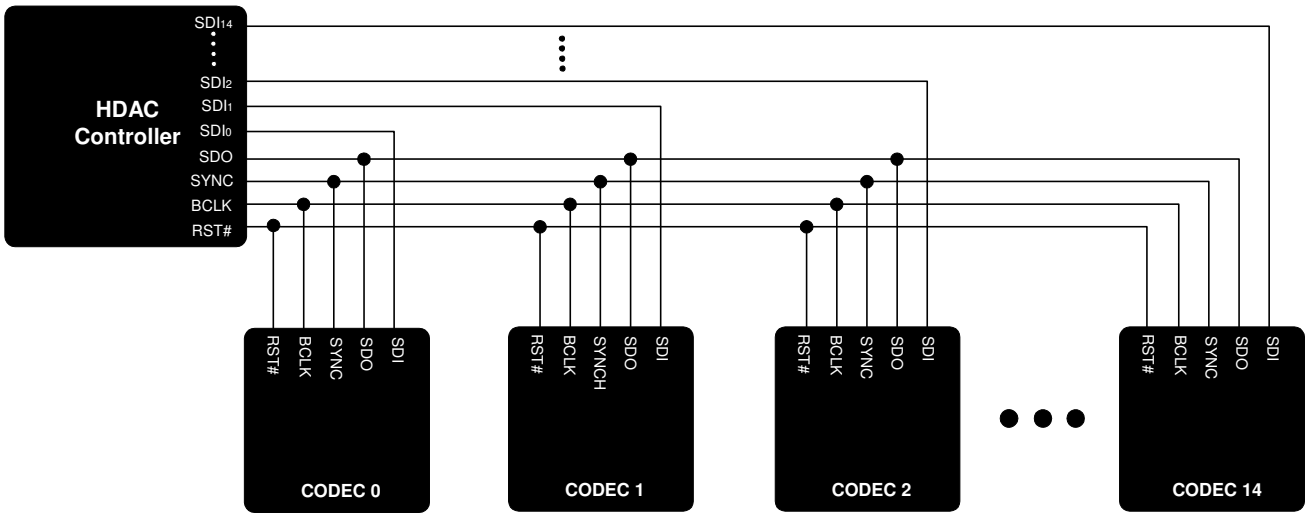

Figure 7. Basic High Definition Audio System

Frame Composition

A frame is defined as a 20.833us window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

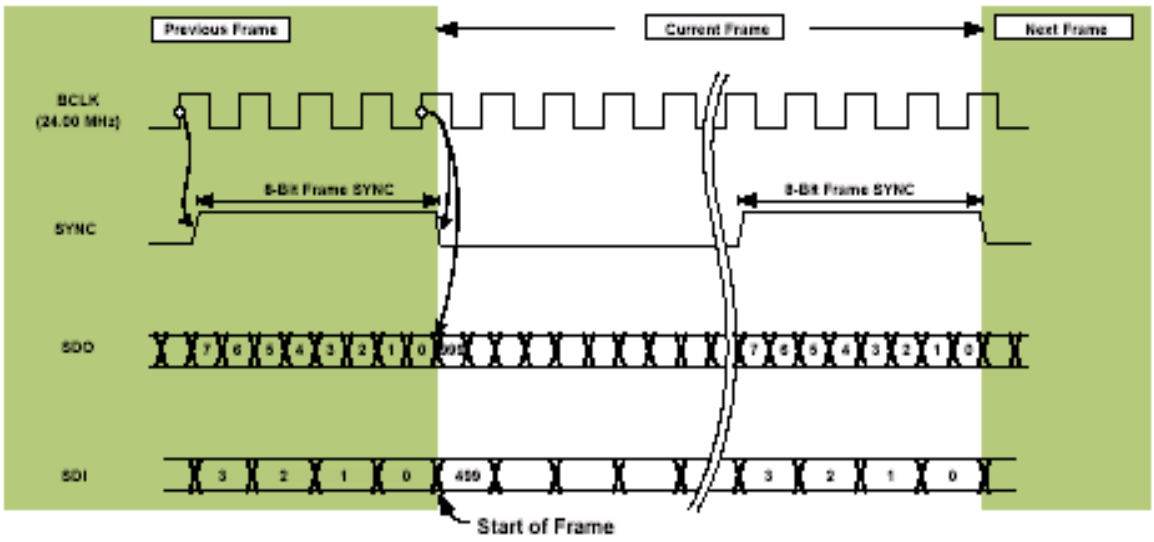

Figure 8. Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

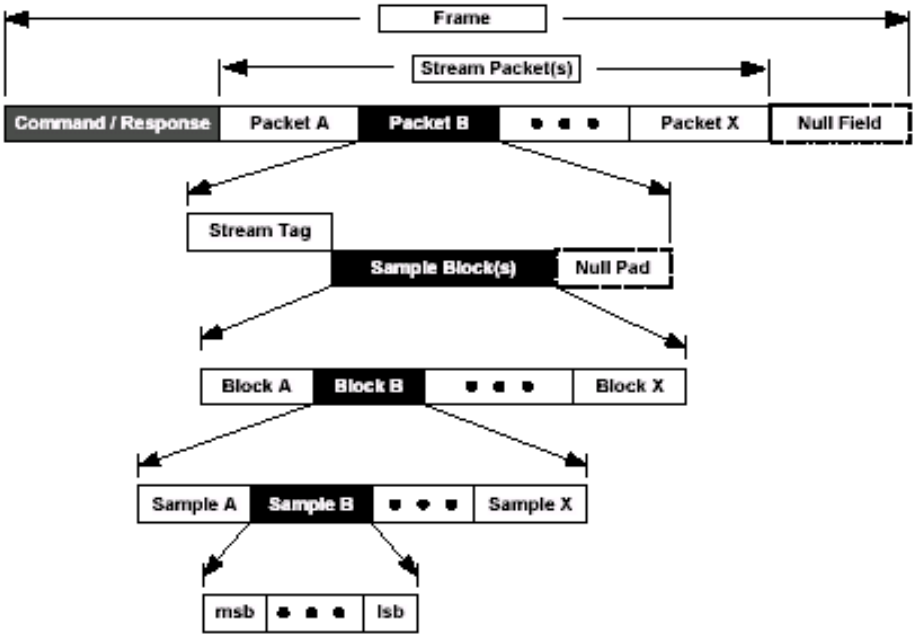

Figure 9. Frame Composition

Command / Response Field is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

Stream Tag is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

Sample Block is a set of one or more samples, the number of which is specified by the "Channels" field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

Sample is a set of bits providing a single sample point of a single analog waveform.

Null Field is used to fill up the remainder of the bits in each frame that are not used for Command/Response or packets. A null field must be transmitted as logical 0's.

Output Frame

Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

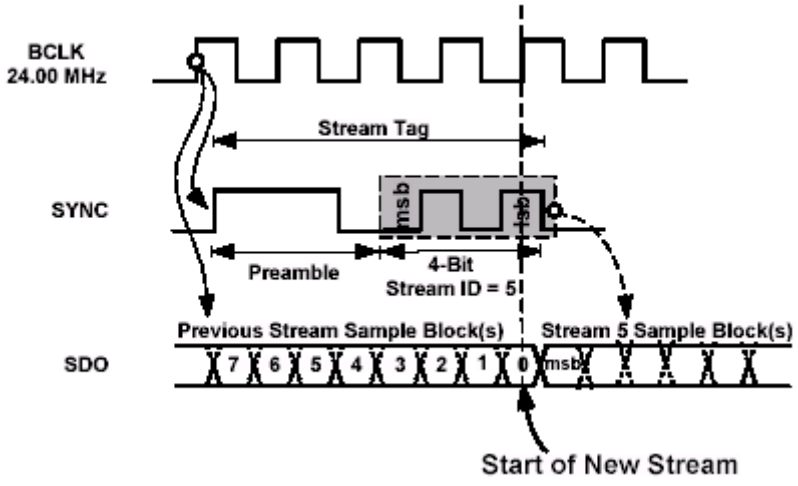

Figure 10. Outbound Stream Tag Format and Transmission

Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are sued to send commands to codec. The controller transmits the tag for the first outbound packet on SYNC during the last eight bit times of the Command field. The sample blocks for the first packet are transmitted on SDO immediately following the Command field. There is no proscribed order in which the different stream packets are to be transmitted. Controllers are required to transmit a null field for the remaining bits within an outbound frame when the transmission of the stream packets completes before the end of the frame.

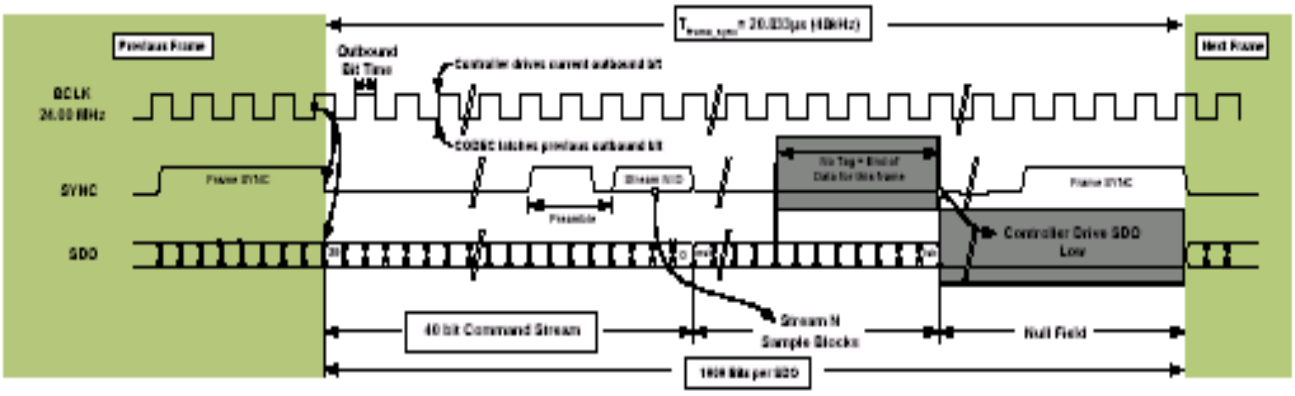

Figure 11. Outbound Frame with Null Field

Input Frame

Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

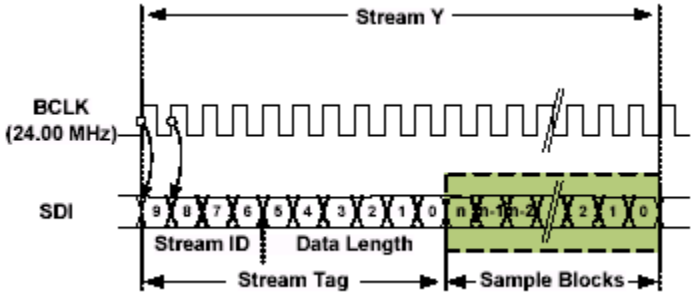

Figure 12. Inbound Tag Format and Transmission

Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codec use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

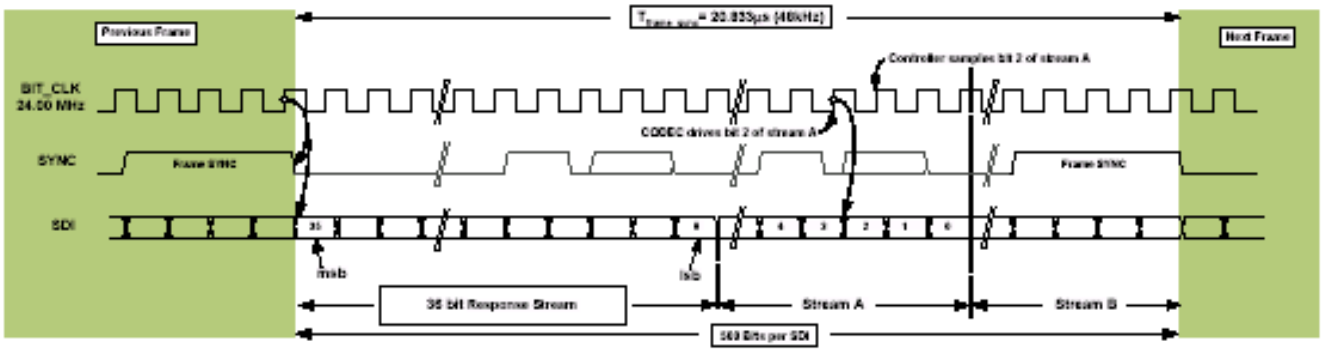

Figure 13. Inbound Frame with No Null Field

Reset and Initialization

Link Reset

A link reset is signaled on the link by assertion of the RESETN signal, and results in all Link interface logic in both codec and controller, including registers, being initialized to their default state. The controller drives all SDO and SYNC outputs low when entering or exiting link reset. A controller may only initiate the link reset entry sequence after completing any currently pending initialization or state change requests.

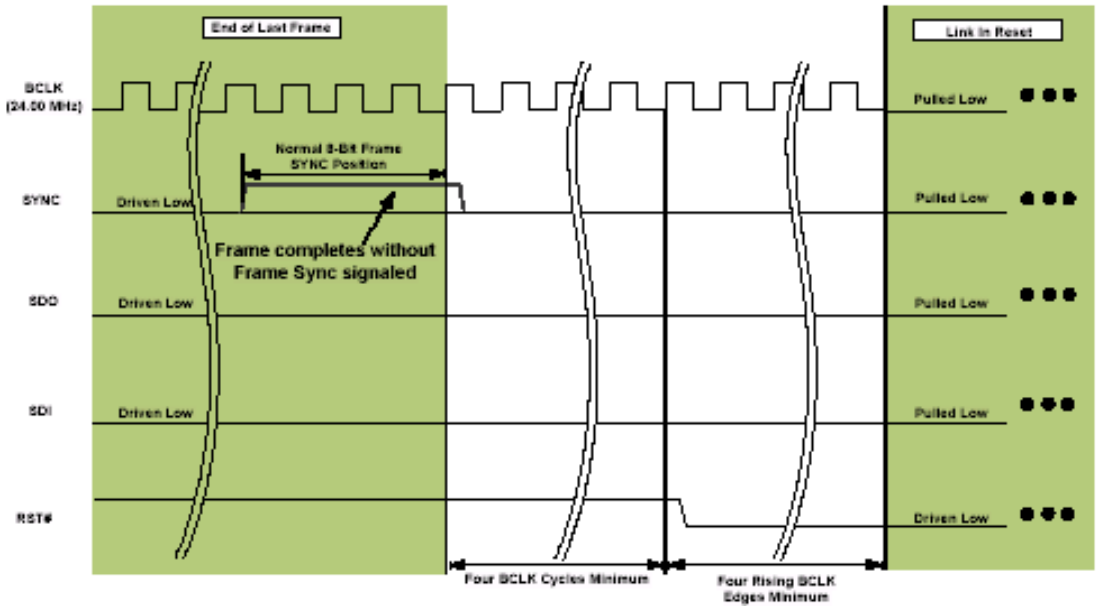

Figure 14. Link Reset Entry Sequence

Codec Initialization

With immediately following the completion of Link Reset sequence (or Function_Reset verb, if enabled by the vendor-defined verb), VT1708B proceeds through a codec initialization sequence, which provides each codec with a unique address by which it can thereafter be referenced with Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

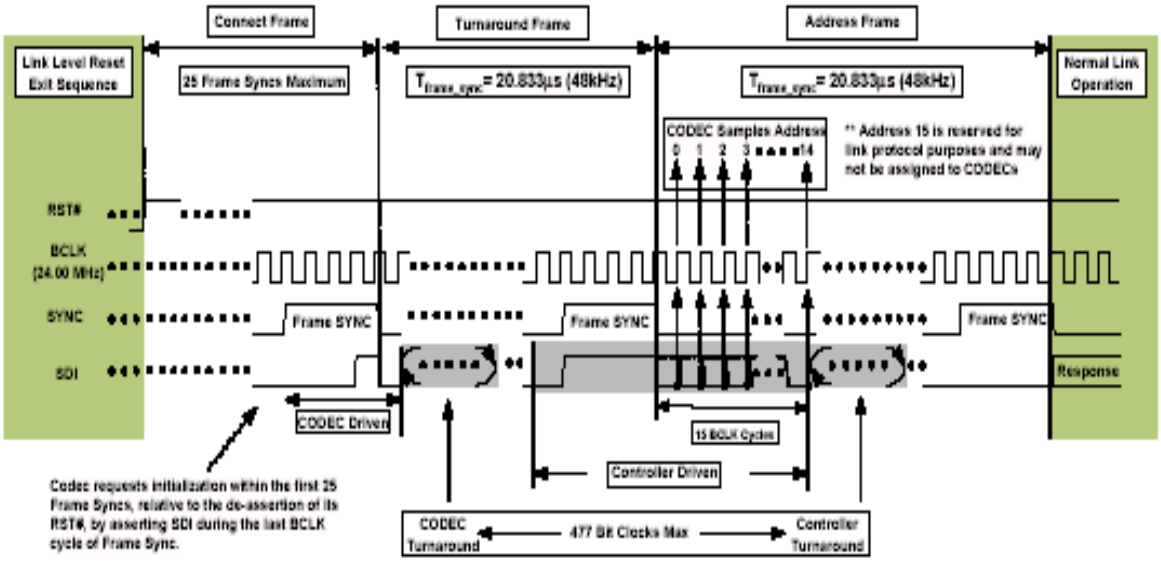

Figure 16. Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, codec are required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled "Connect Frame", "Turnaround Frame" and "Address Frame", are described below.

Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

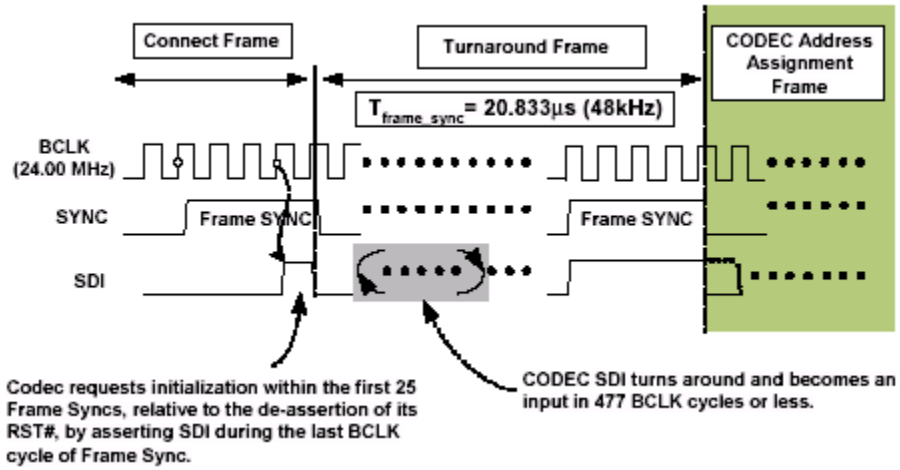

Figure 17. Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and be synchronously de-asserted on the same rising edge of BITCLK as the de-assertion of the Frame Sync. Codec are only permitted to signal an initialization request on a null input frame, in which no response stream or input streams are being sent.

In the Turnaround Frame, codec and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

Address Frames

During the Address Frame, SDI is a codec input and driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus the unique address of the codec becomes the ID of its attached SDI.

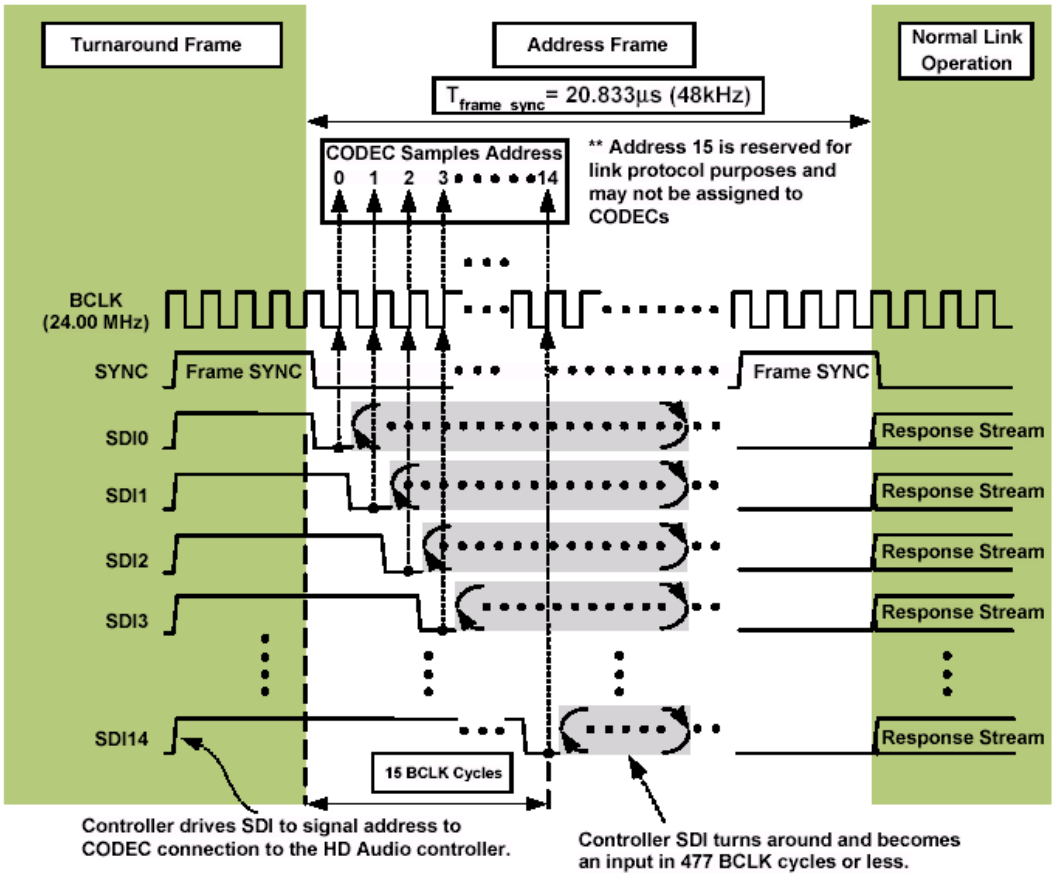

Figure 18. Address Frame

Codec count from zero to fourteen starting on the rising edge of BITCKL following the de-assertion of Frame Sync, and sample the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18th BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

Codec Sample Rendering Timing

VT1708B supports all the multiples and submultiples of the base rates of 48 kHz and 44.1 kHz up to the maximum rate of DAC and ADC respectively. For DAC, up to 192 kHz sample rate is supported. For ADC, the maximum rate is 96 kHz.

Table 4. Sample Rates Supported

Multiple	Base Rate 48 kHz	Base Rate 44.1 kHz
1/6	8 kHz	-
¼	-	11.025 kHz
1/3	16 kHz	-
½	-	22.05 kHz
2/3	32 kHz	-
1	48 kHz	44.1 kHz
2	96 kHz	88.2 kHz
4	192 kHz	176.4 kHz

Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48 kHz, the timing is relatively straightforward. The rates in multiple (N) of 48 kHz are containing N sample blocks in one frame. For the rates in sub-multiple (1/N) of 48 kHz, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48 kHz, streams using a base rate of 44.1 kHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1 kHz, there are occasional frames that will not contain a sample generating the following cadence:

12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long-term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1 kHz apply the "12-11" cadence rule just as a 44.1 kHz sample rate would, except that the non-empty frames contain multiple (2 or 4) sample blocks instead of just one.

For a sample rate of 22.05 kHz, the transmission pattern becomes:
{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{11}-* (repeat)
where
{12} = 1*1*1*1*1*1*1*1*1*1*1*1*
{11} = 1*1*1*1*1*1*1*1*1*1*
and the asterisks * represent a frame in which there is no sample block.

For a sample rate of 11.025 kHz, the transmission pattern becomes:
[12]-*[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[11]-*** (repeat)**
where
[12] = 1*1***1***1***1***1***1***1***1***1***1***1*****
[11] = 1*1***1***1***1***1***1***1***1***1*****
and the asterisks * represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.

Power Management

Whenever the Link is commanded to enter a low power state, it enters the link-reset state. This state is only exited in response to a software command and follows all link rules for exiting the link-reset state.

The Audio Function Group and the analog input / output converter widgets support power control. The whole chip power states can be controlled through the Audio Function Group, while individual DACs and ADCs can also be controlled through the corresponding power state control verbs. The definitions of the power states are described in the following table.

Table 5. Power States Definitions

Power States	Definitions	Referenced with AC97
D0	All power on. Individual ADCs & DACs can be controlled.	-
D1	All amplifiers and analog converters are powered down. Register values maintained, and analog reference voltage is still on.	PR0 & PR1 & PR2
D2	Register values maintained, but analog reference voltage is also down.	PR3
D3	Register values maintained, but analog reference voltage is also down.	PR3

WIDGET DESCRIPTIONS

Node ID List

Table 6. Node ID List

Node ID	Name	Input Connection List
00	**Root Node**	N/A
01	**Audio Function Group** (AFG)	N/A
10	**Analog Output Widget 0** (AOW0)	N/A
11	**Analog Output Widget 1** (AOW1)	N/A
12	**Digital Output Widget 0 for S/PDIF TX** (DOW0)	N/A
13	**Analog Input Widget 0** (AIW0)	17
14	**Analog Input Widget 1** (AIW1)	1E
15	**Digital Input Widget 0 for S/PDIF RX** (DIW0)	21
16	**Analog Mixer** (MW0)	10, 1A, 1B, 1E, 1F, 25
17	**ADC Input Selection** (SW0)	16, 1A, 1B, 1E, 1F
18	**AOW1 Volume** (SW1)	11
19	**Port A** (PW0)	18
1A	**Port B** (PW1)	26
1B	**Port C** (PW2)	18
1C	**Port D** (PW3)	16
1D	**Port E** (PW4)	16,25
1E	**Port F** (PW5)	27
1F	**Pin Widget 8 for CD Input** (PW8)	N/A
20	**Pin Widget 9 for S/PDIF TX** (PW9)	12
21	**Pin Widget 10 for S/PDIF RX** (PW10)	N/A
22	**Port G** (PW6)	26
23	**Port H** (PW7)	27
24	**Analog Output Widget 2** (AOW2)	N/A
25	**Analog Output Widget 3** (AOW3)	N/A
26	**AOW2 Volume** (SW2)	24
27	**AOW3 Volume** (SW3)	25

Root Node (Node ID = 00)

Get Parameter Verb (Verb ID = F00h)

Get Vendor ID (Payload = 00h) **Response Value: 1106 E721h**

Bit	Attr.	Description
31:16	R	**Vendor ID**
15:0	R	**Device ID**

Get Revision ID (Payload = 02h) **Response Value: 0010 nn00h**

Bit	Attr.	Description
31:24	R	**Reserved**
23:16	R	**Revision Number**
15:8	R	**Revision ID**
7:0	R	**Stepping ID**

Get Subordinate Node Count (Payload = 04h) **Response Value: 0001 0001h**

Bit	Attr.	Description
31:24	R	**Reserved**
23:16	R	**Starting Node Number**
15:8	R	**Reserved**
7:0	R	**Total Number of Nodes.** (Only 1 Audio Function Group in the codec)

Get Subsystem ID Control Verbs (Verb ID = F20h / 720h / 721h / 722h / 723h)

	Description	Verb ID	Payload
Get	Get Subsystem ID	F20h	00h
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

Response Value: 1106 0000h

Bit	Attr.	Description
31:16	R	**Manufacturer ID**
15:8	R	**Board SKU**
7:0	R	**Assembly ID**

Note: All 32 bits in the Subsystem ID register are writeable with the power-on default value of **1106 0000h.** The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

Get Power State Verbs (Verb ID = F05h & 705h)

For whole chip power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	**Reserved**. Read as 0.
7:4	R	**PS-Act.** Same as PS-Set for AFG.
3:0	R	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Get Vendor Defined Verbs (Verb ID = F70h / F71h / F72h / F73h / F74h) – Reserved

Get Vendor Defined Verbs (Verb ID = F78h / F79h / F7Ah / F7Bh / F7Ch) – Reserved

Get Vendor Defined Verbs (Verb ID = F80h / F81h / F82h / F83h / F84h) – Reserved

Get Vendor Defined Verbs (Verb ID = F88h / F89h / F8Ah / F8Bh / F8Ch) – Reserved

Get Vendor Defined Verbs (Verb ID = F90h / F91h / F92h / F93h / F94h) – Reserved

Function Reset Verbs (Verb ID = 7FFh)

	Description	Verb ID	Payload
Function Reset	Function Reset	7FFh	00h

Get Vendor Defined Verbs (Verb ID = F88h – F8Ch) – Reserved

Audio Analog Output Converter Widget 0-3 (Node ID = 10, 11, 24, 25)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0000 0411h**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	0000: Audio Output Converter Widget
19:16	R	0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	0: Connection list not present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	**Reserved**
4	R	1: Format information contained
3	R	0: Amplifier parameter not contained
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response Value: 000A 07E0h**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384 kHz not supported
10	R	1: 192 kHz supported
9	R	1: 176.4 kHz supported
8	R	1: 96 kHz supported
7	R	1: 88.2 kHz supported
6	R	1: 48 kHz supported
5	R	1: 44.1 kHz supported
4	R	0: 32 kHz not supported
3	R	0: 22.05 kHz not supported
2	R	0: 16 kHz not supported
1	R	0: 11.025 kHz not supported
0	R	0: 8 kHz not supported

Supported Stream Formats (Payload = 0Bh) **Response Value: 0000 0001h**

Bit	Attr.	Description
31:3	R	**Reserved**
2	R	0: No AC3 support
1	R	0: No Float32 support
0	R	1: PCM supported

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Get Power State Verbs (Verb ID = F05h / 705h)

For DAC power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	**Reserved.** Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	R	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Get Converter Stream, Channel Verbs (Verb ID = F06h / 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	00h
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Get Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	0000h
Set	Set Converter Format	2h	Format

Bit	Attr.	Description
15	R	**Stream Type** 0: PCM 1: Non-PCM (not supported)
14	RW	**Sample Base Rate** 0: 48 kHz 1: 44.1 kHz
13:11	RW	**Sample Base Rate Multiple** 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz, 88.2 kHz 010: x3: 144 kHz (not supported) 011: x4: 192 kHz, 176.4 kHz 100-111: Reserved
10:8	RW	**Sample Base Rate Divisor** 000 = /1: 48 kHz Others: not supported
7	R	**Reserved**
6:4	RW	**Bits per Sample** 000: 8 bits (not supported) 001: 16 bits 010: 20 bits (not supported) 011: 24 bits 100: 32 bits (not supported)
3:0	RW	**Number of Channels** Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000: 1 0001: 2 …… 1111: 16

Digital Output Widget for S/PDIF TX (Node ID = 12)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0000 0611h**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	0000: Audio Output Converter Widget
19:16	R	0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	1: Digital widget
8	R	0: Connection list not present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	**Reserved**
4	R	1: Format information contained
3	R	0: Amplifier parameter not contained
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response Value: 000A 01E0h**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384 kHz not supported
10	R	0: 192 kHz not supported
9	R	0: 176.4 kHz supported
8	R	1: 96 kHz supported
7	R	1: 88.2 kHz supported
6	R	1: 48 kHz supported
5	R	1: 44.1 kHz supported
4	R	0: 32 kHz not supported
3	R	0: 22.05 kHz not supported
2	R	0: 16 kHz not supported
1	R	0: 11.025 kHz not supported
0	R	0: 8 kHz not supported

Supported Stream Formats (Payload = 0Bh) **Response Value: 0000 0001h**

Bit	Attr.	Description
31:3	R	**Reserved**
2	R	0: No AC3 not support
1	R	0: No Float32 support
0	R	1: PCM supported

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Get Power State Verbs (Verb ID = F05h / 705h)

For S/PDIF TX power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	**Reserved.** Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	R	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Converter Stream, Channel Verbs (Verb ID = F06h / 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	00h
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Get S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh / 70Dh / 70Eh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	00h
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]

S/PDIF IEC Control Bits Format

Bit	Attr.	Description
15	R	**Reserved**
14:8	RW	**Category Code[6:0]**
7	RW	**Generation Level**
6	RW	**PRO** 0: Consumer mode 1: Professional mode
5	RW	**AUDIO** 0: Data is PCM format 1: Data is non PCM format
4	RW	**Copyright** 0: Copyright is not asserted 1: Copyright is asserted
3	RW	**Pre-emphasis** 0: Pre-emphasis is none 1: Filter pre-emphasis is 50/15 µs
2	RW	**VCFG.** Determines S/PDIF transmitter behavior when data is not being transmitted.
1	RW	**Validity Flag**
0	RW	**Digital Enable** 0: S/PDIF TX disabled 1: S/PDIF TX enabled

Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	00h
Set	Set Converter Format	2h	Format

Bit	Attr.	Description
15	RW	**Stream Type** 0: PCM 1: Non-PCM
14	RW	**Sample Base Rate** 0: 48 kHz 1: 44.1 kHz
13:11	RW	**Sample Base Rate Multiple** 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz, 88.2 kHz 010: x3: 144 kHz (not supported) 011: x4: 192 kHz, 176.4 kHz (not supported) 100-111: reserved

(continued)

Bit	Attr.	Description
10:8	RW	**Sample Base Rate Divisor** 000 = /1: 48 kHz Others: not supported
7	R	**Reserved**
6:4	RW	**Bits per Sample** 000: 8-bit (not supported) 001: 16-bit 010: 20-bit (not supported) 011: 24-bit 100: 32-bit (not supported)
3:0	RW	**Number of Channels (CHAN).** Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

Analog Input Widget 0-1 (Node ID = 13h, 14h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0010 051Bh**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	0001: Audio Input Converter Widget
19:16	R	0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	1: Connection list is present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	**Reserved**
4	R	1: Format information contained
3	R	1: Amplifier parameter contained
2	R	0: Out Amp not present
1	R	1: In Amp present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response Value: 000A 0560h**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384 kHz not supported
10	R	1: 192 kHz supported
9	R	0: 176.4 kHz not supported
8	R	1: 96 kHz supported
7	R	0: 88.2 kHz not supported
6	R	1: 48 kHz supported
5	R	1: 44.1 kHz supported
4	R	0: 32 kHz not supported
3	R	0: 22.05 kHz not supported
2	R	0: 16 kHz not supported
1	R	0: 11.025 kHz not supported
0	R	0: 8 kHz not supported

Get Power State Verbs (Verb ID = F05h / 705h)

For ADC power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	**Reserved.** Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	RW	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Get Converter Stream, Channel Verbs (Verb ID = F06h / 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	00h
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Get Converter Format Verbs (Verb ID = Ah / 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	0000h
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attr.	Description
15	R	**Stream Type** 0: PCM 1: Non-PCM (not supported)
14	R	**Sample Base Rate** 0: 48 kHz 1: 44.1 kHz
13:11	RW	**Sample Base Rate Multiple** 000: x: 48 kHz, 44.1 kHz 001: x2: 96 kHz 010: x3: 144 kHz (not supported) 011: x4: 192 kHz 100-111: reserved
10:8	RW	**Sample Base Rate Divisor** 000: /1:48 kHz Others: not supported
7	R	**Reserved**
6:4	RW	**Bits per Sample** 000: 8 bits (not supported) 001: 16 bits 010: 20 bits (not supported) 011: 24 bits 100: 32 bits (not supported)

(continued)

Bit	Attr.	Description
6:4	RW	**Bits per Sample** 000: 8-bit (not supported) 001: 16-bit 010: 20-bit (not supported) 011: 24-bit 100: 32-bit (not supported)
3:0	RW	**Number of Channels (CHAN).** Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

Get Amplifier Gain/Mute Verbs (Verb ID = Bh / 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain / Mute	Bh	Format
Set	Set Amplifier Gain / Mute	3h	Format

Get Payload Format

Bit	Attr.	Description
15	W	0: The input amplifier is being requested 1: The output amplifier is being requested (ignored)
14	R	**Reserved**
13	W	0: The right amplifier is being requested 1: The left amplifier is being requested
12:4	R	**Reserved**
3:0	W	Index Ignored

Get Response Format

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Amplifier is not mute. 1: Amplifier is mute.
6:0	R	Amplifier Gain Setting Default is 0.

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set (ignored)
14	W	1: The input amplifier is being set
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	Index Ignored
7	W	0: Not mute 1: Mute
6:0	W	Gain Setting

Digital Input Widget for S/PDIF RX (Node ID = 15h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0010 0711h**

Bit	Attr.	Description
31:24	R	Reserved
23:20	R	0001: Audio Input Converter Widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	1: Digital widget
8	R	1: Connection list is present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	Reserved
4	R	1: Format information contained
3	R	0: Amplifier parameter not contained
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response Value: 000A 01F0h**

Bit	Attr.	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	Reserved
11	R	0: 384 kHz not supported
10	R	0: 192 kHz not supported
9	R	0: 176.4 kHz not supported
8	R	1: 96 kHz supported
7	R	1: 88.2 kHz supported
6	R	1: 48 kHz supported
5	R	1: 44.1 kHz supported
4	R	1: 32 kHz supported
3	R	0: 22.05 kHz not supported
2	R	0: 16 kHz not supported
1	R	0: 11.025 kHz not supported
0	R	0: 8 kHz not supported

Converter Stream, Channel Verbs (Verb ID = F06h / 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	00h
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh / 70Dh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	00h
Set	Set Converter Control State	70Dh	

S/PDIF IEC Control Bits Format

Bit	Description
15	**Reserved**
14:8	**Category Code[6:0]**
7	**Generation Level**
6	**PRO** 0: Consumer mode 1: Professional mode
5	**AUDIO** 0: Data is PCM format 1: Data is non-PCM format
4	**Copyright** 0: Copyright is not asserted 1: Copyright is asserted
3	**Pre-emphasis** 0: Pre-emphasis is none 1: Filter pre-emphasis is 50/15 µs
2	**Reserved**
1	**Validity Flag**
0	**Digital Enable** 0: S/PDIF RX disabled 1: S/PDIF RX enabled

Analog Mixer Widget (Node ID = 16h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0020 050Bh**

Bit	Attr.	Description
31:24	R	Reserved
23:20	R	0010: Audio Mixer Widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	1: Connection list present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	Reserved
4	R	0: Format information not contained
3	R	1: Amplifier parameter contained
2	R	0: Out Amp not present
1	R	1: In Amp present
0	R	1: Stereo

Input Amplifier Capabilities (Payload = 0Dh) **Response Value: 8006 1F17h**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	**Reserved**
22:16	R	**Step Size** 0000110b: Step size is 1.5 dB (no effect)
15	R	**Reserved**
14:8	R	**Number of Steps** 0011111: Number of steps is 31 (-34.5 dB – 12 dB)
7	R	**Reserved**
6:0	R	**Offset** 0010111: Offset 17h is 0 dB

Connection List Length (Payload = 0Eh) **Response Value: 0000 0006h**

Bit	Attr.	Description
31:8	R	Reserved
7	R	0: Short form
6:0	R	0000110: 6 inputs available

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Get Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Bit	Attr.	Description	
		Offset index n = 0	**Offset index n = 4**
31:24	R	**Connection List Entry n+3** 1Bh (PW2, Port C)	00h
23:16	R	**Connection List Entry n+2** 1Ah (PW1, Port B)	00h
15:8	R	**Connection List Entry n+1** 1Fh (PW8, CD)	**Connection List Entry n+1** 25h (AOW3)
7:0	R	**Connection List Entry n** 10h (AOW0)	**Connection List Entry n** 1Eh (PW5, Port F)

Get Power State Verbs (Verb ID = F05h / 705h)

For Mixer power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	Reserved. Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	RW	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Get Amplifier Gain/Mute Verbs (Verb ID = Bh / 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain / Mute	Bh	Format
Set	Set Amplifier Gain / Mute	3h	Format

Get Payload Format

Bit	Attr.	Description
15	W	0: The input amplifier is being requested 1: The output amplifier is being requested (ignored)
14	R	**Reserved**
13	W	0: The right amplifier is being requested 1: The left amplifier is being requested
12:4	R	**Reserved**
3:0	W	**Index**

Get Response Format

Bit	Attr.	Description
31:8	R	Reserved. Read as 0
7	R	0: Amplifier is not mute 1: Amplifier is mute
6:0	R	**Amplifier Gain Setting** Default is 0.

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set (ignored)
14	W	1: The input amplifier is being set
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	0: Not mute 1: Mute
6:0	W	**Gain Setting**

Selector Widget 0 (Node ID = 17h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0030 0501h**

Bit	Attr.	Description
31:24	R	Reserved
23:20	R	0011: Audio Selector Widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	1: Connection list is present
7	R	0: Unsolicited response not supported
6	R	0: No processing control
5	R	Reserved
4	R	0: Format information not contained
3	R	0: Amplifier parameter not contained
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Connection List Length (Payload = 0Eh) **Response Value: 0000 0005h**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	0000101: 5 input available

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Get Connection Select Control Verbs (Verb ID = F01h / 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	00h
Set	Set Connection Select	701h	The connection index value to be set

Get Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Bit	Attr.	Description	
		Offset index n = 0	**Offset index n = 4**
31:24	R	**Connection List Entry n+3** 1Bh (PW2, Port C)	00h
23:16	R	**Connection List Entry n+2** 1Ah (PW1, Port B)	00h
15:8	R	**Connection List Entry n+1** 1Fh (PW8, CD)	00h
7:0	R	**Connection List Entry n** 16h (MW0)	**Connection List Entry n** 1Fh (PW5, Port F)

Get Power State Verbs (Verb ID = F05h / 705h)

For SW0 power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	Reserved. Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	RW	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Selector Widget 1-3 (Node ID = 18h, 26h, 27h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response Value: 0030 050Dh**

Bit	Attr.	Description
31:24	R	Reserved
23:20	R	0011: Audio Selector Widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	1: Connection present
7	R	0: Unsolicited response not supported
6	R	0: No Processing control
5	R	Reserved
4	R	0: Format information not contained
3	R	1: Amplifier parameter contained
2	R	1: Out Amp present
1	R	0: In Amp not present
0	R	1: Stereo

Connection List Length (Payload = 0Eh) **Response Value: 0000 0001h**

Bit	Attr.	Description
31:8	R	Reserved
7	R	0: Short form
6:0	R	0000001: 1 input available

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	Reserved
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Amplifier Capabilities (Payload = 12h) **Response Value: 8006 1B1Bh**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	Reserved
22:16	R	**Step Size** 0000110: Step size is 1.5 dB
15	R	Reserved
14:8	R	**Number of Steps** 0011011: Number of steps is 27 (-40.5 dB – 0 dB)
7	R	Reserved
6:0	R	**Offset** 0011011: Offset 1Bh is 0 dB

Get Connection Select Control Verbs (Verb ID = F01h / 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	00h
Set	Set Connection Select	701h	The connection index value to be set

Get Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Bit	Attr.	Description
31:8	R	**Reserved**
7:0	R	**Connection List Entry n** 11h (AOW1) for SW1 24h (AOW2) for SW2 25h (AOW3) for SW3

Get Power State Verbs (Verb ID = F05h / 705h)

For SW1 – SW3 power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	Reserved. Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	RW	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3

Get Amplifier Gain/Mute Verbs (Verb ID = Bh / 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain / Mute	Bh	Format
Set	Set Amplifier Gain / Mute	3h	Format

Get Payload Format

Bit	Attr.	Description
15	W	0: The input amplifier is being requested (ignored). 1: The output amplifier is being requested.
14	R	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	R	Reserved
3:0	W	**Index Ignored**

Get Response Format

Bit	Attr.	Description
31:8	R	Reserved
7	R	0: Amplifier is not mute. 1: Amplifier is mute.
6:0	R	**Amplifier Gain Setting** Default is 0.

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set
14	W	1: The input amplifier is being set (ignored)
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	0: Not mute 1: Mute
6:0	W	**Gain Setting**

Pin Widget 0 (Node ID = 19h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) **Response Value: 0000 0101h**

Bit	Attr.	Description
31:9	R	Reserved
8	R	1: Unsolicited capable
7:0	R	01h: Audio Function Group

Audio Widget Capabilities (Payload = 09h) **Response Value: 0040 0581h**

Bit	Attr.	Description
31:24	R	Reserved
23:20	R	0100: Pin Widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R Swap
10	R	1: Power control supported
9	R	0: Analog widget
8	R	1: Connection list present
7	R	1: Unsolicited response supported
6	R	0: No processing control
5	R	Reserved
4	R	0: Format information not contained
3	R	0: Amplifier parameter not contained
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response Value:0000 001Ch**

Bit	Attr.	Description
31:17	R	Reserved
16	R	EAPD Capable
15:8	R	VRef Control
7	R	Reserved
6	R	Balanced I/O Pins
5	R	Input Capable
4	R	Output Capable
3	R	Headphone Drive Capable
2	R	Presence Detect Capable
1	R	Trigger Required
0	R	Impedance Sense Capable

Connection List Length (Payload = 0Eh) **Response Value: 0000 0001h**

Bit	Attr.	Description
31:8	R	Reserved
7	R	0: Short form
6:0	R	0000001b: Only 1 input available

Supported Power States (Payload = 0Fh) **Response Value: 0000 000Fh**

Bit	Attr.	Description
31:4	R	Reserved
3	R	**Power State D3 Supported** 1: Supported
2	R	**Power State D2 Supported** 1: Supported
1	R	**Power State D1 Supported** 1: Supported
0	R	**Power State D0 Supported** 1: Supported

Get Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent NID
6:0	R	18h (from SW1)

Get Power State Verbs (Verb ID = F05h / 705h)

For PW0 power down control:

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	00h
Set	Set Converter Power State	705h	PS-Set

Bit	Attr.	Description
31:8	R	**Reserved.** Read as 0.
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	RW	**PS-Set** 00h: Power State is D0 01h: Power State is D1 02h: Power State is D2 03h: Power State is D3