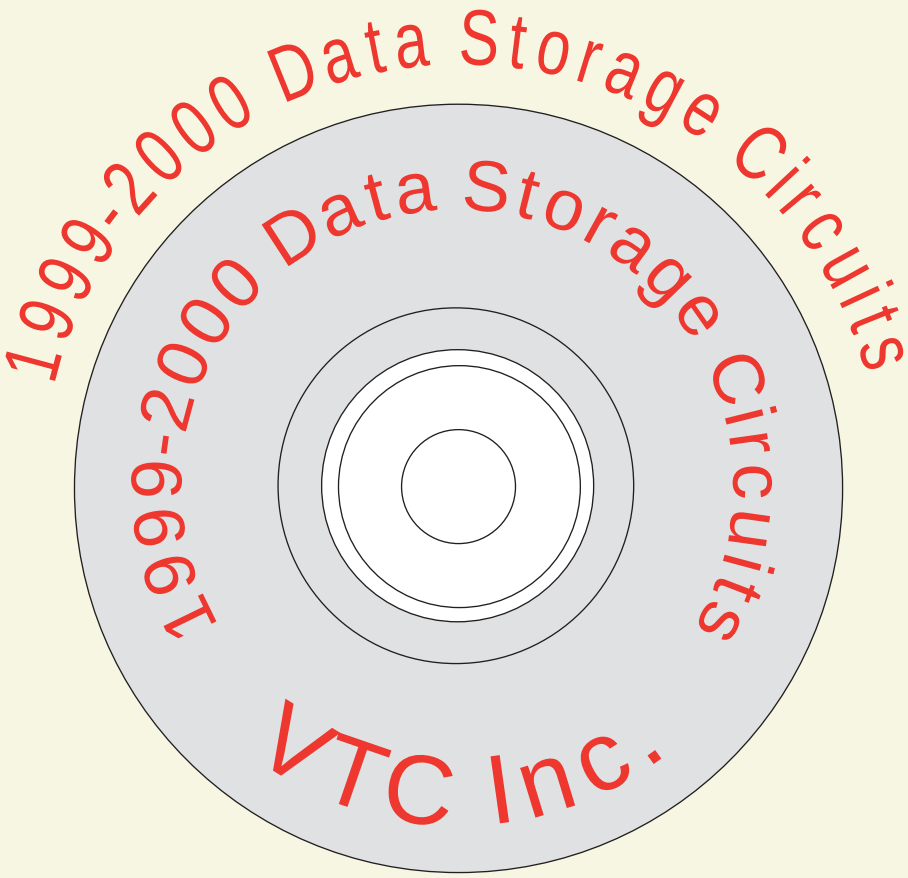

VTC Inc.

Value The Customer™

The leader in quality, high-performance integrated circuits and customer service for the data storage industry.

DATA STORAGE INTEGRATED

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DATA SHEET AND PRODUCT

Advance Information

This data sheet contains the design specifications for products in development. Specifications may change in any manner without notice. Typically this indicates first silicon has been evaluated, but not completely verified.

Preliminary

This data sheet contains preliminary data. Supplementary data will be published at a later date. VTC reserves the right to make changes at any time without notice in order to improve design or enhance the product. Preliminary indicates the product is in the first production stage.

(No Identification)

This data sheet contains final specifications as confirmed through design, verification and device characterization. This device is in final production.

Although all VTC products have input and output circuits that protect against damage due to high static voltage or electrostatic fields, VTC still recommends following normal ESD precautions for handling semiconductor devices.

VTC Inc. reserves the right to make changes to its products without notice in order to improve design, performance, function or reliability. VTC assumes no responsibility for use of any circuits described or represented other than the circuitry embodied in its products.

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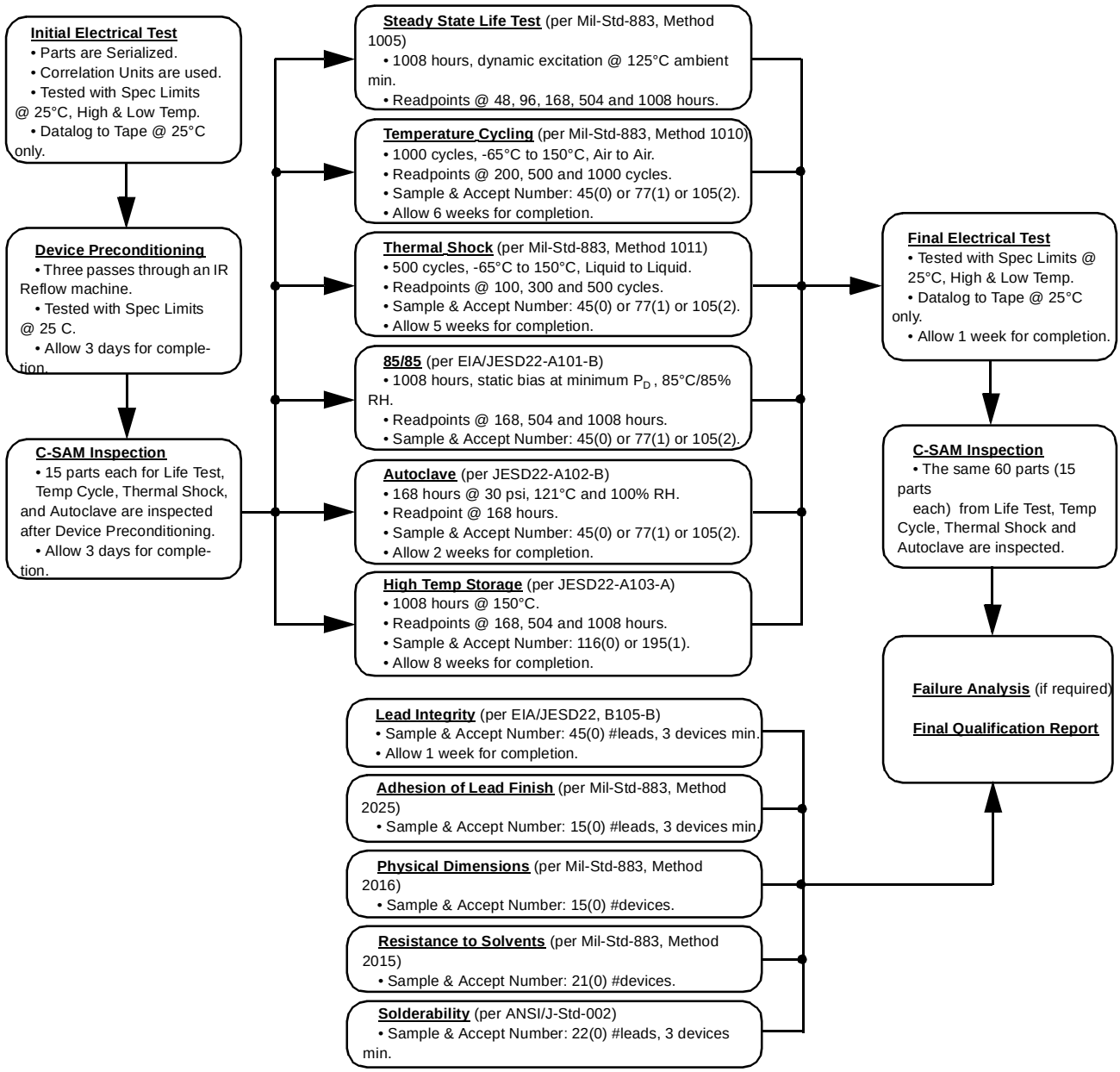
QUALITY AND RELIABILITY

VTC's quality journey encompasses every facet of its business from marketing to manufacturing. The company's objective is to establish industry standards for quality and reliability and to be recognized by its customers as a company dedicated to providing exceptional service with honesty and integrity.

VTC understands that success depends on the high **quality** of products, on the excellence of **service** provided to customers, and on the low **cost** of producing products. To meet the goals of quality, service and cost, VTC involves all its employees in a program of continuous improvement in the following ways:

- Employees are trained in the use of on-line and off-line statistical process control tools, which enables them to understand and reduce variability in manufacturing processes with 6σ as a goal.
- *Quality is designed into products and processes, thus eliminating dependence on quality inspections.*
- *Highly focused project teams use time-proven problem analysis and solution tools.*
- *PPM and qualification/ORT programs are used to monitor progress.*

Commercial Qualification Process



SELECTOR GUIDE

MR HEAD CIRCUITS

Product	# Channels	WDI	Read Gain (V/V) Typ.	Input Noise (nV/ÐHz) Typ.	MR Bias Range (mA)	Write Current Range (mA)	Write Voltage (Vp-p) Min.
V10603	10	PECL	250, 350	0.85	6 - 16	20 - 65	4
V10615	10	PECL	200	0.60	8 - 15	20 - 40	7
VM5131	4, 6		112, 150 or 150, 190	0.60	2 - 9.75	15 - 60	10.8 @ 8V 5.0 @ 5V
VM5141	4, 6, 8		225, 300	0.60	3 - 11	15 - 60	10.8 @ 8V 5.0 @ 5V
VM5430	4, 8	PECL	100 - 250	0.55	2 - 10	15 - 65	6
VM5431	4, 8	PECL	100 - 250	0.55	2 - 10	15 - 65	6
VM5432	4	PECL	100 - 250	0.55	2 - 10	15 - 65	6
VM5435	4, 6, 8	PECL	112 - 316	0.55	2 - 10	10 - 50	6
VM546012	12	PECL	100 - 250	0.55	2 - 10	15 - 65	8
VM546112	12	PECL	100 - 250	0.55	2 - 10	15 - 65	8
VM61210S	10	PECL	150	0.6	8 - 15	20 - 40	7.0
VM6130 Series	12, 14	PECL	350	0.8	8 - 16	20 - 40	5
VM6160 Series	6, 12	PECL	220	0.55	5 - 15	10 - 45	9.5
VM6170S Series	10	PECL	250, 350	0.85	6 - 16	20 - 65	9
VM6180 Series	4, 8	PECL	200, 300	0.73	5 - 16	10 - 50	6
VM6182 Series	4, 8	PECL	200, 300	0.88	5 - 16	10 - 50	6
VM6184 Series	4, 8	PECL	100 - 200	1.0	4 - 14	10 - 45	4 (typ)
VM6185 Series	4, 6, 8	PECL	200, 250	0.67	6 - 18	10 - 63	6
VM61852/4/8 Series	2, 4, 8	PECL	200, 250	0.67	6 - 18	10 - 63	6

Note: Please consult VTC for current information and package availability.

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SELECTOR GUIDE

Servo Write	*Power Supply*	*Programmable*	*Status*	*Comments*
No	+5V, -4.5V	Yes	Obsolete	Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents
Yes	+5V, +3V	No	Obsolete	Thermal Asperity Detection and Compensation
Yes	+5V, +8V	Yes	Advance Info	Pin Layer Reversal Capable, Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, and Writer Overshoot and Undershoot
Yes	+5V, +8V	Yes	Advance Info	Pin Layer Reversal Capable, Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, and Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Dynamic Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, and Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, and Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Thermal Asperity Detection and Compensation Controls, Programmable Bias and Write Currents, Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Programmable Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Programmable Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, Writer Overshoot and Undershoot
Yes	+5V, -5V	Yes	Advance Info	GMR Reader, Programmable Thermal Asperity Detection and Compensation, Programmable Bias and Write Currents, Writer Overshoot and Undershoot
Yes	+5V, -3V	No	Obsolete	Reduced Noise and Transition Times, Available In Die Form For Chip-on-Flex
	+5V	Yes	Obsolete	Thermal Asperity Detection and Compensation
Yes	+5V	No	Obsolete	Thermal Asperity Detection and Compensation
Yes	+5V, -4.5V	Yes	Obsolete	For Dual Chip Applications, Die Form For Chip-on-Flex
Yes	+5V	Yes		Programmable TA Detection, High Write Current
Yes	+5V	Yes		Thermal Asperity Detection and Compensation
Yes	5V	Yes		Thermal Asperity Detection and Compensation
Yes	+5V	Yes	Advance Info	Programmable Read and Write Current
Yes	+5V	Yes	Advance Info	Performance in excess of 220 mbits/sec, Requires One External Component

SELECTOR GUIDE

Product	*# Channels*	*WDI*	*Read Gain (V/V) Typ.*	*Input Noise (nV/ÐHz) Typ.*	*MR Bias Range (mA)*	*Write Current Range (mA)*	*Write Voltage (Vp-p) Min.*
VM6189 Series	4, 8	PECL	138, 220 122, 195	0.8	3 - 12	17 - 52	7 (typ)
VM6203	10	PECL	150 - 300	0.55	AMR 4 - 10 GMR 2 - 5	10 - 50	6 (typ)
VM6204 Series	12	PECL	220, 300	0.55	5 - 12	20 - 60	6 (typ)
VM6205 Series	8	PECL	150, 220	0.55	2 - 8	20 - 60	6 9 typ)
VM6214 Series	12	PECL	220, 300	0.55	2 - 9	20 - 60	6 (typ)
VM623206	6	PECL	220, 300	0.55	3 - 10	20 - 60	6 (typ)

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SELECTOR GUIDE

Servo Write	*Power Supply*	*Programmable*	*Status*	*Comments*
Yes	+5V	Yes	Advance Info	Low Power Detection and Programmable Damping Resistance
Yes	+5V, -5V	Yes	Advance Info	AMR/GMR Reader, Performance in excess of 350 Mbits/sec
Yes	+5V, -5V	Yes	Advance Info	Programmable Read and Write Current, Dual Preamp Control
Yes	+5V, -5V	Yes	Advance Info	Programmable Read and Write Current
	+5V, -5V	Yes	Advance Info	Programmable Read and Write Current
	+5V, -5V	Yes	Advance Info	Programmable Read and Write Current

SELECTOR GUIDE

TWO-TERMINAL PREAMPS

Product	Number of Channels	WDI	Read Gain (V/V) Typ.	Input Noise (nV/ÐHz) Max.	Input Cap. (pF) Max.	Writer Current Gain (mA/mA)	Write Current Range (mA)
VM3500	4, 6, 8	PECL	300	0.50	12	20	5 - 25
VM3600	4, 6, 8	PECL	300	0.54	7	20	5 - 25

MIXED SIGNAL CIRCUITS

Product	Pins	Package Type	Functional Description	Power Supply	Maximum Transfer Rate
VM65011	64	PQFP	Analog PRML Channel for DVC Applications	+5V	Nominal 41.85 Mbits/sec
VM65015	64	PQFP	Analog PRML Channel for Digital VHS Applications	+5V	Nominal 19.14 Mbits/sec
VM65060	80	PQFP	PRML Channel	+5V	180 Mbits/sec

TAPE DRIVE CIRCUITS

Product	Pins	Package Type	Functional Description	Power Supply	Maximum Transfer Rate
V10619	14	VSOP	Inductive, Read Only Differential Preamplifier	+5V	N/A
VT5204	24	SOIC	Inductively Coupled, Read/Write Preamplifier	+5V, +12V	N/A

POWER CONTROL CIRCUITS

Product	Pins	Package Type	Functional Description	Power Range	Maximum Current Capability
VC4005	8	SOIC	+5V to -5V DC Voltage Converter	+3V to +5V	200 mA

Note: Please consult VTC for current information and package availability.

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SELECTOR GUIDE

WRITE VOLTAGE (Vp-p) Min.	Rise/Fall Time L=0, R=0 (ns) Max.	Multiple Servo Write	Head Induct. Range (uH)	Power Supply	WD Flip-Flop On Chip	Status
4.8	2.0	Yes	0.2 - 1.0	+5V	Optional	
5.0	2.6	Yes	0.2 - 1.0	+5V	Optional	

Product Features
5 Tap Adaptive FIR, Vieterbi Path Length of 10 or 21, Dropout Detector, Programmable Write Current Control, Automatic Tracking Frequency Servo Tone Filter and Demodulator
5 Tap Adaptive FIR, Vieterbi Path Length of 10 or 21, Track-Cross Detector, Programmable Write Current Control, Data Rate Adjustment DACs for Both Playback and Trick Play Modes
46 to 180 Mbits/sec Transfer Rate, Programmable 7 Tap Adaptive Filter, Programmable Write Precompensation, 8/9 (0,4/4) Encoder/ Decoder, ZDR, Area Detect Servo

Product Features
High-Performance, Read Only Differential Preamplifier Providing Read Amplification
High-Performance, Read/Write Preamplifier Designed for a Helical-Scan Head Tapes Drives

Product Features
High Efficiency, Switched Capacitor Voltage Converter with Selectable Frequency

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Sections

Magneto-Resistive (MR) Read/Write Preamplifiers

VTC Inc.
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V10603

MAGNETO-RESISTIVE HEAD, HIGH PERFORMANCE, READ/WRITE PREAMPLIFIER

990811 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection, TA Threshold and Options Control)
  - Operates from +5 and -4.5 Volt Power Supplies
  - Up to 10-Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Current Sense Configuration
  - MR BIAS Current 5-bit DAC, 6.2 - 16.4 mA Range
  - Programmable Read Voltage Gain
    (250 V/V or 350 V/V)
  - Fast Read Mode
  - Input Noise = 0.85 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 18 pF Typical
  - Head Inductance Range = 100 nH - 300 nH
  - Mask Select Resistors (0, 10, 15, 30 Ω) in series with RDP, RDN
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 65 mA Range
  - Rise Time = 1.5 ns Typical (L_{total} = 66 nH, I_W = 65 mA)
  - Write Head Inductance Range, 75-200nH

DESCRIPTION

The V10603 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) read/thin film write heads. The V10603 contains a thin-film head writer, an MR reader, and associated fault circuitry. It provides bias current and control loops for setting the DC voltages on the MR element.

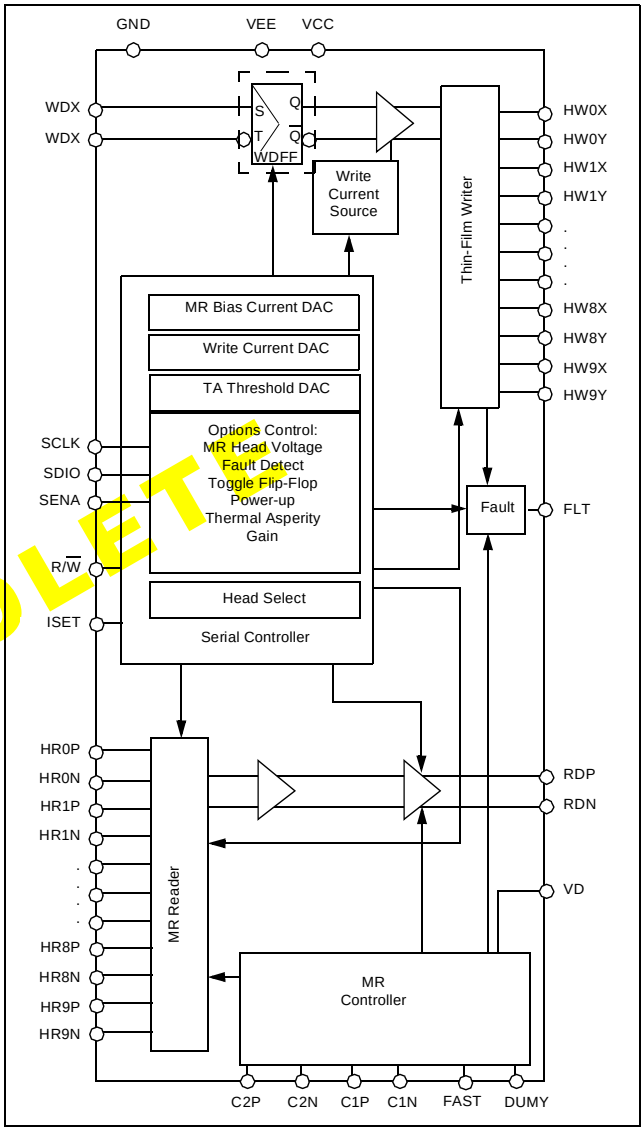
Programmability of the V10603 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, read gain and thermal asperity detection threshold.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, an internal pull-up resistor is connected to the mode select line (R/$\overline{W}$) to prevent accidental writing due to an open line.

The V10603 operates from +5V, -4.5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The V10603 is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



See page 9 for the Pin Function List and Description.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +6V

Read Bias Current, I_{MR} 30mA
Write Current, I_W 100mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -4.5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 20 - 65 mA
Write Head Inductance, L_W ..... 100 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 6 - 16 mA
Read Head Inductance, L_{MR} ..... 10 - 100 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J ..... 0°C to 125°C

Serial Interface Controller

The V10603 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 3 and 4 for a bit description.

Note: Although the serial interface is available during all modes, VTC recommends no serial activity during read and write operations (except to enter Idle mode) since errors may be generated.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, four reserved preamp bits <A7-A5, A1>, and three register address bits <A4-A2>. The second 8 bits <D7-D0> consist of six data bits <D7-D2> and two reserved timing bits <D1-D0>.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the rising edge of the 10th cycle (delayed two cycles to allow the controller to release control of SDIO). Upon the falling edge of the 11th cycle <D2> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. Two reserved timing bits <D1-D0> allow time for the controller to tristate on line SDIO and the V10603 to drive line SDIO.

See Table 7 and Figures 9 and 10 for serial interface timing information.

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the serial registers (the contents of which remain latched).

Idle mode is controlled with the PWRUP bit (register 3, bit <D7>). Note that this bit is the only means of entering idle mode or powering the V10603 out of Idle mode without a fault. This bit has a power-on-reset value of <0> which enables Idle Mode.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The V10603 uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external resistor (2.5kΩ nominal, connected between pin ISET and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{15.5}{(R_{SET})} + k_{IMR}\left(\frac{0.823}{R_{SET}}\right) \qquad \textit{(eq. 1)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{SET} represents the equivalent resistance between the ISET pin and ground (in Ω).
k_{IMR} represents the MR bias DAC setting (0 to 31).

The above I_{MR} equation will give a bias current range of 6.2-16.4 mA.

With the use of a negative supply, the MR head center voltage is near ground potential minimizing current spikes during disk contact.

LOWG (Low Gain)

This control bit (register 0, bit <D2>) selects the gain. When high, a gain of 250 V/V is used; when low, a gain of 350 V/V is used. This bit has a power-on-reset value of <0> which selects high gain (350 V/V).

MRHVE (MR Head Voltage Enabled)

This control bit (register 2, bit <D2>) enables the output of the (I_{MR}×R_{MR}) product of the selected head at the RDP-RDN differential outputs.

Note: For MRHVE to be active, High gain must be selected (register 0, <D2> = 0).

$$I_{MR} \times R_{MR} = V_{MRDC} - V_{OS} \qquad \text{RevE} \qquad \textit{(eq. 2)}$$

$$I_{MR} \times R_{MR} = V_{MRDC} \qquad \text{RevG}$$

$I_{MR} \times R_{MR}$ represents the bias-current/head-resistance product.
V_{MRDC} represents the voltage measured at RDP-RDN with MRHVE=1.
V_{OS} represents the Output Offset Voltage

Fast Read Mode

The Fast Read mode, when enabled, increases the transconductance (tail current) of the first stage of the read amplifier. This effectively increases the lower corner frequency of the amplifier's bandpass by a factor of approximately 15 to 20 without changing the gain.

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MR Bias DAC

The 5 bits in register 1 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, loaded LSB first).

Thermal Asperity Detection

If a head-to-disk contact occurs, the thermal asperity in the MR element will result in a fault condition. The threshold for thermal asperity detection is governed by the following equation:

$$V_{TADT} = 0.3 + (0.119355 \times k_{TADT}) \quad \textit{(eq. 3)}$$

V_{TADT} represents the TA threshold (input-referred in mVb-p).
k_{TADT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will reset only after the amplitude falls to 40% of the programmed detection threshold. (Hysteresis is disabled for the lower half of the programmable threshold range.)
The thermal asperity detection circuitry may be disabled with the TADD bit (register 3, bit <D2>). This bit has a power-on-reset value of <0> which enables thermal asperity detection.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- MR open head detected
- Thermal Asperity detected
- Low power supply voltage
- Device in write mode

The fault detection circuitry may be disabled with the FLTD bit (register 1, bit <D2>). This bit has a power-on-reset value of <0> which enables fault detection.

Write Mode

In the write mode, the circuit operates as a current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.5kΩ resistor (connected between pin ISET and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{50}{R_{SET}} + k_{IW}\left(\frac{3.629}{R_{SET}}\right)\right] \quad \textit{(eq. 4)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{SET} represents the equivalent resistance between the ISET pin and ground (in Ω).
k_{IW} represents the write current DAC setting (0 to 31).

The above I_W equation will give a write current range of 20-65 mA.

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head. See Figure 11 for a timing diagram.

Write Current DAC

The 5 bits in register 2 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, loaded LSB first).

Write-to-Read Recovery Enhancement

The following conditions are maintained to reduce write-to-read recovery time:

- MR bias current is maintained in write mode
- Reader outputs are high impedance so that the AC-coupling capacitors hold their charge until the next read

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open head
- No write current
- Head short to ground (Rev G only)

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Low power supply voltage
- Device in read mode

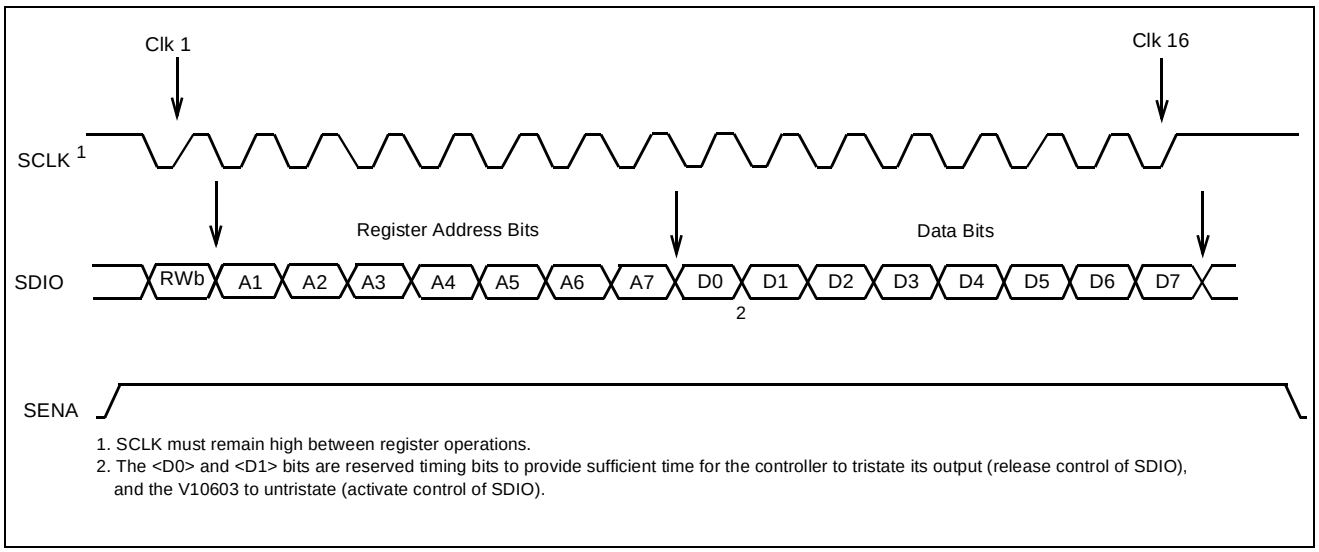
Table 1 Head Select

HS3 3:<D6>	*HS2 3:<D5>*	*HS1 3:<D4>*	*HS0 3:<D3>*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(all other combinations)				0

Note: The head-select lines are equipped with pull-down resistors to ensure known default head selection (head 0). Note that head 0 is selected for all unrecognized head-select codes.

Table 2 DUMY Mode for Bias Current

DUMY (bias only)	*CONDITION*
0	Bias current flows to the selected head. (see Table 1)
1	Bias current flows to a dummy head. (a 42Ω resistor)



1. SCLK must remain high between register operations.
2. The <D0> and <D1> bits are reserved timing bits to provide sufficient time for the controller to tristate its output (release control of SDIO), and the V10603 to untristate (activate control of SDIO).

Figure 8 Serial Port Protocol

Table 3 Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A1>*							*R/W Bit <A0>*
Thermal Asperity / Gain	0	1	1	1	0	0	0	1	1/0
MR Bias / Fault Detect	1	1	1	1	0	0	1	1	1/0
Write Current DAC / MR Head Voltage	2	1	1	1	0	1	0	1	1/0
Power Up / Head Select / Thermal Asperity Disable	3	1	1	1	0	1	1	1	1/0
Vendor ID	4 (read only)	1	1	1	1	0	0	1	1

1. Reserved and not decoded

Table 4 Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Thermal Asperity / Gain	0	TADT4	TADT3	TADT2	TADT1	TADT0	LOWG	1	1
MR Bias / Fault Detect	1	IMR4	IMR3	IMR2	IMR1	IMR0	FLTD	1	1
Write Current DAC / MR Head Voltage	2	IW4	IW3	IW2	IW1	IW0	MRHVE	1	1
Power Up / Head Select / TA Disable	3	PWRUP	HS3	HS2	HS1	HS0	TADD	1	1
Vendor ID	4	2	2	2	2	2	2	1	1

1. Reserved
2. Read Only Register/Bits:
   Register 4:<D1-D0> is reserved for serial I/O timing.
   Register 4:<D4-D2> is preamp revision level (Rev E = 100, Rev G = 110).
   Register 4:<D5>=1 indicates bump die.
   Register 4:<D7-D6> is the Vendor ID. (VTC = 00).

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Table 5 Mode Select

R/$\overline{W}$	*FAST*	*PWRUP 3:<D7>*	*MODE*
1	0	1	Read
1	1	1	Read Fast
0	X	1	Write
X	X	0	Idle

Table 6 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Thermal Asperity / Gain	0	<0000 0000>
MR Bias / Fault Detect	1	<0000 0000>
Write Current DAC / MR Head Voltage	2	<0000 0000>
Power Up / Head Select / TA Disable	3	<0000 0000>
Vendor ID	4	<0000 0000>

Table 7 Serial Interface Parameters

DESCRIPTION	Operational Limits	SYMBOL	MIN	NOM	MAX	UNITS
Serial Clock (SCLK) Rate	Read or Write				20	MHz
SENA to SCLK setup time	Read or Write	T_{SENS}	65			nS
SDIO to SCLK setup time	Read or Write	T_{DS}	15			nS
SDIO from SCLK hold time	Read or Write	T_{DH}	10			nS
SCLK cycle time	Read or Write	T_C	50			nS
SCLK high time	Read or Write	T_{CKH}	20			nS
SCLK low time	Read or Write	T_{CKL}	20			nS
SENA from SCLK hold time	Read or Write	T_{SHLD}	20			nS
Time between I/O operations	Read or Write	T_{SL}	100			nS
Time to tristate controller driving SDIO (release control of SDIO) [1]	Read	T_{TRIC}			40	nS
SCLK falling edge to read data valid	Read	T_{ACT}			20	nS
Duration of SENA	Read or Write	T_{RD}	885			nS
SENA to SDIO Tristate Delay	Read or Write	T_Z			50	nS

1. Maximum time controller can be on bus after last address bit is sent.

Note: **SerEna** assertion level is high.
SCLK must remain high between register operations.

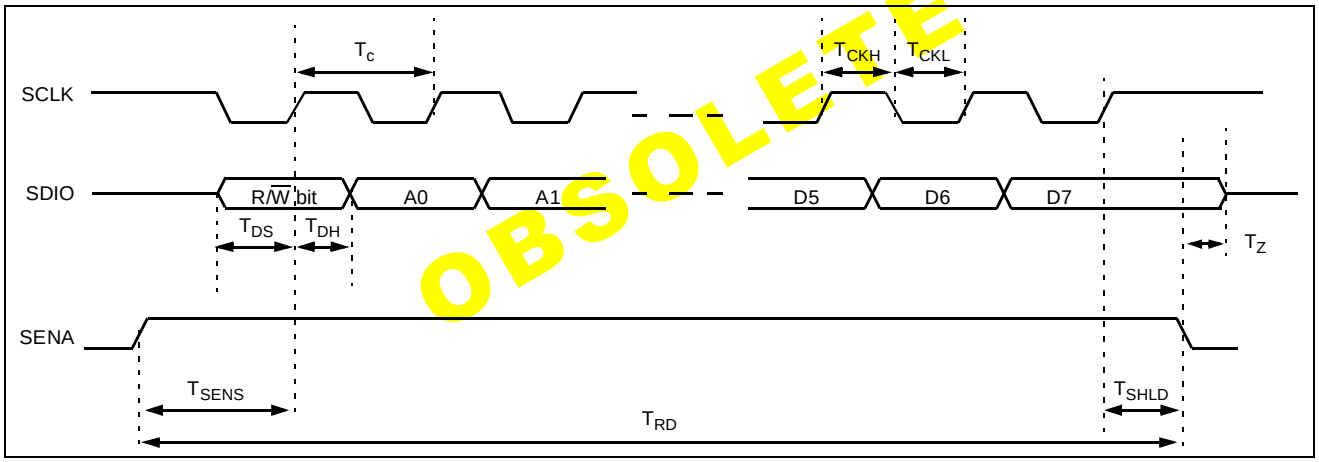


Figure 9 Serial Port Timing

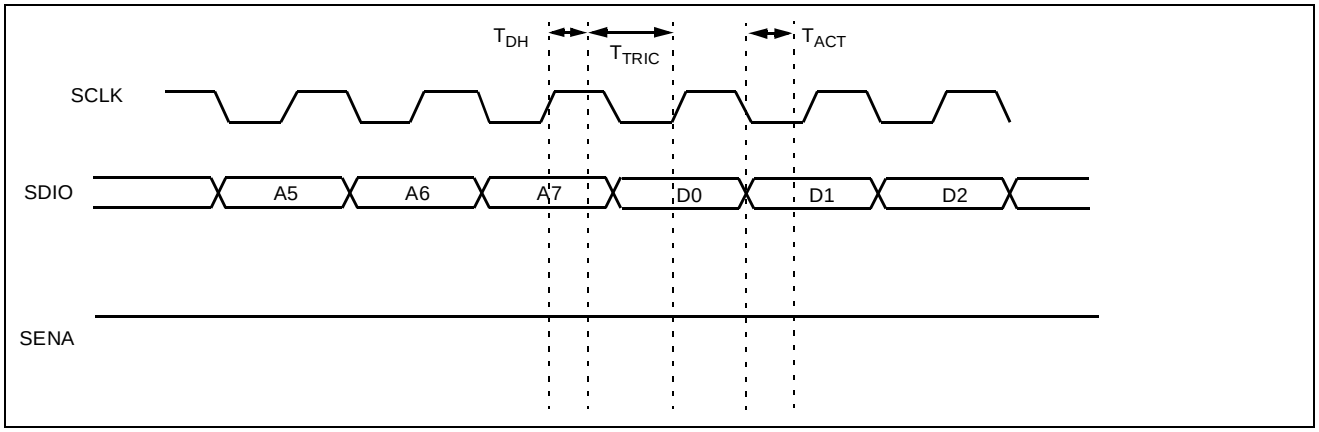


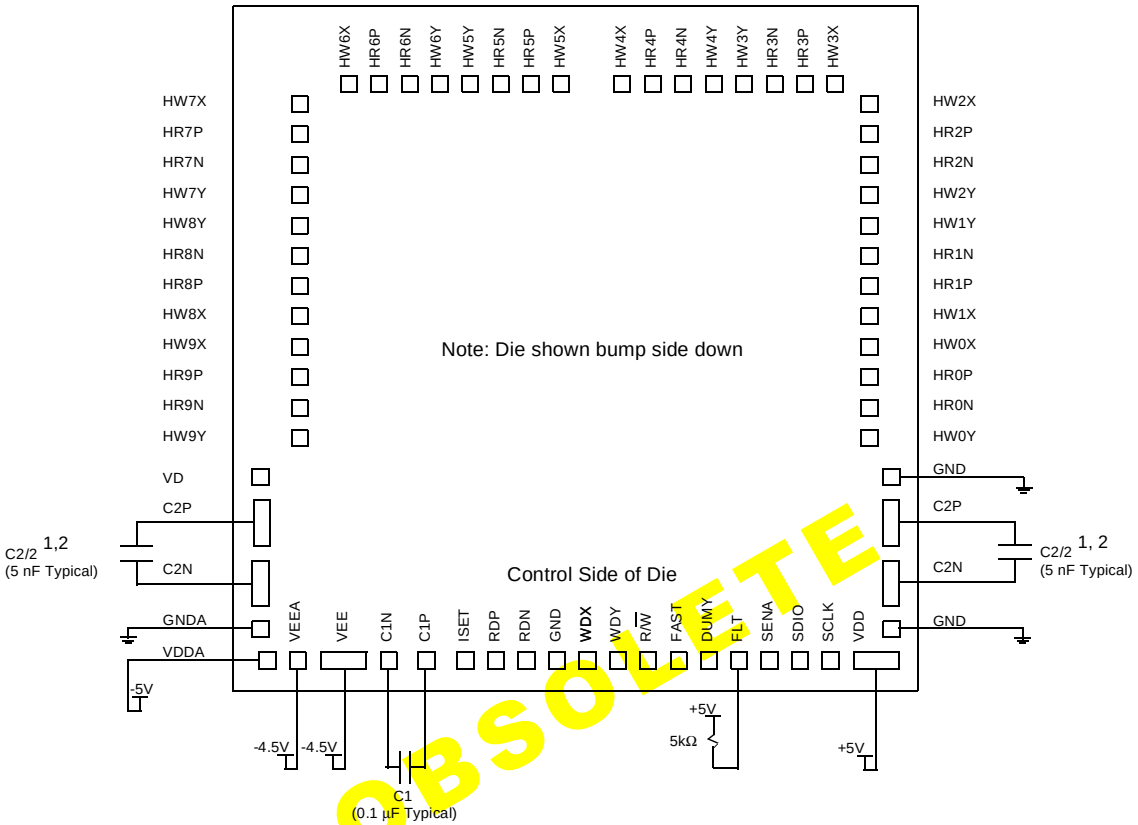
Figure 10 Serial Port Timing - Tristate Control

PIN FUNCTION LIST AND DESCRIPTION

Symbol	*Input/ Output*	*Description*
DUMY	I	Dummy Head for bias current: A TTL high level selects a dummy head (for MR bias current only). Pin defaults low (non-dummy).
R/$\overline{W}$	I [1]	Read/$\overline{\text{Write}}$: A TTL low level enables write mode. Pin defaults high (read mode).
FLT	O [1]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
WDX, WDY	I [1]	Differential Pseudo-ECL write data inputs: Positive edge on WDX toggles the direction of the head current.
HR0P- HR9P	I	MR head connections, positive end.
HR0N- HR9N	I	MR head connections, negative end.
HW0X- HW9X	O	Thin-Film write head connections, positive end.
HW0Y- HW9Y	O	Thin-Film write head connections, negative end
RDP, RDN	O [1]	Read Data: Differential read signal outputs.
C1P, C1N		Noise bypass capacitor input for the MR bias current source.
C2P, C2N		Compensation capacitor for the MR head current loop.
VD	I [1]	Analog Voltage reference for disk bias.
VEE		-4.5V supply
VCC		+5.0V supply
GND		Ground
ISET	[1]	Reference Current for both MR Bias and Write Current.
FAST	I [1]	FAST Read Mode: A TTL high level enables FAST read mode. Pin defaults low (FAST disabled).
SENA	I	Serial Enable: Serial port enable signal; see Figures 9 and 10.
SCLK	I [1]	Serial Clock: Serial port clock; see Figures 9 and 10.
SDIO	I/O	Serial Data: Serial port data; see Figures 9 and 10.

1. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



1. Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.
2. This capacitor is split to minimize parasitics from all heads to the AC-coupling capacitor.
   A single C2 capacitor may be connected to either set of C2P/C2N pads, however, performance may be compromised with a single C2 capacitor configuration.

Application Notes:

1) VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:

   VCC - GND
   VEE - GND

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
$0^oC<T_J<125^oC$, $4.5V<V_{CC}<5.5V$, $-5.0V<V_{EE}<-4.0V$, $k_{IMR} = 16$, $k_{IW} = 31$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Power Supply Current	I_{CC}	Read Mode, Serial I/O Active		99	113	mA
		Read Mode, Serial I/O Inactive		85	100	
		Write Mode		155	175	
		Idle Mode, Serial I/O Active		24		
		Idle Mode, Serial I/O Inactive		15	20	
V_{EE} Power Supply Current	I_{EE}	Read Mode		55	65	mA
		Write Mode		133	145	
		Idle Mode		7	12	
Power Supply Dissipation	P_d	Read Mode, Serial I/O Active		765	864	mW
		Read Mode, Serial I/O Inactive		673	793	
		Write Mode		1374	1528	
		Idle Mode, Serial I/O Active		156	175	
		Idle Mode, Serial I/O Inactive		107	154	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		CMOS	3.5		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{IH} - 1.5		V_{IH} - 0.25	V
		CMOS	-0.3		1.5	V
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{CC} Fault Threshold	V_{CTH}		3.75	4.00	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75	-3.50	-3.25	V
Disk Reference Voltage Range	V_D		-250	0	250	mV
Bias Reference Voltage	V_{SET}	R_{SET} = 2500Ω		2.5		V
Monitored MR DC Voltage Accuracy (RDP-RDN)	V_{MRDC}	Revision E MHVRE = 1	-22		+18	%
		Revision G MHVRE = 1	-10		+10	%

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
$0^{o}C<T_J<125^{o}C$, $4.5V<V_{CC}<5.5V$, $-5.0V<V_{EE}<-4.0V$, $k_{IMR} = 16$, $k_{IW} = 31$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Head Current (HWnX, HWnY)	I_H	Read/Idle Mode $0 < V_{CC} < 5.5V$, $-4.95 < V_{EE} < 0$	-200	0	200	µA
		Write Mode $0 < V_{CC} < 5.5V$, $-4.95 < V_{EE} < 0$	-200	0	200	
		Invalid/Unselected Head	-200	0	200	
		Idle Mode	-200	0	200	

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. $0^oC<T_J<125^oCC$, $4.5V<V_{CC}<5.5V$, $-5.0V<V_{EE}<-4.0V$, $k_{IMR}=16$, $k_{IW}=31$, L_{MR} = 25nH, R_{MR} = 42Ω, RSET = 2500Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		6.2		16.4	mA
MR Head Current Tolerance	I_{MR}	x = 6.2 + 0.329k_{IMR}	0.95x		1.05x	mA
Unselected MR Head Current					100	µA
I_{SET} to MR Bias Current Gain	A_{IMR}	k_{IMR} = 31		16		mA/ mA
Differential Voltage Gain	A_V	V_{IN} = 2mV_{pp} @5MHz, LOWG=0	260	350	440	V/V
		V_{IN} = 2mV_{pp} @5MHz, LOWG=1	185	250	315	
Passband Upper Frequency Limit	f_{HR}	-1dB		TBD		MHz
		-3dB	112			
Passband Lower -3dB Frequency Limit	f_{LR}	C_2 = 6nF	0.1	0.3	0.5	MHz
Passband Lower -3dB Frequency Limit, Fast Recovery Mode	f_{LRF}	$\overline{FAST}$ low		6		MHz
Equivalent Input Noise	e_{in}	1 < f < 120 MHz excluding R_{MR}		0.85		nV/ √Hz
Differential Input Capacitance	C_{IN}	k_{IMR}=16			10	pF
Differential Input Resistance	R_{IN}	k_{IMR}=16			5.8	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 2mV_{pp} @ f = 5 MHz	4			mV_{pp}
Common Mode Rejection Ratio	CMR R	100mV_{PP} on center or R_{MR}, 1 < f < 50 MHz	15			dB
Power Supply Rejection Ratio	PSRR	100mV_{PP} on V_{CC} or V_{EE}, 1 < f < 50 MHz	30			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV_{PP}, 1 < f < 120 MHz	15			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	MRHVE = 0	V_{CC} - 2.9	V_{CC} - 2.6	V_{CC} - 2.2	V
Single-Ended Output Resistance	R_{SEO}	Includes 10Ω resistor in series with reader output; R_{SEO} = [$V_{RDP/N}$ (I_O=-0.5mA) - $V_{RDP/N}$ (I_O=+0.5mA)] / 1mA		30 [1]		Ω
Output Current	I_O	AC-Coupled Load, RDP to RDN, Read mode	±2.5			mA
		AC-Coupled Load, RDP to RDN, Any other mode			1	µA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. $0^oC<T_J<125^oCC$, $4.5V<V_{CC}<5.5V$, $-5.0V<V_{EE}<-4.0V$, $k_{IMR}=16$, $k_{IW}=31$, L_{MR} = 25nH, R_{MR} = 42Ω, RSET = 2500Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK} = 10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			20	mA
MR Head Potential, Selected Head	V_{MR}	I_{MR} = 11.3 mA	V_D - 500		V_D + 500	mV
Total Harmonic Distortion	THD	Vin = 4mVpp, ten harmonics		0.5		%
Thermal Asperity Detection Threshold	TADT	x = 0.3 + 0.119355k_{TADT} Input-Referred, R_{SET} = 2500Ω	0.75x		1.25x	mV_{b-p}

1. Includes 10Ω resistor in series with reader output.

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. $0^oC < T_J<125^oC$, $4.5V < V_{CC} < 5.5V$, $-5.0V < V_{EE} < -4.0V$, k_{IW} = 31, I_W = 65mA, L_H = 90nH, R_H = 17Ω, RSET = 2500Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SET} to Write Current Gain	A_{IW}			65		mA/mA
Write Current Range	I_W		20		65	mA
Write Current Tolerance	ΔI_W	x = 20 + 1.452k_{IW},	0.92x		1.08x	mA
Differential Head Voltage Swing	V_{DH}	Open Head	9	10		V_{pp}
Unselected Head Voltage	V_{UH}	k_{IW} = 16, DC	-250		250	µA
Differential Output Capacitance	C_O				5	pF
Write Data for Safe Condition	F_{SAFE}	FLT low	2			MHz
Time Between Transitions for Fault Inhibition	t_{INH}	FLT function inhibited		15	23	ns

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
$0^oC < T_J<125^oC$, f_{DATA} = 5MHz, L_H = 66nH, R_H = 14Ω, I_W = 65mA, RDP/RDN Channel Impedance < 500Ω, C2 = 6.6nF.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current		30	200	ns
R/$\overline{W}$ to Read Mode	t_{WR}	To within 10mV of DC level; C_2 = 5.6nF		0.5	1.0	µs
Idle (SCLK 16th rising edge) to Read Mode	t_{pu}	To within 10mV of DC level; FAST = low		7	20	µs
		FAST = high		5		
Head (SCLK 16th rising edge) to Any Head (including DUMY)	t_{HS}	To within 10mV of DC level; FAST = low		4	15	µs
		FAST = high		2		
SCLK 16th rising edge to Unselect	t_{RI}	To 10% of read envelope or write current		0.3	0.6	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
$0^{o}C < T_J < 125^{o}C$, f_{DATA} = 5MHz, L_H = 66nH, R_H = 14Ω, I_W = 65mA, RDP/RDN Channel Impedance < 500Ω, C2 = 6.6nF.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
I_{MR} (max) to I_{MR} (min)	t_{IMR}	To 90% of envelope		0.5		µs
I_{MR} (min) to I_{MR} (max)	t_{IMR}	To 90% of envelope		7		µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			20	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H = 0, R_H = 0			0.2	ns
Rise/Fall Time	t_r / t_f	20-80%		1.5	1.9	ns
Settling Time	t_{WSET}	± 10%		20		µs
Overshoot	W_{cov}			50	80	%

1. See Figure 11 for a write mode timing diagram.

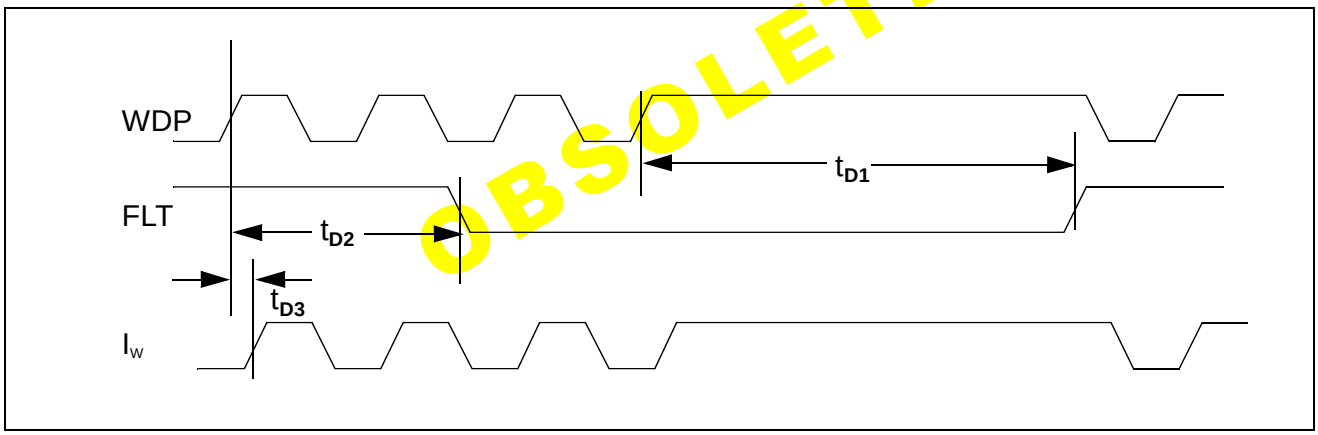


Figure 11 Write Mode Timing Diagram

V10603

10-CHANNEL DIE

Specific Characteristics

Die size: 192 X 191 Mils

Pad Coordinates for the V10603 (in Mils)

Pin Name	X Axis	Y Axis	Pad Size
C1N	52.913	-87.510	4x8
C1P	42.480	-87.510	4x8
C2N	90.965	-62.569	4x12
C2N	90.965	-70.581	4x12
C2N	-90.965	-62.736	4x12
C2N	-90.965	-70.748	4x12
C2P	90.965	-46.555	4x12
C2P	90.965	-54.567	4x12
C2P	-90.965	-46.722	4x12
C2P	-90.965	-54.734	4x12
DUMY	-42.943	-87.510	4x4
FAST	-34.941	-87.510	4x4
FLT	-50.945	-87.510	4x4
ISET	21.713	-87.510	4x4
HR0N	-77.185	-21.831	4x4
HR1N	-77.185	18.228	4x4
HR2N	-77.185	42.264	4x4
HR3N	-48.248	73.780	4x4
HR4N	-24.242	73.780	4x4
HR5N	24.242	73.780	4x4
HR6N	48.248	73.780	4x4
HR7N	77.185	42.264	4x4
HR8N	77.185	18.228	4x4
HR9N	77.185	-21.831	4x4
HR0P	-77.185	-13.819	4x4
HR1P	-77.185	10.217	4x4
HR2P	-77.185	50.276	4x4
HR3P	-56.250	73.780	4x4
HR4P	-16.240	73.780	4x4
HR5P	16.240	73.780	4x4
HR6P	56.250	73.780	4x4
HR7P	77.185	50.276	4x4
HR8P	77.185	10.217	4x4
HR9P	77.185	-13.819	4x4
RDN	5.384	-87.510	4x4
RDP	13.711	-87.510	4x4
RNW	-26.939	-87.510	4x4

Pin Name	X Axis	Y Axis	Pad Size
SCLK	-74.951	-87.510	4x4
SDIO	-66.949	-87.510	4x4
SENA	-58.947	-87.510	4x4
GND	-2.933	-87.510	4x4
GND	-90.965	-38.720	4x4
GND	-90.965	-78.750	4x4
GND	90.965	-79.045	4x8
VD	90.965	-38.553	4x4
VDD	-82.953	-86.752	4x12
VDD	-90.965	-86.752	4x12
VDDA	88.287	-87.510	4x8
VEE	61.378	-87.510	4x12
VEE	69.390	-87.510	4x12
VEEA	77.854	-87.510	4x8
HW0Y	-77.185	-29.843	4x4
HW1Y	-77.185	26.240	4x4
HW2Y	-77.185	34.252	4x4
HW3Y	-40.246	73.780	4x4
HW4Y	-32.244	73.780	4x4
HW5Y	32.244	73.780	4x4
HW6Y	40.246	73.780	4x4
HW7Y	77.185	34.252	4x4
HW8Y	77.185	26.240	4x4
HW9Y	77.185	-29.843	4x4
HW0X	-77.185	-5.807	4x4
HW1X	-77.185	2.205	4x4
HW2X	-77.185	58.287	4x4
HW3X	-64.252	73.780	4x4
HW4X	-8.238	73.780	4x4
HW5X	8.238	73.780	4x4
HW6X	64.252	73.780	4x4
HW7X	77.185	58.287	4x4
HW8X	77.185	2.205	4x4
HW9X	77.185	-5.807	4x4
WDY	-18.937	-87.510	4x4
WDX	-10.935	-87.510	4x4

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

VTC Inc.
Value The Customer™

V10615

10-CHANNEL, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE CAPABILITY

990811 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - Operates from +5 and -3 Volt Power Supplies
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current Range 8 - 15 mA
  - Read Voltage Gain = 200 V/V Typical
  - Input Noise = 0.60 nV/√Hz Typical
  - Input Capacitance = 16 pF Typical
  - Head Inductance Range = 100 nH to 600 nH
  - Fast Thermal Asperity Recovery Mode
- *High Speed Writer*
  - Write Current Range = 20 - 40 mA
  - Rise Time = 2.0 ns Typical (L_H = 220 nH, I_W = 30 mA)
  - Multi-Channel Servo Write
  - Optional WDFF as a bondable option

DESCRIPTION

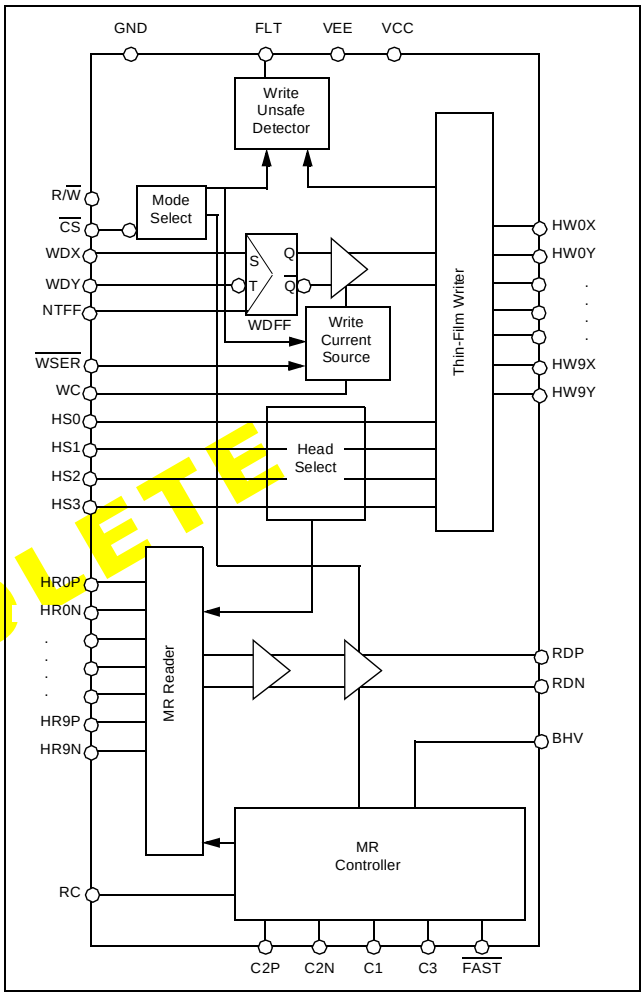
The V10615 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. It provides bias current and control loops for setting the DC voltages on the MR element. The V10615 also provides a servo write feature, enabling the user to write servo information directly through the preamplifier.

Fault protection circuitry ensures that the write current generator is disabled during power sequencing, voltage faults or an invalid head select. This protects the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines (CS and R/W) to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition. Internal pull-up resistors are also provided on the FAST pin (to disable the fast thermal recovery mode) and the WSER pin (to ensure non-servo mode).

The V10615 operates from +5V, -3V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The V10615 is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -5V
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... V_{EE} -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... V_{EE} -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{EE} ..... -3V ± 10%
V_{CC} ..... +5V ± 10%
Junction Temperature (T_J) ..... 10°C to 125°C

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk. The bias generator, input multiplexer, read preamp and read fault detection circuitry is active.

The appropriate TTL levels on the $\overline{CS}$ and R/$\overline{W}$ lines place the preamp in the read mode (see Table 8) and activate the bias generator, the read preamp and the read fault detection circuitry.

The V10615 uses the current bias / voltage sensing MR design. The MR bias current amplitude is determined by an external resistor or an external current source and is described by the following equation:

$$I_{MR} = \frac{40}{R_{RC}} \qquad \textit{(eq. 5)}$$

I_{MR} represents the magnitude of the bias current (in mA).
R_{RC} represents the equivalent resistance between the RC pin and ground (in kΩ).

Due to the use of a negative supply, the MR head center voltage is at ground potential minimizing current spikes during disk contact.

Fast Mode

Applying a TTL low level to the $\overline{FAST}$ pin enables the fast recovery mode. In fast mode, the first stage current is increased by a factor of three to reduce the recovery delay from a thermal asperity.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault can be triggered by any of the following conditions:

- MR bias current too high (1.5 times its programmed value)
- Low power supply voltage

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head. The write unsafe detect circuitry is activated.

The appropriate TTL levels on the $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines place the preamp in the write mode (see Table 8) and activate the write unsafe detect circuitry.

The write current magnitude is determined either by an external resistor or an external current source and is defined by the following equation:

$$I_W = \frac{39}{R_{WC} \times \left(1 + \frac{R_H}{R_D}\right)} \qquad \textit{(eq. 6)}$$

I_W represents the magnitude of the write current (in mA).
R_{WC} represents the equivalent resistance between the WC pin and ground (in kΩ).
R_H represents the series resistance of the head (in kΩ).
R_D represents the internal damping resistance (in kΩ).

Write data pseudo-ECL signals on the WDX and WDY lines drive the current switch of the thin film writer either directly or via the optional internal flip-flop.

Note: The flip-flop is enabled when the NTFF pad is connected to ground (a wire-bond option).

Fault Detection

In the write (and servo write) mode, a TTL high on the FLT line indicates a fault condition. The fault can be triggered by any of the following conditions:

- WDI frequency too low
- Open write head
- Write Head short to ground
- No write current programmed

In addition to triggering a fault the following conditions will result in the shutdown of the write current source internal to the chip:

- Low power supply voltage
- Invalid head select code
- Non-write mode

Servo Write Mode

Low TTL levels on $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$ place the chip in servo write mode.

In servo mode, five channels of the V10615 are written simultaneously. Pin $\overline{WSER}$ controls the servo mode and pin HS0 controls which five heads are simultaneously written. See Table 2 for servo head selection description.

Note: When writing multiple heads, there is a limit to the write current duty cycle that can be used without approaching the maximum junction temperature. This maximum duty cycle is contingent on package type, number of heads selected, write current, heatsinking and airflow. DC erase using multiple heads will exceed the maximum allowable power dissipation.

Table 8 Mode Select

$\overline{CS}$	*R/$\overline{W}$*	*$\overline{WSER}$*	*MODE*
0	1	X	Read
0	0	1	Write
0	0	0	Servo
1	X	X	Idle

Table 9 Servo Mode Head Select

HS0	*DESCRIPTION*
0	Heads 0, 1, 2, 3, and 4
1	Heads 5, 6, 7, 8, and 9

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Table 10 Head Select

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	X	DUMMY[1]
1	1	X	X	DUMMY[1]

1. All other HS combinations select an internal dummy head.

Table 11 Pin Function List and Description

Signal	*I/O*[1]	*Description*
BHV	O[2]	Buffered MR Head Voltage output.
C1		Noise bypass capacitor input for the MR bias current source.
C2P, C2N		Reader AC-coupling capacitor.
C3		Compensation capacitor for the MR head current loop.
$\overline{CS}$	I	Chip select: A TTL low level enables the device. The default is high (disabled).
$\overline{FAST}$	I[2]	Fast Mode: A TTL low level enables the fast thermal recovery mode. The default is high (disabled).
FLT	O[2]	Write/Read Fault: TTL high level indicates a fault in write mode. A low level indicates a fault in read mode.
GND	-	Ground
HR0N-HR9N	I	MR head connections, negative end.
HR0P-HR9P	I	MR head connections, positive end.
HS0-HS3	I[2]	Head Select: Selects one of the ten heads.
HW0X-HW9X	O	Thin-Film write head connections, positive end.
HW0Y-HW9Y	O	Thin-Film write head connections, negative end
NTFF		The write data flip-flop is enabled when this pad is connected to ground.
R/$\overline{W}$	I[2]	Read/Write: A TTL high level enables read mode. The default is high (read mode).
RC	[2]	MR bias current reference pin: Sets the magnitude of MR bias current.
RDP, RDN	O[2]	Read Data: Differential read signal outputs.
VCC	-	+5.0V supply
VEE	-	-3.0V supply
WC	[2]	Write current reference pin: Sets the magnitude of write current.
WDX, WDY	I[2]	Write Data Inputs: Differential Pseudo-ECL.
$\overline{WSER}$	I[2]	Write Servo: A TTL low level enables servo mode. The default is high (non-servo).

1. I=Input pin, O=Output pin.
2. When more than one device is used, these signals can be wire-OR'ed together.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, I_w = 30mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Power Supply Current	I_{CC}	Read Mode		75	88	mA
		Write Mode		133	150	
		Idle Mode		4.5	5	
		Fast Mode		98	118	
		Servo Mode, I_W = 20mA		290	325	
V_{EE} Power Supply Current	I_{EE}	Read Mode		51	61	mA
		Write Mode		101	115	
		Idle Mode		1.15	1.5	
		Fast Mode		71	86	
		Servo Mode, I_W = 20mA		230	265	
Power Supply Dissipation	P_d	Read Mode		528	686	mW
		Write Mode		1065	1205	
		Idle Mode		26	33	
		Fast Mode		703	933	
		Servo Mode, I_W = 20mA		2354	2662	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{CC} - 1.9		V_{CC} - 1.6	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{CTH}	V_{EE} = -3.0V	3.6	3.8	4.0	V
V_{EE} Fault Threshold	V_{ETH}	V_{CC} = 5.0V	-2.3	-2.1	-1.9	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, R_{MR} = 22Ω, L_{MR} = 80nH.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}		8		15	mA
MR Head Current Tolerance	I_{MR}	8 < I_{MR} < 15 mA	-5		+5	%
Unselected MR Head Current					100	µA
MR Bias Reference Voltage	V_{RC}	2667 < R_{RC} < 4000 Ω	1.9	2.0	2.1	V
IRC to MR Bias Current Gain	A_{IMR}	2667 < R_{RC} < 4000 Ω		20		mA/mA
Differential Voltage Gain	A_V	V_{IN} = 2mV_{pp} @ 5 MHz, R_L(RDP, RDN) = 10kΩ	140	200	260	V/V
		Fast Mode	110	185	260	
Passband Upper Frequency Limit	f_{HR}	-1dB, Dependent on C2 parasitics	50	55		MHz
		Fast Mode	50	55		
		-3dB, Dependent on C2 parasitics	90	95		
		Fast Mode	80	85		
Passband Lower -3dB Frequency Limit	f_{LR}		0.1		0.8	MHz
Equivalent Input Noise	e_n	5 < f < 20 MHz		0.60	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}			16	20	pF
		Fast Mode		20	25	
Differential Input Resistance	R_{IN}		1200	2100		Ω
		Fast Mode	600	1000		
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 2mV_{pp} @ f = 5 MHz	8	20		mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, f=10MHz	45	60		dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, f=10MHz	40	45		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, f=10MHz	45	50		dB
Output Offset Voltage	V_{OS}		-150		150	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.7	V_{CC} - 3.2	V_{CC} - 2.7	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)	-250	50	250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		30	50	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	-1.5		+1.5	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, R_{MR} = 22Ω, L_{MR} = 80nH.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK}=10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK}=300pF, R_{DISK}=10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}		-350		350	mV
Buffered Head Voltage Error	BHV	(I_{MR} • R_{MR}) - BHV	-10		+10	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 15Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}		1.9	2.0	2.1	V
I_{WC} to Write Current Gain	A_I			20		mA/mA
Write Current Range	I_W		20		40	mA
Write Current Tolerance	ΔI_W	20 < I_W < 40 mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open Head, I_W = 40mA, V_{CC} = 4.5V, V_{EE} = -2.7V	7.0	8.0		V_{pp}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	(with internal damping resistor)	3760	4700	5640	Ω
Open Head Detect Frequency	f_{OHD}	Open Head		[1]	17	MHz
Open Head Detect Resistance	R_{OHD}	I_W = 40mA, V_{CC} = 4.6V		[2]	26	Ω
Write Data Freq. for Safe Condition	f_{DATA}	FLT low, < 5kΩ pullup	1.4			MHz

1. Open Head Detection is guaranteed up to a frequency of 17MHz and typically operates to 20MHz.
2. Open Head Detection is guaranteed up to a head resistance of 26Ω and typically operates to 35Ω.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 15Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		0.1	0.15	µs
Write to Read Mode	t_{WR}	To 90% of envelope and ±20mV of steady-state offset		1.4	2.0	µs
Idle to Read Mode	t_{CS}	To 90% of envelope and ±20mV of steady-state offset		13	20	µs
HS0-3 to Any Head	t_{HS}	To 90% of envelope and ±20mV of steady-state offset		3	5	µs
Read to Idle	t_{RI}	To 10% of read envelope or write current		0.1	0.5	µs
Safe to Unsafe*	t_{D1}	50% WDX to 50% FLT, < 5kΩ pullup		0.7	1.5	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 15Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Unsafe to Safe[1]	t_{D2}	50% WDX to 50% FLT, < 5kΩ pullup		0.1	0.3	µs
Head Current Propagation Delay*	t_{D3}	From 50% points		12	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0		0.05	0.1	ns
Rise/Fall Time	t_r / t_f	20-80%		1.8	2.5	ns
		10-90%		2.5	3.5	

1. See Figures 12 and 13 for write mode timing diagrams.

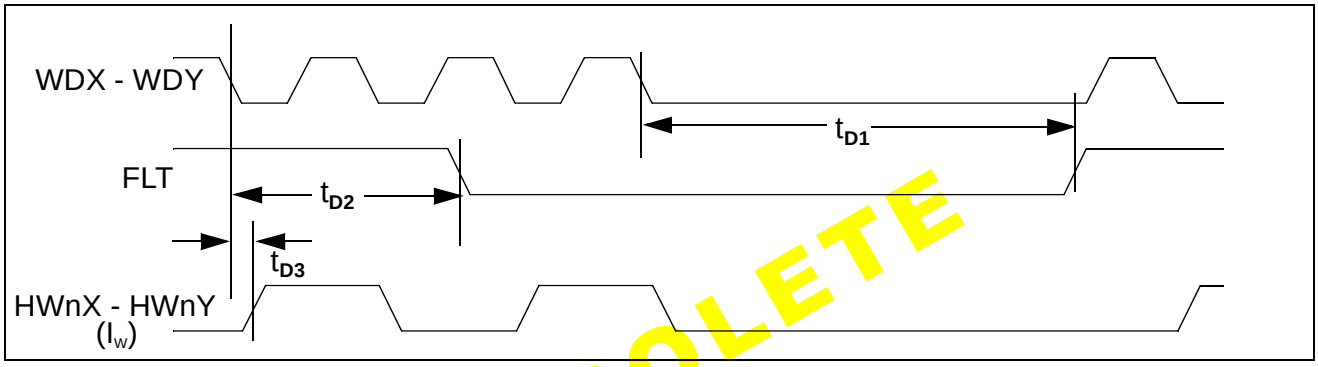


Figure 12 Write Mode Timing Diagram (with flip-flop active)

Note: The write current polarity is toggled on each high to low transition of the expression (WDX - WDY).
A preceding read operation initializes the WDFF so that upon entering the write mode, current flows into the “X” port.

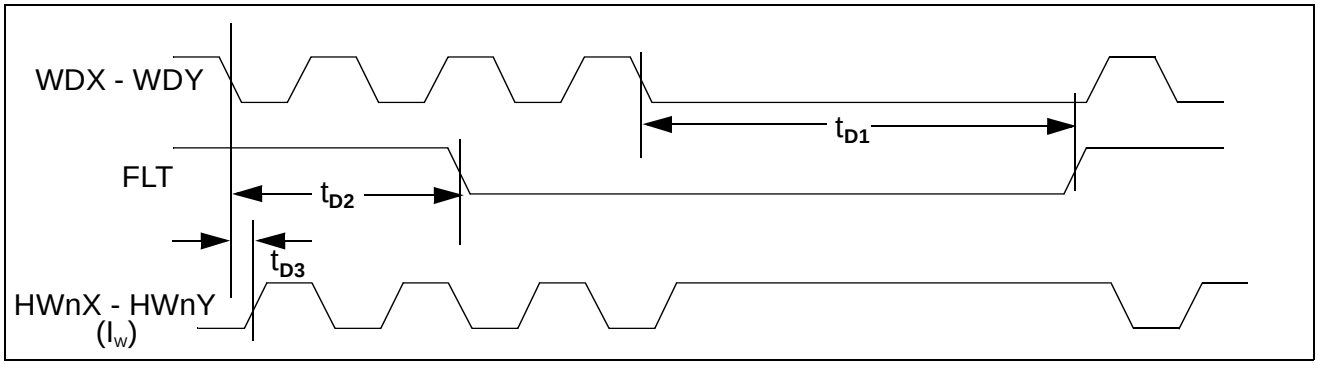
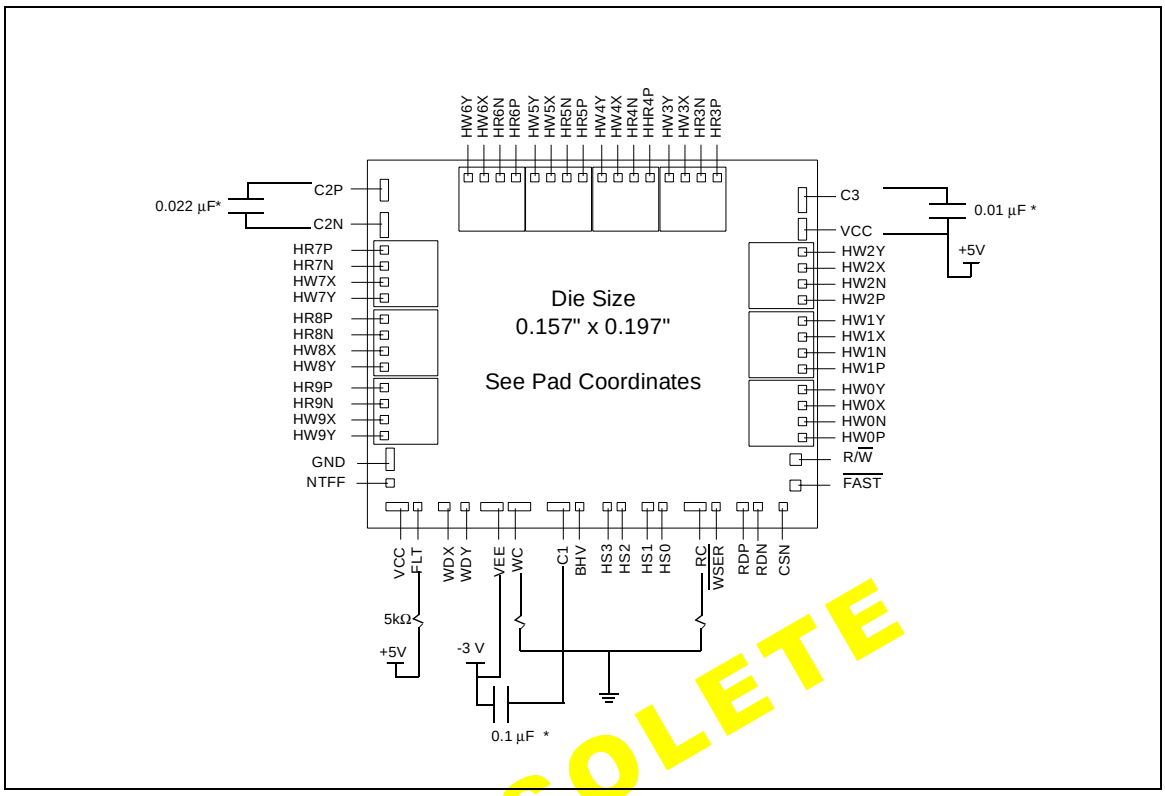


Figure 13 Write Mode Timing Diagram (without flip-flop)

Note: Without the flip-flop, the write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY).
For WDX>WDY current flows into the “X” port; for WDX<WDY current flows into the “Y” port.

TYPICAL APPLICATION CONNECTIONS



Application Notes

- V_{CC} = +5V, GND = Ground, V_{EE} = -3V
- Both VCC pads are electrically-connected on the die, but external connection is preferred for noise immunity.

* Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

V10615

10-CHANNEL DIE

Specific Characteristics

Die size: 192 X 191 Mils

Pad Coordinates for the V10615 (in Mils)

Pad Name	*X Axis*	*Y Axis*
BHV	- 140.0	-1727.75
C1	- 381.0	-1727.75
C2N	-2357.5	1341.75
C2P	-2357.5	1707.75
C3	2357.5	1607.75
$\overline{CS}$	2156.0	-1727.75
FAST	2288.5	-1511.75
FLT	-1972.5	-1727.75
GND	-2288.0	-1210.25
GND	-1143.5	-1727.75
HR0N	2357.5	- 839.25
HR0P	2357.5	-1019.25
HR1N	2357.5	- 74.25
HR1P	2357.5	- 254.25
HR2N	2357.5	690.75
HR2P	2357.5	510.75
HR3N	1237.0	1852.75
HR3P	1417.0	1852.75
HR4N	472.0	1852.75
HR4P	652.0	1852.75
HR5N	- 292.0	1852.75
HR5P	- 112.0	1852.75
HR6N	-1057.0	1852.75
HR6P	- 877.0	1852.75
HR7N	-2357.5	920.75
HR7P	-2357.5	1100.75
HR8N	-2357.5	155.75
HR8P	-2357.5	335.75
HR9N	-2357.5	- 609.25
HR9P	-2357.5	- 429.25
HS0	785.0	-1727.75
HS1	619.0	-1727.75
HS2	322.5	-1727.75
HS3	156.5	-1727.75
HW0X	2357.5	- 659.25
HW0Y	2357.5	- 479.25
HW1X	2357.5	105.75
HW1Y	2357.5	285.75

Pad Name	*X Axis*	*Y Axis*
HW2X	2357.5	870.75
HW2Y	2357.5	1050.75
HW3X	1057.0	1852.75
HW3Y	877.0	1852.75
HW4X	292.0	1852.75
HW4Y	112.0	1852.75
HW5X	- 472.0	1852.75
HW5Y	- 652.0	1852.75
HW6X	-1237.0	1852.75
HW6Y	-1417.0	1852.75
HW7X	-2357.5	740.75
HW7Y	-2357.5	560.75
HW8X	-2357.5	- 24.25
HW8Y	-2357.5	- 204.25
HW9X	-2357.5	- 789.25
HW9Y	-2357.5	- 969.25
NTFF	-2288.5	-1451.25
R/$\overline{W}$	2288.5	-1215.25
RC	1156.5	-1727.75
RDN	1860.0	-1727.75
RDP	1694.0	-1727.75
VCC	-2213.5	-1727.75
VCC	2357.5	1291.75
WC	- 827.0	-1727.75
WDX	-1617.0	-1727.75
WDY	-1437.0	-1727.75
$\overline{WSER}$	1397.5	-1727.75

VTC Inc.
Value The Customer™

VM5131

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/WRITE PREAMPLIFIER with SERVO WRITE

990811 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR/GMR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Operates from +8 and +5 Volt Power Supplies
  - 2.5/3.3V CMOS Compatible Logic Interface
  - Fault Detection Capability
  - Available in a 30 or 38-pin VSOP or TSSOP Packages
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 2 - 9.75 mA Range
  - Programmable Read Voltage Gain
    (112 V/V or 150 V/V typical, 150/190 V/V option available)
  - Thermal Asperity Detection and
    Fast Recovery Compensation
  - Analog and Digital Buffered Head Voltage (ABHV/DBHV) Measurement Modes
  - Input Noise = 0.6 nV/$\sqrt{\text{Hz}}$ Typical
    (R_{MR}=45Ω, I_{MR}=8mA)
  - High Bandwidth = 270 MHz Minimum
    (R_{MR}=45Ω, -3dB)
  - Power Supply Rejection Ratio = (60 dB (1 < f < 100 MHz))
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 60 mA Range
  - Rise Time = 0.8 ns Typical, I_W=40 mA
    (for Real Head Model having L_{TOT}=85 nH)
  - Multi-Channel Servo Write

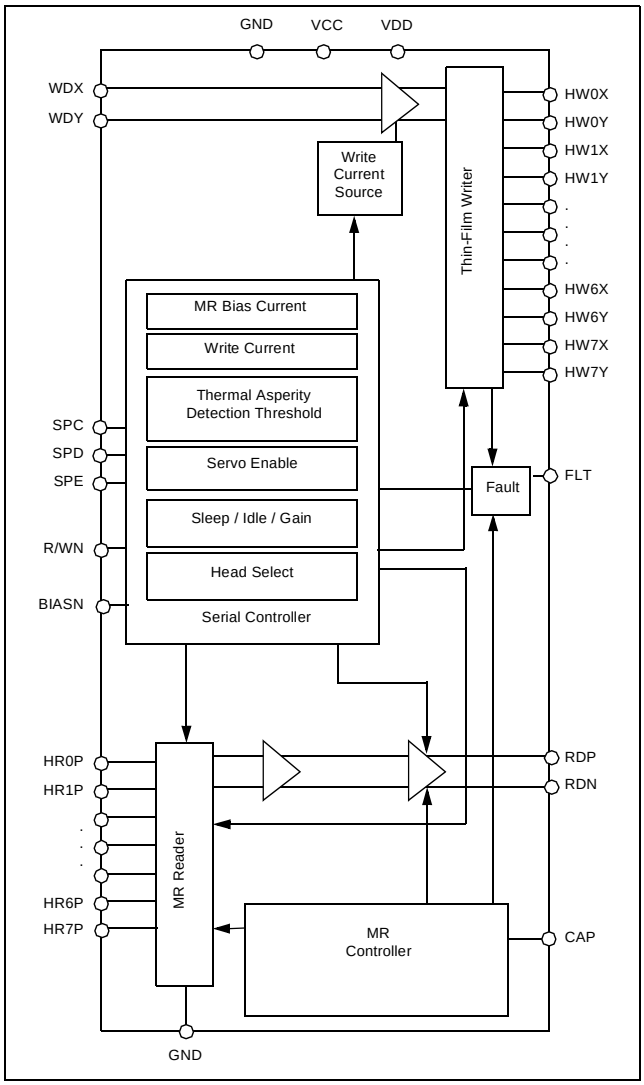
DESCRIPTION

The VM5131 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM5131 operates from +8V and +5V power supplies. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM5131 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available as a 4-channel part in a 30-pin TSSOP package or as a 6-channel part in a 38-pin TSSOP package. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V
- V_{DD} ..... -0.3V to +10V

Read Bias Current, I_{MR} 12mA
Write Current, I_W 65mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
- 30-lead VSOP ..... 101°C/W
- 38-lead VSOP ..... 88°C/W
- 48-lead TQFP ..... 75°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%
- V_{DD} .....+8V ± 10%

Write Current, I_W .....15 - 60 mA
Write Head Inductance, L_W ..... 60 - 160 nH
Write Head Resistance, R_W ..... 5 - 25 Ω
Read Bias Current, I_{MR} ..... 2 - 9.75 mA
Read Head Inductance, L_{MR} ..... 20 - 40 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω
MR Bias Loop Compensation, CAP ..... 22 nF
Junction Temperature, T_J ..... 0°C to 125°C

OPERATIONAL MODES

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element that correspond to magnetic field changes on the disk.

The VM5131 uses the current-bias/current-sensing MR architecture. The magnitude of the bias current ranges from 2 - 9.75 mA and is governed by the following equation:

$$I_{MR} = 2 + 0.25(k_{IMR}) \qquad \textit{(eq. 7)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
k_{IMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>.

A high level signal applied to the R/WN pin and a low level signal applied to the BIASN pin (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the read mode and activates the read fault detection circuitry (see Table 12).

Passing the magnetic media by the MR element causes MR resistance changes as a result of changes in the magnetic field. The change in resistance is sensed as a change in current within the preamp, and this current change is converted to a differential voltage that is amplified prior to being output to the RDX and RDY pins.

MR Bias Current Enable

Taking the BIASN pin low in read mode enables MR bias current to the selected head.

Taking the BIASN pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

The bias current is switched to a 20Ω dummy load during head selection. This allows the bias current to increase from a low bias to the targeted bias current.

Gain and Boost Bits

The GAIN bit (4:<D2>) selects high or low signal gain. The BOOST bit (4:<D4>) increases read gain by 3dB at 80Mhz.

$$A_V = \frac{k}{\frac{25}{I_{MR}} + R_{MR}} \qquad \textit{(eq. 8)}$$

Av represents the Differential Voltage Gain in V/V
Where k = 5390 for low gain or 7219 for high gain.
I_{MR} is in mA.

MR Head Switch Overvoltage Control

The preamp controls the bias current loop capacitor voltage during head switching or modal transitions, in order to prevent overvoltage of the MR element.

When switching between heads, changing I_{MR}, or in any mode where the bias current becomes disabled (Write or Idle modes, or BIASN pin set high in Read mode), the MR bias current is diverted from the MR head while the bias current loop capacitor voltage is quickly discharged to a V_{be} above ground. This ensures that the MR head voltage always rises from a safe voltage to the specific I_{MR}*R_{MR}.

Write Mode

In the write mode, the circuit operates as a thin-film write-current switch, driving the thin-film write element of the MR head.

The magnitude of the write current ranges from 15 - 59.95 mA. The following equation governs the write current magnitude:

$$I_W = 15 + 1.45(k_{IW}) \qquad \textit{(eq. 9)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 31) in 2:<D0-D4>.

A low level applied to R/WN pin (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the write mode (see Table 12). The write data signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 26.

MR Bias Current Enable

Taking the BIASN pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the BIASN pin high in write mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

Write Current Waveform Shaping Control

The write current waveform can be shaped using the control bits in register 5. The OSD bit (5:<D1>) selects an increase (OSD = 0) or decrease (OSD = 1) in the amplitude of the overshoot. The OSC bits (5:<D2-D4> select the percentage of overshoot. The USC bits (5:<D5-D7> select the percentage of undershoot.

Note: The overshoot or undershoot induced by the register settings is dependent on write load and current settings. See Tables 16 and 17, and Figures 17 through 20 for examples.

Servo Write Mode

In the servo write mode, the even, odd or all channels of the VM5131 are written simultaneously. The reader circuitry is shutdown during servo mode to reduce power consumption and the associated heat.

MR head fault detection and reporting are disabled during Servo Write Mode.

Servo mode is initiated by a seven-step process (see Table 12):

1) Select Head 0, 2, 3, 4 or 6 (‘none’ in Servo Bank Write).[1]
2) Select Read mode by setting R/WN pin high.
3) Set the SBW0 bit (4:<D5>) to a ’1’.
4) Set the SBW1 bit (2:<D7>) to a ’1’.
5) Set the SBW0 bit to a ’0’ to initiate Servo mode.
6) Select Heads 1, 5 or 7 (‘odd’, ‘all’ or ‘even’ in Servo Bank Write). [2]
7) Set R/WN pin high to enable servo write current. [3]

1. This step prevents an overvoltage spike to the MR heads when servo mode is entered.
2. The HS0-HS2 register bits (1:<D0-D2>) determine which heads are written (see Table 13).
3. R/WN pin enables or disables write current to the heads but does not affect the servo mode.

To exit Servo mode, set SBW1 to ’0’.

Note: The customer is responsible for ensuring that the thermal constraints of the package are not exceeded.
This may be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo write active duty cycle.
If V_{DD}<7.2V, the LVDIS bit (2:<D6>)must be set to ’1’ in order to continue to write or read.

MR Bias Voltage Enable

Taking the BIASN pin low in servo write mode applies a common voltage bias to all selected heads, see Table 13. The magnitude of this bias voltage ranges from 25 to 226.5 mV and is governed by the following equation:

$$V_{MR} = 25 + 6.5(k_{VMR}) \qquad \textit{(eq. 10)}$$

where V_{MR} represents bias voltage applied to the selected MR element (in mV)
k_{VMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>.

Taking the BIASN pin high in servo write mode disables MR head bias.

MR head fault detection and reporting are disabled during Servo Write mode.

Idle Mode

Setting the IDLEB bit low (4:<D1>) and SLPB bit high (4:<D0>) places the preamp in Idle mode (see Table 12). Only the serial register, bias circuitry and dummy head cell remain active.

The MR bias current source is active and the MR bias current is directed to an internal dummy head. The MR bias current control loop is active and the reader output is clamped at the common-mode voltage.

Sleep Mode

Setting the SLPB bit low (4:<D0>) places the preamp in Sleep mode (see Table 12). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Note: Transitions from Sleep mode to Read mode should always be made by first entering the Idle mode for a minimum of 300µs.

Note: After a transition from Sleep mode to Idle mode, the Fault Register (register 6) must be written. This initializes the register to a defined or cleared state.

Table 12 Mode Select

R/WN	*BIASN*	*Servo*	*IDLEB 4:<D1>*	*SLPB 4:<D0>*	*MODE*
1	1	0	1	1	Read Bias Disabled
1	0	0	1	1	Read Bias Enabled
0	1	0	1	1	Write Bias Disabled
0	0	0	1	1	Write Bias Enabled
X	1	1	1	1	Servo [1]
X	0	1	1	1	Servo [1] Bias Enabled
X	X	X	0	1	Idle Bias Disabled
X	X	X	X	0	Sleep

1. Servo Write Mode on page 29 describes the process for initiating.

Table 13 Head Select

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*Normal [1] Write/Read*	*Servo Bank Write*
0	0	0	0	none
0	0	1	1	odd
0	1	0	2	none
0	1	1	3	none
1	0	0	4	none
1	0	1	5	all
1	1	0	6	none
1	1	1	7	even

1. If *Head Selected* > *Channel Count - 1*, an Invalid Head Select fault will be reported.

ESD PROTECTION FOR MR HEAD

Characteristics for ESD diodes at MRP pins are:
R_{ON} = 2Ω, C = 0.3pF, t_{ON} = 0.6ps.

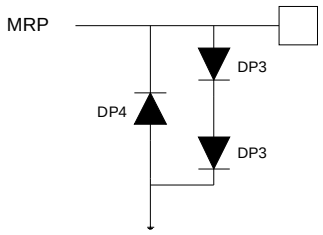


Figure 14 ESD Protection of MR Heads

FAULT HANDLING

Conditions triggering faults, and status and reporting during the fault are listed in Table 14. Non-fault conditions are indicated by a dash, the fault pin level for this condition is that of a safe condition (e.g., Open MR Head in Idle mode, FLT = H).

Table 14 Fault Table

		FLT pin level by Mode [1]					***Register:Bit [2]***
FAULT	***CONDITION***	***Read [3]***	***Write***	***Servo***	***Idle***	***Sleep***	***Setting***
None	Safe	H	L	L	H	H	—
Hot	TEMP bit = 1, Die temperature > 135°C	L	H	H	—	—	6:<D0> = 1
Low V_{CC}	V_{CC} < 3.8V; Resets when V_{CC} > 4.1V	L [4]	H [4,5]	H [5,6]	L	—	—
Low V_{DD}	LVDIS bit = 0, V_{DD} < 6.1V; Resets when V_{DD} > 6.4V	L [4]	H [4,5]	H [5]	L	—	6:<D1> = 1
	LVDIS bit = 1	H	L	L	—	—	6:<D1> = 0
Open MR Head	BIASN pin = L, VMR > 950 mV	L [7]	—	—	—	—	6:<D2> = 1
Shorted MR Head	BIASN pin = L, VMR < 50 mV	L [7]	—	—	—	—	6:<D3> = 1
Invalid Head Select	Head Selected > Channel Count - 1	L [4]	H [6]	—	—	—	—
Open/Shorted Write Head	(ΔV across write element > 2.5V at next WDX/WDY transition, where ΔV = $R_{OpenHead}$*I_W OR Head resistance to GND <15Ω) AND (WDX/WDY transition spacing > Open/Shorted Write Head Blanking Time)	—	H [8]	—	—	—	6:<D4> = 1 6:<D5> = 1
Low Write Frequency	1.5 µs typical between transitions	—	H	—	—	—	6:<D6> = 1
Thermal Asperity	BIASN pin = L, TA DAC > 0, (RDP-RDN) > TA Threshold	L	—	—	—	—	—

1. L = FLT pin low, H = FLT pin high impedance - pulled to level set by external pull-up resistor.
2. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to '0'.
3. Read faults are disabled if MRM is enabled (4:<D3> = 1).
4. MR bias current disabled to MR head. Bias loop capacitor maintained for optimal recovery and at a low voltage to prevent MR element overvoltage.
5. Write current is disabled until the fault is cleared.
6. V_{MR} is not disabled.
7. An open or shorted head fault is latched on the FLT line and the head voltage is clamped to a safe low voltage. The FLT latch and head voltage clamp are cleared by a change in head selection or I_{MR}, or a mode switch.
8. Two WDX/WDY transitions may be required to clear the FLT line after the fault has cleared.

Other Features Utilizing FLT Pin

Three bits (MRM, ABHV, TEMP) affect the FLT pin output. Table 15 defines the function of the output on the FLT pin.

Table 15 FLT Pin Output Functions

Setting	*Function*	*TEMP 4:<D7>*	*ABHV 4:<D6>*	*MRM 4:<D3>*
1	Normal Fault Reporting [1]	0	0	0
2	DBHV - MR Measurement Mode	0	0	1
3	ABHV - Analog Buffered Head Voltage	0	1	0
4	Not Valid	0	1	1
5	Hot Fault Reporting Enabled (in addition to Normal Fault Reporting)	1	0	0
6	Not Valid	1	0	1
7	Analog Temperature	1	1	0
8	Not Valid	1	1	1

1. As defined in Table 14.

MR Measurement / Digital Buffered Head Voltage (DBHV)

Setting the MRM bit high (4:<D3>) while the TEMP and ABHV bits are low allows the digital buffered head voltage (DBHV) to be represented on the FLT pin.

The FLT output is low when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to exceed the threshold level as determined by the TA/DBHV DAC (3:<D6-D0>). The FLT output is high when the $I_{MR} \cdot R_{MR}$ product falls below this level.

Note: The FLT line is not valid for 2µs after changing the TA/DBHV DAC.

$$DBHV = 6(k_{TA}) \qquad \textit{(eq. 11)}$$

DBHV represents the voltage level from the MR element (in mV).
k_{TA} represents the TA/DBHV DAC setting (7 to 127) in 3:<D0-D6>.
The threshold settings in TA/DBHV DAC (0 to 6) cannot be detected.

MR Measurement Mode Procedure

Set a fixed IMR bias current and decrease the TA/DBHV DAC settings until the FLT pin goes low. Example: IMR = 6mA, TA/DBHV DAC setting to cause FLT low = 330mV, then MR resistance = 55Ω (330/6).

Analog Buffered Head Voltage (ABHV)

Setting the ABHV bit high (4:<D6>) while the MRM and TEMP bits are low allows an amplified representation of the MR bias voltage to be multiplexed on the FLT pin. (The external pullup resistor must be removed for this mode.) The voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} \cdot R_{MR}) \qquad \textit{(eq. 12)}$$

Analog Temperature

Setting the ABHV and TEMP bits high while MRM is low multiplexes the voltage representation of the die temperature on the FLT pin. (Note: The external resistor must be removed for this mode of operation.) A voltage (1V to 3V) on the FLT pin represents the die temperature (0°C to 200°C) given by the equation:

$$TEMP(^{o}C) = (V - 1) \times 100 \qquad \textit{(eq. 13)}$$

Where V = voltage (1V to 3V) at FLT pin.

THERMAL ASPERITY DETECTION AND COMPENSATION

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. The thermal asperity may result in a positive or negative signal disturbance. Figure 15 displays the reader output for an uncompensated, positive thermal asperity event.

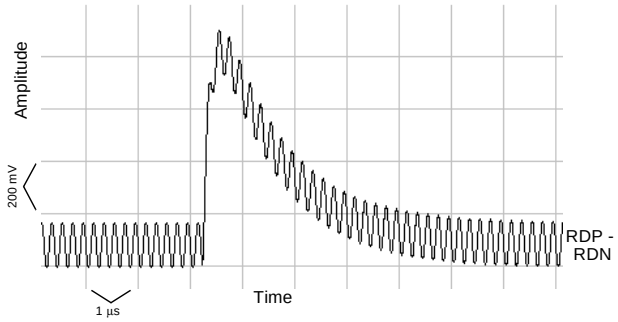


Figure 15 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM5131 implements both a programmable detection threshold and fast recovery compensation for positive, and positive or negative (dual direction) disturbances.

Detection

Programming a non-zero TA detection threshold value (3:<D6-D0>) allows the TA detection circuitry to detect a positive asperity event. Setting the Dual Direction TA bit (7:<D7> = 1) allows detection of positive and negative asperity events. The threshold for thermal asperity detection is output-referred, has a range of 6 - 762 mV and is governed by the following formula:

$$TA_{level} = 6(k_{TA}) \qquad \textit{(eq. 14)}$$

TA_{level} represents the voltage level from the MR element (in mV).
k_{TA} represents the TA DAC setting (1 to 127) in 3:<D0-D6>

TA detection is turned off when the TA detection threshold value is zero (3:<D6-D0> = 0).

Reporting

Whenever a thermal asperity event is detected, it is reported as a low ('0') on the FLT pin.

Compensation and Fast Recovery

When the TAC bit is enabled (3:<D7> = 1), thermal asperity compensation mode is initiated if a thermal asperity is detected.

Note: Setting the TAC bit off (3:<D7> = 0) makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the low corner frequency movement.

When activated, Fast Recovery and Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 10 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 16). Additional TA events during t_{D5} will not be compensated.

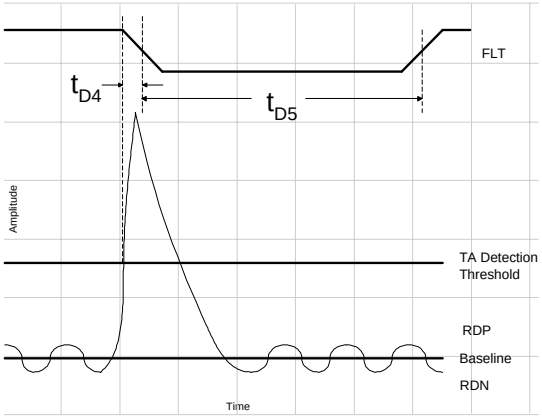


Figure 16 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

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WRITE CURRENT WAVEFORM SHAPING

Tables 16 and 17 summarize write current simulations at both 40 and 60 mA with the load as shown in Figure 17 . The family of curves in Figures 18 through 20 depict the response of programmable overshoot and undershoot under nominal conditions (nominal process, V_{DD} = 8V, V_{CC} = 5V, and T = 75^{o}C). For the calculations of over/undershoot, I_W is the write current amplitude from base (0mA) to the settled point (write current setting in mA). The write current is the current in R2 in the head model depicted in Figure 17.

Table 16 Write Current Overshoot Control

OSD 5:D1	OSC2 5:D4	OSC1 5:D3	OSC0 5:D2	Iw = 40 mA		Iw = 60 mA	
				Overshoot % [1]	% Change from '000' [2]	Overshoot % [1]	% Change from '000' [2]
0	0	0	0	90	0	53	0
0	0	0	1	95	5	57	3
0	0	1	0	103	13	62	8
0	0	1	1	110	20	67	13
0	1	0	0	118	28	70	17
0	1	0	1	128	38	73	20
0	1	1	0	133	43	75	22
0	1	1	1	138	48	77	23
1	0	0	0	90	0	53	0
1	0	0	1	73	-18	45	-8
1	0	1	0	60	-30	40	-13
1	0	1	1	55	-35	37	-17
1	1	0	0	48	-43	30	-23
1	1	0	1	40	-50	25	-28
1	1	1	0	35	-55	20	-33
1	1	1	1	33	-58	17	-37

1. Overshoot % = (Overshoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

Table 17 Write Current Undershoot Control

USC2 5:D7	USC1 5:D6	USC0 5:D5	Iw = 40 mA		Iw = 60 mA	
			Undershoot % [1]	% Change from '000' [2]	Undershoot % [1]	% Change from '000' [2]
0	0	0	-23	0	-18	0
0	0	1	-15	8	-10	8
0	1	0	-10	13	-8	10
0	1	1	-5	18	-7	12
1	0	0	0	23	-5	13
1	0	1	5	28	-3	15
1	1	0	8	30	-2	17
1	1	1	10	33	0	18

1. Undershoot % = (Undershoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

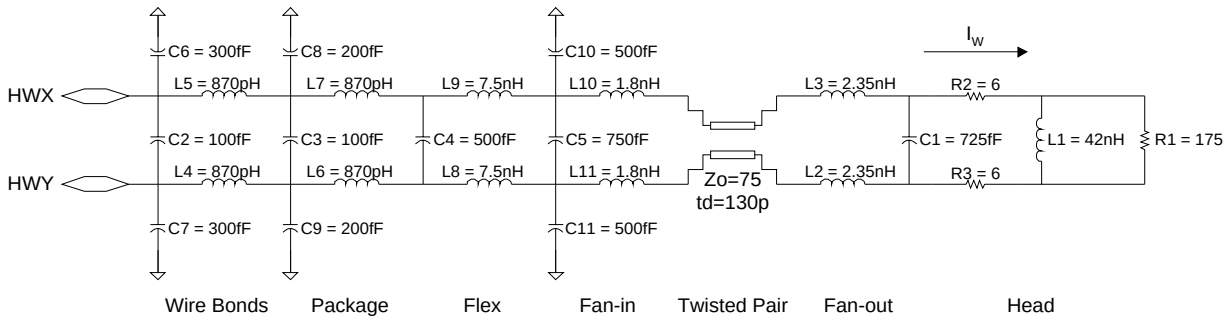


Figure 17 Writer Head Model

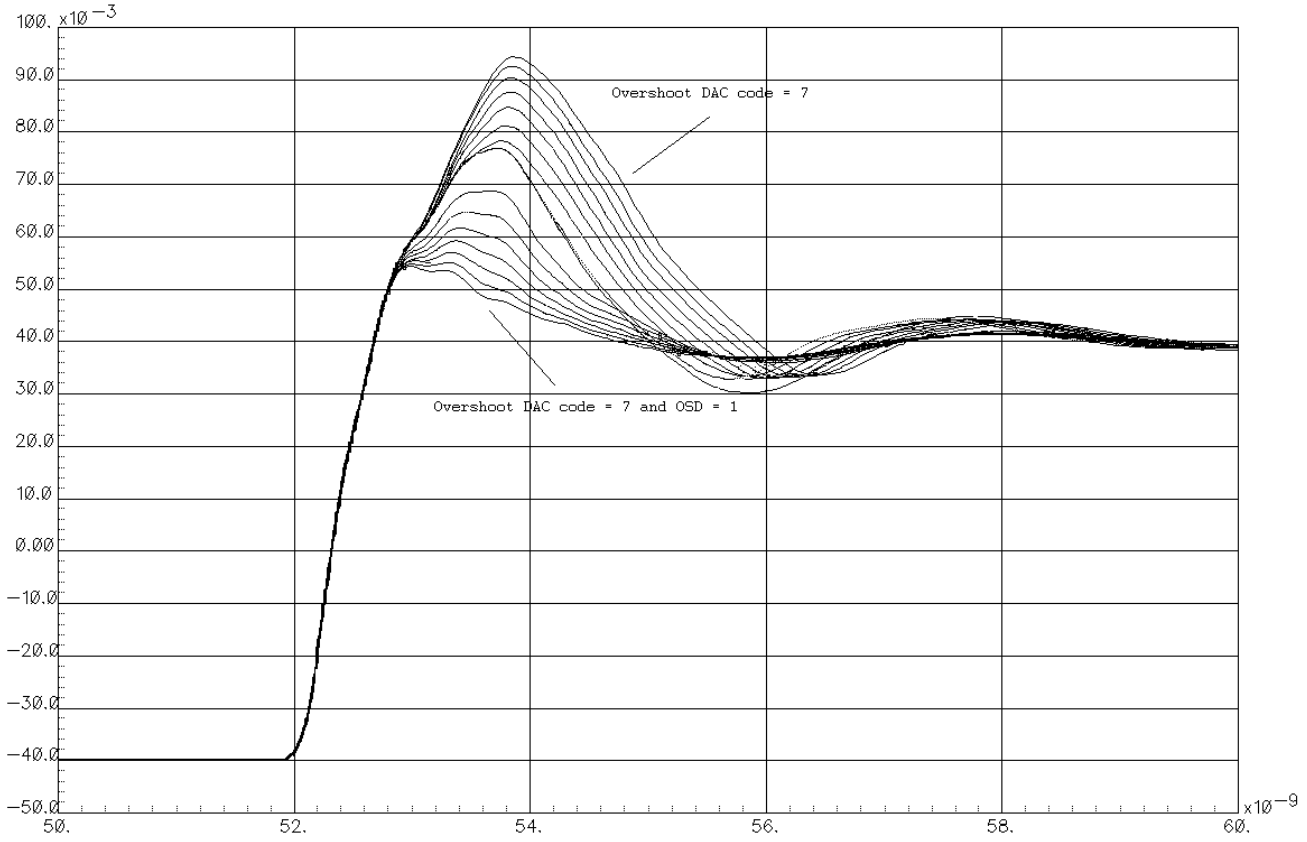


Figure 18 Simulation Of The Programmable Overshoot at Iw=40mA Under Nominal Conditions (nom process, +8,+5V power, 75^{O}C)

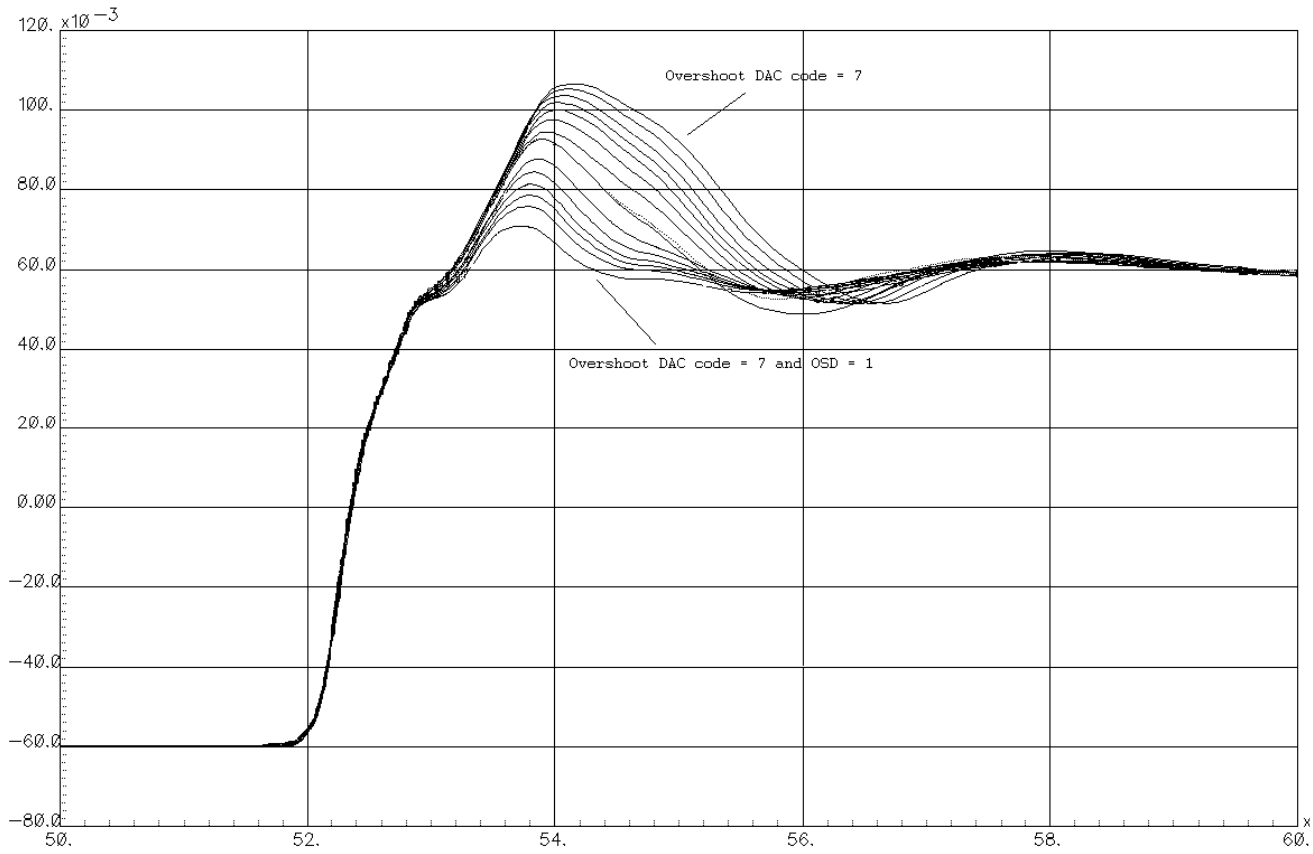


Figure 19 Simulation Of The Programmable Overshoot at Iw=60mA Under Nominal Conditions (nom process, +8,+5V power, 75^{O}C)

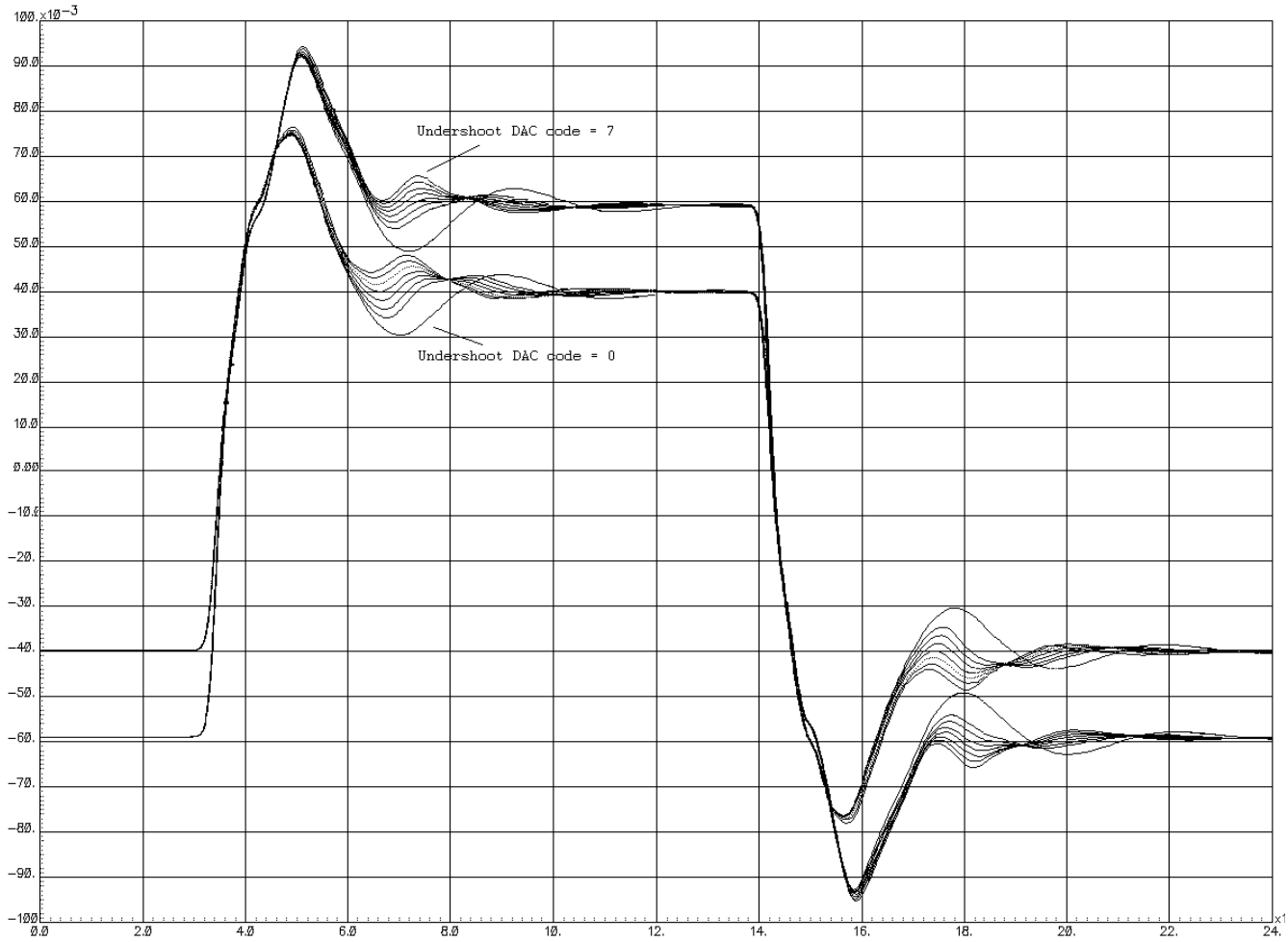


Figure 20 Simulation Of The Programmable Undershoot at Iw=40 and 60mA Under Nominal Conditions (nom process, +8,+5V power, 75°C)

PINNED LAYER REVERSAL MODE

Pinned Layer Reversal (PLR) mode provides a means to correct GMR heads that are affected by a reversed pinned layer. When the preamp is placed in the PLR mode, a positive reset pulse can be applied to the selected head. The external BIASN pin is used to control the timing of the delivery of the reset pulse to the GMR element. Several control bits are provided to shape the reset pulse. These controls include pulse amplitude, duration and decay rate. (See PINNED LAYER REVERSAL CHARACTERISTICS on page 52 for specifications.)

PLR Reset Pulse Controls

The amplitude of the reset pulse ranges from 0.4 to 1.64 V and is governed by the following equation:

$$V_{RESET} = 0.4 + 0.04(k_{PLR}) \qquad \textit{(eq. 15)}$$

where V_{RESET} represents the reset pulse voltage amplitude
k_{PLR} represents the IW DAC setting (0 to 31) in 2:<D0-D4>.
Note that the MR heads ESD diodes may limit the maximum V_{RESET} amplitude achieved to around 1.4V.

The reset pulse duration and decay time are determined by the settings of the PLRPW bits (7:<D2-D3>) as shown in Table 18 and the PLRDT bits (7:<D0-D1>) as shown in Table 19.

Table 18 PLR Reset Pulse Width

PLRPW1 7:<D2>	*PLRPW0 7:<D3>*	*PLR Pulse Width (ns)*
0	0	50
0	1	100
1	0	150
1	1	200

Table 19 PLR Reset Pulse Decay Rate

PLRDT1 7:<D0>	*PLRDT0 7:<D1>*	*PLR Decay Rate (mV/ns)*
0	0	7
0	1	4.67
1	0	2.33
1	1	1.75

PLR Timing and Event Description

Figure 21 depicts a timing diagram for the PLR mode. The steps involved are:

1) Set up VRESET via IW DAC, IMR, PLRPW and PLRDT, and select the head to be reset while in Idle or Read mode.
2) Enter the Read mode by setting IDLEB bit to '1'. Bring BIASN high to disable MR head bias.
3) Enter PLR mode by setting PLREN bit 7:<D4> to '1'.
4) After a minimum time t_{ARM}, bring BIASN low to trigger the pulse.

   Note: The PLR trigger depends on the sequence PLREN set to '1' followed by a high to low transition of the BIASN pin. Subsequent high to low transitions of BIASN will *not* retrigger the PLR mode.

5) Exit the PLR mode after a minimum time t_{EN}, by setting PLREN bit to '0'.
The device returns to Read mode, in which the state of the BIASN pin controls MR head bias.

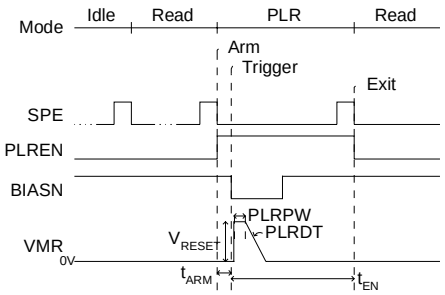


Figure 21 PLR Timing Diagram

VM5131 SERIAL PORT INTERFACE AND CONTROL REGISTERS

The serial port interface and the associated control registers provide programming and monitoring of the VM5131 circuitry. The interface handles the communication between a system control chip and the VM5131 via a three wire interface and related protocols. The control registers hold programming data written to the VM5131 and provide readback monitoring of data held or generated within the VM5131.

Note: If serial port activity is performed during Read mode, crosstalk to the reader output may result.

Serial Port Interface

The serial port interface provides for both writing data to and reading data from the VM5131. Its three pins are:

- SPC (Serial Port Clock) synchronizes the transfer.
- SPD (Serial Port Data) is the bi-directional data pin.
- SPE (Serial Port Enable) enables and disables a serial transfer.

All data writes or reads are enabled by setting SPE = 1 after which the SPC clocks data in or out via the SPD.

Writing to the Serial Port

A data transfer is initiated by setting SPE = '1'. A write data packet is structured as a 16-bit word: '0' for writing + 3 page address bits + 4 byte address bits + 8 programming data bits.

Each rising edge of SPC clocks data into the serial port interface. For valid data transfers, data are loaded into a designated register location upon the falling edge of SPE. Only the first 16 SPC rising edges after SPE goes high are recognized by the serial port interface. Any SPC rising edges after the first 16 are ignored. If less than 16 clock pulses are provided before SPE goes low, the data transfer is aborted.

Figure 22 shows the protocol for a write transfer operation. Refer to Table 20 and Figure 24 for timing specifications for the serial port interface.

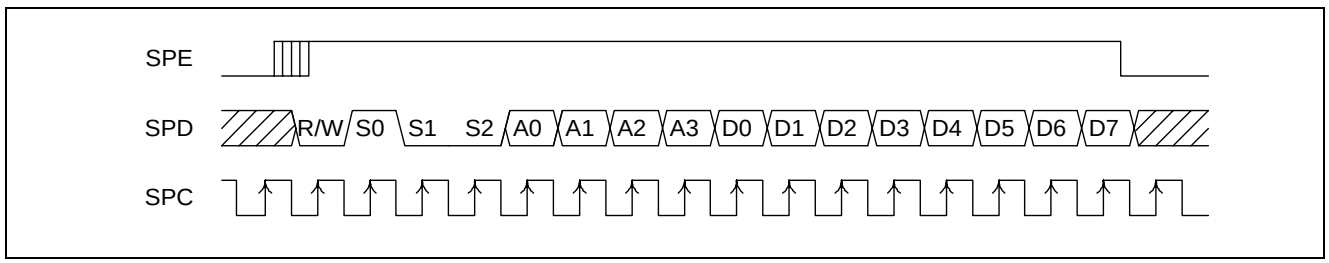


Figure 22 Write Protocol for 3-Write Serial Port Interface

Readback from the Serial Port

The read data packet is structured as: '1' for reading + 3 page address bits + 4 byte address bits + 8 data bits. To perform a read instruction, first set SPE =1 and then input the read instruction bit '1', the 3-bit page address, and the 4-bit byte address. The 8-bits at the specified register address are subsequently clocked out at the SPD pin.

Each rising edge of SPC clocks the instruction bit and the address bits into the serial port interface and the rising SPC edge also clocks out the data information. The SPE falling edge returns the SPD pin to an input pin state. The serial port interface drives the SPD pin only if the page address matches that of the VM5131.

Figure 23 shows the protocol for a read transfer operation. Refer to Table 20 and Figure 24 for timing specifications for the serial port interface.

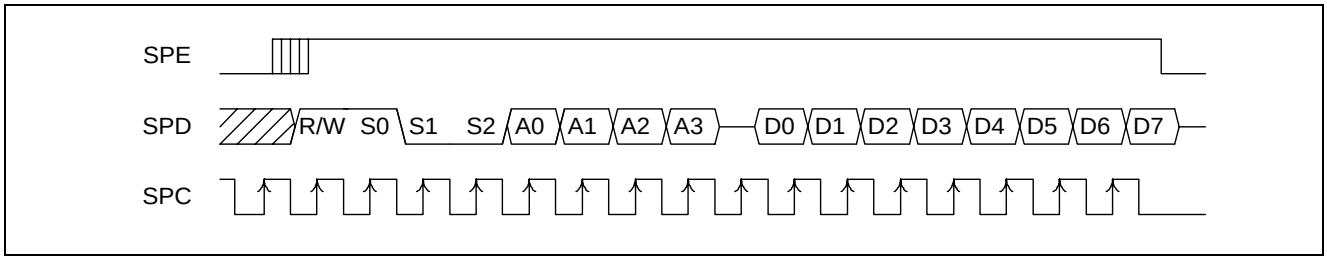


Figure 23 Read Protocol for 3-Wire Serial Port Interface

Table 20 Serial Port Interface Timing Specifications

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SPC Frequency	f_{SPC}	Write operation			25	MHz
		Readback operation			12.5	MHz
SPC High Time	t_{SPCH}	Write operation	14			ns
		Readback operation	32			ns
SPC Low Time	t_{SPCL}	Write operation	14			ns
		Readback operation	32			ns
SPE Rise Setup Time	t_{SEr}	Relative to SPC rising edge	10			ns
SPE Rise Hold Time	t_{HEr}	Relative to SPC rising edge	10			ns
SPE Fall Hold Time	t_{HEf}	Relative to SPC rising edge	10			ns
SPD Setup Time	t_{SD}	Data input relative to SPC rising edge	10			ns
SPD Hold Time	t_{HD}	Data input relative to SPC rising edge	10			ns
SPD Prop Delay	t_{PDD}	Data output relative to SPC rising edge			16	ns
SPD Enable Time	t_{PZD}	Time to take control of SPD relative to SPC rising edge			16	ns
SPD Disable Time	t_{PDZ}	Time to release control of SPD relative to SPE falling edge			16	ns
SPE Low Time	t_{SPEL}	Between transmissions	1/ f_{SPC}			ns

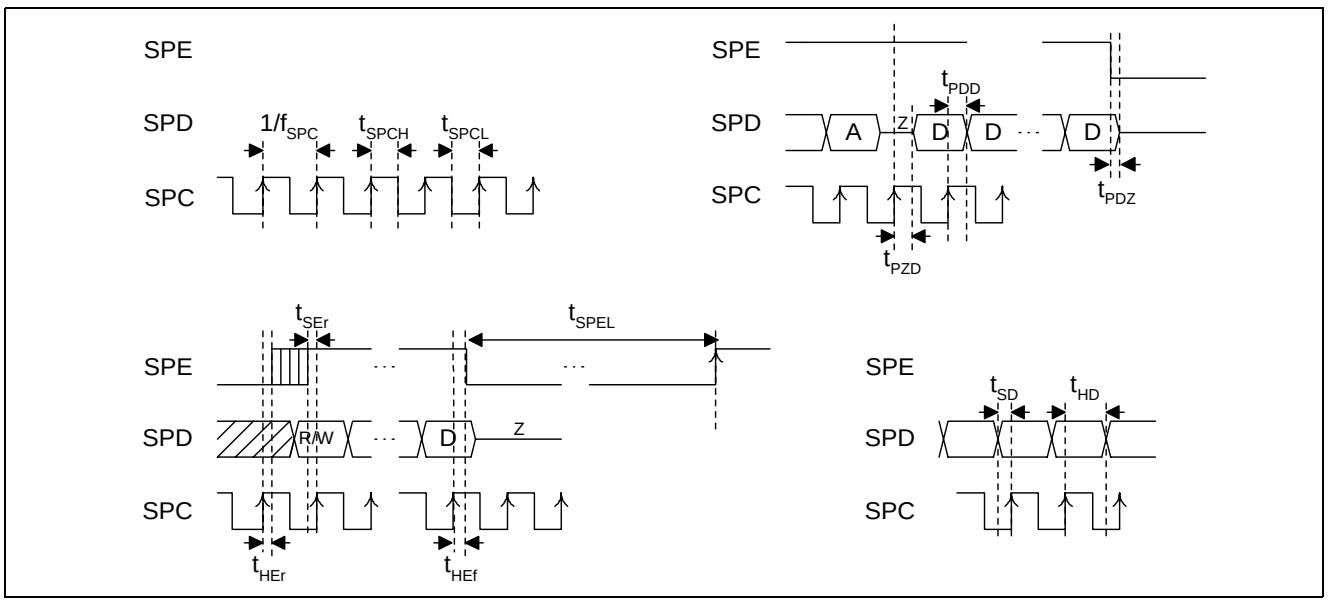


Figure 24 Timing Diagrams for 3-Wire Serial Port Interface

Control Registers

Control registers provide for storage and readback of programming data (i.e., an SRAM type function) and for monitoring of information generated (i.e., SRLatch type function) or hard-coded within the VM5131 (i.e., a ROM type function). The control registers are organized in byte-wide segments, each byte being either an SRAM-type, a ROM-type, or a SRLatch-type.

The addressing scheme for an entire system is as follows. There are 7 bits of address in a system. The first 3 bits, S0-S2, determine the page address, while the last 4 bits, A0-A4, determine a particular byte address within a page. A system may have a total of 8 pages with a total of 16 bytes per page. Each chip in the system is assigned one or more full pages (the VM5131 has a single page). All 16 bytes within each assigned page need not be used. Unused bytes within a chip's page are reserved for possible future use within the assigned chip; they may not be reassigned within the system.

Data written to an unused byte or page address is ignored. Reading from an unused byte in a valid page results in a logic '1' on the SPD line. However, reading from an invalid page address results in no data being transmitted, as the SPD output driver remains turned off until a valid page is addressed. When data is to be read from a valid page address all other chips must keep their SPD output drivers turned off and allow the chip assigned that page address sole control of the SPD line.

VM5131 control registers extend across one page address. The page address is S<0:2> = 1 (001_b) and it contains byte addresses 0 (0000_b) to 15 (1111_b), but not all 16 bytes are used. Table 21 depicts register bit assignments and Table 22 explains the defined register bits. All SRAM and SRLatch registers are set to logic '0' at power-up. Register 0, a ROM type, is hard-coded as follows: the channel count indicator bits (CCI0 to CCI1) are set so that 01_b = 4 channels and 00_b = 6 channels, the revision level bits (REV0 to REV2) are programmed to the appropriate design revision level (0 = 000_b and 7 = $111_{b)}$ and the vendor bits (VEN0 to VEN2) are set to 2 (010_b).

Table 21 Control Register Map

Register			***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0*** [1]
Address	***Title***	***Type***								
0	ID/Rev	ROM	CCI1	CCI0	REV2	REV1	REV0	VEN2	VEN1	VEN0
1	HS/IMR	SRAM	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
2	IW/Servo	SRAM	SBW1	LVDIS	[2]	IW4	IW3	IW2	IW1	IW0
3	TA	SRAM	TAC	TA6	TA5	TA4	TA3	TA2	TA1	TA0
4	Mode	SRAM	TEMP	ABHV	SBW0	BOOST	MRM	GAIN	IDLEB	SLPB
5	WCC	SRAM	USC2	USC1	USC0	OSC2	OSC1	OSC0	OSD	[2]
6	Faults [3]	SRLatch	[2]	LOFR	WRSH	WROP	MRSH	MROP	LOVDD	HOT
7	PLR	SRAM	DUALTA	TOSC	OSDLY	PLREN	PLRPW0	PLRPW1	PLRDT0	PLRDT1

1. <D0> is the first bit written to or read from the register. i.e., LSB first.
2. Reserved
3. See Table 14 for definition of the faults.

Table 22 Control Register Bit Definitions

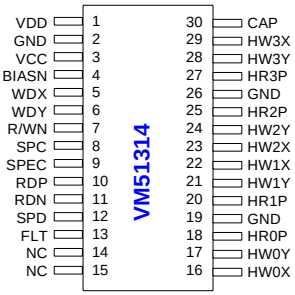
Register/ Bits	*Bit Name*	*Functional Description*
0:<D0-D2>	VEN<0:2>	Vendor ID of device (read only).
0:<D3-D5>	REV<0:2>	Revision level of device (read only).
0:<D6-D7>	CCI<0:1>	Channel Count Indicator (read only); set to 01_b = 4 channels or 00_b = 6 channels.
1:<D0-D2>	HS<0:2>	Head Select setting. See Table 13 on page 29 for further definition.
1:<D3-D7>	IMR<0:4>	MR head bias current DAC setting (0-31). See Read Mode on page 28 for further definition. In servo write mode, setting determines MR bias voltage as defined in (eq. 10) on page 29.
2:<D0-D4>	IW<0:4>	Write current DAC setting (0-31). See Write Mode on page 28 for further definition. In PLR mode, setting determines PLR amplitude as defined in (eq. 15) on page 37.
2:<D6>	LVDIS	Low V_{DD} disable fault reporting; set to 1 to disable reporting.
4:<D5> 2:<D7>	SBW0 SBW1	Servo Bank Write enable; follow sequence in Servo Write Mode on page 29.
3:<D0-D6>	TA<0:7>	Thermal Asperity Detection DAC setting (1-127) or Digital Buffered Head Voltage DAC setting (7-127). See Detection on page 32 or MR Measurement / Digital Buffered Head Voltage (DBHV) on page 31 for further definition.
3:<D7>	TAC	Thermal Asperity Compensation enable; set to 1 to select.
4:<D0>	SLPB	Sleep mode enable; set to 0 to select.
4:<D1>	IDLEB	Idle mode enable; set to 0 to select.
4:<D2>	GAIN	Gain selection: set to 0 for low gain, set to 1 for high gain.
4:<D3>	MRM	Head Resistance Measurement (DBHV) mode enable; set to 1 to select. See Table 15.
4:<D4>	BOOST	Boost circuit enable; set to 1 to select.
4:<D6>	ABHV	Analog Buffered Head Voltage enable; set to 1 to output ABHV at FLT pin. See Table 15.
4:<D7>	TEMP	Temperature fault report enable; set to 1 to report a temperature fault to the HOT bit and the FLT pin. See Table 15.
5:<D1>	OSD	Write current overshoot direction of control; set to 0 to increase, set to 1 to decrease
5:<D2-D4>	OSC<0:3>	Write current overshoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 33 for further definition.
5:<D5-D7>	USC<0:3>	Write current undershoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 33 for further definition.
6:<D0>	HOT	Bit is set to 1 if the HOT fault occurs. [1]
6:<D1>	LOVDD	Bit is set to 1 if the Low V_{DD} fault occurs. [1]
6:<D2>	MROP	Bit is set to 1 if an MR Open head fault occurs. [1]
6:<D3>	MRSH	Bit is set to 1 if an MR Shorted head fault occurs. [1]
6:<D4> 6:<D5>	WROP WRSH	Bits are set to 1 if a Writer Open head or Head Shorted to ground fault occurs. [1]
6:<D6>	LOFR	Bit is set to 1 if the Write data frequency too low fault occurs. [1]
7:<D0-D1>	PLRDT	PLR Delay Time. See Table 19.
7:<D2-D3>	PLRPW	PLR Pulse Width. See Table 18.

Table 22 Control Register Bit Definitions

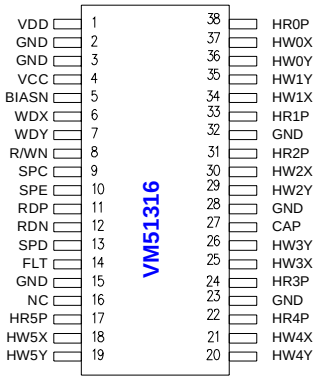
7:<D4>	PLREN	PLR Enable, set to 1 enable PLR mode.
7:<D5>	OSDLY	Additional Write Current Overshoot Control, set to 1 to select.
7:<D6>	TOSC	Manufacturer Test Bit; set to 0 for normal operation.
7:<D7>	DUALTA	Dual Direction TA Detection (positive *and* negative), set to 1 to select.

1. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to '0'.

PIN DESCRIPTION AND FUNCTION LIST



4-Channel
30-lead VSOP (TSSOP)



6-CHANNEL
38VSOP (TSSOP)

Figure 25 Pin Layouts

Table 23 Pin Functions

Signal	*I/O* [1]	*Description*
R/WN	I	Read/WriteNot: Low voltage CMOS input. Internal pull-up resistor (50kΩ). • A low level enables Write mode. • Pin defaults high (Read mode).
BIASN	I	Bias Enable and PLR trigger: Low voltage CMOS input. Internal pull-up resistor (20kΩ) to V_{CC}. • A high level directs bias current to a dummy head. Pin defaults high. • A low level enables MR bias current to the selected head. If PLREN = 1 (7:<D4>), a high to low transition triggers the PLR pulse (V_{MR}). See the PLR Timing and Event Description on page 37.
FLT	O	Fault Status: Open drain output. Requires external pull-up resistor (e.g., 2kΩ to 3V). • In Write mode, a high level indicates a fault. • In Read mode, a low level indicates a fault. • Measurements modes are shown in Table 15 on page 31.
WDX, WDY	I	2V ±100mV write data inputs.
HR0P-HR7P	I	MR head connections, positive end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end.
RDP, RDN	O	Read Data: Differential read signal outputs.
CAP	-	Compensation capacitor (22nF) for the MR bias current loop.
GND	-	Ground and common return for MR heads
VCC	-	+5.0V supply
VDD	-	+8.0V supply
SPE	I	Serial Enable: Low voltage CMOS input; see Figures 24 and 26.

Table 23 Pin Functions

Signal	*I/O* [1]	*Description*
SPC	I	Serial Clock: Low voltage CMOS input; see Figures 24 and 26.
SPD	I/O	Serial Data: Low voltage CMOS input/output; see Figures 24 and 26. Requires external pull-up resistor (e.g., 1kΩ to 3V).

1. I = Input pin, O = Output pin.

POWER CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR}=8 mA, I_W=40.0 mA, I_S=25mA.
Power supply currents for other settings can be calculated using the formulas below.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		7.2	8	8.8	V
V_{DD} Power Supply Current	I_{DD}	Read Mode (See Formula 1 below.)		27	31	mA
		Read Mode, Bias disabled		16	20	
		Write Mode (See Formula 2 below.)		72	82	
		Write Mode, Bias enabled (See Formula 3 below.)		83	93	
		Idle Mode		13	16	
		Sleep Mode		0.15	0.18	
		Servo Write Mode, All heads, VDD=5V, I_S=25mA (See Formula 4 below.)		224	250	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
V_{CC} Power Supply Current	I_{CC}	Read Mode (See Formula 5 below.)		47	56	mA
		Read Mode, Bias disabled		29	35	
		Write Mode (See Formula 6 below.)		41	50	
		Write Mode, Bias enabled (See Formula 7 below.)		48	56	
		Idle Mode (See Formula 8 below.)		18	21	
		Sleep Mode		0.34	0.40	
		Servo Write Mode, All heads, VDD=5V, I_S=25mA (See Formula 9 below.)		53	61	
Power Dissipation	P_d	Read Mode		449	577	mW
		Read Mode, Bias disabled		273	368	
		Write Mode		781	992	
		Write Mode, Bias enabled		900	1127	
		Idle Mode		194	255	
		Sleep Mode		3	4	
		Servo Write Mode, All heads, VDD=5V, I_{WS}=25mA		1387	1712	

1. IDD(Typ): 17.2 + (0.043 * I_W) + I_{MR} — IDD(Max): 20.6 + (0.046 * I_W) + (1.05 * I_{MR})
2. IDD(Typ): — IDD(Max):
3. IDD(Typ): 31.7 + (1.07 * I_W) + I_{MR} — IDD(Max): 38.0 + (1.16 * I_W) + (1.05 * I_{MR})
4. IDD(Typ): 7.77 + (10.1 * Hds) + (1.04 * I_S * Hds) — IDD(Max): 9.32 + (12.1 * Hds) + (1.12 * I_S * Hds)
5. ICC(Typ): 42.1 + (0.083 * I_W) + (0.17 * I_{MR}) — ICC(Max): 50.5 + (0.09 * I_W) + (0.18 * I_{MR})
6. ICC(Typ): — ICC(Max):
7. ICC(Typ): 39.4 + (0.18 * I_W) + (0.17 * I_{MR}) — ICC(Max): 47.3 + (0.19 * I_W) + (0.18 * I_{MR})
8. ICC(Typ): 16.5 + (0.17 * I_{MR}) — ICC(Max): 19.8 + (0.18 * I_{MR})
9. ICC(Typ): 21.9 + (1.95 * Hds) + (0.13 * I_S * Hds) — ICC(Max): 26.3 + (2.34 * Hds) + (0.14 * I_S * Hds)

I/O CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	1.5		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	-0.3		0.7	V
Input High Current	I_{IH}	Applies to SPE, SPC, SPD pins	-1		1	µA
Input Low Current	I_{IL}	Applies to SPE, SPC, SPD pins	-1		1	µA
BIASN Internal Pullup Resistor	R_{pu}	Pullup to V_{CC}	10	20	30	KΩ
R/WN Pin Internal Pullup Resistor	R_{pu}	Pullup to V_{CC}	30	50	70	KΩ
Input Signal Rise/Fall Time	t_{ir}/t_{if}	Applies to R/WN, BIASN, SPE, SPC, SPD pins			10	ns
Input Hysteresis	V_{ihys}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	200			mV
Output High Current	I_{OH}	V_{OH}=3.6V, applies to FLT, SPD			1	µA
Output Low Voltage	V_{OL}	FLT I_{OL}=3mA			0.3	V
		SPD I_{OL}=5mA			0.3	
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400		**TBD**	mV_{ppd}
WDX/WDY Differential Input Voltage	V_{DIFF}	Read Mode	100			mV_{diff}
		Idle Mode	0			mV_{diff}
WDX/WDY Common Mode Source Voltage	V_{CMW}		1.4	2	2.6	V
WDX/WDY Differential Input Impedance	Z_{ID}		100	125	150	Ω
WDX/WDY Input Rise/Fall Time	t_{WR}/t_{WF}	80% of V_{DIFF} into C_L=20pF		0.9	1.05	ns
RDP/RDN Differential Load Resistance	R_{LOAD}	220 Ω resistor (1%) load precedes 100pF coupling capacitors.	218	220	222	Ω
RDP/RDN Common Mode Output Voltage	V_{OCM}	Read Mode, Write Mode, BIASN = L		V_{CC} - 2.5		V
RDP/RDN Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE), BIASN = L	-150		150	mV
RDP/RDN Single-Ended Output Resistance	R_{SEO}	Read Mode		30	**TBD**	Ω
RDP/RDN Output Current	I_O	Source or sink	4			mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		2	7	9.75	mA
MR Head Current Accuracy	ΔI_{MR}	2mA < I_{MR} < 9.75mA	-5		5	%
Unselected MR Head Current		Applicable **TBD** µs after head switch			10	µA
Differential Voltage Gain	A_V	V_{IN}=1mV_{pp} @80MHz, R_L(RDP, RDN)=2kΩ, applies to the following:				V/V
		4 or 6-channel VM5131B1, Gain bit=0	95	112	130	
		4 or 6-channel VM5131B1, Gain bit=1	125	150	175	
		4 or 6-channel VM5131B2, Gain bit=0	125	150	175	
		4 or 6-channel VM5131B2, Gain bit=1	160	190	220	
Gain Deviation Head-to-Head					3	%
Gain Boost	BOOST	f=80MHz, Gain bit=0, Boost bit=1		3		dB
Passband Upper Frequency Limit	f_{HR}	L_{MR}=20nH, -3dB, Gain bit=0	270	300		MHz
		-1dB, Gain bit=0	170			
Passband Lower -3dB Frequency Limit	f_{LR}	Gain bit=0	0.15	0.5	0.8	MHz
Equivalent Input Noise (sense amp only)	e_a	1 < f < 85 MHz		**TBD**		nV/√Hz
Bias Current Noise (referred to Input)	i_n			**TBD**		pA/√Hz
Equivalent Input Noise (total)	e_n	1 < f < 85 MHz		0.6	**TBD**	nV/√Hz
Integrated Noise	e_{in}	L_{MR}=20nH; 1 < f < 140 MHz		**TBD**		µV
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN}=1mV_{pp} @ f=40 MHz, Gain bit=0	10			mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{DD}, 1 < f < 100 MHz	**TBD**			dB
		100 < f < 170 MHz	**TBD**			
Channel Separation	CS	Unselected Channels: V_{IN}=100mV_{pp}, 15 < f < 40 MHz	**TBD**			dB
		40 < f < 170 MHz	**TBD**			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Noise Rejection Any I/O to RDP/RDN	NR	100 mV_{PP} on I/O, 1 < f < 225 MHz	50			dB
Output Offset Voltage	V_{OS}	Low or High Gain	-50		50	mV
Output Offset Voltage Deviation Across Heads	ΔV_{OS}				50	mV
Total Harmonic Distortion	THD	@ f = 20 MHz			**TBD**	%
DBHV Threshold (MR Head Resistance measurement)	V_{BHV}	Programmable	42		762	mV
Buffered Head Voltage Gain	A_{BHV}	VMR = 42mV - 762mV	4.75	5	5.25	V/V
Thermal Asperity Detection Range	V_{TATH}	DC level in RDX/RDY over base-line	6		762	mV_{bp}
Thermal Asperity Detection/ DBHV Threshold Tolerance	ΔV_{TATH}	DAC setting	-(10% + 3mV)		10% +3mV	mV
MR Head Voltage	V_{MR}	$I_{MR} \cdot R_{MR}$	100		900	mV
Overshoot on I_{MR} during Mode Transitions: Idle-to-Read, Write-to-Read, Head-to-Head and Bias Off-to-On	I_{MROV}	0.1V < V_{MR} < 0.9V Percent of final I_{MR}			2	%
Undershoot on I_{MR} during Mode Transitions	I_{MRUS}				0	mA

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(base to peak)	15		59.95	mA
Write Current Tolerance	ΔI_W	15mA < I_W < 59.95mA	-8		8	%
Differential Head Voltage Swing	V_{DH}	Open Head, V_{DD}=7.2V	10.8	14		V_{ppd}
		Open Head, V_{DD}=4.5V	5	8		
Unselected Head Current	I_{UH}				50	μA_{pk}
WDX/WDY Input Frequency Range	f_W		5		160	MHz
HWX/HWY Differential Output Capacitance	C_{OW}			**TBD**	**TBD**	pF
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		6	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time			50	ps
Rise/Fall Time	t_r / t_f	10 - 90%		0.8	1.3	ns

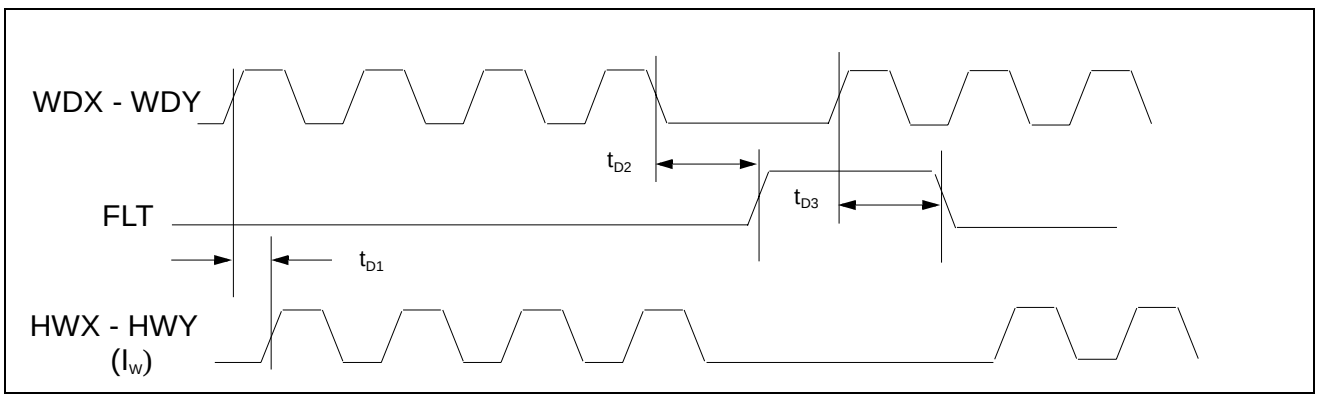


Figure 26 Write Mode Timing Diagram

Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX > WDY current flows into the “Y” port, for WDX < WDY current flows into the “X” port.

SERVO WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply	V_{CC}		4.5	5	5.5	V
	V_{DD}	LVDIS bit = 1	5		5.5	
	V_{DD}	LVDIS bit = 0	7.2		8.8	
Servo Current Range	I_S	base to peak, 6 heads	15		40	mA
		base to peak, 3 heads	15		59.95	
Servo Current Tolerance	ΔI_S	15mA < I_S < 25mA, 35mA < I_S < 59.95mA	-8		8	%
		25mA < I_S < 35mA	-5		5	
MR Head Voltage	V_{MR}	Programmable	25		226.5	mV
Read to Write Mode	t_{RW}	To 90% of servo write current		**TBD**	**TBD**	ns
Read to Write Difference between Heads		To 90% of servo write current for each head			**TBD**	ns

LOW V_{DD} OPERATION CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA, V_{DD}=5V, LVDIS=1.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Rise/Fall Time	t_{rs}/t_{fs}	10-90%		1.75	**TBD**	ns
MR Head Current Accuracy	ΔI_{MR}	2mA < IMR < 9.75mA	**TBD**		**TBD**	%
Differential Voltage Gain	A_V	VIN=1mVpp @80MHz, RL(RDP, RDN)=2kW, applies to the following:				V/V
		4 or 6-channel VM5131B1, Gain bit=0	**TBD**	112	**TBD**	
		4 or 6-channel VM5131B1, Gain bit=1	**TBD**	150	**TBD**	
		4 or 6-channel VM5131B2, Gain bit=0	**TBD**	150	**TBD**	
		4 or 6-channel VM5131B1, Gain bit=0	**TBD**	190	**TBD**	
Equivalent Input Noise (total)	e_n	1 < f < 85 MHz		0.6	**TBD**	nV/$\sqrt{Hz}$
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{DD}, 1 < f < 100 MHz	**TBD**			dB
		100 < f < 170 MHz	**TBD**			
Write to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value [1]		**TBD**	**TBD**	ns

1. MRBIAS/FAST pin low for 10µs preceding R/WN transition (assumes MRB = 1 and IMR DAC).

PINNED LAYER REVERSAL CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PLR Pulse Amplitude	V_{RESET}	Referenced to ground Value set in I_W DAC (2:<D0-D4>). See (eq. 15).	0.4		1.64	V
PLR Pulse Width	t_{PW}	Value set in 7:<D2-D3>. See Table 18	50		200	ns
PLR Pulse Decay Rate	d_V/d_t	Value set in 7:<D0-D1>. See Table 19	1.75		7	mV/ns
PLR Pulse Setup Time	t_{ARM}		500			ns
PLR Pulse Delivery Time	t_{EN}		**TBD**			ns

MODE SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		43	50	ns
Write to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value or 90% of read envelope [1]		180	300	ns
Idle to Read Mode [2]	t_{IR}	RDP/RDN to within ±30mV of final value or 90% of read envelope		6	10	µs
Sleep to Idle Mode [2,3]	t_{SR}	RDP/RDN to within ±30mV of final value or 90% of read envelope		**TBD**	600	µs
Read Mode, Head Select to Any Head, I_{MR} switch [2]	t_{HS}	RDP/RDN to within ±30mV of final value, or 90% of read envelope, or 90% of I_{MR}		6	10	µs
Idle Mode Powerup Time (from Sleep Mode)				300		µs
Read to Idle [2]	t_{RI}	To 10% of read envelope		0.16	0.5	µs
Write to Idle [2]	t_{WI}	To 10% of write current		**TBD**	50	ns
Read Bias Disabled to Bias Enabled	t_{RB}	BIASN pin high to low to 90% of IMR			10	µs

1. BIASN pin low for 10µs preceding R/WN transition.
2. Timing for mode change, which is initiated in serial register, is measured from SPE high to low edge.
3. Sleep to Read mode change transitions through Idle mode and must remain in Idle mode for a minimum of 300µs.

FAULT CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fault Threshold	VCC_{DTH}	I_w < 200µA, Fault detected	3.6	3.8	4.0	V
	VCC_{UTH}	Fault removed	3.9	4.1	4.3	
V_{CC} Fault Threshold Hysteresis	VCC_{HTH}		200	300	400	mV
V_{DD} Fault Threshold	VDD_{DTH}	I_w < 200µA, Fault detected	5.8	6.1	6.4	V
	VDD_{UTH}	Fault removed	6.3	6.6	6.9	
V_{DD} Fault Threshold Hysteresis	VDD_{HTH}		400	500	600	mV
Threshold for Open MR Head Fault Detection			0.95	1.1	1.3	V
Threshold for MR Head Shorted to GND Fault Detection				50		mV
Open MR Head Delay		From Head Switch to Open MR Head reported (SPE goes low to FLT pin low)		10	20	µs
Writer Open/Shorted Head Detection Threshold	V_{OSHD}	ΔV across write element at next WDX/WDY transition, where $\Delta V = R_{OpenHead} * I_W$ OR Head resistance to GND <15Ω.			2.5	V
Open/Shorted Write Head Blanking Time	t_{OS}			7 [1]		ns
FLT delay, Write Safe to Unsafe [2]	t_{D2}	Fault Safe guaranteed for write data transitions <500ns apart.	0.5	1.5	3.6	µs
FLT delay, Write Unsafe to Safe [2]	t_{D3}				1.1	µs
TA FLT Delay [3]	t_{D4}	TA detected to FLT pin low		30	100	ns
TA FLT Pulse Width [3]	t_{D5}		1	1.5	2	µs
Temperature Threshold for Hot Fault	T_{HOT}			135		°C

1. Will not detect or report fault for write current transitions less than 7ns apart.
2. See Figure 26 on page 50.
3. See Figure 16 on page 32.

VTC Inc.
Value The Customer™

VM5141

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR/GMR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Operates from +8 and +5 Volt Power Supplies
  - 2.5/3.3V CMOS Compatible Logic Interface
  - Fault Detection Capability
  - Available in a 30-pin VSOP or TSSOP Packages
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 2 - 9.75 mA Range
  - Programmable Read Voltage Gain
    (195 V/V or 265 V/V Typical)
  - Thermal Asperity Detection and
    Fast Recovery Compensation
  - Analog and Digital Buffered Head Voltage (ABHV/DBHV) Measurement Modes
  - Input Noise = 0.6 nV/$\sqrt{\text{Hz}}$ Typical
    (R_{MR}=45Ω, I_{MR}=8mA)
  - High Bandwidth = 270 MHz Minimum
    (R_{MR}=45Ω, -3dB)
  - Power Supply Rejection Ratio = (60 dB (1 < f < 100 MHz))
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 60 mA Range
  - Rise Time = 0.8 ns Typical, I_W=40 mA
    (for Real Head Model having L_{TOT}=85 nH)
  - Multi-Channel Servo Write

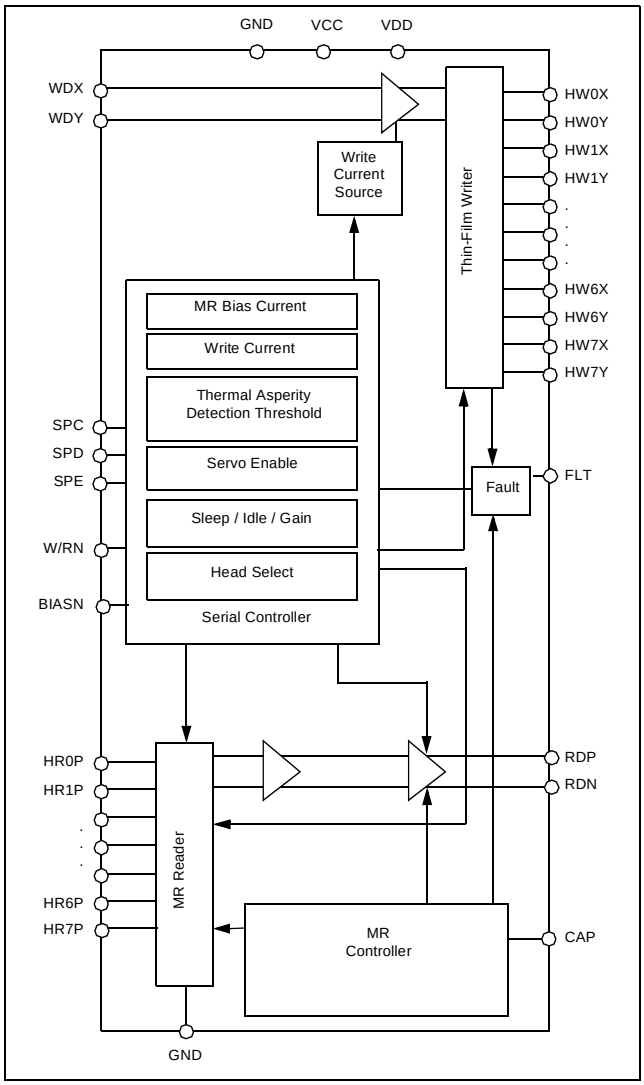
DESCRIPTION

The VM5141 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM5141 operates from +8V and +5V power supplies. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM5141 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available as 4-channel option in a 30-pin VSOP package, as a 6-channel option in a 38-pin VSOP and as a 8-channel option in a 48-pin TQFP package. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V
- V_{DD} ..... -0.3V to +10V

Read Bias Current, I_{MR} 12mA
Write Current, I_W 65mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
- 30-lead VSOP ..... 101°C/W
- 38-lead VSOP ..... 88°C/W
- 48-lead TQFP ..... 75°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%
- V_{DD} .....+8V ± 10%

Write Current, I_W .....15 - 60 mA
Write Head Inductance, L_W ..... 60 - 160 nH
Write Head Resistance, R_W ..... 5 - 25 Ω
Read Bias Current, I_{MR} ..... 2 - 9.75 mA
Read Head Inductance, L_{MR} ..... 20 - 40 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω
Reader Output Load ..... 220 Ω
MR Bias Loop Compensation, CAP ..... 22 nF
Junction Temperature, T_J ..... 0°C to 125°C

OPERATIONAL MODES

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element that correspond to magnetic field changes on the disk.

The VM5141 uses the current-bias/current-sensing MR architecture. The magnitude of the bias current ranges from 2 - 9.75 mA and is governed by the following equation:

$$I_{MR} = 2 + 0.25(k_{IMR}) \qquad \textit{(eq. 1)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
k_{IMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>.

A low level signal applied to the W/RN and BIASN pins (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the read mode and activates the read fault detection circuitry (see Table 24).

Passing the magnetic media by the MR element causes MR resistance changes as a result of changes in the magnetic field. The change in resistance is sensed as a change in current within the preamp, and this current change is converted to a differential voltage that is amplified prior to being output to the RDX and RDY pins.

MR Bias Current Enable

Taking the BIASN pin low in read mode enables MR bias current to the selected head. Taking the BIASN pin high in read mode turns off the bias current to the head. The reader outputs are pulled to the common-mode voltage by the internal high value resistor.

Gain and Boost Bits

The GAIN bit (4:<D2>) selects high or low signal gain. The BOOST bit (4:<D4>) increases read gain by 3dB at 80Mhz.

$$A_V = \frac{k}{\frac{25}{I_{MR}} + R_{MR}} \qquad \textit{(eq. 2)}$$

Av represents the Differential Voltage Gain in V/V
Where k = 10828 for low gain or 14438 for high gain.
I_{MR} is in mA.

MR Head Switch Overvoltage Control

The preamp controls the bias current loop capacitor voltage during head switching or modal transitions, in order to prevent overvoltage of the MR element.

When switching between heads, changing IMR, or in any mode where the bias current becomes disabled (Write or Idle modes, or BIASN pin set high in Read mode), the MR bias current is diverted from the MR head while the bias current loop capacitor voltage is quickly discharged to a Vbe above ground. This ensures that the MR head voltage always rises from a safe voltage to the specific IMR*RMR.

Write Mode

In the write mode, the circuit operates as a thin-film write-current switch, driving the thin-film write element of the MR head.

The magnitude of the write current ranges from 15 - 59.95 mA. The following equation governs the write current magnitude:

$$I_W = 15 + 1.45(k_{IW}) \qquad V_{DD} = 8V$$
$$I_W = 14.5 + 1.4(k_{IW}) \qquad V_{DD} = 5V(\text{Low}V_{DD}\text{Mode}) \qquad \textit{(eq. 3)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 31) in 2:<D0-D4>.

A high level applied to W/RN pin (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the write mode (see Table 24). The write data signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 39.

MR Bias Current Enable

Taking the BIASN pin low in write mode enables MR bias current to the selected head. Taking the BIASN pin high in read mode turns off the bias current to the head. In write mode, the reader outputs are pulled to the common-mode voltage by the internal high value resistor.

Write Current Waveform Shaping Control

The write current waveform can be shaped using the control bits in register 5. The OSD bit (5:<D1>) selects an increase (OSD = 0) or decrease (OSD = 1) in the amplitude of the overshoot. The OSC bits (5:<D2-D4> select the percentage of overshoot. The USC bits (5:<D5-D7> select the percentage of undershoot.

Note: The overshoot or undershoot induced by the register settings is dependent on write load and current settings. See Tables 28 and 29, and Figures 30 through 33 for examples.

Servo Write Mode

In the servo write mode, the even, odd or all channels of the VM5141 are written simultaneously. The servo write current magnitude is governed by (eq. 3) in the Write Mode section.

The reader circuitry is shutdown during servo mode to reduce power consumption and the associated heat. MR head fault detection and reporting are disabled during Servo Write Mode.

Servo mode is initiated by a seven-step process (see Table 24):

6) Select Head 0, 2, 3, 4 or 6 (‘none’ in Servo Bank Write).[1]
7) Select Read mode by setting W/RN pin to a ’0’.
8) Set the SBW0 bit (4:<D5>) to a ’1’.
9) Set the SBW1 bit (2:<D7>) to a ’1’.
10) Set the SBW0 bit to a ’0’ to initiate Servo mode.
11) Select Heads 1, 5 or 7 (‘odd’, ‘all’ or ‘even’ in Servo Bank Write). [2]
12) Set W/RN pin high to enable servo write current. [3]

1. This step prevents an overvoltage spike to the MR heads when servo mode is entered.
2. The HS0-HS2 register bits (1:<D0-D2>) determine which heads are written (see Table 25).
3. W/RN pin enables or disables write current to the heads but does not affect the servo mode.

To exit Servo mode, set SBW1 to ’0’ and perform a head select or toggle the BIASN pin.

Note: The customer is responsible for ensuring that the thermal constraints of the package are not exceeded. This may be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo write active duty cycle.

Low V_{DD} Mode

If V_{DD}<7.2V, the LVDIS bit (2:<D6>)must be set to ’1’ in order to continue to write or read.

MR Bias Voltage Enable

Taking the BIASN pin low in servo write mode applies a common voltage bias to all selected heads, see Table 25. The magnitude of this bias voltage ranges from 25 to 226.5 mV [1] and is governed by the following equation:

1. The values do not include the contribution of servo write current and bond wire.

$$V_{MR} = 25 + 6.5(k_{VMR}) + 0.05([1.1(I_S) + 14.5]N + 26) \quad \textit{(eq. 4)}$$

where V_{MR} represents bias voltage applied to the selected MR element (in mV), k_{VMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>, I_S represents the servo write current DAC setting (0 to 31) in 2:<D0-D4>, and N represents the number of heads in servo bank write. Note: 0.05 is the bond wire resistance.

Taking the BIASN pin high in servo write mode disables MR head bias.

MR head fault detection and reporting are disabled during Servo Write mode.

Idle Mode

Setting the IDLEB bit low (4:<D1>) and SLPB bit high (4:<D0>) places the preamp in Idle mode (see Table 24). Only the serial register, internal read bias circuitry and power supply fault reporting remain active.

The reader outputs are pulled to the common-mode voltage by the internal high value resistor.

Sleep Mode

Setting the SLPB bit low (4:<D0>) places the preamp in Sleep mode (see Table 24). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Note: Transitions from Sleep mode to Read mode should always be made by first entering the Idle mode for a minimum of 300µs.

Note: After a transition from Sleep mode to Idle mode, the Fault Register (register 6) must be written. This initializes the register to a defined or cleared state.

Table 24 Mode Select

W/RN	*BIASN*	*Servo*	*IDLEB 4:<D1>*	*SLPB 4:<D0>*	*MODE*
0	1	0	1	1	Read Bias Disabled
0	0	0	1	1	Read Bias Enabled
1	1	0	1	1	Write Bias Disabled
1	0	0	1	1	Write Bias Enabled
X	1	1	1	1	Servo [1]
X	0	1	1	1	Servo [1] Bias Enabled
X	X	X	0	1	Idle Bias Disabled
X	X	X	X	0	Sleep

1. Servo Write Mode on page 57 describes the process for initiating.

Table 25 Head Select

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*Normal [1] Write/Read Head*	*Servo Bank Write*
0	0	0	0	none
0	0	1	1	odd
0	1	0	2	none
0	1	1	3	none
1	0	0	4	none
1	0	1	5	all
1	1	0	6	none
1	1	1	7	even

1. If *Head Selected* > *Channel Count - 1*, an Invalid Head Select fault will be reported.

ESD PROTECTION FOR MR HEAD

Characteristics for ESD diodes at MRP pins are:
R_{ON} = 2Ω, C = 0.3pF, t_{ON} = 0.6ps.

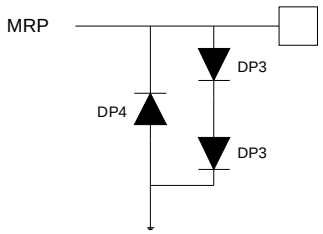


Figure 27 ESD Protection of MR Heads

FAULT HANDLING

Conditions triggering faults, and status and reporting during the fault are listed in Table 26. Non-fault conditions are indicated by a dash, the fault pin level for this condition is that of a safe condition (e.g., Open MR Head in Idle mode, FLT = H).

Table 26 Fault Table

		FLT pin level by Mode [1]					Register:Bit [2]
FAULT	CONDITION	Read [3]	Write	Servo	Idle	Sleep	Setting
None	Safe	H	L	L	H	H	—
Hot	TEMP bit = 1, Die temperature > 135°C	L	H	H	—	—	6:<D0> = 1
Low VCC	VCC < 3.8V; Resets when VCC > 4.1V	L [4]	H [4,5]	H [5,6]	L	—	—
Low VDD	LVDIS bit = 0, VDD < 6.1V; Resets when VDD > 6.4V	L [4]	H [5]	H [5]	L	—	6:<D1> = 1
	LVDIS bit = 1	H	L	L	—	—	6:<D1> = 0
Open MR Head	BIASN pin = L, VMR > 950 mV	L [7]	—	—	—	—	6:<D2> = 1
Shorted MR Head	BIASN pin = L, VMR < 50 mV	L [7]	—	—	—	—	6:<D3> = 1
Invalid Head Select	Head Selected > Channel Count - 1	L [4]	H [6]	—	—	—	—
Open/Shorted Write Head	(ΔV across write element > 2.5V at next WDX/WDY transition, where ΔV = $R_{OpenHead}$*I_W OR Head resistance to GND <15Ω) AND (WDX/WDY transition spacing > Open/Shorted Write Head Blanking Time)	—	H [8]	—	—	—	6:<D4> = 1 6:<D5> = 1
Low Write Frequency	1.5 ms typical between transitions	—	H	—	—	—	6:<D6> = 1
Thermal Asperity	BIASN pin = L, TA DAC > 0, (RDP-RDN) > TA Threshold	L	—	—	—	—	—

1. L = FLT pin low, H = FLT pin high impedance - pulled to level set by external pull-up resistor.
2. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to '0'.
3. Read faults are disabled if MRM is enabled (4:<D3> = 1).
4. MR bias current disabled to MR head. Bias loop capacitor maintained for optimal recovery and at a low voltage to prevent MR element overvoltage.
5. Write current is disabled until the fault is cleared.
6. V_{MR} is not disabled.
7. An open or shorted head fault is latched on the FLT line and the head voltage is clamped to a safe low voltage. The FLT latch and head voltage clamp are cleared by a change in head selection or I_{MR}, or a mode switch.
8. Two WDX/WDY transitions may be required to clear the FLT line after the fault has cleared.

Other Features Utilizing FLT Pin

Three bits (MRM, ABHV, TEMP) affect the FLT pin output. Table 27 defines the function of the output on the FLT pin.

Table 27 FLT Pin Output Functions

Setting	Function	TEMP 4:<D7>	ABHV 4:<D6>	MRM 4:<D3>
1	Normal Fault Reporting [1]	0	0	0
2	DBHV - MR Measurement Mode	0	0	1
3	ABHV - Analog Buffered Head Voltage	0	1	0
4	Not Valid	0	1	1
5	Hot Fault Reporting Enabled (in addition to Normal Fault Reporting)	1	0	0
6	Not Valid	1	0	1

Table 27 FLT Pin Output Functions

7	Analog Temperature	1	1	0
8	Not Valid	1	1	1

1. As defined in Table 26.

MR Measurement / Digital Buffered Head Voltage (DBHV)

Setting the MRM bit high (4:<D3>) while the TEMP and ABHV bits are low allows the digital buffered head voltage (DBHV) to be represented on the FLT pin.

The FLT output is low when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to exceed the threshold level as determined by the TA/DBHV DAC (3:<D6-D0>). The FLT output is high when the $I_{MR} \cdot R_{MR}$ product falls below this level.

Note: The FLT line is not valid for 2µs after changing the TA/DBHV DAC.

$$DBHV = 6(k_{TA}) \qquad \textit{(eq. 5)}$$

DBHV represents the voltage level from the MR element (in mV).
k_{TA} represents the TA/DBHV DAC setting (7 to 127) in 3:<D0-D6>.
The threshold settings in TA/DBHV DAC (0 to 6) cannot be detected.

MR Measurement Mode Procedure

Set a fixed IMR bias current and decrease the TA/DBHV DAC settings until the FLT pin goes low. Example: IMR = 6mA, TA/DBHV DAC setting to cause FLT low = 330mV, then MR resistance = 55Ω (330/6).

Analog Buffered Head Voltage (ABHV)

Setting the ABHV bit high (4:<D6>) while the MRM and TEMP bits are low allows an amplified representation of the MR bias voltage to be multiplexed on the FLT pin. (The external pullup resistor must be removed for this mode.) The voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} \cdot R_{MR}) \qquad \textit{(eq. 6)}$$

Analog Temperature

Setting the ABHV and TEMP bits high while MRM is low multiplexes the voltage representation of the die temperature on the FLT pin. (Note: The external resistor must be removed for this mode of operation.) A voltage (1V to 3V) on the FLT pin represents the die temperature (0^oC to 200^oC) given by the equation:

$$TEMP(^oC) = (V - 1) \times 100 \qquad \textit{(eq. 7)}$$

Where V = voltage (1V to 3V) at FLT pin.

THERMAL ASPERITY DETECTION AND COMPENSATION

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. The thermal asperity may result in a positive or negative signal disturbance. Figure 28 displays the reader output for an uncompensated, positive thermal asperity event.

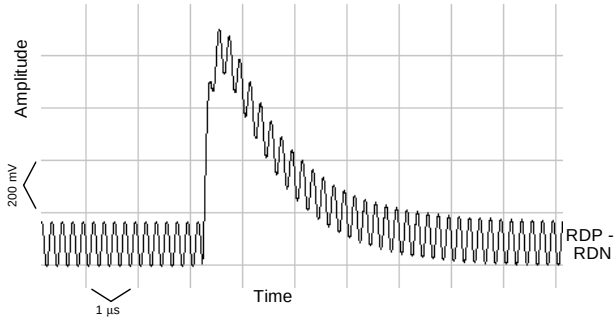


Figure 28 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM5141 implements both a programmable detection threshold and fast recovery compensation for positive, and positive or negative (dual direction) disturbances.

Detection

Programming a non-zero TA detection threshold value (3:<D6-D0>) allows the TA detection circuitry to detect a positive asperity event. Setting the Dual Direction TA bit (7:<D7> = 1) allows detection of positive and negative asperity events. The threshold for thermal asperity detection is output-referred, has a range of 6 - 762 mV and is governed by the following formula:

$$TA_{level} = 6(k_{TA}) \qquad \textit{(eq. 8)}$$

TA_{level} represents the voltage level from the MR element (in mV).
k_{TA} represents the TA DAC setting (1 to 127) in 3:<D0-D6>

TA detection is turned off when the TA detection threshold value is zero (3:<D6-D0> = 0).

Reporting

Whenever a thermal asperity event is detected, it is reported as a low ('0') on the FLT pin.

Compensation and Fast Recovery

When the TAC bit is enabled (3:<D7> = 1), thermal asperity compensation mode is initiated if a thermal asperity is detected.

Note: Setting the TAC bit off (3:<D7> = 0) makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the low corner frequency movement.

When activated, Fast Recovery and Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 10 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 29). Additional TA events during t_{D5} will not be compensated.

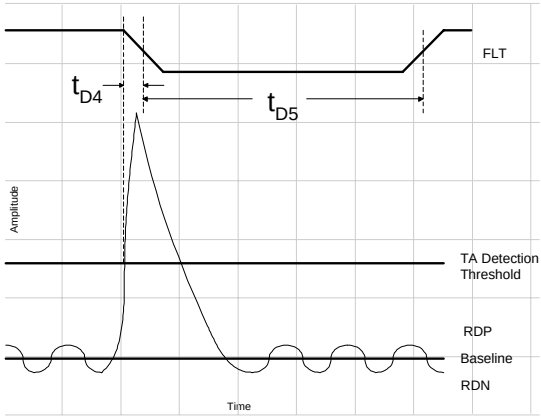


Figure 29 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

WRITE CURRENT WAVEFORM SHAPING

Tables 28 and 29 summarize write current simulations at both 40 and 60 mA with the load as shown in Figure 30 . The family of curves in Figures 31 through 33 depict the response of programmable overshoot and undershoot under nominal conditions (nominal process, VDD = 8V, VCC = 5V, and T = 75oC). For the calculations of over/undershoot, I_W is the write current amplitude from base (0mA) to the settled point (write current setting in mA). The write current is the current in R2 in the head model depicted in Figure 30.

Table 28 Write Current Overshoot Control

OSD 5:D1	OSC2 5:D4	OSC1 5:D3	OSC0 5:D2	Iw = 40 mA		Iw = 60 mA	
				Overshoot % [1]	% Change from '000' [2]	Overshoot % 1	% Change from '000' 2
0	0	0	0	90	0	53	0
0	0	0	1	95	5	57	3
0	0	1	0	103	13	62	8
0	0	1	1	110	20	67	13
0	1	0	0	118	28	70	17
0	1	0	1	128	38	73	20
0	1	1	0	133	43	75	22
0	1	1	1	138	48	77	23
1	0	0	0	90	0	53	0
1	0	0	1	73	-18	45	-8
1	0	1	0	60	-30	40	-13
1	0	1	1	55	-35	37	-17
1	1	0	0	48	-43	30	-23
1	1	0	1	40	-50	25	-28
1	1	1	0	35	-55	20	-33
1	1	1	1	33	-58	17	-37

1. Overshoot % = (Overshoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

Table 29 Write Current Undershoot Control

USC2 5:D7	USC1 5:D6	USC0 5:D5	Iw = 40 mA		Iw = 60 mA	
			Undershoot % [1]	% Change from '000' [2]	Undershoot % 1	% Change from '000' 2
0	0	0	-23	0	-18	0
0	0	1	-15	8	-10	8
0	1	0	-10	13	-8	10
0	1	1	-5	18	-7	12
1	0	0	0	23	-5	13
1	0	1	5	28	-3	15
1	1	0	8	30	-2	17
1	1	1	10	33	0	18

1. Undershoot % = (Undershoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

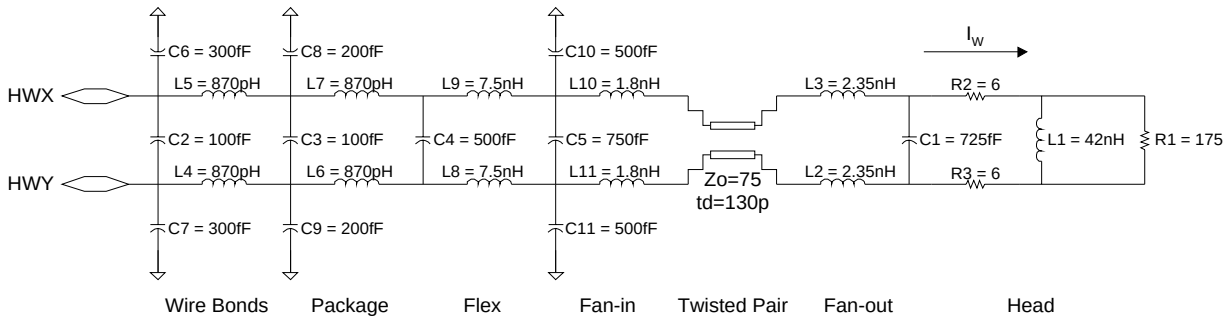


Figure 30 Writer Head Model

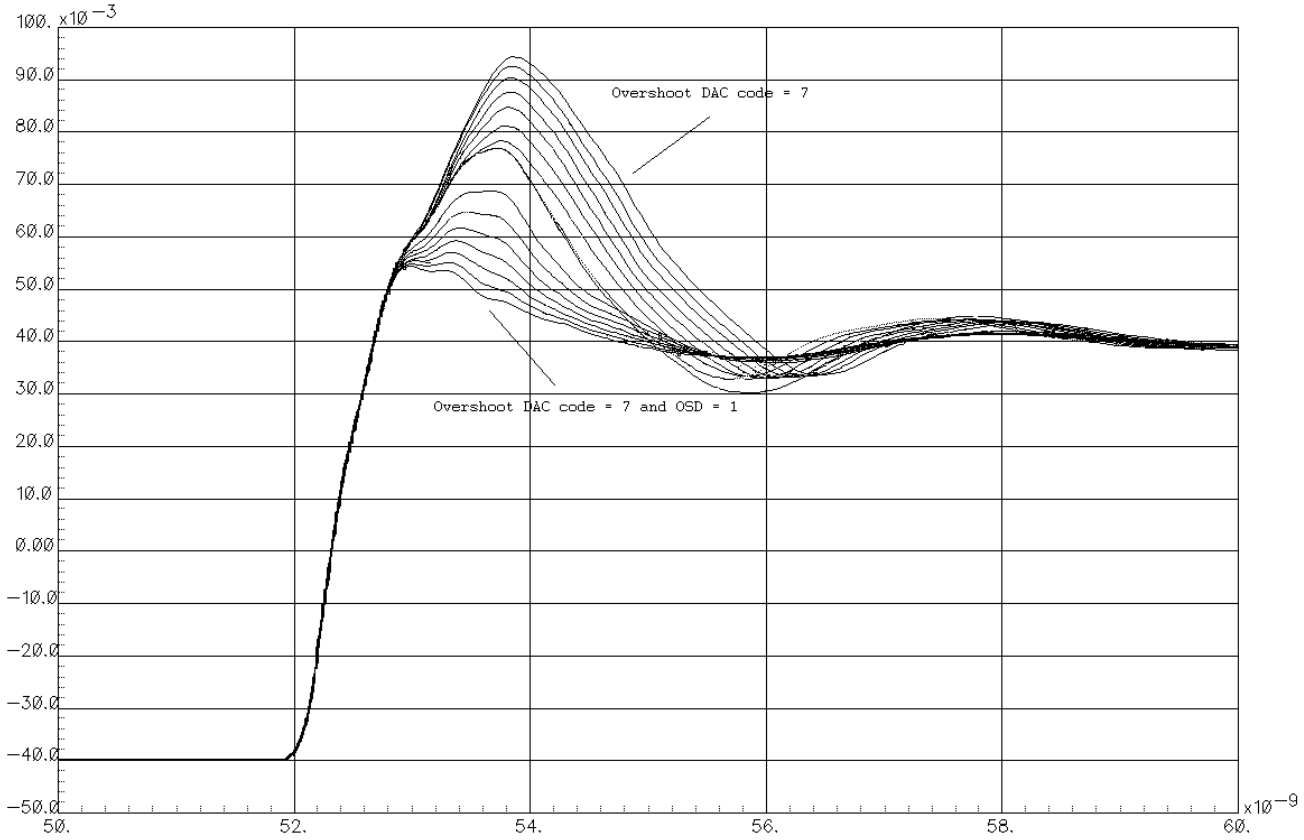


Figure 31 Simulation Of The Programmable Overshoot at Iw=40mA Under Nominal Conditions (nom process, +8,+5V power, 75oC)

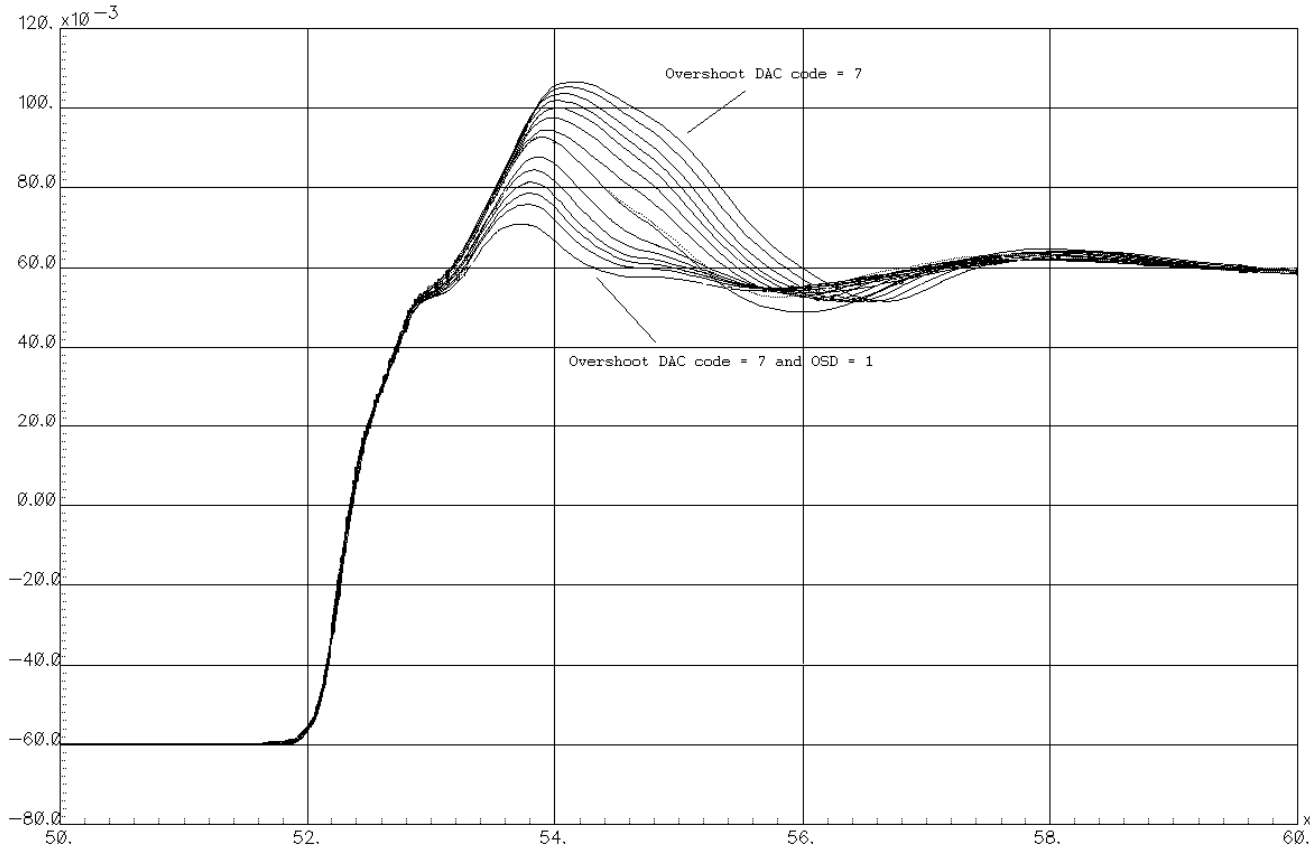


Figure 32 Simulation Of The Programmable Overshoot at Iw=60mA Under Nominal Conditions (nom process, +8,+5V power, 75oC)

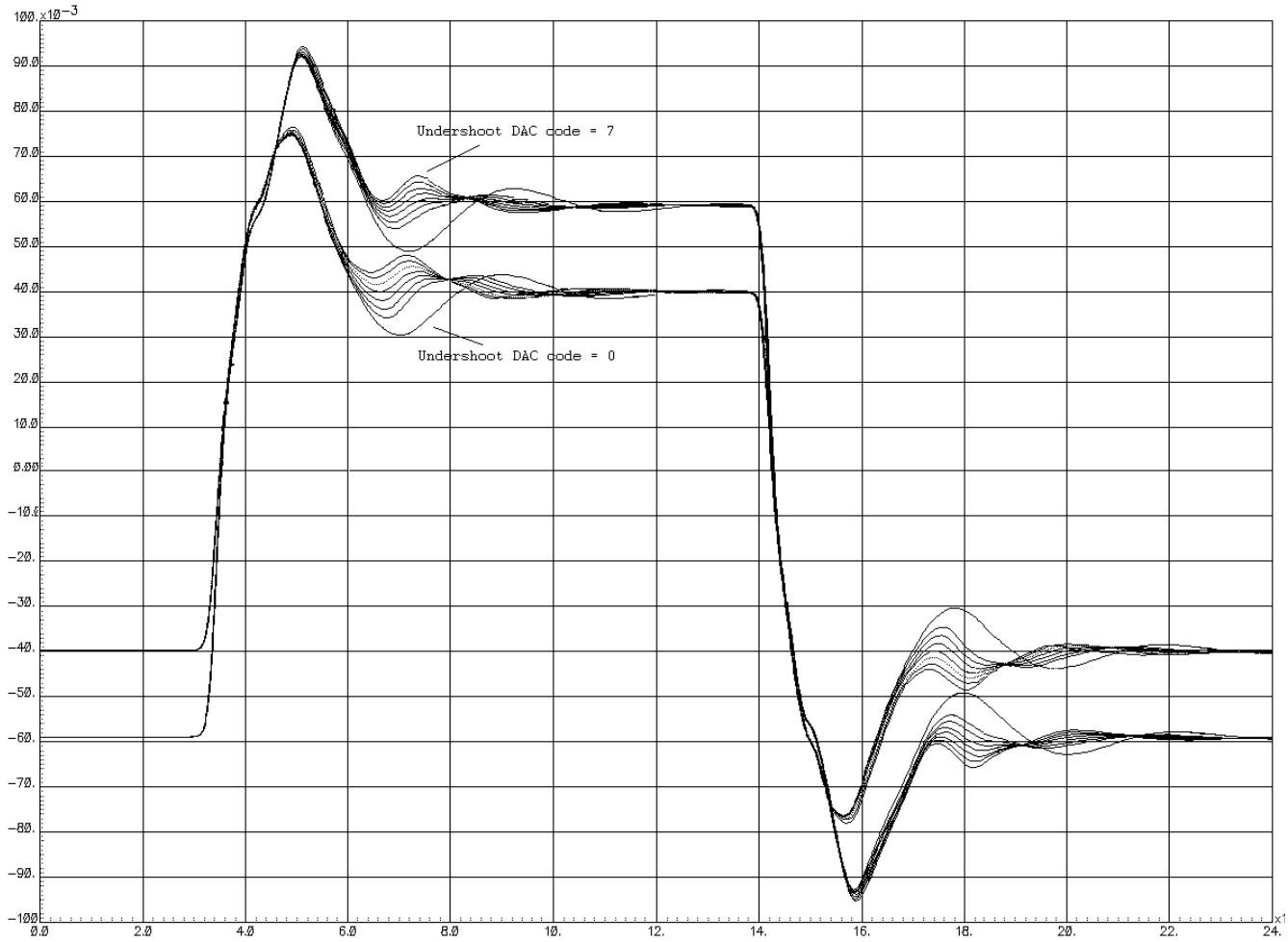


Figure 33 Simulation Of The Programmable Undershoot at Iw=40 and 60mA Under Nominal Conditions (nom process, +8,+5V power, 75oC)

PINNED LAYER REVERSAL MODE

Pinned Layer Reversal (PLR) mode provides a means to correct GMR heads that are affected by a reversed pinned layer. When the preamp is placed in the PLR mode, a positive reset pulse can be applied to the selected head. The external BIASN pin is used to control the timing of the delivery of the reset pulse to the GMR element. Several control bits are provided to shape the reset pulse. These controls include pulse amplitude, duration and decay rate. (See PINNED LAYER REVERSAL CHARACTERISTICS on page 81 for specifications.)

PLR Reset Pulse Controls

The amplitude of the reset pulse ranges from 0.4 to 1.64 V and is governed by the following equation:

$$V_{RESET} = 0.4 + 0.04(k_{PLR}) \qquad \textit{(eq. 9)}$$

where V_{RESET} represents the reset pulse voltage amplitude
k_{PLR} represents the I_W DAC setting (0 to 31) in 2:<D0-D4>.
Note that the MR heads ESD diodes may limit the maximum V_{RESET} amplitude achieved to around 1.4V.

The reset pulse duration and decay time are determined by the settings of the PLRPW bits (7:<D2-D3>) as shown in Table 30 and the PLRDT bits (7:<D0-D1>) as shown in Table 31.

Table 30 PLR Reset Pulse Width

PLRPW1 7:<D2>	*PLRPW0 7:<D3>*	*PLR Pulse Width (ns)*
0	0	50
0	1	100
1	0	150
1	1	200

Table 31 PLR Reset Pulse Decay Rate

PLRDT1 7:<D0>	*PLRDT0 7:<D1>*	*PLR Decay Rate (mV/ns)*
0	0	7
0	1	4.67
1	0	2.33
1	1	1.75

PLR Timing and Event Description

Figure 34 depicts a timing diagram for the PLR mode. The steps involved are:

1) Set up VRESET via IW DAC, IMR, PLRPW and PLRDT, and select the head to be reset while in Idle or Read mode.
2) Enter the Read mode by setting IDLEB bit to ‘1’. Bring BIASN high to disable MR head bias.
3) Enter PLR mode by setting PLREN bit 7:<D4> to ‘1’.
4) After a minimum time tARM, bring BIASN low to trigger the pulse.
   Note: The PLR trigger depends on the sequence PLREN set to ‘1’ followed by a high to low transition of the BIASN pin. Subsequent high to low transitions of BIASN will not retrigger the PLR mode.
5) Exit the PLR mode after a minimum time t_{EN}, by setting PLREN bit to ‘0’.
   The device returns to Read mode, in which the state of the BIASN pin controls MR head bias.
6) To clear the MR Short fault, perform a head select or toggle BIASN.

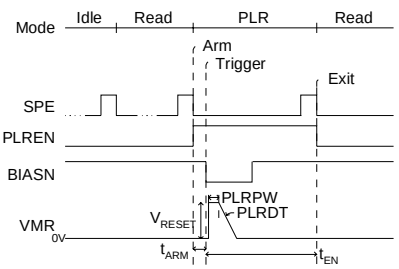


Figure 34 PLR Timing Diagram

VM5141 SERIAL PORT INTERFACE AND CONTROL REGISTERS

The serial port interface and the associated control registers provide programming and monitoring of the VM5141 circuitry. The interface handles the communication between a system control chip and the VM5141 via a three wire interface and related protocols. The control registers hold programming data written to the VM5141 and provide readback monitoring of data held or generated within the VM5141.

Note: If serial port activity is performed during Read mode, crosstalk to the reader output may result.

Serial Port Interface

The serial port interface provides for both writing data to and reading data from the VM5141. Its three pins are:

- SPC (Serial Port Clock) synchronizes the transfer.
- SPD (Serial Port Data) is the bi-directional data pin.
- SPE (Serial Port Enable) enables and disables a serial transfer.

All data writes or reads are enabled by setting SPE = 1 after which the SPC clocks data in or out via the SPD.

Writing to the Serial Port

A data transfer is initiated by setting SPE = '1'. A write data packet is structured as a 16-bit word: '0' for writing + 3 page address bits + 4 byte address bits + 8 programming data bits.

Each rising edge of SPC clocks data into the serial port interface. For valid data transfers, data are loaded into a designated register location upon the falling edge of SPE. Only the first 16 SPC rising edges after SPE goes high are recognized by the serial port interface. Any SPC rising edges after the first 16 are ignored. If less than 16 clock pulses are provided before SPE goes low, the data transfer is aborted.

Figure 35 shows the protocol for a write transfer operation. Refer to Table 32 and Figure 37 for timing specifications for the serial port interface.

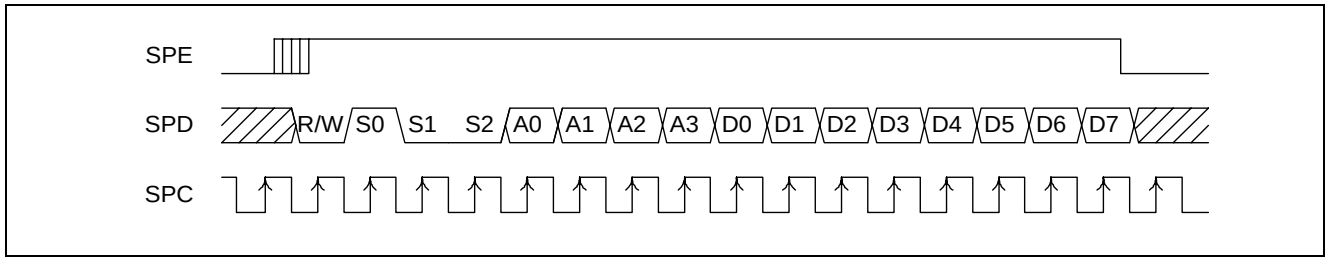


Figure 35 Write Protocol for 3-Write Serial Port Interface

Readback from the Serial Port

The read data packet is structured as: '1' for reading + 3 page address bits + 4 byte address bits + 8 data bits. To perform a read instruction, first set SPE =1 and then input the read instruction bit '1', the 3-bit page address, and the 4-bit byte address. The 8-bits at the specified register address are subsequently clocked out at the SPD pin.

Each rising edge of SPC clocks the instruction bit and the address bits into the serial port interface and the rising SPC edge also clocks out the data information. The SPE falling edge returns the SPD pin to an input pin state. The serial port interface drives the SPD pin only if the page address matches that of the VM5141.

Figure 36 shows the protocol for a read transfer operation. Refer to Table 32 and Figure 37 for timing specifications for the serial port interface.

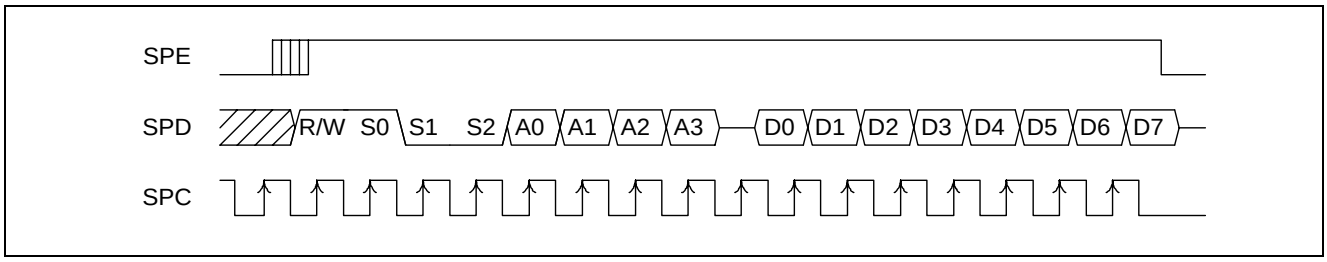


Figure 36 Read Protocol for 3-Wire Serial Port Interface

Table 32 Serial Port Interface Timing Specifications

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SPC Frequency	f_{SPC}	Write operation			25	MHz
		Readback operation			12.5	MHz
SPC High Time	t_{SPCH}	Write operation	14			ns
		Readback operation	32			ns
SPC Low Time	t_{SPCL}	Write operation	14			ns
		Readback operation	32			ns
SPE Rise Setup Time	t_{SEr}	Relative to SPC rising edge	10			ns
SPE Rise Hold Time	t_{HEr}	Relative to SPC rising edge	10			ns
SPE Fall Hold Time	t_{HEf}	Relative to SPC rising edge	10			ns
SPD Setup Time	t_{SD}	Data input relative to SPC rising edge	10			ns
SPD Hold Time	t_{HD}	Data input relative to SPC rising edge	10			ns
SPD Prop Delay	t_{PDD}	Data output relative to SPC rising edge			16	ns
SPD Enable Time	t_{PZD}	Time to take control of SPD relative to SPC rising edge			16	ns
SPD Disable Time	t_{PDZ}	Time to release control of SPD relative to SPE falling edge			16	ns
SPE Low Time	t_{SPEL}	Between transmissions	1/ f_{SPC}			ns

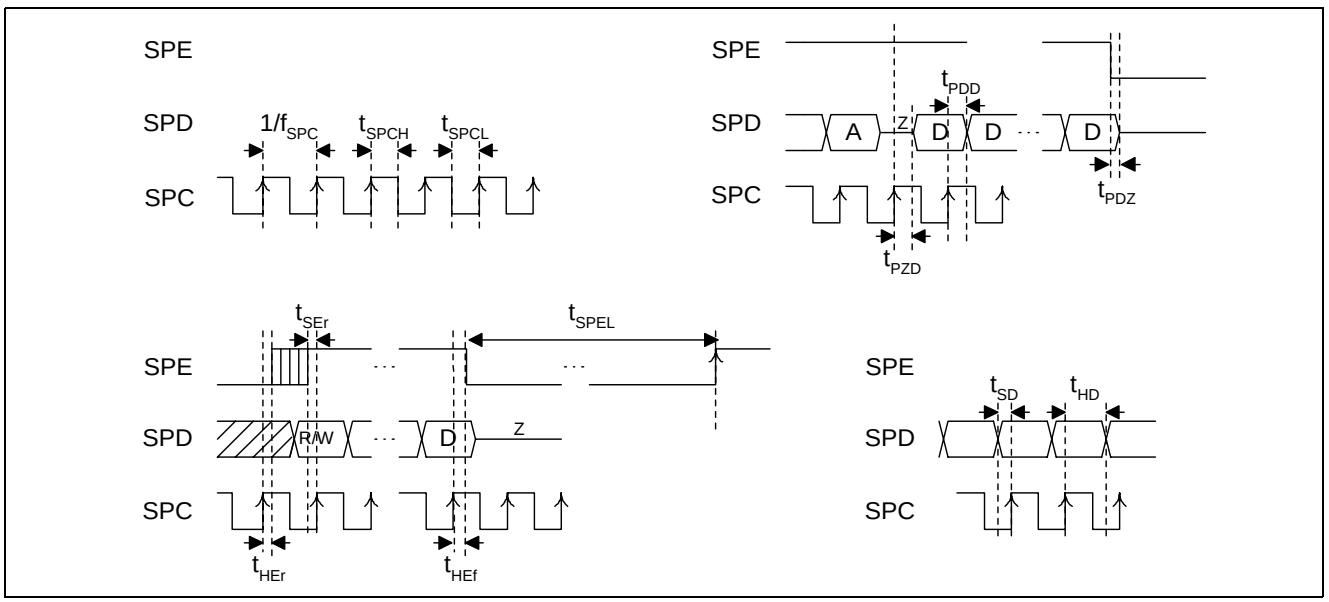


Figure 37 Timing Diagrams for 3-Wire Serial Port Interface

Control Registers

Control registers provide for storage and readback of programming data (i.e., an SRAM type function) and for monitoring of information generated (i.e., SRLatch type function) or hard-coded within the VM5141 (i.e., a ROM type function). The control registers are organized in byte-wide segments, each byte being either an SRAM-type, a ROM-type, or a SRLatch-type.

The addressing scheme for an entire system is as follows. There are 7 bits of address in a system. The first 3 bits, S0-S2, determine the page address, while the last 4 bits, A0-A4, determine a particular byte address within a page. A system may have a total of 8 pages with a total of 16 bytes per page. Each chip in the system is assigned one or more full pages (the VM5141 has a single page). All 16 bytes within each assigned page need not be used. Unused bytes within a chip's page are reserved for possible future use within the assigned chip; they may not be reassigned within the system.

Data written to an unused byte or page address is ignored. Reading from an unused byte in a valid page results in a logic '1' on the SPD line. However, reading from an invalid page address results in no data being transmitted, as the SPD output driver remains turned off until a valid page is addressed. When data is to be read from a valid page address all other chips must keep their SPD output drivers turned off and allow the chip assigned that page address sole control of the SPD line.

VM5141 control registers extend across one page address. The page address is S<0:2> = 1 (001b) and it contains byte addresses 0 (0000b) to 15 (1111b), but not all 16 bytes are used. Table 33 depicts register bit assignments and Table 34 explains the defined register bits. All SRAM and SRLatch registers are set to logic '0' at power-up. Register 0, a ROM type, is hard-coded as follows: the revision level bits (REV0 to REV3) are programmed to the appropriate design revision level (0 = 0000b and 15 = 1111b) and the vendor bits (VEN0 to VEN2) are set to 0 (000b).

Table 33 Control Register Map

Register			***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0*** [1]
Address	***Title***	***Type***								
0	ID/Rev	ROM	CCI	REV3	REV2	REV1	REV0	VEN2	VEN1	VEN0
1	HS/IMR	SRAM	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
2	IW/Servo	SRAM	SBW1	LVDIS	[2]	IW4	IW3	IW2	IW1	IW0
3	TA	SRAM	TAC	TA6	TA5	TA4	TA3	TA2	TA1	TA0
4	Mode	SRAM	TEMP	ABHV	SBW0	BOOST	MRM	GAIN	IDLEB	SLPB
5	WCC	SRAM	USC2	USC1	USC0	OSC2	OSC1	OSC0	OSD	[2]
6	Faults [3]	SRLatch	[2]	LOFR	WRSH	WROP	MRSH	MROP	LOVDD	HOT
7	PLR	SRAM	DUALTA	TOSC	OSDLY	PLREN	PLRPW0	PLRPW1	PLRDT0	PLRDT1

1. <D0> is the first bit written to or read from the register. i.e., LSB first.
2. Reserved
3. See Table 26 for definition of the faults.

Table 34 Control Register Bit Definitions

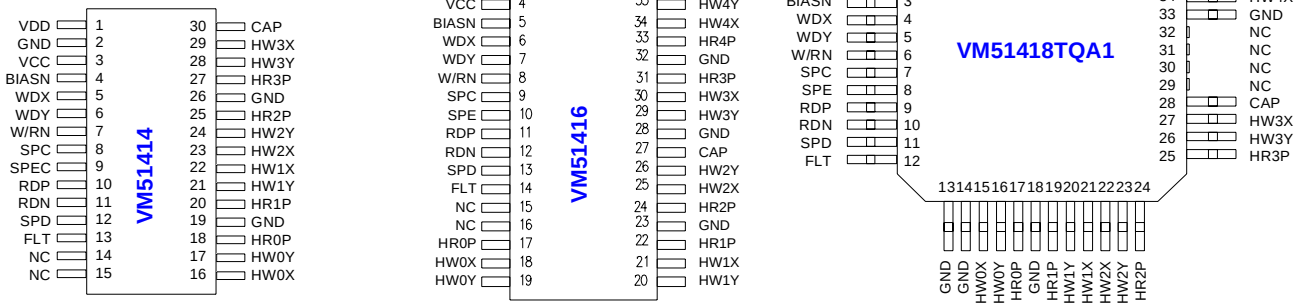
Register/ Bits	*Bit Name*	*Functional Description*
0:<D0-D2>	VEN<0:2>	Vendor ID of device (read only).
0:<D3-D6>	REV<0:3>	Revision level of device (read only).
0:<D7>	CCI	Channel count indicator (read only): 0 indicates 6-channel, 1 indicates 4-channel (VM51414VSD1 only).
1:<D0-D2>	HS<0:2>	Head Select setting. See Table 25 on page 58 for further definition.
1:<D3-D7>	IMR<0:4>	MR head bias current DAC setting (0-31). See Read Mode on page 56 for further definition. In servo write mode, setting determines MR bias voltage as defined in (eq. 4) on page 57.
2:<D0-D4>	IW<0:4>	Write current DAC setting (0-31). See Write Mode on page 56 for further definition. In PLR mode, setting determines PLR amplitude as defined in (eq. 9) on page 66.
2:<D6>	LVDIS	Low VDD disable fault reporting; set to 1 to disable reporting.
4:<D5> 2:<D7>	SBW0 SBW1	Servo Bank Write enable; follow sequence in Servo Write Mode on page 57.
3:<D0-D6>	TA<0:7>	Thermal Asperity Detection DAC setting (1-127) or Digital Buffered Head Voltage DAC setting (7-127). See Detection on page 61 or MR Measurement / Digital Buffered Head Voltage (DBHV) on page 60 for further definition.
3:<D7>	TAC	Thermal Asperity Compensation enable; set to 1 to select.
4:<D0>	SLPB	Sleep mode enable; set to 0 to select.
4:<D1>	IDLEB	Idle mode enable; set to 0 to select.
4:<D2>	GAIN	Gain selection: set to 0 for low gain, set to 1 for high gain.
4:<D3>	MRM	Head Resistance Measurement (DBHV) mode enable; set to 1 to select. See Table 27.
4:<D4>	BOOST	Boost circuit enable; set to 1 to select.
4:<D6>	ABHV	Analog Buffered Head Voltage enable; set to 1 to output ABHV at FLT pin. See Table 27.
4:<D7>	TEMP	Temperature fault report enable; set to 1 to report a temperature fault to the HOT bit and the FLT pin. See Table 27.
5:<D1>	OSD	Write current overshoot direction of control; set to 0 to increase, set to 1 to decrease
5:<D2-D4>	OSC<0:3>	Write current overshoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 62 for further definition.
5:<D5-D7>	USC<0:3>	Write current undershoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 62 for further definition.
6:<D0>	HOT	Bit is set to 1 if the HOT fault occurs. [1]
6:<D1>	LOVDD	Bit is set to 1 if the Low VDD fault occurs. 1
6:<D2>	MROP	Bit is set to 1 if an MR Open head fault occurs. 1
6:<D3>	MRSH	Bit is set to 1 if an MR Shorted head fault occurs. 1
6:<D4> 6:<D5>	WROP WRSH	Bits are set to 1 if a Writer Open head or Head Shorted to ground fault occurs. 1
6:<D6>	LOFR	Bit is set to 1 if the Write data frequency too low fault occurs. 1
7:<D0-D1>	PLRDT	PLR Delay Time. See Table 31.

Table 34 Control Register Bit Definitions

7:<D2-D3>	PLRPW	PLR Pulse Width. See Table 30.
7:<D4>	PLREN	PLR Enable, set to 1 enable PLR mode.
7:<D5>	OSDLY	Additional Write Current Overshoot Control, set to 1 to select.
7:<D6>	TOSC	Manufacturer Test Bit; set to 0 for normal operation.
7:<D7>	DUALTA	Dual Direction TA Detection (positive *and* negative), set to 1 to select.

1. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to ‘0’.

PIN DESCRIPTION AND FUNCTION LIST



4-Channel
30-lead VSOP (TSSOP)

6-CHANNEL
38VSOP (TSSOP)

8-CHANNEL
48TQFP

Figure 38 Pin Layouts

Table 35 Pin Functions

Signal	*I/O* [1]	*Description*
W/RN	I	Write/Read: Low voltage CMOS input. Internal pull-down resistor (50kΩ). • A high level enables Write mode. • Pin defaults low (Read mode).
BIASN	I	Bias Enable and PLR trigger: Low voltage CMOS input. Internal pull-up resistor (20kΩ) to V_{CC}. • A high level deactivates the MR bias current and the MR control loop, while maintaining the MR threshold levels. Pin defaults high. • A low level enables MR bias current to the selected head. If PLREN = 1 (7:<D4>), a high to low transition triggers the PLR pulse (V_{MR}). See the PLR Timing and Event Description on page 66.
FLT	O	Fault Status: Open drain output. Requires external pull-up resistor (e.g., 2kΩ to 3V). • In Write mode, a high level indicates a fault. • In Read mode, a low level indicates a fault. • Measurements modes are shown in Table 27 on page 59.
WDX, WDY	I	2V ±100mV write data inputs.
HR0P-HR7P	I	MR head connections, positive end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end.
RDP, RDN	O	Read Data: Differential read signal outputs.
CAP	-	Compensation capacitor (22nF) for the MR bias current loop.
GND	-	Ground and common return for MR heads
VCC	-	+5.0V supply
VDD	-	+8.0V supply

Table 35 Pin Functions

Signal	*I/O* [1]	*Description*
SPE	I	Serial Enable: Low voltage CMOS input; see Figures 37 and 39.
SPC	I	Serial Clock: Low voltage CMOS input; see Figures 37 and 39.
SPD	I/O	Serial Data: Low voltage CMOS input/output; see Figures 37 and 39. Requires external pull-up resistor (e.g., 1kΩ to 3V).

1. I = Input pin, O = Output pin.

POWER CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR}=8 mA, I_W=40.0 mA, I_S=25mA.
Power supply currents for other settings can be calculated using the formulas below.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		7.2	8	8.8	V
V_{DD} Power Supply Current	I_{DD}	Read Mode (See Formula 1 below.)		27	31	mA
		Read Mode, Bias disabled (See Formula 2 below.)		16	20	
		Write Mode (See Formula 3 below.)		72	82	
		Write Mode, Bias enabled (See Formula 4 below.)		83	93	
		Idle Mode		14	16	
		Sleep Mode		0.17	1	
		Servo Write Mode, Six heads, VDD=5V, I_S=25mA (See Formula 5 below.)		224	250	
		Servo Write Mode with Bias, Six heads, VDD=5V, I_S=25mA, V_{MR} = 181mV, R_{MR} = 45.3Ω. (See Formula 6 below.)		251	282	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
V_{CC} Power Supply Current	I_{CC}	Read Mode (See Formula 7 below.)		45	56	mA
		Read Mode, Bias disabled (See Formula 8 below.)		29	35	
		Write Mode (See Formula 9 below.)		41	50	
		Write Mode, Bias enabled (See Formula 10 below.)		44	52	
		Idle Mode		20	23	
		Sleep Mode		0.6	3	
		Servo Write Mode, Six heads, VDD=5V, I_S=25mA (See Formula 11 below.)		55	64	
		Servo Write Mode with Bias, Six heads, VDD=5V, I_S=25mA, V_{MR} = 181mV, R_{MR} = 45.3Ω. (See Formula 11 below.)		55	64	

POWER CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR}=8 mA, I_W=40.0 mA, I_S=25mA.
Power supply currents for other settings can be calculated using the formulas below.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Dissipation	P_d	Read Mode		451	581	mW
		Read Mode, Bias disabled		273	369	
		Write Mode		781	997	
		Write Mode, Bias enabled		884	1104	
		Idle Mode		212	267	
		Sleep Mode		4	25	
		Servo Write Mode, Six heads, VDD=5V, I_S=25mA		1395	1727	
		Servo Write Mode with Bias, Six heads, VDD=5V, I_S=25mA, V_{MR} = 181mV, R_{MR} = 45.3Ω.		1530	1903	

1. IDD(Typ): 15 + (0.043 * I_W) + (1.26 * I_{MR}) — IDD(Max): 18 + (0.046 * I_W) + (1.32 * I_{MR})
2. IDD(Typ): 14 + (0.043 * I_W) — IDD(Max): 16.8 + (0.046 * I_W)
3. IDD(Typ): 29 + (1.06 * I_W) — IDD(Max): 34.8 + (1.145 * I_W)
4. IDD(Typ): 31 + (1.06 * I_W) + (1.26 * I_{MR}) — IDD(Max): 37.2 + (1.145 * I_W) + (1.34 * I_{MR})
5. IDD(Typ): 9.5 + (9.5 + [1.04 * I_S]) * Hds — IDD(Max): 11.4 + (11.4 + [1.12 * I_S]) * Hds
6. IDD(Typ): 9.5 + (9.5 + [1.04 * I_S] + [1.0 * V_{MR}/R_{MR}]) * Hds — IDD(Max): 11.4 + (11.4 + [1.12 * I_S] + [1.2 * V_{MR}/R_{MR}]) * Hds
7. ICC(Typ): 40 + (0.090 * I_W) + (0.17 * I_{MR}) — ICC(Max): 48 + (0.097 * I_W) + (0.18 * I_{MR})
8. ICC(Typ): 25 + (0.09 * I_W) — ICC(Max): 30 + (0.97 * I_W)
9. ICC(Typ): 33 + (0.19 * I_W) — ICC(Max): 39.6 + (0.205 * I_W)
10. ICC(Typ): 35 + (0.19 * I_W) + (0.17 * I_{MR}) — ICC(Max): 42 + (0.205 * I_W) + (0.18 * I_{MR})
11. ICC(Typ): 23.0 + (2.0 + [0.13 * I_S]) * Hds — ICC(Max): 27.6 + (2.4 + [0.14 * I_S]) * Hds

I/O CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}	Applies to W/RN, BIASN, SPE, SPC, SPD pins	1.5		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	Applies to W/RN, BIASN, SPE, SPC, SPD pins	-0.3		0.7	V
Input High Current	I_{IH}	Applies to SPE, SPC, SPD pins	-1		1	µA
Input Low Current	I_{IL}	Applies to SPE, SPC, SPD pins	-1		1	µA
BIASN Internal Pullup Resistor	R_{pu}	Pullup to V_{CC}	16	20	24	KΩ
W/RN Pin Internal Pulldown Resistor	R_{pd}		40	50	60	KΩ
Input Signal Rise/Fall Time	t_{ir}/t_{if}	Applies to W/RN, BIASN, SPE, SPC, SPD pins			10	ns
Input Hysteresis	V_{ihys}	Applies to W/RN, BIASN, SPE, SPC, SPD pins	200			mV
Output High Current	I_{OH}	V_{OH}=3.6V, applies to FLT, SPD			1	µA
Output Low Voltage	V_{OL}	FLT I_{OL}=3mA			0.3	V
		SPD I_{OL}=5mA			0.3	
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400			mV_{ppd}
WDX/WDY Differential Input Voltage	V_{DIFF}	Read Mode	100			mV_{diff}
		Idle Mode	0			mV_{diff}
WDX/WDY Common Mode Source Voltage	V_{CMW}		1.4	2	2.6	V
WDX/WDY Differential Input Impedance	Z_{ID}		100	125	150	Ω
WDX/WDY Input Rise/Fall Time	t_{WR}/t_{WF}	80% of V_{DIFF} into CL=20pF		0.9	1.05	ns
RDP/RDN Common Mode Output Voltage	V_{OCM}	Read Mode, Write Mode, BIASN = L		V_{CC} - 2.5		V
RDP/RDN Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE), BIASN = L	-150		150	mV
RDP/RDN Single-Ended Output Resistance	R_{SEO}	Read Mode		30	40	Ω
RDP/RDN Output Current	I_O	Source or sink	4			mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		2	7	9.75	mA
MR Head Current Accuracy	ΔI_{MR}	2mA < I_{MR} < 9.75mA	-5		5	%
Unselected MR Head Current (in Idle or Read with Bias Modes)		Applicable 10 µs after head switch			50	µA
Differential Voltage Gain	A_V	V_{IN}=1mV_{pp} @80MHz, R_L(RDP, RDN)=2kΩ, Gain bit=0	170	195	220	V/V
		Gain bit=1	233	265	303	
Gain Deviation Head-to-Head					3	%
Gain Boost	BOOST	f=80MHz, Gain bit=0, Boost bit=1		3		dB
Passband Upper Frequency Limit	f_{HR}	L_{MR}=20nH, -3dB, Gain bit=0	270	320		MHz
		-1dB, Gain bit=0	170			
Passband Lower -3dB Frequency Limit	f_{LR}	Gain bit=0	0.15	0.5	0.8	MHz
Equivalent Input Noise (total)	e_n	1 < f < 85 MHz		0.6		nV/√Hz
Integrated Noise	e_{in}	L_{MR}=20nH; 1 < f < 140 MHz		8.1		µV
Total Harmonic Distortion (and Dynamic Range)	THD	V_{IN}=1mV_{pp}, f=20 MHz		60		dB
	DR	V_{IN}=1mV_{pp}, f=60 MHz	40			
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{DD}, 1 < f < 100 MHz	32			dB
		100 < f < 170 MHz	32			
Channel Separation	CS	Unselected Channels: V_{IN}=100mV_{pp}, 15 < f < 40 MHz	68			dB
		40 < f < 170 MHz	54			
Noise Rejection Any I/O to RDP/RDN	NR	100 mV_{PP} on I/O, 1 < f < 225 MHz	50			dB
Output Offset Voltage	V_{OS}	Low or High Gain	-50		50	mV
Output Offset Voltage Deviation Across Heads	ΔV_{OS}				50	mV
DBHV Threshold (MR Head Resistance measurement)	V_{BHV}	Programmable	42		762	mV
Buffered Head Voltage Gain	A_{BHV}		4.6	5	5.25	V/V
Thermal Asperity Detection Range	V_{TATH}	DC level in RDX/RDY over base-line	6		762	mV_{bp}

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Asperity Detection/ DBHV Threshold Tolerance	ΔV_{TATH}	Threshold 192 to 762 mV	-(10% + 3mV)		10% +3mV	mV
		Threshold 96 to 186 mV	-(20% + 7mV)		10% +6mV	
		Threshold 42 to 90 mV	-(35% + 10mV)		10% +6mV	
MR Head Voltage	V_{MR}	$I_{MR} \cdot R_{MR}$	100		900	mV
Overshoot on I_{MR} during Mode Transitions: Idle-to-Read, Write-to-Read, Head-to-Head and Bias Off-to-On	I_{MROV}	0.1V < V_{MR} < 0.9V Percent of final I_{MR}			2	%
Undershoot on I_{MR} during Mode Transitions	I_{MRUS}				0	mA

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(base to peak)	15		59.95	mA
Write Current Tolerance	ΔI_W	15mA < I_W < 59.95mA	-8		8	%
Differential Head Voltage Swing	V_{DH}	Open Head, V_{DD}=7.2V	10.8	14		V_{ppd}
Unselected Head Current	I_{UH}				50	μA_{pk}
WDX/WDY Input Frequency Range	f_W		5		160	MHz
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		6	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time			50	ps
Rise/Fall Time	t_r / t_f	10 - 90%		0.8	1.3	ns

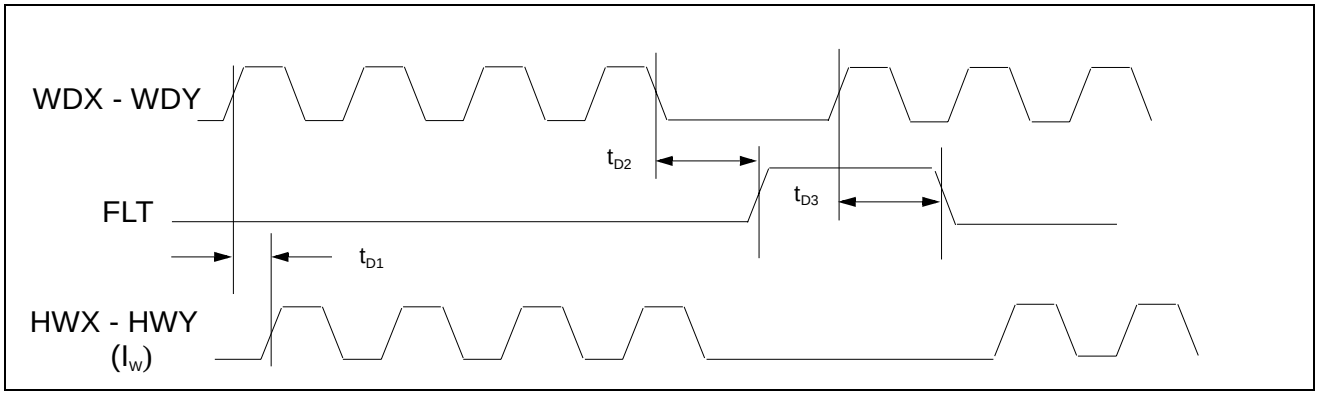


Figure 39 Write Mode Timing Diagram

Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX > WDY current flows into the “Y” port, for WDX < WDY current flows into the “X” port.

SERVO WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply	V_{CC}		4.5	5	5.5	V
	V_{DD}	LVDIS bit = 1	5		5.5	
	V_{DD}	LVDIS bit = 0	7.2		8.8	
Servo Current Range	I_S	base to peak, 6 heads	15		40	mA
		base to peak, 3 heads	15		59.95	
Servo Current Tolerance	ΔI_S	V_{DD} = 5 V: 14.5mA < I_S < 57.9mA V_{DD} = 8 V: 15mA < I_S < 59.95mA	-8		8	%
MR Head Voltage	V_{MR}	Programmable, 6 Heads, I_S = 15mA	36		237.5	mV
MR Head Voltage Accuracy	ΔV_{MR}	I_S = 15mA, Heads = 6				%
		V_{MR} = 36 to 55.5 mV	-45		80	
		V_{MR} = 62 to 81.5 mV	-40		60	
		V_{MR} = 88 to 133.5 mV	-35		35	
		V_{MR} = 140 to 237.5 mV	-30		25	
Read to Write Mode	t_{RW}	To 90% of servo write current		15	50	ns
Read to Write Difference between Heads		To 90% of servo write current for each head		1.5		ns

LOW V_{DD} OPERATION CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA, V_{DD}=5V, LVDIS=1.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Rise/Fall Time	t_{rs}/t_{fs}	10-90%		1.75		ns
Differential Head Voltage Swing	V_{DH}	Open Head, V_{DD}=5.0V	5	8		V_{ppd}
MR Head Current Accuracy	ΔI_{MR}	2mA < IMR < 9.75mA	5		5	%
Differential Voltage Gain	A_V	VIN=1mVpp @80MHz, R_L(RDP, RDN)=2kΩ, Gain bit=0		100		V/V
		Gain bit = 1		130		

PINNED LAYER REVERSAL CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PLR Pulse Amplitude	V_{RESET}	Referenced to ground Value set in I_W DAC (2:<D0-D4>). See (eq. 9).	0.4		1.64	V
PLR Pulse Width	t_{PW}	Value set in 7:<D2-D3>. See Table 30	50		200	ns
PLR Pulse Decay Rate	d_V/d_t	Value set in 7:<D0-D1>. See Table 31	1.75		7	mV/ns
PLR Pulse Setup Time	t_{ARM}		500			ns
PLR Pulse Delivery Time	t_{EN}		1200			ns
PLR Pulse Amplitude Accuracy	ΔV_{RESET}	$0 \leq \Delta V_{RESET} \leq 1$	-20		20	%
		$1 < \Delta V_{RESET}$	-25		25	%
PLR Pulse Width Accuracy	t_{PW}	50 ns $\leq t_{PW} \leq$ 200 ns	-20		20	%
PLR Pulse Decay Rate Accuracy	$\Delta d_V/d_t$	1.75 mV/ns $< d_V/d_t \leq$ 7 mV/ms	-20		20	%

MODE SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		43	50	ns
Write to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value or 90% of read envelope [1]		180	300	ns
Idle to Read Mode [2,3]	t_{IR}	RDP/RDN to within ±30mV of final value or 90% of read envelope		6	10	µs
Read Mode, Head Select to Any Head, I_{MR} switch [2]	t_{HS}	RDP/RDN to within ±30mV of final value, or 90% of read envelope, or 90% of I_{MR}		6	10	µs
Idle Mode Powerup Time (from Sleep Mode)				300		µs
Read to Idle [2]	t_{RI}	To 10% of read envelope		0.16	0.5	µs
Write to Idle [2]	t_{WI}	To 10% of write current		27	50	ns
Read Bias Disabled to Bias Enabled	t_{RB}	BIASN pin high to low to 90% of I_{MR}			10	µs

1. BIASN pin low for 10µs preceding W/RN transition.
2. Timing for mode change, which is initiated in serial register, is measured from SPE high to low edge.
3. Sleep to Read mode change transitions through Idle mode and must remain in Idle mode for a minimum of 300µs.

FAULT CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fault Threshold	VCC_{DTH}	I_w < 350µA, Fault detected	3.6	3.8	4.0	V
	VCC_{UTH}	Fault removed	3.9	4.1	4.3	
V_{CC} Fault Threshold Hysteresis	VCC_{HTH}		200	300	400	mV
V_{DD} Fault Threshold	VDD_{DTH}	I_w < 350µA, Fault detected	5.8	6.1	6.4	V
	VDD_{UTH}	Fault removed	6.3	6.6	6.9	
V_{DD} Fault Threshold Hysteresis	VDD_{HTH}		400	500	600	mV
Threshold for Open MR Head Fault Detection			0.95	1.1	1.3	V
Threshold for MR Head Shorted to GND Fault Detection				50		mV
Open MR Head Delay		From Head Switch to Open MR Head reported (SPE goes low to FLT pin low)		10	20	µs
Writer Open/Shorted Head Detection Threshold	V_{OSHD}	ΔV across write element at next WDX/WDY transition, where $\Delta V = R_{OpenHead} * I_W$ OR Head resistance to GND <15Ω.			2.5	V
Open/Shorted Write Head Blanking Time	t_{OS}			7 [1]		ns
FLT delay, Write Safe to Unsafe [2]	t_{D2}	Fault Safe guaranteed for write data transitions <500ns apart.	0.5	1.5	3.6	µs
FLT delay, Write Unsafe to Safe [2]	t_{D3}				1.1	µs
TA FLT Delay [3]	t_{D4}	TA detected to FLT pin low		30	100	ns
TA FLT Pulse Width [3]	t_{D5}		1	1.5	2	µs
Temperature Threshold for Hot Fault	T_{HOT}			135		°C

1. Will not detect or report fault for write current transitions less than 7ns apart.
2. See Figure 39 on page 79.
3. See Figure 29 on page 61.

VTC Inc.
Value The Customer™

VM5430

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 500 Mbits/sec
  - Designed for Use With Four-Terminal GMR Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 8 Channels Available
  - Fault Detect Capability
  - Servo Bank Write Capability
- *High Performance Reader*
  - Current or Voltage Bias / Voltage Sense Configuration
  - Reader Bias Current/Voltage 6-bit DAC, 2 -10 mA Range
  - Programmable Read Voltage Gain (100 V/V to 250 V/V Typical)
  - Input Noise Voltage = 0.55 $nV/\sqrt{Hz}$ Typical
  - Input Noise Current = 8 $pA/\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Programmable Bandwidths to 350 MHz Typical
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 65 mA Range
  - Rise Time 500 pS Typical (10-90%, I_W = 50 mA, L_{total} = 70 nH, R = 10Ω)

DESCRIPTION

The VM5430 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM5430 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

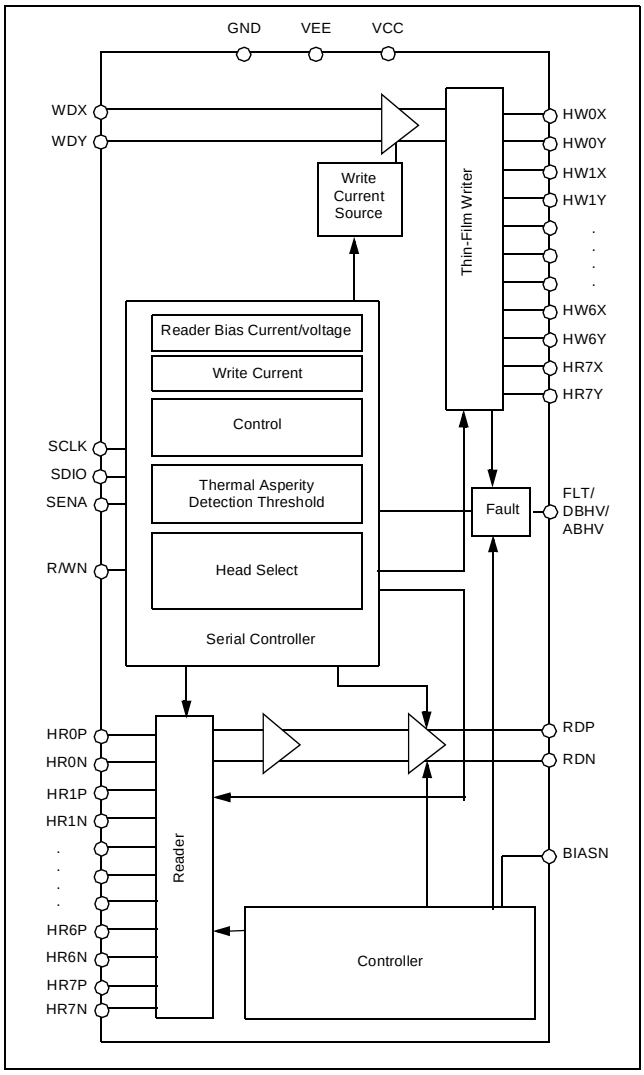
Programmability of the VM5430 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, write current overshoot and undershoot, fault modes, thermal asperity detection and threshold, and dynamic thermal asperity compensation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM5430 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. The device also provides power saving idle and sleep modes.

The VM5430 is available in a 48-pin TQFP package or bump die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR} ..... 18 mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -5V ± 10%

Write Current, I_W ..... 15 - 65 mA
Write Head Inductance, L_W ..... 70 nH
Write Head Resistance, R_W ..... 8 - 16 Ω
Read Bias:
- Current, I_{MR} ..... 2 - 10 mA
- Voltage, V_{MR} ..... 100 - 500 mV

Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM5430 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 87 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

All control lines on the VM5430 may be shared, including the serial lines SCLK, SDIO and SENA. Default settings are listed in Table 43 on page 93.

OPERATING MODES

Pin and register combinations select read/write, servo track write or mode operations as shown in Table 36.

Table 36 Mode Select

Pin		*Register:Bit*				
R/WN pin 5>	*BIASN pin 13>*	*SLEEPN 4:<D0>*	*IDLEN 4:<D1>*	*BANK1 4:<D6>*	*BANK0 2:<D7>*	*Operational Mode*
X	X	0	X	X	X	Sleep
X	X	1	0	X	X	Idle
0	0	1	1	0	0	Write Bias Active
0	1	1	1	0	0	Write
0	X	1	1	1	1	Servo Write
1	0	1	1	0	0	Read Bias Active
1	1	1	1	0	0	Read

Note: Two or more independent failures are required to cause an illegal chip selection, in which case the FLT pin is asserted and an error code is generated.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature or buffered head voltage.

Read Head Resistance

The resistance of the MR head can be measured in three ways: an automatic digital conversion, an iterative method using DBHV and threshold settings to trigger or not trigger a fault, or by monitoring the ABHV output.

Digital Conversion

To perform digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 36).
2) Set the RMR/TEMP bit (9:<D0>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)
4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 7:<D6-D0> = 0010000 the MR head resistance is 16 Ohms. (The measurement range for MR resistance is 0 - 127 Ω.)

Note: MR bias current is always enabled in this mode.

Iterative Resistance Reading

To perform the iterative resistance reading:

1) Place device in Read Mode (see Table 36).
2) Set the DBHV bit (4:<D3>) high to enter the MR resistance measurement mode.
3) Monitor the FLT/ABHV/DBHV pin to determine the voltage across the MR element:
   - A high indicates the voltage is within the window (150mv to 320mv).
   - A low indicates the voltage is outside the window.
4) Vary the MR bias current (9:<D2> and 1:<D3-D7>) to determine where the defined thresholds are crossed. The FLT line is not valid until the I_{MR} change settles; values for this are listed in SWITCHING CHARACTERISTICS on page 101.
5) Resistance can be inferred from the threshold settings.

Buffered Head Voltage

To output the MR head voltage on the FLT/ABHV/DBHV pin:

1) Place device in Read Mode (see Table 36).
2) Set ABHV bit (9:<D7>) high to output the MR head voltage as scaled by a gain of 5.

Note: If ABHV and DBHV are both high, ABHV takes precedence. See the truth table in PIN FUNCTION LIST AND DESCRIPTION on page 95.

Die Temperature Monitoring

The die temperature range is 0°C to 150°C. To measure the die temperature:

1) Set RMR/TEMP (9:<D7>) high to enable the die temperature.
2) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 7:<D6-D0> = 0100000 the die temperature is 38°C (32°C x 1.18).

$$T = 1.18k \qquad \textit{(eq. 10)}$$

where k = 0 - 127 and T is degrees Centigrade

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Sleep Mode

In the sleep mode power consumption is minimized. All outputs are disabled (except in test mode). The writer current source and the reader bias current/voltage source are deactivated and faults are not detected in Sleep Mode.

Sleep mode is selected by setting 4:<D0> = 0, see Tables 36, 40 and 42.

Note: Always transition from Sleep to Idle mode 10 µs before entering an active mode.

Idle Mode

The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN and RDP outputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. Faults are not detected in Idle Mode.

Idle mode is triggered by setting 4:<D1> = 0, see Tables 36, 40 and 42.

Dummy Mode

Setting DUMMY (9:<D1>) high directs the MR bias current/voltage to an internal dummy head. This maintains the reader bias at operational levels for quick read recovery.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting the R/WN pin high. In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM5430 uses the voltage-sensing reader architecture with biasing programmable as current or voltage. The magnitude of the reader bias current/voltage is set to the value programmed in 9:<D2> and 1:<D3-D7>. The equations below govern the read bias current/voltage magnitude:

$$\text{Current Mode} \quad I_{MR} = 2 + [k_{IMR} \cdot 0.127]\text{mA} \qquad \textit{(eq. 11)}$$

$$\text{Voltage Mode} \quad V_{MR} = 100 + [k_{IMR} \cdot 6.35]\text{mV} \qquad \textit{(eq. 12)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes:

- Current bias mode is selected by setting 9:<D4> = 0, and
- Voltage bias mode is selected by setting 9:<D4> = 1.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element. The applied value is programmed in 9:<D2> and 1:<D3-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

The reader enters a fast recovery mode during modal transitions, serial operations, and when the reader is biased during a write mode. The fast recovery mode minimizes signal anomalies on the reader outputs.

Read Bias Enable in Read Mode

Reader bias is controlled in the read mode by the BIASN pin. Taking the BIASN pin high in read mode disables the current to the selected read head.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 44.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 6:<D6-D0> as shown in Table 45. The default setting (0000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 43). The following are valid read fault conditions:

- MR Overcurrent
- Thermal Asperity Detected
- Read Head Open
- Read Head Shorted
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Read Gain

The default gain is 100 V/V with a head resistance of 55Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in 4:<D2 and 9:<D3>. The formula that describes the actual gain is shown below:

$$\text{GAIN} = \frac{475}{420 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 13)}$$

k_{GAIN} = 0-3

Fast Mode

Setting the FAST bit (4:<D5>) high in read mode, raises the low corner frequency to 5MHz. If the FAST bit is low, the low corner frequency is set to the value programmed in LFP (5:<D4-D5>).

Thermal Asperity Detection and Recovery

Detection

Setting the TAD bit high (3:<D3>) enables positive or negative thermal asperity detection.

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the voltage threshold is governed by the following equation and is set in 9:<D6> and 3:<D4-D7>:

$$V_{TAT} = 50 + \left[900 \times \left(\frac{k_{TAT}}{31}\right)\right] \qquad \textit{(eq. 14)}$$

V_{TAT} represents the TA threshold (output-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

Fast Recovery

Setting the TA Compensation (TAC) bit high (9:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised to 5MHz from the nominal value programmed in 5:<D4-D5>. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 3:<D3>.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting the R/WN pin low.

The magnitude of the write current is determined by the write current registers (2:<D0-D4>). The following equation governs the write current magnitude:

$$I_W = 15 + (k_{IW} \cdot 1.61)\,mA \qquad \textit{(eq. 15)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 43 for the timing diagram.

Write Current DAC

Register 2:<D0-D4> represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIASN pin low (at least 5µs before the R/WN pin is set high) enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (5:<D3>) initiates Write Data Inputs in Voltage Mode. Setting the WVORI bit high initiates the Write Data Inputs in Current Mode.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 44.

Specific fault conditions may be disabled by setting the Fault Reporting Mask, 6:<D0-D6> as shown in Table 45. The default setting (000000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 43).

The following are valid write fault conditions:

- Write Data Frequency Low
- Open or Shorted Write Head
- Servo Fault
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Servo Write Mode

In the servo write mode, up to eight channels may be written simultaneously.

Table 42 indicates how heads can be selected for individual or simultaneous writing.

Setting both BANK bits (2:<D7> and 4:<D6>) to ‘1’ and holding the R/WN pin low places the preamp in servo write mode (see Table 36). A high in SHDn (8:<D0> to 8:<D3> selects the specific head pair on which to perform the servo write. The default setting is to select all heads (8:<D0-D3> = 1111).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

A servo fault is generated if BANK bit (2:<D7> or 4:<D6>) settings do not match as shown in Table 37.

Table 37 Servo Faults

BANK1 4:<D6>	*BANK 0 2:<D7>*	*Mode*	*Fault*
0	0	Active [1]	No
0	1	Active [1]	Yes
1	0	Active [1]	Yes
1	1	Servo	No

1. Active includes all modes (read, write, idle, sleep or test), except servo.

SERIAL PORT

Serial Interface

The VM5430 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 39 and 40 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 40.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one command bit <A0> (high for read, low for write),
  - three chip select bits <A3-A1> that validate the preamplifier address logic levels in Table 39, and
  - four register address bits <A7-A4>.
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode. The reader invokes a *fast* mode while a serial interface operation occurs.

See Tables 39 and 40 for a bit description. See Table 38, and Figures 41 and 42 for serial interface timing information.

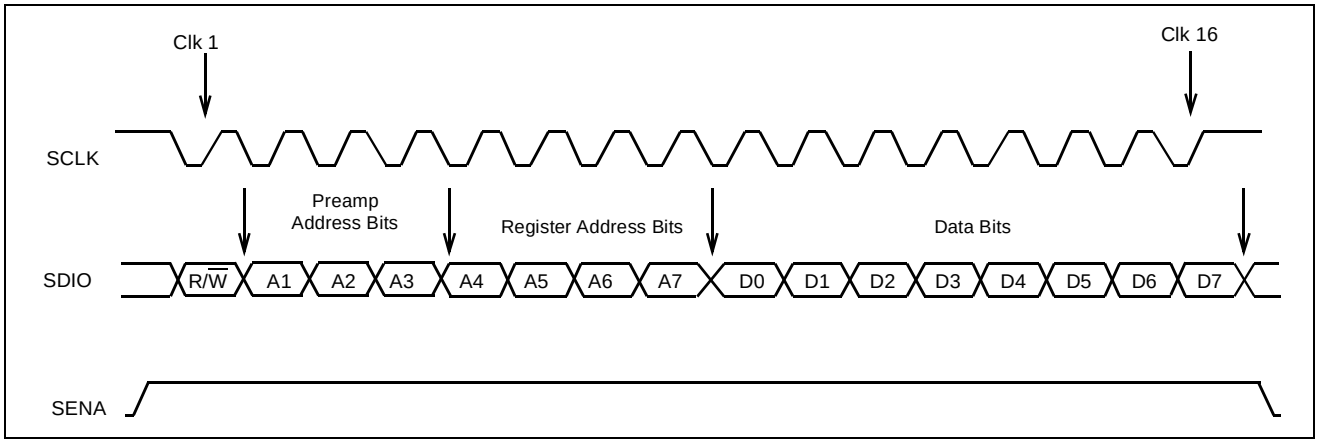


Figure 40 Serial Port Protocol

Table 38 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) rate, write				40	MHz
SENA to SCLK delay	T_{sens}	**TBD**			nS
SDIO setup time, write	T_{wds}	**TBD**			nS
SDIO delay time, read	T_{rds}	**TBD**		**TBD**	nS
SDIO hold time	T_{dh}	**TBD**			nS
SCLK cycle time	T_{c}	**TBD**			nS
SCLK high time	T_{ckh}	**TBD**			nS
SCLK low time	T_{ckl}	**TBD**			nS
SENA hold time	T_{shld}	**TBD**			nS
Time between I/O operations	T_{sl}	**TBD**			nS
Time from controller releasing SDIO (tristate) to SCLK falling edge	T_{tric}	**TBD**			nS
Time to activate SDIO	T_{act}	**TBD**		**TBD**	nS
Duration of SerEna (read)	T_{rd}	**TBD**			nS
Duration of SerEna (write)	T_{wt}	**TBD**			nS

Note: SENA assertion level is high.

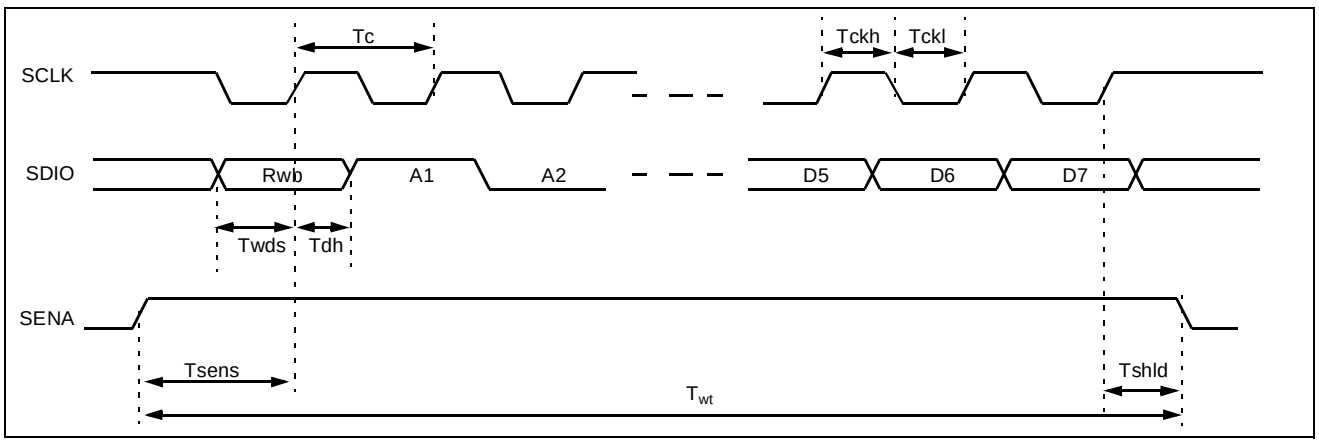


Figure 41 Serial Port Timing - Write Operation

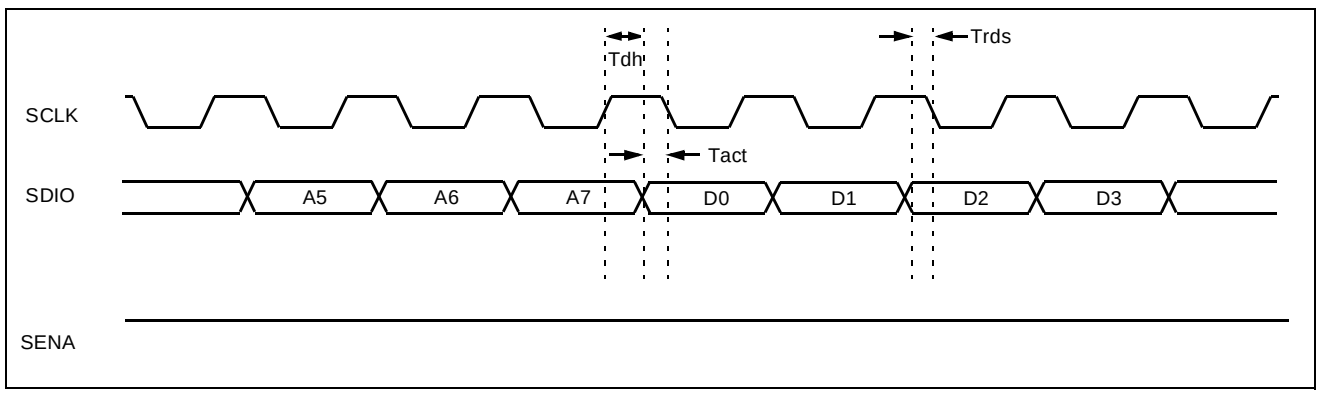


Figure 42 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 39 lists the serial address for each register. Table 40 lists the data contents of the basic register set and Table 41 lists register selections available as options. A description of the individual bits is provided in Table 42.

Table 39 Serial Interface Addressing

Register #	Register Address Bits				Preamp Address Bits			R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	0	0	0	0	0	0	1	0 = write 1 = read
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				

Table 40 Serial Interface Bit Map - Base Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Vendor ID	0 [1]	VEND0	VEND1	VEND2	REV0	REV1	REV2	CHNL	[2]
Head Select/IMR	1	HS0	HS1	HS2 [3]	IMR1	IMR2	IMR3	IMR4	IMR5
Write Current	2	IW0	IW1	IW2	IW3	IW4	[2]	[2]	BANK0
Thermal Asperity	3	OSC0	OSC1	OSC2	TAD	TA1	TA2	TA3	TA4
Mode Select	4	SLEEPN	IDLEN	GAIN0	DBHV	[2]	FAST	BANK1	[2]

1. Read Only Register/Bits:
   Register 0:<D0-D2> is the Vendor ID code (VTC=010),
   Register 0:<D3-D5> is the Vendor revision code. Initial revision shall be (REV0 = 0, REV1 = 0, REV2 = 0),
   Register 0:<D6> is the Channel count (0 = 8 channel, 1 = 4 channel),
2. Reserved.
3. Use restricted to 8-channel device.

Table 41 Serial Interface Bit Map - Optional Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Bandwidth/Under-shoot	5	USC0	USC1	USC2	WVORI	LFP0	LFP1	BW0	BW1
Fault	6	FLT0	FLT1	FLT2	FLT3	FLT4	FLT5	FLT6	CLRFC
Resistance/Temp	7	DSTR0	DSTR1	DSTR2	DSTR3	DSTR4	DSTR5	DSTR6	DIGON
Servo	8	SHD1/0	SHD3/2	SHD5/4	SHD7/6	FCODE0	FCODE1	FCODE2	FCODE3
Other	9	RMR/ TEMP	DUMMY	IMR0	GAIN1	I/V	TAC	TA0	ABHV
VTC Test	10	TTOSC	[1]	[1]	GMCTL	GMCTL	GMCTL	GMCTL	[1]

1. Reserved for VTC testing.

Table 42 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
0	D0-D2	Vendor Code	VENDn	Binary Vendor Code (010 = VTC)			
	D3-D5	Revision of Part	REVn	Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1after exceeding 8.			
	D6	Channel Count	CHNL	0 = 8 Channel device 1 = 4 Channel device			
	D7	Reserved					
1	D0-D2	Head Select	HSn	Binary selection of head	HS2	HS1	HS0
				Head Select	0:<D2>	0:<D1>	0:<D0>
				0	0	0	0
				1	0	0	1
				2	0	1	0
				3	0	1	1
				4	1	0	0
				5	1	0	1
				6	1	1	0
				7	1	1	1
				Note: Use of HS2 (0:<D2>) is restricted to 8-channel device.			
	D3-D7	Bias Level - MSB	IMRn	Binary selection of MR Head Bias - 5 most significant bits Current Bias = 2mA (00000) to 9.87mA (11111) in 0.254mA increments. Voltage Bias = 100mV (00000) to 494mV (11111) in 12.7mV increments. Note: The 5 most significant bits independently function as the I_{MR} or V_{MR} setting. The least significant bit of IMR DAC (9:<D2>)doubles the bias level resolution set by these bits. Note: Current or Voltage Bias is selected in 9:<D4>.			
2	D0-D4	Write Current	IWn	Binary selection of Write Current 15 mA (00000) to 65 mA (11111) in 1.6 mA increments.			
	D5-D6	Reserved					
	D7	Servo Bank 0	BANK0	0/1 = See Table 37, “Servo Faults,” on page 86 Note: BANK1 (4:<D6>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 43).			
3	D0-D2	Overshoot Control	OSCn	Overshoot Control **TBD** % 000) to **TBD** % (111) in **TBD** % increments.			
	D3	Thermal Asperity Detection	TAD	0 = TA Detection disabled. 1 = TA Detection enabled.			
	D4-D7	Thermal Asperity Threshold - MSB	TAn	Binary selection of Thermal Asperity Threshold - 4 most significant bits TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Least significant bit of thermal asperity (TA0) is stored in 9:<D6>.			

Table 42 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
4	D0	Sleep	SLEEPN	0/1 = See Table 36, “Mode Select,” on page 84 Note: This bit has precedence over the IDLEN bit (4:<D1>).		
	D1	Idle Mode	IDLEN	0/1 = See Table 36, “Mode Select,” on page 84 Note: The SLEEPN bit (4:<D0>) has precedence over this bit.		
	D2	Gain - LSB	GAIN0	Binary selection of MR Reader Gain least significant bit:	GAIN1	GAIN0
				Gain	9:<D3>	4:<D2>
				100 V/V	0	0
				150 V/V	0	1
				200 V/V	1	0
				250 V/V	1	1
				Note: Register 9:<D3> defines GAIN1 - MSB.		
	D3	Digital Buffered Head Voltage Output	DBHV	0 = Disable 1 = Enable Note: DBHV is overridden when ABHV (9:<D7>) is enabled.		
	D4	Reserved				
	D5	Fast Mode	FAST	Raises low corner frequency 5 MHz 0 = Disable 1 = Enable		
	D6	Servo Bank 1	BANK1	0/1 = See Table 37, “Servo Faults,” on page 86 Note: BANK0 (2:<D7>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 43).		
	D7	Reserved				
5	D0-D2	Undershoot Control	USCn	Undershoot Control **TBD** % (000) to **TBD** % (111) in **TBD** % increments.		
	D3	Write Voltage or Current	WVORI	0 = Voltage mode write data inputs. 1 = Current mode write data inputs.		
	D4-D5	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth:	LFP1	LFP0
				Low Frequency Bandwidth	5:<D5>	5:<D4>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				5 MHz	1	1
	D6-D7	Bandwidth	BWn	Binary selection of Bandwidth:	BW1	BW0
				Bandwidth	5:<D7>	5:<D6>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
6	D0-D6	Fault Mask	FLTn	Fault Reporting Mask See Table 45.		
	D7	Clear Fault Codes	CLRFC	0 = Retain faults 1 = Clear faults Note: CLRFC resets to 0 after fault codes clear.		

Table 42 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
7	D0-D6	MR Resistance or Die Temperature	DSTRn	Binary output (read only) of MR Head Resistance or Die Temperature: Resistance range is 0 to 127 Ohms. Temperature range is 0 to 150^{o}C. Note: 7:<D7> selects analog or digital output. Note: Register 9:<D0> selects resistance or temperature output.
	D7	Internal Digital Conversion	DIGON	0 = Analog-to-digital conversion off 1 = Start analog-to-digital conversion Note: DIGON resets to 0 when analog-to-digital conversion completes. Note: Reader Resistance or Die Temperature output is selected in 9:<D0> and the measurement is stored in 7:<D0-D6>.
8	D0-D3	Servo Head Select	SHDn	Binary selection of the head pairs to be servo track written. Examples: 1. 1000 = Servo Write Head Pair 6/7 [8 channel IC only (0:<D6> =0)]: 2. 0011 = Servo Write Head Pairs 0/1 and 2/3: - Bit 0 = 1 selects HD0/1 pair - Bit 1 = 1 selects HD2/3 pair - Bit 2 = 0 deselects HD4/5 pair - Bit 3 = 0 deselects HD6/7 pair Note: Default is to servo write all heads (see Table 43). Note: BANK0 and BANK1 (2:<D7> and 4:<D6>) must be selected to servo write.
	D4-D7	Fault Condition	FCODEn	Binary code of Fault(s) See Table 44.
9	D0	MR Head Resistance or Die Temperature	RMR/ TEMP	0 = MR Head Resistance stored in DSTRn register (7:<D0-D6>). 1 = Die Temperature stored in DSTRn register (7:<D0-D6>).
	D1	Dummy MR Head Load	DUMMY	0 = MR Head selected using HSn register (1:<D0-D2>) setting. 1 = Dummy head resistive load selected.
	D2	Bias Level - LSB	IMR0	Binary selection of MR Head Current Bias least significant bit Current Bias = 2mA (000000) to 10mA (111111) in 0.127mA increments. Voltage Bias = 100mV (000000) to 500mV (111111) in 6.35mV increments. Note: The 5 most significant bits of IMR DAC (IMR1 to IMR5) are stored in 1:<D3-D7> and independently function as the I_{MR} or V_{MR} setting. This bit (the LSB) functions as a I_{MR} or V_{MR} resolution doubling bit to the most significant bits (from 0.254mA or 12.7mV when only IMR1-IMR5 are used). Note: Current or Voltage Bias selected in 9:<D4>.
	D3	Gain - MSB	GAIN1	Binary selection of MR Reader Gain - most significant bits See register 4 bit 2 for an explanation of Reader Gain settings. Note: Register 4:<D2> defines GAIN0 - LSB.
	D4	Current or Voltage Bias	I/V	0 = Current bias mode. 1 = Voltage bias mode. Note: Bias level is set in registers 9:<D2> and 1:<D3-D7>
	D5	Thermal Asperity Compensation	TAC	0 = No TA Compensation. 1 = TA Compensation selected. Note: TA Detection must be enabled in 3:<D3> for TAC to function.
	D6	Thermal Asperity Threshold - LSB	TA0	Binary selection of Thermal Asperity Threshold - least significant bit TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Most significant bits of thermal asperity (TA1-TA4) are stored in 3:<D4-D7>.
	D7	Analog Buffered Head Voltage Output	ABHV	0 = Disable 1 = Enable Note: ABHV overrides DBHV (4:<D3>).

Table 42 Serial Register Data Bit Descriptions

Register	*Bits*	*Function*	*Symbol*	*Description*
10	D0	Reserved		
	D1		TTOSC	Reserved for VTC testing
	D2	Reserved		
	D3-D6		GMCTL	Reserved for VTC testing
	D7	Reserved		

Table 43 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Vendor ID	0	<XXXX XXXX>
Head Select/IMR	1	<0000 0000>
Write Current	2	<0000 0000>
Thermal Asperity	3	<0000 0100>
Mode Select	4	<0000 0000>
Bandwidth/Undershoot	5	<1100 0100>
Fault	6	<0000 0000>
Resistance/Temp	7	<0000 0000>
Servo	8	<XXXX 1111>
Other	9	<0000 0000>
VTC Test	10	<0000 0000>

Fault Reporting and Masking

Table 44 Fault Conditions and Codes

Fault Code 8:<D7-D4>	Fault	Priority [1]	Valid Mode(s)	Mask [2]	Conditions
0000	No Fault	–	Read or Write	–	
0001	Reserved	3	Read	–	
0010	MR Overcurrent	2	Read	M	
0011	Thermal Asperity Detected	6	Read	M	
0100	Read Head Open	7	Read	M [3]	
0101	Read Head Shorted	8	Read	M [3]	
0110	Write Data Frequency Low	5	Write	M	
0111	Write Head Open/Shorted	3	Write	M	
1000	Servo Fault	9	Read or Write		Unmatched servo bank bits
1001	Low V_{CC} or V_{EE}	1	Read or Write	M	
1010	Reserved	–	–	–	
1011	Overtemperature	10	Read or Write	M	Temp > 140^{o}C
1100	Invalid Head	4	Read or Write		Only applies to 6 or 12 channel devices
1101	Reserved	–	–	–	
1110	Reserved	–	–	–	
1111	Reserved	–	–	–	

1. First fault reported is latched until a higher priority fault is reported or the code is cleared.
2. See Table 45 for an explanation of fault masking.
3. Single bit masks both faults.

Setting the appropriate bit(s) listed in Table 45 masks the fault(s) at both the fault register and the FLT pin. If 6:<D7-D0> = 0000 0101, an MR Overcurrent fault is masked with the 6:<D0> bit and Read Head Open and Read Head Shorted faults are masked with the 6:<D2> bit.

Table 45 Fault Masking

Mask Bit Register 6	Fault(s) Masked [1]	Mask Bit Register 6	Masked Fault
<D0>	MR Overcurrent	<D4>	Write Head Open/Shorted
<D1>	Thermal Asperity Detected	<D5>	Low V_{CC} or V_{EE}
<D2>	Read Head Open/Shorted	<D6>	Overtemperature
<D3>	Write Data Frequency Low		

1. Single bit masks both Read Head Open and Read Head Shorted faults.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

PIN FUNCTION LIST AND DESCRIPTION

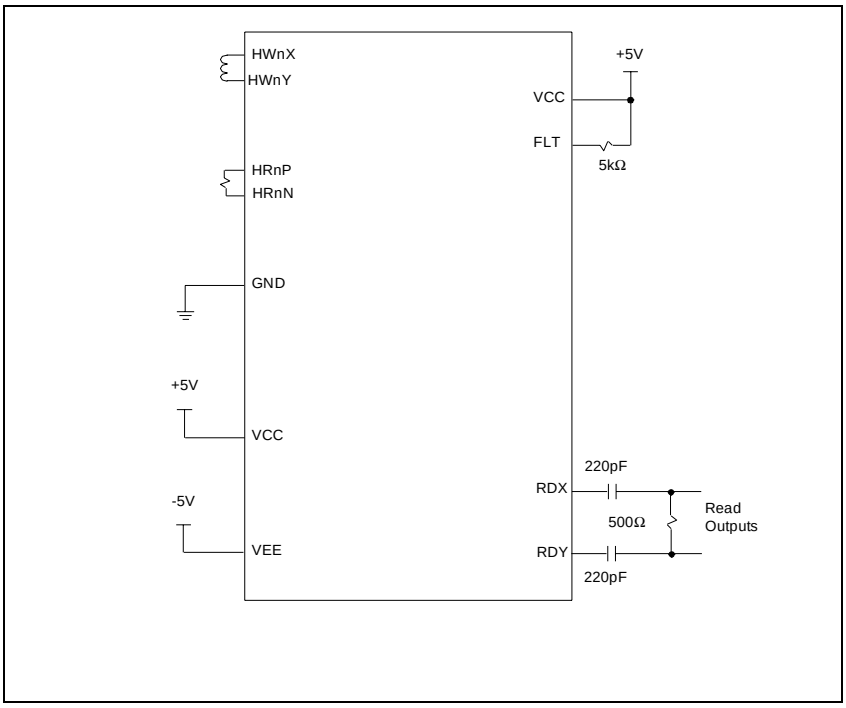
Signal	*Input/Output*	*Logic Level Default* [1]	*Description*
FLT/ABHV/DBHV	O [2]	–	Write/Read Fault and Buffered Head Voltage (Analog or Digital) as shown in truth table: • Fault (FLT) output: - A TTL high level indicates a fault in write mode. - A TTL low level indicates a fault in read mode. • Analog or Digital Buffered Head Voltage output when ABHV and/or DBHV is enabled.
GND	[2]	–	Ground
HR0N-HR7N	I	–	Read head connections, negative end.
HR0P-HR7P	I	–	Read head connections, positive end.
HW0X-HW7X	O	–	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	–	Thin-Film write head connections, negative end
R/WN	I [2]	high	Read/Write: A TTL low level enables write mode.
BIASN		high	MR Bias: • When 4:<D3> = 0 (BIASN): - A TTL high level diverts MR current internally and common mode clamps the reader outputs. - A TTL low level enables bias current through the active head.
RDP, RDN	O [2]	–	Read Data: Differential read signal outputs.
SCLK	I [2]	low	Serial Clock: Serial port clock; see Figure 40.
SDIO	I/O [2]	low	Serial Data: Serial port data; see Figure 40.
SENA	I [2]	low	Serial Enable: Serial port enable; see Figure 40.
VCC	[2]	–	+5.0V supply
VEE	[2]	–	-5.0V supply
WDX, WDY	I [2]	high	Differential Pseudo-ECL write data inputs

Output	*ABHV 9:<D7>*	*DBHV 4:<D3>*
FLT	0	0
DBHV	0	1
ABHV	1	0
ABHV [1]	1	1

1. ABHV overrides DBHV setting. Output is Analog Buffered Head Voltage (ABHV).

1. 40kΩ pullup/pulldown resistors are used to default pins to specified high or low levels.
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- Minimum FLT pullup resistance is 5 kΩ.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Idle Mode		15	**TBD**	
		Sleep Mode			**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Idle Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Idle Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%	3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}	Hysteresis = 100mV ±10%	-4.25	-4.0	-3.75	V
High Level WDATA		PECL	1.9		V_{CC}	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	0.8	1.0	2	

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WDATA PECL swing		Voltage mode differential [1]	0.4			V_{pp}
Voltage compliance for WDATA		CM of inputs when in current mode			V_{CC} -2.3	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		100		V/V
		Gain Bits = 11		250		V/V
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB	**TBD**	350	**TBD**	
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00	**TBD**	1	**TBD**	MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		$nV/\sqrt{Hz}$
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		$pA/\sqrt{Hz}$
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}	**TBD**		2	4	pF
Differential Input Resistance	R_{IN}			400		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	40			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Rejection	PSRR	100mV$_{pp}$ on V_{CC} or V_{EE}, 10 MHz < f < 200 MHz	40			dB
		100mV$_{pp}$ on V_{CC} or V_{EE}, 1 MHz < f < 10 MHz	40			
		100mV$_{pp}$ on V_{CC} or V_{EE}, f < 100 kHz	60			
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV$_{pp}$, 1 MHz < f < 200 MHz	50			dB
Rejection of SCLK and SDIO		100 mV$_{pp}$ on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2.0		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			**TBD**	
Reader Head Resistance	R_{MR}		25	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA, R_{MR}=100Ω.		**TBD**		nS
Reader Bias Current Overshoot					2.5	%
TA Detection Response Time		TA occurred to FLT active		20	40	nS
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		nS
MR Measurement Accuracy				4		%
Temperature Measurement Accuracy				2		^{o}C
BHV Accuracy				5		%
BHV Gain			4.75	5	5.25	V/V

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

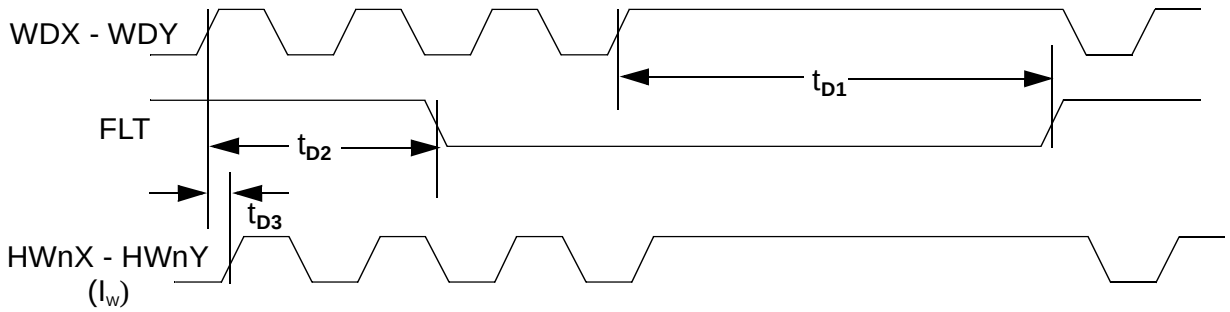
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		15		65	mA
Write Current Tolerance	ΔI_W	$15 < I_W < 65$ mA	-8		8	%
Write Servo Current Tolerance			-10		10	%
Differential Head Voltage Swing	V_{DH}	Open Head	6			V_{PP}
Unselected Head Transition Current	I_{UH}				1	mA_{pk}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			nS
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	nS
Write Data Input Terminal Resistor	w_{RIH}	Voltage mode write data input only		150		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	nS
R/WN to Read Mode	t_{WR}	To 90% of data envelope, DC Offset Level within 30 mV			300	nS
		To 10% of I_W envelope			50	nS
Idle to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 30 mV			5	µS
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 30 mV, **TBD** - Fixed I_{MR}.			1	µS
		To 90% of envelope, DC Offset Level within 30 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			3	µS
Idle (16th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			50	nS
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µS
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		nS
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		nS
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5nS rise/fall time, L_H=0, R_H=**TBD**			100	pS
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=70nH, R_H=10Ω.		500		pS
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.			**TBD**	nS
Read to Servo Write		From 50%R/WN to 90% I_W			50	nS
Read to Servo Write Head Turn-on Variation					**TBD**	nS
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µS
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	nS

1. See Figure 43 for the write mode timing diagram.

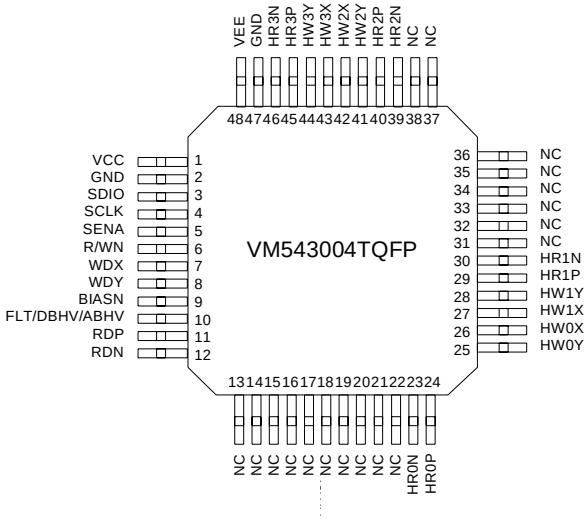


In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 43 Write Mode Timing Diagram *

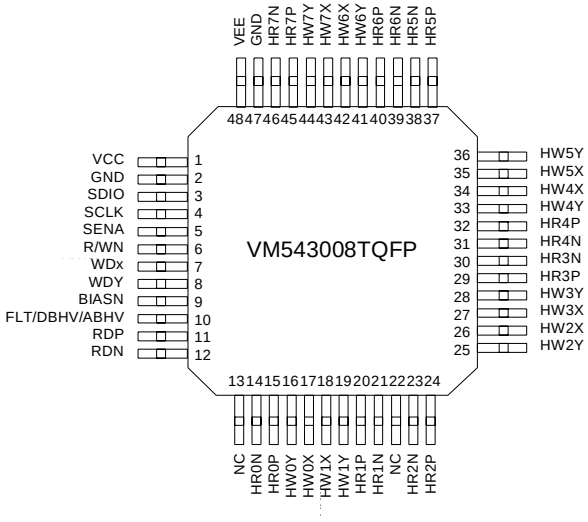
VM5430 PACKAGING

4-CHANNEL CONNECTION DIAGRAM



4-Channel
48-lead TQFP

8-CHANNEL CONNECTION DIAGRAM



8-Channel
48-lead TQFP

VTC Inc.
Value The Customer™

VM5431

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 500 Mbits/sec
  - Designed for Use With Four-Terminal GMR Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 8 Channels Available
  - Fault Detect Capability
  - Servo Bank Write Capability
- *High Performance Reader*
  - Current or Voltage Bias / Voltage Sense Configuration
  - Reader Bias Current/Voltage 6-bit DAC, 2 -10 mA Range
  - Programmable Read Voltage Gain (100 V/V to 250 V/V Typical)
  - Input Noise Voltage = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Noise Current = 8 pA/$\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Programmable Bandwidths to 350 MHz Typical
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 65 mA Range
  - Rise Time 500 pS Typical (10-90%, I_W = 50 mA, L_{total} = 70 nH, R = 10Ω)

DESCRIPTION

The VM5431 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM5431 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

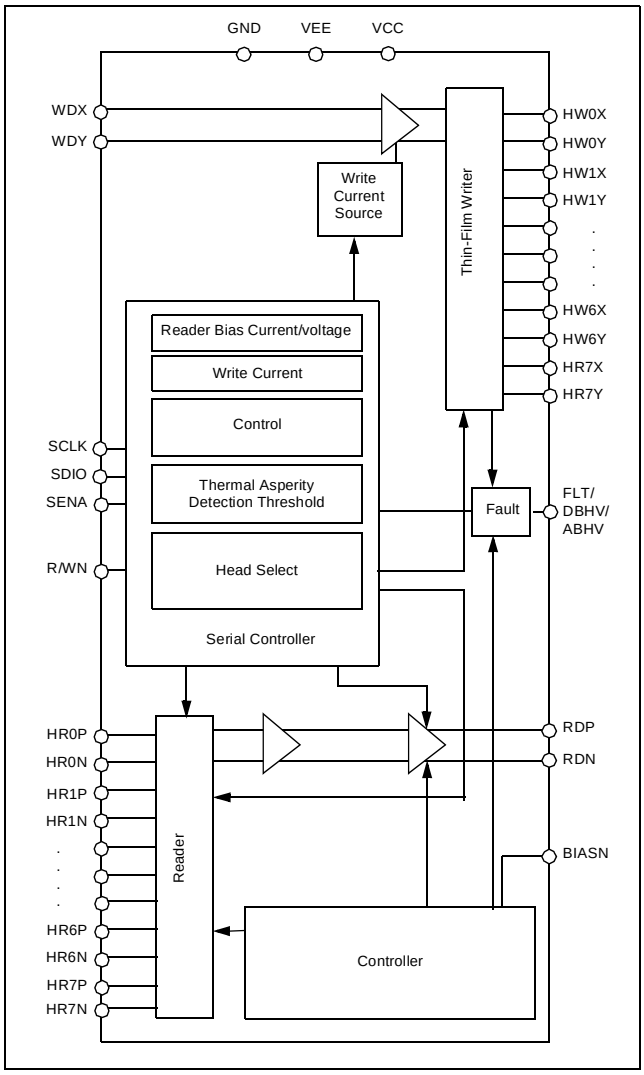
Programmability of the VM5431 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, write current overshoot and undershoot, fault modes, thermal asperity detection and threshold, and dynamic thermal asperity compensation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM5431 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. The device also provides power saving idle and sleep modes.

The VM5431 is available in 4 or 8-channel bump die forms for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR} ..... 18 mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
V_{EE} ..... -5V ± 10%
Write Current, I_W ..... 15 - 65 mA
Write Head Inductance, L_W ..... 70 nH
Write Head Resistance, R_W ..... 8 - 16 Ω
Read Bias:
Current, I_{MR} ..... 2 - 10 mA
Voltage, V_{MR} ..... 100 - 500 mV
Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 30 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM5431 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 109 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

All control lines on the VM5431 may be shared, including the serial lines SCLK, SDIO and SENA. Default settings are listed in Table 53 on page 115.

OPERATING MODES

Pin and register combinations select read/write, servo track write or mode operations as shown in Table 46.

Table 46 Mode Select

Pin		*Register:Bit*				
R/WN pin 5>	*BIASN pin 13>*	*SLEEPN 4:<D0>*	*IDLEN 4:<D1>*	*BANK1 4:<D6>*	*BANK0 2:<D7>*	*Operational Mode*
X	X	0	X	X	X	Sleep
X	X	1	0	X	X	Idle
0	0	1	1	0	0	Write Bias Active
0	1	1	1	0	0	Write
0	X	1	1	1	1	Servo Write
1	0	1	1	0	0	Read Bias Active
1	1	1	1	0	0	Read

Note: Two or more independent failures are required to cause an illegal chip selection, in which case the FLT pin is asserted and an error code is generated.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature or buffered head voltage.

Read Head Resistance

The resistance of the MR head can be measured in three ways: an automatic digital conversion, an iterative method using DBHV and threshold settings to trigger or not trigger a fault, or by monitoring the ABHV output.

Digital Conversion

To perform digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 46).
2) Set the RMR/TEMP bit (9:<D0>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)
4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 7:<D6-D0> = 0010000 the MR head resistance is 16 Ohms. (The measurement range for MR resistance is 0 - 127 Ω.)

Note: MR bias current is always enabled in this mode.

Iterative Resistance Reading

To perform the iterative resistance reading:

1) Place device in Read Mode (see Table 46).
2) Set the DBHV bit (4:<D3>) high to enter the MR resistance measurement mode.
3) Monitor the FLT/ABHV/DBHV pin to determine the voltage across the MR element:
   - A high indicates the voltage is within the window (150mv to 320mv).
   - A low indicates the voltage is outside the window.
4) Vary the MR bias current (9:<D2> and 1:<D3-D7>) to determine where the defined thresholds are crossed. The FLT line is not valid until the I_{MR} change settles; values for this are listed in SWITCHING CHARACTERISTICS on page 123.
5) Resistance can be inferred from the threshold settings.

Buffered Head Voltage

To output the MR head voltage on the FLT/ABHV/DBHV pin:

1) Place device in Read Mode (see Table 46).
2) Set ABHV bit (9:<D7>) high to output the MR head voltage as scaled by a gain of 5.

Note: If ABHV and DBHV are both high, ABHV takes precedence. See the truth table in PIN FUNCTION LIST AND DESCRIPTION on page 117.

Die Temperature Monitoring

The die temperature range is 0°C to 150°C. To measure the die temperature:

1) Set RMR/TEMP (9:<D7>) high to enable the die temperature.
2) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 7:<D6-D0> = 0100000 the die temperature is 38°C (32°C x 1.18).

$$T = 1.18k \qquad \textit{(eq. 16)}$$

where k = 0 - 127 and T is degrees Centigrade

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Sleep Mode

In the sleep mode power consumption is minimized. All outputs are disabled (except in test mode). The writer current source and the reader bias current/voltage source are deactivated and faults are not detected in Sleep Mode.

Sleep mode is selected by setting 4:<D0> = 0, see Tables 46, 50 and 52.

Note: Always transition from Sleep to Idle mode 10 µs before entering an active mode.

Idle Mode

The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN and RDP outputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. Faults are not detected in Idle Mode.

Idle mode is triggered by setting 4:<D1> = 0, see Tables 46, 50 and 52.

Dummy Mode

Setting DUMMY (9:<D1>) high directs the MR bias current/voltage to an internal dummy head. This maintains the reader bias at operational levels for quick read recovery.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting the R/WN pin high. In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM5431 uses the voltage-sensing reader architecture with biasing programmable as current or voltage. The magnitude of the reader bias current/voltage is set to the value programmed in 9:<D2> and 1:<D3-D7>. The equations below govern the read bias current/voltage magnitude:

$$\text{Current Mode} \quad I_{MR} = 2 + [k_{IMR} \cdot 0.127]\text{mA} \qquad \textit{(eq. 17)}$$

$$\text{Voltage Mode} \quad V_{MR} = 100 + [k_{IMR} \cdot 6.35]\text{mV} \qquad \textit{(eq. 18)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes:

- Current bias mode is selected by setting 9:<D4> = 0, and
- Voltage bias mode is selected by setting 9:<D4> = 1.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element. The applied value is programmed in 9:<D2> and 1:<D3-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

The reader enters a fast recovery mode during modal transitions, serial operations, and when the reader is biased during a write mode. The fast recovery mode minimizes signal anomalies on the reader outputs.

Read Bias Enable in Read Mode

Reader bias is controlled in the read mode by the BIASN pin. Taking the BIASN pin high in read mode disables the current to the selected read head.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 54.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 6:<D6-D0> as shown in Table 55. The default setting (0000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 53). The following are valid read fault conditions:

- MR Overcurrent
- Thermal Asperity Detected
- Read Head Open
- Read Head Shorted
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Read Gain

The default gain is 100 V/V with a head resistance of 55Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in 4:<D2 and 9:<D3>. The formula that describes the actual gain is shown below:

$$\text{GAIN} = \frac{475}{420 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 19)}$$

k_{GAIN} = 0-3

Fast Mode

Setting the FAST bit (4:<D5>) high in read mode, raises the low corner frequency to 5MHz. If the FAST bit is low, the low corner frequency is set to the value programmed in LFP (5:<D4-D5>).

Thermal Asperity Detection and Recovery

Detection

Setting the TAD bit high (3:<D3>) enables positive or negative thermal asperity detection.

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the voltage threshold is governed by the following equation and is set in 9:<D6> and 3:<D4-D7>:

$$V_{TAT} = 50 + \left[900 \times \left(\frac{k_{TAT}}{31}\right)\right] \qquad \textit{(eq. 20)}$$

V_{TAT} represents the TA threshold (output-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

Fast Recovery

Setting the TA Compensation (TAC) bit high (9:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised to 5MHz from the nominal value programmed in 5:<D4-D5>. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 3:<D3>.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting the R/WN pin low.

The magnitude of the write current is determined by the write current registers (2:<D0-D4>). The following equation governs the write current magnitude:

$$I_W = 15 + (k_{IW} \cdot 1.61)\,mA \qquad \textit{(eq. 21)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 47 for the timing diagram.

Write Current DAC

Register 2:<D0-D4> represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIASN pin low (at least 5µs before the R/WN pin is set high) enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (5:<D3>) initiates Write Data Inputs in Voltage Mode. Setting the WVORI bit high initiates the Write Data Inputs in Current Mode.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 54.

Specific fault conditions may be disabled by setting the Fault Reporting Mask, 6:<D0-D6> as shown in Table 55. The default setting (000000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 53).

The following are valid write fault conditions:

- Write Data Frequency Low
- Open or Shorted Write Head
- Servo Fault
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Servo Write Mode

In the servo write mode, up to eight channels may be written simultaneously.

Table 52 indicates how heads can be selected for individual or simultaneous writing.

Setting both BANK bits (2:<D7> and 4:<D6>) to ‘1’ and holding the R/WN pin low places the preamp in servo write mode (see Table 46). A high in SHDn (8:<D0> to 8:<D3> selects the specific head pair on which to perform the servo write. The default setting is to select all heads (8:<D0-D3> = 1111).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

A servo fault is generated if BANK bit (2:<D7> or 4:<D6>) settings do not match as shown in Table 47.

Table 47 Servo Faults

BANK1 4:<D6>	*BANK 0 2:<D7>*	*Mode*	*Fault*
0	0	Active [1]	No
0	1	Active [1]	Yes
1	0	Active [1]	Yes
1	1	Servo	No

1. Active includes all modes (read, write, idle, sleep or test), except servo.

SERIAL PORT

Serial Interface

The VM5431 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 49 and 50 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 44.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one command bit <A0> (high for read, low for write),
  - three chip select bits <A3-A1> that validate the preamplifier address logic levels in Table 49, and
  - four register address bits <A7-A4>.
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode. The reader invokes a *fast* mode while a serial interface operation occurs.

See Tables 49 and 50 for a bit description. See Table 48, and Figures 45 and 46 for serial interface timing information.

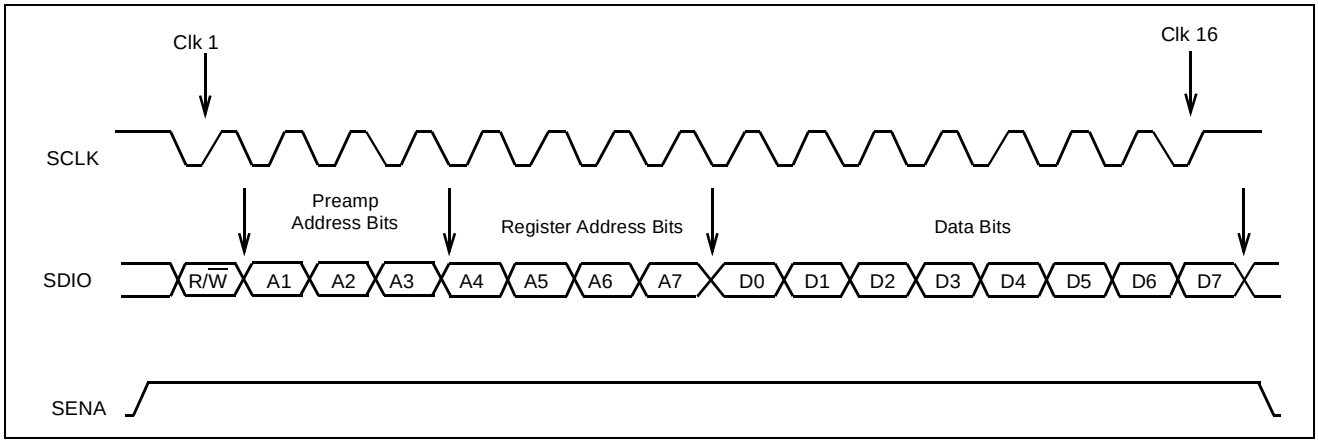


Figure 44 Serial Port Protocol

Table 48 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) rate, write				40	MHz
SENA to SCLK delay	T_{sens}	**TBD**			nS
SDIO setup time, write	T_{wds}	**TBD**			nS
SDIO delay time, read	T_{rds}	**TBD**		**TBD**	nS
SDIO hold time	T_{dh}	**TBD**			nS
SCLK cycle time	T_{c}	**TBD**			nS
SCLK high time	T_{ckh}	**TBD**			nS
SCLK low time	T_{ckl}	**TBD**			nS
SENA hold time	T_{shld}	**TBD**			nS
Time between I/O operations	T_{sl}	**TBD**			nS
Time from controller releasing SDIO (tristate) to SCLK falling edge	T_{tric}	**TBD**			nS
Time to activate SDIO	T_{act}	**TBD**		**TBD**	nS
Duration of SerEna (read)	T_{rd}	**TBD**			nS
Duration of SerEna (write)	T_{wt}	**TBD**			nS

Note: SENA assertion level is high.

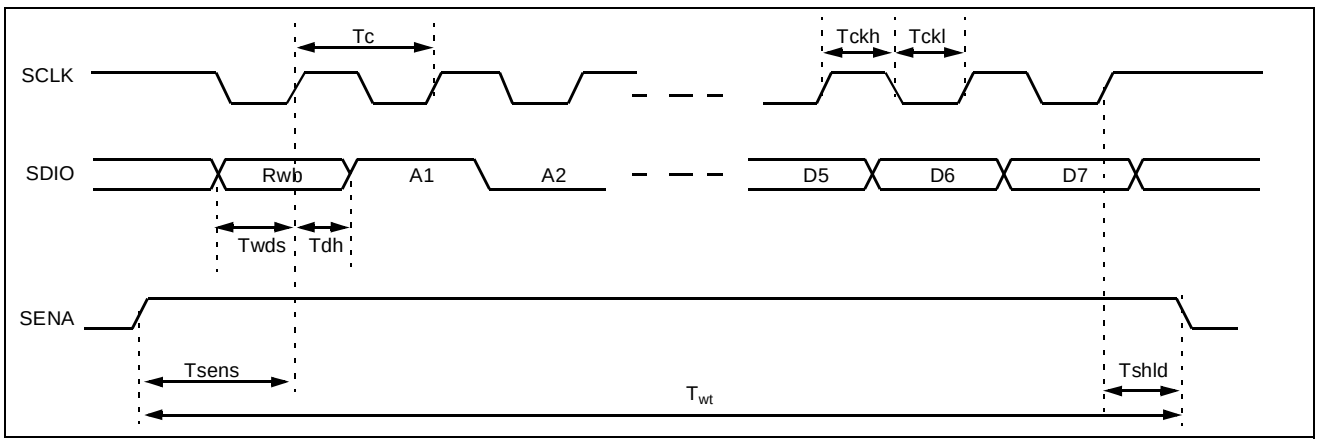


Figure 45 Serial Port Timing - Write Operation

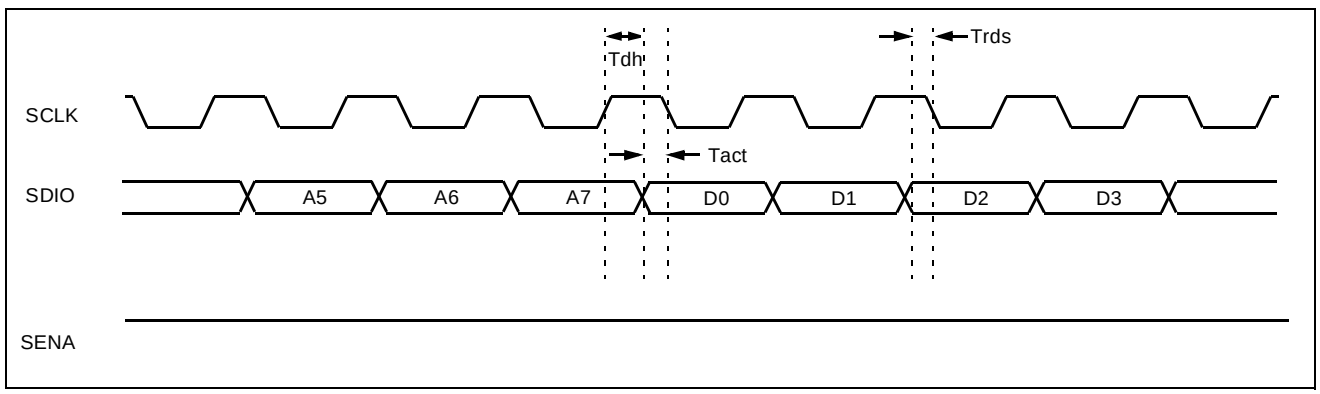


Figure 46 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 49 lists the serial address for each register. Table 50 lists the data contents of the basic register set and Table 51 lists register selections available as options. A description of the individual bits is provided in Table 52.

Table 49 Serial Interface Addressing

Register #	Register Address Bits				Preamp Address Bits			R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	0	0	0	0	0	0	1	0 = write 1 = read
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				

Table 50 Serial Interface Bit Map - Base Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Vendor ID	0 [1]	VEND0	VEND1	VEND2	REV0	REV1	REV2	CHNL	[2]
Head Select/IMR	1	HS0	HS1	HS2 [3]	IMR1	IMR2	IMR3	IMR4	IMR5
Write Current	2	IW0	IW1	IW2	IW3	IW4	[2]	[2]	BANK0
Thermal Asperity	3	OSC0	OSC1	OSC2	TAD	TA1	TA2	TA3	TA4
Mode Select	4	SLEEPN	IDLEN	GAIN0	DBHV	[2]	FAST	BANK1	[2]

1. Read Only Register/Bits:
   Register 0:<D0-D2> is the Vendor ID code (VTC=010),
   Register 0:<D3-D5> is the Vendor revision code. Initial revision shall be (REV0 = 0, REV1 = 0, REV2 = 0),
   Register 0:<D6> is the Channel count (0 = 8 channel, 1 = 4 channel),
2. Reserved.
3. Use restricted to 8-channel device.

Table 51 Serial Interface Bit Map - Optional Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Bandwidth/Under-shoot	5	USC0	USC1	USC2	WVORI	LFP0	LFP1	BW0	BW1
Fault	6	FLT0	FLT1	FLT2	FLT3	FLT4	FLT5	FLT6	CLRFC
Resistance/Temp	7	DSTR0	DSTR1	DSTR2	DSTR3	DSTR4	DSTR5	DSTR6	DIGON
Servo	8	SHD1/0	SHD3/2	SHD5/4	SHD7/6	FCODE0	FCODE1	FCODE2	FCODE3
Other	9	RMR/ TEMP	DUMMY	IMR0	GAIN1	I/V	TAC	TA0	ABHV
VTC Test	10	TTOSC	[1]	[1]	GMCTL	GMCTL	GMCTL	GMCTL	[1]

1. Reserved for VTC testing.

Table 52 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
0	D0-D2	Vendor Code	VENDn	Binary Vendor Code (010 = VTC)			
	D3-D5	Revision of Part	REVn	Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1after exceeding 8.			
	D6	Channel Count	CHNL	0 = 8 Channel device 1 = 4 Channel device			
	D7	Reserved					
1	D0-D2	Head Select	HSn	Binary selection of head	HS2	HS1	HS0
				Head Select	0:<D2>	0:<D1>	0:<D0>
				0	0	0	0
				1	0	0	1
				2	0	1	0
				3	0	1	1
				4	1	0	0
				5	1	0	1
				6	1	1	0
				7	1	1	1
				Note: Use of HS2 (0:<D2>) is restricted to 8-channel device.			
	D3-D7	Bias Level - MSB	IMRn	Binary selection of MR Head Bias - 5 most significant bits Current Bias = 2mA (00000) to 9.87mA (11111) in 0.254mA increments. Voltage Bias = 100mV (00000) to 494mV (11111) in 12.7mV increments. Note: The 5 most significant bits independently function as the I_{MR} or V_{MR} setting. The least significant bit of IMR DAC (9:<D2>)doubles the bias level resolution set by these bits. Note: Current or Voltage Bias is selected in 9:<D4>.			
2	D0-D4	Write Current	IWn	Binary selection of Write Current 15 mA (00000) to 65 mA (11111) in 1.6 mA increments.			
	D5-D6	Reserved					
	D7	Servo Bank 0	BANK0	0/1 = See Table 47, “Servo Faults,” on page 108 Note: BANK1 (4:<D6>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 53).			
3	D0-D2	Overshoot Control	OSCn	Overshoot Control **TBD** % 000) to **TBD** % (111) in **TBD** % increments.			
	D3	Thermal Asperity Detection	TAD	0 = TA Detection disabled. 1 = TA Detection enabled.			
	D4-D7	Thermal Asperity Threshold - MSB	TAn	Binary selection of Thermal Asperity Threshold - 4 most significant bits TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Least significant bit of thermal asperity (TA0) is stored in 9:<D6>.			

Table 52 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
4	D0	Sleep	SLEEPN	0/1 = See Table 46, “Mode Select,” on page 106 Note: This bit has precedence over the IDLEN bit (4:<D1>).		
	D1	Idle Mode	IDLEN	0/1 = See Table 46, “Mode Select,” on page 106 Note: The SLEEPN bit (4:<D0>) has precedence over this bit.		
	D2	Gain - LSB	GAIN0	Binary selection of MR Reader Gain least significant bit:	GAIN1	GAIN0
				Gain	9:<D3>	4:<D2>
				100 V/V	0	0
				150 V/V	0	1
				200 V/V	1	0
				250 V/V	1	1
				Note: Register 9:<D3> defines GAIN1 - MSB.		
	D3	Digital Buffered Head Voltage Output	DBHV	0 = Disable 1 = Enable Note: DBHV is overridden when ABHV (9:<D7>) is enabled.		
	D4	Reserved				
	D5	Fast Mode	FAST	Raises low corner frequency 5 MHz 0 = Disable 1 = Enable		
	D6	Servo Bank 1	BANK1	0/1 = See Table 47, “Servo Faults,” on page 108 Note: BANK0 (2:<D7>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 53).		
	D7	Reserved				
5	D0-D2	Undershoot Control	USCn	Undershoot Control **TBD** % (000) to **TBD** % (111) in **TBD** % increments.		
	D3	Write Voltage or Current	WVORI	0 = Voltage mode write data inputs. 1 = Current mode write data inputs.		
	D4-D5	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth:	LFP1	LFP0
				Low Frequency Bandwidth	5:<D5>	5:<D4>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				5 MHz	1	1
	D6-D7	Bandwidth	BWn	Binary selection of Bandwidth:	BW1	BW0
				Bandwidth	5:<D7>	5:<D6>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
6	D0-D6	Fault Mask	FLTn	Fault Reporting Mask See Table 55.		
	D7	Clear Fault Codes	CLRFC	0 = Retain faults 1 = Clear faults Note: CLRFC resets to 0 after fault codes clear.		

Table 52 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
7	D0-D6	MR Resistance or Die Temperature	DSTRn	Binary output (read only) of MR Head Resistance or Die Temperature: Resistance range is 0 to 127 Ohms. Temperature range is 0 to 150^{o}C. Note: 7:<D7> selects analog or digital output. Note: Register 9:<D0> selects resistance or temperature output.
	D7	Internal Digital Conversion	DIGON	0 = Analog-to-digital conversion off 1 = Start analog-to-digital conversion Note: DIGON resets to 0 when analog-to-digital conversion completes. Note: Reader Resistance or Die Temperature output is selected in 9:<D0> and the measurement is stored in 7:<D0-D6>.
8	D0-D3	Servo Head Select	SHDn	Binary selection of the head pairs to be servo track written. Examples: 1. 1000 = Servo Write Head Pair 6/7 [8 channel IC only (0:<D6> =0)]: 2. 0011 = Servo Write Head Pairs 0/1 and 2/3: - Bit 0 = 1 selects HD0/1 pair - Bit 1 = 1 selects HD2/3 pair - Bit 2 = 0 deselects HD4/5 pair - Bit 3 = 0 deselects HD6/7 pair Note: Default is to servo write all heads (see Table 53). Note: BANK0 and BANK1 (2:<D7> and 4:<D6>) must be selected to servo write.
	D4-D7	Fault Condition	FCODEn	Binary code of Fault(s) See Table 54.
9	D0	MR Head Resistance or Die Temperature	RMR/ TEMP	0 = MR Head Resistance stored in DSTRn register (7:<D0-D6>). 1 = Die Temperature stored in DSTRn register (7:<D0-D6>).
	D1	Dummy MR Head Load	DUMMY	0 = MR Head selected using HSn register (1:<D0-D2>) setting. 1 = Dummy head resistive load selected.
	D2	Bias Level - LSB	IMR0	Binary selection of MR Head Current Bias least significant bit Current Bias = 2mA (000000) to 10mA (111111) in 0.127mA increments. Voltage Bias = 100mV (000000) to 500mV (111111) in 6.35mV increments. Note: The 5 most significant bits of IMR DAC (IMR1 to IMR5) are stored in 1:<D3-D7> and independently function as the I_{MR} or V_{MR} setting. This bit (the LSB) functions as a I_{MR} or V_{MR} resolution doubling bit to the most significant bits (from 0.254mA or 12.7mV when only IMR1-IMR5 are used). Note: Current or Voltage Bias selected in 9:<D4>.
	D3	Gain - MSB	GAIN1	Binary selection of MR Reader Gain - most significant bits See register 4 bit 2 for an explanation of Reader Gain settings. Note: Register 4:<D2> defines GAIN0 - LSB.
	D4	Current or Voltage Bias	I/V	0 = Current bias mode. 1 = Voltage bias mode. Note: Bias level is set in registers 9:<D2> and 1:<D3-D7>
	D5	Thermal Asperity Compensation	TAC	0 = No TA Compensation. 1 = TA Compensation selected. Note: TA Detection must be enabled in 3:<D3> for TAC to function.
	D6	Thermal Asperity Threshold - LSB	TA0	Binary selection of Thermal Asperity Threshold - least significant bit TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Most significant bits of thermal asperity (TA1-TA4) are stored in 3:<D4-D7>.
	D7	Analog Buffered Head Voltage Output	ABHV	0 = Disable 1 = Enable Note: ABHV overrides DBHV (4:<D3>).

Table 52 Serial Register Data Bit Descriptions

Register	*Bits*	*Function*	*Symbol*	*Description*
10	D0	Reserved		
	D1		TTOSC	Reserved for VTC testing
	D2	Reserved		
	D3-D6		GMCTL	Reserved for VTC testing
	D7	Reserved		

Table 53 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Vendor ID	0	<XXXX XXXX>
Head Select/IMR	1	<0000 0000>
Write Current	2	<0000 0000>
Thermal Asperity	3	<0000 0100>
Mode Select	4	<0000 0000>
Bandwidth/Undershoot	5	<1100 0100>
Fault	6	<0000 0000>
Resistance/Temp	7	<0000 0000>
Servo	8	<XXXX 1111>
Other	9	<0000 0000>
VTC Test	10	<0000 0000>

Fault Reporting and Masking

Table 54 Fault Conditions and Codes

Fault Code 8:<D7-D4>	Fault	Priority [1]	Valid Mode(s)	Mask [2]	Conditions
0000	No Fault	–	Read or Write	–	
0001	Reserved	3	Read	–	
0010	MR Overcurrent	2	Read	M	
0011	Thermal Asperity Detected	6	Read	M	
0100	Read Head Open	7	Read	M [3]	
0101	Read Head Shorted	8	Read	M [3]	
0110	Write Data Frequency Low	5	Write	M	
0111	Write Head Open/Shorted	3	Write	M	
1000	Servo Fault	9	Read or Write		Unmatched servo bank bits
1001	Low V_{CC} or V_{EE}	1	Read or Write	M	
1010	Reserved	–	–	–	
1011	Overtemperature	10	Read or Write	M	Temp > 140^{o}C
1100	Invalid Head	4	Read or Write		Only applies to 6 and 12-channel devices.
1101	Reserved	–	–	–	
1110	Reserved	–	–	–	
1111	Reserved	–	–	–	

1. First fault reported is latched until a higher priority fault is reported or the code is cleared.
2. See Table 55 for an explanation of fault masking.
3. Single bit masks both faults.

Setting the appropriate bit(s) listed in Table 55 masks the fault(s) at both the fault register and the FLT pin. If 6:<D7-D0> = 0000 0101, an MR Overcurrent fault is masked with the 6:<D0> bit and Read Head Open and Read Head Shorted faults are masked with the 6:<D2> bit.

Table 55 Fault Masking

Mask Bit Register 6	Fault(s) Masked [1]	Mask Bit Register 6	Masked Fault
<D0>	MR Overcurrent	<D4>	Write Head Open/Shorted
<D1>	Thermal Asperity Detected	<D5>	Low V_{CC} or V_{EE}
<D2>	Read Head Open/Shorted	<D6>	Overtemperature
<D3>	Write Data Frequency Low		

1. Single bit masks both Read Head Open and Read Head Shorted faults.

PIN FUNCTION LIST AND DESCRIPTION

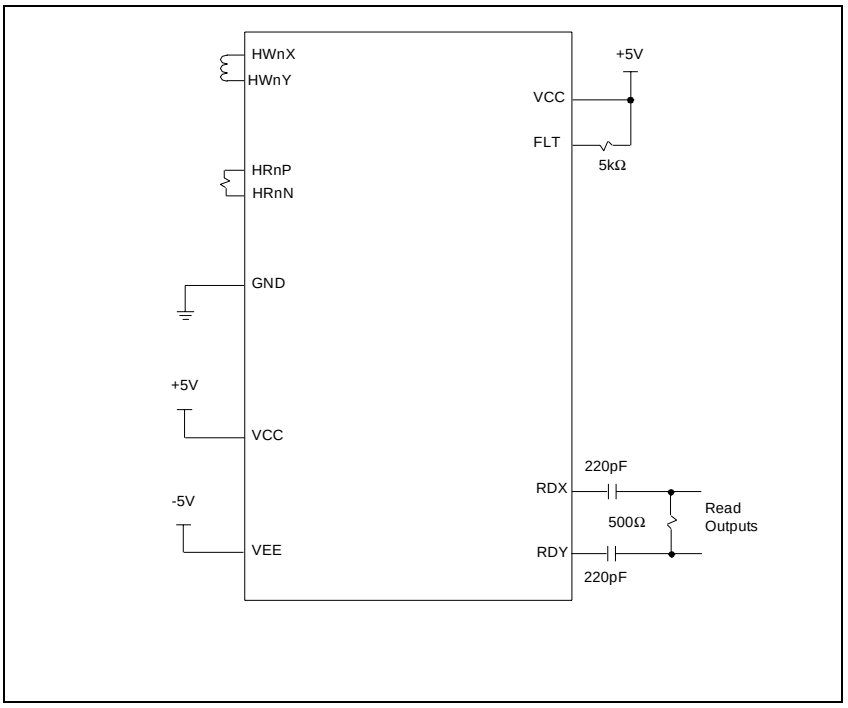
Signal	*Input/Output*	*Logic Level Default* [1]	*Description*
BIASN		high	MR Bias: • When 4:<D3> = 0 (BIASN): - A TTL high level diverts MR current internally and common mode clamps the reader outputs. - A TTL low level enables bias current through the active head.
FLT/ABHV/DBHV	O [2]	–	Write/Read Fault and Buffered Head Voltage (Analog or Digital) as shown in truth table: • Fault (FLT) output: - A TTL high level indicates a fault in write mode. - A TTL low level indicates a fault in read mode. • Analog or Digital Buffered Head Voltage output when ABHV and/or DBHV is enabled.
GND	[2]	–	Ground
HR0N-HR7N	I	–	Read head connections, negative end.
HR0P-HR7P	I	–	Read head connections, positive end.
HW0X-HW7X	O	–	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	–	Thin-Film write head connections, negative end
R/WN	I [2]	high	Read/Write: A TTL low level enables write mode.
RDP, RDN	O [2]	–	Read Data: Differential read signal outputs.
SCLK	I [2]	low	Serial Clock: Serial port clock; see Figure 44.
SDIO	I/O [2]	low	Serial Data: Serial port data; see Figure 44.
SENA	I [2]	low	Serial Enable: Serial port enable; see Figure 44.
VCC	[2]	–	+5.0V supply
VEE	[2]	–	-5.0V supply
WDX, WDY	I [2]	high	Differential Pseudo-ECL write data inputs

Output	*ABHV 9:<D7>*	*DBHV 4:<D3>*
FLT	0	0
DBHV	0	1
ABHV	1	0
ABHV [1]	1	1

1. ABHV overrides DBHV setting. Output is Analog Buffered Head Voltage (ABHV).

1. 40kΩ pullup/pulldown resistors are used to default pins to specified high or low levels.
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- Minimum FLT pullup resistance is 5 kΩ.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Idle Mode		15	**TBD**	
		Sleep Mode			**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Idle Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Idle Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%	3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}	Hysteresis = 100mV ±10%	-4.25	-4.0	-3.75	V
High Level WDATA		PECL	1.9		V_{CC}	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	0.8	1.0	2	

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WDATA PECL swing		Voltage mode differential [1]	0.4			V_{pp}
Voltage compliance for WDATA		CM of inputs when in current mode			V_{CC} -2.3	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		100		V/V
		Gain Bits = 11		250		V/V
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB	**TBD**	350	**TBD**	
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00	**TBD**	1	**TBD**	MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		$nV/\sqrt{Hz}$
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		$pA/\sqrt{Hz}$
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}	**TBD**		2	4	pF
Differential Input Resistance	R_{IN}			400		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	40			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Rejection	PSRR	100mV$_{pp}$ on V_{CC} or V_{EE}, 10 MHz < f < 200 MHz	40			dB
		100mV$_{pp}$ on V_{CC} or V_{EE}, 1 MHz < f < 10 MHz	40			
		100mV$_{pp}$ on V_{CC} or V_{EE}, f < 100 kHz	60			
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV$_{pp}$, 1 MHz < f < 200 MHz	50			dB
Rejection of SCLK and SDIO		100 mV$_{pp}$ on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2.0		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			**TBD**	
Reader Head Resistance	R_{MR}		30	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA, R_{MR}=100Ω.		**TBD**		nS
Reader Bias Current Overshoot					2.5	%
TA Detection Response Time		TA occurred to FLT active		20	40	nS
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		nS
MR Measurement Accuracy				4		%
Temperature Measurement Accuracy				2		^{o}C
BHV Accuracy				5		%
BHV Gain				5		V/V

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

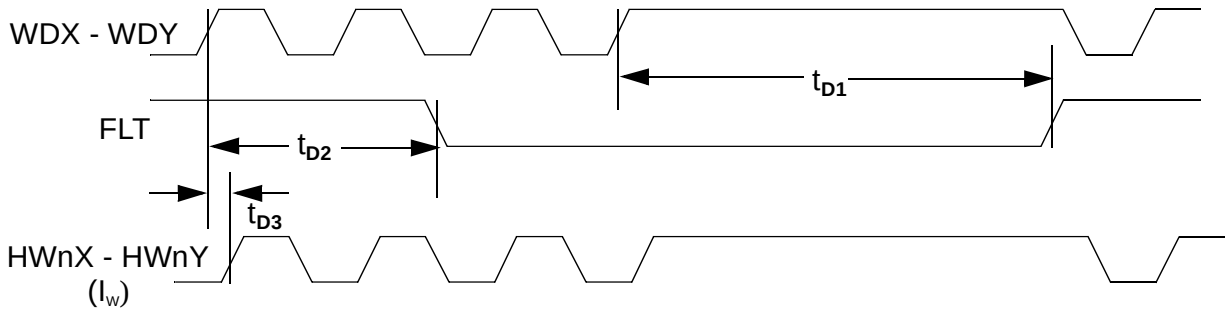
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		15		65	mA
Write Current Tolerance	ΔI_W	15 < I_W < 65 mA	-8		8	%
Write Servo Current Tolerance			-10		10	%
Differential Head Voltage Swing	V_{DH}	Open Head	6			V_{PP}
Unselected Head Transition Current	I_{UH}				1	mA_{pk}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			nS
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	nS
Write Data Input Terminal Resistor	w_{RIH}	Voltage mode write data input only		150		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	nS
R/WN to Read Mode	t_{WR}	To 90% of data envelope, DC Offset Level within 30 mV			300	nS
		To 10% of I_W envelope			50	nS
Idle to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 30 mV			5	µS
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 30 mV, **TBD** - Fixed I_{MR}.			1	µS
		To 90% of envelope, DC Offset Level within 30 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			3	µS
Idle (16th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			50	nS
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µS
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		nS
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		nS
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5nS rise/fall time, L_H=0, R_H=**TBD**			100	pS
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=70nH, R_H=10Ω.		500		pS
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.			**TBD**	nS
Read to Servo Write		From 50%R/WN to 90% I_W			50	nS
Read to Servo Write Head Turn-on Variation					**TBD**	nS
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µS
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	nS

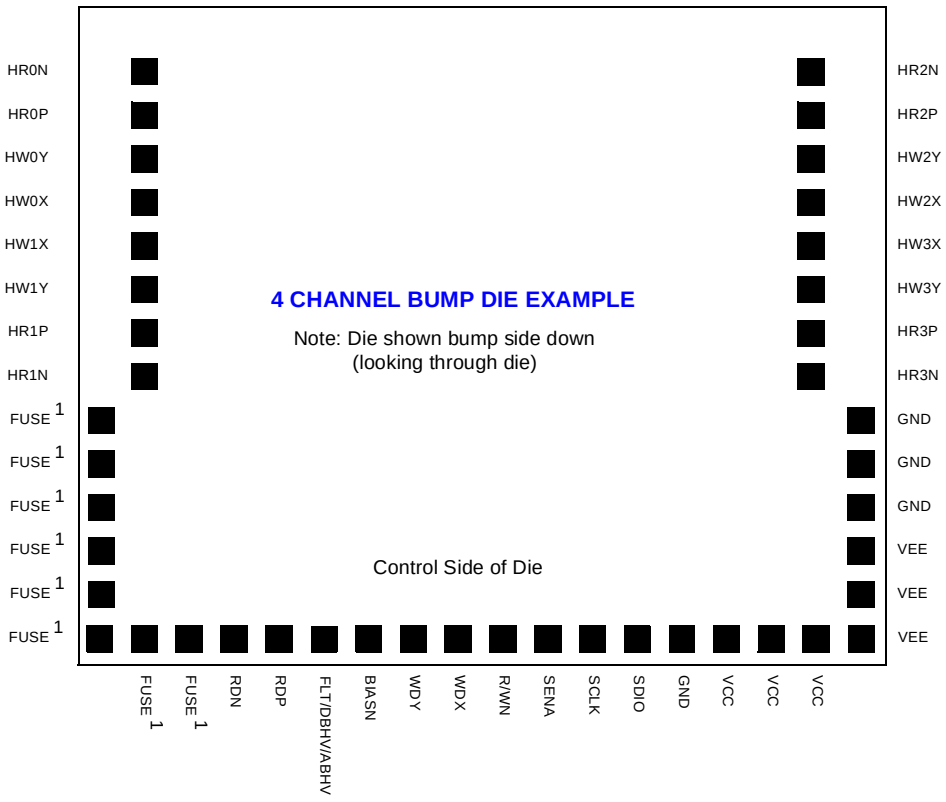
1. See Figure 47 for the write mode timing diagram.



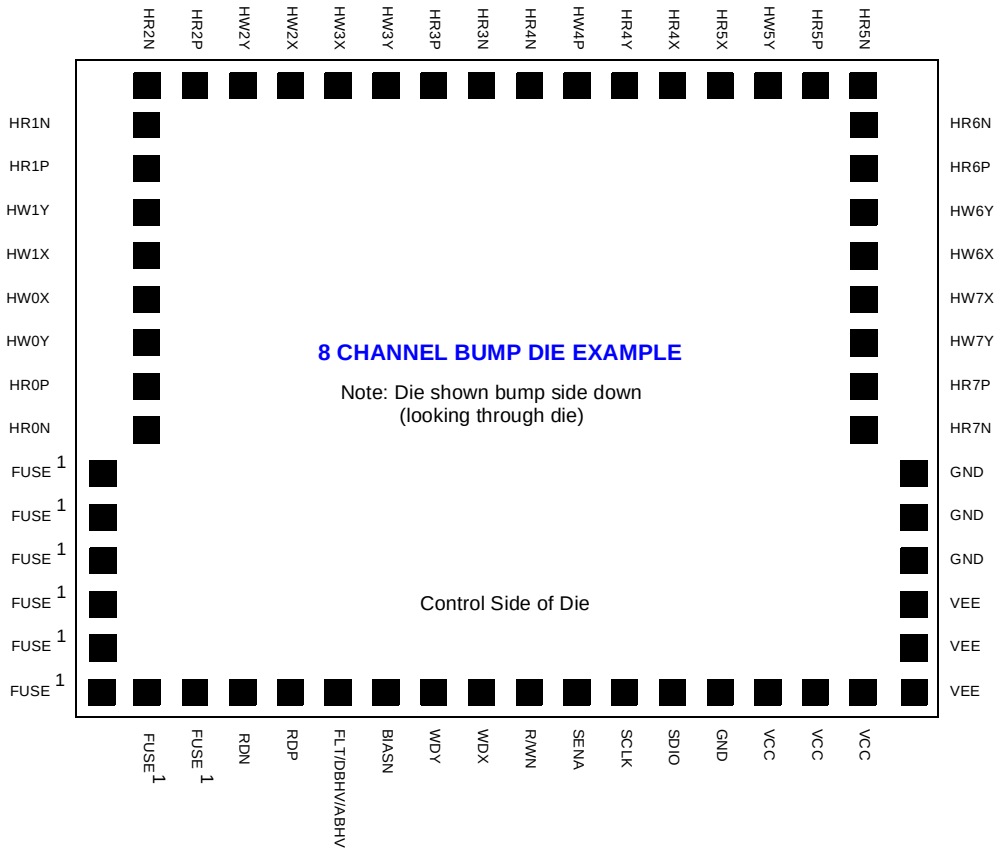
In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 47 Write Mode Timing Diagram

VM5431 PACKAGING



1) Landing pads on flex are required for these pads, but power or ground should not be routed to these pads.



1) Landing pads on flex are required for these pads, but power or ground should not be routed to these pads.

4-CHANNEL PAD COORDINATES

Specific Characteristics

Die size: **TBD** x **TBD** Mils

Pad Coordinates for the VM5431 (in Mils) are “bump down.”

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN	22.016	-60.520	4x4
FLT/ DBHV/ABHV	30.283	-60.520	4x4
FUSE0	52.484	-60.520	4x4oct
FUSE1	66.484	-60.520	4x4oct
FUSE2	67.551	-50.843	4x4oct
FUSE3	67.551	-36.843	4x4oct
FUSE4	67.551	-29.843	4x4oct
GND	-67.551	-39.543	4x4
GND	-67.551	-32.543	4x4
GND	-67.551	-25.543	4x4
GND	-37.157	-60.520	4x4
HR0N	53.319	38.917	4x4
HR0P	53.319	31.917	4x4
HR1N	53.319	-10.122	4x4
HR1P	53.319	-3.122	4x4
HR2N	-53.319	38.917	4x4
HR2P	-53.319	31.917	4x4
HR3N	-53.319	-10.122	4x4
HR3P	-53.319	-3.122	4x4
HW0X	53.319	17.917	4x4
HW0Y	53.319	24.917	4x4
HW1X	53.319	10.878	4x4
HW1Y	53.319	3.878	4x4
HW2X	-53.319	17.917	4x4
HW2Y	-53.319	24.917	4x4
HW3X	-53.319	10.878	4x4
HW3Y	-53.319	3.878	4x4
R/WN	-4.087	-60.520	4x4
RDN	44.878	-60.520	4x4
RDP	37.878	-60.520	4x4
SCLK	-20.622	-60.520	4x4
SDIO	-28.890	-60.520	4x4
SENA	-12.354	-60.520	4x4
VCC	-59.425	-60.520	4x4
VCC	-52.425	-60.520	4x4
VCC	-45.425	-60.520	4x4
VCC	59.484	-69.020	4x4
VCC	59.484	-60.520	4x4
VCC	67.551	-52.343	4x4
VCC	67.551	-43.843	4x4
VCC	67.551	-31.343	4x4
VCC	67.551	-22.843	4x4
VEE	-67.551	-53.543	4x4
VEE	-67.551	-46.543	4x4
VEE	-66.484	-60.520	4x4
WDX	3.575	-60.520	4x4
WDY	14.315	-60.520	4x4

8-CHANNEL PAD COORDINATES

Specific Characteristics

Die size: **TBD** x **TBD** Mils

Pad Coordinates for the VM5431 (in Mils) are “bump down.”

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN	22.016	-69.020	4x4
FLT/ DBHV/ABHV	30.283	-69.020	4x4
FUSE0	52.484	-69.020	4x4oct
FUSE1	66.484	-69.020	4x4oct
FUSE2	67.551	-59.343	4x4oct
FUSE3	67.551	-45.343	4x4oct
FUSE4	67.551	-38.343	4x4oct
GND	-67.551	-48.043	4x4
GND	-67.551	-41.043	4x4
GND	-67.551	-34.043	4x4
GND	-37.157	-69.020	4x4
HR0N	53.319	-18.622	4x4
HR0P	53.319	-11.622	4x4
HR1N	53.319	30.417	4x4
HR1P	53.319	23.417	4x4
HR2N	54.169	54.394	4x4
HR2P	47.169	54.394	4x4
HR3N	5.169	54.394	4x4
HR3P	12.169	54.394	4x4
HR4N	-5.169	54.394	4x4
HR4P	-12.169	54.394	4x4
HR5N	-54.169	54.394	4x4
HR5P	-47.169	54.394	4x4
HR6N	-53.319	30.417	4x4
HR6P	-53.319	23.417	4x4
HR7N	-53.319	-18.622	4x4
HR7P	-53.319	-11.622	4x4
HW0X	53.319	2.378	4x4
HW0Y	53.319	-4.622	4x4
HW1X	53.319	9.417	4x4
HW1Y	53.319	16.417	4x4
HW2X	33.169	54.394	4x4
HW2Y	40.169	54.394	4x4
HW3X	26.169	54.394	4x4
HW3Y	19.169	54.394	4x4
HW4X	-26.169	54.394	4x4
HW4Y	-19.169	54.394	4x4
HW5X	-33.169	54.394	4x4
HW5Y	-40.169	54.394	4x4
HW6X	-53.319	9.417	4x4
HW6Y	-53.319	16.417	4x4
HW7X	-53.319	2.378	4x4
HW7Y	-53.319	-4.622	4x4
R/WN	-4.087	-69.020	4x4
RDN	44.878	-69.020	4x4
RDP	37.878	-69.020	4x4
SCLK	-20.622	-69.020	4x4
SDIO	-28.890	-69.020	4x4
SENA	-12.354	-69.020	4x4
VCC	-59.425	-69.020	4x4
VCC	-52.425	-69.020	4x4
VCC	-45.425	-69.020	4x4
VCC	59.484	-69.020	4x4
VCC	67.551	-52.343	4x4
VEE	-67.551	-62.043	4x4
VEE	-67.551	-55.043	4x4
VEE	-66.484	-69.020	4x4
WDX	3.575	-69.020	4x4
WDY	14.315	-69.020	4x4

VTC Inc.
Value The Customer™

VM5432

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

MR PREAMPS

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 500 Mbits/sec
  - Designed for Use With Four-Terminal GMR Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 8 Channels Available
  - Fault Detect Capability
  - Servo Bank Write Capability
- *High Performance Reader*
  - Current or Voltage Bias / Voltage Sense Configuration
  - Reader Bias Current/Voltage 6-bit DAC, 2 -10 mA Range
  - Programmable Read Voltage Gain (100 V/V to 250 V/V Typical)
  - Input Noise Voltage = 0.55 $nV/\sqrt{Hz}$ Typical
  - Input Noise Current = 8 $pA/\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Programmable Bandwidths to 350 MHz Typical
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 65 mA Range
  - Rise Time 500 pS Typical (10-90%, I_W = 50 mA, L_{total} = 70 nH, R = 10Ω)

DESCRIPTION

The VM5432 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM5432 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

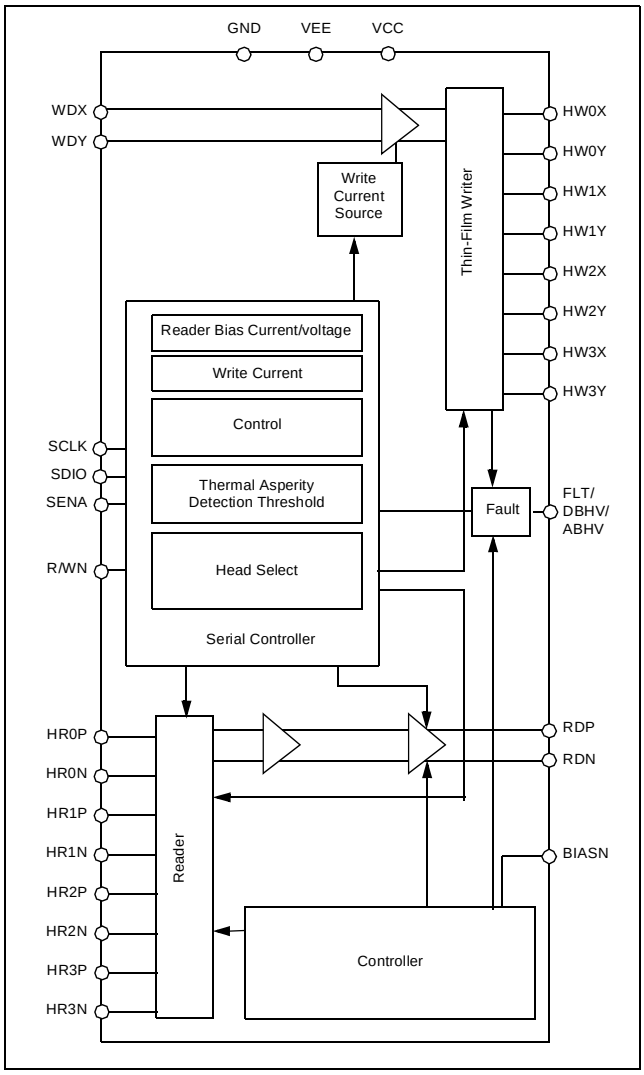
Programmability of the VM5432 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, write current overshoot and undershoot, fault modes, thermal asperity detection and threshold, and dynamic thermal asperity compensation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM5432 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. The device also provides power saving idle and sleep modes.

The VM5432 is available in a 48-pin TQFP package or bump die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR} ..... 18 mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -5V ± 10%

Write Current, I_W ..... 15 - 65 mA
Write Head Inductance, L_W ..... 70 nH
Write Head Resistance, R_W ..... 8 - 16 Ω
Read Bias:
- Current, I_{MR} ..... 2 - 10 mA
- Voltage, V_{MR} ..... 100 - 500 mV

Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM5432 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 133 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

All control lines on the VM5432 may be shared, including the serial lines SCLK, SDIO and SENA. Default settings are listed in Table 63 on page 139.

OPERATING MODES

Pin and register combinations select read/write, servo track write or mode operations as shown in Table 56.

Table 56 Mode Select

Pin		*Register:Bit*				
R/WN pin 5>	*BIASN pin 13>*	*SLEEPN 4:<D0>*	*IDLEN 4:<D1>*	*BANK1 4:<D6>*	*BANK0 2:<D7>*	*Operational Mode*
X	X	0	X	X	X	Sleep
X	X	1	0	X	X	Idle
0	0	1	1	0	0	Write Bias Active
0	1	1	1	0	0	Write
0	X	1	1	1	1	Servo Write
1	0	1	1	0	0	Read Bias Active
1	1	1	1	0	0	Read

Note: Two or more independent failures are required to cause an illegal chip selection, in which case the FLT pin is asserted and an error code is generated.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature or buffered head voltage.

Read Head Resistance

The resistance of the MR head can be measured in three ways: an automatic digital conversion, an iterative method using DBHV and threshold settings to trigger or not trigger a fault, or by monitoring the ABHV output.

Digital Conversion

To perform digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 56).
2) Set the RMR/TEMP bit (9:<D0>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)
4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 7:<D6-D0> = 0010000 the MR head resistance is 16 Ohms. (The measurement range for MR resistance is 0 - 127 Ω.)

Note: MR bias current is always enabled in this mode.

Iterative Resistance Reading

To perform the iterative resistance reading:

1) Place device in Read Mode (see Table 56).
2) Set the DBHV bit (4:<D3>) high to enter the MR resistance measurement mode.
3) Monitor the FLT/ABHV/DBHV pin to determine the voltage across the MR element:
   - A high indicates the voltage is within the window (150mv to 320mv).
   - A low indicates the voltage is outside the window.
4) Vary the MR bias current (9:<D2> and 1:<D3-D7>) to determine where the defined thresholds are crossed. The FLT line is not valid until the I_{MR} change settles; values for this are listed in SWITCHING CHARACTERISTICS on page 147.
5) Resistance can be inferred from the threshold settings.

Buffered Head Voltage

To output the MR head voltage on the FLT/ABHV/DBHV pin:

1) Place device in Read Mode (see Table 56).
2) Set ABHV bit (9:<D7>) high to output the MR head voltage as scaled by a gain of 5.

Note: If ABHV and DBHV are both high, ABHV takes precedence. See the truth table in PIN FUNCTION LIST AND DESCRIPTION on page 141.

Die Temperature Monitoring

The die temperature range is 0^oC to 150^oC. To measure the die temperature:

1) Set RMR/TEMP (9:<D7>) high to enable the die temperature.
2) Set DIGON bit (7:<D7>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 7:<D6-D0> = 0100000 the die temperature is 38^oC (32^oC x 1.18).

$$T = 1.18k \qquad \textit{(eq. 22)}$$

where k = 0 - 127 and T is degrees Centigrade

Sleep Mode

In the sleep mode power consumption is minimized. All outputs are disabled (except in test mode). The writer current source and the reader bias current/voltage source are deactivated and faults are not detected in Sleep Mode.

Sleep mode is selected by setting 4:<D0> = 0, see Tables 56, 60 and 62.

Note: Always transition from Sleep to Idle mode 10 µs before entering an active mode.

Idle Mode

The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN and RDP outputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. Faults are not detected in Idle Mode.

Idle mode is triggered by setting 4:<D1> = 0, see Tables 56, 60 and 62.

Dummy Mode

Setting DUMMY (9:<D1>) high directs the MR bias current/voltage to an internal dummy head. This maintains the reader bias at operational levels for quick read recovery.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting the R/WN pin high. In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM5432 uses the voltage-sensing reader architecture with biasing programmable as current or voltage. The magnitude of the reader bias current/voltage is set to the value programmed in 9:<D2> and 1:<D3-D7>. The equations below govern the read bias current/voltage magnitude:

$$\text{Current Mode} \quad I_{MR} = 2 + [k_{IMR} \cdot 0.127]\text{mA} \qquad \textit{(eq. 23)}$$

$$\text{Voltage Mode} \quad V_{MR} = 100 + [k_{IMR} \cdot 6.35]\text{mV} \qquad \textit{(eq. 24)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes:

- Current bias mode is selected by setting 9:<D4> = 0, and
- Voltage bias mode is selected by setting 9:<D4> = 1.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element. The applied value is programmed in 9:<D2> and 1:<D3-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

The reader enters a fast recovery mode during modal transitions, serial operations, and when the reader is biased during a write mode. The fast recovery mode minimizes signal anomalies on the reader outputs.

Read Bias Enable in Read Mode

Bias is always enabled in read mode.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 64.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 6:<D6-D0> as shown in Table 65. The default setting (0000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 63). The following are valid read fault conditions:

- MR Overcurrent
- Thermal Asperity Detected
- Read Head Open
- Read Head Shorted
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Read Gain

The default gain is 100 V/V with a head resistance of 55Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in 4:<D2 and 9:<D3>. The formula that describes the actual gain is shown below:

$$\text{GAIN} = \frac{475}{420 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 25)}$$

k_{GAIN} = 0-3

Fast Mode

Setting the FAST bit (4:<D5>) high in read mode, raises the low corner frequency to 5MHz. If the FAST bit is low, the low corner frequency is set to the value programmed in LFP (5:<D4-D5>).

Thermal Asperity Detection and Recovery

Detection

Setting the TAD bit high (3:<D3>) enables positive or negative thermal asperity detection.

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the voltage threshold is governed by the following equation and is set in 9:<D6> and 3:<D4-D7>:

$$V_{TAT} = 50 + \left[900 \times \left(\frac{k_{TAT}}{31}\right)\right] \qquad \textit{(eq. 26)}$$

V_{TAT} represents the TA threshold (output-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

Fast Recovery

Setting the TA Compensation (TAC) bit high (9:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised to 5MHz from the nominal value programmed in 5:<D4-D5>. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 3:<D3>.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting the R/WN pin low.

The magnitude of the write current is determined by the write current registers (2:<D0-D4>). The following equation governs the write current magnitude:

$$I_W = 15 + (k_{IW} \cdot 1.61)\,mA \qquad \textit{(eq. 27)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 51 for the timing diagram.

Write Current DAC

Register 2:<D0-D4> represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIASN pin low (at least 5µs before the R/WN pin is set high) enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (5:<D3>) initiates Write Data Inputs in Voltage Mode. Setting the WVORI bit high initiates the Write Data Inputs in Current Mode.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 64.

Specific fault conditions may be disabled by setting the Fault Reporting Mask, 6:<D0-D6> as shown in Table 65. The default setting (000000) is to enable all faults.

Fault codes are cleared by setting the Clear Fault bit, 6:<D7> = 1 or by a power-up reset (see Table 63).

The following are valid write fault conditions:

- Write Data Frequency Low
- Open or Shorted Write Head
- Servo Fault
- Low V_{CC} or V_{EE}
- Overtemperature
- Invalid Head Selected

Servo Write Mode

In the servo write mode, up to eight channels may be written simultaneously.

Table 62 indicates how heads can be selected for individual or simultaneous writing.

Setting both BANK bits (2:<D7> and 4:<D6>) to ‘1’ and holding the R/WN pin low places the preamp in servo write mode (see Table 56). A high in SHDn (8:<D0> to 8:<D3> selects the specific head pair on which to perform the servo write. The default setting is to select all heads (8:<D0-D3> = 1111).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

A servo fault is generated if BANK bit (2:<D7> or 4:<D6>) settings do not match as shown in Table 57.

Table 57 Servo Faults

BANK1 4:<D6>	*BANK 0 2:<D7>*	*Mode*	*Fault*
0	0	Active [1]	No
0	1	Active [1]	Yes
1	0	Active [1]	Yes
1	1	Servo	No

1. Active includes all modes (read, write, idle, sleep or test), except servo.

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SERIAL PORT

Serial Interface

The VM5432 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 59 and 60 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 48.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one command bit <A0> (high for read, low for write),
  - three chip select bits <A3-A1> that validate the preamplifier address logic levels in Table 59, and
  - four register address bits <A7-A4>.
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode. The reader invokes a *fast* mode while a serial interface operation occurs.

See Tables 59 and 60 for a bit description. See Table 58, and Figures 49 and 50 for serial interface timing information.

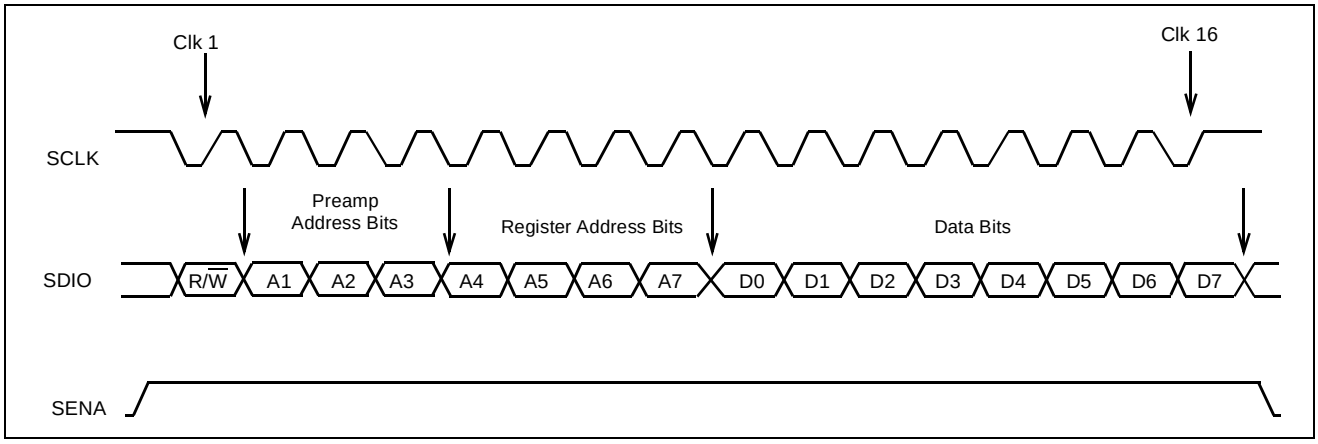


Figure 48 Serial Port Protocol

Table 58 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) rate, write				40	MHz
SENA to SCLK delay	T_{sens}	**TBD**			nS
SDIO setup time, write	T_{wds}	**TBD**			nS
SDIO delay time, read	T_{rds}	**TBD**		**TBD**	nS
SDIO hold time	T_{dh}	**TBD**			nS
SCLK cycle time	T_{c}	**TBD**			nS
SCLK high time	T_{ckh}	**TBD**			nS
SCLK low time	T_{ckl}	**TBD**			nS
SENA hold time	T_{shld}	**TBD**			nS
Time between I/O operations	T_{sl}	**TBD**			nS
Time from controller releasing SDIO (tristate) to SCLK falling edge	T_{tric}	**TBD**			nS
Time to activate SDIO	T_{act}	**TBD**		**TBD**	nS
Duration of SerEna (read)	T_{rd}	**TBD**			nS
Duration of SerEna (write)	T_{wt}	**TBD**			nS

Note: SENA assertion level is high.

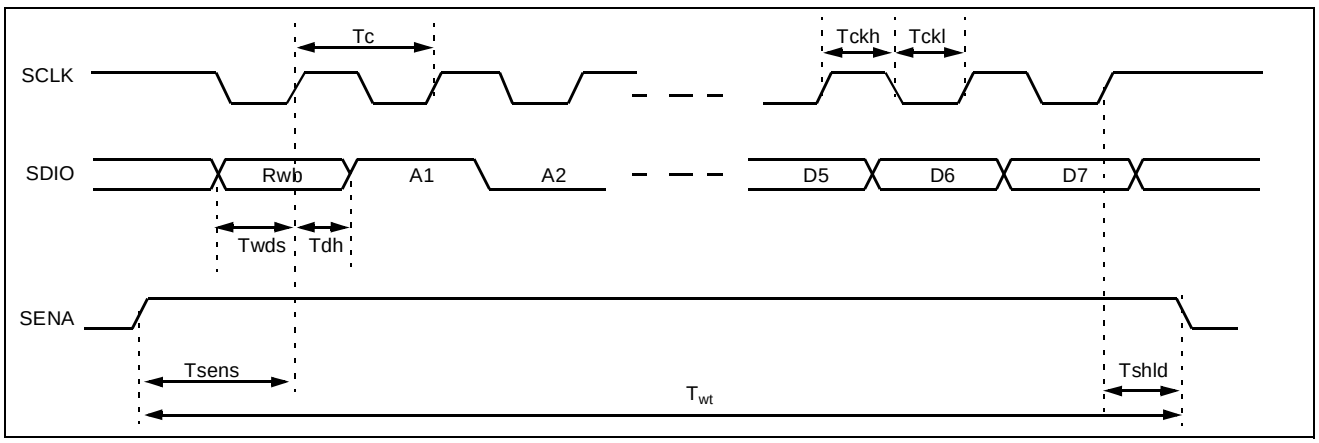


Figure 49 Serial Port Timing - Write Operation

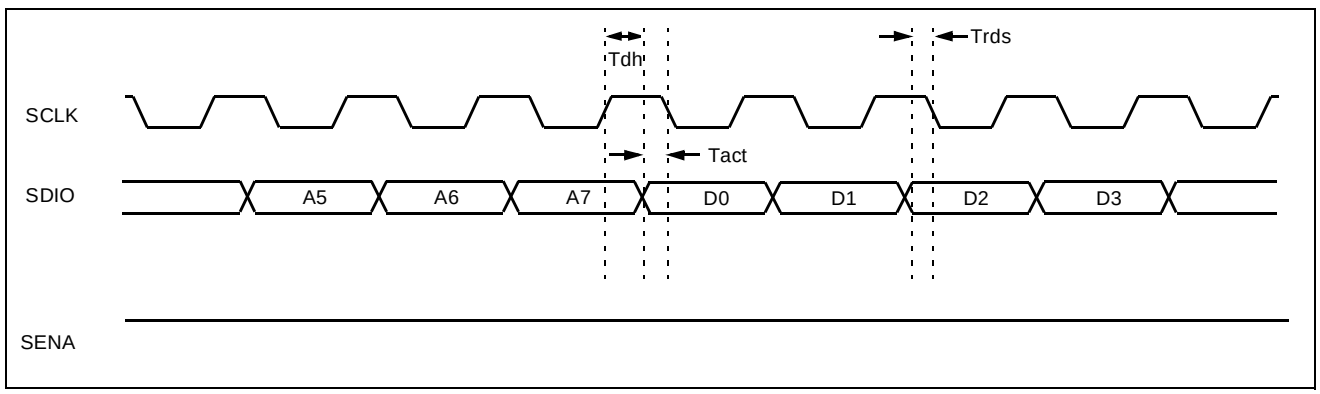


Figure 50 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 59 lists the serial address for each register. Table 60 lists the data contents of the basic register set and Table 61 lists register selections available as options. A description of the individual bits is provided in Table 62.

Table 59 Serial Interface Addressing

Register #	Register Address Bits				Preamp Address Bits			R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	0	0	0	0	0	0	1	0 = write 1 = read
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				

Table 60 Serial Interface Bit Map - Base Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Vendor ID	0 [1]	VEND0	VEND1	VEND2	REV0	REV1	REV2	CHNL	[2]
Head Select/IMR	1	HS0	HS1	HS2 [3]	IMR1	IMR2	IMR3	IMR4	IMR5
Write Current	2	IW0	IW1	IW2	IW3	IW4	[2]	[2]	BANK0
Thermal Asperity	3	OSC0	OSC1	OSC2	TAD	TA1	TA2	TA3	TA4
Mode Select	4	SLEEPN	IDLEN	GAIN0	DBHV	[2]	FAST	BANK1	[2]

1. Read Only Register/Bits:
   Register 0:<D0-D2> is the Vendor ID code (VTC=010),
   Register 0:<D3-D5> is the Vendor revision code. Initial revision shall be (REV0 = 0, REV1 = 0, REV2 = 0),
   Register 0:<D6> is the Channel count (0 = 8 channel, 1 = 4 channel),
2. Reserved.
3. Use of HS2 (1:<D2>) is restricted to 8-channel device.

Table 61 Serial Interface Bit Map - Optional Registers

Function	Register #	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D5>	<D4>	<D6>	<D7>
Bandwidth/Under-shoot	5	USC0	USC1	USC2	WVORI	LFP1	LFP0	BW0	BW1
Fault	6	FLT0	FLT1	FLT2	FLT3	FLT5	FLT4	FLT6	CLRFC
Resistance/Temp	7	DSTR0	DSTR1	DSTR2	DSTR3	DSTR5	DSTR4	DSTR6	DIGON
Servo	8	SHD1/0	SHD3/2	SHD5/4	SHD7/6	FCODE1	FCODE0	FCODE2	FCODE3
Other	9	RMR/ TEMP	DUMMY	IMR0	GAIN1	TAC	I/V	TA0	ABHV
Reserved	10	TTOSC	[1]	[1]	GMCTL	GMCTL	GMCTL	GMCTL	[1]

1. Reserved for VTC testing.

Table 62 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
0	D0-D2	Vendor Code	VENDn	Binary Vendor Code (010 = VTC)			
	D3-D5	Revision of Part	REVn	Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1after exceeding 8.			
	D6	Channel Count	CHNL	0 = 8 Channel device 1 = 4 Channel device			
	D7	Reserved					
1	D0-D2	Head Select	HSn	Binary selection of head	HS2	HS1	HS0
				Head Select	1:<D2>	1:<D1>	1:<D0>
				0	0	0	0
				1	0	0	1
				2	0	1	0
				3	0	1	1
				4	1	0	0
				5	1	0	1
				6	1	1	0
				7	1	1	1
				Note: Use of HS2 (1:<D2>) is restricted to 8-channel device.			
	D3-D7	Bias Level - MSB	IMRn	Binary selection of MR Head Bias - 5 most significant bits Current Bias = 2mA (00000) to 9.87mA (11111) in 0.254mA increments. Voltage Bias = 100mV (00000) to 494mV (11111) in 12.7mV increments. Note: The 5 most significant bits independently function as the I_{MR} or V_{MR} setting. The least significant bit of IMR DAC (9:<D2>)doubles the bias level resolution set by these bits. Note: Current or Voltage Bias is selected in 9:<D4>.			
2	D0-D4	Write Current	IWn	Binary selection of Write Current 15 mA (00000) to 65 mA (11111) in 1.6 mA increments.			
	D5-D6	Reserved					
	D7	Servo Bank 0	BANK0	0/1 = See Table 57, “Servo Faults,” on page 132 Note: BANK1 (4:<D6>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 63).			
3	D0-D2	Overshoot Control	OSCn	Overshoot Control **TBD** % 000) to **TBD** % (111) in **TBD** % increments.			
	D3	Thermal Asperity Detection	TAD	0 = TA Detection disabled. 1 = TA Detection enabled.			
	D4-D7	Thermal Asperity Threshold - MSB	TAn	Binary selection of Thermal Asperity Threshold - 4 most significant bits TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Least significant bit of thermal asperity (TA0) is stored in 9:<D6>.			

Table 62 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
4	D0	Sleep	SLEEPN	0/1 = See Table 56, “Mode Select,” on page 130 Note: This bit has precedence over the IDLEN bit (4:<D1>).		
	D1	Idle Mode	IDLEN	0/1 = See Table 56, “Mode Select,” on page 130 Note: The SLEEPN bit (4:<D0>) has precedence over this bit.		
	D2	Gain - LSB	GAIN0	Binary selection of MR Reader Gain least significant bit:	GAIN1	GAIN0
				Gain	9:<D3>	4:<D2>
				100 V/V	0	0
				150 V/V	0	1
				200 V/V	1	0
				250 V/V	1	1
				Note: Register 9:<D3> defines GAIN1 - MSB.		
	D3	Digital Buffered Head Voltage Output	DBHV	0 = Disable 1 = Enable Note: DBHV is overridden when ABHV (9:<D7>) is enabled.		
	D4	Reserved				
	D5	Fast Mode	FAST	Raises low corner frequency 5 MHz 0 = Disable 1 = Enable		
	D6	Servo Bank 1	BANK1	0/1 = See Table 57, “Servo Faults,” on page 132 Note: BANK0 (2:<D7>) must also be selected for a valid servo write. Note: Register 8:<D0-D3> defines which heads to servo write. Default is to servo write 8 heads (see Table 63).		
	D7	Reserved				
5	D0-D2	Undershoot Control	USCn	Undershoot Control **TBD** % (000) to **TBD** % (111) in **TBD** % increments.		
	D3	Write Voltage or Current	WVORI	0 = Voltage mode write data inputs. 1 = Current mode write data inputs.		
	D4-D5	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth:	LFP1	LFP0
				Low Frequency Bandwidth	5:<D5>	5:<D4>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				5 MHz	1	1
	D6-D7	Bandwidth	BWn	Binary selection of Bandwidth:	BW1	BW0
				Bandwidth	5:<D7>	5:<D6>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
6	D0-D6	Fault Mask	FLTn	Fault Reporting Mask See Table 65.		
	D7	Clear Fault Codes	CLRFC	0 = Retain faults 1 = Clear faults Note: CLRFC resets to 0 after fault codes clear.		

Table 62 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
7	D0-D6	MR Resistance or Die Temperature	DSTRn	Binary output (read only) of MR Head Resistance or Die Temperature: Resistance range is 0 to 127 Ohms. Temperature range is 0 to 150^{o}C. Note: 7:<D7> selects analog or digital output. Note: Register 9:<D0> selects resistance or temperature output.
	D7	Internal Digital Conversion	DIGON	0 = Analog-to-digital conversion off 1 = Start analog-to-digital conversion Note: DIGON resets to 0 when analog-to-digital conversion completes. Note: Reader Resistance or Die Temperature output is selected in 9:<D0> and the measurement is stored in 7:<D0-D6>.
8	D0-D3	Servo Head Select	SHDn	Binary selection of the head pairs to be servo track written. Examples: 1. 1000 = Servo Write Head Pair 6/7 [8 channel IC only (0:<D6> =0)]: 2. 0011 = Servo Write Head Pairs 0/1 and 2/3: - Bit 0 = 1 selects HD0/1 pair - Bit 1 = 1 selects HD2/3 pair - Bit 2 = 0 deselects HD4/5 pair - Bit 3 = 0 deselects HD6/7 pair Note: Default is to servo write all heads (see Table 63). Note: BANK0 and BANK1 (2:<D7> and 4:<D6>) must be selected to servo write.
	D4-D7	Fault Condition	FCODEn	Binary code of Fault(s) See Table 64.
9	D0	MR Head Resistance or Die Temperature	RMR/ TEMP	0 = MR Head Resistance stored in DSTRn register (7:<D0-D6>). 1 = Die Temperature stored in DSTRn register (7:<D0-D6>).
	D1	Dummy MR Head Load	DUMMY	0 = MR Head selected using HSn register (1:<D0-D2>) setting. 1 = Dummy head resistive load selected.
	D2	Bias Level - LSB	IMR0	Binary selection of MR Head Current Bias least significant bit Current Bias = 2mA (000000) to 10mA (111111) in 0.127mA increments. Voltage Bias = 100mV (000000) to 500mV (111111) in 6.35mV increments. Note: The 5 most significant bits of IMR DAC (IMR1 to IMR5) are stored in 1:<D3-D7> and independently function as the I_{MR} or V_{MR} setting. This bit (the LSB) functions as a I_{MR} or V_{MR} resolution doubling bit to the most significant bits (from 0.254mA or 12.7mV when only IMR1-IMR5 are used). Note: Current or Voltage Bias selected in 9:<D4>.
	D3	Gain - MSB	GAIN1	Binary selection of MR Reader Gain - most significant bits See register 4 bit 2 for an explanation of Reader Gain settings. Note: Register 4:<D2> defines GAIN0 - LSB.
	D4	Current or Voltage Bias	I/V	0 = Current bias mode. 1 = Voltage bias mode. Note: Bias level is set in registers 9:<D2> and 1:<D3-D7>
	D5	Thermal Asperity Compensation	TAC	0 = No TA Compensation. 1 = TA Compensation selected. Note: TA Detection must be enabled in 3:<D3> for TAC to function.
	D6	Thermal Asperity Threshold - LSB	TA0	Binary selection of Thermal Asperity Threshold - least significant bit TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV. Note: Most significant bits of thermal asperity (TA1-TA4) are stored in 3:<D4-D7>.
	D7	Analog Buffered Head Voltage Output	ABHV	0 = Disable 1 = Enable Note: ABHV overrides DBHV (4:<D3>).

Table 62 Serial Register Data Bit Descriptions

Register	*Bits*	*Function*	*Symbol*	*Description*
10	D0	Reserved		
	D1		TTOSC	Reserved for VTC testing
	D2	Reserved		
	D3-D6		GMCTL	Reserved for VTC testing
	D7	Reserved		

Table 63 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Vendor ID	0	<XXXX XXXX>
Head Select/IMR	1	<0000 0000>
Write Current	2	<0000 0000>
Thermal Asperity	3	<0000 0100>
Mode Select	4	<0000 0000>
Bandwidth/Undershoot	5	<1100 0100>
Fault	6	<0000 0000>
Resistance/Temp	7	<0000 0000>
Servo	8	<XXXX 1111>
Other	9	<0000 0000>
Reserved	10	<0000 0000>

Fault Reporting and Masking

Table 64 Fault Conditions and Codes

Fault Code 8:<D7-D4>	Fault	Priority [1]	Valid Mode(s)	Mask [2]	Conditions
0000	No Fault	–	Read or Write	–	
0001	Reserved	3	Read	–	
0010	MR Overcurrent	2	Read	M	
0011	Thermal Asperity Detected	6	Read	M	
0100	Read Head Open	7	Read	M [3]	
0101	Read Head Shorted	8	Read	M [3]	
0110	Write Data Frequency Low	5	Write	M	
0111	Write Head Open/Shorted	3	Write	M	
1000	Servo Fault	9	Read or Write		Unmatched servo bank bits
1001	Low V_{CC} or V_{EE}	1	Read or Write	M	
1010	Reserved	–	–	–	
1011	Overtemperature	10	Read or Write	M	Temp > 140^{o}C
1100	Invalid Head	4	Read or Write		Only applies to 6 or 12 channel devices
1101	Reserved	–	–	–	
1110	Reserved	–	–	–	
1111	Reserved	–	–	–	

1. First fault reported is latched until a higher priority fault is reported or the code is cleared.
2. See Table 65 for an explanation of fault masking.
3. Single bit masks both faults.

Setting the appropriate bit(s) listed in Table 65 masks the fault(s) at both the fault register and the FLT pin. If 9:<D7-D0> = 0000 0101, an MR Overcurrent fault is masked with the 9:<D0> bit and Read Head Open and Read Head Shorted faults are masked with the 9:<D2> bit.

Table 65 Fault Masking

Mask Bit Register 6	Fault(s) Masked [1]	Mask Bit Register 6	Masked Fault
<D0>	MR Overcurrent	<D4>	Write Head Open/Shorted
<D1>	Thermal Asperity Detected	<D5>	Low V_{CC} or V_{EE}
<D2>	Read Head Open/Shorted	<D6>	Overtemperature
<D3>	Write Data Frequency Low		

1. Single bit masks both Read Head Open and Read Head Shorted faults.

PIN FUNCTION LIST AND DESCRIPTION

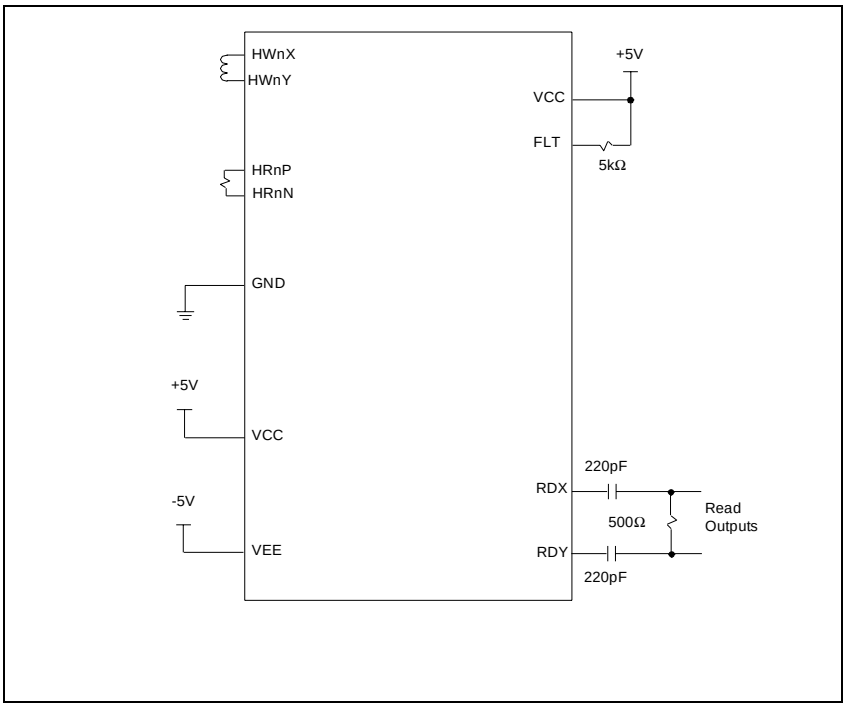
Signal	*Input/Output*	*Logic Level Default* [1]	*Description*
FLT/ABHV/DBHV	O [2]	–	Write/Read Fault and Buffered Head Voltage (Analog or Digital) as shown in truth table: • Fault (FLT) output: - A TTL high level indicates a fault in write mode. - A TTL low level indicates a fault in read mode. • Analog or Digital Buffered Head Voltage output when ABHV and/or DBHV is enabled.
GND	[2]	–	Ground
HR0N-HR3N	I	–	Read head connections, negative end.
HR0P-HR3P	I	–	Read head connections, positive end.
HW0X-HW3X	O	–	Thin-Film write head connections, positive end.
HW0Y-HW3Y	O	–	Thin-Film write head connections, negative end
R/WN	I [2]	high	Read/Write: A TTL low level enables write mode.
BIASN		high	MR Bias: • When 4:<D3> = 0 (BIASN): - A TTL high level diverts MR current internally and common mode clamps the reader outputs. - A TTL low level enables bias current through the active head.
RDP, RDN	O [2]	–	Read Data: Differential read signal outputs.
SCLK	I [2]	low	Serial Clock: Serial port clock; see Figure 48.
SDIO	I/O [2]	low	Serial Data: Serial port data; see Figure 48.
SENA	I [2]	low	Serial Enable: Serial port enable; see Figure 48.
VCC	[2]	–	+5.0V supply
VEE	[2]	–	-5.0V supply
WDX, WDY	I [2]	high	Differential Pseudo-ECL write data inputs

Output	*ABHV 9:<D7>*	*DBHV 4:<D3>*
FLT	0	0
DBHV	0	1
ABHV	1	0
ABHV [1]	1	1

1. ABHV overrides DBHV setting. Output is Analog Buffered Head Voltage (ABHV).

1. 40kΩ pullup/pulldown resistors are used to default pins to specified high or low levels.
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- Minimum FLT pullup resistance is 5 kΩ.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Idle Mode		15	**TBD**	
		Sleep Mode			**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Idle Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Idle Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%	3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}	Hysteresis = 100mV ±10%	-4.25	-4.0	-3.75	V
High Level WDATA		PECL	1.9		V_{CC}	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	0.8	1.0	2	mA

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WDATA PECL swing		Voltage mode differential [1]	0.4			V_{pp}
Voltage compliance for WDATA		CMM of inputs when in current mode			V_{CC} -1.0	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		100		V/V
		Gain Bits = 11		250		V/V
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB	**TBD**	350	**TBD**	
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00	**TBD**	1	**TBD**	MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		nV/√Hz
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		pA/√Hz
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}	**TBD**		2	4	pF
Differential Input Resistance	R_{IN}			400		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	40			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			

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READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Rejection	PSRR	100mV$_{pp}$ on V_{CC} or V_{EE}, 10 MHz < f < 200 MHz	40			dB
		100mV$_{pp}$ on V_{CC} or V_{EE}, 1 MHz < f < 10 MHz	40			
		100mV$_{pp}$ on V_{CC} or V_{EE}, f < 100 kHz	60			
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV$_{pp}$, 1 MHz < f < 200 MHz	50			dB
Rejection of SCLK and SDIO		100 mV$_{pp}$ on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2.0		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			**TBD**	
Reader Head Resistance	R_{MR}		25	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA, R_{MR}=100Ω.		**TBD**		nS
Reader Bias Current Overshoot					2.5	%
TA Detection Response Time		TA occurred to FLT active		20	40	nS
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		nS
MR Measurement Accuracy				4		%
Temperature Measurement Accuracy				2		^{o}C
BHV Accuracy				5		%
BHV Gain			4.75	5	5.25	V/V

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

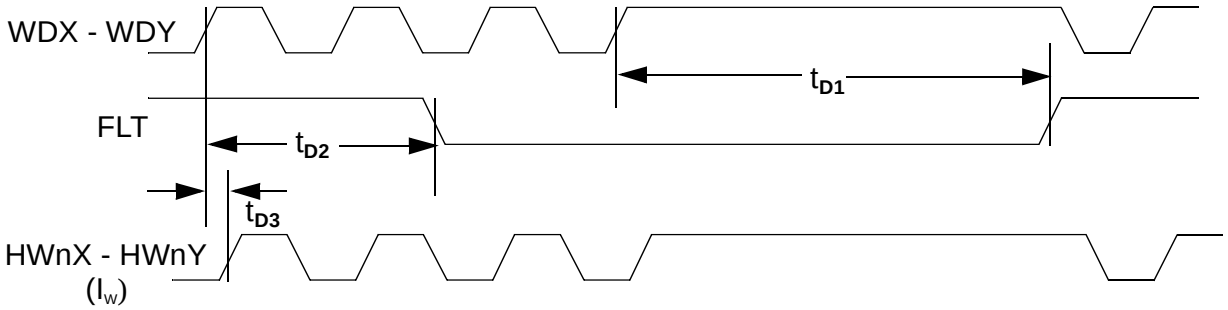
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		15		65	mA
Write Current Tolerance	ΔI_W	$15 < I_W < 65$ mA	-8		8	%
Write Servo Current Tolerance			-10		10	%
Differential Head Voltage Swing	V_{DH}	Open Head	6			V_{PP}
Unselected Head Transition Current	I_{UH}				1	mA_{pk}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			nS
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	nS
Write Data Input Terminal Resistor	w_{RIH}	Voltage mode write data input only		150		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	nS
R/WN to Read Mode	t_{WR}	To 90% of data envelope, DC Offset Level within 30 mV			300	nS
		To 10% of I_W envelope			50	nS
Idle to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 30 mV			5	µS
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 30 mV, **TBD** - Fixed I_{MR}.			1	µS
		To 90% of envelope, DC Offset Level within 30 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			3	µS
Idle (16th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			50	nS
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µS
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		nS
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		nS
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5nS rise/fall time, L_H=0, R_H=**TBD**			100	pS
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=70nH, R_H=10Ω.		500	**TBD**	pS
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.			**TBD**	nS
Read to Servo Write		From 50%R/WN to 90% I_W			50	nS
Read to Servo Write Head Turn-on Variation					**TBD**	nS
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µS
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	nS

1. See Figure 51 for the write mode timing diagram.

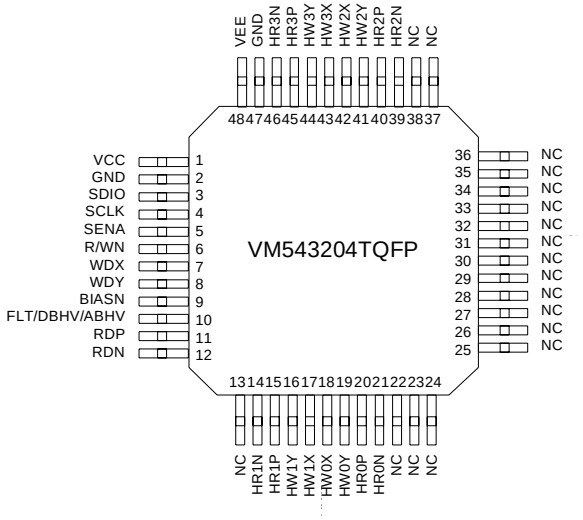


In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 51 Write Mode Timing Diagram *

VM5432 PACKAGING

4-CHANNEL CONNECTION DIAGRAM



4-Channel
48-lead TQFP

VTC Inc.
Value The Customer™

VM5435

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 600 Mbits/sec
  - Designed for Use With Four-Terminal Recording Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 8 Channels Available
  - Fault Detect Capability
  - Servo Write Capability
- *High Performance Reader*
  - Voltage Sense Configuration
  - Voltage/Current Bias Selectable
  - Reader Bias Current/Voltage 6-bit DAC, 2 - 10 mA Range
  - Programmable Read Voltage Gain (112 V/V to 316 V/V Typical)
  - Input Noise Voltage = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Noise Current = 8 pA/$\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Bandwidths in Excess of 350 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 50 mA Range
  - Rise Time = 500 ps Typical (10-90%, L_{HEAD} = 40 nH, Z_0 = 50Ω, I_W = 50 mA)

DESCRIPTION

The VM5435 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM5435 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

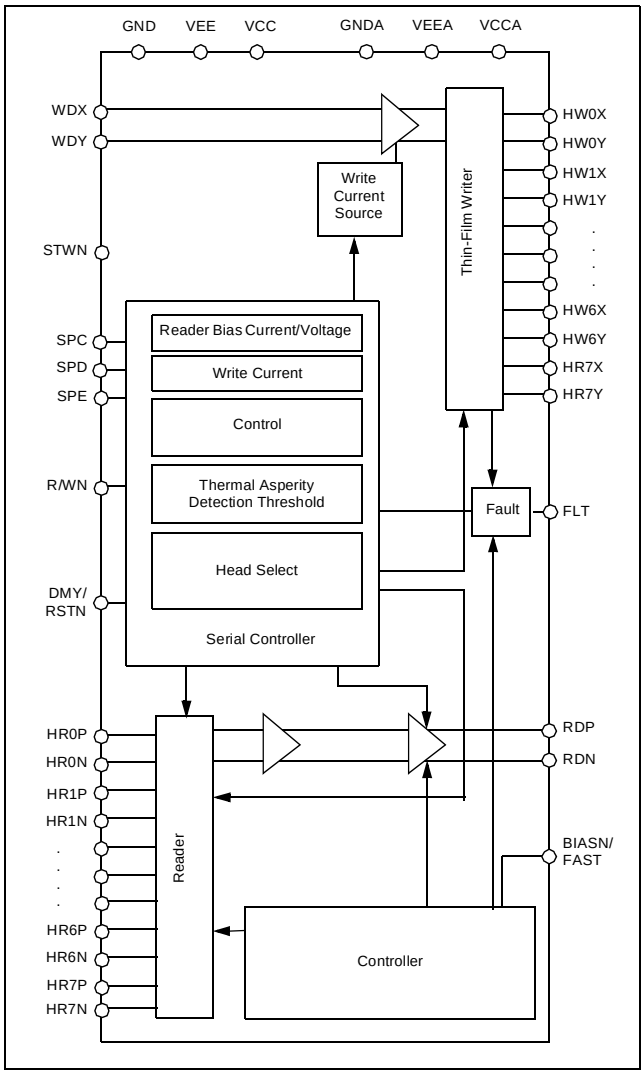
Programmability of the VM5435 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, thermal asperity detection threshold, and fault modes.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM5435 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. When deselected, the device enters an standby mode which reduces the power dissipation.

The VM5435 is available in 4 or 8-channel bump die form for chip-on-flex applications, and in 4, 6 or 8-channel packages. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR}, in Voltage Bias mode 17mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -5V ± 5%

Write Current, I_W ..... 10 - 50 mA
Write Head Inductance, L_W ..... 25 nH
Write Head Resistance, R_W ..... 5 - 15 Ω
Read Bias:
- Current, I_{MR} ..... 2 - 10 mA
- Voltage, V_{MR} ..... 100 - 500 mV

Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM5435 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 153 for protocol descriptions, bit descriptions and timing information.

OPERATING MODES

Table 66 briefly defines the register selects and pin states required to enter a specific operating mode. See the mode descriptions below and the Serial Register Data Bit Descriptions on page 156 for more detailed information.

Note: At initial power-up, both the DMY/RSTN pin and the DUMMYN bit (1:<D5>) must be set to enable the preamp an active mode. The DMY/RSTN pin is pulled high in package versions and pulled low in die versions of this device.

Table 66 Mode Selects

MODE	*MODE0 9:<D0>*	*MODE1 9:<D1>*	*STWHD 0:<D7>*	*STWN*	*A1*	*A2*
Sleep	0	0	0	0	0	0
Sleep	0	0	0	1	0	0
Sleep	0	0	1	0	0	0
Sleep	0	0	1	1	0	0
Active R/W	0	1	0	0	0	0
Active R/W	0	1	0	1	0	0
Active R/W	0	1	1	0	0	0
Active R/W	0	1	1	1	0	0
Standby	1	0	0	0	0	0
Standby	1	0	0	1	0	0
Standby	1	0	1	0	0	0
Standby	1	0	1	1	0	0
Test R/W [1]	1	1	0	0	0	0
Test R/W [1]	1	1	0	1	0	0
Test R/W [1]	1	1	1	0	0	0
Test R/W [1]	1	1	1	1	0	0
Standby	0	0	0	0	1	1
Standby	0	0	0	1	1	1
Standby	0	0	1	0	1	1
Standby	0	0	1	1	1	1
STW [2] 1 Head	0	1	0	0	1	1
Standby	0	1	0	1	1	1
STW [2] 4 Heads	0	1	1	0	1	1
Standby	0	1	1	1	1	1
Standby	1	0	0	0	1	1
Standby	1	0	0	1	1	1
Standby	1	0	1	0	1	1
Standby	1	0	1	1	1	1
STW [2] 2 Heads	1	1	0	0	1	1
Standby	1	1	0	1	1	1
STW [2] All Heads	1	1	1	0	1	1
Standby	1	1	1	1	1	1

1. Entire read path is on during test write.
2. All preamps selected with Multiple Device Select inactive during servo write:
   See Notes 2 and 5 on page 156 regarding STW to a single head.
   See Notes 3 and 5 on page 156 regarding STW to two heads.
   See Notes 4 and 5 on page 156 regarding STW to four heads.
   See Note 5 on page 156 regarding STW to all heads.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature.

Read Head Resistance

The resistance of the MR head can be measured and digitally converted.

To perform the digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 70).
2) Set the RMR/TEMP bit (9:<D5>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (9:<D4>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)
4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 8:<D6-D0> = 0100000 the MR head resistance is 32 Ohms.

Note: MR bias current is always enabled in this mode (Range = 0 Ohms to 127 Ohms).

Die Temperature Monitoring

The die temperature range is 0^oC to 150^oC. To measure the die temperature:

1) Set RMR/TEMP (9:<D5>) high to enable the die temperature.
2) Set DIGON bit (9:<D4>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 8:<D6-D0> = 0100000 the die temperature is 38^oC (32^oC x 1.18).

$$T = 1.18k \qquad \textit{(eq. 28)}$$

where k = 0 - 127 and T is degrees Centigrade

Sleep Mode

In the sleep mode power consumption is minimized by inactivating all circuits, except the serial interface. The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN and RDP outputs switch to a high impedance state. In sleep mode the fault indicator is not active, and the serial register contents and reader output mode are set to default values.

Sleep mode is selected by setting Mode 0 and Mode 1 to 00 (9:<D1-D0>), see Tables 66 and 70.

Note: Always transition from Sleep to Standby mode 10 µs before entering an active mode.

Standby Mode

In the standby mode, power dissipation is reduced. The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN and RDP outputs switch to a high impedance state. The fault indicator is not active in standby mode.

Standby mode is selected by setting Mode 0 and Mode 1 to 01 (9:<D1-D0>), see Tables 66 and 70.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting Mode 0 and Mode 1 to 10 (9:<D1-D0>), see Tables 66 and 70.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM5435 uses the current-bias/voltage-sensing reader architecture. The magnitude of the reader bias current/voltage is set to the value programmed in 2:<D2-D7>. The equations below govern the read bias current/voltage magnitude:

$$\text{Current Mode} \quad I_{MR} = 2 + [k_{IMR} \cdot 0.127]\text{mA} \qquad \textit{(eq. 29)}$$

$$\text{Voltage Mode} \quad V_{MR} = 100 + [k_{IMR} \cdot 6.35]\text{mV} \qquad \textit{(eq. 30)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes: current or voltage. Current bias (1:<D7> = 0) is the default setting.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element by changing the I_{MR}. The applied value is programmed in 2:<D2-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT line indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 72.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 7:<D7-D4> as shown in Table 72. The default setting (0000) is to enable all faults.

Fault codes are cleared on power-up, during a system reset, or by writing to Register 9.

Reader Biasing in Read Mode

Reader bias to the selected head can be disabled in read mode by setting the BFCTL = 0 (1:<D0>) and the BIASN/FAST pin high.

Note: Reader bias must be enabled 5µs before reading data.

Read Gain

The default gain is 112 V/V with a head resistance of 50Ω. Read Gain may be increased in 3dB increments using a 2-digit binary code in 2:<D0-D1>. The formula that describes the actual gain is shown below:

$$GAIN = \frac{475}{420 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 31)}$$

k_{GAIN} = 0-3

Fast Mode

Taking the BIASN/FAST pin low, while BFCTL = 1 (1:<D0>), selects the normal read bandwidth for the head specified in LFP (3:<D0-D1>).

Setting the BIASN/FAST pin high selects read bandwidth with raised lower corner. The raised lower corner is set to 8 MHz in fast mode.

Thermal Asperity Detection and Recovery

Detection

Setting the TAT bit high (5:<D6>) enables thermal asperity threshold setting. The TRANGE bit (5:<D7) selects the range, (Low or High), for the TA threshold (TAT).

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the Voltage Threshold (V_{TAT}) is governed by the following equations and is set in 5:<D4-D0>:

$$\text{TRANGE} = 0$$
$$V_{TAT} = 0.4 + [k_{TAT} \cdot 0.18]\text{mV} \qquad \textit{(eq. 32)}$$

$$\text{TRANGE} = 1$$
$$V_{TAT} = 3.4 + [k_{TAT} \cdot 0.18]\text{mV} \qquad \textit{(eq. 33)}$$

V_{TAT} represents the TA threshold (input-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

Fast Recovery

Setting the TA Compensation (TAC) bit high (5:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised from a nominal value to 8 MHz. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 5:<D6>.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting Mode 0 and Mode 1 to 10 (9:<D1-D0>), see Tables 66 and 70.

The magnitude of the write current is determined by the write current registers (4:<D3-D7>). The following equation governs the write current magnitude:

$$I_W = 10 + (k_{IW} \cdot 1.29)\text{mA} \qquad \textit{(eq. 34)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 56 for the timing diagram.

Write Current DAC

Register 4:<D3-D7> represent the binary equivalent of the DAC setting (0-31, LSB first).

Reader Biasing in Write Mode

Taking the BIASN/FAST pin low in write mode, while BFCTL = 0 (1:<D0>), enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. The common-mode voltage at the reader outputs is maintained by other circuitry which substantially reduces the write-to-read transition time.

Note: Reader bias must be enabled 5µs before switching to read mode from write mode.

Write Data Modes

Setting the WVORI bit low (1:<D1>) initiates the Voltage Write mode. Setting the WVORI bit high initiates the Current Write mode.

In voltage write mode the writer switches on PECL input voltage levels. In current write mode the writer switching is dependent on the amount of current that is sinking from the write data inputs.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT line indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 70.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 7:<D7-D4> as shown in Table 70. The default setting (0000) is to enable all faults.

Fault codes are cleared on power-up, during a system reset, or by writing to register 9.

Write Head Shorted to Read Head Detection

In the write mode, setting HWSHD = 1 (9:<D7>) checks for a write head shorted to a read head. To perform write head short detection:

1) Set HWSHD = 1 (9:<D7>).
2) Place the device in write mode (see Table 66).
3) Select the desired head.
4) Monitor the FLT line: A TTL high level indicates a fault.
5) If a fault condition exists, the contents of the FCODEn registers (7:<D0-D3>) indicate the fault present.

Note: This mode is for test purposes only.

Reset/Dummy Mode

Reset or Dummy mode provides data protection and recovery to known register states or protection of register states should an error occur. The programmed mode is triggered by setting the DMY/RSTN pin low.

If Reset mode is selected (9:<D2> = 0) and the DMY/RSTN pin is set low, the following sequence occurs:

1) Set all register bits to defaults.
2) Remove write current.
3) Place device in sleep mode.

If Dummy mode is selected (9:<D2> = 1) and the DMY/RSTN pin is set low, the following sequence occurs:

1) Retain all register bits settings.
2) Maintain write current level.
3) Select dummy head.

Note: The DMY/RSTN pin is pulled high in package versions and pulled low in die versions of this device.

Servo Write Mode

In the servo write mode, all heads may simultaneously write. Table 70 indicates how heads can be selected for individual or simultaneous writing.

Setting the MODE bits (9:<D1-D0>) to a non-zero value and holding the STWN pin low places the preamp in servo write mode (see Table 66).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

SERIAL PORT

Serial Interface

The VM5435 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 68 and 69 for a bit description.

The serial interface has two input lines, SPC (serial port clock) and SPE (serial port enable), and one bidirectional input/output line SPD (serial port data). The SPC line is used as reference for clocking data into and out-of SPD. The SPE line is used to activate the SPC and SPD lines and power-up the associated circuitry. When SPE is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SPE to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 52.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one command bit <A0> (high for read, low for write),
  - two chip select bits <A2-A1> (that select the operating mode of the device, see levels in Table 66), and
  - five register address bits <A7-A3> (A7 is unused at present).
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SPE). Data present on the serial data input/output line (SPD) will be latched-in on the rising edge of SPC. During a write sequence this will continue for 16 cycles; on the falling edge of SPE, the data will be written to the addressed register.

During a read sequence, SPD will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SPD). At this time <D0> will be presented and data will continue to be presented on the SPD line on subsequent falling edges of SPC.

Note: Data transfers should only take place in standby or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 68 and 69 for a bit description. See Table 67, and Figures 53 and 54 for serial interface timing information.

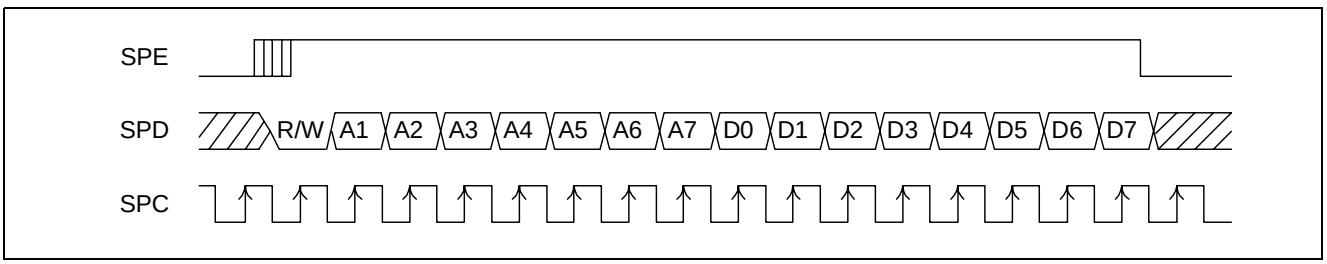


Figure 52 Write Protocol for 3-Write Serial Port Interface

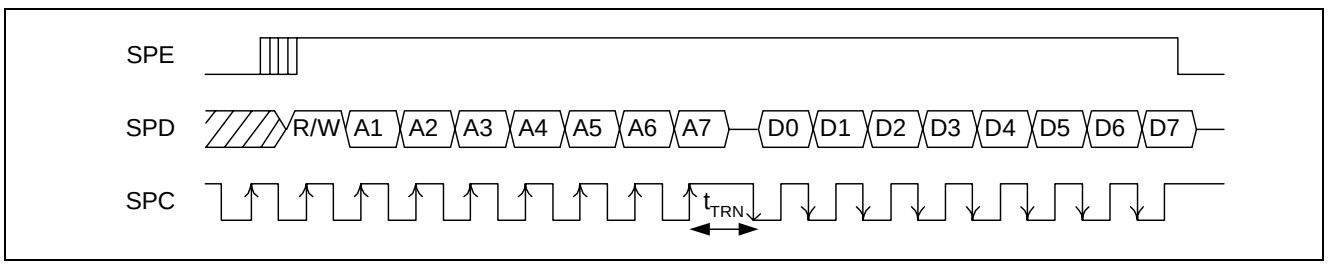


Figure 53 Read Protocol for 3-Wire Serial Port Interface

Table 67 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SPC) rate, write				40	MHz
SPE to SPC delay	T_{sens}	5			nS
SPD setup time, write	T_{wds}	5			nS
SPD delay time, read (setup)	T_{rds}	5		25	nS
SPD hold time	T_{dh}	3.5			nS
SPC cycle time	T_{c}	25			nS
SPC high time	T_{ckh}	10			nS
SPC low time	T_{ckl}	10			nS
SPE hold time	T_{shld}	0			nS
Time between I/O operations	T_{sl}	75			nS
Time to activate SDIO	T_{act} (after clock)	2.5		8	nS
Duration of SPE (read)	T_{rd}	400			nS
Duration of SPE (write)	T_{wt}	400			nS

Note: SENA assertion level is high.

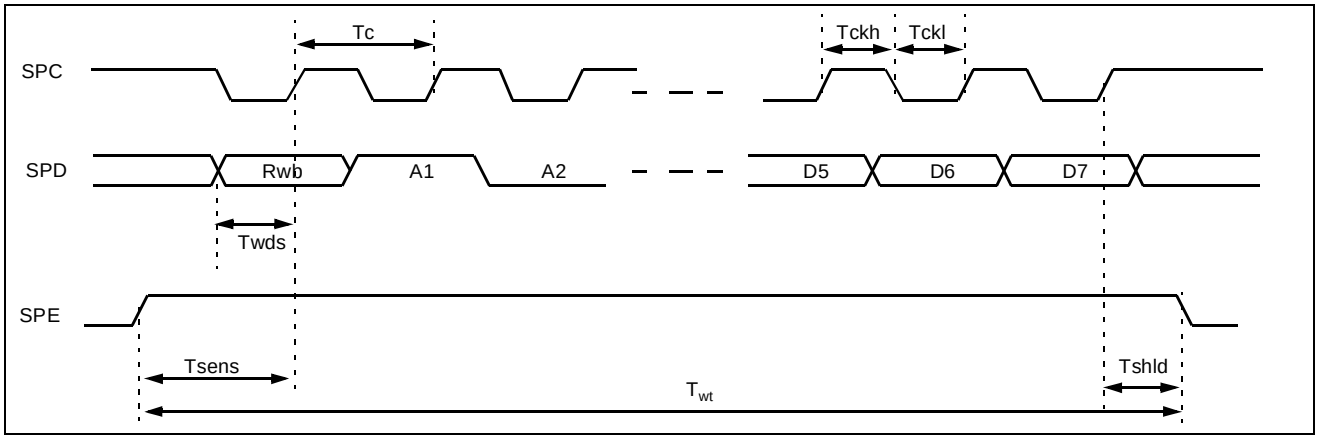


Figure 54 Serial Port Timing - Write Operation

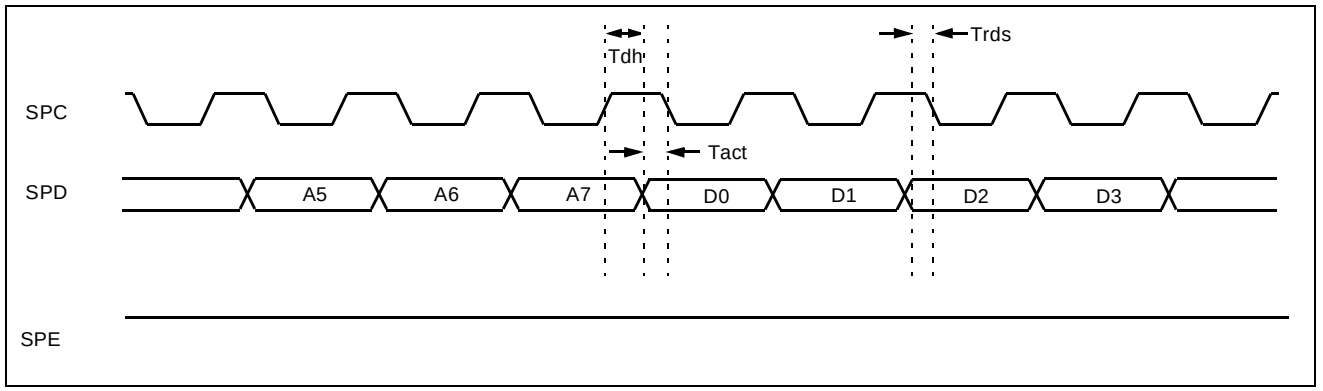


Figure 55 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 68 lists the serial address for each register.Table 69 lists the data contents of the registers. A description of the individual bits is provided in Table 70.

Table 68 Serial Interface Addressing

Register #	Register Address Bits					Preamp Address Bits [1]		R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	X	0	0	0	0	See Table 66 on page 150 for preamp mode selects.		0 = write 1 = read
1	X	0	0	0	1			
2	X	0	0	1	0			
3	X	0	0	1	1			
4	X	0	1	0	0			
5	X	0	1	0	1			
6	X	0	1	1	0			
7	X	0	1	1	1			
8	X	1	0	0	0			
9	X	1	0	0	1			
10	Not Accessible							
11	X	1	0	1	1			
12	Not Accessible							
13	Not Accessible							
14	Not Accessible							
15	X	1	1	1	1			

1. The address bits <A1 and <A2>, along with register and pin settings, select the operating mode of the device. See Table 66, “Mode Selects,” on page 150.

Table 69 Serial Interface Bit Map

Function	Register	Data Bits							
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Head/Chip Select	0	LSC0	LSC1	SELF	SELT	HS0	HS1	HS2	STWHD
Control	1	BFCTL	WVORI	1	2	2	DUMMYN	2	I/V
Reader Bias/Gain	2	GAIN0	GAIN1	IMR0	IMR1	IMR2	IMR3	IMR4	IMR5
Bandwidth	3	LFP0	LFP1	HFP0	HFP1	2	2	2	2
Writer Bias	4	WCOS0	WCOS1	WCOS2	IW0	IW1	IW2	IW3	IW4
Thermal Asperity	5	TAT0	TAT1	TAT2	TAT3	TAT4	TAC	TAT	TRANGE
Channel/Vendor ID	6	CHNL	VEND0	VEND1	VEND2	VEND3	REV0	REV1	REV2
Fault Reporting/Head Testing	7	FCODE0	FCODE1	FCODE2	FCODE3	FLT0	FLT1	FLT2	HWSHD
MR/Temp	8	DSTR0	DSTR1	DSTR2	DSTR3	DSTR4	DSTR5	DSTR6	2
Operating Modes	9	MODE0	MODE1	RSTDMY	SIOLVL	DIGON	RMR/ TEMP	2	2
Not Accessible	10	2	3	3	3	3	3	3	3
Undershoot	11	2	2	2	2	2	WCUS0	WCUS1	WCUS2
Not Accessible	12	3	3	3	3	3	3	3	3
Not Accessible	13	3	3	3	3	3	3	3	3
Not Accessible	14	3	3	3	3	3	3	3	3
Test	15	TTOSC	TEST	TEST	TEST	TEST	2	2	2

1. Reserved
2. Not accessible via serial register.

Table 70 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
0	D0-D1	Logic Select Chip	LSCn	These bits are hardwired low internal to the device. See Table 66 on page 150 for preamp addressing selects.			
	D2	Illegal Multiple Device	SELF	0 = Valid multiple device selection (MDS). 1 = Illegal multiple device selection detected.			
	D3	Multiple Device Select	SELT	0 = Multiple device selection (MDS) inactive. 1 = Multiple device selection active.			
	D4-D6	Head Select	HSn	Binary selection of Head Address	HS2	HS1	HS0
				Head Select	0:<D6>	0:<D5>	0:<D4>
				0	0	0	0
				1	0	0	1
				2	0	1	0
				3	0	1	1
				4	1	0	0
				5	1	0	1
				6	1	1	0
				7	1	1	1
	D7	Servo Track Write Head Select	STWHD	Head(s) to servo track write are selected in HS2 - HS0 (0:<D4-D6>): 0 = Servo write one or two heads per preamp. 1 = Servo write four or more heads per preamp. Note: This bit is valid only when the STWN pin is low. Multiple inputs are required for this selection: See Table 66 on page 150 and the items below for details about the settings. 2) A1 and A2 both high is not a operational preamplifier configuration, except for servo operations (STWN = 0). Setting <A1> and <A2> high while STWN is low allows all preamplifiers to be accessed by a single serial write operation. Note that serial read operations are always limited to a single preamplifier. 3) Head k is selected via HSn (0:<D4-D6>) when k = 0 to 7. 4) Heads k and k +1 are selected in write mode. Selecting the last head (3 or 7) results in wrapping to include head 0. Head k is selected in read mode when k = 0 to 7. 5) If Heads 0-3 are selected, heads 0-3 (BANK0) are servo written. If Heads 4-7 are selected, heads 4-7(BANK1) are servo written. 6) The selected heads become active when the device switches from servo write mode to read mode.			

Table 70 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
1	D0	Bias/Fast Control	BFCTL	0 = Reader Bias in Write Mode, depending on BIASN/FAST pin state. - BIASN/FAST pin low: Read Head bias current/voltage On. - BIASN/FAST pin high: Read Head bias current/voltage Off. 1 = Fast Response Mode, depending on logic level of BIASN/FAST pin. - BIASN/FAST pin low: Normal Response. - BIASN/FAST pin high: Fast Response, with lower corner frequency raised to 8 MHz. Note: Bias current/voltage level is set in 2:<D2-D7>.		
	D1	Write Data Control	WVORI	0 = Voltage mode write data inputs selected. 1 = Current mode write data inputs selected.		
	D2-D4	Reserved				
	D5	Dummy Head Load	DUMMYN	0 = Dummy resistive load selected. 1 = Valid head selected according to HSn (0:<D4-D6>).		
	D6	Reserved				
	D7	Bias Mode	I/V	0 = Current Biasing. 1 = Voltage Biasing. Note: Bias current/voltage is always on when BFCTL=1. FAST is off when BFCTL=0.		
2	D0-D1	Gain Control	GAINn	Binary selection of Reader Gain:	GAIN1	GAIN0
				Gain Select	2:<D1>	2:<D0>
				112 V/V	0	0
				158 V/V	0	1
				224 V/V	1	0
				316 V/V	1	1
	D2-D7	Reader Bias Level	I/VMRn	Binary selection of Reader Current or Voltage Bias: Current: 2 mA (000000) to 10 mA (111111) in 0.127 mA increments. Voltage: 100 (000000) to 500 mV (111111) in 6.35 mV increments.		
3	D0-D1	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Corner in normal read mode only:	LFP1	LFP0
				Low Frequency Bandwidth	3:<D1>	3:<D0>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				4 MHz	1	1
	D2-D3	High Frequency Gain Attenuation	HFPn	Binary selection of High Frequency Gain Attenuation:	HFP1	HFP0
				High Frequency Gain Attenuation	3:<D3>	3:<D2>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
	D4-D7	Reserved				

Table 70 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
4	D0-D2	Write Current Overshoot	WCOSn	Binary selection of Write Current Overshoot Control	WCOS2	WCOS1	WCOS0
				Write Current Overshoot %	4:<D2>	4:<D1>	4:<D0>
				TBD	0	0	0
				TBD	0	0	1
				TBD	0	1	0
				TBD	0	1	1
				TBD	1	0	0
				TBD	1	0	1
				TBD	1	1	0
				TBD	1	1	1
				Note: Write Current Overshoot percentage is specified as a ratio of overshoot to base-to-peak current.			
	D3-D7	Write Current	IWn	Binary selection of Write Current: 10 mA (00000) to 50 mA (11111) in 1.29 mA increments.			
5	D0-D4	Thermal Asperity Threshold	TATn	Binary selection of Thermal Asperity Threshold: Low TA Range = 0.4 mV (00000) to 6.0 mV (11111) in increments of 0.180 mV. High TA Range = 3.4 mV (00000) to 9.0 mV (11111) in increments of 0.180 mV. Note: TA Range (low or high) is selected in 5:<D7>.			
	D5	Thermal Asperity Compensation	TAC	0 = No Automatic fast mode TA Compensation selected. 1 = Automatic fast mode TA Compensation selected. Note: TA Detection must be enabled in 5:<D6>.			
	D6	Detect TAT	TAT	0 = Disable TA Threshold Detection. 1 = Enable TA Threshold Detection.			
	D7	Thermal Asperity Range Shift	TRANGE	0 = Low TA Range (0.4 mV to 6.0 mV) 1 = High TA Range (3.4 mV to 9.0 mV) Note: Threshold value is selected in 5:<D0-D4>.			
6	D0	Channel Count	CHNL	Channel Count of Part: 0 = 4 Channel 1 = 6 or 8 Channel, dependent on TQFP package labeling (die is 8).			
	D1-D4	Part ID	VENDn	Vendor ID: VTC = 1001			
	D5-D7	Revision of Part		Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1after exceeding 8.			

Table 70 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
7	D0-D3	Fault Code	FCODEn	Binary code of Fault(s) See Table 72.			
	D4-D6	Fault Mask	FLTn	Binary selection of Fault Conditions to Disable	FLT2	LFT1	FLT0
				Fault Reporting	7:<D6>	7:<D5>	7:<D4>
				Report all faults	0	0	0
				Disable power supply fault	0	0	1
				Disable temperature fault	0	1	0
				Disable Head open or shorted fault	0	1	1
				Disable write frequency low fault	1	0	0
				Disable MR overcurrent fault	1	0	1
				Disable TA fault	1	1	0
				Disable all faults	1	1	1
	D7	Write Head Shorted	HWSHD	0 = Disable detection of a shorted write head test. 1 = Enable detection of a shorted write head test. Note: This is a VTC test. It has no effect or relationship to the Write Head Shorted fault code (7:<D0-D3> = 0111) or its Fault Masking pattern (7:<D4-D6> = 011).			
8	D0-D6	Digital Storage	DSTRn	Digital storage for the resistance of the reader head or the junction temperature of the device. See Test Modes on page 151. Measurement is selected in 9:<D5>.			
	D7	Reserved					
9	D0-D1	Operating Mode	MODEn	Binary selection of the Operating Mode for the device: Table 66, “Mode Selects,” on page 150 defines the bit selections that select a specific mode. See the section titled "OPERATING MODES" for a more detailed explanation of each mode.			
	D2	Dummy/Reset	DMY/ RST	0 = Selects Reset Mode for DMY/RSTN pin. - If DMY/RSTN pin is low: Reset Mode sequence is: 1. Set all register bits to defaults. 2. Remove write current. 3. Place device in sleep mode. - If DMY/RSTN pin is high: Normal preamp functions available. 1 = Selects Dummy Mode for DMY/RSTN pin. - If DMY/RSTN pin is low: Dummy Mode sequence is: 1. Retain all register bit settings. 2. Maintain Write Current level. 3. Select Dummy Head. - If DMY/RSTN pin is high: Normal preamp functions available. Note: The DMY/RSTN pin is pulled high in package versions and pulled low in die versions of this device.			
	D3	Serial I/O Level	SERLVL	0 = Serial I/O readback data voltage will not exceed 3V. 1 = Serial I/O readback data voltage will not exceed 5V.			
	D4	Internal Digital Conversion	DIGON	0 = Digital Conversion OFF 1 = Digital Conversion ON Note: DIGON resets to off when conversion is complete			
	D5	RMR or Temperature	RMR/ TEMP	0 = Digital resistance (R_{MR}) selected 1 = Digital junction temperature selected			
	D6-D7	Reserved					
10	D0-D7	Not Accessible via Serial Register					

Table 70 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description			
11	D0-D4	Reserved					
	D5-D7	Write Current Undershoot	WCUSn	Binary selection of Write Current Undershoot Control	WCUS2	WCUS1	WCUS0
				Write Current Undershoot	11:<D7>	11:<D6>	11:<D5>
				None	0	0	0
				TBD	0	0	1
				TBD	0	1	0
				TBD	0	1	1
				TBD	1	0	0
				TBD	1	0	1
				TBD	1	1	0
				TBD	1	1	1
12		Not Accessible via Serial Register					
13		Not Accessible via Serial Register					
14		Not Accessible via Serial Register					
15		Test					

Table 71 Power-On Reset Register Values

Function	Register Number	Power-on Reset Value <D0-D7>
Head/Chip Select	0	<0000 0000>
Control	1	<0000 0000>
Reader Bias/Gain	2	<0000 0000>
Bandwidth	3	<0000 0000>
Writer Bias	4	<0010 0000>
Thermal Asperity	5	<0000 0000>
Channel/Vendor ID	6	<cvvv vnnn> [1]
Fault Reporting/Head Testing	7	<0000 0000>
MR/Temp	8	<0000 0000>
Operating Modes	9	<0000 0[2]00>
Not Accessible	10	N/A
Undershoot	11	<0000 0001>
Not Accessible	12	N/A
Not Accessible	13	N/A
Not Accessible	14	N/A
Test	15	<0000 0000>

1. Where c = channel count of part, vvvv is the assigned vendor identification number and nnn = revision level of device.
2. The DMY/RSTN pin is pulled high in package versions and pulled low in die versions of this device.

Table 72 Fault Conditions and Codes

Fault Code [1] 7:<D3-D0>	*Fault*	*Valid Mode(s)*	*Conditions*
0000	No Fault	Read or Write	
0001	Reserved	-	
0010	MR Overcurrent	Read	
0011	Thermal Asperity Detected	Read	
0100	Read Head Open	Read	
0101	Reserved	-	
0110	WDI Frequency Low	Write	F_{WDI} < 2 MHz
0111	Write Head Open/Shorted to Ground	Write	
1000	Reserved	-	
1001	Reserved	-	
1010	Write to Read Short	Write	Test Mode
1011	Low V_{CC} or Low V_{EE}	Read or Write	V_{CC} < +3.9 V typical V_{EE} < -3.9 V typical
1100	Read Head Shorted Across Poles	Read	
1101	Illegal Head Select	Read or Write	Where applicable
1110	Illegal Multiple Device Select	Test	
1111	Overtemperature	Read or Write	T_j > 140°C

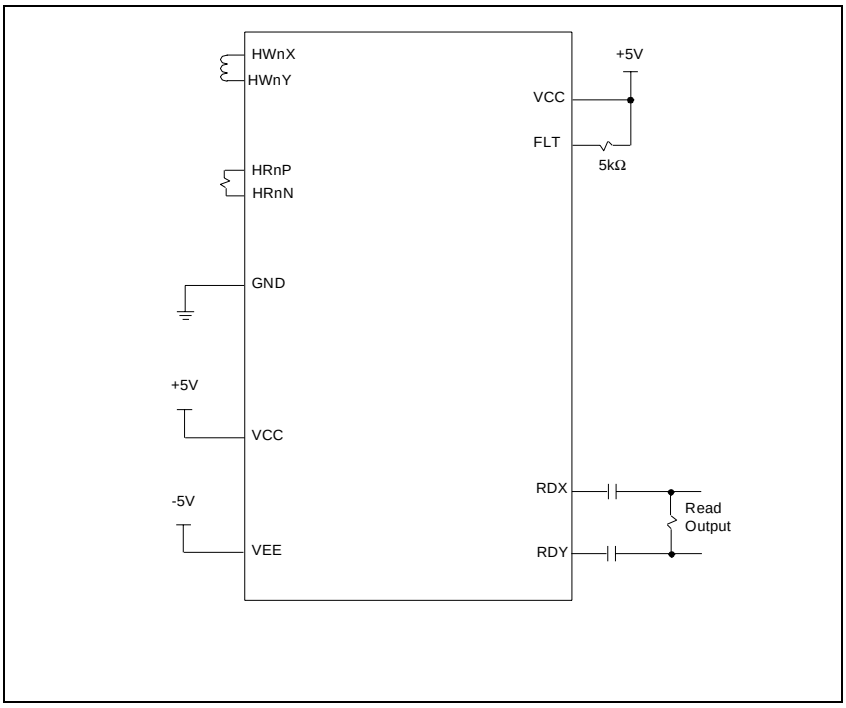
1. Fault codes may be disabled by setting 7:<D4-D6> as described in Table 70.

PIN FUNCTION LIST AND DESCRIPTION

Signal	*Input /Output*	*Logic Level Default*	*Description*
BIASN/FAST	I [1]	low	Bias/Fast Enable: Bias/Fast Control bit (1:<D0>) sets the function of the pin, see Table 70.
DMY/RSTN	I [1]	high: package low: die	Reset/Dummy Select: Register 9:<D2> selects the pin function. See Table 70 for bit selections.
FLT	O [1]		Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
GND	[1]		Ground
HR0N-HR7N	I		Read head connections, negative end.
HR0P-HR7P	I		Read head connections, positive end.
HW0X-HW7X	O		Thin-Film write head connections, positive end.
HW0Y-HW7Y	O		Thin-Film write head connections, negative end
R/$\overline{W}$	I [1]	high	Read/Write: A TTL low level enables write mode.
RDP, RDN	O [1]		Read Data: Differential read signal outputs.
SPC	I [1]	low	Serial Clock: Serial port clock; see Figures 52 and 53.
SPD	I/O [1]	low	Serial Data: Serial port data; see Figures 52 and 53.
SPE	I [1]	low	Serial Enable: Serial port enable; see Figures 52 and 53.
STWN	I	high	Servo Track Write: A TTL low level enables servo write mode.
VCC	[1]		+5.0V supply
VEE	[1]		-5.0V supply
WDX, WDY	I [1]	high	Differential Pseudo-ECL write data inputs.

1. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in standby or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Standby Mode		15	**TBD**	
		Sleep Mode			**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Standby Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Standby Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	mA
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%	3.6	3.8	4.0	V
V_{EE} Fault Threshold	V_{ETH}	Hysteresis = 100mV ±10%	-4.0	-3.8	-3.6	V
High Level WDATA		PECL[1]	1.9		V_{CC}	V
		Current Mode (sink)	0	100	250	µA
Low Level WDATA		PECL[1]	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	1.2	1.6	2	mA
WDATA PECL swing		Voltage mode differential [1]	0.4		0.750	V_{pp}
Voltage compliance for WDATA		CMM of inputs when in current mode			V_{CC} -2.3	V

1. Differential V_{PP} swing from 0.4V to 1.5V and the common mode should be such that for any of the two states the maximum high < VCC, and the minimum low > 3V.

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 50Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		112		V/V
		Gain Bits = 11		316		
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB, BW = 11	350		**TBD**	
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00	**TBD**	1	**TBD**	MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		$nV/\sqrt{Hz}$
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		$pA/\sqrt{Hz}$
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}	**TBD**		2	4	pF
Differential Input Resistance	R_{IN}			420		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	40			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			
Power Supply Rejection	PSRR	100mV_{pp} on VCC or VEE, 10 MHz < f < 200 MHz	40			dB
		100mV_{pp} on VCC or VEE, 1 MHz < f < 10 MHz	40			
		100mV_{pp} on VCC or VEE, f < 100 kHz	60			
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV_{pp}, 1 MHz < f < 200 MHz	50			dB

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 50Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Rejection of SCLK and SDIO		100 mV_{pp} on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			200	mV
Reader Head Resistance	R_{MR}		25	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Overshoot					2.5	%
TA Detection Response Time		TA occurred to FLT active		20	40	ns
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		ns
MR Measurement Accuracy				4		%
Temperature Measurement Accuracy				2		^oC
BHV Gain			4.75	5	5.25	V/V

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WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

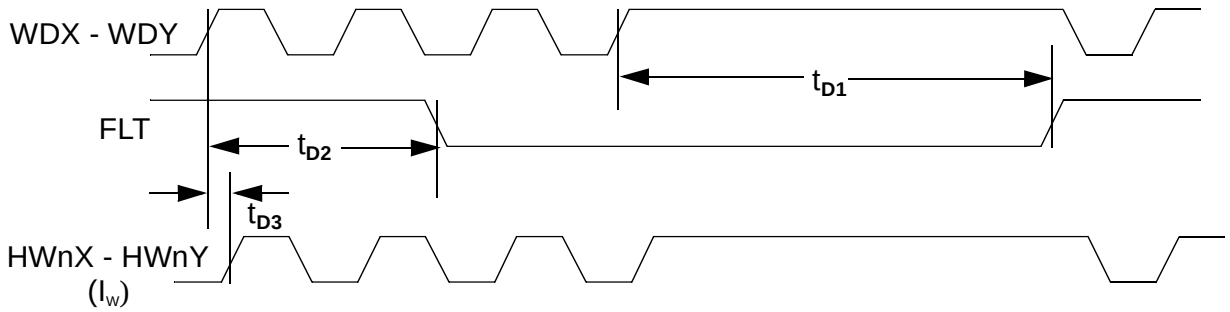
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		10		50	mA
Write Current Tolerance	ΔI_W	$10 < I_W < 50$ mA	-8		8	%
Write Servo Current Tolerance			-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head	6			V_{PP}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			ns
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	ns
Write Data Input Terminal Resistor	w_{RIH}	Voltage mode Preamp active		120		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	ns
R/WN to Read Mode	t_{WR}	To 90% of data envelope			175	ns
		To 10% of I_W envelope			50	ns
Standby to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 10 mV			5	µs
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 10 mV, **TBD** - Fixed I_{MR}.			1	µs
		To 90% of envelope, DC Offset Level within 10 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			1	µs
Standby (16th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			50	ns
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		ns
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5ns rise/fall time, L_H=0, R_H=**TBD**			100	ps
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=40nH, R_H=10Ω.		500		ps
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.		**TBD**		ns
Read to Servo Write		From 50%R/WN to 90% I_W		**TBD**	50	ns
Read to Servo Write Head Turn-on Variation					**TBD**	ns
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µs
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	ns
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA		**TBD**		ns

1. See Figure 56 for the write mode timing diagram.



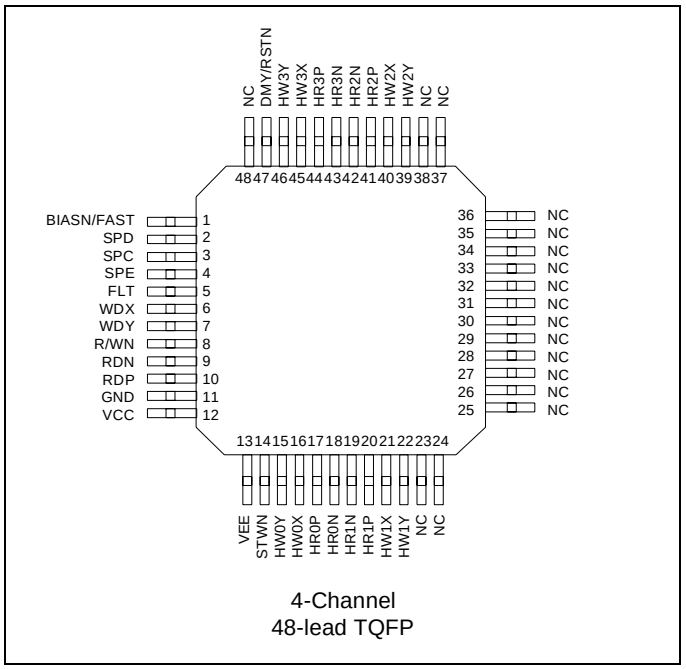
In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 56 Write Mode Timing Diagram *

PACKAGING

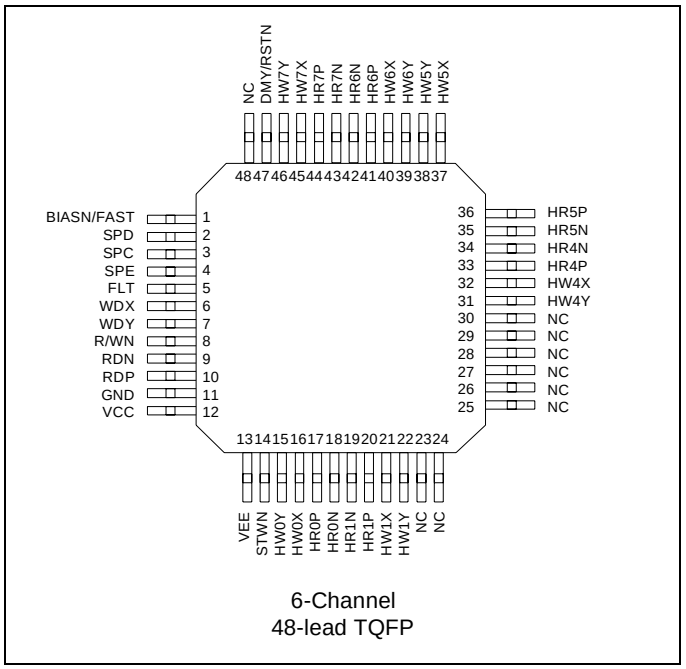
VM5435

4-CHANNEL CONNECTION DIAGRAM



4-Channel
48-lead TQFP

6-CHANNEL CONNECTION DIAGRAM



6-Channel
48-lead TQFP

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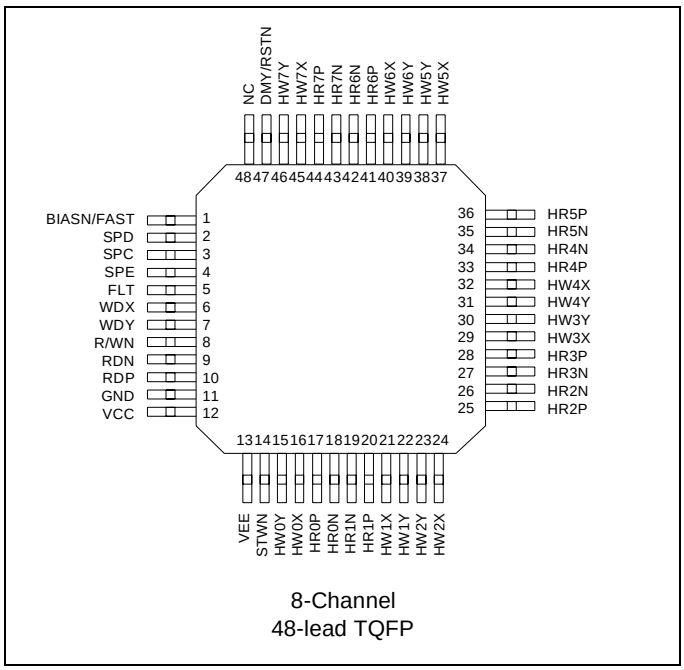
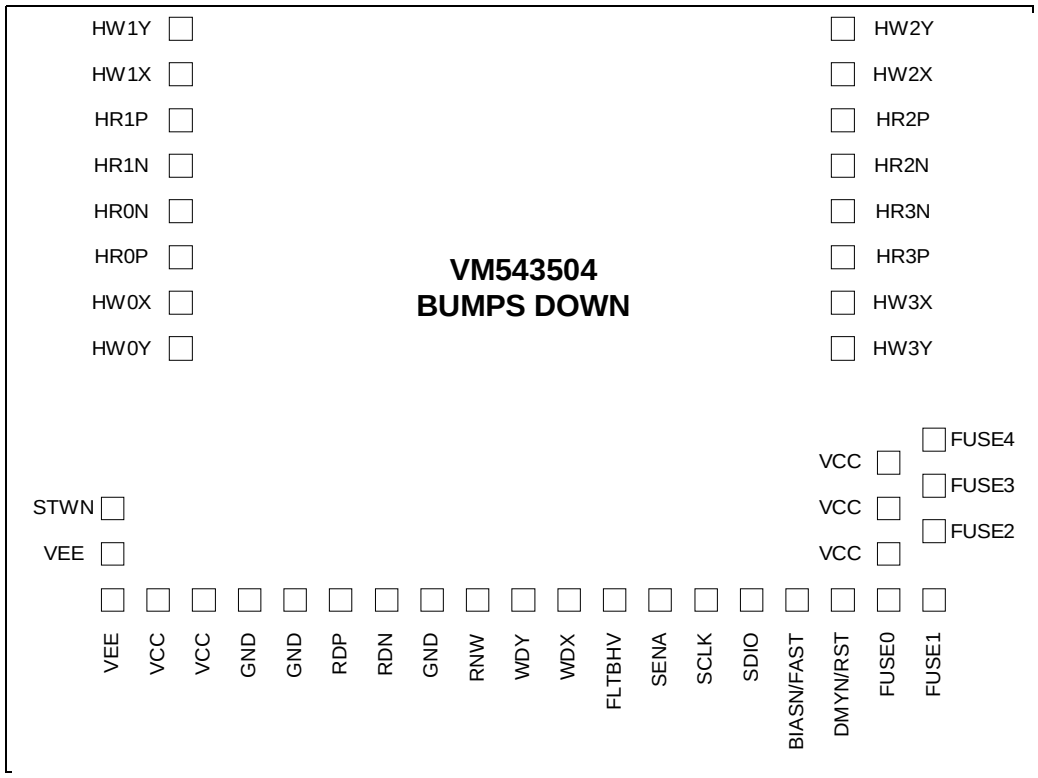
8-CHANNEL CONNECTION DIAGRAM



8-Channel
48-lead TQFP

DIE PAD ORIENTATION



1) Provide adequate space (≥22 mil pad pitch) between adjacent pads for running a ground trace from under die to E-block ground.
2) Landing pads on flex are required for these pads, but power or ground should not be routed to these pads.

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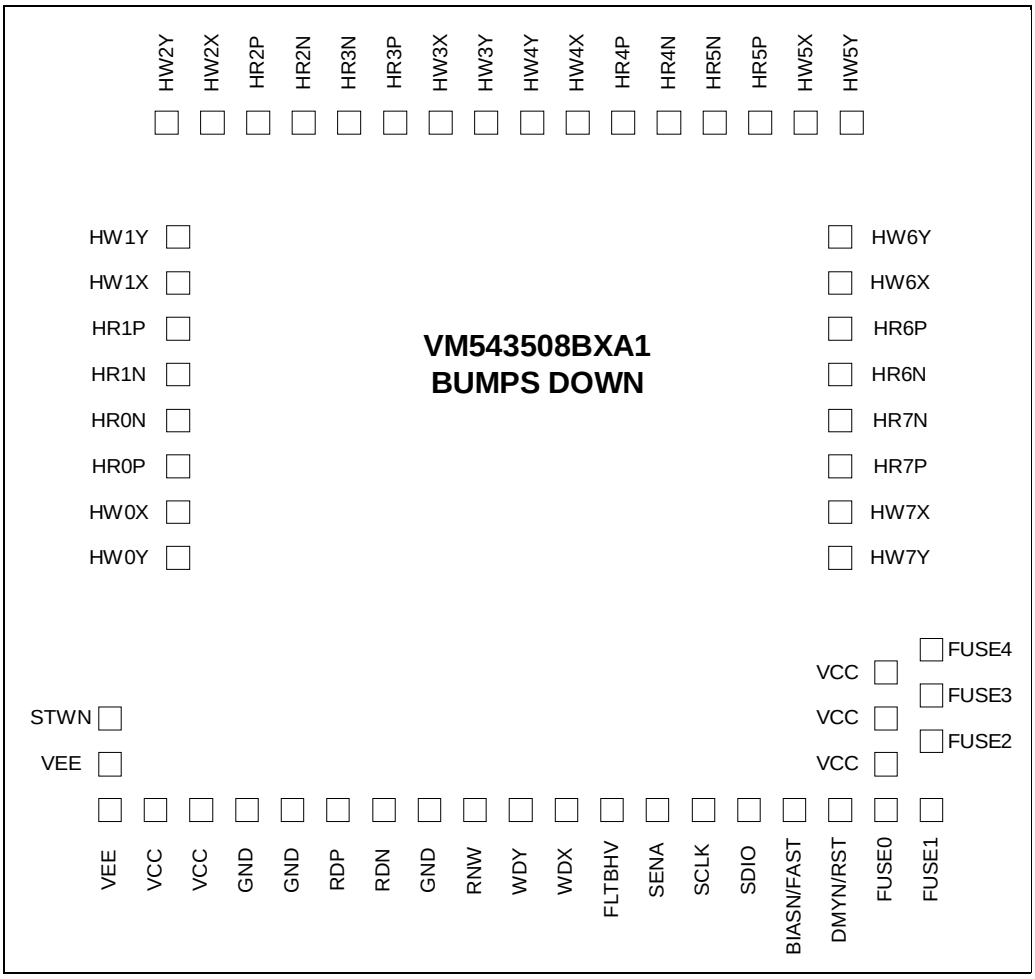

1) Provide adequate space (≥22 mil pad pitch) between adjacent pads for running a ground trace from under die to E-block ground.
2) Landing pads on flex are required for these pads, but power or ground should not be routed to these pads.

VM5435

4-CHANNEL PAD COORDINATES

Specific Characteristics

Die size: **TBD** x **TBD** Mils

Pad Coordinates for the VM5435 (in Mils) are “bump down.”

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN/FAST	47.736	-71.539	4x4
DMY/RSTN	55.736	-71.539	4x4
FLT	15.366	-71.539	4x4
FUSE0	63.831	-71.539	4x4oct
FUSE1	72.638	-71.539	4x4oct
FUSE2	72.638	-60.134	4x4oct
FUSE3	72.638	-51.449	4x4oct
FUSE4	72.638	-42.654	4x4oct
GND	-16.634	-71.539	4x4
GND	-40.634	-71.539	4x4
GND	-48.634	-71.539	4x4
HR0N	-57.520	3.346	4x4
HR0P	-57.520	-4.654	4x4
HR1N	-57.520	11.346	4x4
HR1P	-57.520	19.346	4x4
HR2N	57.520	11.346	4x4
HR2P	57.520	19.346	4x4
HR3N	57.520	3.346	4x4
HR3P	57.520	-4.654	4x4
HW0X	-57.520	-12.654	4x4
HW0Y	-57.520	-20.654	4x4
HW1X	-57.520	27.346	4x4
HW1Y	-57.520	35.346	4x4
HW2X	57.520	27.346	4x4
HW2Y	57.520	35.346	4x4
HW3X	57.520	-12.654	4x4
HW3Y	57.520	-20.654	4x4
R/WN	-8.634	-71.539	4x4
RDN	-24.634	-71.539	4x4
RDP	-32.634	-71.539	4x4
SPC	31.366	-71.539	4x4
SPD	39.366	-71.539	4x4
SPE	23.366	-71.539	4x4
STWN	-72.638	-55.142	4x4
VCC	63.661	-55.539	4x4
VCC	63.661	-46.874	4x4
VCC	63.661	-63.539	4x4
VCC	-56.634	-71.539	4x4

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
VCC	-64.634	-71.539	4x4
VEE	-72.638	-63.142	4x4
VEE	-72.638	-71.539	4x4
WDX	7.366	-71.539	4x4
WDY	-0.634	-71.539	4x4

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VM5435

8-CHANNEL PAD COORDINATES

Specific Characteristics

Die size: **TBD** x **TBD** Mils

Pad Coordinates for the VM5435 (in Mils) are “bump down.”

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN/FAST	47.736	-71.539	4x4
DMY/RSTN	55.736	-71.539	4x4
FLT	15.366	-71.539	4x4
FUSE0	63.831	-71.539	4x4oct
FUSE1	72.638	-71.539	4x4oct
FUSE2	72.638	-60.134	4x4oct
FUSE3	72.638	-51.449	4x4oct
FUSE4	72.638	-42.654	4x4oct
GND	-16.634	-71.539	4x4
GND	-40.634	-71.539	4x4
GND	-48.634	-71.539	4x4
HR0N	-57.520	3.346	4x4
HR0P	-57.520	-4.654	4x4
HR1N	-57.520	11.346	4x4
HR1P	-57.520	19.346	4x4
HR2N	-36.000	57.630	4x4
HR2P	-44.000	57.630	4x4
HR3N	-28.000	57.630	4x4
HR3P	-20.000	57.630	4x4
HR4N	28.000	57.630	4x4
HR4P	20.000	57.630	4x4
HR5N	36.000	57.630	4x4
HR5P	44.000	57.630	4x4
HR6N	57.520	11.346	4x4
HR6P	57.520	19.346	4x4
HR7N	57.520	3.346	4x4
HR7P	57.520	-4.654	4x4
HW0X	-57.520	-12.654	4x4
HW0Y	-57.520	-20.654	4x4
HW1X	-57.520	27.346	4x4
HW1Y	-57.520	35.346	4x4
HW2X	-52.000	57.630	4x4
HW2Y	-60.000	57.630	4x4
HW3X	-12.000	57.630	4x4
HW3Y	-4.000	57.630	4x4
HW4X	12.000	57.630	4x4
HW4Y	4.000	57.630	4x4
HW5X	52.000	57.630	4x4

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
HW5Y	60.000	57.630	4x4
HW6X	57.520	27.346	4x4
HW6Y	57.520	35.346	4x4
HW7X	57.520	-12.654	4x4
HW7Y	57.520	-20.654	4x4
R/WN	-8.634	-71.539	4x4
RDN	-24.634	-71.539	4x4
RDP	-32.634	-71.539	4x4
SPC	31.366	-71.539	4x4
SPD	39.366	-71.539	4x4
SPE	23.366	-71.539	4x4
STWN	-72.638	-55.142	4x4
VCC	63.661	-55.539	4x4
VCC	63.661	-46.874	4x4
VCC	63.661	-63.539	4x4
VCC	-56.634	-71.539	4x4
VCC	-64.634	-71.539	4x4
VEE	-72.638	-63.142	4x4
VEE	-72.638	-71.539	4x4
WDX	7.366	-71.539	4x4
WDY	-0.634	-71.539	4x4

VTC Inc.
Value The Customer™

VM546012

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 500 Mbits/sec
  - Designed for Use With Four-Terminal GMR Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - 12 Channels Available
  - Fault Detect Capability
  - Servo Bank Write Capability
  - Provides for Addressing of Multiple Preamplifiers
- *High Performance Reader*
  - Current or Voltage Bias / Voltage Sense Configuration
  - Reader Bias Current/Voltage 6-bit DAC, 2 -10 mA Range
  - Programmable Read Voltage Gain (100 V/V to 250 V/V Typical)
  - Input Noise Voltage = 0.55 $nV/\sqrt{Hz}$ Typical
  - Input Noise Current = 8 $pA/\sqrt{Hz}$ Typical
  - Input Capacitance = **TBD** pF Typical
  - Programmable Bandwidths to 350 MHz Typical
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 65 mA Range
  - Rise Time 500 pS Typical (10-90%, I_W = 50 mA, L_{total} = 70 nH, R = 10Ω)

DESCRIPTION

The VM546012 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM546012 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

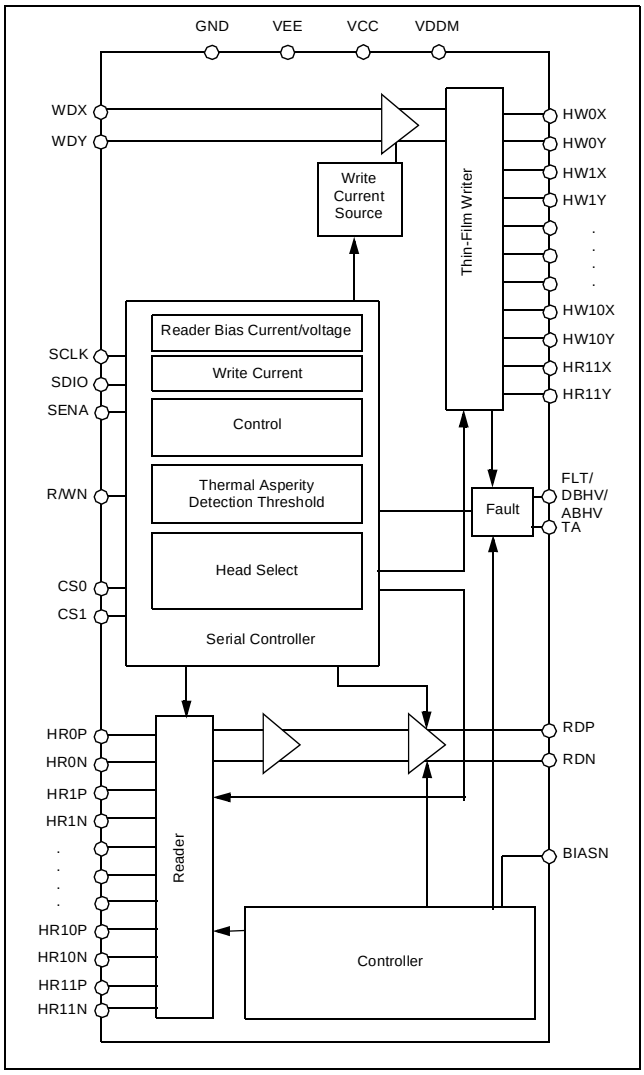
Programmability of the VM546012 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, write current overshoot and undershoot, fault modes, thermal asperity detection and threshold, and dynamic thermal asperity compensation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM546012 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. The device also provides power saving idle and sleep modes.

The VM546012 is available in a die or bump die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR} ..... 18 mA

Write Current, I_W ..... 90 mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -5V ± 10%

Write Current, I_W ..... 15 - 65 mA
Write Head Inductance, L_W ..... 70 nH
Write Head Resistance, R_W ..... 8 - 16 Ω
Read Bias:
- Current, I_{MR} ..... 2 - 10 mA
- Voltage, V_{MR} ..... 100 - 500 mV

Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 30 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM546012 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 181 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

All control lines on the VM546012 may be shared, including the serial lines SCLK, SDIO and SENA. Default settings are listed in Table 80 on page 187.

OPERATING MODES

Pin and register combinations select read/write, servo track write or mode operations as shown in Table 73. The active chip in multiple preamp configurations is selected as shown in Table 74.

Table 73 Mode Select

Pin		Register:Bit				
R/WN pin 5>	BIASN pin 13>	SLEEPN 1:<D2>	IDLEN 1:<D3>	SERV1 3:<D7>	SERV0 10:<D0>	Operational Mode
X	X	0	X	X	X	Sleep
X	X	1	0	X	X	Idle
1	0	1	1	0	0	Read
0	1	1	1	0	0	Write
0	0	1	1	0	0	Write Bias Active
0	1	1	1	0	1	Servo [1]
0	1	1	1	1	0	Servo [1]
0	1	1	1	1	1	Servo [1]
0	0	1	1	1	1	Servo Bias Active

1. SERVO0 and SERVO1 settings must match, or a Servo fault. See Table 75.

Table 74 Multiple Preamplifier Addressing

Pin/Address Values		
CS1/A2	CS0/A1	Chip Status
0	0	Preamp 0
1	0	Preamp 1
0	1	Preamp 2
1	1	Undefined

Note: Address bits A1 and A2 must match the value of CS0 and CS1 to correctly address the preamplifier. See Table 77 for Preamplifier Addressing.
VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.

Sleep Mode

In the sleep mode power consumption is minimized. All outputs are disabled (except in test mode). The writer current source and the reader bias current/voltage source are deactivated while the RDN/RDP outputs and the WDX/WDY inputs switch to a high impedance state. Faults are not detected in Sleep Mode.

Sleep mode is selected by setting 4:<D2> = 0, see Tables 73, 78 and 79.

Note: Always transition from Sleep to Idle mode 10 µs before entering an active mode.

Idle Mode

The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN/RDP outputs and the WDX/WDY inputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. Faults are not detected in Idle Mode.

Idle mode is triggered by setting 4:<D3> = 0, see Tables 73, 78 and 79.

Dummy Mode

Setting DUMMY (1:<D5>) high directs the MR bias current/voltage to an internal dummy head. This maintains the reader bias at operational levels for quick read recovery.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature or buffered head voltage.

Read Head Resistance

The resistance of the MR head can be measured in three ways: an automatic digital conversion, an iterative method using DBHV and threshold settings to trigger or not trigger a fault, or by monitoring the ABHV output.

Digital Conversion

To perform digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 73).
2) Set the RMR/TEMP bit (8:<D7>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (9:<D1>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)

4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 9:<D7-D1> = 0010000 the MR head resistance is 16 ohms. (The measurement range for MR resistance is 0 - 127 Ω.)

Note: MR bias current is always enabled in this mode.

Iterative Resistance Reading

To perform the iterative resistance reading:

1) Place device in Read Mode (see Table 73).
2) Set the DBHV bit (1:<D4>) high to enter the MR resistance measurement mode.
3) Monitor the FLT/ABHV/DBHV pin to determine the voltage across the MR element:
   - A high indicates the voltage is within the window (150mv to 320mv).
   - A low indicates the voltage is outside the window.
4) Vary the MR bias current (2:<D2-D7>) to determine where the defined thresholds are crossed. The FLT line is not valid until the I_{MR} change settles; values for this are listed in "READ CHARACTERISTICS" on page 193.
5) Resistance can be inferred from the threshold settings.

Buffered Head Voltage

To output the MR head voltage on the FLT/ABHV/DBHV pin:

1) Place device in Read Mode (see Table 73).
2) Set ABHV bit (1:<D7>) high to output the MR head voltage as scaled by a gain of 5.

Note: If ABHV and DBHV are both high, ABHV takes precedence. See the truth table in PIN FUNCTION LIST AND DESCRIPTION on page 189.

Die Temperature Monitoring

The die temperature range is 0^oC to 150^oC. To measure the die temperature:

1) Set RMR/TEMP (8:<D7>) high to enable the die temperature.
2) Set DIGON bit (9:<D0>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 9:<D7-D1> = 0100000 the die temperature is 38^oC (32^oC x 1.18).

$$T = 1.18k \qquad \textit{(eq. 35)}$$

where k = 0 - 127 and T is degrees Centigrade

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting the R/WN pin high. In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM546012 uses the voltage-sensing reader architecture with biasing programmable as current or voltage. The magnitude of the reader bias current/voltage is set to the value programmed in 2:<D2-D7>. The equations below govern the read bias current/voltage magnitude:

Current Mode

$$I_{MR} = 2 + [k_{IMR} \cdot 0.127]mA \qquad \textit{(eq. 36)}$$

Voltage Mode

$$V_{MR} = 100 + [k_{IMR} \cdot 6.35]mV \qquad \textit{(eq. 37)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes:

- Current bias mode is selected by setting 1:<D6> = 0, and
- Voltage bias mode is selected by setting 1:<D6> = 1.

Note: Any transition between current and voltage bias modes must occur in the Sleep mode.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element. The applied value is programmed in 2:<D2-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

The reader enters a fast recovery mode during modal transitions, serial register operations, and when the reader is biased during a write mode. The fast recovery mode minimizes signal anomalies on the reader outputs.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT/ABHV/DBHV or the TA pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 81.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 7:<D6-D0> as shown in Table 82. The default setting (0000) is to enable all faults.

Fault codes may be cleared by setting the Clear Fault bit, 7:<D7> = 1. The following are valid read fault conditions:

- MR Bias Not Enabled
- MR Overcurrent
- Thermal Asperity Detected [1]
- Read Head Open
- Read Head Shorted
- Low V_{CC} , V_{DDM} or V_{EE}
- Overtemperature

1. Thermal asperity is flagged on TA pin, all other flagged on FLT/ABHV/DBHV pin.

Read Gain

The default gain is 100 V/V with a head resistance of 55Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in 3:<D2-D3>. The formula that describes the actual gain is shown below:

$$GAIN = \frac{515}{460 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 38)}$$

k_{GAIN} = 0-3

Fast Mode

Setting the FAST bit (1:<D1>) high in read mode, raises the low corner frequency to 5MHz. If the FAST bit is low, the low corner frequency is set to the value programmed in LFP (3:<D0-D1>).

Thermal Asperity Detection and Recovery

Detection

Setting the TAD bit high (5:<D6>) enables positive or negative thermal asperity detection.

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the voltage threshold is governed by the following equation and is set in 5:<D0-D4>:

$$V_{TAT} = 50 + \left[900 \times \left(\frac{k_{TAT}}{31}\right)\right] \quad \textit{(eq. 39)}$$

V_{TAT} represents the TA threshold (output-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

A TA fault is reported on the TA pin, not the FLT pin. The TA and FLT pins may be externally connected to a common point as shown in the TYPICAL CONNECTION DIAGRAM on page 190.

Fast Recovery

Setting the TA Compensation (TAC) bit high (5:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised to 5MHz from the nominal value programmed in 3:<D0-D1>. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 5:<D6>, and TA pin is inactive when preamp is in write mode.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting the R/WN pin low.

The magnitude of the write current is determined by the write current registers (4:<D3-D7>). The following equation governs the write current magnitude:

$$I_W = 15 + (k_{IW} \cdot 1.61)\,mA \quad \textit{(eq. 40)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data signals on the WDX and WDY lines drive the current switch of the selected head.

See Figure 60 for the timing diagram on page 196.

Write Current DAC

Register 4:<D3-D7> represent the binary equivalent of the DAC setting (0-31).

Read Bias Enabled in Write Mode

Taking the BIASN pin low (at least 5µs before the R/WN pin is set high) enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (1:<D1>) initiates Write Data Inputs in Voltage Mode. Setting the WVORI bit high initiates the Write Data Inputs in Current Mode.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 81.

Specific fault conditions may be disabled by setting the Fault Reporting Mask, 7:<D0-D6> as shown in Table 82. The default setting (000000) is to enable all faults.

Fault codes may be cleared setting the CLRFC, 7:<D7>, high.

The following are valid write fault conditions:

- Write Data Frequency Low
- Open or Shorted Write Head
- Servo Fault
- Low V_{CC} , V_{DDM} [1] or V_{EE} [2]
- Overtemperature
- Invalid Head Selected

1. If V_{DDM} is not supplied, the fault is disabled.
1. Low V fault disables write current until proper level is restored.

Servo Write Mode

In the servo write mode, up to eight channels may be written simultaneously.

Table 79 indicates how heads can be selected for individual or simultaneous writing.

Note: VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.

Setting both the SERVO0 and SERVO1 bits (10:<D0> and 3:<D7>) to ‘1’ and holding the R/WN pin low places the preamp in servo write mode (see Table 73).

The BANK bit (10:<D7>) permits writing to even or odd head combinations: high writes to even and low writes to odd heads. A high in SHDn (10:<D1-D6> selects the specific head on which to perform the servo write. The default setting is to select no heads (10:<D7> = 0 and 10:<D1-D6> = 000000).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

A servo fault is generated if the SERVO0 and SERVO1 (10:<D0>, 3:<D7>) settings do not match as shown in Table 75.

Table 75 Servo Faults

SERVO1 3:<D7>	*SERVO0 10:<D0>*	*Mode*	*Fault*
0	0	Active [1]	No
1	0	Active [1]	Yes
0	1	Active [1]	Yes
1	1	Servo	No

1. Active includes all modes (read, write, idle, sleep or test), except servo.

SERIAL PORT

Serial Interface

The VM546012 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 77 and 78 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 57.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one read/write command bit <A0> (high for read, low for write),
  - two preamp address bits <A2-A1>,
  - four register address bits <A6-A3>, and
  - one unused bits <A7>.
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 8th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and the data will be clocked from the SDIO line on subsequent rising edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode. The reader invokes a *fast* mode while a serial interface operation occurs.

See Tables 77 and 78 for a bit description. See Table 76, and Figures 58 and 59 for serial interface timing information.

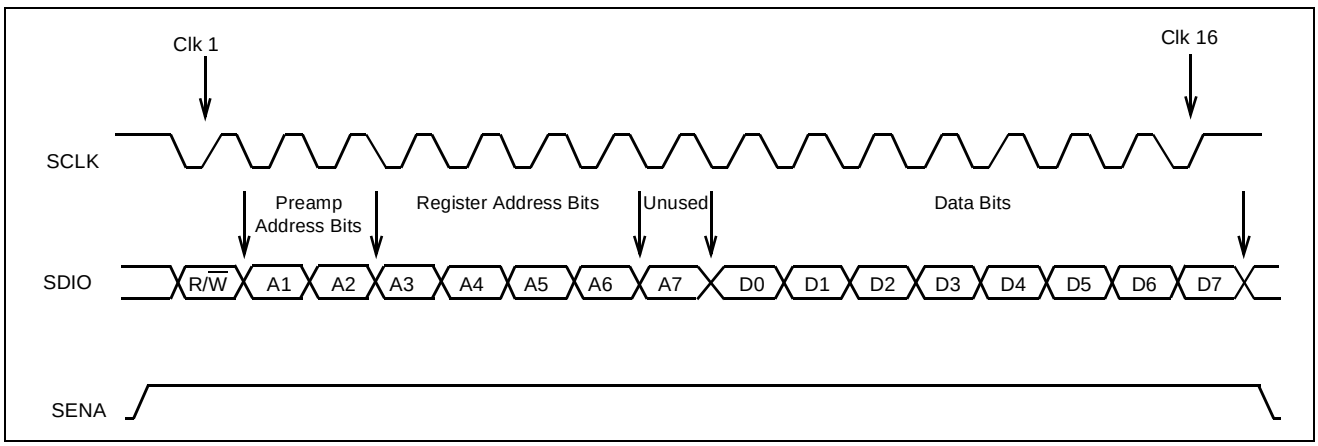


Figure 57 Serial Port Protocol

Table 76 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) rate, write				40	MHz
SENA to SCLK delay	T_{sens}	**TBD**			nS
SDIO setup time, write	T_{wds}	**TBD**			nS
SDIO delay time, read	T_{rds}	**TBD**		**TBD**	nS
SDIO hold time	T_{dh}	**TBD**			nS
SCLK cycle time	T_{c}	**TBD**			nS
SCLK high time	T_{ckh}	**TBD**			nS
SCLK low time	T_{ckl}	**TBD**			nS
SENA hold time	T_{shld}	**TBD**			nS
Time between I/O operations	T_{sl}	**TBD**			nS
Time to activate SDIO	T_{act}	**TBD**		**TBD**	nS
Duration of SerEna (read)	T_{rd}	**TBD**			nS
Duration of SerEna (write)	T_{wt}	**TBD**			nS

Note: SENA assertion level is high.

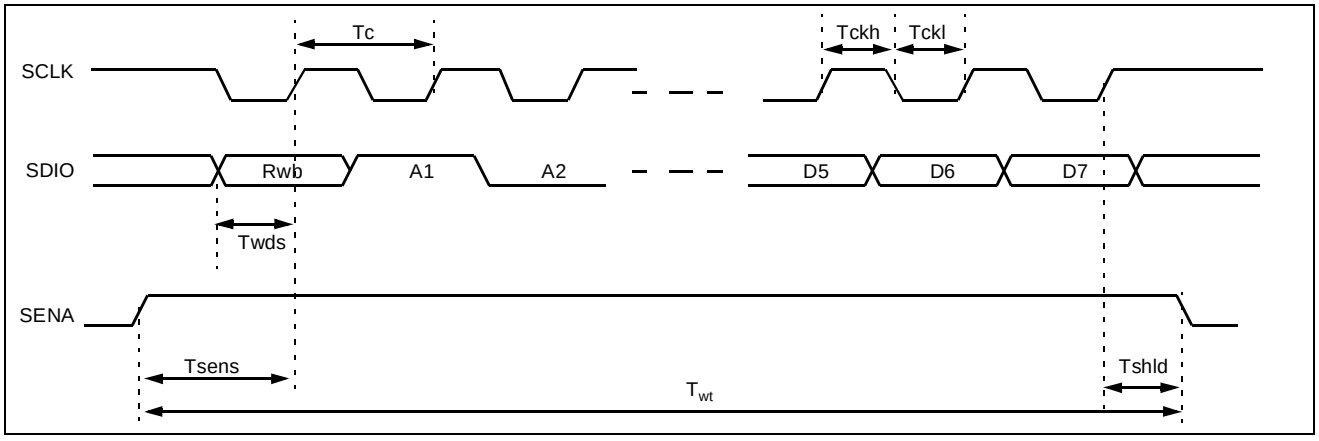


Figure 58 Serial Port Timing - Write Operation

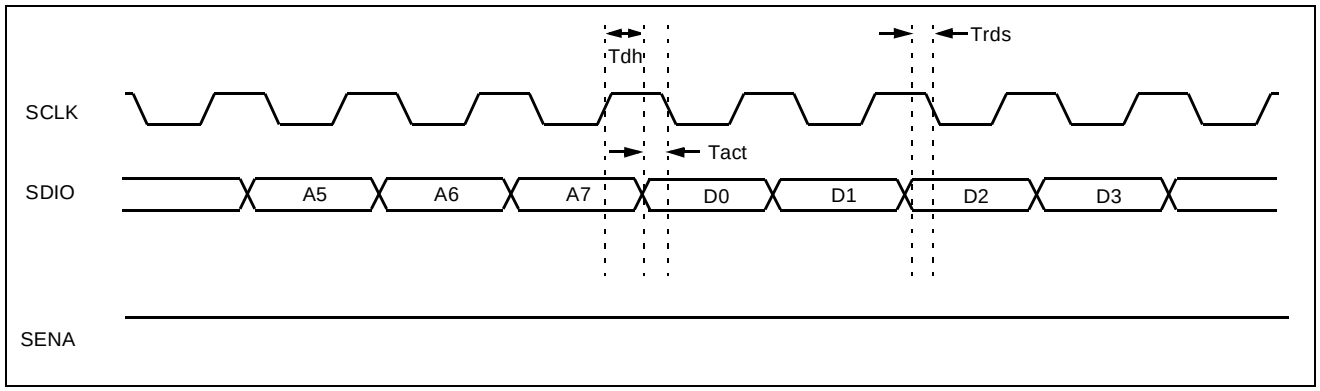


Figure 59 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 77 lists the serial address for each register. Table 78 lists the data contents of the register set. A description of the individual bits is provided in Table 79.

Table 77 Serial Interface Addressing

Register #	Register Address Bits				Preamp Address Bits			R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	X	0	0	0	0	Preamplifier Select Bits See Table 74 for valid chip addressing values.		0 = write 1 = read
1	X	0	0	0	1			
2	X	0	0	1	0			
3	X	0	0	1	1			
4	X	0	1	0	0			
5	X	0	1	0	1			
6	X	0	1	1	0			
7	X	0	1	1	1			
8	X	1	0	0	0			
9	X	1	0	0	1			
10	X	1	0	1	0			

Table 78 Serial Interface Bit Map - Base Registers

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Head Select	0	HS3	HS2	HS1	HS0	[1]	[1]	[1]	[1]
Control	1	ABHV	I/V	DUMMY	DBHV	IDLEN	SLEEPN	WVORI	FAST
IMR	2	IMR5	IMR4	IMR3	IMR2	IMR1	IMR0	GAIN1	GAIN0
Poles	3	SERVO1	USC2	USC1	USC0	BW1	BW0	LFP1	LFP0
Write Current/	4	IW4	IW3	IW2	IW1	IW0	OSC2	OSC1	OSC0
Thermal Asperity	5	[1]	TAD	TAC	TAD4	TAD3	TAD2	TAD1	TAD0
Vendor ID	6 [2]	REV2	REV1	REV0	VEND4	VEND3	VEND2	VEND1	VEND0
Fault Mask/Clear	7	CLRFC	FLT6	FLT5	FLT4	FLT3	FLT2	FLT1	FLT0
Fault Code	8	RMR/ TEMP	TTOSC	[1]	[1]	FCOD3	FCOD2	FCOD1	FCOD0
Data Storage/Digital	9	DSTR6	DSTR5	DSTR4	DSTR3	DSTR2	DSTR1	DSTR0	DIGON
Servo	10	BANK	SHD10/11	SHD8/9	SHD6/7	SHD4/5	SHD2/3	SHD0/1	SERVO0

1. Reserved.
2. Read Only Register/Bits:
   Register 6:<D0-D4> is the Vendor ID code (VTC=**TBD**),
   Register 6:<D5-D7> is the Vendor revision code. Initial revision shall be (REV0 = 0, REV1 = 0, REV2 = 0),

Table 79 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description				
0	D0-D3	Reserved						
	D4-D7	Head Select	HSn	Binary selection of head	HS3	HS2	HS1	HS0
				Head Select	0:<D7>	0:<D6>	0:<D5>	0:<D4>
				0	0	0	0	0
				1	0	0	0	1
				2	0	0	1	0
				3	0	0	1	1
				4	0	1	0	0
				5	0	1	0	1
				6	0	1	1	0
				7	0	1	1	1
				8	1	0	0	0
				9	1	0	0	1
				10	1	0	1	0
				11	1	0	1	1
1	D0	Fast Mode	FAST	Raises low corner frequency 5 MHz 0 = Disable 1 = Enable				
	D1	Write Voltage or Current	WVORI	0 = Voltage mode write data inputs. 1 = Current mode write data inputs. Note: VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.				
	D2	Sleep	SLEEPN	0/1 = See Table 73, “Mode Select,” on page 178 Note: This bit has precedence over the IDLEN bit (1:<D3>).				
	D3	Idle Mode	IDLEN	0/1 = See Table 73, “Mode Select,” on page 178 Note: The SLEEPN bit (1:<D2>) has precedence over this bit.				
	D4	Digital Buffered Head Voltage Output	DBHV	0 = Disable 1 = Enable Note: DBHV is overridden when ABHV (1:<D7>) is enabled.				
	D5	Dummy MR Head Load	DUMMY	0 = MR Head selected using HSn register (0:<D4-D7>) setting. 1 = Dummy head resistive load selected.				
	D6	Current or Voltage Bias	I/V	0 = Current bias mode. 1 = Voltage bias mode. Note: Bias level is set in registers 2:<D2-D7> Note: Any transition between current and voltage bias modes must occur in the Sleep mode.				
	D7	Analog Buffered Head Voltage Output	ABHV	0 = Disable 1 = Enable Note: ABHV overrides DBHV (1:<D4>).				

Table 79 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
2	D0-1	Gain	GAINn	Binary selection of MR Reader Gain least significant bit:	GAIN1	GAIN0
				Gain	2:<D1>	1:<D0>
				100 V/V	0	0
				150 V/V	0	1
				200 V/V	1	0
				250 V/V	1	1
	D2-D7	Bias Level	IMRn	Binary selection of MR Head Current Bias least significant bit Current Bias = 2mA (000000) to 10mA (111111) in 0.127mA increments. Voltage Bias = 100mV (000000) to 500mV (111111) in 6.35mV increments. Note: Current or Voltage Bias selected in 1:<D6>.		
3	D0-D1	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth:	LFP1	LFP0
				Low Frequency Bandwidth	3:<D1>	3:<D0>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				5 MHz	1	1
	D2-D3	Bandwidth	BWn	Binary selection of Bandwidth:	BW1	BW0
				Bandwidth	3:<D3>	3:<D2>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
	D4-D6	Undershoot Control	USCn	Undershoot Control **TBD** % (000) to **TBD** % (111) in **TBD** % increments.		
	D7	Servo Bank 1	SERVO1	0/1 = See Table 75, “Servo Faults,” on page 180 Note: SERVO0 (10:<D0>) must also be selected for a valid servo write. Note: Register 10:<D1-D6> defines which heads to servo write.		
4	D0-D2	Overshoot Control	OSCn	Overshoot Control **TBD** % 000) to **TBD** % (111) in **TBD** % increments.		
	D3-D7	Write Current	IWn	Binary selection of Write Current 15 mA (00000) to 65 mA (11111) in 1.6 mA increments.		
5	D0-D4	Thermal Asperity Threshold - MSB	TAn	Binary selection of Thermal Asperity Threshold TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV.		
	D5	Thermal Asperity Compensation	TAC	0 = No TA Compensation. 1 = TA Compensation selected. Note: TA Detection must be enabled in 5:<D6> for TAC to function.		
	D6	Thermal Asperity Detection	TAD	0 = TA Detection disabled. 1 = TA Detection enabled.		
	D7	Reserved				
6	D0-D4	Vendor Code	VENDn	Binary Vendor Code (10000 = VTC)		
	D5-D7	Revision of Part	REVn	Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1after exceeding 8.		
7	D0-D6	Fault Mask	FLTn	Fault Reporting Mask See Table 82.		
	D7	Clear Fault Codes	CLRFC	0 = Retain faults 1 = Clear faults Note: CLRFC resets to 0 after fault codes clear.		

Table 79 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
8	D0-D3	Fault Condition	FCODEn	Binary code of Fault(s) See Table 81.
	D4-D5	Reserved		
	D6	Test Bit	TTOSC	Manufacturer's test bit - Reserved
	D7	MR Head Resistance or Die Temperature	RMR/ TEMP	0 = MR Head Resistance stored in DSTRn register (9:<D1-D7>). 1 = Die Temperature stored in DSTRn register (9:<D1-D7>).
9	D0	Internal Digital Conversion	DIGON	0 = Analog-to-digital conversion off 1 = Start analog-to-digital conversion Note: DIGON resets to 0 when analog-to-digital conversion completes. Note: Reader Resistance or Die Temperature output is selected in TBD and the measurement is stored in 9:<D1-D7>.
	D1-D7	Data Storage	DSTRn	Data storage of binary output from MR Head Resistance or Die Temperature: Resistance range is 0 to 127 Ohms. Temperature range is 0 to 150^{0}C. Note: 9:<D0> selects analog or digital output.
10	D0	Servo Bank 0	SERVO0	0/1 = See Table 75, "Servo Faults," on page 180 Note: SERVO1 (3:<D7>) must also be selected for a valid servo write. Note: Register 10:<D1-D6> defines which heads to servo write. Default is to servo write all heads (see Table 80).
	D1-D6	Servo Head Select	SHDn	Binary selection of the head pairs to be servo track written. - Bit 1 = 1 *selects* HD0 or HD1. - Bit 2 = 1 *selects* HD2 or HD3. - Bit 3 = 0 *deselects* HD4 or HD5. - Bit 4 = 0 *deselects* HD6 or HD7. - Bit 5 = 0 *deselects* HD8 or HD9. - Bit 6 = 0 *deselects* HD10 or HD11. Register 10:<D7> defines whether even or odd numbered heads are selected from the active pairs. Default is no head selected (see Table 80). Examples when the default (odd) head bank is selected (10:<D7> = 0): 1. 001000 = Servo Write Head 7. 2. 000011 = Servo Write Heads 1 and 3. Note: SERVO0 and SERVO1 (10:<D0> and 3:<D7>) must be selected to servo write.
	D7	Servo Bank Select	BANK	0 = Odd head bank selected 1 = Even head bank selected Note: Register 10:<D1-D6> defines the head combinations to servo write. Default is to servo write the odd head bank (see Table 80). Note: SERVO0 and SERVO1 (10:<D0> and 3:<D7>) must be selected to servo write.

Table 80 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Head Select	0	<0000 XXXX>
Control	1	<0000 0000>
Bias/Gain	2	<0000 0000>
Poles	3	<0100 1100>
Write Current/Overshoot	4	<0000 0100>
Thermal Asperity	5	<0000 0000>
Vendor ID	6	<XXXX XXXX>
Fault Mask/Clear	7	<0000 0000>
Fault Code	8	<XXXX 0000>
Data Storage/Digitization	9	<0000 0000>
Servo	10	<0000 0000>

Fault Reporting and Masking

Table 81 Fault Conditions and Codes

Fault Code 8:<D3-D0>	Fault	Priority [1]	Valid Mode(s)	Mask [2]	Conditions
0000	No Fault	–	Read or Write	–	
0001	Reserved	–	–	–	
0010	MR Overcurrent	2	Read	M	
0011	Thermal Asperity Detected	6	Read	M	
0100	Read Head Open	7	Read	M [3]	
0101	Read Head Shorted	8	Read	M [3]	
0110	Write Data Frequency Low	5	Write	M	
0111	Write Head Open/Shorted	3	Write	M	
1000	Servo Fault	9	Write		Unmatched servo bank bits
1001	Low V_{CC}, V_{DDM} or V_{EE}	1	Read or Write	M	Disables write current until proper voltage level is restored
1010	Reserved	–	–	–	
1011	Overtemperature	10	Read or Write	M	Temp > 140^{o}C
1100	Reserved	–	–	–	
1101	Reserved	–	–	–	
1110	Reserved	–	–	–	
1111	Reserved	–	–	–	

1. First fault reported is latched until a higher priority fault is reported or the code is cleared.
2. See Table 82 for an explanation of fault masking.
3. Single bit masks both faults.

Setting the appropriate bit(s) listed in Table 82 masks the fault(s) at both the fault register and the FLT pin. If 7:<D7-D0> = 0000 0101, an MR Overcurrent fault is masked with the 7:<D0> bit and Read Head Open and Read Head Shorted faults are masked with the 7:<D2> bit.

Table 82 Fault Masking

Mask Bit Register 7	Fault(s) Masked [1]	Mask Bit Register 7	Masked Fault
<D0>	MR Overcurrent	<D4>	Write Head Open/Shorted
<D1>	Thermal Asperity Detected	<D5>	Low V_{CC}, V_{DDM} or V_{EE}
<D2>	Read Head Open/Shorted	<D6>	Overtemperature
<D3>	Write Data Frequency Low	Note: Setting <D7> = 1 clears all fault codes in 8:<D0-D3>.	

1. Single bit masks both Read Head Open and Read Head Shorted faults.

PIN FUNCTION LIST AND DESCRIPTION

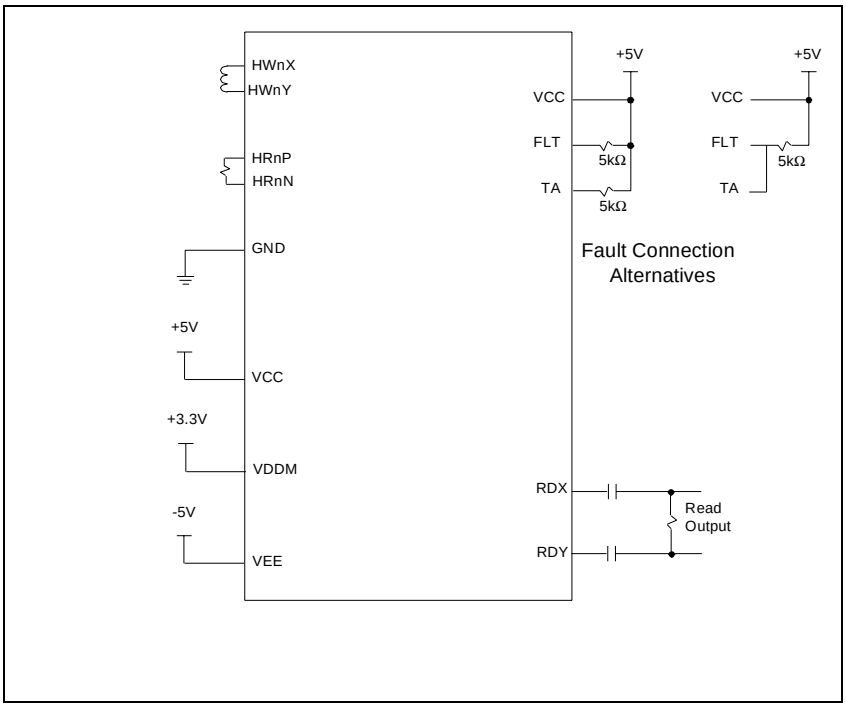
Signal	*Input/Output*	*Logic Level Default* [1]	*Description*
FLT/ABHV/DBHV	O [2]	–	Write/Read Fault and Buffered Head Voltage (Analog or Digital) as shown in truth table: • Fault (FLT) output: - A TTL high level indicates a fault in write mode. - A TTL low level indicates a fault in read mode. • Analog or Digital Buffered Head Voltage output when ABHV and/or DBHV is enabled.
GND	[2]	–	Ground
HR0N-HR11N	I	–	Read head connections, negative end.
HR0P-HR11P	I	–	Read head connections, positive end.
HW0X-HW11X	O	–	Thin-Film write head connections, positive end.
HW0Y-HW11Y	O	–	Thin-Film write head connections, negative end
R/WN	I [2]	high	Read/Write: A TTL low level enables write mode.
BIASN		high	MR Bias: • A TTL low level enables bias current through the active head.
RDP, RDN	O [2]	–	Read Data: Differential read signal outputs.
SCLK	I [2]	low	Serial Clock: Serial port clock; see Figure 57.
SDIO	I/O [2]	low	Serial Data: Serial port data; see Figure 57.
SENA	I [2]	low	Serial Enable: Serial port enable; see Figure 57.
TA	O [2]	high	Thermal Asperity: • When 5:<D6> = 1 (TA Detection enabled): - A TTL high level indicates no TA. - A TTL low level indicates a TA exceeded the threshold programmed in 5:<D0-D4>. **Note:** TA pin is inactive when preamp is in write mode.
VCC	[2]	–	+5.0V supply
VDDM	I [2]	–	+3.3V supply, monitor pin only
VEE	[2]	–	-5.0V supply
WDX, WDY	I [2]	high	Differential Pseudo-ECL write data inputs

Output	*ABHV 1:<D7>*	*DBHV 1:<D4>*
FLT	0	0
DBHV	0	1
ABHV	1	0
ABHV [1]	1	1

1. ABHV overrides DBHV setting. Output is Analog Buffered Head Voltage (ABHV).

1. 40kΩ pullup/pulldown resistors are used to default pins to specified high or low levels.
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- Minimum FLT pullup resistance is 5 kΩ.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Idle Mode		15	**TBD**	
		Sleep Mode		500	**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Idle Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Idle Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	mA
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{CTH}		3.75	4.0	4.25	V
V_{DDM} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%, Fault not detected below 1 VDC.	2.0	2.25	2.5	V
V_{EE} Fault Threshold	V_{ETH}		-4.25	-4.0	-3.75	V
High Level WDATA		PECL	1.9		V_{CC}	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	0.8	2.0	4.0	mA
WDATA PECL swing		Voltage mode differential	0.4		1.5	V_{pp}

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage compliance for WDATA		CMM of inputs when in current mode			V_{CC} -1.0	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		100		V/V
		Gain Bits = 11		250		V/V
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB		350		
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00		1		MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		nV/√Hz
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		pA/√Hz
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}			2	4	pF
Differential Input Resistance	R_{IN}			400		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	20			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			
Power Supply Rejection	PSRR	100mV_{pp} on V_{CC} or V_{EE}, 10 MHz < f < 200 MHz	20			dB
		100mV_{pp} on V_{CC} or V_{EE}, 1 MHz < f < 10 MHz	40			
		100mV_{pp} on V_{CC} or V_{EE}, f < 100 kHz	60			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV_{pp}, 1 MHz < f < 200 MHz	50			dB
Rejection of SCLK and SDIO		100 mV_{pp} on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2.0		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)		50		mV
Reader Head Resistance	R_{MR}		30	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA, R_{MR}=100Ω.		**TBD**		nS
Reader Bias Current Overshoot					2.5	%
Reader Bias Current Overshoot Time Duration					**TBD**	
TA Detection Response Time		TA occurred to FLT active			40	nS
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		nS
MR Measurement Accuracy				4		%
Temperature Measurement Accuracy				2		^{o}C
BHV Accuracy				5		%

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		15		65	mA
Write Current Tolerance	ΔI_W	15 < I_W < 65 mA	-8		8	%
Write Servo Current Tolerance			-10		10	%
Differential Head Voltage Swing	V_{DH}	Open Head	8			V_{PP}
Unselected Head Transition Current	I_{UH}				1	mA_{pk}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Time for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			nS
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	nS
Write Data Input Terminal Resistor	w_{RIH}			150		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

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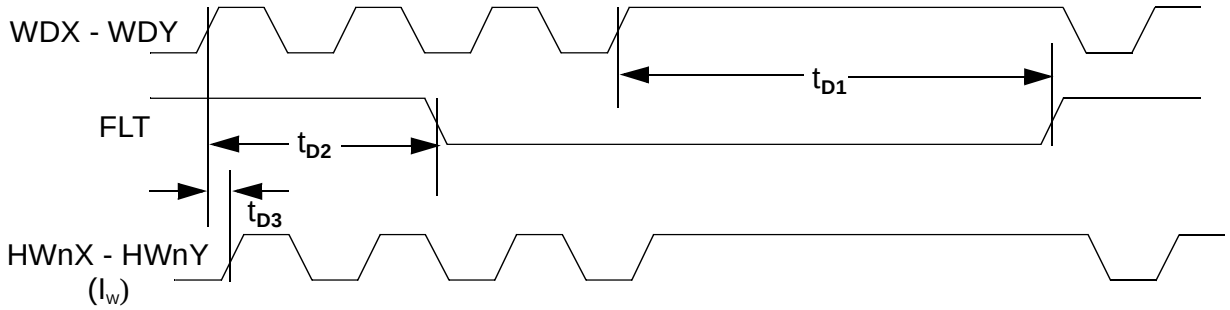
SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	nS
R/WN to Read Mode	t_{WR}	To 90% of data envelope or 20 mV DC			300	nS
		To 10% of I_W envelope			50	nS
Idle to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 20 mV			5	µS
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 20 mV, **TBD** - Fixed I_{MR}.			1	µS
		To 90% of envelope, DC Offset Level within 20 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			3	µS
Active (16th rising edge) to Idle	t_{RI}	To 10% of read envelope or write current			50	nS
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µS
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		nS
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		nS
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5nS rise/fall time, L_H=0, R_H=**TBD**			100	pS
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=70nH, R_H=10Ω.		500		pS
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.				nS
Read to Servo Write		From 50%R/WN to 90% I_W			50	nS
Read to Servo Write Head Turn-on Variation					**TBD**	nS
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µS
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	nS

1. See Figure 60 for the write mode timing diagram.



In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 60 Write Mode Timing Diagram *

PACKAGING

12-Channel Die

Specific Characteristics

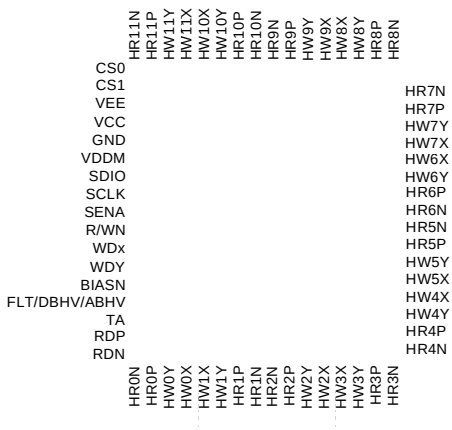
Die size: **TBD** x **TBD** Mils

Wire Bond Coordinates for the VM546012 (in Mils)

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN	**TBD**	**TBD**	**TBD**
CS0	**TBD**	**TBD**	**TBD**
CS1	**TBD**	**TBD**	**TBD**
FLT/ DBHV/ABHV	**TBD**	**TBD**	**TBD**
GND	**TBD**	**TBD**	**TBD**
GND	**TBD**	**TBD**	**TBD**
HR0N	**TBD**	**TBD**	**TBD**
HR0P	**TBD**	**TBD**	**TBD**
HR1N	**TBD**	**TBD**	**TBD**
HR1P	**TBD**	**TBD**	**TBD**
HR2N	**TBD**	**TBD**	**TBD**
HR2P	**TBD**	**TBD**	**TBD**
HR3N	**TBD**	**TBD**	**TBD**
HR3P	**TBD**	**TBD**	**TBD**
HR4N	**TBD**	**TBD**	**TBD**
HR4P	**TBD**	**TBD**	**TBD**
HR5N	**TBD**	**TBD**	**TBD**
HR5P	**TBD**	**TBD**	**TBD**
HR6N	**TBD**	**TBD**	**TBD**
HR6P	**TBD**	**TBD**	**TBD**
HR7N	**TBD**	**TBD**	**TBD**
HR7P	**TBD**	**TBD**	**TBD**
HR8N	**TBD**	**TBD**	**TBD**
HR8P	**TBD**	**TBD**	**TBD**
HR9N	**TBD**	**TBD**	**TBD**
HR9P	**TBD**	**TBD**	**TBD**
HR10N	**TBD**	**TBD**	**TBD**
HR10P	**TBD**	**TBD**	**TBD**
HR11N	**TBD**	**TBD**	**TBD**
HR11P	**TBD**	**TBD**	**TBD**
HW0X	**TBD**	**TBD**	**TBD**
HW0Y	**TBD**	**TBD**	**TBD**
HW1X	**TBD**	**TBD**	**TBD**
HW1Y	**TBD**	**TBD**	**TBD**
HW2X	**TBD**	**TBD**	**TBD**
HW2Y	**TBD**	**TBD**	**TBD**
HW3X	**TBD**	**TBD**	**TBD**

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
HW3Y	**TBD**	**TBD**	**TBD**
HW4X	**TBD**	**TBD**	**TBD**
HW4Y	**TBD**	**TBD**	**TBD**
HW5X	**TBD**	**TBD**	**TBD**
HW5Y	**TBD**	**TBD**	**TBD**
HW6X	**TBD**	**TBD**	**TBD**
HW6Y	**TBD**	**TBD**	**TBD**
HW7X	**TBD**	**TBD**	**TBD**
HW7Y	**TBD**	**TBD**	**TBD**
HW8X	**TBD**	**TBD**	**TBD**
HW8Y	**TBD**	**TBD**	**TBD**
HW9X	**TBD**	**TBD**	**TBD**
HW9Y	**TBD**	**TBD**	**TBD**
HW10X	**TBD**	**TBD**	**TBD**
HW10Y	**TBD**	**TBD**	**TBD**
HW11X	**TBD**	**TBD**	**TBD**
HW11Y	**TBD**	**TBD**	**TBD**
R/WN	**TBD**	**TBD**	**TBD**
RDN	**TBD**	**TBD**	**TBD**
RDP	**TBD**	**TBD**	**TBD**
SCLK	**TBD**	**TBD**	**TBD**
SDIO	**TBD**	**TBD**	**TBD**
SENA	**TBD**	**TBD**	**TBD**
TA	**TBD**	**TBD**	**TBD**
VCC	**TBD**	**TBD**	**TBD**
VDDM	**TBD**	**TBD**	**TBD**
VEE	**TBD**	**TBD**	**TBD**
WDX	**TBD**	**TBD**	**TBD**
WDY	**TBD**	**TBD**	**TBD**

12-CHANNEL CONNECTION DIAGRAM



12-Channel Die

VTC Inc.
Value The Customer™

VM546112

PROGRAMMABLE, DUAL SUPPLY, GIANT MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 500 Mbits/sec
  - Designed for Use With Four-Terminal GMR Heads
  - 3-Line Serial Interface
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - 12 Channels Available
  - Fault Detect Capability
  - Servo Bank Write Capability
  - Provides for Addressing of Multiple Preamplifiers
- *High Performance Reader*
  - Current or Voltage Bias / Voltage Sense Configuration
  - Reader Bias Current/Voltage 6-bit DAC, 2 -10 mA Range
  - Programmable Read Voltage Gain (100 V/V to 250 V/V Typical)
  - Input Noise Voltage = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Noise Current = 8 pA/$\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Programmable Bandwidths to 350 MHz Typical
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 65 mA Range
  - Rise Time 500 pS Typical (10-90%, I_W = 50 mA, L_{total} = 70 nH, R = 10Ω)

DESCRIPTION

The VM546112 is an integrated BiCMOS programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal recording heads. The VM546112 contains a thin-film head writer, a giant magneto-resistive (GMR) reader, and associated control and fault circuitry.

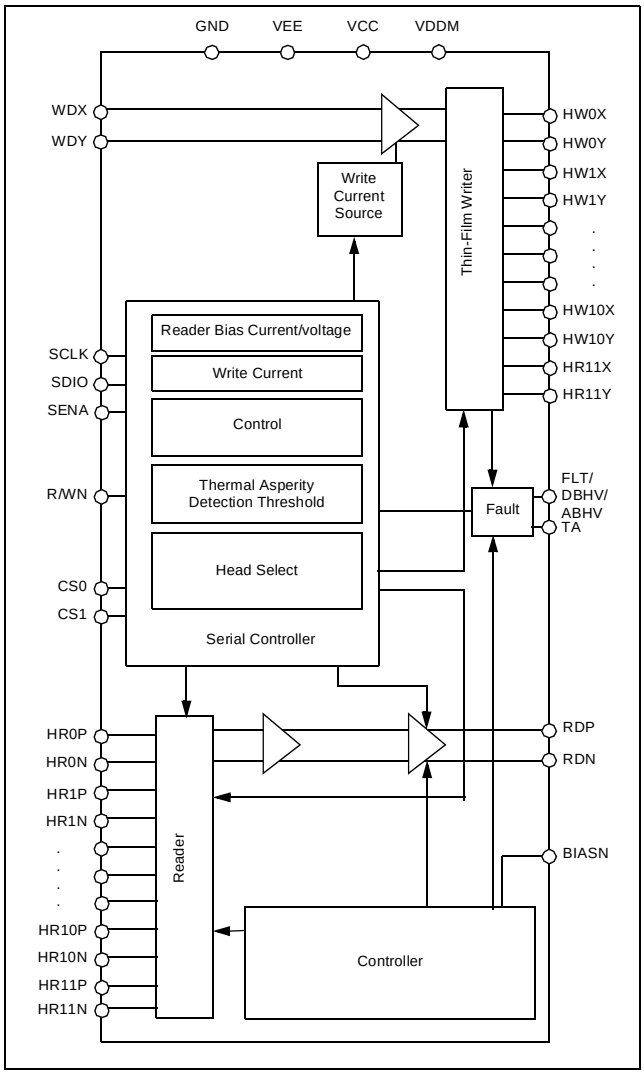
Programmability of the VM546112 is achieved through a 3-line serial interface that is 3.3V TTL/CMOS compatible. Programmable parameters include reader bias current/voltage, write current, gain, head selection and response, write current overshoot and undershoot, fault modes, thermal asperity detection and threshold, and dynamic thermal asperity compensation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to I/O lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM546112 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed BiCMOS processing and innovative circuit design techniques. The device also provides power saving idle and sleep modes.

The VM546112 is available in a die or bump die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -6V

Read Bias:
- Current, I_{MR} ..... 18 mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -5V ± 10%

Write Current, I_W ..... 15 - 65 mA
Write Head Inductance, L_W ..... 70 nH
Write Head Resistance, R_W ..... 8 - 16 Ω
Read Bias:
- Current, I_{MR} ..... 2 - 10 mA
- Voltage, V_{MR} ..... 100 - 500 mV

Read Head Inductance, L_{MR} ..... 10 nH
Read Head Resistance, R_{MR} ..... 30 - 80 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM546112 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude.

See SERIAL PORT on page 203 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

All control lines on the VM546112 may be shared, including the serial lines SCLK, SDIO and SENA. Default settings are listed in Table 90 on page 209.

OPERATING MODES

Pin and register combinations select read/write, servo track write or mode operations as shown in Table 83. The active chip in multiple preamp configurations is selected as shown in Table 84.

Note: VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.

Table 83 Mode Select

Pin		*Register:Bit*				
R/WN pin 5>	*BIASN pin 13>*	*SLEEPN 1:<D2>*	*IDLEN 1:<D3>*	*SERV1 3:<D7>*	*SERV0 10:<D0>*	*Operational Mode*
X	X	0	X	X	X	Sleep
X	X	1	0	X	X	Idle
1	0	1	1	0	0	Read
0	1	1	1	0	0	Write
0	0	1	1	0	0	Write Bias Active
0	1	1	1	0	1	Servo [1]
0	1	1	1	1	0	Servo [1]
0	1	1	1	1	1	Servo [1]
0	0	1	1	1	1	Servo Bias Active

1. SERVO0 and SERVO1 settings must match, or a Servo fault. See Table 85.

Table 84 Multiple Preamplifier Addressing

Pin/Address Values		*Selected Preamp*
CS1/A2	*CS0/A1*	
0	0	0
1	0	1
0	1	2
1	1	3

Note: Address bits A1 and A2 must match the value of CS0 and CS1 to correctly address the preamplifier. See Table 87 for Preamplifier Addressing.

Sleep Mode

In the sleep mode power consumption is minimized. All outputs are disabled (except in test mode). The writer current source and the reader bias current/voltage source are deactivated while the RDN/RDP outputs and the WDX/WDY inputs switch to a high impedance state. Faults are not detected in Sleep Mode.

Sleep mode is selected by setting 4:<D2> = 0, see Tables 83, 88 and 89.

Note: Always transition from Sleep to Idle mode 10 µs before entering an active mode.

Idle Mode

The internal write current generator, write current source and read bias current/voltage source are deactivated while the RDN/RDP outputs and the WDX/WDY inputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. Faults are not detected in Idle Mode.

Idle mode is triggered by setting 4:<D3> = 0, see Tables 83, 88 and 89.

Dummy Mode

Setting DUMMY (1:<D5>) high directs the MR bias current/voltage to an internal dummy head. This maintains the reader bias at operational levels for quick read recovery.

Test Modes

Test modes allows the user to calculate the read head resistance or to monitor the die temperature or buffered head voltage.

Read Head Resistance

The resistance of the MR head can be measured in three ways: an automatic digital conversion, an iterative method using DBHV and threshold settings to trigger or not trigger a fault, or by monitoring the ABHV output.

Digital Conversion

To perform digital conversion of the read head resistance:

1) Place device in Read Mode (see Table 83).
2) Set the RMR/TEMP bit (8:<D7>) low to enter the MR resistance measurement mode.
3) Set DIGON bit (9:<D1>) high and wait 50us for the preamp to convert the resistance. (DIGON automatically resets low when the conversion is complete.)
4) The resistance is stored in DSTR0-6 as a 7-bit word in a direct binary format. For example, if 9:<D7-D1> =

0010000 the MR head resistance is 16 ohms. (The measurement range for MR resistance is 0 - 127 Ω.)

Note: MR bias current is always enabled in this mode.

Iterative Resistance Reading

To perform the iterative resistance reading:

1) Place device in Read Mode (see Table 83).
2) Set the DBHV bit high (1:<D4> = 1) to enter the MR resistance measurement mode.
3) Monitor the FLT/ABHV/DBHV pin to determine the voltage across the MR element:
   - A high indicates the voltage is within the window (150mv to 320mv).
   - A low indicates the voltage is outside the window.
4) Vary the MR bias current (2:<D2-D7>) to determine where the defined thresholds are crossed. The FLT line is not valid until the I_{MR} change settles; values for this are listed in "READ CHARACTERISTICS" on page 215.
5) Resistance can be inferred from the threshold settings.

Buffered Head Voltage

To output the MR head voltage on the FLT/ABHV/DBHV pin:

1) Place device in Read Mode (see Table 83).
2) Set ABHV bit (1:<D7>) high to output the MR head voltage as scaled by a gain of 5.

Note: If ABHV and DBHV are both high, ABHV takes precedence. See the truth table in PIN FUNCTION LIST AND DESCRIPTION on page 211.

Die Temperature Monitoring

The die temperature range is 0°C to 150°C. To measure the die temperature:

1) Set RMR/TEMP (8:<D7>) high to enable the die temperature.
2) Set DIGON bit (9:<D0>) high and wait 50us for the preamp to convert the temperature. (DIGON automatically resets low when the conversion is complete.)
3) The die temperature is stored in DSTR0-6 as a 7-bit word in a binary format using the formula below. For example, if 9:<D7-D1> = 0100000 the die temperature is 38°C (32°C x 1.18).

$$T = 1.18k \qquad \textit{(eq. 41)}$$

where k = 0 - 127 and T is degrees Centigrade

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the reader element which correspond to flux changes on the disk.

Read mode is selected by setting the R/WN pin high. In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM546112 uses the voltage-sensing reader architecture with biasing programmable as current or voltage. The magnitude of the reader bias current/voltage is set to the value programmed in 2:<D2-D7>. The equations below govern the read bias current/voltage magnitude:

$$\text{Current Mode} \quad I_{MR} = 2 + [k_{IMR} \cdot 0.127]\text{mA} \qquad \textit{(eq. 42)}$$

$$\text{Voltage Mode} \quad V_{MR} = 100 + [k_{IMR} \cdot 6.35]\text{mV} \qquad \textit{(eq. 43)}$$

k_{IMR} = 0 to 63

The reader operates in one of two constant bias modes:

- Current bias mode is selected by setting 1:<D6> = 0, and
- Voltage bias mode is selected by setting 1:<D6> = 1.

Note: Any transition between current and voltage bias modes must occur in the Sleep mode.

In the current bias mode a constant current is applied to the MR element. In voltage bias mode a constant voltage is applied to the MR element. The applied value is programmed in 2:<D2-D7>.

Read head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

The reader enters a fast recovery mode during modal transitions, serial register operations, and when the reader is biased during a write mode. The fast recovery mode minimizes signal anomalies on the reader outputs.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT/ABHV/DBHV or the TA pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 91.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, 7:<D6-D0> as shown in Table 92. The default setting (0000) is to enable all faults.

Fault codes may be cleared by setting the Clear Fault bit, 7:<D7> = 1. The following are valid read fault conditions:

- MR Bias Not Enabled
- MR Overcurrent
- Thermal Asperity Detected [1]
- Read Head Open
- Low V_{CC}, V_{DDM} or V_{EE}
- Overtemperature

1. Thermal asperity is flagged on TA pin, all other flagged on FLT/ABHV/DBHV pin.

Read Gain

The default gain is 100 V/V with a head resistance of 55Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in 3:<D2-D3>. The formula that describes the actual gain is shown below:

$$GAIN = \frac{475}{420 + R_{MR}}[100 + 50(k_{GAIN})] \qquad \textit{(eq. 44)}$$

k_{GAIN} = 0-3

Reader Boost

Setting Reader Boost (RB) bit high (8:<D5> = 1) increases the read gain by 3dB at 80 MHz.

Fast Mode

Setting the FAST bit (1:<D1>) high in read mode, raises the low corner frequency to 5MHz. If the FAST bit is low, the low corner frequency is set to the value programmed in LFP (3:<D0-D1>).

Thermal Asperity Detection and Recovery

Detection

Setting the TAD bit high (5:<D6>) enables positive or negative thermal asperity detection.

If a head-to-disk contact occurs, the thermal asperity in the read element will result in a fault condition. The range of the voltage threshold is governed by the following equation and is set in 5:<D0-D4>:

$$V_{TAT} = 50 + \left[900 \times \left(\frac{k_{TAT}}{31}\right)\right] \quad \textit{(eq. 45)}$$

V_{TAT} represents the TA threshold (output-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-31).

Note that a fault condition resulting from a thermal asperity will remain active until the positive or negative hysteresis is ≤20% of the threshold.

A TA fault is reported on the TA pin, not the FLT pin. The TA and FLT pins may be externally connected to a common point as shown in the TYPICAL CONNECTION DIAGRAM on page 212.

Fast Recovery

Setting the TA Compensation (TAC) bit high (5:<D5> = 1) automatically initiates the Fast Recovery mode if a thermal asperity is detected.

The low frequency corner is raised to 5MHz from the nominal value programmed in 3:<D0-D1>. Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled in 5:<D6>, and TA pin is inactive when preamp is in write mode.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the head.

Write mode is selected by setting the R/WN pin low.

The magnitude of the write current is determined by the write current registers (4:<D3-D7>). The following equation governs the write current magnitude:

$$I_W = 15 + (k_{IW} \cdot 1.61)\,mA \quad \textit{(eq. 46)}$$

I_W represents the write current (mA flowing to the selected head).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 64 for the timing diagram on page 218.

Write Current DAC

Register 4:<D3-D7> represent the binary equivalent of the DAC setting (0-31).

Read Bias Enabled in Write Mode

Taking the BIASN pin low (at least 5µs before the R/WN pin is set high) enables reader bias current/voltage to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (1:<D1>) initiates Write Data Inputs in Voltage Mode. Setting the WVORI bit high initiates the Write Data Inputs in Current Mode.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT/ABHV/DBHV pin indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 91.

Specific fault conditions may be disabled by setting the Fault Reporting Mask, 7:<D0-D6> as shown in Table 92. The default setting (000000) is to enable all faults.

Fault codes may be cleared setting the CLRFC, 7:<D7>, high.

The following are valid write fault conditions:

- Write Data Frequency Low
- Open or Shorted Write Head
- Servo Fault
- Low V_{CC}, V_{DDM} [1] or V_{EE} [2]
- Overtemperature
- Invalid Head Selected

1. If V_{DDN} is not supplied, the fault is disabled.
1. Low V fault disables write current until proper level is restored.

Servo Write Mode

In the servo write mode, up to eight channels may be written simultaneously.

Table 89 indicates how heads can be selected for individual or simultaneous writing.

Note: VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.

Setting both the SERVO0 and SERVO1 bits (10:<D0> and 3:<D7>) to ‘1’ and holding the R/WN pin low places the preamp in servo write mode (see Table 83).

The BANK bit (10:<D7>) permits writing to even or odd head combinations: high writes to even and low writes to odd heads. A high in SHDn (10:<D1-D6> selects the specific head on which to perform the servo write. The default setting is to select no heads (10:<D7> = 0 and 10:<D1-D6> = 000000).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the device.)

A servo fault is generated if the SERVO0 and SERVO1 (10:<D0>, 3:<D7>) settings do not match as shown in Table 85.

Table 85 Servo Faults

SERVO1 3:<D7>	*SERVO0 10:<D0>*	*Mode*	*Fault*
0	0	Active [1]	No
1	0	Active [1]	Yes
0	1	Active [1]	Yes
1	1	Servo	No

1. Active includes all modes (read, write, idle, sleep or test), except servo.

SERIAL PORT

Serial Interface

The VM546112 uses a 3-line read/write serial interface for control of most chip functions including head selection, reader bias current/voltage magnitude and write current magnitude. See Tables 87 and 88 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16-bits constitute a complete data transfer as shown in Figure 61.

- The first 8-bits <A7-A0> are write-only and consist of:
  - one read/write command bit <A0> (high for read, low for write),
  - two preamp address bits <A2-A1>,
  - four register address bits <A6-A3>, and
  - one unused bits <A7>.
- The second 8-bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 8th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and the data will be clocked from the SDIO line on subsequent rising edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode. The reader invokes a *fast* mode while a serial interface operation occurs.

See Tables 87 and 88 for a bit description. See Table 86, and Figures 62 and 63 for serial interface timing information.

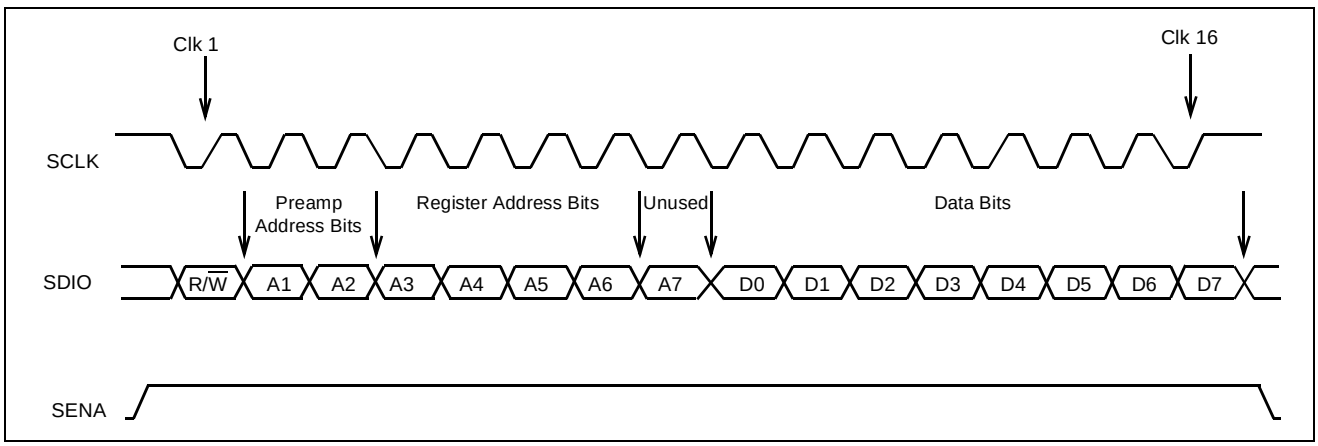


Figure 61 Serial Port Protocol

Table 86 Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) rate, write				40	MHz
SENA to SCLK delay	T_{sens}	**TBD**			nS
SDIO setup time, write	T_{wds}	**TBD**			nS
SDIO delay time, read	T_{rds}	**TBD**		**TBD**	nS
SDIO hold time	T_{dh}	**TBD**			nS
SCLK cycle time	T_{c}	**TBD**			nS
SCLK high time	T_{ckh}	**TBD**			nS
SCLK low time	T_{ckl}	**TBD**			nS
SENA hold time	T_{shld}	**TBD**			nS
Time between I/O operations	T_{sl}	**TBD**			nS
Time to activate SDIO	T_{act}	**TBD**		**TBD**	nS
Duration of SerEna (read)	T_{rd}	**TBD**			nS
Duration of SerEna (write)	T_{wt}	**TBD**			nS

Note: SENA assertion level is high.

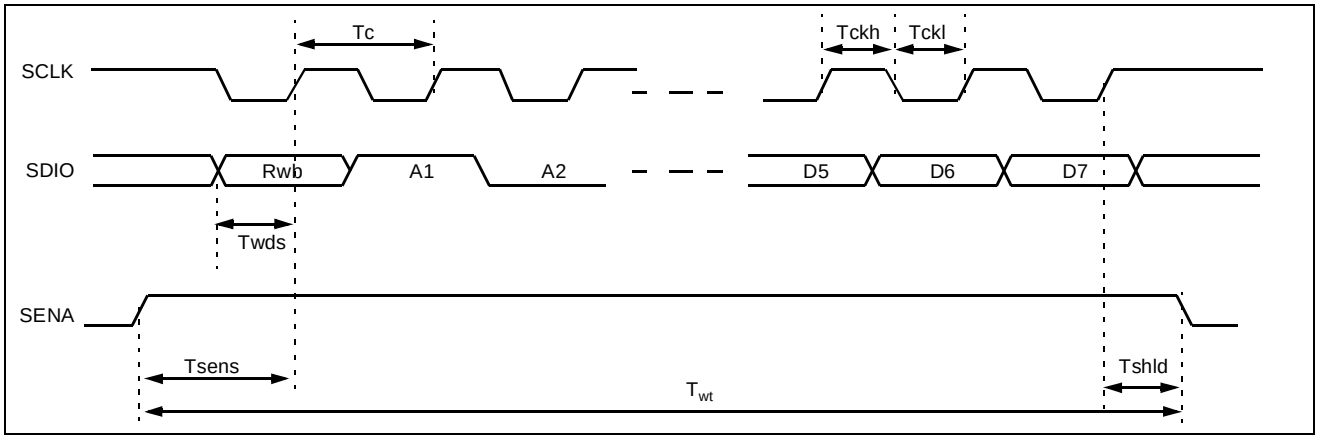


Figure 62 Serial Port Timing - Write Operation

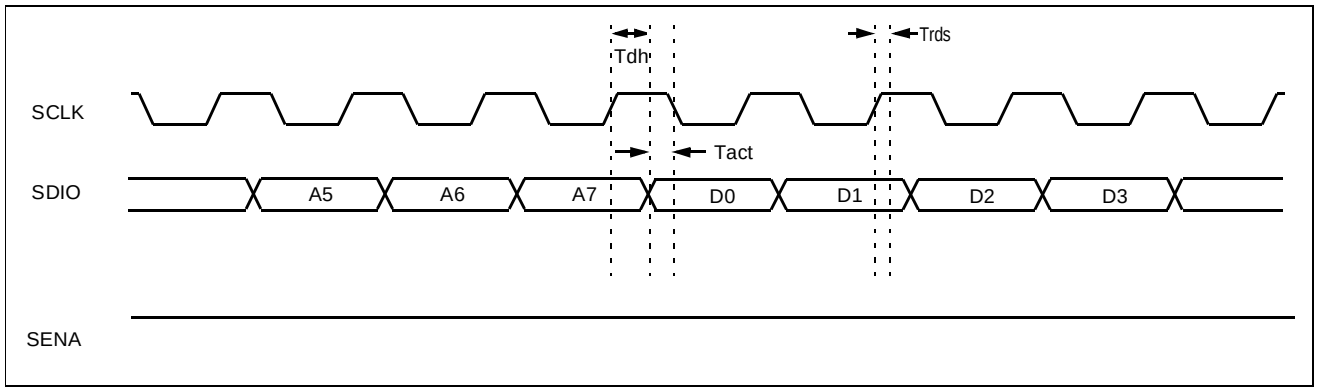


Figure 63 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 87 lists the serial address for each register. Table 88 lists the data contents of the register set. A description of the individual bits is provided in Table 89.

Table 87 Serial Interface Addressing

Register #	Register Address Bits				Preamp Address Bits			R/W Bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	X	0	0	0	0	Preamplifier Select Bits See Table 84 for valid addressing values with multiple preamps.		0 = write 1 = read
1	X	0	0	0	1			
2	X	0	0	1	0			
3	X	0	0	1	1			
4	X	0	1	0	0			
5	X	0	1	0	1			
6	X	0	1	1	0			
7	X	0	1	1	1			
8	X	1	0	0	0			
9	X	1	0	0	1			
10	X	1	0	1	0			

Table 88 Serial Interface Bit Map - Base Registers

Function	Register #								Data Bits
		<D0>	<D1>	<D2>	<D3>	<D4>	<D5>	<D6>	<D7>
Head Select	0	[1]	[1]	[1]	[1]	HS0	HS1	HS2	HS3
Control	1	FAST	WVORI	SLEEPN	IDLEN	DBHV	DUMMY	I/V	ABHV
IMR	2	GAIN0	GAIN1	IMR0	IMR1	IMR2	IMR3	IMR4	IMR5
Poles	3	LFP0	LFP1	BW0	BW1	USC0	USC1	USC2	SERVO1
Write Current/	4	OSC0	OSC1	OSC2	IW0	IW1	IW2	IW3	IW4
Thermal Asperity	5	TAD0	TAD1	TAD2	TAD3	TAD4	TAC	TAD	[1]
Vendor ID	6 [2]	VEND0	VEND1	VEND2	VEND3	VEND4	REV0	REV1	REV2
Fault Mask/Clear	7	FLT0	FLT1	FLT2	FLT3	FLT4	FLT5	FLT6	CLRFC
Fault Code	8	FCOD0	FCOD1	FCOD2	FCOD3	[1]	RB	TTOSC	RMR/ TEMP
Data Storage/Digital	9	DIGON	DSTR0	DSTR1	DSTR2	DSTR3	DSTR4	DSTR5	DSTR6
Servo	10	SERVO0	SHD0/1	SHD2/3	SHD4/5	SHD6/7	SHD8/9	SHD10/11	BANK

1. Reserved.
2. Read Only Register/Bits:
   Register 6:<D0-D4> is the Vendor ID code (VTC=**TBD**),
   Register 6:<D5-D7> is the Vendor revision code. Initial revision shall be (REV0 = 0, REV1 = 0, REV2 = 0),

Table 89 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description				
0	D0-D3	Reserved						
	D4-D7	Head Select	HSn	Binary selection of head	HS3	HS2	HS1	HS0
				Head Select	0:<D7>	0:<D6>	0:<D5>	0:<D4>
				0	0	0	0	0
				1	0	0	0	1
				2	0	0	1	0
				3	0	0	1	1
				4	0	1	0	0
				5	0	1	0	1
				6	0	1	1	0
				7	0	1	1	1
				8	1	0	0	0
				9	1	0	0	1
				10	1	0	1	0
				11	1	0	1	1
1	D0	Fast Mode	FAST	Raises low corner frequency 5 MHz 0 = Disable 1 = Enable				
	D1	Write Voltage or Current	WVORI	0 = Voltage mode write data inputs. 1 = Current mode write data inputs. Note: VTC recommends using Voltage mode as the write data input when servo writing in a multiple preamp application.				
	D2	Sleep	SLEEPN	0/1 = See Table 83, “Mode Select,” on page 200 Note: This bit has precedence over the IDLEN bit (1:<D3>).				
	D3	Idle Mode	IDLEN	0/1 = See Table 83, “Mode Select,” on page 200 Note: The SLEEPN bit (1:<D2>) has precedence over this bit.				
	D4	Digital Buffered Head Voltage Output	DBHV	0 = Disable 1 = Enable Note: DBHV is overridden when ABHV (1:<D7>) is enabled.				
	D5	Dummy MR Head Load	DUMMY	0 = MR Head selected using HSn register (0:<D4-D7>) setting. 1 = Dummy head resistive load selected.				
	D6	Current or Voltage Bias	I/V	0 = Current bias mode. 1 = Voltage bias mode. Note: Bias level is set in registers 2:<D2-D7> Note: Any transition between current and voltage bias modes must occur in the Sleep mode.				
	D7	Analog Buffered Head Voltage Output	ABHV	0 = Disable 1 = Enable Note: ABHV overrides DBHV (1:<D4>).				

Table 89 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description		
2	D0-1	Gain	GAINn	Binary selection of MR Reader Gain least significant bit:	GAIN1	GAIN0
				Gain	2:<D1>	1:<D0>
				100 V/V	0	0
				150 V/V	0	1
				200 V/V	1	0
				250 V/V	1	1
	D2-D7	Bias Level	IMRn	Binary selection of MR Head Current Bias least significant bit Current Bias = 2mA (000000) to 10mA (111111) in 0.127mA increments. Voltage Bias = 100mV (000000) to 500mV (111111) in 6.35mV increments. Note: Current or Voltage Bias selected in 1:<D6>.		
3	D0-D1	Low Frequency (-3dB) Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth:	LFP1	LFP0
				Low Frequency Bandwidth	3:<D1>	3:<D0>
				1 MHz	0	0
				2 MHz	0	1
				3 MHz	1	0
				5 MHz	1	1
	D2-D3	Bandwidth	BWn	Binary selection of Bandwidth:	BW1	BW0
				Bandwidth	3:<D3>	3:<D2>
				200 MHz	0	0
				250 MHz	0	1
				300 MHz	1	0
				350 MHz	1	1
	D4-D6	Undershoot Control	USCn	Undershoot Control **TBD** % (000) to **TBD** % (111) in **TBD** % increments.		
	D7	Servo Bank 1	SERVO1	0/1 = See Table 85, “Servo Faults,” on page 202 Note: SERVO0 (10:<D0>) must also be selected for a valid servo write. Note: Register 10:<D1-D6> defines which heads to servo write.		
4	D0-D2	Overshoot Control	OSCn	Overshoot Control **TBD** % 000) to **TBD** % (111) in **TBD** % increments.		
	D3-D7	Write Current	IWn	Binary selection of Write Current 15 mA (00000) to 65 mA (11111) in 1.6 mA increments.		
5	D0-D4	Thermal Asperity Threshold - MSB	TAn	Binary selection of Thermal Asperity Threshold TA Range = 50 mV (00000) to 949 mV (11111) in increments of 29 mV.		
	D5	Thermal Asperity Compensation	TAC	0 = No TA Compensation. 1 = TA Compensation selected. Note: TA Detection must be enabled in 5:<D6> for TAC to function.		
	D6	Thermal Asperity Detection	TAD	0 = TA Detection disabled. 1 = TA Detection enabled.		
	D7	Reserved				
6	D0-D4	Vendor Code	VENDn	Binary Vendor Code (10000 = VTC)		
	D5-D7	Revision of Part	REVn	Binary Revision Count: Revision 1 (000) to Revision 8 (111). Count restarts at 1 after exceeding 8.		

Table 89 Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
7	D0-D6	Fault Mask	FLTn	Fault Reporting Mask See Table 92.
	D7	Clear Fault Codes	CLRFC	0 = Retain faults 1 = Clear faults Note: CLRFC resets to 0 after fault codes clear.
8	D0-D3	Fault Condition	FCODEn	Binary code of Fault(s) See Table 91.
	D4	Reserved		
	D5	Read Boost	RB	0 = Disable 1 = Enable
	D6	Test Bit	TTOSC	Manufacturer's test bit - Reserved
	D7	MR Head Resistance or Die Temperature	RMR/ TEMP	0 = MR Head Resistance stored in DSTRn register (9:<D1-D7>). 1 = Die Temperature stored in DSTRn register (9:<D1-D7>).
9	D0	Internal Digital Conversion	DIGON	0 = Analog-to-digital conversion off 1 = Start analog-to-digital conversion Note: DIGON resets to 0 when analog-to-digital conversion completes. Note: Reader Resistance or Die Temperature output is selected in TBD and the measurement is stored in 9:<D1-D7>.
	D1-D7	Data Storage	DSTRn	Data storage of binary output from MR Head Resistance or Die Temperature: Resistance range is 0 to 127 Ohms. Temperature range is 0 to 150^{o}C. Note: 9:<D0> selects analog or digital output.
10	D0	Servo Bank 0	SERVO0	0/1 = See Table 85, "Servo Faults," on page 202 Note: SERVO1 (3:<D7>) must also be selected for a valid servo write. Note: Register 10:<D1-D6> defines which heads to servo write. Default is to servo write all heads (see Table 90).
	D1-D6	Servo Head Select	SHDn	Binary selection of the head pairs to be servo track written. - Bit 1 = 1 *selects* HD0 or HD1. - Bit 2 = 1 *selects* HD2 or HD3. - Bit 3 = 0 *deselects* HD4 or HD5. - Bit 4 = 0 *deselects* HD6 or HD7. - Bit 5 = 0 *deselects* HD8 or HD9. - Bit 6 = 0 *deselects* HD10 or HD11. Register 10:<D7> defines whether even or odd numbered heads are selected from the active pairs. Default is no head selected (see Table 90). Examples when the default (odd) head bank is selected (10:<D7> = 0): 1. 001000 = Servo Write Head 7. 2. 000011 = Servo Write Heads 1 and 3. Note: SERVO0 and SERVO1 (10:<D0> and 3:<D7>) must be selected to servo write.
	D7	Servo Bank Select	BANK	0 = Odd head bank selected 1 = Even head bank selected Note: Register 10:<D1-D6> defines the head combinations to servo write. Default is to servo write the odd head bank (see Table 90). Note: SERVO0 and SERVO1 (10:<D0> and 3:<D7>) must be selected to servo write.

Table 90 Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Head Select	0	<0000 XXXX>
Control	1	<0000 0000>
Bias/Gain	2	<0000 0000>
Poles	3	<0100 1100>
Write Current/Overshoot	4	<0000 0100>
Thermal Asperity	5	<0000 0000>
Vendor ID	6	<XXXX XXXX>
Fault Mask/Clear	7	<0000 0000>
Fault Code	8	<0X0X 0000>
Data Storage/Digitization	9	<0000 0000>
Servo	10	<0000 0000>

Fault Reporting and Masking

Table 91 Fault Conditions and Codes

Fault Code 8:<D3-D0>	Fault	Priority [1]	Valid Mode(s)	Mask [2]	Conditions
0000	No Fault	–	Read or Write	–	
0001	Reserved	–	–	–	
0010	MR Overcurrent	2	Read	M	
0011	Thermal Asperity Detected	6	Read	M	
0100	Read Head Open	7	Read	M [3]	
0101	Reserved	–	–	–	
0110	Write Data Frequency Low	5	Write	M	
0111	Write Head Open/Shorted	3	Write	M	
1000	Servo Fault	8	Write		Unmatched servo bank bits
1001	Low V_{CC}, V_{DDM} or V_{EE}	1	Read or Write	M	Disables write current until proper voltage level is restored
1010	Reserved	–	–	–	
1011	Overtemperature	9	Read or Write	M	Temp > 140^{O}C
1100	Reserved	–	–	–	
1101	Reserved	–	–	–	
1110	Reserved	–	–	–	
1111	Reserved	–	–	–	

1. First fault reported is latched until a higher priority fault is reported or the code is cleared.
2. See Table 92 for an explanation of fault masking.
3. Single bit masks both faults.

Setting the appropriate bit(s) listed in Table 92 masks the fault(s) at both the fault register and the FLT pin. If 7:<D7-D0> = 0000 0101, an MR Overcurrent fault is masked with the 7:<D0> bit and Read Head Open and Read Head Shorted faults are masked with the 7:<D2> bit.

Table 92 Fault Masking

Mask Bit Register 7	Fault(s) Masked [1]	Mask Bit Register 7	Masked Fault
<D0>	MR Overcurrent	<D4>	Write Head Open/Shorted
<D1>	Thermal Asperity Detected	<D5>	Low V_{CC}, V_{DDM} or V_{EE}
<D2>	Read Head Open	<D6>	Overtemperature
<D3>	Write Data Frequency Low	Note: Setting <D7> = 1 clears all fault codes in 8:<D0-D3>.	

1. Single bit masks both Read Head Open and Read Head Shorted faults.

PIN FUNCTION LIST AND DESCRIPTION

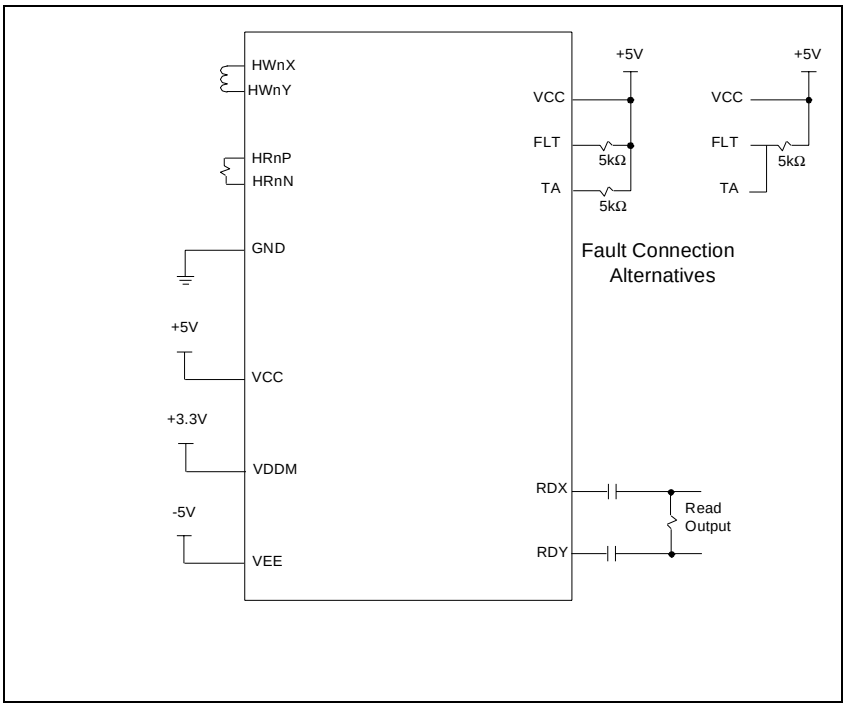
Signal	*Input/Output*	*Logic Level Default* [1]	*Description*
FLT/ABHV/DBHV	O [2]	–	Write/Read Fault and Buffered Head Voltage (Analog or Digital) as shown in truth table: • Fault (FLT) output: - A TTL high level indicates a fault in write mode. - A TTL low level indicates a fault in read mode. • Analog or Digital Buffered Head Voltage output when ABHV and/or DBHV is enabled.
GND	[2]	–	Ground
HR0N-HR11N	I	–	Read head connections, negative end.
HR0P-HR11P	I	–	Read head connections, positive end.
HW0X-HW11X	O	–	Thin-Film write head connections, positive end.
HW0Y-HW11Y	O	–	Thin-Film write head connections, negative end
R/WN	I [2]	high	Read/Write: A TTL low level enables write mode.
BIASN		high	MR Bias: • A TTL low level enables bias current through the active head.
RDP, RDN	O [2]	–	Read Data: Differential read signal outputs.
SCLK	I [2]	low	Serial Clock: Serial port clock; see Figure 61.
SDIO	I/O [2]	low	Serial Data: Serial port data; see Figure 61.
SENA	I [2]	low	Serial Enable: Serial port enable; see Figure 61.
TA	O [2]	high	Thermal Asperity: • When 5:<D6> = 1 (TA Detection enabled): - A TTL high level indicates no TA. - A TTL low level indicates a TA exceeded the threshold programmed in 5:<D0-D4>. **Note:** TA pin is inactive when preamp is in write mode.
VCC	[2]	–	+5.0V supply
VDDM	I [2]	–	+3.3V supply, monitor pin only
VEE	[2]	–	-5.0V supply
WDX, WDY	I [2]	high	Differential Pseudo-ECL write data inputs

Output	*ABHV 1:<D7>*	*DBHV 1:<D4>*
FLT	0	0
DBHV	0	1
ABHV	1	0
ABHV [1]	1	1

1. ABHV overrides DBHV setting. Output is Analog Buffered Head Voltage (ABHV).

1. 40kΩ pullup/pulldown resistors are used to default pins to specified high or low levels.
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- Minimum FLT pullup resistance is 5 kΩ.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		92	**TBD**	mA
		Write Mode		93	175	
		Write Mode, Reader Biased		135	**TBD**	
		Idle Mode		15	**TBD**	
		Sleep Mode		500	**TBD**	µA
V_{EE} Power Supply Current	I_{EE}	Read Mode		38	**TBD**	mA
		Write Mode		68	150	
		Write Mode, Reader Biased		86	**TBD**	
		Idle Mode		2	**TBD**	
		Sleep Mode		20	**TBD**	µA
Power Supply Dissipation	P_d	Read Mode		650	**TBD**	mW
		Write Mode		805	**TBD**	
		Write Mode, Reader Biased		1105	**TBD**	
		Idle Mode		85	**TBD**	
		Sleep Mode		2.6	**TBD**	
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	mA
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	
Input High Current, V_{IH} = 2.0V	I_{IH}	PECL			120	µA
		TTL			80	
Input Low Current, V_{IL} = 0.5V	I_{IL}	PECL			100	µA
		TTL	-160			
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output High Voltage	V_{OH}	TTL, I_{OH}=**TBD**	2.40		V_{CC}	V
Output Low Voltage	V_{OL}	TTL, I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{CTH}		3.75	4.0	4.25	V
V_{DDM} Fault Threshold	V_{DTH}	Hysteresis = 100mV ±10%, Fault not detected below 1 VDC.	2.0	2.25	2.5	V
V_{EE} Fault Threshold	V_{ETH}		-4.25	-4.0	-3.75	V
High Level WDATA		PECL	1.9		V_{CC}	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL	1.5		V_{IH} - 0.4	V
		Current Mode (sink)	0.8	2.0	4.0	mA
WDATA PECL swing		Voltage mode differential	0.4		1.5	V_{pp}

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage compliance for WDATA		CMM of inputs when in current mode			V_{CC} -2.3	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Reader Head Current Range	I_{MR}		2		10	mA
Reader Head Current Tolerance		2 mA < I_{MR} < 10 mA,	-5		+5	%
Reader Head Voltage Range	V_{MR}		100		500	mV
Reader Head Voltage Tolerance		100 mV < V_{MR} < 500 mV,	-5		+5	%
Unselected Reader Head Current					100	µA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 20MHz, R_{Ldiff} = **TBD**, Gain Bits = 00		100		V/V
		Gain Bits = 11		250		V/V
Gain Boost	BOOST	f = 80 MHz, Gain bit = 0, RB bit = 1		3		dB
Passband Upper Frequency Limit	f_{HR}	-1dB	**TBD**	**TBD**	**TBD**	
		No Boost, -3dB		350		
Passband Lower Frequency Limit	f_{LR}	-1dB	**TBD**	**TBD**	**TBD**	
		-3dB, normal mode, LFP = 00		1		MHz
Input Noise Voltage	e_n	1 MHz < f < 100 MHz		0.55		nV/√Hz
Input Noise Bias Current	i_n	I_{MR} = 8 mA, Noise independent of I_{MR} 1 MHz < f < 100 MHz		8		pA/√Hz
Noise Peaking		1 MHz < f < 10 MHz			**TBD**	dB
		10 MHz < f < 200 MHz			**TBD**	dB
Differential Input Capacitance	C_{IN}			2	4	pF
Differential Input Resistance	R_{IN}			400		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = **TBD** @ f = 20 MHz	6			mV_{pp}
Common Mode Rejection	CMRR	V_{CM} = **TBD** mVpp, 10 MHz < f < 200 MHz	40			dB
		1 MHz < f < 10 MHz	40			
		f < 100 kHz	60			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5mA, L_{MR} = 30nH, R_{MR} = 55Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Rejection	PSRR	100mV$_{pp}$ on V_{CC} or V_{EE}, 10 MHz < f < 200 MHz	40			dB
		100mV$_{pp}$ on V_{CC} or V_{EE}, 1 MHz < f < 10 MHz	40			
		100mV$_{pp}$ on V_{CC} or V_{EE}, f < 100 kHz	60			
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV$_{pp}$, 1 MHz < f < 200 MHz	50			dB
Rejection of SCLK and SDIO		100 mV$_{pp}$ on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-	50		mV
Common Mode Output Voltage	V_{OCM}			2.0		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)		50		mV
Reader Head Resistance	R_{MR}		30	55	80	Ω
Single-Ended Output Resistance	R_{SEO}			25		Ω
Output Current	I_O		4			mA
Total Harmonic Distortion	THD				0.5	%
Reader Head Potential, Selected Head	V_{MR}	Any point to GND	-500		500	mV
Reader Head Potential, Unselected Head	V_{MR}				-0.9	V
Reader Differential Voltage (I_{MR}*R_{MR})					700	mV
Reader Bias Current Settling Time	T_{RSET}	I_{MR} = 4 mA, R_{MR}=100Ω.		**TBD**		nS
Reader Bias Current Overshoot					2.5	%
TA Detection Response Time		TA occurred to FLT active			40	nS
Group Delay Variation		(20 - 3 dB cutoff) MHz		**TBD**		nS
MR Measurement Accuracy				5		%
Temperature Measurement Accuracy				2		^{o}C
BHV Gain			4.75	5	5.25	V/V

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50mA b-p, L_H = 70nH, R_H = 10Ω, f_{DATA} = 5MHz, $0^o<T_J<125^oC$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		15		65	mA
Write Current Tolerance	ΔI_W	$15 < I_W < 65$ mA	-8		8	%
Write Servo Current Tolerance			-10		10	%
Differential Head Voltage Swing	V_{DH}	Open Head	8			V_{PP}
Unselected Head Transition Current	I_{UH}				1	mA_{pk}
Differential Output Capacitance	C_O			6		pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Time for Fault Inhibit	f_{DATA}	Minimum bit transition time	7			nS
Write Current Settling Time	t_{WSET}	I_W = 50 mA b-p, Head model provided			**TBD**	nS
Write Data Input Terminal Resistor	w_{RIH}			300		Ω
Write Current Overshoot	W_{COV}	I_W = 50 mA b-p, Head model provided WCP0=0, WCP1=0, WCP2=0		**TBD**		%

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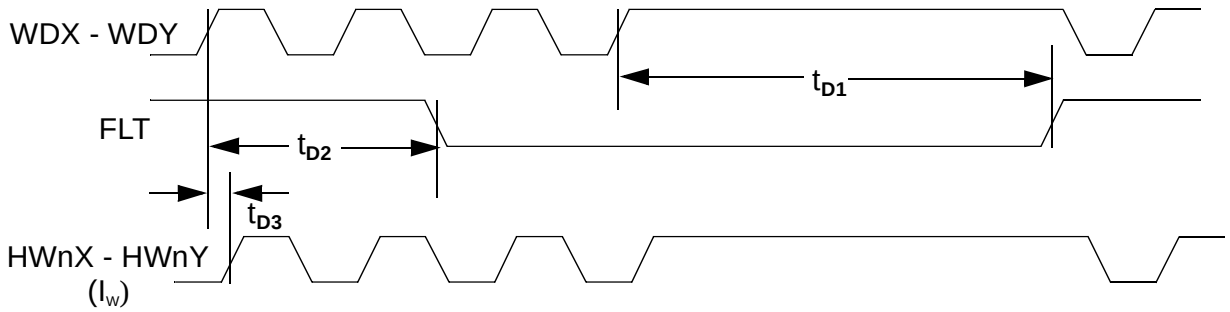
SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write envelope		30	50	nS
R/WN to Read Mode	t_{WR}	To 90% of data envelope or 20 mV DC			300	nS
		To 10% of I_W envelope			50	nS
Idle to Read Mode (SCLK 16th rising edge)	t_{IR}	To 90% of envelope, DC Offset Level within 20 mV			5	µS
HS0-HS2 to Any Head (SCLK 16th rising edge)	t_{HS}	To 90% of envelope, DC Offset Level within 20 mV, **TBD** - Fixed I_{MR}.			1	µS
		To 90% of envelope, DC Offset Level within 20 mV, Head Voltage Change not to exceed 150 to 400 mV, Variable I_{MR}.			3	µS
Active (16th rising edge) to Idle	t_{RI}	To 10% of read envelope or write current			50	nS
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT		1.5		µS
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT		100		nS
Head Current Propagation Delay [1]	t_{D3}	From 50% points, L_H=0, R_H=13Ω.		5		nS
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 0.5nS rise/fall time, L_H=0, R_H=**TBD**			100	pS
Rise/Fall Time	t_r / t_f	10% - 90%, I_W = 50 mA b-p, L_H=70nH, R_H=10Ω.		500		pS
		Head model provided, I_W = 50 mA b-p, L_H=0nH, R_H=0Ω.				nS
Read to Servo Write		From 50%R/WN to 90% I_W			50	nS
Read to Servo Write Head Turn-on Variation					**TBD**	nS
Servo Write to Read		To 90% envelope, DC offset level to within 20mV			1	µS
Servo Write Current Turn-off Time		From 50% R/WN to 10% I_W			**TBD**	nS

1. See Figure 64 for the write mode timing diagram.



In voltage mode: When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode: When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 64 Write Mode Timing Diagram *

PACKAGING

12-Channel Die

Specific Characteristics

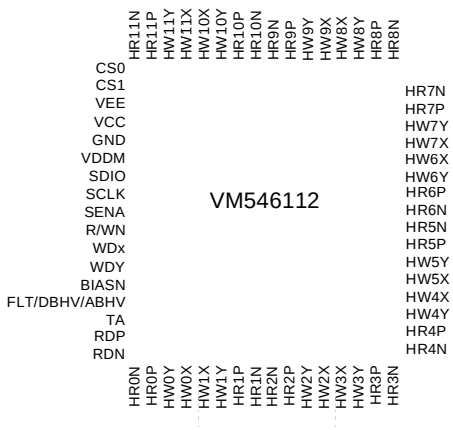
Die size: **TBD** x **TBD** Mils

Wire Bond Coordinates for the VM546112 (in Mils)

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BIASN	**TBD**	**TBD**	**TBD**
CS0	**TBD**	**TBD**	**TBD**
CS1	**TBD**	**TBD**	**TBD**
FLT/ DBHV/ ABHV	**TBD**	**TBD**	**TBD**
GND	**TBD**	**TBD**	**TBD**
GND	**TBD**	**TBD**	**TBD**
HR0N	**TBD**	**TBD**	**TBD**
HR0P	**TBD**	**TBD**	**TBD**
HR1N	**TBD**	**TBD**	**TBD**
HR1P	**TBD**	**TBD**	**TBD**
HR2N	**TBD**	**TBD**	**TBD**
HR2P	**TBD**	**TBD**	**TBD**
HR3N	**TBD**	**TBD**	**TBD**
HR3P	**TBD**	**TBD**	**TBD**
HR4N	**TBD**	**TBD**	**TBD**
HR4P	**TBD**	**TBD**	**TBD**
HR5N	**TBD**	**TBD**	**TBD**
HR5P	**TBD**	**TBD**	**TBD**
HR6N	**TBD**	**TBD**	**TBD**
HR6P	**TBD**	**TBD**	**TBD**
HR7N	**TBD**	**TBD**	**TBD**
HR7P	**TBD**	**TBD**	**TBD**
HR8N	**TBD**	**TBD**	**TBD**
HR8P	**TBD**	**TBD**	**TBD**
HR9N	**TBD**	**TBD**	**TBD**
HR9P	**TBD**	**TBD**	**TBD**
HR10N	**TBD**	**TBD**	**TBD**
HR10P	**TBD**	**TBD**	**TBD**
HR11N	**TBD**	**TBD**	**TBD**
HR11P	**TBD**	**TBD**	**TBD**
HW0X	**TBD**	**TBD**	**TBD**
HW0Y	**TBD**	**TBD**	**TBD**
HW1X	**TBD**	**TBD**	**TBD**
HW1Y	**TBD**	**TBD**	**TBD**
HW2X	**TBD**	**TBD**	**TBD**
HW2Y	**TBD**	**TBD**	**TBD**
HW3X	**TBD**	**TBD**	**TBD**

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
HW3Y	**TBD**	**TBD**	**TBD**
HW4X	**TBD**	**TBD**	**TBD**
HW4Y	**TBD**	**TBD**	**TBD**
HW5X	**TBD**	**TBD**	**TBD**
HW5Y	**TBD**	**TBD**	**TBD**
HW6X	**TBD**	**TBD**	**TBD**
HW6Y	**TBD**	**TBD**	**TBD**
HW7X	**TBD**	**TBD**	**TBD**
HW7Y	**TBD**	**TBD**	**TBD**
HW8X	**TBD**	**TBD**	**TBD**
HW8Y	**TBD**	**TBD**	**TBD**
HW9X	**TBD**	**TBD**	**TBD**
HW9Y	**TBD**	**TBD**	**TBD**
HW10X	**TBD**	**TBD**	**TBD**
HW10Y	**TBD**	**TBD**	**TBD**
HW11X	**TBD**	**TBD**	**TBD**
HW11Y	**TBD**	**TBD**	**TBD**
R/WN	**TBD**	**TBD**	**TBD**
RDN	**TBD**	**TBD**	**TBD**
RDP	**TBD**	**TBD**	**TBD**
SCLK	**TBD**	**TBD**	**TBD**
SDIO	**TBD**	**TBD**	**TBD**
SENA	**TBD**	**TBD**	**TBD**
TA	**TBD**	**TBD**	**TBD**
VCC	**TBD**	**TBD**	**TBD**
VDDM	**TBD**	**TBD**	**TBD**
VEE	**TBD**	**TBD**	**TBD**
WDX	**TBD**	**TBD**	**TBD**
WDY	**TBD**	**TBD**	**TBD**

12-CHANNEL CONNECTION DIAGRAM



12-Channel Die

VTC Inc.
Value The Customer™

VM61210S

10-CHANNEL, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE CAPABILITY

990812 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - Operates from +5 and -3 Volt Power Supplies
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current Range 8 - 15 mA
  - Read Voltage Gain = 150 V/V Typical
  - Input Noise = 0.60 nV/√Hz Typical
  - Input Capacitance = 16 pF Typical
  - Head Inductance Range = 100 nH to 500 nH
  - Fast Thermal Asperity Recovery Mode
- *High Speed Writer*
  - Write Current Range = 20 - 40 mA
  - Rise Time = 2.5 ns Typical (L_H = 220 nH, I_W = 30 mA)
  - Multi-Channel Servo Write
  - Optional WDFF as a bondable option

DESCRIPTION

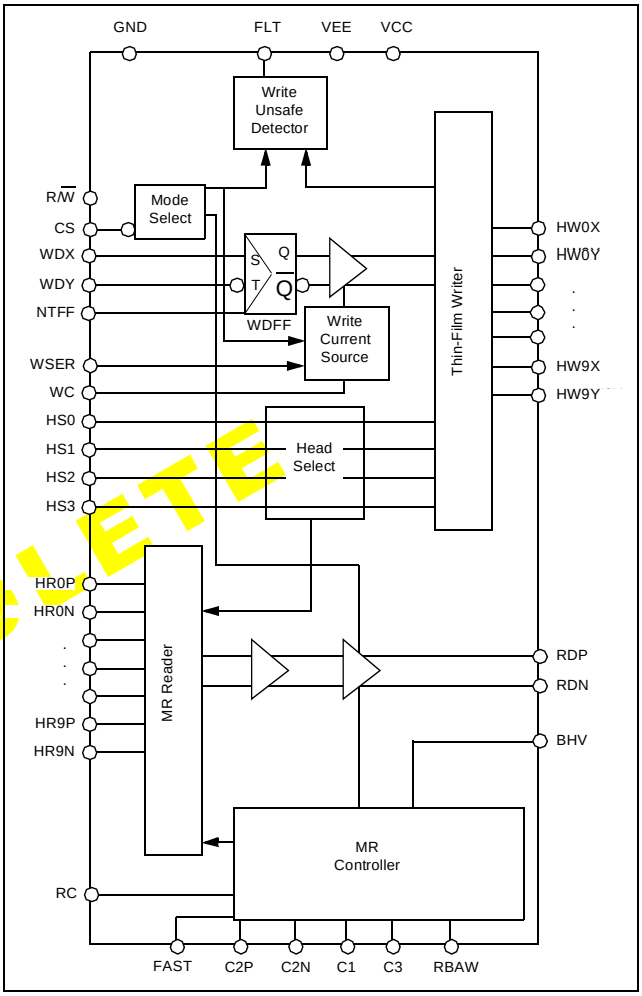
The VM61210S is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. It provides bias current and control loops for setting the DC voltages on the MR element. The VM61210S also provides a servo write feature, enabling the user to write servo information directly through the preamplifier.

Fault protection circuitry ensures that the write current generator is disabled during power sequencing, voltage faults or an invalid head select. This protects the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines (CS and R/W) to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition. Internal pull-up resistors are also provided on the FAST pin (to disable the fast thermal recovery mode) and the WSER pin (to ensure non-servo mode).

The VM61210S operates from +5V, -3V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM61210S is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -5V
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... V_{EE} -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... V_{EE} -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature 150°C

Storage Temperature T_{stg} -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{EE} ..... -3V ± 10%
V_{CC} ..... +5V ± 10%
Junction Temperature (T_J) 0°C to 125°C

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk. The bias generator, input multiplexer, read preamp and read fault detection circuitry is active.

The appropriate TTL levels on the $\overline{CS}$ and R/$\overline{W}$ lines place the preamp in the read mode (see Table 93) and activate the bias generator, the read preamp and the read fault detection circuitry.

The VM61210S uses the current bias / voltage sensing MR design. The MR bias current amplitude is determined by an external resistor or an external current source and is described by the following equation:

$$I_{MR} = \frac{40}{R_{RC}} \qquad \textit{(eq. 47)}$$

I_{MR} represents the magnitude of the bias current (in mA).
R_{RC} represents the equivalent resistance between the RC pin and ground (in kΩ).

Due to the use of a negative supply, the MR head center voltage is at ground potential minimizing current spikes during disk contact.

Fast Mode ($\overline{FAST}$)

Applying a TTL low level to the $\overline{FAST}$ pin enables the fast recovery mode. In fast mode, the first stage current is increased by a factor of three to reduce the recovery delay from a thermal asperity.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault can be triggered by any of the following conditions:

- MR bias current too high (1.5 times its programmed value)
- Low power supply voltage

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head. The write unsafe detect circuitry is activated.

The appropriate TTL levels on the $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines place the preamp in the write mode (see Table 93) and activate the write unsafe detect circuitry.

The write current magnitude is determined either by an external resistor or an external current source and is defined by the following equation:

$$I_W = \frac{40}{R_{WC} \times \left(1 + \frac{R_H}{R_D}\right)} \qquad \textit{(eq. 48)}$$

I_W represents the magnitude of the write current (in mA).
R_{WC} represents the equivalent resistance between the WC pin and ground (in kΩ).
R_H represents the series resistance of the head (in kΩ).
R_D represents the internal damping resistance (in kΩ).

Write data pseudo-ECL signals on the WDX and WDY lines drive the current switch of the thin film writer either directly or via the optional internal flip-flop.

Note: The flip-flop is enabled when the NTFF pad is connected to ground (a wire-bond option).

Fault Detection

In the write (and servo write) mode, a TTL high on the FLT line indicates a fault condition. The fault can be triggered by any of the following conditions:

- WDI frequency too low
- Open write head
- Write Head short to ground
- No write current programmed

In addition to triggering a fault the following conditions will result in the shutdown of the write current source internal to the chip:

- Low power supply voltage
- Invalid head select code
- Non-write mode

Servo Write Mode

Low TTL levels on $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$ place the chip in servo write mode.

In servo mode, five channels of the VM61210S are written simultaneously. Pin $\overline{WSER}$ controls the servo mode and pin HS0 controls which five heads are simultaneously written. See Table 2 for servo head selection description.

Note: When writing multiple heads, there is a limit to the write current duty cycle that can be used without approaching the maximum junction temperature. This maximum duty cycle is contingent on package type, number of heads selected, write current, heatsinking and airflow. DC erase using multiple heads will exceed the maximum allowable power dissipation.

Table 93 Mode Select

$\overline{CS}$	*R/$\overline{W}$*	*$\overline{WSER}$*	*MODE*
0	1	X	Read
0	0	1	Write
0	0	0	Servo
1	X	X	Idle

Table 94 Servo Mode Head Select

HS0	*DESCRIPTION*
0	Heads 0, 1, 2, 3, and 4
1	Heads 5, 6, 7, 8, and 9

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Table 95 Head Select

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Note: All other combinations select an internal dummy head.

PIN_FUNCTION LIST AND DESCRIPTION

7) $\overline{CS}$ I Chip select:
A TTL low level enables the device. The default is high (disabled).

8) R/$\overline{W}$ I [1] Read/Write:
A TTL high level enables read mode. The default is high (read mode).

9) HS0-HS3 I [1] Head Select:
Selects one of the ten heads.

10) $\overline{FAST}$ I [1] Fast Mode:
A TTL low level enables the fast thermal recovery mode. The default is high (disabled).

11) $\overline{WSER}$ I [1] Write Servo:
A TTL low level enables servo mode. The default is high (non-servo).

12) FLT O [1] Write/Read Fault:
A TTL high level indicates a fault in write mode. A low level indicates a fault in read mode.

13) WDX, WDY I [1] Write Data Inputs:
Differential Pseudo-ECL.

14) HR0P-HR9P I MR head connections,
positive end.

15) HR0N-HR9N I MR head connections,
negative end.

16) HW0X-HW9X O Thin-Film write head connections, positive end.

17) HW0Y-HW9Y O Thin-Film write head connections, negative end

18) RDP, RDN O [1] Read Data:
Differential read signal outputs.

19) WC [1] Write current reference pin:
Sets the magnitude of write current.

20) RC [1] MR bias current reference pin:
Sets the magnitude of MR bias current.

21) C1 Noise bypass capacitor input for the MR bias current source.

22) C2P, C2N Reader AC-coupling capacitor.

23) C3 Compensation capacitor for the MR head current loop.

24) BHV O [1] Buffered MR Head Voltage output.

25) NTFF The write data flip-flop is enabled when this pad is connected to ground.

26) VEE - -3.0V supply

27) VCC - +5.0V supply

28) GND - Ground

I = Input pin, O = Output pin

[1] When more than one device is used, these signals can be wire-OR'ed together.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, I_w = 30mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Power Supply Current	I_{CC}	Read Mode		75	88	mA
		Write Mode		123	143	
		Idle Mode		4.5	5	
		Fast Mode		98	118	
		Servo Mode, I_W = 20mA		243	278	
V_{EE} Power Supply Current	I_{EE}	Read Mode		51	61	mA
		Write Mode		91	106	
		Idle Mode		1.15	1.5	
		Fast Mode		71	86	
		Servo Mode, I_W = 20mA		201	226	
Power Supply Dissipation	P_d	Read Mode		528	686	mW
		Write Mode		888	1136	
		Idle Mode		26	33	
		Fast Mode		703	933	
		Servo Mode, I_W = 20mA		1818	2275	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{CC} - 1.9		V_{CC} - 1.6	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{CTH}	V_{EE} = -3.0V	3.6	3.8	4.0	V
V_{EE} Fault Threshold	V_{ETH}	V_{CC} = 5.0V	-2.3	-2.1	-1.9	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, R_{MR} = 22Ω, L_{MR} = 80nH.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}		8		15	mA
MR Head Current Tolerance	I_{MR}	8 < I_{MR} < 15 mA	-5		+5	%
Unselected MR Head Current					100	µA
MR Bias Reference Voltage	V_{RC}	2667 < R_{RC} < 4000 Ω	1.9	2.0	2.1	V
IRC to MR Bias Current Gain	A_{IMR}	2667 < R_{RC} < 4000 Ω		20		mA/mA
Differential Voltage Gain	A_V	V_{IN} = 2mV_{pp} @ 5 MHz, R_L(RDP, RDN) = 10kΩ	117	165	213	V/V
		Fast Mode	85	157	229	
Passband Upper Frequency Limit	f_{HR}	-1dB, Dependent on C2 parasitics	50	55		MHz
		Fast Mode	50	55		
		-3dB, Dependent on C2 parasitics	90	95		
		Fast Mode	80	85		
Passband Lower -3dB Frequency Limit	f_{LR}		0.1		0.8	MHz
Equivalent Input Noise	e_n	5 < f < 20 MHz		0.60	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}			16	20	pF
		Fast Mode		20	25	
Differential Input Resistance	R_{IN}		1200	2100		W
		Fast Mode	600	1000		
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 2mV_{pp} @ f = 5 MHz	8	20		mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, f=10MHz	45	60		dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, f=10MHz	40	45		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, f=10MHz	45	50		dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.7	V_{CC} - 3.2	V_{CC} - 2.7	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)	-250	50	250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		30	50	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	-1.5		+1.5	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 13mA, R_{MR} = 22Ω, L_{MR} = 80nH.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK}=10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK}=300pF, R_{DISK}=10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}		-350		350	mV
Buffered Head Voltage Error	BHV	(I_{MR} • R_{MR}) - BHV	-10		+10	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 25Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}		1.9	2.0	2.1	V
I_{WC} to Write Current Gain	A_I			20		mA/mA
Write Current Range	I_W		20		40	mA
Write Current Tolerance	ΔI_W	20 < I_W < 40 mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open Head, I_W = 40mA, V_{CC} = 4.5V, V_{EE} = -2.7V	7.0	8.0		V_{pp}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	(with internal damping resistor)	560	700	840	Ω
Open Head Detect Frequency	f_{OHD}	Open Head		[1]	17	MHz
Open Head Detect Resistance	R_{OHD}	I_W = 40mA, V_{CC} = 4.6V		[2]	26	W
Write Data Freq. for Safe Condition	f_{DATA}	FLT low, < 5kΩ pullup	1.4			MHz

1. Open Head Detection is guaranteed up to a frequency of 17MHz and typically operates to 20MHz.
2. Open Head Detection is guaranteed up to a head resistance of 26Ω and typically operates to 35Ω.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 25Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		0.1	0.15	µs
Write to Read Mode	t_{WR}	To 90% of envelope and ±20mV of steady-state offset		1.4	2.0	µs
Idle to Read Mode	t_{CS}	To 90% of envelope and ±20mV of steady-state offset		13	20	µs
HS0-3 to Any Head	t_{HS}	To 90% of envelope and ±20mV of steady-state offset		3	5	µs
Read to Idle	t_{RI}	To 10% of read envelope or write current		0.1	0.5	µs
Safe to Unsafe[1]	t_{D1}	50% WDX to 50% FLT, < 5kΩ pullup		0.7	1.5	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 30mA, L_H = 220nH, R_H = 25Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT, < 5kΩ pullup		0.1	0.3	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points		12	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0		0.05	0.1	ns
Rise/Fall Time	t_r / t_f	20-80%		2.5	3.0	ns
		10-90%		3.5	4.0	

1. See Figures 65 and 66 for write mode timing diagrams

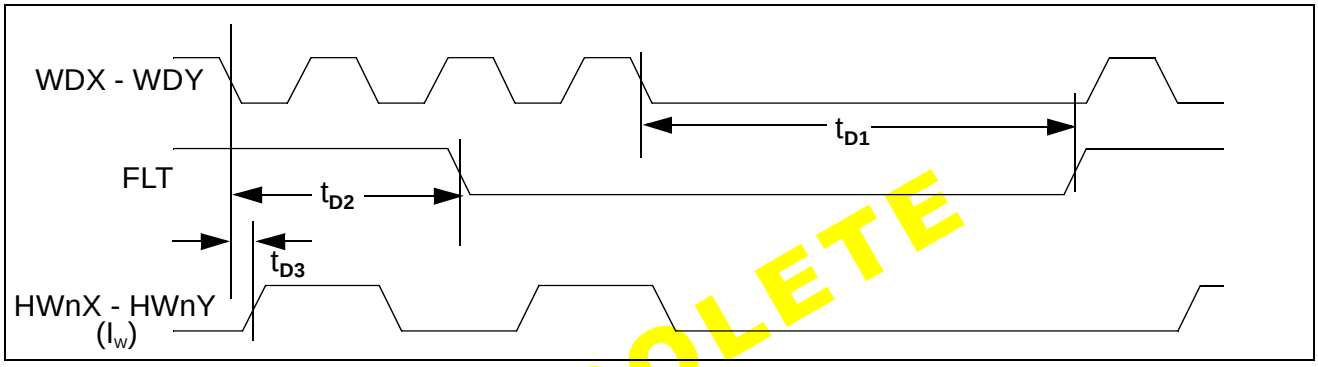


Figure 65 Write Mode Timing Diagram (with flip-flop active)

Note: The write current polarity is toggled on each high to low transition of the expression (WDX - WDY).
A preceding read operation initializes the WDFF so that upon entering the write mode, current flows into the “X” port.

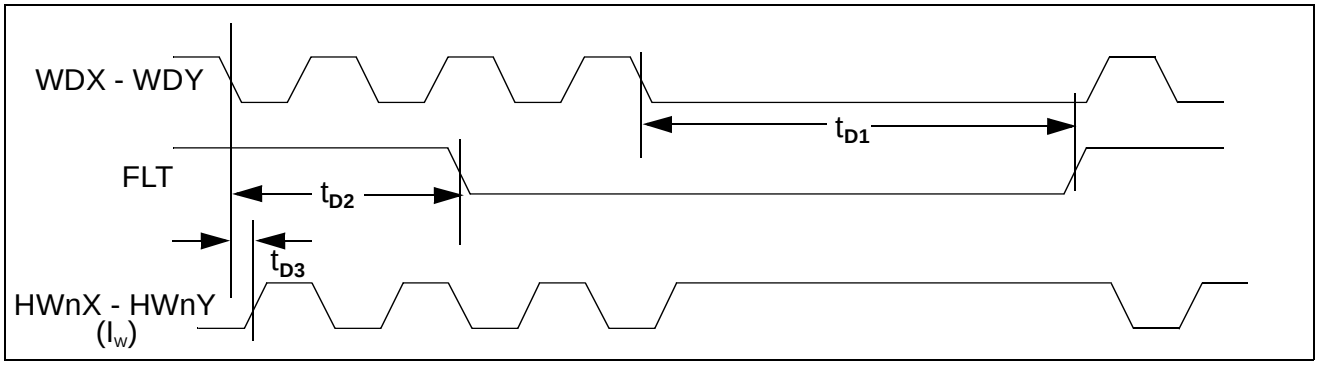
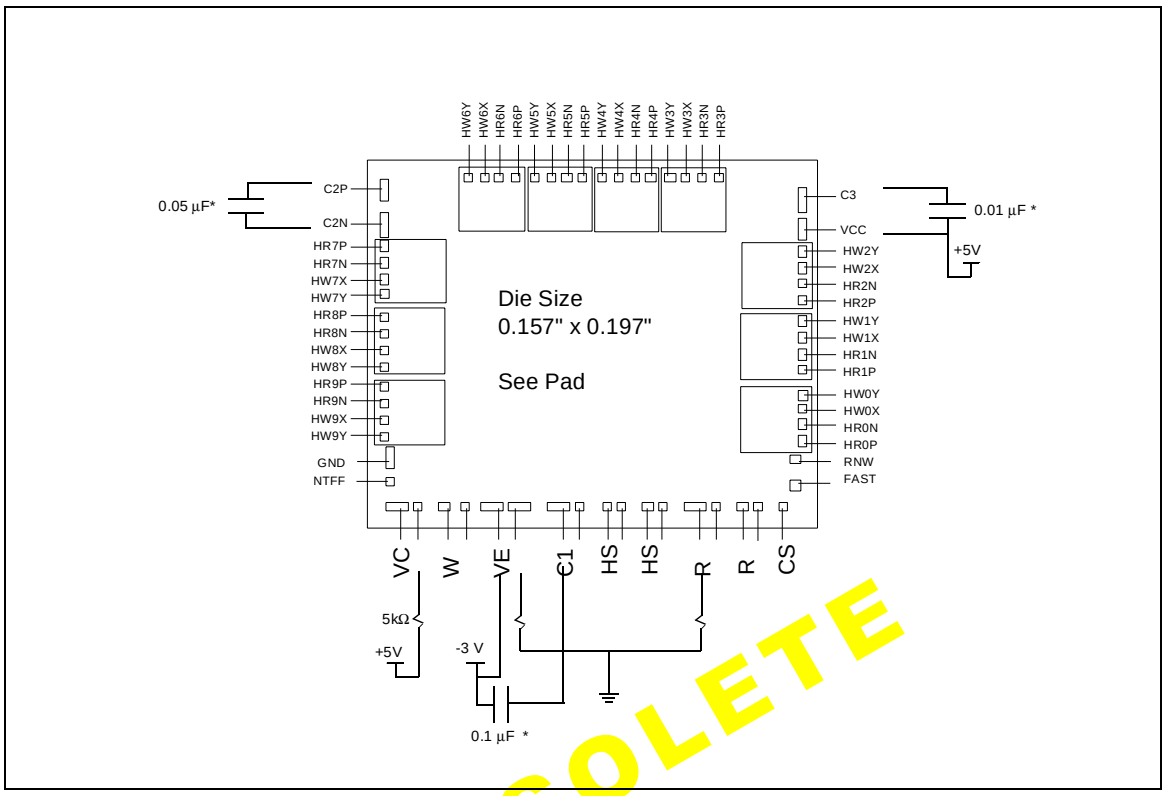


Figure 66 Write Mode Timing Diagram (without flip-flop)

Note: Without the flip-flop, the write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY).
For WDX>WDY current flows into the “X” port; for WDX<WDY current flows into the “Y” port.

TYPICAL APPLICATION CONNECTIONS



Application Notes

- V_{CC} = +5V, GND = Ground, V_{EE} = -3V
- Both VCC pads are electrically-connected on the die, but external connection is preferred for noise immunity.

* Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

VM61210S PAD COORDINATES

Pad Name	X Axis	Y Axis
HR0P	2357.5	-1019.25
HR0N	2357.5	- 839.25
HW0X	2357.5	- 659.25
HW0Y	2357.5	- 479.25
HR1P	2357.5	- 254.25
HR1N	2357.5	- 74.25
HW1X	2357.5	105.75
HW1Y	2357.5	285.75
HR2P	2357.5	510.75
HR2N	2357.5	690.75
HW2X	2357.5	870.75
HW2Y	2357.5	1050.75
HR3P	1417.0	1852.75
HR3N	1237.0	1852.75
HW3X	1057.0	1852.75
HW3Y	877.0	1852.75
HR4P	652.0	1852.75
HR4N	472.0	1852.75
HW4X	292.0	1852.75
HW4Y	112.0	1852.75
HR5P	- 112.0	1852.75
HR5N	- 292.0	1852.75
HW5X	- 472.0	1852.75
HW5Y	- 652.0	1852.75
HR6P	- 877.0	1852.75
HR6N	-1057.0	1852.75
HW6X	-1237.0	1852.75
HW6Y	-1417.0	1852.75
HR7P	-2357.5	1100.75
HR7N	-2357.5	920.75
HW7X	-2357.5	740.75
HW7Y	-2357.5	560.75
HR8P	-2357.5	335.75
HR8N	-2357.5	155.75
HW8X	-2357.5	- 24.25
HW8Y	-2357.5	- 204.25
HR9P	-2357.5	- 429.25
HR9N	-2357.5	- 609.25
HW9X	-2357.5	- 789.25
HW9Y	-2357.5	- 969.25
GND	-2288.0	-1210.25
NTFF	-2288.5	-1451.25
VCC	-2213.5	-1727.75
FLT	-1972.5	-1727.75
WDX	-1617.0	-1727.75
WDY	-1437.0	-1727.75

Pad Name	X Axis	Y Axis
GND	-1143.5	-1727.75
WC	- 827.0	-1727.75
C1	- 381.0	-1727.75
BHV	- 140.0	-1727.75
HS3	156.5	-1727.75
HS2	322.5	-1727.75
HS1	619.0	-1727.75
HS0	785.0	-1727.75
RC	1156.5	-1727.75
WSERN	1397.5	-1727.75
RDP	1694.0	-1727.75
RDN	1860.0	-1727.75
CSN	2156.0	-1727.75
FAST	2288.5	-1511.75
RNW	2288.5	-1215.25
C3	2357.5	1607.75
VCC	2357.5	1291.75
C2P	-2357.5	1707.75
C2N	-2357.5	1341.75

OBSOLETE

VTC Inc.
Value The Customer™

VM6130 Series

MAGNETO-RESISTIVE HEAD, HIGH PERFORMANCE, READ/WRITE PREAMPLIFIER

990812 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - Operates from +5V and -4.5V Power Supplies
  - Power Supply Fault Protection
  - Disk Voltage Monitor
  - Head-to-Disk Contact Monitor
  - Reduced Mode and Head Selection Delays in FAST Mode
  - Low Idle Power = 100 mW Typical
  - 12 or 14 Channels Available
- *High Performance Reader*
  - Current Bias / Current Sense Configuration
  - MR Bias Current Range 8 - 16 mA
  - Read Voltage Gain = 350 V/V Typical
  - Input Noise = 0.8 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 10 pF Typical
  - Head Inductance Range = 0.1 - 0.4 µH
- *High Speed Writer*
  - Write Current Range = 20 - 40 mA
  - Rise Time = 3 ns Typical (L_H = 220 nH, R_H = 40Ω, I_W = 20 mA)
  - Differential PECL Write Data Inputs
  - Write Unsafe Detection
  - Mask-Selectable Write Damping Resistor

DESCRIPTION

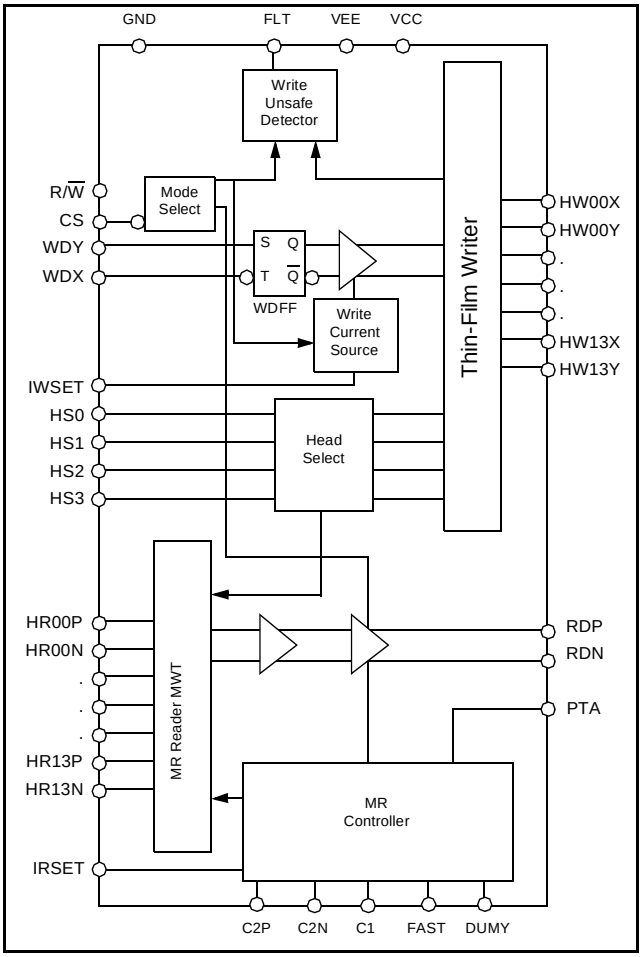
The VM6130 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6130 contains a thin-film head writer, an MR reader and associated fault circuitry. It provides bias current and control loops for setting the DC voltages on the MR element.

Fault protection circuitry ensures that the write current generator is disabled during power sequencing, voltage faults or an invalid head select. This protects the disk from potential data loss. For added data protection, internal pull-up resistors are connected to the mode select lines ($\overline{CS}$ and R/$\overline{W}$) to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM6130 operates from +5V, -4.5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6130 is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- V_{CC} ..... -0.3V to + 7V
- V_{EE} ..... -7V to +0.3V

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (VCC+ 0.3V)

Storage Temperature T_{stg} ..... -65° to 150°C

Junction Temperature T_J ..... 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{EE} ..... -4.5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

Head Voltage Control

In all modes of operation, the VM6130 controls the common mode potential of all MR elements. This is necessary because the MR element cannot be insulated, so that a small voltage differential will cause arcing to the disk and damage the heads.

Head voltages are held within ± 400 mV of the voltage on the VD pin, which monitors the disk potential of the drive. Thus, the disk may be grounded, as is done in disk drives having conventional thin film or ferrite recording heads, or isolated as the application may require.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

The appropriate TTL levels on the $\overline{CS}$ and R/$\overline{W}$ lines place the preamp in the read mode (see Table 96) and activate the bias generator, the read preamp and the read fault detection circuitry.

The VM6130 uses the current-bias/current-sensing MR architecture. An internally-generated 2.5 volt reference is present at the IRSET pin.The magnitude of the MR bias current is determined by an external resistor (connected between the IRSET pin and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{50}{(R_{RSET})} \qquad \textit{(eq. 49)}$$

I_{MR} represents the bias current flowing to the MR element.
R_{RSET} represents the equivalent resistance between the IRSET pin and ground.

RDP and RDN outputs are emitter follower and are in phase with the HRnP and HRnN head ports. These outputs should be AC-coupled to the load.

The output common mode voltage is maintained in the write mode, thereby substantially reducing the write-to-read recovery delay in the subsequent pulse detection circuitry.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
- Head to disk contact
  (the thermal asperity in the MR element will result in an abnormally high readback signal)

Fast Mode

Fast mode is utilized during head-to-head and idle-to-read transitions. When the FAST mode pin is high, the unity-gain frequency of the offset control loop is increased such that it is inside the passband of the reader, allowing the delay to be reduced to less than 5µs.

Note: This pin must be brought low before read data is valid.

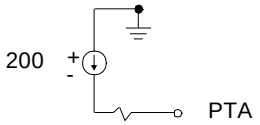
Programmable Thermal Asperity

The programmable thermal asperity pin (PTA), when left open, enables the TA circuitry with a nominal threshold of 3.25Vpp (referred to the input). This TA threshold may be changed and is governed by the following equation:

$$V_{TA} = 3.25\text{mVpp} - (16500 \times I_{PTA}) \qquad \textit{(eq. 50)}$$

V_{TA} represents the Thermal Asperity threshold.
I_{PTA} represents the current sunk from pin PTA in Amperes.

The Thévenin equivalent of pin PTA (in read mode) is 2.2kΩ @ 200mV below ground. See the diagram below:



Note: To disable the Programmable Thermal Asperity function, pin PTA should be connected directly to ground (GND).

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.
(Note that MR bias current is maintained in order to minimize the write-to-read delay.)

The appropriate TTL levels on the $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines place the preamp in the write mode (see Table 96) and activates the write unsafe detect circuitry.

The magnitude of the write current is determined by an external resistor (connected between the IWSET pin and ground). An internally-generated 2.5 volt reference is present at the IWSET pin. The following three equations govern the write current magnitude:

If $I_W \cdot R_H < 450\text{mV}$:

$$I_W = \frac{49.2}{(R_{WSET})\left(1 + \frac{R_H}{R_D}\right)} \qquad \textit{(eq. 51)}$$

If $450\text{mV} < I_W \cdot R_H < 615\text{mV}$:

$$I_W = \frac{(49.2/R_{WSET}) + 3\text{mA}}{1 + (0.008 \cdot R_H)} \qquad \textit{(eq. 52)}$$

If $I_W \cdot R_H > 615\text{mV}$:

$$I_W = \frac{(49.2/R_{WSET}) + 4\text{mA}}{1 + (0.008 \cdot R_H)} \qquad \textit{(eq. 53)}$$

I_W represents the write current flowing to the selected head.
R_{WSET} represents the equivalent resistance between the IWSET pin and ground.
R_H represents the series head resistance.
R_D represents an internal damping resistance of 692 Ω.

The polarity of the current is initially into the HWnY port following a read-to-write transition. Write current polarity is reversed on low-to-high transitions of the write data input (WDX low-to-high).

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
  (The writer is independent of VEE, so VEE faults do not generate a fault condition.)
- No write current
- Open write head
- Insufficient write data transition frequency
  (>2.5µs between transitions)
- Head short to ground

Two positive transitions of write data may be required to clear the fault after the safe condition is restored.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Idle Mode

In idle mode, the MR bias and write current sources are deactivated, and the device enters a low-power mode in which power dissipation is less than 100 mW. Write and read fault detection circuitry is disabled. MR common mode and offset control loops still receive power in order to reduce idle-to-read mode recovery.

Dummy Head

A TTL high level on the DUMY pin selects a dummy head in read or write mode. MR bias current is routed to an internal resistor, and the write current source is disabled to protect recorded data.

This mode is optionally used during power-up/down and following head-to-disk contacts.

An internal pull-up resistor ensures that the dummy head is selected in event of an accidental open.

Note: If this pin is not used it should be grounded for normal operation.

Table 96 Mode Select Logic

R/*W*	*CS*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 97 Head Select Logic

HS3	*HS2*	*HS1*	*HS0*	*DUMY*	*HEAD*
X	X	X	X	1	dummy
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	2
0	0	1	1	0	3
0	1	0	0	0	4
0	1	0	1	0	5
0	1	1	0	0	6
0	1	1	1	0	7
1	0	0	0	0	8
1	0	0	1	0	9
1	0	1	0	0	10
1	0	1	1	0	11
1	1	0	0	0	12
1	1	0	1	0	13
1	1	1	X	0	0

Note: Invalid head select codes disable the writer and select head MR0.

PIN_FUNCTION LIST AND DESCRIPTION

29) $\overline{CS}$ (I) Chip Select:
A TTL low level enables the device.
Pin defaults high (disabled).

30) R/$\overline{W}$ I [1] Read/Write:
A TTL low level enables write mode.
Pin defaults high (read).

31) HS0-HS3 (I [1]) Head Select:
Selects one of fourteen heads. Pins default low (head 0).

32) DUMY (I [1]) Dummy Head:
A TTL high level enables the dummy head. Pin defaults high (dummy head selected).

33) FAST (I [1]) Fast Recovery in Read Mode:
A TTL high level enables fast settling of the reader.

34) FLT (O [1]) Write/Read Fault:
A TTL high level indicates a fault in write mode.
A TTL low level indicates a fault in read mode.

35) WDX, WDY (I [1]) Differential Pseudo-ECL write data inputs:
A positive edge on WDX toggles the direction of the head current.

36) HR00P-HR13P (I) MR head connections, positive end.

37) HR00N-HR13N (I) MR head connections, negative end.

38) HW00X-HW13X (O) Write head connections, positive end.

39) HW00Y-HW13Y (O) Write head connections, negative end.

40) RDP, RDN (O [1]) Read Data:
Differential read signal outputs.

41) IWSET ([1]) Write current pin:
Set the magnitude of write current.

42) IRSET ([1]) MR bias reference pin:
Sets the magnitude of MR bias current.

43) C2P,C2N ([1]) Compensation capacitor for the MR head current loop.

44) C1 ([1]) Noise bypass capacitor for the MR bias current generator.

45) VD (I [1]) Disk Voltage.
Analog reference for the disk bias.

46) PTA (I) Programmable Thermal Asperity input.

47) VEE - -4.5V supply

48) VCC - +5V supply

49) GND - Ground

I = Input pin
O = Output pin

[1] When more than one device is used, these signals can be wire OR'ed together

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 12mA		70	95	mA
		Write Mode, I_W = 30mA, I_{MR} = 12mA		125	145	mA
		Idle Mode		13	16	mA
V_{EE} Power Supply Current	I_{EE}	Read Mode, I_{MR} = 12mA		45	70	mA
		Write Mode, I_W = 30mA, I_{MR} = 12mA		100	125	mA
		Idle Mode		7	10	mA
Power Supply Dissipation	P_d	Read Mode, I_{MR} = 12mA		552	873	mW
		Write Mode, I_W = 30mA, I_{MR} = 12mA		1075	1420	mW
		Idle Mode		100	140	mW
Input High Voltage	V_{IH}	PECL	3.87		4.27	V
		CMOS	3.5			V
Input Low Voltage	V_{IL}	PECL	3.05		3.55	V
		CMOS			1.5	V
Disk Reference Voltage Range	V_D		-250		250	mV
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{CC} Fault Threshold	V_{CTH}		3.65		4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75		-3.15	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		8		16	mA
MR Head Current Tolerance	I_{MR}	$8 < I_{MR} < 16$ mA	-5		+5	%
MR Bias Reference Voltage	V_{RSET}	$2775 < R_{RSET} < 6250\Omega$		2.5		V
IRSET to MR Bias Current Gain	A_{IMR}	$2775 < R_{RSET} < 6250\Omega$		20		mA/mA
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, R_L (RDP, RDN) = 1kΩ, I_{MR} = 12mA, R_{MR} = 28Ω	260	350	440	V/V
Passband Upper Frequency Limit	f_{HR}	-1dB: R_{MR} = 28Ω; L_{MR} = 20nH		50		MHz
		-3dB: R_{MR} = 28Ω; L_{MR} = 20nH	60	80		
Passband Lower -3dB Frequency Limit	f_{LR}	R_{MR} = 28Ω C_2 = 6nF	0.1		0.5	MHz
Equivalent Input Noise	e_n	I_{MR} = 12mA; 1 < f < 80 MHz R_{MR} = 28Ω		.8		nV/√Hz
Differential Input Capacitance	C_{IN}	I_{MR} = 12mA			10	pF
Differential Input Resistance	R_{IN}	I_{MR} = 12mA			4	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 10 MHz	4			mV_{pp}
Power Supply Rejection Ratio	PSRR	100mVp-p on V_{CC} or V_{EE}, I_{MR} = 12mA, 1 < f < 50 MHz, R_{MR} = 28Ω	30			dB
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p	30			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mVp-p, 1 < f < 50 MHz	30			dB
Output Offset Voltage	V_{OS}	I_{MR} = 12mA, R_{MR} = 28Ω			100	mV
Common Mode Output Voltage	V_{OCM}		V_{CC} - 2.8	V_{CC} -2.1	V_{CC}-1.8	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)	- 250		250	mV
Single-Ended Output Resistance	R_{SEO}	(Includes 21Ω series resistor with RDP/RDN)			59	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	±1.5			mA
Total Harmonic Distortion	THD	V_{in} = 4mV_{pp}; ten harmonics			0.5	%
MR Head-to-Disk Contact Current	I_{DISK}	Extended contact, R_{DISK} = 10MΩ			100	µA
		Maximum peak discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			20	mA
MR Head Potential	V_{MR}	I_{MR} = 12mA, R_{MR} = 28Ω	V_D - 400		V_D + 400	mV

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Asperity Detect Threshold	V_{PTA}	R_{MR} = 28Ω, I_{PTA} = 0	2.44	3.25	4.06	mV_{pp}
		R_{MR} = 28Ω, V_{PTA} = 3.25 - (16500 · I_{PTA})	.75 · V_{PTA}	V_{PTA}	1.25 · V_{PTA}	

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
I_W = 30mA, L_H = 200nH, R_H = 15Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
I_{WSET} Pin Voltage	V_{WSET}			2.5		V
I_{WSET} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WSET} * A_I$	46	50	54	V
Write Current Range	I_W		20		40	mA
Write Current Tolerance	ΔI_W	20 < I_W < 40 mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head	5	6		V_{pp}
Unselected Head Transition Current	I_{UH}	I_W = 30mA			50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal damping resistance	560	692	840	Ω
Time Between Write Data Transitions for Safe Condition	t_{SAFE}	FLT = Low			2.5	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
I_W = 30mA, L_H = 200nH, R_H = 30Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.5	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope			1	µs
$\overline{CS}$ to Read Mode	t_{CS}	To 90% of envelope; FAST = low			50	µs
		FAST = high for 3.5µs [1]			15	µs
$\overline{CS}$ to Write Mode	t_{CS}	To 90% of write current			0.5	µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope; FAST = low			50	µs
		FAST = high for 3.5µs [1]			5	µs
DUMY Mode to Any Head	t_{DH}	To 90% of envelope; FAST = low			50	µs
		FAST = high for 3.5µs [1]			5	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe [2]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [2]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [2]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H = 0, R_H = 0			0.2	ns
Rise/Fall Time	t_r / t_f	20-80%; I_W = 20mA; L_H = 220nH, R_H = 40Ω		3	4	ns
		L_H = 0, R_H = 0; I_W = 30mA			1.5	ns
Settling Time	T_{WSET}	I_{WC} = 30mA, L_H = 200nH, R_H = 15Ω; to ±10%			5	ns
Overshoot	W_{COV}	I_{WC} = 30mA; L_H = 200nH, R_H = 15Ω		10		%

1. See Figure 2 for read mode timing diagram.
2. See Figure 1 for write mode timing diagram.

†

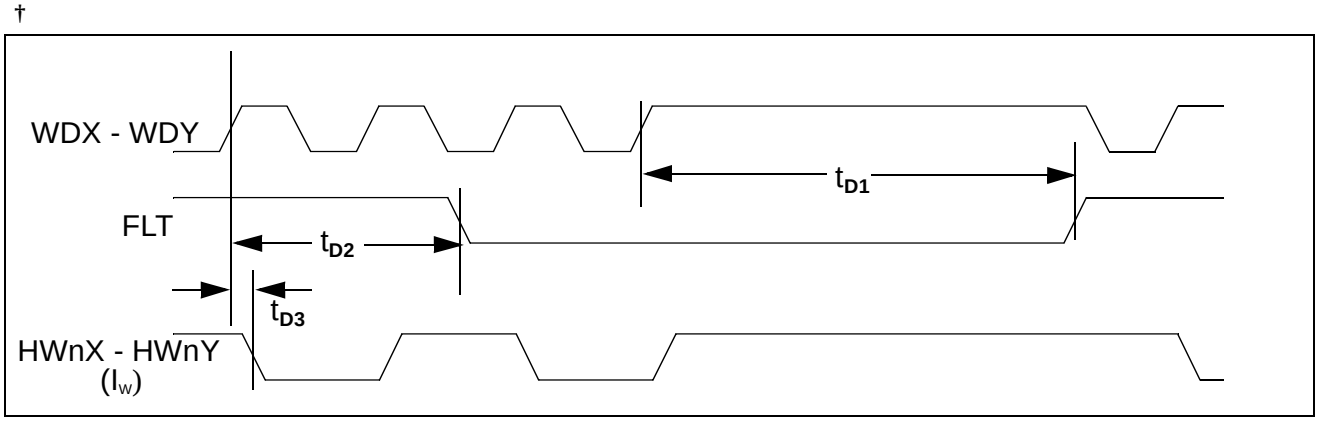


Figure 67 Write Mode Timing Diagram

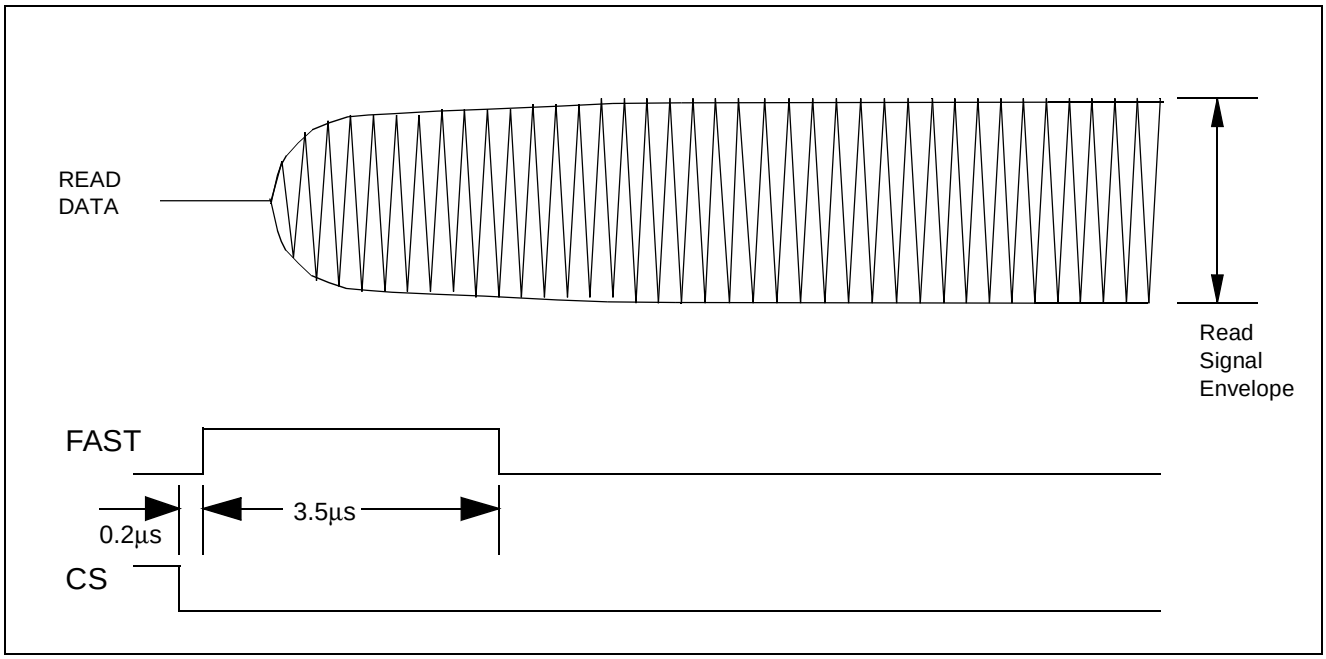
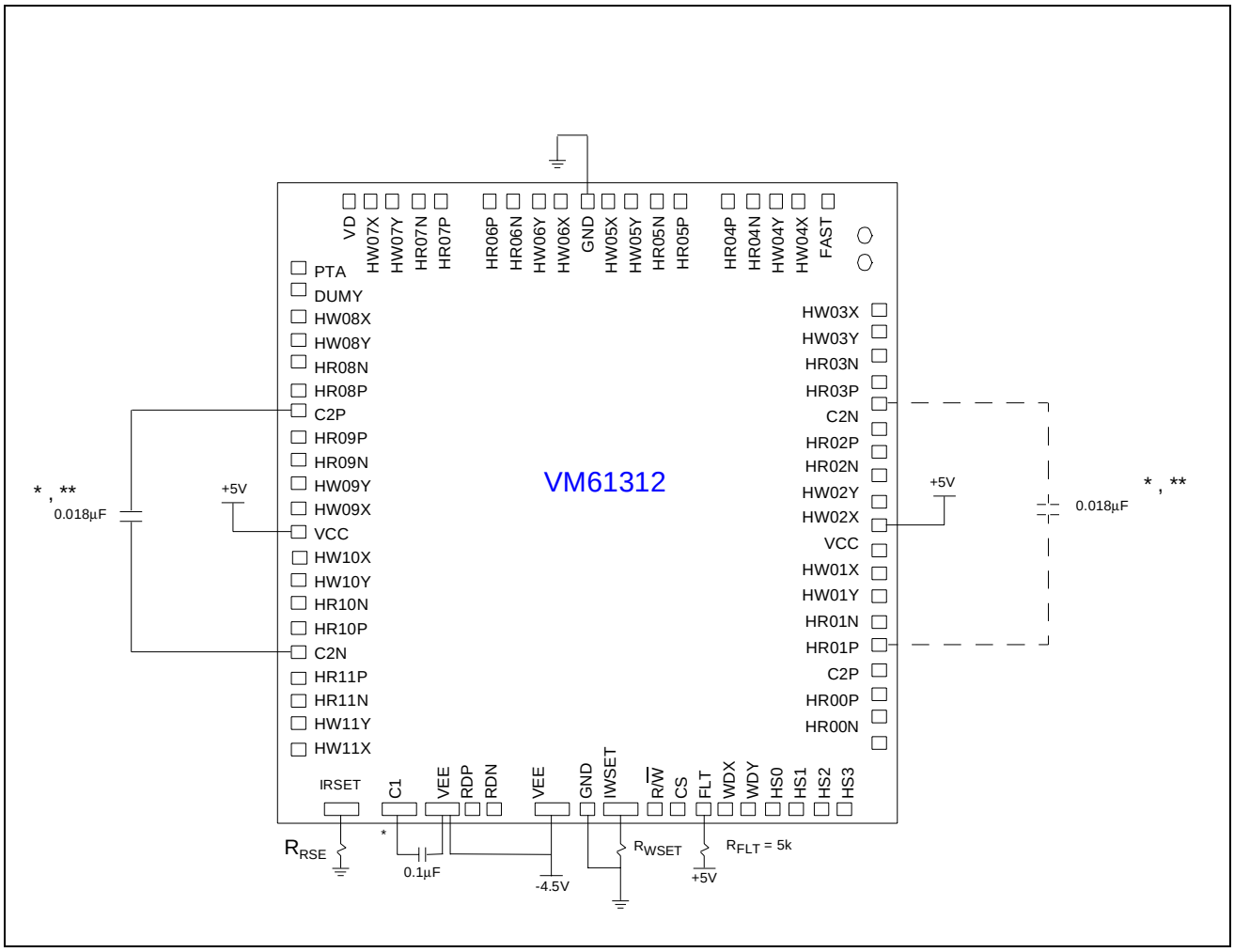


Figure 68 Read Mode Timing Diagram. Also applies to DUMY and HS0 - HS3.

TYPICAL APPLICATION CONNECTIONS



Application Notes

- I_{MR} = MR Bias Current = $50/R_{RSET}$
- I_W = Write Current = $50/R_{WSET}(1+R_H/700)$, R_H = Head Series Resistance
- V_{CC} = +5V, GND = Ground, V_{EE} = -4.5V
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND

* Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

** VTC recommends using only one of the two sets of C2P/C2N pads included on the VM6130 die (and not externally connecting the two sets). The C2 capacitor sets the lower corner frequency of the preamplifier's bandpass filter.

VM61312

12-CHANNEL DIE

Specific Characteristics

Die size: 172 X 181 Mils

VM61312 Pad Coordinates (in Mils)

Pad Name	X Axis	Y Axis	Pad Size
C1	-53.484	-85.502	4x10
C2N	-81.230	-42.874	4x4
C2N:	81.230	27.992	4x4
C2P	-81.230	27.992	4x4
C2P:	81.230	-42.874	4x4
CSN	25.059	-85.502	4x4
DSBF	-81.230	71.457	4x4
DUMY	-81.230	64.793	4x4
FAST	72.323	85.512	4x4
FLT	32.146	-85.502	4x4
HS0	53.406	-85.502	4x4
HS1	60.492	-85.502	4x4
HS2	67.579	-85.502	4x4
HS3	74.665	-85.502	4x4
IRSET	-74.744	-85.502	4x10
IWSET	7.933	-85.502	4x10
HR00N	81.230	-57.047	4x4
HR01N	81.230	-28.701	4x4
HR02N	81.230	13.819	4x4
HR03N	81.230	42.165	4x4
HR04N	49.606	85.512	4x4
HR05N	21.260	85.512	4x4
HR06N	-21.260	85.512	4x4
HR07N	-49.606	85.512	4x4
HR08N	-81.230	42.165	4x4
HR09N	-81.230	13.819	4x4
HR10N	-81.230	-28.701	4x4
HR11N	-81.230	-57.047	4x4
HR00P	81.230	-49.961	4x4
HR01P	81.230	-35.787	4x4
HR02P	81.230	20.906	4x4
HR03P	81.230	35.079	4x4
HR04P	42.520	85.512	4x4
HR05P	28.346	85.512	4x4
HR06P	-28.346	85.512	4x4
HR07P	-42.520	85.512	4x4
HR08P	-81.230	35.079	4x4
HR09P	-81.230	20.906	4x4
HR10P	-81.230	-35.787	4x4
HR11P	-81.230	-49.961	4x4
RDN	-22.697	-85.502	4x4
RDP	-29.272	-85.502	4x4
RNW	17.972	-85.502	4x4
VCC:	-2.106	-85.502	4x4
VCC:	81.230	73.661	4x4 oct
VCC:P	0.000	85.512	4x4
VD	-71.654	85.512	4x4
VDD:	81.230	-7.441	4x4
VDD:	81.230	80.748	4x4 oct
VDD:P	-81.230	-7.441	4x4
VEE:	-40.492	-85.502	4x10
VEE:G	-12.146	-85.502	4x10
HW00Y	81.230	-64.134	4x4
HW01Y	81.230	-21.614	4x4
HW02Y	81.230	6.732	4x4
HW03Y	81.230	49.252	4x4
HW04Y	56.693	85.512	4x4
HW05Y	14.173	85.512	4x4
HW06Y	-14.173	85.512	4x4
HW07Y	-56.693	85.512	4x4
HW08Y	-81.230	49.252	4x4
HW09Y	-81.230	6.732	4x4
HW10Y	-81.230	-21.614	4x4
HW11Y	-81.230	-64.134	4x4
HW00X	81.230	-71.220	4x4
HW01X	81.230	-14.528	4x4
HW02X	81.230	-0.354	4x4
HW03X	81.230	56.339	4x4
HW04X	63.780	85.512	4x4
HW05X	7.087	85.512	4x4
HW06X	-7.087	85.512	4x4
HW07X	-63.780	85.512	4x4
HW08X	-81.230	56.339	4x4
HW09X	-81.230	-0.354	4x4
HW10X	-81.230	-14.528	4x4
HW11X	-81.230	-71.220	4x4
WDY	46.319	-85.502	4x4
WDX	39.232	-85.502	4x4

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1. Octagonal pins are for factory use only.

VM61312

12-CHANNEL DIE (MIRROR)

Specific Characteristics

Die size: 172 X 181 Mils

VM61312 Mirror Pad Coordinates (in Mils)

Pad Name	X Axis	Y Axis	Pad Size
C1	53.484	-85.502	4x10
C2N	81.230	-42.874	4x4
C2N:	-81.230	27.992	4x4
C2P	81.230	27.992	4x4
C2P:	-81.230	-42.874	4x4
CSN	-25.059	-85.502	4x4
DSBF	81.230	71.457	4x4
DUMY	81.230	64.793	4x4
FAST	-72.323	85.512	4x4
FLT	-32.146	-85.502	4x4
HS0	-53.406	-85.502	4x4
HS1	-60.492	-85.502	4x4
HS2	-67.579	-85.502	4x4
HS3	-74.665	-85.502	4x4
IRSET	74.744	-85.502	4x10
IWSET	-7.933	-85.502	4x10
HR00N	-81.230	-57.047	4x4
HR01N	-81.230	-28.701	4x4
HR02N	-81.230	13.819	4x4
HR03N	-81.230	42.165	4x4
HR04N	-49.606	85.512	4x4
HR05N	-21.260	85.512	4x4
HR06N	21.260	85.512	4x4
HR07N	49.606	85.512	4x4
HR08N	81.230	42.165	4x4
HR09N	81.230	13.819	4x4
HR10N	81.230	-28.701	4x4
HR11N	81.230	-57.047	4x4
HR00P	-81.230	-49.961	4x4
HR01P	-81.230	-35.787	4x4
HR02P	-81.230	20.906	4x4
HR03P	-81.230	35.079	4x4
HR04P	-42.520	85.512	4x4
HR05P	-28.346	85.512	4x4
HR06P	28.346	85.512	4x4
HR07P	42.520	85.512	4x4
HR08P	81.230	35.079	4x4
HR09P	81.230	20.906	4x4
HR10P	81.230	-35.787	4x4
HR11P	81.230	-49.961	4x4
RDN	22.697	-85.502	4x4
RDP	29.272	-85.502	4x4
RNW	-17.972	-85.502	4x4
VCC:	2.106	-85.502	4x4
VCC:	-81.230	73.661	4x4oct
VCC:P	0.000	85.512	4x4
VD	71.654	85.512	4x4
VDD:	-81.230	-7.441	4x4
VDD:	-81.230	80.748	4x4oct
VDD:P	81.230	-7.441	4x4
VEE:	40.492	-85.502	4x10
VEE:G	12.146	-85.502	4x10
HW00Y	-81.230	-64.134	4x4
HW01Y	-81.230	-21.614	4x4
HW02Y	-81.230	6.732	4x4
HW03Y	-81.230	49.252	4x4
HW04Y	-56.693	85.512	4x4
HW05Y	-14.173	85.512	4x4
HW06Y	14.173	85.512	4x4
HW07Y	56.693	85.512	4x4
HW08Y	81.230	49.252	4x4
HW09Y	81.230	6.732	4x4
HW10Y	81.230	-21.614	4x4
HW11Y	81.230	-64.134	4x4
HW00X	-81.230	-71.220	4x4
HW01X	-81.230	-14.528	4x4
HW02X	-81.230	-0.354	4x4
HW03X	-81.230	56.339	4x4
HW04X	-63.780	85.512	4x4
HW05X	-7.087	85.512	4x4
HW06X	7.087	85.512	4x4
HW07X	63.780	85.512	4x4
HW08X	81.230	56.339	4x4
HW09X	81.230	-0.354	4x4
HW10X	81.230	-14.528	4x4
HW11X	81.230	-71.220	4x4
WDY	-46.319	-85.502	4x4
WDX	-39.232	-85.502	4x

1. Octagonal pins are for factory use only.

VM61314

14-CHANNEL DIE

Specific Characteristics

Die size: 244 X 181 Mils

VM61314 Pad Coordinates (in Mils)

Pad Name	X Axis	Y Axis	Pad Size
VEE:	-60.463	-85.502	4x4
VCC:	-14.301	-85.502	4x4
VDD:P	-116.663	-7.441	4x4
C2N	-116.663	-42.874	4x4
C2P:	116.663	-42.874	4x4
VDD:	116.663	-7.441	4x4
C2P	-116.663	27.992	4x4
VCC:P	0.000	85.512	4x4
C2N:	116.663	27.992	4x4
VEE:G	-26.762	-85.502	4x10
HR10P	-116.663	35.079	4x4
HR10N	-116.663	42.165	4x4
HW10X	-116.663	56.339	4x4
HW10Y	-116.663	49.252	4x4
HR09P	-77.953	85.512	4x4
HR09N	-85.039	85.512	4x4
HW09X	-99.213	85.512	4x4
HW09Y	-92.126	85.512	4x4
HR03P	116.663	35.079	4x4
HR03N	116.663	42.165	4x4
HW03X	116.663	56.339	4x4
HW03Y	116.663	49.252	4x4
HR04P	77.953	85.512	4x4
HR04N	85.039	85.512	4x4
HW04X	99.213	85.512	4x4
HW04Y	92.126	85.512	4x4
VDD:	116.663	80.748	4x4oct
VCC:	116.663	73.661	4x4oct
HR05P	63.780	85.512	4x4
HR05N	56.693	85.512	4x4
HW05X	42.520	85.512	4x4
HW05Y	49.606	85.512	4x4
HR08P	-63.780	85.512	4x4
HR08N	-56.693	85.512	4x4
HW08X	-42.520	85.512	4x4
HW08Y	-49.606	85.512	4x4
HR13P	-116.663	-49.961	4x4
HR13N	-116.663	-57.047	4x4
HW13X	-116.663	-71.220	4x4
HW13Y	-116.663	-64.134	4x4
HR12P	-116.663	-35.787	4x4
HR12N	-116.663	-28.701	4x4
HW12X	-116.663	-14.528	4x4
HW12Y	-116.663	-21.614	4x4
HR00P	116.663	-49.961	4x4
HR00N	116.663	-57.047	4x4
HW00X	116.663	-71.220	4x4
HW00Y	116.663	-64.134	4x4
HR01P	116.663	-35.787	4x4
HR01N	116.663	-28.701	4x4
HW01X	116.663	-14.528	4x4
HW01Y	116.663	-21.614	4x4
HR11P	-116.663	20.906	4x4
HR11N	-116.663	13.819	4x4
HW11X	-116.663	-0.354	4x4
HW11Y	-116.663	6.732	4x4
HR07P	-7.087	85.512	4x4
HR07N	-14.173	85.512	4x4
HW07X	-28.346	85.512	4x4
HW07Y	-21.260	85.512	4x4
HR02P	116.663	20.906	4x4
HR02N	116.663	13.819	4x4
HW02X	116.663	-0.354	4x4
HW02Y	116.663	6.732	4x4
HR06P	7.087	85.512	4x4
HR06N	14.173	85.512	4x4
HW06X	28.346	85.512	4x4
HW06Y	21.260	85.512	4x4
RDN	-38.888	-85.502	4x4
RDP	-51.053	-85.502	4x4
FLT	40.000	-85.502	4x4
CSN	28.346	-85.502	4x4
WDX	51.654	-85.502	4x4
WDY	63.307	-85.502	4x4
HS0	74.961	-85.502	4x4
HS1	86.614	-85.502	4x4
RNW	16.693	-85.502	4x4
HS2	98.268	-85.502	4x4

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Pad Name	*X Axis*	*Y Axis*	*Pad Size*
HS3	109.921	-85.502	4x4
DUMY	-116.663	63.701	4x4
FAST	108.386	85.512	4x4
DSBF	-116.663	71.447	4x4
IWSET	2.087	-85.502	4x10
IRSET	-90.896	-85.502	4x10
C1	-72.825	-85.502	4x10
VD	-107.087	85.512	4x4

VM61314

14-CHANNEL DIE (Mirror)

Specific Characteristics

Die size: 244 X 181 Mils

VM61314 Mirror Pad Coordinates (in Mils)

Pad Name	X Axis	Y Axis	Pad Size
VEE:	60.463	-85.502	4x4
VCC:	14.301	-85.502	4x4
VDD:P	116.663	-7.441	4x4
C2N	116.663	-42.874	4x4
C2P:	-116.663	-42.874	4x4
VDD:	-116.663	-7.441	4x4
C2P	116.663	27.992	4x4
VCC:P	0.000	85.512	4x4
C2N:	-116.663	27.992	4x4
VEE:G	26.762	-85.502	4x10
HR10P	116.663	35.079	4x4
HR10N	116.663	42.165	4x4
HW10X	116.663	56.339	4x4
HW10Y	116.663	49.252	4x4
HR09P	77.953	85.512	4x4
HR09N	85.039	85.512	4x4
HW09X	99.213	85.512	4x4
HW09Y	92.126	85.512	4x4
HR03P	-116.663	35.079	4x4
HR03N	-116.663	42.165	4x4
HW03X	-116.663	56.339	4x4
HW03Y	-116.663	49.252	4x4
HR04P	-77.953	85.512	4x4
HR04N	-85.039	85.512	4x4
HW04X	-99.213	85.512	4x4
HW04Y	-92.126	85.512	4x4
VDD:	-116.663	80.748	4x4oct
VCC:	-116.663	73.661	4x4oct
HR05P	-63.780	85.512	4x4
HR05N	-56.693	85.512	4x4
HW05X	-42.520	85.512	4x4
HW05Y	-49.606	85.512	4x4
HR08P	63.780	85.512	4x4
HR08N	56.693	85.512	4x4
HW08X	42.520	85.512	4x4
HW08Y	49.606	85.512	4x4
HR13P	116.663	-49.961	4x4
HR13N	116.663	-57.047	4x4
HW13X	116.663	-71.220	4x4
HW13Y	116.663	-64.134	4x4
HR12P	116.663	-35.787	4x4
HR12N	116.663	-28.701	4x4
HW12X	116.663	-14.528	4x4
HW12Y	116.663	-21.614	4x4
HR00P	-116.663	-49.961	4x4
HR00N	-116.663	-57.047	4x4
HW00X	-116.663	-71.220	4x4
HW00Y	-116.663	-64.134	4x4
HR01P	-116.663	-35.787	4x4
HR01N	-116.663	-28.701	4x4
HW01X	-116.663	-14.528	4x4
HW01Y	-116.663	-21.614	4x4
HR11P	116.663	20.906	4x4
HR11N	116.663	13.819	4x4
HW11X	116.663	-0.354	4x4
HW11Y	116.663	6.732	4x4
HR07P	7.087	85.512	4x4
HR07N	14.173	85.512	4x4
HW07X	28.346	85.512	4x4
HW07Y	21.260	85.512	4x4
HR02P	-116.663	20.906	4x4
HR02N	-116.663	13.819	4x4
HW02X	-116.663	-0.354	4x4
HW02Y	-116.663	6.732	4x4
HR06P	-7.087	85.512	4x4
HR06N	-14.173	85.512	4x4
HW06X	-28.346	85.512	4x4
HW06Y	-21.260	85.512	4x4
RDN	38.888	-85.502	4x4
RDP	51.053	-85.502	4x4
FLT	-40.000	-85.502	4x4
CSN	-28.346	-85.502	4x4
WDX	-51.654	-85.502	4x4
WDY	-63.307	-85.502	4x4
HS0	-74.961	-85.502	4x4
HS1	-86.614	-85.502	4x4
RNW	-16.693	-85.502	4x4
HS2	-98.268	-85.502	4x4

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Pad Name	*X Axis*	*Y Axis*	*Pad Size*
HS3	-109.921	-85.502	4x4
DUMY	116.663	63.701	4x4
FAST	-108.386	85.512	4x4
DSBF	116.663	71.447	4x4
IWSET	-2.087	-85.502	4x10
IRSET	90.896	-85.502	4x10
C1	72.825	-85.502	4x10
VD	107.087	85.512	4x4

VTC Inc.
Value The Customer™

VM6160 Series

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection and Servo Control)
  - Operates from +5 and -3 Volt Power Supplies
  - Up to 12-Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC, 5 - 15 mA Range
  - Read Voltage Gain = 220 V/V Typical
  - Input Noise = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 13 pF Typical
  - Head Inductance Range = 10 nH - 220 nH
  - Mask Select Resistors (0, 10, 15, 30 Ω) in series with RDP, RDN
- *High Speed Writer*
  - Write Current 4-bit DAC, 10 - 45 mA Range
  - Rise Time = 1.3 ns Typical
    (20 - 80%, L_{total} = 220 nH, I_W = 25 mA)
  - Multi-Channel Servo Write
  - Optional Write Data Flip-Flop (WDFF)

DESCRIPTION

The VM6160 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6160 contains a thin-film head writer, an MR reader, and associated fault circuitry. It provides bias current and control loops for setting the DC voltages on the MR element.

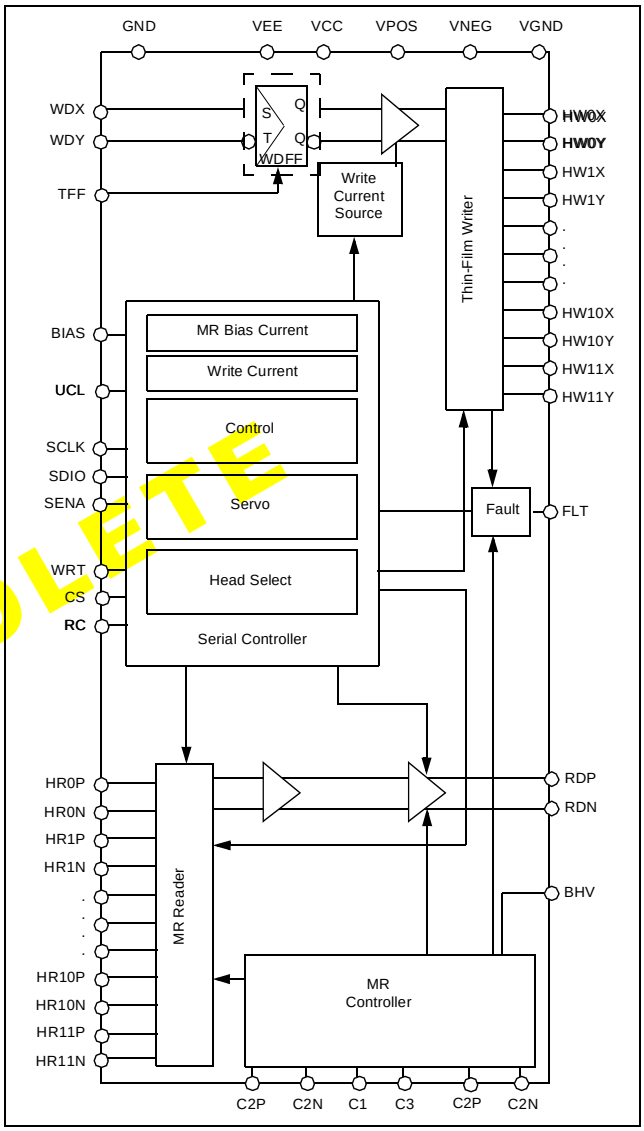
Programmability of the VM6160 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection and servo operation.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, internal pull-up resistors are connected to the mode select lines ($\overline{CS}$ and $\overline{WRT}$) to prevent accidental writing due to open lines.

The VM6160 operates from +5V, -3V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6160 is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



See page 254 for the Pin Function List and Description.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -5V
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 30mA
Write Current, I_W 60mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J 150°C
Storage Temperature, T_{stg} -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -3V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 10 - 45 mA
Write Head Inductance, L_W ..... 10 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 5 - 20 mA
Read Head Inductance, L_{MR} ..... 10 - 100 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J ..... 0°C to 125°C

SERIAL INTERFACE CONTROLLER

The VM6160 uses a VTC proprietary 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 99 and 100 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, three preamp select bits <A3-A1> (which must be <001> for this preamp), and four register address bits <A7-A4>. The second 8 bits <D7-D0> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the 16th rising edge, the data will be written to the addressed register. During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed one cycle to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.

See Table 106 and Figures 70 and 71 for serial interface timing information.

Preamplifier Configuration and Selection

The VM6160 was designed for a single or dual preamp configuration. All control lines may be shared (including the three serial lines SCLK, SENA and SDIO).

Pin UCL determines the preamplifier's upper/lower status in a dual preamp configuration. Pin UCL floats high if left open, and the preamp assumes the "lower preamp" designation. If pin UCL is tied to ground, the preamp will assume the "upper preamp" designation.

In either a single or dual preamp configuration, pin UCL (Upper Chip Low) is exclusively OR'ed with control bit CE (Chip Enable; register 0, bit <D4>*) to determine which preamp is selected.

* Bit <D3> in the 6-channel version.

- UCL ⊕ <CE> = 1, chip selected
- UCL ⊕ <CE> = 0, chip unselected

See Table 101 for Mode Control information.

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the serial registers (the contents of which remain latched).

Idle mode may be entered with $\overline{CS}$, the IDLEOVR bit (register 4, bit <D1>), or a UCL/<CE>/<PWREN> combination. Idle override (IDLEOVR) forces idle mode from any other mode.

If UCL ⊕ <CE> = 0 and <PWREN> = 0, the chip is unselected and enters idle mode. If UCL ⊕ <CE> = 0 and <PWREN> = 1, the chip is unselected and enters read standby mode (see below).

Read Standby Mode

In the read standby mode, MR bias circuitry is active and an internal dummy head is selected (regardless of head selection). In addition, the read amplifier differential outputs RDP/RDN are high impedance (tri-stated).

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6160 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external resistor (connected between pin RC and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{20}{(R_{ext})} + k_{IMR}\left(\frac{1.29}{R_{ext}}\right) \qquad \textit{(eq. 54)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{ext} represents the equivalent resistance between the RC pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

With the use of a negative supply, the MR head center voltage is near ground potential minimizing current spikes during disk contact.

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BHVOE (Buffered Head Voltage Output Enabled)

This control bit (register 4, bit <D5>) enables the output of the $(I_{MR} \times R_{MR}) \times 4$ product of the selected head at the BHV pin. This output is single-ended with respect to ground. When BHVOE is reset, the output pin BHV enters a high-impedance state to minimize noise coupling.

Fast Read Mode

This control bit (register 4, bit <D0>), when enabled, increases the gm (tail current) of the first stage of the read amplifier by a factor of approximately 3. This effectively increases the lower corner frequency of the amplifier's bandpass by a factor of approximately 2. This lower corner frequency can be calculated using the following equation:

$$f_{LF} = \frac{1}{2\pi r_e C2_{total}} \qquad \textit{(eq. 55)}$$

f_{LF} represents the lower -3dB corner frequency of the bandpass.
r_e represents the emitter resistance of the input stage (12Ω).
$C2_{total}$ represents total capacitance between C2N and C2P (.024µF typical).

MR Bias DAC

The 5 bits in register 3 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage**
- Device in write mode

** Note that a power supply fault will reset the serial register to "power-on" values.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external resistor (connected between pin RC and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{40}{R_{ext}} + k_{IW}\left(\frac{8}{R_{ext}}\right)\right]\frac{1}{1+\frac{R_H}{R_D}} \qquad \textit{(eq. 56)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{ext} represents the equivalent resistance between the RC pin and ground (in kΩ).
R_H represents the series head resistance (in kΩ).
R_D represents the damping resistance (in kΩ).
k_{IW} represents the write current DAC setting (0 to 15).

Note: RC equal to 4KΩ gives a write current range of 10-40mA, and an MR bias current range of 5-15mA. A maximum write current of 45mA may be achieved by reducing the RC resistance, but this reduction also affects the MR bias current range.

The write data (PECL) signals on the WDX and WDY lines drive the optional internal flip-flop which drives the current switch of the selected head. A TTL level applied to the $\overline{TFF}$ pin controls the internal write data flip-flop (which defaults to "Inactive" with an internal pull-up resistor).

See Figures 72 and 73 for timing diagrams.

Write Current DAC

The 4 bits in register 2 (<D3-D0>) represent the binary equivalent of the DAC setting (0-15, LSB first).

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- WDI frequency too low (f < 1MHz)
- Open write head
- No write current

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Invalid head select code
- Low power supply voltage**
- Device in read or idle mode

** Note that a power supply fault will reset the serial register to "power-on" values.

Servo Write Mode

The VM6160 is designed for use in a single or dual preamp configuration. Servo may be written to three heads (one of four* servo banks) of a single preamp, to a servo bank of three heads for each preamp in a dual preamp configuration (six heads simultaneously written), or to a single head on each preamp in a "Dual Write" configuration.

* One of two servo banks in a 6-channel die.

Register 2 contains the servo control bits <D6-D0>. See Table 104 for a servo register bit description and Table 105 for servo mode control information.

In servo mode all read circuitry is powered-down to reduce power dissipation. The servo mode maximum duty cycle can be expressed with the following equation:

$$T_{Jmax} \geq T_{ambient}\{[(D_{max})(P_{write}) + (1 - D_{max})(P_{read})]\Theta_{JA}\} \qquad \textit{(eq. 57)}$$

T_{Jmax} represents the maximum junction temperature, D_{max} represents the maximum duty cycle, $P_{write/read}$ represents the power in write or read mode, and Θ_{JA} represents the junction-to-ambient thermal resistance

Table 98 Head Select

HS3* 0:<D3>	HS2 0:<D2>	HS1 0:<D1>	HS0 0:<D0>	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
(all other combinations)				dummy

* 12-channel version only.

Note: The head select lines are equipped with pull-down resistors to ensure known default head selection (head 0).

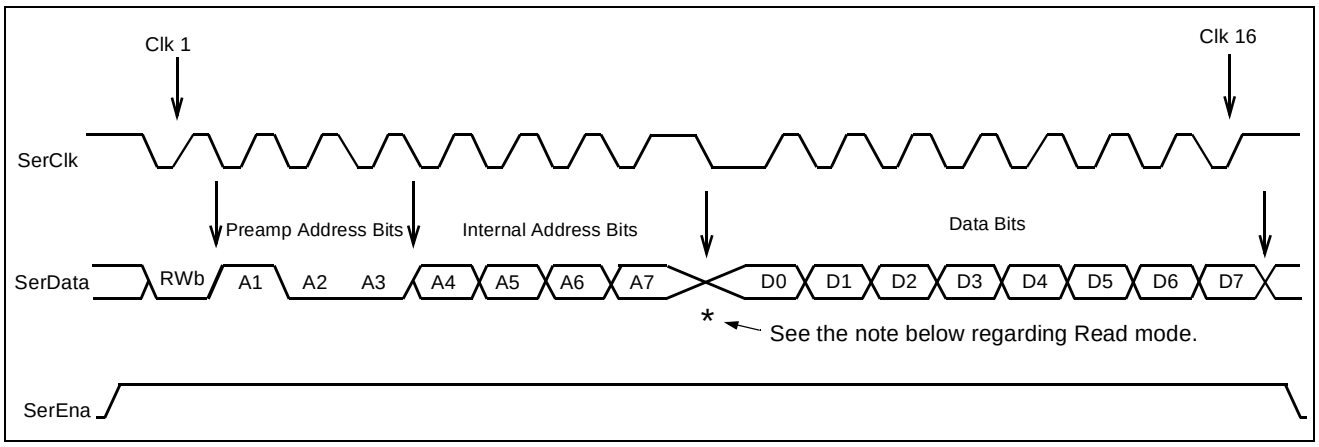


Figure 69 Serial Port Protocol

* For a read operation, the clock rate must be reduced for one period between the <A7> bit and the <D0> bit to provide sufficient time for the controller to tristate its output (release control of SDIO), and the VM6160 to untristate (activate control of SDIO). The clock rate need not be reduced during a write operation.

Table 99 Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A4>*				*Preamp Address Bits <A3-A1>*	*R/W <A0>*
Head Select	0	*	0	0	0	001	1/0
Servo	1	*	0	0	1		1/0
Write Current DAC	2	*	0	1	0		1/0
MR Bias Current DAC	3	*	0	1	1		1/0
Control	4	*	1	0	0		1/0
Vendor ID	5 (read only)	*	1	0	1		1

* Reserved

Table 100Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Head Select	0	*	*	*	CE**	HS3**	HS2	HS1	HS0
Servo	1	*	DWE	UCE	LCE	UC1	UC0	LC1	LC0
Write Current DAC	2	*	*	*	*	WC3	WC2	WC1	WC0
MR Bias Current DAC	3	*	*	*	Bias4	Bias3	Bias2	Bias1	Bias0
Control	4	*	*	BHVOE	PWREN	WSER	BIASOVR	IDLEOVR	FAST
Vendor ID	5 (read only)	***	***	***	***	***	***	1	1

* Reserved
** In the 6-channel version, HS3 is not used; the CE bit occupies bit <D3> and bit <D4> is reserved.
***These values are dependent on channel-count and revision level. Contact VTC for additional information.

Table 101Mode Select

CS	UCL	CE* 0:<D4>	IDLEOVR 4:<D1>	PWREN 4:<D4>	WRT	BIAS	BIASOVR 4:<D2>	WSER 4:<D3>	MODE
1	X	X	X	X	X	X	X	X	Idle
X	X	X	1	X	X	X	X	X	Idle
0	0	0	X	0	X	X	X	X	Idle (unselected preamp)
	1	1							
0	0	0	X	1	X	X	X	X	Read Standby (unselected preamp)
	1	1							
0	1	0	0	X	1	0	0	0	Read Standby
0	1	0	0	X	0	0	0	0	Write (lower), reader off
0	0	1	0	X	0	0	0	0	Write (upper), reader off
0	1	0	0	X	0	1	X	0	Write (lower), reader biased
						X	1		
0	0	1	0	X	0	1	X	0	Write (upper), reader biased
						X	1		
0	1	0	0	X	1	1	X	0	Read (lower), selected head
						X	1		
0	0	1	0	X	1	1	X	0	Read (upper), selected head
						X	1		

* In the 6-channel version the CE bit occupies register 0, bit <D3>.

Note: This table constitutes all valid modes except servo write.
Invalid mode selection will result in Read Standby or Idle mode selection.

Table 102Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Head Select	0	<0001 1111>
Servo	1	<0000 0000>
Write Current DAC	2	<0000 0000>
MR Bias Current DAC	3	<0000 0000>
Control	4	<0000 0010>
Vendor ID	5	<xxxx xx11>**

** These values are dependent on channel-count and revision level. Contact VTC for additional information.

Table 103Control Register Fields

Register:Bit	Name	Description (“active” when bit = 1)
4:<D0>	FAST	High Pass Frequency (raises low corner frequency of bandpass by a factor of 2)
4:<D1>	IDLEOVR	Idle Override (forces part into idle mode)
4:<D2>	BIASOVR	Bias Override (activates MR bias current regardless of mode)
4:<D3>	WSER	Write Servo (activates servo functionality)
4:<D4>	PWREN	Power Enable (places an “unselected” preamp into Read Standby mode)
4:<D5>	BHVOE	Buffered Head Voltage Output Enable (activates BHV output)

Table 104Servo Register Bit Description

Register:Bit	Name	Description	
1:<D6>	Dual Write Enable	Enables a dual preamp / single head servo write. Head Selection is shown in Table 98.	
1:<D5>	Upper Chip Enable	Enables “upper” preamp servo write. (Independent of <D4>)	
1:<D4>	Lower Chip Enable	Enables “lower” preamp servo write. (Independent of <D5>)	
		6-channel	12-channel
1:<D3>	Upper Chip Servo Bank: MSB	Upper Preamp: 0X -- Bank 0 (Heads 0,2,4) 1X -- Bank 1 (Heads 1,3,5)	Upper Preamp: 00 -- Bank 0 (Heads 0,4,8) 01 -- Bank 1 (Heads 1,5,9) 10 -- Bank 2 (Heads 2,6,10) 11 -- Bank 3 (Heads 3,7,11)
1:<D2>	Upper Chip Servo Bank: LSB		
1:<D1>	Lower Chip Servo Bank: MSB	Lower Preamp: 0X -- Bank 0 (Heads 0,2,4) 1X -- Bank 1 (Heads 1,3,5)	Lower Preamp: 00 -- Bank 0 (Heads 0,4,8) 01 -- Bank 1 (Heads 1,5,9) 10 -- Bank 2 (Heads 2,6,10) 11 -- Bank 3 (Heads 3,7,11)
1:<D0>	Lower Chip Servo Bank: LSB		

Table 105Servo Modes

WRT	WSER 4:<D3>	Dual Write Enable 1:<D6>	Upper Chip Enable 1:<D5>	Lower Chip Enable 1:<D4>	Upper Chip Servo Bank 1:<D3,2>	Lower Chip Servo Bank 1:<D1,0>	UCL	Mode
0	0	X	X	X	<X,X>	<X,X>	X	Write (non-servo)
0	1	X	0	1	<X,X>	<0,0> <0,1> <1,0> <1,1>	1	Lower Preamp Servo
0	1	X	1	0	<0,0> <0,1> <1,0> <1,1>	<X,X>	0	Upper Preamp Servo
0	1	X	1	1	<0,0> <0,1> <1,0> <1,1>	<0,0> <0,1> <1,0> <1,1>	X	Both Preamps in Servo
0	1	1	0	0	<X,X>	<X,X>	X	Dual Write, both preamps in servo. Each preamp writes to a single head (governed by the head select table (Table 98).

Note: This table constitutes all valid servo write modes.
Invalid servo write mode selection will result in Read Standby or Idle mode selection.

Table 106Serial Interface Parameters

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNITS
Serial Clock (SCLK) Rate, Write				20	MHz
Serial Clock (SCLK) Rate, Read				14	
SENA to SCLK delay	T_{sens}	30			ns
SDIO setup time	T_{ds}	5			ns
SDIO hold time	T_{dh}	5			ns
SCLK cycle time	T_{c}	50			ns
SCLK high time	T_{ckh}	20			ns
SCLK low time	T_{ckl}	20			ns
SENA hold time	T_{shld}	25			ns
Time between I/O operations	T_{sl}	100			ns
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			50	ns
Time to activate SDIO	T_{act}			50	ns
Duration of SerEna (read)	T_{rd}	905			ns
Duration of SerEna (write)	T_{wt}	855			ns

Note: SENA assertion level is high.

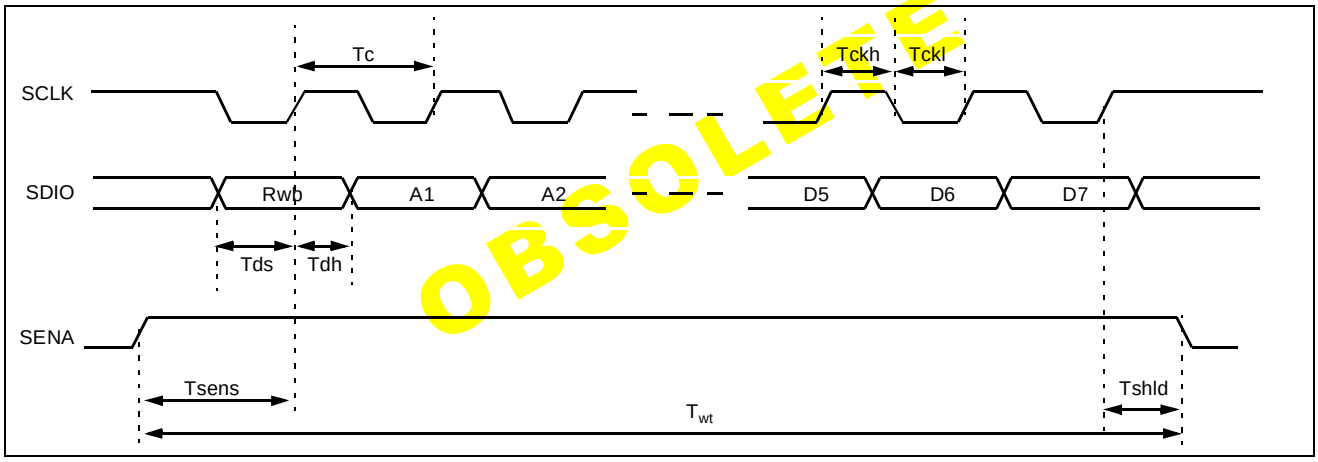


Figure 70 Serial Port Timing

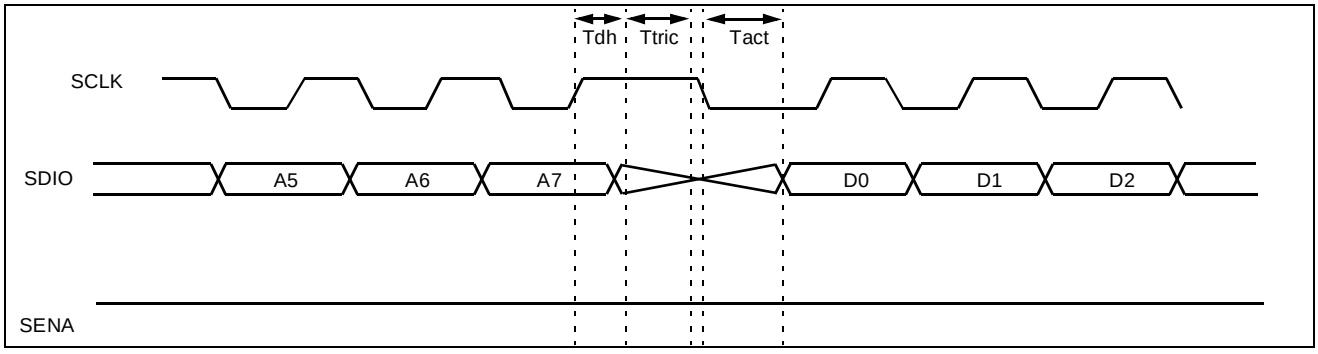


Figure 71 Serial Port Timing - Tristate Control

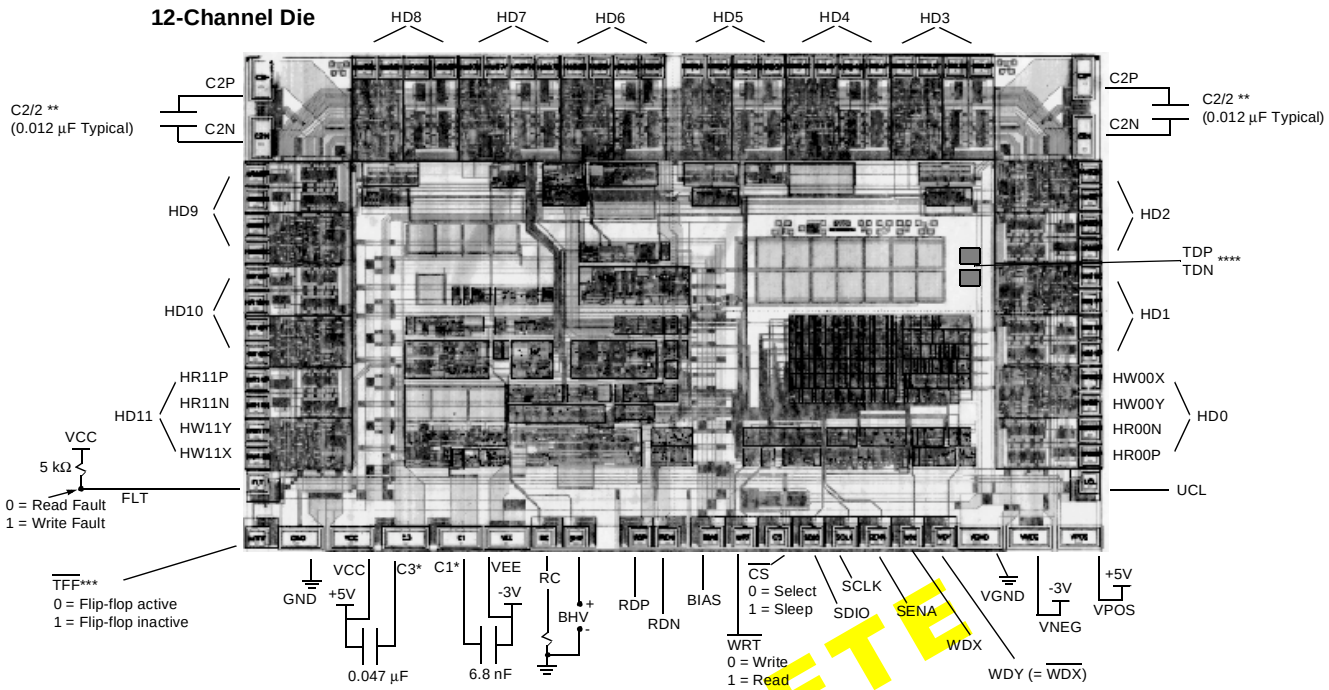
PIN_FUNCTION LIST AND DESCRIPTION

50)	$\overline{CS}$	(I)	Chip Select: A TTL low level enables the device. Pin defaults high (idle).
51)	UCL	(I)	Upper Chip Low: A TTL low level designates preamp as the “upper” preamp. A TTL high level designates preamp as the “lower” preamp. Pin defaults high (lower preamp designation).
52)	$\overline{WRT}$	(I*)	Write: A TTL low level enables write mode. Pin defaults high (non-write).
53)	FLT	(O*)	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
54)	WDX, WDY	(I*)	Differential Pseudo-ECL write data inputs.
55)	HR0P-HR11P	(I)	MR head connections, positive end.
56)	HR0N-HR11N	(I)	MR head connections, negative end.
57)	HW0X-HW11X	(O)	Thin-Film write head connections, positive end.
58)	HW0Y-HW11Y	(O)	Thin-Film write head connections, negative end
59)	RDP, RDN	(O*)	Read Data: Differential read signal outputs.
60)	C1		Noise bypass capacitor input for the MR bias current source.
61)	C2P, C2N		DC blocking capacitor for reader inputs.
62)	C3		Compensation capacitor for the MR head current loop.
63)	BHV	(O)	Buffered MR Head Voltage output.
64)	VEE, VNEG	(*)	-3.0V supply
65)	VCC, VPOS	(*)	+5.0V supply
66)	GND, VGND	(*)	Ground
67)	$\overline{TFF}$	(I*)	Toggle Flip-Flop A TTL high level disables the write data flip-flop. Pin defaults high (flip-flop disabled). A TTL low level (when tied to ground) enables the write data flip-flop.
68)	RC		Reference Voltage for both MR Bias and Write Current.
69)	BIAS	(I*)	Bias Enable: A TTL high level enables MR bias current to the selected head. Pin defaults low (bias disabled).
70)	SENA	(I*)	Serial Enable: Serial port enable signal; see Figures 71 and 72.
71)	SCLK	(I*)	Serial Clock: Serial port clock; see Figures 71 and 72.
72)	SDIO	(I/O*)	Serial Data: Serial port data; see Figures 71 and 72.

(I = Input pin, O = Output pin)

* When more than one device is used, these signals can be wire-OR’ed together.

TYPICAL CONNECTION DIAGRAM



Application Notes:

* Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

** This capacitor is split to minimize parasitics from all heads to the AC-coupling capacitor.
A single C2 capacitor may be connected to either set of C2P/C2N pads, however, gain linearity across heads (and bandwidth) will be compromised with a single C2 capacitor configuration.
The C2 capacitor sets the lower corner frequency of the preamplifier's bandpass filter. The equation that sets this corner can be approximated by: $f = 1/(2\pi RC)$ where $R = 12\Omega$ and $C = C2 = .024\mu F$ typical.

***The $\overline{\text{TFF}}$ (Toggle Flip-Flop) is a bondable option. This pad may be directly connected to VCC (+5V) or GND (0V).
(An internal pull-up resistor defaults the flip-flop to inactive.)

****TDP/TDN (Thermal Diode Positive/Negative). These pads connect to a 'stand-alone' diode that can be used for temperature measurement.

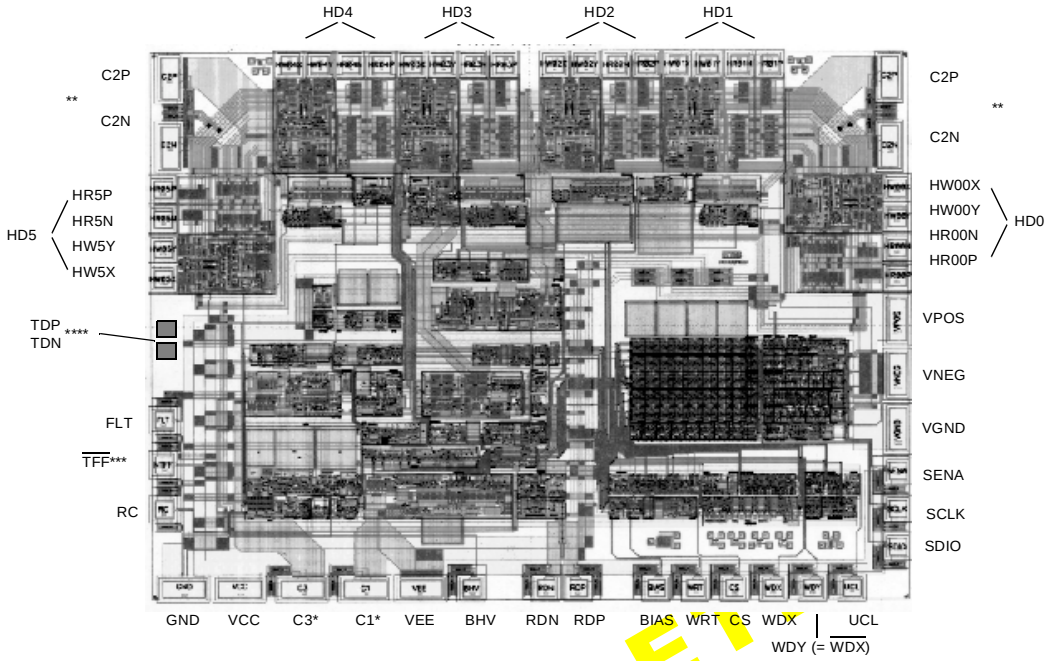
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VPOS - VGND
  VNEG - VGND

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.

- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.

Note: Pad names for the 6-channel die are shown on the following page.

6-Channel Die (application connections and values are identical to those shown on the previous page)



STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 10 mA, I_W = 25 mA, R_{MR} = 30Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode	75	84	105	mA
		Read Mode, Fast Read Enabled	85	105	135	
		Write Mode, BIAS and BIASOVR Low (Bias Current to Dummy Head)	95	122	150	
		Write Mode, BIAS or BIASOVR High (Bias Current to Selected Head)	110	140	175	
		Read Standby	50	60	75	
		Idle Mode	9	13.5	20	
		Servo Mode	160	210	275	
V_{EE} Power Supply Current	I_{EE}	Read Mode	45	55	68	mA
		Read Mode, Fast Read Enabled	60	78	105	
		Write Mode, BIAS and BIASOVR Low (Bias Current to Dummy Head)	65	85	105	
		Write Mode, BIAS or BIASOVR High (Bias Current to Selected Head)	80	105	130	
		Read Standby	27	35	46	
		Idle Mode	0.1	1.3	3.5	
		Servo Mode	135	172	220	
Power Supply Dissipation	P_d	Read Mode	459	585	802	mW
		Read Mode, Fast Read Enabled	545	759	1089	
		Write Mode, BIAS and BIASOVR Low (Bias Current to Dummy Head)	603	865	1172	
		Write Mode, BIAS or BIASOVR High (Bias Current to Selected Head)	711	1015	1392	
		Read Standby	298	405	564	
		Idle Mode	41	71	122	
		Servo Mode	1085	1566	2239	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{CC} - 1.9		V_{CC} - 1.6	V
		TTL	-0.3		0.8	V

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 10 mA, I_W = 25 mA, R_{MR} = 30Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 5V			160	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0V	-160			µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.6	V
V_{CC} Fault Threshold	V_{CTH}	V_{EE} at -3.0V	3.7	4.1	4.4	V
V_{EE} Fault Threshold	V_{ETH}	V_{CC} at +5.0V	-2.4	-2.1	-1.8	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 10mA, L_{MR} = 75nH, R_{MR} = 30Ω, $L_{C1/C2/C3\ (Stray)}$ < 10nH, $C2_{TOTAL}$ = 0.024 µF.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}	R_{RC} = 4kΩ	5	10	15	mA
MR Head Current Tolerance	I_{MR}	5 < I_{MR} < 15 mA	-8		+8	%
		I_{MR} = 10.2 mA	-5		+5	
Unselected MR Head Current					100	µA
MR Bias Reference Voltage	V_{RC}		1.9	2.0	2.1	V
IRC to MR Bias Current Gain	A_{IMR}			10		mA/mA
Differential Voltage Gain	A_V	V_{IN} = 2mV_{pp} @10MHz, R_L(RDP, RDN) = 10kΩ to GND (each side)	180	220	260	V/V
		Fast Mode	175	230	285	
Passband Upper Frequency Limit	f_{HR}	-3dB		130		MHz
		Fast Mode		120		

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 10mA, L_{MR} = 75nH, R_{MR} = 30Ω, $L_{C1/C2/C3\ (Stray)}$ < 10nH, $C2_{TOTAL}$ = 0.024 µF.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Passband Lower -3dB Frequency Limit	f_{LR}	$C2_{total}$ = 0.024µF		600		KHz
		Fast Mode, $C2_{total}$ = 0.024µF		1500		
Equivalent Input Noise	e_{in}	f = 10 MHz		0.55	0.80	$nV/\sqrt{Hz}$
Differential Input Capacitance	C_{IN}			11	16	pF
		Fast Mode		17	26	
Differential Input Resistance	R_{IN}		600	1400		Ω
		Fast Mode	250	700		
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 2mV_{pp} @ f = 10 MHz	6			mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mV_{PP}, f = 10 MHz	45			dB
Power Supply Rejection Ratio	PSRR	100mV_{PP} on V_{CC} or V_{EE}, f = 10 MHz -- no decoupling	40	43		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{PP} , f = 10 MHz	45			dB
Output Offset Voltage	V_{OS}		-125		125	mV
Common Mode Output Voltage	V_{OCM}		V_{CC} - 3.5	V_{CC} - 3.0	V_{CC} - 2.5	V
Common Mode Output Voltage Differential	ΔV_{OCM}	V_{OCM}(Read) - V_{OCM} (Write w/ Bias)	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode No Series Resistance		36	50	Ω
		Read Mode 17Ω Series Resistance	20	56	70	
Output Current	I_O	AC Coupled Load, RDP to RDN	-1.5		1.5	mA
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK} = 10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}	I_{MR} = 10mA	-300		300	mV
		I_{MR} = 15mA	-350		350	
MR Head Potential, Unselected Head	V_{MR}			-700		mV
$I_{MR} \times R_{MR}$ Product	IR_{MR}		150	300	520	mV
Buffered Head Voltage Gain	A_{BHV}		3.92	4	4.08	V/V
BHV Input-Referred Voltage Offset	$V_{OS(BHV)}$	BHV Gain = 4.0 ± 2%	-7		7	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 25mA, $L_H + L_{Stray}$ < 220nH, R_W = 15Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Reference Voltage	V_{RC}	R_{RC} = 4kΩ	1.9	2.0	2.1	V
I_{RC} to Write Current Gain	A_I			10		mA/ mA
Write Current Range	I_W		10		45	mA
Write Current Tolerance	ΔI_W	10 < I_W < 45 mA (Servo mode at T_A = 27°C only)	-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head, I_W = 40mA	9.5	12		V_{pp}
Unselected Head Transition Current	I_{UH}				100	µA
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal Damping Resistance	1520	1900	2280	Ω
Open Head Detect Frequency	f_{OHD}	Open Head	15	20		MHz
Open Head Detect Resistance	R_{OHD}	Open Head	35	41		Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT low, < 5kΩ pull-up	1.0			MHz

* Open Head Detection is guaranteed up to a frequency of 15 MHz and typically operates to 20 MHz.

** Open Head Detection is guaranteed up to a head resistance of 35Ω and typically operates to 60Ω.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. f_{DATA} = 5MHz, $L_H + L_{Stray}$ < 220nH, R_W = 15Ω, I_W = 25mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		45	100	ns
Write to Read Mode	t_{WR}	To 90% of envelope; ± 20mV of final DC value			1.0	µs
Idle to Read Mode [2]	t_{CS}	To 90% of envelope; ± 20mV of final DC value		12	15	µs
HS0 - HS3 to Any Head [2] (Read Mode)	t_{HSR}	To 90% of envelope; ± 20mV of final DC value; I_{MR} unchanged		4.25	5	µs
Write or Read to Idle [2]	t_{RI}	To 10% of read envelope or write current			0.5	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT, < 5kΩ pull-up		0.7	1.5	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT, < 5kΩ pull-up		0.1	0.3	µs
Head Current Propagation Delay[1]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H = 0, R_H = 0			0.1	ns
Rise/Fall Time	t_r / t_f	20-80%		1.3	2	ns
		10-90%		1.9	2.6	

[1] See Figures 72 and 73 for write mode timing diagrams.

[2] From 50% of the 16th rising edge of SCLK when a serial I/O operation is used.

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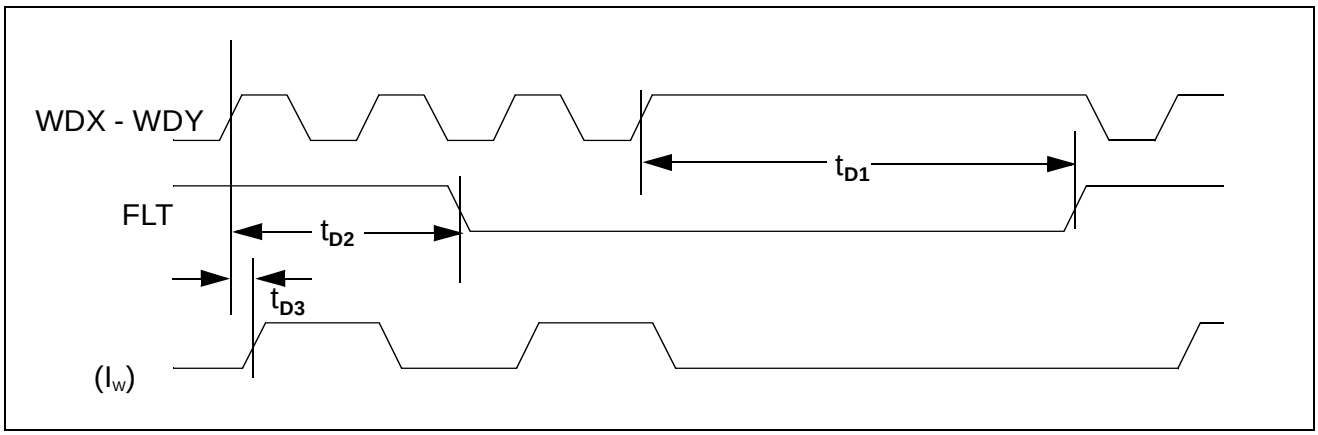

Figure 72 Write Mode Timing Diagram with Flip-Flop Active

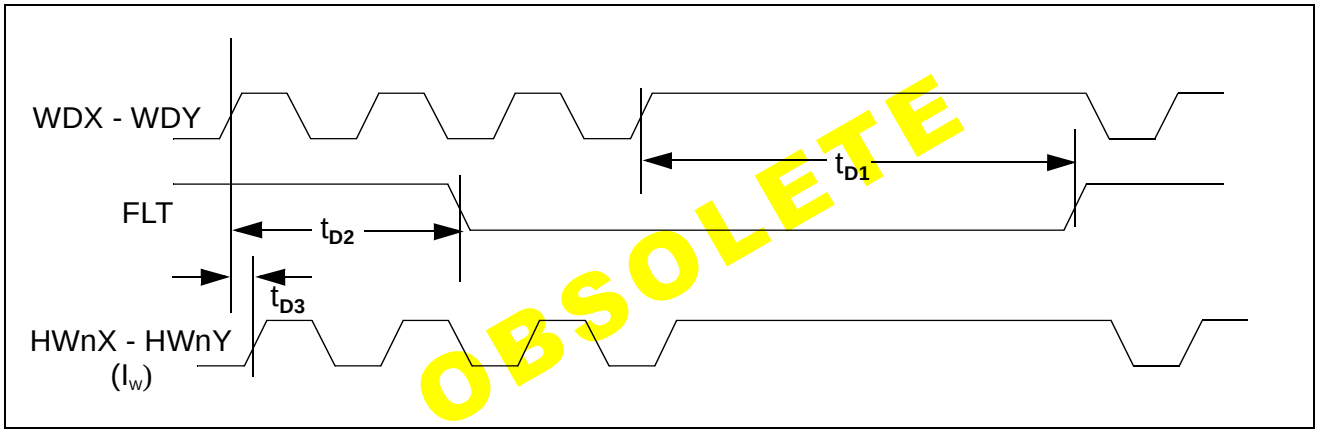

Figure 73 Write Mode Timing Diagram without Flip-Flop Inactive

VM6166

6-CHANNEL DIE

Specific Characteristics

Die size: 172 x 129 Mils

Pad Coordinates for the VM6166 (in Mils)

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BHV	-13.220	-59.941	4x4
BIAS	27.811	-59.941	4x4
C1	-36.776	-59.941	4x10
C2N	79.866	41.071	4x10
C2N	-79.866	41.071	4x10
C2P	79.866	56.835	4x10
C2P	-79.866	56.835	4x10
C3	-50.720	-59.941	4x10
CS	45.150	-59.941	4x4
FLT	-81.441	-21.252	4x4
GND	-77.071	-59.941	4x10
HR00N	81.441	17.823	4x4
HR00P	81.441	11.004	4x4
HR01N	46.504	59.870	4x4
HR01P	53.323	59.870	4x4
HR02N	19.228	59.870	4x4
HR02P	26.047	59.870	4x4
HR03N	-12.409	59.870	4x4
HR03P	-5.591	59.870	4x4
HR04N	-39.685	59.870	4x4
HR04P	-32.866	59.870	4x4
HR05N	-81.441	24.642	4x4
HR05P	-81.441	31.461	4x4
HW00X	81.441	31.461	4x4
HW00Y	81.441	24.642	4x4
HW01X	32.866	59.870	4x4
HW01Y	39.685	59.870	4x4
HW02X	5.591	59.870	4x4
HW02Y	12.409	59.870	4x4
HW03X	-26.047	59.870	4x4
HW03Y	-19.228	59.870	4x4
HW04X	-53.323	59.870	4x4
HW04Y	-46.504	59.870	4x4
HW05X	-81.441	11.004	4x4
HW05Y	-81.441	17.823	4x4
NTFF	-81.441	-31.425	4x4
RC	-81.441	-41.598	4x4
RDN	3.354	-59.941	4x4
RDP	10.484	-59.941	4x4
SCLK	81.441	-41.831	4x4
SDIO	81.441	-50.500	4x4
SENA	81.441	-33.161	4x4
TDN	-81.441	-5.272	4x4oct
TDP	-81.441	2.783	4x4oct
UCL	71.264	-59.941	4x4
VCC	-64.665	-59.941	4x10
VEE	-24.370	-59.941	4x10
VGND	81.441	-23.551	4x10
VNEG	81.441	-11.146	4x10
VPOS	81.441	1.260	4x10
WDX	53.819	-59.941	4x4
WDY	62.488	-59.941	4x4
WRT	36.480	-59.941	4x4

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VM61612

12-CHANNEL DIE

Specific Characteristics

Die size: 227 x 139 Mils

Pad Coordinates for the VM61612 (in Mils)

Pin Name	X Axis	Y Axis	Pad Size
BHV	-25.681	-60.134	4x4
BIAS	9.598	-60.134	4x4
C1	-56.051	-60.134	4x10
C2N	107.327	46.071	4x10
C2N	-107.327	46.071	4x10
C2P	107.327	61.835	4x10
C2P	-107.327	61.835	4x10
C3	-69.996	-60.134	4x10
CS	26.937	-60.134	4x4
FLT	-108.787	-45.362	4x4
GND	-97.638	-60.134	4x10
HR00N	108.787	-31.728	4x4
HR00P	108.787	-38.547	4x4
HR01N	108.787	-4.453	4x4
HR01P	108.787	-11.272	4x4
HR02N	108.787	22.823	4x4
HR02P	108.787	16.004	4x4
HR03N	73.567	64.870	4x4
HR03P	80.386	64.870	4x4
HR04N	46.291	64.870	4x4
HR04P	53.110	64.870	4x4
HR05N	19.016	64.870	4x4
HR05P	25.835	64.870	4x4
HR06N	-12.197	64.870	4x4
HR06P	-5.378	64.870	4x4
HR07N	-39.472	64.870	4x4
HR07P	-32.654	64.870	4x4
HR08N	-66.748	64.870	4x4
HR08P	-59.929	64.870	4x4
HR09N	-108.787	29.642	4x4
HR09P	-108.787	36.461	4x4
HR10N	-108.787	2.366	4x4
HR10P	-108.787	9.185	4x4
HR11N	-108.787	-24.909	4x4
HR11P	-108.787	-18.091	4x4
HW00X	108.787	-18.091	4x4
HW00Y	108.787	-24.909	4x4
HW01X	108.787	9.185	4x4
HW01Y	108.787	2.366	4x4
HW02X	108.787	36.461	4x4
HW02Y	108.787	29.642	4x4
HW03X	59.929	64.870	4x4
HW03Y	66.748	64.870	4x4
HW04X	32.654	64.870	4x4
HW04Y	39.472	64.870	4x4
HW05X	5.378	64.870	4x4
HW05Y	12.197	64.870	4x4
HW06X	-25.835	64.870	4x4
HW06Y	-19.016	64.870	4x4
HW07X	-53.110	64.870	4x4
HW07Y	-46.291	64.870	4x4
HW08X	-80.386	64.870	4x4
HW08Y	-73.567	64.870	4x4
HW09X	-108.787	16.004	4x4
HW09Y	-108.787	22.823	4x4
HW10X	-108.787	-11.272	4x4
HW10Y	-108.787	-4.453	4x4
HW11X	-108.787	-38.547	4x4
HW11Y	-108.787	-31.728	4x4
NTFF	-108.787	-60.134	4x4
RC	-34.035	-60.134	4x4
RDN	-1.795	-60.134	4x4
RDP	-8.925	-60.134	4x4
SCLK	44.276	-60.134	4x4
SDIO	35.606	-60.134	4x4
SENA	52.945	-60.134	4x4
TDN	76.126	7.232	4x4oct
TDP	76.126	16.953	4x4oct
UCL	108.787	-45.362	4x4
VCC	-83.941	-60.134	4x10
VEE	-43.646	-60.134	4x10
VGND	79.894	-60.134	4x10
VNEG	92.945	-60.134	4x10
VPOS	105.992	-60.134	4x10
WDX	61.614	-60.134	4x4
WDY	70.283	-60.134	4x4
WRT	18.268	-60.134	4x4

OBSOLETE

VTC Inc.
Value The Customer™

VM6170S Series

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/ WRITE PREAMPLIFIER

990812 **PRELIMINARY** August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface (Provides Programmable Bias Current, Write Current, Head Selection, TA Threshold and Options Control)
  - Operates from +5 and -4.5 Volt Power Supplies
  - Up to 10-Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Current Sense Configuration
  - MR BIAS Current 5-bit DAC, 6 - 16 mA Range
  - Programmable Read Voltage Gain (250 V/V or 350 V/V)
  - Fast Read Mode
  - Input Noise = 0.85 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 18 pF Typical
  - Head Inductance Range = 100 nH - 300 nH
  - Mask Select Resistors (0, 10, 15, 30 Ω) in series with RDP, RDN
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 65 mA Range
  - Rise Time = 1.5 ns Typical (L_{total} = 66 nH, I_W = 65 mA)
  - Programmable Write Data Flip-Flop (WDFF)

DESCRIPTION

The VM6170S is an integrated bipolar programmable read/ write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6170S contains a thin-film head writer, an MR reader, and associated fault circuitry. It provides bias current and control loops for setting the DC voltages on the MR element.

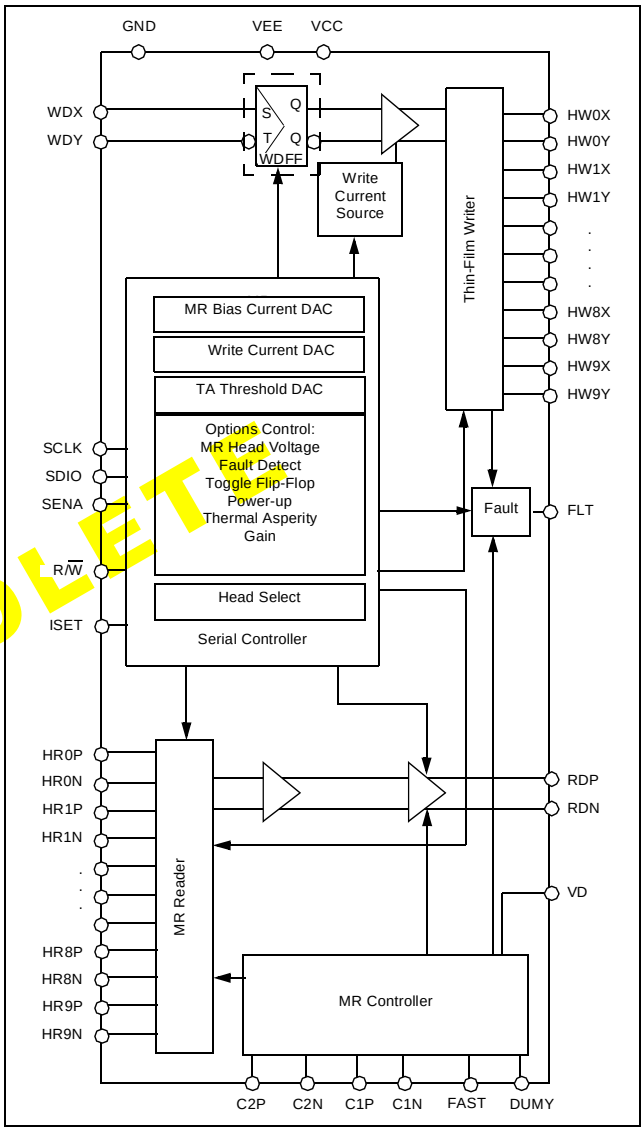
Programmability of the VM6170S is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, read gain and thermal asperity detection threshold.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, an internal pull-up resistor is connected to the mode select line (R/$\overline{W}$) to prevent accidental writing due to an open line.

The VM6170S operates from +5V, -4.5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6170S is available in die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



See page 271 for the Pin Function List and Description.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -7V
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 30mA
Write Current, I_W 100mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J 150°C
Storage Temperature, T_{stg} -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -4.5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 20 - 65 mA
Write Head Inductance, L_W ..... 100 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 6 - 16 mA
Read Head Inductance, L_{MR} ..... 10 - 100 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J 0°C to 125°C

SERIAL INTERFACE CONTROLLER

The VM6170S uses a VTC proprietary 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 109 and 110 for a bit description.

Note: Although the serial interface is available during all modes, VTC recommends no serial activity during read and write operations (except to enter Idle mode) since errors may be generated.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, four reserved preamp bits <A7-A5, A1>, and three register address bits <A4-A2>. The second 8 bits <D7-D0> consist of six data bits <D7-D2> and two reserved timing bits <D1-D0>.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the 16th rising edge, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the rising edge of the 10th cycle (delayed two cycles to allow the controller to release control of SDIO). Upon the falling edge of the 11th cycle <D2> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. Two reserved timing bits <D1-D0> allow time for the controller to tristate on line SDIO and the VM6170S to drive line SDIO.

See Table 113 and Figures 75 and 76 for serial interface timing information.

OPERATIONAL MODES

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the serial registers (the contents of which remain latched).

Idle mode is controlled with the PWRUP bit (register 3, bit <D7>). Note that this bit is the only means of entering idle mode or powering the VM6170S out of Idle mode without a fault. This bit has a power-on-reset value of <0> which enables Idle Mode.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6170S uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external resistor (2.5kΩ nominal, connected between pin ISET and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{15}{(R_{SET})} + k_{IMR}\left(\frac{0.806}{R_{SET}}\right) \qquad \textit{(eq. 58)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{SET} represents the equivalent resistance between the ISET pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

The above I_{MR} equation will give a bias current range of 6-16 mA.

With the use of a negative supply, the MR head center voltage is near ground potential minimizing current spikes during disk contact.

LOWG (Low Gain)

This control bit (register 0, bit <D7>) selects the gain. When high, a gain of 250 V/V is used; when low, a gain of 350 V/V is used. This bit has a power-on-reset value of <0> which selects high gain (350 V/V).

MRHVE (MR Head Voltage Enabled)

This control bit (register 0, bit <D2>) enables the output of the (I_{MR}×R_{MR}) product of the selected head at the RDP-RDN differential outputs. To accurately measure this voltage, the nominal read mode RDP-RDN offset should be noted with no read signal present and MRHVE low. This offset should be subtracted from the differential voltage with MRHVE high:

$$I_{MR} \times R_{MR} = V_{MRDC} - V_{OS} \qquad \textit{(eq. 59)}$$

$I_{MR} \times R_{MR}$ represents the bias-current/head-resistance product.
V_{MRDC} represents the voltage measured at RDP-RDN with MRHVE=1.
V_{OS} represents the RDP-RDN offset with MRHVE=0 and no read signal present.

Fast Read Mode

The Fast Read mode, when enabled, increases the transconductance (tail current) of the first stage of the read amplifier. This effectively increases the lower corner frequency of the amplifier's bandpass by a factor of approximately 15 to 20 without changing the gain.

MR Bias DAC

The 5 bits in register 1 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, loaded LSB first).

Thermal Asperity Detection

If a head-to-disk contact occurs, the thermal asperity in the MR element will result in a fault condition. The threshold for thermal asperity detection is governed by the following equation:

$$V_{TADT} = 0.4 + (0.08 \times k_{TADT}) \qquad \textit{(eq. 60)}$$

V_{TADT} represents the TA threshold (input-referred in mVp-p).
k_{TADT} represents the TA DAC setting (0-15).

Note that a fault condition resulting from a thermal asperity will reset only after the amplitude falls to 40% of the programmed detection threshold. (Hysteresis is disabled for the lower half of the programmable threshold range.)
The thermal asperity detection circuitry may be disabled with the TADD bit (register 3, bit <D2>). This bit has a power-on-reset value of <0> which enables thermal asperity detection.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- MR open head detected
- Thermal Asperity detected
- Low power supply voltage
- Device in write mode

The fault detection circuitry may be disabled with the FLTD bit (register 1, bit <D2>). This bit has a power-on-reset value of <0> which enables fault detection.

Write Mode

In the write mode, the circuit operates as a current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.5kΩ resistor (connected between pin ISET and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{50}{R_{SET}} + k_{IW}\left(\frac{3.629}{R_{SET}}\right)\right] \qquad \textit{(eq. 61)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{SET} represents the equivalent resistance between the ISET pin and ground (in kΩ).
k_{IW} represents the write current DAC setting (0 to 31).

The above I_W equation will give a write current range of 20-65 mA.

The write data (PECL) signals on the WDX and WDY lines drive the optional internal flip-flop which drives the current switch of the selected head.

Control bit TFFD (register 2, bit <D2>) enables the internal write data flip-flop. This bit has a power-on-reset value of <0> which disables the flip-flop.

See Figures 77 and 78 for timing diagrams.

Write Current DAC

The 5 bits in register 2 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, loaded LSB first).

Write-to-Read Recovery Enhancement

The following conditions are maintained to reduce write-to-read recovery time:

- MR bias current is maintained in write mode
- Reader outputs are high impedance so that the AC-coupling capacitors hold their charge until the next read

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open head
- No write current

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Low power supply voltage
- Device in read mode

Table 107Head Select

HS3 3:<D6>	HS2 3:<D5>	HS1 3:<D4>	HS0 3:<D3>	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(all other combinations)				0

Note: The head-select lines are equipped with pull-down resistors to ensure known default head selection (head 0). Note that head 0 is selected for all unrecognized head-select codes.

Table 108DUMY Mode for Bias Current

DUMY (bias only)	CONDITION
0	Bias current flows to the selected head. (see Table 107)
1	Bias current flows to a dummy head. (a 28Ω resistor)

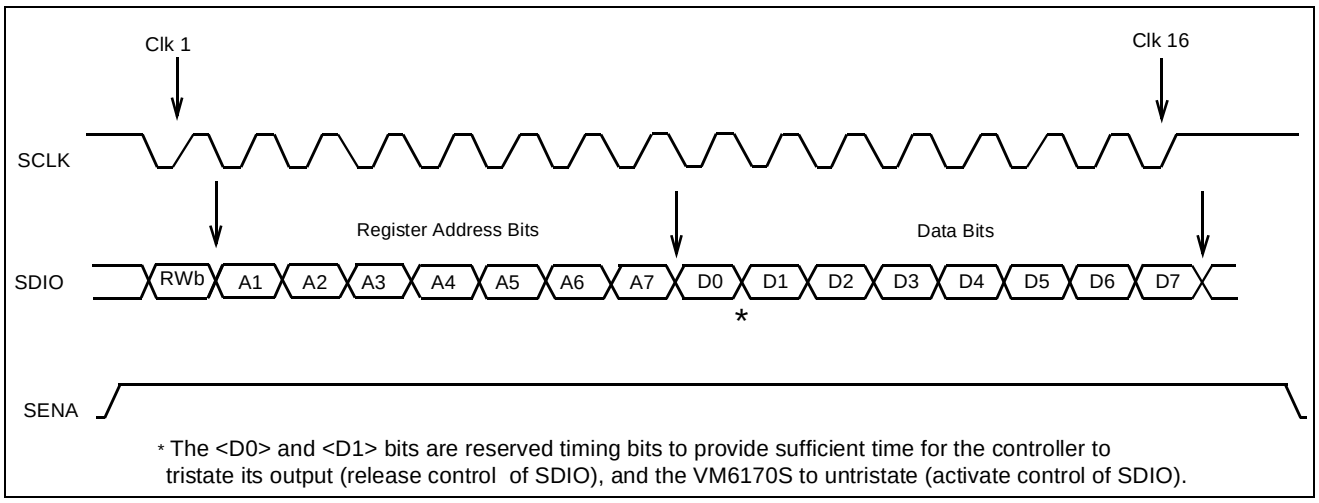


Figure 74 Serial Port Protocol

Table 109Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A1>*							*R/W <A0>*
Gain / Thermal Asperity / MR Head Voltage	0	a	a	a	0	0	0	a	1/0
MR Bias / Fault Detect	1	a	a	a	0	0	1	a	1/0
Write Current DAC / Toggle Flip-Flop	2	a	a	a	0	1	0	a	1/0
Power Up / Head Select / Thermal Asperity Disable	3	a	a	a	0	1	1	a	1/0
Vendor ID	4 (read only)	a	a	a	1	0	0	a	1

a. Reserved

Table 110Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Gain / Thermal Asperity / MR Head Voltage	0	LOWG	TADT3	TADT2	TADT1	TADT0	MRHVE	a	a
MR Bias / Fault Detect	1	IMR4	IMR3	IMR2	IMR1	IMR0	FLTD	a	a
Write Current DAC / Toggle Flip-Flop	2	IW4	IW3	IW2	IW1	IW0	TFFD	a	a
Power Up / Head Select / TA Disable	3	PWRUP	HS3	HS2	HS1	HS0	TADD	a	a
Vendor ID	4 (read only)	0	0	0	0	0	0	a	a

a. Reserved

Table 111Mode Select

$\overline{R/W}$	FAST	PWRUP 3:<D7>	MODE
1	0	1	Read
1	1	1	Read Fast
0	X	1	Write
X	X	0	Idle

Table 112Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Gain / Thermal Asperity / MR Head Voltage	0	<0000 0000>
MR Bias / Fault Detect	1	<0000 0000>
Write Current DAC / Toggle Flip-Flop	2	<0000 0000>
Power Up / Head Select / TA Disable	3	<0000 0000>
Vendor ID	4	<0000 0000>

Table 113Serial Interface Parameters

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNITS
Serial Clock (SCLK) Rate		.001		20	MHz
SENA to SCLK delay	T_{sens}	65			nS
SDIO setup time	T_{ds}	15			nS
SDIO hold time	T_{dh}	10			nS
SCLK cycle time	T_{c}	50			nS
SCLK high time	T_{ckh}	20			nS
SCLK low time	T_{ckl}	20			nS
SENA hold time	T_{shld}	20			nS
Time between I/O operations	T_{sl}	100			nS
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			40	nS
Time to activate SDIO	T_{act}			20	nS
Duration of SENA	T_{rd}	885			nS
SENA to SDIO Tristate Delay	T_{z}			50	nS

Note: SENA assertion level is high.

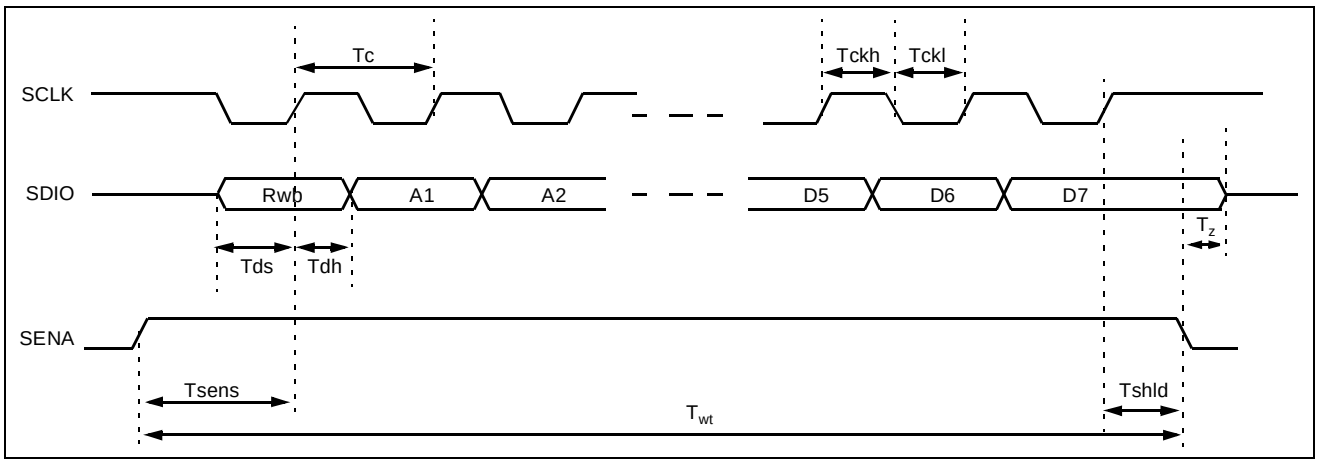


Figure 75 Serial Port Timing

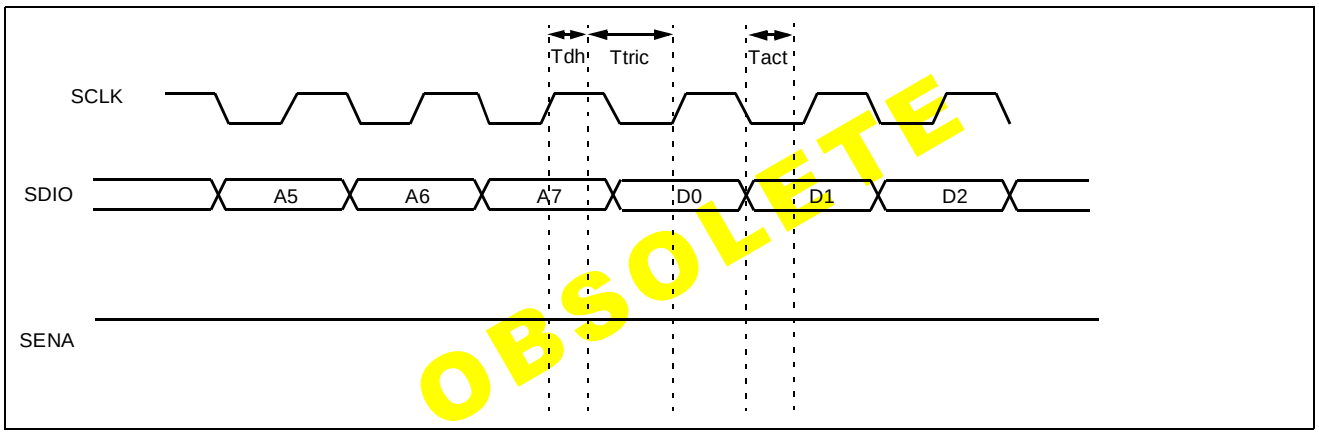


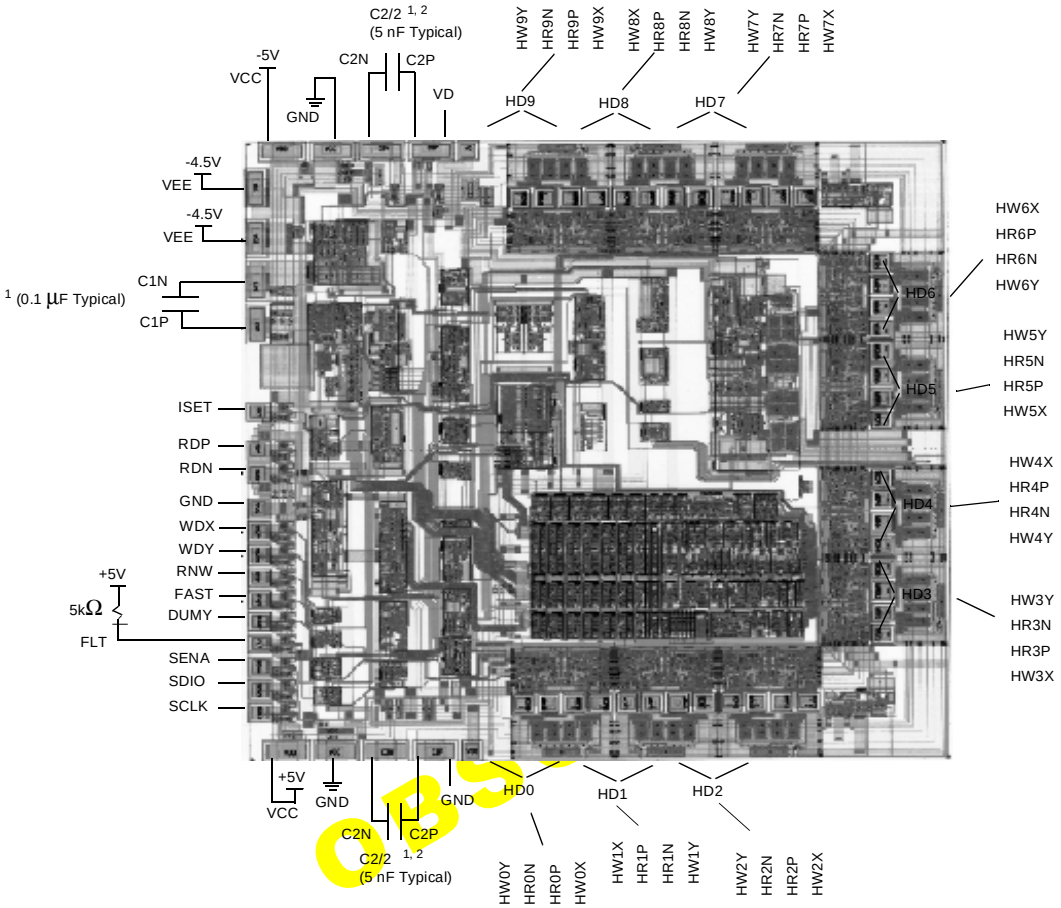
Figure 76 Serial Port Timing - Tristate Control

PIN FUNCTION LIST AND DESCRIPTION

Signal	*Input/Output* [a]	*Description*
DUMY	I	Dummy Head for bias current: A TTL high level selects a dummy head (for MR bias current only). Pin defaults low (non-dummy).
R/$\overline{W}$	I [b]	Read/$\overline{Write}$: A TTL low level enables write mode. Pin defaults high (read mode).
FLT	O [b]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
WDX, WDY	I [b]	Differential Pseudo-ECL write data inputs.
HR0P-HR9P	I	MR head connections, positive end.
HR0N-HR9N	I	MR head connections, negative end.
HW0X-HW9X	O	Thin-Film write head connections, positive end.
HW0Y-HW9Y	O	Thin-Film write head connections, negative end
RDP, RDN	O [b]	Read Data: Differential read signal outputs.
C1P, C1N		Noise bypass capacitor input for the MR bias current source.
C2P, C2N		Compensation capacitor for the MR head current loop.
VD	I [b]	Analog Voltage reference for disk bias.
VEE	[b]	-4.5V supply
VCC	[b]	+5.0V supply
GND	[b]	Ground
ISET	[b]	Reference Current for both MR Bias and Write Current.
FAST	I [b]	FAST Read Mode: A TTL high level enables FAST read mode. Pin defaults low (FAST disabled).
SENA	I [b]	Serial Enable: Serial port enable signal; see Figures 75 and 76.
SCLK	I [b]	Serial Clock: Serial port clock; see Figures 75 and 76.
SDIO	I/O [b]	Serial Data: Serial port data; see Figures 75 and 76.

a. I = Input pin, O = Output pin
b. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL CONNECTION DIAGRAM



Application Notes:

73) Minimizing parasitics at this node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

74) This capacitor is split to minimize parasitics from all heads to the AC-coupling capacitor.
A single C2 capacitor may be connected to either set of C2P/C2N pads, however, performance may be compromised with a single C2 capacitor configuration.

75) VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
VCC - GND
VEE - GND

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 12 mA, I_W = 65 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode, Serial I/O Active		99	113	mA
		Read Mode, Serial I/O Inactive		91.5	101	
		Write Mode		160	172	
		Idle Mode, Serial I/O Active		24		
		Idle Mode, Serial I/O Inactive		17		
V_{EE} Power Supply Current	I_{EE}	Read Mode		61	67	mA
		Write Mode		135	142	
		Idle Mode		8		
Power Supply Dissipation	P_d	Read Mode, Serial I/O Active		765	865	mW
		Read Mode, Serial I/O Inactive		730	804	
		Write Mode		1400	1650	
		Idle Mode, Serial I/O Active		155	TBD	
		Idle Mode, Serial I/O Inactive		120		
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		CMOS	3.5		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{IH} - 1.5		V_{IL} - 0.25	V
		CMOS	-0.3		1.5	V
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{CC} Fault Threshold	V_{CTH}		3.75		4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75		-3.25	V
Disk Reference Voltage Range	V_D		-250		250	mV
Bias Reference Voltage	V_{SET}	R_{SET} = 2500Ω		2.5		V
Monitored MR DC Voltage Accuracy (RDP-RDN)	V_{MRDC}	V_{MRDC}-V_{OS}	-6		6	%

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 12mA, L_{MR} = 25nH, R_{MR} = 42Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}	R_{SET} = 2500Ω	6		16	mA
MR Head Current Tolerance	I_{MR}	x = 6 + 0.322k_{IMR}, R_{SET} = 2500Ω	.95x		1.05x	mA
Unselected MR Head Current					100	µA
I_{SET} to MR Bias Current Gain	A_{IMR}	R_{SET} = 2500Ω, k_{IMR} = 31		16		mA/ mA
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, LOWG=0	260	350	440	V/V
		V_{IN} = 1mV_{pp} @10MHz, LOWG=1	185	250	315	
Passband Upper Frequency Limit	f_{HR}	-1dB		TBD		MHz
		-3dB	110			
Passband Lower -3dB Frequency Limit	f_{LR}	C_2 = 6nF	0.1	0.3	0.5	MHz
Passband Lower -3dB Frequency Limit, Fast Recovery Mode	f_{LRF}	$\overline{FAST}$ low		6		MHz
Equivalent Input Noise	e_{in}	1 < f < 20 MHz		0.85		nV/ $\sqrt{Hz}$
Differential Input Capacitance	C_{IN}				10	pF
Differential Input Resistance	R_{IN}				5.8	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 10 MHz	4			mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 1mV_{PP}, 1 < f < 80 MHz	TBD			dB
Power Supply Rejection Ratio	PSRR	100mV_{PP} on V_{CC} or V_{EE}, 1 < f < 50 MHz	TBD			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV_{PP}, 1 < f < 120 MHz	30			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	MRHVE = 0	V_{CC} - 2.9	V_{CC} - 2.6	V_{CC} - 2.3	V
Common Mode Output Voltage Differential	ΔV_{OCM}	V_{OCM} (Read) - V_{OCM} (Write)	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	[a] Includes 10Ω resistor in series with reader output		27 [a]	37 [a]	Ω
Output Current	I_O	AC-Coupled Load, RDP to RDN, Read mode	2.5			mA
		AC-Coupled Load, RDP to RDN, Any other mode			50	nA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 12mA, L_{MR} = 25nH, R_{MR} = 42Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK} = 10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			20	mA
MR Head Potential, Selected Head	V_{MR}		V_D - 500		V_D + 500	mV
Total Harmonic Distortion	THD	Vin = 4mVpp, ten harmonics			0.5	%
Thermal Asperity Detection Threshold	TDAT	x = 0.25 + 0.09k_{TADT} Input-Referred, R_{SET} = 2500Ω	0.75x		1.25x	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_W = 65mA, L_H = 90nH, R_H = 17Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SET} to Write Current Gain	A_{IW}	R_{SET} = 2500Ω, k_{IW} = 31		65		mA/mA
Write Current Range	I_W	R_{SET} = 2500Ω	20		65	mA
Write Current Tolerance	ΔI_W	x = 20 + 1.452k_{IW}, R_{SET} = 2500Ω	0.92x		1.08x	mA
Differential Head Voltage Swing	V_{DH}	Open Head	9	10		V_{pp}
Unselected Head Transition Current	I_{UH}				50	$µA_{pk}$
Differential Output Capacitance	C_O				5	pF
Time Between Transitions for Safe Condition	t_{SAFE}	FLT low			500	ns
Time Between Transitions for Fault Inhibition	t_{INH}	FLT function inhibited		15	23	ns

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. f_{DATA} = 5MHz, L_H = 66nH, R_H = 14Ω, I_W = 65mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.5	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope; ± 10mV of final DC value			1.0	µs
Idle (SCLK 16th rising edge) to Read Mode	t_{CS}	To 90% of envelope; ± 10mV of final DC value			50	µs
		FAST = high for 3.5 µs			5	
Head (SCLK 16th rising edge) to Any Head (including DUMY)	t_{HS}	To 90% of envelope; ± 10mV of final DC value; I_{MR} unchanged			50	µs
		FAST = high for 3.5 µs			5	
SCLK 16th rising edge to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. f_{DATA} = 5MHz, L_H = 66nH, R_H = 14Ω, I_W = 65mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
I_{MR} (max) to I_{MR} (min)	t_{IMR}	To 90% of envelope; ± 10mV of final DC value		5	TBD	µs
I_{MR} (min) to I_{MR} (max)	t_{IMR}	To 90% of envelope; ± 10mV of final DC value; I_{MR} unchanged		200	TBD	µs
Safe to Unsafe [a]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [a]	t_{D2}	50% WDX to 50% FLT			1.0	µs
Head Current Propagation Delay [a]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H = 0, R_H = 0			0.2	ns
Rise/Fall Time	t_r / t_f	20-80%		1.5	TBD	ns
Settling Time	t_{WSET}	± 10%			TBD	µs
Overshoot	W_{cov}			30	TBD	%

a. See Figures 77 and 78 for write mode timing diagrams.

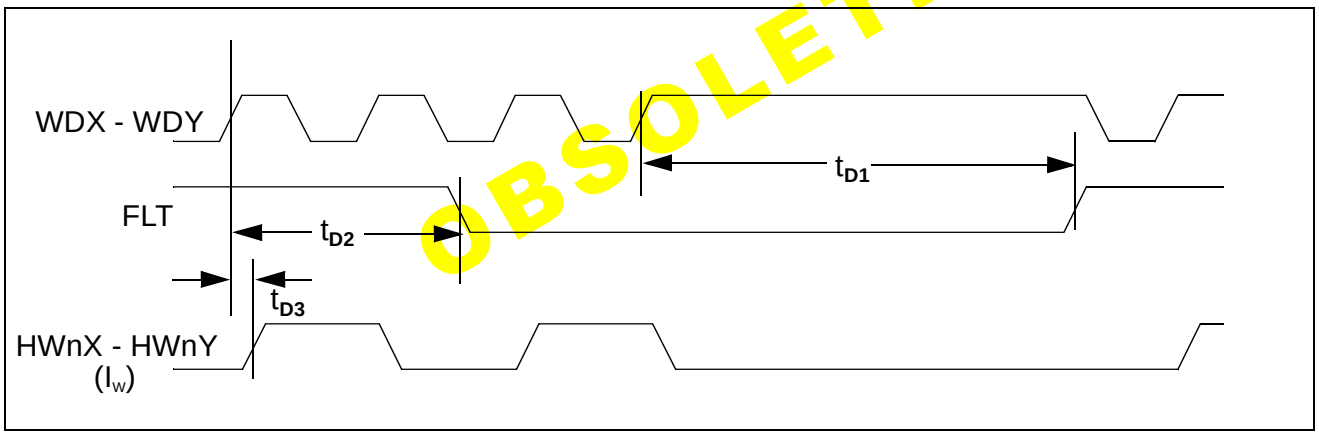


Figure 77 Write Mode Timing Diagram with Flip-Flop Active

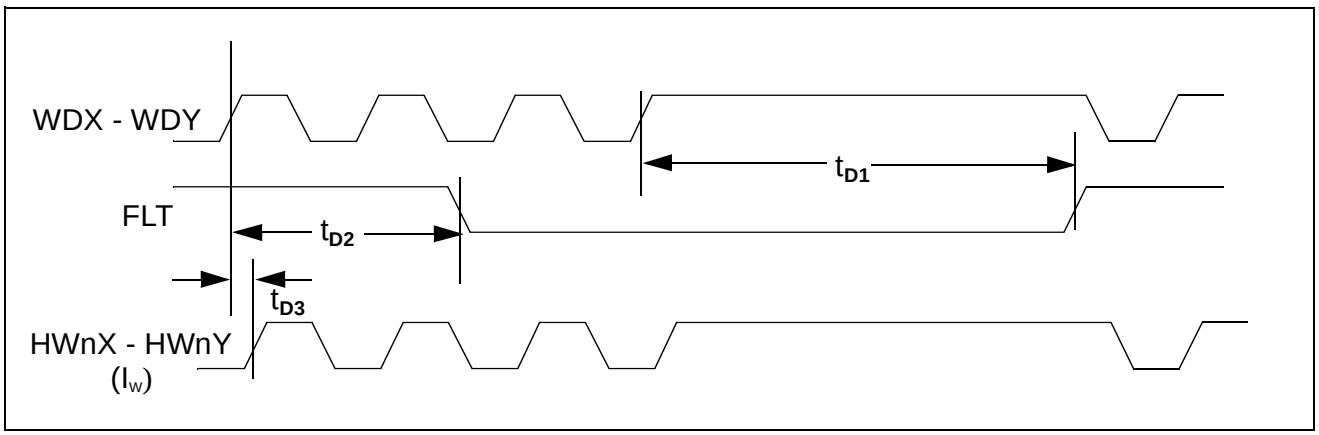


Figure 78 Write Mode Timing Diagram with Flip-Flop Inactive

VM6170S

10-CHANNEL DIE

Specific Characteristics

Die size: 182 X 179 Mils

VM6170S Pad Coordinates (in Mils)

Pin Name	X Axis	Y Axis	Pad Size
C1N	-49.163	-84.902	4x10
C1P	-36.506	-84.902	4x10
C2N	86.398	-53.543	4x10
C2N	-86.398	-53.543	4x10
C2P	86.398	-41.142	4x10
C2P	-86.398	-41.142	4x10
DUMY	49.026	-84.902	4x4
FAST	42.530	-84.902	4x4
FLT	55.522	-84.902	4x4
ISET	-11.732	-84.902	4x4
HR0N	72.618	-12.657	4x4
HR1N	72.618	19.823	4x4
HR2N	72.618	39.311	4x4
HR3N	40.807	71.122	4x4
HR4N	21.319	71.122	4x4
HR5N	-21.319	71.122	4x4
HR6N	-40.807	71.122	4x4
HR7N	-72.618	39.311	4x4
HR8N	-72.618	19.823	4x4
HR9N	-72.618	-12.657	4x4
HR0P	72.618	-6.161	4x4
HR1P	72.618	13.327	4x4
HR2P	72.618	45.807	4x4
HR3P	47.303	71.122	4x4
HR4P	14.823	71.122	4x4
HR5P	-14.823	71.122	4x4
HR6P	-47.303	71.122	4x4
HR7P	-72.618	45.807	4x4
HR8P	-72.618	13.327	4x4
HR9P	-72.618	-6.161	4x4
RDN	6.102	-84.902	4x4
RDP	-0.394	-84.902	4x4
RNW	36.033	-84.902	4x4
SCLK	75.010	-84.902	4x4
SDIO	68.514	-84.902	4x4
SENA	62.018	-84.902	4x4
GND	16.535	-84.902	4x4
GND	86.398	-31.693	4x4
GND	86.398	-65.945	4x10
GND	-86.398	-65.945	4x10
VD	-86.398	-31.693	4x4
VCC	86.398	-78.376	4x10
VCC	-86.398	-78.435	4x10
VEE	-61.604	-84.902	4x10
VEE	-76.132	-84.902	4x10
HW0Y	72.618	-19.154	4x4
HW1Y	72.618	26.319	4x4
HW2Y	72.618	32.815	4x4
HW3Y	34.311	71.122	4x4
HW4Y	27.815	71.122	4x4
HW5Y	-27.815	71.122	4x4
HW6Y	-34.311	71.122	4x4
HW7Y	-72.618	32.815	4x4
HW8Y	-72.618	26.319	4x4
HW9Y	-72.618	-19.154	4x4
HW0X	72.618	0.335	4x4
HW1X	72.618	6.831	4x4
HW2X	72.618	52.303	4x4
HW3X	53.799	71.122	4x4
HW4X	8.327	71.122	4x4
HW5X	-8.327	71.122	4x4
HW6X	-53.799	71.122	4x4
HW7X	-72.618	52.303	4x4
HW8X	-72.618	6.831	4x4
HW9X	-72.618	0.335	4x4
WDY	29.537	-84.902	4x4
WDX	23.041	-84.902	4x4

OBSOLETE

VTC Inc.
Value The Customer™

VM6180 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 **PRELIMINARY** August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface with Readback (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Bandwidth = 200 MHz Nominal (R_{MR} = 33Ω, L_{MR} < 20nH)
  - Operates from a Single +5 Volt Power Supply
  - Fault Detection Capability
  - 4 Channel Available in a 30-pin VSOP Package
  - 8 Channel Available in a 48-pin TQFP Package
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 5 - 16 mA Range
  - Programmable Read Voltage Gain (200 V/V or 300 V/V Typical)
  - Thermal Asperity Detection and Fast Recovery Compensation
  - Digital and Analog Buffered Head Voltage (BHV) Measurement Modes
  - Input Noise = 0.73 nV/√Hz Typical (R_{MR} = 33Ω, I_{MR} = 10mA)
  - Power Supply Rejection Ratio = 45 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 50 mA Range
  - Rise Time (R_H - 15Ω, L_H = 180 nH, I_W = 30 mA): 4 Channel = 2.2 ns Typical, 8 Channel = 2.7 ns Typical
  - Multi-Channel Servo Write

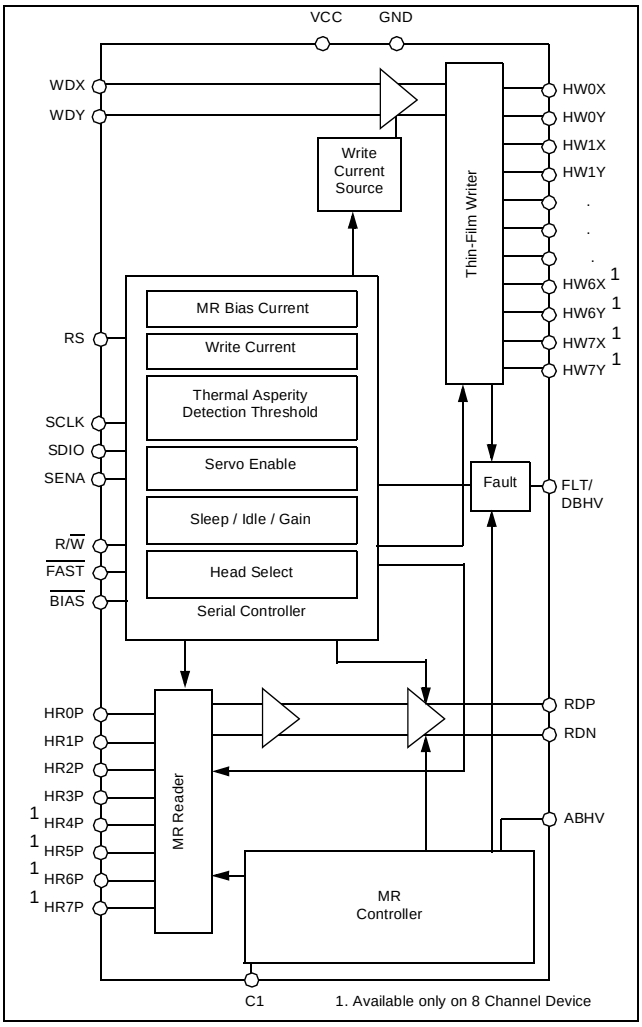
DESCRIPTION

The VM6180 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM6180 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM6180 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available in 4 and 8-channel options. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 30mA
Write Current, I_W 60mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, TJ ..... 150°C
Storage Temperature, Tstg ..... -65° to 150°C
Thermal Impedance, Θ_{JA}
- 30-Lead VSOP ..... 88°C/W
- 48-Lead IQFP ..... 75°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 10 - 50 mA
Write Head Inductance, L_W ..... 10 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 5 - 16 mA
Read Head Inductance, L_{MR} ..... 10 - 100 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J ..... 0°C to 125°C

Serial Interface Controller

The VM6180 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 117 and 118 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry. The bidirectional SDIO line supports full readback.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, three preamp select bits <A3-A1> (which must be <001> for this preamp), and four register address bits <A7-A4>. The second 8 bits <D7-D0> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register. During a read sequence, SDIO will begin outputting data on the falling edge of the 9th cycle. At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.

See Table 119 and Figures 82 and 83 for serial interface timing information.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM6180 uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{10}{R_{RS}} + 0.333(k_{IMR}) \qquad \textit{(eq. 62)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

A "high" TTL level applied to the R/$\overline{W}$ and a "low" TTL level applied to the $\overline{BIAS}$ pins (along with the appropriate levels on the IDLE and $\overline{SLEEP}$ bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 114).

The output of the read preamp is differential.

Read Bias Enable in Read Mode

Taking the $\overline{BIAS}$ pin low in read mode enables MR bias current to the selected head.

Taking the $\overline{BIAS}$ pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

The 5 bits in register 1 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 79 displays the reader output for an uncompensated thermal asperity event.)

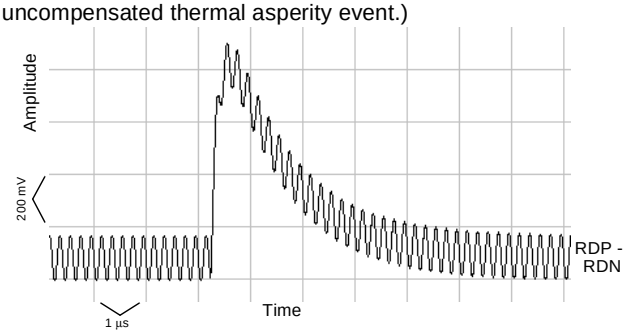


Figure 79 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM6180 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Setting the TADET bit high (register 3, bit <D3>) allows the TA detection circuitry to detect an asperity event (based on the programmable threshold) and report this as a fault condition on the fault line. Setting this bit low disables TA detection.

The threshold for thermal asperity detection has a range of 50 to 800 mV and is governed by the following equation:

$$V_{TADT} = 50(1 + k_{TADT}) \qquad \textit{(eq. 63)}$$

V_{TADT} represents the TA threshold (output-referred in mVpk; ±20%).
k_{TADT} represents the TA DAC setting (0-15).

The TADET bit (register 3, bit <D3>) has a power-on-reset value of <1> which enables thermal asperity detection.

Fast Recovery Compensation

To initiate the Fast Recovery mode:

4) Setting the Fast Recovery (FR) bit high (register 4, bit <D5>) automatically initiates the Fast Recovery mode if a thermal asperity is detected. (Note that the TA detection circuitry must be enabled with the TADET bit.)

5) Taking the $\overline{\text{FAST}}$ pin low (on 8-channel device only) overrides the FR serial bit and initiates the Fast Recovery mode regardless of the detection circuitry. This configuration makes it possible to use the preamp simply as a thermal asperity detector and allows the channel to control the corner frequency movement.

When activated, Fast Recovery Compensation raises the nominal 700 KHz lower -3dB corner frequency to approximately 5 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 80).
After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

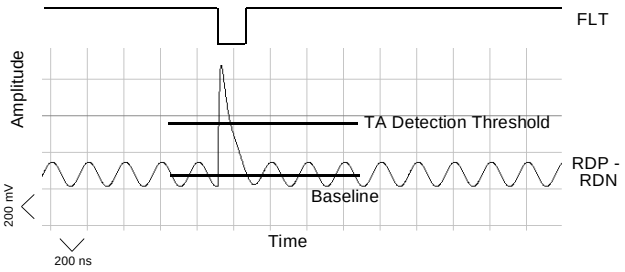


Figure 80 TA Detection and Compensation

Analog Buffered Head Voltage (ABHV)

Setting the MRMEAS bit high (register 4, bit <D3>) allows an amplified representation of the MR bias voltage to be presented on the ABHV pin. This voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} \times R_{MR}) \qquad \textit{(eq. 64)}$$

If the MRMEAS bit is not set, the ABHV pin is high-Z.

Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (register 4, bit <D3>) allows the digital buffered head voltage (DBHV) to be represented on the FLT/DBHV pin.

The DBHV output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 250mV and 450mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Fault Detection

Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the read mode, a low on the FLT line (CMOS with active pull-up) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- Thermal asperity detected (reported if enabled with the TADET bit (register 3, bit <D3>))
- HS2 bit (register 1, bit <D2>) selected (4-channel only)
- An MR open head fault condition is detected but not reported on the FLT line. The voltage on the loop-compensation capacitor (C1) is clamped to provide MR open head protection (until another head is selected or a mode change is initiated).

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{20}{R_{RS}} + 1.29(k_{IW})\right]\left[\frac{1}{1 + \frac{R_H}{R_D}}\right] \qquad \textit{(eq. 65)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).
R_H represents the series head resistance (in Ω).
R_D represents the damping resistance (in Ω).
k_{IW} represents the write current DAC setting (0 to 31).

A “low” TTL level applied to R/$\overline{\text{W}}$ (along with the appropriate levels on the IDLE and $\overline{\text{SLEEP}}$ bits) places the preamp in the write mode (see Table 114). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 84.

Write Current DAC

The 5 bits in register 2 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enable in Write Mode

Taking the $\overline{\text{BIAS}}$ pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the $\overline{\text{BIAS}}$ pin high in write mode disables the MR bias current source and inactivates the MR bias control loop.

Fault Detection

Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the write mode, a high on the FLT line (CMOS with active pull-up) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Write head shorted to ground
- HS2 bit (register 1, bit <D2>) selected (4-channel only)

A low supply fault condition is detected but not reported on the FLT line. The write current source internal to the chip is shutdown and no current flows to any head.

Servo Write Mode

In the servo write mode, four channels or all channels of the VM6180 are written simultaneously.

Setting both the BANK0 and BANK1 bits (register 2, bit <D7> and register 4, bit <D6>) to “1” (along with appropriate levels on the R/$\overline{\text{W}}$ pin and $\overline{\text{IDLE}}$ and $\overline{\text{SLEEP}}$ bits) places the preamp in servo write mode (see Table 114). The HS0 - HS2 register bits (1:<D2-D0>) determine which heads are written (see Table 115).
(For the 4-channel version, all four heads are written whenever servo mode is selected; the head select bits are not used.)

Write mode fault circuits are disabled.

Note: It is the customer's responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Idle Mode

Setting the $\overline{\text{IDLE}}$ bit low (register 4, bit <D1>) places the preamp in Idle mode (see Table 114). The state of the $\overline{\text{BIAS}}$ pin determines the state of the MR bias current source.

Read Bias Enable

Taking the $\overline{\text{BIAS}}$ pin low in Idle mode activates the MR bias current source and directs the MR bias current to an internal dummy head. The MR bias current control loop is active so that the state of the C1 loop capacitor is near its Read mode operating point. The reader output remains in its Idle state (inactive).

Taking the $\overline{\text{BIAS}}$ pin high in Idle mode disables the MR bias current source and inactivates the MR bias control loop.

Sleep Mode

Setting the $\overline{\text{SLEEP}}$ bit low (register 4, bit <D0>) places the preamp in Sleep mode (see Table 114). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Table 114Mode Select

R/$\overline{W}$	*$\overline{\text{BIAS}}$*	*SERVO* [1]	*$\overline{\text{IDLE}}$ 4:<D1>*	*$\overline{\text{SLEEP}}$ 4:<D0>*	*MODE*
1	0	X	1	1	Read
1	1	X	1	1	Read Bias Dummy Head
0	1	0	1	1	Write
0	0	0	1	1	Write Bias MR Head
0	X	1	1	1	Servo
X	1	X	0	1	Idle
X	0	X	0	1	Idle Bias Dummy Head
X	X	X	X	0	Sleep

1. In this table, a "1" in the Servo column represents a combination of high levels on both the BANK0 and BANK1 bits in the serial register (register 2, bit <D7> and register 4, bit <D6>). (A "0" represents all other combinations of these two bits.)

Table 115Servo Mode Head Select

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*HEADS*
1	0	0	none [2]
1	0	1	1, 3, 5 and 7 [2]
1	1	0	2, 4, 6 and 8 [2]
1	1	1	all heads [2]

1. Not used
2. For the 4-channel version, all four heads are written whenever servo mode is selected; the head select bits are not used.

Table 116Head Select (non-servo)

HS2 [1] *1:<D2>*	*HS1 1:<D1>*	*HS0 1:<D0>*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

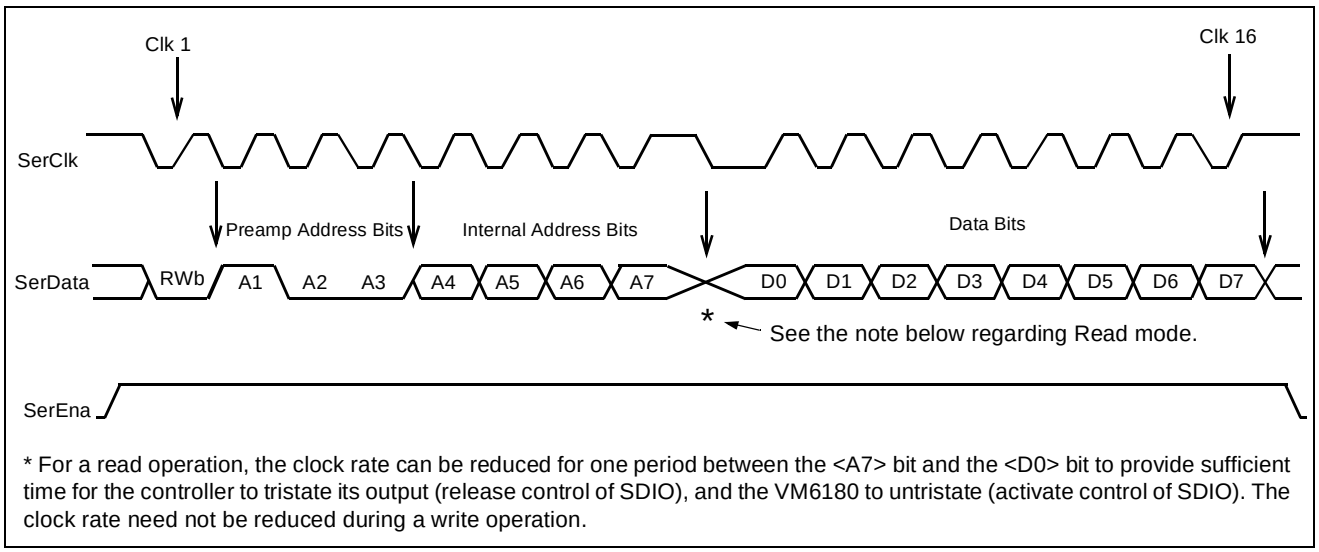
1. Not used on 4-channel device.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

PIN FUNCTION LIST AND DESCRIPTION

Symbol	*Input/Output* [1]	*Description*
R/$\overline{W}$	I	Read/Write: A TTL low level enables write mode. Pin defaults high (Read mode).
$\overline{BIAS}$	I	Bias Enable: A TTL low level enables MR bias current to the selected head (or to an internal dummy head in Idle and Read modes). Pin defaults high (Bias disabled).
$\overline{FAST}$ [2]	I	Fast Read Enable: A TTL low level enables Fast Read mode (regardless of the state of the FR serial bit or the thermal asperity detection circuitry). Pin defaults high (Fast disabled).
ABHV	I/O	Analog Buffered Head Voltage: The preamp drives this pin to an analog voltage representing five times the buffered head voltage.
FLT/DBHV	O	Fault/Digital Buffered Head Voltage: Setting the MRMEAS bit high (register 4, bit <D3>) allows the digital buffered head Voltage (DBHV) to be represented on the FLT/DBHV pin. Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin. • In Write mode, a CMOS high level indicates a fault. • In Read mode, a CMOS low level indicates a fault.
WDX, WDY	I	Differential Pseudo-ECL write data inputs
HR0P-HR7P	I	MR head connections, positive end
HW0X-HW7X	O	Thin-Film write head connections, positive end
HW0Y-HW7Y	O	Thin-Film write head connections, negative end
RDP, RDN	O	Read Data: Differential read signal outputs
C1	-	Compensation capacitor for the MR bias current loop
GND	-	Ground
VCC	-	+5.0V supply
RS		Reference Voltage for both MR Bias and Write Current (External 2kΩ resistor sets reference current for the read and write DACs.)
SENA	I	Serial Enable: Serial port enable signal; see Figures 82 and 83
SCLK	I	Serial Clock: Serial port enable signal; see Figures 82 and 83
SDIO	I/O	Serial Data: Serial port enable signal; see Figures 82 and 83

1. I = Input pin, O = Output pin
2. Pin available only on 8-channel device.



* For a read operation, the clock rate can be reduced for one period between the <A7> bit and the <D0> bit to provide sufficient time for the controller to tristate its output (release control of SDIO), and the VM6180 to untristate (activate control of SDIO). The clock rate need not be reduced during a write operation.

Figure 81 Serial Port Protocol

Table 117Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A4>*				*Preamp Address Bits <A3-A1>*	*R/W <A0>*
Vendor ID / Channel Count	0	1	0	0	0	001	1/0
Head Select / MR Bias Current DAC	1	1	0	0	1		1/0
Write Current DAC / Servo Bank	2	1	0	1	0		1/0
Thermal Asperity	3	1	0	1	1		1/0
Sleep / Idle / Gain	4	1	1	0	0		1/0

1. Reserved

Table 118Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Vendor ID / Channel Count	0	1,2	Channel [1,3]	1 [1]	0 [1]	1 [1]	0 [1]	1 [1]	0 [1]
Head Select / MR Bias Current DAC	1	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
Write Current DAC / Servo Bank	2	BANK0	[2]	[2]	IW4	IW3	IW2	IW1	IW0
Thermal Asperity	3	TA3	TA2	TA1	TA0	TADET	[2]	[2]	[2]
Sleep / Idle / Gain	4	[2]	BANK1	FAST	[2]	MRMEAS	GAIN	$\overline{\text{IDLE}}$	$\overline{\text{SLEEP}}$

1. Read Only
   Register 0:<D0-D2> is Vendor ID Code (VTC = 010).
   Register 0:<D3-D5> is Vendor Revision Code (e.g., Rev P = 101).
2. Reserved
3. 0 = 8 channel device, 1 = 4 channel device

Table 119Serial Interface Timing Parameters

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNITS
Serial Clock (SCLK) Rate		.001		40	MHz
SENA to SCLK delay	T_{sens}	30			ns
SDIO setup time	T_{ds}	5			ns
SDIO hold time	T_{dh}	5			ns
SCLK cycle time	T_{c}	25			ns
SCLK high time	T_{ckh}	20			ns
SCLK low time	T_{ckl}	20			ns
SENA hold time	T_{shld}	25			ns
Time between I/O operations	T_{sl}	50			ns
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			50	ns
Time to activate SDIO	T_{act}			50	ns
Duration of SerEna (read)	T_{rd}	905			ns
Duration of SerEna (write)	T_{wt}	855			ns

Note: SerEna assertion level is high.

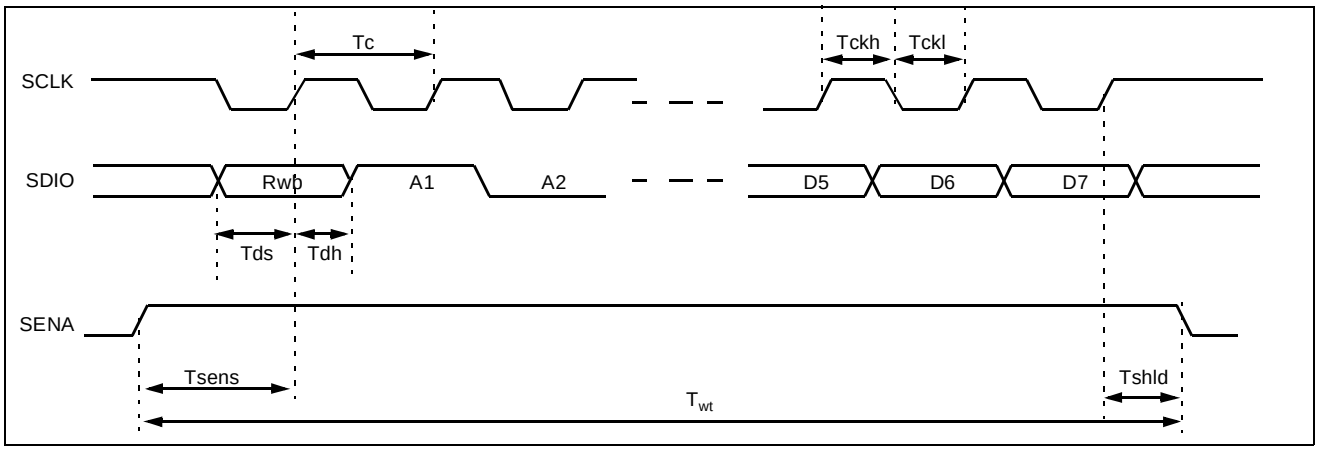


Figure 82 Serial Port Timing

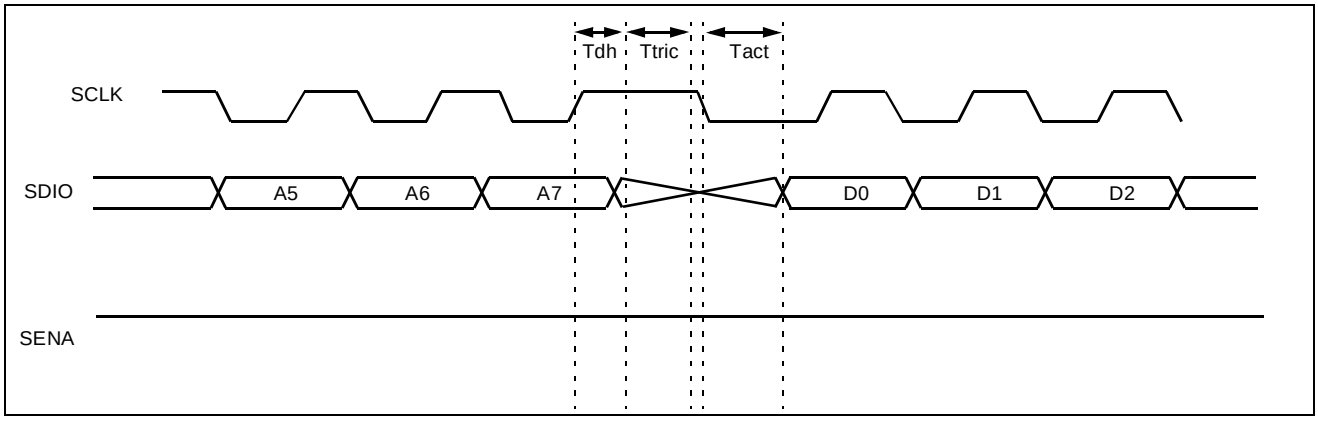


Figure 83 Serial Port Timing - Tristate Control

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 10mA		56	75	mA
		Write Mode, I_W = 25mA		56	75	
		Write Mode, I_W = 25mA, Bias enabled, I_{MR} = 10mA		75	110	
		Idle Mode, Bias disabled		8	20	
		Sleep Mode		2	9	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 4.5V		173	205	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 4.5V,		300	340	
Power Dissipation	P_d	Read Mode, I_{MR} = 10mA		280	412	mW
		Write Mode, I_W = 25mA		290	412	
		Write Mode, I_W = 25mA, Bias enabled, I_{MR} = 10mA		375	605	
		Idle Mode, Bias disabled		40	110	
		Sleep Mode		5	50	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 4.5V		780	923	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 4.5V,		1350	1530	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{IH} - 1.5		V_{IH} - 0.25	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Voltage	V_{OH}	FLT: I_{OH} = -400mA	3.6			V
Output Low Voltage	V_{OL}	FLT: I_{OL} = 400mA			0.5	V
V_{CC} Fault Threshold	V_{DTH}	I_w < 200mA	3.6	4.0	4.2	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		5	10	16	mA
MR Head Current Accuracy	ΔI_{MR}	5mA < I_{MR} < 16mA, R_{RS} = 2kΩ	-10		10	%
Unselected MR Head Current					100	µA
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Buffered Head Voltage Gain	A_{BHV}	Output Range = $A_{BHV} \cdot I_{MR} \cdot R_{MR}$ = 500mV to 2.5V; BHV Load Current = 0-150µA	4.5	5.0	5.5	V/V
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, R_L(RDP, RDN) = 1kΩ, I_{MR} = 10mA, R_{MR} = 33Ω, Gain bit = 0	160	200	240	V/V
		Gain bit = 1	240	300	360	
Passband Upper Frequency Limit	f_{HR}	R_{MR} = 33Ω; L_{MR} < 10nH; -3dB		150		MHz
Passband Lower -3dB Frequency Limit	f_{LR}	R_{MR} = 33Ω; C_1= 0.01µF		0.7	1	MHz
Equivalent Input Noise (sense amp only)	e_n	R_{MR} = 33Ω; I_{MR} = 10mA; 1 < f < 40 MHz		0.50		nV/√Hz
Bias Current Noise (referred to Input)	i_n	I_{MR} = 10mA		16		pA/√Hz
Equivalent Input Noise (total)	e_n	R_{MR} = 33Ω; I_{MR} = 10mA; 1 < f < 40 MHz		0.73		nV/√Hz
Input Resistance	R_{IN}	I_{MR} = 10mA		2.6		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz		5		mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or GND, I_{MR} = 10mA, R_{MR} = 33Ω, 1 < f < 100 MHz		45		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 1 < f < 100 MHz	45			dB
Output Offset Voltage	V_{OS}	I_{MR} = 10mA, R_{MR} = 33Ω	-200		200	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.9		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			300	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode			50	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	1.5			mA

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 150nH, R_H = 20Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current		30		ns
R/$\overline{W}$ to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value		500 [1]		ns
Idle to Read Mode	t_{CS}	RDP/RDN to within ±30mV of final value		12 [1]		µs
Sleep to Read Mode	t_{SR}	RDP/RDN to within ±30mV of final value		12 [1]		µs
Bias Disable to Enable, Read Mode	t_{BDE}	RDP/RDN to within ±30mV of final value		12		µs
HS0 - HS3 to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode		12	25	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.5	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		15	20	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time; L_H = 0; R_H = 0			0.5	ns
Rise/Fall Time	t_r / t_f	4 Channel: I_W = 30mA; L_H = 180nH; R_H = 15Ω; 10 - 90%		2.0	2.5	ns
		8 Channel: I_W = 30mA; L_H = 180nH; R_H = 15Ω; 10 - 90%		2.7	3.2	

1. $\overline{BIAS}$ pin active low for 25 µs preceding the R/$\overline{W}$ transition.

THERMAL ASPERITY CHARACTERISTICS

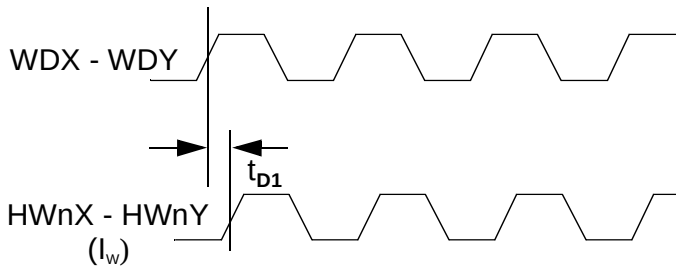
PARAMETER	*SPECIFICATION*
Thermal Asperity Detection Threshold	50[1 + DAC value (0-15)] ± 20%, output-referred
Thermal Asperity Detection Range	50mV - 800mV over baseline DC level in RDP/RDN (low frequency variation in baseline tracked by threshold)

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 150nH, R_H = 20Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(base to peak)	10		50	mA
Write Current Accuracy	ΔI_W	10mA < I_W < 50mA, R_{RS} = 2kΩ	-14		14	%
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V	6	7.5		V_{pp}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Resistance	R_O	Internal Damping [1]		600		Ω

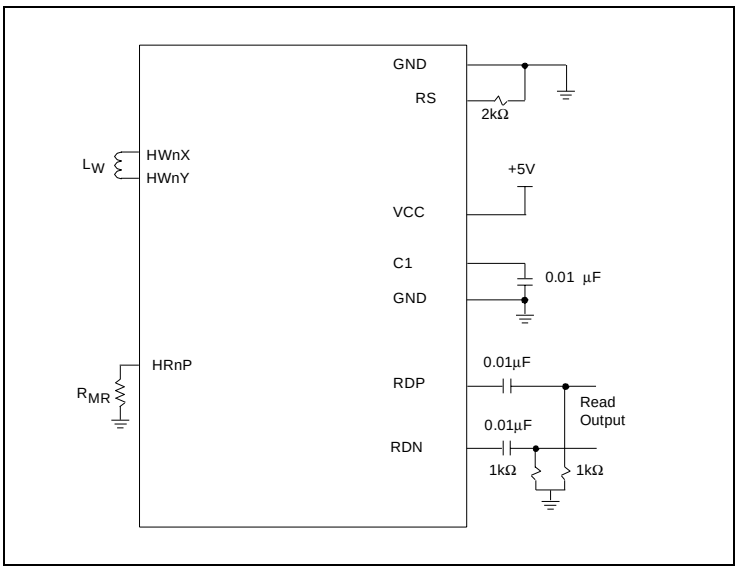
1. An 800 Ohm damping resistor is a metal option. Note that the damping resistance affects the write current equation; see (eq. 65)



Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

Figure 84 Write Mode Timing Diagram

TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Minimizing parasitics at the C1 node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the pins/pads as possible.
- C1 should connect to the same ground to which the read heads are connected.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins/pads:
  VCC - GND
- For maximum stability, place the decoupling capacitors and the R_{RS} resistor as close to the pins/pads as possible.

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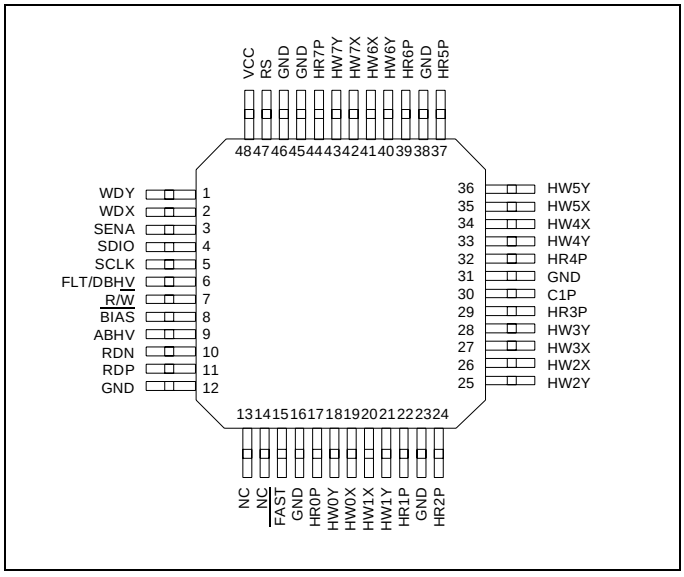
VM6180

8-CHANNEL CONNECTION DIAGRAM



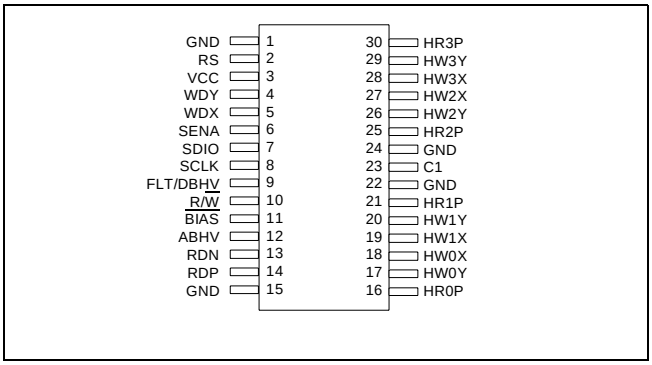
8-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

VM6180

4-CHANNEL CONNECTION DIAGRAM



4-Channel
30-lead TSSOP

Specific Characteristics

See the general data sheet for common specification information.

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VTC Inc.
Value The Customer™

VM6182 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface with Readback (Provides Programmable Bias Current, Gain, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Bandwidth = 150 MHz Min (R_{MR} = 45Ω, L_{MR} < 20nH)
  - Operates from a Single +5 Volt Power Supply
  - Fault Detection Capability
  - Available in 48-pin TQFP and 30-pin VSOP Packages
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 5 - 15.3 mA Range
  - Programmable Read Voltage Gain (200 V/V or 300 V/V Typical, R_{MR} = 45Ω)
  - Thermal Asperity Detection and Fast Recovery Compensation
  - Digital and Analog Buffered Head Voltage (BHV) Measurement Modes
  - Input Noise = 0.88 nV/√Hz Typical (R_{MR} = 45Ω, I_{MR} = 10mA)
  - Power Supply Rejection Ratio = 45 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, VM6182A3: 10 - 50 mA range (R_{DAMP} = 600Ω) VM6182A4: 9 - 45 mA range (R_{DAMP} = 140Ω)
  - Rise Time = 2.3 ns Typical (R_H = 15Ω, L_H = 180 nH, I_W = 30 mA) VM6182A3: 1.9 ns (R_{DAMP} = 600Ω) VM6182A4: 2.7 ns (R_{DAMP} = 140Ω)
  - Multi-Channel Servo Write

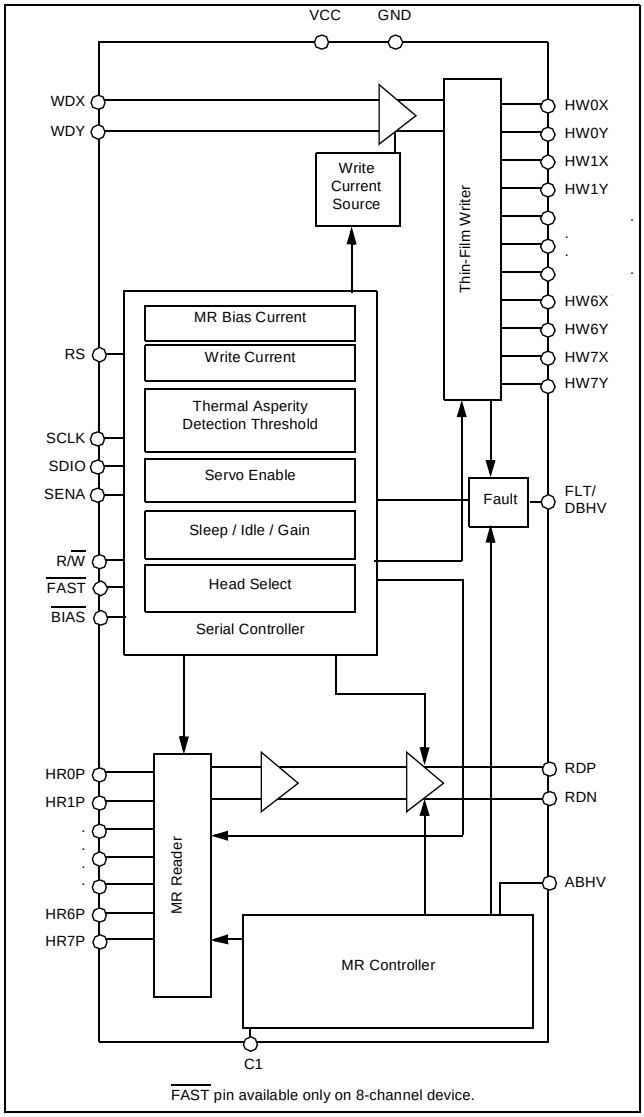
DESCRIPTION

The VM6182 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM6182 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM6182 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available in 4 and 8-channel options. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 30mA
Write Current, I_W 60mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -60°C TO 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 9.03 - 45.15 mA
Write Head Inductance, L_W ..... 10 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 5 - 15.3 mA
Read Head Inductance, L_{MR} ..... 10 - 100 nH
Read Head Resistance, R_{MR} ..... 15 - 55 Ω
Junction Temperature, T_J ..... 0°C to 125°C

Serial Interface Controller

The VM6182 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 123 and 124 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry. The bidirectional SDIO line supports full readback.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, three preamp select bits <A3-A1> (which must be <001> for this preamp), and four register address bits <A7-A4>. The second 8 bits <D7-D0> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register. During a read sequence, SDIO will begin outputting data on the falling edge of the 9th cycle. At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.

See Table 125 and Figures 88 and 89 for serial interface timing information.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM6182 uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{10}{R_{RS}} + 0.333(k_{IMR}) \qquad \textit{(eq. 66)}$$

I_{MR} represents the bias current flowing through the MR element (in mA).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

A "high" TTL level applied to the R/$\overline{W}$ pin and a "low" TTL level applied to the $\overline{BIAS}$ pin (along with the appropriate levels on the IDLE and SLEEP bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 120).

The output of the read preamp is differential.

Note: Transitions to Read mode from Sleep mode should always be made by first entering the Idle mode for a minimum of 20µs.

Read Bias Enable in Read Mode

Taking the $\overline{BIAS}$ pin low in read mode enables MR bias current to the selected head.

Taking the $\overline{BIAS}$ pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

The 5 bits in register 1 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 85 displays the reader output for an uncompensated thermal asperity event.)

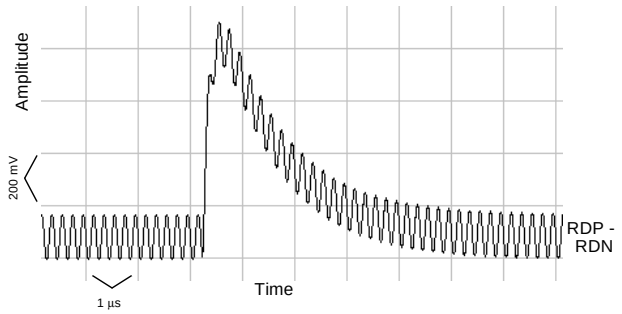


Figure 85 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM6182 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Setting the TADET bit high (register 3, bit <D3>) allows the TA detection circuitry to detect an asperity event (based on the programmable threshold) and report this as a fault condition on the fault line. Setting this bit low disables TA detection.

The threshold for thermal asperity detection has a range of 50 to 800 mV and is governed by the following equation:

$$V_{TADT} = 50(1 + k_{TADT}) \qquad \textit{(eq. 67)}$$

V_{TADT} represents the TA threshold (output-referred in mVpk; ±20%).
k_{TADT} represents the TA DAC setting (0-15).

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Fast Recovery Compensation

A Fast Recovery mode is initiated in two ways:

6) Setting the Fast Recovery (FR) bit high (register 4, bit <D5>) automatically initiates the Fast Recovery mode if a thermal asperity is detected.
(Note that the TA detection circuitry must be enabled with the TADET bit.)
7) Taking the $\overline{\text{FAST}}$ pin low (8-channel only). This overrides the FR serial bit and initiates the Fast Recovery mode regardless of the detection circuitry.

Note: This configuration makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the corner frequency movement.

When activated, Fast Recovery Compensation raises the nominal 700 KHz lower -3dB corner frequency to approximately 5 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 86).

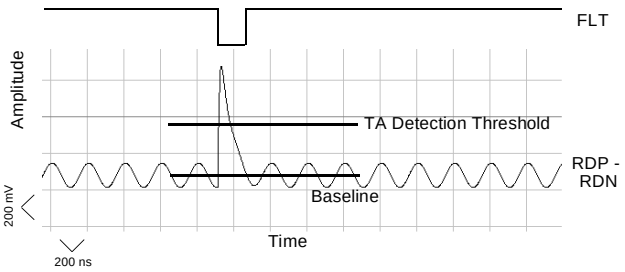

Figure 86 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the nominal 700 kHz lower -3dB corner frequency.

Analog Buffered Head Voltage (ABHV)

Setting the MRMEAS bit high (register 4, bit <D3>) allows an amplified representation of the MR bias voltage to be presented on the ABHV pin. This voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} \times R_{MR}) \qquad \textit{(eq. 68)}$$

If the MRMEAS bit is not set, the ABHV pin is high-Z.

Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (register 4, bit <D3>) allows the digital buffered head voltage (DBHV) to be represented on the FLT/DBHV pin.

The DBHV output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 360mV and 600mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Read Mode Fault Detection

Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the read mode, a low on the FLT line (CMOS with active pull-up) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- Thermal asperity detected (reported if enabled with the TADET bit (register 3, bit <D3>))
- HS2 bit (register 1, bit <D2>) selected (4-channel only)

An MR open head fault condition is detected but not reported on the FLT line. The voltage on the loop-compensation capacitor (C1) is clamped to provide MR open head protection (until another head is selected or a mode change is initiated).

Note: A dwell time of not less than 25µs should be provided to allow the clamping circuitry sufficient time to settle to a safe voltage before switching heads.

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the write current magnitude:

$$I_W = \left(\frac{20}{R_{RS}} + 1.29(k_{IW})\right)\left(\frac{1}{1 + \frac{R_H}{R_D}}\right) \qquad \textit{(eq. 69)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).
R_H represents the series head resistance (in Ω).
R_D represents the damping resistance (in Ω).
k_{IW} represents the write current DAC setting (0 to 31).

A “low” TTL level applied to R/$\overline{\text{W}}$ (along with the appropriate levels on the IDLE and SLEEP bits) places the preamp in the write mode (see Table 120). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 90.

Write Current DAC

The 5 bits in register 2 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enable in Write Mode

Taking the $\overline{\text{BIAS}}$ pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the $\overline{\text{BIAS}}$ pin high in write mode disables the MR bias current source and inactivates the MR bias control loop.

Write Mode Fault Detection

Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the write mode, a high on the FLT line (CMOS with active pull-up) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Write head shorted to ground
- HS2 bit (register 1, bit <D2>) selected (4-channel only)

A low supply fault condition is detected but not reported on the FLT line. The write current source internal to the chip is shutdown and no current flows to any head.

Servo Write Mode

In the servo write mode, four channels or all channels of the VM6182 are written simultaneously.

Setting both the BANK0 and BANK1 bits (register 2, bit <D7> and register 4, bit <D6>) to "1" (along with appropriate levels on the R/W pin and IDLE and SLEEP bits) places the preamp in servo write mode (see Table 120). The HS0 - HS2 register bits (1:<D2-D0>) determine which heads are written (see Table 121).

(For the 4-channel version, all four heads are written whenever servo mode is selected; the head select bits are not used.)

Write mode fault circuits are disabled.

Note: It is the customer's responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Idle Mode

Setting the IDLE bit low (register 4, bit <D1>) places the preamp in Idle mode (see Table 120). The state of the $\overline{BIAS}$ pin determines the state of the MR bias current source.

Read Bias Enable

Taking the $\overline{BIAS}$ pin low in Idle mode activates the MR bias current source and directs the MR bias current to an internal dummy head. The MR bias current control loop is active so that the state of the C1 loop capacitor is near its Read mode operating point. The reader output remains in its Idle state (inactive).

Taking the $\overline{BIAS}$ pin high in Idle mode disables the MR bias current source and inactivates the MR bias control loop.

Sleep Mode

Setting the SLEEP bit low (register 4, bit <D0>) places the preamp in Sleep mode (see Table 120). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Note: Transitions from Sleep mode to Read mode should always be made by first entering the Idle mode for a minimum of 20µs.

Table 120Mode Select

R/$\overline{W}$	*$\overline{BIAS}$*	*Servo* [1]	*Idle 4:<D1>*	*Sleep 4:<D0>*	*Mode*
1	1	X	1	1	Read Bias Active (dummy head)
1	0	X	1	1	Read Bias Active
0	1	0	1	1	Write
0	0	0	1	1	Write Bias Active
0	X	1	1	1	Servo
X	1	X	0	1	Idle
X	0	X	0	1	Idle Bias Active (dummy head)
X	X	X	X	0	Sleep

1. In this table, a "1" in the Servo column represents a combination of high levels on both the BANK0 and BANK1 bits in the serial register (register 2, bit <D7> and register 4, bit <D6>). (A "0" represents all other combinations of these two bits.)

Table 121Servo Mode Head Select

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*Heads*
[1]	0	0	none [2]
[1]	0	1	4, 5, 6 and 7 [2]
[1]	1	0	0, 1, 2 and 3 [2]
[1]	1	1	all heads [2]

1. Not used
2. For the 4-channel version, all four heads are written whenever servo mode is selected; the head select bits are not used.

Table 122Head Select (non-servo)

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*Head*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1 [1]	0	0	4
1 [1]	0	1	5
1 [1]	1	0	6
1 [1]	1	1	7

1. For the 4-channel version, the fault line is activated and the I_{MR}/Write current is diverted to a dummy head.

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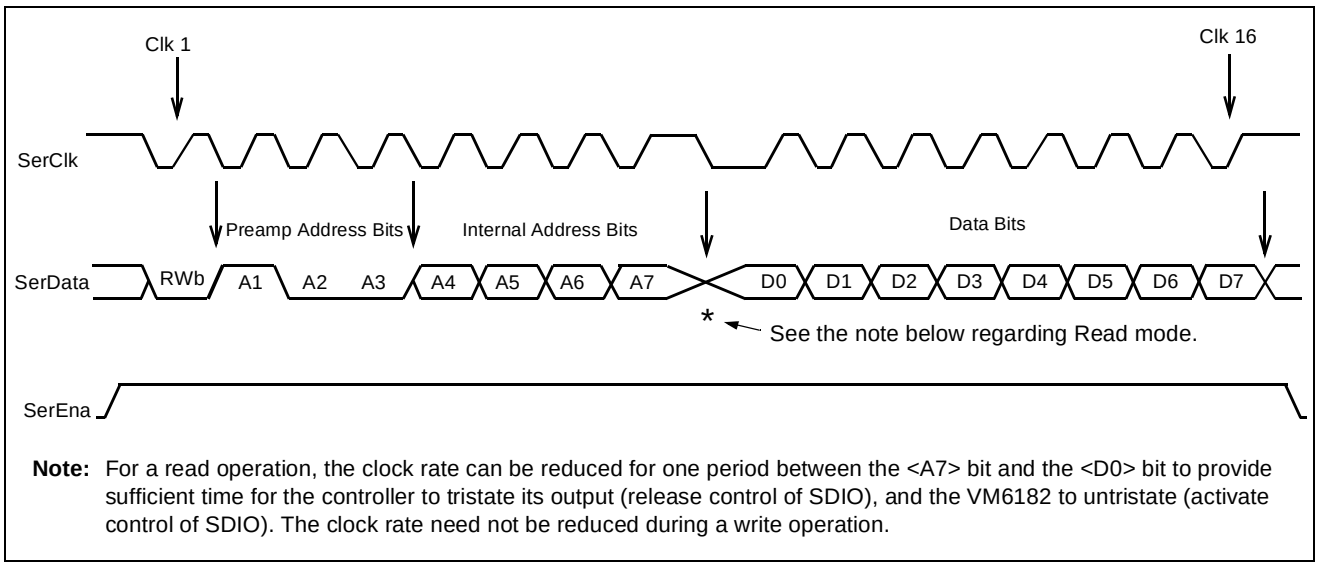
PIN FUNCTION LIST AND DESCRIPTION

Symbol	*Input/Output* [1]	*Description*
R/$\overline{W}$	I	Read/Write: A TTL low level enables write mode. Pin defaults high (read mode).
$\overline{BIAS}$	I	Bias Enable: A TTL low level enables MR bias current to the selected head (or to an internal dummy head in Idle and Read modes). Pin defaults high (bias disabled).
$\overline{FAST}$ [2]	I	Fast Read Enable: A TTL low level enables Fast Read mode (regardless of the state of the FR serial bit or the thermal asperity detection circuitry). Pin defaults high (Fast Read mode disabled).
ABHV	I/O	Analog Buffered Head Voltage: The preamp drives this pin to an analog voltage representing five times the buffered head voltage.
FLT/DBHV	O	Fault/Digital Buffered Head Voltage: Setting the MRMEAS bit high (register 4, bit <D3>) allows the digital buffered head Voltage (DBHV) to be represented on the FLT/DBHV pin. Setting the MRMEAS bit low (register 4, bit <D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin. • In Write mode, a CMOS high level indicates a fault. • In Read mode, a CMOS low level indicates a fault.
WDX, WDY	I	Differential Pseudo-ECL write data inputs
HR0P-HR7P	I	MR head connections, positive end
HW0X-HW7X	O	Thin-Film write head connections, positive end
HW0Y-HW7Y	O	Thin-Film write head connections, negative end
RDP, RDN	O	Read Data: Differential read signal outputs
C1	-	Compensation capacitor for the MR bias current loop
GND	-	Ground
VCC	-	+5.0V supply
RS		Reference Voltage for both MR Bias and Write Current (External 2kΩ resistor sets reference current for the read and write DACs.)
SENA	I	Serial Enable: Serial port enable signal; see Figures 88 and 89
SCLK	I	Serial Clock: Serial port enable signal; see Figures 88 and 89
SDIO	I/O	Serial Data: Serial port enable signal; see Figures 88 and 89

1. I = Input pin, O = Output pin
2. Pin available only on 8-channel device.



Note: For a read operation, the clock rate can be reduced for one period between the <A7> bit and the <D0> bit to provide sufficient time for the controller to tristate its output (release control of SDIO), and the VM6182 to untristate (activate control of SDIO). The clock rate need not be reduced during a write operation.

Figure 87 Serial Port Protocol

Table 123Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A4>*				*Preamp Address Bits <A3-A1>*	*R/$\overline{W}$ <A0>*
Vendor ID / Channel Count	0	1	0	0	0	001	1/0
Head Select / MR Bias Current DAC	1	1	0	0	1		1/0
Write Current DAC / Servo Bank	2	1	0	1	0		1/0
Thermal Asperity	3	1	0	1	1		1/0
Sleep / Idle / Gain	4	1	1	0	0		1/0

1. Reserved

Table 124Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Vendor ID / Channel Count	0	0 [1]	Channel [1,2]	0 [1]	1 [1]	1 [1]	0 [1]	1 [1]	0 [1]
Head Select / MR Bias Current DAC	1	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
Write Current DAC / Servo Bank	2	BANK0	[3]	[3]	IW4	IW3	IW2	IW1	IW0
Thermal Asperity	3	TA3	TA2	TA1	TA0	TADET	[3]	[3]	[3]
Sleep / Idle / Gain	4	[3]	BANK1	FR	[3]	MRMEAS	GAIN	IDLE	SLEEP

1. Read Only
   Register 0:<D0-D2> is Vendor ID code (VTC = 010)
   Register 0:<D3-D5> is Vendor revision code (VM6182A3 = 001, VM6182A4 = 011)
2. 0 = 8 channel device, 1 = 4 channel device
3. Reserved

Table 125Serial Interface Timing Parameters

Description	*Symbol*	*Min*	*Nom*	*Max*	*Units*
Serial Clock (SCLK) Rate		.001		40	MHz
SENA to SCLK delay	T_{sens}	30			ns
SDIO setup time	T_{ds}	5			ns
SDIO hold time	T_{dh}	5			ns
SCLK cycle time	T_{c}	25			ns
SCLK high time	T_{ckh}	20			ns
SCLK low time	T_{ckl}	20			ns
SENA hold time	T_{shld}	25			ns
Time between I/O operations	T_{sl}	50			ns
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			50	ns
Time to activate SDIO	T_{act}			50	ns
Duration of SerEna (read)	T_{rd}	905			ns
Duration of SerEna (write)	T_{wt}	855			ns

Note: SerEna assertion level is high.

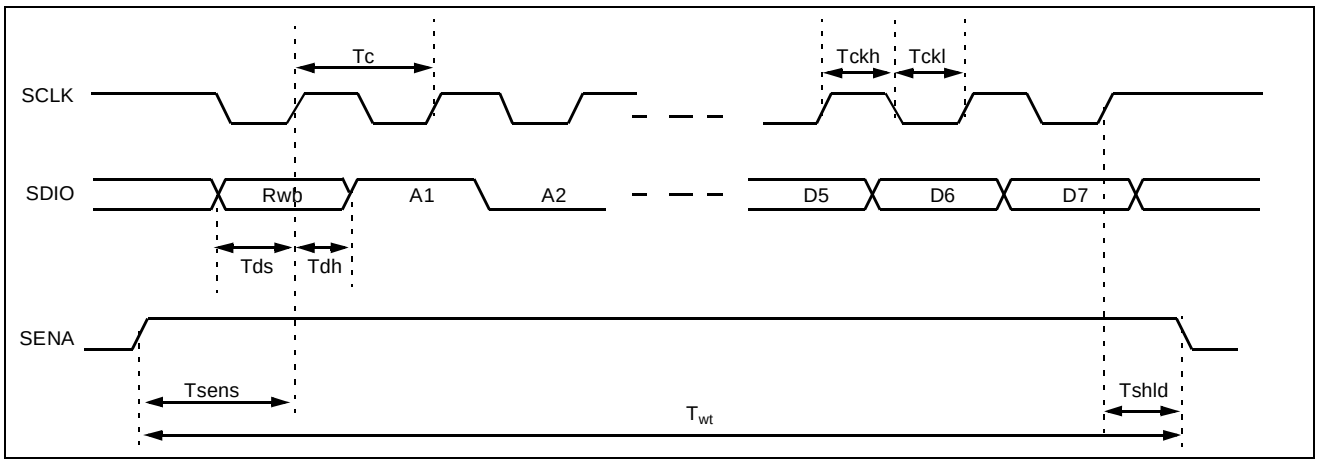


Figure 88 Serial Port Timing

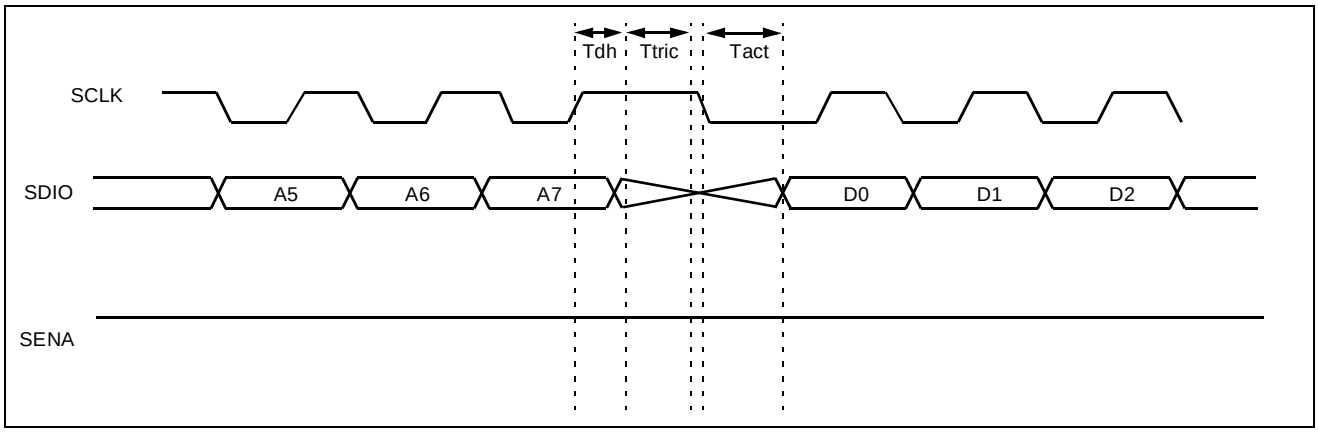


Figure 89 Serial Port Timing - Tristate Control

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 10mA		56	75	mA
		Write Mode, I_W = 25mA, Bias disabled		58	75	
		Write Mode, I_W = 25mA, Bias enabled, I_{MR} = 10mA		83	110	
		Idle Mode, Bias disabled		8	16	
		Sleep Mode		3.5	10	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 4.5V		160	190	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 4.5Vs		320	360	
Power Dissipation	P_d	Read Mode, I_{MR} = 10mA		280	412	mW
		Write Mode, I_W = 25mA, Bias disabled		290	412	
		Write Mode, I_W = 25mA, Bias enabled, I_{MR} = 10mA		415	605	
		Idle Mode, Bias disabled		40	80	
		Sleep Mode		17.5	50	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 4.5V		800	950	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 4.5Vs		1600	1800	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{IH} - 1.5		V_{IH} - 0.25	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			100	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Voltage	V_{OH}	FLT: I_{OH} = -400µA	3.6			V
Output Low Voltage	V_{OL}	FLT: I_{OL} = 400µA			0.4	V
V_{CC} Fault Threshold	V_{DTH}	I_w < 200µA	3.6	4.0	4.2	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
MR Head Current Range	I_{MR}		5	10	15.3	mA
MR Head Current Accuracy	ΔI_{MR}	5mA < I_{MR} < 15.3mA, R_{RS} = 2kΩ	-10		10	%
Unselected MR Head Current					100	µA
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ	1.9	2.0	2.1	V
Buffered Head Voltage Gain	A_{BHV}	Output Range = $A_{BHV} \cdot I_{MR} \cdot R_{MR}$ = 500mV to 2.5V; BHV Load Current = 0-150µA	4.5	5.0	5.5	V/V
MR Head Measurement Threshold (Head Resistance / DBHV)		Low Threshold	334	360	385	mV
		High Threshold	558	600	642	
Differential Voltage Gain	A_V	V_{IN} = 1mV$_{pp}$ @10MHz, R_L(RDP, RDN) = 1kΩ, I_{MR} = 10mA, R_{MR} = 45Ω applies to the following:				V/V
		4-Channel VM6182A3: Gain bit = 0	183	229	275	
		4-Channel VM6182A3: Gain bit = 1	269	337	404	
		4-Channel VM6182A4: Gain bit = 0	167	209	250	
		4-Channel VM6182A4: Gain bit = 1	252	315	378	
		8-Channel VM6182A3: Gain bit = 0	179	223	268	
		8-Channel VM6182A3: Gain bit = 1	269	337	404	
		8-Channel VM6182A4: Gain bit = 0	158	198	237	
		8-Channel VM6182A4: Gain bit = 1	236	295	354	
Passband Upper Frequency Limit	f_{HR}	R_{MR} = 45Ω, L_{MR} < 20nH, -3dB	150	200		MHz
Passband Lower -3dB Frequency Limit	f_{LR}	R_{MR} = 45Ω, C_1= 0.01µF		0.7	1	MHz
Equivalent Input Noise (sense amp only)	e_n	R_{MR} = 45Ω, I_{MR} = 10mA, 1 < f < 40 MHz		0.50		$nV/\sqrt{Hz}$
Bias Current Noise (referred to Input)	i_n	I_{MR} = 10mA		16		$pA/\sqrt{Hz}$
Equivalent Input Noise (total integrated)	e_n	R_{MR} = 45Ω, I_{MR} = 10mA, 1 < f < 50 MHz		0.88	1.0	$nV/\sqrt{Hz}$
Input Resistance	R_{IN}	I_{MR} = 10mA		2.6		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV$_{pp}$ @ f = 5 MHz, Gain bit = 1	3	5		mV$_{pp}$
Power Supply Rejection Ratio	PSRR	100mV$_{pp}$ on V_{CC} or GND, I_{MR} = 10mA, R_{MR} = 45Ω, 1 < f < 100 MHz, input referred		45		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV$_{pp}$, 1 < f < 100 MHz	45			dB

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

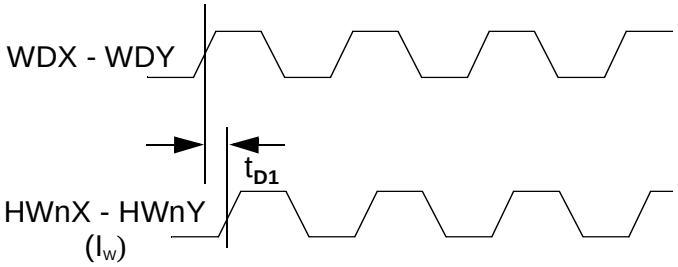
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Offset Voltage	V_{OS}	I_{MR} = 10mA, R_{MR} = 45Ω	-200		200	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.9		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			300	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode	23	28	36	W
Output Current	I_O	AC Coupled Load, RDP to RDN	1.5			mA

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 150nH, R_H = 15Ω, f_{DATA} = 5MHz.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Write Current Range	I_W	VM6182A3: base to peak, R_{DAMP} = 600Ω	10		50	mA
		VM6182A4: base to peak, R_{DAMP} = 140Ω	9		45	
Write Current Accuracy	ΔI_W	9.03mA < I_W < 45.15mA, R_{DAMP} = 140Ω	-15		15	%
Servo Write Current Accuracy	ΔI_{WS}	I_W = 25mA	-8		24	%
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ	1.9	2.0	2.1	V
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V	6	7.5		V_{pp}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Resistance	R_O	VM6182A3: Internal Damping [1]		600		Ω
		VM6182A4: Internal Damping [1]		140		

1. Damping resistance modifies the write current delivered to the head; see the write current equation on page 295.



Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

Figure 90 Write Mode Timing Diagram

THERMAL ASPERITY CHARACTERISTICS

Parameter	*Specification*
Thermal Asperity Detection Threshold	50[1 + DAC value (0-15)] ± 20%, output-referred
Thermal Asperity Detection Range	50mV - 800mV over baseline DC level in RDP/RDN (low frequency variation in baseline tracked by threshold)

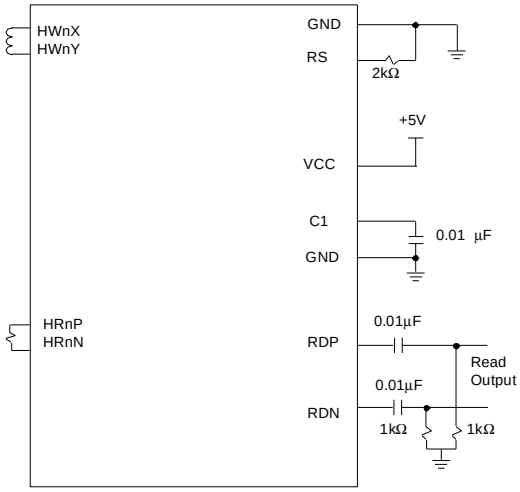
SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 150nH, R_H = 15Ω, f_{DATA} = 5MHz, I_{MR} = 10mA.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current		30		ns
R/$\overline{W}$ to Read Mode	t_{WR}	VM6182A3: RDP/RDN to within ±30mV of final value		1000 [1]		ns
		VM6182A4: RDP/RDN to within ±30mV of final value		700 [1]		
Idle to Read Mode	t_{CS}	RDP/RDN to within ±30mV of final value, I_{MR} = 10mA		22 [1]	30	µs
Sleep to Read Mode	t_{SR}	RDP/RDN to within ±30mV of final value, I_{MR} = 10mA		22 [1]		µs
Bias Disable to Enable, Read Mode	t_{BDE}	RDP/RDN to within ±30mV of final value, I_{MR} = 10mA		25	30	µs
HS0 - HS3 to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode, I_{MR} = 10mA		10	25	µs
Read or Write to Idle	t_{RI}	To 10% of read envelope or write current			0.5	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		15	20	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time; L_H = 0; R_H = 0			0.5	ns
Rise/Fall Time	t_r / t_f	VM6182A3: 10 - 90%, R_{DAMP} = 600Ω		1.9	2.7	ns
		VM6182A4: 10 - 90%, R_{DAMP} = 140Ω		2.7	3.0	

1. $\overline{BIAS}$ pin active low for 25 µs preceding the R/$\overline{W}$ transition.

TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Minimizing parasitics at the C1 node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the pins/pads as possible.
- C1 should connect to the same ground to which the read heads are connected.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins/pads:
  VCC - GND
- For maximum stability, place the decoupling capacitors and the R_{RS} resistor as close to the pins/pads as possible.

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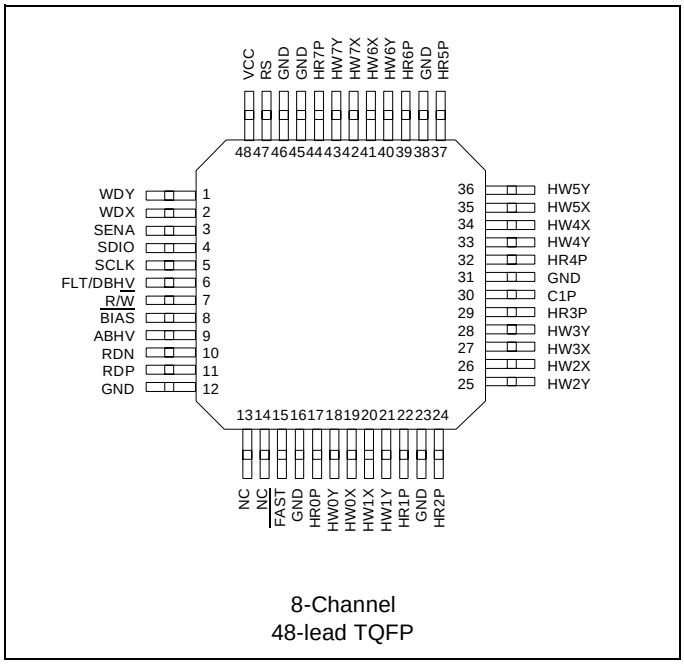
VM6182

8-CHANNEL CONNECTION DIAGRAM



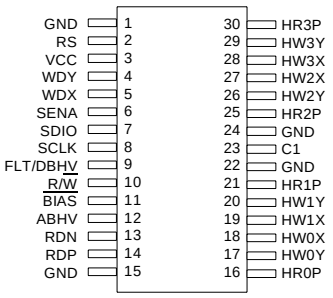
8-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

VM6182

4-CHANNEL CONNECTION DIAGRAM



4-Channel
30-lead VSOP

Specific Characteristics

See the general data sheet for common specification information.

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VTC Inc.
Value The Customer™

VM6184 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/ WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface with Readback (Provides Programmable Bias Current, Write Current, Write Damping Resistance, Head Selection, Read Gain, Thermal Asperity, and Servo Operation)
  - Bandwidth = 160 MHz Min (R_{MR} = 50Ω, L_{MR} = 0nH)
  - Operates from a Single +5 Volt Power Supply
  - Fault Detection Capability
  - Available as a 4- or 8-Channel Device
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 4.25 - 13.55 mA Range
  - Four Programmable Read Voltage Gains (100 V/V TO 200 V/V in 2dB steps, R_{MR} = 50Ω)
  - Thermal Asperity Detection and Fast Recovery Compensation
  - Digital and Analog Buffered Head Voltage (BHV) Measurement Modes
  - Input Noise = 1 nV/$\sqrt{Hz}$ Typical (R_{MR} = 50Ω, I_{MR} = 8.75mA)
  - Power Supply Rejection Ratio = 45 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 45 mA Range
  - Rise Time = 1.7 ns typical (R_H - 16Ω, L_H = 130 nH, R_D = 670Ω, I_W = 30 mA)
  - Multi-Channel Servo Write
  - 3V CMOS or 5V TTL compatible Write Data Inputs

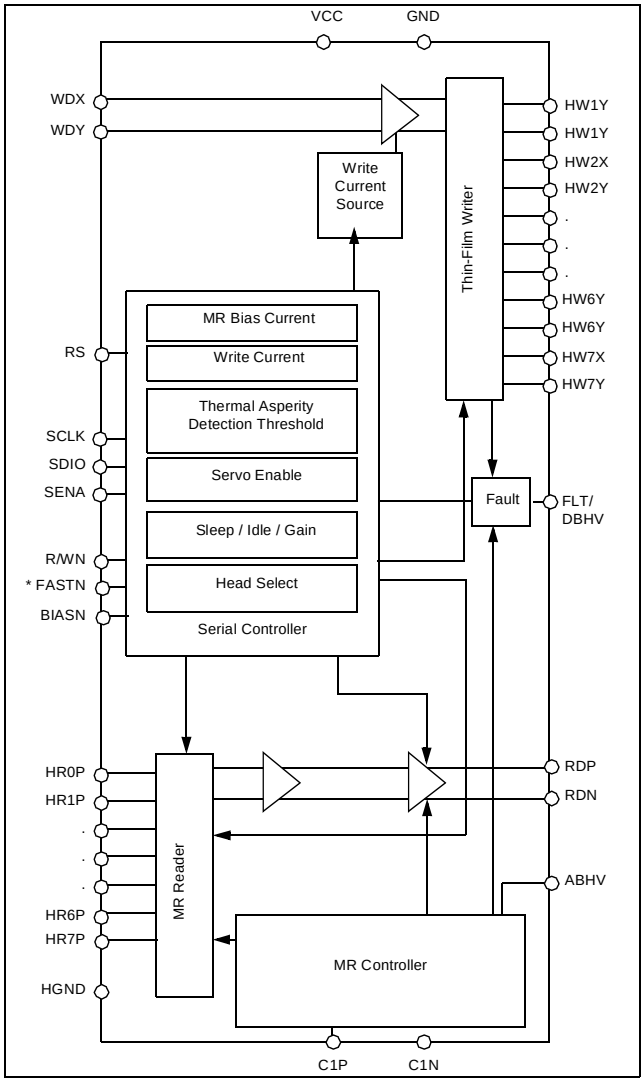
DESCRIPTION

The VM6184 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM6184 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM6184 is achieved through a 3-line, 16-bit serial interface. Programmable parameters include MR bias current, write current, head selection, damping resistance, reader gain, thermal asperity detection threshold and servo operation.

Available in 4- and 8-channel options. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



* This pin available only on 8-Channel device

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Read Bias Current, I_{MR} 16mA
Write Current, I_W 55mA
Input Voltages:
Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
Output Current:
RDP, RDN: I_O ..... -10mA
Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65°C TO 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 10 - 45 mA
Write Head Inductance, L_W ..... 85 - 180 nH
Write Head Resistance, R_W ..... 7 - 21 Ω
Read Bias Current, I_{MR} ..... 4.25 - 13.55 mA
Read Head Inductance, L_{MR} ..... 0 - 100 nH
Read Head Resistance, R_{MR} ..... 40 - 65 Ω
Junction Temperature, T_J ..... 0°C to 125°C

OPERATING MODES AND CONTROLS

Serial Interface Controller

The VM6184 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 131 and 132 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry. The bidirectional SDIO line supports full readback.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, three preamp select bits <A3-A1> (which must be <001> for this preamp), and four register address bits <A7-A4>. The second 8 bits <D7-D0> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register. During a read sequence, SDIO will begin outputting data on the falling edge of the 9th cycle. At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and may result in reader performance degradation.

See Table 134 and Figures 94 and 95 for serial interface timing information.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier that senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM6184 uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{8.5}{R_{RS}} + 0.3(k_{IMR}) \qquad \textit{(eq. 70)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).

R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).

k_{IMR} represents the MR bias DAC setting (0 to 31).

A "high" TTL level applied to the R/WN pin and a "low" TTL level applied to the BIASN pin (along with the "high" levels on the IDLEN and SLEEPN serial register bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 128).

The output of the read preamp is differential.

Read Bias Enable in Read Mode

Taking the BIASN pin low in read mode enables MR bias current to the selected head.

Taking the BIASN pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

The 5 bits in register 1 (1:<D3-D7>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 91 displays the reader output for an uncompensated thermal asperity event.)

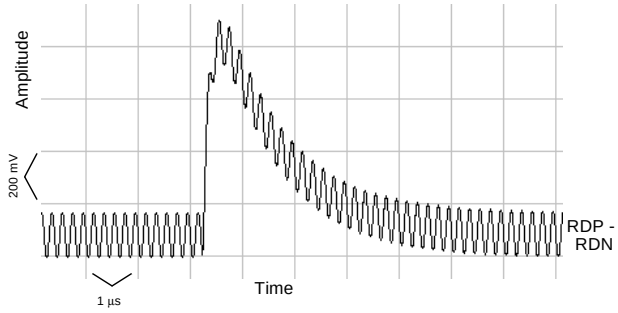


Figure 91 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM6184 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Setting the TADET bit high (3:<D3> = 1) allows the TA detection circuitry to detect an asperity event (based on the programmable threshold) and report this as a fault condition on the fault line. Setting this bit low disables TA detection.

The threshold for thermal asperity detection has a range of 50 to 800 mV and is governed by the following equation:

$$V_{TADT} = 50(1 + k_{TADT}) \qquad \textit{(eq. 71)}$$

V_{TADT} represents the TA threshold (output-referred in mVpk; ±15%).

k_{TADT} represents the TA DAC setting (0-15).

Fast Recovery Compensation

A Fast Recovery mode is initiated in three ways:
(See Table 129 for a diagram of the modes)

8) Setting the Fast Recovery (FR) bit high (4:<D5> = 1).

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9) If both the FR and TADET (3:<D3>) bits are high, a thermal asperity will initiate fast mode.
Note: The thermal asperity must be positive.

10) Taking the FASTN pin low (8 channel only). This overrides the FR serial bit and initiates the Fast Recovery mode regardless of the detection circuitry.

Note: This configuration makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the corner frequency movement.

When activated, Fast Recovery Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 5 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 92).

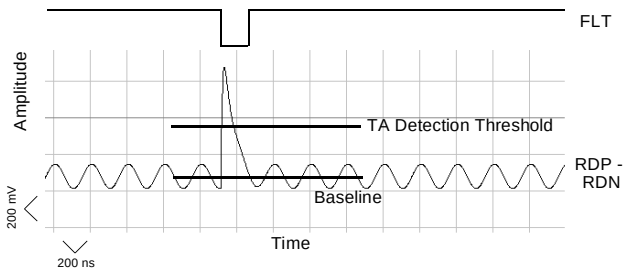

Figure 92 TA Detection and Compensation

Analog Buffered Head Voltage (ABHV)

Setting the MRMEAS bit high (4:<D4>) allows an amplified representation of the MR bias voltage to be presented on the ABHV pin. This voltage is defined by the equation:

$$V_{BHV} = ABHV(I_{MR} \times R_{MR}) + V_{BOS} \qquad \textit{(eq. 72)}$$

ABHV (Analog Buffered Head Voltage Gain) = 5 V/V Typical.
I_{MR} represents the bias current flowing to the MR element (in mA).
V_{BOS} represents the Output Offset Voltage.

If the MRMEAS bit is set low, the ABHV pin goes into a high impedance state.

Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (4:<D4>) allows the digital buffered head voltage (DBHV) to be represented on the FLT/DBHV pin.

The DBHV output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 347mV and 614mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Fault Detection

Setting the MRMEAS bit low (4:<D4>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the read mode, a low on the FLT line (open collector) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- Thermal asperity detected (reported when enabled with the TADET bit (3:<D3> = 1))
- Open MR head

Note: An MR open head fault condition is detected but not reported on the FLT line for 4 to 6 µs. The voltage on the loop-compensation capacitor (C1) is clamped to provide MR open head protection (until another head is selected or a mode change is initiated).

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the write current magnitude:

$$I_W = \left(\frac{20}{R_{RS}} + [1.13 \cdot k_{IW}]\right)\left(\frac{1}{1 + \frac{R_H}{R_D}}\right) \qquad \textit{(eq. 73)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 31).
R_D represents the damping resistance (in Ω).
R_H represents the series head resistance (in Ω).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ)

A “low” TTL level applied to R/WN (along with “high” levels on the IDLEN and SLEEPN serial register bits) places the preamp in the write mode (see Table 128). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 96.

Write Current DAC

The 5 bits (2:<D0-D4>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Write Current Damping

The 2 bits (3:<D1-D2>) represent the programmable damping resistance. The settings are defined in Table 126. The default setting is 670W.

Table 126Write Current Damping Resistance

DR1 3:<D2>	*DR0 3:<D1>*	*Resistance*	*Rise/Fall Time [1]*	*Overshoot*
0	0	670Ω	1.7 ns	30%
0	1	260Ω	1.8 ns	22%
1	0	160Ω	1.9 ns	16%
1	1	120Ω	2.1 ns	10%

1. I_W = 30mA, L_h = 130nH, R_h = 16Ω

Read Bias Enable in Write Mode

Taking the BIASN pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the BIASN pin high in write mode shuts down the reader.

Write Current Boost

Setting Write Current Boost (WCB) bit high (2:<D6>) increases the overshoot from 30% (R_D=670Ω) to 45%.

Fault Detection

Setting the MRMEAS bit low (4:<D4>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the write mode, a high on the FLT line (open collector) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Low power supply voltage (write current disabled)
- Write head shorted to ground
- Low write data frequency

If a low power supply fault condition is detected, the write current source internal to the chip is shutdown and no current flows to any head for the duration of the fault.

Servo Write Mode

In the servo write mode all channels of the VM6184 may be written simultaneously.

Setting both the BANK0 and BANK1 bits (2:<D7> and 4:<D6>) to “1” (along with appropriate levels on the R/WN pin and IDLEN and SLEEPN serial register bits) places the preamp in servo write mode (see Tables 127 and 128). Setting the HS0 - HS1 register bits (1:<D0-D1>) to “1” initiates a servo write to all heads (see Table 127). A combination of “0” and “1” on the HS0-HS1 bits initiates a 4 head bank servo operation for the 8-channel device (see Table 127). All write mode fault circuits are disabled, except for low power supply voltage.

Note: It is the customer’s responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Table 127Servo Mode Head Select

BANK1 4:<D6>	BANK0 2:<D7>	HS1 1:<D1>	HS0 1:<D0>	Heads	
				4-Channel	8-Channel
0	0	X	X	Normal Operation	
0	1	X	X	Normal Operation	
1	0	X	X	Normal Operation	
1	1	0	0	N/A [1]	N/A [1]
1	1	0	1	N/A [1]	N/A [1]
1	1	1	0	N/A [1]	N/A [1]
1	1	1	1	0-3 (All Heads)	0-7 (All Heads)

1. N/A = No head current and no faults reported.

Fault Detection

Setting the MRMEAS bit low (4:<D4> = 0) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the servo write mode, a high on the FLT line (open collector) indicates a fault condition. The fault condition is triggered by the following condition:

- Low power supply voltage (write current disabled)

Idle Mode

Setting the IDLEN bit low (4:D1> = 0) places the preamp in idle mode (see Table 128). The state of the BIASN pin determines the state of the MR bias current source.

Bias Enable

Taking the BIASN pin low in idle mode activates the MR bias current source. The MR bias current control loop is activated so that the state of the C1 loop capacitor remains near its Read mode operating point, but the reader output remains in its idle state (inactive).

Taking the BIASN pin high in idle mode disables the MR bias current source and inactivates the MR bias control loop.

Sleep Mode

Setting the SLEEPN bit low (4:<D0> = 0) places the preamp in Sleep mode (see Table 128). All circuits are inactivated to minimize power dissipation. Only the serial register remains active.

Table 128Mode Select

Servo [1]	BIASN	R/WN	IDLEN 4:<D1>	SLEEPN 4:<D0>	Mode
X	X	X	X	0	Sleep
X	1	X	0	1	Idle
X	0	X	0	1	Idle Bias Active (dummy head)
X	0	1	1	1	Read Bias Active
X	1	1	1	1	Read Bias Inactive (dummy head)
0	0	0	1	1	Write Bias Active
0	1	0	1	1	Write Bias Inactive
1	X	0	1	1	Servo

1. In this table, a “1” in the Servo column represents a combination of high levels on the BANK0 and BANK1 bits in the serial register (2:<D7> and 4:<D6>). A “0” represents all other combinations of those two bits.

Table 129Thermal Asperity Mode Control

FR 4:<D5>	TADET 3:<D3>	FASTN [1]	Mode Control	
			Fast Recovery	TA Detection
X	X	0	On	Off/On
0	0	1	Off	Off
0	1	1	Off	On
1	0	1	On	Off
1	1	1	TA Detection triggers Fast Recovery	

1. This pin available only on 8-channel device.

Table 130Head Select (non-servo)

HS2 1:<D2>	HS1 1:<D1>	HS0 1:<D0>	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1 [1]	0	0	4
1 [1]	0	1	5
1 [1]	1	0	6
1 [1]	1	1	7

1. Valid for 8-channel device only (see Fault Detection on page 309).

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PIN FUNCTION LIST AND DESCRIPTION

Signal	*Input/ Output* [1]	*Description*
R/WN	I	Read/Write: A TTL low level enables write mode. Pin defaults high with 20kΩ pullup resistor (read mode).
BIASN	I	Bias Enable: A TTL low level enables MR bias current to the selected head (or to an internal dummy head in idle mode). Pin defaults high with 20kΩ pullup resistor (bias disabled).
FASTN	I	Fast Read Enable (8-channel device only): A TTL low level enables Fast Read mode (regardless of the state of the FR serial bit or the thermal asperity detection circuitry. Pin defaults high (FASTN disabled).
ABHV	O	Analog Buffered Head Voltage: ABHV (Analog Buffered Head Voltage) is represented on the pin when MRMEAS (4:<D4>) is set high. - The preamp drives this pin to an analog voltage representing five times the product of I_{MR}*R_{MR}. When the MRMEAS bit is set low the output goes into a high impedance state.
FLT/DBHV	O	Fault/Digital Buffered Head Voltage: FLT (Fault) is represented on the pin when MRMEAS (4:<D4>) is set low. Output is an open collector. - In Write mode, a high level indicates a fault. - In Read mode, a low level indicates a fault.DBHV (Digital Buffered Head Voltage) is represented on the pin when MRMEAS (4:<D4>) is set high. Pin defaults high (open collector) to prevent accidental write conditions.
WDX, WDY	I	Differential Pseudo-ECL write data inputs.
HR0P-HR7P	I	MR head connections, positive end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end
RDP, RDN	O	Read Data: Differential read signal outputs.
C1P,C1N	-	Compensation capacitor for the MR bias current loop.
HGND	-	Head Ground, common return for MR Heads and C1N.
GND	-	Ground
VCC	-	+5.0V supply
RS	-	Reference Voltage for both MR Bias and Write Current. (External 2kΩ resistor sets reference current for the read and write DACs.)
SENA	I	Serial Enable: Serial port enable signal; see Figures 94 and 95. Pin defaults low with 20kΩ pulldown resistor.
SCLK	I	Serial Clock: Serial port clock; see Figures 94 and 95. Pin defaults low with 20kΩ pulldown resistor.
SDIO	I/O	Serial Data: Serial port data; see Figures 94 and 95. Pin defaults high with 20kΩ pullup resistor.

1. I = Input pin, O = Output pin

SERIAL INTERFACE

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active.

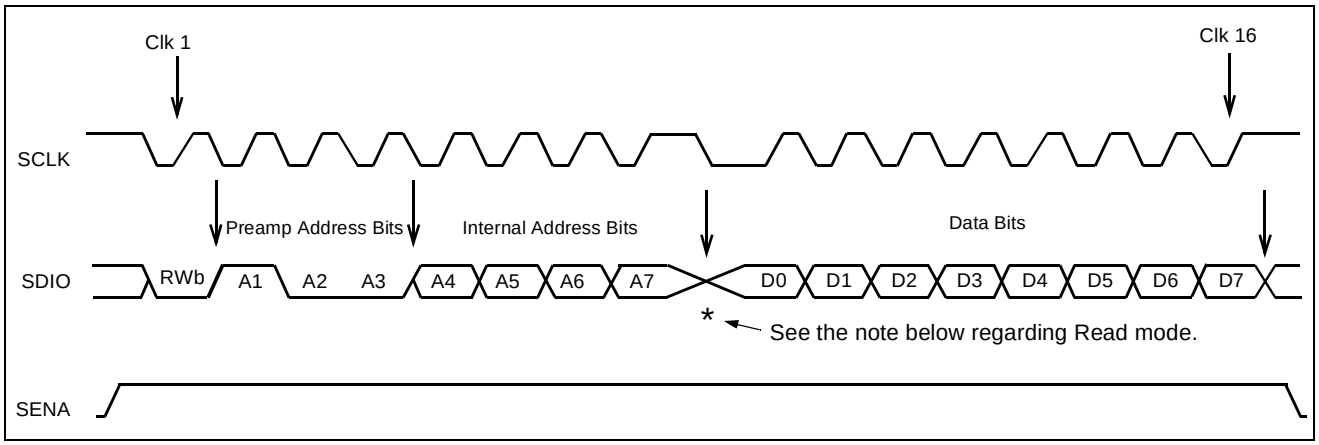
16 bits constitute a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0> (high for read, low for write), three preamp select bits <A1-A3> (which must be <001> for this preamp), and four register address bits <A4-A7>. The second 8 bits <D0-D7> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 131 and 132 for a bit description. See Table 134 and Figures 94 and 95 for serial interface timing information.



* For a read operation, the clock rate can be reduced for one period between the <A7> bit and the <D0> bit to provide sufficient time for the controller to tristate its output (release control of SDIO), and the VM6184 to untristate (activate control of SDIO). The clock rate need not be reduced during a write operation.

Figure 93 Serial Port Protocol

Table 131Serial Interface Bit Description -- Address Bits

Function	***Register #***	***Register Address Bits <A7-A4>***				***Device ID <A3-A1>***	R/WN ***<A0>***
Vendor ID / Channel Count	0	0	0	0	0	001	1/0
Head Select / MR Bias Current DAC	1	0	0	0	1		1/0
Write Current DAC / Servo Bank	2	0	0	1	0		1/0
Thermal Asperity	3	0	0	1	1		1/0
Sleep / Idle / Gain	4	0	1	0	0		1/0

Table 132Serial Interface Bit Description -- Data Bits

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Vendor ID / Channel Count	0 [1]	1 [2]	Channel	VS2	VS1	VS0	0	1	0
Head Select / MR Bias Current DAC	1	IMR4	IMR3	IMR2	IMR1	IMR0	HS2 [3]	HS1	HS0
Write Current DAC / Servo Bank	2	BANK0	WCB	0 [4]	IW4	IW3	IW2	IW1	IW0
Thermal Asperity	3	TA3	TA2	TA1	TA0	TADET	DR1 [2]	DR0 [2]	0 [4]
Mode Select	4	0 [4]	BANK1	FR	MRMEAS	G1	G0	IDLEN	SLEEPN

1. Read Only Register/Bits:
   Register 0, <D0-D2>: Vendor ID code (VTC=010),
   Register 0, <D3-D5>: Vendor revision code. Initial revision shall be (VS0 = 0, VS1 = 0, VS2 = 0),
   Register 0, <D6>: Channel count (0 = 8 channel, 1 = 4 channel),
   Register 0, <D7>: Programmable damping resistance (1 = present).
2. Programmable Damping Resistance Registers/Bits, See Table 126 on page 309 for further definition:
   Register 0, <D7>: Programmable damping resistance (1 = present),
   Register 3, <D1-D2>: Damping resistance DAC value.
3. Head Select Register/Bits. See Table 130 on page 310 for further definition:
   Register 1, <D2>: 1 is invalid for 4 channel device.
4. Reserved Registers/Bits:
   Register 2, <D5>,
   Register 3, <D0>,
   Register 4, <D7>.

Table 133Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Vendor ID / Channel Count	0	<1000 1010> [1]
Head Select / MR Bias Current DAC	1	<0000 0000>
Write Current DAC / Servo Bank	2	<0000 0000>
Thermal Asperity	3	<0000 0000>
Mode Select	4	<0000 0000>

1. Assumes an eight channel device <D6> = 0, first revision of the chip <D5-D3> = 001 from VTC <D2-D0> = 010.

Table 134Serial Interface Timing Parameters

Description	Symbol	Min	Nom	Max	Units
Serial Clock (SCLK) Rate		.001		40	MHz
SENA to SCLK delay	T_{sens}	30			ns
SDIO setup time	T_{ds}	5			ns
SDIO hold time	T_{dh}	5			ns
SCLK cycle time	T_{c}	25			ns
SCLK high time	T_{ckh}	20			ns
SCLK low time	T_{ckl}	20			ns
SENA hold time	T_{shld}	25			ns
Time between I/O operations	T_{sl}	50			ns
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			50	ns
Time to activate SDIO	T_{act}	0		50	ns
Duration of SENA (read)	T_{rd}	905			ns
Duration of SENA (write)	T_{wt}	855			ns
Risetime (CMOS 0.4 to 3.5 Volts, TTL 0.4 to 2.4 Volts)	T_{RIN}			4	ns
Falltime (CMOS 3.5 to 0.4 Volts, TTL 2.4 to 0.4 Volts)	T_{FIN}			4	ns
Risetime (CMOS 0.4 to 3.5 Volts, TTL 0.4 to 2.4 Volts)	T_{ROUT}			5	ns
Falltime (CMOS 3.5 to 0.4 Volts, TTL 2.4 to 0.4 Volts)	T_{FOUT}			5	ns

Note: SENA assertion level is high.

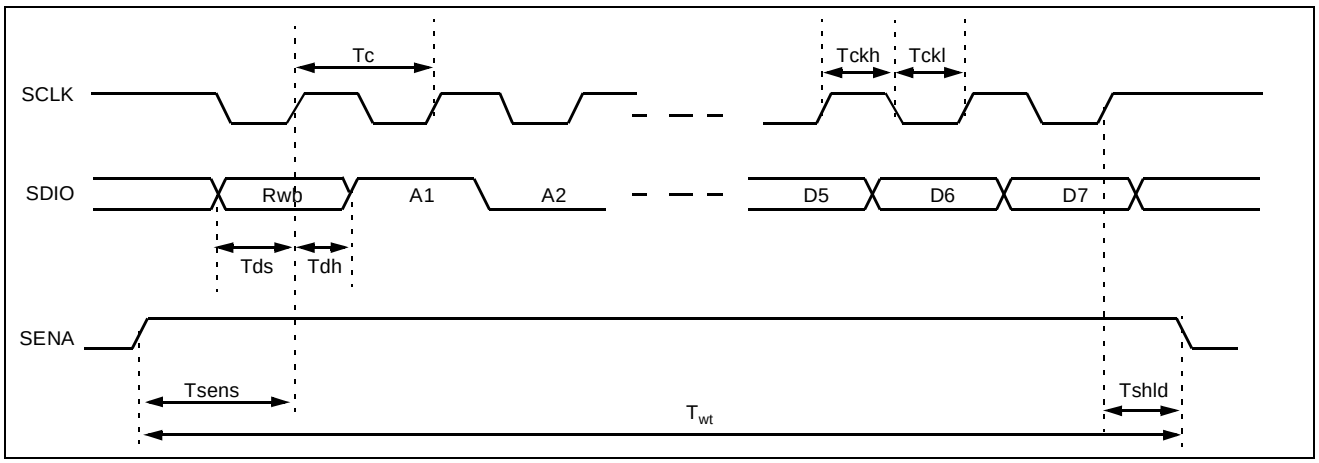


Figure 94 Serial Port Timing

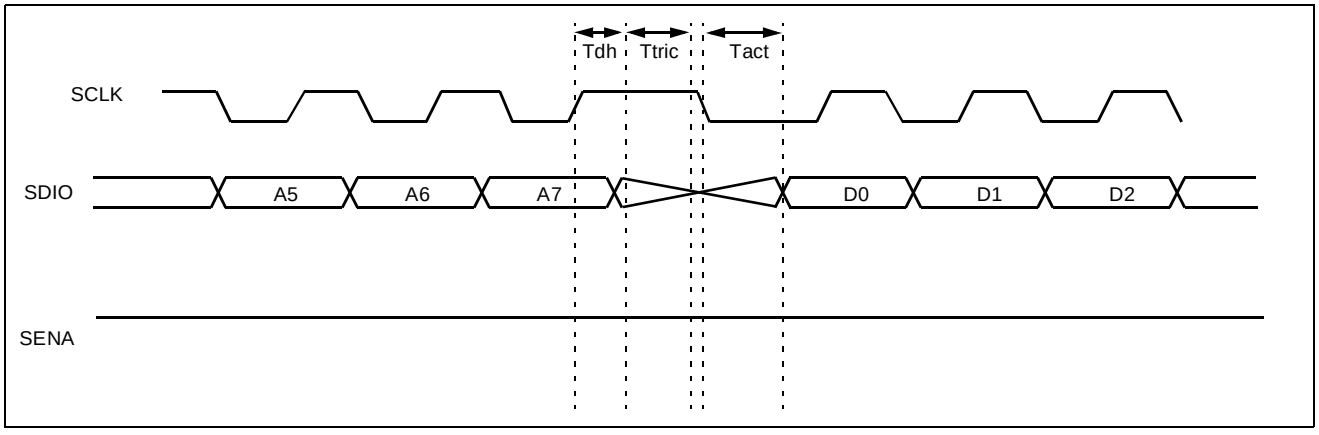


Figure 95 Serial Port Timing - Tristate Control

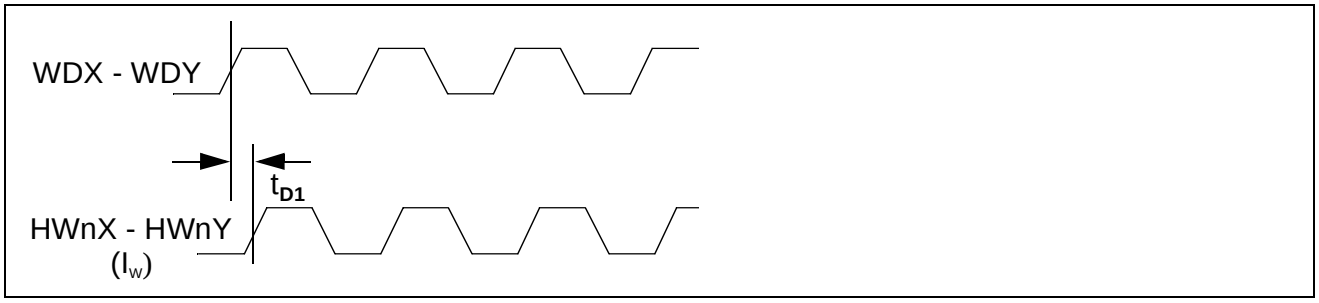


Figure 96 Write Mode Timing Diagram

The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY).
For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 8.75 mA		60	80	mA
		Write Mode, Bias enabled, I_W = 30mA, I_{MR} = 8.75 mA		95	120	
		Idle Mode, Bias disabled		8	16	
		Sleep Mode		3.5	10	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 5.0V		172	200	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 5.0V		330	380	
Power Dissipation	P_d	Read Mode, I_{MR} = 8.75 mA		300	440	mW
		Write Mode, Bias enabled, I_W = 30mA, I_{MR} = 8.75 mA		475	660	
		Idle Mode, Bias disabled		40	83	
		Sleep Mode		17.5	55	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 5.0V		860	1000	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 5.0V		1650	1900	
Input High Voltage	V_{IH}	PECL	1.9		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	
Input Low Voltage	V_{IL}	PECL	1.7		V_{IH} - 0.2	V
		TTL	-0.3		0.8	
PECL Differential Input Swing	WDX-WDY		0.2		1.5	V_{PK}
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			170	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-320			µA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.75mA, R_{MR}=50Ω

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
MR Head Current Range	I_{MR}		4.25	9	13.55	mA
MR Head Current Accuracy	ΔI_{MR}	4.25mA < I_{MR} < 13.55mA, R_{RS} = 2kΩ, V_{CC}=5V, T_A=25°C	-6		6	%
MR Head Current Temperature Sensitivity	$\frac{\Delta I_{MR}}{\Delta(115-25^{o}C)}$			0.6		%
MR Head Current Supply Sensitivity	$\frac{\Delta I_{MR}}{\Delta(0.5V)}$			0.3		%
Unselected MR Head Current					100	µA
MR Bias Top Voltage					800	mV
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Buffered Head Voltage Gain	A_{BHV}	Dynamic Gain I_{MR} (DAC=0) to I_{MR} (DAC=31)	4.5	5.0	5.5	V/V
Buffered Head Output Offset	V_{BOS}		-250	-80	250	mV
Digital Buffered Head Voltage	D_{BHV}	Low Threshold, MRMEAS bit = 1	312	347	382	mV
		High Threshold, MRMEAS bit = 1	553	614	675	
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, R_L(RDP, RDN) = 1kΩ, T_A = 25°C, V_{CC}=5V Gain bits (4:<D3-D2>) = 00	86	102	118	V/V
		Gain bits (4:<D3-D2>) = 01	108	128	148	
		Gain bits (4:<D3-D2>) = 10	134	159	184	
		Gain bits (4:<D3-D2>) = 11	171	204	237	
Differential Voltage Gain Temperature Sensitivity	$\frac{\Delta A_V}{\Delta(115-25^{o}C)}$			6		%
Differential Voltage Gain Supply Sensitivity	$\frac{\Delta A_V}{\Delta(0.5V)}$			0.2		%
Passband Upper Frequency Limit	f_{HR}	L_{MR} < 20nH, -3dB	160	200		MHz

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.75mA, R_{MR}=50Ω

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Passband Lower -3dB Frequency Limit	f_{LR}	C_1= 0.01µF		0.5	1	MHz
		FASTN = 0 or FR bit = 1		5		
Equivalent Input Noise (sense amp only)	e_a	1 < f < 100 MHz		0.62		$\frac{nV}{\sqrt{Hz}}$
Bias Current Noise	i_n			10		$\frac{PA}{\sqrt{Hz}}$
Equivalent Input Noise (total, excluding R_{MR})	e_n	1 < f < 100 MHz		0.8	1.0	$\frac{nV}{\sqrt{Hz}}$
Input Resistance	R_{IN}			3		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz, Gain bits = 11	5			mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC}, 1 < f < 100 MHz Input Referenced	45			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 1 < f < 100 MHz Input Referenced	45			dB
Pin Rejection	PR	100mV_{pp} @ R/WN, BIASN, SCLK, SDIO or SENA, Output Referenced, Gain bit = 0, 1 < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-200		200	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.5		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			300	mV
Differential Output Resistance	R_{DO}	Read Mode		62		Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	2			mA

THERMAL ASPERITY CHARACTERISTICS

Parameter	*Specification*
Thermal Asperity Detection Threshold	50[1 + DAC value (0-15)], ± 20% @ 50 to 100mV, ± 15% @ >100mV, output-referred
Thermal Asperity Detection Range	50mV - 800mV over baseline DC level in RDP/RDN (low frequency variation in baseline tracked by threshold)

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 130nH, R_H = 16Ω, f_{DATA} = 5MHz.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Write Current Range	I_W	base to peak	10		45	mA
Write Current Accuracy	ΔI_W	10mA < I_W < 20mA, V_{CC} = 5V, T= 25°C	-15		15	%
		20mA < I_W < 45mA, V_{CC} = 5V, T= 25°C	-10		10	%
Write Current Sensitivity Temperature	$\frac{\Delta I_W}{\Delta(115-25^oC)}$			3		%
Write Current Sensitivity Supply	$\frac{\Delta I_W}{\Delta(0.5V)}$			0.6		
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V		7		V_{PP}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Resistance	R_O			See Table 126 [1]		Ω
Differential Output Capacitance					12	pF

1. The part has programmable damping resistance.
Note that the write current flowing to the head is dependent on the damping resistance; see equation 73 on page 309.

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SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 130nH, R_H = 16Ω, f_{DATA} = 5MHz, I_{MR}=8.75mA.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
R/WN to Write Mode	t_{RW}	To 90% of write current	20	30	50	ns
R/WN to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value		300 [1]	1000	ns
Read or Write to Idle Mode	t_{RI}/t_{WI}	To 10% of envelope		150	500	ns
Idle to Read Mode	t_{CS}	RDP/RDN to 90% of envelope and within ±30mV of final value		5 [1]	10	µs
Bias Disable to Enable, Read Mode	t_{BDE}	RDP/RDN to within ±30mV of final value		7.5	25	µs
HS0 - HS3 to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode ΔR_{MR} = 0, ΔI_{MR} = 0		6.5	10	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		15	20	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time; L_H = 0; R_H = 0			0.5	ns
Rise/Fall Time	t_r / t_f	10 - 90%, R_D=670Ω		1.7		ns
Bias Current Change	$t(\Delta I_{MR})$	ΔI_{MR} from 5 to 10 mA, RDP/RDN to within ±30mV of final value		7	25	µs

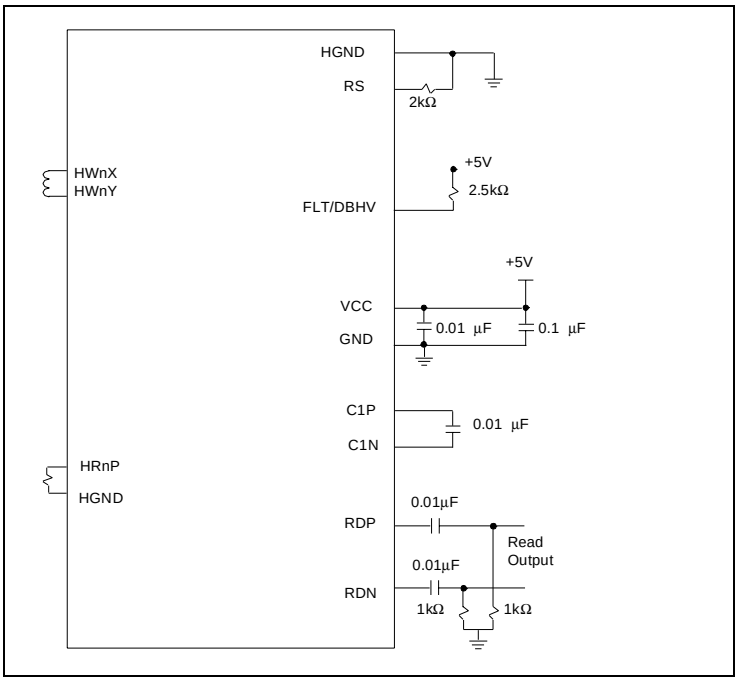
1. BIASN pin active low for 25 µs preceding the mode transition.

FAULT PROCESSING CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC Fault Threshold [1]	V_{LFT}	Fault Detected	3.6	3.9	4.2	V
	V_{UFT}	Fault Removed	3.9	4.1	4.4	
VCC Fault Threshold Hysteresis	V_{HFT}			200		mV
MR Head Open Fault Threshold				1000		mV
Open Head Fault Delay	t_{FLTD}	Good to Open Head		7		µs
Time Between Transitions for Safe Operation	t_{SAFE}			300	500	ns
MR Head Short Fault Threshold				50		mV
Thermal Asperity Detect Delay	TA_{DLY}			50		ns
Output High Current	I_{FLToH}	V_{OH} = 5.0 V			50	µA
FLT/DBHV Output Voltage Low	V_{FLToL}	I_{OL} = 2 mA			0.4	V
FLT/DBHV Settling Time	$DBHV_{SETTLE}$				10	µs

1. Writer Functionality shall be maintained for V_{CC} conditions ranging from the specified V_{CC} limits to the Low Voltage Detector Threshold Voltage.

TYPICAL APPLICATION CONNECTIONS



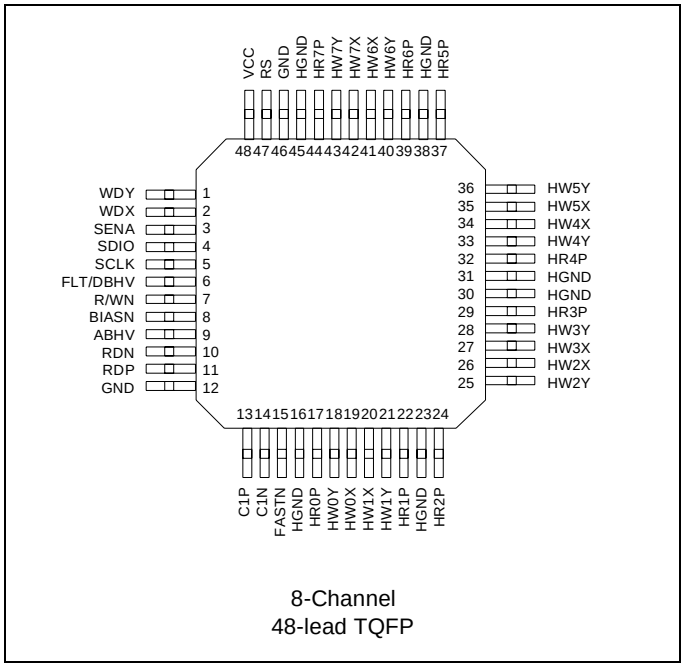
Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Minimizing parasitics at the C1 node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the pins/pads as possible.
- For optimal performance connect C1N externally to the same ground as the read heads (HGND), or isolate C1N as shown above (C1N is tied to HGND internally).
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins/pads:
  VCC - GND
- For maximum stability, place the decoupling capacitors and the R_{RS} resistor as close to the pins/pads as possible.

VM6184

8-CHANNEL CONNECTION DIAGRAM



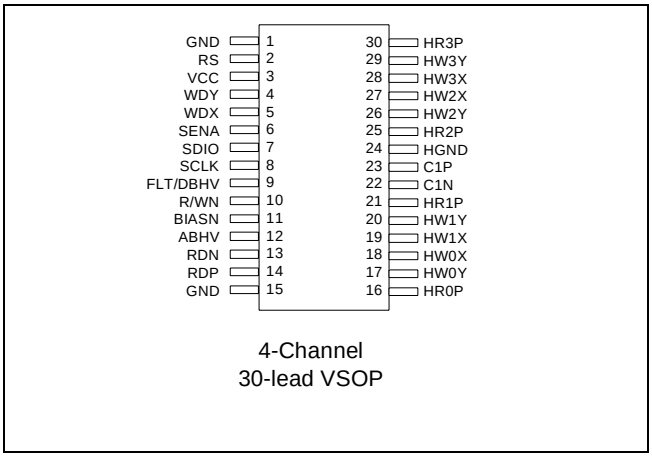
8-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

VM6184

4-CHANNEL CONNECTION DIAGRAM



4-Channel
30-lead VSOP

Specific Characteristics

See the general data sheet for common specification information.

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VTC Inc.
Value The Customer™

VM6185 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Requires One External Component
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Operates from a Single +5 Volt Power Supply
  - Fault Detection Capability
  - Available in a 38-pin VSOP Package
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 6 - 18 mA Range
  - Programmable Read Voltage Gain
    (200 V/V or 250 V/V Typical)
  - Thermal Asperity Detection and
    Fast Recovery Compensation
  - Digital Buffered Head Voltage (DBHV)
    Measurement Mode
  - Input Noise = 0.67 nV/$\sqrt{Hz}$ Typical
    (R_{MR} = 25Ω, I_{MR} = 13.5mA)
  - High Bandwidth = 220 MHz Typical
    (R_{MR} = 30Ω, -3dB)
  - Power Supply Rejection Ratio = 60 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 63 mA Range
  - Rise Time = 1.5 ns Typical
    (R_H - 20Ω, L_H = 180 nH, I_W = 30 mA)
  - Multi-Channel Servo Write

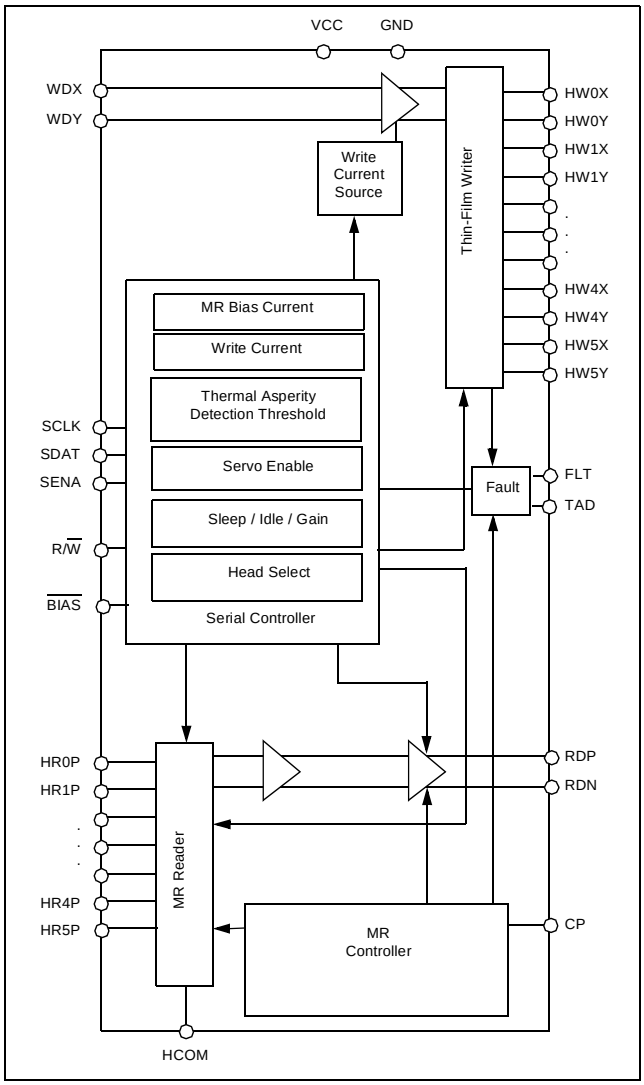
DESCRIPTION

The VM6185 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM6185 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM6185 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available in a 6-channel option in a 38-pin VSOP package. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Read Bias Current, I_{MR} 20mA
Write Current, I_W 70mA
Input Voltages:
Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
Output Current:
RDP, RDN: I_O ..... -10mA
Junction Temperature, T_J 150°C
Storage Temperature, T_{stg} -65° to 150°C
Thermal Characteristics, Θ_{JA}:
38-lead VSOP ..... 88°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Write Current, I_W .....10 - 63 mA
Write Head Inductance, L_W ..... 10 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 6 - 18 mA
Read Head Inductance, L_{MR} ..... 10 - 50 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J 0°C to 125°C

Serial Interface Controller

The VM6185 uses a 3-line serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Table 142 for a bit description.

The serial interface has three input lines: SCLK (serial clock), SENA (serial enable) and SDAT (serial data). The SCLK line is used as reference for clocking data into SDAT. The SENA line is used to activate the SCLK and SDAT lines and power-up the associated circuitry.

A complete data transfer consists of a minimum of 8 bits and could contain any number of bits. If more than 8 bits are used, the first (X-8) bits are ignored. The final 8 bits before SENA drops low should consist of three register address bits <A2-A0> and five data bits <D4-D0>; see Figure 99.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data line (SDAT) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for X cycles; on the falling edge of SENA, the data from the previous 8 cycles will be written to the addressed register. SCLK must be kept high until SENA goes low.

Note: Serial register activity is not recommended in read mode and will result in reader performance degradation.

See Table 143 and Figure 100 for serial interface timing information.

Vendor ID Code Function

While in Sleep mode, data will be written to the vendor ID serial register bits (VEN0 and VEN1; register 3, bits <D0-D1>). When these bits match VTC's vendor ID code (00), the FLT pin will go low.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM6185 uses the current-bias/current-sensing MR architecture. The magnitude of the bias current ranges from 6 - 18 mA and is governed by the following equation:

$$I_{MR} = 6 + 0.5(k_{IMR}) + 4.5(k_{IMR-range}) \quad \textit{(eq. 74)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
k_{IMR} represents the MR bias DAC setting (0 to 15).
$k_{IMR\text{-}range}$ represents the MR bias range bit (0 or 1).

The bias current levels are also represented in the table below:

Table 135MR Bias Current

IMR3 1:<D3>	IMR2 1:<D2>	IMR1 1:<D1>	IMR0 1:<D0>	IMR-R=0 1:<D4> mA	IMR-R=1 1:<D4> mA
0	0	0	0	6	10.5
0	0	0	1	6.5	11
0	0	1	0	7	11.5
0	0	1	1	7.5	12
0	1	0	0	8	12.5
0	1	0	1	8.5	13
0	1	1	0	9	13.5
0	1	1	1	9.5	14
1	0	0	0	10	14.5
1	0	0	1	10.5	15
1	0	1	0	11	15.5
1	0	1	1	11.5	16
1	1	0	0	12	16.5
1	1	0	1	12.5	17
1	1	1	0	13	17.5
1	1	1	1	13.5	18

A "high" TTL level applied to the R/$\overline{W}$ pin and a low level applied to the $\overline{BIAS}$ pin (along with the appropriate levels on the IDLE and SLEEP bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 140).

The output of the read preamp is differential.

Read Bias Enable in Read Mode

Taking the $\overline{BIAS}$ pin low in read mode enables MR bias current to the selected head.

Taking the $\overline{BIAS}$ pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

Four bits in register 1 (<D3-D0>) represent the binary equivalent of the DAC setting (0-15, MSB first). A fifth bit (1:<D4>) represents a range factor.

GAIN and BOOST Bits

The GAIN bit (register 4 <D1>) puts the read gain in low range or high range. The BOOST bit (register 5<D4>) boosts the read gain by 3 dB at 100 MHz when set to 1.

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Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 97 displays the reader output for an uncompensated thermal asperity event.)

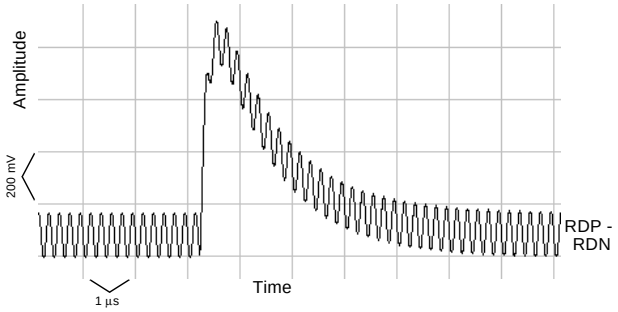


Figure 97 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM6185 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Programming a non-zero TA threshold value (register 2, bits <D3-D0>) allows the TA detection circuitry to detect an asperity event. The threshold for thermal asperity detection is output-referred, has a range of 49 - 385 mV and is governed by the following table:

Table 136Thermal Asperity Detection Threshold

TA3 2:<D3>	*TA2 2:<D2>*	*TA1 2:<D1>*	*TA0 2:<D0>*	*TA Threshold (mV)*
0	0	0	0	OFF
0	0	0	1	49
0	0	1	0	53
0	0	1	1	57
0	1	0	0	63
0	1	0	1	70
0	1	1	0	78
0	1	1	1	91
1	0	0	0	105
1	0	0	1	123
1	0	1	0	146
1	0	1	1	175
1	1	0	0	210
1	1	0	1	256
1	1	1	0	312
1	1	1	1	385

Reporting

Whenever a thermal asperity event is detected, it is reported as a high level on the TAD pin.

Thermal asperity events can also be reported on the FLT pin by setting the $\overline{\text{TAFLT}}$ bit (register 5, bit <D1>) low. When reporting is enabled on the FLT pin, a thermal asperity event will be reported as a low level on the FLT pin. Setting this bit high disables TA output on the FLT pin.

Compensation

The TA compensation mode selection bits (register 4: bits <D4-D3>) determine which compensation mode is initiated if a thermal asperity is detected; see the table below:

Table 137TA Compensation Mode Selection

TACM1 4:<D4>	*TACM0 4:<D3>*	*Mode*
0	0	Off
0	1	Adaptive
1	0	Fast (5 MHz)
1	1	Fast (10 MHz)

Note: Setting the compensation mode to Off makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the corner frequency movement.

(Fast Recovery)

When activated, Fast Recovery Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 5 MHz (or 10 MHz) until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 98).

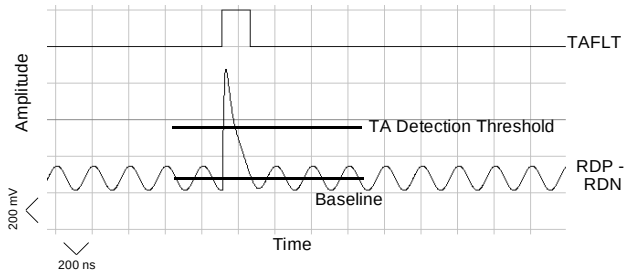


Figure 98 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

(Adaptive Compensation)

With adaptive compensation the fast mode is invoked linearly in proportion to the amplitude of the asperity event.
Note that this adaptive compensation is automatically invoked regardless of whether the programmed detection threshold value has been exceeded.

MR Measurement / Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (register 4, bit <D2>) allows the digital buffered head voltage (DBHV) to be represented on the FLT pin.

The FLT output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 150mV and 450mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Fault Detection

Setting the MRMEAS bit low (register 4, bit <D2>) allows the fault status (FLT) to be represented on the FLT pin.

In the read mode, a low on the FLT line (open collector with internal 3kΩ pull-up resistor) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- MR open head
- Thermal Asperity event (if enabled)

The MR head voltage is clamped to provide MR open-head protection (until another head is selected or a mode change is initiated). The user should provide at least a 25µs delay when switching from an open-head to a connected-head. This allows the clamping head voltage to settle to a safe value from the open head event.

Write Mode

In the write mode, the circuit operates as a thin-film write-current switch, driving the thin-film write element of the MR head.

The magnitude of the write current ranges from 10 - 63 mA. The following equation governs the write current magnitude:

$$I_W = 10 + 3.3(k_{IW}) + Range \qquad \textit{(eq. 75)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 7).
"Range" represents an additional 0mA, 15mA or 30mA; see the table below.

Table 138Write Current Range Selection

IWR1 3:<D4>	*IWR0 3:<D3>*	*Write Current Range Factor*
0	0	Range 0 - Add 0 mA
0	1	Range 1 - Add 15mA
1	0	
1	1	Range 2 - Add 30mA

The write current levels are also represented in the table below:

Table 139Write Current

IW2 3:<D2>	*IW1 3:<D1>*	*IW0 3:<D0>*	*Range 0 mA*	*Range 1 mA*	*Range 2 mA*
0	0	0	10	25	40
0	0	1	13.3	28.3	43.3
0	1	0	16.6	31.6	46.6
0	1	1	19.9	34.9	49.9
1	0	0	23.2	38.2	53.2
1	0	1	26.5	41.5	56.5
1	1	0	29.8	44.8	59.8
1	1	1	33.1	48.1	63.1

A "low" TTL level applied to R/$\overline{W}$ (along with the appropriate levels on the IDLE and SLEEP bits) places the preamp in the write mode (see Table 140). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 101.

Write Current DAC

Three bits in register 3(<D2-D0>) represent the binary equivalent of the DAC setting (0-7, MSB first). Fourth and fifth bits (register 3, bits <D4-D3>) represent two additional range factors.

Read Bias Enable in Write Mode

Taking the $\overline{BIAS}$ pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal "read" state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the $\overline{BIAS}$ pin high in write mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

Fault Detection

Setting the MRMEAS bit low (register 4, bit <D2>) allows the fault status (FLT) to be represented on the FLT pin.

In the write mode, a high on the FLT line (open collector with internal 3kΩ pull-up resistor) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Write head shorted to ground
- Low power supply voltage
- Insufficient write data transition frequency (> 500ns between transitions)

Two transitions on pin WDX, after the fault is corrected, may be required to clear the fault line.

When a low supply fault condition is detected, the write current source internal to the chip is shut down and no current flows to any head.

Note: There is no MR open head detection, reporting or protection in Write mode when the $\overline{BIAS}$ pin is low.

Servo Write Mode

In the servo write mode, three channels or all channels of the VM6185 are written simultaneously.

Servo mode is initiated with a four-step process (see Table 140):

11) Select Read mode (take R/$\overline{W}$ high)
12) Set the Servo bit (register 2; bit <D4>) to a "1"
13) Force the FLT pin to 2V above V_{CC} with a minimum of 6mA
14) Initiate Servo mode (take R/$\overline{W}$ low)

All conditions must be maintained to remain in the servo mode.

The HS0 - HS3 register bits (0:<D3-D0>) determine which heads are written (see Table 141). Write mode fault circuits are disabled.

Note: It is the customer's responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Idle Mode

Setting the IDLE bit low (register 0, bit <D4>) places the preamp in Idle mode (see Table 140). Only the serial register, bias circuitry and dummy head cell remain active.

The MR bias current source is active and the MR bias current is directed to an internal dummy head. The MR bias current control loop is active and the reader output is clamped at the common-mode voltage.

Note: There is no MR open head detection, reporting or protection in Idle mode when the $\overline{\text{BIAS}}$ pin is low.

Sleep Mode

Setting the SLEEP bit low (register 4, bit <D0>) places the preamp in Sleep mode (see Table 140). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Transitions from Sleep mode to Read mode should always be made by first entering the Idle mode for a minimum of 20µs.

Note: There is no MR open head detection, reporting or protection in Sleep mode when the $\overline{\text{BIAS}}$ pin is low.

Table 140Mode Select

$\overline{R/W}$	$\overline{BIAS}$	Servo [1]	$\overline{IDLE}$ 0:<D4>	$\overline{SLEEP}$ 4:<D0>	MODE
1	1	X	1	1	Read Bias Disabled (dummy head)
1	0	X	1	1	Read Bias Enabled
0	1	0	1	1	Write Bias Disabled (dummy head)
0	0	0	1	1	Write Bias Enabled
0	X	1	1	1	Servo
X	X	X	0	1	Idle Bias Disabled (dummy head)
X	X	X	X	0	Sleep

1. In this table, a “1” in the Servo column represents a combination of the SERVO bit being set to a “1” in the serial register (register 2, bit <D4>) and sourcing into the FLT pin a minimum of 6mA with a compliance voltage greater than VCC + 2V.

Table 141Head Select

HS3 0:<D3>	HS2 0:<D2>	HS1 0:<D1>	HS0 0:<D0>	HEAD Normal	HEADS Servo
0	0	0	0	0	none
0	0	0	1	1	1,3,5
0	0	1	0	2	none
0	0	1	1	3	none
0	1	0	0	4	none
0	1	0	1	5	all
0	1	1	0	Idle	none
0	1	1	1	Idle	0,2,4
1	X	X	X	Idle	none

PIN FUNCTION LIST AND DESCRIPTION

Symbol	Input/Output [1]	Description
R/$\overline{W}$	I	Read/Write: A TTL low level enables write mode. Pin defaults high (read mode) with an internal 9.8K pull-up resistor.
$\overline{BIAS}$	I	Bias Enable: A TTL low level enables MR bias current to the selected head. A TTL high level directs bias current to a dummy head. Pin defaults low (selected head) with an internal 39K pull-down resistor.
FLT	O	Fault: Open collector output with internal 3kΩ pull-up resistor. Setting the MRMEAS bit high (register 4, bit <D2>) allows the digital buffered head Voltage (DBHV) to be represented on the FLT pin. Setting the MRMEAS bit low (register 4, bit <D2>) allows the fault status (FLT) to be represented on the FLT pin. In Write mode, a TTL high level indicates a fault. In Read mode, a TTL low level indicates a fault.
TAD	O	Thermal Asperity Detection Fault output. A CMOS high level indicates that a thermal asperity was detected.
WDX, WDY	I	Differential Pseudo-ECL write data inputs.
HR0P-HR5P	I	MR head connections, positive end.
HW0X-HW5X	O	Thin-Film write head connections, positive end.
HW0Y-HW5Y	O	Thin-Film write head connections, negative end
RDP, RDN	O	Differential read signal outputs.
CP	-	Compensation capacitor (10nF) for the MR bias current loop.
HCOM	-	Head Common: Common return for MR heads and external capacitor.
GND	-	Ground
VCC	-	+5.0V supply
SENA	I	Serial Enable: Serial port enable signal; see Figure 100.
SCLK	I	Serial Clock: Serial port clock; see Figure 100.

SDAT	I	Serial Data: Serial port data; see Figure 100.

1. I = Input pin, O = Output pin

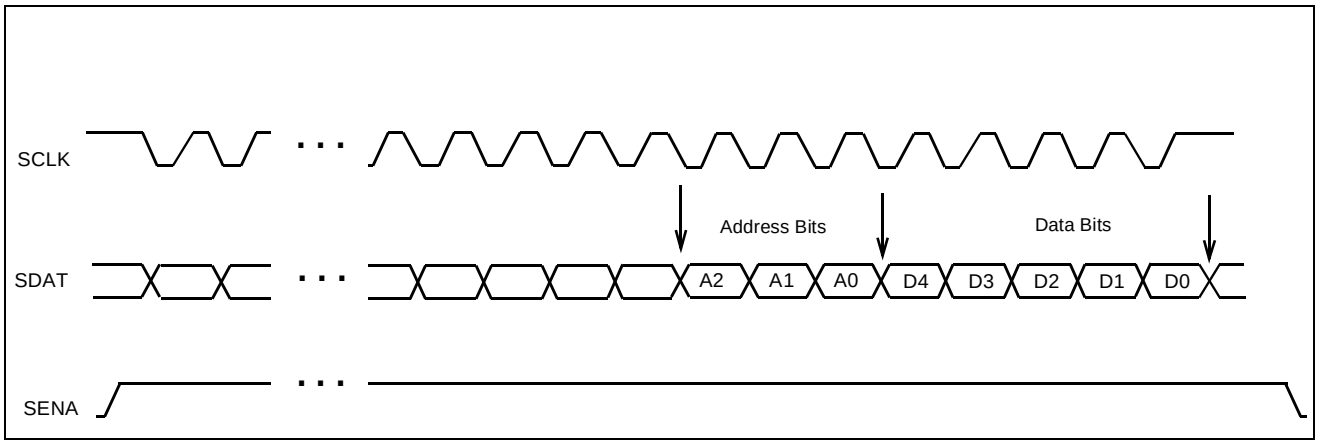


Figure 99 Serial Port Protocol

Table 142Serial Interface Bit Description

Function	*Register #*	*Address Bits*			*Data Bits*				
		<A2>	*<A1>*	*<A0>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Head Select / Idle	0	0	0	0	$\overline{\text{IDLE}}$	HS3	HS2	HS1	HS0
MR Bias Current DAC / Range	1	0	0	1	IMR-R	IMR3	IMR2	IMR1	IMR0
Thermal Asperity DAC / Servo Enable	2	0	1	0	SERVO	TA3	TA2	TA1	TA0
Vendor ID / Write Current DAC / Write Current Range	3	0	1	1	IW-R1	IW-R0	IW2	IW1 / VEN1	IW0 / VEN0
Sleep / Gain / MR Head Measurement (DBHV) / Thermal Asperity Compensation Mode	4	1	0	0	TACM1	TACM0	MRMEAS	GAIN	$\overline{\text{SLEEP}}$
Thermal Asperity Fault Output / Boost	5	1	0	1	BOOST	1	1	$\overline{\text{TAFLT}}$	1

1. Reserved

Table 143Serial Interface Timing Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) Rate				44	MHz
SENA to SCLK delay	T_{sens}	7.5			nS
SDAT setup time	T_{ds}	5			nS
SDAT hold time	T_{dh}	5			nS
SCLK cycle time	T_{c}	23			nS
SCLK high time	T_{ckh}	7.5			nS
SCLK low time	T_{ckl}	7.5			nS
SENA hold time	T_{shld}	7.5			nS
SCLK rise and fall time	T_{ckr}			3	nS

Note: SENA assertion level is high.

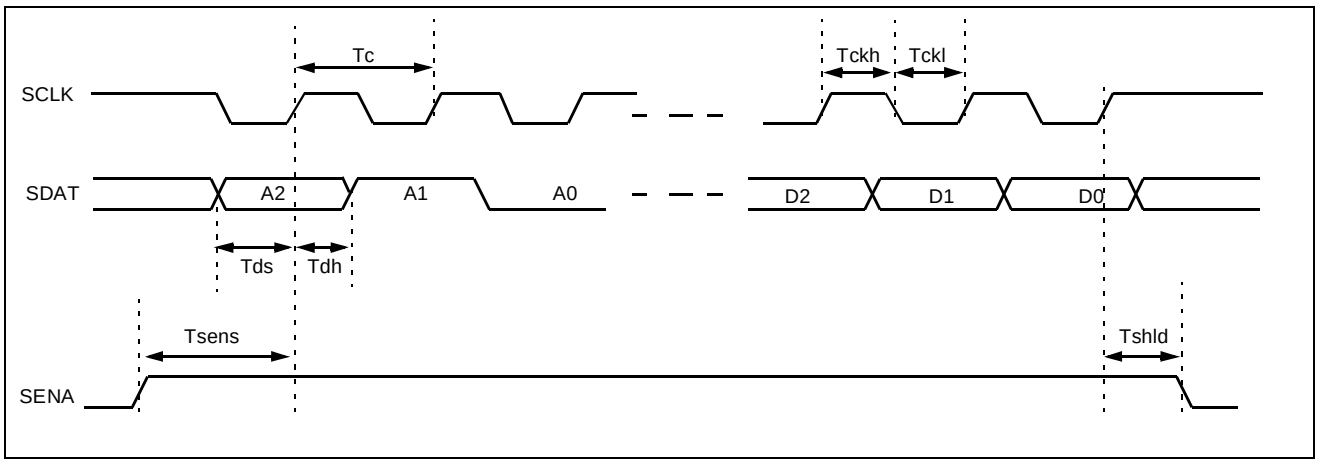


Figure 100 Serial Port Timing

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
V_{CC} Power Supply Current	I_{CC}	Read Mode (See Formula 1 below.)		61	72	mA
		Read Mode, Bias disabled		43	52	
		Write Mode (See Formula 2 below.)		80	90	
		Write Mode, Bias enabled (See Formula 3 below.)		99	111	
		Idle Mode		30	36	
		Sleep Mode, vendor ID = “00”		3	5	
		Servo Mode, I_{WS} = 25mA, Bank of six heads (See Formula 4 below.)		232	252	
Power Dissipation	P_d	Read Mode		306	395	mW
		Read Mode, Bias disabled		215	286	
		Write Mode		399	497	
		Write Mode, Bias enabled		495	612	
		Idle Mode		150	198	
		Sleep Mode, vendor ID = “00”		15	28	
		Servo Mode, I_{Ws} = 25mA, Bank of six heads		1160	1386	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.2		V_{CC} - 0.5	V
		TTL	2.0		V_{CC} + 0.3	
Input Low Voltage	V_{IL}	PECL	V_{IH} - 0.9		V_{IH} - 0.55	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V	-100		100	
		R/$\overline{W}$	-360			
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-80		80	
		R/$\overline{W}$	-640			
PECL Differential Swing	P_{DS}		550		900	mV
Fault Output High Current	I_{OH}	V_{OH} = 5V			50	µA
Fault Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.5	V

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Fault Threshold	V_{CTH}	I_w < 200µA, Fault detected	3.6	3.8	4.0	V
	V_{UTH}	Fault removed	3.9	4.1	4.3	
V_{CC} Fault Threshold Hysteresis	V_{HTH}		200	300	400	mV

Formulas:

1) Typ: 53 + (1.05 x I_{MR}) Max: 63 + (1.1 x I_{MR})
2) Typ: 45 + (1.1 x I_W) Max: 54 + (1.15 x I_W)
3) Typ: 50 + (1.1 x I_W) + (1.05 x I_{MR}) Max: 60 + (1.15 x I_W) + (1.1 x I_{MR})
4) Typ: 23 + (1.1 x Hds x I_S) Max: 28 + (1.18 x Hds x I_S)

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA, L_{MR} = 20nH, R_{MR}=30Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		6	13.5	18	mA
MR Head Current Accuracy	ΔI_{MR}	6mA < I_{MR} < 18mA	-5		5	%
Unselected MR Head Current					100	µA
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, R_L(RDP, RDN) = 1kΩ, Gain bit = 0	170	200	230	V/V
		Gain bit = 1	210	250	290	
Passband Upper Frequency Limit	f_{HR}	-3dB, Gain bit = 0	165	220		MHz
		-1dB, Gain bit = 0	100			
Gain Boost	BST	f = 100MHz, Gain bit = 0, Boost bit = 1		3		dB
Passband Lower -3dB Frequency Limit	f_{LR}	Gain bit = 0		0.5	0.6	MHz
Equivalent Input Noise (sense amp only)	e_{na}	R_{MR} = 25Ω, 1 < f < 50 MHz		0.50		$nV/\sqrt{Hz}$
Bias Current Noise (referred to Input)	i_n	I_{MR} = 13.5mA		16		$pA/\sqrt{Hz}$
Equivalent Input Noise (total)	e_n	R_{MR} = 25Ω; 10 < f < 50 MHz		0.67		$nV/\sqrt{Hz}$
Integrated Noise	e_{in}	R_{MR} = 25Ω; 1 < f < 140 MHz		8.8		µV
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz , Gain bit = 0		5		mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or GND, 1 < f < 100 MHz		60		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 1 < f < 100 MHz	45			dB
Output Offset Voltage	V_{OS}		-50		50	mV
Common Mode Output Voltage	V_{OCM}	Read Mode, Write Mode		V_{CC} - 2.5		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)	-150		150	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode			50	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	1.5			mA
Total Harmonic Distortion	THD	f = 20 MHz, V_{IN}=1mV_{pp}			1	%
MR Head Measurement Threshold (Head Resistance / DBHV)		Low Threshold (FLT goes high)	150	170	210	mV
		High Threshold (FLT goes low)	420	450	480	
Thermal Asperity Detection Range	V_{TATH}	DC level in RDX/RDY over baseline	49		385	mV_{bp}

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA, L_{MR} = 20nH, R_{MR}=30Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Thermal Asperity Detection Threshold Tolerance	ΔV_{TATH}	DAC setting	-15		15	%
MR Head Voltage	V_{MR}	$I_{MR} \cdot R_{MR}$			0.66	V
Overshoot on I_{MR} during Idle-to-Read Transitions	I_{MROV}	0.25V < V_{MR} < .6V		6		%
Clamping Threshold for Open MR Head				820		mV
Clamping Threshold for Shorted MR Head				50		mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 31.6mA, L_H = 180nH, R_H = 20Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Range	I_W	(base to peak)	10		63	mA
Write Current Tolerance	ΔI_W	10mA < I_W < 40mA	-5		5	%
		40mA < I_W < 63mA	-8		8	
Servo Current Range	I_S	base to peak, 6 heads	10		40	mA
		base to peak, 3 heads	10		60	
Servo Current Tolerance	ΔI_S	10mA < I_S < 40mA	-8		8	%
Servo Enable Current at the FLT pin	I_{SE}	V_{CC} + 2.0V < Voltage at FLT pin	6		13	mA
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V	6	7.5		V_{pp}
Unselected Head Current	I_{UH}				50	μA_{pk}
Time between Write Data Transitions for Safe Condition	t_{SAFE}	FLT = Low			500	ns
Open Head Detection	R_{OHD}	Detect Open Head	1000			Ω
	V_{OHD}	Do Not Detect Open Head, $I_W \cdot R_H$			2	V
Shorted Head Detection	R_{SHD}	Detect Shorted Head (to GND)			5	Ω
		Do Not Detect Shorted Head	1000			

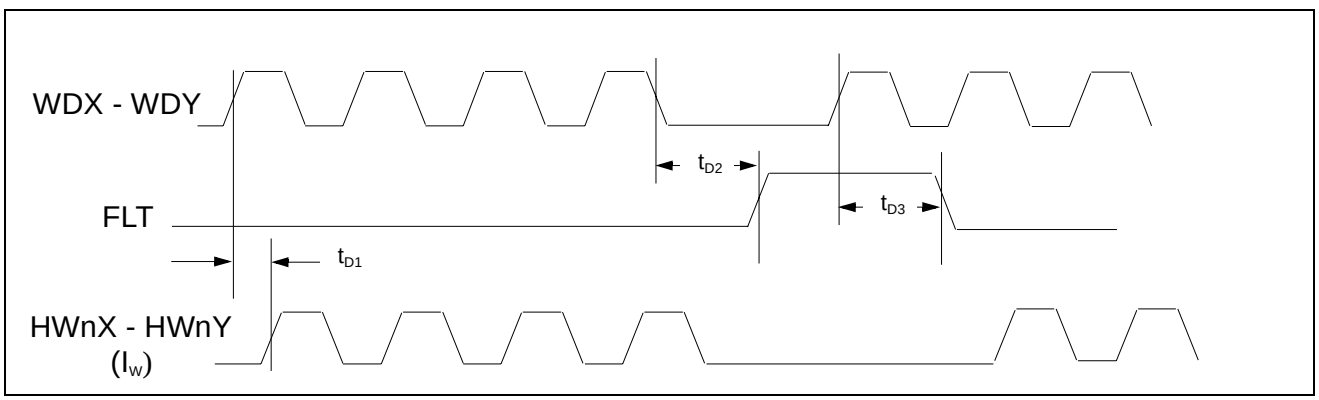


Figure 101 Write Mode Timing Diagram

Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

SWITCHING CHARACTERISTICS

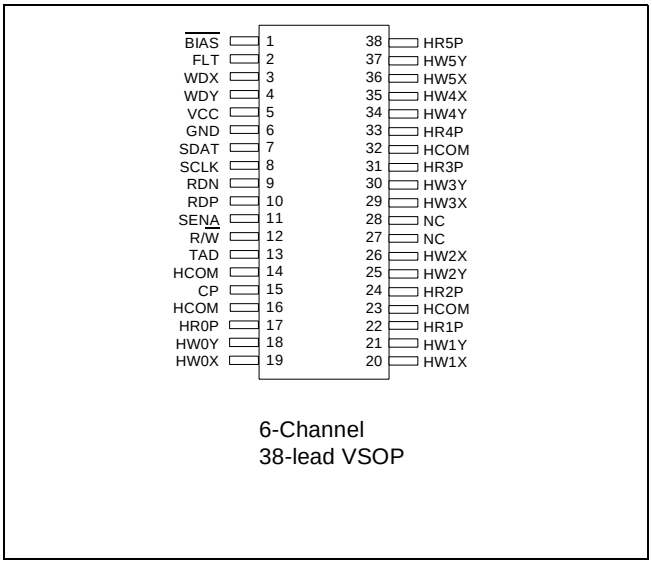
Recommended operating conditions apply unless otherwise specified: I_W = 31.6mA, L_H = 180nH, R_H = 20Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read (R/$\overline{W}$) to Write Mode	t_{RW}	To 90% of write current		50	70	ns
Write (R/$\overline{W}$) to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value[1]		300	400	ns
Idle to Read Mode	t_{IR}	RDP/RDN to within ±30mV of final value		6	10	µs
Sleep to Idle Mode [2]	t_{SI}				20	µs
Head Select to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode		6	10	µs
Read to Idle Mode	t_{RI}	To 10% of read envelope		0.16	0.5	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		6	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time		70	200	ps
Rise/Fall Time	t_r / t_f			1.5	1.8	ns
FLT delay, Write Safe to Unsafe	t_{D2}		0.5		3.6	µs
FLT delay, Write Unsafe to Safe	t_{D3}				1.1	µs
TA FLT delay		TA detected to TAD pin high (or FLT pin low, if enabled)			0.2	µs

1. $\overline{BIAS}$ pin active low for 10 µs preceding the R/$\overline{W}$ transition.
2. Sleep to Read mode changes must transition through Idle Mode

VM6185

6-CHANNEL CONNECTION DIAGRAM



6-Channel
38-lead VSOP

Specific Characteristics

See the general data sheet for common specification information.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

VTC Inc.
Value The Customer™

VM61852/4/8 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

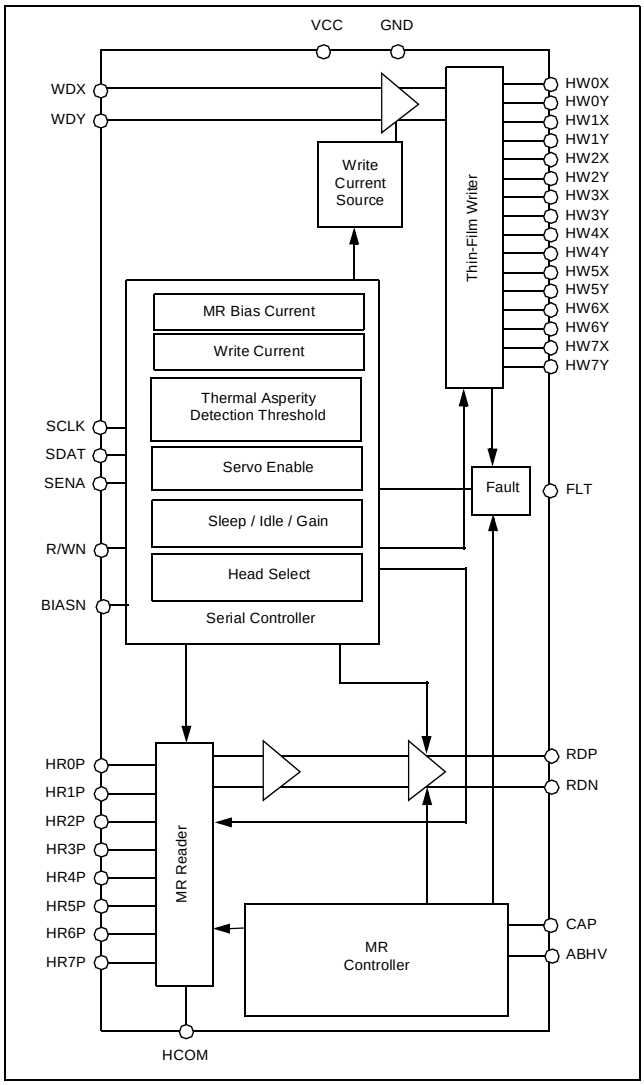
FEATURES

- Requires One External Component
- Designed for Use With Four-Terminal MR Heads
- 3-Line Serial Interface
  (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
- Operates from a Single +5 Volt Power Supply
- Fault Detection Capability
- Available in several Channel/Package Options

- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 6 - 18 mA Range
  - Programmable Read Voltage Gain
    (200 V/V or 250 V/V Typical)
  - Thermal Asperity Detection and
    Fast Recovery Compensation
  - Digital and Analog Buffered Head Voltage
    (DBHV/ABHV)
    Measurement Mode
  - Input Noise = 0.67 nV/$\sqrt{Hz}$ Typical
    (R_{MR} = 25Ω, I_{MR} = 13.5mA)
  - High Bandwidth = 220 MHz Typical
    (R_{MR} = 30Ω, -3dB)
  - Power Supply Rejection Ratio = 60 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally

- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 63 mA Range
  - Rise Time = 1.5 ns Typical
    (R_H - 20Ω, L_H = 180 nH, I_W = 30 mA)
  - Multi-Channel Servo Write

BLOCK DIAGRAM



DESCRIPTION

The VM61852/4/8 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM61852/4/8 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM61852/4/8 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available in the following channel counts/packages:

- 2-Channel in 24-pin SSOP
- 4-Channel in 38-pin VSOP
- 8-Channel in 48-pin TQFP

Please consult VTC for other channel-count and/or package availability.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Read Bias Current, I_{MR} 20mA
Write Current, I_W 70mA
Input Voltages:
Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
Output Current:
RDP, RDN: I_O ..... -10mA
Junction Temperature, T_{J1} ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
24-lead SSOP ..... TBD°C/W
38-lead VSOP ..... 88°C/W
48-lead TQFP ..... 75°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 10 - 63 mA
Write Head Inductance, L_W ..... 10 - 300 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 6 - 18 mA
Read Head Inductance, L_{MR} ..... 10 - 50 nH
Read Head Resistance, R_{MR} ..... 15 - 50 Ω
Junction Temperature, T_J 0°C to 125°C

OPERATING MODES AND CONTROLS

Serial Interface Controller

The VM61852/4/8 uses a 3-line serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Table 151 for a bit description.

The serial interface has three input lines: SCLK (serial clock), SENA (serial enable) and SDAT (serial data). The SCLK line is used as reference for clocking data into SDAT. The SENA line is used to activate the SCLK and SDAT lines and power-up the associated circuitry.

A complete data transfer consists of a minimum of 8 bits and could contain any number of bits. If more than 8 bits are used, the first (X-8) bits are ignored. The final 8 bits before SENA drops low should consist of three register address bits <A2-A0> and five data bits <D4-D0>; see Figure 104.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data line (SDAT) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for X cycles; on the falling edge of SENA, the data from the previous 8 cycles will be written to the addressed register. SCLK must be kept high until SENA goes low.

Note: If serial register activity is performed during read mode, crosstalk to the reader output may result.

See Table 152 and Figure 105 for serial interface timing information.

Vendor ID Code Function

While in Sleep mode, data will be written to the vendor ID serial register bits (VEN0 and VEN1 [3:<D0-D1>]). When these bits match VTC's vendor ID code (00), the FLT pin will go low.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM61852/4/8 uses the current-bias/current-sensing MR architecture. The magnitude of the bias current ranges from 6 - 18 mA and is governed by the following equation:

$$I_{MR} = 6 + 0.5(k_{IMR}) + 4.5(k_{IMR-range}) \qquad \textit{(eq. 76)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
k_{IMR} represents the MR bias DAC setting (0 to 15).
$k_{IMR-range}$ represents the MR bias range bit (0 or 1).

The bias current levels are also represented in the table below:

Table 144MR Bias Current

IMR3 1:<D3>	IMR2 1:<D2>	IMR1 1:<D1>	IMR0 1:<D0>	IMR-R=0 1:<D4> mA	IMR-R=1 1:<D4> mA
0	0	0	0	6	10.5
0	0	0	1	6.5	11
0	0	1	0	7	11.5
0	0	1	1	7.5	12
0	1	0	0	8	12.5
0	1	0	1	8.5	13
0	1	1	0	9	13.5
0	1	1	1	9.5	14
1	0	0	0	10	14.5
1	0	0	1	10.5	15
1	0	1	0	11	15.5
1	0	1	1	11.5	16
1	1	0	0	12	16.5
1	1	0	1	12.5	17
1	1	1	0	13	17.5
1	1	1	1	13.5	18

A "high" TTL level applied to the R/WN pin and a low level applied to the BIASN pin (along with the appropriate levels on the IDLEN and SLEEPN bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 149).

The output of the read preamp is differential.

Read Bias Enable in Read Mode

Taking the BIASN pin low in read mode enables MR bias current to the selected head.

Taking the BIASN pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

Four bits in register 1 (1:<D3-D0>) represent the binary equivalent of the DAC setting (0-15, MSB first). A fifth bit (1:<D4>) represents a range factor.

GAIN and BOOST Bits

The GAIN bit (4:<D1>) puts the read gain in low range or high range. The BOOST bit (5:<D4>) boosts the read gain by 3 dB at 100 MHz when set to 1.

Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 102 displays the reader output for an uncompensated thermal asperity event.)

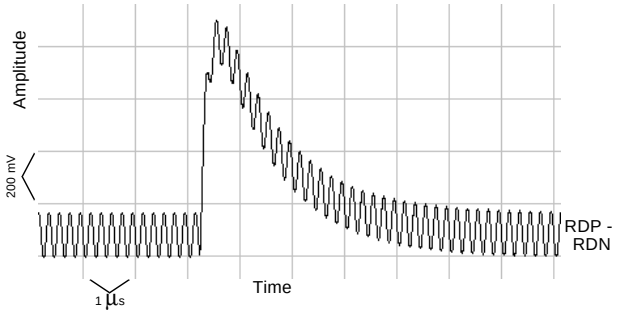


Figure 102 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM61852/4/8 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Programming a non-zero TA threshold value (2:<D3-D0>) allows the TA detection circuitry to detect an asperity event. The threshold for thermal asperity detection is output-referred, has a range of 49 - 385 mV and is governed by the following table:

Table 145Thermal Asperity Detection Threshold

TA3 2:<D3>	*TA2 2:<D2>*	*TA1 2:<D1>*	*TA0 2:<D0>*	*TA Threshold (mV)*
0	0	0	0	OFF
0	0	0	1	49
0	0	1	0	53
0	0	1	1	57
0	1	0	0	63
0	1	0	1	70
0	1	1	0	78
0	1	1	1	91
1	0	0	0	105
1	0	0	1	123
1	0	1	0	146
1	0	1	1	175
1	1	0	0	210
1	1	0	1	256
1	1	1	0	312
1	1	1	1	385

Reporting

Thermal asperity events can be reported on the FLT pin by setting the TAFLTN bit (5:<D1>) low. When reporting is enabled on the FLT pin, a thermal asperity event will be reported as a low level on the FLT pin. Setting this bit high disables TA output on the FLT pin.

Compensation

The TA compensation mode selection bits (4:<D4-D3>) determine which compensation mode is initiated if a thermal asperity is detected; see the table below:

Table 146TA Compensation Mode Selection

TACM1 4:<D4>	*TACM0 4:<D3>*	*Mode*
0	0	Off
0	1	Adaptive
1	0	Fast (5 MHz)
1	1	Fast (10 MHz)

Note: Setting the compensation mode to Off makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the corner frequency movement.

Fast Recovery

When activated, Fast Recovery Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 5 MHz (or 10 MHz) until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 103).

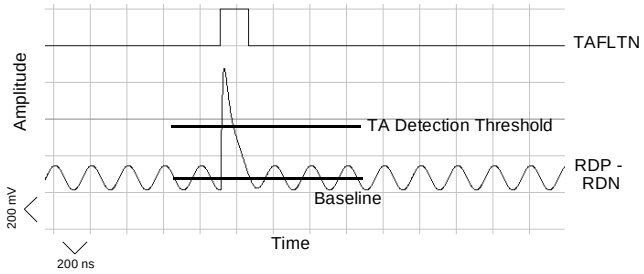


Figure 103 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

Adaptive Compensation

With adaptive compensation the fast mode is invoked linearly in proportion to the amplitude of the asperity event.

Note: When selected, adaptive compensation is automatically invoked regardless of whether the programmed detection threshold value has been exceeded.

MR Measurement / Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (4:<D2>) allows the digital buffered head voltage (DBHV) to be represented on the FLT pin.

The FLT output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 350mV and 450mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Analog Buffered Head Voltage (ABHV)

Setting the ABHV bit high (5:<D0>) allows an amplified representation of the MR bias voltage to be presented on the ABHV pin. This voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} x R_{MR}) \quad \textit{(eq. 77)}$$

If the ABHV bit is not set, the ABHV pin is high-Z.

Fault Detection

Setting the MRMEAS bit low (4:<D2>) allows the fault status (FLT) to be represented on the FLT pin.

In the read mode, a low on the FLT line (open collector with internal 20kΩ pull-up resistor) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- MR Open Head
- Thermal Asperity event (if enabled)

When an MR open head fault condition is detected, the MR head voltage is clamped to provide MR open-head protection (until another head is selected or a mode change is initiated) The user should provide at least a 25µs delay when switching from an open-head to a connected-head. This allows the clamping head voltage to settle to a safe value from the open head event.

Write Mode

In the write mode, the circuit operates as a thin-film write-current switch, driving the thin-film write element of the MR head.

The magnitude of the write current ranges from 10 - 63 mA. The following equation governs the write current magnitude:

$$I_W = 10 + 3.3(k_{IW}) + Range \quad \textit{(eq. 78)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 7).
"Range" represents an additional 0mA, 15mA or 30mA; see the table below.

Table 147Write Current Range Selection

IWR1 3:<D4>	*IWR0 3:<D3>*	*Write Current Range Factor*
0	0	Range 0 - Add 0 mA
0	1	Range 1 - Add 15mA
1	0	
1	1	Range 2 - Add 30mA

The write current levels are also represented in the table below:

Table 148Write Current

IW2 3:<D2>	*IW1 3:<D1>*	*IW0 3:<D0>*	*Range 0 mA*	*Range 1 mA*	*Range 2 mA*
0	0	0	10	25	40
0	0	1	13.3	28.3	43.3
0	1	0	16.6	31.6	46.6
0	1	1	19.9	34.9	49.9
1	0	0	23.2	38.2	53.2
1	0	1	26.5	41.5	56.5
1	1	0	29.8	44.8	59.8
1	1	1	33.1	48.1	63.1

A "low" TTL level applied to R/WN (along with the appropriate levels on the IDLEN and SLEEPN bits) places the preamp in the write mode (see Table 149). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 106.

Write Current DAC

Three bits in register 3(3:<D2-D0>) represent the binary equivalent of the DAC setting (0-7, MSB first). Fourth and fifth bits (3:<D4-D3>) represent two additional range factors.

Read Bias Enable in Write Mode

Taking the BIASN pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal "read" state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the BIASN pin high in write mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

Fault Detection

Setting the MRMEAS bit low (4:<D2>) allows the fault status (FLT) to be represented on the FLT pin.

In the write mode, a low on the FLT line (open collector with internal 20kΩ pull-up resistor) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Write head shorted to ground
- Low power supply voltage
- Insufficient write data transition frequency (> 500ns between transitions)

Two transitions on pin WDX, after the fault is corrected, may be required to clear the fault line.

When a low supply fault condition is detected, the write current source internal to the chip is shut down and no current flows to any head.

Note: There is no MR open head detection, reporting or protection in Write mode when the BIASN pin is low.

Servo Write Mode

In the servo write mode, odd channels, even channels or all channels of the VM61852/4/8 are written simultaneously.

Servo mode is initiated with a four-step process (see Table 149):

15) Select Read mode (take R/WN high)
16) Set the Servo bit (2:<D4>) to a "1"
17) Force the FLT pin to 2V above V_{CC} with a minimum of 6mA
18) Initiate Servo mode (take R/WN low)

The HS0 - HS3 register bits (0:<D3-D0>) determine which heads are written (see Table 150). Write mode fault circuits are disabled.

Note: It is the customer's responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Idle Mode

Setting the IDLEN bit low (0:<D4>) places the preamp in Idle mode (see Table 149). Only the serial register, bias circuitry and dummy head cell remain active.

The MR bias current source is active and the MR bias current is directed to an internal dummy head. The MR bias current control loop is active and the reader output is clamped at the common-mode voltage.

Fault Detection

Setting the MRMEAS bit low (4:<D2>) allows the fault status (FLT) to be represented on the FLT pin.

In Idle mode, a low on the FLT line (open collector with internal 20kΩ pull-up resistor) indicates a fault condition. The fault condition can be triggered by the following condition:

- Low power supply voltage

Note: There is no MR open head detection, reporting or protection in Idle mode when the BIASN pin is low.

Sleep Mode

Setting the SLEEPN bit low (4:D0>) places the preamp in Sleep mode (see Table 149). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Note: There is no MR open head detection, reporting or protection in Sleep mode when the BIASN pin is low.

Table 149Mode Select

R/WN	*BIASN*	*Servo* [1]	*IDLEN 0:<D4>*	*SLEEPN 4:<D0>*	*MODE*
1	1	X	1	1	Read Bias Disabled [2]
1	0	X	1	1	Read Bias Enabled
0	1	0	1	1	Write Bias Disabled [2]
0	0	0	1	1	Write Bias Enabled
0	X	1	1	1	Servo
X	X	X	0	1	Idle Bias Disabled [2]
X	X	X	X	0	Sleep

1. In this table a “1” in the Servo column represents a combination of the SERVO bit being set to a “1” in the serial register (2:<D4>) and sourcing a minimum of 6mA into the FLT pin with a compliance voltage of greater than VCC + 1.5V.
2. MR bias current directed to an internal dummy head.

Table 150Head Select

HS3 0:<D3>	*HS2 0:<D2>*	*HS1 0:<D1>*	*HS0 0:<D0>*	*HEAD 2 Chnl (Normal)*	*HEAD 4 Chnl (Normal)*	*HEAD 8 Chnl (Normal)*	*HEADS (Servo)*
0	0	0	0	0	0	0	none
0	0	0	1	1	1	1	odd[1]
0	0	1	0	N/A	2	2	none
0	0	1	1	N/A	3	3	none
0	1	0	0	Idle	Idle	4	none
0	1	0	1	Idle	Idle	5	all[1]
0	1	1	0	Idle	Idle	6	none
0	1	1	1	Idle	Idle	7	even[1]
1	X	X	X	Idle	Idle	Idle	none

1. 4-channel devices must select the appropriate head (1=odd, 5=all, 7=even) to servo write head combinations, regardless of the head’s presence.

PIN FUNCTION LIST AND DESCRIPTION

Symbol	*Input/ Output* [1]	*Description*
R/WN	I	Read/Write: A TTL low level enables write mode. Pin defaults high (read mode) with an internal 9.8K pull-up resistor.
BIASN	I	Bias Enable: A TTL low level enables MR bias current to the selected head. A TTL high level directs bias current to a dummy head. Pin defaults low with an internal 39K pull-down resistor.
FLT	O	Fault: Open collector output with internal 20kΩ pull-up resistor. Setting the MRMEAS bit high (4:<D2>) allows the digital buffered head Voltage (DBHV) to be represented on the FLT pin. Setting the MRMEAS bit low (4:<D2>) allows the fault status (FLT) to be represented on the FLT pin. Setting the TAFLTN bit low (5:<1>) allows a thermal asperity fault to be represented on the FLT pin. In Read, Write and Idle modes, a TTL low level indicates a fault.
ABHV	O	Analog Buffered Head Voltage: Setting the ABHV bit high (5:<D0>) allows the analog buffered head Voltage (ABHV) to be represented on the ABHV pin.
WDX, WDY	I	Differential Pseudo-ECL Write Data Inputs.
HR0P-HR7P	I	MR Head Connections: Positive end.
HW0X-HW7X	O	Thin-Film Write Head Connections: Positive end.
HW0Y-HW7Y	O	Thin-Film Write Head Connections: Negative end
RDP, RDN	O	Read Data: Differential read signal outputs.
CAPH/CAPL	-	Compensation Capacitor: 10nF for the MR bias current loop.
HCOM	-	Head Common: Common return for MR heads and external capacitor.
GND	-	Ground
VCC	-	+5.0V Supply
SENA	I	Serial Enable: Serial port enable; see Figure 105.
SCLK	I	Serial Clock: Serial port clock; see Figure 105.
SDAT	I	Serial Data: Serial port data; see Figure 105.

1. I = Input, O = Output

SERIAL INTERFACE

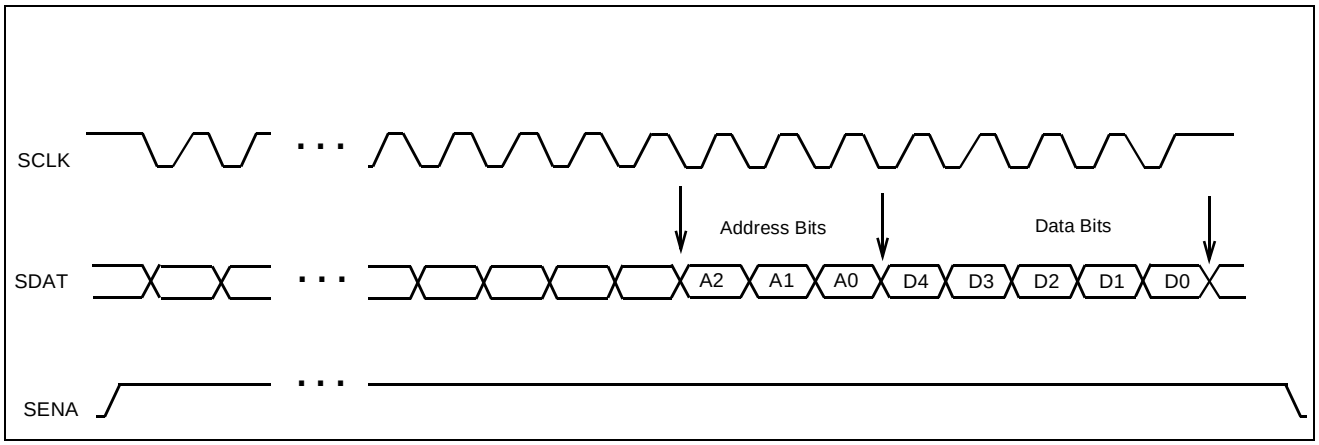


Figure 104 Serial Port Protocol

Table 151Serial Interface Bit Description

Function	*Register #*	*Address Bits*			*Data Bits*				
		<A2>	*<A1>*	*<A0>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Head Select / Idle	0	0	0	0	IDLEN	HS3	HS2	HS1	HS0
MR Bias Current DAC / Range	1	0	0	1	IMR-R	IMR3	IMR2	IMR1	IMR0
Thermal Asperity DAC / Servo Enable	2	0	1	0	SERVO	TA3	TA2	TA1	TA0
Vendor ID / Write Current DAC / Write Current Range	3	0	1	1	IW-R1	IW-R0	IW2	IW1 / VEN1	IW0 / VEN0
Sleep / Gain / MR Head Measurement (DBHV) / Thermal Asperity Compensation Mode	4	1	0	0	TACM1	TACM0	MRMEAS	GAIN	SLEEPN
ABHV / Thermal Asperity Fault Output / Boost	5	1	0	1	BOOST	1	1	TAFLTN	ABHV

1. Reserved

Table 152Serial Interface Timing Parameters

Description	*Symbol*	*Min*	*Nom*	*Max*	*Units*
Serial Clock (SCLK) Rate				44	MHz
SENA to SCLK delay	T_{sens}	7.5			nS
SDAT setup time	T_{ds}	5			nS
SDAT hold time	T_{dh}	5			nS
SCLK cycle time	T_{c}	23			nS
SCLK high time	T_{ckh}	7.5			nS
SCLK low time	T_{ckl}	7.5			nS
SENA hold time	T_{shld}	7.5			nS
SCLK rise and fall time	T_{ckr}			3	nS

Note: SENA assertion level is high.

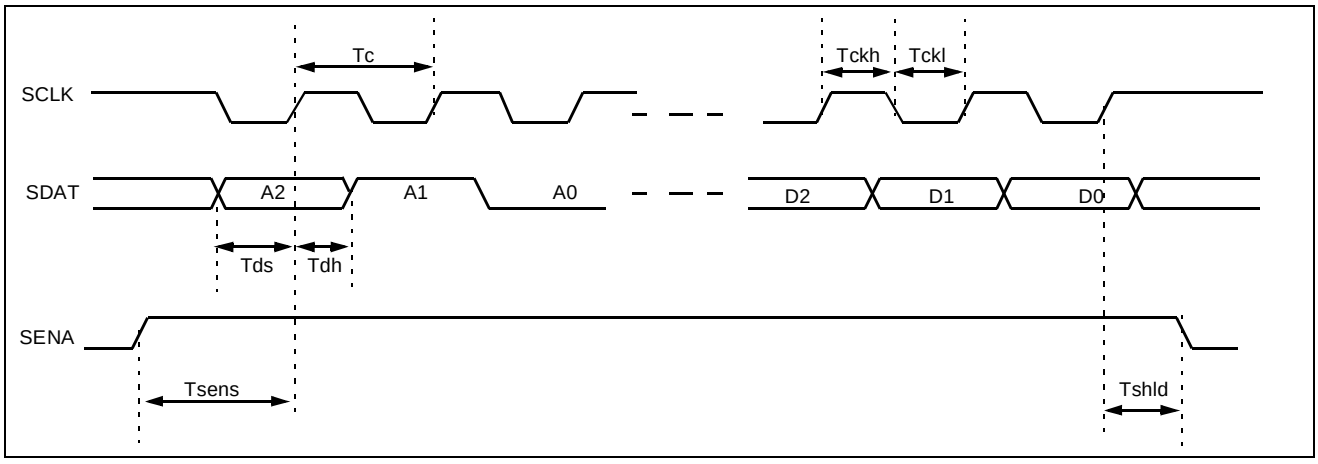


Figure 105 Serial Port Timing

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
V_{CC} Power Supply Current	I_{CC}	Read Mode (See Formula 1 below.)		67	78	mA
		Read Mode, Bias disabled		43	52	
		Write Mode (See Formula 2 below.)		80	90	
		Write Mode, Bias enabled (See Formula 3 below.)		99	111	
		Idle Mode		30	36	
		Sleep Mode, Vendor ID = '00'		3	5	
		Servo Mode, I_s = 25mA, Bank of four heads (See Formula 4 below.)		133	156	
		Servo Mode, I_s = 25mA, Bank of eight heads (See Formula 4 below.)		243	282	
Power Dissipation	P_d	Read Mode		306	395	mW
		Read Mode, Bias disabled		215	286	
		Write Mode		399	497	
		Write Mode, Bias enabled		495	612	
		Idle Mode		150	198	
		Sleep Mode		15	28	
		Servo Mode, I_s = 25mA, Bank of four heads		665	858	
		Servo Mode, I_s = 25mA, Bank of eight heads		1215	1555	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.2		V_{CC} - 0.5	V
		TTL	2.0		V_{CC} + 0.3	
Input Low Voltage	V_{IL}	PECL	V_{IH} - 0.9		V_{IH} - 0.55	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V	-100		100	
		R/WN	-360			
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-80		80	
		R/WN	-640			
PECL Differential Swing	P_{DS}		550		900	mV

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, I_W = 31.6mA.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Fault Output High Current	I_{OH}	V_{OH} = 5V			50	µA
Fault Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.5	V
V_{CC} Fault Threshold	V_{DTH}	I_w < 200µA, Fault detected	3.6	3.8	4.0	V
	V_{UTH}	Fault removed	3.9	4.1	4.3	
V_{CC} Fault Threshold Hysteresis	V_{HTH}		200	300	400	mV

Formulas:

5) Typ: 53 + (1.05 x I_{MR}) Max: 63 + (1.1 x I_{MR})
6) Typ: 45 + (1.1 x I_W) Max: 54 + (1.15 x I_W)
7) Typ: 50 + (1.1 x I_W) + (1.05 x I_{MR}) Max: 60 + (1.15 x I_W) + (1.1 x I_{MR})
8) Typ: 23 + (1.1 x Hds x I_S) Max: 28 + (1.18 x Hds x I_S)

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, R_{MR} = 30Ω.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MR Head Current Range	I_{MR}		6	13.5	18	mA
MR Head Current Accuracy	ΔI_{MR}	6mA < I_{MR} < 18mA	-5		5	%
Unselected MR Head Current					100	µA
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, R_L(RDP, RDN) = 1kΩ, I_{MR} = 13.5mA, R_{MR} = 30Ω, Gain bit = 0	170	200	230	V/V
		Gain bit = 1	210	250	290	
Buffered Head Voltage Gain	A_{BHV}	Output Range = A_{BHV}·I_{MR}·R_{MR} = 500mV to 2.5V; BHV Load Current = 0-150µA	4.5	5.0	5.5	V/V
Passband Upper Frequency Limit	f_{HR}	R_{MR} = 30Ω; L_{MR} = 20nH; -3dB; Gain bit = 0	165	220		MHz
		-1dB, Gain bit = 0	100			
Gain Boost	BST	f = 100MHz, Gain bit = 0, Boost bit = 1		3		dB
Passband Lower -3dB Frequency Limit	f_{LR}	R_{MR} = 30Ω, Gain bit = 0		0.5	0.6	MHz
Equivalent Input Noise (sense amp only)	e_{na}	R_{MR} = 25Ω; I_{MR} = 13.5mA; 1 < f < 50 MHz		0.50		nV/√Hz
Bias Current Noise (referred to Input)	i_n	I_{MR} = 13.5mA		16		pA/√Hz
Equivalent Input Noise (total)	e_n	R_{MR} = 25Ω; I_{MR} = 13.5mA; 1 < f < 50 MHz		0.67		nV/√Hz
Input Resistance	R_{IN}	I_{MR} = 13.5mA		2.6	4	Ω
Input Capacitance	C_{IN}				20	pF

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 13.5mA, R_{MR} = 30Ω.

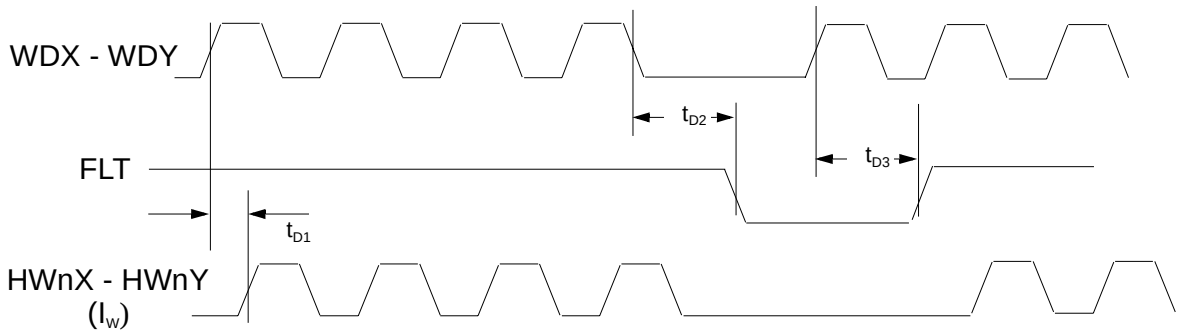
Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Integrated Noise	e_{in}	R_{MR} = 25Ω; I_{MR} = 13.5mA; L_{MR} = 20nH; 1 < f < 140 MHz		8.8		µV
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz, Gain bit = 0		5		mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or GND, I_{MR} = 13.5mA, R_{MR} = 30Ω, 1 < f < 100 MHz		60		dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 1 < f < 100 MHz	45			dB
Output Offset Voltage	V_{OS}	I_{MR} = 13.5mA, R_{MR} = 30Ω	-50		50	mV
Common Mode Output Voltage	V_{OCM}	Read Mode, Write Mode		V_{CC} - 2.5		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)	-150		150	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode			50	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	1.5			mA
Total Harmonic Distortion	THD	f = 20 Mhz, V_{IN} = 1 mV peak-to-peak			1	%
MR Head Measurement Threshold (Head Resistance / DBHV)		Low Threshold [1]	330	350	370	mV
		High Threshold [2]	420	450	480	
Thermal Asperity Detection Range	V_{TATH}	DC level in RDX/RDY over baseline	49		385	mV
Thermal Asperity Detection Threshold Tolerance	ΔV_{TATH}	DAC setting	-15		15	%
MR Head Voltage	V_{MR}	$I_{MR} \cdot R_{MR}$			0.6	V
Overshoot on I_{MR} during Idle-to-Read Transitions	I_{MROV}	0.25V < V_{MR} < 0.6V		6		%
Clamping Threshold for Open MR Head				820		mV
Clamping Threshold for Shorted MR Head				50		mV

1. Fault switching from low to high.
2. Fault switching from high to low.

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 31.6mA, L_H = 180nH, R_H = 20Ω, f_{DATA} = 5MHz.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Write Current Range	I_W	(base to peak)	10		63	mA
Write Current Tolerance	ΔI_W	10mA < I_W < 63mA	-8		8	%
Servo Current Range	I_S	base to peak, 8 heads	10		30	mA
		base to peak, 4 heads	10		60	
		base to peak, 2 heads	10		60	
Servo Current Tolerance	ΔI_S	10mA < I_S < 40mA	-8		8	%
Servo Enable Current at the FLT pin	I_{SE}	V_{CC} + 2.0V < Voltage at FLT pin	6		13	mA
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V	6	7.5		V_{pp}
Unselected Head Current	I_{UH}				50	μA_{pk}
Time between Write Data Transitions for Safe Condition	t_{SAFE}	FLT = High			500	ns
Open Head Detection	R_{OHD}	Detect Open Head	1000			Ω
	V_{OHD}	Do Not Detect Open Head, $I_W \cdot R_H$			2	V
Shorted Head Detection	R_{SHD}	Detect Shorted Head (to GND)			5	Ω
		Do Not Detect Shorted Head	1000			



Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

Figure 106 Write Mode Timing Diagram

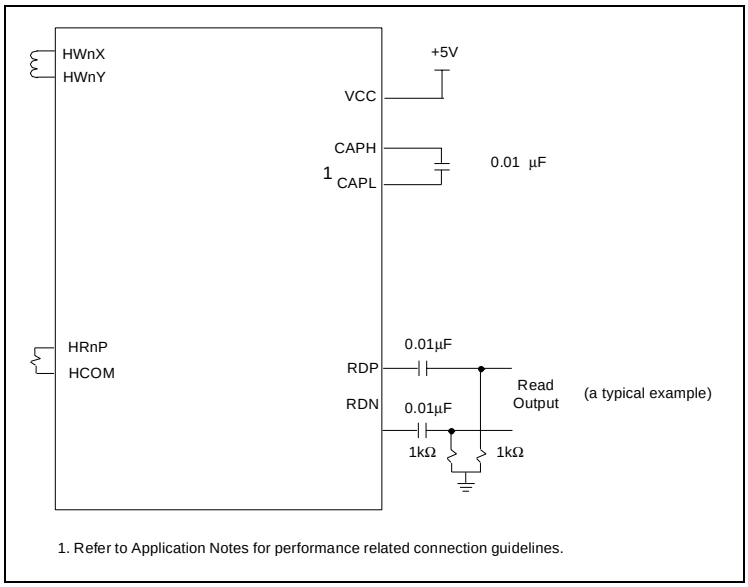
SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified:
I_W = 31.6mA, L_H = 180nH, R_H = 20Ω, f_{DATA} = 5MHz, I_{MR} = 13.5mA, R_{MR} = 30Ω., Bias enabled.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Read (R/WN) to Write Mode	t_{RW}	To 90% of write current		50	70	ns
Write (R/WN) to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value[1]		300	400	ns
Idle to Read Mode	t_{IR}	RDP/RDN to within ±30mV of final value		6	10	µs
Sleep to Read Mode	t_{SR}	RDP/RDN to within ±30mV of final value		30	50	µs
Head Select to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode		6	10	µs
Read to Idle	t_{RI}	To 10% of read envelope		0.16	0.5	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		6	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, Lh = 0nH, Rh = 0Ω.		70	200	ps
Rise/Fall Time	t_r / t_f	10 - 90%		1.5	1.8	ns
FLT delay, Write Safe to Unsafe	t_{D2}		0.5		3.6	µs
FLT delay, Write Unsafe to Safe	t_{D3}	10KΩ pull-up resistor			1.3	µs
TA FLT delay		TA detected to FLT pin low			0.2	µs

1. BIASN pin active low for 10 µs preceding R/WN transition.

TYPICAL APPLICATION CONNECTIONS



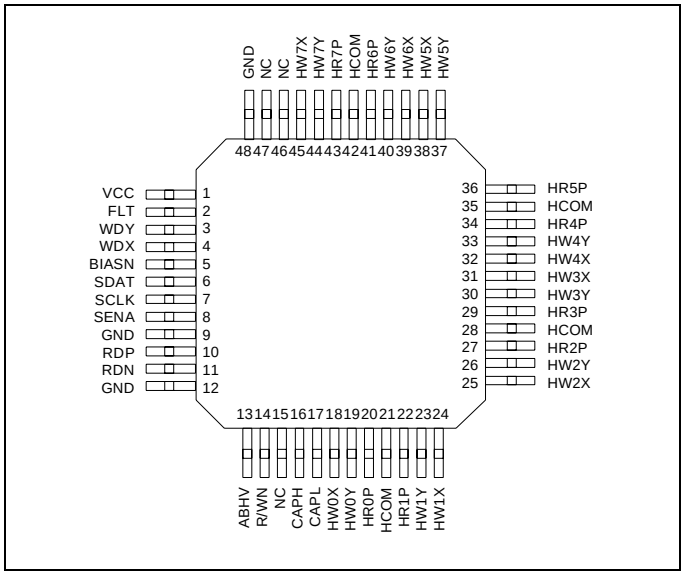
Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Minimizing parasitics at the CAPH/CAPL nodes is vital. Place a high quality (low resistance, low inductance) capacitor as close to the pins/pads as possible.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins/pads:
  VCC - GND
- For maximum stability, place the decoupling capacitors as close to the pins/pads as possible.
- For optimal performance, CAPL should connect to the same common return to which the read heads (HCOM) are connected.

VM61852/4/8

8-CHANNEL CONNECTION DIAGRAM



8-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

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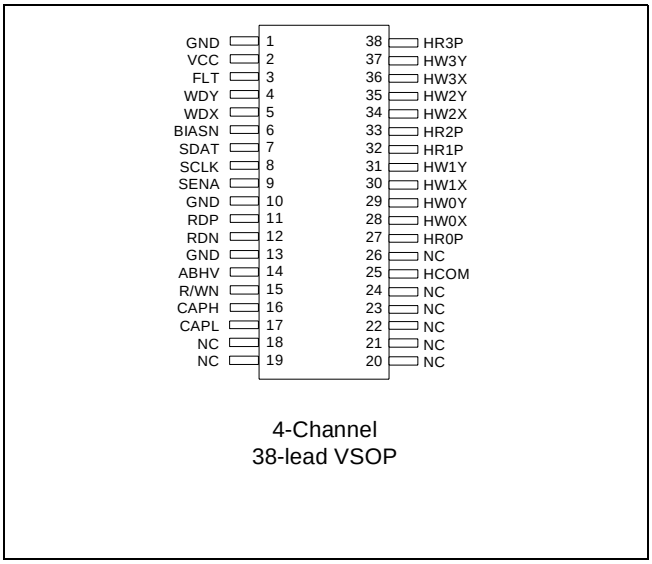
VM61852/4/8

4-CHANNEL CONNECTION DIAGRAM



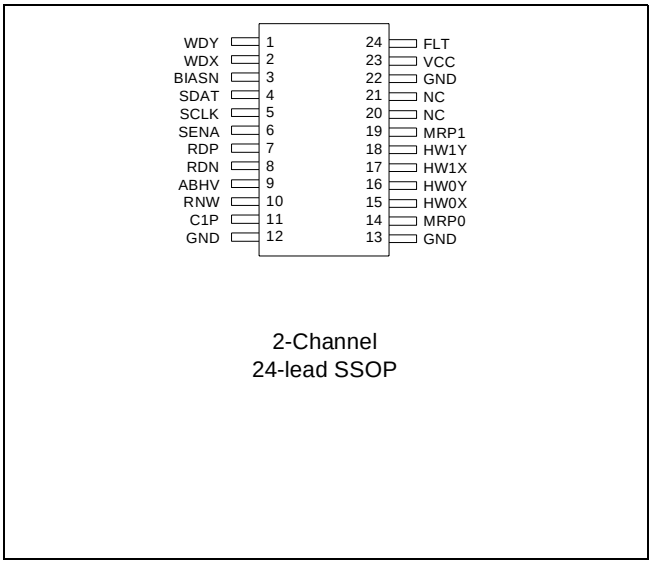
4-Channel
38-lead VSOP

Specific Characteristics

See the general data sheet for common specification information.

VM61852/4/8

2-CHANNEL CONNECTION DIAGRAM



2-Channel
24-lead SSOP

Specific Characteristics

See the general data sheet for common specification information.

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VTC Inc.
Value The Customer™

VM6189 Series

PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/ WRITE PREAMPLIFIER with SERVO WRITE

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR Heads
  - 3-Line Serial Interface with Readback (Provides Programmable Bias Current, Write Current, Write Damping Resistance, Head Selection, Read Gain, Thermal Asperity, and Servo Operation)
  - Bandwidth = 160 MHz Min (R_{MR} = 50Ω, L_{MR} = 0nH)
  - Operates from a Single +5 Volt Power Supply
  - Fault Detection Capability
  - Available as a 4- or 8-Channel Device
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 3.05 - 12.35 mA Range
  - Programmable Read Voltage Gain (4 Channel: 138 V/V or 220 V/V Typical, R_{MR} = 50Ω, 8 Channel: 122 V/V or 195 V/V Typical, R_{MR} = 50Ω)
  - Thermal Asperity Detection and Fast Recovery Compensation
  - Digital and Analog Buffered Head Voltage (BHV) Measurement Modes
  - Input Noise = 0.8 nV/√Hz Typical (R_{MR} = 50Ω, I_{MR} = 8mA)
  - Power Supply Rejection Ratio = 45 dB (1 < f < 100 MHz)
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 17 - 52 mA Range
  - Rise Time = 1.7 ns Typical (R_H - 16Ω, L_H = 130 nH, R_D = 600Ω, I_W = 30 mA)
  - Multi-Channel Servo Write
  - 3V CMOS or 5V TTL compatible Write Data Inputs

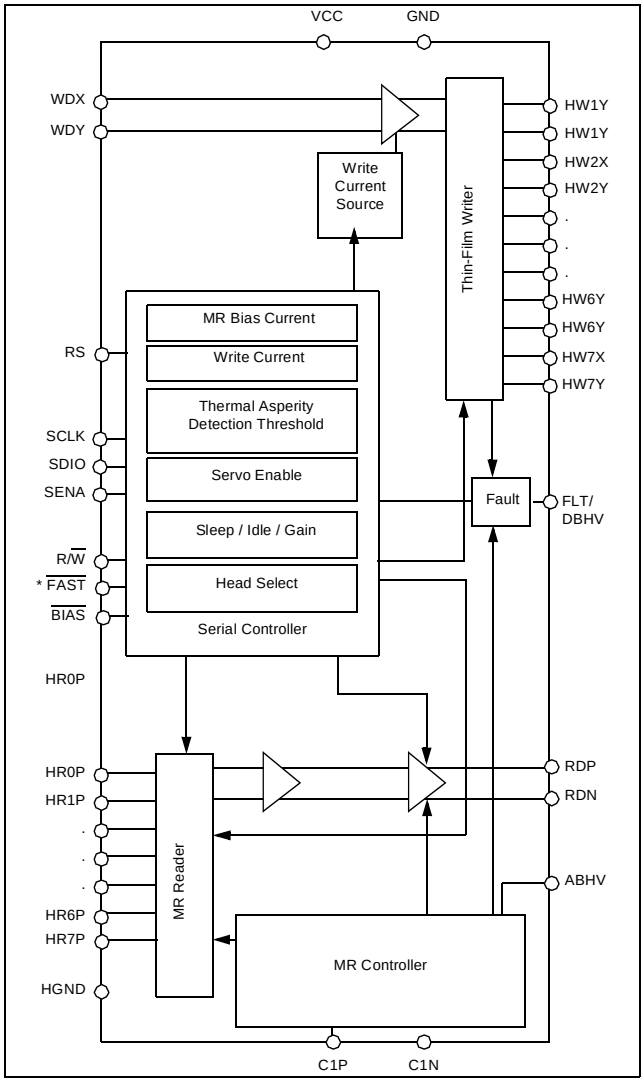
DESCRIPTION

The VM6189 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM6189 operates from a single +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM6189 is achieved through a 3-line, 16-bit serial interface. Programmable parameters include MR bias current, write current, head selection, damping resistance, reader gain, thermal asperity detection threshold and servo operation.

Available in 4- and 8-channel options. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



* This pin available only on 8-Channel device

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 16mA

Write Current, I_W 55mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C

Storage Temperature, T_{stg} ..... -65°C TO 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 17 - 52 mA
Write Head Inductance, L_W ..... 85 - 180 nH
Write Head Resistance, R_W ..... 7 - 21 Ω
Read Bias Current, I_{MR} ..... 3.05 - 12.35 mA
Read Head Inductance, L_{MR} ..... 0 - 100 nH
Read Head Resistance, R_{MR} ..... 30 - 81 Ω
Junction Temperature, T_J ..... 0°C to 125°C

OPERATING MODES AND CONTROLS

Serial Interface Controller

The VM6189 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 158 and 159 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SDCLK and SDIO lines and power-up the associated circuitry. The bidirectional SDIO line supports full readback.

16 bits constitutes a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0>, three preamp select bits <A3-A1> (which must be <001> for this preamp), and four register address bits <A7-A4>. The second 8 bits <D7-D0> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register. During a read sequence, SDIO will begin outputting data on the falling edge of the 9th cycle. At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and may result in reader performance degradation.

See Table 161 and Figures 110 and 111 for serial interface timing information.

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier that senses resistance changes in the MR element which correspond to magnetic field changes on the disk.

The VM6189 uses the current-bias/current-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{6.1}{R_{RS}} + 0.3(k_{IMR}) \qquad \textit{(eq. 79)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).

R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ).

k_{IMR} represents the MR bias DAC setting (0 to 31).

A "high" TTL level applied to the R/$\overline{W}$ pin and a "low" TTL level applied to the $\overline{BIAS}$ pin (along with the "high" levels on the $\overline{IDLE}$ and $\overline{SLEEP}$ serial register bits) places the preamp in the read mode and activates the read unsafe detection circuitry (see Table 155).

The output of the read preamp is differential.

Read Bias Enable in Read Mode

Taking the $\overline{BIAS}$ pin low in read mode enables MR bias current to the selected head.

Taking the $\overline{BIAS}$ pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

MR Bias DAC

The 5 bits in register 1 (1:<D3-D7>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Thermal Asperity Detection and Compensation

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. (Figure 107 displays the reader output for an uncompensated thermal asperity event.)

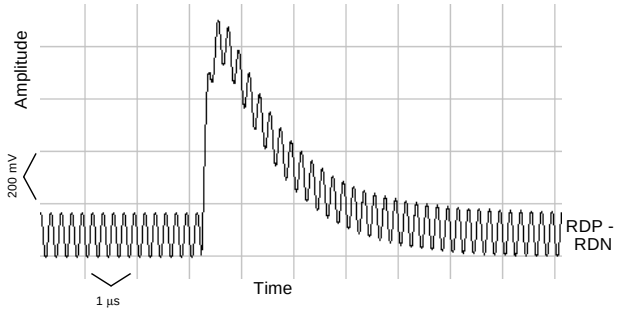


Figure 107 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM6189 implements both a programmable detection threshold and fast recovery compensation for such disturbances.

Detection

Setting the TADET bit high (3:<D3> = 1) allows the TA detection circuitry to detect an asperity event (based on the programmable threshold) and report this as a fault condition on the fault line. Setting this bit low disables TA detection.

The threshold for thermal asperity detection has a range of 50 to 800 mV and is governed by the following equation:

$$V_{TADT} = 50(1 + k_{TADT}) \qquad \textit{(eq. 80)}$$

V_{TADT} represents the TA threshold (output-referred in mVpk; ±15%).

k_{TADT} represents the TA DAC setting (0-15).

Fast Recovery Compensation

A Fast Recovery mode is initiated in three ways:
(See Table 156 for a diagram of the modes)

19) Setting the Fast Recovery (FR) bit high (4:<D5> = 1).

20) If both the FR and TADET (3:<D3>) bits are high, a thermal asperity will initiate fast mode.
Note: The thermal asperity must be positive.

21) Taking the $\overline{\text{FAST}}$ pin low (8 channel only). This overrides the FR serial bit and initiates the Fast Recovery mode regardless of the detection circuitry.

Note: This configuration makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the corner frequency movement.

When activated, Fast Recovery Compensation raises the nominal 700 KHz lower -3dB corner frequency to approximately 3.5 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 108).

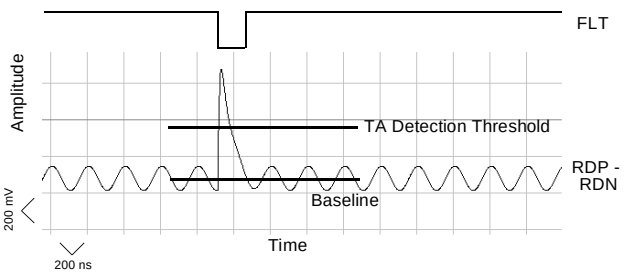


Figure 108 TA Detection and Compensation

Analog Buffered Head Voltage (ABHV)

Setting the MRMEAS bit high (4:<D3>) allows an amplified representation of the MR bias voltage to be presented on the ABHV pin. This voltage is defined by the equation:

$$V_{BHV} = ABHV(I_{MR} \times R_{MR}) + V_{BOS} \qquad \textit{(eq. 81)}$$

ABHV (Analog Buffered Head Voltage Gain) = 5 V/V Typical.
I_{MR} represents the bias current flowing to the MR element (in mA).
V_{BOS} represents the Output Offset Voltage.

If the MRMEAS bit is set low, the ABHV pin goes into a high impedance state.

Digital Buffered Head Voltage (DBHV)

Setting the MRMEAS bit high (4:<D3>) allows the digital buffered head voltage (DBHV) to be represented on the FLT/DBHV pin.

The DBHV output is high when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to fall within the comparator thresholds of 380mV and 520mV. The output is low when the $I_{MR} \cdot R_{MR}$ product falls above or below this range.

Fault Detection

Setting the MRMEAS bit low (4:<D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the read mode, a low on the FLT line (open collector) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Shorted MR element
- Low power supply voltage
- Thermal asperity detected (reported when enabled with the TADET bit (3:<D3> = 1))
- Open MR head
- HS2 selected (current diverted to dummy head) - 4 channel only.

Note: An MR open head fault condition is detected but not reported on the FLT line for 4 to 6 µs. The voltage on the loop-compensation capacitor (C1) is clamped to provide MR open head protection (until another head is selected or a mode change is initiated).

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2kΩ resistor (connected between pin RS and ground). The following equation governs the write current magnitude:

$$I_W = \left(\frac{34}{R_{RS}} + [1.13 \cdot k_{IW}]\right)\left(\frac{1}{1 + \frac{R_H}{R_D}}\right) \qquad \textit{(eq. 82)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 31).
R_D represents the damping resistance (in Ω).
R_H represents the series head resistance (in Ω).
R_{RS} represents the equivalent resistance between the RS pin and ground (in kΩ)

A "low" TTL level applied to R/$\overline{\text{W}}$ (along with "high" levels on the IDLE and SLEEP serial register bits) places the preamp in the write mode (see Table 155). The write data (PECL) signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 112.

Write Current DAC

The 5 bits (2:<D0-D4>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Write Current Damping

The 2 bits (3:<D1-D2>) represent the programmable damping resistance. The settings are defined in Table 153. The default setting is 670W.

Table 153Write Current Damping Resistance

DR1 3:<D2>	*DR0 3:<D1>*	*Resistance*	*Rise/Fall Time [1]*	*Overshoot*
0	0	670Ω	1.7 ns	30%
0	1	260Ω	1.8 ns	22%
1	0	160Ω	1.9 ns	16%
1	1	120Ω	2.1 ns	10%

1. I_W = 30mA (DAC=13), L_h = 130nH, R_h = 16Ω

Read Bias Enable in Write Mode

Taking the $\overline{\text{BIAS}}$ pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal "read" state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the $\overline{\text{BIAS}}$ pin high in write mode shuts down the reader.

Fault Detection

Setting the MRMEAS bit low (4:<D3>) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the write mode, a high on the FLT line (open collector) indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Open write head
- Low power supply voltage (write current disabled)
- Write head shorted to ground
- HS2 selected (write current disabled) - 4 channel only.
- Low write data frequency

If a low power supply or HS2 select fault condition is detected, the write current source internal to the chip is shutdown and no current flows to any head for the duration of the fault.

Servo Write Mode

In the servo write mode all channels of the VM6189 may be written simultaneously.

Setting both the BANK0 and BANK1 bits (2:<D7> and 4:<D6>) to "1" (along with appropriate levels on the R/$\overline{W}$ pin and $\overline{IDLE}$ and $\overline{SLEEP}$ serial register bits) places the preamp in servo write mode (see Tables 154 and 155). Setting the HS0 - HS1 register bits (1:<D0-D1>) to "1" initiates a servo write to all heads (see Table 154). A combination of "0" and "1" on the HS0-HS1 bits initiates a 4 head bank servo operation for the 8-channel device (see Table 154). All write mode fault circuits are disabled, except for low power supply voltage.

Note: It is the customer's responsibility to make sure the thermal constraints of the package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo active duty cycle.)

Table 154Servo Mode Head Select

BANK1 4:<D6>	BANK0 2:<D7>	HS1 1:<D1>	HS0 1:<D0>	Heads	
				4-Channel	8-Channel
0	0	X	X	Normal Operation	
0	1	X	X	Normal Operation	
1	0	X	X	Normal Operation	
1	1	0	0	N/A [1]	N/A [1]
1	1	0	1	N/A [1]	4, 5, 6 and 7
1	1	1	0	N/A [1]	0, 1, 2, and 3
1	1	1	1	0-3 (All Heads)	0-7 (All Heads)

1. N/A = No head current and no faults reported.

Fault Detection

Setting the MRMEAS bit low (4:<D3> = 0) allows the fault status (FLT) to be represented on the FLT/DBHV pin.

In the servo write mode, a high on the FLT line (open collector) indicates a fault condition. The fault condition is triggered by the following condition:

- Low power supply voltage (write current disabled)

Idle Mode

Setting the $\overline{IDLE}$ bit low (4:D1> = 0) places the preamp in idle mode (see Table 155). The state of the $\overline{BIAS}$ pin determines the state of the MR bias current source.

Bias Enable

Taking the $\overline{BIAS}$ pin low in idle mode activates the MR bias current source. The MR bias current control loop is activated so that the state of the C1 loop capacitor remains near its Read mode operating point, but the reader output remains in its idle state (inactive).

Taking the $\overline{BIAS}$ pin high in idle mode disables the MR bias current source and inactivates the MR bias control loop.

Sleep Mode

Setting the $\overline{SLEEP}$ bit low (4:<D0> = 0) places the preamp in Sleep mode (see Table 155). All circuits are inactivated to minimize power dissipation. Only the serial register remains active.

Table 155Mode Select

Servo [1]	$\overline{BIAS}$	R/$\overline{W}$	$\overline{Idle}$ 4:<D1>	$\overline{Sleep}$ 4:<D0>	Mode
X	X	X	X	0	Sleep
X	1	X	0	1	Idle
X	0	X	0	1	Idle Bias Active (dummy head)
X	0	1	1	1	Read Bias Active
X	1	1	1	1	Read Bias Inactive (dummy head)
0	0	0	1	1	Write Bias Active
0	1	0	1	1	Write Bias Inactive
1	X	0	1	1	Servo

1. In this table, a "1" in the Servo column represents a combination of high levels on the BANK0 and BANK1 bits in the serial register (2:<D7> and 4:<D6>). A "0" represents all other combinations of those two bits.

Table 156Thermal Asperity Mode Control

FR 4:<D5>	TADET 3:<D3>	$\overline{FAST}$ [1]	Mode Control	
			Fast Recovery	TA Detection
X	X	0	On	Off/On
0	0	1	Off	Off
0	1	1	Off	On
1	0	1	On	Off
1	1	1	TA Detection triggers Fast Recovery	

1. This pin available only on 8-channel device.

Table 157Head Select (non-servo)

HS2 0:<D2>	HS1 0:<D1>	HS0 0:<D0>	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1 [1]	0	0	4
1 [1]	0	1	5
1 [1]	1	0	6
1 [1]	1	1	7

1. Valid for 8-channel device only (see Fault Detection on page 355).

PIN FUNCTION LIST AND DESCRIPTION

Signal	*Input/ Output* [1]	*Description*
R/$\overline{W}$	I	Read/Write: A TTL low level enables write mode. Pin defaults high with 40kΩ pullup resistor (read mode).
$\overline{BIAS}$	I	Bias Enable: A TTL low level enables MR bias current to the selected head (or to an internal dummy head in idle mode). Pin defaults high with 40kΩ pullup resistor (bias disabled).
FAST	I	Fast Read Enable (8-channel device only): A TTL low level enables Fast Read mode (regardless of the state of the FR serial bit or the thermal asperity detection circuitry. Pin defaults high ($\overline{FAST}$ disabled).
ABHV	O	Analog Buffered Head Voltage: ABHV (Analog Buffered Head Voltage) is represented on the pin when MRMEAS (4:<D3>) is set high. - The preamp drives this pin to an analog voltage representing five times the product of I_{MR}*R_{MR}. When the MRMEAS bit is set low the output goes into a high impedance state.
FLT/DBHV	O	Fault/Digital Buffered Head Voltage: FLT (Fault) is represented on the pin when MRMEAS (4:<D3>) is set low. Output is an open collector. - In Write mode, a high level indicates a fault. - In Read mode, a low level indicates a fault.DBHV (Digital Buffered Head Voltage) is represented on the pin when MRMEAS (4:<D3>) is set high. Pin defaults high (open collector) to prevent accidental write conditions.
WDX, WDY	I	Differential Pseudo-ECL write data inputs.
HR0P-HR7P	I	MR head connections, positive end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end
RDP, RDN	O	Read Data: Differential read signal outputs.
C1P,C1N	-	Compensation capacitor for the MR bias current loop.
HGND	-	Head Ground, common return for MR Heads and C1N.
GND	-	Ground
VCC	-	+5.0V supply
RS	-	Reference Voltage for both MR Bias and Write Current. (External 2kΩ resistor sets reference current for the read and write DACs.)
SENA	I	Serial Enable: Serial port enable signal; see Figures 110 and 111. Pin defaults low with 40kΩ pulldown resistor.
SCLK	I	Serial Clock: Serial port clock; see Figures 110 and 111. Pin defaults low with 40kΩ pulldown resistor.
SDIO	I/O	Serial Data: Serial port data; see Figures 110 and 111. Pin defaults low with 40kΩ pulldown resistor.

1. I = Input pin, O = Output pin

SERIAL INTERFACE

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active.

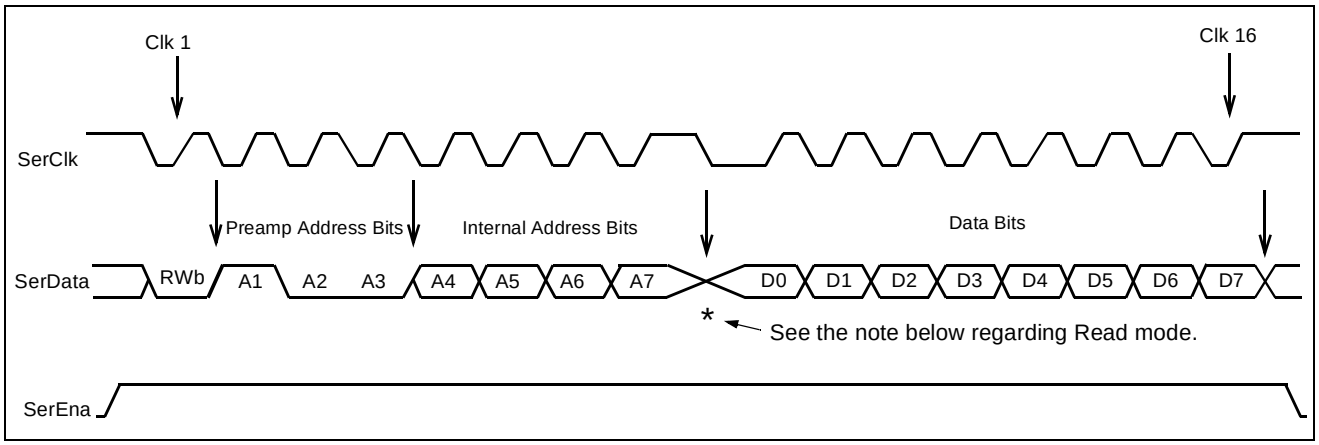
16 bits constitute a complete data transfer. The first 8 bits are write-only and consist of one read/write bit <A0> (high for read, low for write), three preamp select bits <A1-A3> (which must be <001> for this preamp), and four register address bits <A4-A7>. The second 8 bits <D0-D7> consist of data to be written-to or read-from a register.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 158 and 159 for a bit description. See Table 161 and Figures 110 and 111 for serial interface timing information.



* For a read operation, the clock rate can be reduced for one period between the <A7> bit and the <D0> bit to provide sufficient time for the controller to tristate its output (release control of SDIO), and the VM6189 to untristate (activate control of SDIO). The clock rate need not be reduced during a write operation.

Figure 109 Serial Port Protocol

Table 158Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits <A7-A4>*				*Device ID <A3-A1>*	*R/W <A0>*
Vendor ID / Channel Count	0	0	0	0	0		1/0
Head Select / MR Bias Current DAC	1	0	0	0	1		1/0
Write Current DAC / Servo Bank	2	0	0	1	0	001	1/0
Thermal Asperity	3	0	0	1	1		1/0
Sleep / Idle / Gain	4	0	1	0	0		1/0

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Table 159Serial Interface Bit Description -- Data Bits

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Vendor ID / Channel Count	0 [1]	1 [2]	Channel	VS2	VS1	VS0	0	1	0
Head Select / MR Bias Current DAC	1	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
Write Current DAC / Servo Bank	2	BANK0	0 [3]	0 [3]	IW4	IW3	IW2	IW1	IW0
Thermal Asperity	3	TA3	TA2	TA1	TA0	TADET	DR1 [2]	DR0 [2]	0 [3]
Mode Select	4	0 [3]	BANK1	FR	0 [3]	MRMEAS	GAIN	IDLE	SLEEP

1. Read Only Register/Bits:
   Register 0, <D0-D2>: Vendor ID code (VTC=010),
   Register 0, <D3-D5>: Vendor revision code. Initial revision shall be (VS0 = 0, VS1 = 0, VS2 = 0),
   Register 0, <D6>: Channel count (0 = 8 channel, 1 = 4 channel),
   Register 0, <D7>: Programmable damping resistance (1 = present).
2. Programmable Damping Resistance Registers/Bits, See Table 153 on page 355 for further definition:
   Register 0, <D7>: Programmable damping resistance (1 = present),
   Register 3, <D1-D2> = Damping resistance value DAC.
3. Reserved Registers/Bits:
   Register 2, <D5-D6>,
   Register 3, <D0>,
   Register 4, <D4> and <D7>.

Table 160Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Vendor ID / Channel Count	0	<0000 0010> [1]
Head Select / MR Bias Current DAC	1	<0000 0000>
Write Current DAC / Servo Bank	2	<0000 0000>
Thermal Asperity	3	<0000 0000>
Mode Select	4	<0000 0000>

1. Assumes an eight channel device <D6> = 0, first revision of the chip <D5-D3> = 000 from VTC <D2-D0> = 010.

Table 161Serial Interface Timing Parameters

Description	Symbol	Min	Nom	Max	Units
Serial Clock (SCLK) Rate		.001		40	MHz
SENA to SCLK delay	T_{sens}	30			ns
SDIO setup time	T_{ds}	5			ns
SDIO hold time	T_{dh}	5			ns
SCLK cycle time	T_{c}	25			ns
SCLK high time	T_{ckh}	20			ns
SCLK low time	T_{ckl}	20			ns
SENA hold time	T_{shld}	25			ns
Time between I/O operations	T_{sl}	50			ns
Time to tristate controller driving SDIO (release control of SDIO)	T_{tric}			50	ns
Time to activate SDIO	T_{act}	0		50	ns
Duration of SENA (read)	T_{rd}	905			ns
Duration of SENA (write)	T_{wt}	855			ns
Risetime (CMOS 0.4 to 3.5 Volts, TTL 0.4 to 2.4 Volts)	T_{RIN}			4	ns
Falltime (CMOS 3.5 to 0.4 Volts, TTL 2.4 to 0.4 Volts)	T_{FIN}			4	ns
Risetime (CMOS 0.4 to 3.5 Volts, TTL 0.4 to 2.4 Volts)	T_{ROUT}			5	ns
Falltime (CMOS 3.5 to 0.4 Volts, TTL 2.4 to 0.4 Volts)	T_{FOUT}			5	ns

Note: SENA assertion level is high.

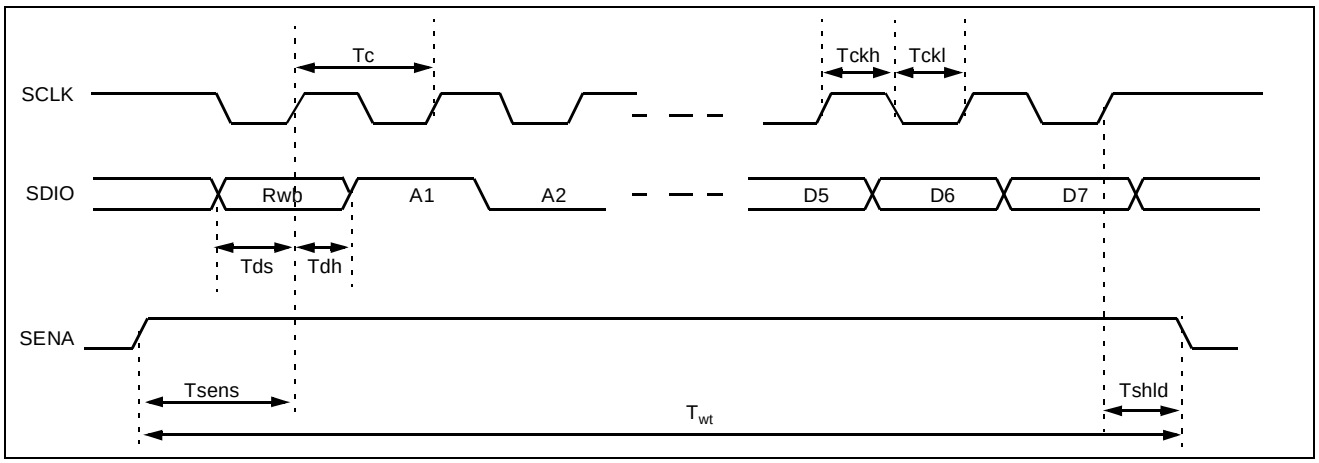


Figure 110 Serial Port Timing

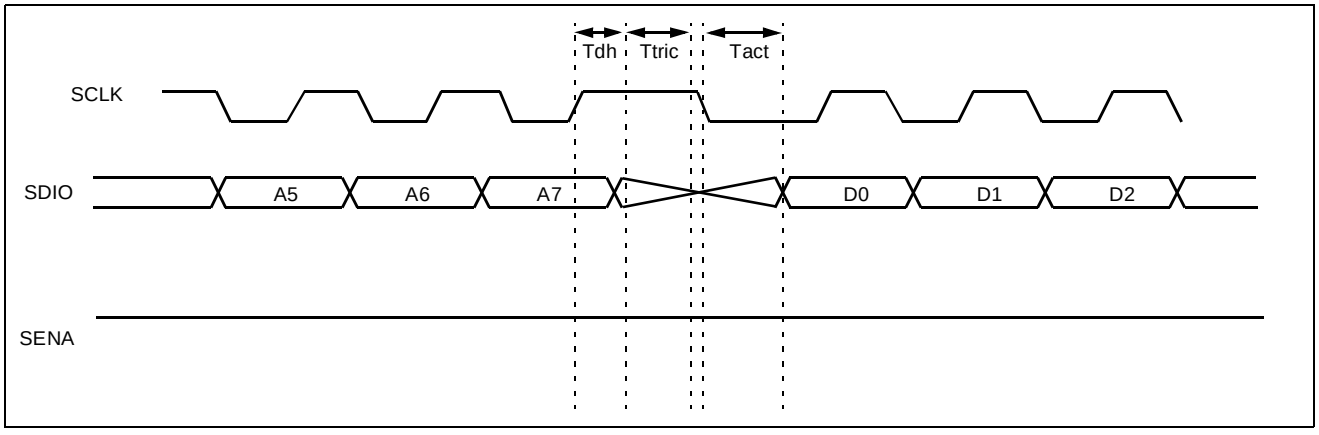


Figure 111 Serial Port Timing - Tristate Control

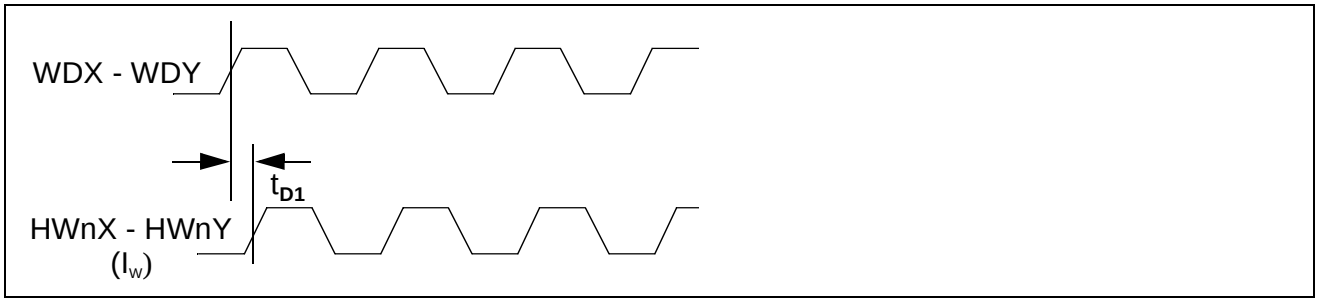


Figure 112 Write Mode Timing Diagram

The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY).
For WDX>WDY current flows into the “Y” port; for WDX<WDY current flows into the “X” port.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 8 mA		55	75	mA
		Write Mode, Bias enabled, I_W = 30mA, I_{MR} = 8mA		92	115	
		Idle Mode, Bias disabled		8	16	
		Sleep Mode		3.5	10	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 5.0V		172	200	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 5.0V		330	380	
Power Dissipation	P_d	Read Mode, I_{MR} = 8mA		280	412	mW
		Write Mode, Bias enabled, I_W = 30mA, I_{MR} = 8mA		375	632	
		Idle Mode, Bias disabled		40	83	
		Sleep Mode		17.5	55	
		Servo Mode, Bank of 4 heads, I_W = 25mA, V_{CC} = 5.0V		860	1000	
		Servo Mode, Bank of 8 heads, I_W = 25mA, V_{CC} = 5.0V		1650	1900	
Input High Voltage	V_{IH}	PECL	1.9		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	
Input Low Voltage	V_{IL}	PECL	1.7		V_{IH} - 0.2	V
		TTL	-0.3		0.8	
PECL Differential Input Swing	WDX-WDY		0.2		1.5	V_{PK}
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8mA, R_{MR}=50Ω

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
MR Head Current Range	I_{MR}		3.05	9	12.35	mA
MR Head Current Accuracy	ΔI_{MR}	3.05mA < I_{MR} < 12.35mA, R_{RS} = 2kΩ, V_{CC}=5V, T_A=25°C	-6		6	%
MR Head Current Temperature Sensitivity	$\frac{\Delta I_{MR}}{\Delta(115-25^{o}C)}$			0.6		%
MR Head Current Supply Sensitivity	$\frac{\Delta I_{MR}}{\Delta(0.5V)}$			0.3		%
Unselected MR Head Current					25	µA
MR Bias Top Voltage					800	mV
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Buffered Head Voltage Gain	A_{BHV}	Dynamic Gain I_{MR} (DAC=0) to I_{MR} (DAC=31)	4.75	5.0	5.25	V/V
Buffered Head Output Offset	V_{BOS}		-260	-80	100	mV
Digital Buffered Head Voltage	D_{BHV}	Low Threshold, MRMEAS bit = 1	350	380	410	mV
		High Threshold, MRMEAS bit = 1	478	520	562	
Differential Voltage Gain	A_V	V_{IN} = 1mV_{pp} @10MHz, T_A = 25°C, R_L(RDP, RDN) = 1kΩ, V_{CC}=5V 4 Channel, Gain bit = 0	117	138	159	V/V
		4 Channel, Gain bit = 1	187	220	253	
		8 Channel, Gain bit = 0	104	122	140	
		8 Channel, Gain bit = 1	166	195	224	
Differential Voltage Gain Temperature Sensitivity	$\frac{\Delta A_V}{\Delta(115-25^{o}C)}$			6		%
Differential Voltage Gain Supply Sensitivity	$\frac{\Delta A_V}{\Delta(0.5V)}$			0.2		%
Passband Upper Frequency Limit	f_{HR}	L_{MR} < 20nH, -3dB	160	200		MHz

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8mA, R_{MR}=50Ω

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Passband Lower -3dB Frequency Limit	f_{LR}	C_1= 0.01µF		0.7	1	MHz
		$\overline{FAST}$ = 0 or FR bit = 1		4.5	7	
Equivalent Input Noise (sense amp only)	e_a	1 < f < 100 MHz		0.62		$\frac{nV}{\sqrt{Hz}}$
Bias Current Noise	i_n			10		$\frac{PA}{\sqrt{Hz}}$
Equivalent Input Noise (total, excluding R_{MR})	e_n	1 < f < 100 MHz		0.8	1.0	$\frac{nV}{\sqrt{Hz}}$
Input Resistance	R_{IN}			3		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz, Gain bit = 1	5			mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC}, 1 < f < 100 MHz Input Referenced	45			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 1 < f < 100 MHz Input Referenced	45			dB
Pin Rejection	PR	100mV_{pp} @ R/$\overline{W}$, $\overline{BIAS}$, SCLK, SDIO or SENA, Output Referenced, Gain bit = 0, 1 < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-200		200	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.5		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			300	mV
Differential Output Resistance	R_{DO}	Read Mode, T_A = 25°C	60	70	80	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	2			mA

THERMAL ASPERITY CHARACTERISTICS

Parameter	*Specification*
Thermal Asperity Detection Threshold	50[1 + DAC value (0-15)]mV, output-referred: ± 20% @ 50 to 100mV or ± 15% @ >100mV
Thermal Asperity Detection Range	50mV to 800mV over baseline DC level in RDP/RDN (low frequency variation in baseline tracked by threshold)

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 130nH, R_H = 16Ω, f_{DATA} = 5MHz.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Write Current Range	I_W	base to peak	17		52	mA
Write Current Accuracy	ΔI_W	V_{CC} = 5V, T= 25°C	-10		10	%
Servo Write Current Accuracy	ΔI_{WS}	V_{CC} = 5V, T= 25°C, IW = 24.9 mA (2:<D0-D4> = 7)	-10		10	%
Write Current Sensitivity Temperature	$\frac{\Delta I_W}{\Delta(115-25^oC)}$			3		%
Write Current Sensitivity Supply	$\frac{\Delta I_W}{\Delta(0.5V)}$			0.6		
I_{MR}/I_W Reference Source	V_{RS}	R_{RS} = 2kΩ		2		V
Differential Head Voltage Swing	V_{DH}	Open Head, V_{CC} = 4.5V		7		V_{PP}
Unselected Head Transition Current	I_{UH}				50	μA_{pk}
Differential Output Damping Resistance	R_O			See Table 153 [1]		Ω
Damping Resistance Tolerance	ΔR_O		-20		20	%
Differential Output Capacitance					12	pF
Write Data Differential Input Resistance	R_{WDI}			120		Ω

1. The part has programmable damping resistance.
Note that the write current flowing to the head is dependent on the damping resistance; see equation 82 on page 355.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 30mA, L_H = 130nH, R_H = 16Ω, f_{DATA} = 5MHz, I_{MR}=8mA.

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current	20	30	50	ns
R/$\overline{W}$ to Servo Write Mode	t_{RWS}	To 90% of servo write current	25	50	65	ns
R/$\overline{W}$ to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value		300 [1]	500	ns
Read or Write to Idle Mode	t_{RI}/t_{WI}	To 10% of envelope		150	500	ns
Idle to Read Mode	t_{CS}	RDP/RDN to 90% of envelope and within ±30mV of final value		5 [1]	10	µs
Bias Disable to Enable, Read Mode	t_{BDE}	RDP/RDN to within ±30mV of final value		7.5	25	µs
HS0 - HS3 to Any Head	t_{HS}	RDP/RDN to within ±30mV of final value; read mode ΔR_{MR} = 0, ΔI_{MR} = 0		6.5	10	µs
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		15	20	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time; L_H = 0; R_H = 0			0.5	ns
Rise/Fall Time	t_r / t_f	10 - 90%, R_D=670Ω		1.7		ns
Bias Current Change	$t(\Delta I_{MR})$	ΔI_{MR} from 5 to 10 mA, RDP/RDN to within ±30mV of final value		7	25	µs

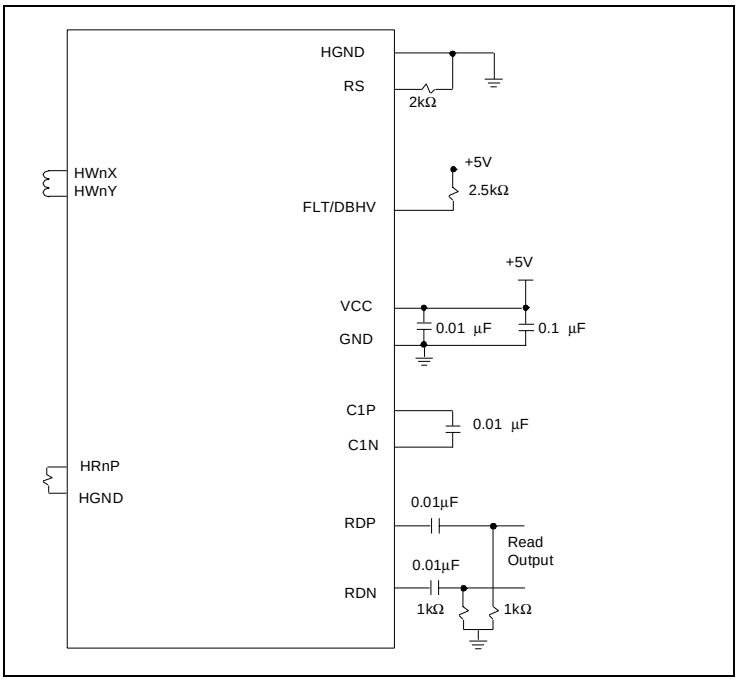
1. $\overline{BIAS}$ pin active low for 25 µs preceding the mode transition.

FAULT PROCESSING CHARACTERISTICS

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
VCC Fault Threshold [1]	V_{LFT}	Fault Detected	3.2	3.6	3.8	V
	V_{UFT}	Fault Removed	3.3	3.75	4.0	
VCC Fault Threshold Hysteresis	V_{HFT}			150		mV
MR Head Open Fault Threshold			850	1000	1150	mV
Open Head Fault Delay	t_{FLTD}	Good to Open Head		5		µs
MR Head Short Fault Threshold				50	60	mV
Low Write Data Frequency Fault	V_{FFT}	FLT = Low (safe)		750	900	ns
Thermal Asperity Detect Delay	TA_{DLY}			50	60	ns
Output High Current	I_{FLToH}	V_{OH} = 5.0 V			50	µA
FLT/DBHV Output Voltage Low	V_{FLToL}	I_{OL} = 2 mA			0.4	V
FLT/DBHV Settling Time	$DBHV_{SETTLE}$				10	µs

1. Writer Functionality shall be maintained for V_{CC} conditions ranging from the specified V_{CC} limits to the Low Voltage Detector Threshold Voltage.

TYPICAL APPLICATION CONNECTIONS



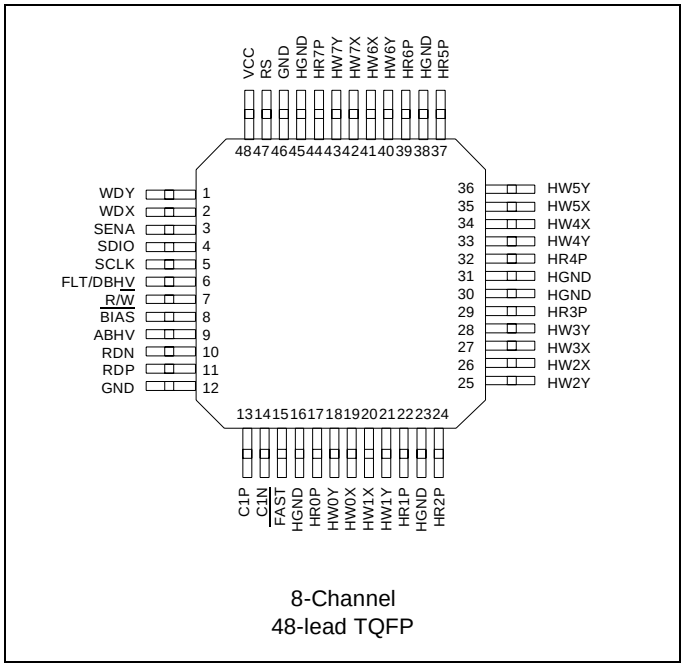
Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Minimizing parasitics at the C1 node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the pins/pads as possible.
- For optimal performance connect C1N externally to the same ground as the read heads (HGND), or isolate C1N as shown above (C1N is tied to HGND internally).
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins/pads:
  VCC - GND
- For maximum stability, place the decoupling capacitors and the R_{RS} resistor as close to the pins/pads as possible.

VM6189

8-CHANNEL CONNECTION DIAGRAM



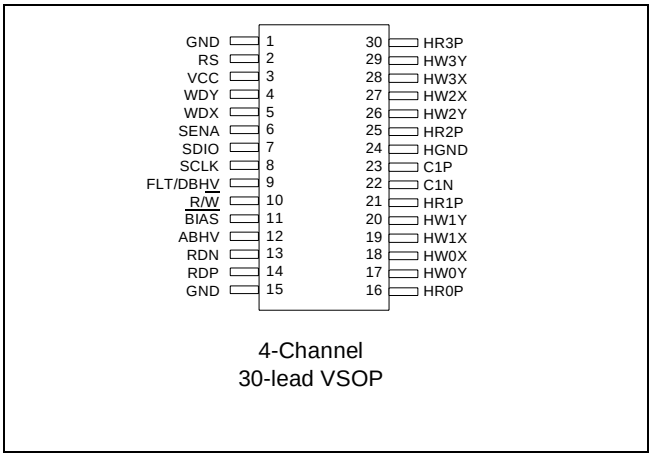
8-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

VM6189

4-CHANNEL CONNECTION DIAGRAM



4-Channel
30-lead VSOP

Specific Characteristics

See the general data sheet for common specification information.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

VTC Inc.
Value The Customer™

VM6203

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 350 Mbits/sec
  - Requires Only One External Component (R_{EXT})
  - Designed for Use With Four-Terminal Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection & Thermal Asperity Detection)
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 12 Channels Available
  - Fault Detect Capability
  - Servo Write Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC
    Mask option: AMR: 4 - 10 mA, GMR: 2 - 5 mA
  - Programmable Read Voltage Gain
    (150, 200, 250 or 300 V/V Typical)
  - Input Noise Voltage = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Noise Current = 12 pA/$\sqrt{Hz}$ Typical
  - Input Capacitance = 6 pF Typical
  - Head Inductance Range = 10 nH - 150 nH
  - Bandwidths in Excess of 250 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 10 - 50 mA Range
  - Rise Time 1.0 ns Typical
    (10-90%, L_{total} = 100 nH, I_W = 40 mA)

DESCRIPTION

The VM6203 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using multiple 4-terminal recording heads. The VM6203 contains a thin-film head writer, an MR reader, and associated fault circuitry. Multiple preamp addressing uses software registers to validate the hardware based address.

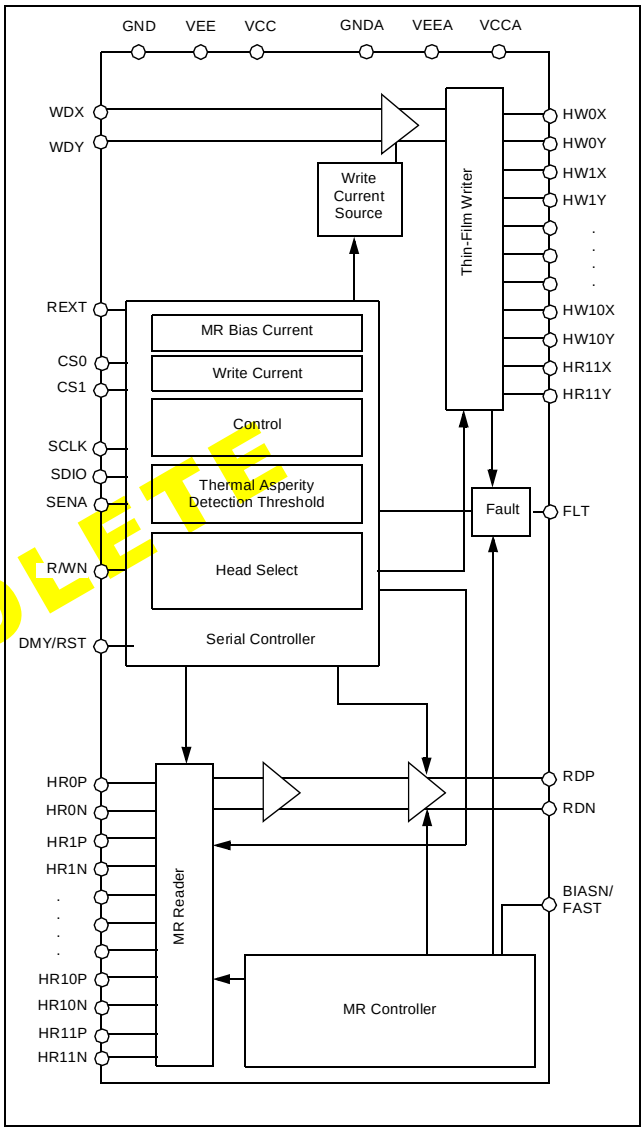
Programmability of the VM6203 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, gain, head selection and thermal asperity detection threshold.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection internal resistors are connected to the R/WN and SENA lines to prevent accidental writing due to an open line and to ensure power-up in a non-writing condition.

The VM6203 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6203 is available in bump die form for chip-on-flex applications. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +6V

Read Bias Current, I_{MR} 18mA
Write Current, I_W 90mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 10 - 50 mA
Write Head Inductance, L_W ..... 10 - 100 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 2 - 10 mA
Read Head Inductance, L_{MR} ..... 10 - 150 nH
Read Head Resistance, R_{MR} ..... 25 - 90 Ω (Imr*Rmr<700mV)
Junction Temperature, T_J ..... 0°C to 125°C

GENERAL DESCRIPTION

Serial Interface Controller

The VM6203 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude.

See “SERIAL PORT” on page 373 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

The VM6203 is designed for a single or multiple preamp configurations. All control lines may be shared (including the three serial lines SCLK, SDIO and SENA).

Pins CS0 and CS1 determine the preamplifier’s address in a dual preamp configuration. Pins CS0 and CS1 are compared to the programmed address stored in register 0, bits <A1-A0> to activate the chip or to select servo track write operation as shown in Table 162.

Table 162Chip Select

Address Pins		
CS1	***CS0***	***Chip Status***
0	0	Active, if matched with register 0, bits <A1-A0>
0	1	Active, if matched with register 0, bits <A1-A0>
1	0	Active, if matched with register 0, bits <A1-A0>
1	1	Broadcast Servo Track Write (STW) according to register 10 settings

OPERATING MODES

Test Modes

Test mode allows the user to calculate the MR head resistance by measuring V_{MR} or to calculate the die temperature.

MR Head Resistance

MR Head Resistance is calculated by setting DIGON (register 8, <D0>) high and setting MR1 and MR0 (register 8, <D2-D1) to one of three binary voltage ranges (00 to 10) shown in Table 167.

Note: An iterative method for determining the MR Head Resistance value is available:
1. Set DIGON = 1.
2. Set MR1 and MR0 (register 5, <D2-D1) to one of three binary voltage settings (00 to 10).
3. Select a 5 bit value in register 5, <D4-D0> corresponding to a MR Head voltage setting.
   - If FLT is 0, the value is lower than the actual V_{MR} value.
   - If FLT is 1, the value is higher than the actual V_{MR} value.
4. Repeat steps 2 and 3 to determine the value of V_{MR}.
5. Apply Ohms Law (R=V/I) to calculate the resistance of the MR head.

Die Temperature Monitoring

Die Temperature is read by setting DIGON (register 8, <D0>) high and setting MR1 and MR0 (register 8, <D2-D1) to temperature mode (11).

Note: An iterative method for determining the Die Temperature value is available:
1. Set DIGON = 1.
2. Set MR1 and MR0 (register 8, <D2-D1) to the temperature setting (11).
3. Select a 5 bit value in register 5, <D4-D0> corresponding to a die temperature setting.
   - If FLT is 0, the value is lower than the die temperature.
   - If FLT is 1, the value is higher than the die temperature.
4. Repeat step 3 to determine the die temperature.

Idle Mode

In the idle mode, power dissipation is reduced. The internal write current generator, write current source and MR bias current source are deactivated while the RDN and RDP outputs switch to a high impedance state. The serial register contents remain latched and filter capacitance bias is maintained to reduce power-up delay. The fault indicator is not active in idle mode.

Idle mode is selected by setting Mode 0 and Mode 1 to 01 (register 9, bits <D1-D0>), see Tables 163 and 166.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier that senses resistance changes in the MR element which correspond to flux changes on the disk.

Read mode is selected by setting Mode 0 and Mode 1 to 10 (register 9, bits <D1-D0>), see Tables 163 and 166.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6203 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external resistor (connected between pin REXT and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{(K_{IMR} \times 0.387) + 8}{R_{EXT}} \times \frac{380}{320 + R_{MR}} \quad \textit{(eq. 83)}$$

I_{MR} represents the bias current (mA) flowing to the MR element.
R_{ext} represents the equivalent resistance (Ω) between the REXT pin and ground.
k_{IMR} represents the MR bias DAC setting (0 to 31).

MR head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±500mV of ground and unselected heads are held at approximately -800mV.

Fault Detection in Read Mode

In the read mode, a TTL low on the FLT line indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 169.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, register 7, bits <D7-D4> as shown in Table 169. The default setting is to enable all faults.

Fault codes may be cleared by reading the vendor identification data stored in register 6. The following are valid read fault conditions:

No Read Bias Current (R_{EXT} open or shorted to power or ground)	
MR head voltage out-of-range	Test Mode only
Thermal asperity detected	
Read head open	Test Mode only
Power supplies out-of-range	
Temperature too high	
Illegal head address	

Read Gain

The default gain is 150 V/V with a head resistance of 60Ω. Read Gain may be increased in 50V/V increments using a 2-digit binary code in register 2, bits <D1-D0> (00 = 150, 01 = 200, 10 = 250 and 11 = 300). The formula that describes the actual gain is shown below:

$$A_V = \frac{380 \times (GainSetting)}{320 + R_{MR}} \quad \textit{(eq. 84)}$$

GainSetting = 150, 200, 250 or 300
R_{MR} is the resistance (Ω) of the MR head.

MR Bias DAC

The 5 bits in register 2 (<D6-D2>) represent the binary equivalent of the DAC setting (0-31, LSB first). Two ranges of bias control are offered as a mask option. The AMR option has an MR Bias DAC range of 4 to 10 mA. The GMR option has an MR Bias DAC range of 2 to 5 mA.

Fast Mode

Taking the BIASN/FAST pin low, while BFCTL = 1 (register 1, bit <D0>), selects the normal read bandwidth for the specified head.

Setting the BIASN/FAST pin high selects read bandwidth with raised lower corner set in LFP (register 3, bits <D1-D0>).

Thermal Asperity Detection

Setting the TAD bit high (register 5, bit <D6>) enables thermal asperity detection. The TRANGE bit (register 5, bit <D7) selects the range, (Low or High, for the TA threshold (TAT).

If a head-to-disk contact occurs, the thermal asperity in the MR element will result in a fault condition. The Range is governed by the following equation and is set in register 5, bits <D4-D0>:

$$V_{TAT} = TBD(TBD + k_{TAT}) \quad \textit{(eq. 85)}$$

V_{TAT} represents the TA threshold (input-referred in mVpk).
k_{TAT} represents the TA DAC setting (0-127).

Note that a fault condition resulting from a thermal asperity will remain active until a positive side hysteresis is ≤20% of the threshold.

Fast Recovery from Thermal Asperity

Setting the TA Compensation (TAC) bit high (register 5, bit <D5>) automatically initiates the Fast Recovery mode if a thermal asperity is detected. The low frequency corner is raised from a nominal value.

Raising the low frequency corner removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence.

Note: The TA detection circuitry must be enabled with the TAD bit.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

Write mode is selected by setting Mode 0 and Mode 1 to 10 (register 9, bits <D1-D0>), see Tables 163 and 166.

The magnitude of the write current is referenced to the current flowing through an external resistor (connected between pin REXT and ground). The following equation governs the write current magnitude:

$$I_W = \frac{(K_{IW} \times 2.58) + 20}{R_{EXT}} \quad \textit{(eq. 86)}$$

I_W represents the write current (mA flowing to the selected head).
R_{ext} represents the equivalent resistance (kΩ) between the REXT pin and ground.
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 116 for the timing diagram.

Write Current DAC

The 5 bits in register 4 (<D7-D3>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIASN/FAST pin low in write mode, while BFCTL = 0 (register 1, bit <D0>), enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Write Data Modes

Setting the WVORI bit low (register 1, bit <D1>) initiates the Voltage Write mode. Setting the WVORI bit high initiates the Current Write mode.

In voltage write mode the writer switches on PECL input voltage levels. In current write mode the writer switching is dependent on the amount of current that is sinking from the write data inputs.

Fault Detection in Write Mode

In the write mode, a TTL high on the FLT line indicates a fault condition. Fault codes, conditions and the modes in which they are valid are listed in Table 169.

Specific fault conditions may be disabled by setting the Fault Reporting Mode, register 7, bits <D7-D4> as shown in Table 169. The default setting is to enable all faults.

Fault codes may be cleared by reading the vendor identification data stored in register 6.

The following are valid write fault conditions:

No write current (R_{EXT} open or shorted to power or ground)	
Open or shorted write head	Write current remains enabled
Write data frequency too low	Write current remains enabled
Device in read or idle mode	Write current disabled
Power supplies out-of-range	Write current disabled
Temperature too high	Write current remains enabled.
Illegal head address	Write current disabled

Reader On Mode

Setting the ROUTON bit high (register 1, bit <7>) turns on the 1st and 2nd Stage Reader and biases the MR Head. This allows a drive to be read regardless of the mode (read, write or idle) of the preamplifier.

If ROUTON = 0, the state of the reader is dependent on other registers and pins (see Table 167).

Servo Write Mode

In the servo write mode, two channels may be written simultaneously.

Table 166 indicates how heads can be selected for individual or simultaneous writing.

Setting the MODE bit (register 9, bits <D1-D0>) to “11” (along with appropriate levels on the R/WN pin and STW Bank and Head bits) places the preamp in servo write mode (see Table 163).

Note: It is the customer’s responsibility to make sure the thermal constraints of the die/flex/package are not exceeded. (This could be achieved by lowering the supply voltage, reducing the write current or cooling the die/flex/package.)

Reset/Dummy Mode

Reset or Dummy mode provides data protection and recovery to known register states or protection of register states should an error occur. The programmed mode is triggered by setting the DMY/RST pin low.

When Reset mode is selected (register 9, <D2> = 0) and the DMY/RST pin is set low the following sequence occurs:

22) Set all register bits to defaults.

23) Remove write current.

24) Select dummy head.

When Dummy mode is selected (register 9, <D2> = 1) and the DMY/RST pin is set low the following sequence occurs:

25) Retain all register bits settings.

26) Maintain write current level.

27) Select dummy head.

Table 163Mode Selects

MODE	*CS1*	*CS0*	*MEAS 5:<4-0>*	*MR1 8:<2>*	*MR0 8:<1>*	*DIGON 8:<0>*
Disable MR HD Measure	1	1	0/1	1	1	0
MR HD V Range	1	1	0/1	0/1	0/1	1
MR HD Temp	1	1	0/1	1	1	1

MODE	*CS1*	*CS0*	*MODE1 9:<D1>*	*MODE0 9:<D0>*	*HEAD 10:<7-1>*	*BANK 10:<D0>*	*R/WN*
Idle	1	1	0	0	X	X	X
Idle	1	1	0	1	X	X	X
Read	1	1	1	0	X	X	1
Write	1	1	1	0	X	X	0
Servo Track Write	1	1	1	1	0/1	0/1	0

MODE	*CS1*	*CS0*	*MODE1 9:<D2>*	*DMY/ RST*
Reset	1	1	0	0
Dummy	1	1	1	0

1. To select the device, the bit pattern (00, 01 or 10) stored in register 0, bits <D1-D0> must match that on pins CS0 and CS1.

SERIAL PORT

Serial Interface

The VM6203 uses a 3-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude. See Tables 165 and 166 for a bit description.

The serial interface has two input lines, SCLK (serial clock) and SENA (serial enable), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. The SENA line is used to activate the SCLK and SDIO lines and power-up the associated circuitry. When SENA is low only the output D-latches and the reference generators remain active. An internal pull-down resistor is connected to SENA to ensure power-up in a non-writing condition and to prevent accidental writing due to open lines.

16 bits constitute a complete data transfer as shown in Figure 113.

- The first 8 bits <A7-A0> are write-only and consist of:
  - one command bit <A0> (high for read, low for write),
  - two chip select bits <A2-A1> (that must match the CS0 and CS1 pad logic levels in Table 165), and
  - five register address bits <A7-A3> (A7 is unused at present).
- The second 8 bits <D7-D0> consist of data to be written-to or read-from the control registers.

A data transfer is initiated upon the assertion of the serial enable line (SENA). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 16 cycles; on the falling edge of SENA, the data will be written to the addressed register.

During a read sequence, SDIO will become active on the falling edge of the 9th cycle (delayed to allow the controller to release control of SDIO). At this time <D0> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 165 and 166 for a bit description. See Table 165 and Figure 113 for serial interface timing information.

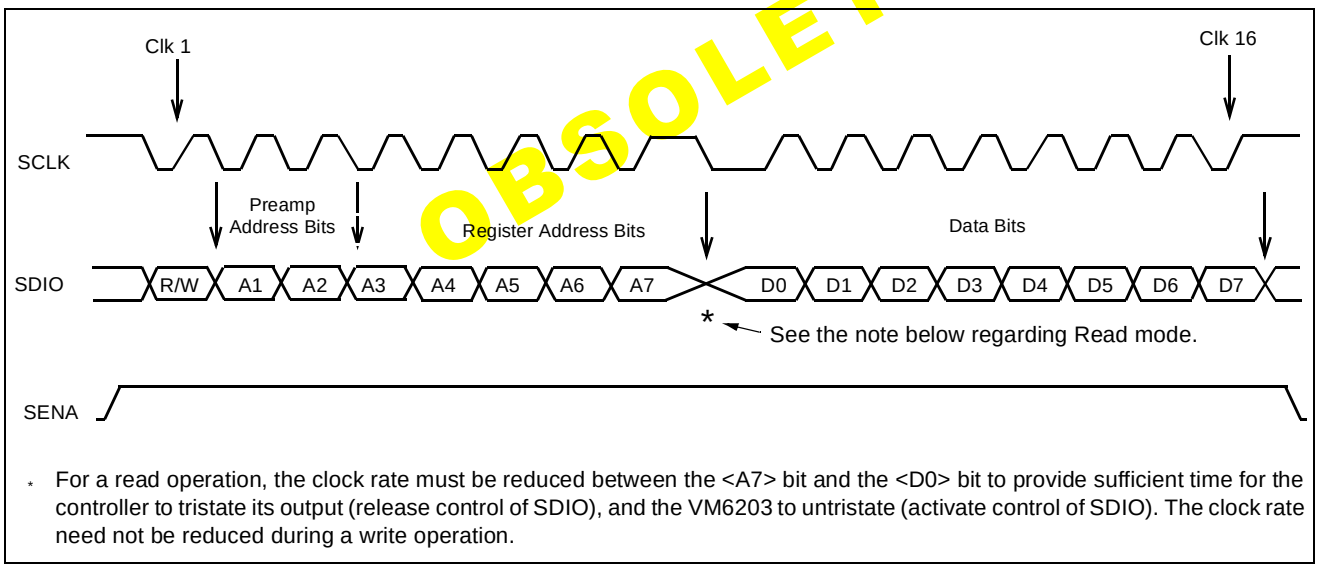


Figure 113 Serial Port Protocol

Table 164Serial Interface Parameters

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNITS
Serial Clock (SCLK) rate, write				30	MHz
SENA to SCLK delay	T_{sens}	TBD			nS
SDIO setup time, write	T_{wds}	TBD			nS
SDIO delay time, read	T_{rds}	TBD		TBD	nS
SDIO hold time	T_{dh}	TBD			nS
SCLK cycle time	T_{c}	TBD			nS
SCLK high time	T_{ckh}	8			nS
SCLK low time	T_{ckl}	8			nS
SENA hold time	T_{shld}	3			nS
Time between I/O operations	T_{sl}	TBD			nS
Time from controller releasing SDIO (tristate) to SCLK falling edge	T_{tric}	TBD			nS
Time to activate SDIO	T_{act}	TBD		TBD	nS
Duration of SerEna (read)	T_{rd}	TBD			nS
Duration of SerEna (write)	T_{wt}	TBD			nS
SDIO output high voltage	V_{OH}	3.85			V

Note: SENA assertion level is high.

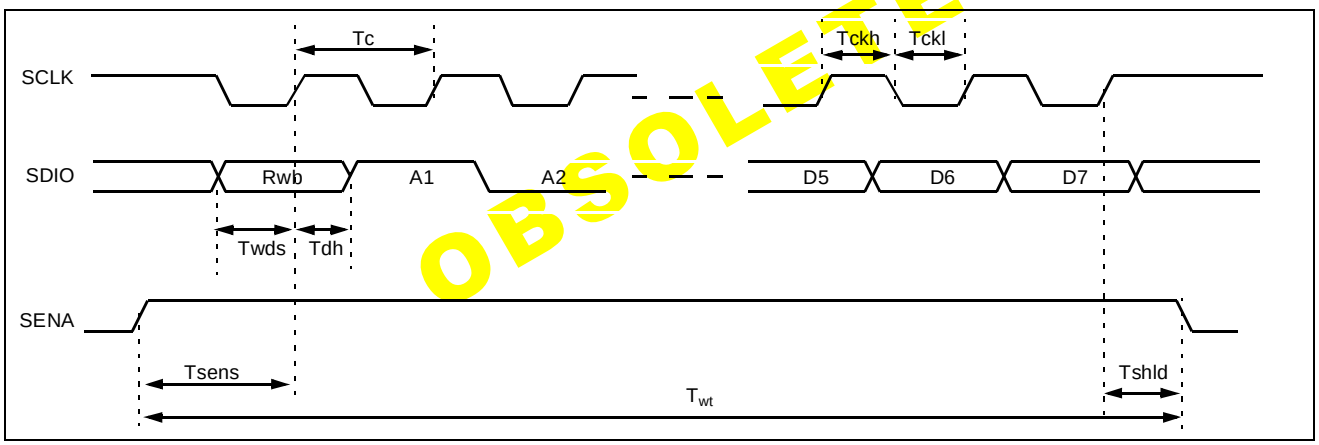


Figure 114 Serial Port Timing - Write Operation

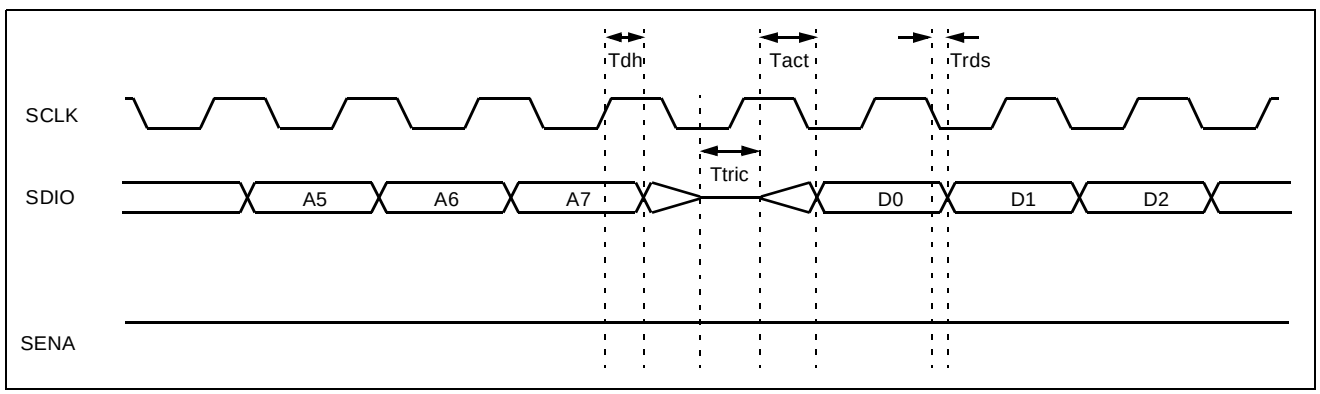


Figure 115 Serial Port Timing - Tristate Control during Read Operation

Serial Registers

8-bit registers are accessible for read/write operations via the serial interface. Table 165 lists the serial address for each register.Table 166 lists the data contents of the registers. A description of the individual bits is provided.

Table 165: Serial Interface Addressing

Register #	Register Address Bits					Preamp Address Bits		R/W bit
	<A7>	<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>
0	1	0	0	0	0	CS1	CS0	1/0
1	1	0	0	0	1	CS1	CS0	1/0
2	1	0	0	1	0	CS1	CS0	1/0
3	1	0	0	1	1	CS1	CS0	1/0
4	1	0	1	0	0	CS1	CS0	1/0
5	1	0	1	0	1	CS1	CS0	1/0
6	1	0	1	1	0	CS1	CS0	1/0
7	1	0	1	1	1	CS1	CS0	1/0
8	1	1	0	0	0	CS1	CS0	1/0
9	1	1	0	0	1	CS1	CS0	1/0
10	1	1	0	1	0	CS1	CS0	1/0

1. Reserved

Table 166Serial Interface Bit Map

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Chip/Head Select	0	HS3	HS2	HS1	HS0	1	1	LSC1	LSC0
Bias/Fast Select	1	ROUTON	1	1	1	1	1	WVORI	BFCTL
IMR/Gain Select	2	DUMMY	IMR4	IMR3	IMR2	IMR1	IMR0	GAIN1	GAIN0
Bandwidth Select	3	1	1	1	1	1	HFP	LFP1	LFP0
Write Current Select	4	IW4	IW3	IW2	IW1	IW0	1	1	1
Thermal Asperity	5	TRANGE	TAD	TAC	TAT4	TAT3	TAT2	TAT1	TAT0
Vendor ID	6	VEND7	VEND6	VEND5	VEND4	VEND3	VEND2	VEND1	VEND0
Fault Reporting	7	FLT3	FLT2	FLT1	FLT0	FCODE3	FCODE2	FCODE1	FCODE0
MR/Temp Select	8	1	1	1	1	1	MR1	MR0	DIGON
Mode Select	9	1	1	1	1	1	DMY/RST	MODE1	MODE0
Servo Select	10	HD12/13	HD10/11	HD8/9	HD6/7	HD4/5	HD2/3	HD0/1	BANK

1. Reserved

Table 167Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
0	D1-D0	Chip Select Logic	LSCn	For the device to be selected, bit settings must match the logic level of the CS0 and CS1 pins as shown in Table 165.
	D3-D2	Reserved		
	D7-D4	Head Select	HSn	Binary Address of selected head.
1	D0	Bias/Fast Control	BFCTL	0 = MR Bias Current On/Off, depending on logic level of BIASN/FAST pin. - BIASN/FAST pin low: MR Head Bias Current On. - BIASN/FAST pin high: MR Head Bias Current Off. 1 = Fast Response Mode, depending on logic level of BIASN/FAST pin. - BIASN/FAST pin low: Normal Response. - BIASN/FAST pin high: Fast Response, with raised lower corner frequency. Note: Bias current is always on when BFCTL = 1. Note: Fast mode is off when BFCTL = 0.
	D1	Write Data Control	WVORI	0 = Voltage Write Mode selected. 1 = Current Write Mode selected. Polarity of Current Mode is: - Positive - pin with no current flow, - Negative - pin with current flowing.
	D6-D2	Reserved		
	D7	Reader ON Control	ROUTON	0 = Off 1 = On Reader On forces the reader to be biased and reader outputs on during all modes of operation (write and read), but does not specify write current to be on during read mode.
2	D1-D0	Gain Control	GAINn	Binary selection of Reader Gain: 00 = 150 V/V 01 = 200 V/V 10 = 250 V/V 11 = 300 V/V
	D6-D2	Reader Bias Control	IMRn	Binary selection of Reader Bias Current: AMR mode = 5 to 10 mA in 0.1935 mA increments. GMR Mode = 2 to 5 mA in 0.0967 mA increments. Note: AMR or GMR is a mask option.
	D7	Internal Dummy Reader	DUMMY	0 = selected. 1 = not selected.
3	D1-D0	Low Frequency Bandwidth	LFPn	Binary selection of Low Frequency Bandwidth in Fast Mode: 00 = 2.5 MHz 01 = 5.0 MHz 10 = 7.5 MHz 11 = 10.0 MHz Note: Fast Response Mode selected in Register 1, bit 0 = 1 and BIASN/FAST pin = high.
	D2	High Frequency Bandwidth	HFP	Binary selection of High Frequency Bandwidth: 0 = 150 MHz 1 = 205 MHz Note: Normal Response Mode selected in Register 1, bit 0 = 1 and BIASN/FAST pin = low.
	D7-D3	Reserved		
4	D2-D0	Reserved		
	D7-D3	Write Current	IWn	Binary selection of Write Current: 10 mA (00000) to 50 mA (11111) in 1.290 mA increments.

Table 167Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
5	D4-D0	Thermal Asperity Detection Threshold	TATn	Binary selection of Thermal Asperity Detection characteristics: Low TA Range = 0.4 mV (00000) to 6.0 mV (11111) in 0.180 mV increments. High TA Range = 3.4 mV (00000) to 9.0 mV (11111) in 0.180 mV increments. Note: TA Range is selected in Register 5, bit 7.
	D5	Thermal Asperity Compensation	TAC	0 = No Automatic TA Compensation selected. 1 = Automatic TA Compensation selected.
	D6	Thermal Asperity Detection	TAD	0 = TA Detection and Compensation not selected. 1 = TA Detection and Compensation selected.
	D7	Thermal Asperity Range Shift	TRANGE	0 = Low TA Range (0.4 mV to 6.0 mV) 1 = High TA Range (3.4 mV to 9.0 mV)
6	D2-D0	Vendor Code	VENDn	Binary Vendor Code (010 = VTC) MSB to LSB
	D4-D3	Part ID		Binary Part Identification (00 = VM620310) MSB to LSB
	D7-D5	Revision of Part		Binary Revision Count: Revision 1 (000) to Revision 8 (111) Note: Revision count restarts at 1 (000) after exceeding 8 (111).
7	D3-D0	Fault Code	FCODEn	See Table 169.
	D7-D4	Fault Reporting Mode	FLTn	Selects which of 4 Fault Modes (FLT3 to FLT0) to report according to the matrix: 0 = Enable Fault 1 = Disable Fault

	FLT 3 <D7>	FLT 2 <D6>	FLT 1 <D5>	FLT 0 <D4>
Enable All Faults	0	0	0	0
Disable Open and Shorted Write Head Faults	1	X	X	X
Disable Voltage Faults	X	1	X	X
Disable MR Head Overvoltage and Open MR Head Faults	X	X	1	X
Disable Temperature Fault	X	X	X	1
Disable All Faults Note: FLT line is disabled, but codes are still available on serial interface.	1	1	1	1

8	D0	Disk Polling with FLT pin	DIGON	0 = Disable MR Head Measurement/Temperature Mode 1 = Enable MR Head Measurement/Temperature Mode Note: Range of MR Head Measurement is selected in Register 8, bits 1 and 2.
	D2-D1	MR Head Temperature Range	MRn	Binary selection for Range of MR Head Measurements: Note: MR Head Measurement Mode (DIGON) is selected in Register 8, bit 0.

MR Head Measurement Range (V_{MR})	MR1 <D2>	MR0 <D1>	DIGON <D0>
Disabled	X	X	0
200 to 400 mV	0	0	1
375 to 575 mV	0	1	1
550 to 750 mV	1	0	1
Temperature Mode	1	1	1

	D7-D3	Reserved		

Table 167Serial Register Data Bit Descriptions

Register	Bits	Function	Symbol	Description
9	D1-D0	Device Mode	MODEn	Binary selection of the Operating Mode for the device: 00 = Idle (Sleep) Mode 01 = Idle (Standby) Mode 10 = Read or Write Mode 11 = Servo Track Write (STW) Mode Note: Active Heads for Servo Track Write are set in Register 10.
	D2	Reset/Dummy	DMY/RST	0 = Selects Reset Mode for DMY/RST pin. - DMY/RST pin low: Reset Mode sequences is: 1. Set all register bits to defaults (see Table 168). 2. Remove Write Current. 3. Select Dummy Head. - DMY/RST pin high: TBD. 1 = Selects Dummy Mode for DMY/RST pin. - DMY/RST pin low: Dummy Mode sequences is: 1. Retain all register bit settings. 2. Maintain Write Current level. 3. Select Dummy Head. - DMY/RST pin high: TBD. Note: DMY/RST pin defaults low due to internal pull-down resistor.
	D7-D3	Reserved		
10	D0	STW Head Bank	BANK	0 = Selects Even-numbered heads to be written as a servo track. 1 = Selects Odd-numbered heads to be written as a servo track. Note: Register 10, bits 1 to 7 define which Head pairs to STW.
	D7-D1	STW Head Select	HDn	Binary selection of the Head pairs to be servo track written. Note: Register 10, bit 0 defines whether to select the odd or even-numbered head. Examples: 1. 00001010 = Servo Bank Write Head 0 and 4: - Bit 0 = 0 selects Even-numbered heads - Bit 1 = 1 selects Head 0 (from the HD0/1 pair) - Bit 3 = 1 selects Head 4 (from the HD4/5 pair) 2. 00001011 = Servo Bank Write Head 1 and 5: - Bit 0 = 0 selects Odd-numbered heads - Bit 1 = 1 selects Head 1 (from the HD0/1 pair) - Bit 3 = 1 selects Head 5 (from the HD4/5 pair) Note: A maximum of 2 heads can be servo track written at one time.

Table 168Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Chip/Head Select	0	<0000 0000>
Bias/Fast/Write Select	1	<0000 0000>
Reader Select	2	<0000 0000>
Bandwidth Select	3	<0000 0000>
Write Current Select	4	<0000 0000>
Thermal Asperity	5	<0000 0000>
Vendor ID	6	<0000 0000>
Fault Reporting	7	<0000 0000>
Mode Select	8	<0000 0000>
Servo Select	9	<0000 0000>
Reserved	10	<0000 0000>

Table 169Fault Conditions and Codes

Fault Code 7:<D3-D0>	*Mode*	*Fault*	*Condition*
0000	Read or Write	No Fault	
0001	-	Reserved	
0010	Read	MR Head Voltage to High / Read Head Open	Test Mode
0011	Read	Thermal Asperity Detected	
0100	-	Reserved	
0101	Write	No Write Current	I_W < 1 mA
0110	Write	WDI Frequency Low	F_{WDI} < 2 MHz
0111	Write	Write Head Open	
1000	Write	Write Head Shorted to GND	
1001	Read or Write	REXT Open or Shorted	
1010	-	Reserved	
1011	Read or Write	Low V_{DD}	V_{DD} < +3.9 V typical
1100	Read or Write	Low V_{EE}	V_{EE} < -3.9 V typical
1101	Read or Write	Illegal Head Select	
1110	-	Reserved	
1111	Read or Write	Overtemperature	T_j > 140°C

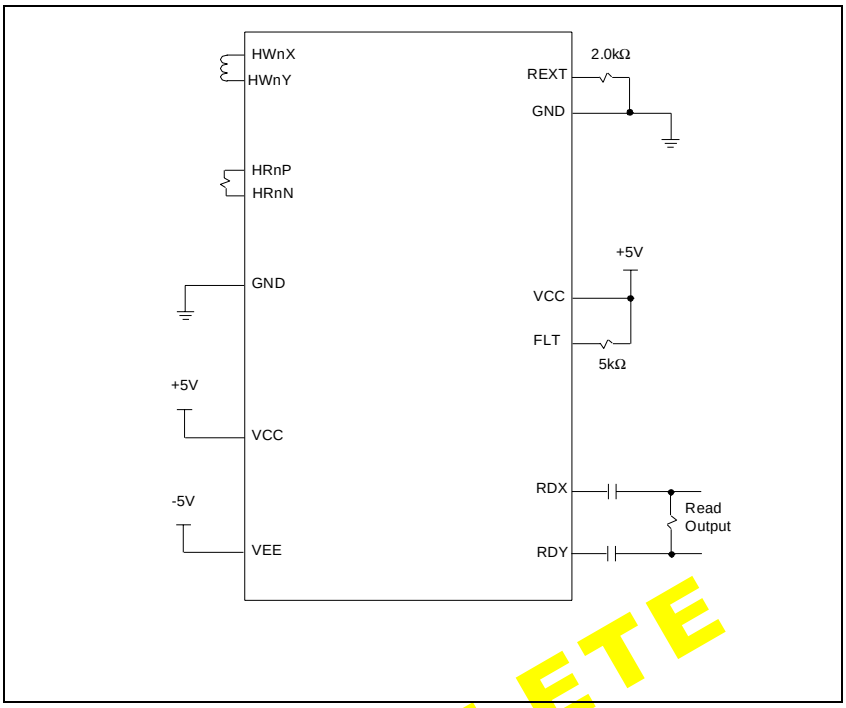
PIN FUNCTION LIST AND DESCRIPTION

Signal	*Input/ Output* [1]	*Description*
CS0, CS1	I	Chip Select: Serial Address, bits 0 and 1 select the chip. See Table 165 for bit selections.
DMY/RST	I	Reset/Dummy Select: Resets preamp to default conditions or enables dummy reader load. Serial Register 9, bit 2 selects the pin function. See Table 167 for bit selections.
R/WN	I [2]	Read/Write: A TTL low level enables write mode. Pin defaults high (read mode).
BIASN/FAST	I	Bias/Fast Enable: Pin defaults high (bias disabled/fast response). Note that the Bias/Fast Control bit (register 1, bit <D0>) sets the function of the pin, see Table 167.
FLT	O [2]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode. Internal 100kΩ pullup resistor defaults pin high.
WDX, WDY	I [2]	Differential Pseudo ECL write data inputs.
HR0P-HR11P	I	MR head connections, positive end.
HR0N-HR11N	I	MR head connections, negative end.
HW0X-HW11X	O	Thin-Film write head connections, positive end.
HW0Y-HW11Y	O	Thin-Film write head connections, negative end
RDP, RDN	O [2]	Read Data: Differential read signal outputs.
VEE	[2]	-5.0V supply
VCC	[2]	+5.0V supply
GND	[2]	Ground
VEEA	[2]	Analog -5.0V supply
VCCA	[2]	Analog +5.0V supply
GNDA	[2]	Analog Ground
REXT	O	Reference Voltage pin for both MR bias current and write current.
SCLK	I [2]	Serial Clock: Serial port clock; see Figure 113. Internal pulldown resistor defaults pin low.
SDIO	I/O [2]	Serial Data: Serial port data; see Figure 113. Internal pulldown resistor defaults pin low.
SENA	I [2]	Serial Enable: Serial port enable; see Figure 113. Internal pulldown resistor defaults pin low.

1. I = Input pin, O = Output
2. When more than one device is used, these signals can be wire-OR'ed together.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

TYPICAL CONNECTION DIAGRAM



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors and the R_{EXT} resistor as close to the pins/pads as possible.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 8 mA, I_W = 40 mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Power Supply Current	I_{CC}	Read Mode, IMR = 7.9 mA		125	TBD	mA
		Write Mode, IWR = 40 mA b-p		114	TBD	
		Write Mode, Reader Biased		160	TBD	
		Idle Mode		26	TBD	
V_{EE} Power Supply Current	I_{EE}	Read Mode, IMR = 7.9 mA		35	TBD	mA
		Write Mode, IWR = 40 mA b-p		80	TBD	
		Write Mode, Reader Biased		80	TBD	
		Idle Mode		2	TBD	
Power Supply Dissipation	P_d	Read Mode, V_{CC} = 5 mV, V_{EE} = -5 mV		800	TBD	mW
		Write Mode, V_{CC} = 5 mV, V_{EE} = -5 mV		975	TBD	
		Write Mode, Reader Biased, V_{CC} = 5 mV, V_{EE} = -5 mV		1200	TBD	
		Idle Mode, V_{CC} = 5 mV, V_{EE} = -5 mV		140	TBD	
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL [1]	2.0		V_{CC} + 0.3	
Input Low Voltage	V_{IL}	PECL	V_{CC} - 1.9		V_{CC} - 1.6	V
		TTL [1]	-0.3		0.8	
Input High Current, V_{IH} = 3.5V	I_{IH}	PECL			120	µA
		TTL [1], V_{IH} = 2.7 V			80	
Input Low Current, V_{IL} = 1.65V	I_{IL}	PECL			100	µA
		TTL [1], V_{IL} = 0.4 V	-160			
Output High current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
VCC Fault Threshold	V_{DTH}		3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-4.25	-4.0	-3.75	V
High Level WDATA		PECL [2]	V_{CC} - 1.0		V_{CC} - 0.7	V
		Current Mode (sink)	25	100	200	µA
Low Level WDATA		PECL [2]	V_{CC} - 1.9		V_{CC} - 1.6	V
		Current Mode (sink)	0.8	1.0	1.2	mA

1. Input levels and currents apply for the following pins: DMY/RST, R/WN, BIASN/FAST, SCLK, SENA and SDIO.
2. Differential V_{PP} swing from 0.4V to 1.5V and the common mode should be such that for any of the two states the maximum high < VCC and the minimum low > 3V.

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 8mA, R_{EXT} = 2.0kΩ, R_{MR} = 60Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}	AMR Mask Option	4		10	mA
		GMR Mask Option	2		5	
MR Head Current Tolerance	I_{MR}	2mA < I_{MR} < 10 mA,	-5		+5	%
Unselected MR Head Current					15	µA
REXT Pin Voltage	V_{SET}			2.0		V
I_{REXT} to MR Bias Current Gain	A_{IMR}			5		mA/ mA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 10MHz, RL(RDP, RDN) = 1kΩ, Gain Bits = 00	120	150	180	V/V
		Gain Bits = 11	245	300	355	V/V
Passband Upper Frequency Limit	f_{HR}	-1dB	135	TBD		MHz
		FAST active, HFP = 1 -3dB	205	TBD		
Passband Lower Frequency Limit -3dB	f_{LR}		1.0	1.3	2.0	MHz
Passband Lower Frequency Limit	C_{LR}	FAST inactive -1dB	0.75	1	2.0	MHz
		FAST active, LFP = 11 -3dB	7.5	10	12.5	
Input Noise Voltage	e_n	1 MHz < f < 200 MHz		0.55	0.65	$\frac{nV}{\sqrt{Hz}}$
Input Noise Bias Current	i_n	1 MHz < f < 200 MHz		10	14	$\frac{pA}{\sqrt{Hz}}$
Noise Peaking		1 MHz < f < 10 MHz			6	dB
		10 MHz < f < 200 MHz			3	dB
Differential Input Capacitance	C_{IN}	Normal Mode		6	10	pF
Differential Input Resistance	R_{IN}	Normal Mode		320		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz	3			mV_{pp}

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 8mA, R_{EXT} = 2.0kΩ, R_{MR} = 60Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Total Harmonic Distortion	THD				0.5	%
Common Mode Rejection Ratio	CMRR	V_{CM} = 100 mVpp, 1 MHz < f < 100 MHz	40			dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, 1 MHz < f < 50 MHz	40			dB
		100mV_{pp} on VCC or VEE, 50 MHz < f < 100 MHz	34			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 1mV_{pp}, 1 MHz < f < 100 MHz	50			dB
Rejection of SCK and SDAT		100 mV_{pp} on pins, 1 MHz < f < 100 MHz	40			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}		VCC - 3.2	VCC -2.9	VCC -2.6	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			50	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		50		W
Output Current	I_O	AC Coupled Load, RDP to RDN	4			mA
MR Head Potential, Selected Head	V_{MR}		-500		500	mV
MR Head Potential, Unselected Head	V_{MR}		-1.0	-0.8		V
MR Bias Current Overshoot					0	%
TA Detection Response Time		TA occurred to FLT active		TBD		nS
Group Delay Variation		(20 - 3 dB cutoff) MHz			0.5	nS
BHV input referred	V_{OS}	Vos_{BHV}	-4		4	mV
BHV output referred			1.96	2.0	2.04	V
I_{MR} * R_{MR}			100		700	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 40mA b-p, L_H = 100nH, R_H = 10Ω, f_{DATA} = 5MHz.

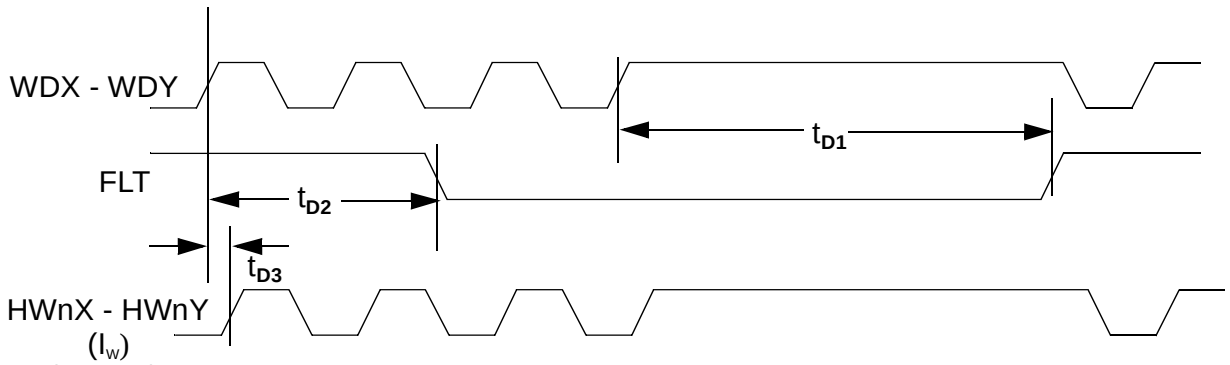
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R_{EXT} Pin Voltage	V_{REXT}			2.0		V
Write Current Range	I_W		10		50	mA
Write Current Tolerance	ΔI_W	$10 < I_W < 50$ mA	-8		8	%
Differential Head Voltage Swing	V_{DH}	Open Head		6		V_{BP}
Unselected Head Transition Current	I_{UH}	I_W=30mA b-p			50	μA_{pk}
Differential Output Capacitance	C_O				10	pF
Differential Output Resistance	R_O	Active Damping Resistance		TBD		W
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}		35			MHz

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 40mA b-p, L_H = 100nH, R_H = 10Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	F_{sclk}				30	MHz
R/WN to Write Mode	t_{RW}	To 90% of write current			50	ns
R/WN to Read Mode	t_{WR}	To 90% of envelope; DC offset level within 10 mV.			0.25	µs
Power Up to Read Mode (SENA falling edge)	t_{CS}	To 90% of envelope; DC offset level with nominal V			5	µs
HS0-3 to Any Head (SENA falling edge)	t_{HS}	To 90% of envelope, DC Offset Level within 10 mV, Fixed I_{MR}			1	µs
		To 90% of envelope, DC Offset Level within 10 mV, Variable I_{MR}			3	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			10	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0Ω			0.1	ns
Rise/Fall Time	t_r / t_f	10% - 90%, I_w = 40 mA b-p, L_H=60nH, R_H=13Ω.			1.5	ns
Write Current Overshoot	W_{COV}	I_w = 40 mA b-p, L_H=60nH, R_H=13Ω.		TBD		%

1. See Figure 116 for the write mode timing diagram.



In voltage mode:
When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode:
When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 116 Write Mode Timing Diagram

VM6203

10-CHANNEL BUMP COORDINATES

Specific Characteristics

Die size: 244 x 174 Mils

Pad Coordinates for the VM6203 (in Mils) are “bump down.”

Pin Name	X Axis	Y Axis	Pad Size
CS0	-117.441	-54.402	4x4
CS1	-117.441	-46.402	4x4
DMY/RST	117.441	-38.402	4x4
BIASN/ FAST	117.441	-46.402	4x4
FLT	44.220	-82.283	4x4
GND	53.547	-82.283	4x12
	61.547	-82.283	
GND	-117.441	-62.575	4x12
	-117.441	-70.575	
GNDA	-3.531	-82.283	4x4
GNDA	-35.417	-82.283	4x4
GNDA	-62.087	-82.283	4x12
	-70.087	-82.283	
HR0N	-101.689	8.634	4x4
HR0P	-101.689	0.634	4x4
HR1N	-101.689	16.634	4x4
HR1P	-101.689	24.634	4x4
HR2N	-101.689	72.634	4x4
HR2P	-101.689	64.634	4x4
HR3N	-65.110	66.571	4x4
HR3P	-57.110	66.571	4x4
HR4N	-9.110	66.571	4x4
HR4P	-17.110	66.571	4x4
HR5N	9.110	66.571	4x4
HR5P	17.110	66.571	4x4
HR6N	65.110	66.571	4x4
HR6P	57.110	66.571	4x4
HR7N	101.689	72.634	4x4
HR7P	101.689	64.634	4x4
HR8N	101.689	16.634	4x4
HR8P	101.689	24.634	4x4
HR9N	101.689	8.634	4x4
HR9P	101.689	0.634	4x4
HW0X	-101.689	-7.366	4x4
HW0Y	-101.689	-15.366	4x4
HW1X	-101.689	32.634	4x4
HW1Y	-101.689	40.634	4x4
HW2X	-101.689	56.634	4x4
HW2Y	-101.689	48.634	4x4
HW3X	-49.110	66.571	4x4
HW3Y	-41.110	66.571	4x4
HW4X	-25.110	66.571	4x4
HW4Y	-33.110	66.571	4x4
HW5X	25.110	66.571	4x4
HW5Y	33.110	66.571	4x4
HW6X	49.110	66.571	4x4
HW6Y	41.110	66.571	4x4
HW7X	101.689	56.634	4x4
HW7Y	101.689	48.634	4x4
HW8X	101.689	32.634	4x4
HW8Y	101.689	40.634	4x4
HW9X	101.689	-7.366	4x4
HW9Y	101.689	-15.366	4x4
NC	-117.441	-38.402	4x4
RDN	-15.429	-82.283	4x4
RDP	-23.520	-82.283	4x4
R/WN	14.559	-82.280	4x4
REXT	-44.795	-82.283	4x4
SCLK	117.441	-66.575	4x4
SDIO	117.441	-54.402	4x4
SENA	117.441	-75.961	4x4
VCC	69.547	-82.283	4x12
	77.547	-82.283	
VCCA	-78.087	-82.283	4x12
	-86.087	-82.283	
VEE	85.547	-82.283	4x12
	93.547	-82.283	
VEEA	-94.087	-82.283	4x12
	-102.087	-82.283	
WDX	35.484	-82.283	4x4
WDY	27.394	-82.283	4x4

VM6203

10-CHANNEL BOND COORDINATES

Specific Characteristics

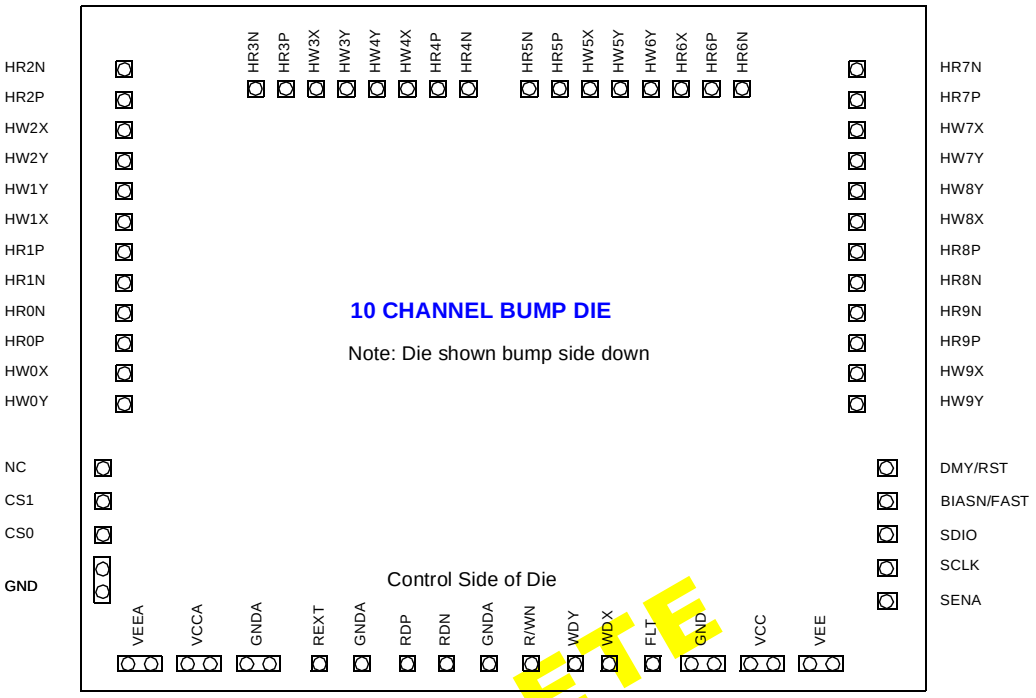
Die size: 244 x 174 Mils

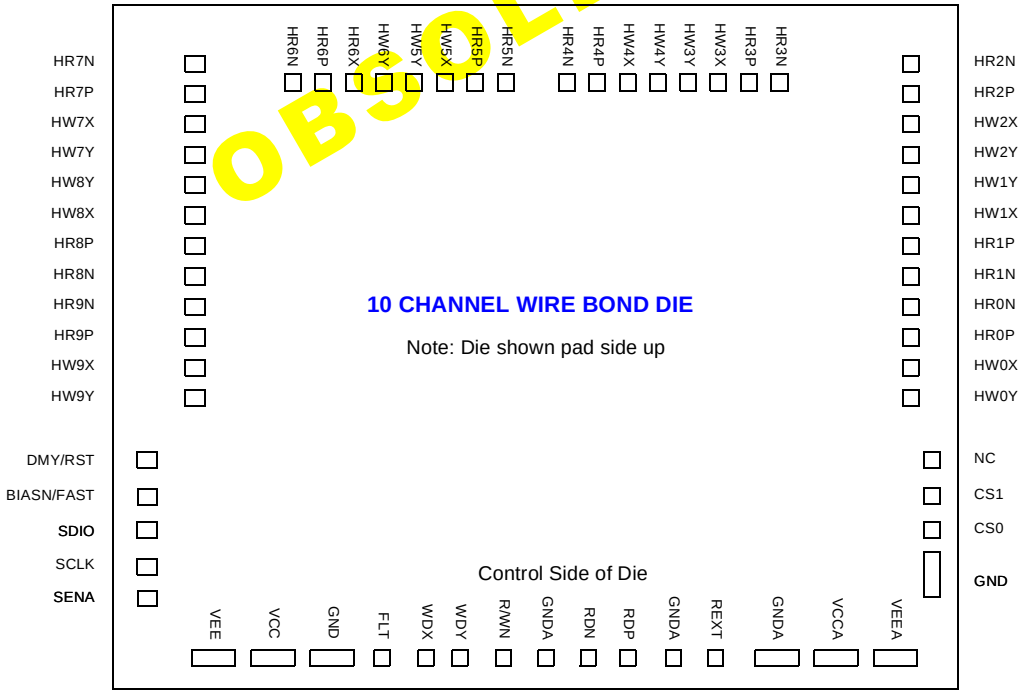
Bond Coordinates for the VM6203 (in Mils).

Pin Name	X Axis	Y Axis	Pad Size
CS0	117.441	-54.402	4x4
CS1	117.441	-46.402	4x4
DMY/RST	-117.441	-38.402	4x4
BIASN/ FAST	-117.441	-46.402	4x4
FLT	-44.220	-82.283	4x4
GND	-57.547	-82.283	4x12[1]
GND	117.441	-66.575	4x12[1]
GNDA	3.531	-82.283	4x4
GNDA	35.417	-82.283	4x4
GNDA	66.087	-82.283	4x12[1]
HR0N	101.689	8.634	4x4
HR0P	101.689	0.634	4x4
HR1N	101.689	16.634	4x4
HR1P	101.689	24.634	4x4
HR2N	101.689	72.634	4x4
HR2P	101.689	64.634	4x4
HR3N	65.110	66.571	4x4
HR3P	57.110	66.571	4x4
HR4N	9.110	66.571	4x4
HR4P	17.110	66.571	4x4
HR5N	-9.110	66.571	4x4
HR5P	-17.110	66.571	4x4
HR6N	-65.110	66.571	4x4
HR6P	-57.110	66.571	4x4
HR7N	-101.689	72.634	4x4
HR7P	-101.689	64.634	4x4
HR8N	-101.689	16.634	4x4
HR8P	-101.689	24.634	4x4
HR9N	-101.689	8.634	4x4
HR9P	-101.689	0.634	4x4
HW0X	101.689	-7.366	4x4
HW0Y	101.689	-15.366	4x4
HW1X	101.689	32.634	4x4
HW1Y	101.689	40.634	4x4
HW2X	101.689	56.634	4x4
HW2Y	101.689	48.634	4x4
HW3X	49.110	66.571	4x4
HW3Y	41.110	66.571	4x4
HW4X	25.110	66.571	4x4
HW4Y	33.110	66.571	4x4
HW5X	-25.110	66.571	4x4
HW5Y	-33.110	66.571	4x4
HW6X	-49.110	66.571	4x4
HW6Y	-41.110	66.571	4x4
HW7X	-101.689	56.634	4x4
HW7Y	-101.689	48.634	4x4
HW8X	-101.689	32.634	4x4
HW8Y	-101.689	40.634	4x4
HW9X	-101.689	-7.366	4x4
HW9Y	-101.689	-15.366	4x4
NC	117.441	-38.402	4x4
RDN	15.429	-82.283	4x4
RDP	23.520	-82.283	4x4
R/WN	-14.559	-82.280	4x4
REXT	44.795	-82.283	4x4
SCLK	-117.441	-66.575	4x4
SDIO	-117.441	-54.402	4x4
SENA	-117.441	-75.961	4x4
VCC	-73.547	-82.283	4x12[1]
VCCA	82.087	-82.283	4x12[1]
VEE	-89.547	-82.283	4x12[1]
VEEA	98.087	-82.283	4x12[1]
WDX	-35.484	-82.283	4x4
WDY	-27.394	-82.283	4x4

1. Double wide pad (4 x 12) coordinates are to the center of the pad

DIE PAD ORIENTATION





Application Notes:

OBSOLETE

VTC Inc.
Value The Customer™

VM6204 Series

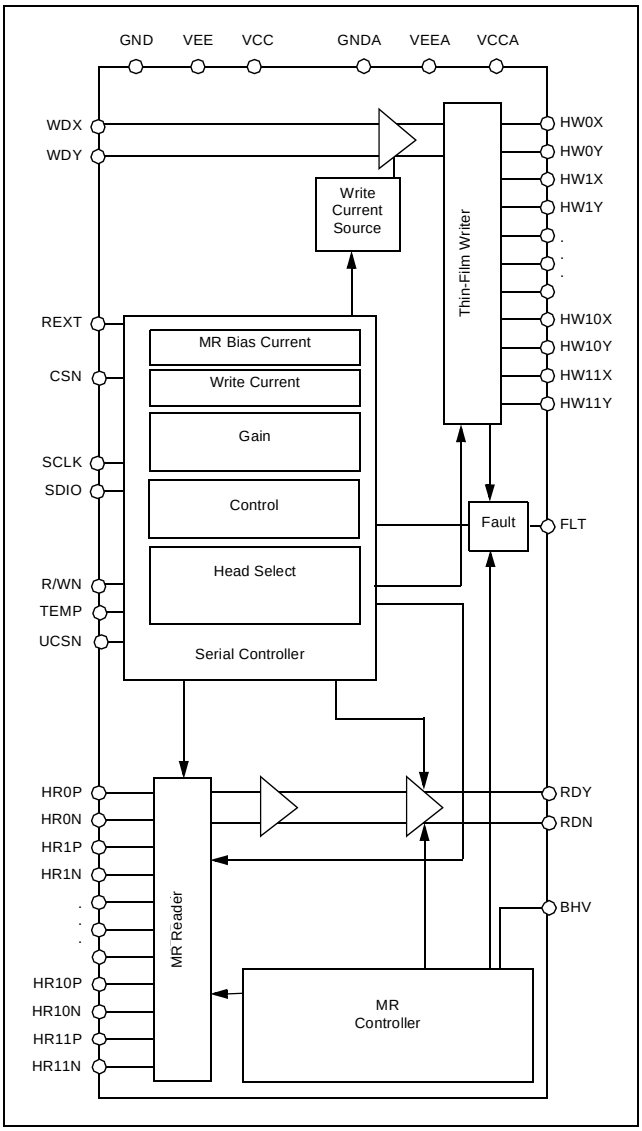
PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 350 Mbits/sec
  - Requires Only One External Component (R_{ext})
  - Designed for Use With Four-Terminal MR Heads
  - 2-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Gain and Head Selection)
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 12 Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC, 5 - 12 mA Range
  - Programmable Read Voltage Gain
    (220 V/V or 300 V/V Typical)
  - Buffered Head Voltage Output
  - Input Noise = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 6 pF Typical
  - Head Inductance Range = 10 nH - 150 nH
  - Bandwidths in Excess of 310 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 60 mA Range
  - Rise Time < 1.0 ns Typical
    (20-80%, L_{total} = 100 nH, I_W = 40 mA)

BLOCK DIAGRAM



DESCRIPTION

The VM6204 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6204 contains a thin-film head writer, an MR reader, and associated fault circuitry.

Compensation capacitors previously required as external components have been integrated into the VM6204. As a result, only one external component (Rext) is required. This advanced design greatly simplifies flex layouts.

Programmability of the VM6204 is achieved through a 2-line serial interface. Programmable parameters include MR bias current, write current, gain and head selection.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, the IDLEOVR bit (register 1:bit <D1>) initializes to 1 (idle mode) and an internal pull-up resistor is connected to the R/WN line to prevent accidental writing due to an open line.

The VM6204 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6204 is available in die form for chip-on-flex applications or a 80-pin TQFP. Please consult VTC for details.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 18mA
Write Current, I_W 90mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 20 - 60 mA
Write Head Inductance, L_W ..... 10 - 100 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 5 - 12 mA
Read Head Inductance, L_{MR} ..... 10 - 150 nH
Read Head Resistance, R_{MR} ..... 25 - 45 Ω (Imr*Rmr<600mV)
Junction Temperature, T_J ..... 0°C to 125°C

SERIAL INTERFACE CONTROLLER

The VM6204 uses a 2-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude.

See “SERIAL INTERFACE” on page 395 for protocol descriptions, bit and fault descriptions, and timing information.

Preamplifier Configuration and Selection

The VM6204 was designed for a single or multiple preamp configuration. All control lines may be shared (including the two serial lines SCLK and SDIO).

Pin UCSN determines the preamplifier’s upper/lower status in a dual preamp configuration. Pin UCSN floats high if left open, and the preamp assumes the “lower preamp” designation. If pin UCSN is tied to ground, the preamp will assume the “upper preamp” designation.

The UPCHP bit (0:<D4>) defines which preamp in a dual preamp configuration was read via the serial interface. A high indicates the upper preamp was read, a low indicates the lower preamp. Serial write operations are performed on both preamps in a dual preamp configuration. The UPCHP bit does not effect servo write operations to multiple channels using the DUALW function (1:<D3>).

The PWREN bit (1:<D4>) places the inactive (unselected) preamp in either Standby or Idle mode.

The DUALW bit (1:<D3>) invokes a special mode where both preamps respond to the lower preamp address field. This Dual Write mode reduces servo write time in a dual preamp configuration.

See Tables 170 and 171 for Mode Select information.

MODES OF OPERATION

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the mode control circuitry and the serial registers (the contents of which remain latched).

Idle mode is selected by taking the CSN pin high.

Note: Setting the IDLEOVR bit high (1:<D1>) forces Idle mode, regardless of the state of the CSN pin.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6204 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{(k_{IMR} \times 0.602) + 13.34}{R_{ext}} \times \left[\frac{385}{R_{MR} + 340}\right] \qquad \textit{(eq. 87)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

MR head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±300mV of ground and unselected heads are held at approximately -800mV.

Read Gain

The gain is nominally 220 V/V with a head resistance of 45Ω. The formula that describes the actual gain is shown below:

$$A_V = \frac{385}{340 + R_{MR}} \times 220 \qquad \textit{(eq. 88)}$$

Note: Setting the GAIN bit high (3:<D5>) selects a nominal gain of 300 V/V.

MR Bias Enable

Setting the BIASOVR bit (1:<D2>) high activates bias current.

MR Bias DAC

The 5 bits in register 3 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

BHV (Buffered Head Voltage)

Setting the BHVOE bit high (1:<D5>) enables the output of the ($I_{MR} \times R_{MR}$)×5 product of the selected head at the BHV pin. This output is single-ended with respect to ground. When bit BHVOE is reset, the output pin BHV enters a low-impedance (low-Z) state to minimize noise coupling.

Note: The reader outputs are disabled.

Fast Read Mode

Setting the FAST bit high (1:<D0>) increases the high-pass corner frequency of the amplifier’s bandpass from a value of 300 kHz to 2.0MHz nominal.

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Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
- Invalid head select code
- Device in write mode

Read Inactive Mode

Taking the BIASOVR bit low in Read mode or selecting an invalid head (setting both the HS3 and HS2 bits high; 0, bits <D3-D2>) invokes a “Read Inactive” mode where bias current is diverted internally to a dummy head and the FLT pin goes low.

The chip drives the RDP/RDN outputs to normal levels and its power consumption is unaffected.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{(k_{IW} \times 3.44) + 53.34}{R_{ext}}\right]\left(\frac{1}{1 + \frac{R_H}{R_D}}\right) \qquad \textit{(eq. 89)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
R_H represents the series head resistance (in kΩ).
R_D represents the damping resistance (in kΩ).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 119 for the timing diagram.

Write Current DAC

The 5 bits in register 2 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Setting the BIASOVR bit high (1:<D2>) in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Dual Write Mode

Setting the DUALW bit high (1:<D3>) initiates a special Dual Write mode.

Dual Write mode allows the writing of one channel in each of two preamps in a dual preamp configuration. When set, both preamps respond to the lower preamp address field.

This mode reduces servo write time when there are two preamps in a single head-disk assembly.

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open write head
- No write current

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Invalid head select code
- Low power supply voltage
- Device in read or idle mode
- Head shorted to ground

Note: Invalid head and head shorted faults are latched and can only be cleared by toggling either the R/WN pin or the CSN pin.

Standby Mode (Inactive Preamp Only)

This special mode allows for power management of the inactive preamp in dual preamp configurations.

Setting the PWREN bit high (1:<D4>) places the inactive preamp in a reduced power consumption Standby mode. Bias current is diverted internally, outputs are not driven, and the serial register remains active. This mode facilitates a rapid recovery when the inactive preamp is selected.

Idle Mode (Inactive Preamp Only)

Setting the PWREN bit low (1:<D4>) places the inactive preamp in a minimal power consumption Idle mode.

All fault detection circuitry is disabled in this mode.

Temperature

The die temperature can be determined by monitoring the voltage at the TEMP pin. This pin is nominally two diode drops above ground. The voltage must be calibrated at known temperatures to determine the voltage change over the temperature range.

MODE SELECTION

- The UCSN pin identifies a preamp as ‘lower” when high and as ‘upper’ when low.
- The UPCHP bit (0:<D4>) selects the upper preamp when high (in a dual preamp configuration) and the lower preamp when low.

Table 170Mode Select (for the Selected Preamp) (UCSN=1, UPCHP=0) or (UCSN=0, UPCHP=1)

CSN	*R/WN*	*BIASOVR 1:<D2>*	*HS3 0:<D3>*	*HS2 0:<D2>*	*MODE*
1	X	X	X	X	Idle
0	1	1	valid head		Read
0	1	0	X	X	Read Inactive (bias to dummy head)
0	X	X	1	1	
0	0	0	valid head		Write
0	0	0	1	1	Write (Write Current Disabled)
0	0	1	valid head		Write with Read Bias Enabled
0	0	1	1	1	Write with Read Bias Enabled (Write Current Disabled)

- The IDLEOVR bit (1:<D1>) forces Idle mode when set high.

Note: Invalid mode selection will select Idle mode.

Table 171Mode Select (for the Unselected Preamp) (UCSN=1, UPCHP=1) or (UCSN=0, UPCHP=0)

PWREN 1:<D4>	*MODE*
0	Idle
1	Standby

- The PWREN bit (1:<D4>) allows for power management of the inactive (unselected) preamp in a dual preamp configuration. When high, the inactive preamp is placed in Standby mode (with reduced power consumption). When low, the inactive preamp is placed in Idle mode (with minimal power consumption).

Note: If the UCSN lines are tied together, taking the CSN pin high places both preamps (in a dual preamp configuration) in the Idle mode.

Note: Setting the DUALW bit high (1:<D3>) initiates a special Dual Write mode that allows the writing of one channel in each of two preamps (both selected and unselected) in a dual preamp configuration. See “Dual Write Mode” on page 393.

Table 172Head Select

HS3 0:<D3>	*HS2 0:<D2>*	*HS1 0:<D1>*	*HS0 0:<D0>*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	X	X	invalid head [1]

1. In Write mode, an invalid head select will disable the writer, dump the head selection current to the positive supply and register a fault.
In Read mode, an invalid head select will force “Read Inactive” mode, divert the read current to a dummy head and register a fault.

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SERIAL INTERFACE

The serial interface has one input line, SCLK (serial clock), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. When the serial register is powered down only the output D-latches and the reference generators remain active. 19 bits constitutes a complete data packet.

A sequence of null bits must precede the data packet to ensure proper framing of the data packet. 18 null bits <R17 - R0> are required to initialize the serial register after the initial application of power. Once initialized, only one null bit must precede each data packet.

The first ten bits of a data packet are write-only and consist of one synchronization bit <S>, an unused bit <A6>, three register address bits <A5-A3>, three preamp select bits <A2-A0>, one read/write bit <RN/W>, and one turnaround bit <T>. The next nine bits consist of 8 data bits <D7-D0> to be written-to or read-from a register and a postamble bit <P> (signifying the end of a data packet).

A data transfer is initiated upon the assertion of the serial clock (SCLK). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 19 cycles; on the 19th rising edge, the data will be written to the addressed register. During a read sequence, SDIO will become active on the falling edge of the 11th cycle. At this time <D7> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. The presentation of the postamble bit in the 19th falling edge signifies the end of the data transfer. The serial interface will only be fully powered between the synchronization and postamble bits.

The finite state machine in the preamp serial interface block must unconditionally complete a transfer sequence by ending in a state where the preamp loads the SDIO line by less than ±160µA (TS). The power-on-reset condition for SDIO is tristate/input mode.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 173 and 174 for a bit description. See Table 176 and Figure 118 for serial interface timing information.

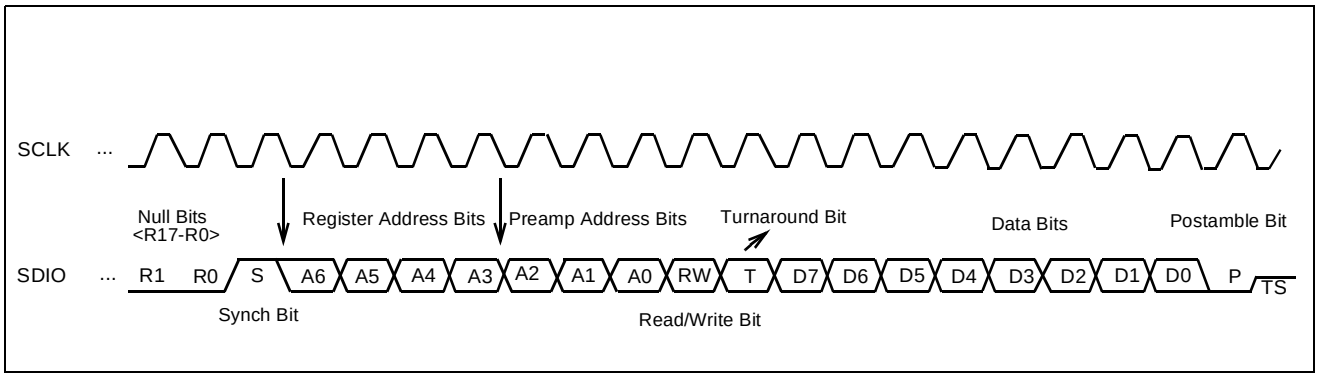

Figure 117 Serial Interface Protocol

Fault Detection

A fault condition is triggered by any of the following serial interface conditions:

28) Address fault - If address bits <A5-A3> select an invalid address or when preamp select bits <A2-A0> ≠ 000, the FLT pin is set and further write or read operations cannot be performed until the serial interface is reset.

29) No end of packet bit - If the 19th falling edge of SCLK is not a low signal, the FLT pin is set and further write operations cannot be performed until the serial interface is reset.

All serial interface faults are cleared on the next serial interface operation.

Table 173Serial Interface Bit Description -- Address Bits

Function	Register #	Register Address Bits				Preamp Address Bits			R/W bit
		<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>	
Head Select	0	1	0	0	0	0	0	0	1/0 [2]
Control	1	1	0	0	1				1/0 [2]
Write Current DAC	2	1	0	1	0				1/0 [2]
MR Bias Current DAC	3	1	0	1	1				1/0 [2]
Vendor ID	4 (read only)	1	1	0	0				0 [2]

1. Reserved
2. R/W Address bit: Read = 0, Write = 1

Table 174Serial Interface Bit Description -- Data Bits

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Head Select	0	1	1	1	UPCHP [2]	HS3	HS2	HS1	HS0
Control	1	1	1	BHVOE	PWREN	DUALW	BIASOVR	IDLEOVR	FAST
Write Current DAC	2	1	1	1	IW4	IW3	IW2	IW1	IW0
MR Bias Current DAC / Gain	3	1	1	GAIN	IMR4	IMR3	IMR2	IMR1	IMR0
Vendor ID	4 (read only)	0	0	1	1	0	0	0	1

1. Reserved
2. Dual preamp configuration only, 1 = Upper Preamp and 0 = Lower Preamp. See Preamplifier Configuration and Selection on page 392 for more information.

Table 175Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Head Select	0	<0001 1111>
Control	1	<0000 0010>
Write Current DAC	2	<0000 0000>
MR Bias Current DAC	3	<0000 0000>
Vendor ID	4	<0011 0001>

Table 176Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) Rate				40	MHz
SCLK cycle time	T_c	20			ns
SCLK high time	T_{ckh}	8			ns
SCLK low time	T_{ckl}	8			ns
SCLK risetime (10 - 90%)		0.8		5	ns
SDIO setup time, write	T_s	6			ns
SDIO delay time, read		8			ns
SDIO hold time, write	T_h	1			ns
SDIO hold time, read		3			ns
SDIO risetime (10 - 90%)		0.8		7	ns
Time between I/O operations		25			ns

Note: SerEna assertion level is high.

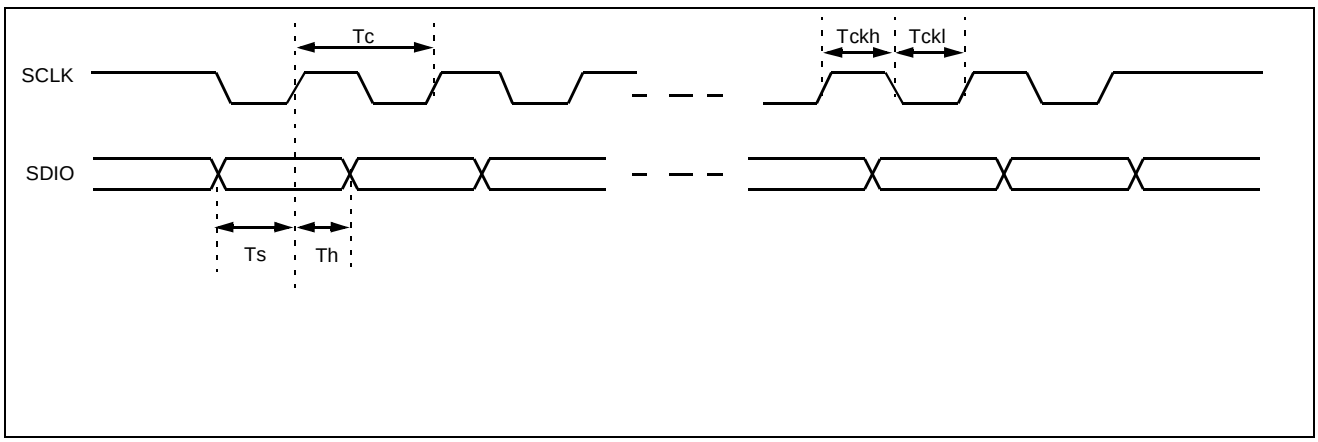

Figure 118 Serial Interface Timing

PIN_FUNCTION LIST AND DESCRIPTION

Symbol	*Input/ Output* [1]	*Description*
BHV	O	Buffered MR Head Voltage output.
CSN	I [2]	Chip Select: A TTL high level initiates Idle mode. A TTL low level enables operation. If left disconnected, the input defaults to a high state. Note that the IDLEOVR bit (1:<D1>) also forces Idle mode.
FLT	O [2]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
GND	[2]	Ground
GNDA	[2]	Analog Ground
HR0P-HR11P	I	MR head connections, positive end.
HR0N-HR11N	I	MR head connections, negative end.
HW0X-HW11X	O	Thin-Film write head connections, positive end.
HW0Y-HW11Y	O	Thin-Film write head connections, negative end
REXT		Reference Voltage pin for both MR bias current and write current.
RDP, RDN	O [2]	Read Data: Differential read signal outputs.
R/WN	I [2]	Read/Write: A TTL low level enables write mode. Pin defaults high (read).
SCLK	I [2]	Serial Clock: Serial port clock; see Figure 171.
SDIO	I/O [2]	Serial Data: Serial port data; see Figure 171.
TEMP	I [2]	Temperature: Two diode drop voltage to measure die temperature.
UCSN	I	Upper Chip Select: A TTL low level designates preamp as the “upper” preamp. A TTL high level designates preamp as the “lower” preamp. Pin defaults high (lower preamp designation).
VCC	[2]	+5.0V supply
VCCA	[2]	Analog +5.0V supply
VEE	[2]	-5.0V supply
VEEA	[2]	Analog -5.0V supply
WDX, WDY	I [2]	Differential Pseudo-ECL write data inputs.

1. I = Input pin, O = Output pin
2. When more than one device is used, these signals can be wire-OR’ed together.

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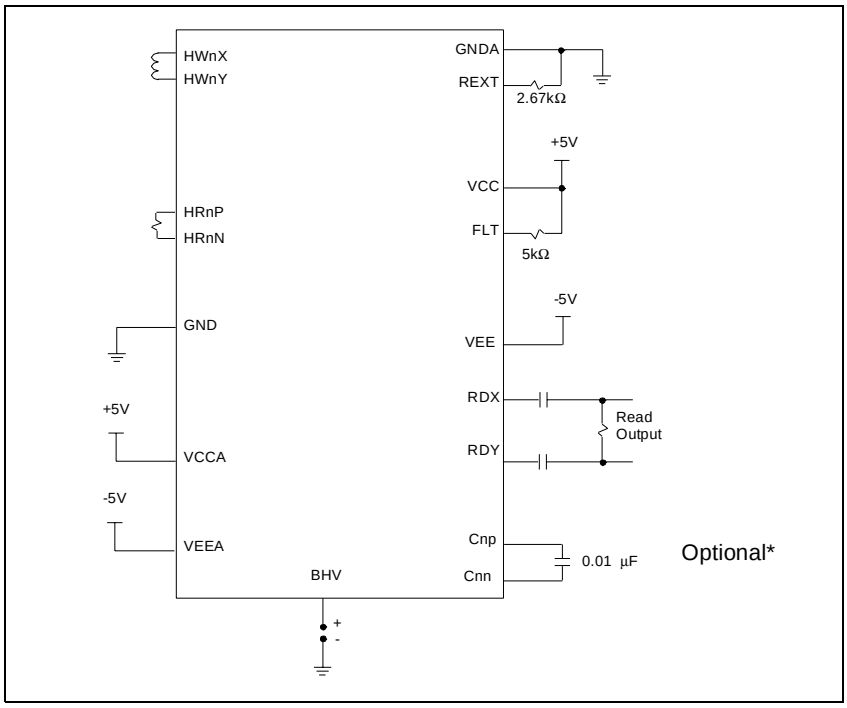
TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors and the R_{EXT} resistor as close to the pins/pads as possible.
- Optional*
  An optional additional supply noise bypass capacitor may be incorporated at the Cnp/Cnn pins/pads.
  Minimizing parasitics at the Cnn/Cnp node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 10 mA, I_W = 40 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode		115	TBD	mA
		Write Mode		105	TBD	
		Write Mode, Reader Biased		155	TBD	
		Idle Mode		20	TBD	
V_{EE} Power Supply Current	I_{EE}	Read Mode		40	TBD	mA
		Write Mode		70	TBD	
		Write Mode, Reader Biased		88	TBD	
		Idle Mode		2	TBD	
Power Supply Dissipation	P_d	Read Mode		775	TBD	mW
		Write Mode		875	TBD	
		Write Mode, Reader Biased		1200	TBD	
		Idle Mode		110	TBD	
Input High Voltage	V_{IH}	PECL	1.8		V_{CC}-0.7	V
		TTL	2.0		V_{CC}+0.3	
Input Low Voltage	V_{IL}	PECL	1.4		V_{IH}-0.4	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH}=2.7V			80	
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL}=0.4V	-160			
Output High current	I_{OH}	FLT: V_{OH}=5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL}=4mA			0.6	V
V_{CC} Fault Threshold	V_{DTH}		3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.8	-3.55	-3.3	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 10mA, R_{EXT}=2.67kΩ, R_{MR} = 45Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}		5		12	mA
MR Head Current Tolerance	I_{MR}	5mA < I_{MR} < 12 mA	-5		+5	%
Unselected MR Head Current					15	µA
REXT Pin Voltage	V_{SET}			2.0		V
I_{REXT} to MR Bias Current Gain	A_{IMR}			5		mA/mA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 10MHz, RL(RDP, RDN) = 1kΩ, Gain Bit=0 Gain = 385/(340+R_{MR})*220	180	220	260	V/V
		Gain Bit=1 Gain = 385/(340+R_{MR})*300	245	300	355	V/V
Passband Upper Frequency Limit	f_{HR}	Normal mode -1dB	135	TBD		MHz
		-3dB	250	280		
Passband Lower -3dB Frequency Limit	f_{LR}	Normal mode	0.1	0.7	0.9	MHz
		Fast mode, Lower 3dB	1.5	2.5	3.5	MHz
Input Noise Voltage	e_n	1 MHz < f < 20 MHz		0.55	0.65	nV/√Hz
Input Noise Bias Current	i_n	1 MHz < f < 20 MHz		10	14	pA/√Hz
Differential Input Capacitance	C_{IN}	Normal Mode		6	10	pF
Differential Input Resistance	R_{IN}	Normal Mode	TBD	340		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz	3			mV_{pp}
Total Harmonic Distortion	THD				2	%
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, 1 MHz < f < 135 MHz	40			dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{EE}, 2 MHz < f < 135 MHz	40			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 2 MHz < f < 135 MHz	30			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.2	V_{CC} -2.9	V_{CC} -2.6	V
Common Mode Output Voltage Difference	ΔV_{OCM}	Read Mode to Write Mode	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		50		W
Output Current	I_O	AC Coupled Load, RDP to RDN	4			mA
MR Head Potential, Selected Head	V_{MR}		-400		400	mV

READ CHARACTERISTICS

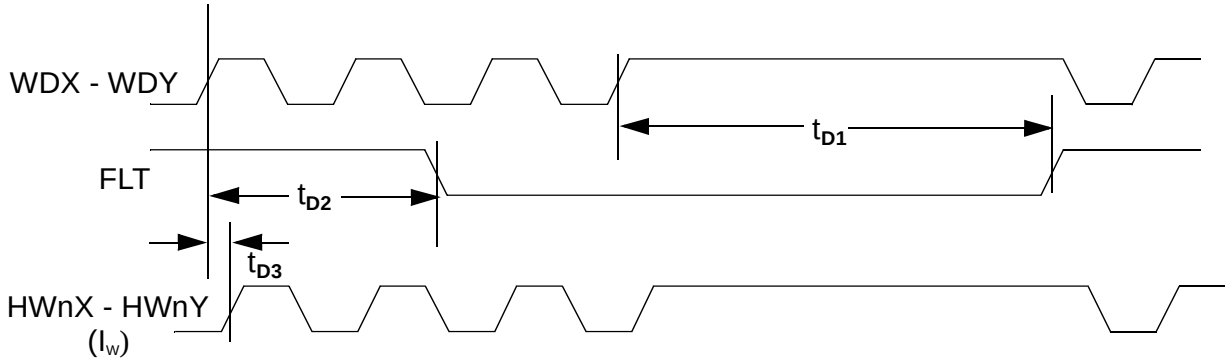
Recommended operating conditions apply unless otherwise specified: I_{MR} = 10mA, R_{EXT}=2.67kΩ, R_{MR} = 45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Potential, Unselected Head	V_{MR}		-1	-.8		V
Buffered Head Voltage Gain	A_{BHV}		4.9	5	5.1	V/V
BHV input referred V_{OS}	Vos_{BHV}		-4		+4	mV
I_{MR}*R_{MR}			100		600	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 40mA, L_H = 100nH, R_{EXT}=2.67kΩ, R_H = 10Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REXT Pin Voltage	V_{SET}			2.0		V
I_{REXT} to Write Current Gain	A_I			20		mA/mA
Write Current Range	I_W		20		60	mA
Write Current Tolerance	ΔI_W	20 < I_W < 60 mA	-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head		6		V_{pk}
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400			mV_{ppd}
Unselected Head Transition Current	I_{UH}	I_W=30mA			100	μA_{pk}
Differential Output Capacitance	C_O				10	pF
Differential Output Resistance	R_O	Damping Resistance present		TBD		Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}		35			MHz
Input Termination Resistance				300		Ω



In voltage mode:
When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode:
When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 119 Write Mode Timing Diagram

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: f_{DATA} = 5MHz, L_H = 100nH, R_H = 10Ω, I_W = 40mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			100	ns
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope; ±20mV of final DC value		250	500	ns
PWRUP to Read Mode (SCLK 19th rising edge)	t_{CS}	To 90% of envelope; ±20mV of final DC value			10	µs
HS0-3 to Any Head (SCLK 19th rising edge) Read Mode	t_{HS}	To 90% of envelope; ±20mV of final DC value Constant IMR			1	µs
		To 90% of envelope; ±20mV of final DC value Min to Max IMR Change			3	µs
HS0-3 to Any Head (SCLK 19th rising edge) Servo Write Mode	t_{SHS}	To 90% of write current; Constant I_W			1	µs
SCLK (19th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0			0.1	ns
Rise/Fall Time	t_r / t_f	20% - 80%		0.950	1.2	ns

1. See Figure 119 for the write mode timing diagram.

VM6204 PACKAGING

12-Channel Die

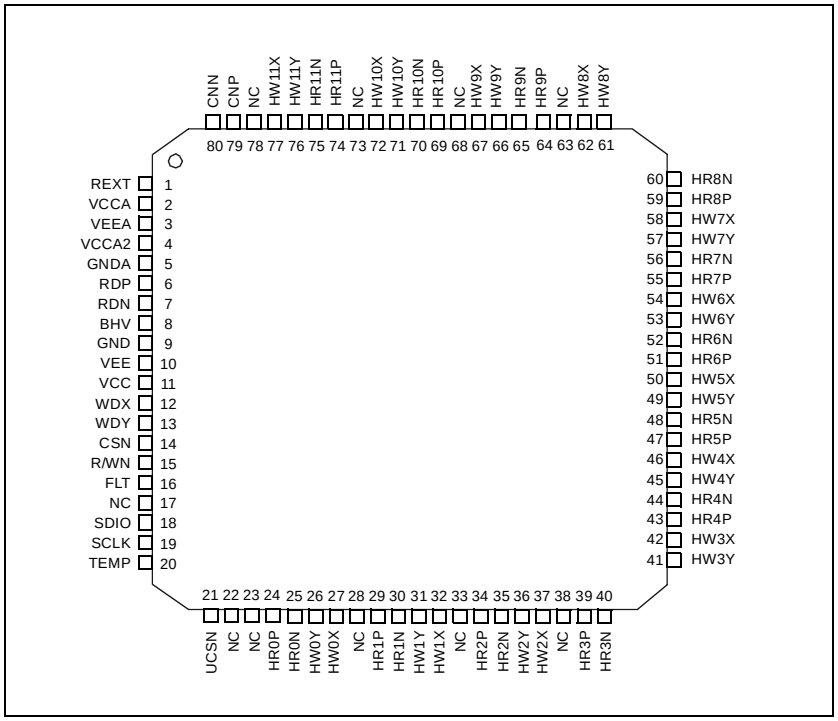
Specific Characteristics

Die size: 220 x 156 Mils

Wire Bond Coordinates for the VM6204 (in Mils)

Pin Name	X Axis	Y Axis	Pad Size
BHV	-5.394	-73.441	4x4
CnN	-90.697	-70.854	4x4
CnP	-90.697	-64.043	4x4
CSN	55.906	-73.441	4x4
FLT	69.528	-73.441	4x4
GND	1.417	-73.441	4x8
GND	8.228	-73.441	4x8
GNDA	-30.917	-73.441	4x8
GNDA	-34.815	-73.441	4x8
HR0N	90.697	-38.449	4x4
HR0P	90.697	-45.260	4x4
HR1N	90.697	-10.906	4x4
HR1P	90.697	-17.717	4x4
HR2N	90.697	17.378	4x4
HR2P	90.697	10.567	4x4
HR3N	78.209	58.622	4x4
HR3P	85.020	58.622	4x4
HR4N	49.917	58.622	4x4
HR4P	56.728	58.622	4x4
HR5N	22.303	58.622	4x4
HR5P	29.114	58.622	4x4
HR6N	-15.492	58.622	4x4
HR6P	-8.681	58.622	4x4
HR7N	-43.106	58.622	4x4
HR7P	-36.295	58.622	4x4
HR8N	-71.398	58.622	4x4
HR8P	-64.587	58.622	4x4
HR9N	-90.697	24.189	4x4
HR9P	-90.697	31.000	4x4
HR10N	-90.697	-4.094	4x4
HR10P	-90.697	2.717	4x4
HR11N	-90.697	-31.610	4x4
HR11P	-90.697	-24.799	4x4
HW0X	90.697	-24.827	4x4
HW0Y	90.697	-31.638	4x4
HW1X	90.697	2.717	4x4
HW1Y	90.697	-4.094	4x4
HW2X	90.697	31.000	4x4
HW2Y	90.697	24.189	4x4
HW3X	64.587	58.622	4x4
HW3Y	71.398	58.622	4x4
HW4X	36.295	58.622	4x4
HW4Y	43.106	58.622	4x4
HW5X	8.681	58.622	4x4
HW5Y	15.492	58.622	4x4
HW6X	-29.114	58.622	4x4
HW6Y	-22.303	58.622	4x4
HW7X	-56.728	58.622	4x4
HW7Y	-49.917	58.622	4x4
HW8X	-85.020	58.622	4x4
HW8Y	-78.209	58.622	4x4
HW9X	-90.697	10.567	4x4
HW9Y	-90.697	17.378	4x4
HW10X	-90.697	-17.717	4x4
HW10Y	-90.697	-10.906	4x4
HW11X	-90.697	-45.232	4x4
HW11Y	-90.697	-38.421	4x4
NC	74.150	-73.441	4x4
R/WN	62.717	-73.441	4x4
RDN	-14.118	-73.441	4x4
RDP	-22.209	-73.441	4x4
REXT	-70.941	-73.441	4x4
SCLK	87.772	-73.441	4x4
SDIO	80.961	-73.441	4x4
TEMP	94.583	-73.441	4x4
UCSN	101.406	-73.441	4x4
VCC	28.661	-73.441	4x8
VCC	35.472	-73.441	4x8
VCCA	-60.212	-73.441	4x8
VCCA	-64.110	-73.441	4x8
VCCA2	-41.965	-73.441	4x4
VEE	15.039	-73.441	4x8
VEE	21.850	-73.441	4x8
VEEA	-49.130	-73.441	4x8
VEEA	-53.028	-73.441	4x8
WDX	42.283	-73.441	4x4
WDY	49.094	-73.445	4x4

12-Channel 80-lead TQFP Pinout



VTC Inc.
Value The Customer™

VM6205 Series

PROGRAMMABLE, ±5 VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

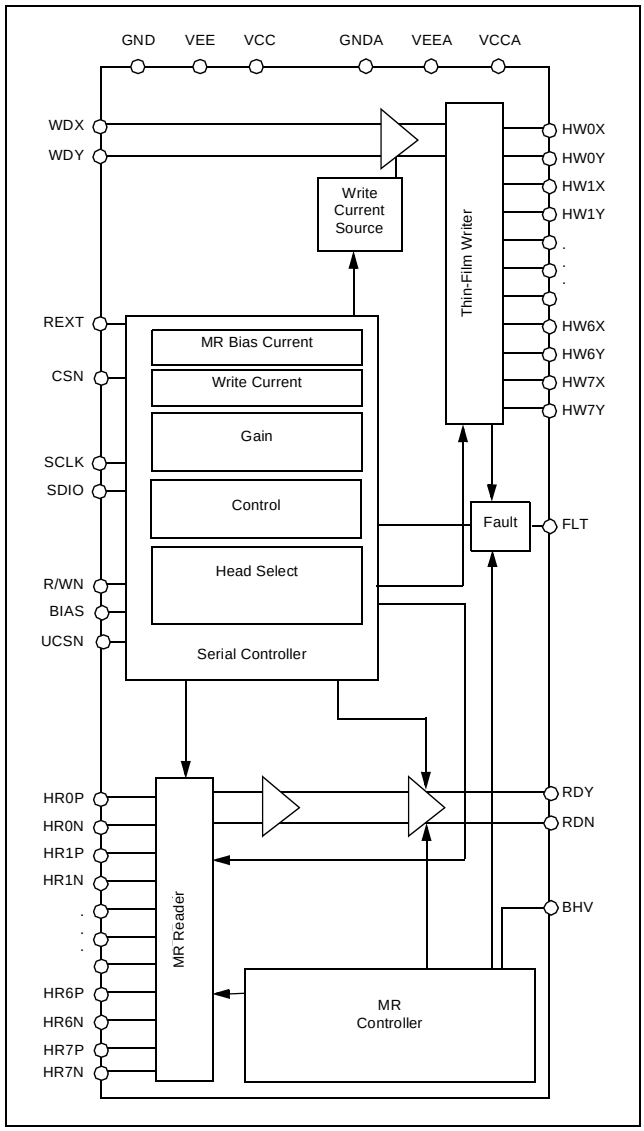
990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- Transfer Rates in Excess of 350 Mbits/sec
- Requires Only One External Component (R_{ext})
- Designed for Use With Four-Terminal MR Heads
- 2-Line Serial Interface
  (Provides Programmable Bias Current, Write Current, Gain and Head Selection)
- Die Temperature Monitor Capability
- Operates from +5 and -5 Volt Power Supplies
- Up to 8 Channels Available
- Fault Detect Capability

- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC, 2 - 8 mA Range
  - Programmable Read Voltage Gain
    (220 V/V or 150 V/V Typical)
  - Buffered Head Voltage Output
  - Input Noise = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 2 pF Typical
  - Head Inductance Range = 10 nH - 150 nH
  - Bandwidths in Excess of 310 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 60 mA Range
  - Rise Time < 1.0 ns Typical
    (20-80%, L_{total} = 100 nH, I_W = 40 mA)
  - Bank Write Capability

BLOCK DIAGRAM



DESCRIPTION

The VM6205 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6205 contains a thin-film head writer, an MR reader, and associated fault circuitry.

Compensation capacitors previously required as external components have been integrated into the VM6205. As a result, only one external component (Rext) is required. This advanced design greatly simplifies flex layouts.

Programmability of the VM6205 is achieved through a 2-line serial interface. Programmable parameters include MR bias current, write current, gain and head selection.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, the IDLEOVR bit (register 1, bit <D1>) initializes to 1 (idle mode) and an internal pull-up resistor is connected to the R/WN line to prevent accidental writing due to an open line.

The VM6205 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6205 is an 8 channel device in die form for chip-on-flex applications or as an 80-pin TQFP. Please consult VTC for details.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +6V

Read Bias Current, I_{MR} 18mA
Write Current, I_W 90mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 20 - 60 mA
Write Head Inductance, L_W ..... 10 - 100 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 2 - 8 mA
Read Head Inductance, L_{MR} ..... 10 - 150 nH
Read Head Resistance, R_{MR} ..... 35 - 70 Ω (Imr*Rmr<600mV)
Junction Temperature, T_J ..... 0°C to 125°C

SERIAL INTERFACE CONTROLLER

The VM6205 uses a 2-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude.

See “SERIAL INTERFACE” on page 411 for protocol descriptions, bit and fault descriptions, and timing information.

Preamplifier Configuration and Selection

The VM6205 was designed for a single or multiple preamp configuration. All control lines may be shared (including the two serial lines SCLK and SDIO).

Pin UCSN determines the preamplifier’s upper/lower status in a dual preamp configuration. Pin UCSN floats high if left open, and the preamp assumes the “lower preamp” designation. If pin UCSN is tied to ground, the preamp will assume the “upper preamp” designation.

Setting the WSER bit high (1:<D3>) selects the servo write mode. See “Servo Write Mode” on page 409 for further information.

See Tables 170 for Mode Select information.

Die Temperature Monitor Capability

A diode is connected to the BIAS pin to provide for the monitoring of die temperature. This diode is referenced to GND.

Sink DC current from the BIAS pin (100µA to 1mA) and monitor the voltage with respect to GND. VTC recommends calibrating the diode in Idle mode initially.

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the mode control circuitry and the serial registers (the contents of which remain latched).

Idle mode is selected by taking the CSN pin high.

Serial interface fault detection is active in this mode, but write and read fault detection is disabled.

Note: Setting the IDLEOVR bit high (1:<D1>) forces Idle mode, regardless of the state of the CSN pin.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6205 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{(k_{IMR} \times 0.516) + 5.34}{2670}\left(\frac{390}{340 + R_{MR}}\right) \quad \textit{(eq. 87)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{MR} represents the resistance of the MR element (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

MR head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±300mV of ground and unselected heads are held at approximately -800mV.

Read Gain

The gain is nominally 220 V/V with a head resistance of 50Ω. The formula that describes the actual gain is shown below:

$$A_V = \frac{390}{340 + R_{MR}} \times 220 \quad \textit{(eq. 88)}$$

Setting the GAIN bit high (3:<D5>) selects a nominal gain of 150 V/V.

MR Bias Enable

Taking the BIAS pin high activates the MR Bias current. to the specified head. Note that setting the BIASOVR bit (1:<D2> high also activates bias current.

Note: Taking the BIAS pin low invokes a “Read Inactive” mode where bias current is diverted internally to a dummy head. See “Read Inactive Mode” on page 409.

MR Bias DAC

5 bits (3:<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

BHV (Buffered Head Voltage)

Setting the BHVOE bit high (1:<D5>) enables the output of the $(I_{MR} \times R_{MR}) \times 5$ product of the selected head at the BHV pin. This output is single-ended with respect to ground. RDX/RDY remains enabled when BHV is enabled. When bit BHVOE is reset, the output pin BHV enters a low-impedance (low-Z) state to minimize noise coupling.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Fast Read Mode

Setting the FAST bit high (1:<D0>) increases the high-pass corner frequency of the amplifier's bandpass from a nominal value of 1 MHz to 2 MHz.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
- Device in write mode

Read Inactive Mode

Taking the BIAS pin low in Read mode invokes a "Read Inactive" mode where bias current is diverted internally to a dummy head and the FLT pin goes low.

The chip drives the RDP/RDN outputs to normal levels and its power consumption is unaffected.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the write current magnitude:

$$I_W = \frac{k_{IW} x 3.44 + 53.34}{R_{ext}} \qquad \textit{(eq. 89)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 120 for the timing diagram.

Write Current DAC

5 bits (2:<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIAS pin high in write mode enables MR bias current to the selected head. The read circuitry is in its normal "read" state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Note: Bias must be active 5µs before a write-to-read transition.

Note: Setting the BIASOVR bit high (1:<D2>) forces bias current to the selected head, regardless of the setting of the BIAS pin.

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open write head (detectable up to 66 MHz)
- No write current

Note: Open head faults will be reported for approximately 1 µs.

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Low power supply voltage
- Device in read or idle mode

Note: Invalid head and head shorted faults are latched and can only be cleared by toggling either the R/WN pin or the CSN pin.

Servo Write Mode

The VM6205 is designed for use in a single preamp configuration. Servo may be written to two heads of a single preamp.

Register 4: <D1-D0> are the servo control bits. See Table 175 for a servo register bit description information.

Note: It is the customer's responsibility to ensure the thermal constraints of the die/flex/package are not exceeded. This may be achieved by lowering the supply voltage, reducing the write current or cooling the device.

ESD PROTECTION FOR MR HEAD

Characteristics for ESD diodes at MRP and MRN pins are:.

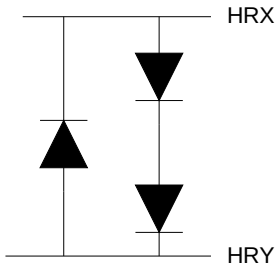


Figure 117 ESD Protection of MR Heads

MODE SELECTION

Table 170Mode Select (for the Selected Preamp)

WSER	*CSN*	*R/WN*	*BIAS*	*HS2 0:<D2>*	*MODE*
X	1	X	X	X	Idle
X	0	1	1	valid head	Read
X	0	1	0	X	Read Inactive (bias to dummy head)
0	0	0	0	valid head	Write
0	0	0	1	valid head	Write with Read Bias Enabled
1	0	0	X	X	Servo

- The IDLEOVR bit (1:<D1>) forces Idle mode when set high.
- The BIASOVR bit (1:<D2>) forces bias current when set high.

Note: Invalid mode selection will select Idle mode.

Note: Setting the WSER bit high (1:<D3>) initiates servo mode. See “Servo Write Mode” on page 409.

Table 171Head Select

HS2 0:<D2>	*HS1 0:<D1>*	*HS0 0:<D0>*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

SERIAL INTERFACE

The serial interface has one input line, SCLK (serial clock), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. When the serial register is powered down only the output D-latches and the reference generators remain active. 19 bits constitutes a complete data packet.

A sequence of null bits must precede the data packet to ensure proper framing of the data packet. 18 null bits <R17 - R0> are required to initialize the serial register after the initial application of power. Once initialized, only one null bit must precede each data packet.

The first ten bits of a data packet are write-only and consist of one synchronization bit <S>, an unused bit <A6>, three register address bits <A5-A3>, three preamp select bits <A2-A0>, one read/write bit <RN/W>, and one turnaround bit <T>. The next nine bits consist of 8 data bits <D7-D0> to be written-to or read-from a register and a postamble bit <P> (signifying the end of a data packet).

A data transfer is initiated upon the assertion of the serial clock (SCLK). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 19 cycles; on the 19th rising edge, the data will be written to the addressed register. During a read sequence, SDIO will become active on the falling edge of the 11th cycle. At this time <D7> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. The presentation of the postamble bit in the 19th falling edge signifies the end of the data transfer. The serial interface will only be fully powered between the synchronization and postamble bits.

The finite state machine in the preamp serial interface block must unconditionally complete a transfer sequence by ending in a state where the preamp loads the SDIO line by less than ±160µA (TS). The power-on-reset condition for SDIO is tristate/input mode.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 172 and 173 for a bit description. See Table 176 and Figure 119 for serial interface timing information.

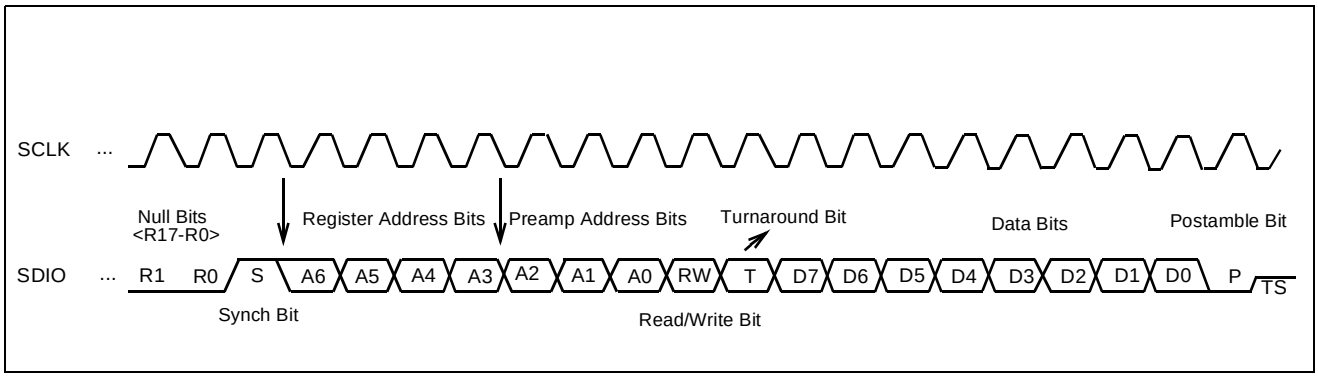


Figure 118 Serial Interface Protocol

Fault Detection

A fault condition is triggered by any of the following serial interface conditions:

28) Address fault - If address bits <A5-A3> select an invalid address or when preamp select bits <A2-A0> ≠ 000, the FLT pin is set and further write or read operations cannot be performed until the serial interface is reset.

29) No end of packet bit - If the 19th falling edge of SCLK is not a low signal, the FLT pin is set.

All serial interface faults are cleared by toggling the R/WN pin from low to high.

Table 172Serial Interface Bit Description -- Address Bits

Function	Register	Register Address Bits				Preamp Address Bits			RN/W bit
		<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>	
Head Select	0	1	0	0	0	0	0	0	1/0 [2]
Control	1	1	0	0	1				1/0 [2]
Write Current DAC	2	1	0	1	0				1/0 [2]
MR Bias Current DAC	3	1	0	1	1				1/0 [2]
Servo	4	1	1	0	0				1/0 [2]
Vendor ID	5 (read only)	1	1	0	1				0 [2]

1. Reserved
2. RN/W bit: Read = 0, Write = 1

Table 173Serial Interface Bit Description -- Data Bits

Function	Register	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Head Select	0	1	1	1	1	1	HS2	HS1	HS0
Control	1	1	1	BHVOE	1	WSER	BIASOVR	IDLEOVR	FAST
Write Current DAC / Gain	2	1	1	1	IW4	IW3	IW2	IW1	IW0
MR Bias Current DAC	3	1	1	GAIN	IMR4	IMR3	IMR2	IMR1	IMR0
Servo [2]	4	1	1	1	1	1	1	LC1	LC0
Vendor ID	5 (read only)	1	1	CHNL	REV2	REV1	REV0	VEN1	VEN0

1. Reserved
2. See Table 175 for a description of these bits.

Table 174Power-on Reset Register Values

Function	Register	Power-on Reset Value <D7-D0>
Head Select	0	<0000 0000>
Control	1	<0000 0010>
Write Current DAC	2	<0000 0000>
MR Bias Current DAC	3	<0000 0000>
Servo	4	<0000 0000>
Vendor ID	5	<0000 0101>

Table 175Servo Mode Register Selects

LC0 4:<D0>	LC1 4:<D1>	HEADS
0	0	0, 4
0	1	1, 5
1	0	2, 6
1	1	3, 7

Table 176Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) Rate				40	MHz
SCLK cycle time	T_c	20			ns
SCLK high time	T_{ckh}	8			ns
SCLK low time	T_{ckl}	8			ns
SCLK risetime (10 - 90%)		0.8		5	ns
SDIO setup time, write	T_s	6			ns
SDIO delay time, read		8			ns
SDIO hold time, write	T_h	1			ns
SDIO hold time, read		3			ns
SDIO risetime (10 - 90%)		0.8		7	ns
Time between I/O operations		25			ns

Note: SerEna assertion level is high.

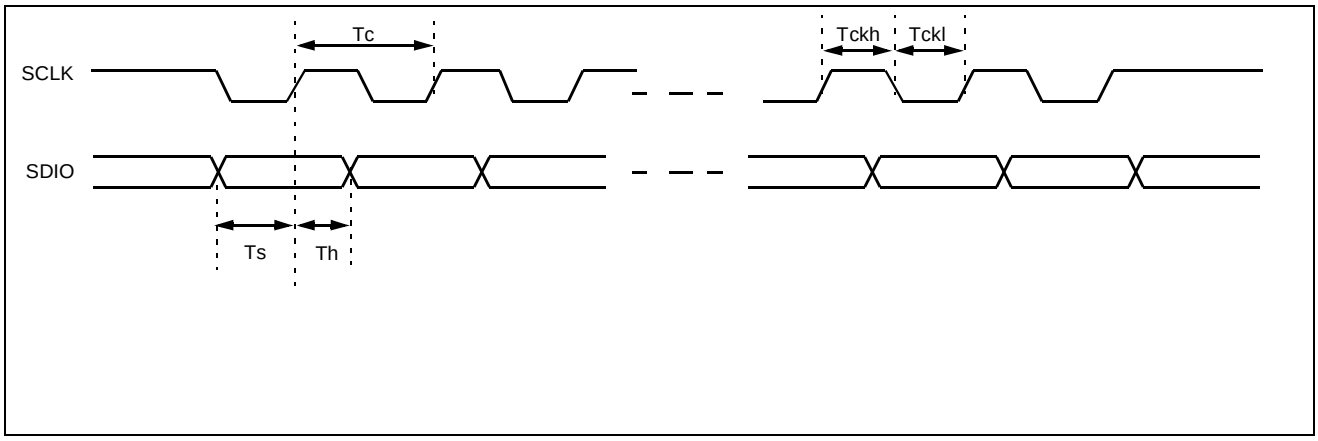


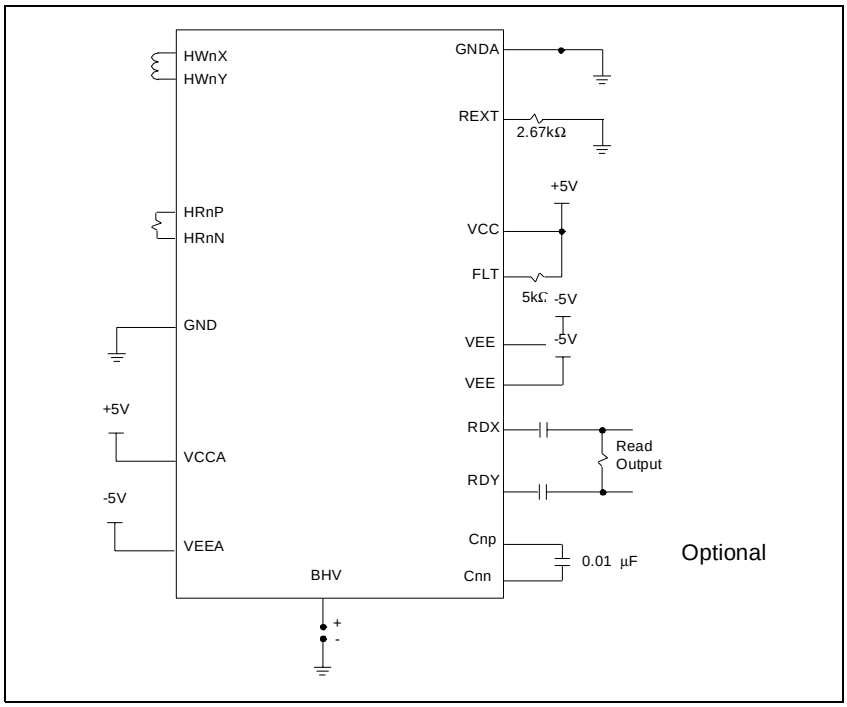
Figure 119 Serial Interface Timing

PIN_FUNCTION LIST AND DESCRIPTION

Symbol	*Input/ Output* [1]	*Description*
BHV	O	Buffered MR Head Voltage output.
BIAS	I [2]	Bias Enable: A TTL high level enables MR bias current to the selected head in both read and write modes. Pin defaults low (bias disabled). Note that the BIASOVR bit (1:<D2>) also forces bias current.
CSN	I [2]	Chip Select: A TTL high level initiates Idle mode. A TTL low level enables operation. If left disconnected, the input defaults to a high state. Note that the IDLEOVR bit (1:<D1>) also forces Idle mode.
FLT	O [2]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
GND	[2]	Ground
GNDA	[2]	Analog Ground
HR0P-HR7P	I	MR head connections, positive end.
HR0N-HR7N	I	MR head connections, negative end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end
REXT		Reference Voltage pin for both MR bias current and write current.
RDP, RDN	O[2]	Read Data: Differential read signal outputs.
R/WN	I [2]	Read/Write: A TTL low level enables write mode. Pin defaults high (read).
SCLK	I [2]	Serial Clock: Serial port clock; see Figure 119.
SDIO	I/O [2]	Serial Data: Serial port data; see Figure 119.
UCSN	I	Upper Chip Select: A TTL low level designates preamp as the “upper” preamp. A TTL high level designates preamp as the “lower” preamp. Pin defaults high (lower preamp designation).
VCC	[2]	+5.0V supply
VCCA	[2]	Analog +5.0V supply
VEE	[2]	-5.0V supply
VEEA	[2]	Analog -5.0V supply
WDX, WDY	I [2]	Differential Pseudo-ECL write data inputs.

1. I = Input pin, O = Output pin
2. When more than one device is used, these signals can be wire-OR’ed together.

TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors and the R_{EXT} resistor as close to the pins/pads as possible.
- Optional
  An optional additional supply noise bypass capacitor may be incorporated at the Cnp/Cnn pins/pads.
  Minimizing parasitics at the Cnn/Cnp node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5 mA, I_W = 50 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Power Supply Current	I_{CC}	Read Mode		110	TBD	mA
		Write Mode		100	TBD	
		Write Mode, Reader Biased		150	TBD	
		Idle Mode		20	TBD	
		Servo Bank Write		TBD	TBD	
V_{EE} Power Supply Current	I_{EE}	Read Mode		40	TBD	mA
		Write Mode		70	TBD	
		Write Mode, Reader Biased		88	TBD	
		Idle Mode		2	TBD	
		Servo Bank Write		TBD	TBD	
Power Supply Dissipation	P_d	Read Mode		750	TBD	mW
		Write Mode		850	TBD	
		Write Mode, Reader Biased		1215	TBD	
		Idle Mode		115	TBD	
Input High Voltage	V_{IH}	PECL	1.8		VCC-0.7	V
		TTL	2.0		VCC+0.3	
Input Low Voltage	V_{IL}	PECL	1.4		V_{IH}-0.4	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH}=2.7V			80	
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL}=0.4V	-160			
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400			mV_{ppd}
Output High current	I_{OH}	FLT: V_{OH}=5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL}=4mA			0.6	V
VCC Fault Threshold	V_{DTH}		3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-4.25	-4.0	-3.75	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 5 mA, I_W = 50 mA, R_{MR} = 50 Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}	R_{EXT} = 2.67kΩ	2		8	mA
MR Head Current Tolerance	I_{MR}	2 < I_{MR} < 4, R_{EXT} = 2.67kΩ	-7		+7	%
		4 ≤ I_{MR} < 8, R_{EXT} = 2.67kΩ	-5		+5	%
Unselected MR Head Current					15	µA
REXT Pin Voltage	V_{SET}	R_{EXT} = 2.67kΩ		2.0		V
Differential Voltage Gain	A_V	VIN = 1mVpp @ 10MHz, RL(RDP, RDN) = 1kΩ, Gain Bit=0	180	220	260	V/V
		Gain Bit=1	**TBD**	150	**TBD**	V/V
Passband Upper Frequency Limit	f_{HR}	Normal mode -1dB	135	TBD		MHz
		-3dB	200	230		
Passband Lower -3dB Frequency Limit	f_{LR}		**TBD**	1.0	**TBD**	MHz
		Fast Bit = 1		2.0		
Input Noise Voltage	e_n	0.9 MHz < f < 5 MHz		0.5	1.0	nV/√Hz
		5 MHz < f < 135 MHz		0.55	0.65	
Input Noise Bias Current	i_n	2 MHz < f < 135 MHz		10		pA/√Hz
Differential Input Capacitance	C_{IN}	Normal Mode		2	4	pF
Differential Input Resistance	R_{IN}	Normal Mode		340		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz	3			mV_{pp}
Total Harmonic Distortion	THD				2	%
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, 1 MHz < f < 135 MHz	40			dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, 2 MHz < f < 135 MHz	40			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 2 MHz < f < 135 MHz	30			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	VCC - 3.2	VCC -2.9	VCC -2.6	V
Common Mode Output Voltage Difference	ΔV_{OCM}	Read Mode to Write Mode	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		50		Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	4			mA

READ CHARACTERISTICS

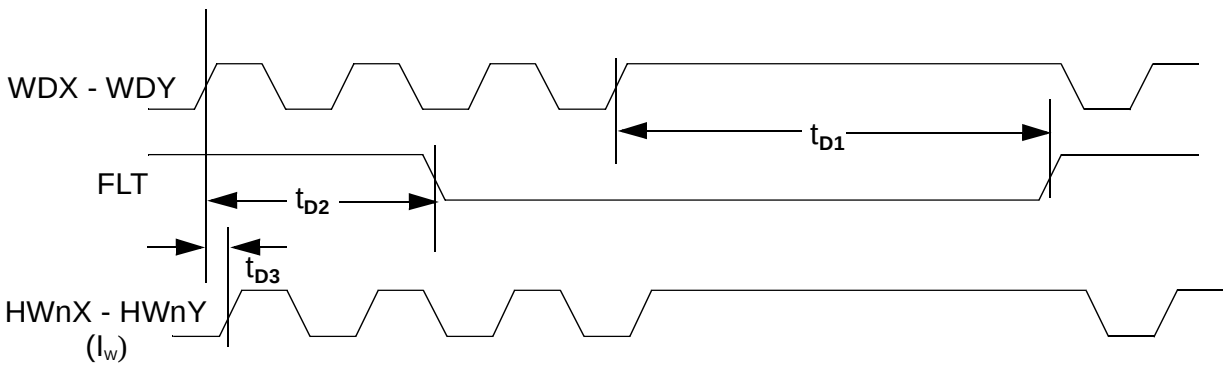
Recommended operating conditions apply unless otherwise specified: I_{MR} = 5 mA, I_W = 50 mA, R_{MR} = 50 Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK}=10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK}=300pF, R_{DISK}=10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}		-400		400	mV
MR Head Potential, Unselected Head	V_{MR}		-1	-.8		V
Buffered Head Voltage Gain	A_{BHV}		4.9	5	5.1	V/V
BHV input referred V_{OS}	Vis_{BHV}		-4		+4	mV
BHV output referred V_{OS}	Vos_{BHV}		1.96	2.0	2.04	V
I_{MR}*R_{MR}			100		600	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 50 mA, L_H = 100nH, R_H = 10Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REXT Pin Voltage	V_{SET}	R_{EXT}=2.67kΩ		2.0		V
Write Current Range	I_W	R_{EXT}=2.67kΩ	20		60	mA
Write Current Tolerance	ΔI_W	20 < I_W < 60 mA	-8		+8	%
Write Current Tolerance, Servo Mode	ΔI_S	20 < I_S < 60 mA	-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head		6		V_{pk}
Differential Output Capacitance	C_O				10	pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}		35			MHz
Input Termination Resistance				300		Ω



In voltage mode:
When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode:
When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 120 Write Mode Timing Diagram

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: f_{DATA} = 5MHz, L_H = 100nH, R_H = 10Ω, I_W = 50mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write current			100	ns
R/WN to Read Mode	t_{WR}	To 90% of envelope; ±20mV of final DC value		250	500	ns
PWRUP to Read Mode (SCLK 19th rising edge)	t_{CS}	To 90% of envelope; ±20mV of final DC value			10	µs
HS0-2 to Any Head (SCLK 19th rising edge) Read Mode	t_{HS}	To 90% of envelope; ±20mV of final DC value IMR change			3	µs
HS0-2 to Any Head (SCLK 19th rising edge) Servo Write Mode	t_{SHS}	To 90% of write current; Constant I_{MR} ±20mV of final DC value			1	µs
SCLK (19th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0			0.1	ns
Rise/Fall Time	t_r / t_f	20% - 80%, 70nH			1	ns
Read to Bank Servo Write					250	ns

1. See Figure 120 for the write mode timing diagram on page 419.

VM6205 PACKAGING

8-Channel Die

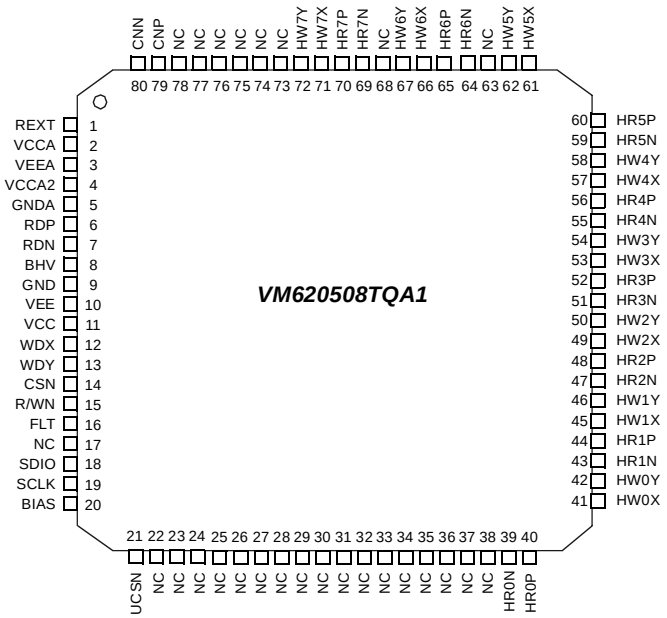
Specific Characteristics

Die size: **TBD** x **TBD** Mils

Wire Bond Coordinates for the VM6205 (in Mils)

Pin Name	*X Axis*	*Y Axis*	*Pad Size*
BHV	**TBD**	**TBD**	4x4
BIAS	**TBD**	**TBD**	4x4
CnN	**TBD**	**TBD**	4x4
CnP	**TBD**	**TBD**	4x4
CSN	**TBD**	**TBD**	4x4
FLT	**TBD**	**TBD**	4x4
GND	**TBD**	**TBD**	4x10
GNDA	**TBD**	**TBD**	4x10
HR0N	**TBD**	**TBD**	4x4
HR0P	**TBD**	**TBD**	4x4
HR1N	**TBD**	**TBD**	4x4
HR1P	**TBD**	**TBD**	4x4
HR2N	**TBD**	**TBD**	4x4
HR2P	**TBD**	**TBD**	4x4
HR3N	**TBD**	**TBD**	4x4
HR3P	**TBD**	**TBD**	4x4
HR4N	**TBD**	**TBD**	4x4
HR4P	**TBD**	**TBD**	4x4
HR5N	**TBD**	**TBD**	4x4
HR5P	**TBD**	**TBD**	4x4
HR6N	**TBD**	**TBD**	4x4
HR6P	**TBD**	**TBD**	4x4
HR7N	**TBD**	**TBD**	4x4
HR7P	**TBD**	**TBD**	4x4
HW0X	**TBD**	**TBD**	4x4
HW0Y	**TBD**	**TBD**	4x4
HW1X	**TBD**	**TBD**	4x4
HW1Y	**TBD**	**TBD**	4x4
HW2X	**TBD**	**TBD**	4x4
HW2Y	**TBD**	**TBD**	4x4
HW3X	**TBD**	**TBD**	4x4
HW3Y	**TBD**	**TBD**	4x4
HW4X	**TBD**	**TBD**	4x4
HW4Y	**TBD**	**TBD**	4x4
HW5X	**TBD**	**TBD**	4x4
HW5Y	**TBD**	**TBD**	4x4
HW6X	**TBD**	**TBD**	4x4
HW6Y	**TBD**	**TBD**	4x4
HW7X	**TBD**	**TBD**	4x4
HW7Y	**TBD**	**TBD**	4x4
RDN	**TBD**	**TBD**	4x4
RDP	**TBD**	**TBD**	4x4
REXT	**TBD**	**TBD**	4x4
R/WN	**TBD**	**TBD**	4x4
SCLK	**TBD**	**TBD**	4x4
SDIO	**TBD**	**TBD**	4x4
UCSN	**TBD**	**TBD**	4x4
VCC	**TBD**	**TBD**	4x10
VCCA	**TBD**	**TBD**	4x10
VCCA2	**TBD**	**TBD**	4x4
VEE	**TBD**	**TBD**	4x10
VEEA	**TBD**	**TBD**	4x10
WDX	**TBD**	**TBD**	4x4
WDY	**TBD**	**TBD**	4x4

8-Channel Pinout



80-pin TQFP

VTC Inc.
Value The Customer™

VM6214 Series

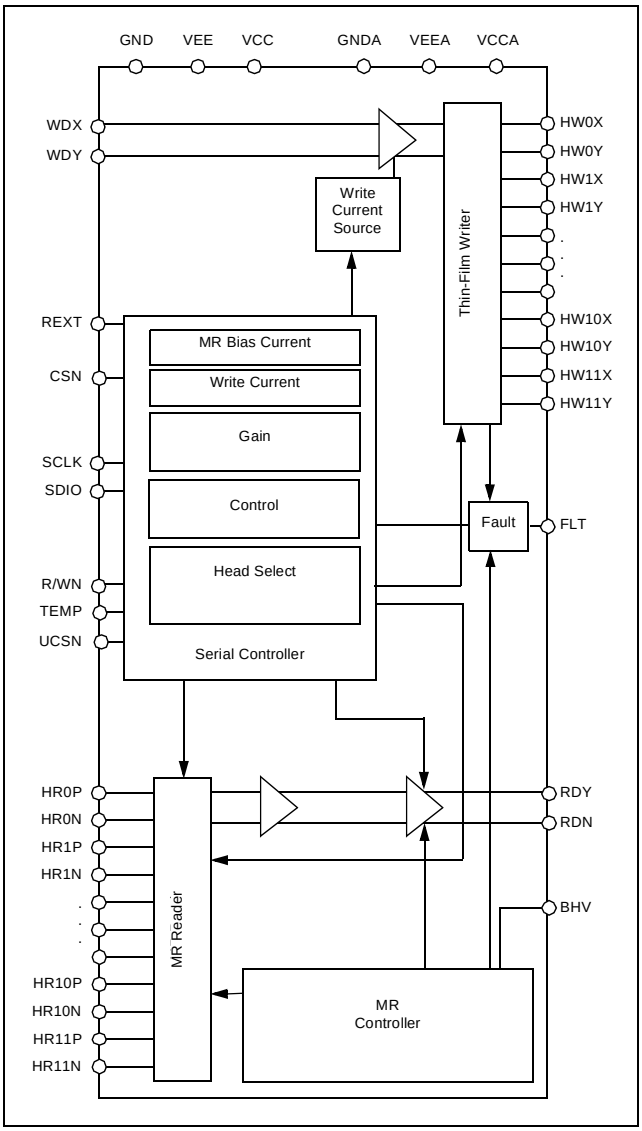
PROGRAMMABLE, 5-VOLT, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER with SERVO WRITE

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 350 Mbits/sec
  - Requires Only One External Component (R_{ext})
  - Designed for Use With Four-Terminal MR Heads
  - 2-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Gain and Head Selection)
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 12 Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC, 2 - 9 mA Range
  - Programmable Read Voltage Gain
    (220 V/V or 300 V/V Typical)
  - Buffered Head Voltage Output
  - Input Noise = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 6 pF Typical
  - Head Inductance Range = 10 nH - 150 nH
  - Bandwidths in Excess of 310 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 60 mA Range
  - Rise Time < 1.0 ns Typical
    (20-80%, L_{total} = 100 nH, I_W = 40 mA)

BLOCK DIAGRAM



DESCRIPTION

The VM6214 is an integrated bipolar programmable read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6214 contains a thin-film head writer, an MR reader, and associated fault circuitry.

Compensation capacitors previously required as external components have been integrated into the VM6214. As a result, only one external component (Rext) is required. This advanced design greatly simplifies flex layouts.

Programmability of the VM6214 is achieved through a 2-line serial interface. Programmable parameters include MR bias current, write current, gain and head selection.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, the IDLEOVR bit (register 1, bit <D1>) initializes to 1 (idle mode) and an internal pull-up resistor is connected to the R/WN line to prevent accidental writing due to an open line.

The VM6214 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM6214 is available in die form for chip-on-flex applications or a 80-pin TQFP. Please consult VTC for details.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +7V

Read Bias Current, I_{MR} 18mA
Write Current, I_W 90mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -5V ± 10%
- V_{CC} ..... +5V ± 10%

Write Current, I_W ..... 20 - 60 mA
Write Head Inductance, L_W ..... 10 - 100 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 2 - 9 mA
Read Head Inductance, L_{MR} ..... 10 - 150 nH
Read Head Resistance, R_{MR} ..... 25 - 45 Ω (Imr*Rmr<600mV)
Junction Temperature, T_J ..... 0°C to 125°C

SERIAL INTERFACE CONTROLLER

The VM6214 uses a 2-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude.

See “SERIAL INTERFACE” on page 427 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

The VM6214 was designed for a single or multiple preamp configuration. All control lines may be shared (including the two serial lines SCLK and SDIO).

Pin UCSN determines the preamplifier’s upper/lower status in a dual preamp configuration. Pin UCSN floats high if left open, and the preamp assumes the “lower preamp” designation. If pin UCSN is tied to ground, the preamp will assume the “upper preamp” designation.

The UPCHP bit (0:<D4>) is used to select the upper or lower preamp (in a dual preamp configuration).

The PWREN bit (1:<D4>) is used to place the inactive (unselected) preamp in either Standby or Idle mode.

The DUALW bit (1:<D3>) is used to invoke a special mode where both preamps respond to the lower preamp address field. This Dual Write mode can reduce servo write time in a dual preamp configuration.

See Tables 170 and 171 for Mode Select information.

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the mode control circuitry and the serial registers (the contents of which remain latched).

Idle mode is selected by taking the CSN pin high.

Note: Setting the IDLEOVR bit high (1:<D1>) forces Idle mode, regardless of the state of the CSN pin.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM6214 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{(k_{IMR} \times 0.602) + 5.34}{R_{ext}} \times \left(\frac{385}{R_{MR} + 340}\right) \qquad \textit{(eq. 87)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

MR head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±300mV of ground and unselected heads are held at approximately -800mV.

Read Gain

The gain is nominally 220 V/V with a head resistance of 45Ω. The formula that describes the actual gain is shown below:

$$A_V = \frac{385}{340 + R_{MR}} \times 220 \qquad \textit{(eq. 88)}$$

Note: Setting the GAIN bit high (3:<D5>) selects a nominal gain of 300 V/V.

MR Bias Enable

Setting the BIASOVR bit (1:D2>) high activates bias current.

MR Bias DAC

The 5 bits in register 3 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

BHV (Buffered Head Voltage)

Setting the BHVOE bit high (1:<D5>) enables the output of the ($I_{MR} \times R_{MR}$)×5 product of the selected head at the BHV pin. This output is single-ended with respect to ground. When bit BHVOE is reset, the output pin BHV enters a low-impedance (low-Z) state to minimize noise coupling.

Note: The reader outputs are disabled.

Fast Read Mode

Setting the FAST bit high (1:<D0>) increases the high-pass corner frequency of the amplifier’s bandpass from a value of 300 kHz to 2.5 MHz nominal.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
- Invalid head select code
- Device in write mode

Read Inactive Mode

Selecting an invalid head (setting both the HS3 and HS2 bits high, 0:<D3-D2>) invokes a “Read Inactive” mode where bias current is diverted internally to a dummy head.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

The chip drives the RDP/RDN outputs to normal levels and its power consumption is unaffected.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the write current magnitude:

$$I_W = \left[\frac{(k_{IW} x 3.44) + 53.34}{R_{ext}}\right] \quad \textit{(eq. 89)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 119 for the timing diagram.

Write Current DAC

The 5 bits in register 2 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Setting the BIASOVR bit high (1:<D2>) in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Dual Write Mode

Setting the DUALW bit high (1:<D3>) initiates a special Dual Write mode.

Dual Write mode allows the writing of one channel in each of two preamps in a dual preamp configuration. When set, both preamps respond to the lower preamp address field.

This mode can reduce servo write time when there are two preamps in a single head-disk assembly.

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open write head
- No write current

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Invalid head select code
- Low power supply voltage
- Device in read or idle mode
- Head shorted to ground

Note: Invalid head and head shorted faults are latched and can only be cleared by toggling either the R/WN pin or the CSN pin.

Standby Mode (Inactive Preamp Only)

This special mode allows for power management of the inactive preamp in dual preamp configurations.

Setting the PWREN bit high (1:<D4>) places the inactive preamp in a reduced power consumption Standby mode. Bias current is diverted internally, outputs are not driven, and the serial register remains active. This mode facilitates a rapid recovery when the inactive preamp is selected.

Idle Mode (Inactive Preamp Only)

Setting the PWREN bit low (1:<D4>) places the inactive preamp in a minimal power consumption Idle mode.

Temperature

The die temperature can be determined by monitoring the voltage at the TEMP pin. This pin is nominally two diode drops above ground. The voltage must be calibrated at known temperatures to determine the voltage change over the temperature range.

MODE SELECTION

- The UCSN pin identifies a preamp as ‘lower” when high and as ‘upper’ when low.
- The UPCHP bit (0:<D4>) selects the upper preamp when high (in a dual preamp configuration) and the lower preamp when low.

Table 170Mode Select (for the Selected Preamp) (UCSN=1, UPCHP=0) or (UCSN=0, UPCHP=1)

CSN	*R/WN*	*BIASOVR 1:<D2>*	*HS3 0:<D3>*	*HS2 0:<D2>*	*MODE*
1	X	X	X	X	Idle
0	1	1	valid head		Read
0	1	0	X	X	Read Inactive (bias to dummy head)
0	X	X	1	1	
0	0	0	valid head		Write
0	0	0	1	1	Write (Write Current Disabled)
0	0	1	valid head		Write with Read Bias Enabled
0	0	1	1	1	Write with Read Bias Enabled (Write Current Disabled)

- The IDLEOVR bit (1:<D1>) forces Idle mode when set high.

Note: Invalid mode selection will select Idle mode.

Table 171Mode Select (for the Unselected Preamp) (UCSN=1, UPCHP=1) or (UCSN=0, UPCHP=0)

PWREN 1:<D4>	*MODE*
0	Idle
1	Standby

- The PWREN bit (1:<D4>) allows for power management of the inactive (unselected) preamp in a dual preamp configuration. When high, the inactive preamp is placed in Standby mode (with reduced power consumption). When low, the inactive preamp is placed in Idle mode (with minimal power consumption).

Note: If the UCSN lines are tied together, taking the CSN pin high places both preamps (in a dual preamp configuration) in the Idle mode.

Note: Setting the DUALW bit high (1:<D3>) initiates a special Dual Write mode that allows the writing of one channel in each of two preamps (both selected and unselected) in a dual preamp configuration. See “Dual Write Mode” on page 425.

Table 172Head Select

HS3 0:<D3>	*HS2 0:<D2>*	*HS1 0:<D1>*	*HS0 0:<D0>*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	X	X	invalid head [1]

1. In Write mode, an invalid head select will disable the writer, dump the head selection current to the positive supply and register a fault.
In Read mode, an invalid head select will force “Read Inactive” mode, divert the read current to a dummy head and register a fault.

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SERIAL INTERFACE

The serial interface has one input line, SCLK (serial clock), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. When the serial register is powered down only the output D-latches and the reference generators remain active. 19 bits constitutes a complete data packet.

A sequence of null bits must precede the data packet to ensure proper framing of the data packet. 18 null bits <R17 - R0> are required to initialize the serial register after the initial application of power. Once initialized, only one null bit must precede each data packet.

The first ten bits of a data packet are write-only and consist of one synchronization bit <S>, an unused bit <A6>, three register address bits <A5-A3>, three preamp select bits <A2-A0>, one read/write bit <RN/W>, and one turnaround bit <T>. The next nine bits consist of 8 data bits <D7-D0> to be written-to or read-from a register and a postamble bit <P> (signifying the end of a data packet).

A data transfer is initiated upon the assertion of the serial clock (SCLK). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 19 cycles; on the 19th rising edge, the data will be written to the addressed register. During a read sequence, SDIO will become active on the falling edge of the 11th cycle. At this time <D7> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. The presentation of the postamble bit in the 19th falling edge signifies the end of the data transfer. The serial interface will only be fully powered between the synchronization and postamble bits.

The finite state machine in the preamp serial interface block must unconditionally complete a transfer sequence by ending in a state where the preamp loads the SDIO line by less than ±160µA (TS). The power-on-reset condition for SDIO is tristate/input mode.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 173 and 174 for a bit description. See Table 176 and Figure 118 for serial interface timing information.

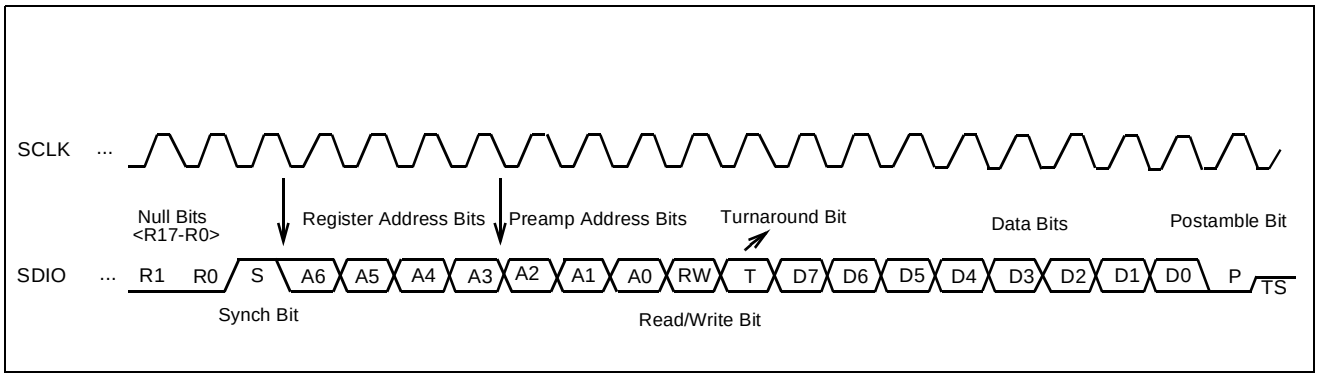

Figure 117 Serial Interface Protocol

Table 173Serial Interface Bit Description -- Address Bits

Function	Register #	Register Address Bits				Preamp Address Bits			RN/W bit
		<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>	<W>
Head Select	0	1	0	0	0	0	0	0	1/0 [2]
Control	1	1	0	0	1				1/0 [2]
Write Current DAC	2	1	0	1	0				1/0 [2]
MR Bias Current DAC	3	1	0	1	1				1/0 [2]
Vendor ID	4 (read only)	1	1	0	0				0 [2]

1. Reserved
2. RN/W Address bit: Read = 0, Write = 1

Table 174Serial Interface Bit Description -- Data Bits

Function	Register #	Data Bits							
		<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Head Select	0	1	1	1	UPCHP	HS3	HS2	HS1	HS0
Control	1	1	1	BHVOE	PWREN	DUALW	BIASOVR	IDLEOVR	FAST
Write Current DAC	2	1	1	1	IW4	IW3	IW2	IW1	IW0
MR Bias Current DAC / Gain	3	1	1	GAIN	IMR4	IMR3	IMR2	IMR1	IMR0
Vendor ID	4 (read only)	0	0	1	1	0	0	0	1

1. Reserved

Table 175Power-on Reset Register Values

Function	Register Number	Power-on Reset Value <D7-D0>
Head Select	0	<0001 1111>
Control	1	<0000 0010>
Write Current DAC	2	<0000 0000>
MR Bias Current DAC	3	<0000 0000>
Vendor ID	4	<0011 0001>

Table 176Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) Rate				40	MHz
SCLK cycle time	T_c	20			ns
SCLK high time	T_{ckh}	8			ns
SCLK low time	T_{ckl}	8			ns
SCLK risetime (10 - 90%)		0.8		5	ns
SDIO setup time, write	T_s	6			ns
SDIO delay time, read		8			ns
SDIO hold time, write	T_h	1			ns
SDIO hold time, read		3			ns
SDIO risetime (10 - 90%)		0.8		7	ns
Time between I/O operations		25			ns

Note: SerEna assertion level is high.

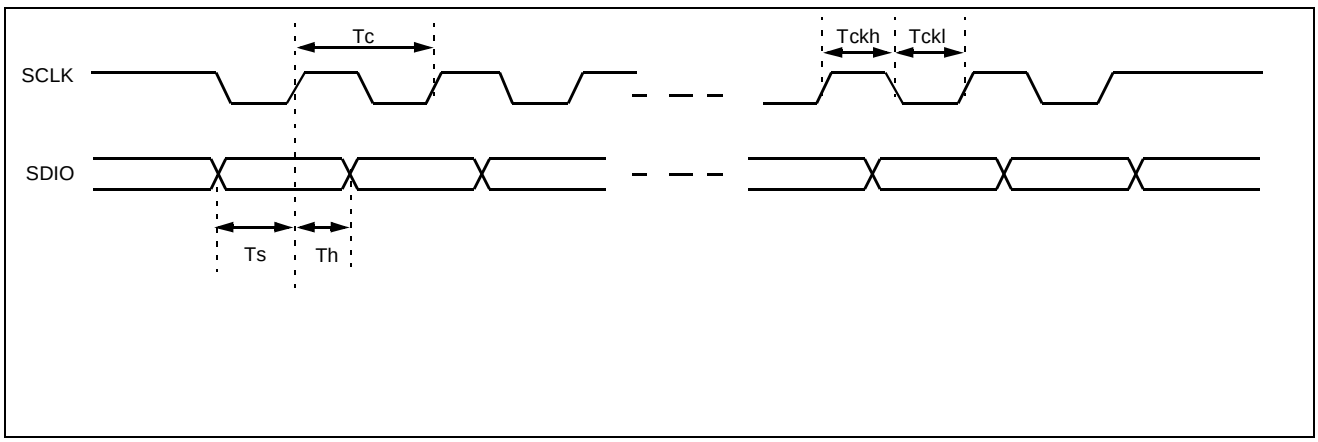

Figure 118 Serial Interface Timing

PIN_FUNCTION LIST AND DESCRIPTION

Symbol	*Input/ Output* [1]	*Description*
BHV	O	Buffered MR Head Voltage output.
CSN	I [2]	Chip Select: A TTL high level initiates Idle mode. A TTL low level enables operation. If left disconnected, the input defaults to a high state. Note that the IDLEOVR bit (1:<D1>) also forces Idle mode.
FLT	O [2]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
GND	[2]	Ground
GNDA	[2]	Analog Ground
HR0P-HR11P	I	MR head connections, positive end.
HR0N-HR11N	I	MR head connections, negative end.
HW0X-HW11X	O	Thin-Film write head connections, positive end.
HW0Y-HW11Y	O	Thin-Film write head connections, negative end
REXT		Reference Voltage pin for both MR bias current and write current.
RDP, RDN	O [2]	Read Data: Differential read signal outputs.
R/WN	I [2]	Read/Write: A TTL low level enables write mode. Pin defaults high (read).
SCLK	I [2]	Serial Clock: Serial port clock; see Figure 171.
SDIO	I/O [2]	Serial Data: Serial port data; see Figure 171.
TEMP	I [2]	Temperature: Two diode drop voltage to measure die temperature.
UCSN	I	Upper Chip Select: A TTL low level designates preamp as the “upper” preamp. A TTL high level designates preamp as the “lower” preamp. Pin defaults high (lower preamp designation).
VCC	[2]	+5.0V supply
VCCA	[2]	Analog +5.0V supply
VEE	[2]	-5.0V supply
VEEA	[2]	Analog -5.0V supply
WDX, WDY	I [2]	Differential Pseudo-ECL write data inputs.

1. I = Input pin, O = Output pin
2. When more than one device is used, these signals can be wire-OR’ed together.

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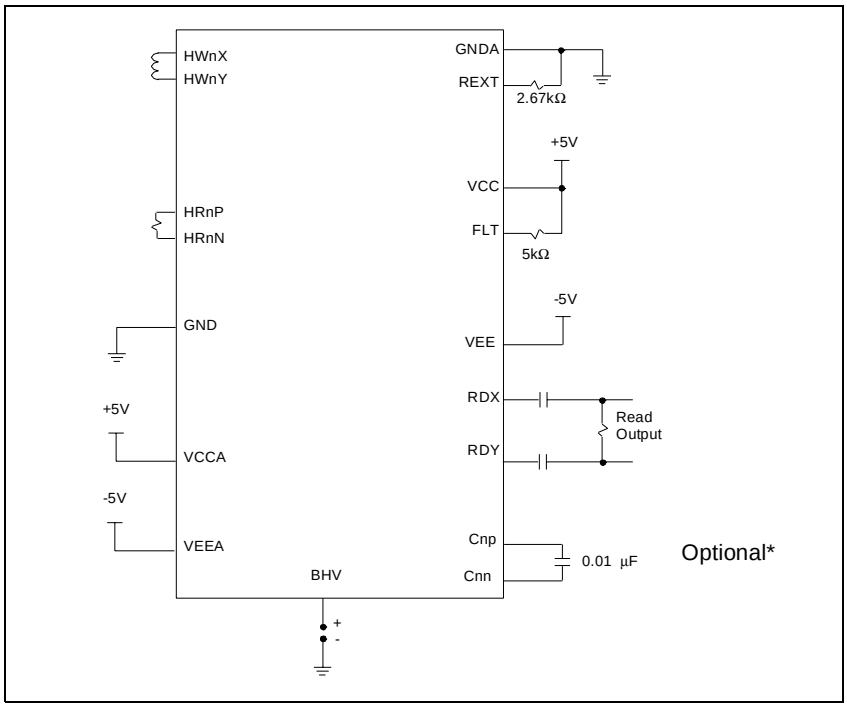
TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations. The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors and the R_{EXT} resistor as close to the pins/pads as possible.
- Optional*
  An optional additional supply noise bypass capacitor may be incorporated at the Cnp/Cnn pins/pads.
  Minimizing parasitics at the Cnn/Cnp node is vital. Place a high quality (low resistance, low inductance) capacitor as close to the die as possible.

STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 6 mA, I_W = 40 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Power Supply Current	I_{CC}	Read Mode		115	TBD	mA
		Write Mode		105	TBD	
		Write Mode, Reader Biased		155	TBD	
		Idle Mode		20	TBD	
V_{EE} Power Supply Current	I_{EE}	Read Mode		40	TBD	mA
		Write Mode		70	TBD	
		Write Mode, Reader Biased		88	TBD	
		Idle Mode		2	TBD	
Power Supply Dissipation	P_d	Read Mode		775	TBD	mW
		Write Mode		875	TBD	
		Write Mode, Reader Biased		1200	TBD	
		Idle Mode		110	TBD	
Input High Voltage	V_{IH}	PECL	1.8		VCC-0.7	V
		TTL	2.0		VCC+0.3	
Input Low Voltage	V_{IL}	PECL	1.4		V_{IH}-0.4	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH}=2.7V			80	
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL}=0.4V	-160			
Output High current	I_{OH}	FLT: V_{OH}=5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL}=4mA			0.6	V
VCC Fault Threshold	V_{DTH}		3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.8	-3.55	-3.3	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 6mA, R_{EXT}=2.67kΩ, R_{MR} = 45Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}		2		9	mA
MR Head Current Tolerance	I_{MR}	2mA < I_{MR} ≤ 4mA	-7		+7	%
		4mA < I_{MR} < 9mA	-5		+5	
Unselected MR Head Current					15	µA
REXT Pin Voltage	V_{SET}			2.0		V
I_{REXT} to MR Bias Current Gain	A_{IMR}			5		mA/mA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 10MHz, RL(RDP, RDN) = 1kΩ, Gain Bit=0 Gain = 385/(340+R_{MR})*220	180	220	260	V/V
		Gain Bit=1 Gain = 385/(340+R_{MR})*300	245	300	355	V/V
Passband Upper Frequency Limit	f_{HR}	Normal mode -1dB	135			MHz
		-3dB	250	280		
Passband Lower -3dB Frequency Limit	f_{LR}	Normal mode	0.1	0.7	0.9	MHz
		Fast mode, Lower 3dB	1.5	2.5	3.5	MHz
Input Noise Voltage	e_n	1 MHz < f < 20 MHz		0.55	0.65	nV/√Hz
Input Noise Bias Current	i_n	1 MHz < f < 20 MHz		10	14	pA/√Hz
Differential Input Capacitance	C_{IN}	Normal Mode		3		pF
Differential Input Resistance	R_{IN}	Normal Mode	TBD	340		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz	3			mV_{pp}
Total Harmonic Distortion	THD				2	%
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, 1 MHz < f < 135 MHz	40			dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, 2 MHz < f < 135 MHz	40			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 2 MHz < f < 135 MHz	30			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	VCC - 3.2	VCC -2.9	VCC -2.6	V
Common Mode Output Voltage Difference	ΔV_{OCM}	Read Mode to Write Mode	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		25		Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	4			mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR} = 6mA, R_{EXT}=2.67kΩ, R_{MR} = 45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Potential, Selected Head	V_{MR}		-400		400	mV
MR Head Potential, Unselected Head	V_{MR}		-1	-.8		V
Buffered Head Voltage Gain	A_{BHV}		4.9	5	5.1	V/V
BHV input referred V_{OS}	Vos_{BHV}		-4		+4	mV
I_{MR}*R_{MR}			100		600	mV

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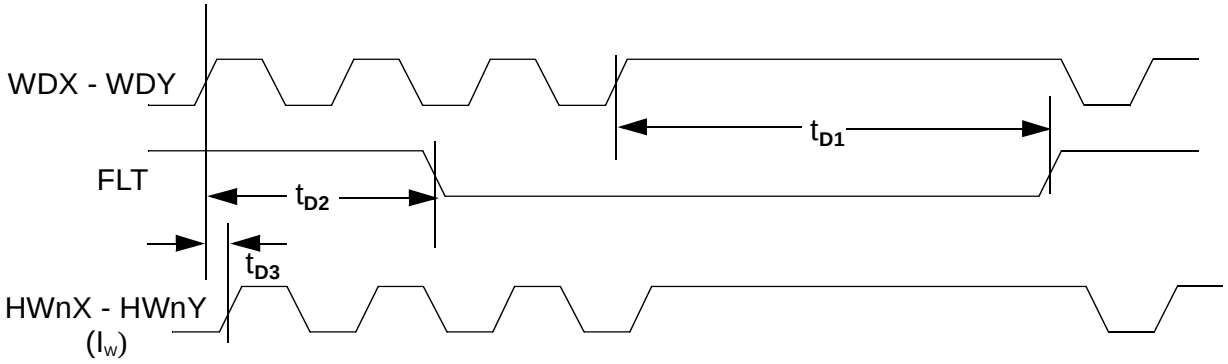
WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W = 40mA, L_H = 100nH, R_{EXT}=2.67kΩ, R_H = 10Ω, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REXT Pin Voltage	V_{SET}			2.0		V
Write Current Range	I_W		20		60	mA
Write Current Tolerance	ΔI_W	20 < I_W < 60 mA	-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head		6		V_{pk}
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400			mV_{ppd}
Unselected Head Transition Current	I_{UH}	I_W=30mA			100	μA_{pk}
Differential Output Capacitance	C_O				10	pF
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}		35			MHz
Input Termination Resistance				300		Ω



In voltage mode:
When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode:
When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 119 Write Mode Timing Diagram

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: f_{DATA} = 5MHz, L_H = 100nH, R_H = 10Ω, I_W = 40mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/WN to Write Mode	t_{RW}	To 90% of write current			100	ns
R/WN to Read Mode	t_{WR}	To 90% of envelope; ±20mV of final DC value		250	500	ns
PWRUP to Read Mode (SCLK 19th rising edge)	t_{CS}	To 90% of envelope; ±20mV of final DC value			10	µs
HS0-3 to Any Head (SCLK 19th rising edge) Read Mode	t_{HS}	To 90% of envelope; ±20mV of final DC value Constant IMR			1	µs
		To 90% of envelope; ±20mV of final DC value Min to Max IMR Change			3	µs
HS0-3 to Any Head (SCLK 19th rising edge) Servo Write Mode	t_{SHS}	To 90% of write current; Constant I_W			1	µs
SCLK (19th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0			0.1	ns
Rise/Fall Time	t_r / t_f	20% - 80%		0.950	1.2	ns

1. See Figure 119 for the write mode timing diagram.

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VM6214 PACKAGING

12-Channel Bump

Specific Characteristics

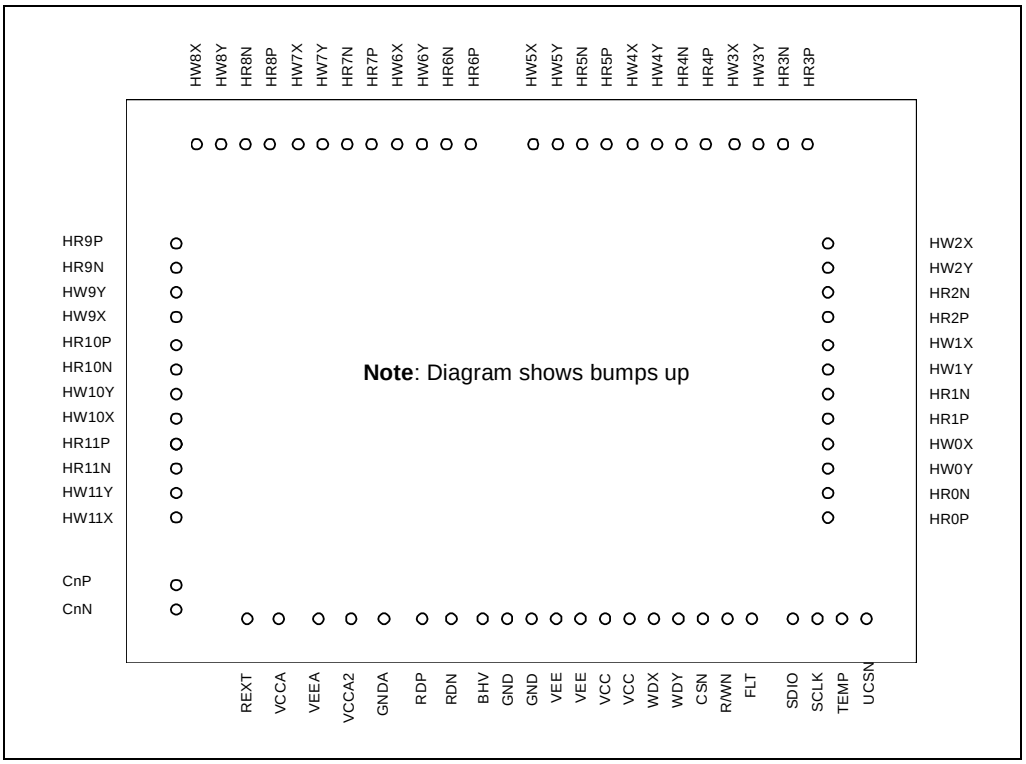
Die size: 220 x 157 Mils

Bump Coordinates for the VM6214 (in Mils)

Pin Name	*X Axis*	*Y Axis*
BHV	-5.394	-72.941
CnN	-90.697	-70.354
CnP	-90.697	-63.543
CSN	55.906	-72.941
FLT	69.528	-72.941
GND	1.417	-72.941
GND	8.228	-72.941
GNDA	-32.866	-72.941
HR0N	90.697	-37.949
HR0P	90.697	-44.760
HR10N	-90.697	-3.594
HR10P	-90.697	3.217
HR11N	-90.697	-31.110
HR11P	-90.697	-24.299
HR1N	90.697	-10.406
HR1P	90.697	-17.217
HR2N	90.697	17.878
HR2P	90.697	11.067
HR3N	78.209	59.122
HR3P	85.020	59.122
HR4N	49.917	59.122
HR4P	56.728	59.122
HR5N	22.303	59.122
HR5P	29.114	59.122
HR6N	-15.492	59.122
HR6P	-8.681	59.122
HR7N	-43.106	59.122
HR7P	-36.295	59.122
HR8N	-71.398	59.122
HR8P	-64.587	59.122
HR9N	-90.697	24.689
HR9P	-90.697	31.500
HW0X	90.697	-24.327
HW0Y	90.697	-31.138
HW10X	-90.697	-17.217
HW10Y	-90.697	-10.406
HW11X	-90.697	-44.732
HW11Y	-90.697	-37.921

Pin Name	*X Axis*	*Y Axis*
HW1X	90.697	3.217
HW1Y	90.697	-3.594
HW2X	90.697	31.500
HW2Y	90.697	24.689
HW3X	64.587	59.122
HW3Y	71.398	59.122
HW4X	36.295	59.122
HW4Y	43.106	59.122
HW5X	8.681	59.122
HW5Y	15.492	59.122
HW6X	-29.114	59.122
HW6Y	-22.303	59.122
HW7X	-56.728	59.122
HW7Y	-49.917	59.122
HW8X	-85.020	59.122
HW8Y	-78.209	59.122
HW9X	-90.697	11.067
HW9Y	-90.697	17.878
R/WN	62.717	-72.941
RDN	-14.118	-72.941
RDP	-22.209	-72.941
REXT	-70.941	-72.941
SCLK	87.772	-72.941
SDIO	80.961	-72.941
TEMP	94.583	-72.941
UCSN	101.406	-72.941
VCC	28.661	-72.941
VCC	35.472	-72.941
VCCA	-62.121	-72.941
VCCA2	-41.965	-72.941
VEE	15.039	-72.941
VEE	21.850	-72.941
VEEA	-51.079	-72.941
WDX	42.283	-72.941
WDY	49.094	-72.941

12-Channel Bump Diagram



VTC Inc.
Value The Customer™

VM623206

PROGRAMMABLE, ±5-VOLT, MAGNETO-RESISTIVE HEAD, READ/ WRITE PREAMPLIFIER with SERVO WRITE

990812 August 12, 1999

FEATURES

- *General*
  - Transfer Rates in Excess of 350 Mbits/sec
  - Requires Only One External Component (R_{ext})
  - Designed for Use With Four-Terminal MR Heads
  - 2-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Gain and Head Selection)
  - Die Temperature Monitor Capability
  - Operates from +5 and -5 Volt Power Supplies
  - Up to 6 Channels Available
  - Fault Detect Capability
- *High Performance Reader*
  - Current Bias / Voltage Sense Configuration
  - MR Bias Current 5-bit DAC, 3 - 10 mA Range
  - Programmable Read Voltage Gain
    (220 V/V or 300 V/V Typical)
  - Buffered Head Voltage Output
  - Input Noise = 0.55 nV/$\sqrt{Hz}$ Typical
  - Input Capacitance = 6 pF Typical
  - Head Inductance Range = 10 nH - 150 nH
  - Bandwidths in Excess of 310 MHz
- *High Speed Writer*
  - Write Current 5-bit DAC, 20 - 60 mA Range
  - Rise Time < 1.0 ns Typical
    (20-80%, L_{total} = 100 nH, I_W = 40 mA)

DESCRIPTION

The VM623206 is an integrated bipolar programmable read/ write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM623206 contains a thin-film head writer, an MR reader, and associated fault circuitry.

Compensation capacitors previously required as external components have been integrated into the VM623206. As a result, only one external component (Rext) is required. This advanced design greatly simplifies flex layouts.

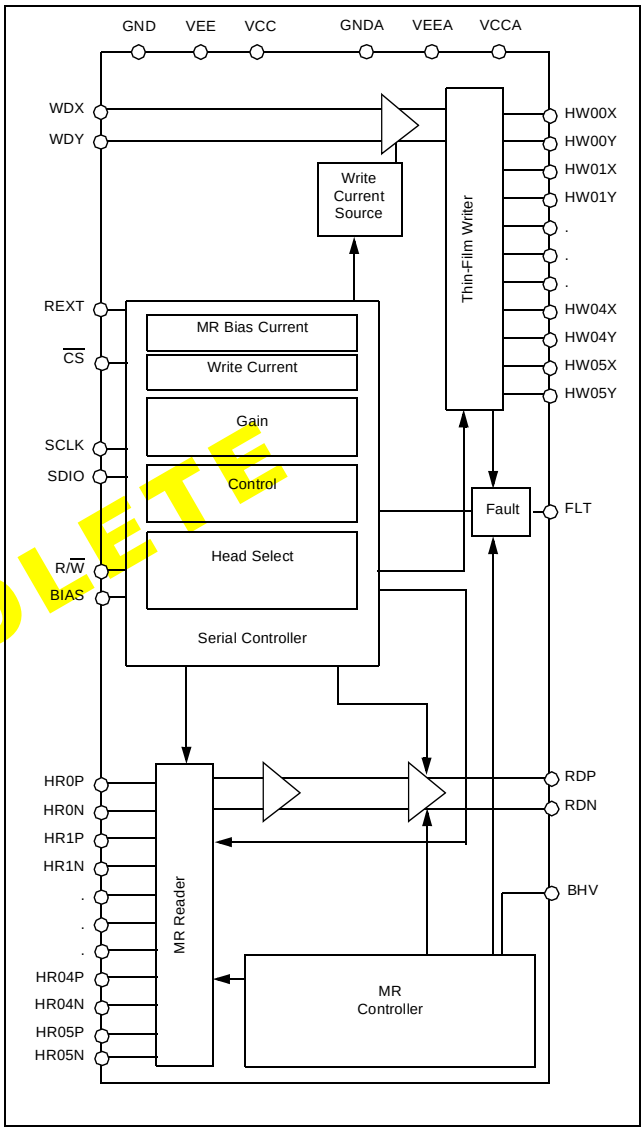
Programmability of the VM623206 is achieved through a 2-line serial interface. Programmable parameters include MR bias current, write current, gain and head selection.

Fault protection circuitry disables the write current generator upon critical fault detection. This protects the disk from potential data loss. For added data protection, the IDLEOVR bit (register 1, bit <D1>) initializes to 1 (idle mode) and an internal pull-up resistor is connected to the R/$\overline{W}$ line to prevent accidental writing due to an open line.

The VM623206 operates from +5V, -5V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters an idle mode which reduces the power dissipation.

The VM623206 is available in 48-pin TQFP package. Please consult VTC for details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -6V
- V_{CC} ..... -0.3V to +6V

Read Bias Current, I_{MR} 18mA
Write Current, I_W 90mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{EE} ..... -5V ± 10%
V_{CC} ..... +5V ± 10%
Write Current, I_W ..... 20 - 60 mA
Write Head Inductance, L_W ..... 10 - 100 nH
Write Head Resistance, R_W ..... 10 - 30 Ω
Read Bias Current, I_{MR} ..... 5 - 12 mA
Read Head Inductance, L_{MR} ..... 10 - 150 nH
Read Head Resistance, R_{MR} ..... 25 - 45 Ω (Imr*Rmr<600mV)
Junction Temperature, T_J ..... 0°C to 125°C

Serial Interface Controller

The VM623206 uses a 2-line read/write serial interface for control of most chip functions including head selection, MR bias current magnitude and write current magnitude.

See “Serial Interface Controller” on page 442 for protocol descriptions, bit descriptions and timing information.

Preamplifier Configuration and Selection

The VM623206 was designed for a single or multiple preamp configuration. All control lines may be shared (including the two serial lines SCLK and SDIO).

The PWREN bit (register 1, bit <D4>) is used to place the inactive (unselected) preamp in either Standby or Idle mode.

See Tables 170 and 171 for Mode Select information.

Die Temperature Monitor Capability

A diode is connected to the BIAS pin to provide for the monitoring of die temperature. This diode is referenced to GND.

Sink DC current from the BIAS pin (10µA to 1mA) and monitor the voltage with respect to GND. VTC recommends calibrating the diode in Idle mode initially.

Idle Mode

In the idle mode, power dissipation is reduced to a minimum. All circuitry is powered-down except the mode control circuitry and the serial registers (the contents of which remain latched).

Idle mode is selected by taking the $\overline{CS}$ pin high.

Serial interface fault detection is active in this mode, but write and read fault detection is disabled.

Note: Setting the IDLEOVR bit high (register 1, bit <D1>) forces Idle mode, regardless of the state of the $\overline{CS}$ pin.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk.

In the read mode the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry are active.

The VM623206 uses the current-bias/voltage-sensing MR architecture. The magnitude of the MR bias current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the MR bias current magnitude:

$$I_{MR} = \frac{(k_{IMR} \times 0.602) + 13.34}{R_{ext}} \times \left[\frac{380}{R_{MR} + 340}\right] \qquad \textit{(eq. 87)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
k_{IMR} represents the MR bias DAC setting (0 to 31).

MR head center voltages are controlled in all modes and are held near ground potential. This reduces the possibility of damaging head-media arcing and minimizes current spikes during disk contacts. Selected heads are held within ±300mV of ground and unselected heads are held at approximately -800mV.

Read Gain

The gain is nominally 220 V/V with a head resistance of 40Ω. The formula that describes the actual gain is shown below:

$$A_V = \frac{380}{340 + R_{MR}} \times 220 \qquad \textit{(eq. 88)}$$

Note: Setting the GAIN bit high (register 3, bit <D5>) selects a nominal gain of 300 V/V.

MR Bias Enable

Taking the BIAS pin high activates the MR Bias current. to the specified head. Note that setting the BIASOVR bit (register 1, bit <D2> high also activates bias current.

Note: Taking the BIAS pin low invokes a “Read Inactive” mode where bias current is diverted internally to a dummy head. See “Read Inactive Mode” on page 440.

MR Bias DAC

The 5 bits in register 3 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

BHV (Buffered Head Voltage)

Setting the BHVOE bit high (register 1, bit <D5>) enables the output of the $(I_{MR} \times R_{MR}) \times 5$ product of the selected head at the BHV pin. This output is single-ended with respect to ground. When bit BHVOE is reset, the output pin BHV enters a low-impedance (low-Z) state to minimize noise coupling.

Note: The reader outputs are disabled.

Fast Read Mode

Setting the FAST bit high (register 1, bit <D0>) increases the high-pass corner frequency of the amplifier’s bandpass from a nominal value of 300 kHz to 9MHz.

Fault Detection

In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Low power supply voltage
- Invalid head select code
- Device in write mode

Read Inactive Mode

Taking the BIAS pin low in Read mode or selecting an invalid head (setting both the HS2 and HS1 bits high; register 0, bits <D2-D1>) invokes a “Read Inactive” mode where bias current is diverted internally to a dummy head.

The chip drives the RDP/RDN outputs to normal levels and its power consumption is unaffected.

Write Mode

In the write mode, the circuit operates as a write current switch, driving the thin-film write element of the MR head.

The magnitude of the write current is referenced to the current flowing through an external 2.67kΩ resistor (connected between pin REXT and ground). The following equation governs the write current magnitude:

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$$I_W = \left[\frac{(k_{IW} x 3.44) + 53.34}{R_{ext}}\right]\left(\frac{1}{1 + \frac{R_H}{R_D}}\right) \quad \textit{(eq. 89)}$$

I_W represents the write current flowing to the selected head (in mA).
R_{ext} represents the equivalent resistance between the REXT pin and ground (in kΩ).
R_H represents the series head resistance (in kΩ).
R_D represents the damping resistance (in kΩ).
k_{IW} represents the write current DAC setting (0 to 31).

The write data (PECL) signals on the WDX and WDY lines drive the current switch of the selected head.
See Figure 119 for the timing diagram.

Write Current DAC

The 5 bits in register 2 (<D4-D0>) represent the binary equivalent of the DAC setting (0-31, LSB first).

Read Bias Enabled in Write Mode

Taking the BIAS pin high in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the outputs are disabled. Another circuit is enabled to maintain the common-mode voltage at the reader outputs, thereby substantially reducing write-to-read transition times.

Note: Setting the BIASOVR bit high (register 1, bit <D2>) forces bias current to the selected head, regardless of the setting of the BIAS pin.

Fault Detection

In the write mode, a TTL high on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- Insufficient write data transition frequency (>500ns between transitions)
- Open write head
- No write current

In addition to generating a write fault, the following conditions will result in the shutdown of the write current source and eliminate current flow to any head:

- Invalid head select code
- Low power supply voltage
- Device in read or idle mode
- Head shorted to ground

Note: Invalid head and head shorted faults are latched and can only be cleared by toggling either the R/$\overline{W}$ pin or the CS pin.

Standby Mode (Inactive Preamp Only)

This special mode allows for power management of an inactive preamp.

Setting the PWREN bit high (register 1, bit <D4>) places the inactive preamp in a reduced power consumption Standby mode. Bias current is diverted internally, outputs are not driven, and the serial register remains active. This mode facilitates a rapid recovery when the inactive preamp is selected.

Idle Mode (Inactive Preamp Only)

Setting the PWREN bit low (register 1, bit <D4>) places the inactive preamp in a minimal power consumption Idle mode.

MODE SELECTION

Table 170Mode Select (for the Selected Preamp)

$\overline{CS}$	R/$\overline{W}$	BIAS	HS2 [1] 0:<D2>	HS1 [2] 0:<D1>	MODE
1	X	X	X	X	Idle
0	1	1	valid head		Read
0	1	0	X	X	Read Inactive (bias to dummy head)
0	X	X	1	1	
0	0	0	valid head		Write
0	0	0	1	1	Write (Write Current Disabled)
0	0	1	valid head		Write with Read Bias Enabled
0	0	1	1	1	Write with Read Bias Enabled (Write Current Disabled)

1. The BIASOVR bit (register 1, bit <D2>) forces bias current when set high.
2. The IDLEOVR bit (register 1, bit <D1>) forces Idle mode when set high.

Note: Invalid mode selection will select Idle mode.

Table 171Mode Select (for the Unselected Preamp)

PWREN [1] 1:<D4>	MODE
0	Idle
1	Standby

1. The PWREN bit (register 1, bit <D4>) allows for power management of the inactive (unselected) preamp. When high, an inactive preamp is placed in Standby mode (with reduced power consumption). When low, an inactive preamp is placed in Idle mode (with minimal power consumption).

Table 172Head Select

HS2 0:<D2>	HS1 0:<D1>	HS0 0:<D0>	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	invalid head [1]
1	1	X	invalid head [2]

1. In Write mode, an invalid head select will disable the writer, dump the head selection current to the positive supply and register a fault.
2. In Read mode, an invalid head select will force “Read Inactive” mode, divert the read current to a dummy head and register a fault.

SERIAL INTERFACE

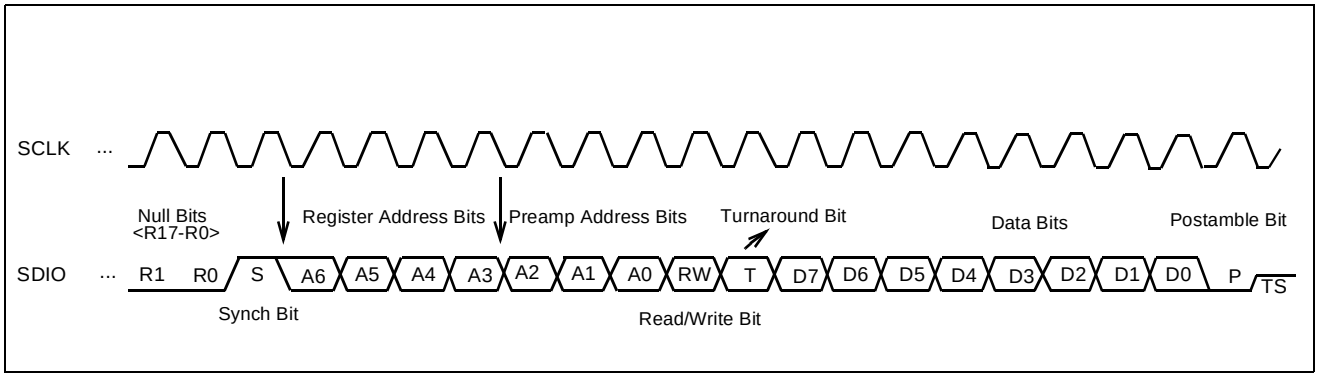


Figure 117 Serial Interface Protocol

Serial Interface Controller

The serial interface has one input line, SCLK (serial clock), and one bidirectional line SDIO (serial data input/output). The SCLK line is used as reference for clocking data into and out-of SDIO. When the serial register is powered down only the output D-latches and the reference generators remain active. 19 bits constitutes a complete data packet.

A sequence of null bits must precede the data packet to ensure proper framing of the data packet. 18 null bits <R17 - R0> are required to initialize the serial register after the initial application of power. Once initialized, only one null bit must precede each data packet.

The first ten bits of a data packet are write-only and consist of one synchronization bit <S>, an unused bit <A6>, three register address bits <A5-A3>, three preamp select bits <A2-A0>, one read/write bit <$\overline{R}$/W>, and one turnaround bit <T>. The next nine bits consist of 8 data bits <D7-D0> to be written-to or read-from a register and a postamble bit <P> (signifying the end of a data packet).

A data transfer is initiated upon the assertion of the serial clock (SCLK). Data present on the serial data input/output line (SDIO) will be latched-in on the rising edge of SCLK. During a write sequence this will continue for 19 cycles; on the 19th rising edge, the data will be written to the addressed register. During a read sequence, SDIO will become active on the falling edge of the 11th cycle. At this time <D7> will be presented and data will continue to be presented on the SDIO line on subsequent falling edges of SCLK. The presentation of the postamble bit in the 19th falling edge signifies the end of the data transfer. The serial interface will only be fully powered between the synchronization and postamble bits.

The finite state machine in the preamp serial interface block must unconditionally complete a transfer sequence by ending in a state where the preamp loads the SDIO line by less than ±160µA (TS). The power-on-reset condition for SDIO is tristate/input mode.

Note: Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and the reader output is disabled during data transfer.

See Tables 173 and 174 for a bit description. See Table 176 and Figure 118 for serial interface timing information.

Fault Detection

A fault condition is triggered by any of the following serial interface conditions:

28) Address fault - If address bits <A5-A3> select an invalid address or when preamp select bits <A2-A0> ≠ 000, the FLT pin is set and further write or read operations cannot be performed until the serial interface is reset.

29) No end of packet bit - If the 19th falling edge of SCLK is not a low signal, the FLT pin is set and further write operations cannot be performed until the serial interface is reset.

30) Vendor ID read - If register 4 is read.

All serial interface faults are cleared by toggling the R/$\overline{W}$ pin from low to high.

Table 173Serial Interface Bit Description -- Address Bits

Function	*Register #*	*Register Address Bits*				*Preamp Address Bits*			*R/W bit*
		<A6>	<A5>	<A4>	<A3>	<A2>	<A1>	<A0>	<W>
Head Select	0	1	0	0	0	0	0	0	1/0[2]
Control	1	1	0	0	1				1/0
Write Current DAC	2	1	0	1	0				1/0
MR Bias Current DAC	3	1	0	1	1				1/0
Vendor ID	4 (read only)	1	1	0	0				0

1. Reserved
2. R/W bit: Read=0, Write=1

Table 174Serial Interface Bit Description -- Data Bits

Function	*Register #*	*Data Bits*							
		<D7>	*<D6>*	*<D5>*	*<D4>*	*<D3>*	*<D2>*	*<D1>*	*<D0>*
Head Select	0	1	1	1	1	1	HS2	HS1	HS0
Control	1	1	1	BHVOE	PWREN	1	BIASOVR	IDLEOVR	FAST
Write Current DAC / Gain	2	1	1	1	IW4	IW3	IW2	IW1	IW0
MR Bias Current DAC	3	1	1	GAIN	IMR4	IMR3	IMR2	IMR1	IMR0
Vendor ID	4 (read only)	0	0	1	1	0	0	0	1

1. Reserved

Table 175Power-on Reset Register Values

Function	*Register Number*	*Power-on Reset Value <D7-D0>*
Head Select	0	<0001 1111>
Control	1	<0000 0010>
Write Current DAC	2	<0000 0000>
MR Bias Current DAC	3	<0000 0000>
Vendor ID	4	<0011 0001>

Table 176Serial Interface Parameters

DESCRIPTION	*SYMBOL*	*MIN*	*NOM*	*MAX*	*UNITS*
Serial Clock (SCLK) Rate				40	MHz
SCLK cycle time	T_c	20			ns
SCLK high time	T_{ckh}	8			ns
SCLK low time	T_{ckl}	8			ns
SCLK risetime (10 - 90%)		0.8		5	ns
SDIO setup time, write	T_s	6			ns
SDIO delay time, read		8			ns
SDIO hold time, write	T_h	1			ns
SDIO hold time, read		3			ns
SDIO risetime (10 - 90%)		0.8		7	ns
Time between I/O operations		25			ns

Note: **SerEna** assertion level is high.

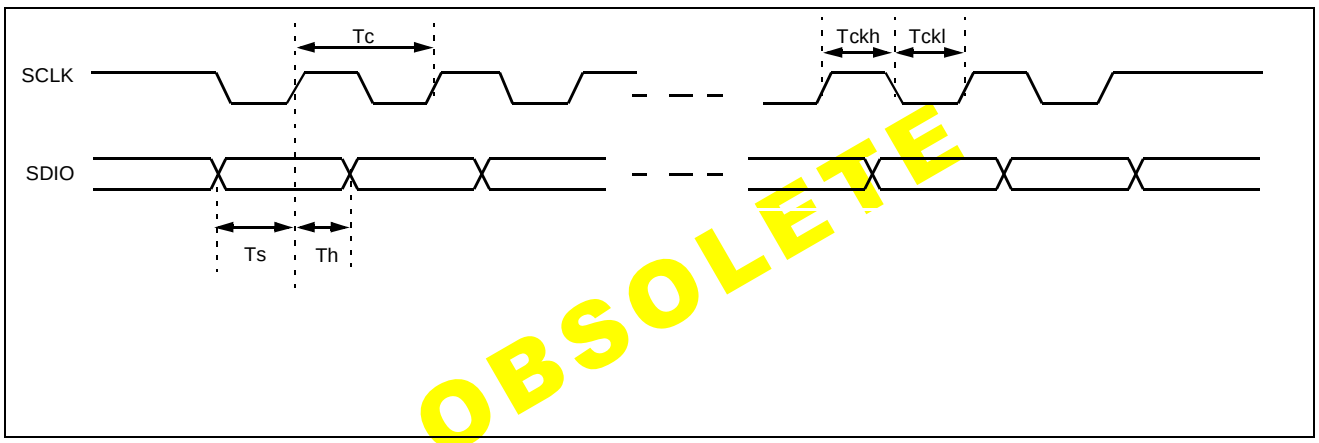


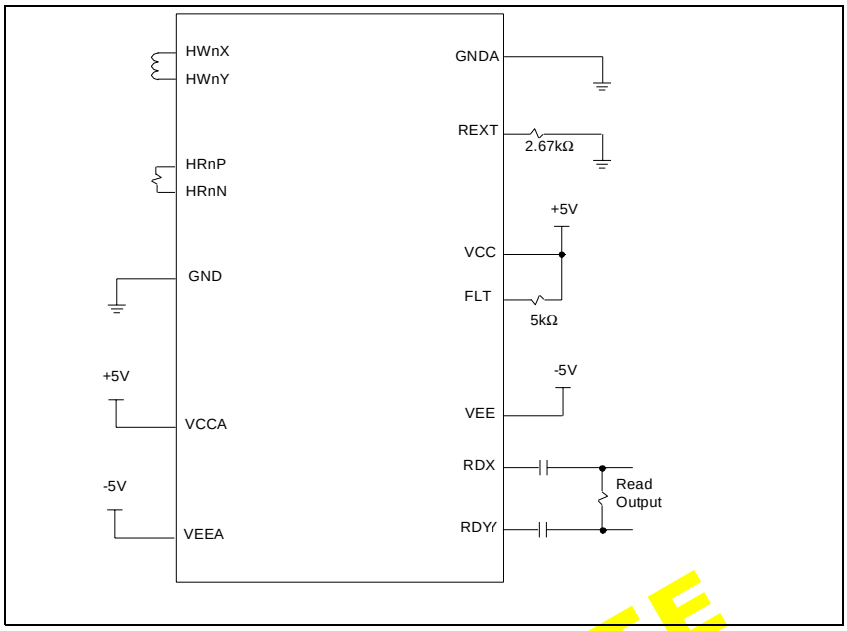
Figure 118 Serial Interface Timing

PIN_FUNCTION LIST AND DESCRIPTION

Signal	*I/O* [1]	*Description*
BHV	O	Buffered MR Head Voltage output.
BIAS	I [2]	Bias Enable: A TTL high level enables MR bias current to the selected head in both read and write modes. Pin defaults low (bias disabled). Note that the BIASOVR bit (register 1, bit <D2>) also forces bias current.
$\overline{CS}$	I [2]	Chip Select: A TTL high level initiates Idle mode. A TTL low level enables operation. If left disconnected, the input defaults to a high state. Note that the IDLEOVR bit (register 1, bit <D1>) also forces Idle mode.
FLT	O [2]	Write/Read Fault: A TTL high level indicates a fault in write mode. A TTL low level indicates a fault in read mode.
GND	[2]	Ground
GNDA	[2]	Analog Ground
HR0P-HR05P	I	MR head connections, positive end.
HR0N-HR05N	I	MR head connections, negative end.
HW0X-HW05X	O	Thin-Film write head connections, positive end.
HW0Y-HW05Y	O	Thin-Film write head connections, negative end
REXT		Reference Voltage pin for both MR bias current and write current.
RDP, RDN	O [2]	Read Data: Differential read signal outputs.
R/$\overline{W}$	I [2]	Read/Write: A TTL low level enables write mode. Pin defaults high (read).
SCLK	I [2]	Serial Clock: Serial port clock; see Figure 118.
SDIO	I/O [2]	Serial Data: Serial port data; see Figure 118.
VCC	[2]	+5.0V supply
VCCA	[2]	Analog +5.0V supply
VEE	[2]	-5.0V supply
VEEA	[2]	Analog -5.0V supply
WDX, WDY	[2]	Differential Pseudo-ECL write data inputs.

1. I = Input pin, O = Output pin
2. When more than one device is used, these signals can be wire-OR'ed together.

TYPICAL APPLICATION CONNECTIONS



Note: The structure placements in the diagram are not meant to indicate pin/pad locations (See “6-CHANNEL CONNECTION DIAGRAM” on page 452 for pin/pad locations). The connections shown will apply regardless of pin/pad location variation.

Application Notes:

- Power supplies have been separated by Read/Write functionality to reduce noise coupling.
  If separate supplies are not available, VTC recommends that the supply lines be connected externally some distance from the preamp.
- Data transfers should only take place in idle or write modes. I/O activity is not recommended in read mode and will result in reader performance degradation.
- VTC recommends placing decoupling 0.1 µF and 0.01 µF capacitors in parallel between the following pins:
  VCC - GND
  VEE - GND
  VCCA - GNDA
  VEEA - GNDA
- For maximum stability, place the decoupling capacitors and the R_{EXT} resistor as close to the pins/pads as possible.

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STATIC (DC) CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 10 mA, I_W = 40 mA.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Power Supply Current	I_{CC}	Read Mode		115	TBD	mA
		Write Mode		105	TBD	
		Write Mode, Reader Biased		155	TBD	
		Idle Mode		20	TBD	
V_{EE} Power Supply Current	I_{EE}	Read Mode		40	TBD	mA
		Write Mode		70	TBD	
		Write Mode, Reader Biased		88	TBD	
		Idle Mode		2	TBD	
Power Supply Dissipation	P_d	Read Mode		750	TBD	mW
		Write Mode		850	TBD	
		Write Mode, Reader Biased		1215	TBD	
		Idle Mode		125	135	
Input High Voltage	V_{IH}	PECL	1.8		VCC-0.7	V
		TTL	2.0		VCC+0.3	
Input Low Voltage	V_{IL}	PECL	1.4		V_{IH}-0.4	V
		TTL	-0.3		0.8	
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH}=2.7V			80	
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL}=0.4V	-160			
Output High current	I_{OH}	FLT: V_{OH}=5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL}=4mA			0.6	V
VCC Fault Threshold	V_{DTH}		3.75	4.0	4.25	V
V_{EE} Fault Threshold	V_{ETH}		-4.25	-4.0	-3.75	V

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR} = 10mA, R_{MR} = 40Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
MR Head Current Range	I_{MR}	R_{EXT}=2.67kΩ	3		10	mA
MR Head Current Tolerance	I_{MR}	R_{EXT}=2.67kΩ	-5		+5	%
Unselected MR Head Current					15	µA
REXT Pin Voltage	V_{SET}	R_{EXT}=2.67kΩ		2.0		V
I_{REXT} to MR Bias Current Gain	A_{IMR}			5		mA/mA
Differential Voltage Gain	A_V	VIN = 1mVpp @ 10MHz, RL(RDP, RDN) = 1kΩ, IMR=10mA, RMR=40Ω Gain Bit=0 Gain = 385*220/(340+R_{MR})	180	220	260	V/V
		Gain Bit=1 Gain = 385*300/(340+R_{MR})	240	300	355	V/V
Passband Upper Frequency Limit	f_{HR}	Normal mode -1dB	135	TBD		MHz
		-3dB	250	TBD		
Passband Lower -3dB Frequency Limit	f_{LR}		0.2	0.7	1.5	MHz
Input Noise Voltage	e_n	0.9 MHz < f < 5 MHz		0.50	1.0	nV/√Hz
		5 MHz < f < 135 MHz		0.55	0.65	nV/√Hz
Input Noise Bias Current	i_n	1 MHz < f < 20 MHz		10	14	pA/√Hz
Differential Input Capacitance	C_{IN}	Normal Mode		6	10	pF
Differential Input Resistance	R_{IN}	Normal Mode	TBD	TBD		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN} = 1mV_{pp} @ f = 5 MHz	3			mV_{pp}
Total Harmonic Distortion	THD				2	%
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, 1 MHz < f < 135 MHz	40			dB
Power Supply Rejection Ratio	PSRR	100mV_{pp} on VCC or VEE, 2 MHz < f < 135 MHz	40			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mV_{pp}, 2 MHz < f < 135 MHz	30			dB
Output Offset Voltage	V_{OS}		-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode	VCC - 3.2	VCC -2.9	VCC -2.6	V
Common Mode Output Voltage Difference	ΔV_{OCM}	Read Mode to Write Mode	-250		250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode		50		W
Output Current	I_O	AC Coupled Load, RDP to RDN	4			mA

READ CHARACTERISTICS

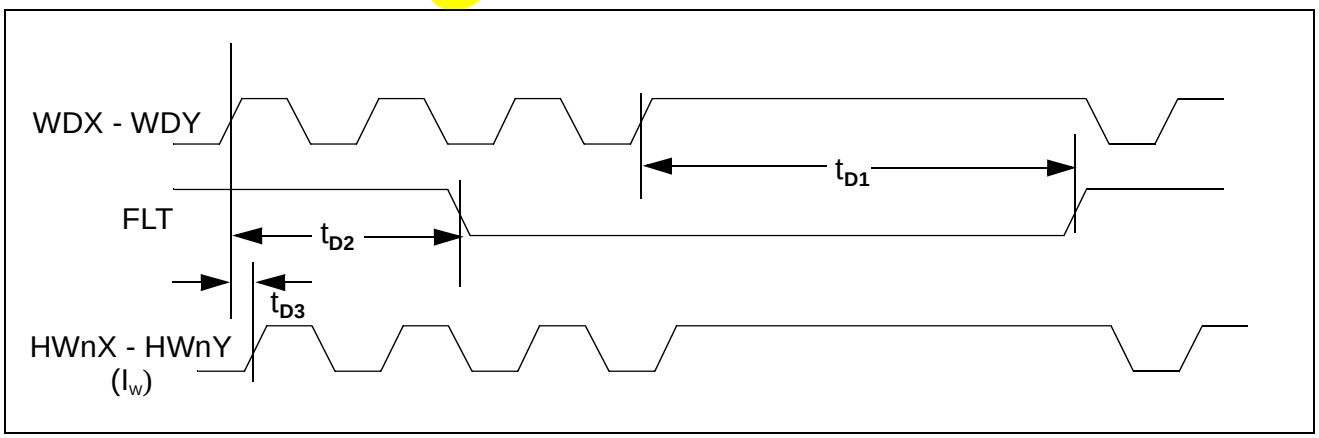
Recommended operating conditions apply unless otherwise specified. I_{MR} = 10mA, R_{MR} = 40Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK}=10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK}=300pF, R_{DISK}=10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}		-400		400	mV
MR Head Potential, Unselected Head	V_{MR}		-1	-.8		V
Buffered Head Voltage Gain	A_{BHV}		4.9	5	5.1	V/V
BHV input referred V_{OS}	Vos_{BHV}		-4		+4	mV
I_{MR}*R_{MR}			100		600	mV

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.
I_W = 40mA, L_H = 100nH, R_H = 10Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
REXT Pin Voltage	V_{SET}	R_{EXT}=2.67kΩ		2.0		V
I_{REXT} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{EXT} * A_I$	36	40	44	V
Write Current Range	I_W	R_{EXT}=2.67kΩ	20		60	mA
Write Current Tolerance	ΔI_W	20 < I_W < 60 mA	-10		+10	%
Differential Head Voltage Swing	V_{DH}	Open Head		6		V_{pk}
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400			mV_{ppd}
Unselected Head Transition Current	I_{UH}	I_W=30mA			100	μA_{pk}
Differential Output Capacitance	C_O				10	pF
Differential Output Resistance	R_O	Damping Resistance present		TBD		Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz
Write Data Frequency for Fault Inhibit	f_{DATA}		35			MHz
Input Termination Resistance				300		Ω



In voltage mode:
When WDX > WDY current will flow from HWnX to HWnY.
When WDY > WDX current will flow from HWnY to HWnX.
In current mode:
When sinking current from WDY current will flow from HWnX to HWnY.
When sinking current from WDX current will flow from HWnY to HWnX.

Figure 119 Write Mode Timing Diagram

SWITCHING CHARACTERISTICS

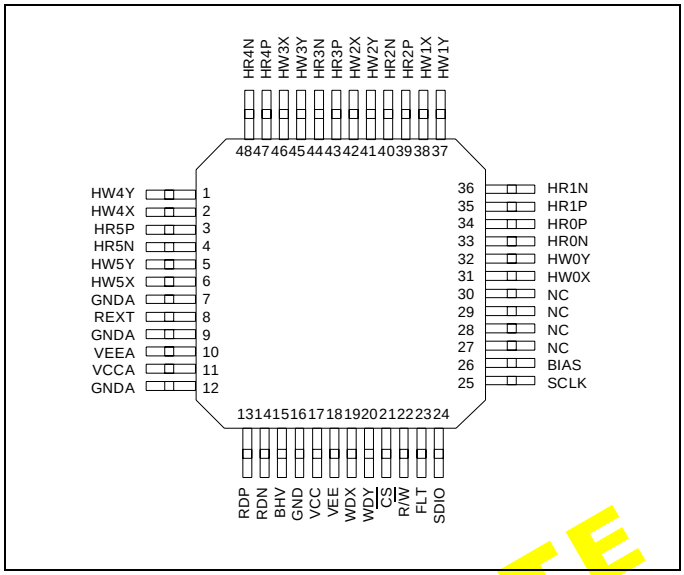
Recommended operating conditions apply unless otherwise specified.
f_{DATA} = 5MHz, L_H = 100nH, R_H = 10Ω, I_W = 40mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			100	ns
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope; ±20mV of final DC value			500	ns
PWRUP to Read Mode (SCLK 19th rising edge)	t_{CS}	To 90% of envelope; ±20mV of final DC value			10	µs
HS0-3 to Any Head (SCLK 19th rising edge)	t_{HS}	To 90% of envelope; ±20mV of final DC value Constant IMR			1	µs
		Change in IMR			3	µs
SCLK (19th rising edge) to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe [1]	t_{D1}	50% WDX to 50% FLT	0.6		3.6	µs
Unsafe to Safe [1]	t_{D2}	50% WDX to 50% FLT			1	µs
Head Current Propagation Delay [1]	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, L_H=0, R_H=0			0.1	ns
Rise/Fall Time	t_r / t_f	20% - 80%		0.950	1.2	ns

1. See Figure 119 for the write mode timing diagram.

VM623206

6-CHANNEL CONNECTION DIAGRAM



6-Channel
48-lead TQFP

Specific Characteristics

See the general data sheet for common specification information.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

2 2-TERMINAL 5V PREAMPLIFIERS

Two-Terminal High-Performance 5 Volt Read/Write Preamplifiers

VTC Inc.
Value The Customer™

VM3500

4, 6 or 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER with MULTIPLE SERVO WRITE CAPABILITY

990812 August 12, 1999

FEATURES

- *General*
  - Single Power Supply (5 V ± 10%)
  - Power Up/Down Data Protect Circuitry
  - Very Low Power Dissipation (3 mW Typical in Sleep Mode)
  - Reduced Write-to-Read Recovery Time
  - Head Inductance Range = 0.2 – 1 µH (0.54 µH Typical)
  - Write Unsafe Detection
  - Available in 4, 6 or 8 Channels
- *High Performance Reader*
  - Read Gain = 300 V/V Typical
  - Input Noise = 0.5nV/√Hz Typical
  - Low Input Capacitance = 8 pF Typical
- *High Speed Writer*
  - Write Current Range 5 - 25 mA
  - I_W Rise/Fall Times = 3.3 ns (L_H = 0.54 µH, I_W = 10 mA b-p)
  - PECL or TTL Write Data Inputs
  - Multi-Channel Servo Write
  - Write Current Range (Servo) 5 - 20 mA
  - Optional Write Data Flip-Flop

DESCRIPTION

The VM3500 is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for up to eight channels.

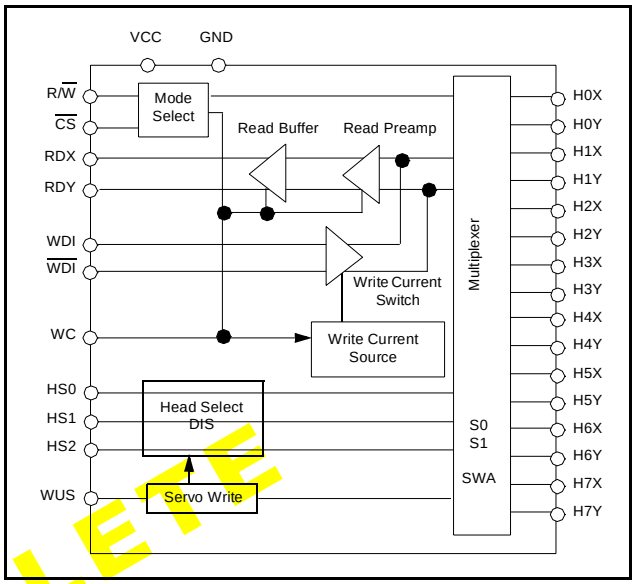
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 3mW.

In multi-channel servo write mode, all heads are written simultaneously. The servo mode is activated via the WUS line.

The VM3500 is available in several different packages. Please contact VTC for package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current, I_W 30mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range, V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O ..... -10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature, Tstg ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 24-lead SSOP ..... 100°C/W
- 32-lead VSOP ..... 100°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%

Write current, I_W ..... 5 to 25mA

Head Inductance, L_H ..... 0.2 to 1µH

Junction Temperature, T_J ..... 25°C to 125°C

CIRCUIT OPERATION

The VM3500 addresses up to eight two-terminal thin-film heads, providing write drive or read amplification. Mode control is accomplished with pins $\overline{CS}$ and R/$\overline{W}$ as shown in Table 177. Head selection is accomplished with pins HS0, HS1 and HS2 as shown in Table 178.

Internal pull-up resistors provided on pins $\overline{CS}$ and R/$\overline{W}$ force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM3500 as a write current switch with the write current toggled between the X and Y side of the selected head in response to transitions on the WDI/$\overline{WDI}$ PECL inputs. The write unsafe (WUS) detection circuitry is also activated at this time to drive the output to a low (Safe) condition.

VM3500: Write current is toggled on each low to high transition of WDI/$\overline{WDI}$. A preceding read operation initializes the write data flip flop (WDFF) so that upon entering the write mode current flows into the "X" port.

VM3500F: For the VM3500F (without the WDFF), the write current polarity is defined by the levels of WDI/$\overline{WDI}$. For WDI > $\overline{WDI}$, current flows into the "X" port; for WDI < $\overline{WDI}$, current flows into the "Y" port.

An internally-generated 2.5 V reference voltage is present at the WC pin. The write current magnitude is determined by an external resistor connected between the WC pin and ground and is defined by the equation:

$$I_W = \left(\frac{K_W}{R_{WC}}\right) + 0.3mA = \left(\frac{50}{R_{WC}}\right) + 0.3mA \quad \textit{(eq. 90)}$$

(0-peak ±10%)

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS:

- No write current
- WDI frequency too low
- Device in read or sleep mode

Two transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

Multi-Channel Servo Write Mode

In servo write mode, the operation is the same as described above except that all channels are written simultaneously. Servo mode is controlled using the WUS pin.

To initiate servo mode:

1. Enter read mode (bring R/$\overline{W}$ high).
2. Select Head 1 (bring HS0 high).
3. Supply 10mA source current into the WUS pin.
4. Enter servo mode (drop the R/$\overline{W}$ line low).

Note: If any other head is selected during servo, the part will exit servo mode and write only the selected head. Unless servo is "formally" exited by removing the 10mA current, servo mode will return whenever head 1 is selected.

To return to normal operations:

1. Enter read mode (bring R/$\overline{W}$ high).
2. Drop the WUS pin (remove the 10 mA current) and return to normal read mode.

Read Mode

The read mode configures the VM3500 as a low-noise differential amplifier. The write current reference remains active to minimize the write/read recovery time. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load.

The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Sleep Mode

In sleep mode ($\overline{CS}$ high), most of the circuit is idle and power dissipation is reduced to 3mW typical.

Table 177Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
0	0	Servo*
1	0	Read
X	1	Idle

* See (Multi-Channel Servo Write Mode on page 4) for additional detail.

Table 178Head Selection

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

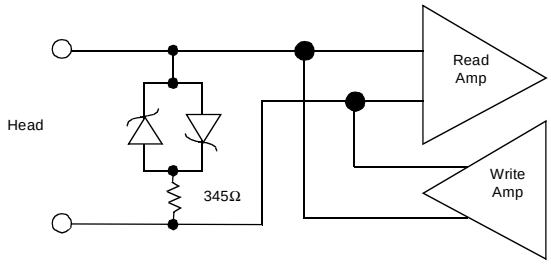
PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I [1]	Head Selects: Selects one of up to eight heads.
H0X - H7X H0Y - H7Y	I/O	X, Y Head Terminals
WDI, $\overline{\text{WDI}}$	I [1]	Write Data Inputs: PECL input signal; a rising edge toggles direction of head current. (Each transition toggles the direction of head current on the “F” option without the write data flip flop.)
$\overline{\text{CS}}$	I	Chip Select: A high level signal puts chip in sleep mode; a low level awakens chip.
R/$\overline{\text{W}}$	I [1]	Read/Write select: A high level selects read mode. A low-level selects write mode
WUS/SE	O [1]	Write Unsafe/Servo Enable: (open collector output) A high level indicates a writes unsafe condition. **Note:** The WUS pin is also used to enter servo mode. See (Multi-Channel Servo Write Mode on page 4).
WC		Write Current Adjust: A resistor adjusts level of write current.
RDX-RDY	O	Read Data Output: Differential output data.
VCC		+5 volt supply
GND		Ground

1. May be wire-OR’ed for multi-chip usage.

Damping Resistor

Unless otherwise indicated, the VM3500 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.



DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
VCC Supply Current	I_{CC}	Read Mode		34 + 0.05I_W	50	mA
		Write Mode, Normal, I_W = 10mA		34 + 1.05I_W	60	
		Write Mode, Servo, I_W = 10mA (4-Channel)		55 + 4.3I_W	125	
		Write Mode, Servo, I_W = 10mA (6-Channel)		100 + 8.6I_W	225	
		Write Mode, Servo, I_W = 10mA (8-Channel)		100 + 8.6I_W	225	
		Sleep Mode		0.5	3	
Power Supply Power Dissipation	PD	Read Mode		175	275	mW
		Write Mode, Normal, I_W = 10mA		225	330	
		Write Mode, Servo, I_W = 10mA (4-Channel)		490	688	
		Write Mode, Servo, I_W = 10mA (6-Channel)		930	1240	
		Write Mode, Servo, I_W = 10mA (8-Channel)		930	1240	
		Sleep Mode		3	16.5	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{\text{WDI}}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.5		V_{CC} - 0.1	V
WDI, $\overline{\text{WDI}}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{IH} - 1.5		V_{IH} - 0.25	V
WDI, $\overline{\text{WDI}}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{\text{WDI}}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	4.0	V
WUS Servo Enable	I_{SE}		10	[1]	20	mA

1. The typical value for servo activation is 6 mA. The minimum value at which servo activation is guaranteed is 10 mA.

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; L_H = 0.54µH, R_H = 20¾, I_W = 10mA, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP [1]	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V ±10%	45	50	55	V
Write Current Range	I_W	10.64k¾ > R_{WC} > 2k¾	5		25	mA
Write Current Tolerance	ΔI_W	V_{CC} ±10%	-10		+10	%
Write Current Tolerance Servo	ΔI_W	V_{CC} ±10%	-14		+14	%
Differential Head Voltage Swing	V_{DH}	Open head @ VCC = 4.5V	5.4	6.0		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				10	pF
Differential Output Resistance	R_{OUT}		3.2			k¾
Unselected Head Current	I_{UH}	I_W = 25mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

SERVO WRITE

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 20mA			10	%
Duty Cycle (20mA/head)		T_A = 25°C, $t_{s\text{-}on}$ < 50ns [1]			50	%

1. The ambient temperature (T_A) and servo-on time ($t_{s\text{-}on}$) limitations are consistent with keeping the peak junction temperature under 125°C.

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1k¾.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* [1]	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	250	300	350	V/V
Bandwidth	BW	-1dB |Zs| < 5¾, V_{IN} = 1mVp-p	50	55		MHz
		-3dB |Zs| < 5¾, V_{IN} = 1mVp-p	90	100		
Input Noise Voltage	e_{in}	BW = 20MHz, L_H = 0, R_H = 0		0.5	0.65	nV/ÐHz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		8	12	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	300	750		¾
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mV P-P
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}	Steady state read	-300		+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.0		
RDX, RDY Common Mode Output Voltage Difference Between Modes	ΔV_{OCM}		-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = 5 MHz			35	¾
Output Current	I_O	AC-coupled load, RDX to RDY	±1			mA

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; I_W = 10mA, f_{DATA} = 5MHz, L_H = 0.54µH, R_H = 20¾, C_L (RDX, RDY) ð 20pF (see Figures 120 and 121).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* [1]	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.06	0.15	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.2	0.4	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 10mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0, I_W = 10mA		1.0	2.0	ns
		10% to 90% points, L_H = 540nH, I_W = 10mA, R_H = 20¾		3.3	5.0	

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

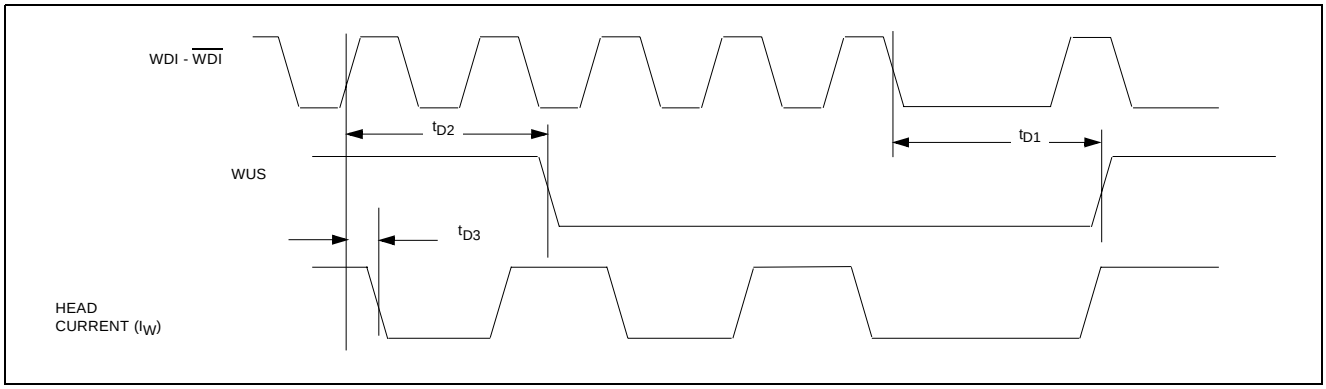


Figure 120 Write Mode Timing Diagram for VM3500

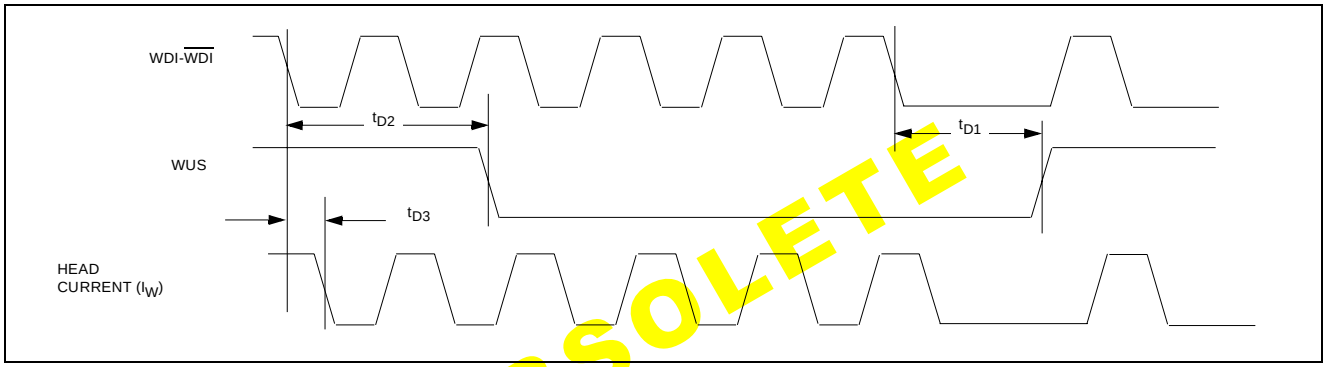


Figure 121 Write Mode Timing Diagram for VM3500F (without write data flip flop)

LIST OF SPECIFIC PART VARIATIONS

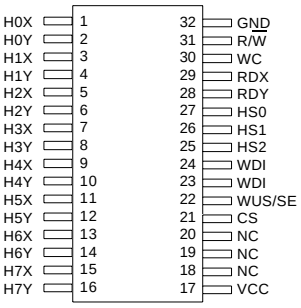
(described on the following pages)

1. This part is non-conventional. See the specific page for details.

OBSOLETE

VM357830

8-Channel Connection Diagram



8-Channel
32-lead VSOP
VM357830FVSM

Note: This part is non-conventional in the following aspects:

- It has an alternate pin-out ($\overline{CS}$ is in a different location).
- It has a bank servo mode where 4 heads are written at a time based on the head selected. (See below.)
- It has a nominal damping resistor value of 250 Ω (Schottky isolated).

Specific Characteristics

See the general data sheet for common specification information.

Multi-Channel Servo Write Mode

In servo write mode, the operation is the same as described in the general datasheet except that four channels are written simultaneously as shown in the table below.

HEAD SELECTED	*HEADS WRITTEN*
0 or 1	none
2	odd (1,3,5 and7)
3	even (0,2,4 and 6)

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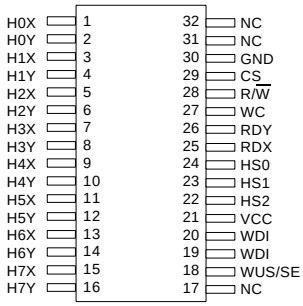
VM355830

8-Channel Connection Diagram



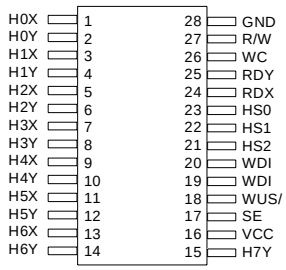
8-Channel
32-lead VSOP
VM355830(F)VSL

Specific Characteristics
See the general data sheet for common specification information.

OBSOLETE

VM355830 (28-lead package)

8-Channel Connection Diagram



8-Channel
28-lead SSOP
VM355830FSS28L

Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

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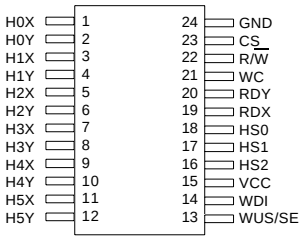
VM356630

6-Channel Connection Diagram



6-Channel
24-lead SSOP
VM356630SSL

Note: This part is non-conventional in one aspect:

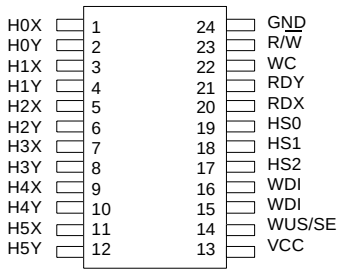
- It has TTL single-ended write data input.
  Write current is toggled on each high-to-low transition of WDI.

Specific Characteristics
See the general data sheet for common specification information.

OBSOLETE

VM355635

6-Channel Connection Diagram



6-Channel
24-lead SSOP
VM355635FSSP

Specific Characteristics

See the general data sheet for common specification information.

- 350 V/V read gain.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	292	350	408	V/V
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		10	14	pF
Single-Ended Output Resistance	R_{SEO}	f = 5 MHz			50	¾

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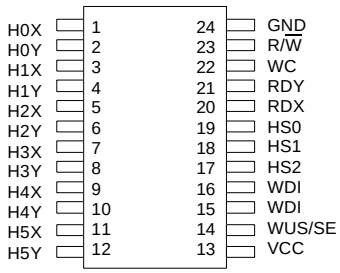
VM355630

6-Channel Connection Diagram



6-Channel
24-lead SSOP
VM355630FSSL

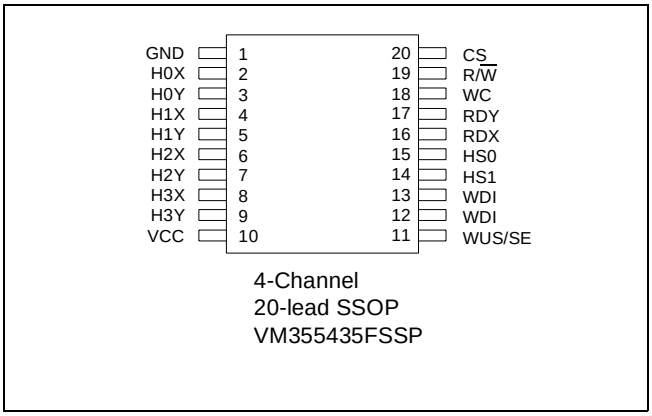
Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

VM355435

4-Channel Connection Diagram



4-Channel
20-lead SSOP
VM355435FSSP

Specific Characteristics

See the general data sheet for common specification information.

- 350 V/V read gain.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	292	350	408	V/V
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		10	14	pF
Single-Ended Output Resistance	R_{SEO}	f = 5 MHz			50	¾

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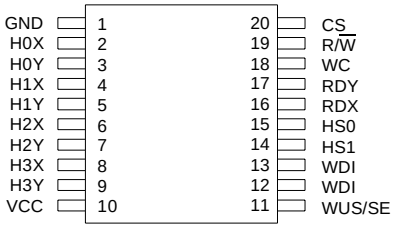
VM355430

4-Channel Connection Diagram



4-Channel
20-lead SOIC, SSOP, VSOP
VM355430SSL

Specific Characteristics
See the general data sheet for common specification information.

VTC Inc.
Value The Customer™

VM3600

4, 6 or 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER with MULTIPLE SERVO WRITE CAPABILITY

990812 August 12, 1999

FEATURES

- *General*
  - Single Power Supply (5 V ± 10%)
  - Power Up/Down Data Protect Circuitry
  - Very Low Power Dissipation (3 mW Typical in Sleep Mode)
  - Reduced Write-to-Read Recovery Time
  - Head Inductance Range = 0.2 – 1 µH (0.54 µH Typical)
  - Write Unsafe Detection
  - Available in 4, 6 or 8 Channels
- *High Performance Reader*
  - Read Gain = 300 V/V Typical
  - Input Noise = 0.54nV/√Hz Typical
  - Low Input Capacitance = 4.6 pF Typical
- *High Speed Writer*
  - Write Current Range 5 - 25 mA
  - I_W Rise/Fall Times = 2.6 ns (L_H = 0.54 µH, I_W = 10 mA b-p)
  - PECL Write Data Inputs
  - Multi-Channel Servo Write
    - Write Current Range (Servo) 5 - 20 mA
  - Optional Write Data Flip-Flop

DESCRIPTION

The VM3600 is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for up to eight channels.

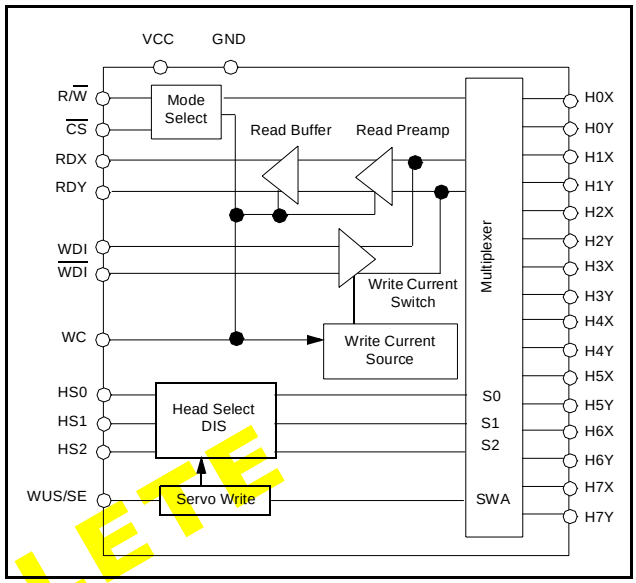
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques. When unselected, the device enters a sleep mode with reduced power dissipation.

In multi-channel servo write mode, all heads are written simultaneously. The servo mode is activated via the WUS/SE line.

The VM3600 is available in several different packages. Please contact VTC for package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current, I_W 30mA

Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS/SE Pin Voltage Range, V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O ..... -10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature, Tstg ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W
- 24-lead SSOP ..... 100°C/W
- 32-lead VSOP ..... 100°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%

Write current, I_W ..... 5 to 25mA

Head Inductance, L_H ..... 0.2 to 1µH

Junction Temperature, T_J ..... 25°C to 125°C

CIRCUIT OPERATION

The VM3600 addresses up to eight two-terminal thin-film heads, providing write drive or read amplification. Mode control is accomplished with pins $\overline{CS}$ and R/$\overline{W}$ as shown in Table 179. Head selection is accomplished with pins HS0, HS1 and HS2 as shown in Table 180.

Internal pull-up resistors provided on pins $\overline{CS}$ and R/$\overline{W}$ force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM3600 as a write current switch with the write current toggled between the X and Y side of the selected head in response to transitions on the WDI/$\overline{WDI}$ PECL inputs. The write unsafe (WUS) detection circuitry is also activated at this time to drive the output to a low (Safe) condition.

VM3600**:** Write current is toggled on each low to high transition of WDI/$\overline{WDI}$. A preceding read operation initializes the write data flip flop (WDFF) so that upon entering the write mode current flows into the “X” port (see Figure 122).

VM3600**F:** For the VM3600F (without the WDFF), the write current polarity is defined by the levels of WDI/$\overline{WDI}$. For WDI > $\overline{WDI}$, current flows into the “X” port; for WDI < $\overline{WDI}$, current flows into the “Y” port (see Figure 123).

An internally-generated 2.5 V reference voltage is present at the WC pin. The write current magnitude is determined by an external resistor connected between the WC pin and ground and is defined by the equation:

$$I_W = \left(\frac{50}{R_{WC}}\right) + 0.2\text{mA} \qquad \textit{(eq. 91)}$$

(0-peak ±10%)

Fault Detection

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS/SE:

- No write current
- WDI transition frequency too low
- Device in read or sleep mode

Two transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

Multi-Channel Servo Write Mode

In servo write mode, the operation is the same as described above except that all channels are written simultaneously. Servo mode is controlled using the WUS/SE pin.

To initiate servo mode:

1. Enter read mode (bring R/$\overline{W}$ high).
2. Select Head 1 (bring HS0 high).
3. Supply 10mA source current into the WUS/SE pin.
4. Enter servo mode (drop the R/$\overline{W}$ line low).

Note: If any other head is selected during servo, the part will exit servo mode and write only the selected head. Unless servo is “formally” exited by removing the 10mA current, servo mode will return whenever head 1 is selected.

To exit servo mode:

1. Enter read mode (bring R/$\overline{W}$ high).
2. Drop the WUS/SE pin (remove the 10 mA current) and return to normal read mode.

Read Mode

The read mode configures the VM3600 as a low-noise differential amplifier. The write current reference remains active to minimize the write/read recovery time. The RDX and RDY outputs are emitter followers and are in phase with the “X” and “Y” head ports. These outputs should be AC-coupled to the load.

The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Sleep Mode

In sleep mode ($\overline{CS}$ high), most of the circuit is idle and power dissipation is reduced to 3mW typical.

Table 179Mode Select

R/$\overline{W}$	*CS*	*MODE*
0	0	Write
0	0	Servo [1]
1	0	Read
X	1	Sleep

1. See Multi-Channel Servo Write Mode for additional detail.

Table 180Head Selection

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

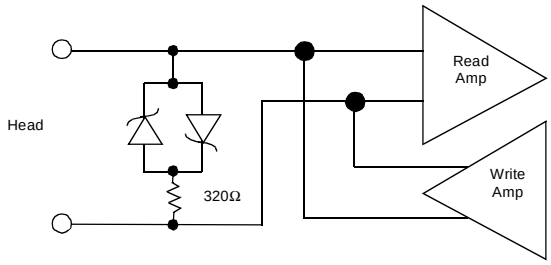
PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I [1]	Head Selects: Selects one of up to eight heads.
H0X - H7X H0Y - H7Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I [1]	Write Data Inputs: PECL input signal; a rising edge toggles direction of head current. (Each transition toggles the direction of head current on the “F” option without the write data flip flop.)
$\overline{CS}$	I	Chip Select: A high level signal puts chip in sleep mode; a low level awakens chip.
R/$\overline{W}$	I [1]	Read/Write select: A high level selects read mode. A low-level selects write mode
WUS/SE	O	Write Unsafe/Servo Enable: (open collector output) A high level indicates a writes unsafe condition. **Note:** The WUS/SE pin is also used to enter servo mode. See (Multi-Channel Servo Write Mode on page 22).
WC		Write Current Adjust: A resistor adjusts level of write current.
RDX-RDY	O [1]	Read Data Output: Differential output data.
VCC		+5 volt supply
GND		Ground

1. May be wire-OR’ed for multi-chip usage.

OPTIONAL DAMPING RESISTOR

The VM3600 is available with damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.



An “N” in the specific part number indicates that no damping resistors have been incorporated into the part.

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
VCC Supply Current	I_{CC}	Read Mode		28 + 0.2I_W	40	mA
		Write Mode, Normal, I_W = 10mA		22 + 1.2I_W	50	
		Write Mode, Servo, I_W = 10mA (4-Channel)		52 + 4.3I_W	140	
		Write Mode, Servo, I_W = 10mA (6-Channel)		100 + 8.6I_W	210	
		Write Mode, Servo, I_W = 10mA (8-Channel)		100 + 8.6I_W	210	
		Sleep Mode		0.5	3	
Power Supply Power Dissipation	PD	Read Mode		155	220	mW
		Write Mode, Normal, I_W = 10mA		200	302.5	
		Write Mode, Servo, I_W = 10mA (4-Channel)		475	770	
		Write Mode, Servo, I_W = 10mA (6-Channel)		1145	1500	
		Write Mode, Servo, I_W = 10mA (8-Channel)		1145	1500	
		Sleep Mode		2.5	16.5	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{\text{WDI}}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 2.0		V_{CC}	V
WDI, $\overline{\text{WDI}}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{IH} - 1.0		V_{IH} - 0.1	V
WDI, $\overline{\text{WDI}}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			160	µA
WDI, $\overline{\text{WDI}}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	3.9	V
WUS Servo Enable	I_{SE}		10	[1]	20	mA

1. The typical value for servo activation is 6 mA. The minimum value at which servo activation is guaranteed is 10 mA.

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; L_H = 0.54µH, R_H = 20Ω, I_W = 10mA, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP [1]	MAX	UNITS
WC Pin Voltage	V_{WC}		2.2	2.5	2.9	V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V ±10%	46	50	54	V
Write Current Range	I_W	10.64kΩ > R_{WC} > 2.54kΩ	5		25	mA
Write Current Tolerance	ΔI_W	V_{CC} ±10%	-10		+10	%
Write Current Tolerance Servo	ΔI_W	V_{CC} ±10%	-14		+14	%
Differential Head Voltage Swing	V_{DH}	Open head @ VCC = 4.5V	5.0	6.0		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				5	pF
Differential Output Resistance	R_{OUT}		4.8			kΩ
Unselected Head Current	I_{UH}	I_W = 25mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

1. Typical values are given at VCC = 5V and TA = 25×C.

SERVO WRITE

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 20mA			10	%
Duty Cycle (15mA/head)		T_A = 25°C, $t_{s\text{-}on}$ < 17ms [1]			60	%

1. The ambient temperature (T_A) and servo-on time ($t_{s\text{-}on}$) limitations are consistent with keeping the peak junction temperature under 125°C.

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* [1]	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	250	300	350	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	70	100		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	130	180		
Group Delay Deviation	GDD	over frequency range from DC to -1dB, L_H = 0, R_H = 0 (-0.5 dB as the reference)	-150		150	ps
Input Noise Voltage	e_{in}	BW = 20MHz, L_H = 0, R_H = 0		0.54	0.65	nV/√Hz
Input Noise Current	i_{in}			3.7	4.5	pA/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 20-80MHz		4.6	7	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 20-80MHz	920	2250		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mV P-P
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	65			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}	Steady state read	-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference Between Modes	ΔV_{OCM}		-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = 5 MHz			35	Ω
Output Current	I_O	AC-coupled load, RDX to RDY	±1			mA

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; I_W = 10mA, f_{DATA} = 5MHz, L_H = 0.54µH, R_H = 20Ω, C_L (RDX, RDY) ≤ 20pF (see Figures 122 and 123).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* [1]	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		30	100	ns
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		20	100	ns
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS7 any Head Delay	t_{HS}	HS0 - HS7 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 10mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0, I_W = 10mA		1.1	1.5	ns
		10% to 90% points, L_H = $_{540}$nH, I_W = 10mA, R_H = 20Ω		2.6	6	
		Rise time with Damping resistor; 10% to 90% points, L_H = $_{540}$nH, I_W = 10mA, R_H = 20Ω		3.6	6	

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

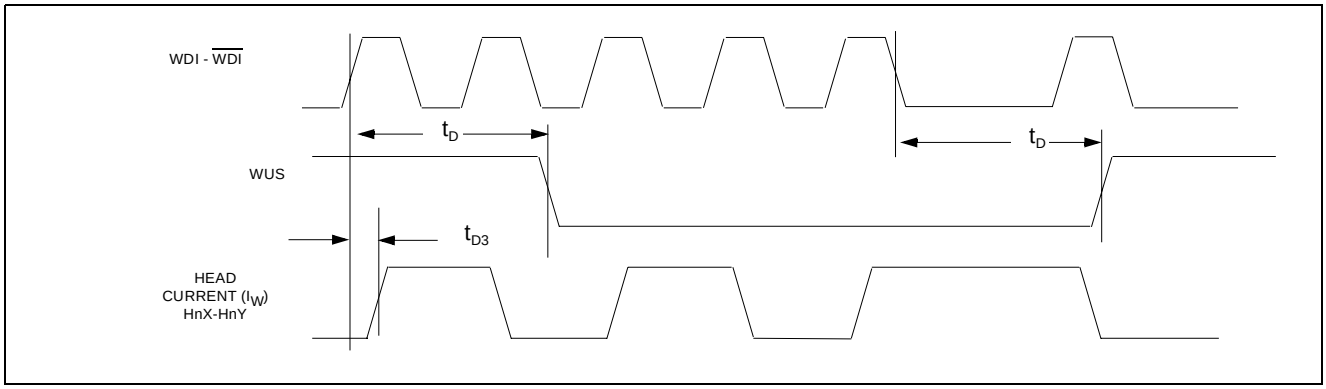


Figure 122 Write Mode Timing Diagram for VM3600

Note: The write current polarity is toggled on each low to high transition of the expression (WDI - $\overline{WDI}$).
A preceding read operation initializes the WDFF so that upon entering the write mode, current flows into the “X” port.

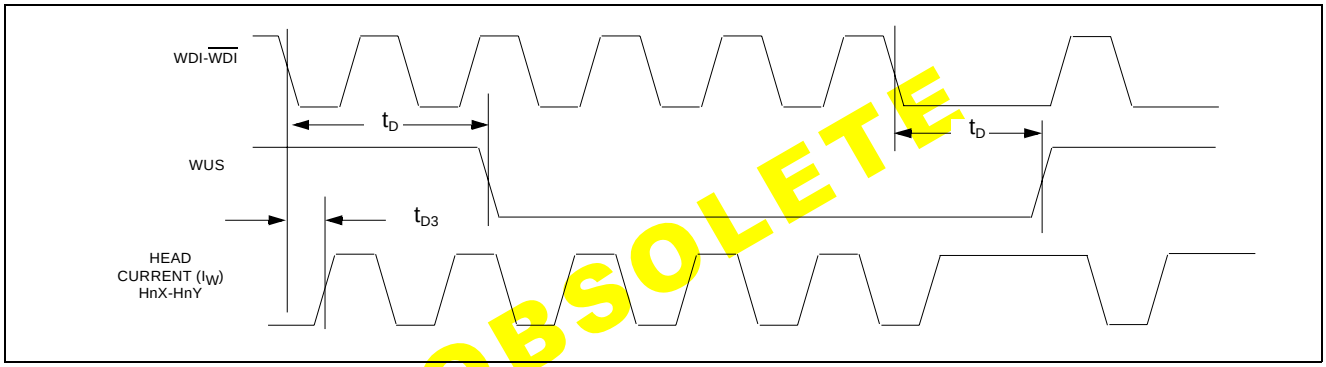
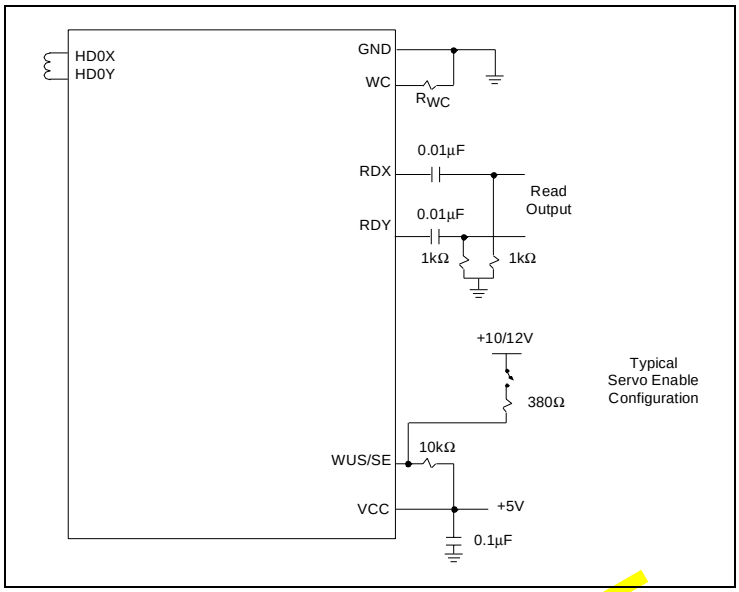


Figure 123 Write Mode Timing Diagram for VM3600F (without write data flip flop)

Note: The write current polarity is defined by the levels of WDI and $\overline{WDI}$ (shown in the expression WDI - $\overline{WDI}$).
For WDI>$\overline{WDI}$ current flows into the “X” port; for WDI<$\overline{WDI}$ current flows into the “Y” port.

TYPICAL APPLICATION CONNECTIONS



Note: The pin placements in the diagram are not meant to be exact and will vary between packages. The connections shown will apply regardless of package variation.

Application Notes:

- For maximum stability, place the decoupling capacitors and the R_{WC} resistor as close to the package pins as possible.
- The voltage at the WUS/SE pin will clamp at two diode drops above VCC.
- The typical servo-enable configuration shown above is presented as an example. Other supply and resistor values are possible, and the supply/resistor symbols shown could be displayed as a 10 mA current source.

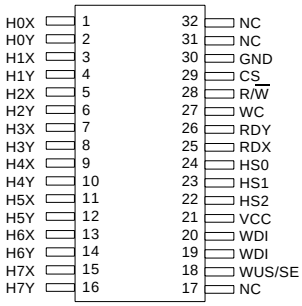
LIST OF SPECIFIC PART VARIATIONS

(described on the following pages)

PART VARIATION	*Page Location*
VM365N830	31
VM365N830 (30-lead package)	32
VM365N630	33
VM365N430	34

VM365N830

8-Channel Connection Diagram



8-Channel
32-lead VSOP
VM365N830VSJ

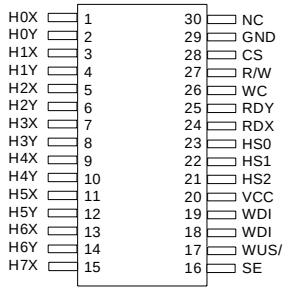
Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

VM365N830 (30-lead package)

8-Channel Connection Diagram



8-Channel
30-lead SSOP
VM365N830SS30J

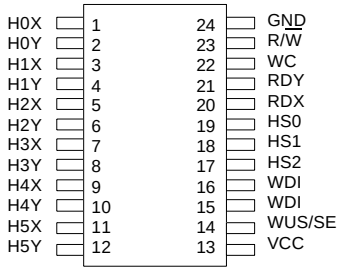
Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

VM365N630

6-Channel Connection Diagram



6-Channel
24-lead SSOP
VM365N630SS

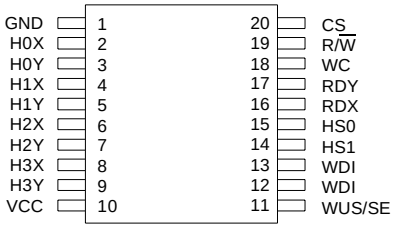
Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

VM365N430

4-Channel Connection Diagram



4-Channel
20-lead SSOP, VSOP
VM365N430SSK
VM365N430VSK

Specific Characteristics

See the general data sheet for common specification information.

OBSOLETE

3 MIXED SIGNAL CIRCUITS

Mixed Signal Circuits

VTC Inc.
Value The Customer™

VM65011

ANALOG PRML CHANNEL for DIGITAL VHS APPLICATIONS

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

Sampled data read channel with maximum likelihood Viterbi detection

- Programmable continuous-time filter with two independently-variable real zeros
- Programmable five tap transversal filter for PR4 equalization
- Self-adapting option for FIR tap weights
- Analog/sampled AGC
- Fast timing recovery loop which locks to random data
- Programmable data dropout detector
- Automatic tracking frequency servo tone filters and demodulator
- Programmable write current reference for Read/Write preamplifier
- Register-programmable power management (<5 mW Power Down Mode)
- Serial interface port for access to internal configuration registers to load and verify register contents
- Single power supply (5V ±10%) with optional 3.3V CMOS output supply
- Small footprint 64-pin PQFP package

DESCRIPTION

The VM65011 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement a Partial Response Maximum Likelihood (PRML) read channel for DVC systems with user data rates at 42.85 Mbps.

BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 64-Lead PQFP package.

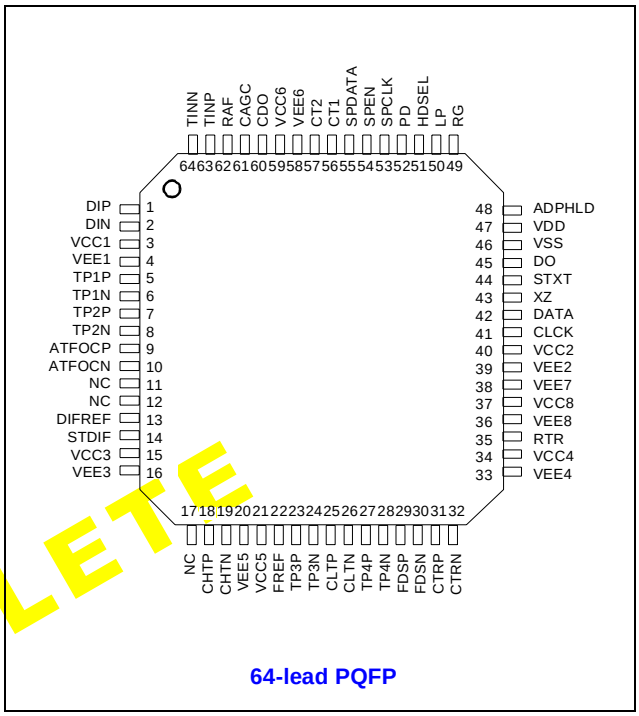
Functional blocks include AGC, programmable continuous time filter, adaptive FIR filter, maximum likelihood Viterbi detector, 2-tone ATF servo processor and data dropout detector.

Programmable functions such as filter cutoff/boost, FIR tap weights, adaption parameters, preamplifier write current, dropout detector gain and ATF gain are controlled by writing to the serial port registers. External component changes are required to change data rates.

The VM65011 achieves an entire read channel with only two ICs when used in conjunction with a suitable preamplifier, such as the VM355435F.

For additional information, call VTC.

CONNECTION DIAGRAM



64-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC}, V_{DD} ..... -0.3V to +7V

Input Voltages, V_{CC} referenced
- Input Voltage ..... -0.3V to V_{CC} + 0.3V

Input Voltages, V_{DD} referenced
- Input Voltage ..... -0.3V to V_{DD} + 0.3V

Storage Temperature T_{stg} ..... -65°C to 150°C

Junction Temperature T_J ..... 150°C

Thermal Impedance, Θ_{JA}
- still air ..... 51°C/W
- 200 fpm air flow ..... 38°C/W
- 600 fpm air flow ..... 27°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage
- V_{CC} ..... 4.5V to 5.5V
- V_{DD} ..... 3.0V to 5.5V

Junction Temperature T_J ..... 0°C to 125°C

External Components
- R_{WC} ..... 3.5kΩ to 12kΩ
- R_{TR} ..... 2.0kΩ to 6kΩ
- R_{AF} ..... 4.0kΩ to 32kΩ
- R_{FSR} ..... 10kΩ to 40kΩ
- R_{LZ} ..... 10kΩ to 40kΩ
- R_L ECL Outputs to V_{EE} ..... 200Ω to 1kΩ
- R_L ECL Outputs to V_{CC} -2V ..... 50Ω to 100Ω

MIXED SIGNAL CIRCUITS

BLOCK DIAGRAM AND DESCRIPTION

General

- Sampled data read channel with Viterbi detection
- Programmable continuous-time filter with two independently variable real zeros
- Programmable five tap transversal filter for PR4 equalization
- Analog/decision-directed AGC
- Fast timing recovery loop which locks to random data
- Dropout detector
- Automatic tracking frequency servo tone filters and demodulator
- Register programmable power management (<5 mW Power Down Mode)
- Serial interface port for access to internal configuration registers to load and verify register contents
- Single power supply (5V ±10%) with optional 3.3V CMOS output supply
- Small footprint 64-pin PQFP package

Automatic Gain Control

- Dual mode AGC, analog during acquisition, decision-directed during read data
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during data read
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Externally adjustable one-shot pulse width for Low Z control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

Low Pass Filter/Equalizer

- Programmable, 7-pole, 0.05° equiripple continuous time filter used for PR4 shaping
- Programmable cutoff frequency of 5 to 15MHz
- Programmable boost/equalization of 0 to 13dB
- Programmable group delay of ±30%
- Minimal size and power

FIR Filter/Equalizer

- Five-tap adaptive filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- ADP hold function controlled by external pin or internal 6T detector

Maximum Likelihood Detector

- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length of 10 or 21
- Excess zeros counter monitoring consecutive recovered data zeros to aid in tape dropout detection

Timing Recovery

- Single external capacitor required
- Fast Acquisition, sampled-data phase-locked loop which locks to random data
- Decision-directed clock recovery from data samples
- Programmable damping ratio

Automatic Tracking Frequency

- Phase-locked loop to select 465kHz and 697.5kHz servo tones buried in the data spectrum
- Programmable VGA to compensate for head and signal variations
- Front end bandpass with gain and test output
- Low-tone gain adjustment capability for channel response compensation
- Output difference amplifier with separate bias pin allowing differential measurement
- Servo burst output indicator with programmable threshold

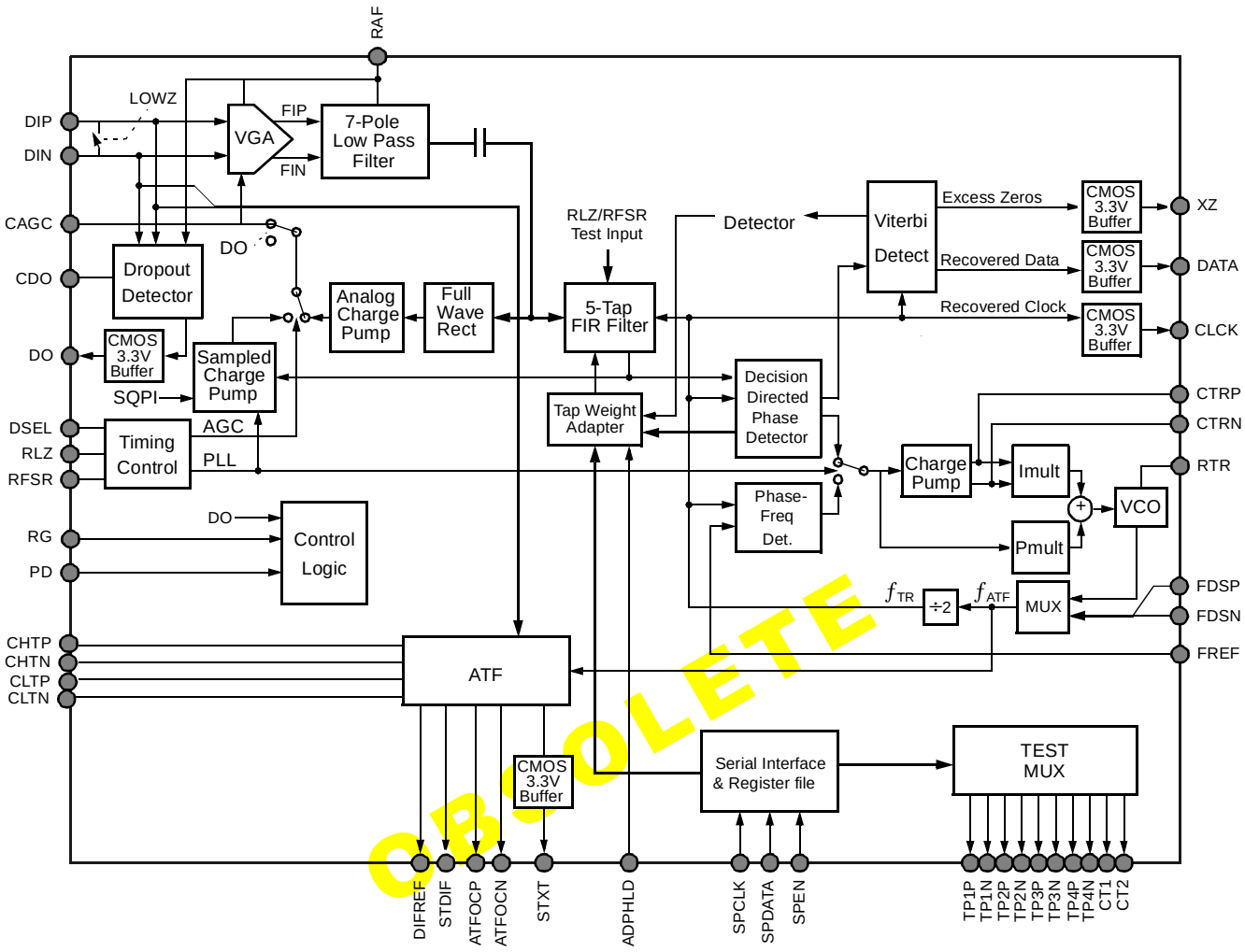


Figure 124 VM65011 Block Diagram

DEFINITIONS AND ABBREVIATIONS

AGC	Automatic Gain Control
ATF	Automatic Tracking Frequency
Biquad	Combination of two integrator stages to produce a two-pole filter element
BiCMOS	Bipolar and CMOS technology
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CTF	Continuous Time Filter
DAC	Digital to Analog Converter
DLL	Delay Locked Loop A PLL with a variable delay cell rather than a VCO. Phase is variable but not frequency
DO	Dropout
DVCR	Digital Video Cassette Recorder
ECL	Emitter-Coupled Logic
EQ	Equalization
FET	Field Effect Transistor
FIR	Finite Impulse Response
fpm	Feet Per Minute
f_0	Center Frequency
f_c	Cutoff Frequency
f_s	Sample Frequency
g_m-C	Transconductance-capacitor integrator stage used in filter
IC	Integrated Circuit
K_V	VCO gain in MHz/V
K_{VCO}	VCO gain in Mrad/V
LPF	Low-Pass Filter
LSB	Least Significant Bit
LMS	Least Mean Squared
Mbps	Megabits per second
ML	Maximum Likelihood
MSB	Most Significant Bit
PGC	Programmable Gain Control
PLL	Phase-Locked Loop
PR	Partial Response
PRML	Partial Response Maximum Likelihood, a type of data recovery
PQFP	Plastic Quad Flat Pack
RM	Read Mode
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator
VCR	Video Cassette Recorder
VGA	Variable Gain Amplifier
VIT_{TH}	Viterbi Detector Threshold Voltage
V_{THDO}	Dropout Detector Threshold Voltage
V_{THST}	Servo STXT output Threshold Voltage
V_{THTR}	Timing Recovery Threshold Voltage
V_{ppd}	Peak-to-Peak Differential Voltage
WM	Write Mode

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BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTION

The VM65011 implements a complete high performance PR4 read channel. The VM65011 includes an AGC, programmable continuous-time filter/equalizer, programmable FIR filter/equalizer with adaptation circuitry, Viterbi algorithm maximum likelihood (ML) detector, decision-directed clock recovery, automatic tracking frequency (ATF) servo tone filters and demodulator, and a write current reference for the read/write preamp. A three-wire serial interface is provided to configure the internal storage registers.

Gain Control

The Gain Control section of the VM65011 consists of a wide-band variable gain amplifier (VGA) with an input impedance switch, a programmable continuous time filter, charge pump, amplitude detector, and exponentiator. A block diagram is shown in Figure 125. The Gain Control has two modes: automatic (AGC), and programmable (PGC) gain control. The mode of the Gain Control is selected by the PGCEN control register bit such that PGCEN='0' defines the AGC mode and PGCEN='1' defines PGC mode. Gain Control is active during Read mode (RM) or Idle mode, defined by setting the WG pin to a '0'.

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the output of the continuous time filter while the input is allowed to vary over a 10:1 range. During signal acquisition an analog AGC loop is used to insure quick convergence to the correct signal amplitude. In Tracking mode a sampled/decision- directed closed loop AGC is used for improved accuracy. The programmable gain control (PGC) circuit is used for test purposes to control the VGA gain with an internal DAC. In PGC mode the AGC loop is disabled, and the VGA gain is a linear function of the DAC count. The read signal is externally AC coupled into the VGA amplifier on the DIP/DIN pins. The gain of the VGA is controlled by the voltage stored on the C_{AGC} hold capacitor. The read signal is amplified and equalized by the continuous time filter. The output of the filter, FNP/FNN, is internally AC coupled, creating the FAP/FAN signal, which connects to an amplitude detector and the FIR filter. The continuous-time AGC loop locks the differential peak-to-peak voltage at FAP/FAN to $V_{FA}=0.5V_{ppd}$ for inputs ranging from 30-300mV_{ppd}.

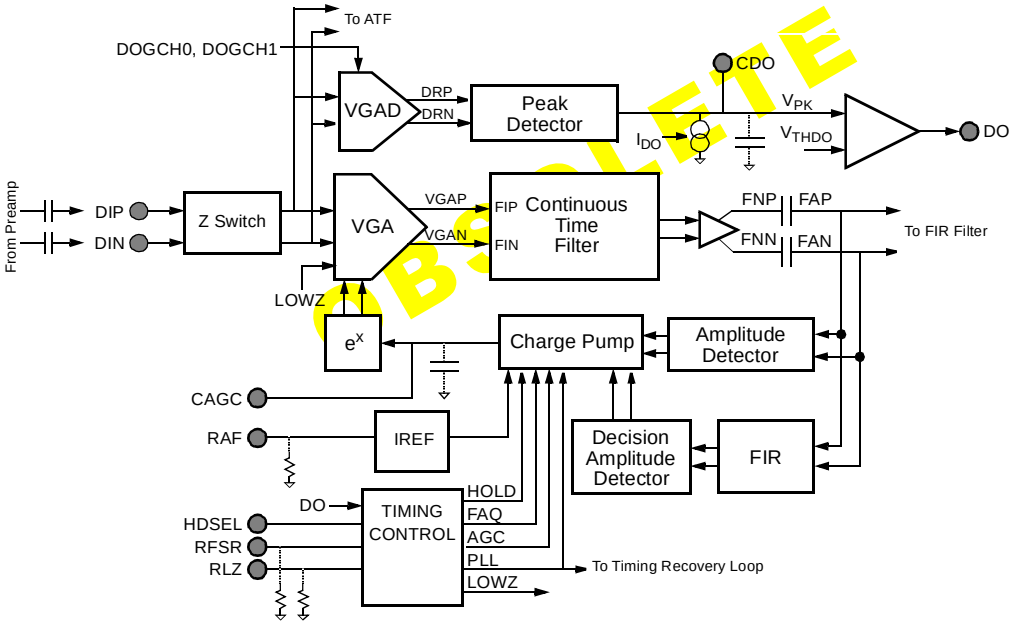

Figure 125 Gain Control Block Diagram

Test modes are provided in which the filter outputs, FNP/FNN, the VGA inputs and outputs, DIP/DIN, VGAP/VGAN, and the dropout detector outputs DRP/DRN, are multiplexed to the TP2P/TP2N output pins.

The analog AGC loop consists of the VGA, programmable continuous time filter (CTF), amplitude detector, exponentiator, and an external capacitor C_{AGC} charged by a dual rate charge pump for fast transient recovery. Charge (or decay) currents increase the capacitor voltage V_{CAGC} and increase the VGA gain while discharge (attack) currents lower the capacitor voltage V_{CAGC} and reduce the VGA gain. The magnitude of the charge pump currents are controlled by various timing signals and DAC settings. In general when a new track of data is read the part enters a fast acquisition mode (FAQ) where the loop enters a continuous AGC mode and the charge pump currents take on high (fast) values to increase the loop gain and reduce lock time. After a time-out period T_{FSR} set by external resistor R_{FSR} the loop enters a normal continuous AGC mode and the charge pump currents take on low or normal values. After another time-out period set by an internal counter counting a programmable number of clock periods, the loop switches into a sampled high gain mode and the charge pump currents are set to their sampled high gain values. Finally a second clock-period counter switches the loop into a sampled low gain mode with a set of sampled low gain currents. Figure 126 and Figure 127 show the timing for the AGC loop and Table 181 shows the various charge pump currents referred to in the following discussion.

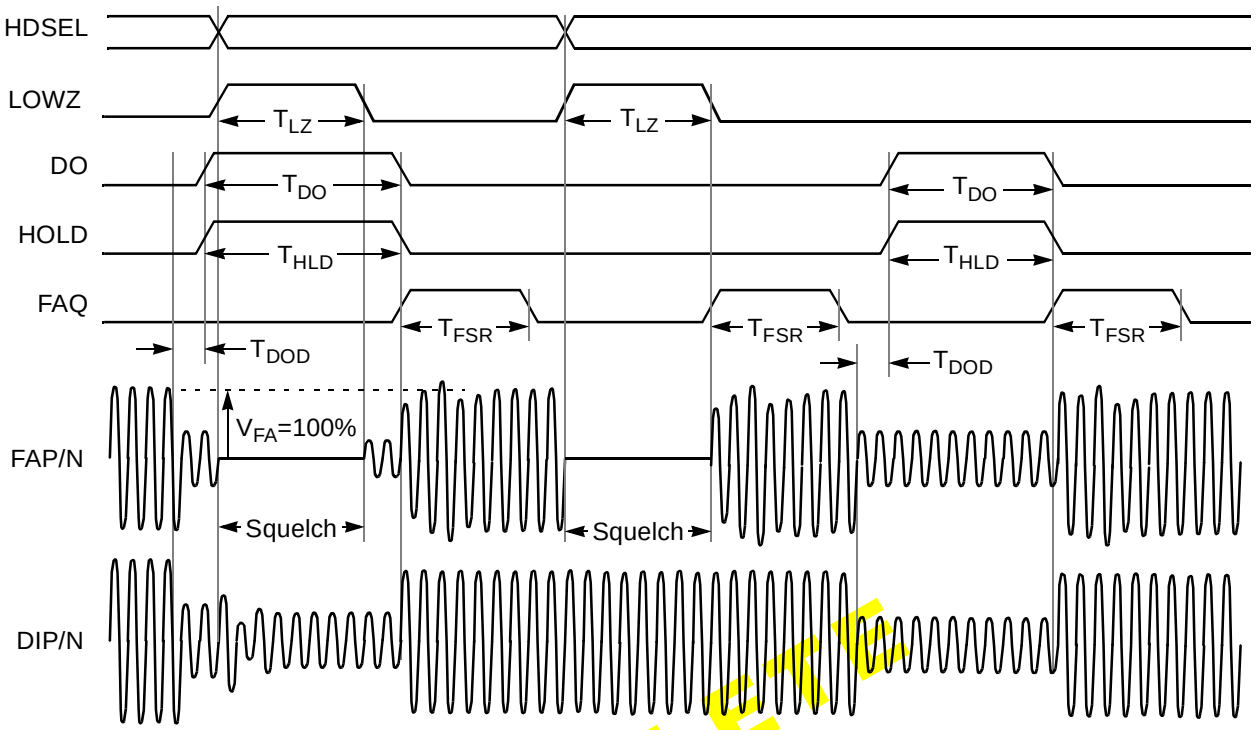

Figure 126 Read Mode AGC Timing Diagram, RG=1

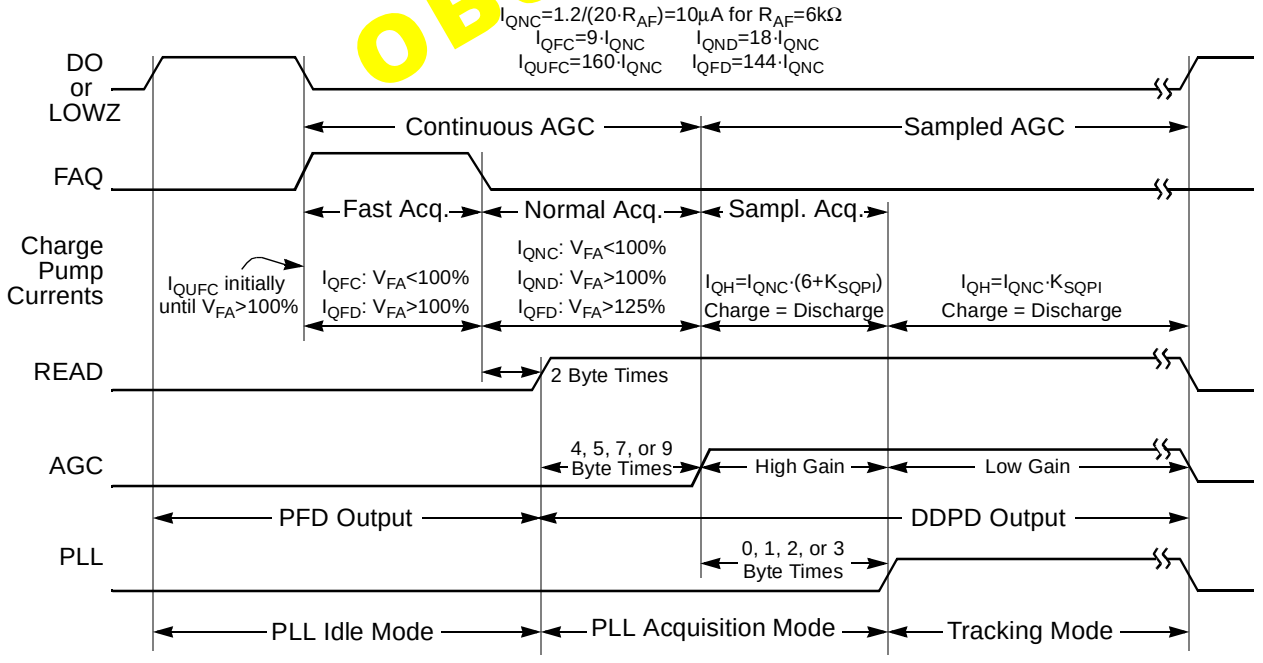

Figure 127 Read Mode Timing Diagram, RG=1

Table 181AGC Charge Pump Operation

Mode	*AGC Loop*	*Event*	*TFAQ*	*DHBW*	*SQPI*	*Discharge Current*	*Charge Current*
LOWZ	HOLD	HDSEL ⌐X¬	X	X	XX	0	0
HOLD	HOLD	HLD=1	XX	XX	XX	0	0
Fast Acq.	Continuous High BW	DO ⌐\ V_{FA}<100% initially	X	0	XX	0	$I_{QUFC}=160 \cdot I_{QNC}$
		V_{FA}>100%	X	0	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
		V_{FA}<100%	X	0	XX	0	$I_{QFC}=9 \cdot I_{QNC}$
	Continuous Low BW	V_{FA}<100 initially	X	1	XX	0	$I_{QUFC}=160 \cdot I_{QNC}$
		V_{FA}>100%	X	1	XX	$I_{QND}=18 \cdot I_{QNC}$	0
		V_{FA}>125%	X	1	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
		V_{FA}<100%	X	1	XX	0	$I_{QNC}=1.2/(20 \cdot R_{AF})$
Normal Acq.	Continuous	FAQ ⌐\ V_{FA}<100%	0	X	XX	0	I_{QNC}
		V_{FA}>100%	0	X	XX	$I_{QND}=18 \cdot I_{QNC}$	0
		V_{FA}>125%	0	X	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
Sampled Acq. (HIgh Gain)	Sampled	AGC ⌐/¬	X	X	00	$I_{QH}=6 \cdot I_{QNC}$	$I_{QH}=6 \cdot I_{QNC}$
					00	$I_{QH}=7 \cdot I_{QNC}$	$I_{QH}=7 \cdot I_{QNC}$
					01	$I_{QH}=8 \cdot I_{QNC}$	$I_{QH}=8 \cdot I_{QNC}$
					10	$I_{QH}=9 \cdot I_{QNC}$	$I_{QH}=9 \cdot I_{QNC}$
Tracking (Low Gain)	Sampled	PLL ⌐/¬	X	X	00	0	0
					01	$I_{QL}=I_{QNC}$	$I_{QL}=I_{QNC}$
					10	$I_{QL}=2 \cdot I_{QNC}$	$I_{QL}=2 \cdot I_{QNC}$
					11	$I_{QL}=3 \cdot I_{QNC}$	$I_{QL}=3 \cdot I_{QNC}$

For the normal continuous AGC mode the normal charge current I_{QNC} charges C_{AGC} for V_{FA} < 100% of the target value. The value of I_{QNC} is set by an external resistor connected between the RAF pin and VEE1, given by the following equation

$$I_{QNC} = \frac{1.2V}{20 \cdot R_{AF}} \qquad \textit{(eq. 92)}$$

R_{AF} also sets the continuous time filter cutoff frequency. For a data rate of 41.85MHz, R_{AF} should be set to 6kΩ. This will yield an I_{QNC} of 10µA. C_{AGC} should be set to 820pF nominally.

If 100% < V_{FA} < 125% the normal discharge current I_{QND} is active which equals18X the normal charge current as given by

$$I_{QND} = 18 \cdot I_{QNC} \qquad \textit{(eq. 93)}$$

For R_{AF}=6kΩ I_{QND}=180µA. The normal attack rate is thus 18X the normal decay rate. If V_{FA} > 125%, a fast discharge current I_{QFD} is active which equals 8X the normal discharge current, or 144X the normal charge current. I_{QFD} is given by

$$I_{QFD} = 8 \cdot I_{QND} = 144 \cdot I_{QNC} \quad \textit{(eq. 94)}$$

The fast attack rate is thus 144X the normal decay rate. For R_{AF}=6kΩ I_{QFD}=1.44mA.

In the fast acquisition mode the charge current is increased to 9X times its normal value and the discharge current is forced to its fast value for all values of V_{FA} > 100%, not just those >125%

$$I_{QFC} = 9 \cdot I_{QNC} \quad \textit{(eq. 95)}$$

For R_{AF}=6kΩ I_{QFC}=90µA. In addition there is an “ultra fast” charge current I_{QUFC} equal to 160X the normal charge current. I_{QUFC} is active only on the initial charge up in the fast acquisition mode. Once V_{FA} has exceeded 100%, I_{QUFC} is disabled and if V_{FA} drops back below 100%, the fast charge current I_{QFC} will be active

$$I_{QUFC} = 160 \cdot I_{QNC} \quad \textit{(eq. 96)}$$

A read cycle can be initiated in one of three ways: A positive transition on RG, a positive or negative transition on HDSEL while RG=’1’, or a negative transition on DO while RG=’1.’ A timing diagram for the AGC read cycle in read mode (pin RG=’1’) is shown in Figure 126. The read cycle is initiated by a negative transition on the DO output indicating that a dropout in the data has been detected by the dropout detector (see Dropout Detector). A data dropout occurs between tracks when either the scanner wraps around from the end of one track to the beginning of another during normal play mode, or when scanning across tracks during a fast forward or rewind “trick” mode (see Figure 145 for an illustration of the scanner and heads). During normal play mode there is typically a head switch during the dropout indicated by a polarity change on the HDSEL input pin. To avoid transients associated with the head switch from being injected into the part, the part is put into a “LOWZ” mode where the VGA gain is squelched to 0 and the input impedance is reduced by 10X. An internal one-shot signal LOWZ defines the LOWZ mode and is initiated each time HDSEL is switched. The width of this pulse T_{LZ} is set by an external resistor, R_{LZ}, connected between pins RLZ and VEE1 as given by

$$T_{LZ} = 0.075 \cdot R_{LZ} \quad \textit{(eq. 97)}$$

where R_{LZ} is measured in kΩ and T_{LZ} in µs.

R_{LZ} should nominally be set to 20kΩ which sets T_{LZ} to 1.5µs. After LOWZ goes low the input impedance is returned to its normal level and the VGA gain is no longer squelched. A second VGA followed by a peak detector is used to detect dropouts in the input data, as occur between tracks or at the beginning or end of a track (see Dropout Detector).

When a dropout is detected, the DO output is switched high and the charge pump output is disabled causing the C_{AGC} capacitor to hold its voltage. When the dropout detector detects normal data levels, DO switches low and the charge pump output is again enabled, allowing the loop to reacquire lock to the new data, using the held C_{AGC} voltage as an initial condition. The loop then normally enters the fast acquisition mode (FAQ) where the “ultra fast” charging current I_{QUFC} increases the VGA gain at 160 times the normal decay rate until V_{FA} exceeds 100% of the target value. Thereafter, the loop response is determined by the fast charging current I_{QFC} and the fast discharging current I_{QFD}. External resistor R_{FSR} sets a time-out period T_{FSR} after which the loop will automatically switch back to the normal mode. T_{FSR} is given by

$$T_{FSR} = 0.075 \cdot R_{FSR} \quad \textit{(eq. 98)}$$

where R_{FSR} is measured in kΩ and T_{FSR} is in µs.

R_{FSR} should nominally be set to 20kΩ which sets T_{FSR} to 1.5µs. If HDSEL is switched at a time other than during a dropout, the FAQ mode will be initiated on the falling edge of LOWZ, as shown in the middle sequence of Figure 126. Also shown is the case where a dropout occurs without a HDSEL switch where the C_{AGC} voltage is held and a fast acquisition sequence is initiated, but there is no LOWZ condition. Only a transition on HDSEL will create a LOWZ condition, but the FAQ mode and subsequent read cycle occurs with either the falling edge of LOWZ or the falling edge of DO.

If control register bit TFAQ is set to a ‘1’, the loop will stay in the fast acquisition mode, ignoring the FAQ pulse and not switching to normal mode until TFAQ is set to a ‘0’. This is to facilitate testing of the fast acquisition mode. If serial register bit DHBW (disable high bandwidth) is set to a ‘1’, the FAQ mode still charges initially at the “ultra fast” rate, but then switches to the normal charge and discharge currents (or fast discharge current if V_{FA} > 125% of the target value as described above) immediately without waiting for FAQ to go low, thus effectively eliminating the fast acquisition (or high bandwidth) mode. Another test bit HLD when set to a ‘1’ forces the charge pump into a hold mode.

The sampled AGC loop consists of the VGA, programmable continuous time filter, sampling 7-tap FIR equalizer, decision amplitude detector and charge pump, and exponentiator. Symmetrical charge and discharge currents are utilized in the sampled mode. A sample is considered a ‘1’ if its amplitude exceeds 50% of $0.71 \cdot V_{FA}$ otherwise it is a ‘0’. Sampled 0’s are ignored by the loop, while sampled 1’s charge C_{AGC} if the sample is below $0.71 \cdot V_{FA}$ and discharge C_{AGC} if the sample exceeds 0.71 V_{FA}. The magnitude of the charge and discharge currents are equal and take on a value of I_{QH} in the high gain, or acquisition, mode; and I_{QL} in the low gain, or tracking, mode.

A negative transition on DO initiates an acquisition sequence where the AGC and timing recovery loops eventually switch into a sampled mode. An acquisition counter begins on the falling edge of FAQ as shown in Figure 127. An internal READ signal is generated after 16 periods of the timing recovery VCO have elapsed. The 16 periods are referred to as two bytes times, since that is the amount of data read in this time period if the timing recovery loop were to be already locked. The AGC loop transition into high gain sampled mode and the PLL transition into tracking mode are based on two programmable sync field counters, the AGC SF counter and the PLL

SF counter respectively, which are started when READ transitions high. The AGC SF count is determined by one of four programmable counts of 4, 5, 7, or 9 byte times. The AGCSFC 2-bit word in the control register sets the byte count, and after counting the proper number of VCO clock cycles, internal signal AGC transitions high and the AGC loop switches into sampled mode with the charge pump in the high gain mode (see Dropout Detector). Similarly, the PLL SF count is programmed by the 2-bit PLLSFC control register word to 0, 1, 2 or 3 byte times following the AGC SF count at which time Internal signal PLL goes high. At this time the sampled AGC charge pump switches to the low gain mode. The PLL transitions from idle to acquisition mode when READ goes high. The PLL remains in acquisition mode through the sum of both the AGC SF and PLL SF counts, whereupon, it transitions into the tracking mode. Table 182 shows the sync field counts corresponding to each AGCSFC and PLLSFC value.

Table 182Sync Field Counts

AGCSFC	*AGC Sync Field Byte Count*
00	4
01	5
10	7
11	9

PLLSFC	*PLL Sync Field Byte Count*
00	0
01	1
10	2
11	3

The sampled charge pump currents I_{QL} and I_{QH} are controlled by the SQPI(1:0) control register bits whose value is represented as K_{SQPI} and varies from 0 to 3.

$$I_{QL} = I_{QNC} \cdot K_{SQPI} \quad \textit{(eq. 99)}$$

$$I_{QH} = I_{QL} + 6 \cdot I_{QNC} = I_{QNC} \cdot (6 + K_{SQPI}) \quad \textit{(eq. 100)}$$

So, for R_{AF}=6kΩ., I_{QL}will equal 0-30µA, and I_{QH} will be to 60-90µA. The charge pump operation for all the various AGC modes is shown below in Table 181.

The VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. The Equation (eq. 101) expresses the VGA normal mode gain (A_V), in Volts/Volts, as an exponential function of the control voltage on the selected CAGC pin where $A_{V(max)}$ is 46V/V and V_{CAGC} nominally ranges from1.4V to 2.8V.

$$A_V = A_{V(max)} \cdot e^{-\left(\frac{2.8V - V_{CAGC}}{0.53V}\right)} \quad \textit{(eq. 101)}$$

When in the PGC mode, the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the PGC control register. The VGA has a linear gain versus DAC count and is expressed by the following equation

$$A_V = 2.24 + 2.8 \cdot K_{PGC} \quad \textit{(eq. 102)}$$

where A_V is in V/V and K_{PGC} is the value of the PGC(3:0) control word which ranges between 0 and 15.

PGC mode is used primarily for test.

Dropout Detector

In parallel with the normal signal path is a separate analog signal path for detecting signal “dropouts”. The dropout detector, shown in Figure 125, consists of a variable gain amplifier (VGAD) with programmable gain followed by a peak detector with an external holding capacitor, C_{DO}, and internal decay current I_{DO}. The signal envelope, V_{PK}, is compared to a fixed threshold, V_{THDO} which equals 0.25V. V_{PK} is set via the 4-bit programmable VGAD gain and should be nominally set to 0.5V, which is 6dB above V_{THDO}. Note that both V_{PK} and V_{THDO} are single-ended peak voltages which are equal to one fourth their peak-to-peak differential equivalents. When the signal envelope decays below V_{THDO}, indicating that the input level is half its normal value, the DO pin goes high. This should only occur when the scanner switches heads between the end of one track and the beginning of another, or between tracks when in search mode. This condition is referred to as a dropout and is used to initiate a new read cycle as illustrated in Figure 127. The decay rate is determined by C_{DO} and a 2-bit programmable decay current, I_{DO}, given by

$$I_{DO} = \frac{0.12V}{R_{AF}} \cdot K_{IDO} \quad \textit{(eq. 103)}$$

where K_{IDO} is controlled by the IDO(1:0) bits in the serial control register as shown in Table 183.

R_{AF} is the value of the same external resistor that sets the AGC charge pump currents and the filter cutoff frequency.

Note that K_{IDO} is not just the decimal equivalent of IDO(1:0). With R_{AF} set to 6kΩ, I_{DO} ranges from 40-200 µA. This results in a decay time T_{DOD} which will vary with the choice of C_{DO} according to

$$T_{DOD} = \frac{(V_{PK} - V_{THDO} - 0.02) \cdot C_{DO}}{I_{DO}} \quad \textit{(eq. 104)}$$

The effect of the decay rate is to delay the DO output by an amount T_{DOD} such that if short dropouts occur before V_{PK} has decayed to V_{THDO}, a dropout will not be detected. When a dropout is detected, DO goes high, the AGC gain is held, and the PLL switches to idle mode. When the normal data levels are again detected, DO immediately transitions back to a low level without delay, and the AGC fast acquisition and PLL lock-to-data sequences are initiated. A data dropout does not squelch the VGA gain nor reduce the input impedance. This happens only during a head switch as explained in Gain Control. Table 183 shows the values of T_{DOD} vs. the IDO(1:0) DAC setting for fixed values of V_{PK}, V_{THDO}, R_{AF} and C_{DO}.

Table 183Dropout Detector Decay Time T_{DO}

IDO(1:0)	K_{IDO}(1:0)	R_{AF}	I_{DO}	V_{PK}	V_{THDO}	C_{DO}	T_{DOD}
00	2	6kΩ	40µA	0.5V	0.25V	1.6nF	10µs
01	3	"	60µA	"	"	"	8.3µs
10	5	"	100µA	"	"	"	4.0µs
11	10	"	200µA	"	"	"	2.0µs

The dropout gain is programmed via the DOGCH0 and DOGCH1 4-bit control registers. The appropriate register is selected with the head select pin, HDSEL. This allows independent programming for the different head characteristics. HDSEL selects parameters for Head0 or Head1 from one of two register banks. Setting HDSEL low selects the Head0 registers while setting HDSEL high selects Head1 registers. Parameters varied by HDSEL are the continuous time filter cutoff, group delay, boost, the dropout gain, and the ATF gain. The dropout gain is given by

$$A_V = 3.3 \cdot (1 + K_{DOGC}) \quad \textit{(eq. 105)}$$

where K_{DOGC} is the value of either the DOGCH0 or DOGCH1 register setting and varies between 0 and 15.

Av is measured in V/V, not dB.

This gain is used to calculate the value of V_{PK} given by

$$V_{PK} = 0.33 \cdot A_V \cdot V_{DI} - 0.04V \quad \textit{(eq. 106)}$$

where V_{DI} is the peak-to-peak differential input voltage and V_{PK} is the single ended peak voltage.

For a given value of V_{DI}, A_V should be chosen such that V_{PK}=0.5V, corresponding to a DRP,N VGAD output of 1.64V_{ppd}. For example with a 100mV_{ppd} input signal a DOGC setting of 4 will produce a gain of 16.5, yielding a VGA output of 1.65V_{dpp} and a V_{PK} of 0.505V. (Note the factor of 0.33 in (eq. 106). Normally to convert peak-to-peak differential to single-ended peak there is a scaling factor of 0.25. The peak detector used here actually has a gain of 1.32 and thus the 0.25 conversion is actually 0.33).

Continuous Time Low-pass Filter/Equalizer

The filter is implemented as a 7-pole, 0.05 degree linear phase, equiripple low pass continuous time filter (CTF). The cutoff frequency, boost, and DC group delay are each individually programmable.The basic building block for the filter is the integrator (g_m-C) stage which consists of a transconductance amplifier driving an on-chip capacitor. Four g_m-C stages and two capacitors interconnected as shown in Figure 128 form a biquad, which has a second order transfer function as shown in (eq. 107) below.

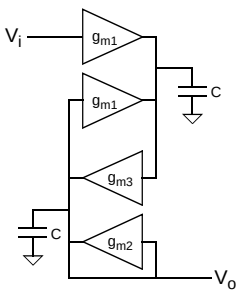

Figure 128 Biquad Block Diagram

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$$\frac{V_o}{V_i} = \frac{\omega_o^2}{s^2 + s(\omega_o/Q_o) + \omega_o^2} \qquad \text{(eq. 107)}$$

where,

$$\omega_o = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{C} \quad \text{and} \quad Q_o = \frac{\sqrt{g_{m1} \cdot g_{m3}}}{g_{m2}}$$

Three of these biquads and a single integrating gm-C stage are cascaded to form a seven-pole low pass filter as shown in Figure 129. Boost, or pulse slimming, is implemented by feeding the filter input through two variable gain (or multiplying) stages to the normally grounded terminals of the capacitors of the gm-C stage in the first and second biquads. Mathematically boost adds zeros to the overall filter transfer function which is shown in (eq. 108) below.

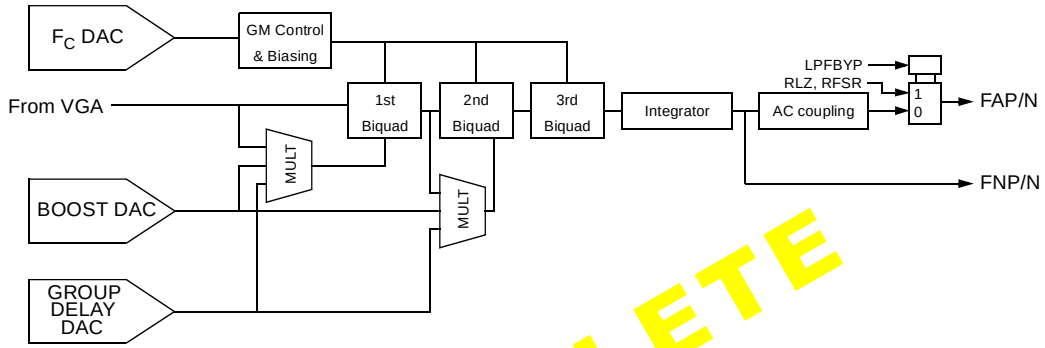

Figure 129 Filter Block Diagram

$$\frac{V_o}{V_i} = A_N \cdot \left(\frac{\omega_{01}^2 - \beta s - \alpha s^2}{s^2 + s(\omega_{01}/Q_{01}) + \omega_{01}^2}\right) \cdot \left(\frac{\omega_{02}^2}{s^2 + s(\omega_{02}/Q_{02}) + \omega_{02}^2}\right) \cdot \left(\frac{\omega_{03}^2}{s^2 + s(\omega_{03}/Q_{03}) + \omega_{03}^2}\right) \cdot \left(\frac{\omega_{04}}{s + \omega_{04}}\right) \qquad \text{(eq. 108)}$$

where, A_N = -3.2dB, $\omega_0 = 2\pi f_C$,

f_C = programmable filter cutoff frequency (FCH1, FCH0)

α = programmable symmetric zero coefficient (BSTH1, BSTH0)

β = programmable asymmetric zero coefficient (GDH1, GDH0)

$\omega_{01} = 1.148 \cdot \omega_0$, $Q_{01} = 0.681$

$\omega_{02} = 1.718 \cdot \omega_0$, $Q_{02} = 1.114$

$\omega_{03} = 2.317 \cdot \omega_0$, $Q_{03} = 2.022$

$\omega_{04} = 0.861 \cdot \omega_0$

Note that the filter has an attenuation factor of -3.2dB. The filter output is coupled to the FIR filter and full-wave rectifier through on-chip coupling capacitors to reduce the effect of offsets in the filter as shown in Figure 124. The low frequency pole associated with the coupling capacitors is set nominally to 20kHz.

Cutoff frequency is controlled by one of two continuous time filter f_C DAC's and a current set by the external R_{AF} resistor. The control word for the DAC is read from either the FCH0 or FCH1 register depending on the value of HDSEL. Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation

$$f_C = (0.15 \cdot K_{FC} + 5.0) \cdot \frac{6}{R_{AF}} \qquad \text{(eq. 109)}$$

where K_{FC} is the value of either the FCH0(5:0) or FCH1(5:0) control words and ranges between 0 and 63, and

R_{AF} is kΩ. (R_{AF} is the same external resistor that sets the Gain Control charging currents.)

Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM65011 group delay

flatness is specified to be less then 4% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 46ns at a cutoff of 10MHz. Thus at this cutoff frequency, the group delay varies by less than 2ns out to 20MHz. A typical group delay is shown in Figure 130.

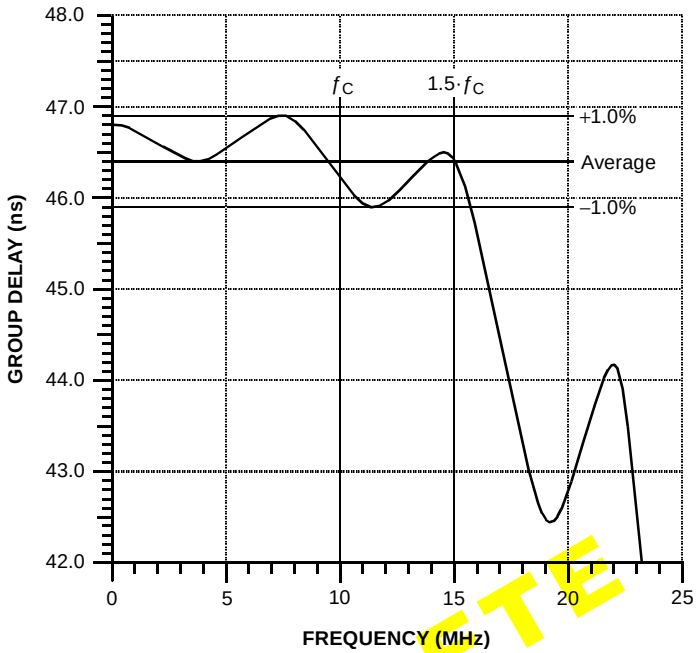

Figure 130 Typical Group Delay of AGC and Filter (with f_C = 10MHz)

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay T_{GD}, in nanoseconds, is expressed as (eq. 110)

$$T_{GD} = \left[3 + \frac{434}{f_C}\right] \text{ns} \qquad \textit{(eq. 110)}$$

where f_C is the filter cutoff frequency in MHz.

A graph of (eq. 110) is shown in Figure 131.

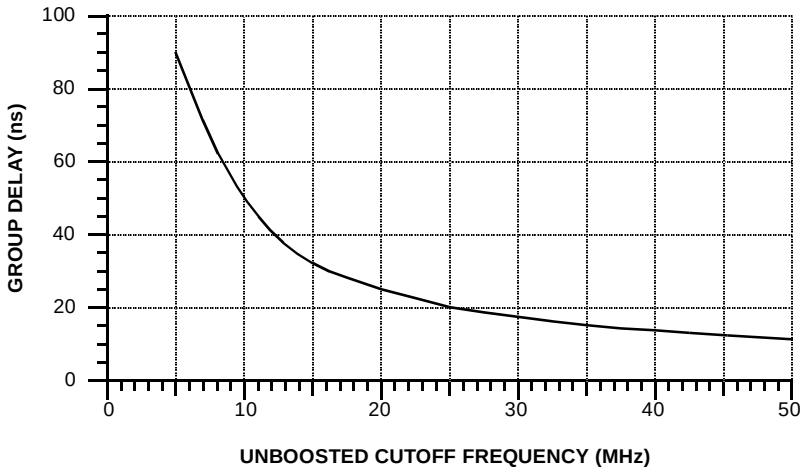

Figure 131 Typical Group Delay vs. Cutoff Frequency

Setting the desired boost through the boost control register bits (with the group delay register set to zero) produces symmetric zeros on the real axis (α in (eq. 108)). This maintains the constant group delay as in the no-boost case. The amount of boost equalization depends on the value output of either the BSTH0(4:0) or BSTH1(4:0) control register words, depending upon the value of HDSEL.

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Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function. Figure 132 shows two normalized filter response curves, one with no boost and the other with maximum boost. Shown are the unboosted and boosted cutoff frequencies and the frequency where the filter response peaks, defined as the gain peak frequency, f_{peak}. Figure 133 shows the nominal relationship between the BST control word and the resulting boost level relative to the DC level. Notice the absence of peaking when BST is below 8. In this region the bandwidth is pushed out but the gain doesn't peak above the DC level.

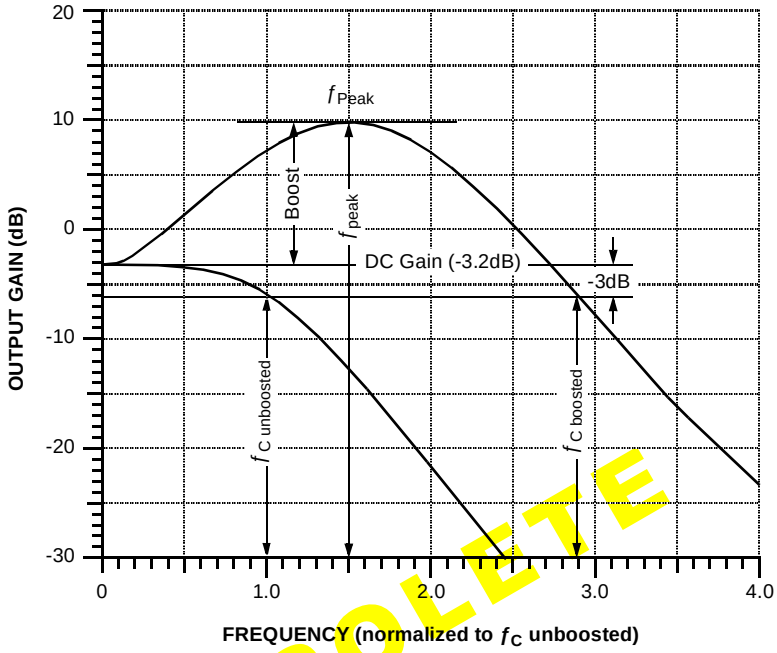

Figure 132 Normalized Filter Frequency Gain, Boosted & Unboosted

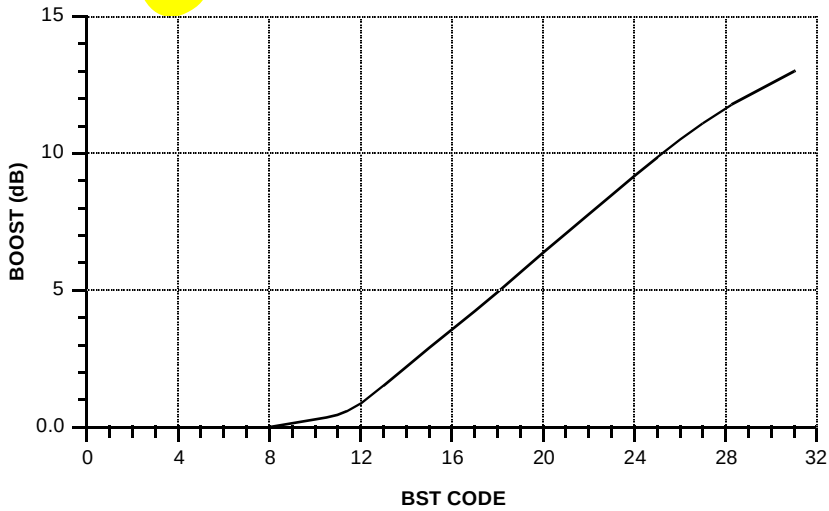

Figure 133 Filter Boost Control

Figure 134 shows the effect of boost on the cutoff frequency. With maximum boost the cutoff frequency is over triple the unboosted value. Also shown is the gain peak frequency, f_{peak}, which for maximum boost achieves a value of over 1.5 that of the unboosted response. Figure 135 displays the same data as Figure 134 plotted against the resultant boost value rather then the DAC code.

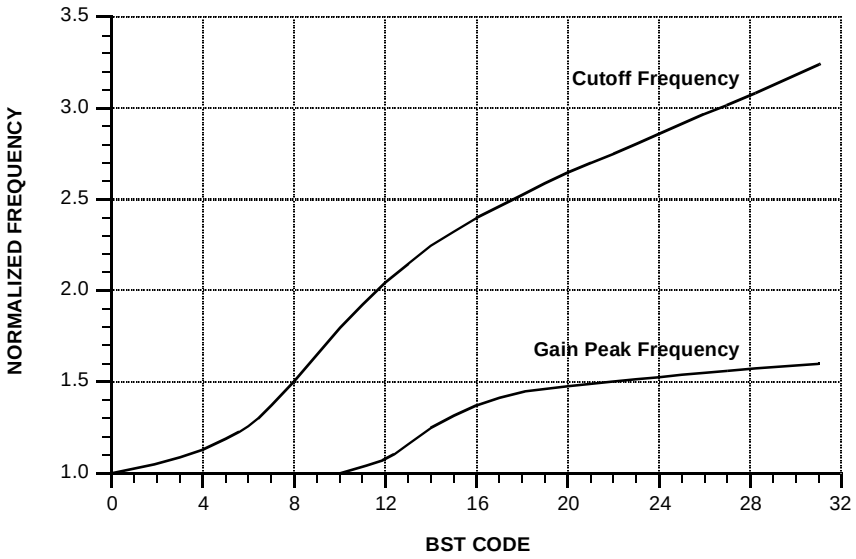

Figure 134 Normalized Cutoff and Gain Peak Frequencies vs. Code

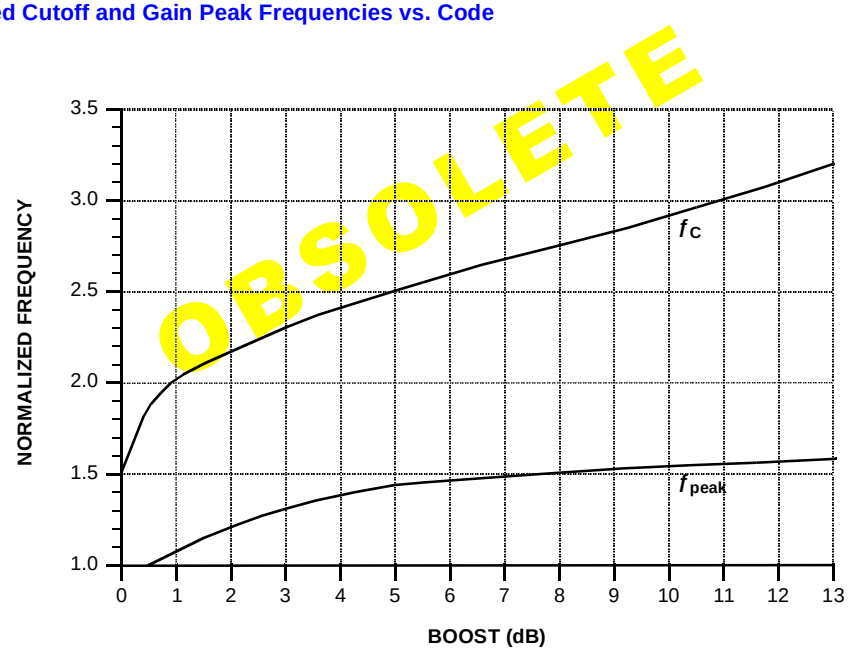

Figure 135 Normalized Cutoff and Gain Peak Frequencies vs. Boost

Group delay can be varied by ±30% from the symmetric zero condition via control DACs in the serial control register. There are two sets of group delay DAC register bits, GDH0(5:0) and GDH1(5:0), corresponding to each head chosen via the HDSEL pin. The group delay registers can be used to produce asymmetry in the zeros causing the group delay to vary with frequency (β in (eq. 108)). This can be desirable to compensate for asymmetry in the heads/media components. The group delay registers are six bits wide and are represented in two's complement format. A code of +31 corresponds to a DC shift in group delay of +30%; a code of -32 corresponds to -30% shift in DC group delay. The percent shift in DC group delay can be expressed as

$$\frac{\Delta T_{GD}}{T_{GD_0}} \times 100 \;=\; 0.95 \cdot K_{GD} \qquad \textit{(eq. 111)}$$

where K_{GD} is the value of the 6-bit GDH0 or GDH1control word.

The boost is held nearly constant as group delay is varied. This is accomplished by moving one zero in and the other zero out in frequency an equal amount. At zero boost, the zeros are at ±∞. Therefore it is impossible to move one out as one is moved in. In this extreme case, it can be seen that the identical unboosted transfer characteristic cannot be maintained as group delay is varied. Figure 136 shows the effect on group delay of programming the group delay register to zero and to the two extremes, and Figure 137 shows the effect on the magnitude response as the group delay register value varies over extremes and under several boost conditions.

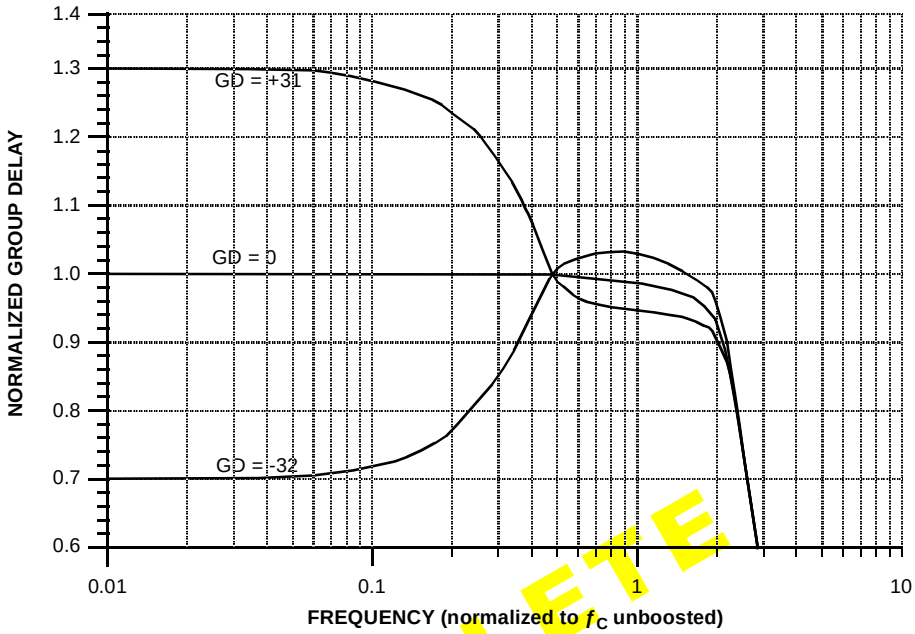

Figure 136 Normalized Group Delay (max f_C, max boost)

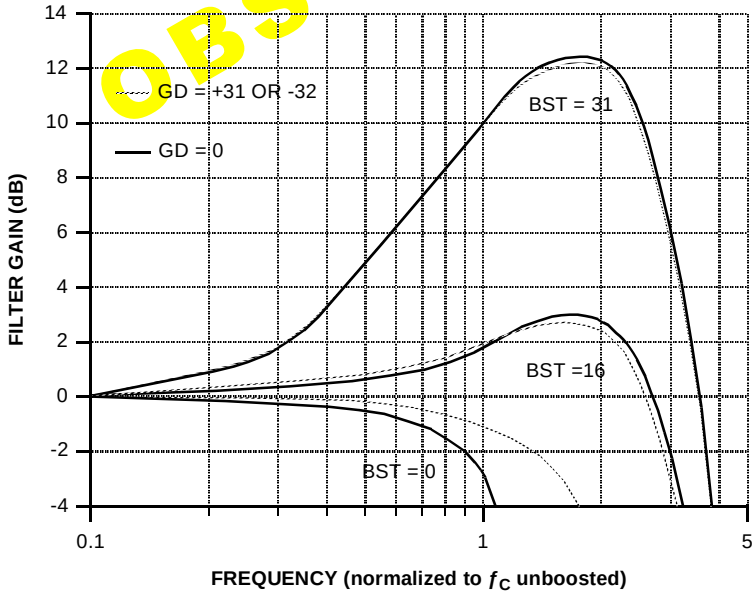

Figure 137 Gain Variations with Different Boost and Group Delay Settings

A test feature exists in the filter where a differential signal may be applied to the RLZ and RFSR input pins which can be input in place of the AC coupled filter output. Control register bit LPFBYP (Low Pass Filter BYPass) when set to a '1' controls this output test MUX, as shown in Figure 129. The voltage level on both RLZ and RFSF should be kept above 2V to insure that the normal RLZ and RFSR bias circuitry remains off.

FIR Filter/Equalizer

The FIR is a five tap transversal filter with independently controllable tap weights. Independent control provides both gain and phase adjustment of the input signal. The tap weights must be directly programmed into the serial registers' weight vector locations designated FIR0 through FIR4, which set tap weights K_0-K_4 respectively. Taps 1 and 3 have two register each, one for each head. The HDSEL pin selects the appropriate register. HDSEL='0' will select registers FIR1H0 and FIR3H0 for FIR1 and FIR3, and HDSEL='1' will select registers FIR1H1 and FIR3H1 for FIR1 and FIR3. Taps 0, 2, and 4 are fixed for both heads.

As with any sampled system the response is periodic in the frequency domain. The center tap provides a flat response over frequency. The inner set of taps adjacent to the center tap produce a periodic response that is sinusoidal in shape and repeats at multiples of the sampling frequency. The sampling frequency in this situation is the channel data rate. The outer set of taps, two delays away from the center tap, are periodic at half the sample frequency. The general frequency response for a given set of taps is given by

$$(e^{j\omega T}) = (K_{-n} + K_n)\cos(n\omega T) + j(K_{-n} - K_n)\sin(n\omega T) \qquad \textit{(eq. 112)}$$

Where n is the count away from the center tap,

K_n is the gain of preceding taps, and

K_{-n} is the gain of past taps.

The T term is the channel sample interval.

This is the ideal response for a single set of taps.

The net response for all the taps is the sum of each pair and the center tap is shown below:

$$He^{j\omega T} = H_0 e^{j\omega T} + H_1 e^{j\omega T} + H_2 e^{j\omega T} \qquad \textit{(eq. 113)}$$

The Figure 138 illustrates the possible gain variations achievable when symmetric taps are swept together over their allowable ranges, as listed in Table 184.

The H_0 term provides only a flat frequency response with varying values of gain. The gain response also includes finite bandwidth characteristics of the sampler. The sampler bandwidth is about 120 MHz and will have some effect on the frequency characteristics. The ideal gain limits for the taps are shown below.

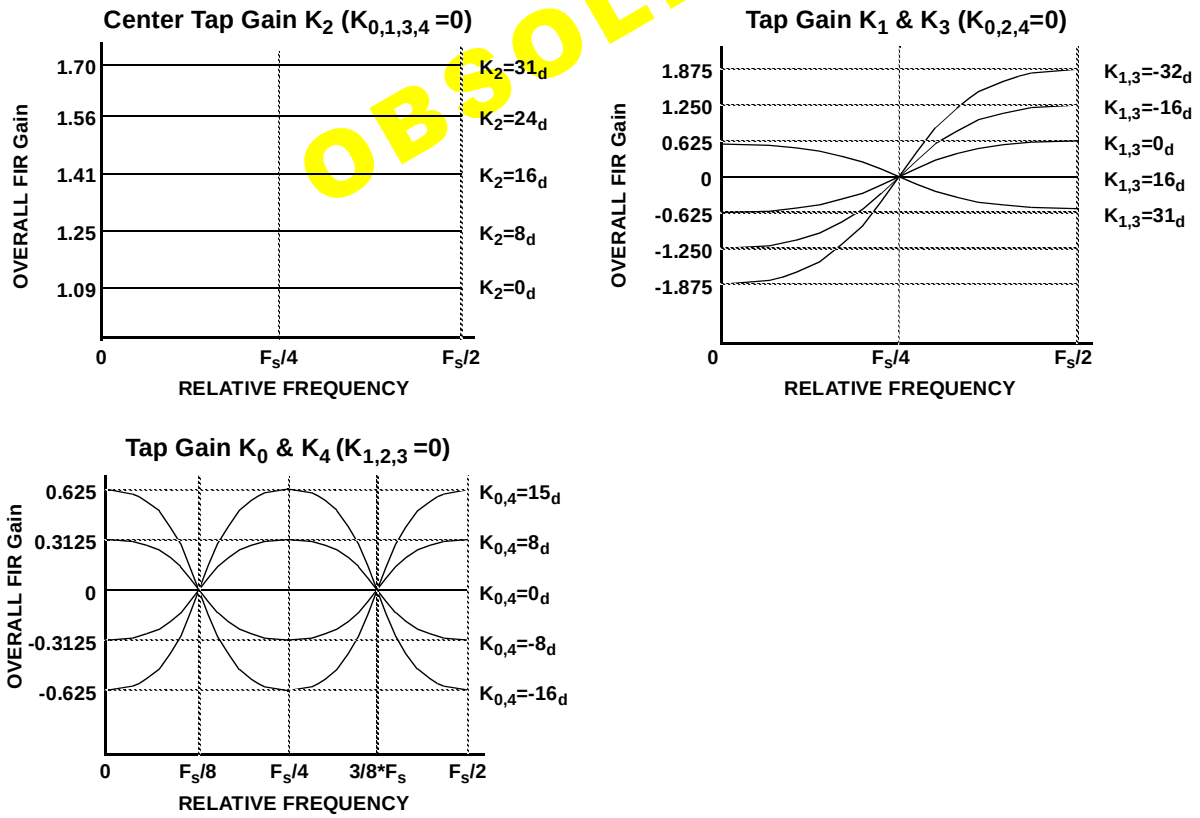

Figure 138 FIR Symmetric Tap Frequency Response Curves

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Table 184 FIR Tap Gain Settings

Tap	K_0	K_1	K_2	K_3	K_4
Gain Range	-0.312 0.293	-0.9375 +0.293	+1.09 +1.70	-0.9375 +0.293	-0.312 +0.293
Actual bits	5	6	5	6	5
Eff. bits	7	7	7	7	7
Resolution	(1/64)·1.25=19.56mV/V				

FIR Adaptation Circuit

An adaptive system of any kind consists of a plant that performs some function (process, filter, etc.), a means of determining the performance of the plant, and an algorithm used to adjust the plant's controls. The FIR Adaptation block uses a decision-directed error metric to quantify the system performance and a sequential binary Least Mean Squared (LMS) adaptation algorithm to adjust the tap weights. In this system the plant is the FIR and the plant controls are the outer tap weights. The center tap weight is not adjusted because it primarily controls the DC gain of the equalizer and that function is taken care of by the AGC block.

Determining the performance of the equalizer can be done by subtracting the output of the FIR from the ideal PR4 data. This can be done if a known data pattern has been written to the disk or the ideal data has been externally supplied to the part. This adaptation circuit uses a decision-directed technique that estimates the ideal data stream from the actual data. A target response is generated from the data by quantizing the output of the FIR into three levels. Three levels are appropriate for a partial response system equalized for the PR4 response shape. In a PR4 system any single transition on the disk produces interference with one adjacent transition in a way that will produce three distinct voltage levels. After the FIR output has been quantized, the appropriate ideal voltage value (+1, 0, -1) can then be subtracted from the output, which generates an estimate of the error signal. Decision- directed systems work well as long as the initial errors are not too large. One case that will cause divergence in the tap weights is when the amplitude is half or below half of what it should be. In this case all the weights converge toward zero. For more realistic cases convergence is not a problem. The system has been shown to converge for a signal containing Lorentzian step response shapes with densities as high as 4bits/pw50 with the initial outer taps set to zero.

The LMS adaptation algorithm is a very robust technique for minimizing the magnitude of the errors produced by a system with respect to a target response. In such a system all the weights are adjusted for each output bit of the channel. The algorithm iteratively adjusts each tap weight in the direction that would reduce the FIR output error based on the value held in its associated tap. This is done by multiplying the FIR output error by the value held in a given tap. For example, when the output is larger than the ideal positive output and the sample held at a given tap is positive, its gain would be decreased, and this would have the effect of reducing the error in that instance. The basic tap weight update recursion is defined by:

$$\vec{W}_K = \vec{W}_{K-1} + 2 \cdot \mu \cdot \varepsilon_{K-1} \cdot \vec{C}_{K-1} \qquad \textit{(eq. 114)}$$

The terms W_{K-1} and C_{K-1} are 5-element vectors with W_{K-1} containing the tap weights of the FIR and C_{K-1} containing the sample values held at each tap of the FIR. μ is a gain term which sets the overall loop gain of the adaptive feedback system, and ε_{K-1} is the error in the output of the FIR at the current time "K-1" which is computed by

$$\varepsilon_{K-1} = d_{K-1} - Y_{K-1} \qquad \textit{(eq. 115)}$$

The d_{K-1} term is the ideal data at the time "K-1" and Y_{K-1} is the FIR output at that time. When decision-directed adaptation is employed, d_{K-1} is replaced by an estimate of the ideal data (+1, 0, -1).

The procedure that is employed by this circuit is a modification of the basic LMS concept. It maintains many of the key features and yet greatly reduces implementation complexity in order to minimize power consumption and die area. The basic approach is to incrementally adapt one weight at a time, based on an average of several LMS update samples, and then repeat this process for each successive weight in a cyclic fashion for a complete read cycle. In this system there is a digitally controlled FIR and the tap weights can only be adjusted in discrete steps, one bit at a time. This sets μ for the part at the value of one LSB which equals 0.0195. The multiplication of the tap values with the output errors is replaced by a binary multiplication. The sign of that operation indicates whether to increment or decrement the tap weight. Averaging the individual updates is used to prevent instabilities and a dead zone is used to reduce the amount of tap weight wander once the steady state values have been reached. An option is available to force symmetrical tap weight adaptation to prevent timing recovery/FIR interactions.

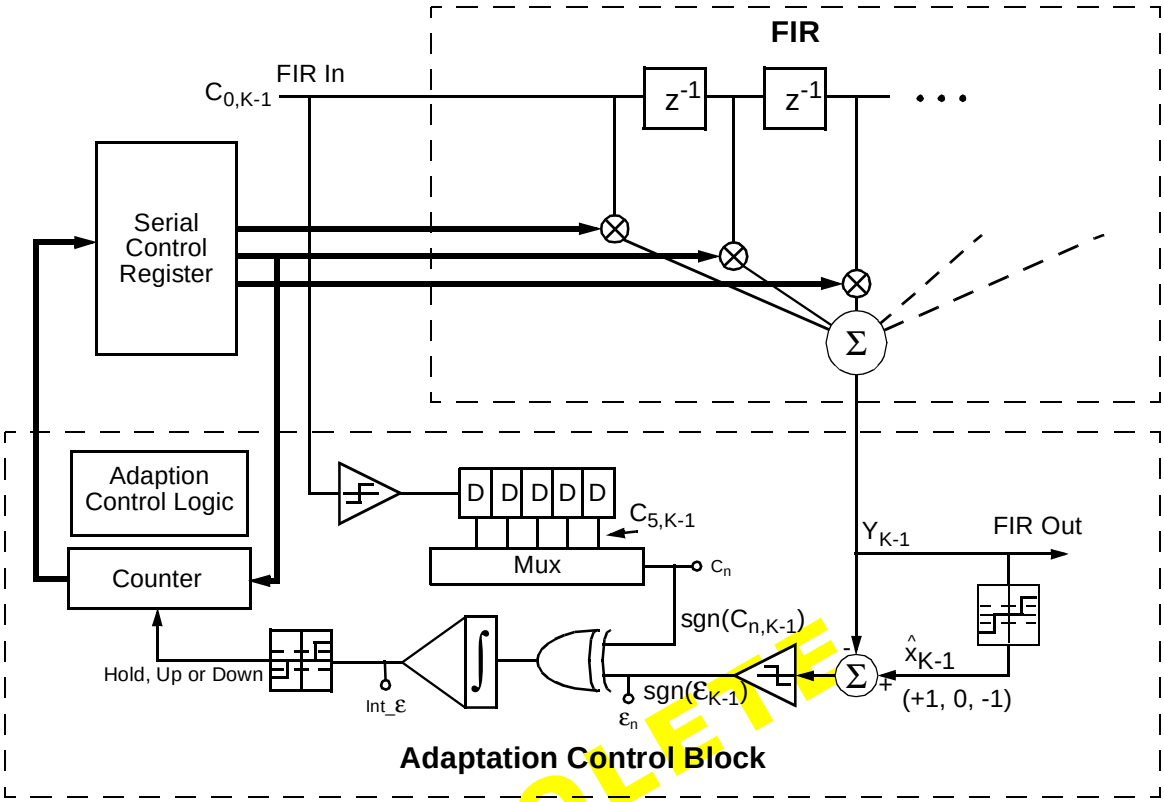

Figure 139 Sequential Binary Least Mean Squared Adaptation

The final adaptation equation becomes

$$\vec{W}_K = \vec{W}_{K-1} + \left(Q_{(1,0,-1)} \left(\frac{\sum_{J=1}^{N} sgn(\varepsilon_{K-1+J}) \cdot sgn(\vec{C}_{K-1+J})}{N} \right) \times lsb \right) \quad \textit{(eq. 116)}$$

The adaptation process starts after a read operation has been initiated and the internal READ signal has gone high (see Figure 127 on page 8). At this time the initial tap weight address is loaded into an address counter. When the internal PLL signal goes high, indicating that the timing recovery loop has transitioned from acquisition to tracking mode, the first tap weight value is loaded into an up/down counter and the averaging process begins. Once the integration time has been reached, the tap update command is latched. The current tap weight is processed and then written back to the serial register. The tap weight address counter is incremented and the next tap weight is loaded. This process continues until a READ cycle ends either through the deassertion of RG, the detection of a dropout, or a transition on HDSEL. It should be noted that since the part is accessing the serial registers during adaptation, the user should NOT attempt any serial register operation while RG is asserted (and DO is low) and the AE bit set.

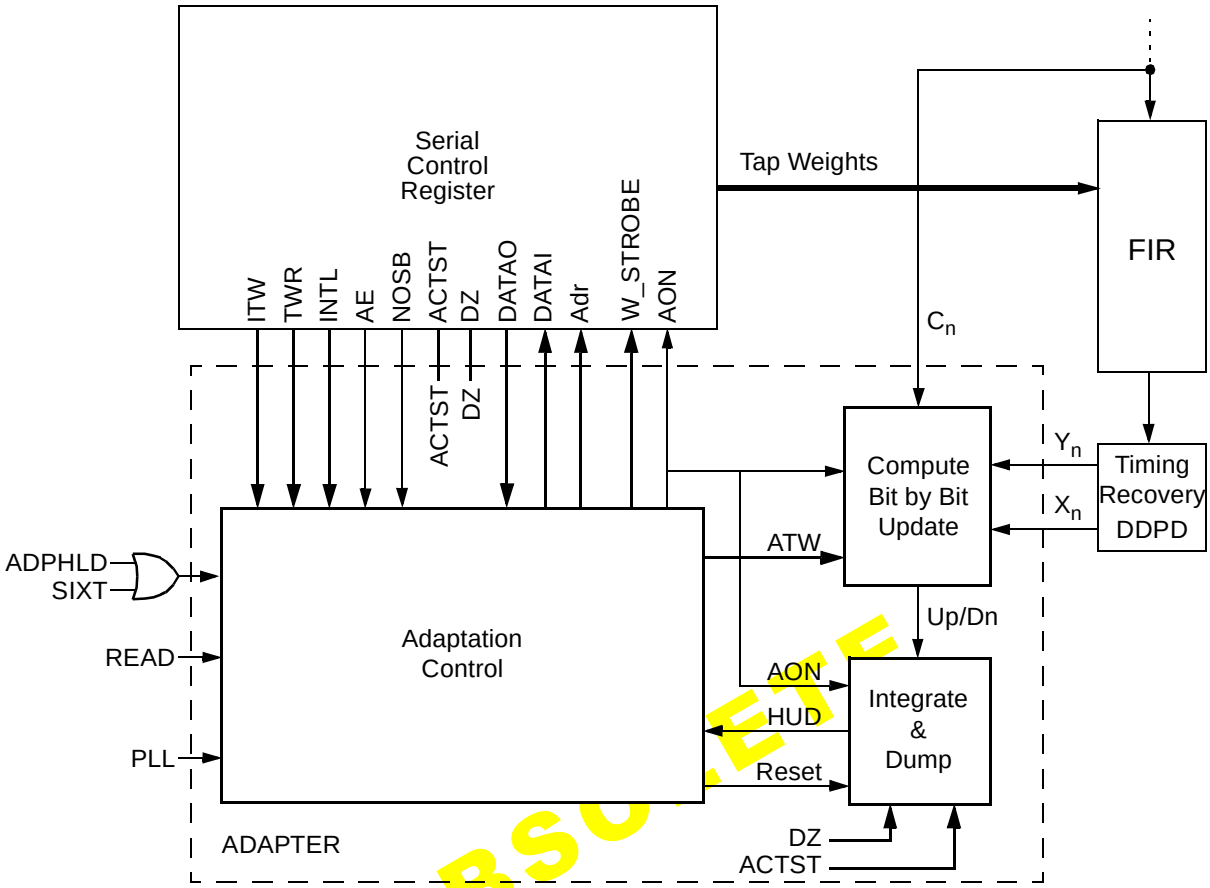

Figure 140 Self adaptation circuitry

Key Features of the Adaptive FIR Filter

Adaptation Control Test: ACTST

Two bit control for the output of the integrator that forces either an up, hold, or down count. This is primarily a test feature for the adaptation control logic. '00' specifies normal operation, '01' specifies an UP count, '10' a DOWN count, & '11' specifies hold. The ADPHLD external pin when set to a '1' will force ACTST into state '11' allowing the user to hold the adaptation and freeze the tap weights at their current values without having to write through the serial register.

Adaptation Enable: AE

When set to a '1' the AE control register bit enables the adaption circuitry. It can not be modified during an adaptation read cycle.

Dead Zone: DZ

Two bit control that specifies the adaption threshold. With ideal tap weight settings, the adaption algorithm will randomly integrate the error signal up and down. Without a dead zone, the tap weights would be changing continuously. The dead zone DAC allows a programmable window inside of which no weights are adapted. Only if there is a net integration in one direction exceeding a programmable threshold, will the tap weight update. The threshold is set in a symmetrical manner as a percentage of the integration length. A DZ value of '00' sets the threshold equal to 35% of the integration length. For example with an integration length of 12 and a DZ value of '00', the tap weight will not adapt unless there is a net up or down integration for at least 4.2 clock cycles. A value of '01' sets a 50% threshold (6 clock cycles with INTL set to 12), '10' sets a 65% threshold (7.8 clock cycles), and '11' sets an 80% threshold (9.6 clock cycles). If there aren't enough up or down commands to exceed the threshold within the integration length time, the system simply holds the current value for that tap during this cycle.

Integration Length: INTL

Two bit control that selects between 12 (INTL='00'),15('01'),18('10'), or 21('11') as the number of samples to average for each update cycle.

Initial Tap Weight: ITW

Two bit word which selects the specific tap to be adapted first. The adaptation would normally proceed in the following order for an ITW value of '000': K_0, K_4, K_1, K_3, K_0, K_4, K_1, K_3, etc. As ITW is incremented by one bit the first tap adapted rotates to the next in the

sequence. The relative order of the tap weights remains the same. Thus ITW='01' starts with K_4, ITW='10' starts with K_1 and ITW='11' starts with K_3. This option allows a sector to be re-read and each tap weight adapted on a different set of data (see Table 191 for the complete ITW bit mapping).

Tap Weight Range: TWR

Two bit control of tap weight range. If all four taps are to be adjusted this value should be set to '00'. By setting this value to '01' through '11', a reduced range of taps will be adjusted. The taps that aren't adjusted are still active but are held at their preprogrammed values. With TWR set to '00' the tap weight pointer counts from '0' to '3' then rolls back to '0', where '0' selects K_0, '1' selects K_4, '2' selects K_1, and '3' selects K_3. Incrementing TRW by one bit reduces number of taps adjusted by starting the count at a value other than '0' and counting to '3' before rolling back to the starting count value. Thus for TRW set to '01' the count starts at '1' and only taps K_4, K_1, and K_3 are adapted. For TRW='10' only taps K_1 and K_3 are adapted. With TWR set to '11', only tap K_3 is adapted.

Tap weights can be written and read by the controller. Thus the initial tap weight values can be preset near their optimal values and the final values can be read back after each adaption read cycle. The final taps weights remain as the initial tap weights for subsequent read cycles.

DZ and INTL Selection

Proper selection of DZ and INTL can allow for rapid adaptation or for slow, stable system tracking.

Symmetry control: SYMC

This is a two bit control that selects a specific set of taps to be controlled in a symmetrical manner. If SYMC is set to '00' the inner two taps (K_1 & K_3) are symmetrically adjusted whereas the rest are independently adapted. The adaptation is done in a ping-pong fashion where the two weights are changed simultaneously in two alternating cycles based on the value held first in one tap and then in the other. This type of adaptation is not as robust as a true LMS routine and will require some care in selecting the training pattern. For SYMC = '01' the two outer taps (K_0 & K_4) are adjusted symmetrically, for SYMC='10' both the inner and outer taps are adjusted symmetrically, and for SYMC='11' none of the taps are symmetrically adjusted.

Viterbi Detector

The Viterbi detector implements the maximum likelihood (ML) detector for PRML. For a discussion of the Viterbi algorithm in the context of magnetic recording, see the article by Tom Matthews and Richard Spencer, "An Integrated Analog CMOS Viterbi Detector for Digital Magnetic Recording", IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, pp. 1294-1302.

The Viterbi detector block diagram is shown in Figure 141. The incoming signal (from the FIR filter via the timing recovery block) has been demultiplexed into the odd and even interleaves on a bit-by-bit basis. This is shown in the diagram as the odd interleave signal and the even interleave signal. Each interleave of the Viterbi detector runs at 1/2 the channel data rate. Note that the odd and even interleaves of the Viterbi detector are clocked on opposite phases of the half rate data clock. Each interleave independently processes its data stream. The data streams from the odd and even interleaves are then multiplexed back together on a bit-by-bit basis to yield the recovered bit stream.

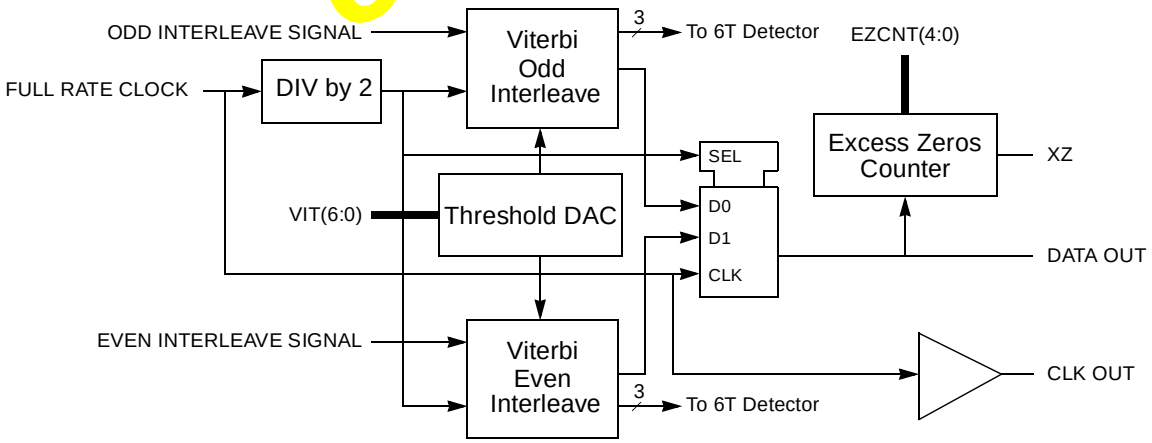

Figure 141 Viterbi Detector Block Diagram

The Viterbi detector operates in the continuous amplitude, discrete time domain. This is also known as the sampled domain. The detector compares the sampled level of the analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The nominal Viterbi threshold window size is set by a 7-bit DAC which is controlled by the Viterbi DAC serial control register 7-bit word VIT as shown below.

$$VIT_{TH} = 0.046 + 0.376 \cdot \left(\frac{K_{VIT}}{127}\right) \qquad \textit{(eq. 117)}$$

where K_{VIT} is the value of the VIT(6:0) Viterbi threshold DAC control word.

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Positive and negative thresholds in the Viterbi detector are modified based on the received data. The dynamic thresholds function to reject pulses of the same polarity as the most recent pulse, but of lesser amplitude. If a pulse of the same polarity as the most recent pulse exceeds the amplitude of the previous pulse, the one associated with the previous pulse (which is of lesser amplitude) is erased in the Viterbi detector's path memory. The path memory only has the ability to erase these smaller pulses if ten or fewer zeroes within each interleave have occurred between the two pulses of the same polarity. The path memory contents are set to zero when the internal PLL signal is low (see Figure 127 on page 8), which is true for all times except during tracking mode.

The AGC circuit adjusts the signal amplitude to ±250 mV peak. Side sampling for PR4 produces a nominal sampled signal amplitude of ±180 mV. This is a pseudo-ternary signal with the ±1 levels equal to ±180 mV and the zero level equal to 0 mV. Thus, the Viterbi threshold, VIT_{TH}, is nominally set to 90 mV. Since the data is pseudo-ternary, the nominal Viterbi threshold window size is $2VIT_{TH}$. An equation describing the Viterbi threshold is (eq. 117).

Figure 142 shows a block diagram of a Viterbi detector interleave. The summing blocks, Sum0 and Sum1, each form two signals that are fed to the metric calculation block. Opposite polarities of the incoming data stream and the difference metric are used by Sum0 and Sum1. The metric calculation block outputs the difference metric (which is fed back to the Sum0 and Sum1 blocks) and the two data streams that are used by the path memory block. One of these two data streams from the metric calculation block represents 1's that come from positive pulses in the ternary data signal. The other data stream represents 1's due to the negative pulses in the ternary data stream. Two 1's in one of the data streams without an intervening 1 in the other data stream results in the path memory erasing the first of these two consecutive 1's. A 0 results when neither of the two data streams is a 1. Decoding of the ternary signal is straightforward: a positive or negative pulse results in a 1; no pulse decodes to a 0. This decoding action can be thought of as undoing the precoding function.

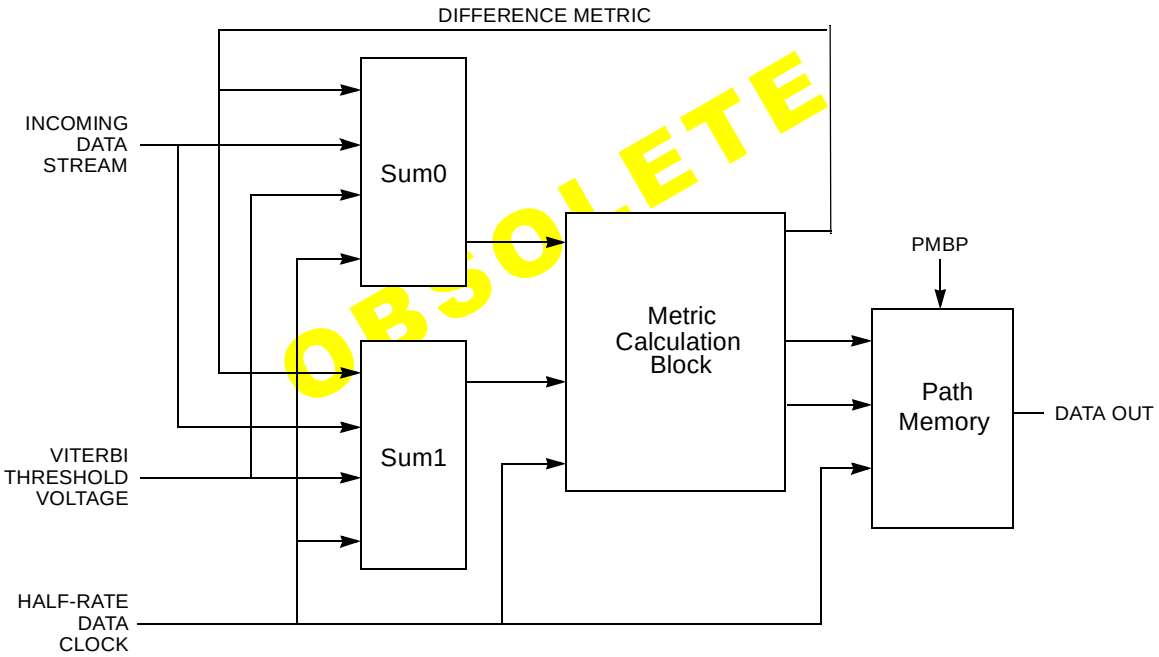

Figure 142 Viterbi Interleave Block Diagram

The Viterbi algorithm is a maximum likelihood detection technique. A conceptual description of the Viterbi algorithm follows. The data into the Viterbi detector is pseudo-ternary, that is, it has valid levels of 0 and ±1. The Viterbi detector uses the fact that two pulses on an interleave of the same polarity must have a pulse of the opposite polarity between them. As long as pulses of alternating polarity are received by the Viterbi detector, it functions like a simple ternary slicer.

The situation where two pulses on an interleave of the same polarity arrive without a pulse of the opposite polarity separating them can be divided into two cases: the first pulse is bigger than the second pulse or the second pulse is bigger than the first pulse. The Viterbi detector does not recognize the case where both pulses are of the same amplitude; it chooses one of the two pulses to be larger. For the following discussion, assume that two +1 pulses have occurred without a -1 pulse in between.

The case where the second pulse is smaller is handled by the dynamic thresholds in the Viterbi detector. The first (larger) pulse pulls the positive threshold up. The following pulse is smaller and therefore won't cross the upper threshold, thereby rejecting the smaller of the two +1 pulses.

The case where the second pulse is bigger than the first is handled by the path memory. The dynamic positive threshold is pulled up by the first +1 pulse and a 1 is output. The second +1 pulse comes along and exceeds the threshold set by the previous +1 pulse, causing a second 1 to be output to the path memory. The only way these two 1s in a row can be output is for the second pulse to be

bigger than the first. The path memory uses this fact and erases the first of these two ones. In order to do this erasure, the default path memory requires that no more than ten zeros occur between the two 1's of the same polarity. Control register bit PML, when set to a '1', allows the path memory to be increased to 21. Control register bit PMBP allows the path memory to be bypassed for test purposes.

After evaluating these two cases of consecutive pulses of the same polarity, the Viterbi algorithm can be seen to operate as a ternary slicer except when two consecutive pulses of the same polarity occur. When this situation happens, the Viterbi algorithm chooses the larger of these two pulses and treats the other as if it were a 0.

The Viterbi detector has two sets of test signals: Vit Sig Odd and Vit Sig Evn; and Held Sig Odd and Held Sig Evn (see Table 192 and Table 193). Vit Sig Odd and Vit Sig Evn are the inputs to either interleave of the Viterbi detector. These signals are held any time a '1' is detected for purposes of computing the difference metric. The held signals are output as Held Sig Odd and Held Sig Evn.

The Viterbi detector also has a programmable counter that counts the number of consecutive zeros occurring in the recovered data stream. If the number of consecutive zeros exceeds the count programmed with the EZCNT control register bits, the excess zeros (XZ) output pin is raised; the XZ pin stays in the high state until a valid 1 resets the counter and causes XZ to drop. This feature is intended to aid in the rapid detection of tape drop outs. The excess zero count EZC is equal to the value of the EZCNT(4:0) DAC as shown in (eq. 118)

$$EZC = 0.5 + K_{EZCNT} \qquad \textit{(eq. 118)}$$

where K_{EZCNT} is the value of the EZCNT control word (0 to 31).

EZC is always 1.5 clock cycles longer than the DAC setting.

Timing Recovery Loop

The timing recovery block uses a fully integrated, fast acquisition phase-locked loop (PLL) to implement clock recovery on the incoming data stream. A block diagram of the timing recovery system is shown in Figure 143. A voltage-controlled oscillator (VCO) generates a frequency which is divided by two and has its phase compared in a phase-frequency detector (PFD) with that of an input reference clock F_{REF}, or with the signal data from the FIR, generating an error term. The error term is converted into a current in the charge pump which is integrated by an off-chip capacitor C_{TR} connected differentially to the CTRP and CTRN pins. The Imult block converts this capacitor voltage into an integral scaling factor which modulates the I_{REF} current and is summed with the current output from the Pmult block which scales its current proportionally with the error at the phase detector output. The summed current controls the VCO frequency, thus forming a control loop

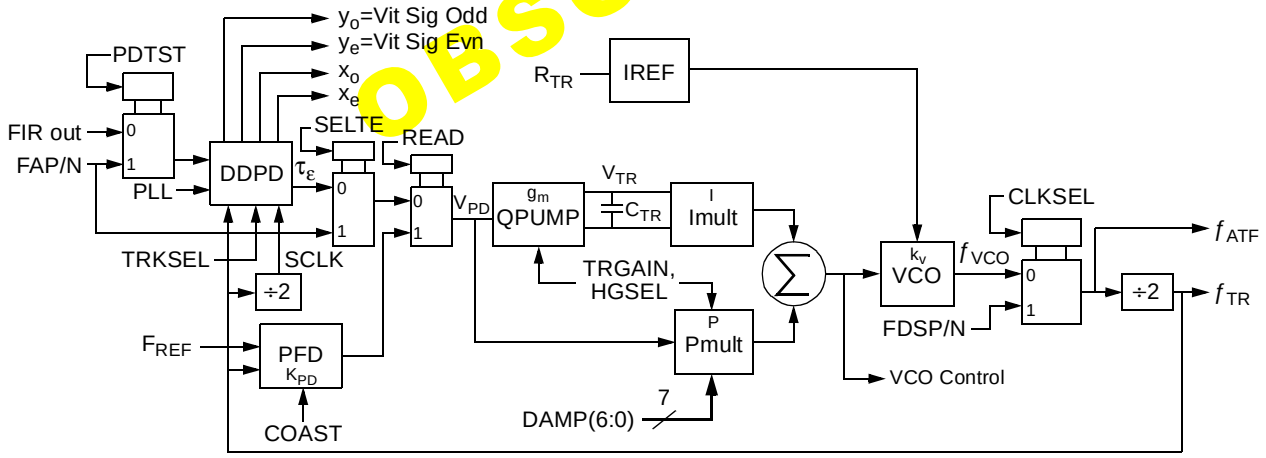

Figure 143 Timing Recovery Block Diagram

Figure 127 on page 8 shows the timing for a read cycle. A low level on the internal READ signal defines idle mode which occurs during dropouts or when in Write Mode (WG pin high). In Idle mode the loop either locks to the external F_{ref} signal through the phase/frequency detector (PFD); or coasts, where the phase/frequency detector is disabled and the VCO runs open-loop. The control register bit COAST when set to a '1' defines the coast mode. A read operation is initiated with a negative transition on the DO output. This defines acquisition mode where samples from the FIR filter are read by the decision-directed phase detector (DDPD) and an acquisition timing gradient algorithm is used to coarse align the data to ideal samples, as illustrated in Figure 143. Because the loop must acquire lock to random data, this acquisition timing gradient algorithm has limitations, so after a fixed time set by the PLL sync count the loop switches into tracking mode where a more precise locking algorithm is applied. The part stays in tracking mode until another dropout is detected where it switches back to idle mode.

The goal in acquisition mode is to adjust the phase of the VCO clock to the point where the tracking timing gradient algorithm can track the data. Ideal PR4 data has three valid sample values, denoted +1, 0, and -1. The AGC loop and the two filters (CTF and FIR) should be set to equalize the data properly to produce these ideal sample values. It is the job of the timing recovery loop to adjust the

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phase and frequency of the sampling clock to converge on these three levels. The acquisition algorithm slices each sample into one of three levels, based strictly on threshold voltages separating a '-1' from a '0' from a '+1'. These samples can be compared with the ideal samples and the phase adjusted accordingly.The decision-directed phase detector (DDPD) operates on sampled data in either an analog or quantized form to compute a timing gradient. Since initially the phase is random, it isn't true that the closest ideal voltage level is necessarily the correct one. It is true, however, that any large transition in the data must have at least one '+1' sample for a positive transition, and at least one '-1' sample for a negative transition. To determine which direction to adjust the phase, the slope of the input waveform must be known, which can't always be determined with sampled information only. Inspection of equalized PR4 data, however, reveals the fact that two consecutive '+1' samples or two consecutive '-1' samples must have a peak between them and consequently a change in slope, and that a '+1' followed by a '-1' must have a negative slope, and a '-1' followed by a '+1' must have a positive slope. Any '0' sample could have any slope and any '0' sample preceding or following a '+1' or '-1' sample could have either slope. The acquisition timing gradient thus operates only on '+1' and '-1' samples. Two consecutive samples are taken and if they are both non-zero, their magnitudes and signs are compared. The signs determine the slope of the timing gradient and the magnitude of the timing gradient is equal to the difference in the samples magnitudes. All other cases are ignored. The phase error is proportional to the timing and the phase and frequency of the clock is adjusted appropriately to minimize the error. The acquisition timing gradient can be expressed mathematically as

$$\Delta\tau_n = -(y_n \cdot \hat{x}_{n-1}) \cdot \hat{x}_n^2 + (y_{n-1} \cdot \hat{x}_n) \cdot \hat{x}_{n-1}^2 \qquad \textit{(eq. 119)}$$

where

$$\hat{x}_n = \begin{cases} 1 \leftarrow y_n \geq V_{THTR} \\ 0 \leftarrow -V_{THTR} < y_n < V_{THTR} \\ -1 \leftarrow y_n \leq -V_{THTR} \end{cases}$$

The 'y' terms are the sampled analog values at the current or previous sample time and the 'x' values are the quantized estimates of the ideal 'y' values. V_{THTR} is a threshold voltage equal to one half the ideal '1' voltage.

After a sufficient number of clock periods it is assumed that the acquisition algorithm has adjusted the phase of the clock to be "close enough" so that the DDPD can switch to the tracking algorithm. This number is set by the AGC and PLL Sync Field counters described in Gain Control The tracking algorithm is similar to the acquisition algorithm comparing adjacent '+1' or '-1' samples to one another, but also compares '0' samples to ideal '0's when the '0' samples are adjacent to a '+1' or '–1'. The tracking timing gradient is mathematically expressed as

$$\Delta\tau_n = -(y_n \cdot \hat{x}_{n-1}) + (y_{n-1} \cdot \hat{x}_n) \qquad \textit{(eq. 120)}$$

where the 'x' values are given in (eq. 119).

This algorithm will converge to a clock phase which produces only three possible sample levels. If the tracking algorithm were used for acquisition, there is a possibility that the loop will converge to a phase exactly 180° off. Thus two algorithms are needed. Note that both terms in (eq. 120) will be non-zero only if there are two successive '±1's. Any '0' data term will null out the sample adjacent to the '0'. A '+1' or '-1' adjacent to a '0' is used to determine the slope of the data and adjust the phase in the proper direction to move the sampled point closer to '0'. Note also the comparison between (eq. 119) and (eq. 120). Equation (eq. 119) has the squared terms to force the timing gradient to zero if either sample is a '0'.

The external differential ECL input pins FDSP/N can be used in place of the VCO for test purposes by setting the CLKSEL control register bit to a '1.' Several test signals are available out of the decision directed phase detector. A hardware simplification of the timing gradient splits the path into odd and even samples rather than into consecutive samples. Hence instead of y_n, y_{n-1}, x_n and x_{n-1} available for test, y_e, y_o, x_e and x_o are instead. The only difference is that each of the odd and even samples is held for two cycles. The sign of the timing gradient will invert with each cycle to account for the fact that the odd and even samples alternate between the n and n-1 samples with each cycle. These same even and odd y samples are referred to VIT SIG O and VIT SIG E as they are also used in the odd and even interleaves in the Viterbi. Also available is the half-rate sampling clock SCLK (see Table 192 on page 42).

Clock Recovery Loop Gains

In the Idle/Write mode, the timing recovery loop is locked to an external reference which is running at the user data rate. The PFD outputs a pulse whose width is proportional to the phase/frequency difference of the loop's phase input θ_i, with respect to the timing recovery VCO's phase output, θ_o with the following relationship

$$\Delta V_{PD} = K_{PD} \cdot (\theta_i - \theta_o) \qquad \textit{(eq. 121)}$$

where K_{PD}=0.125 V/rad.

In read mode the timing recovery loop is updated via the DDPD. The phase detector output may still be modeled similar to that of Idle/Write mode except now the phase error is derived from either equation (eq. 119) or (eq. 120) where the phase error is proportional

to the magnitude of the voltage difference between the received sample and the ideal sample. To maintain the same phase detector gain K_{PD} of 0.125 V/rad as in Idle/Write mode, the timing gradient voltage must be gained up as shown below

$$\Delta V_{PD} = 1.43 \cdot \Delta\tau_n \quad \textit{(eq. 122)}$$

The gain term allows equation (eq. 121) to be valid in Tracking mode as well.

The charge pump (QPUMP) block produces a differential charging/discharging current across the external C_{TR} capacitor proportional to the phase detector output. The QPUMP gain is a function of the timing recovery loop mode. When the loop is switched from acquisition to tracking, the gain of the QPUMP is reduced by a programmable factor of either 5 or 10. This ensures small changes in phase correction while in the tracking mode and thus the loop will be less susceptible to noise.

$$I_{QP} = g_m \cdot \Delta V_{PD} \quad \textit{(eq. 123)}$$

where ΔV_{PD} is given above and g_m equals 460µA/V in Idle, Write, or Acquisition mode and equals 115 µA/V or 460 µA/V in Tracking mode. (Depending on the setting of the HGSEL bit in the control registers as shown in Table 6.)

Table 185Charge Pump and Pmult Gains

Mode	HGSEL	g_m	K_P
Idle/Write	x	460µA/V	1.0
Acquisition	x	460µA/V	1.0
Tracking	0	115µA/V	0.5
	1	460µA/V	1.0

The charge pump pumps the current differentially into an external capacitor C_{TR} producing an integrated voltage ΔV_{TR} across pins TRCP and TRCN. The IMULT block scales this voltage by a scaling factor I as shown below

$$I = 1.0 \quad \textit{(eq. 124)}$$

IMULT provides an integral gain term to the input of the VCO.

The PMULT block provides a proportional gain term to the VCO as shown in (eq. 125)

$$P = K_P \cdot \left(\frac{127 - K_{DAMP}}{127}\right) \quad \textit{(eq. 125)}$$

where K_{DAMP} is the value of the seven bit damping DAC DAMP(6:0), and K_P is the proportional multiplier gain which equals 1.0 in Idle and Acquisition mode, and equals either 0.5, 0.25, or 1.0 in (Tracking mode depending on the setting of the HGSEL bit as shown in Table 6.)

I_{REF} is the reference current for the VCO and is set by connecting an external resistor R_{TR} between pins RTR and VEE4, typically set to 2.5kΩ

$$I_{REF} = \frac{1.25V}{R_{TR}} \quad \textit{(eq. 126)}$$

The VCO center frequency is set by I_{REF}

$$f_0 = k_I \cdot I_{REF} \quad \textit{(eq. 127)}$$

where k_I is 167.4MHz/mA.

The VCO output frequency is determined by summing the IMULT and PMULT terms, modulating the VCO about its center frequency. The VCO frequency can be expressed as

$$f_{VCO} = f_0 \cdot (1 + k_V \cdot (I \cdot \Delta V_{TR} + P \cdot \Delta V_{PD})) \quad \textit{(eq. 128)}$$

where k_V is the VCO gain given by

$$k_V = 0.4V^{-1} \quad \textit{(eq. 129)}$$

The VCO is divided by 2 to create the timing recovery clock frequency f_{TR}

$$f_{TR} = \frac{f_{VCO}}{2} \quad \text{(eq. 130)}$$

Equations (eq. 121) through (eq. 130) can be combined and the closed loop response H(s) in the frequency domain can be expressed as

$$H(s) = \frac{\theta_o}{\theta_i} = \left(\frac{\frac{K_{VCO}K_{PD}P}{2}\left(s + \frac{Ig_m}{PC_{TR}}\right)}{s^2 + \frac{K_{VCO}K_{PD}P}{2}s + \frac{Ig_mK_{VCO}K_{PD}}{2C_{TR}}} \right) \quad \text{(eq. 131)}$$

where

$$_{VCO} = 2\pi \cdot f_0 \cdot k_V$$

This along with the open loop response G(s) can be rewritten using the conventional control system second order loop parameters ω_n, ζ, τ, and K as

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{K\left(s + \frac{1}{\tau}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{(eq. 132)}$$

and

$$G(s) = \frac{\theta_o}{\theta_i} = \frac{K\left(s + \frac{1}{\tau}\right)}{s^2} \quad \text{(eq. 133)}$$

where

$$\omega_n = \sqrt{\frac{Ig_mK_{VCO}K_{PD}}{2C_{TR}}} \qquad \zeta = \frac{P}{2}\sqrt{\frac{K_{VCO}K_{PD}C_{TR}}{2Ig_m}} \qquad \tau = \frac{PC_{TR}}{Ig_m} \quad \textit{and} \quad K = \frac{K_{VCO}K_{PD}P}{2} \equiv 2\pi \cdot f_C$$

ω_n is known as the loop natural frequency, ζ is the loop damping factor, τ is the loop time constant, and K is the loop gain in rad/s, which is also referred to as the unity gain frequency, crossover frequency, or loop bandwidth. f_C is the loop bandwidth (or loop gain) in Hz. Note that user programmable K_{DAMP}, which controls the value of the PMULT gain P, controls both the gain K and damping factor ζ. As the value of K_{DAMP} is increased, the value of P is decreased and thus both the gain and damping factor are decreased. Only by selecting the value of the external capacitor C_{TR} can the relative ratio of gain to damping factor be controlled.

When calculating loop stability, there is an additional phase shift which must be accounted for due to the time delay within both the FIR filter and DDPD associated with sampling. The FIR filter adds a delay of two clock cycles and the DDPD adds an additional two for a total delay of four timing recovery clock cycle delays. The phase shift in the frequency domain associated with a delay in the time domain is

$$\Delta\Phi = -\omega \cdot t_0 = -2\pi f \cdot 4T \quad \text{(eq. 134)}$$

where t_0 is the delay which in this case equals four times the data rate period T which equals $1/f_{TR}$.

Phase margin Φ_R for the system can be derived by calculating the phase, or angle, of equation (eq. 133) and adding it to that of (eq. 134) at the cutoff frequency f_C, and making several substitutions

$$\Phi_R = \tan^{-1}(4\zeta^2) - \frac{f_C}{f_{TR}} \cdot 4 \cdot 360° \quad \text{(eq. 135)}$$

where Φ_R is in degrees.

The user needs to choose the damping factor ζ and loop bandwidth f_C appropriately to achieve adequate phase margin for the system. The effect of the 4T phase shift can be significant for high values of f_C. The user must choose the loop gain sufficiently low so that this phase shift does not adversely affect the loop stability. For example at a data rate of 41.85MHz a loop gain of 436kHz yields a $\Delta\Phi$ of 15°. For a damping factor of 1.0 this creates 60° of phase margin.

An additional factor must be accounted for in designing the loop dynamics and that is that both the acquisition and tracking timing gradient algorithms do not update the loop on every sample. In acquisition mode a '0' sample causes no loop update and in tracking

mode consecutive '0' samples cause no loop update. This has the same effect as increasing the VCO feedback divider (which is equal to 2 in this part) which lowers both the loop gain and damping factor as can be seen by equations (eq. 132) and (eq. 133). Because of this the nominal loop gain can be set much higher than that determined by phase margin calculations based on the assumption that the data is unlikely to have regions free of '0' samples. Loop stability is really data dependent and the user should perform a statistical analysis with either simulation or real data before deciding upon final values for the various loop stability parameters. Favorable simulation results have been obtained on random data at 41.85MHz with C=2.2nF, K_{DAMP}=90, and TRGAIN='0'.

Automatic Tracking Frequency (ATF)

The ATF provides demodulation of two pilot tones used for servo control of the head position. Servo position information is embedded in the data spectrum on alternate tracks. Tracks are designated f_0, f_1 and f_2 as shown in Figure 145. Two heads are mounted on a scanner which rotates the heads across the moving tape at an angle to produce a series of diagonal tracks. Alternating tracks are written with alternating heads. All tracks written with Head 0 are denoted f_0 while tracks written with Head1 are denoted either f_1 or f_2. Each head writes with a different azimuth angle to minimize high frequency crosstalk between tracks. The data spectrum written on all tracks is relatively flat with the exception of two 50kHz wide notches placed at 465kHz and 697.5kHz which are derived by dividing the 41.85MHz F_{ref} clock by either 60 or 90. On track f_0 these notches are >9dB deep. On tracks f_1 and f_2 the notches are >3dB deep. A16-19dB tone is mixed into the data at 465kHz on track f_1, and at 697.5kHz on track f_2. The resultant spectrum for track f1 is shown in Figure 144. These frequencies are low enough to be read by the head on the adjacent track. So, as Head 0 reads track f_0, a fringe field from both f_1 an f_2 will be read. By comparing the relative magnitude of the f_1 tone with the f_2 tone, the scanner position can be servoed to stay in the middle of track f_0.

The tones are mixed into the data by controlling the encoding and scrambling of the data written. At the beginning of each track there is a preamble where the magnitude of the tones is 10dB higher than on the rest of the track. This area is referred to as the burst and lasts 88µs. The magnitude of the fringe field read on track f_0 is 6dB lower than that read on tracks f_1 and f_2. During normal tracking both the burst and normal region are read and used for servoing. During search mode (also known as trick mode), the tape is moved from 2x to 20x faster than in normal mode. A 10x mode is shown in Figure 145. Only the 88µs burst area in the beginning of tracks f_1 and f_2 is used by the servo system in search mode. A third mode known as edit mode exists where only the burst region of track f_0 is read so that the remainder of the track can be overwritten with new data.

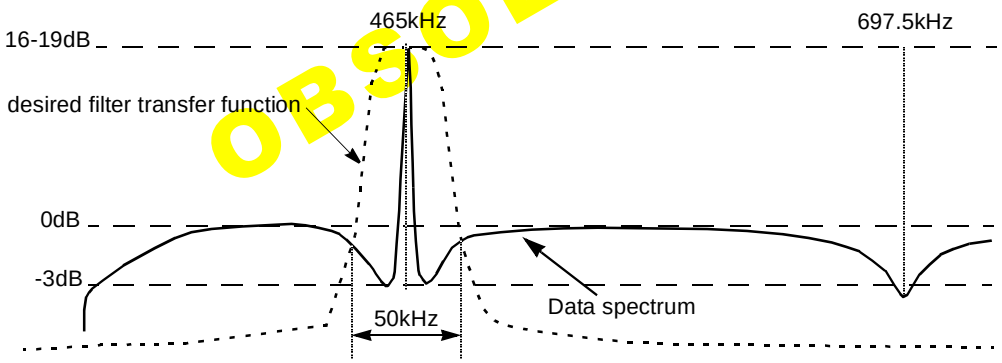

Figure 144 F_1 Pilot Tone characteristics

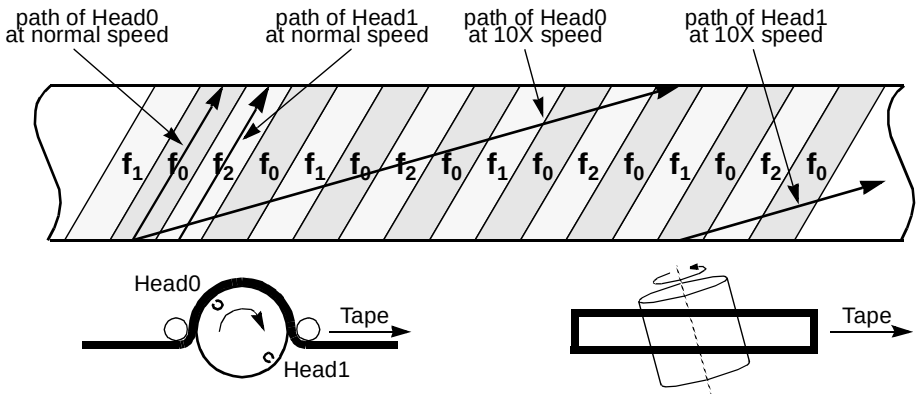

Figure 145 Tape Track Format

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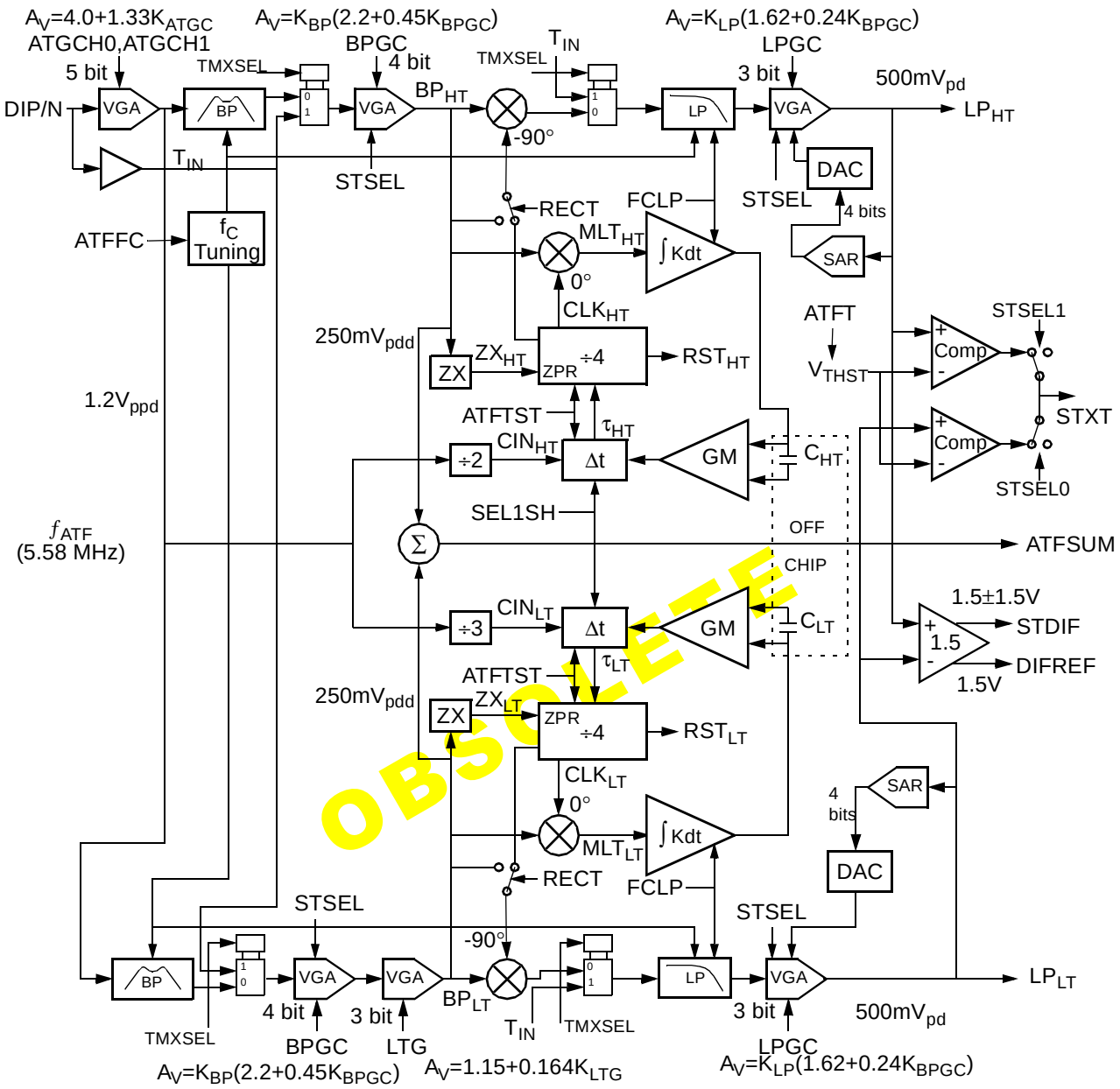

Figure 146 Automatic Tracking Frequency System Block Diagram

A block diagram of the ATF system is shown in Figure 146. The signal passes through an initial gain stage and is then split into two paths, one for the 465kHz low tone, and the other for the 697.5kHz high tone. A bandpass filter is used in each path to improve the signal to noise ratio of the low-level tones. The bandpass output is amplified by a VGA whose nominal value is user programmable and is automatically switched by 6dB in search (or trick) mode. The low tone path has another VGA which allows the user to increase the low tone signal by 4.5dB ±2.5dB to compensate for the channel response of the low tone relative to the high tone. Two phase-locked loops are used to pick the tones out of the data spectrum using the divided-down timing recovery VCO clock, a variable delay cell, analog multiplier and integrating loop filter. The timing recovery VCO runs at twice the timing recovery clock rate so that the proper divide ratios can be created in the ATF circuit (see Figure 143 on page 24). The f_{ATF} signal normally equals the VCO frequency but also allows the FDSP/N input to be multiplexed in for test purposes. An analog multiplier mixes the input signal with the PLL clock and outputs sum and difference frequencies. The DC component is filtered out with a low-pass filter having a cutoff frequency which can be varied from 5 to 35kHz, thus passing only frequencies within a narrow range of the PLL frequency. Another VGA boosts the level of the low tone by a user-programmable amount which automatically switches by 10dB in search and edit modes. The two tone levels can be output on the ATFOCP/N test points directly, while the STDIF pin subtracts the two tone levels and outputs the difference along

with a DC bias level, which is available on pin DIFREF. Either tone level can be compared with a programmable threshold and output on the digital STXT pin which can be used for burst detection in search mode.

Table 186STSEL ATF Mode Control

STSEL	STXT	Mode	K_{BP}	K_{LP}	f_C
00	no tone	track	2.0 (+6dB)	3.3 (+10dB)	Lo
01	low tone	search (trick)	1.0 (0dB)	1.0 (0dB)	Hi
10	high tone	search (trick)	1.0 (0dB)	1.0 (0dB)	Hi
11	both tones	edit	2.0 (+6dB)	1.0 (0dB)	Hi

The 2-bit control register word STSEL(1:0) controls the mode in which the ATF operates, controls the STXT output signal, and sets the various VGA gains appropriately as shown in Table 186. For normal tracking of data, STSEL is set to '00', no signal is output to STXT, the bandpass and lowpass VGA's are set to their maximum values, and the PLL bandwidth and lowpass cutoff are set low. During trick or search mode, the STXT output is used to detect the burst region and either tone can be selected to be compared to a threshold and output on STXT. STSEL='01' selects the low tone (track f_1) while setting STSEL to '10' selects the high tone (track f_2). The bandpass VGA is set 6dB lower than in track mode since the f_1 and f_2 tracks are read directly in this mode rather than the by the fringe field on f_0. The lowpass VGA is set 10dB lower to account for the increased signal in the burst, and the PLL bandwidth and lowpass cutoff are set high so that a servo signal output can be acquired within the 88µs period of the burst. Finally, with STSEL set to '11' the part is programmed for edit mode where both tone comparison outputs are output to STXT. The bandpass VGA is set high, the lowpass VGA is set low, and the PLL bandwidth and lowpass cutoff are set high since the burst on f_0 is being read.

The input programmable VGA allows the user to customize the gain differently for each head. The value of the VGA gain A_V in V/V is given by

$$A_V = 4.0 + 1.33 \cdot K_{ATGC} \qquad \textit{(eq. 136)}$$

where K_{ATGC} is the value of either the 5-bit ATGCH0 or ATGCH1 register setting (0 to 31).

This allows the gain to be varied over the entire 20dB 30-300mV input range. The logic level of the HDSEL pin selects the specific head register as it does for the other head-specific functions (see Gain Control on page 7). The bandpass filters have a signal input limit of $1.2V_{ppd}$ and the user must be careful to set the ATGC registers to the appropriate values so that adequate signal level is obtained without overranging the filter input. Although clamps limit the filter input to keep levels from latching the filter, the input signal must be below $1.2V_{ppd}$ to maintain linearity.

Each bandpass filter is implemented as a 4^{th}-order Chebyshev leapfrog design centered at the tone frequency with a Q of 4.5, which produces nominally 0.5dB ripple in the passband, defined as the region between the -0.5dB rolloff frequencies, and has a roll-off of 40dB/decade. A tuning loop consisting of an MOS biasing network driven with a current mirrored in from the timing recovery VCO is used to tune the center frequency of the bandpass. The tuning network compensates for process, temperature, power supply, and recovered clock frequency variations. A 3-bit DAC controlled by control register bits ATFFC(2:0) allows the center frequency of the bandpass to be varied ~±25% as shown in Table 187. Output pins ATFOCP/N provide a test point for the signal after the bandpass. An optional summer mixes the two bandpass tone outputs together. To activate ATFOCP/N the control register bit BMXEN must be set to a '1'. Table 192 on page 42 shows the mapping of the ATFOCP/N test points with the ATFSEL control bit and HTSEL control bit.

Table 187ATF Center Frequency DAC

ATFFC(2:0)	Δf_0
011	+18.75%
010	+12.5%
001	+6.25%
000	0%
111	-6.25%
110	-12.5%
101	-18.75%
100	-25%

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The bandpass has a variable gain stage following it to allow the user to compensate for variations in the frequency content of the data. The VGA before the bandpass should be set for a $1.2V_{ppd}$ input signal to the bandpass. The signal out of the bandpass will be on the order of mV's depending upon the frequency spectrum of the input data. This signal needs to be amplified to $250mV_{ppd}$ for the ATFOC test point output and to yield the proper loop gain for the PLL, since the PLL loop gain is signal dependent. Control register bits BPGC(3:0) control the bandpass VGA gain according to

$$A_{BP} = K_{BP} \cdot (2.2 + 0.45 \cdot K_{BPGC}) \quad \textit{(eq. 137)}$$

where K_{BPGC} is the value of the 4-bit BPGC register setting (0 to 15), and
K_{BP} is a bit controlled by control register word STSEL(1:0) and is set to '1' in search(trick) and edit modes, and is set to '2' in track mode (see Table 186).

The low-tone path has an additional VGA which allows the channel response to be compensated for since the 465kHz tone will have an inherently lower amplitude than the 697.5kHz tone. Control register word LTG(2:0) allows the gain to be varied 4.5dB±2.5dB according to

$$A_{LT} = 1.15 + 0.164 \cdot K_{LTG} \quad \textit{(eq. 138)}$$

where KLTG is the value of the 3-bit LTG(2:0) register word which can vary from 0 to 7.

A phase-locked loop with an accurate center frequency and a restricted lock range can be used to lock onto a specific input frequency embedded in a spectrum of noise. The loop used here consists of an analog multiplier, a loop filter (or integrator), a variable delay circuit, a divide-by-4 circuit, and the timing recovery clock divided down by 30 for the high tone, and 45 for the low tone. The divide-by-4 is needed so that a quadrature component 90° out of phase can be generated (see further discussion below). The loop frequency is fixed and only the phase is varied through the 1-shot variable delay cell. The analog delay cell is controlled by the analog voltage output by the integrating loop filter, thus completing the loop.

An analog multiplier output signal will go to zero when the two input signals are 90° out of phase, and have a maximum output proportional to signal amplitude at the sum and difference frequencies of the two inputs when the two inputs are in phase. By using two multipliers, one set to 0° inside the loop used to lock onto the proper frequency and phase, and another set to -90°outside the loop, a signal can be generated with a level proportional to the input signal amplitude at the loop frequency. Only difference signals within the lowpass cutoff frequency of the PLL frequency will be output. The lowpass cutoff is set by a geometric ratioing of the lowpass components to that of the bandpass (and thus will change with the ATFFC DAC setting). The loop bandwidth (or loop gain) of the PLL is set to a frequency close to that of the lowpass so the 465kHz and 697.5kHz tones will always be passed. The PLL bandwidth and lowpass cutoff frequencies are varied with mode as shown in Table 188. In search and edit modes, when acquiring lock during the burst, the PLL bandwidth and lowpass cutoff are user adjustable via the FCLP control register bits according to Table 188 which also shows the effective Q of the system.

Table 188FCLP ATF Bandwidth Control

STSEL	FCLP	Mode	PLL BW	Lowpass f_C	Low Tone Q	High Tone Q
00	XX	track	1kHz	5kHz	47	70
$\overline{00}$	00	search/edit	20kHz	20kHz	12	18
$\overline{00}$	01	"	25kHz	25kHz	9.3	14
$\overline{00}$	10	"	30kHz	30kHz	7.7	11.5
$\overline{00}$	11	"	35kHz	35kHz	6.6	10

The low cutoff frequency of the lowpass and PLL puts restrictions on the transient response of the ATF. In the search and edit modes the ITI servo burst section is read which is only 88µs in length. With FCLP the user can trade-off transient response of the system for Q, or system tracking accuracy.

ATF demodulation initiates with the PLL signal from the timing recovery loop (see Figure 127 on page 8) which acts as an enable for the ATF system. Since the phase of the timing recovery clock is used to lock onto the data, it is important that the timing recovery clock is locked to the data before beginning ATF demodulation. To aid in transient response a zero-phase restart circuit is used to align the clock to the data. The zero-cross circuit detects the phase of the data signal and picks the divide-by-4 phase which is closest in phase to that of the data, thus minimizing the phase acquisition process. The divide-by 4 circuit has 4 possible phase outputs. The variable delay cell has limited range and depending on initial phase conditions the loop may try and converge to a phase which is a multiple of 2π away from the proper point. When the loop control voltage reaches an upper or lower bound, the control voltage is reset and the zero-phase restart signal reselects the phase, if the system is reading the burst in search or edit modes, which is determined by decoding the STSEL(1:0) signal (see Table 186). When the control voltage reaches its ±π bound during ATF tracking, the voltage is reset to 0 and the output clock is inverted, thus shifting the phase by 2π.

The PLL multiplier output is lowpass filtered with a second-order lowpass filter to reject the sum frequency leaving only the difference frequency. The filtered tone output of each loop is amplified to the proper output levels by a fixed gain-of-3 gain stage before the

lowpass, and a variable gain stage after the lowpass. The LBGC control register word allows the user to vary the gain of the VGA according to

$$A_{LP} = K_{LP} \cdot (1.62 + 0.24 \cdot K_{LPGC}) \quad \textit{(eq. 139)}$$

where K_{LPGC} is the value of the 3-bit LPGC register setting (0 to 7), and
K_{LP} is a bit controlled by control register word STSEL(1:0) and is set to 1 in search and edit modes, or is set to 3.3 in track mode (see Table 186).
This allows the lowpass gain to be automatically decreased when the burst in edit and search modes.

The two filtered tone signals can be output on the ATFOCP/N test pins according to Table 192. In addition the difference between the two tones is output on the STDIF pin with a bias which is output on pin DIFREF, nominally set to 1.5V. When the two tone magnitudes are equal, the STDIF output level will equal that of DIFREF. As the scanner position is moved off of center towards the low tone f_1, the level of STDIF will increase, and as the scanner moves toward f_2 the STDIF level will decrease. Gains are set such that a maximum signal read by Head0 in the burst area will be ±1.5V about the 1.5V reference. This would correspond to the scanner being completely off track and reading the middle of the f_1 or f_2 track. The normal tracking level would be 1.5V, which is equal to the 1.5V bias plus the difference of the f_1 and f_2 signals, whose levels are now reduced to 238mV since there is a 10dB difference between the burst and normal area. The STDIF output stage has a gain of 3. Thus, for an output swing of $1.5V_p$ only $500mV_{pd}$ will be seen at the lowpass VGA outputs. the user must insure through the settings of the various VGA's that the VGA output does not exceed $500mV_{pd}$.

An additional output STXT compares the output of either tone or both tones with a threshold controlled by the 3-bit serial control register word ATFT. This is used for position detection under search mode. By setting this threshold higher than the normal mode maximum output level, but lower than that of the 10dB servo burst, the STXT pin will pulse high when a servo burst is read. Control bits STSEL(1:0) select the tone according to Table 186. Eq. 140 shows the STXT threshold V_{THST} as a function of the ATFT DAC value K_{ATFT}

$$V_{THST} = 0.254 \cdot (1 + 0.016 \cdot K_{ATFT}) \quad \textit{(eq. 140)}$$

where K_{ATFT} is the value of the 3-bit control register word ATFT(2:0) (0 to 7).
Note that V_{THST} is compared against the lowpass VGA outputs which have 2/3 the amplitude of the final STDIF output.

The control register test bit ATFTST, when set to a '1', allows the variable delay circuit to be bypassed and the divided clock frequency multiplexed directly into the divide-by-4 block. If CLKSEL is set to '1', the external FDSP/N input will replace the timing recovery clock output and be the source clock for the ATF PLL. The phase of this clock can be controlled and used to test the multiplier in an open loop configuration. The SELSH1 register bit changes the current reference for the variable delay cell1-shot circuit. With SEL1SH='0' the delay will track the timing recovery VCO. With SEL1SH='1' the current for the delay cell is fixed and will not vary with data rate. This feature is included primarily for experimental purposes and it is recommended to the user to leave SEL1SH set to '0'.

Table 192 in TEST MODES shows the ATF signals which are available on the various test points. The ATFOCP/N output is controlled by the control register word ATFSEL(2:0) and control register bit HTSEL. This MUX output is also available on test point TP1P/N when control bit TP1SEL is set to 7. Available on ATFOC are the input VGA VGATF Out, the 2 bandpass VGA outputs BP_{LT} and BP_{HT}, the PLL multiplier outputs MLT_{HT} and MLT_{LT}, the PLL control voltages V_{CLT} and V_{CHT}, and the lowpass VGA outputs LP_{LT} and LP_{HT}. The divide-by-15 clock is available on the ECL test point TP4. CMOS test pointsCT1 and CT2 can be set to output the divide-by-2 and divide-by-3 input clocks CLK_{LT} and CLK_{HT}, the variable delay outputs τ_{LT} and τ_{HT}, the divide-by-4 clock output CLK_{LT} and CLK_{HT}, and the control voltage reset signals RST_{LT} and RST_{HT}.

An alternative architecture is available by setting the control register bit RECT to a '1.' This puts the part into the rectifier mode where the phase-locked loop is bypassed and the bandpass VGA output is sliced and used as the clock input to the multiplier. The multiplier will act as a rectifier in this configuration and the lowpass will filter out the high frequencies leaving only the DC level. This mode can be used as an alternative when reading the burst where transient response is a concern, but due to the low Q of the bandpass, tracking performance will suffer. This feature exists primarily to quantify the performance of the PLL and is not the recommended mode of operation for the part.

The control register bit DATF when set to a '1' will disable power to the ATF circuitry.

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Mode Control and Power Management

The fundamental operating modes are controlled by power down (PD), and read gate (RG). If PD is high, the entire chip is powered down. If PD and RG are all low the part is in idle mode where the AGC loop locks to input data, the timing recovery loop locks to the reference, and the FIR and Viterbi detector are powered down. If PD is low and RG is high, the part is in read mode, behaving as described in Gain Control. Both read mode and write mode are asynchronous states and may be initiated or terminated at any time. A power reduction bit PREN in the control register when set to a '1' causes the FIR, Viterbi, and decision-directed phase detector (DDPD) to power down in idle and write mode. A summary of the Mode Control is shown below in Table 189. The ATF circuitry may be powered off by setting the DATF control register bit to a '1'.

Table 189Mode Control

PD	PREN	RG	MODE
1	X	X	Entire chip powered down, serial port still functional
0	0	0	IDLE mode, all blocks powered on
0	0	1	READ mode, all blocks powered on
0	1	0	IDLE mode, FIR, Viterbi, DDPD powered off
0	1	1	READ mode, all blocks powered on

Digital Control

Programmable control of the chip is performed through a serial digital interface and a 16 word,12-bit wide register file. Control information is stored in the register file and used directly as digital control lines or sent to one of the onboard DACs to create analog control signals. The interface consists of three CMOS-level signals for input/output data, clock, and enable. Upon asserting SPEN, the serial port is enabled and ready for input on SPDATA which is clocked by SPCLK. The SPDATA line provides the read/write, address and data information. The Head Select pin selects between two parameter sets for either Head0 or Head1.

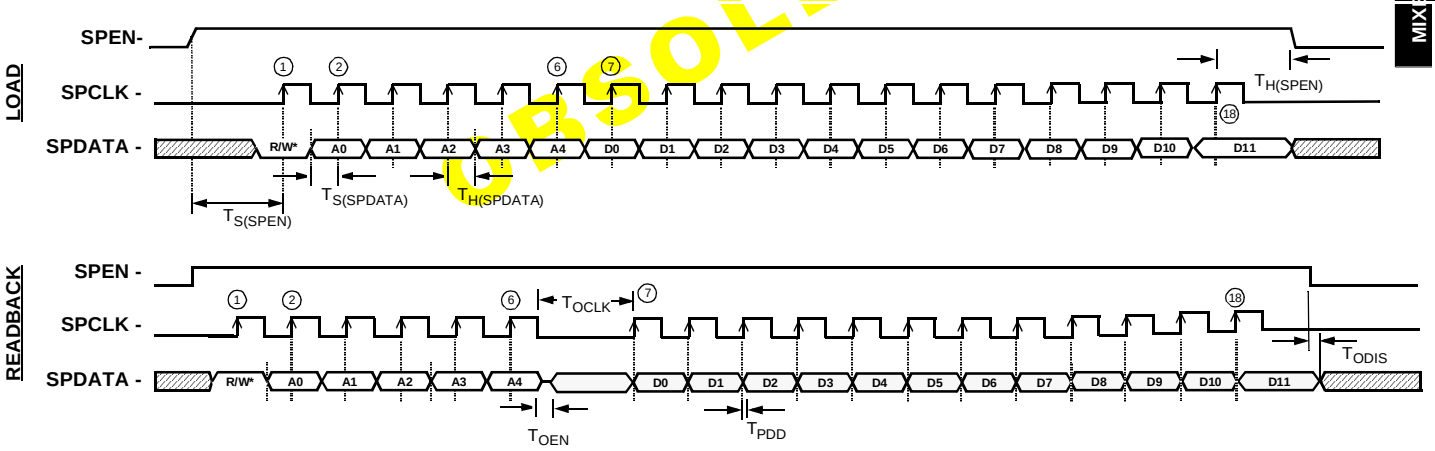

Figure 147 Serial Interface Load & Readback Timing

Table 190Programmable Register Bit Allocation

Reg. Addr.	Data Bit											
	11	10	9	8	7	6	5	4	3	2	1	0
0	PGC: Prog. Gain Control				SQPI		FIR0: FIR Tap 0					reserved
1	IDO: I_{DO} control		DODEN	TMXSEL	RECT	TFAQ	FIR4: FIR Tap 4					reserved
2	GDH0: CTF Data Group Delay, Head 0						FIR1H0: FIR Tap 1, Head 0					
3	GDH1: CTF Data Group Delay, Head 1						FIR1H1: FIR Tap 1, Head 1					
4	LPGC: ATF lowpass Gain Cntrl			DATF	PGCEN	DHBW	FIR3H0: FIR Tap 3, Head 0					
5	BPGC: ATF Bandpass Gain Cntrl				FCLP: ATF LP Fc		FIR3H1: FIR Tap 3, Head 1					
6	LTG: ATF Low Tone Gain			STSEL		TC13	TC2	FIR2: FIR Tap 2				
7	ATFFC: ATF cutoff frequency			reserved	TRKSEL	HGSEL	SLEEP	PRST	DISOSC	DACx2	DISRST	PMBP
8	ATFT: ATF Threshold DAC			SEL1SH	ATFTST	VIT: Viterbi Threshold DAC						
9	ATFSEL: ATF Mux Select			SYMC		DAMP: Damping Ratio DAC						
10	EZCNT: Excess Zeros Count					LPFBYP	PDTST	SELTE	CLKSEL	DISFAST	COAST	PREN
11	HLD	FCH0: CTF Data Fc, Head 0						BSTH0: CTF Data Boost, Head 0				
12	CMXEN	FCH1: CTF Data Fc, Head 1						BSTH1: CTF Data Boost, Head 1				
13	ATGCH0: ATF Gain, Head 0					DOGCH0: Dropout Detector Gain, Head 0				TP1SEL: TP1 Test Mux Select		
14	ATGCH1: ATF Gain, Head 1					DOGCH1: Dropout Detector Gain, Head 1				TSEL: Test Mux Select		
15	FRQ					DAGC	DPLL	BMXEN	AGCSFC		PLLSFC	
24	AE	DZ		INTL		PML	ITW		ACTST		TWR	

Table 191Serial Register Bit Descriptions

Reg. Addr	*Bit(s)*	*Description*	*Usage*
0	5:1	FIR0: FIR Outer Tap 0, 2's complement	$K_0 = 0.0195 \cdot K_{FIR0}$ in V/V $-16 \le K_{FIR0} \le 15$
	7:6	SQPI: AGC Sampled charge pump current DAC	$I_Q = I_{QNC} \cdot K_{SQPI}$ $0 \le K_{SQPI} \le 3$, $I_{QNC} = 1.2/(20 \cdot R_{AF})$
	11:8	PGC: Programmable gain control DAC	$A_V = 2.24 + 2.8 \cdot K_{PGC}$ in V/V $0 \le K_{PGC} \le 15$
1	5:1	FIR4: FIR Outer Tap 4, 2's complement	$K_6 = 0.0195 \cdot K_{FIR4}$ in V/V $-16 \le K_{FIR4} \le 15$
	6	TFAQ: Test Fast Acquisition. Allows for testing of ultra fast decay current.	0: Normal Mode 1: Test Mode (Fast Acquisition always on)
	7	RECT: Puts ATF into Rectifier mode where the bandpass output is input directly into the low-pass, bypassing the PLL	0: Normal ATF PLL mode 1: ATF Rectifier mode
	8	TMXSEL: ATF Band-pass / Low-pass Filter Test Mode	0: Disable 1: Enable
	9	DOD: Drop Out Detect	0: Enable 1: Disable
	11:10	IDO: DropOut detector decay current control	00: 40µA 01: 60µA 10: 100µA 11: 200µA
2	5:0	FIR1H0: FIR Inner Tap 1, Head 0, 2's complement	$K_1 = (0.0195 \cdot K_{FIR1H0}) - K_{TC13}$ in V/V $K_{TC13} = 0.3125$ for TC13=0 $K_{TC13} = 0$ for TC13=1 $-32 \le K_{FIR1H0} \le 31$
	11:6	GDH0: Continuous time filter Group Delay, Head 0, 2's complement	$GD_{DC} = 0.95 \cdot K_{GDH0}$ in% $-32 \le K_{GDH0} \le 31$
3	5:0	FIR1H1: FIR Inner Tap 1, Head 1, 2's complement	$K_1 = (0.0195 \cdot K_{FIR1H1}) - K_{TC13}$ in V/V $K_{TC13} = 0.3125$ for TC13=0 $K_{TC13} = 0$ for TC13=1 $-32 \le K_{FIR1H1} \le 31$
	11:6	GDH1: Continuous time filter Group Delay, Head 1, 2's complement	$GD_{DC} = 0.95 \cdot K_{GDH1}$ in% $-32 \le K_{GDH1} \le 31$

Table 191Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
4	5:0	FIR3H0: FIR Inner Tap 3, Head 0, 2's complement	$K_3 = (0.0195 \cdot K_{FIR3H0}) - K_{TC13}$ in V/V K_{TC13} = 0.3125 for TC13=0 K_{TC13} = 0 for TC13=1 $-32 \le K_{FIR3H0} \le 31$
	6	DHBW: Disable High Bandwidth Mode of AGC. Forces FAQ to remain low. (See Figure 126 and Figure 127)	0: Normal Mode 1: Disable high bandwidth
	7	PGCEN: Programmable gain control enable for VGA. Allows the VGA gain to be adjusted through PGC DAC.	0: Normal Mode (AGC loop active) 1: Programmable Gain Mode
	8	DATF: Disable ATF. Allows ATF circuitry to be disabled and powered off.	0: ATF circuitry enabled 1: ATF circuitry disabled and powered off
	11:9	LPGC: ATF Low Pass Gain Control. Sets gain of both ATF lowpass VGA's. Used to compensate for tone difference between burst and tracking section of data.	$A_V = K_{LP} \cdot 3 \cdot (1.67 + 0.23 \cdot K_{LPGC})$ in V/V $0 \le K_{LPGC} \le 7$, K_{LP} = 3.3 in track mode K_{LP} =1.0 in trick/edit mode
5	5:0	FIR3H1: FIR Inner Tap 3, Head 1, 2's complement	$_3 = (0.0195 \cdot K_{FIR3H1}) - K_{TC13}$ in V/V K_{TC13} = 0.3125 for TC13=0 K_{TC13} = 0 for TC13=1 $-32 \le K_{FIR3H1} \le 31$
	7:6	FCLP: Cutoff Frequency of ATF Low Pass and PLL. Allows PLL loop gain and lowpass cutoff frequencies of both tones to be set in tracking mode.	00: f_C = 20kHz 01: f_C = 25kHz 10: f_C = 30kHz 11: f_C = 35kHz
	11:8	BPGC: ATF bandpass gain control. Allows VGA following both bandpass outputs to be set to compensate for tone level differences between track f0 and tracks f1/f.	$A_V = K_{BP} \cdot (2.2 + 0.45 \cdot K_{BPGC})$ in V/V $0 \le K_{BPGC} \le 15$, K_{BP} = 2.0 in track/edit mode K_{BP} =1.0 in trick mode
6	4:0	FIR2: FIR Center Tap 2	$K_2 = (0.0195 \cdot K_{FIR2}) + K_{TC2}$ in V/V K_{TC2} =1.094 for TC2=0 K_{TC2} =0.7 for TC2=1 $0 \le K_{FIR2} \le 31$
	5	TC2: Tap Centering, 2nd tap. Controls gain offset in FIR center tap (tap 2).	0: Normal Mode$1.09 < K_2 < 1.7$ 1: Test Mode$0 < K_2 < 0.7$
	6	TC13: Tap Centering, 1st and 3rd taps. Controls gain offset in FIR taps 1 and 3.	0: Normal Mode$-0.937 < K_1, K_3 < +0.293$ 1: Test Mode$-0.625 < K_1, K_3 < +0.605$
	8:7	STSEL: Servo tone select. Selects servo tone to be compared against ATF threshold. Comparator output appears on STXT pin. Also defines the user mode as tracking, insert, or trick and adjusts the VGA gains and ATF PLL and lowpass bandwidth.	00 None Track +6dB +10dB Lo 01 Low Trick 0dB 0dB Hi 10 High Trick 0dB 0dB Hi 11 Both Edit +6dB 0dB Hi
	11:9	LTG: Low Tone Gain. Sets Gain of VGA following low tone bandpass VGA. Allows channel response difference between the two tones to be compensated for.	$A_V = 1.15 + 0.164 \cdot K_{LT}$ in V/V $0 \le K_{LTG} \le 7$

Table 191Serial Register Bit Descriptions

Reg. Addr	*Bit(s)*	*Description*	*Usage*
7	0	PMBP: Path Memory Bypass. Allows the path memory to be bypassed in the Viterbi detector.	0: Normal Viterbi Path length 1: Viterbi Path Length = 0
	1	DISRST: Disable DLL Filter Reset. ATF filter caps never reset when = 1.	0: Enable Reset 1: Disable Reset
	2	DACX2: Double Offset Cancellation Range. Double range of DISOSC from 0 to ±60mV to 0 to ±120mV.	0: Disable 1: Enable
	3	DISOSC: ATF Offset Cancellation. Offset cancellation at lowpass VGA output.	0: Enable 1: Disable
	4	PRST: Programmable Reset. Allows internal flip flops to be reset for test purposes. A '1' forces a reset, a '0' releases the reset.	0: Normal Mode 1: Resets flip flops
	5	SLEEP: Enables low power sleep mode.	0: Normal (Powered On) Mode 1: Power Off Mode
	6	HGSEL: High Gain Select. Allows timing recovery charge pump g_m and PMULT gain P to stay at the higher acquisition values in tracking mode.	0: Normal Mode 1: Acq. g_m and K_P used in Tracking Mode
	7	TRKSEL: Tracking Select. Forces the timing gradient in acquisition mode to that used in tracking mode.	0:Normal Mode 1:Tracking mode timing gradient used in acquisition mode
	11:9	ATFFC: ATF bandpass and lowpass cutoff frequency DAC, 2's complement.	See Table 187
8	6:0	VIT: Viterbi threshold DAC	$VIT_{TH} = 0.047 + 0.376\left(\frac{K_{VIT}}{127}\right)$ in Volts $0 \le K_{VIT} \le 127$
	7	ATFTST: AFT Test Mode. Disables variable delay cell in PLL allowing external clock to vary phase (provided CLKSEL=1).	0 = Normal Mode 1 = ATF Test Mode, variable delay disabled
	8	SEL1SH: Selects current reference for ATF 1-shot	0: 1-shot current from 0 TC voltage reference 1: 1-shot current from TR VCO
	11:9	ATFT: ATF threshold DAC. Sets threshold level for comparator whose output appears on STXT pin.	$V_{TH} = V_{RMX} \cdot \left(1 + \frac{K_{ATFT}}{4}\right)$ $0 \le K_{ATFT} \le 7$

Table 191Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
9	6:0	DAMP: Damping Ratio DAC	$P = K_P \cdot \left(\frac{127 - K_{DAMP}}{127}\right)$ $= \frac{P}{2}\sqrt{\frac{K_{VCO}K_{PD}C}{Ig_m}}$ $0 \le K_{DAMP} \le 127$ K_P= P-multiplier gain K_{VCO} = VCO gain K_{PD}= Phase detector gain (PFD in non-data mode, DDPD in data mode) C = Value of external capacitor C_{TR} I = I-multiplier gain g_m = QPUMP gain
	8:7	SYMC: Symmetric Control: Determines which if any of the taps will be symmetrically adjusted. See FIR Filter/Equalizer on page 18 for details.	00: (1 & 3) symmetric 01: (0 & 4) symmetric 10: (1 & 3) & (0 & 4) symmetric 11: no taps symmetric
	11:9	ATFSEL: ATF Mux Select. Selects various analog signals to be Muxed into the ATFOCP/N pins.	See Table 192
10	0	PREN: Power Reduction Enable. Allows the FIR, Viterbi and Decision-directed phase detector (DDPD) to power off in write mode and idle mode.	0: All blocks powered on in write/idle mode 1: FIR/Viterbi/DDPD powered off in write/idle mode
	1	COAST: Disables phase detector in timing recovery loop allowing the loop to coast through a drop-out	0: Phase detector enabled (Normal Mode) 1: Phase detector disabled (Coast Mode)
	2	DISFAST: Disable DLL Fast Acquisition. Fast acquisition sets DLL to High Bandwidth for 70ms after PLLN goes low in track mode.	0: Enable Fast Acquisition 1: Disable Fast Acquisition
	3	CLKSEL: Clock Select. Allows external FDSP/N input to replace timing recovery VCO.	0: TIming Recovery VCO (Normal Mode) 1: External FDSP/N input
	4	SELTE: Selects timing error output as either the DDPD output or AC coupled filter output, which typically is set by the RLZ/RFSR input through LPFBYP.	0: DDPD Timing Error (Normal Mode) 1: AC Coupled filter output (Test Mode)
	5	PDTST: Phase Detector Test. Allows AC coupled filter output to be input directly into decision directed phase detector input, bypassing the FIR. When used with LPFBYP allows external DC signal on RLZ and RFSR to be used as DDPD inputs	0: Normal Mode 1: Bypass FIR
	6	LPFBYP: Low Pass Filter Bypass. Allows differential test signal to be input after the internal AC Coupling Caps. The differential test signal is input on the RLZ and RFSR pins at a level >2V.	0: Normal Mode 1: Test Mode (lowpass filter bypassed)
	11:7	EZCNT: Excess zeros count.	$EZC = K_{EZCNT}$ $0 \le K_{EZCNT} \le 31$

Table 191Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
11	4:0	BSTH0: Continuous time filter Boost, Head 0	See Figure 132 on page 15
	10:5	FCH0: Cutoff Frequency of continuous time LPF for Head 0	$f_c = (0.2 \cdot K_{FCH0} + 5) \cdot \frac{6}{R_{AF}}$ in MHz $0 \le K_{FCH0} \le 63$, R_{AF} in kΩ
	11	HLD: Hold mode for AGC and timing recovery loops.	0: Normal operation. 1: Both AGC and timing recovery loops forced into a hold (coast) mode. Intended for coasting over thermal asperities.
12	4:0	BSTH1: Continuous time filter boost, Head 1	See Figure 132 on page 15
	10:5	FCH1: Cutoff frequency of continuous time LPF for Head 1	$f_c = (0.2 \cdot K_{FCH1} + 5) \cdot \frac{6}{R_{AF}}$ in MHz $0 \le K_{FCH1} \le 63$, R_{AF} in kΩ
	11	CMXEN: CMOS test point muxes enable	0: CMOS Test Muxes disabled (Normal Mode) 1: CMOS Test Muxes enabled
13	2:0	TP1SEL: Selects which internal to MUX out to the TP1 test point	See Table 192
	6:3	DOGCH0: Dropout Gain Control, Head 0	$A_V = 3.3(1 + K_{DOGCH0})$ in V/V $0 \le K_{DOGCH0} \le 15$
	11:7	ATGCH0: ATF gain control, Head 0	$A_V = 4.0 + 1.33 \cdot K_{ATGCH0}$ in V/V $0 \le K_{ATGCH0} \le 31$
14	2:0	TSEL: Output test mux select.	See Table 193
	6:3	DOGCH1: Dropout Gain Control, Head 1	$A_V = 3.3(1 + K_{DOGCH1})$ in V/V $0 \le K_{DOGCH1} \le 15$
	11:7	ATGCH1: ATF gain control, Head 1	$A_V = 4.0 + 1.33 \cdot K_{ATGCH1}$ in V/V $0 \le K_{ATGCH1} \le 31$

Table 191Serial Register Bit Descriptions

Reg. Addr	*Bit(s)*	*Description*	*Usage*
15	1:0	PLLSFC: PLL sync field count: Determines how many bytes of data rate clock pass, after AGC has timed out, before PLL signal and tracking mode begins	00: 0 bytes 01: 1 byte 10: 2 bytes 11: 3 bytes
	3:2	AGCSFC: AGC sync field count: Determines how many bytes of data rate clock pass, after DO has dropped, before AGC signal begins.	00: 4 bytes 01: 5 bytes 10: 7 bytes 11: 9 bytes
	4	BMXEN: Bipolar test point muxes enable	0: Bipolar Test Muxes disabled (Normal Mode) 1: Bipolar Test Muxes enabled
	5	DPLL: Allows the internal PLL signal to be programmably enabled/disabled for test purposes. PLL is asserted at the transition from acquisition mode to tracking mode	0: PLL count enabled (Normal Mode) 1: PLL count disabled
	6	DAGC: Allows the internal AGC signal to be programmably enabled/disabled for test purposes. AGC is asserted once the AGC count is reached in the Sync Field	0: AGC count enabled 1: AGC count disabled
	11:7	FRQ: Timing Recovery VCO Frequency Adjust DAC	f_{tr} =
24	2:0	TWR: Tap Weight Rollover value: Determines which of the FIR taps will be adapted by determining which tap gets adapted following Tap 3. The adaption sequence order of the taps is fixed, only the starting point is changed (see Viterbi Detector on page 22 for more details).	00: Tap order 0, 4, 1, 3, 0, 4,1, 3 etc. 01:.Tap order 4, 1, 3, 4, 1, 3, 4 etc. 10: Tap order 1, 3, 1, 3, 1, 3 etc. 11: Tap order 3, 3, 3, etc.
	3:2	ACTST: Adaption Control Test: Allows the adaption circuitry to be tested by forcing either an up, down or hold signal. See FIR Filter/Equalizer on page 18 for details.	0: Normal operation 1: Up forced 2: Down forced 3: Hold forced

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Table 191Serial Register Bit Descriptions

Reg. Addr	*Bit(s)*	*Description*	*Usage*
	5:4	ITW: Initial Tap Weight: Determines which tap the adaption routine will adapt first (see Viterbi Detector on page 22 for more details).	00: Tap 0 01:.Tap 4 10: Tap1 11: Tap 3
	6	PML: Path Memory length. Allows Viterbi path length to be increased to 21 from 10	0: Viterbi Path Length = 10 1: Viterbi Path Length = 21
	8:7	INTL: Integration Length: Determines the number of cycles the adaption circuit will integrate over when deciding whether the current tap weight should be incremented, decremented or held (see Viterbi Detector on page 22 for more details).	00:12 cycles 01:15 cycles 10:18 cycles 11: 21 cycles
	10:9	DZ: Dead Zone: Determines the threshold as a percentage of integration length that the adaption integrator must exceed in either the up or down direction to qualify an increment or decrement decision. If this threshold is not reached then the current tap weight is simply held (see Viterbi Detector on page 22 for more details).	00: 35% 01: 50% 10: 65% 11: 80%
	11	AE: Adaption Enable: Enables the adaption circuitry	0: Adaption circuit NOT active 1: Adaption circuit enabled

TEST MODES

There are seven sets of test points used in the VM65011. Pins TP1P/N, TP2P/N, and ATFOCP/N are differential analog test outputs, pins TP3P/N and TP4P/N provide differential digital pseudo ECL test outputs, and pins CT1 and CT2 are digital CMOS test outputs. TP1, TP2, TP3, and TP4 are activated by control register enable bit BMXEN, while CT1 and CT2 are activated by enable register bit CMXEN. The TP1 output is controlled by the TP1SEL[2:0] control register bits. TP2,3,4 and CT1 and CT2 are controlled by bitsTSEL[2:0], as shown in Table 192 and Table 193. The ATFOCP/N pins are used for the ATFOC signal under normal operation but can be used as a test point controlled by control register bits ATFSEL[2:0]. The ATFOC mux can also be routed through the TP1 Mux with a TP1SEL setting of '111'. A description of the signals used in the tables is given in Table 194. The LPFBYP register bit when set to a '1' allows an differential input signal applied to the RLZ and RFSR pins to be input to the datapath after the continuous time filter AC coupling capacitors. This allows a signal to be input directly in the FIR. The voltage level for both RLZ and RFSF must be kept above 2V to keep the normal RLZ and RFSF biasing circuitry from turning on. The PDTST bit allows the FIR to be bypassed and the test signal input directly into the decision directed phase detector (DDPD). The SELTE bit allows this test signal to be input at the Timing Error output of the DDPD for purposes of testing the charge pump and PMULT. Register bits TC2 and TC13 shift the gain of FIR taps 2 and 1 and 3 as shown in Table 184.

Table 192TP1 and ATF Test MUX Decode

BMXEN	*TP1SEL[2:0] bits*			*mode*	*Output pin*		*ATFSEL[2:0] bits*			*mode*	*Output pin*
	2	*1*	*0*		*TP1 (diff analog)*		*2*	*1*	*0*		*ATFOC Mux Output (diff analog)*
1	0	0	0	0	CTF ac		0	0	0	0	ATFSUM
1	0	0	1	1	VGA Out		0	0	1	1	VGA In
1	0	1	0	2	Vit Sig Odd		0	1	0	2	VGAD Out
1	0	1	1	3	Vit Sig Evn		0	1	1	3	VGATF Out
1	1	0	0	4	Held Sig Odd		1	0	0	4	BP_{LT}
1	1	0	1	5	FIR Out		1	0	1	5	BP_{HT}
1	1	1	0	6	VCO Control		1	1	0	6	LP_{LT}
1	1	1	1	7	ATFOC Mux		1	1	1	7	LP_{HT}
0	X	X	X	X	power down.						

Table 193Test Mode Register Decode

BMXEN	*CMXEN*	*TSEL[2:0] bits*			*mode*	*Output pins*				
		2	*1*	*0*		*TP2 (diff analog)*	*TP3 (PECL)*	*TP4 (PECL)*	*CT1 (CMOS)*	*CT2 (CMOS)*
1	1	0	0	0	0	Held Sig Evn	ZX_{LT}	ZX_{HT}	CIN_{HT}	CLK_{HT}
1	1	0	0	1	1	Timing Error	CLK_{HIP}	SCLK	LZDEL	FRDEL
1	1	0	1	0	2	VGA Out	f_{ATF}	f_{TR}	HLDEL	RGDP
1	1	0	1	1	3	Vit Sig Odd	MX	T0	RST_{LT}	RST_{HT}
1	1	1	0	0	4	CTF	YHB/YLB	XPB/XNB	AGCN	PLLN
1	1	1	0	1	5	CTF ac	TRUP	TRDN	CIN_{LT}	CLK_{LT}
1	1	1	1	0	6	Int_ε	ε_n	C_n	EA	SHGN
1	1	1	1	1	7	Vit Sig Evn	X_O	X_E	CPK_{LT}	CPK_{HT}
0	1	X	X	X	X	power down	power down	power down	modes 0-7	modes 0-7
1	0	X	X	X	X	modes 0-7	mode 0-7	mode 0-7	power down	power down

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Table 194 Test Signal Descriptions

Test Signal Name	*Description*
CTF ac	AC coupled output of the Continuous Time Filter
VGA Out	Analog output of the Variable Gain Amplifier of the AGC loop
Vit Sig Evn	The even FIR interleave input to the Viterbi detector
Held Sig Odd	Held signal value for the odd interleave of Viterbi detector
FIR Out	Output of the Finite Impulse Response filter
VCO Control	Analog control input to the Timing Recovery VCO
ATFSUM	ATF composite low/high tone bandpass filter output.
VGA in	Analog input to the Variable Gain Amplifiers of the AGC loop, Dropout Detector, and ATF
VGAD Out	Output of Dropout detector VGA
VGATF Out	Output of ATF input VGA
BP_{LT}	Output of ATF low tone Bandpass after the VGA's
LP_{LT}	ATF low tone low pass filter output
BP_{HT}	Output of ATF high tone Bandpass after the VGA
LP_{HT}	ATF high tone low pass filter output
CLK_{H1P}	ATF offset cancellation clock
EA	TBD
Held Sig Evn	Held signal value for the even interleave of Viterbi Detector
Timing Error	Timing error for the Timing Recovery Loop
Vit Sig Odd	The odd FIR interleave input to the Viterbi detector
CTF	Output of the Continuous Time Filter
Int_$\mathcal{E}$	Integrated lms tap weight error
ZX_{LT}	Zero-cross signal of ATF low tone analog signal input (bandpass VGA output)
ZX_{HT}	Zero-cross signal of ATF high tone analog signal input (bandpass VGA output)
DIV15	f_{VCO} signal divided by 15
SCLK	f_{TR} signal divided by 2 used as a sampling clock in the Timing Recovery and Viterbi sections
f_{TR}	Timing recovery clock equal to the VCO (or external clock) divided by 2
f_{ATF}	ATF frequency, equal to the VCO (or external clock) output
MX	FIR mux0 to mux1 transition
T0	FIR track and hold 0 control signal
YHB/YLB	AGC pump up (=0) / down (=1) in sampled mode, qualified by XPB/XNB signal = 1
XPB/XNB	AGC positive/negative sample sign indicator. Equivalent to (X1 xor X2)
TRUP	Pump up signal into the charge pump of the Timing Recovery loop in Idle mode
TRDN	Pump down signal into the charge pump of the Timing Recovery loop in Idle mode

Table 194 Test Signal Descriptions

Test Signal Name	*Description*
ε_n	Sign of the PR4 equalization error estimate
C_n	Sign of the Channel data
X_O	Odd sample sign indicator for decision-directed phase detector in the timing recovery
X_E	Even sample sign indicator for decision-directed phase detector in the timing recovery
CLK_{LT}	ATF clock input to low tone PLL multiplier
CLK_{HT}	ATF clock input to high tone PLL multiplier
LZDEL	One-shot pulse which controls how long the AGC loop stays in low impedance mode
FRDEL	One-shot pulse which controls how long the AGC loop stays in fast acquisition mode
HLDEL	HOLD control signal for the AGC loop
RGDP	Read signal. Internal control signal which is delayed from FRDEL by two bytes after a dropout, and delayed from RG by two bytes after RG switches high.
RST_{LT}	ATF PLL low tone control voltage reset signal
RST_{HT}	ATF PLL high tone control voltage reset signal
AGCN	Internal control signal indicating when the AGC loop switches from the continuous time loop to the sampled time loop (active low).
PLLN	Internal control signal indicating when the timing recovery loop switches from decision- directed acquisition mode to decision-directed tracking mode (active low).
SHGN	Internal control signal indicating when the AGC loop is in the high-gain sampled mode, equal to the exclusive NOR of AGCN and PLLN (active low)
SIXT	6T Detector output. Goes high after 4 or 8 6T cycles have been detected.
CIN_{LT}	ATF low tone PLL clock input equal to f_{VCO} clock divided by 45
CPK_{LT}	Output of low-tone variable delay block
CIN_{HT}	ATF high tone PLL clock input equal to f_{VCO} clock divided by 30
CPK_{HT}	Output of high-tone variable delay block

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PIN FUNCTIONS AND DESCRIPTIONS

Table 195VM65011 Pin Functions and Descriptions

PIN TYPE	PIN NAME	PIN#	INFORMATION
Power Pins	VCC1	3	CT filter, analog AGC, analog test mux power
	VCC2	40	FIR filter, Viterbi detector, timing recovery power
	VCC3	15	ATF power
	VCC4	34	Timing recovery VCO analog power
	VCC5	21	Test point ECL output and TTL input power
	VCC6	59	Internal digital CMOS and tub connection power
	VCC8	37	Viterbi digital CMOS and tub connection power
	VDD	47	3.3/5 V CMOS interface circuitry power
Ground Pins	VEE1	4	CT filter, analog AGC, analog test mux ground
	VEE2	39	FIR, Viterbi detector, timing recovery ground
	VEE3	16	ATF ground
	VEE4	33	Timing recovery VCO analog ground
	VEE5	20	Test point ECL output ground
	VEE6	58	Internal digital CMOS ground
	VEE7	38	Bipolar substrate connection
	VEE8	36	Viterbi digital CMOS ground
	VSS	46	3.3/5 V CMOS interface circuitry ground
5V Bipolar TTL Inputs	FREF	22	41.85 MHz input reference frequency

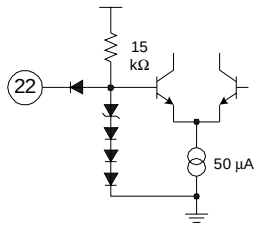


Table 195VM65011 Pin Functions and Descriptions

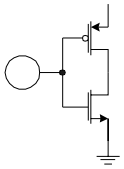
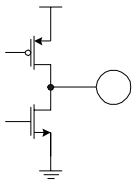
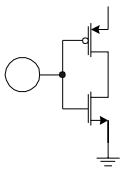
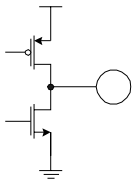
PIN TYPE	PIN NAME	PIN#	INFORMATION	
3.3/5V CMOS TTL Inputs	ADPHLD	48	Adaptive FIR Hold (active high)	
	RG	49	Read Gate. Selects Read mode (active high)	
	LP	50	Long Play. Selects Long Play mode (active high)	
	HDSEL	51	Head Select. Low selects Head 0 registers, high selects Head 1 registers, transition initiates head switch sequence	
	PD	52	Power down control signal. When this signal is asserted, the chip is powered down. (active high)	
	SPCLK	53	Serial port clock (latch on positive edge)	
	SPEN	54	Serial port I/O enable (active high)	
3.3/5V CMOS Outputs	CLCK	41	Recovered Clock.	
	DATA	42	Recovered Data.	
	XZ	43	eXcess Zeros. High level indicates number of consecutive zeros in recovered data has exceeded a programmable value.	
	DO	45	Drop Out indicator. High level indicates tape drop out.	
	STXT	44	Servo Tone eXceeds Threshold. High or low tone is selected via serial interface and compared against programmable threshold. Results of comparison is output on this pin.	
5V CMOS Bidirectional Inputs/Outputs	SPDATA	55	Bid-directional serial port data signal	
5V CMOS Outputs	CT1	56	CMOS Test Output 1	
	CT2	57	CMOS Test Output 2	

Table 195VM65011 Pin Functions and Descriptions

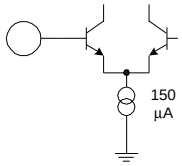
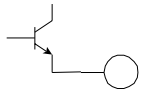
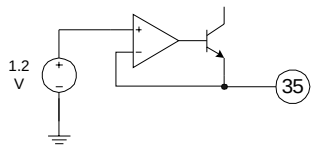
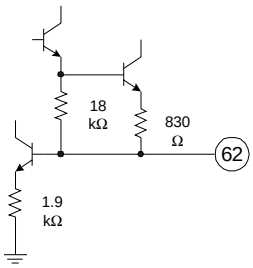
PIN TYPE	PIN NAME	PIN#	INFORMATION	
Pseudo ECL Differential Inputs	FDSP FDSN	29 30	Timing Recovery (Data Separator) test Frequency input	
Pseudo ECL Differential Outputs, V_{CC} referenced	TP3P TP3N	23 24	Digital Bipolar Test point 3 output	
	TP4P TP4N	27 28	Digital Bipolar Test point 4 output	
External Resistor Connections	RTR	35	Timing Recovery PLL reference resistor. An external resistor is connected from this pin to VEE4 (pin 33) to establish a precise internal reference current for the timing recovery VCO center frequency. 2kΩ ±10%.	
	RAF	62	AGC and CT Filter reference resistor. An external resistor is connected from this pin to VEE1 (pin 4) to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency, AGC charge pump currents, and Dropout Detector decay current. 6kΩ ±10%.	

Table 195VM65011 Pin Functions and Descriptions

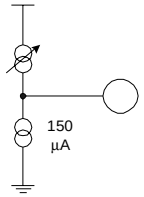
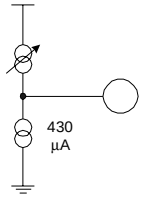
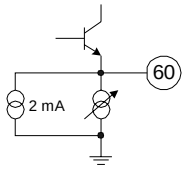
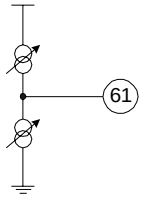
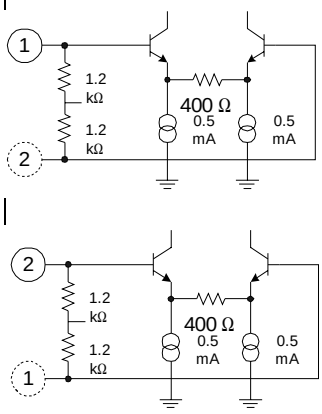
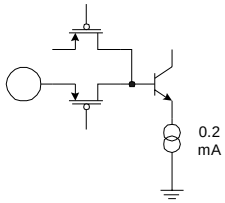
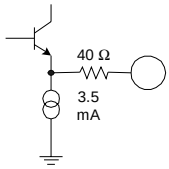
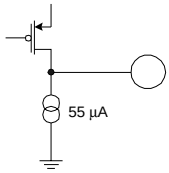
PIN TYPE	PIN NAME	PIN#	INFORMATION	
External Capacitor Connections	CHTP CHTN	18 19	ATF high tone DLL loop filter capacitor. Nominal differential connection of 390 pF.	
	CLTP CLTN	25 26	ATF low tone DLL loop filter capacitor. Nominal differential connection of 390 pF.	
	CTRP CTRN	31 32	Timing Recovery PLL loop filter. Nominal differential connection of 4.7 nF.	
	CDO	60	Dropout time constant capacitor, nominally 1600pF to VEE1 (pin 4).	
	CAGC	61	AGC Gain capacitor, nominally 820 pF to VEE1 (pin 4).	

Table 195VM65011 Pin Functions and Descriptions

PIN TYPE	PIN NAME	PIN#	INFORMATION
Analog Differential Inputs	DIP DIN	1 2	Analog Read Data input 
	TINN TINP	63 64	Analog Test Input 
Analog Outputs	TP1P TP1N	5 6	Differential analog test point 1 output 
	TP2P TP2N	7 8	Differential analog test point 2 output
	ATFOCP ATFOCN	9 10	ATF input bandpass filter output and analog test point.
	DIFREF	13	Differential reference bias for STDIF (pin 14). Nominal output value of 1.5V.
	STDIF	14	Servo Tone Differential output. Indicates amplitude difference between high and low tone servo filters relative to a 1.5V common-mode bias. STDIF is higher than DIFREF if the low servo tone's amplitude is greater than the high servo tone's amplitude. Nominal output range is 0.75 V to 2.25 V. Tone levels are equal if STDIF=DIFREF=1.5V. 

AC and DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: 0°C < T_A < 70°C, 4.5V < V_{CC} < 5.5V, 3.0V < V_{DD} < 3.6V

Overall

Conditions unless otherwise specified: R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ, R_{TR}=2.5kΩ, BMXEN=0, WD R_L=500Ω

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	Powerdown Mode, DATF=1			500	µA
		Read Mode			190	mA
		Idle Mode, PREN=0 PREN=1			190 115	mA mA
V_{DD} Supply Current	I_{DD}				10	mA
Standby to fully functional recovery time	T_{REC}	AGC within 10% final value, Filter cutoff within 10% final value.			TBD	µs

CMOS Digital I/O (CLCK, DATA, XZ, STXT, DO, ADPHLD, WG, RG, HDSEL, PD, SPCLK, SPEN, SPDATA, CT1, CT2)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	V_{IN} = V_{CC}, V_{IN} = V_{EE}			±10	µA
Output High Voltage	V_{OH}	I_{OH}=4mA, (SPDATA,CT1,CT2)	2.7			V
		I_{OH}=4mA, CLCK,DATA,XZ,DO	V_{DD}-1.0V			
Output Low Voltage	V_{OL}	I_{OL}=4mA			0.5	V
Output Leakage Current	I_{OZ}	Output Disabled, V_{OUT} =V_{EE}, 2.7V (SPDATA only)			± 10	µA
Input Capacitance	C_{IN}				10	pF
Output Capacitance	C_{OUT}				10	pF

TTL Inputs (WDI, FREF)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			20	µA
Input Low Current	I_{IL}	V_{IL} = 0.5V			-0.6	mA

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ECL I/O (FDSP, FDSN, WDP, WDN, TP3P, TP3N, TP4P, TP4N)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Common Mode Input Voltage	V_{CM}		V_{CC}-2.8V		V_{CC}	V
Differential Input Voltage	V_D		200			mV
Input Current	I_{IIN}	$V_{IH}=V_{CC}$			10	µA
Output High Voltage	V_{OH}	R_L=50Ω to V_{CC}-2V, T=27°C	V_{CC}-1.3	V_{CC}-1.08		V
Output Low Voltage	V_{OL}	R_L=50Ω to V_{CC}-2.45V, T=27°C		V_{CC}–1.58	V_{CC}–1.3	V
Differential Output Swing	V_{diff}	$I_{OL}=I_{OH}\approx$18mA	400	450	500	mV
Output Leakage Current	I_{OZ}	Output disabled, $V_{OUT}=V_{EE}$, V_{CC}			±200	nA

Gain Control

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ,

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Dynamic Range	V_{DI}	V_{DI} = (V_{DIP} –V_{DIN})	30		300	mV_{ppd}
Input Common Mode Voltage	V_{CMDI}	V_{CMDI} = (V_{DIP} +V_{DIN})/2	V_{CC}–3.1	V_{CC}-2.7	V_{CC}–2.3	V
Differential Input Resistance	$R_{in(DA)}$	LOWZ = Low, WG='0'	1.2	2.5	3.8	kΩ
		LOWZ = High, WG='1'	120	250	380	Ω
Single-ended input Resistance	$R_{in(SA)}$	LOWZ = Low, WG='0'	0.6	1.25	1.9	kΩ
		LOWZ = High, WG='1'	60	125	190	Ω
VGA Minimum Gain	A_{Vmin}	A_V=(V_{VGAP} -V_{VGAN})/V_{DI} V_{CAGC}=0.8V, PGCEN=0			4.0	V/V
VGA Maximum Gain	A_{Vmax}	A_V=(V_{VGAP} -V_{VGAN})/V_{DI} V_{CAGC}=3.2V, PGCEN =0	39	47		V/V
VGA Gain in PGC mode	A_V	A_V=(V_{VGAP} -V_{VGAN})/V_{DI}, PGCEN=1 PGC= 0000 PGC= 0001 PGC= 0011 PGC= 0111 PGC= 1111		2.24 5.0 10.6 21.8 44.5		V/V
Output Common Mode Voltage	V_{VCM}	V_{CM} = (V_{VGAP} +V_{VGAN})/2	V_{CC}–3.2	V_{CC}-2.5	V_{CC}–1.8	V
CAGC Common mode Voltage	V_{CM}		0.8	2.0	3.2	V
Output Offset Voltage	V_{OS}	V_{OS}=(V_{VGAP} -V_{VGAN}), over entire gain range, Test Mode 2	–50		50	mV
Output Distortion	THD	V_{DI} = 30-300mV_{ppd}, V_{VGA}≤0.75V_{ppd}, 1-20MHz 1st, 2nd, and 3rd harmonics only			1.0	%

OBSOLETE

MIXED SIGNAL CIRCUITS

AGC Loop

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{FSR}=20kΩ, R_{LZ}=20kΩ. For Charge Pump Current tests: LPFBYP='1',TFAQ='0', V_{CAGC}=1.2V, WG='0', RG='0'

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RAF Pin Voltage	V_{RAF}		1.16	1.2	1.24	V
RAF Current Range	I_{RAF}	$I_{RAF}=V_{RAF}/R_{AF}$	36	200	310	µA
RFSR Pin Voltage	V_{RFSR}		1.24	1.28	1.31	V
RFSR Current Range	I_{RFSR}	$I_{RFSR}=V_{RFSR}/R_{RFSR}$	30	64	130	µA
RLZ Pin Voltage	V_{RLZ}		1.24	1.28	1.31	V
RLZ Current Range	I_{RLZ}	$I_{RLZ}=V_{RLZ}/R_{LZ}$	30	64	130	µA
Fast Discharge Current, Continuous Mode	I_{QFD}	$V_{RLZ}=V_{CC}$-1.0V $V_{FSR}=V_{CC}$-0.6V $I_{QFD}=144\cdot I_{QNC}$	$0.8\cdot I_{QFD}$	I_{QFD}	$1.2\cdot I_{QFD}$	mA
Normal Discharge Current, Continuous Mode	I_{QND}	$V_{RLZ}=V_{CC}$-0.9V $V_{FSR}=V_{CC}$-0.6V $I_{QND}=18\cdot I_{QNC}$	$0.8\cdot I_{QND}$	I_{QND}	$1.2\cdot I_{QND}$	µA
Normal Charge Current, Continuous Mode	I_{QNC}	$V_{RLZ}=V_{CC}$-0.8V $V_{FSR}=V_{CC}$-0.6V $I_{QNC}=I_{RAF}/20$	$0.8\cdot I_{QNC}$	I_{QNC}	$1.2\cdot I_{QNC}$	µA
Ultra Fast Charge Current, Continuous Mode	I_{QUFC}	$V_{RLZ}=V_{CC}$-0.6V $V_{FSR}=V_{CC}$-0.6V, Set TFAQ to '0', pause and set TFAQ='1' $I_{QUFC}=160\cdot I_{QNC}$	$0.8\cdot I_{QUFC}$	I_{QUFC}	$1.2\cdot I_{QUFC}$	mA
Fast Charge Current, Continuous Mode	I_{QFC}	With device in ultra fast charge condition, set $V_{RLZ}=V_{CC}$-1.0V, $V_{FSR}=V_{CC}$-0.6V, pause and set $V_{RLZ}=V_{CC}$-0.6V, $V_{FSR}=V_{CC}$-0.6V $I_{QFC}=9\cdot I_{QNC}$	$0.8\cdot I_{QFC}$	I_{QFC}	$1.2\cdot I_{QFC}$	µA
Low Gain Charge Pump Current, Sampled Mode	I_{QL}	$V_{RLZ}=V_{CC}$-0.465V $V_{FSR}=V_{CC}$-0.6V, RG='1', PDTST='1', DPLL='0', CLKSEL='1' $I_{QL}=I_{QNC}\cdot K_{SQPI}$	$0.8\cdot I_{QL}$	I_{QL}	$1.2\cdot I_{QL}$	µA
High Gain Charge Pump Current, Sampled Mode	I_{QH}	same conditions as I_{QL}, DPLL='1' $I_{QH}=I_{QNC}\cdot(6+K_{SQPI})$	$0.8\cdot I_{QH}$	I_{QH}	$1.2\cdot I_{QH}$	µA
Charge Pump Leakage current	I_{LK}	HLD='1'			±200	nA
Output dynamic range	V_{FA}	$V_{FA}=(V_{FAP}-V_{FAN})$ $30mV_{ppd} \le V_{DI} \le 300mV_{ppd}$ $1MHz < f_{in} < 20MHz$	0.45		0.55	V_{ppd}
LOWZ One-shot Pulse Width	T_{LZ}	HDSEL or WG transition $T_{LZ}=0.075\cdot R_{LZ}$	$0.8\cdot T_{LZ}$	T_{LZ}	$1.2\cdot T_{LZ}$	µs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSR One-shot Pulse Width	T_{FSR}	HDSEL, WG, or DO transition $T_{FSR}=0.075 \cdot R_{LZ}$	$0.8 \cdot T_{FSR}$	T_{FSR}	$1.2 \cdot T_{FSR}$	µs
Trailing edge of LOWZ to V_{FN} stable to 10%	T_{WR}	C_{AGC} =820pF			500	ns
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW=15MHz $V_{DIP} = V_{DIN}$			10	$nV/\sqrt{Hz}$
Gain settle from –30% V_{DI} step	T_{GSD}	$V_{FN} \geq 0.9 \cdot$(final value) in normal acquisition mode		20	25	µs
Gain settle from +30% V_{DI} step	T_{GSA}	$V_{FN} \leq 1.1 \cdot$(final value) in normal acquisition mode			1.5	µs
VGA Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = A_{Vmax}, f_{in} = 5MHz, $V_{DIP} = V_{DIN} = 100mV_{pp}$	40			dB
Power supply rejection ratio	$PSRR_G$	gain = A_{Vmax}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =$100mV_{pp}$	45			dB
AGC Gain Sensitivity to CAGC voltage	AV_{PV}	(Typical range is 1.4V to 2.8V)		17.5		dB/V
LOWZ extension time	T_{LZE}				500	ns
[1]K_{SQPI} is the value of the sampled charge pump current control register word SQPI(1:0).						

Dropout Detector

Conditions unless otherwise specified: C_{DO}=1600pF, R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input dynamic range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$	30		300	mV_{ppd}
VGA Gain	A_{Vmax}	$A_V=(V_{DRP} - V_{DRN})/V_{DI}$, ATFOCP/N DOGC= 0000 DOGC= 0001 DOGC= 0011 DOGC= 0111 DOGC= 1111		 3.3 6.6 13.2 26.4 52.8		V/V
VGA Output Common Mode Voltage	V_{CM}	$V_{CM} = (V_{DRP} + V_{DRN})/2$	V_{CC}-3.0	V_{cc}-2.3	V_{CC}-1.6	V
VGA Output Offset Voltage	V_{OS}	$V_{OS}=(V_{DRP} - V_{DRN})$, over entire gain range for V_{DI}=0V_{ppd}	-50		50	mV
Output distortion	THD	V_{DI} = 30-300mV_{ppd}, V_{DR} < 2.4V_{ppd}, 1-20MHz 1st, 2nd, and 3rd harmonics only			1.0	%
CDO Output Common Mode Voltage	V_{CDOCM}	V_{DI}=0V_{ppd}	V_{CC}-2.9	V_{CC}-2.6	V_{CC}-2.3	V
CDO Decay Current	I_{DO}	I_{DO} = 40, 60, 100, 200 µA, $V_{CDO}=V_{CDOCM}$+0.5V	0.9·I_{CDO}		1.1·I_{CDO}	µA
Dropout Threshold	V_{THDO}	Measure V_{CDO} when DO switches high	0.215	0.24	0.265	V_p
	ΔV_{THDO}	Increase in V_{THDO} when DO switches low (hysteresis)	20	25	30	mV_p
Dropout Delay	T_{DOD}	IDO=00 IDO=01 IDO=10 IDO=11	8.5 5.6 3.4 1.7	10 6.6 4.0 2.0	11.5 7.6 4.6 2.3	µs
Dropout Recovery Delay	T_{DOREC}	Time from V_{DI} switched high to DO switched low, all I_{DO} currents			TBD	ns
Input referred noise voltage	V_{IRN}	gain =A_{Vmax}, BW=15MHz $V_{DIP} = V_{DIN}$			10	nV/√Hz
VGA Bandwidth	BW	All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = A_{Vmax}, f_{in} = 5MHz, $V_{DIP} = V_{DIN}$ = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = A_{Vmax}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB

Continuous Time Low-Pass Filter/Equalizer

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Dynamic Range	V_{VGA}	V_{FN}<600mV$_{ppd}$	0.1	0.7	1.0	V_{ppd}
Filter cutoff frequency	f_C	f_C=(0.15·K_{FC}+5.0)·I_{RAF}	0.9·f_C	f_C	1.1·f_C	MHz
Normal lowpass gain (V_{FN} vs. V_{FI})	A_{ON}	BST=0, K_{FC}=0, f_{in} = 0.1f_C	-5.0	-3.2	-2.2	dB
Boost accuracy	BA		-1		+1	dB
Filter Boost (low end)	AB_{min}	BST=0		0	0.5	dB
Filter Boost (mid point)	AB_{mid1}	BST=8		0	0.5	dB
Filter Boost (mid point)	AB_{mid2}	BST=20	5.5	6.5	7.5	dB
Filter Boost (high end)	AB_{max}	BST=31	12.0	13.0	14.0	dB
Filter Output Offset	V_{OSFN}	V_{FI} = 0.0V, FNP/N outputs	–200		200	mV
AC coupled filter output offset	V_{OSFA}	V_{FI} = 0.0v, FAP/N outputs	–10		10	mV
Group Delay	T_{GD}	K_{FC}=63, GD=0	27	32	37	ns
Group Delay Variation	T_{GD}	0.1 $f_C \le f_{in} \le$ 1.5 f_C, 5MHz $\le f_C \le$ 15MHz, BST=0, GD=0	–2.0		2.0	%
	T_{GD2}	0.1 $f_C \le f_{in} \le$ 1.5 f_C, 5MHz $\le f_C \le$ 15MHz, BST=31, GD=0	–2.5		2.5	%
Group delay variation nonsymmetric zeros	T_{GD3}	DC @ FNP/N outputs. GD=-32, relative to GD=0	–32		-28	%
	T_{GD4}	DC @ FNP/N outputs. GD=+31, relative to GD=0	28		32	%
Normal output noise voltage	V_{NN}	BW = 100MHz, f_C = 10MHz [1] V_{DIP} = V_{DIN}			TBD	mV_{rms}
Common mode rejection ratio	$CMRR_F$	f_{in} = 5MHz, K_{FC}=63, V_{DIP} = V_{DIN} = 100mV$_{pp}$	40			dB
Power supply rejection ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV$_{pp}$	40			dB
Total harmonic distortion (V_{FN} vs. V_{FI})	THD_F	f_{in} = 0.67f_C, K_{FC}=63, $V_{FI} \le$ 0.7V_{ppd}, 2nd and 3rd harmonics only			1.5	%
Filter settle from step in Fc and BOOST	T_{FS}	K_{FC} or BST step to V_{FN} settle		85	300	ns

[1] K_{FC}=63, BST=31 (boost level of 13dB).

FIR Filter/Equalizer

Conditions unless otherwise specified: TC2=0, TC13=0, $K_{0,4}$ = 0, $K_{1,3}$=16, LPFBYP='1', CLKSEL='1'. Inputs on RLZ and RFSR. f_{TR} > 20MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Nom. Center Tap Gain	A_{Vc}	K_2=8	1.15	1.25	1.3	V/V
Center Tap Gain Variation	DA_{Vc}	K_2=8, Apply a 0.2V D.C. signal measure the gain for eight successive channel samples, compute min vs. max percentage	0	1.0	1.5	%
Nom. Center Tap Offset	OFF_C	K_2=8		3	5	mV
Center Tap offset variation	OFF_V	Same as OFF_C		5	10	mV
Tap Gain & Linearity	TG	Average tap gain per step	17.5	19.5	21.5	V/V
	A_{V2}	K_2=31. Maximum voltage gain of center tap 2		1.699		V/V
	$A_{V0,4}$	$K_{0,4}$=15. Maximum voltage gain of taps 0 and 4		0.1367		V/V
	$A_{V1,3}$	$K_{1,3}$=31. Maximum voltage gain of taps1 and 3		0.293		V/V
Differential non-linearity	DNL			5		mV/V
Integral non-linearity	INL			19.8		mV/V
TH Droop	DAV	Average droop 0.25 v diff [1]			30	V/µs
Center tap Large Signal Bandwidth	LSBW	K_2=8, K_1=K_3=16, 0.5V_{ppd} [1] swept over frequency range		TBD		MHz
Center tap Small Signal Bandwidth	SSBW	K_2=8, K_1=K_3=16, 0.05V_{ppd} [1] swept over frequency range		TBD		MHz
Center tap distortion	$MX2^{nd}$	Set the input to 0.5v_{ppd} @ 31/128*F_S with F_S set to max data rate, center tap only [1]			-35	dBc
	$MX3^{rd}$				–35	dBc
	MXTHD				-30	dBc
Max EQ distortion	$MX2^{nd}$	Same as center tap distortion. with amplitude set to 0.17V_{ppd} Max peaking [2]			-35	dBc
	$MX3^{rd}$				–35	dBc
	MXTHD				-30	dBc
TH Droop	DAV	Average droop 0.25 v diff [1]			30	V/µs
Center tap Large Signal Bandwidth	LSBW	K_2=8, K_1=K_3=16, 0.5V_{ppd} [1] swept over frequency range		TBD		MHz
Center tap Small Signal Bandwidth	SSBW	K_2=8, K_1=K_3=16, 0.05V_{ppd} [1] swept over frequency range		TBD		MHz

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Center tap distortion	$MX2^{nd}$	Set the input to $0.5v_{ppd}$ @ 31/128*F_S with F_S set to max data rate, center tap only [1]			-35	dBc
	$MX3^{rd}$				–35	dBc
	MXTHD				-30	dBc
Max EQ distortion	$MX2^{nd}$	Same as center tap distortion. with amplitude set to $0.17V_{ppd}$ Max peaking [2]			-35	dBc
	$MX3^{rd}$				–35	dBc
	MXTHD				-30	dBc
Noise	η_{CT}	Center tap only [1]		TBD		$V_{rmsd}/\sqrt{Hz}$
	η_{MX}	Max peaking [2]		TBD		$V_{rmsd}/\sqrt{Hz}$
2T boost at $F_S/4$ [3]	MXB_{2T}	K_1 & K_3 set to -32, Vin $=0.1V_{ppd}$, K_2=8			1.91	V/V
	MNB_{2T}	K_1 & K_3 set to 31, Vin $=0.1V_{ppd}$, K_2=8	-0.6			V/V
4T boost at $F_S/4$ [1,3]	MXB_{4T}	$K_0=K_4=16$			0.64	V/V
	MNB_{4T}	$K_0=K_4=5$	-0.6			V/V
[1] Set taps K_2=8 & K_1/K_3 = 16 & K_0/K_4 = 0 [2] Set taps K_2=31, K_1/K_3=-32 & K_0/K_4=15						
[1]These tests should be done at the highest device clock rate.						

FIR Adaptation Circuit

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Integration Slope	IS	ACTST = 3. Observe Int_τ. Set all tap weights to zero except tap 3, which is set to unity. Supply an external CLK and a 4T pattern as shown in the diagrams that follow. Adjust the phase of the CLK relative to the FIR IN signal to create integrate up, down and hold conditions as shown. Measure integrated signal peak relative to reset value and normalize to integration length (12 for INTL='00').				
	IS_U	Integrate up condition		1.15		mV/ns
	IS_D	Integrate down condition		1.15		mV/ns
Integration length	INT_L	Use the conditions for the error integration slope up measurement. For each value of the integration length, measure the time for each cycle of the Int_ε output, and normalize to the CLK period. Subtract 12 cycles to determine the true integration length.				
	IL_{00}	INTL='00'		12		cycles
	IL_{01}	INTL='01'		15		cycles
	IL_{10}	INTL='10'		18		cycles
	IL_{11}	INTL='11'		21		cycles

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Zone Threshold	DZ_{TH}	Use the conditions for the error integration slope up measurement. Set ACTST = 0. Set the FIR TAP 3 weight to mid-scale (zero). Using an external current source to emulate the resistor on RTR, vary the integration slope, starting from zero. For each step in integration slope, perform an adaption of Tap 3. Increase the integration slope until Tap 3 changes. Measure the integration signal peak value. Repeat for integrate down conditions.				
	DZU_{00}	DZ= ‘00’		108		mV
	DZU_{01}	DZ= ‘01’		166		mV
	DZU_{10}	DZ= ‘10’		219		mV
	DZU_{11}	DZ= ‘11’		276		mV
	DZD_{00}	DZ = ‘00’		108		mV
	DZD_{01}	DZ= ‘01’		166		mV
	DZD_{10}	DZ=’10’		219		mV
	DZD_{11}	DZ=‘11’		276		mV

Viterbi Detector

Conditions unless otherwise specified: RG='1', LPFBYP='1', PDTST='1'.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Sliding Window Over-write Voltage	V_{OW}	On each interleave Input series of same-polarity full-height pulses on RLZ/RFSR. Increase height of final pulse by $V_{OW.}$ Observe DATA. Pulse prior to large pulse should get overwrit-ten and DATA='0'. Test both polarities of signal with 1-10 (PML='0') and 1-21 (PML='1') intervening zeros between 1's of same polarity. Repeat for each interleave.	15			mV
Excess Zero Count Delay	T_{EZC}	$X=(0.5+K_{EZC})T_{TR}$ where T_{TR} is the timing recovery clock period[1]	X+2	X	X+20	ns
6T Detector Delay	T_{6T}	$X=(10+6\cdot K_{STL})T_{TR}$ where T_{TR} is the timing recovery clock period[2]. measured from FIR out-put to SIXT test point.	X+2	X	X+20	ns
Viterbi Threshold	VIT_{TH}	$VIT_{TH}=0.047+0.376\cdot(K_{VIT}/127)^3$ Input series of full height pulses on RLZ/RFSF. Reduce height of 1 pulse, vary K_{VIT} while observ-ing DATA. When runt pulse is lower than the threshold, DATA will drop to '0.' Repeat for both interleaves		VIT_{TH}		V
Viterbi Threshold Mini-mum	VIT_{MIN}	$K_{VIT}=0$	0.02	0.023	0.028	V
Viterbi Threshold Maxi-mum	VIT_{MAX}	$K_{VIT}=127$	0.200	0.211	0.222	V
Viterbi Threshold DAC differential nonlinearity	VIT_{DNL}	Worst case step size deviation from ideal			0.047	V
Viterbi Threshold DAC integral nonlinearity	VIT_{IN}	Slope of VIT_{TH} vs. VIT_{DAC}			1	lsb
PLLP 0-to-1 Transition to Path Memory Set released.					TBD	ns

[1] K_{EZC} is the value of the excess zeros count control register word EZC(4:0)
[2] K_{STL} is the value of the STL 6T length control register bit, 0 (4cycles) or1 (8 cycles)
[3] K_{VIT} is the value of the Viterbi Threshold control register word VIT(6:0)

Timing Recovery Loop

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RTR Pin Voltage	V_{RTR}		1.21	1.25	1.28	V
RTR Current Range	I_{RTR}		200	500	645	µA
VCO Reference Current	I_{REF}	$I_{REF}=I_{RTR}=V_{RTR}/R_{TR}$		I_{REF}		mA
VCO Frequency	f_{VCO}	$f_{VCO} = f_0 \cdot (1+k_V(I \cdot \Delta V_{TR} + P \cdot \Delta V_{PD})$		f_{VCO}		MHz
VCO Center Frequency	f_0	$f_0 = k_I \cdot I_{REF}$ [1]	$0.9 \cdot f_0$	f_0	$1.1 \cdot f_0$	MHz
VCO Gain	k_V	Measured at TP4P/N, K_{DAMP}= 127 [2]	0.35	0.4	0.45	V^{-1}
Imult Gain	I		0.9	1.0	1.1	A/A
Pmult Gain (VCO Cntl/Tmg Err.)	P	P=1.0(127-K_{DAMP})/127, Idle/Acq. P=0.25(127-K_{DAMP})/127, Tracking, TRGAIN=0 P=0.5(127-K_{DAMP})/127,Tracking, TRGAIN=1, CTRP=CTRN	0.8·P	P	1.2·P	V/V
VCO Dynamic Range	$f_{dr(VCO)}$	2% R_{TR}	±5			%
CTRP/N CM Voltage	V_{CM}		2.20	2.30	2.40	V
CTRP/N Leakage	I_{LCTR}	COAST='1'			±200	nA
TR Charge Pump Gain (I_{QP}/Timing Error)	I_{TRQP}	Idle/Acquisition Mode	345	460	575	µA/V
		Tracking Mode: TRGAIN = 0	35	46	60	µA/V
		TRGAIN = 1	70	92	120	µA/V
Timing Error Offset	$OFF\tau_E$	LPFBYP='1', PDTST='1', RFSR/RLZ inputs set to +180mV_{ppd}, -180mV_{ppd},and 0mV_{ppd}			±5	mV
Sliced Threshold Voltage	V_{TSL}	LPFBYP='1', PDTST='1', CLKSEL='1', Vary differential voltage on RFSF/RLZ inputs, observe X_e and X_o	80	90	100	mV
Closed Loop Jitter	σ_F	VCO output, sample size=100,000 samples		100		ps

[1] k_I is 167.4 MHz/mA
[2] K_{DAMP} is the value of the Damping Ratio DAC DAMP(6:0), [0 to 127]

Automatic Tracking Frequency

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Dynamic Range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$	30		300	mV_{ppd}

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PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VGA Gain	A_{Vmax}	$A_V=(V_{DAP}-V_{DAN})/V_{DI}$, $V_{DAP/N}$ = 1.2V_{ppd} K_{ATGC}= 00000 K_{ATGC}= 00001 K_{ATGC}= 00011 K_{ATGC}= 00111 K_{ATGC}= 01111 K_{ATGC}= 11111	 3.4 4.53 6.8 11.33 20.4 38.5	 4.0 5.33 8.0 13.33 24.0 45.3	 4.25 5.65 8.5 14.1 25.4 48.0	V/V
VGA Output Common Mode Voltage	V_{CM}	$V_{CM}=(V_{DAP}+V_{DAN})/2$	V_{CC}-3.0	V_{cc}-2.3	V_{CC}-1.6	V
VGA Output Offset Voltage	V_{OS}	$V_{OS}=(V_{DAP}-V_{DAN})$, over entire gain range	-50		50	mV
Low Tone Bandpass Center Frequency	$f_{0(BPLT)}$	f_{TR}=41.85MHz, geometric mean of 3dB BW	442	465	488	kHz
High Tone Bandpass Center Frequency	$f_{0(BPHT)}$	f_{TR}=41.85MHz, geometric mean of 3dB BW	663	697.5	732	kHz
Bandpass Q (Low Tone & High Tone)	Q_{BP}	$f_{0(BP)}$ divided by the bandwidth at the -3dB points.	4.0	4.5	5.0	
Passband Ripple	R_P			0.5	1.0	dB
Low Tone Lowpass Cutoff Frequency	$f_{C(LT)}$	ATFFC='000', STSEL='00' f_{TR}=41.85MHz, -3dB point	4.5	5	5.5	kHz
Low Tone PLL Center Frequency	$f_{0(LT)}$	ATFFC='000', f_{TR}=41.85MHz,	460	465	470	kHz
Low Tone Q	Q_{LT}	$f_{0(LT)}$ divided by the bandwidth at the -3dB points. STSEL='00'	37	47	52	
		STSEL='00'	21	23.5	26	
Low Tone Settling Time	T_{SLT}	Low tone output within 10% of final value in response to DIP/N step from 0 to normal signal level, STSEL='00'			40	µs
		STSEL='00'			20	µs
High Tone Lowpass Cutoff Frequency	$f_{C(HT)}$	STSEL='00', f_{TR}=41.85MHz, -3dB point	4.5	5	5.5	kHz
High Tone PLL Center Frequency	$f_{0(HT)}$	f_{TR}=41.85MHz, STSEL='00'	692.5	697.5	702.5	kHz
High Tone Q	Q_{HT}	$f_{0(LT)}$ divided by the bandwidth at the -3dB points. STSEL='00'	63	70	77	
		STSEL='00'	31	35	39	
High Tone Settling Time	T_{SHT}	High tone output within 10% of final value in response to DIP/N step from 0 to normal signal level, STSEL='00'			40	µs
		STSEL='00'			20	µs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
ATFOCP/N Output Level		Input level and VGATF set for maximum ATF input. ATFSEL=000		240		mV_{ppd}
ATFOCP/N Output Impedance	R_{ATFOC}			33		Ω
DIFREF Output Level	V_{DREF}		1.425	1.5	1.575	V
STDIF maximum Output Level	V_{STDIF}	Measured differentially relative to V_{DREF} with maximum signal conditions.	1.4			V
STXT Threshold	V_{THST}	VTHST=0.254·(1+0.0016·KATF)	$0.95 \cdot V_{THST}$	V_{THST}	$1.05 \cdot V_{THST}$	V

Serial Interface Timing

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SPCLK period	T		50			ns
SPEN set-up time	$T_{S(SPEN)}$	Relative to SPCLK ↑	40			ns
SPEN hold time	$T_{H(SPEN)}$	Relative to SPCLK ↑	50			ns
SPEN high to low to high			50			ns
SPDATA set-up time	$T_{S(SPD}$	Relative to SPCLK ↑	20			ns
SPDATA hold time	$T_{H(SPD)}$	Relative to SPCLK ↑	5			ns
SPDATA enable	T_{OEN}	Relative to SPCLK ↓	5			ns
SPCLK low time	T_{OCLK}	Relative to SPCLK ↓	30			ns
SPDATA disable	T_{ODIS}	Relative to SPEN ↓			30	ns
SPDATA prop. delay	T_{PDD}	Relative to SPCLK ↑			10	ns

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VM65015

ANALOG PRML CHANNEL for DIGITAL VHS APPLICATIONS

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently-variable real zeros
- Programmable five-tap transversal filter for PR4 equalization
- Analog/decision-directed AGC
- Fast timing recovery loop which locks to random data
- Track cross detector
- 6T detector
- Register programmable power management (<5 mW Power Down Mode)
- Serial interface port for access to internal configuration registers to load and verify register contents
- Single power supply (5V ±10%) with optional 3.3V CMOS output supply
- Small footprint 64-pin PQFP package

DESCRIPTION

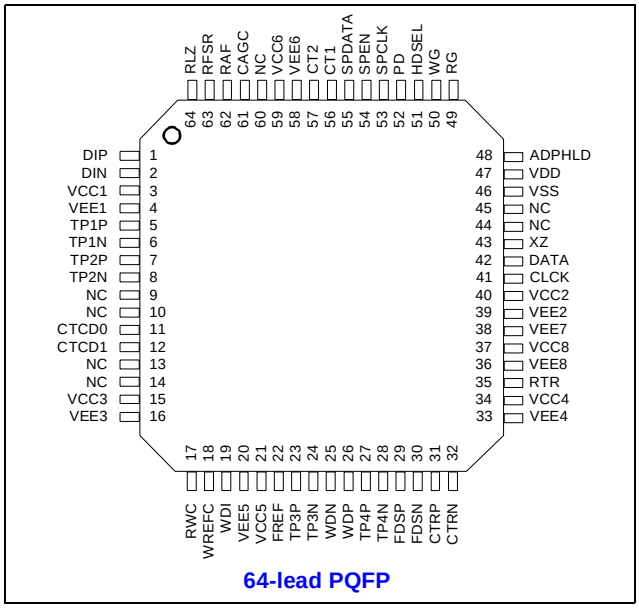
The VM65015 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement the front end of a Partial Response Class 4 (PR4) read channel for digital VHS (DVHS) applications running at 19.1385 Mbps.

Functional blocks include an AGC loop, programmable continuous time filter, sampling FIR filter, decision-directed timing recovery loop, Viterbi detector, internal 6T pattern detector, programmable threshold (read data envelope) track cross detector, programmable preamp write current reference, and a set of test multiplexers for testing various internal signals. Programmable functions such as filter cutoff/boost, FIR tap weights, etc. are controlled by writing to onboard configuration registers through a serial interface.

The VM65015 utilizes advanced BiCMOS process technology along with advanced circuit design techniques that result in a high performance device with low power consumption. The part requires a single 5V power supply and is available in a 64-Lead PQFP package. With the addition of a 3.3V supply, the VM65015 can also interface to 3.3V CMOS logic.

For additional information, call VTC.

CONNECTION DIAGRAM



64-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC} ..... -0.3V to +7V
- V_{DD} ..... -0.3V to +7V

Input Voltages
- V_{CC} referenced ..... -0.3V to (V_{CC} + 0.3V)
- V_{DD} referenced ..... -0.3V to (V_{DD} + 0.3V)

Storage Temperature T_{stg} ..... -65°C to 150°C

Junction Temperature T_J ..... 150°C

Thermal Impedance Characteristics of 64-Lead PQFP, Θ_{JA}:
- still air ..... 51°C/W
- 200 fpm air flow ..... 38°C/W
- 600 fpm air flow ..... 27°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{DD} ..... 3.3V ± 10% or +5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

External Components
- R_{WC} ..... 3.5kΩ to 12kΩ
- R_{TR} ..... 2.0kΩ to 6kΩ
- R_{AF} ..... 4.0kΩ to 32kΩ
- R_{FSR} ..... 10kΩ to 40kΩ
- R_{LZ} ..... 10kΩ to 40kΩ
- R_L ECL Outputs to V_{EE} ..... 200Ω to 1kΩ
- R_L ECL Outputs to V_{CC} -2V ..... 50Ω to 100Ω

MIXED SIGNAL CIRCUITS

BLOCK DIAGRAM AND DESCRIPTION

Automatic Gain Control

- Dual mode AGC, analog during acquisition, sampled during read data
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Externally adjustable charge pump currents
- Low-drift AGC hold circuitry
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

Low Pass Filter/Equalizer

- Programmable, 7-pole, 0.05° equiripple continuous time filter provides:
  - Channel filter and pulse slimming equalization for PR4 shaping
  - Programmable cutoff frequency from 3 to 8.5 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable group delay of ±30%
  - Minimized size and power

FIR Filter/Equalizer

- Five tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- Independent and/or dependent self adaption of tap weights
- ADP hold feature controlled by external pin or internal 6T detector

Timing Recovery

- Single external capacitor required
- Fast acquisition, sampled-data phase-locked loop which locks to random data
- Decision-directed clock recovery from data samples
- Programmable damping ratio

Maximum Likelihood Detector

- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length programmable to ten or twenty-one
- Excess zeros counter monitoring consecutive recovered data zeros to aid in tape dropout detection

6T Detector

- Serial register bit enabled
- 6T length programmable to four or eight
- Invokes FIR adaption hold when detected

Track Cross Detector (TCD)

- Attack (charge) currents limited to reject glitches
- Programmable read data envelope threshold
- Programmable decay (discharge) currents via serial registers
- Head-select-dependent TCD hold capacitors eliminate long transitions due to head differences

Write Circuitry

- Five bit programmable write current reference for preamp
- TTL to differential ECL write data level shifter

DEFINITIONS AND ABBREVIATIONS

AGC	Automatic Gain Control
Biquad	Combination of two integrator stages to produce a two-pole filter element
BiCMOS	Bipolar and CMOS technology
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CTF	Continuous Time Filter
DAC	Digital to Analog Converter
ECL	Emitter-Coupled Logic
EQ	Equalization
FET	Field Effect Transistor
FIR	Finite Impulse Response
fpm	Feet Per Minute
f_0	Center Frequency
f_c	Cutoff Frequency
f_s	Sample Frequency
g_m-C	Transconductance-capacitor integrator stage used in filter
IC	Integrated Circuit
K_V	VCO gain in MHz/V
K_{VCO}	VCO gain in Mrad/V
LPF	Low-Pass Filter
LSB	Least Significant Bit
LMS	Least Mean Squared
Mbps	Megabits per second
ML	Maximum Likelihood
MSB	Most Significant Bit
PGC	Programmable Gain Control
PLL	Phase-Locked Loop
PR	Partial Response
PRML	Partial Response Maximum Likelihood, a type of data recovery
PQFP	Plastic Quad Flat Pack
RM	Read Mode
TCD	Track Cross Detector
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VIT_{TH}	Viterbi Detector Threshold Voltage
V_{THDO}	Dropout Detector Threshold Voltage
V_{THTR}	Timing Recovery Threshold Voltage
V_{ppd}	Peak-to-Peak Differential Voltage
WM	Write Mode

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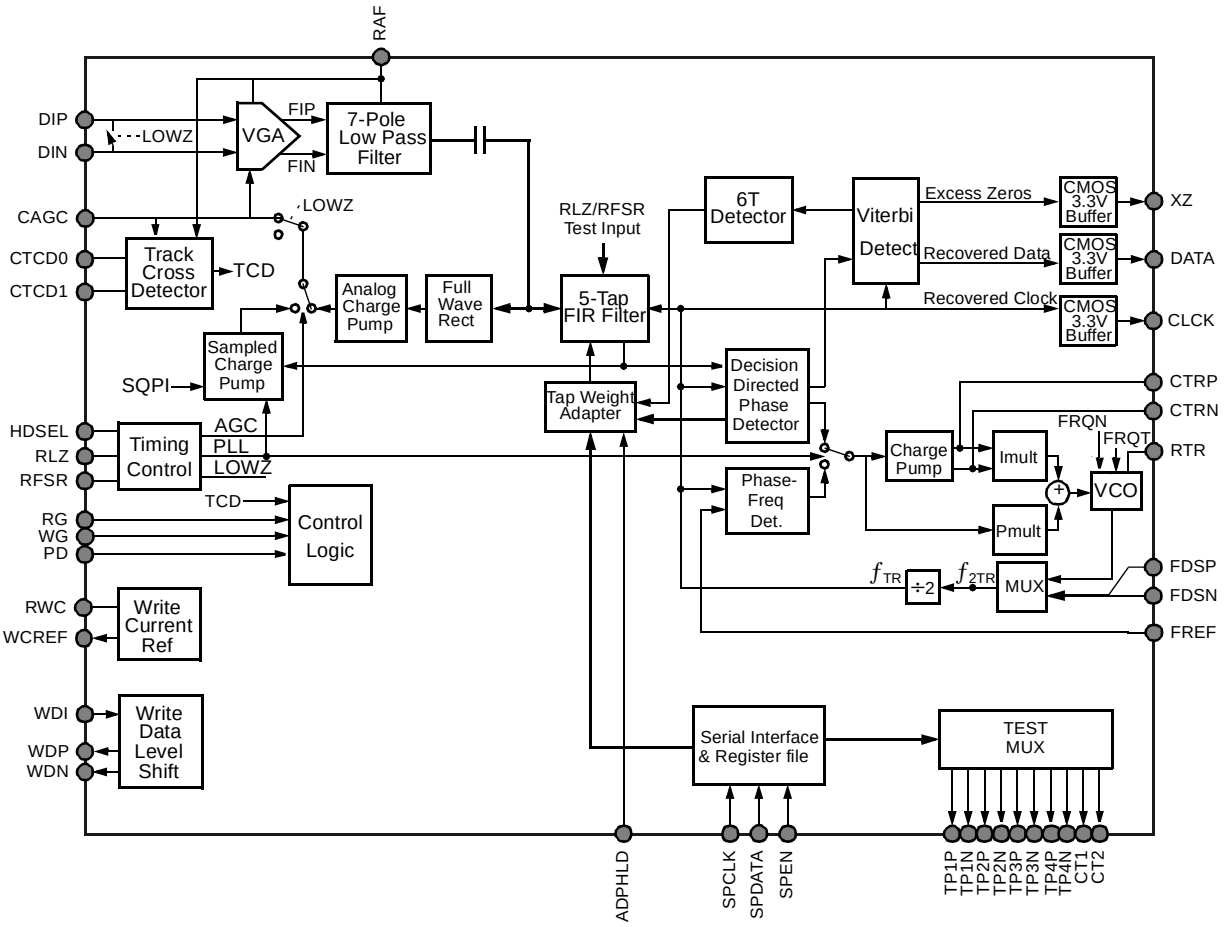


Figure 148 VM65015 Top Level Block Diagram

BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTION

The VM65015 is a high performance PR4 read channel. It includes AGC, track cross detector, programmable continuous-time filter/equalizer, programmable FIR filter/equalizer with adaptation circuitry, decision-directed clock recovery, Viterbi detector, internal 6T pattern detector, and write current reference for the read/write preamp. A three-wire serial interface configures the internal storage registers.

Gain Control

Gain Control consists of a wide-band variable gain amplifier (VGA) with an input impedance switch, a programmable continuous time filter, charge pump, amplitude detector, and exponentiator. A block diagram is shown in Figure 149. The Gain Control has two modes: automatic (AGC), and programmable (PGC) gain control. The mode of the Gain Control is selected by the PGCEN control register bit (register 4:data bit <7>): PGCEN = 0 defines the AGC mode and PGCEN = 1 defines PGC mode. Gain Control is active during read or idle modes, as defined by setting WG signal (pin 50) to '0'.

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the output of the continuous time filter while the input is allowed to vary over a 10:1 range. During signal acquisition an analog AGC loop is used to ensure quick convergence to the correct signal amplitude. In Tracking mode a sampled/decision- directed closed loop AGC is used for improved accuracy. The programmable gain control (PGC) circuit is used for test purposes to control the VGA gain with an internal DAC (0:<D8-D11>). In PGC mode the AGC loop is disabled, and the VGA gain is a linear function of the DAC count. The read signal is externally AC coupled into the VGA amplifier on the DIP/DIN (pins 1 and 2 respectively). The gain of the VGA is controlled by the voltage stored on the C_{AGC} hold capacitor. The read signal is amplified and equalized by the continuous time filter. The output of the filter, FNP/FNN, is internally AC coupled, creating the FAP/FAN signal, which connects to an amplitude detector and the FIR filter. The continuous-time AGC loop locks the differential peak-to-peak voltage at FAP/FAN to V_{FA}=0.5V_{ppd} for inputs ranging from 30-300mV_{ppd}.

Test modes are provided in which the filter outputs, FNP/FNN, and the VGA inputs and outputs, DIP/DIN, VGAP/VGAN, are multiplexed to the TP2P/TP2N output pins.

The analog AGC loop consists of the VGA, programmable continuous time filter (CTF), amplitude detector, exponentiator, and an external capacitor C_{AGC} charged by a dual rate charge pump for fast transient recovery. Charge (or decay) currents increase the capacitor voltage V_{CAGC} and increase the VGA gain while discharge (attack) currents lower the capacitor voltage V_{CAGC} and reduce the VGA gain. The magnitude of the charge pump currents are controlled by various timing signals and DAC settings. In general when a new track of data is read the part enters a fast acquisition mode (FAQ) where the loop enters a continuous AGC mode and the charge pump currents take on high (fast) values to increase the loop gain and reduce lock time. After a time-out period T_{FSR}, set by external resistor R_{FSR}, the loop enters a normal continuous AGC mode and the charge pump currents take on low or normal values. After another time-out period set by an internal counter with a programmable number of clock periods, the loop switches into a sampled high gain mode and the charge pump currents are set to their sampled high gain values. Finally a second clock-period counter switches the loop into a sampled low gain mode with a set of sampled low gain currents. Figure 150 and Figure 151 show the timing for the AGC loop and Table 197 shows the various charge pump currents referred to in the following discussion.

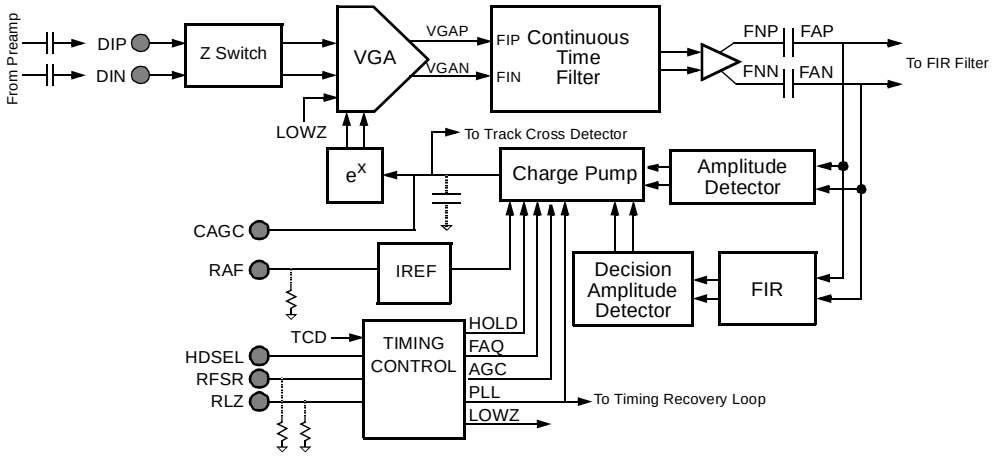


Figure 149 Gain Control Block Diagram

For the normal continuous AGC mode the normal charge current I_{QNC} charges C_{AGC} for V_{FA} < 100% of the target value. The value of I_{QNC} is set by an external resistor connected between RAF and VEE1 (pins 62 and 4), given by the following equation

$$I_{QNC} = \frac{1.2V}{20 \cdot R_{AF}} \qquad \textit{(eq. 141)}$$

R_{AF} also sets the continuous time filter cutoff frequency. For a data rate of 19.1385 MHz, R_{AF} should be set to 10kΩ. This will yield an I_{QNC} of 6µA. C_{AGC} should be set to 820pF nominally.

If 100% < V_{FA} < 125% the normal discharge current I_{QND} is active which equals18X the normal charge current as given by

$$I_{QND} = 18 \cdot I_{QNC} \qquad \textit{(eq. 142)}$$

For R_{AF}=10kΩ and I_{QND}=108µA, the normal attack rate is thus 18X the normal decay rate.

If V_{FA} > 125%, a fast discharge current I_{QFD} is active which equals 8X the normal discharge current, or 144X the normal charge current. I_{QFD} is given by

$$I_{QFD} = 8 \cdot I_{QND} = 144 \cdot I_{QNC} \qquad \textit{(eq. 143)}$$

The fast attack rate is thus 144X the normal decay rate. For R_{AF}=10kΩ I_{QFD}=864µA.

In the fast acquisition mode the charge current is increased to 9X times its normal value and the discharge current is forced to its fast value for all values of V_{FA} > 100%, not just those >125%

$$I_{QFC} = 9 \cdot I_{QNC} \qquad \textit{(eq. 144)}$$

For R_{AF}=10kΩ I_{QFC}=54µA, there is an “ultra fast” charge current I_{QUFC} equal to 160X the normal charge current. I_{QUFC} is active only on the initial charge up in the fast acquisition mode. Once V_{FA} has exceeded 100%, I_{QUFC} is disabled and if V_{FA} drops back below 100%, the fast charge current I_{QFC} will be active.

$$I_{QUFC} = 160 \cdot I_{QNC} \qquad \textit{(eq. 145)}$$

A read cycle can be initiated in one of three ways: A positive transition on RG, a positive or negative transition on HDSEL (pin 51) while RG='1', or a negative transition on the track cross detector (TCD) while RG='1.' A timing diagram for the AGC read cycle in read mode (pin RG='1') is shown in Figure 150. Shown are both transitions of HDSEL, and a TCD pulse. The HDSEL transition indicates that a new head is being used which will invariably have different characteristics from the previous head and hence the need for a new read cycle.

To avoid transients associated with the head switch being injected into the part, the part is put into a "LOWZ" mode where the VGA gain is squelched to 0, the input impedance is reduced by 10X, and the C_{AGC} voltage is held at its current value. An internal one-shot signal LOWZ defines the LOWZ mode and is initiated each time HDSEL is switched. The width of this pulse T_{LZ} is set by an external resistor, R_{LZ}, connected between RLZ and VEE1 (pins 64 and 4) as given by

$$T_{LZ} = 0.075 \cdot R_{LZ} \qquad \textit{(eq. 146)}$$

where R_{LZ} is measured in kΩ and T_{LZ} in µs.

R_{LZ} should nominally be set to 20kΩ which sets T_{LZ} to 1.5µs. After LOWZ goes low the input impedance is returned to its normal level and the VGA gain is no longer squelched. A read cycle can also be initiated by a negative transition on the TCD output indicating that a track crossing has been detected by the track cross detector (see Track Cross Detector on page 73). The track cross detector senses when the input level drops to an unacceptably small level during trick modes as the heads scan across the tracks, and switches the internal TCD signal to a '1.' There is no impedance change nor is the C_{AGC} held in this case. While TCD is high the part is put into idle mode where the PLL locks to the external frequency reference. Control register bit COAST, when set to a '1,' will disable the phase detector in idle mode, allowing the timing recovery capacitor C_{TR} to hold its value, "coasting" the loop. Upon the falling edge of TCD, a new read cycle is initiated.

With either the falling edge of LOWZ or the falling edge of TCD, the charge pump output is again enabled, allowing the loop to reacquire lock to the new data, using the C_{AGC} voltage as an initial condition. The loop then normally enters the fast acquisition mode (FAQ) where the "ultra fast" charging current I_{QUFC} increases the VGA gain at 160 times the normal decay rate until V_{FA} exceeds 100% of the target value. Thereafter, the loop response is determined by the fast charging current I_{QFC} and the fast discharging current I_{QFD}. External resistor R_{FSR} sets a time-out period T_{FSR} after which the loop will automatically switch back to the normal mode. T_{FSR} is given by

$$T_{FSR} = 0.075 \cdot R_{FSR} \qquad \textit{(eq. 147)}$$

wR_{FSR} is measured in kΩ
T_{FSR} is in µs.

R_{FSR} should nominally be set to 20kΩ which sets T_{FSR} to 1.5µs. It is the falling edge of FAQ which activates the internal READ signal, triggering a new read cycle as shown in Figure 151. Only a transition on HDSEL or a negative transition on WG (see Figure 152) will create a LOWZ condition, but the FAQ mode and subsequent read cycle occurs with either the falling edge of LOWZ or the falling edge of TCD. Figure 153 shows a read cycle initiated by the RG pin. Note that for a read to occur there must be both a falling on FAQ and the condition RG='1', the order does not matter.

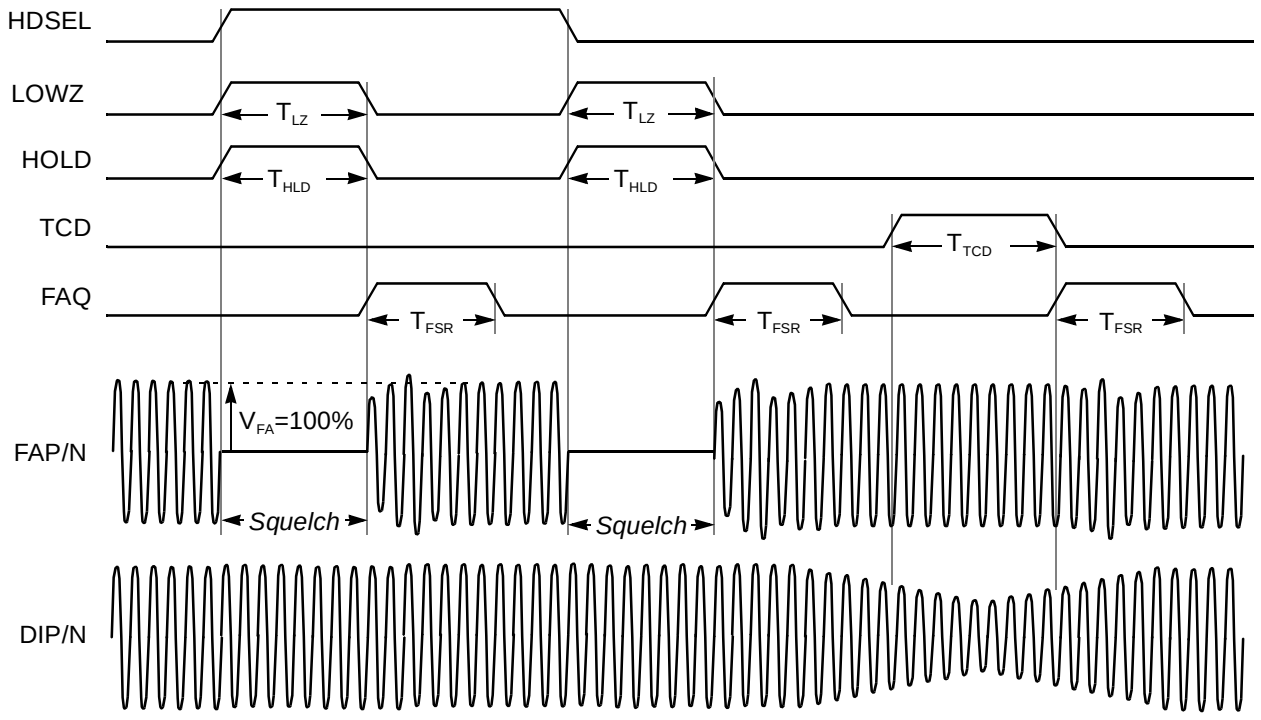


Figure 150 Read Mode AGC Timing Diagram, RG=1

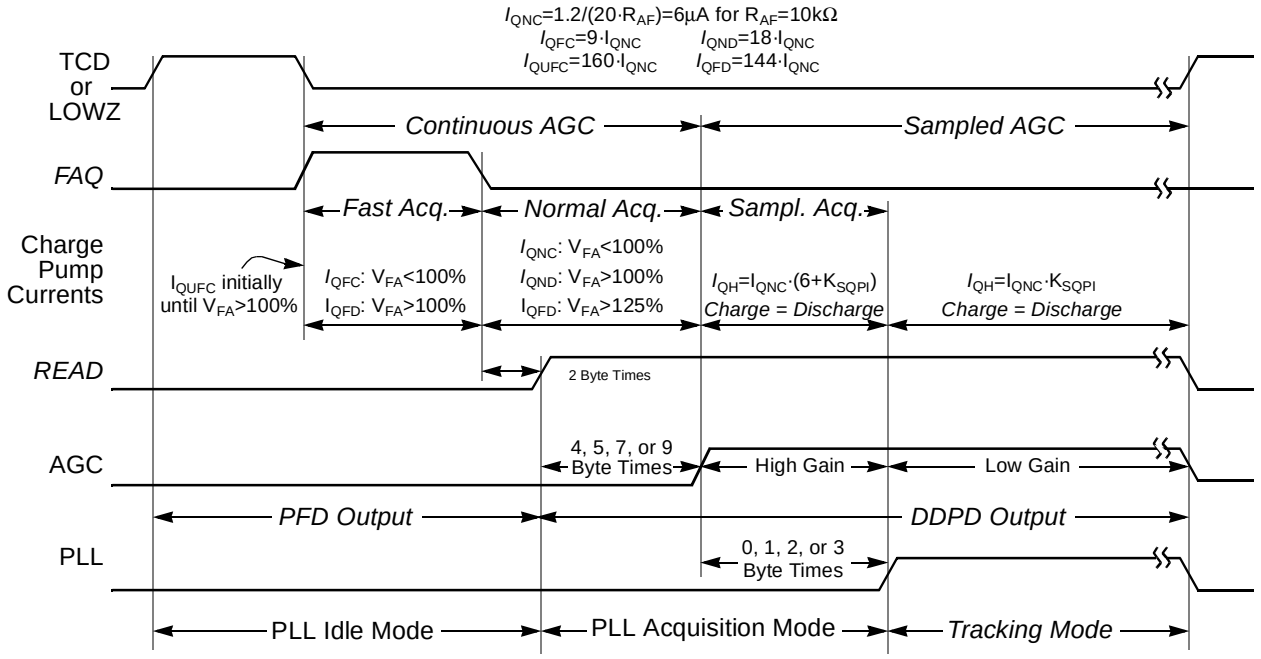


Figure 151 Read Mode Timing Diagram, RG=1

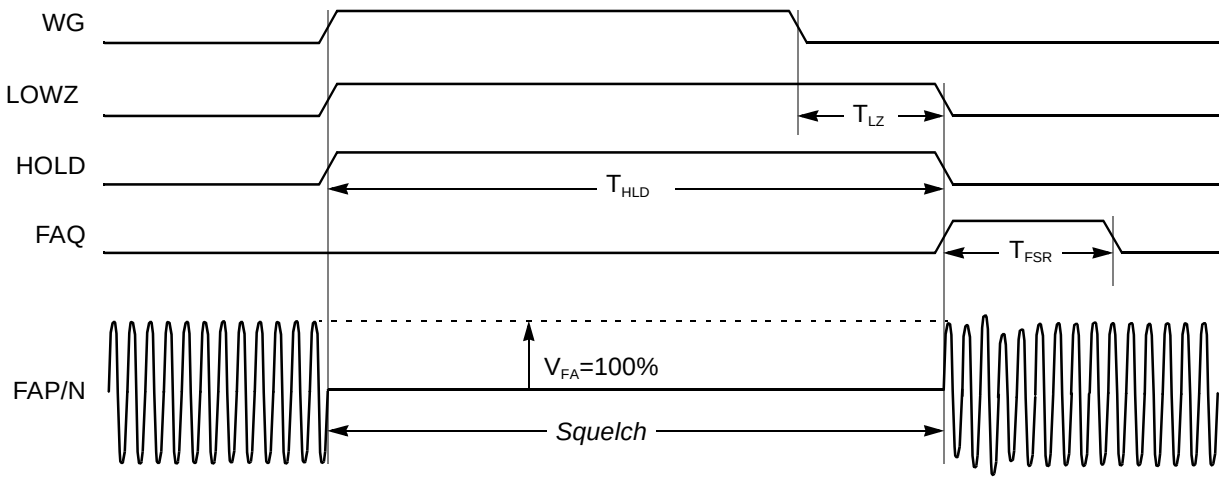


Figure 152 Write/Idle Mode AGC Timing Diagram, RG=0

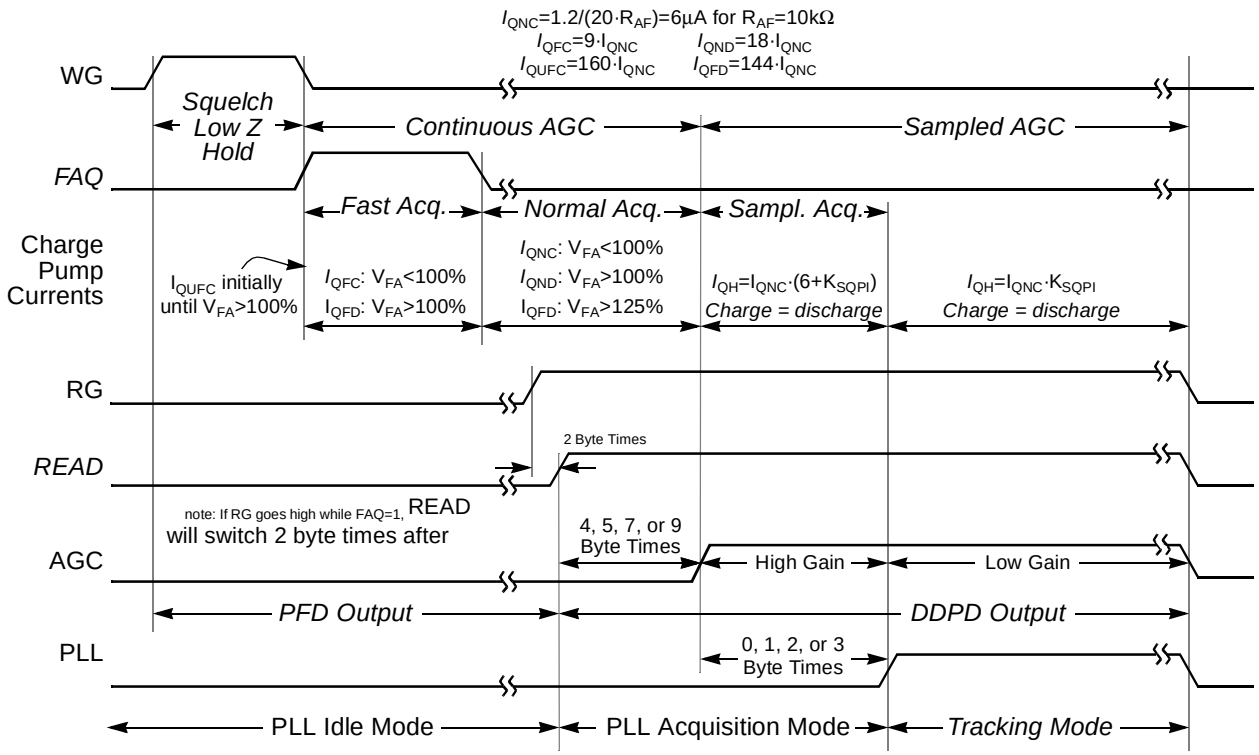


Figure 153 Write-to-Read Timing Diagram

If control register bit TFAQ is set to a '1', the loop will stay in the fast acquisition mode, ignoring the FAQ pulse and not switching to normal mode until TFAQ is set to a '0'. This is to facilitate testing of the fast acquisition mode. If serial register bit DHBW (disable high bandwidth) is set to a '1', the FAQ mode still charges initially at the "ultra fast" rate, but then switches to the normal charge and discharge currents (or fast discharge current if V_{FA} > 125% of the target value as described above) immediately without waiting for FAQ to go low, thus effectively eliminating the fast acquisition (or high bandwidth) mode. The test bit HLD when set to a '1' forces the charge pump into a hold mode.

The sampled AGC loop consists of the VGA, programmable continuous time filter, sampling 7-tap FIR equalizer, decision amplitude detector and charge pump, and exponentiator. Symmetrical charge and discharge currents are utilized in the sampled mode. A sample is considered a '1' if its amplitude exceeds 90mV (50% of 0.71·V_{FA}) otherwise it is a '0'. Sampled 0's are ignored by the loop, while

sampled 1's charge C_{AGC} when the sample is below 180mV ($0.71 \cdot V_{FA}$) and discharge C_{AGC} if the sample exceeds 180mV. The magnitude of the charge and discharge currents are equal and take on a value of I_{QH} in the high or acquisition modes; and I_{QL} in the low or tracking modes.

A falling edge FAQ while RG='1,' or a positive transition on RG initiates an acquisition sequence where the AGC and timing recovery loops will switch into a sampled mode. An acquisition counter begins on the falling edge of FAQ as shown in Figure 151, or the rising edge of 'RG' as shown in Figure 153. An internal READ signal is generated after 16 periods of the timing recovery clock have elapsed. The 16 periods are referred to as two byte times, in reference to the amount of data read during this time period if the timing recovery loop were to be already locked. The AGC loop transition into high gain sampled mode and the PLL transition into tracking mode are based on two programmable sync field counters, AGCSFC (15:<D2-D3>) and PLLSFC (15:<D0-D1>), which are started when READ transitions high. The AGC SF count is determined by one of four programmable counts of 4, 5, 7, or 9 byte times. The AGCSFC 2-bit word in the control register sets the byte count, and after counting the proper number of clock cycles, internal signal AGC transitions high and the AGC loop switches into sampled mode with the charge pump in the high gain mode (see Gain Control on page 67). Similarly, the PLL SF count is programmed by the 2-bit PLLSFC control register word to 0, 1, 2 or 3 byte times following the AGC SF count at which time Internal signal PLL goes high. At this time the sampled AGC charge pump switches to the low gain mode. The PLL transitions from idle to acquisition mode when READ goes high. The PLL remains in acquisition mode through the sum of both the AGC SF and PLL SF counts, whereupon, it transitions into the tracking mode. Table 196 shows the sync field counts and clock cycles corresponding to each AGCSFC and PLLSFC value.

Table 196Sync Field Counts

AGCSFC	AGC Sync Field Byte Count	Clock Cycles
00	4	32
01	5	40
10	7	56
11	9	72

PLLSFC	PLL Sync Field Byte Count	Clock Cycles
00	0	0
01	1	8
10	2	16
11	3	24

During write mode (RG='0', WG='1') the VGA is squelched, the impedance switch goes into the low Z state, and the AGC capacitor voltage is held, the same way that it is during a head switch. Upon the falling edge of WG the AGC loop enters the fast acquisition mode similar to the way it does in read mode when TCD goes low. The only difference is the AGC loop will stay in the normal acquisition mode and the PLL will stay locked to the reference until RG is set high, at which point the READ, AGC, and PLL signals will switch in turn similar to the way they do when TCD switches low. Write-to-Idle-to-read timing is shown in Figure 152 and Figure 153.

The sampled charge pump currents I_{QL} and I_{QH} are controlled by the SQPI(1:0) control register bits whose value is represented as K_{SQPI} and varies from 0 to 3.

$$I_{QL} = I_{QNC} \cdot K_{SQPI} \quad \textit{(eq. 148)}$$

$$I_{QH} = I_{QL} + 6 \cdot I_{QNC} = I_{QNC} \cdot (6 + K_{SQPI}) \quad \textit{(eq. 149)}$$

So, for R_{AF}=10kΩ., I_{QL}will equal 0-18µA, and I_{QH} will be to 36-54µA. The charge pump operation for all the various AGC modes is shown below in Table 197.

The VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. Equation (eq. 150) expresses the VGA normal mode gain (A_V), in Volts/Volts, as an exponential function of the control voltage on the selected CAGC (pin 61) where $A_{V(max)}$ is 46V/V and V_{CAGC} nominally ranges from1.4V to 2.8V.

$$A_V = A_{V(max)} \cdot e^{-\left(\frac{2.8V - V_{CAGC}}{0.53V}\right)} \quad \textit{(eq. 150)}$$

where A_V is in 39 V/V
V_{MAX} is the capacitor voltage at max gain (nominally 2.5V but highly process dependent).
V_{CAGCx} nominally ranges from 0.8 to 2.5V.

In the PGC mode, the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the PGC control register. The VGA has a linear gain versus DAC count and is expressed by the following equation.

$$A_V = 2.24 + 2.8 \cdot K_{PGC} \quad \textit{(eq. 151)}$$

where A_V is in V/V and K_{PGC} is the value of the PGC(3:0) control word which ranges between 0 and 15.

Note: PGC mode is used primarily for test.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Table 197AGC Charge Pump Operation

Mode	AGC Loop	Event	TFAQ	DHBW	SQPI	Discharge Current	Charge Current
LOWZ	HOLD	HDSEL ↓X	X	X	XX	0	0
HOLD	HOLD	HLD=1	XX	XX	XX	0	0
Fast Acq.	Continuous High BW	TCD ↓ LOWZ ↓ V_{FA}<100% initially	X	0	XX	0	$I_{QUFC}=160 \cdot I_{QNC}$
		V_{FA}>100%	X	0	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
		V_{FA}<100%	X	0	XX	0	$I_{QFC}=9 \cdot I_{QNC}$
	Continuous Low BW	V_{FA}<100 initially	X	1	XX	0	$I_{QUFC}=160 \cdot I_{QNC}$
		V_{FA}>100%	X	1	XX	$I_{QND}=18 \cdot I_{QNC}$	0
		V_{FA}>125%	X	1	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
		V_{FA}<100%	X	1	XX	0	$I_{QNC}=1.2/(20 \cdot R_{AF})$
Normal Acq.	Continuous	FAQ ↓ V_{FA}<100%	0	X	XX	0	I_{QNC}
		V_{FA}>100%	0	X	XX	$I_{QND}=18 \cdot I_{QNC}$	0
		V_{FA}>125%	0	X	XX	$I_{QFD}=144 \cdot I_{QNC}$	0
Sampled Acq. (HIgh Gain)	Sampled	AGC ↑	X	X	00	$I_{QH}=6 \cdot I_{QNC}$	$I_{QH}=6 \cdot I_{QNC}$
					00	$I_{QH}=7 \cdot I_{QNC}$	$I_{QH}=7 \cdot I_{QNC}$
					01	$I_{QH}=8 \cdot I_{QNC}$	$I_{QH}=8 \cdot I_{QNC}$
					10	$I_{QH}=9 \cdot I_{QNC}$	$I_{QH}=9 \cdot I_{QNC}$
Tracking (Low Gain)	Sampled	PLL ↑	X	X	00	0	0
					01	$I_{QL}=I_{QNC}$	$I_{QL}=I_{QNC}$
					10	$I_{QL}=2 \cdot I_{QNC}$	$I_{QL}=2 \cdot I_{QNC}$
					11	$I_{QL}=3 \cdot I_{QNC}$	$I_{QL}=3 \cdot I_{QNC}$

Track Cross Detector

The track cross detector is shown in Figure 154. The track cross detector is used in the trick or edit modes when the scanner and heads cross over more than one track in a revolution. It is desirable to read as much valid information from the tape in these modes so video and position information can be obtained.

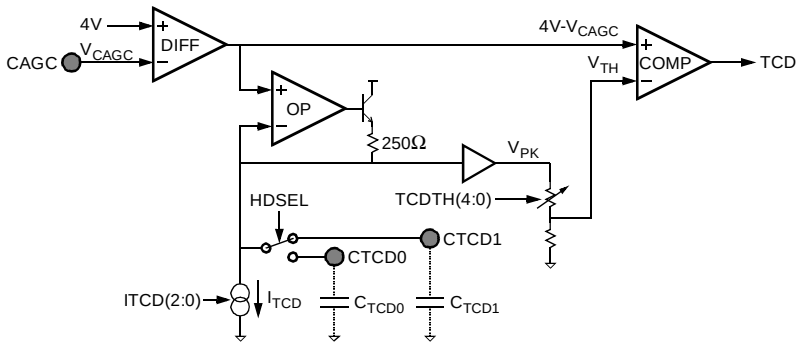


Figure 154 Track Cross Detector Block Diagram

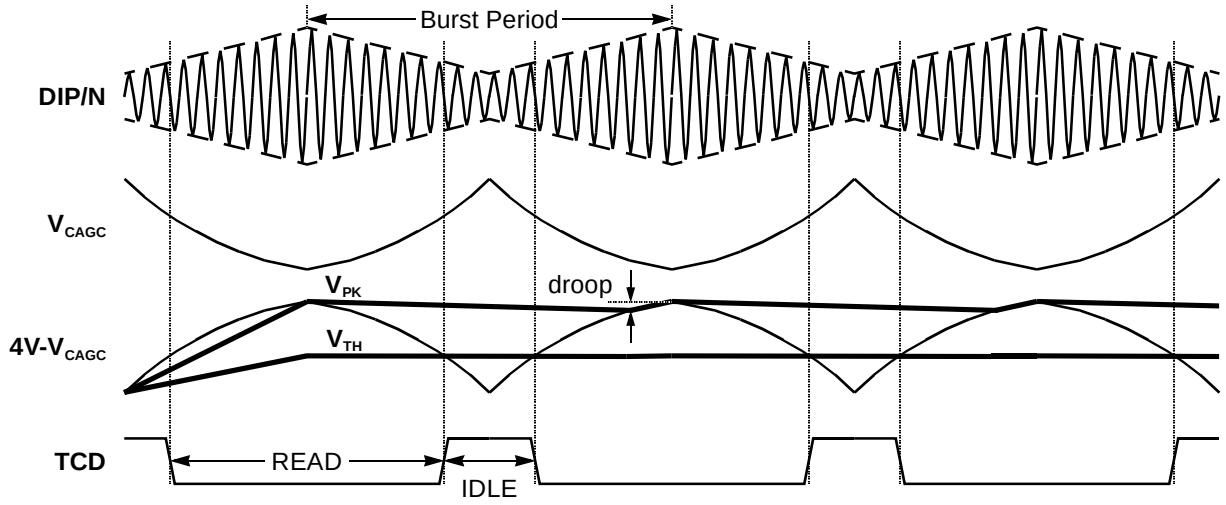


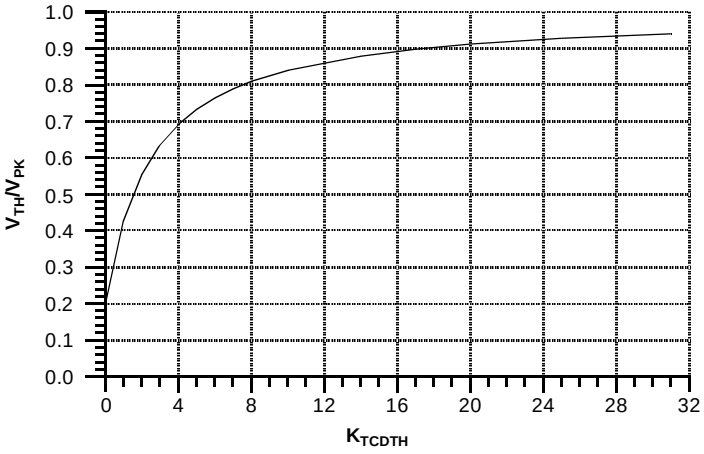
Figure 155 Track Cross Timing Diagram

A timing diagram of the process is shown in Figure 155. The envelope of the input data amplitude will rise and fall, peaking at the track center and going to some minimum value halfway between tracks. Between tracks the data consists of interference between the 2 tracks and thus cannot be read intelligibly. The track cross detector generates an internal signal TCD which goes high when the input level drops to an unacceptably low level. The TCD signal is used to gate the internal READ signal such that when TCD is high, the part switches back into idle mode where the AGC loop is in the continuous time mode, and the PLL is locked to an external reference. When TCD drops low again, a new READ cycle is initiated where the AGC switches into sampled mode and the PLL locks to the input data.

Due to the exponential relationship between gain and input level in the AGC loop, the C_{AGC} voltage, shown in Figure 155, will vary inversely with the data amplitude with a non-linear shape. When the input data peaks, V_{CAGC} will be at a minimum, and when the input data is at a minimum, V_{CAGC} will be at a peak. By subtracting V_{CAGC} from an internal 4V voltage reference, a signal proportional to the input data envelope can be generated, as shown in Figure 155. This signal is peak detected with a fast attack and variable slow decay and drives A DAC-controlled resistor divider that sets the threshold of a comparator which compares the subtracted C_{AGC} to the threshold. The comparator output is TCD. The threshold V_{TH} is user adjustable using a non-linear multiplying DAC such that the level at which TCD switches relative to the input signal can vary between roughly 20% and 60% of the input peak voltage. This corresponds to 20% to 0.94% of the peak signal V_{PK} as shown by

$$V_{TH} = \frac{V_{PK}}{1 + \frac{4}{1 + 2 \cdot K_{TCDTH}}} \qquad \textit{(eq. 152)}$$

where K_{TCDTH} is the value of TCDTH(4:0) bits in the serial control register. A plot of V_{TH} / V_{PK} vs. K_{TCDTH} is shown in Graph 1 on page 75



Graph 1 Track Cross Detect Comparator Threshold vs. DAC Setting

Two external capacitors (C_{TCD0} and C_{TCD1}) connected to CTCD0 and CTCD1 (pins 11 and 12), are used to hold the charge of the peak detector. Since there can be considerable gain and level differences from head to head, two capacitors are used, one per head. The HDSEL signal will switch the proper capacitor into the circuit using an internal analog MUX, as shown in Figure 154. The attack current is fixed with an emitter follower in series with a 250Ω resistor. This limits the attack time and helps reject spikes in the C_{AGC} voltage that result from a head switch and the squelching of the AGC input. The decay time is user programmable and is given by

$$I_{TCD} = \frac{0.065}{R_{AF}} \cdot (K_{ITCD0} + 4 \cdot K_{ITCD1} + 16 \cdot K_{ITCD2}) \qquad \textit{(eq. 153)}$$

where K_{ITCD} is controlled by the ITCD bits (1:<D9-D11>) in the serial control register, and R_{AF} is the value of the same external resistor that sets the AGC charge pump currents and the filter cutoff frequency.

It is desirable for the peak signal to decay about 5% over the length of a track crossing cycle. This allows noise spikes, which may generate an incorrect peak voltage to decay, but still maintains a relatively flat peak voltage. The trick mode speeds can vary from ±4X to ±100X, causing a 25:1 ratio in the track cross period, and thus the decay current will need to vary as well. The non-linearity in the decay time equation is due to the discrete values of trick play speeds and the fact that with the data written on an angle with respect to the tape (see Figure 155), there is a difference in the track cross period between forward and reverse speeds. The system was designed for a C_{TCD} of 0.68µF and an R_{AF} value of 10kΩ, resulting in I_{ITCD} ranging from 6.5-136.5µA. Table 198 shows the various trick modes and their burst periods, the decay current DAC setting and resultant decay current, and the V_{PK} voltage droop for the values of C_{TCD} and R_{AF} given above. Note that decay current scales with R_{AF} but charge current does not, and thus designs with large values of decay current may not exhibit proper peak detect behavior.

Table 198Track Cross Decay Current and Droop

Mode	Track Cross Burst Period	ITCD(2:0)	I_{TCD} (R_{AF}=10kΩ)	Droop Voltage (C_{TCD}=0.68µF)
+4X	11.4ms	001	6.5µA	109mV
-4X	6.7ms	001	6.5µA	64mV
+12X	3.0ms	010	26µA	115mV
-12X	2.55ms	010	26µA	98mV
+24X	1.36ms	011	32.5µA	65mV
-24X	1.3ms	011	32.5µA	62mV
±50X	0.7ms	100	104µA	107mV

Table 198Track Cross Decay Current and Droop

Mode	Track Cross Burst Period	ITCD(2:0)	I_{TCD} (R_{AF}=10kΩ)	Droop Voltage (C_{TCD}=0.68µF)
±100X	0.35ms	111	136.5µA	70mV

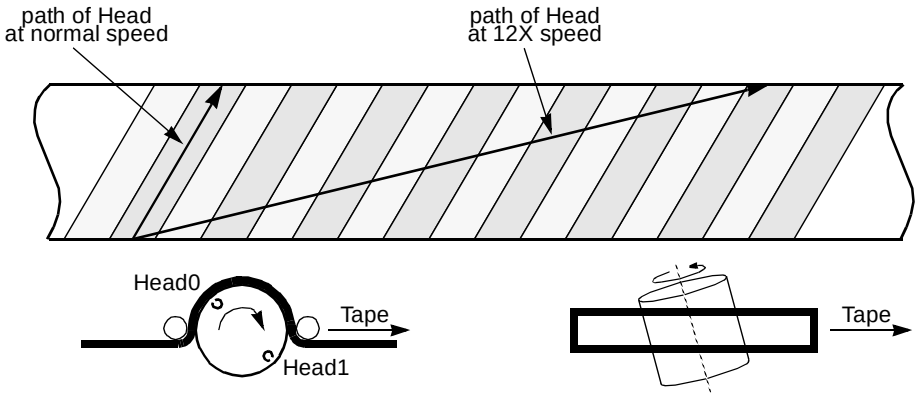


Figure 156 Tape Track Format

In trick mode there can be up to an 8% shift in data rate due to the geometry of the head crossing the track at an angle. This is shown in Figure 156. While TCD is high, the part is locked to the external FREF signal, which does not have the frequency shift in it. There would thus be two different frequencies the VCO would try to lock to depending on the level of TCD, and consequently there would be two different C_{TR} voltages. Transient time would be degraded since there would need to be a frequency lock as well as a phase lock, with the lock time limited by the bandwidth of the PLL (see Timing Recovery Loop on page 87\. The user can improve trick mode performance by using the frequency DAC.

The VCO center frequency can be adjusted up to ±12.5% through the use of two 5-bit DAC's in the serial control register. During normal play (TCD='0') the normal DAC is active and controlled by FRQN(4:0), and during trick mode the trick DAC is active and controlled by FRQT(4:0). The VCO and timing recovery frequencies are modulated by either DAC according to

$$f_{TR} = f_{TR0}\left(1 + \frac{0.125}{32} \cdot K_{FRQ}\right) \qquad \textit{(eq. 154)}$$

where K_{FRQ} is the 2's complement value of either the FRQN(4:0) or FRQT(4:0) control register words and range from -16 to +15, f_{TR0} is the 0-DAC timing recovery clock center frequency, and f_{TR} is the timing recovery frequency modulated by the FRQ DAC.

By setting the appropriate DAC values, the trick mode data rate offset can be accounted for, and the C_{TR} voltage can be maintained between normal play and trick play. Typically the normal DAC will be set to 00000 and the trick DAC will have the frequency offset. By using both DAC's, however, part-to-part variation can be accounted for resulting in better centering of the C_{TR} voltage around 0V where charge pump current offsets (which affect static phase errors) are minimized and VCO dynamic range is maximized, which may lead to performance improvement.

The track cross detector is enabled with the TCDEN bit (7:<D8>) in the serial control register. If TCDEN = 0, TCD will never switch and no new read cycle will be initiated regardless of input level. The normal frequency DAC (13:<D7-D11>) is used throughout. If TCDEN = 1, TCD will determine which DAC input to use. When the signal input is large (4v-V_{CAGC} is above V_{TH}) and TCDEN=1, TCD is low and the FRQT DAC input (14:<D7-D11>) is used. When the input signal is 4v-V_{CAGC} is below V_{TH}) and TCDEN=1, TCD is high the FRQN DAC input (13:<D7-D11>) is used. If no frequency shift is desired in trick mode, then the user will need to program the 2 DAC settings to the same value.

Continuous Time Low-pass Filter/Equalizer

The filter is implemented as a 7-pole, 0.05 degree linear phase, equiripple low pass continuous time filter (CTF). The cutoff frequency, boost, and DC group delay are each individually programmable.The basic building block for the filter is the integrator (g_m-C) stage which consists of a transconductance amplifier driving an on-chip capacitor. Four g_m-C stages and two capacitors interconnected as shown in Figure 157 form a biquad, which has a second order transfer function as shown in equation (eq. 155) below.

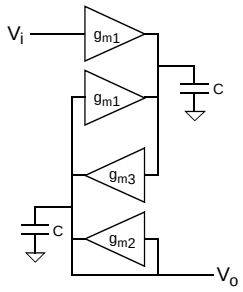


Figure 157 Biquad Block Diagram

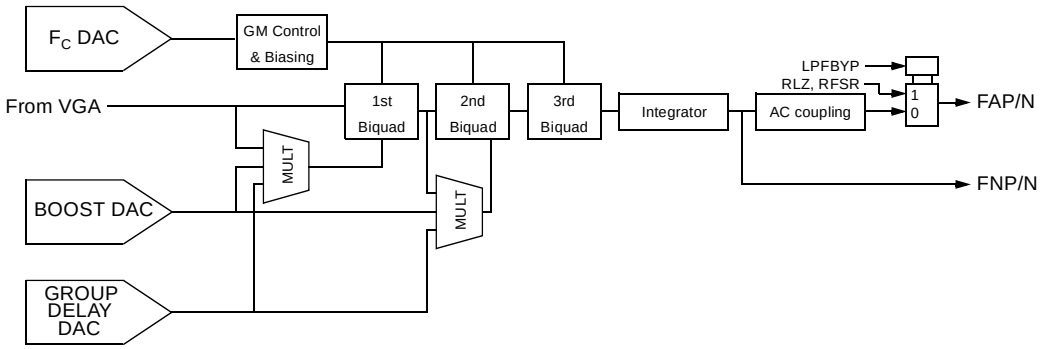


Figure 158 Filter Block Diagram

$$\frac{V_o}{V_i} = \frac{\omega_o^2}{s^2 + s(\omega_o / Q_o) + \omega_o^2} \qquad \textit{(eq. 155)}$$

where,

$$\omega_o = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{C} \quad \textit{and} \quad Q_o = \frac{\sqrt{g_{m1} \cdot g_{m3}}}{g_{m2}}$$

Three of these biquads and a single integrating g_m-C stage are cascaded to form a seven-pole low pass filter as shown in Figure 158. Boost, or pulse slimming, is implemented by feeding the filter input through two variable gain (or multiplying) stages to the normally grounded terminals of the capacitors of the g_m-C stage in the first and second biquads. Mathematically boost adds zeros to the overall filter transfer function which is shown in equation (eq. 156) below.

$$\frac{V_o}{V_i} = A_N \cdot \left(\frac{\omega_{01}^2 - \beta s - \alpha s^2}{s^2 + s(\omega_{o1} / Q_{01}) + \omega_{01}^2} \right) \cdot \left(\frac{\omega_{02}^2}{s^2 + s(\omega_{02} / Q_{02}) + \omega_{02}^2} \right) \cdot \left(\frac{\omega_{03}^2}{s^2 + s(\omega_{03} / Q_{03}) + \omega_{03}^2} \right) \cdot \left(\frac{\omega_{04}}{s + \omega_{04}} \right) \qquad \textit{(eq. 156)}$$

where, A_N = -3.2dB, $\omega_0 = 2\pi f_C$,
f_C = programmable filter cutoff frequency (FCH1, FCH0)
α = programmable symmetric zero coefficient (BSTH1, BSTH0)
β = programmable asymmetric zero coefficient (GDH1, GDH0)
$\omega_{01} = 1.148 \cdot \omega_0$, $Q_{01} = 0.681$
$\omega_{02} = 1.718 \cdot \omega_0$, $Q_{02} = 1.114$
$\omega_{03} = 2.317 \cdot \omega_0$, $Q_{03} = 2.022$
$\omega_{04} = 0.861 \cdot \omega_0$

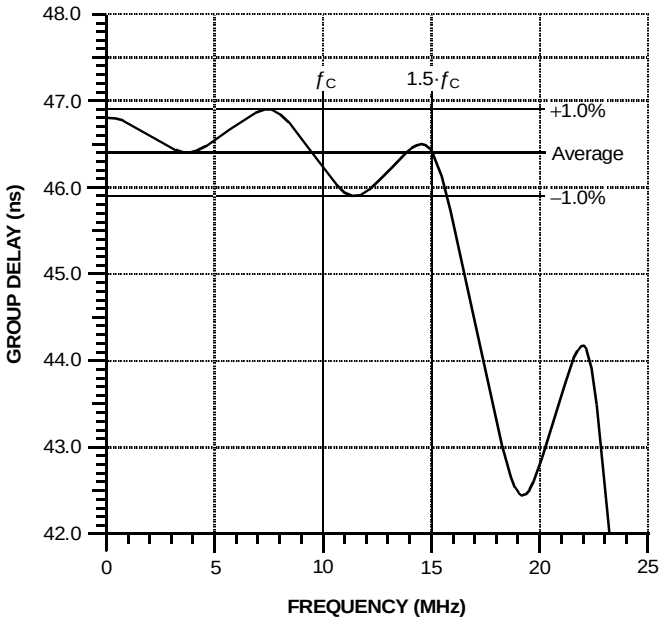
Note that the filter has an attenuation factor of -3.2dB. The filter output is coupled to the FIR filter and full-wave rectifier through on-chip coupling capacitors to reduce the effect of offsets in the filter as shown in Figure 148. The low frequency pole associated with the coupling capacitors is set nominally to 20kHz.

Cutoff frequency is controlled by one of two continuous time filter f_C DAC's and a current set by the external R_{AF} resistor. The control word for the DAC is read from either the FCH0 or FCH1 register depending on the value of HDSEL. Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation

$$f_C = (0.15 \cdot K_{FC} + 5.0) \cdot \frac{6}{R_{AF}} \qquad \textit{(eq. 157)}$$

where K_{FC} is the value of either the FCH0(5:0) or FCH1(5:0) control words and ranges between 0 and 63, and R_{AF} is in kΩ. R_{AF} is the same external resistor that sets the Gain Control charging currents.

Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM65015 group delay flatness is specified to be less then 4% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 46ns at a cutoff of 10MHz. Thus at this cutoff frequency, the group delay varies by less than 2ns out to 20MHz. A typical group delay is shown in Graph 2.



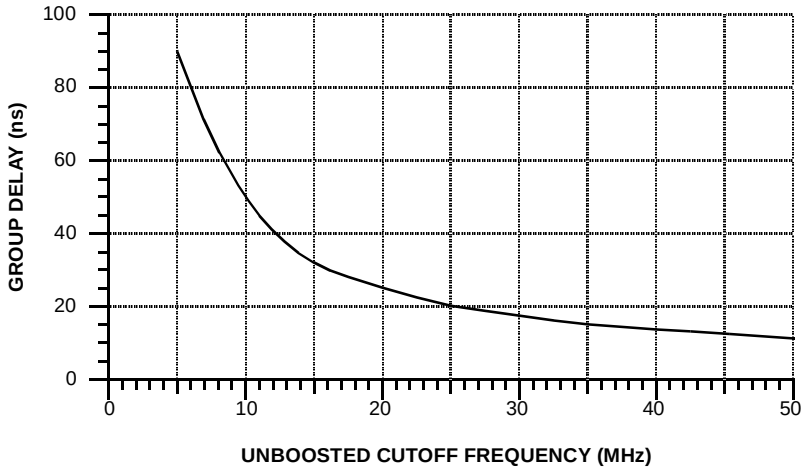
Graph 2 Typical Group Delay of AGC and Filter (with f_C = 10MHz)

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay T_{GD}, in nanoseconds, is expressed as

$$T_{GD} = \left[3 + \frac{434}{f_C}\right] \text{ns} \qquad \textit{(eq. 158)}$$

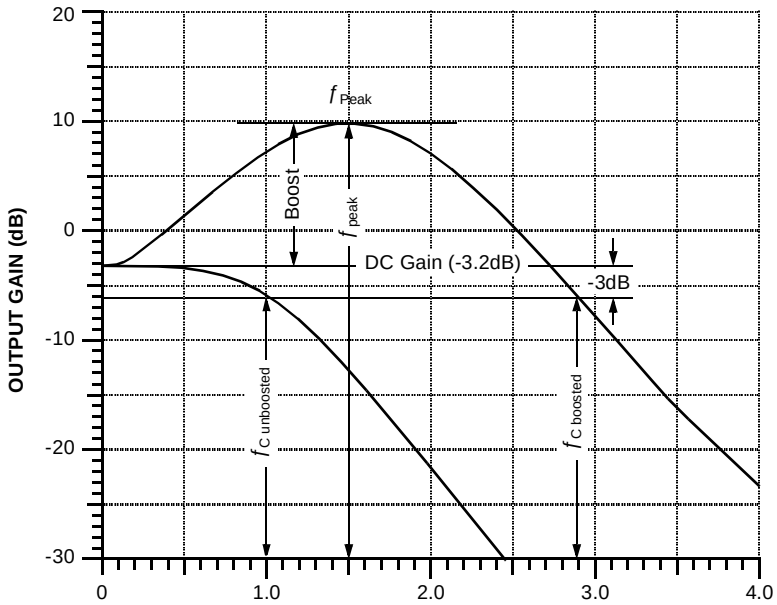
where f_C is the filter cutoff frequency in MHz. A graph of equation (eq. 158) is shown in Graph 3.

MIXED SIGNAL CIRCUITS

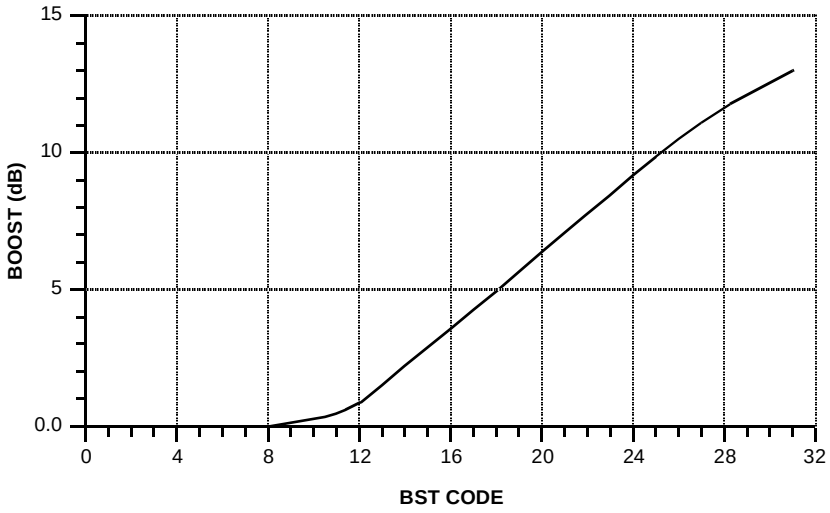


Graph 3 Typical Group Delay vs. Cutoff Frequency

Setting the desired boost through the boost control register bits (with the group delay register set to zero) produces symmetric zeros on the real axis (α in equation (eq. 156)). This maintains the constant group delay as in the no-boost case. The amount of boost equalization depends on the value output of either the BSTH0 (11:<D0-D4>) or BSTH1(12:<D0-D4>) control register words, depending upon the value of HDSEL. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function. Graph 4 shows two normalized filter response curves, one with no boost and the other with maximum boost. Shown are the unboosted and boosted cutoff frequencies and the frequency where the filter response peaks, defined as the gain peak frequency, f_{peak}. Graph 5 shows the nominal relationship between the BST control word and the resulting boost level relative to the DC level. Notice the absence of peaking when BST is below 8. In this region the bandwidth is pushed out but the gain doesn't peak above the DC level.

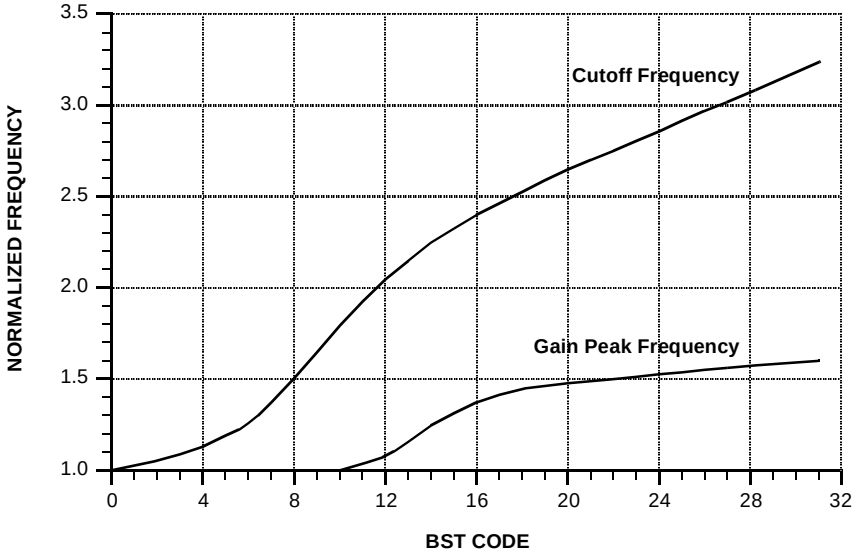


Graph 4 Normalized Filter Frequency Gain, Boosted & Unboosted

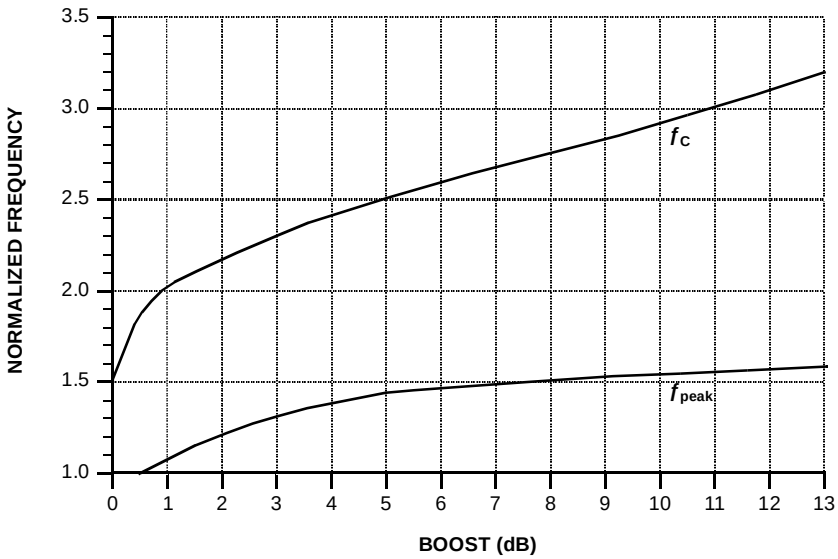


Graph 5 Filter Boost Control

Graph 6 shows the effect of boost on the cutoff frequency. With maximum boost the cutoff frequency is over triple the unboosted value. Also shown is the gain peak frequency, f_{peak}, which for maximum boost achieves a value of over 1.5 that of the unboosted response. Graph 7 displays the same data as Graph 6 plotted against the resultant boost value rather then the DAC code.



Graph 6 Normalized Cutoff and Gain Peak Frequencies vs. Code



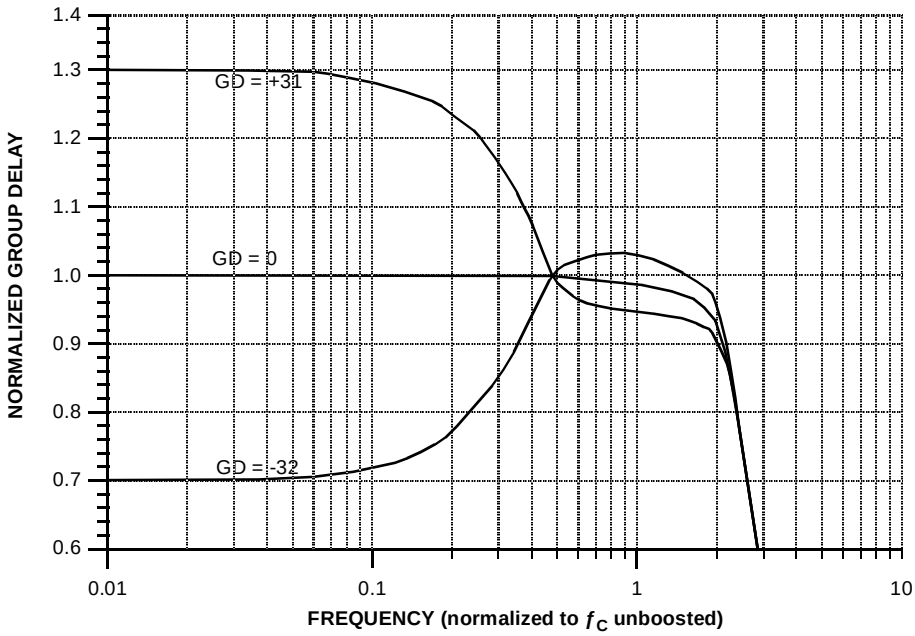
Graph 7 Normalized Cutoff and Gain Peak Frequencies vs. Code

Group delay can be varied by ±30% from the symmetric zero condition via control DACs in the serial control register. There are two sets of group delay DAC register bits, GDH0(2:<D6-D12>) and GDH1(3:<D6-D11>), corresponding to each head chosen via HDSEL (pin 51). The group delay registers can be used to produce asymmetry in the zeros causing the group delay to vary with frequency (β in equation (eq. 156)). This can be desirable to compensate for asymmetry in the heads/media components. The group delay registers are six bits wide and are represented in two's complement format. A code of +31 corresponds to a DC shift in group delay of +30%; a code of -32 corresponds to -30% shift in DC group delay. The percent shift in DC group delay can be expressed as

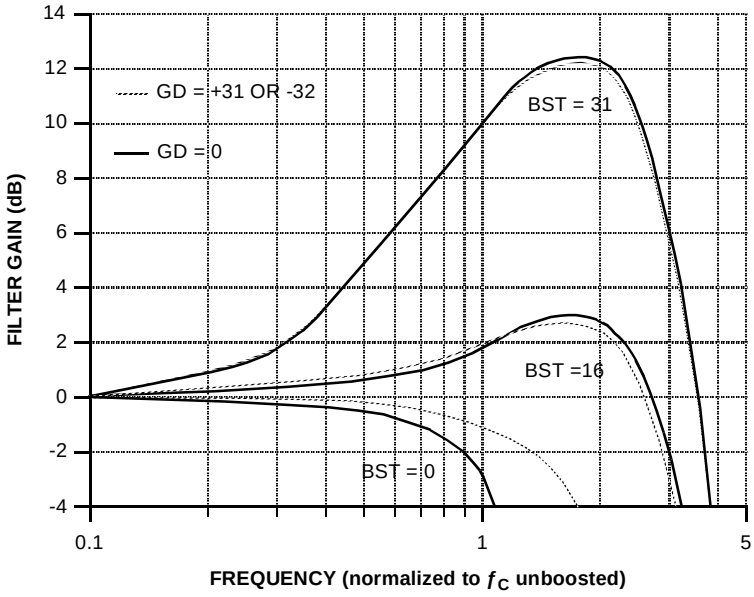
$$\frac{\Delta T_{GD}}{T_{GD_0}} \times 100 \;=\; 0.95 \cdot K_{GD} \qquad \textit{(eq. 159)}$$

where K_{GD} is the value of the 6-bit GDH0 or GDH1control word.

The boost is held nearly constant as group delay is varied. This is accomplished by moving one zero in and the other zero out at the same frequency. At zero boost, the zeros are at ±∞. Therefore it is impossible to move one out as one is moved in. In this extreme case, it can be seen that the identical unboosted transfer characteristic cannot be maintained as group delay is varied. Graph 8 shows the effect on group delay of programming the group delay register to zero and to the two extremes, and Graph 9 shows the effect on the magnitude response as the group delay register value varies over extremes and under several boost conditions.



Graph 8 Normalized Group Delay (max f_C, max boost)



Graph 9 Gain Variations with Different Boost and Group Delay Settings

A test feature exists in the filter where a differential signal may be applied to the RLZ and RFSR inputs (pins 64 and 63) which can be input in place of the AC coupled filter output. Control register bit LPFBYP (Low Pass Filter BYPass) when set to a '1' controls this output test MUX, as shown in Figure 158. The voltage level on both RLZ and RFSR should be kept above 2V to ensure that the normal RLZ and RFSR bias circuitry remains off.

FIR Filter/Equalizer

The FIR is a five tap transversal filter with independently controllable tap weights. Independent control provides both gain and phase adjustment of the input signal. The tap weights must be directly programmed into the serial registers' weight vector locations designated FIR0 through FIR4, which set tap weights K_0-K_4 respectively. Taps 1 and 3 have two registers each, one for each head. HDSEL (pin 51) selects the appropriate register. HDSEL='0' will select registers FIR1H0 (2:<D0-D5>) and FIR3H0 (4:<D0-D5>) for FIR1 and FIR3, and HDSEL='1' will select registers FIR1H1 (3:<D0-D5>) and FIR3H1(5:<D0-D5>) for FIR1 and FIR3. Taps 0, 2, and 4 (0:<D1-D5>, 6:<D0-D4>, and 1:<D1-D5> respectively) are shared by both heads.

As with any sampled system the response is periodic in the frequency domain. The center tap provides a flat response over frequency. The inner set of taps adjacent to the center tap produce a periodic response that is sinusoidal in shape and repeats at multiples of the sampling frequency. The sampling frequency in this situation is the channel data rate. The outer set of taps, two delays away from the center tap, are periodic at half the sample frequency. The general frequency response for a given set of taps is given by

$$H_n(e^{j\omega T}) = (K_{-n} + K_n)\cos(n\omega T) + j(K_{-n} - K_n)\sin(n\omega T) \qquad \textit{(eq. 160)}$$

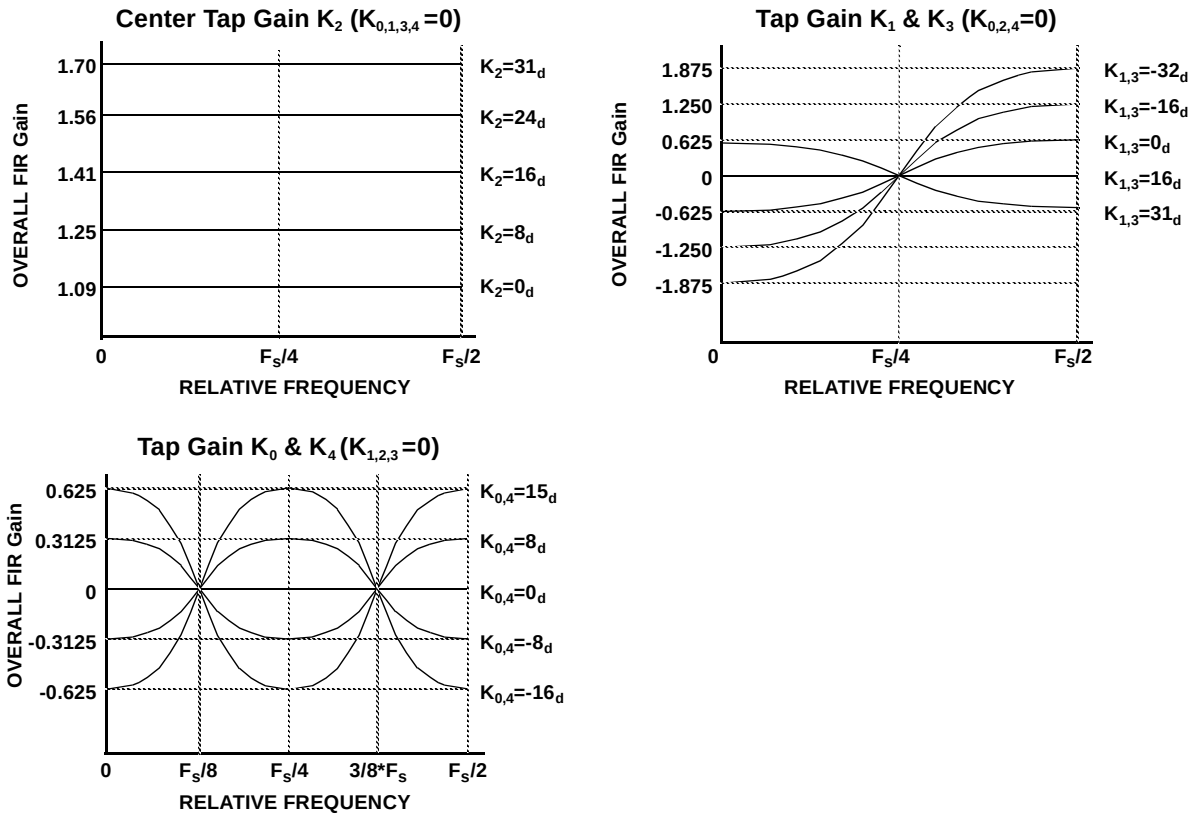
Where n is the count away from the center tap, K_n is the gain of preceding taps, K_{-n} is the gain of past taps.

The T term is the channel sample interval. This is the ideal response for a single set of taps. The net response for all the taps is the sum of each pair and the center tap. As shown below:

$$He^{j\omega T} = H_0 e^{j\omega T} + H_1 e^{j\omega T} + H_2 e^{j\omega T} \qquad \textit{(eq. 161)}$$

The Graph 10 illustrates the possible gain variations achievable when symmetric taps are swept together over their allowable ranges, as listed in Table 199.

The H_0 term provides only a flat frequency response with varying values of gain. The gain response also includes finite bandwidth characteristics of the sampler. The sampler bandwidth is about 120 MHz and will have some effect on the frequency characteristics. The ideal gain limits for the taps are shown below.



Graph 10 FIR Symmetric Tap Frequency Response Curves

Table 199 FIR Tap Gain Settings

Tap	K_0	K_1	K_2	K_3	K_4
Gain Range	-0.312 0.293	-0.9375 +0.293	+1.09 +1.70	-0.9375 +0.293	-0.312 +0.293
Actual bits	5	6	5	6	5
Eff. bits	7	7	7	7	7
Resolution	(1/64)·1.25=19.56mV/V				

FIR Adaptation Circuit

An adaptive system of any kind consists of a plant that performs some function (process, filter, etc.), a means of determining the performance of the plant, and an algorithm used to adjust the plant's controls. The FIR Adaptation block uses a decision-directed error metric to quantify the system performance and a sequential binary Least Mean Squared (LMS) adaptation algorithm to adjust the tap weights. In this system the plant is the FIR and the plant controls are the outer tap weights. The center tap weight is not adjusted because it primarily controls the DC gain of the equalizer and that function is taken care of by the AGC block.

Determining the performance of the equalizer can be done by subtracting the output of the FIR from the ideal PR4 data. This can be done if a known data pattern has been written to the disk or the ideal data has been externally supplied to the part. This adaptation circuit uses a decision-directed technique that estimates the ideal data stream from the actual data. A target response is generated from the data by quantizing the output of the FIR into three levels. Three levels are appropriate for a partial response system equalized for the PR4 response shape. In a PR4 system any single transition on the disk produces interference with one adjacent transition in a way that will produce three distinct voltage levels. After the FIR output has been quantized, the appropriate ideal voltage value (+1, 0, -1) can then be subtracted from the output, which generates an estimate of the error signal. Decision- directed systems work well as long as the initial errors are not too large. One case that will cause divergence in the tap weights is when the amplitude is half or below half of what it should be. In this case all the weights converge toward zero. For more realistic cases convergence is not a problem. The system has been shown to converge for a signal containing Lorentzian step response shapes with densities as high as 4bits/pw50 with the initial outer taps set to zero.

The LMS adaptation algorithm is a very robust technique for minimizing the magnitude of the errors produced by a system with respect to a target response. In such a system all the weights are adjusted for each output bit of the channel. The algorithm iteratively adjusts each tap weight in the direction that would reduce the FIR output error based on the value held in its associated tap. This is done by multiplying the FIR output error by the value held in a given tap. For example, when the output is larger than the ideal positive output and the sample held at a given tap is positive, its gain would be decreased, and this would have the effect of reducing the error in that instance.

The basic tap weight update recursion is defined by:

$$\vec{W}_K = \vec{W}_{K-1} + 2 \cdot \mu \cdot \varepsilon_{K-1} \cdot \vec{C}_{K-1} \qquad \textit{(eq. 162)}$$

W_{K-1} and C_{K-1} are 5-element vectors
W_{K-1} contains the tap weights of the FIR
C_{K-1} contains the sample values held at each tap of the FIR.
μ is a gain term which sets the overall loop gain of the adaptive feedback system
ε_{K-1} is the error in the output of the FIR at the current time "K-1" which is computed by

$$\varepsilon_{K-1} = d_{K-1} - Y_{K-1} \qquad \textit{(eq. 163)}$$

The d_{K-1} term is the ideal data at the time "K-1"
Y_{K-1} is the FIR output at that time.
When decision-directed adaptation is employed, d_{K-1} is replaced by an estimate of the ideal data (+1, 0, -1).

The procedure that is employed by this circuit is a modification of the basic LMS concept. It maintains many of the key features and yet greatly reduces implementation complexity in order to minimize power consumption and die area. The basic approach is to incrementally adapt one weight at a time, based on an average of several LMS update samples, and then repeat this process for each successive weight in a cyclic fashion for a complete read cycle. In this system there is a digitally controlled FIR and the tap weights can only be adjusted in discrete steps, one bit at a time. This sets μ for the part at the value of one LSB which equals 0.0195. The multiplication of the tap values with the output errors is replaced by a binary multiplication. The sign of that operation indicates whether to increment or decrement the tap weight. Averaging the individual updates is used to prevent instabilities and a dead zone is used to reduce the amount of tap weight wander once the steady state values have been reached. An option is available to force symmetrical tap weight adaptation to prevent timing recovery/FIR interactions.

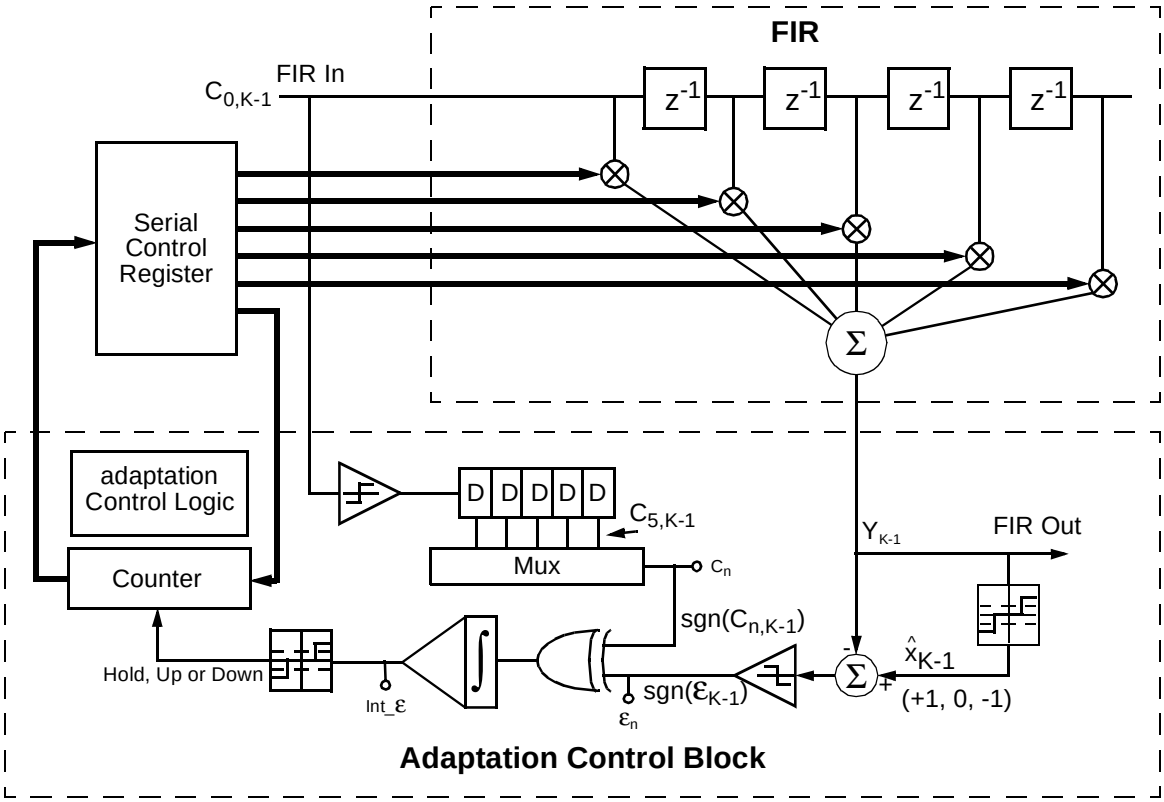


Figure 159 Sequential Binary Least Mean Squared Adaptation

The final adaptation equation becomes

$$\vec{W}_K = \vec{W}_{K-1} + \left(Q_{(1,0,-1)} \left(\frac{\sum_{J=1}^{N} sgn(\varepsilon_{K-1+J}) \cdot sgn(\vec{C}_{K-1+J})}{N} \right) \times lsb \right) \quad \textit{(eq. 164)}$$

The adaptation process starts after a read operation has been initiated and the internal READ signal has gone high (see Figure 151 on page 70 and Figure 153 on page 71). At this time the initial tap weight address is loaded into an address counter. When the internal PLL signal goes high, indicating that the timing recovery loop has transitioned from acquisition to tracking mode, the first tap weight value is loaded into an up/down counter and the averaging process begins. Once the integration time has been reached, the tap update command is latched. The current tap weight is processed and then written back to the serial register. The tap weight address counter is incremented and the next tap weight is loaded. This process continues until a READ cycle ends either through the deassertion of RG, the detection of a dropout, or a transition on HDSEL.

Note: Since the part is accessing the serial registers during adaptation, the user should *not* attempt any serial register operation while RG is asserted and the AE bit set.

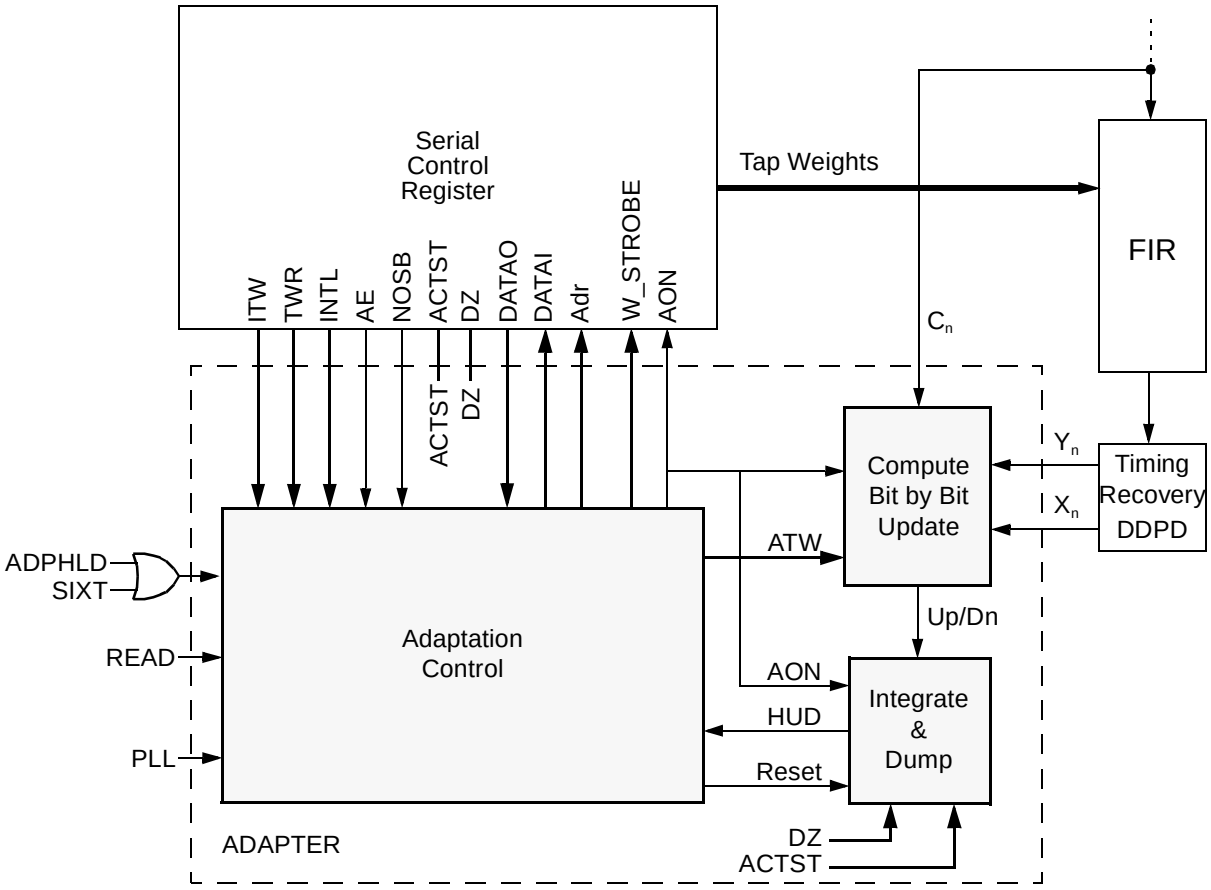


Figure 160 Self Adaptation Circuitry

Key Features of the adaptive FIR filter are outlined below:

31) Adaptation Control test: ACTST (24:<D2-D3>) - Two bit control for the output of the integrator that forces either an up, hold, or down count. This is primarily a test feature for the adaptation control logic. '00' specifies normal operation, '01' specifies an UP count, '10' a DOWN count, & '11' specifies hold. ADPHLD (pin 48) set to a '1' forces ACTST into state '11', this allows the user to hold the adaptation and freeze the tap weights at their current values without having to write through the serial register.

32) Adaptation enable: AE (24:<D11>) - When set to a '1' the AE control register bit enables the adaptation circuitry. It can not be modified during an adaptation read cycle.

33) Dead zone: DZ (24:<D9-D103>) - Two bit control that specifies the adaptation threshold. With ideal tap weight settings, the adaptation algorithm will randomly integrate the error signal up and down. Without a dead zone, the tap weights would be changing continuously. The dead zone DAC allows a programmable window inside of which no weights are adapted. Only if there is a net integration in one direction exceeding a programmable threshold, will the tap weight update. The threshold is set in a symmetrical manner as a percentage of the integration length. A DZ value of '00' sets the threshold equal to 35% of the integration length. For example with an integration length of 12 and a DZ value of '00', the tap weight will not adapt unless there is a net up or down integration for at least 4.2 clock cycles. A value of '01' sets a 50% threshold (6 clock cycles with INTL set to 12), '10' sets a 65% threshold (7.8 clock cycles), and '11' sets an 80% threshold (9.6 clock cycles). If there aren't enough up or down commands to exceed the threshold within the integration length time, the system simply holds the current value for that tap during this cycle.

34) Integration length: INTL (24:<D7-D8>) - Two bit control that selects between 12 (INTL='00'),15('01'),18('10'), or 21('11') as the number of samples to average for each update cycle.

35) Initial tap weight: ITW (24:<D4-D5>) - Two bit word which selects the specific tap to be adapted first. The adaptation would normally proceed in the following order for an ITW value of '000': K_0, K_4, K_1, K_3, K_0, K_4, K_1, K_3, etc. As ITW is incremented by one bit the first tap adapted rotates to the next in the sequence. The relative order of the tap weights remains the same. Thus ITW='01' starts with K_4, ITW='10' starts with K_1 and ITW='11' starts with K_3. This option allows a sector to be re-read and each tap weight adapted on a different set of data (see Table 200 for the complete ITW bit mapping).

36) Tap weight range: TWR (24:<D0-D1>) - Two bit control of tap weight range. If all four taps are to be adjusted this value should be set to '00'. By setting this value to '01' through '11', a reduced range of taps will be adjusted. The taps that aren't adjusted are still active but are held at their preprogrammed values. With TWR set to '00' the tap weight pointer counts from '0' to '3' then rolls back to '0', where '0' selects K_0, '1' selects K_4, '2' selects K_1, and '3' selects K_3. Incrementing TRW by one bit reduces number of taps adjusted by starting the count at a value other than '0' and counting to '3' before rolling back to the starting count value. Thus for TRW set to '01' the count starts at '1' and only taps K_4, K_1, and K_3 are adapted. For TRW='10' only taps K_1 and K_3 are adapted. With TWR set to '11', only tap K_3 is adapted.
Tap weights can be written and read by the controller. Thus the initial tap weight values can be preset near their optimal values and the final values can be read back after each adaptation read cycle. The final taps weights remain as the initial tap weights for subsequent read cycles.

Note: Proper selection of DZ and INTL can allow for rapid adaptation or for slow, stable system tracking.

37) Symmetry control: SYMC (7:<D7-D8>) - This is a two bit control that selects a specific set of taps to be controlled in a symmetrical manner. If SYMC = 00 the inner two taps (K1 & K3) are symmetrically adjusted whereas the rest are independently adapted. The adaptation is done in a ping-pong fashion where the two weights are changed simultaneously in two alternating cycles based on the value held first in one tap and then in the other. This type of adaptation is not as robust as a true LMS routine and will require some care in selecting the training pattern. For SYMC = '01' the two outer taps (K0 & K4) are adjusted symmetrically, for SYMC='10' both the inner and outer taps are adjusted symmetrically, and for SYMC='11' none of the taps are symmetrically adjusted.

Timing Recovery Loop

The timing recovery block uses a fully integrated, fast acquisition phase-locked loop (PLL) to implement clock recovery on the incoming data stream. A block diagram of the timing recovery system is shown in Figure 161. A voltage-controlled oscillator (VCO) generates a frequency which is divided by two and has its phase compared in a phase-frequency detector (PFD) with that of an input reference clock F_{REF}, or with the signal data from the FIR, generating an error term. The error term is converted into a current in the charge pump which is integrated by an off-chip capacitor C_{TR} connected differentially to the CTRP and CTRN (pins 31 and 32). The Imult block converts this capacitor voltage into an integral scaling factor which modulates the I_{REF} current and is summed with the current output from the Pmult block which scales its current proportionally with the error at the phase detector output. The summed current controls the VCO frequency, thus forming a control loop.

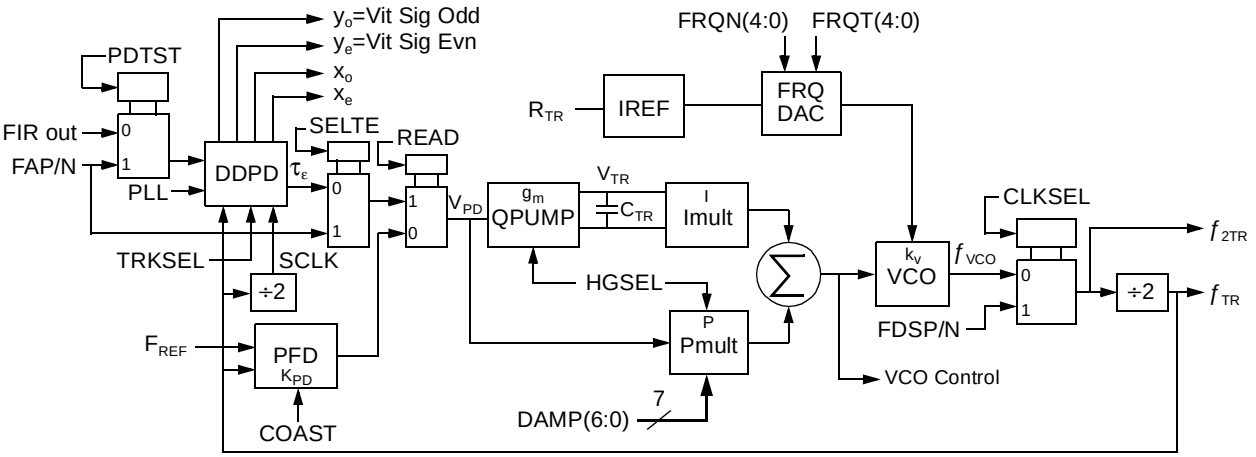


Figure 161 Timing Recovery Block Diagram

Figure 150 on page 70 shows the timing for a read cycle. A low level on the internal READ signal defines idle mode which occurs during when 'RG' is low, when the track cross detector output TCD is low, or when in Write Mode (WG pin high). In idle mode the loop either locks to the external F_{ref} signal through the phase/frequency detector (PFD); or coasts, where the phase/frequency detector is disabled and the VCO runs open-loop. Coast mode is selected by setting the control register bit COAST = 1 (10:<D1>). A read operation is initiated with a positive transition on RG (pin 49), a negative transition on TCD, or a [polarity change on HDSEL (pin 51). This defines acquisition mode where samples from the FIR filter are read by the decision-directed phase detector (DDPD) and an acquisition timing gradient algorithm is used to coarse align the data to ideal samples, as illustrated in Figure 150. Because the loop must acquire lock to random data, this acquisition timing gradient algorithm has limitations, so after a fixed time set by the PLL sync count the loop switches into tracking mode where a more precise locking algorithm is applied. The part stays in tracking mode until another dropout is detected where it switches back to idle mode.

Read mode is initiated by a positive transition on the RG line as shown in Figure 162. The VCO is held in a low output state when the 6T input signal crosses the threshold set by the Zero Phase Restart DAC (9:<D9-D12>). The second time the threshold is crossed

the VCO restarts. The threshold is set to align the VCO to the ideal zero sample of the 6T input. The analog and digital delays in the samplers and the VCO require a slight variation of the sample threshold so a multiplying DAC is used to obtain the optimal set point. Once the VCO restarts, the DDPD output is used as the phase error to drive the PLL. The initial gain will be high to minimize the acquisition time and the computation of the phase error is done with a robust technique which prevents false lock-up modes. Since the AGC gain control is independent of the timing control, it can be switched at any point after the FIR has taken 5 sample (5-tap filter) and is switched slightly before the timing transition from Acquisition to Tracking.

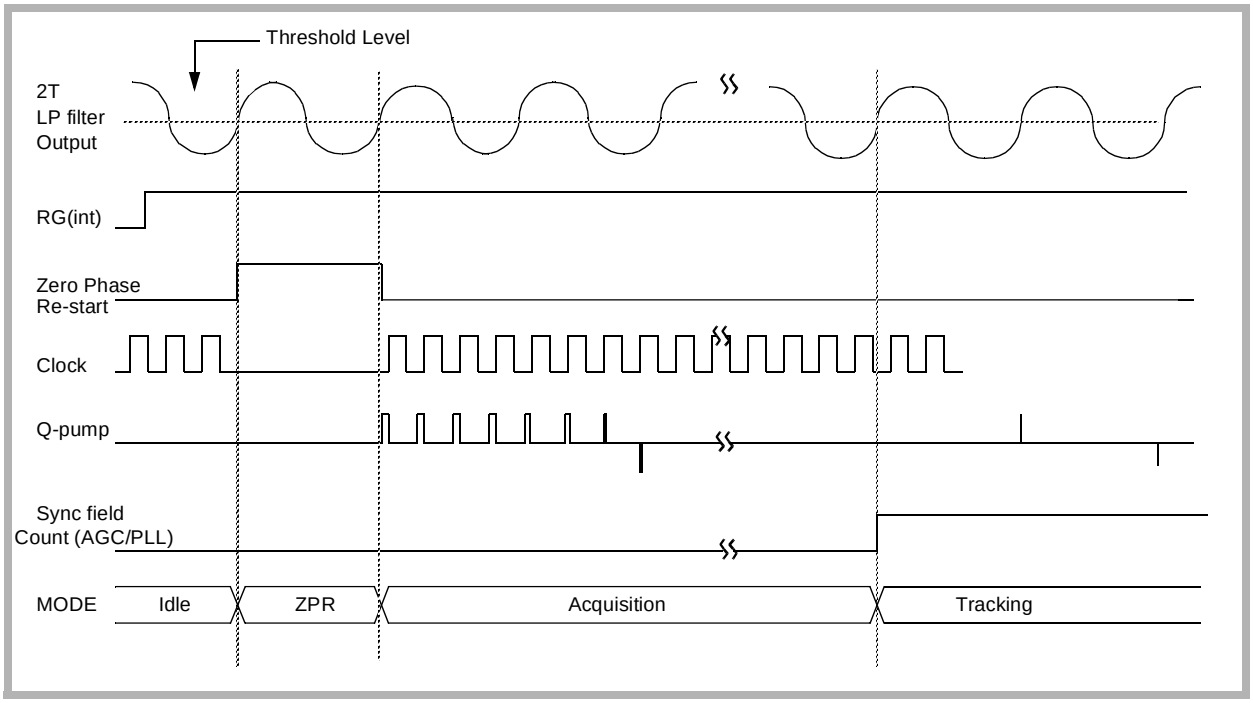


Figure 162 Timing Recovery Operation

The goal in acquisition mode is to adjust the phase of the VCO clock to the point where the tracking timing gradient algorithm can track the data. Ideal PR4 data has three valid sample values, denoted +1, 0, and -1. The AGC loop and the two filters (CTF and FIR) should be set to equalize the data properly to produce these ideal sample values. It is the job of the timing recovery loop to adjust the phase and frequency of the sampling clock to converge on these three levels. The acquisition algorithm slices each sample into one of three levels, based strictly on threshold voltages separating a '-1' from a '0' from a '+1'. These samples can be compared with the ideal samples and the phase adjusted accordingly.The decision-directed phase detector (DDPD) operates on sampled data in either an analog or quantized form to compute a timing gradient. Since initially the phase is random, it isn't true that the closest ideal voltage level is necessarily the correct one. It is true, however, that any large transition in the data must have at least one '+1' sample for a positive transition, and at least one '-1' sample for a negative transition. To determine which direction to adjust the phase, the slope of the input waveform must be known, which can't always be determined with sampled information only. Inspection of equalized PR4 data, however, reveals the fact that two consecutive '+1' samples or two consecutive '-1' samples must have a peak between them and consequently a change in slope, and that a '+1' followed by a '-1' must have a negative slope, and a '-1' followed by a '+1' must have a positive slope. Any '0' sample could have any slope and any '0' sample preceding or following a '+1' or '-1' sample could have either slope. The acquisition timing gradient thus operates only on '+1' and '-1' samples. Two consecutive samples are taken and if they are both non-zero, their magnitudes and signs are compared. The signs determine the slope of the timing gradient and the magnitude of the timing gradient is equal to the difference in the samples magnitudes. All other cases are ignored. The phase error is proportional to the timing and the phase and frequency of the clock is adjusted appropriately to minimize the error. The acquisition timing gradient can be expressed mathematically as

$$\Delta\tau_n = -(y_n \cdot \hat{x}_{n-1}) \cdot \hat{x}_n^2 + (y_{n-1} \cdot \hat{x}_n) \cdot \hat{x}_{n-1}^2 \qquad \textit{(eq. 165)}$$

where

$$\hat{x}_n = \begin{cases} 1 \leftarrow y_n \geq V_{THTR} \\ 0 \leftarrow -V_{THTR} < y_n < V_{THTR} \\ -1 \leftarrow y_n \leq -V_{THTR} \end{cases} \quad \textit{(eq. 166)}$$

The 'y' terms are the sampled analog values at the current or previous sample time
the 'x' values are the quantized estimates of the ideal 'y' values.
V_{THTR} is a threshold voltage equal to one half the ideal '1' voltage.

After a sufficient number of clock periods it is assumed that the acquisition timing gradient has adjusted the phase of the clock to be "close enough" so that the DDPD can switch to the tracking timing gradient. This number is set by the AGC and PLL Sync Field counters described in Gain Control on page 67. The tracking algorithm is similar to the acquisition timing gradient comparing adjacent '+1' or '-1' samples to one another, but also compares '0' samples to ideal '0's when the '0' samples are adjacent to a '+1' or '–1'. The tracking timing gradient is mathematically expressed as

$$\Delta\tau_n = -(y_n \cdot \hat{x}_{n-1}) + (y_{n-1} \cdot \hat{x}_n) \quad \textit{(eq. 167)}$$

where the 'x' values are given in equation (eq. 165).

This algorithm will converge to a clock phase which produces only three possible sample levels. If the tracking timing gradient were used for acquisition, there is a possibility that the loop will converge to a phase exactly 180° off. Thus two algorithms are needed. Note that both terms in equation (eq. 167) will be non-zero only if there are two successive '±1's. Any '0' data term will null out the sample adjacent to the '0'. A '+1' or '-1' adjacent to a '0' is used to determine the slope of the data and adjust the phase in the proper direction to move the sampled point closer to '0'. Note also the comparison between equation (eq. 165) and equation (eq. 167). Equation (eq. 165) has the squared terms to force the timing gradient to zero if either sample is a '0'. For data streams with few occurrences of consecutive '±1's the acquisition timing gradient will be slower to respond than the tracking timing gradient. If the recovered datarate frequency is quite close to the reference frequency and there is little noise in the system (for example under test conditions), the loop may have difficulty acquiring lock. For this reason control register bit TRKSEL was added. With TRKSEL set to a '1', the part will use the tracking algorithm in both Acquisition mode and Tracking mode, avoiding the low gain situation. For normal operation it is recommended that TRKSEL be set to a '0'. Only if the part has difficulty locking should TRKSEL be set to a '1.'

The external differential ECL input pins FDSP/N can be used in place of the VCO for test purposes by setting the CLKSEL control register bit to a '1.' Several test signals are available out of the decision directed phase detector. A hardware simplification of the timing gradient splits the path into odd and even samples rather than into consecutive samples. Hence instead of y_n, y_{n-1}, x_n and x_{n-1} available for test, y_e, y_o, x_e and x_o are instead. The only difference is that each of the odd and even samples is held for two cycles. The sign of the timing gradient will invert with each cycle to account for the fact that the odd and even samples alternate between the n and n-1 samples with each cycle. These same even and odd y samples are referred to VIT SIG O and VIT SIG E as they are also used in the odd and even interleaves in the Viterbi. Also available is the half-rate sampling clock SCLK (see Table 201 on page 94).

Clock Recovery Loop Gains

In the idle and write modes, the timing recovery loop is locked to an external reference which is running at the user data rate. The PFD outputs a pulse whose width is proportional to the phase/frequency difference of the loop's phase input θ_i, with respect to the timing recovery VCO's phase output, θ_o with the following relationship

$$\Delta V_{PD} = K_{PD} \cdot (\theta_i - \theta_o) \quad \textit{(eq. 168)}$$

where K_{PD}=0.125 V/rad.

In read mode the timing recovery loop is updated via the DDPD. The phase detector output may still be modeled similar to that of Idle/Write mode except now the phase error is derived from either equation Eq. 165 or Eq. 167 where the phase error is proportional to the magnitude of the voltage difference between the received sample and the ideal sample. To maintain the same phase detector gain K_{PD} of 0.125 V/rad as in Idle/Write mode, the timing gradient voltage must be gained up as shown below

$$\Delta V_{PD} = 1.43 \cdot \Delta\tau_n \quad \textit{(eq. 169)}$$

The gain term allows equation (eq. 168) to be valid in Tracking mode as well.

The charge pump (QPUMP) block produces a differential charging/discharging current across the external C_{TR} capacitor proportional to the phase detector output. The QPUMP gain is a function of the timing recovery loop mode. When the loop is switched from acquisition to tracking, the gain of the QPUMP is reduced by a factor of 4, and the gain of the PMULT (see discussion below) is reduced by a factor of 2. This lowers the loop gain in Tracking mode, while keeping the damping factor constant, causing the loop to be less susceptible to noise. Control register HGSEL (7:<D6>) when set to a '1' defeat this keeping the part in high gain. The charge pump current I_{QP} is given by

$$I_{QP} = g_m \cdot \Delta V_{PD} \quad \textit{(eq. 170)}$$

where ΔV_{PD} is given above and g_m equals 460µA/V in idle, write, or acquisition modes.

ΔV_{PD} equals either 460µA/V or 115µA/V in tracking mode, depending on the setting of the HGSEL bit in the control register as shown in Table 200.

Table 200Charge Pump and Pmult Gains

Mode	HGSEL	g_m	K_P
Idle/Write	x	460µA/V	1.0
Acquisition	x	460µA/V	1.0
Tracking	0	115µA/V	0.5
	1	460µA/V	1.0

The charge pump pumps the current differentially into an external capacitor C_{TR} producing an integrated voltage ΔV_{TR} across pins CTRP and CTRN. The IMULT block scales this voltage by a scaling factor I as shown below

$$I = 1.0 \quad \textit{(eq. 171)}$$

IMULT provides an integral gain term to the input of the VCO.

The PMULT block provides a proportional gain term to the VCO which sets the damping factor of the timing recovery loop. The gain P of PMULT changes with the mode of the timing recovery loop in a manner similar to that of the QPUMP. When the loop is switched from acquisition to tracking, the gain of PMULT is reduced by a factor of 2. PMULT gain P is shown in equation (eq. 172)

$$P = K_P \cdot \left(\frac{127 - K_{DAMP}}{127} \right) \quad \textit{(eq. 172)}$$

where K_{DAMP} is the value of the seven bit damping DAC DAMP(6:0), and K_P is the proportional multiplier gain which equals 1.0 in Idle and Acquisition mode, and equals either 1.0 or 0.5 in Tracking mode as shown in Table 200.

I_{REF} is the reference current for the VCO and is set by connecting an external resistor R_{TR} between RTR and VEE4 (pins 35 and 33), typically set to 5.6kΩ

$$I_{REF} = \frac{1.25V}{R_{TR}} \quad \textit{(eq. 173)}$$

The VCO center frequency is set by I_{REF} and the value of the frequency DAC

$$f_0 = k_I \cdot I_{REF} \cdot \left(1 + \frac{0.125}{32} \cdot K_{FRQ} \right) \quad \textit{(eq. 174)}$$

where k_I is 167.4MHz/mA and K_{FRQ} is the 2's complement value of either FRQN(13:<D7-D11>) or FRQT(14:<D7-D11>), depending on the value of TCDEN and level of TCD (see Track Cross Detector on page 73).

The VCO output frequency is determined by summing the IMULT and PMULT terms, modulating the VCO about its center frequency. The VCO frequency can be expressed as

$$VCO = f_0 \cdot (1 + k_V \cdot (I \cdot \Delta V_{TR} + P \cdot \Delta V_{PD})) \quad \textit{(eq. 175)}$$

where k_V is the VCO gain given by

$$k_V = 0.4V^{-1}$$

The VCO is divided by 2 to create the timing recovery clock frequency f_{TR}

$$f_{TR} = \frac{f_{VCO}}{2} \quad \textit{(eq. 176)}$$

Equations (eq. 168) - (eq. 176) can be combined and the closed loop response H(s) in the frequency domain can be expressed as

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$$H(s) = \frac{\theta_o}{\theta_i} = \left(\frac{\frac{K_{VCO}K_{PD}P}{2}\left(s + \frac{Ig_m}{PC_{TR}}\right)}{s^2 + \frac{K_{VCO}K_{PD}P}{2}s + \frac{Ig_m K_{VCO}K_{PD}}{2C_{TR}}} \right) \quad \textit{(eq. 177)}$$

where

$$_{VCO} = 2\pi \cdot f_0 \cdot k_V$$

This along with the open loop response G(s) can be rewritten using the conventional control system second order loop parameters ω_n, ζ, τ, and K as

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{K\left(s + \frac{1}{\tau}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textit{(eq. 178)}$$

and *(eq. 179)*

$$G(s) = \frac{\theta_o}{\theta_i} = \frac{K\left(s + \frac{1}{\tau}\right)}{s^2} \quad \textit{(eq. 180)}$$

where

$$\omega_n = \sqrt{\frac{Ig_m K_{VCO}K_{PD}}{2C_{TR}}} \quad \textit{(eq. 181)}$$

$$\zeta = \frac{P}{2}\sqrt{\frac{K_{VCO}K_{PD}C_{TR}}{2Ig_m}} \quad \textit{(eq. 182)}$$

$$\tau = \frac{PC_{TR}}{Ig_m} \quad \textit{(eq. 183)}$$

$$K = \frac{K_{VCO}K_{PD}P}{2} \equiv 2\pi \cdot f_C \quad \textit{(eq. 184)}$$

ω_n is known as the loop natural frequency
ζ is the loop damping factor
τ is the loop time constant
K is the loop gain in rad/s, which is also referred to as the unity gain frequency, crossover frequency, or loop bandwidth
f_C is the loop bandwidth (or loop gain) in Hz.

Note that user programmable K_{DAMP}, which controls the value of the PMULT gain P, controls both the gain K and damping factor ζ. As the value of K_{DAMP} is increased, the value of P is decreased and thus both the gain and damping factor are decreased. Only by selecting the value of the external capacitor C_{TR} (or changing TRGAIN) can the relative ratio of gain to damping factor be controlled.

When calculating loop stability, there is an additional phase shift which must be accounted for due to the time delay within both the FIR filter and DDPD associated with sampling. The FIR filter adds a delay of two clock cycles and the DDPD adds an additional two for a total delay of four timing recovery clock cycle delays. The phase shift in the frequency domain associated with a delay in the time domain is

$$\Delta\Phi = -\omega \cdot t_0 = -2\pi f \cdot 4T \quad \textit{(eq. 185)}$$

where t_0 is the delay which in this case equals four times the data rate period T which equals $1/f_{TR}$.

Phase margin Φ_R for the system can be derived by calculating the phase, or angle, of equation (eq. 180) and adding it to that of (eq. 185) at the cutoff frequency f_C, and making several substitutions.

$$\Phi_R = \tan^{-1}(4\zeta^2) - \frac{f_C}{f_{TR}} \cdot 4 \cdot 360° \qquad \textit{(eq. 186)}$$

where Φ_R is in degrees.

The user needs to choose the damping factor ζ and loop bandwidth f_C appropriately to achieve adequate phase margin for the system. The effect of the 4T phase shift can be significant for high values of f_C. The user must choose the loop gain sufficiently low so that this phase shift does not adversely affect the loop stability. For example at a data rate of 19.1385MHz a loop gain of 200kHz yields a $\Delta\Phi$ of 15°. For a damping factor of 1.0 this creates 60° of phase margin.

An additional factor must be accounted for in designing the loop dynamics and that is that both the acquisition and tracking timing gradient algorithms do not update the loop on every sample. In acquisition mode a '0' sample causes no loop update and in tracking mode consecutive '0' samples cause no loop update. This has the same effect as increasing the VCO feedback divider (which is equal to 2 in this part) which lowers both the loop gain and damping factor as can be seen by equations (eq. 182) and (eq. 184). Because of this the nominal loop gain can be set much higher than that determined by phase margin calculations based on the assumption that the data is unlikely to have regions free of '0' samples. Loop stability is data dependent and therefore the user should perform a statistical analysis with either simulation or real data before deciding upon final values for the various loop stability parameters. Favorable simulation results have been obtained on random data at 19.1385MHz with C=4.7nF, K_{DAMP}=30. With proper setting of the loop parameters, acquisition to random data should occur in less than 400 clock cycles.

Viterbi Detector

The Viterbi detector implements the maximum likelihood (ML) detector for PRML. It inputs sampled analog levels and outputs binary digital data. For a discussion of the Viterbi algorithm in the context of magnetic recording, the reader is directed to the article by Tom Matthews and Richard Spencer, "An Integrated Analog CMOS Viterbi Detector for Digital Magnetic Recording", IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, pp. 1294-1302.

The Viterbi detector block diagram is shown in Figure 163. The incoming signal (from the FIR filter via the timing recovery block) has been demultiplexed into the odd and even interleaves on a bit-by-bit basis. This is shown in the diagram as the odd interleave signal and the even interleave signal. Each interleave of the Viterbi detector runs at 1/2 the channel data rate, with the odd and even interleaves clocked on opposite phases of the half rate data clock, beginning with the even interleave. Each interleave independently processes its data stream. The data streams from the odd and even interleaves are then multiplexed back together on a bit-by-bit basis to yield the recovered bit stream.

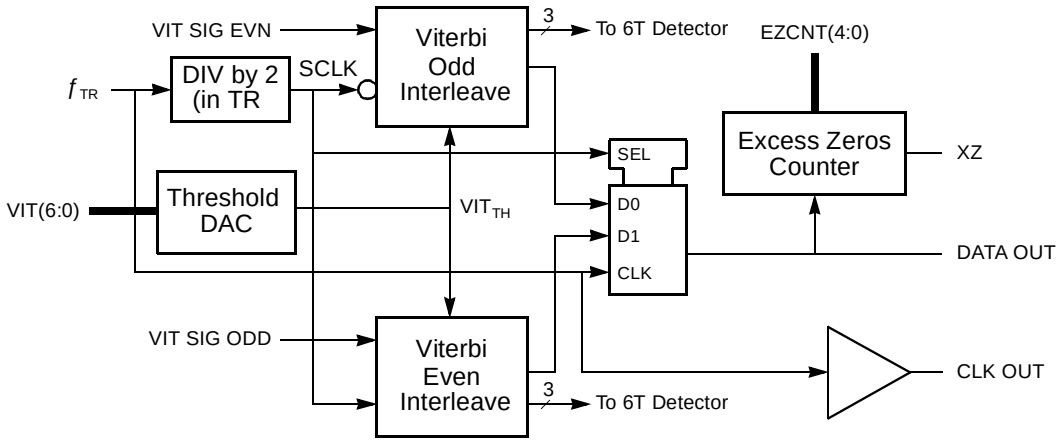


Figure 163 Viterbi Detector Block Diagram

The Viterbi detector operates in the continuous amplitude, discrete time domain. This is also known as the sampled domain. The detector compares the sampled level of the analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The nominal Viterbi threshold window size is set by a 7-bit DAC which is controlled by the Viterbi DAC serial control register 7-bit word VIT as shown below.

$$VIT_{TH} = 0.046 + 0.376 \cdot \left(\frac{K_{VIT}}{127}\right) \qquad \textit{(eq. 187)}$$

where K_{VIT} is the value of the VIT(6:0) Viterbi threshold DAC control word.

The AGC circuit adjusts the signal amplitude to ±250mV peak out of the continuous time filter. Side sampling for PR4 produces a nominal sampled signal amplitude of ±180mV out of the FIR, which is then resampled and split into the two interleave signals in the timing recovery phase detector. This is a pseudo-ternary signal with the ±1 levels equal to ±180mV and the zero level equal to 0mV. An ordinary ternary slicer would set the thresholds to ±90mV. The threshold difference would thus be 180mV. The actual detector used sets the thresholds dynamically by establishing a threshold window equal to 180mV nominally. The window moves with the data such that a comparison is always made on new data relative to the level of the previous data, rather than to an absolute sliced voltage.

Magnetic recording data consists of alternating positive and negative pulses. PR4 data is defined with two samples per pulse. The data into the Viterbi detector is pseudo-ternary, that is, it has valid levels of 0 and ±1 and is a result of binary data being converted into three levels due to the physics involved with writing to and reading from the magnetic media. There are thus restrictions in the data since not every combination of the three received levels is physically possible. This results in a condition that the interleaved data cannot have consecutive same-polarity '1' levels regardless of the number of intervening 0's. The interleaved data thus will consist of a series data pulses all of width 2T, alternating in polarity, where T is the period of the timing recovery clock. It is the utilization of this fact in the detection scheme which makes the Viterbi detector superior in performance when compared to a simple ternary slicer.

Figure 164 shows a block diagram of a Viterbi detector interleave. A new data sample is compared to the most recent '1' data sample, stored in the track and hold amplifier (T/H). The threshold window can be thought to "slide" up and down. For a previously received +1 sample, the threshold window slides up such that the top of the window is equal to the +1 voltage level. If the new sample is more positive than the top of the window, a logic '1' is output on the +1 output to the path memory and the window is slid up to the new value. If the new sample is more negative than the bottom of the window, a logic '1' is output on the -1 output to the path memory and the window is slid down so that the window bottom equals the new sample voltage. If the new sample is within the threshold window when compared to the previous '1' sample, a logic '0' is output on both the +1 and -1 outputs and the window stays where it is. For a previously received -1 sample, the threshold window slides down so the bottom of the window equals the -1 voltage level. If the next sample is more negative then the bottom of the window, a logic '1' is output on the -1 output to the path memory and the window slides down to the new value. If the new sample is more positive than the top of the window, then a 1 is output on the +1 output to the path memory and the window is slid up so the top of the window equals the new sample voltage. If the new sample falls within the threshold window, then a 0 is output on both the +1 and -1 outputs and the window stays where it is. Note that the held signal is always a +1 or -1 sample. 0 samples result in the T/H holding and the window not moving.

Thus, positive and negative thresholds in the Viterbi detector are modified based on the received data. These dynamic thresholds function to reject same-polarity pulses with lesser amplitude than that of the most recent pulse. For example, if there is a large positive data sample followed by a positive data sample with a smaller amplitude, only the first sample will be detected as a +1. Since magnetic recording data must have alternating polarity pulses, the case of receiving two +1 samples without an intervening -1 should never occur.

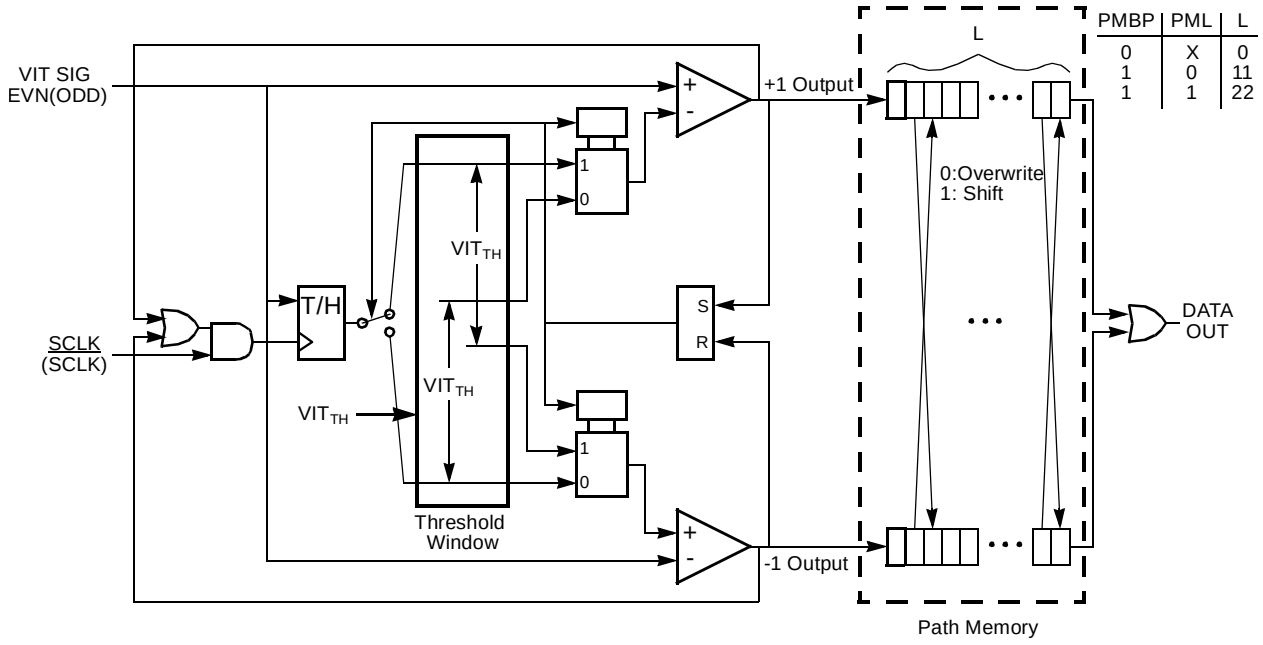


Figure 164 Viterbi Interleave Block Diagram

The path memory consists of two sets of shift registers, one for +1's and the other for -1's. The two shift register outputs are OR'd together to produce the DATA OUT signal. When a '1' is received in the input of either shift register, the contents of the remaining register locations in that shift register are overwritten with the contents of the other shift register. This acts to erase the first of two consecutive same-polarity samples. The shift register length is set with control register bit PML. With PML set to '0' the path memory

length is equal to eleven, and with PML set to '1' the path memory length is increased to twenty-two (the number of consecutive 0's allowed is equal to the path length minus one). Control register bit PMBP allows the path memory to be bypassed for test purposes. The path memory contents are set to zero when the internal PLL signal is low (see Figure 151 on page 70 and Figure 153 on page 71), which is true for all times except during tracking mode.

The error situation where two pulses on an interleave of the same polarity arrive without a pulse of the opposite polarity separating them can be divided into two cases: the first pulse is bigger than the second pulse or the second pulse is bigger than the first pulse. The Viterbi detector does not recognize the case where both pulses are of the same amplitude; it chooses one of the two pulses to be larger. For the following discussion, assume that two +1 pulses have occurred without a -1 pulse in between.

The case where the second pulse is smaller is handled by the dynamic thresholds in the Viterbi detector. The first (larger) pulse pulls the positive threshold up. The following pulse is smaller and therefore won't cross the upper threshold, thereby rejecting the smaller of the two +1 pulses.

The case where the second pulse is bigger than the first is handled by the path memory. The dynamic positive threshold is pulled up by the first +1 pulse and a +1 is output. The second +1 pulse comes along and exceeds the threshold set by the previous +1 pulse, causing a second '1' to be output to the path memory. This causes the +1 memory contents to be overwritten with the contents of the -1 path memory, which will erase the first +1. In order to do this erasure, the default path memory requires that no more than10 (or 21) zeros occur between the two 1's of the same polarity, according to the setting of the PML register bit.

The path memory overwrite is not just an error-correction event that happens on corrupt data, but is a normally occurring event. For example consider the case of a +180mV sample followed by a 0mV sample followed by a -180mV sample, and the threshold window set nominally to 180mV. The detector should detect this as a +1, 0, -1 sequence. The +180mV signal establishes the top of the window at +180mV and a +1 is sent to the path memory. The 0mV level is exactly the value of the threshold window below +180mV and will fall out of the bottom of the window only half the time and thus sometimes be flagged as a -1, and sometimes as a 0. If it doesn't fall out of the window, a 0 is detected and sent to the path memory. The next -180mV sample will certainly fall out of window sending a -1 to the path memory. In this case the sequence +1, 0, -1 is detected properly and the path memory need not do any overwriting. If the 0 does fall out of the window, a -1 is sent to the path memory and the window bottom "moves" to 0mV. The next sample of -180mV is lower than 0mV and thus it too registers as a -1. The sequence is now incorrectly detected as +1, -1, -1. The path memory, however, will take care of this problem as it will overwrite the first -1 level as a 0 upon receiving the second -1 level, and the proper +1, 0, -1 sequence is detected at the path memory output.

The Viterbi detector has two sets of test signals: Vit Sig Odd and Vit Sig Evn; and Held Sig Odd and Held Sig Evn (see Table 201 and Table 202). Vit Sig Odd and Vit Sig Evn are the inputs to either interleave of the Viterbi detector. These signals are held any time a '1' is detected for purposes of computing the difference metric. The held signals are output as Held Sig Odd and Held Sig Evn.

The Viterbi detector also has a programmable counter that counts the number of consecutive zeros occurring in the recovered data stream. If the number of consecutive zeros exceeds the count programmed with the EZCNT control register bits, the excess zeros (XZ) output (pin 43) is raised; XZ stays high until a valid 1 resets the counter and causes it to drop. This feature is intended to aid in the rapid detection of tape drop outs. The excess zero count EZC is equal to the value of the EZCNT(4:0) DAC as shown in equation (eq. 188)

$$EZC = 0.5 + K_{EZCNT} \qquad \textit{(eq. 188)}$$

where K_{EZCNT} is the value of the EZCNT control word and ranges from 0 to 31. EZC is always 1.5 clock cycles longer than the DAC setting.

Table 2016T Detector Operation

EN6T	STL	ADPHLD	FIR Pattern	SIXT	Adaptation State
0	X	0	X	0	Normal
0	X	1	X	0	Hold
1	X	1	X	X	Hold
1	0	0	> 4 6T's	1	Hold
1	0	0	< 4 6T's	0	Normal
1	1	0	> 8 6T's	1	Hold
1	1	0	< 8 6T's	0	Normal

The first three bits in both the even or odd path memory interleaves are used in the 6T detector. The 6T detector senses a bit pattern of 1 1 0 -1 -1 0 (as seen at the FIR output) and activates the adaptive hold feature of the adaptive FIR when either 4 or 8 consecutive 6T bit patterns are detected. Control register bit STL (7:<D27>) sets the count at either 4 (STL='0') or 8 (STL='1'). The 6T detector output SIXT will go high when the pattern is detected and goes low whenever any one bit in the pattern is incorrect. The SIXT signal

can be monitored on CT2 (pin 57), see TEST MODES on page 106. When SIXT is high the adaptation algorithm is held; when it is low the adaptive hold feature is controlled by the ADPHLD (pin 48). The ADPHLD pin can also override the action of the 6T detector. Control register bit EN6T enables the 6T detector when set to a '1'. Table 201 illustrates the operation of the 6T Detector. Due to the latency through the Viterbi Detector, there will be a delay of 10 clock cycles plus a fixed propagation delay before SIXT is seen to switch relative to the FIR output. Figure 165 shows a timing diagram for the 6T detector illustrating the latency between the FIR output, even and odd pathmemory bits, and the SIXT output (note that the even and odd path memory bits are delayed from the VIT SIG Even and Vit SIG Odd test points).

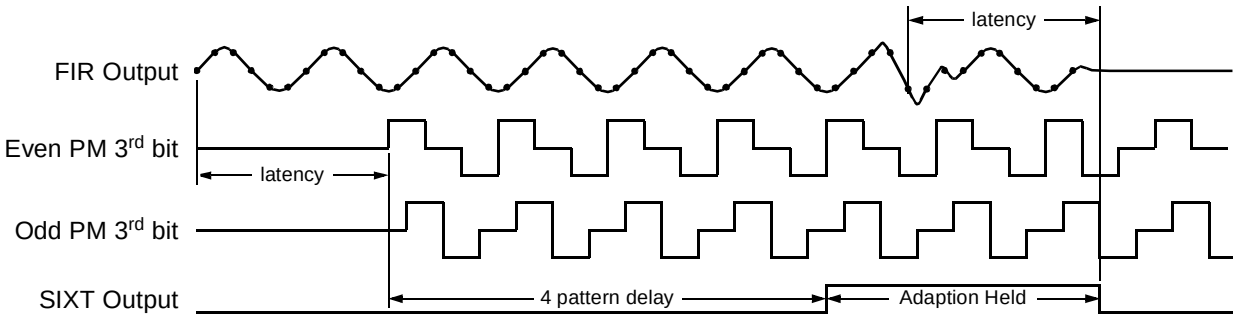


Figure 165 6T Detector Timing, STL='0'

Write Circuitry

A reference write current is provided for a preamplifier which gains this reference current up by a factor of 20. The sink for this reference current on the preamp must be a low impedance of 1.5V or greater. The write current reference is five bit programmable with a nominal range of 0 to 2mA. This reference current is derived from an external resistor R_{WC} connected from pin RWC to VEE3 (pins 17 and 16 respectively) which typically equals 4.7kΩ. The write current I_{WC} is expressed as

$$I_{WC} = \frac{1.25V}{R_{WC}} \cdot \frac{K_{WC}}{4} \qquad \textit{(eq. 189)}$$

where K_{WC} is the value of the 5-bit WC control register word and varies from 0 to 31.

The part also has a TTL to differential ECL write data level converter which takes a TTL input signal on WDI (pin 19) and outputs a differential pseudo ECL signal on WDP and WDN (pins 25 and 26). WDP and WDN are emitter follower outputs which will need external load resistors for proper operation. These may be 50Ω to a potential 2V below V_{CC}, or 200Ω to 1kΩ to V_{EE}.

Mode Control and Power Management

The fundamental operating modes are controlled by power down (PD pin 52), read gate (RG pin 49), and write gate (WG pin 50) inputs. If PD is high, the entire chip is powered down. If PD, WG, and RG are all low the part is in idle mode where the AGC loop locks to input data, the timing recovery loop locks to the reference, and the FIR and Viterbi detector are powered down. If PD and RG are low and WG is high, the part is in write mode where the timing recovery loop locks to the reference, AGC loop holds, the VGA is squelched and the input switches to low impedance. If PD is low and RG is high, the part is in read mode, behaving as described in Gain Control on page 67. Both read mode and write mode are asynchronous states and may be initiated or terminated at any time. A power reduction bit PREN (10:<D0>) in the control register when set to a '1' causes the FIR, Viterbi, and decision-directed phase detector (DDPD) to power down in idle and write modes. A summary of the Mode Control is shown below in Table 202.

Table 202Mode Control

PD	PREN	RG	WG	MODE
1	X	X	X	Entire chip powered down, serial port still functional
0	0	0	0	IDLE mode, all blocks powered on
0	0	0	1	WRITE mode, all blocks powered on
0	0	1	X	READ mode, all blocks powered on
0	1	0	0	IDLE mode, FIR, Viterbi, DDPD powered off
0	1	0	1	WRITE mode, FIR, Viterbi, DDPD powered off
0	1	1	X	READ mode, all blocks powered on

DIGITAL CONTROL VIA SERIAL INTERFACE

Programmable control of the chip is performed through a serial digital interface and a 16 word,12-bit wide register file. Control information is stored in the register file and used directly as digital control lines or sent to one of the onboard DACs to create analog control signals. The interface consists of three CMOS-level signals for input/output data, clock, and enable. Upon asserting SPEN (pin 54), the serial port is enabled and ready for input on SPDATA (pin 55) which is clocked by SPCLK (pin 53). The SPDATA line provides the read/write, address and data information. Head Select (pin 51) selects between two parameter sets for either Head0 or Head1.

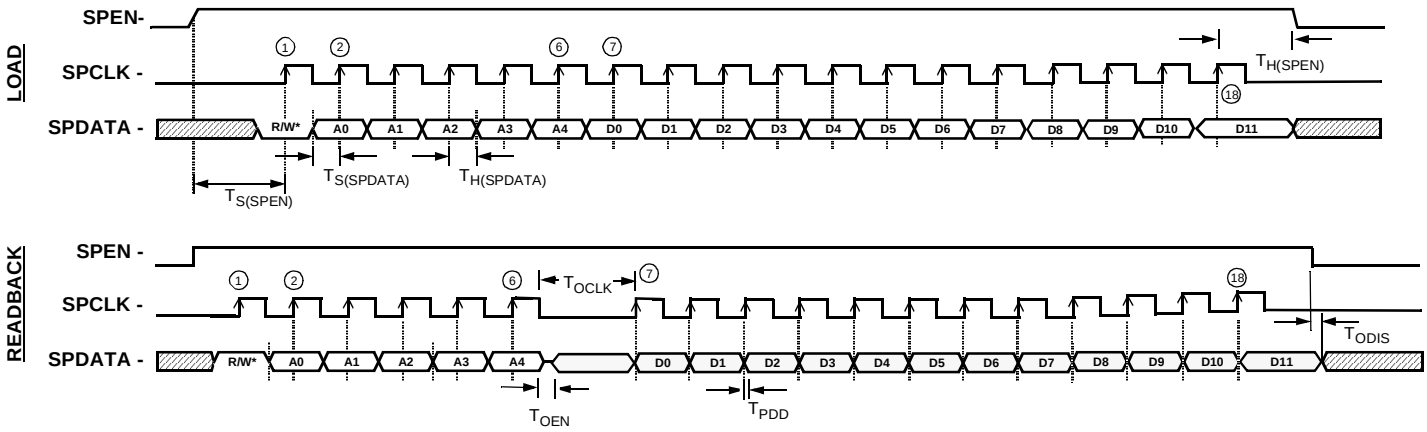


Figure 166 Serial Interface Load & Readback Timing

Serial Interface Timing>

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SPCLK period	T		50			ns
SPEN set-up time	$T_{S(SPEN)}$	Relative to SPCLK ↑	40			ns
SPEN hold time	$T_{H(SPEN)}$	Relative to SPCLK ↑	50			ns
SPEN high to low to high			50			ns
SPDATA set-up time	$T_{S(SPD}$	Relative to SPCLK ↑	20			ns
SPDATA hold time	$T_{H(SPD)}$	Relative to SPCLK ↑	5			ns
SPDATA enable	T_{OEN}	Relative to SPCLK ↓	5			ns
SPCLK low time	T_{OCLK}	Relative to SPCLK ↓	30			ns
SPDATA disable	T_{ODIS}	Relative to SPEN ↓			30	ns
SPDATA prop. delay	T_{PDD}	Relative to SPCLK ↑			10	ns

MIXED SIGNAL CIRCUITS

Table 203Programmable Register Bit Allocation

Reg. Addr.	Data Bit											
	11	10	9	8	7	6	5	4	3	2	1	0
0	PGC: Prog. Gain Control DAC				SQPI		FIR0: FIR Tap 0					rsrv'd
1	ITCD: I_{TCD} Control			rsrv'd	rsrv'd	TFAQ	FIR4: FIR Tap 4					rsrv'd
2	GDH0: CTF Data Group Delay, Head 0						FIR1H0: FIR Tap 1, Head 0					
3	GDH1: CTF Data Group Delay, Head 1						FIR1H1: FIR Tap 1, Head 1					
4	rsrv'd	rsrv'd	rsrv'd	rsrv'd	PGCEN	DHBW	FIR3H0: FIR Tap 3, Head 0					
5	rsrv'd	rsrv'd	rsrv'd	rsrv'd	rsrv'd	rsrv'd	FIR3H1: FIR Tap 3, Head 1					
6	rsrv'd	rsrv'd	rsrv'd	rsrv'd	rsrv'd	TC13	TC2	FIR2: FIR Tap 2				
7	rsrv'd	rsrv'd	rsrv'd	TCDEN	TRK-SEL	HGSEL	SLEEP	PRST	EN6T	STL	PML	PMBP
8	TCDTH: Track Cross Detector Threshold DAC					VIT: Viterbi Threshold DAC						
9	rsrv'd	rsrv'd	rsrv'd	SYMC		DAMP: Damping Ratio DAC						
10	EZCNT: Excess Zeros Count					LPFBYP	PDTST	SELTE	CLK-SEL	CLCKE	COAST	PREN
11	HLD	FCH0: CTF Data Fc DAC, Head 0					BSTH0: CTF Data Boost DAC, Head 0					
12	CMXEN	FCH1: CTF Data Fc DAC, Head 1					BSTH1: CTF Data Boost DAC, Head 1					
13	FRQN: VCO Center Frequency DAC, normal play					rsrv'd	rsrv'd	rsrv'd	rsrv'd	TP1SEL: TP1 Test Mux Select		
14	FRQT: VCO Center Frequency DAC, trick play					rsrv'd	rsrv'd	rsrv'd	rsrv'd	TSEL: Test Mux Select		
15	WC: Write Current DAC					DAGC	DPLL	BMXEN	AGCSFC		PLLSFC	
24	AE	DZ		INTL		rsrv'd	ITW		ACTST		TWR	

MIXED SIGNAL CIRCUITS

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
0	5:1	FIR0: FIR Outer Tap 0, 2's complement	$K_0 = 0.0195 \cdot K_{FIR0}$ in V/V $-16 \le K_{FIR0} \le 15$
	7:6	SQPI: AGC Sampled charge pump current DAC	$I_Q = I_{QNC} \cdot K_{SQPI}$ $0 \le K_{SQPI} \le 3$, $I_{QNC} = 1.2/(20 \cdot R_{AF})$
	11:8	PGC: Programmable gain control DAC	$A_V = 2.24 + 2.8 \cdot K_{PGC}$ in V/V $0 \le K_{PGC} \le 15$
1	5:1	FIR4: FIR Outer Tap 4, 2's complement	$K_4 = 0.0195 \cdot K_{FIR4}$ in V/V $-16 \le K_{FIR4} \le 15$
	6	TFAQ: Test Fast Acquisition. Allows for testing of ultra fast decay current.	0: Normal Mode 1: Test Mode (Fast Acquisition always on)
	11:9	ITCD: Track Cross Detector decay current control	$I_{TCD} = \frac{0.065}{R_{AF}}(K_0 + 4 \cdot K_I + 16 \cdot K_2)$ $0 \le K_{ITCD} \le 7$
2	5:0	FIR1H0: FIR Inner Tap 1, Head 0, 2's complement	$K_1 = (0.0195 \cdot K_{FIR1H0}) - K_{TC13}$ in V/V $K_{TC13} = 0.3125$ for TC13=0 $K_{TC13} = 0$ for TC13=1 $-32 \le K_{FIR1H0} \le 31$
	11:6	GDH0: Continuous time filter Group Delay, Head 0, 2's complement	$GD_{DC} = 0.95 \cdot K_{GDH0}$ in% $-32 \le K_{GDH0} \le 31$
3	5:0	FIR1H1: FIR Inner Tap 1, Head 1, 2's complement	$K_1 = (0.0195 \cdot K_{FIR1H1}) - K_{TC13}$ in V/V $K_{TC13} = 0.3125$ for TC13=0 $K_{TC13} = 0$ for TC13=1 $-32 \le K_{FIR1H1} \le 31$
	11:6	GDH1: Continuous time filter Group Delay, Head 1, 2's complement	$GD_{DC} = 0.95 \cdot K_{GDH1}$ in% $-32 \le K_{GDH1} \le 31$
4	5:0	FIR3H0: FIR Inner Tap 3, Head 0, 2's complement	$K_3 = (0.0195 \cdot K_{FIR3H0}) - K_{TC13}$ in V/V $K_{TC13} = 0.3125$ for TC13=0 $K_{TC13} = 0$ for TC13=1 $-32 \le K_{FIR3H0} \le 31$
	6	DHBW: Disable High Bandwidth Mode of AGC. Forces FAQ to remain low. (See Figure 150 on page 70 and Figure 151 on page 70.)	0: Normal Mode 1: Disable high bandwidth
	7	PGCEN: Programmable gain control enable for VGA. Allows the VGA gain to be adjusted through PGC DAC.	0: Normal Mode (AGC loop active) 1: Programmable Gain Mode

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
5	5:0	FIR3H1: FIR Inner Tap 3, Head 1, 2's complement	$K_3 = (0.0195 \cdot K_{FIR3H1}) - K_{TC13}$ in V/V K_{TC13} = 0.3125 for TC13=0 K_{TC13} = 0 for TC13=1 $-32 \le K_{FIR3H1} \le 31$
6	4:0	FIR2: FIR Center Tap 2	$K_2 = (0.0195 \cdot K_{FIR2}) + K_{TC2}$ in V/V K_{TC2} =1.094 for TC2=0 K_{TC2} =0 for TC2=1 $0 \le K_{FIR2} \le 31$
	5	TC2: Tap Centering, 2nd tap. Controls gain offset in FIR center tap (tap 2).	0: Normal Mode$1.094 < K_2 < 1.699$ 1: Test Mode$0 < K_2 < 0.605$
	6	TC13: Tap Centering, 1st and 3rd taps. Controls gain offset in FIR taps 1 and 3.	0: Normal Mode$-0.937 < K_1,K_3 < +0.293$ 1: Test Mode$-0.624 < K_1,K_3 < +0.605$
7	0	PMBP: Path Memory Bypass. Allows the path memory to be bypassed in the Viterbi detector.	0: Normal Viterbi Path length 1: Viterbi Path Length = 0
	1	PML: Path Memory Length. Allows Viterbi path length to be increased to 21 from 10.	0: Viterbi Path Length = 10 1: Viterbi Path Length = 21
	2	STL: 6T Length. Programs the number of 6T cycles to be detected before switching the SIXT signal high and activating the adaptive hold feature.	0: 6T length = 4 cycles 1: 6T length = 8 cycles
	3	EN6T: 6T Detector Enable. Enables 6T Detector	0: 6T Detector disabled 1: 6T Detector enabled
	4	PRST: Programmable Reset. Allows internal flip flops to be reset for test purposes. A '1' forces a reset, a '0' releases the reset.	0: Normal Mode 1: Resets flip flops $VIT_{TH} = 0.047 + 0.376\left(\frac{K_{VIT}}{127}\right)$
	5	SLEEP: Enables low power sleep mode	0: Normal (Powered On) Mode 1: Power Off Mode
	6	HGSEL: High Gain Select. Allows timing recovery charge pump g_m and PMULT gain P to stay at the higher acquisition values in tracking mode.	0: Normal Mode 1: Acq. g_m and K_P used in Tracking Mode
	7	TRKSEL: Tracking Select. Forces the timing gradient in acquisition mode to that used in tracking mode	0:Normal Mode 1:Tracking mode timing gradient used in acquisition mode
	8	TCDEN: Track Cross Detector Enable.	0: Normal Mode 1: Track Cross Detector enabled

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
8	6:0	VIT: Viterbi threshold DAC	in Volts $0 \le K_{VIT} \le 127$
	11:7	TCDTH: Track Cross Detector Threshold.	$V_{TH} = \frac{V_{PK}}{1 + \frac{4}{1 + 2 \cdot K_{TCDTH}}}$ in Volts $0 \le K_{TCDTH} \le 31$, V_{PK} equal to peak value of $4V\text{-}V_{CAGC}$
9	6:0	DAMP: Damping Ratio DAC	$P = K_P \cdot \left(\frac{127 - K_{DAMP}}{127}\right)$ $\zeta = \frac{P}{2}\sqrt{\frac{K_{VCO}K_{PD}C}{Ig_m}}$ $0 \le K_{DAMP} \le 127$ K_P= P-multiplier gain K_{VCO} = VCO gain K_{PD}= Phase detector gain (PFD in non-data mode, DDPD in data mode) C = Value of external capacitor C_{TR} I = I-multiplier gain g_m = QPUMP gain
	8:7	SYMC: Symmetric Control. Determines which if any of the taps will be symmetrically adjusted. See FIR Filter/Equalizer on page 82 for details.	00: (1 & 3) symmetric 01: (0 & 4) symmetric 10: (1 & 3) & (0 & 4) symmetric 11: no taps symmetric
	11:9	ZPR DAC: Zero Phase Restart DAC. Determine the time before first sample is taken on the Sync Field 6T pattern.	Nominal setting: 100 = 0 ns 111 9 ns CLK late 110 6 ns 101 3 ns 100 0 ns 011 -3 ns 010 -6 ns 001 -9 ns 000 -12 ns

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
10	0	PREN: Power Reduction Enable. Allows the FIR, Viterbi and Decision-directed phase detector (DDPD) to power off in write mode and idle mode.	0: All blocks powered on in write/idle mode 1: FIR/Viterbi/DDPD powered off in write/idle mode
	1	COAST: Disables phase detector in timing recovery loop during idle mode allowing the loop to coast over a track crossing.	0: Phase detector enabled (Normal Mode) 1: Phase detector disabled (Coast Mode)
	2	CLCKE: Selects edge of CLCK output with which DATA is clocked out.	0: DATA switches on positive CLCK edge 1: DATA switches on negative CLCK edge
	3	CLKSEL: Clock Select. Allows external FDSP/N input to replace timing recovery VCO.	0: TIming Recovery VCO (Normal Mode) 1: External FDSP/N input
	4	SELTE: Selects Timing Error. Outputs either the DDPD or AC coupled filter, which typically is set by the RLZ/RFSR input through LPFBYP.	0: DDPD Timing Error (Normal Mode) 1: AC Coupled filter output (Test Mode)
	5	PDTST: Phase Detector Test. Allows AC coupled filter output to be input directly into decision directed phase detector input, bypassing the FIR. When used with LPFBYP allows external DC signal on RLZ and RFSR to be used as DDPD inputs	0: Normal Mode 1: Bypass FIR
	6	LPFBYP: Low Pass Filter Bypass. Allows differential test signal to be input after the internal AC Coupling Caps. The differential test signal is input on the RLZ and RFSR pins at a level >2V.	0: Normal Mode 1: Test Mode (lowpass filter bypassed)
	11:7	EZCNT: Excess zeros count.	$EZC = K_{EZCNT}$ $0 \le K_{EZCNT} \le 31$
11	4:0	BSTH0: Continuous time filter Boost, Head 0	See Graph 4 on page 79
	10:5	FCH0: Frequency Cutoff Head 0. Cutoff Frequency of continuous time LPF for Head 0	$f_c = (0.2 \cdot K_{FCH0} + 5) \cdot \frac{6}{R_{AF}}$ in MHz $0 \le K_{FCH0} \le 63$, R_{AF} in kΩ
	11	HLD: Hold mode for AGC and timing recovery loops.	0: Normal operation. 1: Both AGC and timing recovery loops forced into a hold mode. Intended for coasting over thermal asperities and test.
12	4:0	BSTH1: Continuous time filter boost, Head 1	See Graph 4 on page 79
	10:5	FCH1: Frequency Cutoff Head 1. Cutoff frequency of continuous time LPF for Head 1	$f_c = (0.2 \cdot K_{FCH1} + 5) \cdot \frac{6}{R_{AF}}$ in MHz $0 \le K_{FCH1} \le 63$, R_{AF} in kΩ
	11	CMXEN: CMOS Mux Enable. CMOS test point muxes enable	0: CMOS Test Muxes disabled (Normal Mode) 1: CMOS Test Muxes enabled

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
13	2:0	TP1SEL: Test Point 1 Select. Selects which internal to MUX out to the TP1 test point	See Table 205 on page 106
	11:7	FRQN: Frequency of Normal. VCO center Frequency DAC, Normal Play	$f_{TR} = f_{TR0}\left(1 + \frac{0.125}{32} \cdot K_{FRQN}\right)$ in MHz $-16 \le K_{FRQN} \le 15$
14	2:0	TSEL: Test Select. Output test mux select.	See Table 206 on page 107
	11:7	FRQT: Frequency of Trick. VCO center Frequency DAC, Trick Play	$f_{TR} = f_{TR0}\left(1 + \frac{0.125}{32} \cdot K_{FRQT}\right)$ in MHz $-16 \le K_{FRQT} \le 15$

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
15	1:0	PLLSFC: PLL Sync Field Count: Determines the number of data rate clock cycles after the AGC signal switches high that the PLL signal switches high, defining the start of tracking mode.	00: 0 bytes (0 cycles) 01: 1 byte (8 cycles) 10: 2 bytes (16 cycles) 11: 3 bytes (24 cycles)
	3:2	AGCSFC: AGC Sync Field Count: Determines the number of data rate clock cycles after READ has switched high that the AGC signal switches high, defining the start of the sampled AGC mode	00: 4 bytes (32 cycles) 01: 5 bytes (40 cycles 10: 7 bytes (56 cycles) 11: 9 bytes (72 cycles)
	4	BMXEN: Bipolar test point Muxes Enable	0: Bipolar Test Muxes disabled (Normal Mode) 1: Bipolar Test Muxes enabled
	5	DPLL: Disable PLL. Allows the internal PLL signal to be programmably enabled/disabled for test purposes. PLL is asserted at the transition from acquisition mode to tracking mode	0: PLL count enabled (Normal Mode) 1: PLL count disabled
	6	DAGC: Allows the internal AGC signal to be programmably enabled/disabled for test purposes. AGC is asserted once the AGC count is reached in the Sync Field	0: AGC count enabled 1: AGC count disabled
	11:7	WC: Write Current reference DAC	$I_{WC} = \frac{1.25V}{R_{WC}} \cdot \frac{K_{WC}}{4}$ $0 \le K_{WC} \le 31$

MIXED SIGNAL CIRCUITS

Table 204Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
24	2:0	TWR: Tap Weight Rollover value. Determines which of the FIR taps will be adapted by determining which tap gets adapted following Tap 3. The adaption sequence order of the taps is fixed, only the starting point is changed (see Viterbi Detector on page 92 for more details).	00: Tap order 0, 4, 1, 3, 0, 4,1, 3 etc. 01:.Tap order 4, 1, 3, 4, 1, 3, 4 etc. 10: Tap order 1, 3, 1, 3, 1, 3 etc. 11: Tap order 3, 3, 3, etc.
	3:2	ACTST: Adaption Control Test. Allows the adaption circuitry to be tested by forcing either an up, down or hold signal. See FIR Filter/Equalizer on page 82 for details.	0: Normal operation 1: Up forced 2: Down forced 3: Hold forced
	6:5	ITW: Initial Tap Weight. Determines which tap the adaption routine will adapt first (see Viterbi Detector on page 92 for more details).	00: Tap 0 01:.Tap 4 10: Tap1 11: Tap 3
	8:7	INTL: Integration Length. Determines the number of cycles the adaption circuit will integrate over when deciding whether the current tap weight should be incremented, decremented or held (see Viterbi Detector on page 92 for more details).	00:12 cycles 01:15 cycles 10:18 cycles 11: 21 cycles
	10:9	DZ: Dead Zone. Determines the threshold as a percentage of integration length that the adaption integrator must exceed in either the up or down direction to qualify an increment or decrement decision. If this threshold is not reached then the current tap weight is simply held (see Viterbi Detector on page 92 for more details).	00: 35% 01: 50% 10: 65% 11: 80%
	11	AE: Adaption Enable. Enables the adaption circuitry	0: Adaption circuit NOT active 1: Adaption circuit enabled

TEST MODES

There are seven sets of test points used in the VM65015. TP1P/N and TP2P/N (pins 5, 6, 7 and 8 respectively) are differential analog test outputs, pins TP3P/N and TP4P/N (pins 23, 24, 27 and 28 respectively) provide differential digital pseudo ECL test outputs, and CT1 and CT2 (pins 56 and 57 respectively) are digital CMOS test outputs. TP1, TP2, TP3, and TP4 are activated by control register enable bit BMXEN (15:<D4>), while CT1 and CT2 are activated by enable register bit CMXEN (12:<D11>). The TP1 output is controlled by the TP1SEL[2:0] control register bits (13:<D0-D2>). TP2,3,4 and CT1 and CT2 are controlled by bitsTSEL[2:0] (14:<D0-D2>), as shown in Table 205 and Table 206. A description of the signals used in the tables is given in Table 207. The LPFBYP register bit (10:<D6>) when set to a '1' allows a differential input signal applied to RLZ and RFSR (pins 64 and 63) to be input to the datapath after the continuous time filter AC coupling capacitors. This allows a signal to be input directly in the FIR. The PDTST bit (10:<D5>) allows the FIR to be bypassed and the test signal input directly into the decision directed phase detector (DDPD). The SELTE bit (10:<D4>) allows this test signal to be input at the Timing Error output of the DDPD for purposes of testing the charge pump and PMULT.The voltage level for both RLZ and RFSR must be kept above 2V to keep the normal RLZ and RFSR biasing circuitry from turning on. Register bits TC2 and TC13 (6:<D5> and 6:<D6>) shift the gain of FIR taps 2 and 1 and 3 as shown in Table 199 on page 84.

Table 205TP1 Test MUX Decode

BMXEN	TP1SEL[2:0] bits			mode	Output pin
	2	1	0		TP1 (diff analog)
1	0	0	0	0	CTF ac
1	0	0	1	1	VGA Out
1	0	1	0	2	Vit Sig Odd
1	0	1	1	3	Vit Sig Evn
1	1	0	0	4	Held Sig Odd
1	1	0	1	5	FIR Out
1	1	1	0	6	VCO Control
1	1	1	1	7	VGA In
0	X	X	X	X	power down.

Table 206Test Mode Register Decode

BMXEN	CMXEN	TSEL[2:0] bits			mode	Output pins				
		2	1	0		TP2 (diff analog)	TP3 (PECL)	TP4 (PECL)	CT1 (CMOS)	CT2 (CMOS)
1	1	0	0	0	0	Held Sig Evn	f_{2TR}	f_{TR}	rsrv'd	rsrv'd
1	1	0	0	1	1	Timing Error	SCLK	f_{TR}	LZDEL	FRDEL
1	1	0	1	0	2	VGA Out	f_{2TR}	f_{TR}	HLDEL	READ
1	1	0	1	1	3	Vit Sig Odd	MX	T0	TCD	READ
1	1	1	0	0	4	CTF	YHB/YLB	XPB/XNB	AGCN	PLLN
1	1	1	0	1	5	CTF ac	TRUP	TRDN	SHGN	SIXT
1	1	1	1	0	6	Int_ε	ε_n	C_n	EA	ρσρϖɜδ
1	1	1	1	1	7	Vit Sig Evn	X_O	X_E	rsrv'd	rsrv'd
0	1	X	X	X	X	power down	power down	power down	modes 0-7	modes 0-7
1	0	X	X	X	X	modes 0-7	modes 0-7	modes 0-7	power down	power down

Table 207 Test Signal Descriptions

Test Signal Name	Description
CTF ac	AC coupled output of the Continuous Time Filter
VGA Out	Analog output of the Variable Gain Amplifier of the AGC loop
Vit Sig Evn	The even FIR interleave input to the Viterbi detector
Held Sig Odd	Held signal value for the odd interleave of Viterbi detector
FIR Out	Output of the Finite Impulse Response filter
VCO Control	Analog control input to the Timing Recovery VCO
VGA in	Analog input to the Variable Gain Amplifier of the AGC loop
Held Sig Evn	Held signal value for the even interleave of Viterbi Detector
Timing Error	Timing error for the Timing Recovery Loop
Vit Sig Odd	The odd FIR interleave input to the Viterbi detector
CTF	Output of the Continuous Time Filter
Int_Ɛ	Integrated lms tap weight error
SCLK	f_{TR} signal divided by 2 used as a sampling clock in the Timing Recovery and Viterbi sections
f_{TR}	Timing recovery clock equal to the VCO (or external clock) divided by 2
f_{2TR}	VCO (or external clock) output with frequency 2X f_{TR}
MX	FIR mux0 to mux1 transition
T0	FIR track and hold 0 control signal
YHB/YLB	AGC pump up (=0) / down (=1) in sampled mode, qualified by XPB/XNB signal = 1

Table 207 Test Signal Descriptions

Test Signal Name	Description
XPB/XNB	AGC positive/negative sample sign indicator. Equivalent to (X1 xor X2)
TRUP	Pump up signal into the charge pump of the Timing Recovery loop in idle mode
TRDN	Pump down signal into the charge pump of the Timing Recovery loop in idle mode
ε_n	Sign of the PR4 equalization error estimate
C_n	Sign of the Channel data
X_O	Odd sample sign indicator for decision-directed phase detector in the timing recovery
X_E	Even sample sign indicator for decision-directed phase detector in the timing recovery
LZDEL	One-shot pulse which controls how long the AGC loop stays in low impedance mode
FRDEL	One-shot pulse which controls how long the AGC loop stays in fast acquisition mode
HLDEL	HOLD control signal for the AGC loop
READ	Read signal. Internal control signal which is delayed from FRDEL by two bytes after a dropout, and delayed from RG by two bytes after RG switches high.
AGCN	Internal control signal indicating when the AGC loop switches from the continuous time loop to the sampled time loop (active low).
PLLN	Internal control signal indicating when the timing recovery loop switches from decision- directed acquisition mode to decision-directed tracking mode (active low).
SHGN	Internal control signal indicating when the AGC loop is in the high-gain sampled mode, equal to the exclusive NOR of AGCN and PLLN (active low)
SIXT	6T Detector output. Goes high after 4 or 8 6T cycles have been detected.
EA	Enable for Adaption register write. Goes high when int_ε signal crosses DZ threshold voltage.

PIN FUNCTIONS AND DESCRIPTIONS

Table 208VM65015 Pin Functions and Descriptions

PIN TYPE	PIN NAME	PIN#	INFORMATION
Power Pins	VCC1	3	CT filter, analog AGC, analog test mux power
	VCC2	40	FIR filter, Viterbi detector, timing recovery power
	VCC3	15	Write current reference power
	VCC4	34	Timing recovery VCO analog power
	VCC5	21	Write Data and test point ECL output and TTL input power
	VCC6	59	Internal digital CMOS and tub connection power
	VCC8	37	Viterbi digital CMOS and tub connection power
	VDD	47	3.3/5 V CMOS interface circuitry power

Table 208VM65015 Pin Functions and Descriptions

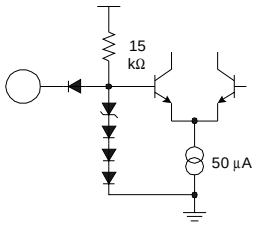
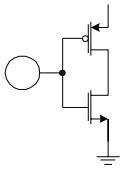
PIN TYPE	PIN NAME	PIN#	INFORMATION	
Ground Pins	VEE1	4	CT filter, analog AGC, analog test mux ground	
	VEE2	39	FIR, Viterbi detector, timing recovery ground	
	VEE3	16	Write current reference ground	
	VEE4	33	Timing recovery VCO analog ground	
	VEE5	20	Write Data and test point ECL output ground	
	VEE6	58	Internal digital CMOS ground	
	VEE7	38	Bipolar substrate connection	
	VEE8	36	Viterbi digital CMOS ground	
	VSS	46	3.3/5 V CMOS interface circuitry ground	
5V Bipolar TTL Inputs	WDI	19	Write Data In from microcontroller. This input is converted to a PECL signal and output on pins WDP and WDN. WDI is also used as the test input clock to the VCO	
	FREF	22	19.1385 MHz input reference frequency	
3.3/5V CMOS TTL Inputs	ADPHLD	48	Adaptive FIR Hold (active high)	
	RG	49	Read Gate. Selects read mode (active high)	
	WG	50	Write Gate. Selects write mode (active high)	
	HDSEL	51	Head Select. Low selects Head 0 registers, high selects Head 1 registers, transition initiates head switch sequence	
	PD	52	Power down control signal. When this signal is asserted, the chip is powered down. (active high)	
	SPCLK	53	Serial port clock (latch on positive edge)	
	SPEN	54	Serial port I/O enable (active high)	
5V CMOS Outputs	CT1	56	CMOS Test Output 1	
	CT2	57	CMOS Test Output 2	

Table 208VM65015 Pin Functions and Descriptions

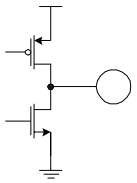
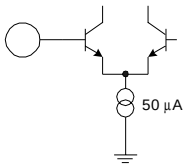
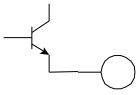
PIN TYPE	PIN NAME	PIN#	INFORMATION	
3.3/5V CMOS Outputs	CLCK	41	Recovered Clock.	
	DATA	42	Recovered Data.	
	XZ	43	eXcess Zeros. High level indicates number of consecutive zeros in recovered data has exceeded a programmable value.	
5V CMOS Bidirectional Input/Outputs	SPDATA	55	Bidirectional serial port data signal	
Pseudo ECL Differential Inputs	FDSP FDSN	29 30	Timing Recovery (Data Separator) test Frequency input	
Pseudo ECL Differential Outputs, V_{CC} referenced	WDP WDN	25 26	Write data output	
	TP3P TP3N	23 24	Digital Bipolar Test point 3 output	
	TP4P TP4N	27 28	Digital Bipolar Test point 4 output	

Table 208VM65015 Pin Functions and Descriptions

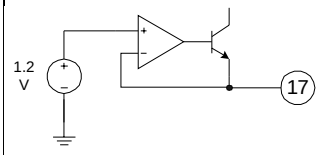
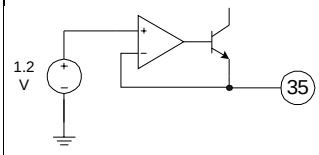
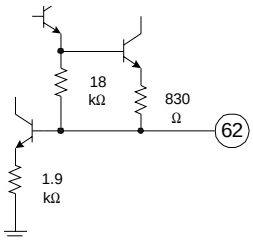
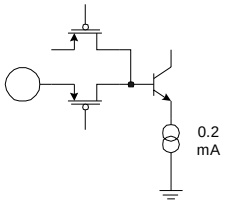
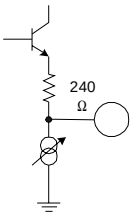
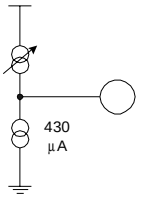
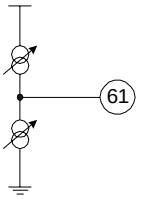
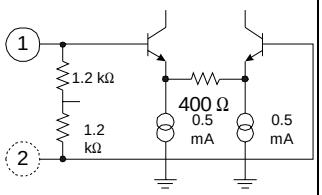
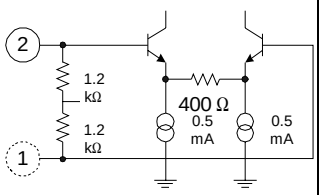
PIN TYPE	PIN NAME	PIN#	INFORMATION	
External Resistor Connections	RWC	17	Write Current reference resistor. An external resistor from this pin to VEE3 establishes range of programmable reference current (output on WREFC) used by preamp as a write current reference. 2.6kΩ <R_{WC}< 12kΩ, 4.7kΩ nominally.	
	RTR	35	Timing Recovery PLL reference resistor. An external resistor is connected from this pin to VEE4 (pin 33) to establish a precise internal reference current for the timing recovery VCO center frequency. 2kΩ <R_{TR}< 6kΩ, 5.6kΩ nominally.	
	RAF	62	AGC and CT Filter reference resistor. An external resistor is connected from this pin VEE1 (pin 4) to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency, AGC charge pump currents, and Dropout Detector decay current. 4kΩ <R_{AF}< 32kΩ,11kΩ nominally.	
	RFSR	63	Fast Recovery reference resistor. A resistor between this pin and VEE1 (pin 4) defines the duration of the fast recovery period. 10kΩ <R_{FSR}< 40kΩ, 20kΩ nominally. Also used as a differential analog test input in conjunction with RLZ (pin 64).	
	RLZ	64	Low Z duration control. A resistor between this pin and VEE1 (pin 4) defines the duration of the Low Z period. 10kΩ <R_{FSR}< 40kΩ, 20kΩ nominally.Also used as a differential analog test input in conjunction with RFSR (pin 63).	

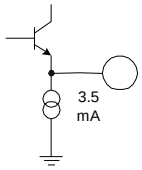
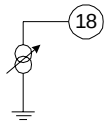
Table 208VM65015 Pin Functions and Descriptions

PIN TYPE	PIN NAME	PIN#	INFORMATION	
External Capacitor Connections	CTCD0	11	Track Cross Detector peak detect capacitor, Head 0. Nominally 0.68µF.	
	CTCD1	12	Track Cross Detector peak detect capacitor, Head 1. Nominally 0.68µF	
	CTRP CTRN	31 32	Timing Recovery PLL loop filter. Differential connections for the timing recovery PLL loop filter capacitor, nominally 4700pF.	
	CAGC	61	AGC Gain capacitor, nominally 820 pF to VEE1(pin 4).	
Analog Differential Inputs	DIP DIN	1 2	Analog Read Data input	 

MIXED SIGNAL CIRCUITS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Table 208VM65015 Pin Functions and Descriptions

PIN TYPE	PIN NAME	PIN#	INFORMATION	
Analog Outputs	TP1P TP1N	5 6	Differential analog test point 1 output	
	TP2P TP2N	7 8	Differential analog test point 2 output	
	WREFC	18	Programmable Write Reference Current used by preamp.	

AC and DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: 0°C < T_A < 70°C

Overall

Conditions unless otherwise specified: R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ, R_{TR}=2.5kΩ, BMXEN=0, WD R_L=500Ω

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	Powerdown Mode			500	µA
		Read Mode			190	mA
		Idle Mode,PREN=0 PREN=1			190 115	mA mA
		Write Mode,PREN=0 PREN=1			215 150	mA mA
V_{DD} Supply Current	I_{DD}				10	mA

CMOS Digital I/O (CLCK, DATA, XZ, ADPHLD, WG, RG, HDSEL, PD, SPCLK, SPEN, SPDATA, CT1, CT2)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	V_{IN} = V_{CC}, V_{IN} = V_{EE}			±10	µA
Output High Voltage	V_{OH}	I_{OH}=4mA, (SPDATA,CT1,CT2)	2.7			V
		I_{OH}=4mA, (CLCK,DATA,XZ)	V_{DD}-1.0V			
Output Low Voltage	V_{OL}	I_{OL}=4mA			0.5	V
Output Leakage Current	I_{OZ}	Output Disabled, V_{OUT} =V_{EE}, 2.7V (SPDATA only)			± 10	µA
Input Capacitance	C_{IN}				10	pF
Output Capacitance	C_{OUT}				10	pF

TTL Inputs (WDI, FREF)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			20	µA
Input Low Current	I_{IL}	V_{IL} = 0.5V			-0.6	mA

ECL I/O (FDSP, FDSN, WDP, WDN, TP3P, TP3N, TP4P, TP4N)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common Mode Input Voltage	V_{CM}		V_{CC}-2.8V		V_{CC}	V
Differential Input Voltage	V_D		200			mV
Input Current	I_{IIN}	$V_{IH}=V_{CC}$			10	µA
Output High Voltage	V_{OH}	R_L=50Ω to V_{CC}-2V	V_{CC}-1.3	V_{CC}-1.08		V
Output Low Voltage	V_{OL}	R_L=50Ω to V_{CC}-2.5V		V_{CC}–1.58	V_{CC}–1.3	V
Differential Output Swing	V_{diff}	$I_{OL}=I_{OH}\approx$18mA	0.485	0.500	0.515	V
Output Leakage Current	I_{OZ}	Output disabled, V_{OUT} = V_{EE}, V_{CC}			±200	nA

Gain Control

Conditions unless otherwise specified: C_{AGC}=820pF, $V_{CDO}=V_{CC}$, R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ,

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Dynamic Range	V_{DI}	V_{DI} = (V_{DIP} –V_{DIN})	30		300	mV_{ppd}
Input Common Mode Voltage	V_{CMDI}	V_{CMDI} = (V_{DIP} +V_{DIN})/2	V_{CC}–3.1	V_{CC}-2.7	V_{CC}–2.3	V
Differential Input Resistance	$R_{in(DA)}$	LOWZ = Low, WG='0'	1.2	2.5	3.8	kΩ
		LOWZ = High, WG='1'	120	250	380	Ω
Single-ended input Resistance	$R_{in(SA)}$	LOWZ = Low, WG='0'	0.6	1.25	1.9	kΩ
		LOWZ = High, WG='1'	60	125	190	Ω
VGA Minimum Gain	A_{vmin}	$A_V=(V_{VGAP}-V_{VGAN})/V_{DI}$ V_{CAGC}=0.8V, PGCEN=0			2.3	V/V
VGA Maximum Gain	A_{vmax}	$A_V=(V_{VGAP}-V_{VGAN})/V_{DI}$ V_{CAGC}=2.5V, PGCEN =0	39	40		V/V
VGA Gain in PGC mode	A_V	$A_V=(V_{VGAP}-V_{VGAN})/V_{DI}$, PGCEN=1 PGC= 0000 PGC= 0001 PGC= 0011 PGC= 0111 PGC= 1111		 2.24 5.0 10.6 21.8 44.5		V/V
Output Common Mode Voltage	V_{VCM}	V_{CM} = (V_{VGAP} +V_{VGAN})/2	V_{CC}–3.2	V_{CC}-2.5	V_{CC}–1.8	V
CAGC Common mode Voltage	V_{CM}		0.5	2.0	3.2	V
Output Offset Voltage	V_{OS}	$V_{OS}=(V_{VGAP}-V_{VGAN})$, over entire gain range, Test Mode 2	–50		50	mV
Output Distortion	THD	V_{DI} = 30-300mV_{ppd}, $V_{VGA}\leq 0.75V_{ppd}$, 1-20MHz 1st, 2nd, and 3rd harmonics only			1.0	%

AGC Loop

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{FSR}=20kΩ, R_{LZ}=20kΩ. For Charge Pump Current tests: LPFBYP='1',TFAQ='0', V_{CAGC}=1.2V, WG='0', RG='0'

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RAF Pin Voltage	V_{RAF}		1.16	1.2	1.24	V
RAF Current Range	I_{RAF}	$I_{RAF}=V_{RAF}/R_{AF}$	36	200	310	µA
RFSR Pin Voltage	V_{RFSR}		1.24	1.28	1.31	V
RFSR Current Range	I_{RFSR}	$I_{RFSR}=V_{RFSR}/R_{RFSR}$	30	64	130	µA
RLZ Pin Voltage	V_{RLZ}		1.24	1.28	1.31	V
RLZ Current Range	I_{RLZ}	$I_{RLZ}=V_{RLZ}/R_{LZ}$	30	64	130	µA
Fast Discharge Current, Continuous Mode	I_{QFD}	$V_{RLZ}=V_{CC}$-1.0V $V_{FSR}=V_{CC}$-0.6V $I_{QFD}=120\cdot I_{QNC}$	$0.8\cdot I_{QFD}$	I_{QFD}	$1.2\cdot I_{QFD}$	mA
	I_{QFD}/I_{QNC}		96	120	144	
Normal Discharge Current, Continuous Mode	I_{QND}	$V_{RLZ}=V_{CC}$-0.88V $V_{FSR}=V_{CC}$-0.6V $I_{QND}=5\cdot I_{QNC}$	$0.8\cdot I_{QND}$	I_{QND}	$1.2\cdot I_{QND}$	µA
	I_{QND}/I_{QNC}		12	15	18	
Normal Charge Current, Continuous Mode	I_{QNC}	$V_{RLZ}=V_{CC}$-0.8V $V_{FSR}=V_{CC}$-0.6V $I_{QNC}=I_{RAF}/17$	$0.8\cdot I_{QNC}$	I_{QNC}	$1.2\cdot I_{QNC}$	µA
Ultra Fast Charge Current, Continuous Mode	I_{QUFC}	$V_{RLZ}=V_{CC}$-0.6V $V_{FSR}=V_{CC}$-0.6V, Set TFAQ to '0', pause and set TFAQ='1' $I_{QUFC}=134\cdot I_{QNC}$	$0.8\cdot I_{QUFC}$	I_{QUFC}	$1.2\cdot I_{QUFC}$	mA
	I_{QUFC}/I_{QNC}					
Fast Charge Current, Continuous Mode	I_{QFC}	With device in ultra fast charge condition, set $V_{RLZ}=V_{CC}$-1.0V, $V_{FSR}=V_{CC}$-0.6V, pause and set $V_{RLZ}=V_{CC}$-0.6V, $V_{FSR}=V_{CC}$-0.6V $I_{QFC}=9\cdot I_{QNC}$	$0.8\cdot I_{QFC}$	I_{QFC}	$1.2\cdot I_{QFC}$	µA
	I_{QFC}/I_{QNC}		7.2	9	10.8	
Low Gain Charge Pump Current, Sampled Mode	I_{QL}	$V_{RLZ}=V_{CC}$-0.465V $V_{FSR}=V_{CC}$-0.6V, RG='1', PDTST='1', DPLL='0', CLKSEL='1', K_{SQPI} = 0,1,2,3 $I_{QL}=I_{QNC}\cdot K_{SQPI}$ [1]	$0.8\cdot I_{QL}$	I_{QL}	$1.2\cdot I_{QL}$	µA
	I_{QL}/I_{QNC}			0 1 2 3		
High Gain Charge Pump Current, Sampled Mode	I_{QH}	same conditions as I_{QL}, DPLL='1', K_{SQPI} = 0,1,2, $I_{QH}=I_{QNC}\cdot(6+K_{SQPI})$ [1]	$0.8\cdot I_{QH}$	I_{QH}	$1.2\cdot I_{QH}$	µA
	I_{QH}/I_{QNC}			6 7 8 9		
Charge Pump Leakage current	I_{LK}	HLD='1'			±200	nA
Output dynamic range	V_{FA}	$V_{FA}=(V_{FAP}-V_{FAN})$ $30mV_{ppd} \le V_{DI} \le 300mV_{ppd}$ $1MHz < f_{in} < 10MHz$	0.45		0.55	V_{ppd}
LOWZ One-shot Pulse Width	T_{LZ}	HDSEL or WG transition $T_{LZ}=0.075\cdot R_{LZ}$	$0.8\cdot T_{LZ}$	T_{LZ}	$1.2\cdot T_{LZ}$	µs

MIXED SIGNAL CIRCUITS

AGC Loop

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{FSR}=20kΩ, R_{LZ}=20kΩ. For Charge Pump Current tests: LPFBYP='1',TFAQ='0', V_{CAGC}=1.2V, WG='0', RG='0'

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
FSR One-shot Pulse Width	T_{FSR}	HDSEL, WG, or TCD transition T_{FSR}=0.075·R_{LZ}	0.8·T_{FSR}	T_{FSR}	1.2·T_{FSR}	µs
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW=15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Gain settle from –30% V_{DI} step	T_{GSD}	V_{FN} ≥ 0.9·(final value) in normal acquisition mode		20	25	µs
Gain settle from +30% V_{DI} step	T_{GSA}	V_{FN} ≤ 1.1·(final value) in normal acquisition mode			1.5	µs
VGA Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = A_{Vmax}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = A_{Vmax}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
AGC Gain Sensitivity to CAGC voltage	AV_{PV}	(Typical range is 1.4V to 2.8V)		17.5		dB/V
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW=15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Gain settle from –30% V_{DI} step	T_{GSD}	V_{FN} ≥ 0.9·(final value) in normal acquisition mode		20	25	µs
Gain settle from +30% V_{DI} step	T_{GSA}	V_{FN} ≤ 1.1·(final value) in normal acquisition mode			1.5	µs
VGA Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = A_{Vmax}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = A_{Vmax}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
AGC Gain Sensitivity to CAGC voltage	AV_{PV}	(Typical range is 1.4V to 2.8V)		17.5		dB/V
Trailing edge of LOWZ to V_{FN} stable to 10%	T_{WR}	C_{AGC} =820pF			500	ns
LOWZ extension time	$\mathbf{T}_{LZE}$				500	ns

1. K_{SQPI} is the value of the sampled charge pump current control register word SQPI(1:0).

Track Cross Detector

Conditions unless otherwise specified: $C_{TCD0,1}$=0.68µF, R_{AF}=10kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ, 0.5V < V_{CAGC} < 3.2v

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TCD Decay Current	I_{TCD}	I_{TCD}= 0.065/R_{AF}(K_1+4K_2+16K_3)	0.9·I_{TCD}		1.1·I_{TCD}	µA
TCD Threshold	V_{TH}	V_{TH}=V_{PK}/(1+4/(1+2K_{TCDTH})) Measure V_{TH} when TCD switches from high to low. Force V_{PK} through CTCD0,1	0.95·V_{TH}		1.05·V_{TH}	V
	ΔV_{TH}	Decrease in V_{TH} when TCD switches from low to high (hysteresis)	55	70	85	mV
TCD Delay	T_{TCDEL}	Time from V_{CAGC} crossing the threshold to TCD switching in100X mode.	5			µs
Input referred noise voltage	V_{IRN}	gain =A_{Vmax}, BW=15MHz V_{DIP} = V_{DIN}			10	nV/$\sqrt{Hz}$
Power supply rejection ratio	$PSRR_G$	gain = A_{Vmax}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB

MIXED SIGNAL CIRCUITS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Continuous Time Low-Pass Filter/Equalizer

Conditions unless otherwise specified: C_{AGC}=820pF, V_{CDO}=V_{CC}, R_{AF}=6kΩ, R_{SFR}=20kΩ, R_{LZ}=20kΩ

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Dynamic Range	V_{VGA}	V_{FN}<600mV_{ppd}	0.1	0.7	1.0	V_{ppd}
Filter cutoff frequency	f_C	f_C=(0.15·K_{FC}+5.0)·I_{RAF}	0.9·f_C	f_C	1.1·f_C	MHz
Normal lowpass gain (V_{FN} vs. V_{FI})	A_{ON}	BST=0, K_{FC}=0, f_{in} = 0.1f_C	-5.0	-3.2	-2.2	dB
Filter Boost (low end)	AB_{min}	BST=0		0	0.5	dB
Filter Boost (mid point)	AB_{mid1}	BST=8		0	0.5	dB
Filter Boost (mid point)	AB_{mid2}	BST=20	5.5	6.5	7.5	dB
Filter Boost (high end)	AB_{max}	BST=31	12.0	13.0	14.0	dB
Filter Output Offset	V_{OSFN}	V_{FI} = 0.0V, FNP/N outputs	–200		200	mV
AC coupled filter output offset	V_{OSFA}	V_{FI} = 0.0v, FAP/N outputs	–10		10	mV
Group Delay	T_{GD}	K_{FC}=63, GD=0	27	32	37	ns
Group Delay Variation	T_{GD}	0.1 $f_C \le f_{in} \le$ 1.5 f_C, 5MHz $\le f_C \le$ 15MHz, BST=0, GD=0	–2.0		2.0	%
	T_{GD2}	0.1 $f_C \le f_{in} \le$ 1.5 f_C, 5MHz $\le f_C \le$ 15MHz, BST=31, GD=0	–2.5		2.5	%
Group delay variation nonsymmetric zeros	T_{GD3}	DC @ FNP/N outputs. GD=-32, relative to GD=0	–32		-28	%
	T_{GD4}	DC @ FNP/N outputs. GD=+31, relative to GD=0	28		32	%
Normal output noise voltage	V_{NN}	BW = 100MHz, f_C = 10MHz [1] V_{DIP} = V_{DIN}			TBD	mV_{rms}
Power supply rejection ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp}	40			dB
Total harmonic distortion (V_{FN} vs. V_{FI})	THD_F	f_{in} = 0.67f_C, K_{FC}=63, $V_{FI} \le$ 0.7V_{ppd}, 2nd and 3rd harmonics only			1.5	%
Filter settle from step in Fc and BOOST	T_{FS}	K_{FC} or BST step to V_{FN} settle		85	300	ns
Boost accuracy	BA		-1		+1	dB

1. K_{FC}=63, BST=31 (boost level of 13dB).

MIXED SIGNAL CIRCUITS

FIR Filter/Equalizer

Conditions unless otherwise specified: TC2=1, TC13=1, $K_{0,4}$ = 0, $K_{1,3}$=0, LPFBYP='1', CLKSEL='1'. Inputs on RLZ and RFSR. f_{TR} > 20MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Nom. Center Tap Gain [1]	A_{VC}	K_2=8	1.15	1.25	1.3	V/V
Center Tap Gain Variation [1]	DA_{VC}	K_2=8, Apply a 0.2V D.C. signal measure the gain for eight successive channel samples, compute min vs. max percentage	0	1.0	1.5	%
Nom. Center Tap Offset [1]	OFF_C	K_2=8		3	5	mV
Center Tap offset variation [1]	OFF_V	Same as OFF_C		5	10	mV
Tap Gain & Linearity [1]	TG	Average tap gain per step	17.5	19.5	21.5	V/V
	A_{V2}	K_2=31. TC2=0, Maximum voltage gain of center tap 2		1.7		V/V
	$A_{V0,4}$	$K_{0,4}$=15, $K_{4,0}$=0. Maximum voltage gain of taps 0 and 4		0.293		V/V
	$A_{V1,3}$	$K_{1,3}$=31, K_3,1=16. TC13=0,Maximum voltage gain of taps1 and 3		0.293		V/V
Differential non-linearity [1]	DNL			5		mV/V
Integral non-linearity [1]	INL			19.8		mV/V
TH Droop	DAV	Average droop 0.25 v diff [2]			30	V/µs
TH Jitter	THJ	K_2=8, $K_{0,1,3,4}$=0		TBD		ps
Center tap Large Signal Bandwidth	LSBW	K_2=8, K_1=K_3=16, 0.5V_{ppd} [3] swept over frequency range		TBD		MHz

1. These tests should be done at the highest device clock rate.
2. Set taps K_2=8 & K_1/K_3 = 16 & K_0/K_4 = 0
3. Set taps K_2=31, K_1/K_3=-32 & K_0/K_4=15

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FIR Adaptation Circuit

Conditions unless otherwise specified: R_{TR}=5.4kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Integration Slope	IS	ACTST = 3. Observe Int_τ. Set all tap weights to zero except tap 3, which is set to unity. Supply an external CLK and a 4T pattern as shown in the diagrams that follow. Adjust the phase of the CLK relative to the FIR IN signal to create integrate up, down and hold conditions as shown. Measure integrated signal peak relative to reset value and normalize to integration length (12 for INTL='00').				
	IS_{U00}	Integrate up, INTL='00		0.46		mV/ns
	IS_{U01}	Integrate up, INTL='01		0.37		mV/ns
	IS_{U10}	Integrate up, INTL='10		0.31		mV/ns
	IS_{U11}	Integrate up, INTL='11'		0.26		mV/ns
	IS_{D00}	Integrate down, INTL='00'		0.46		mV/ns
	IS_{D01}	Integrate down, INTL='01'		0.37		mV/ns
	IS_{D10}	Integrate down, INTL='10'		0.31		mV/ns
	IS_{D11}	Integrate down, INTL='11'		0.26		mV/ns
Integration length	INT_L	Use the conditions for the error integration slope up measurement. For each value of the integration length, measure the time for each cycle of the Int_ε output, and normalize to the CLK period. Subtract 12 cycles to determine the true integration length.				
	IL_{00}	INTL='00'		12		cycles
	IL_{01}	INTL='01'		15		cycles
	IL_{10}	INTL='10'		18		cycles
	IL_{11}	INTL='11'		21		cycles

FIR Adaptation Circuit

Conditions unless otherwise specified: R_{TR}=5.4kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Zone Threshold	DZ_{TH}	Use the conditions for the error integration slope up measurement. Set ACTST = 0. For each step in integration slope, perform an adaptation of Tap 3. Monitor EA and Int_ε test signals. Measure Int_ε voltage when EA goes high. Repeat for integrate down conditions.				
	DZU_{00}	Integrate up, DZ= ‘00’		88		mV
	DZU_{01}	Integrate up, DZ= ‘01’		134		mV
	DZU_{10}	Integrate up, DZ= ‘10’		185		mV
	DZU_{11}	Integrate up, DZ= ‘11’		231		mV
	DZD_{00}	Integrate down, DZ = ‘00’		88		mV
	DZD_{01}	Integrate down, DZ= ‘01’		134		mV
	DZD_{10}	Integrate down, DZ=’10’		185		mV
	DZD_{11}	Integrate down, DZ=‘11’		231		mV

Timing Recovery Loop

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RTR Pin Voltage	V_{RTR}		1.21	1.25	1.29	V
RTR Current Range	I_{RTR}		200	500	645	µA
VCO Reference Current	I_{REF}	$I_{REF}=I_{RTR}=V_{RTR}/R_{TR}$		I_{REF}		mA
VCO Frequency	f_{VCO}	$f_{VCO} = f_0 \cdot (1+k_V(I \cdot \Delta V_{TR} + P \cdot \Delta V_{PD}))$		f_{VCO}		MHz
VCO Center Frequency	f_0	$f_0 = k_I \cdot I_{REF} (1+(0.125/32) \cdot K_{FRQ})$ [1]	$0.9 \cdot f_0$	f_0	$1.1 \cdot f_0$	MHz
VCO Gain	k_V	Measured at TP4P/N, K_{DAMP}= 127 [2]	0.35	0.4	0.45	V^{-1}
Imult Gain	I		0.9	1.0	1.1	A/A
Pmult Gain (VCO Cntl/Tmg Err.)	P	P=1.0(127-K_{DAMP})/127, Idle/Acq. P=0.25(127-K_{DAMP})/127, Tracking, TRGAIN=0 P=0.5(127-K_{DAMP})/127,Tracking, TRGAIN=1, CTRP=CTRN	0.8·P	P	1.2·P	V/V
VCO Dynamic Range	$f_{dr(VCO)}$	2% R_{TR}	±5		±40	%
CTRP/N CM Voltage	V_{CM}		2.20	2.30	2.40	V
CTRP/N Leakage	I_{LCTR}	COAST='1'			±200	nA
TR Charge Pump Gain (I_{QP}/Timing Error)	I_{TRQP}	Idle/Acquisition Mode	345	460	575	µA/V
		Tracking Mode: HGSEL = 0	87	115	144	µA/V
		HGSEL = 0	345	460	575	µA/V
Timing Error Offset	$OFF\tau_E$	LPFBYP='1', PDTST='1', RFSR/RLZ inputs set to +180mV_{ppd}, -180mV_{ppd},and 0mV_{ppd}			±5	mV
Sliced Threshold Voltage	V_{TSL}	LPFBYP='1', PDTST='1', CLK-SEL='1', Vary differential voltage on RFSR/RLZ inputs, observe X_e and X_o	80	90	100	mV
Closed Loop Jitter	σ_F	VCO output, sample size=100,000		100		ps

1. k_I is 167.4 MHz/mA, K_{FRQ} is the value of the VCO center frequency DAC FRQN(4:0), [-16 to 15}, for TCDEN='0' or TCD='1', or FRQT(4:0), [-16 to 15}, for TCDEN='1' and TCD='0'
2. K_{DAMP} is the value of the Damping Ratio DAC DAMP(6:0), [0 to 127]

Viterbi Detector

Conditions unless otherwise specified: RG='1', LPFBYP='1', PDTST='1'.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Sliding Window Over-write Voltage	V_{OW}	On each interleave Input series of same-polarity full-height pulses on RLZ/RFSR. Increase height of final pulse by $V_{OW.}$ Observe DATA. Pulse prior to large pulse should get overwritten and DATA='0'. Test both polarities of signal with 1-10 (PML='0') and 1-21 (PML='1') intervening zeros between 1's of same polarity. Repeat for each interleave.	15			mV
CLCK to DATA Delay	T_{PD}	1.5V on Active edge of CCLK to 1.5V on either DATA edge. CLCKE=0: positive CLCK edge CLCKE=1: negative CLCK edge	2		9	ns
Excess Zero Count Delay	T_{EZC}	$X=(0.5+K_{EZC})T_{TR}$ where T_{TR} is the timing recovery clock period [1]	X+2	X	X+20	ns
6T Detector Delay	T_{6T}	$X=(10+6\cdot K_{STL})T_{TR}$ where T_{TR} is the timing recovery clock period[2]. measured from FIR output to SIXT test point.	X+2	X	X+20	ns
Viterbi Threshold	VIT_{TH}	$VIT_{TH}=0.047+0.376\cdot(K_{VIT}/127)$[3] Input series of full height pulses on RLZ/RFSF. Reduce height of 1 pulse, vary K_{VIT} while observing DATA. When runt pulse is lower than the threshold, DATA will drop to '0.' Repeat for both interleaves		VIT_{TH}		V
Viterbi Threshold Mini-mum	VIT_{MIN}	$K_{VIT}=0$	0.02	0.023	0.028	V
Viterbi Threshold Maxi-mum	VIT_{MAX}	$K_{VIT}=127$	0.200	0.211	0.222	V
Viterbi Threshold DAC differential nonlinearity	VIT_{DNL}	Worst case step size deviation from ideal			0.047	V
Viterbi Threshold DAC integral nonlinearity	VIT_{IN}	Slope of VIT_{TH} vs. VIT_{DAC}			1	lsb
PLLP 0-to-1 Transition to Path Memory Set released.					TBD	ns

1. K_{EZC} is the value of the excess zeros count control register word EZC(4:0)
2. K_{STL} is the value of the STL 6T length control register bit, 0 (4cycles) or1 (8 cycles)
3. K_{VIT} is the value of the Viterbi Threshold control register word VIT(6:0)

Write Circuitry

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RWC Pin Voltage	V_{RWC}		1.21	1.25	1.29	V
RWC Current Range	I_{RWC}	$I_{RWC}=V_{RWC}/R_{WC}$	100	266	500	µA

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Write Circuitry

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WREFC Voltage Range			2V		V_{CC}	V
Output Current	I_{WC}	$I_{WC}=I_{RWC}\cdot K_{WC}/4$ [1]	$0.95\cdot I_{WC}$	I_{WC}	$1.05\cdot I_{WC}$	
Write Current Reference DAC differential nonlinearity		V_{CC}=5V, T=25°C			1	lsb
Write Current reference DAC slope error			$0.95\cdot I_{WC}/4$	$I_{WC}/4$	$1.05\cdot I_{WC}/4$	µA
WDP/N Propagation Delay	T_{WDPD}	R_L=50Ω to V_{CC}-2V			5	ns
WDP/N Rise Times	T_{WDr}	R_L=50Ω to V_{CC}-2V			2	ns
WDP/N Fall Times	T_{WDf}	R_L=50Ω to V_{CC}-2V			2	ns

1. K_{WC} is the value of the Write Current DAC WC(4:0), [0 to 31]

VTC Inc.
Value The Customer™

VM65060
ANALOG PRML CHANNEL

990812 **PRELIMINARY** August 12, 1999

FEATURES

- Register programmable user data rates from 46 to 140 Mbps
- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently-variable real zeros
- Programmable seven-tap transversal filter for PR4 equalization
- Self-adapting option for FIR tap weights
- Programmable two-level write precompensation with 1.25% resolution
- Direct Write/Read feature for equalizer optimization
- Analog/sampled AGC
- Zero phase restart for fast acquisition
- Servo area detectors for burst demodulation
- Fast timing control during acquisition by bypassing FIR filter
- Register programmable power management (<5 mW Power Down mode)
- 4 or 8-bit wide parallel data interface to disk controller
- Serial interface port for access to internal program storage registers to load and verify
- Single power supply (5V ±10%)
- Small footprint 80-pin PQFP package

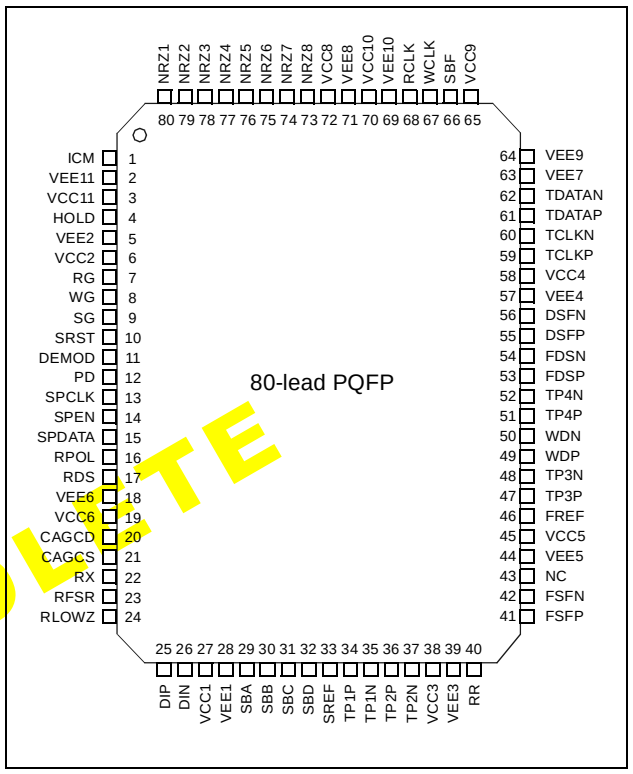
DESCRIPTION

The VM65060 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement a Partial Response Maximum Likelihood (PRML) read channel for zoned recording MR hard disk drive systems with user data rates from 46 to 140 Mbps.

BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 80-Lead PQFP package.

Functional blocks include AGC, programmable continuous time filter, adaptive FIR filter, maximum likelihood Viterbi detector, frequency synthesizer, 2-level nonlinear write precomp and area detectors for servo bursts. Programmable functions such as data rate, filter cutoff/boost, FIR tap weights, adaption parameters, write precomp values, etc. are controlled by writing to the serial port registers. No external component changes are required to change zones.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC} ..... -0.3V to +7V

Input Voltages
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Analog Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V

Storage Temperature T_{stg} ..... -65°C to 150°C
Junction Temperature T_J ..... 150°C
Thermal Impedance Characteristics, Θ_{JA}:
- 80-Lead PQFP ..... 39°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

BLOCK DIAGRAM DESCRIPTION

Automatic Gain Control

- Dual mode AGC, analog during acquisition, sampled during read data
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Internal Low Z for write mode.
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

Low Pass Filter/Equalizer

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 7 to 48 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable group delay of ±30%
  - Differentiator outputs match normal output phase
  - Minimized size and power

FIR Filter/Equalizer

- Seven tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- Independent and/or dependent self adaption of tap weights
- User programmable adaption parameters:
  - Integration time
  - Dead zone control
  - Tap starting points
  - Number of taps to adapt
  - Selection of which taps to independently adjust

Level Qualification

- Level pulse detector for servo and sync field reads
- Independent positive and negative thresholds for asymmetrical signals (e.g. from MR heads)
- Independent thresholds for servo

Maximum Likelihood Detector

- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length of five

Frequency Synthesizer

- Better than 1% frequency resolution
- Up to 200 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

Timing Recovery

- Single external capacitor required
- Register programmable to user data rate of 140 Mbps operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio which is constant over all data rates

Write Precompensation

- Independently-programmable write precompensation for three data patterns
- Step resolution of 1.25% up to 40%
- Precompensation tracks Frequency Synthesizer period
- Differential PECL write data output
- Precoding function suited for PR4 channel
- SERVO:
- Wide bandwidth, precision full-wave rectifier
- Separate, automatically-selected registers for servo f_c, boost, and group delay
- Individual area detectors for servo bursts A, B, C and D
- Programmable servo gain of ± 4 dB

Digital Backend

- 4-bit (nibble) and 8-bit (byte) wide Bidirectional NRZ interface
- Parallel-to-Serial and Serial-to-Parallel converters
- 8/9 (0, 4/4) Encoder and Decoder
- 8-bit wide data Scrambler and Descrambler, with Pseudo Random Number Generator
- SYNC Byte detector, programmable, dual byte (“or” type)
- Channel clock divider
- 4-bit or 8-bit Direct Test Write and Read

PIN FUNCTIONS AND DESCRIPTION

Pin functions are described on page 128.

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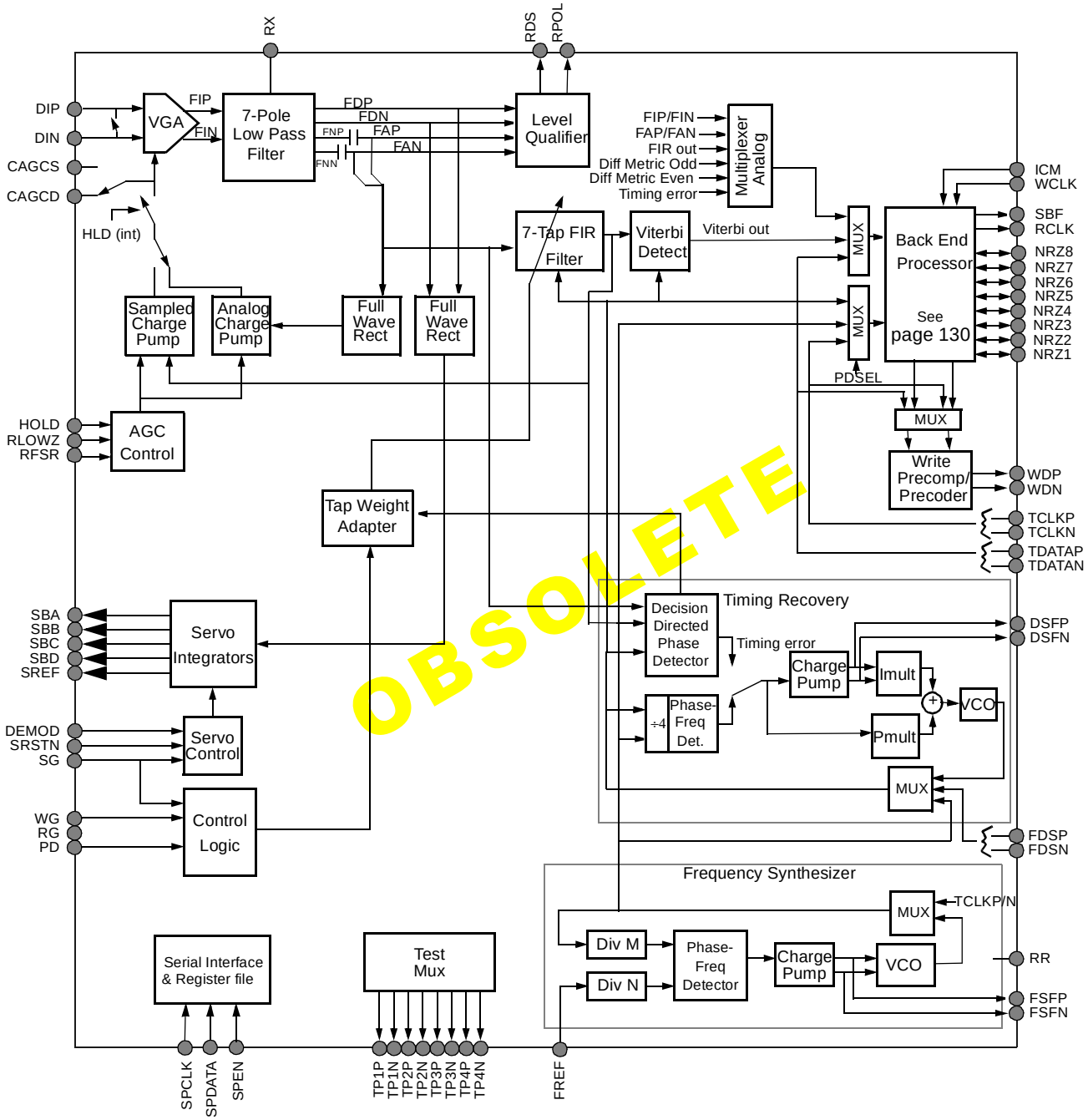
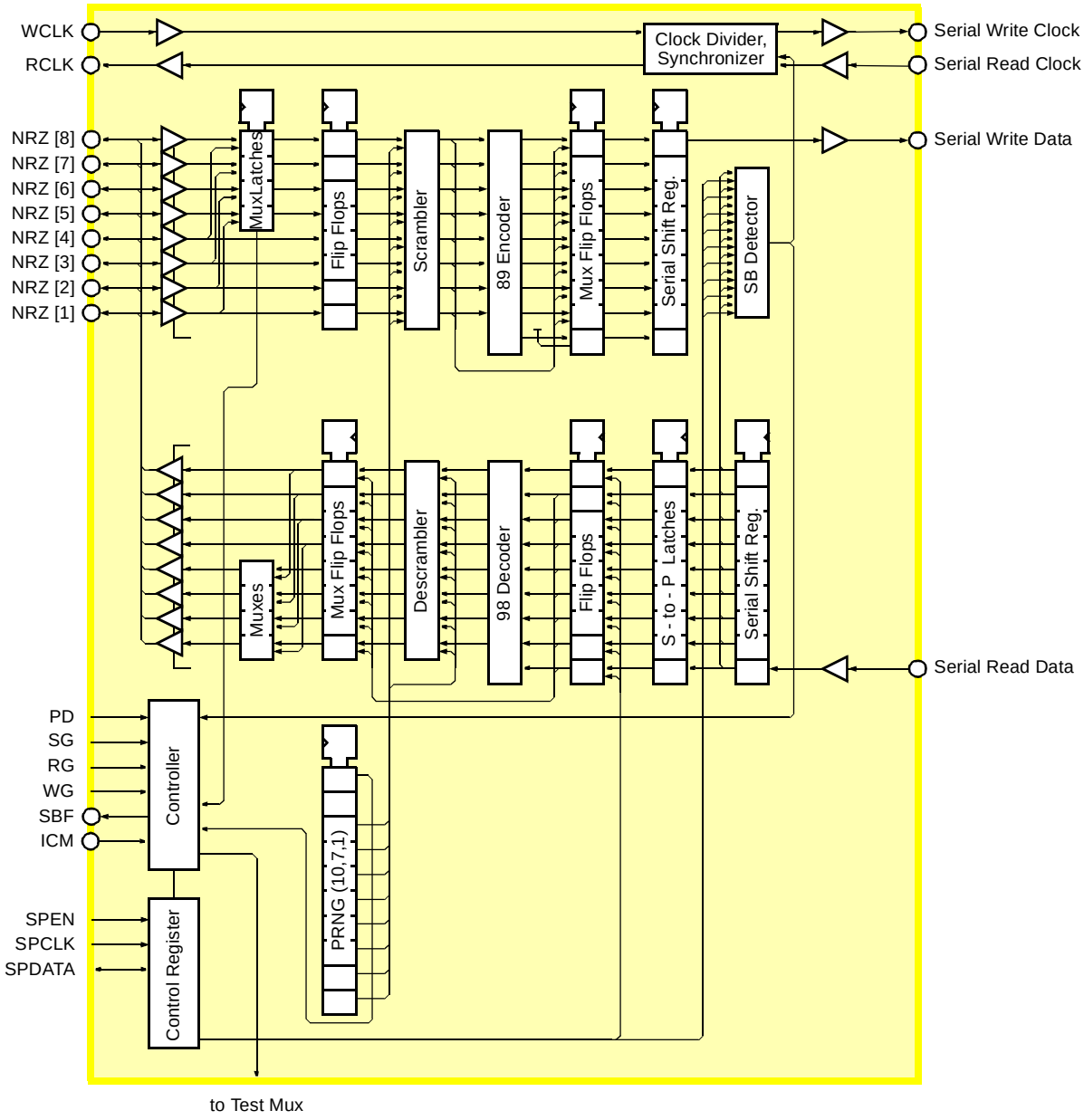
BLOCK DIAGRAM



MIXED SIGNAL CIRCUITS

DIGITAL BACK END TOP LEVEL SCHEMATIC/LOGIC BLOCKS



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BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTION

TheVM65060 implements a complete high performance PRML read channel. The VM65060 includes an AGC, programmable filter/equalizer, adaptive FIR filter, Viterbi detector, frequency synthesizer, decision-directed timing recovery, write precompensation and area detect servo, and supports user data rates up to 140 Mbps. A serial port is provided to read and write control data to the 16 internal programmable storage registers.

Gain Control (GC)

The Gain Control section of the VM65060 consists of a wide-band variable gain amplifier (VGA) and a programmable continuous time filter, with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC). The mode is selected with the PGCEN register bit.

Servo reads employ a fully differential analog AGC loop, while data reads employ both the analog loop (for fast acquisition) and a sampled/decision-directed loop (for fine tuning of the gain). The programmable gain control (PGC) circuit controls the VGA gain with an internal DAC. In PGC mode, the AGC loop is disabled and the VGA gain is a linear function of the DAC count.

The read signal is externally AC-coupled into the VGA amplifier on the DIP/DIN pins. The gain of the VGA is controlled by the voltage stored on the CAGCD hold capacitor for data reads (SG=0) and CAGCS for servo reads (SG=1). Two external holding capacitors allow for data and servo fields to have independent charge and discharge rates to avoid long reacquisitions of the gain at the beginning of the servo and data fields. The read signal is amplified and equalized by a low pass filter. The AGC loop locks the differential peak-to-peak voltage at FAP/FAN to $V_{FA} = 0.5V_{ppd}$ for inputs ranging from 20 to 200 mV_{ppd}. Test modes are provided in which the normal and differentiated filter outputs (FNP/FNN, FDP/FDN), the VGA inputs and outputs (DIP/DIN, DOP/DON), and the pulse detector inputs (FAP/FAN) are multiplexed to the TP2P/TP2N output pins respectively.

The analog AGC loop consists of the VGA amplifier, programmable continuous time filter, amplitude detector, exponentiator, and dual rate charge pump for fast transient recovery. Charge currents (decay) increase the capacitor voltage, V_{cagcx}, and increase the VGA gain while discharge currents (attack) lower the capacitor voltage, V_{cagcx}, and reduce the VGA gain.

When switching between data and servo modes, the VGA gain is momentarily squelched and the input impedance is reduced by a factor of 10 (to allow quick recovery from transient offsets), then a fast recovery mode is initiated. External resistor R_{LOWS} sets the amount of time the low Z state is on.

During ultra fast recovery, the VGA gain is increased to 155 times its normal rate until the signal exceeds its target value. The loop then enters a “fast” mode. This high bandwidth mode continues until the fast acquisition window T_{FAQ} times-out, whereupon normal charge pump currents are reinstated and loop bandwidth is reduced to its normal value for servo mode. External resistor R_{FSQ} sets the fast acquisition window period, T_{FAQ}.

To optimize recovery for constant density recording, all charge pump currents track with the value loaded in the data rate register (DRR); current magnitude ranges from I_{QXX} at maximum DR to $I_{QXX}/2$ at minimum DR. The magnitude of the charge pump currents, I_{QXX}, are set by an external resistor connected between the RX pin and ground and are given by the following equations:

$$I_{QND} = \frac{2.16V}{RX} \text{ (DRR = 11111), RX = 6 k}\Omega \qquad \textit{(eq. 190)}$$

$$I_{QNC} = I_{QND}/18,\ I_{QFC} = I_{QND}/2..0,\ I_{QUFC} = 8.6I_{QND},\ I_{QFD} = 8I_{QND}$$

The RX = 6 kΩ has been optimized for user data rates of 70-140 Mbps and can be scaled appropriately for lower data rates. VTC recommends that the AGC loop response be altered by varying the CAGCx capacitors and not the RX resistor. Since servo data is written at a lower fixed frequency, the magnitudes of charge pump currents in servo mode are set equal to those that occur at the minimum data rate in read mode.

For data reads, the analog AGC loop is utilized to quickly lock onto the incoming sync field preamble. When RG is asserted, the FIR, Viterbi detector, and decision-directed AGC and timing recovery circuits are powered up (if the programmable power reduction feature is enabled). An internal, delayed RG signal (RGD) is then generated two byte times after external RG is asserted. The sync field count begins when RGD is asserted. Refer to Figure 167.

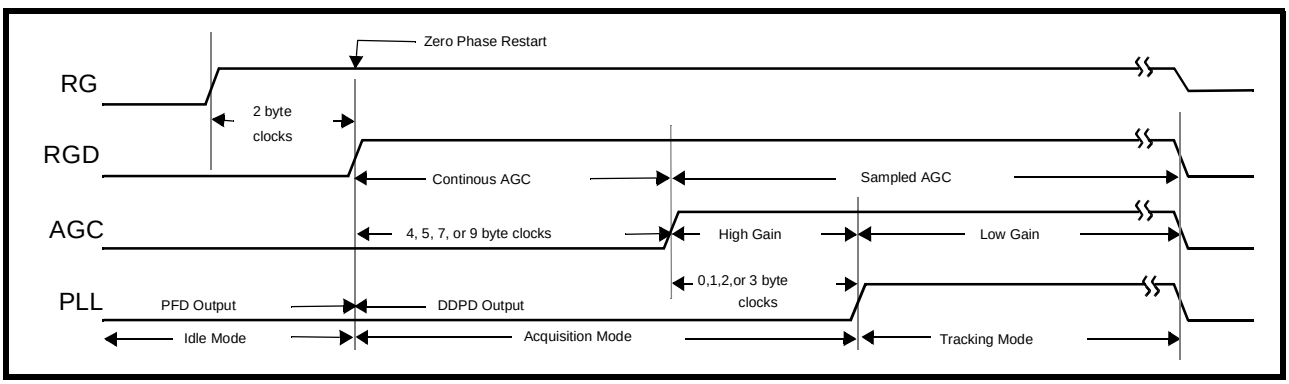


Figure 167 VCO Sync Field Timing Diagram

The AGC transition in high gain mode and the PLL transition into tracking mode are based on two programmable sync-field counters, the AGC SF counter and the PLL SF counter. The AGC transition from continuous to sampled high gain is determined by one of four programmable counts of 4, 5, 7, or 9 byte times (for this discussion, a 'byte time' equals 8 channel-bit times) which are derived from the frequency synthesizer clock; this is the AGC SF count.

Additionally, the PLL acquisition time can be extended by one of four progammable counts of 0, 1, 2 or 3 byte times following the AGC SF count; this is the PLL SF count. The sampled AGC remains in the high gain mode for the sum of both counts, then transitions into low gain. The PLL transitions from idle to acquisition mode when RGD is asserted. The PLL remains in acquisition mode through the sum of both the AGC SF and PLL SF counts, whereupon, it transitions into the tracking mode.

The sampled AGC loop consists of the VGA, the programmable continuous time filter, the sampling 7-tap FIR equalizer, the decision amplitude detector and charge pump. Symmetrical charge and discharge currents are utilized in the sampled mode. To optimize recovery for constant density recording, the charge pump currents in the sampled mode track with the value loaded in the data rate register (DRR); current magnitude ranges from I_Q at maximum data rate (DR) to $I_Q/2$ at minimum DR. The magnitude of the charge pump currents, I_Q, can be programmed from the sample loop control register to 0, 40, 80, or 120 µA for DRR = 11111. The high gain current modes are equal to the low gain current modes.

The VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. When in the PGC mode, the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the PGC control register. The VGA has a linear gain versus DAC count and is expressed by the following equation:

$$A_V = 2.8(N) + 2.4 \qquad \textit{(eq. 191)}$$

where N ranges between 0 and 15 decimal or 0000 to 1111 binary

Pulse Detector

The pulse detector (PD), converts analog read data into a digital pulse stream, utilizing amplitude discrimination. The timing between peaks is provided on the rising edges of the RDS output. The timing channel inputs, FDP/FDN, are direct-coupled from the differentiated output of the filter. The level channel inputs FAP/FAN are AC-coupled from the normal outputs of the filter.

The timing channel inputs (FD = FDP/FDN) are derived from the differentiated output of the low pass filter. A zero-cross comparator at FD detects the peaks of the waveform to preserve the timing of the read pattern. A bi-directional one shot circuit with nominal pulse width of 4ns clocks the D-type Flip-Flop on either positive or negative transitions of the FD input. Visibility into the timing channel signal HCLK is provided in TEST MODES on page 168.

The HCLK pulses are qualified by signals which are derived from the low pass filter output. Two comparators indicate when the positive (LP) and negative (LN) extents of the signal V_{FA} = V_{FAP}-V_{FAN} exceed either the positive threshold (V_{THP}) or the negative threshold (V_{THN}) level. Independent control of positive and negative thresholds is provided with 5-bit DACs ranging from 20-80% of V_{FA}. Vthx=20+1.9×VALUE in percent, where VALUE ranges from 0 to 31. Once the signal exceeds the level threshold, a high level is presented to the D-input of the Flip-Flop. When the peak is reached, the timing channel clocks a '1' into the Flip-Flop and triggers a one-shot producing the RDS output. The Flip-Flop resets on the rising edge of RDS and is ready for the next bit after the one-shot times out. A nominal pulse width of 24 ns is provided at the RDS output. Consecutive same-polarity pulses are also qualified. RDS polarity information is provided with the RPOL output.

Programmable Low Pass Filter (LPF) / Equalizer

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differentiated outputs. The cutoff frequency, boost, and DC group delay equalization are programmable.

The filter supplies normal and differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the level qualifier block to provide data and servo peak position information. The relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter.

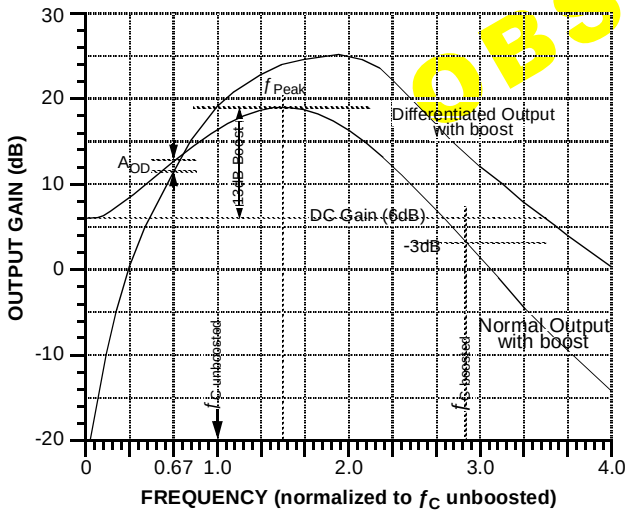
Cutoff frequency is controlled by the continuous time filter f_C DAC. The control word for the DAC is read from the CTF Data f_C register when SG=0; otherwise its read from the CTF Servo f_C register (see Table 218 Serial Register Bit Descriptions). Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation:

$$_C = (0.343 \times N) + 4.5 \qquad \textit{(eq. 192)}$$

where N ranges between 0 and 127 decimal

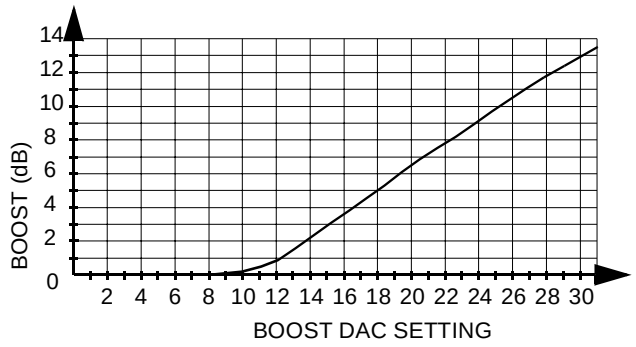
The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function.

Graph 11 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs.



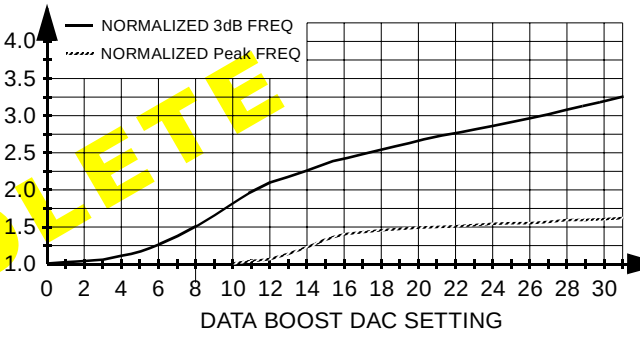
Graph 11 Normal and Differentiated Output Gains

Graph 12 shows the nominal relationship between the BOOST control word and the resulting boost level.



Graph 12 Ideal Boost (in dB) versus BOOST DAC VALUE

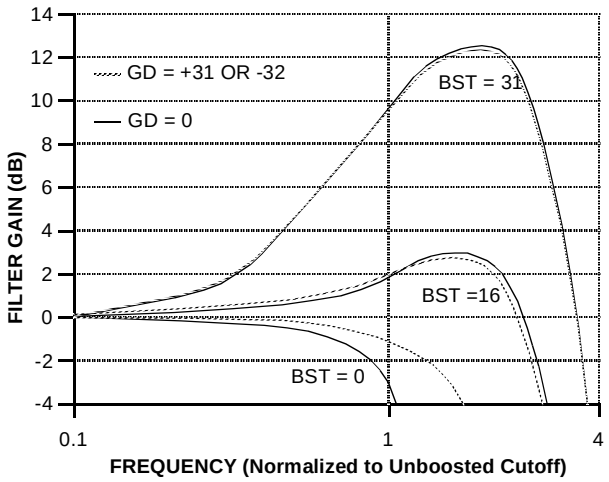
Graph 13 shows the effect of boost on the cutoff frequency.



Graph 13 Normalized f_c and f_{peak} versus DATA BOOST DAC VALUE

Setting the desired boost through the boost register (with the group delay register set to zero) produces symmetric zeros on the real axis. This maintains the constant group delay as in the no boost case. The group delay register can be used to produce asymmetry in the zeros causing the group delay to vary. This can be desirable to compensate for asymmetry in the heads/ media components. Group delay can be varied by ±30% from the symmetric zero (group delay register = 0) condition. The boost is held nearly constant as group delay is varied.

Graph 14 shows what happens to the magnitude response as the Group Delay register varies over extremes and under several boost conditions.



Graph 14 Gain Variations with Different Boost and Group Delay Settings

The group delay register is six bits wide in “two’s complement” format. A code of +31 corresponds to a DC shift in group delay of +30%; a code of -32 corresponds to -30% shift in DC group delay. Group delay is expressed as:

$$GD_{DC} = 0.95 \times GD_{DAC} \qquad \textit{(eq. 193)}$$

Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a “real” filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM65060 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 12 ns at a cutoff of 48 MHz. Thus at this cutoff frequency, the group delay varies by less than 0.18 ns out to 72 MHz.

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency in MHz.

$$GD = \left[3 + \frac{434}{f_C}\right] \text{ns} \qquad \textit{(eq. 194)}$$

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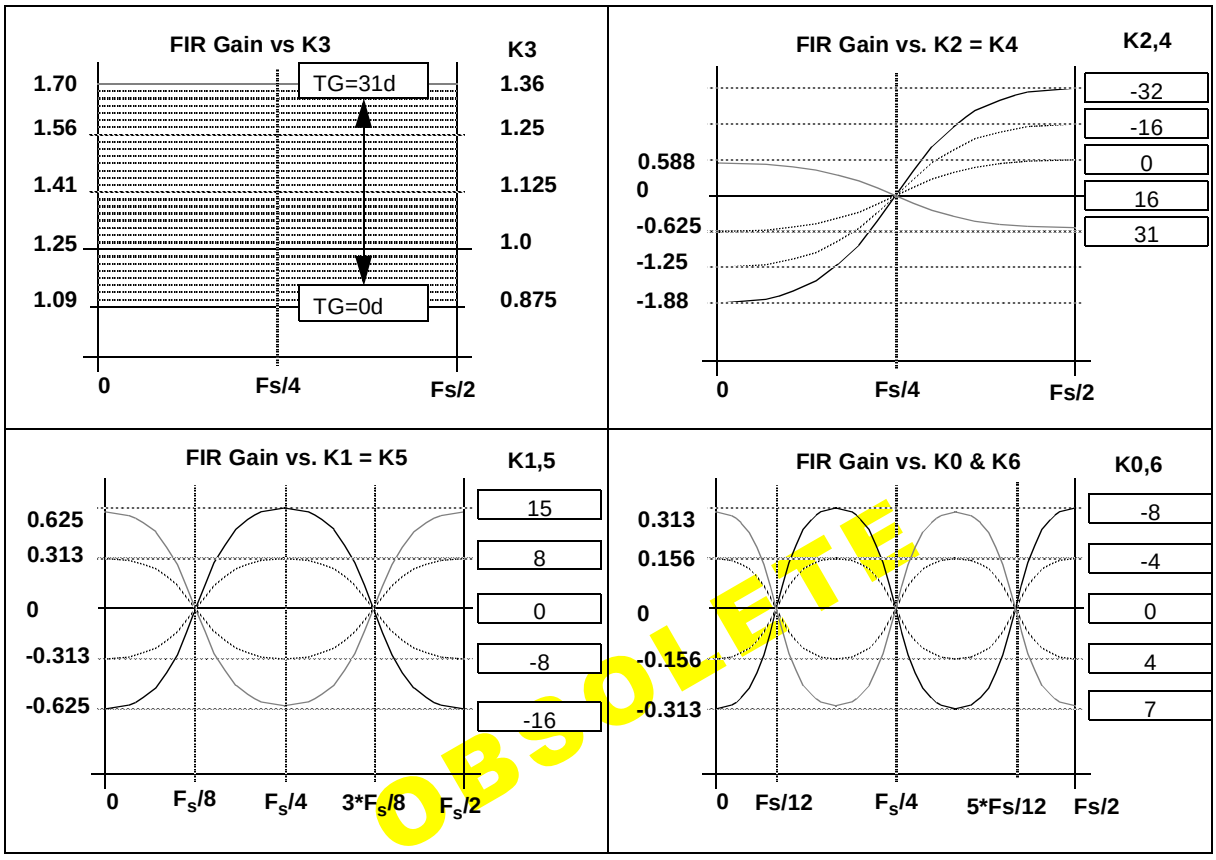
FIR Filter Equalizer

The FIR is a seven (7) tap transversal filter with independently-controllable tap weights. Independent control provides both gain and phase adjustment of the input signal. The following plot illustrates the possible gain variations achievable when symmetric taps are swept together over the allowable ranges, as listed in Table 209.



Graph 15 Symmetric Tap, frequency response curves

The H_0 term provides only a real valued response equal to the center tap gain. The gain response also includes finite bandwidth characteristics of the sampler. The sampler BW is about 250 MHz and will have some effect on the frequency characteristics. The ideal gain limits for the taps are shown below.

Table 209FIR Tap Gain settings

Tap	K_{-3}	K_{-2}	K_{-1}	K_0	K_1	K_2	K_3
Gain Range	-0.078 +0.068	–0.312 +0.293	–0.9375 +0.293	+1.09 +1.70	–0.9375 +0.293	-0.312 +0.293	-0.078 +0.068
Actual bits	4	5	6	5	6	5	4
Eff. bits	8	7	7	7	7	7	8
Resolution	9.78 mV/V	(1/64) X 1.25 = 19.56 mV/V					9.78 mV/V

FIR Adaptation Circuit

Normal Operation

The adaption process starts after RG has been asserted and the internal delayed read gate RGDP has become active. It should be noted that since the part is accessing the serial registers during adaption, the user should NOT attempt any serial register operation while RG is asserted and the AE bit is set.

Parameter Descriptions

- Adaptation Control Test “ACTST”
  These bits allow the basic verification of the Adaptation Control logic.
- Adaptation Enable “AE”
  This bit controls whether adaptation is to be performed. It cannot be modified during an adaptation read cycle.
- Dead Zone “DZ”
  This two-bit control specifies how many update samples are required in either direction to cause adaptation in that direction. The value sets the threshold in a symmetrical manner.
- Integration Length “INTL”
  This two-bit control selects the number of samples to average for each update cycle (12, 15, 18, or 21)
- Initial Tap Weight “ITW”
  This value selects which tap to adapt first.
- No Sync Byte “NOSB”
  This feature causes adaptation to occur at the point where the timing recovery circuit makes the transition from acquisition to tracking modes. This occurs during the VCO sync field even before the sync bytes.
  This option may be useful during initial drive optimization and data recovery modes.
- Tap Weight Range “TWR”
  This value sets the number of taps that are adjusted. If all six taps are to be adjusted this value should be set to “0”. By setting this value to “1” through “5” a reduced range of taps will be adjusted. The taps that are not adjusted are still active but are held at their preprogrammed values.
- Symmetry control “SYMC”
  This two-bit control selects which sets of taps should be controlled in a symmetrical manner.

Tap weights can be written and read by the controller. Thus the initial tap weight values can be preset near their optimal values and the final values can be read back after each adaption read cycle. The final taps weights remain as the initial tap weights for subsequent read cycles.

Proper selection of DZ and INTL can allow for rapid adaptation or for slow highly-stable tracking of system changes.

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Viterbei Detector

The Viterbi detector implements the maximum likelihood (ML) detector for PRML. The Viterbi detector block diagram is shown in Figure 168.

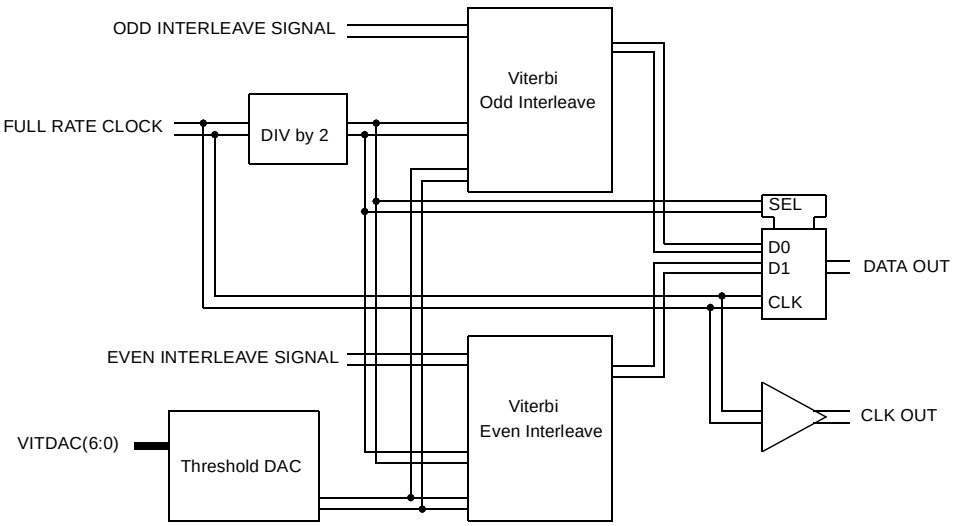


Figure 168 Viterbi Detector Block Diagram

Note that all signals are differential. The incoming signal (from the FIR filter via the timing recovery block) has been demultiplexed into the odd and even interleaves on a bit-by-bit basis. This is shown in the diagram as the odd interleave signal and the even interleave signal. Each interleave of the Viterbi detector runs at 1/2 the channel data rate. Note that the odd and even interleaves of the Viterbi detector are clocked on opposite phases of the full rate data clock. Each interleave independently processes its data stream. The data streams from the odd and even interleaves are then multiplexed back together on a bit-by-bit basis to yield the recovered bit stream.

The nominal Viterbi threshold window size is set by a 7-bit DAC which is controlled by the Viterbi DAC serial control register. Positive and negative thresholds in the Viterbi detector are modified based on the received data.

The dynamic thresholds in the Viterbi detector function to reject pulses of the same polarity as the most recent pulse, but of lesser amplitude. If a pulse of the same polarity as the most recent pulse exceeds the amplitude of the previous pulse, the 1 associated with the previous pulse (which is of lesser amplitude) is erased in the Viterbi detector's path memory. The path memory only has the ability to erase these smaller pulses if four or fewer zeroes have occurred between the two pulses of the same polarity. This requirement is satisfied by the (0,4,4) encoding that is used with this part.

The AGC circuit adjusts the signal amplitude to ±250 mV peak. Side sampling for PR4 produces a nominal sampled-signal amplitude of ±180 mV. This is a pseudo-ternary signal with the ±1 levels equal to ±180 mV and the zero level equal to 0 mV. Thus, the Viterbi threshold, VIT_{TH}, is nominally set to 180 mV. Since the data is pseudo-ternary, the nominal Viterbi threshold window size is $2 \bullet VIT_{TH}$.

$$VIT_{TH} = \left[0.047 + 0.376\left(\frac{VALUE}{127}\right)\right]mV \qquad \textit{(eq. 195)}$$

where VALUE is between 0 and 127, inclusive

Figure 169 shows a block diagram of a Viterbi detector interleave.

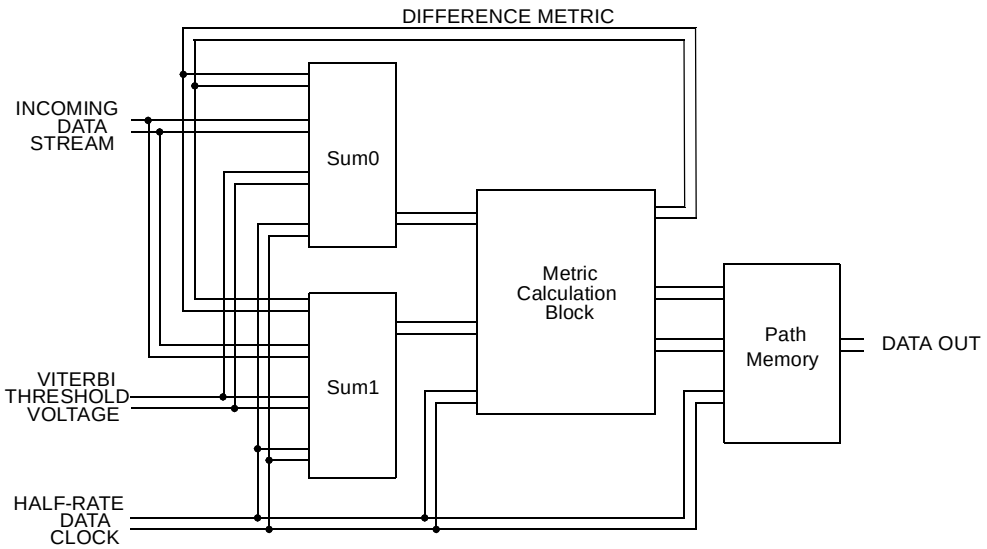


Figure 169 Viterbi Interleave Block Diagram

The summing blocks, Sum0 and Sum1, each form two signals that are fed to the metric calculation block. Opposite polarities of the incoming data stream and the difference metric are used by Sum0 and Sum1. The metric calculation block outputs the difference metric (which is fed back to the Sum0 and Sum1 blocks) and the two data streams that are used by the path memory block. One of these two data streams from the metric calculation block represents 1's that come from positive pulses in the ternary data signal. The other data stream represents 1's due to the negative pulses in the ternary data stream. Two 1's in one of the data streams without an intervening 1 in the other data stream results in the path memory erasing the first of these two consecutive 1's. A 0 results when neither of the two data streams is a 1. Decoding of the ternary signal is straightforward: a positive or negative pulse results in a 1; no pulse decodes to a 0. This decoding action can be thought of as undoing the precoding function.

Frequency Synthesizer

The Frequency Synthesizer (FS) is a PLL-based circuit that provides a programmable reference frequency for constant density recording applications. The frequency synthesizer output frequency can be programmed with a better than 1% accuracy via the M,N ("divide by") and DR (Data Rate) Registers. The synthesizer output frequency, F_{OUT}, should be programmed as close as possible to ((9/8)•User Data Rate). The synthesizer also supplies the timing reference for write precompensation so that the precompensation tracks the VCO period.

The frequency synthesizer requires an external passive loop filter to control its PLL locking characteristics. This filter is pseudo-differential and balanced in order to reduce the effects of common mode noise.

In Write and Idle modes, the programmable frequency synthesizer is used to provide a stable reference frequency to the timing recovery loop. In the Write and Idle modes, the frequency synthesizer output, when selected by the Control Test Mode Register, can be monitored at the TP3 test pin. In the Read mode, the FS output should not be selected for output on the test pins so that the possibility of jitter in the timing recovery PLL is minimized.

The synthesizer output frequency is programmed using the M and N registers of the frequency synthesizer via the serial port, and is related to the external reference clock input, FREF, as follows:

$$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right] \qquad \textit{(eq. 196)}$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center frequency.

The DR register value directly affects the following:

- Center frequency of the frequency synthesizer VCO
- Center frequency of the timing recovery VCO
- Phase detector gain of the frequency synthesizer phase detector
- Write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the GND and RR pins. The VCO center frequency, f_c, and the charge pump current, I_{QP}, are given by the equations below. RR is the resistance of the external resistor in Ohms, X is the decimal equivalent of the DR Register bits and K_{VCO} (rad/V•s) is the VCO gain.

$$f_C = \left(\frac{5292}{RR}\right) \times (42 + X) \quad \text{MHz} \qquad \textit{(eq. 197)}$$

$$K_{VCO} = 0.36 \times f_C \quad \text{MHz/V} \qquad \textit{(eq. 198)}$$

$$I_{QP} = \left(\frac{15,370}{RR}\right) \times (102.8 - X) \quad \mu\text{A} \qquad \textit{(eq. 199)}$$

Timing Recovery

The data synchronizer uses a fully integrated, fast acquisition, PLL to perform clock recovery from the incoming data stream.

Fast acquisition is obtained by locking the loop to the synthesizer during Write, Servo & Idle modes which minimizes the frequency transient that occurs when the Read mode is initiated. Thus the timing recovery PLL uses two separate phase detectors to drive the loop. A Decision-directed Phase Detector (DDPD) is used in the Read mode and phase-frequency detector (PFD) is used in the Write, Servo, and Idle modes.

The Read mode is initiated by performing a zero phase restart of the VCO, which will force a phase alignment to the incoming 2T (1/4 data-rate) clock pattern. The samples taken immediately after the restart will be used by the DDPD to "coarse adjust" the VCO. After the sync field count has reached the programmed count (AGC + PLL offset), as shown in Figure 167, the PLL will be switched to tracking mode which reduces the loop bandwidth (BW) by a factor of 3.16 or 4 depending on the register settings. In the tracking mode the input to the DDPD is taken from the output of the FIR filter.

Timing Recovery Operation

In Write or Idle mode, active when the RG (read gate) line is low, the mux selects the PFD as the input to the Q-pump and P-mult circuits. The two signal paths provide Proportional and Integral error terms to the VCO input. The benefit of this architecture is independent control of the loop parameters BW (bandwidth) and ζ (damping factor) via the control registers. The proportional term is controlled by the Damping Ratio DAC and the integral term is controlled by the Data Rate (DR) DAC. The VCO center frequency is set by the DR DAC; as the rate is increased the VCO gain must increase in order to maintain a constant locking range. The damping factor remains constant as the loop BW is changed. The net result of the loop is that it will settle in a constant number of clock cycles independent of the clock period.

The Read mode is initiated by a positive transition on the “RG” line as shown in Figure 170.

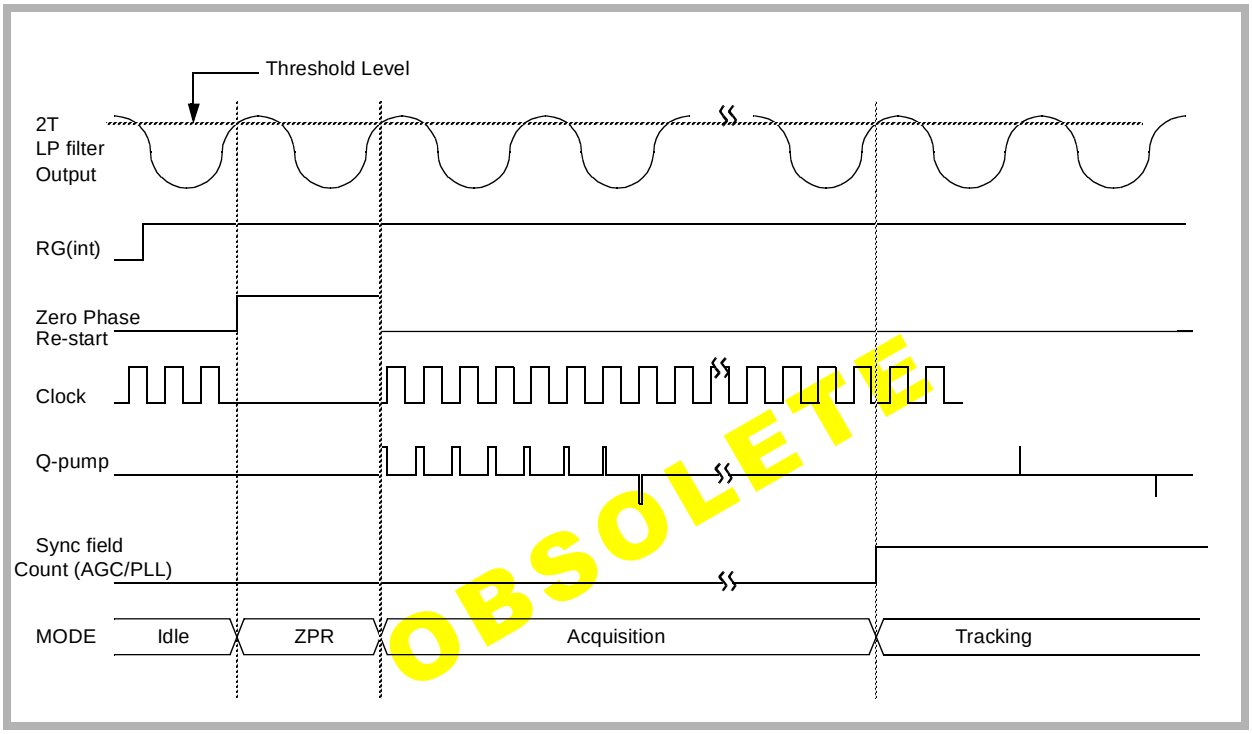


Figure 170 Timing Recovery Operation

The VCO is held in a low output state when the 2T input signal crosses the threshold set by the Zero Phase Restart DAC. The second time the threshold is crossed the VCO restarts. The threshold is set to align the VCO to the ideal PR4 sample phase of Π/4, which is 0.71 times the AGC’s analog servo voltage V_{TH}. The analog and digital delays in the samplers and the VCO require a slight variation of that sample threshold so a multiplying DAC is used to obtain the optimal set point. Once the VCO restarts, the DDPD output is used as the phase error to drive the PLL. The initial gain will be high to minimize the acquisition time and the computation of the phase error is done with a robust technique which prevents any false lock-up modes. After the sync field count has been reached the error detection mode will be changed to allow for three valid signal levels (only two are used in Acquisition) and the gains are reduced to reduce jitter. Since the AGC gain control is independent the timing control it can be switched at any point after the FIR has taken 7 samples (7-tap filter) and is switched slightly before the timing transition from Acquisition to Tracking. If the DSP mode is in progress this transition will enable the detection of the sync byte.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes six specific write data patterns of 4 channel bit lengths and can add delay in the transition of write data bits to counteract the magnetic non-linearity effect. The magnitude of the time shift is programmable via a Register and is made proportional to the frequency synthesizer's VCO period (i.e. data rate). Since the WPC operation is performed prior to the final T-FF (which is part of the precoding function) only three distinct patterns are decoded. Each of these three patterns may be independently programmed. The precoding operation is included with the WPC circuitry.

Each DAC allows write precompensation delay (Twpc) values to be programmed from 0 to 0.20T with 1.25% resolution as shown in the following equations.

$$Twpc(Pattern1, 3) = (0.013 \bullet Kwp + 0.20 \bullet WPCHR) \bullet T \quad \textit{(eq. 200)}$$

$$Twpc(Pattern2) = (0.013 \bullet Kwp) \bullet T \quad \textit{(eq. 201)}$$

where T is the period of the VCO, in nano-seconds, and Kwp is the value of the 4-bit DAC word for any of the three patterns

WPCHR is an independently-programmable bit which allows an addition 20% precompensation for patterns 1 and 3. By setting this bit high, patterns 1 and 3 will have a range from 20 to 40 percent of the VCO period. WPCHR does not affect pattern 2. If no compensation is desired for any of the three patterns, then that particular DAC word may be set to 0.

The precoder and all internal states in the WPC get reset with the de-assertion of write gate (WG) so that the write path is always in the same state upon assertion of WG. This also prevents any false data from being sent to the preamp during non-write modes.

Pattern	*Data Pattern*	*Write Data Pattern*
1	011	0010/1101
2	101	0110/1001
3	111	0101/1010

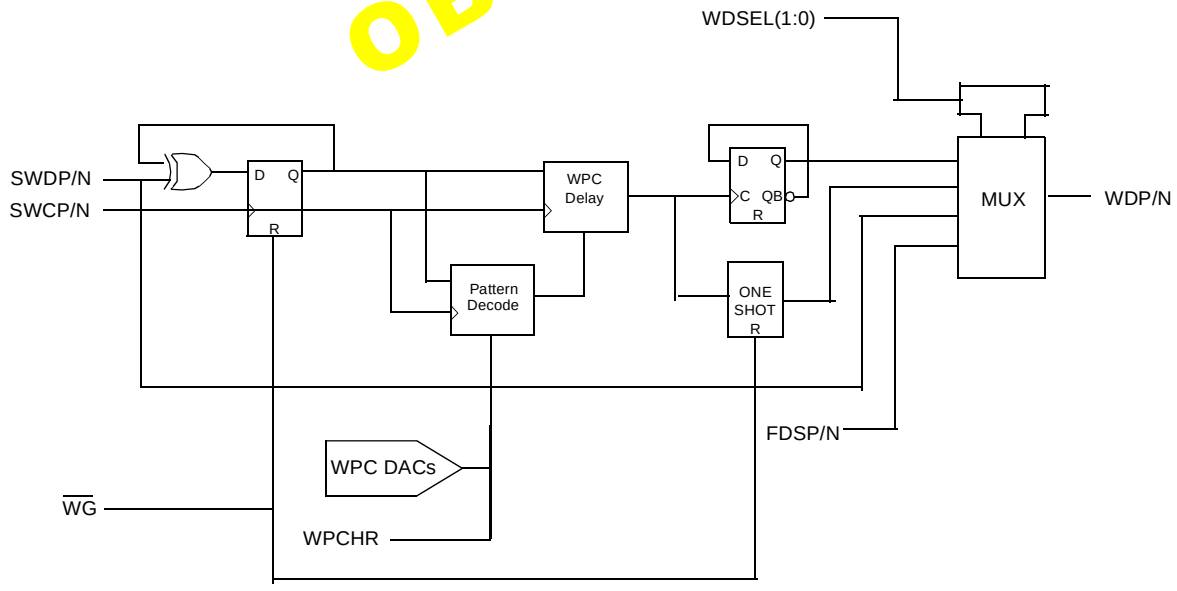


Figure 171 WPC/Precoder Block Diagram

Servo Demodulator

The embedded servo demodulator processor extracts the head position error information from the embedded servo bursts using an area detection technique. It supports full quadrature demodulation through the use of an array of four area detector channels. The area detection technique provides improved noise immunity over peak detection. A block diagram for the servo demodulator is shown in Figure 172.

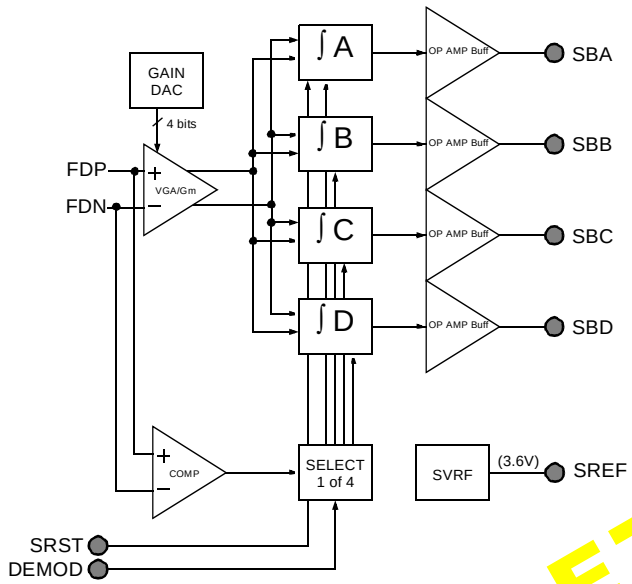


Figure 172 Servo Demodulator Block Diagram

The demodulator contains a variable gain amplifier, rectifier, four pulse area detectors and required timing logic. The differentiated filtered servo bursts are input to a variable gain amplifier (VGA). The VGA allows the demodulator block to accommodate a wide dynamic range of servo burst amplitudes and process variations of the internal integration capacitors and resistors. The gain range of the VGA is ±40% in steps of 5%, as defined in the servo gain control register. The amplified signal is full-wave rectified and input to an array of four area detectors. The area detector consists of a gm stage driving an on-chip integration capacitor. Note that the ±30% tolerance of the on-chip capacitors and gm block can be calibrated by adjusting the gain of the VGA.

Each area detector is selectively enabled when the DEMOD control input goes high and integrates the pulse voltage amplitude of the servo burst. After the burst pulses have been integrated, the DEMOD signal is brought low, the area detector is disabled and the final integrated voltage is held. Consecutive cycles of the DEMOD pin cause the A, B, C, and D area detectors to sample the input waveform. Upon the low level of SRST, the servo burst outputs are reset to the SREF voltage.

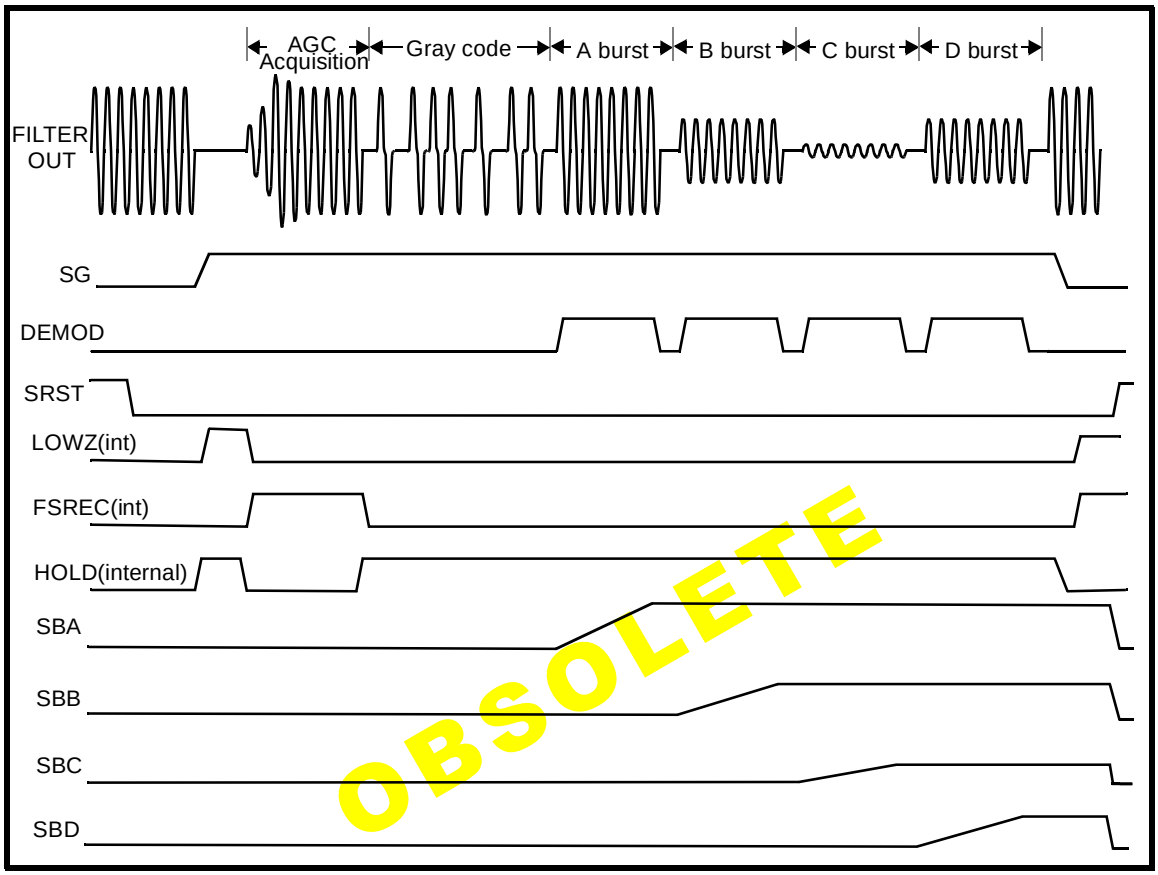


Figure 173 Servo Timing Diagram

Digital Back End

The VM65060's digital back end section consists of the following blocks: byte-wide (eight bit) parallel data interface, nibble-wide (four bit) parallel data interface, 8-bit wide scrambler/descrambler with PRNG, 8/9 (0, 4, 4) encoder/decoder, parallel/serial circuitry, sync byte circuitry, channel clock divider and mode control circuitry. These blocks are described below.

8-bit (Byte-Wide) Bidirectional NRZ Interface

The 8-bit NRZ interface is a set of eight bidirectional pins that provide the ability to interface with a byte-wide disk controller. Each pin has a TTL level input detector and a tristate TTL level output driver. The input detector is disabled during sleep mode. The output driver is put into high impedance when not driving the NRZ line. These pins, when not driving data out of the digital back end, must be driven by external sources (as all CMOS inputs).

In write mode, the NRZ data can be latched-in on the rising edge of WCLK or either edge of RCLK. The setting of two control register bits determines the configuration. The length of the VCO Sync Field is user-determined. Internal circuitry ignores the first two NRZ bytes, assuming them to be zero. This allows for a possible late driving of the NRZ bus with respect to the rising edge of WG. The end of the VCO Sync Field, and the start of the SYNC Byte section, is determined by the first non-zero byte strobed into the VM65060. NRZ[8] through NRZ[5] are used for non-zero detection. NRZ[4] through NRZ[1] are not monitored by the non-zero detector circuitry. Thus the MSB half of the first SYNC Byte *must* be non-zero, while the LSB half can be all zero.

In read mode, the NRZ data is driven out on the falling edge of RCLK. When RG goes high, the NRZ interface will drive low until either SYNC byte has been detected. The first non-zero data driven out on the NRZ pins will be either the first User Data word or else the SYNC Byte pattern. The user has the option to precede the User Data with the SYNC Byte pattern.

4-bit (Nibble-Wide) Bidirectional NRZ Interface

The operation of the 4-bit NRZ interface is similar to that of the 8-bit interface. The main difference being that only the pins NRZ[4] through NRZ[1] are used, with NRZ[8] through NRZ[5] being tied-off by the user. Eight-bit words are still used but they are broken into two 4-bit nibbles. The first nibble is the MSB half and the second nibble is the LSB half. Within the VM65060 the two 4-bit halves are concatenated into a full 8-bit word. During nibble operations the RCLK is run at twice the frequency as the internal byte clock, thus maintaining equivalent byte speed operation.

8-bit wide Scrambler / Descrambler, with PRNG

The Scrambler and Descrambler circuits, which are used to randomize user data, half-add each bit of an 8-bit Pseudo Random Number (PRN) to each bit of the 8-bit user data. The half-adding is done through the use of eight XNOR gates. The same PRN is half-added during write and again during read, resulting in the original user data being returned. The PRN comes from a shared Pseudo Random Number Generator (PRNG) which itself is based upon the $X^{10} + X^3 + 1$ polynomial.

At the beginning of write mode the PRNG is initialized to all 0's. The PRNG then generates a PRN of continuous 00_H until it is set with the FF_H seed. This continuous 00_H PRN in turn allows the scrambler to act as inverting buffers on the NRZ's VCO Sync Field during write mode. This causes the continuous 00_H being detected on the NRZ inputs to be inverted into continuous FF_H before entering the Encoder. At the end of the VCO Sync Field the PRNG is set to all 1's. This allows for a maximum run length PRN pattern as well as allowing the scrambler to act as a noninverting buffer on the NRZ's SYNC Bytes and Spacer byte. At the end of the three Sync Byte cycles, the PRNG is enabled into a free-running condition where PRN's are generated and half-added to the User Data until the end of the write mode.

At the beginning of read mode the PRNG is initialized to all 1's. Following the successful detection of a Sync Byte, the PRNG is enabled into a free-running condition where PRN's are generated and half-added to the User Data before being passing on to the NRZ output drivers until the end of the read mode.

During Idle, Sleep, or Direct Test modes the PRNG's clock is disabled to save power. During normal Write or Read modes the PRNG's clock is enabled. The user has the option to not scramble and descramble the User Data by not generating PRN's with the PRNG. When this option is chosen, the PRNG remains set at all 1's throughout the User Data fields, and the scrambler and descrambler circuitries simply buffer the User Data in both the write path and the read path.

8/9 (0, 4, 4) Encoder / Decoder

In order to provide for proper partial response maximum likelihood (PRML) signaling and detection in the recording channel, a run length limited (RLL) code of parameters (0, 4, 4) is being provided. As 8-bit data words are being provided for recording, the simplest (0, 4, 4) RLL code for 8-bit words is to use a set of qualified 9-bit code words. There are 279 qualified 9-bit code words, out of the possible 512 9-bit words. Only 256 of these are required to encode the 8-bit data word. This is known as an 8/9 code. The code word to data word assignments have been made to minimize both logic delay and chip area. Circuitry has been designed to provide for both encoding and decoding the 8-bit data words.

Table 210 and Table 211 show the relationships between the 8-bit data words (shown in hexadecimal notation) and the 9-bit code words (shown in octal notation) incorporated in the encoder circuitry. Unused or invalid codewords are not shown.

Table 2108-bit Data Word (hexadecimal) and 9-bit Code Word (octal)

DATA	CODE	DATA	CODE	DATA	CODE	DATA	CODE
00	356	40	756	80	456	C0	416
01	351	41	751	81	451	C1	411
02	357	42	222	82	457	C2	622
03	341	43	223	83	441	C3	623
04	354	44	754	84	454	C4	414
05	355	45	755	85	455	C5	415
06	344	46	226	86	444	C6	626
07	345	47	227	87	445	C7	627
08	353	48	753	88	453	C8	413
09	311	49	231	89	431	C9	631
0A	307	4A	232	8A	432	CA	632
0B	313	4B	233	8B	433	CB	633
0C	314	4C	234	8C	434	CC	634
0D	315	4D	235	8D	435	CD	635
0E	316	4E	236	8E	436	CE	636
0F	317	4F	237	8F	437	CF	637
10	656	50	706	90	446	D0	646
11	651	51	261	91	461	D1	661
12	657	52	262	92	462	D2	662
13	641	53	263	93	463	D3	663
14	654	54	264	94	464	D4	664
15	655	55	265	95	465	D5	665
16	644	56	266	96	466	D6	666
17	645	57	267	97	467	D7	667
18	653	58	703	98	443	D8	643
19	611	59	271	99	471	D9	671
1A	607	5A	272	9A	472	DA	672
1B	613	5B	273	9B	473	DB	673
1C	614	5C	274	9C	474	DC	674
1D	615	5D	275	9D	475	DD	675
1E	616	5E	276	9E	476	DE	676
1F	617	5F	277	9F	477	DF	677
20	156	60	116	A0	556	E0	516
21	151	61	111	A1	551	E1	511
22	157	62	322	A2	557	E2	722
23	141	63	323	A3	541	E3	723
24	154	64	114	A4	554	E4	514
25	155	65	115	A5	555	E5	515
26	144	66	326	A6	544	E6	726
27	145	67	327	A7	545	E7	727
28	153	68	113	A8	553	E8	513
29	131	69	331	A9	531	E9	731
2A	132	6A	332	AA	532	EA	732
2B	133	6B	333	AB	533	EB	733
2C	134	6C	334	AC	534	EC	734
2D	135	6D	335	AD	535	ED	735
2E	136	6E	336	AE	536	EE	736
2F	137	6F	337	AF	537	EF	737
30	146	70	346	B0	546	F0	746
31	161	71	361	B1	561	F1	761
32	162	72	362	B2	562	F2	762
33	163	73	363	B3	563	F3	763
34	164	74	364	B4	564	F4	764
35	165	75	365	B5	565	F5	765
36	166	76	366	B6	566	F6	766
37	167	77	367	B7	567	F7	767
38	143	78	343	B8	543	F8	743
39	171	79	371	B9	571	F9	771
3A	172	7A	372	BA	572	FA	772
3B	173	7B	373	BB	573	FB	773
3C	174	7C	374	BC	574	FC	774
3D	175	7D	375	BD	575	FD	775
3E	176	7E	376	BE	576	FE	776
3F	177	7F	377	BF	577	FF	777

Table 2119-bit Code Word (octal) and 8-bit Data Word (hexadecimal)

CODE	DATA	CODE	DATA	CODE	DATA	CODE	DATA
111	61	313	0B	461	91	633	CB
113	68	314	0C	462	92	634	CC
114	64	315	0D	463	93	635	CD
115	65	316	0E	464	94	636	CE
116	60	317	0F	465	95	637	CF
131	29	322	62	466	96	641	13
132	2A	323	63	467	97	643	D8
133	2B	326	66	471	99	644	16
134	2C	327	67	472	9A	645	17
135	2D	331	69	473	9B	646	D0
136	2E	332	6A	474	9C	651	11
137	2F	333	6B	475	9D	653	18
141	23	334	6C	476	9E	654	14
143	38	335	6D	477	9F	655	15
144	26	336	6E	511	E1	656	10
145	27	337	6F	513	E8	657	12
146	30	341	03	514	E4	661	D1
151	21	343	78	515	E5	662	D2
153	28	344	06	516	E0	663	D3
154	24	345	07	531	A9	664	D4
155	25	346	70	532	AA	665	D5
156	20	351	01	533	AB	666	D6
157	22	353	08	534	AC	667	D7
161	31	354	04	535	AD	671	D9
162	32	355	05	536	AE	672	DA
163	33	356	00	537	AF	673	DB
164	34	357	02	541	A3	674	DC
165	35	361	71	543	B8	675	DD
166	36	362	72	544	A6	676	DE
167	37	363	73	545	A7	677	DF
171	39	364	74	546	B0	703	58
172	3A	365	75	551	A1	706	50
173	3B	366	76	553	A8	722	E2
174	3C	367	77	554	A4	723	E3
175	3D	371	79	555	A5	726	E6
176	3E	372	7A	556	A0	727	E7
177	3F	373	7B	557	A2	731	E9
222	42	374	7C	561	B1	732	EA
223	43	375	7D	562	B2	733	EB
226	46	376	7E	563	B3	734	EC
227	47	377	7F	564	B4	735	ED
231	49	411	C1	565	B5	736	EE
232	4A	413	C8	566	B6	737	EF
233	4B	414	C4	567	B7	743	F8
234	4C	415	C5	571	B9	746	F0
235	4D	416	C0	572	BA	751	41
236	4E	431	89	573	BB	753	48
237	4F	432	8A	574	BC	754	44
261	51	433	8B	575	BD	755	45
262	52	434	8C	576	BE	756	40
263	53	435	8D	577	BF	761	F1
264	54	436	8E	607	1A	762	F2
265	55	437	8F	611	19	763	F3
266	56	441	83	613	1B	764	F4
267	57	443	98	614	1C	765	F5
271	59	444	86	615	1D	766	F6
272	5A	445	87	616	1E	767	F7
273	5B	446	90	617	1F	771	F9
274	5C	451	81	622	C2	772	FA
275	5D	453	88	623	C3	773	FB
276	5E	454	84	626	C6	774	FC
277	5F	455	85	627	C7	775	FD
307	08	456	80	631	C9	776	FE
311	09	457	82	632	CA	777	FF

279 of 512 9-bit words meet the (0, 4, 4) RLL requirement. Of these, only 256 are needed to encode the 256 8-bit data words. Therefore many breaks occur in the codeword sequence of Table 216.

The 256 codewords that are utilized (out of the 279 valid codewords) were chosen so as to be able to realize encoder and decoder logic circuitry in the simplest and fastest means possible. A maximum of five gate delays through the encoder and through the decoder have been realized.

Valid codewords do not allow for runs of more than four zeros in either the data sequence, or in either the even indexed or odd indexed interleaves. Codewords that have zero pairs at either end, in either the main sequence or in either of the interleaves are allowed. Therefore, codewords with zero triplets at either end of any sequence are invalid.

Invalid codeword configurations are identified below.

Table 212Invalid Codeword Configurations

$000\ XXX\ XXX_B$	$XX0\ 000\ 0XX_B$	$XXX\ XXX\ 000_B$
$0XX_O$	603_O	$XX0_O$
$0X0\ X0X\ XXX_B$		$XXX\ X0X\ 0X0_B$
$20X_O$ $24X_O$		$X02_O$ $X42_O$
$21X_O$ $25X_O$		$X12_O$ $X52_O$
$X0X\ 0X0\ XXX_B$		$XXX\ 0X0\ X0X_B$
$10X_O$ $42X_O$		$X01_O$ $X21_O$
$12X_O$ $50X_O$		$X04_O$ $X24_O$
$40X_O$ $52X_O$		$X05_O$ $X25_O$

Invalid cases are shown in Table 216. A total of 233 9-bit words are invalid.

Table 213Unused and Invalid 9-bit Word (octal) 8-bit Word (hexadecimal)

CODE : DATA	CODE : DATA	CODE : DATA	CODE : DATA
117 : 62	051 : 01	220 : 40	460 : 90
147 : 3A	052 : 08	221 : 41	470 : 98
303 : 08	053 : 08	224 : 44	500 : E2
306 : 00	054 : 04	225 : 45	501 : E3
347 : 7A	055 : 05	230 : 48	502 : E8
417 : C2	056 : 00	240 : 12	503 : E8
447 : 9A	057 : 02	241 : 13	504 : E6
517 : E2	060 : 10	242 : 58	505 : E7
547 : BA	061 : 11	243 : 58	506 : E0
606 : 10	062 : 12	244 : 16	507 : EA
647 : DA	063 : 13	245 : 17	510 : E0
707 : 5A	064 : 14	246 : 50	512 : E8
711 : 59	065 : 15	247 : 5A	520 : A0
713 : 5B	066 : 16	250 : 10	521 : A1
714 : 5C	067 : 17	251 : 11	522 : A2
715 : 5D	070 : 18	252 : 18	523 : A3
716 : 5E	071 : 19	253 : 18	524 : A4
717 : 5F	072 : 1A	254 : 14	525 : A5
741 : 43	073 : 1B	255 : 15	526 : A6
744 : 46	074 : 1C	256 : 10	527 : A7
745 : 47	075 : 1D	257 : 12	530 : A8
747 : FA	076 : 1E	260 : 50	540 : A2
757 : 42	077 : 1F	270 : 58	542 : B8
000 : 42	100 : 62	300 : 02	550 : A0
001 : 43	101 : 63	301 : 03	552 : A8
002 : 48	102 : 68	302 : 08	560 : B0
003 : 48	103 : 68	304 : 06	570 : B8
004 : 46	104 : 66	305 : 07	600 : 12
005 : 47	105 : 67	310 : 08	601 : 13
006 : 40	106 : 60	312 : 0A	602 : 18
007 : 4A	107 : 6A	320 : 60	603 : 18
010 : 40	110 : 60	321 : 61	604 : 16
011 : 41	112 : 68	324 : 64	605 : 17
012 : 48	120 : 20	325 : 65	610 : 18
013 : 48	121 : 21	330 : 68	612 : 1A
014 : 44	122 : 22	340 : 02	620 : C0
015 : 45	123 : 23	342 : 78	621 : C1
016 : 40	124 : 24	350 : 00	624 : C4
017 : 42	125 : 25	352 : 04	625 : C5
020 : 00	126 : 26	360 : 70	630 : C8
021 : 01	127 : 27	370 : 78	640 : 12
022 : 02	130 : 28	400 : C2	642 : D8
023 : 03	140 : 22	401 : C3	650 : 10
024 : 04	142 : 38	402 : C8	652 : 18
025 : 05	150 : 20	403 : C8	660 : D0
026 : 06	152 : 28	404 : C6	670 : D8
027 : 07	160 : 30	405 : C7	700 : 52
030 : 08	170 : 38	406 : C0	701 : 53
031 : 09	200 : 12	407 : CA	702 : 58
032 : 0A	201 : 13	410 : C0	704 : 56
033 : 0B	202 : 18	412 : C8	705 : 57
034 : 0C	203 : 18	420 : 80	710 : 58
035 : 0D	204 : 16	421 : 81	712 : 5A
036 : 0E	205 : 17	422 : 82	720 : E0
037 : 0F	206 : 10	423 : 83	721 : E1
040 : 02	207 : 1A	424 : 84	724 : E4
041 : 03	210 : 18	425 : 85	725 : E5
042 : 18	211 : 19	426 : 86	730 : E8
043 : 18	212 : 1A	427 : 87	740 : 42
044 : 06	213 : 1B	430 : 88	742 : F8
045 : 07	214 : 1C	440 : 82	750 : 40
046 : 10	215 : 1D	442 : 98	752 : 48
047 : 1A	216 : 1E	450 : 80	760 : F0
050 : 00	217 : 1F	452 : 88	770 : F8

Parallel-to-Serial and Serial-to-Parallel Converters

One of the main features of the digital back end is the conversion of 8-bit parallel NRZ data into a high speed serial bit stream, and the conversion of high speed serial data back to 8-bit parallel NRZ data. In write operations a 9-bit word is loaded in parallel onto the high speed serial write data bit stream every ninth channel clock cycle (every eighth in direct test) and then shifted out to the analog front end. And in read operations nine bits of the high speed read data bit stream are captured in parallel every ninth channel clock cycle (every eighth in direct test) and then passed toward the NRZ pins.

The coordination of these transfers is timing critical. In write operations, the transfer takes place as a parallel load of a serial shift register for a single channel clock cycle during the second half of the internal NRZ write clock period. This allows the parallel data plenty of time to have settled prior to its parallel loading into the serial shift register of the high speed write data bit stream.

In read operations, the transfer only takes place following a successful SYNC Byte word detection so that the RCLK will have been synchronized with the user data word boundaries. Once synchronization of the clock has been achieved, the user data is captured in 9-bit segments once every ninth cycle and made available to the decoder, descrambler, and NRZ output pins. In direct test the user data is captured in 8-bit segments once every eighth cycle and bypasses the decoder and descrambler on its way to the NRZ output pins.

SYNC Byte Detector, Programmable

Detection of a SYNC Byte word in read mode is used to set the framing of the user data field into user data words that can then be passed on to the disk controller. The VCO Sync field, which precedes the SYNC Byte words, is searched at the beginning of read mode by the SYNC Byte detector circuitry. It is looking for either of the two SYNC Byte words to come along in the serial data stream so that the proper data word framing, or boundaries, can be determined and set.

In normal operation, the SYNC Byte words are two 9-bit words separated by a 9-bit spacer word, while in direct test operation they are the combination of 8-bit SYNC Byte words and the last bit of the VCO Sync Field, ‘1’, for SB1 and the last bit of the 8-bit spacer word, ‘0’, for SB2. In order to detect the SYNC Byte words, the detector circuitry must be informed for which pattern to search. The 9-bit SYNC Byte pattern for which to search is stored in the control register. This pattern is for the second SYNC Byte word, SB2, while the pattern for SB1 is the bit by bit inverse of SB2.

The SYNC Byte detector circuitry consists of a bank of nine XNOR/XOR gates. Each gate interrogates a single bit of the serial bit stream, resulting in a string of nine bits being checked in parallel. Each bit is checked with respect to the corresponding bit stored in the control register. If all nine serial stream bits mismatch their corresponding stored pattern, XNOR’s $\Rightarrow$ 1, and SB1 is said to be found. If all nine bits are matched, XOR’s $\Rightarrow$ 0, and SB2 is said to be found.

Upon detecting either SB1 or SB2 in the serial bit stream, a synchronization signal is passed on to the channel clock divider circuitry so that the divided clock can be adjusted for framing the user data word boundaries. Also, a blocking signal is set that stops the detector circuitry from continuing to search for and detecting subsequent patterns that also match the SYNC Byte patterns. In addition, a SYNC Byte Flag is set and eventually driven out on the SBF pin.

If the SYNC Byte detector circuitry fails to detect either SYNC Byte pattern as it passes through in the serial data stream, possibly due to a corrupted bit stream, the search is allowed to continue until the end of the read mode during which a possible false detection of user data patterns as the SYNC Byte words might occur. Acknowledging the failure to detect the SYNC Byte during the proper portion of the Read Mode is left up to the Controller chip.

The user has the option of requiring patterns SB1 and SB2 to *both* be detected prior to the passing of user data words on to the disk controller. In this way the user can configure tighter error tolerances during the SYNC Byte zone by requiring that both SYNC Bytes must be error free, rather than just one.

As there is a relationship between SB1 and SB2, they must be coordinated when chosen and written. Two tables have been include here to aid in determining pairs of SYNC Bytes.

Table 214 lists the 110 possible SYNC Byte pairs that can be used in 8/9 encoded normal modes. These all have SB1 and SB2 that are the bit-by-bit inverses of each other. SB1’s that have NRZ[8:5]= 0 are excluded from this list as they would not be detected properly by the non-zero detector in the write path.

Table 214SYNC Byte Paris for 9/9 (0, 4, 4) Normal

SB1			SB2		
Hex	Oct	Binary	Binary	Oct	Hex
13	641	110100001	001011110	136	2E
16	644	110100100	001011011	133	2B
17	645	110100101	001011010	132	2A
19	611	110001001	001110110	166	36
1B	613	110001011	001110100	164	34
1C	614	110001100	001110011	163	33
1D	615	110001101	001110010	162	32
1E	616	110001110	001110001	161	31
21	151	001101001	110010110	626	C6
23	141	001100001	110011110	636	CE
24	154	001101100	110010011	623	C3
25	155	001101101	110010010	622	C2
26	144	001100100	110011011	633	CB
27	145	001100101	110011010	632	CA
29	131	001011001	110100110	646	D0
2A	132	001011010	110100101	645	17
2B	133	001011011	110100100	644	16
2C	134	001011100	110100011	643	D8
2E	136	001011110	110100001	641	13
30	146	001100110	110011001	631	C9
31	161	001110001	110001110	616	1E
32	162	001110010	110001101	615	1D
33	163	001110011	110001100	614	1C
34	164	001110100	110001011	613	1B
36	166	001110110	110001001	611	19
38	143	001100011	110011100	634	CC
42	222	010010010	101101101	555	A5
43	223	010010011	101101100	554	A4
46	226	010010110	101101001	551	A1
49	231	010011001	101100110	546	B0
4A	232	010011010	101100101	545	A7
4B	233	010011011	101100100	544	A6
4C	234	010011100	101100011	543	B8
4E	236	010011110	101100001	541	A3
51	261	010110001	101001110	516	E0
52	262	010110010	101001101	515	E5
53	263	010110011	101001100	514	E4
54	264	010110100	101001011	513	E8
56	266	010110110	101001001	511	E1
60	116	001001110	110110001	661	D1
61	111	001001001	110110110	666	D6
62	322	011010010	100101101	455	85
63	323	011010011	100101100	454	84
64	114	001001100	110110011	663	D3
65	115	001001101	110110010	662	D2
66	326	011010110	100101001	451	81
68	113	001001011	110110100	664	D4
69	331	011011001	100100110	446	90
6A	332	011011010	100100101	445	87
6B	333	011011011	100100100	444	86
6C	334	011011100	100100011	443	98
6E	336	011011110	100100001	441	83
70	346	011100110	100011001	431	89
71	361	011110001	100001110	416	C0
72	362	011110010	100001101	415	C5

SB1			SB2		
Hex	Oct	Binary	Binary	Oct	Hex
73	363	011110011	100001100	414	C4
74	364	011110100	100001011	413	C8
76	366	011110110	100001001	411	C1
78	343	011100011	100011100	434	8C
81	451	100101001	011010110	326	66
83	441	100100001	011011110	336	6E
84	454	100101100	011010011	323	63
85	455	100101101	011010010	322	62
86	444	100100100	011011011	333	6B
87	445	100100101	011011010	332	6A
89	431	100011001	011100110	346	70
8A	432	100011010	011100101	345	07
8B	433	100011011	011100100	344	06
8C	434	100011100	011100011	343	78
8E	436	100011110	011100001	341	03
90	446	100100110	011011001	331	69
91	461	100110001	011001110	316	0E
92	462	100110010	011001101	315	0D
93	463	100110011	011001100	314	0C
94	464	100110100	011001011	313	0B
96	466	100110110	011001001	311	09
98	443	100100011	011011100	334	6C
A1	551	101101001	010010110	226	46
A3	541	101100001	010011110	236	4E
A4	554	101101100	010010011	223	43
A5	555	101101101	010010010	222	42
A6	544	101100100	010011011	233	4B
A7	545	101100101	010011010	232	4A
B0	546	101100110	010011001	231	49
B8	543	101100011	010011100	234	4C
C0	416	100001110	011110001	361	71
C1	411	100001001	011110110	366	76
C2	622	110010010	001101101	155	25
C3	623	110010011	001101100	154	24
C4	414	100001100	011110011	363	73
C5	415	100001101	011110010	362	72
C6	626	110010110	001101001	151	21
C8	413	100001011	011110100	364	74
C9	631	110011001	001100110	146	30
CA	632	110011010	001100101	145	27
CB	633	110011011	001100100	144	26
CC	634	110011100	001100011	143	38
CE	636	110011110	001100001	141	23
D0	646	110100110	001011001	131	29
D1	661	110110001	001001110	116	60
D2	662	110110010	001001101	115	65
D3	663	110110011	001001100	114	64
D4	664	110110100	001001011	113	68
D6	666	110110110	001001001	111	61
D8	643	110100011	001011100	134	2C
E0	516	101001110	010110001	261	51
E1	511	101001001	010110110	266	56
E4	514	101001100	010110011	263	53
E5	515	101001101	010110010	262	52
E8	513	101001011	010110100	264	54

Table 215 shows the 239 possible SYNC Byte pairs that can be used in 8/8 nonencoded direct test modes.

Table 215SYNC Byte Paris for Direct Test (8-bit)

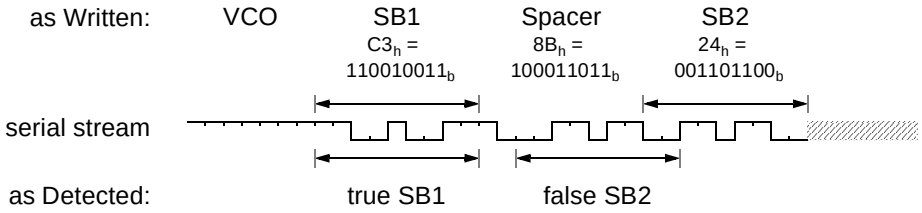
SB1		SB2	
Hex	Binary	Binary	Hex
~~00~~	~~(1)00000000~~	~~(0)11111111~~	~~FF~~
~~01~~	~~(1)00000001~~	~~(0)11111110~~	~~FE~~
~~02~~	~~(1)00000010~~	~~(0)11111101~~	~~FD~~
~~03~~	~~(1)00000011~~	~~(0)11111100~~	~~FC~~
~~04~~	~~(1)00000100~~	~~(0)11111011~~	~~FB~~
~~05~~	~~(1)00000101~~	~~(0)11111010~~	~~FA~~
~~06~~	~~(1)00000110~~	~~(0)11111001~~	~~F9~~
~~07~~	~~(1)00000111~~	~~(0)11111000~~	~~F8~~
~~08~~	~~(1)00001000~~	~~(0)11110111~~	~~F7~~
~~09~~	~~(1)00001001~~	~~(0)11110110~~	~~F6~~
~~0A~~	~~(1)00001010~~	~~(0)11110101~~	~~F5~~
~~0B~~	~~(1)00001011~~	~~(0)11110100~~	~~F4~~
~~0C~~	~~(1)00001100~~	~~(0)11110011~~	~~F3~~
~~0D~~	~~(1)00001101~~	~~(0)11110010~~	~~F2~~
~~0E~~	~~(1)00001110~~	~~(0)11110001~~	~~F1~~
~~0F~~	~~(1)00001111~~	~~(0)11110000~~	~~F0~~
10	(1)00010000	(0)11101111	EF
11	(1)00010001	(0)11101110	EE
12	(1)00010010	(0)11101101	ED
13	(1)00010011	(0)11101100	EC
14	(1)00010100	(0)11101011	EB
15	(1)00010101	(0)11101010	EA
16	(1)00010110	(0)11101001	E9
17	(1)00010111	(0)11101000	E8
18	(1)00011000	(0)11100111	E7
19	(1)00011001	(0)11100110	E6
1A	(1)00011010	(0)11100101	E5
1B	(1)00011011	(0)11100100	E4
1C	(1)00011100	(0)11100011	E3
1D	(1)00011101	(0)11100010	E2
1E	(1)00011110	(0)11100001	E1
1F	(1)00011111	(0)11100000	E0
20	(1)00100000	(0)11011111	DF
21	(1)00100001	(0)11011110	DE
⋮	⋮	⋮	⋮
EE	(1)11101110	(0)00010001	11
EF	(1)11101111	(0)00010000	10
F0	(1)11110000	(0)00001111	0F
F1	(1)11110001	(0)00001110	0E
F2	(1)11110010	(0)00001101	0D
F3	(1)11110011	(0)00001100	0C
F4	(1)11110100	(0)00001011	0B
F5	(1)11110101	(0)00001010	0A
F6	(1)11110110	(0)00001001	09
F7	(1)11110111	(0)00001000	08
F8	(1)11111000	(0)00000111	07
F9	(1)11111001	(0)00000110	06
FA	(1)11111010	(0)00000101	05
FB	(1)11111011	(0)00000100	04
FC	(1)11111100	(0)00000011	03
FD	(1)11111101	(0)00000010	02
FE	(1)11111110	(0)00000001	01
~~FF~~	~~(1)11111111~~	~~(0)00000000~~	~~00~~

These also have SB1 and SB2 that are the bit-by-bit inverses of each other; SB1's that have NRZ[8:5]= 0, along with the indiscernible case of all 1's and all 0's, have been crossed out in the table. The MSB 9th bits of both SB1 and SB2 are shown in parentheses to shown that for SB1 a '1' is added from the VCO Sync field, and for SB2 a '0' is added from the Spacer word. In both tables it is the 9-bit binary SB2 that must be stored in the control register.

It should be noted that the Spacer word plays a more important role than simply separating SB1 and SB2. Although it separates the two sync bytes so that a bit error late in SB1 does not also corrupt SB2 (resulting in failure to synchronize), it performs an additional function. The LSB of the Spacer word completes the SB2 pattern (which here must be a '0'), as seen in the non-encoded direct test case.

In addition, care must be taken in selecting a Spacer word that coordinates with the SB1 and SB2 patterns so as to not allow a false detection of SB2.

The following example illustrates how an unfortunate choice of SB1, Spacer, and SB2 words can lead to problems. SB2 was chosen to be 24_h, which means (per Table 214) that SB1 would then be $C3_h$. A Spacer word of $8B_h$ was also chosen. How these three words combine into a serial bit stream is shown below.



The problem with this combination of choices is that it results in the SB2 bit patterns showing up more than once in the bit stream. An additional, and false, SB2 is noted below the bit stream, due to the combination of the Spacer and the SB2 words. If a bit error were to foul SB1, or if the user chose to require both SYNC Bytes, then the false SB2 would be detected resulting in an incorrect clock synchronization and data word framing.

This illustrates that a user must study his choice of SB1, Spacer, and SB2 words and examine their resultant serial bit stream, checking for possible false or alias patterns. This is equally true for 8/9 encoded normal mode and for 8/8 non-encoded direct test mode, where the use of the last VCO '1' and last Spacer bit '0' are used to complete the SB1 and SB2 patterns.

The user also has the option to forego SYNC Byte detection and framing altogether. In this option the serial bit stream is not searched for the SB1 and SB2 patterns, the RCLK is not synchronized to anything, and the serial bit stream is simply captured in sequential eight bit sections and passed out to the NRZ pins. This is intended as a 'last resort' option when the serial bit stream is so corrupted that SYNC Byte words can not be detected for use in framing.

Channel Clock Divider

The base (or channel rate) clock for the digital back end write or read operations comes from the frequency synthesizer (or timing recovery) in the analog front end. The maximum frequency for this clock is beyond 202.5MHz (which is 9/8 x 180Mbit/sec, where 180Mbit/sec is the NRZ bit rate or frequency). This same clock is echoed by the digital back end during write mode operations as the serial write clock to strobe serial write data out of the digital back end and into the analog front end.

The minimum pulse width (high or low) for RCLK in byte mode is four channel-rate clock periods, regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free-running or synchronizing up to the SYNC Byte words. In Direct Test (÷ 8) both high and low pulses of RCLK are four channel-rate clock periods. In normal operation (÷ 9) the high pulse remains at four while the low pulse is expanded out to five channel rate clock periods.

For nibble mode, the minimum pulse width (high or low) for RCLK in byte mode is two channel-rate clock periods. This, too, is regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free-running or synchronizing up to the SYNC Byte words. In Direct Test both high and low pulses of RCLK are two channel-rate clock periods. In normal operation the low pulses remain at two while the high pulses alternate between two and three channel-rate clock periods. Thus the normal nibble clock period alternates between four and five channel clock periods just as the normal byte clock pulses alternate between four high and five low.

The NRZ read clock, RCLK, is used to strobe parallel NRZ data out of the VM65060 to the disk controller on the falling edge. This same clock is used to strobe parallel NRZ data into the VM65060. Either edge of the RCLK output can be selected and used to accommodate for phase delays either in the controller chip or in the NRZ interconnect lines. Also, an ‘echo’ of the RCLK output, supplied back to the WCLK input, can be used to strobe NRZ data in using the WCLK input’s rising edge.

When synchronization occurs at a SYNC Byte word, either the low or the high pulse of one RCLK period is expanded per the figures below. Short pulse glitches during synchronization are thus not allowed to happen.

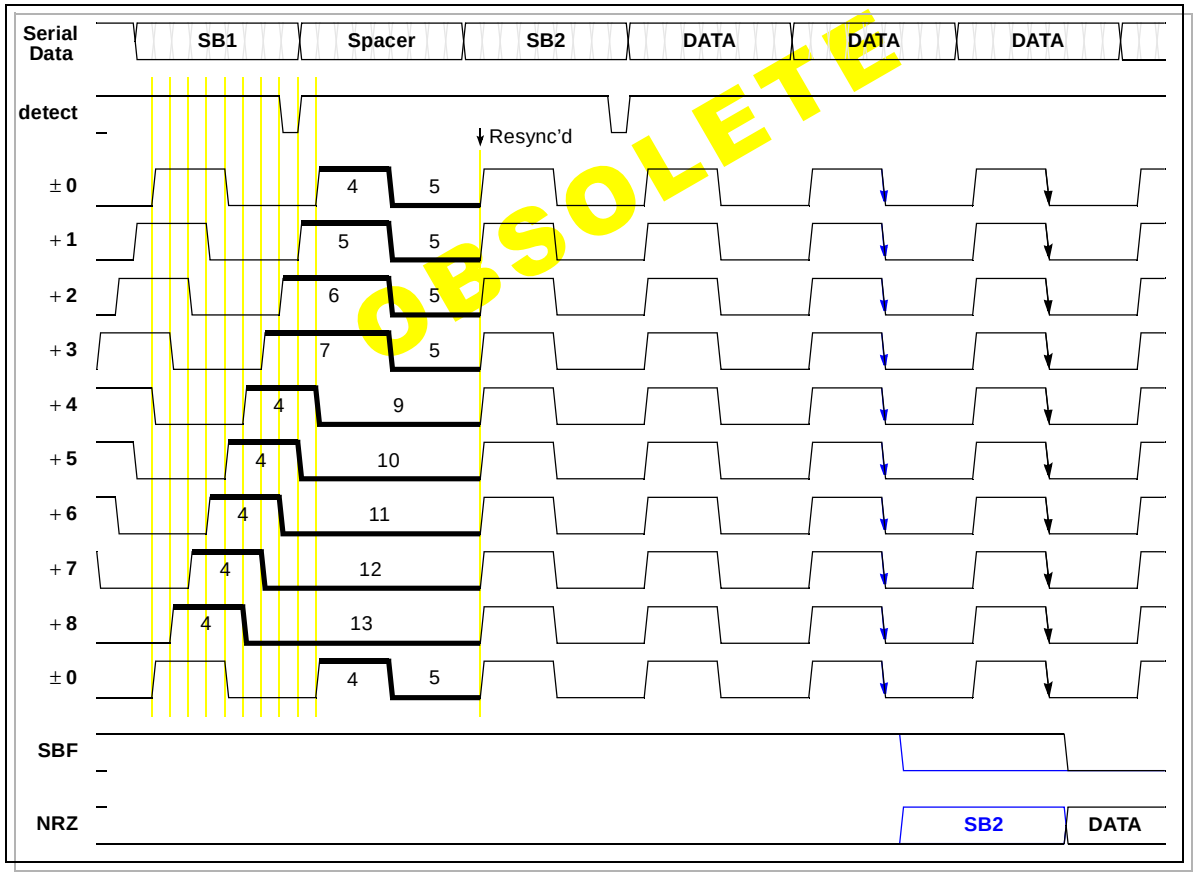


Figure 174 RCLK Synchronization Cases (Byte-Wide)

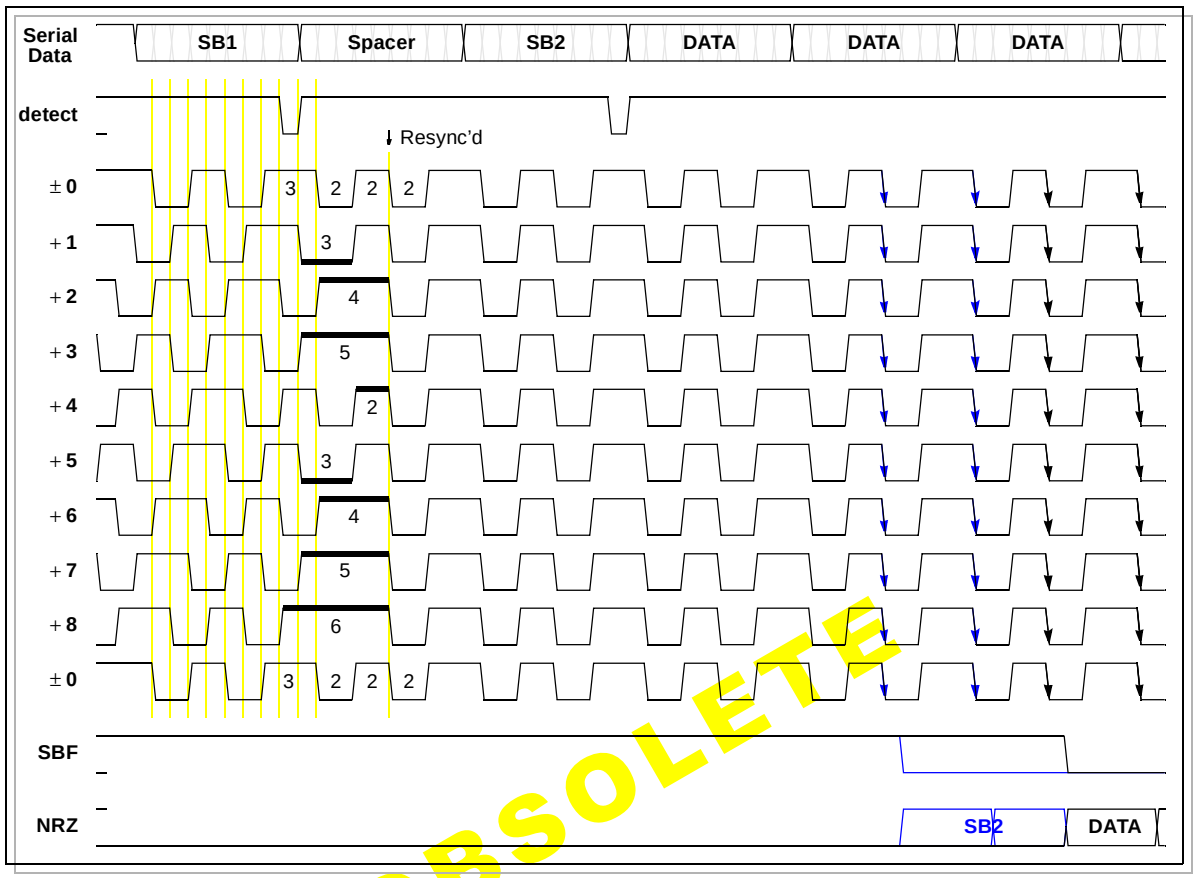


Figure 175 RCLK Synchronization Cases (Nibble-Wide)

The channel clock divider circuitry consists of a 4-bit counter that rolls over after either eight or nine clock cycles, depending on the setting of the DT bit in the serial control register. The rollover, or clearing, of the counter is based on the established count length or on the detection of a SYNC Byte word. When a SYNC Byte word is detected, the counter is cleared regardless of where it is in the count. The RCLK is created through the use of a synchronous set/reset flip flop with setting and resetting based on various decoded count values of the counter. The use of this flip flop eliminates any clock glitches during synchronization. The clearing of the counter due to the detection of a SYNC Byte words may cause either a second reset to follow an earlier reset resulting in an extended low pulse, or a second set to follow an earlier set resulting in an extended high pulse. There is no case where either pulse would be shortened due to synchronization.

The clock divider circuitry also creates the pulses used to control the parallel-to-serial and the serial-to-parallel transfers of data. These pulses are framed up with the incoming NRZ data words (with the first non-zero word) for write operations, and with the SYNC byte words for read operations.

WCLK Input

The WCLK input provides an optional input strobe for parallel NRZ data being written into the digital back end. The rising edge of this input is used as the strobing edge. The Control Register bit EXT is used to select the WCLK option. The signal sent to the WCLK input must be a copy, or echo, of the RCLK output. An externally-generated signal replicating the RCLK frequency is not acceptable. The RCLK output itself may be tied back into the WCLK input, but a more common practice is for the RCLK output to drive into a controller chip, used there to strobe out NRZ data; the controller then “turns around” the received RCLK and sends it back to the VM65060, along with the NRZ data, as the WCLK signal.

Initialize Clock Maker (ICM) Input

In order to synchronize testing of the digital back end, the Clock DIvider circuitry needs to be initialized to a known starting point and then released.

The Control Register bit VTC2 can be used for this purpose. but this requires writing the bit twice. An alternate method is provided via the ICM input pin. A ‘1’ on ICM initializes the clock divider, and a falling edge releases it to respond to serial clock pulses. Note that the bit VTC2 and the pin ICM must both be low for normal operation of the VM65060.

MODE CONTROLLER AND SEQUENCE CONTROLLERS

Four signal pins and three control register bits guide and determine the main operations of the digital back end. The pins are Servo Gate (SG), Read Gate (RG), Write Gate (WG), and Power Down (PD). The control register bits are Direct Test Mode (DTM), No Scramble (NOPR), and Sleep (SLEEP).

SG=X RG=X WG=X PD=X SLEEP bit =1

- ♦ Power Down Mode [PDM]
  - CML logic off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated
- ⇒ Can exit this PDM only by changing SLEEP bit to '0'.
  This should be done with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=X RG=X WG=X PD=1 SLEEP bit =0

- ♦ Power Down Mode [PDM]
  - CML logic off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated
- ⇒ Should exit PDM only with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=0 WG=0 PD=0 SLEEP bit =0

- ♦ Idle Mode [IM]
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated

SG=1 RG=X WG=X PD=0 SLEEP bit =0

- ♦ Servo Mode [SM] (SM ≡ IM for the digital back end)
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated
- ⇒ Should exit SM only with RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=1 WG=X PD=0 SLEEP bit =0

- ♦ Read Mode [RM]
  - CML logic on
  - NRZ outputs enabled, initially driving low
  - PRNG ready and waiting for enable upon SBF, uses RCLK
  - NRZ inputs disabled
- ⇒ Should exit RM only with SG=0, & WG=0, i.e. into Idle Mode
- ⇒ Should enter RM only with SG=0, & WG=0, i.e. from Idle Mode

SG=0 RG=0 WG=1 PD=0 SLEEP bit =0

- ♦ Write Mode [WM]
  - CML logic on
  - PRNG ready and waiting for enable upon NZD, uses internal WCLK (RCLK ↑ or RCLK ↓)
  - NRZ inputs enabled
  - NRZ outputs tristated
- ⇒ Should exit WM only with SG=0, & RG=0, i.e. into Idle Mode
- ⇒ Should enter WM only with SG=0, & RG=0, i.e. from Idle Mode

As seen above, the Sleep bit (SLEEP), when set to a '1', has the effect of overriding the four controlling pins. The No Scramble (NOPR), and Direct Test Mode (DTM) bits only modify the performance and operations within the various modes.

In byte operations (NIB=0) whenever DTM=0 the clock divider circuitry divides the serial channel clock frequency by nine to create RCLK. Whenever DTM=1 the division is changed to eight.

Whenever DTM=1, the PRNG circuitry is also disabled, regardless of the value of NOPR. Whenever DTM=0, the enabling of the PRNG is dependent upon the value of NOPR, with NOPR=1 providing a disable and NOPR=0 providing an enable.

The following figure shows, in state diagram form, the three operational modes of the digital back end. These modes are Idle / Servo mode, Read mode, and Write mode. Note that Idle and Servo modes are one and the same for the digital back end. This is not the case for the analog front end, where Idle mode is not equivalent to Servo mode. Also shown are the transitions between these modes. The usual and intended transitions are shown with the heavy arrows and control settings in bold. Other possible valid but less standard transitions are shown with dotted arrows.

These transitions are set via the hierarchy: SG overrides RG which overrides WG. These inputs are, by nature, all asynchronous. But there is a relationship between WG input, NRZ input, and the active clock write strobe edge, be it WCLK, RCLK rising, or RCLK falling. The first two input write clock edges following WG rising, or whichever signal put the chip into Write mode, are the two NRZ inputs that are ignored and assumed to be zero, whereas the third clock edge actually strobes in the NRZ inputs that are first checked for non-zero patterns.

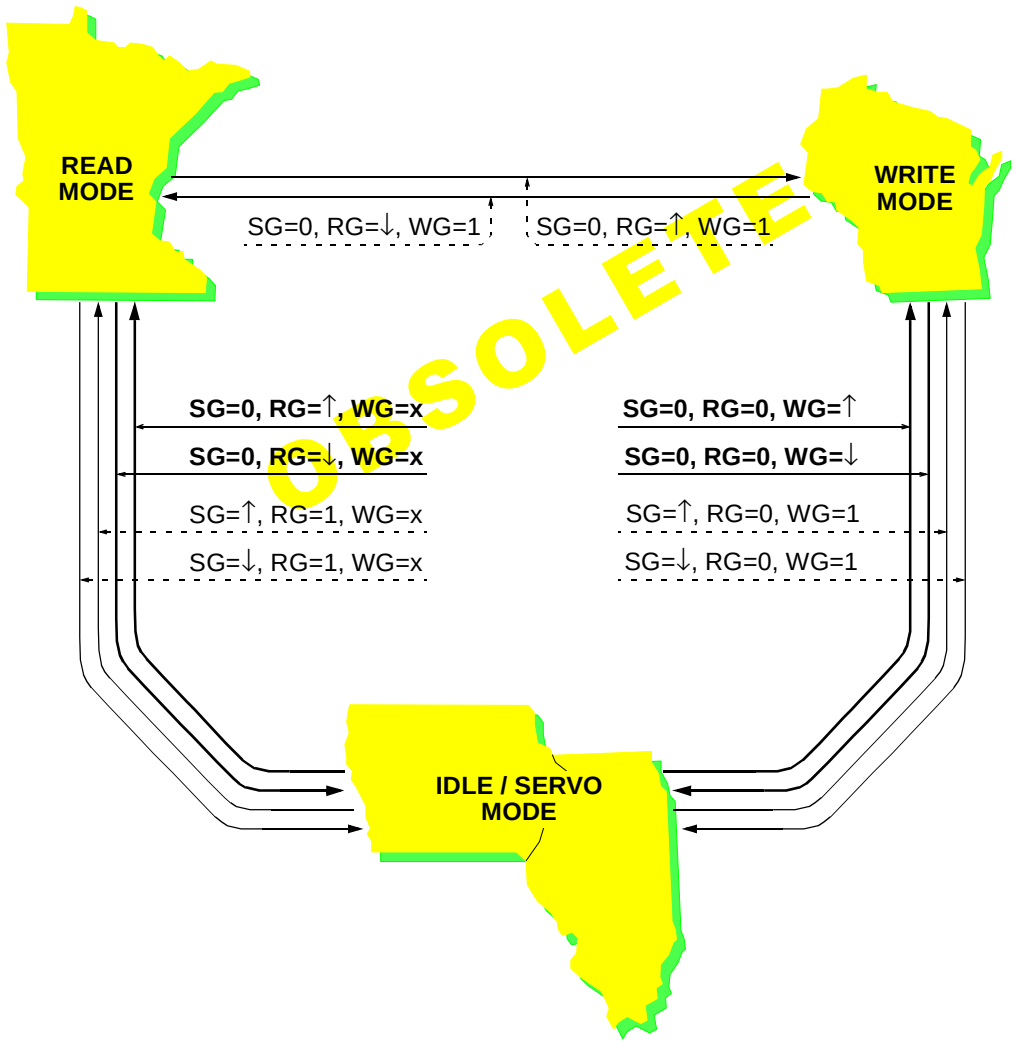


Diagram 1 State Diagram of Mode Transitions

MODE CONTROL AND POWER MANAGEMENT

The fundamental operating modes are controlled by the servo gate (SG), read gate (RG), and write gate (WG) input pins. The exclusive assertion of any of these inputs causes the circuit to enter that mode. If none of these inputs is asserted, the circuit is in IDLE mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately. SG and RG are asynchronous inputs and may be initiated or terminated at any time. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse to the preamp.

Table 216 Mode Control

WG	*RG*	*SG*	*PD*	*MODE*
X	X	X	1	Entire chip powered down; serial port still functional
0	0	0	0	IDLE mode; read data blocks powered down if PREN = '1'
X	X	1	0	SERVO mode; read data blocks powered down if PREN = '1'
X	1	0	0	READ mode; read data blocks powered on
1	0	0	0	WRITE mode; read data blocks powered down if PREN = '1'

DIGITAL CONTROL

Control of the chip is performed through a serial digital interface and a (16,12) bit wide register file. Control information is stored in the register file and used directly as digital control lines or sent to one of the DACs to create analog control signals.

The interface consists of three TTL-level signals for input/output data, clock, and enable. Upon asserting SPEN, the serial port is enabled and ready for input on SPDATA and SPCLK. The SPDATA line provides the read/write, address and data information.

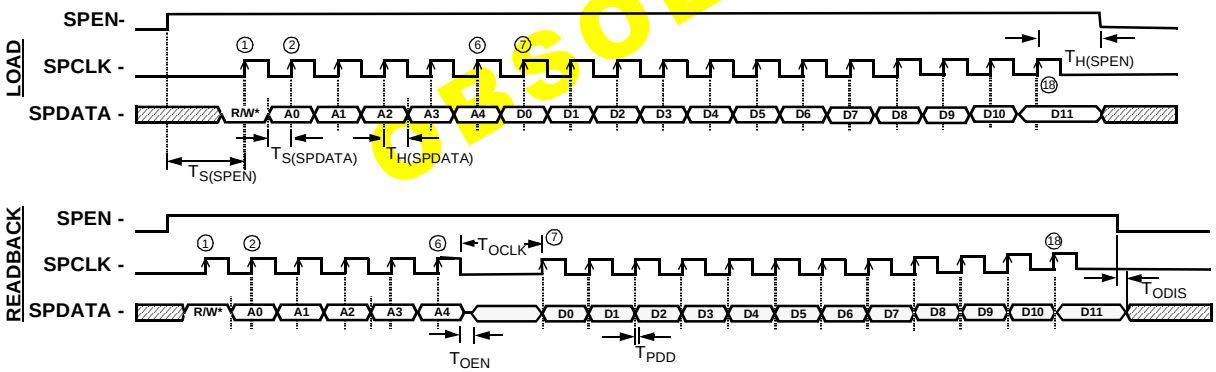


Diagram 2 Serial Register Load & Readback Timing

Table 217Serial Register Bit Allocation

Register Address	Data Bit											
	11	10	9	8	7	6	5	4	3	2	1	0
0	PGC DAC				SQPI DAC		FIR Tap 0				rsrv'd	rsrv'd
1	DR DAC						FIR Tap 6				rsrv'd	rsrv'd
2	CTF Data Group Delay						FIR Tap 1					rsrv'd
3	CTF Servo Group Delay						FIR Tap 5					rsrv'd
4	WPC Pattern 2				PGC EN	DHB W	FIR Tap 2					
5	WPC Pattern 3				WP CHR	FAQ SEN	FIR Tap 4					
6	WPC Pattern 1				TRB WR	TC2 4	TC3	FIR Tap 3				
7	FS Divide-by-N						SLE EP	PRS T	TRC KSL	PED	PDT ST	VIT OWD
8	Servo Gain				FSC KSL	Viterbi Threshold DAC						
9	Level Qual Pos V_{TH}					Damping Ratio DAC						
10	Level Qual Neg V_{TH}					LPF BYP	WDSEL[1:0]		SRV DB	TRG AIN	REF SEL	PRE N
11	CTF Data Fc							CTF Data Boost				
12	CTF Servo Fc							CTF Servo Boost				
13	HLD	TSR V	CPT ST	ACTST		SYMC		Zero Phase Restart DAC			PE Offset DAC	
14	CMX EN	TP1 Select			SEL TE	DAG C	DPL L	BMX EN	Test Mux Select			
15	FS Divide-by-M								AGC SF Count		PLL SF Count	
16	rsrv'd	VTC2	SB9	SB8	SB7	SB6	SB5	SB4	SB3	SB2	SB1	rsrv'd
17	DTM	NON E	BOT H	BESE L	FESE L	TFA Q	EXT	SBRT	EDG E	NOP R	NIB	rsrv'd
24	AE	DZ		INTL		ITW			NOS B	TWR		

*rsrv'd bits are VTC reserved control bits which should be programmed low

Table 218Serial Register Bit Descriptions

Reg. Addr	*Bit(s)*	*Description*	*Usage*
0	1:0	rsrv'd	always program low
	5:2	FIR Tap 0 2's Complement	K_0=0.0194×VALUE in V/V -8 ≤ VALUE ≤ 7
	7:6	SQPI DAC: AGC Sampled Charge Pump Current DAC	I=20×VALUE in µA I=Charge Pump Current
	11:8	PGC DAC: Programmable Gain Control DAC	$_V = [2(2.5 + VALUE)]$ 0 ≤ VALUE ≤ 15 A_V=VGA Gain
1	1:0	rsrv'd	always program low
	5:2	FIR Tap 6 2's Complement	$K_6 = 0.0194 \times$ VALUE in V/V -8 ≤ VALUE ≤ 7
	11:6	DR DAC: Data Rate DAC	$\omega_C = \left(\frac{\pi \times 10^{10}}{RR}\right) \times (33 + VALUE)$ in Mrad/s 0 ≤ VALUE ≤ 31 ω_c = VCO center frequency RR = Value of external resistor in Ohms
2	0	rsrv'd	always program low
	5:1	FIR Tap 1 2's Complement	$K_1 = 0.0195 \times$ VALUE in V/V -16 ≤ VALUE ≤ 15
	11:6	CTF Data Group Delay 2's Complement	$GD_{DC} = 0.95 \times VALUE$ in % -32 ≤ VALUE ≤ 31
3	0	rsrv'd	always program low
	5:1	FIR Tap 5 2's Complement	$K_5 = 0.0195 \times$ VALUE in V/V -16 ≤ VALUE ≤ 15
	11:6	CTF Servo Group Delay 2's Complement	$GD_{DC} = 0.95 \times VALUE$ in % -32 ≤ VALUE ≤ 31

Table 218Serial Register Bit Descriptions

4	5:0	FIR Tap 2 2's Complement	K_2 = (0.0195 × VALUE) -0.3125 in V/V -32 ≤ VALUE ≤ 31
	6	DHBW: Disable High Bandwidth Mode of AGC. Forces FAQ to remain low.	0: Normal Mode 1: Disable high bandwidth
	7	PGCEN: Enable Programmable Gain Control Mode of VGA. Allows the VGA gain to be adjusted through PGC DAC.	0: Normal Mode (AGC loop active) 1: Programmable Gain Mode
	11:8	WPC Pattern 2: Determines amount of precomp for pattern 2	Twpc = (0.013 • VALUE) • T 0 ≤ VALUE ≤ 15 Twpc = time delay of pattern transition T = Period of Data Rate clock
5	5:0	FIR Tap 4 2's Complement	K_4 = (0.0195 × VALUE) -0.3125 in V/V -32 ≤ VALUE ≤ 31
	6	FAQSEN: Enable Fast Acquisition on falling edge of Servo Gate (SG).	0: Normal Mode 1: Enable fast Acquisition
	7	WPCHR: WPC High Range Bit; Selects patterns 1& 3's precomp range See WPC Pattern 1 & 3	0: 0 - 20% Precompensation 1: 20 - 40% Precompensation
	11:8	WPC Pattern 3: Determines amount of precomp for pattern 3	Twpc = (0.013 • VALUE + 0.20 • WPCHR) • T 0 ≤ VALUE ≤ 15 Twpc = time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting
6	4:0	FIR Tap 3	K_3 = (0.0195 × VALUE) + 1.094 in V/V 0 ≤ VALUE ≤ 31
	5	TC3: Tap Centering, 3rd Tap. Controls gain offset in FIR center tap (tap 3).	0: Normal Mode, 1 < gain < 1.7 1: Test Mode, 0 < gain < 0.7
	6	TC24: Tap Centering, 2nd & 4th Taps. Controls the gain offset of FIR taps 2 & 4.	0: Normal Mode, -.93 < gain < +.3 1: Test Mode, -.62 < gain < +.62
	7	TRBWR: Reduces the Pmultiplier gain by factor of 1/4 in tracking mode.	0: Selects Pmult gain, P 1: Selects Pmult gain, P/4
	11:8	WPC Pattern 1: Determines amount of precomp for Pattern 1	Twpc = (0.013 • VALUE + 0.20 • WPCHR) • T 0 ≤ VALUE ≤ 15 Twpc = time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting

Table 218Serial Register Bit Descriptions

7	0	VITOWD: Viterbi OverWrite Disable. Allows the path memory over-write feature to be disabled in the Viterbi Detector	0: Normal Mode 1: Over-write disabled
	1	PDTST: Phase Detector Test. A high prevents the input to the decision-directed phase detector (and Viterbi detector) from switching from the low pass filter output to the FIR output.	0; Normal Mode 1: Test Mode
	2	PED: Timing Recovery Phase adjustment direction.	0: I_{offset} set by PE offset DAC added to DSFN 1: I_{offset} set by PE offset DAC added to DSFP
	3	TRCKSL: Timing Recovery Clock select, chooses between the TR VCO output being chosen or an alternative reference in its place	0: Timing Recovery VCO chosen (Normal) 1: Alternative reference chosen, specific reference determined by REFSEL bit
	4	PRST: Programmable reset for synth. dividers and divide-by-4's	0: Normal Mode 1: Reset Mode
	5	Sleep	0: Normal (Powered On) Mode 1: Power Off Mode
	11:6	FS Divide-by-N: Reference divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ in MHz f_{out} = the output frequency of VCO f_{FREF} = input frequency on FREF pin M = divide-by-M setting N = divide-by-N setting
8	6:0	Viterbi Threshold DAC. Nominal setting is VALUE = 45.	$VIT_{TH} = 0.047 + 0.376\left(\frac{VALUE}{127}\right)$ in Volts $0 \le VALUE \le 127$
	7	FSCKSL: Frequency Synthesizer clock select	0: VCO output selected (Normal Mode) 1: TCLKP/N input selected
	11:8	Servo Gain DAC: 4 bit DAC which controls the voltage gain of the servo block.	$V_{SB} = \left[\left(\frac{N \cdot V_{DIFF}}{3}\right) \cdot \left(0.6 + \frac{SDAC}{20}\right)\right] + 0.05$ V_{SB} = Integrated servo burst output in V. N = Number of integer servo burst cycles. V_{DIFF} = Continuous time filter differentiated output. (dppV). This signal can be measured on TP2 test point output. SDAC = Servo DAC setting (0 - 15). Nominal setting: 1000.

Table 218Serial Register Bit Descriptions

9	6:0	Damping Ratio DAC	$P = K \bullet \left(\frac{127 - VALUE}{127}\right)$ $\xi = \frac{P}{2}\sqrt{\frac{KVCO \cdot KDS \cdot C}{I \cdot G_m}}$ $0 \le VALUE \le 127$ K = Gain of Pmultiplier KVCO = Gain of TR VCO KDS = Gain of phase detector, either the PFD in W/I mode or DDPD in Read Mode C = Value of external capacitor I = Gain of Imultiplier G_m = Gain of QPUMP
	11:7	Level Qual Pos V_{TH}: PDQ Positive Threshold Qualification Level. Measured as a percentage of V_{LQ}	Vth = 20 + (1.9 × VALUE) in percent $0 \le VALUE \le 15$
10	0	PREN: WRITE/IDLE (W/I) mode power reduction enable	0: No power reduction in W/I mode 1: FIR/VIT/DDPD powered off during W/I
	1	REFSEL: Selects reference to use in place of Timing Recovery VCO output. Used in conjunction with TRCKSL Bit	0: Selects FDSP/N Input 1: Selects synth. output as reference
	2	TRGAIN: Selects Gain of QPUMP and Pmultiplier while in Tracking Mode compared to respective gains in Acquisition Mode	0: Attenuate QPUMP gain by 16, Pmult by 4 1: Attenuate QPUMP gain by 4, Pmult by 2
	3	SRVDB: Disables (powers down) Servo block and enables analog test mux	0: Servo block enabled 1: Servo block disabled
	5:4	WDSEL: Write Data Select, determines what signal will be output on the WDP/N lines	BIT (5:4) 0 0: Toggle Flip-Flop in data path 0 1: No Toggle Flip-Flop in data path 1 0: bypass precoder and write precomp 1 1: FDSP/N inputs outputted
	6	LPFBYP: Low Pass Filter Bypass. Allows differential signal to be injected immediately after the internal AC Coupling Caps. Test signal is input on RLOWZ and RFSR pins	0: Normal Mode 1: Test Mode (lowpass filter bypassed)
	11:7	Level Qual Neg V_{TH}: PDQ Negative Threshold Qualification Level. Measured as a percentage of V_{LQ}	V_{TH} = -20 + (1.9 × VALUE) in percent $0 \le VALUE \le 15$
11	4:0	CTF Data Boost	See Graph 12 on page 133
	11:5	CTF Data Fc: Cutoff frequency of LPF while in READ Mode	$f_C = (0.323 \times VALUE) + 7$ in MHz $0 \le VALUE \le 127$
12	4:0	CTF Servo Boost	See Graph 12 on page 133
	11:5	CTF Servo Fc: Cutoff frequency of LPF while in SERVO Mode	$f_C = (0.323 \times VALUE) + 7$ in MHz $0 \le VALUE \le 127$

Table 218Serial Register Bit Descriptions

13	1:0	PE Offset DAC: Phase Error Offset DAC used to add current to DSFP or DSFN depending on the PED bit setting. Corrects for phase offset in the timing recovery loop.	0.....0 µA 1.....5 µA 2.....10 µA 3.....15 µA
	4:2	ZPR DAC: Zero Phase Restart DAC used to determine time before first sample is taken on the Sync Field 2T pattern	Nominal setting: 10001
	6:5	Symmetric Control: Determines which if any of the taps will be symmetrically adjusted. See FIR Adaptation Circuit on page 136 for details.	SYMC.....Taps which will be identical --- 0.....(2 & 4) 1.....(2 & 4) & (1 & 5) 2.....(2 & 4) & (1 & 5) & (0 & 6) 3.....all taps asymmetric
	8:7	Adaption Control Test: Allows the adaption circuitry to be tested by forcing either an up, down or hold signal. See FIR Adaptation Circuit on page 136 for details.	ACtest.....Resulting mode --- 0.....Normal operation 1.....Up forced 2.....Down forced 3.....Hold forced
	9	CPTST: Used to test timing recovery charge pump (QPUMP) gains in Idle mode.	0: Normal Mode 1: Test Mode
	10	TSRV: Test Servo operating mode	0: Normal Mode (synchronous) 1: Test Mode (asynchronous)
	11	HLD: Hold mode for AGC and timing recovery loops.	0: Normal operation. 1: Both AGC and timing recovery loops forced into a hold (coast) mode. Intended for coasting over thermal asperities.

Table 218Serial Register Bit Descriptions

14	3:0	Test Mux Select: Selects which internal signal will be outputted on the various output pins	See Table 220
	4	BMXEN: Enables the Bipolar test point muxes	0: Bipolar Test Muxes disabled (Normal Mode) 1: Bipolar Test Muxes enabled
	5	DPLL Allows the internal PLL signal to be programmably enabled/disabled for test purposes. PLL is asserted at the transition from acquisition mode to tracking mode	0: Normal Mode, (PLL SF count enabled) 1: Test Mode, (PLL SF count disabled)
	6	DAGC: Allows the internal AGC signal to be programmably enabled/disabled for test purposes. AGC is asserted once the AGC count is reached in the Sync Field	0: Normal Mode, (AGC SF count enabled) 1: Test Mode, (AGC SF count disabled)
	7	SELTE: Selects which Timing Error the QPUMP will receive from the DDPD	0: Resampled Timing Error (Normal Mode) 1: Non-resampled Timing Error
	10:8	TP1 Select: Selects which internal signal to mux out to the TP1 test point.	See Table 219
	11	CMXEN: CMOS Test muxes enable	0: CMOS test mode disabled (Normal Mode) 1: CMOS test mode enabled

Table 218Serial Register Bit Descriptions

15	1:0	PLL SF Count: Determines how many user data bytes of data rate clock pass, after AGC has timed out, before PLL signal, tracking mode, begins	Bit Byte Clocks 1 0 0 0 0 1 0 1 2 1 0 3 1 1
	3:2	AGC SF Count: Determines how many user data bytes of data rate clock pass, after RGD has occurred, before AGC signal begins RGD occurs 2 user data bytes clocks following external RG being asserted	Bit Byte Clocks 1 0 4 0 0 5 0 1 7 1 0 9 1 1
	11:4	FS Divide-by-M: VCO feedback divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ in MHz f_{out} = the output frequency of VCO f_{FREF} = input frequency on FREF pin M = divide-by-M setting N = divide-by-N setting

Table 218Serial Register Bit Descriptions

16	0	rsrv'd	always program low
	9:1	Sync Byte 2 Pattern	This nine bit pattern and its complement define the two sync bytes.
	10	VTC2: Test mode to initialize clockmaker. Must be low for normal operation of VM65060.	0: Normal Mode 1: Clockmaker held at reset state
	11	rsrv'd	always program low
17	0	rsrv'd	always program low
	1	NIB: Control bit to determine NRZ interface mode	0: 8-bit wide (byte) mode 1: 4-bit wide (nibble) mode
	2	NOPR: Control bit which allows the pseudo random number generator to be disabled, thus the scrambler/descrambler also controlled	0: Normal Mode 1: Pseudo Random Number Generator (Scrambler/Descrambler) disabled
	3	EDGE: Determines which edge of RCLK the NRZ lines will be strobed in on	0: Positive edge of RCLK 1: Negative edge of RCLK
	4	SBRT: Determines if Sync Byte 2 will be returned prior to user data	0: No sync byte returned 1: Sync Byte 2 returned
	5	EXT: Select clock to strobe NRZ input data in	0: internal RCLK 1: External WCLK rising edge
	6	TFAQ: Test Fast Acquisition. Allows for testing of ultra fast decay current.	0: Normal Mode 1: Test Mode (Fast Acquisition. always on)
	7	FESEL: Front End Select. Allows signals inputted on TDATA/TCLK to be sent to the endec processor (digital backend)	0: Normal Mode 1: TDATA/TCLK sent to endec processor
	8	BESEL: Backend Select. Allows signals inputted on TDATA/TCLK to be sent to Precoder/WPC	0: Normal Mode 1: TDATA/TCLK sent to Precoder/WPC
	9	BOTH: Determines if both sync bytes need to be found or either	0: Either Sync Bytes may be found 1: Both Sync Bytes must be found
	10	NONE: Control bit which allows readback framing to be initialized with RG rather then Sync Byte Detect	0: Normal Mode 1: RG initializes readback framing
	11	DTM: Direct Test Mode which allows NRZ data to be directly passed through the backend, i.e. no scrambling/descrambling or encoding/decoding	0: Normal Mode 1: Direct Test Mode enabled

Table 218Serial Register Bit Descriptions

24	2:0	Tap Weight Rollover value: Determines which of the FIR taps will be adapted by determining which tap gets adapted following Tap 4. See FIR Adaptation Circuit on page 136 for details.	TWR .....Tap to 'roll-back' to ---------- 0.....Tap 0 1.....Tap 6 2.....Tap 1 3.....Tap 5 4.....Tap 2 5.....Tap 4
	3	NO Sync Byte: Allows the FIR adaption routine to begin without requiring a Sync Byte Found to occur. Adaption will begin after PLL SF Count has been reached with this bit set.	0: Normal mode, Sync Byte starts adaption 1: PLL SF Count starts adaption
	6:4	Initial Tap Weight: Determines which tap the adaption routine will adapt first. See FIR Adaptation Circuit on page 136 for more details.	ITW.....Tap to adjust first ---------- 0.....Tap 0 1.....Tap 6 2.....Tap 1 3.....Tap 5 4.....Tap 2 5.....Tap 4
	8:7	Integration Length: Determines the number of cycles the adaption circuit will integrate over when deciding whether the current tap weight should be incremented, decremented or held. See FIR Adaptation Circuit on page 136 for more details.	INTL.....Integration Length ---------- 0.....12 cycles 1.....15 cycles 2.....18 cycles 3.....21 cycles
	10:9	Dead Zone: Determines the required differential number of updates (delta) in either direction to qualify an increment or decrement decision. If this delta is not reached then the current tap weight is simply held. See FIR Adaptation Circuit on page 136 for more details.	DZ.....Differential number of updates ---------- 0.....delta = 2 1.....delta = 4 2.....delta = 6 3.....delta = 8
	11	Adaption Enable: Enables the adaption circuitry	0: Adaption circuit NOT active 1: Adaption circuit enabled

TEST MODES

There are sixteen test modes that are used in the VM65060. The test modes are controlled by two different sets of test addresses (TSEL[3:0] & TP1[2:0]) in the serial register, the bipolar test enable (BMXEN) and the CMOS test enable (CMXEN), as shown in Table 220 and Table 221.

Table 219 TP1 Control

BMXEN	TP1 SEL[2:0] bits			Output pins
	2	1	0	TP1 (diff analog)
1	0	0	0	TR VCO/4
1	0	0	1	Timing Error
1	0	1	0	Y_n
1	0	1	1	Vit Sig E
1	1	0	0	Held Sig Odd
1	1	0	1	FIR out
1	1	1	0	TR VCO Control
1	1	1	1	CTF norm ac
0	X	X	X	normal op.

Table 220 Bipolar Test Register Decode

BMXEN	TSEL[3:0] bits				mode	Output pins		
	3	2	1	0		TP2 (diff analog)	TP3 (PECL)	TP4 (PECL)
1	0	0	0	0	0	CTF norm	DV64	DV256
1	0	0	0	1	1	VGA in	FSUP	FSDN
1	0	0	1	0	2	VGA out	FS VCO	TR VCO
1	0	0	1	1	3	Vit Sig O	TR VCO/4	T0
1	0	1	0	0	4	Held Sig Evn	YHB/YLB	XPB/XNB
1	0	1	0	1	5	CTF diff	TRUP	TRDN
1	0	1	1	0	6	Int_ε	ε_n	C_n
1	0	1	1	1	7	Y_{n-1}	X_1	X_{N1}
1	1	0	0	0	8	none	FEDATA	FECLK
1	1	1	1	1	15	none	BEDATA	BECLK
0	X	X	X	X	X	power down	power down	power down

Table 221 CMOS Test Register Decode

CMXEN	TSEL[2:0] bits			mode	Output pins	
	2	1	0		RDS (CMOS)	RPOL (CMOS)
1	0	0	0	0	LP/LN	HCLK
1	0	0	1	1	LZDEL	FRDEL
1	0	1	0	2	HLDEL	RGDP
1	0	1	1	3	DMN	SRVCNT
1	1	0	0	4	AGCN	PLLN
1	1	0	1	5	SHGN	PDSELN
1	1	1	0	6	dv/dt comp	EA
1	1	1	1	7	NZD	PRN10
0	X	X	X	X	normal op.	normal op.

Table 222Test Signal Descriptions

Test Signal Name	Description
TR VCO/4	Timing recovery VCO clock divided by 4
Timing Error	Timing error for the Timing Recovery Loop.
Yn	Resampled FIR output at the “current” time
Vit Sig E	The even FIR interleave being input to the Viterbi detector.
Held Sig Odd	Held signal value for the odd interleave of Viterbi detector.
FIR out	Output of the Finite Impulse Response filter.
TR VCO Control	Analog control input to the Timing Recovery VCO.
CTF diff	Differentiated output of the Continuous Time Filter.
Held Sig Evn	Held signal value for the even interleave of Viterbi Detector.
DV64	Output of the 6-bit divide-by-N counter in the frequency synthesizer.
DV256	Output of the 8-bit divide-by-M counter in the frequency synthesizer.
VGA in	Analog input to the Variable Gain Amplifier of the AGC loop.
FSUP	Pump up signal from the phase-frequency detector in the frequency synthesizer.
FSDN	Pump down signal from the phase-frequency detector in the frequency synthesizer.
VGA out	Analog output of the Variable Gain Amplifier of the AGC loop.
FS VCO	Frequency synthesizer VCO output.

Table 222Test Signal Descriptions

Test Signal Name	*Description*
TR VCO	Timing recovery VCO output.
Vit Sig O	The odd FIR interleave being input to the Viterbi detector.
T0	FIR track and hold 0 control signal.
CTF norm	Normal output of the Continuous Time Filter
YHB/YLB	Timing recovery pump up (=0) / down (=1) in sampled mode, qualified by XPB/XNB signal = 1.
XPB/XNB	Timing recovery positive/negative sample sign indicator. Equivalent to (X1 xor X2).
CTF norm ac	AC coupled normal output of the Continuous Time Filter
TRUP	Pump up signal into the charge pump of the Timing recovery loop.
TRDN	Pump down signal into the charge pump of the Timing recovery loop.
Int_ε	Integrated lms tap weight error
ε_n	Sign of the PR4 equalization error estimate
C_n	Sign of the Channel data
EA	Enable Adaptation - This line indicates that either the positive or negative adaptation DZ threshold has been crossed by the integrator in the LMS_UPDATE block.
Yn-1	Resampled FIR output at the sampled one clock cycle before the “current” time
X1	Positive sample sign indicator for decision directed phase detector in the timing recovery.
XN1	Negative sample sign indicator for decision directed phase detector in the timing recovery.
LP	Signal from the level qualifier block indicating when the input pulse exceeds the programmed threshold.
HCLK	Signal from the level qualifier block which outputs a pulse for each input peak.
LZDEL	One-shot pulse which controls how long the AGC loop stays in low impedance mode. The RLOWZ external resistor controls the one-shot pulse width.
HLDEL	Hold control signal for the AGC loop. Active only in servo mode.
FRDEL	One-shot pulse which controls how long the AGC loop stays in fast acquisition mode. The RFSR external resistor controls the one-shot pulse width.
RGDP	Read gate delayed. Internal control signal which is delayed from RG by two bytes.
dv/dt comp	The CTF differentiated output after passing it through a comparator. Used by the servo block.
AGCN	Internal control signal indicating when the AGC loop switches from continuous time loop to samples time loop.
PLLN	Internal control signal indicating when the timing recovery loop switches from decision directed acquisition mode to decision directed tracking mode.
PDSELN	Phase detector select signal. Lo selects the decision directed phase detector, hi selects the phase frequency detector.
DMN	Servo control signal that when hi indicates one of the servo channels is integrating.
NZD	Non Zero Detect; test signal from digital backend.
SRVCNT	One bit from the servo 2-bit counter which controls servo channel selection sequence.

Table 222Test Signal Descriptions

Test Signal Name	*Description*
PRN10	Pseudo Random Number 10; PRNG output from digital backend.
BEDATA	Test signal: Digital Back End Data
BECLK	Test signal: Digital Back End Clock
FEDATA	Test signal: Analog Front End Data
FECLK	Test signal: Analog Front End Clock

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage

VCC . . . . . -0.3V to +7V

Input Voltages

Digital Input Voltage V_{IN} . . . . . -0.3V to V_{CC}+0.3V

Analog Input Voltage V_{IN} . . . . . -0.3V to V_{CC}+0.3V

Storage Temperature T_{stg} . . . . . -65°C to 150°C

Junction Temperature T_J . . . . . 150°C

Thermal Impedance, Θ_{JA} 80-Lead PQFP . . . . . 43°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage

VCC . . . . . +5V ± 10%

Junction Temperature T_J . . . . . 0°C to 125°C

PIN FUNCTION LIST AND DESCRIPTION

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty. A table showing the various pin types is provided in Table 223 below.

Table 223 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
Power Supplies	VCC1	27	LPF, servo, analog AGC, analog pulse qualification, analog test mux power
	VCC2	6	FIR, Viterbi detector, digital test muxes power
	VCC3	38	Frequency synthesizer analog power
	VCC4	58	Timing recovery analog power
	VCC5	45	Frequency synthesizer digital, timing recovery digital, write precomp and PECL output power
	VCC6	19	Front end digital CMOS power and N well.
	VCC6IO		Front end digital I/O power
	VCC7		Not Used (not a pin)
	VCC8	72	Digital backend CMOS power
	VCC9	65	Digital backend bipolar read power
	VCC10	70	Digital backend I/O N well connection
	VCC10Q		Digital backend CMOS core logic N well connection
	VCC11	3	Digital backend bipolar write power
Ground Supplies	VEE1	28	LPF, servo, analog AGC, analog pulse qualification, analog test mux ground
	VEE2	5	FIR, Viterbi detector, digital test muxes ground
	VEE3	39	Frequency synthesizer analog ground
	VEE4	57	Timing recovery analog ground
	VEE5	44	Frequency synthesizer digital, timing recovery digital and write precomp ground
	VEE6	18	Front end digital CMOS ground
	VEE6IO		Front end digital I/O ground and ESD substrate
	VEE7	63	Bipolar substrate connection
	VEE8	71	Digital backend CMOS ground
	VEE9	64	Digital backend bipolar read ground
	VEE10	69	Digital backend CMOS substrate
	VEE11	2	Digital backend bipolar write ground

Table 223 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
CMOS Inputs	ICM	1	Initialize ClockMaker, VTC test control. MUST BE LOW FOR NORMAL OPERATION.
	HOLD	4	External hold control which overrides the internally generated hold signal (Active Low)
	RG	7	Read Gate. When this signal is asserted, the read path circuitry is enabled (active high).
	WG	8	Write Gate. When this signal is asserted, the write path circuitry is enabled (active high).
	SG	9	Servo Gate. When this signal is asserted, the servo demodulator circuitry is enabled (active high).
	SRST	10	Servo Reset (active high)
	DEMOD	11	Enables selected area detector
	SPEN	14	Serial port I/O enable (active high)
	SPCLK	13	Serial port clock (latch on positive edge)
	PD	12	Power down control signal. When this signal is asserted, the chip is powered down (active high).
	WCLK	67	NRZ Write Clock; if used, must be synchronous with RCLK
Bipolar TTL Input	FREF	46	Reference frequency for the frequency synthesizer
CMOS Bidirectional	SPDATA	15	Bidirectional serial port data signal
	NRZ8-NRZ1	73-80	NRZ Parallel Read/Write Data
CMOS Outputs	RDS	17	Level qualifier data output. A high indicates a servo peak of qualified amplitude.
	RPOL	16	Level qualifier polarity output. A high indicates positive servo polarity. A low indicates negative servo polarity.
	SBF	66	Sync Byte Found Flag (Active Low)
	RCLK	68	User Data Read Clock

Table 223 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
Bipolar ECL-like Differential inputs (PECL)	FDSP FDSN	53 54	Reference frequency used to replace the timing recovery VCO output.
	TDATAP TDATAN	61 62	Test-mode Data inputs
	TCLKP TCLKN	59 60	Test-mode Clock inputs
Bipolar ECL-like Differential Outputs (PECL)	WDP WDN	49 50	Write data to the preamplifier.
	TP3P TP3N	47 48	Test point 3 output
	TP4P TP4N	51 52	Test point 4 output
Analog Inputs	DIP DIN	25 26	Differential Analog Read Data input from the preamplifier chip.
Analog Outputs	SREF	33	Servo Reference Voltage (0.6V)
	SBA	29	Servo burst A integrator output
	SBB	30	Servo burst B integrator output
	SBC	31	Servo burst C integrator output
	SBD	32	Servo burst D integrator output
	TP1P TP1N	34 35	Differential Analog test point 1 output
	TP2P TP2N	36 37	Differential Analog test point 2 output

Table 223 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
External Component Connections	RX	22	Filter reference resistor. An external 1% resistor is connected from this pin to analog ground to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency. Resistor (4KΩ to 32KΩ) to ground [see Eq. 190]
	RR	40	PLL reference resistor. An external 1% resistor is connected from this pin to analog ground to establish a precise internal reference current for the DACs controlling the timing recovery and synthesizer VCO center frequencies. Resistor (2.67KΩ to 5.11KΩ) to ground [see Eq. 197]
	RLOWZ	24	Low Z duration control. A resistor between this pin and ground defines the duration of the Low Z period.
	RFSR	23	Fast recovery/decay duration control. A resistor between this pin and ground defines the duration of the fast gain acquisition period.
	CAGCD	20	AGC data field gain storage, capacitor (390pF) to ground
	CAGCS	21	AGC servo field gain storage, capacitor (390pF) to ground
	DSFP DSFN	55 56	Timing Recovery PLL loop filter. Differential connections for the timing recovery PLL loop filter component. Capacitor (150pF) between pins.
	FSFP FSFN	41 42	Frequency Synthesizer PLL loop filter. Differential connections for the frequency synthesizer PLL loop filter components.
No Connect	nc	43	This pin may be connected to ground, if desired.

ELECTRICAL PARAMETERS, BY FUNCTIONAL DESCRIPTION

AC and DC Characteristics

Recommended operating conditions apply unless otherwise specified. 0°C < T_A < 70°C, 4.5V < VCC < 5.5V

Table 224Overall

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	Read Mode, Data Rate = 55 Mbps		270		mA
		Read Mode, Data Rate = 140 Mbps		280	330	mA
		Powerdown or Sleep Mode		3	6	mA
Recovery Time Standby to Fully Functional	T_{REC}	AGC with 10% final value, Pulse Detector without pulse pairing, Filter cutoff with 10% final value			10	uS

Table 225Logical Signals; TTL Compatible CMOS Inputs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	V_{IL} = 0.8V, all TTL compatible inputs except FREF			±10	µA
	I_{IL}	V_{IL} = 0.8V, FREF	120		360	µA
	I_{IH}	V_{IH} = 2.0V			±10	µA
Control Signal Rise and Fall Times	T_{CS}				100	ns
Input Capacitance	C_{IN}				10	pF

Table 226Logical Signals; TTL Compatible BiCMOS Outputs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	VOH_BICMLO	I_{OH} = -100 µA	V_{CC}-1.7	V_{CC}-1.4		V
	VOH_BICMOS	I_{OH} = -2 mA	V_{CC}-2.0	V_{CC}-1.6		V
Output Low Voltage	VOL_BICMLO	I_{OL} = 100 µA		0.02	0.1	V
	VOL_BICMOS	I_{OL} = 2 mA		0.21	0.5	V
Capacitive Load					20	pF

Table 227Logical Signals; PECL Inputs and Outputs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common Mode Input Voltage			V_{CC}-2.8V		V_{CC}	V
Differential Input Voltage			200			mV
Input Current	IIN	V_{IH}=V_{CC}			10	µA

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Table 227Logical Signals; PECL Inputs and Outputs

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	VOH_PECL	R_L=50Ω to V_{CC}-2V, T=27°C	V_{CC}-1.2	V_{CC}-1.02		V
Output Low Voltage	VOL_PECL	R_L=50Ω to V_{CC}-2.45V, T=27°C		V_{CC}–1.41	V_{CC}–1.2	V
Differential Output Swing		I_{OL}=I_{OH}≈18mA	300	390	500	mV
Output Leakage Current		Output disabled, V_{OUT}=V_{EE}, V_{CC}			±200	nA

Table 228Gain Control

Unless otherwise specified: V_{DI} = (V_{DIP} – V_{DIN}).

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Dynamic Range	V_{DI}	V_{DI} range such that the AGC is holding CTF_norma_ac at a locked amplitude. V_{DI} = 20 mVppd and 200 mVppd f_{in} = 5 MHz and 40 MHz	20		200	mV_{ppd}
Output Dynamic Range	V_{FA}	Measure CTF_norma_ac V_{DI} = 20 mVppd and 200 mVppd f_{in} = 5 MHz and 40 MHz	500		750	mV_{ppd}
Input Common Mode Voltage	V_{CMDI}	V_{CMDI} = (V_{DIP} +V_{DIN})/2	V_{CC}–3.1	V_{CC}-2.7	V_{CC}–2.3	V
Differential Input Resistance	R_{in}(DA)	LOWZ = Low	1.2	2.5	3.8	kΩ
	R_{in}(DA)_WG	LOWZ = High, WG=4.0V	120	250	380	Ω
Single Ended Input Resistance	R_{in}(SA)P R_{in}(SA)N	LOWZ = Low	.6	1.25	1.9	kΩ
	R_{in}(SA)P_WG R_{in}(SA)N_WG	LOWZ = High, WG=4.0V	60	125	190	Ω
VGA Minimum Gain PGCEN Reg bit=0	AVMIN_D AVMIN_S	VGA_{OUT}/V_{DI}, V_{CAGCX}=0.8V Idle mode and Servo mode		1.85	4.0	V⁄V
VGA Maximum Gain PGCEN Reg bit=0	AVMAX_D AVMAX_S	VGA_{OUT}/V_{DI}, V_{CAGCX}=3.2V Idle mode and Servo mode	39	44.5		V/V
VGA Maximum Gain PGCEN Reg bit=1	AV_{max}	AV=(V_{TP2P} -V_{TP2N})/V_{DI}, TM2 DAC= 0000 DAC= 0001 DAC= 0011 DAC= 0111 DAC= 1111		 5 12 18 28 46		V/V
Offset Voltage at CTF_norm	VOSFN	V_{DI} = 0, PGCEN = 1, PGC = 15 Measure V_{offset} at CTF_norm	-250	33	250	mV
Offset Voltage at CTF_diff	VOSFD	V_{DI} = 0, PGCEN = 1, PGC = 15 Measure V_{offset} at CTF_diff	-100	10	100	mV

Table 228Gain Control

Unless otherwise specified: $V_{DI} = (V_{DIP} - V_{DIN})$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Offset Voltage at CTF_norm_ac	VOSFA	V_{DI} = 0, PGCEN = 1, PGC = 15 Measure V_{offset} at CTF_norm_ac	-50	2	50	mV
PGC Gain	APGC_0 APGC_1 APGC_3 APGD_7 APGD_15	VGA_{OUT}/VGA_{IN}, PGCEN=1, Idle PGCDAC=0000 PGCDAC=0001 PGCDAC=0011 PGCDAC=0111 PGCDAC=1111	 1.8 4.4 9.0 19 41	 2.4 5.2 10.5 21.5 47.0	 3.0 6.0 12 24 53	V/V
Exponentiator Gain	AVGAexp	$20 \cdot \log_{10}[A_{VGA}(V_{CAGCx}=2.0V)]$ - $20 \cdot \log_{10}[A_{VGA}(V_{CAGCx}=1.5V)]$ Idle Mode and Servo Mode	7	8.6	10	dB
Output Common Mode Voltage	V_{CM}	$V_{CM} = (VGA_{OUTP} + VGA_{OUTN})/2$	V_{CC}–3.2	VCC-2.5	V_{CC}–1.8	V
VGA Output Offset Voltage	VOSV-GAMIN VOSGAMID VOSV-GAMAX	V_{DI}=0, PGCEN=1, Measure V_{OFFSET} at VGA_out PGCDAC=0000 PGCDAC=0111 PGCDAC=1111	 –75	 5	 75	mV
Frequency Response of CTF_diff	AVFD/ octave	Measure CTF_diff/VGAin over dynamic range of frequency. Determine slope of gain vs. frequency		5.6		dB/ octave

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Table 229AGC / Charge Pump

Unless otherwise specified: Idle mode, RG = 0, force V_{CAGCX} = 1.2V, LPFBYP = 1, TFAQ = 0, FAQSEN = 0, $V_{CM} = V_{CC}$ - 0.5 V, $V_{RLOWZ} = V_{CM} + V_D/2$, $V_{RFSR} = V_{CM} - V_D/2$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RX pin voltage	V_{RX}	R_{ext} = 6kΩ	1.05	1.2	1.35	V
Normal Charging Current, Continuous Mode,	I_{QNC_063} I_{QNC_00}	$V_D = (V_{RLOWZ}-V_{RFSR}) = 200mV$ SG=0, DRDAC=11111 SG=0, DRDAC=00000	16 8	20 10	24 12	µA µA
Normal Discharging Current, Continuous Mode	I_{QND_063} I_{QND_00}	V_D=275mV, TFAQ=0, FAQSEN=0 SG=0, DRDAC=111111 SG=0, DRDAC=000000	288 144	360 180	432 216	µA µA
Fast Discharging Current, Continuous Mode	I_{QFD_063} I_{QFD_00} I_{QFD_115}	$V_D = (V_{RLOWZ}-V_{RFSR}) = 375mV$ SG=0, DRDAC=11111 SG=0, DRDAC=00000 SG=1, DRDAC=XXXXX	2.24 1.12 1.12	2.80 1.40 1.40	3.36 1.68 1.68	mA mA mA
Fast Charging Current, Continuous Mode	I_{QFC_063} I_{QFC_00} I_{QFC_115}	$V_D=(V_{RLOWZ}-V_{RFSR})$ = 200mV then 375mV then 0 mV SG=0, DRDAC=11111 SG=0, DRDAC=00000 SG=1, DRDAC=XXXXX	144 72 72	180 90 90	236 118 118	mA mA mA
Ultra Fast Charging Current, Continuous Mode	I_{QUFC_063} I_{QUFC_00} I_{QUFC_115}	$V_D=(V_{RLOWZ}-V_{RFSR}) = 0.0mV$ SG=0, DRDAC=11111 SG=0, DRDAC=00000 SG=1, DRDAC=XXXXX	2.48 1.24 1.24	3.10 1.55 1.55	3.72 1.86 1.86	mA mA mA
Charge Pump Currents, Sampled Mode	$I_{QSU\_0\_63}$ $I_{QSU\_0\_0}$ $I_{QSU\_1\_63}$ $I_{QSU\_1\_0}$ $I_{QSU\_\_2\_63}$ $I_{QSU\_2\_0}$ $I_{QSU\_3\_63}$ $I_{QSU\_3\_0}$	V_D = 135mV, SG = 0, RG = 1, DRDAC=11111, SQPIDAC = 00 DRDAC=00000, SQPIDAC = 00 DRDAC=11111, SQPIDAC = 01 DRDAC=00000, SQPIDAC = 01 DRDAC=11111, SQPIDAC = 10 DRDAC=00000, SQPIDAC = 10 DRDAC=11111, SQPIDAC = 11 DRDAC=00000, SQPIDAC = 11	-3 -3 36 19 74 39 108 58	0 0 41 23 81 45 120 66	3 3 46 27 88 51 132 74	µA µA µA µA µA µA µA µA
	$I_{QSD\_0\_63}$ $I_{QSD\_0\_0}$ $I_{QSD\_1\_63}$ $I_{QSD\_1\_0}$ $I_{QSD\_\_2\_63}$ $I_{QSD\_2\_0}$ $I_{QSD\_3\_63}$ $I_{QSD\_3\_0}$	V_D = 225mV, SG = 0, RG = 1, DRDAC=11111, SQPIDAC = 00 DRDAC=00000, SQPIDAC = 00 DRDAC=11111, SQPIDAC = 01 DRDAC=00000, SQPIDAC = 01 DRDAC=11111, SQPIDAC = 10 DRDAC=00000, SQPIDAC = 10 DRDAC=11111, SQPIDAC = 11 DRDAC=00000, SQPIDAC = 11	-3 -3 33 15 72 36 107 54	0 0 38 19 79 41 119 62	3 3 43 23 86 47 131 70	µA µA µA µA µA µA µA µA

Table 229AGC / Charge Pump

Unless otherwise specified: Idle mode, RG = 0, force V_{CAGCX} = 1.2V, LPFBYP = 1, TFAQ = 0, FAQSEN = 0, $V_{CM} = V_{CC}$ - 0.5 V, $V_{RLOWZ} = V_{CM} + V_D/2$, $V_{RFSR} = V_{CM} - V_D/2$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Charge Pump Leakage Current	I_{LK}	HOLD = Active, Test Mode	–10		10	nA
Output Dynamic Range	V_{FA}	$V_{FA} = (V_{FAP}-V_{FAN})$ $20mV_{ppd} \leq V_{DI} \leq 200mV_{ppd}$ $5MHz < f_{in} < 40MHz$	0.45		.55	V_{ppd}
Output Distortion	THD	V_{DI} =200 mV_{ppd}, $V_{TP2} \leq 0.75V_{ppd}$, Test Mode 2, 1st, 2nd, and 3rd harmonics only			1.0	%
Gain Settle from –30% V_{DI} Step	T_{GD}	$V_{FN} \geq 0.9 \cdot$(final value)		20	25	µs
Gain Settle from +30% V_{DI} Step	T_{GA}	$V_{FN} \leq 1.1 \cdot$(final value)			1.5	µs
LOWZ One-shot Pulse Width	PW_{LZ}	LOWZ = Active, R_{LOWZ}=10kΩ	0.25	0.35	0.42	µs
FSREC One-shot Pulse Width	PW_{FSR}	LOWZ = Active, R_{FSR}=20.0kΩ	1.2	1.5	1.8	µs
Differential Input Capacitance	$C_{in(DA)}$				10	pF
Input Referred Noise Voltage	V_{IRN}	gain =AV_{max}, BW = 15MHz $V_{DIP} = V_{DIN}$			10	$nV/\sqrt{Hz}$
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common Mode Rejection Ratio	$CMRR_G$	gain = AV_{max}, f_{in} = 5MHz, $V_{DIP} = V_{DIN}$ = 100mV_{pp}	40			dB
Power Supply Rejection Ratio	$PSRR_G$	gain = AV_{max}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
AGC Gain Sensitivity to CAGCx Voltage	AV_{PV/V_D} AV_{PV/V_S}	(Typical range is 1.4V to 2.8V)		17.5		dB/V

Table 230Low Pass Filter (7-Pole, 0.05^{o}, Equiripple Phase)

Signals measured at TP2 unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Filter Cutoff Frequency (low end)	f_{Cmin_d} f_{Cmin_s}	Fc_{DAC}=00h, REXT=6kΩ, Idle mode and Servo mode	3.15	4.5	5.85	MHz
Filter Cutoff Frequency (middle)	f_{Cmid_d} f_{Cmid_s}	Fc_{DAC}=40h, REXT=6kΩ, Idle mode and Servo mode	24.0	26.0	28.0	MHz
Filter Cutoff Frequency (high end)	f_{Cmaxd} f_{Cmaxs}	Fc_{DAC}=7Fh, REXT=6kΩ , Idle mode and Servo mode	45.6	48	50.4	MHz
Normal Lowpass Gain (V_{FN} vs. V_{FI})	AO_N	$BOOST_{DAC}$=00h, Fc_{DAC}=00h, REXT=6kΩ, f_{in} = 4MHz	-4.2	-3.2	-2.2	dB
Differentiated Lowpass Gain (V_{FD} vs. V_{FN})	AO_D	$BOOST_{DAC}$=00h, f_{in} = 4MHz Fc_{DAC}=00h, REXT=6kΩ,	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
Boost Accuracy	BA		-1		+1	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$=00h, REXT=6kΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$=1Fh, REXT=6kΩ	12.0	13.0	14.0	dB
Normal Filter Output Offset	V_{OSFN}	V_{FI} = 0.0V	–200		200	mV
Differentiated Filter Output Offset	V_{OSFD}	V_{FI} = 0.0V, FDP/N outputs	–10		10	mV
AC Coupled Filter Output Offset	V_{OSFA}	V_{FI} = 0.0V, FAP/N outputs	–10		10	mV
Total Harmonic Distortion (V_{FN} or V_{FD} vs. V_{FI})	THD_F	$f_{in} = 0.67 f_C$, Fc_{DAC}=7Fh, REXT=6kΩ, $V_{FI} \leq 0.7V_{ppd}$, 2nd, and 3rd harmonics only			1.5	%
Group Delay	T_{GD}	Fc_{DAC}=7Fh, REXT=6kΩ	10	12	14	ns
Group Delay Variation (normal or differential), GD=00h (i.e. symmetric zeros). Measured at Normal Outputs.	T_{GD1}	$0.1 f_C \leq f_{in} \leq 1.5 f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$=00h, REXT=6kΩ	–2.0		2.0	%
	T_{GD2}	$0.1 f_C \leq f_{in} \leq 1.5 f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$=1Fh, REXT=6kΩ	–2.5		2.5	%
Group Delay Variation Nonsymmetric Zeros	T_{GD3}	DC @ FNP/N outputs. GD_{DAC}=-32, relative to GD_{DAC}=0	–32		-28	%
	T_{GD4}	DC @ FNP/N outputs. GD_{DAC}=+31, relative to GD_{DAC}=0	28		30	%
Normal Output Noise Voltage	V_{NN}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			TBD	mV_{rms}
Differentiated Output Noise Voltage	V_{ND}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			9.0	mV_{rms}
Common Mode Rejection Ratio	$CMRR_F$	f_{in} = 5MHz, Fc_{DAC}=7Fh, REXT=6kΩ$V_{DIP} = V_{DIN}$ = 100mV_{pp}	40			dB

Table 230Low Pass Filter (7-Pole, 0.05^0, Equiripple Phase)

Signals measured at TP2 unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp}	40			dB
Filter Settle From Step in Fc and BOOST	T_{FS}	Fc_{DAC} or $BOOST_{DAC}$ step to V_{FN} settle		85	300	ns
[1] Fc_{DAC}=7Fh, $BOOST_{DAC}$=1Fh (boost level is 13dB).						

Table 231Finite Impulse Response Filter

Conditions unless otherwise specified: TC3=0, TC24=0, taps $K_{0,1,5,6}$=0 and $K_{2,4}$=16dec, ZPR=0.

PARAMETER	SYM	CONDITIONS[1]	MIN	TYP	MAX	UNITS
Nominal Center Tap Gain	AV_c	Set bit three in K3	1.15	1.25	1.3	V/V
Center Tap Gain Variation		Set bit three in K3. Min vs. max percentage gain when a 0.2v dc signal is applied for eight successive channel samples.	0	1.0	2.0	%
Center Tap Offset	OFF_c	Set bit three in K3		3	5	mV
Feed Through	FTH	Set all taps to 0, clear TC3 & TC24 feed in a.5vp-p low freq. square wave		TBD		Vp-p diff
Output Toggle Test	OTT	Same as AV_c with.5vp-p $F_S/2$ square wave [2]		TBD		Vp-p diff
TH Droop	DAV	Average droop 0.25 Vdiff[2]			30	V/µs
Center Tap Large Signal BW	LSBW	Same as AV_c,with the input being a swept AC signal 0.5vp-p diff.[2]		TBD		MHz
Center Tap Small Signal BW	SSBW	Same as AV_c,with the input being a swept AC signal 0.05vp-p diff.[2]		TBD		MHz
Center Tap Offset Variation	OFFv	P-P offset synchronized by T0		5	10	mV
Tap Gain & Linearity	TG	Average tap gain per step (K 1-5)	17.5	19.5	21.5	Mv/v
	AV_3	K_3=11111 bin Maximum Voltage gain of center tap		1.699		V/V
	$AV_{0,6}$	$K_{0,6}$ =0111 bin Maximum Voltage gain of taps 2 or 4		0.0685		V/V
	$AV_{1,5}$	$K_{1,5}$ =01111 bin Maximum Voltage gain of taps 1 or 5		0.0293		V/V
	$AV_{2,4}$	$K_{2,4}$ =011111 bin Maximum Voltage gain of taps 2 or 4		0.0293		V/V
	DNL	Differential non-linearity	25	100	175	%
	INL	Integral non-linearity		1.5		lsb
Sampler phase matching	SPM	Differentially measure 40MHz sinewave vp=0.4V at zero crossing from edge to edge synchronized by T0.		1 or 14mV		deg. dV

Table 231Finite Impulse Response Filter

Conditions unless otherwise specified: TC3=0, TC24=0, taps $K_{0,1,5,6}$=0 and $K_{2,4}$=16dec, ZPR=0.

PARAMETER	*SYM*	*CONDITIONS*[1]	*MIN*	*TYP*	*MAX*	*UNITS*
TH Droop	DAV	Average droop 0.25 v diff [3]			30	V/µs
	DD	Delta droop max to min [3]			15	V/ns
Center Tap Distortion	MX2nd	Set the input to 0.5vp-pdiff @ 31/ 128*F_S with F_S set to max data rate			-35	dBc
	MX3rd				–35	dBc
	MXTHD				-30	dBc
Max EQ Distortion	MX2nd	Same as center tap distribution. with amplitude set to 0.17vp-pdiff. Max peaking [5]			-35	dBc
	MX3rd				–35	dBc
	MXTHD				-30	dBc
Noise	η_{CT}	CT only [4]				Vrmsd/ √Hz
	η_{MX}	Max peaking [4]				Vrmsd/ √Hz
2T Boost at F_S/4 [5]	MXB_{2T}	K2 & K4 set to 32, Vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/2		2.5		V/V
	MNB_{2T}	K2 & K4 set to 31, vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/2		0		V/V
4T Boost at F_S/4 [3,5]	MXB_{2T}	K1 & K5 set to 16, vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/4		1.875		V/V
	MNB_{2T}	K1 & K5 set to 15, vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/4		0.664		V/V
6T Boost at F_S/4 [3,5]	MXB_{6T}	K0 & K6 set to 8, vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/2		1.5625		V/V
	MNB_{6T}	K0 & K6 set to 7, vin =0.1 Vp-p diff, K3=8, Fin = Fchannel/2		0.9765625		V/V

[1]The part must be placed in test mode and the ac bypass will be used as an input and the FIR out test points used as outputs. The sample clock is taken from the external clock input and the frequency can be set for convenience.
[2]These test should be done at the highest device clock rate.
[3] Set taps K3=8 & K2/K4 = 16 and clear all others
[4] Set taps K3=31, K2/4=32, K1/5=16, & K0/6=8
[5] Relative to the nominal center tap gain

Table 232FIR Adaptation Circuit

Conditions unless otherwise specified: R_{TR}=2kΩ

Integration Slope (Up and Down)	IS_{U00}	ACTST = 3. DRDAC = 31. Tap weights = zero gain, except Tap 3 = unity gain. CLK phase adjusted relative to FIR IN signal to create integrate up, down and hold conditions. Signal peak measured relative to reset value and normalized to integration length (12 for INTL='00')		4.65		mV/ns
	IS_{U01}			3.7		mV/ns
	IS_{U10}			3.1		mV/ns
	IS_{U11}			2.6		mV/ns
	IS_{D00}			4.6		mV/ns
	IS_{D01}			3.7		mV/ns
	IS_{D10}			3.1		mV/ns
	IS_{D11}			2.6		mV/ns
Integration Length	IL_{00}	ACTST = 3. DRDAC = 31. Tap weights = zero gain, except Tap 3 = unity gain. CLK phase adjusted relative to FIR IN signal to create integrate up conditions. IL + 12 = INT_ε output normalized to CLK period.		12		cycles
	IL_{01}			15		cycles
	IL_{10}			18		cycles
	IL_{11}			21		cycles
Dead Zone Threshold (Up and Down)	DZU_{00}	ACTST = 0. DRDAC = 31. Tap weights = zero gain, except Tap 3 = unity gain. CLK phase adjusted relative to FIR IN signal to create integrate up, down and hold conditions. Int_ε measured when EA goes high.		106		mV
	DZU_{01}			145		mV
	DZU_{10}			192		mV
	DZU_{11}			237		mV
	DZD_{00}			106		mV
	DZD_{01}			145		mV
	DZD_{10}			192		mV
	DZD_{11}			237		mV

Table 233Viterbei Detector

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Exhaustive Path Memory Overwrite Test	VIT_{EMPATH}	Test all possible overwrite paths in path memory. Signal into RFSR/RLOWZ, LPFBYP = 1, PDTST = 1, VITOWD = 0, VIT TH DAC = 45d			0	Wrong bits
Sliding Window Test (see test plan for test definition)	Signal into RFSR/RLOWZ,LPFBYP = 1, PDTST = 1, VITOWD = 1					
	VIT_{TH_MIN}	Vit the DAC setting to get error free Pattern 1 out of FEDATA test point			35	
	VIT_{TH_MAX}	Vit the DAC setting to get error free Pattern 2 out of FEDATA test point	55			
	VIT_{TH_DELTA}	Difference between the 2 DAC settings				
Viterbi DAC Differential Nonlinearity					2	LSB

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Table 234Detecting Servo Demodulator

Conditions unless otherwise specified: test SBA-SBD, f_{IN} = 10 MHz, integration time = 900ns (9 cycles of 10 MHz)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Servo Input Frequency	f_{INS}		4	10	13.5	MHz
Gain $[(V_{SBX}–V_{SREF})/V_{LQ}]$	AV_S	measured over 1/4 to 3/4 of scale [1] SDAC=1000b [3]	0.84	1.20	1.56	V/V
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [2]	–0.5		0.5	%
Linearity of $V_{SVO}–V_{SVR}$ vs. V_{DI}	V_{DL1}	measured over 1/8 to 7/8 of scale [2]	–1.4		1.4	%
Output Offset (not referred to input)	V_{SO}	intercept of regressed line [2]	–40		40	mV
Output for Zero Input	V_{ZI}		0	50	60	mV
Channel A, B, C & D Mismatch	V_{MM}	Variation for a common input % of full scale @ 1/2 of full scale	-1.0		1.0	%
SREF Voltage	V_{SR}		3.50	3.60	3.70	V
Integrating Cap Decay Rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec
Servo DAC linearity	$SDAC_{LIN}$	Linearity bits SDAC=1,2,4,8	-1/2		1/2	LSD
Channel to Channel Cross Talk	V_{CT}	Effect of A on B etc. % of full scale	-0.5		0.5	%
Output Impedance	R_{SO}	SREF and SRVOUT pins			50	Ω
Demodulator Repeatability (52dB)	N_{DR}	Repeatability without external noise	-5.0		5.0	mV
Power Supply Rejection Ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp} [4]	25			dB
Common Mode Rejection Ratio	$CMRR_S$	0MHz ≤ f_{in} ≤ 1MHz V_{LQP} = V_{LQN} = 100mV_{pp} [4]	25			dB
Total System Gain Variation $[(V_{SVO}–V_{SVR})/V_{DI}]$	AV_A	over all V_{DI}, SDAC=1000b [3] 1/4 to 3/4 of scale [1]	0.84	1.20	1.56	V/V

[1] This specification is the slope of the characteristic ratio of a DC voltage out (SBA-SBD) to a peak to peak voltage (sine wave).
[2] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[3] SDCA = Servo DAC.
[4] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

Table 235Frequency Synthesizer

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSVCO Center Frequency	FS_ $R_{MIN}\_D_{MAX}$ $R_{MIN}\_D_{MIN}$ $R_{NOM}\_D_{MAX}$ $R_{NOM}\_D_{MIN}$ $R_{MAX}\_D_{MAX}$ $R_{MAX}\_D_{MIN}$	$f_{0(VCO)}$=(5292/RR)·(42+DRDAC) DR=63, f_{0MAX}(2.67k) DR=0, f_{0MAX}(2.67k) DR=63, f_{0MAX}(4k) DR=0, f_{0MAX}(4k) DR=63, f_{0MAX}(5.11k) DR=0, f_{0MAX}(5.11k)	 187 75 125 50 97 40	 208 83 139 56 108 44	 229 91 153 62 119 48	MHz
Normalized VCO Gain	KS_RR_DR	measured at TP4P/N	0.32		0.42	V^{-1}
FSVCO Center Frequency Ratio	FS_RR_RAT	f_{0MAX}/f_{0MIN}, RR=2.67k, 4k, 5.11k	2.42	2.47	2.52	MHz/MHz
FSVCO Center Frequency Linearity	FSLIN_RR	(f_{0MAX}/f_{0MIN})/31 = LSB, RR = 2.67k, rk, 5.11k f_{0ideal}, DPR=127 DR=0,1,2,4,8,16,32,63	-1/2		1/2	LSB
RR Voltage	V_{rr}_RR		1.20	1.28	1.36	V
FSFP Voltage	DV_{fsfp}	V_{fsfp}-V_{fsfn}	-1.0		1.0	V
FSFN Voltage	V_{fsfn}		2.10	2.35	2.60	V
FSFILT Leakage Current	SQ_{PUMP}_LEAK		-300		300	nA
FS Charge Pump Current	SQD_RR_DR	I_{fsqp}=(15,370/RR)•(102.8-DRDAC)	0.90·I_{fsqp}		1.10·I_{fsqp}	µA
		Guaranteed Range	120		700	µA
DOWN/UP FS Charge Pump Currents	SQD/SQU	(I_{FSQP} DOWN) / (I_{FSQP} UP)	0.98		1.05	
Closed Loop Jitter	VCO_{FS} Jitter	(I_{fsfp} - V_{fsfn}) = 0, 160 MHz		35		ps_{rms}

k_I is 5.05 MHz/mA
K_{fsf} is the value of the Data Rate DAC word, [0 to 31]
I_{REF} is the reference current being sunk from pin RR in µA, $I_{REF}=V_{rr}/R_{ext}$

Table 236Timing Response (TR) Loop

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DSFP/N Common Mode Voltage	VCM_DSF		1.8	2.1	2.4	V
TRVCO Center Frequency	FTR_ $R_{MIN}\_D_{MAX}$ $R_{MIN}\_D_{MIN}$ $R_{NOM}\_D_{MAX}$ $R_{NOM}\_D_{MIN}$ $R_{MAX}\_D_{MAX}$ $R_{MAX}\_D_{MIN}$	$f_{0(RR)}$=(5410/RR)·(39.1+DRDAC) DPR=127, V_{dsfp}-V_{dsfn}=0 DR=63, f_{0MAX}(2.67k) DR=0, f_{0MAX}(2.67k) DR=63, f_{0MAX}(4k) DR=0, f_{0MAX}(4k) DR=63, f_{0MAX}(5.11k) DR=0, f_{0MAX}(5.11k)	 186 71 124 48 97 37	 207 79 138 53 108 41	 228 87 152 58 119 45	MHz
TRVCO Center Frequency Ratio	FTR_RR_RAT	f_{0MAX}/f_{0MIN}, RR=2.67k, 4k, 5.11k	2.3	2.6	2.9	MHz/MHz

Table 236Timing Response (TR) Loop

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
TRVCO Center Frequency Linearity	FTRLIN_RR	f_0/f_{0ideal}, DR=0, 1, 2, 4, 8, 16, 32, 63 f_{0ideal}={[(f_{0MAX}-f_{0MIN})/63]•DR} + f_{0MIN} RR = 2.67k, rk, 5.11k, DPR=127	-2		2	LSB
TRVCO Gain	KTR_RR_DR	k_v = (f(.5) - f(-.5)/f_0 D_{dsfp}-V_{dsfn} = ±0.5V, DPR = 127	0.18		0.27	MHz/V
FS/TR VDCO f_C Ratio	Fs/FTR_RR_DR	DRDAC =), 63; RR = 2.67k, 5.11k	0.96		1.09	
TR Charge Pump Offset Current	QPUMP_IOS HLD TRGN0 TRGN1	IDEL mode, HLD=1, Vdsfp-Vdsfn=0, PE Offset DAC = 00 CPTST=0 CPTST=1, TRGAIN=0 CPTST=1, TRGAIN=1	 -3 -6 -6		 3 6 6	 µA µA µA
TR Phase Offset Current	PEOS_ PED0_01 PED1_01 PED0_10 PED1_10 PED0_11 PED1_11	HLD=1, Vdsfp-Vdsfn=0, CPTST=1, TRGAIN=1 PED=0, PE Offset DAC=01 PED=1, PE Offset DAC = 01 PED=0, PE Offset DAC=10 PED=1, PE Offset DAC = 10 PED=0, PE Offset DAC=11 PED=1, PE Offset DAC = 11	 -5 1 -8 4 -12 6		 -1 5 4 8 -6 12	 µA µA µA µA µA µA
TR Charge Pump Gain (I_{QP}/Timing Error)	I_{TRQP}	Idle/Acquisition Mode, CPTST=0	420	600	780	µA/V
		Tracking Mode: TRGAIN = 0, CPTST =1 TRGAIN = 1, CPTST =1	 31 49	 39 61	 47 73	 µA/V µA/V
		Hold Mode: HLD=1	-0.1		0.1	µA/V
Pmult Offset Voltage	P_{MULT_VOS}	DR=0, (V_{dsfp}-V_{dsfn})=0, DPR=0, VCOIN=TP1, SEL=6	-25		25	mV
Imult Offset Voltage	I_{MULT_VOS}	DR=0, (V_{dsfp}-V_{dsfn})=0, DPR=127 VCOIN=TP1, Sel=6	-25		25	mV
Imult Gain	 I_{MULTAV}_R_{MIN}_D_{MX} I_{MULTAV}_R_{MIN}_D_{MN} I_{MULTAV}_R_{NOM}_D_{MX} I_{MULTAV}_R_{NOM}_D_{MN} I_{MULTAV}_R_{MAX}_D_{MX} I_{MULTAV}_R_{MAX}_D_{MN}	VCOIN/(V_{dsfp}-V_{dsfn}), VCOIN=TP1, SEL=6, V_{dsfp}-V_{dsfn} = ±0.25V, DPR=127 DR=63, A_{IMAX}(2.67k) DR=0 A_{IMIN}(2.67k) DR=63, A_{IMAX}(4k) DR=0 , A_{IMIN}(4k) DR=63, A_{IMAX}(5.11k) DR=0, A_{IMIN}(5.11k)	 1.44 0.53 0.96 0.36 0.75 0.28	 1.80 0.67 1.20 0.45 0.94 0.35	 2.20 0.80 1.44 0.54 1.13 0.42	V/V
Imult Gain Linearity	IMULTLIN_RR	(A_{IMAX} - A_{IMIN})/63 = LSB RR= 2.67k, 4k, 5.11k A_{ideal} = LSB* DR + A_{IMIN}, A_I/A_{ideal} , DR=0, 1, 2, 4, 8, 16, 32, 63	-1		1	LSB

Table 236Timing Response (TR) Loop

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Pmult Gain	PMULTAV/1 PMULTAV/4	$TRVCO_{Control}$/TimingError V_{dsfp}-V_{dsfn}=0, DPR=0 , READ mode Timing error = +/- 200 mV TRBWR=0 TRBWR=1	.9 .209		1.1 .259	V/V V/V
Pmult Gain Linearity	PMULT_LIN	A_{PMAX}/127 = LSB, A_{ideal} = LSB* DPR, A_P/A_{ideal}, DPR=1, 2, 4, 8, 16, 32, 64, IDLE mode, Force pump UP/DOWN,	-3		3	LSB
Phase/Frequency Output Swing	PFSWING_UP PFSWING_DOWN	IDLE mode, TP1,Sel=1 Force Pump Up Force Pump Down	.59 -.59	.65 -.65	.71 -.71	V V
Decision Directed P.D. Yn,Yn-1 Offset	YN_VOS YN-1_VOS	V_{Rlowz}-V_{Rfsr}=0, Vcm=4.3V, LPYBPY=1, PDTST=1, Fclk(FDSP/N)=40 MHz	-20		20	mV
Decision Directed P.D. Timing Error Offset	TE_VOS_SELTE1 TE_dVOS_SELTE0	V_{Rlowz}-V_{Rfsr}=+/-0.2, Vcm=4.3V, LPYBPY=1, PDTST=1, Fclk(FDSP/N)=40MHz SELTE=1 SELTE=0	-30 V_{ofs1}-5		30 V_{ofs1}+5	mV mV
Decision Directed P.D. Yn,Yn-1 Gain	DDPD_YN_GAIN DDPD_YN-1_GAIN	V_{Rlowz}-V_{Rfsr}=+/-.2V, Vcm=4.3V, LPYBPY=1, PDTST=1, Fclk(FDSP/N)=40 MHz	2.65	3.15	3.65	V/V
Decision Directed P.D. Threshold 100%	VTH100_ 160MV 190MV	V_{cm}=4.3V, LPYBPY=1 PDTST=1. Fclk(FDSP/N)=40 MHz. Measured @ YHB/YLB TP3, Sel=4 V_{Rlowz}-V_{Rfsr}=±0.16 V_{Rlowz}-V_{Rfsr}=±0.19	Vcc-1.2		Vcc-1.2	V V
Decision Directed P.D. Threshold 50%	VTH50_ XPB_P75MV X1_P75MV Xn1_N75MV XPB_P95MV X1_P95MV Xn1_P95MV X1_N95MV Xn1_N95MV	Vin = V_{Rlowz}-V_{Rfsr}, Vcm=4.3V, LPYBPY=1, PDTST=1 Fclk(FDSP/N)=40 MHz Vin =±+.075 @XPB/XNB TP4, Sel=4 Vin =+.075 @ X1, TP3, Sel=7 Vin =-.075 @ Xn1, TP4, Sel=7 Vin =±+.095 @XPB/XNB TP4,Sel=4 Vin =+.095 @ X1 TP3, Sel=7 Vin =+.095 @ Xn1 TP4, Sel=7 Vin =-.095 @ X1 TP3, Sel=7 Vin =-.095 @ Xn1 TP4, Sel=7	Vcc-1.2 Vcc-1.2 Vcc-1.2		Vcc-1.2 Vcc-1.2 Vcc-1.2 Vcc-1.2 Vcc-1.2	V

Table 236Timing Response (TR) Loop

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Decision Directed P.D. Gain	DDPD_GAIN	V_{Rlowz}-V_{Rfsr}=500mVppd @ 10Mhz, Vcm=4.3V, LPYBPY=1, PDTST=1. Fclk(FDSP/N)=40 MHz. Adjust Clock delay to zero, Timing Error(Te) = Tdzero. Measure Timing Error at Tdzero ±2ns (i.e. ±rad/2). Kpd= [Te(2ns)-Te(-2ns)] V/rad	0.20	0.27	0.34	V/rad
Closed Loop Jitter	σ_F	TRVCO output, sample size=100,000 samples		100		ps

k_I is 3.98MHz/mA
K_{fsf} is the value of the Data Rate DAC word, [0 to31]
K_{pmult} is the value of the Damping Ratio DAC word, [0 to127]
I_{REF} is the reference current being sunk from pin RR in µA, $I_{REF}=V_{rr}/R_{ext}$

Table 237Pulse Detector

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Locked CTF_norm_ac Voltage	VFA_AGC	Measure CTF_norm_ac V_{DI} = 100mV_{ppd}, f_{in} = 10 MHz	450		750	mV
Comparator Threshold Percent of VFA_AGC	LPFB=1, V_{IN} = V_{RLOWZ} = V_{RFSR}, V_{CM} = V_{CC} - 1.4 V. Vary V_{IN} (dc voltage), observe LP/LN = RDS output, TSEL = 0 for transition.					
	VTHN0 VTHN1 VTHN2 VTHN4 VTHN8 VTHN16 VTHN32	DVTH = 0, NVTH = 0 DVTH = 0, NVTH = 1 DVTH = 0, NVTH = 2 DVTH = 0, NVTH = 4 DVTH = 0, NVTH = 8 DVTH = 0, NVTH = 16 DVTH = 0, NVTH = 32		20 21.9 23.8 27.6 35.2 50.4 78.9		%
	VTHP0 VTHP1 VTHP2 VTHP4 VTHP8 VTHP16 VTHP32	NVTH = 0, DVTH = 0 NVTH = 0, DVTH = 1 NVTH = 0, DVTH = 2 NVTH = 0, DVTH = 4 NVTH = 0, DVTH = 8 NVTH = 0, DVTH = 16 NVTH = 0, DVTH = 32		20 21.9 23.8 27.6 35.2 50.4 78.9		%
Level Threshold Linearity	Vth_{Lin}	$V_{Thres}(0)$-$V_{Thres}(31)/31$ = LSB Vth_{ideal} = LSB*LTH+$V_{Thres}(0)$ Vth/Vth_{ideal} , LTH=1,2,4,8,16	-1/2		1/2	LSB
RDS Pulse Width	RDS_PW	RDS Output	19	25	31	ns
Pulse Pairing	PULSE_PR	Threshold DAC's set to 0	0		10	ns
RPOL to RDS delay time	RPOL_RDS		-10		10	ns
All dynamic pulse qualifier measurements are performed with a 10 MHz input sine wave unless otherwise specified. Signal amplitudes refer to the signal at the input of the pulse qualifier block (the continuous time filter output).						

TIMING PARAMETERS

AC Characteristics

Recommended operating conditions apply unless otherwise specified. 0°C < T_A < 70°C, 4.5V < VCC < 5.5V

Table 238Servo Demodulator Timing

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SRST Pulse Width	T_{SR}		600			ns
DEMOD Pulse Width	TDMD		150			ns
DEMOD Recovery Time	TREC		150			ns
DEMOD to Corresponding Select Clock Delay	T_{DS}		0			ns
Trailing Edge SRST to SBA-SBD Reset Delay	TR	0.25% of final value [1]	150			ns
Trailing Edge SRST to DEMOD Recovery	TRR		100			ns

[1] Load conditions given below.

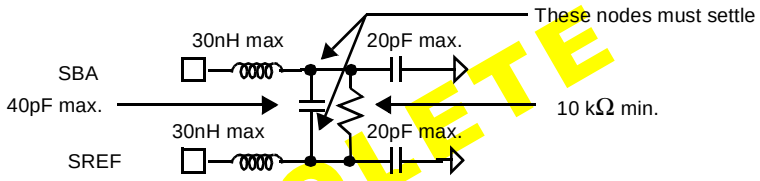


Table 239Servo System Timing

Pins: SG, DEMOD

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSREC Leading Edge to V_{FN} Stable	TFD	V_{FN} stable within 10%			2.3	µs
Trailing Edge of LOWZ to V_{FN} Stable to 10%	TWR	CAGCD value correct			500	ns
Lead, Trailing Edge SG to V_{FN} stable 10%	TGS	CAGCS or D value correct			500	ns
WG Pulse Width (given for reference only)	TWG		1.6			µs

Table 240Write Precompensation Timing

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WPC Delay	T_{wpc}	X = (0.013·K_{wp}+0.20·WPCHR)·T 1&3 X = 0.013·K_{wp}·T Pattern 2	0.9·X		1.1·X	ns
Polarity Asymmetry	T_{PA}	Time difference for 2 pulses that start in one direction vs. 2 pulses that start in the other		100		ps
Jitter				50		ps_{rms}

T is the period of the VCO clock
WPCHR is the WPC high range bit in serial register
K_{wp} is value of the write precompensation DAC word [0 to 15]

Digital Backend I/O

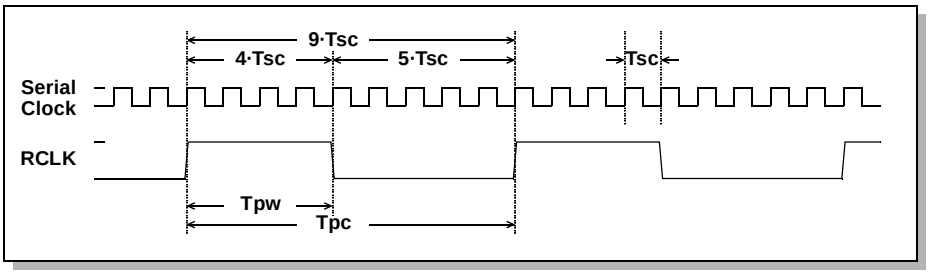


Figure 176 Byte-Wide RCLK with respect to serial clock, Normal

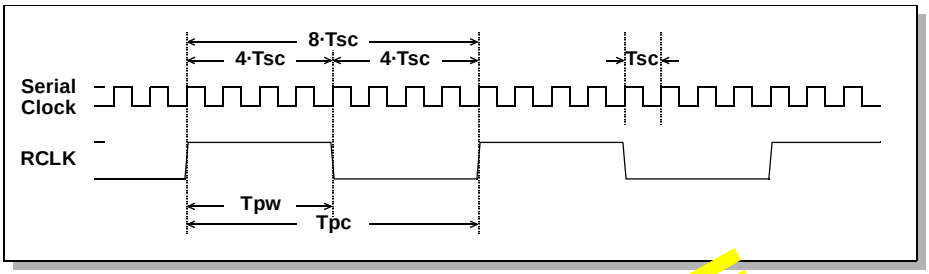


Figure 177 Byte-Wide RCLK with respect to serial clock, Direct Test

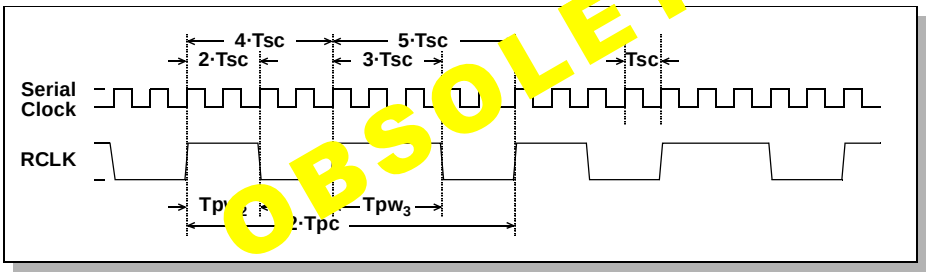


Figure 178 Nibble-Wide RCLK with respect to serial clock, Normal

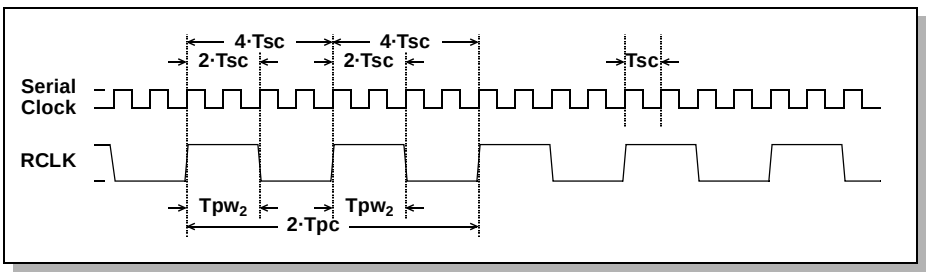


Figure 179 Nibble-Wide RCLK with respect to serial clock, Direct Test

Table 241Digital Backend I/O Timing

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Channel Clock Frequency	f_{chclk} (max)	Data Rate=140Mbit/s	157.5			MHz
Parallel Read Clock Frequency	f_{RCLK} (max)	Control Reg Bit DTM=0; Byte-wide	17.5	$1/9 \cdot f_{chclk}$		MHz
		Control Reg Bit DTM=1; Byte-wide	19.7	$1/8 \cdot f_{chclk}$		MHz
Serial Channel Clock Period	T_{SC} (min)	Data Rate=140Mbit/s			6.35	ns
		Data Rate=180Mbit/s			4.94	ns
Parallel Read Clock Pulse Width	TPW	at 1.5V points; $C_L \leq 15pF$	$4 \cdot T_{SC} - x$		$4 \cdot T_{SC} + x$	ns
	TPW2	at 1.5V points; $C_L \leq 15pF$	$2 \cdot T_{SC} - x$		$2 \cdot T_{SC} + x$	ns
	TPW3	at 1.5V points; $C_L \leq 15pF$	$3 \cdot T_{SC} - x$		$3 \cdot T_{SC} + x$	ns
Parallel Read Clock Period	T_{PC}	Byte-wide, Normal Operation	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	ns
		Byte-wide, Direct Test	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	ns
	$2 \cdot T_{PC}$	Nibble-wide, Normal Operation	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	ns
		Nibble-wide, Direct Test	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	ns
Control Signal rise and fall times	t_{CS}	20% to 80%			< 10 >	ns
Recovery time Powerdown to fully functional	t_{REC}				<TBD>	ns

Parallel Write Timing

Pins: WG, WCLK or RCLK, NRZ[8:1] or NRZ[4:1]

Timing Diagrams:

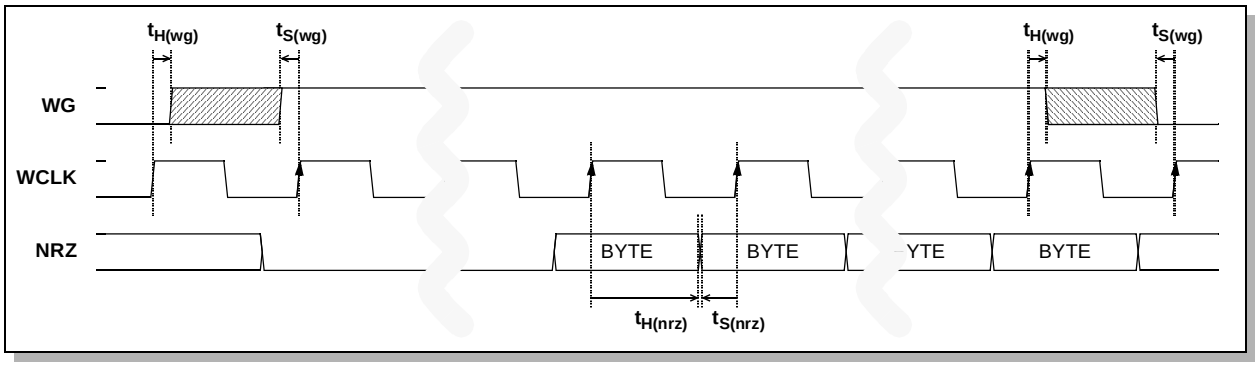


Figure 180 Parallel Write Timing: WCLK, Byte-Wide

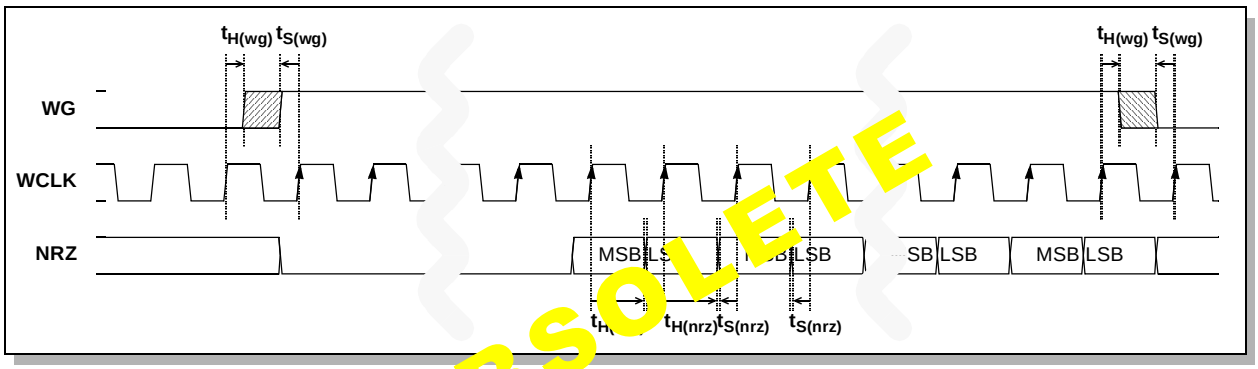


Figure 181 Parallel Write Timing: WCLK, Byte-Wide

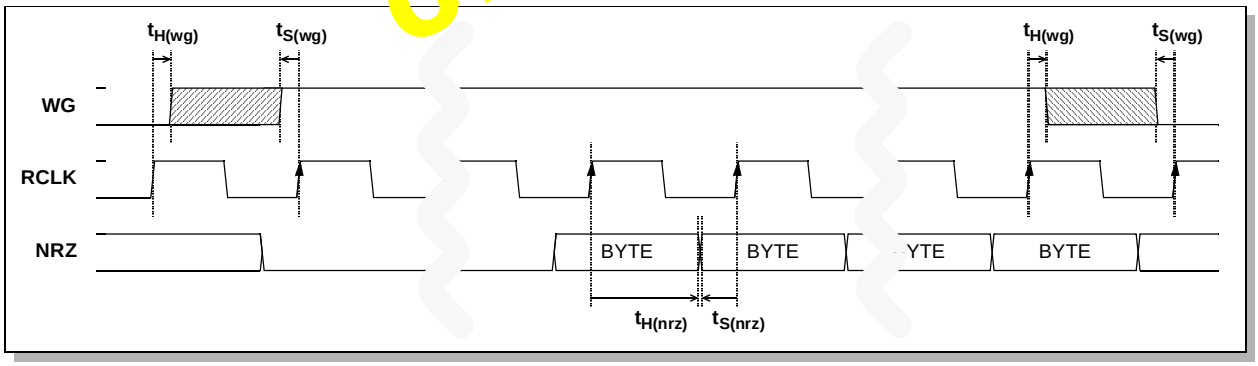


Figure 182 Parallel Write Timing: RCLK Rising Edge, Byte-Wide

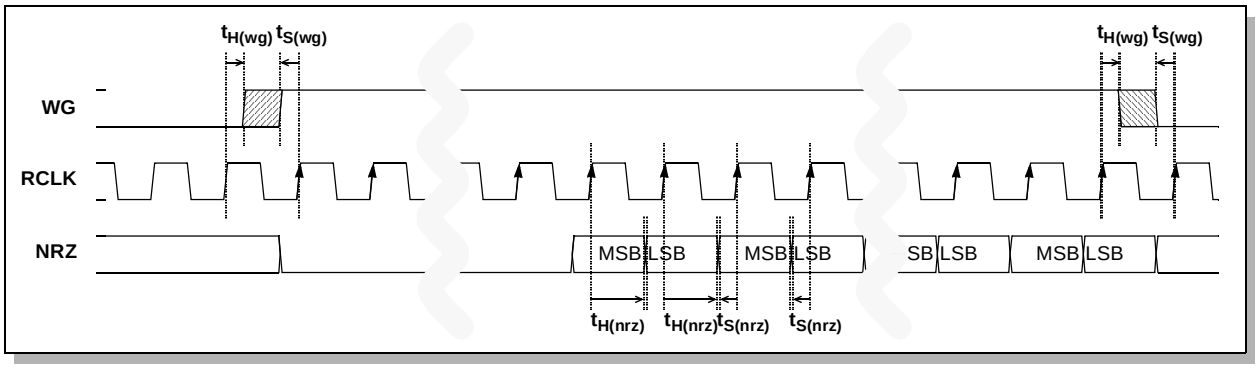


Figure 183 Parallel Write Timing: RCLK Rising Edge, Nibble-Wide

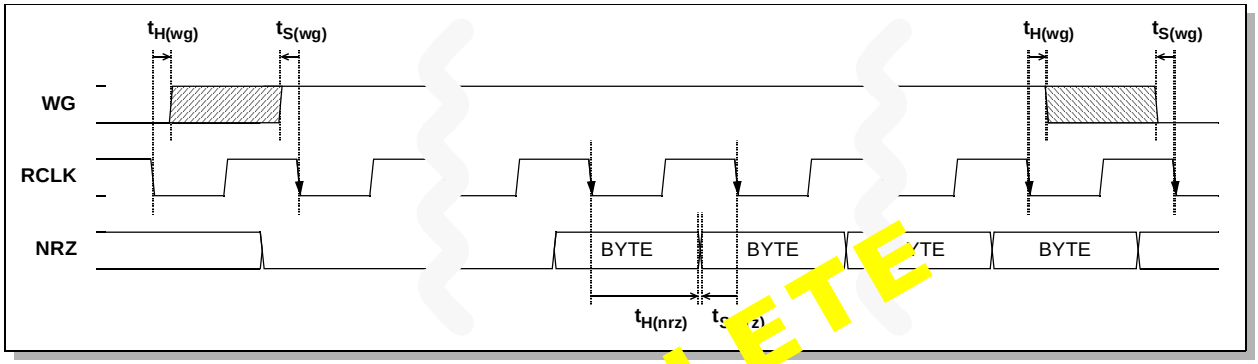


Figure 184 Parallel Write Timing: RCLK Falling Edge, Byte-Wide

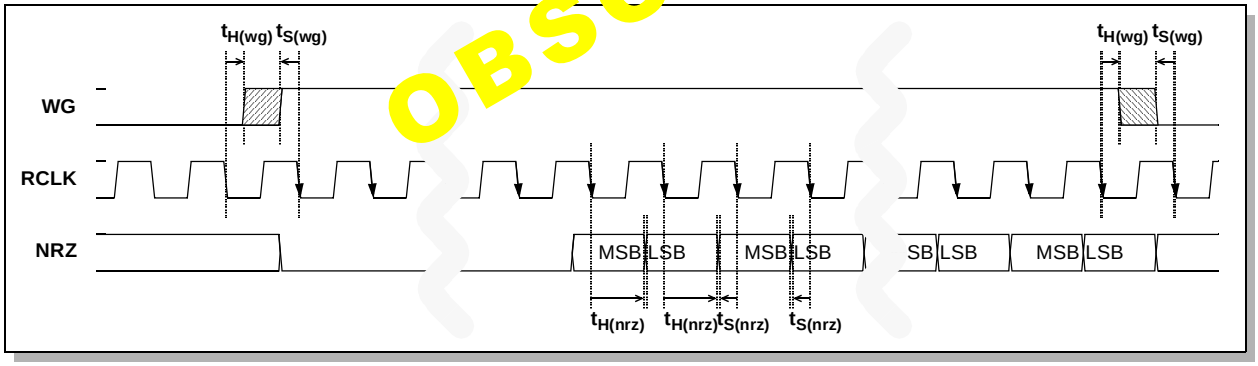


Figure 185 Parallel Write Timing: RCLK Falling Edge, Nibble-Wide

Table 242Parallel Write Timing

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WG Hold Time	tH(wg)	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
WG Setup Time	tS(wg)	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
NRZ Hold Time	tH(nrz)	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
NRZ Setup Time	tS(nrz)	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
$\overline{WM}$ time prior to WM	t $\overline{WM}$	$\overline{WM}$ = Idle mode or Read mode	<TBD>			ns

Parallel Read

Pins: RG, RCLK, SBF, NRZ[8:1] or NRZ[4:1]

Timing Diagrams:

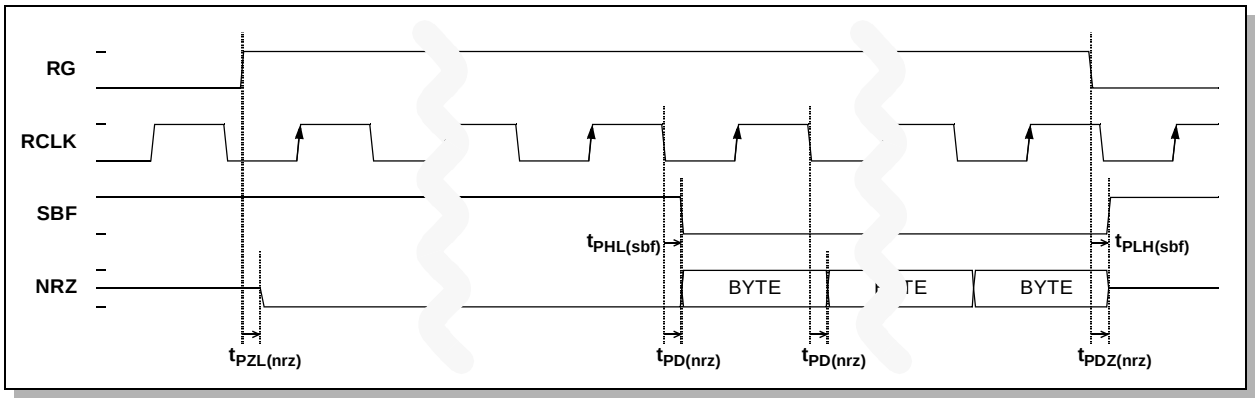


Figure 186 Parallel Read Timing: Byte-Wide

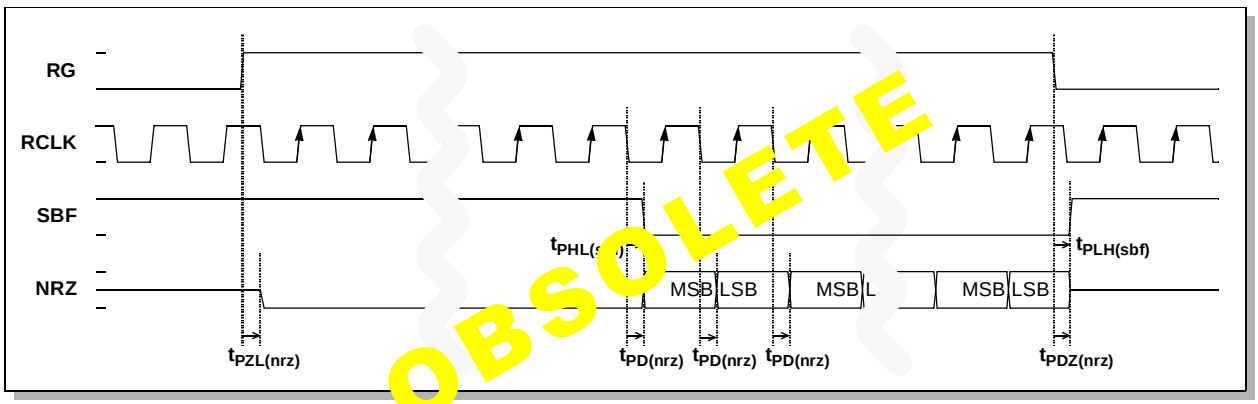


Figure 187 Parallel Read Timing: Nibble-Wide

Table 243Parallel Read Timing

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RCLK to SBF falling	tPHL(sbf)	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to SBF rising	tPLH(sbf)	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to NRZ enabled	tPZL(nrz)	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RCLK to NRZ change	tPD(nrz)	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to NRZ disabled	tPDZ(nrz)	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
$\overline{RM}$ time prior to RM	t $\overline{RM}$	$\overline{RM}$ = Idle mode or Write mode	<TBD>			ns

SERIAL INTERFACE TIMING

Table 244Serial Interface Timing

PARAMETER	*SYM*		*MIN*	*TYP*	*MAX*	*UNITS*
SPCLK period	T		50			ns
SPEN set-up time	$T_{S(SPEN)}$	Relative to SPCLK ↑	40			ns
SPEN hold time	$T_{H(SPEN)}$	Relative to SPCLK ↑	50			ns
SPEN hi to low to hi (Time between successive operations)	T		50			ns
SPDATA set-up time	$T_{S(SPDATA)}$	Relative to SPCLK ↑	20			ns
SPDATA hold time	$T_{H(SPDATA)}$	Relative to SPCLK ↑	5			ns
SPDATA enable	T_{OEN}	Relative to SPCLK ↓	5			ns
SPCLK low time	T_{OCLK}	Relative to SPCLK ↓	30			ns
SPDATA disable	T_{ODIS}	Relative to SPEN ↓			30	ns
Delay to SPDATA output data change	T_{PDD}	Relative to SPCLK ↑			10	ns

4 TAPE DRIVE CIRCUITS

Tape Drive Circuits

VTC Inc.
Value The Customer™

V10619
DUAL CHANNEL, READ-ONLY DIFFERENTIAL PREAMPLIFIER

990812 August 12, 1999

FEATURES

- *General*
  - Single Power Supply, 5V ±10%
  - Very Low Power Dissipation
  - Head Inductance 0.2 - 1 µH
  - 8 Ohms maximum output resistance
  - 14 pin VSOP package
- *High Performance Reader*
  - Read Gain = 350 V/V Typical
  - Input Noise = 0.54nV/√Hz Typical

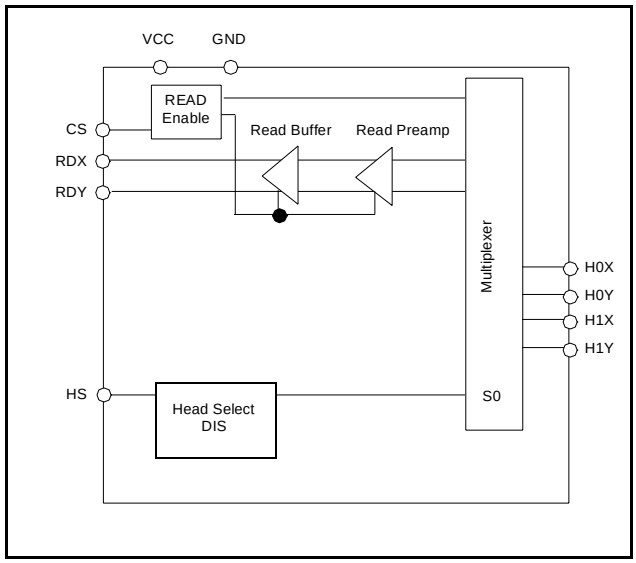
ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Input Voltages:
Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V
Output Current:
RDX, RDY: I_O ..... -25mA
Junction Temperature ..... 150°C
Storage Temperature, Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
14-lead VSOP ..... 120°C/W
10-ball CBGA ..... 70 °C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Head Inductance, L_H ..... 0.2 to 1µH
Junction Temperature, T_J ..... 25°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

The V10619 addresses up to two, two-terminal inductive heads and provides read amplification. Read Mode enable is accomplished with the $\overline{CS}$ pin as shown in Table 245. Head selection is accomplished with the HS pin as shown in Table 246.

An internal pull-up resistor provided on the $\overline{CS}$ pin disables the device if the control line is opened accidentally.

Table 245Mode Select

CS	*MODE*
0	Read
1	Sleep

Table 246Head Selection

HS	*HEAD*
0	0
1	1

Read Mode

The read mode configures the V10619 as a low-noise differential amplifier. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load.

Note: The RDX, RDY common-mode voltage is not maintained in the sleep mode.

Sleep Mode

In sleep mode ($\overline{CS}$ high), most of the circuit is idle and power dissipation is reduced to 3mW typical.

TAPE DRIVE CIRCUITS

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
VCC Supply Current	I_{CC}	Read Mode		27	40	mA
		Sleep Mode		0.5	3	
Power Supply Power Dissipation	PD	Read Mode		110	220	mW
		Sleep Mode		2.5	16.5	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP[1]	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	300	350	400	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	50	100		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p		80		
Group Delay Deviation	GDD	Over frequency range from DC to -1dB, L_H = 0, R_H = 0 (-0.5 dB as the reference)	-150		150	ps
Input Noise Voltage	e_{in}	BW = 20MHz, L_H = 0, R_H = 0		0.54	0.65	nV/√Hz
Input Noise Current	i_{in}			3.7	4.5	pA/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 20-80MHz		4.6	7	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 20-80MHz	920	1700		Ω
Dynamic Range Gain Linearity	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mV P-P
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	65			dB
Output Offset Voltage	V_{OS}	Steady state read	-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.8		V
Single Ended Output Resistance	R_{OUT}	f = 5 MHz			8	Ω
Output Current	I_O	AC-coupled load, RDX to RDY	–1		+1	mA

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

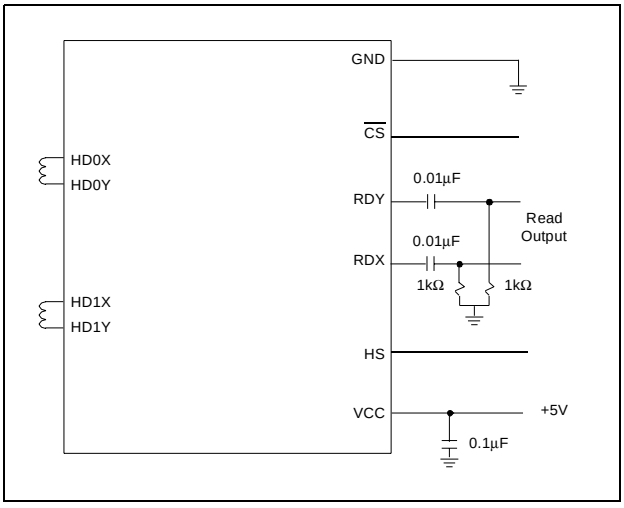
SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified; f_{DATA} = 5MHz, L_H = 0.54µH, R_H = 20Ω, C_L (RDX, RDY) ≤ 20pF.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP[1]*	*MAX*	*UNITS*
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of 100mV, 10MHz read signal envelope			0.6	µs
HS0 - HS1 Head-Head Delay	t_{HS}	HS0 - HS1 to 90% of 100mV, 10MHz read signal envelope			0.6	µs

1. Typical values are given at V_{CC} = 5V and T_A = 25°C.

TYPICAL APPLICATION CONNECTIONS



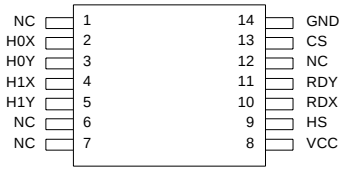
Note: The pin placements in the diagram are tentative. The connections shown apply regardless of package variation.

Application Note:

- For maximum stability, place the decoupling capacitors as close to the package pins as possible.

V10619

2-CHANNEL CONNECTION DIAGRAM



2-Channel
14-lead VSOP
V10619VSA1

Specific Characteristics

See the general data sheet for common specification information.

PIN FUNCTIONS AND DESCRIPTION LIST

Name	*I/O*	*Description*
$\overline{CS}$	I	Chip Select: A high level signal puts chip in sleep mode A low level puts chip in READ mode
GND		Ground
HS	I [1]	Head Select: Selects one of two heads
HnX	I/O	X Head Terminals
HnY	I/O	Y Head Terminals
RDX-RDY	O [1]	Read Data Output: Differential output data
VCC		+5 volt supply

1. May be wire-OR'ed for multi-chip usage.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

VTC Inc.
Value The Customer™

VT5204

2-CHANNEL, HIGH-PERFORMANCE, INDUCTIVELY COUPLED FERRITE HEAD, READ/WRITE PREAMPLIFIER

990812 August 12, 1999

FEATURES

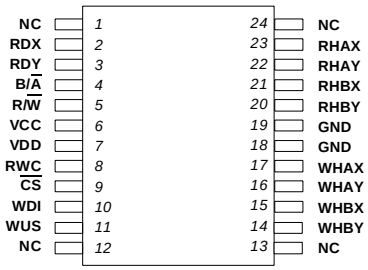
- High Performance
  - Rise/Fall Times = 8.5 ns Typical into 2.3 µH Head
  - Input Capacitance = 8 pF Typical
  - Input Noise = 0.72 nV/√Hz Typical
  - Head Inductance Range = 1 – 7 µH
  - Voltage Gain = 240 or 375 V/V
- TTL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- Options Available:
  - WDFF on the Write Data Inputs Connected or Disconnected
  - Open Collector or Emitter Follower Output in Read Mode
  - With or Without Switchable Damping Resistor

DESCRIPTION

The VT5204 is a high-performance, integrated read/write preamplifier designed for a helical-scan head which is coupled to the circuit by an inductive transformer. The VT5204 has eight head pins which connect to two read heads and two write heads. The circuit has one input which allows analog control of the write current for the selected write head and two digital inputs which allow selection of write/read mode and A/B channel.

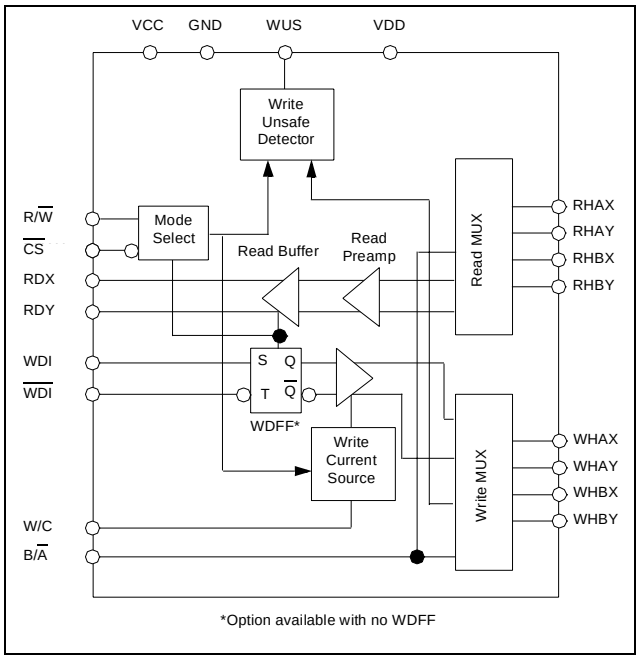
The VT5204 circuit is powered by a +12/+5VDC supplies. The circuit is designed to have a power supply fault detect circuit which shuts off write current in the event the power supply level drops below a unsafe threshold. This protects the data on the media from potential transients. If a line should open up, the mode select lines will be forced into a high state to prevent the device from affecting data recorded on the media.

CONNECTION DIAGRAM



2-Channel
24-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 35mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Read Head Port Voltage V_{RH} ..... -0.3V to (V_{CC} + 0.3)V
- Write Head Port Voltage V_{WH} ..... -0.3V to (V_{CC} + TBD)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O ..... -10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 24-lead SOIC ..... 90°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} ..... 12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

S

TAPE DRIVE CIRCUITS

CIRCUIT OPERATION

The VT5204 addresses the head selected by the digital inputs providing write drive or read amplification. Head selection and mode control are accomplished with pins B/$\overline{A}$, R/$\overline{W}$, and $\overline{CS}$. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VT5204 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current flows into the "X" head port when WDI is a logical "1" and flows into the "Y" head port when WDI is a logical "0".

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (± 8%) is:

$$IW = 50/RWC \pm 0.5\ mA \qquad (eq.\ 202)$$

(mA, 0-pk, RWC in k¾)

In programmable write current applications, the proper write current level can be selected by using a current DAC or by selecting different resistor values using analog switches or MOS gates. The magnitude of the write current can also be calculated as:

$$IW = 20 * IWC \qquad (eq.\ 203)$$

(mA, 0-pk, IWC is programmed value in mA)

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VT5204 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load.

The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode. This substantially reduces the recovery time delay when switching between write mode and read mode.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 16mW for a sleep mode.

Table 247: Head Select

B/$\overline{A}$	*HEAD*
0	A
1	B

PIN DESCRIPTIONS

NAME	*#*	*DESCRIPTION*
NC	1	No connect (or ground)
RDX	2	Read amplifier multiplexed differential output (X)
RDY	3	Read amplifier multiplexed differential output (Y)
B/$\overline{A}$	4	TTL Digital Control: switches between A and B channels
R/$\overline{W}$	5	TTL Digital Control: switches between write and read modes
VCC	6	+5V DC power supply input
VDD	7	+12V DC power supply input
WC	8	Output write current control reference (I_{WC} = 20 * I_{WC})
$\overline{CS}$	9	Chip Select: $\overline{CS}$ ='0', normal operation; $\overline{CS}$ ='1', enables low power mode
WDI	10	TTL Digital Write Data: WDI = '1' I_W into WHX pin
WUS	11	Write unsafe (flags improper write conditions)
NC	12	No connect (or ground)
NC	13	No connect (or ground)
WHBY	14	Write head channel B, Y output
WHBX	15	Write head channel B, X output
WHAY	16	Write head channel A, Y output
WHAX	17	Write head channel A, X output
GND	18	Ground
GND	19	Ground
RHBY	20	Read head channel B, Y input
RHBX	21	Read head channel B, X input
RHAY	22	Read head channel A, Y input
RHAX	23	Read head channel A, X input
NC	24	No connect (or ground)

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DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	I_{CC}	Read Mode		33.5	50	mA
		Write Mode		24	35	
		Idle Mode		2.0	4.0	
VDD Supply Current	I_{DD}	Read Mode		0.5	1.0	mA
		Write Mode		8 + I_W	20 + I_W	
		Idle Mode		0.5	1.5	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		173	262	mW
		Write Mode: I_W = 20mA		456	655	
		Idle Mode		16	38	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-100			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.0	9.6	10.5	V
VCC Fault Voltage	V_{CCF}		3.5	3.9	4.5	V
Write Head Current	I_H	Write protect mode, power supply fault or non-selected head	-200		+200	µA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply: C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.
Input source (head), impedance is L_H (typical) = 5µH, L_H (minimum) = 1µH, R_H < 1Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	206	240	274	V/V
			322	375	428	
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	25	40		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	40	65		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.72	1	nV/ÐHz
Input Noise Current	I_{IN}			1.8		pA/ÐHz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		8	11	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (T_A = 25°C)	1000	3000		Ω

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply: C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ. Input source (head), impedance is L_H (typical) = 5µH, L_H (minimum) = 1µH, R_H < 1Ω.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Range	DR	AC input voltage where the gain falls to 90%, A_V @ V_{IN} = 0.2mVrms, f = 5MHz	2	4		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = V_{CC} + 100mVp-p @ f = 5MHz	50	75		dB
Power Supply Rejection Ratio	PSRR	100mVp-p, f = 5MHz on V_{DD} or V_{CC}	45	75		dB
Channel Separation	CS	Unselected channel V_{IN} = 100mVp-p, f = 5MHz, V_{IN} = 0mVp-p selected	45	60		dB
Output Offset Voltage	V_{OS}		-215		215	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		V
		Write Mode		V_{CC} - 2.7		
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		15	35	Ω
Output Current	I_O	AC coupled load	-1.5		1.5	mA

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply: I_W = 20mA, L_H = 2.3µH, R_H = 1Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		VDC
Write Current Voltage	V_{DH}	I_{WC} = 35mA		19		V
Unselected Head Write Current	I_{UH}			0.8	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			5		pF
Differential Output Resistance	R_{OUT}	Internal damping resistance @ 2.5kΩ		1.5		kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	350			kHz
Write Current Range	I_W	1430Ω< R_{WC} < 10kΩ	5		35	mA
Write Current ERR	I_{ERR}	I_W range 5mA to 35mAo-p	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 188)

Unless otherwise specified, recommended operating conditions apply: I_W = 20mA, L_H = 2.3µH, R_H = 1Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	Delay to 90% I_W		75	300	ns
Write to Read Mode	t_{WR}	Delay to 90% I_W or to 90% of 100mVp-p output @ 10MHz			600	ns
$\overline{CS}$ to Select	t_{IR}	Delay to 10% I_W			600	ns
$\overline{CS}$ to Unselect	t_{IW}	Delay to 90%, 100mVp-p output @ 10MHz		100	600	ns
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns

SWITCHING CHARACTERISTICS (see Figure 188)

Unless otherwise specified, recommended operating conditions apply: I_W = 20mA, L_H = 2.3µH, R_H = 1Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Asymmetry	A_{SYM}	Duty cycle 50% WDI, 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	L_H = 2.3µH, R_H = 1Ω, internal damping resistance 2.5kΩ		8.5	11.0	ns
Output Current Rise/Fall Time	t_r/t_f	L_H = 0µH, R_H = Ω		2	5	ns

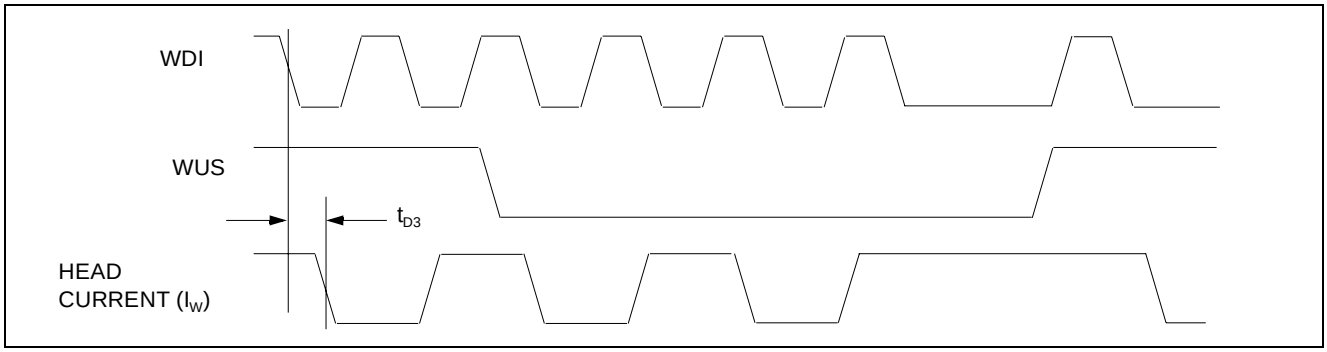


Figure 188 Write Mode Timing Diagram

Power Control Circuits

VTC Inc.
Value The Customer™

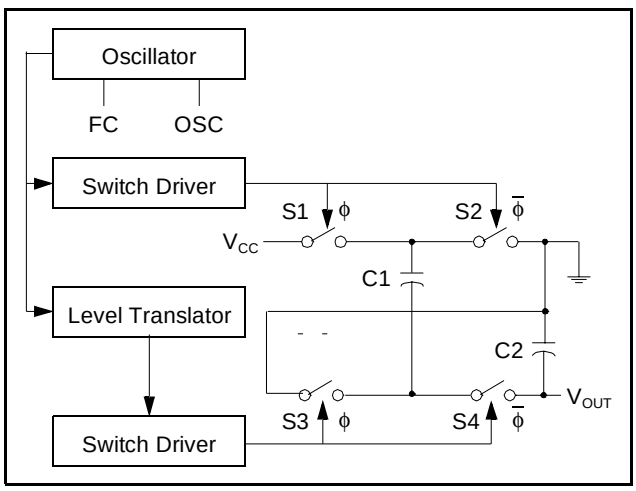
VC4005
+5 VOLT TO -5 VOLT DC VOLTAGE CONVERTER

990812 **ADVANCE INFORMATION** August 12, 1999

FEATURES

- *General*
  - 8 pin SOIC package
  - Inverts input supply voltage (+3V - +5.5V)
  - Very low power dissipation
  - 200mA supply current capability @ R_{OUT} = 3.5Ω
  - High efficiency conversion factor (Typically 85% @ 200mA with V_{IN} = +5.0V)
  - 3Ω typical output resistance
- *Applications*
  - Disk drives utilizing dual-supply preamps
  - Laptop computers
  - Dual supply op-amp power supplies
  - Interface power supplies
  - Medical instruments
  - Cellular phones

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Voltages:
V_{IN} ..... -0.3V to 7V
Junction Temperature ..... 150°C
Storage Temperature, Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
8-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Input Voltages:
V_{IN} ..... +3V to +5.5V
Switch Capacitors ..... see page 6
Junction Temperature, T_J ..... 25°C to 125°C

CIRCUIT OPERATION

The VC4005 is a high efficiency, switched capacitor voltage converter which inverts the voltage on V_{IN} (+3V to +5.5V) to V_{OUT}. It is capable of 200mA of supply current for applications requiring higher than standard currents such as dual supply preamps for hard disk drives. The VC4005 is also suitable for other dual supply applications such as those listed above. The VC4005 is available with various switch frequencies to best suit the application

Operational Mode

The VC4005 contains four large CMOS switches (S1 - S4) which invert the input supply voltage by switching in a specific sequence. Energy transfer and storage are provided by external capacitors as shown in “Typical Applications” on page 5.

The voltage conversion sequence has two distinct steps:

38) When S1 and S3 are closed, C1 charges to supply voltage V+. S2 and S4 are open during this time interval.

39) When S2 and S4 are closed, C1 charges C2. S1 and S3 are open during this time interval

After several cycles, the voltage across C2 rises to V+.

The output at the cathode of C2 equals -(V+) because the anode of C2 is connected to ground (assuming no load on C2, no loss in the switches, and no ESR in the capacitors). The charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the equivalent series resistance (ESR) of the capacitors.

PIN FUNCTION LIST AND DESCRIPTION

NAME	*I/O*	*DESCRIPTION*
V_{IN}	I	Input voltage to be inverted.
V_{OUT}	O	Output voltage (C2 positive connection)
FC	I	Frequency control: • FC = open, f_{OSC} = 200 kHz. • FC = +V, f_{OSC} = 400 kHz. • FC has no effect when OSC pin is driven externally. • FC must be tied either high or low during operation
CAP +	I/O	C1 positive connection
GND		Power ground
CAP -	I/O	C1 negative connection
OSC	I	Oscillator control input: • Internal 15 pF capacitor. • Connect an external capacitor to ground to lower switching frequency. • Drive with external oscillator to adjust switching frequency.
LV	I	Logic ground

POWER CONTROL PRODUCTS

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	R_L = 1KΩ	3.0	5.0	5.5	V
Power Supply Power Dissipation		Operational Mode		56	**TBD**	mW
Supply Current	I_Q	No Load		3.5	11	mA
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = V_{IN}$			80	µA
Input Low Current	I_{IL}	V_{IL} = 0 V	-160			µA

NORMAL OPERATION CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

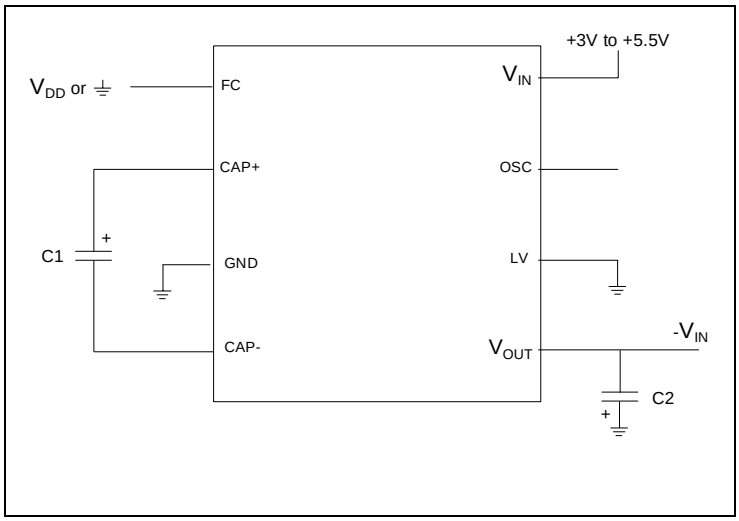
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Output Resistance	R_{OUT}[1]	I_L = 200 mA		3.5	8	Ω
Output Current	I_O	$V_{OUT} \geq -V_{IN}$	200			mA
Oscillator Frequency	F_{OSC}	OSC open, FC = GND	TBD	200		KHz
		OSC open, FC = $+V_{IN}$	TBD	400		
Oscillator Input Current	I_{OSC}	f = 200 kHZ	TBD	+15		µA
		f = 400 kHz	TBD	±30		
Power Efficiency	P_{EFF}	R_L = 500Ω between +V and OUT I_L = 200mA to GND V_{IN} = +5.0 V	TBD TBD	96 86		%
Voltage Conversion Efficiency	V_{CEFF}	No Load	TBD	99		%

1. R_{OUT} includes internal switch resistance and capacitor ESR.

POWER CONTROL PRODUCTS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

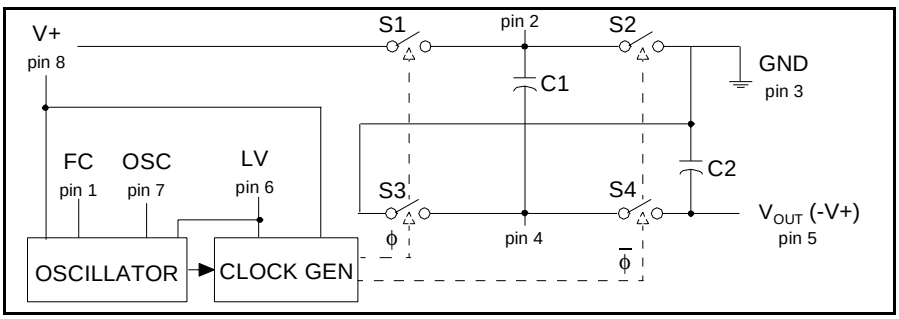
TYPICAL APPLICATION CONNECTIONS



The approximate output of this circuit can be characterized as an ideal voltage source in series with a resistor. The voltage source equals -(V+). The output resistance R_{OUT} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C1 and C2. Since the switching current charging and discharging C1 is approximately twice the output current, the effect of the ESR of the pumping capacitor C1 is multiplied by four in the output resistance. The output capacitor C2 is charging and discharging at a current approximately equal to the output current, therefore its ESR only counts once in the output resistance. A mathematical approximation is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2}$$

Note: R_{SW} is the sum of the ON resistance of the internal MOS switches shown below.



High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the 2/(f_{OSC} x C1) term. Once this term is trivial compared with R_{SW} and the ESRs, further increase of the oscillator frequency and capacitance becomes ineffective.

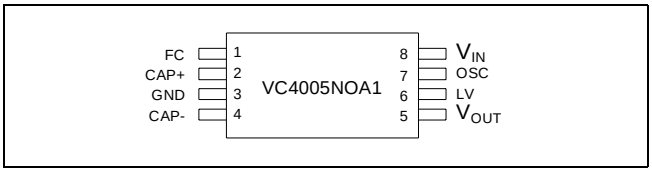
The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C2.

$$V_{ripple} = \frac{I_{Load}}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2}$$

Note: Use of a low ESR capacitor reduces voltage ripple.

PIN ASSIGNMENTS

VC4005 8-lead SOIC



Specific Characteristics

See the general data sheet for common specification information.

NOTES

76) To achieve maximum frequency (400/200 KHz) minimize parasitic capacitance on the oscillator input by *not* bonding-out the oscillator pin.

77) To turn off the converter, drive the oscillator pin to GND or V_{CC}.

78) Use of 10µF, low equivalent series resistance (ESR) capacitors are suggested for C1 and C2. Suppliers/products include:

Supplier [1]	***Part No.***	***Type***	***Value***
Murata	GRM230 Y5V 475 Z16	Ceramic	4.7 µF
	GRM235 Y5V 685 Z16		6.8 µF
	GRM235 Y5V 106 Z16		10.0 µF
	GRM235 Y5V 226 Z10		22.0 µF
Taiyo Yuden	LMK316 BJ 335 ML	Ceramic	3.3 µF
	LMK316 BJ 475 ML		4.7 µF
	JMK316 BJ 106 ML		10.0 µF
	LMK325 F 226 ZN		22.0 µF
AVX	TPSC226 * 016 # 0375	Tantalum	22.0 µF
	TPSC336 * 016 # 0300		33.0 µF
	TPSC476 * 016 # 0350		47.0 µF
	TPSC476 * 016 # 0250		47.0 µF
Sprague	593D335X 035C20	Tantalum	3.3 µF
	593D475X 035C20		4.7 µF
	593D685X 035C20		6.8 µF
	593D106X 035C20		10.0 µF
	593D226X 035C20		22.0 µF
	593D476X 010C20		47.0 µF

1. Supplier telephone numbers are: Murata 800-831-9172, Taiyo Yuden 800-348-2496, AVX 803-448-9411, Sprague 207-324-414.

For best performance, place the capacitors as close as possible to the VC4005. The resistance of the printed circuit board (PCB) will add to the ESR of the capacitors, which reduces the output voltage and efficiency of the VC4005.

79) The test circuit contains capacitors C1 (**TBD**µF) and C2 (**TBD**µF) and ESR (**TBD**). Capacitors with higher ESR will increase the output resistance, which decreases the output voltage and efficiency of the VC4005.

6 APPLICATION NOTES

Application Notes

PHASE LOCK LOOP APPLICATION FUNDAMENTALS FOR DISK DRIVES

990812 **APPLICATION NOTE** August 12, 1999

SUMMARY

Phase-locked loops (PLLs) are widely used in disk drives to recover the READ clock and to generate the WRITE clock at a variety of frequencies as needed for zoned-density recording. Such PLLs have off-chip components such as capacitors and resistors as well as on-chip registers (for division ratios, DAC inputs, etc.), which allow performance to be tailored to a given set of requirements. This application note describes typical PLLs in hard disk drives, how to select external components and internal register values, and the trade-offs and optimizations that a user will need to understand when designing with PLLs.

INTRODUCTION

The reading of data from a disk drive is an asynchronous operation. The rotation of the disk is not synchronized with the system clock and the pulse peaks representing flux reversals can have any phase with respect to the system clock. It is necessary to extract a read clock from the data itself. The read clock establishes the timing of proper bit-cell boundaries, and is used to determine the bit value (0 or 1) within each read-data window. Read clock extraction is done using a phase-locked loop which employs negative feedback to force a voltage-controlled oscillator (VCO) to be in synchronism with the read signal.

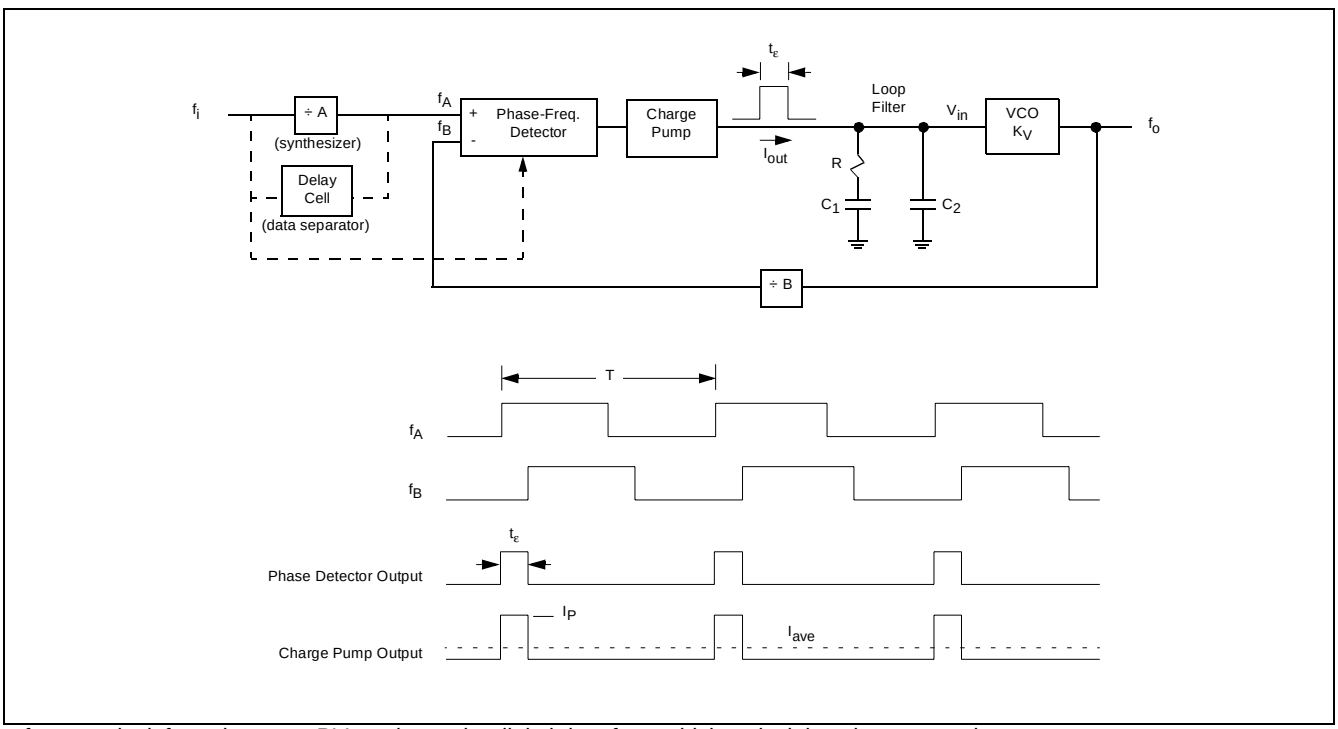
Most disk drives use zoned-density recording (ZDR) today. The disk rotation rate is fixed, but a higher data frequency is used near the outer diameter (OD) than at the inner diameter (ID) such that the physical width of a bit cell is kept approximately the same over the whole disk area. A zone is defined between two radii r_1 and r_2, and a typical drive will have from four to twenty zones in all. The write frequency is constant within a given zone. This requires different write frequencies be generated in each zone. For this purpose a type of phase-locked loop called a frequency synthesizer is used to derive multiple output frequencies from a single input frequency.

This report describes phase-locked loops in the form commonly used in disk drives, and includes a systematic mathematical analysis of PLL loop dynamics in both the time and frequency domain. Then two types of applications are described (data separators/synchronizers and frequency synthesizers); the selection of the user-specified parameters (capacitors, resistors, divider ratios, etc.) is discussed in terms of the performance objectives for each device.

The scope of this application note is limited to the common concerns of disk drive designers. Phase-locked loops are a large subject and several excellent texts exist which cover details beyond the scope of this report. References can be found at the end of this report.

PLL BASICS: TIME DOMAIN

Figure 1 shows a generic phase-locked loop with a lead/lag loop filter (R, C_1, C_2). The input frequency is f_i and the output frequency is f_o. f_o is locked to have some exact ratio to f_i. The input may be a crystal-controlled reference frequency, a



reference clock from the servo PLL, or it may be digital data from which a clock is to be extracted.

Figure 1 General model for a charge-pump phase-locked loop with a lead/lag loop filter

For a Frequency Synthesizer:

In a frequency synthesizer, the input frequency is divided by A, which is an integer, using a digital frequency divider. This produces a frequency f_A at the positive input to the phase-frequency detector.

$$f_A = \frac{f_i}{A} \quad \textit{(eq. 1)}$$

The VCO output frequency is similarly divided by an integer B, producing a frequency f_B, which is fed into the negative input of the phase-frequency detector.

$$f_B = \frac{f_o}{B} \quad \textit{(eq. 2)}$$

The phase-frequency detector puts out a string of pulses with a width t_ε, equal to the time difference between the rising edges of f_A and f_B, which is fed into the charge pump. The charge pump puts out a similar string of current pulses of width t_ε and amplitude I_p which are fed into the loop filter. The current pulses can be positive or negative depending on the phase relation between f_A and f_B. This current is averaged over many cycles by the loop filter capacitors. Thus, in the steady state (or locked) condition where time periods are long compared to $T = 1/f_A = 1/f_B$, we can represent the current by its average value:

$$I_{ave} = I_p\left(\frac{\tau_\varepsilon}{T}\right) \quad \textit{(eq. 3)}$$

The value of I_p is user-controlled in most cases. The loop filter stores the charge pumped by the charge pump on capacitors C_1 and C_2 (ordinarily $C_1 >> C_2$) and in the steady state, produces a voltage V_{in} given approximately by:

$$V_{in} = \left(\frac{1}{C_1}\right)\int I_{ave}\,dt \quad \textit{(eq. 4)}$$

Note that in this simplified discussion we treat the filter as a capacitor (neglecting R and C_2). In a real PLL, the resistor R is used to put a zero into the transfer characteristics which improves stability. If the loop had only R and C_1 the stability would be OK, but the pump current would produce a very large instantaneous voltage drop across R putting a voltage spike into the VCO and causing problems. Capacitor C_2 is added to reduce these voltage spikes.

Thus, the VCO converts its input voltage V_{in}, to an output frequency f_o with a transfer gain of K_V given by:

$$f_o = K_V V_{in} \quad \textit{(eq. 5)}$$

The output frequency f_o is divided by B to complete the loop. This arrangement can be thought of as a negative feedback scheme. The phase-frequency detector produces an error signal proportional to the phase difference between f_A and f_B. The loop filter and VCO are connected so as to force f_A and f_B to be in phase. With ideal components, the phase difference is forced to exactly zero.

To get a better understanding of the situation consider the case where f_A and f_B are out of phase, with f_A leading f_B, as shown in the timing diagram of Figure 1. The phase-frequency detector output turns on the charge pump for a time t_ε pumping a charge Q_ϕ into the loop filter with a value of:

$$Q_\phi = I_p t_\varepsilon \quad \textit{(eq. 6)}$$

This charge increases the voltage at V_{in} by:

$$\Delta V = \frac{Q\phi}{C1} \quad (C_1 >> C_2) \quad \textit{(eq. 7)}$$

and f_o will increase by:

$$\Delta f = K_V \Delta V_{in} \quad \textit{(eq. 8)}$$

With the frequency increasing, the rising edges of f_B will now occur earlier in time. This causes the next t_ε pulse to be shorter and the process continues until $t_\varepsilon = 0$ (at which point f_A and f_B are in phase), $I_{ave} = 0$, and V_{in} is constant in time. A similar argument can be made if f_A lags f_B. Since f_A and f_B are equal in phase and frequency:

$$f_o = \left(\frac{B}{A}\right) f_i \quad \textit{(eq. 9)}$$

This is the basic frequency synthesizer equation. A very large number of output frequencies can be produced by simply changing the frequency division ratios A and B.

For a Data Separator:

The model presented above can represent a data separator (data synchronizer) PLL if we set B to 1 and replace the divide-by-A block with a delay cell (as shown with dashed lines in Figure 1).

The input to a frequency synthesizer is always a square wave and the loop will align every “Ath” data input edge with every “Bth” VCO edge. In a data separator the data input is no longer a square wave but a data stream where logic 1's are represented by the leading edge of positive pulses and logic 0's are represented by a flat ‘0’ level with no edges. The delay cell allows the phase/frequency detector to be activated on the rising edge of the input, comparing the edge of the VCO with that of the delayed data edge. The phase/frequency detector is said to operate in “phase only” mode with this method. This allows the loop to update only when necessary, and only when reading 1's. Otherwise the loop would try and align each edge of the VCO with each edge of the data, which would lead to a huge frequency error in the VCO.

Since the loop now updates only when logic 1's are read, if a long string of 0's occurs in the data the loop will never update and possibly drift in frequency. Because of this fact, run-length limited (RLL) codes are used where the number of consecutive 0's in the data is limited. For (1,7) code there must be at least one 0 separating 1's, and there may be no more than seven 0's separating 1's.

Since the loop doesn't update on 0's, VCO edges corresponding to the 0's are ignored by the loop. This has the same effect as having a bigger B divider and thus the same

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model for the frequency synthesizer can be used for the data separator if we allow the value of B to be changed.

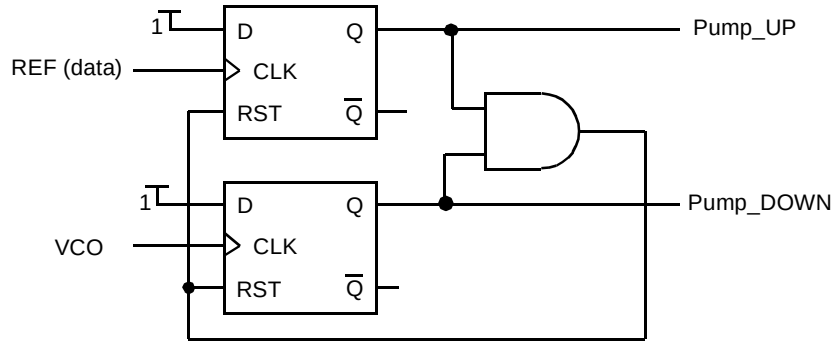

Figure 2a

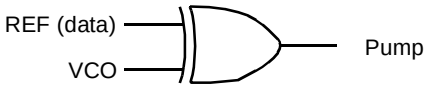

Figure 2b

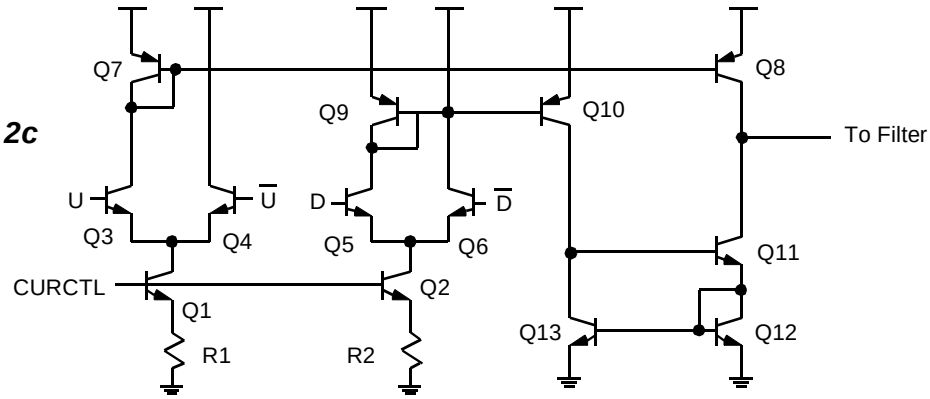

Figure 2c

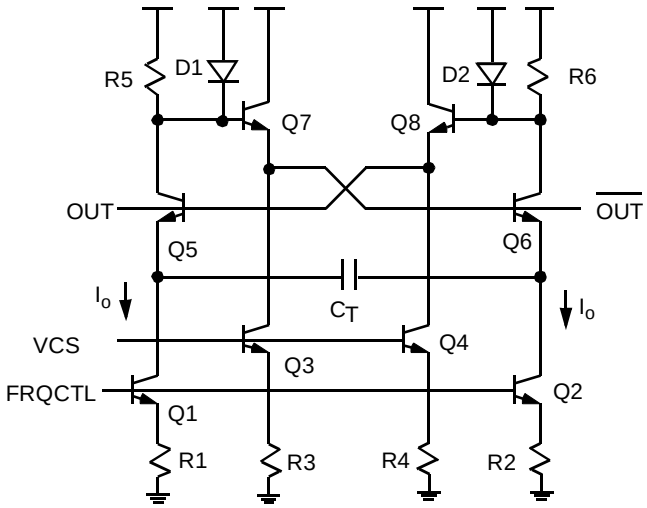

Figure 2d

Figure 2 Typical circuitry in PLL blocks. (a) Phase-frequency detector. (b) Phase detector. (c) Charge pump. (d) Voltage-controlled oscillator.

PLL BLOCKS

It is desirable that the user of PLLs have an idea of how the main circuit blocks work at the transistor level. In this section we give typical simplified schematics of phase detectors, charge pumps, and voltage-controlled oscillators (VCOs).

Phase Detectors

Phase detection is generally done using logic circuits. Such digital circuits handle phase as an analog quantity by using pulse width as an analog variable. The most commonly used phase detector is shown in Figure 2a and is a phase-frequency detector (see reference [3] for additional information).

The reference input[1] is fed into the clock input of one edge-triggered D flip-flop and the VCO output is fed into the other. The true outputs are ANDed together and fed back to asynchronous reset inputs for both flip-flops. To understand the circuit operation, first consider the situation where the rising edges of the VCO pulses arrive later than those of the reference frequency. This means that the VCO phase is lagging, and we need to increase its frequency to catch-up. Assume an initial state where both flip-flops have Q = 0 (the usual case). The reference rising edge arrives first and causes the Q output of the upper flip-flop to go to a '1'. This signal is called Pump_UP and is used to turn on a current source which feeds current into the filter. The rising edge of the VCO output arrives later and causes the lower flip-flop to be set to Q = 1. This causes a '1' to appear at the output of the AND gate, which feeds back to return both flip-flops to the initial Q = 0 state and turns off the Pump_UP current source. The cycle then repeats.

It is obvious from this description that the position of the waveform edge is the only thing that counts here, and that the phase error is in-effect sampled once per edge.

This type of phase-frequency detector has a practical problem when the phase error is very small. In real flip-flops the Q output will not get fully flipped before the reset action comes around. This is described as a dead band which happens with nearly zero phase error and can cause erratic operation. One solution to this problem is to insert extra gate delays after the AND gate so that in the locked condition, both pump-up and pump-down pulses are of finite, but equal width. With the averaging effect of the filter, the pulses will cancel each other out.

Figure 2b shows an alternative type of detector called a phase or phase-only detector (see reference [3] for additional information). It is simply an exclusive-OR gate. Here the single output is used to cause a pump-up condition when '1' or a pump-down condition when '0'. The steady-state condition of the circuit occurs when the pump-up and pump-down pulses occur with equal duty cycle and this can only occur when the two inputs (VCO and REF) are 90° out of phase (i.e., shifted by T/4, where T = 360°).

The phase-frequency detector has the desirable property that it shows little tendency to lock on harmonics (see reference [3] for additional information).

Charge Pumps

A typical charge pump circuit is shown in Figure 2c. The U and D inputs and their complements are the Pump_UP and Pump_DOWN outputs of Figure 2a, suitably level shifted. The pump current is generated by the current sources Q1, Q2, R1, R2 and is controlled by the CURCTL analog input which allows the value of the pump current to be changed (DAC-controlled, for example). In the normal condition (U = D = 0), the pump current is steered to VCC through Q4 and Q6, but when either U or D is high it is fed to one of the current mirrors (Q7, Q8 and Q9, Q10). The Pump_DOWN current is again mirrored by Q11-Q13 so that it turns on a current sink. The up and down pulses are then combined at the collectors of Q11 and Q8 and this net current is fed to the filter.

This circuit has a number of non-ideal features. The collector currents of Q8 and Q11 must match exactly for ideal operation. If they do not, a steady-state phase error will occur. But in reality component mismatches of this sort cause only small deviations from this condition. The pump-down current must pass through the extra mirror Q11-Q13 and this has a small effect on current matching and current switching dynamics. The collector currents of Q8 and Q11 are not completely independent of the DC voltage at the filter (the Early effect) and this is an additional source of error. Practical charge pumps often contain additional circuitry to cancel or correct these errors. In general, charge pumps work much better if fast PNP transistors are available in the process.

VCOs

The circuit of Figure 2d is often called an emitter-coupled multivibrator and is very widely used for VCOs (see reference [6] for additional information). The current sources Q1, Q2, R1, R2 set up two equal currents I_O, with the value of the current controlled by the voltage FRQCTL which comes from the filter output[2]. In the two half-cycles of circuit operation there is current through R5 and not through R6 or vice versa. Let us begin by assuming a state where there is current in R5, and none in R6. R5 has a relatively high value, so some of the collector current of Q5 flows through D1, which effectively clamps the voltage at the base of Q7 at $V_{CC} - V_{be}$. Thus the base of Q5 will have a potential about V_{be} higher than Q6. Both currents I_O pass through the emitter of Q5, one directly and the other through timing capacitor C_T. As current passes through C_T, it is gradually discharged and the potential at the emitter of Q6 ramps down, eventually becoming low enough that Q6 can turn on. When this point is reached, there is a very rapid regenerative (positive feedback) switching event which flips the circuit to the other half-cycle. A half-cycle requires that a current I_O change the voltage across C_T by $2V_{be}$, so that period $T = 1/f \approx 4V_{be}C_T/I_O$. Note that the frequency is proportional to the current I_O (and also FRQCTL) — important for a linear PLL. The inherent 50% duty cycle of the complementary outputs from this circuit is a desirable feature.

The VCO circuit as shown has a few problems. For one thing the frequency is temperature-dependent through $V_{be}(T)$. There are also tolerance questions since the VCO center frequency must be controlled to fairly close limits. Practical VCOs of this class incorporate additional circuitry for wide-range temperature-independent operation. There is often extra circuitry which can freeze the VCO in one half-cycle, so that it can then be started in synchronism with a detected read-data edge thus shortening the lock-on transient (this feature is called

[1] This input is the reference frequency for a synthesizer or the data for a data separator.

[2] Often a unity-gain buffer is placed between filter and VCO, designed in such a way as to drain minimal current from the filter capacitors during a hold condition. Otherwise the filter would have to supply base current for Q1 and Q2.

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zero-phase restart). Another important feature is input clamping. The circuitry must be designed in such a way that the frequency can vary only between two values f_1 and f_2. If the frequencies are too low (e.g., too-low FRQCTL values), the oscillator may simply stop oscillating, and there may be no recovery from this extreme nonlinear condition. If the allowed range is too broad, there is a potential for locking onto harmonics with equally disastrous results.

Early data separators had capacitor C_T off-chip so that it was user-selected. Today most integrated PLLs have C_T on-chip so that a much lower C_T value can be used and power saved. With fast-switching transistors, on-chip VCOs usable to beyond 300 MHz have been built.

When very low phase jitter is desired (as in a frequency synthesizer) great care must be taken to prevent crosstalk (e.g., from clocks, switchmode power supplies, etc.) from the VCO to extraneous signals. This requires good chip design, careful board layout, and bypassing by the user.

DATA SEPARATION

The Use of Codes.

As noted above, the coding scheme for data written on a disk must ensure that there is at least some minimum number of transitions (flux reversals) per unit time. Without readout peaks the data separator soon loses track of the correct phase of the read clock and will give erroneous results when it hits data again.

The most common code in use today is the (1,7) code. There are several versions, all of which obey the rules given below:

- Two input (NRZ) bits are encoded as 3 output bits.
- '1' bits must be separated by at least one '0' bit.
- There can be no more than seven '0' bits separating '1' bits.

Such codes are often referred to as RLL (Run-Length Limited) codes since the "no-more-than-7-zeroes" constraint imposes a limit on the length of runs of same-type symbols.

From the viewpoint of PLL operation, the data in an RLL input stream differs fundamentally from the square-wave input of a frequency synthesizer. The positions of '1' and '0' symbols are random and the data contains many different frequencies. So, steps must be taken in design to ensure that phase comparisons are made only where a transition (edge) occurs in the data.

Data Separator Block Diagram

Data separator PLLs take the general form described for frequency synthesizers, but have some additional features. Figure 3 shows a generic data separator PLL. The basic PLL is at the upper right. The RD_GATE signal is used to control switches S1 and S2.

During write operations the read PLL is on standby and gets its input from the reference clock (S1 in lower position and S2 in the upper position). This keeps the PLL locked at about the right frequency so that it can rapidly switch to reading upon command (i.e., without a long settling transient).

In read mode, the phase detector D inputs are driven by the undelayed read signal and the clock is driven by the delayed[3] read signal, which has the effect of suppressing phase

[3] The data is delayed by T/3 relative to the NRZ period or T/2 relative to the coded data period for optimal window centering of the PLL.

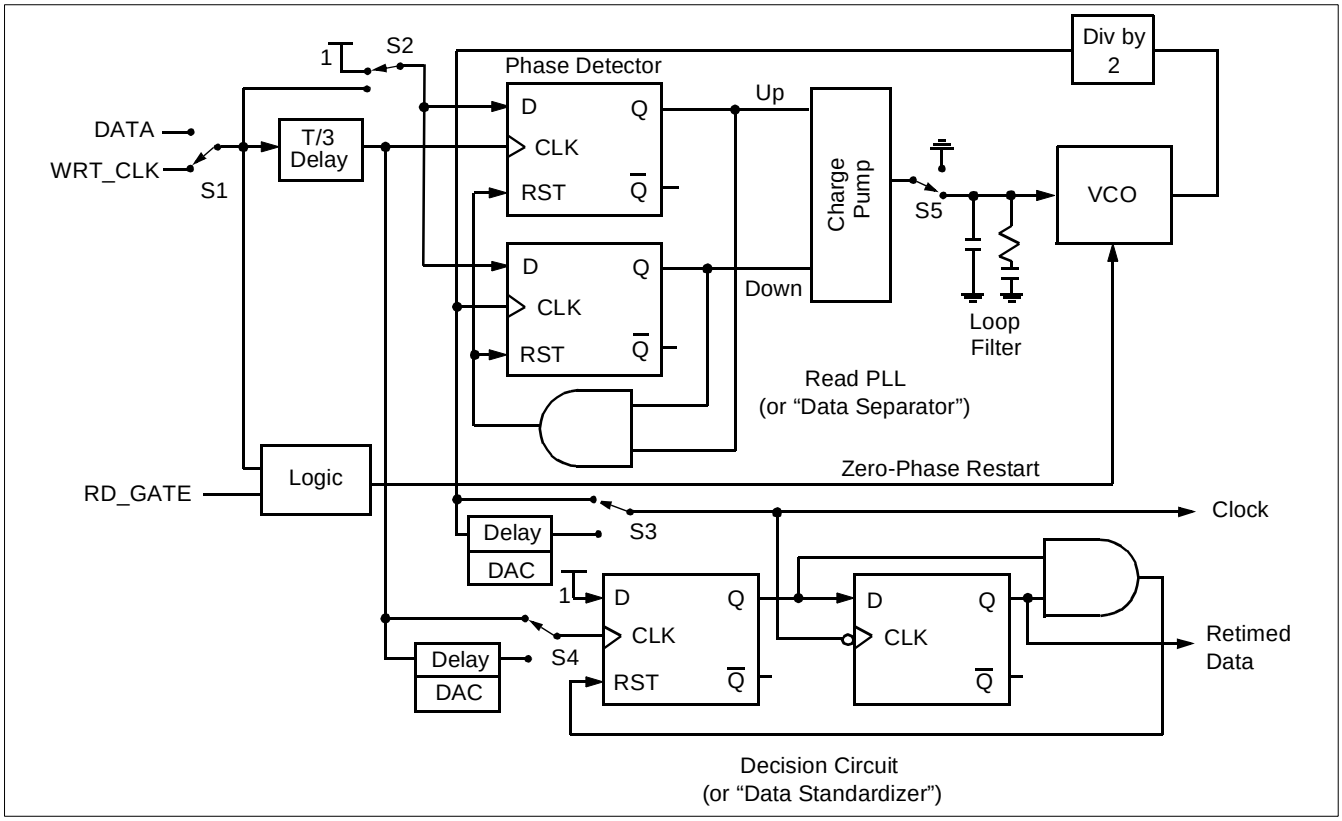

Figure 3 A typical clock recovery PLL (data separator or read PLL)

comparisons when there is no edge. This corresponds to S1 in the upper position and S2 in the lower position. This has the effect of enabling the phase detector only when logic '1' input edges are read, and disabling the loop when zeroes are read.

During certain operations such as seeks, there are times when the data separator PLL is idle but one would like to keep the same frequency so as to be able to lock again rapidly. This is done using the coast mode or hold mode controlled by switch S5. In the down position shown the PLL operates normally. In the up position (the coast mode) the loop filter capacitors are isolated and hold the VCO frequency as a stored charge. There is a certain slow bleed-off of charge due to base currents and low-level leakages which leads to errors in the frequency and limits the length of time over which the VCO remembers its frequency.

Lock Acquisition; Preambles; Zero-Phase Restart

The data separator reacquires the read clock at the beginning of each sector. The sector header information contains a region of constant-frequency data (such as repeating "001" symbols) during which the PLL acquires the clock. This is called the preamble. Often the charge pump current I_p is temporarily increased during the preamble to promote faster lock (wider loop bandwidth).

Because the data separator PLL has been locked to the reference clock when idle, it is at about the right frequency when it hits the preamble. However, it may begin the lockup transient with a substantial phase error. In order to promote rapid clock acquisition, a zero-phase restart signal is generated within the chip. When RD_GATE is asserted the restart control logic looks for edges in the preamble data. It then issues a zero-phase restart command to the VCO which momentarily freezes it in a '1' or '0' state and then releases it with a definite phase (usually nominally zero) simultaneously with a data edge. This greatly aids in fast clock acquisition.

The Read Window; Window Margin; Marginalization

The data separator PLL is set up to align the rising edges of the recovered read clock with the rising edges of the data coming from the pulse detector. Ideally, the decision circuit (or "data standardizer") at the bottom of Figure 3 will work correctly if the data edge is anywhere within the read window shown in Figure 4a (the ideal case). It is possible to get a non-centered window as shown in Figure 4b in the pulse detector circuitry for a number of reasons — finite propagation delay in the decision circuit logic, imbalance in internal signal lines, offsets and other problems (e.g. pulse pairing, mismatch of the UP and DOWN currents in the charge pump). The amount of early or late mistiming (bit shift) of the data edges which can be tolerated without an error is referred to as the window margin.

Another important problem is jitter, as shown in Figure 4c. This picture is what would be seen if one looked at the data separator output while triggering on the recovered clock. This jitter arises from a number of causes such as noise in the read signal or noise in the VCO and loop filter. If there is too much jitter for an acceptable BER (Bit Error Rate), changes may need to be made in bits/inch or preamplifier and head components.

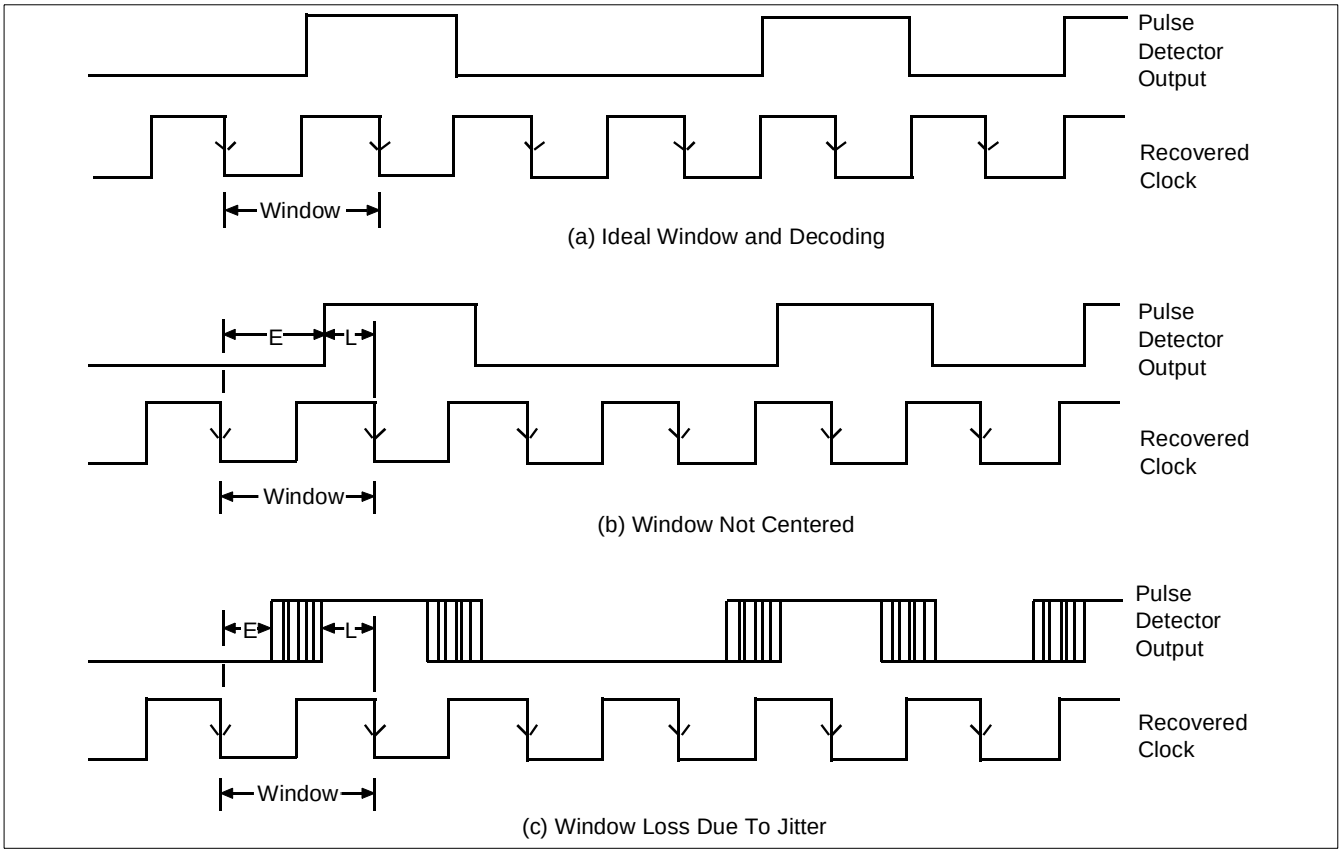

Figure 4 A typical clock recovery PLL (data separator or read PLL)

The window centering error shown in Figure 4b can be compensated for by what is called marginalization. In normal PLL operation, switches S3 and S4 are in the up position, so that the decision circuit operates directly on the clock and data. When the marginalization is active, two DAC-controlled delays are inserted before the decision circuit, with the DAC values being set by on-chip serial register bits. This allows the user to skew the timing deliberately either way. As a diagnostic tool, this allows the drive designer to determine the earliest and latest edges which lead to a given error rate, thus allowing window centering to be determined. The marginalization feature can also be used in an adaptive scheme in which a calibration procedure is done for each head. In this way, the optimum marginalization delay can be individually set for each head.

FREQUENCY-DOMAIN DESCRIPTION OF A PLL; OVERSHOOT AND STABILITY

In our simple time-domain analysis of the PLL in Figure 1 we neglected the effects of C_2 and R as nonessential to a basic qualitative explanation. In reality all three filter elements are necessary for satisfactory operation. A full analysis of the charge pump PLL including a description of the action of the lead-lag filter requires a more rigorous treatment of the PLL and that is provided here.

In the simple picture treated earlier (neglecting R and C_2) we saw that if f_A leads f_B the negative feedback action will steadily increase the VCO frequency until the phase difference is zero. Actually, when the phase difference has reached zero, the VCO frequency will be substantially higher than its steady-state center frequency, f_o. Thus, the phase will continue to decrease and pass through the zero-phase point, becoming negative, and a new correction cycle will begin. If the loop filter is only a capacitor, the PLL exhibits substantial overshoot in its phase dynamics. The additional filter elements R and C_2 allow the user to control this overshoot and optimize the phase dynamics[4].

We will assume that the loop is running near its center frequency, f_o. We also assume that any changes in the input phase difference or the VCO frequency occur slowly enough that f_B and f_A differ by only a small amount, but can have any phase relationship. Phase can be thought of as the relative position of the rising edge of one signal as compared to a second signal, divided by the period T ($T \approx 1/f_A \approx 1/f_B$).

A PLL of this kind is a sampled-data system. The phase is only defined at the edges of the f_A and f_B signals (see reference [1] for additional information) In our analysis we are in effect making a continuous approximation that the highest frequencies in the behavior of the loop dynamics are much lower than the center frequency, or equivalently, that the bandwidth of the loop filter is much lower than the center frequency. In Nyquist terms, we are assuming that there are many samples per period for the shortest period in the loop response. Most practical PLLs operate in this regime. At the same time we are in effect considering only the linear behavior of the system so that the ordinary ideas of linear system theory apply. With large phase and frequency deviations the system will show nonlinear behavior, and in fact the initial capture transient is always nonlinear (see references [2], [3] and [6]). A rigorous sampled-data treatment has been given by Gardner (see reference [1] for additional information).

Mathematically, the phase $\Theta(t)$ (in radians) is the time integral of the angular frequency ω:

$$\Theta(t) = \int \omega dt \qquad \text{where } \omega = 2\pi f \qquad \textit{(eq. 10)}$$

The f_A and f_B signals can be described by their phases $\Theta_A(t)$ and $\Theta_B(t)$. The phase-frequency detector thus puts out an error phase $\Theta_\varepsilon(t)$ equal to the phase difference of $\Theta_A(t)$ and $\Theta_B(t)$:

$$\Theta_\varepsilon(t) = \Theta_A(t) - \Theta_B(t) \qquad \textit{(eq. 11)}$$

This is the analog equivalent of the time error t_ε in the “PLL Basics” section:

$$t_\varepsilon = \left(\frac{\Theta_\varepsilon(t)}{2\pi}\right)T \qquad \textit{(eq. 12)}$$

The charge pump outputs a current I_P only during t_ε and the average charge pump current will be:

$$I_{ave} = I_p\left(\frac{t_\varepsilon}{T}\right) = \left(\frac{I_p}{2\pi}\right)\Theta_\varepsilon(t) \equiv K_{cp}\Theta_\varepsilon(t) \qquad \textit{(eq. 13)}$$

The loop filter impedance is Z_F, so:

$$V_{in} = I_{ave}Z_F \qquad \textit{(eq. 14)}$$

The VCO converts its input voltage V_{in} to an output frequency f_o (where $K_{VCO} = 2\pi K_V$):

$$f_o = K_V V_{in} \quad \text{or} \quad \omega_o = K_{vco}V_{in} \qquad \textit{(eq. 15)}$$

Thus, the VCO output phase is:

$$\Theta_o(t) = \int \omega_o dt \qquad \textit{(eq. 16)}$$

The frequency dividers scale the phase as well as the frequency, so:

$$\Theta_B(t) = \frac{\Theta_o(t)}{B}, \qquad \Theta_A(t) = \frac{\Theta_i(t)}{A} \qquad \textit{(eq. 17)}$$

Combining the equations, we find that:

$$\Theta_B(t) = \left(\frac{K_{VCO}}{B}\right)\left(\frac{I_p}{2\pi}\right)\int\{Z_F[\Theta_A(t) - \Theta_B(t)]\}dt \qquad \textit{(eq. 18)}$$

Taking the Laplace transform of this equation (which puts things in terms of the complex frequency variable s), we find:

$$\Theta_B(s) = \left(\frac{1}{s}\right)\left(\frac{K_{VCO}}{B}\right)\left(\frac{I_p}{2\pi}\right)Z_F(s)(\Theta_A(s) - \Theta_B(s)) \qquad \textit{(eq. 19)}$$

where,

[4] The frequency and phase in a PLL behave like the displacement and momentum of a simple mechanical oscillator and many analogies can be drawn. In most practical cases the behavior is oscillatory. When the phase error is at a maximum the frequency error will be zero and conversely during a system transient.

$$Z_F(s) = \frac{\left(R + \frac{1}{sC_1}\right)\left(\frac{1}{sC_2}\right)}{R + \frac{1}{sC_1} + \frac{1}{sC_2}}$$

$$= \frac{R\left(s + \frac{1}{RC_1}\right)}{SC_2R\left[s + \frac{1}{RC_1}\left(\frac{C_1 + C_2}{C_2}\right)\right]} \quad \textit{(eq. 20)}$$

In what follows we will use the phases as independent variables in describing the loop dynamics, as shown in the signal-flow diagram of Figure 5.

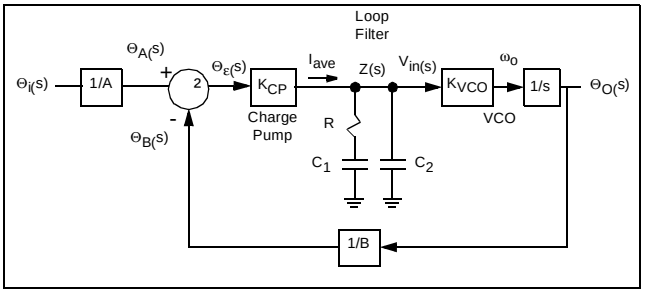

Figure 5 Signal flow diagram for a phase-locked loop with a lead-lag loop filter

Putting in the explicit form of $Z_F(s)$, we can now write $\Theta_B(s)$ as:

$$\Theta_B(s) = \frac{K_{VCO}K_{CP}\left(s + \frac{1}{RC_1}\right)}{Bs^2C_2\left[s + \frac{1}{RC_1}\left(\frac{C_1 + C_2}{C_2}\right)\right]}(\Theta_A(s) - \Theta_B(s)) \quad \textit{(eq. 21)}$$

This is the transfer function for $\Theta_B(s)$ in the complex frequency domain. Both the numerator and denominator are polynomials in s. Thus, $\Theta_B(s)$ can be described by an amplitude and phase response (a Bode plot, etc.) like any other dynamical variable. We can also consider the amplitude response of the phase and the phase response of the phase, just as for an amplifier.

A word of caution: unlike a feedback amplifier where the transfer function of interest is voltage gain, a phase-locked loop deals with phase gain. The transfer function has real and imaginary components which can be described in terms of a magnitude and angle (or argument). For a feedback amplifier the angle is actually the phase of the signal. It is rather easy to comprehend the gain and phase of an amplifier and consequently the angle of the complex transfer function is routinely referred to as phase. In the case of a PLL, however, the magnitude of the transfer function is the phase gain while the angle represents a time delay of the phase gain. It is tempting to refer to the angle as the phase and retain terms like phase margin that are already familiar from amplifier analysis. Thus, we have the phase of the phase which can be rather confusing. The solution to this situation is to treat the frequency domain phase variable as just a gain variable with real and imaginary parts, which have mathematical and graphical stability properties that are true regardless of the particular PLL application. Here the magnitude of the transfer function will be referred to as phase gain while the angle will simply be called the angle. The term phase margin will still be used to refer to the angle of the transfer function in relation to 180°.

The closed-loop gain of the system is denoted by H(s), and is the gain from input $\Theta_A(s)$ to output $\Theta_B(s)$:

$$H(s) = \frac{\Theta_B(s)}{\Theta_A(s)} \quad \textit{(eq. 22)}$$

The open-loop gain of the system is denoted G(s) and is the phase gain from input to output if the feedback loop is broken. This is equivalent to the gain from $\Theta_\varepsilon(s)$ to $\Theta_B(s)$:

$$G(s) = \frac{\Theta_B(s)}{\Theta_\varepsilon(s)} = \frac{\Theta_B(s)}{(\Theta_A(s) - \Theta_B(s))} \quad \textit{(eq. 23)}$$

Thus G(s) = H(s)/(1 - H(s)) and H(s) = G(s)/(1 + G(s)). From the relations above:

$$G(s) = \frac{K_{VCO}K_{CP}\left(s + \frac{1}{RC_1}\right)}{Bs^2C_2\left[s + \left(\frac{1}{RC_1}\right)\left(\frac{C_1 + C_2}{C_2}\right)\right]} \quad \textit{(eq. 24)}$$

Let: $\tau = RC_1$
$\omega_1 = 1/\tau = 1/RC_1$
$K = K_{VCO}K_{CP}R/B = K_VI_pR/B$
$b = 1 + (C_1/C_2) = (C_1 + C_2)/C_2$
$\omega_2 = b\omega_1 = [(C_1 + C_2)/C_2]/RC_1$

then:

$$G(s) = \frac{K(\omega_2 - \omega_1)(s + \omega_1)}{s^2(s + \omega_2)} \quad \textit{(eq. 25)}$$

The open-loop response of the system is third-order, type II (see references [2] and [3]). There are two poles at s = 0, a third pole at s = $-\omega_2$, and a zero at s = $-\omega_1$. Insight into the loop behavior can be gained by drawing a Bode plot of G(jω) as shown in Figure 6.

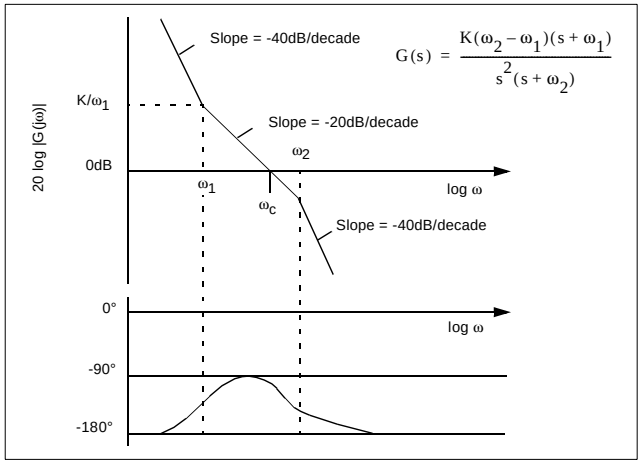

Figure 6 Bode plot of the open-loop response G(jw) for a charge-pump PLL

APPLICATION NOTES

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The open-loop response is infinite when $\omega = 0$ and rolls off at -40 dB/decade due to the two poles at the origin until $\omega = \omega_1$. This zero cancels one of the poles causing the response to roll off at -20dB/decade until $\omega = \omega_2$. At this point it rolls off again at -40dB/decade due to the pole at ω_2. The angle of G(jω) starts at -180° and rises to -90° at some point above $\omega = \omega_1$, and then returns to -180° beyond $\omega = \omega_2$.

Linear system theory dictates that for a system to be stable, the angle of the transfer function at the frequency where $|G(j\omega)| = 1$ should be more than 45° from -180° (in a feedback amplifier system this is referred to as phase margin)[5]. From the Bode diagram we see that this can only happen if $|G(j\omega)|$ crosses the unity-gain axis at a point where the slope of $|G(j\omega)|$ is -20dB/decade.

The frequency at which $|G(j\omega)| = 1$ is called the crossover frequency ω_c. As seen from the Bode diagram:

$$|G(j\omega)| = 1 \quad @ \quad \omega = \omega_c \qquad \textit{(eq. 26)}$$

A necessary condition for stability is:

$$\omega_1 < \omega_c < \omega_2 \qquad \textit{(eq. 27)}$$

We also see that if ω_1 and ω_2 are too close to one another $\angle G(j\omega)$ will never rise much above -180°. According to Gardner [1], $\omega_2 > 9\ \omega_1$ for most practical cases. This fact can be used to simplify G(s). For $\omega << \omega_1$, $s + \omega_2 \approx \omega_2$ and $\omega_2 - \omega_1 \approx \omega_2$:

$$G(s) \approx \frac{K(s + \omega_1)}{s^2} \qquad \textit{(eq. 28)}$$

Using the asymptotic approximation characteristics of the Bode Diagram:

$$|G(\omega_1)| = \frac{K}{\omega_1} \quad \text{for} \quad \omega_1 << \omega << \omega_c \qquad \textit{(eq. 29)}$$

If $\omega_c << \omega_2$, and $\omega_c >> \omega_1$, then:

$$|G(\omega_c)| = 1 = \frac{K}{\omega_c} \Rightarrow \omega_c = K \qquad \textit{(eq. 30)}$$

The unity gain or crossover frequency for the loop is equal to K, which is known as the loop gain. ω_c is often referred to as the loop bandwidth since it represents the frequency above which frequency variations are filtered out of the loop. The loop is said to track any change in input frequency below ω_c. In a data synchronizer application the loop bandwidth should be set high enough so that bit shifts due to mechanical inaccuracies in the drive will be tracked by the loop. In a frequency synthesizer, however, loop bandwidth is generally set low so that any jitter in the input frequency (from a switching power supply for example) will be filtered out.

Thus we see that loop gain and the loop bandwidth are actually the same thing. This seems somewhat puzzling intuitively, but if the third-order loop equation is inspected we see that K must have units of frequency. Remember too that the VCO in effect integrates frequency into phase, yielding the additional 1/s term which must be accounted for in the units for K, so that G(s) is unitless.

We now consider the closed-loop response H(s):

$$\frac{\Theta_B(S)}{\Theta_A(S)} = H(s) = \frac{G(s)}{1 + G(s)} = \frac{K(\omega_2 - \omega_1)(s + \omega_1)}{s^3 + \omega_2 s^2 + K(\omega_2 - \omega_1)s + K(\omega_2 - \omega_1)\omega_1} \qquad \textit{(eq. 31)}$$

In general this is a third-order polynomial and there are no simple formulas for the roots (zeroes). A number of inexpensive computer programs are available which can find the roots of any reasonable polynomial.

If $\omega_2 >> \omega_1$, which we know must be true from the open-loop stability analysis, then we can approximate the loop as second order by letting ω_2 approach infinity; this provides the equation:

$$H(s) = \frac{K(s + \omega_1)}{s^2 + Ks + K\omega_1} \qquad \textit{(eq. 32)}$$

The denominator is a quadratic second order equation which can be rewritten as:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad \textit{(eq. 33)}$$

$$\text{where} \quad \omega_n = \sqrt{K\omega_1} \quad \text{and} \quad \zeta = \frac{1}{2}\sqrt{\frac{K}{\omega_1}}$$

ω_n is called the natural frequency of the loop and ζ is known as the damping factor. The poles of H(s) are found by solving the equation:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \qquad \textit{(eq. 34)}$$

When this is done we find the poles P_1 and P_2 are:

$$P_1, P_2 = -\omega_n[\zeta \pm \sqrt{(\zeta^2 - 1)}] \qquad \textit{(eq. 35)}$$

Different values of ζ lead to the following three cases:

1. If $\zeta > 1$, then P_1 and P_2 are real and the loop is unconditionally stable and is said to be overdamped.
2. If $\zeta = 1$, then $P_1 = P_2 = \omega_n$ and the loop is unconditionally stable and is said to be critically damped.
3. If $\zeta < 1$, then P_1 and P_2 form a pair of complex conjugate poles and the loop becomes less stable as ζ approaches 0 and is said to be underdamped.

The damping concept should be familiar from other disciplines (such as mechanics). Often the loop is specified to have a desired damping factor ζ and loop bandwidth ω_c. Damping is of practical importance in disk drive design because we require that the phase errors[6] of the recovered read clock be settled to

[5] The condition is often stated in the form that oscillation will occur if the phase response is 360°. In our case a feedback transfer function phase response of 180° will lead to oscillation because the inherent negative feedback (inversion) in the phase detector is equivalent to a 180° phase shift.

[6] That is to say, the phase difference between the VCO output and the peaks in an ideal read signal.

some specified degree before we regard the recovered data as valid. It is the damping which determines how long it takes the phase error to settle to zero.

There are a number of useful identities for the second-order loop:

$$\omega_n = \sqrt{K\omega_1} = \sqrt{\frac{K}{\tau}} = \frac{\omega_c}{\tau} = \sqrt{\omega_c\omega_1}$$
$$\zeta = \frac{1}{2}\sqrt{\frac{K}{\omega_1}} = \frac{1}{2}\sqrt{K\tau} = \frac{1}{2}\sqrt{\omega_c\tau} = \frac{1}{2}\sqrt{\frac{\omega_c}{\omega_1}} \quad \textit{(eq. 36)}$$

thus:

$$\omega_c = K = 2\zeta\omega_n,\ K\tau = \frac{\omega_c}{\omega_1} = 4\zeta^2,$$
$$\frac{K}{\tau} = \omega_c\omega_1 = \omega_n^2,\ \omega_n\tau = \frac{\omega_n}{\omega_1} = 2\zeta \quad \textit{(eq. 37)}$$

The loop is completely specified with either pair of variables K and τ or ω_n and ζ, and one set can be calculated from the other.

The loop transient response is of interest. An underdamped system is fairly responsive but tends to overshoot and ring. An overdamped system has no overshoot but is rather slow in reaching its final steady-state value when responding to a transient input. It can be shown (see references [2] and [3]) that a damping factor of $\zeta = 0.707 = 1/\sqrt{2}$ will yield an optimal transient response to a frequency ramp input. Here the phase of the output will reach its final steady state output in $3.4/\omega_n$ with 5% overshoot. Generally most data synchronizers have ζ between 0.5 and 0.8 so that they can acquire lock quickly at the beginning of a read cycle.

The noise bandwidth B_L of a second-order PLL is given by reference [3]:

$$B_L = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] = \frac{1}{4}(\omega_c + \omega_1) \quad \textit{(eq. 38)}$$

An input noise signal at frequencies above B_L will be filtered out of the loop. B_L is at a minimum of $0.5\omega_n$ for $\zeta = 0.5$, but is still only $0.53\omega_n$ at $\zeta = 0.707$. In a frequency synthesizer noise filtering is important and consequently it has a damping factor range of about 0.5 to 1.0 as well.

COMPONENT SELECTION FOR THE SECOND-ORDER LOOP

Choosing the resistor and two capacitors in the lead/lag filter is one of the main problems facing the disk drive designer. Before proceeding the following parameters must be specified:

Charge pump gain:	$K_{cp} = I_p/2\pi$
VCO gain:	$K_{VCO} = 2\pi K_V$
Feedback divider ratio:	B
Loop bandwidth:	$f_c = \omega_c/2\pi = K/2\pi$
Damping factor:	ζ

The first three may be fixed by the monolithic design of the phase-locked loop, but for chips supporting zone-density recording they usually can be controlled by the user over some restricted range. The last two are always user-definable for devices with off-chip loop filter components.

In the second-order approximation, the capacitor C_2 should be chosen such that $C_2 \le C_1/10$. This follows from the stability criteria and is also required for the second-order approximation to be valid. The bigger C_2 is, however, the more the charge pump ripple is filtered, yielding lower VCO jitter.

The charge pump gain is usually specified as a current I_p. The VCO gain is usually given as K_V in MHz/V. Often the VCO gain scales with frequency and may be specified as a fixed fraction of the center frequency:

$$K_V = \kappa f_o \quad \textit{(eq. 39)}$$

where κ generally ranges from 0.1 to 0.5. Note that κ has units of 1/V. The feedback divider is simply an integer. Zone-programmable frequency synthesizers allow B to be changed, typically through a serial register interface. Data synchronizers sometimes allow the feedback divider to be programmed, but B as defined here also incorporates the effect of the data pattern. Thus, the effective B value will change as the data pattern varies from “01010” to “01000000010” (the extreme limits for (1,7) code). To ease confusion, B can be rewritten as the product of the internal hard-wired (or firm-wired) divider ratio and the data pattern length. Let T_R be the relative data pattern length such that $T_R = 2$ for a 2T[7] pattern, 3 for a 3T pattern, etc., and let N be the hardware division ratio. Then:

$$B = NT_R \quad \textit{(eq. 40)}$$

From the equations derived earlier:

$$f_c = \frac{\omega_c}{2\pi} = \frac{K}{2\pi} = \frac{K_{VCO}K_{CP}R}{2\pi B} = \frac{K_V I_p R}{2\pi B} = \frac{\kappa f_o I_p R}{2\pi N T_R} \quad \textit{(eq. 41)}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_c}{\omega_1}} = \frac{1}{2}\sqrt{2\pi f_c R C_1} \quad \textit{(eq. 42)}$$

Solving for R and C_1 we find:

$$R = \frac{2\pi f_c B}{K_V I_p} = \frac{2\pi f_c N T_R}{\kappa f_o I_p} \quad \textit{(eq. 43)}$$

$$C_1 = \frac{2\zeta^2}{\pi f_c R} = \left(\frac{\zeta}{\pi f_c}\right)^2 \frac{K_V I_p}{B} = \left(\frac{\zeta}{\pi f_c}\right)^2 \frac{\kappa f_o I_p}{N T_R} \quad \textit{(eq. 44)}$$

The phase margin ϕ_R for the loop can be calculated by determining the angle of the open loop transfer function G(s) at $\omega = \omega_c$ relative to -180°. Using the second-order loop approximation:

[7] In disk drives a 2T pattern is a repeating “01”, a 3T pattern is a repeating “001”, a 4T pattern is a repeating “0001”, etc.

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$$G(s) \approx \frac{K(s+\omega_1)}{s^2}$$

$$\angle G(j\omega_c) = \angle \frac{K(j\omega_c+\omega_1)}{(j\omega_c)^2}$$

$$= \tan^{-1}\frac{\omega_c}{\omega_1} - \pi \qquad \textit{(eq. 45)}$$

$$= \tan^{-1}(4\zeta^2) - \pi$$

$$\phi_R = [\tan^{-1}(4\zeta^2) - \pi] - (-\pi)$$

$$= \tan^{-1}(4\zeta^2)$$

From the results given in [4] this can be approximated as:

$$\phi_R \approx 100\zeta \quad (\text{for } \phi_R \text{ in degrees}) \qquad \textit{(eq. 46)}$$

For a data synchronizer, the phase margin, and hence the damping factor, should be calculated for each data pattern to ensure stability of the loop. Generally phase margin should exceed 45°, which implies $\zeta > 0.5$. As an example:

$$\text{for} \quad \zeta = \frac{1}{\sqrt{2}} = 0.707, \quad \phi = 63.4° \qquad \textit{(eq. 47)}$$

SECOND ORDER EXAMPLE USING THE VM5351 DATA SEPARATOR

How do we best set up the variable loop parameters such as the filter components for (1,7) code using the second order approximation?

The phase-frequency detector is only active when there is an edge in the data input. In real data the edges are spaced far apart and this has the same effect on the loop as changing the feedback divider B. For (1,7) code the highest-frequency data pattern is a repeating “0101” pattern. This is called a 2T pattern because it has a period of 2T, where T is the period of the 1.5f code clock. Because it is necessary to generate both a 1f and a 1.5f clock from the data synchronizer loop, the VCO is often run at 3f so a divide-by-2 circuit can be used for the 1.5 f clock and a divide-by-3 circuit for the 1f clock. The frequency at f_B must be 1.5f, thus a divide-by-2 circuit is needed in the feedback path. The 2T pattern acts like another divide-by-2:

$$B = NT_R = 2 \bullet 2 = 4 \text{ for a 2T pattern}$$

The lowest-frequency pattern in (1,7) code is “01000000010” which has an 8T period. This is effectively a division ratio of 16:

$$B = 2 \bullet 8 = 16 \text{ for an 8T pattern}$$

The filter components should be chosen to get satisfactory response under these extreme conditions, as well as all patterns in between.

Assume the following specifications:

Code (1,7), 2/3 RLL
NRZ Data Rate = 64Mbits/sec (= f)
VCO Center Frequency = f_o = 192MHz (= 3f)
REFOSC Frequency = 96MHz (= 1.5f)
Crossover Frequency, ω_c = 1000K rad/s
Damping Factor, ζ = 0.7
Preamble length = 11 NRZ bytes (EDSI min.)
= 3.67µs (44 recorded pulses)

Refer to Figure 7. The impedance of the loop filter can be written as follows:

$$Z(s) = \frac{s + \frac{1}{RC_1}}{sC_2\left(s + \frac{1}{RC_1} + \frac{1}{RC_2}\right)} \qquad \textit{(eq. 48)}$$

The open loop gain is:

$$G(s) = \frac{K_{VCO}K_{CP}K_{div}\left(s + \frac{1}{RC_1}\right)}{s^2C_2\left[s + \frac{1}{RC_1}\left(\frac{C_1+C_2}{C_2}\right)\right]} \qquad \textit{(eq. 49)}$$

where: $K_{CP} = K_d = 1.18/R_L$,
$K_{VCO} = K_O = 0.105f_o$,
$K_{div} = 1/AB = 1/ANT_R = 1/A2T_R$

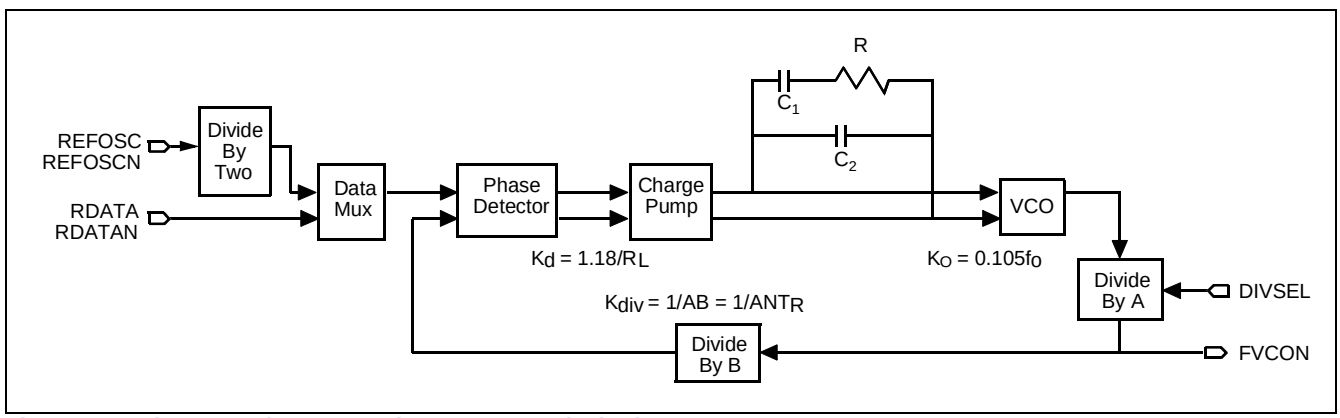

Figure 7 Basic VM5351/VM5352 and VM5353 PLL Block Diagram

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B is defined as NT_R. N = 2 and T_R is the relative encoded data pattern length. For example, a 4T preamble field would correspond to T_R equaling 4. When locked to the reference, T_R is equal to 2. The divide-by-A block is defined as:

A = 1 if the DIVSEL pin is LO
A = 2 if the DIVSEL pin is HI

The VCO center frequency is f_o. R_L is either the HGREXT or LGREXT external resistor, depending on whether the PLL is in high-gain or low-gain mode.

Substituting these values into G(s) and using the second order approximation where $C_2 << C_1$, G(s) becomes:

$$G(s) = \frac{K(s+\omega_1)}{s^2}, \quad \text{where } \omega_1 = \frac{1}{RC_1}$$
$$\text{and } K = K_{CP}K_{VCO}K_{div}R = \frac{0.124f_oR}{A2T_RR_L} \qquad \textit{(eq. 50)}$$

Looking at G(s), there are two poles at s = 0 and one zero at s = -ω1. The closed loop gain H(s) is defined as:

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{K(s+\omega_1)}{s^2+Ks+K\omega_1} \qquad \textit{(eq. 51)}$$

The denominator of H(s) is called the characteristic equation. It can be compared to the standard form for second degree characteristic equation as follows:

$$s^2+Ks+K\omega_1 = s^2+2\zeta\omega_n+\omega_n^2 \qquad \textit{(eq. 52)}$$

Equating the component values gives:

$$K = 2\zeta\omega_n \text{ and } K\omega_1 = \omega_n^2 \qquad \textit{(eq. 53)}$$

where ω_n is the natural frequency of the loop and ζ is the damping factor.

Now, substituting for K and ω_1 (in equations 43, 44 and 50), the values for R, C_1, and C_2 can be obtained:

$$R = \frac{(2\zeta\omega_n)A2T_RR_L}{0.124f_o} = \frac{\omega_cA2T_RR_L}{0.124f_o} \qquad \textit{(eq. 54)}$$

$$C_1 = \frac{0.124f_o}{\omega_n^2A2T_RR_L} = \left(\frac{2\zeta}{\omega_c}\right)^2\frac{0.124f_o}{(A2T_R)R_L} \qquad \textit{(eq. 55)}$$

$$C_2 \text{ is choosen such that; } \frac{C_1}{1000} < C_2 < \frac{C_1}{10} \qquad \textit{(eq. 56)}$$

Component values can now be selected in accordance with specific system requirements. The following system parameters must be specified: f_o (VCO center frequency), R_L (in high or low gain mode), T_R, ω_n or ω_c and ζ in order to choose values for R, C_1 and C_2.

Since the VCO center frequency is greater than 60MHz, the DIVSEL pin should be tied low, which implies that A = 1 for the divide-by-A block.

The first step is to choose the three external resistors. The HGREXT and LGREXT resistors setup the change pump current gain, and VCOREXT sets the VCO center frequency. They are determined as follows:

$$HGREXT = \frac{1.18V}{\text{HG Charge Pump Current}} = \frac{1.18V}{1.0mA} = 1.18k\Omega \qquad \textit{(eq. 57)}$$

$$LGREXT = \frac{1.18V}{\text{LG Charge Pump Current}} = \frac{1.18V}{0.3mA} = 3.9k\Omega \qquad \textit{(eq. 58)}$$

$$VCOREXT = 0.268 + \frac{223.2}{192} + \frac{7632}{192^2} = 1.6k\Omega \qquad \textit{(eq. 59)}$$

The low gain mode is used when locking to data and the high gain mode is used when locking to the reference oscillator or preamble. The component values can be chosen for either the high or low gain mode. Assuming lock-to-data, LGREXT will be used for R_L. Also, an average data pattern of 4T is assumed.

The values for R, C_1 and C_2 are calculated as follows (based on the equations derived above):

$$R = \frac{(1000\times10^3)(1)(2)(4)(3900)}{0.124(192\times10^6)} = 1310\Omega \qquad \textit{(eq. 60)}$$

$$C_1 = \left(\frac{2(0.7)}{1000\times10^3}\right)^2\left(\frac{0.124(192\times10^6)}{(1)(2)(4)(3900)}\right) = 1.5nF \qquad \textit{(eq. 61)}$$

$$C_2 = 0.01C_1 = 15pF \qquad \textit{(eq. 62)}$$

Now, ω_c and ζ should be recalculated to ensure accuracy and the phase margin ϕ_R should be calculated:

$$\omega_c = K = \frac{0.124f_oR}{A2T_RR_L} = 999Krad/s \qquad \textit{(eq. 63)}$$

$$\zeta = \frac{1}{2} = \sqrt{RC_1\omega_c} = \frac{1}{2}\sqrt{(1310)[1.5\times10^{-9}(999\times10^3)]} = 0.7 \qquad \textit{(eq. 64)}$$

$$\phi_R \cong \tan^{-1}(4\zeta^2) = \tan^{-1}[4(0.7)^2] = 62.96° \qquad \textit{(eq. 65)}$$

The values for ω_c and ζ did not change much here, but depending on what standard component values are used, they could change substantially. The phase margin should be greater than 45° for stability. In this case there is plenty of margin since ϕ_R = 63°.

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The above values are most likely not optimized for all systems using this data rate, code and preamble. The derivations are only shown as an example.

COMPONENT SELECTION FOR THE THIRD-ORDER LOOP

The second-order loop approximation results in loop filter component value calculations which are algebraically quite simple. This gives the user a quick way to get the loop running about where it should be. Often the second-order loop approximation works fine, particularly if $C_2 << C_1$. However, the purpose of C_2 is to filter the ripple on R and C_1 inherent to charge pump design, so it is desirable to make C_2 as large as possible. The loop will then also roll off more quickly with frequency (i.e., higher Q) which may be desirable. The user who needs maximum performance from the PLL should really treat the loop as a true third-order loop. Unfortunately, the results are not as simple algebraically and numerical methods are often needed. Some useful approximations can still be made, however.

Note that the third-order loop requires one more parameter to be specified. That parameter, b, is defined as:

$$b = 1 + (C_1/C_2) \qquad \textit{(eq. 66)}$$

Standard values for capacitors are usually 1 decade apart, so b is often chosen to be 11.

From inspection of the open loop Bode diagram (Figure 6), it can be seen that for small ω_2 values which approach ω_1 it is hard to achieve a good phase margin for the system. Phase margin is optimal when the crossover frequency ω_c occurs at the point where $\angle G(\omega)$ peaks. Graphically we expect this to happen when ω_c is half-way between ω_1 and ω_2. Because of the logarithmic scale used in Bode diagrams, this half-way point is the geometric mean of ω_1 and ω_2:

$$\omega_c = \sqrt{\omega_1\omega_2} \quad \text{for optimal phase margin} \qquad \textit{(eq. 67)}$$

We recall that:

$$G(s) = \frac{K\omega_1(b-1)(s+\omega_1)}{s^2(s+b\omega_1)} \qquad \textit{(eq. 68)}$$

$$\omega_2 = b\omega_1 \qquad \textit{(eq. 69)}$$

so:

$$\omega_c = \sqrt{b\omega_1^2} = \omega_1\sqrt{b} \qquad \textit{(eq. 70)}$$

In the asymptotic approximation for $\omega_1 < \omega_c < \omega_2$:

$$G(s) \approx \frac{K\omega_1(b-1)s}{s^2 b\omega_1} = \frac{K}{s}\left(\frac{b-1}{b}\right) \qquad \textit{(eq. 71)}$$

By definition:

$$\left|G(j\omega_c)\right| = 1 = \left(\frac{K}{\omega_c}\right)\frac{b-1}{b} \Rightarrow \omega_c = \frac{K(b-1)}{b} \qquad \textit{(eq. 72)}$$

Substituting for ω_1 and K, C_1 can be found as follows:

$$\omega_1\sqrt{b} = \frac{K(b-1)}{b} \Rightarrow \omega_1 = \frac{K(b-1)}{b\sqrt{b}}$$
$$\frac{1}{RC_1} = \frac{K_V I_P R(b-1)}{Bb\sqrt{b}} \qquad \textit{(eq. 73)}$$

or:

$$C_1 = \frac{Bb\sqrt{b}}{K_V I_P R^2(b-1)} \qquad \textit{(eq. 74)}$$

Now R can be found as follows:

$$\omega_c = \frac{K(b-1)}{b} = \left(\frac{K_V I_P R}{B}\right)\left(\frac{b-1}{b}\right) \qquad \textit{(eq. 75)}$$

or:

$$R = \left(\frac{\omega_c B}{K_V I_P}\right)\frac{b}{b-1} \qquad \textit{(eq. 76)}$$

Collecting all of these results together, the filter component values C_1, C_2, and R for the optimized third-order loop can be calculated from the expressions:

$$C_1 = \left(\frac{K_V I_P}{(2\pi f_c)^2 B}\right)\frac{b-1}{\sqrt{b}} = \left(\frac{\kappa f_o I_P}{(2\pi f_c)^2 N T_R}\right)\frac{b-1}{\sqrt{b}} \qquad \textit{(eq. 77)}$$

$$C_2 = \frac{C_1}{b-1} \qquad \textit{(eq. 78)}$$

$$R = \left(\frac{2\pi f_c B}{K_V I_P}\right)\frac{b}{b-1} = \left(\frac{2\pi f_c N T_R}{\kappa f_o I_P}\right)\frac{b}{b-1} \qquad \textit{(eq. 79)}$$

This analysis only applies to a PLL with optimal phase margin. As T_R, and hence B vary, the phase margin will vary. One can optimize the phase margin for a typical data pattern, such as 3T (001) and then calculate the phase margins for other data patterns. Phase margin is defined as:

$$\phi_R = \angle G(j\omega_c) - (-\pi)$$
$$G(j\omega_c) = \frac{K\omega_1(b-1)(j\omega_c+\omega_1)}{(j\omega_c)^2(j\omega_c+b\omega_1)}$$
$$\angle G(j\omega_c) = \angle(j\omega_c+\omega_1) - \angle(j\omega_c+b\omega_1) - \pi$$
$$\phi_R = \tan^{-1}\left(\frac{\omega_c}{\omega_1}\right) - \tan^{-1}\left(\frac{\omega_c}{b\omega_1}\right) \qquad \textit{(eq. 80)}$$

The crossover frequency ω_c can be found as follows:

$$\left|G(j\omega_c)\right| = 1 = \frac{K\omega_1(b-1)\sqrt{\omega_c^2+\omega_1^2}}{\omega_c^2\sqrt{\omega_c^2+b^2\omega_1^2}} \qquad \textit{(eq. 81)}$$

The equation above (eq. 81) can be transformed to:

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$$\omega_c^6 + b^2\omega_1^2\omega_c^4 - K^2\omega_1^2(b-1)^2\omega_c^2 - K^2\omega_1^2(b-1)^2\omega_1^2 = 0 \quad \textit{(eq. 82)}$$

This is a cubic polynomial in ω_c^2 which can be solved numerically given K, ω_1, and b which are all functions of K_V, I_p, B, R, C_1, and b. ω_c can then be used to calculate ϕ_R exactly. Alternatively we can use the asymptotic approximation for ω_c derived earlier:

$$\omega_c \approx K\left(\frac{b-1}{b}\right) \quad \textit{(eq. 83)}$$

then:

$$\phi_R \approx \tan^{-1}\left(\frac{K(b-1)}{\omega_1 b}\right) - \tan^{-1}\left(\frac{K(b-1)}{\omega_1 b^2}\right) \quad \textit{(eq. 84)}$$

For the loop with optimized phase margin we have:

$$\frac{K}{\omega_1} = \frac{b\sqrt{b}}{b-1} \Rightarrow \frac{K(b-1)}{\omega_1 b} = \sqrt{b} \quad \textit{(eq. 85)}$$

$$\text{or,} \quad \phi_R \approx \tan^{-1}(\sqrt{b}) - \tan^{-1}\left(\frac{1}{\sqrt{b}}\right) \quad \textit{(eq. 86)}$$

As an example, if b = 11, then ϕ_R = 56.4°. This is lower than that calculated from the second-order approximation but still a reasonable value.

The damping factor ζ is no longer applicable to the third-order loop, so besides ω_c and b we need a third parameter to completely specify the loop. We could choose ϕ_R but then the values for K and ω_1 and hence R and C_1 would be embedded inside a transcendental equation. The recommended design procedure is to roughly calculate R and C_1 using the second-order approximation on an average data pattern and then calculate phase margins for all data patterns. Should any one of them drop below 45°, adjust the R and C values, recalculate ϕ_R, and iterate until adequate phase margin is achieved. An example of this procedure for the VM5711 Frequency Synthesizer used in a zone-density application is given in the THIRD ORDER EXAMPLE USING THE VM5711 FREQUENCY SYNTHESIZER on page 17.

APPLICATION CONSIDERATIONS FOR FREQUENCY SYNTHESIS

In this section we will describe some important aspects of frequency synthesizer operation and give a complete detailed example of a multi-zone setup for the VM5711.

Frequency Divider Ratios

Typically a frequency synthesizer operates continuously, but during a seek operation between zones it must settle to a new frequency. The settling time should be kept less than a typical minimum seek time, often a few milliseconds. This might seem like plenty of time, but in reality there are a couple of factors which slow things down. In the first place, drive designers may wish to have fine frequency resolution. This calls for large divider ratios, and with large divider ratios waveform edges only occur infrequently at the phase detector. Phase comparison only occurs at edges, so in effect the sampling rate becomes quite low. This leads in turn to low ω_n, and slow response (which calls for a large C_1).

Consider a case where we are synthesizing an output frequency of 21.37 MHz (T = 46.8 nanoseconds) with the B divider (Figure 1) set at 211. Then we only sample the phase every 46.8 x 211 = 9875 nanoseconds. If it requires 50 sampling periods to achieve adequate settling then the transient conditions will last for 50 x 9875 = 0.49 milliseconds. Smaller divider ratios will reduce this transient recovery time.

Phase Jitter, Pull-Out Problems; Cycle Slips

For frequency synthesizers a very low RMS jitter is usually required. The overall read/write error budget is better if the write jitter can be made negligible. The noise bandwidth B_L scales as ω_n. Minimum in-band noise and, thus, minimum phase jitter is achieved by making ω_n as small as possible. There would seem to be no real limit to this, leading one to the idea of 20 µF filter capacitors (or larger). Bigger is not, however, always better.

In fact, if too-large filter capacitors are used, *even a rather small disturbance can lead to loss of lock and a cycle slip*. This basically relates to the nonlinear behavior of the circuit and cannot be treated exactly. Best [3] gives us the following equation:

$$\Delta\omega_{PO} = 1.8\omega_n(\zeta+1) = \frac{1.8\omega_c(\zeta+1)}{2\zeta} \quad \textit{(eq. 87)}$$

Here $\Delta\omega_{PO}$ is the largest frequency step which can be tolerated by the PLL without loss of lock (the so-called pull-out condition). How could such a frequency step arise? Suppose that some electrical event causes the VCO input voltage to change. Since large filter capacitors are needed for frequency synthesizers they are invariably off-chip, and nearby clocks, logic signals, switching power supply glitches etc. can be picked up by the filter components. *A voltage step at the VCO input is a frequency step to the PLL*, and it will go into a transient condition when one occurs. Suppose that:

ω_n = 5.103 rad/s (about 1 kHz)
ζ = 0.7 (near-optimum)
K_{VCO} = 15.106 rad/V-s (1 V shifts f_o by 2.4 MHz)

Then $\Delta\omega_{PO}$ = 15,300 rad/s. The VCO input voltage shift ΔV_{PO} corresponding to this is:

$$\Delta V_{PO} = \frac{\Delta\omega_{PO}}{K_{VCO}} = \frac{1.8\omega_n(\zeta+1)}{K_{VCO}} = 1.8\omega_c\left(\frac{\zeta+1}{2\zeta}\right)\left(\frac{1}{K_{VCO}}\right) = 1.02\text{mV} \quad \textit{(eq. 88)}$$

In other words, *a 1 mV disturbance on the filter capacitors will cause loss of lock under these conditions!* It is probably not practical to design a board which keeps pickup pulses below 1 mV, and thus the pull-out condition imposes a practical upper limit on the sizes of filter capacitors.

This pull-out instability (loss of lock) and the resulting cycle slips show up in drives as an intermittent failure of the write clock and can be a problem both in theory and in practice.

We also note that there is a certain irreducible jitter (phase noise) in the VCO itself, and the use of very narrow loop bandwidths does not defeat this. The currents and voltages

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within the VCO are subject to thermal and shot noise, and this in effect makes small random changes in the switching thresholds for regeneration from cycle to cycle. This phenomenon has been described in a closely related type of oscillator in [7].

THIRD ORDER EXAMPLE USING THE VM5711 FREQUENCY SYNTHESIZER

We will treat the VM5711 Frequency Synthesizer with the following set of assumed specifications:

- (1,7) RLL code
- f_c = 20 kHz
- Input clock f_i = 16 MHz
- Three zones with NRZ data rates of:27 Mbits/s
  38 Mbits/s
  50 Mbits/s

The following equations define loop parameters for the VM5711:

$$I_p\ (\mu A) = 0.878 \times 10^6 (5/3 - X/32)/R_{ext} \qquad \textit{(eq. 89)}$$

$$f_o\ (MHz) = 0.23 \times 10^6 (2/3 + X/32)/R_{ext} \qquad \textit{(eq. 90)}$$

$$K_V\ (MHz/V) = 0.38 f_o \qquad (f_o \text{ in MHz}) \qquad \textit{(eq. 91)}$$

R_{ext} represents the value (in ¾) of an external user-selected resistor which sets the center frequency of the VCO.
X represents the value of an internal DAC which can be varied for each zone by means of a serial register (1 ð X ð 32).

Choose Rext

R_{ext} must be chosen to keep the VCO centered in its range for all three zones for values of X between 1 and 32. In the VM5711 the VCO runs at three times the NRZ clock frequency, and for (1,7) code we must have:

f_o = 81 MHz (zone 1)
f_o = 114 MHz (zone 2)
f_o = 150 MHz (zone 3)

The largest available frequency ratio for the DAC is (5/3 - 0)/(5/3 - 31/32) = 2.39, while the largest frequency ratio required for the zones is 150/81 = 1.85. If the DAC is centered over the VCO range, then:

$$0.23 \times 10^6 (2/3 + 16/32)/R_{ext} = (105 + 81)/2 \qquad \textit{(eq. 92)}$$

From this equation it follows that R_{ext} = 2.32 k¾.

Determine the DAC setting X for each zone.

$$X = 32\left\{\left(\frac{f_o R_{ext}}{0.23 \times 10^6}\right) - \left(\frac{2}{3}\right)\right\} \qquad \textit{(eq. 93)}$$

thus:
X = 5 (zone 1)
X = 15 (zone 2)
X = 27 (zone 3)

Determine divider settings M and N for each zone.[8]

M and N must be chosen for each zone such that:

$$f_o = \frac{2M}{N} f_i \qquad \textit{(eq. 94)}$$

The factor of 2 is needed because (1,7) code is being used. The CDSEL input for the VM5711 must be set HIGH, so:

$$81 = (2M_1/N_1)(16\ MHz) \qquad \textit{(eq. 95)}$$

$$114 = (2M_2/N_2)(16\ MHz) \qquad \textit{(eq. 96)}$$

$$150 = (2M_3/N_3)(16\ MHz) \qquad \textit{(eq. 97)}$$

There are a variety of solutions which will work, but because the VM5711 has a charge pump current which scales inversely with X and a VCO gain which scales linearly with X, the result is a loop gain which scales with M:

$$K = \frac{K_V I_p R}{B} = \frac{K_V I_p R}{2M} \qquad \textit{(eq. 98)}$$

Thus, we will want to fix B (M) for all zones. (Not all synthesizers have a charge pump current which scales with zone, so keeping M fixed with zone is not valid in general). Simplifying the equations, we have:

$$M_1 = (81/32)N_1 = 2.53\ N_1 \qquad \textit{(eq. 99)}$$

$$M_2 = (114/32)N_2 = 3.56\ N_2 \qquad \textit{(eq. 100)}$$

$$M_3 = (150/32)N_3 = 4.69\ N_3 \qquad \textit{(eq. 101)}$$

For the VM5711, M can range from 1 to 256 while N goes from 1 to 32. The following M and N values will work to synthesize exactly the data rates specified:

M_1 = 81; N_1 = 32
M_2 = 57; N_2 = 16
M_3 = 75; N_3 = 16

Note that M is not fixed as desired. This will cause a shift in ω_c, which will probably not be a big problem. The alternative is to adjust the data rates to something which will allow a fixed M. In general the user will have to make these trade-offs. A perfect solution may not always be possible for every design.

Calculate R, C_1, and C_2.

These values are the same for all zones, so some compromises may have to be made. Using the second-order approximation:

$$R = \frac{2\pi f_c B}{K_V I_p} = \frac{4\pi f_c M}{K_V I_p} \qquad \textit{(eq. 102)}$$

[8] Here we use M and N in place of the A and B of the earlier text to conform to the VM5711 data sheet.

$$C_1 = \frac{2\zeta^2}{\pi f_c R} \quad \textit{(eq. 103)}$$

Substituting for K_V, I_p, B, and R_{ext} we find:

$$R = \frac{2\pi(2320)(2M)f_c}{(0.38)(0.878\times10^6)[(5/3)-(x/32)]f_o} = \left(\frac{2.79}{(53.3-X)}\right)\left(\frac{Mf_c}{f_o}\right) \quad \textit{(eq. 104)}$$

Putting in the zone-dependent values X, M, and f_o we find:

R = 2.79 (81) f_c / (53.3 - 5) (81) = 0.058 f_c (zone 1)
R = 2.79 (57) f_c / (53.3 - 15) (114) = 0.036 f_c (zone 2)
R = 2.79 (75) f_c / (53.3 - 27) (150) = 0.053 f_c (zone 3)

Zone 2 will have the highest f_c for the same R. Usually the specified bandwidth f_c is the highest bandwidth desired, so if zone 2 is used to calculate R we have:

R = 0.036 (20 kHz) = 720¾ *(eq. 105)*

Rounding to the closest standard value we get R = 750¾.

Recalling the open-loop Bode plot, ω_1 is fixed by R and C_1 and hence the zone with the lowest f_c will have the lowest ζ and hence the smallest ϕ_R. Thus, zone 1 is used to calculate C_1.

$$C_1 = \frac{2\zeta^2}{\pi f_c R} \quad \text{where} \quad f_c = \frac{R}{0.058} \quad \textit{(eq. 106)}$$

If we let ζ = 0.7 then:

$$C_1 = \frac{2(0.7)^2(0.058)}{\pi(750)^2} = 0.032\,\mu F \quad \textit{(eq. 107)}$$

Picking a standard value closest to this, C_1 is set to 0.033 µF. C_2 is found assuming b = 11 and so C_2 = 0.0033 µF. We now calculate the phase margin ϕ_R and bandwidth f_c for each zone using:

$$\phi_R = \tan^{-1}\left(\frac{K(b-1)}{\omega_1 b}\right) - \tan^{-1}\left(\frac{K(b-1)}{\omega_1 b^2}\right) \quad \textit{(eq. 108)}$$

$$f_c = \left(\frac{K}{2\pi}\right)\left(\frac{b-1}{b}\right) \quad \textit{(eq. 109)}$$

These equations were derived using the third-order asymptotic model. For convenience all pertinent equations are shown below along with a tabulation of loop parameters for each zone:

$K = K_V I_p R/B$ $B = 2M$ $K_V = 0.38\ f_o$
$\omega_1 = 1/RC_1$ $b = 1 + (C_1/C_2)$ $\zeta = (1/2)(K/\omega_1)^{1/2}$
R = 750¾ C_1 = 0.033µF C_2 = 0.0033µF
R_{ext} = 2.32k¾ $I_p = 0.878 \times 10^6 (5/3 - X/32)/R_{ext}$ (µA)

Parameter	*Zone 1*	*Zone 2*	*Zone 3*
NRZ Data Rate (Mb/s)	27	38	50
f_o (MHz)	81	114	150
X (DAC setting)	5	15	27
N	32	16	16
M	81	57	75
K_V (MHz/V)	30.8	43.3	57
I_p (µA)	572	453	311
f_c (kHz)	11.8	18.7	12.8
ζ	0.71	0.89	0.74
DVPO (mV)	0.83	0.82	0.47
ϕ_R	51.9°	56.2°	53.1°

The results above show that the loop has adequate phase margin and a loop bandwidth within specifications for each zone.

Note: A chart like this can be generated for any zone-density drive design. It may be convenient to use a spread sheet program.

APPLICATION NOTES

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990812 APPLICATION NOTE August 12, 1999

INTRODUCTION

Several VTC ICs provide automatic gain control for the READ signal from a rigid disk drive. The method used has a number of features that optimize it for this application. The system has two thresholds for the signal amplitude, V+ and V-. When the output voltage V_S of the AGC amplifier satisfies $V_S > V+$ the gain is steadily reduced until $V_S = V+$ at which point the gain stabilizes (this is called a release transient). When V_S satisfies $V_S < V+$ and $V_S > V-$ the gain is steadily increased until $V_S = V+$ at which point the gain stabilizes (this is called an attack transient). When V_S satisfies $V_S < V-$ the gain is in a “hold” mode and changes only very slowly (due to device leakage currents). The latter feature is useful during periods of low or noisy signal when the gain would otherwise be driven to its maximum value resulting in a long recovery time when a normal signal level is restored.

AGC OUTPUT SAMPLING CIRCUIT

An AGC loop must sample the output and generate a suitable amplitude-control voltage which is fed back to the variable gain stage(s). The arrangement for sampling the AGC output amplitude is shown schematically in Figure 189. The signals V_S+ and V_S- (shown as solid and dashed lines) are the complementary outputs of the AGC amplifier. They are fed to four emitter followers, two of which have their emitters tied together to form a full-wave rectifier. Offset resistors R_L and R_H create two level-shifted replicas of the rectified signal. A set of comparators (1-4) generates level crossings which are then ORed in pairs and fed to an ***edge-triggered*** RS flipflop. The flip-flop outputs are then used to control two switchable nominally equal-valued current sources (CSUP and CSDN) which are connected to a capacitor C in a charge-pump arrangement. The capacitor voltage is then fed back (through a suitable buffer) to the amplitude control input of the AGC stage(s).

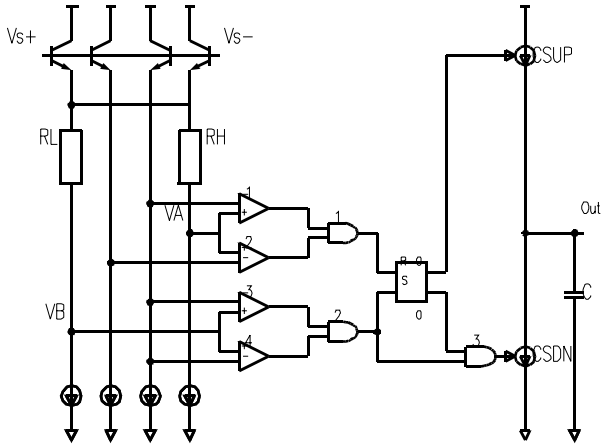

Figure 189 Output sampling and charge pump scheme for the AGC loop

The charge pump provides loop filtering for the AGC loop, and the value of C governs the response time of the AGC loop.

Figure 190 shows ideal circuit waveforms when the output amplitude is too high. Note that the duty cycle for the PUMP UP and PUMP DOWN waveforms is such that the PUMP DOWN current source is on for a much longer time than the PUMP UP source, so that the output amplitude will steadily ramp down under these conditions. Figure 191 shows the waveforms when the output amplitude is very close to the intended value. Now the PUMP UP and PUMP DOWN duty cycles are nearly identical and the output amplitude will stabilize. Note that when the data pattern contains a missing pulse both current sources are off, so that the AGC feedback is unaffected, i.e., the amplitude detection scheme senses only peaks (it “coasts” over missing pulses). The waveforms when V_S lies between V- and V+ are shown in Figure 192. Here the outputs of comparators C1 and C2 are always LOW, and the first rising edge on the C3 or C4 output will set the RS flipflop into a state where the PUMP UP current is on at all times, leading to a steady increase in the voltage gain and output amplitude until C1 and C2 begin to change state.

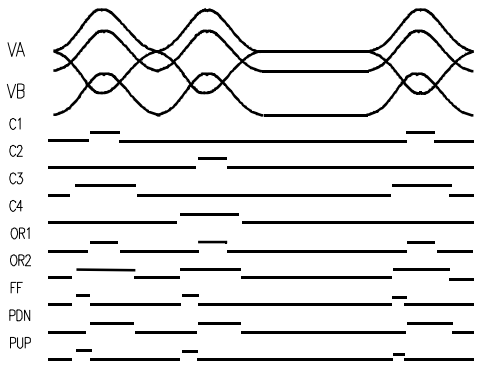

Figure 190 AGC sampling and charge pump operation when V_S substantially exceeds V+

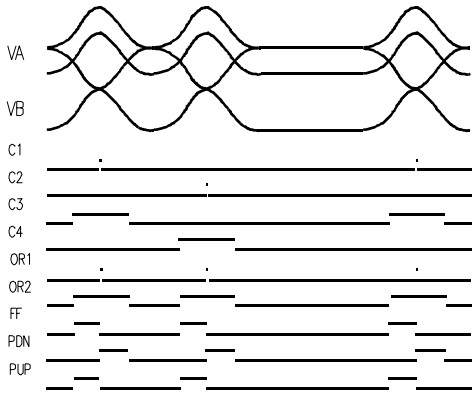

Figure 191 AGC sampling and charge pump operation when V_S exceeds V+ by only a small amount.

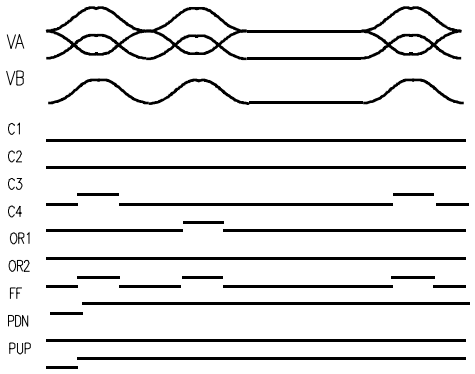

Figure 192 AGC sampling and charge pump operation when V_S lies between V- and V+

Figure 193 shows the waveforms when V_S is less than V-. Here none of the comparator outputs ever goes high, and both current sources remain off. This puts the AGC loop into a “hold” condition, similar to that which occurs during a missing pulse. The behavior of the gain under these conditions depends on the leakage currents present in the chip and on the board, and the resulting behavior is usually a slow rise in the AGC gain (i.e., leakage sources predominate over leakage sinks).

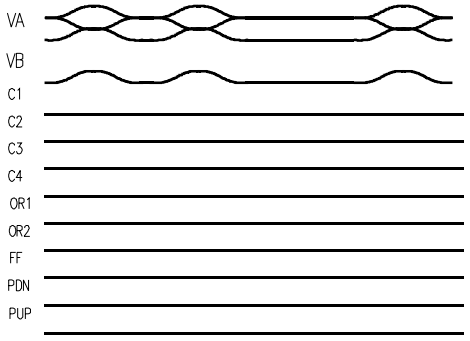

Figure 193 AGC sampling and charge pump operation when V_S is less than V-

THE IMPEDANCE SWITCH

The READ signal normally comes into the pulse detector chip as a capacitively-coupled differential signal. While this is convenient for avoiding offsets, etc., the relatively high impedance presented at the AGC amplifier input means that when there is a sudden change of input amplitude or waveform the recovery will be slow and the AG loop will take a long time to stabilize unless special measures are taken. In many of its AGC amplifiers VTC provides a ***fast acquisition*** mode to facilitate rapid stabilization of the AGC loop. It is controlled by an external logic signal (normally labeled FAQ) which, when asserted causes the input impedance to be lower by several-fold than its normal value.

A fast acquisition operation begins with a high-to-low transition of FAQ, which lowers the input impedance and reduces the output signal to zero. The output signal will remain at zero as long as FAQ is held low. Upon a low-to-high transition of FAQ the input impedance is rapidly restored to its normal value and a PUMP UP current source with a magnitude many times larger than the normal ***slow-tracking*** value switches on and rapidly brings the output amplitude within the control range. When the output amplitude reaches its nominal value the large PUMP UP current source is automatically turned off by circuits within the chip.

ADJUSTING THE AGC PARAMETERS

Most of the AGC parameters, such as minimum and maximum gain, attack and release time, AGC loop response time constant, etc. can be adjusted by suitable choice of off-chip discrete resistors and capacitors. The details differ for various chips, and are covered in the corresponding data sheets.

The convention for the control action is when a logical high is generated the current is ON and with a logical low it is OFF.

990812 APPLICATION NOTE August 12, 1999

This note provides a basic overview of the general operation of VTC's serial loader programs.

Serial Loader programs are used to load serial registers, view the current contents of serial registers, and retrieve previous register configurations that have been saved with a Serial Loader program.

All of the parameters needed for viewing, loading, or evaluating a serial register configuration can be easily accessed from the main Serial Loader screens.

The Serial Loader programs serve three purposes:

- *It allows easy selection and viewing of serial register parameters.*
- *It allows a user to modify serial register parameter values.*
- *It allows a user to save register configurations as files.*

SERIAL LOADER PROGRAM PARAMETERS

All serial register parameters that affect the operation of the particular part are generally accessible from the Serial Loader program.

Viewing Register Parameters

The present settings for the serial register parameters are displayed on the main Serial Loader screen. This screen is generally divided into three distinct regions:

One upper portion of the screen contains two columns. The WRITE column displays the values that would be written to the serial registers if the WRITE function were selected. The READ column displays the values that have been read from the serial registers if the READ function has been selected.

Another upper portion of the screen displays the multi-bit register fields that are most likely to be modified. The serial loader program provides a slide-bar for easier adjustment of these parameters without manually adjusting a series of individual bits.

The *bottom portion of the screen* displays the specific contents of a given register (the register number is identified in a label box centered above the individual values). Each of the individual bits in the serial registers can be accessed from this portion of the screen.

Selecting Which Register is Displayed

There are several methods of selecting which register to display at the bottom of the Serial Loader screen. The individual bits for the selected register are then displayed and accessible.

1) Select the register number in the WRITE column at the far left side of the screen (with the left mouse button).
2) Select the register contents in the WRITE column.
3) Select a multi-bit parameter name in the upper half of the screen. The contents of the register associated with this parameter will be displayed.

Setting Register Parameters

Register parameters can be set in two ways:

40) After selecting a register for display at the bottom of the Serial Loader screen, toggle the appropriate bits by selecting them with the left mouse button.
Note that the register contents will also change in the WRITE field in the left portion of the screen.
Any multi-bit parameter setting on the right hand side of the screen which is affected by the bit change will also change.

41) Select one of the change arrows in the multi-bit parameter section in the right portion of the screen. Changing a multi-bit parameter value by selecting the right/left slide bar arrows will change the contents of the WRITE field for the register containing the bits for that parameter. If the affected register is displayed in the bottom box the appropriate bits will also change as the parameter is varied.

Note: Selecting the **W/R** (Write/Read) button on the bottom left side of the screen will load the serial registers with the serial loader screen contents and read them back to determine if they loaded properly. If the register contents on readback do not match the written values, the background behind the register(s) in question will change from blue to red.

Menu Bar Definitions

The following options are available from the menu bar at the top of the Serial Loader screen.

File

Allows saving of current serial loader and serial register contents and the quick retrieval and loading of previously-saved register contents (through the **Open**, **Save**, and **Save As** options) and a means to exit the program (with the **Exit** option).
Once a file has been recalled to the Serial Loader screen the remaining four menu options may be useful:

W/R

Write/Read. (Shortcut key - F6)
Writes the values currently displayed on the Serial Loader screen to the serial registers and immediately reads back the contents of the registers.
If the values in the WRITE field (far left column on screen) do not match the register the values read back from the registers (the READ column), any registers with non-matching values will show up with a red background in the READ field.
If the values match the read field will maintain a blue background.

APPLICATION NOTES

Write:

(Shortcut key - F7)
Writes the values displayed in the WRITE column to the serial registers.

Read:

(Shortcut key - F8)
Reads back values set in the serial registers to the READ column at the left side of the screen.

Ports:

Note that these port options may not be available on all versions.

H278, H378, H3BC

These are the three standard parallel port addresses. The customer should verify which address their system is using.

H280

The Quatech card.

Test Port

This is a form to test if the computer is talking to the parallel port correctly. This feature eliminates one possibility from the equation when troubleshooting serial port problems.

HELP [1]

Bit Map

Allows quick location of the register containing a particular bit.
Select the button representing the first letter of the name of the particular bit you wish to locate. A list of bit names starting with that letter will be displayed. Selecting the desired name will bring up the contents of the appropriate register at the bottom of the screen.

EXIT [1]

Save Before Exit

Allows register settings to be saved to a file for future reference before the Serial Loader program is closed. Specify the file name and directory path.

Exit Without Save

Immediately closes the Serial Loader program without saving register contents to a file.

Button Definitions

READ

Reads the serial register contents and displays them in the READ column in the left portion of the Serial Loader screen. If the values read back do not match the values previously written by the serial loader the background for registers in question changes from blue to red.

W/R

Writes the current Serial Loader values to the IC registers and performs a read to verify to verify the correct values were written (see above).

Note:

In some Serial Loader programs, Help is available (descriptions of labels and buttons) by pressing the right mouse button.

[1] Note that these menu bar options may not be available in all Serial Loader programs.

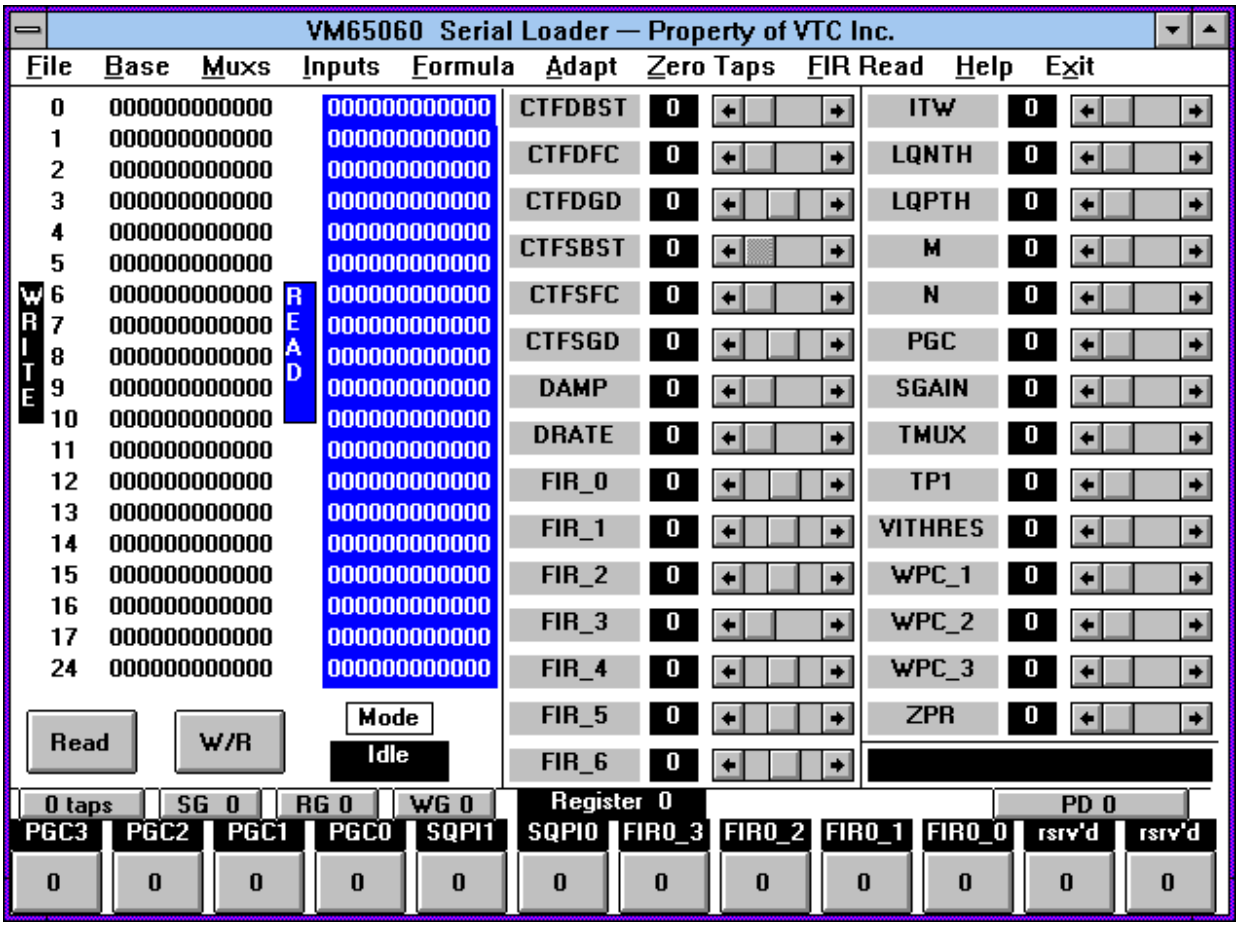

Figure 194 The Main Screen of a Serial Loader program.

ADAPTIVE FIR FILTER PARAMETERS

The following parameters affect the operation of the VM65015. The parameters are set through the serial registers.

Definitions

AE **Adaption Enable.**
(Not displayed on the Adaptive FIR Control screen.) Controls whether adaption is performed. Logic '1' equals adaption enable.
This bit is activated automatically when a "Run" command is issued from the Adaptive FIR Control screen.
Note: This bit can be accessed through the Serial Registers, but it must *not* be toggled during an adaption cycle.
The Adapt Hold (ADPHLD) pin allows adaptation to be temporarily halted. When AE = 1, a high on the ADPHLD pin temporarily halts adaptation while a low allows adaptation to occur.

DZ **Dead Zone length.**
Specifies how many update samples are required in either direction to cause the tap to be updated in that direction.

INTL **Integration Length.**
Selects the number of samples to integrate over for each tap weight (12, 15, 18 or 21). One sample is one clock cycle.
Note: See Figure 195 for a depiction of the interrelationship between Dead Zone and Integration Length settings.

ITW **Initial Tap Weight.**
Selects which tap begins the first adaptation cycle when a new read cycle is started. Table 248 describes the order of adaption for each DAC setting.
Note: All subsequent adaptation cycles use the TWR setting (see Table 249 and Figure 196) to determine the order of tap cycling.

Table 248Order of Adaption with TWR = 0

DAC	*ITW*	*Order of Tap Weight Adaption*								
00	0	0	4	1	3	0	4	1	3	...
01	4	4	1	3	0	4	1	3	0	...
10	1	1	3	0	4	1	3	0	4	...
11	3	3	0	4	1	3	0	4	1	...

TWR **Tap Weight Rollover.**
Determines how many of the taps are adjusted. Table 249 describes which taps are adjusted.Setting the DAC to 00 adjusts all 5 taps (0 through 4).

Table 249Taps Adjusted with TWR Settings

TWR DAC	*Taps Adjusted*			
00	0	4	1	3
01		4	1	3
10			1	3
11				3

Note: Taps which are not adjusted are still active but held at their pre-adaption values.

SYMC Symmetry Control.
Determines which if any of the taps will be symmetrically adjusted:

Table 250Symmetrically Adjusted Taps

SYMC DAC	*Taps Adjusted Symmetrically*
00	1 and 3
01	0 and 4
10	1 and 3, 0 and 4
11	none

SUGGESTED INITIAL SETTINGS

Tap Weights
To set the desired tap weight, select "Set Weights." from the main menu bar.
Setting the tap weights to their center positions on the Serial Loader screen (0,0,15,0,0) does not result in flat response of the FIR filter. Tap weight settings for flat response are (0,16,15,16,0).

DZ
10 or 11 (65% or 80%, see Figure 195)

INTL
10 or 11 (18 cycles or 21 cycles, see Figure 195)

ITW
10 (tap 4, see Table 248)

TWR
10 (taps 1 and 3, see Table 249)

SYMC
00 (taps 1 and 3, see Table 250)

APPLICATION NOTES

DVHS ADAPTATION

Two methods are available to select default values for FIR Taps. One method employs historical data to set a default the other relies on test results to provide specific settings for each DVHS deck. The following examples describe each of the methods.

Historical Data Use

Optimize each DVHS deck for FIR during early builds. Histogram the results from each deck and use the mean settings as defaults for all DVHS decks.

Deck Specific Testing

This method is probably best suited for automated testing and adjustment of FIR taps on a production line basis. This method guarantees optimized FIR defaults for each DVHS deck.

Performing this routine as a periodic maintenance function is recommended throughout the life of the deck. FIR taps should be periodically adjusted to accommodate head degradation.

Each step is the adaptation process is numbered and explanations are provided where appropriate.

Adapting on Each Playback

When the play button is pushed, the deck aligns the heads on-track by adjusting the scanner speed for maximum amplitude from the preamplifier. After acquiring tracking, adaptation can be enabled. The recommended sequence to follow in adapting is listed below.

Note: Do not Adapt while searching for on-track.

80) Set the ADPHLD pin high.
    Adaptation should only be attempted in the main code area of the data. See Figure 197 for an example of proper timing.

81) Set Dead Zone to 11.

82) Set Integration length to 11.
    Setting the Dead Zone and Integration length to 11 provides the most stable adaptation. These settings will guarantee convergence and holding of proper FIR tap settings. See Graph

83) Set Symmetrical to 00.
    Setting Symmetrical to 00 results in symmetrical adaptation of FIR Tap pairs (1 & 3,0 & 4). This setting provides a check-and-balance of the adaption decision which results in a more stable adaptation.

84) Set Initial Tap Weight to 10.

85) Set Tap Rollover Weight to 10.
    Setting ITW and TRW to 10 causes only Taps 1 and 3 to adapt (because Taps 0 and 4 are shared between Head 0 and 1). Data shows Taps 0 and 4 should be set to 0 and left, as this selects a flat response and provides independent adaption for each head.

86) Set Adaptation Enable to 1 and the other register values to default settings.
    This allows the ADPHLD (adapt hold) pin to control adaptation.

87) Toggle the ADPHLD pin after tracking is acquired for a short time (10 to 100 tracks). Then hold the ADPHLD pin high for the duration of playback.
    This keeps the internal noise to PRML at a minimum and prevents doubling of the Bits in Error. (The BER doubles when the adaption must follow off-track and then on-track). When adaption is on errors are detected both when going off-track and when returning on-track. When adaption is off, errors are detected only when going off-track.

Note: An average is preferred, but is not absolutely necessary. However, an average eliminates stopping that may result from an off-track or bad adaption.

Checking ECC Events as a Measure of Optimal Adaptive FIR Tap Settings

To establish the threshold of ECC events requires a small sample build of DVHS decks. Use the sample to optimize all channel parameters (including FIR tap settings) and to collect data on ECC events.

1) The ECC event threshold should be set close to the least acceptable performance level (with enough margin to guarantee performance). The risk with this method is not being able to achieve the ECC threshold level. A routine can protect against this (e.g., a very poor quality tape) happening.

2) Initiate Adaptation of the FIR. Stop adaptation before checking against ECC threshold. If the ECC results are acceptable retain FIR settings. If not repeat this step.

IMPORTANT NOTES

- Do *not* attempt to change serial register settings during an adaption cycle.
- It is important that random data be used as a training sequence. Convergence problems for the LMS algorithm may result if random data is not used.
- Proper selection of Dead Zone (DZ) and Integration Length (INTL) parameters can bring about rapid adaption or slow, highly stable tracking of system changes.

- Short integration lengths and narrow dead zones will allow for more rapid adaption at the risk of non-optimal adaption.
- Wide dead zones can prevent convergence of the adaption routine (particularly with short integration lengths).
  This occurs because DZ sets the number of update commands in a given direction before an update can occur.

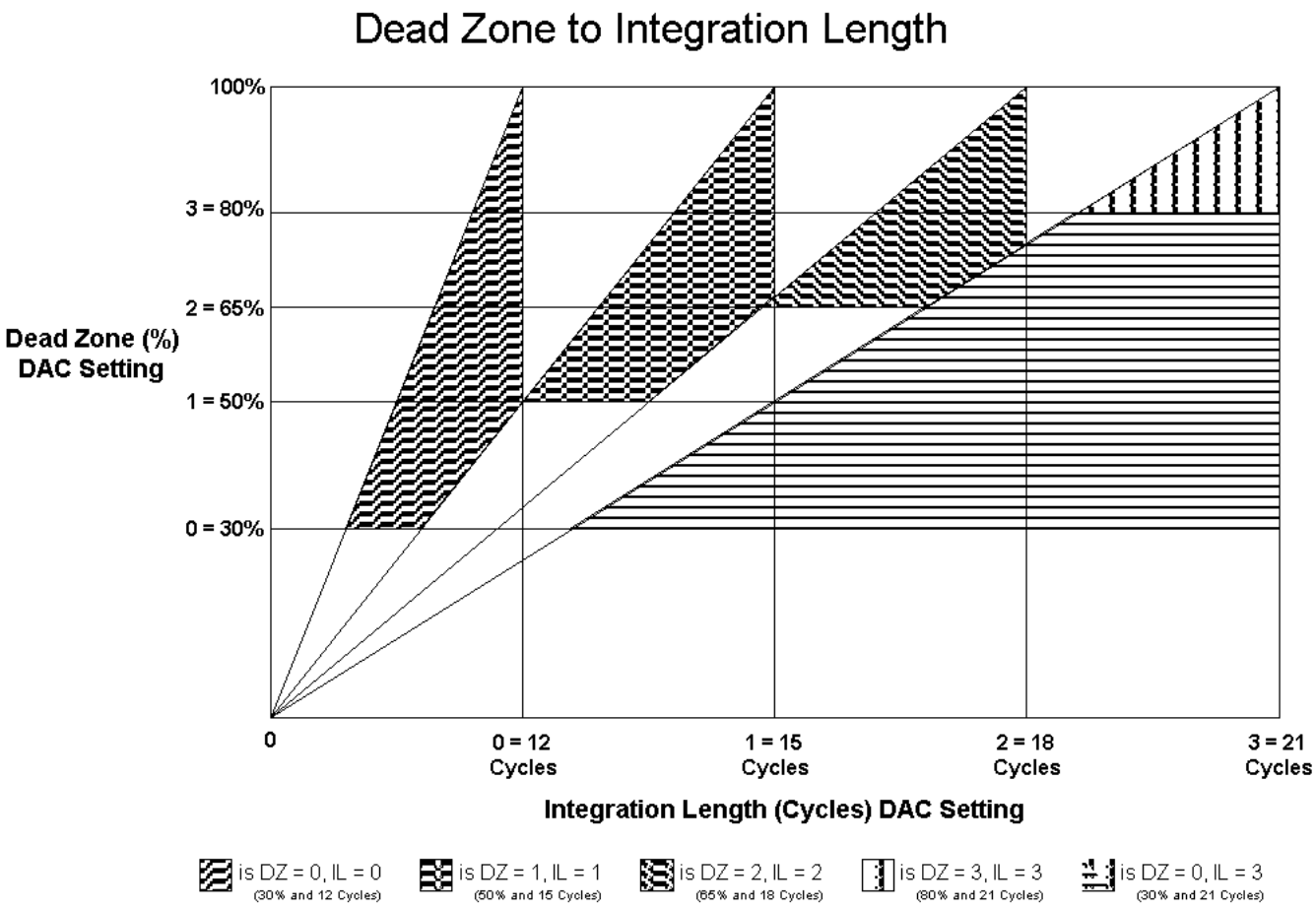

Figure 195 Interrelationship of Dead Zone % Settings and Integration Length Cycles

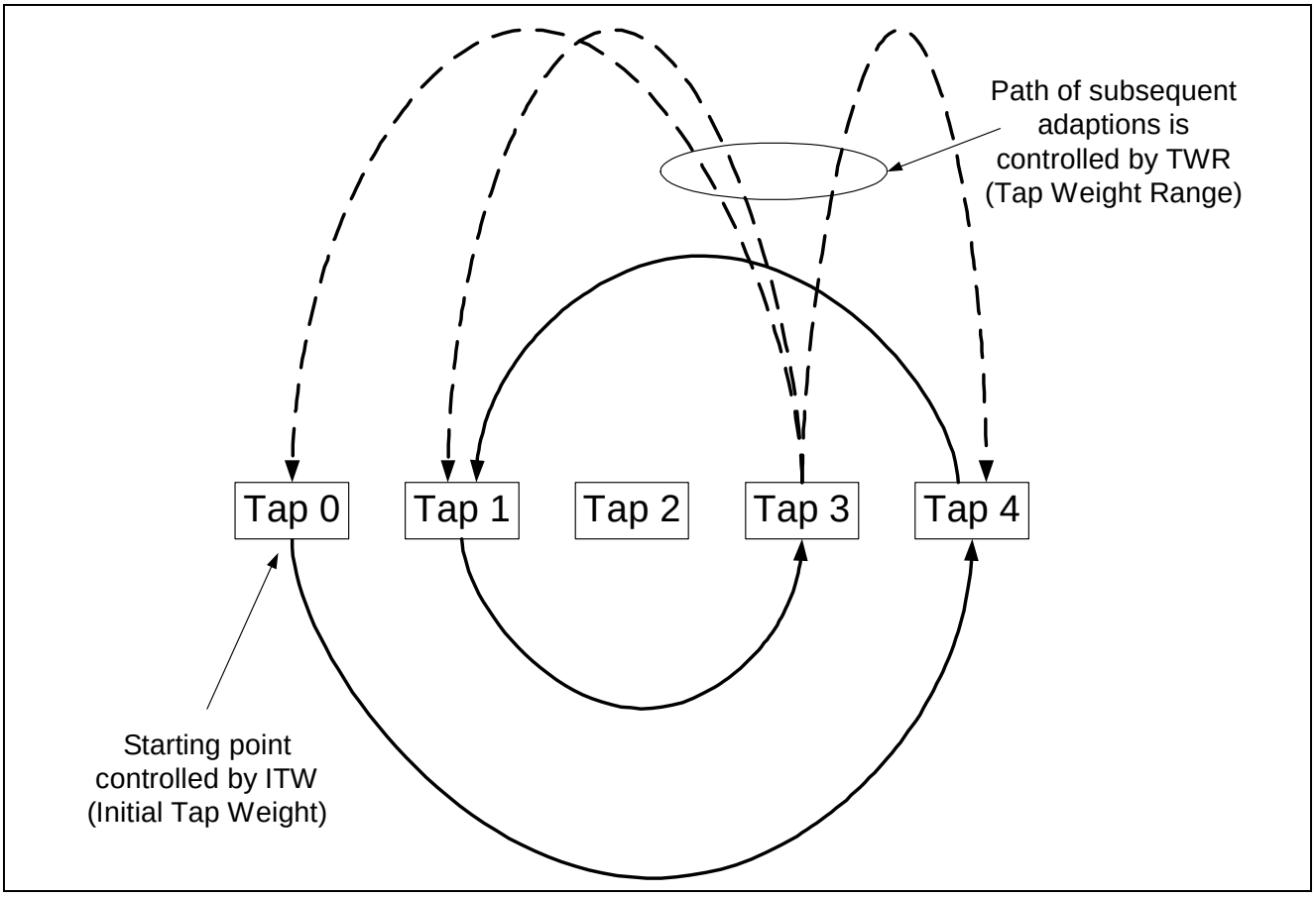

Figure 196 Tap Adaption Progression

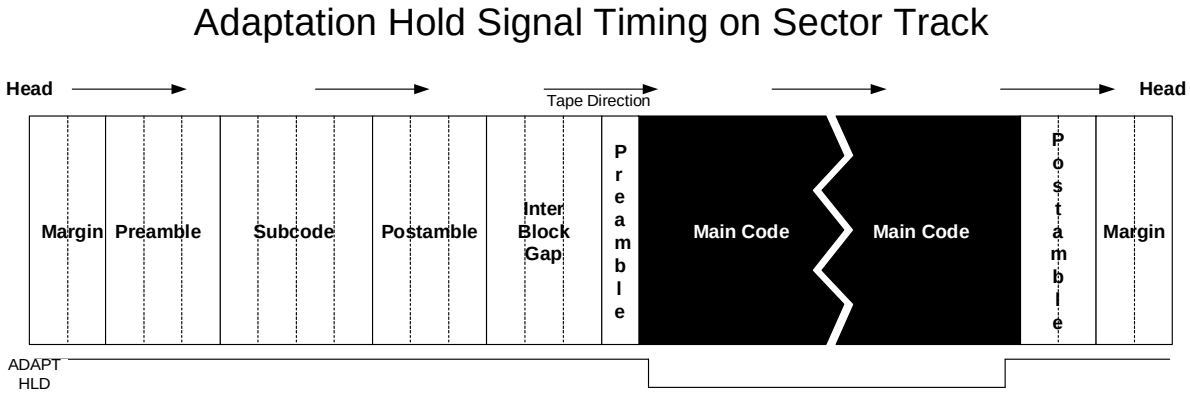

Figure 197 ADPHLD Timing Limiting Adaption to Main Code

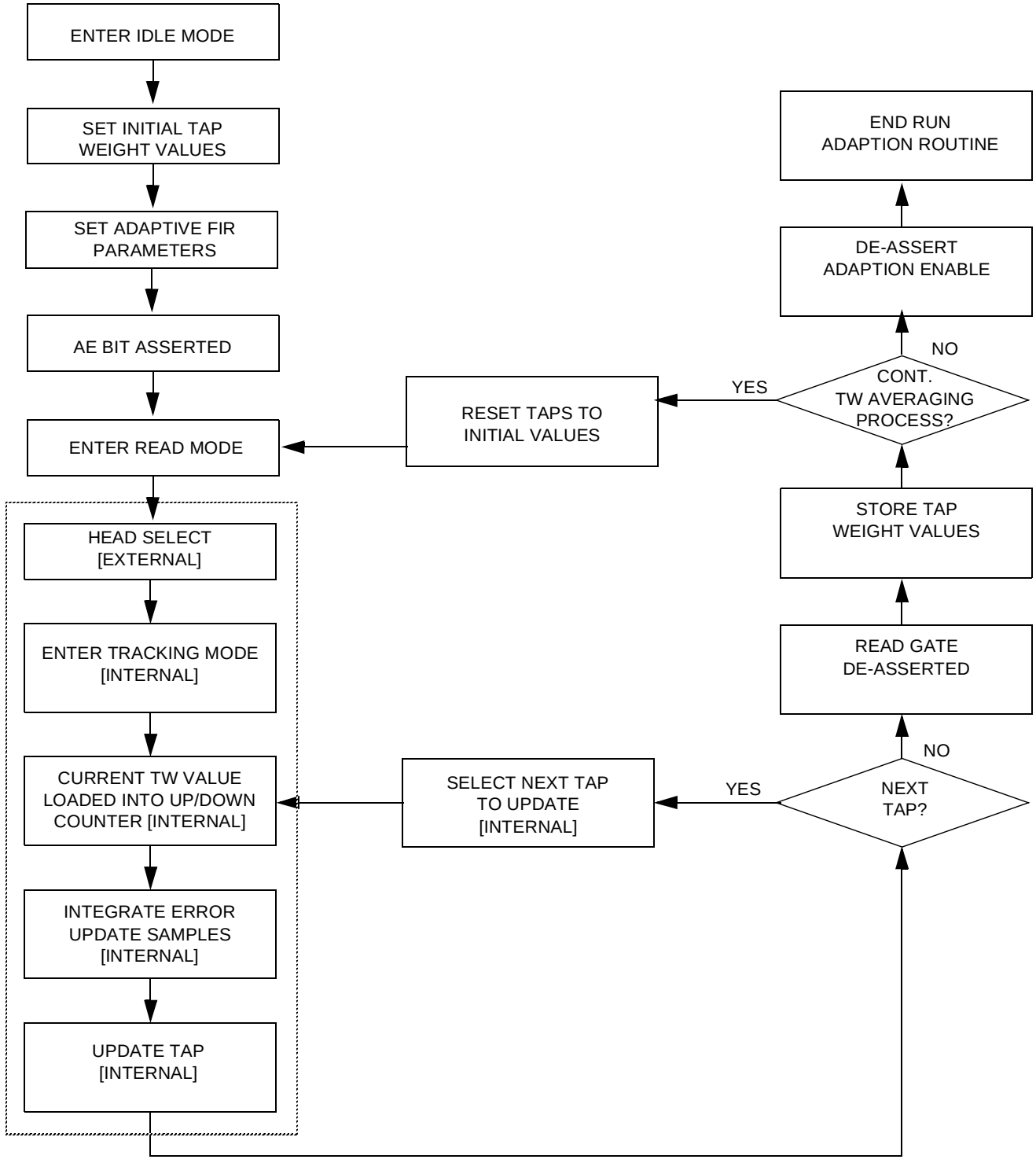

Figure 198 Run Adaption Routine

FLEX CIRCUIT LAYOUT GUIDELINES

The following statements describe basic principles that should be followed when designing flex layouts.

3) *Bypass capacitors should be as close to the IC as possible* to minimized decoupling of the capacitor from the circuit at high frequencies due to series inductance.

4) In certain high Z input preamps:
An external Ac coupling capacitor sets the low frequency pole of the system. Because this capacitor is at an extremely low impedance node, any inductance in series with capacitor will set a high frequency RL pole which can limit the upper cutoff frequency of the preamp.

For instance, if $F_C=R/2\pi L$, R=8Ω (the node impedance) and L=10nH (the node inductance), F_C would then equal 127MHz. Note that there can easily be several nanoHenries in the bond wires alone.

The bottom line is that *these leads need to be kept as short as possible and as wide as possible to minimize L and maintain the bandwidth of the system*.

5) In high Z input preamps:

The equivalent input circuit is a 2-pole circuit, meaning it will resonate and peak. The amount of peaking will be proportional to the resistive damping involved. The L/C ratio will also affect the amount of peaking; the higher the ratio of series inductance to parasitic capacitance the greater the peaking.

Parasitic inductance and capacitance must be minimized. This will minimize peaking of the frequency response and maintain bandwidth.

6) *Power distribution connections should be kept as short and wide as practical to minimize inductance*. This applies to V_{CC} and V_{EE} as well as Ground.

7) Most readers have emitter-follower outputs. These are prone to oscillation if certain precautions are not taken:

42) *Do not try to drive large amounts of capacitance* (this includes certain probes without 10:1 dividers).

43) *Pay particular attention to the emitter-follower AC return path*. For an NPN emitter-follower this is through V_{CC}, **not ground**. Proper bypassing of V_{CC} is extremely critical.

Larger values of bypass capacitance do not necessarily mean more effective bypassing.

At high frequencies (where the follower is more likely to become unstable) series inductance in the capacitor degrades its effectiveness.

Smaller capacitor values will tend to have less series inductance and may actually be more effective. It is again important that the bypass capacitor be as close to the preamp as possible.

8) *Symmetry of RDP and RDN lines should be preserved* or the common mode rejection ratio (CMRR) at the input to the channel IC will be compromised.

9) In some cases signals induced on control lines can find their way back to the inputs. Therefore *RDP and RDN should be positioned away from control lines*.

10) In certain low Z input preamps:

A compensation capacitor is connected across the bases of the input differential pairs. Any noise picked-up by the capacitor will be transferred directly to the input of the reader. Any series resistance introduced at this point will also result in an additional thermal noise component introduced at the input. *Keep the leads to this capacitor as short and wide as practical*.

11) When “guarding” RDP and RND lines, care must be exercised so that the guard lines do not mutually-couple extraneous noise into RDP and RDN.

This means the *guards lines should be ground on only one end* (usually the preamp end).

VTC Inc.
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DEMYSTIFYING NOISE SPECIFICATIONS FOR DATA STORAGE PREAMPLIFIERS

990812 **APPLICATION NOTE** August 12, 1999

INTRODUCTION

Some of the most confusing and misunderstood preamplifier specifications are those relating to noise. This is because there are a number of noise contributors in any preamplifier/head system and there are a number of ways to combine them into a specification which represents the total noise performance of the system. Complicating this is the fact that the units involved can be somewhat non-intuitive. The end result is that the specification often does not adequately represent the performance of the system (or the specification is misconstrued to mean something it doesn't).

This note attempts to provide the underlying principles necessary to interpret noise specifications and outlines some of the common pitfalls when examining or creating noise specifications for data storage head preamplifiers (particularly MR preamplifiers).

TYPES OF NOISE

Thermal Noise

All resistive elements generate noise due to thermal agitation of electrons. This is also called "Johnson noise." Thermal noise generated by a complex impedance is due strictly to the "real" or resistive component of the impedance. Pure reactances do not generate thermal noise!

Thermal noise is "white noise." White noise has a constant noise power for a given bandwidth anywhere in the frequency domain. In addition, the probability density function for instantaneous values of white noise voltages is Gaussian and therefore white noise is also called Gaussian noise. Thermal noise voltage is defined as follows and has units volts/$\sqrt{Hz}$.

$$v_t = \sqrt{4kTBR} \qquad \textit{(eq. 204)}$$

v_t = rms thermal noise voltage in volts/$\sqrt{Hz}$
k = Boltzman's Constant (1.38 x 10^{-23} joules/ degKelvin)
T = Absolute temperature in degrees Kelvin
B = Noise bandwidth in Hz
R = Resistance in Ohms

Thermal noise is usually responsible for setting the lower limit on the amplifier noise floor. Note that if we increase the resistance value of an MR head the thermal noise presented to the input of the preamp is increased in proportion to the square root of the resistance. The noise power (often quoted in specifications) is the noise voltage squared or v^2/Hz. Therefore the noise power increases in direct proportion to resistance.

Note that this only applies to thermal noise generation. There are other factors affecting noise that can be affected by changing the head resistance. These will be discussed later.

Shot Noise

Shot noise is due to current flow across a potential barrier such as a semiconductor junction.

$$I_{sh} = \sqrt{2qI_{dc}B} \qquad \textit{(eq. 205)}$$

I_{sh} = rms shot noise current
q = Electron charge
I_{dc} = Average DC current through potential barrier
B = Noise bandwidth in Hz

Shot noise also has a Gaussian distribution and is strictly a function of DC current through the device.

Flicker Noise or 1/f Noise

Although the physical mechanisms causing flicker noise are not well understood, it is believed to be caused by discontinuities in the conducting medium. The name "1/f noise" is derived from the fact that below a certain "1/f" corner frequency the noise voltage is proportional to 1/f.

Flicker noise is usually not a factor in bipolar MR preamps because the lower corner frequency of the MR preamp is above the 1/f corner frequency. In MOS preamps the 1/f corner frequency can extend out past 1 MHz, therefore in these preamps it is very important to understand total noise power taken over the entire bandwidth and the spectral distribution.

Popcorn or "Burst" Noise

Popcorn noise is due to manufacturing defects in materials and is usually not a significant concern in modern processes.

NOISE SPECTRUM

Noise defined at a particular frequency has the units volts/$\sqrt{Hz}$ or amps/$\sqrt{Hz}$. This is frequently called "spot noise." If we plot spot noise vs. frequency we obtain the "noise density" or "spectral density function" (SDF). If we define a bandwidth of interest the "total rms noise" is the area under the spectral density function curve within that bandwidth. The reason the units v^2/Hz are commonly used is apparent here -- when calculating the total noise the Hz units cancel out and we are left with v^2 or total noise power. (Note that unless the bandwidth used to calculate the total noise power is known, the number is quite meaningless.)

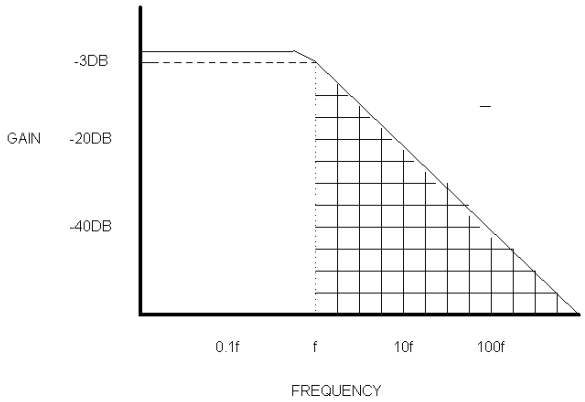
The main point here is that noise can (and does) vary with frequency. What is important is the total noise power within a given bandwidth and how that noise is distributed with respect to frequency. A spot noise measurement only tells us about a single point on the noise floor. In most cases it is specified at the lowest point on the noise floor. It tells us little about noise performance over the bandwidth of interest. When looking at noise specifications it also pays to look carefully at units (v/$\sqrt{Hz}$ vs. v^2/Hz can describe the same thing but yield quite different numbers).

Remember that the same units can be used to describe a number of different measurements; it is important to understand how a particular specification number was derived!

APPLICATION NOTES

NOISE BANDWIDTH

A common mistake when calculating thermal noise, shot noise or total noise is to assume that the -3db bandwidth defines the noise bandwidth. The following figure shows that this will not include a significant portion of the area under the transfer function curve.



The shaded area represents the area under the transfer function curve that is not accounted for when the -3db bandwidth is used to calculate the noise voltage (such as when calculating thermal noise passed through an MR preamplifier with a finite bandwidth). As can be seen from the graph, if we use the -3db bandwidth in our calculations the calculated noise will be in error. The area under the curve beyond the -3db point must be included. If the roll-off is the result of one or more poles, the -3db bandwidth can be multiplied by a correction factor as follows:

Roll-off in DB/Octave	*Multiply -3db Bandwidth by*
6	1.57
12	1.22
18	1.15
24	1.13

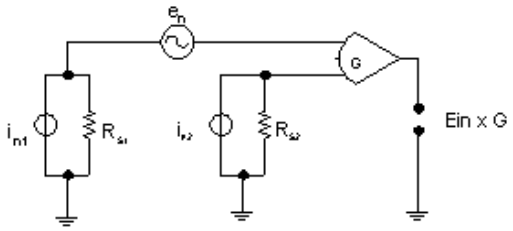
Note: This assumes the gain is flat out to the -3db point and Gaussian noise. In the case of MR preamps the SDF may not be flat and the high frequency roll-off will not be well defined. In these cases integration or “counting the squares” must be used to calculate the area under the curve and thus the total noise.

AMPLIFIER NOISE SOURCES AND EQUIVALENT INPUT NOISE

Noise sources within an amplifier can be modeled as an equivalent noise generated at the input of an amplifier. If the total noise at the output of the preamplifier is known the Equivalent Input Noise (EIN) can be determined by dividing by the amplifier gain. The total noise seen at the output of the amplifier can be caused by voltage or current noise. The EIN figure does not tell us anything about the contribution of voltage noise vs. current noise to the total noise at the output of the preamplifier.

Each gain stage has a certain amount of voltage noise and current noise. As it turns out, in most amplifiers the first stage is the predominant noise generator due to the noise being gained up more than the noise from later stages.

The following figure shows a differential amplifier and how its noise sources can be modeled as equivalent current and voltage noise generators at the input.



Noise voltages add in rms fashion. If we make the assumption that the noise sources are uncorrelated then the equivalent rms input noise due strictly to the amplifier is:

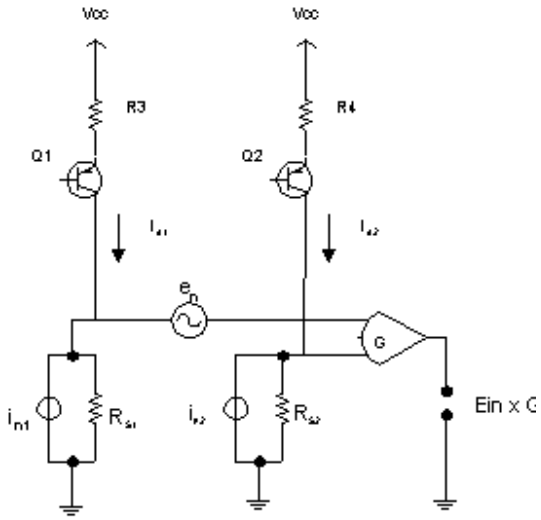
$$EINa = \sqrt{(i_{n1}^2)(R_{s1}^2) + (i_{n2}^2)(R_{s2}^2) + e_n^2} \qquad \textit{(eq. 206)}$$

Taken one step further, the thermal noise from the source resistances can be accounted for giving the equivalent rms input noise for the head/preamp system:

$$E_{INs} = \sqrt{(i_{n1}^2)(R_{s1}^2) + (i_{n2}^2)(R_{s2}^2) + e_n^2 + v_{t1}^2 + v_{t2}^2} \qquad \textit{(eq. 207)}$$

v_{t1} and v_{t2} represent the thermal noise from R_{s1} and R_{s2} respectively

In the case of a differential MR preamp, R_{s1} + R_{s2} represent the MR head resistance. In addition there are two other noise sources we must contend with in the form of bias current sources for the head. These noise sources can be modeled as two additional current noise sources as shown below:



The total rms equivalent input noise for a differential MR preamp can be described by:

(eq. 208)

$$E_{INmr} = \sqrt{(i_{n1}^2)(R_{s1}^2) + (i_{n2}^2)(R_{s2}^2) + e_n^2 + v_{t1}^2 + v_{t2}^2 + (i_{s1}^2)(R_{s1}^2) + (i_{s2}^2)(R_{s2}^2)}$$

APPLICATION NOTES

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Multiplying this number by the amplifier gain gives the noise voltage at the output. This number does not tell about the spectral distribution, but knowing this equation provides insight into the contribution of the various noise sources.

There are several methods of determining the amplifier noise contribution. For instance, if R_{s1} and R_{s2} are made extremely small, the contributions of the noise currents and thermal noise sources are eliminated allowing easy determination of the amplifier noise voltage contribution. Knowing the voltage contribution simplifies determination of the noise currents. Another method to determine the noise currents involves varying the source impedances and noting the difference in E_{IN}. In the case of MR preamps, it would be better to employ the latter method since making the source resistance small means shorting the inputs. In many cases this will seriously disturb the stability of the preamp or cause the bias current sources to inject additional noise into the inputs. It is important to note that the additional bias current noise sources are not accounted-for in some MR preamp specifications.

Although reactances do not generate thermal noise themselves, a noise current passed through a reactance will generate a noise voltage. If reactances are present at the input of the preamplifier the $i_n^2R_s^2$ and e_n^2 terms will become frequency-dependent (remember that only the real parts of any impedance affect thermal noise and therefore those terms are not directly affected).

This means that any reactances at the input, parasitic or otherwise, will become factors in the determining EIN and the noise spectral distribution.

NOISE IN ACTIVE DEVICES

In order to fully understand which noise parameters are important in any given application, it is necessary to understand a few key points about what influences noise performance in an active gain stage. Whether voltage noise or current noise predominates is influenced by the active device type (bipolar or MOS), current magnitudes, transconductance, beta, base spreading resistance and gate source capacitance. It is very important to understand which type of noise predominates when examining MR preamp specifications. There are trade-offs which may result in voltage noise being minimized at the expense of current noise or vice versa. For instance, MOS preamps will have very low input noise current but may have substantially higher input noise voltage. Per the above equation for E_{INmr}, even though the current noise may be lower, the total E_{INmr} may be higher.

OPTIMUM SOURCE IMPEDANCE

As can be seen from the equation for E_{INs}, for any combination of input-referred voltage noise and current noise there is an optimum value of source resistance. In most cases this is equal to e_n/i_n. In the case of MR preamplifiers an increase in head resistance will not only increase thermal noise contributed by the head but will increase the noise contribution due to current noise. If there is parasitic inductance the noise will increase with frequency in proportion to the inductance. It would seem on the surface that one would want the lowest input noise current possible. HOWEVER, lower input noise current may come at the expense of input noise voltage. Therefore noise current, noise voltage, thermal noise and parasitic reactances all need to be considered when examining specifications.

SIGNAL TO NOISE RATIO AND NOISE FIGURE

In many situations what is ultimately important is the dynamic range between the noise floor and the signal level. Signal to noise ratio usually denotes the ratio of the maximum signal the gain stages can handle divided by the noise floor. If the performance of an MR preamplifier is specified in terms of signal to noise ratio we need to know the absolute noise floor and the signal level to determine the usefulness of the preamp in any given application. For example, if the noise floor is extremely high and the preamplifier accepts unusually high input levels it would be capable of high signal to noise ratios. But it would be useless in our application since we are working with relatively low level signals and need a low noise floor to achieve reasonable signal to noise ratios.

Pay attention to units! If the noise measurement is noise power, the signal measurement should also represent signal power. Also, pay attention to what constitutes the noise measurement in the bottom term -- is it a spot noise measurement or total noise power taken over some bandwidth. Frequently this is not spelled-out in the datasheet. Sometimes “Noise Figure” or “Noise Factor” is used to specify the noise performance of an amplifier and its signal source. This is the ratio of noise power at the output to the noise power at the input due to the thermal noise of the source resistance. This is a figure of merit for how much noise is added by the amplifier. If no noise is added then the noise factor will be “1”. There are a number of shortcomings to this method of specifying noise. The main one is that it is not valid for reactive sources. In addition, in some cases it is possible to increase the source resistance, thereby lowering the noise factor. However, the total EIN may be increased due to the increase in thermal noise.

SUMMARY

When examining noise specifications keep the following points in mind:

12) Noise specifications without the bandwidth over which the measurements were taken are useless.
13) Spot noise measurements are often used to specify the magnitude of the noise floor. This method of specifying the noise can be misleading since it does not describe the noise performance over the total bandwidth.
14) Make sure that any equivalent input noise specification includes all the relevant noise sources.
15) Just because an amplifier is specified with a lower voltage or current noise at the input does not mean that the total noise seen at the output is less. All noise sources must be considered together.
16) Pay special attention to units.

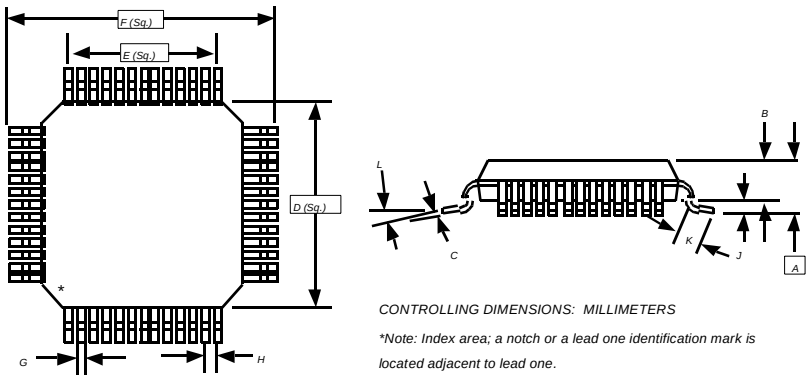
7 PACKAGING AND ORDERING

Packaging and Ordering

Plastic Quad Flatpack (PQFP)

52-LEAD PQ10 (10 x 10 x 2.0mm, 1.60mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.085 nom	0.093	2.15 nom	2.35
B	0.077	0.083	1.95	2.10
C	0.005	0.009	0.13	0.23
D	0.400 BSC		10.00 BSC	
E	0.307 REF		7.80 REF	
F	0.528 BSC		13.20 BSC	
G	0.009	0.015	0.22	0.38
H	0.0256 BSC		0.65 BSC	
J	0.004	0.010	0.10	0.25
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°

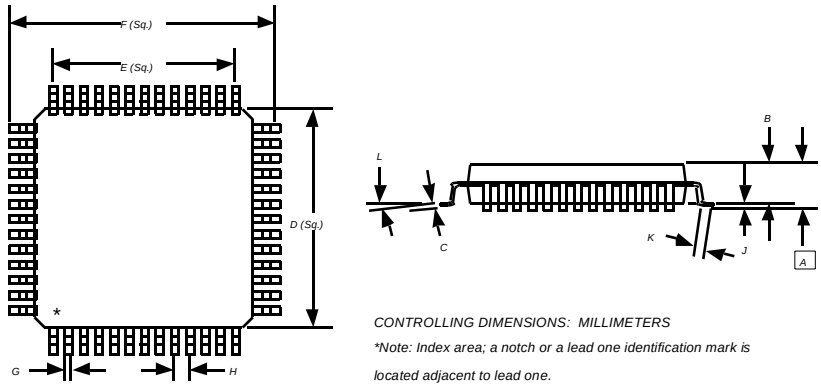


CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

52-LEAD PQ14 (14 x 14 x 2.67mm, 1.60mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.111 nom	0.118	2.82 nom	3.00
B	0.100	0.108	2.55	2.75
C	0.005	0.009	0.13	0.23
D	0.560 BSC		14.00 BSC	
E	0.472 REF		12.00 REF	
F	0.688 BSC		17.20 BSC	
G	0.014	0.022	0.35	0.50
H	0.0394 BSC		1.00 BSC	
J	0.004	0.010	0.10	0.25
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°

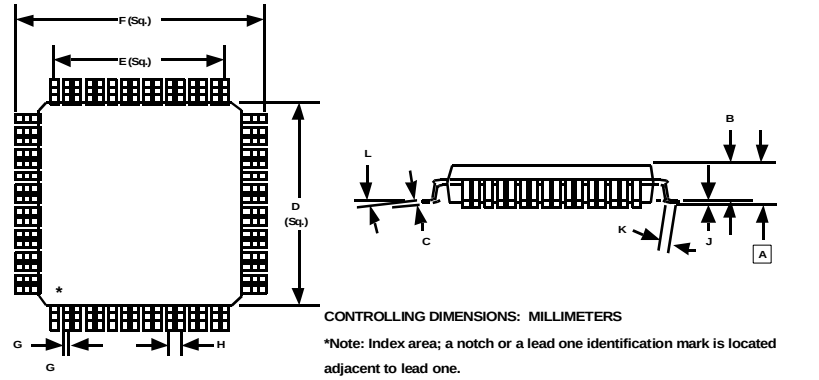


CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

64-LEAD PQ14 (14 x 14 x 2.67mm, 1.60mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.111 nom	0.118	2.82 nom	3.00
B	0.100	0.108	2.55	2.75
C	0.005	0.009	0.13	0.23
D	0.560 BSC		14.00 BSC	
E	0.472 REF		12.00 REF	
F	0.688 BSC		17.20 BSC	
G	0.012	0.018	0.30	0.45
H	0.0315 BSC		0.80 BSC	
J	0.004	0.010	0.10	0.25
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°



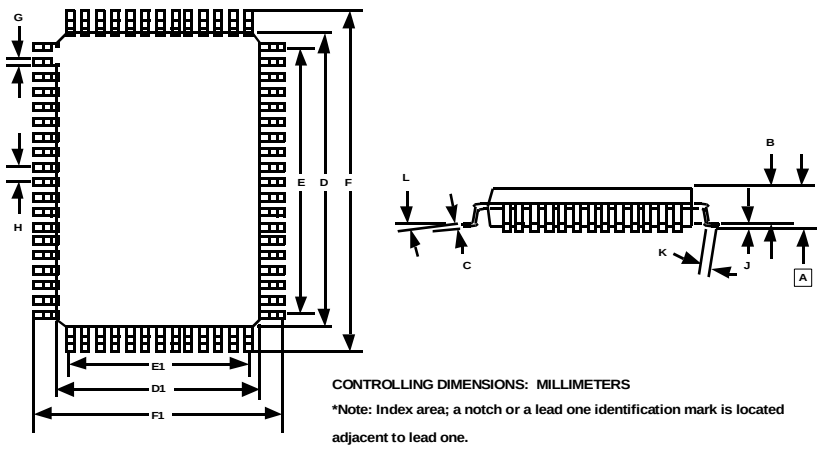
CONTROLLING DIMENSIONS: MILLIMETERS

***Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.**

PACKAGING & ORDERING

Plastic Quad Flatpack (PQFP)

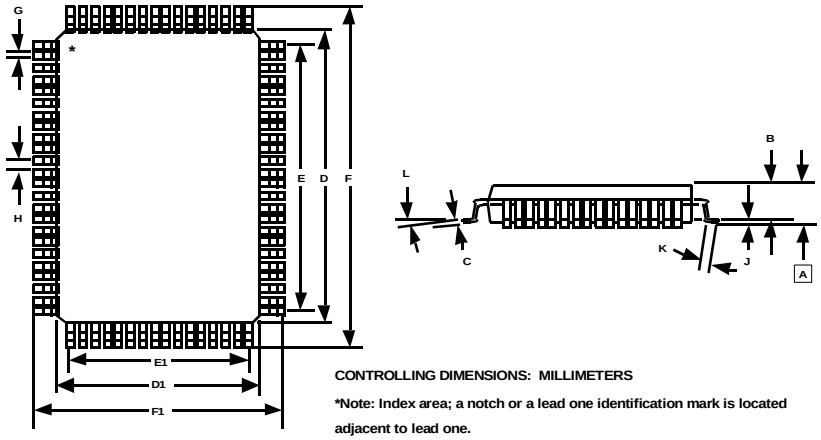
64-LEAD PQ20 (14 x 20 x 2.71mm, 1.60mm leadform)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.120 nom	0.134	3.04 nom	3.40
B	0.101	0.113	2.57	2.87
C	0.005	0.009	0.13	0.23
D	0.800 BSC		20.00 BSC	
D1	0.560 BSC		14.00 BSC	
E	0.720 REF		18.00 REF	
E1	0.480 REF		12.00 REF	
F	0.928 BSC		23.20 BSC	
F1	0.688 BSC		17.20 BSC	
G	0.014	0.020	0.35	0.50
H	0.0394 BSC		1.00 BSC	
J	0.010	.013 nom	0.25	0.33 nom
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°



CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

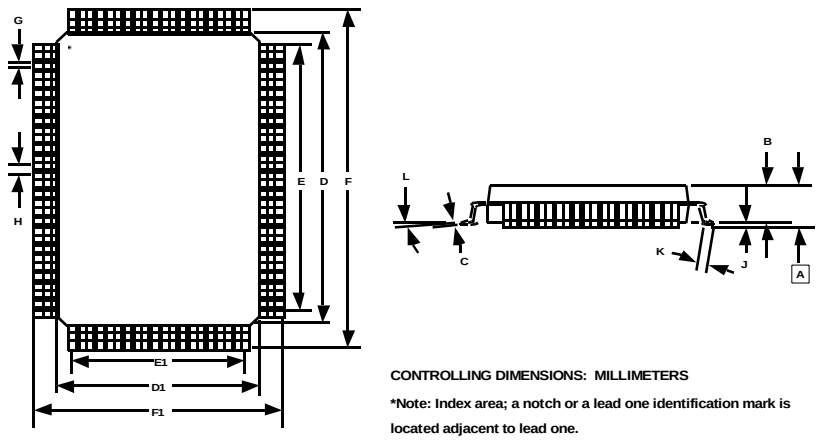
80-LEAD PQ20 (14 x 20 x 2.71mm, 1.60mm leadform)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.120 nom	0.134	3.04 nom	3.40
B	0.101	0.113	2.57	2.87
C	0.005	0.009	0.13	0.23
D	0.800 BSC		20.00 BSC	
D1	0.560 BSC		14.00 BSC	
E	0.724 REF		18.40 REF	
E1	0.480 REF		12.00 REF	
F	0.928 BSC		23.20 BSC	
F1	0.688 BSC		17.20 BSC	
G	0.012	0.018	0.30	0.45
H	0.0315 BSC		0.80 BSC	
J	0.010	.013 nom	0.25	0.33 nom
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°



CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

100-LEAD PQ20 (14 x 20 x 2.71mm, 1.60mm leadform)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.120 nom	0.134	3.04 nom	3.40
B	0.101	0.113	2.57	2.87
C	0.005	0.009	0.13	0.23
D	0.800 BSC		20.00 BSC	
D1	0.560 BSC		14.00 BSC	
E	0.742 REF		18.85 REF	
E1	0.486 REF		12.35 REF	
F	0.928 BSC		23.20 BSC	
F1	0.688 BSC		17.20 BSC	
G	0.009	0.015	0.22	0.38
H	0.0256 BSC		0.65 BSC	
J	0.010	.013 nom	0.25	0.33 nom
K	0.0292	0.0412	0.73	1.03
L	0°	7°	0°	7°

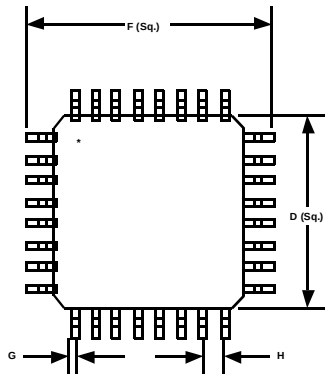


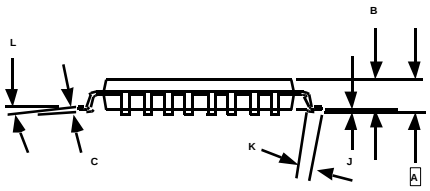
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

32-PIN TQFP (7 x 7 x 1.0mm, 1.00mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.048	—	1.20
B	0.038	0.042	0.95	1.05
C	0.004	0.008	0.09	0.20
D	0.280 BSC		7.00 BSC	
F	0.360 BSC		9.00 BSC	
G	0.012	0.018	0.30	0.45
H	0.032 BSC		0.80 BSC	
J	0.002	0.006	0.05	0.15
K	0.018	0.030	0.45	0.75
L	0°	7°	0°	7°



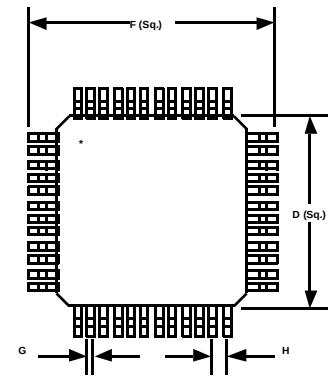


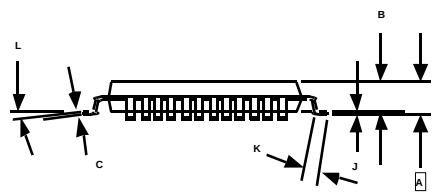
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

48-PIN TQFP (7 x 7 x 1.0mm, 1.00mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.048	—	1.20
B	0.038	0.042	0.95	1.05
C	0.004	0.008	0.09	0.20
D	0.280 BSC		7.00 BSC	
F	0.360 BSC		9.00 BSC	
G	0.007	0.011	0.17	0.27
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.018	0.030	0.45	0.75
L	0°	7°	0°	7°



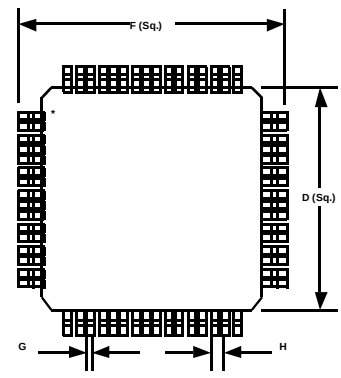


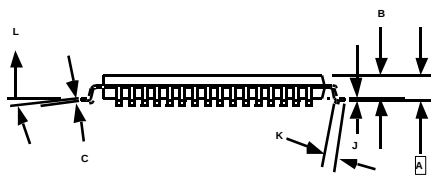
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

64-LEAD TQFP (10 x 10 x 1.0mm, 1.00mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.050	—	1.27
B	0.037	0.044	0.95	1.12
C	0.004	0.008	0.09	0.20
D	0.400 BSC		10.00 BSC	
F	0.480 BSC		12.00 BSC	
G	0.0052	0.0092	0.13	0.23
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.018	0.030	0.45	0.75
L	0°	7°	0°	7°





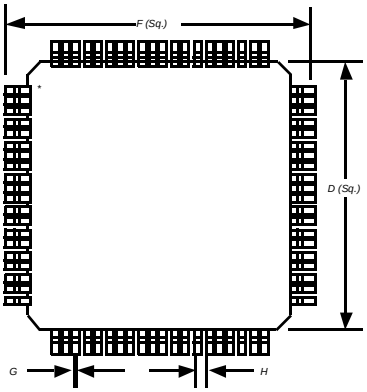
CONTROLLING DIMENSIONS: MILLIMETERS

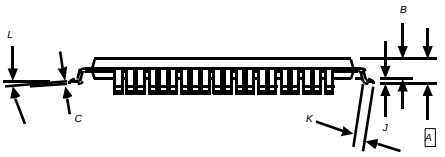
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

Thin Quad Flat Pack (TQFP)

80-LEAD TQFP (12 x 12 x 1.0mm, 1.00mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.048	—	1.20
B	0.037	0.042	0.95	1.05
C	0.004	0.008	0.09	0.20
D	0.473 BSC		12.00 BSC	
F	0.552 BSC		14.00 BSC	
G	0.007	0.011	0.17	0.27
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.018	0.030	0.45	0.75
L	0°	7°	0°	7°



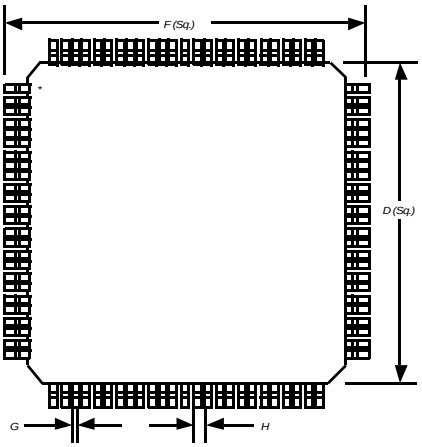


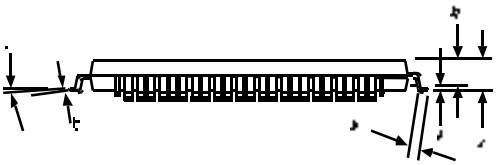
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

100-LEAD TQFP (14 x 14 x 1.4mm, 1.00mm leadform)

SYM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.063	—	1.60
B	0.053	0.057	1.35	1.45
C	0.004	0.008	0.09	0.20
D	0.552 BSC		14.00 BSC	
F	0.630 BSC		16.00 BSC	
G	0.007	0.011	0.17	0.27
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.018	0.030	0.45	0.75
L	0°	87	0°	7°





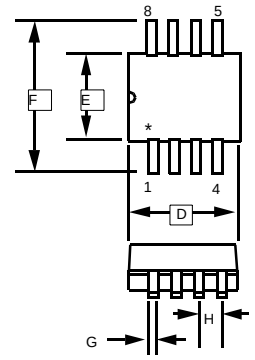
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

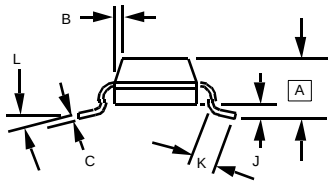
PACKAGING & ORDERING

8-Lead SOIC (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0 °	8 °	0 °	8 °

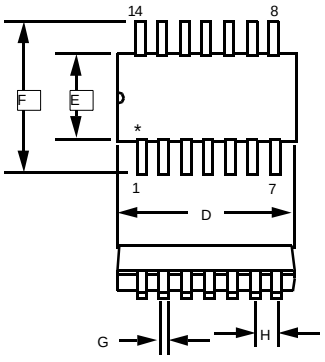


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

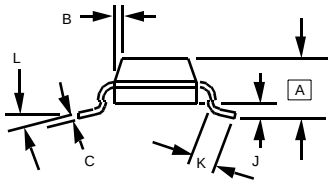


14-Lead Narrow SOIC (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.337	0.344	8.58	8.74
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0 °	8 °	0 °	8 °

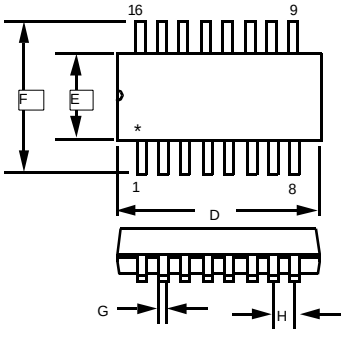


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

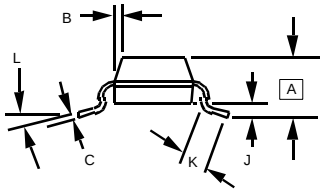


16-Lead SOIC NARROW (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0 °	8 °	0 °	8 °



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

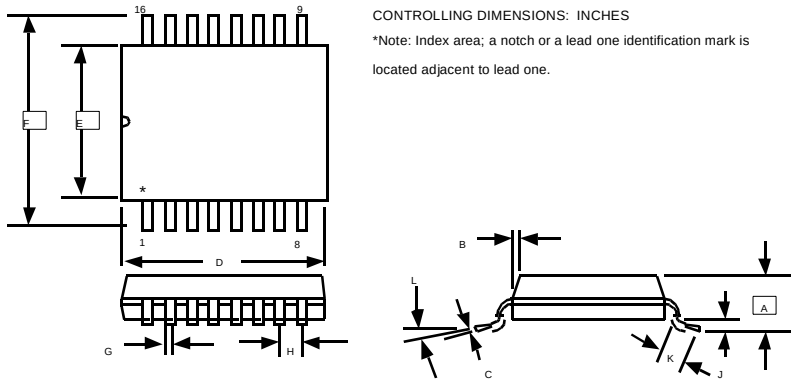


PACKAGING & ORDERING

Small Outline Integrated Circuit (SOIC)

16 PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050 BSC		1.27 BSC	
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °

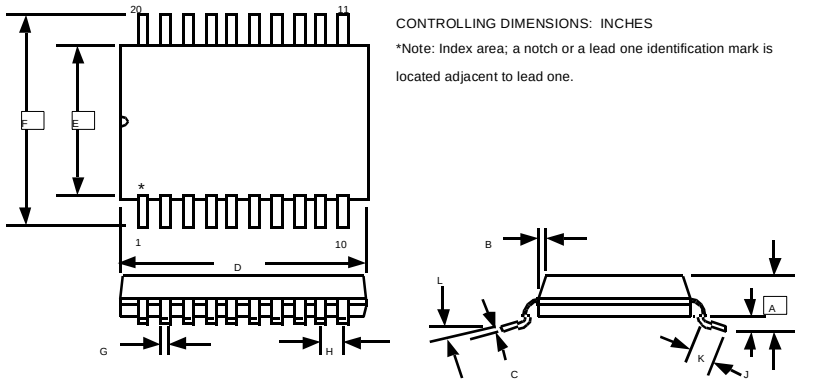


CONTROLLING DIMENSIONS: INCHES

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

20 PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050 BSC		1.27 BSC	
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °

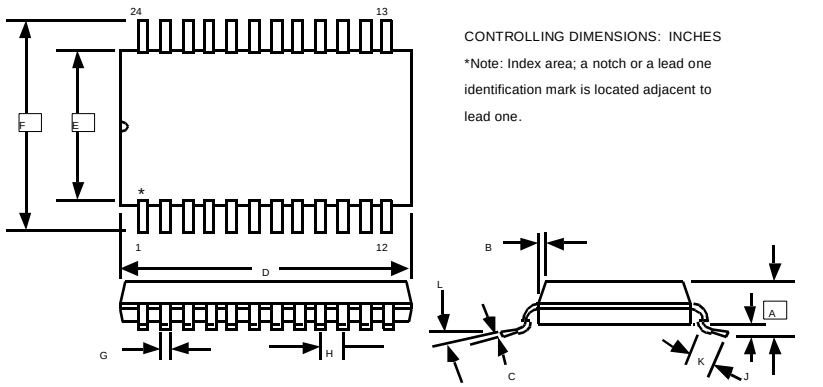


CONTROLLING DIMENSIONS: INCHES

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24-PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050 BSC		1.27 BSC	
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °



CONTROLLING DIMENSIONS: INCHES

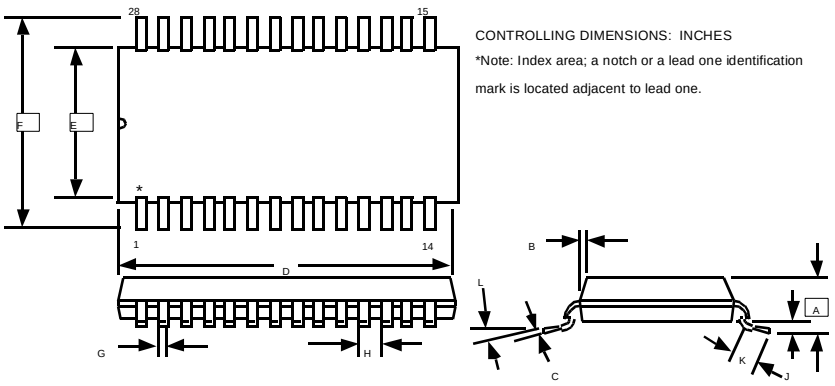
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

PACKAGING & ORDERING

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

28-PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.701	0.711	17.81	18.06
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050 BSC		1.27 BSC	
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °

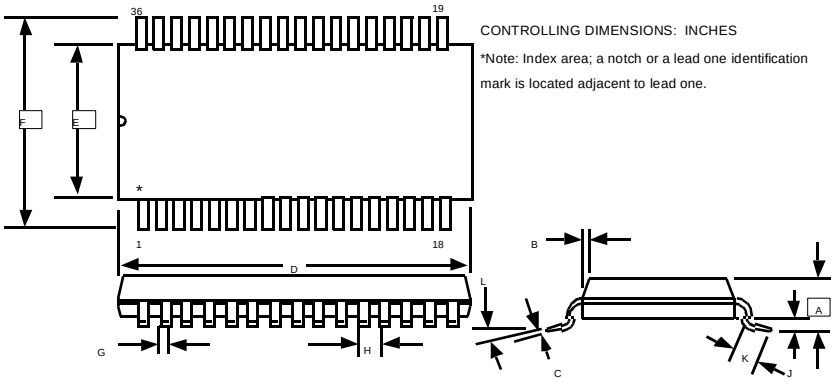


CONTROLLING DIMENSIONS: INCHES

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

36-PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.094	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.33
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.012	0.018	0.30	0.46
H	0.0315 BSC		0.80 BSC	
J	0.004	0.012	0.10	0.30
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°

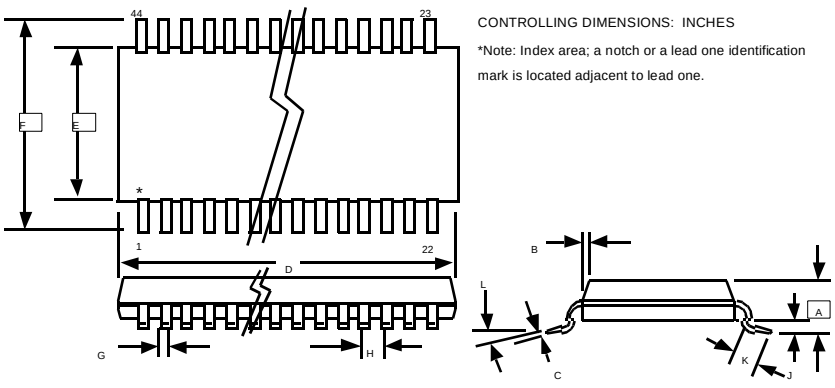


CONTROLLING DIMENSIONS: INCHES

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

44-PIN SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.094	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.33
D	0.701	0.711	17.81	18.06
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.012	0.018	0.31	0.46
H	0.0315 BSC		0.80 BSC	
J	0.004	0.012	0.10	0.30
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°



CONTROLLING DIMENSIONS: INCHES

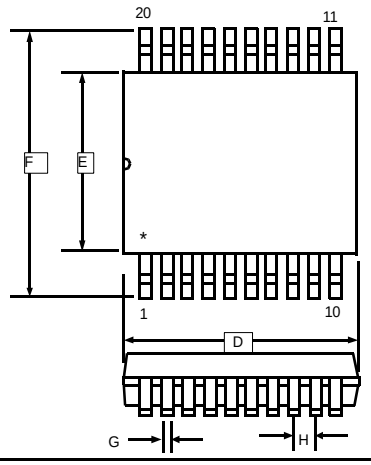
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

PACKAGING & ORDERING

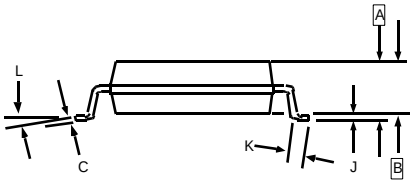
Shrink Small Outline Package (SSOP)

20-LEAD SSOP (5.3mm BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.278	.289	7.07	7.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°

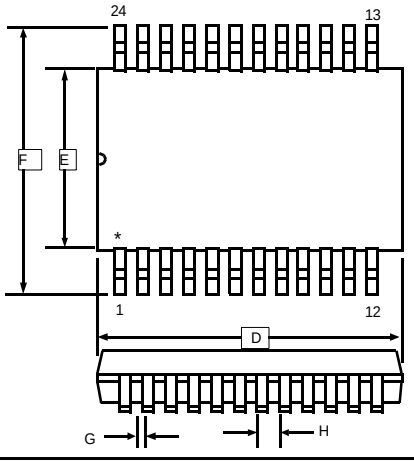


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

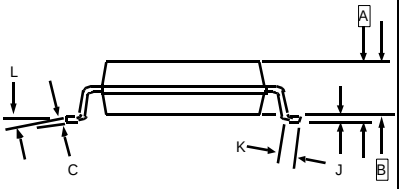


24-LEAD SSOP (.209" BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.318	.328	8.07	8.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°

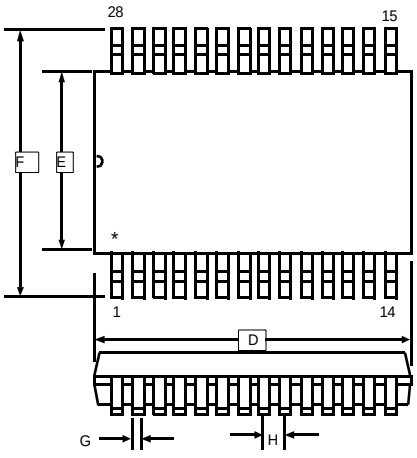


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

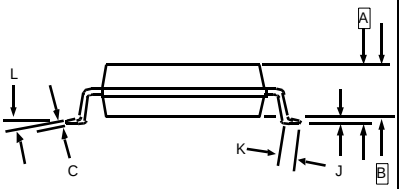


28-LEAD SSOP (5.3mm BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.397	.407	10.07	10.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°



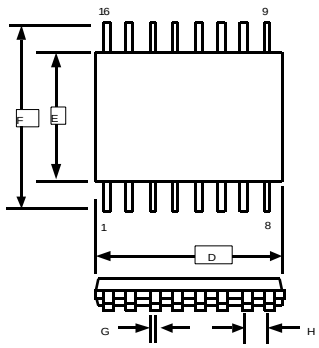
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



PACKAGING & ORDERING

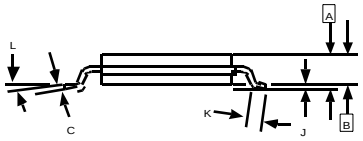
16 PIN VSOP (4.4mm BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	0.0433	–	1.10
B	0.0334	0.0374	0.85	0.95
C	0.004	0.006	0.090	0.16
D	0.193	0.201	6.40	6.60
E	0.169	0.177	4.30	4.50
F	0.246	0.256	6.25	6.50
G	0.008	0.012	0.19	0.30
H	0.0256 BSC		0.65 BSC	
J	0.002	0.006	0.05	0.15
K	0.020	0.028	0.50	0.70
L	0°	8°	0°	8°



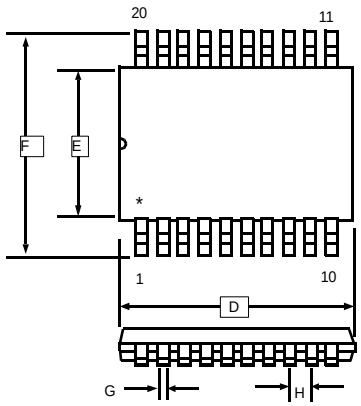
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

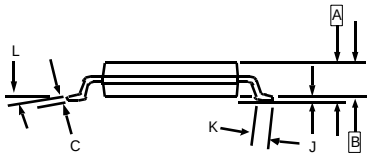


20-Lead VSOP (4.40mm BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	.0394	–	1.00
B	.0325	nom	0.825	nom
C	.004	.0078	0.107	0.197
D	.252	.260	6.40	6.60
E	.169	.176	4.30	4.48
F	.246	.256	6.25	6.50
G	.004	.012	0.10	0.30
H	.0256	BSC	0.65	BSC
J	.002	.006	0.05	0.15
K	.016	.024	0.40	0.60
L	0°	8°	0°	8°

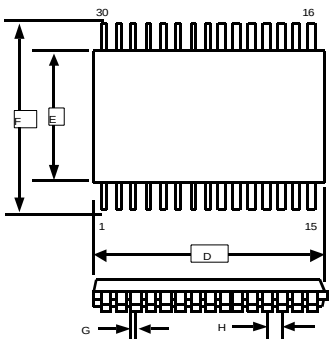


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



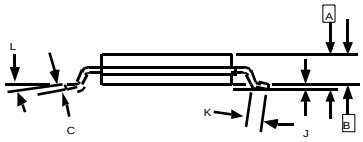
30 PIN VSOP (4.4mm BODY, 0.50mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	0.0433	–	1.10
B	0.0335	0.0374	0.85	0.95
C	0.004	0.006	0.090	0.16
D	0.303	0.311	7.70	7.90
E	0.169	0.177	4.30	4.50
F	0.246	0.256	6.25	6.50
G	0.007	0.011	0.17	0.27
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.020	0.028	0.50	0.70
L	0°	8°	0°	8°



CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

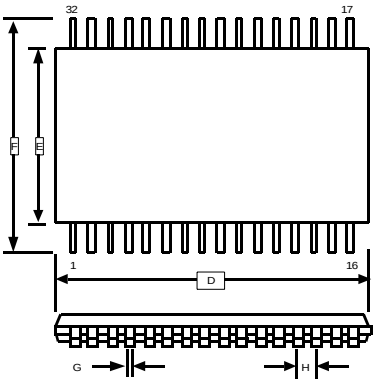


PACKAGING & ORDERING

Very Small Outline Package (VSOP)

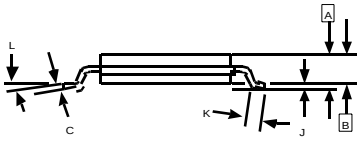
32 PIN VSOP (6.1mm BODY, 0.65mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	0.0433	–	1.10
B	0.034	0.037	0.85	0.95
C	0.004	0.006	0.090	0.16
D	0.429	0.437	10.90	11.10
E	0.236	0.244	6.00	6.20
F	0.313	0.325	7.95	8.25
G	0.008	0.012	0.19	0.30
H	0.0256 BSC		0.65 BSC	
J	0.002	0.006	0.05	0.15
K	0.020	0.030	0.50	0.75
L	0°	8°	0°	8°



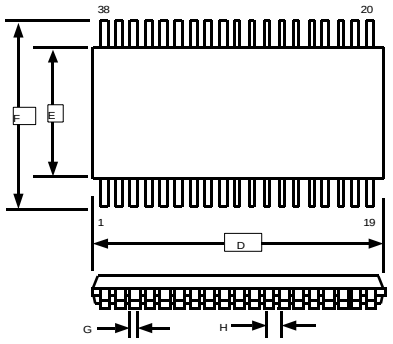
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



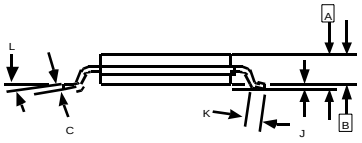
38 PIN VSOP (4.4mm BODY, 0.50mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	0.0433	–	1.10
B	0.034	0.037	0.85	0.95
C	0.004	0.006	0.090	0.16
D	0.378	0.386	9.60	9.80
E	0.169	0.177	4.30	4.50
F	0.246	0.256	6.25	6.50
G	0.007	0.011	0.17	0.27
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.020	0.030	0.50	0.75
L	0°	8°	0°	8°



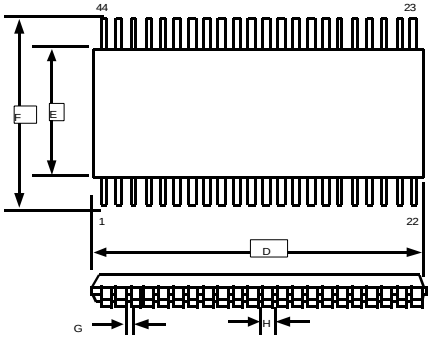
CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



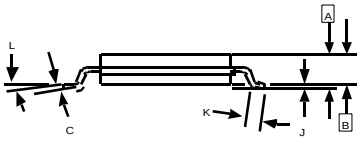
44 PIN VSOP (4.4mm BODY, 0.50mm LEAD PITCH)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	0.0433	–	1.10
B	0.034	0.037	0.85	0.95
C	0.004	0.006	0.090	0.16
D	0.448	0.456	11.20	11.40
E	0.169	0.177	4.30	4.50
F	0.246	0.256	6.25	6.50
G	0.008	0.012	0.10	0.30
H	0.0197 BSC		0.50 BSC	
J	0.002	0.006	0.05	0.15
K	0.020	0.030	0.50	0.75
L	0°	8°	0°	8°



CONTROLLING DIMENSIONS: MILLIMETERS

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



PACKAGING & ORDERING

Fax or Mail Orders to: VTC Inc.
Attn: Customer Service

Mailing Address: 2800 East Old Shakopee Road
Bloomington, MN 55425-1350

Fax: (612) 853-3355

Telephone: (612) 853-5100

Toll Free: (800) VTC-DISC

Email: info@vtc.com

Web Site: www.vtc.com

Ordering Guide for Mass Storage Products

V M 715 N XX 4 PO *

Manufacturer's ID

Family
M = Mass Storage (Disk Drive Circuits)

Part Number

Damping Resistor Designator on Preamps
R = Indicates Damping Resistor
N = No Damping Resistor
No Designator = Indicates a Schottky Isolated

Channel Count on Preamps

Two Most Significant Digits of Read Voltage Gain

Package Code
BX = Flip Chip (Bumped Die)
CP = Plastic Sampling Package (CAVPAK)
CQ = Ceramic Quad Flatpack
EQ = EPAD
F = No Flip Flop
NO = Narrow SOIC
QF = Plastic Quad Flatpack (PQFP)
QH = Heat Spreader
PM = Plastic SOIC Mirror Image
PQFP= PQFP with Heat Spreaders
PO = Plastic Small Outline Integrated Circuit (SOIC)
SM = Mirror Image SSOP
SS = Shrink Small Outline Package (SSOP)
TQ = Thin Quad Flatpack (TQFP)
VS = Very Small Outline Package (VSOP)
X = Die

Revision Designator Supplied by Factory
J = First Revision