WD2511/WD2840
Technical Package
April, 1984

WESTERN DIGITAL
CORPORATION

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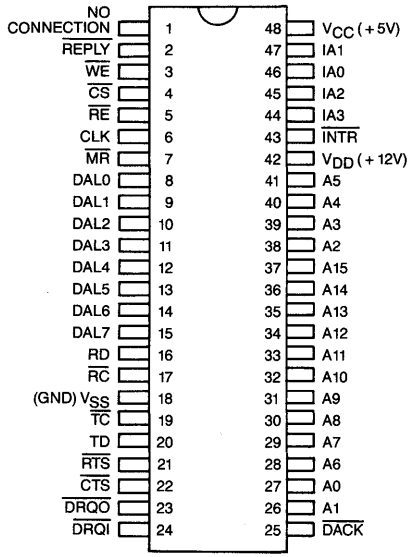
PRELIMINARY

WD2511 X.25 Packet Network Interface (LAPB)

FEATURES

- Packet switching controller, complies with CCITT Recommendation X.25, level 2, LAPB.
- Programmable primary timer (T1) and retransmission counter (N2).
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing.
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insertion and deletion.
- Automatic appending and testing of FCS field.
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines.
- DC to 1.1 MBPS data rate.
- TTL compatible.
- 48 pin dual in-line packages.



PIN DESIGNATION

DESCRIPTION

The WD2511 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25's LAPB with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER
STORE AND FORWARD SYSTEM
HIGH REL POINT TO POINT COMMUNICATIONS
BIT ORIENTED PROTOCALS WITH BUILT IN DMA

INTERFACE SIGNALS DESCRIPTION (All signals are TTL compatible.)

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1		No Connection	Leave pin open.
2	$\overline{\text{REPLY}}$	Reply	An active low output indicates the WD2511 has either a $\overline{\text{CS}}$•$\overline{\text{RE}}$ or a $\overline{\text{CS}}$•$\overline{\text{WE}}$ input condition.
3	$\overline{\text{WE}}$	Write Enable	The data on the DAL are written into the selected register when $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are low.
4	$\overline{\text{CS}}$	Chip Select	Active low chip select for CPU control of I/O registers.
5	$\overline{\text{RE}}$	Read Enable	The contents of the selected register is placed on DAL when $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low.
6	CLK	Clock	Clock input used for internal timing. Must be square wave and should be greater than 500 KHz.
7	$\overline{\text{MR}}$	Master Reset	Active low initializes the chip. All registers reset to zero, except control bits MDISC and $\overline{\text{LINK}}$ which are set to 1. $\overline{\text{DACK}}$ must be stable high before $\overline{\text{MR}}$ goes high.
8-15	DAL0-DAL7	Data Access Lines	An 8-bit bi-directional three-state data bus for CPU and DMA controlled transfers.
16	RD	Receive Data	Receive serial data input.
17	$\overline{\text{RC}}$	Receive Clock	This is a 1x clock input. RD is sampled on the rising edge of $\overline{\text{RC}}$.
18	V_{SS}	Ground	Ground.
19	$\overline{\text{TC}}$	Transmit Clock	A 1x clock input. TD changes on the falling edge of $\overline{\text{TC}}$.
20	TD	Transmit Data	Transmit serial data output.
21	$\overline{\text{RTS}}$	Request-To-Send	An open collector (drain) output which goes low when the WD2511 is ready to transmit either flags or data.
22	$\overline{\text{CTS}}$	Clear-To-Send	An active low input which signals the WD2511 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.
23	$\overline{\text{DRQO}}$	DMA Request Out	An active low output signal which initiates CPU bus request so the WD2511 can output data onto the bus.
24	$\overline{\text{DRQI}}$	DMA Request In	An active low output signal which intitiates CPU bus request so that data may be input to the WD2511.
25	$\overline{\text{DACK}}$	DMA Acknowledge	An active low input from the CPU in response to $\overline{\text{DRQI}}$ or $\overline{\text{DRQO}}$. $\overline{\text{DACK}}$ must not be low if $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low or if $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are low.
27, 26, 38-41, 28-37	A0-A15	Address Lines Out	Sixteen address outputs from the WD2511 for DMA operation. If the control bit ADRV is 1; the outputs are TTL drives at all times. If ADRV is 0, the outputs are three-state, and are HI-Z whenever $\overline{\text{DACK}}$ is high. (ADRV is in Control Register #1.)
42	V_{DD}	Power Supply	+ 12VDC power supply input.

INTERFACE SIGNALS DESCRIPTION CONTINUED (All signals are TTL compatible.)

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
43	$\overline{INTR}$	Interrupt Request	An active low interrupt service request output. Returns to high when Status Register #1 is read.
46, 47, 45, 44	IA0-IA3	Address Lines In	Four address inputs for CPU controlled read/ write operation of the I/O registers in the WD2511. If ADRV = 0, these may be tied to A0-A3. (ADRV is in Control Register = 1.)
48	V_{CC}	Power Supply	+5VDC power supply input.

ORGANIZATION

Note: See appendix D for a glossary of terms used throughout this document.

A detailed block diagram of the WD2511 is shown in Figure 1.

Mode control and monitor of status by the user's CPU is performed through the Read/Write Control circuit which reads from or writes into I/O registers addressed by IA0-IA3.

Transmit and receive data are accessed through the DMA control. Serial data is generated and received by the bit-oriented controllers.

Internal Control of the WD2511 is by means of three internal microcontrollers; one for transmit, one for receive, and one for overall control.

Parallel transmit data are entered into the Transmitter Holding Register (THR), and then presented to the Transmitter Register (TR) which converts the data to a serial bit stream. The Cyclic Redundancy Check (CRC) is computed in the 16-bit CRC register, and the result becomes the transmitted Frame Check Sequence (FCS).

Parallel receive data enters the Receiver Holding Register (RHR) from the 24-bit serial Receiver Register (RR). The 24-bit length of RR permits stripping of the FCS prior to transfer in to the RHR. The receiver CRC register is used to test the validity of the received FCS. A 3-stack FIFO is included in the receiver.

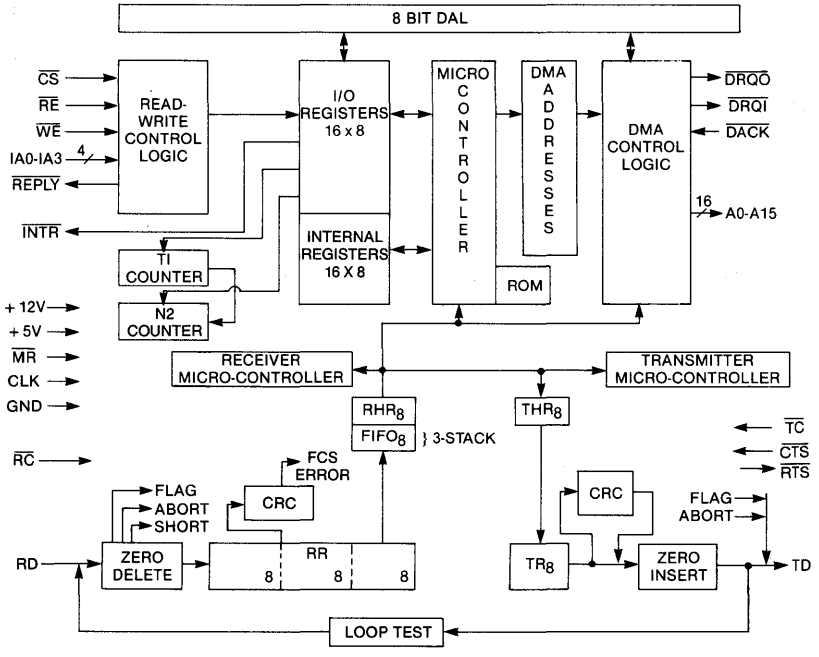


Figure 1 WD2511 BLOCK DIAGRAM — DETAILED

FRAME FORMAT

The WD2511 performs "bit-oriented" data communications control. According to the general format for bit-oriented procedures (HDLC, SDLC, ADCCP), each serial block of data is called a frame.

Each frame starts and ends with a Flag (01111110). A single flag may be used both as the closing flag of one frame and the opening flag of the next frame. In between flags, data transparency is provided by the insertion of a 0 bit after all sequences of 5 contiguous 1 bits. The receiver will strip the inserted 0 bits. The last 16-bits before the closing flag is in the Frame Check Sequence (FCS). Each frame also includes address and control fields (A and C fields).

The FCS calculation includes all data between the opening flag and the first bit of the FCS, except for 0's inserted for transparency. The 16-bit FCS has the following characteristics:

Polynomial = $X^{16} + X^{12} + X^5 + 1$
Transmitted Polarity —Inverted
Transmitted Order —High Order Bit First
Preset Value —All I's

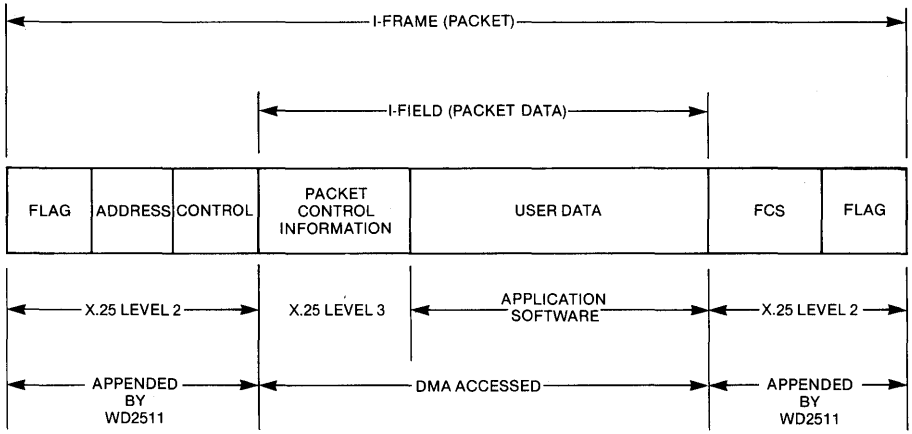
After the frame is received, if there were no errors then the remainder in the CRC register (internal in the WD2511) will be:

1111000010111000 FOB8

The WD2511 generates and tests the Flag, FCS, A-Field, C-Field, and performs zero bit insertion and deletion.

According to the X.25 protocol, there are three types of frames: supervisory (S-frame), un-numbered (U-frame), and information (I-frame). The WD2511 performs frame level (level 2) link access control. All S- and U-frames are automatically generated and tested by the WD2511. The user need only be concerned with the I-frames, which are packets.

The WD2511 will transmit contiguous flags for interframe time fill (full duplex mode).



X.25 MODE

NOTE: X.25 Level 1, is the Physical Interface

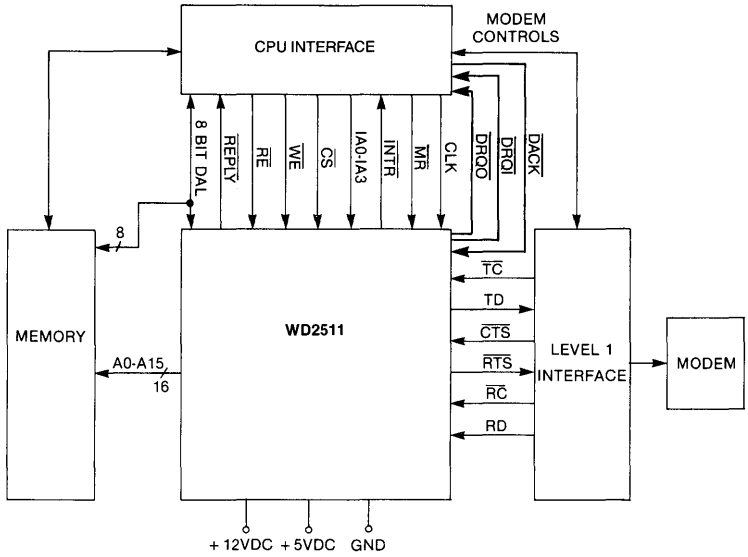


Figure 2. SYSTEM CONNECTION

II. PROGRAMMING THROUGH REGISTERS

The WD2511 is controlled and monitored by sixteen I/O registers.

Control, status, and error bits will be referred to as CR, SR, or ER, respectively, along with two digits. For example, SR16 refers to status register #1 and bit 6, which is "XBA."

REGISTER DEFINITION

REG #	IA3	IA2	IA1	IA0	REGISTER	REGISTER GROUPING
0	0	0	0	0	CR0	OVERALL CONTROL AND MONITOR
1	0	0	0	1	CR1	
2	0	0	1	0	*SR0	
3	0	0	1	1	*SR1	
4	0	1	0	0	*SR2	
5	0	1	0	1	*ER0	
6	0	1	1	0	*CHAIN MONITOR	RECEIVER MONITOR
7	0	1	1	1	*RECEIVED C-FIELD	
8	1	0	0	0	T1	TIMER
9	1	0	0	1	N2/T1	
A	1	0	1	0	TLOOK HI	DMA SET-UP
B	1	0	1	1	TLOOK LO	
C	1	1	0	0	CHAIN/BUFFER SIZE	
D	1	1	0	1	NOT USED	
E	1	1	1	0	XMT COMMAND "E"	"A" FIELD
F	1	1	1	1	XMT RESPONSE "F" (Note 1)	

*CPU READ ONLY. (Write Not Possible)

NOTE:
1. Registers E and F should be set-up while MDISC = 1.

CONTROL, STATUS, ERROR REGISTERS

REGISTER	BIT # 7	6	5	4	3	2	1	0
CR0	$\overline{\text{ADISC}}$	0	H/$\overline{\text{F}}$	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	RAMT	RECR	MDISC
CR1	TXMT	TRCV	$\overline{\text{XI}}$	ADRV	0	0	0	SEND
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX
SR1	[1]PKR	[1]XBA	[1]ERROR	0	NE2	NE1	NE0	0
SR2	T1OUT	IRTS	REC IDLE	0	0	0	0	$\overline{\text{LINK}}$
ER0	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

[1] Causes Interrupt ($\overline{\text{INTR}}$ Goes Low).

CONTROL REGISTER 0

REGISTER	CR07	CR06	CR05	CR04	CR03	CR02	CR01	CR00
CR0	$\overline{\text{ADISC}}$	0	H/$\overline{\text{F}}$	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	RAMT	RECR	MDISC

BIT	DESCRIPTION
CR00	MDISC (mandatory disconnect command) MDISC will cause a logical disconnect in the link. No DMA accessed data will be transferred as long as MDISC = 1. After Master Reset, MDISC will be set. The WD2511 will neither transmit nor accept received data until MDISC = 0.
CR01	RECR (Receiver Ready) indicates the CPU's is receiver buffer is Ready (CR01 = 1). If RECR = 1, the WD2511 may begin receiving I-frames. (See SR00)
CR02	RAMT — Internal Register Test when set. (See Self Tests)
CR03	The LOOP TEST bit will connect the transmit data output to the receive data input. The receiver input pins RD and $\overline{\text{RC}}$ are then logically disconnected from the internal circuitry. The "E" and "F" data registers of the A-field must be equal.
CR04	The Active/Passive bit when set, in conjunction with MDISC = 0, will cause the WD2511 to initiate link set-up. When this bit is reset, the WD2511 will wait for a link setup from the remote station.
CR05	H/F selects full duplex if CR05 = 0, and half duplex if CR05 = 1. (See Appendix A).
CR06	Unused control bits should remain at 0.
CR07	$\overline{\text{ADISC}}$ (disconnect) is used when CR04 = 1 (ACTIVE). When the WD2511 actively initiates link set-up, a DISC will be transmitted and acknowledged prior to transmission of the SABM if CR07 = 0. If CR07 = 1, the WD2511 will send only the SABM.

CONTROL REGISTER 1

REGISTER	CR17	CR16	CR15	CR14	CR13	CR12	CR11	CR10
CR1	TXMT	TRCV	$\overline{XI}$	ADRV	0	0	0	SEND

BIT	DESCRIPTION
CR10	The SEND bit is used to command the WD2511 to send the next packet or packets. If SEND = 1, the WD2511 will read from TLOOK the BRDY bit of the next segment for transmission. If BRDY = 0, the WD2511 will clear SEND and no action occurs. If BRDY = 1, the WD2511 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the WD2511 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and transmission of packets is stopped. As a matter of good practice, the CPU should set SEND each time a BRDY bit is set.
CR11-13	Unused bits, write in 0's.
CR14	The ADRV (ADDRESS VALID) bit is the control for the 16 bit output addresses (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{DACK}$ is low. If ADRV = 1, the outputs are always low impedance (TTL), and are forced high-level (logical 1) when $\overline{DRQO}$, $\overline{DRQI}$ and $\overline{DACK}$ are all high.
CR15	$\overline{XI}$ — (Transparent I-field) Used when TXMT = 1 $\overline{XI}$ = 0.Frame ≥ 3 bytes excluding FCS and Flag. $\overline{XI}$ = 1.Frame < 3 bytes excluding FCS and Flag.
CR16	TRCV — Transparent Receive. Receive all frames including unknown frames. See Appendix A.
CR17	TXMT — Transparent transmit. See Appendix A.

STATUS REGISTER 0

REGISTER	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX

BIT	DESCRIPTION
SR00	RNRX. An RNR has been transmitted or will be at next opportunity. The CPU should set RECR when receive buffers are available.
SR03-SR01	NB2-NB0. Next block to be transmitted.
SR04	RNRR. This bit is set when an RNR frame is received. Once set, it is cleared when an RR, REJ, SABM, or UA is received.
SR07-SR05	NA2-NA0. Next block of transmitted data to be Acknowledged.

STATUS REGISTER 1

REGISTER	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10
SR1	$_1$PKR	$_1$XBA	$_1$ERROR	0	NE2	NE1	NE0	0

BIT	DESCRIPTION
SR10	0 (not used)
SR13-SR11	NE2-NE0. Next Expected packet number and next RLOOK segment number.
SR14	0 (not used)
SR15$_1$	The ERROR bit indicates: 1) An error has occurred which is not recoverable by the WD2511 or 2) A significant event has occured. For the specific reason for the ERROR bit being set, see error register (ER0) on next page.
SR16$_1$	The XBA (transmitted block acknowledgement) bit set, indicates that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK'ED bit is set to "1" for each segment in TLOOK which was acknowledged.
SR17$_1$	The PKR bit stands for Packet Received. PKR = 1 indicates a packet has been received error-free and in correct sequence according to the received N (S) count. The I-field data has been placed in the host's RAM memory. NE is advanced.

NOTE 1:
The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an interrupt request ($\overline{INTR}$ goes low). After SR1 is read, all three bits are reset to 0, and $\overline{INTR}$ returns to high.

STATUS REGISTER 2

REGISTER	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20
SR2	T1OUT	$\overline{IRTS}$	REC IDLE	0	0	0	0	LINK

BIT	DESCRIPTION
SR20	If the link is established, $\overline{LINK}$ = 0. If the link is logically disconnected, $\overline{LINK}$ = 1.
ST24-21	Unused Bits — 0.
SR25	REC IDLE (Receiver Idle) indicates that the WD2511 has received at least 15 contiguous 1's.
SR26	$\overline{IRTS}$ stands for the Internal Request-To-Send bit, and indicates that the transmitter is attempting (successful or not) to send either data or flags.
SR27	T1OUT bit means that timer T1 has timed-out. This bit returns to 0 when T1 is re-started. When T1OUT = 1, T1 is not running. NOTE: This bit could be a 1 for a few microseconds in between intervals when T1 stops and is restarted.

ERROR REGISTER (ER0)

HEX VALUE	ERROR/EVENT
02	Receiver overrun. The Receiver Register (RR) had a character to load into the FIFO but the FIFO was full. See note 2.
04	Transmitter underrun. The Transmitter (TR) needed a character from the Transmitter Holding Register (THR) but the THR was not ready. The frame being transmitted is aborted. See note 2.
10	RLOOK not ready. REC RDY bit of next segment is 0 but RECR = 1. This interrupt will not occur if RECR = 0.
21	Link is up. Was down.
22	DISC sent. REC IDLE for time T1xN2.
24	DISC sent. SABM sent N2 times without receiving UA.
30	Received DISC or DM while link was up.
41	Going to next chain segment.
42	Next chain segment of the Receiver was not ready.
80	Link reset (SABM) received.
88	S-command sent N2 times without acknowledgement.
C0	Frame Reject (FRMR) received. See note 1.
C1	Frame Reject (FRMR) transmitted. See note 3. The received C-field (returned in the first I-field byte of the FRMR frame) was invalid.
C3	Frame Reject (FRMR) transmitted. See note 3. The received and rejected frame contained an I-field which is not permitted with this frame type.
C4	Frame Reject (FRMR) transmitted. See note 3. Received I-field exceeded the total amount of I-field data bytes established in Register C.
C8	Frame Reject (FRMR) transmitted. See note 3. The received frame contained an invalid N(R).

NOTES:

1. Whenever a Frame Reject (FRMR) is received, the I-field will have been placed in the appropriate memory location by the DMA. A link reset (SABM) will be transmitted. The NB is not advanced.
2. Receiver overrun and Transmitter underrun are indication that the $\overline{TC}/\overline{RC}$ clocks are either too fast for the WD2511, or the $\overline{DACK}$ response is too slow, or both.
3. As a result of FRMR transmitted, a SABM is received, causing link reset. In this case, only the Frame Reject interrupt is indicated.

W, X, Y, Z OF FRMR

A frame reject (FRMR) contains a three byte I-field. The first byte is the rejected frame control field. The second byte contains the current N(S) and N(R) counts of the station reporting the reject condition. The third byte contains W-X-Y-Z-0-0-0-0 where W is the LSB.

W set to 1 indicates that the control field received and returned in the first I-field byte was invalid.

X set to 1 indicates the rejected frame contained an I-field which is not permitted with this command.

W is also set to 1 in this case.

Y set to 1 indicates the received I-field exceeded the maximum I-field data byte count established (CHAIN/BUFFER SIZE). Y is mutually exclusive with W.

Z set to 1 indicates the received control field contained an invalid N(R). Z is mutually exclusive with W.

Upon receiving a FRMR, the WD2511 will place the 3 byte I-field in memory by DMA, just as if the FRMR were a packet.

When the WD2511 transmits a FRMR, the frame reject condition is entered. Only a received SABM or DISC will clear this condition. If any other command is received, the WD2511 will re-transmit the FRMR. Also, the WD2511 will **not** transmit packets while in the frame reject condition.

In the FRMR I-field, bit #4 of the second byte is a "1" if the rejected frame was a response and a "0" if the frame was a command.

MEMORY ACCESS METHOD

The WD2511 memory access is accomplished by the use of DMA and two look-up tables. These tables are set-up to allow up to 7 I-frames to be outstanding in each direction of the communications link. The look-up tables are divided into a transmit and a receive area (TLOOK and RLOOK) and are located in memory external to the WD2511.

TLOOK
RLOOK

These tables contain address and control information for individual Transmit/Receiver packets.

To provide the WD2511 access to TLOOK and RLOOK load only the starting address of TLOOK into the WD2511 registers A and B.

REG A	A15	A14	A13	A12	A11	A10	A9	A8
REG B	A7	A6	A5	A4	A3	A2	A1	A0

A0-A15 16 bit TLOOK starting address

The TLOOK and RLOOK tables are each divided into 8 segments and each segment contains 8 bytes. Figure 3 illustrates the segmentation of TLOOK and RLOOK. Figure 5 and 6 illustrate the contents of a single TLOOK and RLOOK segment.

TRANSMIT

To transmit, the WD2511 will have read from TLOOK the starting address and length of the first packet to be transmitted. The WD2511 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory buffer. At the end of the information field, the WD2511 will automatically send the FCS and closing Flag. The WD2511 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the WD2511 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

RECEIVE

When received, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit mode. If the packet is received error-free and in proper N(S) sequence count, an interrupt is generated and the WD2511 is ready for the next packet which will be placed in the next location.

Figure 4 shows a "store-and-forward" example that is useful in a network node.

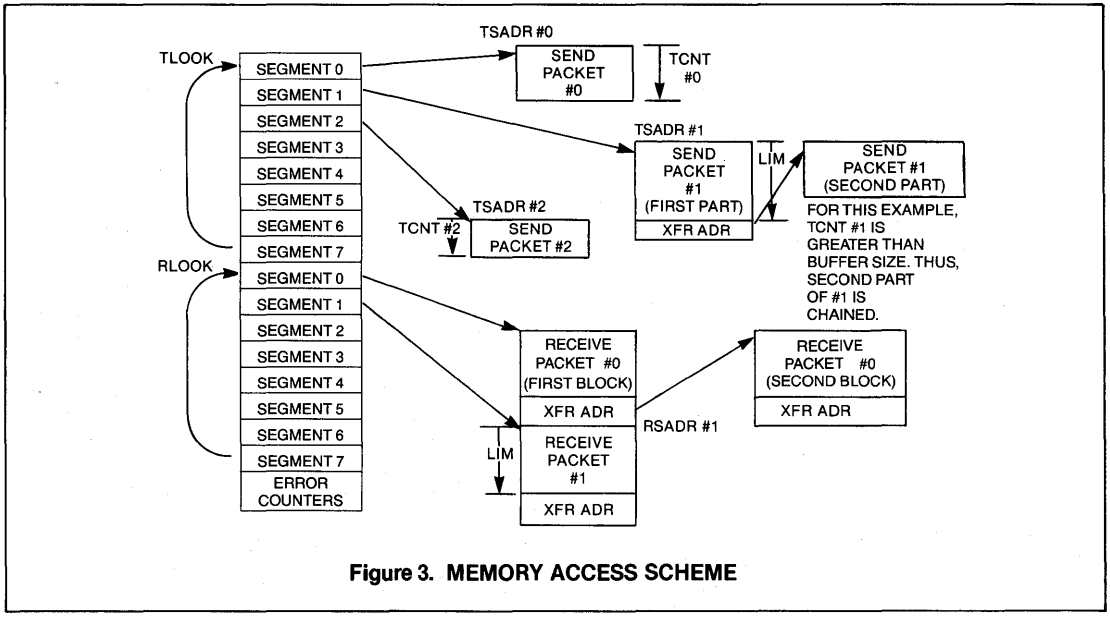


Figure 3. MEMORY ACCESS SCHEME

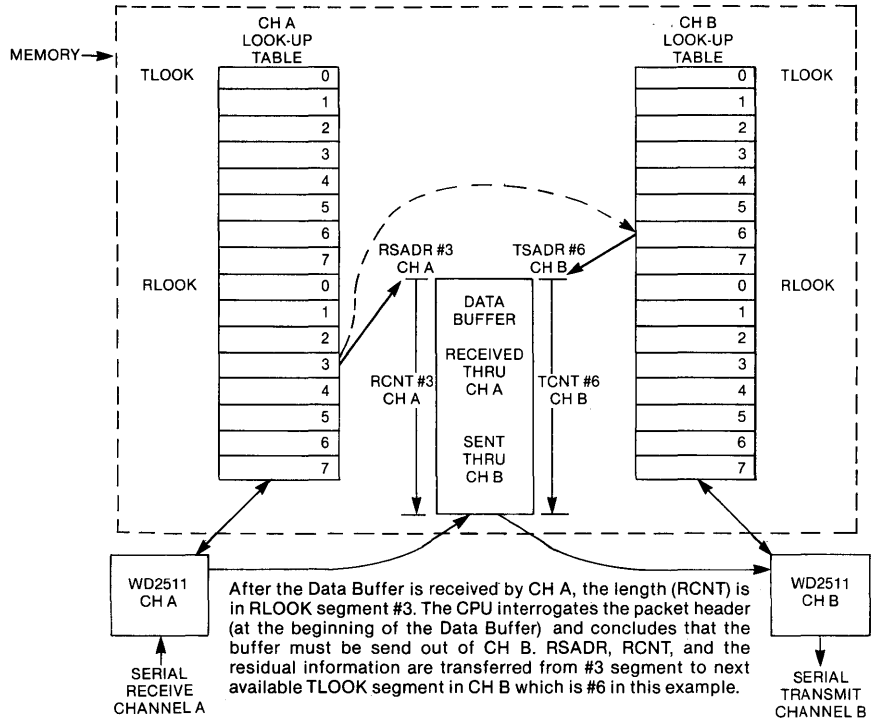


Figure 4. STORE-AND-FORWARD EXAMPLE

TLOOK AND RLOOK

Figures 5 and 6 detail the individual segments for TLOOK and RLOOK.

BRDY means that the transmit buffer is ready. The WD2511 will send the block only after the CPU sets BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the WD2511 will set BRDY = 0 and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknowledgement is contained in the received N(R) count of an I-frame or S-frame. Upon acknowledgement, the WD2511 will set ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the WD2511 that the receive buffer is ready. The WD2511 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the WD2511 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet with correct N(S), the WD2511 will, in order: 1) Set FRCML (Frame Complete), clear REC RDY and store received residual count. 2) Store the received length, in characters, of the I-field in RCNT HI and RCNT LO. 3) Advance the NE count and generate a packet received interrupt. 4) Acknowledge the received packet at the first opportunity.

The addresses (TSADR and RSADR) are 16-bit binary addresses. HI represents the upper 8-bits and LO represents the lower 8-bits. The counts (TCNT and RCNT) are 12-bit binary numbers for the number of characters in the I-field.

TSADR is the starting address of the buffer to transmit and TCNT is the binary count of the number of bytes to transmit. (4087 is the maximum value allowed in TCNT.)

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the WD2511 will write the value of RCNT which is the binary length of the received packet.

Whether the WD2511 accesses a look-up table or a memory block, a DMA Cycle is required for each access.

BYTE # IN SEGMENT	BIT # 7	6	5	4	3	2	1	0
1	ACK'ED	NU	NU	NU	NU	NU	NU	BRDY
2	TSADR HI							
3	TSADR LO							
4	SPARE				TCNT HI			
5	TCNT LO							
6	SPARE FOR USER DEFINITION							
7	SPARE							
8	SPARE							

NU = Not Used

FIGURE 5. TLOOK SEGMENT

The control bits in TLOOK (BRDY and ACK'ED) and in RLOOK (FRCML and REC RDY) define various states for each segment. These states are shown below:

TLOOK STATES

ACK'ED	BRDY	STATE
0	1	Ready To Transmit (CPU set BRDY, cleared ACK'ED)
0	0	*Transmitted and Awaiting Acknowledge (WD2511 cleared BRDY)
1	0	Received Acknowledge (WD2511 set ACK'ED)
1	1	This state not allowed

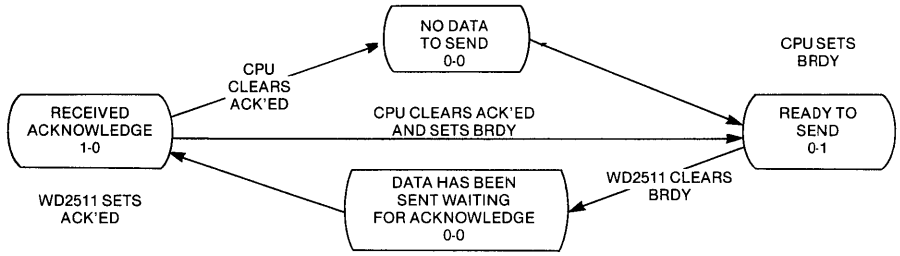
*State 0-0 could also occur whenever there is no data ready to send.

BYTE # IN SEGMENT	BIT # 7	6	5	4	3	2	1	0
1	FRCML*	NU	NU	NU	RES2	RES1	RES0	REC RDY
2	RSADR HI							
3	RSADR LO							
4	NOT USED				RCNT HI			
5	RCNT LO							
6	SPARE FOR USER DEFINITION							
7	SPARE							
8	SPARE							

NU = Not Used (NOTE: The "not used" bits may be either 1 or 0).

*FRCML = Frame Complete

FIGURE 6. RLOOK SEGMENT



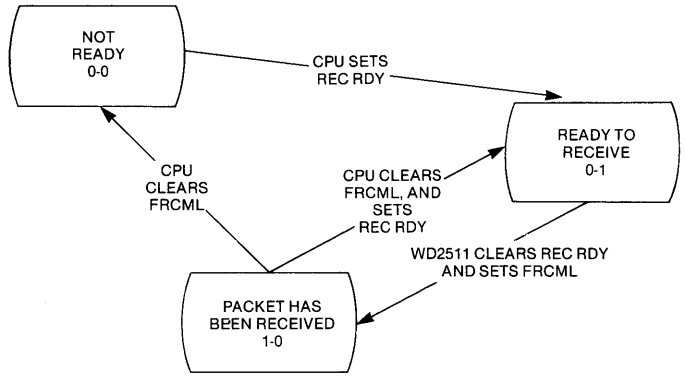
TLOOK SEGMENT STATE FLOW

Notice that in a TLOOK segment, the 0-0 state could have two meanings. Due to control internal to the WD2511, this will not pose an ambiguity to the WD2511. However, if it is a difficulty to the CPU, the CPU could at start-up, set all ACK'ED bits. Since this would only be a start-up procedure, this would not violate the "deadly embrace" rule.

In the "WAITING FOR ACKNOWLEDGE" state, one or more re-transmissions could occur.

RLOOK STATES

FRCML	REC RDY	STATE
0	1	Ready To Receive (CPU set REC RDY, cleared FRCML)
1	0	Received Packet (WD2511 set FRCML, cleared REC RDY)
0	0	Not Ready (CPU cleared FRCML)
1	1	This state not allowed



RLOOK SEGMENT STATE FLOW

REGISTER	CHAIN				BUFFER SIZE			
C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

CHAINING/BUFFER SIZE

The WD2511 includes a chained-block feature which allows the user more efficient use of memory particularly in situations where the maximum packet size is much larger than the average packet size.

Register C is used to program the chaining feature. The upper 4 bits define CHAIN which is the number of chain segments allowed in addition to the first segment. (If this feature is not used, make CHAIN all 0's.)

The lower 4 bits of Register C define the buffer size, which is the size of the buffer in multiples of 64 bytes including the transfer address (XFR ADR). If buffer size is 0000, the size is 64. For 0001, the size is 128, and so on.

The maximum amount of I-field data bytes that can be contained in this buffer is the buffer size minus 2 bytes (XFR ADR) for all transmitter and receiver chaining blocks, except for the last receiver chaining block. For this block, the maximum amount of I-field data bytes is the buffer size minus 3.

For example, suppose that the buffer size defines a segment size of 128 and that CHAIN defines 8 additional segments in addition to the first. (Register C would be hex 81 in this example.) When 126 bytes of I-field data have been received, the WD2511 will read the next two buffer bytes as a transfer address (XFR ADR) pointing to another segment. At the end of that segment is another XFR ADR, and so on, up to a maximum of 9 total segments, (in this example).

For the receiver, a XFR ADR of all 0's will mean that the next segment is not ready. If the WD2511 reaches a XFR ADR on the receiver with all 0s, there will be an Error Interrupt code 42. Otherwise, there will be an Interrupt code 41 which is a status indication that the WD2511 is going to the next segment. I/O Register 6 upper 4 bits gives a status of which chain segment is currently being used.

The transmitter chaining works like the receiver with the following exceptions:

1. XFR ADR = all 0's will not indicate next segment not ready.
2. There is no interrupt when going from one segment to another.
3. There is no status of the current segment being used.
4. Last chaining block is allowed to contain one more I-field data byte.

Total amount of I-field data bytes in receiver = (64 x (1 + BUFFER SIZE) − 2) x (1 + CHAIN) − 1.

The total amount of I-field data bytes in transmitter = (64 x (1 + BUFFER SIZE) − 2) x (1 + CHAIN).

Also, note that the transmitter and receiver counts are modified by 2 for each time a chain boundary is crossed. For example, if BUFFER SIZE = 0001 (segment size = 128 bytes including XFR ADR), and if an I-field of 270 bytes is to be transmitted, then there will be two times that a chain boundary is crossed. The TCNT must be made 274 to send 270 bytes. The same is true for RCNT. Note that the largest block of data that can be sent without chaining is 1021 bytes.

"DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the WD2511. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the WD2511 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK and to the I/O registers. The Error Counters do not apply to this rule.

> RULE: If a bit is set by the CPU, it will not be set by the WD2511, and vice versa. If a bit is cleared by the WD2511, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segments is only set by the CPU and only cleared by the WD2511.

SEND BIT CONTENTION

The WD2511 may be clearing the Send bit when the host is setting it. To insure that the bit is set the host should read the status of the Send bit after it is set. If the Send bit is cleared the host should set it again.

TLOOK AND RLOOK POINTERS

There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SR0) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted and is advanced at the end of each block transmission. NA is the value of the segment of the next block to be acknowledged. If all transmitted blocks have been acknowledged, then NA = NB.

In SR1 is a 3-bit counter, NE, used in conjunction with RLOOK. NE is the value of the segment number where the next received packet will be placed.

NA = Next to be Acknowledged

NB = Next Block to be Transmitted

NE = Next Expected to be Received

VARIABLE BIT LENGTH AND RESIDUAL BITS

The WD2511 will only send 8 bits per character and all transmitted frames will have an integral number of bytes.

The WD2511 may receive a packet with, or without, an integral number of bytes. The "RES" bits in the RLOOK tables indicate the number of received residual bits. The residual bits occupy the lower portion of the last received character.

RES 2	RES 1	RES 0	Received Residual Bits
0	0	0	0
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

ERROR COUNTERS

Following contiguously after RLOOK are six 8-bit error counters. The WD2511 will increment each counter at the occurrence of the defined event. However, the WD2511 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

ERROR COUNTER	TYPE OF ERROR
1	*Received Frames with FCS Error (includes frames ABORTed in the I-field).
2	Received Short Frames (less than 32-bits)
3	**Number of times T1 ran-out (completed)
4	Not used
5	*REJ Frames Received
6	REJ Frames Transmitted

*These counters are incremented only if the received A-field is equal to either Register E or F.
**Incremented only when attempting to transmit a command.

The Error Counters are accessed by the WD2511 transmitter DMA channel. Therefore, if multiple errors are received while the WD2511 is transmitting a long frame, only the last error will be counted. The only Counters which could miss counts because of this are Counters #1, #2, and #5. The error Counters are incremented only when the link is up (LINK = 0).

OTHER I/O REGISTERS

RECEIVED C-FIELD

Register 7 is the C-field of the last received frame, provided the A-field of the frame was equal to either register E or F, the FCS was good, the frame contained 32 or more bits, and the WD2511 is not waiting for a SABM or DISC in response to a transmitted FRMR.

TIMER

Registers 8 and 9 define a 10-bit timer (T1), and a 6-bit Maximum Number of Transmissions and Retransmissions counter (N2).

	BIT #							
REGISTER	7	6	5	4	3	2	1	0
8	T1							LSB
9	N2							
	MSB					LSB	MSB	

MSB = Most Significant Bit
LSB = Least Significant Bit

T1 provides the value of a delay in waiting for a response and/or acknowledgement. The delay is the binary count multiplied by time CT where:

$$CT = \frac{16384}{CLK} \text{ sec}$$

Thus, if CLK = 1 MHz, then T1 may be set in increments 16.384 milliseconds, to a maximum delay of 16.78 seconds. All ones in T1 is maximum delay.

Once the CPU establishes T1 and N2, there is no need to write into T1 and N2 again unless a master reset ($\overline{MR}$) has occurred, there is a power loss, or the CPU needs to change T1 or N2. If a time-out occurs, the WD2511 will still retain T1 and N2.

The conditions for starting, stopping, or restarting T1 are shown below: ("Re-start" means starting T1 before it ran-out).

START T1	RE-START T1	STOP T1
1. *I-frame sent and T1 not already in progress due to previous I-frame.	*Acknowledgement received to some, but not all, I-frames.	Acknowledgement received for all I-frames.
2. —	*RNR received while link up.	
3. *SABM or DISC sent. (N2 restarted at first occurrence)	—	UA or DM Received
4. Receiver Idle (REC IDLE = 1)	*Frame sent, while REC IDLE = 1	Detected REC IDLE = 0
5. S — command sent		—

*N2 is restarted.

"A" FIELD REGISTERS

Registers E and F provide a programmable A-field. This allows the WD2511 to be a super-set of the X.25 document. That is, the WD2511 can handle a wider range of application than the DTE-DCE links defined in X.25. These wider ranges include: DTE-to-DTE connection, multipoint, and loop-back testing.

If the WD2511 is strictly in an X.25 DTE-DCE link, use the values shown below:

DTE	Register E = 01 Register F = 03
DCE	Register E = 03 Register F = 01

If performing a loop-back test, either internal (CR03 = 1) or external (CR03 = 0), registers E and F should be the same.

V. LAPB PROCEDURE

The Link Access Procedure Balanced (LAPB) is described in CCITT Recommendation X.25 as the Level 2 protocol for the Asynchronous Balanced Mode (ABM).

Zero bit insertion/deletion, use of flags, and FCS are part of Level 2, and have been discussed in this document.

The DTE is the Data Terminal Equipment and the DCE is the Data Circuit Termination Equipment (the network side of the DTE-DCE connection).

The DTE and DCE are each "combined" stations in that each can transmit and receive commands and responses. Whether a particular frame is to be taken as a command or a Response is determined by the contents of the address field. Commands from the DCE and the associated responses from the DTE use address A (hex 03).

Commands from the DTE and the associated responses from the DCE use address B (hex 01).

The individual commands and responses are shown in Figure 7.

USE OF POLL BIT

One use of the Poll bit (P) is in conjunction with Time-Out Recovery. Timer T1 is started at the beginning of a transmitted command provided it has not been previously started. If T1 runs out, the command will be retransmitted with P = 1. If T1 runs out again, the command will again be retransmitted, with P = 1 up to N2 times. At N2 + 1, an error interrupt will occur. If the command was an S-frame (originally an I-frame), the WD2511 will reset the link by transmitting a SABM. If the command was a SABM, the WD2511 will send a DISC. If a DISC, the WD2511 will continue to send a DISC indefinitely.

LAPB Commands and Responses (Bit 0 is transmitted first).
Only the FRMR and I-frame contain I-fields.

FRAME TYPE	COMMAND	RESPONSE	BIT #							
			7	6	5	4	3	2	1	0
INFORMATION (I)	I-FRAME (PACKET)		N(R)			P	N(S)			0
UNNUMBERED (U)	SABM		0	0	1	P	1	1	1	1
	DISC		0	1	0	P	0	0	1	1
		UA	0	1	1	F	0	0	1	1
		FRMR	1	0	0	F	0	1	1	1
		DM	0	0	0	F	1	1	1	1
SUPERVISORY (S)	RR	RR	N(R)			P/F	0	0	0	1
	RNR	RNR	N(R)			P/F	0	1	0	1
	*REJ	REJ	N(R)			P/F	1	0	0	1

*The WD2511 will not send a REJ command (will send REJ response, only), but may receive either a REJ command or REJ response.

FIGURE 7.

TRANSMISSION OF ABORT

An ABORT (seven contiguous 1's) is transmitted to terminate a frame in such a manner that the receiving station will ignore the frame. There are two conditions which will cause the WD2511 to transmit an ABORT:

1. Transmitter Under-Run
2. While transmitting a packet, a REJ is received.

LOOP-BACK TEST

The loop-back may be internal (CR03 = 1) or external (CR03 = 0). Of course, if external, RD and TD must be tied together either directly or remotely.

If CR03 = 1, TD is internally tied to RD, and the RD signal (pin 16) is internally disconnected. Also, $\overline{TC}$ is internally tied to $\overline{RC}$ and the pin at $\overline{RC}$ (pin 17) is internally disconnected. $\overline{CTS}$ must be connected externally to GND or $\overline{RTS}$.

WD2511 ELECTRICAL SPECIFICATIONS:

ABSOLUTE MAXIMUM RATINGS:

Voltages referenced to V_{SS}

High Supply Voltage (V_{DD}) . . . . . −0.3 to +15V
Voltage at any Pin . . . . . −0.3 to +15V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

Operating DC Characteristics: V_{SS} = 0V, V_{CC} = +5.0V ±0.25, V_{SS} = +12.0V ±0.6V T_A = 0° to +70°C

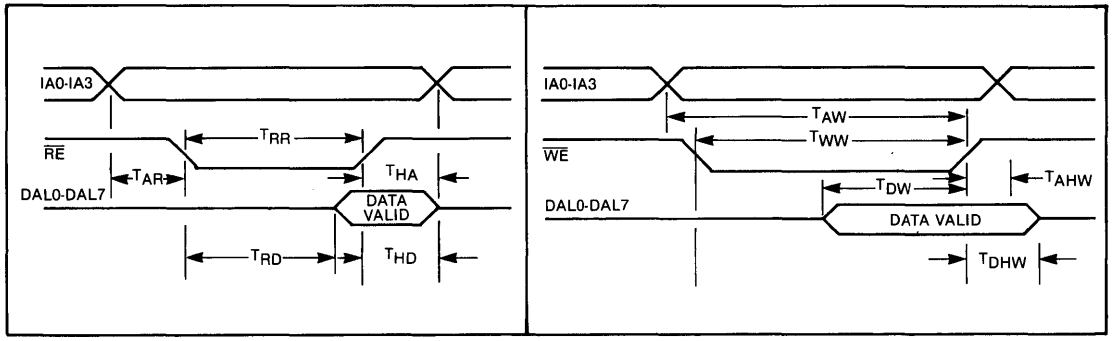
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	V_{DD} Supply Current		20	70	mA	
I_{CC}	V_{CC} Supply Current		200	280	mA	
V_{DD}	High Voltage Supply	11.4	12	12.6	V	
V_{CC}	Low Voltage Supply	4.75	5	5.25	V	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −0.1mA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{LH}	Input Source Current			10	μA	Vin = V_{CC}
I_{LL}	Input Sink Current			10	μA	Vin = +0.4V
I_{OZH}	Output Leakage (High Impedance)			50	μA	Vin = V_{CC}
I_{OZL}	Output Leakage (High Impedance)			50	μA	Vin = +0.4V

AC Timing Characteristics (AC):

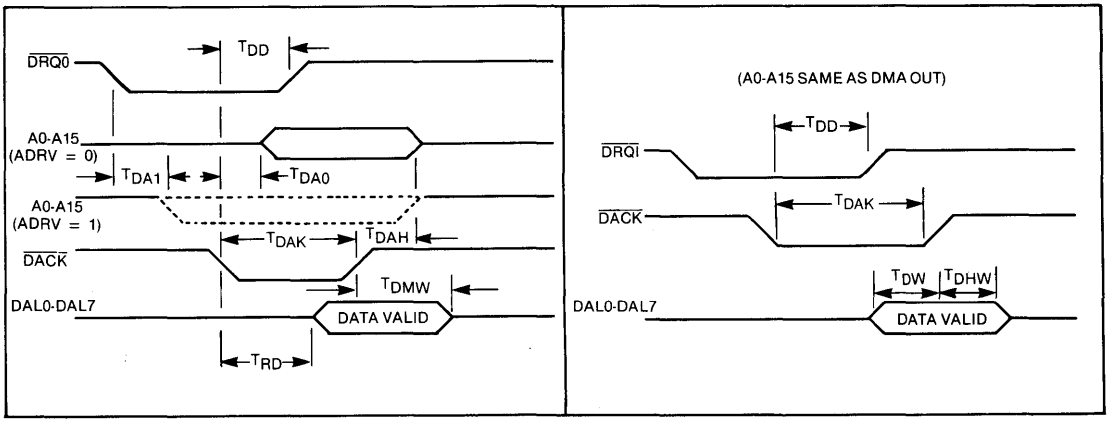
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CLK	Clock Frequency	0.5		2.05	MHz	Note 1
RC	Receive Clock Range	0			MHz	Note 4
TC	Transmit Clock Range	0			MHz	Note 4
MR	Master Reset Pulse Width	10			mS	
T_{AR}	Input Address Valid to $\overline{RE}$	0			nS	
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid	2		375	nS	Note 5, 2
T_{HD}	Data Hold Time from Read to Strobe	20		100	nS	
T_{HA}	Address Hold Time from Read Strobe	0			nS	
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	100			nS	
T_{WW}	Minimum $\overline{WE}$ Pulse Width	200			nS	
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100			nS	Note 2, 3
T_{WRR}	CS High between Writes	300			nS	
T_{RDR}	CS High between RE	300			nS	
T_{RR}	RE Pulse Width	375			nS	
T_{DAK}	DACK Pulse Width	375				
T_{AHW}	Address Hold Time after $\overline{WE}$	80			nS	
T_{DHW}	Data Hold Time after $\overline{WE}$ or after $\overline{DACK}$ for DMA Write	100				
T_{DA1}	Time from $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1			80	nS	Note 3
T_{DA0}	Time from $\overline{DACK}$ to Output Address Valid if ADRV = 0			375	nS	Note 5
T_{DD}	Time from Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)			375	nS	Note 5
T_{DAH}	Output Address Hold Time from $\overline{DACK}$	20		100	nS	
T_{DMW}	Data Hold Time from $\overline{DACK}$ for DMA Out	20		100	nS	Note 2
T_{TDV}	TD Valid	100			nS	
T_{SRD}	RD Setup	0			nS	
T_{HRD}	RD Hold	320			nS	

NOTES:

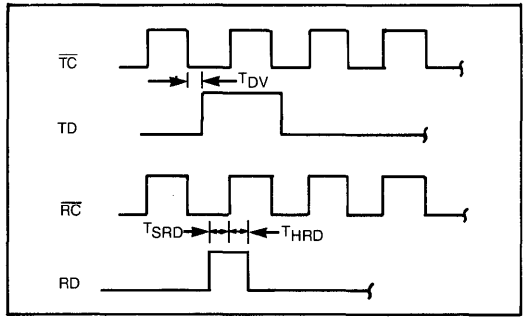
1. Clock must have 50% duty cycle.
2. There must not be a CPU read or write ($\overline{CS}$-$\overline{RE}$ or $\overline{CS}$-$\overline{WE}$) within 500 nanoseconds after the trailing (rising) edge of $\overline{DACK}$.
3. There must not be the leading (falling) edge of $\overline{DACK}$ allowed within 500 nanoseconds after the completion of a CPU write ($\overline{CS}$-$\overline{WE}$).
4. See "Ordering Information" for maximum serial rates.
5. C(load) = 100pf
6. Measured by discharging a 100pf capacitor to each pin through a 1K ohm resistor.



CPU READ ($\overline{CS}$ IS LOW) **CPU WRITE ($\overline{CS}$ IS LOW)**



DMA OUT **DMA IN**



TD-RD TIMING

APPENDIX A

TRANSPARENT MODES

The WD2511 was originally intended to be a link level controller meeting the requirements of X.25 LAPB and this has been accomplished. However, there has been an increasing demand from potential WD2511 users for additional frame types not included in the LAPB frame type repertoire.

For example, the Bell System standard, BX.25, calls for the use of XID (exchange identification) in LAPB connections of DTE-to-DTE and in Dial access. (Of course, DTE-to-DTE and Dial access are not X.25 in the strictest sense.) Also, Western Digital has received several requests for the use of a SIM (set initialization mode). Also, there has been one request to allow "unknown" frames to pass thru the chip for the purpose of teleloading.

Therefore, we have added two selectable modes to the WD2511: transparent transmit and transparent receive. Basically, these two modes allow the user the option to pass certain non-LAPB frames thru the chip without controlling these frames according to the LAPB protocol.

FEATURES OF THE TRANSPARENT MODES

- May transmit any A and C field under transparent control.
- May receive any U-frame not part of the LAPB repertoire if transparent-receive enabled.
- Transparent modes are link state independent.

1.0 HOW THE TRANSPARENT MODES WORK

Two control bits have been added. TXMT (CR17) is the bit to enable the Transparent Transmit and TRCV (CR16) will enable the Transparent Receive.

1.1 TRANSPARENT TRANSMIT

When TXMT = 1, the WD2511 will transmit the frame in the next TLOOK segment provided SEND (CR10) = 1 and BRDY of that TLOOK segment is 1. The link may be either UP or DOWN. The WD2511 will not add the A and C fields to the Transparent Transmitted frame. The user's CPU must add these fields as the first two bytes in the transmit buffer. Thus, the significance of the transmit count (TCNT) is different from normal packet transmission. In packet transmission, TCNT is the count of the I-field. In transparent transmission, TCNT is the I-field plus the A and C fields (I-field plus two bytes).

The timer, T1, will be disabled in transparent transmission. Therefore, if using this feature while the link is UP, it is advised that TXMT be set only when there are no outstanding (unacknowledged) packets which is indicated whenever NA = NB.

At the end of the transparent transmission, there will be an interrupt with XBA = 1. The SEND bit will be cleared, but the BRDY bit will not be cleared. The NB pointer will not be incremented. To send another transparent frame, set SEND. To resume packet transmission, clear TXMT and set SEND. (Of course, the TLOOK segment must be set-up prior to setting SEND.)

If SEND is set while the link is down, a transmission will occur even if TXMT = 0. Under this condition, a packet will be transmitted from current TLOOK segment, NB and V(S) will be incremented, and the chip will go on to the next TLOOK segment just as if the link were UP. However, the WD2511 will expect no acknowledgment to the packet(s). If the link is brought UP later, NB and V(S) are cleared to 0 at the time the link comes UP.

The bit $\overline{XI}$ (CR15) is used only when TXMT = 1. $\overline{XI}$ stands for Transmit I-field. If the frame contains three, or more bytes, not counting FCS, set $\overline{XI}$ = 0. If the frame contains two bytes not counting FCS, set $\overline{XI}$ = 1. When $\overline{XI}$ = 1, only two frame bytes will be transmitted regardless of TCNT. DO NOT attempt to transmit a frame with TXMT = 1 and $\overline{XI}$ = 0 if TCNT is 2, 1, or 0.

1.2 TRANSPARENT RECEIVE

For the purposes of this discussion, it is necessary to define an "unknown frame." That is, a frame which is "unknown" to the WD2511.

Unknown Frame: A U-frame (unnumbered) frame which is not part of the LAPB repertoire. The U-frame repertoire in LAPB is SABM, DISC, DM, UA, and FRMR. For the purposes of this discussion, "UF" will refer to an unknown frame without an I-field, and "UFI" will refer to an unknown frame with a I-field.

A received SREJ (Selective REJect), which is an S-frame, is not considered an unknown frame by the WD2511. If the link is DOWN and an SREJ command is received, a DM response will be sent. If the link is DOWN and a SREJ response is received, the SREJ is disregarded. If the link is UP and a SREJ command or response is received, a FRMR will be sent with W = 1. The WD2511 will treat a received SREJ the same whether TRCV is 0 or 1.

A received packet (I-frame) response is not considered an unknown frame by the WD2511. If the link is DOWN, the frame is disregarded. If the link is UP, a FRMR will be sent with W = 1 and X = 1. The received packet response is treated the same whether TRCV is 0 or 1.

Whether TRCV is 0 or 1, the WD2511 will check all received frames to insure that the A-field equals either Register E or F, that the FCS is correct, and that the frame contains 32 bits or more. If TRCV = 0, and if a UF or UFI is received, and if the link is UP, the WD2511 will send a FRMR with W = 1 (W and X are 1 in the case of a UFI). See "States of the WD2511."

When TRCV = 1, the WD2511 will be enabled to receive all frames. If the frame is "known" by the WD2511, it will be treated according to the protocol just as if TRCV = 0. However, if the frame is a UF or UFI, it will be passed on to the user's CPU.

When an unknown frame is received while TRCV = 1, there will be an interrupt with ERROR = 1 and the Error Register (ER0) will contain one of the following hexidecimal values:

ER0	FRAME RECEIVED
60	UFI Response
61	UFI Command
62	UF Response
63	UF Command

The C-field of the received frame is contained in Register #7. If the frame had an I-field, the frame will be placed in the next RLOOK segment and the value of RCNT will represent the count of bytes in the I-field (not including the A and C fields). The RLOOK pointer, NE, will be incremented. Therefore, the relationship between NE and V(R) will not be guaranteed if transparent receive is used while the link is UP. However, this will not cause a sequence problem in the protocol since the actual V(R) is maintained in an internal register in the WD2511. Note that NE is cleared when the link is brought UP. Thus, if transparent receive is used only when the link is DOWN, then NE will be equal to V(R).

A word of caution. If the next RLOOK segment is not ready when a UFI is received, the Error Register (60 or 61) will be overwritten almost immediately with an error code 10 (RLNR) and the user will not know if the received UFI was a command or response.

If RECR is set while the link is DOWN, the WD2511 will prepare to receive I-fields, whether TRCV is 0 or 1. If a packet command is received, there will be a PKR interrupt, and the NE and V(R) will be incremented. Of course, NE and V(R) are cleared once the link is brought up.

The following tables show what action the WD2511 will take when various frames are received.

TABLE 1. PACKET RECEIVED (command, not response)

LINK	RLOOK READY	TRCV	ACTION BY WD2511
DOWN	NO	0 or 1	DISREGARD
DOWN	YES	0 or 1	If N(S) = V(R), PKR interrupt, V(R) and NE incremented. No ack transmitted. If N(S) not = V(R), DISREGARD.
UP	NO	0 or 1	If N(S) = V(RT), RNR sent, Else, REJ condition entered.
UP	YES	0 or 1	If N(S) = V(R), PKR interrupt, V(R) and NE incremented. Acknowledgement sent at next opportunity. If N(S) not = V(R), enter REJ condition.

TABLE II. UFI RECEIVED

LINK	RLOOK READY	TRCV	ACTION BY WD2511
DOWN	NO	0 or 1	DISREGARD
DOWN	YES	0	DISREGARD
DOWN	YES	1	Error interrupt 60 or 61. NE incremented.
UP	NO	0	FRMR sent. W = 1 X = 1
UP	NO	1	DISREGARD
UP	YES	0	FRMR sent. W = 1 X = 1
UP	YES	1	Error interrupt 60 or 61. NE incremented.

If TRCV = 1 and UF (no I-field) is received, there will be an Error interrupt 62 or 63, independent of the link state or the readiness of RLOOK.

Of course, the received C-field of any frame will be in Register #7 provided the A-field matched either Register E or F, the FCS was good, and the frame contained 32, or more, bits.

APPENDIX B

HALF DUPLEX OPTION

The WD2511 is basically a full duplex device. The receiver is maintained in an "always ready" condition even if the receive buffer is not ready. Thus, whether the received frame came from a full or half duplex system is of no consequence to the WD2511.

Therefore, the half duplex option affects only the WD2511 transmitter. Half duplex is enabled when H/$\overline{F}$ (CR05) = 1.

The WD2511 will transmit one frame at a time according to the following procedure:

A. Enable $\overline{RTS}$ ($\overline{RTS}$ goes low).

B. Wait for $\overline{CTS}$ ($\overline{CTS}$ input goes low).

C. Transmit frame (when $\overline{CTS}$ is active).

D. Remove $\overline{RTS}$ ($\overline{RTS}$ goes high $2^1/_2$ bits of time after the last 0 of the trailing flag.)

NOTES:

The leading flag will be transmitted somewhere between 5 and 13 bits after $\overline{CTS}$ goes low.

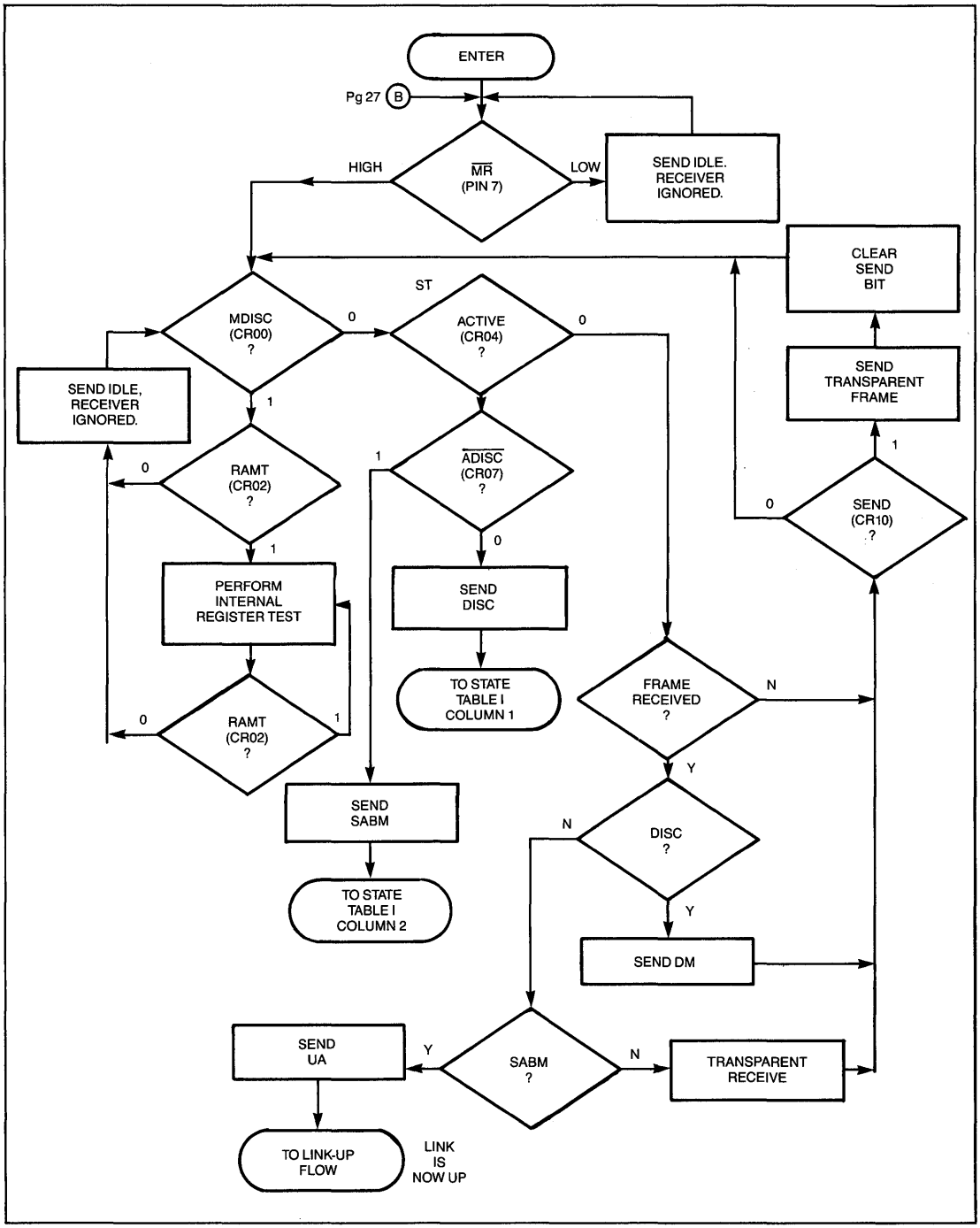
Interframe fill will be all 1's (IDLE).

If T1 is internally activated it is started when $\overline{RTS}$ goes low.

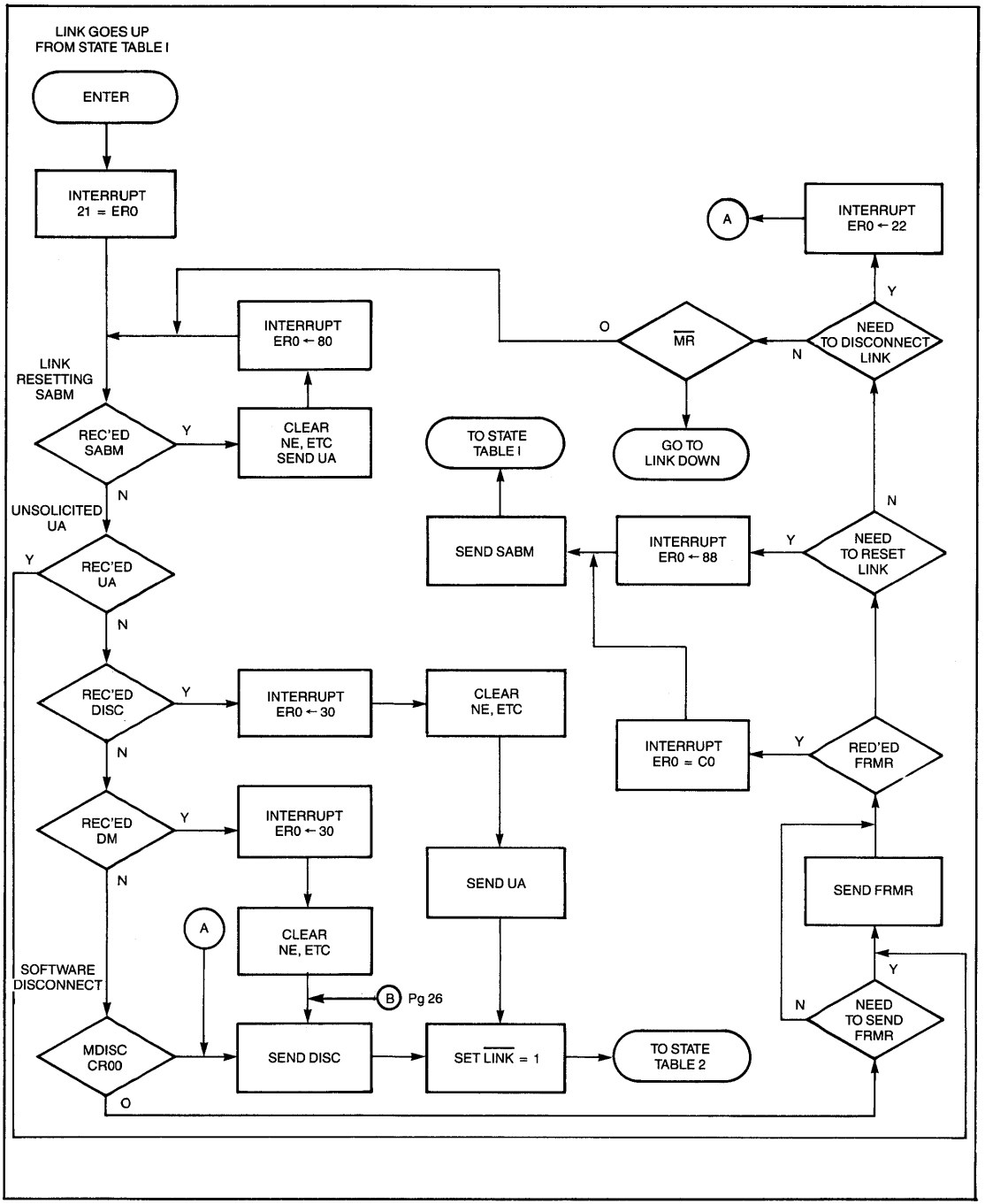
After $\overline{RTS}$ goes low, the frame will not begin transmission until $\overline{CTS}$ goes low. After the frame has started, the transmission of that frame is completed even if $\overline{CTS}$ returns high during the frame.

APPENDIX C STATE DESCRIPTIONS

LINK DOWN



CONDITION FOR RESET OR DISCONNECT LINK IS UP



STATE TABLE I
LINK DOWN, BUT GOING UP

(Column 2 also applies to link reset)

ACTION BY WD2511

STIMULUS:	COLUMN 1: DISC sent. Waiting for UA or DM.	COLUMN 2: SABM sent. Waiting for UA.
T1 runs out	Re-send DISC. P = 1.	Re-send SABM. P = 1.
T1 and N2 run out	Re-send DISC. P = 1.	Send DISC. Interrupt ER0 = 24. Go to column 1
Received UA	Send SABM. Go to column 2	Clear NA, NB, NE, V(R), V(S). Go to link up flow.
Received DISC	Send DM.	Send DM.
Received SABM	Disregards	Send UA. Clear NA, NB, NE, V(R), V(S). Keep waitiing for UA.
Received DM	Send SABM. Go to column 2.	Send DISC. Go to column 1.
Received something other than UA, DM, DISC, or SABM	Disregard.	Disregard.

STATE TABLE II
LINK GOING DOWN (WAS UP)

User sets MDISC, Chip sends DISC.

ACTION BY WD2511

STIMULUS	DISC sent. Waiting for UA.
T1 runs out	Re-send DISC. P = 1.
Received UA or DM	Go to Link Down Flow
Received SABM	Disregard
Received DISC	Send DM. Go to Link Down Flow
Received something other than DISC, SABM, UA, or DM	Disregard.

USE OF FLAGS BY THE WD2511

Once MDISC has been reset the WD2511 will send interframe flags (hex 7E) if full duplex is selected (CR05 = 0) (point ST of the Link Down Flow point has been entered). If half duplex is selected, (CR05 = 1), interframe fill will be all 1's (IDLE).

The WD2511 does not require the interframe time fill flags. Either idle or flags will be accepted. However, if the receiver detects idle for time T1 X N2, the WD2511 will send a DISC.

When sending continuous flags, the WD2511 will send:

0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 0 1 1 . . .

The WD2511 will accept either the above sequence as continuous flags, or the "shared zero" pattern:

0 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 . . .

DEFINITIONS OF COMMAND AND RESPONSE

A transmitted or received command or response is a frame with the A-field defined below:

FRAME	A-FIELD =
Transmitted Command	Register E
Received Command	Register F
Transmitted Response	Register F
Received Response	Register E

For non-transparent transmitted frames, only commands or responses are transmitted. A transparent transmitted frame (TXMT = 1) may have any A-field the user chooses.

All received frames must be either commands or responses or the frame is disregarded ("thrown away"), even if transparent receive is enabled (TRCV = 1).

STATE TABLE III
SENDING I-FRAMES (PACKETS) AND S-COMMANDS

NOTES:
In all subsequent pages, the link is considered Up (LINK = 0) unless otherwise stated. X = don't care. TXMT = 0 for Table III.

SEND	BRDY	NA AND NB	RNRR	T1 EXPIRES	RCVD REJ	ACTION BY WD2511
1	0	X	0	No	No	Clear SEND (CR10)
1	1	X	0	No	No	Send next packet with N(S) = NB. After transmission complete. Increment NB. Exception: If NB + 1 = NA, do not send next packet. There are 7 outstanding.
X	X	X	1	Yes	No	Send S-command, P = 1.
X	X	not =	X	Yes	No	Send S-command, P = 1.
X	X	not =	X	No	Yes	Make NA = received N(R). Start sequential retransmission of packets beginning with N(S) = NA. See Note 3.

NOTES ON STATE TABLE III

1. Received S-frames in Table III are assumed to have valid N(R)'s.
2. When an acknowledgement of one or more previously transmitted packets is received, NA is set equal to the received N(R). All TLOOK segments from the old value of NA up to N(R) — 1 are acknowledged and the appropriate ACKED bits in the TLOOK segments will be set. After setting the ACKED bits, an XBA interrupt is generated.
3. Assuming appropriate TLOOK segments are ready, packets are transmitted sequentially without waiting for an acknowledgement, with three exceptions:
   a. There are already seven outstanding (unacknowledged) packets (NB + 1 = NA).
   b. The remote station has indicated a busy condition by sending an RNR frame (RNRR). T1 is started and an S-command will be transmitted with P = 1 when T1 expires.
   c. T1 expired and there are one or more outstanding packets. An S-command will be transmitted with P = 1.
4. If an S-frame command is received, the WD2511 will transmit an S-frame response at the next opportunity.
5. If SEND = and TXMT = 1, a frame will be transmitted from the next TLOOK segment if BRDY = 1. After transmission, SEND is cleared by the WD2511.

RECEIVING AND TRANSMITTING A NULL PACKET

If an error-free (FCS good) packet is received with a correct N(S), but has no I-field, that packet will be treated the same as a packet with an I-field. The fact that there was no I-field is shown by RCNT equal to all 0's.

The WD2511 will not transmit a null packet. TCNT must not be allowed to be all 0's.

SENDING A REJ (RESPONSE)

1. The REJ condition is entered any time an error-free packet is received with an out-of-sequence N(S). Exception: If the received N(S) + 1 = V(R), then the received N(S) has been acknowledged, and either an RR or RNR is transmitted.
2. When the REJ condition is entered, the REJ frame with N(R) = V(R) is transmitted immediately if a packet is not being transmitted, or, at the completion of the current packet. There are two exceptions, as noted in 3 and 4 below.
3. If a link resetting SABM needs to be transmitted, the SABM is sent. When the UA is received for the SABM, the REJ condition is cleared.
4. If the receiver is not ready (RNRX = 1), the REJ is not sent.
5. Once the REJ condition is entered, only one REJ will be transmitted. Another REJ is not transmitted unless the REJ condition is cleared and re-entered. The REJ condition is cleared if a packet is with correct N(S) if a SABM is received, or if a SABM is transmitted and a UA received.
6. When the REJ is transmitted, error counter #6 is incremented.

RECEIVING A REJ (RESPONSE OR COMMAND)

Suppose a REJ has been received error-free with no I-field, then:

1. If the N(R) is not valid, an interrupt is generated with ER0 = C8, and a FRMR is transmitted.

2. If the N(R) is valid, and greater than NA, at least one transmitted packet is acknowledged. The appropriate ACKED bits in TLOOK are set and an XBA interrupt is generated.
3. If the N(R) is valid and less than NB, the WD2511 will begin sequential retransmission starting with V(S) = received N(R). If a packet is being transmitted when the REJ was received, that packet is aborted. If the N(R) is valid and equal to NB and a packet is being transmitted, that packet (which will be #NB) is aborted and retransmission will begin.
4. If the N(R) is valid and equal to NB and there is no packet being transmitted, there is no retransmission initiated. In this case the REJ has the same effect as an RR.
5. If in 2, 3, or 4 above, the received REJ is a command, the WD2511 will transmit a RR or RNR response at the next respond opportunity.

DEFINITION OF VALID RECEIVED N(R)

Reference
CCITT Recommendation X.25 paragraphs 2.4.10 and 2.3.4.10.

Definition
A valid received N(R) is greater than or equal to NA, and less than or equal to NB.

1. The "greater than" and "less than" relationships must be understood in a circular sense. 0 could be greater than 7 depending on the values of NA and NB.
2. If NA = NB, there is only one possible valid received N(R), N(R) = NA.
3. If NB + 1 = NA, there are seven outstanding packets and any received N(R) will be valid: N(R) = NB ACK's all of the outstanding frames, N(R) = NA ACK's none of them, and an N(R) in between ACK's some of the packets.
4. Basically, a received N(R) which is not valid is one which acknowledges a packet, or packets, never transmitted.

STATE TABLE IV
LOCAL STATION BUSY (SENT RNR: RNRX = 1)

$\overline{\text{LINK}}$	RECR	REC RDY	ACTION
1	X	X	No S-frame transmitted when link down.
1 → 0	1	1	RLOOK ready. No RNR frame sent.
1 → 0	1	0	RNR response sent immediately after link Up. RNRX set. RLNR Interrupt
1 → 0	0	X	RNR response sent immediately after link Up. RNRX set. No RLNR interrupt
0	1	1	Receiver ready to accept packets.
0	1 → 0	1	Receiver ready to accept packets.
0	1	0	RNR response sent. RNRX set. RLNR Interrupt.
0	0 → 1	1	If RNRX was set, then RNRX will be cleared after the next received packet or S-command. After that, an RR or REJ response is sent.
0	0	0	RNR response sent. RNRX set. There is no RLNR interrupt.

NOTES ON STATE TABLE IV

1. The arrows (→) indicate a change in state from the value on the left to the value on the right.
2. The RNRX status bit is set at the time the receiver-not-ready condition was established. The RNR frame will be sent immediately if no packet is being sent or after the end of the current packet.
3. When a received packet is brought into memory with RNRX = 0, the packet will be accepted provided the FCS and N(S) are correct and the I-field is not too long. The N(R) may or may not be correct but is checked separately. If N(R) is not valid, a FRMR is transmitted.
4. Whenever RNRX = 1, the I-field of a received frame is not brought into memory. For received packets, the N(S) and N(R) are checked as usual. If the N(S) is out-of-sequence, the REJ will not be transmitted.
5. If a link resetting SABM is transmitted when RNRX = 1, RNRX will be cleared when the UA is received. If the condition which caused receiver-not-ready still exists, an RNR is sent and RNRX is set. However, if the receiver instead is ready, I-field data may be brought into memory.

   The same also applies when a link resetting SABM is received.

STATE TABLE V
REMOTE STATION BUSY (RECEIVED RNR: RNRR = 1)

SEND	NA AND NB	RECVD ACK?	RECVD RNR	RECVD RR, REJ OR UA	T1 EXPIRES	ACTION
X	not =	Yes	Yes	No	No	Set RNRR. Restart T1 and N2. Update NA.
0	Equal	No	Yes	No	No	Set RNRR. Start T1.
X	not =	No	No	No	Yes	Send S-command (P = 1). If RNR subsequently received restart T1 and N2.
X	not =	Yes	No	Yes, but not UA	No	Clear RNRR. Restart T1 and N2. Update NA.
X	X	X	No	Yes	No	Clear RNRR.
0 → 1	Equal	No	No	No	No	Send next packet. Increment NB after transmission. (Then, NB does not = NA). Start T1 and N2.

2. NOTES OF TABLE V

1. If SEND = 1, it is assumed for this table that BRDY of the next TLOOK segment is set.
2. If RNRR = 1, an RR or RNR command is transmitted at T1 intervals.

SENDING S-FRAME COMMANDS

When an S-frame command is to be transmitted, an RR command is transmitted if RNRX = 0 or an RNR command is transmitted if RNRX = 1. If RNRX = 0, and a REJ is waiting to be transmitted, a REJ command is transmitted.

For all transmitted S-commands, the P bit is set to 1.

An S-command will be transmitted at T1 intervals if an RNR is received (RNRR = 1) or if T1 has expired due to waiting for an acknowledgement to previouusly transmitted packets.

CONDITIONS FOR SENDING SABM (LINK RESET)

1. FRMR received.
2. Have sent an S-command N2 times with P = 1 (at T1 intervals) without receiving an S-response with F = 1.

UNSOLICITED UA OR UNSOLICITED F BIT

If an unsolicited UA or an unsolicited F bit is received with the link up, a FRMR will be transmitted with W = 1.

SENDING AN FRMR

An FRMR may be transmitted for any of the reasons indicated in X.25 (W, X, Y, Z). An FRMR is transmitted only if the link is up.

Upon sending a FRMR, the WD2511 will not send a packet until the FRMR condition is cleared. The WD2511 will also discard any received I-fields. The FRMR condition is cleared when either a SABM or DISC is received.

If an S or I-frame is received which acknowledges a previously transmitted packet(s), the acknowledgement(s) is accepted, the appropriate ACKED bits in TLOOK are set, and there is an XBA interrupt.

While in the FRMR condition, the WD2511 will act as shown below:

FRAME RECEIVED	ACTION BY WD2511
SABM	Send UA. Clear FRMR condition. Enter information transfer phase.
DISC	Send UA. Clear FRMR condition. Enter logical disconnect state.
Packet with good N(R)	Retransmit FRMR
S-frame with good N(R) (command or response)	Retransmit FRMR
Packet or S-frame with bad N(R)	Transmit new FRMR (Z = 1)
Any frame with violation W, X, Y	Transmit new FRMR

RECEIVING AN FRMR

After a FRMR has been received:

1. The FRMR I-field will bee in the memory referenced by the current NE segment, provided the receiver was ready.
2. The SEND bit is cleared.
3. No more I-field data is allowed to come into memory until the user makes the receiver memory ready.
4. A link resetting SABM is transmitted and an error interrupt, ER0 = C0 is generated.
5. After the UA is received for the SABM, the NA, NB, NE, V(R), and V(S) are cleared to 0.

PROTOCOL SIGNIFICANCE OF TLOOK/RLOOK POINTERS

The NE, NA, and NB pointers have a relationship with the sequence counters used in the LAPB protocol.

The RLOOK pointer NE is equal to V(R) at all times if TRCV = 0. However TRCV = 1 and the link is UP, there is no guaranteed relationship between NE and V(R).

TLOOK pointer NB is the Next Block to be transmitted. If the chip is not in packet retransmission, NB is equal to the V(S) of the next new packet to be transmitted.

TLOOK pointer NA is the Next packet to be Acknowledged. It represents the V(S) number for the oldest packet in the retransmission buffer.

USE OF THE RECR BIT

The RECR (CR01) bit should be understood as an instruction to the WD2511 to enable the receiver function. The WD2511 will test RECR as soon as MDISC is cleared, and will retest RECR after each link set-up and each link reset. Once the receiver is ready, the WD2511 will not test RECR again unless there is a link set-up or a link reset.

The receiver-not-ready condition is indicated by RNRX = 1. This condition is cleared after the user makes RECR = 1 with RECRDY = 1 (in RLOOK #0) and after either a packet or an S-frame is received from the remote station.

If RECRDY of the next RLOOK is 0 but RECR = 0, there will not be an RLNR interrupt, but RNRX will be set. If RECR = 1 but the RECRDY bit of the next RLOOK segment is 0, there will be an RLNR interrupt (error code 10) and RNRX will be set.

HOST PROCEDURE FOR LINK RESET

The host should keep its own set of variables to determine the index of the Next Packet to be Received and the Next Packet to be Acknowledged because if a Link Reset occurs, the chip resets its NA, NB, and NE counters. After a Link Reset the host should look for unprocessed received packets (FRCML = 1) in the RLOOK table beginning at its Next Packet to be Received segment and proceeding in order until it finds FRCML = 0. Furthermore, if RLOOK0 has RECRDY = 1 and RECR is set to 1, a packet can be stored into RLOOK0 immediately after a Link Reset. Therefore, the host should also look for received packets beginning at RLOOK0 after a Link Reset.

The chip resets the SEND bit after a Link Reset so no new TLOOK buffers will be sent until the host sets SEND again. After a Link Reset the host should look for any unprocessed acknowledged packets (ACKED = 1) in the TLOOK table beginning at its Next Packet to be Acknowledged segment and proceeding in order until it finds a segment with ACKED = 0. Then the host must set up the TLOOK segments again so that the oldest unacknowledged packet is in TLOOK0, the next in TLOOK1, and so on, setting the BRDY = 1 in each occupied segment. (New packets may be added to the TLOOK at the next available segment.) When the host has finished setting up the TLOOK segments, it should set the SEND bit to 1. At this point packet transmission will resume if the remote station is up and is not in a receiver not ready (RNRR = 1) condition.

When presenting packets to the chip for transmission, the host should implement a timer. The value of the timer is system dependent and varies with packet size and line speed but should be in the order of seconds. If a packet has not been acknowledged by the time the timer expires, the host should check the SEND bit. If it is reset, set it to 1 again and restart the timer. If it was still set, the link must be reset. Do this by setting the MDISC bit (CR00 = 1), waiting for the link to go down (LINK = 1), then resetting MDISC (CR00 = 0), and waiting for the link to come back up (ER0 = 21 or, if RLOOK0 was not ready, 11 and LINK = 0).

For more software information refer to the WD2511 Application Note.

APPENDIX D

GLOSSARY OF DATA COMMUNICATIONS TERMS

The following is a list of industry-accepted data communications terms that are applicable to this specification.

ABM	Asynchronous Balanced Mode
ADCCP	Advanced Data Communications Control Procedure (ANSI BSR X3.66)
ANSI	American National Standards Institute
ARM	Asynchronous Response Mode
CCITT	International Consultative Committee for Telegraphy and Telephony
CMDR	Command Reject. A U-Frame
DCE	Data Circuit Termination Equipment (the network side of the DTE/DCE link)
DISC	Disconnect. A U-Frame
DTE	Data Terminal Equipment
DM	Disconnect Mode. A U-Frame (LAPB, only)
ECMA	European Computer Manufacturers Association
FCS	Frame Check Sequence
FDX	Full Duplex (also called "two way simultaneous")
FRAME	Basic serial block of bit-oriented data. Includes leading and trailing flags, address field, control field, FCS field, and an optional information field.
FRMR	Frame Reject. A U-Frame (LAPB, only)
HDLC	High-Level Data Link Control (ISO 3309)
HDX	Half Duplex (also called "two way alternate")
HOST	Another name for a DTE
I-Frame	Information Frame. Control field bit 0 is 0. In X.25 an I-frame is a packet.
ISO	International Standards Organization
LINK	The logical and physical connection between two data terminals
LAP	Link Access Procedure
LAPB	Link Access Procedure Balanced
N2	Maximum number of retransmissions of a frame. (Also called retransmission count variable.)
NODE	Another name for a DCE or DTE.
N(R)	Sequence number of next frame expected to be received.
N(S)	Sequence number of current frame being transmitted.
OCTET	An 8-bit byte
PACKET	An I-Frame in X.25
PAD	Packet Assembly/Disassembly facility
REJ*	Reject. An S-Frame
RNR*	Receiver Not Ready. An S-Frame
RR*	Receiver Ready. An S-Frame
S-Frame	Supervisory Frame. Control field bit 0 = 1 and bit 1 = 0
SARM	Set Asynchronous Response Mode. (LAP, only)
SABM	Set Asynchronous Balanced Mode. (LAPB, only)
SDLC	Synchronous Data Link Control (IBM document GA27-3093)
T1	A Primary Timer for a delay in waiting for a response to a frame
U-Frame	Unnumbered Frame. Control Field bit 0 = 1 and bit 1 = 1
UA	Unnumbered Acknowledge. A U-Frame
X.25	Recommendation by CCITT on Interfacing to Public Packet Switching Networks

X.3, X.28, X.29 Recommendations by CCITT involving PAD facilities

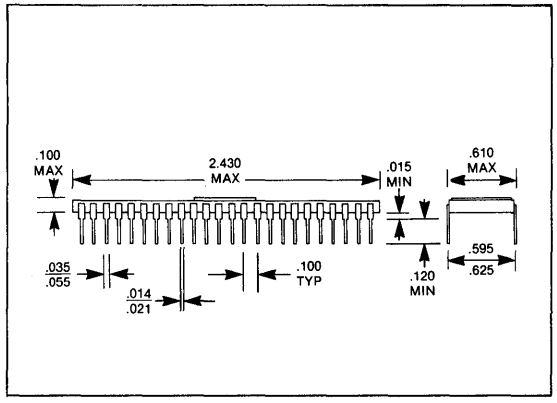
*There are also RR, RNR, and REJ packets which are not the same as the S-frame RR, RNR and REJ discussed in this document.

ORDERING INFORMATION

Order Number	Maximum Data Rate
WD2511AN-01	100 Kbps
WD2511AN-05	500 Kbps
WD2511AN-11	1.1 Mbps*

*Higher speeds available on special order.

Package Diagram



48 LEAD CERAMIC "T" or "AN"

APPLICATION NOTE

Application Note
Using The WD2511

This application note provides an introduction to the X.25 communication protocol and introduces the ISO reference model. The link layer of X.25 is highlighted as it can today be implemented with a single LSI device, the WD2511.

The bulk of this document provides details of the hardware and software interfaces that a user typically encounters when using the WD2511. Schematic and timing diagrams for a typical Z80 interface along with high level flowcharts for initialization and operation are given. This circuitry is applicable for applications where the TC/RC speed is 64 Kbps and below.

CONTENTS

1.0 THE WD2511 GENERAL DESCRIPTION

The WD2511 is an LSI device that fully handles the link level (level 2) of the CCITT X.25 communications protocol.

In addition to the traditional parallel/serial converters and FCS logic, the WD2511 incorporates a highly efficient micro-programmed processor that fully handles the required link set-up and frame sequencing operations conventionally delegated to a "user defined" processor. The WD2511 also contains an intelligent two-channel DMA controller to further simplify its integration into a user's system.

2.0 THE WD2511 AND THE ISO MODEL

The CCITT X.25 recommendation comprises three levels of protocols (Level 1 to 3). See Figure 1.

Level 1 is the physical level, which concerns the actual means of bit transmission across a physical medium.

Level 2 is the link level which includes frame formatting, error control and link control.

Level 3 is the packet (network) level which controls the traffic of the different virtual calls and multiplexes these for passage over the physical line.

These three levels are completely independent of each other, which allows changes to be made to one level without disrupting the operation of any other level. An adjacent level is affected only if the changes affect the interface to that level.

Each level performs one well defined set of functions, using only a well defined set of services provided by the level below. These functions implement a set of services that can be accessed only from the level above. Each level is strictly controlled by the systems engineer according to formal functional and interface specifications.

The WD2511 implements level 2. Without additional logic, it generates the frame, performs error checking, performs link management (set up/disconnect) and ensures reliable data transmission by evaluating the sequence number associated with each I-frame. The device automatically acknowledges received I-frames and fully supports up to 7 outstanding (unacknowledged) frames, including retransmission if required.

3.0 HARDWARE

The WD2511 must be connected to the Physical Level (Level 1). This generally amounts to simple line drivers/receivers.

A typical X.25 DTE/DCE station block diagram is shown in Figure 2. Figure 3 shows a circuit diagram of the actual X.25 hardware interface of this same station. Table 1 is a description of signal functions for this circuit diagram. This is to be connected directly to a Z80 microprocessor on one side and an EIA RS-422 interface on the other side.

Figures 4 and 5 are DMA cycle timing diagrams for this particular station.

General notes to this interface:

- A modem would be needed for long-distance communication lines.
- The hardware interface in Figure 3 includes all hardware options. Simpler interfacing is possible.
- The function of the CPU Bus Driver Control Circuit (CBDCC) is to control the direction and/or timing of the data-line transceivers and the two address latches.
- If the CPU clock frequency is not higher than the WD2511 CLK maximum frequency, the High Speed Control Circuit (HSCC) is not needed. The function of the HSCC circuit is to divide a high speed CPU

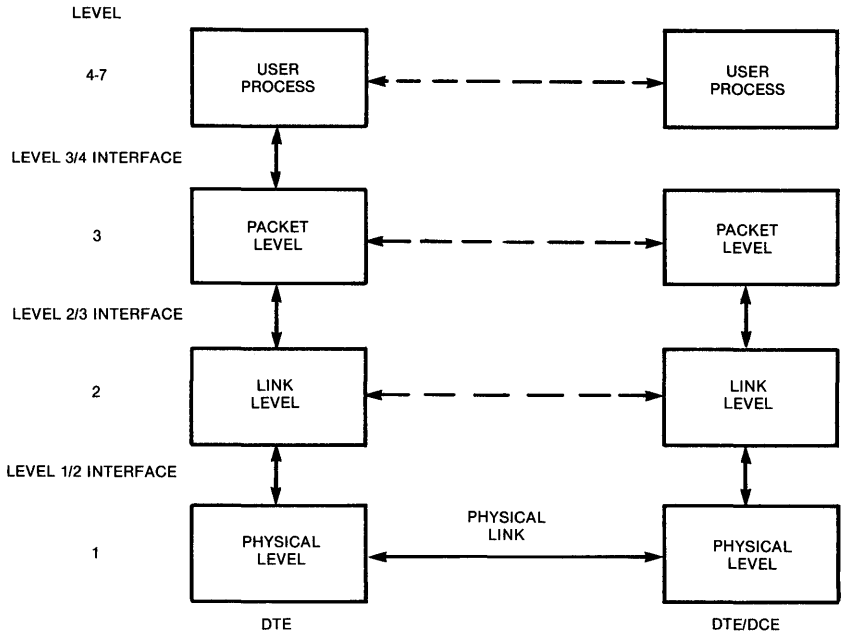


Figure 1. LAYERED ARCHITECTURE FOR COMPUTER NETWORKS

The only real physical connection between the two stations (DTE and DTE/DCE) is the Physical Link between the two physical layers. The other connections shown between two of the same layers (peer to peer interface) is not a physical but rather a logical connection made up by the respective protocols for that particular level.

Each level n "interfaces" to the corresponding level n on the other side of the Data Communication Link through the level n-1, then n-2 etc., via the physical link and up through the levels to n-2, n-1 and to level n.

clock signal (0) down to half the frequency (01A). It also delays the reset of $\overline{\text{BUSRQ}}$ with one additional 01 clock cycle when a high speed CPU clock is used. These functions are needed to establish a time window of at least 500ns between $\overline{\text{DACK}}$ being active and a CPU Write/Read function.

- When a high speed CPU clock is used, connect 01A signal to 01 signal and $\overline{\text{BUSRQA}}$ signal to $\overline{\text{BUSRQ}}$ signal. When a low speed CPU clock is used, connect CPU clock (0) direct to 01 signal and $\overline{\text{BUSRQ2}}$ signal to $\overline{\text{BUSRQ}}$ signal.
- The DMA I/O circuit matches the timing between the Z80 and the WD2511.
- The $\overline{\text{RTS}}$ open collector output needs a pull-up resistor.
- In this particular example, line drivers/receivers are of type EIA RS-422. However, RS-232C or RS-423 can also easily be used.
- Port A of a PIO in this example is programmed to be an output. In this case, the CPU controls the DTR output to the modem. Port B of the PIO is programmed to be interrupt controlled inputs; the CPU can be interrupted by $\overline{\text{DSR}}$ and/or $\overline{\text{INTR}}$ as programmed.
- $\overline{\text{MRW}}$ (Memory Read/Write) signal enables the output of the memory address decoder for the computer system memory chips. As an example, if a PROM type 28S42 is used as the memory address decoder, $\overline{\text{MRW}}$ is connected direct to $\overline{\text{E}}$ (Pin 15) input.
- The WD2511 $\overline{\text{CS}}$ input is to be connected to a port address decoder (or memory address decoder). $\overline{\text{MWE}}$ is connected to all $\overline{\text{WE}}$ inputs, and $\overline{\text{MOE}}$ is connected to all $\overline{\text{OE}}$ inputs of the system memory chips.
- $\overline{\text{REPLY}}$ output is not used in this application.

3.1 READ/WRITE CONTROL OF I/O REGISTERS

The sixteen I/O registers are directly accessible from the CPU data bus (DAL0-DAL7) by a read and/or write operation by the CPU. The CPU must activate the WD2511 register address (IA0-IA3). Chip Select ($\overline{\text{CS}}$). Write Enable ($\overline{\text{WE}}$) or Read Enable ($\overline{\text{RE}}$) before each data bus transfer operation. The read/write operation is

completed when $\overline{CS}$ or $\overline{RE}/\overline{WE}$ is brought high. During a write operation, the falling edge of $\overline{WE}$ will initiate a WD2511 write cycle. The addressed register will then be loaded with the content of the Data Bus. The rising edge of $\overline{WE}$ will latch that data into the addressed register.

During a read operation, the falling edge of $\overline{RE}$ will initiate a WD2511 read cycle. The addressed register will then place its content onto the Data Bus.

The CPU must set-up all transmit data, TSADR HI and LO, TCNT HI and LO, and residual bits before setting BRDY in the applicable TLOOK segment.

The CPU must set aside receiver memory (at least one chain segment with transfer address), and set-up RSADR HI and LO before setting REC RDY in the applicable RLOOK segment.

3.2 DMA IN/OUT OPERATION

The Direct Memory Access (DMA) operation is completely controlled by the WD2511. During a DMA cycle, the CPU sets its address bus, data bus and three-state control signals to their high impedance states.

(See DMA In/Out timing diagrams, Figures 4 and 5.)

In this application example, the data bus transceivers are permanently enabled (low impedance state). When the CPU has control, the direction of these transceivers is pointing from the CPU bus towards the WD2511. During a DMA In cycle, this is not changed. During a DMA Out cycle however, the direction is reversed (WD2511 towards the CPU bus).

The address bus latches are in high impedance state while the CPU has control of the bus. When the WD2511 has control of the CPU bus, the address latches are in the low impedance state. During the DMA Out cycle, these latches function as regular bus drivers. During the DMA In cycle however, the address gets latched to assure enough data hold time for the WD2511.

3.2.1 DMA IN

During a DMA In cycle, the task of transferring one byte of I-field data from memory into the WD2511 is performed. The CPU time (in the example described in this paragraph to execute this task) is five T-states for a low speed CPU clock system and ten T-states for a high speed CPU clock system.

The DMA In function starts when the WD2511 is ready to receive a byte from memory to be transmitted out to the remote station. This condition causes the $\overline{DRQI}$ signal to go LO, which in turn activates the $\overline{BUSRQ}$ (Bus Request) signal. Also at this time (ADRV bit = 1), the WD2511 presents the address (on A0-A15) of the data byte to be retrieved from memory.

The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last CPU clock (0) period of any machine cycle. In this case, because the $\overline{BUSRQ}$ signal is active, the CPU goes into high impedance state with the rising edge of the next CPU clock pulse. At this time, the CPU also switches the control over to the WD2511 by activating the $\overline{BUSAK}$ signal. This causes $\overline{DACK}$ to go LO at the following rising edge of 01 clock. This is the actual indication for the WD2511 to start the DMA In cycle. $\overline{DACK}$ also causes $\overline{DRQI}$ to return to the HI state.

At the next rising edge of the 01 clock, $\overline{MOE}$ (Memory Output Enable) is activated. This causes the memory to output the addressed data byte onto the Data Bus. Also, the address is now latched into the address bus latches (74LS373) at this time.

At the next falling edge of the 01 clock, $\overline{DACK}$ gets deactivated, causing the WD2511 to latch the data byte (DAL0-DAL7) and to set its address lines (A0-A15) to logical HI state (ADRV bit = 1). The address bus latches hold the address active until $\overline{DMOE}$ signal is deactivated.

At the next rising edge of the 01 clock (low speed CPU clock), $\overline{BUSRQ}$ gets deactivated. When high speed CPU clock is used, $\overline{BUSRQ}$ is deactivated after an additional 01 clock cycle.

At the next following rising edge of 01 clock, $\overline{BUSRQ}$ is sampled by the CPU. This causes $\overline{BUSAK}$ and $\overline{MOE}$ to become deactivated, but not until the next falling edge of the CPU (0) clock. This is the end of the DMA In cycle. At the next rising edge of the CPU clock, the CPU again controls the CPU bus.

3.2.2 DMA OUT

This operation is very similar to the DMA In function. During this cycle, one byte of I-field data is transferred from the WD2511 to the memory. The CPU-time in this example described to perform this task is the same as for the DMA In cycle.

The DMA Out function starts when the WD2511 is holding a received I-field byte and is ready to transfer this to the memory. This condition activates the $\overline{DRQO}$ signal, which in turn sets the $\overline{BUSRQ}$ to LO. Also at this time (ADRV bit = 1), the WD2511 presents the address to the memory location to where the respective data byte is to be loaded.

The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last CPU clock period of any machine cycle. Since the $\overline{BUSRQ}$ signal is active, the CPU goes into high impedance state with the rising edge of the following CPU clock pulse. Now the CPU also switches the control over to the WD2511 by activating the $\overline{BUSAK}$ signal. This causes $\overline{DACK}$ to go LO at the next rising edge of 01 clock, which indicates to the WD2511 to start the DMA Out cycle. This causes $\overline{DRQO}$ to reset back to HI state and to load the data byte to be transferred onto the data-bus.

At the next rising edge of the 01 clock, $\overline{MWE}$ (Memory Write Enable) is activated. This causes the memory to input the addressed data byte.

At the following rising edge of the 01 clock, $\overline{MWE}$ goes HI, latching the data into the memory. Also at this time

TABLE 1. SIGNAL NAMES FOR THE HARDWARE INTERFACE (See Note)

NAME	SYMBOL	FUNCTION
RECEIVE	RCV	When activated (LO), sets the direction of the data bus transceivers from WD2511 towards the CPU bus. This is done only during CPU Read or DMA Out cycle.
DRM TRANSFER	$\overline{\text{DTFR}}$	When activated (LO), enables the output of the address bus latches. This is done during a DMA In/Out cycle.
DMA MEMORY OUTPUT ENABLE	$\overline{\text{DMOE}}$	Is activated during a DMA In cycle. Generates the $\overline{\text{MOE}}$ signal and latches the DMA In addresses.
MEMORY OUTPUT ENABLE	$\overline{\text{MOE}}$	Is activated during a DMA In or a CPU Read cycle. Enables the memory outputs. Is to be connected to the $\overline{\text{OE}}$ pin of the memory circuits.
MEMORY WRITE ENABLE	$\overline{\text{MWE}}$	Is activated during a DMA Out or a CPU Write Cycle. Enables the memory write function. Is to be connected to the $\overline{\text{WE}}$ input of the memory circuits.
MEMORY READ/WRITE	$\overline{\text{MRW}}$	Is activated during a DMA In/Out function or a Memory Read/Write cycle by the CPU. Enables the output of the Memory Address decoder.
DMA OUT	DMA OUT	Is activated during a DMA Out function.
DMA IN	DMA IN	Is activated during a DMA In function.
INTERNAL LOOP	ILOOP	Is activated during an internal loop-back test. Keeps the $\overline{\text{RTS}}$ signal to the modem in off condition and logically connects $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$.
BUS ACKNOWLEDGE 1	$\overline{\text{BUSAK1}}$	When active, indicates that the CPU has switched bus control over to the WD2511. Compared to $\overline{\text{BUSAK}}$ signal, this is delayed one 01 clock cycle when going LO to allow a time window of at least 500 ns before $\overline{\text{DACK}}$ becomes activated.
BUS REQUEST 1	$\overline{\text{BUSRQ1}}$	When active, requests the CPU via $\overline{\text{BUSRQ2}}$ and $\overline{\text{BUSRQ}}$ (low speed CPU clock) to switch control over to the WD2511.
BUS REQUEST 2	$\overline{\text{BUSRQ2}}$	Same function as $\overline{\text{BUSRQ1}}$, except that $\overline{\text{BUSRQ2}}$ is delayed one 01 cycle when going HI. The delay allows a time window of at least 500 ns between $\overline{\text{DACK}}$ being active and a CPU Read/Write function.
BUS REQUEST A	$\overline{\text{BUSRQA}}$	Same function as $\overline{\text{BUSRQ2}}$, except is delayed an additional 01 cycle when going HI. This delay allows the necessary 500 ns time window between $\overline{\text{DACK}}$ being active and a CPU Read/Write function when an high speed CPU clock is used. This is then directly driving the $\overline{\text{BUSRQ}}$ signal.

(low speed CPU clock), $\overline{\text{BUSRQ}}$ signal gets deactivated. When high speed CPU clock is used, $\overline{\text{BUSRQ}}$ is deactivated after an additional 01 clock cycle.

At the next rising edge of 01 clock, the $\overline{\text{BUSRQ}}$ signal is sampled by the CPU.

$\overline{\text{DACK}}$ goes HI half a 01 clock cycle after $\overline{\text{MWE}}$ goes HI. This ends the DMA Out cycle by the WD2511 setting its data-lines in high impedance state and the address-lines (A0-A15) to logical HI state (ADRV bit = 1).

After CPU has sampled and detected $\overline{\text{BUSRQ}}$ being deactivated, it resets $\overline{\text{BUSAK}}$ to HI at the next falling edge of the CPU clock.

At the next rising edge of the CPU clock, the CPU again controls the bus.

TABLE 1. (Continued) SIGNAL NAMES FOR THE HARDWARE INTERFACE (See Note)

NAME	SYMBOL	FUNCTION
01	01	Clock used for timing of this hardware interface. The 01 frequency is not allowed to be higher than the CLK maximum frequency of the WD2511. When a low speed CPU clock is used, 01 signal is connected directly to the CPU clock (0). When a high speed CPU clock is used, this is connected to the 01A signal.
01A	01A	Clock signal with half the CPU clock frequency. This is driving the 01 clock when a high speed CPU clock is used.
+5 RESISTIVE	+5R	+5V through a resistor.

NOTE: Signals described in this paragraph are signals generated by this circuitry only. Other signals are described in either the WD2511 device specification or in the Z80 CPU data sheets.

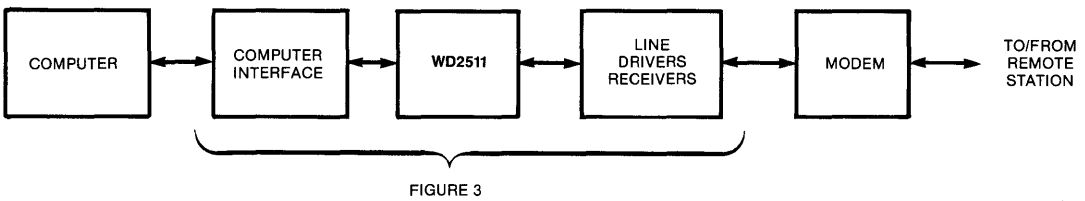


FIGURE 2. DTE/DCE STATION BLOCK DIAGRAM

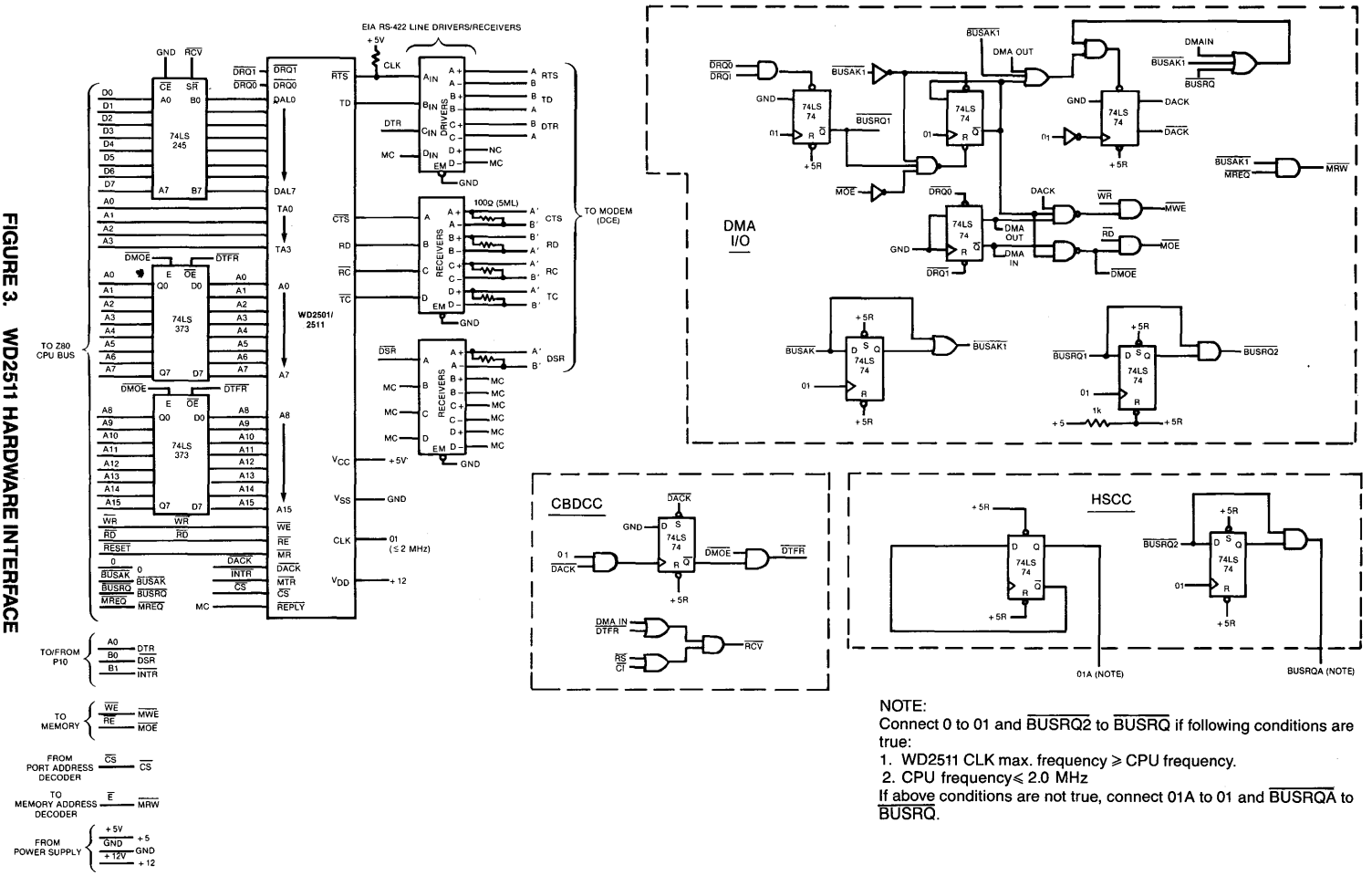
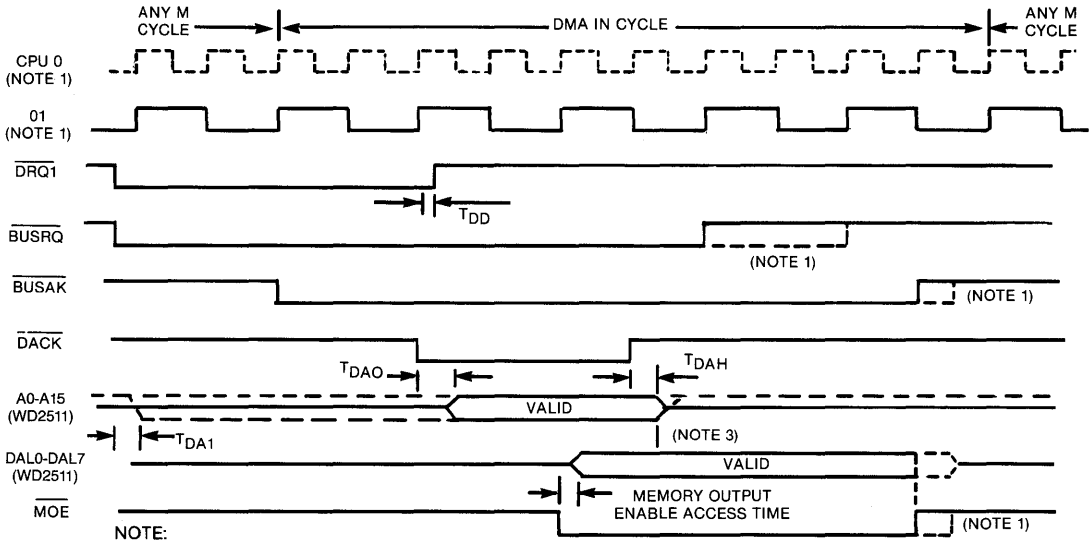


FIGURE 3. WD2511 HARDWARE INTERFACE

NOTE:
Connect 0 to 01 and $\overline{\text{BUSRQ2}}$ to $\overline{\text{BUSRQ}}$ if following conditions are true:

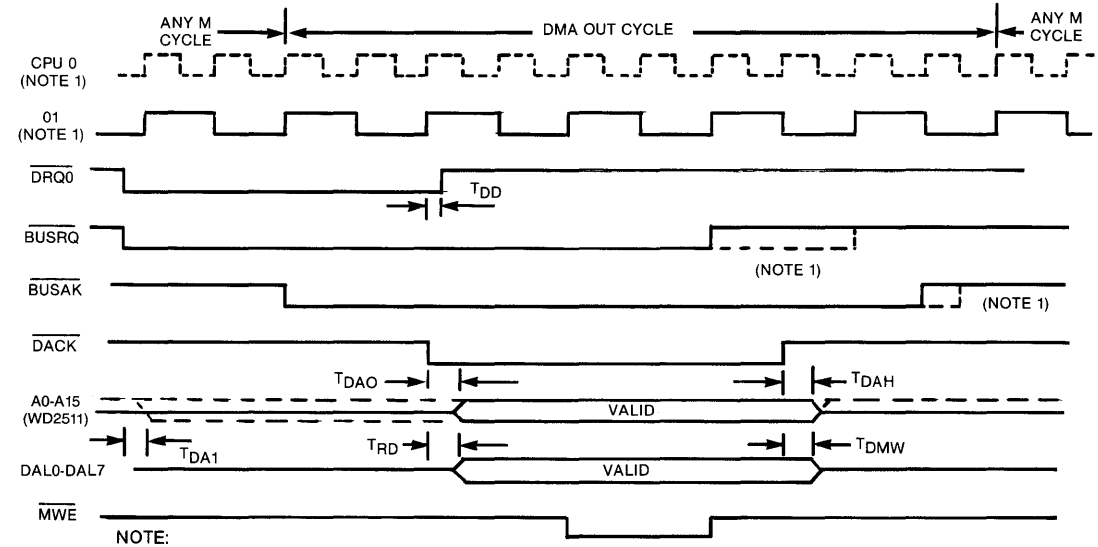
1. WD2511 CLK max. frequency ≥ CPU frequency.
2. CPU frequency≤ 2.0 MHz

If above conditions are not true, connect 01A to 01 and $\overline{\text{BUSRQA}}$ to $\overline{\text{BUSRQ}}$.



NOTE:
1. These dashed lines show the respective signals when a fast CPU 0 clock is used. Solid lines show same signals for a slow CPU 0 clock (CPU 0 = 01).
2. Propagation delay is omitted in this diagram unless timing symbol is shown.
3. Data would become non-valid after the address becomes non-valid if address latches were not used.

Figure 4. DMA IN TIMING



NOTE:
1. These dashed lines show the respective signals when a fast CPU 0 clock is used. Solid lines show same signals for a slow CPU 0 clock (CPU 0 = 01).
2. Propagation delay is omitted in this diagram unless timing symbol is shown.

Figure 5. DMA OUT TIMING

3.3 SERIAL INTERFACE

The receiver and transmitter sub-systems are completely independent of each other, the CPU Read/Write functions and the DMA In/Out functions.

The serial data is synchronized by the externally supplied $\overline{TC}$ clock and $\overline{RC}$ clock. The falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data.

After initilization and before the first frame is sent, the TD output sends Idles (continuous 1s).

After the first frame is sent or the ACTIVE/$\overline{PASSIVE}$ bit is set, continuous flags are sent in between frames.

For detailed information on what type of frames are sent for certain conditions, see the WD2511 specifications.

4.0 SOFTWARE

Initialization of the WD2511 and I-field data processing (level 3) is accomplished by user written software. This software need not be realtime, since the WD2511 responds to link exceptions and overhead functions on its own.

Configuring the WD2511 for certain test functions, modes, timer values, location of initial memory pointers, chain buffer lengths and link level addresses is performed via the sixteen I/O registers.

All buffer management support, buffer chaining and free/busy flags occur in user memory. Here two look-up tables (TLOOK/RLOOK), located in the user memory, contain pointers/counters for up to eight outstanding transmit/receive packets. The WD2511 contains only one address pointer which is the starting address of Segment #0 in the TLOOK table. Segment #0 in the RLOOK table always begins 40(Hex) bytes after TLOOK, Segment #0, byte #0. See section "Memory Access Scheme" in the WD2511 specifications.

Link monitoring is done by use of the I/O registers and the memory buffers. The WD2511 indicates to the system CPU that a certain event has occurred by setting a bit in status register 1 and setting the interrupt flag. This indicates whether a packet has been received, a transmitted packet has been acknowledged, a non-recoverable error condition or some other condition needs the attention of the CPU.

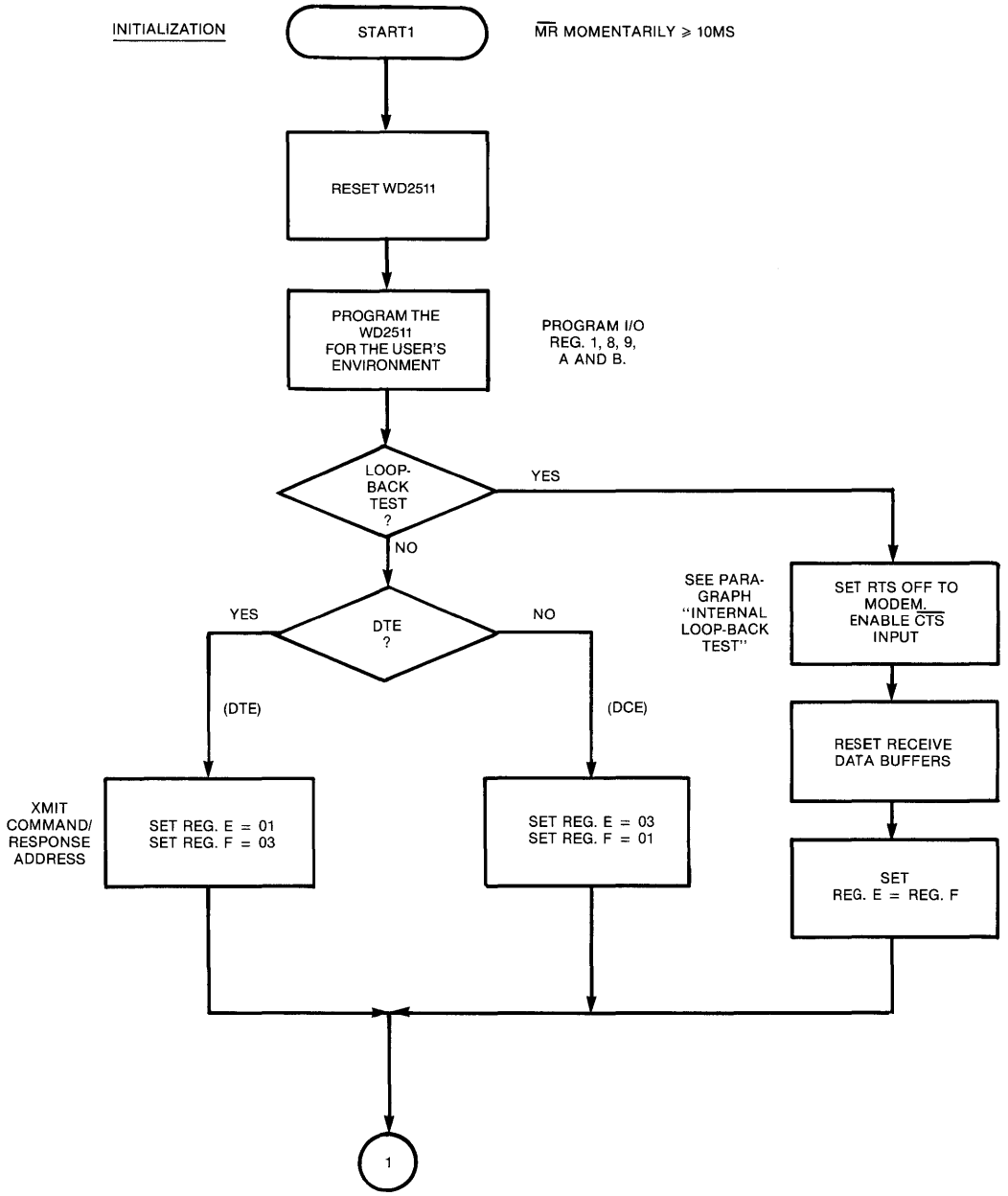
In this section a flow-chart is given to show the user how to program the WD2511. For more details refer to the data sheets.

The flow for programming/monitoring the WD2511 for transmitting or receiving a packet(s) or for a loop-back test is shown in the flowchart below. The flow starts at START1 if a power-up was just done and/or if no data communication environment programming (initialization) has been done.

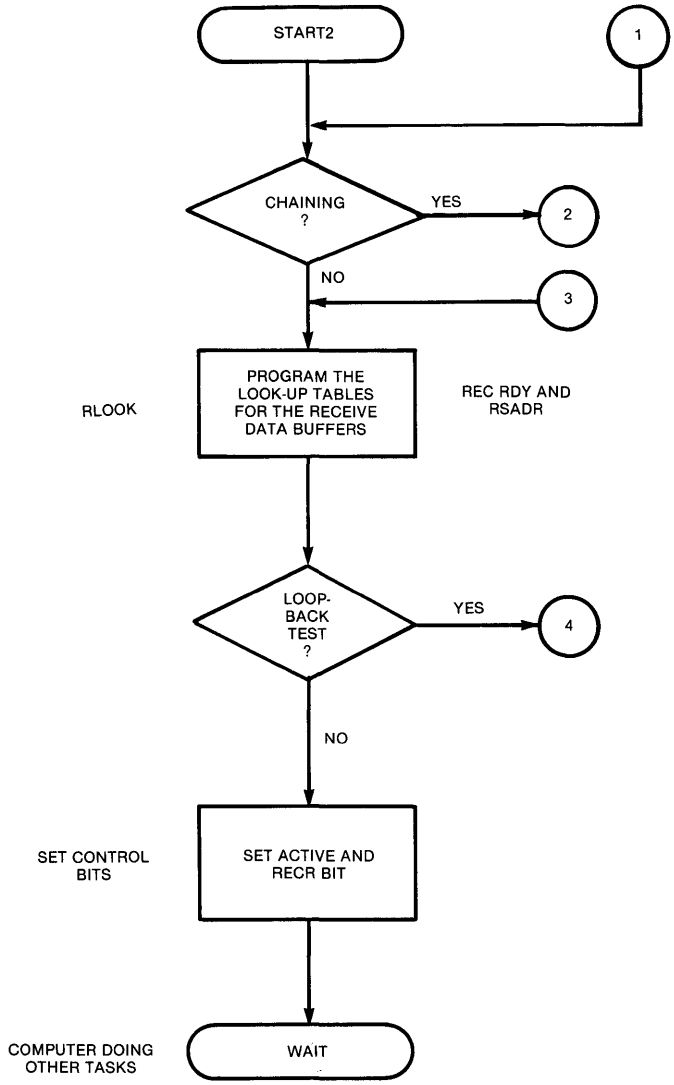
If initialization is complete, the flow starts at START2 when the WD2511 is to be enabled to receive a packet(s).

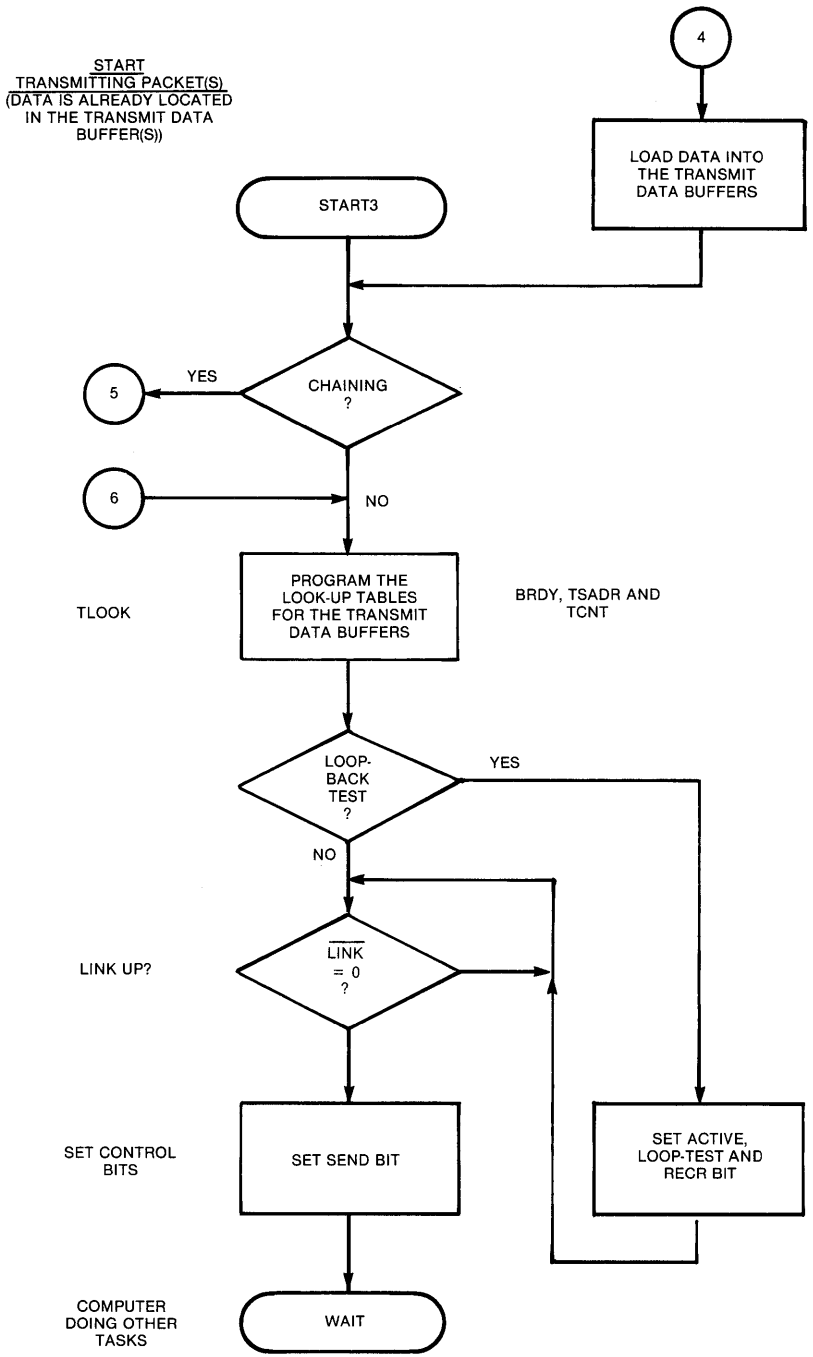
If a packet is to be transmitted and initialization is complete, the flow starts at START3.

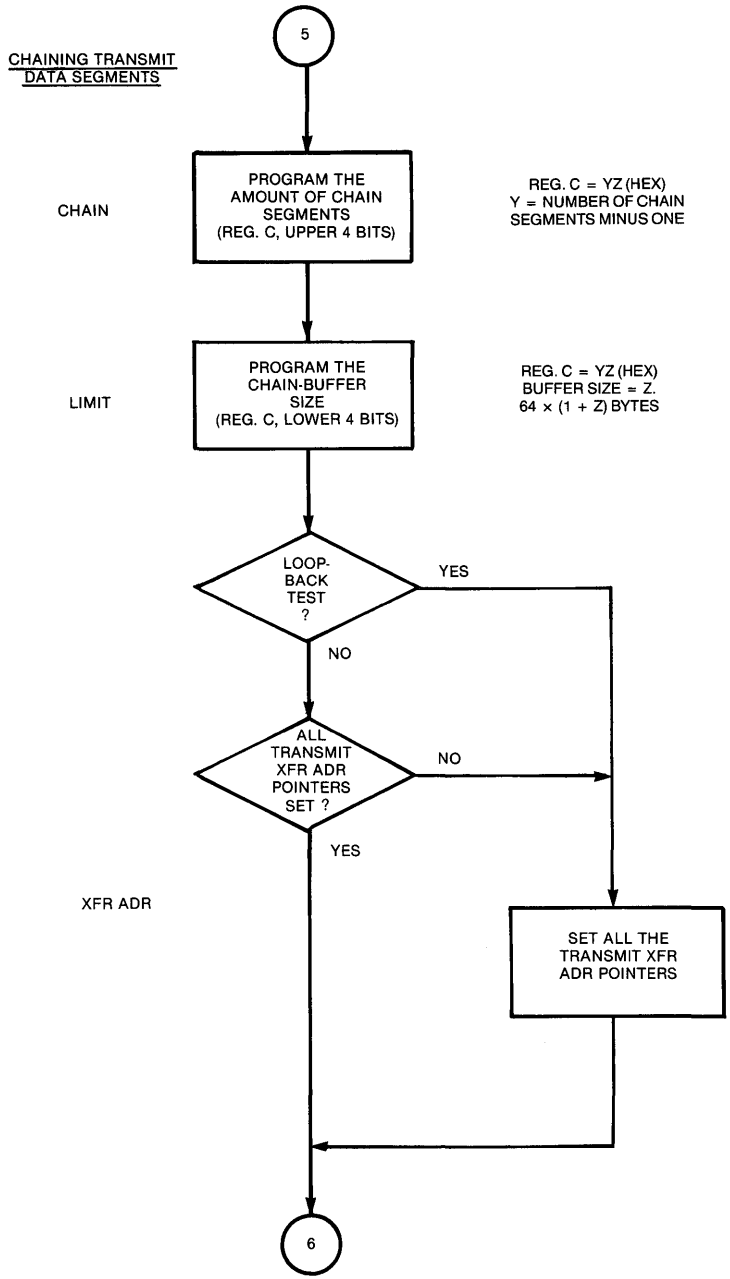
WD2511 PROGRAMMING FLOWCHART

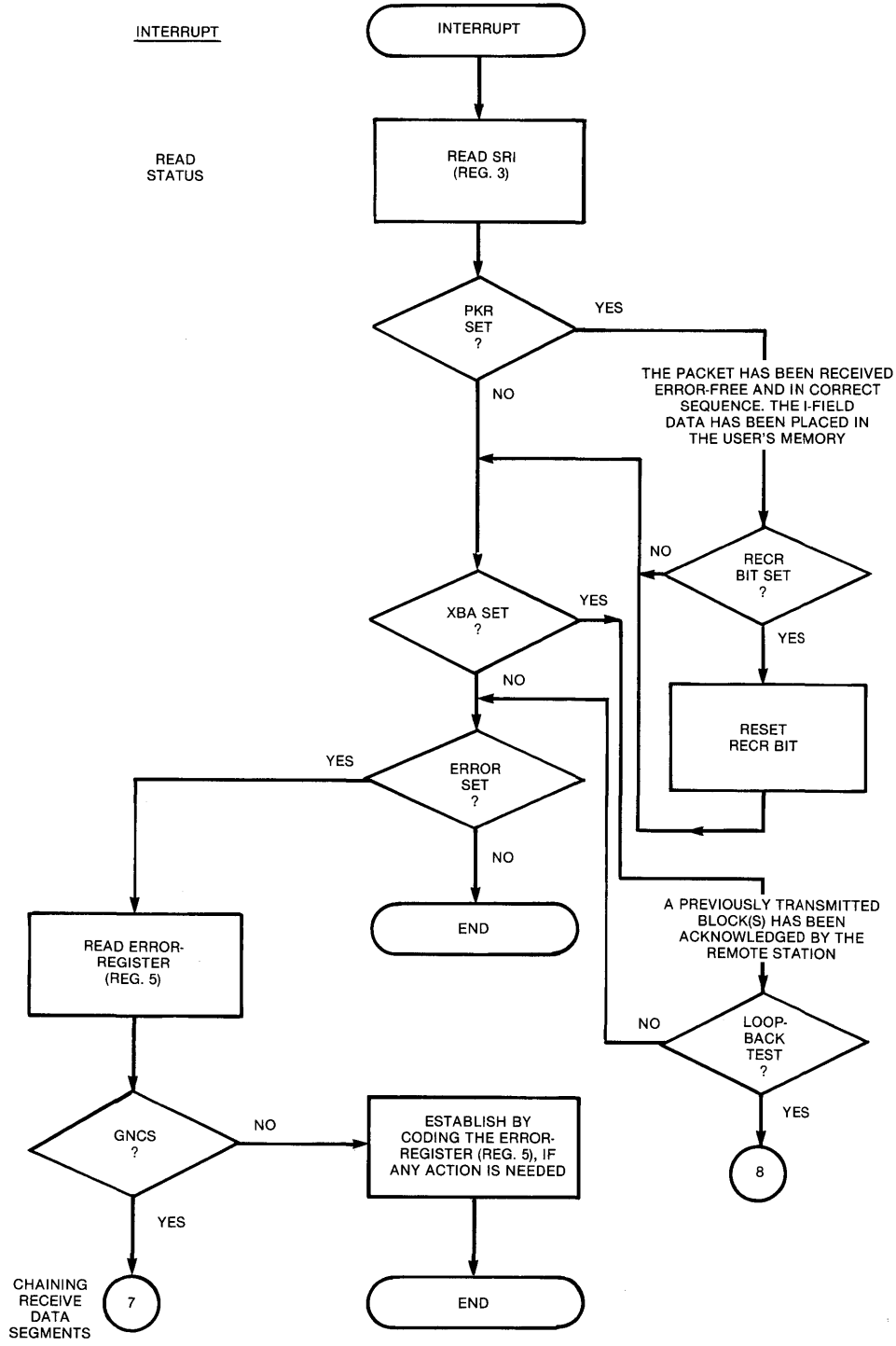


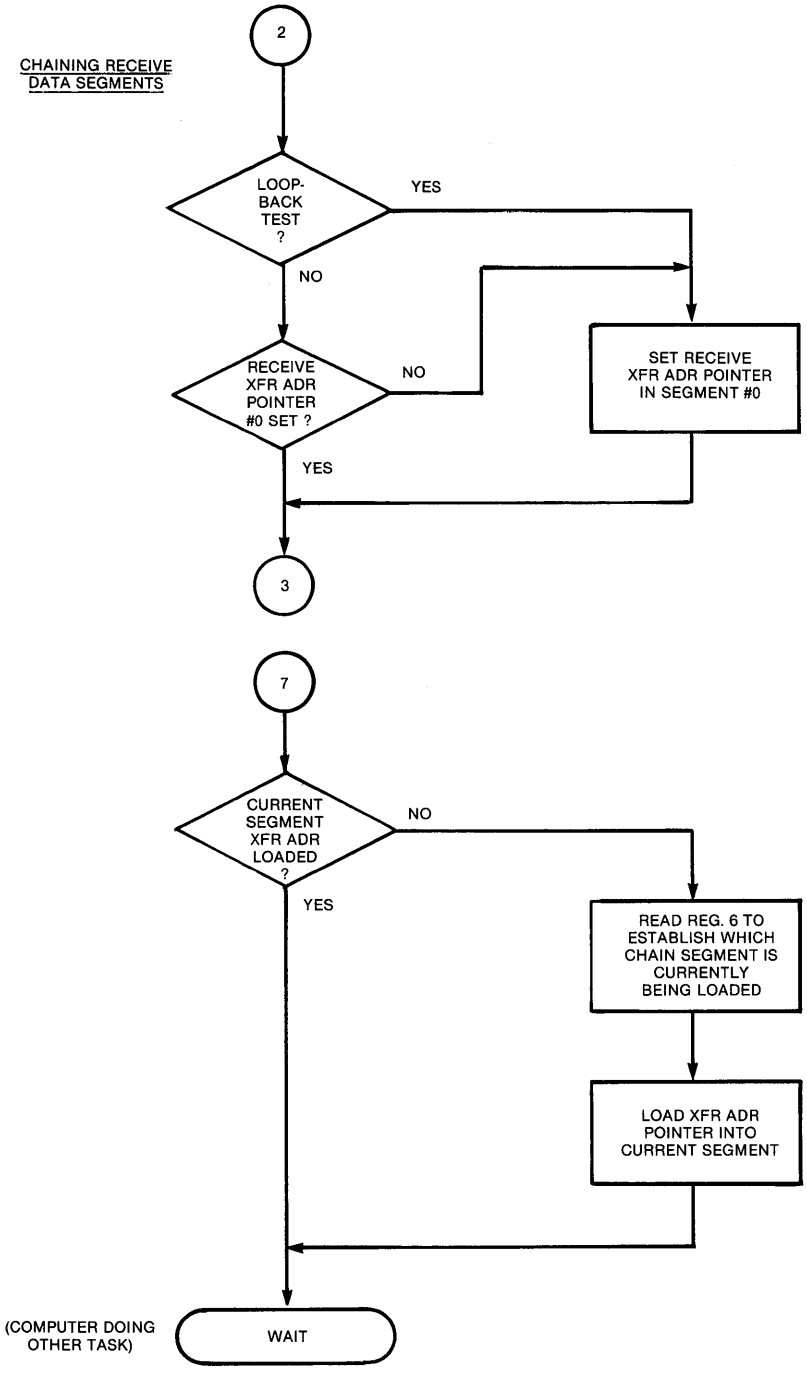
ENABLE RECEPTION
OF PACKET(S)

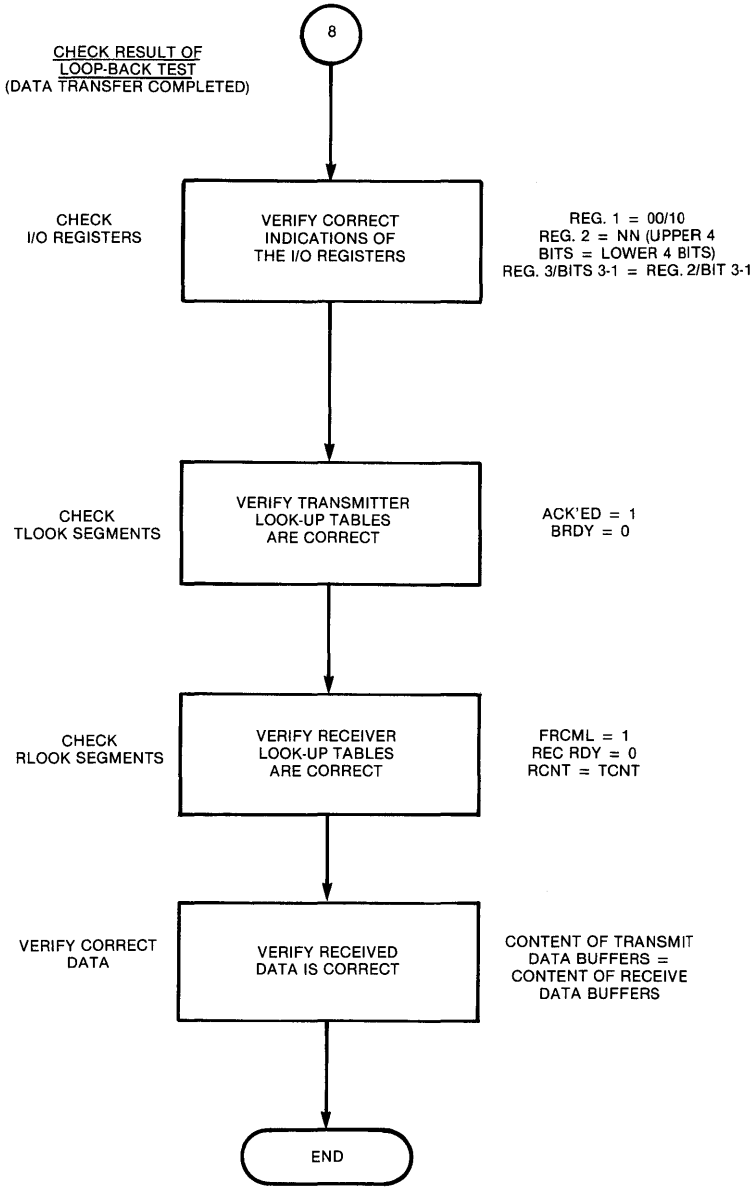



START
TRANSMITTING PACKET(S)
(DATA IS ALREADY LOCATED
IN THE TRANSMIT DATA
BUFFER(S))
4
LOAD DATA INTO
THE TRANSMIT
DATA BUFFERS
START3
5
YES
CHAINING
?
6
NO
TLOOK
PROGRAM THE
LOOK-UP TABLES
FOR THE TRANSMIT
DATA BUFFERS
BRDY, TSADR AND
TCNT
LOOP-
BACK
TEST
?
YES
NO
LINK UP?
LINK
= 0
?
SET CONTROL
BITS
SET SEND BIT
SET ACTIVE,
LOOP-TEST AND
RECR BIT
COMPUTER
DOING OTHER
TASKS
WAIT


CHAINING TRANSMIT DATA SEGMENTS
5
CHAIN
PROGRAM THE AMOUNT OF CHAIN SEGMENTS (REG. C, UPPER 4 BITS)
REG. C = YZ (HEX)
Y = NUMBER OF CHAIN SEGMENTS MINUS ONE
LIMIT
PROGRAM THE CHAIN-BUFFER SIZE (REG. C, LOWER 4 BITS)
REG. C = YZ (HEX)
BUFFER SIZE = Z.
64 x (1 + Z) BYTES
LOOP-BACK TEST ?
YES
NO
ALL TRANSMIT XFR ADR POINTERS SET ?
NO
YES
XFR ADR
SET ALL THE TRANSMIT XFR ADR POINTERS
6


INTERRUPT
INTERRUPT
READ STATUS
READ SRI (REG. 3)
PKR SET ?
YES
NO
THE PACKET HAS BEEN RECEIVED ERROR-FREE AND IN CORRECT SEQUENCE. THE I-FIELD DATA HAS BEEN PLACED IN THE USER'S MEMORY
RECR BIT SET ?
NO
YES
XBA SET ?
YES
NO
RESET RECR BIT
ERROR SET ?
YES
NO
END
A PREVIOUSLY TRANSMITTED BLOCK(S) HAS BEEN ACKNOWLEDGED BY THE REMOTE STATION
READ ERROR-REGISTER (REG. 5)
LOOP-BACK TEST ?
NO
YES
8
GNCS ?
NO
ESTABLISH BY CODING THE ERROR-REGISTER (REG. 5), IF ANY ACTION IS NEEDED
YES
CHAINING RECEIVE DATA SEGMENTS
7
END


CHAINING RECEIVE DATA SEGMENTS
2
LOOP-BACK TEST ?
YES
NO
RECEIVE XFR ADR POINTER #0 SET ?
NO
SET RECEIVE XFR ADR POINTER IN SEGMENT #0
YES
3
7
CURRENT SEGMENT XFR ADR LOADED ?
NO
YES
READ REG. 6 TO ESTABLISH WHICH CHAIN SEGMENT IS CURRENTLY BEING LOADED
LOAD XFR ADR POINTER INTO CURRENT SEGMENT
(COMPUTER DOING OTHER TASK)
WAIT


8
CHECK RESULT OF LOOP-BACK TEST (DATA TRANSFER COMPLETED)
CHECK I/O REGISTERS
VERIFY CORRECT INDICATIONS OF THE I/O REGISTERS
REG. 1 = 00/10
REG. 2 = NN (UPPER 4 BITS = LOWER 4 BITS)
REG. 3/BITS 3-1 = REG. 2/BIT 3-1
CHECK TLOOK SEGMENTS
VERIFY TRANSMITTER LOOK-UP TABLES ARE CORRECT
ACK'ED = 1
BRDY = 0
CHECK RLOOK SEGMENTS
VERIFY RECEIVER LOOK-UP TABLES ARE CORRECT
FRCML = 1
REC RDY = 0
RCNT = TCNT
VERIFY CORRECT DATA
VERIFY RECEIVED DATA IS CORRECT
CONTENT OF TRANSMIT DATA BUFFERS = CONTENT OF RECEIVE DATA BUFFERS
END

4.1 INTERNAL LOOP-BACK TEST (Example 1)

The loop-back test feature is an internal programmable loop-back of data, enabling the user to make an almost complete test of the WD2511. It allows diagnostic testing of the WD2511 and the interfacing circuitry. In this mode, transmitted data to the TD pin is internally routed to the received data input circuitry, thus allowing this WD2511 to set-up a link, send a number of packets to itself and then reset the link.

The $\overline{RC}$ clock is internally connected to $\overline{TC}$ clock. $\overline{CTS}$ input however, must be connected externally to GND or the $\overline{RTS}$ output.

The loop-back test allows the verifying of proper operation of practically all the various functions of the WD2511. The features tested here, the addresses and values of the variables chosen are only used as examples and are as follows:

TLOOK segments starting address = 0800H
Transmit Data buffer #0 starting address = 1000H
Received Data buffer #0 starting address = 1800H
Number of packets transferred = 1
Number of I-field bytes per packet = 1024
Number of residual bits = 0
T1 = 101H
N2 = 20H

Chaining is used in this example. The 1024 bytes are divided into 256 byte chain segments. Five segments are needed for this operation with 256 bytes of I-field data and two XFR ADR bytes per segment in the first four chain-segments. The rest of the I-field data (8 bytes) are located in the fifth chain-segment.

Programming:

CHAIN = 4 = number of CHAIN segments – 1
LIMIT = 3 = (number of bytes per segment divided by 64) – 1

For buffer management programming, see memory access scheme in Figure 7.

XMIT Command Address and XMIT Response Address (REG. E and F) must be the same value.

In some applications it is necessary to keep the $\overline{RTS}$ signal to the modem in the Off condition during internal loop-back test. Also, to accomplish the most complete test, $\overline{RTS}$ output should be connected to $\overline{CTS}$ input externally (not done internally). Figure 6 shows one example of how to implement these two functions. The ILOOP signal is connected directly to a PIO output.

In the loop-back test example shown in this section, the logic in Figure 6 is used and contains the Z80 CPU, programmable I/O (PIO) etc., as shown in Figure 3.

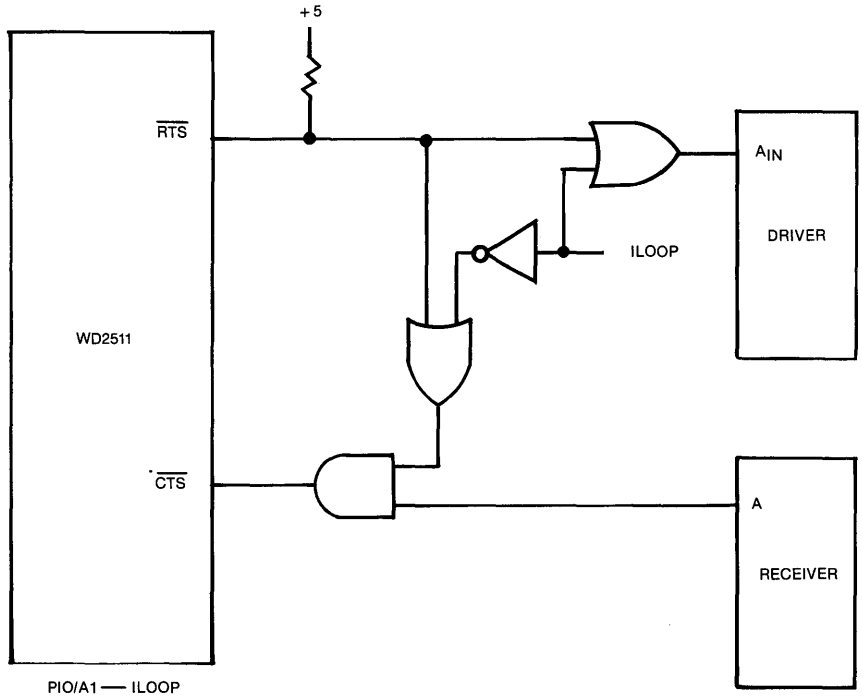


Figure 6. LOGIC FOR INTERNAL LOOP-BACK TEST

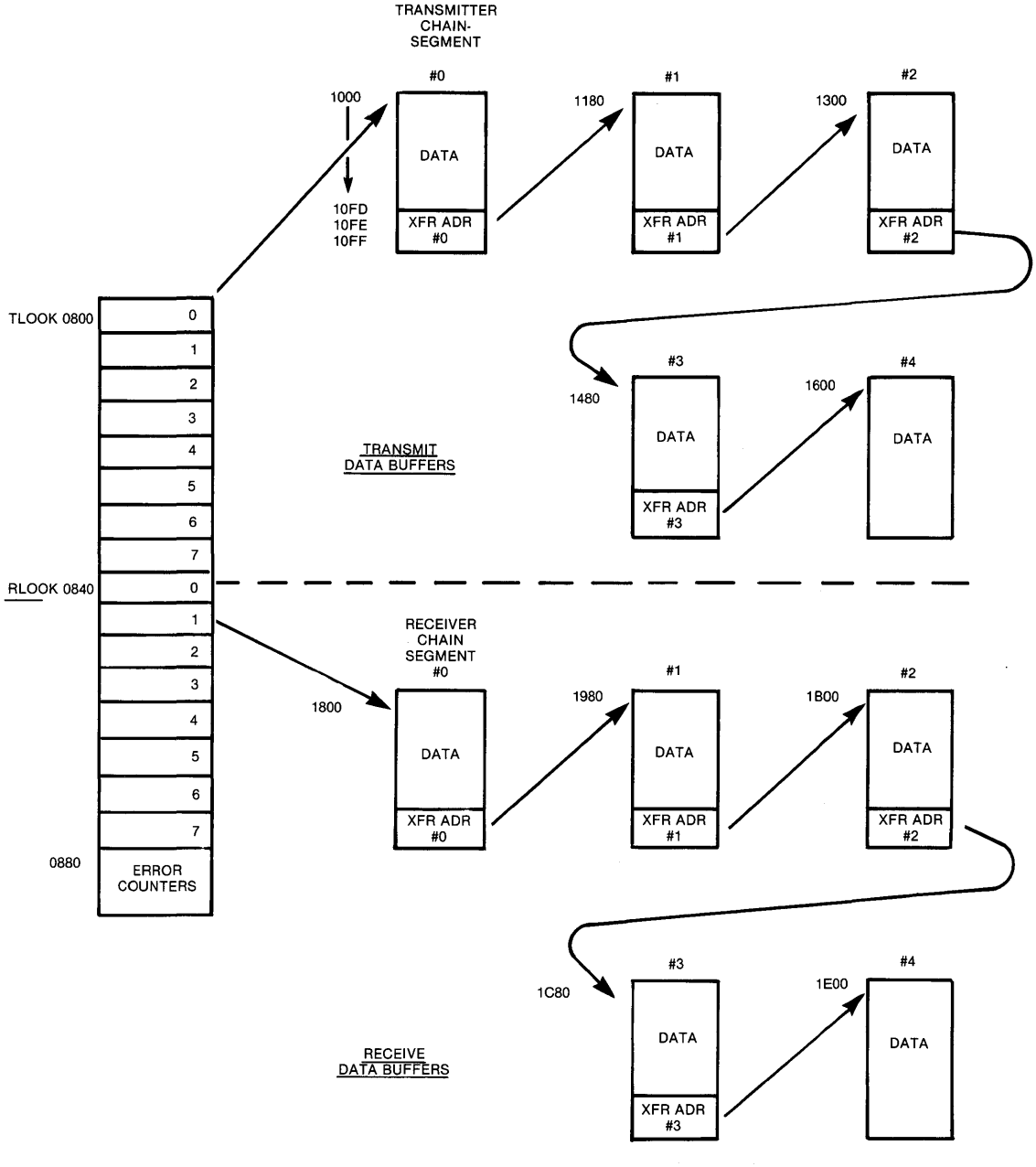


Figure 7. MEMORY ACCESS SCHEME FOR LOOP-BACK TEST (Example 1)

APPENDIX A
GLOSSARY OF DATA COMMUNICATIONS TERMS

The following is a list of industry-accepted data communications terms that are applicable to this specification.

ABM	Asynchronous Balanced Mode
ADCCP	Advanced Data Communications Control Procedure (ANSI BSR X3.66)
ANSI	American National Standards Institute
ARM	Asynchronous Response Mode
CCITT	International Consultative Committee for Telegraphy and Telephony
CMDR	Command Reject. A U-Frame
DCE	Data Circuit Termination Equipment (the network side of the DTE/DCE link)
DISC	Disconnect. A U-Frame
DTE	Data Terminal Equipment
DM	Disconnect Mode. A U-Frame (LAPB, only)
ECMA	European Computer Manufacturers Association
FCS	Frame Check Sequence
FDX	Full Duplex (also called "two way simultaneous")
FRAME	Basic serial block of bit-oriented data. Includes leading and trailing flags, address field, control field, FCS field, and an optional information field.
FRMR	Frame Reject. A U-Frame (LAPB, only)
HDLC	High-Level Data Link Control (ISO 3309)
HDX	Half Duplex (also called "two way alternate")
HOST	Another name for a DTE
I-Frame	Information Frame. Control field bit 0 is 0. In X.25 an I-frame is a packet.
ISO	International Standards Organization
LINK	The logical and physical connection between two data terminals
LAP	Link Access Procedure
LAPB	Link Access Procedure Balanced
N2	Maximum number of retransmissions of a frame. (Also called retransmission count variable.)
NODE	Another name for a DCE or DTE.
N(R)	Sequence number of next frame expected to be received.
N(S)	Sequence number of current frame being transmitted.
OCTET	An 8-bit byte
PACKET	An I-Frame in X.25
PAD	Packet Assembly/Disassembly facility
REJ*	Reject. An S-Frame
RNR*	Receiver Not Ready. An S-Frame
RR*	Receiver Ready. An S-Frame
S-Frame	Supervisory Frame. Control field bit 0 = 1 and bit 1 = 0
SARM	Set Asynchronous Response Mode. (LAP, only)
SABM	Set Asynchronous Balanced Mode. (LAPB, only)
SDLC	Synchronous Data Link Control (IBM document GA27-3093)
T1	A Primary Timer for a delay in waiting for a response to a frame
U-Frame	Unnumbered Frame. Control Field bit 0 = 1 and bit 1 = 1
UA	Unnumbered Acknowledge. A U-Frame
X.25	Recommendation by CCITT on Interfacing to Public Packet Switching Networks
X.3, X.28, X.29	Recommendations by CCITT involving PAD facilities

*There are also RR, RNR, and REJ packets which are not the same as the S-frame RR, RNR and REJ discussed in this document.

APPENDIX B

THE DIFFERENCE BETWEEN LAP AND LAPB

In March 1976, the CCITT adopted Recommendation X.25 as an interface standard for public packet-switching networks. The link level procedure adopted was called Link Access Procedure (LAP) and used the HDLC Asynchronous Response Mode (ARM). However, ARM was not designed for peer-to-peer communications so LAP had some subtle problems. Therefore, in 1977, when Provisional Recommendation X.25 was adopted, a procedure called LAPB was added. LAPB is Link Access Procedure-Balanced and operates under the HDLC Asynchronous Balanced Mode (ABM). Unfortunately, the 1977 LAPB lacked good symmetry between the DTE and DCE, and was unworkable.

In the April 1979 CCITT meeting, the LAPB was greatly enhanced, especially in the DTE/DCE symmetry. This enhanced version was approved in the February 1980 Plenary meeting of the CCITT. We now have a good, workable LAPB standard. LAPB is a superior procedure and the usage of LAP is being replaced with LAPB.

LAPB COMMANDS AND RESPONSES

			CONTROL FIELD				
FRAME TYPE	**COMMAND**	**RESPONSE**	**BIT #**				
			7 6 5	**4**	**3 2 1**	**0**	
I-FRAME	I-FRAME		N(R)	P	N(S)	0	
S-FRAME	RR	RR	N(R)	P/F	0 0 0	1	RECEIVER READY
	RNR	RNR	N(R)	P/F	0 1 0	1	RECEIVER NOT READY
	REJ	REJ	N(R)	P/F	1 0 0	1	REJECT
U-FRAME	SABM		0 0 1	P	1 1 1	1	SET ASYNCHRONOUS BALANCED MODE
	DISC		0 1 0	P	0 0 1	1	DISCONNECT
		DM	0 0 0	F	1 1 1	1	DISCONNECT MODE
		UA	0 1 1	F	0 0 1	1	UNNUMBERED ACKNOWLEDGE
		FRMR	1 0 0	F	0 1 1	1	FRAME REJECT

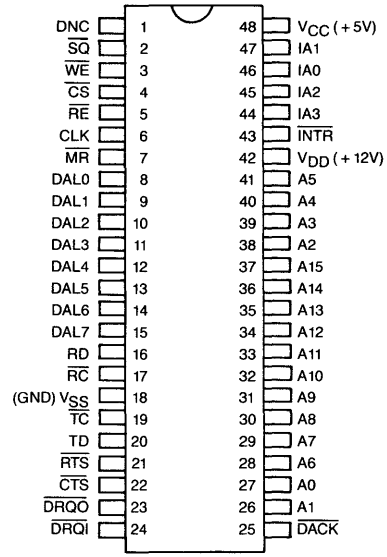
Only the FRMR and I-frame contain I-fields
P = Pole Bit F = Final Bit

PRELIMINARY

WD2840 Local Network Token Access Controller

FEATURES

- Broadcast Medium Independent (Coax, RF, CATV, IR, etc.)
- Up to 254 nodes
- Dual DMA/Highly efficient Memory Block Chaining
- Token based protocol
- Acknowledge option on each datagram
- Adjustable fairness, stations may be prioritized
- Frame format similar to industry standard HDLC
- Supports Global Addressing
- Diagnostic Support: Self-Tests, System and Network
- TTL Compatible



PIN DESIGNATION

DESCRIPTION

The WD2840 is a MOS/LSI device intended for local network applications, where reliable data communications over a shared medium is required. The device uses a buffer chaining scheme to allow efficient memory utilization. This scheme minimizes the host CPU time requirements for handling packets of data. The WD2840 frees the host CPU from extensive overhead by performing network initialization, addressing, coordination, data transmission, acknowledgements and diagnostics.

APPLICATIONS

The WD2840 is a general purpose Local Network Token Controller applicable to virtually all types of multi-point communications applications. The token protocol allows the sharing of one bus by up to 254 nodes. WD2840's will be designed into process control equipment, micro-computers, mini-computers, personal computers, proprietary micro-processor based applications, intelligent terminals, front-end processors, and similar equipment.

The great advantage for the design engineer is the ease with which he can implement a local network function. The WD2840 handles autonomously all major communications tasks as they relate to the local network function.

1.1 PIN DEFINITIONS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1	DNC	DO NOT CONNECT	Leave pin open.
2	$\overline{SQ}$	SIGNAL QUALITY	An active low input which signals the WD2840 that a frame may be received. The modem may negate this signal if its receive signal quality is below a reliability threshold, ensuring that the WD2840 will not accept the frame.
3	$\overline{WE}$	WRITE ENABLE	The data on the DAL are written into the selected register when $\overline{CS}$ and $\overline{WE}$ are low. $\overline{RE}$ and $\overline{WE}$ must not be low at the same time.
4	$\overline{CS}$	CHIP SELECT	Active low chip select for CPU control of I/O registers.
5	$\overline{RE}$	READ ENABLE	The content of the selected register is placed on DAL when $\overline{CS}$ and $\overline{RE}$ are low.
6	CLK	CLOCK	Clock input used for internal timing.
7	$\overline{MR}$	MASTER RESET	Initialize on active low. All registers reset to zero, except control bit ISOL is set to 1. DACK must be stable high before MR goes high. Status Register 0 is not defined at power-up (this register will be set-up upon entry into the Network mode).
8-15	DAL0-7	DATA ACCESS LINES	An 8-bit bi-directional three-state bus for CPU and DMA controlled data transfers.
16	RD	RECEIVE DATA	Receive serial data input.
17	$\overline{RC}$	RECEIVE CLOCK	This is a 1X clock input, and RD is sampled on the rising edge of $\overline{RC}$.
18	V_{SS}	GROUND	Ground.
19	$\overline{TC}$	TRANSMIT CLOCK	A 1X clock input. TD changes on the falling edge of $\overline{TC}$.
20	TD	TRANSMIT DATA	Transmitted serial data output.
21	$\overline{RTS}$	REQUEST-TO-SEND	An open collector output which goes low when the WD2840 is ready to transmit either data or flags.
22	$\overline{CTS}$	CLEAR-TO-SEND	An active low input which signals the WD2840 that transmission may begin.
23	$\overline{DRQO}$	DMA REQUEST OUT	An active low output signal to initiate CPU bus request so that the WD2840 can output onto the bus.
24	$\overline{DRQI}$	DMA REQUEST IN	An active low output signal to initiate CPU bus requests so that data may be input to the WD2840.
25	$\overline{DACK}$	DMA ACKNOWLEDGE	An active low input from the CPU in response to $\overline{DRQO}$ or $\overline{DRQI}$. $\overline{DACK}$ must not be low if $\overline{CS}$ and $\overline{RE}$ are low or if $\overline{CS}$ and $\overline{WE}$ are low.
26-41	A0-A15*	ADDRESS LINES OUT	Sixteen address outputs from the WD2840 for DMA operation.
42	V_{DD}	POWER SUPPLY	+12VDC power supply input.
43	$\overline{INTR}$	INTERRUPT REQUEST	An active low interrupt service request output. Returns high when Interrupt Register is read.
44-47	IA0-IA3*	ADDRESS LINES IN	Four address inputs to the WD2840 for CPU controlled read/write operations with registers in the WD2840. If ADRV = 0, these may be tied to A0-A3.
48	V_{CC}	POWER SUPPLY	+5VDC power supply input.

WD2840 LOCAL NETWORK TOKEN ACCESS CONTROLLER

INTRODUCTION

The WD2840 is a single LSI device which gives systems designers the ability to include networking capabilities into their unique products simply and economically.

A general and fundamental advantage to the use of complex LSI in a given system is the partitioning of required technical expertise. A successful user of the WD2840 need not be a data-communications expert, and further, he need not be at all concerned with low level network details (though these details are documented and available to him if he is interested). The potential user of the WD2840 must simply evaluate the communications facilities provided by the device to determine its suitability for the intended use.

The WD2840 is designed to logically interconnect 2 to 254 user devices over a shared communications medium. Examples of typical mediums include coax cable, twisted pair bus, RF, and CATV. All network control functions, such as data framing and error checking, destination filtering, fair and adjustable transmission scheduling, and network initialization and fault recovery (caused by noise for example) are handled completely by the WD2840.

The protocol implemented allows guaranteed station access intervals allowing applications in factory automation and other critical communications environments where "statistical delays" are not acceptable. The WD2840 token protocol also allows the addition and/or removal of stations to a network at anytime, including while operating.

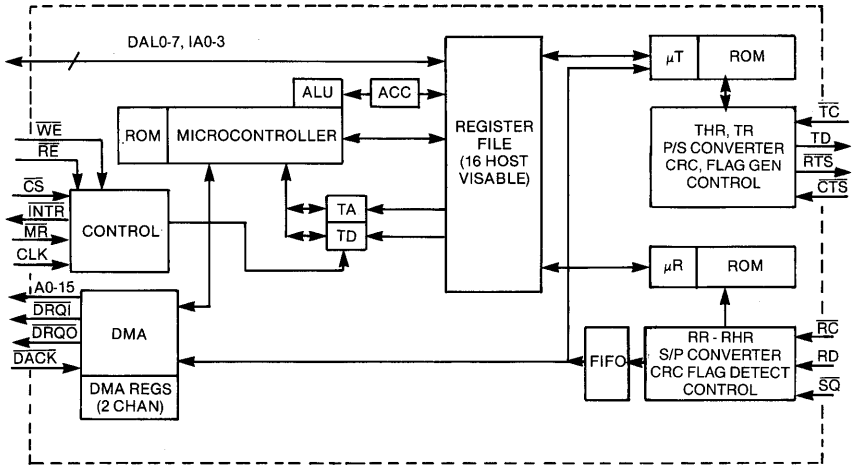


Figure 1.1 BLOCK DIAGRAM

Serious attention has also been given to the user's interface to the device. The interface is a combination of conventional I/O registers and an elaborate DMA buffer chaining interface. This chaining feature allows the user much more efficient use of his system memory, particularly in situations where the maximum message sent over the network is much longer than the average size. This feature also allows the automatic queueing of messages independently of the user's consumption rate, in effect, speed decoupling the user's CPU and processing requirements from the network.

The WD2840 has several parameters (registers) that allow tailoring to the user's requirements. In this way, network priority and access ordering, to name two, can be manually set if desired.

Using an integrated version of these network algorithms saves not only the development costs already mentioned, but further, the total processing power required for the user's application is not increased. In other words, a CPU upgrade can likely be avoided by "distributing" the network processing task into LSI devices such as the WD2840.

SCOPE

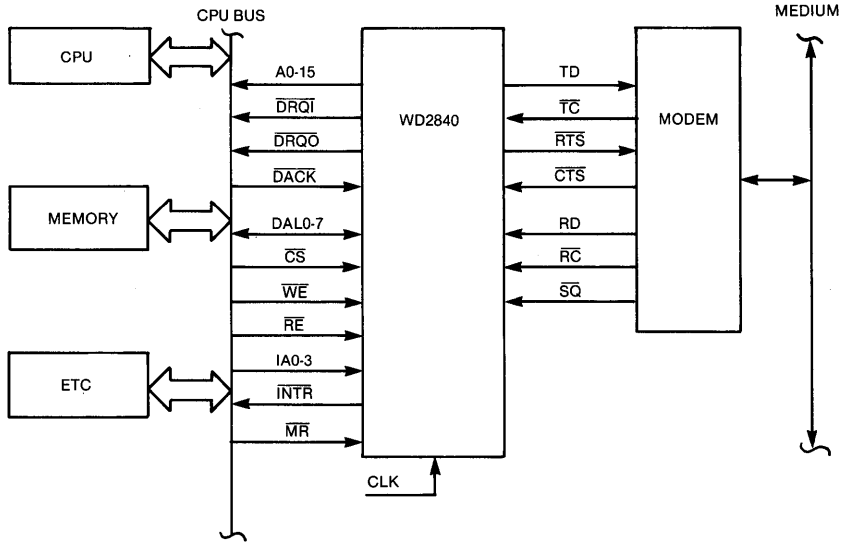
This document differs from traditional LSI data sheets in that it details not only the LSI implementation of a function, but also defines the overall function in detail. Specifically, this document includes details of the communications protocol implemented by the WD2840 Token Access Controller.

The document is organized into three main sections:

SECTION ONE is much like a traditional data sheet including register descriptions, pin definitions, and hardware architecture.

SECTION TWO describes the interfaces to the WD2840. The network side is conventional, the host side consists of an elaborate DMA interface with control blocks and WD2840/host handshaking.

SECTION THREE details the network protocol implemented by the device. Normal operation, initialization, and the handling of error conditions are described.



TYPICAL SYSTEM CONNECTION

1.2 DEVICE ARCHITECTURE

A detailed block diagram of the WD2840 is shown in Figure 1.1.

Mode control and monitor of status by the user's CPU is performed through the Read/Write Control circuit, which reads from or writes into registers addressed by IA0-IA3.

Transmit and receive data are accessed through DMA control. Serial data is generated and received by the bit-oriented controllers.

Internal control of the WD2840 is by means of three internal micro-controllers; one for transmit, one for receive, and one for overall control.

Parallel transmit data is entered into the Transmitter Holding Register (THR), and then presented to the Transmitter Register (TR) which converts the data to a serial bit stream. The Frame Check Sequence (FCS) is computed in the sixteen bit CRC register, and the results become the transmitted FCS.

Parallel receive data enters the Receiver Holding Register (RHR) from the 24 bit serial Receive Register (RR). The 24-bit length of RR prevents received FCS data from entering the RHR. The receiver CRC register is used to test the validity of the received FCS. A three level FIFO is included in the receiver.

The WD2840 sends all information, network control and user data, in blocks called frames. Each frame starts and ends with a single flag (binary pattern 01111110). In between flags, data transparency is provided by the insertion of a zero bit after all sequences of five contiguous one bits. The receiver will strip the inserted zero bits. (See section on frame format for location of address, control, and FCS fields.)

1.3 REGISTER DEFINITION

The WD2840 is controlled and monitored by sixteen 8 bit registers. This set of registers consists of two Control Registers, three Status Registers, an Interrupt Event Register, a Counter Register and a variety of Parameter Registers. In general the host is responsible for defining these registers (except certain host read-only registers: SR0-2, IR0, CTR0 and NA) to contain proper and meaningful values prior to entering Network Mode from Isolate State. Furthermore, while the WD2840 is in Network Mode, the CBP (H,L) and MA registers must not be changed by the host. Register NAR may be changed arbitrarily but will only be considered by the WD2840 in response to the NEWNA (CR10) control bit being set. The two Control Registers and the TA, TD, AHOLT, TXLT registers may change dynamically to control the behavior of the WD2840.

REG [1]	NAME	DESCRIPTION
0	CR0	Control Register 0
1	CR1	Control Register 1
2[2]	SR0	Status Register 0
3[2]	IR0	Interrupt Event Register
4[2]	SR1	Status Register 1
5[2]	SR2	Status Register 2
6[2]	CTR0	Counter Register 0
7[2]	NA	Next Address
8	TA	ACK Timer
9	TD	Net Dead Timer
A	CBPH	Control Block Pointer (MSB)
B	CBPL	Control Block Pointer (LSB)
C	NAR	Next Address, Request
D	AHOLT	Access Hold-off Limit
E	TXLT	Transmit Limit
F	MA	My Address

[1] = Hexadecimal representation of IA0-IA3.
[2] = CPU read only, write not possible.

Control, status, and interrupt bits will be referred to as CR, SR, or IR, respectively, along with two digits. For example, SR21 refers to status register #2 and bit 1, which is "STATE."

SUMMARY — CONTROL, STATUS, INTERRUPT REGISTERS

REGISTER	BIT # 7	6	5	4	3	2	1	0
CR0	TXDEN	TXEN	RXEN	ITOKON	ILOOP	COPY	NOINT	ISOL [1]
CR1[2] CR1[4]	DIAGC DIAGC	PIGT 0	INIT 0	ADRV ADRV	GIRING DMAT	0 LOOPT	TOFF RAMT	NEWNA NUDIAG
SR0	LASTF	SENDACK	L2	0	BSZ3 ...	BSZ2 ...	BSZ1 ...	BSZ0
IR0 [3]	ITERR	IROR	INS	ITRAN	IREC	ITOK	ITA	ITD/M
SR1	TAOUT	$\overline{\text{IRTS}}$	RECIDL	1	1	1	1	1
SR2	NXTT0	NXTR0	TR	ACKRQ	RETRY	TSENT	STATE	INRING
NOTE: ZERO BITS (0) SHOWN ABOVE ARE RESERVED AND SHOULD NOT BE USED.								

NOTES:

[1] = Set to 1 on power-up or master reset.

[2] = Non diagnostic mode only (CR17-DIAGC cleared).

[3] = Any bit set causes host interrupt ($\overline{\text{INTR}}$ goes true) when Master Interrupt Suppress (CR01) is clear. All bits are cleared when register is read by the host.

[4] = Diagnostic State only (CR17-DIAGC set). See diagnostic section for register usage in diagnostic mode.

CR0 — CONTROL REGISTER 0 DEFINITION

REGISTER	CR07	CR06	CR05	CR04	CR03	CR02	CR01	CR00
CR0	TXDEN	TXEN	RXEN	ITOKON	ILOOP	COPY	NOINT	ISOL

BIT	NAME	DESCRIPTION
CR00	ISOL	Isolate. Set true on power up or master reset. Host clears this bit after the host memory based WD2840 control block and other WD2840 registers have been set up. May be set by the host at any time (will be ignored if WD2840 is in diagnostic state). There is some delay for the WD2840 to respond to any state change request. A state change to network mode is acknowledged by the state confirmation status bit (SR21-STATE) being cleared. Setting ISOL while the WD2840 is in Network State will cause a state change to Isolate State, confirmed by an interrupt event (IR00-ITM) and the STATE status bit (SR21) being set. This transaction will be delayed until the node does not possess the token. Any in-progress frame transmission will be completed normally (at the current frame, regardless of queue length), followed by a normal token pass sequence.
CR01	NOINT	Master Interrupt Suppress. When clear, the WD2840 will generate host interrupt requests ($\overline{\text{INTR}}$ low) if any bit in the WD2840 interrupt request register (IR0) is set. When set, only the interrupt request is suppressed, not the setting of bits in IR0. Note that any interrupt request will be dropped by the WD2840 when IR0 is read since this will clear IR0.
CR02	COPY	Enables COPY mode. When set causes all received data frames to be accepted and DMA'ed into memory regardless of destination address. (See description in Diagnostics Section.)
CR03	ILOOP	Instructs the WD2840 to loop data internally from transmitter to receiver. Used with the LOOP diagnostic. Must NOT be set while in network mode (CR00-ISOL clear).
CR04	ITOKON	Enable Token received interrupts. When clear no Token received interrupts are generated. When set the WD2840 generates an Itok interrupt when a token is received.

BIT	NAME	DESCRIPTION
CR05	RXEN	Receive Data Enable. When clear, the WD2840 still makes normal responses to supervisory frames (scan, token pass), but will not DMA any data frames into memory and ignores the receiver buffer chain. However any data frame which is addressed to this node and for which an ACK is requested, will be NAK'ed with a "receiver not enable" Nak code. When RXEN is set, it allows the receiver to DMA appropriate data frames into memory. RXEN may be arbitrarily set and reset while in Network State but changes will not affect any frames in progress. NOTE: Even when RXEN is clear, the WD2840 is "following" the receiver buffer chain with an internal register pointing either to the next available buffer (NXTR0 set) or, if the chain is exhausted, to a link field of zero (NXTR0 clear). The constraints on host manipulation of the receiver buffer chain are the same regardless of the state of RXEN. See the subsequent section on Receiver Memory Interface for more details.
CR06	TXEN	Master Transmit Enable. When clear no transmissions will occur and the transmit buffer chain will be ignored. When set, transmission activity is further dependent upon TXDEN (CR07). NOTE: Even when TXEN is clear, the WD2840 is "following" the transmitter buffer chain with an internal register pointing either to the next frame to transmit (NXTT0 set) or, if the chain is exhausted, to a link field of zero (NXTT0 clear). The constraints on host manipulation of the transmitter buffer chain are the same regardless of the state of TXEN. See the subsequent section on Transmitter Memory Interface for more details.
CR07	TXDEN	Data Transmit Enable. Has no meaning unless TXEN is set. When set in conjunction with TXEN, normal WD2840 transmission of data and supervisory frames will occur. When clear and with TXEN set, only data frame transmission will be suppressed. That is, token pass and Ack/Nak supervisory frames will still be transmitted when appropriate. NOTE: The note above for TXEN applies.

CR1 — CONTROL REGISTER 1 DEFINITION

REGISTER	CR17	CR16	CR15	CR14	CR13	CR12	CR11	CR10
CR1	DIAGC	PIGT	INIT	ADRV	GIRING	0	TOFF	NEWNA
CR1	DIAGC	0	0	ADRV	DMAT	LOOPT	RAMT	NUDIAG

BIT	NAME	DESCRIPTION (CR17 = 0, Network mode)
CR10	NEWNA	Update NA register. When set causes WD2840 to copy the contents of register NAR into register NA. The WD2840 clears this bit after the function is complete. This mechanism allows the host to define the WD2840's successor in the logical ring. The node's next token pass will be to the new NA node. NOTE: The normal token pass recovery applies. If the token pass to the new NA is not successful, a normal scan sequence will occur where the WD2840 attempts a single token pass to each node address in numerical sequence until a successful pass occurs or the node's address itself is reached.
CR11	TOFF	When set causes WD2840 to ignore timers. (This is NOT intended to be used in an operational network, but is provided to support network diagnosis.) CAUTION: This control bit disables all automatic network error recovery.
CR12	—	(Not used, Reserved.)
CR13	GIRING	Get in logical ring. Instructs the WD2840 to gain entry into the logical ring at the next opportunity (i.e. respond to a token pass). The INRING status bit (SR20) is confirmation; when INRING is set, it indicates that the WD2840 is participating in a logical ring of at least two nodes. If the host clears GIRING while INRING is set, the WD2840 will not accept the next token pass to it at which time INRING will be cleared as confirmation.

BIT	NAME	DESCRIPTION (CR17 = 0, Network mode)
CR14	ADRV	Address Driver Enable. Enables the sixteen output address (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{DACK}$ goes low. If ADRV = 1, the outputs are always TTL levels.
CR15	INIT	Network Initialization Enable. When clear, the WD2840 will not attempt to (re)initialize the network if the net dead timer (TD) expires. When set, TD timer expiration causes the WD2840 to enter Scan Mode. In this mode it transmits a token pass frame to each node numerically higher in address, one after another, until either network activity occurs (another node responds) or until the node's own address is reached. When Scan Mode begins, the first node address used is the then current NA (Next Address) node address. This value is derived from and is affected by the following actions: 1. At transition into Network State it defaults to MA + 1. 2. It may be set by the host using the NAR register and the NEWNA (CR10) control flag. 3. Upon receipt of a Scan Mode frame, NA is redefined to MA + 1. The successful initialization of the network by Scan Mode causes NA to be defined as the first responding node (hence, this node's successor). All node address computations are ascending and circular within the valid node address range of 1-254. NOTE: Since this network initialization activity comes about because of a timer expiration, TOFF (CR11) must be clear.
CR16	PIGT	If set, instructs WD2840 to piggy back token on last data frame transmitted. This request is honored if the last frame is determined as a result of limit TXLT or the LAST bit set in the TX-FCB, but not if transmission ends due to the reaching of the end of the chain.
CR17	DIAGC	Enables diagnostic mode. In network mode this bit must be zero.

CR1 — CONTROL REGISTER 1 DEFINITIONS

BIT	NAME	DESCRIPTION (CR17 = 1, Diagnostic mode)
CR10	NUDIAG	Perform a new diagnostic. When set causes WD2840 to perform the selected diagnostics. The host initializes the appropriate registers for the particular diagnostic and by setting this bit can initiate the test. The WD2840 clears this bit after completion of the diagnostic.
CR11	RAMT	Selects internal RAM test if in diagnostic mode.
CR12	LOOPT	Selects Loop Test if in diagnostic mode.
CR13	DMAT	Selects DMA Test if in diagnostic mode.
CR14	ADRV	Address Driver Enable. Enables the sixteen output address (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{DACK}$ goes low. If ADRV = 1, the outputs are always TTL levels.
CR15	—	(Not used, Reserved.)
CR16	—	(Not used, Reserved.)
CR17	DIAGC	Enables diagnostic mode. Confirmation of diagnostic mode is via status bit STATE (SR21). When DIAGC and STATE are both set, diagnostic functions of CR1 apply. When DIAGC is cleared, after the selected set of diagnostics in progress complete, the WD2840 will transition to the Isolate state. This transition will cause an interrupt event (ITM).

SR0 — STATUS REGISTER 0 DEFINITION

REGISTER	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
SR0	LASTF	SENDACK	L2	0	BSZ3	BSZ2	BSZ1	BSZ0

BIT	NAME	DESCRIPTION
SR00 .. .. SR03	BSIZ	BSIZ0 — BSIZ3 Buffer size, defines the buffer size in multiples of 64 bytes (the value ranges from 0 to 15_H. Corresponding to a buffer size of 64 to 1024 bytes in 64 byte increments). This value is used internally to define buffer boundaries to allow the chip to link buffers. A maximum of 16 buffers may be used for a single frame.
SR04	—	Not used.
SR05	L2	An internal flag set during frame transmission if the length value of the current frame is equal to eight. For normal data frame transmission this means the frame has no data field and for transparent frame transmission this means the frame is an access control frame. (SCAN FRAME)
SR06	SENDACK	An internal flag set during data frame reception to indicate that the incoming frame should be acknowledged (send ack/nak frame). This flag is cleared when the acknowledgement has been transmitted.
SR07	LASTF	An internal flag set during data frame transmission to indicate that the current frame will be the last to be transmitted with this token. Five situations can cause this to occur: 1) ISOL (CR00) becoming set, 2) TXDEN (CR07) becomes clear, 3) current frame flagged (via FCB) to be "last frame," 4) the current token frame count reaching the TXLT limit, 5) transmitter under-run detection. Note in particular that the last frame in the transmit queue will not cause LASTF to set since it's being last is not known until frame end. Also if a piggy-back token is permitted (CR16 set) and no acknowledge is requested (via FCXB), the token will be piggybacked on the current (last) data frame. LASTF is not cleared until the next data frame transmission begins.

IR0 — INTERRUPT REGISTER DEFINITION

REGISTER	IR07	IR06	IR05	IR04	IR03	IR02	IR01	IR00
IR0	ITERR	IROR	INS	ITRAN	IREC	ITOK	ITA	ITD/M

The setting of any bit in this register by the WD2840 causes an interrupt request ($\overline{INTR}$ = low) if NOINT (CR01) is clear. The reading of this register by the host clears all bits (and any interrupt request).

BIT	NAME	DESCRIPTION (1)
IR00	ITD/M	Network dead or mode change (dual use). When in Network mode, timer TD expiring (with TOFF clear) causes this bit to be set to indicate no network activity has occurred within the timeout period. Also INRING (SR20) is cleared and, if INIT (CR15) is set, the WD2840 will enter Scan Mode (see INIT - CR15 for details). Transition from Network or Diagnostic State to the Isolate State will be confirmed by this interrupt. The choice between the ITD and ITM interpretations is easily made based on the ISOL (CR00) bit.
IR01	ITA	Date Frame Transmission Unsuccessful. This interrupt indicates that a transmitted data frame with an acknowledge request was not successfully acknowledged. Either a NAK or no response after two transmissions will cause this. The exact cause can be determined by inspecting the appropriate FSB.
IR02	ITOK	The token has been received.

BIT	NAME	DESCRIPTION (1)
IR03	IREC	Data Frame Received. This interrupt signifies that a good data frame has been properly received and DMA'ed into the buffer chain. Frames that have been received can be identified by following the buffer chain noting the WD2840 frame status bytes (FSB). A non-zero FSB (host must clear when queuing free buffers) indicates a properly received frame. The host may freely remove all received frames from the chain up to but NOT necessarily including the last one posted. The last one posted may only be removed if the WD2840 NXTR0 (SR26) is set. For more details see the explanation for NXTR0.
IR04	ITRAN	Indicates that at least one data frame has been transmitted. The number of frames transmitted and the status of each (i.e. ACK/NAK, retry count) is determined by following the transmit chain and inspecting frame status bytes (FSB). All transmitted frames up to but NOT including the last posted may be freely removed. The last one posted may only be removed if the WD2840 NXTT0 (SR27) is set. For more details see the explanation for NXTT0.
IR05	INS	New successor. The WD2840 has identified a new successor in the logical ring. This happens when the prior successor either failed to respond to a token pass or as instigated by a network scan frame.
IR06	IROR	Receiver over-run. The WD2840 ran out of buffers or access to the DMA channel was delayed by the host so long as to cause loss of received data.
IR07	ITERR	Transmitter error. Three abnormal frame transmission cases can cause the ITERR interrupt. The causes are "transmitter underrun," "premature end of chain," and "exceeded 16 buffers." The frame transmission will repeat once per token until the host removes the WD2840 from the network, or the cause of the error is fixed.

(1) = Non diagnostic mode only. See diagnostic section for register usage for diagnostics.

SR1 — STATUS REGISTER 1 DEFINITION

REGISTER	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR00
SR1	TAOUT	$\overline{\text{IRTS}}$	RECIDL	1	1	1	1	1

BIT	NAME	DESCRIPTION
SR10 :: SR14	—	(Not used, reserved.)
SR15	RECIDL	Receiver Idle. Indicates the WD2840 has received at least 15 contiguous ones.
SR16	$\overline{\text{IRTS}}$	Internal Request To Send. Indicates the transmitter is attempting (successful or not) to send either data or flags. If the $\overline{\text{RTS}}$ pin is not tied to ground or WIRE-OR'ED with another signal, then $\overline{\text{IRTS}}$ = $\overline{\text{RTS}}$.
SR17	TAOUT	Timer TA expired.

SR2 — STATUS REGISTER 2 DEFINITION

REGISTER	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20
SR2	NXTTO	NXTRO	TR	ACKRQ	RETRY	TSENT	STATE	INRING

BIT	NAME	DESCRIPTION
SR20	INRING	In logical ring. Indicates the node has had the token and has successfully passed it at least once (therefore it is included in a logical ring of at least two nodes). See GIRING (CR13) for other comments.
SR21	STATE	Mode confirmation. Depending on DIAGC (CR17), the WD2840 is either in Isolate or Diagnostic state. When ISOL (CR00) is set, STATE set confirms the WD2840 is not in Network State. When ISOL is clear, STATE clear confirms Network State. Note any state transition into Isolate State causes an interrupt event to occur (ITM).
SR22	TSENT	An internal flag. TSENT is set when the WD2840 passes the token. It may have been either a piggyback or explicit token pass frame. TSENT is cleared when the next frame is received.
SR23	RETRY	An internal flag which is set when either a data frame or a token pass frame must be retransmitted. Data frames are only retransmitted if they have an acknowledge request and no response at all occurred. Token pass frames (except Scan) are retransmitted if no network activity was detected. Both of these situations are detected as a result of a TA timeout.
SR24	ACKRQ	An internal flag set during data frame transmission if an acknowledgement is requested for the specific frame. If this is the case, the WD2840 pauses to await the ACK/NAK response frame; if the TA timer expires before the response, a single retry will occur (see RETRY-SR23). ACKRQ is not cleared until the beginning of the next data frame transmission.
SR25	TR	An internal flag set when the WD2840 receives a token passed to it. It is cleared when the token is passed (or if it is ignored for any reason. For example, piggyback token on a bad data frame, TXEN clear, or detection of duplicate tokens in the logical ring).
SR26	NXTR0	Internal Receive Buffer Pointer State. Because of the linked list approach used in the buffer chains, the WD2840 internal register used to follow the list is either pointing to the next buffer in the chain or at the address of the next buffer in the chain (prior buffer's link field). The WD2840 will always advance along the chain so that it has the address of the next buffer to be used. However, when a zero link is encountered, the WD2840 retains the link field address expecting eventually that the chain will be extended by the host making the link some non-zero value. When the WD2840 actually needs the next buffer, it looks again at the contents of the link field expecting it to have been changed (chain extended) to the address of an available buffer. The NXTR0 bit differentiates between these two situations. When set it indicates the WD2840 has the address of the next buffer and that all prior frames (denoted by posted FSB's) can be removed from the chain for received frame processing by the host. When NXTR0 is clear it indicates that the WD2840 has advanced to a zero link (end of chain). NOTE: In this situation, the last posted frame CANNOT be removed from the chain for processing since it is the link field of his last buffer that must be set in order to extend the receiver buffer chain.
SR27	NXTT0	Internal Transmit Buffer Pointer State. The comments for NXTR0 (SR26) apply (in an analogous manner) to NXTT0 since the transmit buffer chain is handled by the WD2840 using an identical scheme. When NXTT0 is set it indicates that the WD2840 has the address of the next frame to transmit in its internal register. However when clear, it indicates that the transmit chain internal register points to the link field of the last buffer of the last transmitted frame. This link field contained zero when first read. For the transmit case, this is a normal situation corresponding to no data frames to transmit. NOTE: As in the receive case, when NXTT0 is set, all previously transmitted frames (denoted by posted FSB's) can be removed from the chain for reuse. However, when NXTT0 is clear it indicates that the transmit chain must be extended by the host before removing the very last frame that has been transmitted (posted).

OTHER REGISTER DEFINITIONS

NAME	DESCRIPTION
CTR0	Running Limit Counter. Used by the WD2840 for Access Hold-Off Limit (AHOLT) checking and Transmit Limit (TXLT) checking. When transmitting data frames CTR0 is used for TXLT counting; otherwise it is used for AHOLT counting. The counter runs from zero to the 8-bit limit value.
NA	Next Address. This register shows the current (instantaneous) successor node in the network logical ring. For validity, the WD2840 should be "in the ring" (see GIRING - CR13 and INRING - SR20 for more details). The successor node may be changed for a variety of reasons: 1. Any attempted token pass that fails twice will cause the WD2840 to attempt to locate a new successor by sequentially trying token passes to successively higher node addresses beginning with NA + 1. 2. A received Scan frame will cause NA to be set to MA[$] 1. If the next token pass fails case 1 applies. 3. The host may arbitrarily redefine NA by using the NAR register and the NEWNA (CR10) control bit. At a convenient point the WD2840 recognizes NEWNA, copies NAR into NA, then clears NEWNA as confirmation. If the next token pass fails case 1 applies.
TA	Acknowledgement Timer. Value of maximum allowed time between frame transmission and ACK/NAK (if requested), or between token sent and network activity. The delay is in increments of 64 times the period of the clock CLK. Thus, if CLK = 2 MHz, then TA may be set in increments of 32 microseconds (range of 32 μs to 8.2 ms).
TD	Network Dead Timer. Value of maximum time interval between received valid frames on the network. 32X range of TA.
CBP (H,L)	Control Block Pointer. A sixteen bit pointer to the WD2840 control block in the user's memory. Must not be modified while the WD2840 is in network mode.
NAR	Next Address, Request. Used in conjunction with the NEWNA (CR10) control bit to cause the WD2840 to update the NA register. This redefines the node's successor in the network logical ring. It MUST be an address in the range 1-254. The acceptance of this update is confirmed when the NEWNA control bit is cleared. On the next token pass, if the redefined successor fails to accept the token, this WD2840 enters Scan mode where it sequentially attempts a token pass to successively higher nodes.
AHOLT	Access Hold-off Limit. This register is set at a value indicating the number of access cycles (tokens received) that must be skipped before the data frame may be transmitted. (A token pass frame will be sent even if a data frame may not be sent at a given access cycle.) Initialized to zero at power up.
TXLT	Transmit Limit. This register is set at the maximum number of consecutive data frames the WD2840 may transmit during one access cycle. A value of zero allows the WD2840 to transmit all frames queued up to 256. Initialized to zero at power up.
MA	My Address. The WD2840 receives only frames with this destination address (along with the broadcast address) and inserts this address into the SA field of any transmitted frame. Must be set by the host (range is 1 to 254).

1.4 DIAGNOSTIC AIDS

There are three levels of diagnostics supported by the WD2840; those that are associated with the network as a whole, those associated with the individual node, and those that are limited to the WD2840 as a device. These tests are Network Diagnostics, System Diagnostics and Self Diagnostics respectively. The Network Diagnostics can be performed while the WD2840 is in the logical ring, but the System Diagnostics and the Self Diagnostics may be used only while the WD2840 is in the diagnostic mode.

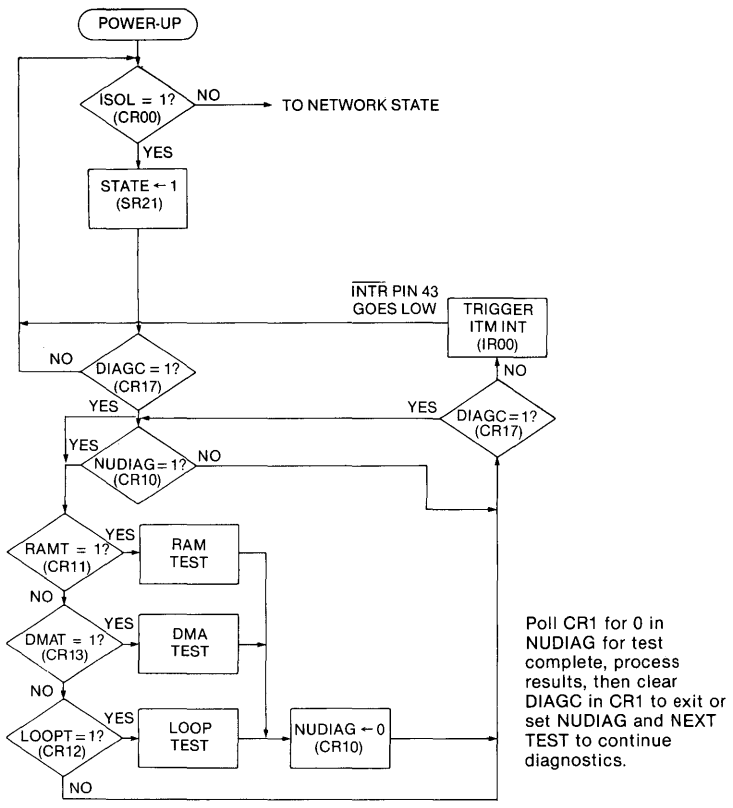
DIAGNOSTIC MODE CONTROL			
CR00 ISOL	CR17 DIAGC	SR21 STATE	DEFINITION
1	0	0	WD2840 "Isolated." Power-up condition or isolate request.
0	0	0	WD2840 active.
1	0	1	Isolate request function confirmed.
1	1	0	Host request to enter diagnostic mode.
1	1	1	Diagnostic mode confirmed. Diagnostic functions of CR1 apply.
0	0	1	Illegal.
0	1	0	Illegal.
0	1	1	Illegal.

Diagnostic mode may be entered after power-up or from the network mode by manipulation of the mode control bits. The mode transition is confirmed by the WD2840 via the STATE status bit.

Once in diagnostic mode, the desired test is selected via CR1. Because most of registers 8 through F are interpreted differently for each test, only one of the diagnostic test bits should be set at a time. In conjunction with setting the diagnostic bits, the NUDIAG (CR10) bit must be set to perform the diagnostic test requested.

At the completion of the selected test NUDIAG is cleared by the WD2840. Therefore the host can initiate a diagnostic by entering the diagnostic mode, initializing the proper registers, setting the desired diagnostic bit, and setting NUDIAG. The host then moniters CR1 for NUDIAG going to zero, indicating the completion of the requested diagnostic.

DIAGNOSTIC STATE FLOW CHART



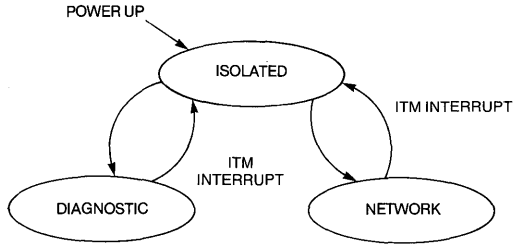


Figure 1.3 FUNCTIONAL STATES

1.4.1 SELF DIAGNOSTICS

Internal Ram and Interrupt Test

There are nine eight bit registers in the WD2840 which are not directly accessable by the users CPU. This test provides a means to check those registers and the interrupt register. The contents of register A are placed into the interrupt register and five even internal registers, and the contents of register B in four odd internal registers. The nine registers are then added together without carry and the result is placed in registers 2, 5, 6, 7.

Use the following procedure to initiate the RAM test:

1. Enter diagnostic mode.
2. Set up registers A and B
3. Set RAMT.
4. Set NUDIAG (can be set with RAMT bit together).
5. Wait for NUDIAG to be cleared.
6. Read registers 2, 5, 6, 7. Clear RAMT.

Note that the setting of any bit in the interrupt register while NOINT is clear will generate a hardware interrupt ($\overline{INTR}$, pin 43 goes true).

1.4.2 SYSTEM DIAGNOSTICS

DMA Test

This test verifies proper operation of the DMA subsystem by reading the value from a register and writing it into the user memory. The test continues by reading the value from the same location in memory and writing it into another register.

The value is read from register C. Using the transmitter DMA sub-system, it is written into memory location addressed by register A and B (location N; register A is the MSB). The receiver DMA sub-system is used and contents of the same address is read and it is stored into the register 7. Next the receiver dma is used and the contents from register D is written into location N + 1. The transmitter dma reads the value from location N + 1 and stores it into register 6.

It is the host's responsibility to check if the contents of registers C and register 7 and memory location N match. The same is true for registers D and 6 and memory location N + 1.

Loop-Back Test

The host can test the WD2840 transmitter and receiver logic by using the Loop Test.

There are two Loop Tests available for diagnostic purposes — internal and external.

(CR12) LOOPT	(CR03) 1LOOP	DEFINITION
0	0	Not in Loop Test
0	1	Do not use in network mode
1	0	External loop
1	1	Internal loop

When using the external loop the interface or modem must have the necessary logic to tie TD to RD and $\overline{TC}$ to $\overline{RC}$.

Use the following procedure to run the loop test.

1. Set up a 256 byte transmit buffer with the data pattern to be transmitted.
2. Initialize a 256 byte receive buffer with all "00s" or "FFs."
3. Load register A (MSB) and B (LSB) with the address of the transmit buffer.
4. Load register C (MSB) and D (LSB) with the address of the receive buffer.
5. Load register 0 for Internal or External Loop.
6. Load register 1 for diagnostic & loop. (85_H)
7. Refer to Diagnostic State Flow Chart.

NOTE:
If this test frame is allowed onto the network, transmission collisions may occur. Further, the first three bytes of the transmit buffers will be interpreted as TC, DA and SA, respectively, by the other stations. Therefore in case this test is initiated while this node is in the logical ring, care should be taken for choosing these three values for external loop-back test.

For proper operation of the internal loop-back test the $\overline{CTS}$ and $\overline{SQ}$ pins of the WD2840 should be either tied to ground or tied to $\overline{RTS}$ pin of the WD2840.

1.4.3 NETWORK DIAGNOSTICS

Duplicate Station Detection

Duplicate stations (more than one station with the same address) can result from the faulty programming of internal register MA (due to wrong address switch settings on the user's device, for example). This is expected to occur often enough to warrant the addition of a detection algorithm in the users WD2840 initialization procedure.

After initialization, the user should place the WD2840 in the network mode with TXEN off and ITOKON on. This will cause the WD2840 to generate an ITOK interrupt each time a token is passed to its address (MA). The host must provide the timeout algorithm which should be greater than the maximum time for the network to pass the token around the ring twice. Checking twice eliminates the possibility that the Network is in the scan mode and sending tokens to non-existing stations.

It is useful to note that this constraint requiring each node which is participating in the network logical ring to have a unique address does not extend to nodes which are "listening" but not "in the ring." It might be useful to a network designer to have groups of receive only nodes which have the same node address but do not participate in the network token passing (see GIRING - CR13). Data frames transmitted to such clusters must not request acknowledgement since all nodes in the cluster would simultaneously respond.

Copy Mode

The COPY Mode is selected by setting the COPY control bit (CR02). Normally the WD2840 receives (DMA's into the receive buffer chain) data frames only if they contain the general broadcast destination address or if they are specifically addressed to the WD2840. This occurs when the frame's destination address (DA) matches the WD2840 my address (MA, set by the host).

However, when COPY mode is selected data frames which are specifically addressed to other nodes will be treated as broadcast frames by this node. The COPY mode allows a specific node to "eavesdrop" on data frame traffic on the network.

Nak Response

The WD2840 sends negative acknowledgements (NAK's) on response to received frames under several circumstances. The NAK prevents the transmitting node from wasting bandwidth retrying indiscriminately, and further, lends visibility to individual network node problems. The NAK includes a reason code which is available to the transmitter's software (via the TFSB).

Each data frame to be transmitted can be specifically marked (via the FCB) by the host to require an ACK/NAK response from the receiving WD2840. In the absence of errors, an acknowledge (ACK) frame will be returned to the transmitter as confirmation. However, several circumstances cause a Negative Acknowledge (NAK) to be returned:

1. Insufficient buffer space
2. Receiver not enabled (RXEN - CR05 cleared)
3. Receiver overrun
4. Frame exceeded 16 buffers in length

This information is placed in the transmitted frames's FSB. See section 2.1.2 for more details on the Transmit Frame Status Byte (TFSB).

2.0 INTERFACES

There are two interfaces to the WD2840: the host computer side, and the network side. The network side is conventional from an electrical point of view, the WD2840 performs all logical functions required to ensure communications capability on broadcast media (such as coax or RF).

The host interface involves two separate functional interfaces: the status/control registers described in section one, and a DMA interface that is described in the following subsection.

2.1 HOST

The WD2840 uses a complex memory buffer architecture allowing it to respond in real time to its network obligations (e.g., to meet network data rate and processing delay requirements). These memory structures are managed cooperatively by the host and the WD2840.

Memory management functions requiring real time response (e.g., traversing chains) are completely handled by the WD2840. Other important, but not time critical operations are the responsibility of the host software (such as removing used buffers from the transmit chain).

All memory references by the WD2840 are pointed to by memory locations (and internal registers) initially defined and set up by the host software. Initial values and memory based registers are grouped together and called the WD2840 Control Block.

The location of this control block is written into the registers CBPH and CBPL anytime the WD2840 is in Isolate State. This control block has the following structure:

CBP→	+0	NXTR (H)	Receive Buffer Chain (MSByte)
	+1	NXTR (L)	Receive Buffer Chain (LSByte)
	+2	NXTT (H)	Transmit Buffer Chain (MSByte)
	+3	NXTT (L)	Transmit Buffer Chain (LSByte)
	+4	BSIZE	Buffer Size / 16 (0-F = 64-1024 bytes)
	+5	EVT0	
	+6	EVT1	Eleven separate Event Counters, see section 2.1.1 for details
	....		
	+F	EVT10	

As the WD2840 transitions to Network State, it reads and uses the first five bytes of the control block. The remaining eleven bytes of event counters are accessed by the WD2840 only when each specific event condition occurs.

Either the Receive (NXTR) or Transmit (NXTT) chain entries in the control block may initially be zero; in such a case the WD2840 expects the chain to be extended by the host's changing the zero link field in the control block. Thereafter any such zero link would be in a buffer.

The WD2840 uses constant size buffers; their length is set by the value in location BSIZE. The buffer size is indicated by a 4-bit count in the least significant 4 bits of the BSIZE byte in the WD2840 control block. The buffer sizes available are multiples of 64; (BSIZE+1) 64 is the buffer size used by the WD2840. Thus a BSIZE range of 0-15 corresponds to actual buffer sizes of 64 through 1024 bytes. This buffer length is inclusive of control bytes and buffer link pointers.

The WD2840 includes a chained-block feature which allows the user more efficient use of memory, particularly in situations where the maximum packet size is much larger than the average packet size. One or up to 16 buffers may make up a frame but a buffer may not contain more than one frame.

Byte counters are associated with each frame (at the memory interface, not actually transmitted within the frame) so that frames on the network need not be integer multiples of buffers. The byte counters include all buffer management overhead. Therefore, a frame consisting of 100 transmitted data bytes, occupying two 64-byte buffers, would have a byte count of 110 (six bytes per frame + 2 bytes per buffer).

Since the WD2840 receive and transmit buffer chains are linked lists (see section 2.1.2 and 2.1.3) and are "followed" by the WD2840 but managed by the host; it is expected that the host will maintain both a FIRST and a LAST address for each chain. On transition into Network State, the chain origin information in the WD2840 control block is the same as FIRST. In fact, since the WD2840 does not change these control block entries, they can be maintained directly as FIRST by the host. An explicit LAST could be placed in an extended control block section.

The WD2840 "follows" the linked buffer chains by maintaining a NEXT address internally for each chain. This NEXT address can be in one of two states: 1) it can be the address of the next buffer in the chain, or 2) at the chain end (zero link), it can be the address of the buffer containing the zero link. The WD2840 uses a status bit for each chain, NXTR0 (receive) and NXTT0 (transmit), to differentiate the two states. When set they indicate the WD2840 chain NEXT address is in state 1 above; when clear they indicate state 2 above. This is an important distinction since it indicates whether the last buffer posted in a chain can be removed by the host (because the WD2840 has advanced to the buffer beyond) or must be left until the chain can be extended so the WD2840 can advance.

The host software monitors the progress of the NEXT pointer, and updates FIRST and LAST as it adds (and removes) buffers to (from) the chains as required. The WD2840 provides Interrupt Events (see IR0) and NXTR0, NXTT0 status bits to indicate when it advances along the two chains and exactly what state its NEXT address registers are in. The operation of these chains will be explained by example in later sections.

"Deadly Embrace" Prevention

A "Deadly Embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the WD2840. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the WD2840 and should also be obeyed by the user's CPU. This rule applies to the WD2840 memory registers and to the I/O registers. The Event Counters are an exception to this rule.

Rule:
If a bit is set by the CPU, it will not be set by the WD2840, and vice versa. If a bit is cleared by the WD2840, it will not be cleared by the CPU, and vice versa.

As an example, the NEWNA (CR10) control bit is only set by the host and is only cleared by the WD2840.

Dual DMA

The WD2840 may, for efficiency, interleave frame data fetch/store operations with fetches and stores of pointers and flags in memory. In all cases, operation sequencing is such as to prevent deadlocks and ambiguities between the WD2840 and software.

2.1.1 EVENT COUNTERS

Several non-fatal logical events are tabulated by the WD2840 and made visible to the host via memory based event counters (see WD2840 control block organization for specific locations). The WD2840 will increment each counter at the occurance of the specified event. Note that the WD2840 will not increment past 255. The host has the responsibility of initializing each counter.

COUNTER	DESCRIPTION
EVT0	"Set scan mode" frame received from the network. The NA register was redefined to MA + 1 at the time.
EVT1	Transmission error first attempt, second try successful. Can only occur for frames requiring an acknowledgement. It indicates no response was received for the first transmission; however, the second transmission was either ACK'ed or NAK'ed.
EVT2	Transmission error. Attempt aborted due to either transmitter underrun or frame length exceeding 16 buffers.
EVT3	Timer TD (network dead) expired.
EVT4	Access Control Frame Reception Error. A one or two byte supervisory frame (ACK/NAK, Token Pass, Scan Mode) has been received in error. This may be due to an FCS error, frame abort, or carrier loss detection.
EVT5	Data Frame Reception Error. An incoming data frame was incorrectly received due to an FCS error, frame abort, carrier loss detection, or receiving a data frame when expecting an ACK/NAK frame.
EVT6	NAK sent. Can occur for any of the following reasons: 1. Insufficient buffers in chain 2. Receiver not enabled (RXEN clear) 3. Receiver overrun 4. Frame length exceeded 16 buffers
EVT7	Invalid frame received. Caused by the detection of certain abnormal network conditions such as receiving an ACK/NAK frame when not expecting one, receiving a Scan mode frame when expecting an ACK/NAK frame, or receiving an invalid supervisory frame.
EVT8	Duplicate token detected. This counter will be incremented when the WD2840 determines that more than one token exists in the logical ring. This happens if a token pass is received when the WD2840 already has the token, or a data frame is received when the WD2840 is waiting for an acknowledgement frame.
EVT9	Not used.
EVT10	Duplicate node address. This counter will be incremented when a data frame being DMA'd into memory has a source address (SA) equal to the WD2840 node address (MA). This counter when used with COPY mode (CR02) is one way for detecting other nodes with the same node number (MA).

2.1.2 TRANSMIT MEMORY INTERFACE

When the token is received, data transmission is enabled (TXEN - CR06 and TXDEN - CR07 both set), and if the access hold-off counter has reached its limit, the WD2840 will determine whether any data frames are pending in the transmit chain. If so, it will transmit the first data frame in the chain. Otherwise the token will be passed. A given data frame will be the last frame transmitted for this token if any of several conditions occur:

1. ISOL (CR00) is set indicating the host has requested a transition to Isolate State.
2. TXDEN (CR07) is clear indicating the host has changed data frame transmission rights.
3. The frame FSB indicates this frame should be the last transmitted for this token.
4. The running frame counter has reached its limit (TXLT).
5. No further frames are pending in the transmit chain.

If any of the first four reasons above are true a token pass will occur. If the last frame does not require an acknowledgement, the WD2840 will piggyback the token pass if that is permitted (CR16). If the token cannot be piggybacked or if the last frame transmitted is the last frame pending (condition #5 above), an explicit token pass will occur. A piggyback token will not occur for the last pending frame because, for the general multiple buffer case, it is not known to be the last pending frame until after the transmission is complete.

The WD2840 will read and evaluate the address of the next frame at two specific points in time:

1. At the end of the prior frame, even if the prior frame is the last to be transmitted for this token.
2. When the token is received and data frame transmission is permitted.

If a non-zero frame address is found at time 1 above, it is kept and used without being re-read at time 2 above. However, if no pending frame is found at time 1, this is noted with the NXTT0 flag clear and the chain re-inspected on each occurrence of time 2 above.

As frame transmission commences, the WD2840 reads the address of the next buffer, the frame control byte, (FCB) and the frame length. It then starts reading bytes from the buffer and sending them until the frame length count or the end of the buffer is reached. The new buffer is read and data transmitted as before. (See Figure 2.1)

The frame length provided in the LENGTH field must be the sum of the overhead bytes and number of data bytes (see Fig. 2.1).

Simplified formula for LENGTH:

LENGTH = # of data bytes + 2 link bytes per buffer + 6 overhead constants per frame.

Example #1

LENGTH = 8 (0010_H in LENGTH field)

implies one buffer is used for this frame (64 bytes) two link + six overhead, no data.

Example #2

LENGTH = # of data bytes + 2 link bytes per buffer + 6 overhead constants per frame.

Programmed buffer size = 64 bytes per buffer. Two buffers are used in this frame for a total of four link bytes (2 per buffer), six overhead, and 57 data bytes.

The General Formula for LENGTH

WHERE

N_D = # of data bytes (max 4095)

6 = Overhead Constant per frame (FSB, FCB, LENGTH (H), LENGTH (L), DA, SA)

B_K = B SIZE in bytes (64, 128, etc.) a constant preprogrammed into the WD2840 on 64 byte boundaries to a max of 1024 bytes.

GIVEN N_D

$$L = N_D + 8 + 2^* \text{ TRUNC } \frac{N_D + 5}{B_K - 2}$$

GIVEN L

$$\#B's = 1 + \text{TRUNC } \frac{L - 1}{B_K}$$

$$N_D = L - 6 - 2(\#B's)$$

NOTE:
The expression for N_D fails for values of $L = B_K + 1$. This is okay since the 2840 doesn't generate such values.

Examples: Find L given N_D

	N_D	L	
	0	8	
	1	9	1 bufr
	56	64	
$B_K = 64$	57	67	2 bufrs
	118	128	
	119	131	3 bufrs
	120	128	1 bufr
$B_K = 128$	121	131	2 bufrs
	246	256	
	247	259	3 bufrs

Find #B's, N_D given L

	L	#B's	N_D
	8	1	0
	9	1	1
$B_K = 64$	64	1	56
	67	2	57
	128	2	118
	131	3	119

	L	#B's	N_D
	128	1	120
	131	2	121
$B_K = 128$	256	2	246
	258*	3	246
	259	3	247

***NOTE:**
Case corresponds to buffer end and frame end on same byte . . . extra buffer consumed.

When the frame length is finally reached, the WD2840 pauses if an acknowledgement has been requested. The frame status byte (FSB) is updated when the frame is completed; its posting indicates frame completion and gives information about the success or failure of the frame transmission. At frame completion, the WD2840 attempts to advance along the transmission chain to identify the next frame regardless of whether it will be transmitted with this token or later.

The host may add frames to the end of the transmit chain at any time by changing the zero link in the last buffer. Also buffers of all posted frames up to but NOT including the last buffer of the most recently posted, may be arbitrarily removed from the chain. The last posted frame (more specifically, the last buffer of the last frame) may only be removed and reused if NXTT0 is set. This indicates that the WD2840 has advanced its NEXT address to the next frame but that its transmission has not been completed (in fact, perhaps not even started).

NOTE:
The WD2840 checks only the most significant byte of the link field for zero link detection. This has the following implications:

1. When writing into a zero link field, the host must write the LSB of the new link field first, followed by the corresponding MSB.

2. All buffers must have a starting address greater than or equal to Hex '0100'.

TRANSMIT FRAME STATUS BYTE (WRITTEN BY WD2840)

BIT #	7	6	5	4	3	2	1	0
Name	DONE	WIRING	X	X	SELF	VAL2	VAL1	VAL0

BIT	NAME	DESCRIPTION
7	DONE	Set to guarantee a non-zero value for the posted FSB.
6	WIRING	Value of the corresponding bit in received ACK frame.
5-4	—	Reserved.
3	SELF	When set, indicates the ACK/NAK code appears in the value field (bit 2-0) of this FSB is assigned by the WD2840 transmitter routine. When clear, indicates value resulted from ACK/NAK code from receiving station.
2-0	VAL	An encoded field whose interpretation depends upon the SELF flag (bit 3) in this FSB. a. SELF clear 0 0 0 — No receive error (= ACK when DONE is set). 0 0 1 — Insufficent buffers for frame. 0 1 0 — Receiver not enabled at frame start. 0 1 1 — Receiver over-run. 1 0 0 — Frame exceeded 16 receive buffers. b. SELF set 0 0 0 — No transmit error. 0 0 1 — Transmission failed after retry. 0 1 0 — Transmission under-run. 0 1 1 — Premature end of chain. 1 0 0 — Transmission frame exceeded 16 buffers.

Transmit Frame Status and Control Bytes

Each frame has two bytes reserved, one for host control information needed by the WD2840, the other for status information posted by the WD2840 at frame transmission completion. The frame control byte (FCB) is only read by the WD2840, never changed; the frame status byte (FSB), is written (posted) by the WD2840 with no regard for its prior contents. On completion, the FSB value will always be non-zero; it is important that the host zero the FSB byte in order to be able to recognize a posted frame.

NOTE:
Specifically note in Figure 2.1 that the first buffer of each frame has a different structure than any overflow buffers for that frame. In particular, each frame has only one set of FSB, FCB, and LENGTH fields regardless of the number of buffers required by the frame.

TRANSMIT FRAME CONTROL BYTE (WRITTEN BY HOST)

BIT #	7	6	5	4	3	2	1	0
Name	WACK	FCBLF	TRANSP	X	X	X	X	X

BIT	NAME	DESCRIPTION
7	WACK	Wait for Acknowledgement. Instructs the WD2840 to wait for an ACK/NAK response from the receiver for this particular frame only. The token control (TC) byte in the frame is automatically set to cause the destination node to respond. This bit must NOT be set if the frame uses the broadcast destination address. Inadvertently doing so will cause the frame to be posted "Transmission failed, due to max retries."
6	FCBLF	Last Frame. This bit will cause the WD2840 to pass the token either piggybacked with this frame (if possible) or explicitly after the frame transmission completes.
5	TRANSP	Transparent Frame. This bit will cause the WD2840 to interpret the buffer contents to be the exact sequence of bytes to be transmitted. The normal token control (TC) byte and source address (SA) byte generation is suppressed. Note that for a non-transparent data frame the TC byte must NOT appear in the buffer.
4-0	—	Reserved.

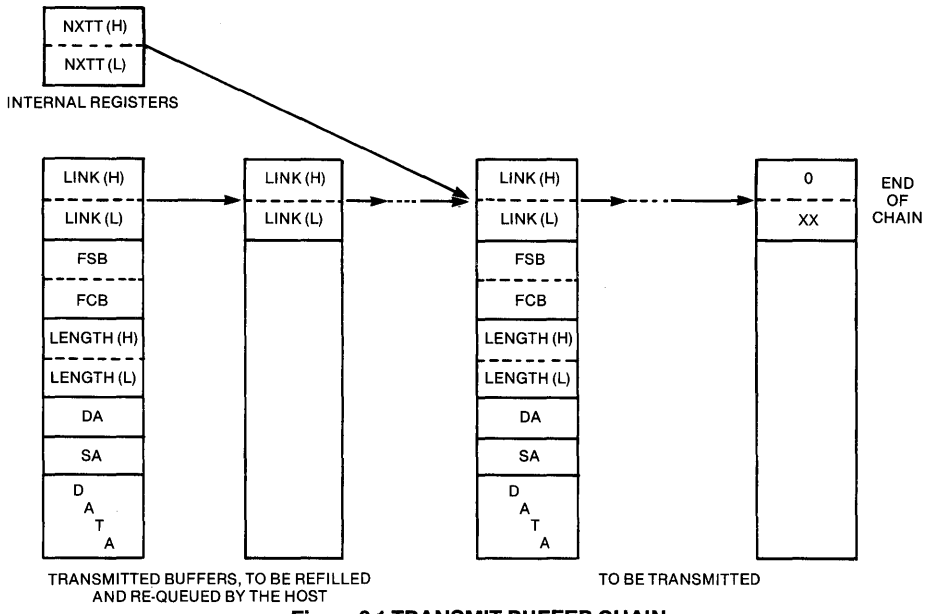


Figure 2.1 TRANSMIT BUFFER CHAIN

2.1.3 Receive Memory Interface

After the third byte of an incoming data frame is detected, the WD2840 will begin to place frame data into memory if several conditions are satisfied:

1. Receiver Enabled (RXEN-CR05 set).
2. There is an available buffer in the receive buffer chain.
3. The frame is addressed to this node specifically, it is a broadcast frame, or COPY mode has been selected by the host.

As the frame continues, it may completely fill its buffer. If this happens the WD2840 reads and inspects the link field of the current buffer. If this link is zero, an error occurs and the receive chain is reset to reuse from the first buffer used by the dropped frame. However, if another buffer is available, the incoming frame is continued beginning in the third byte of that buffer. This continues until one of several things happen:

1. Receiver overrun. The WD2840 has a four byte FIFO to buffer incoming frame data; however, if the host DMA responds too slowly a receiver overrun will occur. If this happens an event counter is incremented, the frame is dropped, and the receiver buffer chain is reset to reuse buffers of the dropped frame.
2. Current buffer capacity exhausted. If 16 buffers have been used for the current frame, an event occurs with the frame being dropped and the chain reset. Otherwise the WD2840 attempts to advance to the next buffer in the receiver buffer chain. The frame data will be continued in this subsequent buffer. If the end of the receiver buffer chain is reached an event counter is incremented, the frame is dropped, and the chain reset.
3. Frame ends. If the FCS is not correct an event counter is incremented, the frame is dropped, and the chain is reset. If correct however, the frame length is placed in the LENGTH field and the Frame Status Byte (FSB) is posted "done, no error."

If the frame is addressed to this node and indicates an acknowledgement is required (TC = 255), whether or not an error occurs, the WD2840 responds with an ACK/NAK supervisory frame indicating either success or failure. In case of receiver over-run, bad FCS, and SA = MA acknowledgement request will be ignored. (See section 1.4.3 for details)

It is the host's responsibility to ensure that buffers are available, initialized (FSB zero'ed), and attached to the end of the receive buffer chain.

RECEIVE FRAME STATUS BYTE (WRITTEN BY WD2840)

BIT #	7	6	5	4	3	2	1	0
Name	DONE	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
7	DONE	Set to indicate the frame reception is complete.
6-0	—	Reserved.

RECEIVE FRAME CONTROL BYTE (WRITTEN BY HOST)

BIT #	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
7-0	—	Reserved.

2.2 MODEM INTERFACE

The modem interface is the conventional half duplex NRZ type with separate data and clock (Figure 2.3). When the WD2840 desires to transmit, it asserts $\overline{RTS}$ and awaits $\overline{CTS}$. $\overline{RTS}$ is generally used to enable the modem transmitter. After a system dependent preamble is generated, the modem asserts $\overline{CTS}$ which allows the WD2840 to begin the actual transmission of the frame. (Note: $\overline{CTS}$ may be asserted permanently if the transmission system does not need to generate a preamble).

The $\overline{SQ}$ input is used on receive to indicate a valid carrier. If this term is negated anytime during a receive message, the WD2840 will presume the message is in error and treat it as an abort. This signal is used to augment message integrity beyond that of the CRC by allowing a modem to detect and report low level faults (such as out-of-frequency carrier or missing clock).

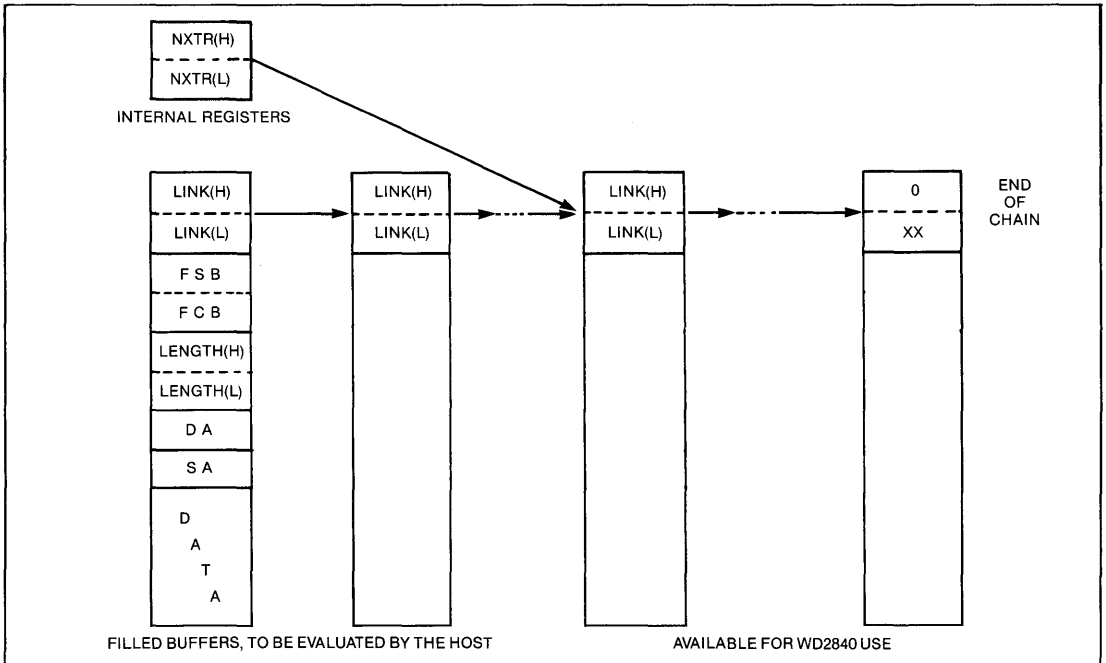


Figure 2.2 RECEIVE BUFFER CHAIN

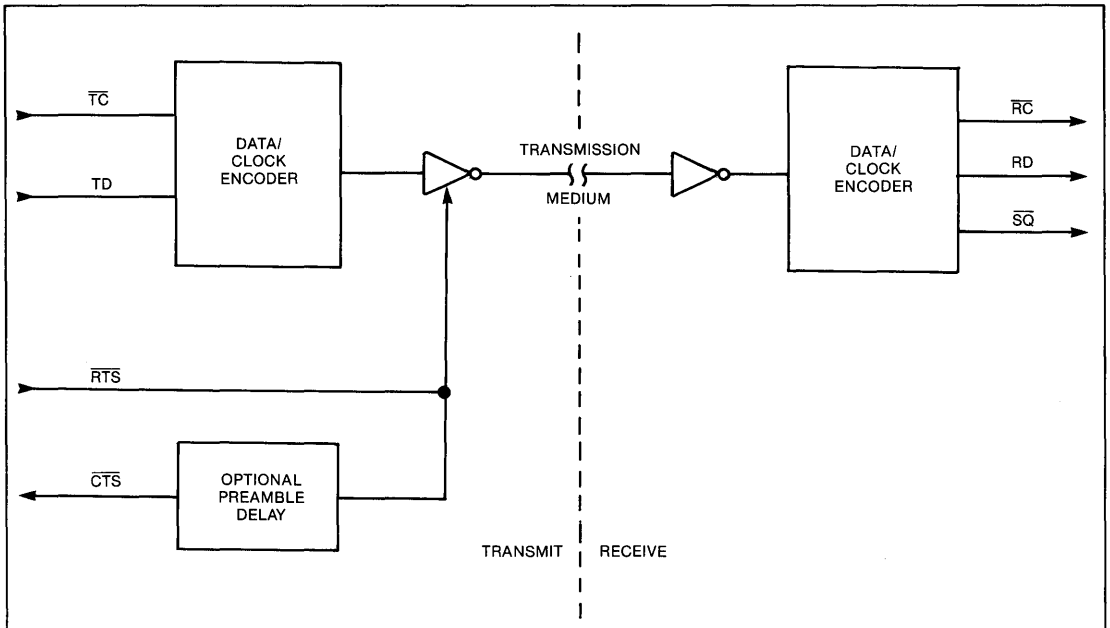


Figure 2.3 CONCEPTUAL MODEM

3.0 NETWORK PROTOCOL

To enable operation on a broadcast medium without the need for a central controller performing device polling, the WD2840 implements a media access protocol. The particular access protocol designed into the WD2840 prevents self-induced transmission collisions and ensures a fair and guaranteed distribution of transmission time among attached controllers. (See Appendix A for Protocol flowcharts.)

This design-out of collisions allows the WD2840 a greatly expanded selection of transmission media, since no physical characteristics of a particular medium are relied upon for proper network operation. Another benefit of this lack of collisions is the visibility of network faults. If a collision is detected, it is treated consistently in a error recovery mode by the WD2840 and is also unambiguously visible to service personnel as a fault.

Secondly, the WD2840 can ensure that a transmitted message was correctly received and buffered by requiring acknowledgement of its receipt. This is sometimes called "acknowledging datagrams" where the sender awaits a predefined period after a frame is sent for a reply from its destination. With this method, no sequence counters nor multi-frame retransmission buffering is required. The scheme is efficient since local network applications such as the WD2840 address do not encounter extremely long transmission delays (such as satellite links) as in conventional data networks (such as X.25).

Both functions are parameterized, allowing tuning and optimization by the user to his unique application. These parameters may be adjusted in real time by the user's software, allowing a dynamic network, responsive to constantly changing requirements.

The two functions, access control and data transmission, function simultaneously though independently. Thus they are described separately as subprotocols for clarity.

3.1 Data Transmission

The data transmission cycle is entered after the token has been received and data transmission rights validated (see section 3.2 "access method"). The WD2840 determines if there is a frame to be sent and, if not, simply sends the token to the next station.

If something is queued for transmit, the WD2840 DMA's it from memory and sends it. After the complete frame has been sent, the WACK (Wait for ACK) bit is tested in the TFSB (Transmit Frame Status Byte). If set, the WD2840 waits for, and expects, an acknowledgement from the frames recipient. A timer (TA) is started. In the normal case, the ACK is received before TA expires which causes the WD2840 to send the next frame queued, repeating this procedure. Thus, the WD2840 sends multiple frames to various destinations until the transmit queue is emptied or a programmed limit (register TXLT) is exceeded.

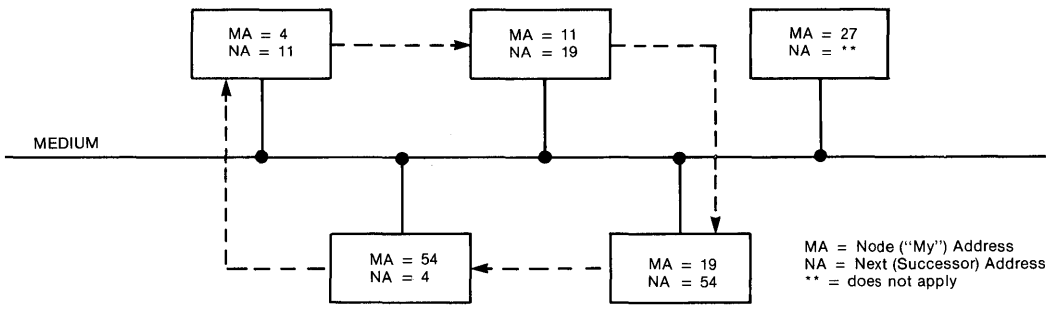


Figure 3.1 TOKEN PASSING ON A LOGICAL RING

In the event TA expires, the frame is re-transmitted once. (Note: it is the responsibility of higher level protocol operating in the host to protect against the possibility of duplicate frame reception.) If TA expires again, usually indicating the destination node is off-line, the FSB is updated to reflect the unsuccessful transmission, interrupt bit ITA is set, and the frame is skipped.

A frame is also skipped and tagged if the destination station sends a NAK, indicating it cannot presently process the frame.

TRANSMISSION OF ABORT

An ABORT is transmitted by the WD2840 to terminate a frame in such a manner that the receiving station will ignore the frame. An ABORT is sent when there is a Transmitter Under-Run. The abort sequence is a zero, followed by seven ones, after which RTS is set false.

3.2 ACCESS METHOD

The WD2840 network access method is based on the use of tokens, the specific granting of transmission rights passed from station to station. At any given time, exactly one station has the right to transmit (this right is called the token) and is obligated to pass it on when finished with it.

This can be clarified by referring to Figure 3.1. We assume in this figure that the network has already been initialized (meaning that the linkages in the access ring have already been established) and the token is held at this instant by station 4 (the station whose MA register = 4).

When station 4 is ready to pass his access right on, he sends a message to the station number called out in his internal register NA, in this case 11. The message, and thus the token, are received by station 11 who can now transmit its message(s). When station 11 is ready to pass the token, it sends a message to station 19, as directed by its internal register NA and the cycle continues, in a circular fashion, from station 4 to 11 to 19 to 54 to 4...

Notice that the station numbers need not be contiguous. This relatively arbitrary station numbering (in the example) poses no inefficiency to the access method. The value of this is the ability to add and remove stations (re-configure) on the network without re-arranging everyone elses addresses. (See section 3.2.2 for an example).

In this way, the token is passed from one station to the next in a logical ring.

3.2.1 ACCESS INITIALIZATION/ERROR RECOVERY

When the WD2840 is commanded into Network State, the Next Address Request (NAR) register and the NEWNA (CR10) flag must be used to define the Next Address (NA) register. When it is necessary to pass the token, it is passed to the current node number in register NA. If station NA is not on-line, determined by its lack of response, station NA + 1 is tried. This process continues until a station is found

which does respond. The responding station number is written into register NA so that this scanning procedure need not be repeated on subsequent access cycles.

NOTE: 1. Node numbers 0 and 255 are reserved and cannot be used. Consequently scanning occurs circularly in the range 1-254.

2. During Scan mode token passing to each node is only tried once.

Anytime a station cannot successfully pass a token within two attempts, register NA is updated to NA + 1, and a new "next" station is searched for. The result is the removal of non-responding station(s) from the access ring. An interrupt (INS) is generated indicating a network exception caused a change to NA.

The above description covers network recovery from station failure and purposeful removal of stations during on-line network operation. Setting stations in the scan mode can also be accomplished by sending control frames (a Scan frame redefines NA = MA + 1) over the network. The control frame may be directed to a single station, or all stations simultaneously (using the broadcast address). It is this scanning for new stations that permits on line addition to the access ring.

NOTE:
The policy of the SCAN frame is redefined by the user software as required by the application. For example: in a process control environment where stations are not often added while the network is in use, this procedure would be initiated rarely if at all.

3.2.2 REMOVING A STATION

There are two ways a station can be removed from the access ring: non-response due to station failure and non-response due to host commanded transition to the Isolate State. Both are treated identically from a network point of view.

Referring to Figure 3.1, assume that station 19 is removed from the network (either physically or logically). In this example, station 11 would detect a network fault when trying to pass the token to 19 (time TA would expire since station 19 will not respond). Station 11 detects this and finds the next station in the access ring by using the "scan" function (similar to initialization). The next attempt at passing the token would be to station 20, register NA + 1.

By starting the token ring recovery procedure at the intended station plus one (station 20) rather than MA + 1 (station 12) as is done in initialization, recovery delays are minimized (since fewer stations are tested for presence, 8 less in this example).

The next station found would be number 54 in the example which station 11 writes into his register NA (now "patching out" dead station 19). The next time station 11 is finished with the token, it directly sends it to 54, making the sequence now 11 to 54 to 4 to 11 to 54...

3.2.3 ADDING STATIONS

There are three primary methods by which a station can be added to a network. The first is a distributed method, in which each station in the network can poll for new stations in the gap between its address and the next address (between MA and NA). Second is a centralized method, in which an individual station designated by the network architect can interrogate the entire address space seeking a new station desiring INRING. The third — central scan — is a simpler (from the host point of view), centralized method in which a station can send a global frame causing all the on-line TACs to reset their next address register. This causes each TAC to poll its address space at its next token-pass attempt. Each method has advantages and disadvantages.

Distributed Method

The distributed method does not rely on a specific station. Thus, there are no problems or efforts spent selecting the administrator, nor is there any concern about backup administrators. In the distributive method, each station has the same responsibility to allow new access members as other stations. This method is the most host intensive and requires each station to maintain a timer (that can be configuration set as to its value) as to how often it should poll its gap for new stations.

For example, assume the timer in each station is 5 sec. and that station 4's timer has expired (Fig. 3.2.3.1). The host attached to station 4 notes that the next address register (NA in the TAC) is set to 11, which indicates that a new station might be added to the network as station number 5, 6, 7, 8, 9, or 10.

The host queues a frame into the TAC transmit chain, polling station 5. This frame will be sent by 4 with an acknowledgement requested from 5. If 5 is present it responds; otherwise, the TAC aborts its attempt after time TA. The TAC marks the result on the frame in the host memory space and proceeds with other tasks.

After this exchange, the host, at its leisure, checks the transmit status of the frame. The host sees that the frame acknowledgement timed out, meaning that station 5 has not been added to the network, or that station 5 is on the network and whether the request INRING is set in the network code field. In either case, the host takes appropriate action. If the desired INRING bit is set, station 4 changes its NA register to 5, allowing its next token to be passed to 5. This action puts station 5 in the ring.

Depending on an application's sophistication, a control message can be sent to station 5. That message says, "Your successor is X." In this case, X = 11, so that 5 is not forced to poll for its successor. In any case, 4 updates its next address register to 5 and does not need to go through this distributive polling cycle again because there is no gap between 5's address and the next address; there is no possibility that a new station can be inserted between addresses 4 and 5. If 5 didn't respond to 4's poll, station 4 updates its poll counter so that the next time that the poll timer times out, station 6 will be tried.

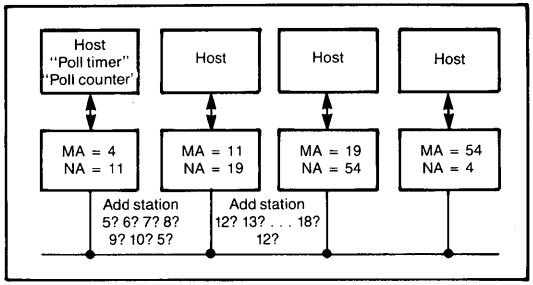


Fig. 3.2.3.1 Distributed polling. *Each host polls the gap in its address space for the possible addition of new stations. The host internal poll timer and poll counter set the polling rate and range as desired.*

If node 6 responds, its desired INRING bit is tested as above. If 6 does not respond, the host will queue a poll to station 7 the next time its poll timer expires. This continues until the host completes 10, when the cycle goes back to 5 and repeats. In this example, with a gap of 6 stations (between 4 and 11), and with a 5-sec. clock, a new node can be added within 30 sec.

In the centralized station-addition method, a single station can poll the entire address space, seeking a new station that desires INRING. One reason for centralizing this function might be the more careful control that can be placed in a network. There can also be optimizations. For example, the central polling station can keep track of the stations that already exist and, therefore, bypass some address ranges. A polling station may know the network will never have more than, say, 75 stations, In the example of Fig. 3.2.3.2, when station 4 starts polling, it polls only to address 75 before resetting to zero. This works like the distributed method except that a single station does all the work.

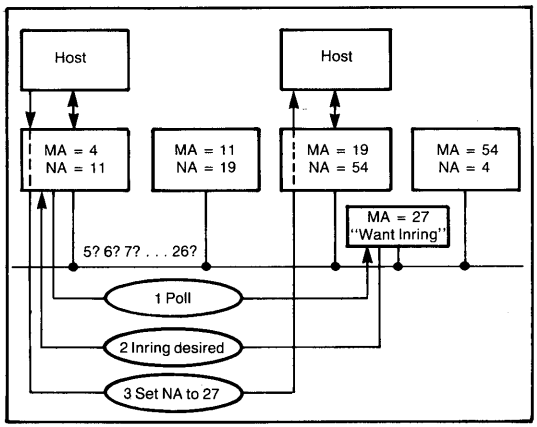


Fig. 3.2.3.2 Central polling. *A single station — in this case, station 4 — dubbed "the administrator," can be charged with all polling tasks. This simplifies the software in the other stations and centralizes network control.*

When the polling station determines that a station has been added, it must place the new station in the access ring. For example, station 4 is the centralized station doing all the polling (Fig. 3.2.3.2), and it discovers that station 27 has recently been added. Station 4 knows this because station 27 now responds to a first-time poll, and because its status bit is set, indicating that it wants to be added to the ring. (Some stations may be receive only, never desiring the right to initiate transmissions.) Station 4 sends a high-level message to the software in station 19, telling it to change its next address register to 27. This message can also prompt station 19 to tell 27 its next address register should be 54. This gets confusing, but it is all done with high-level software. These tasks are not real time and are quite efficient from the network point of view.

Station 4, the administrator, need not create and maintain a table of active stations on the network because the poll response returns three pieces of information. As node 4 polls the stations on the network, it finds out (a) that the polled station does not respond at all, as it would if it polled station 12 in Fig. 3.2.3.2 (b) that the station is already part of the network an is already in the ring or is receive only, as it would if station 4 happened to poll station 11 or 19; and (c) whether the station is attached to the network, is alive and wants to be in the ring, as is the case with a poll to 27. These indications are conveyed by a combination of status bits sent back by the acknowledge frame. This acknowledge frame and status information are transferred at a TAC device level, so a host is not concerned with whether its station wants to be in the ring. The host simply sets up the proper bits in the control registers; the bits are relayed automatically by the TAC. Thus, with a simple algorithm, an administrative station can poll the entire network address range and know the network's exact membership and status.

Central Scan

Central scan is the simplest method of adding stations to a network. It involves sending a global frame to all

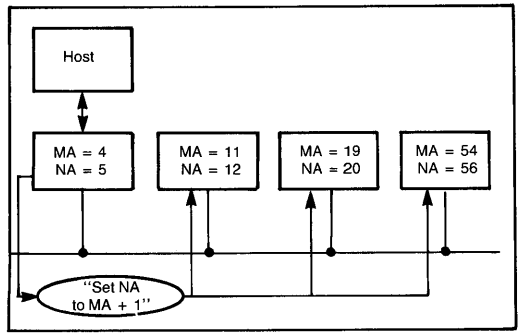


FIG. 3.2.3.3 Central scan request. *A special command can be sent by any station causing all attached TACs to set their NA register to the address of the next possible node. This causes each TAC to poll without the help of the host.*

stations on the network, which forces each to update its own next address register to its station address plus one (NA = MA + 1). Assume station 4 is the centralized station and sends the scan command frame (Fig. 3.2.3.3). Station 11, upon receiving it, automatically sets its next address register to 12 (the TAC does this; the host is not involved but is notified of the situation). Also, station 19 sets its next address register to 20, and station 54 sets its NA register to 55.

The result of this is a round of polling at the TAC level. Station 11, on completing its use of the token, tries to send it to 12. The token to station 12 times out because 12 is not present. Station 11 reclaims the token trying to send it to 13 and so on, causing 11 to poll for station addition. The drawback of this is the huge time disruption incurred by the simultaneous polling.

It is not required that station 4 send this scan control frame to all stations at the same time. If it is known that station 11 exists in the network and that a station may be trying to add into the network after station 11 in the address space, a command can be sent to 11 telling it to set its next address register to 11 + 1. Now 11 will go through scanning station 12, 13, 14 . . . again without intervention from station 11's host software. This directed scanning has the effect of smoothing the polling disturbance over a greater time.

The trade-off of all these methods is the software complexity distribution. If a TAC user assumes more responsibility, providing more intelligence distributed in the software, the system can be more sophisticated in handling new stations. If a user wants the TAC to handle this task itself, saving host software development, he pays only slightly in inefficiency. TAC gives the user an option.

3.2.4 INTERACTION OF THE SUB-PROTOCOLS

After a station is given the token, it will send an information frame, a token frame, or a combination of both. It is this combination frame, referred to as a "piggy back" token, that causes the sub-protocols to interact slightly.

In the normal case (no time-out), the SOURCE may transmit a combination frame to the DATASINK when his access period is over. All stations on the network observe this; after the reception of the current frame is complete, the one whose MA register matches the token address in the frame (TC) knows it has the token.

In the case of a combination frame, the SENDer resets his timer TA on transmission complete and waits for the NA station to transmit something valid,

FIELD DESCRIPTIONS AND ENCODING

TC

The token control byte has the dual purpose of transferring access control between stations and conveying a request for immediate acknowledgement of the frame by its intended receiver.

There is no interaction between the TC field and the DA or SA fields. Thus the token may be transferred to one station and data sent to the same or a different station, with one single frame. The value entered into the TC field is determined by the WD2840 and does not appear in the buffer (except for transparent frames).

TC Value	Meaning
0	Token not affected at this time.
1-254	After current frame, the token belongs to station TC. (The sending station has recovery responsibility).
255	Immediate ACK requested. Token not affected.

NOTE:
The sharing of this field prevents the passing of the token with data (piggy-back) and acknowledgement requests on the same frame. This combination is specifically disallowed because of its undesirable characteristics in network error situations.

DA

Destination address. Value of zero is reserved, 1 to 254 indicates the destination address of the frame. The value 255 is the global (or broadcast) address.

SA

Source address. The values of 0 and 255 are reserved. A value of 1 thru 254 is the address of the sender of the frame.

I

Information Field. User defines format and content.

FCS

Frame Check Sequence. The FCS calculation includes all data between the opening flag and the first bit of the FCS, except for 0's inserted for transparency. The sixteen bit FCS is compatible with the standard HDLC FCS.

AC

Access Control. Conveys supervisory information. May be sent as a command using transparent mode or received in response to an ACK/NAK request. Its format is shown below:

ACCESS CONTROL FIELD

BIT #	7	6	5	4	3	2 1 0
Name	SCANF	WIRING	0	0	0	NVAL2 — NVAL1 — NVAL0

BIT	NAME	DESCRIPTION
7	SCANF	Scan Mode (Command). Indicates that the addressed node(s) must redefine NA = MA + 1 for use on its next token pass.
6	WIRING	Wants in ring (Response). This bit when set informs the node requesting the ACK frame that this node is not in the logical ring, but is requesting entry. It is the logical function of the transmitting node's GIRING .AND. INRING. (see CR13 and SR20) The WD2840 does not act on this information but merely passes it to the host via the ACK'ed frame's FSB.
5-3	—	Reserved.
2-0	NVAL	An encoded NAK/ACK value (Response). The receiving node will set one of the following codes depending upon the state of the last received frame: 0 0 0 — No error 0 0 1 — Insufficient buffers for frame 0 1 0 — Receiver not enabled at frame start 0 1 1 — Receiver overrun 1 0 0 — Frame exceeded 16 receive buffers

to verify his reception of the piggy back token. If the timer expires, the sender sends an explicit token (the data from the combination frame is assumed to have been accepted) and enters the normal token sub-protocol.

The user is prevented from sending a combination frame and requesting an acknowledgement at the same time to prevent possible network state conflict under time-out conditions.

3.3 FRAME FORMAT

The frame format the WD2840 uses to transmit all data and control frames is similar to the industry standard HDLC. A 16 bit CRC is implemented and standard zero insertion (CRC16-CCITT) is used for framing. This framing method allows the use of standard network monitoring and diagnostic equipment such as data scopes and logic analyzers.

Additional address fields and control points are defined as required to support the protocol.

Normal Frame Format:

F - TC - DA - SA - I - FCS - F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
DA = Destination Address (8 bit)
SA = Source Address (8 bit)
I = Information Field (0 to 4095 bytes or 16 buffers, whichever is less).
FCS = Frame Check Sequence (16 bit)

Access Control Format:

F - DA - AC - FCS - F

F = Flag, binary pattern 01111110
DA = Destination Address (8 bit)
AC = Access Control Field (8 bit)
FCS = Frame Check Sequence (16 bit)

Token Pass Format:

F - TC - FCS - F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
FCS = Frame Check Sequence (16 bit)

3.4 SENDING A TRANSPARENT OR ACCESS FRAME

Two types of frames are transmitted under the transparent mode under user control. A scan access frame or a transparent frame. The format of the frames are described under 3.3 Frame Format with the transparent format the same as Normal Frame Format.

ACCESS FRAME COMMANDS

There is only one Access Frame type permitted under user control — Scan Frame. The node that is addressed must redefine NA = MA + 1 for use on its next token pass. The format for sending this frame is:

LINK (H)	Pointer to next frame.
LINK (L)	
00 (FSB)	
20h (FCB)	Transparent frame, no acknowledge allowed.
00 LENGTH (H)	Access Control frame size (H, L).
08 LENGTH (L)	
DA	Destination Address or 255 broadcast.
80h	Set Scan Mode.

The FCB can be set for last frame, the acknowledge bit has no effect and no acknowledgements will be given to access frames nor will they be expected by the transmitting WD2840.

The node receiving the access frame will only recognize a scan access frame as a command. Event count #0 will increment and the receiving node will set its NA to MA + 1. Any other access code will increment Event Counter #7.

TRANSPARENT FRAME

Link (H)	
Link (L)	
FSB	
20H FCB	
XX Length (H)	
>08H Length (L)	
TC	pass token, broadcast, ackreq.
DA	
SA	
DATA	

The Transparent Data Frame allows a user to control the token pass, or TC field of a frame by using the first byte after length rather than the FCB. The frame transmitted will look like the User Info part of the buffer without the WD2840 firmware generating anything else but the flags and FCS.

4.0 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

Voltages referenced to V_{SS}
High Supply Voltage (V_{DD}) ..... −0.3 to 15V
Voltage at any Pin ..... −.03 to 15V
Storage Temperature Range .... −55°C to +125°C
Electro-static voltage at any pin ..... 400V (Note 6)

NOTE:
Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

OPERATING CHARACTERISTICS (DC):

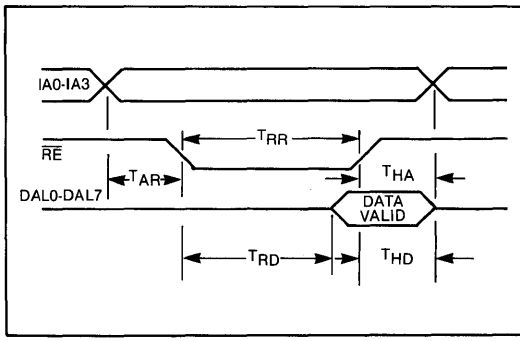
Operating Temperature Range ..... 0°C to +70°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{DD}	V_{DD} Supply Current		18	30	mA	
I_{CC}	V_{CC} Supply Current		160	220	mA	
V_{DD}	High Voltage Supply	11.4	12	12.6	V	
V_{CC}	Low Voltage Supply	4.75	5	5.25	V	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -0.1mA$
V_{OL}	Output Low Voltage			0.4	V	$I_O = 1.6mA$
I_{OZH}	Three-State Leakage			50	μA	$V_{IN} = V_{CC}$
I_{OZL}	Three-State Leakage			50	μA	$V_{IN} = 0.4V$
I_{IH}	Input Current			10	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Current			10	μA	$V_{IN} = 0.4V$

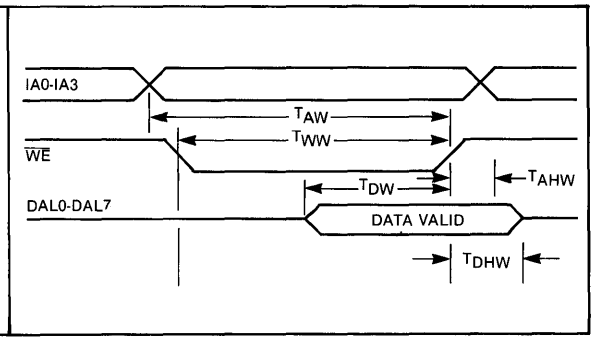
5.0 TIMING CHARACTERISTICS (AC):

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CLK	Clock Frequency	0.5		2.05	MHz	Note 1, 7
RC	Receive Clock Range	0			MHz	Note 4, 7
TC	Transmit Clock Range	0			MHz	Note 4, 7
MR	Master Reset Pulse Width	10			mS	
T_{AR}	Input Address Valid to $\overline{RE}$	0			nS	
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid	2		375	nS	Note 5, 2
T_{HD}	Data Hold Time From Read to Strobe	20		100	nS	
T_{HA}	Address Hold Time From Read Strobe	0			nS	
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	100			nS	
T_{WW}	Minimum $\overline{WE}$ Pulse Width	200			nS	
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100			nS	Note 2, 3
T_{WRR}	CS High Between Writes	300			nS	
T_{RDR}	CS High Between RE	300			nS	
T_{RR}	RE Pulse Width	375			nS	
T_{DAK}	DACK Pulse Width	375				
T_{AHW}	Address Hold Time After $\overline{WE}$	80			nS	
T_{DHW}	Data Hold Time After $\overline{WE}$ or After $\overline{DACK}$ for DMA Write	100				
T_{DA1}	Time From $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1			80	nS	
T_{DA0}	Time From $\overline{DACK}$ to Output Address Valid if ADRV = 0			375	nS	Note 5
T_{DD}	Time From Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)			375	nS	Note 5
T_{DAH}	Output Address Hold Time From $\overline{DACK}$	20		100	nS	
T_{DMW}	Data Hold Time From $\overline{DACK}$ For DMA Read	20		100	nS	Note 2
T_{TDV}	TD Valid	100			nS	
T_{SRD}	RD Setup	0			nS	
T_{HRD}	RD Hold	320			nS	

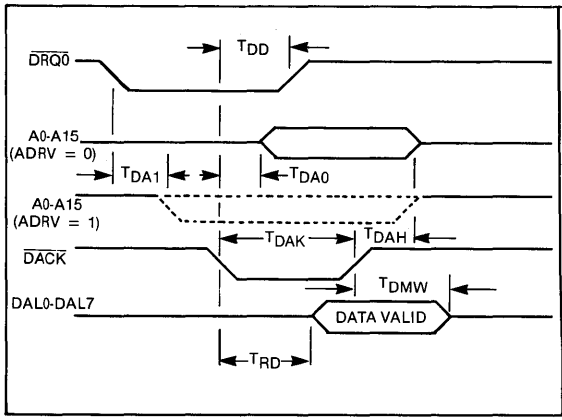
NOTES:
1. Clock must have 50% duty cycle.
2. There must not be a CPU read or write ($\overline{CS}$-$\overline{RE}$ or $\overline{CS}$-$\overline{WE}$) within 500 nanoseconds after the trailing (rising) edge of $\overline{DACK}$.
3. There must not be the leading (falling) edge of $\overline{DACK}$ allowed within 500 nanoseconds after the completion of a CPU write ($\overline{CS}$-$\overline{WE}$).
4. See "Ordering Information" for maximum serial rates.
5. C(load) = 100pf
6. Measured by discharging a 100pf capacitor to each pin through a 1K ohm resistor.
7. TC/RC must be <43% of CLK when transmitting multiple buffers.



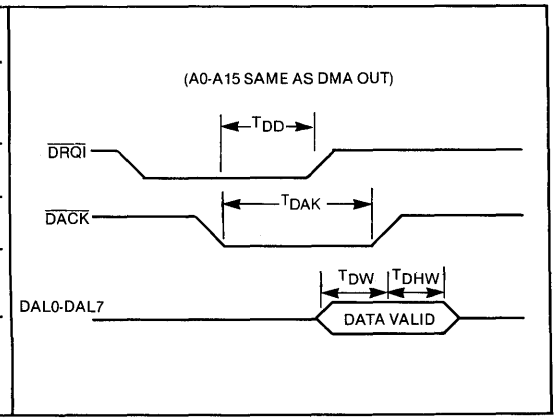
CPU READ ($\overline{CS}$ IS LOW)



CPU WRITE ($\overline{CS}$ IS LOW)



DMA OUT

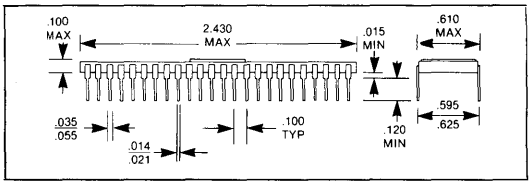


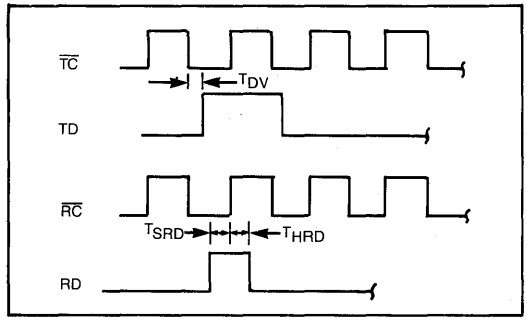
DMA IN

6.0 ORDERING INFORMATION

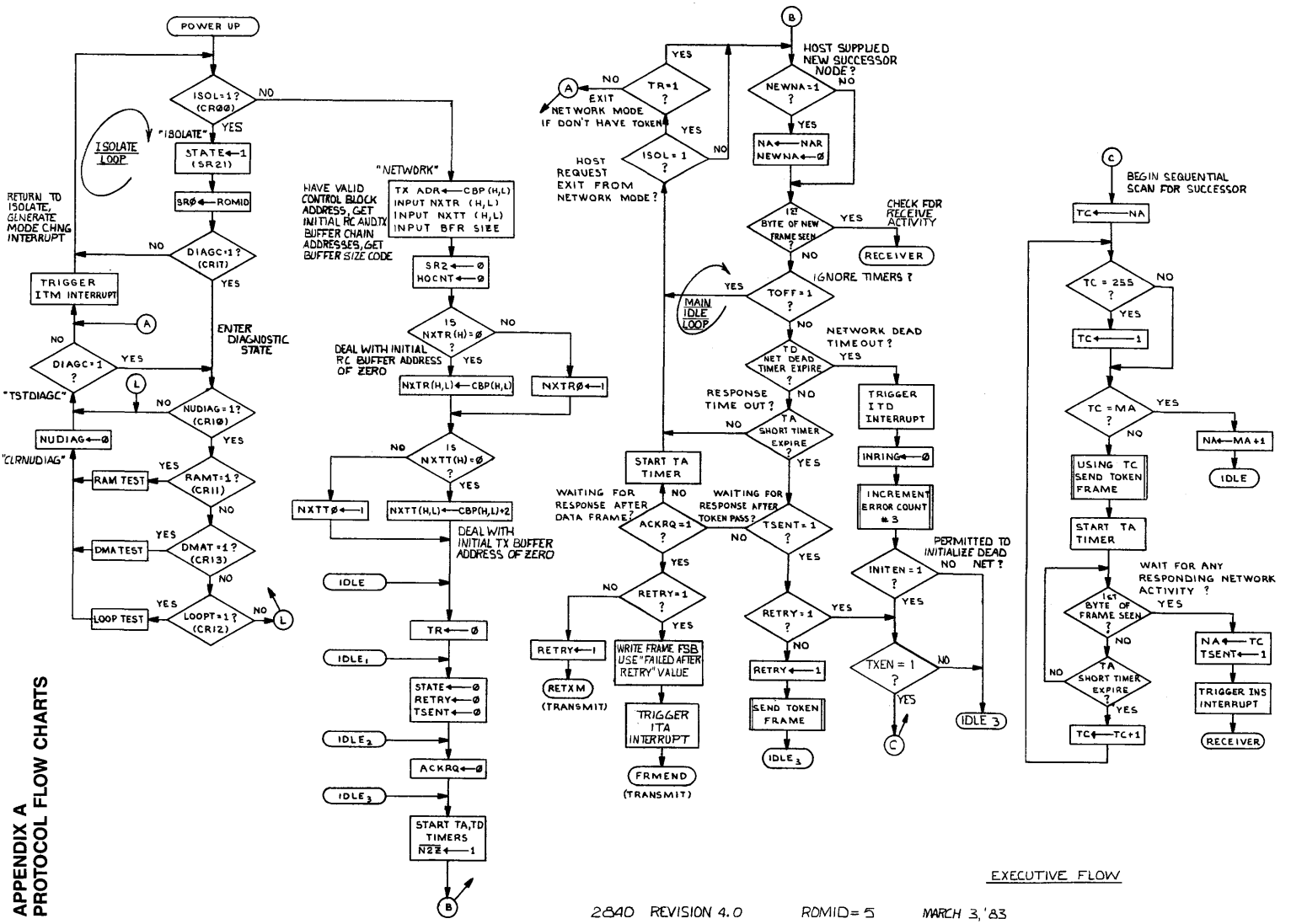
DEVICE NUMBER	MAXIMUM RATE
WD2840-01	100 Kbps
WD2840-05	500 Kbps
WD2840-11	1.0 Mbps

Package Diagram





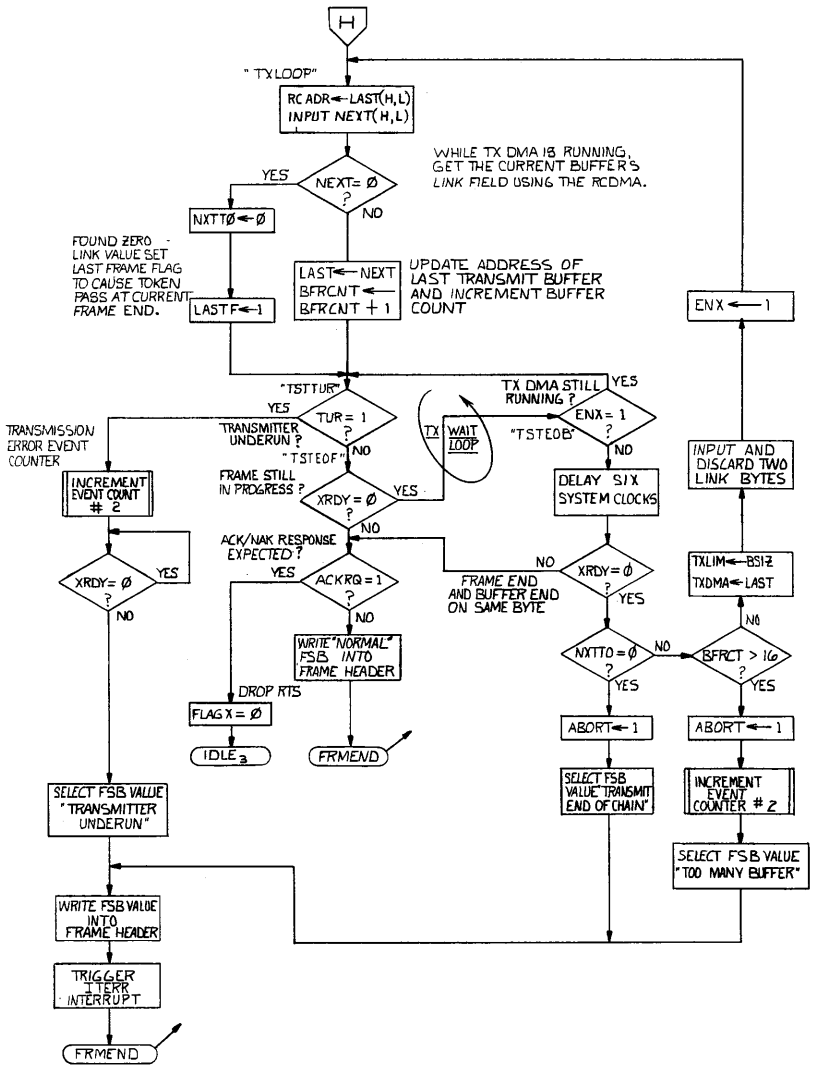
TD-RD TIMING

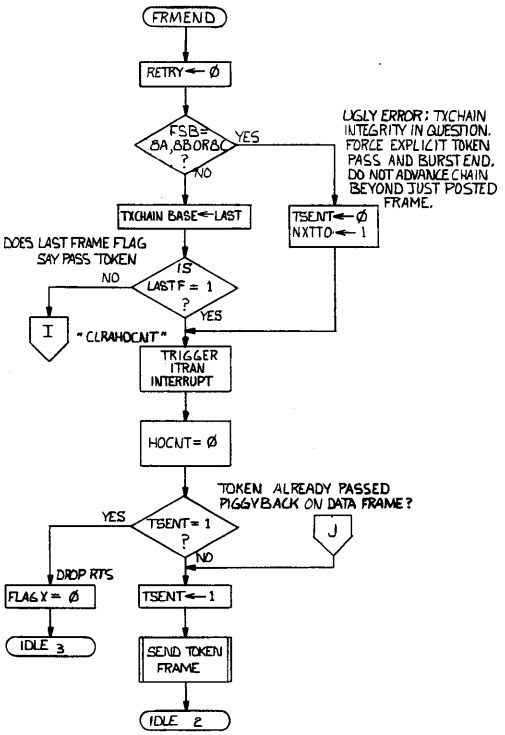


EXECUTIVE FLOW

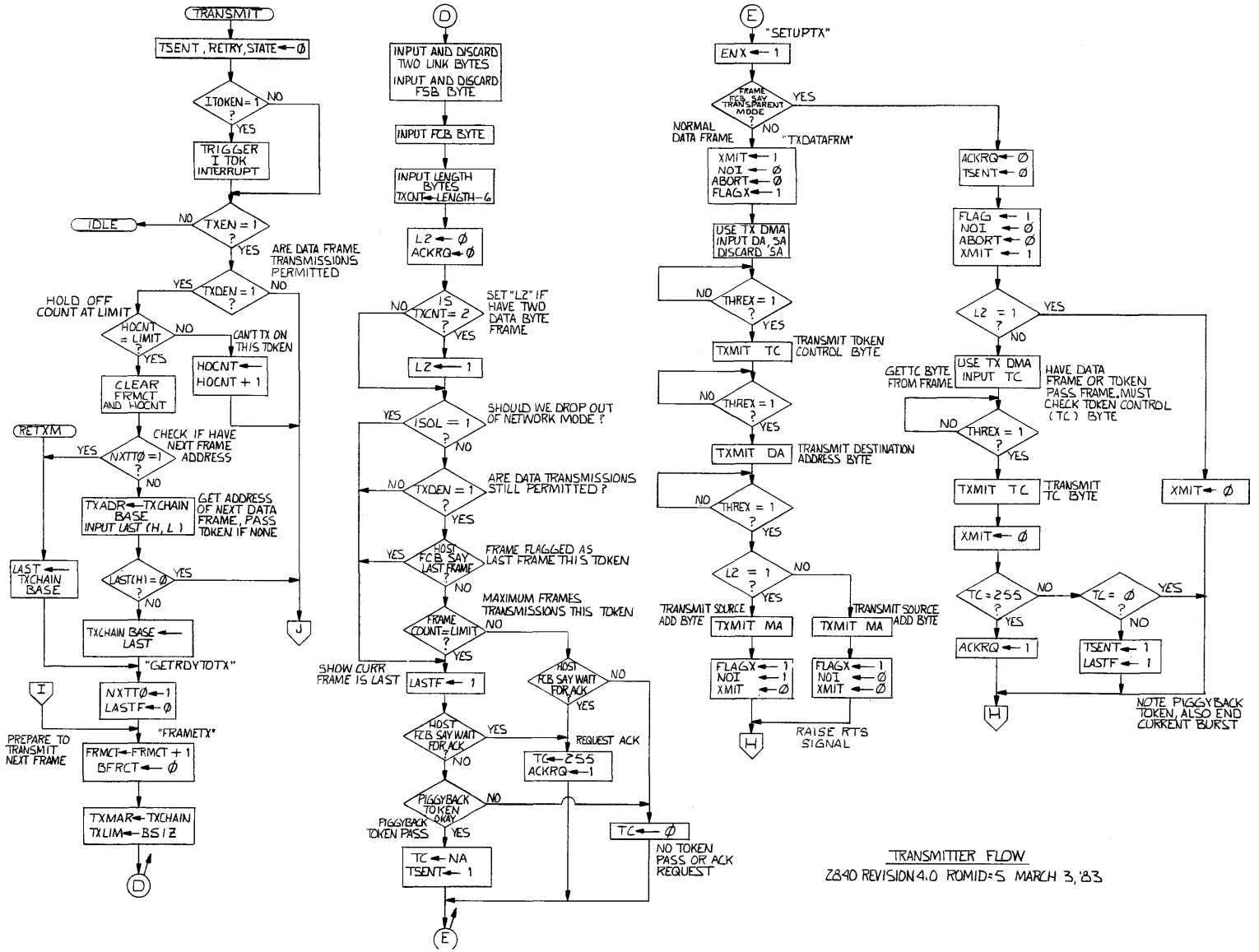
2840 REVISION 4.0 ROMID=5 MARCH 3,'83

APPENDIX A
PROTOCOL FLOW CHARTS



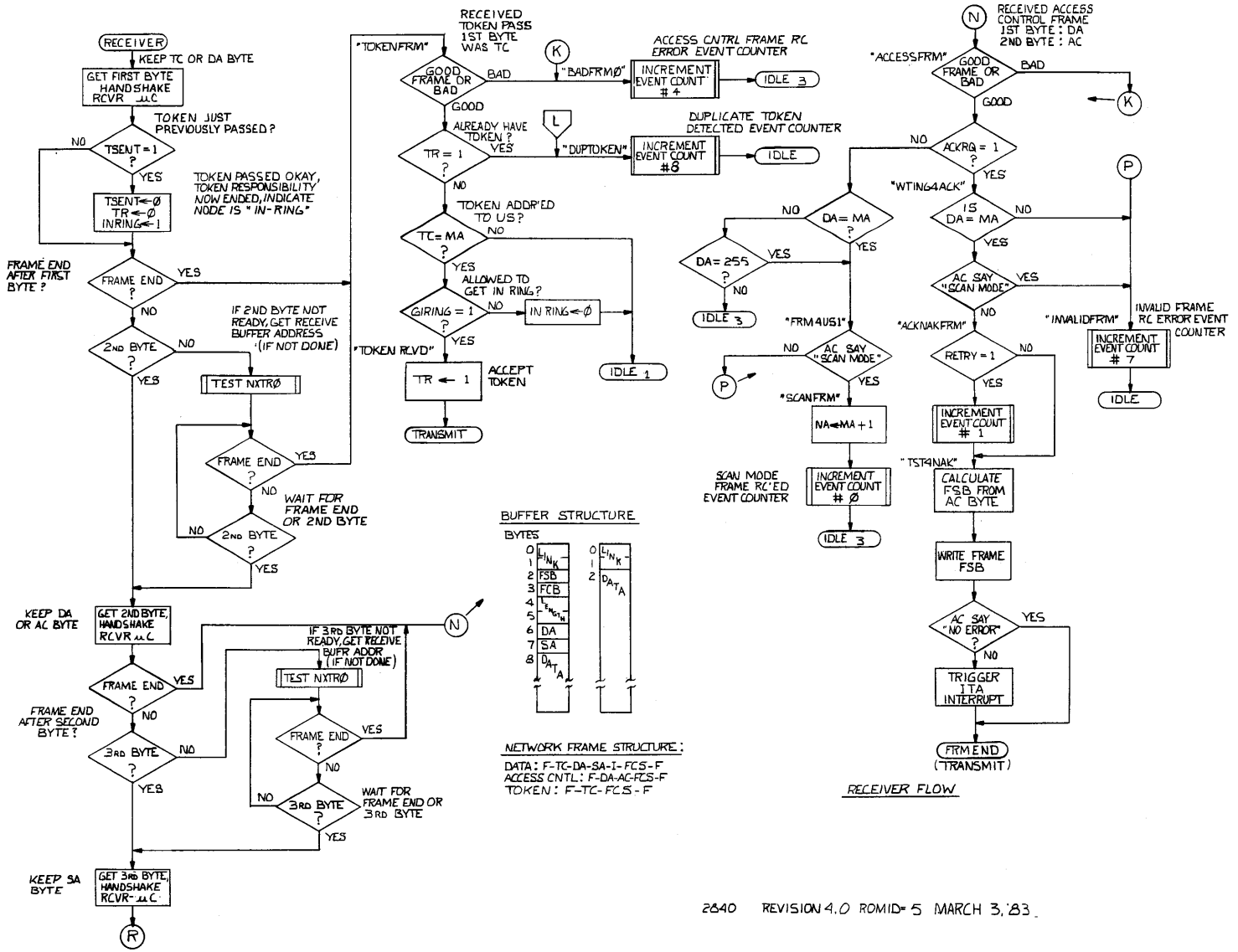


TRANSMITTER FLOW

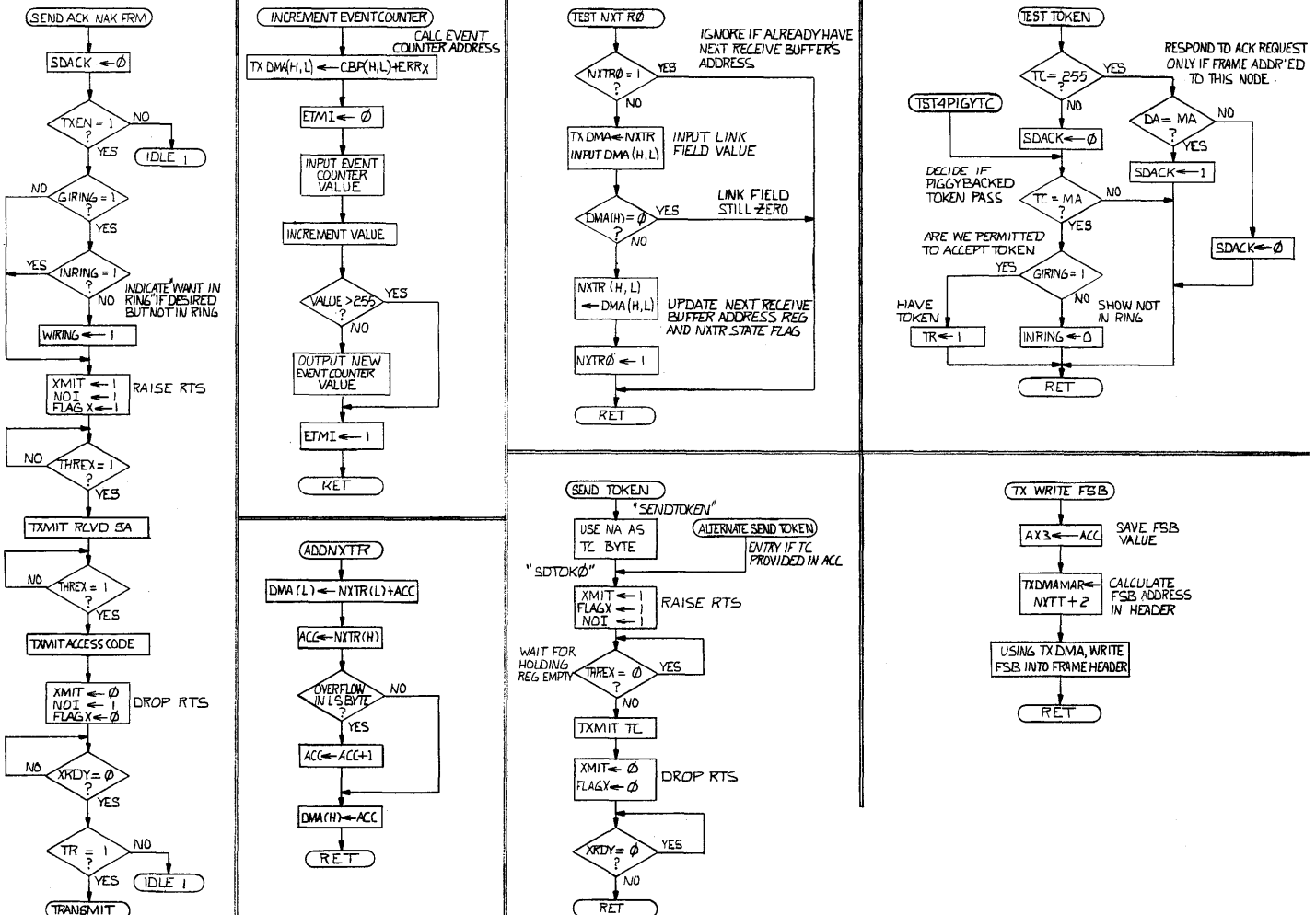


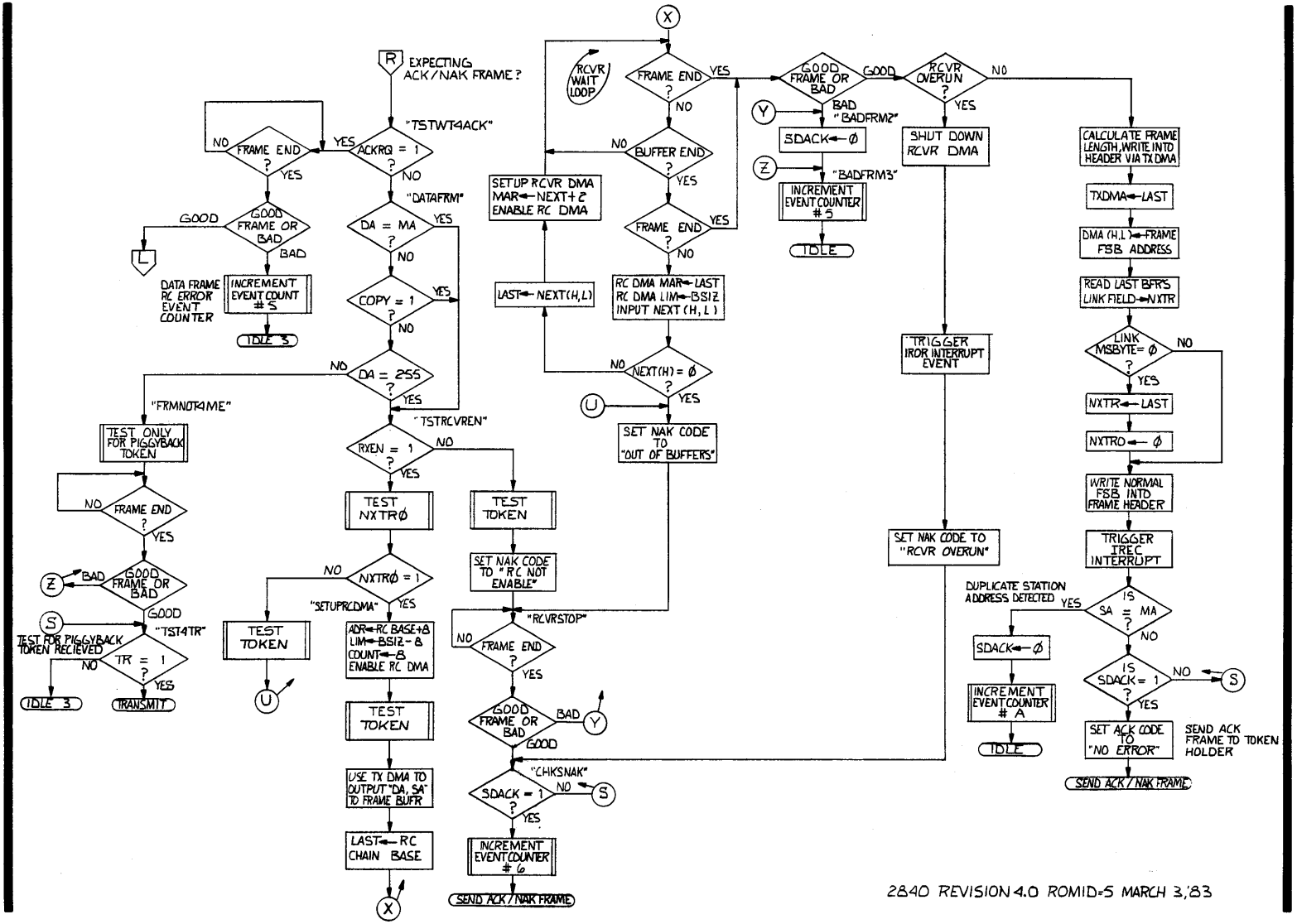
TRANSMITTER FLOW

Z840 REVISION 4.0 ROMID=5 MARCH 3, '83



2840 REVISION 4.0 ROMID= 5 MARCH 3, '83


SEND ACK NAK FRM
SDACK ← Ø
TXEN = 1 ?
NO
YES
IDLE 1
GIRING = 1 ?
NO
YES
INRING = 1 ?
YES
NO
INDICATE WANT IN RING IF DESIRED BUT NOT IN RING
WIRING ← 1
XMIT ← 1
NOI ← 1
FLAGX ← 1
RAISE RTS
THREX = 1 ?
NO
YES
TXMIT RCVD SA
THREX = 1 ?
NO
YES
TXMIT ACCESS CODE
XMIT ← Ø
NOI ← 1
FLAGX ← Ø
DROP RTS
XRDY = Ø ?
NO
YES
TR = 1 ?
NO
YES
IDLE 1
TRANSMIT
INCREMENT EVENT COUNTER
CALC EVENT COUNTER ADDRESS
TX DMA(H,L) ← CBP(H,L)+ERRX
ETMI ← Ø
INPUT EVENT COUNTER VALUE
INCREMENT VALUE
VALUE > 255 ?
YES
NO
OUTPUT NEW EVENT COUNTER VALUE
ETMI ← 1
RET
ADDNXTR
DMA(L) ← NXTR(L)+ACC
ACC ← NXTR(H)
OVERFLOW IN LS BYTE ?
NO
YES
ACC ← ACC+1
DMA(H) ← ACC
RET
TEST NXT RØ
IGNORE IF ALREADY HAVE NEXT RECEIVE BUFFER'S ADDRESS
NXTRØ = 1 ?
YES
NO
TX DMA ← NXTR
INPUT DMA(H,L)
INPUT LINK FIELD VALUE
DMA(H) = Ø ?
YES
NO
LINK FIELD STILL ZERO
NXTR(H,L) ← DMA(H,L)
UPDATE NEXT RECEIVE BUFFER ADDRESS REG AND NXTR STATE FLAG
NXTRØ ← 1
RET
SEND TOKEN
"SENDTOKEN"
USE NA AS TC BYTE
ALTERNATE SEND TOKEN
ENTRY IF TC PROVIDED IN ACC
"SDTOKØ"
XMIT ← 1
FLAGX ← 1
NOI ← 1
RAISE RTS
WAIT FOR HOLDING REG EMPTY
THREX = Ø ?
YES
NO
TXMIT TC
XMIT ← Ø
FLAGX ← Ø
DROP RTS
XRDY = Ø ?
YES
NO
RET
TEST TOKEN
TC = 255 ?
YES
NO
RESPOND TO ACK REQUEST ONLY IF FRAME ADDR'ED TO THIS NODE
TST4PIGYTC
DA = MA ?
NO
YES
SDACK ← Ø
SDACK ← 1
DECIDE IF PIGGYBACKED TOKEN PASS
TC = MA ?
NO
YES
ARE WE PERMITTED TO ACCEPT TOKEN
GIRING = 1 ?
YES
NO
SDACK ← Ø
HAVE TOKEN
SHOW NOT IN RING
TR ← 1
INRING ← Ø
RET
TX WRITE FSB
AX3 ← ACC
SAVE FSB VALUE
TXDMAMAR ← NXTT+2
CALCULATE FSB ADDRESS IN HEADER
USING TX DMA, WRITE FSB INTO FRAME HEADER
RET



2840 REVISION 4.0 ROMID=5 MARCH 3,'83

APPLICATION NOTE

WD2840 Application Note

INTERFACING THE WD2840 TO A VERSABUS SYSTEM USING A DUAL PORT MEMORY

This application note describes one possible method of interfacing the WD2840 Token Access Controller with a general purpose microprocessor based system. This is intended to be an example design only, no effort has been made to minimize the logic required to perform these functions as would be done in a production design. Rather, the design has been kept "clean" to promote readability.

This implementation is designed with a dual-port memory concept allowing its use in systems that either do not support DMA at all, as well as systems that are unable to guarantee reasonable DMA response to a request (Figure 1). Examples of these systems are low end personal computers that allow their disk controllers to "hog" the DMA channel for an entire sector transfer. Very high end systems are also candidates for the dual-port memory technique. Here, the system bus may be shared by multiple hosts and be of such extreme bandwidth that the internal WD2840 DMA controller may be inefficient.

In most applications, the WD2840, can simply self-DMA its data directly to/from the host system's working memory. In the applications described above, the WD2840 must DMA its messages to/from the network into a local RAM allowing the host to access it at its leisure.

REFERENCES

- WD2840 Token Access Controller Specification, Western Digital Corporation, 1983.
- "Token Passing Cashes in with Controller Chip" Electronic Design, October 14, 1982.
- Versabus Technical Reference Manual Motorola,
- RS-422 Technical Specification

This design is described in six sections:

- Host dependent logic, here designed for the Motorola Versabus system, including all required bus interface drivers and timing.
- Local two-port buffer memory which is shared by the host and the WD2840.
- Arbitration logic to fairly share the buffer memory, especially when both the host and WD2840 demand access at the same time.
- WD2840 Token Access Controller and associated timing
- Media interface consisting of a manchester encoder/decoder and liner drivers
- Generalized initialization flowchart

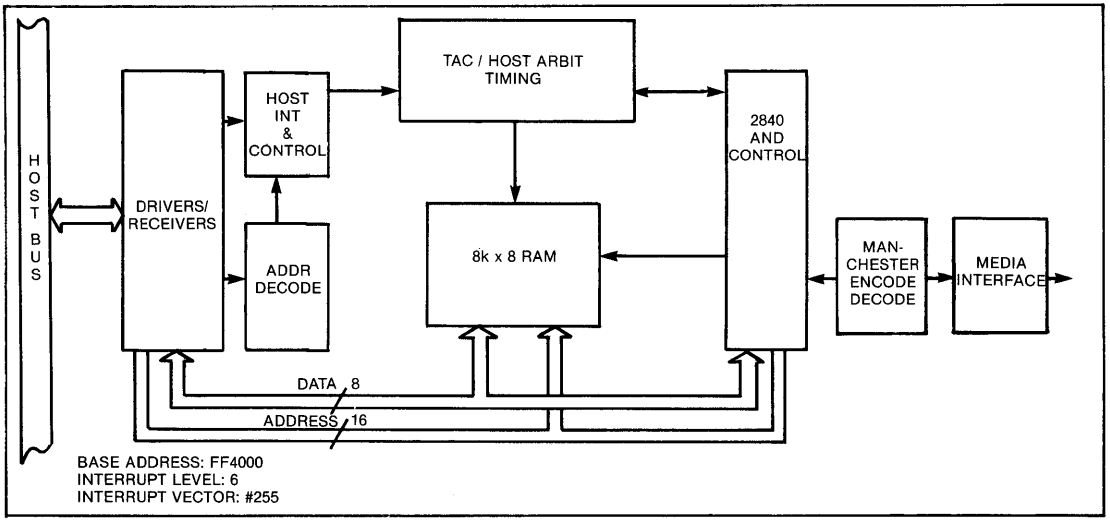


Figure 1. Versabus Application of WD2840 Using Dual Port Memory

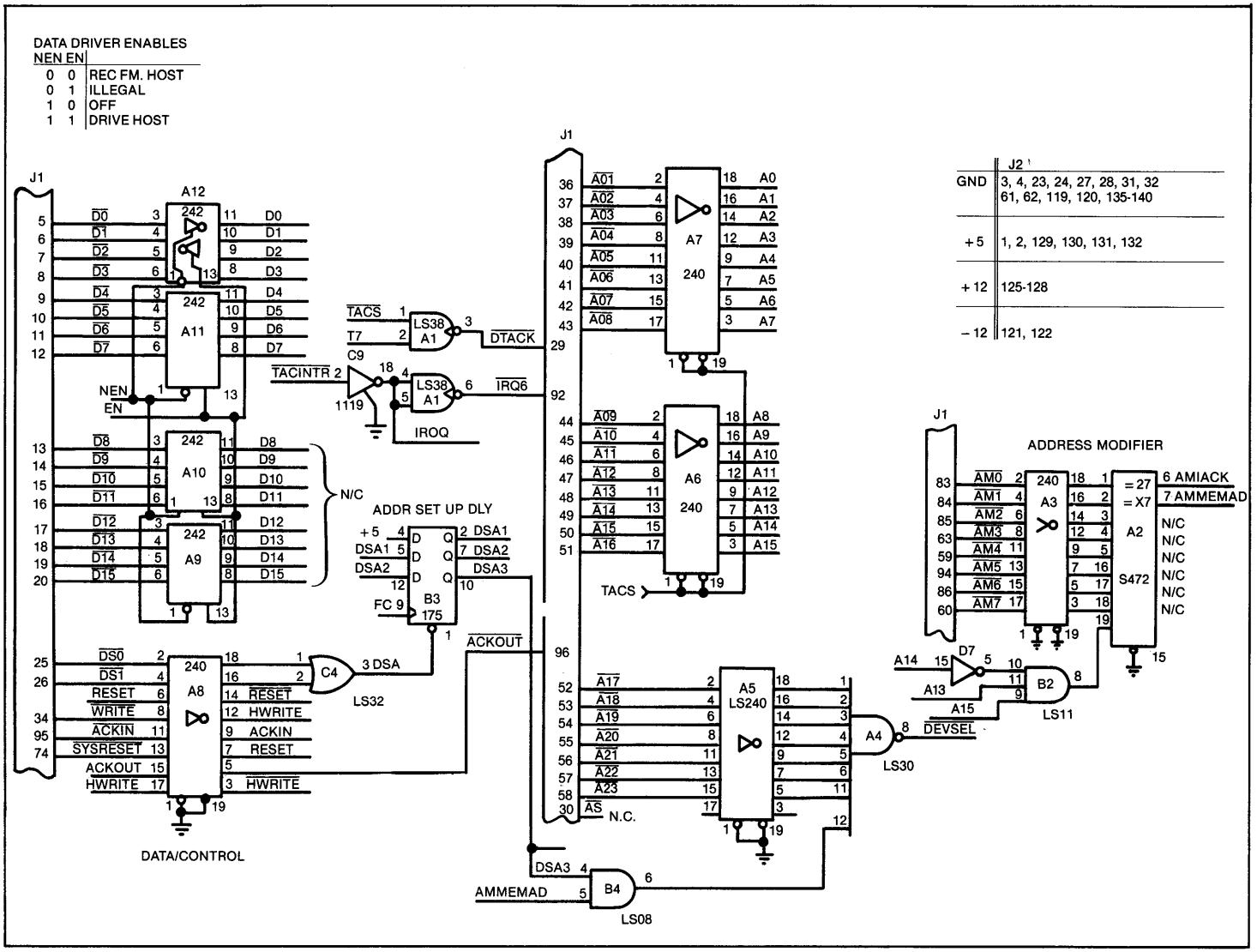


Figure 2. Host Interface

HOST INTERFACE

The host interface (Figure 2) utilizes common three-state bus drivers buffering the Versabus from the internal data bus. They are enabled low-Z onto the host bus whenever the host "reads" from the local memory (or WD2840 registers) and are enabled to drive the internal bus whenever the host writes to the internal memory (or registers). All other times these are hi-Z allowing other modules on the Versabus side to use that bus, as well as allowing the WD2840 to use the internal bus. Only an eight bit internal data bus is used mapping all host memory accesses into the lower byte. (Bus drivers A10 and A11 are not used)

Sixteen address bits are buffered and driven onto the internal address bus when the host has access to the RAMs (otherwise the WD2840 drives the internal address bus). The additional address lines of the Versabus are "anded" with the I/O Data Strobe signals DS0 and DS1 and address modifier bits creating a device select signal (DEVSEL) when all are active simultaneously indicating the host actually wants to access this module.

The Host Interrupt and Driver control logic (Figure 3) supplies the host interrupt vector (0FFH) when acknowledged (C10). Acknowledgement occurs when the Versabus ACKIN is received in conjunction with the proper priority level (set at 4 in this design), the proper address modifier (AMIACK), a short deskew delay (DSA3), and a signal indicating an interrupt was indeed generated by this module (IROQ).

The logic on this sheet also controls the direction of the data buffers previously described (with signals EN and NEN), presuming the host has active control of the local bus (HOST = 1). The host requests control of the bus for access to the on-board RAM and during interrupt acknowledgement.

CLOCK/ARBITRATION

This logic (Figure 4) generates the synchronous timing used in the rest of the sections. A 16MHz signal derived from a crystal oscillator (part of the manchester logic, described later) is buffered (by C9 and then called FC). This high speed clock is also divided down for the WD2840 system clock CLK at 2 MHz (other slower rates are not used in this design).

This high speed clock clocks a simple latch (B7) until either the host or the WD2840 request local bus access. If the host desires access to this module, HOST is made true, the on-board WD2840 DMA request generated TACDRQ. When either (or both) of these signals occur, IDLE goes false (B5 pin4) freezing the state of latch B7.

IDLE going false starts the timing chain (B1, C1) that generates general timing pulses used later.

When the local memory sequence is complete, at time T10 for the TAC (B8 pin 6) or at time T7 for the

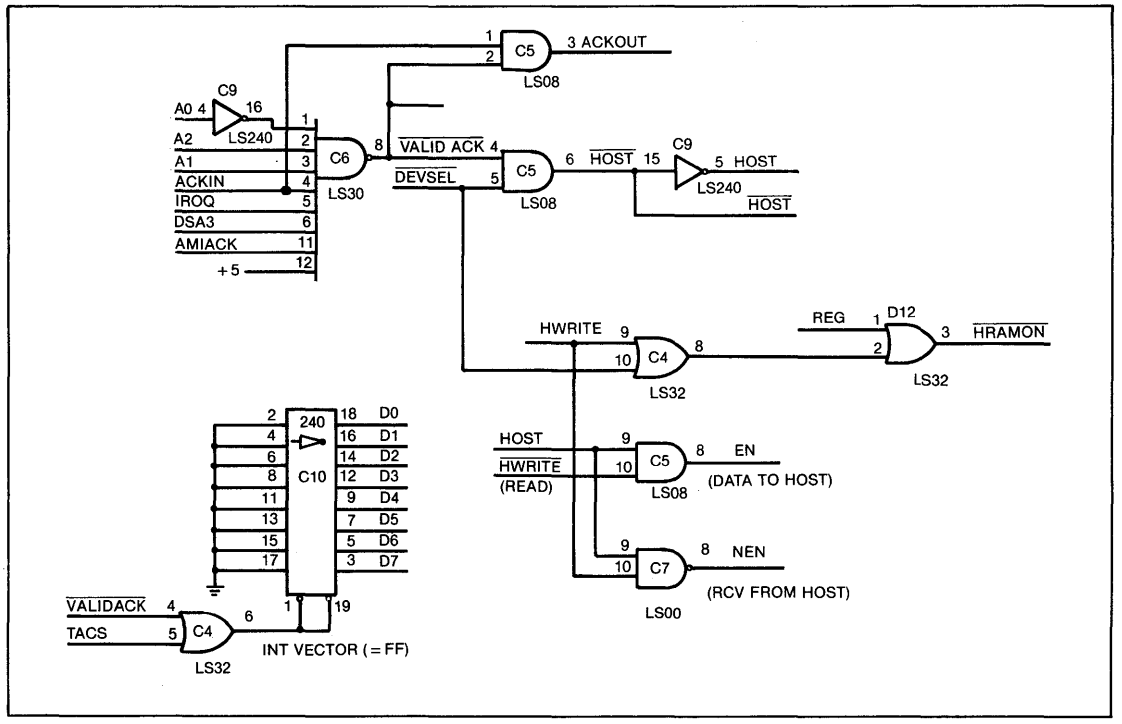


Figure 3. Host Interrupt and Driver Control

host (B2 pin 6) a special end of cycle delay is initiated (via shift register E7). This delay ensures that at least 500ns is maintained between WD2840 DMAs and possible host I/O accesses. At the end of this delay, flip-flop B6 generates a one clock "DONE" pulse resetting the arbitration logic.

MEMORY ARRAY

The memory (Figure 5) uses simple static memories configured as 8K by 8 bits. The RAM data lines are buffered onto the local data bus due to loading considerations. The RAM array is enabled during all I/O operations except those to the first sixteen locations, which are used for accessing the sixteen internal WD2840 registers (REG).

WD2840 SUPPORT

The WD2840 interface logic is given in Figure 6. The system clock (CLK) is derived from the timing generator (Figure 4). (This clock may be asynchronous with the transmit and receive data clocks if desired.) Address latches are used in this design to provide additional signal drive and to improve memory access timing (the WD2840 does have internal address latches that are useful in less stringent applications).

Host Write (HWRITE) is used to control the direction of I/O operations with the WD2840. When true, the WD2840 expects its internal registers to be written into. This occurs when both WE (pin 3) and CS (pin 4) are both low. Gate C7 1,2,3 ensures that the WE* signal goes false prior to the data changing (ensures hold time). Chip select logic (D10, 1,2,13,12) enables reads or writes only when the host has access to the internal bus, the internal address bus holds a value in the range of 0-15 (REG true), and a short set-up timer has expired (T1).

Gate F10 (11,12,13) "ands" the WD2840s DMA input and output requests and presents them to the arbitration logic described earlier (via TACDRQ). The sense of the WD2840 DMA request (input or output) is latched (with E10). The DMA output signal is delayed for RAM setup (T2) and turned off before the data is removed to meet RAM hold timing (T7) and presented to the RAM control logic to generate the write pulse.

MANCHESTER ENCODER/DECODER

The manchester encoder/decoder used here is a Harris HD-6409 (Figure 7). This device is ideal for use with the WD2840 in that its "invalid manchester output," that detects missing clocks, etc., can be directly connected to the WD2840's SQ input. A 16 Mhz crystal controls the internal digital phase locked loop used for clock recovery and generated the 16 Mhz master clock (FC) used for general timing in this design.

The "modem" consists of a simple RS-422 balanced driver and receiver. More elaborate media interfaces are possible, including FSK and broadband, depending on speed / distance / number of taps / cost requirements.

INITIALIZATION

Figure 10 "flow chart" gives a generalized method of initializing a WD2840 based communications subsystem. First the WD2840 internal diagnostic are preferred, followed by loading of station parameters. Next the network is tested for activity and potential duplicate addresses. Finally the WD2840 TXEN is set allowing normal network generation. The Host now simply monitors TX and RX chains to sent/receive network data.

SUMMARY

This application note details a simple WD2840 subsystem designed around the VERSAbus form factor. The on-board RAM makes removes any DMA/host bus access questions from the system design. A very simple line driver allows a number of these modules to communicate at speeds of 1 Mbps.

Note that this application note is intended for illustration only; simpler and more elaborate interfaces are possible.

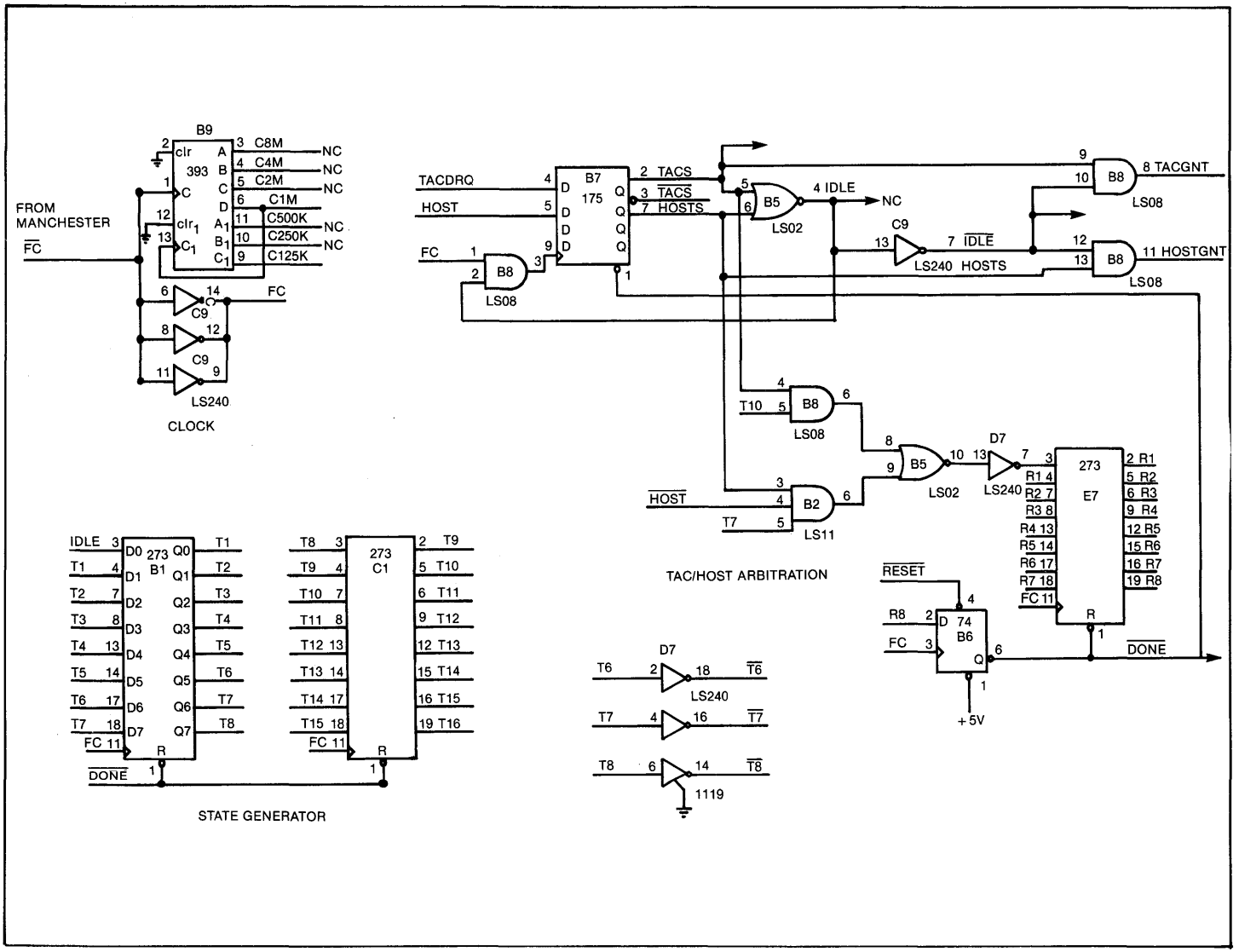


Figure 4. Clock and Arbitration

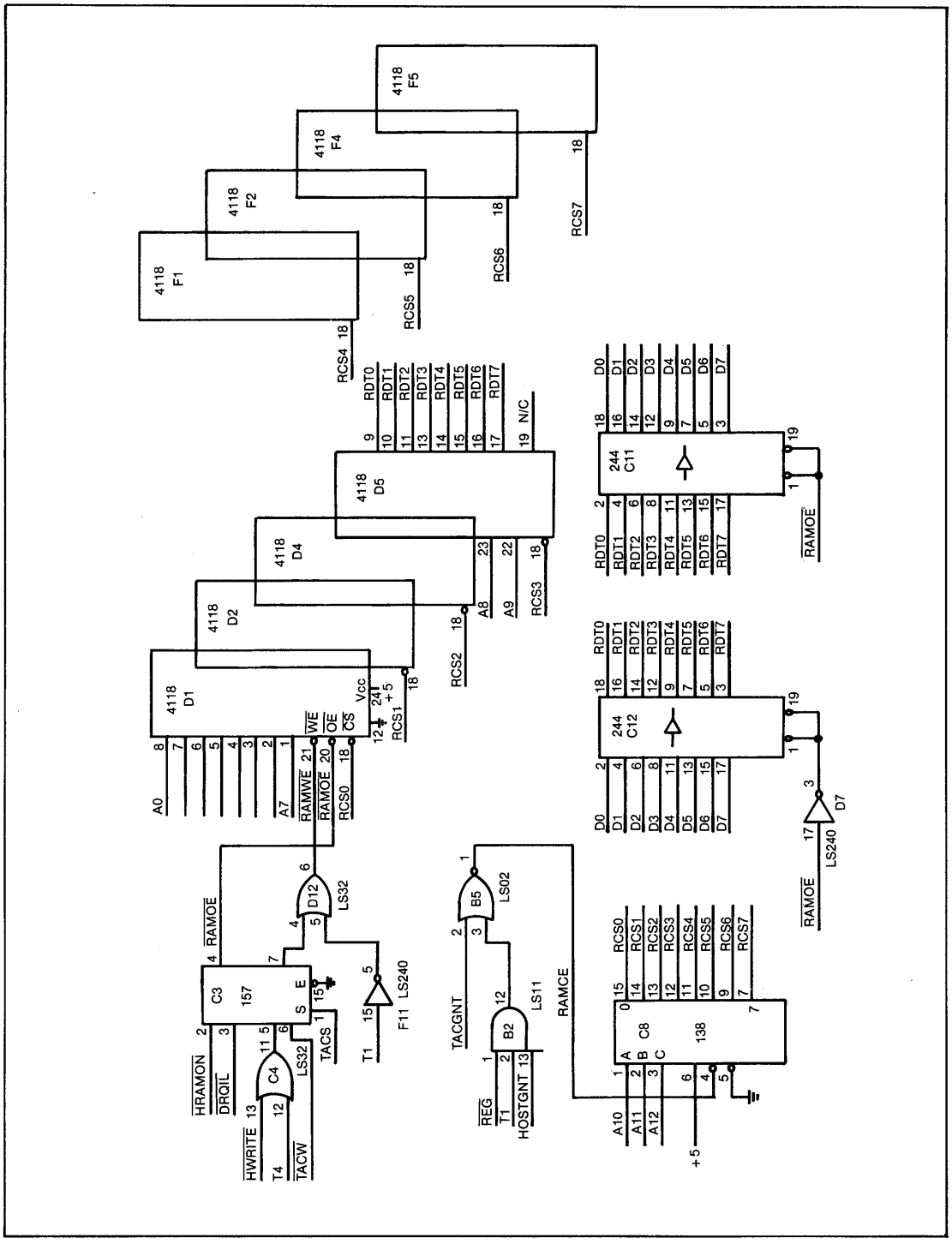


Figure 5. Memory Array

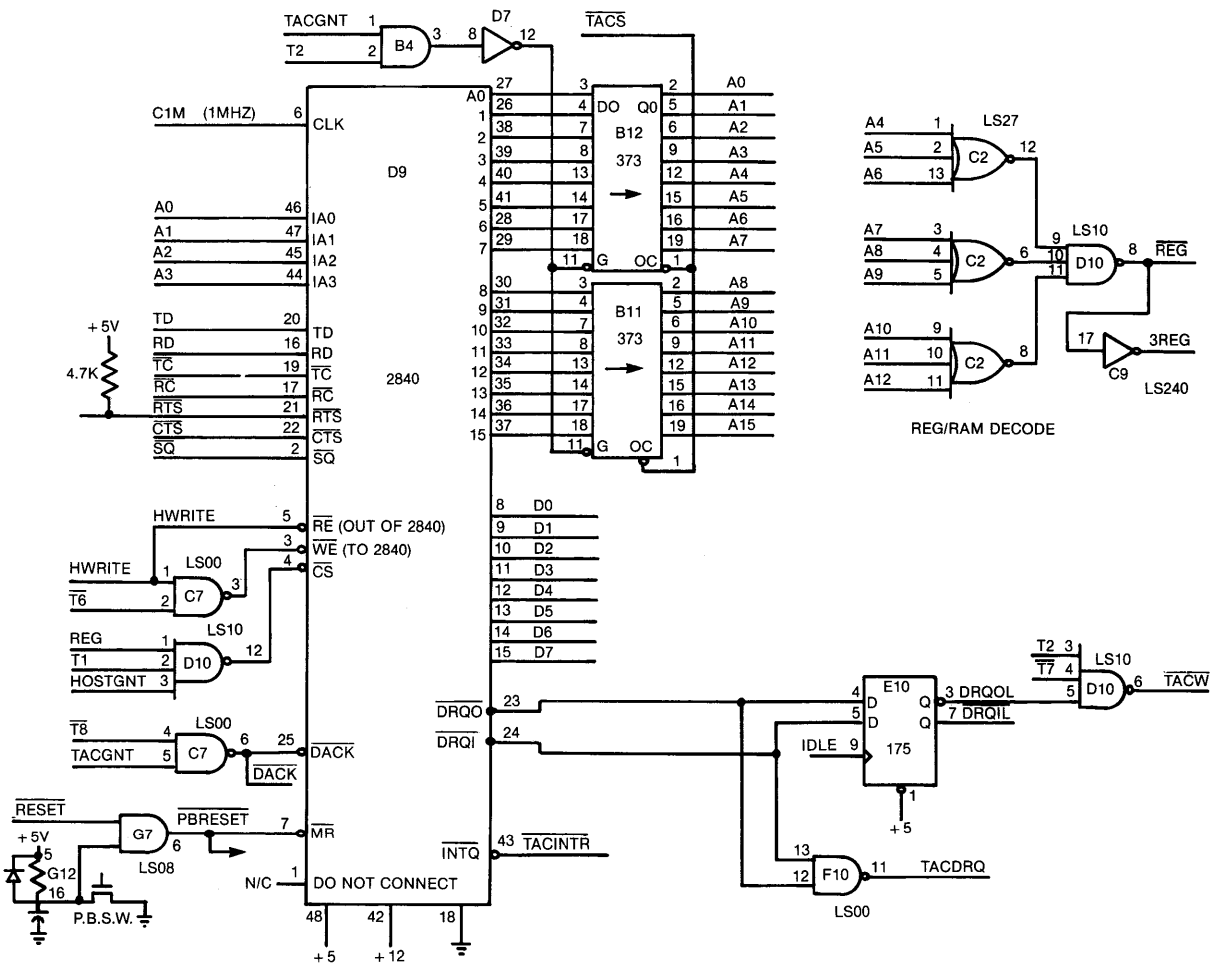


Figure 6. WD2840 Support

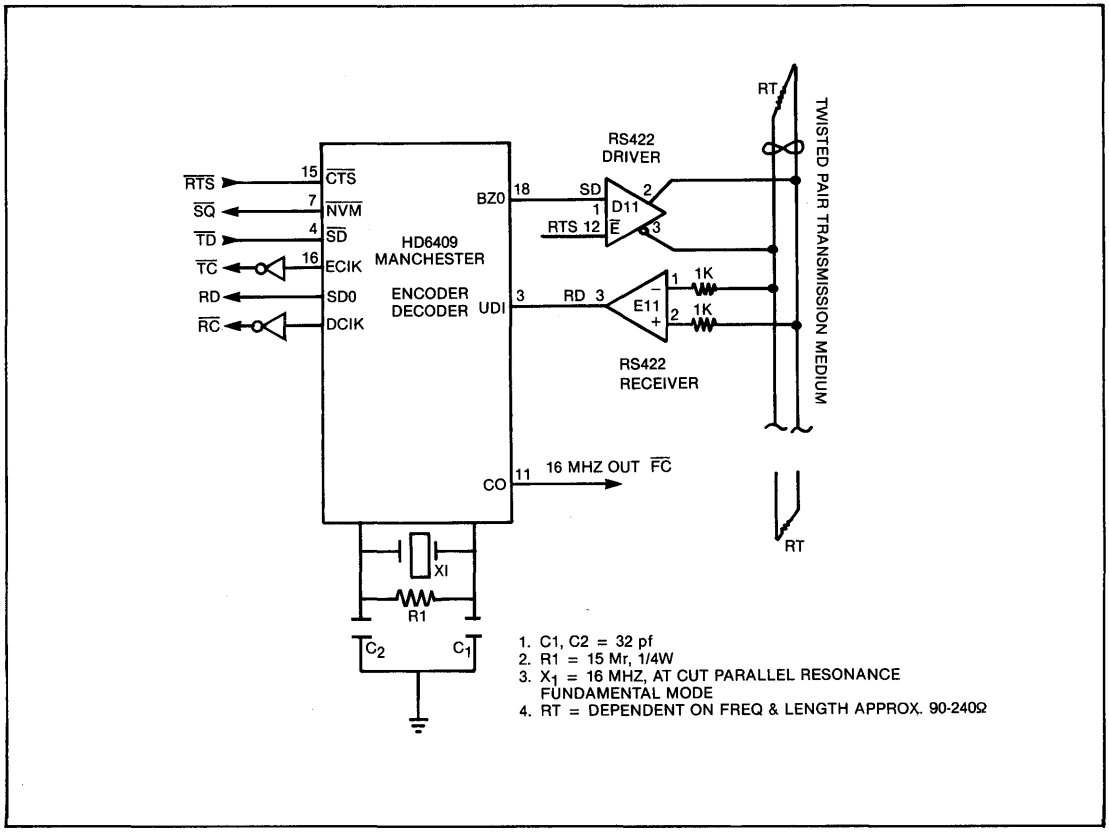


Figure 7. Manchester Encoder/Driver

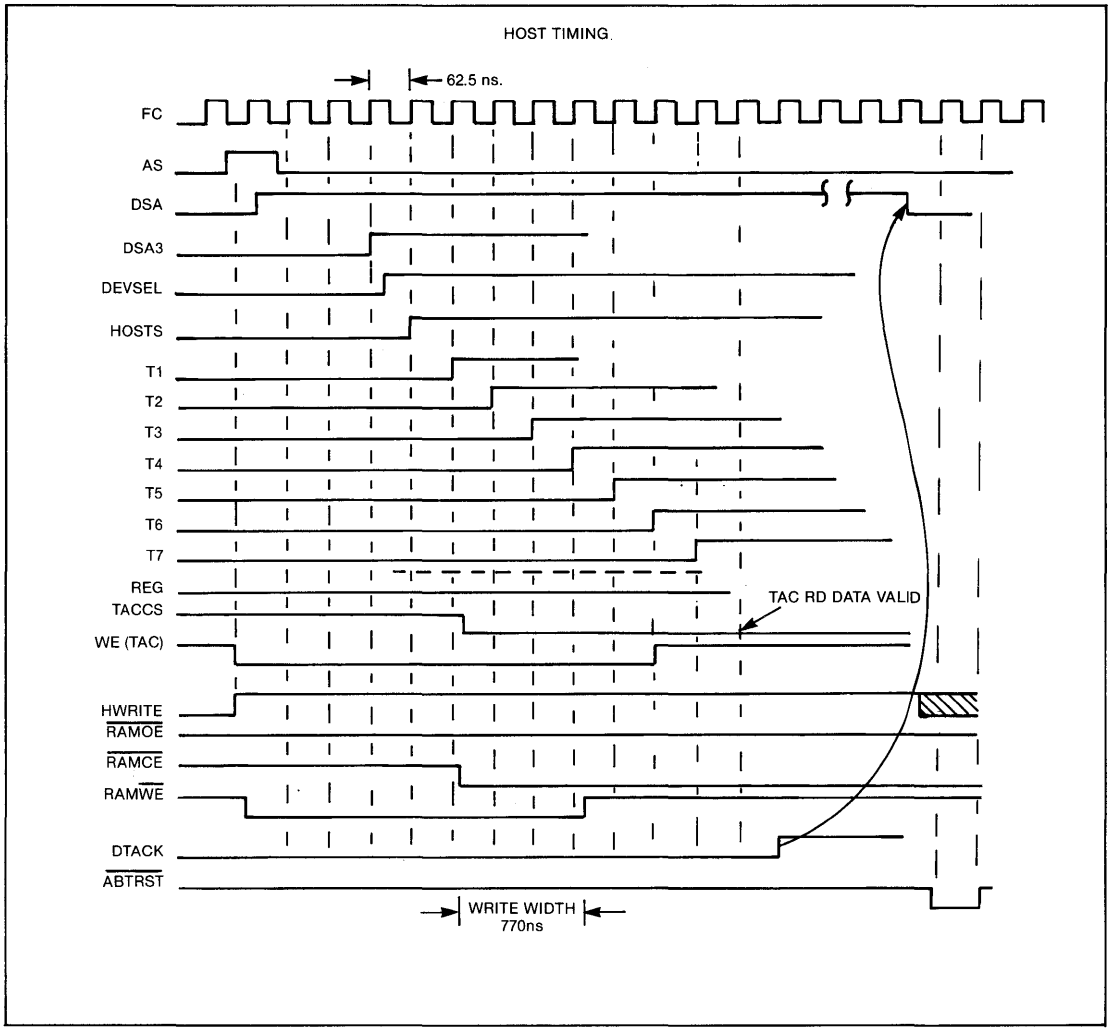


Figure 8. Host Timing

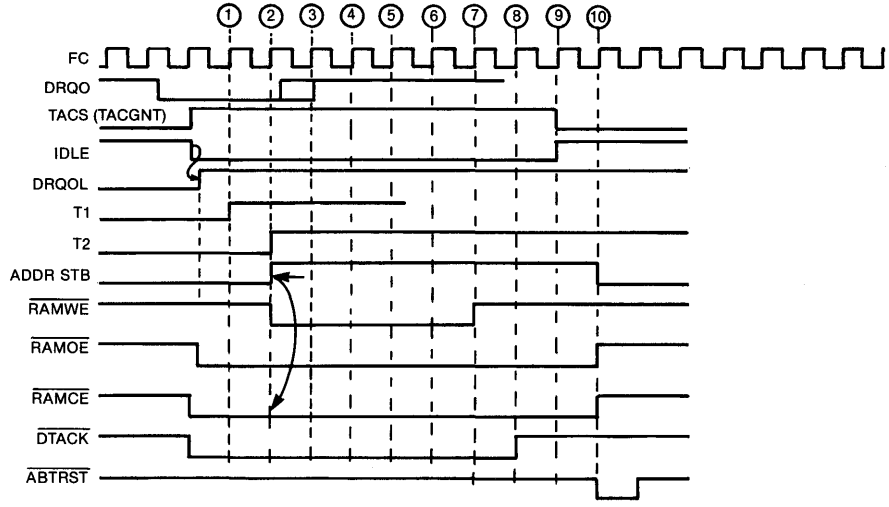


Figure 9. TAC Timing

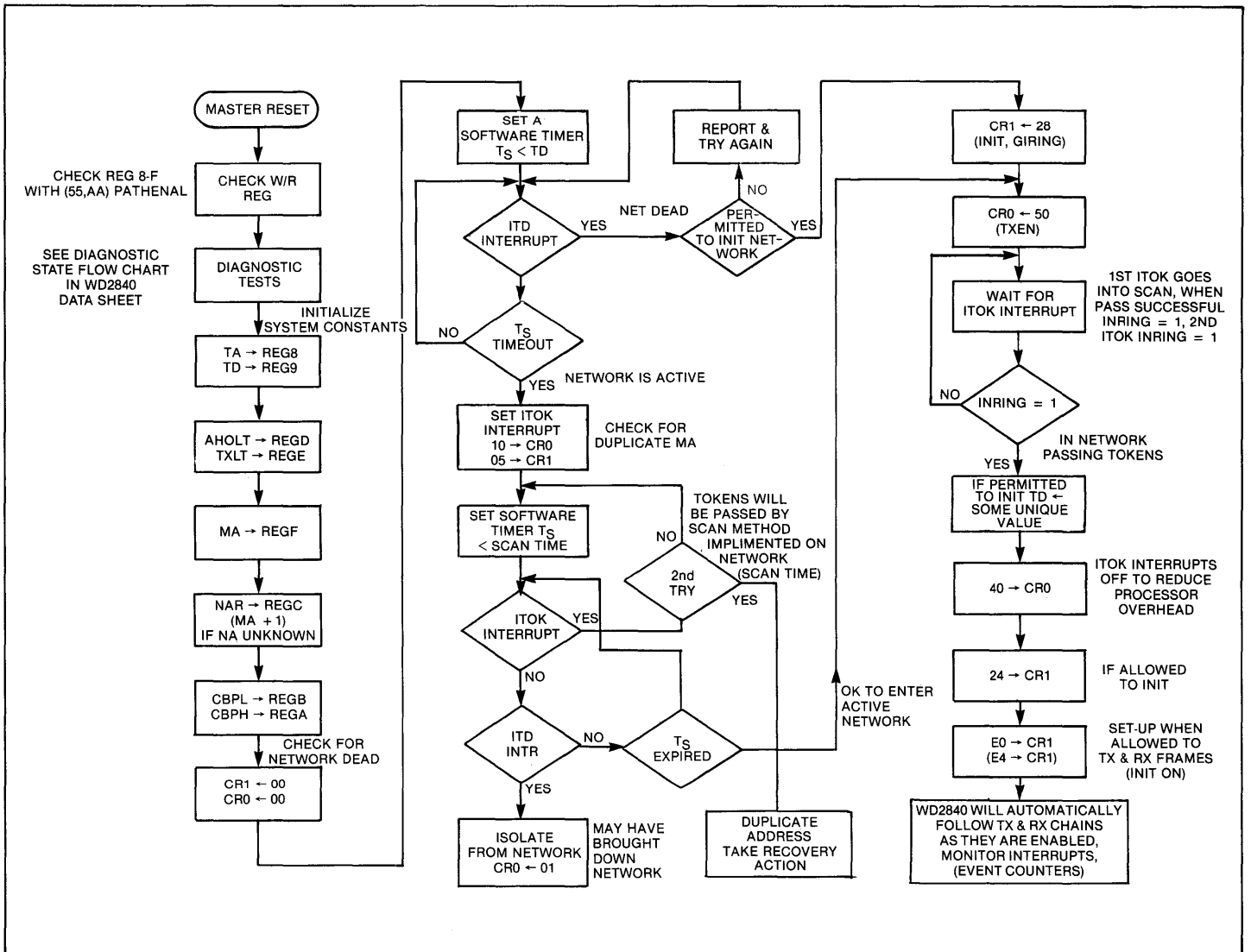
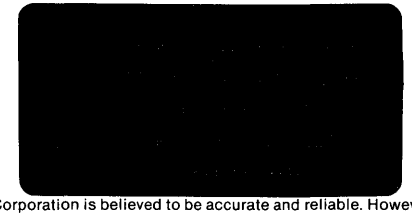


Figure 10. Typical Set-Up Sequence For WD2840



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