WESTERN DIGITAL CORPORATION

WD33C93A

DATA SHEET AND APPLICATION NOTES

WESTERN DIGITAL CORPORATION

NOVEMBER, 1990

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PRODUCT: **WD33C93A**

Sept 15, 1990
Number **071-A**

WD33C93A Application Note List

Number	*Affected*	*Description*
E062-B	WD33C93_/A/B	**Version Differences:** All changes, additions, deletions, and part numbers for each of the released versions of the WD33C93 SCSI Bus Interface Controller (SBIC) chip.
E031-A	WD33C93A	**Data Sheet:** Contains the data sheet for the WD33C93A SCSI Bus Interface Controller (SBIC) chip.
E025-A	WD33C93_/A	**Conversion to the A version:** List of design considerations for converting to the WD33C93A from the non-A version.
E018-A	WD33C93A	**Bug List:** All known problems in the WD33C93A.
E022-A	WD33C93A	**DRQ Bug, Rev C,D only:** The DRQ signal may erroneously deassert for a short time under some conditions
E024-A	WD33C93_/A	**DRQ/DACK in Polled I/O mode:** During polled I/O mode, these lines should be held to a false state.
E033-A	WD33C9x	**SCSI system design issues concerning bus noise:** A paper on the sources of noise on the SCSI bus and what to do about them.
E039-A	WD33C93_/A	**ACK assertion timing:** ACK\ may be deasserted prior to REQ\
E040-A	WD33C92/93_/A	**Parity Errors during Select-and-Transfer:** A parity error may be masked by other interrupt conditions.
E042-A	WD33C92/3_/A	**Synchronous/Asynchronous Transfers:** Descriptions and issues concerning SBIC chip transfers.

E043-A	WD33C93A	**Auxiliary Status Register Notes:** Msc notes on use and function of the Auxiliary Status register of the SBIC chip.
E044-A	WD33C92/93_/A	**Aborting a Wait-for-Select-and-Transfer:** How to do it...
E045-A	WD33C92/93_/A	**Address Translation Times:**
E046-A	WD33C92/93_/A	**Unexpected Disconnect affects transfer count:** Internal and external transfer counts may differ in this circumstance.
E047-A	WD33C92/93_/A	**Select-and-Transfer command flow chart:**
E048-A	WD33C92/93_/A	**Target Mode Vendor Unique CDBs:** How the SBIC chip handles various sizes of Command Descriptor Blocks.
E049-A	WD33C92/93_/A	**ALE Timing requirements:** Maximum time length specification.
E050-A	WD33C92/93_/A	**Initiator Mode Vendor Unique CDBs:** How the SBIC chip handles various sizes of Command Descriptor Blocks.
E051-A	WD33C92/93_/A	**Target Mode- Delay of ATN Interrupt:** Timing irregularity.
E065-A	WD33C92/93-all	**Host Transfer modes:** Descriptions of the 4 modes of data transfer between the SBIC chip and the host.
E066-A	WD33C93A	**Command/Interrupt Guide:** A matrix of interrupts and commands for the WD33C93A.
E067-A	WD33C93A	**SCSI Status Register:** Description of logic orientation of SCSI phase bits in the status register.

E029-A	All	**WD Sales Offices by Region:** List of WD world wide sales offices listed by region of responsibility.
E030-A	All	**North American Distributors and Resellers:** List of all distributors in North America by state/province, list of all resellers.
E032-A	all	**Decoding WD LSI part numbers:** Top/bottom side part number branding explained for LSI parts.
E070-A	All	**Reserved Register Bits:** Default programming of these bits should always be with a value of zero (0).

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PRODUCT: Model #: **WD33C93_/A/B**
Manf #: 3393, 4393, 5393, 7393

August 17, 1990
Number **E062-B**

WD33C93 Version Differences

Current Sales: WD33C93A rev F
Future Sales: WD33C93B Samples in 10/90, Production Quantity in 1/91
Note: This part will be sold in addition to the WD33C93A

WD33C93B (differences from WD33C93A)
The WD33C93B is functional and performance improvement over the WD33C93A. The additions to the WD33C93B are for SCSI 2 support and for improved system performance. The B part is completely backwards compatible with the A part and may replace it in most applications with no hardware or firmware modifications (see note for #5). Some minor changes are required to make use of the additional functions of the B part.

1. **Addition: Fast SCSI-** The WD33C93B supports fast SCSI transfer rates of up to 10MB/s. Bit 7 of the Synchronous Transfer register enables fast SCSI transfers. Clock frequencies of between 16 and 20Mhz are required for this mode.

2. **Addition: Tag Message Support-**
   a) Message Type: Bits 3,4 in the Destination ID register now indicate the type of tagged message sent or received:

   0 0 No Message
   0 1 Simple Queue tag
   1 0 Head of Queue tag
   1 1 Ordered Queue tag

   b) Queue Tag: A Queue Tag register has been added to hold the value of the second byte of the tag messages associated with the Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands

3. **Addition: FIFO Status Bit-** Bit 3 of the Auxiliary Status register (FFE) now indicates FIFO full or empty depending on the direction of transfer. The bit indicates FIFO empty (FFE=1) when the µp is transferring data into the 12 byte FIFO. The bit indicates FIFO full when the µp is reading from the FIFO. These enable the µp to transfer up to 12 bytes with-

out the need to poll the DBR output prior to each transfer.

4. **Addition: Reselection Information:** Bit 5 of the Target LUN register now indicates what type of information is in the lower bits of the Target LUN register:
   0 Logical Unit Number
   1 Target Routine Number

5. **Addition: Increased Target Mode Fault SCSI Bus Tolerance-** The following features affect only the Target mode of operation. They are enabled by the RAF bit (formerly the EIH bit) in the Own ID register. Applications which use this bit with the WD33C93A will have to modify F/W accordingly:

   a) Transfer Error Detection: When enabled, the WD33C93B will abort a Send or Receive command with a 25h interrupt if it detects a possible transfer corruption caused by noise on the REQ and ACK signals.

   b) Unexpected Bus Free Detection (new to Target mode, already exists in Initiator mode): When enabled, the WD33C93B will generate either a 85h or 41h interrupt in the event of unexpected disconnection. This is intended to catch noise on the SEL line which causes the device to erroneously disconnect from the SCSI bus.

   Note: If applications made use of the EIH bit in the WD33C93A, the F/W will have to be modified to either disable the bit or accommodate the additional types of interrupts.

6. **WD33C93B Number Reference:**

Model #	Manf #	Description
WD33C93B PL 00 02	7393KB11PL	40 pin Plastic DIP
WD33C93B JM 00 02	7393KB11JM	44 pin PLCC

WD33C93A (differences from WD33C93)

1. **H/W Addition: Faster Transfer Rate-**
   a) The WD33C93A can now transfer data at up to 5MB/s.

   b) A burst DMA mode on the µp side has been added to help accommodate higher data bandwidths. Bit 5 of the Control register has been added to enable the DMA burst mode.

   c) The maximum clock frequency has been increased to 20Mhz

   d) Selectable dividers controlled by bits 7,6 in the Own ID register have been added to manage transfer rate and arbitration timing.

2. **H/W Addition: Host Parity-** The PLCC version of the WD33C93A now supports host parity generating and checking.
   a) Bit 5 (EHP) of the Own ID register has been added to enable the Host Parity feature.
   b) Bit 4 (HHP) of the Control register has been added to enable Halt on Host Parity error.
   c) Pin 11 of the PLCC is the µp data parity pin. This pin was "Test" and was not used under normal operations.

3. **H/W Addition: Extended FIFO-** The WD33C93A internal data FIFO has been expanded to 12 bytes from 5 bytes for the WD33C93. Bit 3 has been added to the offset counter in the Synchronous Transfer register to accommodate the increased FIFO size.

4. **H/W Change: Faster Execution Times-** The command decode and algorithms of many commands have been modified to greatly reduce controller overhead in both Target and Initiator modes.

5. **Cmd Addition: Send-Status-and-Command-Complete (0Dh) -** This target mode command has been added to the WD33C93A. This command first sends the status byte, as specified in the CDB byte 11. This command will send a linked command complete message. Linked command complete with flag is sent when bit 1 of CDB 12 is set. The command will also chain to the command fetch portion of WAIT-for-Select-and-receive.

6. **Cmd Addition: Send-Disconnect-Message (0E) -** This target mode command is used to disconnect from the SCSI bus when the target expects to seek, find the first block, deal with long tape operations, fill a buffer, etc.. The command sends the disconnect message, followed by a disconnect from the bus. If the IDI bit is set to one, a Save-Data-Pointer message is sent prior to the disconnect message.

7. **Cmd Addition: Set IDI bit (0F) -** This command is used to set the IDI bit when a level II command is in progress. This is needed since the register file is not accessible to the µp at that time.

8. **Cmd Deletion: Transfer Pad Command:** The Transfer Pad command is no longer supported in the WD33C93A.

9. **Cmd Deletion: Abort Command:** The Abort command is no longer supported in the Initiator mode.

10. **Feature Addition: Advanced Feature Control-** Bit 3 (EAF) of the Own ID register has been added to enable the following features:

    a) Unexpected Reselection handling: Following a reselection by an unexpected target during a Select-andTransfer command, by an unexpected target during a Select-and-Transfer command, or when idle and the Enable Reselection bit is 1, the WD33C93A will continue and go fetch the identify message before interrupting the host.

    b) Unknown Command Group size: In the Target mode, if the first byte of the CDB is an opcode for an unknown command group (groups 2, 3, 4, 6, or 7), the device will interrupt the host and ask for the total command length to be loaded into the Own ID register. This feature is for Wait-for-Select-and-Receive for Select-and-Transfer only.

    c) Data Phase Direction check: Bit 6 (DPD) has been added to the Destination ID register to specify the expected direction of the SCSI data phase. This allows an error condition to be generated if an incorrect data phase has been generated. This function is only applicable to the operation of Select-and-Transfer commands.

    d) Data Phase Direction Check Disable: Bit 5 (DF) has been added to the Destination ID register to enable or disable both the Data Phase Direction check feature and the link from Send-Status-and-Command-Complete to Wait-for-Select-and-Transfer. Note: This feature is is only in the revision E and F parts.

11. **Feature Addition: New Status Codes-** The following status codes have been added:

    a) WD33C93A Advanced Features Enabled- code 0000 0001: This code is returned after a "Soft Reset" if the Enable Advanced Features (EAF) bit is set (bit 4, Own ID). The code provides a means of verifying the presence of the A part.

    b) Unexpected Reselection- code 0010 0111: This code is returned when an unexpected reselection occurs during a Select-and-Transfer command, and indicates that the Target LUN register contains a valid identify message.

    c) Reselection- code 1000 0001: This code is returned when a reselection occurs when the device is idling with Advanced features Mode enabled. The code indicates that the Data register contains a valid identify message.

    d) Device Pause- code 1000 0111: This code is returned when the device has paused to get the command length in the Own ID register.

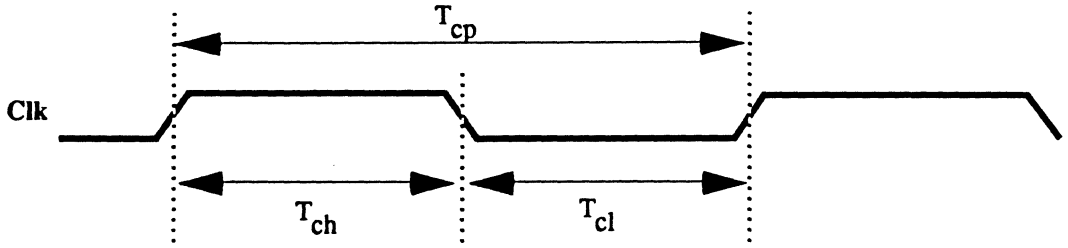
12. **Feature Addition: Reselect-and-Transfer Cmd Enhancement:** These commands may now be resumed in the same manner as the initiator Select-and-Transfer commands. Also,

these commands may be chained to the new Send-Status-and Command-Complete and Send-Disconnect-Message commands using the EDI bit in the control register, and the command link select bit in the destination ID register.

13. **Feature Addition: Wait-for-Select-and-Receive Cmd Enhancement:** This command may now be resumed in the same manner as the initiator Select-and-Transfer commands. Also, this command may be chained to from the new Send-Status-and-Command-Complete command. When EDI is set, this command will chain to the Send-Disconnect-Message command if CDB byte 1 indicates a read command has been received.

14. **Feature Addition: 20MHz clock rate:** The input clock timings for the WD33C93A have been changed from those listed in the WD33C93A data sheet, which specified a maximum frequency of 16Mhz. The WD33C93A is now guaranteed to operate with a maximum input clock frequency of 20MHz, and the revised timings are listed below:

Symbol	Characteristic	Min	Max	Units
T_{cp}	Clock Period	50	125	ns
T_{ch}	Clock High	20	---	ns
T_{cl}	Clock Low	20	---	ns



14.

15. **Function Change- Single byte Transfers:** The WD33C93 did not corrupt the Transfer Count register during a Single-Byte-Transfer. This allowed a previous multi-byte operation to be resumed without reloading the Transfer Count register after a Single-Byte-Transfer command. This was an "undocumented feature" that no longer exists in the WD33C93A. The Transfer Register is corrupted during a Single-Byte-Transfer and must be reloaded after execution of that command.

16. **Function Change- Phase Interrupts:** The WD33C93 generates a Phase Change interrupt following an Invalid Command interrupt. This is an unnecessary interrupt and basically an unplanned "feature" of the WD33C93. The WD33C93A does not provide a Phase Change interrupt following a Invalid Command interrupt.

17. Msc Changes/Additions:

a) CDB byte 11 register: This register is now also used to specify the status byte for Send-Status-and-Command-Complete commands

b) CDB Byte 12 register: When the Flag bit (Bit 1) is 0 and IDI is 1, Linked Command Complete (message code = 0Ah) is sent during a Send-Status-and-Command-Complete command. When this bit is 1 and IDI is 1, Linked Command Complete with Flag (message code = 0Bh) is sent during a Send-Status-and-Command-Complete command.

c) Target LUN register: This register can also contain the identify message received during an unexpected reselection if advanced features are enabled.

d) Select Command Chain Control: Bit 7 (SCC) in the Destination ID register has been added to control which command is chained to when the data transfer is completed:

0 Chain to Send-Status-and-Command-Complete
1 Chain to Send-Disconnect-Message

18. Rev E and F Changes only:

The following changes were incorporated into revisions E and F only of the WD33C93A part. Revision F is the current production part.

a) Enable Immediate Halt: Bit 5 (EIH) has been added to the Own ID register. This Target mode feature allows an immediate halt to occur on SCSI parity error or if ATN and HA are both true instead of waiting for a 4k data boundary to occur .

b) Bit 5 (DF) has been added to the Destination ID register to inhibit both the Data Phase Direction check in the Advanced Features mode and the link from Send-Status-and-Command-Complete to Wait-for-Select-and-Transfer.

19. Register Difference Summary:

Register	Bit	WD33C93	WD33C93A
a) Own ID register:	3	----	EAF- Enable Advanced Features
	4	----	HHP- Halt on Host Parity error
	5	----	EIH- Enable Immediate Halt
	6,7	----	Xfr rate control
b) Control register:	5	----	DBA- DMA Burst Enable
c) Destination ID register:	5	----	DF- Data Phase Dir Chk Enable
	6	----	DPD- Data Phase Dir check
	7	----	SCC- Select Command Chain
d) CDB Byte 12 register:	1	----	LCC- Linked Command Control
e) Synch Xfr register	3	----	extra bit for 12 byte FIFO

20. **WD33C93A Incompatibilities when being used with a WD33C93 also on the SCSI bus:**
Performance optimization of both the internal microcode and the LSI design have resulted in the following incompatibilities between the WD33C93A and the WD33C93:

    a) WD33C93 offset values: Due to timing differences between the two parts, the WD33C93 offset must not be set to its maximum value of five during synchronous transfers from the WD33C93A to the WD33C93. Any other offset value (0 through 4) may be used.

    b) The WD33C93A checks for ATN\ assertion before the start of a data transfer. A Receive or Send command will halt if HA is set prior to the transfer of any data. The WD33C93 allows a data transfer to occur before looking for ATN\.

21. **Function Change- 47h interrupt difference:** The 47h interrupt in the WD33C93 is generated for a parity error in the status, message, or command bytes as well as for an incorrect message. The 47h interrupt in the WD33C93A is only generated for a parity error in the status byte. A 4Fh interrupt is now generated for a parity error in the message or command bytes as well as for an incorrect message. The 43h interrupt is generated for all other parity errors (data/command bytes).

    To determine the cause of a 4Fh interrupt, issue a Transfer Information command. Either a message byte (if an incorrect message) or a 43h interrupt (if a parity error) will result.

22. **Function Change- Interrupt Difference:** A 13h interrupt is generated after Selection has occurred and an Abort command has been issued. The WD33C93 version issued a 23h interrupt.

23. **Function Change- MR (Master Reset) Input:** A hard reset (MR pin input) resets only the Own ID register. The WD33C93 hard reset clears all registers. All other functions of the hard reset are unchanged.

24. **Synchronous Transfer Period change:** The programming of the Synchronous Transfer Period register has changed from the WD33C93. Previously it was necessary to program the desired value+1. In the WD33C93A, the desired value is directly programmed (a period of 3 clocks is now programmed as "3" rather than "4" as in the WD33C93).

25. **RCS pulse in WD-Bus mode:** The WD33C93A no longer the RCS line to indicate a Ready to Transfer state. After the microprocessor issues a command to the SBIC chip, the microprocessor should then assert DRQ when it is ready for data transfer. The SBIC will sample the DRQ line and begin data transfer when ready.

26. Timing Differences:

Signal	Mode	WD33C93	WD33C93A	Max/Min
T_{RHDI}	**PIO**	10	5	ns min
T_{DLQH}	**DMA**	40 - 90	no min - 75	ns min-max
T_{DHQL}		30	0	ns min
T_{SHWI}	**WD-Bus**	0	no min spec	ns min
T_{SHRI}		0	no min spec	ns min
T_{SLWV}		20	30	ns max
T_{SLRV}		20	30	ns max
T_{WHDI}		30	20	ns min
T_{DVRH}		10	20	ns min
T_{RHDI}		10	0	ns min
T_{DVAL}	Async-Target	5	0	ns min
T_{RHDI}		0	replaced by T_{ALDI}	ns min
T_{ALDI}			0	ns min
T_{AHDI}	-Initiator	0	replaced by T_{RHDI}	ns min
T_{RHDI}			0	ns min
T_{RHDI}	Sync-Target			
T_{RHDI}	-Initiator			

27. I_{CC} Specifcation change: The maximum specification for the supply current has been increased from 20ma to 36ma.

28. WD33C93A Number Reference:

Model #	Manf #	Description
WD33C93A PL 00 08	5393KF09PL	40 pin Plastic DIP
WD33C93A JM 00 08	5393KF09JM	44 pin PLCC

WD33C93 Number Reference:

Model #	Manf #	Description
WD33C93 PL 00 bb	3393AB09PL	40 pin Plastic DIP
WD33C93 JM 00 bb	3393AB09JM	44 pin PLCC

Changes from Applications Note E035 rev A:

- Items 21 through 27 where added to the differences list for WD33C93A.

WESTERN DIGITAL

Storage LSI Applications Note

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PRODUCT: Model # **WD33C93A**
Manf # 5393

August 17, 1990
Number **E031-A**

WD33C93A Data Sheet

Contents:

Data Sheet

WD33C93A: A MOS/VLSI 40/44 pin chip providing high and low level interface functions to the SCSI bus. Full SCSI bus features include arbitration, disconnect, reconnect, parity generation and checking, synchronous and asynchronous transfers up to 4 Mbytes/s, DMA, and built in 48ma drivers for direct connection to a single ended SCSI bus. The main differences between the WD33C93A and the previous version (WD33C93) are faster transfer rates, host parity generation and checking, an extended FIFO, faster command execution times and a number of new commands. For more information on these changes and additions refer to WD Storage LSI Applications Note # E062.

Source Document #: 79-000199, WD16278 6/88

Part Numbers:

Model #	**Manf #**	**Description**
WD33C93A PL 00 08	5393KF09PL	40 pin Plastic DIP
WD33C93A JM 00 08	5393KF09JM	44 pin PLCC

International Offices:
Hong Kong 852-736-5123; Korea 822-554-0508; Munich 498-9922-0060; Ontario 416-566-4702; Paris 331-6985-5757; Quebec 514-697-1532; Singapore 65-448-4700; Taiwan 886-2717-4775; Tokyo 813-791-2001; U.K. 443-7274-2955.

WD33C93A SCSI Bus Interface Controller

FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers.
- Asynchronous Data transfers up to 2.5 Mb/sec
- Synchronous Data transfers up to 5.0 Mb/sec
- Synchronous offset selectable from 1 to 12 bytes.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Can be used as host adapter (SCSI Initiator) or peripheral adapter (SCSI Target).
- Local host data transfer options include programmed I/O, single byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Includes 48-ma drivers for direct connection to the SCSI bus.
- 24 bit transfer counter.
- Programmable timeout for selection and reselection.
- Internal Microcontroller
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Special "Translate Address" command performs the Logical-to-Physical addressed translation.
- Single +5V supply.
- Available in 44-pin chip carrier or 40-pin DIP.
- Low power CMOS design.

DESCRIPTION

The WD33C93A is a MOS/VLSI device which is implemented in Western Digital's CMOS process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL-compatible.

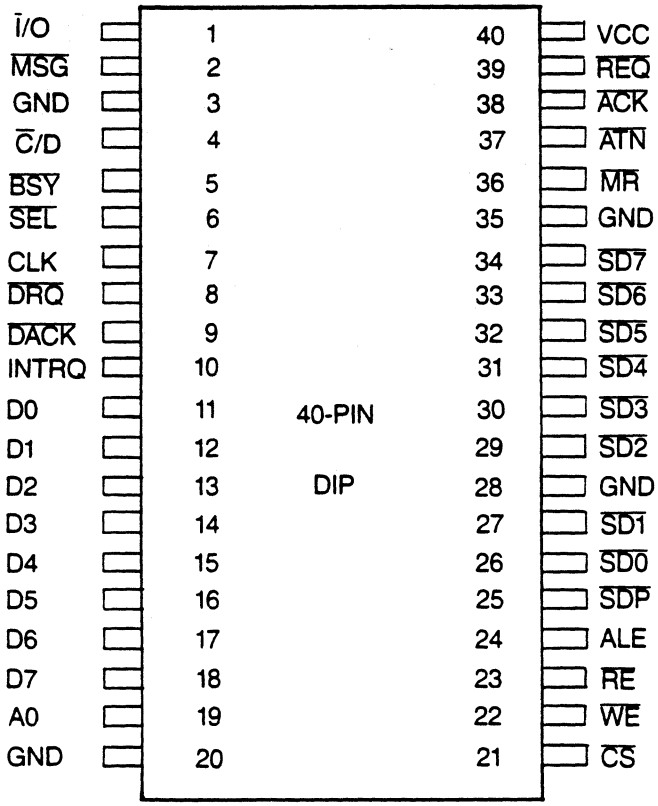
The WD33C93A is intended for use in systems which interface to the SCSI (Small Computer System Interface) Bus. The WD33C93A can operate in both the Initiator (typically, a host computer system) and the Target (typically, a peripheral device) SCSI bus roles.

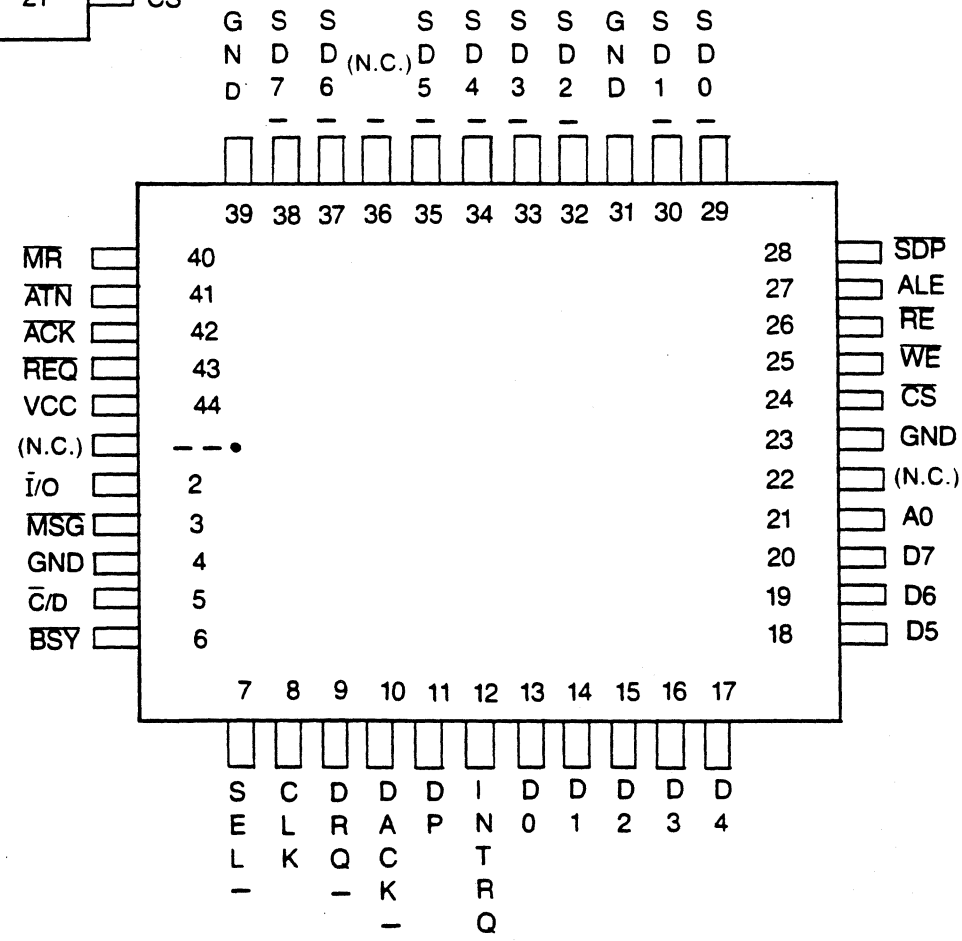
When used in the host system, the WD33C93A interfaces to both the host bus and to the SCSI bus. To perform a SCSI operation, the host processor must issue a command to the WD33C93A to select the desired Target. The WD33C93A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a higher priority bus device, it continues trying, notifying the host when it has succeeded by generating an interrupt. At this point, the WD33C93A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the WD33C93A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the WD33C93A. The WD33C93A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The WD33C93A also offers high level Select-And-Transfer commands, which may be used to eliminate the interrupt-handling which is otherwise typically required between each SCSI bus phase.

When the WD33C93A is used in a peripheral system, it interfaces with a local processor and the SCSI bus just as it does when used as a host adapter. In this environment, the WD33C93A will operate primarily in a Target role. The Target-role command set enables the WD33C93A to request each SCSI bus phase individually, or the special combination commands may be used for automatic SCSI bus phase sequencing.

The WD33C93A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.





NOTE: Pin labeled N.C. should be left not connected.

4. PIN DESCRIPTIONS

4.1 PROCESSOR/DMA INTERFACE

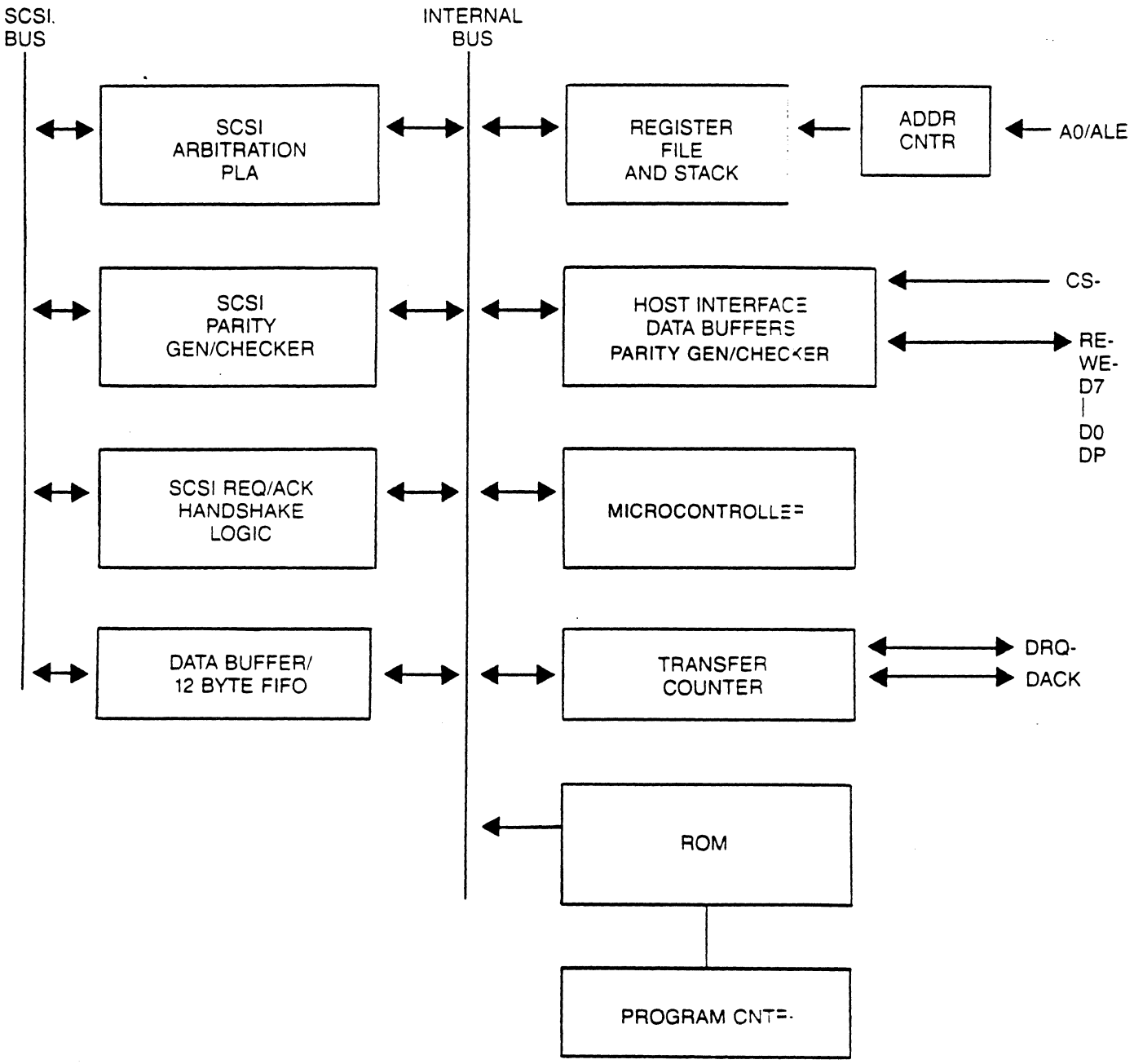
DIP (40 PIN)	PLCC (44 PIN)	NAME	I/O	FUNCTION
7	8	CLK	I	8–16 MHz square wave clock.
36	40	$\overline{MR}$	I	Reset is an active low input which forces the WD33C93A into an idle state. All SCSI signals are forced to the negated state.
10	12	INTRQ	O	Interrupt Request to external microprocessor. Used to indicate command completion/termination or a need to service the SCSI interface. This bit is reset when the SCSI Status register is read.
23	26	$\overline{RE}$	I/O	Read enable is an active low input which is used with CS- to read a WD33C93A register. In WD Bus mode, it is used as an output to read data from a sector buffer. (Tri-State)
22	25	$\overline{WE}$	I/O	Write enable is an active low input which is used with CS- to write a WD33C93A register. In WD Bus mode, it is used as an output to write data to a sector buffer. (Tri-State)
21	24	$\overline{CS}$	I	Chip Select is an active low input which is used to qualify RE- and WE- when accessing a register. This signal must be inactive during a DMA cycle (DACK- active in DMA/burst mode, or DRQ active in WD Bus mode).
19	21	AO	I	Address pin used to access the internal registers for non-multiplexed address/data busses (i.e., the ALE pin is grounded). The address of the desired register is loaded into the Address register during a write cycle with A0 = 0. The selected register is then accessed when A0 = 1.
24	27	ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired WD33C93A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the Address register for a complete discussion of direct and indirect addressing.
9	10	$\overline{DACK}$/($\overline{RCS}$)	I/O	DMA acknowledge input used for interfacing to an external DMA controller. When DACK is low, all bus transfers are to/from the Data register regardless of the contents of the ADDRESS register. In WD Bus mode, this pin functions as a RAM chip select output to allow the WD33C93A to access a sector buffer. RE- and WE- are outputs when RCS- is active. Since this pin can be an open drain output, a pullup resistor is required when operating in WD Bus mode.
8	9	$\overline{DRQ}$/ (DRQ)	I/O	Data request is an output when interfacing to an external DMA controller, and an input when in WD Bus mode. When used with an external DMA controller, DRQ- and DACK- form the handshake for the data-byte transfers. In Burst mode, DRQ- remains low as long as there is data to transfer. In WD Bus mode, the WD33C93A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, RCS- is false, and the RE- and WE- outputs are disabled. Since this pin can be an open drain output, a pullup resistor is required when operating in DMA or Burst mode.
18-11	17-13	D7-D0	I/O	Host processor data bus.
	11	DP	I/O	Data Parity, used only for checking/generating host data bus parity during data transfers. (odd)

4.2 SCSI INTERFACE

Note: All pins have open-drain output drivers.

DIP (40 PIN)	PLCC (44 PIN)	NAME	I/O	FUNCTION
39	43	$\overline{REQ}$	I/O	REQ- is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ ACK data transfer.
38	42	$\overline{ACK}$	I/O	ACK- is an output in the initiator role and an input in the target role. It is used to indicate an acknowledgement for a REQ/ACK data transfer handshake.
37	41	$\overline{ATN}$	I/O	ATN- is an output in the initiator role and an input in the target role. It is used to indicate the SCSI Attention condition.
2	3	$\overline{MSG}$	I/O	MSG- is an input in the initiator role and an output in the target role. It is asserted during a Message phase.
4	5	$\overline{C}$/D	I/O	C/D- is an input in the initiator role and an output in the target role. It is used to indicate whether Control or Data information is on the SCSI data bus.
1	2	$\overline{I/O}$	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
5	6	$\overline{BSY}$	I/O	BSY- is asserted when the WD33C93A is attempting to arbitrate for the SCSI bus or when connected as a Target.
6	7	$\overline{SEL}$	I/O	SEL- is asserted when the WD33C93A is attempting to select or reselect another SCSI device.
N/A	28	$\overline{SDP}$	I/O	SCSI data bus parity signal. (odd)
34–26	38–29	$\overline{SD7}$–$\overline{SD0}$	I/O	SCSI data bus.

5. WD33C93A BLOCK DIAGRAM



6. WD33C93A REGISTERS

6.1 REGISTER MAP

A0	R/W	REGISTER ACCESSED		ADDRESS (Hex)
0	R	AUXILIARY STATUS		XX
0	W	ADDRESS REGISTER		XX
1	R/W	OWN ID REGISTER	/CDB SIZE	00
1	R/W	CONTROL REGISTER		01
1	R/W	TIMEOUT PERIOD REGISTER		02
1	R/W	TOTAL SECTORS REGISTER	/CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER	/CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER (MSB)	/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER (LSB)	/CDB 4TH	06
1	R/W	LOGICAL ADDRESS (MSB)	/CDB 5TH	07
1	R/W	LOGICAL ADDRESS (2ND)	/CDB 6TH	08
1	R/W	LOGICAL ADDRESS (3RD)	/CDB 7TH	09
1	R/W	LOGICAL ADDRESS (LSB)	/CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER	/CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER	/CDB 10TH	0C
1	R/W	CYLINDER NUMBER REGISTER (MSB)	/CDB 11TH	0D
1	R/W	CYLINDER NUMBER REGISTER (LSB)	/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER		0F
1	R/W	COMMAND PHASE REGISTER		10
1	R/W	SYNCHRONOUS TRANSFER REGISTER		11
1	R/W	TRANSFER COUNT REGISTER (MSB)		12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)		13
1	R/W	TRANSFER COUNT REGISTER (LSB)		14
1	R/W	DESTINATION ID REGISTER		15
1	R/W	SOURCE ID REGISTER		16
1	R	SCSI STATUS		17
1	R/W	COMMAND REGISTER		18
1	R/W	DATA REGISTER		19
1	R	AUXILIARY STATUS	(DIRECT ADDRESSING MODE)	1F

NOTES:
1. All unused bits of a defined register are reserved and must be zero.
2. Reading an undefined or unavailable register results in an all-ones data bus output.
3. Register addresses are determined by the Address register bits AR0 thru AR7.
4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the Address register is loaded with ALE. In this mode, the Auxiliary Status register is mapped at Hex 1F.
5. See section 6.3 for a description of how reset affects the internal registers.

6.2 REGISTER DESCRIPTIONS

6.2.1 AUXILIARY STATUS REGISTER (Address Hex IF)

The Auxiliary Status register is a read-only register which contains general status information not directly associated with the interrupt condition. The Auxiliary Status register may be accessed at any time, except during DMA accesses (DACK- asserted in DMA/Burst mode, or DRQ asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 0 DBR Data Buffer Ready is used during programmed I/0 to indicate to the processor whether or not the Data register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the WD33C93A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.

Bit 1 PE Parity Error status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus, and is checked on data received from the SCSI bus during transfers out to the host bus. Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the Control register. The PE bit is cleared when a new command is issued.

Bit 2 Not used, will be zero.

Bit 3 Not used, will be zero.

Bit 4 CIP COMMAND IN PROGRESS, when set, indicates that the WD33C93A is interpreting the last command entered into the Command register and therefore this register is unavailable. When this bit is reset, a command may be written to the Command register.

Bit 5 BSY BUSY indicates that a Level II command is currently executing and therefore only the Command register (when CIP = 0), the DATA register, and the Auxiliary Status register are accessible by the host. A Level II command may not be written to the Command register when this bit is one.

Bit 6 LCI LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored and this status set.

Bit 7 INT INTERRUPT PENDING indicates that the Intrq pin is asserted. The host should read the SCSI Status register to clear Intrq prior to issuing any commands.

6.2.2 ADDRESS REGISTER [Address XX Hex]

The Address register is a write-only register which contains the address of the register to be accessed. Registers in the WD33C93A may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The ALE is typically then followed by the CS- and WE- or RE- signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F Hex.
- Indirect addressing (separate address/data busses). In indirect addressing, the register access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the Address register is loaded by performing a write of the desired address to the WD33C93A (WE- and CS- asserted) with A0 = 0. Then the register is accessed by asserting CS- and WE- or RE-, with A0 = 1. Also, following every access with A0 = 1, the Address register will automatically increment to point at the next register, with the exception of the following locations: Auxiliary Status register, Data register, and the Command register. In indirect addressing, the Auxiliary Status register is accessed by performing a read (CS- and RE- asserted) with A0 = 0.

6.2.3 OWN ID/CDB SIZE REGISTER [Address 00 Hex]

The Own ID/CDB Size register, in its first mode, contains both the encoded ID of the WD33C93A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the input clock division. In its second mode (when advanced features are enabled, see 7.3), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the WD33C93A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and then a "Reset" command issued, to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see 7.3).

OWN ID/CDB SIZE REGISTER

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0–2 IDn SCSI ID Bits 0–2 set the SCSI bus ID number that the WD33C93A will use during arbitration and selection.

Bit 3 EAF ENABLE ADVANCED FEATURES, when set to one, causes the WD33C93A to enable certain advanced features (see section 7.3). When this bit is zero, those features are disabled.

Bit 4 EHP ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the Auxiliary Status register will indicate parity errors detected on the host bus, and the HHP bit in the Control register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero.

NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 Not used, will be zero.

Bit 6–7 FSn FREQUENCY SELECT 0–1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8–10	0	0	2
12–15	0	1	3
16	1	0	4
xx	1	1	undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

$$\text{MAXIMUM SCSI TRANSFER RATE} = \frac{\text{INPUT CLOCK FREQUENCY}}{\text{CLOCK DIVISOR}} \text{ [MByte/sec]}$$

6.2.4 CONTROL REGISTER [Address 01 Hex]

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.

BIT	7	6	5	4	3	2	1	0
	DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP The HALT on SCSI PARITY ERROR bit enables the WD33C93A to terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the ACK- pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.

Bit 1 HA The HALT on ATTENTION bit (in Target mode only) enables the WD33C93A to terminate a Send or Receive command if the ATN- input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the WD33C93A. The ATN- input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI The Intermediate Disconnect Interrupt bit, when set, enables the WD33C93A to generate an 85H disconnect interrupt and suspends a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode combination commands that serve to reduce host system overhead. Refer to Section 7 for more details.

Bit 3 EDI When the Ending Disconnect Interrupt bit is set, the 16H interrupt which normally follows the Command Complete message during the execution of a Select-And-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to Section 7 for more details.

Bit 4 HHP The Halt on Host Parity Error bit enables the WD33C93A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the ACK- signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.

Bit 5–7 DMx DMA Mode Select bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	Polled I/0 Mode, or no DMA enabled. All data phase transfers are performed by polling for DBR in the Auxiliary Status register, and then writing (reading) the data to (from) the Data register.
0	0	1	Burst Mode selects a demand-mode DMA interface. In this mode, the DRQ- signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and RE-/WE- as long as DRQ- is active.
0	1	0	WD Bus Mode should be selected when the WD33C93A is connected to a WD Bus. This mode is also referred to as Direct Buffer Access (DBA) mode. In this mode, the WD33C93A acts as a bus master, and all data access signals reverse their direction: The DRQ- signal become the DRQ input, which enables the WD33C93A to drive the buffer bus control signals. The DACK- signal becomes the RCS- output, which is asserted as a chip select for the buffer. RE- and WE- become outputs which drive the read and write functions of the external FIFO/RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or the host/local up decides to pause the transfer by negating the DRQ signal; after negating DRQ, one more transfer may occur before the RCS-, RE-, and WE- signals are negated.
1	0	0	DMA Mode is selected when the WD33C93A is to be used with a DMA controller in single-type transfer mode. In this mode, DRQ- is asserted and then negated, and the DMA controller responds by asserting DACK- and WE- or RE-, for each data byte transferred to/from the WD33C93A.

6.2.5 TIMEOUT PERIOD REGISTER [Address 02 Hex]

The Timeout Period register is an 8-bit register containing a preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} * \text{Ficlk}}{80\text{d}}$$

Where:

Tper = the desired timeout period in milliseconds;
Ficlk = the input clock frequency at the CLK pin in Megahertz (with no divisor applied).
d = decimal

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the WD33C93A will wait for a response (indicated by assertion of the BSY- signal) after it has begun the selection phase (assert SEL- and negate BSY-) before terminating the command. The timeout function can be disabled by loading the Timeout Period register with zero.

NOTE: The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

6.2.6 TOTAL SECTORS REGISTER/ CDB 1ST BYTE [Address 03 Hex]

Translate Address: The Total Sectors register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer: This register should be loaded with the first byte of the Command Descriptor Block before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the first byte of the received CDB in this register.

6.2.7 TOTAL HEADS REGISTER/ CDB 2ND BYTE [Address 04 Hex]

Translate Address: This register holds the total number of heads during a Translate Address command.

Select-And-Transfer: This register should be loaded with the second byte of the CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the second byte of the received CDB in this register.

6.2.8 TOTAL CYLINDERS REGISTER/ CDB 3RD AND 4TH BYTES [Address 05, 06 Hex]

Translate Address: This is a 16-bit register which holds the total number of cylinders.

Select-And-Transfer: This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the third and fourth bytes of the received CDB in this register.

6.2.9 LOGICAL ADDRESS REGISTER/ CDB 5TH-8TH BYTES [Address 07, 08, 09, 0A Hex]

Translate Address: The Logical Address register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-And-Transfer: For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-For-Select-And-Receive: The WD33C93A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

6.2.10 SECTOR NUMBER REGISTER/CDB 9TH BYTE [Address 0B Hex]

Translate Address: This register will contain the resulting sector number following a Translate Address command.

Select-And-Transfer: This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the ninth byte of a ten or twelve byte received CDB in this register.

6.2.11 HEAD NUMBER REGISTER CDB 10TH BYTE [Address 0C Hex]

Translate Address: The Head Number register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed by the WD33C93A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-And-Transfer: This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the tenth byte of a ten or twelve byte received CDB in this register.

6.2.12 CYLINDER NUMBER REGISTER/CDB 11TH AND 12TH BYTES [Address 0D, 0E, Hex]

Translate Address: The Cylinder Number register is a

16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the Head Number register initially contains a non-zero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track * total heads — total spare sectors/cyl) before issuing the command.

Select-And-Transfer: This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing a Select-and-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-And-Command-Complete: The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-And-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the WD33C93A. If bit 0 of the CDB12 register is set to one, then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A Hex (FLAG = 0) or a OB Hex (FLAG = 1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 Hex) is sent.

6.2.13 TARGET LUN REGISTER [Address 0F Hex]

The Target LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various WD33C93A commands and sequences. During a Select-And-Transfer or Reselect-And-Transfer command, the contents of this register (along with the Source ID register) are used to generate and check the Identify messages which are transferred across the SCSI bus. In addition, the Target LUN register is used to hold the Target Status byte received during a Select-And-Transfer command.

BIT	7	6	5	4	3	2	1	0
	TLV	DOK	0	0	0	TL2	TL1	TL0

During Wait-For-Select-And-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether or not the Initiator has enabled disconnects.

During Reselect-And-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.

In advanced mode, during Select-And-Transfer commands, this register is used to handle reselection by an unexpected Target. In this mode, this register will hold the image of the Identify message received from the Target. In this case, the TLV bit is one, since the Target always sends the Identify message.

6.2.14 COMMAND PHASE REGISTER [Address 10 Hex]

The Command Phase register is used during combination commands to indicate which phases of these multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

6.2.15 SYNCHRONOUS TRANSFER REGISTER [Address 11 Hex]

The Synchronous Transfer register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3 – OF0 = 0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if WD-Bus mode is used, the transfer period and the width of the RE-/WE- strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.

BIT	7	6	5	4	3	2	1	0
	0	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0–3 OFx The OFFSET bits are used to select the desired offset according to the following:

OF3	OF2	OF1	OF0	SELECTED OFFSET
0	0	0	0	Note 1
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	0	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	12
1	1	1	X	12

Note 1* — Asynchronous data phase transfers

Bit 4-6 TPx The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

TP2	TP1	TP0	SCSI/WD-BUS TRANSFER PERIOD	(SCSI REQ/ACK synchronous pulse width and WD-BUS RE-/WE- pulse width)
0	0	X	8 cycles	(4 cycles)
0	1	0	2 cycles	(1 cycle)
0	1	1	3 cycles	(1 cycle)
1	0	0	4 cycles	(2 cycles)
1	0	1	5 cycles	(3 cycles)
1	1	0	6 cycles	(4 cycles)
1	1	1	7 cycles	(4 cycles)

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

$$\text{CYCLE } (\mu s) = \frac{\text{DIVISOR (from OWN ID)}}{2 * \text{INPUT CLOCK FREQUENCY (MHZ)}}$$

6.2.16 TRANSFER COUNT REGISTER [Address 12, 13, 14 Hex]

The Transfer Count register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a successful completion interrupt when the counter reaches zero. In combination commands, this register specifies the number of bytes to be transferred during a Data phase.

The counter function can be disabled by loading the Transfer Count register with zeroes prior to issuing a command or by setting the Single-Byte Transfer bit in the Command register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the Transfer Count register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the Transfer Count register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including clearing the internal FIFO of any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the Transfer Count register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the Transfer Count should be used to determine the actual number of bytes transferred to/from the SCSI bus.

6.2.17 DESTINATION ID REGISTER [Address 15 Hex]

The Destination ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.

BIT	7	6	5	4	3	2	1	0
	SCC	DPD	0	0	0	DI2	DI1	DI0

Bit 0–2 Destination ID bits DI0-DI2 contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or a Select command is issued.

Bit 6 DPD DATA PHASE DIRECTION, when advanced features are enabled (see 7.3), is used to specify the expected direction of the SCSI data phase. This allows the WD33C93A to verify the direction during Select-And-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.

Bit 7 SCC SELECT COMMAND CHAIN is used only when the Reselect-And-Transfer command is issued with EDI = 1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

6.2.18 SOURCE ID REGISTER [Address 16 Hex]

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the WD33C93A. It also contains bits that enable and control response to selection and reselection.

BIT	7	6	5	4	3	2	1	0
	ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bit 0–2 SIx Source ID Bits 2–0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the WD33C93A.

Bit 3 SIV Source ID Valid is set to one after the WD33C93A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the WD33C93A) during the select/reselect phase. This bit is zero if only the bus ID bit of the WD33C93A was asserted.

Bit 4 Not used, will be zero.

Bit 5 DSP Disable Select Parity, when set to one, causes the WD33C93A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.

Bit 6 ES Enable Selection, when set to one, enables the WD33C93A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.

Bit 7 ER Enable Reselection, when set to one, enables the WD33C93A to respond to a reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.

6.2.19 SCSI STATUS REGISTER [Address 17 Hex]

The SCSI Status register is a read-only register which indicates the cause of the most recent interrupt request assertion. Interrupt request is asserted whenever a condition occurs within the WD33C93A that requires intervention by the host; for example:

- the WD33C93A has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

Once interrupt request has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the WD33C93A has been reset.

BIT	7	6	5	4	3	2	1	0
	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0–3 SSx SCSI Status bits 0–3 are status qualifiers whose meaning depends upon which upper (4–7) status bit is set.

Bit 4–7 SSx SCSI Status bits 4–7 define the type of interrupt that occurred. The possible codes are defined in the following table:

STATUS	CODE	GROUP MEANING
0000	xxxx	The WD33C93A is in a reset state.
0001	xxxx	A WD33C93A command has completed successfully.
0010	xxxx	A WD33C93A command has paused or was aborted by an Abort command.
0100	xxxx	A WD33C93A command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'State' column indicates the current state from which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The table below summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

RESET STATE INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0000	0000	D, T, I	WD33C93 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the WD33C93A is disconnected.
0000	0001	D, T, I	WD33C93A Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the WD33C93A is disconnected.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

SUCCESSFUL COMPLETION INTERRUPTS

STATUS.	CODE	STATE*	SPECIFIC MEANING
0001	0000	D	A Reselect command completed successfully. The new state of the WD33C93A is connected as a Target.
0001	0001	D	A Select command completed successfully. The new state of the WD33C93A is connected as an Initiator.
0001	0010		Reserved for future use.
0001	0011	D, T	A Receive, Send, Reselect-And-Transfer, Wait-For-Select-And-Receive, Send-Status-And-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN- is not asserted).
0001	0100	D, T	A Receive, Send, Reselect-And-Transfer, Wait-For-Select-And-Receive, Send-Status-And-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN- is asserted).
0001	0101	D, T	A Translate Address command completed successfully.
0001	0110	D, I	A Select-And-Transfer command completed successfully.
0001	0111		Reserved for future use.
0001	1MCI	I	A Transfer (non-Message IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

PAUSED OR ABORTED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0010	0000	I	A Transfer Info (Message-In phase) command has paused with ACK- asserted. This allows the host to examine the message before accepting it.
0010	0001	I	A Save Data Pointers message was received during a Select-And-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select or Reselect command was aborted.
0010	0011	T	A Receive or Send command has halted by an error or was aborted (ATN- is not asserted).
0010	0100	T	A Receive or Send command has halted by an error or ATN-asserted, or was aborted (ATN- is asserted).
0010	0101	D	An Abort was issued while the WD33C93A was in the process of being selected or reselected.
0010	0110		Reserved for future use.
0010	0111	D	The WD33C93A has been reselected during a Select-And-Transfer (with IDI = 0) by a Target that does not match the SCSI bus ID loaded into the Destination ID register; or the following Identify message did not match the LUN loaded into the Target LUN register. ACK- has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the Source ID and Target LUN registers. (Advanced Mode only)
0010	1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

TERMINATED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0100	0000	D, T, I	An invalid command was issued.
0100	0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the WD33C93A is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the WD33C93A is disconnected.
0100	0011	T, I	A parity error caused a command to terminate (ATN- is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	T, I	A parity error caused a command to terminate (ATN- is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	D, T	The Logical Address exceeded the disk boundaries.
0100	0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the Destination ID register has reselected the WD33C93A during a Select-And-Transfer command (with IDI = 0). This interrupt occurs when the WD33C93A is not in Advanced Mode. The new state of the WD33C93A is connected as an Initiator.
0100	0111	I	An incorrect status byte (i.e. the status byte has a parity error) was received during a Select-And-Transfer command. The Data Register can be read to observe the status byte in error.
0100	1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested. This is typically caused by a phase change before the Transfer Count has reached zero, or an unexpected phase sequence occurred during a Select-And-Transfer command.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

SERVICE REQUIRED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
1000	0000	D	The WD33C93A has been reselected. The new state of the WD33C93A is connected as an Initiator. No Identify message transfer has yet occurred.
1000	0001	D	The WD33C93A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the Source ID register. The Identify message from the Target may be read from the Data register. The ACK- signal is left asserted. The new state of the WD33C93A is connected as an Initiator.
1000	0010	D	The WD33C93A has been selected (no ATN- assertion). The new state of the WD33C93A is connected as a Target.
1000	0011	D	The WD33C93A has been selected (ATN- was asserted). The new state of the WD33C93A is connected as a Target.
1000	0100	T	The ATN- signal has been asserted.
1000	0101	I	A disconnect has occurred. The new state of the WD33C93A is disconnected.
1000	0110		Reserved for future use.
1000	0111	T	The Wait-For-Select-And-Receive command has paused because the first byte of the incoming CDB is not a known command group. The Own ID register must be loaded with the CDB length, and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the WD33C93A is connected as a Target. (Advanced Mode only)
1000	1MCI	I	The REQ signal has been asserted following connection or when the WD33C93A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

6.2.20 COMMAND REGISTER [Address 18 Hex]

The Command register is used to issue the WD33C93A commands. Since the WD33C93A expects the SCSI Status to have been read before the host can issue a valid command, a command should not be loaded into the Command register within seven microseconds (independent of input clock frequency) from the last SCSI Status read to avoid the command being ignored (indicated by the LCI bit in the Auxiliary Status register). Also, this register should never be loaded when the CIP or INT bits (in Auxiliary Status) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The Single-Byte Transfer (SBT) bit in the Command register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the Transfer Count register.

Refer to the Commands section for a description of the commands and their corresponding command codes.

BIT	7	6	5	4	3	2	1	0
	SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

6.2.21 DATA REGISTER [Address 19 Hex]

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/WD BUS interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the interval twelve byte FIFO of the WD33C93A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the WD33C93A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the host processor during a data phase when the CONTROL register DMA mode select bits are all reset (= 0), and when the DBR bit in the Auxiliary Status register is true. The processor writes (reads) the DATA register by loading the Address register with a Hex value of 19 and asserting the WE- (RE-) and CS- pins. This access also occurs during non-data phases.

When the Control register DMA mode selects bits are set for DMA mode or Burst mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the DACK- and WE- pins are asserted in response to the assertion by the WD33C93A of the DRQ- pin.

When the WD-BUS is selected by the DMA mode select bits, the RCS- pin functions as an external buffer chip select and the WE- and RE- pins become outputs, allowing the WD33C93A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any device by negating the DRQ pin.

6.3 RESET CONDITIONS

6.3.1 HARDWARE RESET

The following results occur when the WD33C93A is reset by the assertion of the MR- signal:

- The LCI and PE bits in the Auxiliary Status register are reset to zero. The DBR bit in the Auxiliary Status Register is reset to zero. The BSY and CIP are reset to zero, and the INT bit (and INTRQ pin) is set to one when the hardware reset is complete.
- The Own ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the Source ID register are reset to zero.
- The SCSI Status register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the MR- signal:
  - Registers 01 Hex through 15 Hex;
  - Source ID (16 Hex) register bits 0–3;
  - Command register (18 Hex).

NOTE: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the WD33C93A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

6.3.2 SOFTWARE RESET

The following results occur when the WD33C93A executes the Reset command:

- The DBR bit in the Auxiliary Status register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter, offsets, and state machines are cleared.
- The Own ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 Hex through 16 Hex are reset to zero. The Command register (18 Hex) is also reset to zero.
- The SCSI Status register is set as commanded by the EAF bit in the Own ID register.

7. COMMANDS
7.1 COMMAND LISTS

COMMAND CODE (Hex)	COMMAND	VALID STATES	LEVEL
00	Reset	D,T,I	I
01	Abort	D,T,I	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-With-ATN	D	II
07	Select-Without-ATN	D	II
08	Sel w/ATN-And-Transfer	D,I	II
09	Sel w/o ATN-And-Transfer	D,I	II
0A	Reselect-And-Receive Data	D	II
0B	Reselect-And-Send Data	D	II
0C	Wait-For-Select-And-Receive	D	II
0D	Send-Status-And-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

WD33C93A valid states:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

7.2 WD33C93A COMMAND TYPES

There are two basic types of WD33C93A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an Auxiliary Status of BSY = 1, CIP = 0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single WD33C93A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence.These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can also be chained together to minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The WD33C93A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the Command List. An attempt to issue a Level II command which is invalid for the present WD33C93A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

7.3 ADVANCED MODE FEATURES

The WD33C93A has several new features included which add new functions to the original WD33C93 design. Some of these features cause the WD33C93A to be incompatible with the WD33C93. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the WD33C93A is reset by the MR- signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAR) bit set in the Own ID register. The host can determine if advanced features have been enabled (thereby implying that a WD33C93A is installed) by examining the SCSI status register after issuing the 'Reset' command.

The features enabled by this bit are described below.

7.3.1 UNEXPECTED RESELECTION:

When in normal mode, a reselection when idle (ER = 1) or when disconnected during a Select-And-Transfer command (and the Target bus ID does not match the Destination ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the WD33C93A will continue to the Message In phase to fetch the Identify message. If the WD33C93A was idle, the SCSI status register will be set to 81 Hex, and the Identify message will be in the Data register. If the WD33C93A was executing a Select-And-Transfer command, the SCSI status register will be set to 27 Hex, and the Identify message will be in the Target LUN register. In either case, the Source ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rejected.

7.3.2 UNKNOWN SCSI COMMAND GROUPS

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7–5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F Hex), group 1 (opcodes 20 to 3F Hex), and group 5 (opcodes A0 to BF Hex) commands are defined by the SCSI standard (X3.131–1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the WD33C93A will assume that these undefined groups are six byte commands when executing Select-And-Transfer or Wait-For-Select-And-Receive commands. In Advanced Mode, the following events will occur:

- **Select-And-Transfer:** When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The WD33C93A uses this value to make sure the correct number of bytes are then transferred in the command phase.
- **Wait-For-Select-And-Receive:** When receiving the CDB from the Initiator, the WD33C93A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host processor can examine the first command byte in the CDB 1ST register, and then load the Total command length into the Own ID register. The SCSI status register is set to 87 Hex, and the Command Phase register is set to 31 Hex, when this interrupt occurs.

After the interrupt, the WD33C93A will only accept a Resume Wait-For-Select-And-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the WD33C93A will continue to transfer the first six bytes of the command into its internal FIFO.

7.3.3 DATE PHASE DIRECTION

During a Select-And-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the WD33C93A will not detect this error but expects that the transfer will continue. In Advanced Mode, the DPD bit in the Destination ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI status register.

7.4 LEVEL I COMMANDS

7.4.1 RESET (00 HEX)

The Reset command performs a similar function to the hardware reset caused by asserting the MR- pin except that the Own ID register is sampled for information concerning the operating configuration of the WD33C93A. The WD33C93A is also initialized as described in the RESET CONDITIONS section. The Reset command may be executed in any WD33C93A state and will force the WD33C93A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 Hex or 01 Hex, depending on the contents of the OWN ID register.

7.4.2 ABORT (01 HEX)

The Abort command is valid in any WD33C93A state: Disconnected, Target, or Initiator. The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State: In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the WD33C93A has won arbitration, the WD33C93A releases the SCSI bus by removing the Bus ID bits while SEL- is asserted and checking for a negated BSY- signal. If, after at least 200 μS, there is no BSY- response, the WD33C93A goes to a Bus Free condition, and a "paused/aborted" interrupt is generated. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the WD33C93A has not yet won arbitration, it will immediately abort the Select or Reselect command.

Target State: When the WD33C93A is in a Connected as a Target state, the Abort command may be used to abort RECEIVE, SEND, or the data phase portion of a Target combination command. When issuing an Abort in the Connected as a Target state, the following rules apply:

1. When an Abort command is issued to abort a SEND or Reselect-and-SEND command, the local processor must not service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The WD33C93A removes the data request at an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.

2. When an Abort command is issued to abort a RECEIVE or Reselect-and-RECEIVE command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processor has received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C93A remains in the connected as a Target state. The WD33C93A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

Initiator State: When the WD33C93A is in a connected as an Initiator state, the Abort command may be used to abort TRANSFER INFO, TRANSFER PAD, Select, or Select-and-TRANSFER command. When issuing an Abort in the connected as an Initiator state, the local processor must continue to service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the data destination.

After the Abort command is processed and the local processor has received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C93A remains in the connected as an Initiator state. The WD33C93A is now ready to receive any appropriate Initiator mode command, including a resume of the command that was aborted.

7.4.3 DISCONNECT (04 HEX)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the WD33C93A transitions to the Disconnected state.

7.4.4 ASSERT ATN (02 HEX)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (the Target is expected to respond by performing a Message Out Phase).

ATN- is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the Target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the WD33C93A to automatically assert ATN- prior to the release of SEL- providing the bus arbitration is won.

7.4.5 NEGATE ACK (03 HEX)

The Negate Ack command causes ACK- to be negated. It is used when Connected as an Initiator following Message-In type Transfer Info commands, or when the WD33C93A has detected a parity error on any received information and the Halt on SCSI Parity Error (HSP) bit is set. Host parity errors do not affect the ACK- signal. For all other Initiator transfers, ACK- negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "Message Reject" or a "Message Parity Error" Message by issuing the Assert ATN command prior to issuing the Negate Ack command. If the incoming message is to be accepted, only the Negate Ack command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by parity error, the Assert ATN command can again be issued prior to Negate ACK, this time indicating the Initiator's intent to send an "Initiator Detected Error" Message.

7.4.6 SET IDI (0F HEX)

The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the Control register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of WD33C93A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

7.5 SIMPLE LEVEL II COMMANDS

7.5.1 SELECT-WITH-ATN (06 HEX)

Select-with-ATN is valid only in the Disconnected state and when issued will cause the WD33C93A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the Destination ID register. When the Select-with-ATN command is issued, the WD33C93A begins bus arbitration. If the WD33C93A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x Hex) is generated.

Should the WD33C93A win the arbitration, SEL- and ATN- are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then BSY- is deasserted. At this time, a timeout sequence whose length is determined by the value in the Timeout Period register begins. If BSY- is not asserted by the Target before a timeout occurs, the WD33C93A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select-with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the WD33C93A negates the Sel- signal, putting the WD33C93A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the WD33C93A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the WD33C93A is disconnected from the bus and a "paused/aborted" interrupt is generated.

7.5.2 SELECT-WITHOUT-ATN (07 HEX)

The Select-without-ATN command is identical to the Select-with-ATN command except that ATN- is not set during the Selection Phase.

7.5.3 RESELECT (05 HEX)

The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the WD33C93A being Connected as a Target.

7.5.4 RECEIVE (10–13 HEX)

There are four RECEIVE commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of Receive command selected determines the state of the I/O-, C/D-, and MSG- outputs during the command according to the following chart below (1 = asserted).

The Receive commands are information transferrring commands and are therefore dependent on the SBT bit in the Command register for determination of a successful completion. In addition to a termination caused

RECEIVE COMMAND TYPE	OPCODE	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

by reset (via either a Reset command being issued or assertion of the MR- pin), a Receive command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT = 1 or the Transfer Count register is loaded with zero) and a single byte has been read from the Data register; (2) The counter has decremented to zero (with SBT = 0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the received data bytes (and HSP = 1); (4) The ATN- pin is asserted (and HA = 1); (5) The Abort command is issued; or (6) A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the Transfer Count register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the WD33C93A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the Control register for the Data register accessing mode. These bits determine whether the Data register accesses will be handled by the processor or through a DMA/WD interface. When the processor is required to read the Data register (i.e. DMA mode select bits = 0), it must monitor the DBR status bit (in Auxiliary Status) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the Data register and set when a byte is loaded into the Data register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the Synchronous Transfer register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

7.5.5 SEND (14–17 HEX)

As in the case of the RECEIVE commands, there are four Send commands which are distinguished only by the state of the I/O-, C/D-, and MSG- pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular commands as follows shown in the chart below (asserted = 1).

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the Command register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Send command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT = 1 or the Transfer Count register is loaded with zero) and a single byte has been read from the Data register; (2) The counter has decremented to zero (with SBT = 0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the data bytes from the host (and HHP = 1); (4) The ATN- pin is asserted (and HA = 1); (5) The Abort command is issued; or (6) A Disconnect command is issued. The WD33C93A remains Connected-As-A-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, Data register accessing is controlled by the DMA mode select bits in the Control register. When these bits are set to the appropriate mode, loading of the Data register is accomplished by a DMA controller or through the WD-Bus interface. If the DMA mode select bits are zero, the processor must poll the Auxiliary Status register and can write to the Data register only when the Data Buffer Ready bit is set (DBR = 1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the Data register and set when a byte is transferred from the Data register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

7.5.6 TRANSFER (20 HEX)

Transfer Info is used to send and receive data, command, status, and message information.

SEND	COMMAND TYPE	OPCODE	MSG	C/D	I/O
Send	Status	14	0	1	1
Send	Data	15	0	0	1
Send	Message In	16	1	1	1
Send	Unspecified Info In	17	1	0	1

The first Req- assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI Status register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the WD33C93A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when the Transfer Info command completion is to be dependent upon the internal transfer counter, the processor should load the Transfer Count register prior to issuing this command. The DMA mode select bits in the Control register, the offset and transfer period bits in the Synchronous Transfer register, and the SBT bit in the Command register are used during Transfer Info commands just as they are during the Send-And-Receive commands. However, for processor access of the Data register during Transfer Info commands (when the DMA mode select bits are zero, or the bus phase is other than Data phase), behavior of the Data Buffer Ready (DBR) status bit is determined by the direction of information transfer as defined by the I/O- pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the Data register and is set when the byte is transferred from the Data register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the Data register and is reset by reading the Data register. DBR is also reset whenever a Transfer Info command is issued.

There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect or Abort command. The Abort command will cause a "paused/aborted" interrupt to be generated after execution (leaving the WD33C93A in a connected state), while the Disconnect command causes an immediate disconnect and does not generate an interrupt.

A Transfer Info command will be either completed or paused when the specified number of bytes (either a single byte or multiple bytes as defined by the Single-Byte Transfer bit in the Command register) have been sent or received. The WD33C93A generates a "successful completion" interrupt only after receiving another REQ- from the Target during non-Message In information phases, but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional REQ- (Note that when the completed Transfer Info command was a Message-In transfer phase, the ACK- pin will be left asserted by the WD33C93A in the last REQ-ACK cycle of the command, and the processor is required to issue a negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message respectively).

If a parity error is detected on a data byte received from the SCSI bus (and HSP = 1), or on a data byte received from the host (and HHP = 1), then the WD33C93A will terminate the command and, for SCSI parity errors, will leave ACK- asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, negation of the BSY- signal (i.e. the Target suddenly disconnects) or a transition in the I/O-, C/D-, and/or MSG- pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP = 0 or HHP = 0, as appropriate), the WD33C93A will still set the Parity Error status bit in the Auxiliary Status register but will not terminate the command as a result of this error.

7.5.7 TRANSLATE ADDRESS (18 HEX)

The Translate Address Command is used to perform a logical-to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can reload the logical address into the WD33C93A Logical Address register and then issue the Translate Address command to have the WD33C93A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read three WD33C93A registers to extract the Cylinder Number, Head Number, and Sector Number corresponding to the logical address. The disk parameters contained in the Total Sectors, Total Heads, and Total Cylinders registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the WD33C93A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded in the Head Number and Cylinder Number registers respectively. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

7.6 COMBINATION LEVEL II COMMANDS

7.6.1 SELECT-AND-TRANSFER (08 AND 09 HEX)

The Select-And-Transfer commands are capable of greatly reducing the host or local processor interrupt-handling burden by enabling the WD33C93A's internal microprocessor to manage the low-level SCSI protocol.

This results in as few as one interrupt per SCSI operation. Select-And-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases: (1) Selection of a Target device; (2) Sending of a command; (3) Reception of status information; and (4) Reception of a Command Complete Message. These commands optionally consist of a Data Transfer phase and additional Message Transfer phases. During execution of a Select-And-Transfer command, the Command Phase register will be updated to indicate which bus phases of the SCSI operation have been completed, so that upon completion or termination of the command, the WD33C93A may be interrogated to find out where the SCSI operation was stopped.

The two Select-And-Transfer commands are distinguished from each other only by whether or not the ATN- pin is asserted during the Selection phase. Select-And-Transfer commands directly support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte) SCSI commands. In addition, the ability to have ATN- asserted during Selection supports the SCSI Message Protocol which calls for an Identify Message Out phase following the Selection. When the Select w/Atn-And-Transfer commands is issued, the WD33C93A expects the first information phase request from the Target to be a Message Out phase, whereas for a Select w/o Atn-and-Transfer command, the first information phase request is expected to be a Command Out phase.

When a Select-And-Transfer command is issued, the WD33C93A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-And-Transfer command is terminated and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the Command Phase register contains all zeroes. If the Selection is successful, no interrupt is generated, but the Command Phase register will be set to a Hex 10.

After completing the Selection phase, the WD33C93A begins an information transfer phase. If ATN- has been asserted (i.e. a Select w/Atn-And-Transfer command was issued), the WD33C93A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the WD33C93A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the WD33C93A will respond by automatically sending an Identify Message. This single byte message is of the binary form: 1r000ttt, where r = 1 if the Enable Reselect bit in the Source ID register is equal to 1, and ttt is the encoded Target Logical Unit Number contained in the Target LUN register. Once the Identify Message has been sent, the WD33C93A will set the Command Phase register to Hex 20.

Following the Message Out phase (or Selection phase when ATN- was not asserted during Selection), a Command phase is expected by the WD33C93A. Again, and throughout the entire Select-And-Transfer command execution, if the Target requests an unexpected information phase type, the WD33C93A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the WD33C93A will extract the SCSI command from the internal Command Descriptor Block registers and send 6, 10, or 12 bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The Command Phase register is set to Hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the Command Phase register will contain Hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the WD33C93A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The WD33C93A therefore expects to receive either a Save Data Pointer Message (Hex 02) or a Disconnect Message (Hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the Data register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save Data Pointer message is received, a "paused/aborted" interrupt is generated and the Select-And-Transfer command terminated to allow the processor to save the SCSI data pointers. However, if a Disconnect message is received, the Command Phase register will be updated to Hex 42 and command execution continues.

When the actual Target-disconnection does occur, the Command Phase register is updated to Hex 43 and if the IDI bit is set, the WD33C93A terminates the Select-And-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the WD33C93A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the WD33C93A, a "terminated" interrupt is generated. However, if the original Target Reselects the WD33C93A, no interrupt is generated and the Command Phase register is set to Hex 44.

Following the original Target Reselection, the WD33C93A expects a Message In phase which should consist of the Target sending an Identify Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target Lun. If the data received by the WD33C93A is different or the Target Lun specified in this byte does not match the contents of the Target Lun register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct Identify Message In phase results in the Command Phase register being updated to Hex 45.

After the Identify Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase,

or Status phase should occur. If the Transfer Count register contains any non-zero value, then the WD33C93A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the WD33C93A will use the Transfer Count register to determine the number of bytes to be transferred, and all host-side Data register accesses will be accomplished via the method selected by the DMA mode select bits in the Control register. When the internal counter reaches zero, the Data Transfer phase is complete and the Command Phase register is set to Hex 46.

Note that any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The Command Phase register will cycle through the disconnect phases (41-45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the WD33C93A following the Data Transfer phase (or instead of the Data Transfer phase when the Transfer Count register contains a value of zero). At the start of the Status phase, the Command Phase register is loaded with Hex 47. Upon completion of the Status phase, the Command Phase register will be updated to Hex 50, and the received status byte is stored in the Target Lun register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The WD33C93A expects the Target to send a Command Complete Message (Hex 00) to indicate that the SCSI command operation has been completed. After the WD33C93A receives this Command Complete Message, the Command Phase register advances to Hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the Target Lun register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when another REQ- is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion; interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-And-Transfer commands, an abnormal or unexpected condition will cause the WD33C93A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the WD33C93A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the WD33C93A being in a Disconnected state. Transfer

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The WD33C93A is in the disconnected state.
10	The Target has been selected. The WD33C93A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save Data Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The WD33C93A is now in the disconnected state.
44	The WD33C93A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The WD33C93A is now in the connected as an Initiator state.
45	The WD33C93A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The WD33C93A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The WD33C93A has successfully received a Command Complete message from the Target.

COMMAND PHASE	MEANING
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun (REQ- asserted).
41	Resume after Command phase or after Save Data Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data phase has been completed, expecting Status phase or a Save Data Pointer/Disconnect Message In phase. An implied Negate ACK does not occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the Command Phase register can take during the **Select-And-Transfer** commands, and their meanings relative to command termination:

A "Resume Select-And-Transfer" command is assumed whenever a normal "Select-And-Transfer" command is issued while the WD33C93A is in the Connected-Initiator state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Select-And-Transfer command execution. This feature, in conjunction with the Intermediate Disconnect Interrupt enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The table above briefly describes the valid settings of the Command Phase register when resuming a Select-And-Transfer command:

7.6.2 RESELECT-AND-TRANSFER (0A AND 0B HEX)

The Reselect-And-Transfer commands include the Reselect-and-Receive Data and the Reselect-and-Send Data commands. These commands cause the WD33C93A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the Control Register; and the SCC bit in the Destination ID register. The SCSI bus phase sequences are summarized below. Refer to the command descriptions of the Send-Status-And-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

(1) Reselect-and-Receive command, EDI = 0, and SCC = don't care:
- Reselection phase;
- Send Identify Message In;
- Receive Data Out phase;
- Completion interrupt.

(2) Reselect-and-Send command, EDI = 0, and SCC = don't care:
- Reselection phase;
- Send Identify Message In;
- Receive Data In phase;
- Completion interrupt.

(3) Reselect-and-Receive command, EDI = 1, and SCC = 0:
- Reselection phase;
- Send Identify Message In;
- Receive Data Out phase;
- Chain to Send-Status-and-Command Complete.

(4) Reselect-and-Send command, EDI = 1, and SCC = 0:
- Reselection phase;
- Send Identify Message In;
- Receive Data In phase;
- Chain to Send-Status-And-Command Complete.

(5) Reselect-and-RCV command, EDI = 1, and SCC = 1:
- Reselection phase;
- Send Identify Message In;
- RCV Data Out phase;
- Chain to Send-Disconnect-Message.

(6) Reselect-and-Send command, EDI = 1, and SCC = 1:

- Reselection phase;
- Send Identify Message In;
- Send Data In phase;
- Chain to Send-Disconnect-Message.

If the reselection attempt times out during a Reselect-And-Transfer command, ATN- is asserted and HA = 1, or if a parity error is detected on an incoming data byte (and HSP = 1 or HHP = 1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the Command Phase register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI = 0, then a "successful completion" interrupt would be generated at this point. However, if EDI = 1, no interrupt is generated and command chain occurs (as described above).

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The WD33C93A is in the disconnected state.
10	The WD33C93A has successfully reselected the Initiator. The WD33C93A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

The following table summarizes the possible values that the Command Phase register can take during the Reselect-And-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

A "Resume Reselect-And-Transfer" command is assumed whenever a normal "Reselect-And-Transfer" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Reselect-And-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Reselect-And-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify Message Out; start with data transfer phase. If Transfer Count is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.6.3 WAIT-FOR-SELECT-AND-RECEIVE (0C HEX)

The Wait-For-Select-And-Receive causes the WD33C93A to idle until it is selected by an Initiator, at which time the WD33C93A will enter the Target mode and message and command information will automatically be requested. As an option, the WD33C93A may be programmed to disconnect when a SCSI read command is received while executing a Wait-For-Select-And-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If ATN- was asserted by the Initiator during the selection phase, the WD33C93A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (Hex addresses 03 to 0E), and if a valid Identify message is received, it will be saved in the Target Lun register (Hex address 0F). The number of command bytes requested by the WD33C93A is determined by the SCSI group code in the first byte of the CDB.

After the WD33C93A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-For-Select-And-Receive command, the WD33C93A is enabled to perform an automatic disconnect when a SCSI read command is received. There-

fore, when EDI=1 and the 1st CDB byte received contains a 6, 10 or 12 byte read command code, then the WD33C93A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the Command Phase register should be read to determine which phase of the Wait-For-Select-And-Receive command was last completed before the error condition occurred. A Command Phase Hex value of Hex 10 indicates that the WD33C93A was successfully selected. A Hex value of 20 indicates that a message was received from the Initiator, and when the WD33C93A begins receiving command bytes, the Command Phase is set to Hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the Command Phase register can take during the Wait-For-Select-And-Receive command, and their meanings relative to command termination. See other command descriptions for additonal values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The WD33C93A has not been selected. The WD33C93A is in the disconnected state.
10	The WD33C93A has been successfully selected by the Initiator. The WD33C93A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The WD33C93A has begun command phase by setting the SCSI bus phase signals and asserting REQ-.
31	The WD33C93A has transferred 1 command byte from the Initiator. The SCSI Status may indicate the need for the host to load the command size into the OWN ID register.
3x	The WD33C93A has transferred x command bytes from the Initiator.

A "Resume Wait-For-Select-And-Receive" command is assumed whenever a normal "Wait-For-Select-And-Receive" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Wait-For-Select-And-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Wait-For-Select-And-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the Initiator is complete: start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the Target Lun register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the WD33C93A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the Own ID register.

7.6.4 SEND-STATUS-AND-COMMAND-COMPLETE (0D HEX)

The Send-Status-And-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-And-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs. Note that the bits used by the WD33C93A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the Command Phase register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

(1) CDB12 bit0 = 0, bit1 = don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 Hex). A "successful completion" interrup now occurs.

(2) CDB12 bit0 = 1, bit1 = 0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A Hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. WD33C93A command execution proceeds as described for that command.

(3) CDB12 bit0 = 1, bit1 = 1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (OB Hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. WD33C93A command execution proceeds as described for that command.

A Send-Status-And-Command-Complete command may be terminated by ATN- asserted when HA = 1, or when a Disconnect or Reset command is issued. In addition, it may be aborted on a SCSI bus-phase boundary by issuing an Abort command.

The following table summarizes the possible values that the Command Phase register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-And-Command-Complete" command is assumed wheneve a normal "Send-Status-And-Command-Complete" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Send-Status-And-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Send-Status-And-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

7.6.5 SEND-DISCONNECT-MESSAGE (0E HEX)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save Data Pointers message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The Command Phase register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save Data Pointers message is sent, the Command Phase will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the Command Phase register will contain a 43H.

A Send-Disconnect-Message command may be terminated by ATN- asserted when HA = 1, or when a Disconnect or Reset command is issued. In addition, it may be aborted on a SCSI bus-phase boundary by issuing an Abort command.

The following table summarizes the possible values that the Command Phase Register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
41	The Save Data Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The WD33C93A is now in the disconnected state.

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND	−0.5V to +7.0V
Operating temperature	0 to 70 degrees C
Storage temperature	−55 to +125 degrees C
Power dissipation	500 mW
Input Static Discharge Protection	1200 V pin to pin

DC OPERATING CHARACTERISTICS

Ta = 0 to 70 deg. C
VCC = +5V +/− .25V, GND = 0V

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
IIL	INPUT LEAKAGE		10	uA	VIN = .4 TO VCC
IOL1	SCSI OUTPUT LEAKAGE (INACTIVE)		50	uA	VOUT = .5 TO VCC
IOL2	OUTPUT LEAKAGE (TRI-STATE)		10	uA	VOUT = .4 TO VCC
VIH	INPUT HIGH VOLTAGE	2.0		V	
VIL	INPUT LOW VOLTAGE		0.8	V	
VIHYS	SCHMITT TRIGGER INPUT HYSTERISIS (ALL SCSI PINS)	0.2		V	
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IO = −400 uA
VOL1	SCSI OUTPUT LOW VOLTAGE		0.5	V	IO = 48.0 mA
VOL2	OUTPUT LOW VOLTAGE (ALL OTHERS)		0.4	V	IO = 4.0 mA
ICC	SUPPLY CURRENT		20	mA	Ta = +25 deg. C

9. TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the SCSI bus timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

$$Tcyc = \frac{Ticlk * DIVISOR}{2}$$

Where:

Tcyc is the internal clock cycle time;

Ticlk is the period of the clock at the MCK input;

DIVISOR is the clock divisor selected in the OWN ID register.

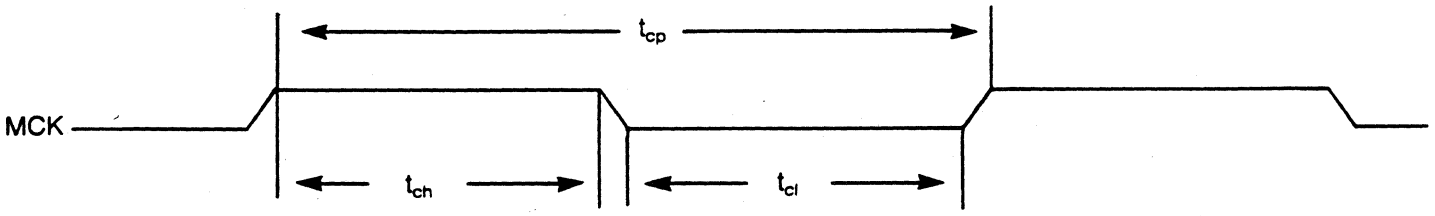
For example, with a 16MHz clock input to the WD33C93A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

$$Tcyc = \frac{62.5\ nsec * 4}{2} = 125\ nsec$$

9.1 PROCESSOR/DMA INTERFACE

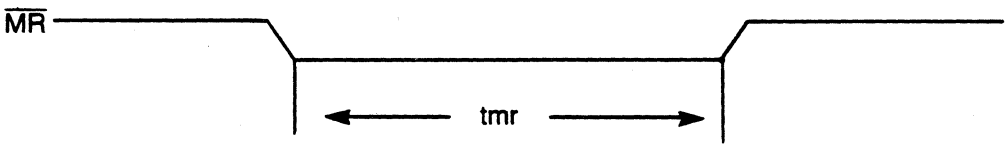
9.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{cp}	CLOCK PERIOD	62.5	125	ns
t_{ch}	CLOCK HIGH	28		ns
t_{cl}	CLOCK LOW	28		ns



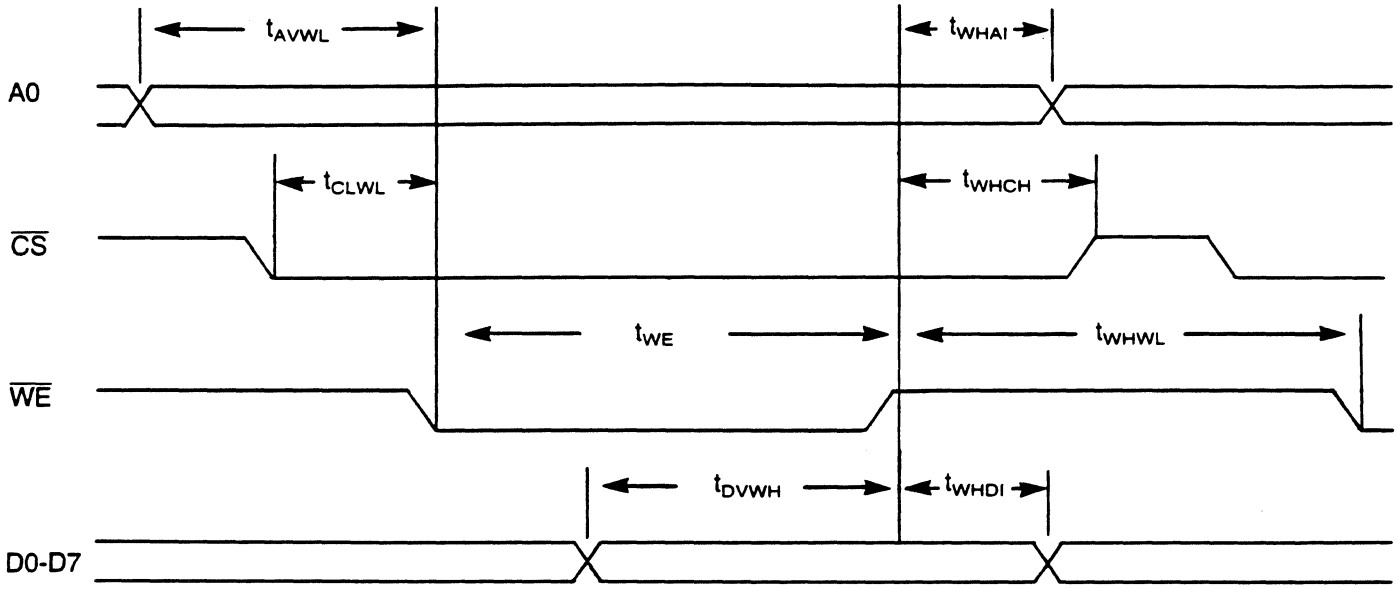
9.1.2 $\overline{MR}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	$\overline{MR}$ PULSE WIDTH	1		us



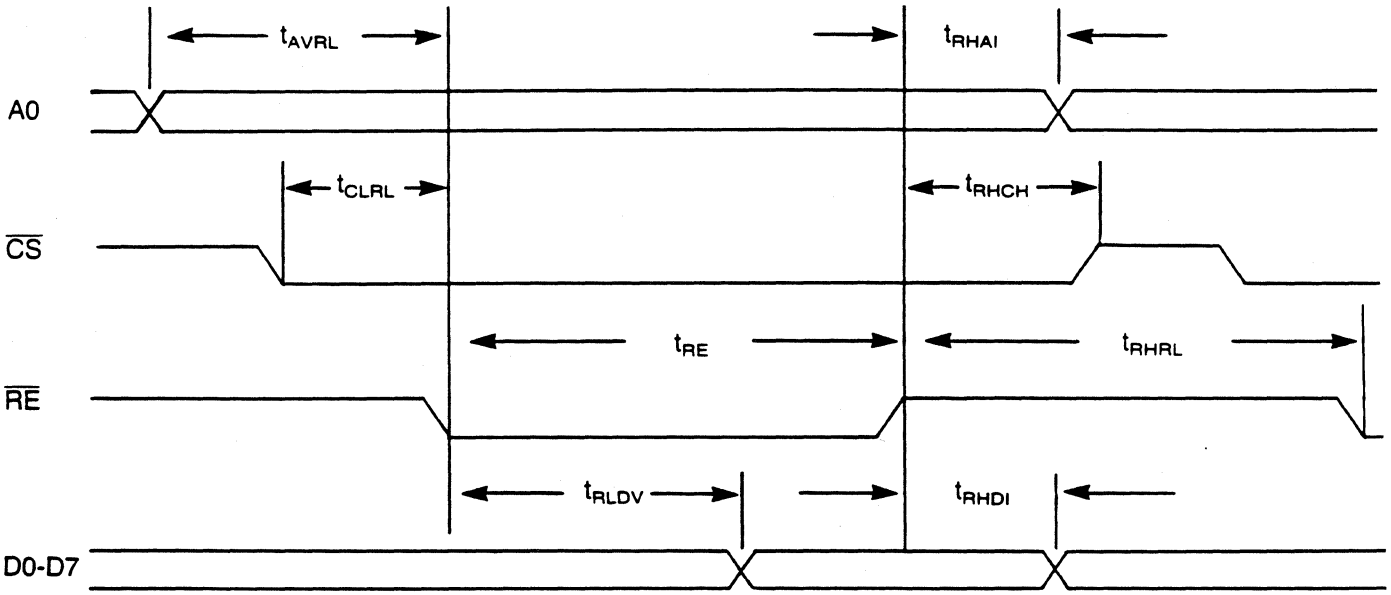
9.1.3 PROCESSOR WRITE — INDIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{avwl}	ADDR VALID TO $\overline{WE}$ LOW	0		ns
t_{clwl}	$\overline{CS}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{we}	$\overline{WE}$ PULSE WIDTH	120		ns
t_{dvwh}	$\overline{DATA\ VALID\ TO}$ WE HIGH	70		ns
t_{whai}	$\overline{WE}$ HIGH TO ADDR. INVALID	0		ns
t_{whch}	$\overline{WE}$HIGH TO $\overline{CS}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns



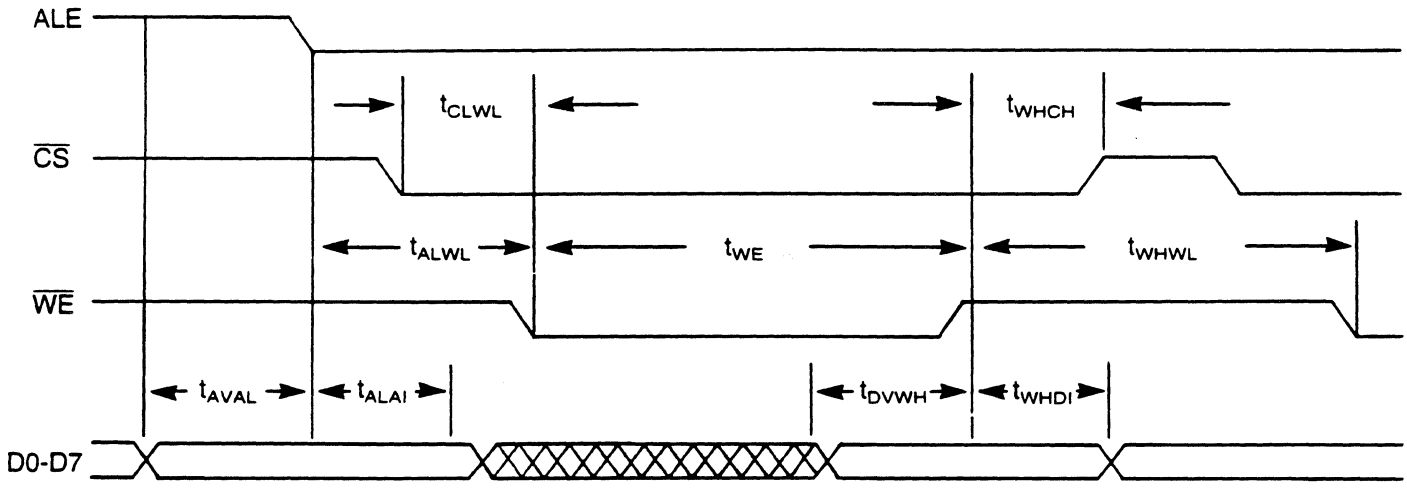
9.1.4 PROCESSOR READ — INDIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{avrl}	ADDR VALID TO $\overline{RE}$ LOW	0		ns
t_{clrl}	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{re}	$\overline{RE}$ LOW TO DATA VALID	180	10000	ns
t_{rldv}	$\overline{RE}$ PULSE WIDTH LOW TO DATA VALID	180	180	ns
t_{rhch}	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10	40	ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns
t_{rhai}	$\overline{RE}$ HIGH TO A0 INVALID	0		ns



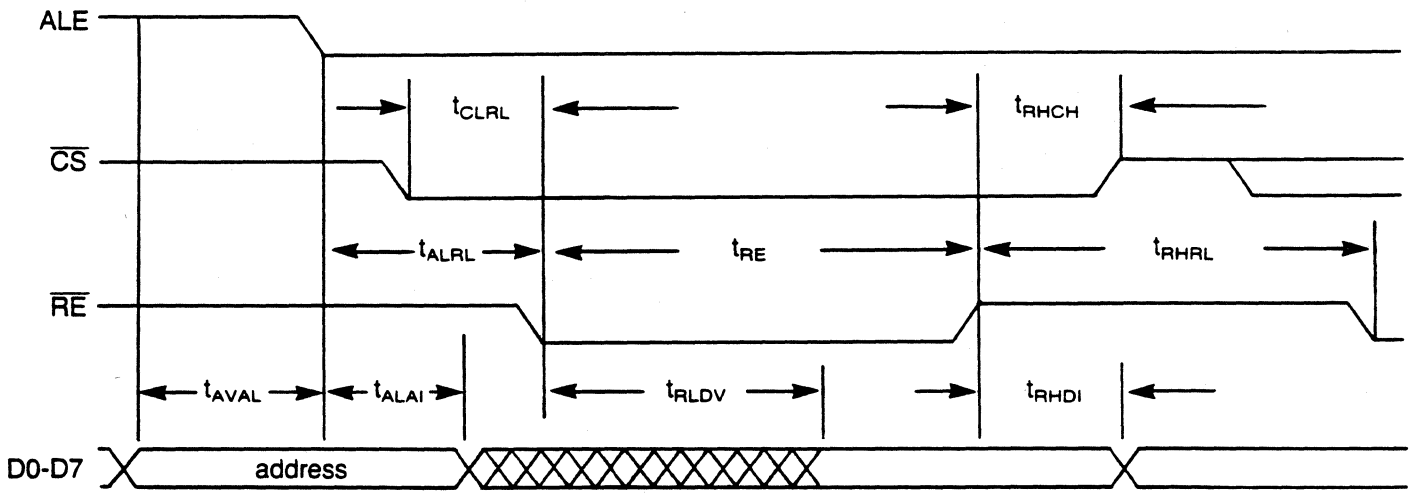
9.1.5 PROCESSOR WRITE — DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{aval}	ADDR VALID TO $\overline{ALE}$ LOW	40		ns
t_{alai}	ALE LOW TO ADDR INVALID	0		ns
t_{alwl}	ALE LOW TO $\overline{WE}$ LOW	90		ns
t_{clwl}	$\overline{CS}$LOW TO $\overline{WE}$ LOW	0		ns
t_{we}	$\overline{WE}$ PULSE TO $\overline{WE}$ HIGH	120		ns
t_{dvwh}	DATA VALID TO $\overline{WE}$ HIGH	70		ns
t_{whch}	$\overline{WE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns



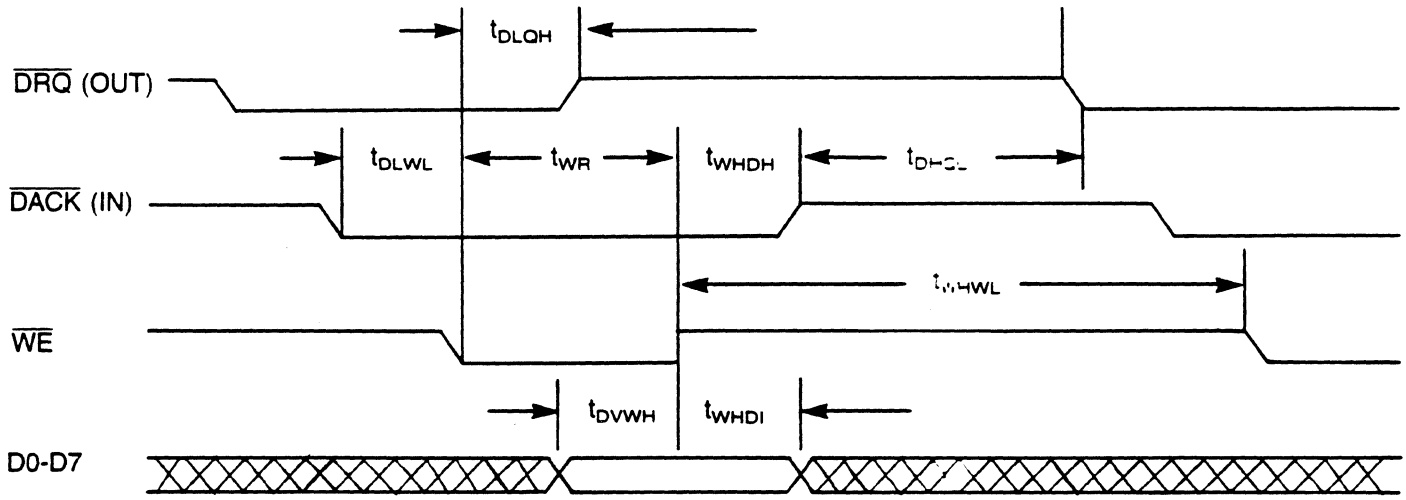
9.1.6 PROCESSOR READ — DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{aval}	ADDR VALID TO $\overline{ALE}$ LOW	40		ns
t_{alai}	ALE LOW TO ADDR INVALID	0		ns
t_{alrl}	ALE LOW TO $\overline{RE}$ LOW	30		ns
t_{clrl}	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{re}	$\overline{RE}$ PULSE WIDTH	180	10000 ns	
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		180	ns
t_{rhch}	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10	40	ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns



9.1.7 DMA WRITE

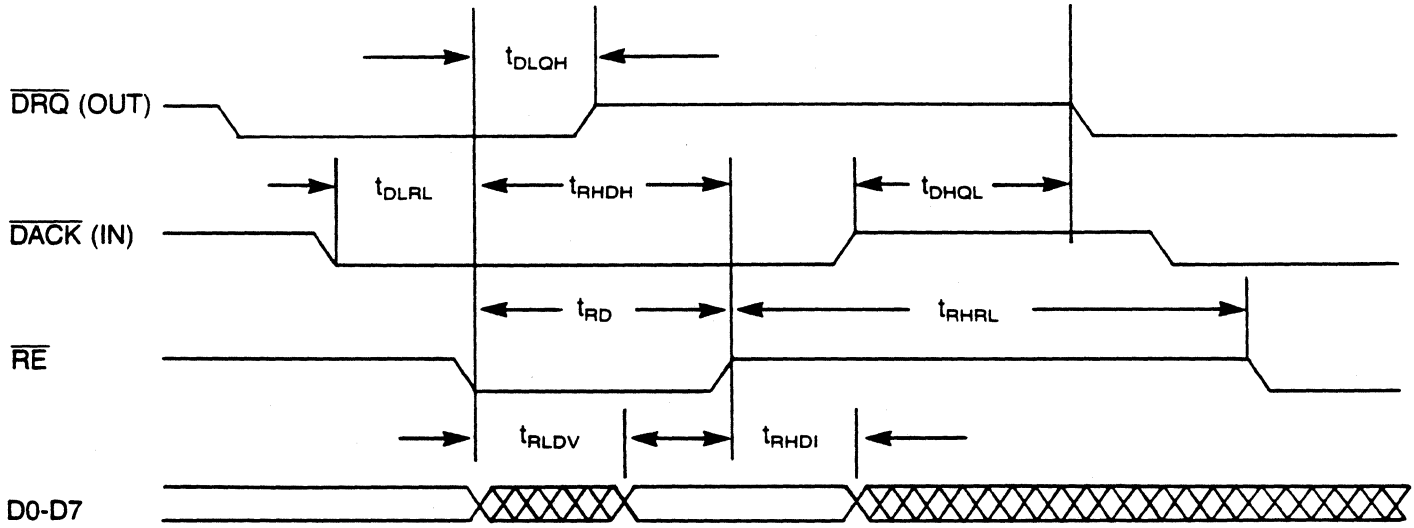
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlwl}	$\overline{DACK}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{dlqh}	$\overline{DACK}$, $\overline{WR}$ LOW TO $\overline{DRQ}$ HIGH	40	90	ns
t_{wr}	$\overline{WE}$ PULSE WIDTH	50		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	100		ns
t_{dvwh}	DATA VALID TO $\overline{WE}$ HIGH	25		ns
t_{whdh}	$\overline{WE}$ HIGH TO DACK HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{dhql}	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	30		ns



NOTE: External load on $\overline{DRQ}$ & $\overline{DACK}$ is assumed to be 1KΩ.

9.1.8 DMA READ

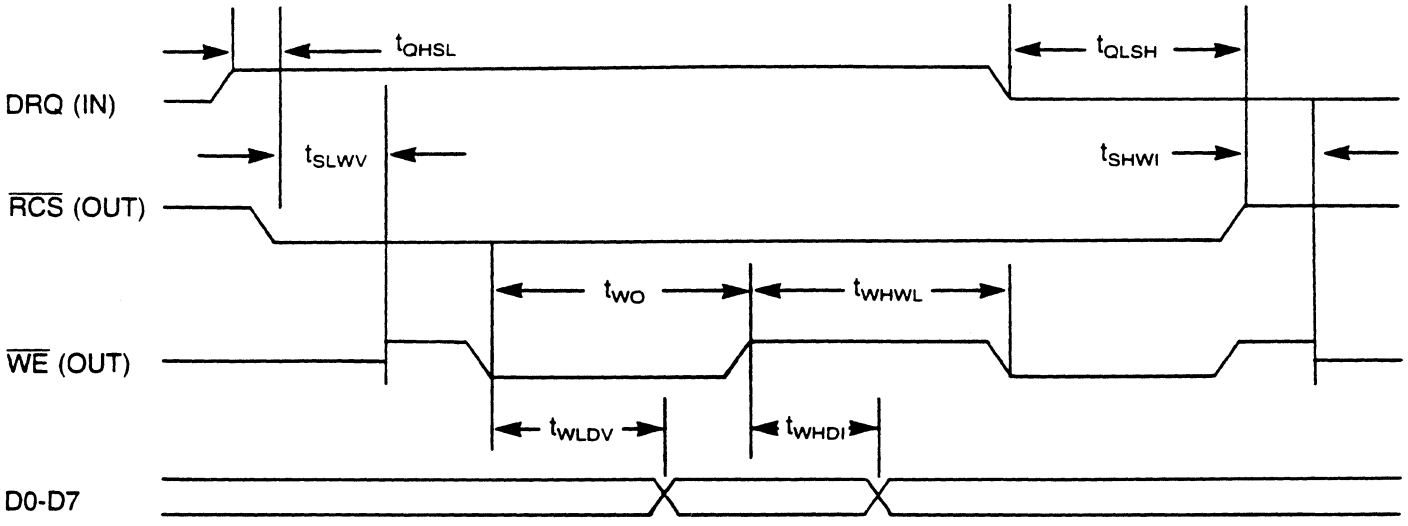
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlrl}	$\overline{DACK}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{dlqh}	$\overline{DACK}$, $\overline{RE}$ LOW TO $\overline{DRQ}$ HIGH	40	90	ns
t_{rd}	$\overline{RE}$ PULSE WIDTH	80		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	100		ns
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		70	ns
t_{rhdh}	$\overline{RE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns
t_{rhdl}	$\overline{DRQ}$ HIGH TO $\overline{DRQ}$ LOW	100		ns
t_{dhql}	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	30		ns



NOTE: External load on $\overline{DRQ}$ & DACK is assumed to be 1KΩ.

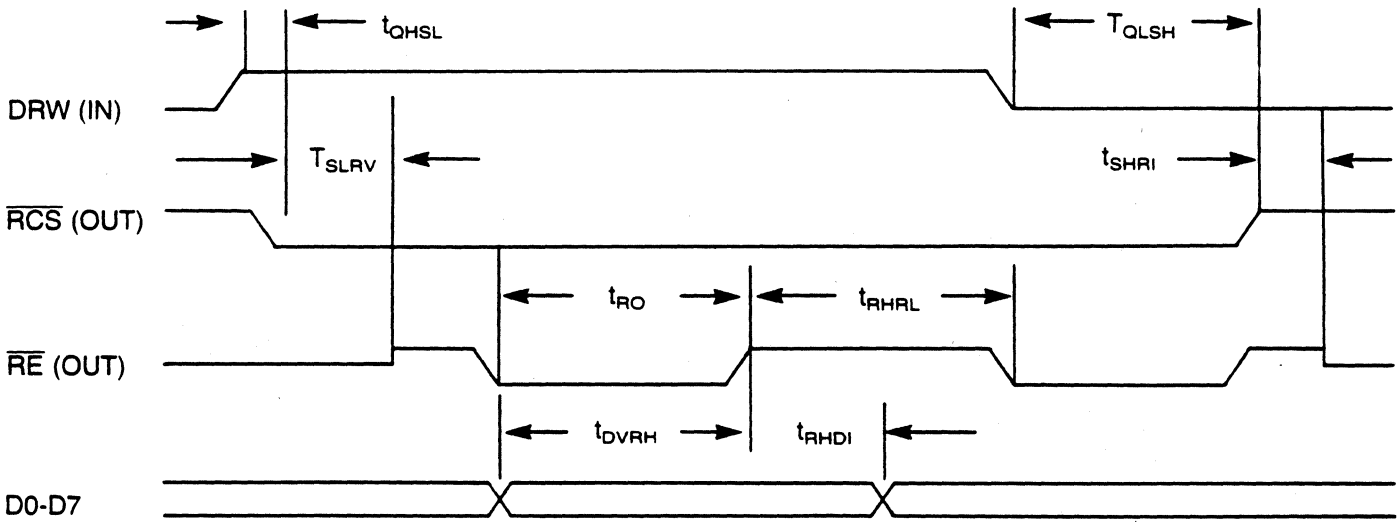
9.1.9 WD-BUS BUFFER WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{qhsl}	DRQ HIGH TO $\overline{RCS}$ LOW	0		ns
t_{slwv}	$\overline{RCS}$ LOW TO $\overline{WE}$ VALID	0	20	ns
t_{wo}	$\overline{WE}$ PULSE WIDTH	Tcyc-20		ns
t_{wldv}	$\overline{WE}$ LOW TO DATA VALID		50	ns
t_{whdi}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	30		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	Tcyc-20		ns
t_{qlsh}	DRQ LOW TO $\overline{RCS}$ HIGH	8*Tcyc	10*Tcyc	ns
t_{shwi}	$\overline{RCS}$ HIGH TO $\overline{WE}$ INVALID	0	100	ns



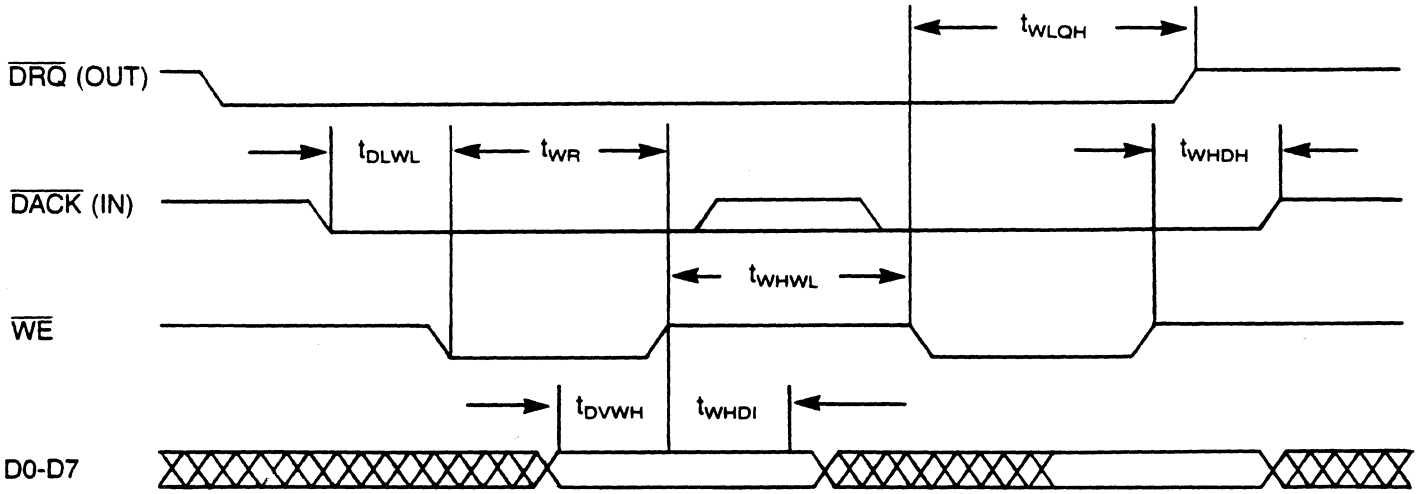
9.1.10 WD-BUS BUFFER READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{qhsl}	DRQ HIGH TO $\overline{RCS}$ LOW	0		ns
t_{slrv}	$\overline{RCS}$ LOW TO $\overline{RE}$ VALID	0	20	ns
t_{ro}	$\overline{RE}$ PULSE WIDTH	Tcyc-20		ns
t_{dvrh}	DATA VALID TO $\overline{RE}$ HIGH	10		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	TCYC-20		ns
t_{qlsh}	DRQ LOW TO $\overline{RCS}$ HIGH	8*Tcyc	10*Tcyc	ns
t_{shri}	$\overline{RCS}$ HIGH TO $\overline{RE}$ INVALID	0	100	ns



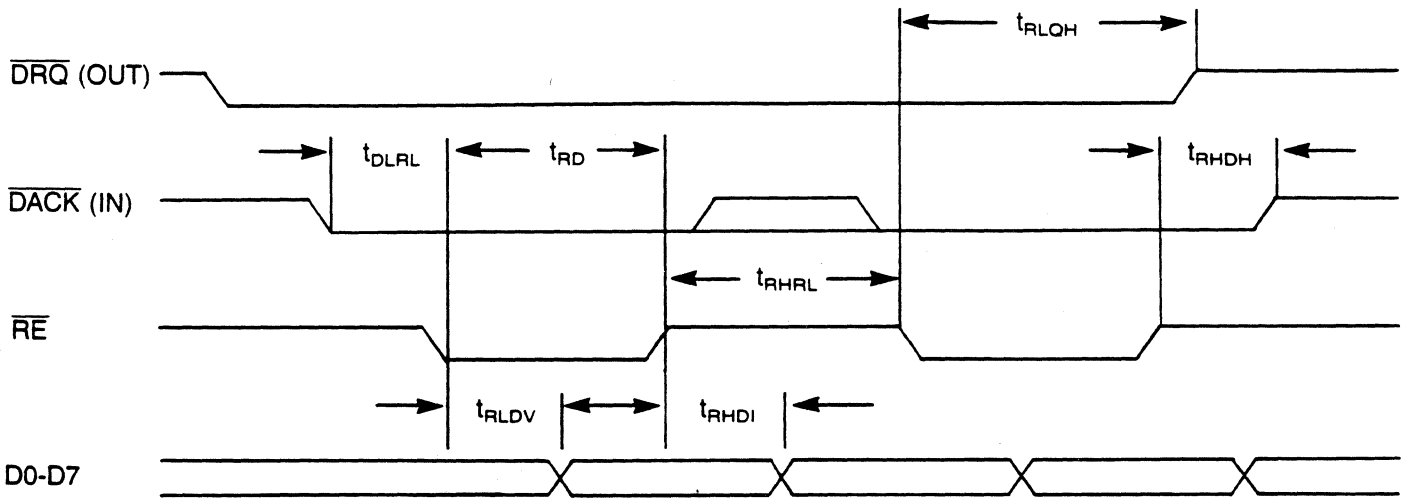
9.1.11 BURST DMA WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlwl}	$\overline{DACK}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{wlqh}	$\overline{WE}$ LOW TO $\overline{DRQ}$ HIGH		75	ns
t_{wr}	$\overline{WE}$ PULSE WIDTH	50		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	80		ns
t_{dvwh}	$\overline{DATA\ VALID\ TO}$ WE HIGH	25		ns
t_{whdh}	$\overline{WE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns



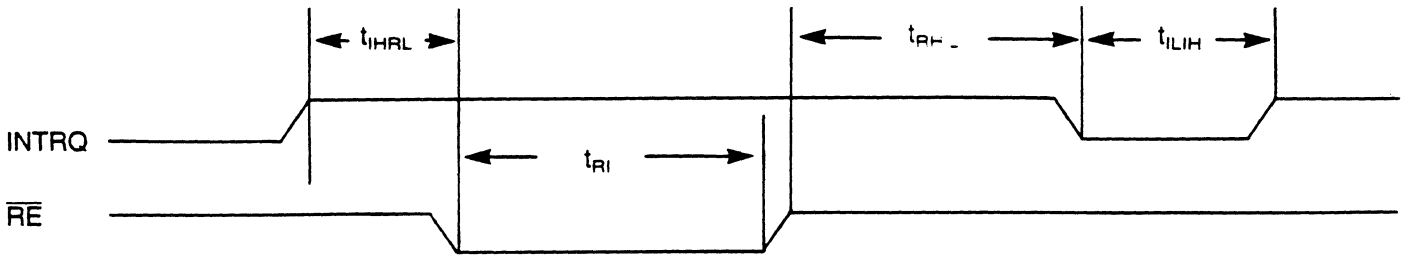
9.1.12 BURST DMA READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlrl}	$\overline{DACK}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{rlqh}	$\overline{RE}$ LOW TO $\overline{DRQ}$ HIGH		75	ns
t_{rd}	$\overline{RE}$ PULSE WIDTH	80		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	80		ns
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		50	ns
t_{rhdh}	$\overline{RE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns



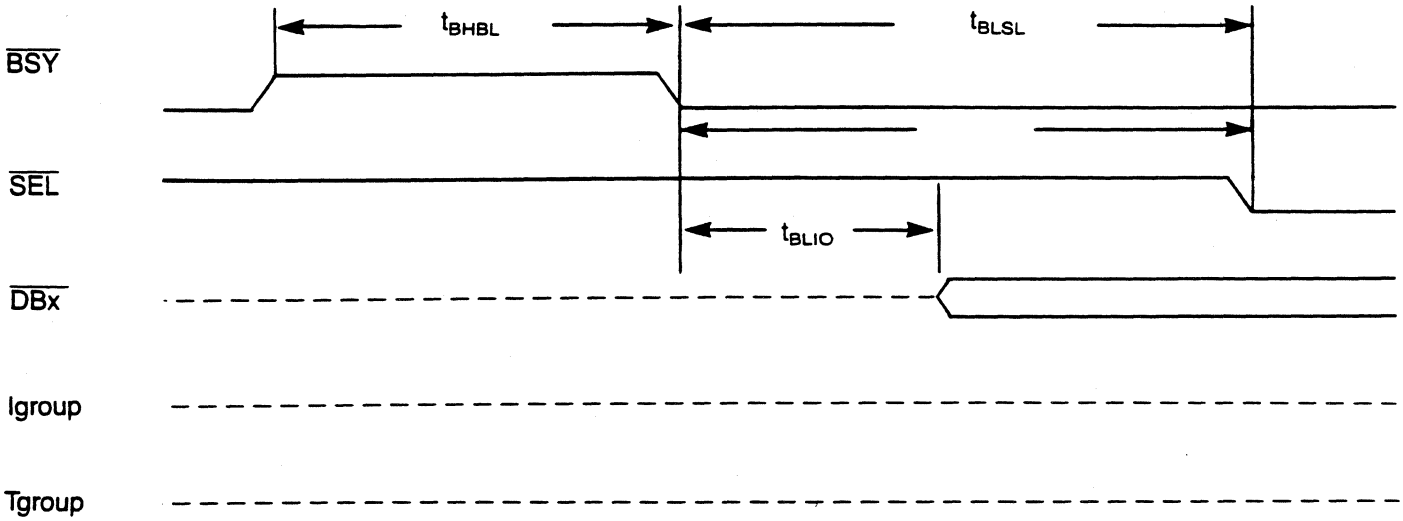
9.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{ihrl}	INTRQ HIGH TO $\overline{RE}$ LOW	0		ns
t_{ri}	$\overline{RE}$ PULSE WIDTH	180		ns
t_{rhil}	$\overline{RE}$ HIGH TO INTRQ LOW	0	100	ns
t_{ilih}	INTRQ LOW TO INTRQ HIGH	100		ns



9.2 SCSI INTERFACE
9.2.1 ARBITRATION

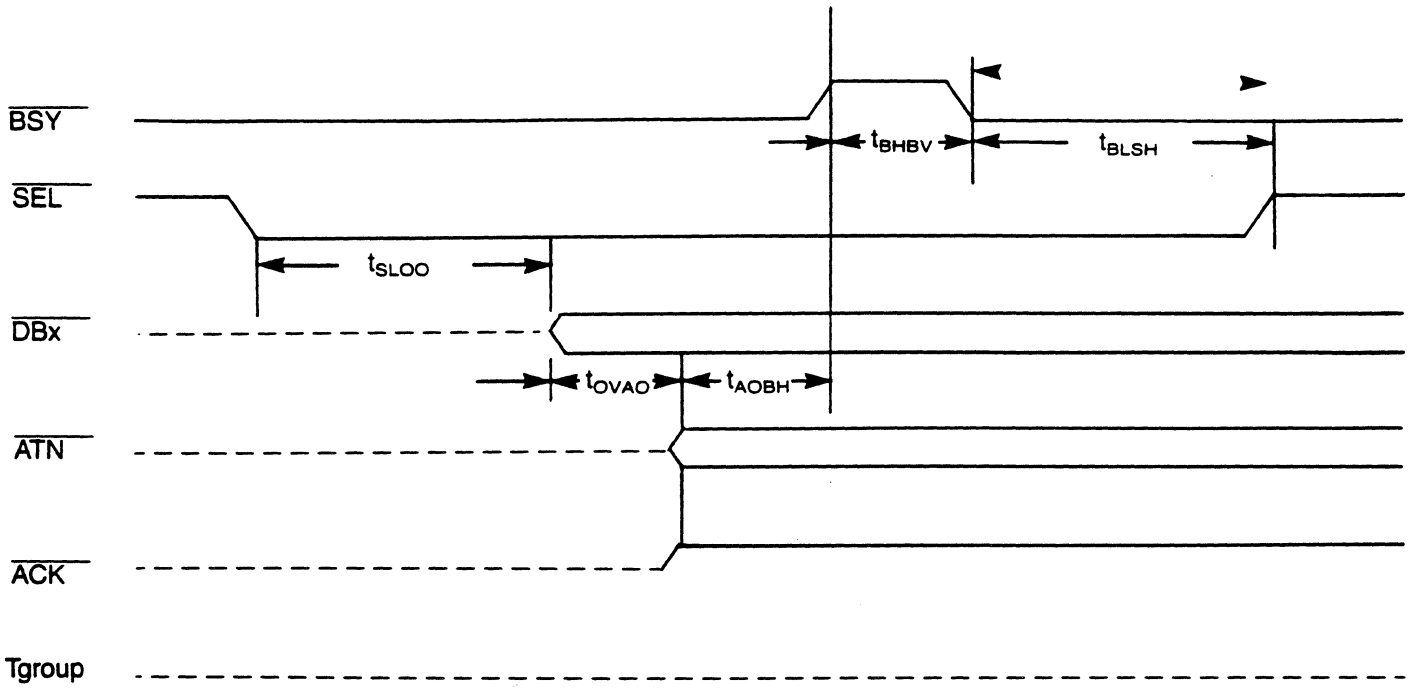
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhbl}	$\overline{BSY}$, $\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT LOW	12*Tcyc	16*Tcyc	ns
t_{blio}	$\overline{BSY}$ OUT LOW TO BUS ID OUT	−50	50	ns
t_{blsl}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ OUT LOW	2.2		us



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

9.2.2 SELECTING A TARGET (AS AN INITIATOR)

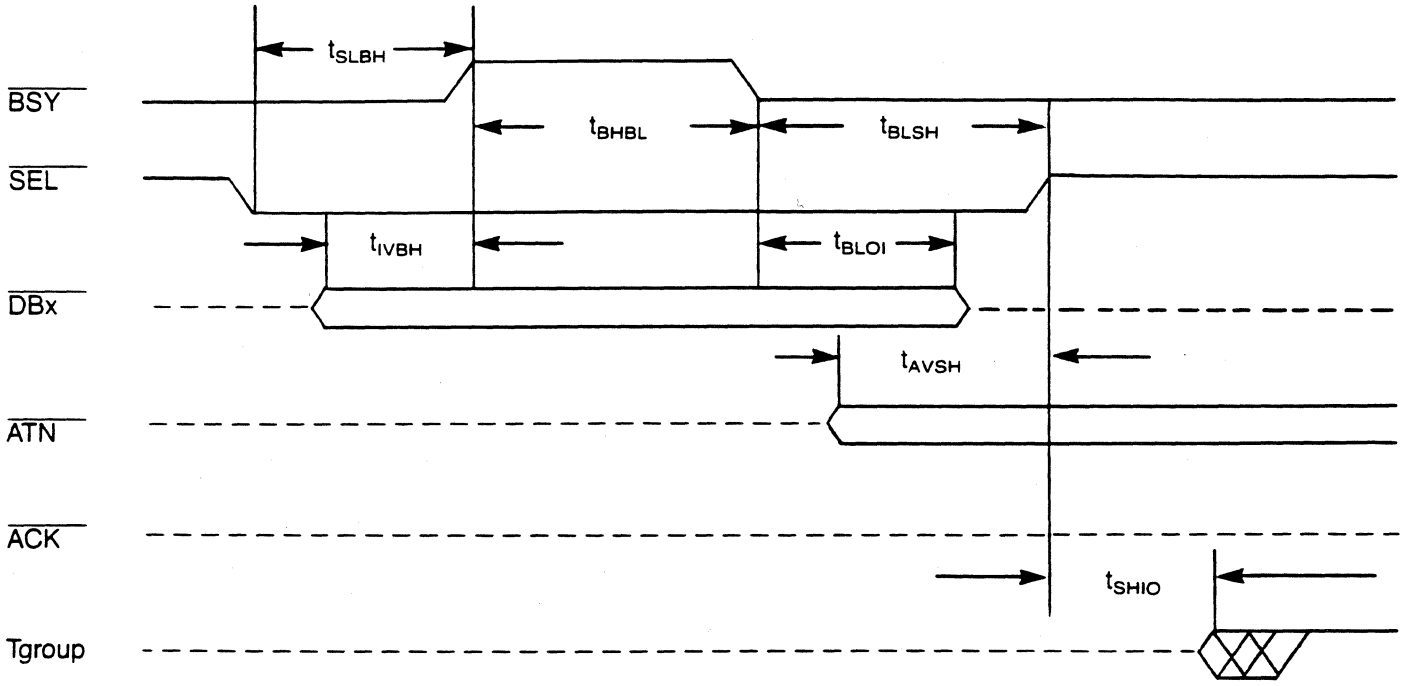
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{sloo}	$\overline{SEL}$ OUT LOW TO "OR-ED" ID OUT	1.2		us
t_{ovao}	"OR-ED" ID OUT VALID TO $\overline{ACK}$, $\overline{ATN}$ OUT	100		ns
t_{aobh}	$\overline{ACK}$, $\overline{ATN}$ OUT VALID TO $\overline{BSY}$ OUT HIGH	100		ns
t_{bhbv}	$\overline{BSY}$ OUT HIGH TO $\overline{BSY}$ IN LOW VALID	400		ns
t_{blsh}	$\overline{BSY}$ IN LOW TO $\overline{SEL}$ OUT HIGH	100		ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

9.2.3 RESPONSE TO SELECTION (AS A TARGET)

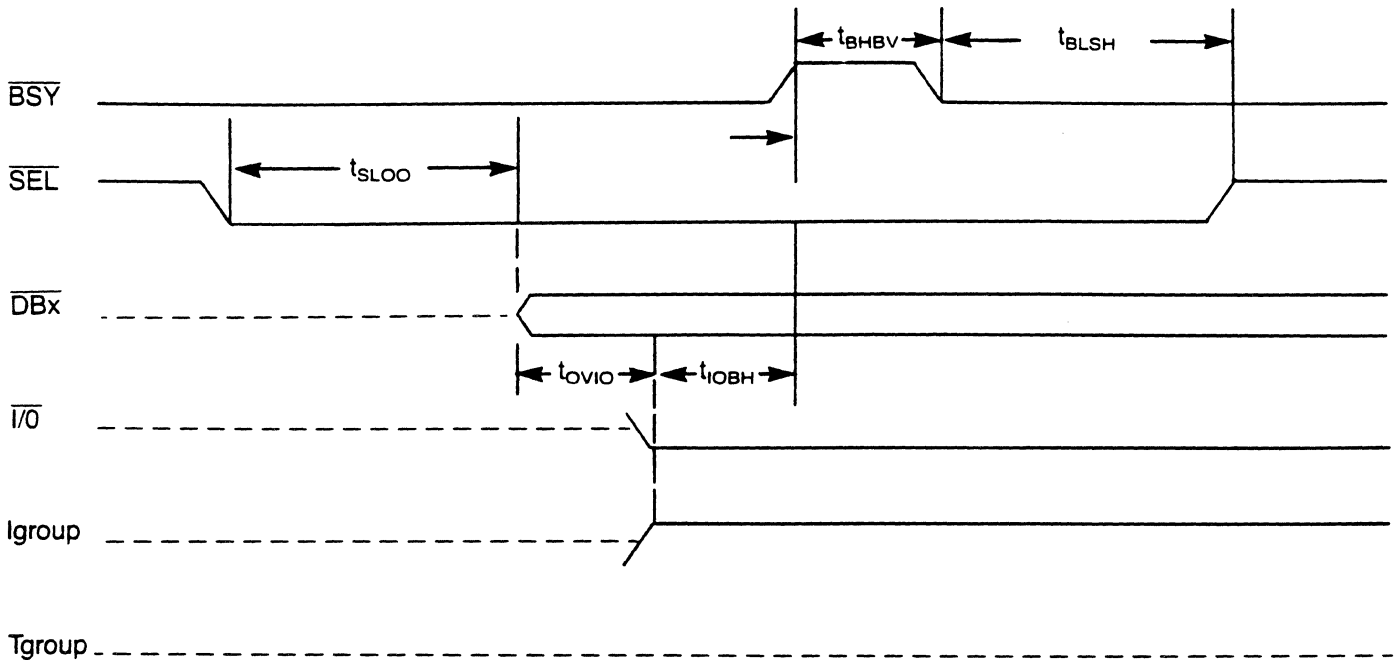
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{ivbh}	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
t_{bhbl}	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO $\overline{BSY}$ LOW	0.4	200	us
t_{bloi}	$\overline{BSY}$ OUT LOW TO "OR-ED" ID INVALID IN	0		ns
t_{blsh}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
t_{avsh}	$\overline{ATN}$ VALID IN TO $\overline{SEL}$ IN HIGH	0		ns
t_{shio}	$\overline{SEL}$ IN HIGH TO Tgroup OUT	100		ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

9.2.4 RESELECTING AN INITIATOR (AS A TARGET)

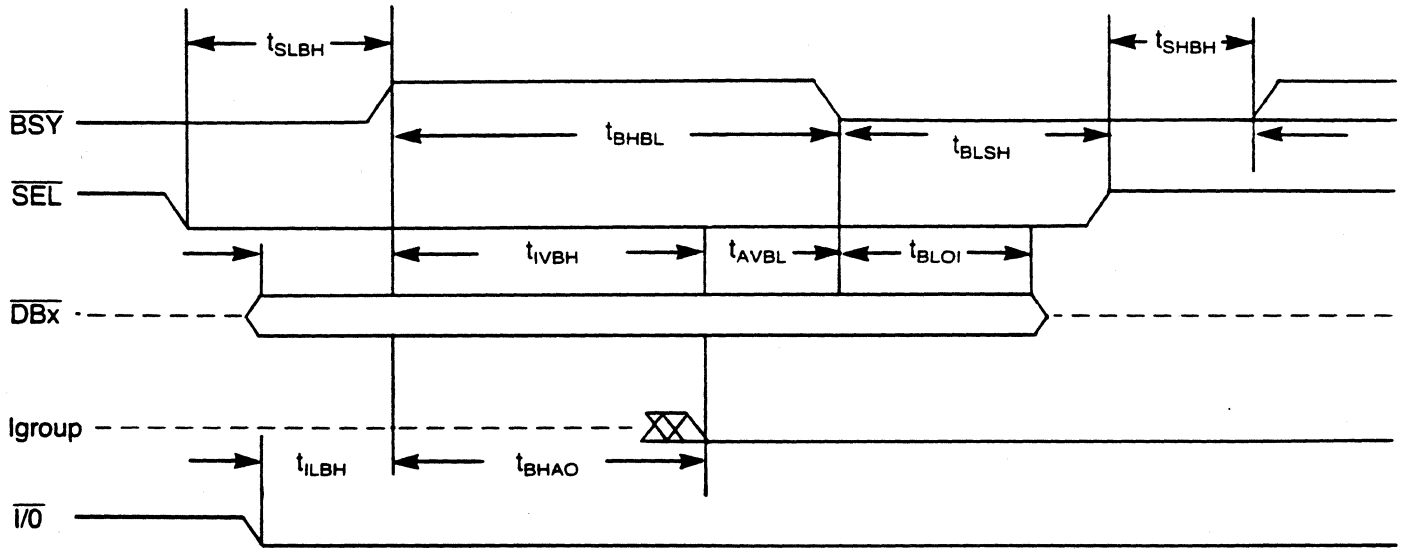
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{sloo}	$\overline{SEL}$ OUT LOW TO "OR-ED" ID OUT	1.2		us
t_{ovio}	"OR-ED" ID VALID TO I/O and Tgroup OUT VALID	100		ns
t_{iobh}	I/O and Tgroup OUT VALID TO $\overline{BSY}$ OUT HIGH	100		us
t_{bhbv}	$\overline{BSY}$ OUT HIGH TO $\overline{BSY}$ IN LOW VALID	400		ns
t_{blsh}	$\overline{BSY}$ IN LOW TO $\overline{SEL}$ OUT HIGH	100		ns



NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

9.2.5 RESPONSE TO RESELECTION (AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{ivbh}	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
t_{ilbh}	$\overline{I/O}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{bhao}	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO Igroup OUT	100		ns
t_{avbl}	Igroup VALID OUT TO $\overline{BSY}$ OUT LOW	100		ns
t_{bhbl}	$\overline{BSY}$ IN HIGH TO $\overline{BSY}$ OUT LOW	0.4	200	us
t_{bloi}	$\overline{BSY}$ OUT LOW TO "OR-ED" INVALID IN	0		ns
t_{blsh}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
t_{shbh}	$\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT HIGH	0		ns

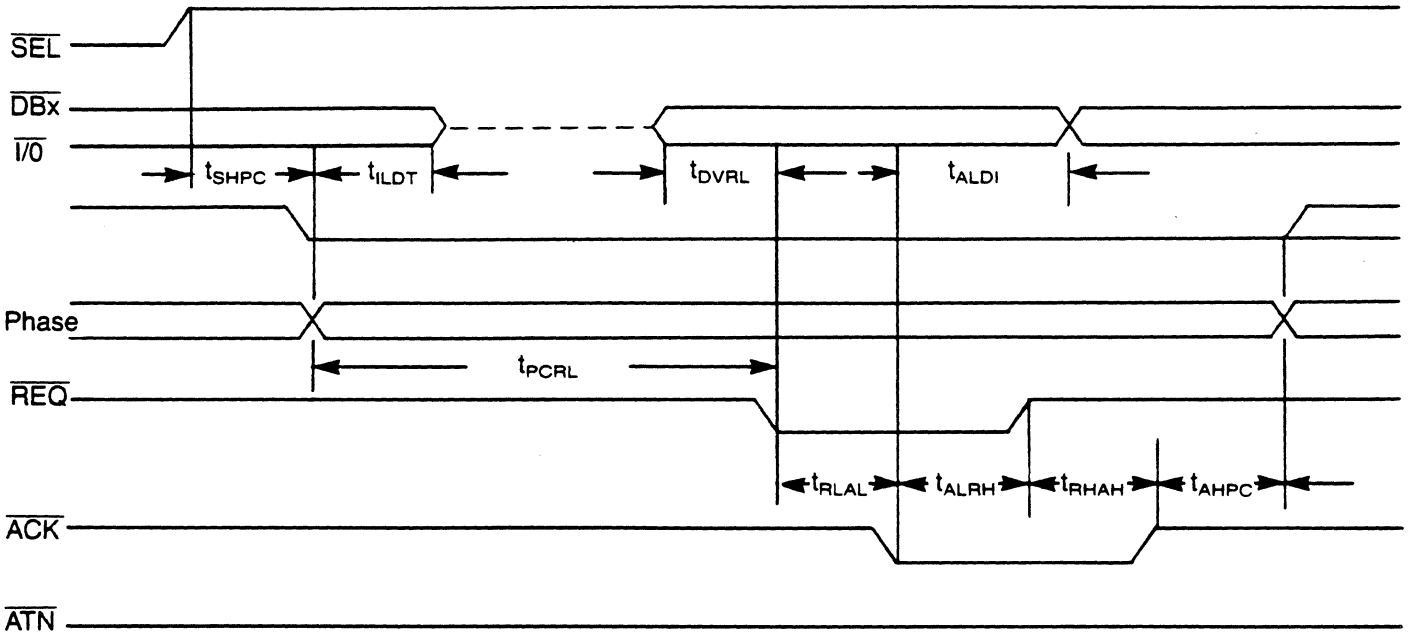


NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

*** $\overline{BSY}$ will still be driven low by the reselecting target.

9.2.6 RECEIVE ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

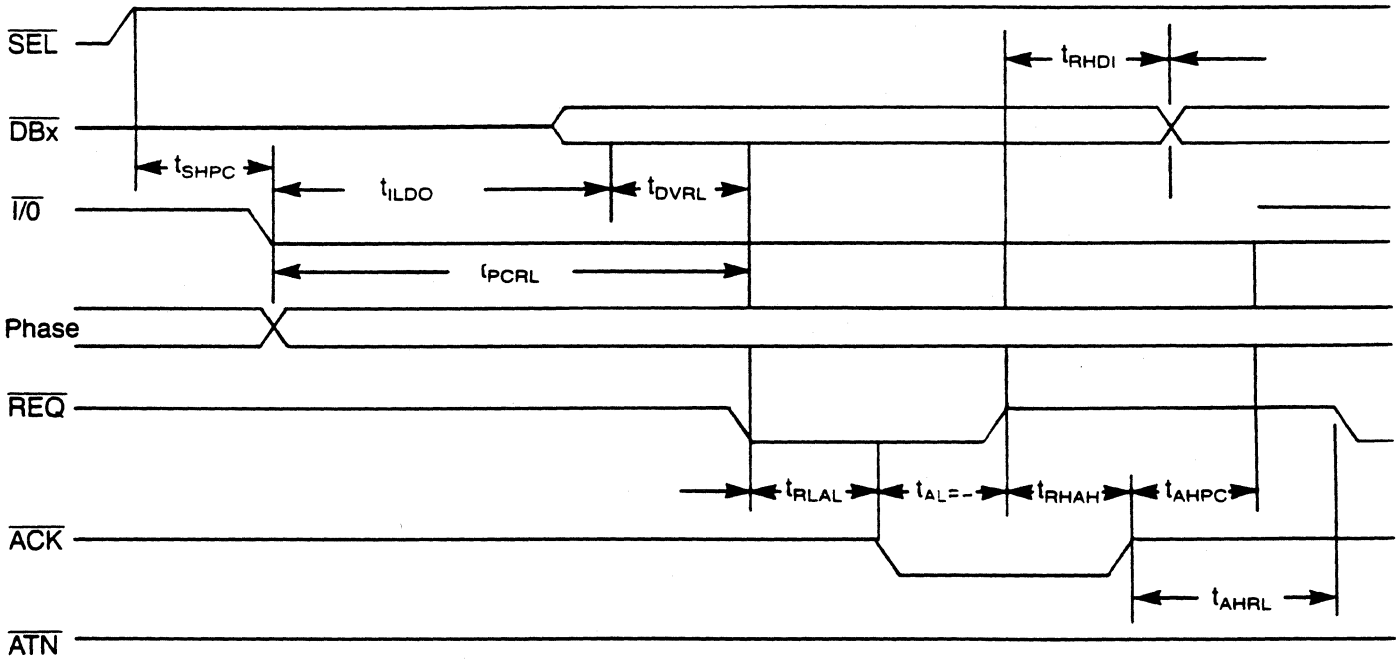
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
t_{ildt}	$\overline{I/O}$ IN LOW TO DATA BUS TRISTATE	0	125	ns
t_{pcrl}	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
t_{dvrl}	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
t_{rlal}	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
t_{aldi}	$\overline{ACK}$ OUT LOW TO DATA INVALID IN	0		ns
t_{alrh}	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
t_{rhah}	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.7 SEND ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

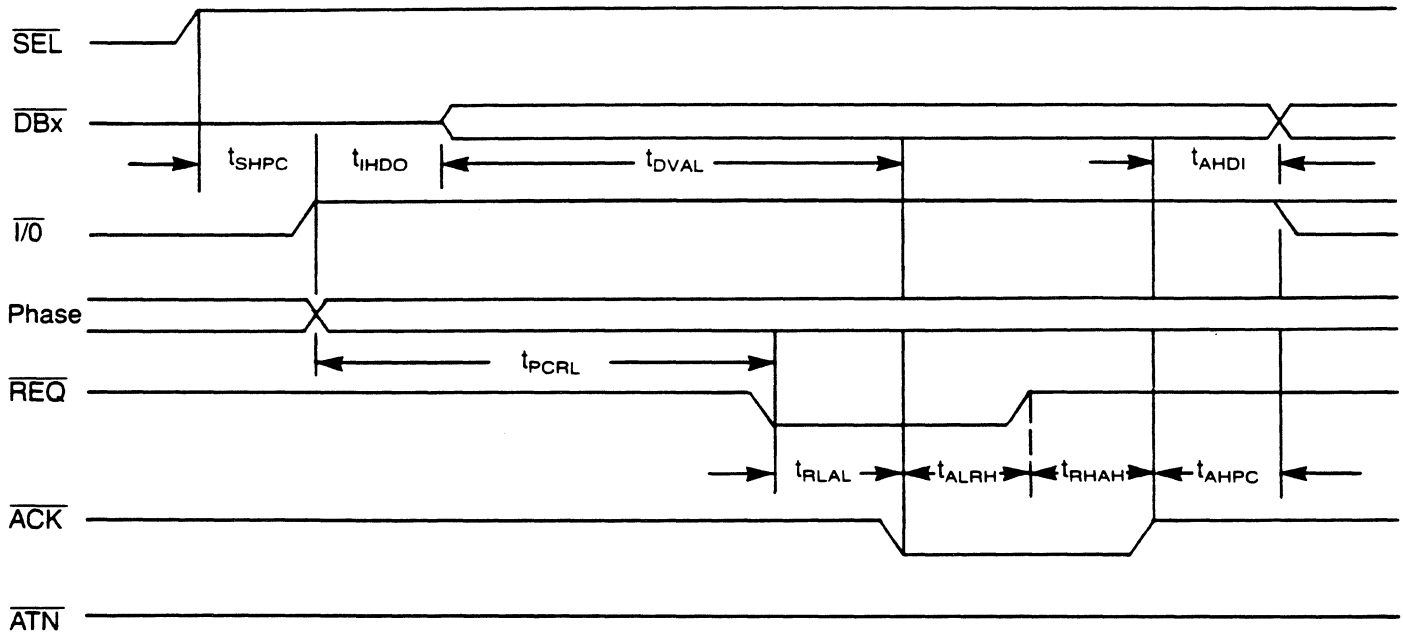
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ildo}	$\overline{I/O}$ OUT LOW TO DATA OUT	800		ns
t_{dvrl}	DATA OUT VALID TO $\overline{REQ}$ OUT LOW	55		ns
t_{pcrl}	PHASE CHANGE OUT TO $\overline{REQ}$ OUT LOW	500		ns
t_{rlal}	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
t_{alrh}	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
t_{rhdi}	$\overline{REQ}$ OUT HIGH TO DATA OUT INVALID	0		ns
t_{rhah}	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ahrl}	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.8 SEND ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

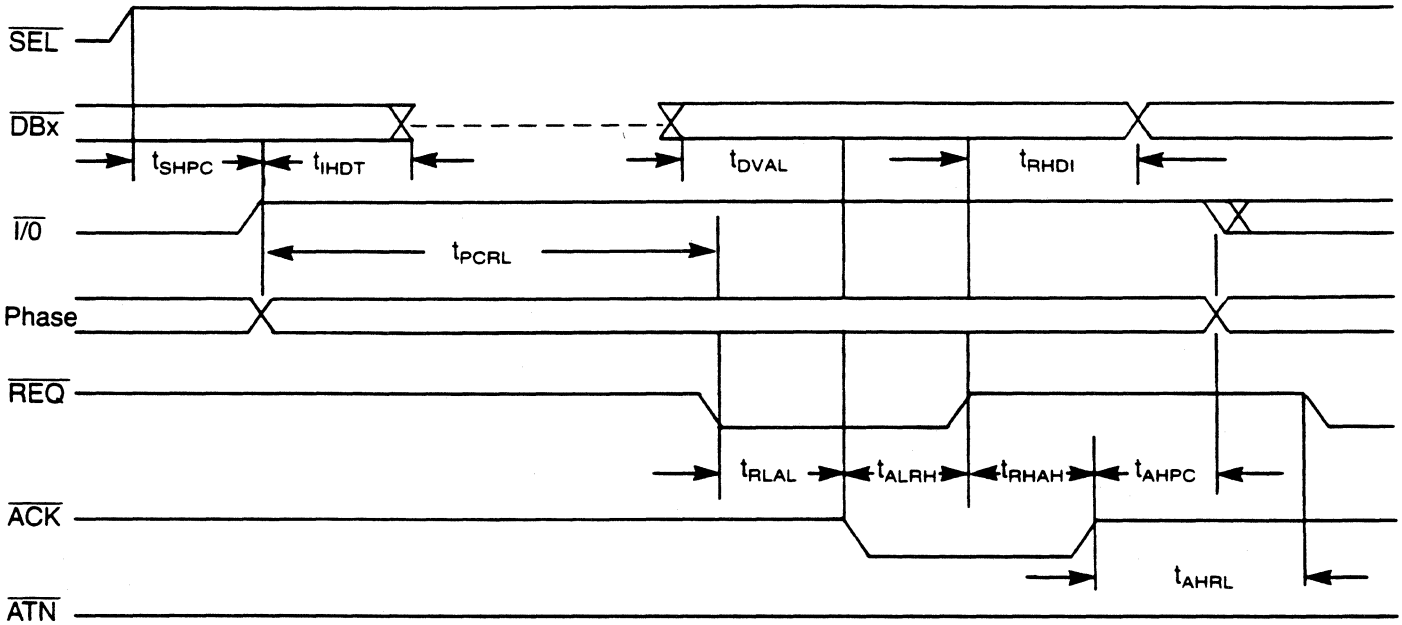
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
t_{ihdo}	$\overline{I/O}$ IN HIGH TO DATA OUT	0		ns
t_{pcrl}	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
t_{rlal}	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
t_{dval}	DATA OUT VALID TO $\overline{ACK}$ OUT LOW	55		ns
t_{alrh}	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
t_{rhah}	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
t_{ahdi}	$\overline{ACK}$ OUT HIGH TO DATA OUT INVALID	0		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.9 RECEIVE ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ihdt}	$\overline{I/O}$ OUT HIGH TO DATA BUS TRISTATE		0	ns
t_{pcrl}	PHASE CHANGE TO $\overline{REQ}$ OUT LOW	500		ns
t_{rlal}	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
t_{dval}	DATA IN VALID TO $\overline{ACK}$ IN LOW	5		ns
t_{alrh}	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
t_{rhdi}	$\overline{REQ}$ OUT HIGH TO DATA IN INVALID	0		ns
t_{rhah}	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns
t_{ahrl}	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns

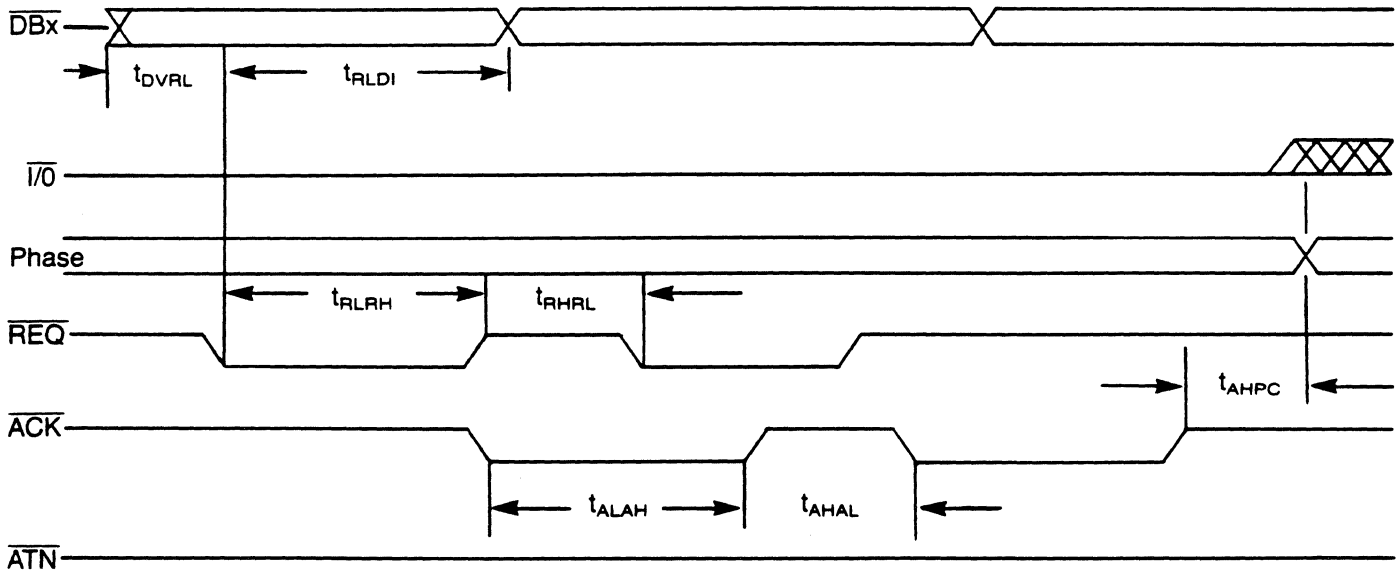


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.10 RECEIVE SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dvrl}	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
t_{rldi}	$\overline{REQ}$ IN LOW TO DATA INVALID	45		ns
t_{rlrh}	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	50		ns
t_{rhrl}	$\overline{REQ}$ IN HIGH TO REQ IN LOW	50		ns
t_{alah}	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH	Tcyc-10		ns
t_{ahal}	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW	Tcyc-25		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 9.2.6.

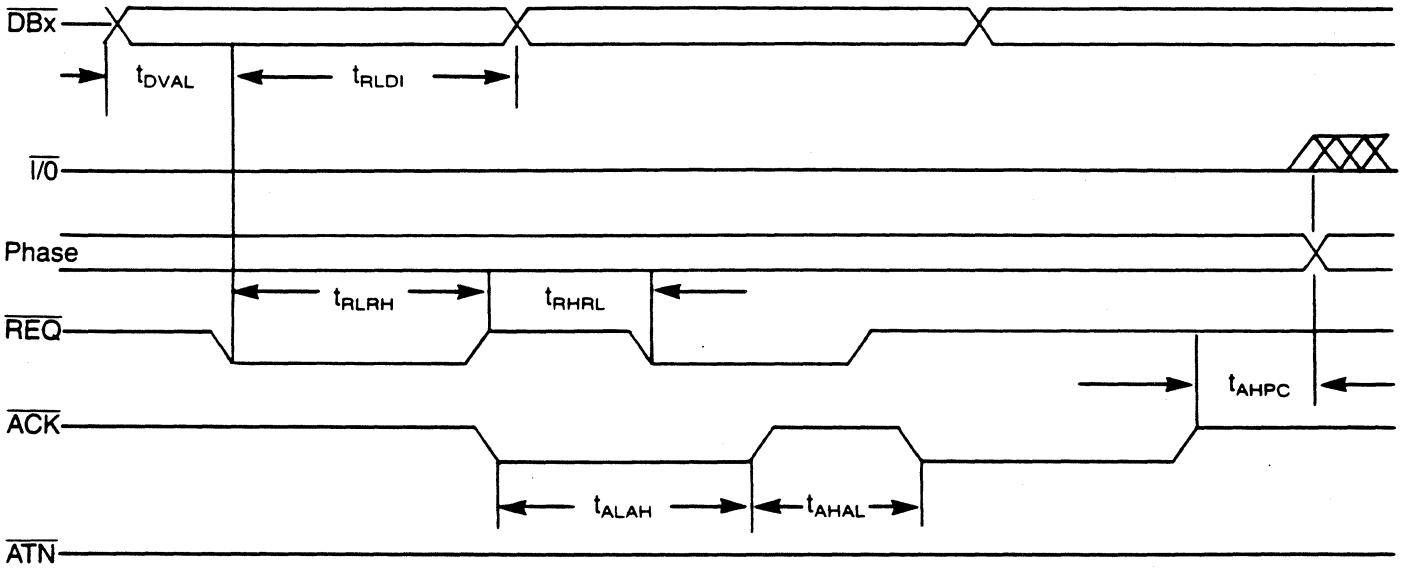


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.11 SEND SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dvrl}	DATA VALID OUT TO $\overline{REQ}$ OUT LOW	55		ns
t_{rldi}	$\overline{REQ}$ OUT LOW TO DATA INVALID OUT	100		ns
t_{rlrh}	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH	Tcyc-10		ns
t_{rhrl}	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW	Tcyc-25		ns
t_{alah}	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	50		ns
t_{ahal}	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	50		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN SUBSECTION 9.2.7.

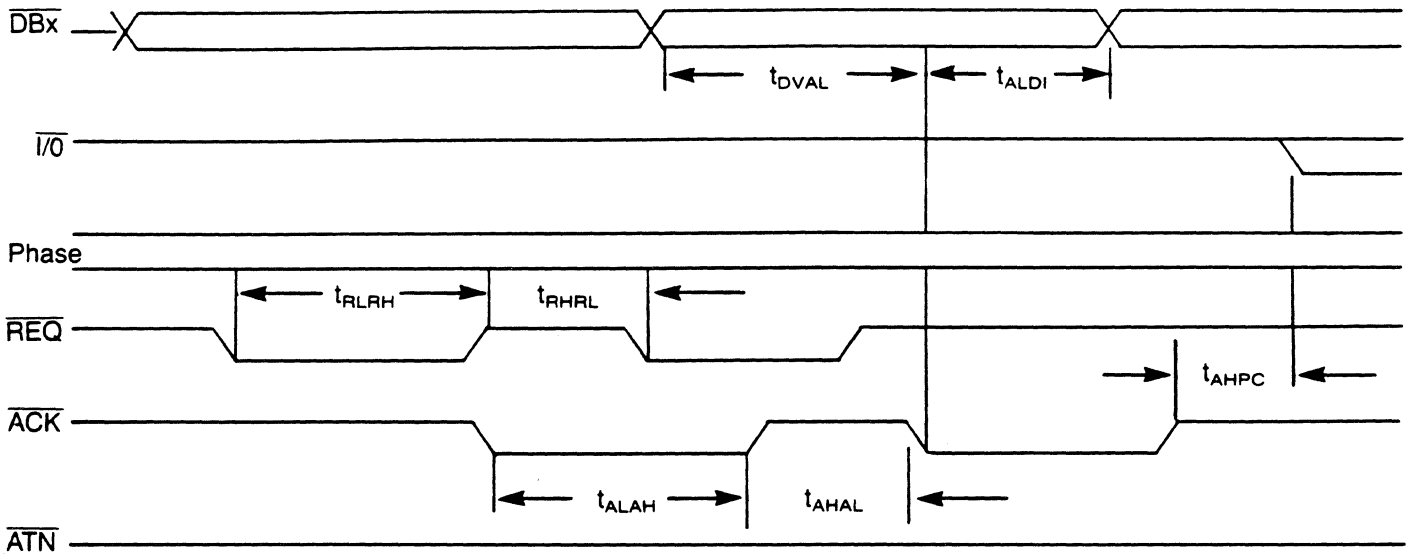


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.12 SEND SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dval}	DATA VALID OUT TO $\overline{ACK}$ OUT LOW	55		ns
t_{aldi}	$\overline{ACK}$ OUT LOW TO DATA INVALID OUT	100		ns
t_{rlrh}	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	50		ns
t_{rhrl}	$\overline{REQ}$ IN HIGH TO $\overline{REQ}$ IN LOW	50		ns
t_{alah}	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH	Tcyc-10		ns
t_{ahal}	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW	Tcyc-25		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 9.2.8.



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

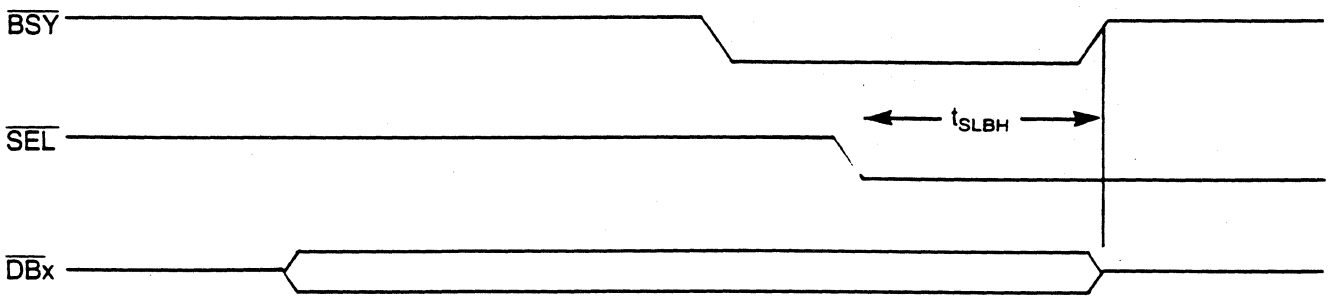
9.2.13 RECEIVE SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dval}	DATA VALID IN TO $\overline{ACK}$ IN LOW	0		ns
t_{aldi}	$\overline{ACK}$ IN LOW TO DATA INVALID	45		ns
t_{rlrh}	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH	Tcyc-10		ns
t_{rhrl}	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW	Tcyc-25		ns
t_{alah}	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	50		ns
t_{ahal}	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	50		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS t_{shpc}, t_{ildt}, and t_{pcrl} ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN SUBSECTION 9.2.9.

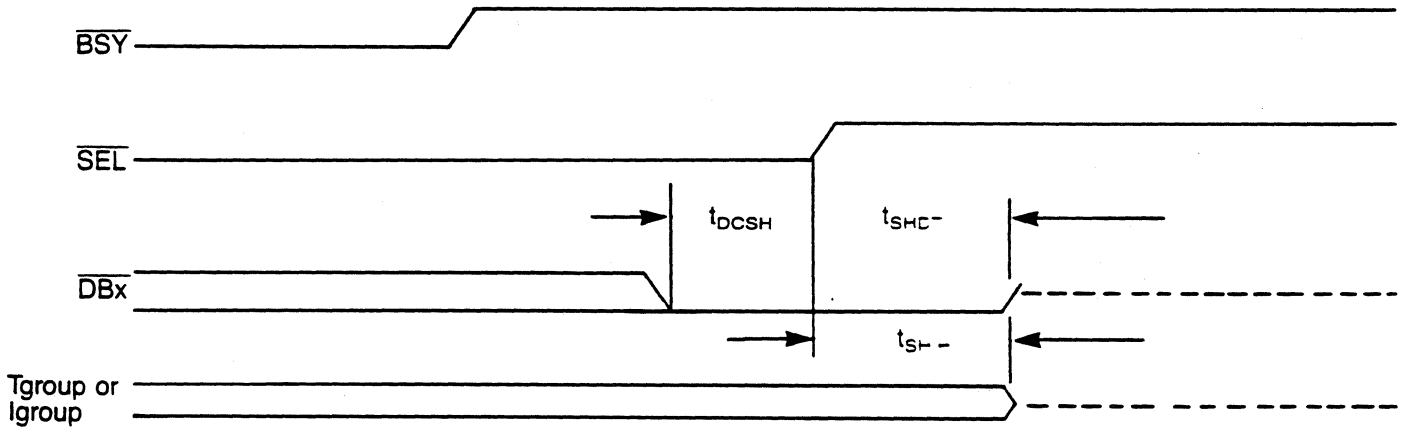
9.2.14 ARBITRATION TO BUS FREE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ HIGH, DATA TRI-STATE		8*Tcyc +75	ns



9.2.15 SELECTION (AS AN INITIATOR) OR RESELECTION (AS A TARGET) TO BUS FREE (SELECTION TIMEOUT)

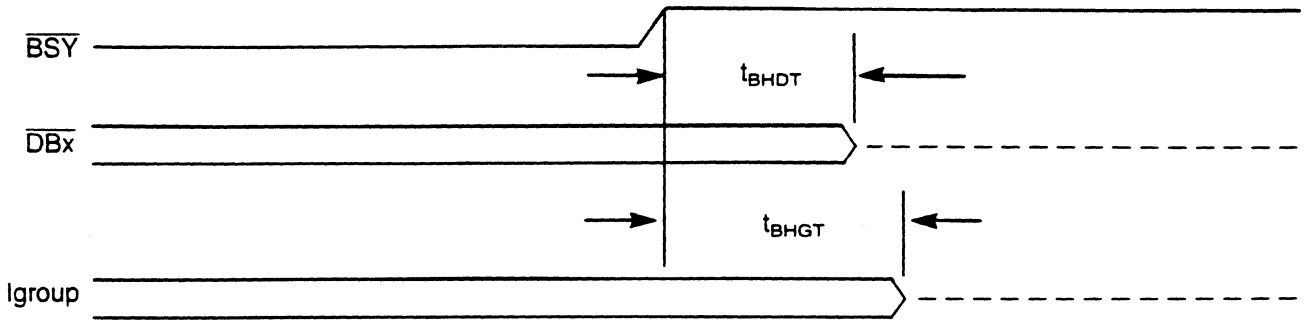
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{tadc}	TIMEOUT OR ABORT TO DATA BUS CLEARED	0		ns
t_{dcsh}	DATA BUS CLEARED TO $\overline{SEL}$ OUT HIGH	200		us
t_{shdt}	$\overline{SEL}$ OUT HIGH TO DATA BUS TRISTATE		800	ns
t_{shih}	$\overline{SEL}$ OUT HIGH TO cntl TRISTATE		800	ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

9.2.16 CONNECTED-AS-AN-INITIATOR TO BUS FREE

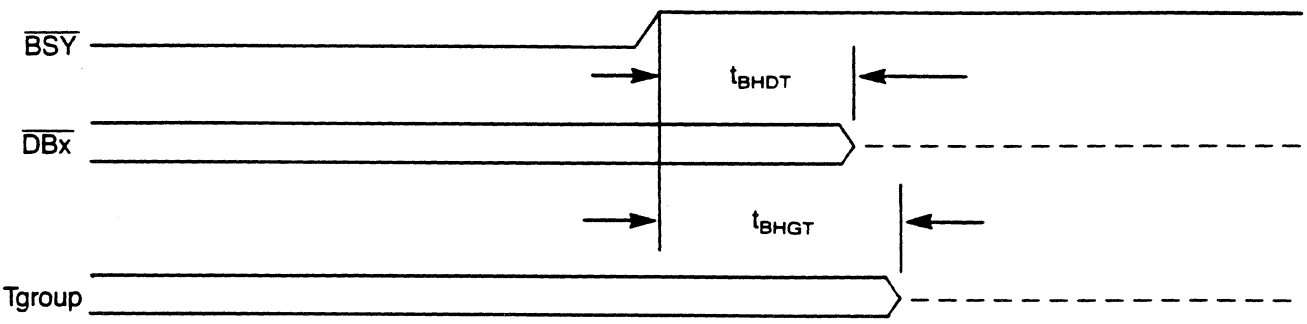
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhdt}	$\overline{BSY}$ IN HIGH TO DATA BUS TRISTATE		8*Tcyc +75ns	ns
t_{bhgt}	$\overline{BSY}$ IN HIGH TO Igroup TRISTATE		8*Tcyc +75ns	ns



NOTE: Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

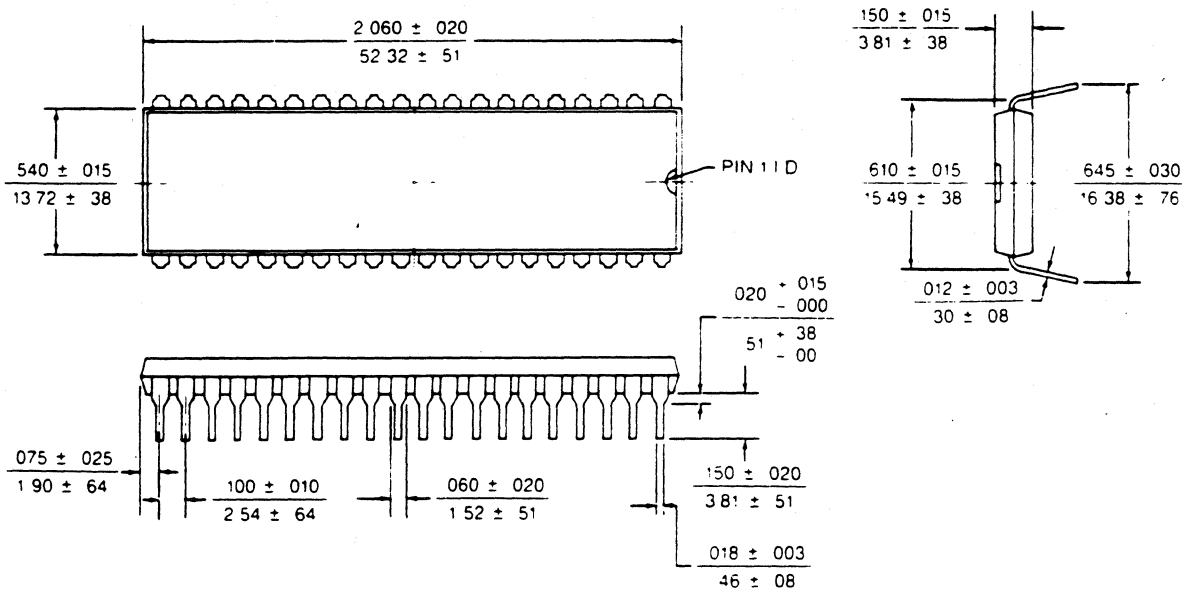
9.2.17 CONNECTED-AS-A-TARGET TO BUS FREE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhdt}	$\overline{BSY}$ OUT HIGH TO DATA BUS TRISTATE	8*Tcyc +75ns	ns	
t_{bhgt}	$\overline{BSY}$ OUT HIGH TO Tgroup TRISTATE		8*Tcyc +75ns	ns

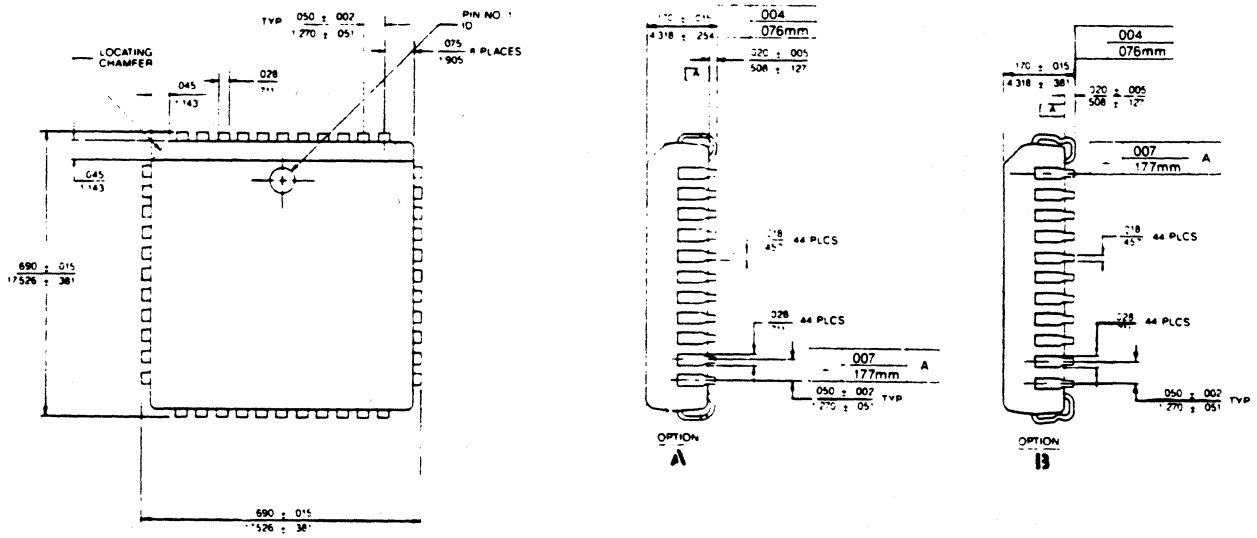


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

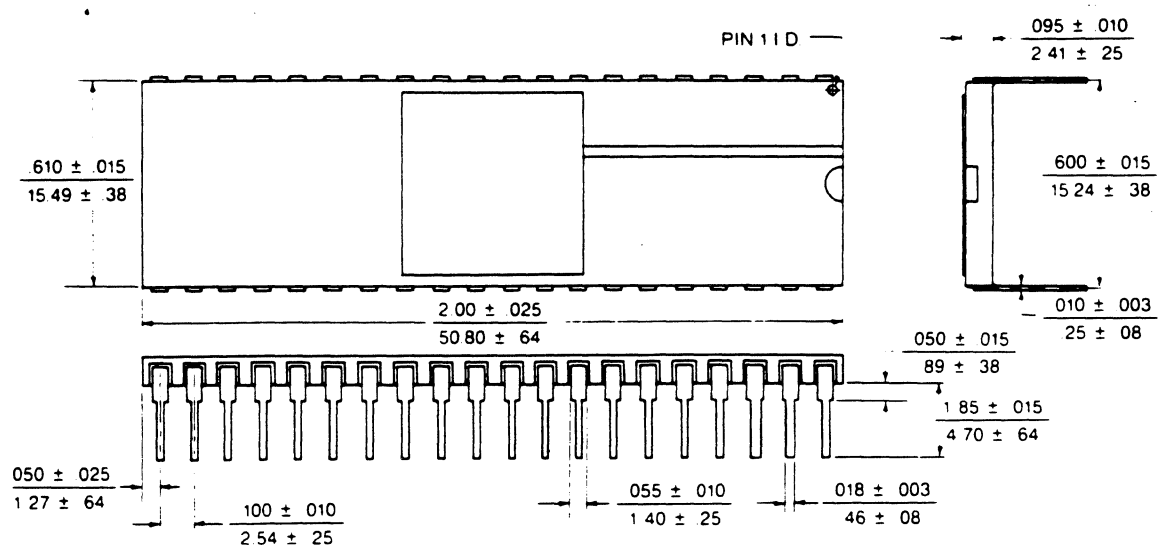
PACKAGE DIAGRAMS



40 LEAD PLASTIC "PL"
WD33C93A



44 LEAD PLASTIC "JM"
WD33C93A



40 LEAD CERAMIC "AL"
WD33C93A

DOCUMENT # 79-000199

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PRODUCT: Model #: **WD33C93A**
Manf #: 5393

August 17, 1990
Number **E025-A**

Converting from the WD33C93 to the WD33C93A

The WD33C93 SCSI Bus Interface Controller (SBIC) chip has been superseded by the WD33C93A. In general there should be no problems in converting from the non-A to the A part. The areas of differences between the two chips are listed in the following pages under 3 sections:

WD33C93A Number Reference:

Model #	Manf #	Description
WD33C93A PL 00 08	5393KF09PL	40 pin Plastic DIP
WD33C93A JM 00 08	5393KF09JM	44 pin PLCC

WD33C93 Number Reference:

Model #	Manf #	Description
WD33C93 PL 00 bb	3393AB09PL	40 pin Plastic DIP
WD33C93 JM 00 bb	3393AB09JM	44 pin PLCC

Changes that could cause conversion issues:

These are design changes in the WD33C93A that are not compatible with normal hardware/firmware design practices for the WD33C93.

1. **Cmd Deletion: Transfer Pad Command:** The Transfer Pad command is no longer supported in the WD33C93A.

2. **Cmd Deletion: Abort Command:** The Abort command is no longer supported in the Initiator mode.

3. **Function Change- Single byte Transfers:** The WD33C93 did not corrupt the Transfer Count register during a Single-Byte-Transfer. This allowed a previous multi-byte operation to be resumed without reloading the Transfer Count register after a Single-Byte-Transfer command. This was an "undocumented feature" that no longer exists in the WD33C93A. The Transfer Register is corrupted during a Single-Byte-Transfer and must be reloaded after execution of that command.

4. **Function Change- Phase Interrupts:** The WD33C93 generates a Phase Change interrupt following an Invalid Command interrupt. This is an unnecessary interrupt and basically an unplanned "feature" of the WD33C93. The WD33C93A does not provide a Phase Change interrupt following a Invalid Command interrupt.

Changes that shouldn't make a difference under normal use

These are design changes in the WD33C93A that will not cause problems with normal hardware/firmware design practices in the WD33C93 but should be checked.

Register Difference Summary:

Under normal design practices, these bits should not be written to nor should their state upon being read make any difference. It is sometimes found that previously non-functional bits are written to or decoded upon read as a matter of programming efficiency and therefore cause problems when a new version of a part is substituted for the original. Below is a list of all register changes (bits not previously active) that should be checked i firmware for proper handling. For more information on the function of these bits, please refer to WD Storage LSI Application Note #E062 on Version Differences in the WD33C93 chip family.

Register	Bit	WD33C93	WD33C93A
a) Own ID register:	3	----	EAF- Enable Advanced Features
	4	----	HHP- Halt on Host Parity error
	5	----	EIH- Enable Immediate Halt
	6,7	----	Xfr rate control
b) Control register:	5	----	DBA- DMA Burst Enable
c) Destination ID register:	5	----	DF- Data Phase Dir Chk Enable
	6	----	DPD- Data Phase Dir check
	7	----	SCC- Select Command Chain
d) CDB Byte 12 register:	1	----	LCC- Linked Command Control
e) Synch Xfr register	3	----	extra bit for 12 byte FIFO

2. **H/W Change: Faster Execution Times-** The command decode and algorithms of many commands have been modified to greatly reduce controller overhead in both Target and Initiator modes.

   Increases in host response timing in general should not cause a problem under normal design practices, but under some circumstances should be checked.

3. **Feature Addition: New Status Codes-** The following status codes have been added:

   a) WD33C93A Advanced Features Enabled- code 0000 0001: This code is returned after a "Soft Reset" if the Enable Advanced Features (EAF) bit is set (bit 4, Own ID). The code provides a means of verifying the presence of the A part.

   b) Unexpected Reselection- code 0010 0111: This code is returned when an unexpected

reselection occurs during a Select-and-Transfer command, and indicates that the Target LUN register contains a valid identify message.

c) Reselection- code 1000 0001: This code is returned when a reselection occurs when the device is idling with Advanced features Mode enabled. The code indicates that the Data register contains a valid identify message.

d) Device Pause- code 1000 0111: This code is returned when the device has paused to get the command length in the Own ID register.

New Status Codes may cause erroneous errors in the Status Code decode section of some types of firmware algorithms and should be checked.

Changes in the WD33C93A that will cause no conversion issues:

1. **H/W Addition: Faster Transfer Rate-**
   a) The WD33C93A can now transfer data at up to 5MB/s.

   b) A burst DMA mode on the µp side has been added to help accommodate higher data bandwidths. Bit 5 of the Control register has been added to enable the DMA burst mode.

   c) The maximum clock frequency has been increased to 20Mhz

   d) Selectable dividers controlled by bits 7,6 in the Own ID register have been added to manage transfer rate and arbitration timing.

2. **H/W Addition: Extended FIFO-** The WD33C93A internal data FIFO has been expanded to 12 bytes from 5 bytes for the WD33C93. Bit 3 has been added to the offset counter in the Synchronous Transfer register to accommodate the increased FIFO size.

3. **Cmd Addition: Send-Status-and-Command-Complete (0Dh) -** This target mode command has been added to the WD33C93A. This command first sends the status byte, as specified in the CDB byte 11. This command will send a linked command complete message. Linked command complete with flag is sent when bit 1 of CDB 12 is set. The command will also chain to the command fetch portion of WAIT-for-Select-and-receive.

4. **Cmd Addition: Send-Disconnect-Message (0E) -** This target mode command is used to disconnect from the SCSI bus when the target expects to seek, find the first block, deal with long tape operations, fill a buffer, etc.. The command sends the disconnect message, followed by a disconnect from the bus. If the IDI bit is set to one, a Save-Data-Pointer message is sent prior to the disconnect message.

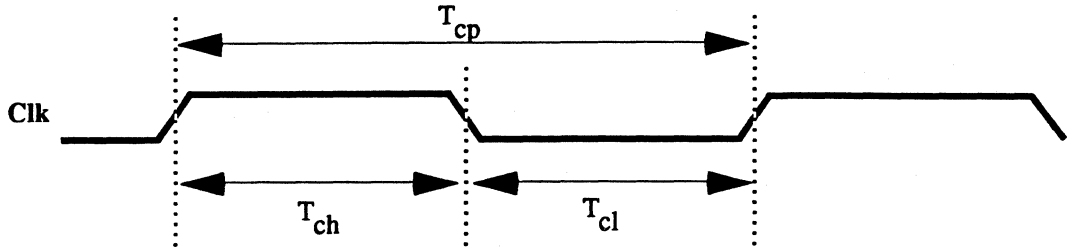
5. **Cmd Addition: Set IDI bit (0F) -** This command is used to set the IDI bit when a level II command is in progress. This is needed since the register file is not accessible to the µp at that time.

6. **Feature Addition: Reselect-and-Transfer Cmd Enhancement:** These commands may now be resumed in the same manner as the initiator Select-and-Transfer commands. Also, these commands may be chained to the new Send-Status-and Command-Complete and Send-Disconnect-Message commands using the EDI bit in the control register, and the command link select bit in the destination ID register.

7. **Feature Addition: Wait-for-Select-and-Receive Cmd Enhancement:** This command may now be resumed in the same manner as the initiator Select-and-Transfer commands. Also, this command may be chained to from the new Send-Status-and-Command-Complete command. When EDI is set, this command will chain to the Send-Disconnect-Message command if CDB byte 1 indicates a read command has been received.

8. **Feature Addition: 20MHz clock rate:** The input clock timings for the WD33C93A have been changed from those listed in the WD33C93A data sheet, which specified a maximum frequency of 16Mhz. The WD33C93A is now guaranteed to operate with a maximum input clock frequency of 20MHz, and the revised timings are listed below:

Symbol	Characteristic	Min	Max	Units
T_{cp}	Clock Period	50	125	ns
T_{ch}	Clock High	20	---	ns
T_{cl}	Clock Low	20	---	ns



14.

9. **Msc Changes/Additions:**

a) CDB byte 11 register: This register is now also used to specify the status byte for Send-Status-and-Command-Complete commands

b) CDB Byte 12 register: When the Flag bit (Bit 1) is 0 and IDI is 1, Linked Command Complete (message code = 0Ah) is sent during a Send-Status-and-Command-Complete command. When this bit is 1 and IDI is 1, Linked Command Complete with Flag (message code = 0Bh) is sent during a Send-Status-and-Command-Complete command.

c) Target LUN register: This register can also contain the identify message received during an unexpected reselection if advanced features are enabled.

d) Select Command Chain Control: Bit 7 (SCC) in the Destination ID register has been added to control which command is chained to when the data transfer is completed:

0 Chain to Send-Status-and-Command-Complete
1 Chain to Send-Disconnect-Message

WD33C93A Incompatibilities when being used with a WD33C93 also on the SCSI bus:
Performance optimization of both the internal microcode and the LSI design have resulted in the following incompatibilities between the WD33C93A and the WD33C93:

a) WD33C93 offset values: Due to timing differences between the two parts, the WD33C93 offset must not be set to its maximum value of five during synchronous transfers from the WD33C93A to the WD33C93. Any other offset value (0 through 4) may be used.

b) The WD33C93A checks for ATN\ assertion before the start of a data transfer. A Receive or Send command will halt if HA is set prior to the transfer of any data. The WD33C93 allows a data transfer to occur before looking for ATN\.

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PRODUCT: Model #: **WD33C93A**
Manf #: 5393

August 17, 1990
Number **E018-A**

WD33C93A Bug List

Known Problems:

Additions and Changes:

DETAILED PROBLEM DESCRIPTIONS and WORK-AROUNDS

P1) Unexpected Data In Phase:

Affects: Initiator mode, Data In phase, Identify Message

Instructions: Select-and-Transfer

Description: An unexpected Data In Phase follows the Identify message out of Select-and-Transfer. This may cause spurious new phase interrupts.

Work-Around: Resume the Select-and-Transfer command with the Command phase register set to 41h

P2) Assert-ATN bug :

Affects: Initiator mode, Identify Message Out, Command phase

Instructions: Select-and-Transfer

Description: Issuing the Assert-ATN\ command during the Identify Message Out or Command phases of the Select-and-Transfer command will cause the WD33C93A to behave unpredictably

Work-Around: Do not issue the Assert-ATN\ command until the Command phase has completed when using Select-and-Transfer or us the separate Select and Transfer Info commands to implement the Select-and-Transfer sequence up to the end of the Command phase.

P3) FIFO data loss:

Affects: Initiator mode, Data Out phase, Disconnect message

Instructions: Select-and-Transfer

Description: The WD33C93A will lose any bytes stored in the FIFO during the Data Out phase of the Select-and-Transfer command when the Target changes phase to send a Disconnect message. If the IDI bit is not set, the host will never know that the FIFO bytes were lost.

Work-Around: Set the IDI bit before issuing the Select-and-Transfer command when Target disconnects are enabled and a Data Out phase is expected.

P4) REQ\ assertion timing error:

Affects: Target mode, timing from phase line change to REQ\ assertion

Instructions: Wait-for-Select-and-Receive

Description: Under some circumstances, the WD33C93A will violate the minimum time required

by the SCSI specification between changing the phase lines and asserting REQ/ These violations occur during the Wait-for-Select-and-Receive command when the WD33C93A sets the phase lines for a message out phase and asserts REQ\ to obtain the Identify message byte and the first byte of a Tag message.

Work-Around: Set the Enable Selection (ES) bit in the Source ID register to allow selection by another SCSI device. Use the Receive-Message command to request any message bytes and then resume the Wait-for-Select-and-Receive command starting with the command phase.

P5) False Bus Free detection:

Affects: Bus free detection

Instructions: - - - -

Description: The WD33C93A may detect a false Bus Free condition. Bus Free is defined in the SCSI specification as both BSY\ and SEL\ being false for ≥ 400ns. The WD33C93A may signal a Bus Free condition for BSY\ and SEL\ being negated for ≥200ns.

Work-Around: No specific work-around is available. Try to ensure as clean a SCSI bus as possible to minimize reflections. Normal conditions should not produce glitches in the 200ns to 400ns range.

P6) T_{whdi} Timing Violation:

Affects: Host bus interface, WD Bus interface mode

Instructions: - - - -

Description: The WD33C93A does not meet the timing requirements for Twhdi (WE\ high to data invalid) in the WD bus interface mode. The data hold time after WE\ goes false is specified as ≥ 30ns. The actual hold time will perform as ≥ 10ns

Work-Around: The specification will be changed to Twhdi ≥10ns.

P7) T_{slrv}, T_{slrv} Timing Violation:

Affects: Host bus interface, WD Bus interface mode

Instructions: - - - -

Description: The WD33C93A does not meet the timing requirements for Tslrv (RCS\ low to RE\ valid) or Tslwv (RCS\ low to WE\ valid) in the WD bus interface mode. The set up time for RCS\ out going true until RE\ or WE\ goes true is specified as ≥0 ns. The internal timing for these outputs is such that the actual performance is ≥ -5ns for RCS\ true to WE\ or RE\ true.

Work-Around: The specification will be changed to Tslrv, Tslwv ≥ -5ns.

Additions and Changes

1) 20MHz clock rate:

Affects: maximumClock input frequency

Instructions: - - - -

Description: The input clock timings for the WD33C93A have been tightened from those listed in the WD33C93A data sheet, which specified a maximum frequency of 16Mhz. The WD33C93A is now guaranteed to operate with a maximum input clock frequency of 20MHz, and the revised timings are listed below:

Symbol	Characteristic	Min	Max	Units
T_{cp}	Clock Period	50	125	ns
T_{ch}	Clock High	20	---	ns
T_{cl}	Clock Low	20	---	ns