WD83C584

Bus Interface

Controller Device

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DESCRIPTION

The WD83C584 is a single device bus interface controller that enables a LAN controller device to function with the standard PC XT, AT or compatible bus with minimum external logic. This device interfaces with BIOS ROM, shared memory, external EEPROM and the LAN controller. It's internal registers are automatically loaded with configuration data from the external EEPROM.

1.2 FEATURES

- Host: IBM PC/XT/AT, PS/2s, and compatibles
- Interfaces to:
  - WD83C690, 8390
  - BIOS ROM: 16, 32 or 64 Kbyte windows in memory space
  - Shared Memory
- 16-bit or 8-bit Memory Data
  - 8-bit I/O Data
- Bus Speed: Supports 8.33 MHz EISA
- SRAM Memory:
  - 8-bit: 8 or 32 Kbyte
  - 16-bit: 16 or 64 Kbyte
- Shared Memory Mapped
  - allowing 16-bit 1 wait state or 8-bit 4 wait state transfers
  - Zero Wait State on AT busses allowing 16-bit 0 wait state or 8-bit 2 wait state memory transfers
- Interfaces to external EEROM which stores:
  - I/O Address
  - Memory Address
  - Memory Size
  - BIOS ROM Address
  - Configuration
  - LAN Address
- Controls 128 Byte External EEROM

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2.0 PIN OUTS

2.1 PIN DESCRIPTIONS

2.2.1 PC Bus Signals

PIN	NAME	DESCRIPTION
97 96 95 94 93 92 91	LA23 (I) LA22 LA21 LA20 LA19 LA18 LA17	PC LA ADDRESS BUS These input signals (unlatched) are used to address memory. They give the system up to 16 Mbyte of addressability. They are valid when BALE is high. Their purpose is to generate memory address decodes during 0 and 1 wait state memory Read/Write cycles.
19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03	SA19 (I) SA18 SA17 SA16 SA15 SA14 SA13 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0	PC ADDRESS BUS Address lines SA 19-13 & SA 9-0 are used to decode and address memory. SA 15-13 and SA 9-0 are used for I/O addressing.
99	BALE (I)	PC ADDRESS LATCH ENABLE Used to enable address lines LA23-17 from the LA bus.
98	$\overline{\text{SBHE}}$ (I)	PC BUS HIGH ENABLE Indicates a transfer of data on the upper byte of the data bus, SD8 - SD15.
100	$\overline{\text{M16CS}}$ (0)	PC MEMORY 16-BIT CHIP SELECT Signals the system board that the present transfer is a 16-bit memory cycle. It is derived from a decode of LA23 - LA17. It is driven by a tri-state driver.
77	BIT8 (I)	PC 8-BIT BUS / 16-BIT BUS A 0 or low signal on this input indicates that the data bus is an 16-bit bus. A 1 or high signal indicates that the data bus is 8 bits.
47 46 45 44 43 42 41 40	SD7 (I/O) SD6 SD5 SD4 SD3 SD2 SD1 SD0	PC DATA BUS These signals provide the low order data bus bits. They are the PC's access to the internal registers.

TABLE 2-1. PC BUS SIGNALS

PIN	NAME	DESCRIPTION
21	CLK (I)	PC CLOCK PC system clock used to synchronize the zero wait state line when used in the 8-bit interface mode.
33	RSTDRV (I)	PC RESET Used to reset or initialize logic at power up time.
58	$\overline{IOR}$ (I)	PC I/O READ When low, this input transfers the contents of the selected I/O register onto the PC data bus.
59	$\overline{IOW}$ (I)	PC I/O WRITE When low, this input transfers the contents of the PC data bus onto the selected I/O register.
82 22	$\overline{MEMR}$ (I) $\overline{SMEMR}$ (I)	PC MEMORY READ These inputs connect to the memory read signals on the PC bus. When this signal is active, it enables data from the buffer memory onto the PC data bus. $\overline{SMEMW}$ is active only when the memory address is within the first 1 Mbyte of memory space.
81 23	$\overline{MEMW}$ (I) $\overline{SMEMW}$ (I)	PC MEMORY WRITE This input connects to the memory write signal on the PC bus. When this signal is active, it enables data on the PC bus to be stored on the buffer memory. $\overline{SMEMW}$ is active only when the memory address is within the first 1 Mbyte of memory space.
20	AEN (I)	PC ADDRESS ENABLE This input connects to the address enable signal on the PC bus. If Address Enable is active, the WD83C584 will not respond to any command.
24	IORDY (O)	PC READY I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lenthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. This signal is driven by a tri-state buffer capable of sinking 24 mA.
32	$\overline{0WS}$ (O)	PC ZERO WAIT STATE Zero wait state signal tells the host processor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, $\overline{0WS}$ is derived from an address decode gated with a $\overline{MEMR}$ or $\overline{MEMW}$ command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, $\overline{0WS}$ should be driven active one system clock after the $\overline{SMEMR}$ or $\overline{SMEMW}$ command is gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. $\overline{0WS}$ is a tri-state output capable of sinking 24 mA.
90 86 87 88 89 85 84 83	IRQ2/9 (O) IRQ3 (O) IRQ4 (O) IRQ5 (O) IRQ7 (O) IRQ10 (O) IRQ11 (O) IRQ15 (O)	PC INTERRUPT REQUESTS An interrupt request is generated when INT is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request. Only one line is active at a time; all others are tri-stated.

TABLE 2-1. PC BUS SIGNALS (Continued)

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2.2.2 LAN Signals

PIN	NAME	DESCRIPTION
37 38 39	$\overline{B0OE}$ (O) $\overline{B1OE}$ (O) $\overline{SWAP}$ (O)	PC BUFFER OUTPUT ENABLE Controls the least significant, most significant and swap byte buffers respectively.
36	BUFDIR (O)	PC BUFFER DIRECTION Provides direction control for an external data buffer. BUFDIR is "1" for writes and "0" for reads.
78	BSCK (I)	LAN CLOCK 20 MHz clock.
55	BREQ (I)	LAN BUS REQUEST Bus Request is used to request the local bus for DMA transfers. this signal is generated when the LAN controller FIFO needs servicing.
56	BACK (O)	LAN BUS ACKNOWLEDGE Bus Acknowledge indicates that the LAN controller has been granted the bus.
60	$\overline{CS}$ (O)	LAN CHIP SELECT Places the LAN in slave mode for access to LAN internal registers.
57	$\overline{ACK}$ (I)	LAN SLAVE I/O ACKNOWLEDGE Active low when LAN controller grants access to WD83C584. Used to insert wait states to WD83C584 until the LAN controller is synchronized for a register read or write operation.
54	INT (I)	LAN INTERRUPT Indicates that the LAN controller requires CPU attention after reception transmission or completion of DMA transfers.
53	$\overline{RESET}$ (O)	LAN RESET Hardware reset to the LAN controller IC.

TABLE 2-2. LAN SIGNALS

2.2.3 EEROM Signals

PIN	NAME	DESCRIPTION
50 49 48	$\overline{\text{INIT2}}$ (I) $\overline{\text{INIT1}}$ (I) $\overline{\text{INIT0}}$ (I)	EEROM INITIALIZE There are three EEPROM initialization pins. Depending on the state of these pins, the WD83C584 registers will power up from different EEROM bytes. The following table shows the bytes from which it will power up. Refer to each register to determine the value of each byte loaded at power up. One case is special, it causes the WD83C584 to its INITIAL state which overrides EEROM. (Refer to each register for their INITIAL values.) Note that the LAN ADDRESS is read from locations 40-47.

$\overline{\text{INIT2}}$	$\overline{\text{INIT1}}$	$\overline{\text{INIT0}}$	EE ADDRESS
1	1	1	00-07
1	1	0	08-0F
1	0	1	10-17
1	0	0	18-1F
0	1	1	20-27
0	1	0	28-2F
0	0	1	30-37, INITIAL CONDITION
0	0	0	38-3F

35	$\overline{\text{TEST}}$	TEST Used for factory testing. Must be pulled up to +5V with 10 Kohm, 5% resistor.
64	EECS (O)	EEROM CHIP SELECT
63	EESK (O)	EEROM CLOCK
62	EEDI (O)	EEROM DATA INPUT
61	EEDO (I)	EEROM DATA OUTPUT An external 9346 serial EEROM is used to store up to 1024 bits of EEROM data. The above signals interface to this chip. The EEROM is used to initialize registers at power up time. It takes about 2 ms to read all 16 registers after the end of the reset pulse. It takes about 200 ms to store EEROM.

TABLE 2-3. EEROM SIGNALS

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2.2.4 RAM Signals

PIN	NAME	DESCRIPTION
71	$\overline{\text{RAMOE}}$ (O)	RAM OUTPUT ENABLE This output connects to the output enable pins on the buffer RAM.
70	$\overline{\text{RAMWR}}$ (O)	RAM WRITE ENABLE This output connects to the write enable pins on the buffer RAM.
68 69 67	$\overline{\text{RMCS0}}$ (O) $\overline{\text{RMCS1}}$ (O) RAM12 (O)	RAM0 CHIP SELECT RAM1 CHIP SELECT These outputs provide the chip select signals needed by the buffer RAMs.
66 65	MA13 (I) MA0 (I)	These inputs are connected to memory address bus. They are used for memory address decode.
73	MEM16 (O)	MEMORY 16 ENABLE Indicates the host PC to RAM access will be 16 bits wide. This output will not go active if the WD83C584 is used and programmed for 8-bit applications.
72	LAN16 (O)	LAN 16 ENABLE Indicates the LAN controller to RAM access will be 16 bits wide.

TABLE 2-4. RAM SIGNALS

2.2.5 General I/Os

PIN	NAME	DESCRIPTION
52 26 27	OUT3 (O) OUT2 (O) OUT1(O)	OUTPUTS These three output pins follow bits D1, D2 and D3 in the IRR register.
30 31	INPUT2 (I) INPUT1 (I)	INPUTS These two input pins are readable via software from IRR bits D1 and D2.

TABLE 2-5. GENERAL I/Os

2.2.6 ROM Signals

PIN	NAME	DESCRIPTION
76	$\overline{\text{ROMOE}}$ (O)	BIOS ROM OUTPUT ENABLE Chip Select for BIOS ROM. This signal gates ROM data onto the SD7-0 bus.
75 74	ROM15 (O) ROM14 (O)	ROM ADDRESS LINES These attach to the ROM address bits 15 and 14. Depending on the state of the RAM and FLSH bits, these lines do the proper addressing and write strobes for RAM and FLASH ROM.

TABLE 2-6. ROM SIGNALS

2.2.7 Voltages

PIN	NAME	DESCRIPTION
34	POWER (I)	POWER SENSING INPUT This signal is used to sense that the input power has risen to a useable level. This signal has a Schmidtt trigger input.
02,28, 79	VCC (I)	+5V (3 pins)
01,29 51,80	GND (I)	GROUND (4 pins)

TABLE 2-7. VOLTAGES

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3.0 THEORY OF OPERATION

3.1 INITIALIZATION

Upon power-up, the WD83C584 accesses an external EEROM to set up its initial configuration. This takes about 2 milliseconds to read the data from the EEPROM into the WD83C584. After this time the BIOS ROM and I/O Ports will be enabled. The Shared Memory is always disabled upon power up, and must be enabled by software.

3.2 ARBITRATION

Arbitration for the bus is mainly between the PC and the LAN controller. The LAN controller asserts BREQ and if the bus is free, a BACK is returned. When the LAN controller has the bus, it is in complete control and must provide all RAM and interface signals. Also, access to the ROM and the internal registers on the WD83C584 must also arbitrate for the bus.

3.3 RAM BUFFER

The RAM buffer uses either 8K or 32K SRAMs. It may be either 8 bits or 16 bits wide (giving 64K maximum).

3.4 EXTERNAL EEROM

The WD83C584 accesses an external EEROM. The contents of the EEROM are loaded into the internal registers of the WD83C584 upon power up.

The use of EEROM has several advantages over a separate PROM for the LAN address. It can also reduce the number of jumpers needed on the board. It allows for reconfiguration without removing the board from the system.

Upon power up, the EEROM data is read into the WD83C584 registers. Of course, the first time the EEROM is powered up, it will have random data. The $\overline{\text{INIT}}$ inputs allow the EEROM to be set to a known initial state.

All 128 bytes of EEROM can be accessed and modified from the WD83C584. They are read into the LAN Address registers 8 bytes at a time. Once there, they can be changed and stored back into the EEPROM.

4.0 INTERNAL REGISTERS

In the following descriptions, several values of each register are given as follows:

RESET	The value during RSTDRV time.
INITIAL	If the $\overline{INIT2}$, 1, 0 pins (50,49,48) are connected such that 001 is present on these inputs, this value is loaded into the register immediately after RSTDRV time.
POWER-UP	If not in the INITIAL setting, this value is loaded into the register immediately after RSTDRV time.
RECALL	This value is loaded each time a recall is performed.
REGISTER VALUES:	? = value unknown EE = value loaded from EEROM 1 = logical 1 0 = logical 0 n/a = not used

4.1 I/O MAP

0x00	MEMORY SELECT REGISTER (MSR)
0x01	INTERFACE CONFIGURATION REGISTER (ICR)
0x02	I/O ADDRESS REGISTER (IA)
0x03	BIOS ROM ADDRESS REGISTER (BIO)
0x04	INTERRUPT REQUEST REGISTER (IRR)
0x05	LA ADDRESS REGISTER (LAAR)
0x06	INITIALIZATION JUMPERS
0x07	GENERAL PURPOSE DATA REGISTER (GP2)
0x08-0x0F	LAN ADDRESS REGISTERS (LAR)
0x10-0x1F	LAN CONTROLLER REGISTERS (LAN)

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4.2 MEMORY SELECT REGISTER (MSR)

Offset 0x00

Upon power-up, MENB is 0. Thus the memory is disabled at power up, and will not be enabled until the MSR has been programmed with the MENB bit a "1". It is possible to program the memory select bits and the memory enable bit simultaneously.

	D7 RST	D6 MENB	D5 RA18	D4 RA17	D3 RA16	D2 RA15	D1 RA14	D0 RA13
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	EE	EE	EE	EE	EE	EE
POWER-UP	0	0	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	RST	SOFTWARE RESET Set to 1 and then back to 0 to force a hardware reset to the LAN Controller.
D6	MENB	MEMORY ENABLE Set to 1 to enable PC access to shared memory.
D5	RA18	MEMORY ADDRESS BITS
D4	RA17	Must be set to the address at which the shared memory is to be placed. These
D3	RA16	bits correspond to system memory address bits SA18 through SA13.
D2	RA15	SA19 is assumed to be a "1". For example, address C4000 could be selected
D1	RA14	by writing 0x62 to this register. In 16-bit mode, A19 is set by the LAAR register.
D0	RA13	

4.3 INTERFACE CONFIGURATION REGISTER

(ICR) Offset 0x01, (Read/Write)

The ICR determines the configuration of the WD83C584.

	D7 STO	D6 RIO	D5 RX7	D4 RLA	D3 MSZ	D2 IR2	D1 n/a	D0 BT16
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	0	0	0	0	0
POWER-UP	0	0	0	0	EE	EE	EE	NA
RECALL	EE	EE	EE	EE	EE	EE	EE	NA

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BIT	NAME	DESCRIPTION
D7	STO	NON-VOLATILE EEROM STORE Set to 1 to store registers into EEROM. The bit will be automatically reset. It takes a maximum of 200 ms for a store to take place. It will be reset when the store is complete. This bit may be polled to determine when the store operation is complete. The EEROM has a limited number of stores that can take place. The store operation should only take place at initial board configuration or at initial installation.
D6	RIO	RECALL I/O ADDRESS FROM EEROM Set to 1 to recall the I/O address from EEROM into the I/O Address Register. It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D5	RX7	RECALL ALL BUT I/O and LAN ADDRESS Set to 1 to recall registers with offsets 0x00 and 0x02 through 0x07. It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D4	RLA	RECALL LAN ADDRESS Set to 1 to recall the LAN address only from EEROM (Registers 0x08 through 0x0F). It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D3	MSZ	SRAM SIZE This is the physical size of the SRAM chips on the board. 0 = 8K, 1 = 32K In order to determine the RAM window in host memory, this bit must be combined with LAN16 as follows: **MSZ** **LAN16** **SIZE** 0 0 8 Kbytes 0 1 16 Kbytes 1 0 32 Kbytes 1 1 64 Kbytes
D2	IR2	Used to select the second set of IRQ lines. See IRR register.
D1	OTHER REGISTER ACCESS	This bit idetermines whether the BIOS ROM Address Register (BIO) or the EEROM Address Register (EAR) is enabled. At power up, BIO is enabled. 0 = BIO; 1 = EAR.
D0	BIT16	16-BIT BUS When the WD83C584 is used in an 8-bit interface, this bit is read/writable. When used in a 16-bit interface, it will always read a 1.

4.4 I/O ADDRESS REGISTER (IAR)

Offset 0x02, (Read/Write)

The IAR sets the I/O address of the board. If the INIT2, INIT1, INIT0 pins are "001" at power-up, the I/O address will be hard initialized at 280.

	D7 IA15	D6 IA14	D5 IA13	D4 IA9	D3 IA8	D2 IA7	D1 IA6	D0 IA5
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	IA15	I/O ADDRESS BITS
D6	IA14	Must be set to the I/O address at which you want the board to be placed. These
D5	IA13	bits correspond to system address bits SA15 thru SA13 and SA9 thru SA5.
D4	IA9	For example, address 0x280 could be selected by writing to 0x14 to this register.
D3	IA8	
D2	IA7	
D1	IA6	
D0	IA5	

Note: Address bits SA15 through SA13 can be used to select multiple boards while still taking up what is normally considered only 32 bytes of I/O space.

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4.5 BIOS ROM ADDRESS REGISTER (BIO)

EEROM Address Register (EAR)
Offset 0x03, (Read/Write)

There are two registers at this offset. Depending on what was **last written** to ICR-D1 (OTHER) one register or the other will be accessed.

ICR-D1 = 0:BIO will be accessed
ICR-D1 = 1:EAR will be accessed.

The BIO sets the memory address of the BIOS ROM.

The ROM socket may be populated with a 64K ROM, a 32K RAM, or a 32K FLASH ROM.

	D7 RS1	D6 RS0	D5 BA18	D4 BA17	D3 BA16	D2 BA15	D1 BA14	D0 INT
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	RS1	BIOS ROM SIZE
D6	RS0	RS1 RS0 0 0 ROM cannot be accessed 0 1 16 Kbyte ROM 1 0 32 Kbyte ROM 1 1 64 Kbyte ROM
D5	BA18	BIOS ROM MEMORY ADDRESS BITS
D4	BA17	Must be set to the memory address at which you want the BIOS ROM is to be
D3	BA16	placed. These bits correspond to system memory address bits SA18 through
D2	BA15	SA13. SA19 is assumed to be a "1". For example, a 16 Kbyte ROM at
D1	BA14	D8000 could be selected by writing 0x6C to this register.
D0	INT	Setting this bit raises one of the IRQ lines to the PC. This may be used as a software interrupt. It must be reset to remove the IRQ.

4.6 EEROM ADDRESS REGISTER (EAR)

The EAR allows additional EEROM to be accessed. In order to access this register a "1" should be written to ICR-D1 (OTHER).

Operation of EEROM is as follows:

During power up or recall, 8 bytes of EEROM are loaded into the WD83C584 first 8 registers. Which 8 bytes are read depends on the position of the INIT input jumper pins. In the case that the INIT pins are all unjumpered (all 1s), bytes from 0X00 to 0X0F will be read. In all cases, these bytes will be from EEROM locations between 0X00 and 0X3F. During a store operation, the first 8 bytes are always written to the first 8 EEROM locations (0X00 through 0X07).

At power up, the EAR was set with EA6, EA5, EA4, EA3 = 1000. The next 8 bytes are read into the LAN address registers using the EAR register addresses. Thus the LAN address should be stored at 0X40.

When the ICR-D1 bit is set. This EAR register may be programmed to point at other EEROM addresses. A STO or RLA would then transfer between the LAN address registers and this other EEROM address.

During a recall, ICR-D1 bit is not changed. Also the BIOS ROM ADDRESS (BIO) is recalled to offset 3 and not this EAR. There is no EEROM backup for the EAR. During a STO, the BIO is stored.

When the ICR-D1 bit is set, the EAR is readable from the host, not the BIO.

	D7 EA6	D6 EA5	D5 EA4	D4 EA3	D3 RAM	D2 RPE	D1 RP1	D0 RP
RESET	1	0	0	0	0	0	0	0
INITIAL	1	0	0	0	0	0	0	0
POWER-UP	1	0	0	0	0	0	0	0
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	EA6	EEROM ADDRESS
D6	EA5	This determines which 8 bytes will be accessed with a recall or STO store.
D5	EA4	The default 0x80 says that bytesD4 EA3 0x40-0x47 will be read into the
D4	EA3	LAN registers. A 0x10 would cause bytes 0x08-0x0F to be stored or read to or from the LAN ADDRESS registers. When ICR-D1 = 0, the EEROM Address will be reset to 0x40.
D4	RAM	RAM Indicates that a 32K RAM is installed in the ROM socket.
D2	RPE	ROM PAGE
D1	RP1	RPE enables ROM paging. The RP1 and RP0 bits determine what page of
D0	RP0	ROM will be accessed. A page is equal to 16 Kbytes. Four 16-Kbyte pages are accessible.

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4.7 INTERRUPT REQUEST REGISTER (IRR)

Offset 0x04, (Read/Write)

The IRR controls which Interrupt Request will be used.

	D7 IEN	D6 IR1	D5 IR0	D4 FLSH	D3 OUT3	D2 OUT2	D1 OUT1	D0 OWS8
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	IEN	INTERRUPT ENABLE Enables the appropriate IRQ line onto the bus. The IRQ lines are tri-stated otherwise.
ICR-D2	IR2	INTERRUPT REQUEST
D6	IR1	These bits determine which Interrupt Request Line will be enabled. IR2
D5	IR0	is found as ICR-D2.

IR2	IR1	IR0
0	0	0 IRQ2/9
0	0	1 IRQ3
0	1	0 IRQ5
0	1	1 IRQ7
1	0	0 IRQ10
1	0	1 IRQ11
1	1	0 IRQ15
1	1	1 IRQ4

D4	FLSH	FLASH MEMORY This says that a 32K flash memory is in the ROM socket. It may be written to.
D3	OUT3	OUTPUT PINS
D2	OUT2	The three output pins follow the data stored on these bits.
D1	OUT1	
D0	0WS8	8-BIT ZERO WAIT STATE ENABLE If set to 0: Zero Wait State disabled . Every memory byte access will include 4 states. If set to 1: Zero Wait State enabled, 2 wait states will be included with every memory byte access.

4.8 LA ADDRESS REGISTER (LAAR)

Offset 0x05 (Read/Write)

The LA address bits are used to decode the high order memory address when operating in 16-bit memory access mode. This register contains the LA bits which the memory will be compared against. This register has LA address bits LA23-19. Bits A18 and A17 are selected in the Memory Address register.

	D7 M16EN	D6 L16EN	D5 OWS16	D4 LA23	D3 LA22	D2 LA21	D1 LA20	D0 LA19
RESET	0	0	0	0	0	0	0	1
INITIAL	0	0	0	0	0	0	0	1
POWER-UP	0	EE	EE	EE	EE	EE	EE	EE
RECALL	0	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	M16EN	ENABLE 16 BIT MEMORY ACCESS Set to 1 to enable 16-bit memory access. This bit should only be set when all other interrupts have been disabled.
D6	L16EN	ENABLE 16 BIT LAN OPERATION Set to 1 to allow 16-bit operation between the LAN controller and the on-board RAM memory. This bit has another function, when operating in 8 bit mode only 8K byte RAM will be used. In 16-bit mode, the entire RAM (either 16K byte or 64K byte) will be available.
D5	0WS16	0WS 16 ENABLE Enable zero wait state operation when running 16 bit memory accesses.
D4-0	LA23-19	LA MEMORY DECODE BITS Must be set to select the address at which the shared memory is to be accessed. These bits correspond to system memory address bits LA23 through LA19. For example, to select and enable base address register D0000, write a 0x01 to this register and 0x68 to the memory address register.

4.9 INITIALIZE JUMPER REGISTER

Offset 0x06 (Read)

PIN	NAME	DESCRIPTION
D7		Undefined, will read a "0".
D6	IN2	INPUT PINS
D5	IN1	These bits read the state of the 2 input pins.
D4,3		Undefined, will read a "0".
D2	INIT2	INITIALIZE PINS
D1	INIT1	These read the contents of the 3 initialize pins. They are active low.
D0	INIT0	

4.10 GENERAL PURPOSE REGISTER 2 (GP2)

Offset 0x07 (Read/Write)

The GP2 is a byte register which is completely undefined and may be used as needed by software.

	D7	D6	D5	D4	D3	D2	D1	D0
RESET	?	?	?	?	?	?	?	?
INITIAL	EE	EE	EE	EE	EE	EE	EE	EE
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

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4.11 LAN ADDRESS REGISTERS (LAR)

Offset 0x08-0x0F

The LAN Address Registers contains the unique LAN address that has been assigned to a board. It should be read and written to the LAN controller. Bytes of the LAN address may be read at the offsets given below.

	D7	D6	D5	D4	D3	D2	D1	D0
RESET	?	?	?	?	?	?	?	?
INITIAL	EE	EE	EE	EE	EE	EE	EE	EE
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

OFFSET	DESCRIPTION
0x08	Globally Assigned Address Block (LSB)
0x09	Globally Assigned Address Block
0x0A	Globally Assigned Address Block (MSB)
0x0B	Unique Board Address (LSB)
0x0C	Unique Board Address
0x0D	Unique Board Address
0x0E	WD Board ID Byte
0x0F	Checksum, causes the twos complement sum of all 8 LAN Address Register bytes to be 0xFF.

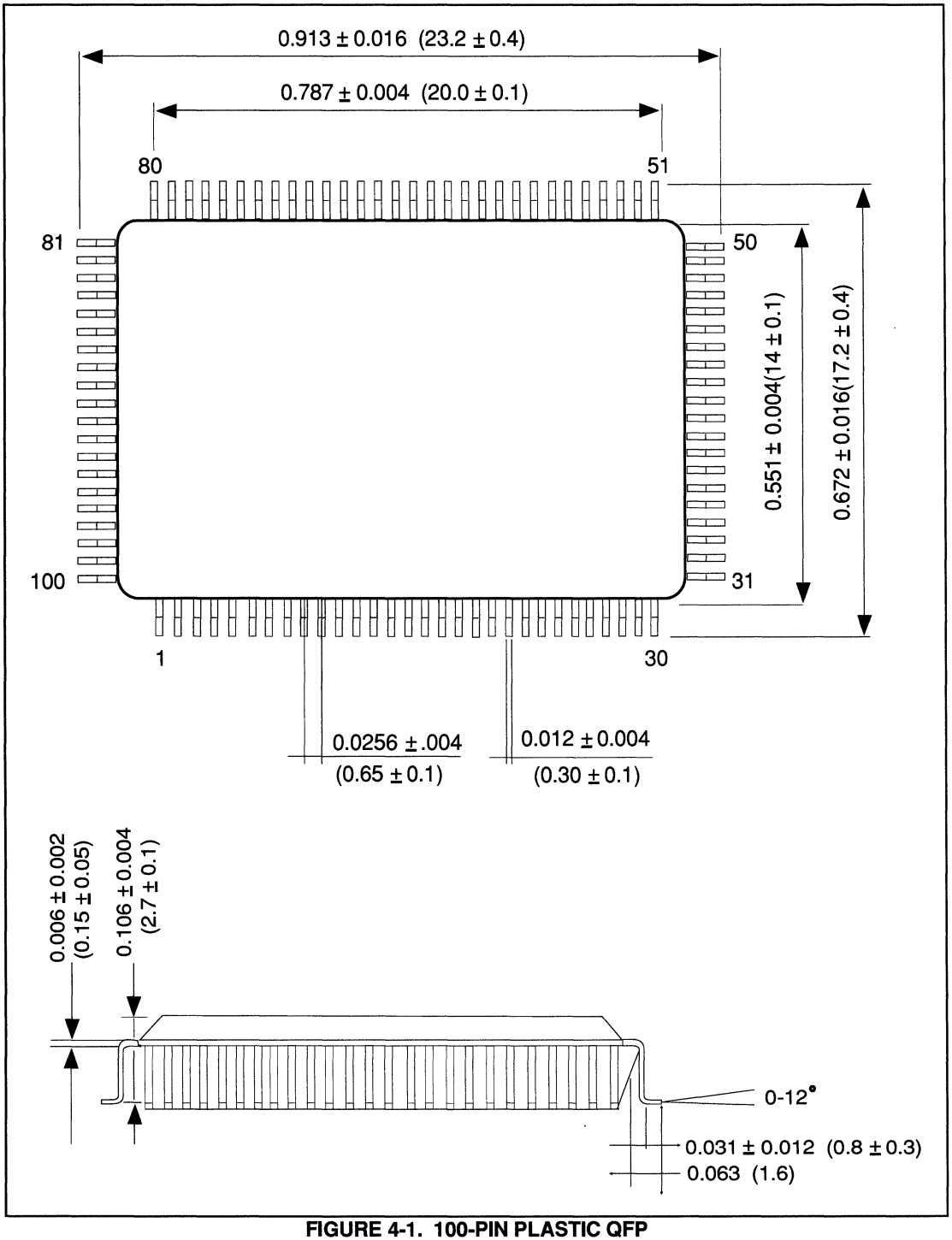

FIGURE 4-1. 100-PIN PLASTIC QFP

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5.0 TIMING DIAGRAMS

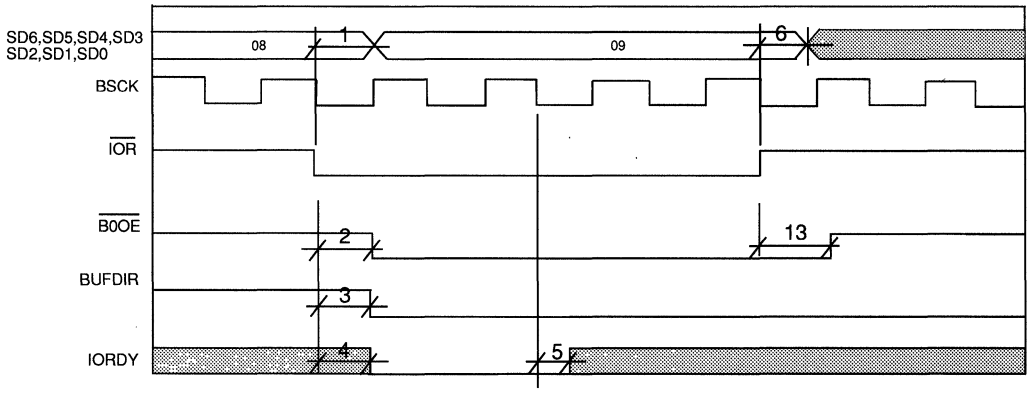

FIGURE 5-1. I/O READ

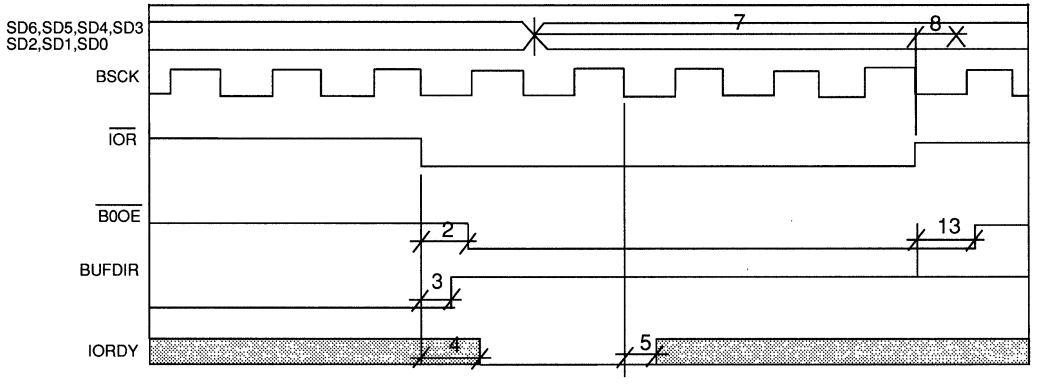

FIGURE 5-2. I/O WRITE

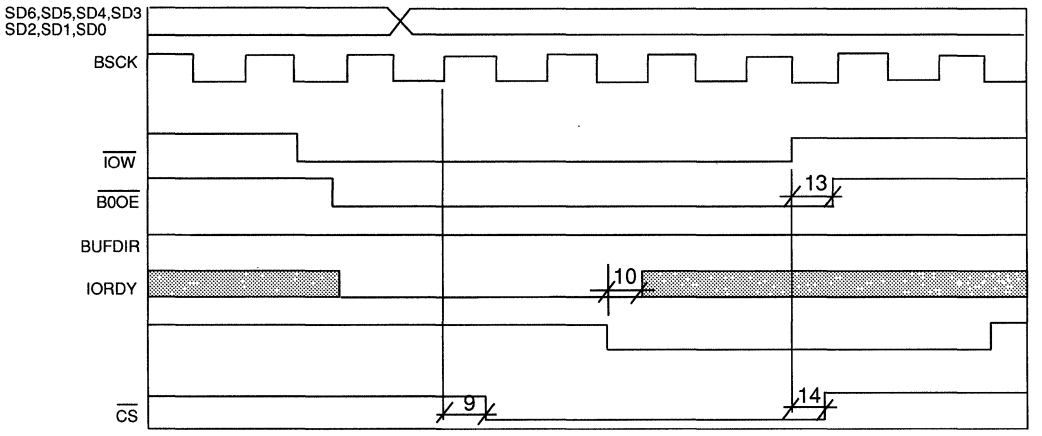

FIGURE 5-3. I/O WRITE TO LAN CONTROLLER

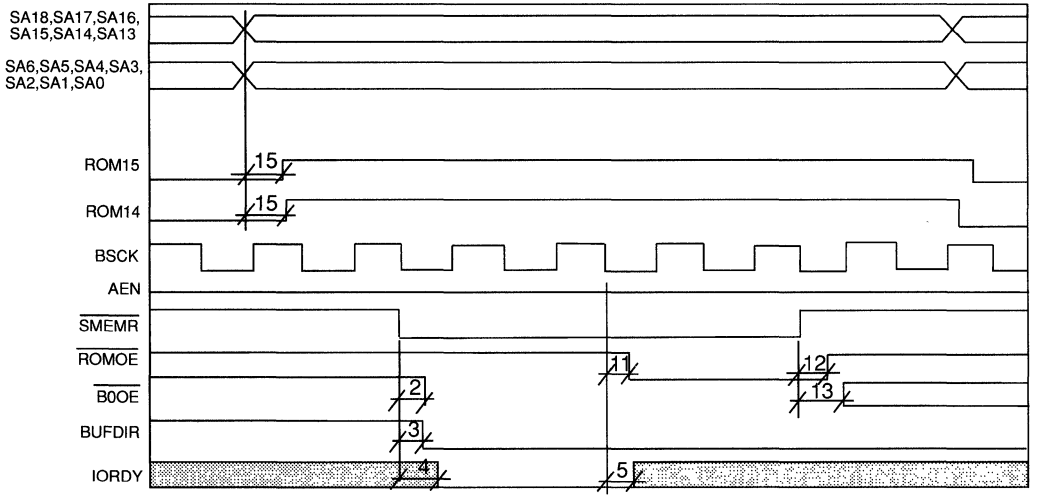

FIGURE 5-4. ROM READ

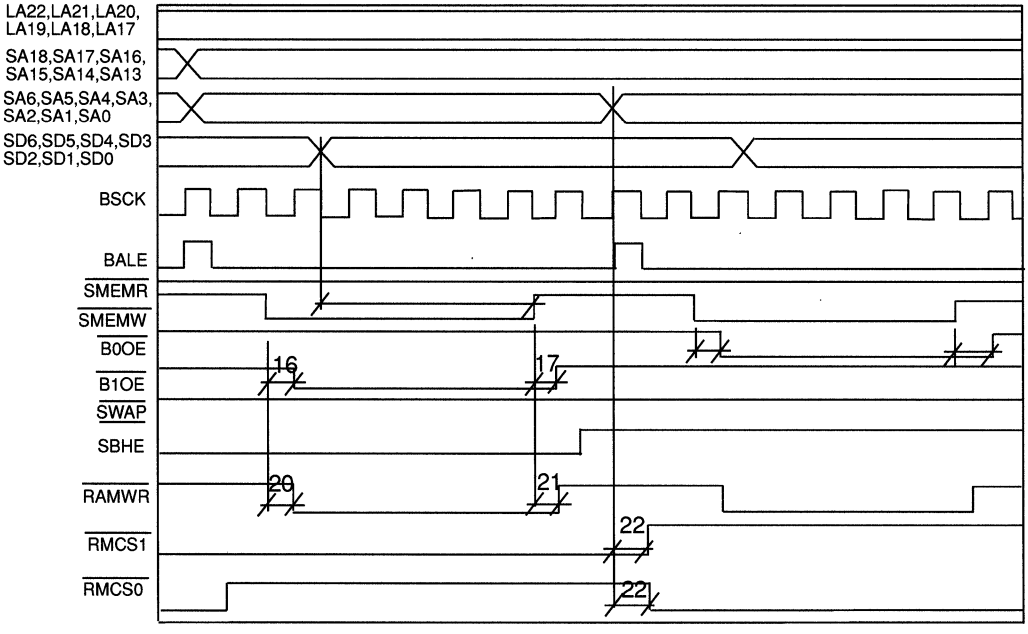

FIGURE 5-5. RAM WRITE, 8 BIT

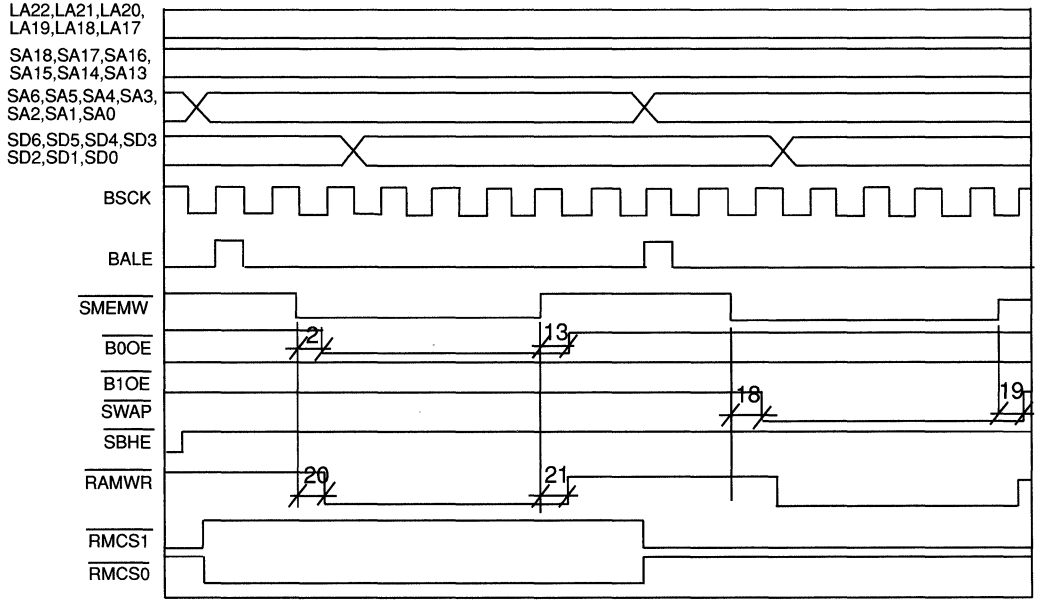

FIGURE 5-6. RAM WRITE, 8 BIT

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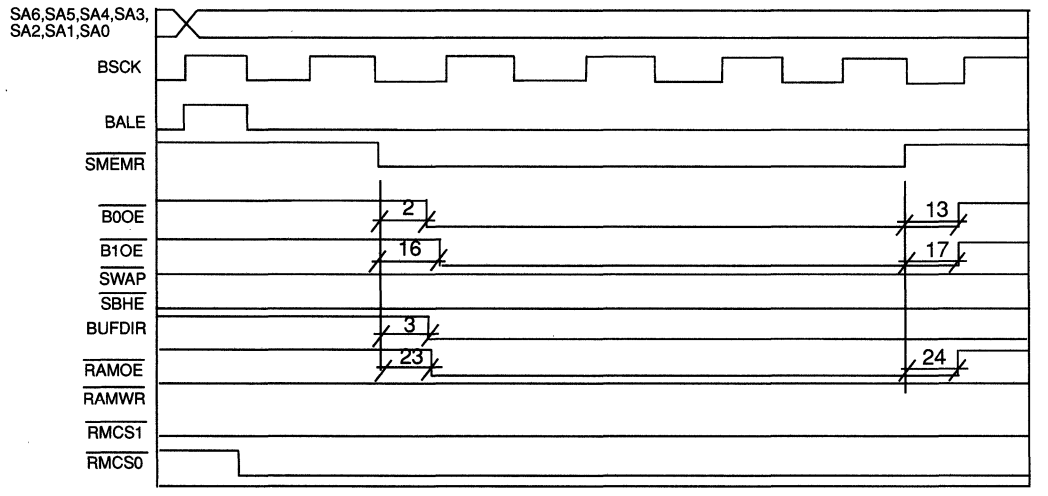

FIGURE 5-7. RAM READ, 16 BIT

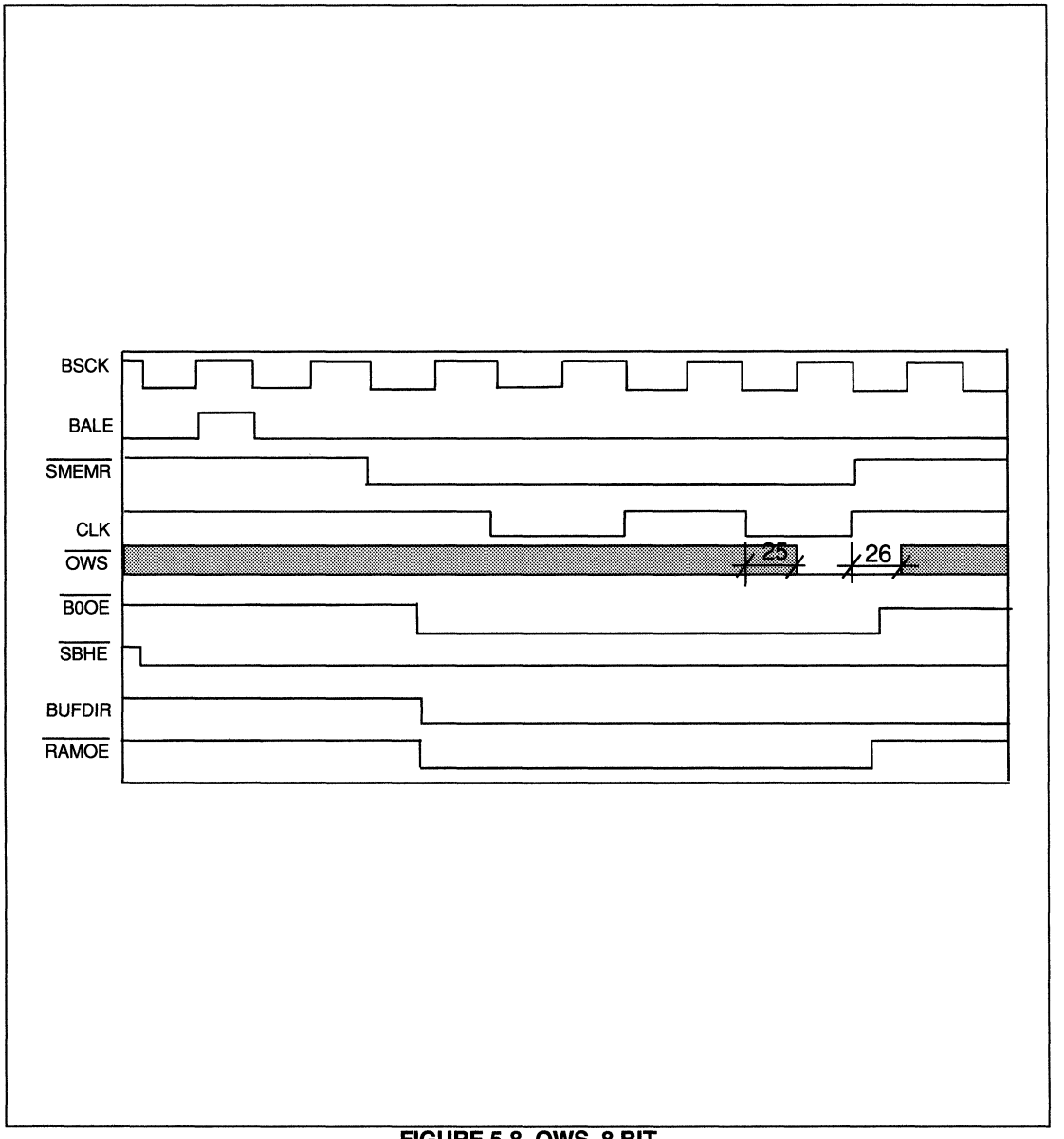

FIGURE 5-8. OWS, 8 BIT

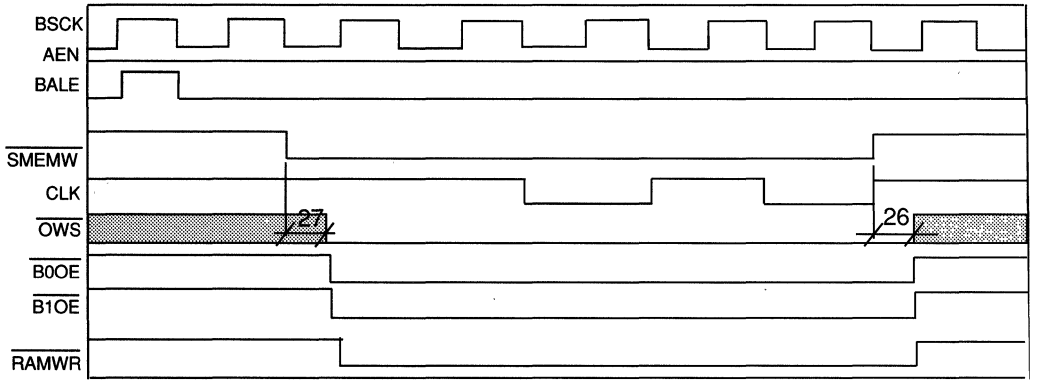

FIGURE 5-9. OWS, 16 BIT

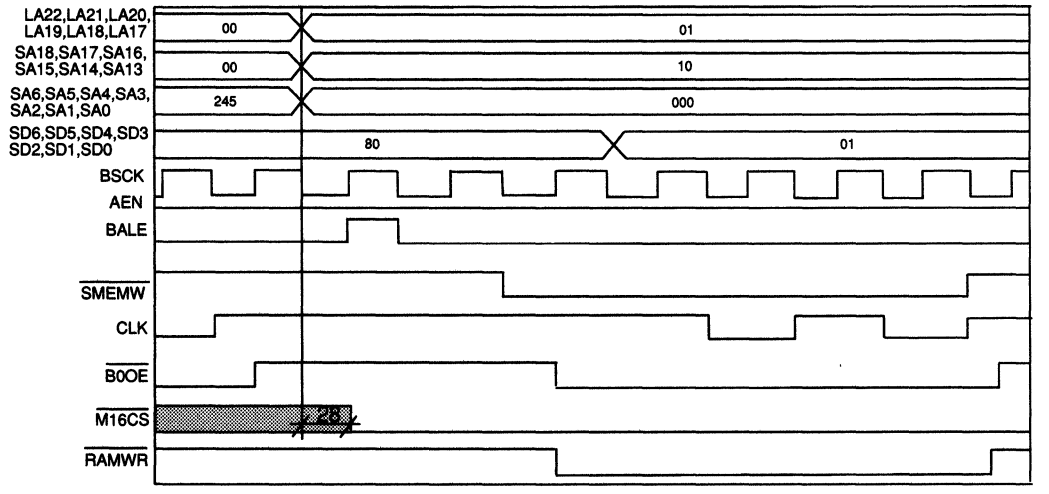

FIGURE 5-10. M16CS

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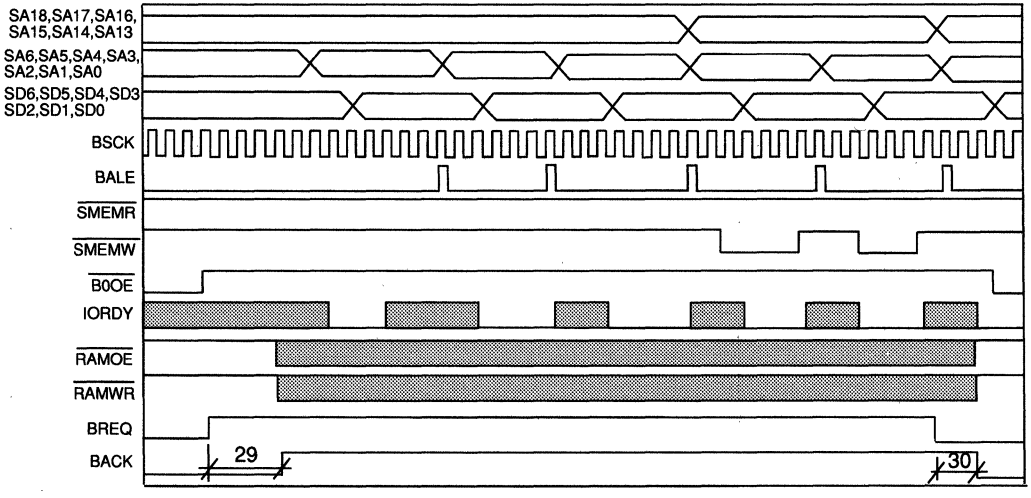

FIGURE 5-11. BREQ/BACK

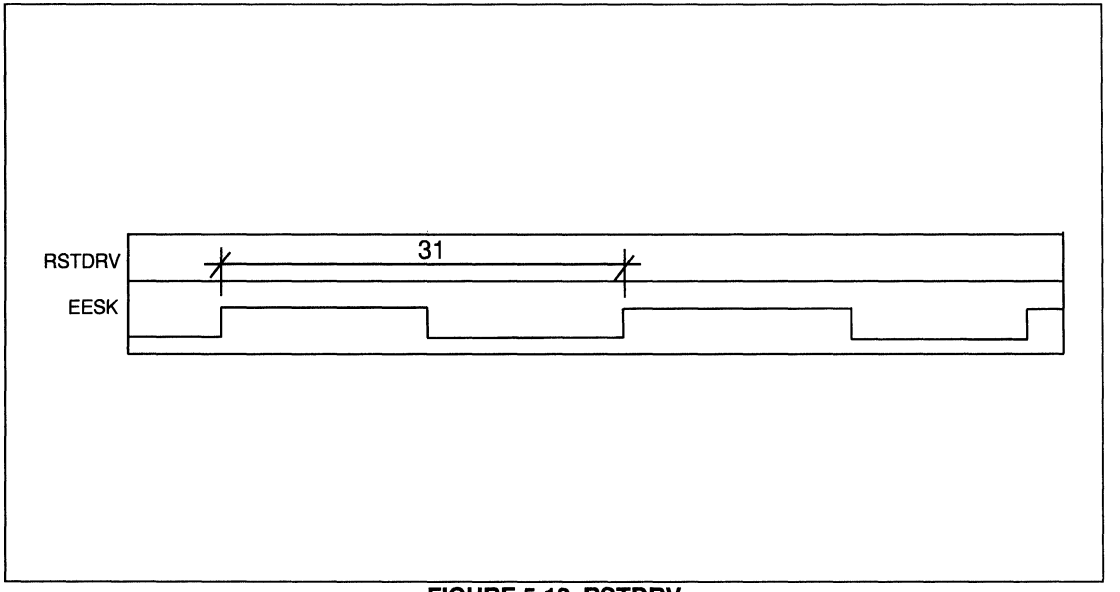

FIGURE 5-12. RSTDRV

t	DESCRIPTION	MIN	TYP	MAX
1	Read/Write Strobe to data valid	11		26 ns
2	Read/Write Strobe to $\overline{\text{BOOE}}$ low	8		21
3	Read/Write to BUFDIR change	9		17
4	Read/Write to IORDY low	9		23
5	BSCK to IORDY tri-state	14		34
6	Read Strobe to Data tri-state	6		17
7	Register Write Data Setup	5		
8	Register Write Data Hold			18
9	BSCK to $\overline{\text{CS}}$ low	12		30
10	ACK to IORDY tri-state	7		16
11	BSCK to $\overline{\text{ROMOE}}$ low	12		29
12	Read Strobe to $\overline{\text{ROMOE}}$ high	6		13
13	Read/Write Strobe to $\overline{\text{BOOE}}$ high	8		20
14	Read/Write Strobe to $\overline{\text{CS}}$ high	6		14
15	Address to ROM15, ROM14 change	7		18
16	Read/Write Strobe to $\overline{\text{B1OE}}$ low	8		19
17	Read/Write Strobe to $\overline{\text{B1OE}}$ high	8		21
18	Read/Write Strobe to $\overline{\text{SWAP}}$ low	9		23
19	Read/Write Strobe to $\overline{\text{SWAP}}$ high	10		24
20	Write Strobe to $\overline{\text{RAMWE}}$ low	6		16
21	Write Strobe to $\overline{\text{RAMWE}}$ high	6		15
23	Read Strobe to $\overline{\text{RAMOE}}$ low	12		16
24	Read Strobe to $\overline{\text{RAMOE}}$ high	6		14
25	CLK to $\overline{\text{OWS}}$ (8 bit) low	8		20
26	Read/Write Strobe to $\overline{\text{OWS}}$ tri-state	11		27
27	Read/Write Strobe to $\overline{\text{OWS}}$ (16 bit) low	7		17
28	Address to M16CS low	8		19
29	BREQ to BACK high	250		
30	BREQ to BACK low	50		
31	ESCK Period		6400	

TABLE 5-1. WD83C584 TIMING

APPENDIX A - SOFTWARE COMPATIBILITY

Compatibility of the WD83C584 with previous products is especially important. This section describes in what areas the WD83C584 is incompatible with the previous WD83C583. These incompatibilities are minor and should require little or no software changes. Changes to be made will be related to setup programs, since they are used to set up and configure the EEPROM data.

- The WD83C584 requires 2 ms to read all 16 registers after power-up or a RECALL instruction. Register 0x01 may be polled to determine the finish of this read. The WD83C583 reads its internal EEPROM within 5 ms.
- The WD83C584 requires 200 ms to store EEPROM and may be polled to determine finish, whereas the WD83C583 required 20 ms and gave no indication of finish.
- MSZ (ICR-D#) on the WD83C584 shows SRAM size, not total RAM size.
- ICR-D@ on the WD83C584 is used as IR2. It was DMA on the 83C583 and was always a 0.
- ICR-D0 on the WD83C584 is 16BIT. ITs function has totally changed. In the 83C583, it was WTS.
- IRR-D2 and D1 on the WD83C584 are not used. They were effectively not used in the 83C583.
- The user can select 1 of 8 groups of 8 bytes each to be loaded into the WD83C584 from the EEPROM at power up. To be compatible with previous WD83C583 setup programs, the WD83C584 setup program will need to be modified so that 1of the 8 groups represents the setup data used with the previous WD83C583 device.

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APPENDIX B - ELECTRICAL OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{dd}	VDD Supply Current			40	mA	
V_{dd}	Voltage Supply	4.75	5	5.75	V	
V_{ih}	Input High Voltage	2.0			V	
V_{il}	Input Low Voltage				V	
V_{ils}	Input High Voltage (Schmitt)	2.5	20,21,33 34,99	0.6		
V_{ihs}	Input Low Voltage (Schmitt)	2.5	20,21,33 34,99	0.6		
V_{oh}	Output High Voltage	V_{dd}-.4			V	I_{oh} = -2mA
V_{ol}	Output Low Voltage			V_{ss}+.4	V	I_{ol} = 6mA
V_{olc}	Output Low Voltage (Open Collector)			V_{ss}+.4		I_{ol}=24mA
I_{l}	Input Leakage Current	-10		10	µA	V_{ih}=V_{dd}
I_{oz}	Tristate High Current	-10		10	µA	V_{in}=V_{dd}
R_{pu}	Pull-up Resistor	-50	21,34,35 48,49,50 77,81,82 91-99	500	K	

TABLE B-1. DC PARAMETER CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Storage Temperature	-65		150	Deg.C
Voltage on any pin with respect to Vss	-0.6		Vdd+0.3	Volts
Voltage on Vcc with respect to Vss			7.0	Volts

TABLE B-2. NON-OPERATIONAL SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature	0	25	70	Deg.C
Humidity	10		95	Percent

TABLE B-3. OPERATIONAL SPECIFICATIONS