WD83C593

Micro Channel Bus Interface

Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

FIGURES

TABLES

39

1.0 DESCRIPTION AND APPLICATION

The WD83C593 is a Micro Channel bus interface controller designed for non-intelligent Ethernet or StarLAN boards. The device is used as an interface to the LAN controller, BIOS ROM, buffer RAM (which functions as shared memory), and the host Micro Channel bus.

1.1 FEATURES

- Direct interface between a non-intelligent Ethernet or StarLAN LAN controller and a Micro Channel bus
- Ten bytes of internal electrically erasable programmable read only memory (EEPROM)
- 84-pin ASIC, 2.0 micron CMOS technology
- Programmable BIOS ROM size (16, 32, or 64 Kbytes)
- Programmable RAM size (16 or 64 Kbytes)
- Single, 5V power supply
- Four Vcc, ground, and program-selectable IRQ pins
- Testable/programmable before and after assembly

1.2 THEORY OF OPERATION

The WD83C593 non-intelligent interface device connects the Micro Channel bus (as a non-DMA slave) to the LAN controller, BIOS ROM, and buffer RAM. The WD83C593 satisfies all necessary interface requirements, performs all decoding for local I/O and memory spaces, and generates the necessary chip select control and handshake signals.

In order for the WD83C593 non-intelligent Micro Channel bus interface device to function properly, the mode select pin must be left open (internally pulled high).

This enables the WD83C593 to arbitrate between the host and WD83C690 LAN controller for the BD00-BD15 data bus. During local WD83C690 DMA bursts in and out of the buffer RAM, the device isolates the BD data bus from the Micro Channel via external buffering, and prevents the host from intervening until the process is complete. When a valid decode occurs, the device negates the CDCHRDY signal.

The remainder of the time, the device enables the external buffers so that the host can perform memory or I/O cycles (anywhere on the card). The host uses a 16-bit wide "move" string operation to transfer data to and from the buffer RAM. During this time, the WD83C593 generates the RAM control signals (tri-state during local RAM accesses).

3 9

2.0 POS REGISTERS AND DECODING

Designers of Micro Channel adapters are required by the Micro Channel architecture to use two read-only ID bytes and (up to) six read/write programmable option select (POS) registers. This arrangement accomplishes the following:

- eliminates switches and jumpers
- permits the installation of multiple identical cards
- allows the identification of any card by slot
- resolves resource assignment conflicts

Designers are also required to provide an adapter description file (.ADF) that reports the contents of the ID bytes, the number of POS registers used on the card, their purpose and contents, and their "alternate contents."

The Micro Channel bus defines the architecture of the following bits:

POS[2] bit 0.......Card enable (address 102h)

POS[5] bit 7.......CH CK active indicator (105h)

POS[5] bit 6.......CH CK status available
                   indicator (105h)

The remaining POS registers are "free form" and can be used for space decoding, establishing arbitration levels, and so on. When the system is reset, each adapter must turn off the card enable bit, which in turn disables all outputs from the card, including the interrupt request lines.

The central configuration software checks all slots independently for ID bytes, and uses the .ADF files provided to resolve conflicts and set up the POS registers. It is during this time only that the POS registers can be accessed, and they can be accessed only by the configuration software.

The CDSETUP line, together with the least significant three address lines, is used for decoding POS register accesses.

2.1 Space Decodings

Three POS registers, POS[2], POS[3], and POS[4], are used to decode the card I/O space, shared RAM space, and BIOS ROM space, respectively. The mode select pin, as indicated previously, must be left open.

2.1.1 POS[2] Register

Bit	Bit Assignment
7	LA11
6	LA10
5	LA09
4	LA08
3	LA07
2	LA06
1	LA05
0	CDEN

If a 29h is written in POS[2], the WD83C593 I/O space is placed in the range 280h - 029Fh. This is one of 128 possible 32-Kbyte ranges. For each of the primary and alternate choices, one or more interrupt levels are defined in the .ADF file.

Bit (7:1)

These bits are used to decode the I/O space for the application.

Bit 0

Card Enable.
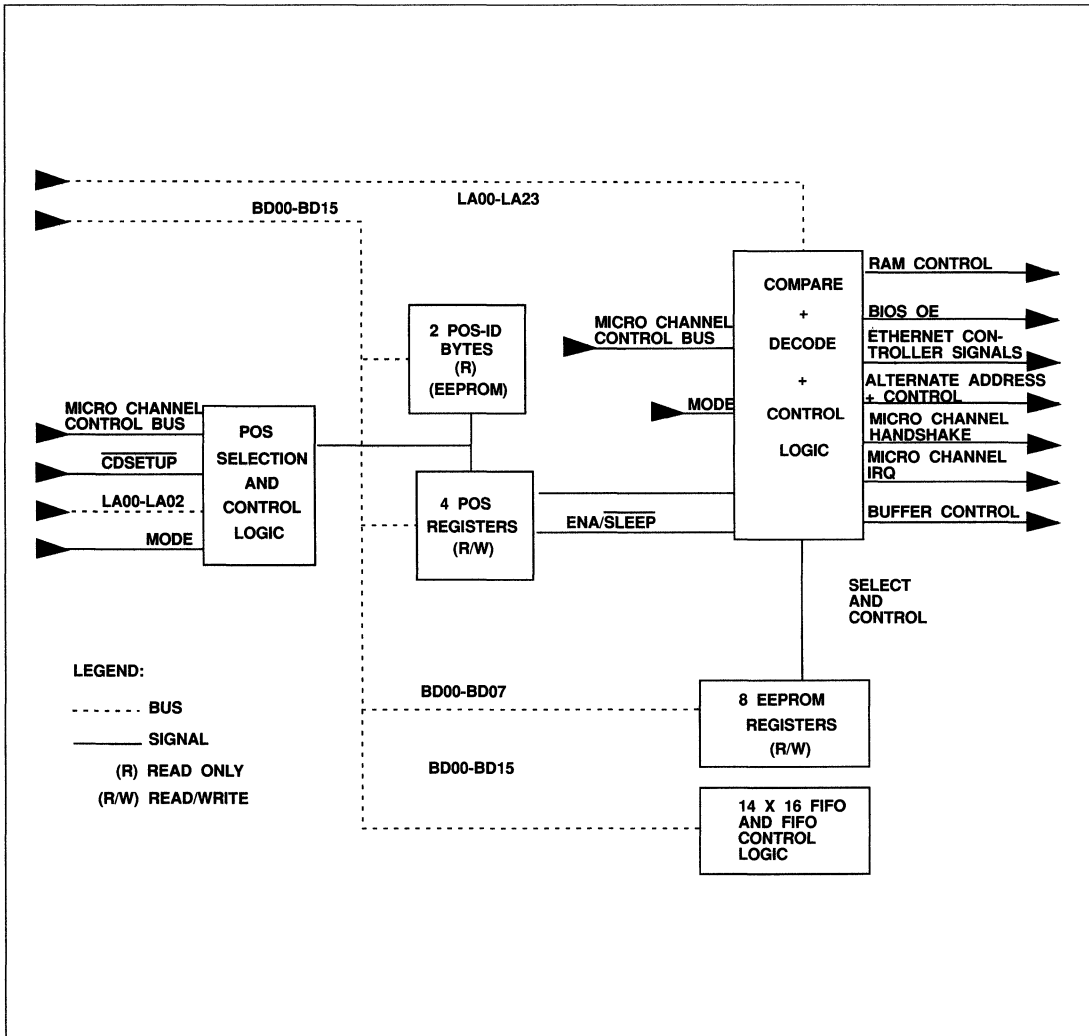Bit 0 wakes up low and, until it is set by the configuration routine, keeps the card in "sleep" mode.

```
                                                              RAM CONTROL
                   BD00-BD15          LA00-LA23
                                                   COMPARE   BIOS OE
                                                      +
                                     MICRO CHANNEL   DECODE  ETHERNET CON-
                         2 POS-ID    CONTROL BUS             TROLLER SIGNALS
                          BYTES                         +    ALTERNATE ADDRESS
                           (R)                 MODE  CONTROL + CONTROL
   MICRO CHANNEL        (EEPROM)                             MICRO CHANNEL
   CONTROL BUS   POS                                LOGIC   HANDSHAKE
                 SELECTION                                  MICRO CHANNEL
     CDSETUP     AND                                        IRQ
                 CONTROL     4 POS                          BUFFER CONTROL
    LA00-LA02    LOGIC      REGISTERS   ENA/SLEEP
                            (R/W)
      MODE
                                                           SELECT
                                                           AND
                                                           CONTROL

   LEGEND:
   - - - - - -  BUS
                           BD00-BD07       8 EEPROM
   ————  SIGNAL                            REGISTERS
     (R) READ ONLY                          (R/W)
                           BD00-BD15
     (R/W) READ/WRITE
                                           14 X 16 FIFO
                                           AND FIFO
                                           CONTROL
                                           LOGIC
```

FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM

2.1.2 POS[3] Register

Bit	Bit Assignment
7	LA19
6	LA18
5	LA17
4	LA16
3	LA15
2	LA14
1	PME
0	CLAIM

If a C2h is written in POS[3], the shared RAM space is placed in the range 0C0000h - 0C3FFFh. This is one of 64 possible 16-Kbyte ranges. It is intended to place shared RAM in the general range, 0C0000h - 0DFFFFh.

Bit (7:2)

These bits are used to set the shared RAM space for the application.

Bit (1:0)

Memory Enable; Claim.
Bit 1 wakes up low and, until it is set by the configuration routine, keeps the RAM buffer disabled. Bit 0 is provided for use by the driver software (to identify availability when multiple cards are used in the same system).

2.1.3 POS[4] Register

Bit	Bit Assignment
7	LA19
6	LA18
5	LA17
4	LA16
3	LA15
2	LA14
1	BE1
0	BE0

If a D0h is written in POS[4], the BIOS ROM space is placed in the range 0D0000h - 0D3FFFh. This is one of 64 possible 16-Kbyte ranges. It is intended to place the BIOS ROM in the general range, 0C0000h - 0DFFFFh.

Bit (7:2)

These bits are used to set the BIOS ROM location for the application.

Bit (1:0)

BIOS Size/Enable.
Bits 1 and 0 are used to set the size of the BIOS ROM and, when necessary, to disable it as follows:

BE1	BE0	FUNCTION
0	0	BIOS is 16 Kbytes
0	1	BIOS is 32 Kbytes
1	0	BIOS is Disabled
1	1	BIOS is 64 Kbytes

2.2   Other POS Functions ! POS[5] Register

POS[5] provides bits that increase memory size, divide the BSCK clock by "2" (for internal use), and enable /disable interrupts to the host.

Bit	Bit Assignment
7	CH CK
6	CH CK
5	N/A
4	N/A
3	MSE
2	CDIV
1	IEN1
0	IEN0

Bit (7)

Active Indicator (Micro Channel defined).

Bit (6)

Status Available Indicator (Micro Channel defined).

Bit (5:4)

Not applicable.

Bit 3

Memory Size Enable.
When set to "1", this bit increases the memory size from 8 x 16 Kbytes to 32 x 16 Kbytes.

Bit 2

Clock Divider.
This bit, when reset, divides the BSCK clock by "2" for internal use. When the system is powered off, the bit is reset.

Bit (1:0)

Interrupt Enable.
Together, these bits enable/disable the interrupts to the host, and determine the level of the interrupt as follows.

IEN1	IEN0	FUNCTION
0	0	Interrupt level is IRQ0
0	1	Interrupt level is IRQ1
1	0	Interrupt level is IRQ2
1	1	Interrupt level is IRQ3

39

3.0 PROGRAMMING THE EEPROM REGISTERS

The WD83C593 contains ten, internal eight-bit registers implemented in EEPROM technology (see Table B-2). These registers contain random data when the device is shipped from the factory and must be programmed by you for your application. If they are not, the device will not function properly.

To initially program the EEPROM registers, you must write the data to be sorted to each register. Figure 3-1 illustrates a typical EEPROM register bit cell. Data is stored in the latch and its output is presented to the input of the EEPROM cell. Once the data is stored in the registers, you must write the following to the EEPROM control register: A5h (followed by) 00h. It is important that you write the numbers in the order given. This starts the programming process of all ten EEPROM registers with data stored in the latches. The program operation requires a maximum of 20 milliseconds to complete. During this time, it is important that you do not access any of the registers in the device. Refer to Appendix B for more information on the EEPROM registers.
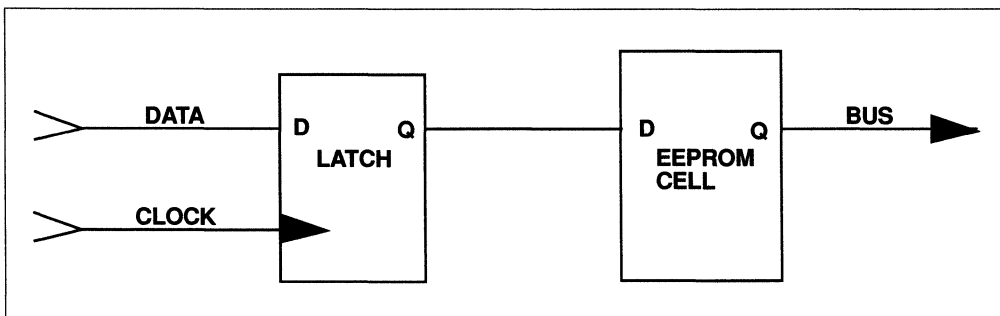

FIGURE 3-1. TYPICAL EEPROM REGISTER BIT CELL

APPENDIX A -- PIN DESIGNATIONS

Figure A-1 illustrates the 84-pin PLCC device.
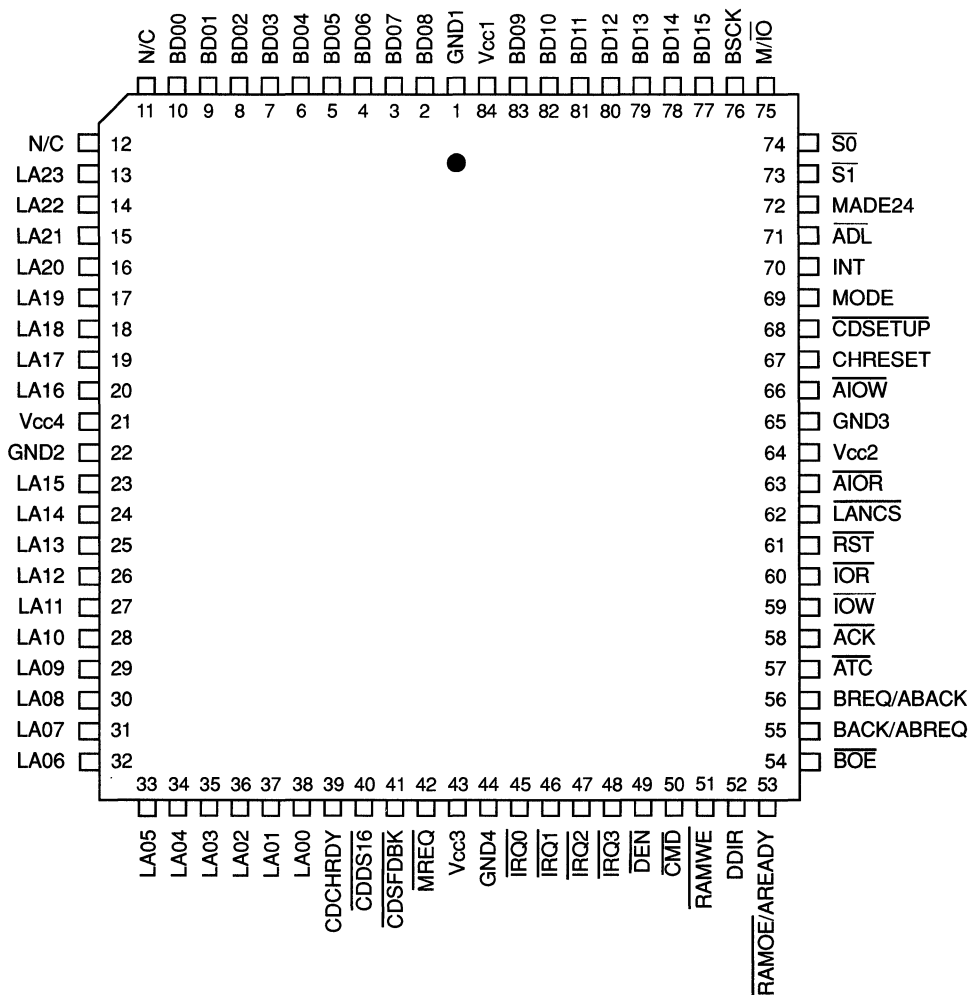Table A-1 lists all pin designations.

Top pins (left to right): N/C, BD00, BD01, BD02, BD03, BD04, BD05, BD06, BD07, BD08, GND1, Vcc1, BD09, BD10, BD11, BD12, BD13, BD14, BD15, BSCK, M/$\overline{IO}$

Pin numbers top row: 11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75

Left side:
Pin	Number
N/C	12
LA23	13
LA22	14
LA21	15
LA20	16
LA19	17
LA18	18
LA17	19
LA16	20
Vcc4	21
GND2	22
LA15	23
LA14	24
LA13	25
LA12	26
LA11	27
LA10	28
LA09	29
LA08	30
LA07	31
LA06	32

Right side:
Number	Pin
74	$\overline{S0}$
73	$\overline{S1}$
72	MADE24
71	$\overline{ADL}$
70	INT
69	MODE
68	$\overline{CDSETUP}$
67	CHRESET
66	$\overline{AIOW}$
65	GND3
64	Vcc2
63	$\overline{AIOR}$
62	$\overline{LANCS}$
61	$\overline{RST}$
60	$\overline{IOR}$
59	$\overline{IOW}$
58	$\overline{ACK}$
57	$\overline{ATC}$
56	BREQ/ABACK
55	BACK/ABREQ
54	$\overline{BOE}$

Pin numbers bottom row: 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53

Bottom pins (left to right): LA05, LA04, LA03, LA02, LA01, LA00, CDCHRDY, $\overline{CDDS16}$, $\overline{CDSFDBK}$, MREQ, Vcc3, GND4, $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQ3}$, $\overline{DEN}$, CMD, RAMWE, DDIR, RAMOE/AREADY

FIGURE A-1. 84-PLCC PINOUT

39

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
Host Micro Channel Bus Signals		
2-10 77-83	BD00-BDI5 (I/O)	HOST MICRO CHANNEL DATA BUS: This bus needs to be externally buffered.
11	$\overline{\text{REFRESH}}$ (I)	REFRESH CYCLE: Input from host system. Indicates when a system memory refresh cycle is taking place.
15-20 23-38	LA00-LA21 (I)	HOST MICRO CHANNEL ADDRESS LINES: These are the 20 bits of the host Micro Channel address lines.
39	CDCHRDY (O)	CHANNEL READY: This output, normally active, is pulled inactive to allow additional time to complete a channel operation.The maximum time that this line can be held inactive is 3.5 μsec.
40	$\overline{\text{CDDS16}}$ (O)	CARD DATA SIZE 16: This output is used to indicate to the host Micro Channel that the current data transfer is 16 bits wide. It is derived from a valid address decode.
41	$\overline{\text{CDSFDBK}}$ (O)	CARD SELECTED FEEDBACK: This output is asserted as an acknowledgement when an I/O or memory device on the LAN card is selected.
45-48	$\overline{\text{IRQ}}$0-3 (O)	INTERRUPT REQUEST: These outputs tell the host micro-processor that an interrupt has occurred and the LAN card needs attention.
50	$\overline{\text{CMD}}$ (I)	COMMAND: This input is used to define when data is valid on the data bus. The trailing edge of the signal indicates the end of the bus cycle.
67	CHRESET (I)	CHANNEL RESET: This signal is generated by the host when the host Micro Channel is powered up.
68	$\overline{\text{CDSETUP}}$ (I)	CARD SETUP: This input is generated by the host logic to individually select channel connectors during system configuration and error recovery procedures. This input, together with LA0-LA2, is used to access the POS registers. The $\overline{\text{CDSFDBK}}$ output is not asserted during configuration.

TABLE A-1. PIN DESCRIPTIONS

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
Host Micro Channel Bus Signals, Cont.		
71	$\overline{\text{ADL}}$ (I)	ADDRESS DECODE LATCH: This input is used to indicate that the Micro Channel addresses are to be latched. The trailing edge is used.
72	MADE24 (I)	MEMORY ADDRESS ENABLE 24: This input, when active, indicates that an unextended address space equal to or less than 16M is present on the address bus.
74, 73	$\overline{\text{S0}}$, $\overline{\text{S1}}$ (I)	STATUS BITS 0 AND 1: These inputs indicate the start of a channel cycle and also define the type of channel cycle as follows.

$\overline{\text{M/IO}}$	$\overline{\text{S0}}$	$\overline{\text{S1}}$	TYPE
0	0	0	Reserved A
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Reserved B
1	0	0	Reserved C
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved D

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
75	M/$\overline{\text{IO}}$ (I)	MEMORY/$\overline{\text{INPUT OUTPUT}}$: This input distinguishes a memory cycle from an I/O cycle.
LAN Controller Signals		
55	BACK/ABREQ (O)	LAN BUS ACKNOWLEDGE: This output is generated to acknowledge a LAN BUS REQUEST.
56	BREQ/ABACK (I)	LAN BUS REQUEST: This input is generated by the LAN controller to indicate that a DMA transfer is needed. It is automatically generated when the LAN controller's FIFO buffers need servicing.
58	$\overline{\text{ACK}}$ (I)	LAN SLAVE I/O ACKNOWLEDGE: This input is asserted by the LAN chip when it grants access to its internal registers. The input is used to insert wait states until the LAN is synchronized for a register read or write operation.
59	$\overline{\text{IOW}}$ (O)	LAN I/O WRITE: This output, together with $\overline{\text{LANCS}}$, is used to write to the internal LAN registers.

39

TABLE A-1. PIN DESCRIPTIONS (Continued)

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
LAN Controller Signals, Cont.		
60	$\overline{IOR}$ (O)	LAN I/O READ: This output, together with $\overline{LANCS}$, is used to read the internal LAN registers.
61	$\overline{RST}$ (O)	LAN RESET: This output places the LAN in reset mode immediately. No packets are received or transmitted by the LAN until the STA bit in the LAN is set.
62	$\overline{LANCS}$ (O)	LAN CHIP SELECT: This output places the LAN device in slave mode for access to internal registers.
70	INT (I)	LAN INTERRUPT: This input indicates that the LAN controller needs host attention (at the end of an operation, when an error occurs, etc.).
76	BSCK (I)	CLOCK: This input is the 40-MHz clock.
69	MODE (I)	ALTERNATE MODE SELECT: This input must be left open (internally pulled high). It signifies that the WD83C593 is being used on a non-intelligent board, directly interfacing the WD83C690 LAN controller to the buffer memory.
RAM Signals		
51	$\overline{RAMWE}$ (O)	RAM WRITE ENABLE: This output is used to write host data into the buffer RAM.
53	$\overline{RAMOE}/\overline{AREADY}$ (O)	RAM OUTPUT ENABLE: This output is used to gate the buffer RAM onto the data bus, BD00-BD15.
ROM Signal		
54	$\overline{BOE}$ (O)	BIOS ROM OUTPUT ENABLE: This output is the chip select for the BIOS ROM. It gates data onto BD0-BD7.
Buffer Control Signals		
42	$\overline{MREQ}$ (O)	MEMORY REQUEST: This output is provided for use in a possible memory mapped scheme. This is an unlatched memory decode indicator.
49	$\overline{DEN}$ (O)	DATA BUFFER ENABLE: This output is generated to enable or disable the external bidirectional data buffers.

TABLE A-1. PIN DESCRIPTIONS (Continued)

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
52	$\overline{\text{DDIR}}$ (O)	DATA DIRECTION: This output is generated to control the direction of the external bidirectional buffers between the host data bus and DB00-DB15 (local data bus).
Power		
21,43, 64,84	Vcc	+5V dc
1,22, 44,65	GND	GROUND.
No Connection		
11,12	N/C	Pins 11, 12 must be left open. They are used for factory testing.

TABLE A-1. PIN DESCRIPTIONS (Continued)

3 9

APPENDIX B -- REGISTER DESIGNATIONS

This appendix provides information on the WD83C593's internal registers. Table B-1 sum-marizes the I/O mapping, and the remainder of the appendix describes each register in detail.

Offset	Type	Name
0x00	R/W	Memory Enable, Reset Register (MER)
0x01	W	EEPROM Control Register (EEC)
0x02	R (EEPROM)	Reserved (PID0)
0x03	R (EEPROM)	Reserved (PID1)
0x05	R/W	Internal Mask and Command Control Register (IMCCR)
0x07	R/W	General Purpose Register (GPR)
0x08-0x0F	R (EEPROM)	LAN Address Registers (LAR)
0x10-0x1F	R/W	LAN Controller Registers (LAN)

TABLE B-1. INTERNAL REGISTER I/O MAP

Name: MEMORY ENABLE, RESET (MER)					**Offset:** 0x00		

Description: Only bits 7 and 6 in this register are used. Setting bit 7, and clearing it after 1 μsec, resets the LAN controller, as well as the other registers (except LAR, PID0, PID1 and FEX). Setting bit 6 enables the host Micro Channel to share the on-board buffer RAM. When bit 6 is cleared, RAM is disabled. A hard reset clears all bits in this register.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
REST	MENB	N/A	N/A	N/A	N/A	N/A	N/A

Name: EEPROM CONTROL (EEC)					**Offset:** 0x01		

Description: Writing A5h first and then 00h to this register starts the program process for the EEPROM registers. See the EEPROM programming instructions for a detailed description on how this register is used.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	0	1	0	0	1	0	1

Name: RESERVED (PID0)	**Offset:** 0x02

Description: This write-only register is used only by manufacturing to set the Micro Channel POS ID numbers.

Name: RESERVED (PID1)	**Offset:** 0x03

Description: This write-only register is used only by manufacturing to set the Micro Channel POS ID numbers.

TABLE B-2. REGISTER DESCRIPTIONS

Name: INTERNAL MASK AND COMMAND CONTROL   **Offset:** 0x05
       REGISTER (IMCCR)

Description: Bit 2 is cleared when the host Micro Channel is powered off or undergoes a soft reset.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
-	-	-	-	-	EIL	-	-

Note:

bit2 (EIL)   This bit is used to enable or disable an interrupt from the LAN controller to the host Micro Channel. The host Micro Channel sets this bit to "1" to enable the interrupt.

Name: GENERAL PURPOSE REGISTER (GPR)   **Offset:** 0X07

Description: This is an 8-bit wide general purpose register.

Name: LAN ADDRESS REGISTERS (LAR)   **Offset:** 0X08 - 0X0F

Description: The values for these eight read-only registers are permanently stored in the internal EEPROM. See EEPROM programming instructions.

Name: LAN CONTROLLER REGISTERS (LAN)   **Offset:** 0X10 - 0X1F

Description: These sixteen registers are physically located on the LAN controller chip. Only the decode and control circuitry is internal to the WD83C593.

TABLE B-2. REGISTER DESCRIPTIONS (Continued)

3 9

APPENDIX C - ELECTRICAL CHARACTERISTICS

Table C-1 lists the dc electrical parameters for the WD83C593, Table C-2 lists the non-operational specifications, and Table C-3 lists the operational specifications.

Ta = 0°C (32°F) to 70°C (158°F), Vcc = 5V % 10%

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	V_{DD} Supply Current	-	8	10	mA	-
V_{DD}	Voltage Supply	4.5	5	5.5	V	-
V_{IH}	Input High Voltage	2.0	-	-	V	-
V_{IL}	Input Low Voltage	-	-	0.8	V	-
V_{OH}	Output High Voltage	2.4	-	-	V	note 1
V_{OL}	Output Low Voltage	-	-	0.5	V	note 2
I_{LH}	Input Source Current	-	-	0.1	μA	$V_{IN} = V_{DD}$
I_{LL}	Input Sink Current	-	-	-1.0	μA	$V_{IN} = 0$
I_{OZH}	Tri-state High Current	-10	-	10	μA	$V_{IN} = V_{DD}$
I_{OZL}	Tri-state Low Current	-10	-	10	μA	$V_{IN} = 0$
V_{OL}	Output Low Voltage (Pins IRQ0, IRQ1, IRQ2, and IRQ3)	-	-	0.5	V	note 3
V_{OL}	Output Low Voltage (All pins except IRQ0, IRQ1, IRQ2, and IRQ3)	-	-	0.4	V	note 4

TABLE C-1. DC PARAMETERS

NOTES

1. I_{OH} = -24 mA on IRQ0, IRQ1, IRQ2 and IRQ3.

    I_{OH} = -8 mA on all other outputs and I/O pins.

2. I_{OL} = 0.5V (and 24 mA) on IRQ0, IRQ1, IRQ2, and IRQ3.

    I_{OL} = 0.4V (and 8 mA) on all other outputs and I/O pins.

3. I_{OL} = 24 mA on pins IRQ0, IRQ1, IRQ2, and IRQ3.

4. I_{OL} = 8 mA on all other outputs and I/O pins.

PARAMETER	MIN	TYP	MAX	UNIT
Storage temperature	-65	-	150	Degrees Centigrade
Voltage on any pin with respect to V_{SS}	-0.6	-	Vcc + 0.3 (except Vpp)	Volts
Voltage on V_{CC} with respect to V_{SS}	-	-	7.0	Volts

TABLE C-2. NON-OPERATIONAL SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Ambient temperature	0	25	70	Degrees Centigrade
Humidity	20	-	95	Percent
V_{CC} supply voltage with respect to V_{SS}	4.50	5.0	5.50	Volts
I_{CC} supply current (full loading)	-	-	100	Milliamps
Power dissipation	-	-	500	Milliwatts

TABLE C-3. OPERATIONAL SPECIFICATIONS

39

APPENDIX D - AC OPERATING CHARACTERISTICS

This appendix provides information on the WD83C593's ac operating characteristics. Table D-1 lists the ac operating characteristics. Figures D-1 and D-2 illustrate timing information.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_1	Status active low from ADDRESS, M/$\overline{\text{IO}}$, $\overline{\text{REFRESH}}$ valid	10	-	nsec
t_2	$\overline{\text{CMD}}$ active low from status active low	55	-	nsec
t_3	$\overline{\text{ADL}}$ active low from ADDRESS M/$\overline{\text{IO}}$, $\overline{\text{REFRESH}}$ valid	45	-	nsec
t_4	$\overline{\text{ADL}}$ active low to $\overline{\text{CMD}}$ active low	40	-	nsec
t_5	$\overline{\text{CDDS16}}$ active low from ADDRESS, M/$\overline{\text{IO}}$, $\overline{\text{REFRESH}}$ valid	-	55	nsec
t_6	$\overline{\text{CDSFDBK}}$ and CDCHRDY low from ADDRESS valid	-	60	nsec
t_7	$\overline{\text{CMD}}$ active low from ADDRESS valid	85	-	nsec
t_8	$\overline{\text{CMD}}$ pulse width	90	-	nsec
t_9	Write data setup to $\overline{\text{CMD}}$ active low	0	-	nsec
t_{10}	Write data hold time from $\overline{\text{CMD}}$ high (at the PS/2 bus)	30	-	nsec
t_{11}	Read data setup time to $\overline{\text{CMD}}$ high (at the PS/2 bus)	60	-	nsec
t_{12}	Read data hold time from $\overline{\text{CMD}}$ high (at the PS/2 bus)	5	-	nsec

TABLE D-1. AC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{13}	$\overline{CMD}$ high to $\overline{RAMOE}$ or $\overline{RAMWE}$ high	0	-	nsec
t_{14} WRITE CYCLE	$\overline{CMD}$ high to $\overline{DEN}$ high (during WRITE)	15	-	nsec
t_{14} READ CYCLE	$\overline{CMD}$ high to $\overline{DEN}$ high (during READ)	-	25	nsec
t_{15}	$\overline{CMD}$ high to DDIR low	0	-	nsec
t_{16}	DDIR low to pulse* (read cycles only)	0	-	nsec
t_{17}	BREQ active high to BACK active high	1 clk cyc time	-	
t_{18}	BREQ low to BACK low	1 clk cyc time	3 clk cyc time + 25 nsec	
t_{19}	$\overline{LANCS}$ active low to $\overline{IOR}$ or $\overline{IOW}$ active low	0	-	nsec
t_{20}	$\overline{ACK}$ active low from $\overline{IOR}$ or $\overline{IOW}$ active low	0	-	nsec
t_{21}	$\overline{ACK}$ high from $\overline{IOR}$ or $\overline{IOW}$ high	0	-	nsec
t_{22}	$\overline{CDSETUP}$ active low to $\overline{ADL}$ active low	15	-	nsec
t_{23}	$\overline{CDSETUP}$ hold from $\overline{ADL}$ high	25	-	nsec
t_{24}	CDCHRDY inactive low from $\overline{CDSETUP}$ active low	-	100	nsec
t_{25}	$\overline{CDSETUP}$ hold from $\overline{CMD}$ active low	30	-	nsec

TABLE D-1. AC OPERATING CHARACTERISTICS (Continued)

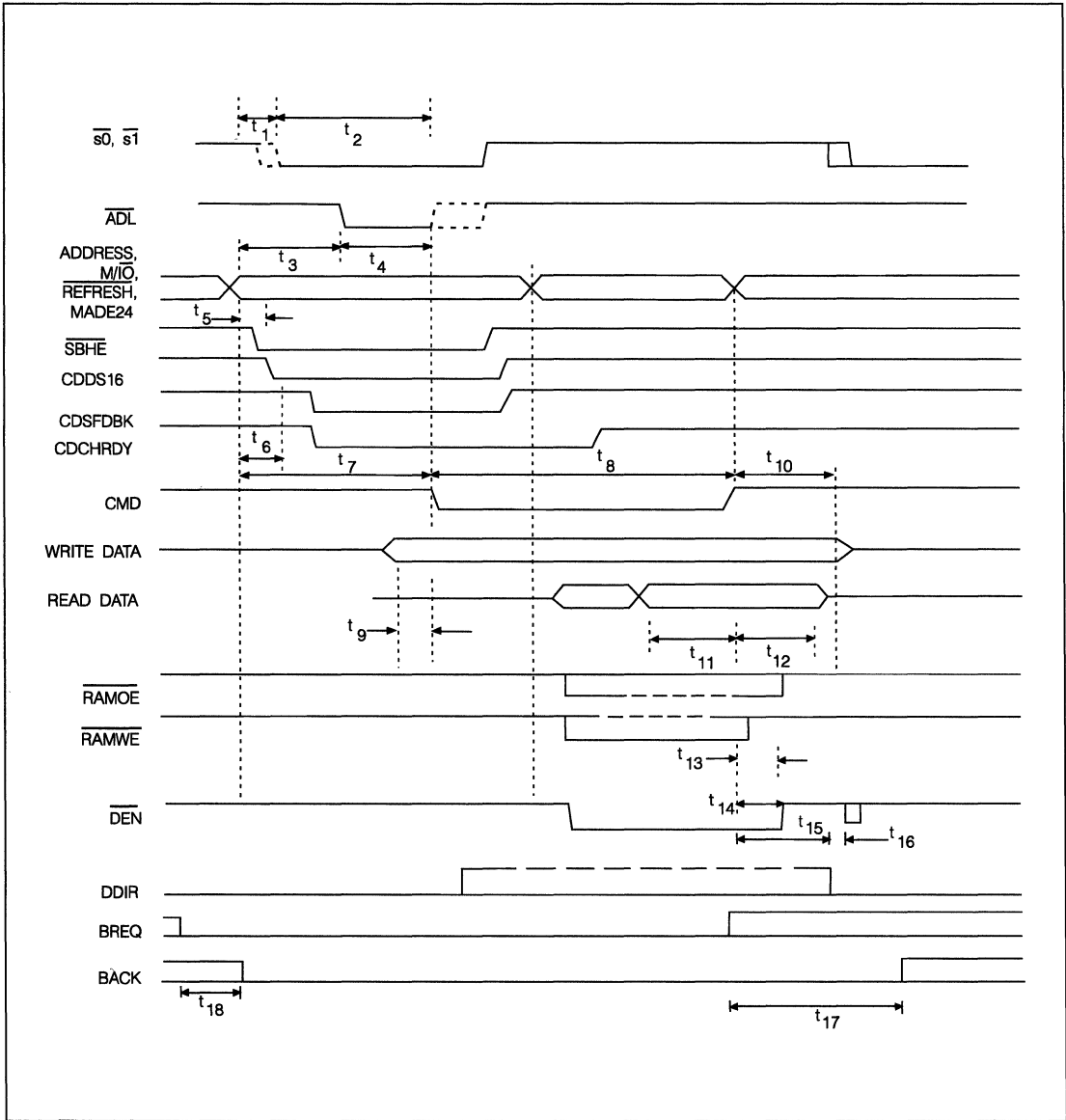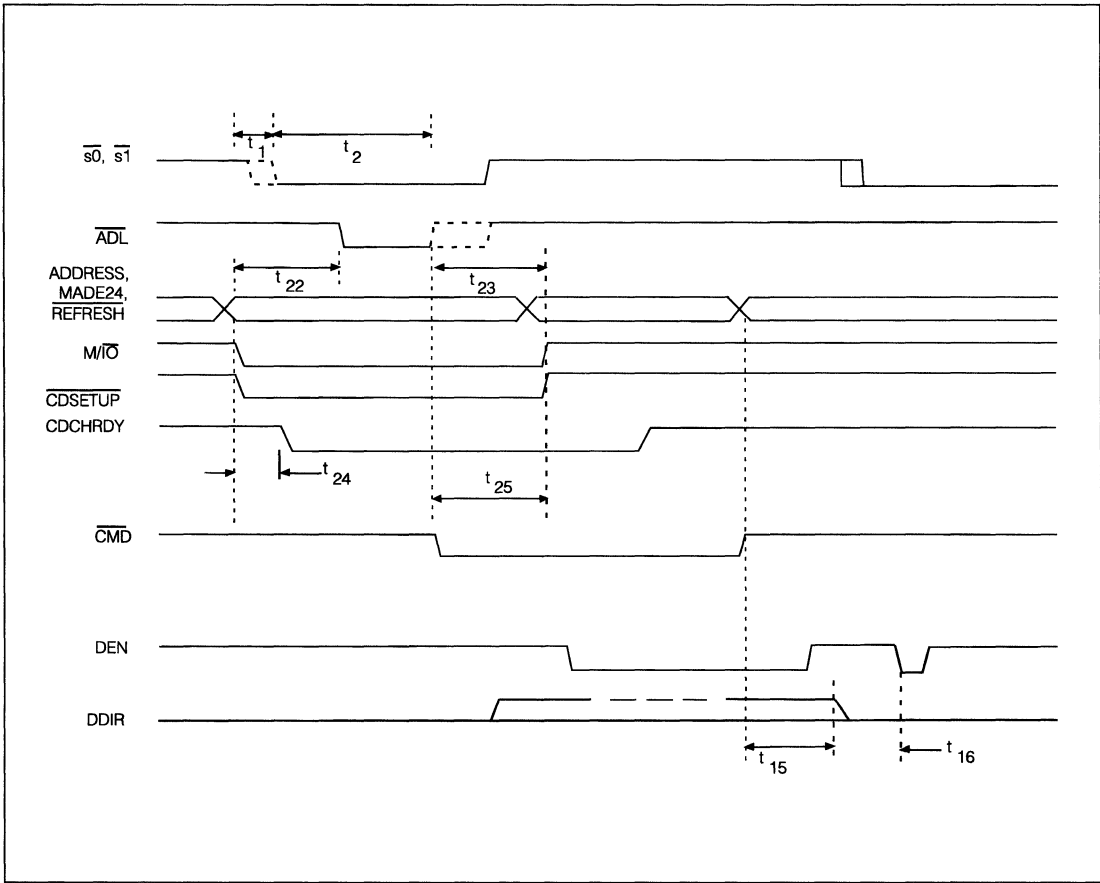*The pulse occurs on the DEN line, when the DDIR signal goes low during read cycles.

3 9

FIGURE D-1. HOST-MEMORY READ/WRITE TIMING

FIGURE D-2. SET-UP TIMING

3 9