WESTERN DIGITAL IMAGING

PERSONAL WORKSTATION

GRAPHICS ARRAY–1

(PWGA–1)

DATA BOOK

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General Information

INTRODUCTION

Product Summary

The Western Digital Imaging Personal Workstation Graphics Array-1 (PWGA-1) is a set of two proprietary VLSI chips designed to serve as the primary components of intelligent high-resolution color graphics add-in boards for the IBM PS/2 and PC-AT computer systems and compatibles. When the remaining board-level components and software are properly selected and integrated, the PWGA-1 will provide for complete emulation of the IBM Display Adapter 8514/A with superior performance plus functional enhancements (Western Digital extensions). Western Digital Imaging supplies register definitions, Adapter Interface (AI) software and BIOS extension firmware for the on-board EPROM in order to take full advantage of all features, including the unique extensions.

Feature Notes

- Full functional emulation of the IBM Display Adapter 8514/A, including 100% register-level compatibility.

- *Western Digital extension*: can be used with PC-AT bus as well as PS/2 Micro Channel with no loss of functionality.

- Performance is 30% to 100% faster than 8514/A in all graphic operations.

- BITBLT performance four times that of IBM 8514/A in Turbo 4-bit mode using either sixteen 64Kx4 VRAM chips or eight 256Kx4 VRAM chips; Turbo 4-bit mode is two times faster than regular 4-bit or 8-bit mode in BITBLT.

- *Western Digital extension*: Locked-in feature for a double set of video timing registers to ensure software compatibility when interfacing with different monitors.

- Pixel resolution supported:

  IBM 8514/A emulation: one screen page of 1024x768 pixels or two screen pages of 640x480 pixels, with 16/256 colors simultaneously displayable in both cases (1024x768x4/8 or 2@ 640x480x4/8).

  Western Digital extension: Enhanced resolution of one page of 1280x1024 pixels or two pages of 1024x768 pixels, also with 256 displayable colors in both cases (1280x1024x8 or 2@ 1024x768x8).

- *Western Digital extension*: High-speed hardware generation of textured lines and enhanced solid lines.

- *Western Digital extension*: Flicker-free video DAC programming option.

- All features, including most extensions, are supported by AI driver software and EPROM BIOS available from Western Digital.

- Supports both 64Kx4 and 256Kx4 video RAM (VRAM) in different speed grade; minimum configuration is four 256Kx4 chips or sixteen 64Kx4 chips. PWGA-1 can optimize performance by selecting different memory cycle timing for different speed grade VRAMs.

- Supports both INMOS and Brooktree video DACs and compatibles, with back-end integration to minimize external glue logic.

- Supports both interlaced and non-interlaced video monitors at up to 70Hz vertical refresh

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rate. Software written for 8514A interlaced monitors needs no modification for non-interlaced monitors.

■ Packaged as two 132-pin Plastic Quad Fine Pitch Packs (PQFPs), fabricated with 1.25 micron CMOS technology.

Options and Advantages

In addition to full emulation of the IBM 8514/A, which provides intelligent graphics functions such as polyline drawing, pattern fill for rectangles, "areas" (polygons), and "scissoring" (clipping), the PWGA-1 provides several functional enhancements and options as well as superior performance.

A major enhancement is the support of higher screen resolution, 1280x1024 pixels with 256 simultaneously displayable colors, as opposed to the 1024x768 maximum for the IBM 8514/A. Alternatively, the PWGA-1 can support a second screen page at the highest 8514/A resolution.

The PWGA-1 will give end users dramatic speed improvement in almost all graphics operations; in regular 4-bit mode, the PWGA-1 performs Bit Block Transfers (BITBLTs) twice as fast as the IBM 8514/A. In Turbo 4-bit mode, it is four times as fast. In particular, enhanced performance will be obvious when moving large images on the screen (e.g., scrolling). Under turbo mode all horizontal data movement will be twice as fast. This includes BITBLT, rectangle fill, horizontal line, and polygon search and fill.

Users will also notice considerable performance improvement with the PWGA-1 in all new line-drawing operations, because it directly performs several functions that the IBM 8514/A must perform in much slower CPU software. One such improvement is the direct generation of textured lines; another is the automatic, high-speed calculation of line parameters by the PWGA-1, replacing the tedious CPU software procedures with simple specifications of only the beginning and ending points of any line.

Whereas the IBM Display Adapter 8514/A is designed only for use in the PS/2 computer models that use the Micro Channel bus, the PWGA-1 provides an alternate interface to allow full 8514/A functionality (with extensions) for the Micro Channel, and more importantly, for all PC-AT computers and compatibles. The interface selection is made with a single device pin that is "strapped" at board design time.

Many graphics applications result in noticeable screen flickering, when the software steals refresh cycles to modify the color palette in the video DAC. A unique low-cost board design option will provide flicker-free display operation by allowing the PWGA-1 to buffer the new palette values and apply them during the monitor's horizontal retrace (flyback).

PWGA-1-based boards can accommodate both interlaced display monitors, such as the IBM 8514, and non-interlaced monitors; the PWGA-1 will drive either, automatically configuring itself at reset time based on the signals in the monitor interface cable (for IBM-compatible interlaced monitors) or on users' selection through AUTOEXEC.BAT utility. End users can thus exploit cost/performance trade-offs that are not available with the IBM 8514/A board.

Software written directly to 8514/A registers programs the video registers to IBM 8514/A display interlaced timing for 1024x768 resolution. To achieve maximum flexibility for driving different monitors, two sets of video registers are provided: one for 1024x768 resolution and one for 640x480 resolution. These registers can be preprogrammed by the BIOS EPROM at power up and their values locked in so that direct access by software later will not affect the preset video timing.

For the board designer, the PWGA-1 provides several further cost/function/performance trade-off opportunities, and also saves design time, board space, and component costs by integrating much of the peripheral logic into its design. The designer can choose among several video memory (VRAM) architectures, using either 64Kx4 or 256Kx4 VRAM chips, with back-end logic integrated into the PWGA-1 for 8514/A emulation and extension to two pages of 1024x768x8 (1280x1024 extended resolution requires off-chip logic support). The designer may also exploit the use of different clock rates for the drawing process and the screen refresh process; and bypass design of video data multiplexing and serializing, as these functions are integrated into the PWGA-1 chips.

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HOW TO USE THIS DOCUMENT

This data book is modularized for use in two ways. Chapters 1, 2, and 3 (General Information, Board Design Guide, Software Interface) plus the four appendices (specifications, including summary pin-out, and timing diagrams) contain the information required to use the PWGA–1 chip set in a board design and then use the resulting board in a computer system. In particular, Chapter 2 contains a detailed presentation of pin interfaces as well as guidelines for the selection and configuration of other necessary board-level components.

Note that much of the material in these three chapters is presented in a quasi-tutorial style, for the benefit of readers who may not be expert in advanced graphics hardware.

The following IBM publication may be useful for the board designer: *IBM Personal System/2 Display Adapter 8514/A Technical Reference*, publication no. 68X2248/S68X-2248-0, April 1987.

BOARD OPERATION OVERVIEW

The functions of any PWGA–1-based board, as well as those of the IBM 8514/A, can be summarized as follows:

A. *Screen refresh*: A key function is driving the display monitor. The board reads data from its VRAM-stored representation of the screen image, and then converts the data, pixel by pixel, into RGB signals for the display monitor, in synchronization with the sweeping of the monitor's RGB guns across its screen.

B. *Drawing*: The other major board function, less time-critical than screen refresh, is the generation of new lines and areas within VRAM in response to commands from the system CPU. In this context, "drawing" includes filling polygonal shapes with patterns, establishing boundaries for "scissor-

ing" (clipping), and similar operations. Drawing operations can involve complex algorithms, and they require correspondingly sophisticated processing by the PWGA–1.

C. *Image transfer*: In most graphics work, it is common to save board-drawn images (e.g., pop-up menu) elsewhere in main system memory and/or on disk for later restoration to on-board video memory and thence to the display screen.

D. *VGA input*: The host CPU may request that the monitor be driven by the VGA (Video Graphics Array), a similar but less sophisticated graphics facility located elsewhere in the system; in this case the PWGA–1-based board (or the 8514/A) essentially becomes a passive pass-through channel, taking video data and sync signals from the "auxiliary video extension" bus connector. Note that another monitor can be attached directly to the VGA; if the PWGA–1-based board (or 8514/A) is not in pass-through mode, then the two monitors can simultaneously display different images.

E. *Palette loading*: Pixel color interpretation is mediated by a small "palette" memory in the video DAC on the board. The CPU can very rapidly effect changes on the screen by changing the contents of this memory, as distinct from issuing drawing commands. The palette is further discussed in the next section.

F. *EPROM access*: The board includes a small EPROM containing a BIOS extension available to the CPU. The EPROM is mainly for initialization and diagnostic testing during power up. (Note that a portion of EPROM contains certain board configuration information read by the PWGA–1 upon power up.)

G. *Other*: Finally, the board design must provide for customary CPU handshaking, interrupts, and miscellaneous bus interface signals.

ARCHITECTURE

External Architecture

Figure 1-1 illustrates the logical architecture of a PWGA-1-based board in block-diagram style. Each of its major elements, which for now are presented as functional "black boxes," is discussed below.

The *PWGA-1* (Western Digital Personal Workstation Graphics Array-1) consists of two 132-pin chips: the *PAM* (Pixel Address Manager) and the *PDM* (Pixel Data Manager). The next sections provide a brief explanation of the internal components of the PAM and PDM; their detailed architecture and operation are discussed in the proprietary portion of this document, in Chapters 4 and 5, respectively.

The *VRAM* block in Figure 1-1 represents the video memory subsystem, used to store screen images generated in the PWGA-1 (as a result of CPU drawing instructions) or sent from the CPU (typically for the purpose of restoring previously drawn images that had been stored elsewhere in the system). The PWGA-1 then accesses these images for automatic display-screen refresh. Drawing operations take place within a pixel coordinate space of 2K by 2K; similar to the 8514/A, remaining VRAM storage is available to the PWGA-1 and the CPU for "off-screen" use, including storage of fill patterns and scratchpad data. Chapter 2 describes VRAM operation, presents a selection of configuration choices, and defines the detailed interface of the VRAM subsystem to the PWGA-1 chip set.

In the standard board configuration, the PWGA-1 is responsible for serializing and multiplexing data extracted from VRAM for screen refresh, and then forwarding the data to the DAC via the video interface logic block. In VRAM architectures using external back-end support, which is necessary to achieve 1280x1024 pixel resolution, serializing and multiplexing is done within the VRAM block, and the resultant screen refresh data bypasses the PWGA-1, as shown in Figure 1-1.

The *video DAC* (Digital-to-Analog Converter) has the primary function of generating analog intensity signals for the red, blue, and green guns of the display monitor, varying these values in synchronization with pixel coordinates as the guns sweep across the screen. The source of these val-

ues is the "pixel data" that the PWGA-1 reads out of VRAM in its screen refresh operation. With external back-end support, extra intelligence is required in the DAC to assist in the data formatting begun in the serializing and multiplexing logic within the VRAM block.

The DAC contains the *color palette*, a small memory that maps a given pixel data value into a specific combination of RGB intensities, according to the contents of each of the cells in palette memory. For example, in a 256-color arrangement, an eight-bit pixel data value selects one of 256 palette memory cells. Each of the latter have been loaded with an 18-bit datum partitioned into three 6-bit fields whose values are in turn converted into red, blue, and green signal intensities when that cell is selected. Palette values may be loaded directly from the CPU, or, with the Western Digital flicker-free option, indirectly through the PWGA-1.

The video DAC and its interfaces, the auxiliary video extension (used to drive the monitor from an off-board source, normally the system VGA), the monitor interface, and other related logic and interfaces together comprise the "video DAC and interface subsystem," described in detail in Chapter 2. Note that the small block in Figure 1-1 labelled "Video Interface Logic" represents only a modest amount of logic and, in fact, consists largely of pass-through routing of signals; the block is drawn chiefly for convenience in explanation.

The *CPU Interface Logic* block contains the bus transceivers and TTL glue logic necessary to interface the PWGA-1 chips to the system bus (either the IBM PS/2 Micro Channel or the IBM PC-AT bus, or compatible buses). This block also provides a data path to the DAC, used by the CPU to directly access palette values, and to the EPROM. The CPU interface logic is described in detail in Chapter 2.

The remaining board elements are the EPROM (containing Western Digital-supplied BIOS extension firmware), the clock generators, and a grouping of minor components (pull-up/down logic and DIP switches) used by the PWGA-1 to sense its environmental configuration: whether Micro Channel or AT bus, VRAM organization, etc. These elements are described in Chapter 2, together with the inter-chip (PAM-PDM) connections.

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Finally, the PWGA-1 contains a set of user-accessible internal registers that are compatible with those on the IBM 8514/A board, plus certain extra registers to support Western Digital extensions. From the user's point of view, the registers exist chiefly as destinations for software commands ("orders," in IBM terminology) and their parameters. User programming considerations required to exploit the Western Digital extensions are discussed in Chapter 3.

PWGA-1 Functional Organization

Figure 1-2 introduces the internal functional blocks of the PAM and PDM chips. Communication between the two chips is mediated by two Internal Bus Interface Units (IBIUs); they are transparent to user operations, and are not shown in the diagram.

In addition to the internal registers and the IBIUs, the functional modules within the PWGA-1 are as follows:

Within the PAM:
CIU: CPU Interface Unit
GP: Graphics Processor
MIC: Memory Interface Controller

Within the PDM:
DP: Data Processor
DSP: Display Processor

The CIU controls communication with the system bus (via the CPU interface logic block external to the chip set), and passes data to and from all the other units on the chip set. It also performs certain miscellaneous functions, such as forwarding addresses from the system bus to the EPROM.

The GP performs the actual drawing computations; it supports all 8514/A graphics modes, plus Western Digital extensions. The modes include line drawing, fill area outline drawing (arbitrary polygons), rectangle drawing, image transfer from the CPU, BITBLT copying (Bit Block Transfer within VRAM), and scissoring. The GP receives its drawing instructions from the CIU and sends the resulting pixel coordinates to the MIC.

The MIC controls VRAM addressing and access. In a typical drawing operation, it will convert the GP-supplied pixel coordinates into VRAM addresses, cause the VRAM to send the addressed data (pixel color values) to the DP for modification, and then rewrite back into VRAM. When not involved in a drawing or special-purpose access, the MIC manages the VRAM addressing portion of the constantly on-going screen refresh process. The MIC gives screen refresh the highest priority for VRAM access; next is timer-based VRAM chip refresh, with GP-requested drawing access given the lowest priority.

The DP is responsible for updating VRAM in support of drawing and data transfer operations and altering pixel data (color values) according to masks and parameters, including "mix" specifications supplied in shared internal registers by the DP and GP. The DP receives pixel data on a bidirectional bus from VRAM, modifies it, and then writes it back on the same bus.

The DSP manages the DAC and monitor, coordinating its role in the screen refresh process with the MIC. With an integrated back-end support VRAM design, the DSP serializes and multiplexes pixel data, "pumped" out of VRAM by the MIC, to the DAC, in synchronization with the timing of the monitor's sweep across the display screen. (With external back-end support, this DSP function is assumed by extra logic within the VRAM block and the DAC.)

Test Considerations

To facilitate board testing, all output pins of both PAM and PDM can be disabled during Reset through the test strap pin (Bit 6 of IAD bus).

If the test strap pin is low, all output signals except SLD are tri-stated. SLD is tri-stated if TSEL2–TSEL0 are also high.

For PC board in-circuit test, the test strap pin should be low and TSEL2–TSEL0 should be high. All bi-directional pins are forced to be input. All input and bi-directional pads have internal pull-up resistors, therefore they are high if not actively driven low.

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Figure 1-1. Board Architecture

Note: This diagram is intended to illustrate the logical connections of board-level elements, not physical board layout.

(Dotted lines represent paths used with external back-end support only.)

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General Information

To Configuration
Strapping

Pixel Address Manager Chip (PAM)

To CPU Interface
Logic and EPROM

CIU

GP

MIC

To VRAM
(Address and Control)

Inter-chip
Boundary

DSP

DP

To VRAM Parallel Data
Port (for drawing)

To VRAM Parallel Data
Port (for screen refresh)

This path is *not*
used with external
back-end support.

Pixel Data Manager Chip (PDM)

To Video Interface
Logic (control and
pixel color selection)

Not Illustrated:

A) Internal Registers (continued within
    both chips)

B) Internal Bus Interface Units (for inter-
    chip communication)

C) Clock Inputs (used by all modules)

D) Power and Ground Connections

Figure 1-2. PWGA-1 Internal Modules

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CPU INTERFACE

The PAM provides interface pins to connect to either the IBM PS/2 Micro Channel or the AT bus via a small amount of external logic, illustrated in Figures 2-1 and 2-2. The CIU configures itself for one of the two different interfaces according to the value of a configuration strapping pin, described later in this chapter (Table 2-10).

Because of the two possible external environments, most of these CPU interface pins have two alternate interpretations, as shown in the following tables. In both cases, however, the names and uses of most of these pins correspond precisely to the IBM specifications for the Micro Channel or AT bus, and so do not need special explanation.

Table 2-1. CPU Interface Pins (PAM) for Micro Channel Interface (see Figure 2-1)

Name	PAM Pin #	I/O	Description
A0–A19	62–69, 71–82	I	CPU address Bits 0 through 19
AUP	85	I	Decoding of upper CPU address Bits 23–20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the PWGA-1-based board
M/-IO	57	I	Distinguishes memory access from I/O access
-S0	59	I	-Status Bit 0
-S1	58	I	-Status Bit 1
-ADL	61	I	-Address Latch
-CMD	60	I	-Command
-SBHE	56	I	-System Byte High Enable
RESET	52	I	Channel Reset
-CDSETUP	86	I	-Card Setup
CD CHRDY	90	O	Channel Ready
-IRQ	88	O	-Interrupt Request; tied to Micro Channel -IRQ 9
-CD SFDBK	89	O	-Card Selected Feedback
-CD DS16	55	O	-Card Data Size 16
-DBEN	91	O	-Data Bus Enable
D0–D15	94–98, 100–110	I/O	CPU Data Bits 0 through 16
DBDIR	92	O	Data Bus Direction (high for CPU read, low for CPU write)

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Table 2-2. CPU Interface Pins (PAM) for AT Bus Interface (see Figure 2-2)

Name	PAM Pin #	I/O	Description
SA0–SA19	62–69, 71–82	I	CPU address Bits 0 through 19
AUP	85	I	Decoding of upper CPU address Bits 23–20; all these should be 0 if the lower 20 bits of address are to be considered valid for the PWGA-1-based board
–SBHE	56	I	–System Bus High Enable
–MEMR	57	I	–Memory Read
–MEMW	59	I	–Memory Write
–IOR	58	I	–I/O Read
–IOW	60	I	–I/O Write
BALE	61	I	Buffered Address Latch Enable
AEN	86	I	Address Enable
RESET	52	I	System Reset
I/O CHRDY	90	O	I/O Channel Ready
IRQ	88	O	Interrupt Request; tied to any AT bus interrupt line
–I/O CS16	55	O	–I/O 16-bit Chip Select
–DBEN	91	O	–Data Bus Enable
SD0–SD15	94–98, 100–110	I/O	CPU Data Bits 0 through 16
DBDIR	92	O	Data Bus Direction (high for CPU read, low for CPU write)
ATCLK	84	I	AT Bus Clock

VRAM DESIGN AND INTERFACE

The PWGA-1 supports four VRAM designs. Each of these in turn can be implemented with two or three levels of chip population, for a total of ten implementations. The design choice depends on the desired combination of the following criteria (with only certain combinations possible):

- pixel resolution: 640x480, 1024x768, or 1280x1024

- pixel depth: 4 or 8 bits per pixel

- number of screen pages: one or two

- size of VRAM chips to be used: 64Kx4 or 256Kx4

- number of VRAM chips (and hence board size)

- field upgradeability

- type of design: with back-end support (serializing and multiplexing of pixel data for screen refresh) integrated within the PWGA-1, or with external back-end support

External back-end support—which includes use of a more sophisticated DAC—is required to achieve 1280x1024 resolution.

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Figure 2-1. CPU Interface Logic: Micro Channel

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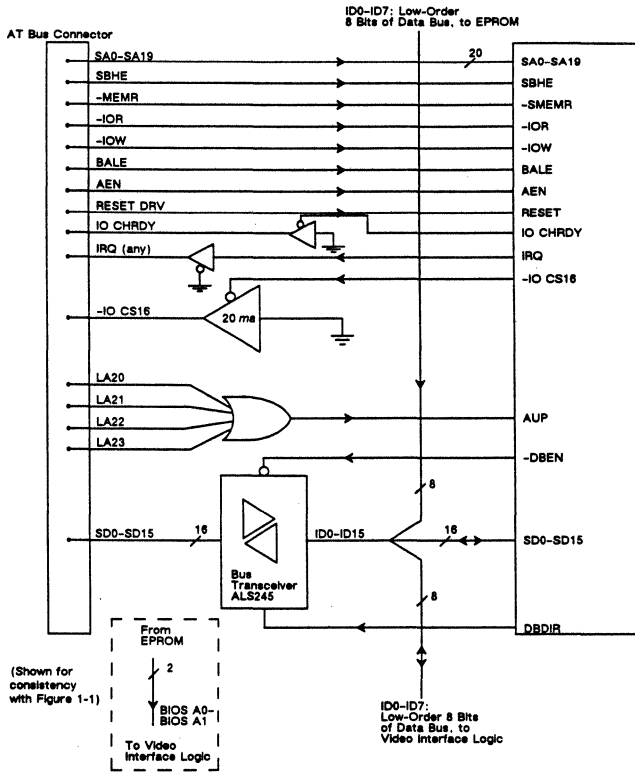
Figure 2-2. CPU Interface Logic: AT Bus

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Table 2-3. VRAM Parameters

I/E*	Chip Size	No. of Chips	Pixel Resolution	Pixel Depth	# of Screen Pages	S/W**
I	64Kx4	16	1024x768	4	1	S
			640x480	4	2	S
		32	1024x768	8	1	S
			1024x768	4	2	W
			640x480	8	1	S
I	256Kx4	4	1024x768	4	1	S
			640x480	4	2	S
		8	1024x768	8	1	S
			1024x768	4	2	W
			640x480	8	1	S
		16	1024x768	8	2	W
			1024x768	4	2	W
			640x480	8	2	W
E	256Kx4	8	1280x1024	4	1	W
			1024x768	8	1	S
			1024x768	4	2	W
			640x480	8	1	S
		16	1280x1024	8	1	W
			1024x768	8	2	W
			1024x768	4	2	W
			640x480	8	2	W

*I = Integrated (on PWGA-1 chips) back-end support
 E = External back-end support

**S = Standard capability within 8514/A emulation
 W = Western Digital extension to 8514/A capability

The capabilities of the various VRAM designs, with their several levels of chip population, are shown in Table 2-3. Note: Although not shown, each level of chip loading for a given design includes the capabilities of the smaller chip population(s).

Since the 16-chip implementation of 64Kx4 of this design cannot support maximum IBM 8514/A resolution, the 32-chip version, shown in Figure 2-3, will typically form the basis for board design except for special applications. Figure 2-3 does, however, illustrate which chip positions should be left unpopulated if a 16-chip field-upgradeable version is to be produced.

If maximum IBM 8514/A resolution is desired, this design should be implemented to at least the 8-chip 256Kx4 level; implementation at the 16-chip level provides for the extended capability of doubling the number of screen pages supported by the 8-chip version. Figure 2-4 illustrates the 16-chip version with indications of which chips should be left unpopulated if field upgradeable 4-chip and/ or 16-chip versions are to be produced. The same diagram can also serve as the basis for an 8-chip design, with half of those chips omitted for future field upgrade if desired.

Figure 2-5 illustrates the 16-chip version with 256Kx4 VRAMS and external backend support. A Brooktree 8-bit video DAC BT458 is used. Figure 2-6 shows the detail connections for 256Kx4 VRAMs to PAM and PDM.

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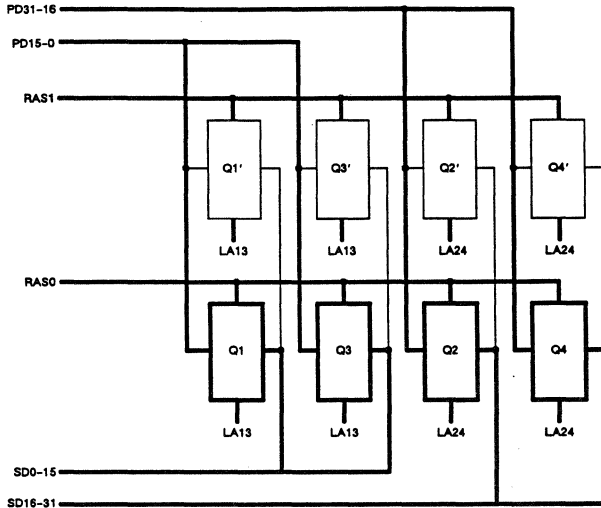
- Heavy lines represent minimum chip population (16 chips).
- Heavy lines plus light lines represent standard chip population (32 chips).

Control Signal Assignments

Quad (4 chips)	SE	SC	RAS	CAS	WE	Display Memory Configuration
Q1	SE12A	SC13	RAS0	CAS12	WE0-3	
Q2	SE12A	SC24	RAS0	CAS12	WE4-7	1024x1024x4
Q3	SE34A	SC13	RAS0	CAS34	WE0-3	
Q4	SE34A	SC24	RAS0	CAS34	WE4-7	
Q1'	SE12B	SC13	RAS1	CAS12	WE0-3	
Q2'	SE12B	SC24	RAS1	CAS12	WE4-7	1024x1024x8
Q3'	SE34B	SC13	RAS1	CAS34	WE0-3	2048x1024x4
Q4'	SE34B	SC24	RAS1	CAS34	WE4-7	

Figure 2-3. VRAM Design with 64Kx4 Chips and Integrated Back-End Support

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PD31-16

PD15-0

RAS1

```
        ┌─ ─ ─┐     ┌─ ─ ─┐
        │     │     │     │
        │  Q3 ├─┐   │  Q4 │
        │     │ │   │     │
        └─ ─ ─┘ │   └─ ─ ─┘
          LA13  │     LA24
```

RAS0
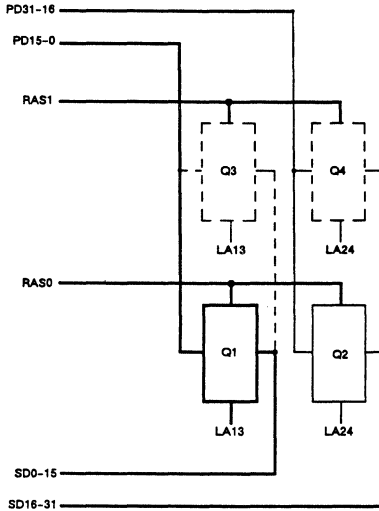
Note: In 4-chip population, the high 16 bits of both data buses are unused. The unused pins will be pulled high by the internal pull-up resistors.

```
        ┌─────┐     ┌─────┐
        │     │     │     │
        │  Q1 │     │  Q2 │
        │     │     │     │
        └─────┘     └─────┘
          LA13        LA24
```

SD0-15

SD16-31

- Heavy lines represent minimum chip population (4 chips).
- Heavy lines plus light lines represent standard chip population (8 chips).
- Heavy lines plus light lines plus dotted lines represent extended chip population (16 chips).

Control Signal Assignments

Quad (4 chips)	SE	SC	RAS	CAS	WE	Display Memory Configuration
Q1	SE12A	SC13	RAS0	CAS12	WE0-3	1024x1024x4
Q2	SE12A	SC24	RAS0	CAS12	WE4-7	1024x1024x8 / 2048x1024x4
Q3	SE34A	SC13	RAS1	CAS34	WE0-3	2048x1024x8
Q4	SE34A	SC24	RAS1	CAS34	WE4-7	2048x2048x4

Figure 2-4. VRAM Design with 256Kx4 Chips and Integrated Back-End Support

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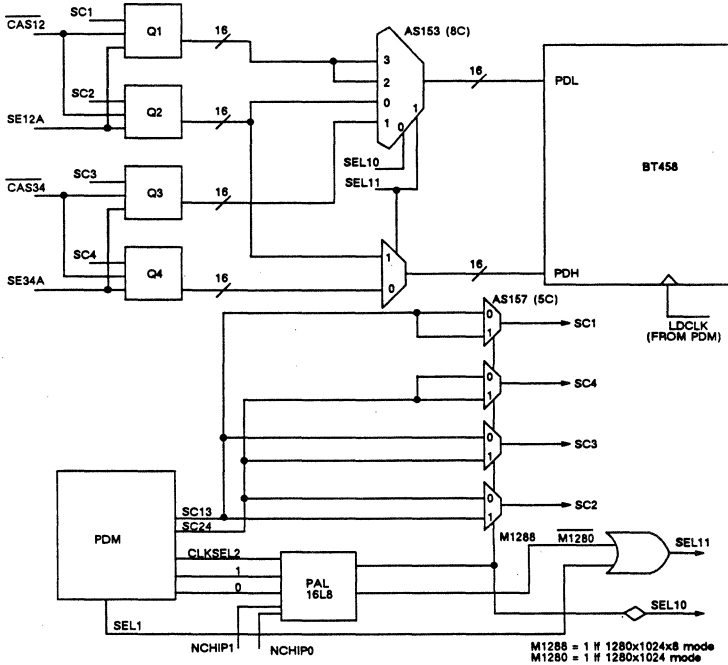
Control Signal Assignments

QUAD	SE	SC	RAS	CAS	WE
Q1	SE12A	SC1	RAS0	CAS12	WE0-3
Q2	SE12A	SC2	RAS0	CAS12	WE4-7
Q3	SE34A	SC3	RAS1	CAS34	WE0-3
Q4	SE34A	SC4	RAS1	CAS34	WE4-7

Figure 2-5. VRAM Design with 256Kx4 Chips and External Back-End Support

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Q3

PAM
CHIP

Q1

2-9

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

2-10
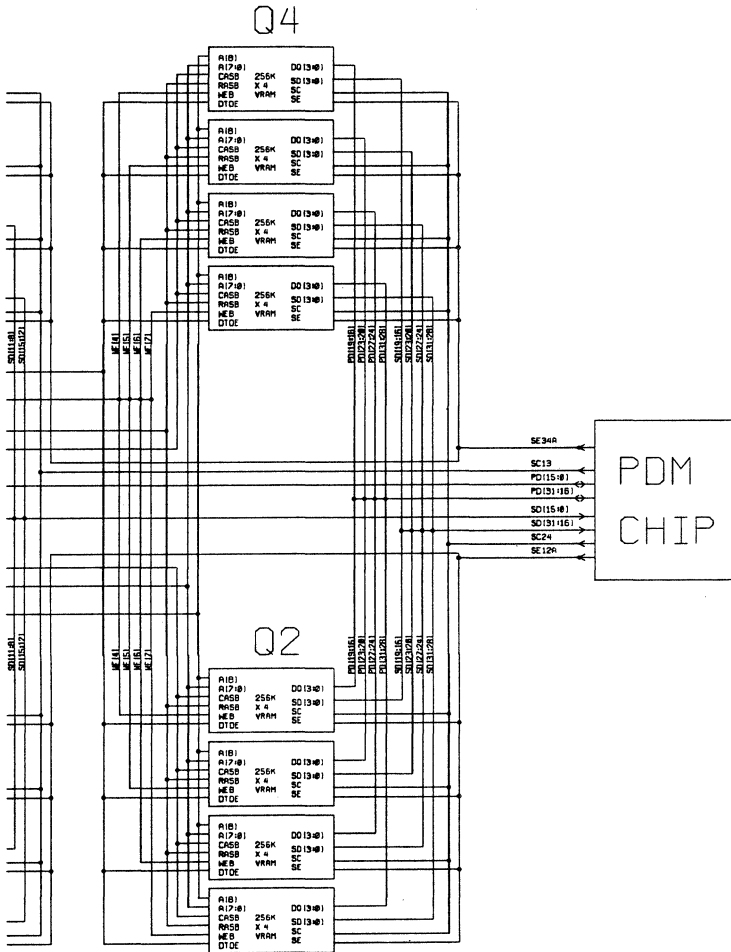
Table 2-4. PAM Pin Interface to VRAM

Pin Name	PAM Pin #	Description
MA7–MA0	19, 16–10	Low-order address lines, into all quads. For 64Kx4 designs, MA7 is not used; for 256Kx4 chips, all eight lines are used.
LA13	34	Used as high-order address bit (MA8) for quads Q1, Q3, and their "'" counterparts, in all designs.
LA24	35	Used as high-order address bit (MA8) for quads Q2, Q4, and their "'" counterparts, in all designs.
–RAS0	22	Row Address Strobe 0
–RAS1	23	Row Address Strobe 1
–CAS12	20	Column Address Strobe 1
–CAS34	21	Column Address Strobe 2
WE7–WE0	31–24	Pixel data Write Enable lines to enable writing into VRAM on the PD bus (bidirectional Parallel Data bus, between VRAM and DP; see below). A given quad receives either WE0–3 or WE4–7.
–DT/–OE	32	Transfer-cycle control and serial data output enable, used by all quads.

Certain interfacing information is common to all VRAM designs. For example, all designs use the concept of "quadding" the VRAM chips into groups of four, with each of the four chips in a "quad" receiving the same control signals. (The write enable lines are an exception; the signal assignment tables show a given quad receiving WE0–3 or WE4–7, but the four lines are distributed individually to each of the four chips within the quad.) The diagrams (Figures 2–3 to 2–5) label quads as Q1, Q2, Q3, and Q4 for minimum chip population, with a "'" symbol added for the second population level.

Tables 2-4 and 2-5 show the PAM and PDM pins used to form the VRAM interface. The four VRAM design diagrams (Figures 2–7a, b, c, d) that follow include tables that specify which quads receive which control signals. Not all signals are used in a given VRAM design and chip population.

All the pins in Table 2-4 drive control signals generated by the MIC.

The PD Pixel Data bus is managed by the Data Processor module (DP); all other pins in Table 2-5 are managed by the Display Processor (DSP).

WE0–3 are for pixel positions 0–3, respectively. In turbo mode, WE4–7 are for positions 4–7. For x8 mode, WE4–7 are the same as WE0–3.

2-11

93-000032-00

Table 2-5. PDM Pin Interface to VRAM

Pin Name	PDM Pin #	Description
PD31–PD0	90–93, 95–98, 100–114, 117–125	Parallel Data bus, connecting the DP module to the VRAM block; data is bidirectional. (This is the path through which the DP first reads, then rewrites pixels in support of drawing operations.)
SD31–SD0	46–49, 52–67, 71–82	Serial Data bus; in VRAM designs with integrated back-end support, this is the path by which screen refresh data is extracted (by a transfer cycle) from the serial ports of the VRAM chips and then moved to the DSP module for serializing and multiplexing before being sent to the DAC. In VRAM designs with external back-end support, the serial data bus to the DSP is not used; instead, the DSP reconfigures itself to use some of these pins (replacing SD5,SD6) as output drivers for additional control signals to VRAM, as shown below.
SE12A, SE34A SE12B, SE34B	87, 85, 86, 84	Serial data output enable
SC13	88	Serial data clock 1
SC24	89	Serial data clock 2

The following pins are changed for external back-end support:

SEL1 (SD5)	77	Mux select 1 (External back-end support. See Fig 2-5)
LDCLK (SD6)	76	(With external back-end support, this pin is reconfigured from SD6 to the LDCLK signal to the DAC, as discussed in the next section. See Fig 2-5)

In the following VRAM design diagrams, the PD lines connect to the parallel data ports of the VRAM chips, while the SD lines connect to their serial data ports.

The different resolution modes require different memory addressing schemes to configure the display memory properly for screen pixel position. Figures 2-7a, 2-7b, 2-7c and 2-7d show how the PAM generated addresses connect to the row and column addresses of the 256Kx4 VRAMS (see Figure 2-6). X2 to X9 indicates the horizontal position of each "4 pixel" group from left to right on the screen. X0 and X1 are not shown because of the "4 pixel" group organization. Y0 to Y9 indicates the vertical position of each pixel from top to bottom on the screen. Each figure also has a small map for the top left-hand corner of the screen showing the X,Y position and the row-column address of the VRAM.

2-12

Memory Config :   1024x768x4   Four 256Kx4 Chips

PAM Memory Address Line	VRAM Row Address	Column Address	Comments
LA13	Y9	Y0	A8 for Q1 chips
LA24	D.C.	D.C.	Unused Pin
MA7	Y8	X9	
MA6	Y7	X8	
MA5	Y6	X7	
MA4	Y5	X6	
MA3	Y4	X5	
MA2	Y3	X4	
MA1	Y2	X3	
MA0	Y1	X2	

RAS Decoding : RAS0 and RAS1 active regardless of address

CAS Decoding : CAS12 active, CAS34 inactive regardless of address

WE Decoding : Pixel Write Mask not nibble swapped

Display Memory Map :

```
            X4 | 0000 | 0000 | 0000 | 0000 |
            X3 | 0000 | 0000 | 1111 | 1111 |
            X2 | 0000 | 1111 | 0000 | 1111 |
   Y Y Y   X1 | 0011 | 0011 | 0011 | 0011 |
   2 1 0   X0 | 0101 | 0101 | 0101 | 0101 |
   ---------+------+------+------+------+
   0 0 0    |  Q1  |  Q1  |  Q1  |  Q1  |
            | 0, 0*| 0, 1 | 0, 2 | 0, 3 |
   ---------+------+------+------+------+
   0 0 1    |  Q1  |  Q1  |  Q1  |  Q1  |
            |0,100 |0,101 |0,102 |0,103 |
   ---------+------+------+------+------+
   0 1 0    |  Q1  |  Q1  |  Q1  |  Q1  |
            | 1, 0 | 1, 1 | 1, 2 | 1, 3 |
   ---------+------+------+------+------+
   0 1 1    |  Q1  |  Q1  |  Q1  |  Q1  |
            |1,100 |1,101 |1,102 |1,103 |
   ---------+------+------+------+------+
```

*Row Address, Column Address respectively in HEX

Figure 2-7a. Display Memory Addressing for 1024x768x4

2-13

DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT OF	

93-000032-00

Memory Config :   640x480x4(x 2 page)   Four 256Kx4 Chips

PAM Memory Address Line	VRAM Row Address	Column Address	Comments
LA13	Y9	X9	A8 for Q1 chips
LA24	D.C.	D.C.	Unused Pin
MA7	Y8	X8	
MA6	Y7	X7	
MA5	Y6	X6	
MA4	Y5	X5	
MA3	Y4	X4	
MA2	Y3	X3	
MA1	Y2	X2	
MA0	Y0	Y1	

RAS Decoding : RAS0 and RAS1 active regardless of address

CAS Decoding : CAS12 active, CAS34 inactive regardless of address

WE Decoding : Pixel Write Mask not nibble swapped

Display Memory Map :

```
            X4 | 0000 | 0000 | 0000 | 0000 |
            X3 | 0000 | 0000 | 1111 | 1111 |
            X2 | 0000 | 1111 | 0000 | 1111 |
    Y Y Y   X1 | 0011 | 0011 | 0011 | 0011 |
    2 1 0   X0 | 0101 | 0101 | 0101 | 0101 |
    ---------+------+------+------+------+
    0 0 0    |  Q1  |  Q1  |  Q1  |  Q1  |
             | 0, 0*| 0, 2 | 0, 4 | 0, 6 |
    ---------+------+------+------+------+
    0 0 1    |  Q1  |  Q1  |  Q1  |  Q1  |
             | 1, 0 | 1, 2 | 1, 4 | 1, 6 |
    ---------+------+------+------+------+
    0 1 0    |  Q1  |  Q1  |  Q1  |  Q1  |
             | 0, 1 | 0, 3 | 0, 5 | 0, 7 |
    ---------+------+------+------+------+
    0 1 1    |  Q1  |  Q1  |  Q1  |  Q1  |
             | 1, 1 | 1, 3 | 1, 5 | 1, 7 |
    ---------+------+------+------+------+
```

*Row Address, Column Address respectively in HEX

Figure 2-7b. Display Memory Addressing for 640x480x4 (2 page)

2-14

	WESTERN DIGITAL CORPORATION	
DWG SIZE **A**	DRAWING NUMBER	REV.
SCALE	SHT OF	

93-000032-00

Memory Config :   1024x768x8   Eight 256Kx4 Chips

PAM Memory Address Line	VRAM Row Address	Column Address	Comments
LA13	Y9	Y0	A8 for Q1 chips
LA24	Y9	Y0	A8 for Q2 chips
MA7	Y8	X9	
MA6	Y7	X8	
MA5	Y6	X7	
MA4	Y5	X6	
MA3	Y4	X5	
MA2	Y3	X4	
MA1	Y2	X3	
MA0	Y1	X2	

RAS Decoding : RAS0 and RAS1 active regardless of address

CAS Decoding : CAS12 active, CAS34 inactive regardless of address

WE Decoding : Upper nibble of write mask is generated by replicating lower nibble.

Display Memory Map :

```
              X4 | 0000 | 0000 | 0000 | 0000 |
              X3 | 0000 | 0000 | 1111 | 1111 |
              X2 | 0000 | 1111 | 0000 | 1111 |
        Y Y Y X1 | 0011 | 0011 | 0011 | 0011 |
        2 1 0 X0 | 0101 | 0101 | 0101 | 0101 |
        ---------+------+------+------+------+
        0 0 0    |Q1&Q2 |Q1&Q2 |Q1&Q2 |Q1&Q2 |
                 | 0, 0*| 0, 1 | 0, 2 | 0, 3 |
        ---------+------+------+------+------+
        0 0 1    |Q1&Q2 |Q1&Q2 |Q1&Q2 |Q1&Q2 |
                 |0,100 |0,101 |0,102 |0,103 |
        ---------+------+------+------+------+
        0 1 0    |Q1&Q2 |Q1&Q2 |Q1&Q2 |Q1&Q2 |
                 | 1, 0 | 1, 1 | 1, 2 | 1, 3 |
        ---------+------+------+------+------+
        0 1 1    |Q1&Q2 |Q1&Q2 |Q1&Q2 |Q1&Q2 |
                 |1,100 |1,101 |1,102 |1,103 |
        ---------+------+------+------+------+
```

*Row Address, Column Address respectively in HEX

Figure 2-7c. Display Memory Addressing for 1024x768x8

2-15

93-000032-00

Memory Config :   1024x768x4x2 Turbo Mode   Eight 256Kx4 Chips

PAM Memory Address Line	VRAM Row Address	Column Address	Comments
LA13	Y9	X2 V. Access, Y0 H. Access	A8 for Q1 chips
LA24	Y9	X2 V. Access, -Y0 H. Access	A8 for Q2 chips
MA7	Y8	X10	
MA6	Y7	X9	
MA5	Y6	X8	
MA4	Y5	X7	
MA3	Y4	X6	
MA2	Y3	X5	
MA1	Y2	X4	
MA0	Y1	X3	

RAS Decoding : RAS0 and RAS1 active regardless of address

CAS Decoding : CAS12 active, CAS34 inactive regardless of address

WE Decoding : Pixel Write Mask will be nibble swapped if LA13=1.

Page Zero Display Memory Map (X10 = 0) :

```
            X4 | 0000 | 0000 | 0000 | 0000 |
            X3 | 0000 | 0000 | 1111 | 1111 |
            X2 | 0000 | 1111 | 0000 | 1111 |
    Y Y Y   X1 | 0011 | 0011 | 0011 | 0011 |
    2 1 0   X0 | 0101 | 0101 | 0101 | 0101 |
   ---------------+------+------+------+------+
    0 0 0      | Q1   | Q2   | Q1   | Q2   |
               | 0, 0*|0,100 | 0, 1 |0, 101|
   ---------------+------+------+------+------+
    0 0 1      | Q2   | Q1   | Q2   | Q1   |
               | 0, 0 |0,100 | 0, 1 |0,101 |
   ---------------+------+------+------+------+
    0 1 0      | Q1   | Q2   | Q1   | Q2   |
               | 1, 0 |1,100 | 1, 1 |1,101 |
   ---------------+------+------+------+------+
    0 1 1      | Q2   | Q1   | Q2   | Q1   |
               | 1, 0 |1,100 | 1, 1 |1,101 |
   ---------------+------+------+------+------+
```

*Row Address, Column Address respectively in HEX

Page One Display Memory Map (X10 = 1)

```
            X4 | 0000 | 0000 | 0000 | 0000 |
            X3 | 0000 | 0000 | 1111 | 1111 |
            X2 | 0000 | 1111 | 0000 | 1111 |
    Y Y Y   X1 | 0011 | 0011 | 0011 | 0011 |
    2 1 0   X0 | 0101 | 0101 | 0101 | 0101 |
   ---------------+------+------+------+------+
    0 0 0      | Q1   | Q2   | Q1   | Q2   |
               | 0,080|0,180 | 0,081|0,181 |
   ---------------+------+------+------+------+
    0 0 1      | Q2   | Q1   | Q2   | Q1   |
               |0,080 | 0,180| 0,081|0,181 |
   ---------------+------+------+------+------+
    0 1 0      | Q1   | Q2   | Q1   | Q2   |
               | 1,080|1,180 |1,081 |1,181 |
   ---------------+------+------+------+------+
    0 1 1      | Q2   | Q1   | Q2   | Q1   |
               | 1,080|1,180 |1,081 |1,181 |
   ---------------+------+------+------+------+
```

Figure 2-7d. Display Memory Addressing for 1024x768x4 (2 page, Turbo Mode)

WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER	REV.
A		

SCALE	SHT	OF

93-000032-00

VIDEO DAC AND INTERFACE SUBSYSTEM

This section includes the following information for the board designer:

- Routing of VRAM pixel data to the video DAC. This involves two alternative designs, depending on whether back-end support is performed by the PWGA-1 or by external components.

- Routing of control information from the PWGA-1 to the DAC and the monitor.

- Signal routing in support of "VGA modes," in which the monitor is driven by control and data signals originating off-board, in the system VGA, and passed through to the monitor from the auxiliary video extension connector.

- Palette access, with the board design option of implementing "flicker-free mode," a Western Digital extension.

Note that a related topic, PWGA-1 recognition of monitor type, is grouped with other configuration strapping issues, and is discussed later in this chapter .

The PDM pins associated with the video interface subsystem are all outputs from the DSP, and are shown in Table 2-6.

Table 2-6. PDM Pin Interface to Video Subsystem

Name	PDM Pin #	Description
VDATA0-7	30-27 (O) 24-21 (O)	With integrated back-end support, these pins output the video data for the DAC. With external back-end support, they are not used for this purpose, since the DAC receives its data from the external logic within the VRAM block. In both cases, however, these same pins are the source of palette-loading data in flicker-free mode. (tri-state output)
SELVD	132 (O)	With the flicker-free design option, this pin selects the source of palette-loading data to be either the low eight bits of the PC data bus (normal mode) or VDATA0-VDATA7 (flicker-free mode). SELVD is also the tri-state control signal for -DACRD and -DACWR of PAM. When it is high, it disables the -DACRD and -DACWR signals of PAM.
VCLK	25 (O)	Video clock for DAC (tri-state output)
BLANK	20 (O)	Video blank signal for DAC (tri-state output)
-DACRD	31 (O)	-DAC palette read (Note that data read from the palette is always routed to the PC data bus in the CPU interface logic.)
-DACWR	32 (O)	-DAC palette write (see SELVD, above)
HSYNC	33 (O)	Horizontal sync, to the monitor (tri-state output)
VSYNC	34 (O)	Vertical sync, to the monitor (tri-state output)

WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER	REV.
A		
SCALE	SHT	OF

93-000032-00

Table 2-6. PDM Pin Interface to Video Subsystem (cont.)

Name	PDM Pin #	Description
–ENVGA	42 (O)	Enables VGA pass-through mode. This signal selects the source of video data to the DAC (either VDATA0–7 from the PDM or P0–7 from the auxiliary video extension), the control signals to the DAC (either VCLK and BLANK from the PDM, or DCLK and BLANK from the auxiliary extension), and the sync signals to the monitor (either HSYNC and VSYNC from the PDM, or HSYNC and VSYNC from the auxiliary extension).
LDCLK (SD6)	76 (O)	For external back-end support (Figure 2-9), this output signal is provided to drive the LD (load) input of the Bt451/458 DAC, where it synchronizes the serializing of the 32 bits of pixel data from the VRAM into four 8-bit pixel color selections. (With integrated back-end support, this pin is SD7 of the serial data bus from VRAM, as discussed in the previous section.)

Figures 2-8 and 2-9 describe board implementation of the video DAC and interface subsystem with integrated and external back-end support, respectively. The flicker-free design option applies to both, and is discussed later.The PWGA–1 chip set supports INMOS IMS G171/176/178, Brooktree BT471/478 and compatible video DACs for 8514/A modes. It also supports Brooktree BT451/458 and compatible for Western Digital enhanced 1280x1024 mode.

The Brooktree Bt471 DACs include a 256x18 palette, loaded with 6-bit R, G, and B color intensity values; the high two bits of the 8-bit data lines supplying these values are ignored. The Bt478 substitute a 256x24 palette, with all eight bits used for finer control of color. The DAC8 pin from PAM can be used to select 6-bit or 8-bit palette fields. Note that the palette overlay capabilities are not used; the DAC's RS2 and OL0–OL3 pins should be tied down.

Without the flicker-free option, CPU software writes data into the DAC's color palette on the low eight bits of the system data bus. The PWGA–1 intercepts CPU addressing and controls

DAC access using the low two bits of its EPROM address bus, BIOSA1 and BIOSA0. When the flicker-free option is incorporated into the board design, as shown in Figures 2-8 and 2-9, the CPU software can invoke flicker-free mode, as discussed in Chapter 3. In this mode, palette data is buffered by the PWGA–1 and released to the DAC over the VDATA0–7 lines, with the SELD control signal activated to select the VDATA lines in preference to the system data bus. Routing of the latter lines to the DAC via the SELD multiplexor is still required, both to allow for non-flicker-free mode (8514/A emulation) and for palette reads.

Figure 2-9 shows the implementation of 1280x1024 resolution with external back-end support and two DACs. The fast DAC Bt451/Bt458 is used for 1280x1024 and 1024x768 resolutions. The slow DAC is used for VGA video signal. The flicker-free capabilities do not apply to that DAC.

The CLKSEL lines and high-frequency clock source in Figure 2-9 are described later in this chapter.

2-18
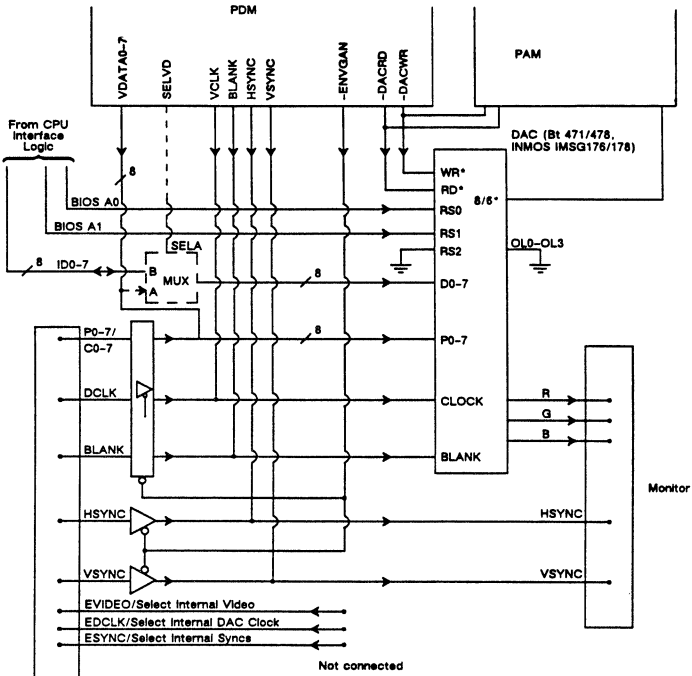
Figure 2-8. Video DAC and Interface Subsystem with Integrated Back-End Support

2-19

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

Figure 2-9a. 1280x1024 Resolution Implementation with Two DACs

WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

Figure 2-9b. Detail Schematic, pal 1280
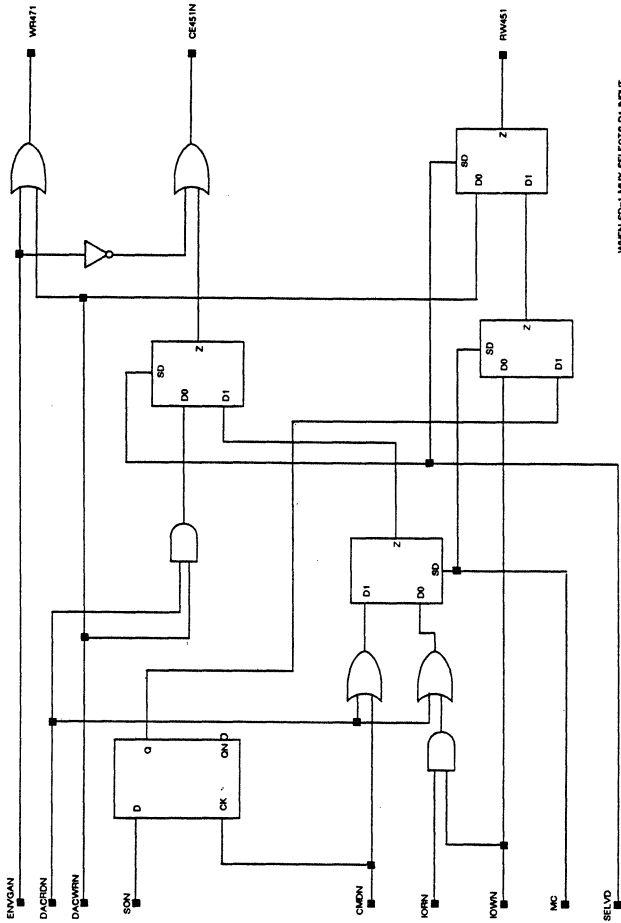
WHEN SD=1 MUX SELECTS D1 INPUT
THE LATCH IS OPEN WHEN CK IS HIGH

2-21

OTHER BOARD DESIGN ELEMENTS

EPROM

A 27256 32K UV EPROM is used on the Micro Channel board to store the Western Digital BIOS extension plus two configuration parameters that the PWGA-1 loads into internal registers upon board reset: the POS ID (for PS/2 Micro Channel system integration), chosen by the customer, and a VRAM wait-state control parameter (dependent on characteristics of the VRAM chips chosen for the board, and automatically selected from among four choices depending on how two configuration parameter pins are strapped); see Figure 2-10a &b.

EPROM is remapped for the AT bus board because of VGA conflict and widespread use of

Shadow RAM in 386 machines. BIOS EPROM Address mapping for PWGA-1 chip set is as stated in Table 2-7.

For PC AT and compatibles, 2 sets of addresses that minimize memory conflict with other products have been selected, i.e. C8800–C9FFF or D8800–D9FFF. Either address can be selected by a jumper in a board design.

The EPROM is accessed through the CIU on the PAM, which generates addressing for the EPROM and activates an output enable line. Data from EPROM ties to both the CIU and the system bus through an 8-bit connection to the internal data bus, as shown in Figure 2-11. (See also Figures 2-1 and 2-2.) The PAM pins involved are shown in Table 2-8.

Table 2-7. BIOS EPROM Address Mapping

		AT Bus	
	Micro Channel	IAD5=0 *	IAD5=1 *
2K (Fixed)	C6800–C6FFF	C8800–C8FFF	D8800–D8FFF
4K (Bank Selectable)	C7000–C7FFF	C9000–C9FFF	D9000–D9FFF
2K (Fixed)	CA000–CA7FF		

* Reset strapping signal on pin IAD5 selectable by jumper.

Table 2-8. EPROM Interface Pins

Name	PAM Pin #	I/O	Description
BSA0–BSA14	54, 53, 49–37	O	EPROM BIOS address lines
–BS OE	36	O	–EPROM BIOS chip select

2-22

EPROM Contents (Bytes)   EPROM Byte Address

	EPROM Contents (Bytes)	EPROM Byte Address
	POS ID (MSByte)	7FFF
	POS ID (LSByte)	7FFE
		7FFD
	RESERVED	↑ ↓
		7FF8

VRAM Chip Speed*	VRAM Chip Type*		EPROM Contents	EPROM Byte Address
1	1	VWSCP3**	(MSB)	7FF8
1	0	VWSCP3	(LSB)	7FF7
		VWSCP2	(MSB)	7FF6
0	1	VWSCP2	(LSB)	7FF5
0	0	VWSCP1	(MSB)	7FF4
		VWSCP1	(LSB)	7FF3
		VWSCP0	(MSB)	7FF2
		VWSCP0	(LSB)	7FF1
				7FF0
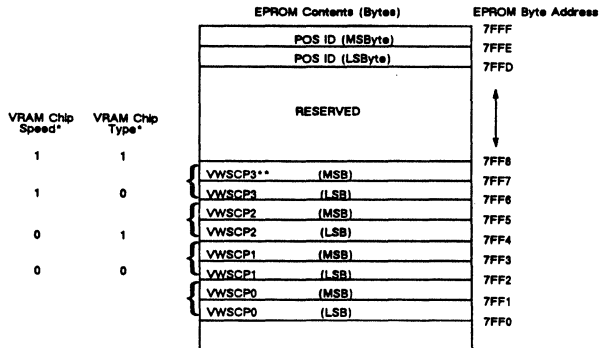
*These are signals from two of the configuration
strapping pins described in the section titled
"Configuration Strapping" as follows:

VRAM Chip Speed: 0 if –8 spec, 1 if –10 spec, IAD4 pin
VRAM Chip Type: 0 if 64Kx4, 1 if 256Kx4, IAD0 pin

***VWSCP* = VRAM Wait-State Control Parameter

Figure 2-10a. EPROM Configuration Parameters

2-23

DWG SIZE A	DRAWING NUMBER	REV.
SCALE		SHT OF

93-000032-00

15	14	13	12 11 9	8 7	6 5	4 3	2 1 0
PB	TM	DPL	DPM ROW	RH	PW	EW	CPW RPW

RPW<1:> : RAS Precharge Wait is used to select the minimum RAS precharge time. Encoding of this field is as follows:

RPW<1:0>		Min. RAS Precharge Clocks
0	0	5
0	1	6
10 1	0	7
1	1	8

CPW<1:0> : CAS Precharge Wait is used to select the minimum CAS precharge time, the minimum time CAS will be high in between page mode cycles. Encoding of this field is as follows:

CPW<1:0>		Min. CAS Precharge Clocks
0	0	2
0	1	3
1	0	4
1	1	5

EW<1:0> : Entry Wait is used to select CAS low time for entry cycles. Encoding of this field is as follows:

EW<1:0>		CAS low for _ clocks during entry
0	0	3
0	1	4
1	0	5
1	1	6

PW<1:0> : Page Wait is used to select CAS low time for page mode cycles. Encoding of this field is as follows:

EW<1:0>		CAS low for _ clocks during page mode
0	0	3
0	1	4
1	0	5
1	1	6

RH : RAS Hold. If set, RAS address hold time will be extended from 2 clocks to 3 clocks.

ROW<2:0> : Raster Operation Wait. The binary value in this field, a value between 0 and 7, gives the minimum number of clocks between the read and write of a destination RMW.

DPM : Disable Page Mode. If this bit is set, none of the memory cycles will be done in page mode regardless of their addresses.

DPL : Delay Pixel Location. If this bit is set, the earliest that pixel location information on the IAD bus, and the swap pin, can change is one clock before the rising edge of CAS, if cleared two clocks.

TM : Test Mode, if this bit is cleared the MIC operates normally. If set, the MIC goes into test mode were DRAM refresh cycles are requested every 135 clocks, and in page mode the RAS low timer times out after 20 clocks of RAS low.

Figure 2-10b. VRAM Wait-State Control Parameters

2-24

	WESTERN DIGITAL		REV.
	C O R P O R A T I O N		
DWG SIZE	DRAWING NUMBER		
A			
SCALE		SHT	OF

93-000032-00

Figure 2-11. EPROM

Within the figure:
- 2
- EPROM
- 15
- −BS OE   BSA0−14
- 8
- PAM
- BIOS A0-BIOS A1, To DAC via Video Interface Logic
- ID0-ID7: Low 8 bits of ID Data Bus, to CPU Interface Logic
- (Note: For consistency with Figure 1-1, these links are shown passing through the CPU Interface Logic first.)
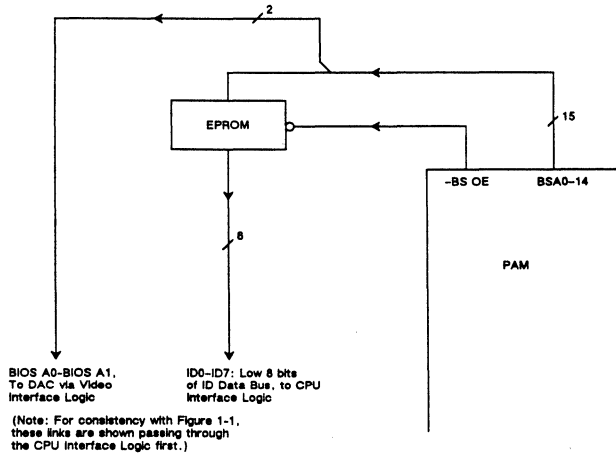
PAM-PDM Interface

The PAM and PDM are connected to each other through a 22-pin interface. Both chips include an internal bus interface unit (IBIU) which controls inter-chip communication; one of its functions is to buffer data transfers larger than eight bits, since the general-purpose inter-chip data bus is eight bits wide due to pin count constraints. Inter-chip communication is transparent to the user.

Table 2-9 specifies the interface.

Configuration Strapping

The PWGA-1 configures itself to its board design environment by latching the values of certain strapped input pins on the rising edge of the CPU's RESET signal. (It also reads two parameters from the EPROM, as mentioned earlier in this chapter.) One of these pins, which distinguishes between the Micro Channel and PC AT bus CPU interfaces, is dedicated to this purpose. Three other dedicated pins receive monitor type information, as shown in Figure 2-12 and Table 2-11. The remaining pins, which all deal with VRAM configuration information, are actually part of the inter-chip communication interface; the strapped values are driven to the inter-chip lines through tri-state buffers, as shown in Figure 2-13.

Note that if a field-upgradeable VRAM design is selected (with the VRAM chips partially populated), the appropriate strappings should be implemented with jumpers, switches, or some other method that allows the user to change the strapped values in the course of field upgrade.

Table 2-10 specifies the strappings for supplying the PWGA-1 with environmental information.

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Table 2-9. Inter-chip Interface Pins

PAM Pin No.	Signal Direction	PDM Pin No.	Signal Name
PAM 125	<--->	PDM 9	IAD0
PAM 126	<--->	PDM 8	IAD1
PAM 127	<--->	PDM 7	IAD2
PAM 128	<--->	PDM 6	IAD3
PAM 129	<--->	PDM 5	IAD4
PAM 130	<--->	PDM 4	IAD5
PAM 131	<--->	PDM 3	IAD6
PAM 132	<--->	PDM 2	IAD7
PAM 124	--->	PDM 10	IADSTAT
PAM 8	--->	PDM 126	-RWCAS
PAM 123	--->	PDM 11	RD/-WR
PAM 122	--->	PDM 12	-AS
PAM 121	--->	PDM 13	-DS
PAM 114	<---	PDM 19	RMWE
PAM 2	<---	PDM 132	SELVD
PAM 119	<---	PDM 15	SLC
PAM 118	<---	PDM 16	SLD
PAM 6	--->	PDM 128	WROE
PAM 3	--->	PDM 131	MDT0
PAM 4	--->	PDM 130	MDT1
PAM 5	--->	PDM 129	MDT2
PAM 7	--->	PDM 127	SWAP

Clock Considerations

A major design element of the PWGA–1 is the provision of two separate and independent clock rates: one for drawing operations, the other for screen refresh. In particular, faster monitors can be used without changing the clock rate of the drawing facilities within the PWGA–1, and conversely, use of slower monitors will not degrade drawing speed.

The system clock signal, provided by an external 60-MHz oscillator, drives the drawing processes within the PWGA–1, and is used to generate VRAM timing. The pixel clock, used to drive the screen refresh process, is selected from among four oscillator outputs to accommodate different types of monitors. Three PDM output signals, CLKSEL2, CLKSEL1 and CLKSEL0, are provided to make the selection.

In the United States, non-interlaced video monitors use a vertical refresh frequency of 60 Hz; in Europe, the standard is 70 Hz. Including the interlaced IBM 8514 monitor (vertical frequency 43.48 Hz) produces Table 2-13, in which the "Pixel Frequency" is the frequency of the oscillator selected by CLKSEL2, CLKSEL1 and CLKSEL0 as input to the PDM's PCLK pin.

WESTERN DIGITAL C O R P O R A T I O N			
DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT	OF

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Table 2-10. Configuration Strapping Pins

PAM Pin No.		Description
PAM 120		(MC/-AT) High if Micro Channel, low if PC-AT bus
PDM 36-38		(MID2-MID0) Monitor ID Bits 2-0 (See Table 2-11)
PAM 130/PDM 4	IAD5	EPROM location for AT Bus design (not used in Micro Channel): low for EPROM memory address at C8800h to C9FFFh, high for address at D8800h to D9FFFh
PAM 131/PDM 3	IAD6	Test Mode: Low if test mode, high if normal mode
PAM 132/PDM 2	IAD7	DAC Type: Low if 6-bit DAC, high if 6-/8- bit DAC
PAM 129/PDM 5	IAD4	VRAM chip speed: high if -10 spec, low if -8 spec (Jumper/switch if appropriate for field upgrade)
PAM 128/PDM 6 for	IAD3	Maximum resolution allowed by VRAM design: low if 1280x1024, high if 1024x768 (Jumper/switch if appropriate field upgrade)
PAM 125/PDM 9	IAD0	VRAM chip type: high if 256Kx4, low if 64Kx4
PAM 126/PDM 8	IAD1	Low-order bit of two-bit VRAM chip count field (see below; jumper/switch if appropriate for field upgrade)
PAM 127/PDM 7	IAD2	High-order bit of two-bit VRAM chip count field (see below; jumper/switch if appropriate for field upgrade)

CHIP-COUNT STRAPPING		256Kx4	64Kx4
IAD2	IAD1		
0	0	4 chips	16 chips
0	1	8 chips	32 chips
1	0	16 chips	reserved
1	1	reserved	reserved

PAM Pin No.		Description
PAM 122/PDM 12	-AS	Monitor Type Select
PAM 123/PDM 11	RD/-WR	Monitor Type Select

-AS	RD/-WR	Type
0	0	8514A display
0	1	60-Hz monitor
1	0	reserved
1	1	70-Hz monitor

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Figure 2-12. Monitor ID Strapping

Table 2-11. Monitor ID Interpretation

MID2	MID1	MID0	Monitor Type
0	0	0	Not defined
0	0	1	Not defined
0	1	0	IBM 8514 (color, 1024x768, interlaced)
0	1	1	Not defined
1	0	0	Not defined
1	0	1	IBM 8503 (monochrome, 640x480, non-interlaced)
1	1	0	IBM 8513 (color, 640x480, non-interlaced) & 8512
1	1	1	Other display*

* MID2-0 have internal pull-up resistors. During reset, MID2-0 can be also used to test PDM internal counters. For in-circuit board test MID2-0 should be high when RESET is asserted.
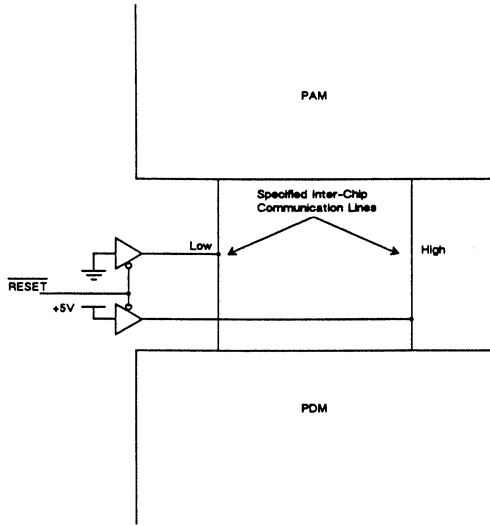
Figure 2-13. VRAM Configuration Strapping Examples (see Table 2-10)

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WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT OF	

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Table 2-12. Pixel Clock Frequency Derivation

CLKSEL2	CLKSEL1	CLKSEL0	Resolution*	Vertical Frequency	Horizontal Frequency	Pixel Frequency
0	0	0	640x480N	60.00 Hz (U.S.)	31.47 kHz	25.18 MHz
1	0	0	640x480N	70.00 Hz (Eur.)	37.28 kHz	31.32 MHz
0	0	1	1024x768I	43.48 Hz (IBM)	35.52 kHz	44.90 MHz
1	0	1	1280x1024N	60.00 Hz (U.S.)	63.78 kHz	109.64 MHz**
			1280x1024N	70.00 Hz (Eur.)	74.83 kHz	136.71 MHz**
0	1	1	1024x768N	60.00 Hz (U.S.)	49.06 kHz	63.98 MHz
1	1	1	1024x768N	70.00 Hz (Eur.)	56.18 kHz	74.16 MHz

*N=Non-interlaced
I=Interlaced
**In these cases, the oscillator output frequency must be halved (to 54.82 MHz or 68.36 MHz) before being connected to the PCLK input pin of the PDM. Since this resolution requires external back-end support, however, the original frequency, as shown, must remain intact to drive the Bt451/458 DAC clock, as per Figure 2-9.

Table 2-13. Clock Pin Summary

Name	Pin #	I/O	Description
SCLK	PDM 39/PAM 113	I	System clock input; requires 60 MHz
CLKSEL2	PDM 43	O	Selects from among seven frequencies for PCLK, as per Table 2-12
CLKSEL1	PDM 44	O	See Table 2-12
CLKSEL0	PDM 45	O	See Table 2-12
PCLK	PDM 68	I	Pixel clock input
VCLK	PDM 25	O	DAC clock source (see "Video DAC and Interface Subsystem")
LDCLK (SD6)	PDM 76	O	LD signal source for Bt451/458 DAC, for external back-end support (see earlier in this chapter)

The typical PWGA-1-based board will therefore be configured with oscillators at 25.28, 44.90, and 64.37 MHz for use with U.S. standard monitors, or with oscillators at 31.40, 44.90, and 74.16 MHz for use with European standard monitors. A more ambitious design might include all seven clock frequencies, with the MID2–MID0 inputs (as per "Configuration Strapping" earlier in this chapter) aiding in the selection.

The PWGA–1 pins involved in clock signal generation and use are summarized in Table 2-13.

3
Software Interface

IBM® 8514/A COMPATIBLE REGISTERS

Although a PWGA-1-based board is significantly more capable than the IBM 8514/A, especially when configured with sufficient VRAM, the base mode of the board's operations is that of exact 8514/A emulation, including exact compatibility with the 8514/A's user-accessible registers.

The PWGA-1 internal registers that are compatible with the IBM 8514/A are defined in this section. Summary of 8514/A compatible registers and Western Digital enhanced registers are shown in Table 3-6 and Table 3-7 respectively.

All PWGA-1 registers, except DAC interface registers, are 16-bit word-addressed. The unused bits are either not shown or marked with the letter U in the description of the register definitions below. The reserved bits are marked with the letter R.

DAC Interface

The 8-bit registers in Table 3-1 are used to program the external video DAC. It is possible to write and read the DAC. Once the read/write index is written, multiple read/write operations can be performed without having to set the index for each entry.

Procedure to write to the DAC:

1. Set start write color index at 02ECH.

2. Write three bytes (R, G, B values) at 02EDH (The index auto increments to the next write entry).

3. Repeat step 2 until the desired number of entries have been programmed.

Procedure to read from the DAC:

1. Set start read color index at 02EBH.

2. Read three bytes (R, G, B values) at 02EDH (The index auto increments to the next read entry).

3. Repeat step 2 until the desired number of entries have been read.

Table 3-1. DAC Color Programming Registers

Color Programming	8514/A	VGA
Look Up Table Mask (R/W)	02EA	03C6
Read Color Index	02EB (Write Only)	03C7 (Write Only)
DAC State	02EB (Read Only)	03C7 (Read Only)
Color Index (R/W)	02EC	03C8
RGB Color Value (R/W)	02ED	03C9

3-1

WESTERN DIGITAL
CORPORATION

DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT	OF

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Graphics Mode Control Register

Graphics mode is selected by writing to the Graphics Mode Control (GMC) Register at address 4AE8h (see Figure 3-1). This register is used by all modules within the PWGA-1. Set Bit 0 to 1 to select 8514/A graphics mode or 0 to select VGA pass through mode. Bits 1 and 3 are reserved for mode extension; set Bit 1 to 1. Bit 2 selects the screen resolution; set Bit 2 to 1 to select 1024x768 (44.9 MHz) or 0 to select 640x480 (25.175 MHz).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	U	U	U	U	U	U	U	R		1	

Mode
  L 0=VGA
    1=8514/A

Reserved
(Don't Care)

Resolution
0=640x480
1=1024x768
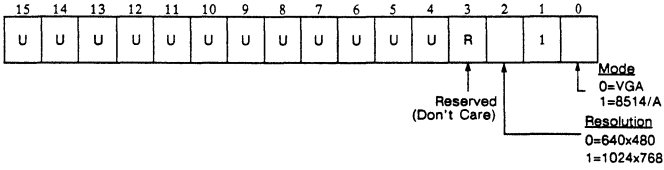
Figure 3-1. Graphics Mode Control Register (4AE8h Write Only)

3-2

Video Timing Setup Registers

There are nine registers for setting up video timing: four for horizontal, four for vertical, and one for control. Two sets of these registers (Table 3-2) are provided by PWGA-1 to allow video timing parameters to be preprogrammed and locked in for 640x480 and 1024x768 resolutions by Western Digital's BIOS. This extended feature is designed for interfacing with different monitors requiring different timing parameters. Once the timing parameters are locked in (see Figure 3-38), application software that writes directly to the video registers will not need to be changed for dif-

ferent monitors, e.g., interlaced vs. non-interlaced. These registers affect the DSP module of the PWGA-1. The horizontal and vertical registers are set by the selected resolution. For example, if 1024x768 is the graphics mode selected by the GMC Register, then the horizontal and vertical registers are set accordingly. Table 3-2 shows what register value to set depending on the resolution selection.

Figures 3-2 through 3-9 show the format for the horizontal and vertical registers. Vertical timing is programmed in line resolution. Horizontal timing is programmed in 8-pixel resolution.

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Set Number of Pixels per Line
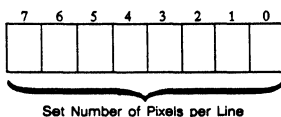
**Figure 3-2. Horizontal Total Register
(02E8h Write Only)**

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ 0 │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Set Number of Pixels Displayed
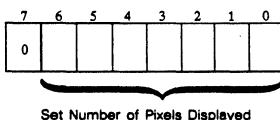
**Figure 3-3. Horizontal Active Register
(06E8h Write Only)**

3-3

	WESTERN DIGITAL CORPORATION	
DWG SIZE **A**	DRAWING NUMBER	REV.
SCALE	SHT	OF

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Set Horizontal Sync Position
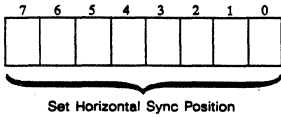
Figure 3-4. Horizontal Sync Position Register
(0AE8h Write Only)

Set Number of Lines Displayed
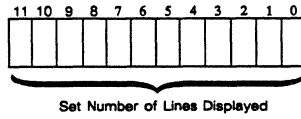
Figure 3-7. Vertical Active Register (16E8h
Write Only)

Polarity
1=negative   Set Horizontal Sync Width
0=positive
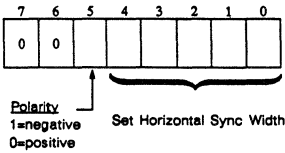
Figure 3-5. Horizontal Sync Width and Polar-
ity Register (0EE8h Write Only)

Set Vertical Sync Position
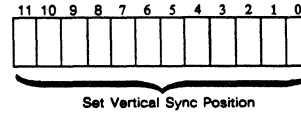
Figure 3-8. Vertical Sync Position Register
(1AE8h Write Only)

Set Number of Lines per Frame
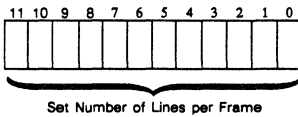
Figure 3-6. Vertical Total Register (12E8h
Write Only)

Polarity   Set Vertical Sync Width
1=negative
0=positive
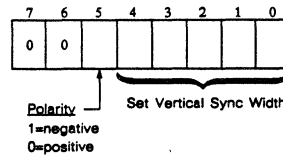
Figure 3-9. Vertical Sync Width and Polarity
Register (1EE8h Write Only)

3-4

Table 3-2. CRT Control Register Parameters And Timing

		1024x768			640x480 (4 or 8)	
frame rate pclk		43Hz I. 44.90MHz 22.27ns	60Hz NI. 63.98MHz 15.63ns	70Hz NI. 74.16MHz 13.46ns	60Hz NI. 25.18MHz 39.92ns	70Hz NI. 31.32MHz 31.93ns
02E8	Htotal	9d	a2	a4	63	68
06E8	Hdisplay	7f	7f	7f	4f	4f
0AE8	Hsync pos.	81	83	83	52	54
0EE8	Hsync & polarity	16	16	16	2c	2c
12E8	Vtotal	660	660	642	830 (4) 418 (8)	848 (4) 426 (4)
16E8	Vdisplay	5fb	5fb	5fb	779 (4) 3bb (8)	779 (4) 3bb (8)
1AE8	Vsync pos.	600	600	600	7a8 (4) 3d2 (8)	7b8 (4) 3de (8)
1EE8	Vsync & polarity	8	8	8	22	22
22E8	CONTROL	33	23	23	21 (4) 23 (8)	21 (4) 23 (8)
Htotal	(us)	28.25	20.38	17.80	31.78	26.82
Hdisp.	(us)	22.89	16.00	13.81	25.42	20.44
Hblank	(us)	5.37	4.376	3.99	6.355	6.39
Hsync.	(us)	3.93	2.751	2.373	3.813	3.07
Hfporch	(us)	0.178	0.375	0.323	0.636	1.02
Hbporch	(us)	1.25	1.250	1.294	1.906	2.30
Vtotal	(ms)	23.08	16.65	14.29	16.68	14.24
Vdisp.	(ms)	21.70	15.65	13.67	15.25	12.87
Vblank	(ms)	0.706 (even) 0.678 (odd)	0.999	0.623	1.430	1.368
Vsync.	(ms)	0.113	0.082	0.071	0.079	0.067
Vfporch	(ms)	0.0141 (even) 0 (odd)	0.020	0.018	0.350	0.402
Vbporch	(ms)	0.579 (even) 0.565 (odd)	0.897	0.534	1.00	0.898
HS polarity		+	+	+	-	-
VS polarity		+	+	+	-	-

3-5

Display Control Register

The Display Control (DSC) Register sets various control features for the display functions (see Figure 3-10).

Skip Y1   Set Bit 1 to 0 to skip Bit 1 of the y scan counter in the screen refresh. This allows two pages to be displayed in 640x480x4 screen resolution.

Skip Y2   Set Bit 2 to 0 to skip Bit 2 of the y scan counter in the screen refresh.

This allows two pages to be displayed in 1024x768x4 screen resolution.

Scan   Bit 3 set to 1 specifies double scan (2); 0 specifies single scan (1).

Interlace   Bit 4 set to 1 specifies interlace mode; 0 specifies non-interlace mode.

Enable Display   Bits 5 and 6 work together to enable/reset the display. The display is enabled when Bits 5 and 6 are set to 01 and reset when set to 10. These two bits are not affected by the locked-in extended feature.
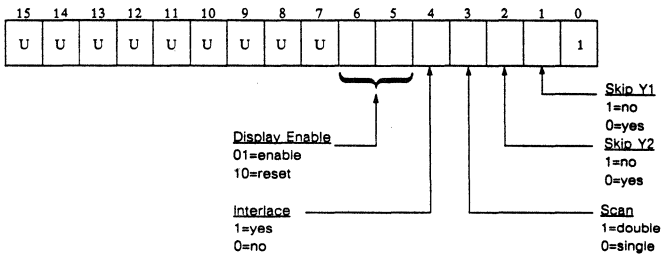

Figure 3-10. Display Control Register (22E8h Write Only)

3-6

DWG SIZE	DRAWING NUMBER	REV.
A		
SCALE	SHT	OF

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Interrupt Control Register

The Interrupt Control (IC) Register at address 42E8h is used for interrupt and reset control of the PWGA-1 FIFO and other CPU interface functions (see Figure 3-11). This register is write only and affects Bits 3-0 of the Interrupt Status (IS) Register (see "Interrupt Status Register" in this chapter). The IS Register is a read only register also at address 42E8h.

Vsync   Bit 0 puts a 0 in the vertical sync status bit of the IS Register that can be read at address 42E8h.

Graphic Engine (GE) Busy   Bit 1 puts a 0 in the GE busy status bit of the IS Register that can be read at address 42E8h.

FIFO Overflow & Invalid   Bit 2 puts a 0 in the FIFO overflow status bit of the IS Register that can be read at address 42E8h. This bit is

Read   cleared at the end of every line during a read across the plane.

FIFO Empty   Bit 3 puts a 0 in the FIFO empty status bit of the IS Register that can be read at address 42E8h.

Vsync   Bit 8 enables/disables the vertical sync interrupt.

GE Busy   Bit 9 enables/disables the GE busy interrupt.

FIFO Overflow   Bit 10 enables/disables the FIFO overflow interrupt.

FIFO Empty   Bit 11 enables/disables the FIFO empty interrupt.

Hardware Test   Bit 12=1, Bit 13=0 is used for Normal mode.

GE Reset   Bits 15 and 14 are used to switch between normal mode and reset

bit 13	bit 12	
0	0	No Change
0	1	Normal
1	0	Test

bit 15	bit 14	Graphic Engine Reset
0	1	Normal
1	0	Reset
0	0	No Change
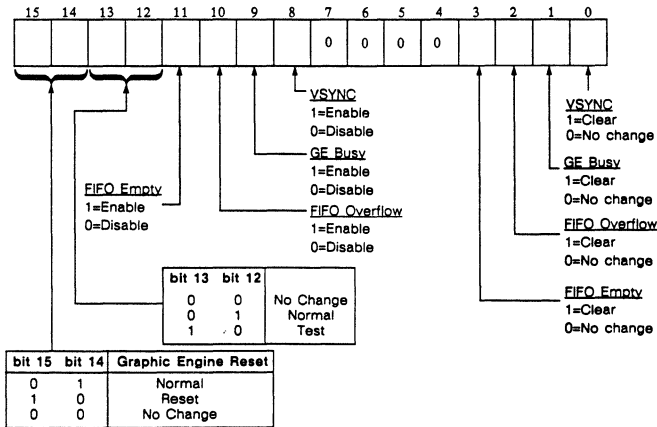
Figure 3-11. Interrupt Control Register (42E8h Write Only)

3-7

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EPROM Selection Register

The EPROM Select (ES) Register is used by the CIU to enable EPROM bank selection and select a bank of EPROM. Figure 3-12 shows the register format for bank selection. Bit 3 enables/disables bank selection. This register is remapped to 36E8h for AT Bus because VGA uses the 46E8h register.


```
 7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ U │ U │ U │ U │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘

        EPROM
        1=Enable
        0=Disable    ┌───┬───┬───┬─────────────┐
                     │ 2 │ 1 │ 0 │ Select Bank │
                     ├───┼───┼───┼─────────────┤
                     │ 0 │ 0 │ 0 │      0      │
                     │ 0 │ 0 │ 1 │      1      │
                     │ 0 │ 1 │ 0 │      2      │
                     │ 1 │ 1 │ 1 │      3      │
                     │ 1 │ 0 │ 0 │      4      │
                     │ 1 │ 0 │ 1 │      5      │
                     │ 1 │ 1 │ 0 │      6      │
                     │ 1 │ 1 │ 1 │      7      │
                     └───┴───┴───┴─────────────┘
```
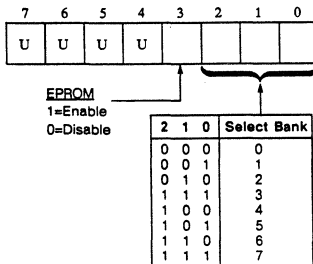
Figure 3-12. EPROM Select Register (46E8h Write Only—Micro Channel)
(36E8h Write Only—AT Bus)

BIOS EPROM Memory Location

BIOS EPROM memory location for Micro Channel consists of 2K fixed at C6800h to C6FFFh, 2K fixed at CA000h to CA7FFh, and 4K banks at C7000h to C7FFFh. BIOS EPROM memory location for AT bus consists of two options: C8800–C9FFF or D8800–D9FFF (see Table 3-3), selectable by the strapping pin IAD5.

Table 3-3. Options for BIOS EPROM Memory Locations for AT Bus

Memory Location	Micro Channel	AT Bus	
		Strapping IAD5=0	Strapping IAD5=1
2K Fixed	C6800h–C6FFFh	C8800h–C8FFFh	D8800h–D8FFFh
4K Bank Selected	C7000h–C7FFFh	C9000h–C9FFFh	D9000h–D9FFFh
2K Fixed	CA000h–CA7FFh		

3-8

Drawing Control

There are sixteen registers involved in drawing control. These registers affect the operation of the GP, DP, MIC, and CIU.

Current Y Position (CYP) Register

The CYP Register at address 82E8h uses Bits 10-0 to define the current position of y for the pixel being drawn (see Figure 3-13). The value is 11 bits unsigned. Note that Bit 11 is reserved for higher resolution. PWGA-1's enhanced resolution (1280x1024) mode does not use this bit.

Current X Position (CXP) Register

The CXP Register at address 86E8h uses Bits 10-0 to define the current position of x for the pixel being drawn (see Figure 3-14). The value is 11 bits unsigned. Note that Bit 11 is reserved for higher resolution. PWGA-1's enhanced resolution (1280x1024) mode does not use this bit. The status of this register can be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	R											

↑
Reserved   Current Y of Drawing Point Value
(Don't Care)
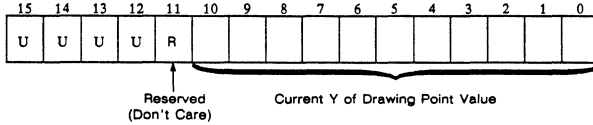
Figure 3-13. Current Y Position Register (82E8h Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	R											

↑
Reserved   Current X of Drawing Point Value
(Don't Care)
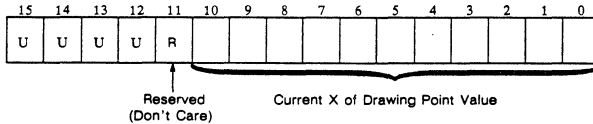
Figure 3-14. Current X Position Register (86E8h Read/Write)

3-9

	WESTERN DIGITAL		
	C O R P O R A T I O N		
DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT	OF

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Copy Y Destination/Incr 1 (CYDI) Register

The CYDI Register at address 8AE8h uses either Bits 10–0 to define the y destination when BITBLT copying, or Bits 11–0 to define Incre-ment 1 value when drawing a line (see Figure 3-15). The command performed is specified by the Drawing Command (DC) Register. The value is 12 bits unsigned when line drawing is specified. The minterm for the line drawing is:

Increment 1 = $2 \cdot (\min(|dx|, |dy|))$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U					2's complement							

Line Parameter : Increment 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	R											

Reserved
(Don't Care) Copy Y Destination

Figure 3-15. Copy Y Destination/Incr 1 Register (8AE8h Write Only)

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Copy X Destination/Incr 2 (CXDI) Register

The CXDI Register at address 8EE8h uses either Bits 10-0 to define the *x* destination when BITBLT copying, or Bits 12-0 to define Incr2

value when drawing a line (see Figure 3-16). The command performed is specified by the Drawing Command (DC) Register. The value is 13 bits signed when line drawing is specified. The min-term for the line drawing is:
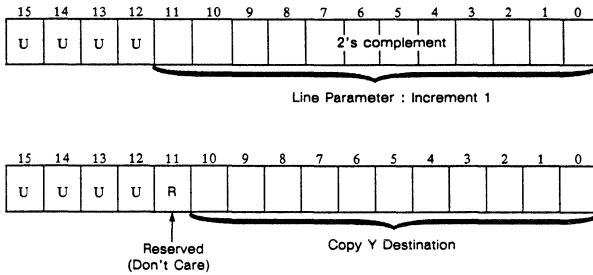
Increment 2 $= 2*(min(|dx|,|dy|)-max(|dx|,|dy|))$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U					2's complement (always negative)								

Line Parameter : Increment 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	R											

Reserved (Don't Care) ↑   Copy X Destination
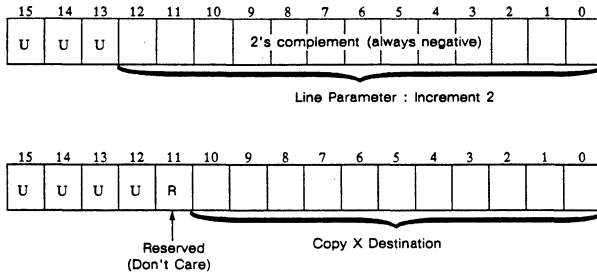
Figure 3-16. Copy X Destination/Incr 2 Register (8EE8h Write Only)

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

Delta Line (DL) Register

The DL Register at address 92E8h uses Bits 12–0 to define the delta for the current line drawing (see Figure 3-17). The value is 13 bits signed 2's complement. The minterm for the line drawing is:

$$2 \cdot [\min(|dx|,|dy|)] - \max(|dx|,|dy|) - 1$$

if starting x < ending x, and

$$2 \cdot [\min(|dx|,|dy|)] - \max(|dx|,|dy|)$$

if starting x $\geq$ ending x.

The status of this register, when read after line drawing, is sign extended to 16 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								2's complement							

Sign Extension   Delta Line Value
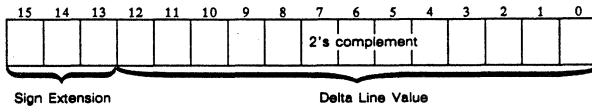
Figure 3-17. Delta Line Register (92E8h Read/Write)

3–12

WESTERN DIGITAL CORPORATION		
DWG SIZE **A**	DRAWING NUMBER	REV.
SCALE	SHT	OF

93-000032-00

Rectangle Width/Max (RWM) Register

The RWM Register at address 96E8h uses Bits 10-0 to either define the width for a rectangle in BITBLT or rectangle mode or draw a line (see Figure 3-18). The command performed is speci-fied by the Drawing Command (DC) Register. The value is 11 bits unsigned. When line drawing is specified, the minterm for the line drawing is:

Line Parameter = $\max(|dx|,|dy|)$

Rectangle Width Value = Rectangle Width − 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U											

Rectangle Width Value or Line Parameter: Max Delta
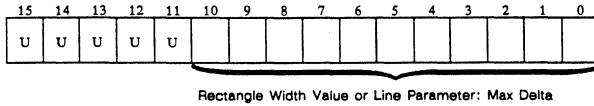
Figure 3-18. Rectangle Width/Max Register (96E8h Write Only)

3-13

Drawing Command (DC) Register

The DC Register at address 9AE8h provides commands for drawing (see Figure 3-19). All parameters have to be set before this command is sent to activate the drawing.

R/W   Bit 0 specifies a read operation when set to 0 and a write operation when set to 1.

Pixel   Bit 1 specifies single-pixel mode when
Mode   set to 0 and multi-pixel mode when set to 1.

Last Pixel   Bit 2 specifies the last pixel is drawn
Off   when set to 0 and turned off when set to 1.

Dir Type   Bit 3 specifies the type of line drawing direction as either radial (Deg) or co-ordinate-based (XY). The programmed direction is specified by Bits 7–5 of the DC Register. Direction type is radial when set to 1 and coordinate-based when set to 0.

Draw   Bit 4 specifies draw when set to 1 and update the drawing point only when set to 0.

Drawing   Bits 7–5 specify the direction to draw
Direction   using the direction type indicated by Bit 3 (see Figure 3-19).

Wait   Bit 8 provides a wait state when set to 1 to allow waiting for CPU data during functions such as image transfer and texture line drawing.

Bus Select   Bit 9 specifies that the 16-bit data bus is selected when set to 1 and the 8-bit data bus is selected when set to 0.

Future   Bit 10 allows the PAM to interface with two PDM chips. This capability is not currently supported.

Swap   Bit 12, when set to 1, specifies that
MSB/LSB   the most significant byte (MSB) be swapped with the least significant byte (LSB) when the 16-bit data bus is selected (i.e., Bit 9=1). Bit 12 is normally set to 0, the MSB is drawn first, then the LSB.

Command   Bits 15–13 specify the commands for
Type   drawing (see Figure 3-19).

3-14

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0	R										

- Wait
  - 1=Yes
  - 0=No
- Bus Select
  - 1=16
  - 0=8
- Future
  - (Don't Care)
- SWAP MSB/ LSB
  - 1=Yes
  - 0=No
- Draw
  - 1=Yes
  - 0=No
- DIR Type
  - 1=Deg
  - 0=XY
- Last Pixel
  - 1=Off
  - 0=On
- Pixel Mode
  - 1=Multi
  - 0=Single
- R/W
  - 1=W
  - 0=R

			Drawing Direction	
7	6	5	Bit 3=1	Bit 3=0
0	0	0	0 degrees	Y neg, X major, X neg
0	0	1	45 degrees	Y neg, X major, X pos
0	1	0	90 degrees	Y neg, Y major, X neg
0	1	1	135 degrees	Y neg, Y major, X pos
1	0	0	180 degrees	Y pos, X major, X neg
1	0	1	225 degrees	Y pos, X major, X pos
1	1	0	270 degrees	Y pos, Y major, X neg
1	1	1	315 degrees	Y pos, Y major, X pos

15	14	13	Drawing Function Command
0	0	0	No Operation
0	0	1	Draw Line
0	1	0	Fill Rectangle (Hor. 1st by 4 Hor. pixels); Search & Fill*
0	1	1	" " (Vert. 1st by 2 Vert. pixels)*
1	0	0	" " (Vert. 1st by 4 Hor. pixels)
1	0	1	Draw Line (Polygon Boundary)
1	1	0	BITBLT
1	1	1	Not defined

* see BEE8-A

Figure 3-19. Drawing Command Register (9AE8h Write Only)

3-15

Short Stroke Vector Control (SSVC) Register

The SSVC Register at address 9EE8h provides two bytes of data. Each byte specifies the length, direction, and move/draw control for a short vector.

Pixel Line Length   Bits 3–0 and 11–8 define the pixel line length.

Move/Draw Bit 4 indicates a draw function when set to 1 and a move function when set to 0.

Drawing Direction Bits 7–5 and 15–13 specify the direction to draw using the direction type, either radial-based or coordinate-based, as specified by Bit 3 of the DC Register.
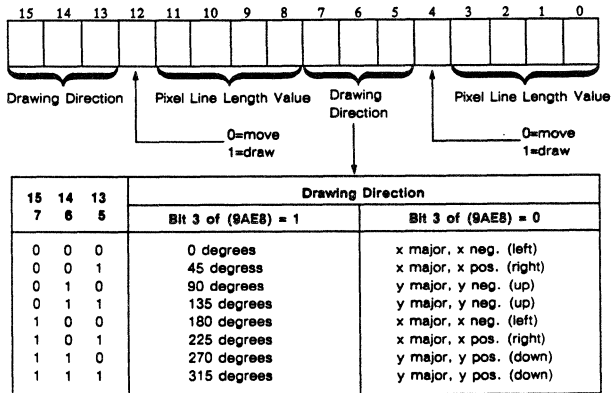

15 14 13	Drawing Direction	
7 6 5	Bit 3 of (9AE8) = 1	Bit 3 of (9AE8) = 0
0 0 0	0 degrees	x major, x neg. (left)
0 0 1	45 degress	x major, x pos. (right)
0 1 0	90 degrees	y major, y neg. (up)
0 1 1	135 degrees	y major, y neg. (up)
1 0 0	180 degrees	x major, x neg. (left)
1 0 1	225 degrees	x major, x pos. (right)
1 1 0	270 degrees	y major, y pos. (down)
1 1 1	315 degrees	y major, y pos. (down)

Figure 3-20. Short Stroke Vector Control Register (9EE8h Write Only)

3-16

93-000032-00

Background Color (BC) Register

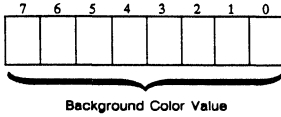The BC Register at address A2E8h specifies the background color (see Figure 3-21). The MSB in this word is not used.

```
 7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Background Color Value

Figure 3-21. Background Color Register
(A2E8h Write Only)

Foreground Color (FC) Register

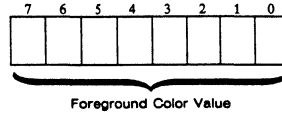The FC Register at address A6E8h specifies the foreground color (see Figure 3-22). The MSB in this word is not used.

```
 7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Foreground Color Value

Figure 3-22. Foreground Color Register
(A6E8h Write Only)

3-17

WESTERN DIGITAL			
C O R P O R A T I O N			
DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT	OF

93-000032-00

Bit-plane Write Mask (BWM) Register

The BWM Register at address AAE8h specifies the bit-plane selected for graphics or text update (see Figure 3-23). The MSB in this word is not used.

Bit-plane Read Mask (BRM) Register

The BRM Register at address AEE8h specifies the read source mask for graphics or text update (see Figure 3-24). The value is the true mask rotated left one bit; that is, Bit 0 is the mask for plane 7 and Bits 1-7 are the mask bits for planes 0-6, respectively. However, for polygon fill, Bits 2, 3, and 4 are for planes 2, 3, and 4, respectively. The MSB in this word is not used.
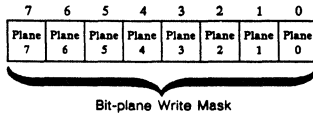
7	6	5	4	3	2	1	0
Plane 7	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0

Bit-plane Write Mask

Figure 3-23. Bit-plane Write Mask Register (AAE8h Write Only)

BITBLT

			4	3	2	1	0
			Plane 3	Plane 2	Plane 1	Plane 0	

4-bit Bit-plane

7	6	5	4	3	2	1	0
Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0	Plane 7

8-bit Bit-plane

7	6	5	4	3	2	1	0
Plane 7*	Plane 6*	Plane 5*	Plane 4*	Plane 3*	Plane 2*	Plane 1*	Plane 0*

* = plane no. corresponds to bit no.
for search & fill.

For each plane: 1=yes
0=no
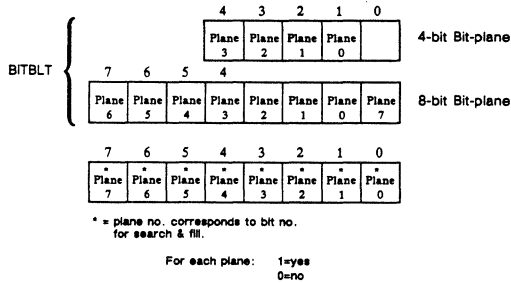
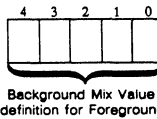**Figure 3-24. Bit-plane Read Mask Register (AEE8h Write Only)**

3-18

Comparison Color (CC) Register

The CC Register at address B2E8h specifies the comparison color (see Figure 3-25). The MSB in this word is not used.

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Comparison Color Value
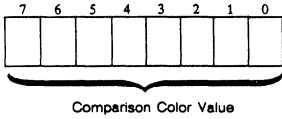
**Figure 3-25. Comparison Color Register
(B2E8h Write Only)**

Background Mix (BM) Register

The BM Register at address B6E8h specifies the background mix (see Figure 3-26). The MSB in this word is not used.

```
      4   3   2   1   0
    ┌───┬───┬───┬───┬───┐
    │   │   │   │   │   │
    └───┴───┴───┴───┴───┘
```

Background Mix Value
see definition for Foreground Mix

**Figure 3-26. Background Mix Register
(B6E8h Write Only)**

3–19

Foreground Mix (FM) Register

The FM Register at address BAE8h specifies the foreground mix (see Figure 3-27). Bits 4-0 spec-ify the foreground mix command. Bits 6 and 5 specify color selection. The MSB in this word is not used.
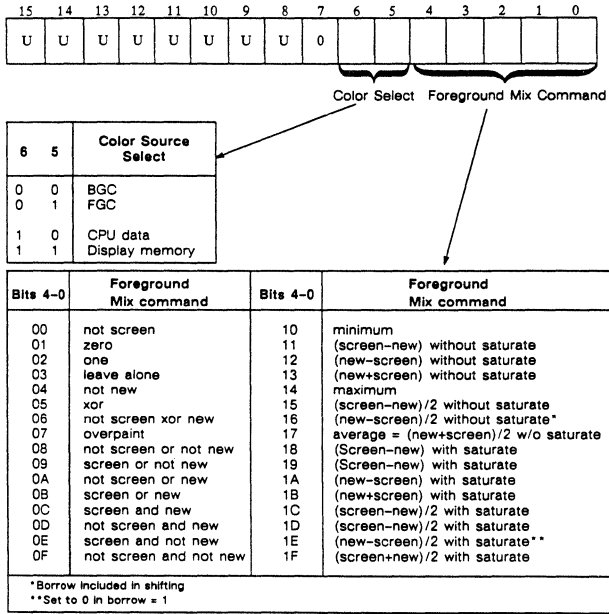
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	U	U	U	0							

Color Select Foreground Mix Command

6	5	Color Source Select
0	0	BGC
0	1	FGC
1	0	CPU data
1	1	Display memory

Bits 4-0	Foreground Mix command	Bits 4-0	Foreground Mix command
00	not screen	10	minimum
01	zero	11	(screen-new) without saturate
02	one	12	(new-screen) without saturate
03	leave alone	13	(new+screen) without saturate
04	not new	14	maximum
05	xor	15	(screen-new)/2 without saturate
06	not screen xor new	16	(new-screen)/2 without saturate*
07	overpaint	17	average = (new+screen)/2 w/o saturate
08	not screen or not new	18	(Screen-new) with saturate
09	screen or not new	19	(Screen-new) with saturate
0A	not screen or new	1A	(new-screen) with saturate
0B	screen or new	1B	(new+screen) with saturate
0C	screen and new	1C	(screen-new)/2 with saturate
0D	not screen and new	1D	(screen-new)/2 with saturate
0E	screen and not new	1E	(new-screen)/2 with saturate**
0F	not screen and not new	1F	(screen+new)/2 with saturate

*Borrow included in shifting
**Set to 0 in borrow = 1

Figure 3-27. Foreground Mix Register (BAE8h Write Only)

3-20

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Multifunction Control (MC) Register

The MC Register at address BEE8h specifies several drawing control parameters (see Figure 3-28a). Bits 15–12 control the use of this register; when these bits are changed, the register changes function.

Rectangle Height Register

When Bits 15–12 are set to 0, the value in Bits 10–0 specifies rectangle height.

    Value = rectangle height – 1

Clip Window Top Limit Register

When Bits 15–12 are set to 1, the value in Bits

10–0 specifies the clipping window top limit.

Clip Window Left Limit Register

When Bits 15–12 are set to 2, the value in Bits 10–0 specifies the clipping window left limit.

Clip Window Bottom Limit Register

When Bits 15–12 are set to 3, the value in Bits 10–0 specifies the clipping window bottom limit.

Clip Window Right Limit Register

When Bits 15–12 are set to 4, the value in Bits 10–0 specifies the clipping window right limit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				R											

Drawing Select — Rectangle/Clipping Parameter Value

Bit 11 is reserved.
(Don't care for BEE8-0.)

15	14	13	12	Addr.	Parameter
0	0	0	0	BEE8-0	Rectangle height – 1
0	0	0	1	BEE8-1	Clipping window top limit
0	0	1	0	BEE8-2	Clipping window left limit
0	0	1	1	BEE8-3	Clipping window bottom limit
0	1	0	0	BEE8-4	Clipping window right limit

Figure 3-28a. Multifunction Control Register (BEE8-0,1,2,3,4 Write Only)

3-21

WESTERN DIGITAL CORPORATION		
DWG SIZE **A**	DRAWING NUMBER	REV.
SCALE	SHT	OF

93-000032-00

Memory Configuration Register

When Bits 15–12 are set to 5, memory configuration is selected. Bit 0 is reserved and should be set to 0. Bit 1 is reserved and should be set to 1. Bits 2 and 3 (RES) specify resolution and Bit 4 specifies planes for drawing (see Figure 3-28b).
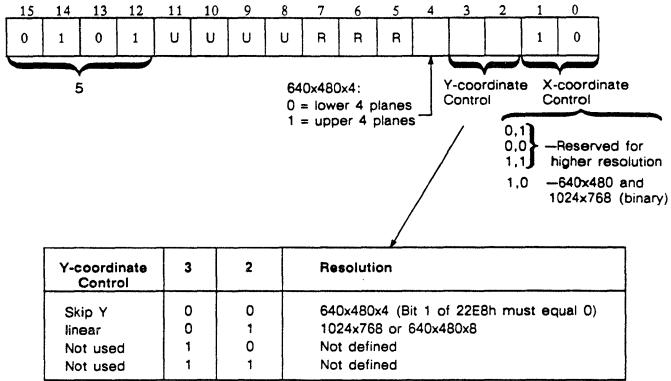
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	U	U	U	U	R	R	R				1	0

5

640x480x4:
0 = lower 4 planes
1 = upper 4 planes

Y-coordinate Control

X-coordinate Control

0,1
0,0 —Reserved for
1,1 higher resolution

1,0 —640x480 and
1024x768 (binary)

Y-coordinate Control	3	2	Resolution
Skip Y	0	0	640x480x4 (Bit 1 of 22E8h must equal 0)
linear	0	1	1024x768 or 640x480x8
Not used	1	0	Not defined
Not used	1	1	Not defined

Figure 3-28b. Memory Configuration Register (BEE8-5 Write Only)

3-22

93-000032-00

Pixel Position Mix Control/L Register

When Bits 15-12 are set to 8, Pixel Position Mix Control/L is selected (see Figure 3-28c). Bits 4-1 specify the pixel position mix control for pixels 0-3.

Pixel Position Mix Control/H Register

When Bits 15-12 are set to 9, Pixel Position Mix Control/H is selected (see Figure 3-28c). Bits 4-1 specify the pixel position mix control for pixels 4-7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0		U	U	U	U	U	U	U					0

Position Mix Control
0=low   BEE8-8
1=high   BEE8-9

Position Mix Control

High	Low
pixel 4	pixel 0
pixel 5	pixel 1
pixel 6	pixel 2
pixel 7	pixel 3

0=no
1=yes

Figure 3-28c. Pixel Position Mix Control Register (BEE8-8, BEE8-9 Write Only)

3-23

	WESTERN DIGITAL		
	C O R P O R A T I O N		
DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

Data Extension/Compare (DEC) Control Register

When Bits 15-12 are set to A, Data Extension/Compare is selected (see Figure 3-28d) and the following applies to Bits 7-2:

Packed Data/ Search Enable   Bit 2 = 0 is normal. Bit 2 = 1 enables use of packed data. When in an operation involving read, packed data is computed from the source. Packed Data is defined as "the screen data ORed with the complement of the bitplane read mask." If the result is all 1, then 1 is extracted, otherwise 0 is extracted per pixel. When write operation is selected, PWGA-1 goes into a special search and fill mode. The screen data is read and if the packed data extracted is 0, write operation is suspended. When a packed data "1" is encountered, write operation is enabled until the next "1". This mode is used to detect the boundary of a polygon for fill operation.

Data Compare   Bits 5-3 specify data comparison parameters.

Data Extension   Bits 6 and 7 specify data extension, mix type, and extension sources.

3-24

WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0							0	0

A — Data extension — Data compare — Packed Data/Search Enable

2	Packed Data		Use
1	Enabled	Read	Read packed data
		Write	Search and fill mode
0	No	Read/Write	Normal

	Data Extension	Mix Operation	Use
7 6	• Bit pattern from the following sources	• Color sources selected by Bit 5, 6, of BAE8h	
0 0	Bit pattern = always 1	Bit 6=0, Bit 5=1 (BAE8h)	Regular
0 1	Pixel position Mix Control BEE8-8,9	Color Source & Foreground Mix (FMX)	Limited use: certain textures horizontal line
1 0	CPU pixel data	Data=1 → Background Color (BGC) & Background Mix (BMX)	CPU 10-bit pattern image transfer to display memory
1 1	Display memory used to display packed data* bit pattern	Data=0 →	BITBLT across the plane or from 1 bit-plane to FGC and BGC through all planes
1 1	Packed data* same as above	Bit 6=1, Bit 5=0 (BAE8h) Data=1 → CPU data & FMX Data=0 → BGC & BMX	Special marker** mode

*packed data—the screen data is ORed with the complement of the bitplane read mask. If the result is all 1, then 1 is extracted, otherwise 0 is extracted per pixel.
**marker—special BITBLT mode used for multi-color marker. A 10 pattern is stored in display memory. During BITBLT, if display memory data=1, CPU data is used. If data=0, background color is used.

Bits 3–5	Comparison Type
0	False (always draw)
1	True (never draw)
2	Plane data >= comparison
3	Plane data < comparison
4	Plane data <> comparison
5	Plane data = comparison
6	Plane data <= comparison
7	Plane data > comparison

Figure 3-28d. Multifunction Control Register (BEE8-A Write Only)

3-25

Image Read/Write (IRW) Register

The IRW Register at address E2E8h specifies the read/write port for image transfer. For across the plane image transfer, read/write data is determined by nibble boundary on the screen. The starting point will fall on the first nibble group. For word mode, two nibbles of data can be transferred for each read/write (see Figure 3-29). For through the plane image transfer, two pixels can be transferred for each read/write operation in word mode (see Figure 3-30).

For Pixel Read operation across the plane:

$$bit\ value = \prod_{i=1}^{n} (P_i + \overline{RM}_i)$$

n = maximum bit-plane value

P_i = pixel value of the bit-plane

RM_i = read mask for the i-th bit-plane

For Pixel write operation across the plane:

bit value=0 will write background color
bit value=1 will write foreground color

screen pixel from left to right: 0 1 2 3 4 5 6 7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	pixel 0	pixel 1	pixel 2	pixel 3	U	U	U		pixel 4	pixel 5	pixel 6	pixel 6	U

Pixel Read/Write value
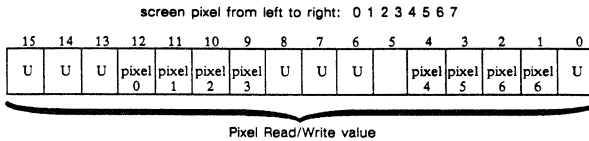
Figure 3-29. Image Read/Write Register (E2E8h Read/Write) Across the Plane (swap = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0	bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0

Pixel 1 if 16-bit Mode Selected   Pixel 2
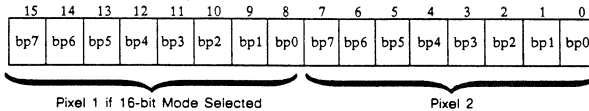
Figure 3-30. Image Read/Write Register (E2E8h Read/Write) through the Plane (swap = 0)

3-26

Status

There are three status registers that can be read to acquire information; the Interrupt Status (IS) register at address 42E8h, and the FIFO Status (FS) Register at address 9AE8h, and the Video Status (VS) register at address O2E8h.

Interrupt Status (IS) Register

The IS Register provides interrupt status, monitor ID, and plane size (see Figure 3-31).

Vsync   Bit 0 indicates a vertical sync interrupt when set to 1.

GE Busy   Bit 1 indicates GE busy when set to 1.

FIFO Overflow   Bit 2 indicates FIFO overflow when set to 1.

FIFO Empty   Bit 3 indicates a FIFO empty when set to 1.

Monitor ID   Bits 4–6 indicate the monitor type being driven by the PWGA-1 or 8514/A.

Plane Size   Bit 7 indicates a 4-bit plane when set to 0 or an 8-bit plane when set to 1.
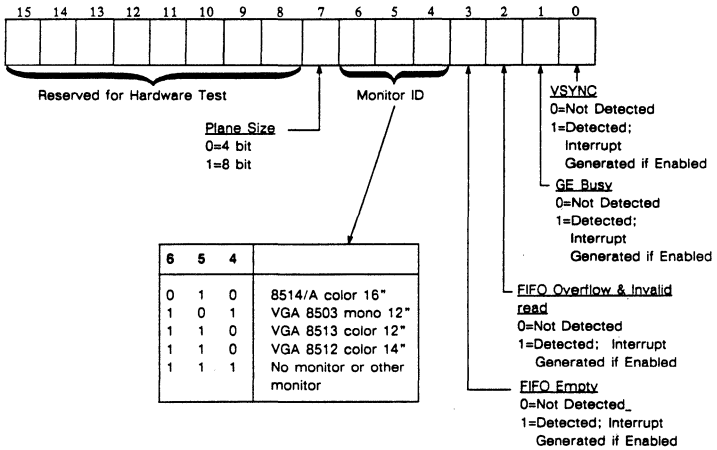
Figure 3-31. Interrupt Status Register (42E8h Read Only)

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WESTERN DIGITAL
CORPORATION

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

FIFO Status (FS) Register

The FS Register provides FIFO status information, PC read data status, and hardware busy status (see Figure 3-32).

FIFO Occupied Bits 7-0 of the FS Register indicate data status of the FIFO (i.e., a 1 in Bit 2 indicates that the third entry of the input FIFO is occupied by data).

Data Available Bit 8 indicates that PC read data is available when set to 1 and not taken when set to 0.

Hrdwr Busy Bit 9 indicates that the hardware is busy when set to 1 and not busy when set to 0.
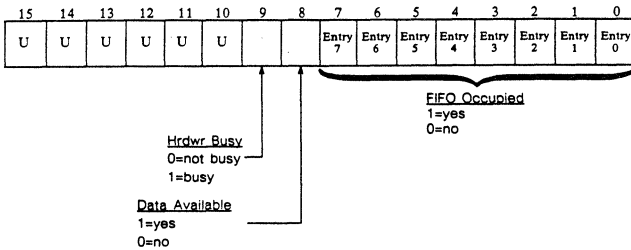
Figure 3-32. FIFO Status Register (9AE8h Read Only)

Video Status (VS) Register

(See Figure 3-33). The VS Register provides video status information.

Bit 1 : vertical sync
VGA mode : 1.28 ms-positive polarity
640x480 mode : 16.8 ms-negative polarity
1024x768 mode : 11.6 ms-positive polarity
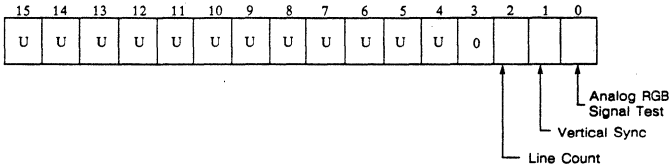
Figure 3-33. Video Status Register (02E8h Read Only)

3-28

93-000032-00

Table 3-4 illustrates how the addresses are decoded for 8514/A compatible registers. The left most column gives the hexadecimal value of address bits 15–12, and the top row shows the value of the rest of the twelve address bits. For example, the read address a2e8 (hex) is decoded as e2e8 under the "2e8' column at the a–th row. This also means an I/O read from address a2e8 is the same as if reading from address e2e8, the IRW register. Address decoding for read is different from that for write.

Table 3-4. Address Decoding tables for 8514/A Compatible Registers

Address Decoding Table for Read

Bits 15–12/11–0	2e8	6e8	ae8	ee8h
0	2e8	2e8	2e8	2e8
1	2e8	2e8	2e8	2e8
2	2e8	2e8	2e8	2e8
3	2e8	2e8	2e8	2e8
4	42e8	42e8	42e8	42e8
5	42e8	42e8	42e8	42e8
6	42e8	42e8	42e8	42e8
7	42e8	42e8	42e8	42e8
8	82e8	86e8	0*	0*
9	92e8	0*	9ae8	0*
a	e2e8	e2e8	0*	0*
b	0*	0*	0*	0*
c	82e8	86e8	0*	0*
d	92e8	0*	9ae8	0*
e	e2e8	e2e8	0*	0*
f	0*	0*	0*	0*

* A value of zero will be read

Address Decoding Table for Write

Bits 15–12/11–0	2e8	6e8	ae8	ee8h
0	2e8	6e8	ae8	ee8
1	12e8	16e8	1ae8	1ee8
2	22e8	X	X	X
3	X	X	X	X
4	42e8	46e8	4ae8	X
5	42e8	46e8	4ae8	X
6	42e8	46e8	4ae8	X
7	42e8	46e8	4ae8	X
8	82e8	86e8	8ae8	8ee8
9	92e8	96e8	9ae8	9ee8
a	a2e8	a6e8	aae8	aee8
b	b2e8	b6e8	bae8	bee8
c	82e8	86e8	8ae8	8ee8
d	92e8	96e8	9ae8	9ee8
e	a2e8	a6e8	aae8	aee8
f	b2e8	b6e8	bae8	bee8

When in wait CPU data mode and graphic engine is busy, register a2e8h, a6e8h, e2e8h, and e6e8h are the same as e2e8.

SOFTWARE INTERFACE EXTENSIONS

Suitable CPU Adapter Interface software (AI), such as the Western Digital Adapter Interface (WDAI) can make use of the PWGA-1's advanced capabilities by invoking "Western Digital Enhanced Mode" on a short-term basis, as explained later.

There are two consequences to this software interface design. First, a PWGA-1-based board can be inserted into a system with no change in software, and it will function as a faster 8514/A. Second, it provides for performance enhancement for custom software.

In order to minimize future register conflict, all functions for Western Digital Enhanced Mode are implemented using one register address, 96E8h.

A dummy IO Read at address 28E9h must precede any access to 96E8h for Western Digital Enhanced Mode. Under 8514/A emulation mode, 96E8h is write only register for Rectangle Width.

Extended Register Operation

To identify the PWGA-1 chip set, see Figure 3-34. To escape to Western Digital Enhanced Mode, the AI should execute a byte read of I/O address 28E9h. (The only purpose of the byte read is to perform the escape; the PWGA-1 does not return any data.) This operation is a no-op for the IBM 8514/A, since it involves a write-only register, which furthermore does not respond to any access to an odd-numbered byte address. This operation will tag the next register access through a special bit in the FIFO. FIFO is fully functional in Western Digital Enhanced Mode.

After escaping to Western Digital Enhanced Mode, the PWGA-1 will automatically reset itself back to 8514/A emulation mode in one of these four circumstances:

1. If, as its next board access immediately after the escape, the AI reads the Western Digital Status Register (I/O address 96E8h).
2. If, as its next board access immediately after the escape, the AI writes to one of the six Western Digital Control Registers, or to the Rectangle Width Register (I/O address 96E8h).
3. If, as its next board access immediately after an escape, the AI writes to either I/O address 82E8 (register name in 8514/A Emulation

Mode: Current Y Position Register) or I/O address 8AE8 (register name in 8514/A Emulation Mode: Copy Y Destination/Incr 1 Register).
4. When, having performed an I/O read or write other than the ones listed above, the AI executes a command (by writing to the Drawing Command Register, I/O address 9AE8).

The reasoning behind the first two cases is clear: the AI programmer is spared from having to remember to take explicit action to release Western Digital Enhanced Mode after performing a single, discrete action that applies to a Western Digital enhancement.
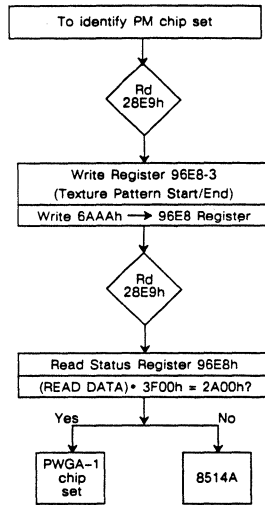
Figure 3-34. Method of Identifying PWGA-1 Chip Set

3-30

The purpose of the second two, however, deserves explanation. Western Digital enhancements simplify and speed line drawing commands in two ways: First, line drawing parameters are simpler, in that the AI needs to specify only the pixel coordinates of the line's end point, rather than the tediously calculated parameters used by the 8514/A. Therefore, the PWGA-1 needs to be in Western Digital Enhanced Mode to "know" that the write into register 8AE8 contains the Y ending point parameter, in preparation for line-drawing command (case 4). Second, in 640x480 resolution, the PWGA-1 can, through Western Digital Enhanced Mode, make use of a much sim-

pler Y-coordinate format than is required by the 8514/A, and therefore must be "told," by being in Western Digital Enhanced Mode, that this simpler format is being written to one of the Y-coordinate registers (82E8 or 8AE8, case 3 above). The drawing parameters are defined in this chapter in "Enhanced Solid Line Drawing." See Figures 3-35a and 3-35b.

The same system I/O address (96E8) is used to access the Western Digital Status Register, and all six of the Western Digital Control Registers. In 8514/A Emulation Mode, this address is that of the Rectangle Width Register.
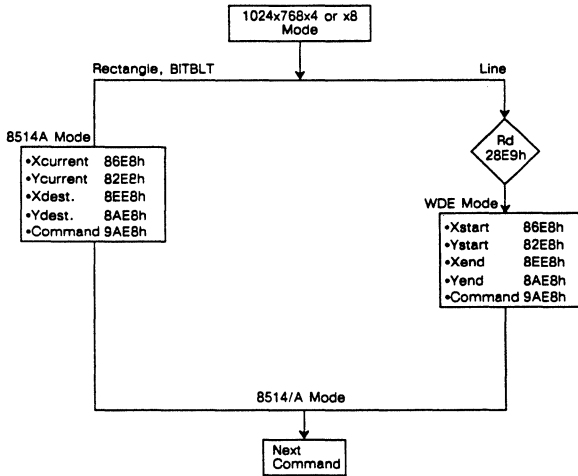
Figure 3-35a. Western Digital Enhanced (WDE) Mode Usage in 1024x768 Resolution

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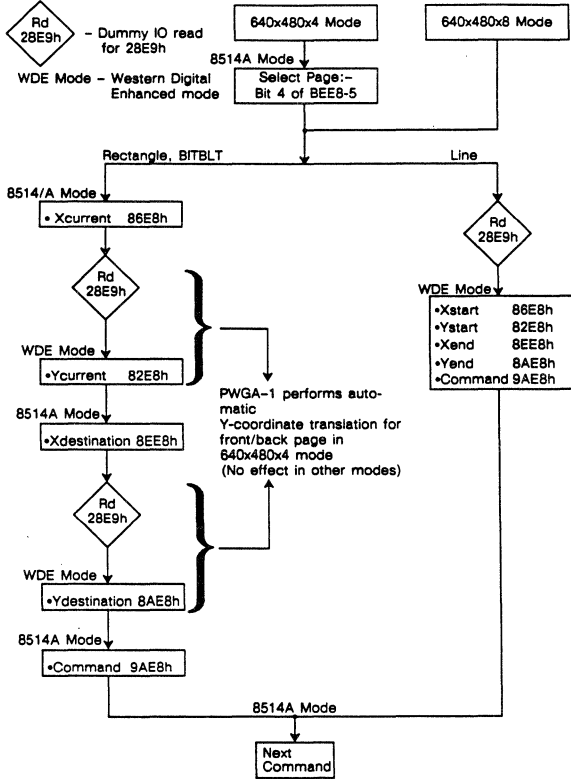
Figure 3-35b. Western Digital Enhanced Mode Usage in 640x480 Resolution

A 16-bit *read* of this address, 96E8, yields the contents of the Western Digital Status Register (see Figure 3-36). Note that in 8514/A Emulation Mode, 96E8 is a write-only register.

VRAM Type	When Bit 0 is set to 0, it indicates 64Kx4 bit VRAM chip type; when set to 1, it indicates 256Kx4 bit VRAM chip type.
# of VRAM Chips	Bits 2 and 1 indicate the number of VRAM chips of the type indicated in Bit 0.
Max Res	Bit 3 indicates the maximum resolution permitted by the VRAM design. When set to 0, it indicates 1024x768; when set to 1, it indicates 1280x1024.

Pal Write	Bit 4 indicates whether a palette write is pending. When set to 0, a palette write is not pending; when set to 1, a palette write is pending.
DAC Type used	Bit 5 indicates whether the DAC used is 6 bit only or 6 bit and 8 bit switchable. The 6-/8- bit DAC allows compatibility at 6 bit/color to 8514A and a large 8-bit/color palette that requires special programming.
Current Texture Pattern Position	Bits 13–8 indicate the current texture pattern position described in "Textured Line Drawing" in this chapter.
Monitor Selection Information	Used by software to read jumper selectable monitor types.
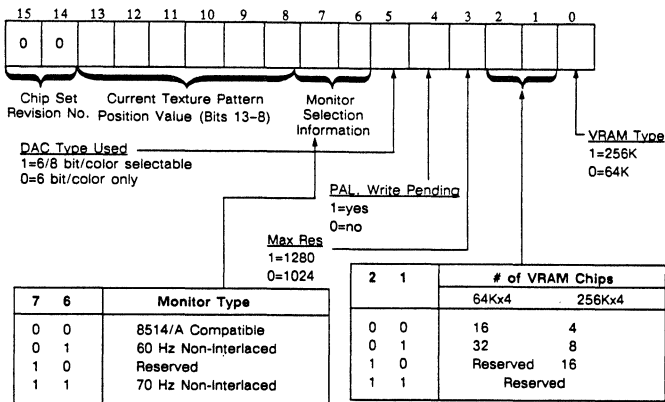
Figure 3-36. Western Digital Status Register (96E8, Western Digital Enhanced Mode, Read Only)

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In Western Digital Enhanced Mode, when a 16-bit *write* is made to address 96E8, the PWGA–1 interprets the high 3 bits as a selection of one of six Western Digital Control Register destinations for the lower 13 bits of data (see Figure 3-37). In this sense, address 96E8 can be thought of as a "gateway" for writes to the six Western Digital Control Registers, and the notations 96E8-1, 96E8-2, ..., 96E8-7 are used to refer to those registers. Note also that this design provides "double insurance" against accidental 8514/A-mode access to these registers: first, they can be accessed only after escaping to Western Digital Enhanced Mode; second, the rectangle width parameter should never be so large as to involve 1-bits in the high three bit positions of the 16-bit

data (and in fact, "96E8-0" leads to the "real" rectangle width register).

When Bits 15–13 are set to 3, Bits 11–6 specify the texture pattern ending position and Bits 5–0 specify the texture pattern starting position within the 48 bits available in the four texture pattern registers (see "Textured Line Drawing" in this chapter). Bit 12 is unused.

Figure 3-38 defines the Western Digital Enhanced Mode Register (i.e., Bits 12–0 of 96E8 when Bits 15–13=001). All the control fields in this register are one-bit mode controls; they select between two alternate modes, and the selected mode remains in effect through all future operations until the AI changes it by inverting the associated control bit.

Figure 3-37. Western Digital Control Registers (96E8, Western Digital Enhanced Mode, Write Only)

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Pixel Depth	Bit 0 specifies the number of bit-planes to be used in all operations. 4 bit-planes are specified when set to 0 and 8 bit-planes are specified when set to 1.
Page Select Draw	Bit 1 specifies screen page selection for drawing (if the VRAM supports two screen pages at the current resolution). Page 1 is selected when set to 0 and page 2 is selected when set to 1. Note that the page-select controls provide a simple mechanism for drawing "in the background," so that the user can instantly replace one screen image with another.
Page Select View	Bit 2 specifies screen page selection for viewing (source of screen refresh). Page 1 is selected when set to 0 and page 2 is selected when set to 1. Note that the page-select controls provide a simple mechanism for drawing "in the background," so that the user can instantly replace one screen image with another.
Mode Extension	Bit 3 in conjunction with Bit 2 of Register 4AE8 are used to select different resolutions. Bit 3=0 is the default for 8514A resolution modes (i.e., 1024x768 and 640x480).
DAC Palette Selection	Bit 6 is used only if the board has a 8/6- bit/color switchable DAC (see Western Digital Status Register). Bit 6=1 selects 8-bit/color mode and bit

	6=0 selects 6-bit/color mode (default).
Texture Mode	Bit 5 specifies Western Digital textured line mode (see "Textured Line Drawing" in this chapter). Setting this bit to 1 enables this mode and a 0 clears the mode. For proper execution, set BEE8_A: Bit 7=0 and Bit 6=1. Also Bit 6,5 of BAE8=01.
Flicker-Free Mode	Bit 4 specifies flicker-free palette loading mode control (see "Flicker-Free Palette Loading" in this chapter). Setting this bit to 1 enables this mode and a 0 clears the mode.
Standard Video Registers Enable	Bit 9 controls the programming of the standard video registers.
Alternate Video Registers Enable	Bit 10 controls the programming of the Alternate video registers (PWGA–1's extended feature).
Monitor Type and Vertical Refresh Frequency	Bits 8–7 combined with the mode extension bit and 8514A mode bit (Bit 2 of 4AE8) set the CLKSEL values that select the pixel clock frequency (see Table 3-6). Notice that Bit 2 of 4AE8 will automatically select a proper frequency after the control bits are programmed by the BIOS.

Mode Ext.	8514A Mode	Monitor Type (Bit 8)	Vert. Refresh Freq. (Bit 7)	CLKSEL2–0
0	0	X	0	000, 640x480, 60 Hz
0	0	X	1	100, 640x480, 70 Hz
0	1	0	0	001, 1024x768, 43 Hz
0	1	1	0	011, 1024x768, 60 Hz
0	1	X	1	111, 1024x768, 70 Hz
1	1	X	X	101, 1280x1024

Table 3-5. Monitor Type and Vertical Refresh Frequency Settings

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WESTERN DIGITAL
C O R P O R A T I O N

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

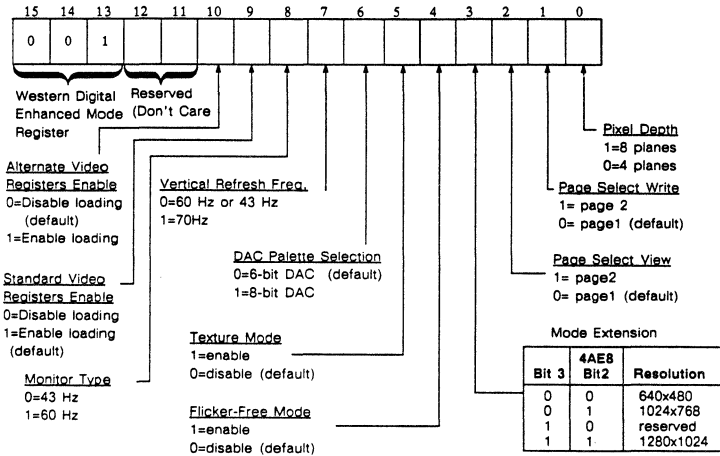| 10	9	Description
0	1	Load Standard Video Timing Registers (default)
1	0	Load Alternate Video Timing Registers
1	1	Load Both Register Sets
0	0	Activate automatic switching between register sets: 4AE8h Bit 2=0 (640x480) selects Standard Register Set Bit 2=1 (1024x768) selects Alternate Register Set

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1													

Western Digital
Enhanced Mode
Register

Reserved
(Don't Care

Alternate Video
Registers Enable
0=Disable loading
   (default)
1=Enable loading

Standard Video
Registers Enable
0=Disable loading
1=Enable loading
   (default)

Monitor Type
0=43 Hz
1=60 Hz

Vertical Refresh Freq.
0=60 Hz or 43 Hz
1=70Hz

DAC Palette Selection
0=6-bit DAC (default)
1=8-bit DAC

Texture Mode
1=enable
0=disable (default)

Flicker-Free Mode
1=enable
0=disable (default)

Pixel Depth
1=8 planes
0=4 planes

Page Select Write
1= page 2
0= page1 (default)

Page Select View
1= page2
0= page1 (default)

Mode Extension

Bit 3	4AE8 Bit2	Resolution
0	0	640x480
0	1	1024x768
1	0	reserved
1	1	1280x1024

Figure 3-38. Western Digital Enhanced Mode Control Register (96E8-1)

3-36

Enhanced Solid-Line Drawing

The following procedure should be used to draw a solid line in Western Digital Enhanced Mode:

1. Escape to Western Digital Enhanced Mode by doing a byte read of I/O address 28E9.

2. Write the X pixel coordinate of the beginning point of the new line to I/O address 86E8 ("Current X Drawing Point" register). If this value has not changed since the last drawing operation (i.e., the new line will start with the X-coordinate of the current drawing point), then instead, the X pixel coordinate of the ending point of the new line should now be written to I/O address 8EE8 ("Ending X" register in Western Digital Enhanced Mode), even if that X coordinate has not changed; the reason is that at least one of the two X-coordinate registers must be loaded prior to loading a Y-coordinate register, to avoid leaving Western Digital Enhanced Mode prematurely.

3. Write the Y pixel coordinate of the beginning point of the new line to I/O address 82E8 ("Current Y Drawing Point" register). If in 640x480 resolution, see below for the format of this coordinate. If this value has not changed since the last drawing operation (i.e., the new line will start with the same Y-coordinate as where the last one ended), this step may be skipped.

4. Unless already done in step 2, write the X pixel coordinate of the ending point of the new line to I/O address 8EE8 ("Ending X" register in Western Digital Enhanced Mode). If this value has not changed since the last drawing operation, this step may be skipped.

5. Write the Y pixel coordinate of the ending point of the new line to I/O address 8AE8 ("Ending Y" register in Western Digital Enhanced Mode). This must to be done to start the line parameter calculation.

6. Conclude by writing the standard line-drawing command to the Command Register, at I/O address 9AE8.

Western Digital Enhanced Mode simplifies the calculation of Y coordinates when using two pages, including the case of 640x480 resolution. In contrast to the 8514/A Emulation Mode, Western Digital Enhanced Mode requires no transformations; the desired page-oriented Y coordinate can be written directly into the Y-coordinate registers. The coordinates will apply to the page selected by the drawing page selection bit in the Western Digital Enhanced Mode Control Register, as described in Figure 3-38.

In both 8514/A Emulation Mode and Western Digital Enhanced Mode, however, the user must be aware of pixel coordinate usage with regard to boundaries.

First, under all circumstances, X and Y coordinates wrap around at the 2K boundary; in other words, pixel coordinates are processed as 11-bit values and hence manipulated modulo 2048.

Second, under all circumstances, Y coordinates between 1K and 2K are "lost." (i.e., drawn objects or parts of drawn objects whose Y coordinates are between 1K and 2K are not recorded in VRAM.)

Third, where only one page is available (except for the 1280x1024 case), X coordinates between 1K and 2K are similarly "lost." (See below for 1280x1024.)

Fourth, where two pages are available, first-page X coordinates between 1K and 2K will "intrude" into the second page (modulo 1024), and second-page X coordinates between 1K and 2K will intrude into the first page (modulo 1024). The reason is that when two pages are provided, the 1Kx1K pages are arranged "side by side" in physical memory, with the logical (page-oriented) X coordinate internally processed as a physical X coordinate between 0 and 2K. The intrusion can be avoided by establishing clipping boundaries at the 1K page limit (or less).

Finally, images drawn within a (1Kx1K) page but beyond the screen viewing boundary (1Kx768 or 640x480) are not "lost," and can be copied from their "off-screen" location into the viewing area by a BITBLT operation. In the (single page) case of 1280x1024 resolution, off-screen storage is provided for X coordinates between 1280 and 2K.

3-37

```
15 14 13   12  11 10 9 8 7 6 5 4 3 2 1 0
┌──┬──┬──┬────┬──┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┐
│ 0│ 1│ 1│  R │  │ │ │ │ │ │ │ │ │ │ │ │
└──┴──┴──┴────┴──┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┘
```
Reserved   Ending Bit   Starting Bit
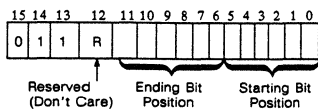(Don't Care)   Position   Position

**Figure 3-39. Texture Pattern Start/End
Register (96E8-3, Western Digital Enhanced
Mode, Write Only)**

Textured-Line Drawing

In Western Digital Enhanced Mode, textured
lines can be drawn directly. After the "texture
pattern" and its pointers have been set up as de-
scribed below, the AI need only turn on the West-
ern Digital textured-line mode control bit, set bits
7, 6 of BEE8-A to 01, set bits 6, 5 of BEA8 to 01
(see Figure 3-38), and then use the same proce-
dure as for solid-line drawing (see "Enhanced
Solid-Line Drawing" in this chapter).

The texture pattern is a string of bits whose 0/1
values are consulted in sequence as the PWGA-1
draws the line, applying the current mix to the
combination of current texture-pattern bit and
current pixel. (For example, a "1" bit in the tex-
ture pattern might be interpreted as an overpaint
instruction.)

The pattern may be up to 48 bits long. Four
Western Digital Control Registers—96E8-4,
96E8-5, 96E8-6, and 96E8-7—are provided for its
storage, as shown in Figure 3-35. (Bit 12 of each
of these registers is reserved.) The pattern must
be defined beginning at Bit 47, but need not con-
tinue to Bit 0; the 6-bit "ending position" field in
Western Digital Control Register 96E8-3 is pro-
vided to specify the number of its last bit (see
Figure 3-39).

The related 6-bit "starting position" field, how-
ever, is used differently: this specifies where (be-
tween Bit 47 and the ending-position bit) the
texture-pattern pointer should be placed at the
beginning of a textured line-drawing operation.
The pointer will be moved in synchronization with
the line-drawing process from that start position
toward the defined ending position (i.e., from
high-order to low-order bits within the texture pat-
tern); after the PWGA-1 uses the texture-pattern
bit at the ending position, it will circulate the

pointer back, not to the specified starting position,
but to Bit 47, and then repeat the process.

After the line is complete, the PWGA-1 will
place the current position of the texture-pattern
pointer into the appropriate field within the West-
ern Digital Status Register (see Figure 3-34),
where it may be read by the AI. If the user does
not store a new value into the starting position
field, then in its next textured-line-drawing opera-
tion, the PWGA-1 will use the current pointer po-
sition from the status register. The chief purpose
of this feature is convenience in allowing the user
to automatically continue a texture pattern from
one line to the next without needing to do an ex-
plicit read and write of the pointer position; for
example, a dashed line will properly turn a corner
without user concern for the texture pattern point-
er.

Note that after board reset, all texture controls,
including current position, are undefined, and
must be initialized by the AI.

Flicker-Free Palette Loading

When using the IBM 8514/A, the CPU must wait
for vertical screen refresh before reloading its
color palette. In a high resolution design, how-
ever, especially with a non-interlaced monitor, the
vertical retrace time (typically less than 600 mi-
croseconds) may not be long enough to program
all 256 color entries.

When the Western Digital flicker-free option is
incorporated into the design of a PWGA-1-based
board ("Video DAC and Interface Subsystem" in
Chapter 2), the PWGA-1 can accept palette
writes from the CPU at any time, but will buffer
them in the DSP until horizontal retrace time;
during horizontal flyback, it will write them to the
DAC's palette, avoiding flicker.

Note that in VGA pass-through mode, any VGA
palette-loading operation also loads the DAC on
the 8514/A (and hence will do the same on a
PWGA-1-based board). Flicker-free program-
ming does not apply in VGA pass-through mode.

Flicker-free mode is enabled by setting Bit 4 of
the Western Digital Enhanced Mode Control Reg-
ister, shown in Figure 3-36. When sending color
data to the board, however, the AI must monitor
Bit 4 of the Western Digital Status Register, shown
in Figure 3-34; if set, this bit indicates that a pal-
ette write is pending, and no further palette color

data should be sent until the PWGA-1 clears the bit. When clear, the AI can then send three bytes, representing the contents of one of the 256 entries in the palette.

Other AI accesses of the DAC, including reading color values, are independent of the flicker-free design, and should emulate 8514/A operations.

Table 3-6. IBM 8514/A Compatible Registers

I/O Address	Read/Write	Function
O2EA/03C6	R/W	Look Up Table Mask
O2EB/03C7	W	Read Color Index
O2EB/03C7	R	DAC State
O2EC/03C8	R/W	Color Index
O2ED/03C9	R/W	RGB Color Value
02E8	R	Video Control Status
02E8	W	Horizontal Total
06E8	W	Horizontal Active
0AE8	W	Horizontal Sync Position
0EE8	W	Horizontal Sync Width/Polarity
12E8	W	Vertical Total
16E8	W	Vertical Active
1AE8	W	Vertical Sync Position
1EE8	W	Vertical Sync Width/Polarity
22E8	W	Display Control
42E8	W	Interrupt Status
42E8	W	Interrupt/FIFO/Reset Control
46E8	W	EPROM Selection
4AE8	W	Graphics Mode Control
82E8	R/W	Current Y Position
86E8	R/W	Current X Position
8AE8	W	Copy Y Destination/Incr 1 Line
8EE8	W	Copy X Destination/Incr 2 Line
92E8	R/W	Delta Line
96E8	W	Rectangle Width/Max for Line
9AE8	R	FIFO Status
9AE8	W	Drawing Command Control
9EE8	W	Short Stroke Vector Control
A2E8	W	Background Color
A6E8	W	Foreground Color
AAE8	W	Bit-Plane Write Mask
AEE8	W	Bit-Plane Read Mask
B2E8	W	Comparison Color
B6E8	W	Background Mix
BAE8	W	Foreground Mix
BEE8		Multifunction Control
BEE8 (0)	W	Rectangle Height
BEE8 (1)	W	Clipping Window Top Limit

3-39

Table 3-6. IBM 8514/A Compatible Registers (cont.)

I/O Address	Read/Write	Function
BEE8 (2)	W	Clipping Window Left Limit
BEE8 (3)	W	Clipping Window Bottom Limit
BEE8 (4)	W	Clipping Window Right Limit
BEE8 (5)	W	Memory Configuration
BEE8 (8)	W	Pixel Position Mix Control—Low
BEE8 (9)	W	Pixel Position Mix Control—High
BEE8 (A)	W	Data Extension/Compare Control
E2E8	R/W	Image Read/Write

Table 3-7. PWGA-1 Enhanced Registers

I/O Address	Read/Write	Function
28E9	R	Dummy Read/Enable for 96E8
36E8	W	EPROM Select—AT Bus Only
8AE8	W	Ending X Point for Line
8EE8	W	Ending Y Point for Line
96E8	R	Western Digital Status
96E8 (1)	W	Western Digital Enhanced Mode
96E8 (3)	W	Texture Pattern Start End
96E8 (4)	W	Texture Pattern 11–0
96E8 (5)	W	Texture Pattern 23–12
96E8 (6)	W	Texture Pattern 35–24
96E8 (7)	W	Texture Pattern 47–36

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A

Pin Description

Table 1. Pixel Address Manager Pin Description

Name	Pin #	Type	Description
A19–A0 SA19–SA0	82–71, 69–62	I	Address bits 19 through 0 (MC) Address bits 19 through 0 (AT)
AUP	85	I	Decoding of upper address bits 23–20 (AT) Decoding of upper address bits 23–20 and MADE24 (MC)
D15–D0 SD15–SD0	110–100, 98–94	I/O	Data bits 15 through 0 (MC) Data bits 15 through 0 (AT)
–CDDS16 –I/O CS16	55	O	–Card Data Size 16 (MC) –I/O 16-bit Chip Select (AT)
M/–IO –MEMR	57	I	Memory/–Input Output (MC) –Memory Read (AT) Full Memory Address Range
–S0 –MEMW	59	I	–Status Bit 0 (MC) –Memory Write (AT)
–S1 –IOR	58	I	–Status Bit 1 (MC) –I/O Read, –I/O Write (AT)
–CMD –IOW	60	I	–Command (MC) –I/O Write (AT)
CHRESET RESET DRV	52	I	Channel Reset (MC) System Reset (AT)
–IRQ IRQ	88	O	–Interrupt Request (MC) Interrupt Request (AT)
CD CHRDY I/O CHRDY	90	O	Channel Ready (MC) I/O Channel Ready (AT)
–SBHE –SBHE	56	I	–System Byte High Enable (MC) –System Bus High Enable (AT)
–ADL BALE	61	I	–Address Latch (MC) Buffered Address Latch Enable (AT)
–CD SFDBK	89	O	–Card Selected Feedback (MC)
–CD SETUP AEN	86	I	–Card Setup (MC) Address Enable (AT)
–BIOS OE	36	O	–Output Enable for BIOS EPROM (MC & AT)
BIOS A14–A01	54, 53, 49–37	O	BIOS EPROM Address bits 14–0 (MC & AT)
MC/AT	120	I	Select Microchannel (high) or AT Bus (low)
–DBEN	91	O	–Data Bus Enable (MC & AT)
DBDIR	92	O	Data Bus Direction (MC & AT) high –> CPU read, low –> CPU write
ATCLK	84	I	AT Bus System Clock (AT)

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Table 1. Pixel Address Manager Pin Description (cont.)

Name	Pin #	Type	Description
IAD7-IAD0	135-125	I/O	Time-multiplexed Internal Address & Data Bus bits 7-0, this bus is used to load/read control registers and pass/read data for through/across the plane operations.
IADSTAT	124	O	Internal AD Bus Status selects the usage of IAD
-RWCAS	8	O	-Read/Write CAS, the rising edge of this signal is used to latch pixel data
RD/-WR	123	O	Read/-Write control for passing data between PAM and PDM
-AS	122	O	-Address Strobe, rising edge indicates address is valid
-DS	121	O	-Data Strobe indicates data is valid for read/write
RMWE	117	I	Read-Modify-Write Enable
SLC	119	I	Scan Line Clock, for clocking in serial data
SLD	118	I	Scan Line Data, serial data for communicating scan refresh information
SWAP/X2	7	O	Swap the high and low pixel data bus, used by Western Digital Turbo Mode. In all other modes, this signal is the same as pixel address X2.
MDT2-MDT0	5, 4, 3	O	Memory Data Type, field used to tell the PDM chip what type of display memory cycle is being done. Encodings are as follows: MDT2-MDT0 Cycle Type 0 0 0 No Operation 0 0 1 (reserved) 0 1 0 Drive Write Per Bit Mask 0 1 1 Write Cycle 1 0 0 BITBLT Read Source Data first group 1 0 1 BITBLT Read Source Data 1 1 0 Read Destination Data for RSOP first group 1 1 1 Read Destination Data for RSOP
WROE	6	O	WRite Output Enable, enables the pixel data bus in PDM
SCLK	113	I	System Clock (60MHz)
MA7-MA0	19, 16-10	O	Memory Address Lines
LA13	34	O	Line address for C1 and C3 memory chips
LA24	35	O	Line address for C2 and C4 memory chips
-RAS1 - -RAS0	23, 22	O	Memory -RAS strobe
-CAS12, -CAS34	21, 20	O	Memory -CAS strobes
WE7-WE0	31-34	O	Pixels Write Enable Lines, one per pixel
-DT/-OE	32	O	Transfer control and Output Enable
-DACWR (-DACWE)	112	O	-DAC Write (or -WE for BT451/458 DAC), 3-stated

A-2

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Table 1. Pixel Address Manager Pin Description (cont.)

Name	Pin #	Type	Description
-DACRD (-DACRD)	111	O	-DAC Read (or -CE for BT451/458 DAC), tri-stated
DAC8	114	O	Color Value alignment for designs with 8-bit DAC
SELVD	2	I	-DACWR and -DACRD tri-state control, the DAC read and write signals are tri-stated when SELVD is high
VDD	17, 50, 70, 93, 115		Seven +5V power pins
VSS	1, 9, 18, 33, 51, 83, 87, 99, 116		Seven GND pins
Total pin count = 132			

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Table 2. Pixel Data Manager Pin Description

Name	Pin #	Type	Description
IAD7–IAD0	2–9	I/O	Time-multiplexed Internal Address & Data Bus bits 7–0, this bus is used to load/read control registers and pass/read data for through/across the plane operations.
IADSTAT	10	I	Internal AD Bus Status selects the usage of IAD
–RWCAS	126	I	–Read/Write CAS, the rising edge of this signal is used to latch pixel data
RD/–WR	11	I	Read/–Write control for passing data between PAM and PDM
–AS	12	I	–Address Strobe, rising edge indicates address is valid
–DS	13	I	–Data Strobe indicates data is valid for read/write
RMWE	19	O	Read-Modify-Write Enable
SLC	15	O	Scan Line Clock, for clocking in serial data in PDM
SLD/TOUT	16	O	Scan Line Data, serial data for communicating scan refresh information. Under the test mode, it is the test output pin.
SWAP	127	I	Swap the high and low pixel data bus
MDT2–MDT0	129–131	I	Memory Data Type, field used to tell the PDM chip what type of display memory cycle is being done. (same encoding as PAM)
WROE	128	I	WRite Output Enable, enables the pixel data bus in PDM
RESET	40	I	Reset for internal registers and states
SCLK	39	I	60 MHz System Clock
PCLK	68	I	Pixel Clock
PD31–PD0	90–93, 95–98, 100–114, 117–125	I/O	Pixel Data Bus Bits 31–0
VCLK	25	O	Video Clock for DAC, tristate output
HSYNC	33	O	Horizontal Sync, tristate output
VSYNC	34	O	Vertical Sync, tristate output
BLANK	20	O	Video Blank, tristate output. A zero will drive the video output of the DAC to blanking level.
VDATA7–VDATA0	21–24, 27–30	O	Video Data Bits, tristate output
–DACWR (–DACWE)	32	O	–DAC Write (or –WE for BT451/458 DAC), 3-stated
–DACRD (–DACRD)	31	O	–DAC Read (or –CE for BT451/458 DAC), 3-stated
SELVD	132	O	Select PC data bus or VDATA7–VDATA0 for programming color values in flicker free mode
–DACV/TIN	35	I	–DAC Valid, indicates that the RGB analog output of DAC is valid. Under the test mode, it is the TIN signal for internal counter testing.

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Table 2. Pixel Data Manager Pin Description (cont.)

Name	Pin #	Type	Description
MID2-MID0	36-38	I	Monitor ID Bits 2-0
			0 1 0 IBM 8514 (16") display
			1 0 1 IBM 8503 (12") monochrome display
			1 1 0 IBM 8513 (12")/8512 (14") display
			1 1 1 other display
TSEL2, TSEL1, TSEL0			Under the test mode, MDT2-MDT0 select one of the six internal counters for testing. They are renamed as TSEL2-TSEL0, respectively.
CLKSEL2-CLKSEL0	43-45	O	Pixel Clock Select
			0 0 0 640x480 (60Hz) non-interlaced, default
			0 0 1 1024x768 (86Hz) interlaced
			0 1 0 800x600 (60Hz) non-interlaced
			0 1 1 1024x768 (60Hz) non-interlaced
			1 0 0 640x480 (70Hz) non-interlaced
			1 0 1 1280x1024 (60Hz) non-interlaced pixel input clock = 55 MHZ
			1 1 0 800x600 (70Hz) non-interlaced
			1 1 1 1024x768 (70Hz) non-interlacd
-ENVGA	42	O	-Enable VGA Mode

The following pins or signals may have different definitions in various designs. The definitions listed here are for the base 8514A emulation with background integration.

Name	Pin #	Type	Description
SD31-SD0	46-49, 52-67, 71-82	I	Video data shifted in from VRAM
SE12A, SE34A	87, 85	O	Serial Output Enable for VRAM
SE12B, SE34B	86, 84		(support 2 page 1023x768x4 & 1page 1024x768x8)
SC13-SC24	88, 89	O	Serial Data Clock for VRAM
VDD	17, 50, 70, 94, 116		Seven +5V power pins
VSS	1, 14, 18, 26, 41, 51, 69, 83, 99, 115		Eight ground pins

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Table 3. Pin Description for Different Design

This table lists all signals which have different definitions in different designs. These signals are in PDM and are mainly for VRAM and DAC interface. See Application Notes for Details.

Case	1	2	3
Pin #			
87	SE12A	SE12A	SE12A
85	SE34A	SE34A	SE34A
86	SE12B	–	–
84	SE34B	–	–
77	SD5	–	SEL1
88	SC13	SC13	SC13
89	SC24	SC24	SC24
76	SD6	–	LDCLK
25	VCLK	VCLK	VCLK

Case 1:   64Kx4, 1024x768x8, with backend integration

Case 2:   256Kx4, 1024x768x8, with backend integration

Case 3:   256Kx4, 1280x1024x4 or x8, with external backend support

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B

Electrical Specifications

WD95C00 (PAM) I/O ELECTRICAL SPECIFICATIONS

PAM AC Specification

CLK period: 16 ns minimum, 16.7 ns typical.
CLK rise and fall time (0.4V to 2.4V): 2.5 ns maximum.
All outputs rise and fall time (10% to 90%): t.b.d.
Input capacitance: 10 pF maximum.

PAM DC Specification

Absolute maximum ratings:
 Voltages on all imputs and outputs with respects to GND .... -0.3 V to 7.0 V
 Operating ambient temperture .... $0°$ C $\leq$ TA $\leq 65°$ C
 Storage temperature .... $-65°$ C to $150°$ C

DC Characteristics:

	Min	Max	Unit	Condition
Supply voltage (VCC)	4.5	5.5	V	
Input low voltage (VIL)	-0.3	0.8	V	
Input high voltage (VIH)	2.0	VCC	V	
Output low voltage (VOL)		0.4	V	Refer to Table B-1
Output high voltage (VOH)	2.4			Refer to Table B-1
Input leakage current (ILI)		±10	uA	VIN=0 to VCC
Tri-state output leakage current (IOL)		±10	uA	VOUT=0.4 V to VCC
Power supply current (ICC)			mA	

Note1: All inputs have static charge and latch up portection circuits.

Note2: All inputs including bi-directional pads have 20K ohm pull-up resisitors.

B-1

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Table B-1. Output Specifications

Signal Name	IO	IOL (Min) @ 0.4V	IOH (Min) @ 2.4V	Capacitive Loading
D15-0	I/O	1.0 mA	-50 uA	75 pF
-CDDS16	O	2.0 mA	-50 uA	250 PF
-IRQ	O	2.0 mA	-50 uA	250 pF
CHRDY	O	2.0 mA	-50 uA	250 pF
SFDBK	O	2.0 mA	-50 uA	250 pF
-BIOSOE	O	1.0 mA	-50 uA	50 pF
BIOSA14-0	O	1.0 mA	-50 uA	50 pF
-DBEN	O	1.0 mA	-50 uA	50 pF
DBDIR	O	1.0 mA	-50 uA	50 pF
WROE	O	1.0 mA	-50 uA	50 pF
-DACWR	O	1.0 mA	-50 uA	100 pF
-DACRD	O	1.0 mA	-50 uA	100 pF
DAC8	O	0.5 mA	-50 uA	50 pF
-RWCAS	O	1.0 mA	-50 uA	50 pF
IADSTAT	O	1.0 mA	-50 uA	50 pF
IAD7-0	I/O	1.0 mA	-50 uA	50 pF
RD/-WR	O	1.0 mA	-50 uA	50 pF
-AS	O	1.0 mA	-50 uA	50 pF
-DS	O	1.0 mA	-50 uA	50 pF
SWAP	O	1.0 mA	-50 uA	50 pF
MDT2-0	O	1.0 mA	-50 uA	50 pF
MA7-0	O	1.0 mA	-50 uA	130 pF
LA13	O	1.0 mA	-50 uA	80 pF
LA24	O	1.0 mA	-50 uA	80 pF
LA24	O	1.0 mA	-50 uA	100 pF
-RAS1	O	1.0 mA	-50 uA	100 pF
-RAS0	O	1.0 mA	-50 uA	100 pF
-CAS12	O	1.0 mA	-50 uA	100 pF
-CAS34	O	1.0 mA	-50 uA	100 pF
WE7-0	O	1.0 mA	-50 uA	50 pF
-DTOE	O	1.0 mA	-50 uA	160 pF

WD95C01 (PDM) I/O ELECTRICAL SPECIFICATIONS

PAM AC Specification

SCLK period: 16 ns minimum, 16.7 ns typical.
PCLK period: 13.5 ns minimum, 15.4 ns or 22.2 ns typical.
CLK rise and fall time (0.4V to 2.4V): 2.5 ns maximum.
All outputs rise and fall time (10% to 90%): t.b.d.
Input capacitance: 10 pF maximum.

PDM DC Specification

Absolute maximum ratings:
       Voltages on all imputs and outputs with respects to GND .... -0.3 V to 7.0 V
       Operating ambient temperture .... $0°\ C \leq TA \leq 65°\ C$
       Storage temperature .... -65° C to 150° C

DC Characteristics:

	Min	Max	Unit	Condition
Supply voltage (VCC)	4.5	5.5	V	
Input low voltage (VIL)	-0.3	0.8	V	
Input high voltage (VIH)	2.0	VCC	V	
Output low voltage (VOL)		0.4	V	Refer to Table B-2
Output high voltage (VOH)	2.4	VCC		Refer to Table B-2
Input leakage current (ILI)		±10	uA	VIN=0 to VCC
Tri-state output leakage current (IOL)		±10	uA	VOUT=0.4 V to VCC
Power supply current (ICC)		t.b.d.	mA	

Note 1: All inputs have static charge and latch up portection circuits.

Note 2: All inputs including bi-directional pads have 20K ohm pull-up resistors.

B-3

Table B-2. Output Specifications

Pad Names	IO	IOL (Min) @ 0.4V	IOH (Min) @ 2.4V	Capacitive Loading (max)
IAD7–IAD0	I/O	4.20 mA	–50 uA	50
RMWE	O	1.00 mA	–50 uA	50
SLC	O	4.20 mA	–50 uA	50
SLD/TOUT	O	4.20 mA	–50 uA	50
PD31–PD0	I/O	4.20 mA	–50 uA	50
VCLK	O	4.20 mA	–50 uA	30
HSYNC	O	4.20 mA	–50 uA	70
VSYNC	O	4.20 mA	–50 uA	70
BLANK	O	4.20 mA	–50 uA	30
VDATA7–VDATA0	O	4.20 mA	–50 uA	30
–DACWR (–DACWE)	O	4.20 mA	–50 uA	50
–DACRD (–DACRD)	O	4.20 mA	–50 uA	50
SELVD	O	4.20 mA	–50 uA	50
CLKSEL2–CLKSEL0	O	0.80 mA	–50 uA	50
–ENVGA	O	4.80 mA	–50 uA	100
SE12A, SE34A, SE12B, SE34B	O	4.20 mA	–50 uA	70
SC13,SC24	O	4.20 mA	–50 uA	70
SD6,SD5	I/O	4.20 mA	–50 uA	100

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DWG SIZE	DRAWING NUMBER		REV.
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C

TIMING DIAGRAMS

RESET INITIALIZATION TIMING

Table C-1. Reset Initialization Timing Parameter

Symbol	Timing Parameter	Min	Max
t_{RW} *	Reset high period	$20t_c$	
t_{DOC} †	–BIOS OE delay from falling edge of RESET	$40t_c$	
t_{DSTP}*	STRAP DATA valid after falling edge of RESET (hold time)	$4t_c$	
t_{ROEL}†	Initial –BIOS OE low period after RESET	$160t_c$	
t_{BRC}†	Read Cycle Time after RESET	$23t_c$	

* Apply to both PAM and PDM
† Apply to PAM only

C-1
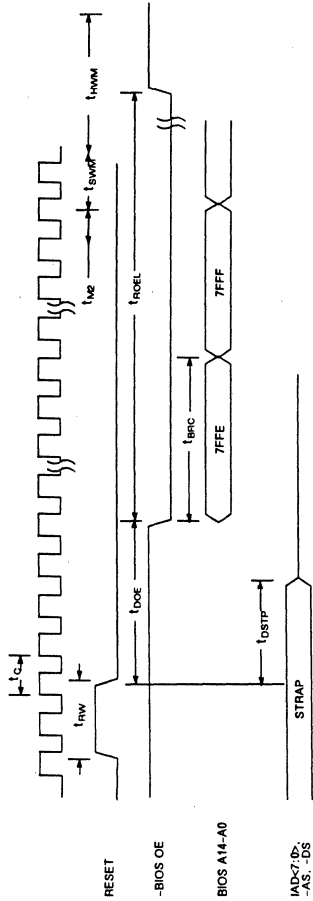
Figure C-1. Reset Initialization Timing Diagram

C-2

MICRO CHANNEL INTERFACE TIMING

This section provides the specification for critical timing parameters for Micro Channel interface. Timing parameters related to PAM are listed separately.

Setup Cycle

This occurs during system configuration following reset. −CD SETUP is pulled low by writing to I/O Port 96H. Then Adapter ID is read from I/O registers 100H and 101H using default cycles. Next an asynchronous extended I/O write cycle is performed to 102H.
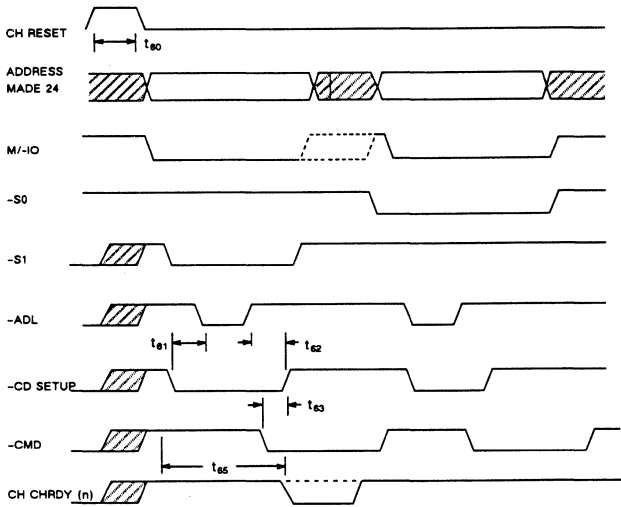
Figure C-2. Setup Cycle Timing Diagram

C-3

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Table C-2. Setup Cycle Timing (Refer to the Micro Channel Spec)

Timing Parameter	Min/Max
CHRESET active (high) pulse width	100/ – ns
–CD SETUP (n) active (low) to –ADL active (low)	15/ – ns
–CD SETUP (n) hold from –ADL inactive (high)	25/ – ns
–CD SETUP (n) hold from –CMD active (low)	30/ – ns
CD CHRDY (n) inactive (low) form –CD SETUP (n) active	–/100 ns

Default Cycle

Reading of POS registers and reading/writing of DAC registers are done using this cycle.
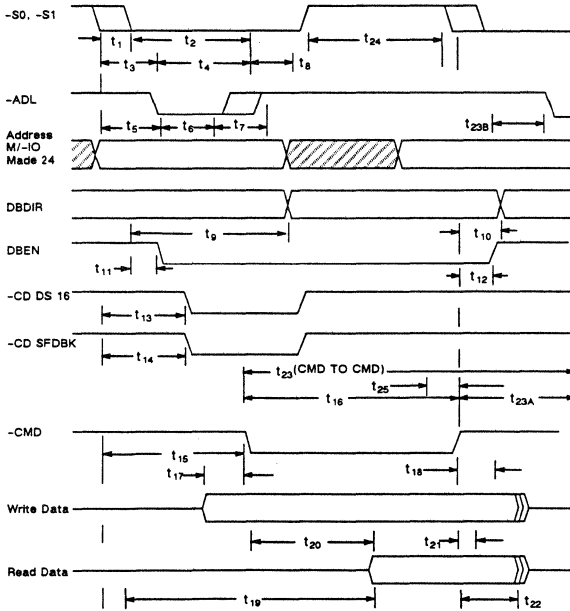
Figure C-3. I/O Default Channel Timing Diagram

C-4

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DWG SIZE **A**	DRAWING NUMBER		REV.
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93-000032-00

Table C-3. I/O and Memory Default Cycle (200 nanosecond minimum)
(Min/Max Parameters are from the Micro Channel Spec)

	Timing Parameter	Min/Max	PAM
t_1	Status active (low) from ADDRESS, M/–IO, valid	10/ – ns	
t_2	–CMD active (low) from Status active (low)	55/ – ns	
t_3	–ADL active (low) from ADDRESS, M/IO, valid	45/ – ns	
t_4	–ADL active (low) to –CMD active (low)	40/ – ns	
t_5	–ADL active (low) from Status active (low)	12/ – ns	
t_6	–ADL pulse width	40/ – ns	
t_7	Status hold from –ADL inactive (high)	25/ – ns	
t_8	ADDRESS, M/–IO, hold from –ADL inactive	15/ – ns	
t_9	DBDIR change from status active (low)	–/–	–/40 ns
t_{10}	DBDIR change from –CMD high	–/–	–/40 ns
t_{11}	–DBEN change from –S0, S1	–/–	–/35 ns
t_{12}	–DBEN change from –CMD high	–/–	–/30 ns
t_{13}	–CD DS 16 active (n) (low) from ADDRESS, M/–IO valid	–/ 55 ns	
t_{14}	–CD SFDBK active (low) from ADDRESS, M/–IO valid	–/ 60 ns	
t_{15}	–CMD active (low) from Address valid	85/ – ns	
t_{16}	–CMD pulse width	90/ – ns	
t_{17}	Write data setup to –CMD active (low)	0/ – ns	
t_{18}	Write data hold from –CMD inactive (high)	30/ – ns	
t_{19}	Status to Read Data valid (Access Time)	–/125 ns	
t_{20}	Read data valid from –CMD active (low)	–/60 ns	
t_{21}	Read data hold from –CMD inactive (high)	0/ – ns	
t_{22}	Read data bus tri-state from –CMD inactive (high)	–/40 ns	
t_{23}	–CMD active to next –CMD active	190/ – ns	
t_{23A}	–CMD inactive to next –CMD active	80/ – ns	
t_{23B}	–CMD inactive to next –ADL active	40/ – ns	
t_{24}	Next Status active (low) from Status inactive	30/ – ns	
t_{25}	Next Status active (low) to –CMD inactive	–/ 20 ns	

Asynchronous Extended Cycle (General Case)

Access to all registers in PWGA–1 or the BIOS EPROM uses this cycle. An Asynchronous Extended cycle occurs when the chip set releases CD CHRDY asychronously. However, the chip set provides the Read data within the specified time form CD CHRDY release. The timing sequence is illustrated by the Figure C-4. Figure C-4 shows only the parameters additional to the default cycle. All other parameters are the same as the default cycle.
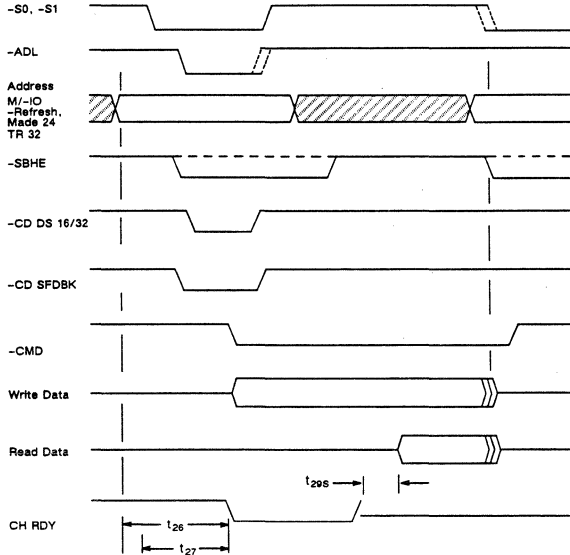
C-5

Figure C-4. Asynchronous Extended Cycle Timing Diagram

Table C-4. Asynchronous Extended Cycle Timing
(Min/Max Parameters are from the Micro Channel Spec)

	Timing Parameter	Min/Max
t_{26}	CD CHRDY (n) inactive (low) from ADDRESS valid	-/60 ns
t_{27}	CD CHRDY (n) inactive (low) from Status active	0/30 ns
t_{29S}	Read data valid from CD CHRDY (n) active (high)	-/60 ns

C-6

16-BIT AT BUS INTERFACE TIMING

I/O Memory Extended Read Cycle

All registers inside PWGA-1 are read using this cycle.
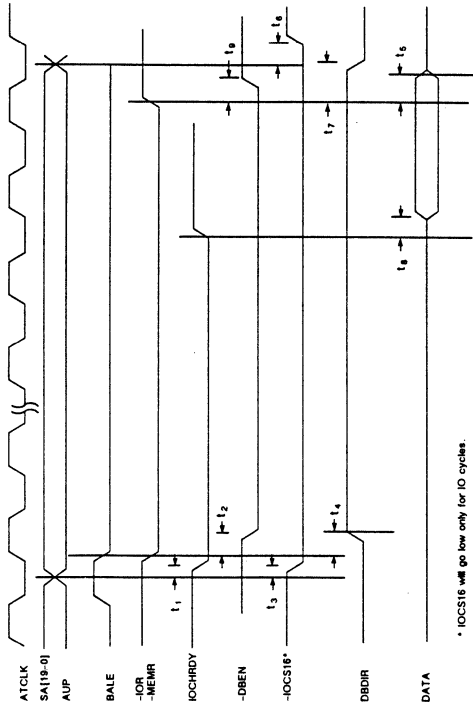
Figure C-5. AT Bus IO/Memory Timing Diagram

* IOCS16 will go low only for IO cycles.

C-7

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I/O Extended Write Cycle

All registers inside PWGA-1 are written using this cycle.
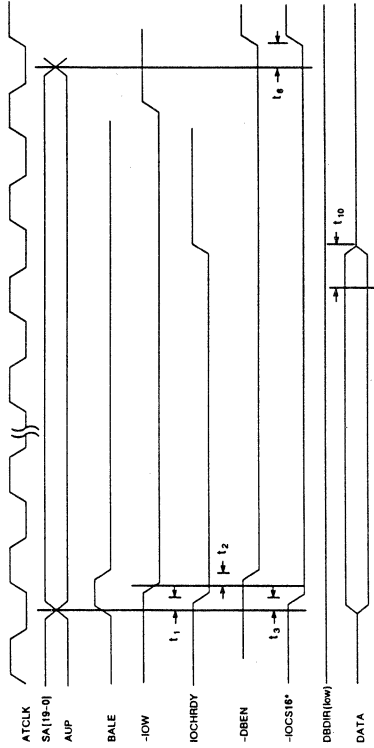
Figure C-6. AT Bus I/O Write Cycle (>1 Wait States) Timing Diagram

C-8

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I/O Read Cycle

This cycle is used only for DAC access.
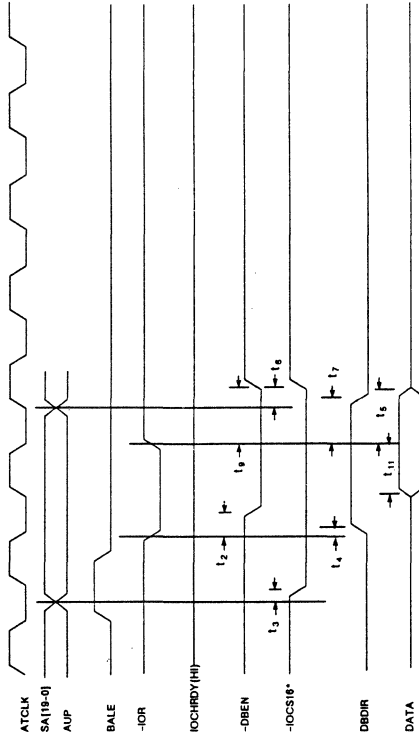
Figure C-7. AT Bus / I/O Read (1 Wait State) Timing Diagram

C-9

I/O Write Cycle

This cycle is used only for DAC access (flicker-free mode disabled).
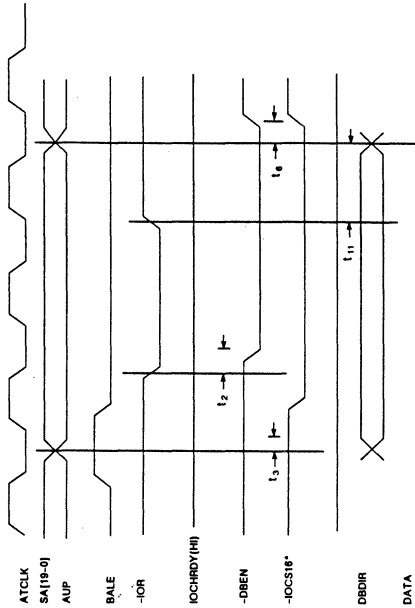
Figure C-8. AT Bus / I/O Write (1 Wait State) Timing Diagram

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Table C-5. AT Response Time

Symbol	Timing Parameter	Min	Max
t_1	SA[19-0] valid to IOCHRDY (BALE is high)	–	65*
t_2	–IOR, –MEMR, –IOW valid to –DBEN low	35	–
t_3	SA[19-0] valid to –IO CS16	–	55
t_4	DBDIR delay from –IOR, –MEMR	–	40
t_5	–IOR invalid to data valid	40	–
t_6	SA[19-0] invalid to –IO CS16	–	55
t_7	–IOR high to DBDIR low	–	40
t_8	IOCHRDY high to valid read data	–	55
t_9	–IOW, –MEMR, –IOR high to DBENN high	–	30
t_{10}	Write data hold from IOCHRDY	0	–
t_{11}	Read data setup to –IOR high	40	–

*If no command (MEMR, IOR, IOW) becomes active IOCHRDY will time out and go high after four (4) ATCLK cycles.

VRAM MEMORY INTERFACE TIMING

Page mode cycle will follow the standard entry cycle if the row address of subsequent access is the same. Page mode terminates, if operations are completed, a memory refresh request is pending, different row address in next access or RAS low width = 50.

C-11

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DWG SIZE **A**	DRAWING NUMBER		REV.
SCALE		SHT	OF

93-000032-00

VRAM Read Cycle

Figure C-9. VRAM Read Cycle Timing Diagram

Table C-6. VRAM Read Cycle

Parameter	Symbol	Min	Max
		**	
Random read/write cycle time	t_{RC}	$(12+RPW+EW+RH)t_C$	–
Page mode cycle time	t_{PC}	$(5+CPW+PW)t_C$	–
–RAS precharge time	t_{RP}	$(5+RPW)t_C$	–
–CAS precharge time	t_{CP}	$(2+CPW)t_C$	–
–RAS pulse width	t_{RAS}	$(7+EW+RH)t_C$	$500t_C$
–RAS to –CAS delay	t_{RCD}	$(4+RH)t_C$	–
–CAS pulse width	t_{CAS}	$(3+EW)t_C*$	–
Row address setup	t_{ASR}	$2t_C$	–
Row address hold	t_{RAH}	$(2+RH)t_C$	–
Column address setup	t_{ASC}	$2t_C$	–
Column address hold	t_{CAH}	$(3+EW)t_C*$	–
–CAS high to –RAS precharge time	t_{CRP}	$(5+RPW)t_C$	–
–OE low to read data valid	t_{OEA}	–	$(2+EW)t_C$
–OE low to read data valid for page mode	t_{POEA}	–	$(3+PW)t_C$
Access time from –RAS	t_{RAC}	$(6+RH+EW)t_C$	–
Access time from –CAS	t_{CAC}	$(2+EW)t_C$	–
Read data setup time	t_s	32	–
Read data hold time	t_h	0	–

*under page mode cycle, EW = PW

** RPW, EW, CPW, PW and RH are all memory wait control parameters. Their definitions are given in Fig 2-10b.

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VRAM Write Cycle

Page mode cycle will follow the standard entry cycle if the row address of subsequent access is the same. Page mode terminates if operations are complete, a memory refresh request is pending, different row address in next access or RAS low width = 50.

Figure C-10. VRAM Write Cycle Timing Diagram

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Table C-7. VRAM Write Cycle

Parameter	Symbol	Min	Max
Write Command to –RAS lead time	t_{RWL}	$(3+EW)t_c$ *	–
Write Command to –CAS lead time	t_{CWL}	$(3+EW)t_c$ *	–
Setup time	t_{RCS}	t_c	–
Write command pulse width	t_{WP}	$(3+EW)t_c$ *	–
Write Command to –CAS lead time	t_{CW}	$(3+EW)t_c$ *	–
Data-in setup time	t_{DS}	0	–
Data-in hold time	t_{DH}	$2t_c$	–
Write-per-bit setup time	t_{WBS}	$2t_c$	–
Write-per-bit hold time	t_{WBH}	$(3+RH)t_c$	–
Write bit selection setup time	t_{WS}	$2t_c$	–
Write bit selection hold time	t_{WH}	$(2+RH)t_c$	–

*under page mode cycle, EW = PW

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VRAM Transfer Read Cycle Timing

This cycle happens during retrace time where VRAM serial port is in standby mode.
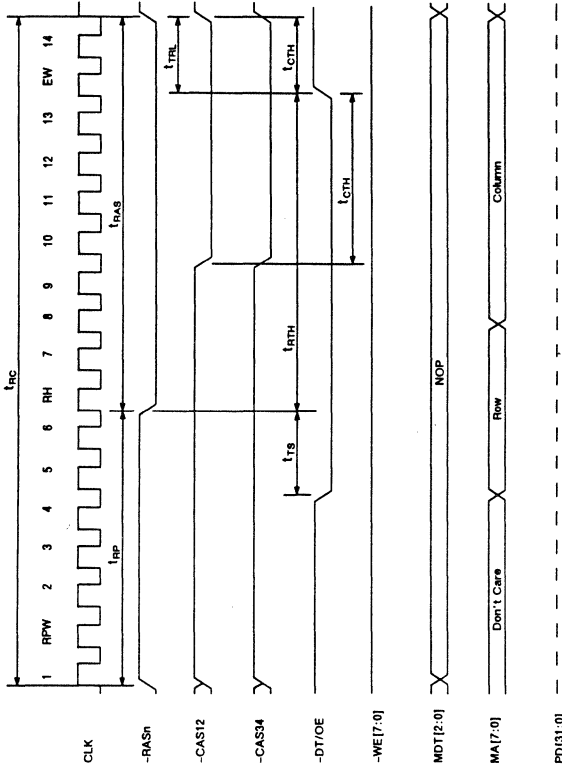
Figure C-11. VRAM Data Transfer Read Cycle Timing Diagram

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Table C-8. VRAM Data Transfer Read Cycle

Parameter	Symbol	Min	Max
–DT low setup time	t_{TS}	$2t_C$	–
–DT low hold time after –RAS low	t_{RTH}	$(8+RH)t_C$	–
–DT low hold time after –CAS low	t_{CTH}	$4t_C$	–
–DT high to –RAS high delay	t_{TRL}	$(1+EW)t_C$	–
–DT high to –CAS high delay	t_{CTH}	$(1+EW)t_C$	–

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A		

SCALE	SHT	OF

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VRAM Refresh Timing

Figure C-12. VRAM Refresh Timing Diagram

DWG SIZE	DRAWING NUMBER		REV.
A			
SCALE		SHT	OF

93-000032-00

Table C-9. VRAM CAS Before RAS Refresh Timing

Parameter	Symbol	Min	Max	Range $t_c = 16.667ns$
-CAS before -RAS setup time	t_{CSR}	$3t_c$	-	50
-CAS before -RAS hold time	t_{CHR}	$(4+RH)t_c$	-	66-83
-RAS rising to -CAS falling	t_{RPC}	$(2+RPW)t_c$	-	33-83

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SCALE		SHT OF	

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Serial Read Cycle Timing

Serial output from VRAM is read into PDM for all integrated back-end support designs.
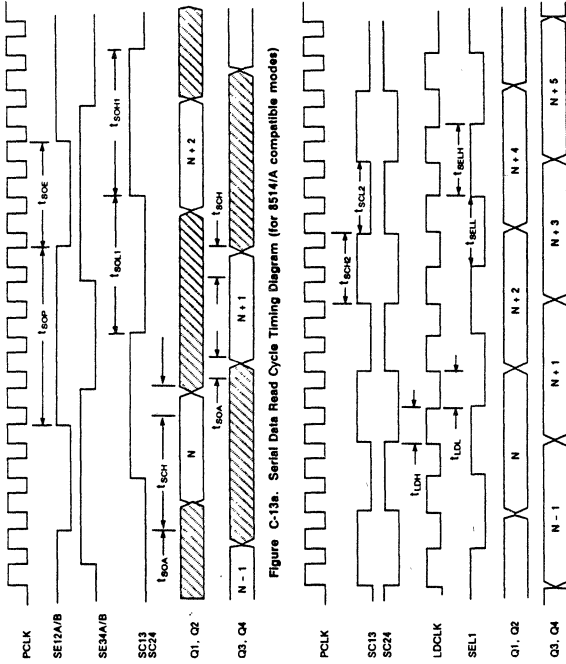
Figure C-13a. Serial Data Read Cycle Timing Diagram (for 8514/A compatible modes)

Figure C-13b. Serial Data Read Cycle Timing Diagram for 1280x1024 Mode

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Table C-10. Serial Data Read Cycle

Parameter	Symbol	Min	Max
SE† pulse width	t_{SOE}	$3t_C$	–
SE† precharge time	t_{SOP}	$5t_C$	–
SC* pulse width	t_{SCL1}	$4t_C$	–
SC* precharge time	t_{SCH1}	$4t_C$	–
serial output hold	t_{SOH}	$5t_C$	–
serial output access time from SE†	t_{SOA}	–	$1.5t_C$ (max)
SC* pulse width	t_{SCL2}	$2t_C$	–
SC* precharge time	t_{SCH2}	$2t_C$	–
LDCLK high time	t_{LDH}	t_C	–
LDCLK low time	t_{LDL}	t_C	–
SEL1 high time	t_{SELH}	$2t_C$	–
SEL1 low time	t_{SELL}	$2t_C$	–

† SE12A, SE12B, SE34A, SE34B, SE only toggles during active display period in 640x480 mode using 64Kx4. It stays high or low for all other modes.

* SC13, SC24

C-21

BACK-END VIDEO TIMING

Figure C-14. Video Timing Delay from VCLK
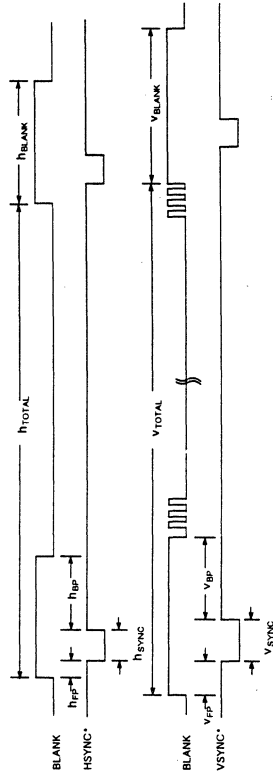
Figure C-15. Video Scan Timing Parameters

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Table C-11. Video Delay Timing Parameters

Symbol	Timing Parameter	Min	Max
t_{BLNK}	Delay of BLANK from the rising edge of VCLK	3	$t_{pc} -3$
t_{VD}	Delay of VDATA from the rising edge of VCLK (same as t_{HVD} in Figure 4.6.2)	3	$t_{pc} -3$
t_{DHSYNC}	Delay of HSYNC from the rising edge of VCLK	3	$t_{pc} -3$

Table C-12. Video Time Parameter Relationship to Video Registers

Symbol	Video Register Programming Equation		Units
H_{total} =	[(02E8)* +1]x8		pixels
H_{disp} =	[(06E8)+1]x8		pixels
H_{sync} =	(Bits 4–0; 0EE8)** x8		pixels
H_{fp} =	[(0ae8)x8] –H_{disp}		pixels
H_{bp} =	H_{total} –H_{syncw} –(0AE8)x8		pixels
V_{total}† =	[(12E8)]+1		lines
V_{disp}† =	[(16E8)]+1		lines
V_{sync} =	(Bits 4–0; 1EE8)/2		lines
V_{fp}† =	[(1AE8)]–[(16E8)]	lines	lines
V_{bp}† =	V_{total} –V_{syncw} –(1AE8)		lines

* (02E8) – content of register 02E8H

** (Bits 4–0; 0EE8) – value of Bits 4–0 for register 0EE8H

† The true value of these parameters are controlled by bit 2 and bit 1 of 22E8 register. See the table below.

Register 22E8		
bit 1	bit 2	Function
0	0	skip y2 and y1
1	0	skip y2
0	1	skip y1
1	1	no skip

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INTERCHIP TIMING

Figure C-16. Write-Per-Bit Mask Timing Diagram

Figure C-17. Interchip (PAM -> PDM) Read/Write Control Timing Diagram (IADSTAT = Low)

* In turbo mode, SWAP will change value at the same time as MDT field.

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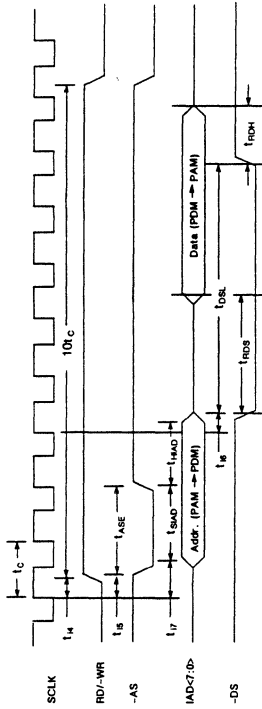
Figure C-18. Interchip Data Read Cycle Timing Diagram (IADSTAT = High)
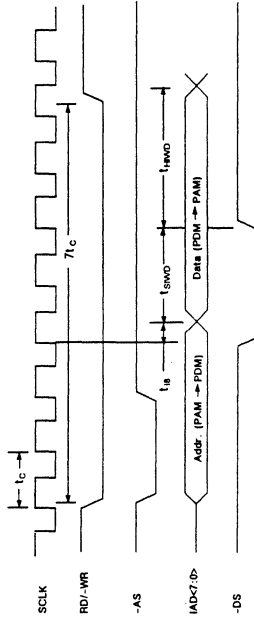
Figure C-19. Interchip Data Write Cycle Timing Diagram (IADSTAT = High)

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Table C-13. Delay from SCLK for Interchip Timing Parameters

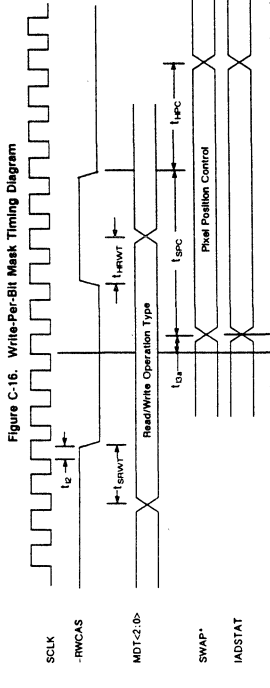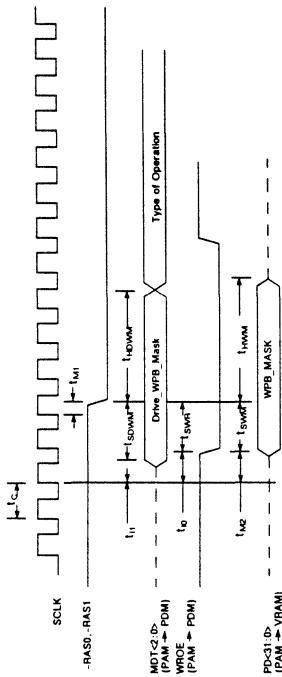| Symbol	Timing Parameter	PAM/PDM	Min	Max
t_{i0}	WROE active from rising edge of SCLK	PAM	–	26 ns
t_{i1}	MDT valid from rising edge of SCLK	PAM	–	26 ns
t_{i2}	–RWCAS change from rising edge of SCLK	PAM	–	30 ns
t_{i3a}	SWAP valid from rising edge of SCLK	PAM	–	26 ns
t_{i3b}	IADSTAD valid from rising edge of SCLK	PAM	–	35 ns
t_{i4}	RD/–WR valid from rising edge of SCLK	PAM	–	35 ns
t_{i5}	–AS change from rising edge of SCLK	PAM	–	35 ns
t_{i6}	–DS change from rising edge of SCLK	PAM	–	26 ns
t_{i7}	Addr. valid from rising edge of SCLK	PAM	–	35 ns
t_{i8}	Write Data valid from rising edge of SCLK	PAM	–	35 ns
t_{m1}	–RAS low from rising edge of SCLK	PAM	–	28 ns
t_{m2}	PD bus WPWGA-1_Mask valid from rising edge of SCLK	PDM	–	31 ns

Table C-14. Interchip Relative Timing Parameters

Symbol	Timing Parameter	PAM	PDM
t_{SWR}	Setup time for WROE to falling edge of –RAS	$(2t_C + t_{m1} - t_{i0})$	
t_{SDWM}	Setup time for MDT to falling edge of –RAS	$(2t_C + t_{m1} - t_{i1})$	
t_{HDWM}	Hold time for MDT from falling edge of –RAS	$(3t_C - t_{m1} + t_{i1})$	
t_{SWM}	Setup time for PD Write-mask to falling edge of –RAS	$(2t_C + t_{m1} - t_{m2})$	
t_{HWM}	Hold time for PD Write_mask from falling edge of –RAS	$(3t_C - t_{m1} + t_{m2})$	
t_{SRWT}	Setup time for MDT to falling edge of –RWCAS	$(2t_C + t_{i2} - t_{i1})$	
t_{HRWT}	Hold time for MDT from rising edge of –RWCAS	$(t_C - t_{i2} + t_{i1})$	
t_{SPC}	Setup time for IAD control to falling edge of –RWCAS	$(4t_C - t_{i3} + t_{i2})$	
t_{HPC}	Hold time for IAD control from falling edge of –RWCAS	$(2t_C + t_{i3} - t_{i2})$	
t_{ASL}	–AS low time)	$(2t_C)$	
t_{DSL}	–DS low time	$(2t_C)$ for write, $(3t_C)$ for read	
t_{SIAD}	Setup time for IAD address to rising edge of –AS	$(2t_C + t_{i5} - t_{i7})$	
t_{HAD}	Hold time for IAD address from rising edge of –AS	$(t_C - t_{i5} + t_{i7})$	
t_{SIRD}	Setup time for IAD read data to rising edge of –DS	$(2t_C - t_{i8} + t_{i6})$	
t_{HIRD}	Hold time for IAD read data from rising edge of –DS	$(t_C + t_{i8} - t_{i6})$	
t_{SIWD}	Setup time for IAD write data to rising edge of –DS	$(2t_C - t_{i9} + t_{i6})$	
t_{HIWD}	Hold time for IAD write data from rising edge of –DS	$(2t_C + t_{i9} - t_{i6})$	
t_{RDS}	IAD read data access time		max 38 ns

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RAMDAC INTERFACE TIMING

Figure C-20. DAC Write Operation Timing Diagram in Flicker-free Mode Only

Figure C-21. Pixel Video Clock and Data Timing Diagram

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Table C-15. DAC Interface Timing Parameter

Symbol	Timing Parameter	Min	Max
t_{DWL}	-DACWR low time (PDM)	$5t_{pc}$	-
t_{DWH}	-DACWR high time (PDM)	$5t_{pc}$	-
t_{SWD}	Setup time for Write Data to -DACWR	$4t_{pc}$	-
t_{HWD}	Hold time for Write Data from -DACWR	$2t_{pc}$	-
t_{D1}	Delay of -DACWR(PDM) from rising edge of PCLK	-	30
t_{D2}	Delay of VDATA<7:0> from rising edge of PCLK	-	30
t_{VC}	Output Video Pixel Clock Period	t_{pc}	$2t_{pc}$
t_{SVD}	Setup time for Video Data to rising edge of VCLK	3	
t_{HVD}	Hold time for Video Data from rising edge of VCLK (same as t_{vd} in Figure 4.4.1)	3	
t_{ACT}	SELVD high to -DACWR/-DACRD actively driven low	$2t_{pc}$	
t_{DIS}	-DACRD/-DACWR inactive to SELVD low	t_{pc}	
t_{VACT}	-ENVGA high to VDATA, BLANK, HSYNC and VSYNC active	t_c	
t_{VDIS}	VDATA, BLANC, HSYNC and VSYNC inactive to -ENVGA low	t_c	

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Pin Diagrams

WD95C00 (PAM)

Pin 1 Indicator

17 1 117

18 WD95C00 116

50 84

51 83
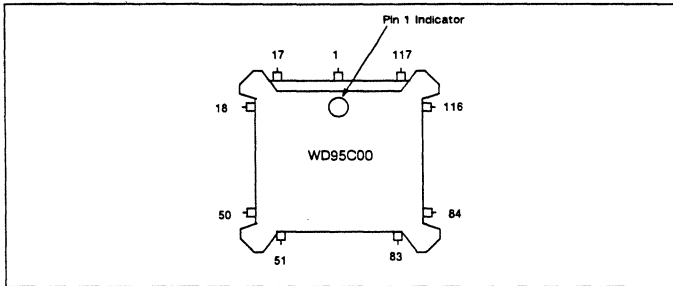
Figure D-1. WD95C00 132-Pin JEDEC Flat Pack

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	24	-WE0 (O)	47	BSA10 (O)	70	VDD
2	SELVD (I)	25	-WE1 (O)	48	BSA11 (O)	71	A8 (I)
3	MDT0 (O)	26	-WE2 (O)	49	BSA12 (O)	72	A9 (I)
4	MDT1 (O)	27	-WE3 (O)	50	VDD	73	A10 (I)
5	MDT2 (O)	28	-WE4 (O)	51	VSS	74	A11 (I)
6	WROE (O)	29	-WE5 (O)	52	RESET (I)	75	A12 (I)
7	SWAP (O)	30	-WE6 (O)	53	BSA13 (O)	76	A13 (I)
8	-RWCAS (O)	31	-WE7 (O)	54	BSA14 (O)	77	A14 (I)
9	VSS	32	-DT/-OE (O)	55	-DS/IO16 (O)	78	A15 (I)
10	MA0 (O)	33	VSS	56	-SBHE (I)	79	A16 (I)
11	MA1 (O)	34	LA13 (O)	57	MIO/-MEMR (I)	80	A17 (I)
12	MA2 (O)	35	LA24 (O)	58	-S1/-IOR (I)	81	A18 (I)
13	MA3 (O)	36	-BIOS OE (O)	59	-S0/-MEMW (I)	82	A19 (I)
14	MA4 (O)	37	BSA0 (O)	60	-CMD/-IOW (I)	83	VSS
15	MA5 (O)	38	BSA1 (O)	61	-ADL/BALE (I)	84	ATCLK (I)
16	MA6 (O)	39	BSA2 (O)	62	A0 (I)	85	AUP (I)
17	VDD	40	BSA3 (O)	63	A1 (I)	86	-SETUP/AEN(I)
18	VSS	41	BSA4 (O)	64	A2 (I)	87	VSS
19	MA7 (O)	42	BSA5 (O)	65	A3 (I)	88	-IRQ (O)
20	-CAS12 (O)	43	BSA6 (O)	66	A4 (I)	89	-CDSFDBK (O)
21	-CAS34 (O)	44	BSA7 (O)	67	A5 (I)	90	CHRDY (O)
22	-RAS0 (O)	45	BSA8 (O)	68	A6 (I)	91	-DBEN (O)
23	-RAS1 (O)	46	BSA9 (O)	69	A7 (I)	92	DBIR (O)

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Pin	Name	Pin	Name	Pin	Name	Pin	Name
93	VDD	103	D8/SD8 (I/O)	113	SCLK (I)	123	RD/-WR (O)
94	D0/SD0 (I/O)	104	D9/SD9 (I/O)	114	DAC8 (O)	124	IADSTAT (O)
95	D1/SD1 (I/O)	105	D10/SD10 (I/O)	115	VDD	125	IAD0 (I/O)
96	D2/SD2 (I/O)	106	D11/SD11 (I/O)	116	VSS	126	IAD1 (I/O)
97	D3/SD3 (I/O)	107	D12/SD12 (I/O)	117	RMWE (I)	127	IAD2 (I/O)
98	D4/SD4 (I/O)	108	D13/SD13 (I/O)	118	SLD (I)	128	IAD3 (I/O)
99	VSS	109	D14/SD14 (I/O)	119	SLC (I)	129	IAD4 (I/O)
100	D5/SD5 (I/O)	110	D15/SD15 (I/O)	120	MC/AT (I)	130	IAD5 (I/O)
101	D6/SD6 (I/O)	111	-DACRD (O)	121	-DS (O)	131	IAD6 (I/O)
102	D7/SD7 (I/O)	112	-DACWR (O)	122	-AS (O)	132	IAD7 (I/O)

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WD95C01 (PDM)
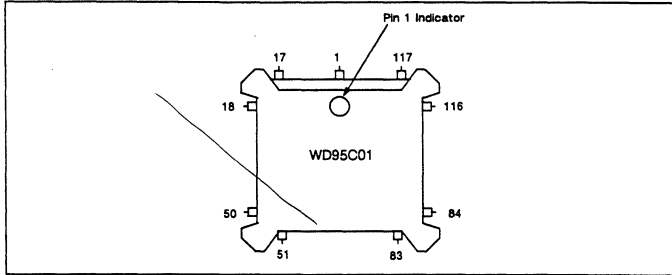
Figure D-2. WD95C01 132-Pin JEDEC Flat Pack

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	35	-DACV (I)	68	PCLK (I)	101	PD22 (I/O)
2	IAD7	36	MID2 (I)	69	VSS	102	PD21 (I/O)
3	IAD6	37	MID1 (I)	70	VDD	103	PD20 (I/O)
4	IAD5	38	MID0 (I)	71	SD11 (I)	104	PD19 (I/O)
5	IAD4	39	SCLK (I)	72	SD10 (I)	105	PD18 (I/O)
6	IAD3	40	RESET (I)	73	SD9 (I)	106	PD17 (I/O)
7	IAD2	41	VSS	74	SD8 (I)	107	PD16 (I/O)
8	IAD1	42	-ENVGA (O)	75	SD7 (I)	108	PD15 (I/O)
9	IAD0	43	CLKSEL2 (O)	76	SD6 (I)	109	PD14 (I/O)
10	IADSTAT	44	CLKSEL1 (O)	77	SD5 (I)	110	PD13 (I/O)
11	RD/-WR	45	CLKSEL0 (O)	78	SD4 (I)	111	PD12 (I/O)
12	-AS	46	SD31 (I)	79	SD3 (I)	112	PD11 (I/O)
13	-DS	47	SD30 (I)	80	SD2 (I)	113	PD10 (I/O)
14	VSS	48	SD29 (I)	81	SD1 (I)	114	PD9 (I/O)
15	SLC (O)	49	SD28 (I)	82	SD0 (I)	115	VSS
16	SLD (O)	50	VDD	83	VSS	116	VDD
17	VDD	51	VSS	84	SE34B (O)	117	PD8 (I/O)
18	VSS	52	SD27 (I)	85	SE34A (O)	118	PD7 (I/O)
19	RMWE (O)	53	SD26 (I)	86	SE12B (O)	119	PD6 (I/O)
20	BLANK (O)	54	SD25 (I)	87	SE12A (O)	120	PD5 (I/O)
21	VDATA7 (O)	55	SD24 (I)	88	SC13 (O)	121	PD4 (I/O)
22	VDATA6 (O)	56	SD23 (I)	89	SC24 (O)	122	PD3 (I/O)
23	VDATA5 (O)	57	SD22 (I)	90	PD31 (I/O)	123	PD2 (I/O)
24	VDATA4 (O)	58	SD21 (I)	91	PD30 (I/O)	124	PD1 (I/O)
25	VCLK (O)	59	SD20 (I)	92	PD29 (I/O)	125	PD0 (I/O)
26	VSS	60	SD19 (I)	93	PD28 (I/O)	126	-RWCAS (I)
27	VDATA3 (O)	61	SD18 (I)	94	VDD	127	SWAP (I)
28	VDATA2 (O)	62	SD17 (I)	95	PD27 (I/O)	128	WROE (I)
29	VDATA1 (O)	63	SD16 (I)	96	PD26 (I/O)	129	MDT2 (I)
30	VDATA0 (O)	64	SD15 (I)	97	PD25 (I/O)	130	MDT1 (I)
31	-DACRD (O)	65	SD14 (I)	98	PD24 (I/O)	131	MDT0 (I)
32	-DACWR (O)	66	SD13 (I)	99	VSS	132	SELVD (O)
33	HSYNC (O)	67	SD12 (I)	100	PD23 (I/O)		
34	VSYNC (O)						

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Figure D-3. Socket Diagram

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WESTERN DIGITAL IMAGING
PERSONAL WORKSTATION
GRAPHICS ARRAY-1
(PWGA-1)

REGISTER DEFINITIONS

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Rev. 1 March 1989

Contents

IBM® 8514/A COMPATIBLE REGISTERS

A board based on the PWGA-1 chip set is 100 percent compatible with the IBM 8514/A at the register level.

DAC Interface

The 8-bit registers shown in Table 1 are used to program the external video DAC. It is possible to write and read the DAC. Once the read/write index is written, multiple read/write operations can be performed without having to set the index for each entry.

Procedure to write to the DAC:

1. Set start write color index at 02ECH.

2. Write three bytes (R, G, B values) at 02EDH (The index auto increments to the next write entry).

3. Repeat step 2 until the desired number of entries have been programmed.

Procedure to read from the DAC:

1. Set start read color index at 02EBH.

2. Read three bytes (R, G, B values) at 02EDH (The index auto increments to the next read entry).

3. Repeat step 2 until the desired number of entries have been read.

Color Programming	8514/A	VGA
Look Up Table Mask (R/W)	02EA	03C6
Read Color Index	02EB (Write Only)	03C7 (Write Only)
DAC State	02EB (Read Only)	03C7 (Read Only)
Color Index (R/W)	02EC	03C8
RGB Color Value (R/W)	02ED	03C9

Table 1. DAC Color Programming Registers

Graphics Mode Control Register

Graphics mode is selected by writing to the Graphics Mode Control (GMC) Register at address 4AE8h (Figure 1). This register is used by all modules within the PWGA-1. Set Bit 0 to 1 to select 8514/A graphics mode or 0 to select VGA pass through mode. Bits 1 and 3 are reserved for mode extension; set Bit 1 to 1. Bit 2 selects the screen resolution; set Bit 2 to 1 to select 1024x768 (44.9 MHz) or 0 to select 640x480 (25.175 MHz).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												R		1	

Mode
    0=VGA
    1=8514/A

Reserved

Resolution
0=640x480
1=1024x768
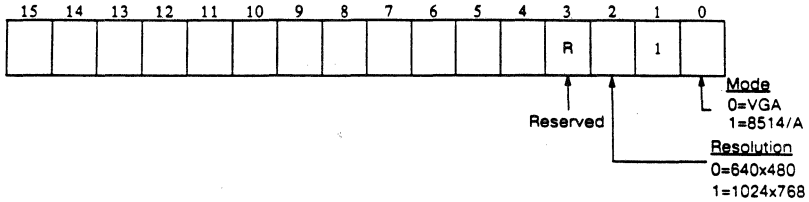
Figure 1. Graphics Mode Control Register (4AE8h Write Only)

Video Timing Setup Registers

There are nine registers for setting up video timing: four for horizontal, four for vertical, and one for control. These registers affect the video display of the PWGA-1. The horizontal and vertical registers are set by the selected resolution. For example, if 1024x768 is the graphics mode se-

lected by the GMC Register, then the horizontal and vertical registers are set accordingly. Table 2 shows what register value to set depending on the resolution selection.

Figures 2 through 9 show the format for the horizontal and vertical registers. Vertical timing is programmed in line resolution. Horizontal timing is programmed in 8-pixel resolution.

Register Address	Resolution		
	640x480	1024x768	
02E8	63h	9Dh	
06E8	4Fh	7Fh	
0AE8	52h	81h	
0EE8	2Ch	16h	
	640x480x4	640x480x8	1024x768
12E8	830h	418h	660h
16E8	779h	3BBh	5FBh
1AE8	7A8h	3D2h	600h
1EE8	22h	22h	08h
22E8	21h	23h	33h

Table 2. Settings for Video Timing Registers

Set Number of Pixels per Line
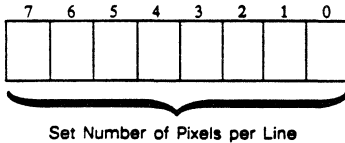
Figure 2. Horizontal Total Register
(02E8h Write Only)

Set Number of Pixels Displayed
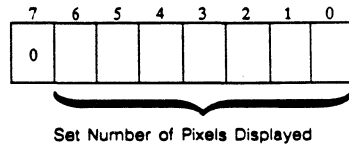
Figure 3. Horizontal Active Register
(06E8h Write Only)

Set Horizontal Sync Position
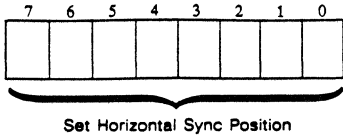
Figure 4. Horizontal Sync Position Register (0AE8h Write Only)

Set Number of Lines Displayed
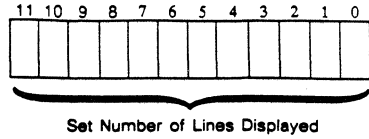
Figure 7. Vertical Active Register (16E8h Write Only)

Polarity
1=negative   Set Horizontal Sync Width
0=positive
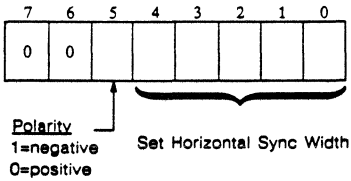
Figure 5. Horizontal Sync Width and Polarity Register (0EE8h Write Only)

Set Vertical Sync Position
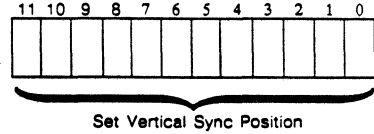
Figure 8. Vertical Sync Position Register (1AE8h Write Only)

Set Number of Lines per Frame
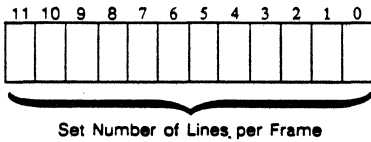
Figure 6. Vertical Total Register (12E8h Write Only)

Polarity   Set Vertical Sync Width
1=negative
0=positive
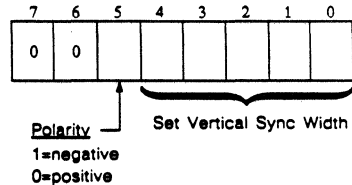
Figure 9. Vertical Sync Width and Polarity Register (1EE8h Write Only)

Display Control Register

The Display Control (DSC) Register sets various control features for the display functions (see Figure 10).

Skip Y1 Set Bit 1 to 0 to skip Bit 1 of the *y* scan counter in the screen refresh. This allows two pages to be displayed in 640x480x4 screen resolution.

Skip Y2 Set Bit 2 to 0 to skip Bit 2 of the *y* scan counter in the screen refresh. This allows two pages to be displayed in 1024x768x4 screen resolution.

Scan Bit 3 set to 1 specifies double scan (2); 0 specifies single scan (1).

Interlace Bit 4 set to 1 specifies interlaced mode; 0 specifies non-interlaced mode.

Enable Bits 5 and 6 work together to enable/
Display reset the display. The display is enabled when Bits 5 and 6 are set to 01 and reset when set to 10.

DSC = 033h (1024x768); 021h (640x480x4); 023h (640x480x8)
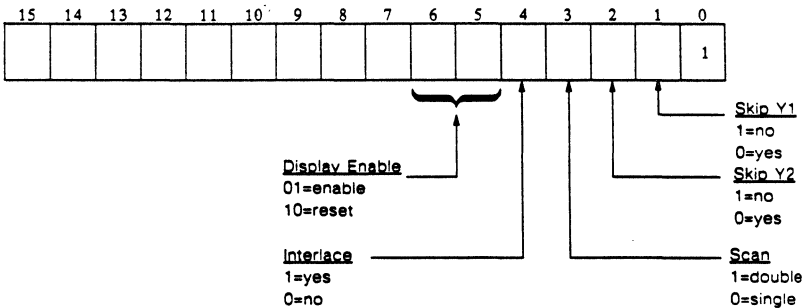
Figure 10. Display Control Register (22E8h Write Only)

5

Interrupt Control Register

The Interrupt Control (IC) Register at address 42E8h is used for interrupt and reset control of the PWGA-1 FIFO and other CPU interface functions (see Figure 11). This register is write only and affects Bits 3–0 of the Interrupt Status (IS) Register (see "Interrupt Status Register"). The IS Register is a read only register also at address 42E8h.

Vsync	Bit 0 puts a 0 in the vertical sync status bit of the IS Register that can be read at address 42E8h.
Graphic Engine (GE) Busy	Bit 1 puts a 0 in the GE busy status bit of the IS Register that can be read at address 42E8h.
FIFO Overflow & Invalid Read	Bit 2 puts a 0 in the FIFO overflow status bit of the IS Register that can be read at address 42E8h. This bit is cleared at the end of every line during a read across the plane.

FIFO Empty	Bit 3 puts a 0 in the FIFO empty status bit of the IS Register that can be read at address 42E8h.
Vsync	Bit 8 enables/disables the vertical sync interrupt.
GE Busy	Bit 9 enables/disables the GE busy interrupt.
FIFO Overflow	Bit 10 enables/disables the FIFO overflow interrupt.
FIFO Empty	Bit 11 enables/disables the FIFO empty interrupt.
Hardware Test	Bit 12=0, Bit 13=1 is used for Normal mode.
GE Reset	Bits 15 and 14 are used to switch between normal mode and reset.
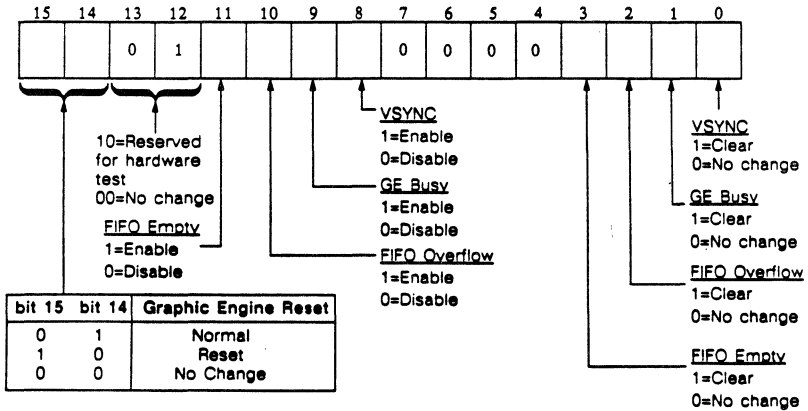
Figure 11. Interrupt Control Register (42E8h Write Only)

EPROM Selection Register

The EPROM Select (ES) Register is used by the CIU to enable EPROM bank selection and select a bank of EPROM. Figure 12 shows the register format for bank selection. Bit 3 enables/disables bank selection.
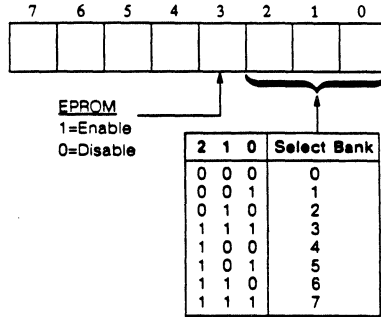
Figure 12. EPROM Select Register (46E8h Write Only)

BIOS EPROM Memory Location

BIOS EPROM memory location for Micro Channel consists of 2K fixed at C6800h to C6FFFh, 2K fixed at CA000h to CA7FFh, and 4K banks at C7000h to C7FFFh (see Table 3).

Table 3. Options for BIOS EPROM Memory Locations

Memory Location	Micro Channel
2K Fixed	C6800h–C6FFFh
4K Bank Selected	C7000h–C7FFFh
2K Fixed	CA000h–CA7FFh

Drawing Control

There are sixteen registers involved in drawing control.

Current Y Position (CYP) Register

The CYP Register at address 82E8h uses Bits 10-0 to define the current position of y for the pixel being drawn (see Figure 13). The value is 11 bits unsigned. Note that Bit 11 is reserved.

Current X Position (CXP) Register

The CXP Register at address 86E8h uses Bits 10-0 to define the current position of x for the pixel being drawn (see Figure 14). The value is 11 bits unsigned. Note that Bit 11 is reserved. The status of this register can be read.

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0
```
```
                R
```
Reserved   Current Y of Drawing Point Value
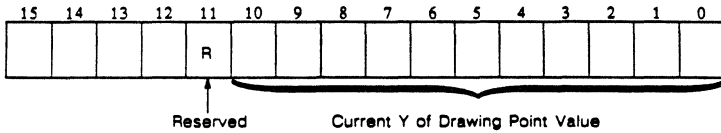
Figure 13. Current Y Position Register (82E8h Read/Write)

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0
```
```
                R
```
Reserved   Current X of Drawing Point Value
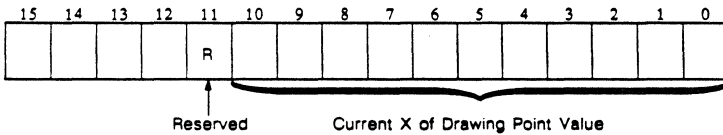
Figure 14. Current X Position Register (86E8h Read/Write)

Copy Y Destination/Incr 1 (CYDI) Register

The CYDI Register at address 8AE8h uses either Bits 10-0 to define the *y* destination when BITBLT copying, or Bits 11-0 to define Incre-ment 1 value when drawing a line (see Figure 15). The command performed is specified by the Drawing Command (DC) Register. The value is 12 bits unsigned when line drawing is specified. The minterm for the line drawing is:

Increment 1 = $2 \cdot (\min(|dx|,|dy|))$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									2's complement						

Line Parameter : Increment 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				R											
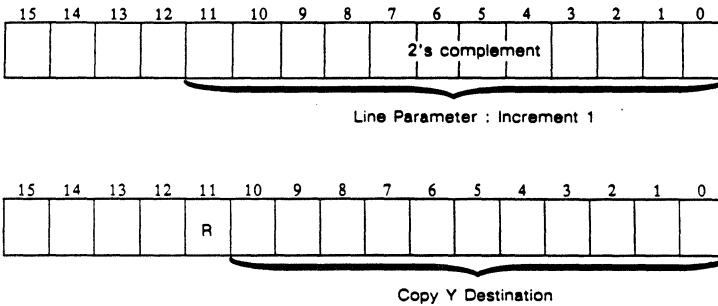
Copy Y Destination

Figure 15. Copy Y Destination/Incr 1 Register (8AE8h Write Only)

Copy X Destination/Incr 2 (CXDI) Register

The CXDI Register at address 8EE8h uses either Bits 10-0 to define the *x* destination when BITBLT copying, or Bits 12-0 to define Incr2 value when drawing a line (see Figure 16). The command performed is specified by the Drawing Command (DC) Register. The value is 13 bits signed when line drawing is specified. The min-term for the line drawing is:

Increment 2 = $2 * (\min(|dx|,|dy|) - \max(|dx|,|dy|))$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						signed 2's complement (always negative)									

Line Parameter : Increment 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				R											
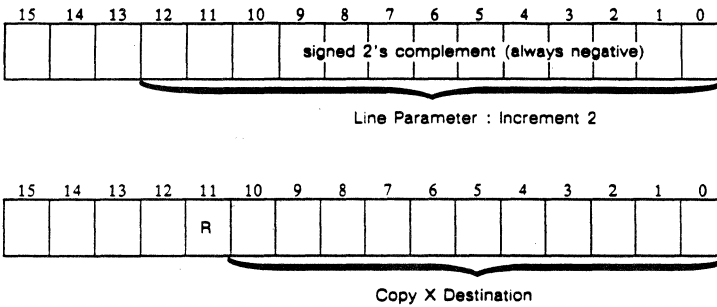
Copy X Destination

Figure 1-16. Copy X Destination/Incr 2 Register (8EE8h Write Only)

Delta Line (DL) Register

The DL Register at address 92E8h uses Bits 12–0 to define the delta for the current line drawing (see Figure 17). The value is 13 bits signed 2's complement. The minterm for the line drawing is:

$$2 \cdot [\min(|dx|,|dy|)] - \max(|dx|,|dy|) - 1$$

if starting x < ending x, and

$$2 \cdot [\min(|dx|,|dy|)] - \max(|dx|,|dy|)$$

if starting $x \gtreqless$ ending x.

The status of this register, when read after line drawing, is sign extended to 16 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Sign Extension   Delta Line Value
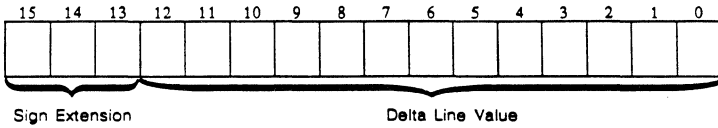
Figure 17. Delta Line Register (92E8h Read/Write)

Rectangle Width/Max (RWM) Register

The RWM Register at address 96E8h uses Bits 10-0 to either define the width for a rectangle in BITBLT or rectangle mode or draw a line (see Figure 18). The command performed is specified by the Drawing Command (DC) Register. The value is 11 bits unsigned. When line drawing is specified, the minterm for the line drawing is:

$$\text{Line Parameter} = \max(|dx|, |dy|)$$

$$\text{Rectangle Width Value} = \text{Rectangle Width} - 1$$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Rectangle Width Value or Line Parameter: Max Delta
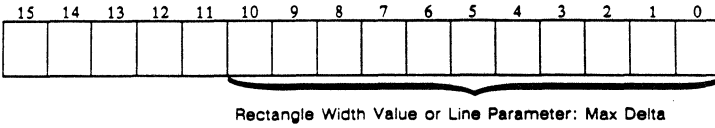
Figure 18. Rectangle Width/Max Register (96E8h Write Only)

Drawing Command (DC) Register

The DC Register at address 9AE8h provides commands for drawing (see Figure 19). All parameters have to be set before this command is sent to activate the drawing.

R/W   Bit 0 specifies a read operation when set to 0 and a write operation when set to 1.

Pixel   Bit 1 specifies single-pixel mode when
Mode   set to 0 and multi-pixel mode when set to 1.

Last Pixel   Bit 2 specifies the last pixel is drawn when set to 0 and turned off when set to 1.

Dir Type   Bit 3 specifies the type of line drawing direction as either radial (Deg) or co-ordinate-based (XY). The programmed direction is specified by Bits 7-5 of the DC Register. Direction type is radial when set to 1 and coordinate-based when set to 0.

Draw   Bit 4 specifies draw when set to 1 and update the drawing point only when set to 0.

Drawing   Bits 7-5 specify the direction to draw
Direction   using the direction type indicated by Bit 3 (see Figure 19).

CPU Data   Bit 8 provides a wait state when set to
Transfer   1 to allow waiting for CPU data during functions such as image transfer and texture line drawing.

Bus Select   Bit 9 specifies that the 16-bit data bus is selected when set to 1 and the 8-bit data bus is selected when set to 0.

Swap   Bit 12, when set to 1, specifies that
MSB/LSB   the most significant byte (MSB) be swapped with the least significant byte (LSB) when the 16-bit data bus is selected (i.e., Bit 9=1). Bit 12 is normally set to 0; the MSB is drawn first, then the LSB.

Command   Bits 15-13 specify the commands for
Type   drawing (see Figure 19).

Bit diagram showing bits 15 through 0.

Bit 11 = 0, Bit 10 = R

Labels:
- PC Data Transfer: 1=Yes, 0=No
- Bus Select: 1=16, 0=8
- Reserved
- SWAP MSB/LSB: 1=Yes, 0=No
- Draw: 1=Yes, 0=No
- DIR Type: 1=Deg, 0=XY
- Last Pixel: 1=Off, 0=On
- Pixel Mode: 1=Multi, 0=Single
- R/W: 1=W, 0=R

			Drawing Direction	
7	6	5	Bit 3=1	Bit 3=0
0	0	0	0 degrees	Y neg, X major, X neg
0	0	1	45 degrees	Y neg, X major, X pos
0	1	0	90 degrees	Y neg, Y major, X neg
0	1	1	135 degrees	Y neg, Y major, X pos
1	0	0	180 degrees	Y pos, X major, X neg
1	0	1	225 degrees	Y pos, X major, X pos
1	1	0	270 degrees	Y pos, Y major, X neg
1	1	1	315 degrees	Y pos, Y major, X pos

15	14	13	Drawing Function Command
0	0	0	No Operation
0	0	1	Draw Line
0	1	0	Fill Rectangle (Hor. 1st by 4 Hor. pixels); Search & Fill*
0	1	1	" " (Vert. 1st by 2 Vert. pixels)*
1	0	0	" " (Vert. 1st by 4 Hor. pixels)
1	0	1	Draw Line (Polygon Boundary)
1	1	0	BITBLT
1	1	1	Not defined

* see BEE8-A

Figure 19. Drawing Command Register (9AE8h Write Only)

Short Stroke Vector Control (SSVC) Register

The SSVC Register at address 9EE8h provides two bytes of data. Each byte specifies the length, direction, and move/draw control for a short vector.

Pixel Line Length Bits 3-0 and 11-8 define the pixel line length.

Move/Draw Bit 4 indicates a draw function when set to 1 and a move function when set to 0.

Drawing Direction Bits 7-5 and 15-13 specify the direction to draw using the direction type, either radial-based or coordinate-based, as specified by Bit 3 of the DC Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Drawing Direction | Pixel Line Length Value | Drawing Direction | Pixel Line Length Value

0=move
1=draw

0=move
1=draw

15	14	13	Drawing Direction	
7	6	5	Bits (9AE8) = 1	Bits (9AE8) = 0
0	0	0	0 degrees	x major, x neg. (left)
0	0	1	45 degress	x major, x pos. (right)
0	1	0	90 degrees	y major, y neg. (up)
0	1	1	135 degrees	y major, y neg. (up)
1	0	0	180 degrees	x major, x neg. (left)
1	0	1	225 degrees	x major, x pos. (right)
1	1	0	270 degrees	y major, y pos. (down)
1	1	1	315 degrees	y major, y pos. (down)
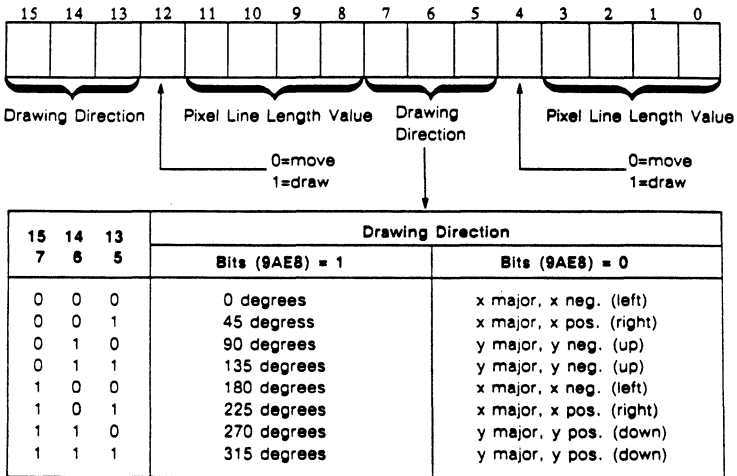
Figure 20. Short Stroke Vector Control Register (9EE8h Write Only)

Background Color (BC) Register

The BC Register at address A2E8h specifies the background color (see Figure 21). The MSB in this word is not used.

7	6	5	4	3	2	1	0

Background Color Value
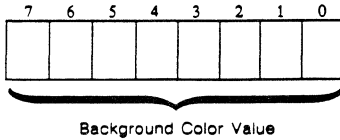
Figure 21. Background Color Register (A2E8h Write Only)

Foreground Color (FC) Register

The FC Register at address A6E8h specifies the foreground color (see Figure 22). The MSB in this word is not used.

7	6	5	4	3	2	1	0

Foreground Color Value
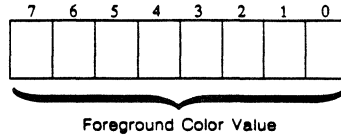
Figure 22. Foreground Color Register (A6E8h Write Only)

Bit-plane Write Mask (BWM) Register

The BWM Register at address AAE8h specifies the bit-plane selected for graphics or text update (see Figure 23). The MSB in this word is not used.

Bit-plane Read Mask (BRM) Register

The BRM Register at address AEE8h specifies the read source mask for graphics or text update (see Figure 24). The value is the true mask rotated left one bit; that is, Bit 0 is the mask for Plane 7 and Bits 1-7 are the mask bits for Planes 0-6, respectively. However, for polygon fill, Bits 2, 3, and 4 are for Planes 2, 3, and 4, respectively. The MSB in this word is not used.

7	6	5	4	3	2	1	0
Plane 7	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0

Bit-plane Write Mask
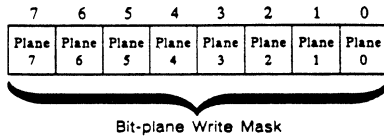
Figure 23. Bit-plane Write Mask Register (AAE8h Write Only)

BITBLT

			4	3	2	1	0	
			Plane 3	Plane 2	Plane 1	Plane 0		4-bit Bit-plane

7	6	5	4	3	2	1	0	
Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0	Plane 7	8-bit Bit-plane

7	6	5	4	3	2	1	0
* Plane 7	* Plane 6	* Plane 5	* Plane 4	* Plane 3	* Plane 2	* Plane 1	* Plane 0

* = plane no. corresponds to bit no. for search & fill.

For each plane: 1=yes
              0=no
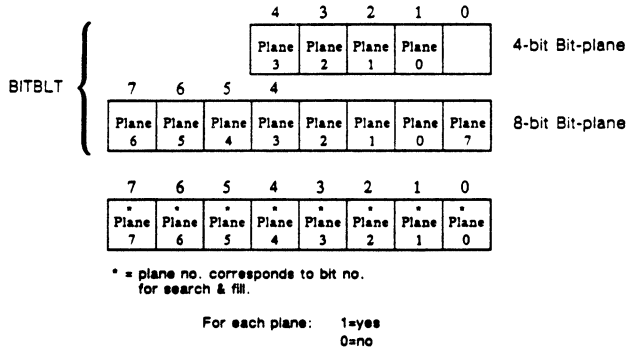
Figure 24. Bit-plane Read Mask Register (AEE8h Write Only)

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Comparison Color (CC) Register

The CC Register at address B2E8h specifies the comparison color (see Figure 25). The MSB in this word is not used.

Comparison Color Value
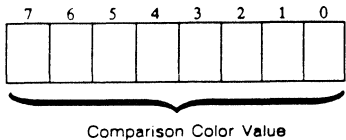
Figure 25. Comparison Color Register (B2E8h Write Only)

Background Mix (BM) Register

The BM Register at address B6E8h specifies the background mix (see Figure 26). The MSB in this word is not used.

Background Mix Value
see definition for Foreground Mix
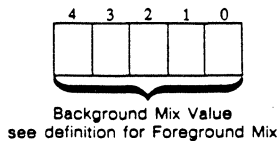
Figure 26. Background Mix Register (B6E8h Write Only)

Foreground Mix (FM) Register

The FM Register at address BAE8h specifies the foreground mix (see Figure 27). Bits 4-0 specify the foreground mix command. Bits 6 and 5 specify color selection. The MSB in this word is not used.

6	5	Color Source Select
0	0	BGC
0	1	FGC
1	0	CPU data
1	1	Display memory

Bits 4-0	Foreground Mix command	Bits 4-0	Foreground Mix command
00	not screen	10	minimum
01	zero	11	(screen−new) without saturate
02	one	12	(new−screen) without saturate
03	leave alone	13	(new+screen) without saturate
04	not new	14	maximum
05	xor	15	(screen−new)/2 without saturate
06	not screen xor new	16	(new−screen)/2 without saturate*
07	overpaint	17	average = (new+screen)/2 w/o saturate
08	not screen or not new	18	(Screen−new) with saturate
09	screen or not new	19	(Screen−new) with saturate
0A	not screen or new	1A	(new−screen) with saturate
0B	screen or new	1B	(new+screen) with saturate
0C	screen and new	1C	(screen−new)/2 with saturate
0D	not screen and new	1D	(screen−new)/2 with saturate
0E	screen and not new	1E	(new−screen)/2 with saturate**
0F	not screen and not new	1F	(screen+new)/2 with saturate

*Borrow included in shifting ·
**Set to 0 in borrow = 1

Figure 27. Foreground Mix Register (BAE8h Write Only)

Multifunction Control (MC) Register

The MC Register at address BEE8h specifies several drawing control parameters (see Figure 28a). Bits 15-12 control the use of this register; when these bits are changed, the register changes function.

Rectangle Height Register

When Bits 15-12 are set to 0, the value in Bits 10-0 specifies rectangle height.

Value = rectangle height - 1

Clip Window Top Limit Register

When Bits 15-12 are set to 1, the value in Bits 10-0 specifies the clipping window top limit.

Clip Window Left Limit Register

When Bits 15-12 are set to 2, the value in Bits 10-0 specifies the clipping window left limit.

Clip Window Bottom Limit Register

When Bits 15-12 are set to 3, the value in Bits 10-0 specifies the clipping window bottom limit.

Clip Window Right Limit Register

When Bits 15-12 are set to 4, the value in Bits 10-0 specifies the clipping window right limit.

15	14	13	12	Addr.	Parameter
0	0	0	0	BEE8-0	Rectangle height - 1
0	0	0	1	BEE8-1	Clipping window top limit
0	0	1	0	BEE8-2	Clipping window left limit
0	0	1	1	BEE8-3	Clipping window bottom limit
0	1	0	0	BEE8-4	Clipping window right limit

Figure 28a. Multifunction Control Register (BEE8-0,1,2,3,4 Write Only)

Memory Configuration Register

When Bits 15–12 are set to 5, memory configuration is selected. Bit 0 is reserved and should be set to 0. Bit 1 is reserved and should be set to 1. Bits 2 and 3 (RES) specify resolution and Bit 4 specifies planes for drawing (see Figure 28b).
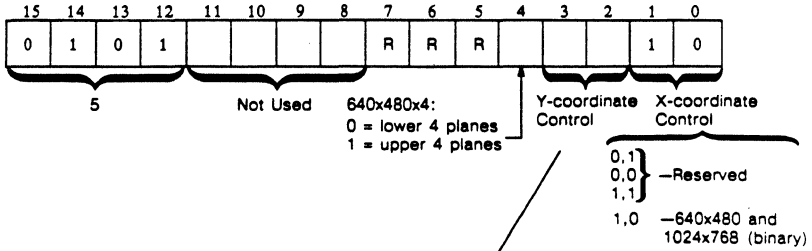
Y-coordinate Control	3	2	Resolution
Skip Y	0	0	640x480x4 (Bit 1 of 22E8h must equal 0)
linear	0	1	1024x768 or 640x480x8
Not used	1	0	Not defined
Not used	1	1	Not defined

Figure 28b. Memory Configuration Register (BEE8-5 Write Only)

Pixel Position Mix Control/L Register

When Bits 15–12 are set to 8, Pixel Position Mix Control/L is selected (see Figure 28c). Bits 4–1 specify the pixel position mix control for pixels 0–3.

Pixel Position Mix Control/H Register

When Bits 15–12 are set to 9, Pixel Position Mix Control/H is selected (see Figure 28c). Bits 4–1 specify the pixel position mix control for pixels 4–7.

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┐
│ 1 │ 0 │ 0 │   │   │   │   │   │   │   │   │   │   │   │   │ 0 │
└───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┘
```

Position Mix Control
0=low   BEE8-8
1=high   BEE8-9

Position Mix Control

High	Low
pixel 4	pixel 0
pixel 5	pixel 1
pixel 6	pixel 2
pixel 7	pixel 3

0=no
1=yes
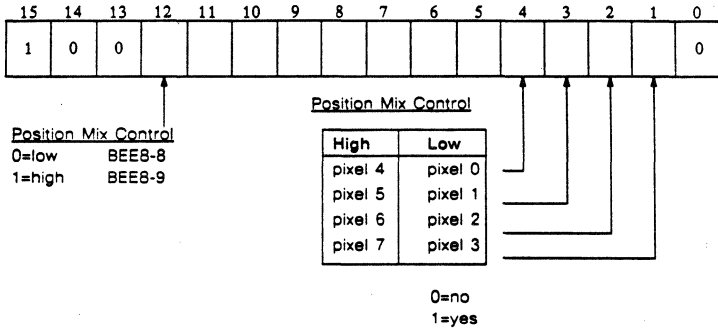
Figure 28c. Pixel Position Mix Control Register (BEE8-8, BEE8-9 Write Only)

Data Extension/Compare Control Register

When Bits 15–12 are set to A, Data Extension/Compare is selected (see Figure 28d) and the following applies to Bits 7–2:

Packed Data/ Search Enable   Bit 2 = 0 is normal. Bit 2 = 1 enables use of packed data. When in operation involving read, packed data is computed from the source. Packed Data is defined as "the screen data ORed with the complement of the bitplane read mask." If the result is all 1, then 1 is extracted, otherwise 0 is extracted per pixel. When write operation is selected, PWGA–1 goes into a special search and fill mode. The screen data is read and if the packed data extracted is 0, write operation is suspended. When a packed data "1" is encountered, write operation is enabled until the next "1". This mode is used to detect the boundary of a polygon for fill operation.

Data Compare   Bits 5–3 specify data comparison parameters.

Data Extension   Bits 6 and 7 specify data extension, mix type, and extension sources.

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0							0	0

A

Data extension

Data compare

Packed Data/Search Enable

2	Packed Data		Use
1	Enabled	Read	Read packed data
		Write	Search and fill mode
0	No	Read/Write	Normal

	Data Extension	Mix Operation	Use
7 6	• Bit pattern from the following sources	• Color sources selected by Bit 5, 6, of BAE8h	Use
0 0	Bit pattern = always·1	Bit 6=0, Bit 5=1 (BAE8h)	Regular
0 1	Pixel position Mix Control BEE8-8,9	Data=1 → Color Source & Foreground Mix (FMX)	Limited use: certain textures horizontal line
1 0	CPU pixel data	Background Color (BGC) & Data=0 →	CPU 10-bit pattern image transfer to display memory
1 1	Display memory used to display packed data* bit pattern	Background Mix (BMX)	BITBLT across the plane or from 1 bit-plane to FGC and BGC through all planes
1 1	Packed data* same as above	Bit 6=1, Bit 5=0 (BAE8h) Data=1 →CPU data & FMX Data=0 →BGC & BMX	Special marker** mode

*packed data—the screen data is ORed with the complement of the bitplane read mask. If the result is all 1, then 1 is extracted, otherwise 0 is extracted per pixel.

**marker—special BITBLT mode used for multi-color marker. A 10 pattern is stored in display memory. During BITBLT, if display memory data=1, CPU data is used. If data=0, background color is used.

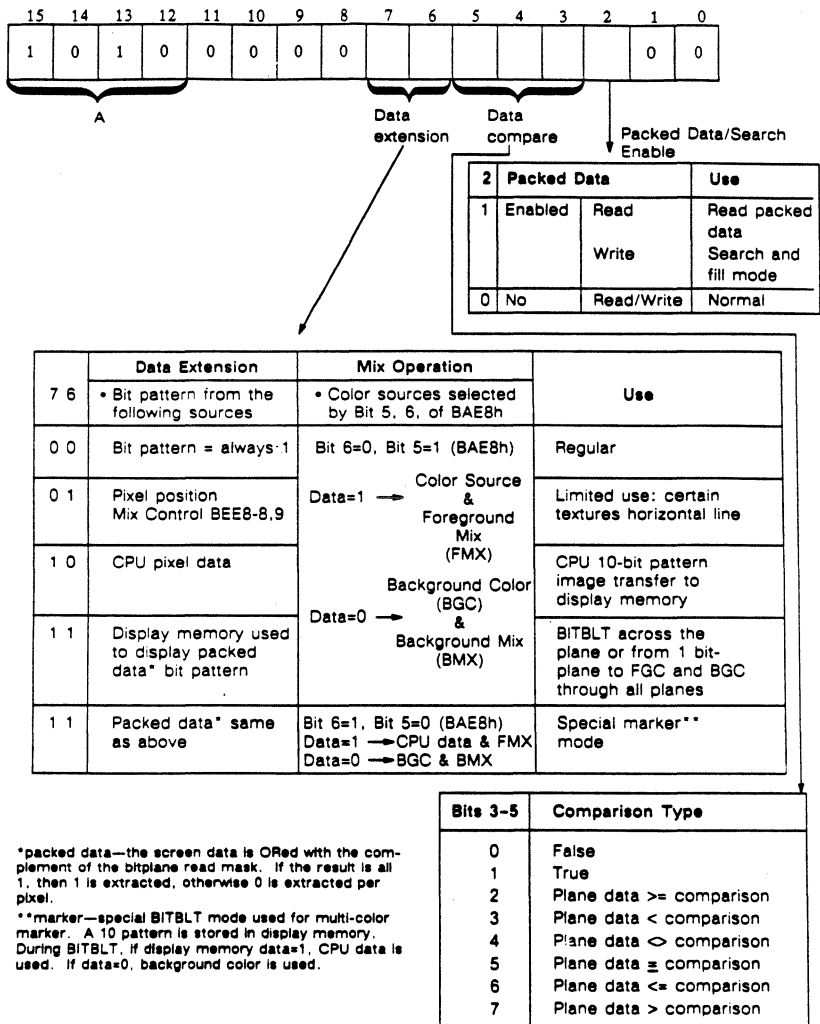| Bits 3-5	Comparison Type
0	False
1	True
2	Plane data >= comparison
3	Plane data < comparison
4	Plane data <> comparison
5	Plane data ≥ comparison
6	Plane data <= comparison
7	Plane data > comparison

Figure 28d. Multifunction Control Register (BEE8-A Write Only)

Image Read/Write (IRW) Register

The IRW Register at address E2E8h specifies the read/write port for image transfer. For across the plane image transfer, read/write data is determined by nibble boundary on the screen. The starting point will fall on the first nibble group. For word mode, two nibbles of data can be transferred for each read/write (see Figure 29). For through the plane image transfer, two pixels can be transferred for each read/write operation in word mode (see Figure 30).

For Pixel Read operation across the plane:

$$\text{bit value} = \prod_{i=1}^{n} (P_i + \overline{RM}_i)$$

n = maximum bit-plane value
P_i = pixel value of the bit-plane
RM_i = read mask for the i-th bit-plane

For Pixel write operation across the plane:

bit value=0 will write background color
bit value=1 will write foreground color

screen pixel from left to right: 0 1 2 3 4 5 6 7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			pixel 4	pixel 5	pixel 6	pixel 7					pixel 0	pixel 1	pixel 2	pixel 3	

Pixel Read/Write value
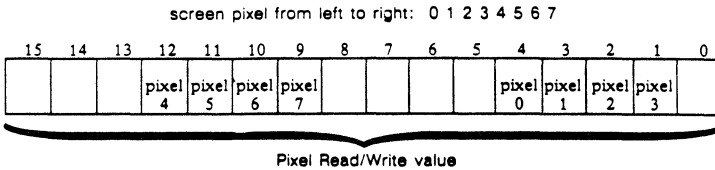
Figure 29. Image Read/Write Register (E2E8h Read/Write) Across the Plane

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0	bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0

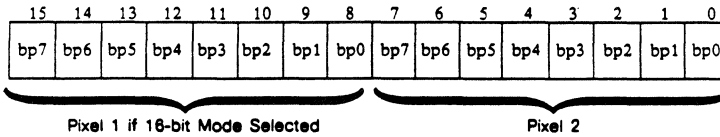Pixel 1 if 16-bit Mode Selected   Pixel 2

Figure 30. Image Read/Write Register (E2E8h Read/Write) through the Plane

Status

There are three status registers that can be read to acquire information; the Interrupt Status (IS) register at address 42E8h, and the FIFO Status (FS) Register at address 9AE8h, and the Video Status (VS) register at address O2E8h.

Interrupt Status (IS) Register

The IS Register provides interrupt status, monitor ID, and plane size (see Figure 31).

Vsync   Bit 0 indicates a vertical sync interrupt when set to 1.

GE Busy   Bit 1 indicates GE busy when set to 1.

FIFO Overflow   Bit 2 indicates FIFO overflow when set to 1.

FIFO Empty   Bit 3 indicates FIFO empty when set to 1.

Monitor ID   Bits 4–6 indicate the monitor type being driven by the PWGA-1 or 8514/A.

Plane Size   Bit 7 indicates a 4-bit plane when set to 0 or an 8-bit plane when set to 1.

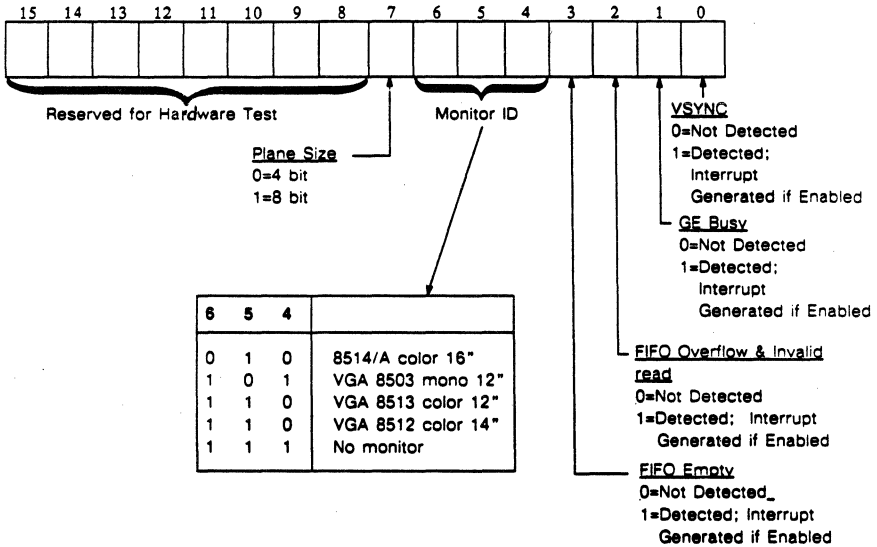| 6	5	4	
0	1	0	8514/A color 16"
1	0	1	VGA 8503 mono 12"
1	1	0	VGA 8513 color 12"
1	1	0	VGA 8512 color 14"
1	1	1	No monitor

Figure 31. Interrupt Status Register (42E8h Read Only)

FIFO Status (FS) Register

The FS Register provides FIFO status information, PC read data status, and hardware busy status (see Figure 32).

FIFO   Bits 7–0 of the FS Register indicate
Occupied   data status of the FIFO (i.e., a 1 in Bit 2 indicates that the third entry of

the input FIFO is occupied by data).

Data   Bit 8 indicates that CPU read data is
Taken   taken when set to 1 and not taken when set to 0.

Hrdwr   Bit 9 indicates that the hardware is
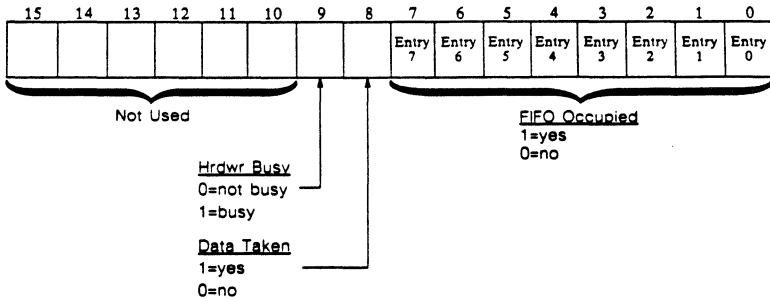*Busy*   busy when set to 1 and not busy when set to 0.

Figure 32. FIFO Status Register (9AE8h Read Only)

Video Status (VS) Register

The VS Register (Figure 33) provides video status information.

Bit 1 : vertical sync
VGA mode : 1.28 ms-positive polarity
640x480 mode : 16.8 ms-negative polarity
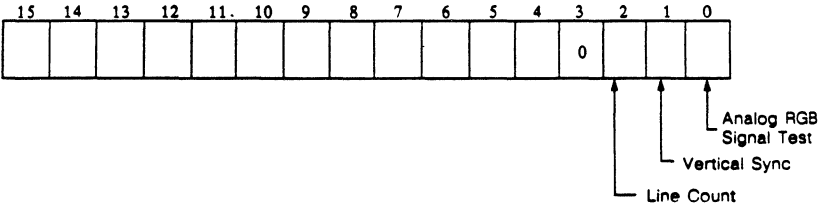1024x768 mode : 11.6 ms-positive polarity

Figure 33. Video Status Register (02E8h Read Only)

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Table 4. Address Decoding Tables

Address Decoding Table for Read

Bits 15-12/11-0	2e8	6e8	ae8	ee8h
0	2e8	2e8	2e8	2e8
1	2e8	2e8	2e8	2e8
2	2e8	2e8	2e8	2e8
3	2e8	2e8	2e8	2e8
4	42e8	42e8	42e8	42e8
5	42e8	42e8	42e8	42e8
6	42e8	42e8	42e8	42e8
7	42e8	42e8	42e8	42e8
8	82e8	86e8	0*	0*
9	92e8	0*	9ae8	0*
a	e2e8	e2e8	0*	0*
b	0*	0*	0*	0*
c	82e8	86e8	0*	0*
d	92e8	0*	9ae8	0*
e	e2e8	e2e8	0*	0*
f	0*	0*	0*	0*

* A value of zero will be read

Address Decoding Table for Write

Bits 15-12/11-0	2e8	6e8	ae8	ee8h
0	2e8	6e8	ae8	ee8
1	12e8	16e8	1ae8	1ee8
2	22e8	X	X	X
3	X	X	X	X
4	42e8	46e8	4ae8	X
5	42e8	46e8	4ae8	X
6	42e8	46e8	4ae8	X
7	42e8	46e8	4ae8	X
8	82e8	86e8	8ae8	8ee8
9	92e8	96e8	9ae8	9ee8
a	a2e8	a6e8	aae8	aee8
b	b2e8	b6e8	bae8	bee8
c	82e8	86e8	8ae8	8ee8
d	92e8	96e8	9ae8	9ee8
e	a2e8	a6e8	aae8	aee8
f	b2e8	b6e8	bae8	bee8

When in wait CPU data mode and graphic engine is busy, register a2e8h, a6e8h, e2e8h, and e6e8h are the same as e2e8.

Table 5. IBM 8514/A Compatible Registers

O2EA/03C6	R/W	Look Up Table Mask
O2EB/03C7	W	Read Color Index
O2EB/03C7	R	DAC State
O2EC/03C8	R/W	Color Index
O2ED/03C9	R/W	RGB Color Value
02E8	R	Video Control Status
02E8	W	Horizontal Total
06E8	W	Horizontal Active
0AE8	W	Horizontal Sync Position
0EE8	W	Horizontal Sync Width/Polarity
12E8	W	Vertical Total
16E8	W	Vertical Active
1AE8	W	Vertical Sync Position
1EE8	W	Vertical Sync Width/Polarity
22E8	W	Display Control
42E8	R	Interrupt Status
42E8	W	Interrupt/FIFO/Reset Control
46E8	W	EPROM Selection
4AE8	W	Graphics Mode Control
82E8	R/W	Current Y Position
86E8	R/W	Current X Position
8AE8	W	Copy Y Destination/Incr 1 Line
8EE8	W	Copy X Destination/Incr 2 Line
92E8	R/W	Delta Line
96E8	W	Rectangle Width/Max for Line
9AE8	R	FIFO Status
9AE8	W	Drawing Command Control
9EE8	W	Short Stroke Vector Control
A2E8	W	Background Color
A6E8	W	Foreground Color
AAE8	W	Bit-Plane Write Mask
AEE8	W	Bit-Plane Read Mask
B2E8	W	Comparison Color
B6E8	W	Background Mix
BAE8	W	Foreground Mix
BEE8		Multifunction Control
BEE8 (0)	W	Rectangle Height
BEE8 (1)	W	Clipping Window Top Limit
BEE8 (2)	W	Clipping Window Left Limit
BEE8 (3)	W	Clipping Window Bottom Limit

Table 5. IBM 8514/A Compatible Registers (cont.)

BEE8 (4)	W	Clipping Window Right Limit
BEE8 (5)	W	Memory Configuration
BEE8 (8)	W	Pixel Position Mix Control—Low
BEE8 (9)	W	Pixel Position Mix Control—High
BEE8 (A)	W	Data Extension/Compare Control
E2E8	R/W	Image Read/Write