YAMAHA LSI

YMF715x (OPL3-SA3)

- Register Description Document-

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1. FM-Synthesizer Descriptions

The followings are the detail descriptions of FM-synthesizer block that are shown in YMF715x (OPL3-SA3) specification. The FM-synthesizer is compatible with YMF262(OPL3)/YMF289B(OPL3-L) used for the Sound Blaster/Adlib game music synthesizer which is de facto standard in sound card market.

1-1. Overview of FM-synthesizer

FM stands for “Frequency Modulation”. FM synthesis exploits the fact that modulating one waveform with another waveform will produce a waveform with many more harmonics than were present in the modulator or carrier (the modulated wave form). The frequency ratio of modulator to carrier will determine which harmonics will result. Using integer and non-integer ratios allows the user to create rich harmonic and inharmonic sounds from two sine waves.

In Fig.1-1, the sine wave oscillators are called *operators*. The first box is called a *modulator* and next box is called a *carrier*. The arrangement of operators is called an *algorithm*. YMF715x (OPL3-SA3) FM-synthesizer can use two operators in two different algorithms and four operators in four different algorithms.

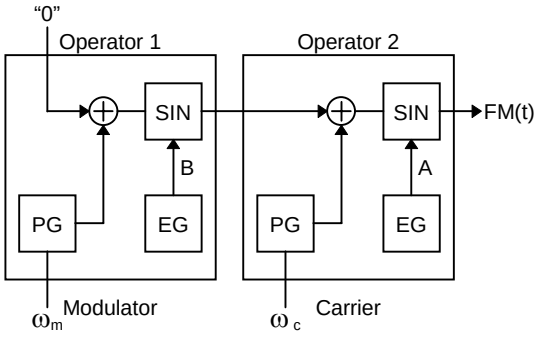


Fig. 1-1 Basic Configuration of a simple FM System

The configuration shown in Fig.1-1 can be expressed in an equation as follows :

$$FM(t) = A \sin (\omega_c t + B \sin \omega_m t)$$

In this equation, A and B represent the amplitude of operators 2 and 1 respectively. The angle frequency of operators 2 and 1 are respectively represented by ω_c and ω_m.

YMF715x (OPL3-SA3) FM-synthesizer also provides an operator that features feedback which allows that operator to modulate itself as shown in fig.1-2.

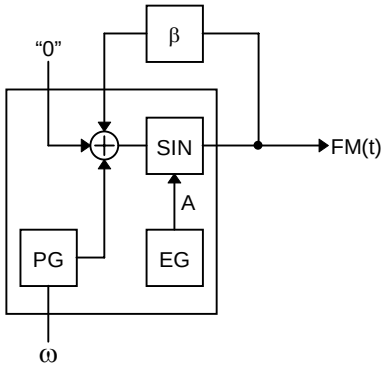


Fig. 1-2 Feedback FM System

This oerator can be expressed in the equation below:

$$FM(t) = A \sin \{\omega t + \beta FM(t)\}$$

where β represents *feedback ratio*. Feedback FM is an economic way of producing a spectra rich in harmonics. One feedback operator can produce a sawtooth-like spectra (which is useful when trying to make string sounds).

1-2. Register Interface

Listed below are the YMF715x (OPL3-SA3) FM-synthesizer registers for AdLib compatibility. Table 1-1 is the all register mapping of the FM-synthesizer.

Adlib base+0	R	Status Register port
Adlib base+0	W	Address Register port (array 0)
Adlib base+1	R/W	Data Register port
Adlib base+2	W	Address Register port (array 1)
Adlib base+3	R/W	Data Register port

Table 1-1. FM-synthesizer Status/Data Register Mapping

Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	IRQ	FT1	FT2	-	-	BUSY	-	BUSY

Data Register Array 0 (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
02h	TIMER 1							
03h	TIMER 2							
04h	RST	MT1	MT2	-	-	-	ST2	ST1
08h	-	NTS	-	-	-	-	-	-
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

Data Register Array 1 (R/W)

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
04h	-	-	CONNECTION SEL					
05h	-	-	-	-	-	NEW3	*	NEW
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

When the YMF715x (OPL3-SA3) FM-synthesizer is used with /EXTEN pin when SEL=3, 4, 7 is driven "L" for a wavetable upgrade as a chip-set with the YMF721 (OPL4-ML2), the additional I/O ports listed below can also be accessed. In the case of SB (Sound Blaster) mode, AdLib base + 2, 3 port are write-only registers.

Adlib base+4	R	Status Register port for Wavetable
Adlib base+4	W	Address Register port for Wavetable
Adlib base+5	R/W	Data Register port for Wavetable
Adlib base+6	R/W	Command write/response port
Adlib base+7	R/W	Control write/status port

1-3. Status Register

The follwing are FM-synthesizer status register.

Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	IRQ	FT1	FT2	-	-	BUSY	-	BUSY

YMF715x (OPL3-SA3) FM-synthesizer block has two programmable timers. Each timer provides the flag according to value of timer 1 or timer 2. The host can read these flags as status information or interrupt signal.

IRQ

Interrupt ReQuest flag : This bit can read as "1" when either of FT1 or FT2 bit is set to "1". This bit is reset when index 04h (array 0), RST bit is set to "1".

FT1

Flag Timer 1 : This bit can be read "1" when the time set at timer 1 has elapsed. This bit is cleared when index 04h (array 0), RST bit is set to "1".

FT2

Flag Timer 2 : This bit can be read "1" when the time set at timer 2 has elapsed. This bit is cleared when index 04h (array 0), RST bit is set to "1".

BUSY

BUSY flag : This bit is available when index 05h (array 1), NEW3 bit is set to "1". YMF715x (OPL3-SA3) FM-synthesizer block requires approximately 960nsec (*1) wait time until data presented at Data Bus will be written to internal register. This bit indicates wait time, in which access to register is prohibited. When this bit can be read as "1", don't access the register.

*1) About 1.6µsec in case of YMF715/715B.

default : 00h

1-4. Data Registers

This section describes all FM-synthesizer data registers of YMF715x (OPL3-SA3). These data registers are compatible with YMF289B (OPL3-L) and readable. Note that data regsigers of YMF262 (OPL3) are not readable. All registers are cleared except index C0-C8h, CHR and CHL bits is set to "1" after power-on-reset.

LSI TEST : (array0,1)

00-	D7	D6	D5	D4	D3	D2	D1	D0
01h	LSI TEST							

LSI TEST

These two registers are used for LSI testing . All bits should be left "0".

default : 00h

TIMER1/2 (R/W) : (array0)

index	D7	D6	D5	D4	D3	D2	D1	D0
02h	TIMER 1							

index	D7	D6	D5	D4	D3	D2	D1	D0
03h	TIMER 2							

Timer operation is described below. When index 04h (array0), ST1/ST2 bit is set to “1”, the value of timer 1/2 register is loaded into counter 1/2 and counter 1/2 starts to count down. When counter 1/2 occurs underflow, the interrupt signal, IRQn assigned by software is active and status register, FT1/FT2 can be read as “1”. The counter 1/2 reloads the value of timer 1/2 register and continues to count down.

TIMER1

Timer 1 value set : Timer 1 has 80.8 usec resolution. The elapsed time between underflow is expressed as follows.

t1 [msec]=(256-N1) X 0.0808

(N1 : register value)

TIMER2

Timer 2 value set : Timer 2 has 323.1 usec resolution. The elapsed time between underflow is expressed as follows.

t2 [msec]=(256-N2) X 0.3231

(N2 : register value)

default : 00h (index 02, 03h)

TIMER Control (R/W) : (array0)

index	D7	D6	D5	D4	D3	D2	D1	D0
04h	RST	MT1	MT2	-	-	-	ST2	ST1

RST

Timer Reset : When this bit is set to “1”, status register, IRQ, FT1 and FT2 bits are reset. after these flag bits are reset, this RST bit is automatically set to “0”.

MT1

Timer 1 Disable : When this bit is set to “1”, status register flag, FT1 is “0” regardless of timer 1 operation.

MT2

Timer 2 Disable : When this bit is set to “1”, status register flag, FT2 is “0” regardless of timer 2 operation.

ST2

Timer 2 Start : When this bit is set to “1”, timer 2 counter loads the value of timer 2 register (index 03h) and starts to count down. When it is set to “0”, timer 2 counter stops to count.

ST1

Timer 1 Start : When this bit is set to “1”, timer 1 counter loads the value of timer 1 register (index 02h) and starts to count down. When it is set to “0”, timer 1 counter stops to count.

default : 00h

4-Operator Mode Set (R/W) : (array1)

index	D7	D6	D5	D4	D3	D2	D1	D0
04h	-	-	CONNECTION SEL					

CONNECTION SEL

4-Operator mode set : When these bits are set to “1”, the corresponding slot can be used as the 4-operator mode. The relationship between these bits and 4-operator mode channel number is shown below.

index	D5	D4	D3	D2	D1	D0
4-operator mode Channel No.	6	5	4	3	2	1

default : 00h

Expansion Register (R/W) : (array1)

index	D7	D6	D5	D4	D3	D2	D1	D0
05h	-	-	-	-	-	NEW3	*	NEW

NEW3

OPL3-L expansion register : When this bit and NEW bit are set to “1”, extended bit, status register, BUSY bit is available.

NEW

When this bit is set to “1”, registers expanded to YMF262(OPL3) from YMF3812(OPLII), i.e. register array 1 is available. Notice that should be set NEW bit to “0”, when the application software operates in OPLII mode, i.e. only register array 0 is available, because the sound data could fail to be available in this mode.

Notice) The bit marked * indicate that this can be read/written but is not effective.

default : 00h

Keyboard Split Selection (R/W) : (array0)

index	D7	D6	D5	D4	D3	D2	D1	D0
08h	-	NTS	-	-	-	-	-	-

NTS

Keyboard Split : Rate scaling is performed by splitting 8 octaves into 16 parts. This bit determines the keyboard split separation points.

“0” : determined by the second bit of the F_number

“1” : determined by the MSB of the F_number

This is shown in the table below.

NTS=“0”

Block	0		1		2		3		4		5		6		7	
F_MSB	-		-		-		-		-		-		-		-	
F_2nd	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
KSN	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

NTS=“1”

Block	0		1		2		3		4		5		6		7	
F_MSB	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
F_2nd	-		-		-		-		-		-		-		-	
KSN	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Note) Block is “Octave”, F_MSB is “F_number MSB”, F_2nd is “F_number 2nd” and KSN is “Key scale No”.

default : 00h

Slot Register 1 (R/W) : (array0,1)

20-35h	D7	D6	D5	D4	D3	D2	D1	D0
	AM	VIB	EGT	KSR	MULT 3-0			

AM

Tremolo effect : When this bit is set to “1”, a tremolo effect can be applied to the corresponding slot. The tremolo frequency is 3.7Hz. Its depth is determined by index BDh, DAM bit.

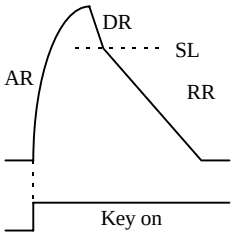
VIB

Vibrato effect : When this bit is set to “1”, a vibrato effect can be applied to the corresponding slot. The vibrator modulation frequency is 6.0Hz. Its depth is determined by index BDh, DVB bit.

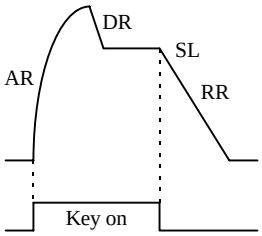
EGT

Non-percussive sound : This bit determines whether percussive sound or non percussive sound. The envelope wave form of each mode is shown below.

a) Percussive sound



b) Non-percussive sound



KSR

Rate Key Scale : Setting this bit to “1” performs the rate key scaling. “Rate key scale” simulates the phenomena that rising time (falling time) of sound becomes faster as the note of acoustic instrument is higher.

Note) Relation between set value and actual time

The actual ATTACK/DECAY/RELEASE time is the sum of Attack Rate : AR/Decay Rate : DR/Release Rate : RR and the key scaling offset , R_{of}, shown below. The key scaling offset is specified as follows.

KSN	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
KSR=0	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
KSR=1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

To find the actual rate time, calculate the RATE value and then refer to the "Rate Value-Actual Time Table". The RATE is specified as follows.

RATE=(RATE Value)X4+R_{of}

when RATE Value is "0", RATE="0". When RATE exceeds 63, RATE=63 is assumed.

MULT 3-0

Frequency Multiplier : These bits specify the multiplier for the frequency determined by index B0-B8h, BLOCK bits and index A0-B8h, F_number bits. These bits determines the frequency ratio between operators.

MULT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Multiplier	1/2	1	2	3	4	5	6	7	8	9	10	10	12	12	15	15

default : 00h

Slot Register 2 (R/W) : (array0,1)

40-	D7	D6	D5	D4	D3	D2	D1	D0
55h	KSL1-0		TL 5-0					

KSL

Level Key Scale : The volume of acoustic instruments decreases as the note of sound is higher. Level key scale simulates this phenomena. This bit gives the attenuation to every octave as follows. The relation between set value and the attenuation is shown below.

KSL	0	1	2	3
Damping	0	3dB/oct	1.5dB/oct	6dB/oct

Note) The actual level attenuation is determined by the value of the higher 4 bits of the F_number. When these bits are "1", the attenuation is specified as follows.

OCT FNUM	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	3.000	6.000	9.000
2	0	0	0	0	3.000	6.000	9.000	12.000
3	0	0	0	1.875	4.875	7.875	10.875	13.875
4	0	0	0	3.000	6.000	9.000	12.000	15.000
5	0	0	1.125	4.125	7.125	10.125	13.125	16.125
6	0	0	1.875	4.875	7.875	10.875	13.875	16.875
7	0	0	2.625	5.625	8.625	11.625	14.625	17.625
8	0	0	3.000	6.000	9.000	12.000	15.000	18.000
9	0	0.750	3.750	6.750	9.750	12.750	15.750	18.750
10	0	1.125	4.125	7.125	10.125	13.125	16.125	19.125
11	0	1.500	4.500	7.500	10.500	13.500	16.500	19.500
12	0	1.875	4.875	7.875	10.875	13.875	16.875	19.875
13	0	2.250	5.250	8.250	11.250	14.250	17.250	20.250
14	0	2.625	5.625	8.625	11.625	14.625	17.625	20.625
15	0	3.000	6.000	9.000	12.000	15.000	18.000	21.000

KSL="2" : 1/2 of the above

KSL="3" : double of the above

TL 5-0

Total Level : These bits set the envelope damping. This can control the volume and modulation rate. Total level is given by the following equation.

TL[dB]=(-24XL5) + (-12XL4) + (-6XL3) + (-3XL2) + (-1.5XL1) + (-0.75XL0)

default : 00h

Slot Register 3 (R/W) : (array0,1)

60-	D7	D6	D5	D4	D3	D2	D1	D0
75h	AR 3-0				DR 3-0			

AR3-0

Attack Rate : These bits specify the attack rate. The set value is 0 to 15. The larger the set value, the shorter the rise time of the sound. Please refer to index 20-35h, Rate Key Scale and "Rate-Actual Time Table" section as regards the actual rate time.

DR3-0

Decay Rate : These bits specify the decay rate. The set value is 0 to 15. The larger the set value, the shorter the time. Please refer to index 20-35h, Rate Key Scale and "Rate-Actual Time Table" section as regards the actual rate time.

default : 00h

Notice) For the envelope, see the "Envelope Rate" section.

Slot Register 4 (R/W) : (array0,1)

80-	D7	D6	D5	D4	D3	D2	D1	D0
95h	SL 3-0				RR 3-0			

SL3-0

Sustain Level : These bit specify sustain level. When index 20-35h, EGT bit is set to "1" (non-percussive), the level output from slot is held after the attenuation reaches the level set in these bits. When EGT bit is set to "0" (percussive), the falling rate is switched to release rate from decay rate after the attenuation reaches the level set in these bits. The sustain level is specified by attenuation as follows.

L[dB]=(-24XSL3) + (-12XSL2) + (-6XSL1) + (-3XSL0)

When all the bits are "1", SL becomes -93dB.

RR3-0

Release Rate : These bits specify the release rate. The set value is 0 to 15. The larger the set value, the shorter the time. Please refer to index 20-35h, Rate Key Scale and "Rate-Actual Time Table" section as regards the actual rate time.

default : 00h

Notice) For the envelope, see the "Envelope Rate" section.

Slot Register 5, 6 (R/W) : (array0,1)

A0-	D7	D6	D5	D4	D3	D2	D1	D0
A8h	F_NUMBER 7-0							

B0-	D7	D6	D5	D4	D3	D2	D1	D0
B8h	-	-	KON	BLOCK 2-0			F_NUM 9-8	

F_NUMBER 9-0

Frequency Information : These bits determine the frequency information for one octave.

KON

Key on : This bit controls synthesize on/off.

"1" : key on

"0" : key off

BLOCK

Octave : This bit specifies the octave information. F_number is determined by tone pitch (frequency) and BLOCK as follows.

$$F\_Number = \frac{(Tone\ Pitch) \times 2^{19}}{2^{BLOCK-1} \times 49.518kHz}$$

Example of F_Number setting (BLOCK value is set to "4"). F_Number can also be set to other than the below.

Note	Frequency	F_Number (Dec)
C	261.6[Hz]	346
C#	277.2[Hz]	367
D	293.7[Hz]	389
D#	311.1[Hz]	412
E	329.6[Hz]	436
F	349.2[Hz]	462
F#	370.0[Hz]	490
G	392.0[Hz]	519
G#	415.3[Hz]	550
A	440.0[Hz]	582
A#	466.2[Hz]	617
B	493.9[Hz]	654
C	523.3[Hz]	693

default : 00h(A0-A8h, B0-B8h)

Rhythm Instrument Sel. (R/W) : (array0)

index	D7	D6	D5	D4	D3	D2	D1	D0
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH

DAM

Tremolo depth : This bit determines the tremolo depth.

DAM="1" : 4.8dB

DAM="0" : 1.0dB

DVB

Vibrato depth : This bit determines the vibrato depth.

DVB="1" : 14cent

DVB="0" : 7cent

One cent is a semi-tone divided by 100.

RHY

RHYTHM Enable : When this bit is set to "1", slots 13 to 18 are enabled to the rhythm mode.

BD, SD, TOM, TC, HH

These bits controls synthesizing of each rhythm. If RHY bit is set to "1" (rhythm mode), the sound of rhythm instrument is synthesized when the bit corresponding to the desired instrument is set to "1". The slot number used by each rhythm instrument is shown below. Set the rate, etc. to match the special features of each musical instrument. The parameters (F_NUMBER, EGT, MULT, TL, AR, DR, SL, RR, and WS) are available. Notice that set KEY ON of slots 13 to 18 to "0".

Rhythm instrument	Slot No.
Bass drum (BD)	13, 16
Snare drum (SD)	17
Tom-tom (TOM)	15
Top cymbal (TC)	18
Hi-hat cymbal (HH)	14

default : 00h

Slot Register 7 (R/W) : (array0,1)

C0-	D7	D6	D5	D4	D3	D2	D1	D0
C8h	*	*	CHR	CHL	FB 2-0			CNT

CHR, CHL

Output Right/Left Channel Selection : These bits control which channel sound data is output from. When CHR/CHL bit is set to "1", sound data is output from R/L channel. In 4-operator mode, notice that operators 1 and 2 are controlled by index C0-C2h and operator 3 and 4 are controlled by C3-C5h. This suggests that the same value setting for CHR/CHL bits of index C0h should be set for CHR/CHL bits of index C3h (index C4h for index C1h and index C5h for index C2h) when you use all of the four operators.

FB 2-0

Feedback : Feedback modulation can be applied to slot 1 of each channel. When feedback modulation is used, string instrument sounds can be produced. The feedback modulation rate is selected by setting these bits. The relation between these bits and modulation rate is shown below.

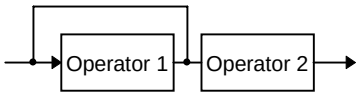
FB	0	1	2	3	4	5	6	7
Rate	0	$\pi/16$	$\pi/8$	$\pi/4$	$\pi/2$	π	2π	4π

CNT

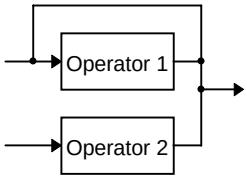
Algorithm Select : This bit selects the algorithm. An "algorithm" is a combination of operators.

(a) 2-operator mode

When CNT bit is set to "0", algorithm 1 is selected. When this bit is set to "1", algorithm 2 is selected. Algorithm can be selected by every channel, i.e. index C0-C8h.



Alogorithm 1



Alogorithm 2

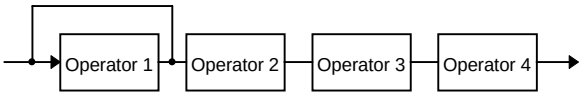
(b) 4-operator mode

4 algorithm types are selectable by setting two CNT bits. The two CNT bits needed in algorithm selection at each channel are summarized in the table below.

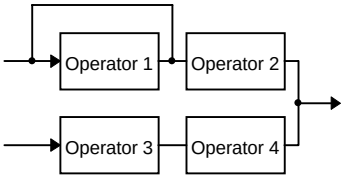
offset array	4-ope mode Channel No.	Set CNT bit register	
		CNT_n	CNT_{n+3}
0	1	C0h	C3h
0	2	C1h	C4h
0	3	C2h	C5h
1	4	C0h	C3h
1	5	C1h	C4h
1	6	C2h	C5h

The algorithm is specified by CNT_n and CNT_{n+3} as follows.

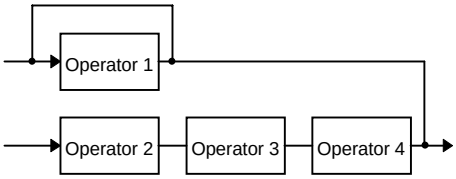
(i) Alogorithm 1 CNT_n="0" CNT_{n+3}="0"



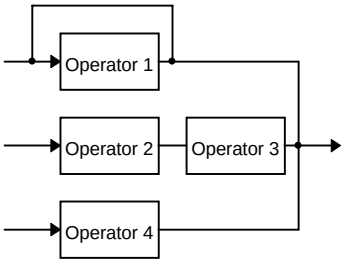
(ii) Alogorithm 2 CNT_n="0" CNT_{n+3}="1"



(iii) Alogorithm 3 CNT_n="1" CNT_{n+3}="0"



(iv) Alogorithm 4 CNT_n="1" CNT_{n+3}="1"



Notice) The bits marked * indicate that these can be read/written but are not effective.

In OPLII mode, i.e. array 1, index 05h, NEW="0", output of FM-synthesizer becomes monaural mode and setting of CHR/CHL bits are ignored. In this case, R and L channel are always enabled and output data are the same.

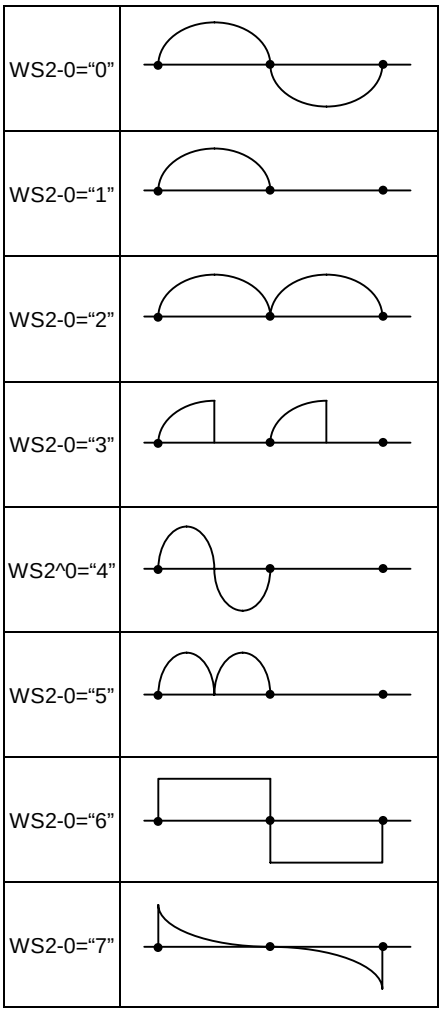
default : 30h

Slot Register 8 (R/W) : (array0,1)

E0-	D7	D6	D5	D4	D3	D2	D1	D0
F5h	-	-	-	-	-	WS 2-0		

WS 2-0

Waveform : The waveform used in FM operation can be set by every slot unit. The relation between these bits and selectable waveform is shown below. In OPLII mode, i.e. array 1, index 05h, NEW="0", only WS 2-0= "0"-"3" can be selected.

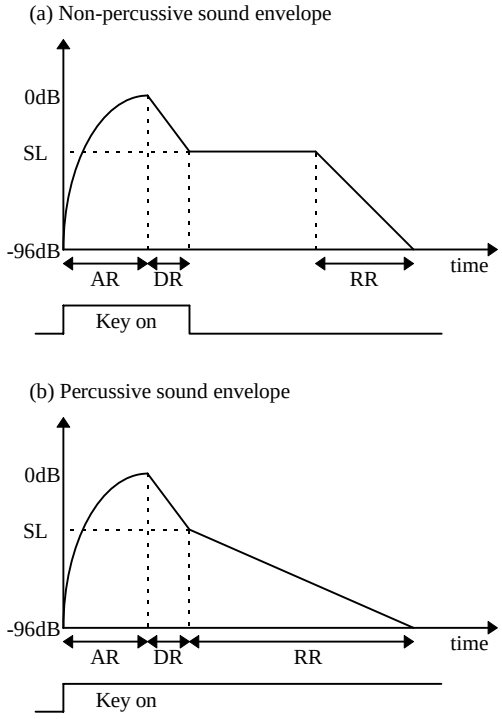


default : 00h

1-5. Envelope Rate

In case of non-percussive sound envelope, the envelope has a dynamic range of 96 dB (resolution : 0.1875 dB). After index B0-B8h, KON bit is set to "1", the level changes exponentially to 0 dB in attack time. When the level reaches 0 dB, envelope is switch to falling from rising and the level is attenuated linearly to sustain level in decay time. The level is held at sustain level until KON bit will be set to "0". When KON bit is set to "0", the level is attenuated to -96 dB in release time.

In case of percussive sound envelope, after KON bit is set to "1", the level changes exponentially to 0 dB in attack time. When the level reaches 0 dB, envelope is switch to falling from rising and the level is attenuated linearly to sustain level in decay time. When the level reaches sustain level, the level is attenuated linearly to -96dB in release time regardless of value of KON bit.



The following are Actual Time Tables of attack and decay/release rate.

(a) Attack Rate

(Units : msec)

Rate	Time (0-100%)	Time (10-90%)
0, 1, 2, 3	infinity	infinity
4	2826.24	1482.75
5	2252.80	1155.07
6	1884.16	991.23
7	1597.44	868.35
8	1413.12	741.38
9	1126.40	577.54
10	942.08	495.62
11	798.72	434.18
12	706.56	370.69
13	563.20	288.77
14	471.04	247.81
15	399.36	217.09
16	353.28	185.34
17	281.60	144.38
18	235.52	123.90
19	199.68	108.54
20	176.76	92.67

21	140.80	72.19
22	117.76	61.95
23	99.84	54.27
24	88.32	46.34
25	70.40	36.10
26	58.88	30.98
27	49.92	27.14
28	44.16	23.17
29	35.20	18.05
30	29.44	15.49
31	24.96	13.57
32	22.08	11.58
33	17.60	9.02
34	14.72	7.74
35	12.48	6.78
36	11.04	5.79
37	8.80	4.51
38	7.36	3.87
39	6.24	3.39
40	5.52	2.90
41	4.40	2.26
42	3.68	1.94
43	3.12	1.70
44	2.76	1.45
45	2.20	1.13
46	1.84	0.97
47	1.56	0.85
48	1.40	0.73
49	1.12	0.61
50	0.92	0.49
51	0.80	0.43
52	0.70	0.37
53	0.56	0.31
54	0.46	0.26
55	0.42	0.22
56	0.38	0.19
57	0.30	0.14
58	0.24	0.11
59	0.20	0.11
60	0.00	0.00
61	0.00	0.00
62	0.00	0.00
63	0.00	0.00

(b) Decay/Release Rate

(Units : msec)

Rate	Time (0-100%)	Time (10-90%)
0, 1, 2, 3	infinity	infinity
4	39280.64	8212.48
5	31416.32	6574.08
6	26173.44	5509.12
7	22446.08	4730.88
8	19640.32	4106.24
9	15708.16	3287.04
10	13086.72	2754.56
11	11223.04	2365.44
12	9820.16	2053.12
13	7854.08	1643.52
14	6543.36	1377.28
15	5611.52	1182.72
16	4910.08	1026.56
17	3927.04	821.76
18	3271.68	688.64
19	2805.76	591.36
20	2455.04	513.28
21	1936.52	410.88
22	1635.84	344.34
23	1402.88	295.68
24	1227.52	256.64
25	981.76	205.44
26	817.92	172.16
27	701.44	147.84
28	613.76	128.32
29	490.88	102.72
30	488.96	86.08
31	350.72	73.92
32	306.88	64.16
33	245.44	51.36
34	204.48	43.04
35	175.36	36.96
36	153.44	32.08
37	122.72	25.68
38	102.24	21.52
39	87.68	18.48
40	76.72	16.04
41	61.36	12.84
42	51.12	10.76
43	43.84	9.24
44	38.36	8.02
45	30.68	6.42
46	25.56	5.38
47	21.92	4.62
48	19.20	4.02
49	15.36	3.22
50	12.80	2.68
51	10.96	2.32
52	9.60	2.02
53	7.68	1.62
54	6.40	1.35
55	5.48	1.15
56	4.80	1.01
57	3.84	0.81
58	3.20	0.69
59	2.74	0.58
60	2.40	0.51
61	2.40	0.51
62	2.40	0.51
63	2.40	0.51

1-6. Register Setting Manner

YMF715x (OPL3-SA3) FM-synthesizer block has 36 sine-wave generators. The FM-synthesizer modulates frequency using these sine-wave. The sine-wave generators is called an "*operator*" or "*slot*". One sound generated by combining two or four operators is called an "*channel*". These are two kind of register: one is controlled by every slot unit, another is controlled by every channel unit.

(a) Register setting in slot units

Index 20-35h, 40-55h, 60-75h, 80-95h and E0-F5h registers are controlled by every slot unit. Registers address x6h, x7h, xEh, and xFh does not exit. The following is example of register address.

Register Index							
20h	21h	22h	23h	24h	25h	-	-
28h	29h	2Ah	2Bh	2Ch	2Dh	-	-
30h	31h	32h	33h	34h	35h		

(b) Slot number

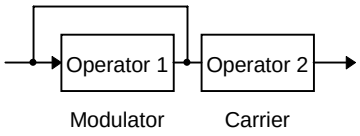
The 36slots are numbered 1 to 36, which are called "*Slot Number*". The correspondence between Slot Number and register address is determined as follows.

Slot Num.	Register Address (Array 0)				
1	20h	40h	60h	80h	E0h
2	21h	41h	61h	81h	E1h
3	22h	42h	62h	82h	E2h
4	23h	43h	63h	83h	E3h
5	24h	44h	64h	84h	E4h
6	25h	45h	65h	85h	E5h
7	28h	48h	68h	88h	E8h
8	29h	49h	69h	89h	E9h
9	2Ah	4Ah	6Ah	8Ah	EAh
10	2Bh	4Bh	6Bh	8Bh	EBh
11	2Ch	4Ch	6Ch	8Ch	ECh
12	2Dh	4Dh	6Dh	8Dh	EDh
13	30h	50h	70h	90h	F0h
14	31h	51h	71h	91h	F1h
15	32h	52h	72h	92h	F2h
16	33h	53h	73h	93h	F3h
17	34h	54h	74h	94h	F4h
18	35h	55h	75h	95h	F5h
19	20h	40h	60h	80h	E0h
20	21h	41h	61h	81h	E1h
21	22h	42h	62h	82h	E2h
22	23h	43h	63h	83h	E3h
23	24h	44h	64h	84h	E4h
24	25h	45h	65h	85h	E5h
25	28h	48h	68h	88h	E8h
26	29h	49h	69h	89h	E9h
27	2Ah	4Ah	6Ah	8Ah	EAh
28	2Bh	4Bh	6Bh	8Bh	EBh
29	2Ch	4Ch	6Ch	8Ch	ECh
30	2Dh	4Dh	6Dh	8Dh	EDh
31	30h	50h	70h	90h	F0h
32	31h	51h	71h	91h	F1h
33	32h	52h	72h	92h	F2h
34	33h	53h	73h	93h	F3h
35	34h	54h	74h	94h	F4h
36	35h	55h	75h	95h	F5h

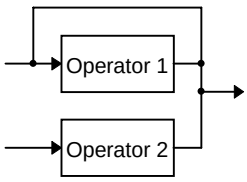
(c) Slot Number and Channel in 2 -operator Mode

In the 2-operator mode, one FM sound (one channel) is generated using 2 slots. Therefore, 18 channels are generated in 2-operator mode. Channels are numbered same as slot number. These number are called "*Channel Number*". In two-operator mode, two algorithm are available as follows.

Alogorithm 1



Alogorithm 2



The correspondence between channel number and slot number is shown as follows.

offset array	Slot Number		Channel Number
	Operator 1	Operator 2	
0	1	4	1
	2	5	2
	3	6	3
	7	10	4
	8	11	5
	9	12	6
	13	16	7
	14	17	8
	15	18	9
1	19	22	10
	20	23	11
	21	24	12
	25	28	13
	26	29	14
	27	30	15
	31	34	16
	32	35	17
	33	36	18

In case of algorithm 2, any slot of 2 slots can correspond to operator 1 (operator 2). However, in case of algorithm 1 the timbre depend on which slot is the modulator (which slot is carrier). Therefore, be careful about slot number.

(d) Register setting in channel units

- 2-operator mode -

Index A0-A8h, B0-B8h and C0-C8h registers are controlled every channel unit. The correspondence between channel number and register address is determined as follows.

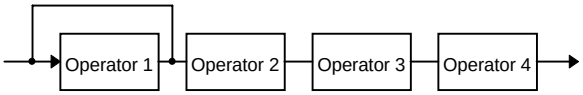
Slot Num.	Register Address (Array 0)		
1	A0h	B0h	C0h
2	A1h	B1h	C1h
3	A2h	B2h	C2h
4	A3h	B3h	C3h
5	A4h	B4h	C4h
6	A5h	B5h	C5h
7	A6h	B6h	C6h
8	A7h	B7h	C7h
9	A8h	B8h	C8h

Slot Num.	Register Address (Array 1)		
10	A0h	B0h	C0h
11	A1h	B1h	C1h
12	A2h	B2h	C2h
13	A3h	B3h	C3h
14	A4h	B4h	C4h
15	A5h	B5h	C5h
16	A6h	B6h	C6h
17	A7h	B7h	C7h
18	A8h	B8h	C8h

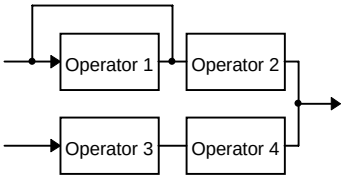
(e) Slot Number and Channel in 4-operator Mode

In 4-operator mode, one FM sound (one channel) is generated using 4 slots. 6 channels are generated using 24 slots in 4-operator mode. In 4-operator mode, 4 algorithm are available as follows.

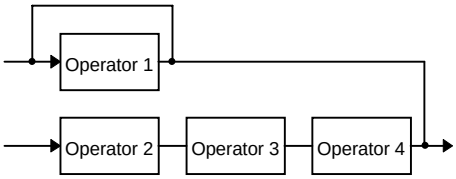
(i) Alogorithm 1



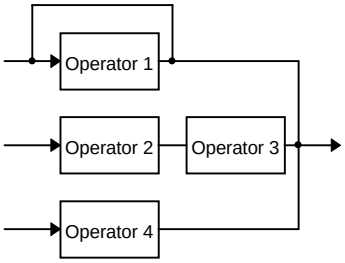
(ii) Alogorithm 2



(iii) Alogorithm 3



(iv) Alogorithm 4



In 4-operator mode, the correspondence between slot number and each operator (operator 1, 2, 3 or 4) is determined as follows.

offset array	Slot Number				Channel Number
	Operator 1	Operator 2	Operator 3	Operator 4	
0	1	4	7	10	1
	2	5	8	11	2
	3	6	9	12	3
1	19	22	25	28	4
	20	23	26	29	5
	21	24	27	30	6

(f) Register setting in channel units

- 4-operator mode -

Index A0-A2h, B0-B2h and C0-C2h registers are controlled by every channel unit. However, index C3-C5h, CNT bits are used as algorithm parameter (refer to description of CNT bit). The correspondence between channel number and register address is determined as follows.

Slot Num.	Register Address (Array 0)		
1	A0h	B0h	C0h
2	A1h	B1h	C1h
3	A2h	B2h	C2h
-	Register Address (Array 1)		
4	A0h	B0h	C0h
5	A1h	B1h	C1h
6	A2h	B2h	C2h

(g) Rhythm slot number

The FM-synthesizer block can generate 5 rhythm instruments (bass drum, snare drum, tom-tom, top cymbal and hi-hat cymbal) using 6 slots. Rhythm slot number are determined to 13-18. Please refer to Data Register section.

(h) Summary

How all 36 slots are used is summarized below.

(i) Slot number 1-12 are used in 2-operator mode or 4-operator mode.

(ii) Slot number 13-18 are used in 2-operator mode or rhythm mode.

(iii) Slot number 19-30 are used in 2-operator mode or 4-operator mode.

(iv) Slot number 31-36 are used in only 2-operator mode.

2. Sound Blaster Pro Register Descriptions

The following are the detail descriptions of Sound Blaster Pro block that are shown in YMF715x (OPL3-SA3) specification. The Sound Blaster Pro block is compatible with the standarad game on DOS application in regarad to audio data playback mainly and de facto standarad in sound card market.

2-1. Register Interface

The following are the Sound Blaster Pro block registers of YMF715x (OPL3-SA3) which is de facto standard on game applications.

SB base+0	R	FM Status Register port
SB base+0	W	FM Address Register port (array 0)
SB base+1	R/W	FM Data Register port
SB base+2	W	FM Address Register port (array 1)
SB base+3	R/W	FM Data Register port
SB base+4	W	Mixer Address Register
SB base+5	R/W	Mixer Data Register
SB base+6	W	DSP Reset Register
SB base+8	R	FM Status Register port
SB base+8	W	FM Address Register port (array 0)
SB base+9	R/W	FM Data Register port
SB base+A	R	DSP Read Data Register
SB base+C	W	DSP Write Command Data Register
SB base+C	R	DSP Write-buffer Status Register
SB base+E	R	DSP Read-buffer status port

2-2. Register Descriptions

This section describes all the Sound Blaster pro compatible registers.

FM-synthesizer Status Register (R):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	Stauts Register							

FM-synthesizer Address Register(array0) (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	Address Register (array 0)							

FM-synthesizer Data Register(array0) (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+1h	Data Register (array 0)							

FM-synthesizer Address Register(array1) (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+2h	Address Register (array 1)							

FM-synthesizer Data Register(array1) (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+3h	Data Register (array 1)							

FM-synthesizer Status Register (R):

port	D7	D6	D5	D4	D3	D2	D1	D0
+8h	Stauts Register							

FM-synthesizer Address Register(array0) (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+8h	Address Register (array 0)							

FM-synthesizer Data Register(array0) (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+9h	Data Register (array 0)							

These register are mapped to the appropriate FM-synthesizer. Please refer to the “FM-synthesizer descriptions”.

Mixer Address Register (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+4h	Mixer Address 7-0							

Mixer Address 7-0

This register is used to specify the mixer address. This register should be written before any data is accessed from the mixer registers.

Mixer Data Register (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+5h	Mixer Data 7-0							

Mixer Data 7-0

This register is read/written and provides the access to the mixer register depending on the index address specified in the mixer address register, port+4h.

DSP Reset Register (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+6h	DSP RESET							

DSP RESET

When bit [0] of this register is set to “1” and set to “0” after waiting 3.3 usec, the Sound Blaster Pro block will be reset.

DSP Read Data Register (R):

port	D7	D6	D5	D4	D3	D2	D1	D0
+Ah	DSP Read Data 7-0							

DSP Read Data 7-0

This register is for reading the Data/Command response. Before reading this port, make sure that the Read-buffer status port (port+ Eh) bit [7] is 1.

DSP Write Command Data Register (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+Ch	COMMAND Data 7-0							

COMMAND Data 7-0

This register is used as the write command/data register for writing.

DSP Write-buffer Status Register (R):

port	D7	D6	D5	D4	D3	D2	D1	D0
+Ch	Write-buffer Status							

Write-buffer status

This register is used as the write-buffer status for reading. Before writing this register, read this port and make sure that bit [7] is “0”.

2-3. Mixer Register Descriptions

This section describes the mixer registers in the Sound Blaster Pro compatible block. The table below is the register mapping of the Sound Blaster Pro mixer.

Table 2-1 Sound Blaster Pro Mixer Register Mapping

Index	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset Mixer							
04h	Voice Vol. Lch			-	Voice Vol. Rch			
0Ah	-	-	-	-	-	MIC Vol.		-
0Ch	-	-	Input Filter	-	Low Pass Filter	Input Source		-
0Eh	-	-	Output Filter	-	-	-	Stereo SW	-
22h	Master Vol. Lch			-	Master Vol. R			-
26h	MIDI Vol. Lch			-	MIDI Vol. Rch			-
28h	CD Vol. Lch			-	CD Vol. Rch			-
2Eh	Line Vol. Lch			-	Line Vol. Rch			-

Notice that Bits marked ▭ indicate that these can be read and written but are not effective.

Reset Mixer(W):

index	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESET MIXER							

RESET MIXER

Writing any value to this register will reset the Sound Blaster Pro Mixer Register.

Voice Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
04h	Voice Vol. Lch			-	Voice Vol. Rch			-

Voice Vol. L/Rch

Voice Volume Control : These bits determine the gain level for the left/right channel of the Voice in 8 steps.

default : 99h

MIC Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	-	-	-	-	-	MIC Vol.		-

MIC Vol.

These bit can be read/written but are not effective, so MIC volume control is not supported.

default : 11h

Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	-	-	Input Filter	-	Low Pass Filter	Input Source		-

Input Filter, Low Pass Filter, Input Source

These bit can be read/written but are not effective, so the capture feature is not supported in Sound Blaster Pro.

default : 11h

Output Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	-	-	Output Filter	-	-	-	Stereo SW	-

Output Filter, Stereo SW

When Stereo SW bit is set to “1”, output is Stereo mode, when this bit is set to”0”, output is Mono mode.

default : 11h

Master Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
22h	Master Vol. Lch			-	Master Vol. Rch			-

Master Vol. L/Rch

Master Volume Control : These bits determine the gain level for the left/right channel of the master in 8 steps.

default : 11h

MIDI Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
26h	MIDI Vol. Lch			-	MIDI Vol. Rch			-

MIDI Vol. L/Rch

MIDI Volume Control : These bits determine the gain level for the left/right channel of the MIDI in 8 steps.

default : 99h

CD Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
28h	CD Vol. Lch			-	CD Vol. Rch			-

CD Vol. L/Rch

CD Volume Control : These bits determine the gain level for the left/right channel of the CD in 8 steps.

default : 11h

LINE Volume Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	LINE Vol. Lch			-	LINE Vol. Rch			-

LINE Vol. L/Rch

LINE Volume Control : These bits determine the gain level for the left/right channel of the LINE in 8 steps.

default : 11h

The actual values written to the Master Vol., MIDI Vol., CD Vol. and Line Vol. are based on the Table 2-2 shown below. When read, the actual value cannot be read --- the value written to each register is read instead.

Table 2-2 Master Volume vs. Each Volume

Master vs. Voice, CD, and Line Volume Table

		Voice Vol. (04h), CD Vol. (28h), Line Vol. (2Eh)							
		0	1	2	3	4	5	6	7
	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-28.5dB	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB
	2	mute	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB
	3	mute	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB
	4	mute	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB
	5	mute	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB	0dB
	6	mute	-3.0dB	0dB	0dB	0dB	0dB	0dB	0dB
	7	mute	0dB	0dB	0dB	0dB	0dB	0dB	0dB

Master vs. MIDI Volume Table

		MIDI Vol. (26h)							
		0	1	2	3	4	5	6	7
	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-24.0dB	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB
	2	mute	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB
	3	mute	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB
	4	mute	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	5	mute	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	6	mute	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	7	mute	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB

Sound Blaster Pro Mixer registers correspond to the CODEC Mixer registers as follows. The default state of the Sound Blaster Mixer registers are as follows.

Sound Blaster Pro Mixer register vs. CODEC Mixer register

Sound Blaster Pro	CODEC
LINE Vol.	LINE Vol.
CD Vol.	AUX1 Vol.
MIDI Vol.	AUX2 Vol.

Sound Blaster Pro	Mixer Default Value
Master Vol.	(99h)
MIDI Vol.	+4.5 [dB] (99h)
Voice Vol.	0 [dB] (99h)
LINE Vol.	mute (11h)
CD Vol.	mute (11h)

2-4. DSP Command

Listed below are the supported DSP commands defined by Sound Blaster Pro. Notice the supported commands are compatible with the standarad game on DOS application in regarad to audio data playback mainly.

CMD	Support	Function
10h	o	8 bit direct mode digitized sound I/O output
14h	o	8 bit single-cycle DMA mode digitized sound output
16h	*	8 bit to 2 bit ADPCM single-cycle DMA mode digitized sound output
17h	*	8 bit to 2 bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
1Ch	o	8 bit auto-init DMA mode digitized sound output
1Fh	*	8 bit to 2 bit ADPCM auto-init DMA mode digitized sound output with ref. byte
20h	*	8 bit direct mode single byte digitized sound input
24h	*	8 bit single-cycle DMA mode digitized sound input
2Ch	*	8 bit auto-init DMA mode digitized sound input
30h	o(*)	Polling mode MIDI input
31h	o(*)	Interrupt mode MIDI input
34h	o(*)	UART polling mode MIDI I/O
35h	o(*)	UART interrupt mode MIDI I/O
36h	o(*)	UART polling mode MIDI I/O with time stamping (MIDI data can not be received)
37h	o(*)	UART interrupt mode MIDI I/O with time stamping (MIDI data can not be received)
38h	o(*)	MIDI output
40h	o	Set digitized sound transfer Time Constant
48h	o	Set DSP block transfer size
74h	o	8 bit to 4 bit ADPCM single-cycle DMA mode digitized sound output
75h	o	8 bit to 4 bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
76h	*	8 bit to 3 bit ADPCM single-cycle DAM mode digitized sound output
77h	*	8 bit to 3 bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
7Dh	o	8 bit to 4 bit ADPCM auto-init DMA mode digitized sound output with ref. byte
7Fh	*	8 bit to 3 bit ADPCM auto-init DMA mode digitized sound output with ref. byte
80h	o	Pause DAC for a duration
90h	o	8 bit high-speed auto-init DMA mode digitized sound output
91h	o	8 bit high-speed single-cycle DMA mode digitized sound output
98h	*	8 bit high-speed auto-init DMA mode digitized sound input
99h	*	8 bit high-speed single-cycle DMA mode digitized sound input
A0h	*	Set input mode to mono
A8h	*	Set input mode to stereo
D0h	o	Pause 8 bit DMA mode digitized sound I/O
D1h	*	Turn on speaker
D3h	*	Turn off speaker
D4h	o	Continue 8 bit DMA mode digitized sound I/O
D8h	*	Get speaker status
DAh	o	Exit 8 bit auto-init DMA mode digitized sound I/O
E1h	o	Get DSP version number

Note:

1) The commands marked "*" are performed in state-machine, but they are not effective.
2) Additional undocumented commands are included.
3) YMF715/715B are not supported the commands marked "(*)".

3. CODEC Register Descriptions

The following are the detail descriptions of YMF715x (OPL3-SA3) CODEC registers that are shown in YMF715x (OPL3-SA3) specifcation.

3-1. General Description

YMF715x (OPL3-SA3) CODEC is the integrated circuit for performing audio data playback/recording in PC enviroment. The functions include stereo Analog-to Digital and Digital-to Analog converters, analog mixer, 5 analog inputs (LINE, AUX#1(CD), AUX#2, MIC, Mono), simultaneous capture and playback at the same sampling frequency (supports the independent sampling frequency by software (device driver)) and programmable timer (resolution 9.969/9.921 usec). 5 analog inputs can be mixed with output of DAC, synthesizer (FM/wavetable/ZV port) and Sound Blaster audio data with volume control. 3 analog inputs (LINE, AUX#1(CD), MIC) can be multiplexed to the ADC. Some data modes are supported including 8/16 bit linear etc.

YMF715x (OPL3-SA3) CODEC has analog mixer that includes attenuation controls for audio sources. Then individual audio source are summed into the mixer. Example, the AUX#1 (CD) mix register provides 32 volume control in 1.5dB steps and mute control. YMF715x (OPL3-SA3) CODEC is compliant with MPC Level-3.

The following are the I/Os for YMF715x (OPL3-SA3) CODEC.

CODEC base+0	R	Configuration Register
CODEC base+3	R	Status Register
CODEC base+4	R/W	Direct Register Index Address port
CODEC base+5	R/W	Direct Register Index Data port
CODEC base+6	R/W	Direct Register Status Register
CODEC base+7	R/W	Direct Register PIO Data port

3-2. Configuration/Status Register

This section describes about confiuration and status register.

Configuration Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	“0”	“0”	IRQ 2-0			DMA 2-0		

This register is used to indicate which resources are assigned; it is a read only register.

IRQ 2-0:

“0” : No interrupt channel is available
“1” : IRQ7 is available
“2” : IRQ9 is available
“3” : IRQ10 is available
“4” : IRQ11 is available
“5”-”7” : reserved.

DMA 2-0:

“0” : No DMA channel is available
“1” : DMA0 is available
“2” : DMA1 is available
“3” : DMA3 is available
“4”-“7” : reserved

Note)
When the CODEC is in Dual DMA mode, only the playback DMA channels are valid and the recording DMA channels are ignored.

Configuration Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+3h	SBHC	“0”	“0”	“0”	“0”	“1”	“0”	“0”

SBHC

If this bit is “0”, the board is in a 16-bit slot, and if this bit is “1”, the board is in an 8-bit slot and DMA0, IRQ10, and IRQ11 are not valid.

D5-0

Always returns 04h.

Table 3-1 CODEC Direct Register Mapping

CODEC Direct Registers (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+4h	INIT	MCE	TRD	Index Address				
+5h	Index Data							
+6h	CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT
+7h	PIO Data							

Table 3-2 CODEC Indirect Register Mapping

CODEC Indirect Registers (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00h	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0
01h	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0
02h	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
03h	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
04h	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
05h	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
06h	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0
07h	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
08h	FM1	FM0	C/L	S/M	CFS2	CFS1	CFS0	CSL
09h	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
0Ah	XTL1*	XTL0*	-	-	-	-	IEN	-
0Bh	COR	PUR	ACI	DRS	“0”	“0”	“0”	“0”
0Ch	MID	MODE	-	-	ID3	ID2	ID1	ID0
0Dh	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
0Eh	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
0Fh	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
10h	OLB	TE	CMCE	PMCE	-	-	-	DACZ
11h	-	-	-	-	-	-	-	HPF*
12h	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
13h	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
14h	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
15h	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
16h	-	-	-	-	-	-	-	-
17h	-	-	-	-	-	-	-	-
18h	-	TI	CI	PI	CU	CO	PO	PU
19h	V2	V1	V0	-	-	CID2	CID1	CID0
1Ah	MIM	-	-	-	MIA3	MIA2	MIA1	MIA0
1Bh	-	-	-	-	-	-	-	-
1Ch	FMT1	FMT0	C/L	S/M	-	-	-	-
1Dh	-	-	-	-	-	-	-	-
1Eh	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
1Fh	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

3-3. CODEC Direct Registers

The Table 3-1 is shown the CODEC direct register mapping. This section describes all the direct registers.

Index Address Register (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+4h	INIT	MCE	TRD	Index Address 4-0				

INIT

CODEC Initialization : During CODEC initialization, this bit is read as “1”. CODEC initialization is caused by changing sampling frequency and clock format and resetting by RESET pin. This bit is read only.

MCE

Mode Change Enable : This bit should be set to “1” whenever the current mode of the YM715x (OPL3-SA3) CODEC is changed. The Data Format (indirect register, index 08, 1Ch) and Interface Configuration (indirect register, index 09h) registers CANNOT be changed unless this bit is set to “1”. The exceptions are index 09h, CEN and PEN bits. The wave output is muted when MCE is set to “1”.

TRD

Transfer Request Disable :

Index Address 4-0

These bits specify the address of the indirect register accessed by the Index Data Register (port+5h). Bit 4 allows access to indirect registers 10-1Fh. Bit 4 is only available MODE=1 (indirect register, index 0Ch). These bits are read/write.

default : 40h

Index Data Register (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+5h	Index Data 7-0							

Index Data 7-0

These bits are the Data register referenced by the Index Address register (port+4h).

default : 00h

Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+6h	CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

CU/L

Capture Upper/Lower Byte ready : This bit indicates whether the capture data ready is for the upper or lower byte of the channel. If this bit is set to “1”, upper byte or any 8-bit ready.

CL/R

Capture Left/Right Sample : This bit indicates whether the capture data waiting is for the left channel or right channel. If this bit set to “1”, left channel or Mono data.

CRDY

Capture Data Ready :

SER

Sample Error : This bit indicates that sample was not serviced in time and an error has occurred. The bit indicates an overrun of capture and underrun for playback.

PU/L

Playback Upper/Lower Byte ready : This bit indicates whether the playback data needed is for the upper or lower byte of the channel. If this bit is set to “1”, upper byte or any 8-bit mode.

PL/R

Playback Left/Right Sample : This bit indicates whether the playback data needed is for the left channel or right channel. If this bit set to “1”, left channel or Mono data.

PRDY

Playback Data Ready :

INT

Interrupt Status : This indicates the status of the internal interrupt logic of YMF715x (OPL3-SA3). This bit is cleared by any write of any value to this register. Indirect register, index 0Ah, IEN bit determines whether the state of this bit is reflected on the IRQn signal pin assigned to the CODEC. If this bit is read as “1”, interrupt active.

default : CCh

PIO Data Register (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+7h	PIO Data							

PIO Data

Playback/Capture Data port : This is the control register where playback/capture data is written/read during programmed I/O data transfers.

default : 80h

3-4. CODEC Indirect Registers

The Table 3-2 is shown the CODEC indirect register mapping. This section describes all the indirect registers. Note that indirect registers, index 10-1Fh are only available when the indirect register, index 0Ch, MODE bit is set to “1”.

Left ADC Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
00h	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0

LSS1-0

Left ADC Input Source Select : These bits determine the analog input source for left channel recording.
“0” : Left LINE - LINEL
“1” : Left AUX1 - AUX1L
“2” : Left MIC - MIC
“3” : Left Line out Loopback

LMGE

Left MIC gain enable : This bit enables the 20dB gain stage of the left mic input signal.

LIG3-0

Left ADC Gain : These bits determine the left channel gain level of the analog source recording volume in -1.5 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (+22.5 dB).

default : 00h

Right ADC Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
01h	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0

RSS1-0

Right ADC Input Source Select : These bits determine the analog input source for right channel recording.
“0” : Right LINE - LINER
“1” : Right AUX1 - AUX1R
“2” : Right MIC - MIC
“3” : Right Line out Loopback

RMGE

Right MIC gain enable : This bit enables the 20dB gain stage of the right mic input signal.

RIG3-0

Right ADC Gain : These bits determine the right channel gain level of the analog source recording volume in -1.5 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (+22.5 dB).

default : 00h

Left Aux#1 Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
02h	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1M

Left Aux#1 Mute : Setting this bit to “1” mutes the left channel of the AUX#1.

LX1G4-0

Left AUX#1 Gain : These bits determine the gain level for the left channel of the AUX#1 in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5dB).

default : 88h

Right Aux#1 Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
03h	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1M

Right Aux#1 Mute : Setting this bit to “1” mutes the right channel of the AUX#1.

RX1G4-0

Right AUX#1 Gain : These bits determine the gain level for the right channel of the AUX#1 in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5 dB).

default : 88h

Left Aux#2 Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
04h	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2M

Left Aux#2 Mute : Setting this bit to “1” mutes the left channel of the AUX#2.

LX2G4-0

Left AUX#2 Gain : These bits determine the gain level for the left channel of the AUX#2 in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5 dB).

default : 05h (+4.5[dB])

Right Aux#2 Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
05h	RX2M	-	-	RX2G4	RX2G3	RX1G2	RX1G1	RX1G0

RX1M

Right Aux#2 Mute : Setting this bit to “1” mutes the right channel of the AUX#2.

RX1G4-0

Right AUX#2 Gain : These bits determine the gain level for the right channel of the AUX#2 in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5 dB).

default : 05h (+4.5[dB])

Left Wave Output Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
06h	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0

LOM

Left Wave Mute : Setting this bit to “1” mutes the left channel of the wave output.

LOA5-0

Left Wave output Gain : These bits determine the gain level for the left channel of the wave output in -1.5 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (-94.5 dB).

default : 80h

Right Wave Output Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
07h	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0

ROM

Right Wave Mute : Setting this bit to “1” mutes the right channel of the wave output.

ROA5-0

Right Wave output Gain : These bits determine the gain level for the right channel of the wave output in -1.5 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (-94.5 dB).

default : 80h

Fs and Playback Data Format (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
08h	FM1	FM0	C/L	S/M	CFS2	CFS1	CFS0	CSL

FM1-0, C/L

The FM1-0 and C/L bits set the audio data format as shown below. If index 0Ch, MODE=0, FM1 is forced low, FM0, and C/L bits are used for both playback and capture. If MODE=1, These bits are only used for playback format, and indirect register, index 1Ch is only used for capture format. Direct register, port+4h, MCE bit or indirect register, index 10h, PMCE bit must be set to “1” to modify these bits.

FM1	FM0	C/L	Remark
0	0	0	Linear, 8-bit unsigned
0	0	1	u-Law, 8bit companded
0	1	0	Linear, 16-bit 2’s complement Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	Reserved
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit 2’s complement Big Endian
1	1	1	Reserved

S/M

Stereo/Mono Select : This bit determines how the audio data streams are formatted. If MODE=0, this bit is used for both playback and capture. If MODE=1, this bit is only used for playback format, and indirect register, index 1Ch is only used for capture format. If this bit is set to “1”, audio data format is Stereo. Direct register, port+4h, MCE bit or indirect register, index 10h, PMCE bit must be set to “1” to modify this bit.

CFS2-0, C2SL

Clock Frequency Divide Select : CFS2-0 bits specify the audio sample frequency for both playback and capture. C2SL bit specifies the clock source used for the audio sample rates for both playback and capture. Direct register, port+4h, MCE bit must be set to “1” to modify these bits.

CFS2-0	Divide	C2SL=0	C2SL=1
“0”	3072	8.0kHz	5.51kHz
“1”	1536	16.0kHz	11.025kHz
“2”	869	27.42kHz	18.9kHz
“3”	768	32.0kHz	22.05kHz
“4”	448	N/A	37.8kHz
“5”	384	N/A	44.1kHz
“6”	512	48.0kHz	33.075kHz
“7”	2560	9.6kHz	6.62kHz

default : 00h

Interface Configuration (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
09h	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN

CPIO

Capture PIO Enable : This bit determines whether the capture data is transferred via DMA or PIO. If this bit is set to “1”, PIO transfers.

PPIO

Playback PIO Enable : This bit determines whether the playback data is transferred via DMA or PIO. If this bit is set to “1”, PIO transfers.

ACAL

Digital Filter Initialize Enable : If this bit is set to “1”, index 0Bh, ACI bit is read as “1” during about 64fs whenever direct register, port+4h, MCE bit changes from “1” to “0” and internal digital filter is initialized. If this bit is set to “0”, ACI bit is read as “0” and internal digital filter is not initialized.

SDC

Single DMA Channel : This bit forces YMF715x (OPL3-SA3) to use one DMA channel. If this bit is set to “1”, single DMA channel mode, and if this bit is set to “0”, dual DMA channel mode.

CEN

Capture Enabled : This bit enables the capture data. This bit may be set to “1”/”0” without setting the MCE bit. If this bit set to “1”, capture enabled.

PEN

Playback Enabled : This bit enables the playback data. This bit may be set to “1”/”0” without setting the MCE bit. If this bit set to “1”, playback enabled.

default : 08h

Pin Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	XTL1	XTL0	-	-	-	-	IEN	-

XTL1-0

These bits can be read/written but are not effective.

IEN

Interrupt Enable : This bit enables the YMF715x (OPL3-SA3) CODEC interrupt. The interrupt will reflect the direct register, port+6h, INT bit.

default : 00h

Error Status and Initialization (RO):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	COR	PUR	ACI	DRS	“0”	“0”	“0”	“0”

COR

Capture overrun : This bit is read as “1” when the capture data has not been read by the host before the next sample arrives. This bit is read as ”1” when an error condition occurs and will not clear until the direct register, port+6h is read.

PUR

Playback Underrun : This bit is read as “1” when the playback data has not arrived from host in time to be played. This bit is read as ”1” when an error condition occurs and will not clear until the direct register, port+6h is read.

ACI

Digital Filter Initialization in-progress : This bit indicates the state of digital filter initialization. If this bit is read as “1”, digital filter initialization is inprogress.

DRS

DRQn status : This bit indicates the current status of the DRQn assigned to YMF715x (OPL3-SA3) CODEC. If this bit is read as “1”, capture or playback DRQn are presently active.

default : 00h

MODE and ID (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	MID	MODE	-	-	ID3	ID2	ID1	ID0

MID

Manufactured ID : This bit is read as ”1” and read only.

MODE

Mode enable : Setting this bit to “1” enables access to indirect registers, index 10-1Fh and their associated features.

ID3-0

CODEC ID : These bits are read as “$(1010)_b$” and read only.

default : 8Ah

Loopback Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE

LBA5-0

Loopback Attenuation : These bits determine the gain level for the loopback in -1.5 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (-94.5 dB).

LBE

Loopback Enable : Setting this bit to “1” enables that the ADC data is digitally mixed with data sent to the DACs.

default : 00h

Playback Upper Base (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-0

Playback Upper Base : This register is the upper byte which represents the 8 MSB of 16 bit playback base register. Reading from this register return the same value which was written. The current count registers cannot be read. If index 0Ch, MODE=0 and index 09h, SDC=1, this register is used for both the playback and capture base registers.

default : 00h

Playback Lower Base (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-0

Playback Lower Base : This register is the lower byte which represents the 8 LSB of 16 bit playback base register. Reading from this register return the same value which was written. The current count registers cannot be read. If index 0Ch, MODE=0 and index 09h, SDC=1, this register is used for both the playback and capture base registers.

default : 00h

Alternate Feature Enable 1 (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
10h	OLB	TE	CMCE	PMCE	-	-	-	DACZ

OLB

Output Level Bit : This bit controls output level.
“0” : Full scale 2.0Vp-p
“1” : Full scale 2.8Vp-p

TE

Timer Enable : Setting this bit to “1” enables the CODEC timer to run and report the interrupt to host at the specified frequency in the timer registers, index 14-15h.

CMCE

Capture Mode Change Enable : This bit should be set to “1” when the stereo/mono and audio data format bits for the capture channel, index 1Ch is changed. Direct register, port+4h, MCE bit should be used to change the sample frequency in index 08h.

PMCE

Playback Mode Change Enable : This bit should be set to “1” when the stereo/mono and audio data format bits for the playback channel, index 08h is changed. Direct register, port+4h, MCE bit should be used to change the sample frequency in index 08h.

DACZ

DAC Zero : This bit will force the output of the playback channel to AC zero.
“0” : Go to center scale
“1” : Hold previous valid sample

default : 00h

Alternate Feature Enable 2 (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
11h	-	-	-	-	-	-	-	HPF

HPF

This bit can be read/written but are not effective.

default : 00h

Left Line Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
12h	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0

LLM

Left Line Mute : Setting this bit to “1” mutes the left channel of the Line.

LLG4-0

Left Line Gain : These bits determine the gain level for the left channel of the Line in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5dB).

default : 88h

Right Line Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
13h	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0

RLM

Right Line Mute : Setting this bit to “1” mutes the right channel of the Line.

RLG4-0

Right Line Gain : These bits determine the gain level for the right channel of the Line in -1.5 dB steps. When all bits are set to “0”, volume is maximum (+12 dB) and when all bits are set to “1”, volume is minimum (-34.5 dB).

default : 88h

Timer Lower/Upper Byte (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
14h	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

index	D7	D6	D5	D4	D3	D2	D1	D0
15h	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TL7-0

Lower Timer Bits : This is the low order byte of the 16-bit timer.

TU7-0

Upper Timer Bits : This is the high order byte of the 16-bit timer. The time base is determined by the clock source selected.
C2SL=0 : 24.5760MHz/245 - 9.969 us
C2SL=1 : 33.8688MHz/336 - 9.921 us

default : 00h (index14-15h)

Notice)
Index 16-17h registers are reserved. Don't access these registers.

Alternate Feature Status (RO):

index	D7	D6	D5	D4	D3	D2	D1	D0
18h	-	TI	CI	PI	CU	CO	PO	PU

TI

Timer Interrupt : This bit indicates that an interrupt is pending from the timer count registers. This bit is reset by writing "0" to it or by writing any value to the status register, port+6h.

CI

Capture Interrupt : This bit indicates that an interrupt is pending from the record DMA count registers. This bit is reset by writing "0" to it or by writing any value to the status register, port+6h.

PI

Playback Interrupt : This bit indicates that an interrupt is pending from the playback DMA count registers. This bit is reset by writing "0" to it or by writing any value to the status register, port+6h.

CU

Capture Underrun : This bit indicates that the host has read more data out of the FIFO than it contained. In this condition, this bit is read as "1" and the last valid byte is read by the host.

CO

Capture Overrun : This bit indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case this bit is read as "1" and the new sample is discarded.

PO

Playback Overrun : This bit indicates that the host attempted to write data into a full FIFO and the data was discarded.

PU

Playback Underrun : This bit indicates that the DAC has run out of data and a sample has been missed.

default : 00h

Version/ID (RO):

index	D7	D6	D5	D4	D3	D2	D1	D0
19h	V2	V1	V0	-	-	CID2	CID1	CID0

V2-0

Version Number : These bits indicate version of YMF715x (OPL3-SA3) CODEC and are read as "$(100)_b$".

CID2-0

CODEC Identification : These bits indicate identification of YMF715x (OPL3-SA3) CODEC and are read as "$(000)_b$"

default : 80h

Mono Input Control (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
1Ah	MIM	-	-	-	MIA3	MIA2	MIA1	MIA0

MIM

Mono Input Mute : Setting this bit to "1" mutes the Mono input.

MIA3-0

Mono Input Gain :These bits determine the gain level for the mono input -3.0 dB steps. When all bits are set to “0”, volume is maximum (0 dB) and when all bits are set to “1”, volume is minimum (-30.0 dB).

default : C0h

Notice)
Index 1Bh register is reserved. Don’t access this register.

Capture Data Format (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	FM1	FM0	C/L	S/M	-	-	-	-

FM1-0, C/L

The FM1-0 and C/L bits set the audio data format as shown below. These bits are only used for capture format in MODE=1. Indirect register. Direct register, port+4h, MCE bit or indirect register, index 10h, CMCE bit must be set to “1” to modify these bits.

FM1	FM0	C/L	Remark
0	0	0	Linear, 8-bit unsigned
0	0	1	u-Law, 8bit companded
0	1	0	Linear, 16-bit 2’s complement Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	Reserved
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit 2’s complement Big Endian
1	1	1	Reserved

S/M

Stereo/Mono Select : This bit determines how the audio data streams are formatted. This bit is only used for capture format in MODE=1. If this bit is set to “1”, audio data format is Stereo. Direct register, port+4h, MCE bit or indirect register, index 10h, CMCE bit must be set to “1” to modify this bit.

default : 00h

Notice)
Index 1Dh register is reserved. Don’t access this register.

Capture Upper Base (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
1Eh	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-0

Capture Upper Base : This register is the upper byte which represents the 8 MSB of 16 bit capture base register. Reading from this register return the same value which was written.

default : 00h

Capture Lower Base (R/W):

index	D7	D6	D5	D4	D3	D2	D1	D0
1Fh	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-0

Capture Lower Base : This register is the lower byte which represents the 8 LSB of 16 bit capture base register. Reading from this register return the same value which was written.

default : 00h

3-5. Digital Filter Initialization

The following are shown YMF715x (OPL3-SA3) CODEC digital filter initialization sequence.

When the register values concerned with Fs or XTAL (indirect register, index 08, 1Ch) are only changed, direct register, port+4h, INIT bit is set to “1” during about 2-3fs if indirect register, index 09h, ACAL bit is set to “1”. If ACAL bit is set to “1”, index 0Bh, ACI bit is read as “1” during about 64fs whenever direct register, port+4h, MCE bit changes from “1” to “0”. ACI bit read as “1” means that digital filter initialization is inprogress. So notice that YMF715x (OPL3-SA3) CODEC needs the wait during this time. If ACAL bit is set to “0”, YMF715x (OPL3-SA3) CODEC digital filter is not initialized.

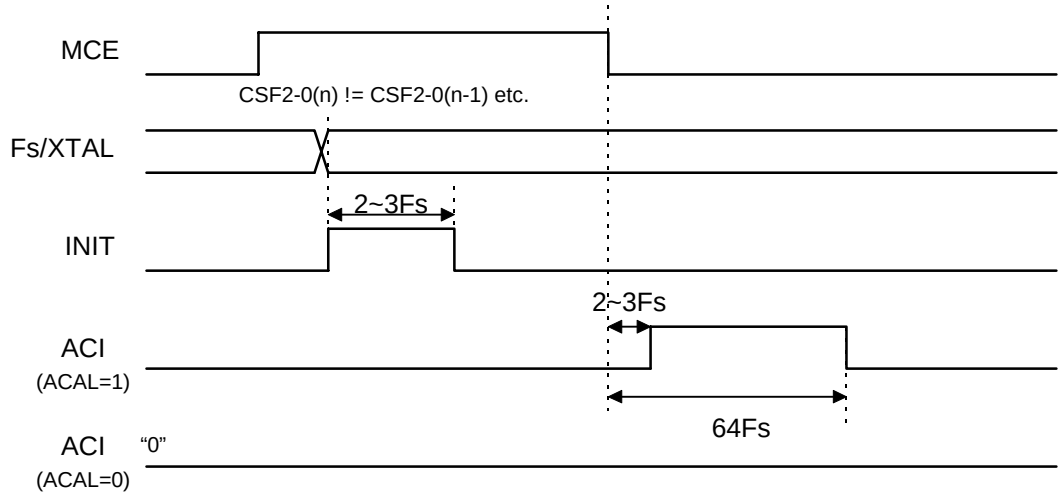


Fig.3-1 YMF715x(OPL3-SA3) CODEC Digital Filter Initialization Chart

4. MPU401 Descriptions

MPU401 is the standard interface for controlling MIDI devices, e.g., wavetable synthesizer YMF721 (OPL4-ML2) etc. from a PC. The YMF715x (OPL3-SA3) has an MPU401 MIDI interface with a 16-byte receive/transmit FIFO. The MIDI output data of the transmit FIFO will be serialized out the TXD pin of the YMF715x (OPL3-SA3). MIDI input data can be received from the RXD pin of the YMF715x (OPL3-SA3). The following are the I/Os for MPU401 compatibility.

MPU base+0	R/W	MIDI Data receive/transmit port
MPU base+1	R	Status Register port
MPU base+1	W	Command Register port

4-1. Register Descriptions

This section describes all the MPU401 compatible registers.

MIDI Data Transmit/Receive Port (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	MIDI Data							

MIDI Data

MIDI Data Write/Read port : This is the port for transmit/receive of MIDI data. During both transmit and receive, it is necessary to watch the status register DSR and DRR bits. The YMF715x (OPL3-SA3) has an internal 16-byte FIFO for transmit/receive of MIDI data.

Status Register Port (R):

port	D7	D6	D5	D4	D3	D2	D1	D0
+1h	DSR	DRR	-	-	-	-	-	-

DSR

Receive Status : When MIDI data is ready, and when a command has been written, this will be “0”. When this bit is “0”, MIDI data must not be read.

DRR

Transmit Status : When MIDI data can be written, this will be “0”. When this bit is “1”, MIDI data may not be written.

default : $(10xx\ xxxx)_b$

Command Register Port (W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+1h	COMMAND Data							

COMMAND Data

Command Data Write : Writing command data to this register will set the DSR bit to “0”, and FEh will be returned to the MIDI data register as an acknowledgment. YMF715x (OPL3-SA3) supports the following commands.

“FFh” : MPU Reset (return the interface to non-UART mode

“3Fh” : Set the interface to UART mode

Note) UART Mode

The UART mode is used to convert parallel data to the serial data required by MIDI. The serial data rate is fixed at 31.25k bps (+/- 1%). The serial data format is that 1 start bit, 8 data bits (LSB fast) and 1 stop bit. After power-on reset, MPU 401 interface is “non-UART mode”. When writing “3Fh” to the command register port, set the interface into “UART mode” and generate an interrupt and status register port, port+1h, DSR bit can be read as “0”. When the MIDI data port is read “FEh” as an acknowledge, the interrupt is reset and DSR bit can be read as “1”. When writing “FFh” to the command register port, set the interface into “non-UART mode (MPU Reset)”.

5. Game Port

Joystick port(Game port) consists of one I/O location, and has the following one read register. Currently the Joystick port is located at 201h in most games software (please refer to YMF715x (OPL3-SA3) specification, “recommended resource data” section).

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JBB2

Joystick B, Button 2

JBB1

Joystick B, Button 1

JAB2

Joystick A, Button 2

JAB1

Joystick A, Button 1

JBCY

Joystick B, Coordinate Y

JBCX

Joystick B, Coordinate X

JACY

Joystick A, Coordinate Y

JACX

Joystick A, Coordinate X

A write to this register, Joystick port(Game port), triggers quad timers. A read from this register returns quad status bits corresponding to the joystick fire buttons and four bits that correspond to the output from the quad timers. Each timer output remains low for a period of time determined by the current joystick portion.

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