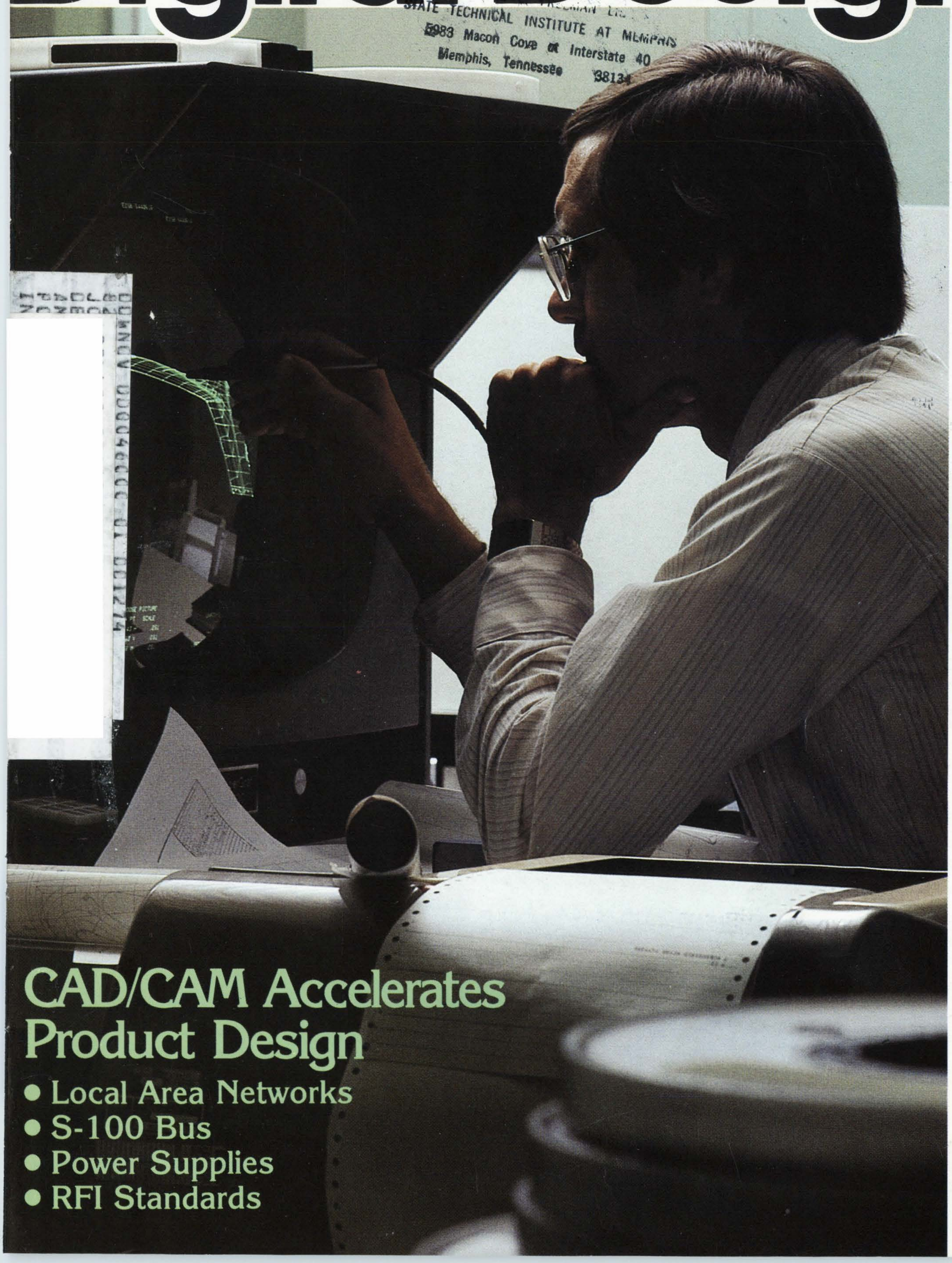
A MORGAN-GRAMPIAN PUBLICATION

Digital Design

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 11/82



CAD/CAM Accelerates Product Design

- Local Area Networks
- S-100 Bus
- Power Supplies
- RFI Standards

VOL. 12
NO. 11

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The 6170 Series 8″ Winchester disk drives have always provided unmatched performance for the lowest unit price in the industry.

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Models 6172 and 6173 have capacities of 24.5 and 40.9 megabytes respectively. They feature a linear voice coil positioner and a brushless DC spindle motor located outside of the sealed head/disk assembly to avoid inducing heat into the HDA, which yields high reliability and extends component life. Interface options allow the OEM to select between SMD, ANSI, and our inexpensive Disk Bus.

The 6170 Series has all the essentials: reliability, high performance, low cost, and immediate availability.

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The CalComp Computer Graphics Glossary

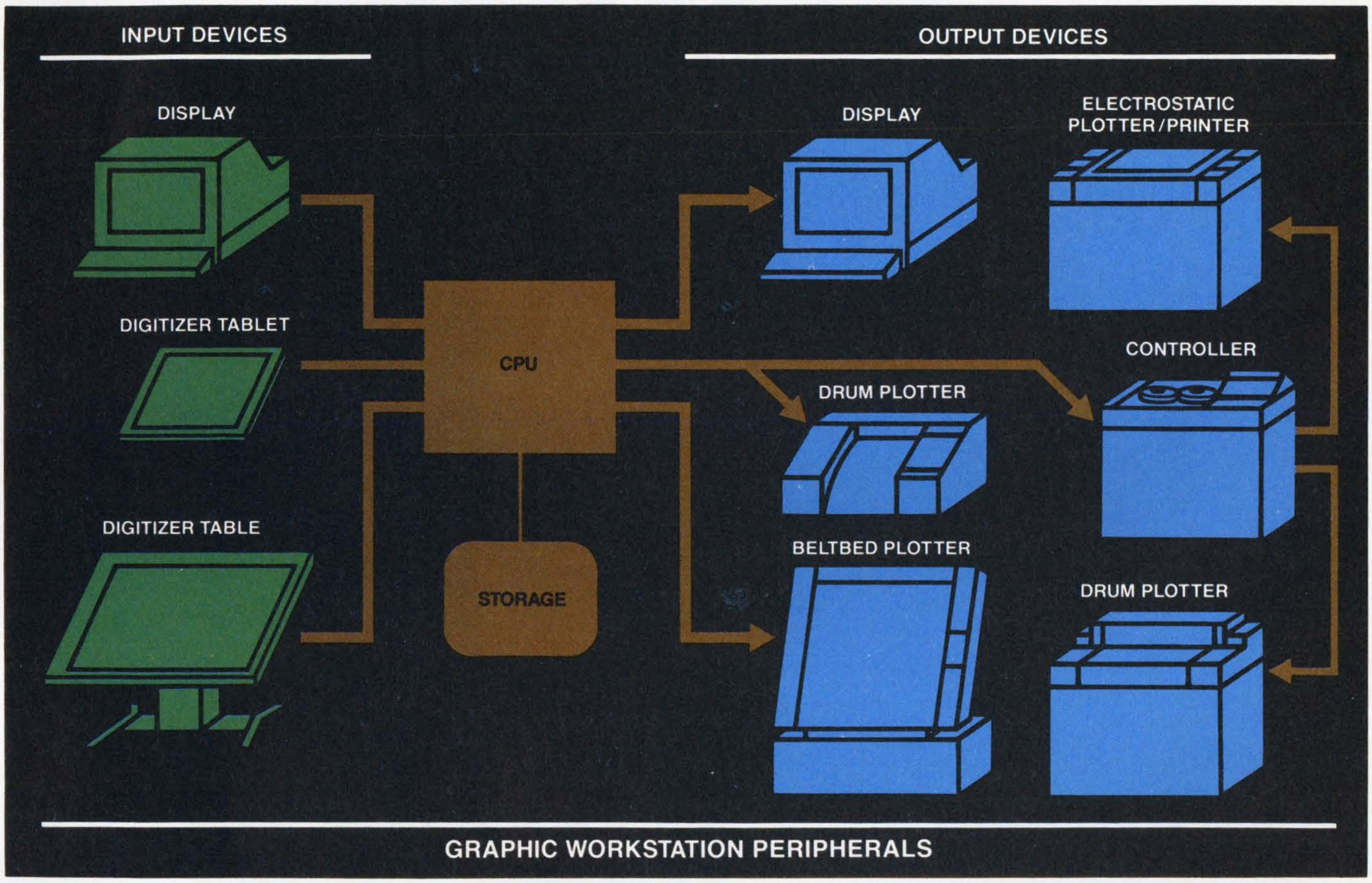
Source: A complete spectrum of computer graphic peripherals from CalComp

In the dynamic world of computer graphic peripherals, only CalComp can offer a complete line of quality products spanning the entire spectrum of input and output devices. Whether you are an OEM systems integrator, a multiple-product end user, or simply trying to build the best possible graphic workstation for a particular application, CalComp is *the* source.

Quality products and attractive new pricing.
CalComp is now offering the "Multi-product Sales Plan" to provide maximum discount leverage. When you agree to buy a specified quantity of plotters, digitizers or displays from CalComp, the same quantity discount applies to all other eligible CalComp products over the life of the agreement. This plan is a major price breakthrough for multiple-product end users and OEMs.

Products for every application.
More and more industries are discovering that computer aided design is a competitive necessity, and the market is expected to quadruple by 1986. Today's graphic workstation environments already include computer rooms, offices, trucks, ships, drilling platforms and more. But unlike so many new companies with single product offerings, CalComp offers more than 40 different products—digitizers—displays—plotters—to allow you to configure a system to meet your needs.

- CalComp offers a wide assortment of digitizers—both tablets and wide area tables—providing exceptional accuracy and high resolution. Solid and backlighted surfaces are available.
- CalComp continues to dominate the pen plotter field, with drum, beltbed and flatbed models. All have outstanding resolution, high throughput, simplicity of operation and dependability.
- A growing force in Electrostatic Plotter/Printers, CalComp offers a full range of EPPs for high quality "quick copies." These are available in floor models and a new rack-mounted mobile unit.
- CalComp has online, offline and combination controllers driving its plotters, including those that can run both pen *and* electrostatic plotters.
- Providing a new definition for the term "interactive," is the new 4000 Series of Vistagraphic™



Displays:
Resolution - 640 x 512, 1024 x 768, 1024 x 1024
Models - Color or Monochrome
CPU - Dual Motorola MC68000

Digitizers:
Tablets - 11" x 11" to 24" x 24"
Tables - 24" x 36" to 44" x 60"

Drum Plotters:
Widths - 11," 36," 54," 72"
Speeds - 4.5, 10, 30 Inches/Second

Flatbed Plotter:
Plotting Area - 48" x 82"
Speed - 30 Inches/Second

Beltbed Plotters:
Plotting Area - 34" x 59" - 52" x 80"
Speed - 30 Inches/Second

Electrostatic Plotter/Printers:
Widths - 11," 22," 36"
Resolution - 100, 200 Dots/Inch

Displays, available in both monochrome and color. Two microprocessors are used, one devoted to display processing and the second for peripherals and communications.

Service protects your investment.
With more than 15,000 graphics systems installed worldwide, CalComp understands how *vital* responsive service is. Backing CalComp's superior parts and labor warranty are over 75 field service offices. And with our Maintenance Alert Program, if problems cannot be solved quickly, we'll call in our senior national technicians to get you back on line without costly delay. Our ability to maintain and service our equipment throughout the world underscores CalComp's commitment to stand behind its products *and* its customers!

Single source simplicity.
For hardware, software, supplies, service and advice, no one even comes close to CalComp as the single source for all your computer graphic peripheral needs.

Write 6 on Reader Inquiry Card

To find out how we can meet your graphics needs, call **800-CALCOMP (800-225-2667).**

For a list of international sales and service offices write:
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P.O. Box 3250, Anaheim, CA 92803.

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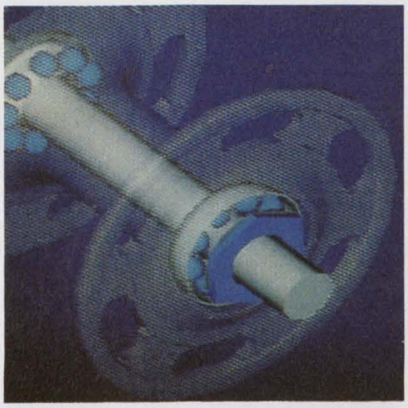
The Graphics People

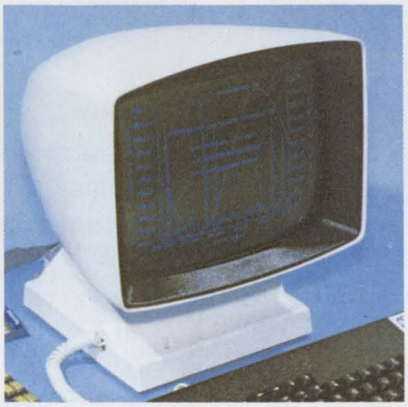
NOVEMBER 1982/VOL. 12, NO. 11

Digital Design



p. 40 (photo courtesy Lexidata)

p. 32 (photo courtesy LH Research)



p. 68 (photo courtesy Andromeda Systems)

Cover

This month's front cover illustrates the use of computer aided design equipment at the Ford Motor Company (photo courtesy of Prime Computer).

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BEACON™ PUTS MORE GRAPHICS AT YOUR FINGERTIPS.

It's a rare graphics system that can produce business graphics and also operate as an engineering work station for under $20,000. The Beacon™ System from Florida Computer Graphics puts it all right at your fingertips.

Using Multi-Processor Architecture (MPA) and 48-bit microcoded firmware, the Beacon System produces virtually instantaneous generation of vectors, arcs, circles, rectangles, and polygon fills. And BeaconBRIGHT™ makes those images far more visible even in brightly lit areas.

With the addition of 640KB of optional graphics memory, Beacon's 640 X 480 resolution can create a 1280 X 960 addressable image, typical of many CAD/CAM applications. This higher resolution, combined with the standard BeaconROAM™ and Zoom features, makes Beacon ideal for many engineering and scientific applications.

Check these unique Beacon features, standard on all models.

- A wide range of true graphics and character graphics including dot addressability, 1X zoom increments (up to 16X), horizontal and vertical scrolling in variable speed, and more.
- A palette of 256 colors; 32 usable at one time (16 in the graphics planes, 16 in the alphanumeric plane).
- Superior ergonomic design. From a display that's *twice as steady* as those advertised as "flicker free" to the monitor that tilts, swivels, and adjusts in height. Beacon leads the way in human-factors engineering.

Beacon works with joysticks, light pens, digitizer tablets, printers or plotters. It also interfaces with slide cameras, color copiers and even large screen video projectors.

For generating either business or engineering graphics, the Beacon System (stand alone or host dependent), offers a spectrum of capabilities unmatched in its price category. To find out more write for our full color literature:

Marketing Communications Manager
Florida Computer Graphics, Inc.
1000 Sand Pond Road, Lake Mary, FL 32746.
Or call (305) 321-3000. In the Continental U.S. outside Florida, dial 1-800-327-3170.

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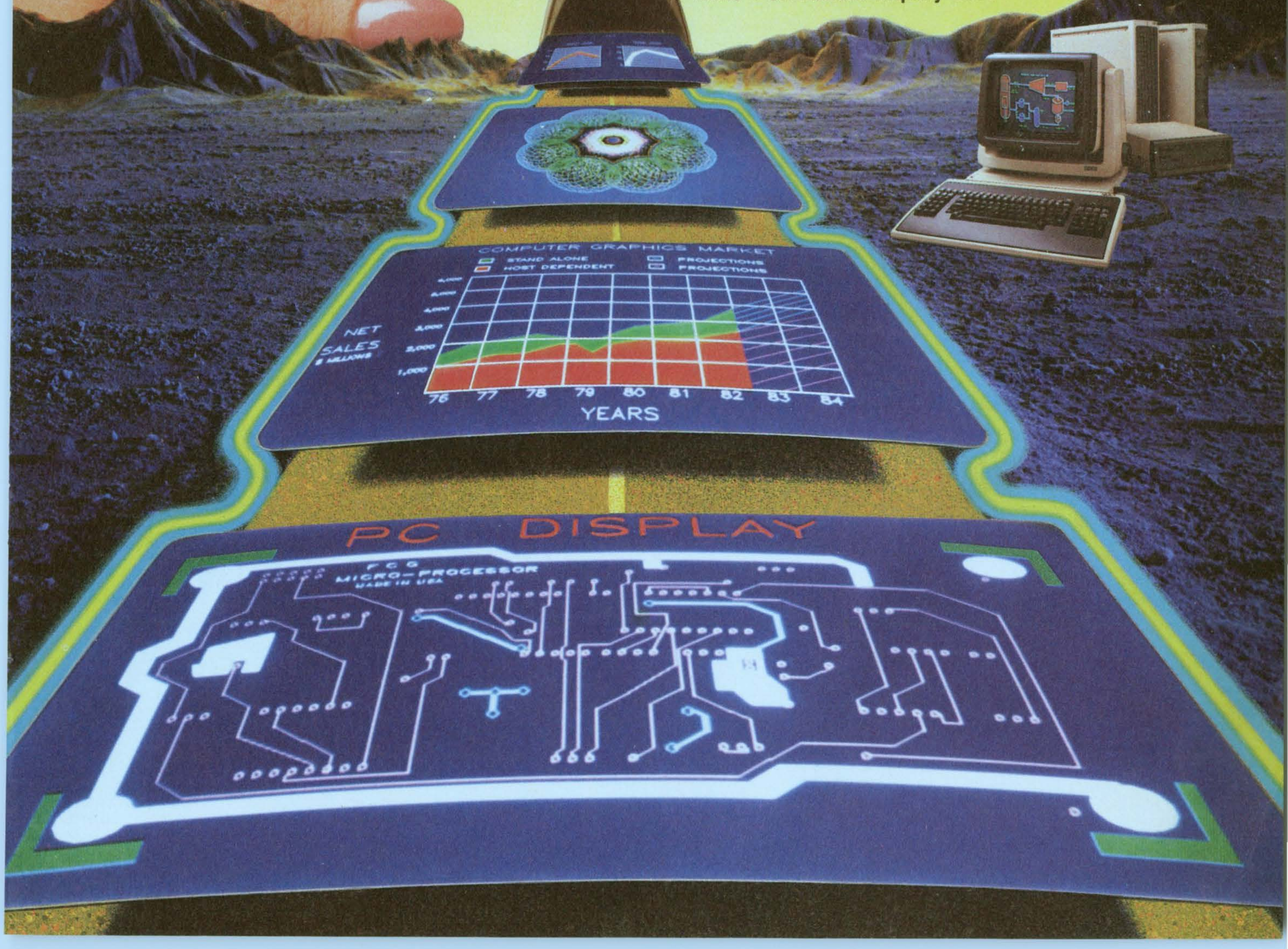
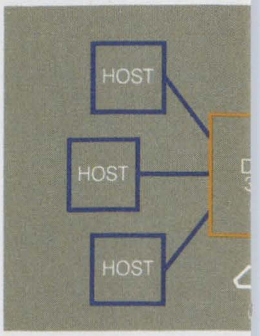
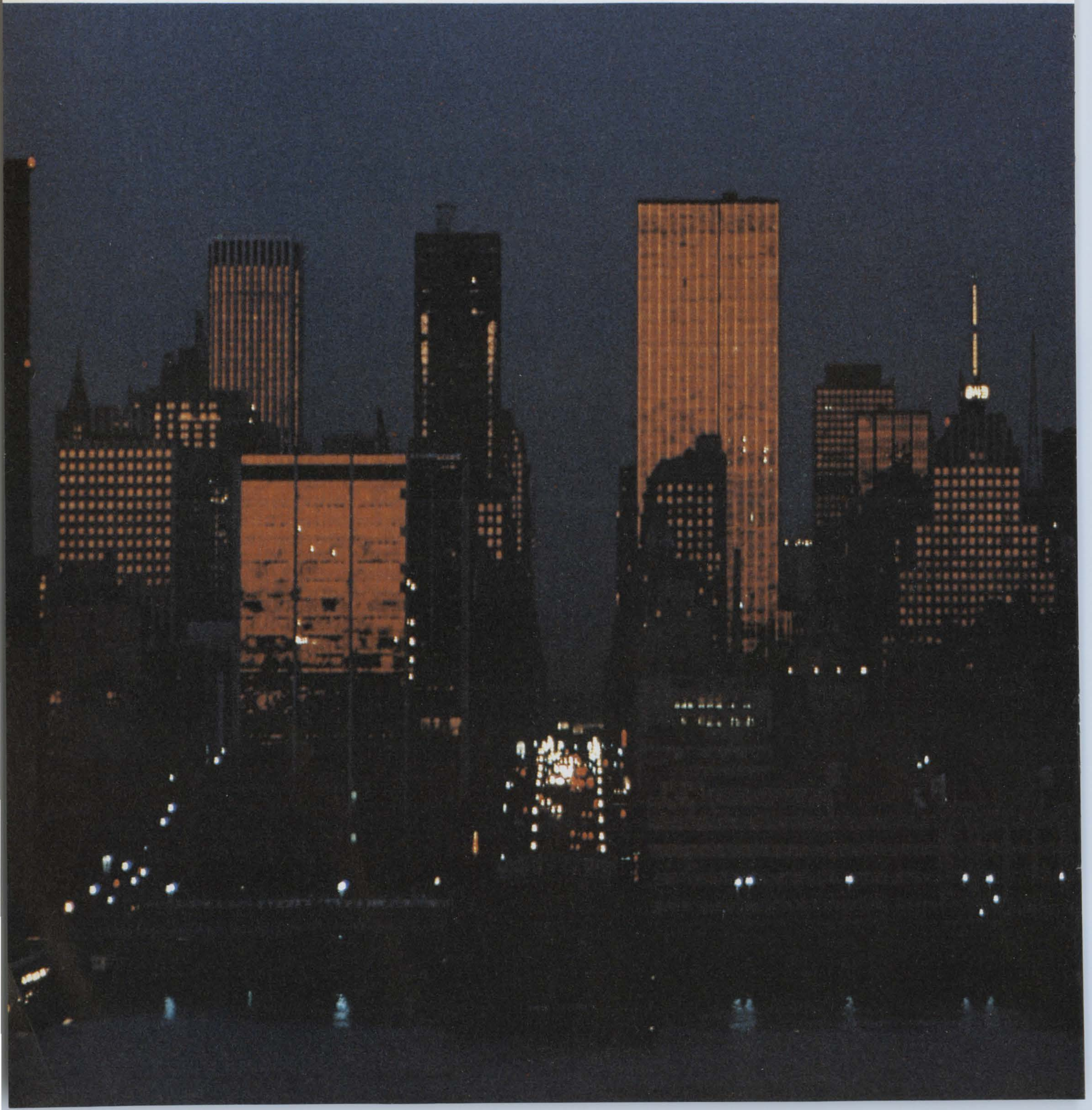


OUR BIG INVENTION FOR BIG BUSINESS

DCA. We're the ones who pioneered the development of a master network processor with host selection—a system especially helpful to larger companies with many terminals accessing several computers. With our 355 Master Network Processor, costs are reduced because unnecessary equipment is eliminated. Any terminal user can tie in with any host computer in the network—resulting in greater flexibility and increased capacity. And all DCA systems are designed with plug-compatible modular hardware, allowing systems to be easily upgraded as networks expand.

But that's just part of the story. Since the beginning, we've been the innovators in solving communications problems systematically. We were the first to make it possible to cost-effectively interface with X.25 standard protocols. This offers you low-cost access to public data networks and to host computers which support





November 30–December 1

CAD/CAM Seminar. Barbizon Plaza Hotel, New York, NY. "Understanding and Using CAD/CAM." Contact: Carol Sapchin, Frost & Sullivan, 106 Fulton St., New York, NY 10038. (212) 233-1080.

December 1–3

Digital Voice & Video Course. Washington, DC. Course No. 451DC. Contact: Continuing Engineering Education, George Washington U., Washington, DC 20052. (800) 424-9773.

December 2–3

Computer Graphics Seminar. Barbizon Plaza Hotel, New York, NY. "Understanding and Using Computer Business Graphics." Contact: Carol Sapchin, Frost & Sullivan, 106 Fulton St., New York, NY 10038. (212) 233-1080.

December 2–5

Personal Electronics And Computer Expo. Baltimore Convention Center, Baltimore, MD. Contact: J. Spargo & Associates, 5205 Leesburg Pike, Suite 308, Falls Church, VA 22041. (703) 931-2321.

December 6–8

Automated Office VI. 6th Annual Conference. Los Angeles, CA. Contact: Dept. PR, NIMR Seminars, PO Box 3727, Santa Monica, CA 90403. (213) 450-0500.

December 6–8

Net 1000 Seminar. New York, NY. Seminar devoted to American Bell's Advanced Information Systems Net 1000 service. Contact: Technology Transfer Institute, 741 10th St., Santa Monica, CA 90402. (213) 394-8305.

December 6–10

Systems Analysis and Design Workshop. New York Sheraton, New York, NY. Contact: Institute for Advanced Technology, 6003 Executive Blvd., Rockville, MD 20852. (800) 638-6590.

December 7

Robotics Satellite Seminar. Locations nationwide. Contact: IEEE Service Center, Continuing Education, 445 Hoes Lane, Piscataway, NJ 08854. (201) 981-0060 ×329.

December 7–9

Dexpo/West '82. The 2nd National DEC Compatible Industry Exposition. Anaheim Convention Center, Anaheim, CA. Contact: Expoconsul International, 19 Yeger Rd., Cranbury, NJ 08512. (609) 799-1661.

December 8–9

Compusource '82. Red Lion Inn and Convention Center, 2050 Gateway Place, San Jose, CA. Offers OEMs a look at state-of-the-art graphics. Contact: Norm DeNardi Enterprises, 289 S. San Antonio Rd., Suite 204, Los Altos, CA 94022. (415) 941-8440.

December 12–14

Imaging Industries Conference. Andover Inn, Andover, MA. "Imaging Industries Over the Next Decade." Contact: Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

December 13–17

Microprocessor Course. Houston, TX. Contact: The Center for Professional Advancement, Dept. NR, PO Box H, East Brunswick, NJ 08816. (201) 249-1400.

December 14–16

Computer Graphics Conference. Andover Inn, Andover, MA. "Business Applications for Computer Graphics." Contact: Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

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The Bit Pad family. The world's best-selling low-cost digitizers. Designed and built to dependably meet all of your cursor control, menu selection, data entry and graphic needs. That's why Summagraphics digitizers and data tablets have become the standard of industry worldwide.

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We've responded to the needs of the digitizer marketplace since our start — anticipating and reacting quickly to evolving customer needs. It began a decade ago with an R&D program that has so far produced a comprehensive line of digitizers and data tablets. And you won't have long to wait until you know what we've done for you lately.

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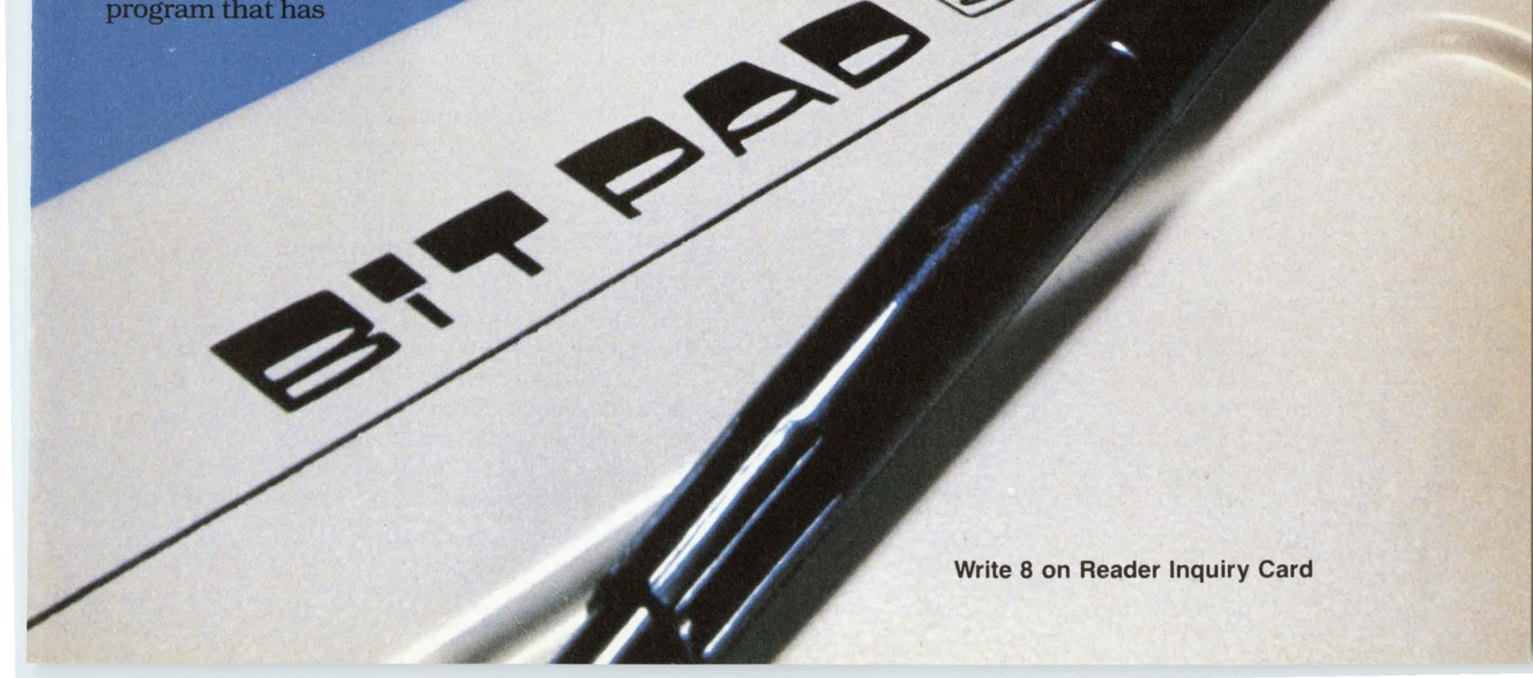

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News Update

Custom MOS Arrays Signs License With RACAL

Custom MOS Arrays has announced an exclusive license agreement with Racal Microelectronics Systems, England, to design, produce and sell Racal's family of gate array devices in the US. The initial gate array family is now available in a 5 micron silicon gate (SiGate) CMOS family with products ranging from 448 to 1,550 gate complexity. A 3 micron SiGate CMOS family will be available in June.

Archive Provides Drives To ADES

Archive Corp. has been awarded a $1 million contract to supply streaming tape drives to Adaptive Data & Energy Systems. ADES will purchase Archive's 20 Mbyte Intelligent Sidewinder 1/4" streaming cartridge tape drives and then incorporate them into ADES combined disk/streaming tape subsystems.

AMD/Motorola Agreement

AMD and Motorola have agreed to cooperate on the development of three new bipolar devices for addition to the Am2960 Family of Memory Support products, the Am2968 Dynamic Memory Controller (DMC) and the Am2969/Am2970 Memory Timing Controllers (MTC). Samples of all three devices are expected in the fourth quarter of 1983, with production commencing early in 1984.

CP/M-68K For Development System

Under an agreement with Digital Research, Motorola will sell the CP/M-68K operating system for the M68000-based EXORmacs development system. "The agreement with Digital Research is the foundation of Motorola's plan to become heavily involved with third party software for the 68000," said Bill Lowery, Motorola MOS Systems representative.

OEM Sales Of Interfaces

Southern Systems, FL, has started up a new OEM sales program for SSI-developed and manufactured computer-printer interfaces. The program will be an addition to the company's servicing of end-users with complete line printer systems. Southern Systems designs and manufactures line printer interfaces and controllers for DEC, Interdata, TI, HP, IBM and Burroughs computers.

CP/M-On-A-Chip

Intel Corp. has announced its 80150 CP/M software-in-silicon component. The 80150 combines Intel's iAPX 86 family compatible version of Digital Research's CP/M operating system with essential operating system hardware on a single silicon device. The CP/M-86-based 80150 is the second operating system processor offered by Intel. The first was the iRMX-86-based 80130, which was introduced in 1981.

National Memory Systems Launched

National Memory Systems Corp. has been formed in Livermore, CA, to provide memory storage subsystems for the DEC, TI, DG and PE minicomputer markets. Founder and President of the new company is Victor Weber, most recently with Spectra Logic Corp. of Santa Clara, where he was Western Regional Sales Manager. National Memory Systems offers subsystems which include Winchester disk drives, disk/tape single board controllers and streaming or start/stop tape drives.

Seagate Licenses Disk Drive From Sony

Seagate Technology has reached agreement with Sony Corp. whereby Seagate would supply the Sony 3½" micro-floppy disc drive under license from Sony. Finis Conner, Seagate's executive VP said that a standard is needed for the less than 5¼" floppy marketplace, and would expect a licensing agreement with Sony to help establish that standard.

Intel And TI Sign Development Agreements With IBM

Texas Instruments and IBM have entered a joint development agreement for VLSI ICs for local area networks. TI will design the chips according to IBM's functional specifications, and the development program will be managed by IBM's Communication Products Division (CPD) and TI's Semiconductor

Eaton printer power

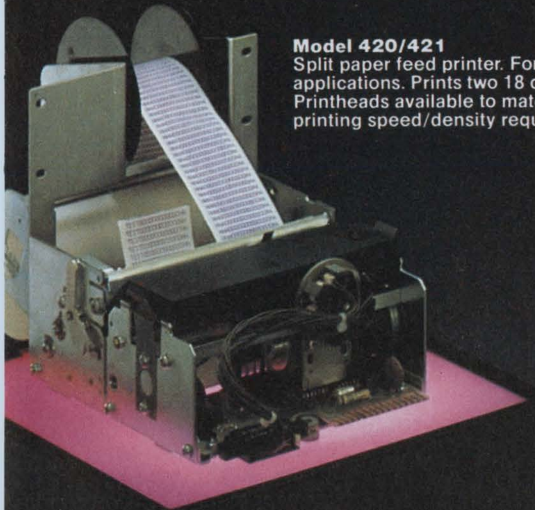
Works fast and economically wherever hard copy is needed—industrial, commercial, consumer.

Eaton's line of alphanumeric dot matrix impact printers give you printer power plus. You get performance, exclusive product features, attractive prices—all designed and backed by Eaton—one of the great names in American industry.

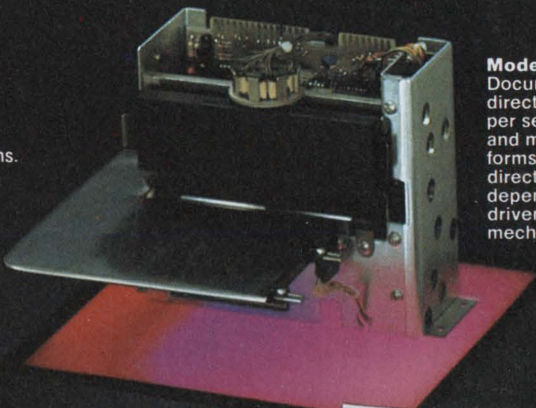
Eaton printers feature a 100 million character life printhead, easy interfacing and a simple, low maintenance design.

We'll assist in the design of the interface for your equipment and if you require a modified or custom printer unit, our engineers will be happy to work with you.

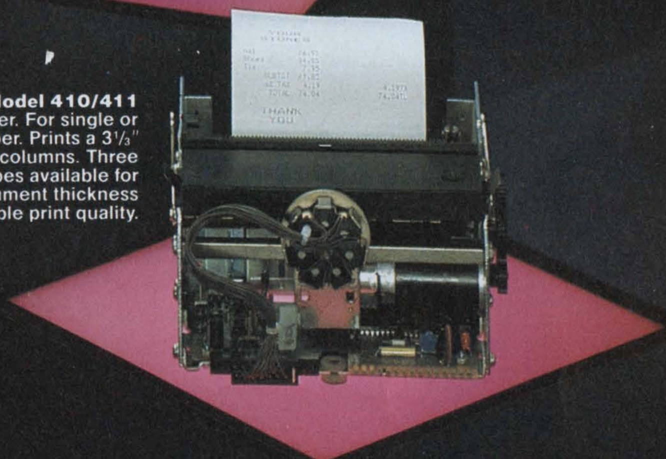
For additional technical information call or write: Eaton Corporation, Printer Products Operation, Riverton, Wyoming 82501. Phone: 307/856-4821.



Model 420/421
Split paper feed printer. For receipt/audit applications. Prints two 18 character columns. Printheads available to match paper and printing speed/density requirements.

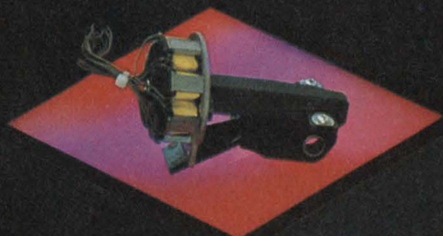


Model M-400
Document printer. Prints bi-directionally up to 3 lines per second. Handles single and multi-ply tickets and forms. Speed 3 lps bi-directionally. Has a quiet, dependable stepper motor driven paper advance mechanism.



Model 410/411
Single roll printer. For single or multi-ply paper. Prints a 3 1/3" line up to 40 columns. Three printhead types available for various document thickness and dependable print quality.

Model 7000+
Designed for commercial and industrial needs. Simple design, no special paper needed. Attractive case. 40 or 64 character capacity.



Printheads
Choose from 3 printhead models for integration with your own equipment. All with a minimum of 100 million characters and lifetime, low maintenance reliability. Short, medium, and long stroke models. Available in either 40 or 24 VDC.

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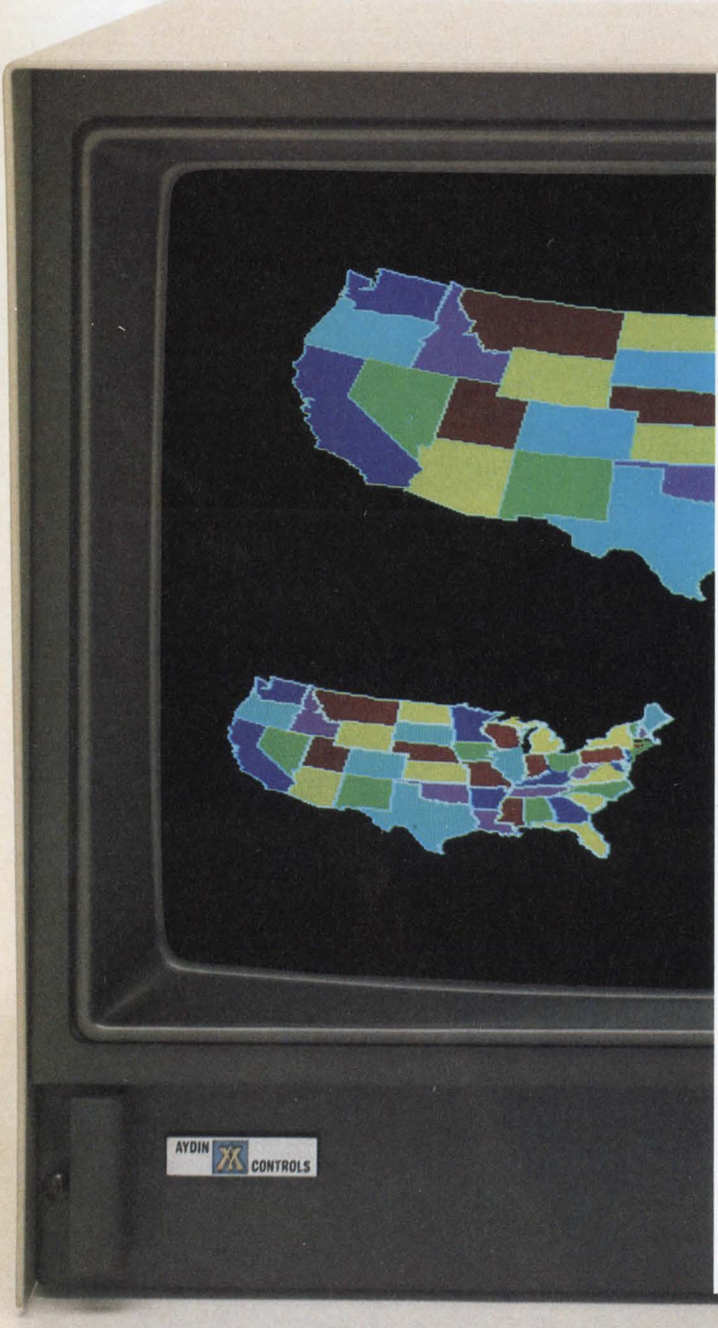
Made in USA

Aydin Patriot™ Color Monitors

Aydin Controls introduces its American-made, in-line gun, high resolution Patriot Series of Color Monitors.



Aydin Controls, a leader in high resolution color display terminals, now manufactures Patriot™, its own in-line gun series of color monitors. The Patriot series will supplement Aydin's well known family of delta and in-line gun monitors.

Patriot's 13-inch Model 8810 and 19-inch Model 8830 both offer the latest state-of-the-art features plus all of the advantages of American technology and manufacturing. Patriot features high video bandwidth, wide horizontal line rates, fixed convergence, excellent high voltage regulation, modular construction, analog or TTL inputs and rack mountability. The Patriot Series can be customized to fit special needs.

Patriot monitors provide outstanding performance at an attractive price coupled with an 18-month OEM warranty; off-the-shelf availability; quick delivery of spare parts; and fast, reliable service. For more information contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel: 215-542-7800 (TWX 510-661-0518).

AYDIN CONTROLS

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Group. Under the Intel/IBM agreement, Intel will provide 64K-bit dynamic RAM process and design information to IBM. IBM will have the option of manufacturing the Intel 2164A for use in its information-processing equipment.

CompuPro Licenses Digital Research Software

CompuPro and Digital Research have entered into a software licensing agreement which enables authorized CompuPro dealers to configure CompuPro hardware with the complete library of DRI programming languages and productivity tools. DRI products covered by the arrangement include CBASIC, CBASIC-86, Pascal MT and Pascal MT-86, PL-1, Cobol-80, Cobol-86, and CB-80. Operating systems supported are CP/M, CP/M 86, and MP/M 8-16, CompuPro's proprietary version of MP/M 86 Version 2.

Tandon Building New Plant

Tandon Corp. has broken ground for a 61,000 ft^2 plant for its Magnum Division that will more than triple its capacity to produce 8″ half-height floppy disk drives. Scheduled to be completed and in operation by next April, it is expected to employ over 500 persons when operating at capacity.

C. Itoh Apple Printer Contract

C. Itoh Electronics and Apple Computer have signed a long-term contract that will supply Apple with C. Itoh dot matrix impact printers. The dot matrix printer will carry the Apple logo and be totally supported by Apple's distribution, sales and service.

Cutting the height of standard 8" floppys in half is a step in the right direction. But our market research said in this age of "smaller is better," it doesn't go quite far enough.

That's why, at MPI, we didn't stop at halfway. We cut the height to 2.0". And thereby created the new industry standard.

It's our Slimline™ series. The smallest 8" disk drives ever made.

They're designed so you can easily fit one under a CRT or keyboard. Or, where one drive used to go, you can stack two.

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E^2PROM-based μC To Be Launched At Next ISSCC

Seeq Technology will announce a μC with on board E^2PROM at next February's International Solid State Circuits Conference, according to Seeq Technology President Gordon Campbell. Mr. Campbell would not say which μC the new part would be based around, but having signed a technology agreement with Rockwell International (*Digital Design*, September 1982) it seems likely the part may be a 6500-type machine. Intel Corp. is also trying very hard to have such a μC ready by next year, according to Campbell.

Putting E^2 memory on board a microcontroller will give the board level designer much greater flexibility, especially in control applications.. Instead of using UV EPROM to store program memory, the designer will now be able to reconfigure the μC's program memory without having to remove the part from the board.

Campbell sees the E^2PROM to be the dominant memory technology by the end of this decade, and his company reflects this well. Earlier this year Seeq introduced a 5V only E^2PROM (the 5213), a 2K × 8 part on which data is electrically written by either a TTL pulse or a voltage between 15 and 22V on the Write Enable pin (*Digital Design*, March 1982).

At Wescon this year, Seeq announced a competition based around the 5213. Grand prize: a Porsche 944. To enter the contest an original application for the part must be designed and submitted to Seeq. Also, Seeq is allowing contestants to purchase a limit of two 5213s for $9.95 each from October 11 to January 10, 1983. To receive this special price, contestants must submit a signed, written request on company letterhead to Mr. Bill Reardon at Schweber Electronics Inc., Jerico Turnpike, Westbury, New York 11590. —*Wilson*

The North American Presentation Level Protocol—Positioned to Replace ASCII?

Events of the past summer have brought together the different technologies of videotex, computer graphics, and data communications, and in the form of a proposed US standard to the CCITT (The International Consultative Committee on Telephony and Telegraphy) for the communication of graphics and text. This draft standard is being tabled at the November meeting of the CCITT in Geneva in the hope of creating an international standard for videotex. However, European countries who make up the CEPT (Council of European Postal and Telecommunications Ministries) will be proposing their own standard, and there is likely to be contention over which standard is more acceptable internationally.

Despite the low profile of the issue, it is of tremendous importance for the electronics industries of all of the industrialized nations, due to the potential mass market of videotex and because of the enormous investment already made by European companies in developing videotex systems and markets. In the United Kingdom alone, for example, there are already over one-half million users of teletext (the broadcast form of videotex). The US State Department, and members of its Technical Panel of Videotex Experts have, however, modified earlier proposals to insure that adoption of the NA-PLPS will not adversely affect the use of systems such as those in Britain. In fact the standard has been designed with future growth and refinement of videotex systems in mind—leaving unspecified such features as the algorithms used to render images.

While the CCITT standard would form part of the body of international telecommunications policy (that is, become one of the documents of the CCITT's parent organization, the International Communications Union), there needs to be a technical standard promulgated and adopted by the equivalent international technical organization, i.e. the ISO (International Standards Organization). With both the US and Canadian representatives (ANSI and the CSA respectively) to the ISO having agreed upon the standard already, there seems to be a consensus in North America that the NA-PLPS will be accepted.

The importance of the standard was attested to in July of this year at the SIGGRAPH conference when 18 manufacturers including DEC, Tektronix, Intel, Honeywell, and others announced their support for the NA-PLPS. This was a powerful recognition that computer graphics and videotex have a great deal in common and recognition of the importance of the market by the manufacturers. The NA-PLPS for instance, takes a traditional computer graphics approach to graphics creation in which the entire screen's pixels may be addressed. Similarly, a "unit screen coordinate system" based on the world coordinate systems of the SIGGRAPH CORE standard is adopted which allows the displays to be created as a function of the display's size (allowing terminal independence). The advantage of this approach may also be seen as allowing information or pictures to be stored without having to format the data for a specific display standard.

Under the NA-PLPS, graphics are encoded as instructions for the creation of geometric primitives: points, lines, arcs, rectangles, polygons, and incrementals. These primitives are modified by command controls to allow the shift of color, texture, blinking, or pixel size. The standard will even allow the use of other display and transmission techniques including: alpha-mosaics, alpha-photographics, and dynamically redefinable character sets.

Like ASCII, the NA-PLPS is a presentation level communications protocol—that is, it belongs to the sixth level of ISO's Open System Interconnect Model. However, while ASCII is the telecommunications protocol for the transmission of alphanumerics, NA-PLPS is designed to accept the encoding of both graphics and text. The implication of the acceptance and use of such a standard is that the communications of pictures is becoming as important as that of text and numbers. If the use of graphics becomes as widespread as current marketing and research indicate, the NA-PLPS could, in the eyes of many of its developers, eventually replace ASCII as the terminal or display device standard. Further evidence supporting such a point of view may be found in the widespread use of graphics in new microcomputer systems—where over 45 manufacturers currently provide for graphics displays. *—Borrell*

STD Bus Fever Increases

Several important additions to cement the position of the STD bus firmly in the area of industrial control have been announced over the past few months.

The first, from GE's Intersil Division in Sunnyvale, CA came in the form of a character graphics video terminal with a 10-slot card cage that allows the user to add up to six STD bus cards for his own application (**Figure 1**). The ISB 80/85 can be used as a console for any distributed STD bus control system. An integrated ISB-ICP operating system based on CP/M 2.2 offers the standard utilities of editor, assembler, debugger, etc.

In addition, Intersil provides utilities to format floppy disks and the Winchester hard disk, and the ability to invoke graphics character output to the video display. The user can further enhance his software capability by choosing other CP/M compatible software from Intersil's product line. This includes high level language support, such as Pascal or Fortran.

Second, a two card combo from Analog Devices; a 13-bit A/D-CPU card (RT1-1270) and companion 4-channel signal conditioning/multiplexer cards (RT1-1271), eliminate the need for external signal conditioning components and the task of writing linearization, data acquisition and conversion routines (**Figure 2**). The signal conditioning cards provide excitation, filtering, cold junction compensation and optional ± 1000V isolation. The A/D-CPU card scans the input channels, amplifies, linearizes and converts the data to engineering units and stores it in on-board memory. The RTI-1270 provides solution to system integrators who must interface thermocouples, RTDs, strain gages, mV, V and mA signals to an STD bus in the presence of electrical noise, ground loops and common mode voltages.

—Wilson

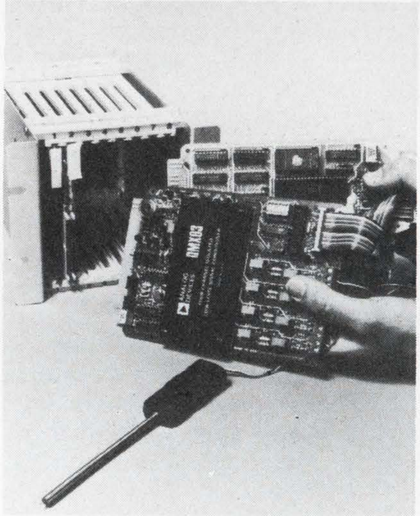

Figure 2: Analog Devices' RTI-1270/1271 STD Bus compatible boards. On board μP control reduces software overhead.

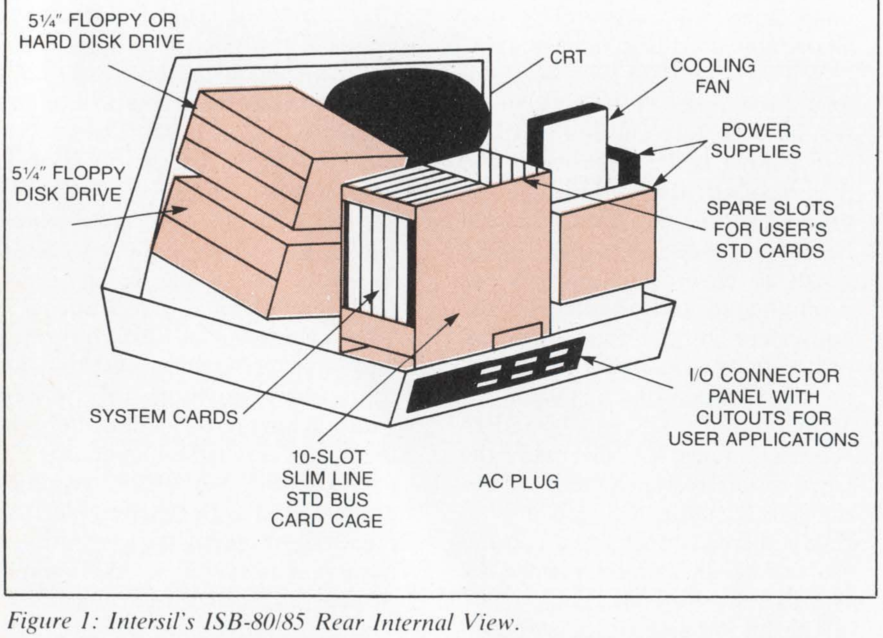

Figure 1: Intersil's ISB-80/85 Rear Internal View.

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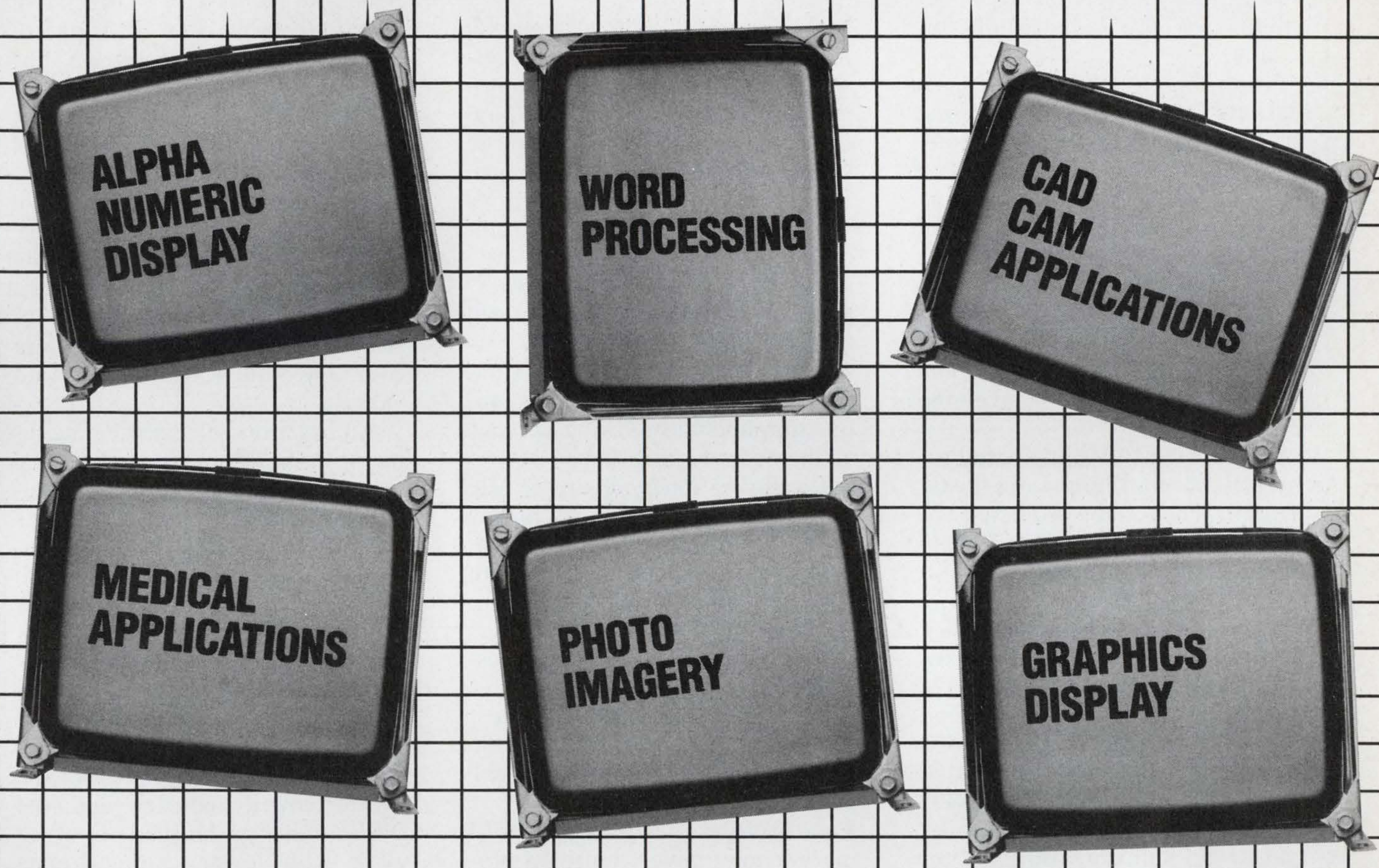

Yesterday's ideas might not be good enough for today or tomorrow, and selecting the proper data display has never been more significant. Recent studies in the computer marketplace indicate the CRT display has become the single-most important element in today's computer systems. An easy-to-read, jitter-free display is of course a dynamic part of this critical man/machine interface.

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Hybrid Circuit Market Forecast To Grow At 17–18% Annual Rate

The overall market for hybrid circuits in the US and Canada will grow approximately 17–18% per annum for the balance of this decade.

According to "Hybrid Circuits Market," a new study by Frost and Sullivan, total sales will climb from $2.91 billion in 1982 to $5.39 billion by 1990.

Sales in the merchant segment are seen advancing from $1.15 billion in 1982 to $1.98 billion in 1986 and $3.66 billion by 1990. The captive market is forecast to expand from $1.76 billion to $3.41 billion and $6.55 billion over the same period.

Similar growth is anticipated for thick film materials markets. Overall sales are projected to climb from $209 million in 1982 to $410 million in 1986 and $791 million by 1990.

The captive market for thick film materials is expected to grow from $49 million in 1982 to $128 million in 1986 and $298 million by 1990. The merchant market is forecast to increase from $160 million to $282 million and $493 million over the same time frame.

Frost & Sullivan's outlook for hybrids in various markets is as follows:

- *Military/Aerospace.* This area has not been affected by the recession. In fact, the large defense budget should put demand for hybrids on a higher growth track, increasing about 20% per year, the study says. Cutbacks in the space budget are seen having minimal impact.
- *Commercial.* While this market has been affected by the recession, the areas hurt most—industrial controls, laboratory equipment, electronic toys—are those where hybrids have the least penetration. Areas where hybrids have gained more ground, medical, computerized games, etc., still have fairly high growth rates.
- *Custom/Specialty.* This area will be affected by the recession, particularly on the custom side. Standard circuits are still holding up, but suppliers are growing nervous as the order rate declines.
- *Computer/Peripherals.* While the larger computer segments have been stung by the recession, peripherals and μCs—areas with the least amount of captivity—continue to grow at a fast pace.
- *Telecommunications.* The recession has had little impact on this area. The major concern of most manufacturers is what will be the ultimate effect of the AT&T restructuring.
- *Automotive.* This depressed market may never return to previous levels, the study suggests. This is especially true of the merchant market, as the major manufacturers are keeping as much work as possible in-house to maximize profits and to respond to union pressure.

On the technical front, the report notes that large substrates and polymeric thick films did not penetrate the market to the extent that had once been anticipated. They will only represent a few percent of the market unless some totally unforeseen technology event occurs at the fundamental material level.

Non-noble materials have gained a foothold in the market, but their impact is seen remaining modest due to the failure to obtain a non-noble, compatible resistive system that will operate over the full range of desired values.

Automation of hybrid manufacturing has been slowed by the recession and a lack of standards—particularly for carriers and mounting techniques. Automation appears to be moving into the test side first, and assembly second.

The study adds that earlier concerns that energy and environmental factors could erode hybrids' cost position against PWBs have proven unfounded. Both the hybrid circuit industry and the PWB industry learned how to work with lower energy inputs and lower level environmental pollution. As a result, there was no major market shift and none is foreseen in the immediate future.

For further information contact, Customer Service, Frost and Sullivan, 106 Fulton Street, New York, NY 10038 Tel: (212) 233-1080.

Massive Growth Of Data Converter Consumption

The market for A/D and D/A converters is poised for massive expansion. The optimistic outlook can be directly linked to the shift toward digital techniques in virtually all segments of electronic instrumentation, as well as to the continuing displacement of mechanical measurement and control devices with electronic counterparts.

The result is an extraordinarily favorable market expansion for A/D and D/A converters that are required to interface computers with the real world. 1982 shipments of data conversion components, including A/D and D/A converters, sample/hold amplifiers, and analog multiplexers will reach the $377.0 million level. The forecasted 33% average annual increase in consumption of these components will result in a $1.2 billion market in 1986. Furthermore, these projected shipments are dramatically higher than the $40.0 million worth of circuit conversion produced in 1975.

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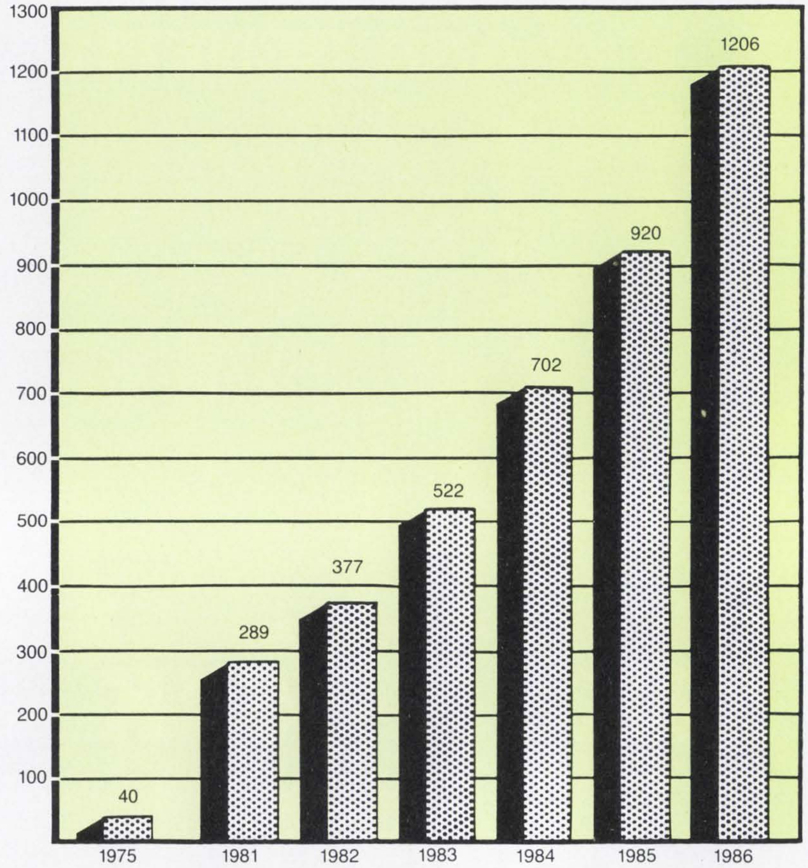
These views are from a market study on "The A/D and D/A Converter Industry: A Strategic Analysis" recently published by Venture Development Corp., Wellesley, MA.

Although military markets for data converters will be somewhat less dynamic, increased converter usage will occur in radar, navigation, and communications applications.

In addition, major new high growth applications for data converters appear likely. The recording and broadcast industries are becoming increasingly aware of the benefits of digital signal processing, particularly in digital audio and digital video. Similarly, the use of μPs and data converters in automobiles is continuing to accelerate. But, ultimately, the consumer market could very well become the largest application for A/D and D/A converters, including games, appliances, energy and environmental control.

Further information regarding this report can be obtained from: Venture Development Corporation, One Washington Street, Wellesley, MA 02181. Tel: (617) 237-5080.

SAMPLE/HOLD AMPLIFIERS, AND ANALOG MULTIPLEXERS
(Millions of Dollars)



Buyer Perceptions Key To Computer Marketing

"Techno-preneurs"—hardware and software engineers who start their own firms—need "hard-nosed marketing skills if they are to survive in the 80s, let alone succeed," according to Gene R. Talsky, president of Professional Marketing Management Inc. (PROMARK, Seattle, WA).

"There are too many products that look alike to buyers, who will always know more about running their businesses than they will about computers. We have to deal with the perceptions of buyers, not product features," Talsky told a recent meeting of 200 systems house managers at the Third Annual Product, Marketing and Management seminar hosted by The Office Manager Inc.

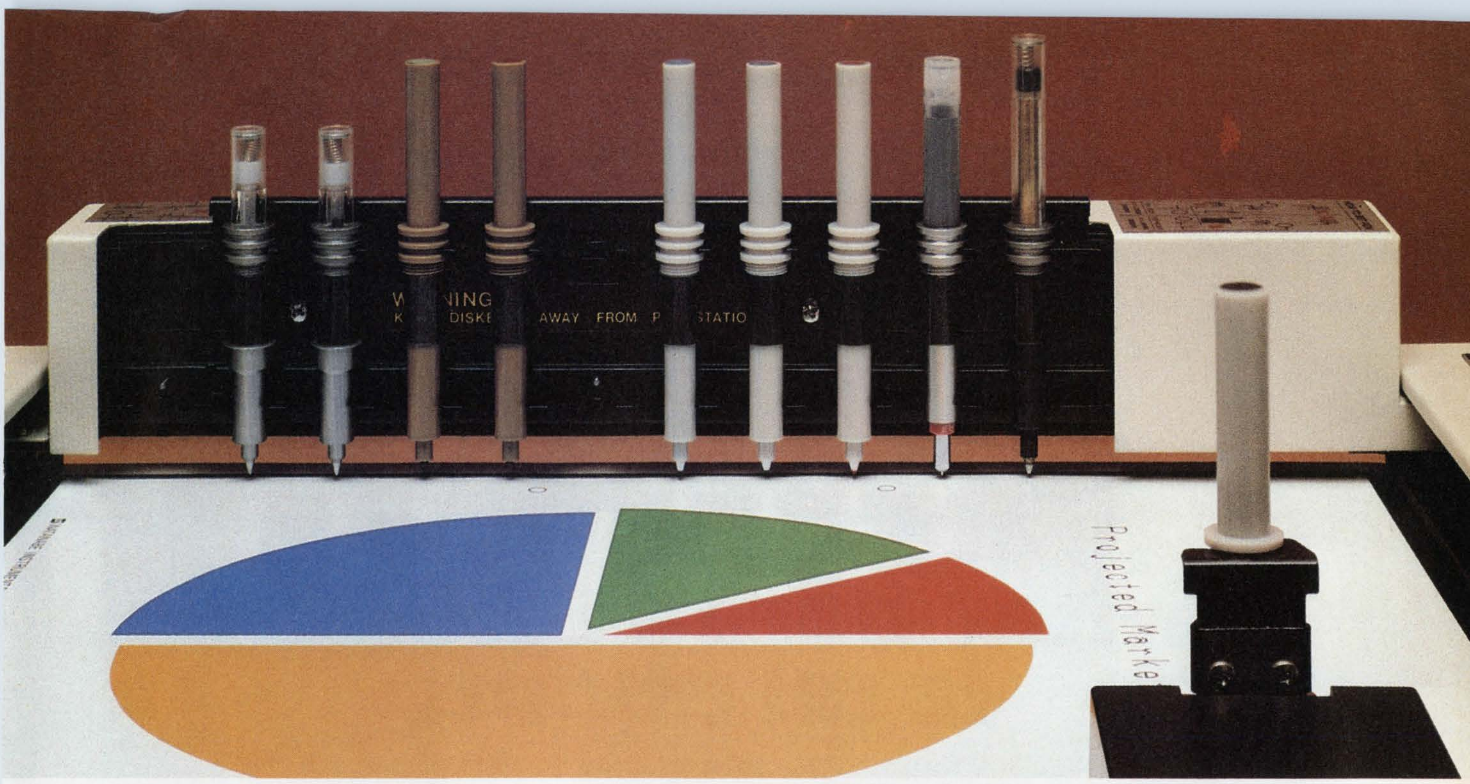
Techno-preneurial organizations often lack the ability to address user perceptions, Talsky said. They need "scientific marketing based on sound product strategy, innovative sales programs, strong marketing and sales organizations and effective promotion," he said.

"The computer industry was driven by engineers in the 60s, when buyers were waiting for anything the manufacturers could produce.

"During the 70s, the buyers were still lined up, but wanted more bang for the buck. The 80s are now totally marketing driven," he said.

To succeed in the 80s, techno-preneurs will need good marketing and business plans based on empathy, perception, discipline and science, according to Talsky. The inability of new techno-preneurial firms to market their undifferentiated 8-, 16- and 32-bit computers will not only result in their failure, buy may cause problems for the whole computer industry, Talsky predicted, "as end users become unable to obtain support and maintenance."

Problems with undifferentiated, poorly marketed software are only "one wave behind" those in hardware, he concluded. "How many Visi-clones does the world need?"



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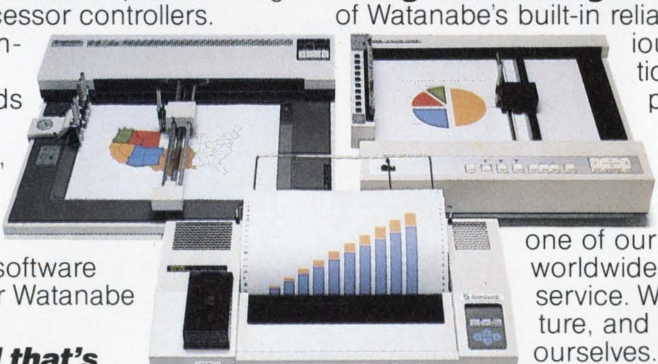

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Use water or oil-based pens, or ink pens. Choose from sheet-feed or roll-feed models, or produce drawings on acetate for overhead projection. In addition to programmable graphics and function commands, the complete ASCII character set is standard. Each plotter can interface to any computer with an RS-232-C serial interface, IEEE-488 interface, or parallel port.

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A μP-Based PROM-Burner For The Intel 2716 EPROM.

By Michael Coppola
Applied Engineering Concepts

How many times have you needed to burn an EPROM in a hurry, but couldn't because a) your EPROM burner was down, b) you couldn't afford a burner, c) you couldn't wait for delivery on one, or d) you were frightened at the cost of getting it burned by some outside outfit. Whether or not you've experienced these problems, this simple project is for you. It was designed for the 2716 EPROM since it is the most common EPROM used at Applied Engineering Concepts (AEC). The Intel version of the 2716 does not require that non-TTL levels be applied to the address or data pins to program the 2716. For this reason it is very convenient to use the TTL levels readily available from standard buffered output ports. The only non-TTL level required is +24 V on the V_{pp} pin; this can be obtained from an external supply (more on that later). The cost of this burner is under $20, assuming you have available a micro with at least four 8-bit I/O ports.

The PROM-Burner uses a 24-pin DIP socket (a ZIF socket is strongly recommended), a 24 V supply, and four 8-bit ports, exclusive of wiring of course. **Figure 1** shows the pin out for the Intel 2716. There are 11 address lines (A0-A10) used to address from 0000H to 07FFH (2048 bytes), eight data lines (D0-D7) used to read and write information, V_{cc} (5V), and V_{ss}(0V). V_{pp} is the read/program supply pin; 5V here when reading the 2716 and 24V on this pin to program the EPROM.

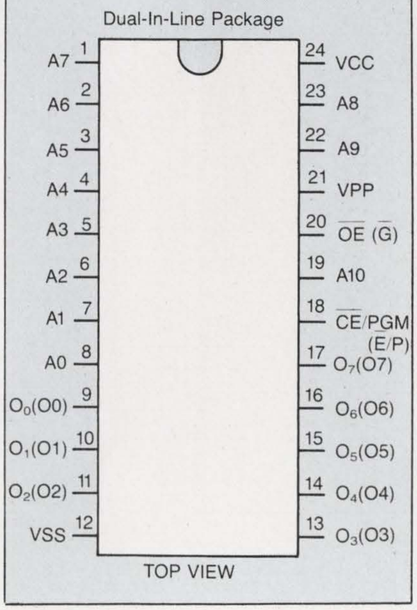
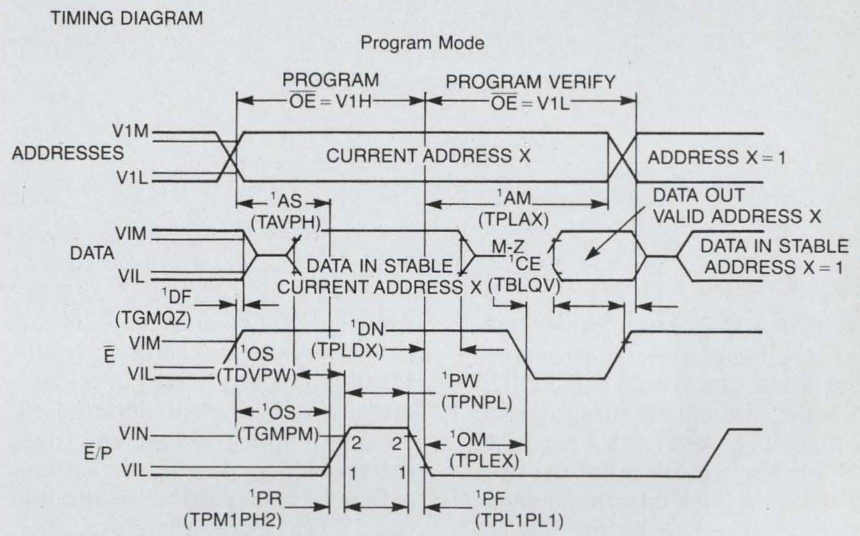


Figure 1: Pin out for the Intel 2716 EPROM.



AC Characteristics and Operating Conditions (Notes 1, 2, and 6)
(T_A = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
ALTERNATE	STANDARD					
tAS	TAVPH	Address Setup Time	2			μs
tOS	TGHPH	OE Setup Time	2			μs
tDS	TDVPH	Data Setup Time	2			μs
tAH	TPLAX	Address Hold Time	2			μs
tOH	TPLGX	OE Hold Time	2			μs
tDH	TPLDX	Data Hold Time	2			μs
tDF	TGHOZ	Chip Disable to Output Float Delay (Note 4)	0		100	ns
tCE	TGLOV	Chip Enable to Output Delay (Note 4)			120	ns
tPW	TPHPL	Program Pulse Width	45	50	55	ms
tPR	TPH1PH2	Program Pulse Rise Time	5			ns
tPF	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.
Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.
Note 3: 0.45V ≤ VIN ≤ 5.25V
Note 4: CE.PGM = VIL.VPP = VCC = 0.6V.
Note 5: VPP = 26V.
Note 6: Transition times ≤ 20 ns unless noted otherwise.

Figure 2: Timing diagram with symbol table.

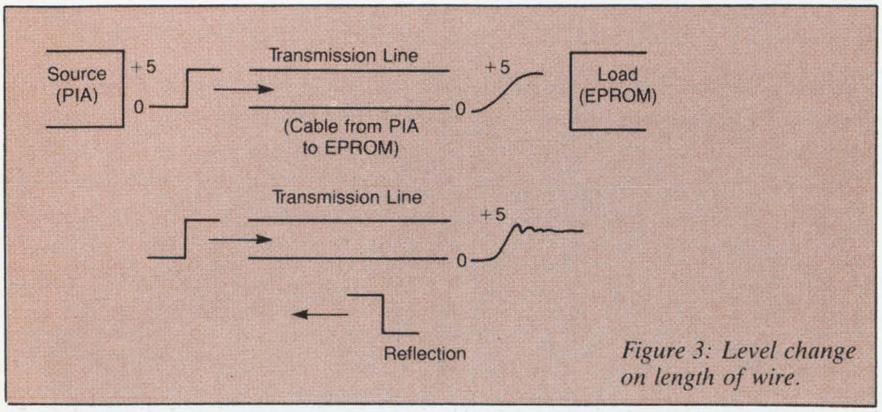


Figure 3: Level change on length of wire.

$\overline{OE}$ ($\overline{G}$) is the output enable pin, and is self explanatory: output enable when low. The $\overline{CE}$/PGM ($\overline{E}$/P) is the chip enable/program pin. A high logic level (5V) here and 24V on V_{pp} will program the data on the data lines into the memory locations specified by the ten address lines. Remember, the output must be disabled to program the EPROM ($\overline{G}$)-5 V.

Figure 2 is a timing diagram with symbol table. These diagrams tend to be difficult to read if you've never seen one before. As can be seen from the table, all setup and hold times are less than 2μS, the exception here being the programming time (50mS). Since any micro takes longer than 2μS to execute a short sequence of I/O bound instructions, delays for setup and hold times are inherent to the micro. The major limiting factor here is the programming delay time, which must be 50mS (±5mS) for each individual address. Delaying is also necessary to assure proper level settling.

In **Figure 3,** observe what occurs when a level is changed on any length of wire. As an output port (usually a peripheral interface adapter or PIA) changes its level from low to high, the rise time of the level at the load is affected by the cable capacitance. This causes the high level at the load to be delayed. The 2μS delays mentioned above assure in part that the level at the load has actually changed. A further reason for the delay is the settling time. As a fast rise time pulse reaches an unterminated load, a reflection occurs, which causes ringing. This ringing may appear to the load as an incorrect level. Fortunately, the delays in the micro are of sufficient duration to eliminate both rise time and ringing problems. A note of caution: a PIA is only capable of driving one TTL load; therefore, the wires connecting the PIA to the EPROM should be relatively short (within a few feet) if the PIA is not buffered.

An outline of the programming procedure is listed below:

- Apply address, ($\overline{G}$) = HIGH (output disabled).
- Apply data, $\overline{E}$/P = HIGH (program enable).
- Delay 50mS for programming.
- Remove program enable ($\overline{E}$/P = LOW); enable output ($\overline{G}$) = LOW; read data and compare to check accuracy.
- If data is incorrect, then try again—up to five times if necessary (arbitrary). Abort if unable to program and save unprogrammable data byte and the bad data byte from the EPROM.
- If data is correct, then go on to next address.

The wiring from the micro to the socket is shown in **Figure 4.**

The program is written in 8080A assembler and makes use of a TTY output routine (COUT) at address 03FAH. It robs data to be sent to the 2716 starting at memory location GTROM. A to-

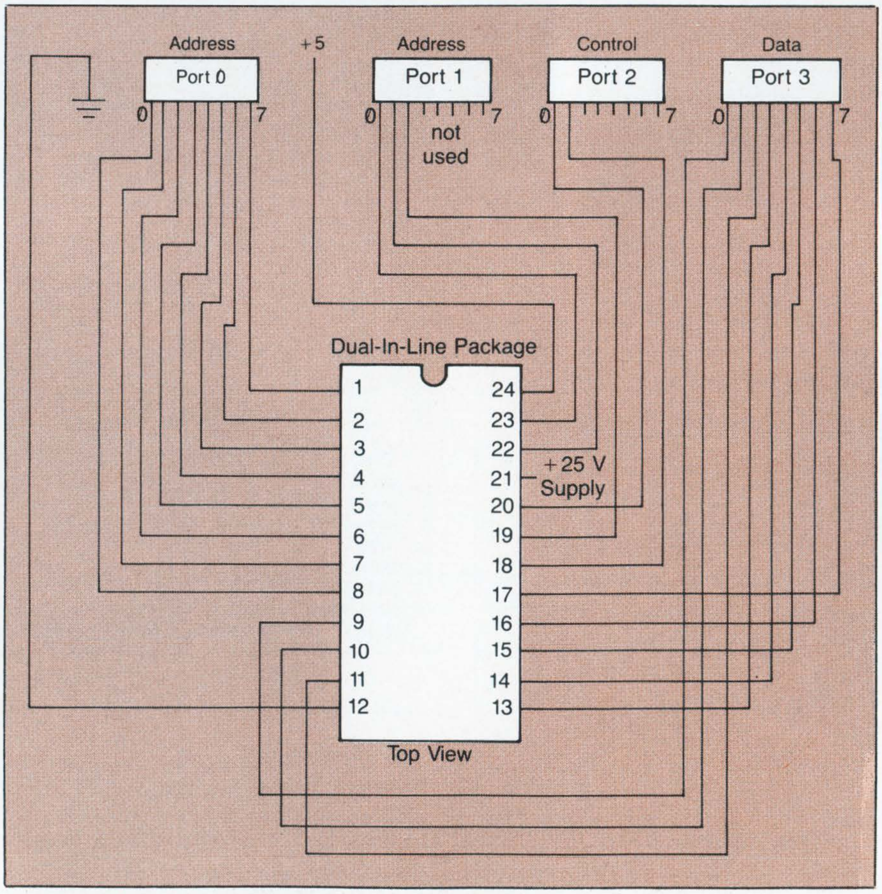


Figure 4: Wiring from the micro to the DIP socket.

tal of four ports are used—two ports are used for the ten-bit address, one port for the data, and the last port for chip control. To convert to the 2732, simply add one more address line and modify the software a bit (no pun intended).

The program is listed in **Table 1**. Execution takes about one minute. For a nominal charge, the program is available on a mini floppy disk. For more information, write to:

Michael Coppola, Applied Engineering Concepts, P.O. Box 801, Binghamton, New York 13902

Keyboard Conversions Made Easy

What do you do when you have a standard keyboard and want function keys or special encoding? What if your keyboard is ASCII and you need EBCDIC? You could use a software look-up table, but a much simpler solution is to build this simple little circuit.

A normal keyboard (ASCII or EBCBIC) will generate a hex code for each key press. The range of these codes is from 0 to 255 (FF_H) for EBCDIC and 0 to 127 ($7F_H$) for ASCII.

When you use this circuit you can redefine the codes generated by the keyboard. The output of the keyboard is used as the address input lines to the EPROM. What is burned at that location is then substituted.

When an "A" key is pressed on the keyboard a 41_H is generated by the keyboard. This is then used by the EPROM as location 41_H. The contents of locations 41_H is then sent to the computer.

An example of this is in **Table 1.** When an "A" and a shift is pressed a 41_H is generated by the keyboard and the EPROM sends a 41_H to the computer. When an "A" is pressed with no shift the alternate character set is used ($41_H + 80_H = C1_H$) generating a $C1_H$ from the keyboard. The EPROM then emits a 61_H which is an "a" in ASCII.

If your keyboard generates a $7F_H$ as a backspace but the computer is expecting a 08_H, you just put a 08_H at location $7F_H$ and the conversion is done for you.

The circuit in **Figure 1** is set up for an Apple keyboard which produces 0 to $5F_H$ (upper case only).

The keyboard plugs into the dip socket. The seven data lines go to Address 0-6 of the EPROM. Address 7 is attached to shift key on the keyboard (it can go to any key). The press of this key will invoke the alternate code set.

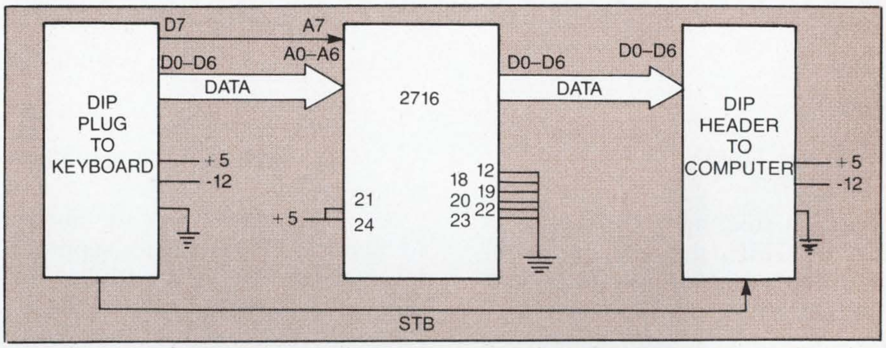


Figure 1: This EPROM-based circuit allows special encoding and function keys, as well as ASCII/EBCDIC conversion, on a standard keyboard.

8000	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
8010	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
8020	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	
8030	30	31	32	33	34	35	36	37	38	39	3À	3B	3C	3D	3E	3F	WITH SHIFT
8040	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
8050	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	
8060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
8070	00	.00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
8080	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
8090	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
80A0	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	
80B0	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	WITHOUT SHIFT
80C0	40	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	
80D0	70	71	72	73	74	75	76	77	78	79	7A	5B	5C	5D	5E	5F	
80E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
80F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	

Table 1: This table lists the code required to make an Apple upper case keyboard into an upper/lower case keyboard with use of the shift key.

Note that the power lines and STROBE line bypass the EPROM. This allows for a repeating keyboard to remain functional.

Table 1 has the code required to make an Apple upper case keyboard into an upper/lower case keyboard with use of the shift key.

What provides this circuit with versatility is that it is based on an EPROM, so the encoding can be redefined easily. Also a switch can be used to provide an alternate character set.

By using the shift key as the extra character set switch, you could make an uppercase only keyboard have upper/lowercase, and only affect the alphabetic keys. This eliminates problems with hardware gates and software routines that work for converting an "A" to "a" but also converts an underscore (5F) to a delete (7F). A similar situation exists when a computer needs uppercase characters for system commands but is equipped with an upper/lower keyboard. The switch would involve the alternate character set which would convert all the codes for 61_H to $7A_H$ and not affect $7B_H$ through $7F_H$.

Mark Hanslip, Development Engineer, NCR Corp, Dayton, OH 45479.

External CML Reference Power Supply Offers Versatility, Economy

by George Field

In current steering circuits, such as ECL or CML, the reference voltage can be designed into the chip or furnished by an outside power supply. If a semiconductor supplier is designing the circuit, they will build the reference supply inside the chip. It saves a package pin, is easier to test and has value added.

A system supplier, however, in designing the chip usually will furnish the reference voltage external to the chip—from the system itself. This is especially true in case of a large system design, such as the Honeywell DPS 88 very large scale system introduced in October.

The main advantage of an external reference power supply is that it allows the designer to determine operating margins in his system. By varying the reference voltage throughout the total system, or large portions of the system—such as the processor, for instance—the noise and timing operational margins can be determined. Periodically accomplishing this on the same system will detect any early drift components.

When utilizing a current mode logic (CML) type of current steering, it is possible to use a lower Vee supply and a smaller logic swing. This results in a low voltage requirement for Vref.—thus making for a difficult design problem. Described here is a 250mv reference regulator design utilizing a 3.3V Vee supply. This design also allows convenient margining of the Vref. voltage.

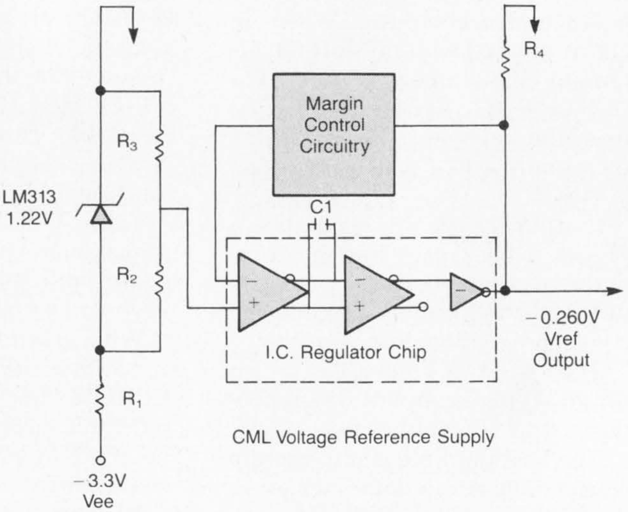
As a diagnostic tool, the ability to "schmoo" the reference supply is invaluable. This is especially important in large computer systems. Marginal performance conditions and failures due to low noise immunity are identified by running T & D (timing and diagnostic) programs while margining the reference source(s).

The external reference is economical, i.e. system overhead alloted to reference supplies is minimal. In one application, at Honeywell for example, a single reference regulator is packaged in a DIP and mounted on a 2″ × 3″ PWB. It can provide a reference voltage for up to 10,000 CML logic gate.

The main advantage of an external reference power supply is that it allows designers to determine noise and timing operational margins within the system.

George Field is Technical Communications Director for Honeywell Inc., Waltham, MA.

Figure 1: This diagram illustrates the complete CML voltage reference supply: -0.260V at 0.3A. The bandgap voltage source establishes a stable -1.22V signal. Divider R2 and R3 provides the 0.260V signal for the regulator chip. Register R1 and biases the 1.22V source. Since the regulator chip can only sink current, R4 provides the pull-up path. Margin control circuitry consists of switchable voltage dividers for margining "schmooing" the 0.260V reference output voltage. C1 sets the frequency compensation.



CML Voltage Reference Supply

Although CML does not require a tracking reference voltage, which is a function of Vee and chip temperature, an external reference source can be made to track these or any other parameters as required.

Reference regulator design is complicated by the low voltages involved. This problem is expected to become worse, in the future, as power supply and logic swing voltages are reduced in order to decrease the speed-power product of future logic gates. For this reason a custom chip is required. There are no off-the-shelf regulator chips that operate at CML voltage levels.

At Honeywell we manufacture a monolithic reference regulator chip for use with our CML logic family. The monolithic regulator consists of 2 cascaded operational amplifiers and a buffer. The regulator operates from a nominal Vee supply voltage of −3.3V. It delivers a reference output voltage of −0.210 to −0.310V at 0.3A. This chip, plus a LM313 1.22V bandgap voltage source and a few resistors comprise the entire reference supply for a CML logic board containing up to 10,000 gates.

Although a reference chip can provide high control loop gain and regulate within 10's of microvolts, it can do so only at the sense/feedback point. A 5–6mV drop in the connector or PWB run is a 2% error in a 260mV reference voltage! Layout of the reference voltage bus system must be short paths of large cross-sectional area with a minimum of connectors.

The reference supply is mounted directly on bus bars with copper brackets to minimize series impedance between the reference supply and CML logic gate reference voltage input pins.

Since the regulator is manufactured using high speed CML technology the bandpass is high; 15MHz. While a high bandpass is desirable for good step response, the parasitic reactance in the reference voltage bus system can ring and cause under/overshoot in the reference voltage. Considering these tradeoffs, the bandpass was set at 200KHz. □

Power Supply Selection And Design

by Ed Pevovar,
Contributing Technical Editor

Varying voltages and currents of power sources, transients and noise, load isolation needs, and varied supply voltages, have all necessitated the need for well-regulated power supplies.

There are, at present, many "Design Houses," where purchasing all types of supplies is rather simple. You check your needs against those specs listed and obtain a price quote. Usually, the supplies listed will not be exactly what you want, and in that case, it may be necessary to make some alterations to the equipment you purchase. By virtue of the design and the technology behind it, alterations could range from a simple task to an "impossible dream." Cautiously consider all your needs, and the time allotment you are working with. You may want to do a feasibility study to properly compare quantity pricing of purchasing units versus manufacturing that quantity. My attitude to designing and manufacturing my own power supply is not that it is cheaper to buy milk instead of owning a cow. If the volume production of the end product that incorporates the power supply is low, the cost of buying power supplies may be a prohibitive factor; it will be better to design your own. These can be built in any quantity the designer wishes, and costs are based upon what specifications the designer wants to incorporate, no more, no less.

Design Criteria

The design of most power supplies presents a multitude of challenges. Most of the problems stem from the usual series of design events. As the total system is planned-out, subsystem equipment space becomes allocated, and parameters are set for subsystem implementation. Normally, the design of power supplies follows the design of the equipment it serves, causing designers to follow closely established performance criteria that complicate the task severely. Criteria which all designers must consider but are not limited to, are to some extent bounded by: performance requirements, load characteristics, operating parameters (such as ripple, and power related to time and volume/weight), the effects caused by any peripheral devices, thermomechanical and electromagnetic considerations, and packaging.

Two types of power supplies prevail: DC/DC converters, which provide a DC output voltage, and DC/AC inverters, which supply an AC output voltage; both are switchers. Any DC/DC converter has a DC/AC inverter. The output is rectified and regulated to provide any required DC output: DC/AC inverters do not have DC/DC converters. The converter and the inverter yield many design constraints based upon component and environmental criteria: power and switching transistors, amplification, regulation, filtration, oscillation, transient responses, and the elimination of noise generated in the circuit and external to it.

The main form of line power is AC, and there are three types of AC/DC power supplies that provide desired DC output voltages: series regulated; ferroresonant; and switching. The function of AC-to-DC supplies is to rectify AC, and provide pulsating DC. The pulsating DC is filtered, to produce a constant voltage. A feedback circuit is designed to maintain the output voltage levels at constant values, regardless of any change in output load. One of the most common supplies used in equipment is the series-regulated-linear supply, and there exist three common functional blocks regarding these supplies: 50Hz to 400Hz transformers; rectifiers; series pass transistors, and regulators in feedback circuits. Isolation is by virtue of transformers the size of which is inversely proportional to frequency. Rectifiers (bridge type) deliver unregulated DC to a pass transistor, in series with the load. The current depends on voltage changes (and circuit loading). This pass transistor acts as a variable resistor and dissipates power continuously. Under the worst high-input line voltage and low output DC voltage conditions, power dissipation becomes excessive, and there may be a 20% decline in efficiency. Even under favorable conditions, efficiency won't exceed 35%.

Series regulated linears offer good voltage and are fairly insensitive to line frequency shifting. The cost is moderate, but due to poor efficiency, they become expensive to operate. This type of supply is widely used in audio amplifiers and may be found in a wide range of electronic equipment. Some laboratory supplies are series regulated linears, although today, laboratory supplies may be based upon a multitude of various de-

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	FD340	39.00	+5V, 0.5A/ 0.7A PK.	+12V, 0.9A/ 1.8A PK.	——	——	CP340	FAA-512	2BXFD
OPPY DISK 4"	FD323	61.00	+5V, 2A	+12V, 4A	——	——	CP323	FBB-512	2BBXFD
	FD205	76.00	+5V, 1.0A	−5V, 0.5A	+24V, 1.5A/ 1.7A PK.	——	CP205	FBAA-45W	2DFD***
OPPY DISK	FD206	97.00	+5V, 2.5A	−5V, 0.5A	+24V, 3.0A/ 3.4A PK.	——	CP206	FCBB-90W	2PFD
	FD162	89.00	+5V, 3.0A	−5V, 0.6A	+24V, 5.0A/ 6.0A PK.	——	CP162	FNBB-140W	2PFD***
RSCI	FD272	69.00	+5V, 1.7A/ 2.2A PK.	−5V, 0.15A/ 0.2A PK.	+24V, 0.2A/ 3.0A PK.	7-10V UNREG 1.2A/10A PK.	CP272	N/A	2PRD

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sign techniques. Switching-regulated-supplies are more efficient than linear regulated-supplies, by at least a factor of 2, due to pass transistors not drawing current continuously. They are switched "full-on" and "full-off," reducing wasteful power dissipation. The term *"switcher"* can apply to a number of different designs where pass transistors are switched from 60Hz to about 200kHz, adjusting the output to line and load conditions. The term generally describes a supply with a designed-in multitransistor inverter regulator, operating at some constant frequency (usually 20kHz). These supplies have the ability to shut-down, in the event of a power failure.

Frequencies less than 20kHz yield audible noise in the form of a hum, and frequencies higher than 40kHz yield complex radio frequency interference problems. They may also create manufacturing problems because the selection of components becomes limited with higher frequency ranges.

Due to various design innovations and component enhancements, commercial switching supplies are common in outputs ranging from 25W to more than 1000W, with single, dual, and triple output capability. They are used in portable equipment where energy must be conserved (such as computers and computer terminals). Compared to series-regulated supplies of the same rating, switchers occupy about one-third of the volume, and are much lighter in weight. Switchers have been available for about 17 years, and most commercial sales have occurred within the last 8 years due, in part, to the need for energy-efficient circuitry. New and improved switching transistors, very low-leakage electrolytics, and more efficient Schottky diodes have generated many improvements. MTBF's are ranging from 3 to 8 years, presently.

Reducing Costs

There are ways for a design engineer to create less costly units which are more reliable and a little less cumbersome in their complexity, by designing with his own performance specifications in mind. It is not all that difficult if the designer knows a great deal about the idiosyncrasies of the load that he would like to regulate with this supply. The first consideration here is the surge requirement. A duty cycle must first be specified and any components with safety factors in excess of the circuit's real needs must be eliminated. Safety factors (i.e. $V_{cc} \simeq 150\%$, $I_c \simeq 150\%$), must be considered by the designer, for peak requirements. Here, please note that the actual load *must* be known, for best engineering, compatability and ease of design. We should further consider voltage regulation requirements together with the need for low output impedance (0.015Ω from DC to 100Hz). In most cases we need a constant output (DC) in the presence of line/load variations.

There have been tremendous strides in the MOS FET IC component technology, aimed at diversification of the power supply design task. The design effort here has ejected our 20Hz to 30kHz spectrum well above 100kHz, without attaching cumbersome stigmas, such as size and weight. Back in the 1970's the μA723 regulator was introduced, and later began to revolutionize supply design. Now various types at all kinds of ratings are around, and they are further simplifying power supply design. However, there are still plenty of little things left to complicate the job for you! Evolutionary to the μA723, many voltage reference chips are performing very well, and achieving very high accuracies of ±0.20%. In addition, bipolar devices are attaining new switching speeds, and switching high-current in 1.5–1.8μs, at voltages of 1KV+.

The last basic design item is the transformer. Designers are limited to *smallest-possible-volume* designs, and a *tiny* transformer core is essential. Transformer designers use the standard equation:

$$A_cN_1 = \frac{E_{in} \times 10^8}{4.44\ fB_{max}K}$$

where:

A_c = Area of the core; N_1 = Number of turns of the primary; E_{in} = The applied EMF; (Volts); f = switching frequency; B_{max} = The flux density of the core material (max.); and K = The stacking factor of the core material.

Here it is simple to see the two ways in which the size of the transformer may be reduced: increase the frequency, or use a material with a higher flux density.

As can be seen, in any complex piece of electronic gear, the supply system becomes a quite complicated sub-level design. Following some of the guidelines below will aim you in the appropriate direction:

(1) AC Output, or DC output? What waveform?
(2) What oscillators? At what frequency?
(3) What is the P_{out}?
(4) What is the V_{in}? and the V_{out}?
(5) What is the t_a(°c)?
(6) What do you know about the load? It's regulation? Extreme conditions?
(7) What about efficiency? RFI? and mechanical against electrical constraints?

If you can effectively answer these basic questions, then consider:

(8) Frequency stability.
(9) Transistor configurations (electrical)? How many?
(10) How to suppress line-transients; how much suppression?
(11) What type of mechanical design should envelope this supply?
(12) What about cooling? Heat sinking? Fault detection?

Once you have accomplished this level of basic research and application into your supply design, you will be able to begin designing the appropriate circuit. □

Meeting the New Radio Interference Standards

by Robert Brunelle

The Federal Communications Commission recently introduced new regulations for Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) in electronic systems equipment. These regulations will almost always require that manufacturers use shielded cable to make external interconnections for data communications.

The new regulations take effect on October 1, 1983. After that date any electronic device or system that generates and uses timing signals or pulses at a rate in excess of 10,000 pulses (cycles) per second and uses digital techniques must meet the limits set by the FCC (**Table A**). So must any device or system that generates and uses radio frequency energy to perform data processing functions. Class A systems include computing devices marketed for use in commercial, industrial or business environments. Class B systems include equipment marketed for use at home as well as in the office.

Robert Brunelle is a Senior Product Engineer with the Electronic & Industrial Cable Div./Brand-Rex Co.

Any system generating radio frequency to perform data processing functions must meet FCC standards.

Types of Interference

Interference can take several forms, including electromagnetic radiation (EMR), EMI, RFI and electromagnetic pulse (EMP).

EMR is radiation generated by electrical means. It ranges from a stationary magnetic or electrostatic field, to high frequency changing fields, to transmitted waves of radio frequency.

EMI is EMR that causes an undesirable response in the function of electrical equipment in the low frequency range of 1 Hz-10KHz.

There are two forms of radio frequency interference: conducted RFI and radiated RFI. Both are forms of EMR that cause an undesirable response in the high frequency range of 10KHz and above. In conducted RFI, interference is fed back to AC power lines from a device. The power lines act as

FCC REGULATION LIMITS

SPECIFICATIONS:
Radiated RFI will be limited as follows:
Class A Computing Devices

Frequency (f) (MHz)	Distance (Meters)	Maximum Field Strength (μV/m)
30-88	30	30
88-216	30	50
216-1000	30	70

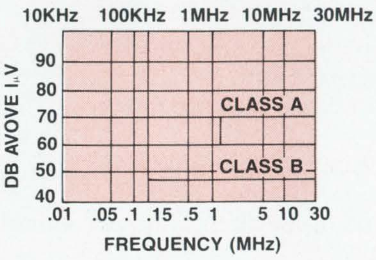
Class B Computing Devices

Frequency (f) (MHz)	Distance (Meters)	Maximum Field Strength (μV/m)
30-88	3	100
88-216	3	150
216-1000	3	200

Conducted RFI will be limited as follows:

Frequency (MHz)	Maximum RF Line Voltage (db above 1μV) Class A	Class B
0.45-1.6	60	48
1.6 -30	69.5	48

CONDUCTED EMISSION LIMITS



Note: Conducted limits in the frequency range of 10 to 450 kHz are under consideration.

transmitting antennae. In radiated RFI a device and its interconnecting cables act as an antenna radiating interference into the atmosphere.

Electromagnetic pulse is EMR of large magnitude resulting from the detonation of nuclear weapons.

An Electromagnetic Compability (EMC) test measures the equipment's ability to tolerate EMR produced by other devices while not itself producing EMR.

Proper Shielding

Minimizing outside interference is the primary objective of the FCC regulations. Thus the design engineer must select the appropriate wire, cable and shielding to minimize outside interference.

Whenever any of these forms of interference exist, a shielded cable must be used. The shield, a conductive envelope placed around the conductor or group of conductors, provides an electromagnetic barrier against interference.

The type of shielding used in a specific system is chosen with respect to type of field (magnetic or electric) and frequency present in the operating environment. Shielding variables to be considered may include material used, the method of application, and its thickness.

Designing The System

Avoiding the delay in redesigning a non-compliant system can best be accomplished by involving the cable manufacturer in the design plan at the beginning. Although equipment manufacturers may be concerned about protecting proprietary designs, agreements with the cable manufacturer can allow systems designers to use the cable manufacturer's expertise and capabilities without fear of piracy.

The ability of the cable manufacturer to build the right cable for a system can result in substantial savings. Simply shielding currently-used cable is not necessarily the most desirable solution. For example, one manufacturer previously used unshielded, unjacketed, manually terminated, twisted-pair flat cable. To shield and jacket this cable would double or triple its cost. A shielded round cable, however, was available at no additional cost, and worked well in the application.

In some designs it can be advantageous to build in a margin of safety. One equipment manufacturer, for example, used a shielded and jacketed 90–95% braid, which is considered a good shield. To meet the new FCC regulations, the company decided to use an additional shield and jacket. By this decision, the company avoided a number of expensive, time-consuming tests to make its system comply.

Size, Cost, Volume

The issue of interference also interacts with other system design considerations, such as limited space at systems installations, cost, and increasing volumes of data traffic.

Shielding a cable reduces interference, but always makes the cable larger and more costly. Since cable for many systems is installed under the floor, increased size can create a problem. Several manufacturers have developed miniature coaxial cable that takes up less space.

Those who are concerned with both interference and large volumes of data may wish to specify fiber optic cable rather than conventional cable. Since optical fibers transmit pulses of light, the cable is totally immune to EMI/RFI. Fiber optic cable can also transmit large volumes of data, making it suitable for applications where the data rate is expected to increase. And since it is much smaller than conventional cable, fiber optic cable is especially useful in applications where space is at a minimum.

Cost can be an important factor in choosing fiber optic cable. Not only is it more expensive than con-

VDE REGULATION LIMITS
(West German Regulations

SPECIFICATION:

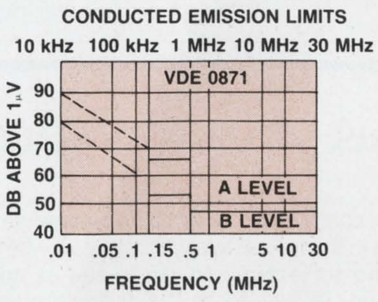
Conducted RFI is Limited As Follows:

Frequency MHz	Maximum RF Line Voltage (db above 1 μV) A Level	B Level
.15-.50	66	52
.50- 30	60	48

Note: Conducted limits in the frequency range of 10-150 KHz are recommended, not regulations.

METHODS OF MEASUREMENT

Test procedure is very similar to FCC test procedure.
There is one significant difference in the procedures—
The receiver bandwidth.
The FCC specifies a broader bandwidth in the lower frequencies, essentially making the conducted emission limits tougher than the VDE limits.
Bandwidth:
Tolerance in cycles per second (Hertz) expressing the difference between its limiting frequencies.



ventional cable, but it also requires redesigning the system, since special transmitters and receivers are needed.

Designing Systems

The entire system must comply with FCC regulations. Even though cable is properly shielded, the system itself may not comply because of other problems, such as with cabinet or connector design. Thus the cable must be tested in the system to make sure it complies. The cable manufacturer can also help here, recommending the right cable for the environment in which the system will operate. The cable supplier must also know what type of cable is being replaced if a system is being redesigned to comply. Few large equipment manufacturers use standard interconnect cables. Most use unique designs based on desired electrical characteristics. The final choice of cable depends on the original system design and how well it reduces interference.

International Regulations

Equipment manufacturers must also meet standards set by the countries to which they export. Many nations, including West Germany, France, and Switzerland, have developed emission standards for products ranging from household appliances to data processing systems (**Table B**). These standards are coordinated through the International Electrotechnical Commission in Geneva. In the United States, the American National Standards Institute in New York can provide information on international standards.

The issue has become so important that consultants now offer engineers training in interference measurement and control.

Materials And Capability

It is important to work with a company that offers a full range of products and materials to meet the FCC regulations. No one cable or shield can meet every design specification. A custom cable capability is also important, since the best cable to meet regulations may not be available off the shelf. □

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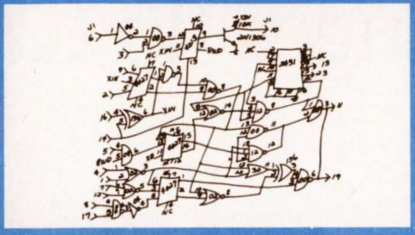
FREE-HAND SKETCH



"DS1" allows operator to digitize directly from a free-hand sketch. Vocal Output prompts operator as IBM Microcomputer collects data. Enter a "D" size in 1 hour. NO GRIDS. EDITS are performed in minutes.

COMPUTER PROCESSING

HP1000
DG Nova 4X, Eclipse, MV 8000
DEC VAX, PDP11
UNIVAC
HARRIS
IBM, plus others

Computer straightens slanted lines, uses correct size symbols and enters alignments among symbols entered by user during input. Drum plotter or Electrostatic plotter output.

CONNECTION NET LISTING

AD123789 GENERATED 4/10/80 AT 3:01:00 PAGE 1

SIGNAL NAME	UNIT	PIN	SHEET	ZONE
NET001	J1	6	1	A1
NET001	U1	1	1	A1
NET002	U1	2	1	A1
NET002	J2	1	1	A1
NET003	J1	3	1	A1
NET003	U2	2	1	A1
NET004	U2	3	1	A2
NET004	U3	12	1	A2
NET005	U2	8	1	B2
NET005	U2	13	1	C2
NET005	U11	13	1	D2
NET005	U7	10	1	D2
NET005	U4	10	1	C2
RWD	U2	5	1	C1
RWD	U3	8	1	B1
XIN	U3	11	1	A2
XIN	U6	1	1	B2
XIN	U8	6	1	B2
XIN	U4	3	1	D1

BILL OF MATERIALS

BILL OF MATERIALS FOR DRAWING NUMBER AD123789

ITEM	QTY	PART NUMBER	DESCRIPTION
1	4	054-4000	SN7404N
2	12	054-002	SN7402N
3	8	054-6080-67	RESISTOR 1.5K 1/2W 5%
4	2	079-5784-1	ZENER DIODE 1N821 6.2L

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
CR1	079-5784-1	ZENER DIODE 1N821 6.2L
R1	054-6080-67	RESISTOR 1.5K 1/2W 5%
U1	054-4000	SN7404N
U2	054-002	SN7402N

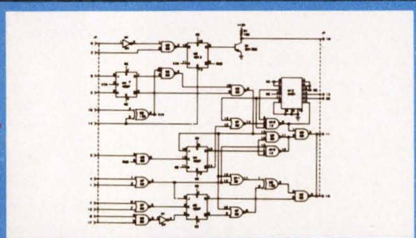
"DS1" automatically provides Net and Bill Lists directly from data base of digitized schematic.

P.C.B. ROUTER INTERFACES

ASI-PRANCE
AUTOMATE '80
COMPUTERVISION
REDAC
SCICARDS™
others available

"DS1" interfaces to P.C.B. Routers, Wire Wrap, Simulation and Test Programs.

UPDATED SCHEMATIC



"DS1" performs Back-Annotation from a "Was-To" list derived from the P.C. Router. "Back-Annotation" automatically updates the schematic to agree with the circuit board component placement.

Write 7 on Reader Inquiry Card

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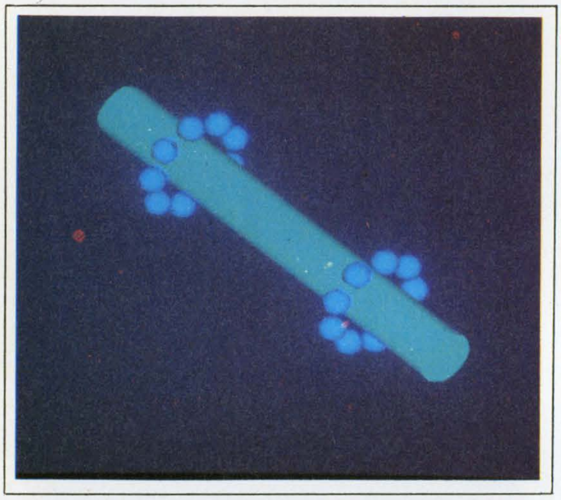
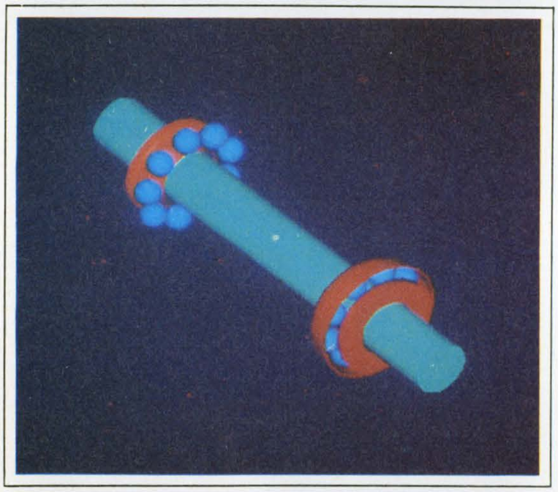
CAD/CAM: The Acronym Changes To CAE

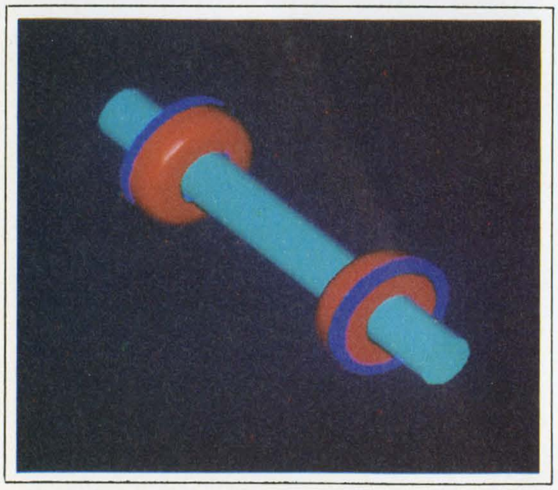




by Dave Wilson

Acronyms are in no short supply in the computer industry. And, as in many fast moving industries, such acronyms may become obsolete or take on a new meaning. Computer-aided design/Computer-aided manufacturing or CAD/CAM for short, is such an example. Evolving rapidly during the last decade, the industry has evolved into two camps: those who design using computers and those who manufacture using computers. In the future, the increasing processing capability of such computers may radically change this situation, as designers find that they are able to transfer their designs directly to machines that will produce prototypes within a matter of hours. CAD/CAM will then become one entity—that of computer-aided engineering (CAE).

At present, CAE systems are made up of both CAD and CAM.



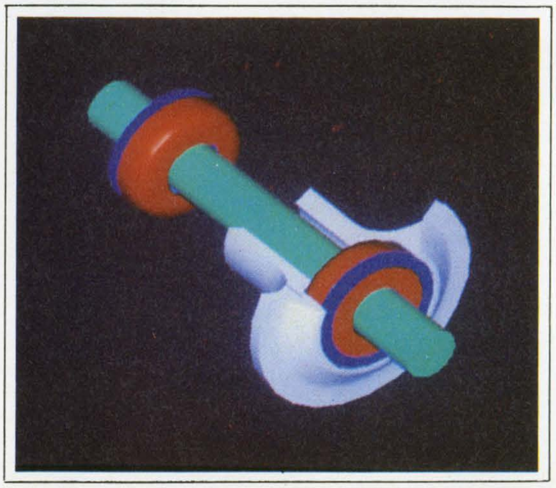


Photo sequence courtesy of Lexidata

The designers who work with computers on engineering projects may find that the systems produce faster, more accurate and more testable designs. However, to prototype such designs may involve the production of numerical control tapes or disks for systems that are not compatible with the original system the product was designed on. Such systems are only just being offered as total packages to solve this problem. To understand where the CAE market is today it is first necessary to examine what is on offer to the computer-aided design engineer, then to the system integrator and finally to the manufacturer who wants to be involved not in CAD or CAM but CAE.

CAD: The Mechanicals

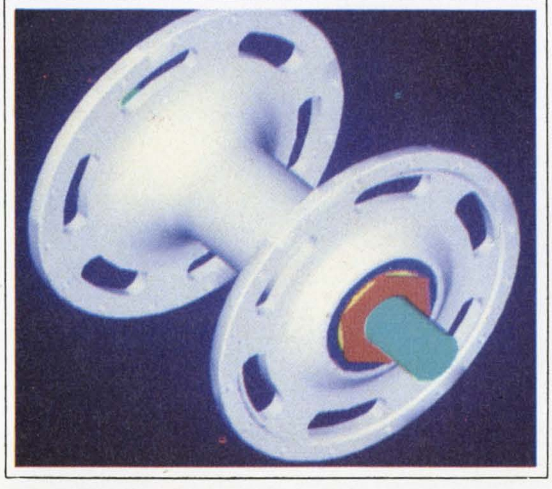
In 1981, 41% of all CAD systems shipped were to manufacturers involved in mechanical design with electronic and electrical applications taking second place with 28%. Such systems may have been sold as total solution packages where both computing power and software are supplied or part-solutions where either the software has been supplied for the user's own computer or just the hardware was sold, leaving the user to find his own software solution. Either way, the designer will find himself sitting at one of three types of terminal: a host-based terminal with no computing power of its own (unintelligent), a semi-intelligent host-based computer terminal or a stand-alone terminal capable of performing all of the design functions. CAD systems have followed closely the path of the computer itself. Previously, manufacturers wishing to incorporate such functions as geometric modelling, design drafting, finite element modelling and production of numerical control data needed a large amount of computing hardware. Their only solution was mainframe computers.

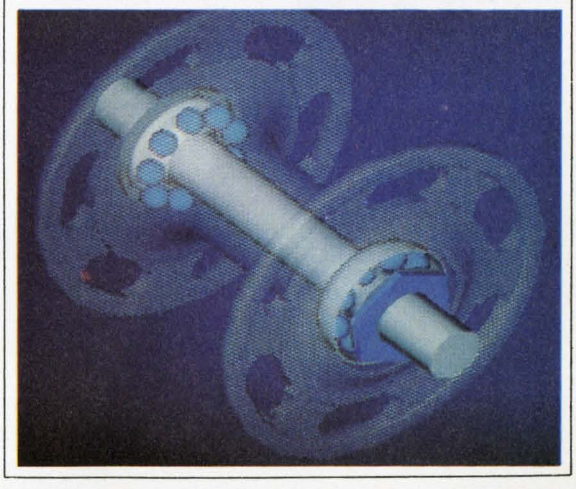
Designers find that they are able to transfer their designs directly to machines. CAD/CAM will then become one entity: CAE.

Now, with the introduction of such microprocessors as Motorola's 68000 and AMD's 2901, the ability to perform this processing is being transferred to the local workstation. And, as the workstations have become more intelligent, so too the large mainframes have become increasingly redundant. The reason: cost. Even in complicated designs, such as aircraft modelling, where the use of a mainframe computer may still be needed, such intelligent terminals can be used to reduce the processing overhead of the main frame. To reduce this overhead further, many manufacturers of stand-alone or semi-intelligent terminals have taken advantage of the concept of local area networking. This has allowed individual workstations and terminals to be tied together and for a large data base to be shared among them. As with terminals tied to mainframes, the most important part of any CAD system is the data base itself. Many applications of CAD systems involve tailoring existing parts to a new application, and to serve these applications libraries of parts are needed. While intelligent CAD stations may not yet be able to replace host mainframes for the most complicated designs, they are moving in quickly.

What's Available

According to Megatek's John Moreland, users of CAD systems first look at the job they have to perform and are open to a number of ways of doing it. In the past, this may have meant evaluating only a few systems. Now, literally hundreds are available. Computervi-





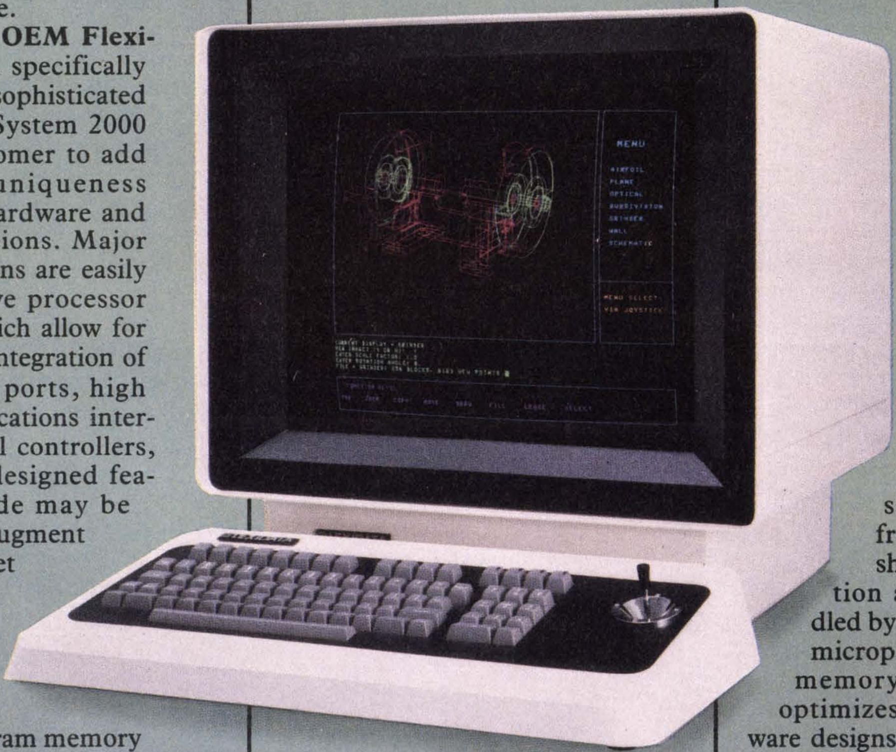
Introducing a new, improved way to give your competition headaches.

The Lexidata System 2000 is more than a new standard in high performance graphics terminals. It's a real competitive edge. The System 2000 is a family of high resolution, intelligent graphics terminals that give you the latest developments in raster technology at an unbelievably low price.

1. Outstanding OEM Flexibility. Designed specifically for OEMs and sophisticated end-users, the System 2000 allows the customer to add value and uniqueness through both hardware and software extensions. Major system expansions are easily achieved via five processor option slots, which allow for the convenient integration of multiple serial ports, high speed communications interfaces, peripheral controllers, and customer-designed features. User code may be downloaded to augment the instruction set and achieve a distributed graphics processing environment. Additional program memory (up to 1.28MB in 128KB or 256KB increments) can be installed using the Processor bus option slots.

2. Cost Effective Ergonomics. The high resolution display area offers the Lexidata unique functionality of four hardware-assisted, user-definable workspaces. With special attributes for each workspace, the System 2000 allows maximum flexibility for user tasks. These workspaces reduce the overall system costs by eliminating the need for a separate alphanumeric display and a menu space on the digitizer work surface.

A detachable keyboard with RS-232 interfaces and integral proportional rate joystick allows easy text and graphic entry.



3. Superior User Friendliness. The System 2000 has a multitasking, PROM-resident operating system, which uses an English Command Structure for text and graphics generation, display manipulation, and local programming. The Command Structure is designed for easy functional expansion.

4. Tektronix PLOT-10™ Compatibility. The System 2000's PLOT-10 compatibility is the best in the industry. User experience has shown that the System 2000 is quickly and easily installed into a PLOT-10 environment.

5. Black and White, $8250.* Color, $11,621.* With a resolution of 1280 x 1024, the System 2000 sets the standard for high resolution raster terminals. Black-and-white configurations are 50/60Hz noninterlaced, providing stable, flicker-free graphics. Color configurations are interlaced with long persistence monitors, and provide 16 simultaneous colors from a palette of 4096 shades. Display generation and control are handled by a Motorola MC68000 microprocessor, whose large memory address capability optimizes firmware and hardware designs. Design aids such as zoom, pan, text scroll, and independently controlled cursors are standard, and an 11" x 11" data tablet is optionally available.

If you are interested in evaluating the System 2000 for your low-cost graphics system, call (617) 663-8550 or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

LEXIDATA

The clear choice in raster graphics.

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*U.S. dollars for OEM quantity of 50.

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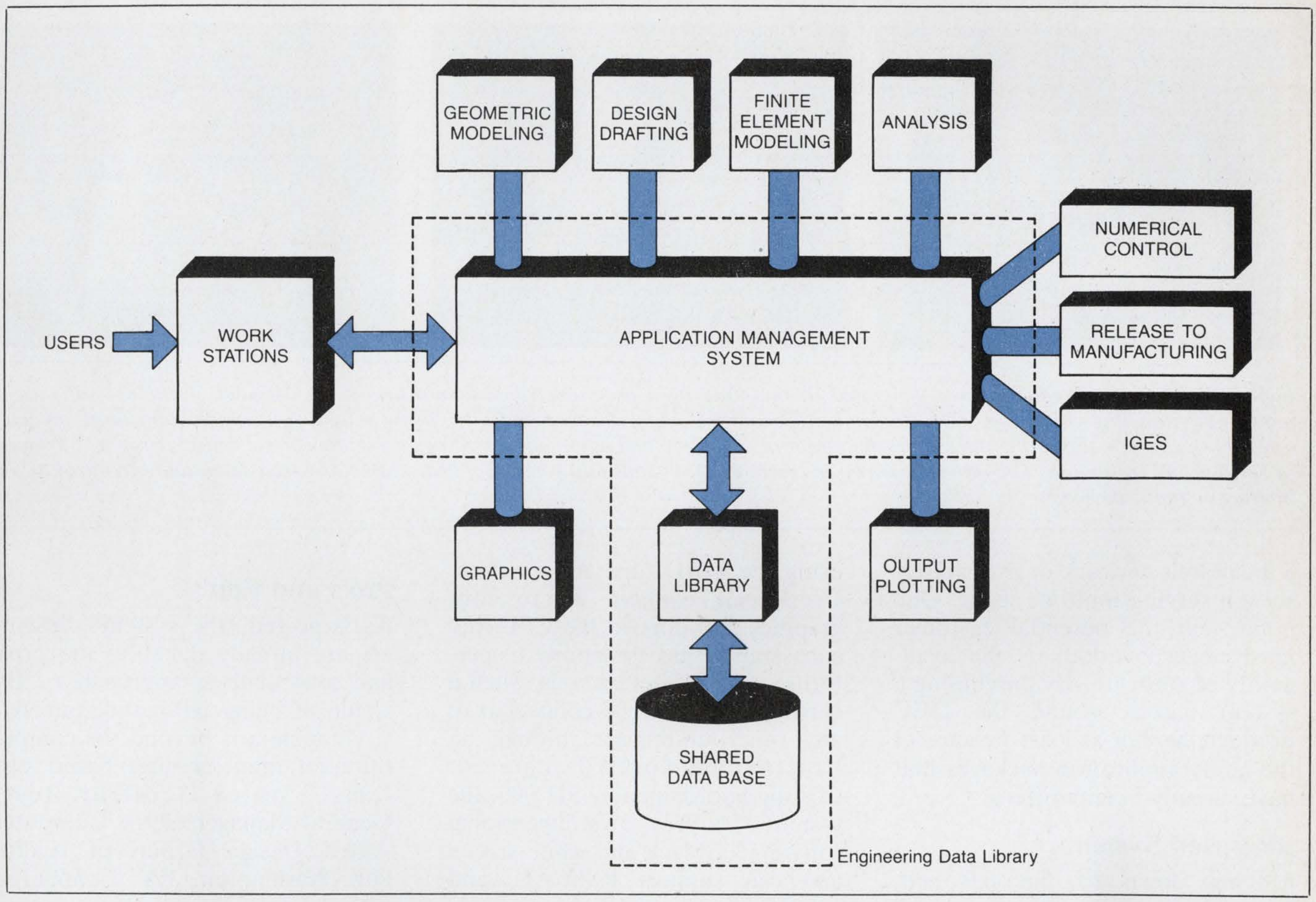

Figure 1: Control Data's ICEM solution provides access to applications, workstations, training, consulting. The Engineering Data Library provides an Application Management System, through which the user can access the CAD/CAM functions of geometric modeling, design, drafting, finite element modeling, numerical control, and release to manufacturing. The Engineering Data Library also provides access to data bases that can be shared by the application functions. Plotting output can be generated and data transmitted in or out of the system via IGES (Initial Graphics Exchange Specification).

sion is alone at the top of the turnkey market with one third of the market, based on estimated 1981 turnkey system revenues, and five other firms with market shares ranging from 7.2 to 13.1 percent, make up about 53 percent of the market collectively, and some 25 others compete for the remaining 15 percent.

At the top end of the market, mainframe manufacturers are getting together with terminal vendors to provide complete or turnkey packages. Under the terms of a recent signing between Digital Equipment Corporation and Ramtek Corporation, Digital supplies the VAX computer power and Ramtek supplies its Marquis graphics display. As for software? This will be provided by a number of software vendors who have signed affiliation programs with two firms. A complete package from three independent vendors, marketed jointly by two of them!

Also based on the DEC VAX family is Autotrol's GS-32 system which the company claims to be the first integrated 32-bit CAD system of its kind. Supplied with application and software packages, products can be completely designed and analyzed on the system and the resulting data can be accessed by manufacturing personnel for use in designing machinery and in developing control parts programs. And, to meet customer needs, a VAX can be purchased as part of a GS-32 system of Autotrol's software and workstations can be interfaced with an installed VAX. Potential buyers of CAD systems who find these announcements fairly awesome may like to be reminded that many companies are now providing training, consulting and support for their systems. Control Data Corporation is but one example. By hiring the company's CAD system, the user can access the CAD functions of geometric modelling, drafting, finite element modelling and numerical control, all without the cost of purchasing a system of his own.

For many applications in CAD, the use of a VAX is not necessary and many users will find that an LSI-11/23 or 16-bit μP based terminals will fit the bill. Introduced in July this year, the AEDS11 from Advanced Electronic Design is an LSI-11/23 based system that may be used as a stand-alone, as part of

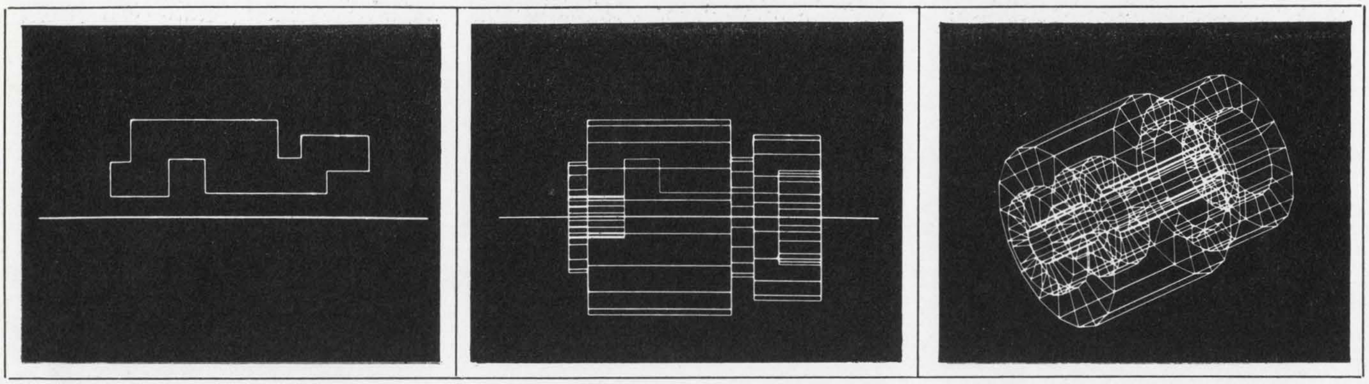

Figure 2: The above sequence was generated in real-time by a program which demonstrates the Megatek Template software's interactive modeling capability. The user inputs the initial skeletal drawing and then, using only a few simple subroutine invocations, the program allows the interactive definition of a surface and automatically draws a 3-dimensional object using a "surfaces of revolution" technique. The object is drawn in a matter of seconds and can be rotated, scaled and translated under control of an interactive input device.

a local area network or as a master station serving multiple users. One point that the potential customer must never overlook is the availability of software. By purchasing a system based around the DEC product, he can at least be sure of the many application packages that have already been written.

μP-Based Systems

Moving down to the μP end, Forward Technology's "Gateway" graphics workstation is based around Motorola's 68000, features 256K bytes of RAM, and operates using the UNIX operating system. Users can connect up to four graphics monitors to the CPU and each station has the ability to perform stand alone functions. Such a cluster could then be connected to any other equipment through an Ethernet network, if required. Costing approximately $11,000, the system features two-dimensional software, a black and white screen and can support PASCAL, and BASIC.

Pro's and Con's

As expected, the system's designers are already debating the pro's and con's of these approaches. "By virtue of being μP-based, our Ay-CAD system is beyond the competition of minicomputer based systems," states Geoffrey Best, General Manager of the Computer Aided Design Group of Aydin, Fort Washington, PA. Configured with 3 Intel μPs two math co-pro-

CAD/CAM For Personal Computers?

While directors at board meetings across the nation ponder over the value of CAD/CAM, they may find that their five-year old son is already playing with his own scaled down version in his bedroom. Now, owners of Apple II and IBM PCs can record the x, y, and z co-ordinates of any three dimensional object with The Space Tablet, a Spatial Digitizer from Micro Control Systems, Inc., Simsbury, CT.

Complete with the Space Graphics or Penguin Software's Complete Graphics System II, The Space Tablet consists of a sturdy, 13.5″ by 16″ clear lucite tablet on which is mounted an easy-to use precision machined aluminum and delrin arm. Either of the Tablet's two available models can be utilized as a two-or three-dimensional digitizer. The professional model provides an additional axis of rotation, or fourth degree of freedom. Price of the hardware/software package is less than $600.

Write 203

Dataram goes to extremes to satisfy LSI-11 users.

	DATARAM B23 PLUS	PDP-11/23 PLUS	DATARAM M23	PDP-11/24	DATARAM W23
CHASSIS	5¼" Front loading	5¼" Front loading	5¼" Rear loading	5¼" Side loading or 10½" Top loading	10½" Top loading with 80 MB Winchester
BACKPLANE	8 x 4	9 x 4	9 x 6	9 x 6	9 x 6
I/O MAPPING	None	None	Q-MAP	KT24	Q-MAP
BUS	22-bit Q-BUS	22-bit Q-BUS	22-bit Q-BUS and 18-bit Q-BUS	22-bit extended UNIBUS (EUB) & 18-bit UNIBUS	22-bit Q-BUS and 18-bit Q-BUS
MEMORY & PERIPHERAL SUPPORT	Up to 4.0MB, but limited to 256KB when using peripherals other than RL01/RL02 or RX01		Up to 4.0MB. No basic limitation on peripherals.		
PRICING	B23, M23, and W23 are approximately 35% less than comparable DEC systems in 1.0MB configurations. Additional 1.0MB memory modules from Dataram are about 40% less than DEC's equivalent 1.0MB memory. Contact us for actual price comparisons.				

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From Q-BUS Pricing to UNIBUS Performance

From top to bottom, chart the range of LSI-11 system performance you get from Dataram...and only Dataram.

It starts with our low-end B23 PLUS Q-BUS system at lower (much lower!) than DEC prices. And continues with high-end M23 and W23 Q-BUS systems that use Dataram's innovative Q-MAP™ I/O mapping module to generate a separate 18-bit bus from the LSI-11/23's 22-bit bus. Allowing you to put 4.0MB of memory on the 22-bit bus while interfacing your high-performance peripherals (RM02, TM11, RX02 and more) to the 18-bit bus. Giving you much more performance than provided by the PDP-11/23 PLUS, which supports only the RL01/RL02 and RX01 on its 22-bit bus.

It's possible, because Dataram's Q-MAP duplicates the functions of DEC's KT24 — which exists only in UNIBUS minicomputers from DEC — enabling Dataram's 4.0MB M23 and W23 minicomputers to be completely compatible with RSX11-M, RSX11-M PLUS, RSTS, UNIX and any other operating system which supports KT24 memory management.

Our W23 system goes a step further, integrating an 80MB Winchester drive and associated controller to provide even greater performance.

Q-BUS pricing...UNIBUS performance...in an LSI-11 megabyte system. Plus a wide range of disk and tape controllers, and related LSI-11 accessories. Only from Dataram. **Call us at (609) 799-0071. We'd like to tell you more about our family of LSI-11/23 based systems.**

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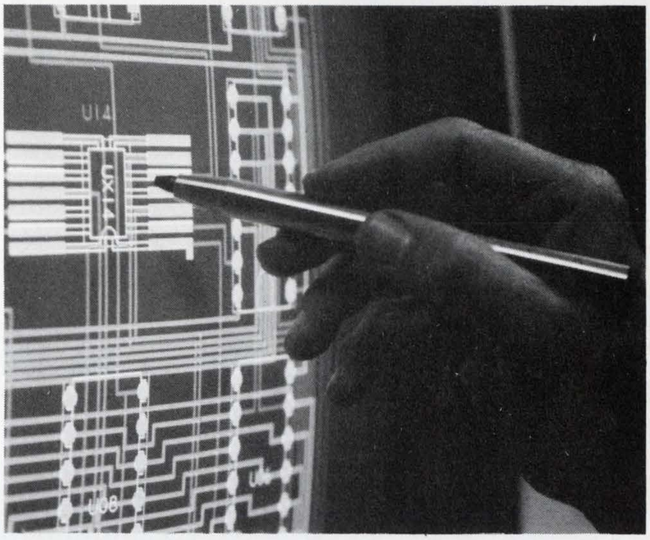
Light Pens And Graphics Tablets Speed Data Input



The light pen is only one of several computer graphic accessory devices that can allow the operator to interact with a raster graphic system. Other devices include keyboard and digitizer tablets.

Almost all graphics systems have keyboards. It is the universal operator input device. However, it is the other devices, such as light pens and data tablets that allow the operator the ease and speed required to make the CRT a truly electronic drafting tool. A light pen is a graphic input device that allows an operator to interact directly with the CRT display. Resembling a writing pen, the device actually operates in a reverse manner. It does not write on the screen, but rather reads the displayed images.

The light pen enables the operator to "pick" a point, character, or vector on the CRT screen and to cause the system to take some action on the object "picked." It contains a switch that is actuated when its tip is pressed against the CRT screen. It also contains a light sensor that is excited when the pen is pointed at an intensified point on the screen. The system's reaction to either the tip switch or the light sensor is dependent upon the application program.

The Spectragraphics System 1250 shown here emulates the IBM 3250 using a color raster display system. Due to inherent architectural differences between stroke and raster systems, some operations are performed in a different manner on the System 1250 than on the IBM 3250. in the System 1250, a light pen "detect" on the screen does not provide information as to which display element caused the "detect." Therefore, the System 1250 "re-builds" the image until it finds a displayed element which was in the field of view of the light pen. The buffer address of this element and its co-ordinates are then used to generate the IBM channel attention in the same manner as in the IBM 3250. This re-scan of the buffer program to get the pen detect information is transparent to the user.

Optional to the System 1250 is a data tablet that emulates the light pen functions. Using a pencil-like stylus, it has a switch that is actuated when its tip is pressed against the tablet. An internally-generated cursor is displayed on the CRT screen at the point that corresponds to where the stylus is placed on the tablet. An important facet of the tablet is that it has a two-dimensional surface analogous to that of the graphics display screen.

Naturally, each system has major advantages—and probably user preference along with software selection are the most important criteria for selecting each system. With the light pen, the direct interplay with the CRT is most important. It also allows the placement of a variety of menus on the screen from which the operator can choose.

Digitizer tablets have become the second most important interactive graphics accessory, next to the keyboard itself. Rather than using a stylus, maximum precision can be obtained from a cross-hair probe ("cursor") which has a flat or magnifying glass lens at the center of a circular loop. The advantage of this device is that both the probe and tablet may be provided with push buttons to facilitate various tablet functions. **Write 204**

cessors and a bit slice machine, the AyCAD system does not require host interfacing. In describing AyCAD, Mr. Best pushes the systems' data base together with its price of $75,000 as two of its biggest selling points.

Design Phases

The selection of CAE tools will depend to a great extent on the specific nature of the problem the designer has, the phases of development he wishes to automate, and last, but not the least, the capitol he can invest in product.

Typically, a design will pass through a conceptual phase, then on to analysis-finite element manufacturing studies and geometric studies. An FE analyst creates a mesh for the model that is then sent to the computer. When it is returned it may be compared to the original to study whether the stresses and displacements placed upon the model are tolerable—if not a redesign or rechoice of material may result. (Two well known finite-element analysis packages used here are STRUDL and NASTRAN.) In all stages of analysis, manufacturers are attempting to increase the "user friendliness" of their machines. Intergraph's (Huntsville, AL) FEMS (Finite Element Modeling System) provides the analyst with selections for loads, constraints, boundary conditions, automatic mesh generation and coarse/fine mesh transitions. The company delivers their VAX-based systems with FEMS and interfaces to both STRUDL and NASTRAN. The designer may also wish to study the relationship of his new part when integrated into an assembly. It is now possible to produce quickly, in color, and in 3 dimensions the various stages of such a design. At the Siggraph Show in Boston, Lexidata Corp, announced its new Solidview, an approach to displaying solid images that takes seconds as opposed to minutes by offloading the time consuming tasks of hidden surface removal and visi-

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

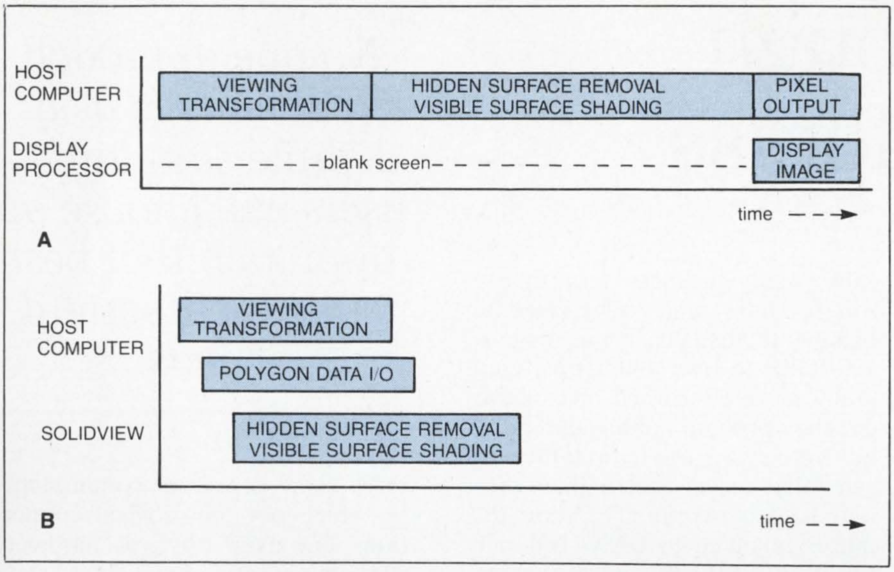


Figure 3: (A) The entire image is usually constructed at the host, and then sent, pixel by pixel, to the display processor. Not only is this process slow, it is I/O and host intensive, and requires large amounts of memory.
(B) With Lexidata's Solidview system, the workload is shared evenly with the host. As soon as the first polygon is computed, it is sent to the Solidview system, where hidden surfaces are removed, are smoothly shaded, and the result is displayed. The response is virtually immediate, and the solid model builds in a visually useful sequence.

ble surface shading from the host computer.

Numerical Control

After creating the part, analysing it, and examining the final assembly, the CAE system can be used to generate the Numerical Control toolpaths that will illustrate the cutting path of the machine tool to ensure that it will not collide with any part of the fixture.

The numerical Control data can then be used to produce a prototype of the part for evaluation.

The Future

The factory of the future is fast becoming a reality as manufacturers attempt to increase productivity and lower cost. Part of that future belongs to CAE. Coupled with rapid advances in robotics technology, it will not be long before the designer will be able to design, analyze and construct test samples with one day turnaround times. □

Sorting Through The LAN Morass

No one approach will emerge as a definite standard—users will choose an approach that best suits their system needs.

by Ed Pevovar and Brian McGann

No single topic in today's data communications industry is more intriguing and at the same time more confusing to a potential customer than that of local area networks (LANs). Heated arguments stressing the advantages of baseband technology as opposed to broadband abound. Pessimistic predictions of the 'inevitable' demise of entire LAN offerings along with their suppliers and customers have become common. Trade publication readers are deluged with announcements of entirely new LANs comprised of yet more combinations of LAN hardware and software technologies, and must somehow make sense out of 'developments' in the seemingly interminable effort to define LAN standards.

What Are LANs?

At least three broad categories of data communication networks exist today: computer system buses, LANs, and long-haul network. The most 'local' of these network types is the computer system bus. These are typically restricted to distances of less than 100 ft., and are designed for very high speed communication between processing elements of a classically integrated computer system. The least local of these is the long-haul network, that often spans great distances, interconnecting communicating elements located across a nation or even the globe.

LANs have characteristics which fall between these two. They typically span distances less than a square mile and offer medium bandwidth, usually in the range of 100 KBps to over 100 MBps. Generally privately owned and operated, they provide a more unregulated operating environment with generally easier access than most long-haul networks. The short distances involved in LANs generally result in relatively short propagation delays.

There are a number of characteristics of this 'middle range' network class which are attractive from an economic point of view. First, LANs allow sharing costly data processing resources among a large number of users. For example, the high cost of a sophisticated laser printer may be justified in a relatively small organization if all potential users of the printer are given ready access to it by means of the LAN. Second, LANs typically force some degree of commonality by which not only logical connections but even physical hardware connections are made. This 'standardization' feature is usually well received by an organization's technical support staff, making the administrative as well as technical difficulties of network maintenance easier to contend with. In moving to a single cable LAN, the number of physical communication cables in an installation is reduced, often resulting in a substantial increase in overall network reliability, and reduction in the cost of each interconnect.

LANs also offer a set of perfor-

Example: Deleting a file on an Internet	OSI Model
FTP›I'd like to delete 'MyFile'.	7: Application
FTPServer = call (program = FileDirectoryService, procedure = GetRemoteFileServer, filename = 'MyFile'); SuccessCode = call (program = FTPServer, procedure = Delete filename = 'MyFile', password = 'MyName');	6: Presentation
Gain access to an instance of the remote FTPServer using the password, 'MyName'. Once FTPServer is ready, send him the procedure call message and wait for his response.	5: Session
Despite a bad connection, repeat the message until the remote end has it exactly.	4: Transport
Although it may be impossible to guarantee success, make a 'best effort' to send the message to the appropriate local network on the internet.	3: Network
Send the message to the appropriate station on the local network and be sure a corrupted message is at least detectable.	2: Data link
Guarantee that communication cables may be plugged together and that everyone has the same understanding as to what constitutes a "1" and a "0" on the network cable.	1: Physical

Figure 1: The OSI Model: A Functional Representation.

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mance features not generally available from other network types. First, the standard interconnect model fundamental to the LAN makes it possible to integrate a tremendous diversity of data processing equipment. This model provides a practical baseline by which not only mainframes of different types may communicate, but equipment from previously separate classes, including printers, terminals, mainframes, minis and μCs, may all be interconnected and communicate as peers. Second, LANs provide a channel bandwidth which is generally well matched to the needs of the environment. In many distributed systems, communications is often 'transaction' oriented, with a certain amount of processing delay expected between a given 'command' and a subsequent 'response'. The result is that network traffic is often 'bursty'; even though it is desirable to move data between communicating parties at a very high speed when they are ready, they are ready only a certain portion of the time. The idle time may be used by other communicating parties that are ready, resulting in relatively high overall network utilization.

Third, the LAN may concurrently support a diverse set of communication services to meet different client needs. These range from the transport of simple internetwork 'datagrams', through reliable 'virtual circuit' connections, to more complex interprocess communication primitives. The tradeoff is generally the degree of network naivete allowed the client, offset by the amount of supporting communications overhead required. For example, datagrams provide a simple communications mechanism with minimal overhead, but generally there is no guarantee that any particular datagram will ever reach its destination. On the other hand, a client who is willing to pay a higher price in support overhead to gain access to a sophisticated inter-process communications facility, may perform such networking feats as making in-line procedure calls to remotely located processes with no direct concerns as to either the specific location at which they will be executed nor even the network by which access is made possible.

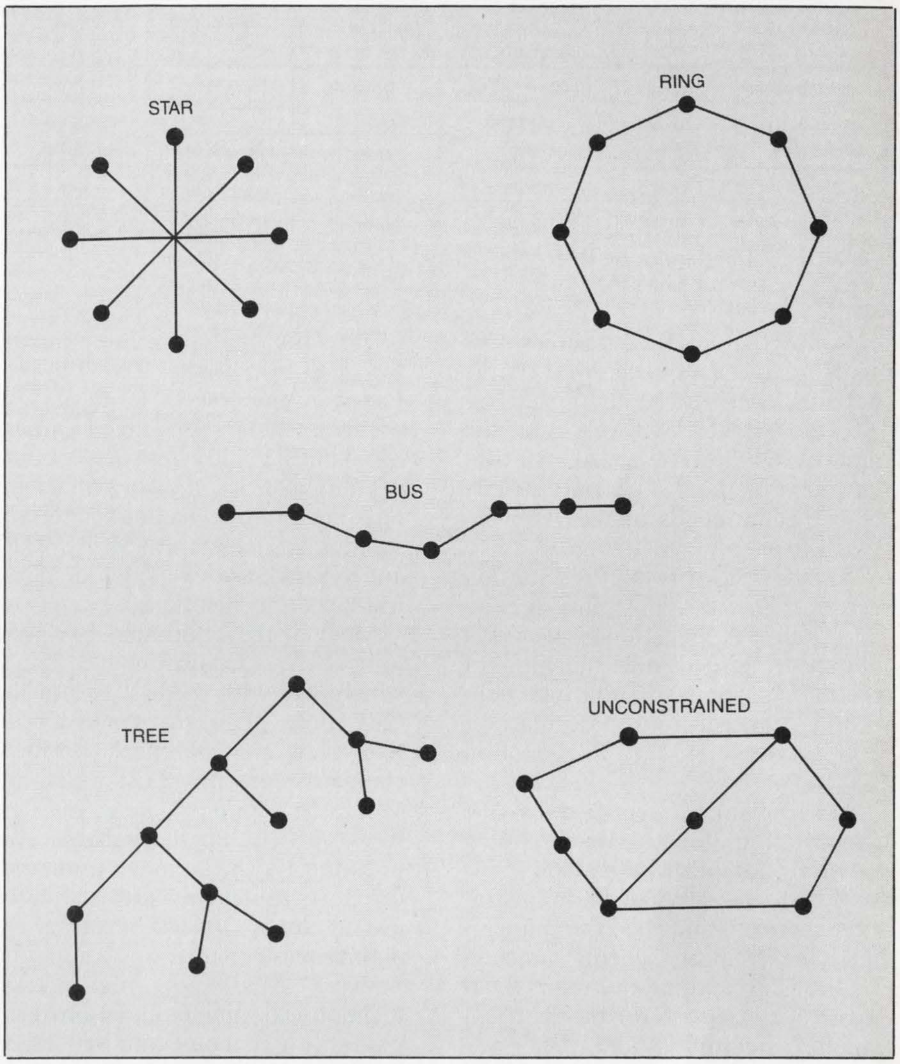

Figure 2: Schematic representation of network topologies.

If it is accepted that LANs effectively fill a useful niche, one is faced again with the problem of sorting through a morass of information to draw some intelligent conclusions. What is needed is a model—a structure within which these pieces of information may be filed and their relations kept in perspective.

The OSI Model

In 1979, the International Standards Organization published such a structure in its 'Open System Interconnection Reference Model.' This model organizes the various services offered by a general communications network into seven hierarchical layers. Each layer builds upon the services offered by the next lower layer; this provides a higher level service to the client layer above. No client service depends upon or even need be aware of the existence of the services of layers not immediately below it, and it provides its value-added services only to clients immediately above it. Another way to view the model is that each level offers its client a different view of the network—a view which becomes more conceptual and naive of the actual network implementation the higher up the pyramid one goes. A functional representation of the OSI Model is contained in **Figure 1.**

The topmost layer is known as the 'Application Layer', whose cli-

Topology	Reliability	Interface Complexity	Modularity	Flexibility	Cost
Unconstrained	very good	very high	moderate	poor	high
Star	poor	simple	moderate	poor	high
Ring	moderate	simple	good	moderate	moderate
Bus	good	moderate	good	good	low
Tree	good	moderate	good	good	low

Table 1: Characteristics of Different Network Topologies.

ents are the ultimate sources and sinks for the data exchanged on the network. It is by means of the Application Layer Services that the end user is directly served. All other layers of the model exist strictly to serve the needs of the Application Layer.

The next layer is the Presentation Layer, whose responsibility it is to allow the Application Layer the ability to discern the meaning of the data exchanged. Data type definitions and their bit representations are services of the Presentation Layer.

The Session Layer serves the Presentation Layer by providing 'session administration' and 'session dialogue' services. Administration services bind the communicating presentation clients into a relationship and unbind them. Dialogue Services control the data exchange, delimiting and data synchronization operations. Level Four is the Transport Layer. It provides a universal service for the transfer of data between communicating session clients. It is the Transport Layer's responsibility to optimize the cost-effective use of available communications services on the network to provide the level of performance in terms of reliability and throughput required by the client session services. At Level Three, the Network Layer provides a network connection service for data exchange between transport clients, hiding all routing and switching requirements from the client's view. Level two is the Data Link Layer. It supports the lowest level logical connection between communicating network clients. It provides the ability to gain access to the communications media, to address a set of data to a particular network client, and to subsequently release the communications media for use by others. The Physical Layer is the lowest level of OSI model. It defines the electrical and mechanical characteristics of the communications media and its interconnection. Familiar interface standards such as ANSI RS-232C and RS-449 are examples of physical layer specifications.

Most of the effort that has gone into LANs to date involves issues which deal with the first two of the OSI protocol layers. Only a relatively few comprehensive protocol standards currently exist which address the complete range of network services up through the Application Layer, although a number of efforts to develop such standards are underway. Indeed, a careful examination of the various competing network topologies, transmission technologies and modulation techniques which constitute the Physical Layer, along with the various network access methods, frame level formats and station addressing mechanisms which comprise the Data Link Layer will yield a fairly comprehensive survey of current LAN offerings.

The Physical Layer

The different Physical Layer implementations which are in common use today may be organized by means of three key attributes: network topology, transmission medium and transmission mode. For each attribute we can choose a set of criteria by which the relative strengths of each approach may be judged.

There are five major types of network topology: unconstrained, the star, the ring, the bus and the tree. These are schematically represented in **Figure 2. Table 1** shows the relative strength of each topology type in terms of inherent reliability, 'modularity' or the ease of adding new network nodes, 'flexibility' or the ease of adding new network connections between nodes, the complexity of the typical hardware and software network interface, and overall cost of implementation.

There exist three main types of transmission media generally used in today's LANs: these are twisted pairs, coaxial cable and optical fibers. Criteria useful in comparing the relative performance of different transmission media include maximum useable distance, noise immunity, topology versatility, ease of installation and maintenance, and cost. A comparison of the relative strengths of a number of different transmission media is included in **Table 2.**

In comparing the relative costs of different physcial level approaches, it should be pointed out that the cost of cable is generally insignificant compared to that of the supporting transceiver and controller hardware which may be required. Twisted pairs, coaxial cable and optical fibers are all inexpensive both in price and installation and it is generally the transmission mode which dictates the nature of the interface hardware and this in turn determines the overall cost of the physical layer implementation.

Transmission Medium	Bandwidth	Distance	Topology Versatility	Ease of Installation	Cost	Noise Immunity
Twisted pairs	low (6 MHz)	short	high	moderate	low	low
Coaxial cable	medium (300 MHz)	moderate	high	easy	moderate	high
Optical fibers	high (300 GHz)	long	moderate (bus and tree are difficult)	moderate	moderate	very high

Table 2: Transmission Media Characteristics.

The next category distinguishing physical layer implementations is the transmission mode. Today's LANs generally utilize one of two different transmission modes: baseband or broadband. **Table 3** illustrates the relative strengths of baseband and broadband transmission modes based on maximum distance, noise immunity, projected connection cost, the ability to support multiple communication channels and the ability to support passive rather than active taps.

Transmission Mode	Distance	Noise Immunity	Passive Taps	Projected Interconnect Cost	Multiple Channels
Baseband	moderate	low	yes	low	no
Broadband	unlimited	moderate	no	moderate	yes

Table 3: Transmission Modes Characteristics.

Broadband mode allows virtually unlimited distance with relatively good noise immunity. In addition, today's broadband systems generally yield a lower cost per connection than do baseband systems, although many expect that within a year or two the tables will turn. Baseband networking technology relies heavily on the CATV industry and as such already enjoys the advantage of component price reduction resulting from high volume production. On the other hand, most baseband interfaces, such as those for Ethernet, require fairly complex controller logic which today is only partially integrated at the circuit level. As a result, today's baseband controllers are characteristically costly. However, a massive effort has been underway over the last two years to squeeze integrated controllers for both the physical and data link layers suitable for baseband systems into only a few integrated circuits. The resulting cost per connection to the Ethernet, for example, is expected to fall to as low as $50 dollars within a few years.

The major disadvantage of baseband systems is their inability to support more than one information channel at a time. In defense, many supporters of baseband systems claim that the advantages in supporting voice and video on the same cable as data are minimal in light of the profusion of existing PABX systems. Others point to studies showing how voice traffic may be digitized, packetized, and indeed sent along with data on the baseband network. However, it is generally granted that if the simultaneous transfer of voice and video traffic along with data is a network requirement, then broadband is the only viable transmission mode.

Data Link Layer

The key attribute of Data Link Layer implementation is known as the 'network access method.' The access method is the mechanism by which a network node acquires, and subsequently releases a share of the total transmission medium resource to facilitate its data transfer. Criteria useful in judging the relative strengths of competing access methods include the degree of contention, bandwidth utilization, flexibility, expandability, and message end-to-end delay. A comparison of the most common access methods is included in **Table 4**.

Access Method	Degree of Contention	Bandwidth	Flexibility	Modularity	Message End-to-end Delay
Space division multiplex	low	poor	poor	moderate	low
Frequency division multiplex	low	poor	poor	moderate	low
Time division multiplex	low	poor	poor	moderate	low
Token ring	low	good	moderate	moderate	low
Slotted ring	low	good	moderate	moderate	moderate
Carrier sense multiple access	high	good	good	good	non-deterministic

Table 4: Comparison of Access Methods.

Access methods which are receiving the greatest attention today can be separated into three major types: those which provide dedicated allocation, those which use polling in some form or another, and those which employ random access. Dedicated access methods are those which permanently allocate a portion of the total transmission medium resource among the total number of network clients. They include Space Division Multiplexing (SDM), Frequency Division Multiplexing (FDM), and Time Division Multiplexing (TDM).

SDM access methods assume every node on the network has a dedicated physical line connecting it with a central communications processor. Accordingly, virtually contention free service may be obtained, at the expense of relatively high installation cost and low bandwidth utilization. The star network topology is generally associated with SDM systems, the PABX being representative of a common network employing the SDM access method.

With FDM, the total frequency spectrum of the transmission medium is split into a specific set of frequency channels. Each client of the network is assigned to one or more of these channels, providing essentially point to point service between communicating network nodes. Frequency channels may be statically or dynamically allocated, depending upon network complexity.

TDM works in essentially the same way as FDM, except the distribution of the transmission medium is by division in the time domain rather than the frequency domain. Network modes are permanently assigned an ordered time slot during which it has full access to the network transmission medium.

The major polling schemes in use today are known as the 'slotted' ring and the 'token' ring. The slotted ring generally assumes a physical ring network topology while the token ring assumes only a logical ring topology. In the slotted ring, the transmission medium resource is divided into slots of typically equal length which continuously circulate around the ring from one network node to the next. Each slot carries a header which indicates whether it is empty, or if it's not empty, to whom its contents are addressed. As each slot arrives at a network node, the node controller determines whether the slot is free or busy. If it is busy, and if the contained destination address matches that of the node, the controller copies the data from the slot, marks the slot free and returns it to the ring. If the slot is free and if the node has data to transmit, the controller writes the data to the slot, writes the destination address in the slot header, and sends it onto the ring.

Advantages of the slotted ring include its simplicity and its high utilization of available network bandwidth. Multiple nodes may concurrently write to free slots in the ring and the network as a whole very simply adapts to a wide range of bandwidths of attached devices. Disadvantages include the reliability weaknesses inherent in a physical ring topology and the fact that slots are fixed in length, which invariably offsets some of the advantages of high bandwidth utilization.

The token ring, for many applications, is an improvement over the slotted ring. In this access method, the ring structure need only be a logical construction; the physical topology may be virtually any type. A logical 'token' is passed by means of a network control message from node to node in an assigned sequence—the sequence itself constituting the logical ring. In some implementations, when a node receives the token, it has access to the entire transmission medium for potentially an unlimited length of time. If it has data to send, it maintains possession of the token until it is finished. Otherwise, it sends an appropriate message to the next node in the logical ring, thereby passing to it the token and relinquishing control of the transmission medium. The token ring approaches the high bandwidth utilization advantages characteristic of the slotted ring. Furthermore, since the token ring does not require a physical ring topology, it does not have the inherent reliability problems of the slotted ring. The potential for losing the token, however, does pose some new reliability considerations. In addition, error recovery mechanisms in general as well as initial startup and gracefully adding and deleting nodes from the ring tend to be fairly complex operations requiring relatively sophisticated interface implementations.

Random Access methods are simple to implement and are well matched to environments with a large number of intermittant users.

Random Access methods are the third type of network access methods in general use, the most notable of which is the Carrier Sense Multiple Access with Collision Detection (CSMA/CD). In this scheme, each node on the network is given an equal chance at any instant in time at acquiring control of the transmission medium. If a node is ready to send data onto the network, it first listens to see whether the medium is already in use. If the network is found to be idle, it immediately assumes control of the network medium and begins transmission. The node recognizes the possibility that another node may have at the same time also assumed control of the network and may concurrently be transmitting data, and so during its transmission it monitors the network to detect a collision. If a collision is detected, the node transmits a jamming sequence to be sure the competing node has also detected a collision, and then stops all transmission on the network. The node then performs what is called a 'random backoff' calculation to determine an exponentially increasing pseudo-random time interval during which it will wait before attempting to acquire control of the bus again.

Random Access methods are typically simple to implement and are well matched to environments with a large number of bursty users. The ability to support message broadcasting simultaneously to a large number of network nodes is also a feature. Major disadvantages include the non-deterministic nature of the network acquisition time due to the finite possiblity that a particular node's attempt to acquire the transmission medium may repeatedly result in a collision and may, in fact, never succeed at all. Further, under high load conditions in which messages are typically large, as would be the case if a number of users were concurrently transferring large files across the network, average network access time may become relatively large and the overhead incurred by each contending controller due to the resulting large number of collisions may grow annoyingly high.

Network Layer And Beyond

When we look to higher layers of the OSI model, it becomes clear that very little effort has gone into the development of LAN products which offer services above the data link level. A few 'turnkey' network suppliers offer application level services, but the ability of network us-

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ers to gain access to the characteristic services of each layer, independent of the others, is, in general, lacking.

One explanation might point to a general lack of systems level experience in integrating current LAN products. It is sometimes difficult for the user to appreciate higher level issues until he is faced with the practical problem of integrating lower level products into a comprehensive system in which useful work may be accomplished. Further, although a 'top down' product design approach is preferable in general, it probably does not make a lot of sense from a marketing standpoint to spend a great deal of effort generating products supporting high level services before the low level products upon which they depend are in place. Lastly, the difficulties in adopting appropriate protocol standards have not been limited to the physical and data link levels alone, but have manifested themselves also in arriving at protocols for the higher levels. In fact, although a number of standards organizations are currently groping with the problem of defining standards for the higher service layers, few comprehensive specifications have resulted. Final adoption of most is generally acknowledged to be at least a year or two away.

One exception is Xerox Corp's Network Systems (NS) protocol standard which includes one or more protocol specifications for all but the session layer of the OSI model.

Xerox Protocols

In September 1980, Digital Equipment Corp, Intel Corp and Xerox Corp (DIX), jointly published a specification for the data link and physical layers of a LAN called Ethernet. The technical motivation for Ethernet was to provide a simple, reliable and inexpensive means by which a number of products may be interconnected physically by means of a single patch of coaxial cable.

The DIX Ethernet specification took one of the first steps in achieving this goal. The physical layer specification describes mechanical and electrical characteristics of the bus cable, the cable connection, the bus transceiver and its interconnect cable, as well as the electrical signals and their characteristics on the network cable. The data link layer specification describes the method by which communications are addressed as well as the mechanisms by which access to the network cable is arbitrated between a number of potential users. It also describes the organization by which the bits of the messages to be communicated will be grouped into message frames.

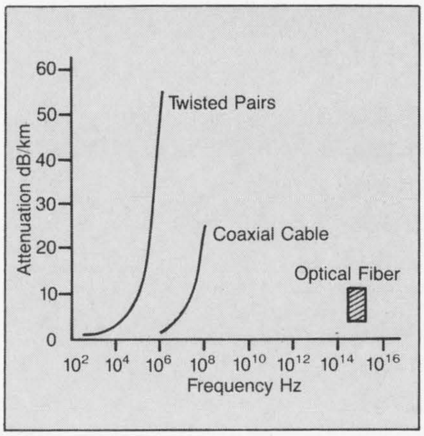

Figure 3: Comparison of transmission media.

It should be noted that the physical and data link protocol layers together comprise a 'best effort' message delivery technique; that is, although various mechanisms have been built into the protocol whereby delivery errors may be detected and in some cases acted upon, in general error detection capability is not supported and error recovery procedures are largely undefined.

The ability to guarantee error-free message delivery, however, is an absolute requirement of the communications backbone of a general distributed processing system. In addition, the ability to deliver messages across network boundaries, the ability to define standard data types within messages, the ability to support variable message lengths which in general have no relationship to frame length, and the ability to name, locate and utilize the various high level processing services distributed throughout the network are all necessary features of a practical, integrated system.

Xerox Corp, in October and December of 1981, took the next steps in specifying standards by which these higher level features could be realized. They published, the 'Clearinghouse,' the 'Internet Transport Protocols' and 'Courier: The Remote Procedure Call Protocol' standards as modular elements of their large NS protocol family.

The Internet Transport Protocols are actually a set of protocols which fit into the internet and transport protocol layers of the ISO Open Systems Interconnect Reference Model. These consist of the Internet Datagram Protocol at the network layer and a group of protocols at the transport layer, including the Sequenced Packet, Packet Exchange, Echo, Routing Information, and Error Protocols. The Internet Datagram Protocol supports the addressing and delivery of individual frames of data to destinations which transcend network boundaries. It is the workhorse by which all point to point communications on the internet are delivered and upon which all higher level protocols are constructed. The Internet Datagram Protocol provides only 'best effort' delivery service. The transport protocols provide various desirable facilities to support the exchange of streams of related frames between clients on the internet. These facilities provide end-to-end error-free communication paths, flow-control, internetwork routing information and some run-time diagnostics support.

The 'Courier' protocol fits into layer 6 of the OSI model. Its specification is extremely significant to the implementation of a distributed processing system of even the simplest type. Communication may be made transparent, allowing the system designer to deal with the higher level abstraction of making procedure calls to remotely located services. In fact, neither the actual geographical location nor the specific piece of supporting hardware upon which the service is implemented is of concern to the user;

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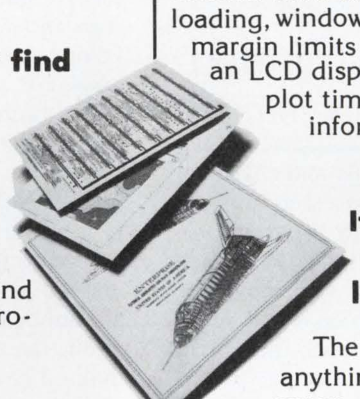

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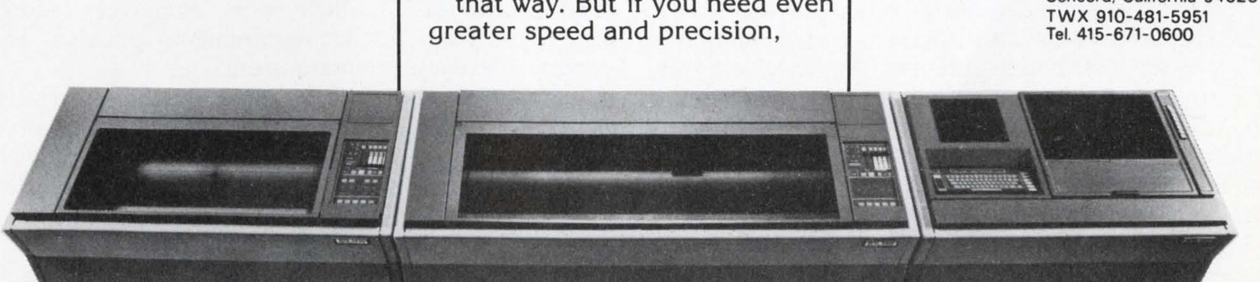

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the entire internet, potentially including a myriad of general and special purpose processors, may be dealt with as one large, amorphous, virtual processing system.

Courier supports the model of remote procedure calls and subsequent returns. It also defines a set of data types by which the contents of data packets are organized into 'messages,' independent of packet boundaries. Messages are in turn interpreted and given meaning by mutual agreement between communicating, high level processes. These processes need not be concerned with the details of the mechanisms by which their messages are formatted and transported across the internet, but instead deal with the contents of these messages by means of the high level and natural data type definitions they are familiar with.

For example, if in the course of implementing a given function, process A requires the services of process B to operate on a list of six integers followed by a variable length string of characters, process A merely makes a Courier procedure call to process B, passing it the list of arguments in the form with which it internally deals with them. It makes no specification as to where process B will be implemented, nor on what type of hardware, nor does it reformat in any way its internal representation of the arguments it passes to B; it merely assumes that the published services of process B are available to general clients of the internet and it makes a simple procedure call to gain access to them. Process A's view of the distributed system is by design exceptionally naive.

The Courier interface, in conjunction with the facilities of the lower level protocol layers, handles the details of reformatting the calling arguments into standard data types, structuring a corresponding 'Call' message, establishing an error-free communication path across the internet to the host at which process B is supported, starting up an instance of process B on that host and passing to it the original 'Call' message. The message is in turn broken down by process B's Courier interface into its component data elements in the internal representation which is natural to the environment of process B, going through the same set of operations in the opposite direction to return the results of the invoked procedure to the calling process. Finally, both Courier interfaces join to stop the instance of process B on its host, to break the communication path reestablished between process A and B, and finally to resume execution of process A.

As far as process A is concerned, it issued a simple procedure call from which it has subsequently returned. Its integer list and character string have been processed and it is ready to move on to the next processing function. It has remained oblivious to where and how the procedure was implemented, concerning itself only with the functionality of the service the procedure offers.

The ability to guarantee error-free message delivery is an absolute requirement for the communications backbone of a general distributed processing system.

With 'Courier' in place, the implementation of higher level services on the internet becomes straightforward. Filing, printing, virtual terminal support all may be implemented by means of sets of related procedures which are publicly defined, published and accessible to clients by means of Courier procedure calls. New protocols may be designed and implemented with a minimum of effort; all the facilities of Courier and the lower protocol layers remain intact and energy need only be expended on developing those portions of the higher level protocols which are actually new.

One special higher level protocol is the 'Clearinghouse.' The Clearinghouse is actually both a convention by which users, services and virtually all elements of the internet are named, and also a service itself, accessible by means of Courier procedure calls, by which those names may be retrieved and their meanings discerned. The Clearinghouse service can be thought of as a sort of "internet telephone directory."

Taken together, the NS protocol family published to date represents a significant advance in the development of an integration standard by which distributed processing systems can efficiently be realized. The Ethernet specification of 1980 provided a foundation. It was however, only the first step and insufficient alone to provide the higher level 'glue' required to easily interconnect distributed services for the purpose of creating an environment suitable for performing useful work. The Internet Transport Protocols specification was the next step and with 'Courier,' system developers are finally supported at a level by which their efforts may prove both technically efficient and commercially meaningful.

Ongoing Challenge

It is generally accepted today that no one approach will eventually emerge as a definitive standard for all applications; rather, it will remain the user's responsibility to make a choice from all existing approaches to arrive at a combination which most effectively addresses the requirements peculiar to his environment.

It is also clear that relatively little has been done by LAN product vendors to assist the user in solving the various higher level issues he inevitably will face in implementing a useful local area network. Although a few vendors offer a limited set of application level services, general access to each service layer of the network is typically unavailable. Even the emergence of widely embraced protocol standards which address the higher service layers appears to be some time away. □

Designing A 16032 CPU Card For The S–100

by Richard Kalish

The S-100 bus has been around for more than six years and now has become a recognized standard by the IEEE. The IEEE 696/S–100 bus can now be designed around with a high degree of probability that there will be compatibility between a variety of manufacturers and products. Although the bus was originally intended for an 8080 8-bit processor, the standard now has provisions for full 16-bit transfers between memory, I/O and the processor.

The IEEE 696/S-100 Standard for permanent bus masters is well documented for all bus operations.

To design a 16-bit 16032 processor board for the IEEE 696/S–100 bus, all other boards in the system must also be considered. The system should be able to remain the same except for the new processor board.

Design Requirements

In the design of a 16032 CPU card for the IEEE 696/S–100 bus, some basic design requirements must be established. Having established these requirements, we can then proceed to meet these goals and any other requirements that may become apparent in the process. The design goals are:

- Full compatibility with the IEEE 696/S–100 bus specifications for a permanent master.
- Compatible with existing 8-bit memory and peripheral boards as well as with newer 16-bit memory and peripheral boards according to the handshaking defined in the standard.
- On board sockets for the Memory Management (MMU) unit and the Floating Point Unit (FPU). These devices are to be optional parts so the board must be able to run without them installed for a minimum configuration system.
- Compatible with current IEEE 696 DMA devices for floppy and hard disk control.
- Ability to support the full vectored interrupt capability of the IEEE 696/S–100 bus.
- Capable of running with an 8-bit slave processor to allow both processors to share the bus in a time sharing mode.

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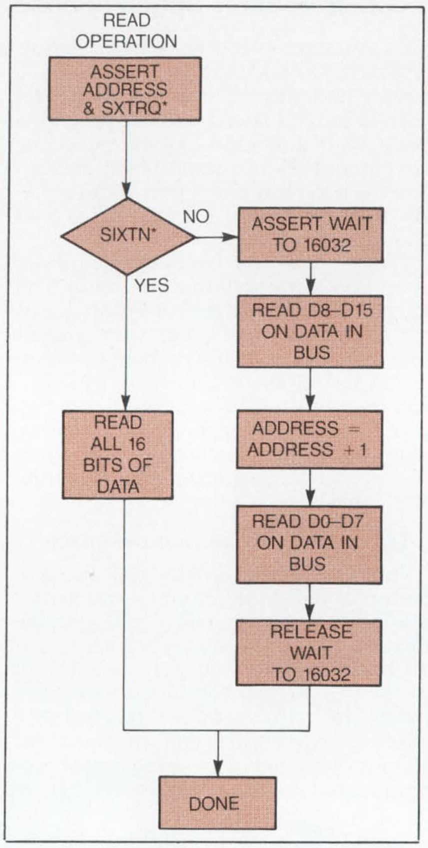


Figure 1: The read operation in the above flow chart is of the state machine which performs a second fetch from memory while the processor is held in a wait state.

The IEEE 696/S–100 Bus

Originally the S–100 bus was designed around the 8080 processor and an edge connector with 100 pins. As the bus grew and matured, the IEEE Microcomputer Standards Committee gave the S–100 bus a working number of 696. The specifications give detailed timing and physical requirements (see July 1979 IEEE Computer for original published standard) to allow the

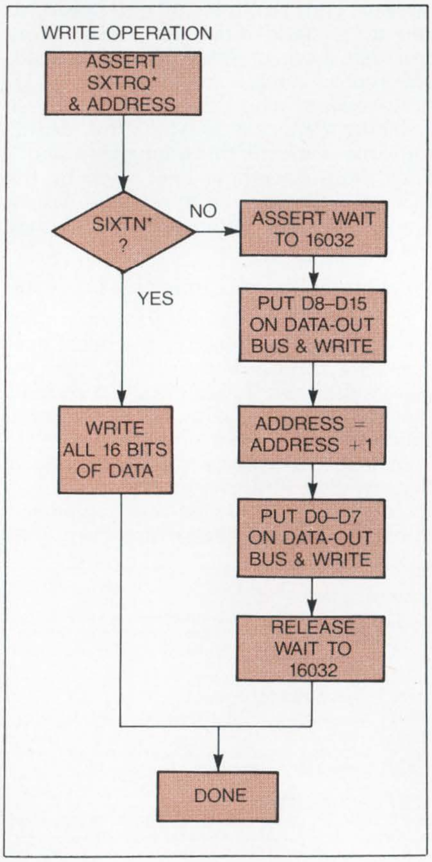


Figure 2: The write operation in this flow chart is for a state machine to perform a second write to memory when the processor is in a wait state.

designer to implement a board which should work with any other board conforming to the standard. This allows the end-user the flexibility of designing a custom system from a variety of manufacturers and have a high degree of success at integrating the system.

Bus Timing

Because the bus was originally designed around an 8-bit processor there are some major design requirements to get a 16-bit processor like the 16032 on the bus. Fortunately, the original bus contained two 8-bit unidirectional data busses for data-in and data-out from the processor. By defining two unused lines on the bus as sXTRQ* (sixteen request) and SIXTN* (sixteen acknowledge), transfer can occur on two 8-bit unidirectional data busses or one 16-bit bidirectional data bus. These changes can happen at any time in the system and the system can have a mix of 8-bit memory boards as well as 16-bit memory boards.

When the processor wants a word (16 bits) from memory, it will assert the address requested and drive the sXTRQ* line low. If the memory board addressed is a word wide board it will see the sXTRQ* signal and return a SIXTN* signal back to the processor within a specified period of time. This will tell the processor that a 16-bit wide transfer can be accomplished. If the processor does not receive the SIXTN* signal back, then it will assume there is 8-bit wide memory and perform two 8-bit fetches on the bus with address line AO low for the first fetch and high for the second fetch. This same process occurs for write to memory as well. This function allows a system integrator to replace an older 8-bit processor with a 16-bit processor and not have the added expense of adding all new memory boards. Eventually, to achieve the highest throughput, new memory which is word wide will be desired, but is not necessary.

There have been CompuPro memory boards available for over a year which will support 16-bit and 8-bit transfers depending on the processor used. These boards use the same sXTRQ* and SIXTN* signals to determine if they should switch between an 8–bit mode or 16–bit mode.

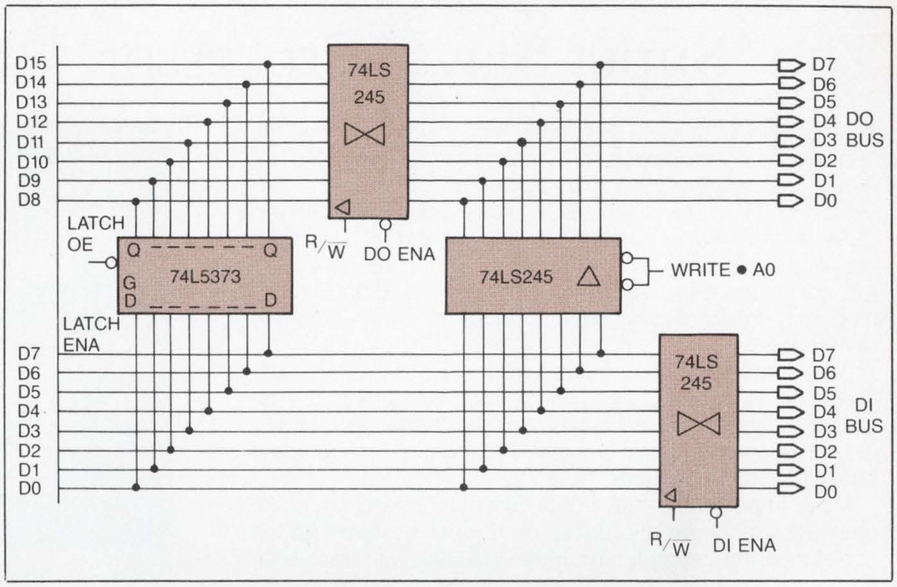


Figure 3: This block diagram illustrates the data bus for the 16032.

Design Considerations For The 16032

The IEEE 696/S–100 Standard for permanent bus masters is well documented for all bus operations and should always be close at hand when trying to design a board for that bus. The 16032 timing was relatively close to bus requirements and what was not there could easily be synthesized from other timing signals coming from the processor. The 16032 has multiplexed address and data lines on the lower 16 address lines so external latches are required to bring the data and address out on seperate bus lines. The Address Latch Enable (ALE) signal is used for latching the address as well as for determining the start of a cycle. The ALE signal and other signals coming from the 16032 are used to match the timing requirements of the bus specifications. Status signals for the bus can be decoded from the four-bit function code coming from the processor—the function code provides an address for a bipolar PROM which provides the status signals for the bus. This makes the status signals reasonably fast coming from the processor. Also, since the function code comes out quite early in the cycle, there is plenty of settling time before the status has to be valid on the bus.

Because the 16032 is a 16-bit processor there must be some external logic associated with reading and writing to memory to allow for 8-bit memory boards. The process involves a state machine to perform a second fetch from memory (or write to memory) while the processor is held in a wait state. This is accomplished with a transparent latch on the lower half of the bidirectional data bus (the Data In bus) which is used to grab the first byte of data and wait for the second operation to get the second byte and then present the two bytes to the processor as a word while releasing the wait state. If the SIXTN* signal comes back from word wide memory, then the wait will be aborted and the processor can run at full speed. This operation happens for each read or write which allows any mix of memory on the bus, assuming it is fast enough to respond to the speed of the processor. The flow chart of the state machine and data bus direction circuitry are illustrated in **Figures 1, 2, and 3.**

The MMU from National Semiconductor will greatly increase the flexibility of the 16032 to allow for multi-user systems with easier context switching between users. It will

The "Super-Slave" Processor

A new concept in multi-user multi-processing systems, the "Super-Slave" processor, provides a dedicated CPU for every user without putting limitations on system size. Designed to fit in any S-100 Bus motherboard, the Super-Slave won't slow a system down like current one-CPU configurations. With its own memory, Z80A processor and I/O ports, the Super-Slave actually shares data with its host only when accessing the drives or other common peripherals.

An unlimited number of users will therefore cause no degredation in system time whatsoever, according to Advanced Micro Digital President Hossein Asadi. In fact, users will even see improvements in response time on some hard disk-based systems, he said.

More importantly, the Super-Slave is priced to make multi-user systems affordable. A 16-user system can be configured, for example, for under $15,000, with each user turning a "dumb" terminal into his own S-100 microcomputer.

Each Super-Slave board includes: a Z80A CPU; four Serial and two Parallel I/O ports; 2K (expandable to 4K) of EPROM; and 64K (expandable to 128K) of Bank-Switched RAM.

Each Super-Slave is linked through the S-100 Bus to a "master" board, like Advanced Micro Digital's own Super-Quad single-board computer.

Together, the boards form a master-slave network that is virtually crashproof, due primarily to the advanced failure detection and recovery capabilities of the Turbo-Dos operating system they utilize.

"We chose Turbo-Dos over CP/M or CP/Net because of its modular architecture," Asadi said. "The software's set of 'building block' modules let us produce—in essence—a family of compatible operating systems."

This "family" of operating systems enhances the dedicated capabilities of each Super-Slave, Asadi said; individual users can perform on single-task, multi-task or networking levels without affecting other users, he claimed.

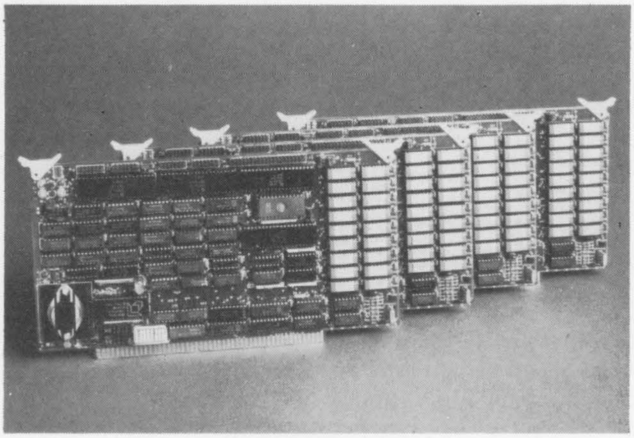


Figure 1: Advanced Microdigital Corp.'s "Super-Slave" processor provides a dedicated CPU for every user without putting limitations on system size.

The boards are available from stock and include full documentation and a one-year warranty on parts and labor. The Super-Slave carries a list price of $650; OEM discounts are available. Super-Slave and Super-Quad boards are available separately or as part of Advanced Microdigital's own Super-System S-100 microcomputer. For more detailed information about any of the products, please call or write:

Hossein Asadi
Advanced Microdigital Corp.
12700 B Knott Ave.
Garden Grove, CA 92641
(714) 891-4004

Write 201

* Turbo-Dos is a trademark of Software 2000, Inc. CP/M and CP/Net are trademarks of Digital Research.

also allow for an easier implementation of operating systems requiring large amounts of memory for each user.

The MMU is to be an option on the CompuPro 16032 CPU. Therefore a requirement of the board is to have jumper provisions to work around not having the MMU, but still make it easy for the systems integrator to add the option at any time in the future. The CompuPro 68000 CPU has the same option. In that device, the problem was solved with two DIP shunts which plug in where the MMU for that board would go. This way the board can be field upgraded with a minimum of down time. This same approach is being done with the 16032 CPU.

The FPU is optional, rather than standard, due to the high initial cost of the part and the fact that many potential users do not need the power that this part adds to the system. The socket on the 16032 board can be filled at any time, and by initializing the 16032, the CPU can be informed that the FPU is present and ready to perform high speed number crunching.

The arbitration between permanent bus masters and temporary bus masters (DMA devices) is also well defined in the standard, and since CompuPro manufactures a number of DMA devices it is very important that the 16032 processor board will flawlessly give up the bus and allow DMA operations on the bus. The HOLD/HOLD-ACKNOWLEDGE handshake of most μPs is fairly straightforward, but the bus must be made to look the same for every type of processor. The control bus must remain in a certain state when the bus is given up by the permanent master and received back by the permanent master. These conditions must be met to avoid glitches on the control bus which may cause spurious writes into memory.

Since throughput is the main goal, the process of handling interrupts and flexibility can make or

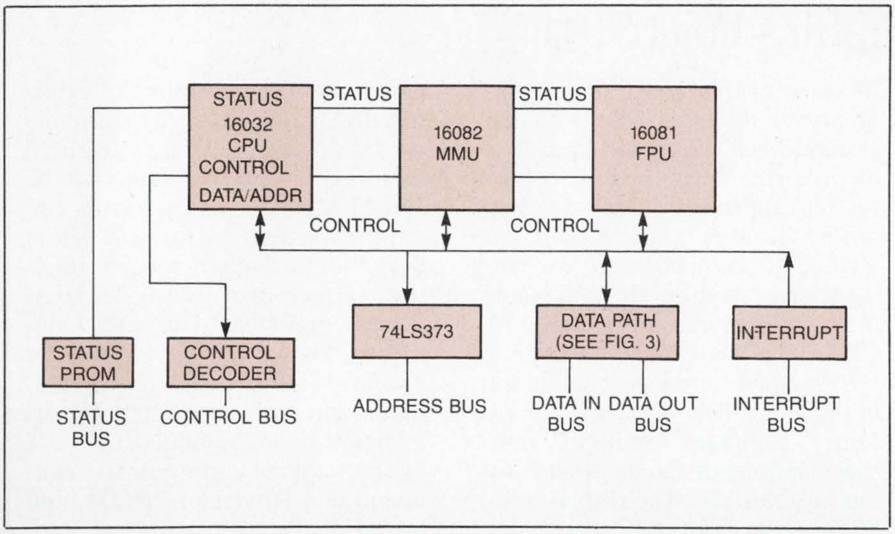


Figure 4: This block diagram shows the 16032 CPU board with its optional parts.

break a multiuser system. With this in mind, the decision to not design in the National Semiconductor Interrupt Control Unit (ICU) was made. CompuPro already has a board which will support the interrupts on the bus with the flexibility needed. In a multiuser environment, this board—The CompuPro System Support 1—would be needed, and adding the ICU would add unnecessary complication. Also, the physical limitations of the board size contributed partially to the decision to leave the ICU off. By making the processor card respond in the specified manner on the bus during an interrupt operation, any interrupt controller conforming to the standard could be used.

The 16032 operates at a maximum clock speed of 10 MHz, and the possibility of faster processors is always there. Due to the fact that the IEEE 696/S–100 bus timing specifies a maximum clock of 6 MHz, there may be some disagreement on how the board meets the standard. But by following the specification so that it meets the standard at 6 MHz, and then just increasing the speed of the board, there should be no major timing problems, assuming the peripherals are fast enough. The set-up and hold times will be shorter, but they will all be proportionally shorter. The CompuPro 16032 CPU can support any speed processor by changing the crystal to correspond to the speed desired. □

Controller Provides Graphics For LSI-11

Small computer users are discovering the power of low cost computers to communicate complex concepts using graphics. One of the most widely installed small computers is DEC's LSI-11. Graphics compatibility for LSI-11 based systems has been made easier with a new add-in intelligent graphics controller, the VDC11-C, from Andromeda Systems. Designed to be transparent to existing LSI-11 software, the VDC11-C emulates industry standard Tektronix 4010 in the graphics mode and DEC's VT52 in the alphanumeric mode. The VDC11-C is also offered as part of a complete graphics terminal, the VDT11-C.

Conventional graphics often uses the storage intensive direct-memory map technique. With memory mapping, each pixel is represented by one host system memory bit. This involves significant CPU overhead to generate a point by point display and results in a slow image write rate, inability to use standard terminal handling software, and often the inability to do much else with the system when a graphic update is in progress. The distributed processing approach chosen by Andromeda, uses a μP within the VDC11-C controller to execute successive high-level commands that are generated by the host CPU. These are input through a DLV11 type serial port emulator in the controller. A typical "Draw Line" command requires only specifications of the end-points by the host LSI-11. The display processor in the VDC11-C then, independently, calculates which pixels in the display memory are to be set to display a straight line between the specified end-points. A 64 Kbyte display memory provides adequate space in the controller for two pages of display memory and a processor scratch pad.

The VDC11-C operation may be seen from the block diagram of **Figure 1**. The Q-bus interface sees two "DLV11" serial interfaces. One drives an RS232 serial port, and is useful for coupling to external RS232 devices such as printers and modems. The second "DLV11" interface appears to the LSI-11 host processor and its operating systems are a true serial port, but is really a special parallel interface driving a 6502-based display processor within the controller. The 6502 was selected for its ease in implementing bit manipulation operations and for its interrupt handling ability.

The control program is contained in 6 Kbytes of PROM, and includes the 6502 control program, alphanumeric character generation and keyboard encoder. Eight Motorola 6665-type 64K dynamic RAMs form the two port display memory. This is partitioned as two 16 Kbyte display pages, 16 Kbyte of scratchpad memory containing the stack and working storage area, and an additional 16 Kbyte available for future enhancements. Note that one port of the RAM connects to the display processor bus, while a second port drives video generator logic.

The video generator creates horizontal and vertical sync, plus video output for a standard "direct drive" B/W video monitor in a 512H by 256V raster scan. To get the desired 256 line vertical scan, the horizontal frequency is increased from a standard 15,750Hz rate to 16,250Hz. This is well within the tolerance of a well designed monitor. Completing the system is an input port to receive data from either a serial or a parallel keyboard.

The performance features of the VDC11-C display controller include the ability to emulate the Tektronix 4010 with a 512H by 256V physical resolution. The 1024H by 768V logical display of the 4010 is automatically remapped to that of the VDC11-C. Experience has shown that this is quite adequate for a large variety of graphic operations.

Several additional features beyond those of the 4010 are pro-

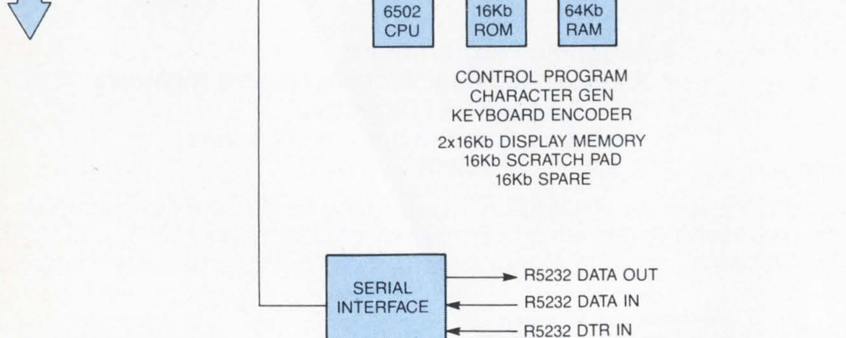


Figure 1: Block diagram of the VDC11-C display controller.

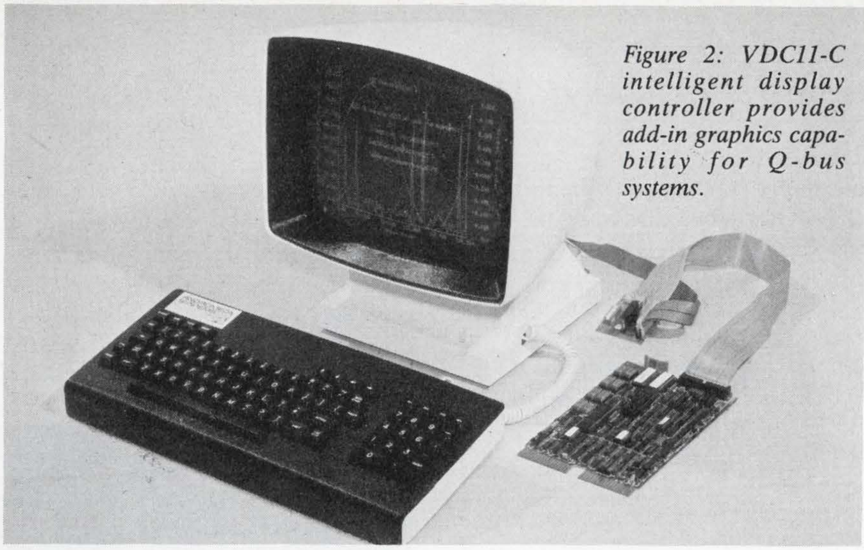


Figure 2: VDC11-C intelligent display controller provides add-in graphics capability for Q-bus systems.

vided: selective erase; two pages of display memory—useful for alternating between an alphanumeric menu and a graphic image; and for animation. The entire display may be read back to the host system, allowing storage and host CPU processing of images. A "strip chart" mode is available where the graphics may be vertically scrolled. Graphic data developed by the host as vectors can be converted to raster format by the VDC11-C and output via an RS232 port for printing on a dot matrix printer/plotter.

Full emulation of virtually any alphanumeric terminal is possible with the VDC11-C by alternating the control ROM contents. The DEC VT52, plus some enhancements, is presently supported. The enhancements include smooth scrolling for easier reading during scrolling, and support of the VT52 special graphics set as standard. A VIEW mode is provided where the control characters are displayed rather than executed—particularly useful for analysis of serial line operations.

The entire VDC11-C is packaged on a standard dual height Q-bus compatible card and draws all power from the Q-bus backplane. The controller is available at $1700 (qty 1) and as part of a complete turnkey graphic display terminal, the VDC11-C, including a 12" video monitor, serial keyboard and all cabling at $2200 (qty 1). OEM pricing is available. Delivery in small quantities.

Andromeda Systems, Inc., 9000 Eton Ave, Canoga Park, CA 91304 **Write 199**

Carbon Coating Protects Thin-Film Media

While offering many theoretical advantages, thin-film plated disk media have proven too fragile to compete seriously with standard particulated media in the magnetic computer storage market. However, new thin-film disks developed at Datapoint Corp. (Sunnyvale, CA) use a carbon coating—applied with a proprietary semiconductor process—in order to achieve the high wear resistance necessary for reliable operation. These thin film disks are used in the model 9301, which stores 20 Mbytes on four 5¼″ disks.

While this sort of capacity could have been achieved with ordinary particulated media, engineers at Datapoint felt that it was important to begin developing thin-film disks. The theoretical values associated with thin-film media made it clear that the use of such disks would open room for considerable technological enhancements.

Coercivity strongly influences the output and resolution of recording media, and while the practical limit for particulated media is about 600 oersted, the limit for thin-film media is about 1,000 oersted. Output is directly proportional to the media's remanence, and the remanence of plated material is close to its theoretical limit of 15,000 gauss. But the limit for particulated media is about 3,000 gauss, and is hard to reach because of the binder material used to hold the particles together.

When development began on the 9301, none of the commercially available thin-film disks met all the requirements of wear and magnetic properties. However, the possibility of thin-film media with a protective carbon overcoat had been explored in previous research at the Peripheral Products Division, and the 9301 was developed on that basis during the next six months.

The Disk

The disk itself is made of nickel-phosphorous-plated aluminum, with coercivity averaging 625 oersted provided by a cobalt-nickel layer 15–.30 μm thick. A carbon film .1 to .15 μm thick is ap-

DISK TYPE	WEAR MARK APPEARED AFTER
Carbon coated	2 hours
Hard Cobalt-oxide	1.5 hours
Soft Cobalt-oxide	20 seconds
Rhodium coated	1.5 minutes
3350-type oxide	about 20 seconds

Note: hard cobalt-oxide coatings cannot be used since the high temperature application process causes permanent magnetization of the disk.

Figure 1: Carbon coating raises thin- film disk longevity considerably.

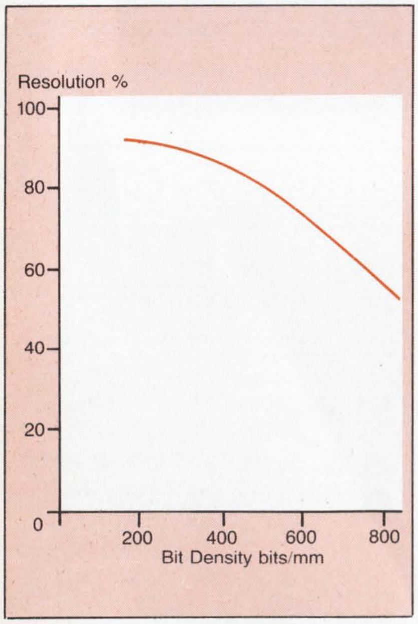
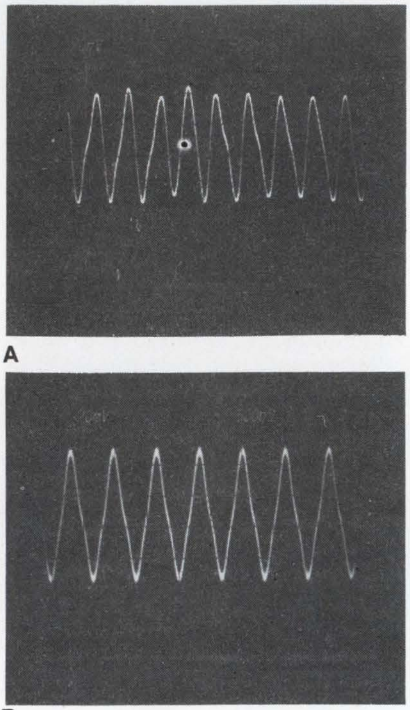


Figure 2: A typical resolution curve showing resolution against bit density. The measurement was made using a head with a gap length of 1.016 μm. The head-to-disk spacing was about 0.2 μm. The curve shows more recording bit density growth potential on this disk than on any commercially available particulated disks.



A

B

Figure 3: A and B show the modified frequency modulation pulse shape of a hexadecimal AAAA and FFFF bit patterns, respectively. They show no bit crowding tendency. The amplitude resolution is in the 80–85 percent range.

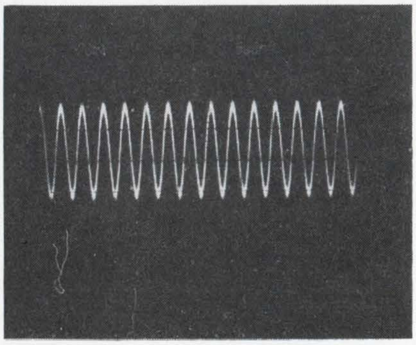


Figure 4: The read-back signal from a "worst case" hexadecimal B6D9 bit pattern. No peak shift problem is visible.

plied to the top of the magnetic layer.

Comparative tests for wear resistance were carried out with a .25 mm ferrite head held in contact with a spinning disk at a 45° angle by a 5-gram load. Each test went on until a visible wear mark was detected. The results were quite favorable. **(Figure 1).** It was also noted that the head did not penetrate the carbon coating even after 200 hours of continuous wear.

Recording Characteristics

Thin film disks are more sensitive to media noise than standard particulate disks, since they have to use a narrower track width. Narrower tracks are necessary because of the greater effect of head fringing on thin-film disks—the area of magnetization covers a larger area. Considerable attention was spent on plating techniques and chemical compositions to assure low noise levels. The result was a media noise level of −32db, filtered at 6 MHz.

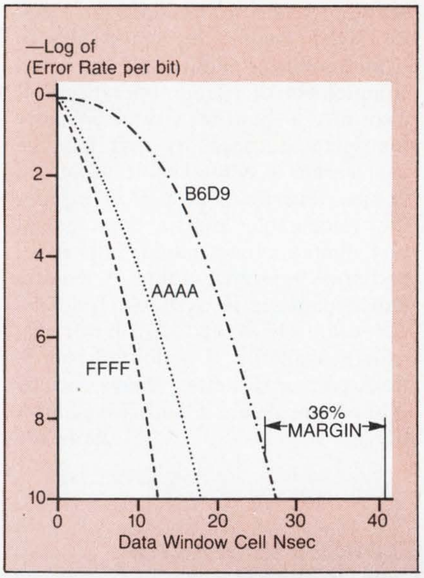


Figure 5: A typical MVFO (Marginal Variable Frequency Oscillator) plot of MFM recording at 473 bits/mm. Using the B6D9 "worst case" bit pattern, the disk used only 64% of the window cell to achieve an error rate of one in one billion. At 315 bits/mm, it used 55%.

The new thin-film disk has been successfully used in the Datapoint 9301 disk system, which records at 325 bits/mm and 19.7 tracks/mm. It is plain that the magnetic properties of the 9301 are not being fully utilized, that the bit density could be much higher. Also, these magnetic properties could be further enhanced through proper control of the parameters involved in the disk manufacturing process.

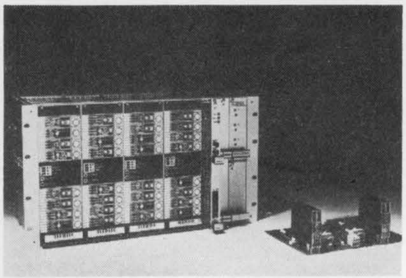
But most importantly, the carbon overcoat has proven successful in strengthening thin-film media, opening it up as a new field for enhancing the technology of magnetic storage.

Contact: Francis King, Datapoint Corp, Sunnyvale, CA **Write 197**

PROCESS CONTROL INTERFACE

Designed To Meet Eurocard Specifications

$M^2\pi$ operates on a stand alone basis, requiring no I/O software drivers. The interface is seen by the CPU as a memory mapped block of internal RAM, allowing the computer to access the real-time data base through read/write operations. Since the tech-



nique eliminates CPU I/O overhead, the interleaving of multiple tasks is simplified by a very low level of interrupt activity. In the event of CPU failure, the system will either maintain control outputs at the last valid setting or reset them to user selected fail-safe levels. A single $M^2\pi$ universal I/O card accommodates all types and mixes of input and output modules, such as analog signals and contact closures, up to a maximum of eight. Each module is labeled with all primary point data, including name, number, and wire number. Functions are shown graphically at the front of each module, and LEDs indicate point activity and in- and out-of-service status. **Monitek, Inc.,** Digital Systems Division, 1495 Zephyr Avenue, Hayward, California 94544. **Write 160**

CROSS ASSEMBLER

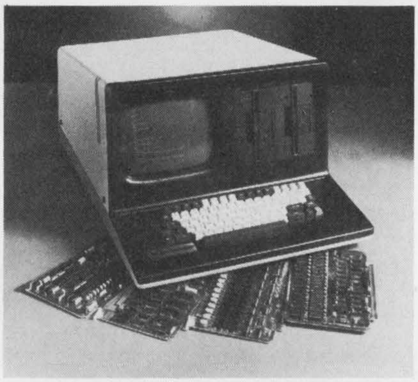
Permits M68000 Software Development On VAX And PDP-11 Systems

A cross assembler lets users develop Motorola 68000 assembly language source code on VAX-family systems running VMS or UNIX, or on PDP-11-based systems running UNIX or RSX-11M. The package bundles a relocatable assembler, linker, object module librarian, and cross reference utility in one standard integrated package. The assembler is fully compatible with Motorola's 68000 resident assembler, and offers conditional assembly, macro processing, an "INCLUDE" facility, command files to handle multiple input files, and a full complement of pseudo-operations. It also has a built-in virtual memory management capability that lets the user create a symbol table unlimited in size. The price of $3,000 includes the relocatable macro cross-assembler, linker, object module librarian, and cross reference utility. A maintenance package is available for $300 per year. OEM and distributor discounts available. Distribution on 9-track tape or diskettes. **Oasys, Inc.,** 60 Aberdeen Ave., Cambridge, MA 02138. **Write 168**

EXORSET 35 DESKTOP CONTROLLER

Includes User Interface, Floppy Disk Storage

Three versions are available that provide optional amounts of mass storage: the 351-0 with no floppy disk drives; the 351-1 with one double-sided mini-floppy disk drive for 164 Kbytes of storage, and the 351-2 with two disk drives for 328 Kbytes of stor-



age. All three versions include 2K bytes of dynamic RAM for CRT character refresh, 56K bytes of dynamic RAM and three strappable sockets that can be configured for 1K, 2K, 4K, or 8K ROMs or EPROMs. A fourth socket, normally containing the 4K EXORbug firmware, can be configured for a user-designed monitor routine. The EXORset 35 memory map is defined by PROMs, allowing the user to easily reconfigure the architecture of the system. Price (in quantities of 20) for the 0, 1, 2, models are $3,305, $4,070, $4,675 ea., respectively. **Motorola,** P.O. Box 20912, Phoenix, AZ 85036. **Write 165**

OEM PACKAGES FOR 68000

Comparable Utilities, Source-Level Debugger

Two new compilers produce code that can be linked and executed on the MC68000. One package resides on the VERSAdos operating system, the other on the RSX operating system of the Digital PDP-11 series. Both have comparable utilities, including a source-level debugger. The compilers are versions of Oregon Software's Pascal-2, and support all capabilities of standard Pascal, conforming closely to the draft proposed Pascal standard (International Standards Organization dp7185.1). Both OEM products offer an option that allows concurrent programming in Pascal, including true priority scheduling and the ability to write device drivers in Pascal. The concurrent package allows user programs to run without an operating system. **Oregon Software,** 2340 SW Canyon Road, Portland, Oregon 97201. **Write 164**

10-MBYTE μC SYSTEM

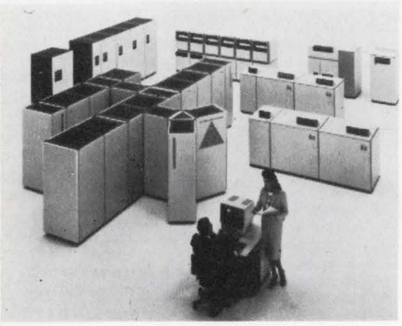
A complete, newly-designed 10-Mbyte microcomputer system for only $5995 is the centerpiece of a complete range of highly competitive new products. The new system includes: 10-Mbyte hard disk; one 5-¼" single sided, dual-density floppy disk back-up; 8-bit μP; disk controller; 10-slot S-100 motherboard; 28-amp power supply; 12" video monitor; standard intelligent 62-key ASCII keyboard; 132-column dot-matrix printer; CP/M operating system; 64K RAM. Options include 5- or 18-Mbyte hard disk; 16-bit μP; 256K RAM; intelligent 86-key ASCII ex-

tended keyboard; single or double dual-density 8" floppy disk drives. **Fischer-Freitas Corp.,** IMSAI Division, 910 81st Avenue, Oakland, CA 94621. **Write 169**

ARRAY PROCESSOR SYSTEM

Supercomputers Capable Of 630/ 315 MFLOPS

Two models are available: the S-810/ 20 can execute 630 MFLOPS and has a maximum of 32 channels rated at 96 Mbytes/s. Its main storage has a maximum capacity of 256 MB. Monthly rentals start at approximate-

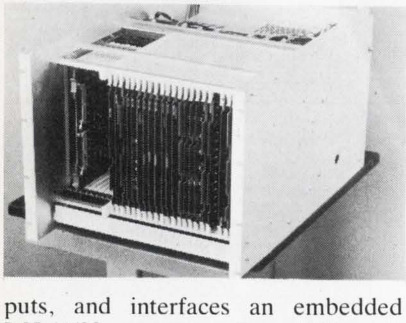


ly $280,000. The S-810/10 model is rated at 315 MFLOPS. It has a maximum of 32 channels (96 MB/sec.) and a maximum main storage capacity of 128 MB. The S-810 system adopts a control program based on Hitachi's operating system (VOS3: Virtual Operating System 3). The system is able to provide various VOS3 functions such as TSS and resource management, and to use peripheral and terminal equipment for the M-series machines. It is also possible to realize a multi-processor system by connecting an S-810 processor with an M-series processor. **Hitachi,** Computer Sales and Service Division, 950 Elm Ave., San Bruno, CA 94066. **Write 163**

MULTISPECTRAL/ MULTITEMPORAL IMAGE PROCESSOR

Integrates Consoles/Work Stations

The Model 75 accepts image data in digitized form from host computers as well as RS-170 compatible video in-



puts, and interfaces an embedded LSI-11/23 computer. In addition, it features an extensive range of remote host CPUs. The use of 64K dynamic RAMs makes available up to 16 channels of 512 × 512 × 8-bit refresh memory on only eight boards. Other features include simplified image analysis (split screen and roam function), improved, high-efficiency region-of-interest generation and analysis (using graphic bit planes to select different transforms preloaded in the look-up table), and continuous-frame digitization and feedback capabilities for accelerated recursive processing functions. **International Imaging Systems,** 1500 Buckeye Drive, Milpitas, CA 95035. **Write 167**

MULTIPROCESSOR MINIS

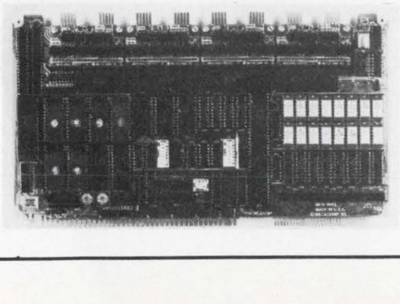
Compatible Superset Of DG NOVA

Using microprogrammed firmware, bit-slice 16-bit technology and the powerful PCOS operating system, the PolyComputer provides user transparent multiprocessing and virtual memory operations in multiple batch, timesharing and real time modes. The complete system, including the PCOS multiprocessing virtual memory operating system and one compiler (choice of BASIC, COBOL, FORTRAN, or Pascal), utilities, and debugging facility is only $36,950, end user quantity one. A nine processor Model 903A with 2,112KB of MOS memory, 158MB high performance Winchester disk, ½ inch magnetic tape drive, 16 communication channels, plus enclosure is $65,850. A fully expanded system with 17 CPU's and over 4MB of MOS memory fits within one system cabinet and is priced at less than $100,000 end user quantity one. **PolyComputers,** 18003-L Skypark South, Irvine, CA 92714. **Write 161**

COMMUNICATIONS CONTROLLER

Supports Eight Channels

The MCS-1062 is an intelligent Multibus compatible serial I/O controller that features eight serial channels, programmable for asynchronous, synchronous or bit-oriented protocols, a



unique packaging concept that allows field interchangeable "plug in" modules to support a variety of electrical interfaces, and dual port RAM of up to 64 Kbytes for parameter passing, buffers and semaphore signaling between a master processor board and the on-board slave processor. Bus operations are supported for 8 or 16 bit systems with 20 bit addressing.

The MCS-1062 is suited for serial communications applications requiring many low or medium speed channels, particularly those in which the master CPU cannot be burdened with character-by-character servicing of multiple serial I/O devices. The controller resources can provide the distributed intelligence necessary for implementing data link protocols and line disciplines of many types. Price: $1,570 for 50 pcs. with RS-232 modules. **Metacomp, Inc.,** 7290 Engineer Rd., Suite F, San Diego, CA 92111. **Write 170**

68000-BASED SYSTEM

For Multiuse Environments

The ACS68000 system, based on an 8 MHz 68000 CPU, offers 8 to 16-user capability with 40 MB of 8" Winchester hard disk storage and ½ MB floppy backup. Options include an additional hard disk of up to 80 MB and mag tape cartridge drive for backup. Local area networking to other Altos 16-bit machines is accomplished with Altos-Net using twisted pairs (RS-422). Similarly, it may be operated with the company's implementation of Ethernet using the same networking software. With 512K to 1MB of

RAM, the system will offer a proprietary demand paged virtual memory (to be introduced in the first quarter of 1983). The ACS68000-14 with 40 MB Winchester hard disk storage is $14,500; the 80 MB system, available in the first quarter of 1983, will be $16,500. **Altos Computer Systems,** 2360 Bering Drive, San Jose, CA 95131. **Write 166**

240 MBYTE DISK

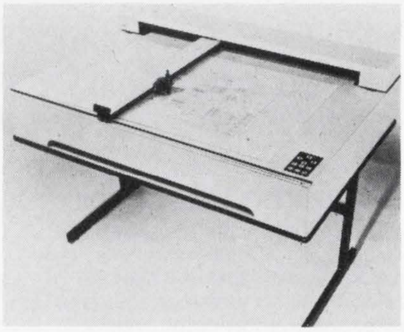
Offers Removable Disk Convenience

The removable disk drive, Qualex Model 3321, is available with Qualex's four proprietary cache options and shares the same controller as the Qualex Group 3000 600 Mbyte fixed Winchester drive introduced earlier this year. Model 3321 is priced at $26,500 in single unit quantities for a master drive and $21,450 for Model 3301, a slave unit. Dual I/O ports are optional on the Qualex Model 3321 disk drives. Mean time between failures (MTBF) has been rated from between 4,000 to 6,600 hours with from four to six pack swaps per day. Up to 16 of the drives can be daisy-chained together if required. **Qualex Technology, Inc.,** 31220 LaBaya Dr., Suite 110, Westlake Village, CA 91362. **Write 158**

FLATBED PEN PLOTTER

D-Size, Interfaces To Any Computer

Called the Model 3200, the new plotter has a plotting area of 25″ × 37″, and has plot subroutines built-in as part of the controller. This eliminates the need for special host software and reduces memory requirements in the host. As a result, Model 3200 plotters are compatible with any programming language and any operating system at any revision level. Model 3200 plotters also feature 2496 bytes of user-programmable RAM. Repetitive graphic element symbols, such as grids, logos and design symbols can be downloaded, to further free up the host computer. The Model 3200 plotter is furnished with an RS-232-C/CCITT V.24 asynchronous serial ASCII interface. A GPIB (IEEE-488) interface is optional. Dimensions for the plotter (not including table) are: 12″ H × 52″ W × 36″ D. Single unit price is $11,500. **Data Design Logic Systems, Inc.,** 4800 Patrick Henry Drive, Santa Clara, CA 95054. **Write 157**



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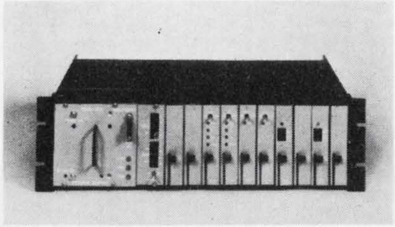
T1 RATE DIGITAL MULTIPLEXER

Interfaces With T Carrier Transmission Systems

The T1 Rate Digital Multiplexer, TDM-150, with a drop and insert and terminal capability, provides a simple, cost-effective way to interface with T carrier transmission systems. Voice

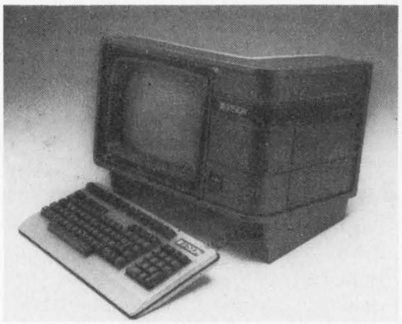


frequency telephony, data circuits and high quality audio program channels can be inserted or dropped from existing digital transmission facilities, or channels can be originated and terminated. With the TDM-150, any channel card can be placed in any channel location within the TDM-150 shelf since locations are not dedicated, and cards may be figured to access any channel number in either direction of the T1 line. The TDM-150 is compatible with D1D, D2, D3 and D4 channel banks. Existing T1 system maintenance and alarm signal formats are preserved. Pricing starts at $1,650 for a receive only terminal to $2,290 for a drop and/or insert two-way configuration. Either AC or DC power supply is included in the basic pricing. Individual channels range in price from several hundred dollars for low speed data and voice to $975 for a 15kHz program channel transmitter. **Tau-Tron, Inc.,** 27 Industrial Ave., Chelmsford, MA 01824. **Write 151**

FREEDOM ARCHITECTURE CRTs

Customizable, Multiprocessor Architecture

These terminals, called Vision, make extensive use of Freedom, a customizable, multi-processor architecture that allows changes in protocols, data handling and CRT functions to be programmed in high-level language without costly re-engineering. All Vision terminals are equipped with the Freedom architecture, making them ideal for communication networks with multi-protocol requirements. Standard features for the Vision Series include a 15″ or 12″ video screen

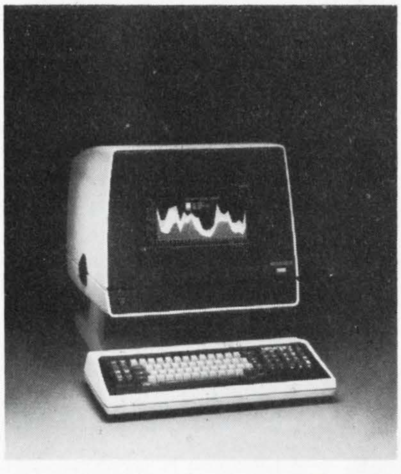


in either amber, green or black on white; 24 line × 80 or 132-column display with 25th status line; up to four pages of screen memory; electronic screen tilt and programmable brightness control; and enchanced character formation using a unique "dot stretch" and "dot delay" technique for up to 512 different character symbols. **Northern Technologies,** 85 Torbay Rd, Markham, Ont, L3R 1H1. **Write 144**

COLOR DISPLAY STATION

IBM Compatible

Functionally interchangeable with the IBM 3279, the 2079 accommodates up to seven colors, alphanumeric data and business graphics. Compatible in IBM SNA/SDLC or bisynchronous environments, the 2079 allows operators to enter alphanumeric data and special APL and Text characters and to retrieve that data in alphanumeric and graphic form from the IBM System 360, 370, 303X, 3081, 43XX, 8100 and Amdahl processors. The three standard models of the 2079 all include keyboard numeric lock, audible alarm and unprotected field indicator. Prices begin at $4,395 for a standard 4-color display. **Memorex,** San Tomas at Central Expressway, Santa Clara, CA 95052. **Write 146**



New Products • PERIPHERALS

LOGIC ANALYZER TRACE MODULE

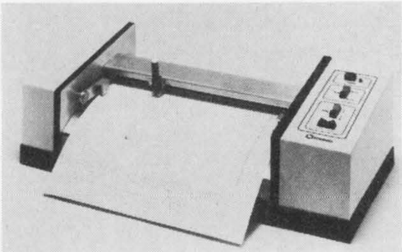
Permits Full Disassembly of 16-Bit 68000 μPs

TM 68000 trace modules incorporate a hardware emulation of the 68000, allowing them to disassemble the hard-to-understand digital operations back into operands and instructions that can be displayed on the logic analyzer's screen. These instructions are in the mnemonic language that the designer understands. This hardware emulation is complemented by a full disassembly software package residing in ROM chips that are plugged into sockets provided in Dolch's LAM 4850A, 48-channel logic analyzer. In addition, the company provides a simple interface to the 68000 product under development. This is a dedicated, high impedance buffer probe that clips over the μP chip and can drive a cable as long as 10 feet. The TM 68000 sells for $3500, including full disassembly software; delivery is 90 days. **Dolch Logic Instruments,** 230 Devcon Dr, San Jose, CA 95112. **Write 147**

LOW-PRICED PLOTTER

Grit-Roller Paper Transport

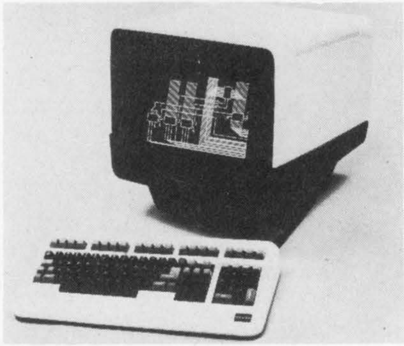
This plotter's low-inertia grit-roller paper transport produces a superior line quality, eliminates slip, provides excellent repeatability, and, because only the paper moves for the X axis, overcomes problems caused by inertia in earlier plotter designs. This low-inertia system has mechanical resonant frequencies higher than plotting velocities which minimizes pen vibrations for a uniform smooth line. A unique feature is the resident program for plotting smooth non-polygonal arcs with which motor speeds for both X and Y axes are simultaneously controlled while the arcs are plotted, producing smoothly uniform lines at virtually slew rates. The programmable step size is 0.005″, and the transport step size, 0.0025″. Plotting areas range from 8½″ × 11″ to 11″ × 36″. Firmware for vectors, arcs, line types, markers, 96 ASCII characters, character and marker scaling from .08″ to 2″, full 360° character and marker rotation in 1° increments is standard. Up to 3,800 ASCII command characters can be stored, or this same buffer capacity can be used to store special down-loaded customer defined fonts. Single-quantity price is $1295. **Numonics Corp.,** 418 Pierce St., Lansdale, PA 19446. **Write 145**



GRAPHICS DISPLAY TERMINAL

Displays Up To 16 Colors

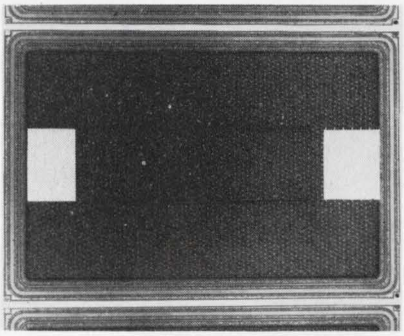
The Autograph Color X5A, a 512 × 512 × 4 resolution, full bit map, color display terminal enables the user to choose from a palette of 511 colors—on a 14 inch, non-interlaced tube. The non-interlaced display totally eliminates any flickering that would cause user eyestrain. The Color X5A is fully compatible with software systems supporting Tektronix 4010, 4014 and 4027 terminals. The terminal scales the Tektronix 1024 × 780 viewing image to a 512 × 390 view with an exact 1:2 scaling ratio. The Color X5A features on-board intelligence for drawing circles, arcs, ellipses, and for filling in blank areas. Other graphics functions include integer zoom, precision pan, bidirectional scrolling, and multiple character sizes. Suggested end user price: under $5,000. **Data-Type, Inc.,** 2615 Miller Avenue, Mountain View, CA 94040. **Write 155**



SCRs GO MOS

Eliminates Need For Interface Device

A Silicon Controlled Rectifier series using MOS technology offers the advantages of the high input impedance and fast turn-on time of a power MOSFET and the regenerative, latching action of a thyristor. These 200 nsec turn-on SCRs drive directly from logic without the need for an interface device. The MOS SCR was developed from the vertically structured TMOS transistors by changing the substrate doping from N+ material to P+. In this manner a four-layer structure evolved (PNPN) creating the two transistor equivalent which has the latch feature of SCR's and the gate drive and switching characteristic of MOS transistors. The MCR1000 MOS SCR series in the TO-220 pack-



age has a 15 amp current rating and is designed primarily for very high speed switching, high current pulse applications—laser modulators, printers, fluorescent lighting and switching power supplies. Prices range from \$5.20 to \$6.90 (qty. 100). **Motorola Semiconductor Products,** P.O. Box 20912, Phoenix, AZ 85036. **Write 143**

LOW-COST PARALLEL MULTIPLIER

For μC-based Systems

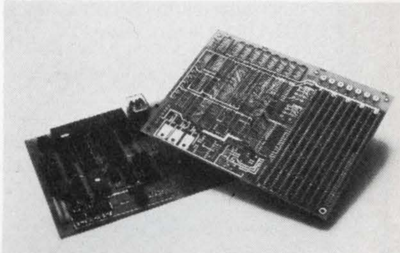
This 16×16 NMOS parallel array multiplier costs less than half as much as existing products of comparable functionality. The WTL2516 and WTL2517 Parallel Multipliers also consume less than one-fourth the power of available bipolar multipliers. To achieve their cost/performance advantage, the devices use a modified Booth's algorithm and advanced NMOS VLSI design processes. They feature input/output latches that can be operated in either clocked or transparent mode. Input data are accepted in the form of 16-bit two's

complement or unsigned magnitude. Mixed data format operation is also acceptable. The devices operate on a +5-volt power supply and have TTL-compatible input/output levels. Price is \$65, in quantities of 100. **Weitek,** 3255 Scott Blvd., Bldg. 2B, Santa Clara, CA 95054. **Write 142**

DEVELOPMENT PCB

Suited For Intelligent Industrial Controller Applications

The TMC-35 is a user configurable development printed circuit board especially suited for intelligent industrial controller applications. The resident MPU is Intel's popular 8035/8048 single chip μP. The TMC-35 lends itself particularly to prototyping, new product development or short run produc-

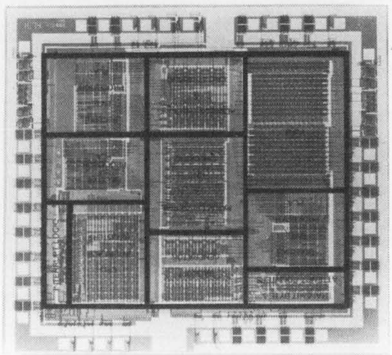


tion of ROM based microcontrollers. Price for the board only is \$67; board with CPU, latch, EPROM socket, other support hardware assembled and tested is \$127. **Treline,** 17891 Sky Park Circle, Suite K, Irvine, CA 92714. **Write 141**

MONOLITHIC ETHERNET DATA LINK CONTROLLER

Focused On Dedicated Station Controllers

This controller chip, developed with the help of a silicon compiler, is the first device in the industry to have silicon structures generated by a logical function description. The model 8001 EDLC also reflects careful planning



with a key systems builder to ensure that the most useful and streamlined chip for Ethernet local area networks (LANs) was developed. The 8001 provides all the functionality needed to transmit and receive data within an Ethernet network. These functions include collision detection, error checking, cyclic redundancy code (CRC) generation and checking, automatic calculation of the interval between retransmitting, and address matching. Thus the CPU can view the 8001 as merely another parallel port. Samples of the 8001 EDLC are now available, with production quantities in January. In quantities of 100, the 8001 will sell for $135 each. **SEEQ Technology, Inc.,** 1849 Fortune Dr., San Jose, CA 95131. **Write 129**

512 KBYTE RAM

Packaged On Single 5½" × 9" Card

This very high-density dynamic RAM card enhances all Chieftain computers. Just two of the cards allow the system to operate with its full 1 Mbyte addressing range. After the operating system and BASIC are loaded into the system, there is still 950K available for user programs. The RAM card, designated the M-512-X, is designed to operate with the 16 bit, 6809 processor from Motorola. Through a proprietary refresh circuit, the board allows the high speed version of the 6809 (68B09) to operate at full-rated speed without stretching or slowing of the processor clock. This is the company's first use of dynamic RAM in its products and the M-512-X uses the type 4164 64K chips. The M-512-X has a flexible array of switching options permitting the system designer the option of enabling or disabling certain areas of each page. This allows graphics boards or other devices which use memory space to co-exist in a multi-user environment with the same area normally occupied by the M-512-X when fully enabled. The board is also available in 128K and 256K versions. Prices: M-512-X $1,895, M-256-X $1,295, M-128X $995; delivery is stock to 30 days. **Smoke Signal Broadcasting,** 31336 Via Colinas, Westlake Village, CA 91362 **Write 130**

DC/DC CONVERTERS FOR 48 VDC INPUT

Aimed At Telecommunications Applications

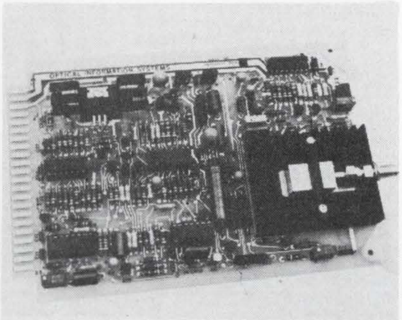
Designed for inputs of 48 VDC, this line of DC/DC converters provides total power output from five to six watts. They offer excellent regulation, voltage isolation, input filtering, internal shielding, and other features particularly well suited to telecommunications requirements. All five models feature input/output isolation up to 500VDC; Pi-type input filters; current limited short circuit protection; and six-sided continuous copper shielding to minimize EMI/RFI. The units offer line regulation within .02%, and load regulation within .04% for single output models and .02% for dual output models. Ripple and noise is 50mV P-P (max.) for single output models and 35mV P-P (max.) for dual output models. Prices range from $68.60 for single output

models to $72.10 for dual output models in quantities of 100; delivery time is stock to eight weeks, depending on quantity. **Power Products,** Div. of Computer Products, Inc, 2801 Gateway Dr, Pompano Beach, FL 33060. **Write 136**

ECL COMPATIBLE FIBER-OPTIC TRANSMITTER

Operates At Up To 300 Mb/S (NRZ)

The OT8100 Series Fiber Optic Transmitter is an ECL-compatible unit incorporating an OIS semiconductor laser as the optical source. The transmitter provides a clean optical pulse with rise and fall times of less than

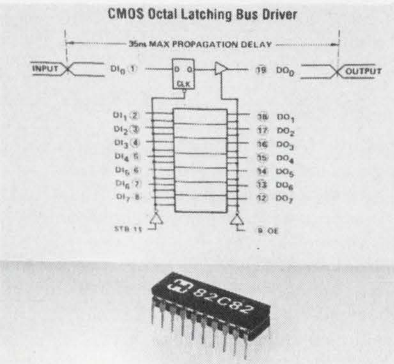


1.4ns, allowing use over a wide range from DC up to 300 Mb/s (NRZ). The operating temperature range is O° to +55°C. The module operates from a single −5.2V power supply appropriate for ECL logic designs. Programmed diagnostic circuitry is incorporated with on-card visual indicators and remote-sensing outputs to signal transmitter status. The price is $2000 each for quantities of 1–4; delivery is stock to 5 weeks ARO. **Optical Information Systems Inc.,** 350 Executive Blvd, Elmsford, NY 10523. **Write 135**

CMOS 80C86

Replaces Intel Bipolar Part

This device, the 82C82 CMOS octal lathing bus driver, is a pin-for-pin and TTL-compatible replacement for the Intel bipolar part. The 82C82 is designed using Harris' advanced scaled SAJI IV CMOS process and features a power dissipation of 55 μW, a factor of 10,000 reduction from the bipolar level of 880 mW. The Harris CMOS latch also has gated inputs which disable device inputs while data is

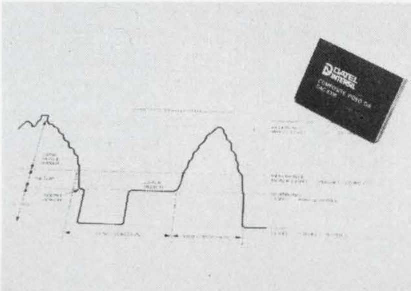


latched, resulting in a further reduction in operating power dissipation. 82C82 timing specifications equal those of the similar grade bipolar device, with a propagation delay of 35 ns guaranteed over the specified operating temperature and voltage ranges and with a 300 pf load. ID82C82, industrial temperature version, $7.41 each (qty. 100); MD82C82, military temperature grade, $22.24 (qty. 100). **Harris Corp.,** Semiconductor Group, P.O. Box 883, Melbourne, FL 32901. **Write 128**

8 BIT D/A CONVERTER

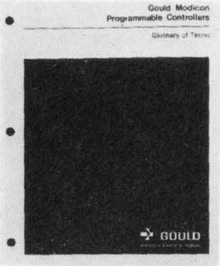
Features Ultra-Fast Composite Video Output

The DAC-8308 and DAC-8318 are ultra fast, high performance D/A converters specifically designed for video and graphic display applications. The DAC-8308 accepts 8 bits at throughput rates up to 40 MHz, producing a

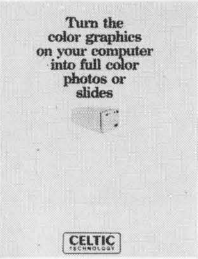


composite video output signal with 256 gray levels. Adjustable setup, composite sync, composite blanking and peak white signals are derived from separate digital inputs. The converter features a more precise setup adjustment, and a peak white level not available on competing devices. The setup produces an apparent shift in the "brightness" of reference black. The peak white level is a "whiter than white" level not within the normal range of the picture. Ten percent brighter than reference white (110 IRE units), this level is sometimes used for generating cursors or outlines. All digital inputs are TTL compatible. The DAC-8318 is the same converter without the composite video digital inputs. The DAC-8318 includes set and reset inputs that produce zero or full scale outputs respectively when activated. Price for the DAC-8308 is $120 (qty. 1–9); the DAC-8318 is $115. Availability is stock to 8 weeks. **Datel-Intersil,** 11 Cabot Blvd., Mansfield, MA 02048. **Write 126**

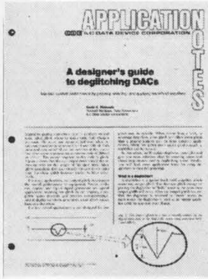
New Literature



Glossary Of Electronic Terms. The 7-pp. brochure explains terminology used most frequently to describe programmable controllers and related systems. Terms such as "bit rotate function," "dump," "register," and "transitional contact," are covered in the glossary.
Gould Modicon **Write 264**



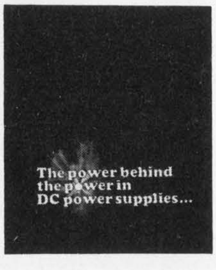
Computer Peripheral Fact Sheet. Describes current principal products such as the VFR-2000, an easy to use, low-cost video film recorder that produces 35mm slides; the VFR-2000I, a similar system offering instant prints; and the VFR-6000, a video film recorder that produces 8×10 transparencies, 35mm slides and instant prints.
Celtic Technology **Write 260**



Deglitching DAC's. A 4-pp. application note explains the causes of glitch in digital-to-analog converters (DAC's), and suggests solutions. Entitled "A Designer's Guide to Deglitching DAC's," it includes guidelines for the selection of a deglitcher and also has application hints for layout, noise reduction and use of latches.
ILC Data Device **Write 262**

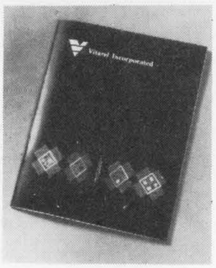
Fiber Optics. A 4-pp. application note describes the use of fiber optic communications in high resolution color computer graphics systems. Artel's "Application Note CG-1" details ways of configuring the SL-2000 Fiber Optic Transmission System to achieve long distance remoting of Red-Green-Blue (RGB) color computer graphics workstations in CAD/CAM, process control, military C^3 and other graphics applications.
Artel **Write 268**

Increase User Productivity. An 8-pp. brochure describes the options for Atlantic Research Corp's new low-cost INTERVIEW 29A/30A/40A series Data Communications Analyzers. The options described in this brochure extend the usefulness and capabilities of the series, thus helping to increase the productivity of those who use them. The brochure also describes upgrade kits, special codes, and other accessories for the new series.
Atlantic Research Corp. **Write 252**



Linear Power Supplies. Fact Sheet describes Powertec, a designer, manufacturer and marketer of linear power supplies. Includes information on ValuSwitcher, SuperSwitcher, MultiMod, Sub-Modular, and OEM II.
Powertec **Write 261**

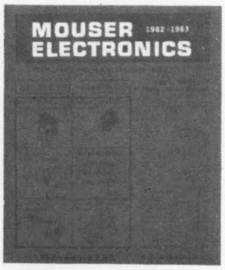
EPABX Brochure. This 6-pp., four-color brochure contains general features, station related features, attendant related features and technical data on Siemens' SD-192MX EPABX. SD-192MX provides the small-to-medium sized businesses with advanced time and cost saving features like least cost routing, speed calling and more.
Siemens **Write 263**



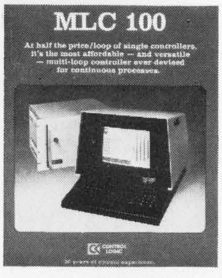
Microelectronic Packages. A 12-pp., four-color brochure describes Viterel's high-density, high-reliability microelectronic devices and production capabilities. Photos and diagrams illustrate Vita Pak, a device in which proven LSI chips are connected in back-to-back cavities. The brochure also describes the company's microcircuit research, development and assembly capabilities.
Vitarel Inc. **Write 250**

Data Logging Brochure. A new battery-operated HP-IL/HP-IB data-acquisition and control unit from Hewlett-Packard is described in this four-color, 22-pp. brochure. Standard in the Hewlett-Packard Model 3421A mainframe is a scanner, HP-IL (Hewlett-Packard Interface Loop), an A/D converter and a frequency counter and display.
Hewlett Packard **Write 257**

Disk Heads Data Sheets. New high density "Tri-Pliant" design floppy-disk heads are described in two data sheets. Each data sheet describes Applied Magnetics' exclusive "Tri-Pliant" suspension design, typical performance specifications and mechanical dimensions. Includes information on disk heads used in 5¼″ and 8″ double-sided floppy disk drives.
Applied Magnetics **Write 251**



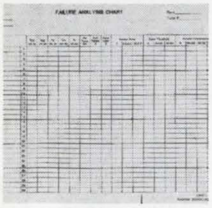
Electronic Components. The 140-pp. 1982-83 edition of the Mouser Electronics Catalog offers information on over 12,000 items stocked. Provides quick access to up-to-date product data and pricing of standard stocked industrial electronic components.
Mouser Electronics **Write 255**



Multi Loop Controller. Specifications, diagrams, and how-to-use information are provided in a 4-pp. product brochure. The brochure describes how tighter control can be achieved with a digital controller at a significantly reduced cost. It highlights how quickly MLC 100™ can be installed and how to use it with the "no programming" feature.
Control Logic **Write 253**

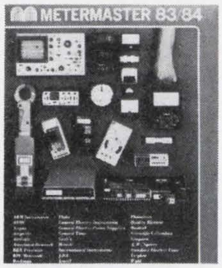
New Literature

CRT Power Supply. A 4-pp. brochure describing Precision High Voltage CRT Power Supplies, includes both single and multi-output high voltage power supplies for use in high performance CRT display systems. Also described is a CRT test set, complete specifications for five multi-output power supplies, single output modules, and lab instruments with capabilities suitable for providing anode, focus, G2 and G1 voltages.
Bertran **Write 254**



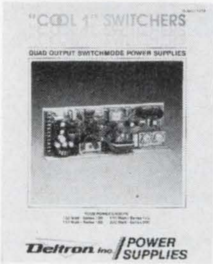
Failure Analysis Chart. A Failure Analysis Chart for digital integrated circuits simplifies the task of qualitative and/or quantitative data logging. The charting system may be used as an aid in statistical analysis or as supportive documentation when returning defective parts to manufacturers.
American ElectroData **Write 256**

Application Brochure. Three case histories in which statistical multiplexing has improved transmission efficiency, network manageability and overall network costs are the focus of Codex's "6000 Series Application Brochure." This brochure documents how Rockwell, Ford, and California's Riverside County met their application needs with the 6000 Series.
Codex **Write 265**



Metermaster Catalog. The Metermaster 1983 catalog, with more than 400 pages of panel meters and general purpose test and measurement equipment, has complete specs on thousands of instruments from 40 leading manufacturers. Can be used as a single reference book for both buyers and engineers in design, production, instrumentation, maintenance, quality control and field service.
Metermaster **Write 259**

Short Form Catalog. Quartz tuning fork crystals as small as 7×2.7×1.7 mm are described in this new short form catalog from Statek Corp. Crystals with various lead configurations are covered, along with leadless types for surface mounting. Also included are five series of miniature oscillators based on Statek quartz crystals.
Statek Corp **Write 258**



Quad Output Switchers. A 4-pp. bulletin describes new quad output "Cool 1" Series switchmode power supplies. Details include features, specifications, standard and custom options, dimension drawings and voltage/current rating charts for the sixteen new hi-efficiency switchers. #143A.
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