

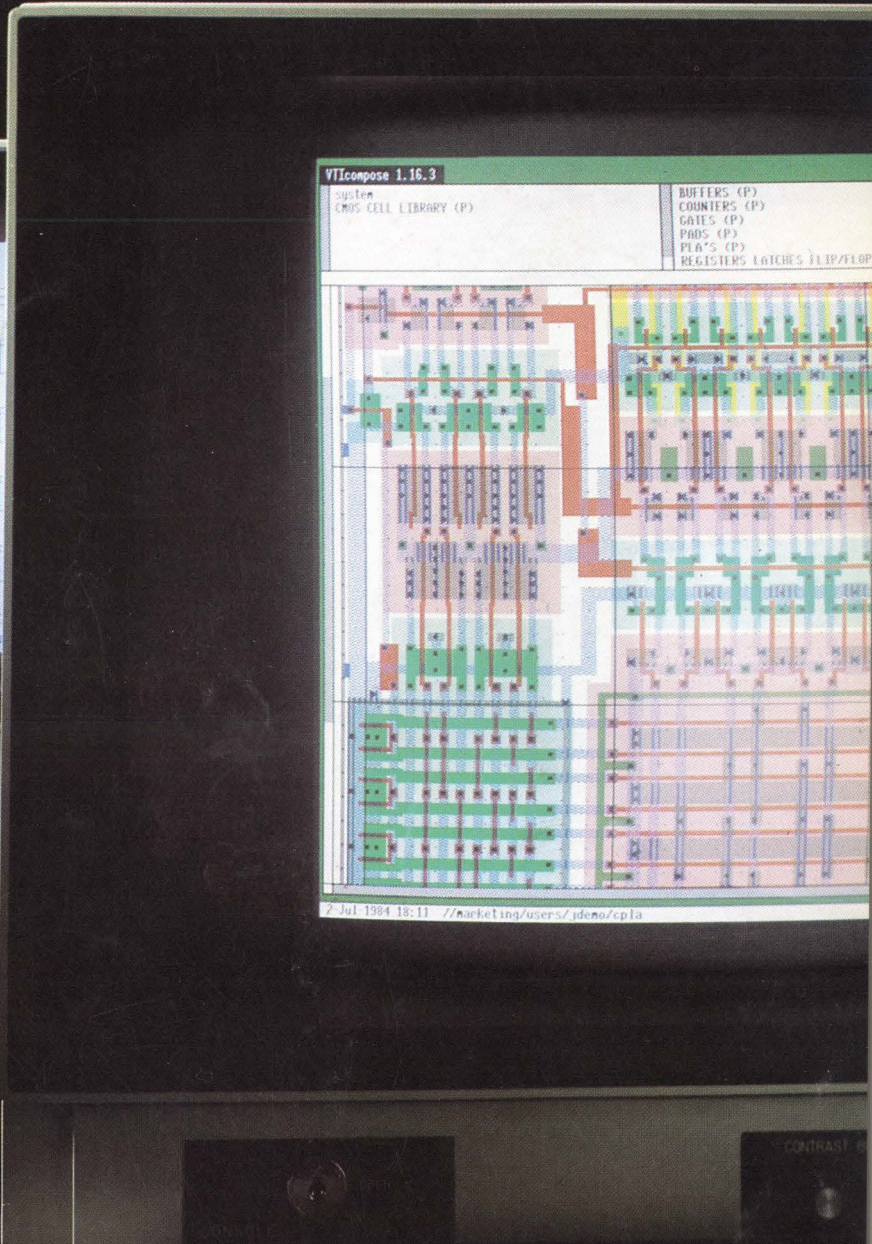
DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

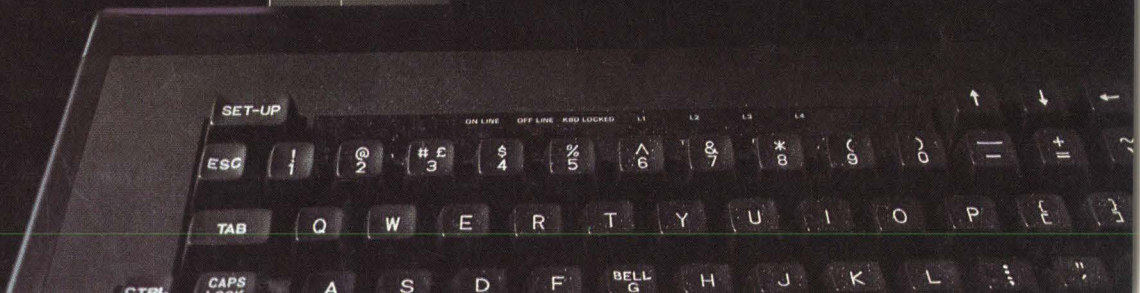
AUGUST 1984

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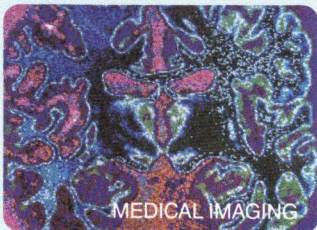
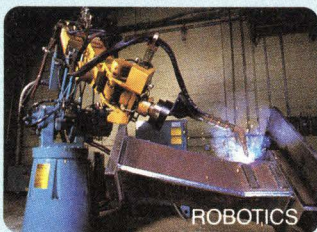
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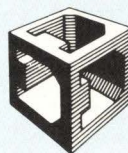
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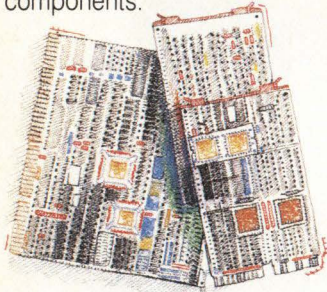


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NOTHING IN THE WORLD SUPPORTS OEMS LIKE Q-BUS.

Few companies could legitimately promise you either the experience or the insight into the OEM market that has helped make Digital the number one choice and world's leader in systems and 16-bit components.



With well over 25 years' experience behind us, we've learned quite a bit about what it takes to be a good OEM and how we – as a supplier – can help.

We're aware of your concern for reliability and dependability. With your name on the product, you're naturally the first one to get any calls.

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We also understand the commitment you make when you select an architecture. And your need for support of that architecture. Not just from the manufacturer, but from third party sources as well.

These are precisely the reasons to choose Digital's Q-Bus* architecture. Because only

Q-Bus gives you the proven products and technologies, the flexibility, the commitment and support to help you reach your market. On time. And on target. With a minimum of risk.

CHOOSE THE INTEGRATION LEVEL THAT'S MOST PRACTICAL FOR YOU.

Q-Bus is nothing if not flexible. And that flexibility begins with the level of integration you

choose. From chips to boards to boxes to complete systems.

You may, for instance, have the time and resources to develop your own system around one of our J11* microprocessors, thus helping to reduce your hardware costs.

On the other hand, if deadlines are tight, you might opt for one of our complete systems, like the standalone Pro 350* workstation, the multi-user MicroPDP-11*, or our powerful

32-bit desktop MicroVAX I*. By radically reducing development time, perhaps almost eliminating it altogether, you increase your chances of beating your competition to market, thus permitting you to earn the higher margins available at the beginning of a product life cycle.

If your needs fall somewhere in between, we recently introduced three board level CPU products to work with. Our LSI-11/73*, a new CMOS microcomputer that benchmark studies show exceeds the performance of a similarly configured MC68000 or NS 16032 in most applications. Our KXT11-C* peripheral processor, which for the first time allows you to place multiple PDP-11* processors on the Q-Bus, assigning separate tasks to each. And Falcon-PLUS*, one of the smallest 16-bit single-board computers for dedicated or limited RAM applications. In addition, you have two versions of Micropower/Pascal* system software available to you for use in VMS* or RSX* development environments.

Digital's new board-level products also take full advantage of the Q-Bus' block mode transmission, which effectively doubles previous throughput to nearly 3 megabytes per second. That means Q-Bus – along with these new products and future generations – will be running strong well into the future with the full commitment of Digital behind them.

And since all are based on the industry standard PDP-11,

ENGINEERING APPLICATIONS	UTILITIES MANAGEMENT
MEDICAL/FINANCIAL SYSTEMS	METAL FABRICATION SYSTEMS
OCR DATA ENTRY	WOOD & PAPER PROCESS CONTROL
CUSTOMER SYSTEMS	ELECTRONIC INSTRUMENT TESTING
EDUCATIONAL RESEARCH	PUBLIC UTILITY QUALITY CONTROL
BUSINESS INSURANCE	WHOLESALE BUSINESS ADMINISTRATION
X-RAY DATA COLLECTION	MIXING PROCESS CONTROL
CREDIT PAYMENT COLLECTION SYSTEM	SCIENTIFIC LAB DEVICES
HIGH SPEED-DAC/ADC	RACETRACK BETTING EQUIPMENT
COMMUNICATION SWITCH	DATA COLLECTION DEVICE
INSPECTION SYSTEM FOR P.C. BOARDS	REALTIME CONTROLLERS
TELEPHONE INDUSTRY EQUIPMENT	PROCESS CONTROL
FINGERPRINT ID	DESK TOP GRAPHICS
ROBOTICS	ENERGY MANAGEMENT SYSTEM
EARTH STATION ANTENNA CONTROLLERS	GRAPHICS SYSTEMS
TORQUE DETECTION	COMPUTER BACKPLANE TESTER
SOFTWARE DEVELOPMENT	DATA ANALYSIS SUBSYSTEM
MOBILE COMM TERMINAL INSTRUMENTATION	PORTABLE COMPUTER
CAT SCANNERS	COMM FRONT-END PROCESSOR
DATA ACQUISITION	GYRO TEST STAND
INTELLIGENT CONTROLLERS	INDUSTRIAL PROCESS CONTROL
MILITARY NETWORK COMMUNICATIONS	CLUSTER STATION CONTROLLERS
WORKSTATION CONTROLLER	TELETYPES
DATA CONCENTRATORS	INFUSION PUMP
CABLE TV CONTROLLER	TYPESETTING
MEDICAL BILLING SYSTEM	HYDRAULIC ELEVATORS
INDUSTRIAL CONTROLS	TR SUBSCRIPTION MONITORING SYSTEM
FRONT-END CONNECTION TO NETWORKS	UNDERWATER SOUNDWAVE ANALYZER
IMAGE PROCESSING	FINANCIAL SERVICE FOR HOME BANKING
MACHINE TOOL CONTROLLER	COMMUNICATION MULTIPLEXER
COMMUNICATIONS	DATABASE MANAGEMENT
SMALL BUSINESS SYSTEMS	MULTI-USER WORKSTATION
COMPUTER TOMOGRAPHY	ETHERNET CONTROLLER
MEDICAL OFFICE SOFTWARE	MEASUREMENT
DATA ACQUISITION SYSTEM	COIN-OP GAMES
FRONT-END PROCESSOR	GRAPHICS BOARD FOR WORKSTATION
BAR CODE READER/CONTROLLER	DIAGNOSTICS CONTROL
FILE SORTER/NETWORK CONTROLLERS	PROTOCOL AND GRAPHICS TRANSLATOR
CLUSTER STATION CONTROLLER	TERMINAL MODE CONCENTRATOR
DESK TOP COMPUTER	SIGNAL PROCESSING
USER FILTERS	NETWORK TO LAZER MACHINES
CON FOR P.C. BOARD	GRAPHICS WORKSTATIONS

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you get the best of both worlds. Advanced capabilities. With proven technologies. So you become more competitive with less risk.

COMPATIBILITY MEANS MORE FLEXIBILITY, LESS REDEVELOPMENT.

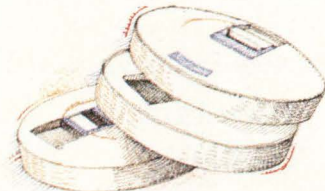
From the beginning, Digital has been dedicated to a single philosophy with its product families. Compatibility. Not just from product to product. But from generation to generation.

To the OEM, that's particularly important because it means you can upgrade your product at any time you like, with an absolute minimum of development.

Suppose, for instance, you designed around the world's first 16-bit microcomputer, our LSI-11*. And now you find that new demands on your product require a more powerful system. Upgrading your processor to our LSI-11/23* or LSI-11/73 is a simple matter. You don't need to learn a new operating system. And the changes to your software are absolutely minimal. With Q-Bus, instead of going back to the boards and starting over, you move your product to market. Faster. With far less expense.

MORE THIRD PARTY SUPPORT THAN ANY OTHER ARCHITECTURE IN THE WORLD.

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Q-Bus is not only supported by Digital's own line of processors and peripherals, but by those of any number of third party sources as well. From memo-

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BUILDING AUTOMATION	SIGNAL PROCESSING
ACCESS CONTROL ENERGY MANAGEMENT	MEDICAL ELECTRONICS
GRAPHIC ARTS	REALTIME TRAFFIC SIGNAL CONTROL
MILITARY ELECTRONICS	LASER MACHINE CONTROL
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TELEPROCESSING	RADIOLOGY
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SURFACE SCIENCE LASER DIODE TEST	GENERAL ACCOUNTING
ARTIFICIAL INTELLIGENCE DEVELOPMENT	DECISION SUPPORT SYSTEMS
VIBRATION ANALYSIS	OFFICE AUTOMATION
GENERAL ADMINISTRATION	GENERAL TIMESHARING
INDUSTRY SPECIFIC MIS	CENTRAL COMPUTING
INVENTORY	DATA PROCESSING
BUSINESS MANAGEMENT	MACHINE TOOL TESTING
MACHINE & PROCESS CONTROL	WEATHER DISPLAY SYSTEMS
QUALITY MANAGEMENT	OEM INSTRUMENTATION
QUALITY CONTROL LABS	ACCOUNTING DISTRIBUTION SYSTEMS
STRUCTURAL ANALYSIS	COLOR WEATHER GRAPHICS
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EARTH RESOURCE MANAGEMENT	SECURITY CENTRAL STATION
COMPUTER AIDED DESIGN	WELL LOGGING
ELECTRONIC ENGINEERING	PROJECT CONTROL
MATERIALS RESOURCE PLANNING	GRAPHICS, FILING
AUTOMATED MATERIALS HANDLING	DATA REDUCTION
ACADEMIC COMPUTATION	OPTICS
COMPUTER BASED EDUCATION	RESEARCH & DEVELOPMENT
COMPUTER AIDED MANUFACTURING	TEST APPLICATIONS
CHEMICAL RESEARCH	IMAGE PROCESSORS & MANUFACTURING
FACTORY CONTROL	SIGNAL PROCESSING
AUTOMOTIVE EMISSION TEST	MESSAGE PROCESSING SYSTEMS
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BOARD TESTING	SUPERVISORY CONTROLS, GAS
FACILITY MANAGEMENT	RECORD MAINTENANCE
HEALTH CARE	X-RAY
MEDICAL TEST EQUIPMENT	BUILDING AUTOMATION ENERGY MANAGEMENT
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ROBOTICS CONTROL	HIGHER EDUCATION ADMINISTRATIVE/AC
MACHINE VISION DEVELOPMENT	VOICE INPUT/OUTPUT
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DATA TRANSMISSION	PROCESSING ELECTRIC LOGS
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INSTRUMENTATION ANALYSIS	REALTIME I/O
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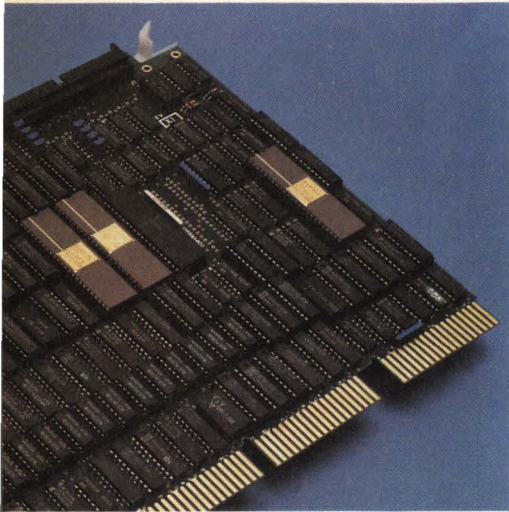
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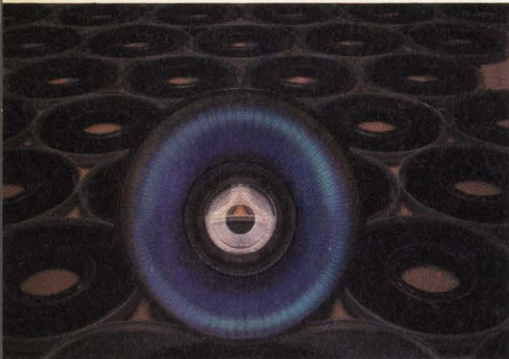
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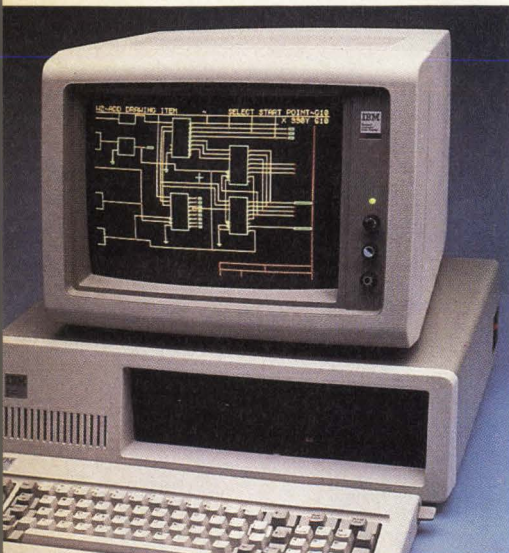
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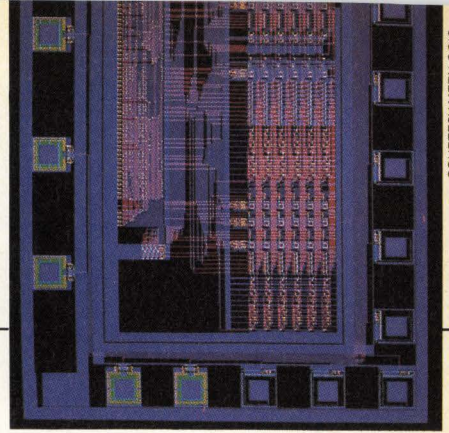
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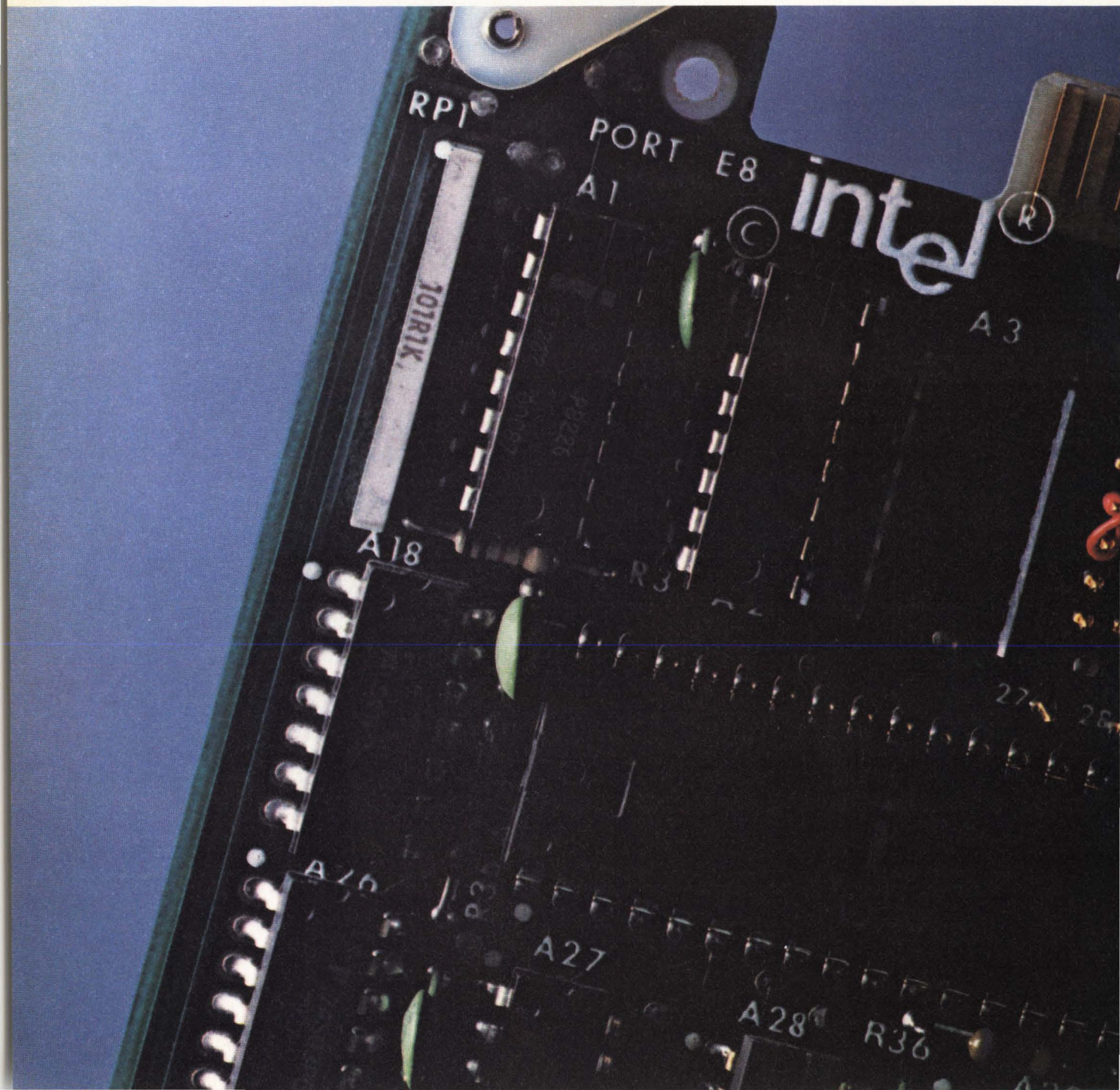
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The next generation of 32-bit machines from Zilog, National Semiconductor, Motorola, and Intel will include full 32-bit address and data paths, and the ability to support virtual memory.
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Although Pascal is an example of structured programming, others in the industry feel that it isn't a very good example, at least when applied to "real world" programming problems.

ON THE COVER

VLSI Technology Inc.'s (San Jose, CA) completely integrated cell-based IC design system takes a design from hierarchical chip planning through schematic entry, physical layout, simulation and verification, and results in PG tapes ready for fabrication in VTI's silicon foundry. VTI's advanced proprietary tools include a cell compiler library that gives a designer the convenience and ease of designing with cells that can be modified to meet the functional and parametric needs of a particular design.

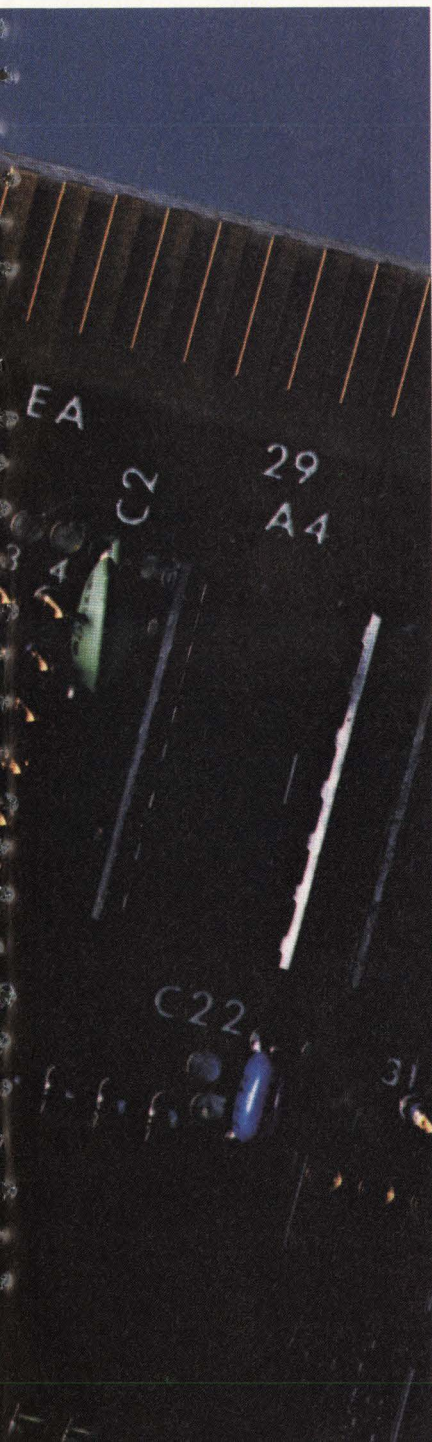
Photo courtesy VLSI Technology Inc.

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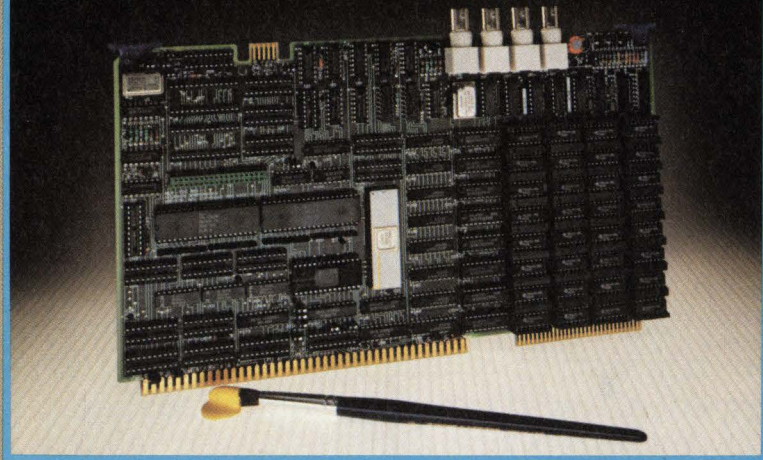
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The Lundy UltraGraf[®] is absolutely the fastest draw in the West or anywhere else.

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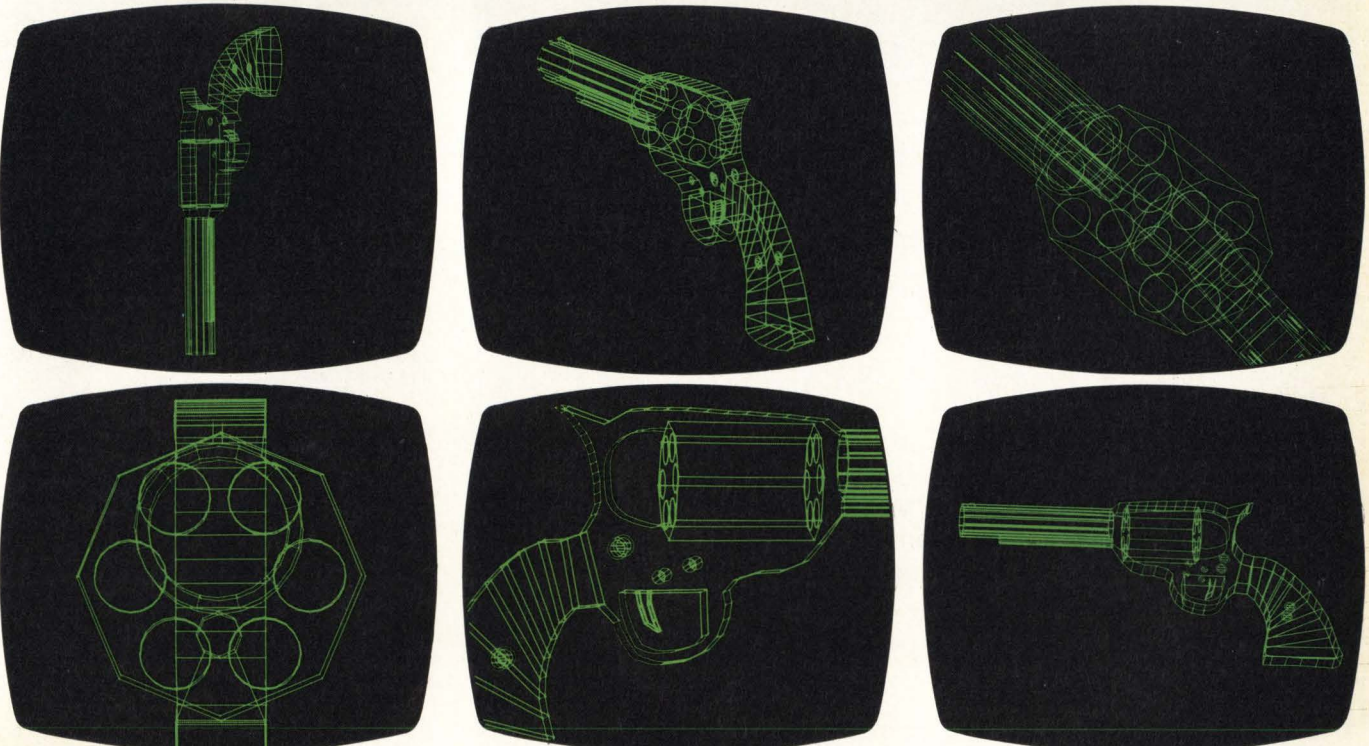
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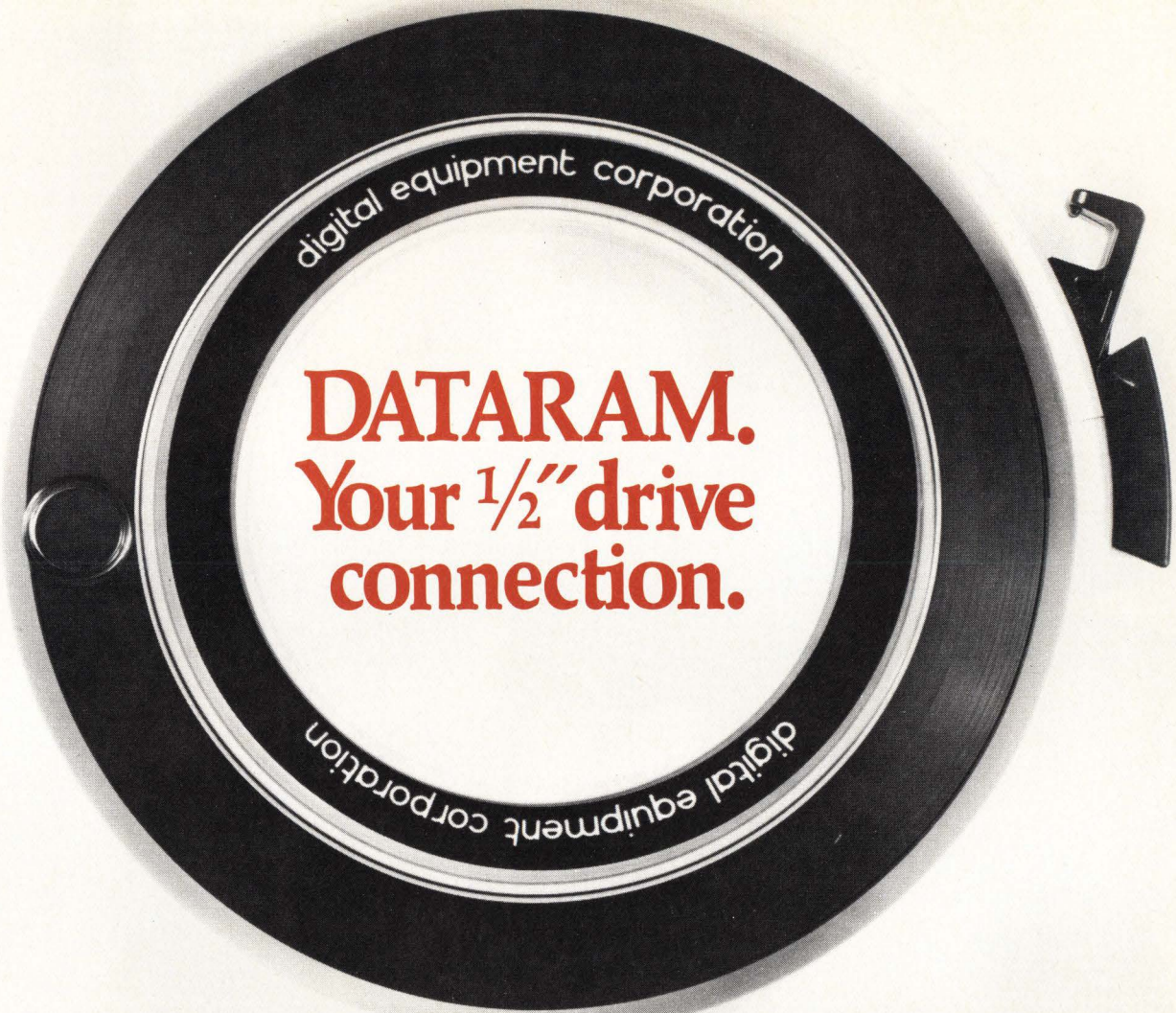
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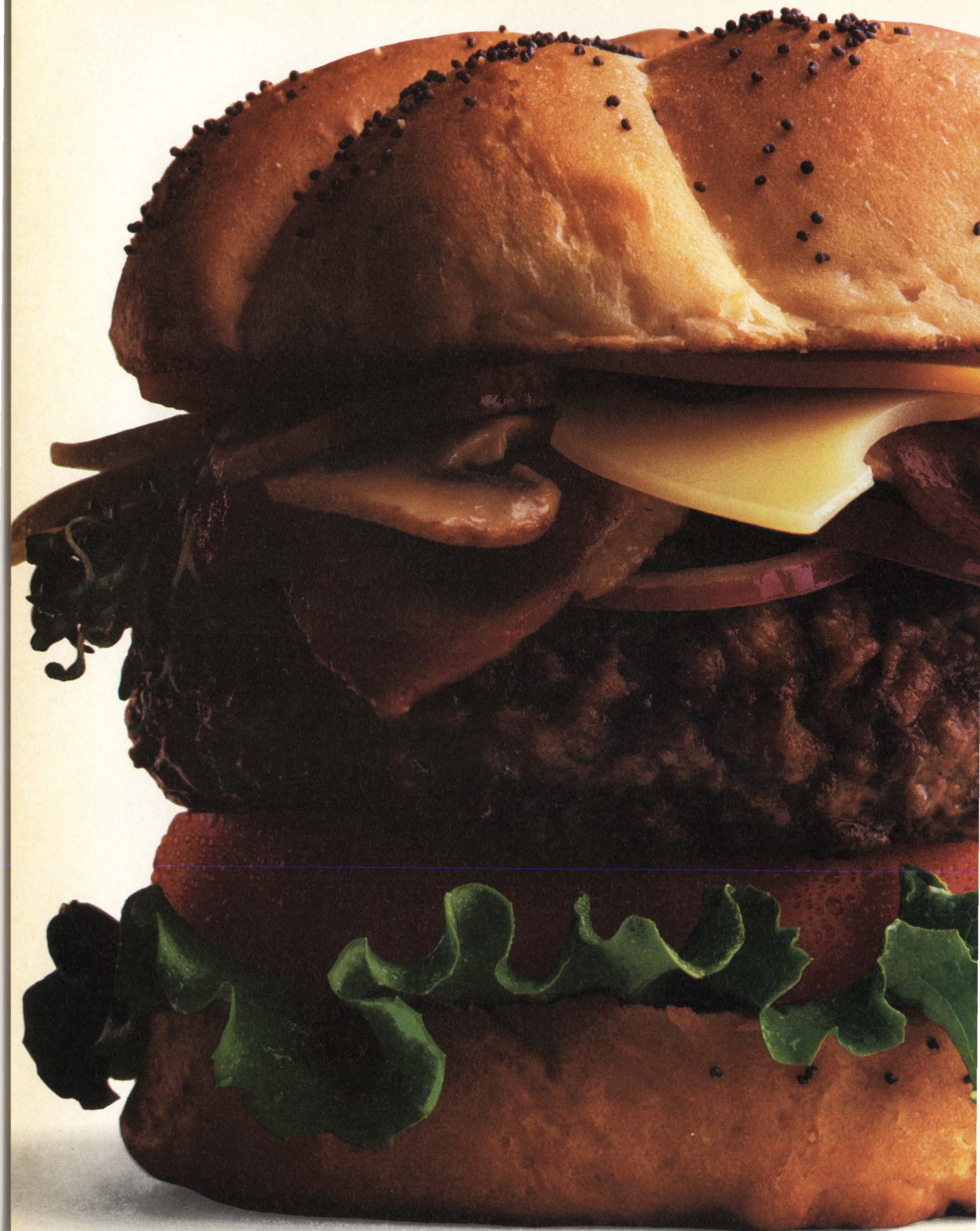
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‘Demands for more processing and storage in smaller packages are being met by products shown at NCC. Making VLSI-based products to meet needs within market windows could be easier with silicon compilation.’

EDITOR'S COMMENT

Packing high-performance computing into desktop or smaller sizes is a major thrust for our industry. The first of the full 32-bit microprocessors will meet some demands for more power in smaller devices. Motorola's 68020 and the NCR 32 were both displayed at the NCC show in Las Vegas last month. Our article on 32-bit microprocessors this month demonstrates that, like other areas of design, there are trade-offs between products. The 68020, for example, has only instruction cache; data cache is not on-chip.

The NCR 32-bit microprogrammable processor may be used by Spectra Systems in their next VAX minicomputers-in-a-desktop-package, according to spokesmen at NCC. Using new processors, semi-custom and custom VLSI, such systems pack the power and operating methods of established computer lines, in this case DEC computers, in packages a fraction the size.

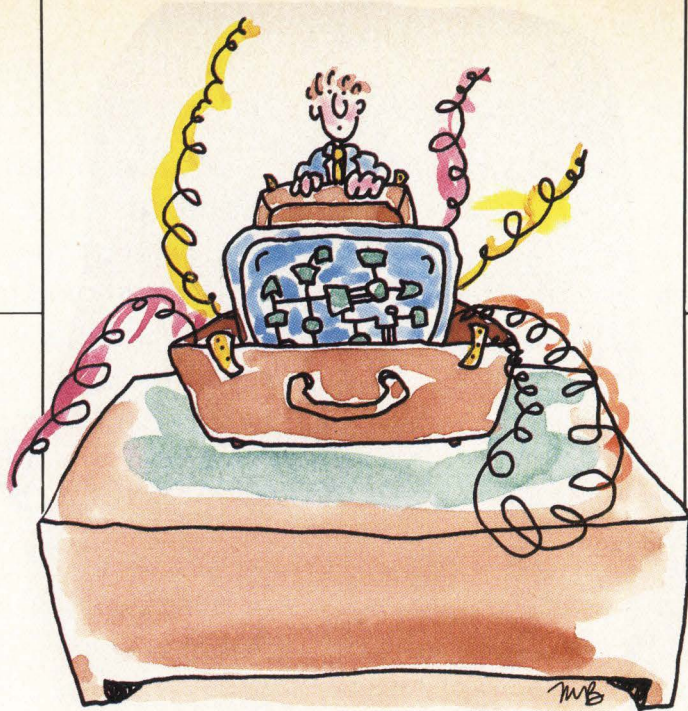
Desktop and smaller systems with power formerly offered only by refrigerator-size minicomputers need high-capacity data storage in a small footprint. In this issue, Bob Hirshon looks at magnetic disk and tape drives to meet the needs of micro and portable computer storage.

Downsized memory systems with low power consumption and very high capacity were everywhere in evidence at the NCC. Disk and tape drives in a 3½" form factor were displayed, as well as 5¼" high-capacity drives. Interdyne showed a 3½" tape system with no cassette or cartridge, for interchangeability. Small high-capacity drives like the Maxtor 170 Mbyte 5¼" Winchester were also displayed in configured systems and storage subsystems, like US Design's subsystems. Companies including Priam showed small disk drives integrated with backup.

Another type of dense data storage was premiered at NCC — optical disk drives. Although initial systems are not in a small form factor, the 1-4 Gbytes available on a single 12" or 14" disk surface is phenomenal. As pointed out in this month's article on optical disk storage, these drives will not compete with magnetic systems, since they are not erasable. They should become a new class of storage peripheral for on-line archives.

As much storage and processing power as is available is already in demand for graphics systems. Both the products at NCC and Gregory MacNicol's article in this issue show that graphics modules are designed to accommodate the demands of specific applications. The article focuses on choices when designing bus-based graphics systems from the board level.

Several new systems at the NCC pointed out innovations in architecture and bus structure. Argonne announced a loosely-coupled multiple-CPU system based around the Multibus II,



which Intel themselves have not yet used commercially. Flexible Computer is using an "erector set" architecture to develop a multiprocessing real time system. With two common buses, 10 local buses and a VME bus, the computer can easily be expanded or condensed.

It seems that DEC-compatibility is no longer such a hot item, however. Many of the vendors in that market seemed relatively idle. It looks as if DEC themselves may purchase subsystems from several companies to meet market window.

Vendors of communications and particularly local area networking products seemed very busy. At the main entrance to the exhibit hall, 13 major computer, communications and industrial controls manufacturers linked their equipment in two LANs with NBS protocols. One booth, spearheaded by General Motors, used IEEE 802.4 broadband token passing topology. The other was Ethernet-like 802.3 CSMA/CD baseband.

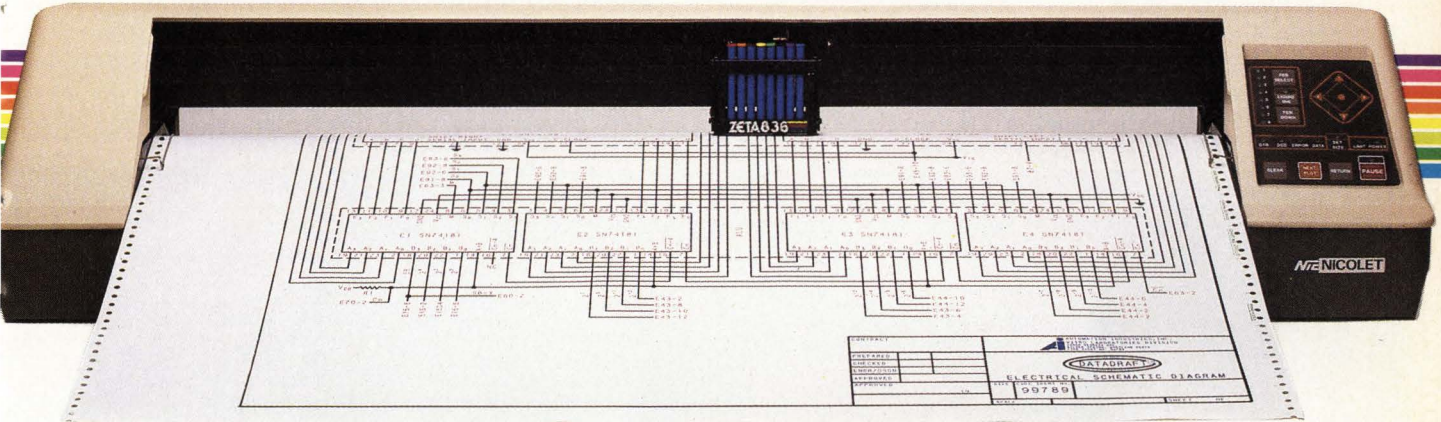
As any large trade show, the NCC juxtaposed some of the largest companies in the world with new start-ups. Meeting production dates and specs without suffering continue to be problems for small companies.

But Ron Collett's article this month presents a new VLSI design methodology that could allow more firms to produce working products during the critical market window: silicon compilation. This design path allows logic designers to create application-specific ICs in silicon very rapidly. Market windows formerly open exclusively to companies with vast resources could open up to smaller systems houses now. The major semiconductor and computer houses are researching silicon compilation, too. But the tradeoff of larger die size may not pay off for the quantities they will produce.

New methodologies and technologies could shake up the industry. Judging from the low attendance, NCC probably didn't. It appears that I'm not the only one suffering from trade show burnout. Or maybe it was fear and loathing of Las Vegas in July. At the rate technology is going, we may be able to avoid travel to trade shows. I hope we can really pack a VAX in our briefcase and analyze all of the new products on display in a traveling tractor-trailer.

Julie Pingry, Senior Editor

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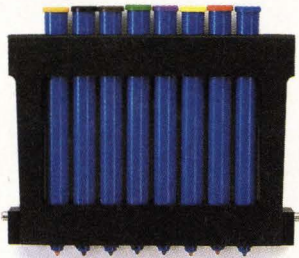


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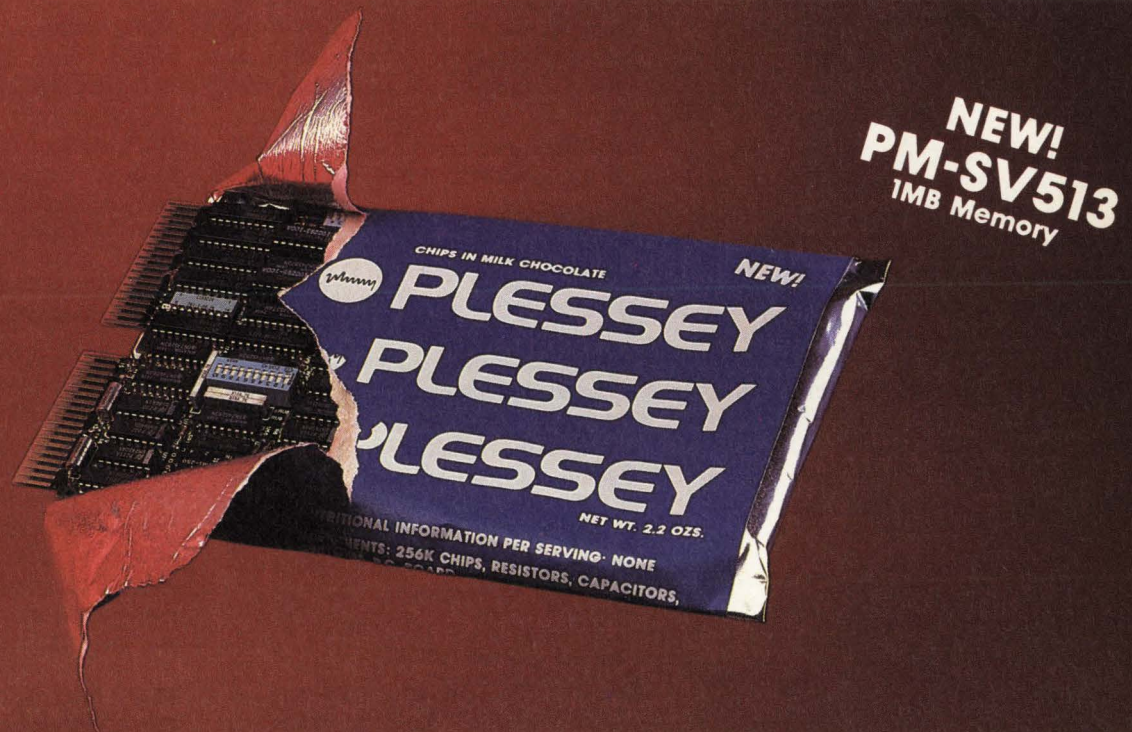
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VAX LISP

The first fully supported Artificial Intelligence (AI) product from DEC, VAX LISP, is designed to run on Digital's VAX computer line and VAXclusters, and is targeted towards AI programmers and researchers in university, industry and government. VAX LISP is an implementation of COMMON LISP, a version of the LISP programming language.

Second Sourcing

Western Digital Corp. has entered into a license agreement with Texas Instruments whereby TI will become a second source for various storage and communications controllers designed and manufactured by Western Digital. The agreement covers components from Western Digital's line of integrated circuit floppy disk controllers and high level protocol devices. TI plans to manufacture and market Western Digital's WD1770/1772 and WD1773 floppy disk controllers, the WD279X family of floppy disk controllers, and the WD2501/2511 X.25 communications controllers.

Printronix Acquires Anadex



Printronix, Inc., manufacturer of computer line printers, has signed an agreement in principle to acquire Anadex, Inc., a privately-held California-based company engaged in the design, manufacture and sale of serial matrix computer printers, in exchange for \$8,000,000 of Printronix common stock. Printronix designs, manufactures and markets medium and low speed matrix impact line printers designed for use with minicomputer systems and microcomputers, such as multi-workstation office systems and other small computer systems.

Disk Controller Development for VME

Interphase Corp. and Mostek Corp.'s Systems Technology Division have entered into a technology development agreement to develop an SMD disk controller for the VME microcomputer bus. The single-board controller would be the first available which matches the performance capabilities of the 32-bit VMEbus. The VMEbus was developed in 1982 by Mostek and two other companies (Motorola and Signetics). The bus also supports 16-bit and 8-bit microcomputers.

Daisy Supplies IMI With Workstations



Daisy Systems Corp. will supply computer-aided engineering (CAE) workstations to International Microcircuits Inc. (IMI), of Santa Clara, CA, a gate-array semiconductor manufacturer. IMI will lease the Daisy workstations to its customers so they can design IMI semi-custom gate-array CMOS circuits on the system in-house.

UNIX System V Ported To Intel iAPX 286

Digital Research Inc. has retained UniSoft Systems, of Berkeley, CA, to assist in the development of a version of AT&T's UNIX System V operating system for Intel Corp.'s iAPX 286 microprocessor. Under previously announced agreements, Digital Research and Intel are engaged in a program to produce a version of UNIX System V for the iAPX 286 for AT&T Technologies. Digital Research will design the memory-management portion of the UNIX System V kernel for the 286. UniSoft will contribute to that design and will participate in its implementation.

Gould Joins MCC

Gould Inc. has joined the multi-company research venture Microelectronics and Computer Technology Corporation (MCC), located in Austin, TX. Gould is the 18th participant in MCC, which was formally launched in 1983 to conduct long-range, advanced electronics research. Gould's prime areas of research will include computer science and software, digital signal processing, microelectronic devices and advanced materials for electronics.

CSPI, DEC Marketing Effort

Digital Equipment Corp. and CSP Inc. (Billerica, MA) have signed a cooperative marketing agreement intended to promote customer recognition of the benefits of the joint use of CSPI's MAP array processors and Digital's VAX-II and PDP-II computers for computationally demanding applications. The two companies will work cooperatively in marketing, promotion, sales, and applications support efforts. CSPI's Mini-MAP product line is specifically configured to provide 32-bit floating-point arithmetic enhancements to VAX and PDP-II computer systems.

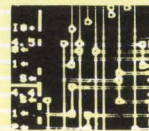
Computervision And Metheus Joint Venture

Computervision Corp. and Metheus Corp. have formed a joint venture to design, develop, and market electrical computer-aided engineering (CAE) workstation products. Headquartered in Hillsboro, OR, the joint venture will be called Metheus-CV, Inc., and will combine products and include personnel from both Metheus and Computervision. Market emphasis will be in the areas of CAE, design, test, and manufacturing products for custom ICs, standard cell and gate arrays, hybrid, and printed circuit board design applications.

ILC Data Device Establishes Japanese Subsidiary

ILC Data Device Corporation (DDC) has established a subsidiary company in Japan to sell and market DDC's products in Japan and the Far East. The new company, DDC Electronics K.K., should allow DDC to expand its presence in the Far East marketplace and result in increased growth for the Company. ILC Data Device Corporation develops and manufactures hybrid and discrete data conversion and MIL-STD-1553 data bus products.

Fairchild/VTI Co-Development



The Gate Array Division of Fairchild Camera and Instrument Corp. and VLSI Technology, Inc. (VTI) have signed a co-development and alternate source agreement for Fairchild's two-micron CMOS gate array family. The agreement includes provisions for joint product specification and development, product and software exchanges and process cooperation. VTI will have the right to offer Fairchild's gate array development system, FAIRCAD, to its customers through its regional design centers, and Fairchild will have the right to use VTI's proprietary cell-based custom design system for the development of additional gate arrays and gate array macros.

CIE Systems To Market Pick

CIE Systems, Inc., a subsidiary of C. Itoh Electronics, Inc., has signed an agreement with Pick Systems to license the Pick operating system for use with its line of 68000-based multi-user business computer systems. Initial production is set for the third quarter 1984.

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UPDATE

PC Systems Design Software



Arthur Andersen & Co. announced the availability of a systems design software package, known as DESIGN/1, that can improve the productivity of systems design teams in large software development projects. The proprietary DESIGN/1 package runs on IBM PC or PC XT personal computers, and can support a multiple workstation environment using a local area network. It is primarily intended to support design teams working on systems development and implementation projects for medium and large computers.

PC Company Focuses On OEM Niche

OEMTEK, Inc., a new compatible PC company, has been formed to offer an open-architecture line strictly to OEMs, value added resellers and systems integrators. They hope to fill the void created by the current market scramble, which has left the needs of the OEM unaddressed.

Corvus Acquires AI Software

Corvus Systems, Inc., a subsidiary of Corvus Corp., has acquired BL Associates, a Department of Defense contractor specializing in artificial intelligence software. BL is Corvus' second recent acquisition in the artificial intelligence arena. With its earlier acquisition of Greenbriar Systems, Inc., Corvus is now marketing services to the defense and intelligence communities.

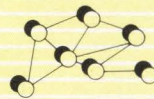
Control Data Integrates Xerox 8700

A multi-million dollar agreement to sell electronic printers to Control Data Corp. was recently announced by Xerox Corp. The printer is the OEM version of the Xerox 8700 electronic printing system. As part of the agreement, the printers will be used exclusively for the Control Data line of mainframe computer products, including the company's CYBER Systems and its new CYBER 180 product line.

DEC Rainbow and IBM PC Subsystems Use SyQuest Drives

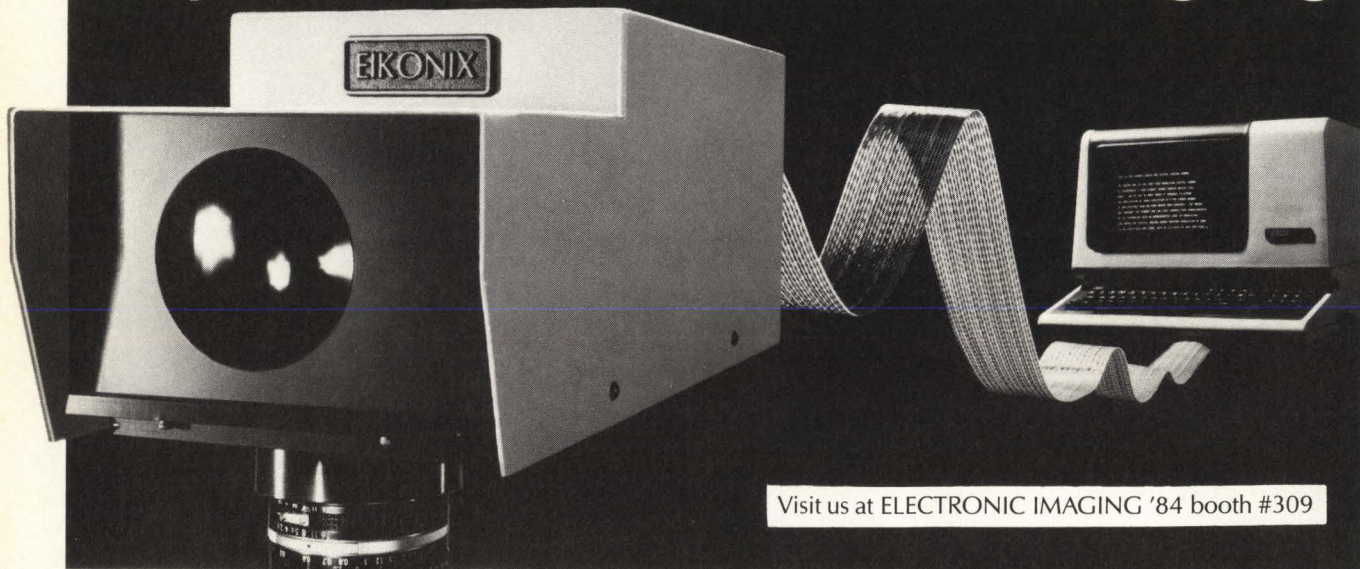
Under terms of a recently signed \$5 million contract, SyQuest Technology is shipping SQ306RD, 6.38 Mbyte, removable Winchester-technology disk drives to Univation Inc. The drives will be sold by Univation as part of add-on subsystems, and integrated into computer systems featuring both DEC Rainbow 100, and IBM/PC personal computers.

Rixon Acquired By Case



Case (Computer And Systems Engineering plc) of Watford, England has completed its acquisition of US data communications manufacturer Rixon Inc. (Silver Spring, MD). The purchase, valued at approximately \$27 million net of Rixon's cash balances, was previously attempted by Digital Communications Associates (DCA) of Norcross, GA, but never completed.

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WASHINGTON REPORT

by Anne A. Armstrong

House Increases NSF Funds For Supercomputers

In what Congressional backers proclaimed was a clear statement of support for supercomputers, the House has increased fiscal 1985 funding for supercomputer research at the National Science Foundation to \$60 million — a 50% increase over figures proposed by the Reagan administration in its budget.

The legislative history which accompanies the bill makes clear that the House expects not just a research effort, but also support services for universities and industry researchers. The House Science and Technology committee specifically mentioned that it wanted to see the establishment of a distributed supercomputer network that would create a market for lower-priced, high-performance machines.

The House also broadened NSF's traditional emphasis on basic science research to include more support for engineering research, a move that had been promoted by IEEE and other professional engineering societies.

The National Bureau of Standards did not fare so well in its efforts to get into supercomputers. Authorization for \$4.3 million to buy a class 6 supercomputer was cut in half as the NBS administration was instructed to look into longer leases or lease-back arrangements.

Incompatible Chip Protection Bills

Bills to provide protection to semiconductor masks have passed both houses of Congress, but in such different forms that major compromises will be necessary in conference if any legislation is to be sent to the President for signature this year.

The House version creates a new form of intellectual property protection for semiconductor masks, similar to that proposed for design works. It protects reverse engineering and limits damages by innocent infringers to "a reasonable royalty."

In contrast, the Senate version is based on traditional copyright concepts because Senate supporters were unwilling to jettison that accumulated body of copyright law and precedent in favor of a new concept that has not been

judicially tested. Under the Senate version, reverse engineering is not permitted as fair use and the criminal penalties that have been part of the copyright law are retained for all infringements.

Although both bills have grown out of a concern that some protection must be offered to creators of chips, the fundamental differences between the two approaches are so great industry officials are concerned that conferees are going to have major problems reconciling the wishes of both chambers.

National Semi, Boeing, and SDC Run Into Trouble

The Defense Logistics Agency is prepared to bar National Semiconductor Corp. from supplying military aerospace parts for up to three years if the company does not meet government demands and name the personnel involved in a testing and certification fraud against the government. Last March, National pled guilty to 40 counts of making false statements to the government concerning the testing of chips for the Pentagon. As a result, the company agreed to pay \$1.7 million in fines and, according to industry figures, expected in return some form of suspension or reprimand.

During negotiations with the government concerning the payment of court costs, DLA asked for the names of seven individuals it believes were involved in the fraud. When National refused to provide individual names, but insisted the company itself would stand responsible for any crimes, DLA moved to bar the chip maker from any contracts for which it is not the sole source for a period of up to three years. National officials have indicated that they plan to appeal the action. A large portion of the company's current business with the government is sole source work, a company spokesman said.

Boeing Computer Services Company's federal systems division has run afoul of the Interior Dept. in a contract for the Parks Service. Interior claims that Boeing has inside information which it used to formulate its winning bid for a \$5.9 million financial and cost-tracking system for the park service. As a result, the contract has been cancelled and the federal systems group has been suspended from bidding on any future

government contracts for one year. Boeing has indicated that it will appeal the suspension.

The Federal Bureau of Investigation has been ordered by a federal court judge to cancel its contract with System Development Corp., a subsidiary of Burroughs Corp., and award the \$49 million contract instead to Delta Data Systems of Trevese, PA. Delta Data had sued to block the contract charging that both its bid to supply terminals and printers to the FBI was lower and its equipment more advanced than SDC's. The FBI was accused of downgrading the technical rating of the company's bid because it was uncertain about Delta Data's financial health.

When the contract was cancelled, SDC had already supplied 634 B-20 Burroughs terminals and 312 printers out of the more than 6000 terminals and nearly 3500 printers specified in the original contract. Changing vendors in midstream has thrown both the FBI and SDC into confusion. Already in place for the summer is an SDC-based system to monitor the security for the Summer Olympics and the national political conventions. And SDC has already spent millions executing the contract, according to a company spokesman. He suggested that changing vendors at this point would be very expensive for all concerned.

E-COM Shut Down Facilities

The U.S. Postal Service's Board of Governors has decided to close down the Postal Service's electronic mail operation, E-COM, and to sell or lease its equipment. E-COM has lost money since it was launched in 1982 and has met with objections from private sector competitors concerned that E-COM's low rates were made possible by subsidies from first-class mail. The Board offered no explanation for its decision to act at this time.

The governors directed the USPS to file a termination notice with the Postal Rate Commission within 30 days. How long after that it takes to actually end the service and dispose of the equipment remains uncertain. Postal Service officials estimate some \$40 million worth of equipment in 25 post offices will be sold or leased to private firms.

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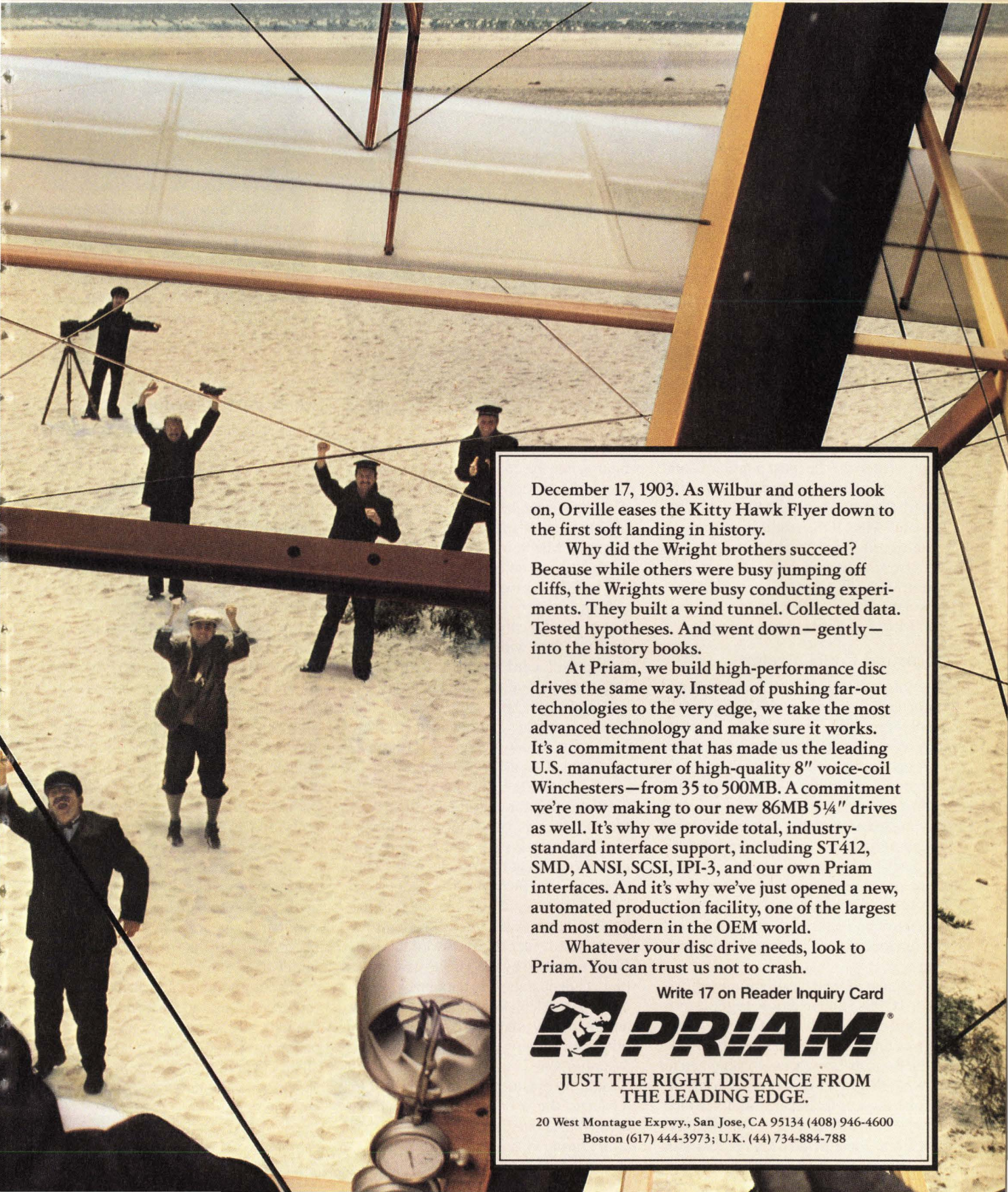
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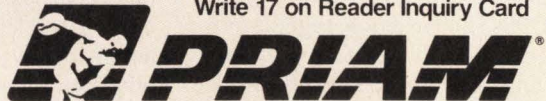
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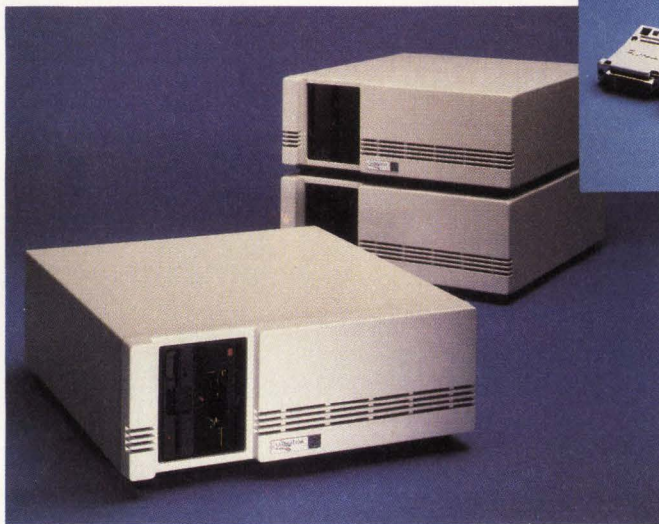


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Applications Run Concurrently In Multi-Operating System Environment

In order to offer users a wider choice of available applications, Molecular Computer (San Jose, CA) has introduced two new multiprocessor systems, the Molecular Series 9 and Series 36. Both are software compatible members of Molecular's Supermicro "X" family of systems. These new generation multi-user systems have been designed to allow users to concurrently run applications written for the most popular 8- and 16-bit operating systems, including CP/M-80, MP/M-80, CP/M-86, MP/M-86, and MS-DOS. Additionally, these systems provide a virtually linear growth path from a low-end three-user configuration with 20 Mbyte of hard disk to a powerful 64-user system supporting over 400 Mbyte of online mass storage.



Terminal Concentrator

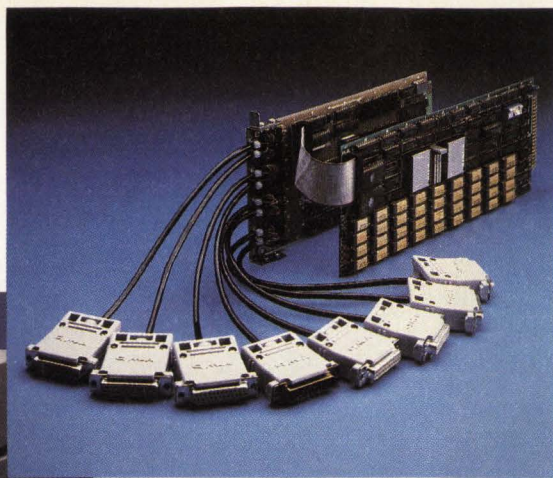
The introduction of a terminal concentrator to Molecular's networking environment increases user flexibility. Systems may be configured for the particular mix of 8- and 16-bit processors (and operating systems) required for a given set of applications. Additionally, any user may rapidly make a transition between different operating systems, leaving time-consuming batch processing to execute in a stand-alone processor. When the job stream is complete, the user may reattach to the processor and either release it to be used by someone else or execute another program.

A typical Series 9 configuration utilizing a TCP is shown above. Eight terminals are attached to the TCP, with each user having the ability to select from one of the 8- or 16-bit processors attached to the system bus. This particular configuration has a terminal concentrator, a tape interface card, and a mix of application processors, occupying a total of 9 slots in

the base system chassis. Additional boards may be configured in the system by adding one or more expansion chassis. The same expansion chassis may also be used to increase the online disk storage in 20 or 60 Mbyte increments, depending on the cabinet selected.

The TCP is a two-board set consisting of both a processor and multiplexer card. The processor card is actually a standard 16-bit AP/186 with 256K of RAM. The multiplexer card employs four 2-port DART chips that provide eight ports of serial I/O at 19.2K baud per port (for an aggregate maximum throughput of 153.6K baud). The AP/186 is connected to the multiplexer via a parallel bus and acts as a dedicated controller for the multiplexer.

When configured in as part of the TCP, the AP/186 runs a proprietary multitasking operating system that oversees the operation of each terminal port. This firmware also provides the system logic functions for each user attached to the TCP. When a particular user identifies himself and enters his password, his profile is searched by the TCP to determine his default operating system choice, if one exists. If a default has been selected, he is automatically attached to an application processor running that operating system, assuming one is immediately available. Should no default have been defined in advance, the user is presented with a menu that allows him to select his choice of operating system.



Above: Molecular's Terminal Concentrator Processor (TCP) is a two board solution allowing user-selectable 8- and 16-bit processors and multiple operating systems. Left: The Molecular Series 9 multimicro computer features 8- and 16-bit processors; CP/M, MP/M and MS/DOS. The expansion module is in the background.

Modular Expansion

Molecular has also developed the MMI, or Molecular Modular Interconnect. The MMI allows the system bus (m/BUS) to be extended between system enclosures. Thus, two systems may be physically joined to operate as a single, larger system. Also, multiple expansion cabinets (to a maximum of five) may be attached, accommodating additional users and/or mass storage capacity.

For example, a small business may start with a single three-user 20 Mbyte configuration and enlarge the system with 8- or 32-slot expansion cabinets to a maximum of 64 application processors and 400+ Mbyte of online disk storage. Processor and mass storage capacity may be independently added to accommodate different varieties of application and user environments. Also, 8- and 32-slot systems and expansion cabinets may be freely interchanged as required.

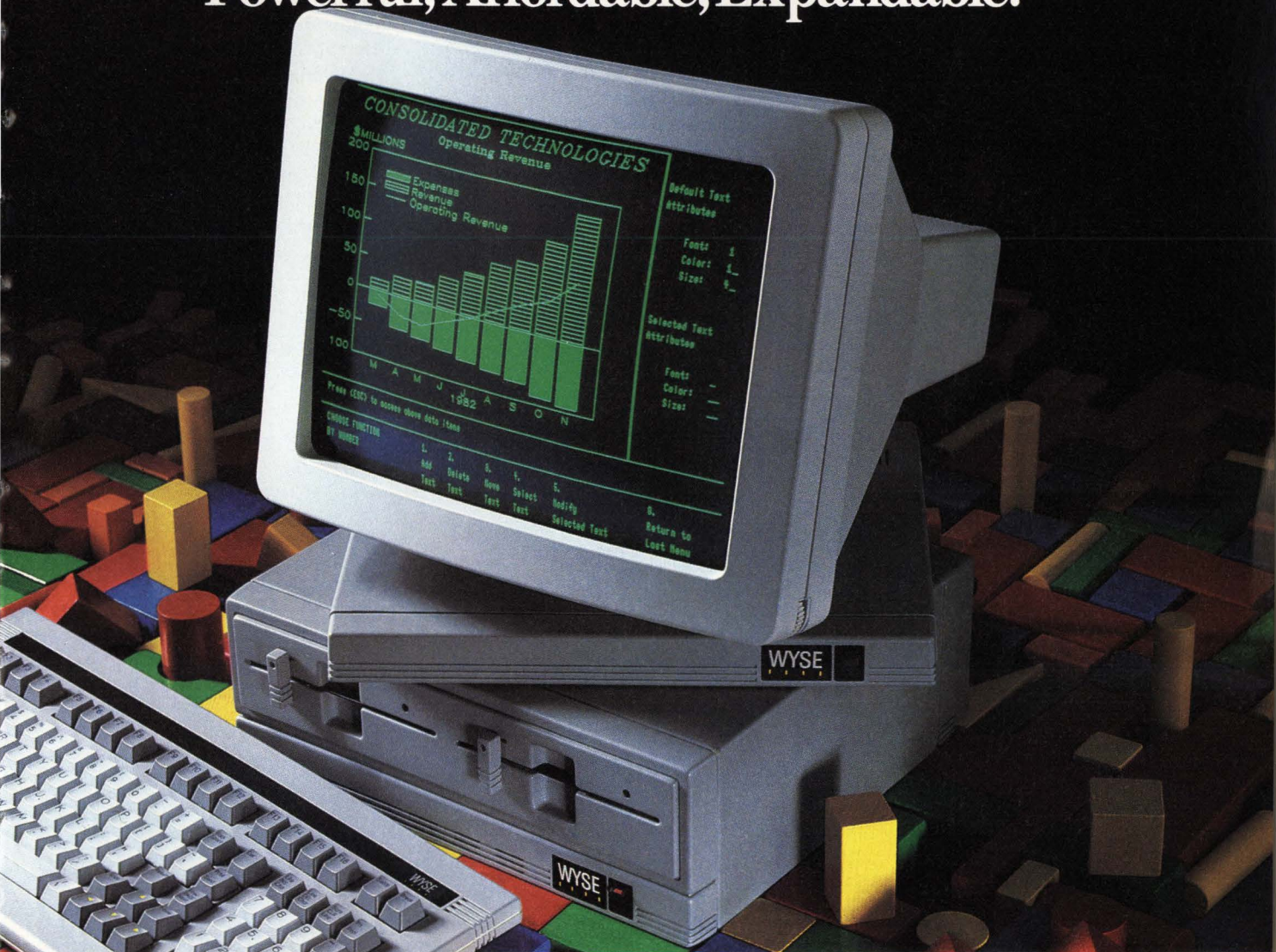
The MMI may also be used to reduce mass storage contention in disk-intensive applications. Expansion cabinets may be configured with separate File Processors, in order to distribute disk I/O among different disk drives and controllers. By eliminating a single controller as a system "bottleneck," overall performance may be dramatically improved. The n/STAR operating system will automatically route all disk operations to the appropriate File Processor, yielding a true distributed I/O environment.

The MMI's ability to interconnect cabinets with separate File Processors

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also helps reduce technological obsolescence in Supermicro systems. As new mass storage technology is made available, disk/file processor subsystems may be introduced in separate expansion cabinets that attach via the MMI. This allows future generation mass storage products to be mixed with existing disk drives in a single system.

Multiple Operating System Support

As described earlier, the TCP provides the ability for users to easily switch between applications running under different operating systems. However, this addresses only part of the problem of supporting multiple operating systems in a single system. Differences between the MS-DOS and CP/M file structure provide another challenge to developers.

Two alternatives were considered in addressing these file structure differences: disk partitioning and hosting. Partitioning would require that a part of the system disk drive be reserved for the MS-DOS file structure. The remainder would be maintained by n/STAR, in its own native CP/M format. This necessitates permanently reserving space that may never be used and is inaccessible to CP/M software. Additionally, maintaining different work areas for each MS-DOS user would be impractical and wasteful of space.

Hosting was selected as the method of choice for supporting MS-DOS on Molecular systems. This involves the integration of MS-DOS "volumes," which appear to MS-DOS programs as separate disk drives within the existing CP/M file structure. Each MS-DOS volume, with its directories and other file structure elements, is fully contained within a CP/M disk file. A volume may be as large as 10

Mbytes, and there is no limit to the number of separate MS-DOS volumes that may exist within a single system. Import and export utilities are provided to facilitate the moving of data between MS-DOS and CP/M files.

Each MS-DOS user has a "profile" that contains the CP/M file name and location of every volume that he wishes to access. For example, a user may have his own volume assigned to MS-DOS's "A:" unit and a different volume assigned as "B:". Another user would have a completely different set of assignments. When the MS-DOS user logs in to the system and identifies himself, his unique profile is loaded and becomes active. This enables each MS-DOS user to have a private volume that appears as a separate "disk drive." He may also access a number of other volumes, including common work areas.

—Jerry Braun,
Molecular Computer
Write 223

8" Winchester Subsystems Provide More Storage For PCs

Powerful programs that allow personal computers to perform database management and other complex functions push the limits of PC storage peripherals. Winchester disks for micros are becoming common, and the increased expense of these disks makes backup a critical issue. Two major storage manufacturers, Priam (San Jose, CA) and Interphase (Dallas, TX) have incorporated hard disks with some means of backup into subsystems for personal computers.

Both of these subsystems include between 70 and 90 Mbytes of 8" Winchester storage, a controller and interface for the IBM PC (Priam also offers these for Apple) and a power supply. The configuration of the systems is very different, however. Interphase's RDS 375 uses 50 Mbytes of fixed and 25 Mbytes of removable 8" disk cartridge for 75 Mbytes of storage. Priam incorporates a tape drive for backup of their 86 Mbyte hard disk in the DataTower.

Simplifying backup is important for networked business microcomputers used for the critical work once reserved

for larger systems, as both of these companies have pointed out. Priam claims that DataTower allows file backup on the integral 1/4" 45 Mbyte streaming tape during system use with five commands. This scheme of integral backup capability on a Winchester subsystem is in all of Priam's DataTower subsystems, just an-

nounced this spring with IBM and Apple interfaces.

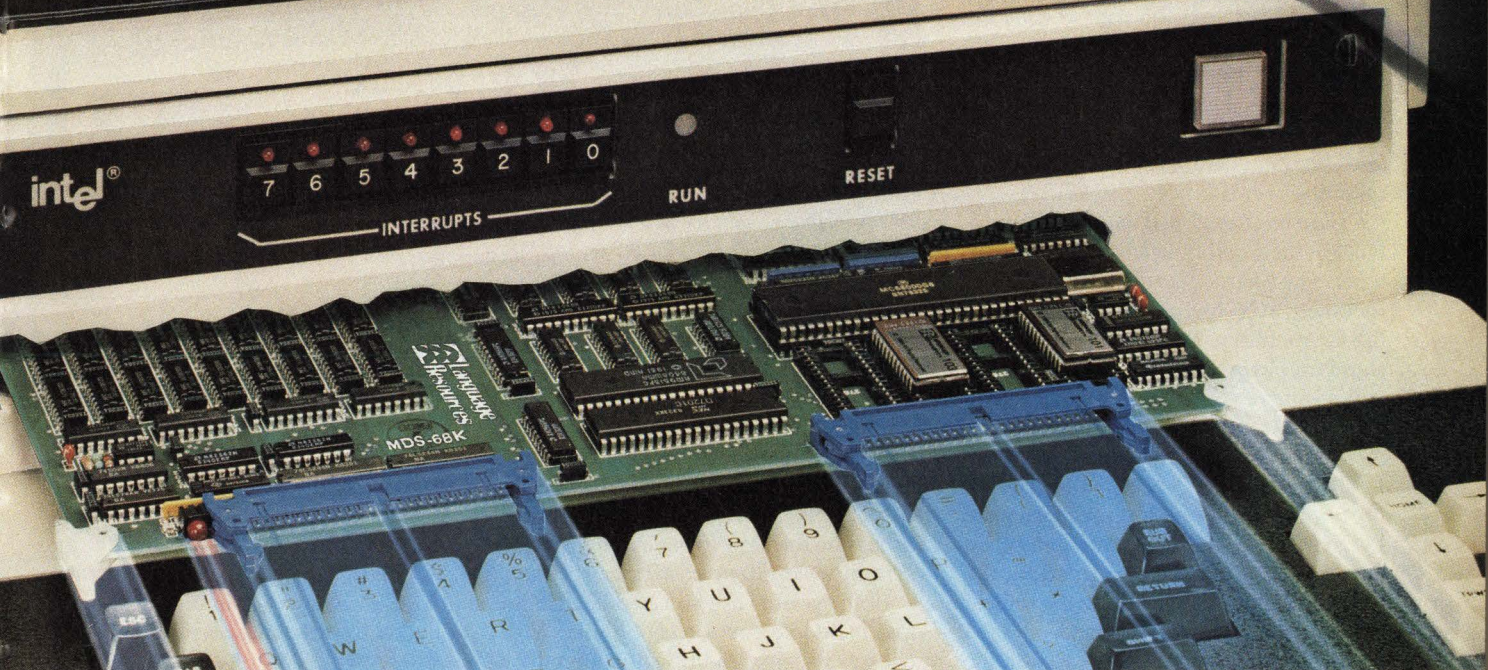
Though the Interphase system does not provide the traditional tape or floppy drive for backup, the removable Winchester of the Century Data Systems C2075 drive does provide high-speed secondary file storage. Unlike a fixed



Priam's DataTower pictured with Apple's LISA.

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LR's MDS-68K CPU board contains a 68000 CPU, 256K bytes of high speed RAM, proprietary ROM's, 2 serial I/O ports and a memory management subsystem. Plug it into any Multibus master card slot in an MDS system chassis, and run code in a true 68000 environment.

Development software tools — 68000 macro assembler, linker/locator, symbolic debugger, optional Pascal compiler and optional Host Communication Utility are supplied on ISIS compatible diskettes. Firmware on the MDS-68K CPU board contains

the ISIS I/O interface code. Together they allow you to develop and run 68000 user programs in the Intellec MDS environment.

With MDS-68K, you can extend the range of an Intel MDS to include full 68000 family development support without sacrificing those Intel features you have come to depend on. MDS-68K software and hardware is passive unless you access it through the special software provided in the package. Plus you can use available Intel tools (e.g., CREDIT[™], UPM) concurrently with MDS-68K.

The plug-in board provides you with two serial I/O ports for interfacing to one of the several available 68000 hardware emulators. You can develop code for Intel microprocessors while adding 68000 development capability without swapping out boards.

Our MDS-68K base package, including Motorola compatible assembler, linker/locator, symbolic debugger, 68000 CPU board and extensive documentation is \$5995. The optional Pascal compiler (C and PL/M-68K compilers available soon) are \$1995 each.

Major Benefits

- Provides 68000 family design freedom for your current Intel Intellec MDS
- Meets development support needs for designs using a 68000 family chip and an Intel controller chip (e.g. 8051)
- Saves capital equipment costs by utilizing existing MDS equipment
- Frees you from having to spend time learning a new development system's editor and other support tools
- Generates code identical to LR's XDS-68 cross-software on VAX/VMS and IBM VM/CMS.



Language Resources

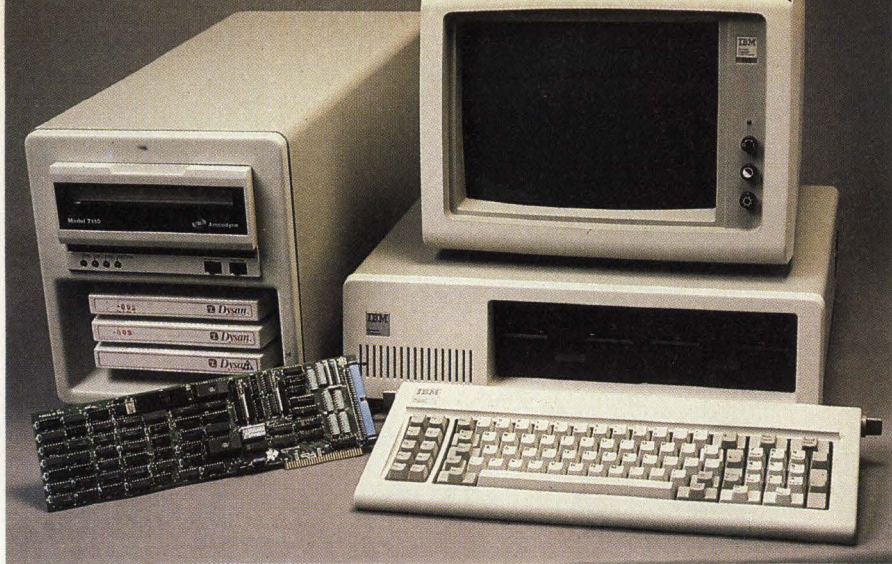
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disk, the removable cartridge allows unlimited storage in a single drive by replacement of the medium.

The systems both use the 8" form factor and the intelligent interfaces previously reserved for storage peripherals on larger systems. Interphase uses the high-performance, high-reliability SMD interface for the RDS 375. With the same SMD interface as many drives and subsystems already on the market, OEMs and integrators are working with a known quantity.

Priam has developed the SmartT interface for their combined disk/tape subsystems. The board, also designated DSI01, includes a 16-bit microprocessor and buffer memory. But OEMs desiring a standard peripheral interface to the system are not excepted from using Priam systems. At the same time as their introduction of the IBM and Apple interfaces for the DataTower, Priam announced support of the SCSI and high performance IPI standard interfaces. For combined tape and disk control as needed for the DataTower, the IPI would be the logical choice for a standard interface.

Many users are making use of the power of multiple PCs in a network, and Interphase points out that large capacity



Interphase incorporates fixed and removable storage, for 75 Mbytes total, in the RDS 375.

disk subsystems like these can be used for file servers in local area networks of microcomputers. The primary advantage these 8" systems have over the 5 1/4" storage systems traditionally used with PCs is speed. Priam claims 35 msec average access on the DataTower and Interphase systems offer 30 msec average access.

Both systems use voice coil actuators and include error correction, like Winchester systems traditionally offered for large computer systems. The Interphase RDS 375, like lower-capacity RDS series

storage peripherals for the IBM PC and compatibles, is a desktop unit. The Priam DataTowers are all standalone units. These versions are \$8,995 in single quantities. List price for the RDS 375 is \$9,495, quantity one. Interphase is also offering the SMD controller and prewired subsystem enclosure separately for those who wish to buy disk drives directly from the manufacturer. —Pingry

Priam Write 225
Interphase Write 226

DEPARTMENTS/Boards

PC Clone Boards: More Power At A Smaller Size

The proliferation of software for the IBM PC is inducing systems integrators to design around the PC's hardware. Having development tools, peripherals, and software in nearly all languages, the PC reigns high in functionality and is being seen more in industrial applications.

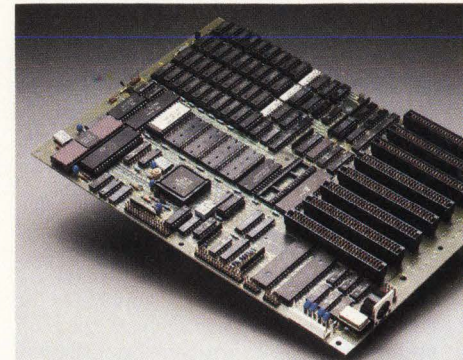
Responding to an ever increasing marketplace, Faraday (Palo Alto, CA) manufactures PC compatible boards for the OEM. Stressing compatibility, Faraday's aim has always been 100% IBM PC compatibility. The original 6400 series, introduced earlier this year, supports PC-DOS, MS-DOS and both concurrent and standard CP/M via the BIOS in EPROM. Adding a disk controller and display controller, systems integrators can attain economical results while retaining complete

compatibility with the PC.

Faraday's newest addition, the FE6420 series, offers even more power at a smaller size. Thanks to three CMOS gate arrays, the multi-layered board size has been reduced to 8.5" x 12", while consuming only 12 watts. The board has eight expansion slots for a wide array of applications, and includes monochrome display on-board. A floppy disk controller is available on all three memory configurations; 64K, 128K and 256K. The 6420 is upgradable to 640K using 256K RAMs. EPROM space is also expanded to 64K supporting 2764, 27128 or 27256s. Not available on the 6400 or 6410 series, the 6420 series has a socket for the 8087 co-processor.

The new board has two serial ports and

The Faraday board offers more I/O slots, an 8087 chip socket and on-board CRT and floppy disk controllers.

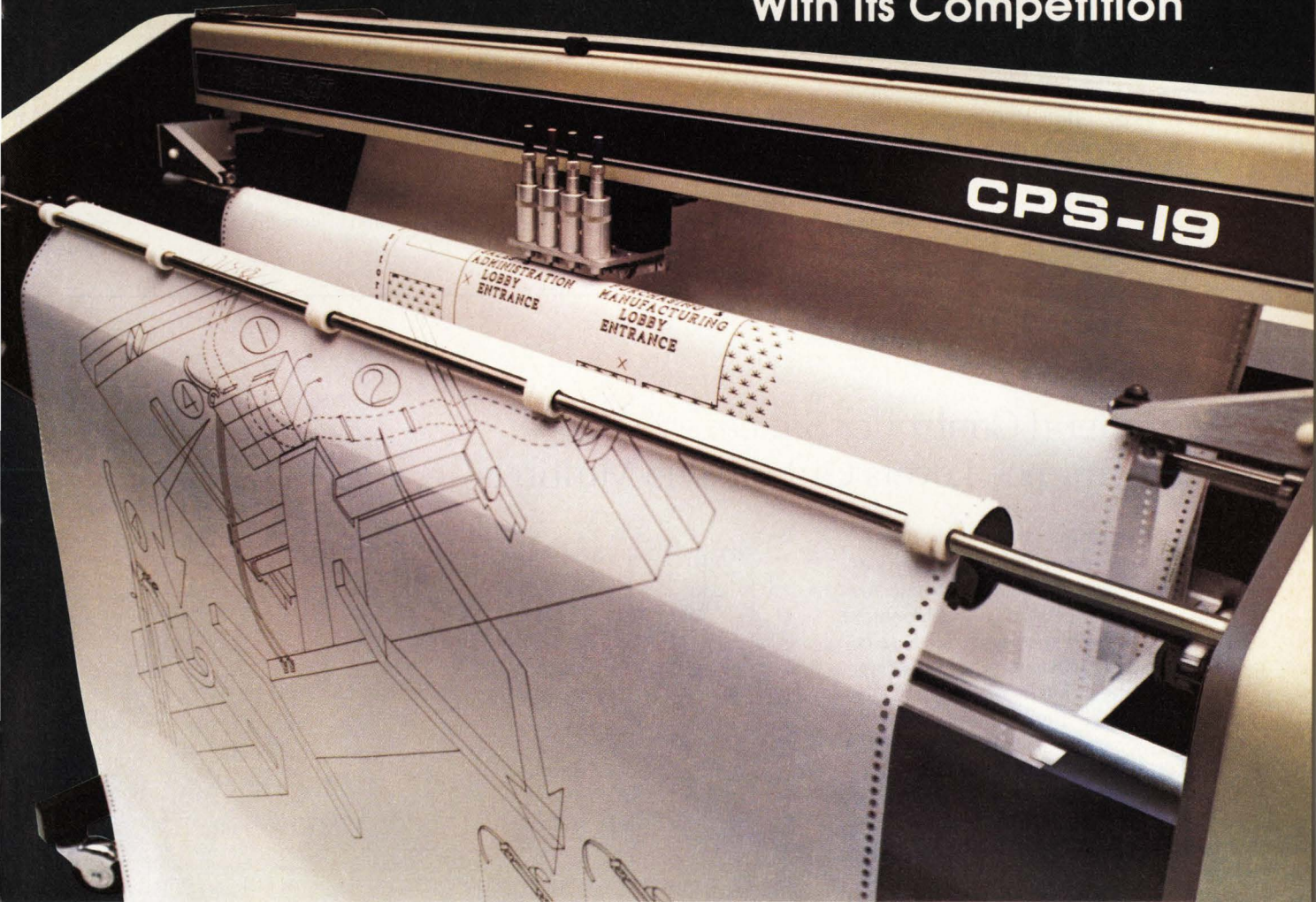


a parallel Centronics port. Fully tested and burned in for industrial use, it comes with a one year warranty.

The gate arrays allow the smaller board space by eliminating 40 chips on the monochrome display alone. The func-

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tions of the three chips are: monochrome display controller, CPU controller, and the floppy disk controller.

Faraday is making a major commitment to OEMs by selling all three gate arrays. The monochrome display controller and the CPU controller come in a 68 pin J-type surface mount chip carrier. The CPU controller is designed to complement the 8088 by providing a keyboard

interface, clock generator, parity generator/checker, and a wait state generator. The monochrome display controller interfaces with the 6845 and provides all video timing and I/O channel synchronizing. Both CMOS chips are second sourced.

The floppy disk controller is a 48-pin CMOS dip. Designed to complement the NEC 765 or Intel 8272 controller chip, the combination provides a complete IBM compatible floppy disk adaptor. It has its own internal crystal oscillator circuit, and complete data separation can be FM or MFM decoded.

As a result of the Faraday board series, new markets are opening up such as terminals, instrumentation, process control, communications, and factory automation. Image analysis, where up to six boards are used, can utilize the full capability of many expansion slots. Without having to re-invent microprocessor design, system integrators and OEMs can take advantage of available software, diagnostics, support and peripherals to integrate a powerful system economically and effectively.

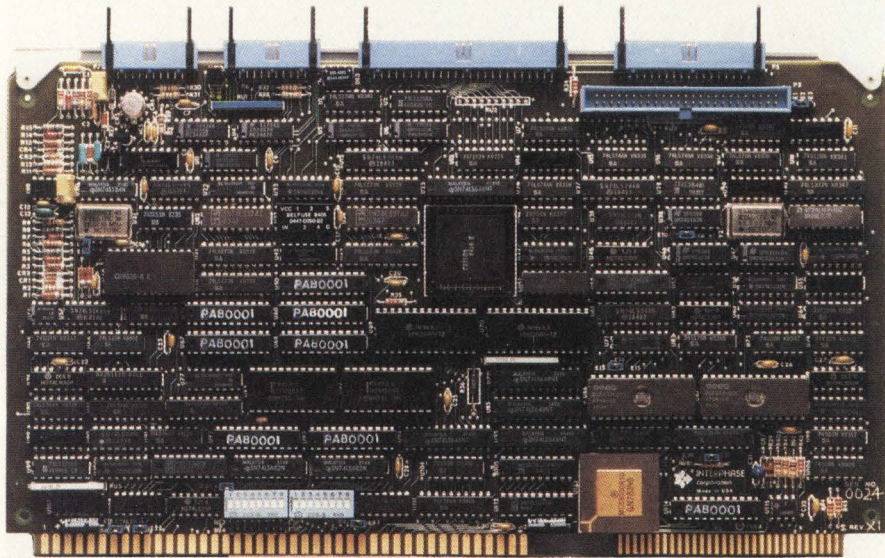
—MacNicol
Write 221

Peripheral Controller Squeezes New Performance Levels Out Of The Multibus

Use of an on-board 68000 microprocessor, two high-speed bipolar state machines and two gate arrays manufactured by Signetics, are the key design base behind the latest disk controller from Interphase Corporation (Dallas, TX). Called the "Storager," it will support up to two 5¼" Winchesters using the ST506, ESDI or ST412HP interfaces. Additionally, it will support up to four quarter inch tapes using either QIC-02 or Archive interfaces and up to two 3½", 5¼" or 8" floppy disks.

The key to the design is its multitasking, virtual buffer architecture. The two bipolar state machines are used to manage the high speed data streams between the controller and the Multibus and between the controller and the peripheral devices. These state machines operate independently, allowing simultaneous data movement between the controller and the bus and between the controller and the peripherals. The 68000 is used to regulate activity on the controller. It breaks up commands and sets up data transfer operations. More important, it manages a pool of virtual buffers. The Storager has on-board 16 Kbytes of memory that can be treated as a series of sector buffers. At any given time individual buffers may be allocated to any of three devices—the disk, the tape or the Multibus. The 68000 will dynamically allocate buffers as they are requested or released by the various devices. Since each device has a seemingly limitless supply of buffers, overrun and underrun problems are eliminated.

With a large pool of buffers available, the controller applies certain techniques



to reduce rotation disk latency. A traditional controller, upon receiving a multi-sector request from the operating system, will wait until it encounters the first requested sector before beginning to read and transfer data. Thus, it will undergo, on the average, a rotational latency equivalent to half a track or eight milliseconds. If the request is for a full track of data, the controller will take a revolution and a half to accomplish the transfer.

The Storager, however, will begin reading data as soon as the head lands and will begin transferring data as soon as it encounters any of the sectors of interest without waiting to rotate around to the beginning of the requested string. Thus, the controller will never take any more than a single revolution to transfer an entire track of data.

A multi-function caching disk/tape Controller, "the Storager" supports ST506 and high performance 5¼" Winchesters for Multibus-based microcomputers.

The buffers also enable the controller to implement an intelligent caching scheme. Once the Storager has completed a read operation and transferred requested data, it will continue to read sequential data into the cache. If operating systems are designed for logically sequential data, the Storager can supply those from the cache without accessing the disk.

Software options supported include all the ESDI specified methods of sector addressing—hard sectoring, address mark and byte clock. It also supports all specified methods of head positioning, including serial cylinder selection and stepper pulses, with software control of step rates to take advantage of drives supporting buffered steps.

—Wilson

Write 219



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For the D-SCAN GR-1104, it's child's play. Because this is

the compact desktop terminal that thinks it costs twice what it does. And acts that way.

Picture this. A 60Hz non-interlaced 14" display. Bright. Stable. And flicker-free. With 1024 x 780 resolution!

But that's just the beginning. The 1104 lets you display 8 colors from a palette of 512 (not the usual 64). And lets you expand display list memory to a full 512K!

All of which means someone is going to be very happy. Visual cueing is better. And picture manipulation is localized. Which, of course, makes operators faster and more productive. And mainframes less burdened. Two cost-efficiencies every company can live with.

The 1104 will even support ANSI 3.64. And give you a VT100 keyboard (with 16 function keys). So there are no re-learning curves to finance.

What's more, the 1104 is Plot 10 compatible. Which means it can emulate the TEK 401X instruction set. And you can save a lot of time and money on software development.

Now for some impressive technology.

The 1104 uses four (not the usual one) graphic display controllers. So figures are drawn, filled and manipulated faster. There's no drag on the system caused by processor or memory overload.

Next, the video formatter is our own custom-LSI design. A gate array (2000 gates) that reduces power consumption and board space. And provides the video speed necessary for output to our high resolution display.

Which, we hasten to add, is beautiful. Especially with its .31mm pitch shadow mask. And contrast enhancement filter that eliminates screen glare and improves visual acuity.

You'll also be happy to note that the 1104 supports our Graphics Tablets (there are two) and Color Hard Copier (the one that's already taking the industry by storm).

One last item. Because we design, build, sell and service all of our products, you can count on getting the back-up you need. Direct service from 13 offices across the U.S.

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You'll see that getting better resolution from a more user-friendly terminal, for a lot less money, really is child's play.



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Write 18 on Reader Inquiry Card

J-11 Microprocessor Designs Offer DEC Compatibility

Designing products based around DEC's J-11 microprocessor can give the OEM some real advantages in the marketplace. Probably the most important of these is the ability to take advantage of the extensive operating system and application software that has been written for the PDP-11 over the years.

That was the philosophy behind the MCP 32/16, a new J-11-based computer system from Argonne Systems (Sugarland, TX). Built around Intel's new Multibus II architecture, the design allows multiple, closely-coupled central processors to run their own operating systems within the same enclosure. A high system performance is achieved by giving each central processor a dedicated execution bus with attached memory. System resources (disk and tape) may be shared or uniquely dedicated to a single central processor at the discretion of the systems integrator.

PDP-11 compatibility is provided by the use of the J-11 on the MCP 32/16 processor card, that also offers PDP-11/70 memory management and FP11 floating-point operations. A storage control processor and I/O processor on the

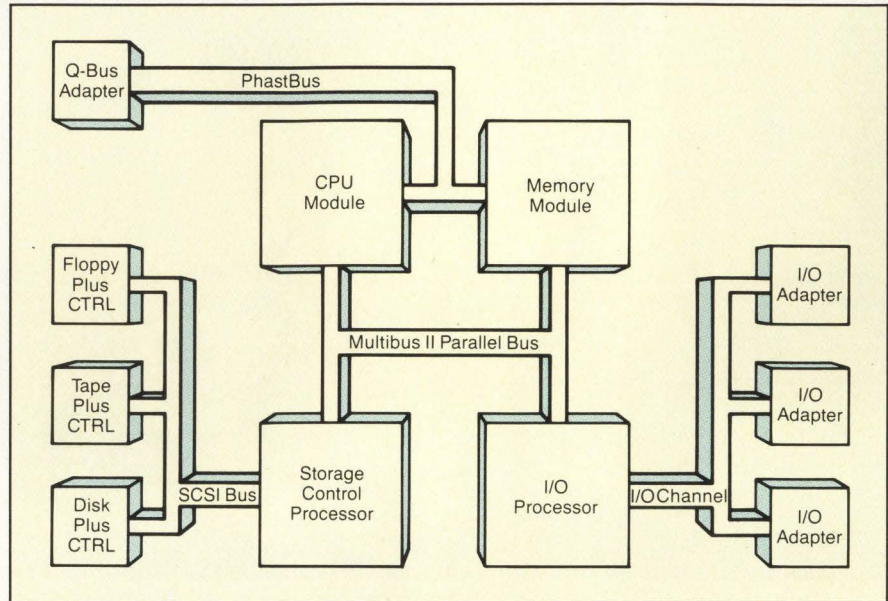


Figure 1: The Argonne system architecture.

Multibus II supply multi-ported interfaces between peripherals and central processors. These auxiliary processors emulate standard DEC interfaces. Sys-

tems can be configured with a combination of peripheral devices: 10 Mbyte Winchester; 10 Mbyte removable disk; dual 5 1/4" floppies and a 20-45 Mbyte cartridge tape.

Within a week of the Argonne announcement, Digital Equipment Corp. (Hudson, MA) unveiled their own system implementation of the J-11 chip set — the micro PDP-11/73. Claimed to be comparable in performance to the PDP-11/44, it may be used as a multiuser personal computer, as a host to personal computers or as a front-end to a larger host, such as a VAX.

Q-bus-based, the new machine features the same enclosure and power requirements as the microPDP-11, avoiding the necessity for OEMs to repack the whole system. It will be offered as a box, as a packaged system or as a system building block.

As well as using the J-11 as a central processing unit, other designs have realized its capability to offload the host in a co-processing environment. MDB Systems (Orange, CA), for example,

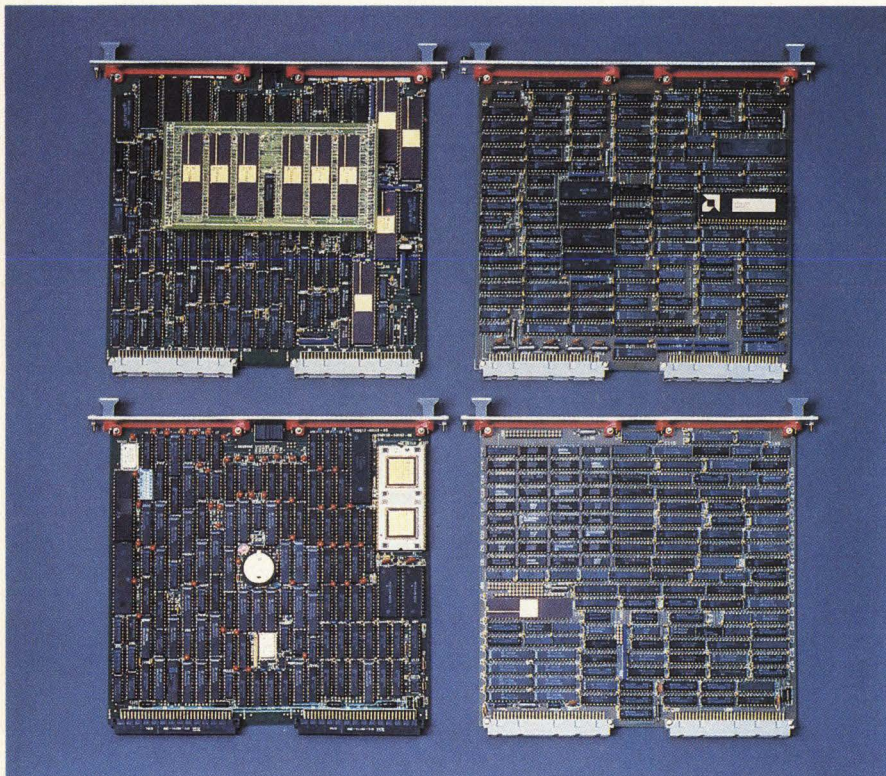
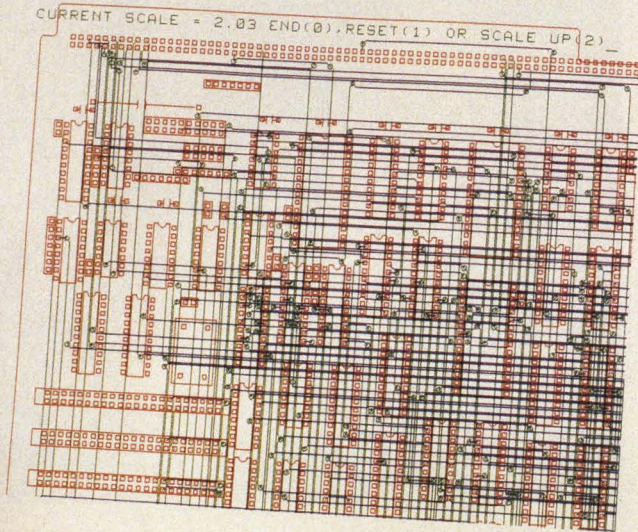
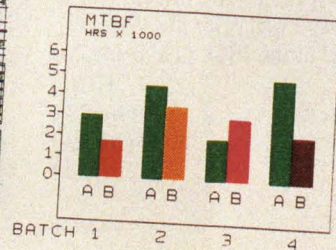


Figure 2: These four Multibus II boards form the heart of the Argonne system.



- * PROBLEM AREA
- * MTBF
- * COST TO REPAIR



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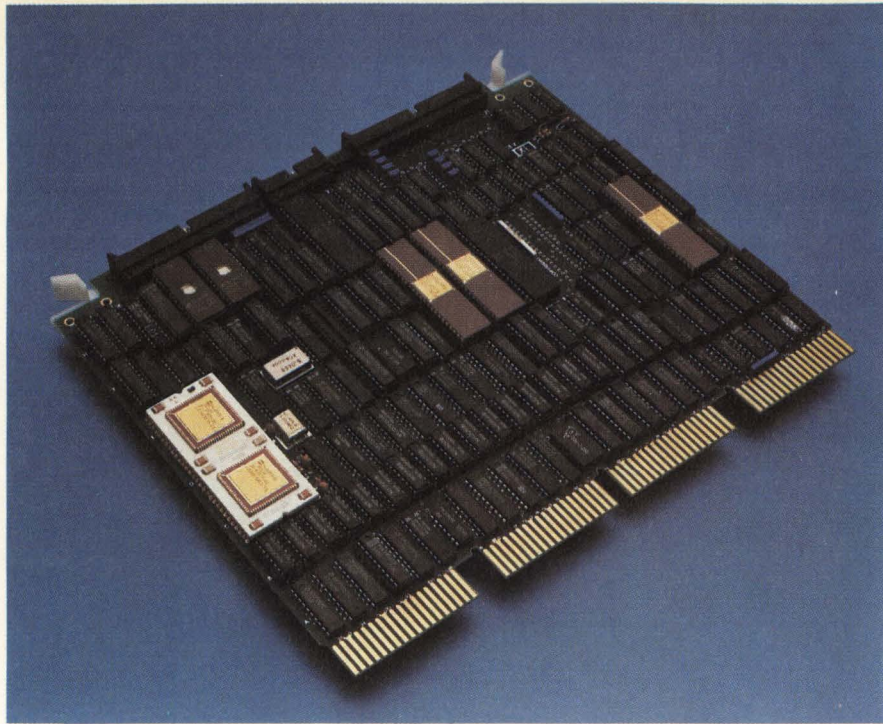
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recently announced a J-11 based front-end processor that features an on-board 512 Kbytes of dual-ported memory, two high-speed serial ports and an external parallel I/O bus. Dubbed the MLSI-JFEP11, it is expected to find applications in data compression/decompression, message processing and routing and protocol conversion. The announcement marks a departure for MDB who intends to move into the subsystems marketplace.

The availability of the J-11 processor will continue to allow designers to build powerful DEC compatible board level and systems products. It will be interesting to see if DEC will offer the VAX chip sets discussed at the ISSCC in a similar way.

— Wilson

Argonne Systems Write 232
 MDB Systems Write 233
 DEC Write 234



NEC, Zilog To Market V Series Microprocessors

Following a March agreement granting NEC a second source license for Zilog's Z80,000, the two companies have signed another license giving Zilog non-exclusive rights to worldwide manufacture and marketing of NEC's V Series of 8-, 16- and 32-bit microprocessors and peripherals. The V Series includes two families

of CMOS microprocessors, the standard micro μ COM-70K family of 8- and 16-bit devices, and the supermicro μ COM700K family of 16- and 32-bit devices.

The first two V Series devices will belong to the standard micro family. The 8-bit μ PD70108C has an 8-bit external bus and a 16-bit internal bus. The 16-bit ma-

chine, the μ PD70116C has a true 16-bit internal and external bus.

To reduce the number of processing steps for instruction execution, a dual data bus method has been adopted for the μ PD70108. The two data buses (the main data bus and the subdata bus) are both 16 bits wide. For addition/subtraction, logical, and comparison operations, processing time has been increased some 30% over single bus systems. Dedicated hardware for memory access related operations is built in. Called an effective address generator, the circuit is reserved only for calculating effective addresses and requires only two clock cycles for addresses to be generated in any addressing mode.

Both the processor's program counter (PC) and the prefetch pointer (PFP) functions are provided in hardware. A time saving of several clock cycles is realized for branch, call, return, and break instruction execution compared with microprocessors that have only one instruction pointer.

The 70108 is object code, but not microcode compatible with the Intel 8088. New instructions include bit field manipulation instruction, packed BCD opera-

	μ PD70108C	μ PD70116C
Process	CMOS	
Transistor Counts	63K	
Number of Instructions	101	
Minimum Instruction Execution Time	400 ns / 5 MHz	
High Speed Multiply/Divide Instruction Execution Time	6 to 8 μ s / 5 MHz	
Memory Addressing Space	1 M Bytes	
Instructions With Special Features	Bit Field Manipulation Instructions	
	Bite Manipulation Instructions	
	Packed BCD Operations	
	Array Boundary Check Instruction Stack Frame Generation/Deletion Instruction	
Emulation Capability	8080AF Instruction Set	
Standby Function	Yes	
Data Bus Width	internal	16 bits
	external	8 bits
Power Supply	5 volts	
Power Consumption	500 mW (in operation mode)	
	50 mW (in standby mode)	
Package	40-Pin Plastic DIP	

Table 1: Features of the 70108 and the 70116.

TeleVideo corrects the VT220 key mistakes.

The new TeleVideo® 922 shares but one feature with the VT220®: full DEC®-compatibility. The similarity ends there.

1. Take our keyboard, for example. The

RETURN key is within direct, easy reach. But VT220 users must stretch over an additional key to hit RETURN. Or have the hands of a concert pianist.



DEC VT220

2. Our ESCAPE key is located above the TAB key, right where you'd expect to find it.

Theirs isn't.

In fact, you have to go hunt for the VT220 ESCAPE key halfway across the row of function keys.

3. Take a look below

at the 922 keyboard. That's a true accounting keypad, complete with a Clear Entry, Double Zero and a TAB key. Not merely the numeric keys you get with the VT220.

4. Our SHIFT key is exactly where it should be, so it does exactly what it should do—shift. Their SHIFT key is shoved over by the < and > key to create lots of < and > on the CRT. Of course with a little practice, you could re-learn their keyboard. But why, now that you've seen our 922?

Moving The Shift Key Is A Mistake.

922 Display Screen.

<oving <he <hift Key <s A <istake.

VT220 Display Screen.

5. And after we built a better keyboard, we built a better terminal. With exceptional reliability. Quality. Advanced ergonomics. Everything you'd expect from the industry ANSI leader.

The new 922 is available now and priced to move now. And it's backed by a worldwide sales and support network. Which means doing business with TeleVideo is yet another key difference.

6. Here are 6 more advantages to the 922.

	TeleVideo 922	DEC VT220
Programmable Function Keys	15 (30 with shift)	15 (shifted only)
True Accountant Keypad	YES	NO
Plug-in Graphics Upgrade Option	YES	NO
Non-glare, Green Phosphor Screen	YES	NO
Full Tilt & Swivel	YES	NO
Enhanced ANSI Mode	YES	NO

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In California, call 408-745-7760.

The TeleVideo® 922

• TeleVideo Systems, Inc.

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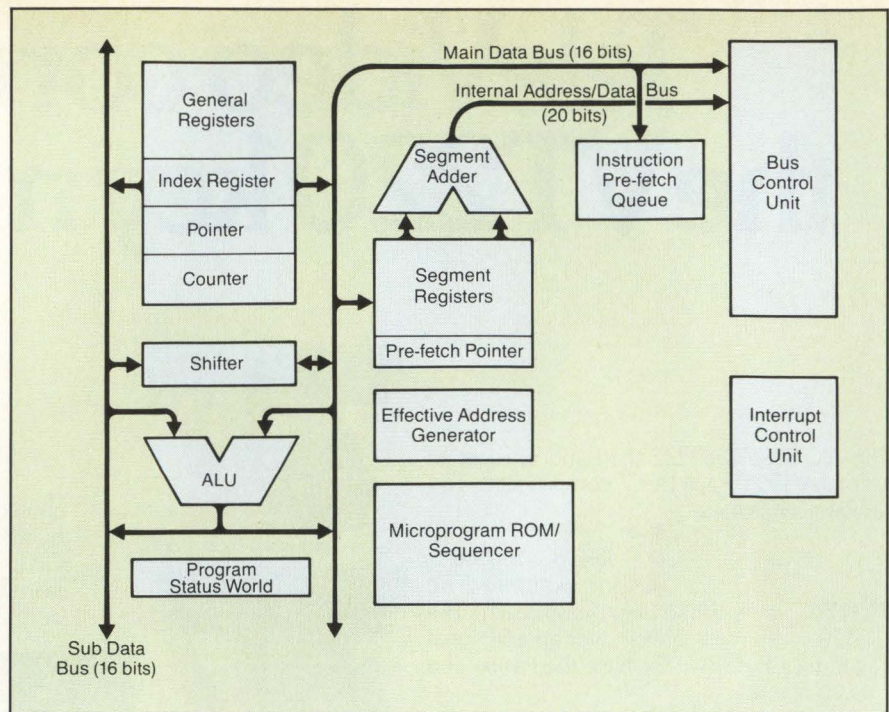
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Figure 1: Architecture of the 70108 and the 70116.

tion instructions, and bit manipulation instructions. The latter is effective for graphic operations such as video data processing for bit map displays. In addition, such instructions as an array boundary check and stack frame generation/deletion are also in place to support high level languages.

A 32-bit microprocessor (V70) version of the supermicro μ COM-700K family is currently under development. According to NEC, it will be a VLSI device integrating about 700,000 transistors and will be designed using a five pattern CMOS process with 16 micron channel lengths.

—Wilson
Write 220



DEPARTMENTS/Communications

IBM's Statement On Communications Rouses LAN Activity

From the beginning of the work on standards for local area networks, IBM has made their interest in token passing ring architectures clear. This spring, the Information Systems Group (Rye Brook, NY) finally announced an IBM cabling system (not a network, but a cable scheme that might allow token passing). As part of this release on the cabling system, they suggested that the token passing 802.5-style ring LAN is still two to three years off. In addition, "IBM Industrial Communications Direction," calling for token passing bus networks in the industrial environment, was published by the Industrial Systems Division (Boca Raton, FL).

IBM's stance of waiting on the office/campus network hasn't kept other companies from working on token ring networking. Proteon (Natick, MA), for example, has long based their popular proNET system on a baseband token-passing ring. The cabling system that IBM did announce is similar to Proteon's physical configuration. Both the IBM cabling system and proNET provide a logical ring in a physical star configura-

tion or daisy-chained stars. (Figure 1). A single distribution closet or wiring center, as Proteon calls it, houses all of the facilities for rearranging network nodes.

The IBM in-building cabling system uses a distribution panel in the hub closet that can be connected to as many as 64 twisted pair cables. These low-cost cables are permanently wired from wall outlets throughout a building and into closets for connection. Moving a device from one office to another requires only unplugging from one wall socket and into another and moving a patch cable at the panel; not total rewiring. Though the twisted pair cable is generally lower performance than coaxial or other LAN cable, quality is sufficient for PBX and telephone systems from major manufacturers to operate at full speed. In conjunction with ease of device reconfiguration, the cable system can be relatively low cost.

Cabling systems from IBM are to be available in October, with prices for four types of cable, faceplates for wall outlets, voice and data connectors, distribution panels and device interface equipment

already announced. The interconnection of distribution boxes is specified for either twisted pair or fiber optic cable.

In the wake of the publication of IBM's cabling system specs, Ungermann-Bass (Santa Clara, CA), one of the longest-established turnkey LAN suppliers, announced that they will provide a network to operate on it. They feel that by providing for both voice-grade and data-grade twisted pair, IBM is endorsing PBXs and LANs side-by-side in the office. The Ungermann-Bass Net/One has long been available on baseband, broadband and optical fiber cable; now they will add twisted-pair copper, as well.

What may be an even more significant direction for IBM is the industrial emphasis. The new Industrial Systems Division is not slacking off. At the Programmable Controllers show in Houston, IBM was present in force; they announced a ruggedized version of the PC/XT, the 5531, industrial software to connect to the four major programmable controller manufacturers' products to the Series/1, and also showed a Multimedia Plant Floor Terminal.

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SPECTRA 25 fully emulates DEC's RM02/5 and RM80 disk subsystems, and TS11 tape subsystem. It can run two SMD disk drives and four tape drives, in any combination. Plus an E²PROM lets you easily reconfigure while the controller is in your system.

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It could be all the controller you'll ever need. For further information on our expanding family of controllers for DEC Q-BUS and UNIBUS® computers, call or write us today.

	SPECTRA 15*/ SPECTRA 25	SPECTRA 111*/ SPECTRA 121	SPECTRA 12*/ SPECTRA 21
BUS	Q-BUS (Block-mode)	UNIBUS	UNIBUS
Disc Emulation	RM02/05, RM80, RP06 (2 drives)	RM02/05, RM80, RP06 (4 drives)	RK06/07 (4 drives)
Tape Emulation	TS11 (4 drives)	TS11 (4 drives)	TS11, TM11 (4, 8 drives)
Disc Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Configurable On-Line	Yes	Yes	No
*Single function disk controller			

Spectra Logic Corporation, 1227 Innsbruck Drive, Sunnyvale, CA 94089, (408) 744-0930, TWX 910-339-9566, TELEX 172524 SPL SUVL. International Sales Office: The Netherlands (31) 23 273744, TELEX 71080 SPECL.

SPECTRA LOGIC

The Multifunction Controller Company.

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Their industrial plans for communications include networking, specifically token passing broadband bus to the IEEE 802.4 standard. This is the same choice General Motors has made for their MAPS network, demonstrated at the NCC this summer (*Digital Design*, June, 1984). Broadband cabling is sensible for the industrial environment; it permits mixing of LAN information with the video common for monitoring and, in fact, many factories have broadband cable already installed.

Since both the industrial and the office communications systems from IBM allow multiple-vendors to be connected, the fact that IBM is the originator will have a big impact on LAN and linking schemes throughout the industry. Because IBM has not announced LAN products for the office environment, but only a cabling scheme with voice and data wires, Ethernet will continue to hold market and momentum for the office. More companies will work on token-passing networks, and IBM, in the rapidly awakening industrial market, will set communications standards with products in a range of specifically industrial configurations.

— Pingry

- IBM Information Systems . . . Write 228
- IBM Industrial Systems Div. Write 229
- Proteon Write 230
- Ungermann-Bass Write 231

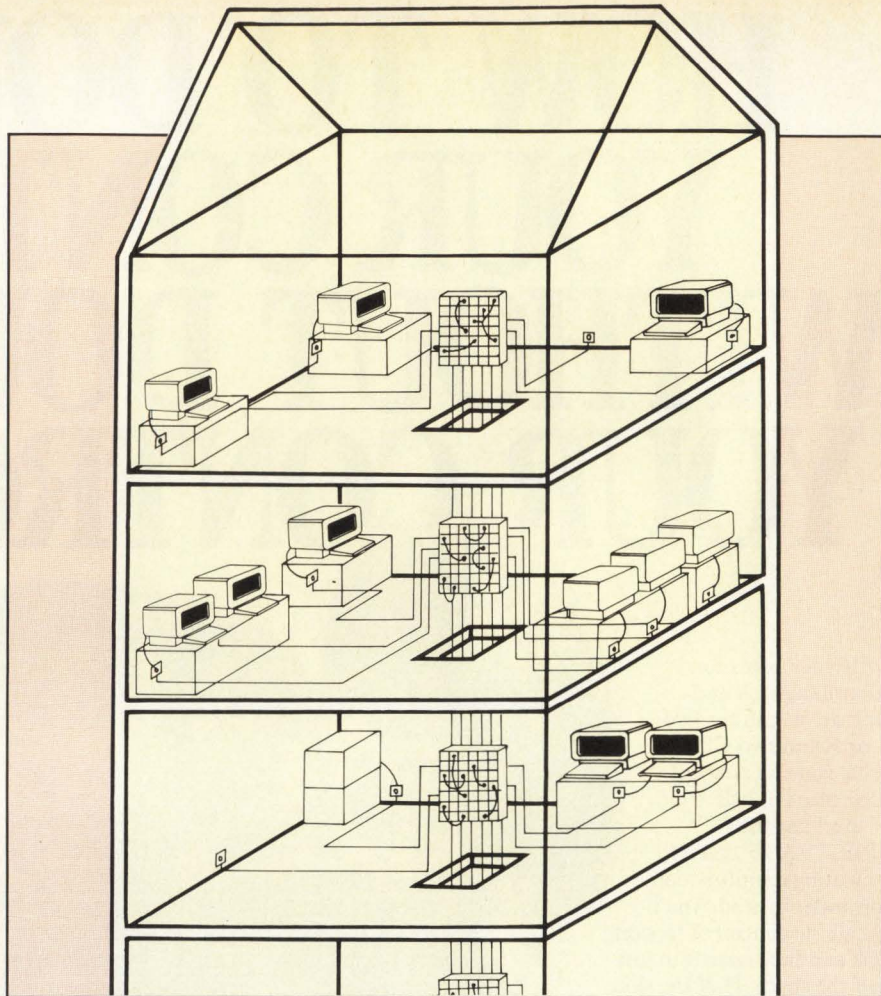


Figure 1: IBM's single cabling system can be used instead of coaxial, twinaxial, twisted pair and other special purpose cabling. The diagram shows terminals connected to wall outlets which, in turn, are connected to distribution panels mounted in wiring closets. Computers and devices can be connected by using patch cables on the panel. Wiring closets in the same building or different buildings on a campus can be connected.

Global Digital Network Gets Silicon Development Commitments

Components are finally in development for interfaces to a global information network. Seven semiconductor manufacturers and three telecommunications system firms have announced their intention to create products compatible with evolving Integrated Services Digital Network (ISDN) standards.

The Consultative Committee for International Telephone & Telegraph (CCITT) and ISO have been working on standards for this end-to-end digital facility since 1981. The goal is for ISDN to be a global standard for all information transport, including data, voice and other user facilities like videotext and broadcast services, as well as monitoring and control.

This spring, Intel (Chandler, AZ), Harris (Palm Bay, FL), Texas Instruments (Richardson, TX), Siemens (Munich, West Germany), Matra Harris (Nantes, France), Philips (Eindhoven, Netherlands) and SGS (Phoenix, AZ) voiced their commitment to producing chips for the ISDN architecture. All of the manufacturers are working on ICs for various functions of the equipment for both digital and analog services. SGS and Harris are developing the SLIC (Subscriber Line Interface) chips for the PBX-like customer site equipment. Intel has published an architectural overview of their Line Card Controller and Feature Control Combo Codec.

ISDN user interfaces to the digital lines

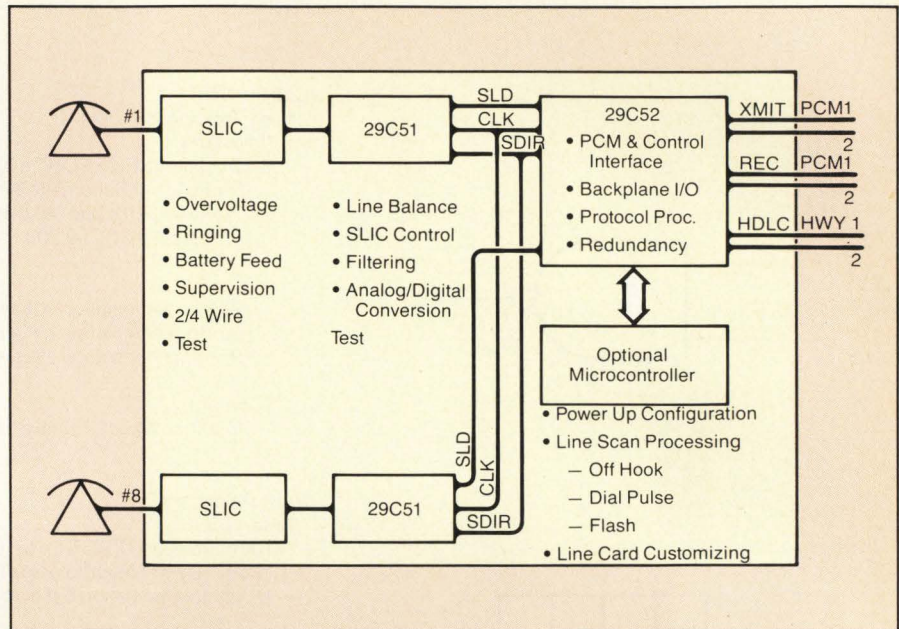
of the network will use a serial bus backplane architecture. Both analog and digital line cards to interface to the bus will be developed. Intel's schematic of an analog line card using their parts (**Figure 1**) shows a generalized configuration.

The work on ISDN is also supported by telephone system makers CIT-Alcatel (Paris, France), Siemens and Ericsson (Stockholm, Sweden). The cooperation of several sectors will be critical in developing a network appropriate to all users and suppliers. In work planned to span the next two decades, users, national governments and international communications and standards organizations should all be involved in setting ISDN specifications.

Figure 1: An analog line card for the ISDN serial bus backplane using Intel's iATC 29C52 Line Card Controller and iATC 29C51 Feature Control Combo.

National governments are particularly important, since except in the U.S., they control telecommunications services. The difference in who controls services has created two views of ISDN up to this point. The U.S. view of a "digital pipe" is narrower than the European "lake," which includes processing and storage as well as transportation of information. Current agreements from many sectors promise global compatibility, despite this discrepancy. ISDN will be a data and information network available to all users for any mix of current and future information services.

—Pingry



DEPARTMENTS/CAD/CAM

An Evolving Design Data Standard

The wide variety of available CAD/CAE systems combined with the expanding semi-custom IC industry has created the need for a standard format to exchange design information.

Presently, few standards exist that meet the needs of all types of design data. As a result, passing information from one software or hardware tool to another is not a trivial task.

Most interchange formats currently used suffer from any one of several drawbacks. One of the major problems is that many formats have been developed to address only specific types of design data. For instance, a particular format might be quite useful for netlist information but unusable for mask artwork. None have addressed the entire scope of the problem.

Although some formats may exist to include all types of design data, they are proprietary to a particular semiconductor or CAD manufacturer.

Also, as IC design methods evolve, new parameters must be added to the data. However, most current formats are not flexible enough to permit this growth.

During the past few years, several interchange formats have been developed, each addressing one or more of the drawbacks mentioned. These efforts were started to combat the mounting design data standardization problems.

The Electronic Design Interchange Format (EDIF) is one format that seems to be gaining respect as a possible industry standard for design data communication. The current EDIF effort was begun by the principles involved in four of these early development projects. It includes the best features of each, thereby providing a single more powerful format. Organizations involved in the current effort are: Daisy Systems, Mentor Graphics, Motorola, National Semiconductor, Tektronix and Texas Instruments.

EDIF version 1.0 is aimed at facilitating the exchange of design information for semi-custom IC designs (gate arrays and standard cells) in a multivendor environment. This will allow semi-custom IC customers to use any vendor's fabrication facilities or front end resources even if the task was begun on another vendor's

equipment.

It is important to note that EDIF is a format for the transmission of design data. It is neither a programming language nor a database system. An EDIF description is expressed in a hierarchy, abstract at its top level, becoming progressively more detailed at the lower levels. This allows the user to confront only the necessary amount of information for the particular task at hand.

The syntax of this format is similar to the Lisp programming language in which all data are represented as symbolic expressions. The basic building of EDIF are primitive data such as strings, signals, ports, layers, numbers and modifiers. More complex structures are built by parenthesized lists that contain either these primitive data or other lists. Often, the first element of a list is a keyword. It is reserved by the language definition to provide meaning to the subsequent elements, based on their position in the list. New keywords can be added, responding to changing demand without requiring changes to existing parsers. By ignoring

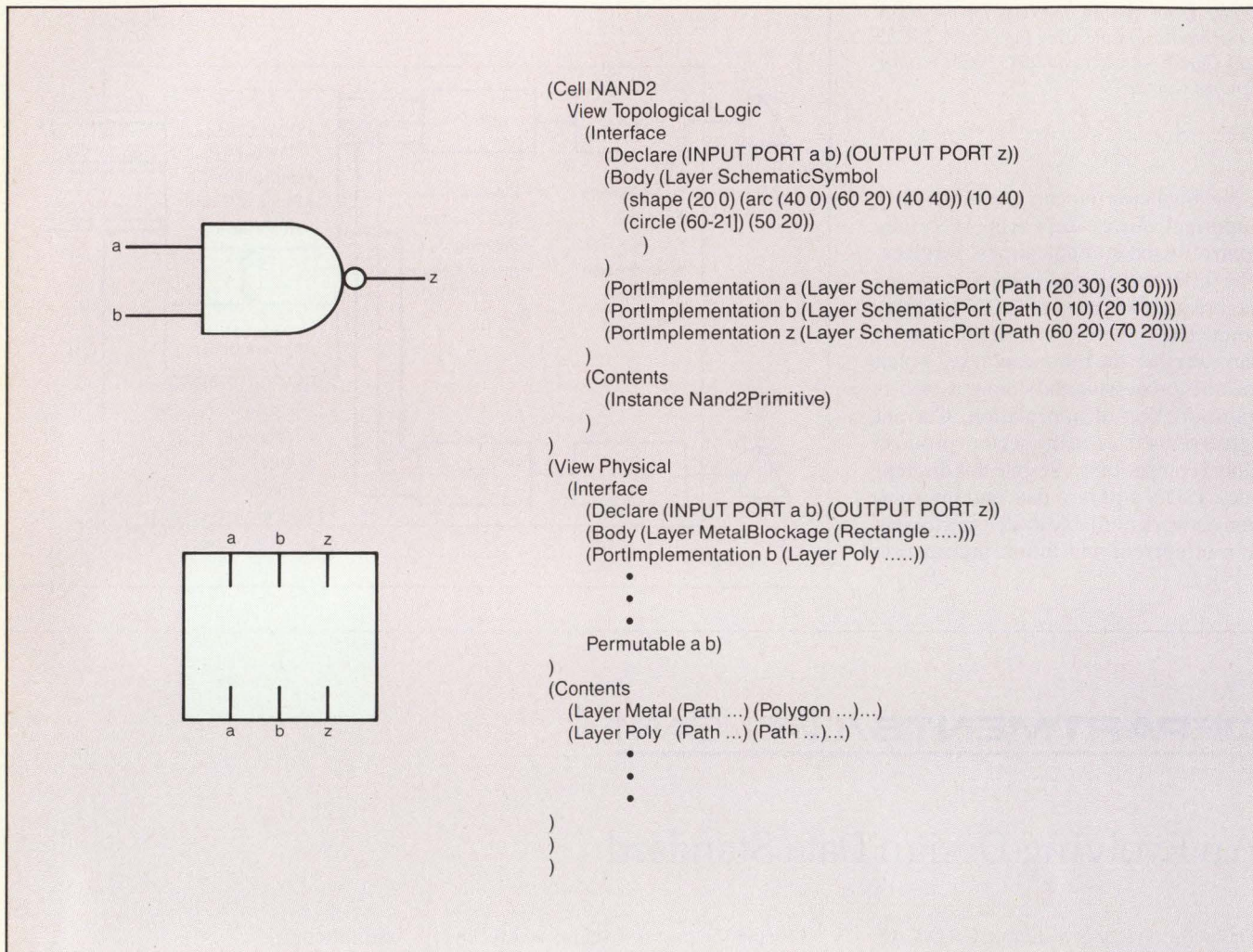


Figure 1: Shown, using the EDIF format, is a dual two-input NAND gate cell. Included in the description is the logic model, schematic symbol, detailed layout, and layout abstraction for placement and routing.

unrecognized keywords, old parsers may continue to extract their information, while new parsers may utilize additional information contained by an extended format.

Several different kinds of design data can be exchanged using EDIF. Some of

the more common types include: logic models, circuit models, macrocell layout, layout abstractions, schematic symbols, base arrays, detailed layouts and netlists (Figure 1).

One area where this format is lacking concerns behavioral descriptions which

is one of the most difficult aspects of standardization. This and many other areas are currently under development by the six vendors mentioned earlier. The current version of EDIF is not a panacea, however, it does represent a big step forward. — Collett

Hardware Logic Simulator Decreases Simulation Execution Time

With the capabilities to integrate hundreds of thousands of transistors on a single chip, and incorporate many of these chips within a single system, IC fabrication process technology continues to tax the CAD/CAE tools that facilitate

system design. Of the many tools currently used in the design cycle, logic simulation is probably the most important bridge between design and verification.

Until recently, logic simulation was performed using software based simula-

tors such as Calma's TEGAS, running on a mainframe. For early design efforts, that had low gate counts, these simulators served very well. However, as in many expanding areas of technology, these simulators are having great difficulty

keeping pace with the demands of simulating today's VLSI based systems. For example, a large design simulated with a software based simulator, running on a VAX or IBM mainframe, might take from 6 to 30 hours to finish. To most OEMs striving to introduce a product within a narrow market window, these lengthy execution times are unacceptable.

Realizing that rapid execution of logic simulation is crucial to effectively implement a design, Zycad (Arden Hills, MN) has attacked the problem "head-on" by introducing one of the most useful tools on the market — the Logic Evaluator. This logic simulation system, introduced just over a year ago, has proven itself as a viable solution for rapid execution of logic simulations.

The Logic Evaluator (LE-1000 series) eliminates the speed problem found with software based simulators by implementing traditional software simulation algorithms in hardware. In addition, the system is easily upgradable so that users purchasing a low-end model can increase its capabilities as the simulation problems get more complex.

Unlike many design verification tasks, logic simulation is not mathematically intensive. Memory access speed and large memory requirements are the demanding aspects of logic simulation. Most software based simulators take approximately 500 instructions to simulate a logic event. An event is defined as a change in the output of a 3-input gate (or logic element such as a flip-flop), and the associated fanout change on the inputs of the next level of gates (Figure 1). Executing 500 instructions for each event taking place in a VLSI system requires excessive amounts of time. Zycad's Logic Evaluator, however, does not rely on these software instructions to simulate logic; these simulation instructions are implemented completely in hardware. Each of the algorithms implemented in hardware uses a dedicated processor that is directly linked to a separate large block of high speed solid state memory (Figure 2). Each of the processors are linked in a pipeline so that new data is continuously processed.

When benchmarked, a small simulation running under TEGAS on a VAX took 10 minutes. The same simulation running on the Logic Evaluator took 0.8 seconds. The Logic Evaluator can execute close to 16 million events/sec when used with all 16 possible modules.

— Collett
Write 227

Figure 1: This logic diagram defines an event on Zycad's hardware simulator. Input c is changed; the changes in state at the output of the 3-input AND gate d and the changes in state on the fanout inputs (e,f,g,h) represent a single event.

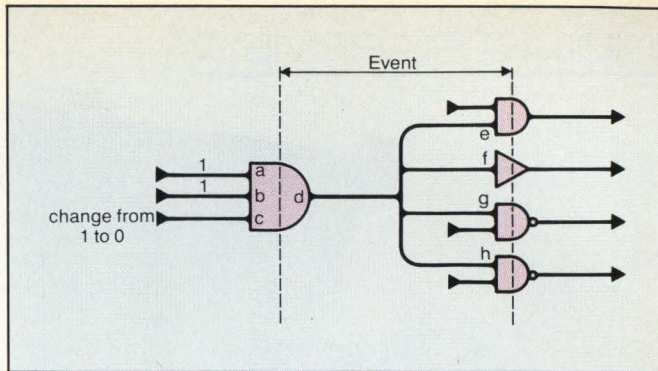
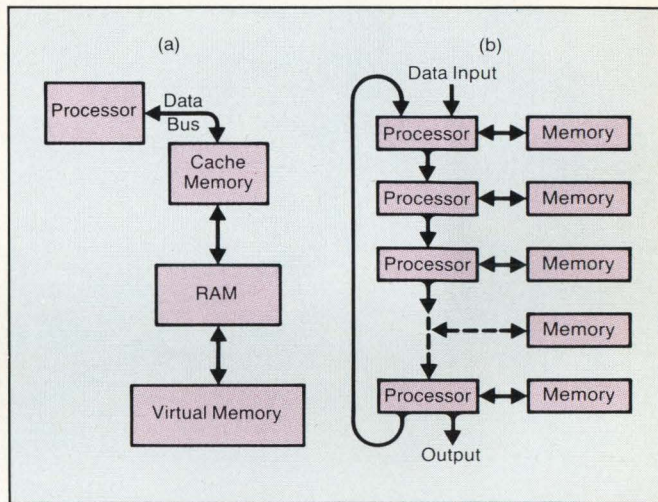


Figure 2: These block diagrams show the difference in architecture between a traditional computer (a) used to run simulation and Zycad's (b) parallel processor Logic Evaluator. Memory bandwidth and size are the two major bottlenecks found in architecture (a). These bottlenecks are completely eliminated in architecture (b).



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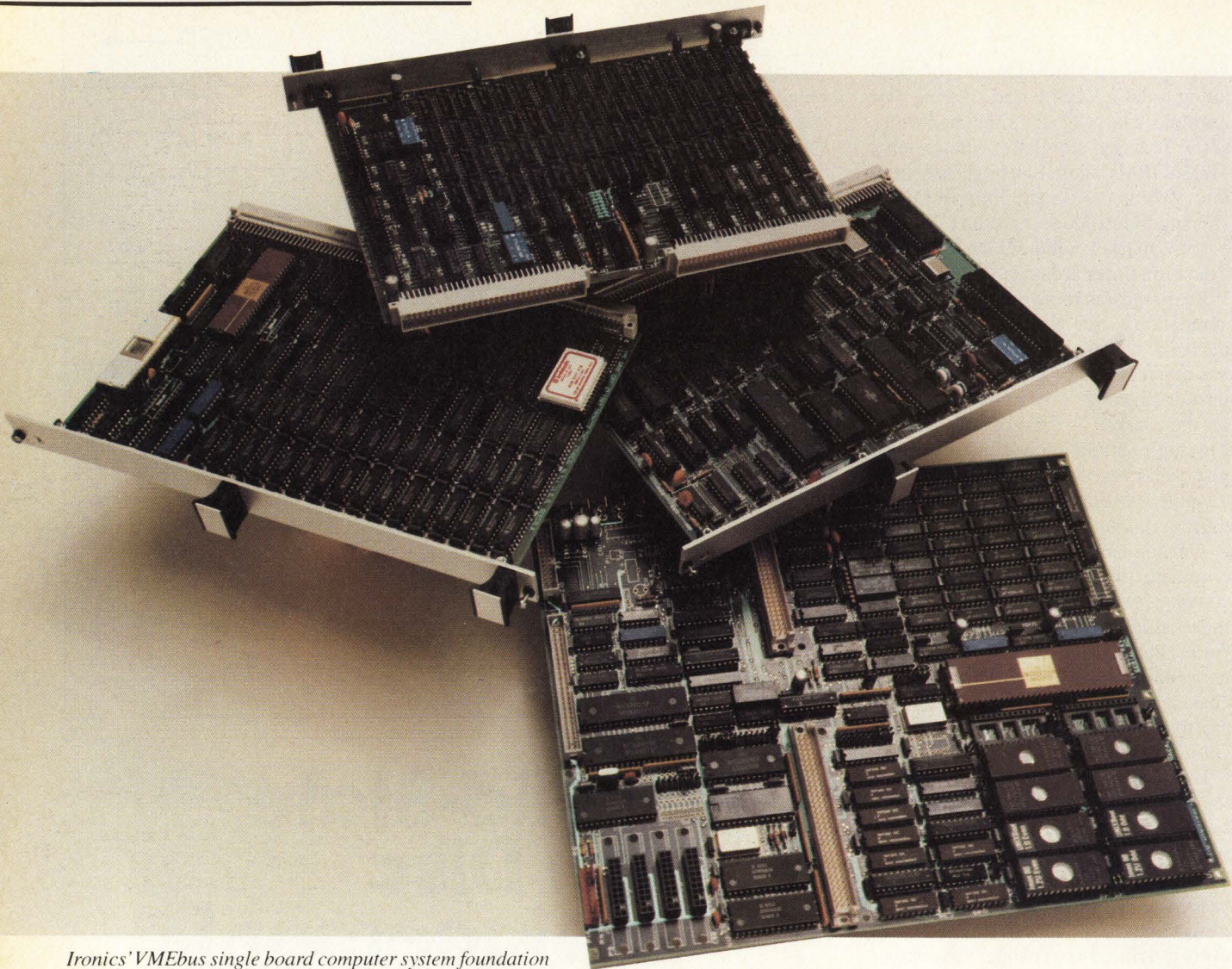
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Ironics' VMEbus single board computer system foundation module; VMEbus 512K/2 Mbyte dynamic RAM; VMEbus graphic display controller; and VMEbus CRT controller.

Building Graphics Systems From The Board Level

by Gregory MacNicol,
West Coast Technical Editor

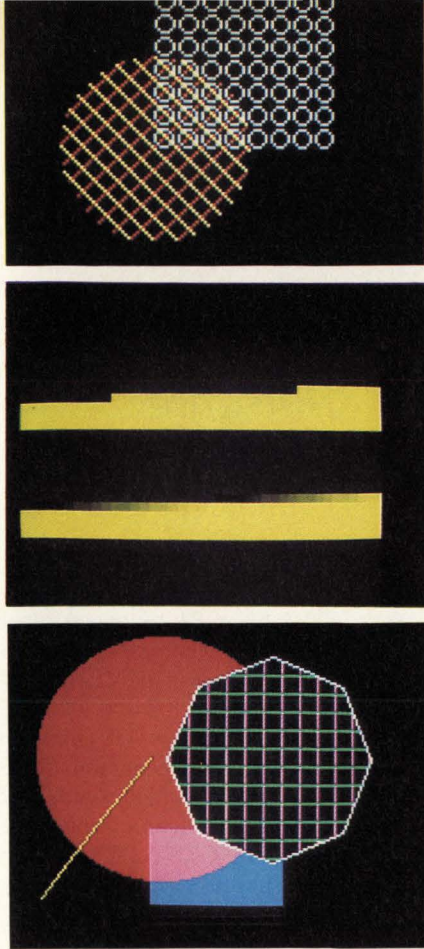
The versatility of the board approach as opposed to building from the chip level in a graphics system is substantiated by its promise of shorter design/production time and potential for better price/performance. More important, if additional colors are desired, for example, or a

faster display at higher resolution is required, upgrading is not difficult.

The graphics processor is driven by virtually any operating system. Further, the availability of any mass memory storage system, I/O, LAN or special terminal drivers may be chosen. Powerful graphics support may also be added with image analysis boards, array processors, and video digitizers. The growing number of

graphics workstations that depend on separate boards on a common bus is evidence of the success of the integrated graphics board approach (**Figure 1**).

The primary criteria for choosing a graphics processor board are resolution, color, display speed and cost. While these qualities are of primary importance in any graphics system, the graphics board integrator is faced with a major



These three examples of solid modeling are from Parallax Graphics. Top: Stippling uses 8×8 pixel patterns to enhance color and aid pattern recognition. Middle: DeJag is used to smooth edges of an image. The top image is without using the DeJag command, the bottom using it. Bottom: High level instructions include four basic drawing commands: polygon, box, circle and vector and form basic drawing modes: solid, stipple, outline and BITBLT.

choice: which system interface bus to use. Six buses dominate the graphics processor arena: the Intel Multibus, the DEC Q-bus and Unibus, the S-100 bus, the VME and STD bus.

On The Multibus

For the industrial and commercial market, VMI (Winooski, VT) offers two graphics processor boards for the Multibus; the VM8850A and the VM8851. Both boards use an 8 MHz 8088 for local intelligence, DMA for fast memory access, and variable display format and depth. They also utilize "Interact," a resident graphics command language in firmware. Interact is a powerful feature providing users with 83 high level and 29 graphics parameters, such as text with multiple fonts, pan, zoom, area fill, run length encoding, clipping and 3-D. Macro capabilities are unique with the firmware, where 256 macros, nesting at 16 levels,

are possible. Control of the maximum 256 displayable colors is through a 4096 palette lookup table.

The more powerful UM8851 draws pixels at 40 nsec to $3 \mu\text{sec}$ per pixel onto a 640×480 or 512×512 , 256 color display. The fast speed is partially due to execution of 8 pixels per CPU cycle in addition to use of Programmable Logic Arrays. A unique feature of the UM8851 is its ability to create large characters without appearing "blocky." A text smoothing algorithm creates proper looking characters at any scale.

VMI provides graphics system support with a video digitizer that interfaces easily with their graphics boards. The UM8830 two-board set accepts $512 \times 512 \times 8$ of RGB data from a camera scanning at 30 lines/sec. The set includes an 8088, firmware, and an ALU for real time functions on one or two buffers of video data. Applications of a fast video digitizer combined with a graphics processor include Landsat image analysis, pattern recognition, and automated inspection.

The never-ending demand for speed has fostered Multibus boards designed around the bit slice AMD29116. The new VG-150 graphics module from Datacube (Peabody, MA) uses the part to interpret and execute a microcoded library of nine commands. The user can also develop proprietary microcode with several tools that include a microcode assembler, compiler, writable control store, option board and a UNIX-based development system. The $1408 \times 1100 \times 1$ pixel display can be moved at a rate of over 1.5 Mpixels/sec. The additional .5 Mpixels of the 2 Mpixels on the board (Figure 3) is used for fast access to symbols, character fonts, complex cursors or any frequently displayed symbol.

Choosing a totally new architecture, Parallax (Sunnyvale, CA) achieves a drawing rate of 12 million pixels/sec. The design is based around four 4-bit ALUs instead of four AMD 2901s. The controller displays 640×480 pixels out of a 512×1024 pixel memory at either 4 or 8 pixels deep. It features a dual-ported video memory, two frame buffers, and RS-170 with genlock.

Genlock is a feature in which external synchronization signals are used to trigger the board's sync signals. This allows synchronization of a display output from a board, with, for example, an external camera.

The real power of the system is con-

The graphics board integrator is faced with a major choice: which system interface bus to use.

tained in the firmware. The 85-command instruction set provides not only the standard list of graphics functions but more useful instructions such as Clear Count Field and Read Count Field. These instructions determine precisely how many fields have elapsed during critical operations. The "Wait For Vertical Retrace" command provides a means of synchronizing operations to the blanking period in the display signal. The boundary fill and interior fill are impressively fast. Another useful instruction allows the capability of selectively drawing specified colors. Especially useful is DeJag, where vectors are anti-aliased. Bit Block Transfer (BITBLT) is becoming a popular function on graphics controllers. With this command any section of any image using opaque and transparent overlays can be copied and repeated elsewhere on the screen.

Focused on the OEM, Matrox (Montreal, Canada) provides all the Multibus boards needed for a complete system including terminals, software and disk drives. Twelve graphics boards are offered from basic display controllers to the GXB-1000, boasting a $2K \times 2K$ read/write display area. The image, 1600×1200 pixels at 4 bits deep, can accept up to 16 image planes. A large 256-instruction command set is interpreted by a 5 MHz 8088, pixel processor, video ECL processor and a hardware vector generator. Matrox also offers a Tektronix 4113 emulation package in C which runs on the MBC-86/12 (8086/8087) CPU board. The package uses a real time kernel which supports multitasking.

It may be useful to fully emulate popular terminal functions on a board. Genisco (Costa Mesa, CA) is primarily a manufacturer of CAD/CAM terminals and sells the $12" \times 16"$ board that drives the G-2200 terminal. The Integrated Graphics Terminal (IGT) board has two graphics processors, four planes of mem-

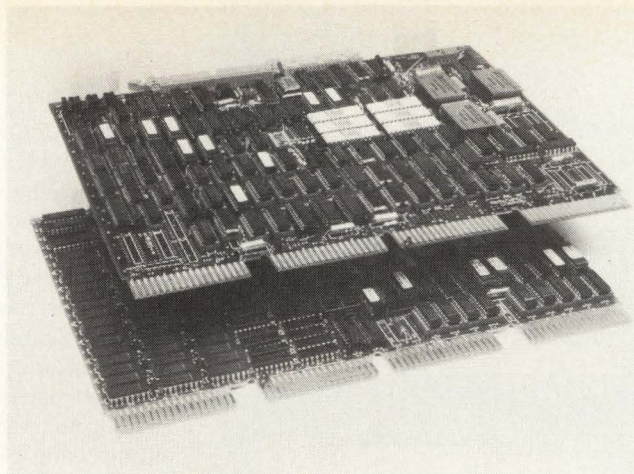
ory, and three I/O ports. Software support is a key factor in choosing a board such as this because interfacing software such as TEMPLATE, ANVIL, DI-3000, or emulating VT-100 terminals is already internally implemented. An OEM can later upgrade the system using the Genisco terminal with no change in software.

A major trend in computer graphics is graphics functionality on a chip. Silicon Graphics (Sunnyvale, CA) and Weitek (Sunnyvale, CA) have developed graphics chips providing major graphics display functions. While Silicon Graphics does not sell their geometry engine, Weitek sells boards in addition to a workstation aimed at the CAD/CAM market.

Weitek sells two products based on the Multibus providing different functions. One board, the Transformation Processor, executes all global graphics functions such as rotation and translation using a 3-D database. It can take high level equations that describe a parametric bi-cubic patch and display the image at 100,000 3-D points/sec. The second product is a two board set they call the Tiling Engine. The Tiling Engine is a fast processor specifically designed for quickly displaying shaded objects using a hidden surface removal algorithm. Through the use of a 24-bit deep z-buffer, objects are given display priority. Each pixel is also given an intensity value. One board contains the z-buffer memory while the other is the actual Tiling Engine. The fast processing is due to on-board 32-bit floating point processing. The three board set includes what Weitek calls a Solid Modeling Engine. While the resultant image cannot be read back after it has been displayed, the fast processing ability easily lends itself to the demands of CAD/CAM, where rotating a smoothly shaded object must be done quickly.

Q-Bus/Unibus

The long history of Digital Equipment Corporation has brought widespread acceptance of the Q-bus and Unibus. A large number of hardware and software developers continue to support these buses, utilizing mainframe power at a reasonable cost. While DEC is focused on developing their VAX line, they haven't abandoned support for the Q-bus



The G-500, Genisco's powerful two-board, quad size frame buffer.

or Unibus. DEC had recently introduced several boards based on the Q-bus and aimed at computational and I/O intensive applications. Additional enhancements such as block mode DMA transfers and 22-bit addressing make the Q-bus competitive with alternative buses.

Peritek (Oakland, CA) has long supported the Q-bus and Unibus with several board level products. Six graphics boards are offered on the Q-bus for monochrome

or color applications. The VCH-Q displays a 512 x 512 x 8 bit-mapped image using a 256 x 24-bit color look up table. The higher resolution of the VRH-Q displays a monochrome 1024 x 1024 display and includes a 64 x 128 character alphanumeric display generator. PALs and IFLs allow the dual-high boards to be compact: 8" x 5". Software support includes a version of GKS, VDI, two levels of graphics subroutines, and an image

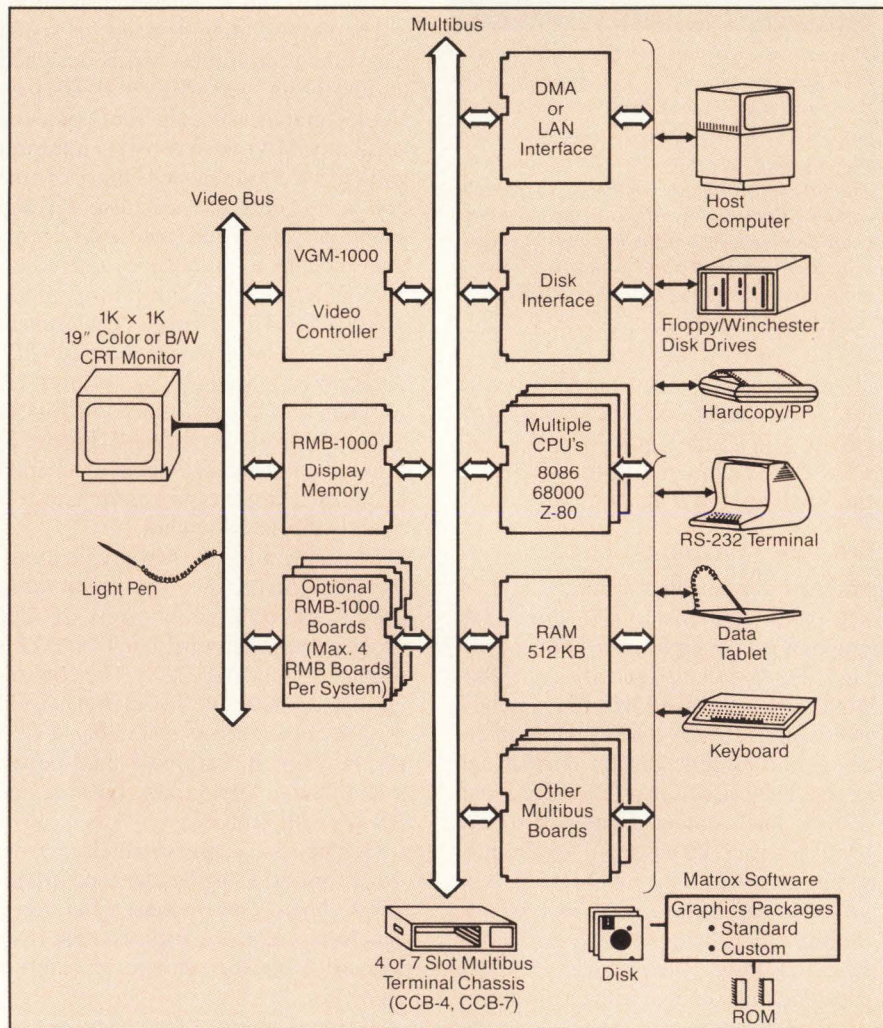


Figure 1: Typical high performance color graphics terminal using Matrox' GXB-1000 complete graphics system.

Vectrix has the graphics system for your next system. Already.

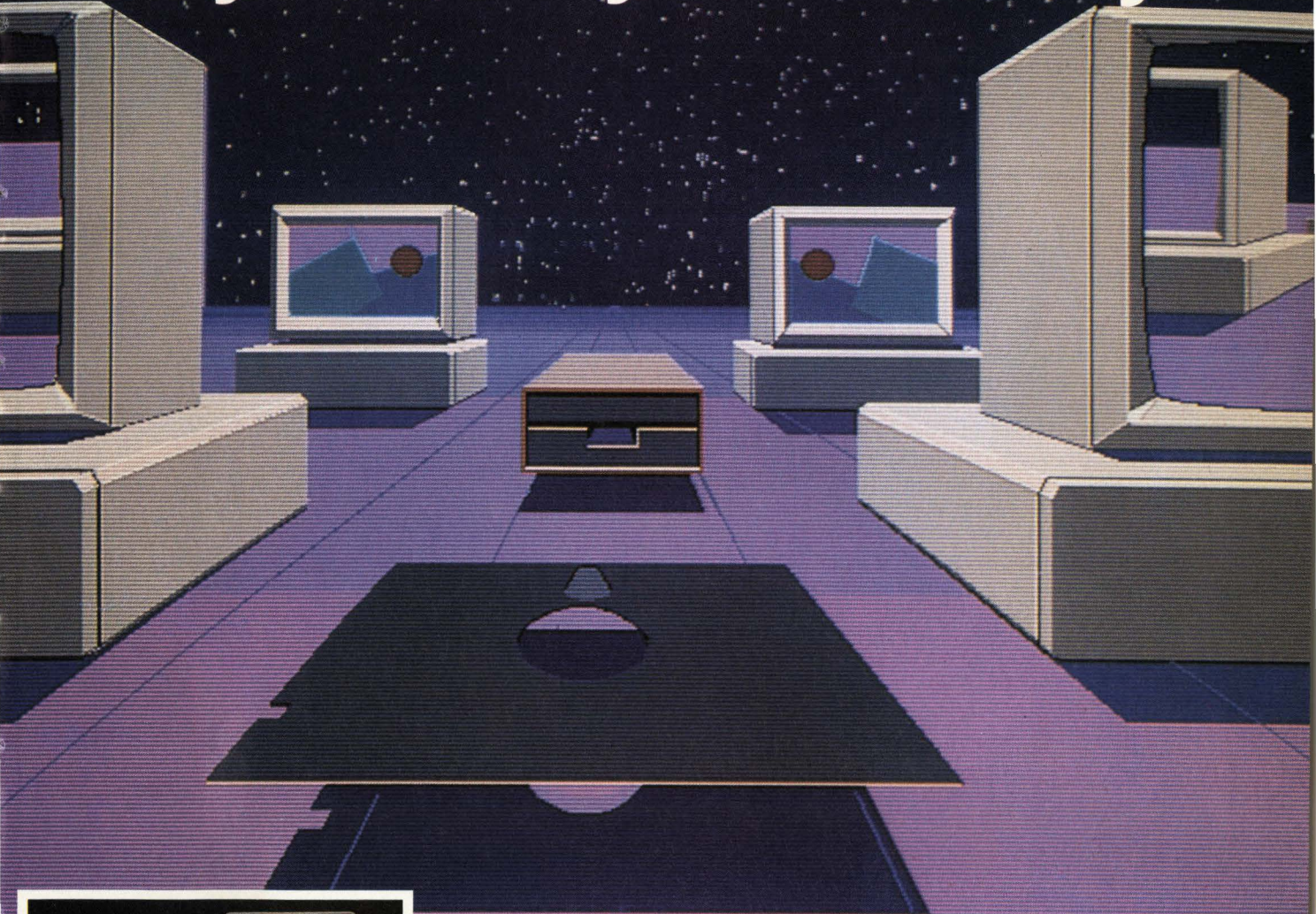


Image created on VX384A which will work with any computer.

For whatever system you're designing there's already an advanced color graphics system to go with it. Either the economical, easy to use VX128A or the versatile VX384A with its 16.8 million color palette and 512 simultaneously viewable colors.

When you add one of the Vectrix Systems to your system you turn your computer into a powerful graphics workstation with a fully integrated graphic command processor, a bit mapped

graphics frame buffer, and a 672 x 480 pixel high resolution flicker-free monitor. Both systems deliver high quality, high performance color graphics. Because the simple command set works with any computer and any programming language, Vectrix makes any system a valuable tool for CAD/CAM, business graphics, medical imaging, video processing, computer assisted instruction, control systems, weather displays, or any of a host of graphics applications in demand.

The Vectrix VX128A and VX384A, part of an expanding line of graphics

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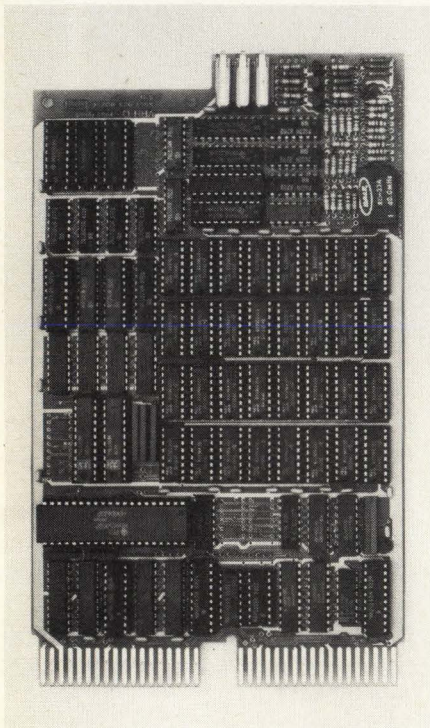
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editor using a mouse.

Riding The 32-Bit Bus

When it comes to greater functionality and power, larger 32-bit machines become a natural choice. However, greater memory addressability and computational power are not the only reasons for the popularity of the larger word size. Newer boards with their display power can utilize software already written for advanced graphics applications. CAD/CAM, animation and image analysis programs are easily interfaced with graphics boards having large instruction sets. Also, support tools, multitasking operating systems, floating point processors and memory management units increase the virtues of a graphics processor board.

Some manufacturers are betting heavily on the newer 32-bit CPUs like Motorola's 68020. One such company, Graphics Strategies (San Jose, CA) is using the Versabus for its VGM series of graphics boards based on the NEC 7220. Users can develop programs on the 68000 and then upgrade the system with no change in software. The VGM series comes in three resolutions at 4 bits deep: 512 x 512, 1024 x 768, and 1184 x 885. Each



Peritek's VRH-Q, offered on the Q-bus, is capable of a monochrome 1024 x 1024 display and includes a 64 x 128 character alphanumeric display generator.

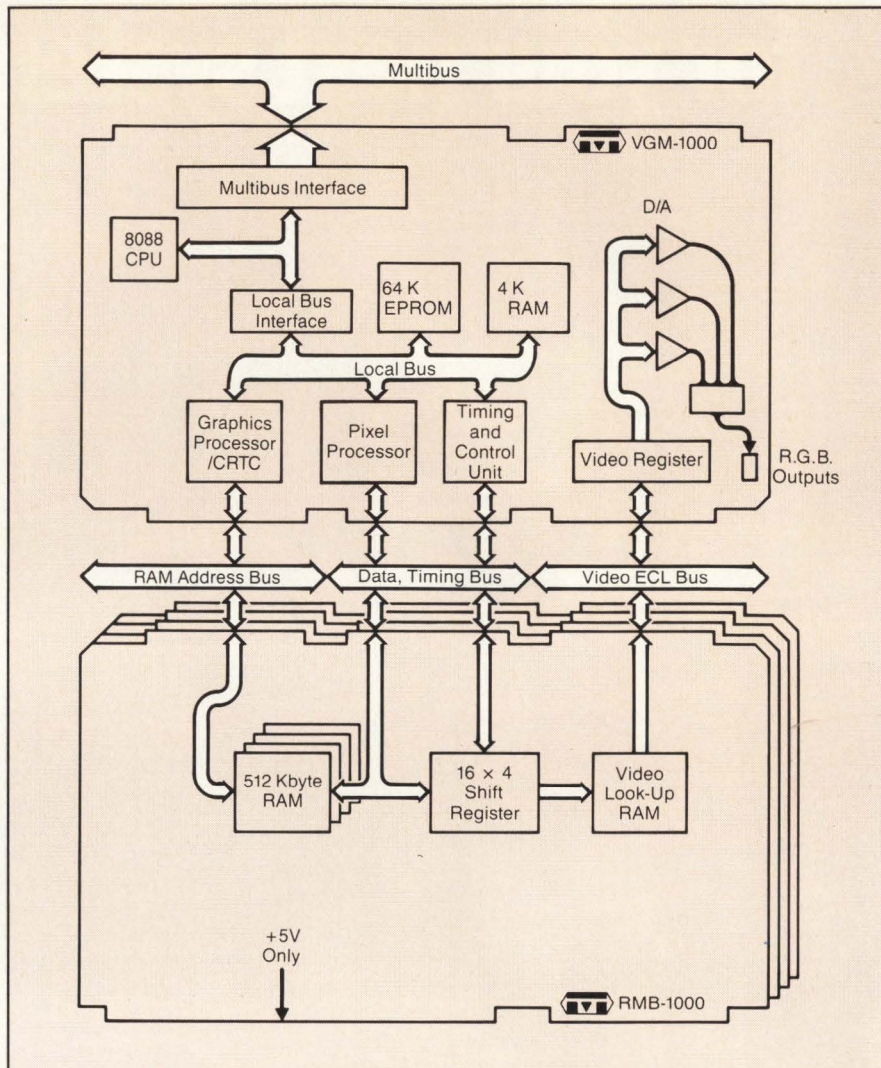


Figure 2: The GXB-1000 board set from Matrox combines VLSI circuits with high-speed ECL logic and advanced software.

board can process 36 graphics primitives in addition to alphanumeric. The VME-512 is a similar board but is based on the VME bus. It can display eight colors at 512 x 512 pixels in two intensities.

VMEbus Support

Strong support for the VME bus comes from Ironics (Ithaca, NY). They supply a complete set of VME boards in addition to a graphics board. Based on the NEC 7220, three resolutions on the IV-1651 are available: 16 colors at 600 x 800, four colors at 1024 x 1024 or 1280 x 768. Additional cards can be synchronized to obtain more colors at the higher resolution. A CRT board supports displays up to 66 lines of 102 characters, interlaced. It has a 256 character set and allows users to de-

fine their own fonts and mosaics for special applications. Both boards may be combined to overlay alphanumeric on graphics.

For some system integrators, terminal emulation is important. PsiTech (Tustin, CA) is a manufacturer of terminals and also sells graphics boards separately. They offer three versions: the VME/1, /2, and the /3. The VME/1 has all the features of their 6809-based terminal. The /2 is a higher resolution version of the /1 at 640 x 480 noninterlaced or 1024 x 1024 interlaced. The /3 is an even greater upgrade with a text overlay plane allowing extra functionality such as scrolling or non-scrolling windows. Up to 16 windows can be displayed beyond the viewport, if the user, for instance, wanted to

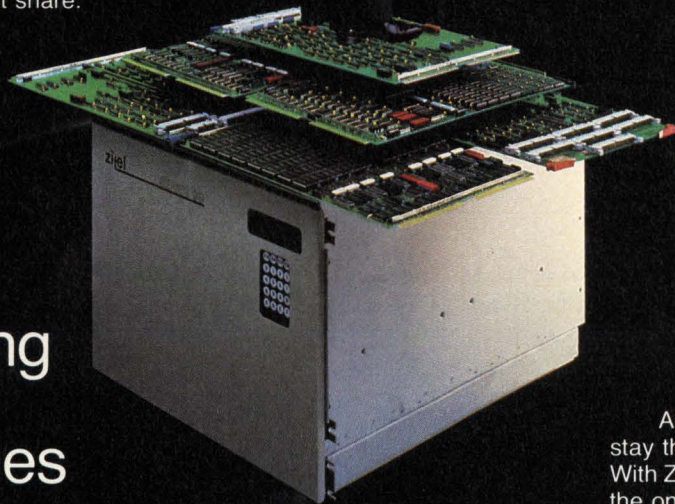
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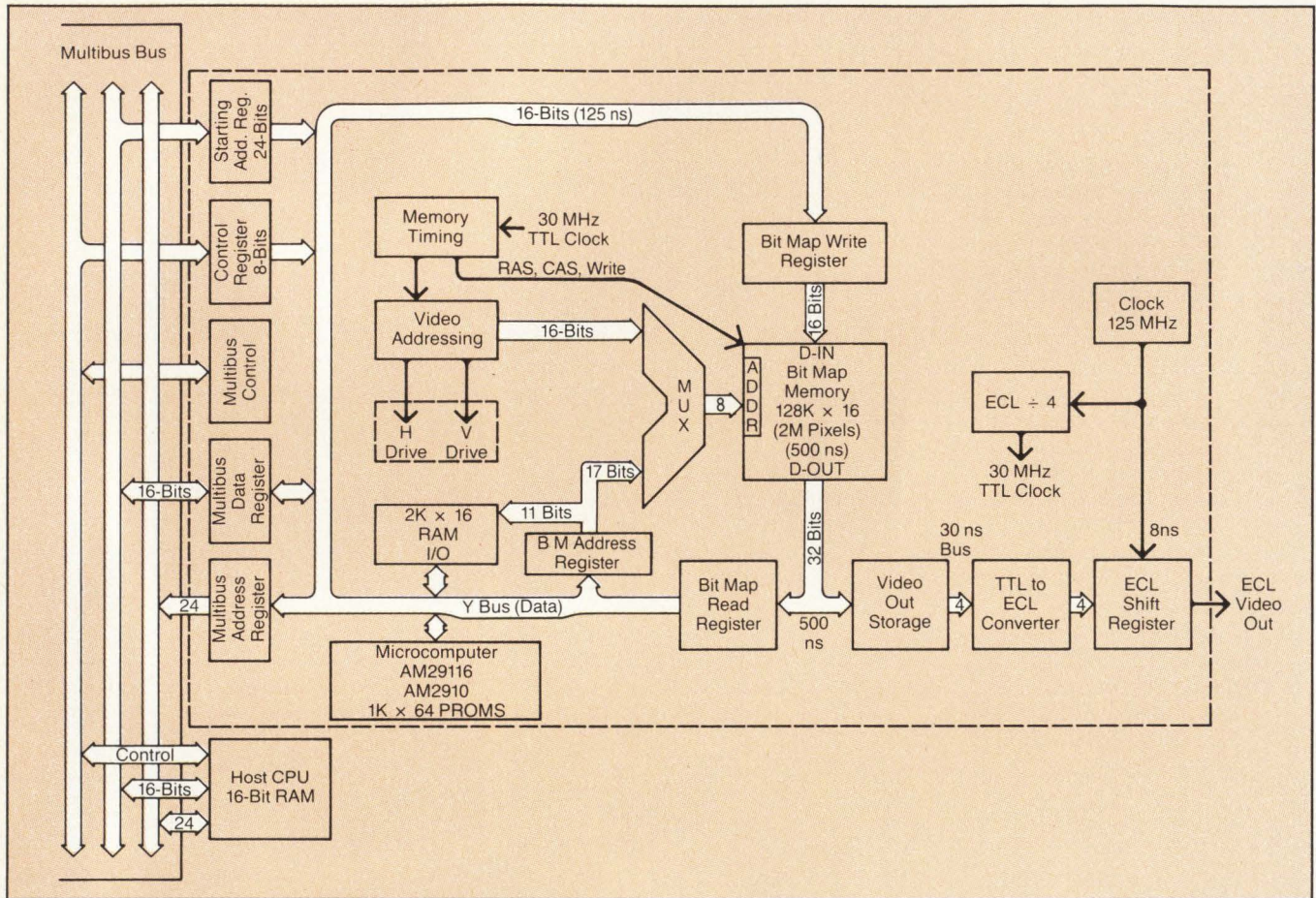
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Figure 3: Datacube's VG150 board functional diagram.



Software support for Peritek's VRH-Q includes a version of GKS, VDI, two levels of graphics subroutines, and an image editor using a mouse.

see six lines out of 100 existing lines of text. Terminal emulation of Tektronix 4107 is possible on the /3 for easy interfacing with ISSCO and PVI software.

The S-100 And STD Buses

Originally designed for 8-bit hobbyist applications, the S-100 bus still prevails, with numerous systems and boards available. Endorsed by the IEEE, many S-100 based graphics boards are available with functionality rivaling that of miniframes. Systems integrators find the S-100 based boards less expensive than comparable boards on other buses.

Many manufacturers cater to specific markets. Digital Graphics Systems (Palo Alto, CA) manufactures eight graphics boards at different resolutions. The CAT 1600 is their most powerful and comes in three versions: a single image plane at 8 bits deep, three images also at 8 bits deep, and one image at 24 bits deep. An extensive on-board library of functions is interpreted by a 7 MHz 8086 providing smooth scroll, pan and logarithmic zoom, in addition to basic image processing functions. A dual ported memory

provides fast Direct Image Access. Using a 68000 host, the image transfer rate to and from the static RAM is 3 Mbytes/sec. These high data transfer rates are required for video animation.

Industrial applications opting for small size and high reliability have utilized the STD bus for 8-bit industrial applications. As a result, manufacturers such as Matrox and Ironics who have experience making graphics boards on other buses also offer an STD configuration. A number of other companies such as Applied Micro Technology (Tucson, AZ) rely on the 6845 to provide graphics boards for the industrial market such as real time process control display.

High Resolution For The IBM PC

The popularity of the IBM PC and its clones has led to peripherals galore, some with remarkable capabilities on a single board. Thanks to the NEC 7220 and 64K RAMs, small board size is possible without compromising performance.

Vectrix (Greensboro, NC) makes the Midas board displaying 480 x 672 pixels with 4096 simultaneous colors. The

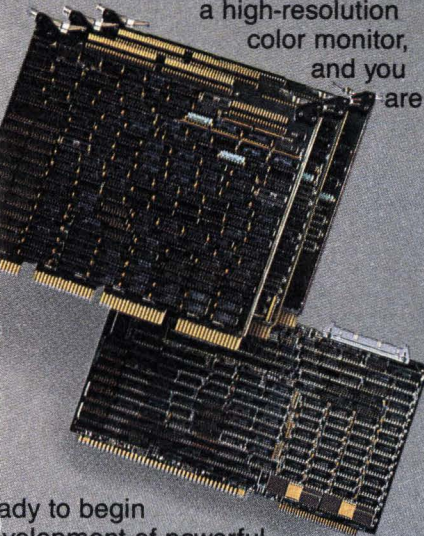
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Easy To Integrate

Parallax's high-performance series of graphics controllers let OEMs and system integrators add astonishing graphics power to standard microcomputers — Multibus and Q-bus controllers are available now.

These controllers are designed for easy integration and are self-hosting — just plug the Parallax controllers into a Multibus or Q-bus system, add a high-resolution color monitor, and you are



ready to begin development of powerful graphics applications.

The Parallax graphics controllers also give you the advantages of low power consumption, light weight — and with their advanced board-level designs, provide a price/performance ratio that is ideal for individual graphics workstations.

Exceptional Speed

With drawing speeds of up to 88 million pixels per second, you get

more productive interactivity between the operator and your microcomputer graphics system.

- The Series 600 single-board controllers draw at 12 million pixels per second.
- The high performance Series 1000 board-set controllers draw at 88 million pixels per second, with Block Image Transfers (BLIT) at 14 million pixels per second.

“...drawing speeds of up to 88 million pixels per second.”

With immediate interactivity, applications such as animation, CAD/CAM, on-screen page make-up, and business graphics are easier to work with, simply because images and graphics appear instantly on screen — and can be changed just as quickly.

Parallax's rich instruction set provides single-instruction Polygon, Box, Circle and Vector drawing, Solid Fill, Outline, Stipple, Block Image Transfer, Opaque/Transparent, standard and user-defined Text modes, vector DeJagging — and the list goes on.

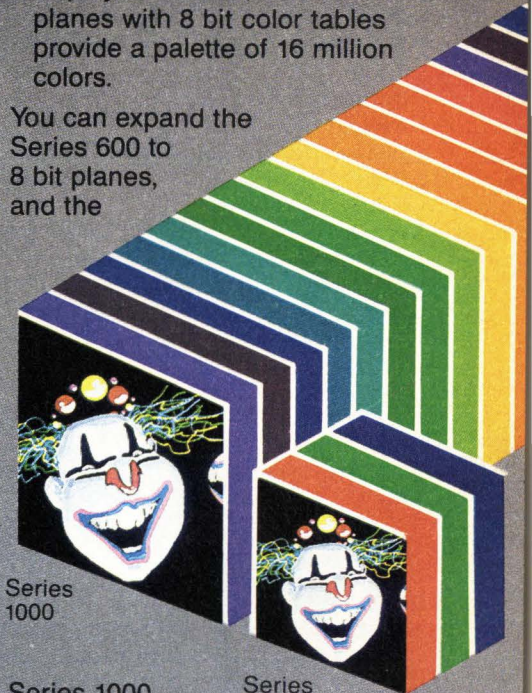
High Resolution

1024 x 1024, 60 Hz non-interlaced display is yours with Parallax's high-performance graphics controllers.

- The Series 600 provides 640 x 480 display resolution; standard 4 bit planes provide 16 colors from a palette of 4096 colors.

- The Series 1000 provides 1024 x 1024, 60 Hz non-interlaced display resolution; standard 4 bit planes with 8 bit color tables provide a palette of 16 million colors.

You can expand the Series 600 to 8 bit planes, and the



Series 1000

Series 600

Series 1000 is expandable to 24 bit planes. Other standard Parallax features include double buffering, smooth pan, and integer zoom along either axis — Parallax controllers have a long list of features that mean high performance graphics power for your microcomputer system.

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board functions similarly to their VX-384 graphics processor having nearly the same 80-command instruction set. The difference is the Midas board has faster performance with an 80188 and DMA.

Graphics Board Manufacturers

To receive more information on the graphics board manufacturers mentioned in the preceding article, please write in the appropriate number on the Reader Inquiry Card.

VMI	Write 300
Datacube	Write 301
Parallax	Write 302
Matrox	Write 303
Genisco	Write 304
Weitek	Write 306
Peritek	Write 308
Graphics Strategies	Write 309
Ironics	Write 310
PsiTech	Write 311
Applied Micro Technology	Write 312
Number Nine	Write 313
Omnicom Graphics	Write 314
Vectrix	Write 315
Digital Graphics Systems	Write 316

Options include a Siggraph Core library, 4010 emulation, Plot-10 compatible library and a paint system.

Also relying on the NEC 7220, Number Nine (Cambridge, MA), manufactures a board displaying a maximum of 1448 × 1448. At 512 × 512 resolution, the board can display 256 simultaneous colors. Multiple boards for more bit planes can be added for additional colors. RS-170 genlock is standard, slaving external video sync to the boards' video output.

Omnicom Graphics Corp. (Houston, TX), packs massive power on a single board for interfacing with many buses. The Omni 1000 GDC has a display resolution of 1024 × 1024 at eight planes. It uses an 8086, 8087, 8089, and a 7220 for graphics processing. 1024 Kbytes of RAM is used for display while 256 Kbytes is used for list and image processing. Software support includes 140 GKS commands. What is unique about the board is its ability to interface with other buses via interface boards. These are available for the IBM PC, Multibus, and DEC buses. In addition, it allows a VAX to talk with an IBM PC.

The competition for greater performance

on the board level has led to two predominant trends. Increased use of VLSI and more important, custom chips, are beating the path to greater functionality, not just speed. Some chips are aimed at display techniques while others are focused on accelerating numerical execution.

The other major trend is software support, where specialized tasks such as shading and hidden line algorithms are implemented in firmware. Printer control, light pen inputs, graphics tablet input, and other functions that liberate the host CPU will be seen more on graphics boards.

As users become more sophisticated, demands on graphics board manufacturers increase. Integrators and OEM's have much to look forward to, as CPUs, firmware and architecture power and functionality improve. □

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Bert

How many co's named "Data Systems"? Must be 50!
Milt

How new say: is oriented respons. compet. market

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for

Leadership certainly has its advantages. As well as its problems.

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But one of the rewards of leadership is that you don't have to create excuses. If your heart is true. And your products are outstanding.

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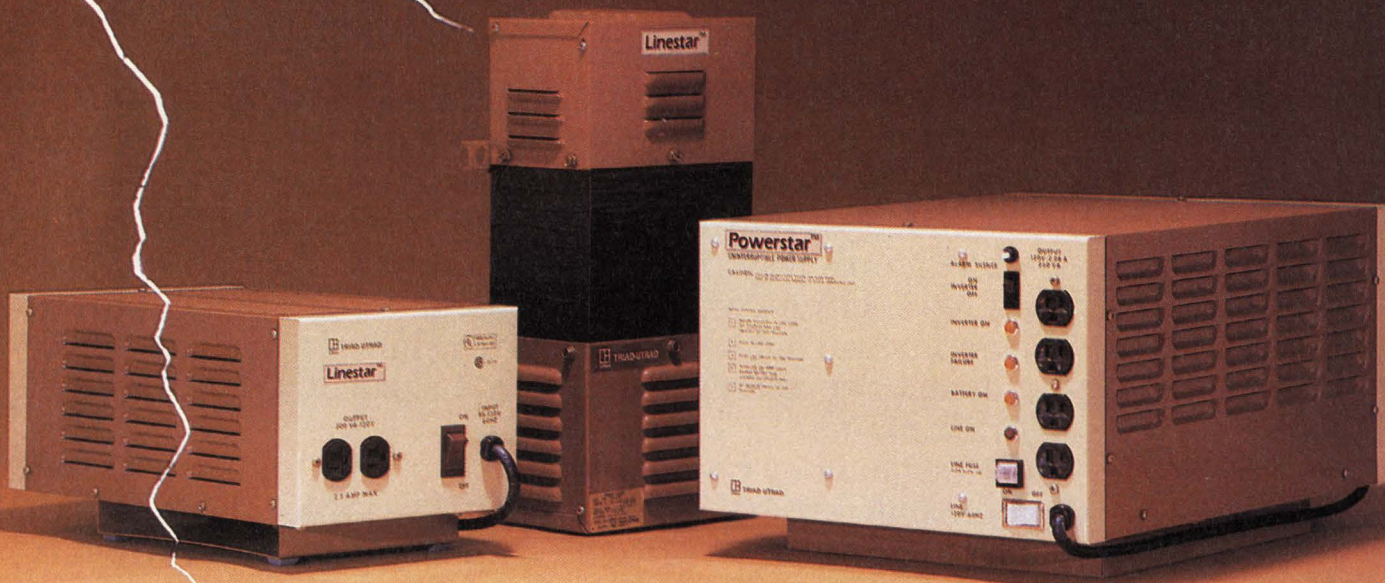
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Designer's Guide Series UPS



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Designer's Guide To Uninterruptible Power Supplies

by Dave Wilson, Executive Editor

AC power delivered to most facilities is neither steady nor reliable. In fact, commercial utility power is rarely of the consistent quality required for the operation of a wide range of modern electronic and industrial equipment.

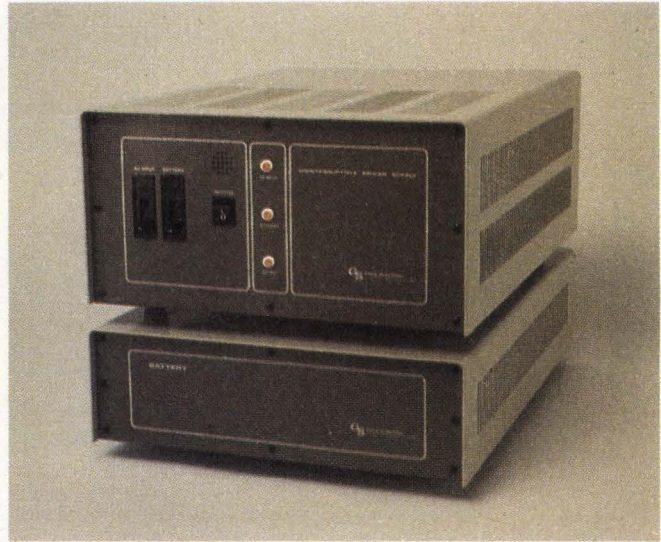
Utilities have specifications defining limits for frequency variations, amplitude variations and harmonic distortion. They do not, however, officially recognize the existence of fluctuations lasting less than 30 msec that occur during load switching or phase compensation. This official silence is not wholly unreasonable, since many of the transients, fluctuations and interruptions are not caused by power company equipment. Some officials, however, have disclosed that voltage variations, conceivably as great as 300%, and lasting from 30 msec to one minute, are more likely to occur several times a day than several times a year. While power generating companies make every effort to ensure the quality of their output, it would still be impossible to control every disruptive variable that might be encountered in the distances between the generators and the AC socket where critical equipment is connected.

It is important to note that the American National Standards Institute (ANSI) allows normal transmission line power to sag below nominal (typically 120V AC) by as much as 8.3% by the time it reaches the users' service entrance. ANSI also allows an additional 3.4% drop in voltage due to the normal intra-building impedances, such as cables, connectors and fuses. Together, these allowed voltage losses may provide AC power that is 11.7% below nominal before it reaches the users' equipment (Figure 1).

Defense Against Power Problems

Most smaller computer-based systems cannot operate properly when AC voltage reaches approximately 15% below nominal. But sensitive equipment often operates from a power line which is near this level even during normal conditions. Under adverse conditions, it is not uncommon for AC voltage to drop as much as 21% below nominal, well outside the tolerance range of computer-based equipment. In order to ascertain the quality of the power output, it is first necessary to have some familiarity with the nature of the problems that may exist.

Blackouts are the easiest power problem to detect, except for those with very short durations, such as half second switchovers



Above: This 1.0 kVA UPS is from Sola Electric. Preceding page: Various size and power UPS systems comprise the Isoguard series.

In order to ascertain the quality of the power output, it is first necessary to have some familiarity with the nature of the problems that may exist.

from one substation to another. These can have the most detrimental effects on equipment, data files and manufacturing processes. Uninterruptible power supplies (UPS) are the only realistic cure for problems of this magnitude.

Brownouts are planned voltage reductions that can be relatively easy to detect and are often announced by the power companies in anticipation of excessive demand. Generally, they even fall within the 10% working tolerances of most equipment. An overall voltage reduction, however, can result in greater susceptibility to other voltage or noise problems. The effect of moderate level brownouts can be alleviated with the use of a power line conditioner. Unplanned undervoltages and all voltage drops in excess of 15% usually require the installation of a UPS.

Voltage fluctuations, when severe, can be detected by the visible flickering of electric lights. Fluctuations to high voltage can result in damage to equipment, while short periods of low voltage can cause a loss of data, improper functioning of real-time manufacturing systems with the possibility of a resulting waste of materials, disturbance of continuity in security sys-

tems, and erroneous readings in monitoring systems.

Noise and transients superimposed on the power line are the most common sort of power disturbances, but fortunately, the easiest to correct. They are, however, often the most difficult to detect, as their durations average only one to 200 μ sec. Power line noise can be caused by lightning, poor grounding and radio and TV transmissions. Noise and transients can cause false triggering, lost data, data entry errors and in extreme cases, equipment damage. Line conditioners and UPS are designed to eliminate this problem.

An uninterruptible power supply is the answer to the widest range of power problems. It may not always be necessary unless blackouts or severe low-voltage fluctuations are expected or the operation being protected is essential.

To effectively deal with noise, transients and voltage fluctuations, a number of line conditioner solutions exist and can be selected, based on the specific combination of power problems. But where any combination of severe line conditions or critical applications exist, a UPS is the solution.

Choosing a UPS

When determining the proper UPS system, there are several factors that must be taken into consideration. These include the voltage demands of the load, the efficiency of the UPS, the quality of the AC power output desired, and the sensitivity of the load to voltage changes.

The first step in selecting a UPS is deciding what size kVA rating is needed. A collective power rating will consist of not only the critical load or protected device, but also any peripheral devices, such as emergency lighting and power to ventilate the battery room. The AC service input line should carry approximately one and one-quarter the total kVA rating. This is required because following a line failure, the UPS must draw enough power to satisfy the load and recharge the battery bank simultaneously.

Several factors are important to consider in the evaluation of UPS units. 1) Steady-state regulation is a measure of the UPS voltage output fluctuation going to the critical load under nor-

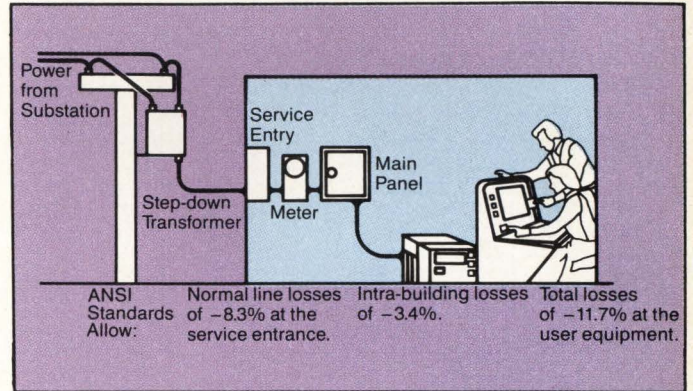


Figure 1: Together, allowed voltage losses may provide AC power 11.7% below nominal before it reaches the user's equipment — courtesy Topaz.

mal conditions. UPS systems with the least fluctuation better protect the load. 2) Dynamic regulation is a measure of the over-voltage and undervoltage that occurs in the output voltage waveform when the load changes. This should be within 8%. 3) Transient response is a measure of the speed with which the UPS system can react to sudden changes in the critical load. The faster the response, the better the protection and regulation. Output harmonic distortion is one measure of the quality of the AC sine wave created by the UPS system. Minimal harmonic distortion provides cleaner power. This should be within 5% total and 3% single harmonic. 4) Overload capability is a measure of the amount of output power overload a UPS system can withstand without damage. The figure should reach up to 125%.

Forward Vs. Reverse Transfer

Before examining some of the design issues that relate to UPS, it is important to note the distinction between forward and reverse transfer systems. In forward transfer systems (Figure 2), the UPS is off-line, and the commercial line actually drives the critical load through a transfer switch. During this time, the UPS is rectifying that same commercial line and providing "hot standby" current for the inverter as well as the current necessary to maintain the battery at full charge. The inverter idles during this time, supplying no power to the critical load.

When the commercial power is interrupted or fails, a switch transfers the critical load to the inverter. In this mode the inverter draws current from the battery until commercial power is restored. Note that the rectifier-charger is never required to provide current directly to the loaded inverter, but need only be large enough to recharge the battery.

Because the critical load operates from the commercial power line in the normal mode, it is vulnerable to any transient, fluctuation or noise that occurs. In reverse transfer UPS systems (Figure 3), the UPS acts as a buffer between the commercial power source and the critical load. The rectifier/charger pro-



Behlman Engineering's Model UPS 100-II.

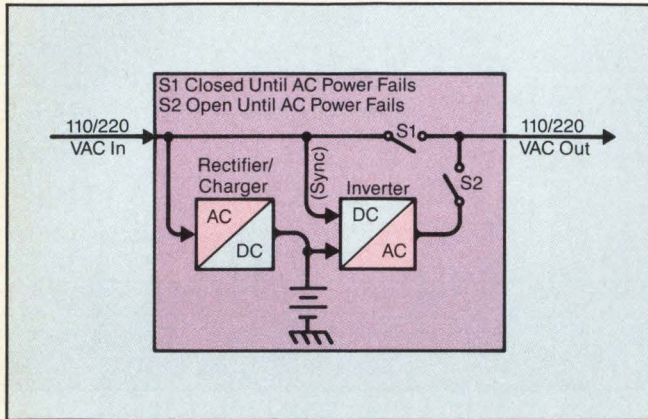


Figure 2: *SUPS—forward transfer is common in systems greater than 1kVA.*

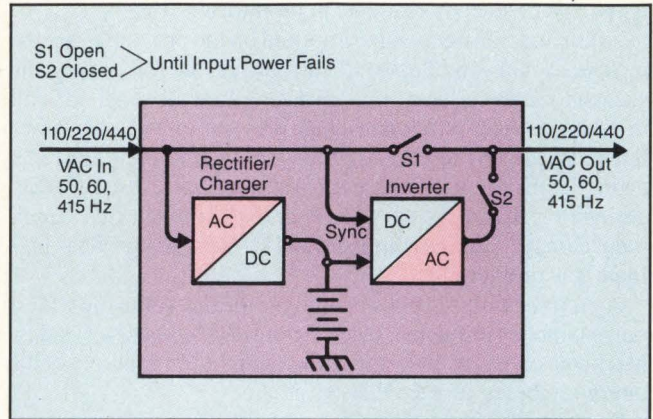


Figure 3: *SUPS—reverse transfer is used in systems less than 1kVA.*

vides current to the inverter and maintains the battery charge. The charger must be able to meet the input requirements of the loaded inverter as well as maintaining the battery charge. Consequently, it must be larger than the charger used in a forward transfer system. Also, the inverter is under more stress, since it is always "on-line."

Powering The UPS

The rectifier/charger is the heart of the UPS. Its principle functions are to deliver the power required to drive the inverter and maintain the charge on the battery. It must be able to deliver enough power to drive the inverter at full load (except in the forward transfer system) and have sufficient margin to handle

momentary overloads on the order of 125-130%. The inverter subsystem of a UPS is the major determining factor in the quality of AC power delivered to the load. Each type has certain characteristics which are directly related to its suitability for various applications.

The function of the inverter is to change the DC voltage from the rectifier/charger or the battery to DC which in turn can be shaped and filtered to produce a sinusoidal voltage to meet the requirements of the critical load. The most commonly used types of inverters are the ferroresonant, quasi-square wave, pulse width modulation and stepped wave. A hybrid inverter combines the features of the stepped wave and pulse width modulated inverters.

Ferroresonant Inverters

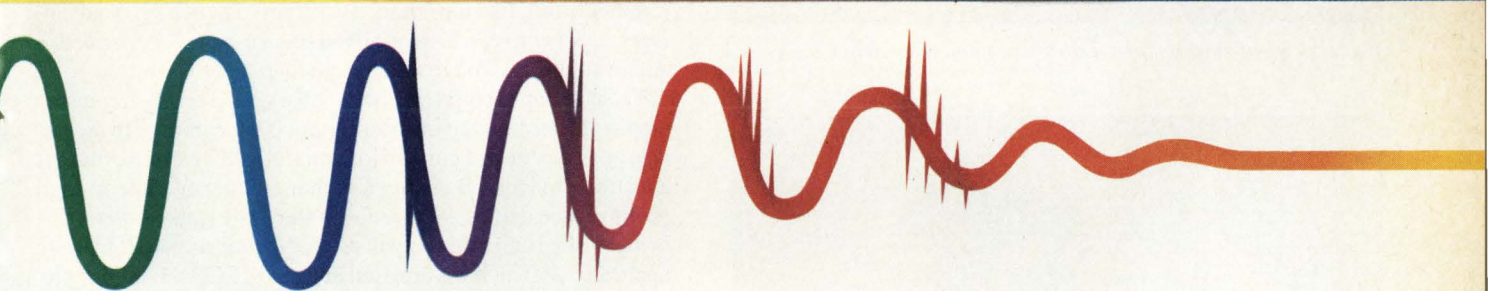
Commonly used for single-pulse inverters and line voltage regulators, the ferroresonant transformer has been adapted for three-phase UPS use. The size and weight of ferroresonant inverters limit their use to smaller kVA installations.

Topaz, for example, makes use of ferroresonant inverter circuitry for its UPS systems below output power levels of 3kVA. In the middle power range of 3kVA to 15kVA, Topaz claims that the quasi-square wave circuitry has cost, performance and reliability advantages.

The ferroresonant approach (Figure 4) starts with an unregulated inverter producing a square wave or quasi-square wave and has a ferroresonant transformer for its output. The transformer regulates the output voltage, smooths the waveform to acceptable distortion limits and provides current limiting. An inherently simple approach, it does have its limitations. Since it depends on energy storage to perform its functions, a ferroresonant inverter always has considerable overshoot upon load removal, and a significant undervoltage upon load addition. Because of its simplicity and low component count, the design is reliable and relatively inexpensive.



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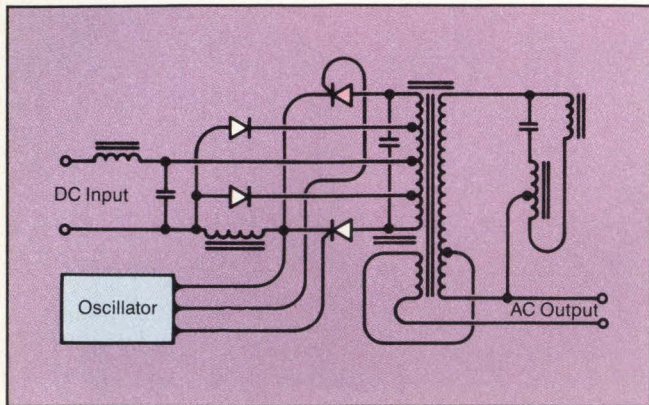


Figure 4: Configuration of a ferroresonant inverter from Gould.

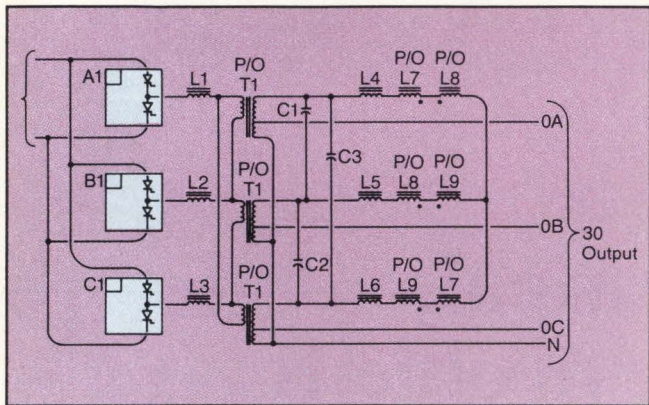


Figure 5: Regulation and filtering circuit diagram from Lortec.

A three-phase ferroresonant inverter is three single-phase inverters tied together with their square waves 120° apart. Ferroresonant output is inherently limited by the current due to the inductive coupling between the primary and secondary of the transformer. Output voltage of a ferroresonant is not dependent on a closed loop, but more on the design of a transformer.

Inverter System Choices

A different regulation and filtering technique has been used by Lortec Power Systems for its three-phase inverters. Like ferroresonant inverters, the Lortec design is simple, rugged and reliable. But where the ferroresonant is a single-phase device adapted to three-phase UPS use, the Lortec circuit is inherently a three-phase device.

A simplified circuit schematic of the Lortec system is shown in **Figure 5**. Inverter modules A1, B1 and C1 produce square wave outputs that are phase shifted from each other by 120°. The square waves are coupled to the primaries of transformer T1 through linear inductors L1, L2 and L3. T1 is a conventional three-phase isolation transformer, not the three single-phase saturating transformers typically used in a ferroresonant inverter. The primaries of T1 are connected in a delta configuration to eliminate the third order harmonic and all other harmonics which are odd order multiples of the third. As a result,

less filtering is required than for a ferroresonant system.

The quasi-square wave approach (**Figure 6**) is the simplest that uses true electronic (rather than magnetic) regulation. It creates a variable duty cycle that must be filtered by the tuned series and parallel LC networks (L1-C1 and L2-C2). Since these filters are tuned, this inverter responds slowly to load transients and its frequency must be fixed. Its efficiency is typically about 75% and it requires voltage-regulation and current-limiting networks, which increases component count and circuit complexity. The performance characteristics of this approach are generally limited by filter design and impedance.

The pulse width modulation inverter is in reality a combination of two inverters. Sometimes referred to as a fourth generation inverter, like the others it does have its own set of advantages/disadvantages. Essentially, a square wave is generated at a high frequency and its duty cycle is varied.

The number of pulses per half cycle depend on the frequency employed, as does the inverter output performance. In the design and selection of pulse-width modulated inverters, there is a distinct tradeoff. By using a higher frequency system, high performance can be achieved, but the SCR state-of-the-art is being pushed and reliability is severely compromised. In these applications, transistors are used in place of SCRs. For example, in RTE Deltec's 3000 series of on-line UPS systems, available in 500VA, and 1kVA ratings, FETs switching at 50 KHz are used.

The step-wave inverter (**Figure 8**) is usually employed in large three-phase inverters. An expensive system, it combines a number of inverters: three, six and sometimes twelve.

Three-phase six-step inverters provide very stable output voltage, compensate for line droop and allow instantaneous and infinite control of voltage. Multiple SCRs turn the DC input into a six-step wave configuration approximating a sine wave. A filter system removes harmonic components to produce a true AC sine wave. Because fifth and seventh harmonics must be removed, a filter is necessary.

The three-phase twelve-step inverter increases the number of SCRs used. This produces a truer approximation of the sine wave before passing through the filtering system to become a true AC sine wave. Because less harmonics must be removed, smaller filtering systems can be used. This reduces space and weight and makes the three-phase twelve-step inverter ideal for larger kVA rated systems.

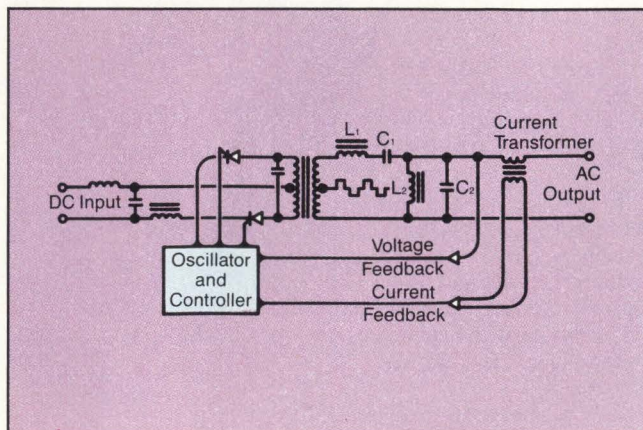
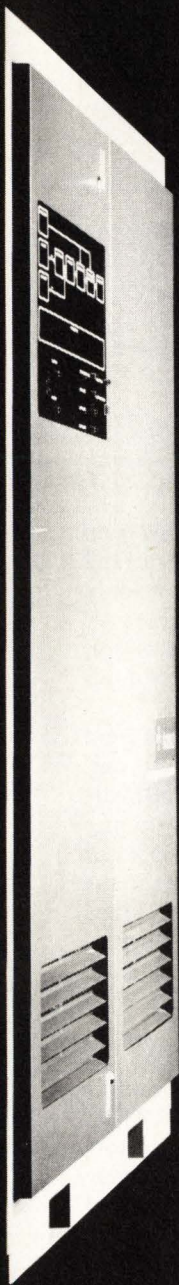


Figure 6: A quasi-square wave inverter—courtesy Gould.

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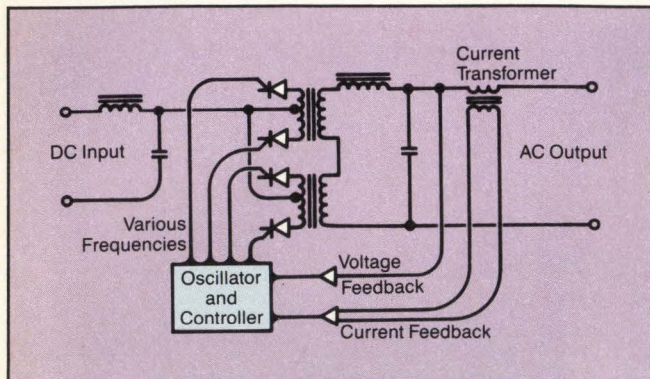


Figure 7: A Gould block diagram of a pulse width inverter.

Output Transfer Switch

The output transfer switch is designed to protect the load from interruption by continuously monitoring both the inverter and load. Three types of output transfer switches are commonly employed – electromechanical, static and a hybrid of the two.

1) An electromechanical transfer switch is a relay or contactor. Because of the relay action, there will be a loss of power for two to six cycles during transfer.

2) The static switch is a solid-state device configured from power SCRs, that can transfer the load between the inverter output and auxiliary power in a few msec with virtually no interruption. 3) A hybrid switch is a cross between the electromechanical and static switch, consisting of both motor-operated circuit breakers and SCRs. The SCRs maintain power to the load until the inverter breaker opens and bypass breaker closes. Continuous UPS systems only have a manual transfer or bypass switch, since adding an automatic transfer switch converts the continuous UPS to a reverse transfer UPS.

Battery Backup

UPS systems are installed with batteries which provide from as little as 30 seconds to 24 hours or greater backup time. Many people purchase a UPS primarily to prevent the costly errors that line transients can cause and only want a reserve adequate to effect an orderly shutdown of their operation when a total blackout occurs. Others will install a standby engine-generator to provide long-term blackout support, supplying power to the UPS input when the utility has failed. Other UPS users may require continuous operation regardless of utility conditions and do not wish to get involved with installing a generator.

Different battery options exist depending on the application. Lead-calcium, for example, offers many advantages to the user who has no secure, ventilated area in which to locate a conventional wet-cell battery bank or who wishes to perform no maintenance. The disadvantages of these is their finite life in UPS applications – approximately five years. Conventional lead-calcium batteries are typically warranted on a prorated basis for at least 10 years; they must, however, be installed in a secure ventilated area.

Lead-antimony batteries are equivalent to lead-calciums in terms of current and support lines. However, their warranty periods are only about half that of lead-calcium and require

Familiarity with the varieties of power supply problems that may exist at any particular installation is the first step in determining whether an uninterruptible power supply is truly a necessity.

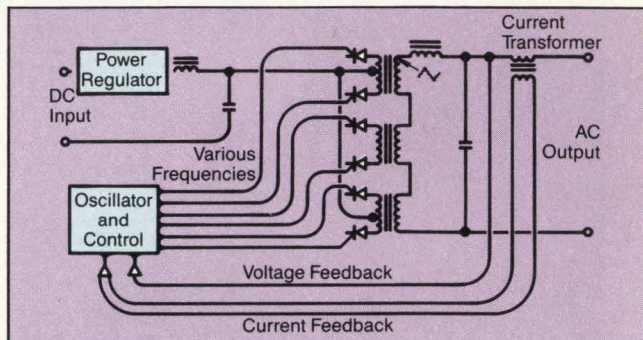


Figure 8: A step-wave inverter – courtesy Gould.

monthly equalize charging to retain their capacity. Nickel-Cadmium (NICAD) batteries are typically the most expensive of the battery types used in UPS. Their advantages lie in small size and weight for a given capacity and excellent high and low temperature properties. NICADs do require monthly equalize charging as well as periodic deep discharge cycles to retain their capacity. They have long life, nearly that of lead-calciums and require maintenance at six-month or shorter intervals.

Conclusion

Familiarity with the varieties of power supply problems that may exist at any particular installation is the first step in determining whether an uninterruptible power supply is truly a necessity. Certainly, other options exist, ranging from surge suppressors to line power conditioners. These may solve a great majority of the computer integrators' problems.

UPS systems, however, available in a wide range of sizes and features, still remain the answer to the widest range of power supply problems.

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- 2) *UPS Systems*. Standby Power Inc. □

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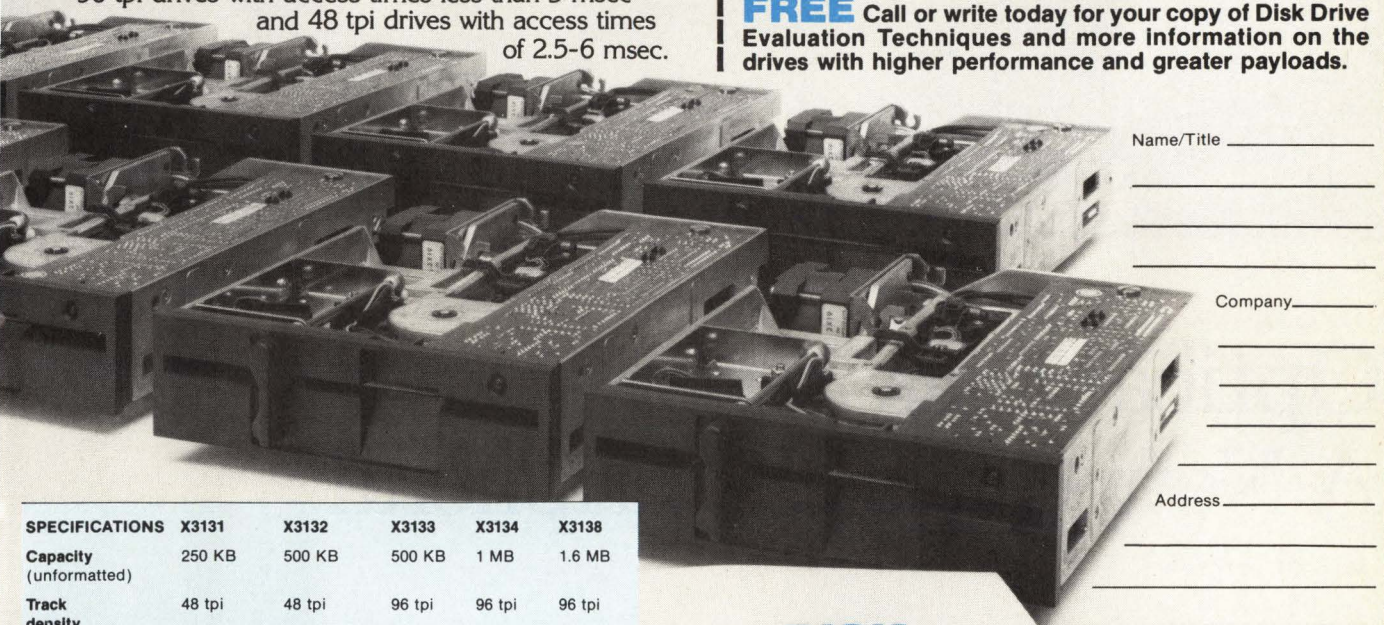
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Optical Disk Technology Creates A New Class Of Peripheral

by Julie Pingry, Senior Editor

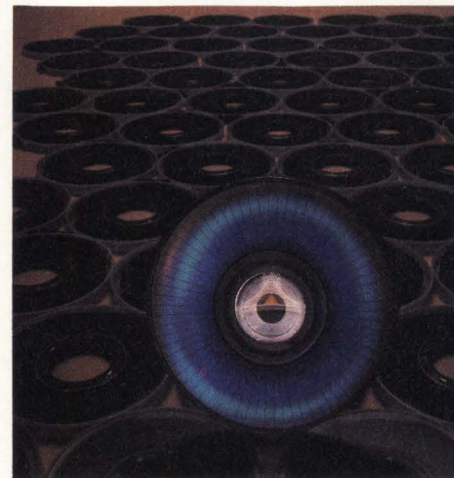
Dramatic increases in computers' capabilities create escalating demand for quantity mass storage. Equally rapid decreases in system size put a premium on space. Partly because of these trends, optical disk data storage, with the capacity to store at least 1 Gbyte on a single 12" surface, has received significant attention and development funding.

Though single optical disks can store larger quantities of data than magnetic disk or tape, they are not erasable. Therefore, the impact of these devices is not like that of new high capacity Winchester, tapes or solid state memory. Optical

disk drives are actually a new class of mass storage peripheral.

Not only is the recording technology new, the capabilities and advantages of optical storage drives are different than any existing part of a computer system. Optical disks offer higher density than magnetic memory, with both more bits and more tracks per inch (bpi, tpi) possible. In addition, the medium is removable, one of the advantages that has made floppy disks so pervasive.

The spinning disk provides fast quasi-random access to data, like magnetic disks. Optical disks generally spin more slowly than magnetic platters, but the speed to access 1 Gbyte is much better,



This new technology provides a removable, permanent file that can be rapidly electronically accessed.

since the data is on one disk surface and can be accessed without pausing to change disks.

Because current optical disks are a non-erasable medium, they are a fail-safe means of permanent archival storage. Users cannot inadvertently modify optically stored data by recording over it. Error correction codes can correct small overwrite errors so no change is ever seen. If a large area is overwritten, the ECC should flag the area as unrecoverable. OSI and Optimem include write protection for each sector. Also different from the magnetic tape now used for computer archives is that optical disks degrade very slowly over time (most are guaranteed for 10 years or more) and don't need rewinding.

Still, optical data storage will not likely replace magnetic tape altogether. Tape has value as an alterable archive for relatively short-term storage when speed of access is not critical. It is compact removable storage that allows modification of files. Filing cabinets could be the main victim of early optical drives, since computers can directly access archives on optical disk. This new technology provides a removable, permanent file that can be rapidly electronically accessed.

Devices announced thus far include Write Once, Read Many times (WORM) and Optical Read Only Memory (OROM). There is a huge effort to produce erasable optical memory to compete with magnetic storage devices. The drive in **Figure 1** announced by Matsushita (Osaka, Japan) is to be available next year, but generally, further research is needed to make rewritable optical disks feasible. Commercial offerings from other firms are probably at least a year or two from announcement.

Typical of new technologies, optical

storage has, as yet, no standards. This will undoubtedly slow the acceptance of optical drives. In introducing a new class of peripherals, optical system manufacturers must launch a large education campaign to convince users of the advantages. The technology and products are here now, and will likely have a solid place in system design soon.

Available Systems

Current optical disk storage systems are either read-only, similar to video and audio optical disks, or writable only once. Most early products are the latter WORM systems. These provide permanent copies of files for backup to a computer's primary storage system. Read-only drives, like video or audio record players, are designed to allow access to information generated at a master site.

Some of the earliest optical systems were huge, expensive multiple-disk systems. Jukebox configurations from RCA, Philips and Panasonic (*Digital Design*, September, 1983) promise nearly instantaneous retrieval of Terabytes of stored information. Even for mainframe computer systems, the instant access capability of these expensive, sophisticated optical jukeboxes is generally overkill. The systems that RCA (Camden, NJ) is preparing for two government customers hold 128 disks, and can access up to 10^{13} bits in under five seconds. Though only two such drives have been ordered, many companies working on optical memory drives admit that the enormous on-line capacity of jukebox-style systems makes them a product under consideration for future development.

To address larger segments of the market, several companies have announced 19" rack-mountable optical drives. As of this spring, five companies had announced 12" disk systems (**Figure 2**) that will be available by the end of the year.

These mid-range drives are specified to read and record 1 to 1.3 Gbytes per disk surface. This spring's conference on Optical Data Storage sported papers describing systems in this range from Optical Storage International (OSI) (Santa Clara, CA), a joint venture between Control Data and Philips (*Digital Design*, June, 1984); Shugart's Optimem Division (Sunnyvale, CA), Thomson-CSF (Le Plessis-Robinson, France), NEC (Kawasaki, Japan) and Hitachi (Tokyo, Japan).

All these systems use disks of a similar size and capacity and are aimed at the same market as backup and archival storage for medium-size computers. With initial systems in production this year, integrators can begin to design optical drives into systems demanding massive on-line storage.

Read-only is the other type of non-erasable optical memory that will be commercial very soon. Like audio and video laser disks, a master copy is replicated to produce prerecorded disks. The first contender in that market is Reference Technology (Boulder, CO). Their system reads digital data from standard video format disks. The use of these disks, which are in mass production, will do much toward keeping media costs down.

These read-only systems will allow the dissemination of large, unchanging or periodically updated bodies of information at relatively low costs; the drive is



Left: A 3M WORM optical disk stores as much as reels of tape.

Figure 1: (right) The first erasable optical disk drive from Matsushita/Panasonic.

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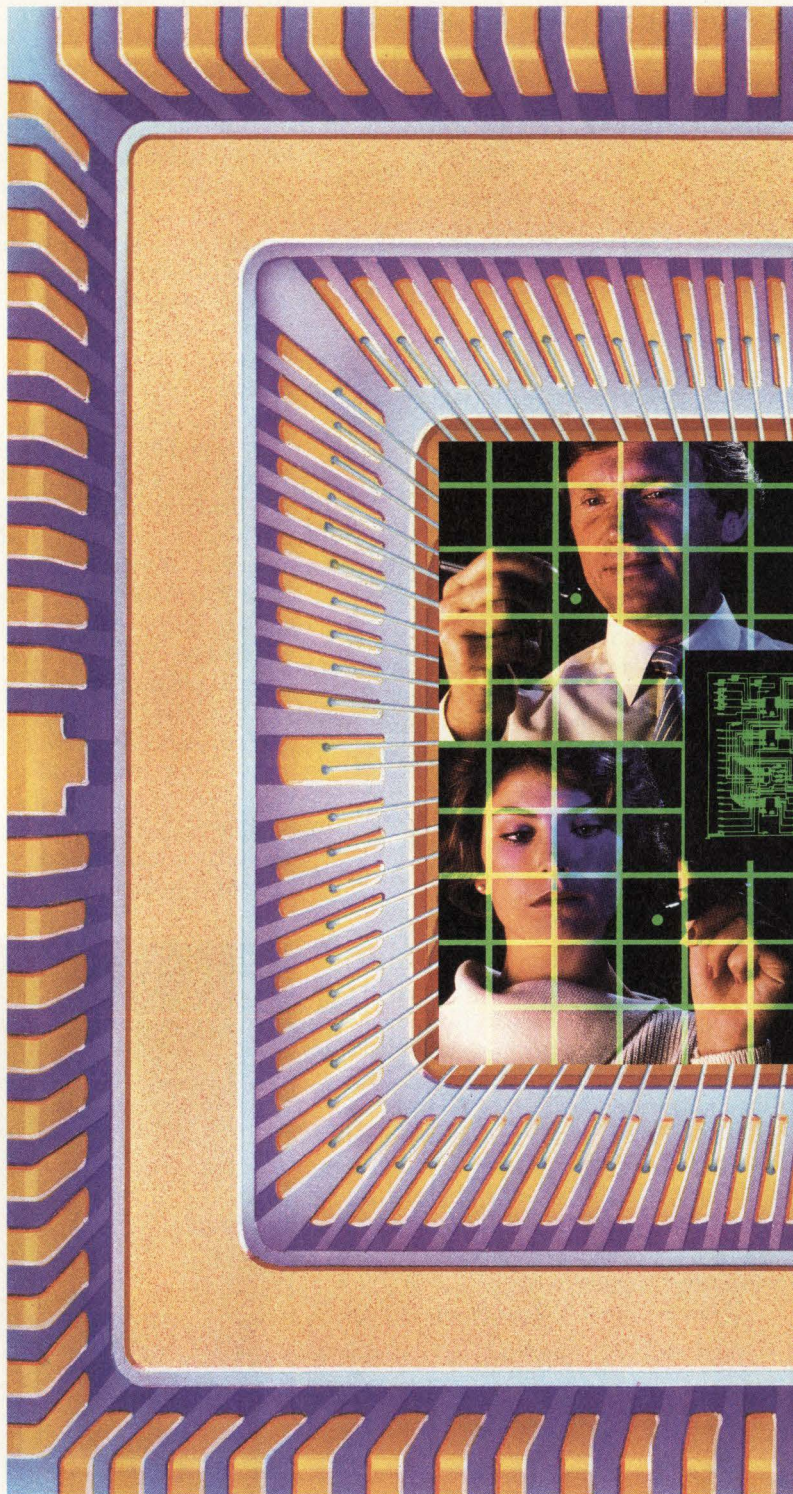
TECHNOLOGY	GATE LENGTH	PROP DELAY TIME*	GATE COUNT
STD CMOS	3.6 μ	7.0 ns	700-3900
H CMOS	2.8 μ	5.0 ns	440-3900
VH CMOS	2.3 μ	2.5 ns	2600-8000

*2-Input NAND Gate, F/O = 2

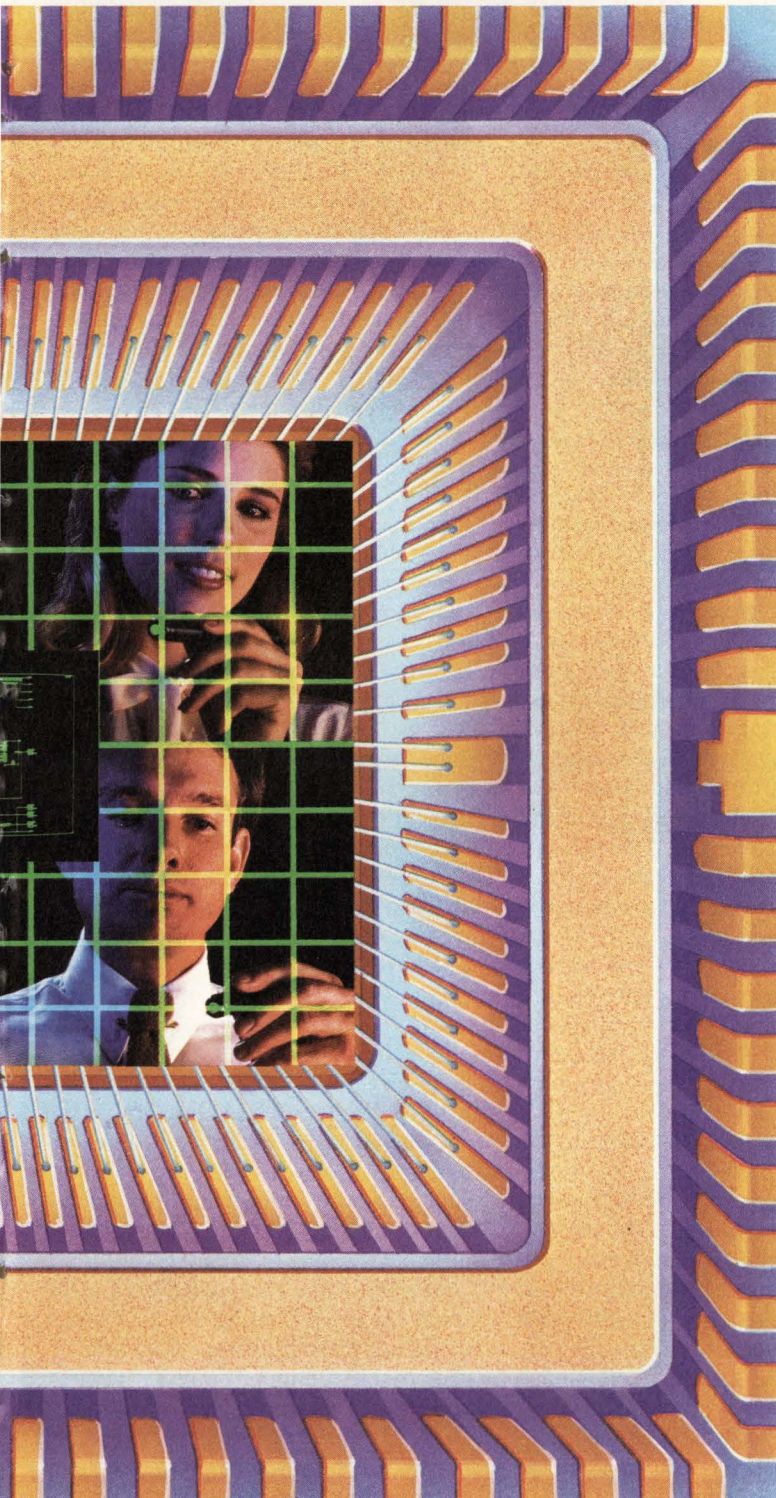
BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

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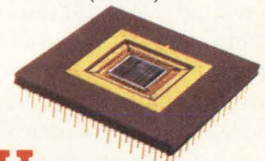
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expected to cost under \$10,000, and disks can be stamped out for under \$10 each now. The main application of this type of optical drive will be software and database distribution. Read-only systems will have a specific niche, and are yet another new peripheral emanating from the optical disk technology.

The huge capacities of optical disks may offer immediate advantages to large computing facilities currently using sophisticated Winchester disk packs. The initial commercial offering of a single-platter system for use with mainframe and large computers comes from Storage Technology Corporation (Louisville, CO). Their 7640 OEM unit is over 4½" tall and uses 14" disks, packing 4 Gbytes of formatted data on a side. Units with an IBM interface as well as an OEM model for integration into other large computer systems are available. The basic drive costs about \$130,000, and platters will cost between \$150 and \$250.

Comparing the Storage Technology system to the 12" systems is like viewing an IBM 3380 next to a small disk system. The technology and basic principles are similar, but the markets served are different. Optical storage drives for use with medium to high-range computers, both writable and read-only, are in beta test and will be available by the beginning of next year.

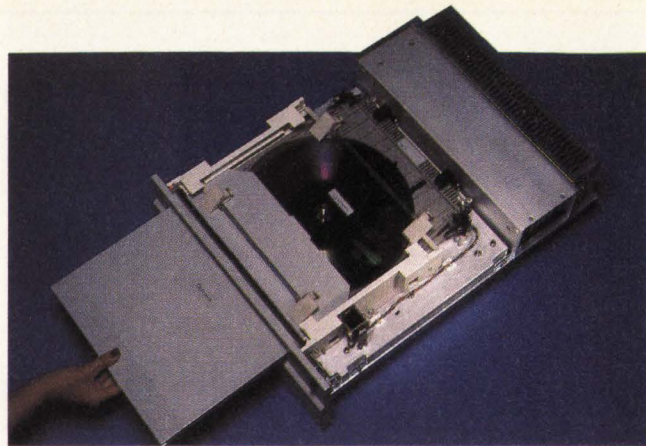
Parameters Of A New Peripheral

There is a concentration of WORM single platter drive products using 12" video size disks of about the same capacity in protective cartridges. Most of these initial systems are offered by traditional data storage manufacturers. Their expertise and understanding of peripheral integration will probably be an advantage in the launching of the new technology.

The announced drives all use a standard disk drive interface. In the case of the Optimem and Thomson-CSF, the SCSI is used; OSI is offering SCSI or the high-performance ISI and Hitachi's drive will use the GPIB. Only NEC has modified their interface, the SCSI. The other drives will be integrated through available controller boards and boxes. This foresight will almost certainly have the desired effect of increasing the number of designers willing to try optical storage.

Fierce competition for market share should provide rapid enhancements and innovative strategies. The five manufacturers of 12" drives offer users the same

Figure 2: Optimem's 1000 drive is one of several systems that reads and writes 1 Gbyte per side of 12" disks.



general capacities and average access times (seek time plus average latency) ranging from 157 msec (with the Optimem drive) to 250 msec on the NEC and Hitachi drives. The systems will have similar capabilities and integrate in a similar fashion, making optical disk drives a true class of computer peripheral.

The majority of new products in the next year will probably be smaller form factor drives, not larger. As seen in magnetic disks, the popularity of small sizes increases with the power of desktop systems. Companies like Information Storage Inc. (Colorado Springs, CO) have 5¼" products close to announcement.

Several start-up companies are eyeing that and even smaller sizes, for use with the microcomputers that have made these sizes popular for magnetic disk drives. According to Ed Rothchild's *Optical Memory Newsletter*, Cherokee Data Systems (Boulder, CO) plans to focus on 5¼" and smaller ruggedized drives. Optical Information Systems Ltd. (Hong Kong), a new company formed by British firms Acorn and BSR, will also look at the small form factor drives.

Regardless of the size of the drive or disk, these systems are the same class of peripheral. They store large quantities of information in a small space, but are removable. Because they depend on sensing optical signals instead of magnetic flux changes, the head flies much higher off the disk surface than magnetic heads. As a result, the drive is nearly impervious to effects of dust on the disk surface.

The big difference between these new devices and magnetic drives is that the information cannot be overwritten. Though that is an advantage for unchanging archives, it could require software revamping. Most software programs now assume that data on a disk can be erased and overwritten and will need to be altered to operate in a write-once fashion.

Optical Recording Schemes

Prices of optical systems vary, and the techniques involved in recording differ greatly, even between those 12" products of nearly the same capacity. The Optimem and Thomson systems are an exception. Since they were developed jointly, they look very much alike and are planned to be compatible, for second-sourcing and disk interchangeability.

Most disks now use glass sandwiched over the sensitive layer. This keeps dust and dirt away from the recording surface, for physical protection as well as an element of distance. Because of the distance between the outer surface and recording layer, any dust or dirt is out of focus.

The goal is to use plastic layers instead of glass, for lower costs per disk. Optimem and Thomson say that their drives will use pregrooved disks available in either glass or plastic. The pregrooving is a common method for recording permanent clock and tracking marks. The recording of grooves doesn't add much to disk cost, but does enhance the interchangeability, since head position markings are not created by the write optics of a particular drive.

Formatting the disk is a key consideration for maximizing data density and minimizing access times of optical disk drives. There are several methods of formatting data to mark sectors. For servo and tracking, various areas on a disk can be marked to serve as reference. Formats similar to those for magnetic disks are effective, although optical systems use a different tracking technology.

The Optimem/Thomson design uses spiral tracks in contrast to concentric tracks like magnetic disks. Spiral tracks can provide continuous transfer of very large files. This is not generally a critical advantage, since transfer rates are very fast, and the stepping of a laser head at the end of each track of disks with concentric

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Figure 3: A greatly magnified photo of a recorded band on the STC 7640: the large white areas at the edges are prerecorded band boundaries; the central patterns are user-recorded tracks.

tracks is a minimal portion of that time. Nevertheless, for use as tertiary storage, unbroken transfers to magnetic primary memory can be an advantage.

On the other hand, short files may not be easy to access on a spiral track. Using the same mechanisms as magnetic disk drives, but with slightly different methods, is the common mode for optical drives. One way to format concentric tracks is to group tracks into bands. StorageTek's 7640 uses this scheme; 48 user tracks can be written per band (Figure 3). At the band boundaries, special tracks are prewritten for servo information. This has a similar effect to that of pregrooving.

There are two main head-to-media interactions now used to optically read and record data on a disk. The technique most used and talked about is ablative, in which the write beam melts holes in a tellurium surface (Figure 4). These holes are then detected by their changed reflec-

tivity in the presence of the read laser. Optimum and Thomson use a bubble-forming recording method, in which the write laser beam heats up the medium, forming gas that is trapped under a metal substrate but has enough force to deform the covering layer. The read beam of the laser in these systems detects the surface deformation.

The makers of bubble-forming systems claim that this type of recording layer is more stable and corrosion-resistant than ablative materials. In addition, there is some improvement in signal to noise (SNR) because the rim of material displaced during ablation (Figure 4) can cause diffraction. But the SNR of optical recording is so much higher than magnetic that these differences are of little consequence. In addition, the tellurium used for ablative holds promise as an erasable medium, as demonstrated by the Matsu-shita system.

The optical heads of the 12" products are all similar (Figure 5). Lenses collimate the diode laser's light into a parallel, circular beam. A mirror routes the light through a quarter-wave plate that changes the linear polarization of the light by 45° and passes it through to the objective lens that forms part of the actuator system. Light reflected from the disk comes back up through the same objective lens and polarization plate. Now linear again and rotated 90° from the original, the plate reflects the beam through an optical system and onto a photodetector. The feedback from the detector is used to check focus and tracking during recording. Such direct

read after write (DRAW) techniques allow continuous error detection.

These single-laser optical recording systems are capable of recording about 14,500 bpi of user information on tracks spaced about 1.6 μm apart. While denser than magnetic storage, this is not the technology's recording limit. Advances in lasers and disk drive electronics should allow even more storage per optical disk surface.

For more sophisticated systems, such as the Storage Technology 7640 drive, a trade-off of complexity is made for capacity and speed. Three lasers are used in the 7640 for the accuracy of recording at a density of 400 Mbits per square inch. A very high power laser diode acts as write device, a low power HeNe gas laser performs reading, focusing and fine tracking, while another laser is needed for coarse seeking and tracking. This compares to a single laser diode, writing at high power and reading at a lower intensity, in the smaller drives.

Integrating Optical Drives

Prior to these optical systems, there have been three vehicles of long-term data storage: floppy disks, magnetic tapes and, for permanent storage, paper files. Optical disks will provide easy access and more compact storage than any of these.

One advantage of a non-erasable recording device is that a permanent record will be made of not only current files, but all iterations they undergo. Unlike current hardcopy files that require both a printer and filing cabinets, even a

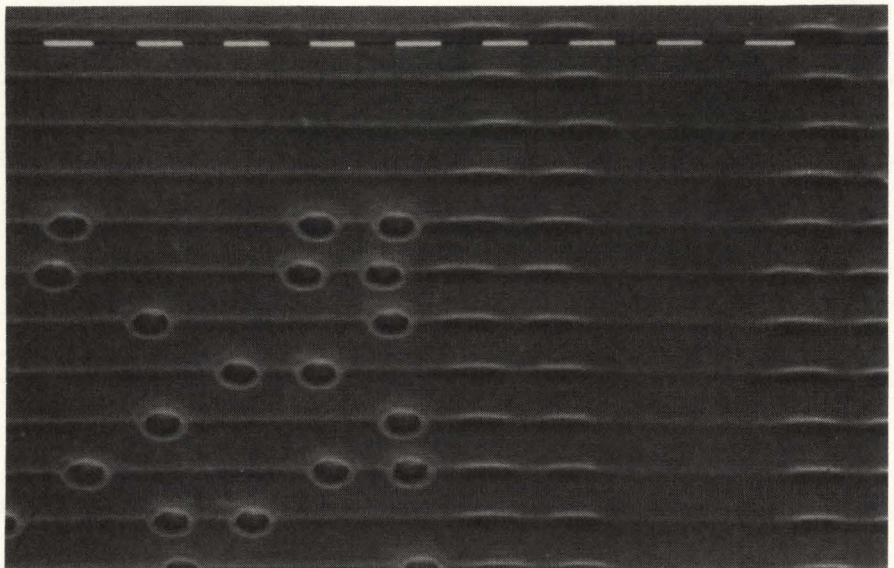
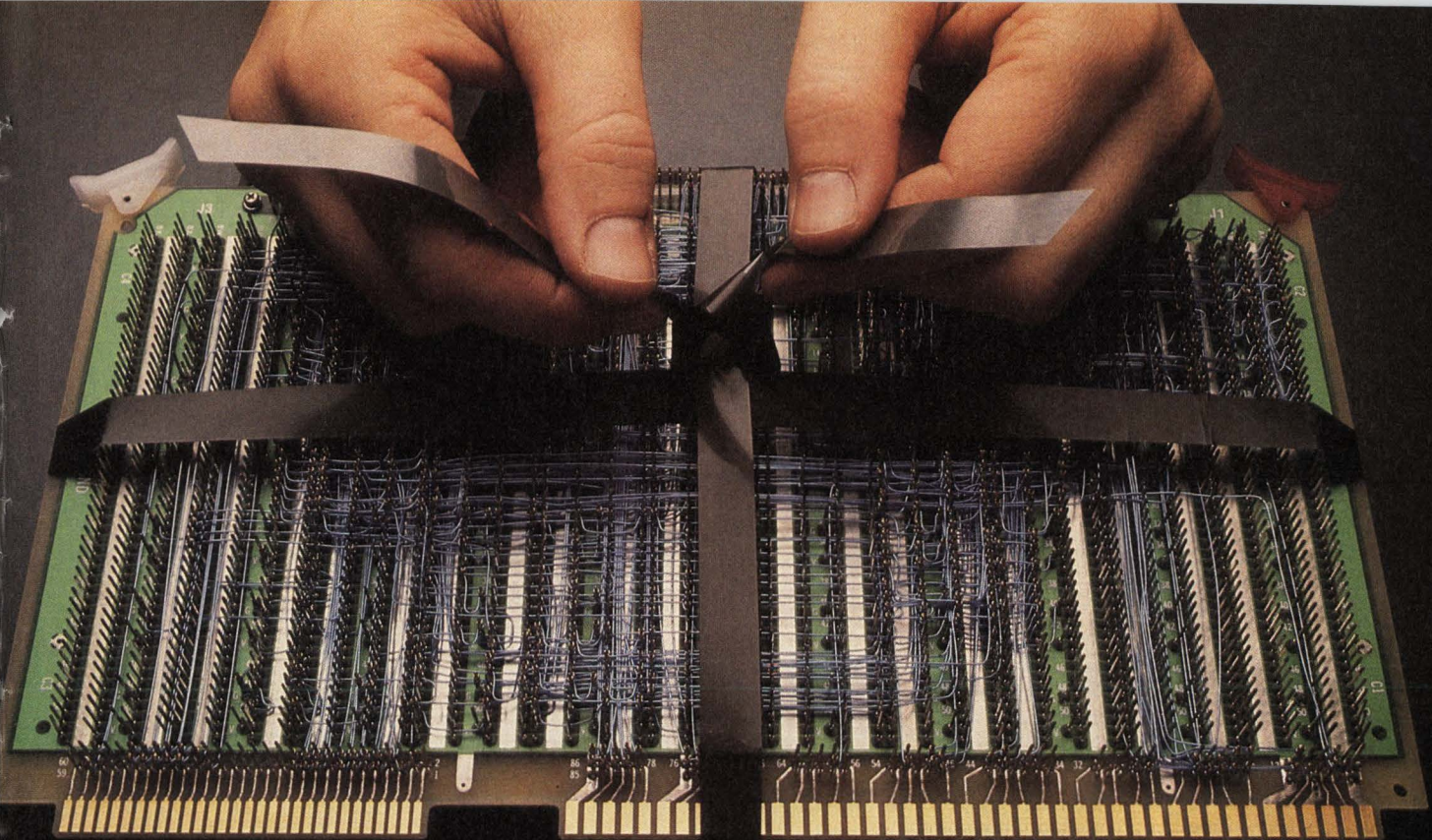


Figure 4: Data on the right was written by ablation in a Philips tellurium surface that is pregrooved (horizontal lines); notice the rims of displaced material around the holes.



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filled disk will provide rapid, on-line access to all of the information stored. The huge capacities of optical disks allow all versions, even of older files, to be saved. In contrast, when a filing cabinet gets full, the user must sort through all of the stored information for priority and chronology and throw some of it away.

Data files stored on magnetic tape or floppies, though more compact and accessible than paper, are usually recorded-over at some point, and older information is discarded. In addition, the information on a magnetic disk is rarely in sequential order, so sector seeking on a disk is highly critical. Optical disks provide that same random access to information in sequential format like tapes. But since optical systems use disks instead of lengths of tape, access is not slowed by sequential formatting.

Using optical disk data storage could allow magnetic tape and disks to be used as a temporary record only, while information may still be rewritten and altered. Once information is in a form useful for future reference, it may be optically recorded. For storage of applications programs, optical storage could replace tape; tape has provided accessible off-line storage for such data and with the capacity of optical disks, many programs could be stored on-line.

This is the general premise behind the Integrated Electronic Filing System from Canon (Tokyo, Japan). It uses optical disk and microfilm for document storage compatible with older office microfilm files plus high capacity rapid access to any information on optical disk.

If stored data is of general interest, like a database or training course, it could be used to master ROM disks. Distribution of large bodies of data would be inexpensive with the pressed disks. In addition, shipment would not be a problem for the plastic, cartridge-encased platters.

Vendors of optical drives have chosen standard interfaces, realizing that they will face obstacles in selling the new devices. The same controllers already in place for magnetic disk drives will be available for integrating optical storage. Even with StorageTek's product for high-end markets, either the IBM or an OEM-configurable host interface is offered.

Software design is really the only element that could be tricky in transferring some storage from magnetic to optical. Optical storage should not present major problems when used only as backup for

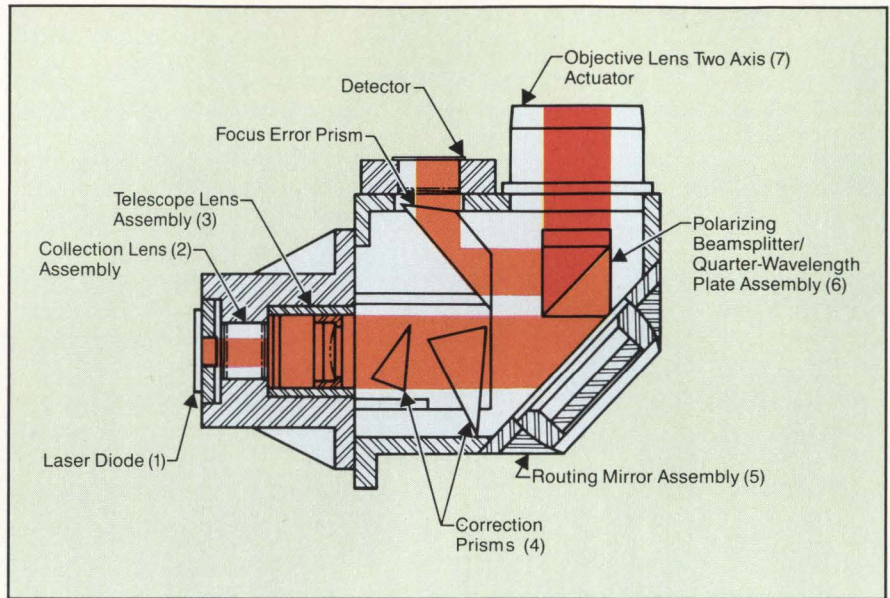


Figure 5: The numbers associated with parts of Optimum's laser read/write head indicate the order in which light passes through them; the recording medium would be at the top of the illustration.

magnetic media. But to use optical and magnetic recording simultaneously requires a clear understanding of how the format of data on the optical record differs from that on magnetic tape or disk.

As erasable optical systems become commercial, users will have the choice of magnetic or optical. Features that will make optical systems attractive include high capacity removable disks and the small effect of dirt and dust on error rates. The goal is for units to be capable of recording either write-once or erasable disks. With two types of recording possible, these future optical drives may be more flexible than magnetic drives.

Erasable Optical To Compete

In addition to the improvements in technology for WORM and ROM optical storage, the next few years will bring the industry closer to erasability. Only Matsushita now claims that they have a material and method that is effective for erasable and rewritable optical storage.

There are two types of optical processes that lend themselves to erasing and rewriting: one involves a combination of optical and magnetic technology, called magneto-optic; the other is based on a phase change in the sensitive material from crystalline to amorphous. It is difficult to get a strong enough signal from a magneto-optic device for it to be reli-

ably detected at reasonable carrier to noise (CNR) levels. Phase changes tend to take longer than is practical for data recording, and several write/read cycles tend to permanently deform the surface.

The Matsushita erasable optical storage system uses phase changes in tellurium with submetals added for reversibility. Two lasers are used for the system. A single lens for the two lasers allows nearly simultaneous erasing and recording (Figure 6).

Most in the optical industry contend that magneto-optic is more promising for commercial erasable systems. This technique uses optics to sense the effect of a magnetic field on a laser beam returning from the magnetized disk. Magneto-optic technology displays very good cyclability and data retention.

The current research is targeted on finding materials that do not lose their coercive force (strength of holding magnetic field) after repeated write cycles. Methods of increasing the Kerr rotation (the light quality actually sensed) are also under study, so signals can be discerned from noise. SNR will need to be improved for recording density with magneto-optics to compete with phase change.

Several companies are working on this combination optical/magnetic recording. The consensus seems to be that multiple layer recording through glass and metal layers to a rare earth transition metal sen-

sitive layer holds the promise of efficient magneto-optic data recording.

When methods of erasing become available, optical drives will compete with magnetic drives. But the place for non-erasable optical recording will not be threatened. In fact, most of the erasable drives will probably be made by the same firms as the current WORM and OROM devices. New drives will likely read non-erasable disks as well.

Though the density and environmental immunity of erasable optical recording may give it advantages over floppy drives and the removability should give it an edge on Winchester, it probably will not replace magnetic storage altogether. The sheer quantity of data now on magnetic disks and tape will keep the market alive.

Improving Optical Storage

In bringing optical disk drives to the market, concentrated development work has been devoted to focus and tracking and error detection/correction mechanisms. The raw bit error rate (BER) of optical data storage disks is between 10^{-5} and 10^{-7} , not nearly good enough for archives. These are about the specs for video disks; audio disks are corrected to about 10^{-8} or 10^{-9} . But these only need to be as sensitive as human hearing and sight demand. Sophisticated error correction codes (ECC) used on all of the commercial drives lower the BER to 10^{-12} in the 12" products. To match the high performance of their system, STC's 4 Gbyte platters show 10^{-13} BER.

As for focus and tracking, the pre-grooved tracks and DRAW head have been critical in developing working products. The schemes are effective, however,

at the expense of heavy read/write heads. Some advanced work in holographic and integrated optical components could make optical heads lighter. This is several years away, but could provide the possibility of transportable optical drives.

Transportability again brings up the issue of size. Smaller form factor drives will be appearing close on the heels of the current class of drives. Most companies with products announced will admit that 5¼" and smaller disks are under study, and the new companies popping up are strong evidence of the trend toward this size optical drive.

As with other storage devices, there will be a variety of sizes and capacities to serve various computer systems. Optical drives from jukeboxes to 3" single disk systems will all find markets. Companies like Drexler Technology (Mountain View, CA) are working on alternative formats; in their case, it is a card. Optical tape cassettes have been developed by DOCdata (Venlo, The Netherlands). They have shown a prototype carousel similar to disk jukeboxes. There has also been study of spherical surfaces, in which the head would not have to move. Beam deflection methods have been most cumbersome, however.

Developments in lasers could be a huge factor in optical data storage systems. With shorter wavelength lasers, data packing density can increase. To increase data rates, lasers about 10 times as powerful as those used now, or about 100 mW out, would be ideal. Laser lifetimes could stand improvement, as could their immunity to electrical interference.

A particularly interesting possibility is the use of several diode lasers in an array

for optical recording. RCA has developed a head using a 10-diode monolithic array. This would allow either much higher data rates or simultaneous multiple track seeks. A good lens can see 100 tracks, so this method would allow moving only the laser beam and not the head.

Critical in all of the developments in optical data storage devices will be compatibility. The companies in the field have made a major commitment to the technology and will no doubt make increasingly sophisticated drives. Downward compatibility of future models with older models will be critical. With the similarity in current write-once and erasable recording technologies, manufacturers hope to develop erasable systems that will also read non-erasable disks.

Conclusion

Improvements in magnetic recording will keep users' capacity needs satisfied for some time. Future development of erasable optical storage could bring the technology into competition with magnetics. At that point, the technologies and markets will dictate where each is used and whether optical storage will replace magnetic.

These first non-erasable optical storage drives do not compete directly with existing magnetic drives, however. As the differences between WORM and OROM non-erasable and any sort of erasable media become clear, optical storage could find a niche in the archiving and electronic publishing and database distribution markets.

The sheer capacity of a single optical disk will allow entire software systems to be put in one place and distributed or mailed. Storage of documents and large files will be greatly facilitated, and initial jukebox systems are being tested for document storage in the Library of Congress.

Optical storage will be another peripheral to accompany magnetic disk and tape drives for the next couple of years. Once the uses and requirements for the WORM and ROM optical systems are realized, this new class of computer peripherals will become more significant. □

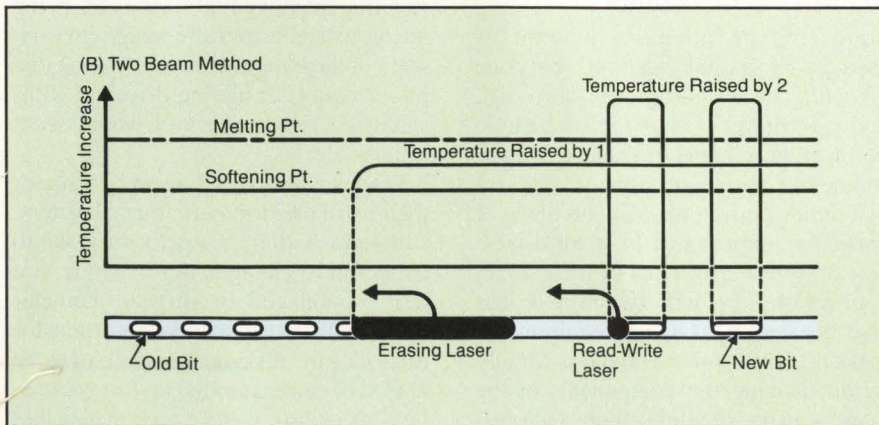
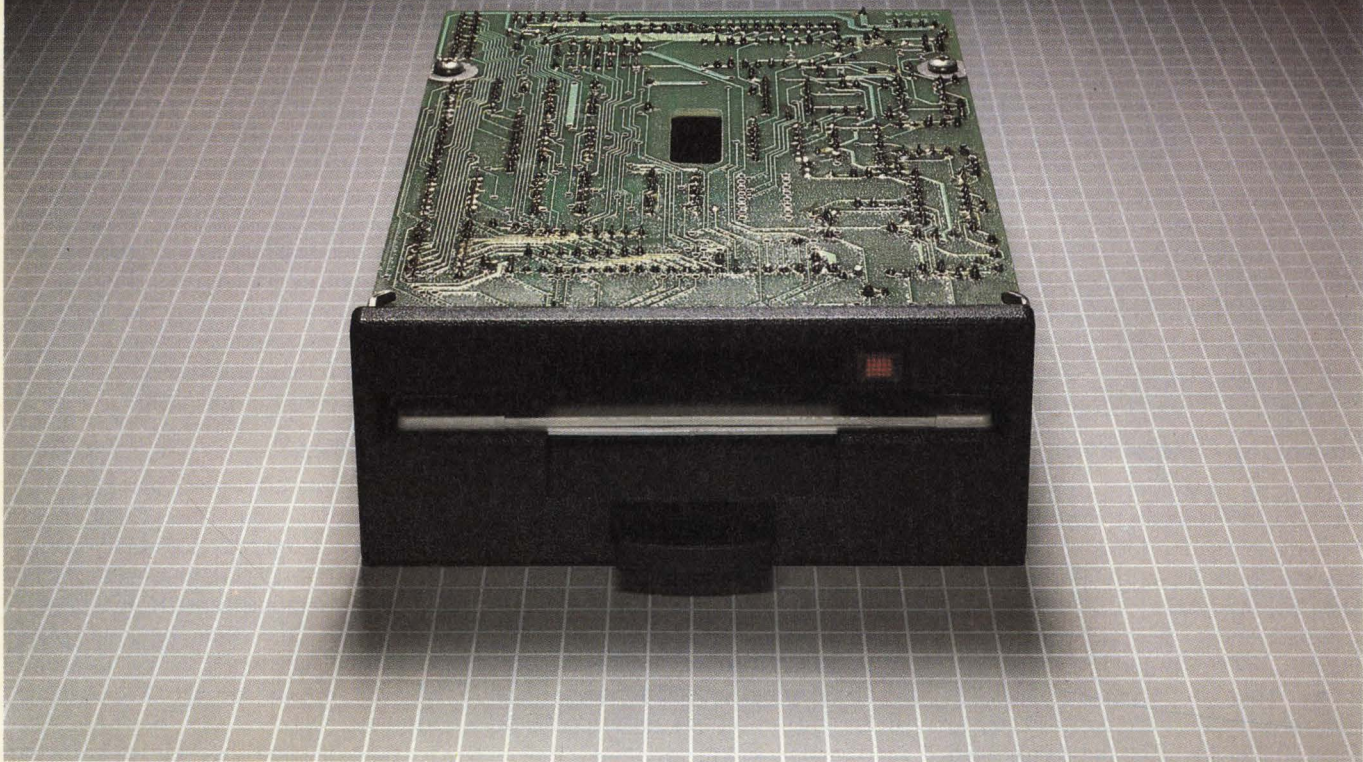


Figure 6: Matsushita uses two lasers; a large spot lower-power erasing laser heats the tellurium alloy to the softening point; the read/write laser produces a smaller spot that raises the material temperature to melting.

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Mass Memory For Tight Spots



by **Bob Hirshon, Contributing Editor**

Business computer manufacturers are fond of saying that the most valuable real estate in America is the executive's desk-top. As notebook-sized computers become more powerful and popular, the real estate inside his briefcase is becoming equally valuable. Personal and portable design and test systems are now doing the same for the property values of engineers' desk-tops and briefcases.

Rotating memory is a key constraint in downsizing small computers to answer this demand. Because disk and tape drives are electromechanical devices, it is especially difficult to reduce their size and their power requirements. As electromechanical devices, they are more susceptible to shock and vibration — an

Bob Hirshon is Contributing Editor, Peripherals, of Digital Design and Editor-in-Chief of Memory Update (78 Oldham St., Pembroke, MA 02359. 1-800-962-2001), a news journal of mass memory technology.

important consideration for computers intended for travel.

Nonetheless, more and more companies are meeting these challenges and introducing miniature rigid disk drives, flexible disk drives, and tape drives designed for the confines of small personal, portable and even notebook-sized computers.

Small Considerations

Squeezing an adequate amount of capacity into a small footprint is only one difficulty in designing downsized disk and tape drives. Other factors include power requirements, resistance to environmental stress, and cost.

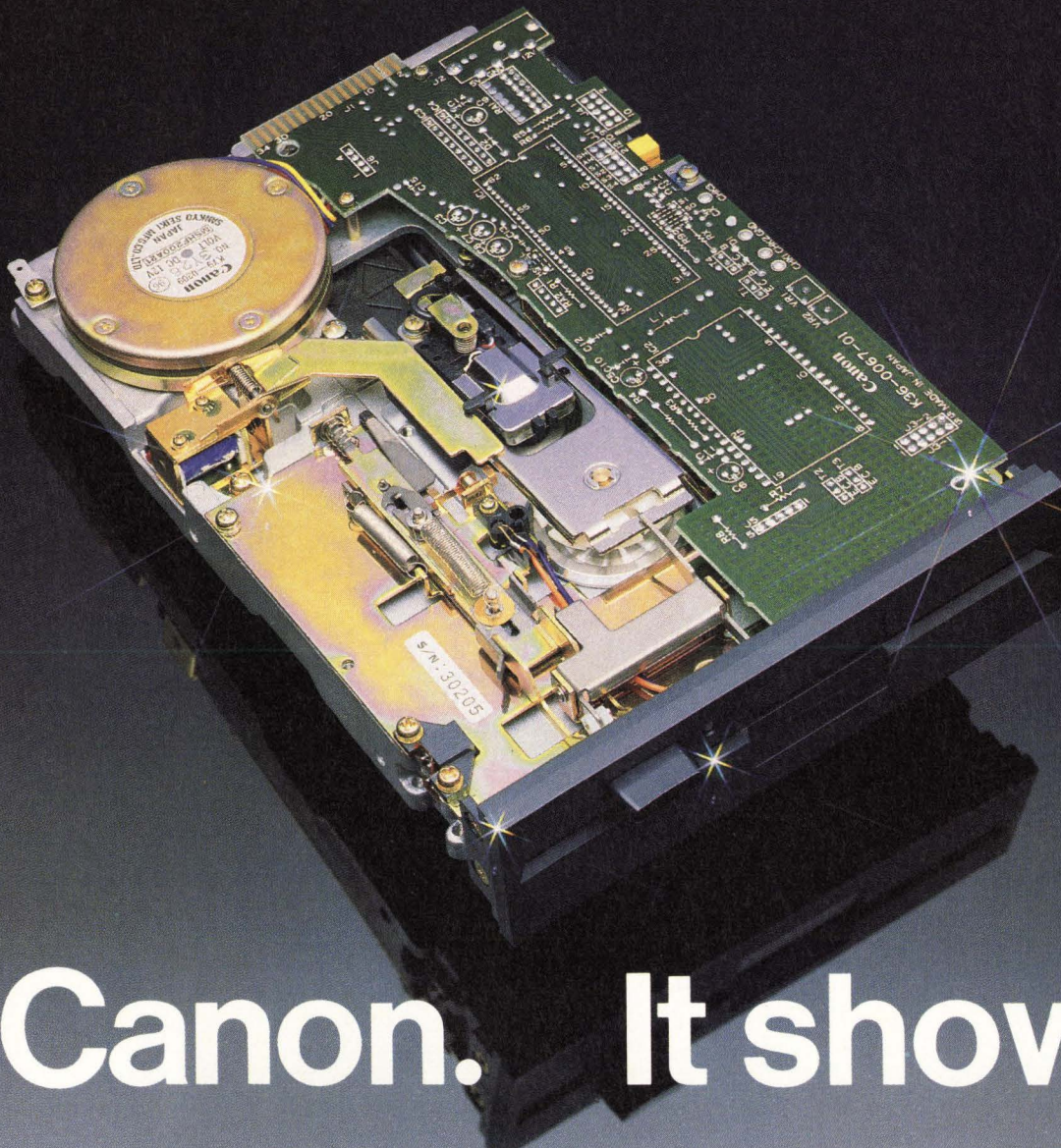
Keeping power requirements low is of particular importance in small drives. Not only because many of their target applications are battery-powered, but also because tight space requirements make heat dissipation a problem. Merely by downsizing the components of the drive — using smaller spindle and positioning motors, for instance — power is reduced. In addition, the use of CMOS-based electronics, although costly, is

Figure 1: Microflopies are currently offered that use 3", 3.25", and 3.5" media. The 3.5" drives, like the Shugart drive pictured, are to date the most popular.

necessary for portable applications.

Environmental stress is also of special importance for portable applications. Rotating memory is notorious for being unable to handle even the benign environment of the computer room. Taking that into account, designing drives to withstand the rigors of travel would seem impossible.

Downsizing drives, however, increases their resistance to environmental factors. Problems with media deformity due to temperature changes, for example, are less pronounced in smaller diameter disks. This is especially important for microfloppy diskettes, which may be mailed or carried around in shirt pockets. Less recording surface area means less chance of surface contamination from particulates, both for microflopies and 3.5" Winchesters. And the shorter,



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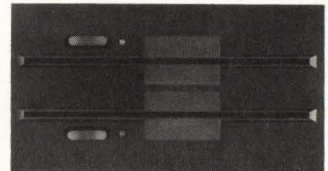
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Standard half-height bezel



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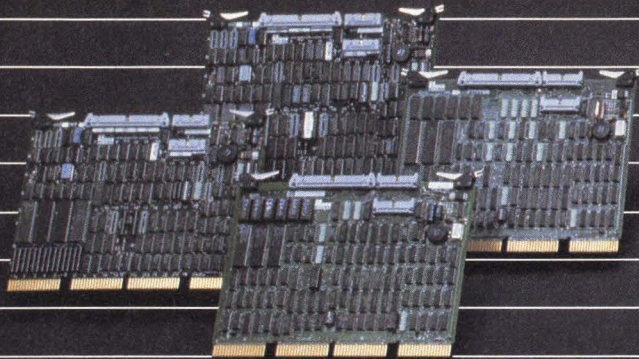


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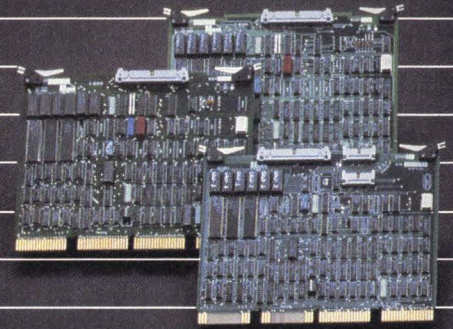
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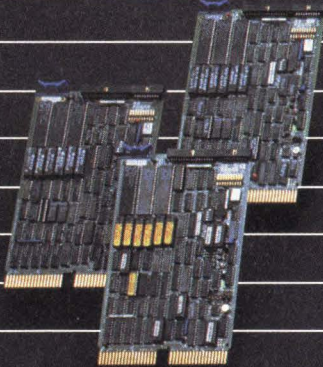


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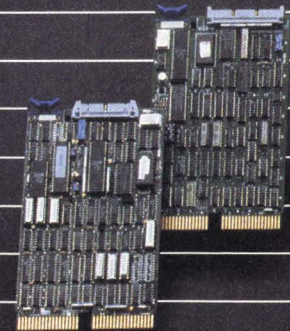
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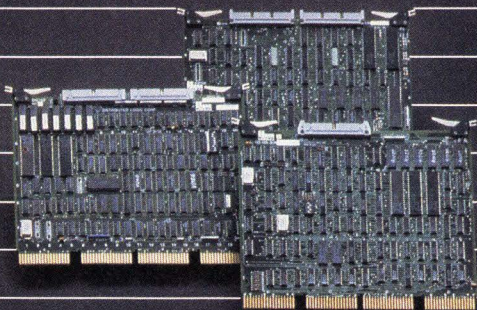
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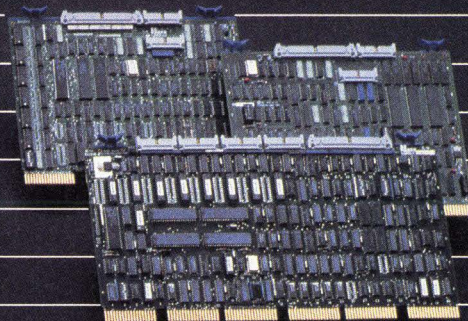
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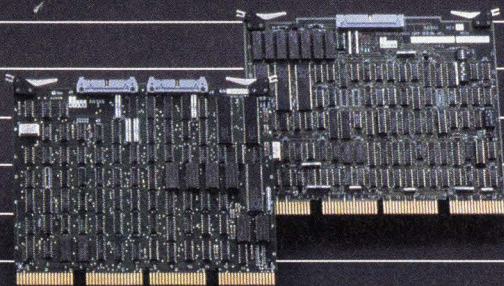
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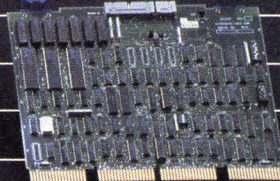
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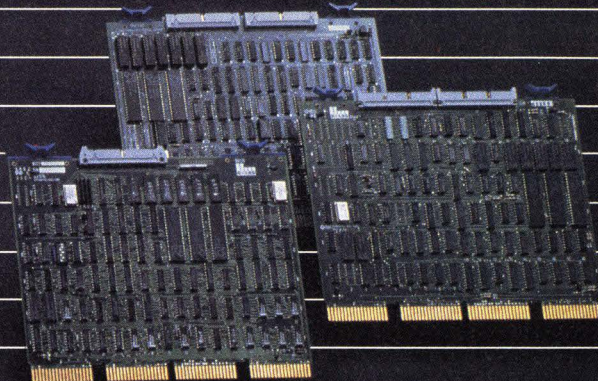
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Demand for higher performance portable computers and more compact desktops has spurred a demand for smaller, lower power disk and tape drives.

lighter, more rigid R/W head armatures used in the smaller disk drives are less susceptible to vibration and shock.

Cost is an important factor in all mass memory devices, but it is especially important with miniature memory devices. This is because the same applications that call for tight constraints on size call for tight constraints on price. Portable computers and knee-top computers must remain below strict price ceilings to be competitive. This means that the total cost allotment for mass memory in these computers ranges from about \$150 to \$800.

Consequently, price, not state-of-the-art technology, determines the performance level of miniature memory components. High-performance, high-capacity drives can easily be built, but their price would be a substantial percentage of the total system cost. The challenge is designing drives of adequate capacity and performance, priced low enough for portable applications.

Smaller Rigid Disks

Two years ago, high capacity 5.25" micro-Winchesters attracted considerable attention at NCC. Last year, half-height 5.25" drives did likewise. This year, the spotlight is on 3.5" Winchesters.

The class "3.5"" is a general term for Winchesters with a faceplate measuring 1.625" high by 4" wide (the same as that of microfloppy disk drives). The platters on 3.5" Winchesters vary in diameter, but are generally about 3.75". Seagate, Miniscribe and several media manufacturers proposed standard physical dimensions for the media last year, which most U.S. manufacturers may eventually adopt. Media manufacturers, however, are willing to supply media of any dimension provided there is sufficient market, and

since there is no interchangeability question with fixed Winchester disks, there's far less need for a standard than with other memory media (such as flexible disk and tape).

For space-constrained memory applications, half-height 5.25" Winchesters may also be suitable. With a faceplate measuring 1.62" by 5.75", and a length of about 8", they may be somewhat large for notebook computers, but ideal for small desktops and portables. U.S. companies now offering half-height 5.25" drives include Cogito Systems, Microcomputer Memories, Inc. (MMI), Microscience International, Miniscribe, Quantum, Seagate, Shugart, Tandon and Tulin.

Half-heights have a number of advantages over 3.5" drives that will keep them popular in applications where smallest possible footprint isn't the overriding concern. The most important advantage is that half-height drives are a more established technology, having been manufactured for a longer time by more companies. They use many of the same readily available, standard components used in full-height Winchesters. Also, because they have more disk surface area, they can easily accommodate higher capacities. Until 3.5" Winchesters mature, half-height 5.25" drives will continue to fill many space-constrained, portable computer applications.

Sizing Up The Sub-4" Drives

The first sub-4" Winchester introduced was SyQuest Technology's 3.9" removable cartridge Winchester, announced in May of 1982 (Figure 2). Although the media is 3.9" (100mm), the form factor of the drive is half-height 5.25". It wasn't designed to fit the industry standard sub-4" form factor because it was announced before there was an industry standard.

As a non-standard drive using unique media, the SyQuest drive took a long time to move into volume production, and a long time to gain market acceptance. Now that SyQuest has ramped up, they have a sizeable backlog, and they claim to have shipped 35,000 of the drives. In addition, they are manufacturing 25-Mbyte and 38-Mbyte half-height fixed-disk drives, and are developing a 10-Mbyte removable cartridge.

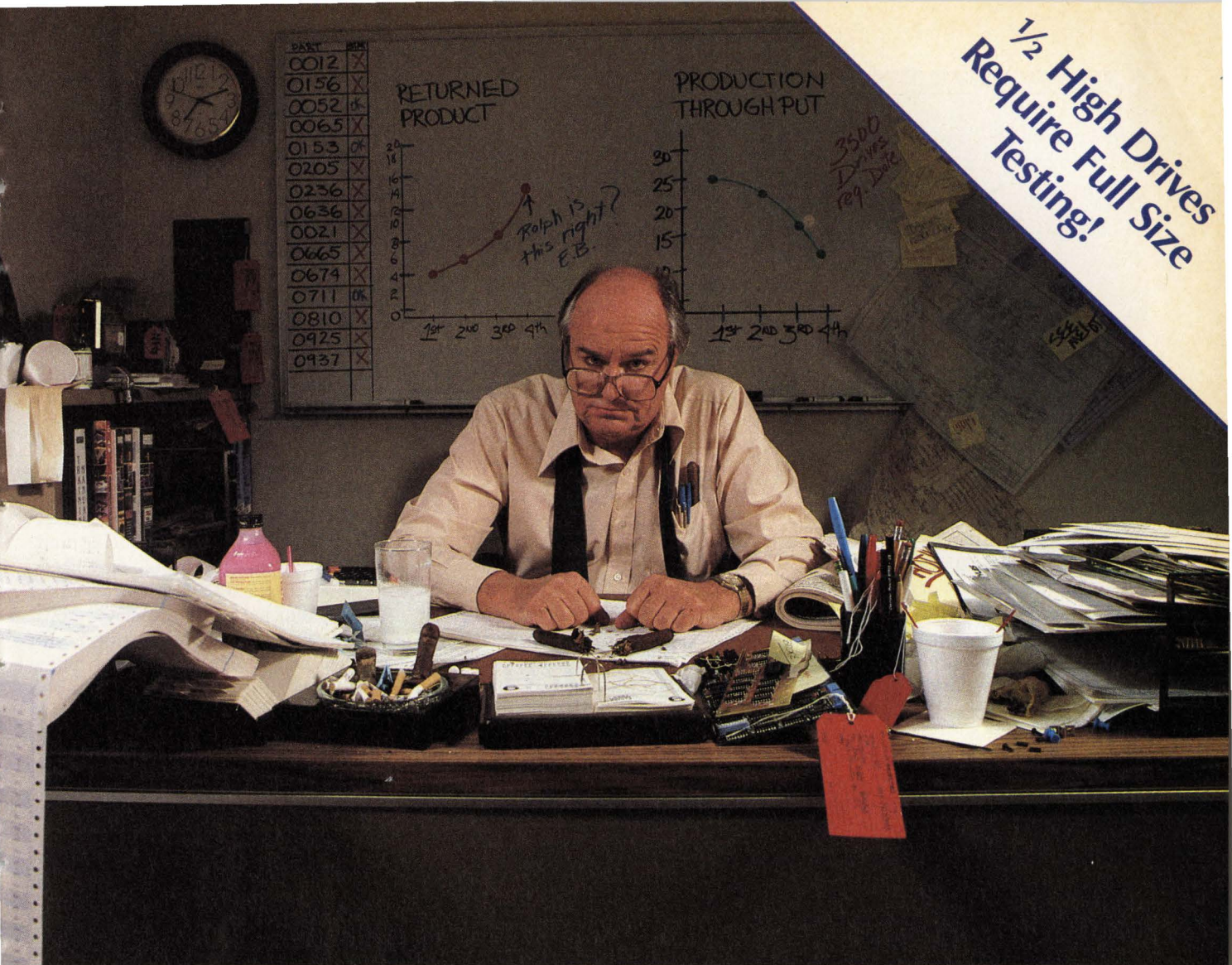
The first company to offer 3.5" Winchesters was Rodime plc (Glenrothes, Scotland). Announced in January of 1983, their RO 350 series includes 5- and 10-Mbyte (formatted) versions using oxide media and ferrite heads. Their open loop positioning system is precise enough to record at 600 tracks per inch (tpi), and has an average access time of 85 msec.

The market for 3.5" drives over the past year was small, but Rodime's 350, being alone in the field, managed to attract a number of contracts. These include Compaq, TeleVideo and, most recently, Applied Computer Techniques, who designed the Rodime drive into their new Apricot executive portable computer. To keep up with this demand, and to minimize shipping costs to U.S.-based customers, Rodime recently opened a production facility in Boca Raton, FL. By ramping up production quickly in Boca Raton, Rodime hopes to maintain a leadership position in 3.5" Winchesters, despite the entry of a number of U.S.-based manufacturers.

The first U.S.-based disk drive manufacturer to introduce a 3.5" Winchester was Control Data Corp. (Minneapolis, MN). Their 5-Mbyte Cricket was introduced at last year's NCC, but then was withdrawn. CDC claimed that their market research found the Cricket to be too slow (117 msec average access time) and too low capacity to compete effectively.

Figure 2: SyQuest's 306RD was the first Winchester to use sub-4" media. The 100mm disk cartridges currently store 5 Mbytes; a 10 Mbyte version is planned.





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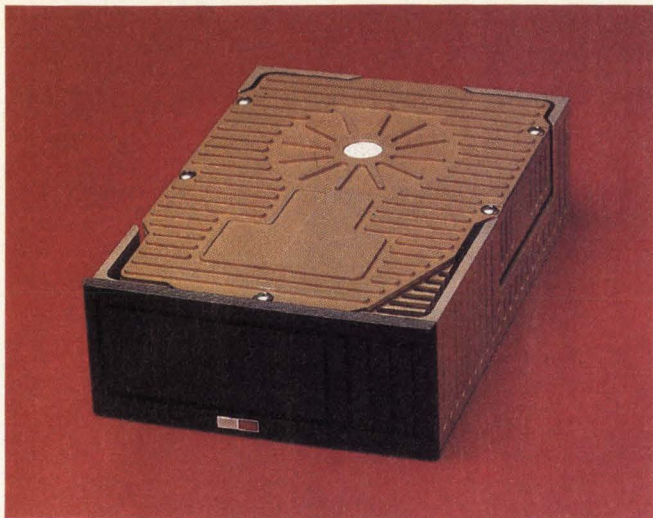


Figure 3: A new company offering 3.5" Winchester disk drives is LaPine Technology. Their Ranger series stores up to 10 Mbytes (formatted) and withstands shock of up to 100G in a non-operating condition.

They have been working on a higher-performance, higher-capacity model ever since, but introduction of that drive has been delayed indefinitely.

Meanwhile, at least a half-dozen other companies have either announced 3.5" drives, or have announced plans to announce 3.5" drives. These include LaPine Technology, Microcomputer Memories, Inc. (MMI), Microscience International, Miniscribe, Seagate Technology, and Tandon. In addition, Hewlett-Packard and a new start-up company called Epelo are developing drives.

Most of the initial offerings are 5-Mbyte to 10-Mbyte drives with open loop, stepper motor positioning. Higher-capacity, higher-performance drives with closed-loop, voice coil actuated positioning are promised from some of the companies.

LaPine Technology stresses ruggedness as the major advantage of their Ranger series of drives (**Figure 3**) over the rest of the pack. "You can throw this drive in the back of your car," claims one LaPine spokesman. With power off, the Ranger drives withstand a shock of 40G; with optional external shock mounts, this is increased to 100G. Power off temperature range is -40°F to 158°F . During operation, the drives can tolerate temperatures of 40°F to 122°F .

MMI offers a pair of 3.5" drives similar to LaPine's, as well as a half-height 5.25" drive. Both LaPine and MMI introduced their 3.5" Winchesters several months before NCC, avoiding the stampe of similar products announced by other drive manufacturers. Both companies plan to get an early lead in low-performance 3.5" Winchesters and then, when the arena gets glutted with manufacturers, bring out high-performance versions with 30 Mbytes to 50

Mbytes and sub-40 msec access times. This formula of addressing immature markets by using advanced technology, keeping slightly ahead of the larger, more conservative disk drive manufacturers, worked well for a number of start-up 5.25" and half-height 5.25" drive makers. LaPine and MMI will try the same strategy with 3.5" drives.

Another company keeping one step ahead of the big drive companies is Microscience International. They were an early manufacturer of low-capacity half-height 5.25" drives. As more companies entered the market, they introduced a higher-capacity version of the half-height (20 Mbytes). Now, as more firms are entering the 20-Mbyte half-height 5.25" Winchester arena, Microscience has announced a 10-Mbyte 3.5" drive.

A new company, Epelo, is developing a high-performance high-capacity (50-Mbyte) disk drive, for introduction next year. Former Atasi CEO Frank Gibeau is directing the effort.

Large Companies Enter Market

With high-performance 5.25" drives, the large Winchester manufacturers lagged far behind the smaller firms. With 3.5" drives, however, several big drive makers are only a step in back of the start-ups. While high-performance, high-priced 5.25" drives have a limited market, distasteful to companies geared for high volume, 3.5" drives have the potential to be commodity items. Therefore, the large companies have no intention of letting the start-up firms deprive them of market share, even if it means announcing products earlier than they would have liked.

Miniscribe and Seagate, two leaders in 5.25" Winchester drives, have shown their first 3.5" products, storing 10-Mbyte, and Tandon is expected to follow suit. Hewlett-Packard is also working on a 3.5" Winchester, to serve as an upgrade to the 3.5" microfloppy it now offers on its desktop computers. HP also is expected to offer the drive to OEMs.

Microflops Mature

Sub-4" flexible disk drives are more mature technologically by about a year than sub-4" Winchesters. Three different media types are offered — 3" hard shell, 3.25" flexible jacket, and 3.5" hard shell — and although the 3.5" hard shell is by far the most popular, the other formats

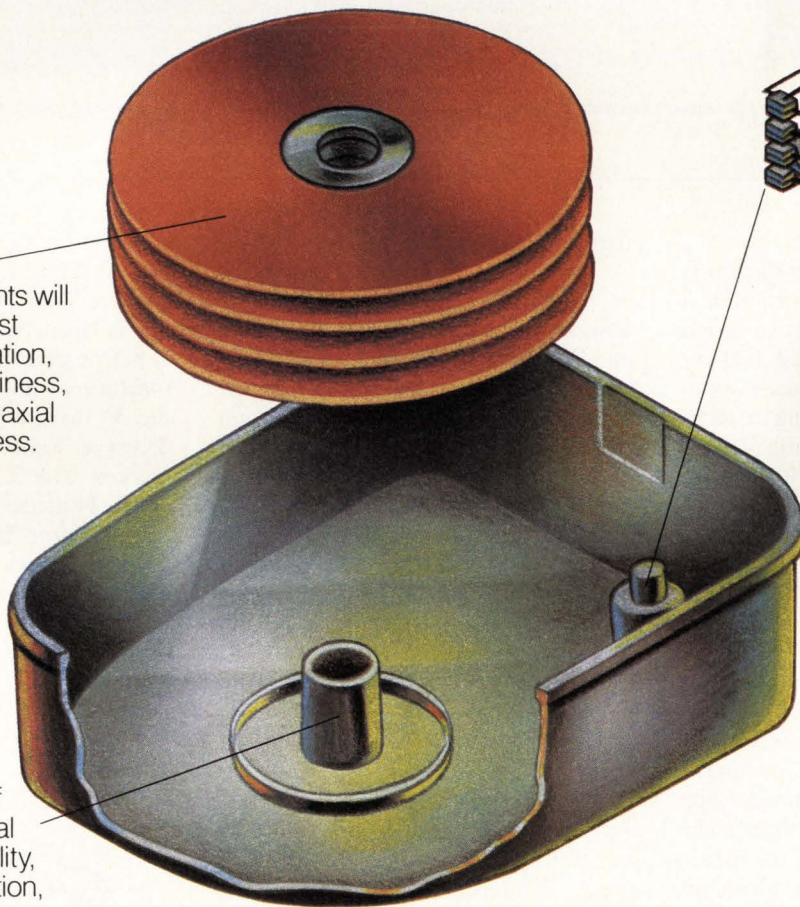


Figure 4: The Irwin Magnetics 210 tape drive fits into a 3.5" footprint and stores 10.38 Mbytes on a single minicartridge tape.

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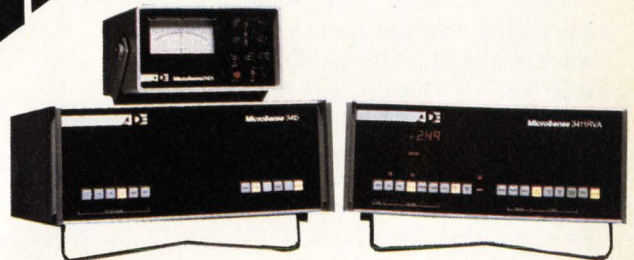
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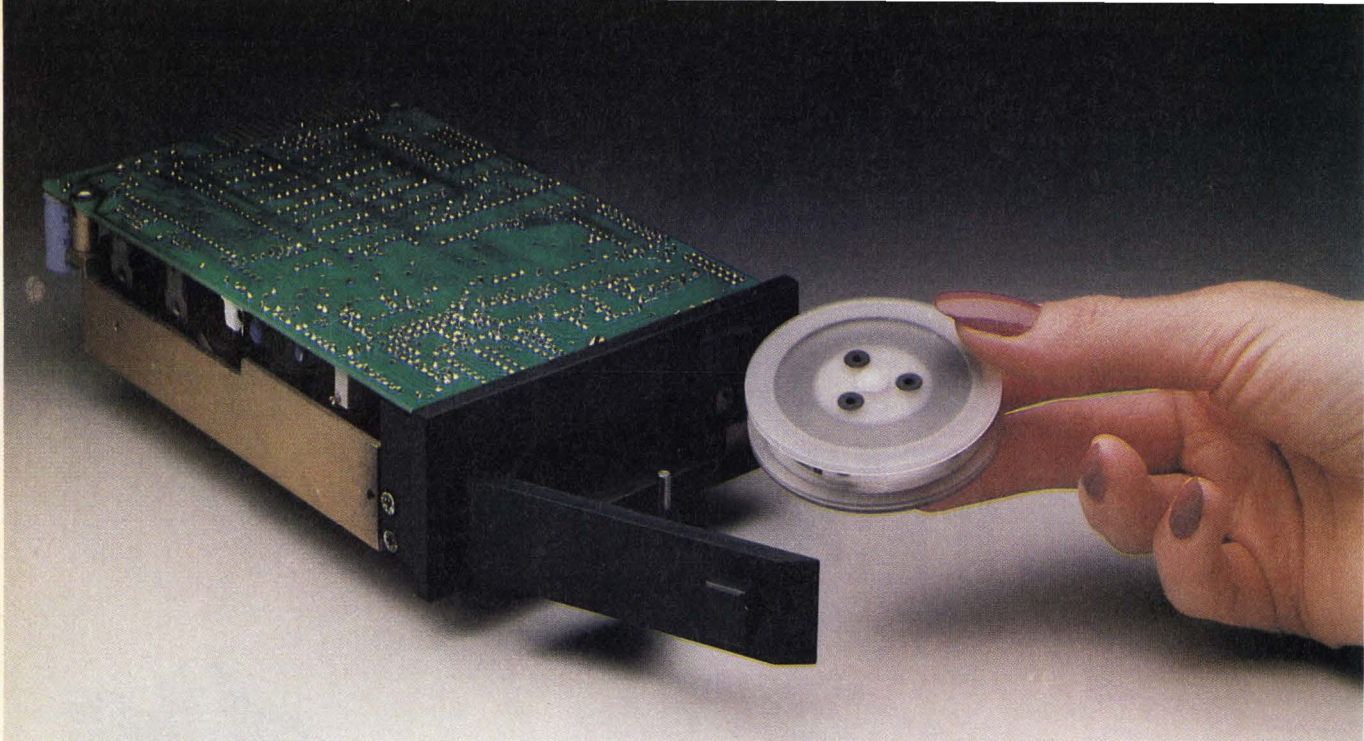


Figure 5: Interdyne's ID 1000 series fits into a standard 3.5" footprint and stores up to 20 Mbytes on a reel of quarter-inch tape, and 40 Mbytes on a reel of half-inch tape.

still have their following.

Last year, when drive manufacturers failed to get a unanimous decision on a microfloppy media standard and ended up with three different formats, industry analysts predicted that the market would decide the question, comparing the technical merits of each format and picking the winner. "The market is a lot smarter than you might think," said James DeStefano, Dysan Business Strategist. The comparison used to describe the situation was the videotape market, in which Beta-format and VHS-format tape cartridges vied for the market, with VHS ultimately dominating, based on a number of technical advantages.

The microfloppy market, however, has proven far different. Buyers of microfloppy drives, unlike buyers of videotape equipment, care little about slight technical advantages, as long as the drives function reliably and are available in quantity. The number of companies supporting a standard, and the reputation of those companies, is the most important consideration of large volume OEMs.

As a result, the 3.5" hard shell format has clearly emerged as the leader. This was not a result of the market deciding that the 3.5" format was technically superior — all of the formats are serviceable, and each has its advantages — but rather a result of the majority of drive manufacturers supporting one format, the users favoring the drive with the most

industry support.

Over a dozen manufacturers now make 3.5" microfloppy drives, most notably Shugart (Figure 1) and Tandon. Apple and Hewlett-Packard are the two major buyers of the drives, and IBM is expected to join them shortly, incorporating them into a transportable computer. But small computers may be only one of many applications for the microfloppy. "3.5" microflops will be used in many applications other than computers," predicts Shugart spokesman Jim McCartney. "For example, they will be incorporated into telephone and television-based systems, storing directories, and even into cars, storing maps for navigation systems."

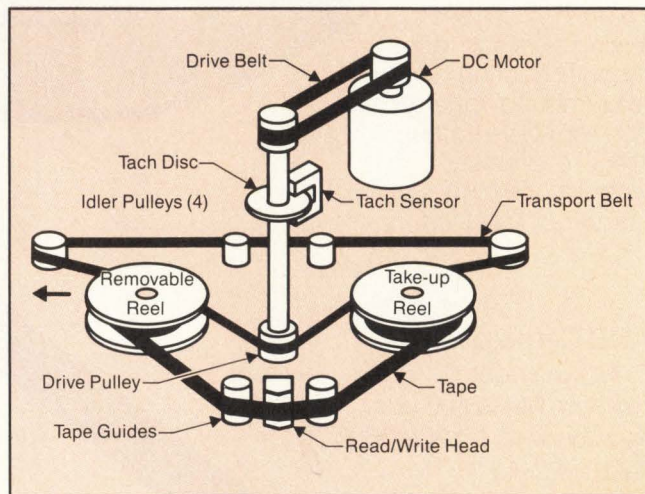
The other two microfloppy formats are

suitable for the same range of applications as the 3.5", but to date have limited support. The 3" hard shell format is popular in Japan, but has fared less well in the U.S. Consequently, some Japanese manufacturers who initially supported only the 3" diskette now are offering 3.5" drives as well, to compete in the U.S. market. The 3.25" format, supported chiefly by media-maker Dysan and drive-manufacturer Tabor, remains a viable product, thanks to Dysan's promotional efforts. But even Dysan has announced that they will also support the 3.5" format if the market demands.

Tape Fits Back-Up Role

No Winchester manufacturer questions

Figure 6: Interdyne claims their self-threading tape transport system has performed over 150,000 loads without a failure.



the importance of backing up data recorded on fixed disk drives, but few address the problem. This is especially true of small Winchester drives.

The first Winchester drives introduced in a given size category generally are used as floppy disk upgrades, offering greater performance and approximately 10 times the capacity. Back-up for these drives is usually accomplished by pairing the drive with a flexible disk drive. But as higher-capacity Winchesters in the same size category are introduced, flexible disk drives become inadequate for the task. At this point, designers must turn to magnetic tape or removable disk cartridges to serve as back-up.

For 5.25" Winchesters, quarter-inch cartridge tape drives provide an answer to high-capacity back-up needs. Clever packaging has even allowed the design of half-height quarter-inch cartridge drives; the drives are not much larger than the media they contain. But no amount of ingenious packaging can produce a quarter-inch cartridge drive for a 3.5" footprint — the media itself is considerably wider than the 3.5" drive faceplate. Therefore, designers looking for tape back-up in a 3.5" drive footprint must look to other technologies.

Minicartridges, which are smaller versions of the quarter-inch cartridges, are small enough for use in a 3.5" footprint tape drive. The only company offering a product for this purpose thus far is Irwin Magnetics.

The Irwin 210 (Figure 4) stores 10.35 Mbytes on a DC-100A minicartridge. It operates in streaming or start/stop modes, and can dump or restore an entire tape in eight minutes (streaming). The 210 draws 14.5W of power and weighs 1.7 lbs. — both about the same as a 3.5" Winchester. Dimensions are 4" by 6" by 1.688" high, again about the same as a 3.5" Winchester, although addition of the electronics card adds about 0.25" in height. The 210 uses a standard minifloppy interface (SA 450), and can be connected in a four-device daisy chain.

Another type of tape drive specifically designed for 3.5" Winchester back-up has been announced by Interdyne. Their ID 1000 family consists of drives that use a 2.25" reel of magnetic tape, and stores 5 Mbytes, 10 Mbytes, or 20 Mbytes per reel, using quarter-inch tape, and 40 Mbytes using half-inch tape (Figure 5). The drives operate in streaming as well as random access modes.

Interdyne uses a self-threading tape transport which they claim has performed over 150,000 loads without a

failure (Figure 6). The drives measure 4" by 6" by 1.625", weigh 1.4 lbs., and draw 8.5W. Interface is via standard minifloppy SA 450/SA 300 "The ID 1000 family interface is truly a floppy interface," stresses Interdyne's Paul Gillovich, "using a Dysan PAT-II floppy tester for product assurance."

Finally, cassette tape is well-suited for 3.5" Winchester back-up, and the companies now offering cassette drives in half-height 5.25" formats can be expected to bring out 3.5" format versions in the near future.

Forecast Bright and Unsettled

The future of miniature memory components is bright, but uncertain in some of the low-capacity applications, primarily because of the advent of high-density semiconductor memory.

Intel's introduction of an entire family of low-power CHMOS dynamic RAMs, for example, could eventually have a profound effect on portable computer applications. At \$150 per part, these RAMs currently have no impact on price-sensitive portable computers. But as prices come down, this may change. According to Intel, a study performed by Montgomery Securities predicted that by 1988, 1 Mbyte of dynamic RAM, consisting of 32 256K chips, will cost about \$200. It is possible that by then, most portable computers will use semiconductor memory, rather than magnetic memory. In fact, semiconductor memory may fill many primary storage needs, with magnetic storage used as non-volatile back-up.

Nonetheless, the growing need for higher-capacity memory for memory-intensive operating systems, such as UNIX, and for memory-intensive applications, such as computer graphics, will still require magnetic memory. And magnetic memory still has plenty of technological room to grow. In the not-too-distant future, improved media, high-density recording techniques (including vertical recording), and improved positioning systems will allow capacities of over 100 Mbytes in a 3.5" footprint, and access times under 20 msec. Miniature memory components have come a long way in recent years, but clearly they have far to go before reaching their technological limits.

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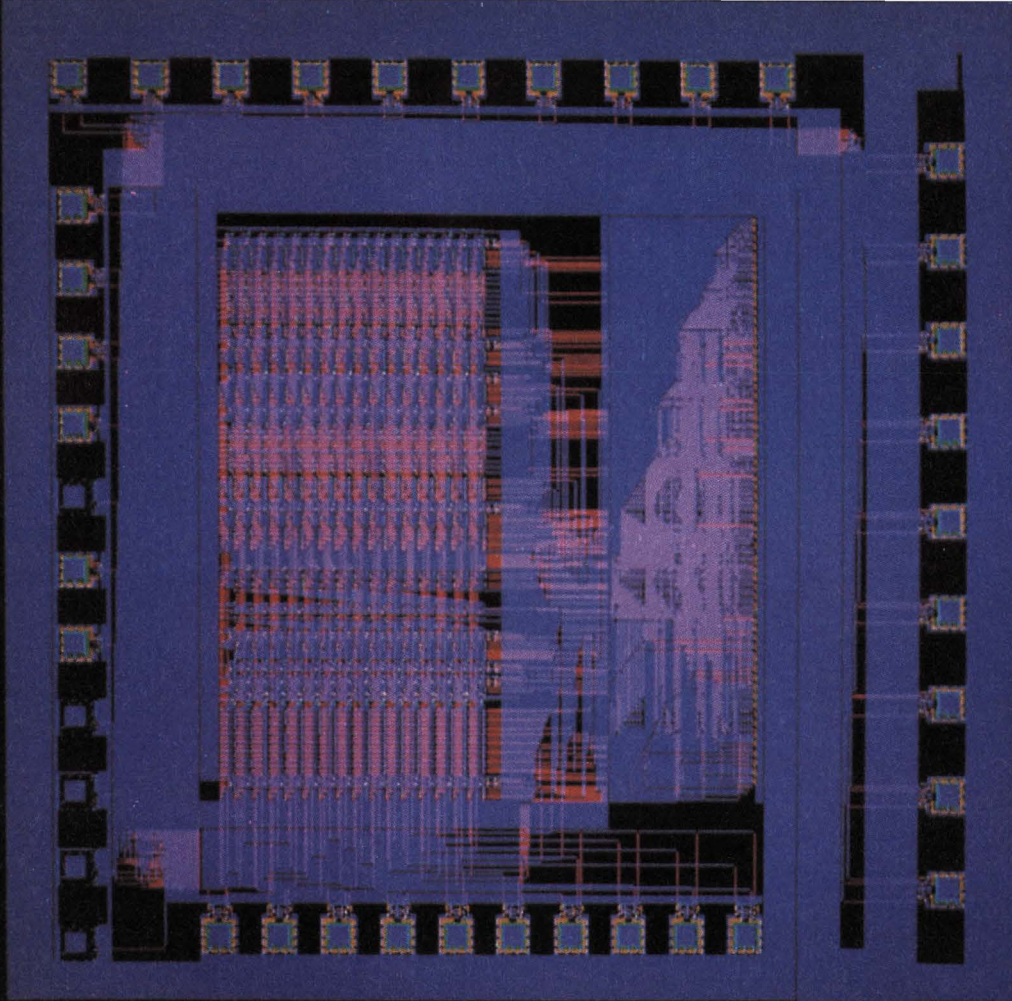
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Silicon Compilation: A Revolution In VLSI Design

by Ronald Collett, Technical Editor

Until recently, a system that automatically synthesized complex VLSI chips with minimal human intervention was wishful thinking. However, several research laboratories and a few vendors have been quietly engaged in the development of this ultimate IC design tool—a silicon compiler. Not surprisingly, silicon compilation promises to have dramatic impact on the entire electronics industry.

To fully appreciate the power of a silicon compiler, compare it to a Fortran compiler and the difference between writing a program in Fortran and writing that same program in machine language. With the Fortran program, the compiler converts the high level instructions to machine language. Similarly, a system

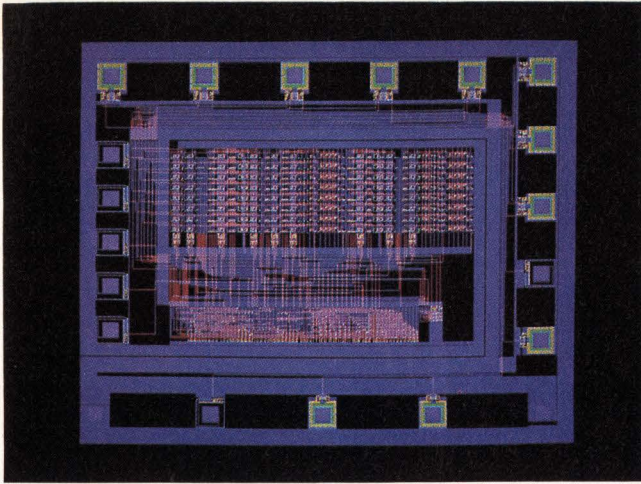
*The expanding
application-specific
integrated circuit
market has spawned
a new generation of
tools that automate
VLSI design.*

architect describes the operation of the chip in a high level language and the silicon compiler automatically synthesizes the masks necessary to fabricate the chip.

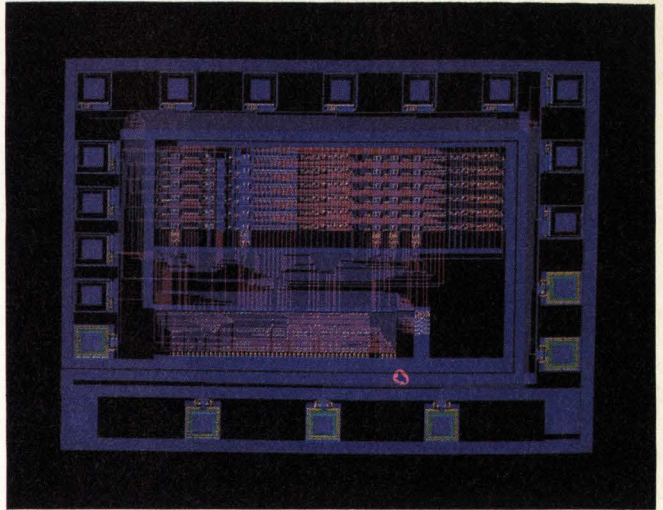
Forces Driving Silicon Compilation

Handcrafted full-custom chips typically require one to two years to develop, with costs ranging from \$200,000 to \$1 million. In addition, only a few highly specialized engineers have the skills necessary to design a full-custom chip. To make matters worse, high volume and a wide market window are two criteria for the profitability of a handcrafted IC. If these parameters are questionable, the development of a custom chip is often too risky.

Lengthy design cycles, high costs and shortages of chip designers have given impetus to other methodologies that facilitate the design of application-specific integrated circuits (ASIC). Among the various ASIC alternatives, semi-custom ICs (i.e. gate arrays and standard cells)



Left: This 16-bit, "Fanatically Reduced Instruction Set Computer," (FRISC) was designed by Metalogic's silicon compiler. Above: This simplified Universal Asynchronous Receiver/Transmitter (UART) was also designed with Metalogic's silicon compiler.



Using Metalogic's silicon compiler, this Automatic Gain Control (AGC) chip was designed in less than three weeks by a digital systems designer who had no previous IC design experience.

are spearheading the migration away from off-the-shelf components. Unlike full-custom, semi-custom and silicon compilation allow logic designers to use their current skills to build chips. The latter is based on a different design philosophy and until now, has been confined to the research lab.

Absolving the design engineer from transistor layout tasks is the primary benefit of a semi-custom chip. For instance, imagine a particular design having 25 blocks (from a block diagram) which corresponds to 5000 gates, translating to 12,000 transistors—equaling nearly 250,000 polygons. With semi-custom, the design engineer would be responsible for managing and implementing only the block and gate level data. In addition, turn around times for these parts typically span six to 20 weeks with non-recurring engineering (NRE) costs ranging from \$5,000 to \$75,000. In comparison to full-custom handcrafted designs, there is little doubt that gate arrays and standard cells have overwhelming advantages. However, semi-custom design forces the system architect to become entangled in circuit and logic design.

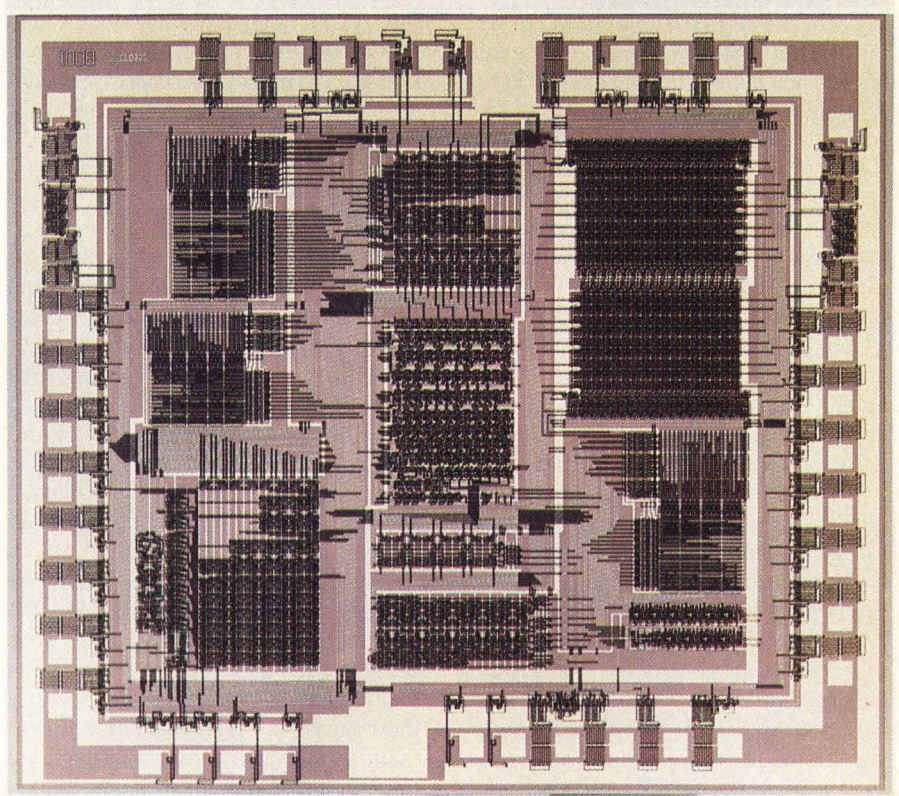
Aside from being caught in a labyrinth of transistors, gates or registers, traditional design routes force engineers to follow an inefficient design cycle. Al-

though most projects are organized in an efficient top-down style on paper, those models are not a reflection of actual design practices.

In a typical design cycle, for example, the system problem is defined first, then the system definition is born. Drawing a block diagram of the solution is the next step and each engineer on the project is given a portion of the system to implement (Figure 1a). Observing this com-

mon style of organization and flow, one would think that this is a true top-down procedure. However, since each engineer is designing a small piece of the system and rarely knows how the entire system works, the design is actually being implemented from the bottom up (Figure 1b).

The engineers designing the logic are usually given a specification of the electrical output signals their circuit is ex-



Designed by Silicon Compilers Inc. and marketed by Seeq Technologies, this Ethernet data-link controller chip was the industry's first Ethernet local area network VLSI product.

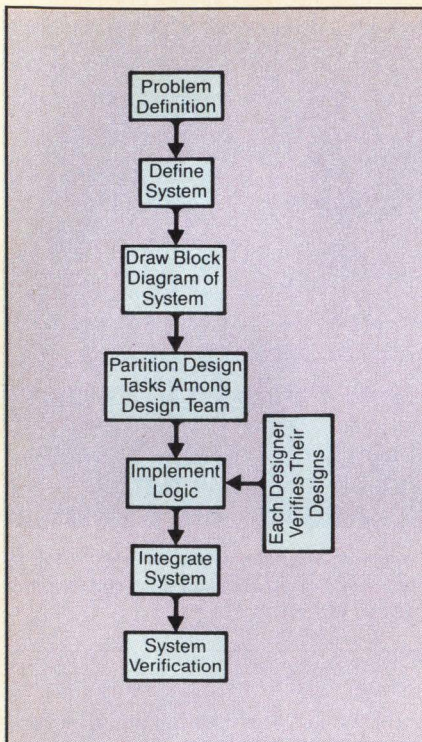


Figure 1a: This flow chart outlines a typical design cycle using a top-down approach. This is, however, only a conceptual procedure and not a reflection of what actually occurs.

pected to produce. This is based on another specification outlining the input signals which are coming from another engineer's design. As a result, the building blocks that make up a complete system are put together by many individuals who typically have limited knowledge of how these elements are related to the remainder of the system.

With this scenario in mind, the design is orchestrated using a top-down strategy and then implemented from the bottom up. From a system point of view, the engineers' creativity is never realized since they are not given a full appreciation of global architecture. Only the few that conceived the architectural definition are able to exercise creativity at the system level.

In addition, once the logic is designed, it is very difficult and excessively time consuming to alter the system's architecture. This discourages engineers from making architectural enhancements—even if they recognize areas needing improvement. Freeing the designer from this constraint is one of the primary advantages of silicon compilation.

In contrast to semi- and full-custom designs, silicon compilation divorces the system architect from transistor layout

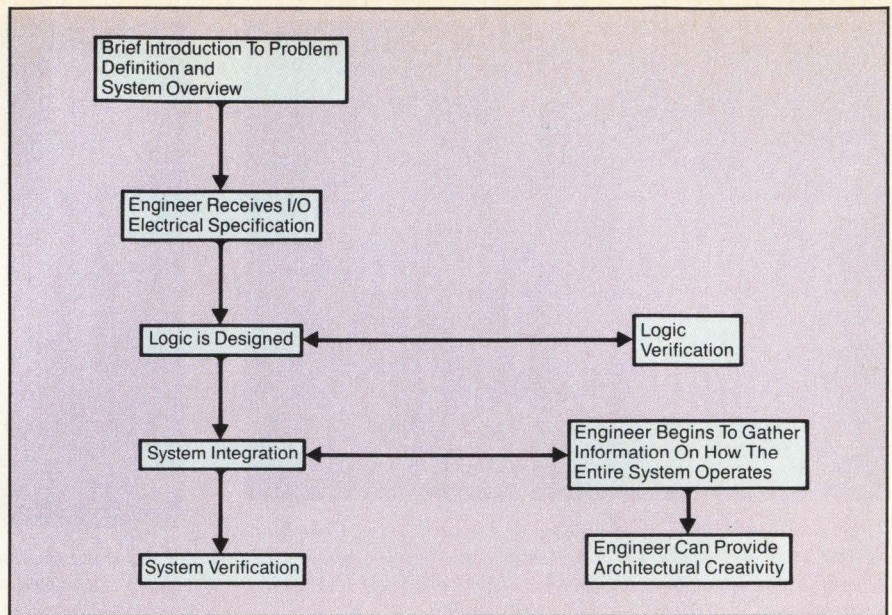


Figure 1b: Each engineer actually implementing the circuitry follows this design cycle. Compared to Figure 1a, this is a bottom-up procedure which discourages the engineer from exercising architectural creativity until the latter stages of the design cycle.

and logic/circuit design. With this portion of the design cycle eliminated, engineers can spend more time on optimizing the chip's architecture. Of equal importance, silicon compilation provides greater leverage with the minimum effort necessary to achieve maximum output. Gaining maximum leverage is a primary concern when choosing among the various VLSI design methodologies and tools. With this in mind, silicon compilers have the potential to decrease the design cycle's length by an order of magnitude.

Approaches to Silicon Compilation

Presently, there are two schools of thought on how silicon compilers should tackle design problems. These differences of opinion boil down to a single argument—how much of the design should be done by the compiler versus how much should be performed by the human. Compilers from one camp rely on engineers to define the chip's architecture, whereas the second school allows the computer to take on those responsibilities.

The first group maintains that silicon compilers cannot adequately solve the architectural problems associated with designing a VLSI chip. After the design team delineates the chip's architecture, the compiler is responsible for implementing the various functions that have been outlined. Vendors including Silicon

Compilers Inc. (SCI) (Los Gatos, CA) and VLSI Technology Inc. (VTI) (San Jose, CA) have taken this approach.

VLSI Technology's system is based on an Apollo computer and includes 175 different "cell compilers." Some of the more sophisticated compilers synthesize such functions as PLAs, ROMs, RAMs and ALUs. Selecting a particular cell compiler from the library causes the system to prompt the user for electrical parameters that are variable within the cell. With these parameters, the compiler generates the geometrical primitives of an IC layout in the Caltech Intermediate Format.

On the other hand, according to SCI's President, Phil Kaufman, the turnkey system SCI is planning to introduce next month (September, 1984) will be much different from VTI's system. It appears that SCI's system will require less detail about the function it's told to implement, and rely more on register transfer type data. Kaufman explains, "Our silicon compiler supports exploratory design. In other words, given a little bit of input information about the architecture, the compiler will provide the engineer with parameters such as die size, speed and power consumption."

SCI's silicon compiler is based on David Johannsen's (one of the firm's founders) doctoral thesis on silicon compilation prepared at the California Institute of Technology in 1981. Bristle

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Blocks, the name given to Johannsen's compiler, focused on generating geometries for IC layout. It synthesized a structured data flow and was limited in the types of architectures it could build. SCI claims that Bristle Blocks has been extended so that virtually any architecture can now be synthesized.

Analog circuits, however, cannot be synthesized by the compiler. To integrate analog circuits into a chip that the compiler is creating, the user can either build the function or call it up from an already established analog library. Once the electrical and physical parameters of the circuit are known, the user tells the compiler that a prefabricated design is to be included on the chip.

Although SCI's turnkey silicon compilation system will not be formally introduced until next month, the firm has made the compiler's accomplishments known. Three chips have been synthesized, including the data path chip for Digital Equipment Corporation's MicroVAX I (Figure 2). This chip was reportedly finished in seven months. However, details about the amount of human effort that went into the chip's development were not made public.

Other achievements from SCI include an Ethernet controller which was designed by Seeq Technology Inc., and a high resolution graphics chip which is used in Sun Microsystems's workstations. The Ethernet and graphics chips were reportedly developed in five months and nine months, respectively.

The Second Approach

For the most part, the second approach to silicon compilation has stayed in the research laboratory. Since this version puts far greater design responsibility in the hands of the compiler, it is much more difficult to develop.

A spin-off from MIT/Lincoln Laboratory, Metalogic (Cambridge, MA) is engaged in the development of a compiler that falls into this second category. While working at MIT/Lincoln Laboratory, the founders of Metalogic, Jeff Siskind, Jay Southard and Ken Crouch developed MacPitts—a silicon compiler funded by the Defense Advanced Research Projects Agency. This combined research effort is the foundation of the firm's current work.

According to Southard, the firm is currently putting the final touches on a silicon compiler which is scheduled to go into beta site this month. The new compiler, called MetaSyn, is an extension of the MacPitts effort.

One of the problems of MacPitts was that it did not have a performance prediction system. Without this, it was very difficult to determine an IC's critical timing areas and maximum clocking speed. Metalogic recognized many of the shortcomings of the MacPitts effort and has since incorporated these enhancements into MetaSyn.

Although their system requires some human intervention, it can supposedly extract register transfer data from a simplified behavioral description of the chip. The behavioral input is in the form of an

algorithm which describes how the chip operates. The language used to interface to the compiler is similar to LISP, although it has many characteristics specifically tailored to IC design.

MetaSyn makes architectural decisions and tradeoffs about the hardware used to implement the algorithm. For example, if a macrofunction composed of an accumulator and a multiplier were synthesized by MetaSyn and the input algorithm stated that another multiplication function was needed, MetaSyn would explore whether the multiplier contained in the macrofunction could be used to perform this additional multiplication task. If MetaSyn found that the multiplier contained within the macro (multiplier/accumulator) was not used when the additional multiplication task was needed, it would implement some extra control logic so that the imbedded multiplier could be used during that time period.

As a result of this exploration, the silicon compiler would synthesize simple control logic instead of another complex multiplier. This allows design engineers to explore not only the tradeoffs associated with the hardware implementation but also the performance of the algorithm driving the hardware. This is far more important, since the hardware is only as good as the algorithm.

Silicon Compilation In A Nutshell

The objective of silicon compilation is to transform behavioral or structural descriptions into the geometric data necessary to fabricate an IC. The difference between the two approaches to silicon compilation is determined by whether the description is behavioral or structural. Also, it should be understood that silicon compilation is a concept as opposed to a piece of software. It involves the transformation of a conceptual description to a concrete piece of circuitry. As a result, there are many differing ideas about the exact definition of a silicon compiler.

A complete explanation of the various approaches to silicon compilation is best described in the Y-chart developed by Gajski and Kuhn shown in Figure 3. Their objective was to develop a hierarchical model of the various approaches to VLSI design. Each line segment of the Y depicts one of the various ways to describe the functional elements (building blocks) of a chip: behaviorally, structurally or geometrically. All three are then further broken down hierarchically such that by moving from the center to the outside of the Y, the elements become larger.

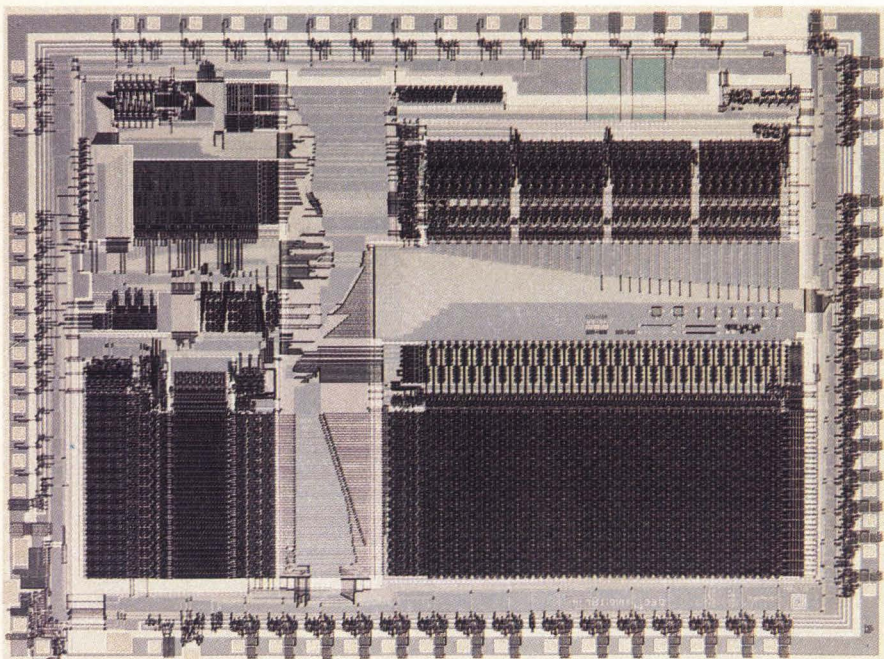


Figure 2: The DEC MicroVAX I Data-Path chip, developed by Silicon Compilers Inc. was finished in seven months.

The dotted arcs shown between the axes represent CAD tools that transform one type of representation to another. For example, the two arcs shown in **Figure 4** depict a silicon compiler that can transform Boolean expressions to gate representations and then to mask geometries. The loop on this gate level represents an analytical tool such as a logic simulator. Similarly, the loop on the mask geometries represents an automatic design rule checker.

Behavioral representations sit at the highest and most abstract level of the Y-chart and are implemented as a function of time. For example, if the system architect wanted a circuit to add two numbers (x and y), the memory location of these variables and the type of ALU would be left to the compiler's discretion. The description would say nothing about how the addition function is implemented. It would simply instruct the compiler to synthesize a device that added two numbers at time=t1 and output the results at time=t2.

At its lowest level, the behavioral characterization might take the form of Boolean equations. Moving away from the center, the Y diagram shows the compiler accepting behavioral data in the form of an algorithm. (Metalogic's silicon compiler, MetaSyn, is represented at this point in **Figure 5**). Finally, at the apex of the behavioral axis, the system architect could describe the chip in terms of its system level input and output behavior.

Moving down the hierarchy (across the Y), a compiler working from a structural description defines a distinct set of functions to implement, say, a microprocessor. With this type of compiler, the chip's global architecture is first defined by the system architect. The various blocks needed to implement the design would then be constructed by the silicon compiler. (SCT's silicon compiler is represented at this position on the Y diagram of **Figure 6**). In this case, the fact that the microprocessor's architecture was defined by the system architect and not by the computer highlights the major difference between structural and behavioral strategies.

Compilation shown on the structural axis accepts only structural data, such as a transistor, gate or register. Such a structural description can come from one of two sources. As described above, the design team may specify the input data. The other possibility is that structural output data from a compiler on the behavioral axis can act as the front end. In this case, compilation that falls along the structural axis is an interim compilation level of behaviorally specified data.

The geometrical representation of the Y diagram ignores the function that the chip is destined to perform and deals primarily with the hardware implementation of the structural or behavioral parameters. Moving away from the Y's hub, the first level would be mask geometries which refer to the polygons used to

form a transistor. Continuing along the geometric axis, a cell could pertain to several transistors joined together to make a gate. Layout refers to the physical silicon area where a function is assigned and represents the highest level in geometric hierarchy.

The ideal silicon compiler requires no human intervention to define a chip's architecture. So, to make design trade-offs, the compiler must have a certain amount of intelligence. Research into the use of expert systems coupled to silicon compilers is underway at the University of Illinois under the direction of Dr. Daniel Gajski. Other research into the use of expert systems has also come from Carnegie-Mellon University. Some of the results of their work include an automated design tool that synthesized an MCS-6502 microcomputer in four hours. As research into this technology continues, these automated chip design tools will acquire greater decision-making power.

Problems To Conquer

Large die sizes are one of the major problems that plague today's silicon compilers. Chips synthesized by these automated tools have yielded dies that are 1.3 to 10 times larger than those done by hand. (The more advanced compilers can consistently produce chips 1.3 to 3 times as large.) With the cost of silicon at a premium, this poses a serious obstacle to industry's acceptance of this new technol-

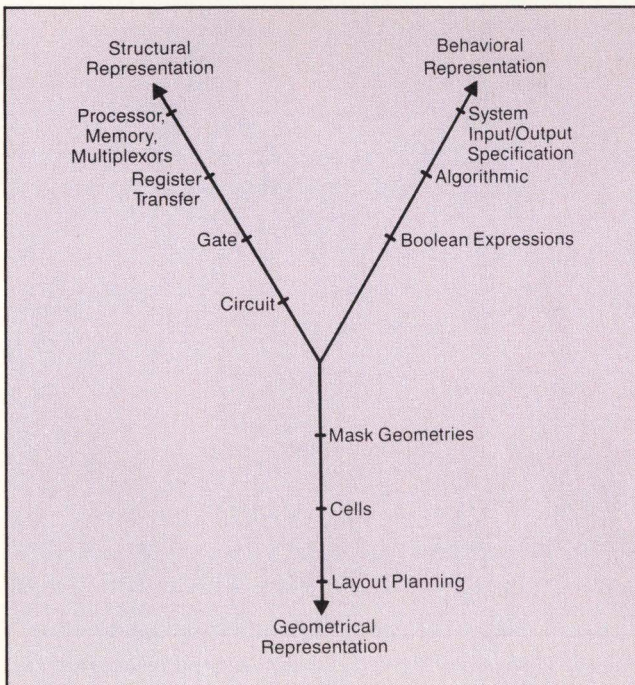


Figure 3: The Y diagram illustrates the three ways to represent the VLSI design data: behaviorally, structurally or geometrically.

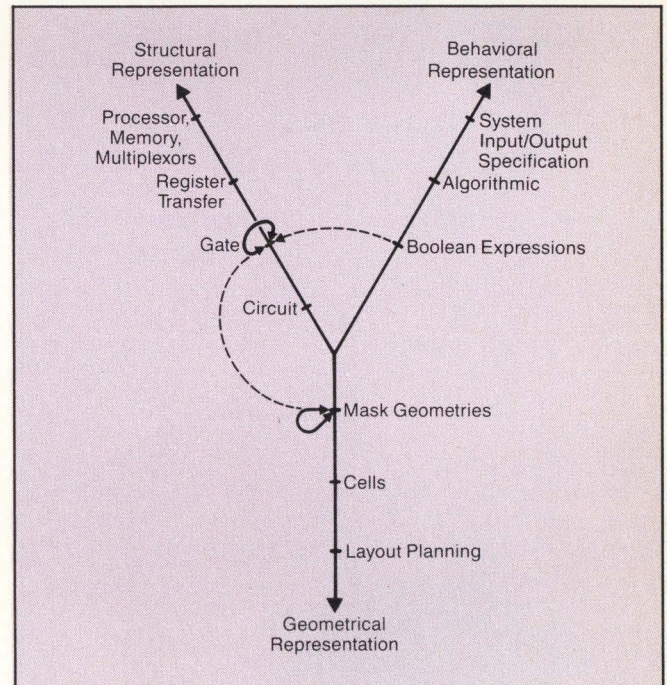


Figure 4: The dotted arcs illustrate CAD tools such as a silicon compiler that transforms one data representation to another.

Another Player in the Arena

Silicon Design Labs, Inc. is developing several products using a silicon compiler technology. The silicon compiler is based on a new language designed specifically for the description of integrated circuits; it supports both circuit attributes (geometry, connectivity, etc.) and computing. For example, Transistor is a language primitive and routing is handled within the language. Programs that can synthesize full-custom circuits are written in this language and can be linked together hierarchically to build larger blocks.

One of the key parameters in efficient silicon compilation is the lowest level language performing the layout. The quality of the behavioral- or structured-level human interface is strongly influenced by the flexibility of the language. If the silicon-level language can only compile rigid or semi-rigid cells and not build an application-specific circuit, then the silicon compiler may not map the designer's exact requirements into silicon. Hierarchy is used to control and manage complexity of SDL's system.

The first initiation of these principles was the PLEX project, undertaken by SDL founders while with Bell Labs and presented at the ICCAD Conference last September. PLEX was

a full-custom core microcomputer that could vary the data width, instruction set and word size, data word size, stack depth, etc., depending on the application it was to perform. It also built a unique instruction decoder based on the instructions actually used in the program.

PLEX was a malleable computer that could be tailored to fit a particular instruction set. It could be changed through the use of variables in the silicon compiler. PLEX was a demonstration of how a highly complex digital component could be translated from functional specification to a hand-quality layout with the system designer doing no work at the silicon level. This capability to create full-custom solutions with only a functional description can most readily be accomplished using a compiler technology that supports hierarchies and full parameterization.

The products SDL is developing rely on the concept of hierarchy and a unique layout language. SDL is developing products for both the IC designer and the systems designer that are both design rule and technology independent.

— Peter D. Rip, Vice-President,
Silicon Design Labs, Basking Ridge, NJ
Write 317

ogy. Much research is currently underway to solve this potentially crippling problem. Silicon compilation experts confess that it will be several more years before the size of a silicon compiled die is equivalent to handcrafted designs.

Die size will be the most significant tradeoff when deciding between a silicon compiled or full-custom approach. OEMs

making the choice must decide whether small die size is more important than short time to market. Turn-around times for silicon compiled chips should range from a few weeks to a few months. Judging from the present, shorter time to market has the most influence over whether or not a full-custom chip can be implemented into a system.

Laying out a chip is the second area where silicon compilers fall short. Unlike gate arrays whose cells have fixed dimensions or a standard cell which has a fixed height, functional blocks synthesized by most silicon compilers are of variable height and width. The automatic place-and-route algorithms now used to lay out chips are unable to effectively cal-

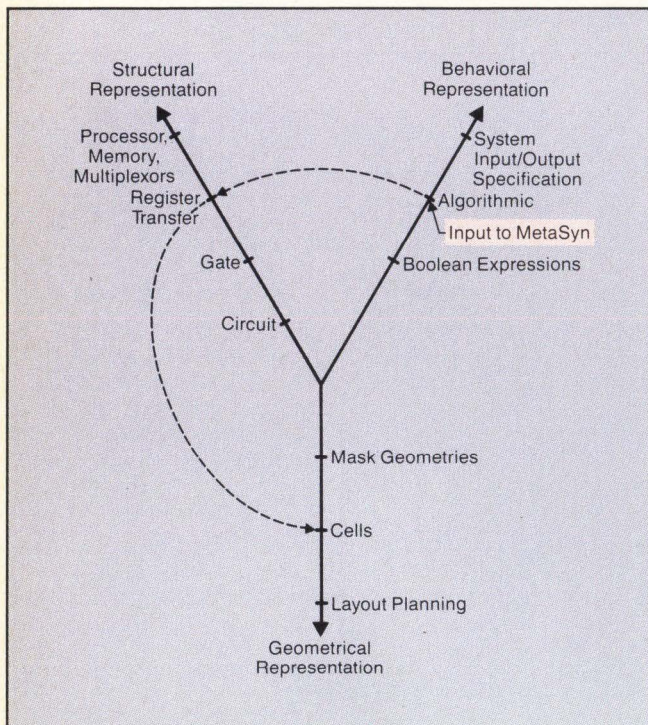


Figure 5: MetaSyn, Metalogic's silicon compiler, accepts design data in the form of an algorithm and transforms it into cell level data.

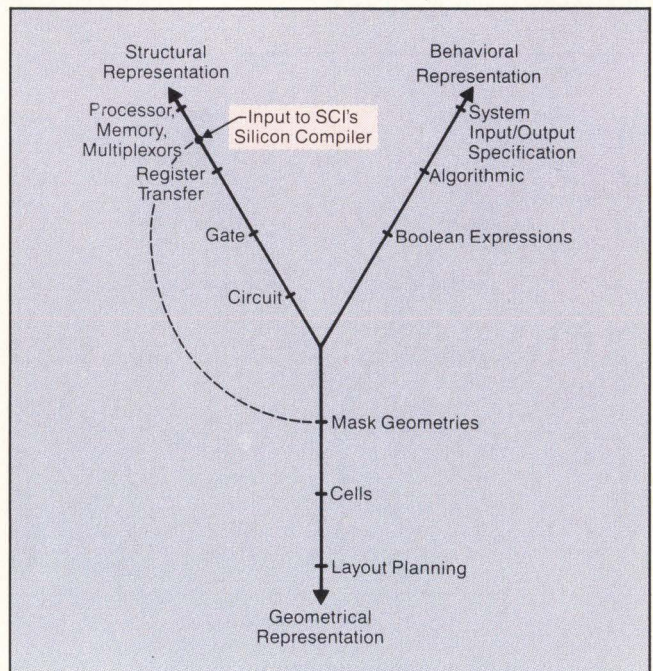


Figure 6: Silicon Compilers Inc. is scheduled to introduce a turnkey silicon compiler next month that will accept structural representations of design data. The compiler will automatically transform this input into mask level data.

The availability of silicon compilation will create a revolution in VLSI design.

culate the most efficient placement of variable sized blocks. In addition, as the number of blocks increases, the time the computer needs to make layout calculations increases exponentially. As a result of this problem, current silicon compilers leave most of the layout task to humans.

Conclusion

The availability of silicon compilation will create a revolution in VLSI design. In essence, silicon compilation is the realization of "computers designing computers." This evolving technology will be the cure for the tremendous demand of custom chips.

Present CAD/CAE design tools such as workstations are bandaids that temporarily ease the VLSI design problem. These tools are quite useful for moderately sized design efforts: the task of designing a chip with 200,000 gates is overwhelming if each gate, flip-flop or register must be drawn. Essentially, schematic capture tools are electronic upgrades of the drafting boards of a manual design methodology.

The real solution to the increasing demand for custom ICs requires tools that remove system architects from logic design. New formulas for VLSI design must be truly top-down, to allow engineers to exploit their design expertise.

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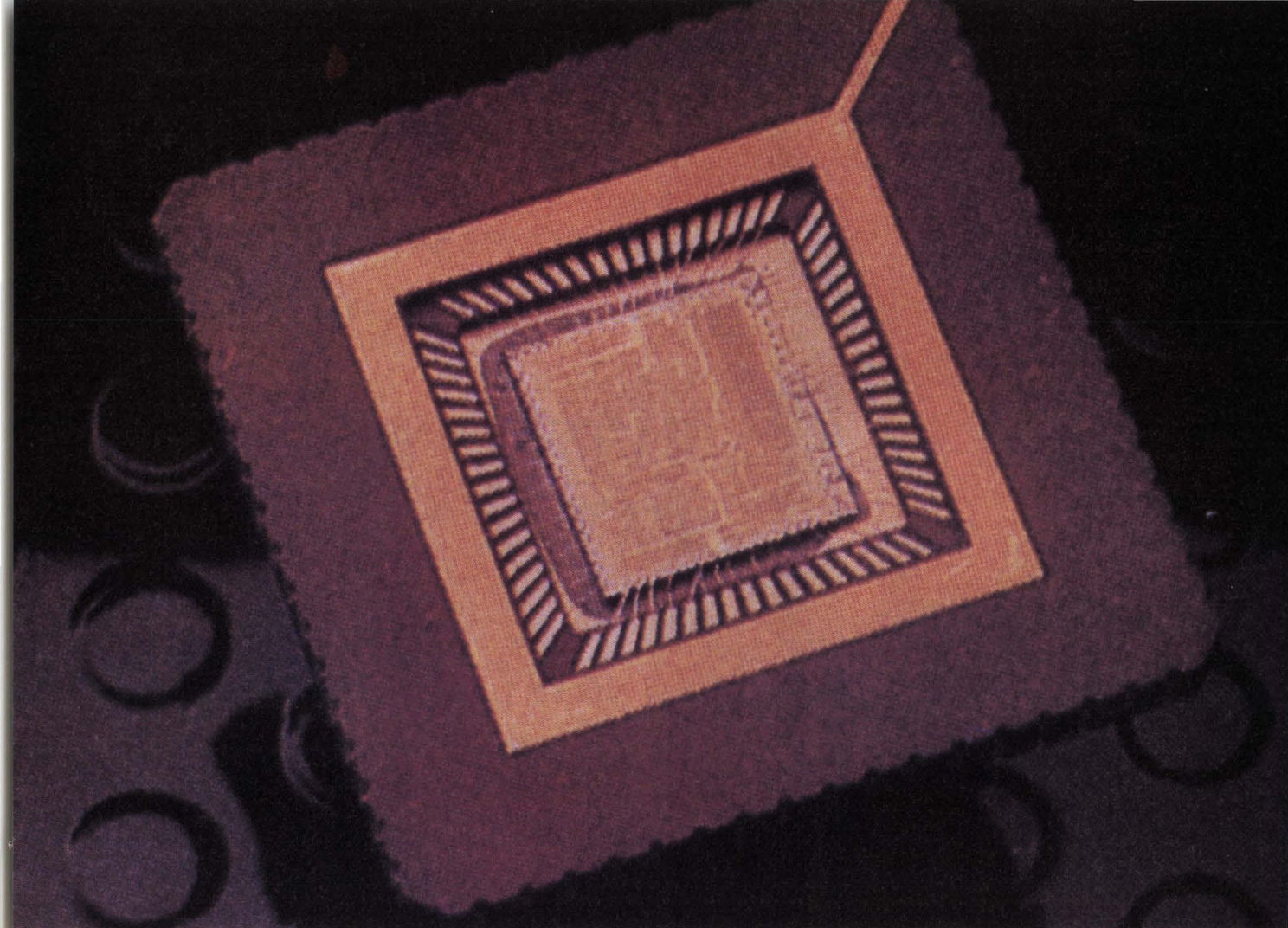


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32-Bit Microprocessors Support Parallelism And Cache

by Ram Appalaraju

Today, some 16/32-bit microprocessor-based computer systems are claiming performance comparable to minicomputers. In the future, the threat to higher-end systems will be further compounded by the introduction of the next generation of 32-bit machines. Manufactured by Zilog (Z80,000), National Semiconductor (NS32032), Motorola (MC68020) and Intel (iAPX386), the features of these processors include full 32-bit address and data paths, and the ability to support virtual memory.

The high performance of these processors is mainly due to three design innovations: pipelined architecture, cache memory and memory management to sup-

port virtual memory. In some respects, the implementation of one or all of these features is unique to the manufacturer. For example, the Z80,000 is a six staged pipelined architecture whereas the iAPX 286 implements pipelining in four stages. The Z80,000's cache is used both by instruction and data whereas the MC68020 has a cache exclusively for instructions.

Pipelined Architecture

Designers of previous generations of processors have relied heavily on ever higher clock frequencies to provide increased throughput with more complex instructions and memory systems. However, the design considerations of a higher clock frequency and the memory speeds re-

quired made such designs expensive. The alternative is to implement pipelining techniques to minimize the number of clock cycles for each instruction.

Intel's approach to pipelining allows the processor to perform four million register-to-register instructions per second. The 286 processor is pipelined at three levels: the memory bus interface, functional unit level and within a functional unit. Four functional units perform one step in the instruction pipeline. They are called the bus unit, the instruction unit, the execution unit and the address unit (**Figure 1**).

The bus unit provides the interface between external memory and the internal units. Housed in the bus unit are a bus cycle controller and functional blocks for

In some respects, the implementation of pipelined architecture, cache memory and memory management on 32-bit chips is unique to the manufacturer.

implementing code prefetch, and buffers to write data from the last instruction. The prefetch block holds up to six code bytes for the instruction unit. Functionally, the bus unit is used by various other internal units like the address unit, data unit, etc. The prioritizer in the unit examines bus cycle requests from four sources and prioritizes them according to source as follows: HOLD request from bus master, processor extension data transfer, address unit and code prefetch unit.

The memory bus interface provides memory cycle pipelining. This enables a faster transfer of information between the internal logical units and memory. In the 286, a data transfer consumes as few as two clocks, thus providing a bandwidth of 8 Mbytes per second. The pipelining is achieved by examining the address of the next memory cycle while the current memory cycle is in progress (Figure 2).

An important element of the NS32032 pipelined implementation is shown in the block diagram of Figure 3. An 8-byte queue FIFO synchronizes the operation of the bus interface unit and the instruction decoder. The effect of this is that the instructions are ready to be executed when needed by the processor, i.e. the fetch time has been overlapped with execution of prior instructions.

The instruction decoder pulls instructions from the FIFO, a process that requires cooperation with the execution unit. As the execution unit signals the end of each instruction fetch, the decoder begins assembling the next one, while the execution unit performs the specified operation. When room for another 32-bit transfer has been freed in the FIFO, the bus interface unit performs another read.

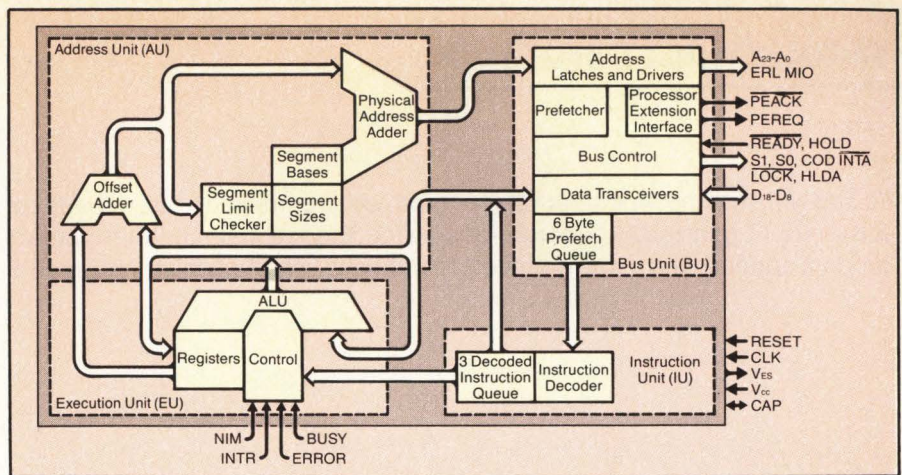
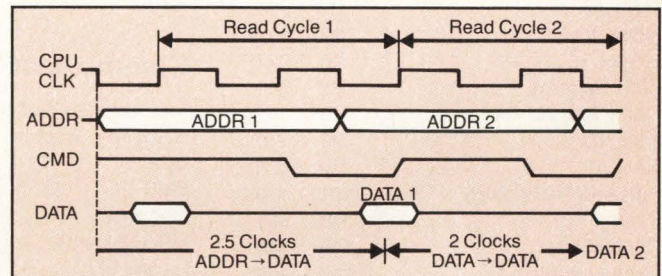


Figure 1: In this internal block diagram of the iAPX286, the four functional units are divided off by dotted lines.

Figure 2: Pipelining on the iAPX286 high performance bus involves the presence of the address for the next memory cycle during a current cycle.



The Z80,000 has a six-stage pipeline architecture that performs the functions shown in Figure 4. For simpler instructions, all stages of the pipeline (except for operand store) are completed in one processor cycle (two clock cycles). Therefore at 10 MHz, the peak instruction execution rate is 5 MIPS. In practice the instruction execution rate is about one third the peak rate depending on the instruction mix and system configuration.

The on-chip cache is time-multiplexed between instructions and data accesses within the same processor cycle. The pipeline then flows smoothly without having two stages competing for the same resource. Similarly, there are two ALUs, one for address calculation and one for instruction execution. This eliminates sharing a single ALU between the address calculation stage and the execution stage. The on-chip translation buffer also helps smooth the pipeline flow as the address translation is done in the address calculation stage without having to go off-chip.

Operand storage is the only stage which requires several cycles. Performance is not seriously degraded, however, because most instructions do not store results in memory, and the store operation can usually overlap with the processing of other instructions.

Cache Memory

In spite of pipelining and improved bus timing and control, a lot of time is still

consumed by memory read and write operations. To enhance the processing capability of the CPU, cache memory may be added between the CPU and the main memory. Cache improves performance mainly by decreasing memory access time. Faster access rate is achieved by making a copy of previously selected main memory into cache. When a CPU needs data or address for execution it first checks for it in the cache; if the required information is found there, fetch time is considerably reduced.

Previously, cache memory has been a feature of only larger systems. But the advent of VLSI has enabled a single chip to incorporate cache, memory management unit, etc., in addition to the CPU.

Zilog's 80,000 uses a 256 byte, fully associative cache memory to attain an access rate of 80 nsec. The cached is organized in 16 blocks each containing 16 bytes of data. The processor, according to Zilog, allows the system programmer to cache instructions only, data only, instructions and data or fixed memory.

In contrast, the MC68020, uses cache only for instruction fetching. The instruction cache is best used when the program involves many short branch loops. The processor fetches data from external memory and executes them through the instructions found in the cache (Figure 5). Such an organization, according to Motorola, assures that only the latest data is used in the system where another processor or source may modify the data.

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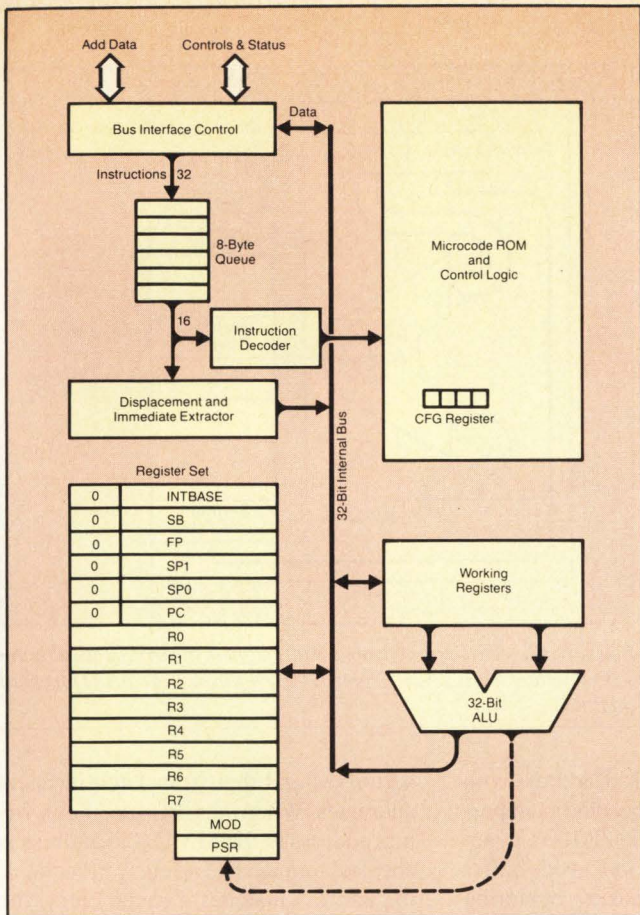


Figure 3: The 8-byte queue FIFO in the NS 32032 provides pre-fetched instructions to the decoder; fetching occurs during execution of the previous instruction.

In the Z80,000 and the iAPX286 (and probably the 386), memory management is on-chip. The NS32032 and MC68020 are supported by NS32082 and MC68451/MC68851 respectively for memory management. The Z80,000 and NS32082 use demand paging while the iAPX286 implements memory management by segmentation. Motorola can use either technique.

A segmented address space is essentially a collection of small linear address spaces. Segmented addresses consist of two components: the segment selector, which picks the segment in which a datum is located; and the displacement selector, that specifies the number of bytes from the start of the segment to the desired location.

Some claim that a segmented memory is better tuned to the organization of modern modular programs and structured data than a linear memory. Since the structure of logical address spaces in a segmented architecture reflects the logical structure of the program, mechanisms for preventing access to segments can be used to protect meaningful program units.

Unfortunately, most segmented architectures allow only fewer than 128 segments of 64 Kbytes or less each. This size limitation was originated to allow software compatibility with systems in which the entire linear address space was 64 Kbytes.

Intel's 80286 operates in two modes: iAPX86 real address mode and protected virtual address mode. In real address mode, programs use real addresses with up to 1 Mbyte of address space. Programs use virtual addresses in protected virtual address mode. Both modes provide the same base instruction set, registers and addressing modes.

(continued from p. 97)

The looping mechanism and the cache in the 68020 enable custom user-written string operations to be executed faster. After the first pass, loops need only access read and write data. In terms of programming, repetitive operations may optimally make use of such a scheme. Since the instruction cache organization leaves the external data bus free for use by another processor or DMA controller in the system, performance is further enhanced.

Virtual Memory

In many computer systems, the logical address space is far larger than the semiconductor memory. Virtual memory frees the user from limits on physical memory size by making the entire logical address space appear available. At any given moment, only a few pages of the logical address space are mapped onto physical memory. The other pages, stored on a peripheral storage device such as a disk can also be accessed in a virtual memory scheme.

Whenever the CPU of a virtual memory system generates a memory address, the hardware checks whether that address lies in a page in main memory. If it does, the address is translated to the appropriate physical address. If not, an operation called a swap is performed, and the oper-

ating system software loads the missing page from disk. If this operation is performed rapidly, the user will have the impression of having an enormous physical memory.

There are two distinct approaches to swapping: segmentation and demand paging. In a demand paged memory, the size of the swap is based on a fixed-sized unit called a page. Page size is specified by the system designer. In a segmented memory system, the size of the swap is variable, determined by the size of the segment.

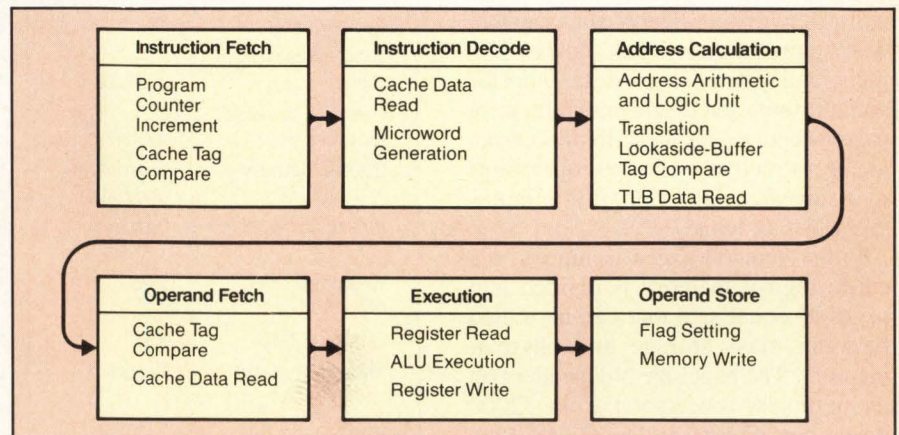


Figure 4: The Z80,000 uses six stages of pipelining; instruction fetch, instruction decode, address calculation, operand fetch, execution and operand store.

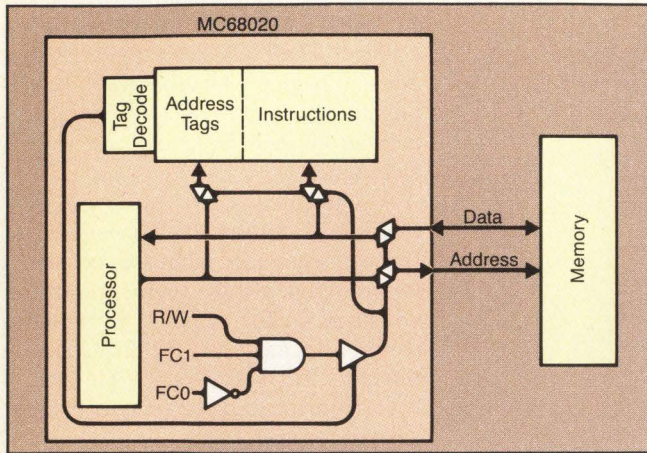


Figure 5: Cache on the 68020 is for instructions only, important to programs with many short loops.

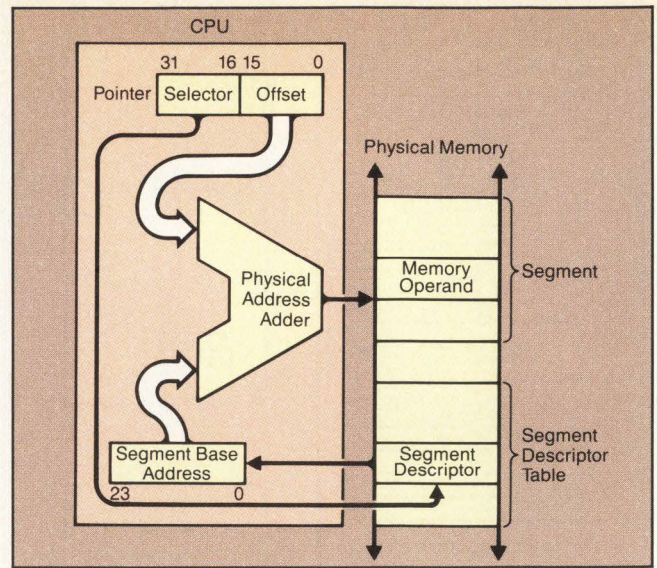


Figure 6: Protected mode memory addressing in the iAPX 286 adds the 32-bit pointer to the 24-bit segment base address to form the physical address.

In protected mode, the CPU automatically maps 1 Gbyte of virtual addresses per task into a 16 Mbyte real address space. This mode protects memory to isolate the operating system and ensure privacy of each task's programs and data.

As in the real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory-resident table rather than the upper 16 bits of a real memory address, and the 24-bit base address of the desired segment is obtained from the tables. The 16-bit offset is added to the base address to form the physical address as shown in Figure 6. All iAPX286 instructions which load a segment register will reference the memory-based tables, that contain 8-byte values called descriptors.

Descriptors define the use of memory or new functions for transfer of control and task switching. The 286 has segment descriptors for code, stack and data segments and system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multiprocessor systems.

In the demand paged technique, the entire logical memory is divided into pages of equal size that can be traded between mass storage and physical memory. The page size is dependent on the particular processor. For the 32000 series, it is 512 bytes and for the Z80,000, it is 1024 bytes.

Minimizing the delays associated with

the translation of logical addresses to physical addresses has become an important consideration. In the Z80,000, a special on-chip translation look-aside buffer (TLB) minimizes these delays by storing logical addresses and their corresponding physical addresses as they are translated through the memory-resident tables. Subsequent accesses to the same page are simply retrieved from the TLB. Only when an entry does not exist in the TLB (a TLB miss) must the tables perform a translation. The 286's TLB can hold the 16 most recently referenced pages.

In National's demand-paged approach, the NS32032 MMU utilizes an associative on-chip translation cache containing the 32 most recently accessed virtual

addresses and their translated physical addresses. When the CPU specifies a virtual address to the MMU, the address is checked for match to an entry in cache. If the address matches a cache entry, the MMU will check for protection level and, if access is permitted, make the physical address available for memory immediately.

In segmented multi-program systems, available memory space can become fragmented during swapping. This can leave inadequate contiguous physical memory for a large segment. Because of this memory fragmentation problem associated with swaps in segment-based virtual memory systems, some claim that page-based mapping may be more efficient.

	Z80,000	NS32032	MC68020	iAPX386
Technology	NMOS	HMOS	XMOS	HMOS III
Pins per chip	64	68	84	68
Clock frequency (MHz)	10,18,25	6-10	8,10,16	8
Direct accessible memory	4 Gbytes	16 Mbytes	256 Mbytes	32 Mbytes
Cache memory	instructions and data	NO	instruction only	NO
Instruction queue	6 stages 2 ALUs	8 bytes	2 words	4 stages
Extended processing	YES	YES	YES	YES
On chip MMU	YES	NO	NO	YES
Virtual memory	Paged	Paged	Paged/ Segmented	Segmented
DMA	Optional	Optional	Optional	Optional

Table 1: A comparison of the critical parameters of four 32-bit microprocessors.

Attribute	Paging	Segmentation
Page Size	Fixed	Variable
Replacement algorithm	Hardware	Software
No. of linear addressing spaces	1	Many
Ability to protect a procedure and data separately	No	Yes
Ability to distinguish a procedure and data separately	No	Yes
Fluctuating table sizes	Cannot be accommodated	Can be accommodated
Sharing of procedures between users	No	Yes
Unused memory space	none	possible

Table 2: There are significant advantages to each of the two schemes for virtual memory, segmentation and demand-paging; the choice depends on system needs.

Since all pages of a demand-paged system are the same size, if any physical page frame is available, it can hold any page being swapped. There is no need for the virtual memory management strategies to deal with large, odd-sized blocks of main memory, or to take into account any information about how memory will be used by the running task.

32-Bit Choices

The choice of a microprocessor is, to a great extent, dependent on application. For example, if an application requires a high I/O transfer rate, it is best if address and data lines are non-multiplexed, as in the MC68020. However, multiplexing can reduce the pin count and hence the chip area. The pin count of the 68020 is

as large as 84, compared to 68 for the NS32032, which uses multiplexed address and data buses.

Various amounts of pipelining, implemented on different parts of the system, are factors in the speed and complexity of 32-bit machines. With cache memory, not only the size, but also what is able to go to cache is important. Cache may be for instructions only, as with the 68020; this will require some external logic for faster access to data. The Z80,000 allows a choice of what is in cache: data only, instructions only or both.

Virtual memory management is the other critical factor in differentiating between the 32-bit microprocessors. Of the discussed, two use external support chips for memory management and the others have on-chip management. Efficient space utilization during swapping with demand-paged schemes is traded off against the protection of logical segments in segmented virtual memory systems. □

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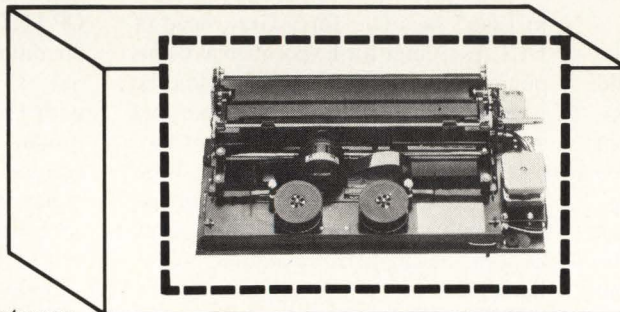
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Extensions And Performance Improvements Keep Pascal Competing

The emerging Big Three advanced languages appear to be Pascal/Modula-2, Ada, and Lisp.

by Michael Cashman,
West Coast Technical Editor

In the late '60s, Professor Edsger Dijkstra complained that we in the computer industry would be headed for a disaster in the future if we didn't clean up the act of programming.

His specific complaint was about the GO TO statement in Fortran (he could have cited other examples and other languages). Although the GO TO statement was seen by programmers as very flexible, it did encourage "spaghetti coding." Programmers could jump all around in a program — and did so with great regularity. Consequently, programs written in this fashion were often impossible for their own programmers to debug. This was an affront to mathematicians like Dijkstra who suggested that we desperately needed languages that would encourage more logical programming habits. Otherwise, the future's more sophisticated programming projects would be almost impossible to implement.

Another European professor, Nicklaus Wirth, reacted to Dijkstra's vision by creating what can be termed a teaching language for demonstrating to students the emerging technique which came to be known as structured programming. He named the language Pascal. Although

Pascal is an example of structured programming, others in the industry (often with vested interests) feel that it isn't a very good example. At least when applied to "real world" programming problems, they claim Pascal falls short.

The language does have its shortcomings, but so do all languages. Even Wirth moved on to an expanded, updated language which is very Pascal-like, which will be discussed later. But there is a large pool of university-trained programming talent that has grown up on Pascal and learned to minimize or work around the language's shortcomings.

Extending Pascal

"If I were constructing a relatively complicated program for industry and had a good idea what it would look like, no doubt I'd program that application in Pascal. But if it were a very complicated experimental system and I wasn't too sure whether it could be done, I'd program it in Lisp," says Dr. Terry Gray, head of UCLA's Center for Experimental Computer Science. Dr. Gray states that he wouldn't have been able to make that statement a year ago, before performance and programming improvements were made to the language. One of the companies specifically mentioned by Dr. Gray as contributing to this condition is Borland International (Scotts Valley, CA).

Philippe Kahn, President of Borland, feels that Pascal is a very good programming language, but that it needed to be extended. He was frustrated with using the Pascal implementation made popular by the University of California at San Diego and set out with others to create a better one.

This product, called Turbo Pascal, is generating new interest in the language. First, Kahn defined the set of extensions he felt the language needed to be a more powerful program development tool. These included:

- absolute address variables
- bit/byte manipulation

- direct access to CPU memory and data ports
- dynamic strings
- free ordering of sections within declaration portion
- full support of operating system facilities
- in-line machine code generation
- include files
- logical operations on integers
- program chaining with common variables
- random access data files
- structured constants
- type conversion functions
- automatic overlays
- windowing (for IBM PC, XT, or jr. and true compatibles).

In three man-years, Turbo Pascal was written in assembler code for Z-80 and 8088/8086-based microcomputers, with support for the 8087 co-processor on the way. The one-pass compiler generates native code for machines running the CP/M, CP/M-86, and MS-DOS/PC-DOS operating systems. Turbo Pascal requires only 35 Kbytes of disk space, compared with 129 to 300 Kbytes for competitive products, and this includes a full-screen editor. Finally, sensing that the features contained in Turbo Pascal might make it a very popular software product, Kahn priced it at \$49.95.

It always seems that compilers which compile and link code relatively fast tend not to provide comparable run-time performance, but that isn't the case with Turbo Pascal. For example, Turbo Pascal's compile and link speed on the Eight Queens program contained in Nicklaus Wirth's book "Algorithms + Data Structures = Programs" yields the (claimed) performance values in **Table 1**.

"I won't claim we've made any revolutionary advances in compiler design," says Kuhn. "I just think that the product managers at the other companies have either forgotten or never knew what a compiler should be. Other products are relatively inefficient; they are the result of poor

programming habits, and they appear to be committee compromises. A compiler *must* be an effective tool: It must be fast and interactive, it must be one-pass, and the user interface must be good."

Pascal-Like Language

Languages have their supporters and their detractors. Dick Heiser is a California-based computing consultant who may be putting recent Pascal developments in a fair perspective. "I feel Pascal's prime time has passed. Some of these recent developments, like Turbo Pascal, should have come out some years ago. Even Pascal's creator [Wirth], after creating advanced versions of Pascal, went on to create new languages which can only be described as being Pascal-like."

The latest of these languages is Modula-2. While some fatal shortcomings can be observed in seemingly any programming language, about the only criticism lodged against Modula-2 is that it isn't yet popular. In creating Modula-2, Wirth didn't just engage in an exercise to fix every alleged shortcoming of Pascal. By this time (1977), he had years of experience in struggling with the problems of attempting to apply structured, logical programming techniques to real-world computing problems.

Modula-2 uses self-contained modules to solve many of the problems inherent in Pascal. The programming statements themselves look very similar to Pascal, and it's claimed that Pascal programmers can be up and working in Modula-2 within hours and proficient within a week. A similar learning curve is claimed for C programmers.

Volition Systems (Del Mar, CA) is the first commercial vendor of Modula-2. Versions are supplied for the Apple II, IIe, and III; IBM PC and XT, and the Sage II and IV. Modula-2 in this implementation is not just a compiler; rather it is a total integrated development system. It contains the Modula Operating System similar to Apple Pascal. For example, in the IBM PC and XT implementations, it runs as a subsystem under PC DOS 2.0, and permits programs to transparently access DOS data files. Features of this product include:

- interrupt support (except Apple III)
- one-pass Modula-2 compiler
- syntax error messages displayed with erroneous source
- conditional compilation
- no module linking required for compilation
- source compatibility between Apple,

IBM and Sage

- comprehensive module library and library manager utility
- text editor (ASE™)
- program development utilities for the IBM and Sage
- a set of 48 sample and tutorial programs, and
- documentation, including an introduction to Modula-2

One especially nice feature of this system is called p-Shell. p-Shell is a collection of Modula-2 programs that provide a UNIX-like programming environment. It consists of a command shell and several commonly used UNIX commands. The shell supports UNIX-like features that include wildcards, scripts, and input/output redirection. Although the pipes feature is implemented as intermediate files, it's claimed that it offers approximately the same level of efficiency as UNIX' pipes. Pricing for Modula-2 begins at \$295.

Both Heiser and UCLA's Gray feel that this is a system to watch over time. "Just solving the problem of how to store local variables was a big step in qualifying this language for financial applications, which are miserable to accomplish without this capability," says Heiser.

	Turbo Pascal	IBM Pascal	Apple Pascal	Pascal MT+
compile/link	1 sec.	97 sec.	14 sec.	90 sec.
execution	2.2 sec.	9 sec.	65 sec.	3 sec.

Table 1: A comparison of the performance of Turbo Pascal with three other microcomputer versions of Pascal running "Eight Queens" shows its great speed advantage for both compile/link and execution.

Lisp, Ada Gain Ground

UCLA's Gray likes Modula-2, but feels that interest is swinging toward Lisp and its variants and also mentions Ada. "For example, Pascal seems to be of little or no interest at MIT. There, Lisp is the language that is taught." While this language is closely associated with artificial intelligence research, it is by no means limited to these exotic applications. Gray sees its influence spilling over into more generalized applications despite the fact that Lisp lacks the strong advantage Pascal features in rigorous data typing. Lisp, of course, is typically interpreted; only recently have compatible Lisp compilers and interpreters become available.

According to Gray, Ada is coming on strong, with heavy usage building in the aerospace community. This particular

The conversion, if it can be called that, from Pascal to Modula-2, doesn't seem very great.

language is criticized by almost everyone as trying to be all things to all people, but the power of government to mandate its usage in defense applications is compelling use, if not acceptance.

Pascal's Future

For now, Pascal, a language that industry charged (with some fairness) as being out of touch with real-world applications, yet become so widely taught inside the university community, seems to have gotten its second wind. At the least, this will lead to more converts for a language avant garde theorists feel should pass from the scene. Still, the conversion, if it can be

called that, from Pascal to Modula-2, doesn't seem very great. In fact, Borland International is thinking of developing Modula-2 and C compilers that it feels will complement, rather than compete with, its Turbo Pascal.

Systems implementers should carefully evaluate these advanced languages and analyze whether it is time to convert to a language that simplifies the system development process and overall product reliability. □

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Marketing The Integration Solution

Market window pressure on design cycles is encouraging companies to invest in computer-aided engineering and design systems. Some companies have automated the individual stages in the electronics development cycle, but bottlenecks invariably develop in transferring between those automated systems.

Racal-Redac (Westford, MA) has recently introduced their CIEE (Computer Integrated Electronic Engineering) system to provide integration of CAE, CAD and CAM. Running on industry-standard hardware, including the VAX, Apollo's CAE and graphics workstations and the IBM PC, CIEE provides specific software packages for each stage of the design cycle, integrating these packages with a relational database.

The CIEE system enables an engineer to conceptualize and create circuitry on a workstation and then simulate its performance before design commitment. The same system supports the design phase for PCB, hybrid, gate array, standard cell and full-custom circuitry. As other Racal-Redac systems, it provides both automatic and interactive facilities for maximum design productivity. CIEE also provides a range of outputs for manufacturing, including NC drills and profilers, pattern generators, automatic component insertion and automatic test equipment. This single system thus brings a circuit from concept through design, manufacture and test.

A key feature of CIEE is its relational database which enables data transfer between all workstations and software packages. The database can be used to

Racal-Redac's CIEE engineering design software being displayed on an IBM PC.



establish job files containing all the pertinent information on the status of individual jobs and allows the creation of authorization levels and procedures for management control and project management. The database also allows data transfer to existing office and CAD systems, for full integration.

Racal-Redac's marketing agreement with Apollo Computer represents the first time such an extensive range of applications software for the electronic design process—including integrated circuit and printed circuit board design—has been integrated into one package on Apollo's DOMAIN workstations. While the VAX brings high speed

and the capacity to handle complex computational programs, the Apollo workstations offer a flexible environment through the DOMAIN network.

CIEE products will become available over the next six to nine months. Circuit design and data capture facilities on the IBM PC will be available in September 1984. Circuit design, analysis and simulation will be available on Apollo workstations in October 1984. The complete range of CIEE software, including full-custom, standard cell, gate array and an alternative PCB design package will be available in the second quarter of 1985.

—Hanrahan
Write 236

AT&T PC Coexists In MS-DOS/UNIX Environment

AT&T's complement to the previously announced 3B line of superminis and supermicros is the PC6300, a personal computer which rounds out AT&T's "blueprint for the future," the Information Systems Architecture. AT&T has offered an answer to the IBM PC by designing its machine in MS-DOS with capabilities to access a UNIX environment.

AT&T particularly emphasizes the new

PC working in tandem with the 3B2, a multi-user, multi-tasking 32-bit UNIX-based supermicro that is of desktop dimension and accommodates up to 18 users. Through a device called a Context Switch, a user can switch between a PC application and terminal emulation mode for access to outside applications while suspending the PC application. This capability allows the advantages of UNIX

to be accessed from an MS-DOS environment, thus protecting the large installed base of DOS programs and, at the same time, offering opportunities to use the coming influx of UNIX software. With the Context Switch the user can operate a PC as a stand-alone MS-DOS system or a dumb UNIX terminal.

Jack Scanlon, V.P. of the AT&T Computer Systems Division, described cor-



The AT&T PC6300 operates in MS-DOS yet can act as a UNIX dumb terminal.

porate strategy as "UNIX all the way down to the PC" stating that it is quite natural to expect UNIX on any box that AT&T offers. A UNIX-based PC is tentatively scheduled for introduction in

the fall.

AT&T will continue its strategy of an open architecture approach by encouraging OEMs to design specific interfaces either with the PC or the 3B2, particu-

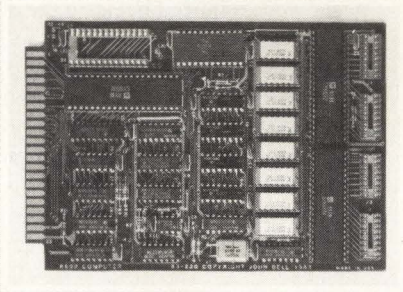
larly in the area of special communications devices or interfaces to various peripherals. Scanlon emphasizes AT&T's commitment to open architecture by encouraging OEMs, "We're very happy to provide them with all the bus specs and technical assistance to design their interface."

The 6300 is built on Intel's 8086, claiming an 80% operation speed increase over the comparable IBM PC's 8088. Seven usable expansion slots are offered, six slots include hard disk configuration. A 16 to 8 bit data bus converter allows use of industry standard 8-bit expansion boards for communication interfaces. The memory available on the 6300 is either 128K expandable to 640K or 256K expandable to 640K.

The display resolution is higher than that of the IBM PC; PC-DOS compatible color graphics are 320x200, while the proprietary display resolution is 640x400.

The PC6300 is now available and is priced at \$2,745 up to \$4,945 with additional memory.

— Hanrahan
Write 235



6502 64K COMPUTER-CONTROLLER

The model 83-230 single board computer has 55K of dynamic RAM, up to 8K of EPROM, four parallel ports, 1 serial RS232 port, and four timers. This 4.5" X 6.5" computer uses the 44 pin AIM bus. This computer was designed to be used as an industrial controller. A 2716 monitor EPROM is available for \$19.95. Bare board for \$49.95 or assembled and tested for \$299.95.

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Medical Device Uses In-Circuit Programming

A "state-of-the-art" solution to the unique programming needs of a manufacturer of implantable medical devices has been implemented by Medtronic, Inc. (Minneapolis, MN). Medtronic selected the Data I/O 156A In-Circuit Programming System to program its MemoryMod software cartridge for system flexibility and ease of use.

The MemoryMod is a small, 56 Kbyte, EPROM-based memory cartridge containing seven 27C64 EPROMs plus interface circuitry. The cartridge was designed to plug into a Medtronic cardiac pacemaker programmer. The 156A makes it possible to program eight of the MemoryMod cartridges at once. The system will also allow Medtronic to program loaded circuit boards simultaneously instead of programming individual, or batches of individual EPROMs to be placed onto circuit boards later.

The system was also chosen because it was relatively simple to adapt the 156A electrical and mechanical design to create the programming interface. Medtronic engineers created the basic design with assistance from Data I/O over a three-month period. The software-based operation makes the 156A easily adaptable to future applications, which include plans for use with two other medical instruments within the next year. The CRT display and full typewriter keyboard operation make for easier use.

In the early stages of its development, the MemoryMod was programmed singly with a Data I/O Model 19 that was especially modified for Medtronic's MemoryMod application. Switches on the modified UniPak selected one of seven 27C64s to be programmed. The production schedule required a less time-consuming system making it possible to program many parts at one time. In the near future Medtronic will be able to download the data from an HP64000 microprocessor development station directly to the 156A via its RS-232 port, making future software changes simple to make.

Specifications for the MemoryMod called for a part that is small, low power and user replaceable. In addition, the cartridge must interface to an NSC800 CMOS microprocessor. In order to meet the initial requirements, Medtronic chose EPROMs rather than masked ROM. The



The MemoryMod is used for the Medtronic Model 9710 pacemaker programming system.

EPROMs provide a memory module with the flexibility to respond to producing not only production quantities of parts, but quickly producing small quantities of parts to support clinical studies. EPROMs also provide the quickest method for producing MemoryMods and getting them to physicians following a clinical study and FDA approval. Medtronic is able to program the part and avoid the time delay associated with masked ROM. The customer can then return his current part which can be erased, tested, and reprogrammed.

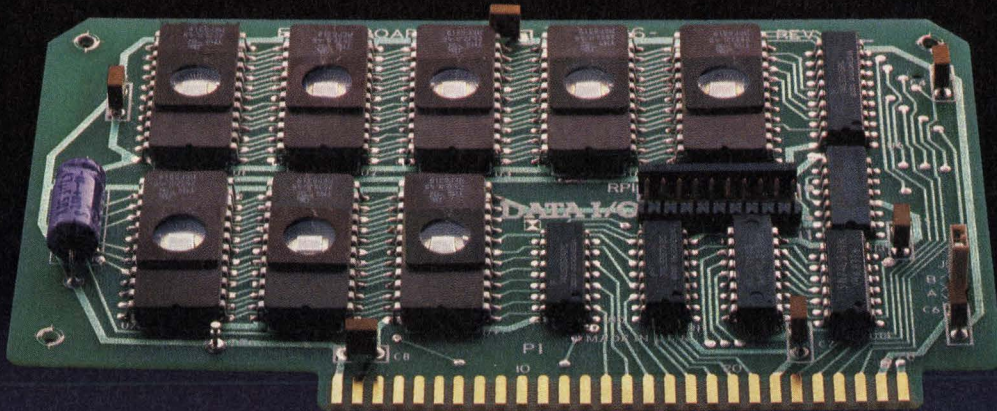
The Memory Mod was designed to include on-board address/data demultiplexing and a bidirectional data bus to accommodate the EPROM programming write cycle. Low power components were required because the device was to be battery powered. This requirement was met by using Fujitsu 27C64 EPROMs and 7400 series high-speed, CMOS circuits for the interface.

Medtronic was able to accommodate the small size requirements by using EPROM and interface ICs in die form and having them wire-bonded to a ceramic



The Medtronic MemoryMod is a small 56 Kbyte, EPROM-based memory cartridge containing seven 27C64 EPROMs plus interface circuitry.

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also be available.

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DATA I/O

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substrate. The part meets environmental requirements for storage and operation of the device, and the circuitry is hermetically sealed with a sapphire window for ultraviolet penetration. This exotic form of high reliability packaging was produced for Medtronic by Teledyne Microelectronics (Los Angeles, CA). The resulting part has a 25-pin, sub-miniature D connector and dimensions of $2.9 \times 1.35 \times .24$ inches and is contained in a plastic case that is $3.2 \times 1.7 \times .38$ inches.

The MemoryMod is used for the Medtronic Model 9710 pacemaker programming system which consists of the programmer, printer and transmitting head. The system was designed to fit into a small attache case for easy portability and storage. Criteria for creating the 9710 system were based on input from physicians, who indicated they wanted a simple to use, compact and updateable system.

With the programmer, implanted pacemakers can be reprogrammed from out-

side the body as the patient's needs change. The physician can use the Medtronic Model 9710 programmer with all present and future Medtronic pacemakers by replacing the MemoryMod cartridge. Earlier programmers could not be updated to interface with new pacemaker models.

Medtronic produces neurological systems, mechanical heart valves, and instrumentation for medical diagnosis and monitoring. **Write 218**

Fiber Optics Joins Advanced Microcontroller In Distributed Workstation Architecture

When interfaces between the components of a workstation are not general purpose, the system designer may find product evolution difficult. Connecting cables between modules may be expensive in terms of material and labor. The ubiquitous RS-232C interconnect is insufficient for such designs. Cabling itself can lead to EMI and data security problems. In addition, low data rates between modules are often a system performance limiter.

A workstation design which overcomes these drawbacks while keeping modular system design advantages is illustrated in **Figure 1**. This design uses an advanced central microprocessor, the Intel 80186, 16-Bit microprocessor, to provide a highly integrated system console.

The main system console consists of an iAPX 186 microprocessor CPU with up to 1 Mbyte of DRAM controlled by an 8208 DRAM Controller. The 8208 DRAM Controller directly drives memory and provides refresh and timing control. An 8MHz 80186 allows use of 150 ns DRAMs with the 8208 to provide zero wait state performance. The remainder of the system console consists of two boot/diagnostic EPROMs, system real time clock, disk interface, and the primary serial station which links each peripheral subsystem.

The disk interface subsystem uses an 82062 Hard Disk Controller to support up to four disks, and an 8272A Floppy Double Density Disk Controller to support up to four floppies. DMA support for the disk subsystem is provided by one 80186 DMA channel. This DMA chan-

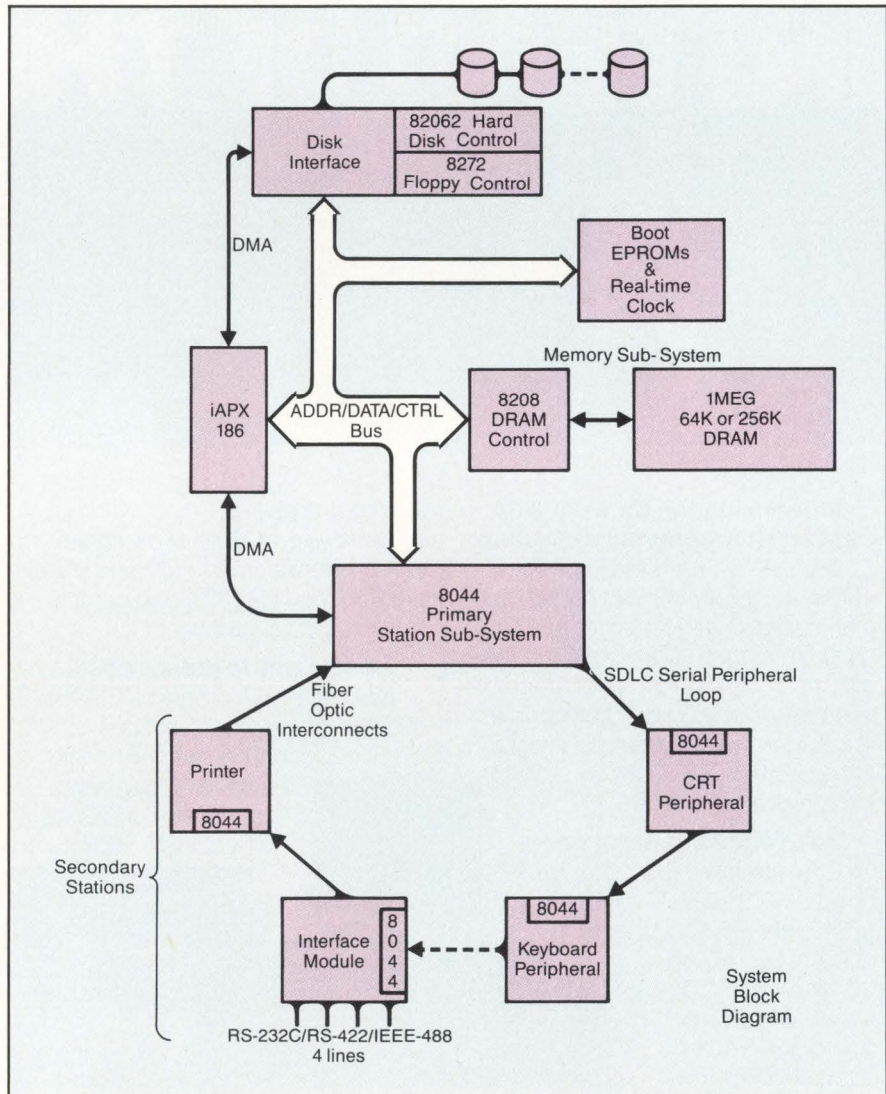
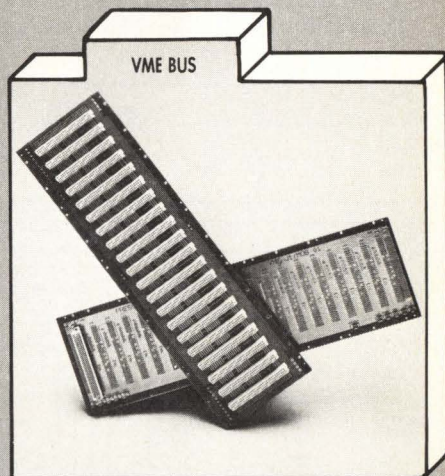
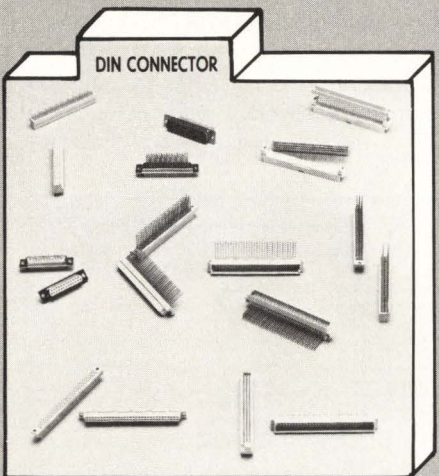
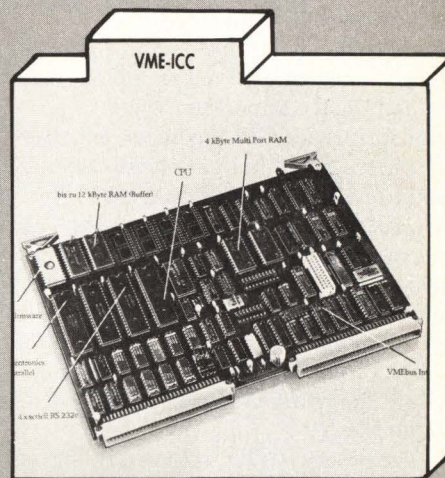
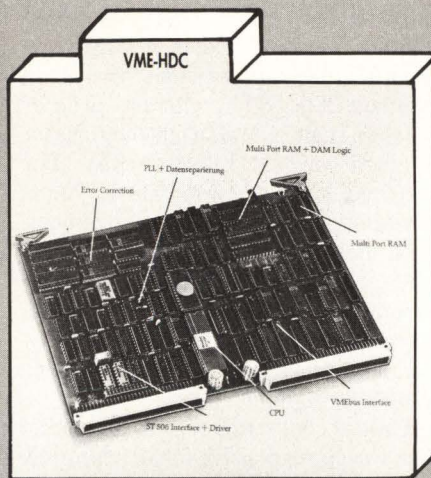
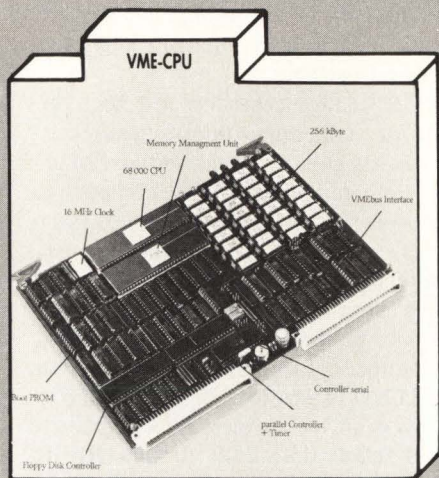


Figure 1: System block diagram illustrates workstation designed around the Intel 80186, plus a distributed peripheral architecture providing system modularity.

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- 6809 CPU
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VME-ICC

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nel is multiplexed between the hard and floppy disks as needed. Using this interface for bulk transfers leaves the serial peripheral loop free to support CRTs, keyboards, printers, plotters, and special I/O devices.

Up to this point, the system architecture is conventional, using highly integrated VLSI components wherever possible to provide CPU, memory, and disk resources. All other peripherals, which would normally reside on the CPU bus are distributed across a serial link. The peripheral link in this design is a high speed (375K baud), low cost, self-clocked serial path using SDLC loop protocols for link control. Loop architecture combined with self-clocked data allows a single data path to link all system modules.

The primary SDLC station residing on the main system console is based on Intel's 8044 microcontroller. This 8044 is

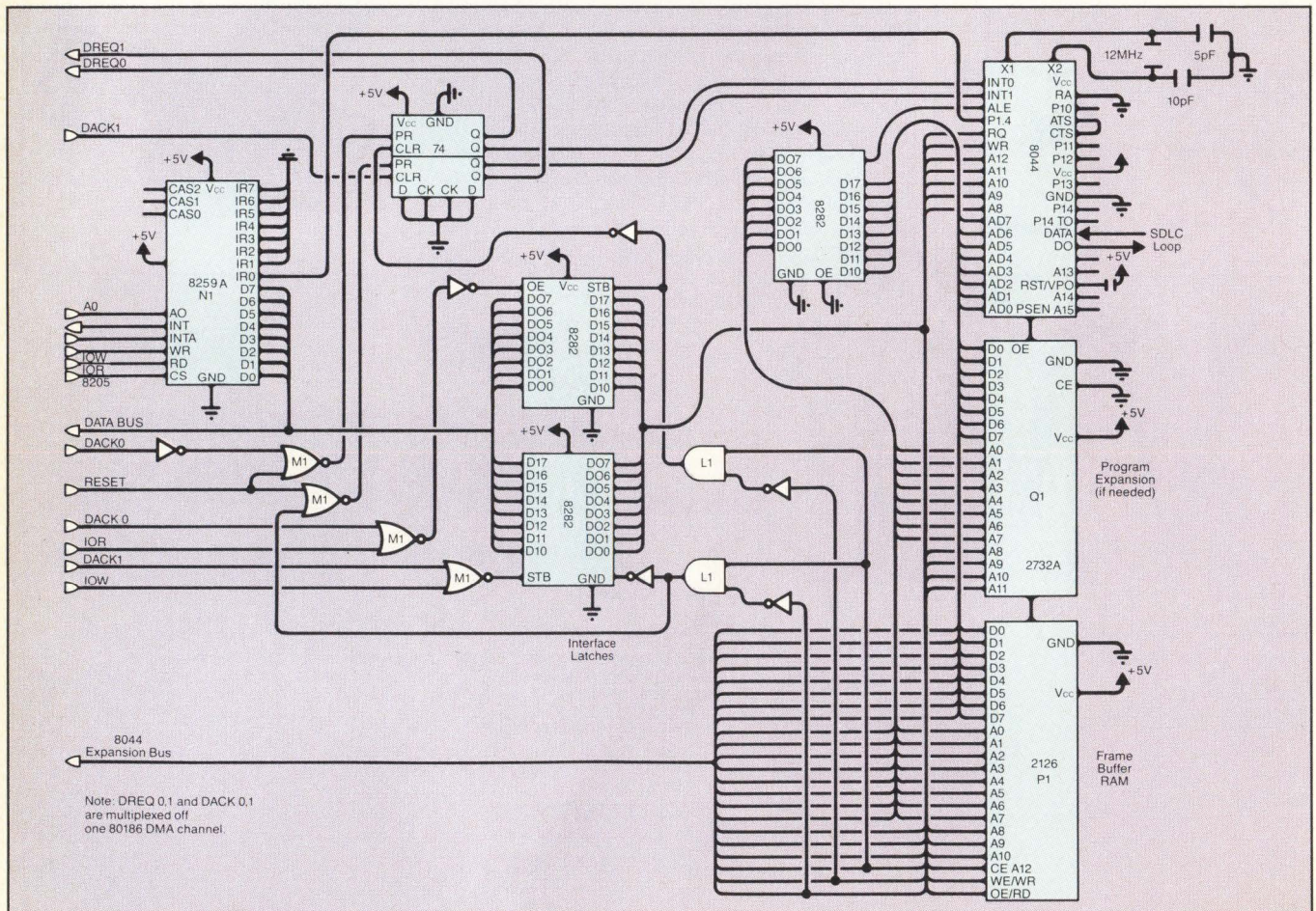
dedicated to running the serial network and driving the 186 data and command interface. The 8044 to 80186 hardware interface is detailed in **Figure 2**. One 186 DMA channel drives the send/receive ports to the 8044. In turn, the 8044 handles the data and command ports from the 186 and provides serial loop control. The 8044 can pre-process incoming data or format outgoing data for specific device requirements. For instance, format conversion to suit a particular printer can be handled here, with the details hidden from the main CPU. Serial loop transmit and receive functions are handled by the 8044's Serial Interface Unit, thus reducing the communications processing load and increasing system throughput.

Until recently this type of peripheral link was too expensive for attaching low cost peripherals such as dumb terminals or inexpensive dot-matrix printers. Using the 8044 microcontroller for link control, as well as the peripheral function, solves part of the interconnect problem. Problems of cabling cost, size, EMI, and data

rate support must also be addressed. Since Intel has a loop configuration for peripheral interconnects, fiber optics is a good transmission medium. This reduces system restrictions concerning module placement, eliminates possible cable EMI problems, and provides excellent data security.

Recent advances in low cost, high performance fiber optic transmitters/receivers have significantly reduced cost for this type of interconnect. These components plus inexpensive plastic duplex fibers are fine for data rates and distances used in this design. Such devices are available from Hewlett-Packard Opto electronics in their HFBR series, and from Motorola's Fiber optic Low-Cost System (FLCS). Prices for the transmitter/receivers in these lines are competitive with standard RS-232C drivers. HFBR-1502 transmitter from Hewlett-Packard, combined with the HFBR-2502 receiver, can support data rates of 1 Mbaud up to 22 meters. This is the device selected for peripheral interconnects. **Figure 3** shows the interface between the 8044

Figure 2: The 8044 Primary Station Subsystem.



The 8044 Sub-System Controller

The 8044 is a complete peripheral sub-system controller (Figure 1). It contains CPU, program memory, data memory, parallel I/O, timer/counters, plus a serial processor which directly supports the high speed SDLC serial interface on a single chip. CPU and peripheral functions are identical to the 8051 single-chip microcontroller except for a larger data memory (192 bytes) and special HDLC/SDLC serial processor.

The serial port or Serial Interface Unit (SIU) is a processor in it's own right and operates concurrently with the CPU, off-loading most of the SDLC link control tasks. The SIU implements a SDLC protocol subset directly in hardware, and contains on-chip support for SDLC loop mode used in this application. The SIU responds to polling sequences from the primary station automatically. A complete frame may be transmitted in response to a poll with no intervention from the 8051 CPU. Acknowledgement of received frames is also handled transparently by the SIU processor. This "Auto" mode provides fast turnaround time and a simplified software interface to the serial link. In Auto mode the 8044 acts as a normal response mode secondary station adhering strictly to IBM's SLDC definitions.

The Serial Interface Unit (SIU) to 8051 processor interface is through dual-port RAM and registers. This allows the SIU to run concurrently with the main 8044 CPU. The SIU can be programmed to act as either primary or secondary station of a SDLC loop. In this application, the system console 8044 acts as primary station, and each peripheral system 8044 acts as a secondary station. These secondary stations run in "Auto" mode, supporting many automatic communications operations without CPU overhead.

To receive a frame in Auto mode, the CPU writes a buffer start address and receive length into two on-chip registers. The

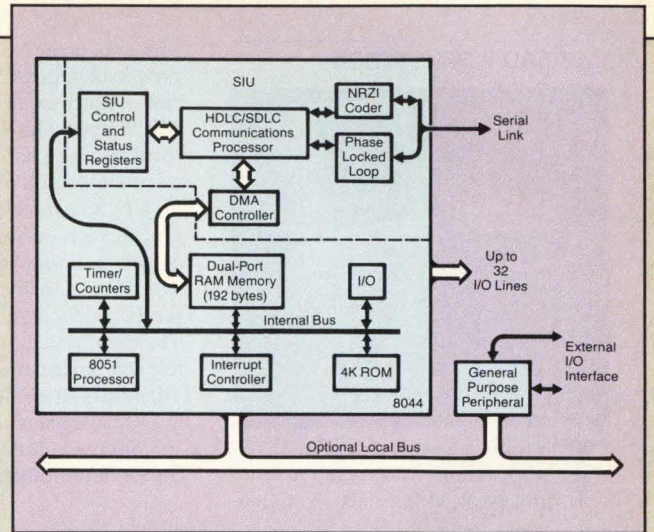


Figure 1: 8044 block diagram.

SIU receives the frame, verifies the Frame Check Sequence, examines the control byte, and takes appropriate action. If the frame is an information frame, the SIU will load the receive buffer, interrupt the CPU (to have the receive buffer read), and issue the acknowledgement to the primary station automatically.

To send a frame, the CPU fills the transmit buffer and writes buffer start address and length into two on-chip registers. The SIU sends the frame, complete with proper sequence numbers, when the Go Ahead flag is received. After the frame is transmitted the SIU waits for acknowledgement. If the acknowledgement is negative the frame is retransmitted, otherwise the SIU interrupts the CPU to signify transmission is complete. This entire sequence occurs without intervention by the 8051 CPU.

and the fiber link.

The physical interconnect mechanism for the loop consists of two fiber strands, one for inbound and one for outbound data. Each module interconnect uses an optical receiver to accept loop data, with an optical transmitter providing the link to the next station. A switch in each module connector identifies the final outbound module by absence of additional cable connections, and turns the inbound route back to the main system console, via the inbound fibers. This daisy chain arrangement allows simple physical bus construction of the logical SDLC loop and supports automatic reconfiguration of the peripheral network. To add a peripheral to Intel's workstation, simply attaching the snap-in cable at the end of the daisy chain extends the loop to support the new device.

The system supports multiple CRTs,

keyboards, several printers, plotters, and other specialized devices. Some of these devices will be designed with the 8044 as the total solution, such as the dumb CRT,

keyboard and printer.

— Michael K. Webb,
Intel Corporation

Write 224

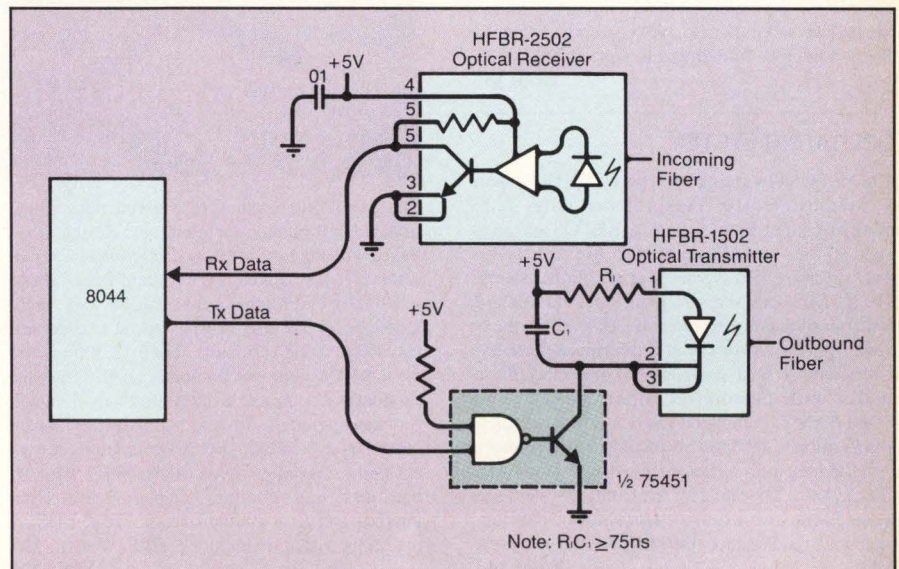
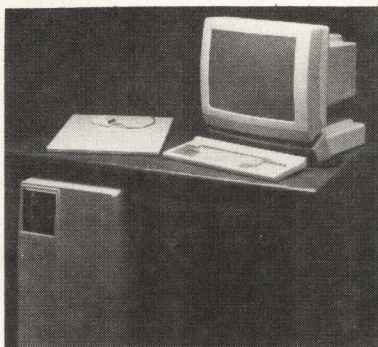


Figure 3: The 8044 link to optical interconnect.

CAE/CAD WORKSTATION



The Saber Station is a CAE/CAD workstation whose application processor utilizes the National

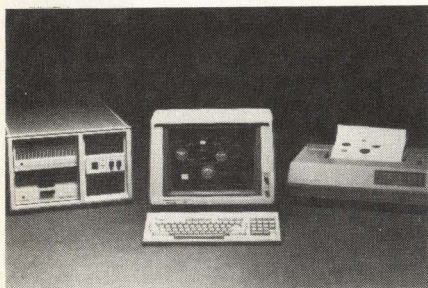
Semiconductor NS32032 32-bit micro-processor. Operating at a 10 MHz clock rate, it executes an instruction set at 1.2 MIPS. It provides demand-paged virtual memory and a hardware floating-point co-processor. Industry-standard Berkeley UNIX is provided. The workstations graphics processor uses a 32-bit, 20 Mbyte per second op-code/data bus structure. Image memory is 1664 × 1248 pixels, producing a 2-megapixel display. The basic system is available with two-to-eight image planes per pixel. The expanded system allows expansion of up to 24 image planes and a color pallet of 16 million colors. Price is \$40,000. **Saber Technology**, San Jose, CA
Write 128

H P-BASED CAD SYSTEM



Artech is a CADD workstation that includes a 32-bit Hewlett-Packard computer and can be connected in a network. The system displays two- and three-dimensional images on a 19" color screen, and utilizes a graphics tablet. A fully configured system includes workstation, dual disk drive, a D-size plotter, and SKOK's Arplan two-dimensional design and drafting software. Price is \$27,000. **Skok Systems**, Cambridge, MA
Write 139

STRUCTURED ANALYSIS TOOLS



The Structured Analysis Tools are targeted to provide front-end system and software requirements definition through graphic editing, error checking, error correcting and data output techniques. The SA Tools include a graphic editor which allows the entry and modification of data flow diagrams, and formats the diagrams in accordance with SA notation. Another tool checks for errors such as undefined data paths and syntax errors in the data dictionary. A third checks the consistency of the analysis, including relationships between elements at different levels in the hierarchy. A formatting tool allows the analysis to be output to color copiers and plotters. Price is \$9,500. **Tektronix**, Beaverton, OR

Write 135

SOLIDVIEW SYSTEM

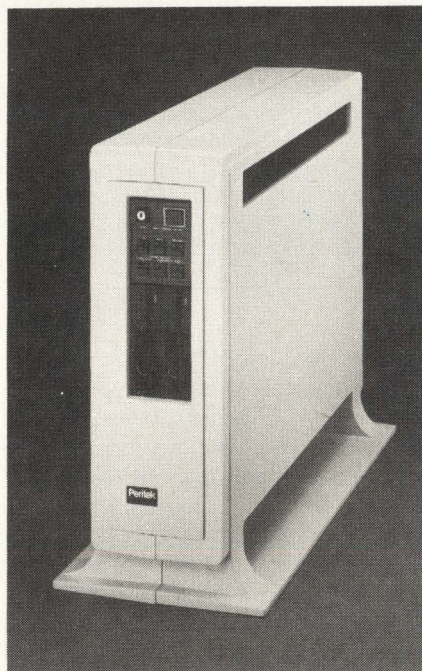
This 1280 × 1024 version of Lexidata's Solidview display system generates line drawings and solid images. The Model 34SV-3 has eight image planes, a 12-plane depth buffer, a color look-up table capable of displaying 256 colors simultaneously, a serial communications processor, and a 19" color monitor. Options include parallel interfaces to several minicomputers, three-axis joystick, data tablet, and keyboard. Price is \$39,500. **Lexidata**, Billerica, MA
Write 138

PERSONAL ENGINEERING WORKSTATION



The EAS/300 personal workstation provides an integrated environment for electronic design when linked with the EAS/770 workstation and PCX software. Net-list data can be extracted from various levels of the hierarchy to feed data for logic simulation, or for physical board layout via an integrated EAS/700 PCB CAD system. The EAS/300 is based on the IBM personal computer. EAS offers the product as a complete turnkey workstation, or will provide upgrade hardware and software kits for customer-owned IBM PC/XT computers. A typical hardware configuration includes 640K of RAM, hard disk, color monitor, graphic mouse, serial interface and network controller. The IBM-DOS 2.1 operating system is included. **EAS**, Boston, MA
Write 133

SPEECH DATA ENTRY SYSTEM



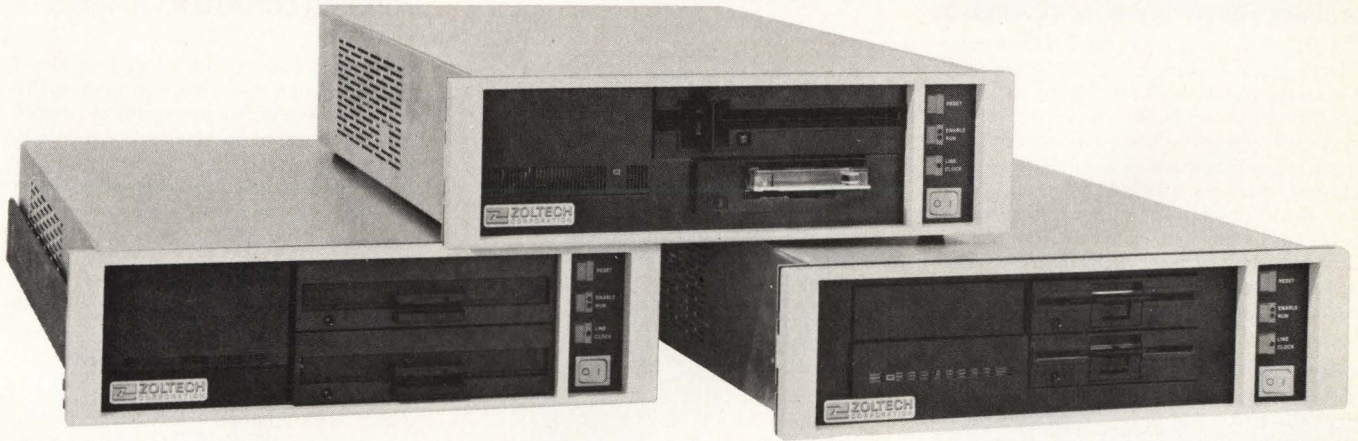
The Model 3015 voice data entry system allows four users to share one speaker dependent, continuous speech processor. The system is able to connect to any computer that supports RS-232C interfaces. The Model 3015 has a vocabulary of 360 words, which can be divided among four users to supply them with independent application vocabularies of 90 words each. Users enter data sequentially and the system recognizes the current user by processing the input through a speech input multiplexor, which transfers the input to the single speech processor. An applications interface provides buffering and message table translations, in addition to interface control to the user's host computer system. **Verbex**, Bedford, MA
Write 132

OPERATING SYSTEM

The XELOS Operating System is a UNIX System V derivative for the Perkin-Elmer Series 3200 family of superminicomputers. XELOS software includes the MenuMaker interface to create menus that customize XELOS based application systems. The XELOS operating system includes the standard AT&T command interpreter shell, as well as the C Shell from the University of California at Berkeley. Users who so wish can augment or replace these shells with customized interfaces. C and FORTRAN-77 compilers, a Series 3200 assembler, and a symbolic debugger are included in the software development tools packaged into the XELOS operating system. The Source Code Control System and Make Facility were designed for software development and maintenance. **Perkin-Elmer**, Oceanport, NJ
Write 144

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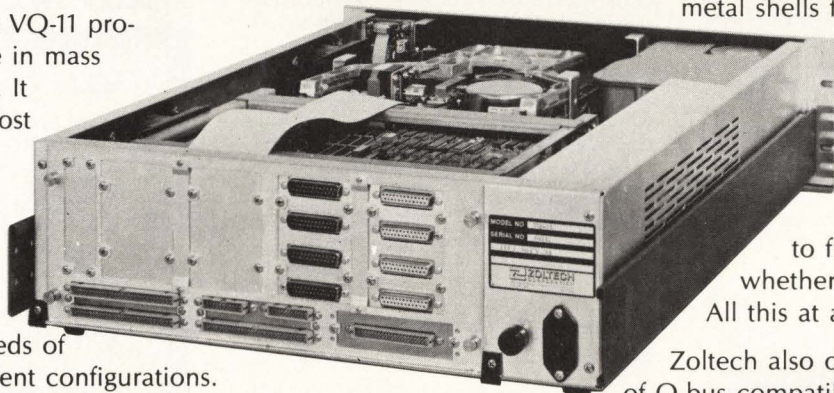
The flexibility of the VQ-11 does not stop with mass storage. The 8x4, 8x2 and 4x4 card cages provide the full 22-bit Q-bus at all slots. The I/O distribution panel is compatible with the Micro/PDP-11 while providing more flexibility. In addition to the illustrated rack-mount enclosures, the VQ-11 is also available in desktop and floor-standing versions.

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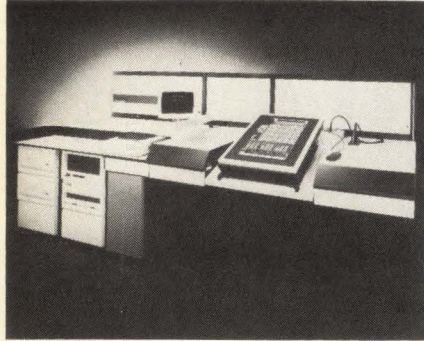
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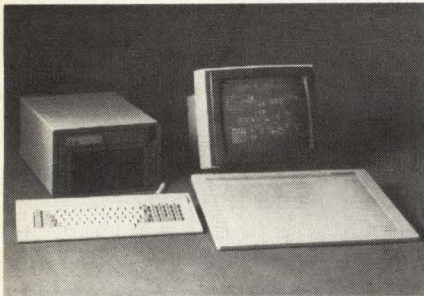
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BOARD TEST SYSTEM



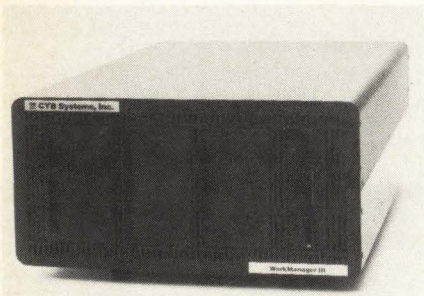
The L280 test system includes peripherals for operator/programmer interaction. A VT240 Operator's Monitor, is mounted on a rotating arm and may be tilted to the viewing angle of the operator's choice. A plain paper printer is housed in the system's cabinet. It may be plugged into jacks on either side of the fixture. A hand-held Control Module replaces the Operator's Console for interaction with the test system during production operation. The system is designed for testing boards such as the 8088, 68000, gate arrays, and custom LSI. Price starts at \$425,000. **Teradyne**, Boston, MA **Write 141**

MONOCHROME AND COLOR CAD/D SYSTEMS



Terak Corp. enhanced their CAD/D Systems by adding a 10 Mbyte hard disk drive, 15" monochrome monitor, a 12" x 17" CAD/D digitizing tablet, and a low-profile adjustable keyboard. The systems are called the Terak 8510/10 Monochrome CAD/D System and the Terak 8600/10 Color CAD/D System. They incorporate a 1.2 Mbyte floppy disk drive and a 10 Mbyte 5 1/4" Winchester hard disk. The new monitor has 640 x 480 x 2 resolution. Price starts at \$12,500. **Terak**, Scottsdale, AZ **Write 137**

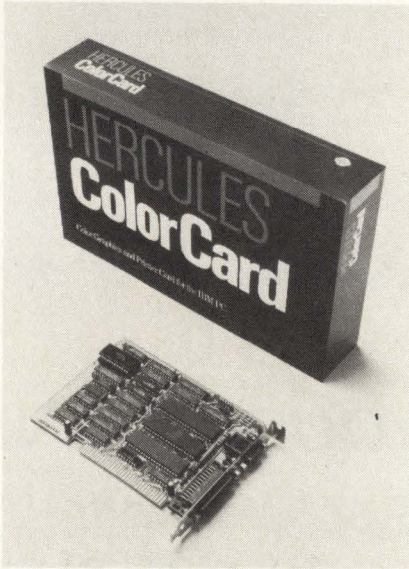
UNIX SYSTEM V-BASED SUPERMICROS



CYB Systems has added three systems to its family of UNIX System V-based supermicrocomputers. The systems are called WorkManager II & III and

the WorkMaster. The WorkManager II & III are based on a 10 MHz MC68000 processor, while the WorkMaster uses the MC68010. All three systems use Multibus IEEE-796 architecture. The WorkManager II & III offer 10 disk drive options in floppy, Winchester and SMD formats ranging from 10 to 474 Mbytes. Both the Work Manager II & III use the UniSoft implementation of AT&T's multiuser UNIX System V operating system and have memory that may be expanded to 4.5 Mbytes, and offer disk storage of up to 594 Mbytes. The WorkMaster has memory expansion of up to 8.5 Mbytes and disk storage of up to 1,116 Mbytes. Any of the three systems may be configured with 18 I/O ports, a floating point processor, and Ethernet options. Price starts at \$10,383. **CYB System**, Austin, TX **Write 140**

COLOR CARD FOR IBM PC



The Hercules Color Card for the IBM PC is half the size of the IBM graphics monitor/adaptor card and can be inserted into one of the XT's short expansion slots. The Color Card is compatible with all color graphics software for the IBM color card such as Microsoft Flight Simulator, Logo, and Supercalc III. The card can also be kept in the system at the same time as the Hercules Graphics Card, which provides graphics capabilities for the monochrome display of the IBM PC. The card is supported by software packages including Lotus 1-2-3, Microsoft Word, Chartmaster, AutoCAD, Halo, and PS. Price is \$245. **Hercules Computer** Berkeley, CA **Write 143**

COMPUTER-AIDED ENGINEERING SYSTEM

The CIEE system supports the design of PCB, Hybrid, Gate Array, Standard Cell and Full Custom chips. Outputs include NC drills and profilers, pattern generators, automatic component insertion and automatic test equipment. DEC VAX computers are used in conjunction with Racal-Redac's V-Series workstations for PCB design. The A-Series are based on Apollo systems. IBM personal computers are needed for data capture and engineering capabilities to complement other workstations. A relational database which enables data transfer between all workstations and software packages. **Racal-Redac**, Westford, MA **Write 142**

VLSI DESIGN WORKSTATION

The Chipmaster is a CAE workstation which enables integrated-circuit designers to address the complete design cycle of custom VLSI chips from logic design to mask set definition, including simulation and test development. Based on Intel's 80286 microprocessor, Chipmaster has a hardware graphics accelerator to meet the data requirements of VLSI chips. The Chipmaster has a VLSI mask editor, called MAX. The system includes a 32-bit data base and an 80-million-pixels/sec color graphics accelerator. Price is \$126,000 per terminal. **Daisy Systems**, Sunnyvale, CA **Write 145**

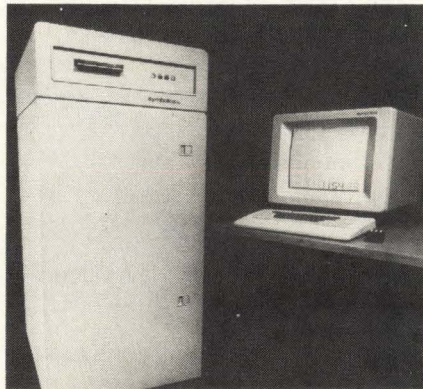
MODULAR COMPUTER GRAPHICS SYSTEM

The Perigraf 1 computer graphics system has an open-architecture design based on the Q-bus. The bus accepts nine Peritek graphic display controller cards, color and monochrome, dot graphics and alphanumeric. A single LSI-II/73 CPU is standard. A 42 Mbyte hard disk drive and two DDDS 96 tpi minifloppy disk drives are mounted on a plug-in module. Software includes multi-terminal RT-II, Peritek's image editor (paint) system, along with GKS-compatible routines. A mouse is optional. **Peritek**, Anaheim, CA **Write 131**

INTERACTIVE PCB CAD SYSTEM

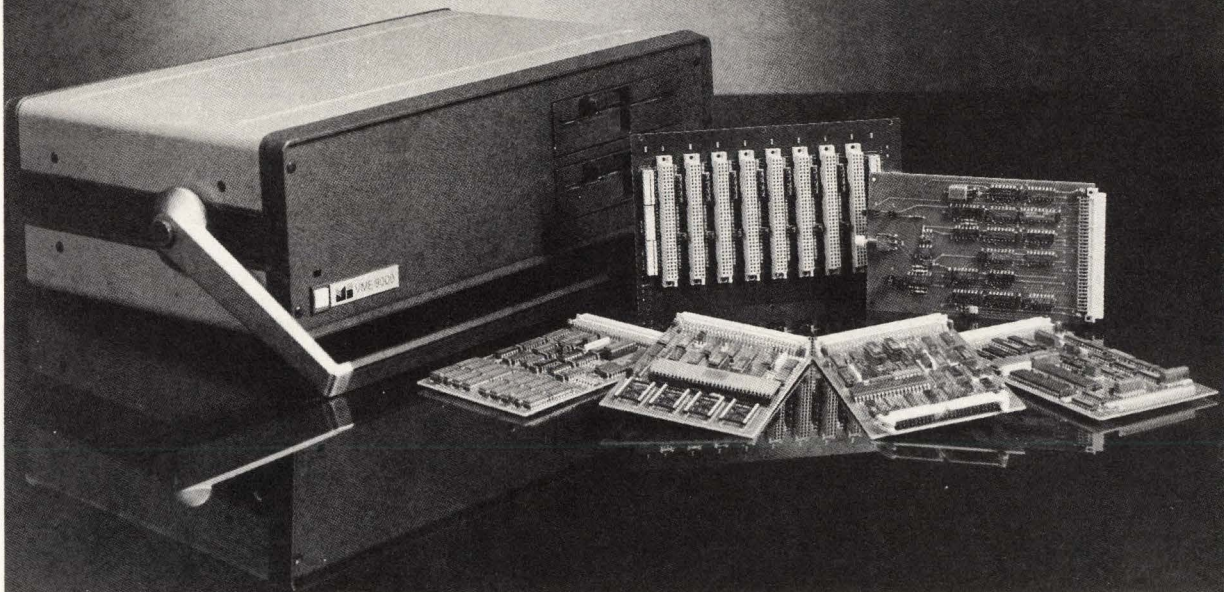
The Circuit Master is a fully interactive, PCB CAD system which features Demand Routing and Wave Tracer allowing the designer to interactively perform complete or partial routing, either manually or automatically. A Demand Component feature routs the board in the shortest possible time. The system also includes automatic placement, gate and pin swapping, rats nest, and density histogram routines. The Circuit Master system generates a paper tape for NC drilling, can provide a printed wirelist for verification, and provides the output to photoplot a positive 1:1 or scaled artwork of the various layers of the board. Price is \$69,950. **Bishop Graphics**, Pasadena, CA **Write 127**

SYMBOLIC PROCESSOR



The Symbolics 3670 symbolic processing computer features a backplane with 14 optional expansion slots and can support 30 Mbytes of physical memory. The processor has one Gbyte of address space. An FPA option executes floating point operations in parallel with data-type checking in the 3670. Its I/O Processor implements a buffered, pipelined pixel memory system for the graphics console. The 3670 disk drive alternatives are 167.5 or 474 Mbyte fixed media disks or a 300 Mbyte removable media disk. Price is \$84,500. **Symbolics**, Cambridge, MA **Write 130**

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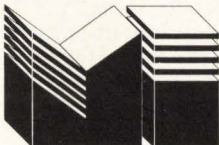
These larger size modules (233mm x 160mm) allow more functions per board, giving you the capability of implementing a high performance computer system configured to the user's needs. Performance is improved because fewer bus accesses are needed. Call Mizar for double height VMEbus modules including a 68010 CPU module with serial and parallel ports. EPROM sockets, dual ported dynamic RAM and system controller functions, a 1 Mbyte dynamic RAM module, a Winchester and floppy disk controller, CMOS battery-backed RAM, Dual Channel GPIB Controller and a graphics module offering 3 planes of display memory with 1024 by 1024 resolution.

Software and Systems

CP/M-68K™ is a single user system for the VME9000 or the VME9100 based on Digital Research's popular 8 bit CP/M. CP/M-68K has been completely rewritten to run on the 68000 and offers built-in commands, including DIR, DIRS, ERA, REN, SUBMIT, TYPE and USER. Standard utilities include DDT-68K, ED, PIP, STAT, archive (AR68), DUMP, relocation (RELOC), SIZE68 and SENDC68. Programming tools include a 68000 assembler (AS68), an object file linker (LO68) and a "C" Compiler.

For those users who need a real-time multi-tasking operating system, Mizar offers OS9/68000™ from Microware Systems Corp. OS9/68000 is a Unix-like operating system that has been optimized for low-cost, high performance applications in personal computers, industrial control systems and general-purpose multi user systems. OS9/68000 offers such features as hierarchical disk directory structure, ROM-able code for use with or without a disk system, UNIX™ software compatibility at C source code level and language support for Basic, C, Pascal and Fortran 77.

CP/M is a trade name of Digital Research
OS9/68000 is a trade name of Microware Systems Corp.
UNIX is a trade name of Bell Labs



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COLOR GRAPHICS CONTROLLER Graphics to IBM PC



The Q1000 and Q1080 are two versions of Quintar's stand-alone color graphics controller which enable an IBM PC to interface with a high-resolution color monitor, large screen video projector or slide making device to produce graphics output. The Q1000 has two pages/screens of display, each in 512×512×4 resolution, while the Q1080 offers 832×630×4 resolution. Both controllers have a Z-80B (6MHz) CPU and a NEC 7220 graphics display controller chip and 16K of RAM for program, I/O, or communications buffers. The devices have 256 Kbytes of display memory, 32K of EPROM, two RS-232C serial ports and one 8-bit parallel interface. Prices are \$1,995 (Q1000) and \$2,195 (Q1080). **Quintar**, Torrance, CA **Write 176**

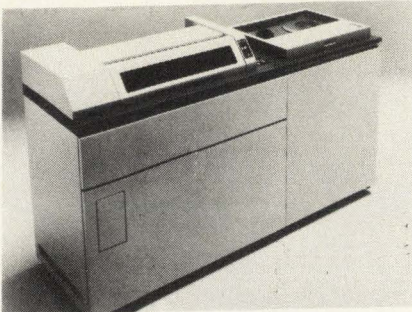
VIDEO BANDWIDTH SIGNAL PROCESSOR

The SP-123 signal processor operates at 14.3 Mpixels/sec and has 768×512 spatial resolution. Pixel control allows an arbitrary, user defined area, to form the bounds of image processing operations. Hardware on the two mother/daughter board pairs include an 8-bit multiplier, 2 Kbyte look-up tables, 16-bit ALU, and a programmable clipper and rotator. Real time processes include spatial filtering, acquisition, image multiplexing and discontinuous transforms. **Datacube**, Peabody, MA **Write 164**

MAGNETIC TAPE SYSTEM

The Series Ten GCR Magnetic Tape System performs dual density 800/1600 cpi or tri-density 800/1600 at 75"/sec and 6250 cpi at 45"/sec. The system is plug compatible with the HP operating system and DVR23 driver. Features include transfer rates of 280,000 bps a second, single board interface in M/E/F chassis and DVR23 plug compatibility. Prices are \$17,390 (dual-density) and \$19,995 (tri-density). **Dylon Data**, San Diego, CA **Write 177**

ELECTROSTATIC GRAPHICS PLOTTER

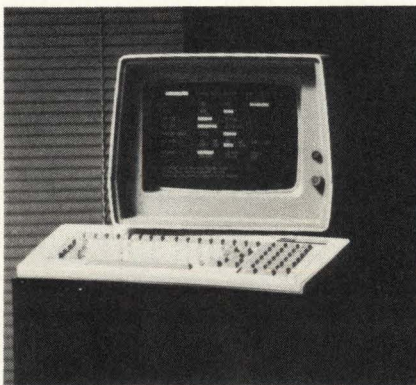


The CIE-2400 and the CIE-3600 are 400 dpi electrostatic graphic plotters which are compatible with IBM, VAX and other mainframes. The plotters have a built-in vector-to-raster converter and feature plotting speeds of .93 and 1.1 ips. The plotters' have RS-232C and high-speed RS-422A interfaces. Users can plot drawings in vector format for pen plotters and have 2 Mbyte of buffered memory to store 200,000 vectors. Price is \$45,000-\$65,000. **C. Itoh Electronics**, Irvine, CA **Write 172**

MICRO TO MAINFRAME COMMUNICATIONS

IRMA is an IBM 3270-based, micro-to-mainframe communications for decision support environments. IRMA fits into the PC backplane and attaches via coaxial cable to most local or remote IBM 3270 controllers. IRMA allows an IBM PC to emulate an IBM 3278 or 3279 terminal. The link includes text and binary file transfer which operates under MVS/TSO EDIT or VM/CMS XEDIT modes. Users can capture mainframe data files, transfer files from a PC to the mainframe, or transfer data from PC to PC by using the mainframe as an intermediate storage facility. Price is \$1,195. **DCA**, Norcross, GA **Write 169**

INTELLIGENT TERMINAL



The VTZ 3/20 series of intelligent terminals for system 8000 supermicros uses a 12" CRT with dynamic focusing and a 25-line by 80- or 132-column display. The 103-key, detachable low-profile keyboard is configured with 16 function keys each with two shift modes, allowing 32 individually programmable sequences. The VTZ 3/20 has 256 graphic characters and 128 alphanumeric characters as well as four display pages of memory, RS-232 and RS-422 communications ports for the host computer and an RS-232 printer port. The VTZ 3/20 may be used with any of the four System 8000 models, which support eight to 24 users and up to 672 Mbyte disk storage. Price is \$1,295. **Zilog**, Campbell, CA **Write 184**

MULTIPLEXER FOR MEMOREX CONTROLLERS

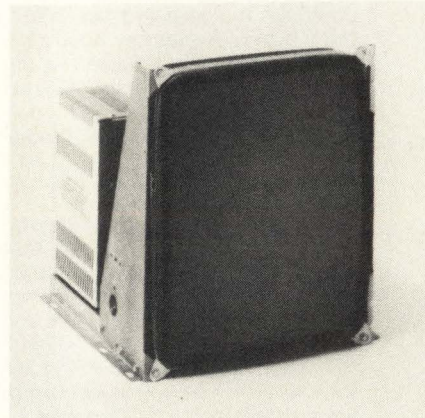


The FM1699 is a fixed 8-port coaxial cable multiplexer designed for users of Memorex controllers and IBM 3274/A local and remote control units. The multiplexer operates with all Memorex Category A peripherals by connecting 8 ports from a Memorex or 3274/A controller at a distance of 4,000 ft over a RG 62 A/U coaxial cable. At the peripheral side, a second Model FM 1699 connects to the sole coaxial cable and permits eight peripherals to be served. Price is \$2,200. **Fibronics**, Hyannis, MA **Write 163**

INTELLIGENT TERMINALS USE MS-DOS OR CP/M-80

The 8200 VIS (Very Intelligent System) Series combines universal terminal emulation with 8- and 16-bit processing capabilities. The VIS units support emulation for IBM 3275/71/77, DEC VT 100/200, ADDS Regent-40, Data General 410/460 and UTS 30/40, U100/200. The series includes an 8 MHz or 10 MHz MC68000 with 1,024 Kbyte RAM, 128 Kbyte EPROM and 2 Kbyte EAROM. Users have a choice of MS-DOS or CP/M-80 as well. The MS-DOS CPU option adds an 8 MHz 8088. The CP/M-80 PC option features a 4 MHz Z80 processor. Price in volume discounts is \$4,350. **Megadata**, Bohemia, NY **Write 157**

MONOCHROME DISPLAY OFFERED IN THREE SIZES



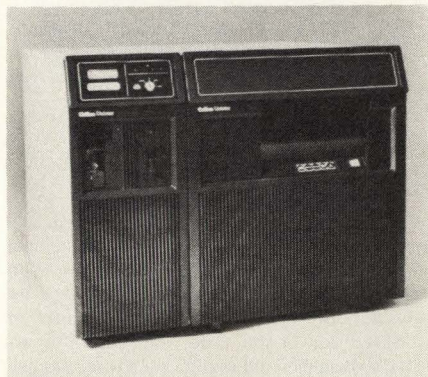
The HD100 series are high resolution monochrome displays available in three sizes: 15", 17", and 20". The monitors use a switching power supply which has a reduced cabinet thermal rise and wide input line voltage operation. The transformer size and component count of the switch mode supply has been reduced which lowers the overall display weight. The displays use 1% metal film resistors, NPO ceramic capacitors, and 100ppm cermet pots. **Ball Electronic Systems Div.**, St. Paul, MN **Write 161**

THREE PORT MODEM



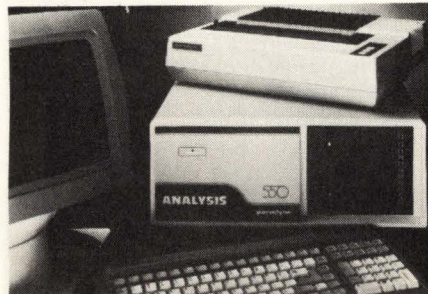
The TriMux.212 is a triple port modem which allows three computers and peripherals to simultaneously share one dial-up line. The TriMux.212 has a three-channel statistical multiplexer with an auto dial/auto answer Bell 212A modem. Data from three devices can be multiplexed onto a dial-up call, and the modem provides retransmission in case of transmission line errors. When the modem is not being used, any of the three local devices can communicate with each other, and devices running at different speeds can communicate with one another transparently. Price is \$1,495. **Complexx Systems**, Huntsville, AL **Write 167**

EXPANSION UNIT FOR UNISTAR 300



The Peripherals Expansion Module designed for the UNISTAR 300 has a nine-track streaming tape and incremental back-up mode. The module supports 10" reels of 1/2" tape at 1600 bpi, and a 474 Mbyte SMD Winchester disk drive with 17 ms of average access speed. When set up in a network, the Peripheral Expansion Module can function as a file-server and backup server. Price is \$9,950. **Callan Data Systems**, Westlake Village, CA **Write 160**

NETWORK CONTROLLER

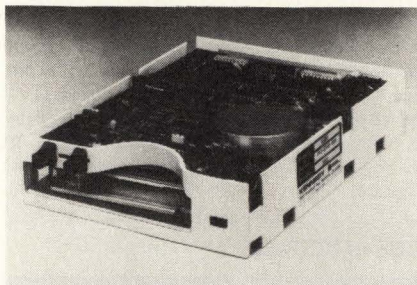


The Analysis 550 network controller manages from one to 10 lines while monitoring line, terminal and modem problems at 512 locations. Analysis 550 tracks line impairments and analyzes data from network locations on a continuous, non-interfering

basis. Modem diagnostic microprocessors extract information on the condition of the phone lines. Analysis 550 control allows software-generated configuration strapping options of Paradyne MPX modems to be downline loaded. A user can display the strapping configuration of any modem in the network. Price is \$12,500. **Paradyne**, Largo, FL

Write 183

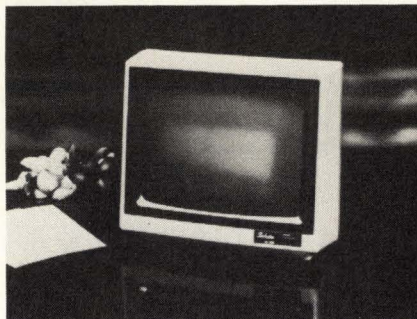
60 MBYTE STREAMING CARTRIDGE



The Series 6500 is a 5.25" streaming cartridge transport which has 16 Kbyte buffer storage and a 90 ips operating speed. The nine-track transport has two-track stepping heads and a formatted capacity of 60 Mbytes with a 600 ft cartridge and 45 Mbytes with a 450ft cartridge. Time to backup 60 Mbytes is 12 minutes.

The series 6500 is available in full-height configuration with formatter card installed and half-height without formatter. The formatter adopts the QIC-02 drive interface standard and also is compatible with the ANSC X3T9.6/83-20 interface definition along with the QIC-II and QIC-24 tape format which allows media interchangeability among transports. The drive-level interface is QIC-36. Price is \$1,275. **Kennedy**, Monrovia, CA **Write 216**

AMBER MONITOR



The Sakata SA-1000 is a 12" CRT display amber monitor which includes a composite video input signal, scanning frequency of 15.75 KHz (horizontal) and 60 KHz (vertical). The monitor has a resolution of 900 dots center and 800 dots corner and includes a RCA jack input connector and 2,000 characters display format. Price is \$159. **Sakata**, Elk Grove Village, IL **Write 179**

10 PEN DIGITAL PLOTTER

The FP 5301 is a B/A3 size 10 pen plotter for CAD, engineering and graphics applications. The FP 5301 has a speed of 17.7" ips axially and 25" diagonally. The plotter has several pen types and a built-in pen sensor detects the type of pen and the necessary plotting speed and pressure. The FP 5301 is available with RS-232C, GPIB/IEEE-488 or 8-bit parallel interfaces. The unit has GPGL and HP/GL compatibility. Price is \$3,000. **Western Graphtec**, Irvine CA **Write 178**

FIBER OPTIC BUS EXTENDER



This fiber optic bus extender is designed to remotely locate graphics display workstations up to 2KM from the host. The CBE-200, a parallel-to-serial/serial-to-parallel multiplexer, with the DMA interface module connects to the UNIBUS or Q-BUS. It communicates 500 Kwords/sec over two fibers. The CBE-200 is plug compatible with ribbon cable off the DRII-W interface providing the user with a single cable, single link solution. **Canoga Data Systems**, Canoga, Park, CA **Write 159**

3.2 MBYTE FLOPPY DISKETTE

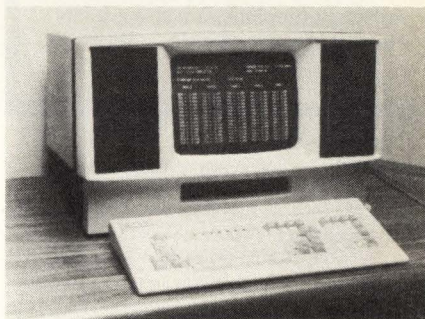
The Model 1865 is a half-height 5.25" floppy disk drive which can store 3.2 Mbytes of data. The 1865 records at 10,250 bpi and 170 tpi. Track-to-track access time is two msec with buffered seeks. The drives proprietary read/write head positioning technique allows diskette interchangeability at 170 tpi. Price is \$330. **Amlyn**, San Jose, CA

Write 181

CURSOR WITH COLOR-CODED KEYS

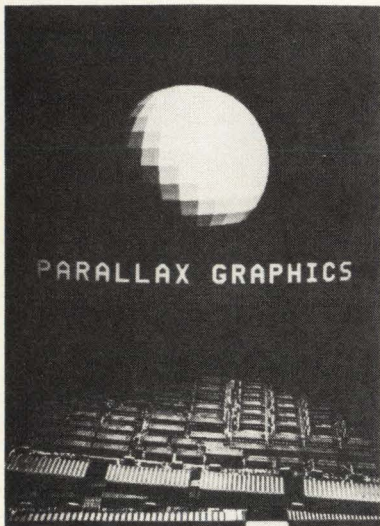
Models DP5-4CX and MD7-4CX are cursors for CAD digitizing functions. The cursors have painting, menuing and tracing features, and color-coded keys arranged for compatibility with one- and four-button digitizing cursors, as well as a three-button mouse. Price in quantities of 100 is \$210 (DP5-4CX) and \$120 (MD7-4CX) **GTCO**, Rockville, MD **Write 165**

32-BIT OFFLINE WORKSTATION



The Model 42 MultiTasker is a 32-bit offline autorouter/multitasking workstation which can perform as an additional node on PTC's Series 300 Network System, or as an offline workstation compatible with Paragon's 100A and 200A PCB design graphics workstations. Autorouting, design rule checking and data preparation functions operate concurrently with output tasks such as penplotting, photoplotting, magnetic tape generation and CAT report generation. The CPU is a DEC 32-bit LSI 11/73 running at 15 MHz; memory capacity is 512 Kbytes, and the system also includes three serial ports. The console accommodates an 8" floppy disk drive and a 20 Mbyte Winchester disk drive and controller. Price is \$30,000. **Paragon Technology**, Pleasant Hill, CA **Write 170**

GRAPHICS CONTROLLER



The Parallax 600 is a raster graphics controller which features a proprietary bit-slice drawing processor with 12 million pixels per second drawing speed. The controllers are available in versions for Multibus and Q-Bus microcomputers. The controllers provide a choice of 16 colors from a palette of 4096 in the 4-bit per pixel version, or 256 from a 16 million color palette in the 8-bit per pixel version. The controllers have dual-ported video memory, RS-170 video compatibility with gen-lock, two frame buffers, zoom, smooth pan and scroll. The controllers display 640 × 480 pixels out of a 512 × 1024 pixel memory with four bit planes. Versions with eight bit planes are also available. **Parallax, Sunnyvale, CA Write 198**

16-CHANNEL MULTIPLEXER

The MLSI-F-DZII-E is a 16-port DZII software compatible multiplexer for Q-bus computers, that upgrades FCC compliant DEC or MDB Micro/II workstations. The multiplexer subsystem includes a 3" by 5" distribution panel with 9-pin male connectors to bring out all functional signals of the multiplexer. Transmit and receive data signals can be transposed by use of jumper plugs, to minimize the different types of cables a user might require. 32 lines of multiplexed data can be installed into a 5/4" high chassis and two 25-pin connectors of each 16-channel distribution panel can be internally disconnected from the DZII circuitry by jumper plugs and connected to the two ports of an 11/23 PLUS CPU or MXVII module. Price is \$2,600. **MDB Systems, Orange, Write 212**

32-CHANNEL CONTROLLER

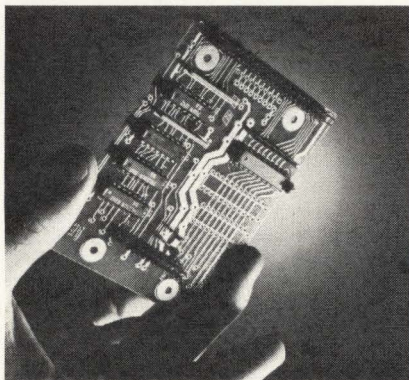
The EMC 5258 is a communications interface for all Prime-manufactured computers. The 5258 is capable of supporting 32 asynchronous channels

with a single card and operates under Prime's DMQ transfer mode, as well as under DMT mode. The EMC 5258 has 16 standard baud rates (up to 19,200 BPS) for any one of the channels, and the option to program baud rates for special applications. Price is \$6,500. **EMC, Natick, MA Write 190**

TAPE CONTROLLER

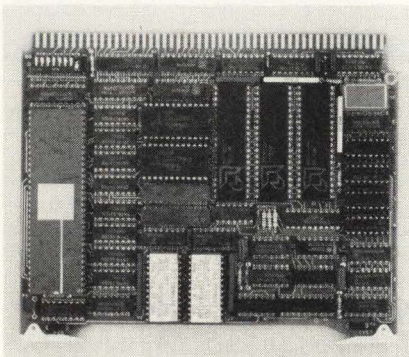
The Quartermaster is a controller for 1/4" tape drives. The Quartermaster controls four cartridge tape drives conforming to the QIC-2 interface standard, including 8" and 5 1/4" form factor drives from Archive, Cipher, DEI/Tandberg, Northern Telecom and Wangtek. The controller handles speeds of 90 ips drives, and provides access to 60 Mbytes of on-line storage per drive using a 600 foot cartridge, or 45 Mbytes using a 450 foot cartridge. Price is \$384. **Ciprico, Plymouth, MN Write 193**

BUS INTERFACE



The SASI-100 board converts the 8255A parallel port on the MCP8U-800 or MCP8U-900 board to a SASI bus compatible format. The SASI bus gives the user access to hard disk, cartridge disk, and streaming tape controller boards manufactured by Xebec, Shugart, DTC, and Western Digital. The SASI-100 connects to the microcomputer parallel I/O with CBL-26 and to the desired controller board with CBL-50S. Power is transferred to the SASI-100 thru CBL-26. **Miller Technology, Los Gatos, CA Write 206**

SINGLE CARD FFT PROCESSOR



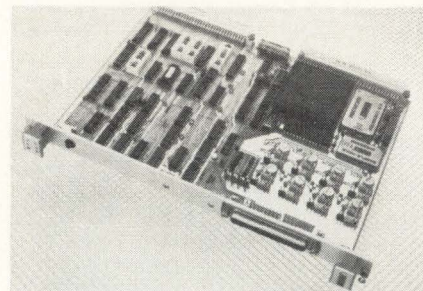
The Ariel FFT 523 is a single card FFT processor that plugs into a single backplane slot of Hewlett-Packard Series 200 desktop computers. An FFT is performed by execution of a single program line in BASIC or Pascal. Disk-based, machine-language driver routines, provided with the FFT 523, make the host/peripheral interface transparent to the user. Standard (PROM resident) algorithms include:

Forward and Inverse FFT, Hamming Window, and Power Spectral Density. The FFT 523 will transform arrays of up to 1024 complex points in 9.2 msec. Price is \$1,600. **Ariel, New York, NY Write 197**

COLOR GRAPHICS BOARD

The XL bit map graphics board has 1024 × 512 × 4 resolution and standard primitives which include vectors, arcs, circles, bars, and N-sided elliptical polygons. Standard drawing modes include combine, complement, force to color, draw behind and conditional draw and erase. The board has sixteen pixel addressable colors or eight colors with blink plus auto-dithering for 1000 simultaneously displayable colors. Text mode supports 24 or 48 line operation with four independent text areas definable as any group of lines and columns in display memory. The XL operates under ANSI X3.64 and is Tektronix 4010 compatible. Price is \$2,000. **Color-graphic Communications, Atlanta, GA Write 211**

ANALOG INPUT BOARD



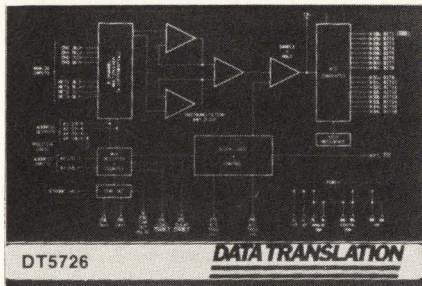
The MPV950 is a VMEbus compatible 16-channel analog input system which has a total throughput time of 3μsec per channel. The board has 12-bit resolution and 16 single-ended inputs. The series uses Burr-Brown's 12-bit ADC803 A/D converter (1.5μsec conversion time) and Burr-Brown's SHC803 sample/hold amplifier (250 nsec acquisition time). The board can convert accurately at speeds beyond the limit of the ADC. To achieve this samples may be skipped to preserve data integrity. **Burr-Brown, Tucson, AZ Write 209**

ERRATA

In the May, 1984 issue of *Digital Design*, there was an error on p.52 of the article, "Modular Architectures May Be The Next Array Processor Design." Star Technologies' ST-100 multiprocessor system that attaches to one or more general purpose computers was incorrectly priced. The correct price is \$250,000.

In the article entitled, "Trends in Flat Information Display Technology," *Digital Design*, May 1984, we inadvertently failed to mention that Dale Electronics (Columbus, NB) is another major manufacturer of segmented and bar graph type plasma display panels. Dale is also developing high information content plasma displays capable of presenting 2,000 characters.

16-BIT A/D MODULE

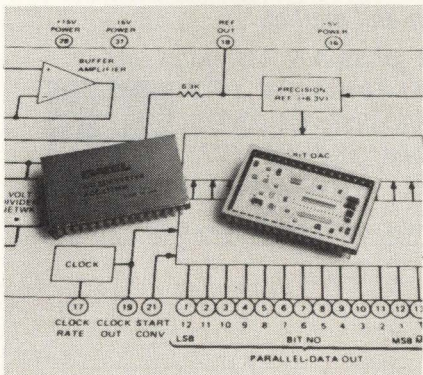


The DT5726 is a 16-bit data acquisition module with 100KHz sampling rate for four differential analog inputs. The DT5726 consists of a four channel differential input multiplexer, an instrumentation amplifier, sample and hold circuitry, fast analog to digital converter, and internal timing and control. Maximum conversion rate is 100,000 samples/sec in the multichannel mode and 111,000 samples/sec in the single channel mode. The DT5726 has a sample and hold aperture delay of 100ns with an aperture uncertainty of ± 0.2 ns. Price is \$1,595. **Data Translation**, Marlboro, MA **Write 199**

MULTIBUS ETHERNET CONTROLLER

The NI3210 is a single board, Multibus Ethernet communications controller. When attached to an Interlan NT10 transceiver the controller provides a link-level connection to Ethernet for Multibus systems. The controller board performs the specified data link and physical channel functions, permitting 10 Mbps data communications between stations separated by 2500 meters. Dual port memory buffers packets between Ethernet and the host Multibus system, allows the host CPU to inspect received packets to determine if they are to go in host system memory. The NI3210 uses linked list buffer management for chaining small buffers together. Price is \$760. **Interlan**, Westford, MA **Write 201**

12-BIT A/D CONVERTER



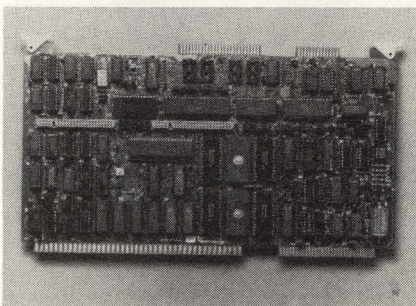
The ADC-811 is a high speed hybrid successive approximation analog to digital converter which converts 12-bits in four msecs. Accuracy specifications of the ADC-811 include a ± 20 ppm/ $^{\circ}$ C maximum gain tempco, ± 5 ppm/ $^{\circ}$ C maximum zero drift and 0.002%/ maximum power supply sensitivity. Differential nonlinearity tempco is ± 2 ppm/ $^{\circ}$ C maximum and power requirements are ± 15 V and $+5$ V. The ADC-811 has four pin-programmable input voltage ranges: 0 to $+10$ V, 0 to $+20$ V, ± 5 V and ± 10 V. A user selectable amplifier is included for applications requiring high input impedance. Price in quantities of 100 is \$152.50-\$234. **Datel**, Mansfield, MA **Write 205**

UNIVERSAL PROGRAMMER



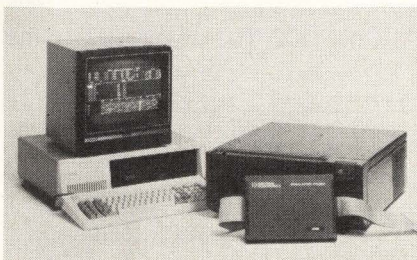
The 29B Universal Programmer has $64K \times 8$ data RAM, which can be expanded to accommodate larger devices. The 29B uses software-controlled modules to adapt it to different programming needs. Optional features include parallel interface logic devices with device handlers. All operations are menu-driven, and program data files can be stored on, altered, and retrieved from the floppy disks. Price is \$3,995 **Data I/O**, Redmond, WA **Write 213**

8086-COMPATIBLE CPU BOARD



The CBC 86C/05 is a CMOS single board computer which is hardware and software compatible with Intel's iSBC 86/05. The Multibus-based board has an 80C86 CPU, of CMOS RAM/ROM mix expandable to 80K, on-board battery backup with memory protect logic and 24 parallel I/O lines. The board includes three counter/timers, RS-232C serial port, and two iSBX-compatible bus interfaces. The board requires 200mA (max.) at 5V operating current. Price is \$1,395. **Diversified Technology**, Ridge-land, MS **Write 202**

EMULATOR PORT FOR IBM PC



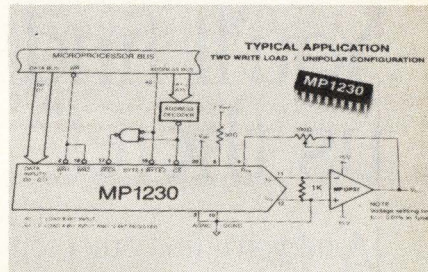
The Kentron PC Interface Package is an emulator port that turns the IBM PC/XT into a universal development system for the design, test, debug and implementation of hardware and software for micro-processor devices. The package consists of hardware and a set of development support software tools, including cross-assembler, linker, emulator software and additional CP/M utilities. For opera-

tion, the KPCI requires an IBM PC/XT with monitor and DOS. A Kontron emulator subsystem and Pascal compilers are optional. Price is \$1,500. **Kontron**, Redwood City, CA **Write 194**

CMOS GATE ARRAY

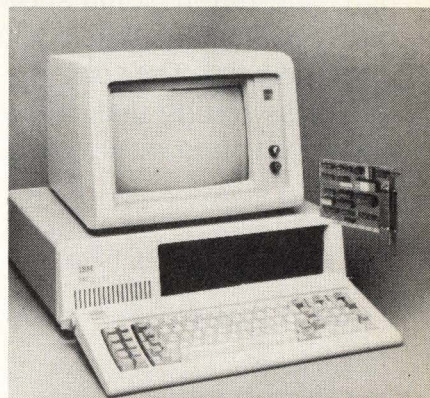
The μ PD65100 is a CMOS gate array comprised of 11,000 gates. Processing speed is two ns per gate. The array has a maximum power dissipation of 20 mw per gate and packaged in 72-, 312-, 176- or 208-pin grid arrays. Price in 5K quantities is \$200. **NEC**, Mountain View, CA **Write 215**

12-BIT DOUBLE BUFFERED DAC



Micro Power Systems have introduced six CMOS μ P compatible, double buffered, 12-bit DACs. The MPS models are MP1208/09/10 and MP1230/31/32. The MP1208 series provides 12 input lines. The MP1230 series provides 12-bit data loading over eight input lines for direct hook up to 8-bit data buses. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM. Features include 12-bit linearity, low bus feed-through, sensitivity to amplifier V_{os} , and low output capacitance. The series is offered in 10, 11 and 12-bit linearity, and in commercial, industrial and military temperature ranges, with 24-pin plastic and 24-pin Cerdip packaging. Price in quantities of 100, is \$13.70-\$48.75. **MicroPower Systems**, Santa Clara, CA **Write 210**

MULTIPLEXER/AMPLIFIER

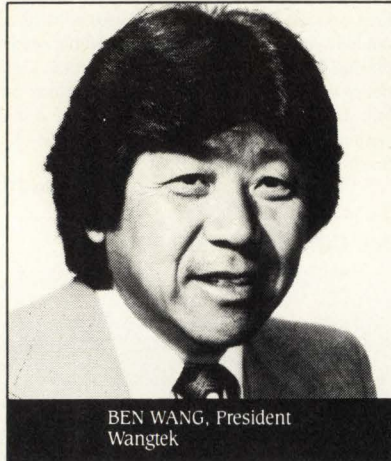


The EXP-16 is an expansion multiplexer/amplifier system that can be used with any data acquisition system. The EXP-16 concentrates 16 differential analog input channels into 1 analog output channel providing signal amplification, filtering and condition. The channel switching is solid state and the channel is selected by a 4-bit TTL/CMOS compatible input address. Provision is made on the board for input shunts, filters and attenuators. All analog input connections are made on miniature screw connector strips. Price is \$345. **MetaByte**, Stoughton, MA **Write 188**

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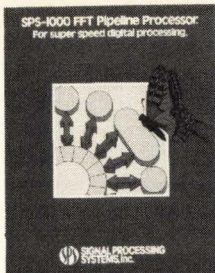
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NEW LITERATURE



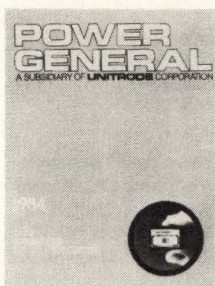
Signal Processor Brochure. This 12-page brochure from Signal Processing Systems describes its SPS-1000 digital processor as well as its operation and architecture. The information will be helpful to users interested in processors for applications such as radar, sonar, time delay measurement, communications, image processing, seismic data processing, and simulation.

Signal Processing Systems Write 263



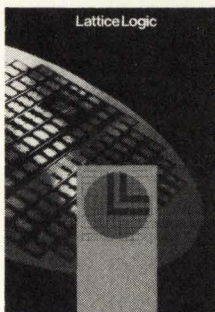
PC Board Equipment Catalog. This six-page catalog of PC board production equipment from Union Tool Corp. includes descriptions of specialized board handling machines. Described are a Dual Station Stacker, Return Conveyors, Vacuum Transfer Machines, a Drop Leaf Stacker and a Staggered PC Feeder. Also included is the company's standard line of board equipment.

Union Tool Corp. Write 261



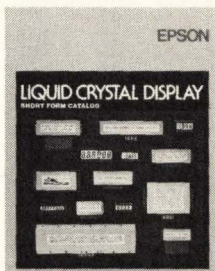
DC-DC Converter Handbook. This 32-page product handbook from Power General provides data on its line of DC-DC converters, including over 35 new products. Power supply characteristics are presented in selection tables followed by engineering data on all models. Also included is a glossary of terminology and tutorial information about DC-DC converter operation.

Power General Write 256



Interpreter Brochure. This six-page brochure from Lattice Logic describes its BASIC Interpreter for the Apollo Domain workstation. The BASIC Interpreter is also available on machines in the DEC VAX range, the IBM 4300, the Perkin-Elmer 3200 and the NS16000 series offering the same syntax, error codes and operating conditions.

Lattice Logic Write 264



Liquid Crystal Display Catalog. This short form catalog from Epson America describes its liquid crystal display products on alphanumeric modules, intelligent alphanumeric modules and display panels. Descriptions include features and specification charts.

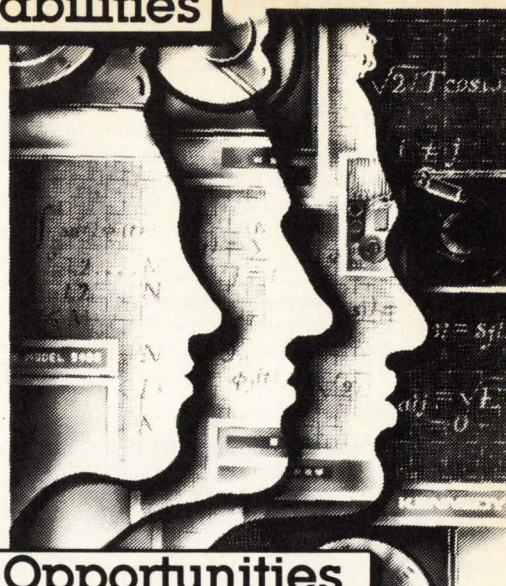
Epson America Write 251



Instrument Catalog. This 176-page catalog from Racal-Dana Instruments describes GPIB instruments, logic analyzers, digital multimeters, AC and RF voltmeters, electronic counters, function, pulse and signal generators, and switching systems. The catalog provides application assistance product specification, ordering information and an overview of its capabilities.

Racal-Dana Write 266

Capabilities



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Electronic Displays '84. Frankfurt/Main, FRG. Contact: Network Events Ltd., Printers Mews, Market Hill Buckingham, MK18 1JX, England. Tele. Buckingham (0280) 815226.

September 5-7

The National Software Show. Anaheim, CA. Contact: Raging Bear Productions, Inc., 21 Tamal Vista Drive, Suite 175, Corte Madera, CA 94925. (415) 924-1194.

September 6

Invitational Computer Conferences. Newton, MA. (Also in Southfield/Detroit, MI, Sept. 25 and Cherry Hill, NJ, Oct. 10.) Contact: Susan Fitzgerald, The Invitational Computer Conference, 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

September 10-13

Defense Computers-Graphics (DCG'84). Washington, D.C. Contact: Defense Computers-Graphics '84, 2033 M St., N.W., Suite 333, Washington, D.C. 20036. (202) 775-9556.

September 10-13

Electronic Imaging. Boston, MA. Contact: Morgan-Grampian Expositions Group, 2 Park Ave., New York, NY 10016-5667. (212) 340-9700.

September 11-12

How to Use dBASE II On Your Personal Computer. Los Angeles, CA. (Also in Phila-

delphia, PA, Sept.18-19.) Contact: American Management Associations, PO Box 319, Saranac Lake, NY 12983. (518) 891-0065.

September 11-14

Data Communications. Washington, D.C. (Also in San Diego, CA, Sept. 25-28.) Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45450, Los Angeles, CA 90045. (213) 417-8888.

September 11-14

Designing Real-Time Systems. Los Angeles, CA. (Also in Washington, D.C., Sept. 25-28.) Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45450, Los Angeles, CA 90045. (213) 417-8888.

September 11-14

Designing Real-Time Hardware for Digital Signal Processing. San Diego, CA. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45450, Los Angeles, CA 90045. (213) 417-8888.

September 16-20

Comcon Fall '84. Arlington, VA. Contact: Comcon Fall 84, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

September 18-21

Computers in Cardiology. Park City, UT. Contact: Computers in Cardiology, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

September 26-28

Eurocon 84, 6th Conference on Electro-

technics: Computers in Communication and Control. Brighton, UK. Contact: Conference Secretariat, IEE, Savoy Place, London WC2R 0BL, United Kingdom. Tele. 01-240-1871, Ext. 337.

October 2-4

Automatic and Test Instrumentation '84. Paris, France. Contact: Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England. Tele. Buckingham (0280) 815226.

October 2-4

Northcon/84. Seattle, WA. Contact: Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045. (213) 772-2965.

October 2-4

Mini/Micro Northwest-84. Seattle, WA. Contact: Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045. (213) 772-2965.

October 2-4

East Coast Computer Faire. Boston, MA. Contact: Computer Faire, Inc., 181 Wells Ave., Newton, MA 02159. (617) 965-8350.

October 2-5

Distributed Processing: Mini and Microcomputer Implementations. Palo Alto, CA. (Also in Boston, MA, Sept. 25-28.) Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45450, Los Angeles, CA 90045. (213) 417-8888.

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