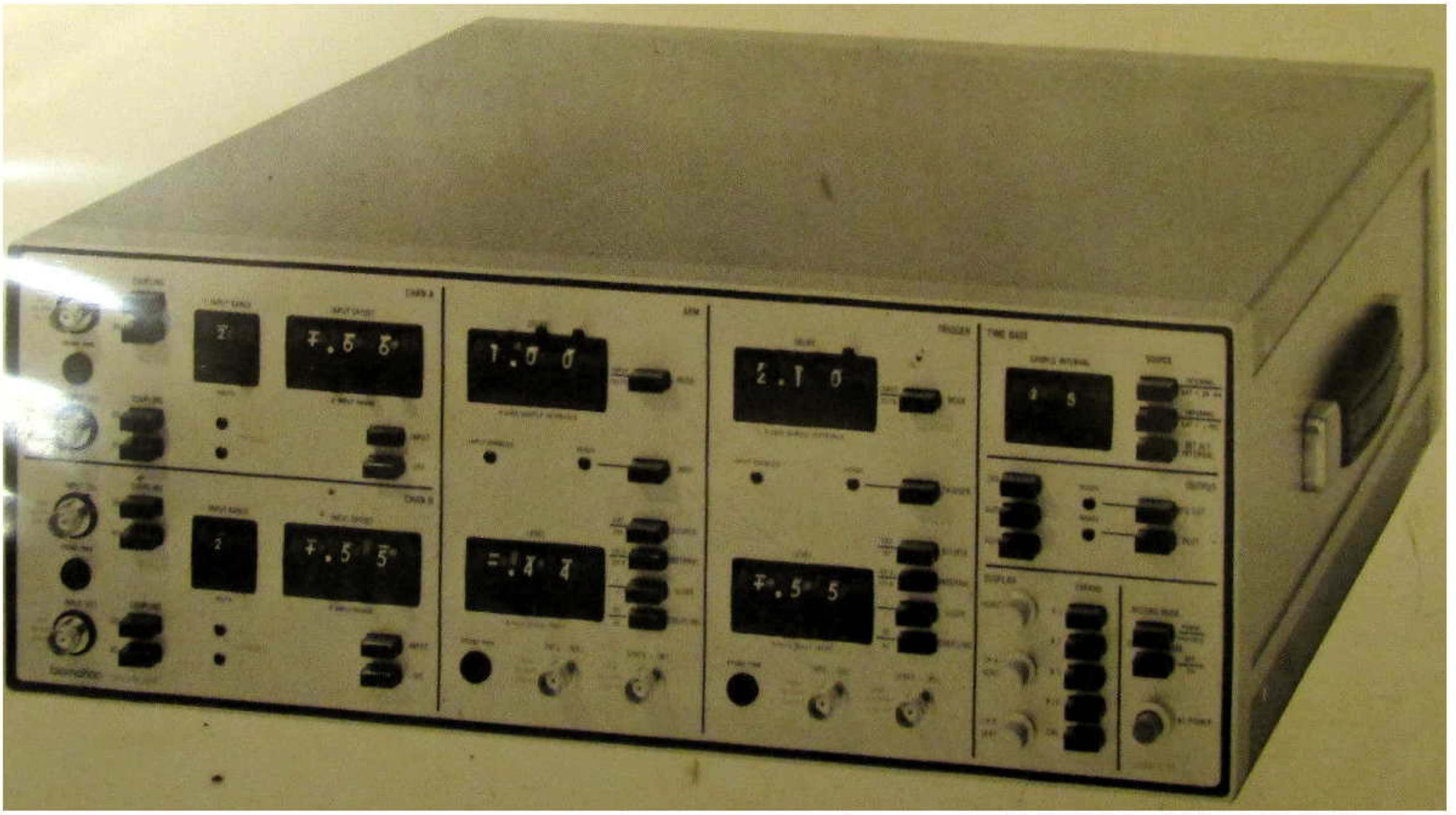
biomation

MODEL 8100
WAVEFORM RECORDER



OPERATING AND SERVICE MANUAL

Part No. 0810-0144

3/1/78

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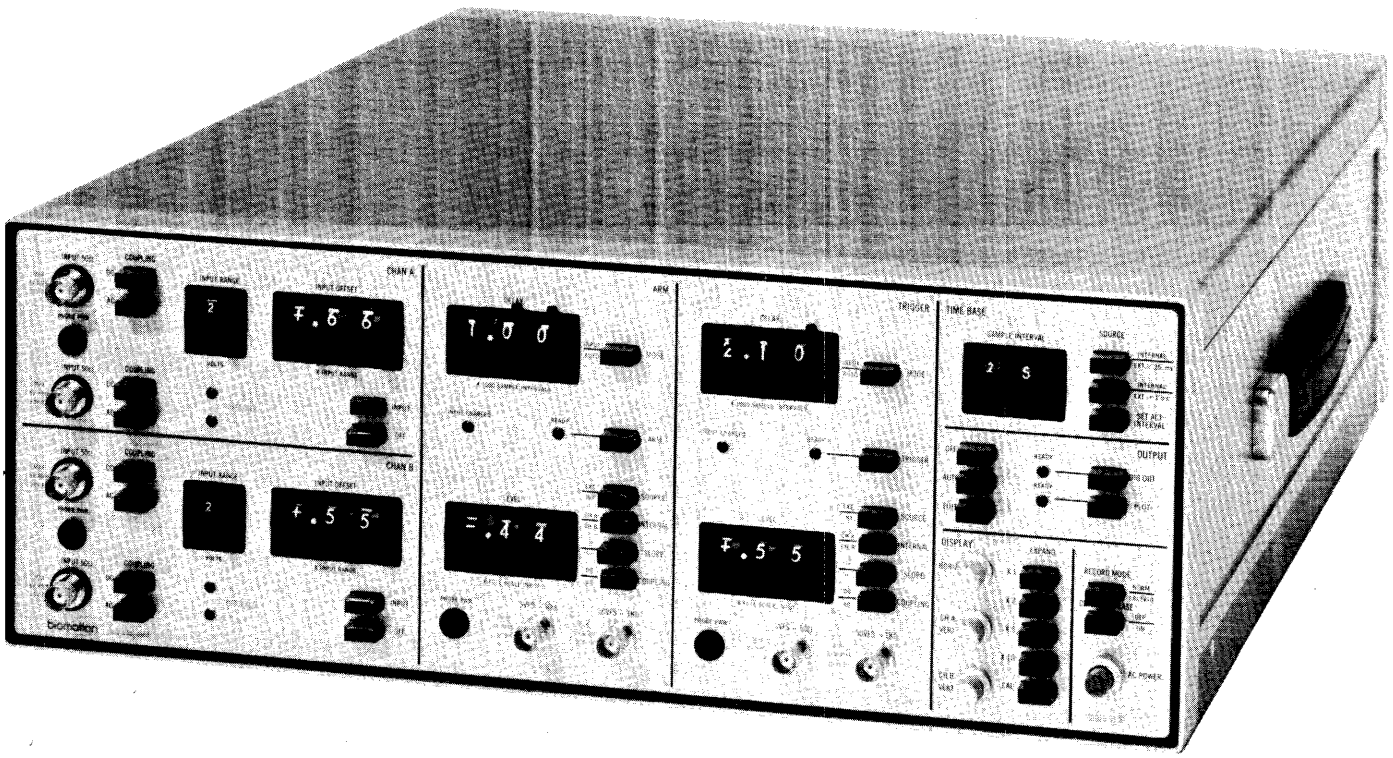

OPERATING AND SERVICE MANUAL

Gould Inc., Biomation Division 4600 Old Ironsides Drive, Santa Clara, CA 95050
(408) 988-6800 TWX: 910-338-0509 Printed in U.S.A.

GOULD

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GOULD

OPERATING & SERVICE MANUAL

MODEL 8100

Table of Contents

SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

The Model 8100 Waveform Recorder is a compact solid state electronic instrument that stores the digital equivalent of electrical waveforms in memory. The outputs of the Model 8100 can be interfaced to display instruments such as oscilloscopes, CRT displays, plotters or strip chart recorders. It can also be interfaced directly to digital computers and is readily interfaced to digital recorders, time share terminals, magnetic tape storage devices, etc., as a part of a data acquisition system.

The Model 8100 is a bench-type instrument with tilt-up stand and may also be rack mounted, occupying a 7-inch vertical space in a standard 19" wide rack. Specifications for the Model 8100 are shown on the following pages.

NOTE: The total record time is given as 2048 times the sample interval and the memory length is stated as 2024 words. This apparent discrepancy is due

to the fact that, although the physical size of the digital memory is 2048 words, only (the first) 2024 words are guaranteed to contain accurate data.

1.4 Specifications

ANALOG INPUT CHARACTERISTICS

Channels. Two independent channels, each differential or single ended. Dual channel operation (inputs sampled alternately) is permissible for sample intervals of 100 nS or greater.

Impedance. 50 Ω each input to ground. Unit will power and accommodate standard FET active probes to achieve 10 MΩ, 10 pf input impedance, with 10:1 voltage division.

Range. ±50 mV to ±5 V full scale (100 mV to 10 V peak to peak). Independent selection on each channel by 7 position (1, 2, 5 sequence) lever switch. Attenuator accuracy ±3% on any position.

Maximum Voltage. 25 V peak, 8 V RMS.

Coupling. AC or DC for each input of each channel. Time constant of 100 μS on AC coupling.

Offset. Zero to ± 0.99 of full scale. Selections in increments of 0.01 of full scale.

Offscale Indicators. ± Offscale indicators to indicate signals beyond range of A/D.

Bandwidth. DC to 25 MHz for DC coupling on all ranges. Low frequency 3 dB cutoff of 1.5 KHz on AC coupling.

Overload Recovery. Less than 10 nS for recovery from 500% (5X) overload. Less than 50 nS for 10X overload. Subject to maximum input voltages above.

Common Mode Rejection. 40 dB from DC to 10 MHz.

DC Stability. Drift, including offset, of less than 5% of full scale over 24 hours.

Gain Stability. Gain changes less than 3% over 24 hours, less than 1% over ten minutes.

ANALOG TO DIGITAL CONVERTER

Resolution. 8 Bits (1 part in 256, or .4%) at all sampling rates.

Effective Aperture Uncertainty. Less than 2 nS.

Bit Rate. 800 Megabits per second at .01 μS sample interval.

TIME BASE AND MEMORY

Sample Interval. **INTERNAL.** Selectable. 01 μS to 10 S, in a 1, 2, 5 sequence with range multipliers of μS, mS, S.
EXTERNAL. Via rear panel BNC connector, TTL level (0 to +5 V), samples on negative going edge. Continously variable intervals between following bands: .02 μS to .25 mS, .25 mS to 1 mS, and greater than 1 mS. Minimum pulse width 10 nS.

Time Base. 100 MHz crystal controlled oscillator.

Memory. 8 bits X 2048 words. First 2024 words specified to contain valid data. In dual channel operation, 1012 words shared per channel. Dynamic MOS shift register.

Total Record Time. 2048 times sample interval. Varies from 20 μS to 20 000 S (5.55 hrs.) when using internal sample interval selection.

ARM AND TRIGGER FUNCTIONS

These specifications apply equally to both functions.

Auto. Function provided automatically at a fixed interval internally.

Input. **MANUAL.** Front panel pushbutton.
INTERNAL. Selectable either Channel.
EXTERNAL. Front panel BNC; 50 Ω, 1 KΩ impedance.

Slope. Selectable positive or negative.

Coupling. Selectable AC or DC. DC only for internal, dual channel.

Level. **INTERNAL.** Adjustable from 0 to ± 0.99 in increments of 0.01 of input range.
EXTERNAL. Adjustable in increments of 0.05 V (50 Ω input) or 0.5 V (1 KΩ input).

Width. Greater than 50 nS.

Amplitude Change. **INTERNAL.** 5% of input range.
EXTERNAL. Greater than 200 mV.

Maximum Input Voltage. **50 Ω INPUT.** 25 V peak, 8V RMS.
1 KΩ INPUT. 100 V peak, 30 V RMS.

Delay. **ADJUSTMENT.** Selectable in increments of 10 sample intervals from 0 to 9990 sample intervals.
STABILITY. ± one sample interval.

Synchronizing Connectors. Rear Panel BNC connectors for event distribution among several 8100s.

RECORD MODES.

Normal. Unit will accept trigger after (delayed) arm. Recording begins at (delayed) trigger. Recording stops after 2048 sample intervals.

Pretrigger. Recording starts with arm signal, and stops with (delayed) trigger signal. Mode provides storage of entire leading edge of a pulse while detecting a trigger from any part of the pulse, allowing user to look back in time.

Dual Time Base. A given record sweep may start at one sample interval and switch to another sample interval during the sweep. Usable in both Normal and Pre-trigger Modes. Not usable when one sample interval is greater than 0.5 mS and the other is less than 0.5 mS; whenever the alternate, or second, sample interval is 0.01 μS.

ANALOG OUTPUT

X Out. Repetitive 1 Vpp ramp, 1 mS period. Origin adjustable between −1 V and + 0.2 V. Sweep expansion selectable X1, X2, X5, X10 (1 V, 2 V, 5 V, 10 V ramp).

Y Out. Repetitive analog reconstruction of data in memory. Full scale amplitude 0.8 V, internally adjustable from 0.5 V to 1.2 V. Origin adjustable ± 1X full scale. Independent position adjustment for channels A and B.

Z Out. Nominal 0 to + 5 V pulse, 24 μS duration. Used for display scope time base trigger, or for CRT display blanking.

$\bar{Z}$ Out. Nominal + 5 to 0 V pulse, 24 μS duration. Used for display scope time base trigger, or for CRT display blanking.

Display Calibrate. Full scale square wave with period of 400 sample intervals. Applied to Y Out BNC connector via front panel pushbutton.

Plot. When in Edit Mode, front panel pushbutton initiates single analog output of memory contents for input to an YT plotter or strip chart recorder. Standard output rate is 10 mS per point (20 S total plot time), 20 mS per point for dual channel output. Optional rates available.

Pen. 1 mS positive TTL pulse coincident with start of plot output. Optionally available as an inverted pulse (TTL level), or as a positive TTL level during entire plot output.

DIGITAL INTERFACE

Control Signals. Command input, Flag output, TTL levels (0 to +5 V). Selectable positive or negative true.

Digital Output. OFF. Digital output not available. Unit automatically reverts to display mode when not recording.

AUTO. Single data output (2048 words) at end of record sweep. Reverts to display output after data output completed.

EDIT. Output mode enabled upon demand.

DATA OUTPUT. 8 bit parallel, TTL levels. No output when not addressed. Selectable positive or negative true. Asynchronous transfer under Flag/Command handshake control. Average data rates continuous from 10 K to 2 M words/sec. Data rates less than 10 K words/sec. exhibit up to 1 mS latency.

Programming. PROGRAMMABILITY. All front panel controls are programmable, except display controls and power switch.

PROGRAM INPUT. 16 bit parallel, TTL levels. Selectable positive or negative true. Three bit address assignment and three bit address field.

MISCELLANEOUS

Size. HEIGHT. 6.25 in (16 cm).

WIDTH. 17 in (43 cm).

DEPTH. 21 in (53 cm), exclusive of front panel controls and connectors.

WEIGHT. Approx. 60 lbs. (27.2 Kg).

Power. Approx. 200 W, 115/230 V RMS, 50-60 Hz.

SECTION II

Installation

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage and installation of the Model 8100.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division representative or Gould Inc., Biomation Division in Santa Clara, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice. A factory approved shipping carton can also be obtained by contacting Biomation.

2.4 Power Connection

Line voltage: the Model 8100 may be operated from either 115 or 230 volt (±10%) power lines. The line cord connector contains a line filter.

The desired line voltage may be selected as follows: disconnect the line cord at the instrument. Using a narrow blade screwdriver, slide the voltage selection switch so that the proper line voltage appears on the switch.

For 115 V operation, use a 3A slow blow fuse. For 230 V operation, use a 1.5A slow blow unit.

> CAUTION: Before plugging instrument into AC power line, be sure line voltage switch is properly positioned.

Power cable: the Model 8100 is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only a 2-blade outlet is available, use a connector adapter, then connect the short wire from the side of the adapter to ground.

2.5 Preparation for Use

The Model 8100 can be operated in a self-contained system by simply connecting it to a CRT display or oscilloscope. Or it can be interfaced with other types of instrumentation for data storage or analysis. The following sections of this manual cover operation, setups and interface requirements.

2.6 Initial Warm-up

Although the Model 8100 is a solid state instrument, a brief warm-up period of approximately 10 minutes is required for the input amplifier and the analog-to-digital converter to reach thermal stabilization.

SECTION III

Principles of Operation

3.1 Introduction

The Model 8100 Waveform Recorder presents new standards of performance for digital data acquisition equipment. The unit is a member of a class of electronic instruments that uses digital techniques to record a defined time segment of an analog signal. Thus, the waveshape, during the selected period of time, is recorded and held in the instrument's memory. The information stored in the memory can be output in any or all of the following three ways:

1. A reconstructed analog signal is available repetitively along with an appropriate sweep ramp and a retrace blanking signal to produce a flicker-free display on a CRT or oscilloscope.

2. The reconstructed analog signal is available at very slow rates for hard copy recording on a strip chart or XT recorder.

3. The signal is available in digital form for input to a digital recorder and/or a digital computer for off-line signal analysis or processing.

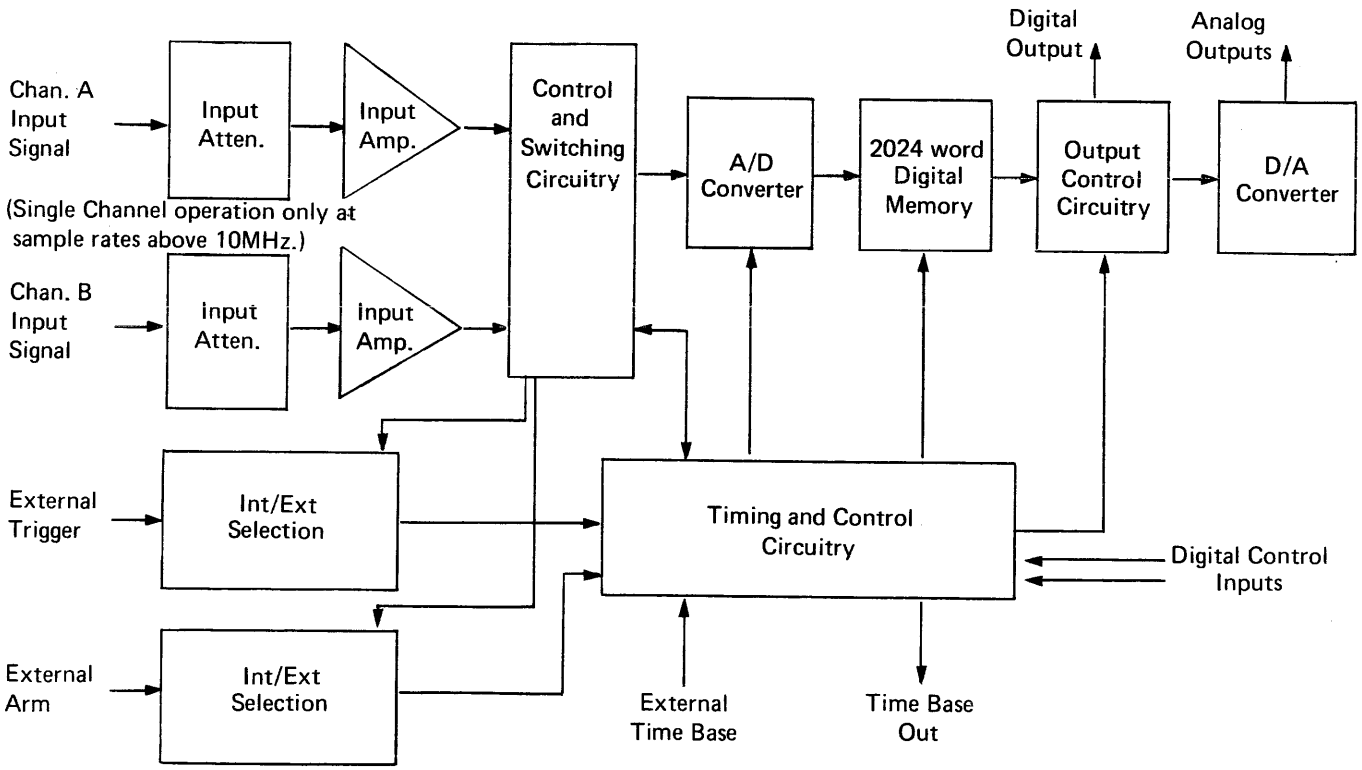


Figure 3.1

3.2 Basic Functional Description

The waveform recorder as an electronic instrument is conceptually quite simple. Its basic form consists of an A/D converter integrally connected with a digital memory, both of which are regulated by common timing and control circuitry. A digital-to-analog converter is also included to produce an analog output in addition to the digital output. Versatile arming, triggering and other user functions are also featured. A simplified block diagram of the Model 8100 is shown in Figure 3.1.

3.2.1 Signal Inputs

Two signal input channels are provided with an input attenuator and amplifier for each channel. Each channel is useable independently and provides a choice of single-ended, inverted, or a balanced input. The two input channels are also useable simultaneously at sample rates up to 10 MHz (100 nsec sample intervals) with half of the memory used for the samples from each input. When both input channels are used, successive samples are taken alternatively by each input channel. This results in an effective sample rate per channel of one-half of the selected sample rate for the unit.

3.2.2 Arm and Trigger Inputs

Signals to provide the Arm and Trigger Functions for the Model 8100 can be independently derived from the input signal from either channel or from external sources. External Arm and Trigger inputs are provided for five volt or fifty volt full-scale signals. Synchronizing connections are also available to permit simultaneous arming and/or triggering of multiple units.

3.2.3 External Time Base Input and Time Base Output

An external time base input is provided to permit the sampling rate to be determined by an external oscillator. The circuitry is arranged such that the sample rate will be at the same rate as the external time base input signal when this input is being used. If a nonlinear external sample rate is used, it must be constrained to <0.25 msec, 0.25 msec to 1.0 msec, or >1.0 msec intervals. Alternatively, the internally derived sampling frequency is provided via an output connector to permit the synchronization of other devices to the sampling frequency in the unit.

3.2.4 Digital Control Inputs

A comprehensive digital control interface is provided that permits remote digital control of all controls and functions of the unit with the exception of the analog output display controls and the on/off power switch. This interface accepts digital instructions as successive 16 bit words, stores each instruction and executes each desired function. Refer to Section 5.5 for a detailed description of the Digital Control Inputs.

3.2.5 Digital Output

The digital output is arranged such that it can be accessed and

controlled in conjunction with the digital control inputs. The operational status of the unit as well as the digital data in the unit's memory can be output under the direction of the digital control inputs. Alternatively, the digital data in the memory can be output directly under the control of simple front panel functions and the device receiving the data. The output data is available for asynchronous transfer under flag/command "handshake" control. IMPORTANT - Once the digital output of the data is initiated, the unit is prohibited from accepting an Arm or Trigger signal. This prevents the stored data from being changed until it has been "dumped". Average data rates are continuous from 1×10^4 to 2×10^6 words/sec. Data rates less than 1×10^4 words/sec will exhibit up to 1.0 msec latency, i.e., if more than 100 usec occurs between data request commands, delays of up to 1.0 msec will occur between output data Flags. When in the digital output mode, further recording is inhibited. Refer to Section V for a detailed description of the digital output functions.

3.2.6 Analog Outputs

A reconstructed analog signal output is provided in two forms. The Y display output presents the reconstructed signal repetitively (approximately once each millisecond) to permit the signal to be continuously displayed without flicker on a cathode-ray-tube display or oscilloscope. The unit also produces a synchronized sweep ramp output (X output) to provide the horizontal deflection signal for the CRT plus a direct (Z output) and inverted ($\bar{Z}$ output) retrace blanking signal for CRT display. The reconstructed analog signal is also available (but not simultaneously) for output to a strip-chart recorder or YT plotter. The standard plot time is 20 sec. No compatible sweep ramp is provided in conjunction with the plot output, but a "pen" signal is produced to facilitate the use of this feature. When two channel operation is used, each channel is displayed on alternate output sweeps and each channel may be plotted separately. As with the digital output, Arm or Trigger signals are prohibited during a Plot output sweep.

3.3 Operational Functions

Operation of the Model 8100 Waveform Recorder resembles in many respects the operation of an oscilloscope. The 8100 does, however, provide greater flexibility, settability and range of control functions than normally found on most oscilloscopes, as well as operational features not possible with an oscilloscope. Anyone familiar with the use of modern laboratory oscilloscopes should be able to efficiently operate the Model 8100 after a relatively short learning period.

The operation of the Model 8100 is basically concerned with the signals or events that determine the initiation and termination of the sampling and recording of the input signal. The following subparagraphs describe the various signals and events and their interrelationships in the functional operation of the unit.

3.3.1 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are often used. The term "sweep" is used to designate the succession of samples taken on the input signal during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the memory with contiguous samples of the input signal. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

3.3.2 Arm, Trigger and End-of-Sweep Functions

The Arm, Trigger and end-of-sweep functions, together with two adjustable delays (associated with the Arm and Trigger events) control the sequence-of-events in the operation of the record cycle of the Model 8100. The effect of each of these functions or events on the sequence-of-events is dependent upon the operational configuration or mode of operation selected for the unit. This interdependence will be described in a later paragraph.

The Arm function could also be termed "trigger #1" or trigger reset. Detection of an event to "Arm" the unit has all of the flexibility of the Trigger function, i.e., it can be derived internally from the input signal of either channel or from a separate external input. The detection threshold is adjustable over the entire input signal range and can be selected for positive or negative signal transitions, and the detection level can be based on the dc value of signal or the relative value by removal of the dc component. In addition, all of these criteria for the Arm function can be bypassed by selection of the Auto Arm function which provides an automatic Arm event for each successive record sequence. The essential thing to remember is that the Arm and its attendant delay function must occur prior to the Trigger event, or succinctly: no Arm -- no Trigger!

The Delayed Arm function is self explanatory. The amount of delay is adjustable from 10 sample intervals minimum (see p 65B) up to five times the sweep time.

The Trigger function could also be called "Trigger #2," and detection of the event to provide this function has all of the flexibility of the Arm function described above including an Auto Trigger function for the trigger event for each successive record sequence.

Similarly, the Delayed Trigger Function is available and is adjustable from 10 sample intervals minimum (see p 65B) up to five times the sweep time.

The end-of-sweep function, or the EOS function as it is sometimes abbreviated, occurs 2048 sample intervals after recording commences.

3.3.3 Modes of Operation

The operational modes for the record sequence in the Model

8100 are determined by the record mode selected and the choice of the Single or Dual Time Base function. Two basic record modes are provided. They are called Normal mode and Pretrigger mode. The time base function selection and the record mode selection provide four basic record configurations under the control of the Arm, Trigger and EOS events described in the preceding paragraphs. These four record configurations are illustrated graphically in Figure 3.2.

3.3.3.1 Normal Record Mode, Single Time Base

In the normal record mode with the dual time base turned off (single time base), the record cycle is initiated by the Delayed Trigger, and it is ended at the end-of-sweep (EOS). This operation configuration can be used in various ways depending on the setting of the Arm and Trigger delays. With both delays set to zero, a straight-forward Normal sweep mode is produced.

If the Arm Delay is set for a significant delay time, a mode of operation sometimes referred to as "trigger holdoff" is produced. Trigger hold-off is useful to examine a relatively short-lived signal that occurs at low repetition rates. If the signal is such that the only signal (or trigger) perturbations are those which are the object of investigation, then there is no problem. However, it often occurs that the signal under investigation is accompanied with unwanted perturbations which are capable of triggering the unit. The Arm Delay can be used in such cases to "holdoff" the acceptance of a trigger until the unwanted perturbations have passed. In this way the desired information in the memory will not be disturbed.

The Normal sweep mode can also be configured for "delayed sweep" operation by setting the trigger delay to a significant value. The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the trigger and the desired information is greater than the optimum sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the Trigger Delay and sampling the signal at a faster rate, the information can be recorded with good resolution.

3.3.3.2 Pretrigger Mode, Single Time Base

Pretrigger recording is a unique feature of Biomation Waveform Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good trigger available follows the information of interest.

In the normal recording modes the memory is filled with new information when the trigger occurs, or later. In the pretrigger recording mode of operation the memory is continuously being updated after the unit has been "Armed," and will discard information (from the "other end" of the memory) at the same rate. When the trigger occurs, the recording function ceases after the selected Trigger Delay time. If the Trigger Delay is zero, the memory will contain the information for the signal which occurred for one complete sweep time

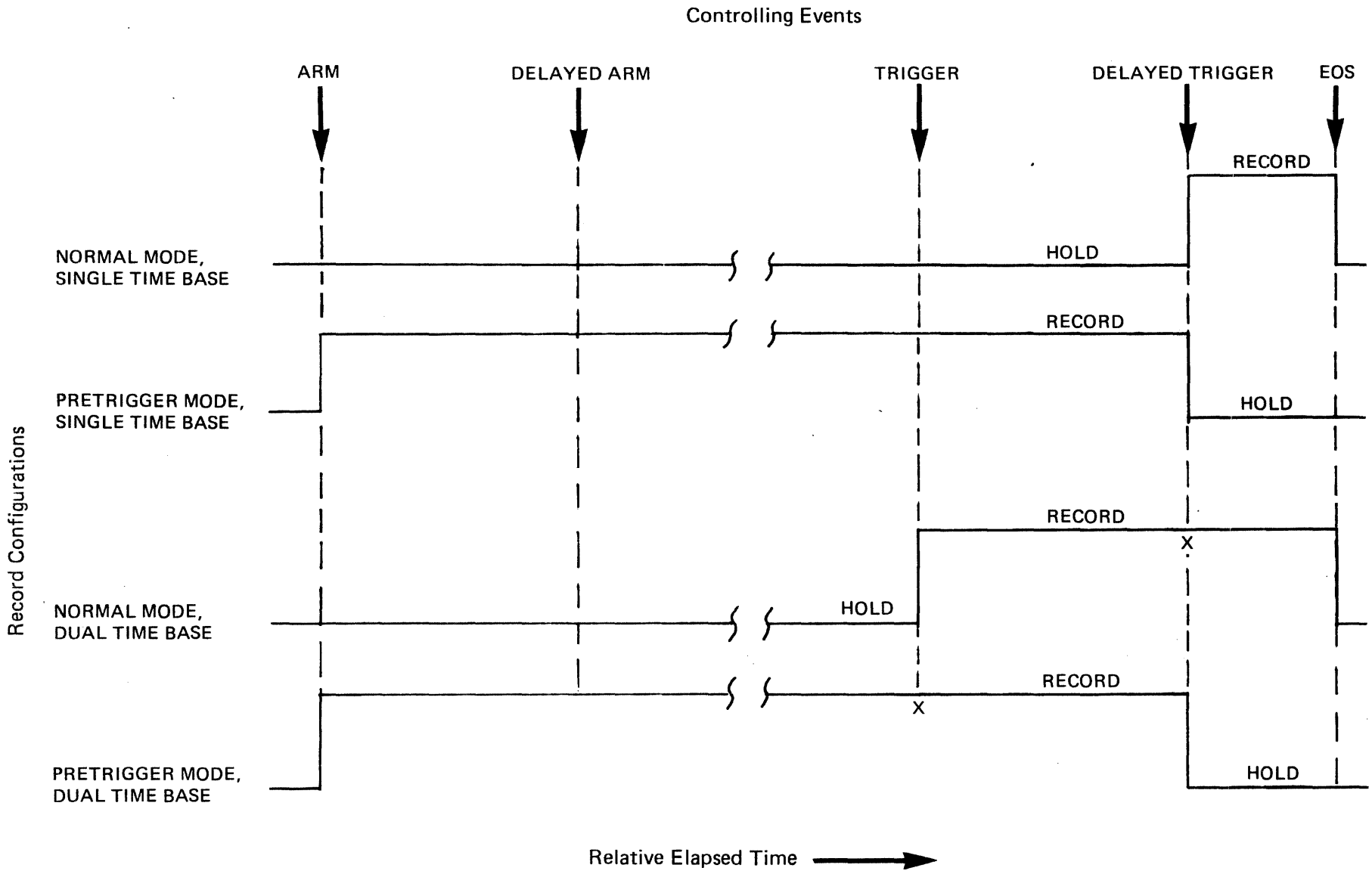


Figure 3.2 Model 8100 Record Modes

prior to the trigger. The delay set on the Trigger Delay in this mode will determine which portion of the signal in the memory occurred after the trigger. Thus, any portion of the sweep time can be set to occur before or after the trigger event in the Pretrigger record mode of operation by simply adjusting the Trigger Delay setting. In this mode, the Arm Delay determines what portion of the memory will be filled before allowing a Trigger. If the sum of the Arm Delay and Trigger Delay is set to a total of 2000 sample intervals or more, one can be sure that the entire memory will be filled with useful data during each measurement cycle.

3.3.3.3 Dual Time Base Operation

The dual time base operation of the Model 8100 permits the recording to begin at one sweep rate and conclude with a different sweep rate, i.e., sampling of the input signal in the dual time base rate and switches to sample intervals at another linear rate for the conclusion of the recording period. The point at which the switching occurs is dependent upon the front panel control settings and the record mode selected as described in the succeeding paragraphs. The Dual Time Base operation is useable for most combinations of sample intervals for each portion of the record sequence with the following exceptions:

1. The Dual Time Base function is not useable when one sample interval is less than 0.5 msec and the other sample interval is greater than 0.5 msec.

2. The Dual Time Base function is not useable when the second sample interval (alternate time base) is 0.01 usec, i.e., if the alternate time base is set for a sample interval of 0.01 usec, Dual Time Base operation is not specified to provide accurate sampling and storage of the input signal.

3.3.3.4 Normal Sweep Mode, Dual Time Base

This mode of recording permits the recording of an input signal with portions of the signal recorded at two independent rates. This is particularly useful in studying waveforms which contain fast and slow components. The point at which the record rate switches from the first sweep rate to the next is determined by the setting of the Trigger Delay. Thus, recording is initiated by the Trigger, the rate is changed by the Delayed Trigger, and the recording is terminated by the EOS. "Trigger holdoff" operation is available in this mode through use of the Arm Delay as described above, but delayed sweep cannot be accommodated because the Trigger Delay is used for the record rate switching.

3.3.3.5 Pretrigger Mode, Dual Time Base

This mode is essentially the same as the Pretrigger Record mode described above with the addition of the switching of the record rate by the Trigger. This mode is very convenient for recording at a slow rate a long period of time (but relatively few samples) prior to a

trigger event, and then recording at a rapid rate (good time resolution) the signal occurring after the trigger event.

3.4 Data Acquisition Limitations

The Model 8100 is basically an all-digital instrument. The user should not overlook this fact because, by its very nature, the digital approach to signal storage has certain limitations. There are some conditions under which these limitations can seriously affect the quality of the information stored. This section will deal with these limitations.

3.4.1 Sampling Rate

The sampling theorum states that the sampling rate must be at least twice the highest input frequency to be measured. In practical situations any complex waveform, such as a sine wave, should have at least five data points throughout the full cycle in order to adequately display the signal details. The sampling limitation can easily be demonstrated by taking a high frequency continuous signal, such as a sine wave, and operating the Model 8100 through all of its available sweep speeds. It will be observed that at slow sweep speeds a very respectable signal can be obtained which bears a little or no relationship to the input signal. This limitation can be avoided by the use of the proper sweep time or with an external low pass filter to attenuate the frequencies above the band of interest.

3.4.2 Output Smoothing

The digital information coming out of the Model 8100 memory goes through a smoothing digital-to-analog converter. This converter makes the output appear to be a somewhat continuous trace rather than a series of points normally expected from a digital instrument. The most important thing to remember is that the digital information contained in the memory may indicate a faster risetime than the visual presentation because of the smoothing circuit employed in obtaining the visual presentation.

3.4.3 Amplitude Resolution

The Model 8100 converts all analog input signals to an accuracy of 8 binary bits. This means that the resolution can be no better than 1 part in 256, or 0.4% of the full scale amplitude. Note that resolution does not imply an accuracy specification. Resolution is 0.4%; accuracy depends on resolution, drift, gain tolerance, signal slew rate vs A/D aperture, and amplifier bandwidth, among other things.

SECTION IV

Operation

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, setup procedures prior to using the Model 8100, and step by step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.2.1 Control Clusters

The controls of the Model 8100 are divided into eight groups called "control clusters." The groups contain separate controls with related functions. For convenience, they are presented together with a photograph of the front panel in Figure 4.1. The eight control clusters are as follows:

Channel A Input	Time Base
Channel B Input	Output Modes
Arm	Display
Trigger	Record Modes

4.2.2 Digital Switches

Advantage has been gained through the digital nature of the unit by permitting the extensive use of digital control switches in lieu of the more common analog "knob". This facilitates the readability and more importantly,the repeatability of the control settings. Use of this type of controls by the uninitiated does require some familiarization.

Two types of digital switches are used on the Model 8100. One is a novel multiposition switch resembling a common "Thumbwheel" switch, but utilizing a convenient "lever" to set the desired position. The other type used is a two-position pushbutton, also called a latching pushbutton switch. The control functions are given adjacent to each of these pushbuttons as a dual legend separated by a line. The upper legend designates the function selected when the pushbutton is out (unlatched) and the lower (bottom) legend is for the function selected with the pushbutton in (latched). In other words, Upper function: push button out; Lower function: push button in.

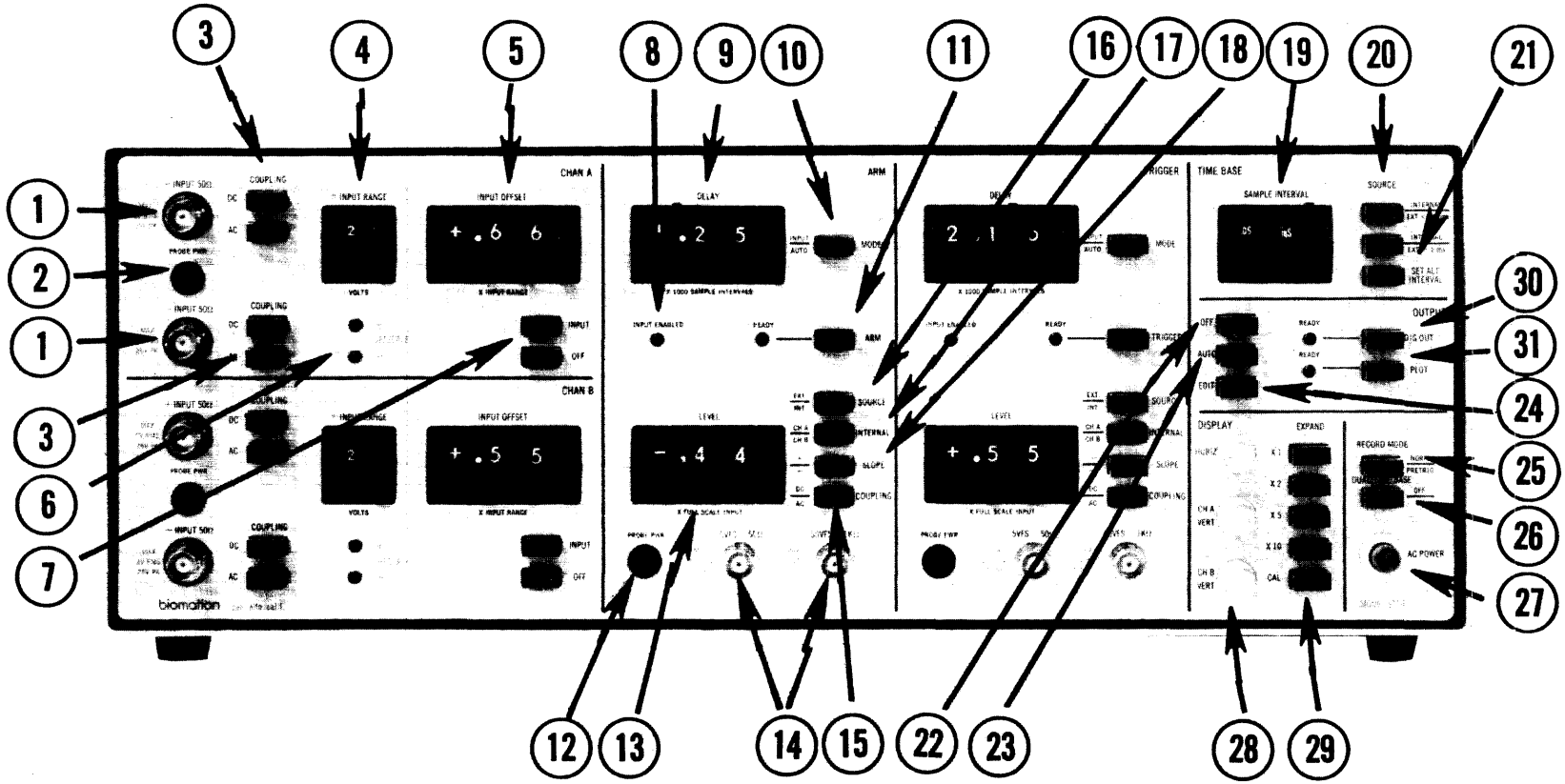


Figure 4.1 Front Panel Functions

4.2.3 Channel A Input Controls*

Signal Input Connectors (1)

Impedance 50 ohms to ground. Two BNC type connectors are used for the positive and negative voltage input.

Probe Power Output (2)

Provides 30 ma of +15 V and -12.6 V to power active FET probes such as the hp 1124A which gives input impedances of 10 megohm, 10 pf.

Coupling (3)

Four pushbutton switches marked either dc or ac are associated with the two input connectors. If all four pushbuttons are not depressed, neither input is connected. If one pushbutton is depressed, single ended or inverted input will result with the indicated coupling, and if a pushbutton associated with each connector is depressed, a balanced input results.

Input Range (4)

Full scale voltage ranges from ±0.05 V to ±5 V are selected by the digital lever switch. A 1-2-5 sequence gives plus and minus 0.05, 0.1, 0.5, 1, 2, and 5 volts full scale.

Input Offset (5)

Level compensation from 0 to ±0.99 times the input range is available. By offsetting a unipolar signal to center it around zero, the maximum possible resolution may be obtained.

*Note: These identical functions and controls are provided for Input Channel B.

Offscale Indicator (6)

These indicators light if the input signal exceeds 100% of the input range at any time during the recording period. The indication is reset when the unit is Armed for the next recording cycle.

Input/Off (7)

These buttons connect or disconnect the input amplifier to the measurement circuitry. They also control the output sweep information in dual channel operation.

4.2.4 Arm Controls

Input Enabled Indicator (8)

Lights when "INPUT" (10) is selected - see below. This indicates that an Arm signal must be provided for each complete record cycle.

Delay (9)

Determines the time between detection of the arming signal and the arming of the unit. Digital lever-switches provide delays from 0 to 9990 sample intervals selectable in intervals of 10 samples. A 10 sample interval delay exists between receipt of the Arm signal and when the unit will accept a trigger, and between the Trigger and start of recording. See p 65B.

Mode (10)

Selects "INPUT" or "AUTO" mode of operation. In INPUT mode, the ARM command is derived manually by push button, internally from the signal, or from an external pulse. In AUTO mode the unit Arms itself without waiting for a selected event. AUTO mode must be initiated by depressing the Arm push button.

Arm Pushbutton and Ready Light (11)

The Arm pushbutton is used to manually Arm the unit and to initiate the Auto-arm function. When the unit is ready to be Armed (i.e., is unarmed), the Ready Light is on. The Ready Light will also be extinguished by the timely occurrance of an internal or external Arm signal.

Probe Power Output (12)

Provides the same voltages as connector (2) above. This permits an FET active probe to be used on the 50 ohm Arm input (14).

Level (13)

Determines the level at which the unit Arms. The digital lever-switch is adjustable from 0 to ±0.99 in increments of 0.01 of the Input Range for internal mode. For external Arm signals the 0.01 increments are the equivalent of 0.05 V on the 50 ohm input, or 0.5 V on the 1 K ohm input.

Arm Signal Input Connectors (14)

Two BNC connectors are provided for the input of Arm signals from external sources. (The Arm signal enables the unit to recognize a trigger. See section 3.32.) The level control (13) determines the "Arming" level with respect to the appropriate full scale input voltage:

5 V full scale - 50 ohms input impedance.

50 V full scale - 1000 ohms impedance.

Power for an active probe to be used with the 50 ohm input is provided (12).

Coupling (15)

A pushbutton that selects ac or dc coupling for the Arm circuitry. The coupling is to either Internal or External sources, as selected by the Source switch (16). Use is limited to dc only when Internal is selected and two channel operation is used.

Source (16)

Selects the source of the arming command. EXT (switch 16 out) selects Arm signals from the two BNC connectors (14). INT (switch 16 in) causes the unit to Arm when the input signal itself crosses the selected level (13) at the selected slope (18).

Internal (17)

This pushbutton selects whether the Arm signal is derived from Channel A or Channel B when the Source button is set to INT. Arm signals from Channel A are used when the pushbutton is out, and from Channel B when the pushbutton is in.

Slope (18)

Selects positive or negative slope for the Arm signal whether derived from Internal or External signals. Positive slope is required when the pushbutton is out (+), negative when the button is in (-).

4.2.5 Trigger Controls

These controls cause the unit to begin or end a measurement sweep as described in section 3.32. They are identical to the Arm controls described in 4.23, except that the controls all apply to Trigger instead of Arm.

4.2.6 Time Base Controls

Sample Interval (19)

Digital lever-switches select the recording sample interval (linear record rate) of the internal time base. Intervals from 0.01 microsecond to 10 seconds are selectable with intervals of 0.01, 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10 µsec, msec, or seconds.

Source Internal/External (20)

Two bushbutton switches select the internal time base or permit an external clock signal to control the sample rate. With both buttons out, the internal source is selected. Pushing in the upper button permits clock pulses to be input with intervals from 20 ns to 0.25 ms per pulse. Pushing in the lower button (with the upper button out) permits clock pulses to be input with intervals of 1 ms per pulse or slower. Depressing both buttons permits external sampling pulses with intervals between 1 ms and 0.25 ms to be input.

Set Alternate Interval (21)

When used in the Dual Time Base mode (see section 3.33), this button is used to enter the alternate time base. In this mode the unit switches to an alternate (second) sample interval at a point controlled by the trigger delay setting. To select the alternate sample interval, set the SAMPLE INTERVAL switch to the second interval and momentarily depress the SET ALT INTERVAL button (21). This "stores" the information in internal registers. Change the SAMPLE INTERVAL switch to the desired first interval, and the two time bases are selected. CAUTION: The "stored" sample interval will be lost "erased" on loss of line power and will be indeterminate until reset.

4.2.7 Output Controls

These pushbuttons control the digital and plotter outputs of the Model 8100.

Output Off (22)

With OFF depressed, the unit automatically switches to Display mode at the end

of the record period. No digital data is output and no plot output is possible.

Automatic Output (23)

With AUTO depressed the unit automatically switches to the OUTPUT mode after the record sweep. Display is inhibited until the data has been clocked out of the 8100. Record is also prohibited until the data has been clocked out (2048 words) or until the output is switched OFF. After output, the Display mode will return and no further digital output can occur until after a subsequent record cycle.

Edit (24)

The EDIT mode permits the user to see the display before initiating digital output or a plot output sweep. The unit remains in Display until output is initiated by pushing the DIG OUT button (30) (or through the digital interface - see section V) to initiate the digital output, or the PLOT button (31) to initiate the plot output. In EDIT, the digital output or the plot sweep may be repeated on demand as many times as desired.

Digital Output Initiate (30)

The DIG OUT pushbutton manually initiates the output of digital information in EDIT mode. The Ready light indicates that the record sweep is complete and the digital information is ready to be output.

Plot (31)

This button causes the analog output to a plotter to be initiated in EDIT mode. During output the analog level being output is displayed on the screen. After a two channel record cycle, plots of the data from each channel can be selectively plotted by selecting the "input" selector (7) for the desired output channel and deselecting the unwanted channel by placing its Input (7) OFF.

4.2.8 Display Controls

Position Controls (28)

Control the position of the display output on the CRT face. The HORIZ and EXPAND are functional only when using the X output for the display sweep. Separate vertical position adjustments CH A VERT and CH B VERT are provided for two-channel operation.

Sweep Expand (29)

The Expand buttons enable the horizontal resolution of the display to be increased. In X1 the full 2000 points are displayed. By use of the X2, X5 and X10 buttons, protions of the recorded information may be "enlarged" to give a more detailed picture. For example, in the X10 position only 200 points are displayed along the X-axis. The HORIZ Control (28) enables the 200 points displayed to be selected anywhere on the recorded waveshape.

Calibrate (29)

The CAL button causes a full scale square wave with a period of 400 samples to be displayed for calibration and positioning on the scope face. It does <u>not</u> imply a calibrated input injected into the input.

4.2.9 Record Mode Controls

Normal/Pretrigger Mode (25)

Selects the mode of recording used (see section 3.33). With the pushbutton in, "Pretrigger" recording is selected. With it out, "Normal" recording will occur (see section 3.3).

Dual Time Base On/Off (26)

Selects the Switched Time Base mode of operation (see section 3.3).

4.2.10 AC Power Switch (27)

An illuminated switch indicates ac power on.

4.3 Rear Panel Controls and Connectors

Figure 4.2 shows the rear panel connections.

4.3.1 Display Outputs

X OUT (2)

A +1 V peak ramp of 1 ms duration is provided for sweeping X-Y CRT displays. The origin is adjustable between -1 V and +0.2 V. The Sweep Expand buttons (#29 in Fig. 4.1) increase the ramp amplitude proportionately (2 V for X2, 5 V for X5, etc.).

Y OUT (3)

The analog representation of the stored signal is produced here for use with an X-Y display. Signal is .8 V full scale with origin adjustable ± 1.0 V dc and amplitude (internally) adjustable from .5 V to 1.2 V.

4.3.2 Blanking Voltages

Z OUT (5) and $\overline{Z}$ OUT (6)

Provide signals for retrace blanking or oscilloscope trigger. $\overline{Z}$ OUT is a TTL voltage level from 0 to +5 V (nominal) at the start of the display period. It stays positive for 2000 words (1ms) and returns to 0 V for 24 µs during retrace. Z Out is held at 0 V during display and goes to +5 V during retrace.

4.3.3 Plot Output (4)

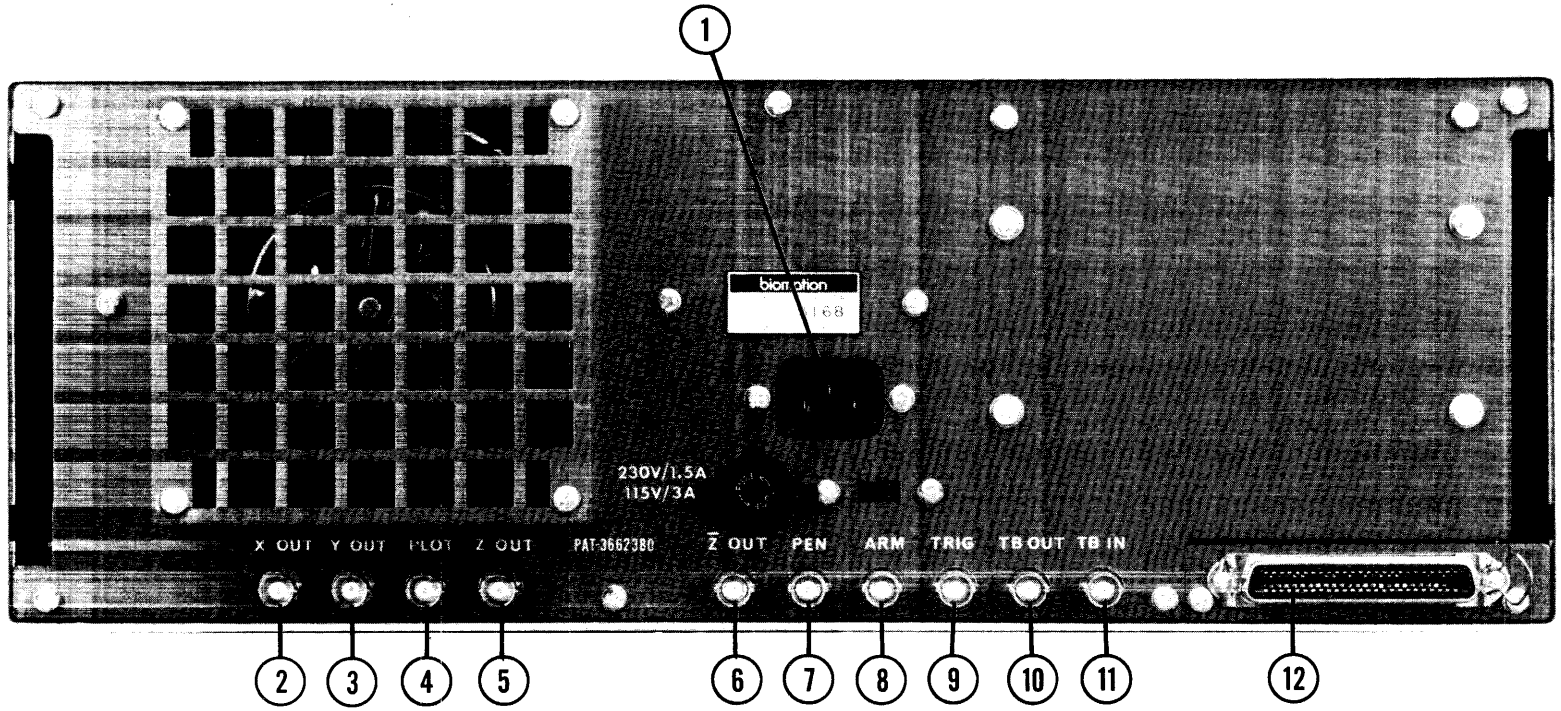


Figure 4.2 Rear Panel Functions

Analog output to drive a strip chart or YT recorder is provided when the front panel PLOT pushbutton is pushed. The standard plot sweep time is 20 seconds, optionally to 200 seconds.

Pen (7)

A 1 ms positive TTL pulse (+3 V) is provided at the start of the Plot Output period for pen or plotter control. Optionally available as a negative going pulse from +5 volts or a positive level during the entire plot sweep or a positive level whenever not in plot output.

4.3.4 Synchronizing Connections

Multiple 8100 units may share the same Arm and Trigger commands. The ARM (8) and/or TRIGGER (9) connectors of the units can be interconnected. For this operation the one unit is set to trigger as desired. The other units have the Arm and/or Trigger SOURCE set to EXT, and the Arm and/or Trigger LEVEL set to about +0.5 to avoid possible noise trigger. The end of the interconnecting cable/s should use 50Ω terminations.

NOTE: These are not inputs for external arm and trigger commands.

4.3.5 Time Base

The time base selected by the front panel SAMPLE INTERVAL switch is available at TB OUT (10). This may be used to synchronize an experiment to the 8100 or as an external time base source for a second 8100. In that application it is connected to the TB IN connector (11) of the second unit. When an external time base is selected by the Time Base Source buttons (#20 in Fig. 4.1), it is supplied to the TB IN connector (11).

4.3.6 AC Line Connector, Fuse holder, and Line Voltage Selector (1).

The connector housing contains a line filter. Note the fuse ratings printed on the

rear panel. When changing line voltage, ensure that the proper fuse is used. The line voltage selector may be changed using a small screwdriver. Leave line cord unplugged while changing fuse and selector.

4.4 Set Up Procedure

4.4.1 Initial Set Up

This section describes the connection of a Model 8100 with a CRT display or oscilloscope and the steps to record and display a known signal.

Before connecting the unit to line power, check the voltage selector switch on the rear panel to ensure that it is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 8100 to a function generator and CRT display as shown in Figure 4.3a or 4.3b. It may be necessary to use the $\overline{Z}$ output of the 8100 for the retrace blanking signal as CRT drive circuitry varies greatly in the polarity of this input. NOTE - connection of the retrace blanking signal is optional when using the triggered horizontal sweep of an oscilloscope as in Figure 4.3a. If the retrace blanking signal is not used, a slightly displaced (in the X direction) "double" signal may be observed whenever the Model 8100 is repetitively triggered in rapid succession. CAUTION - Some older "tube type" oscilloscopes have a high voltage on their $\overline{Z}$ axis inputs. THIS COULD DAMAGE THE MODEL 8100's Z or $\overline{Z}$ OUTPUT.

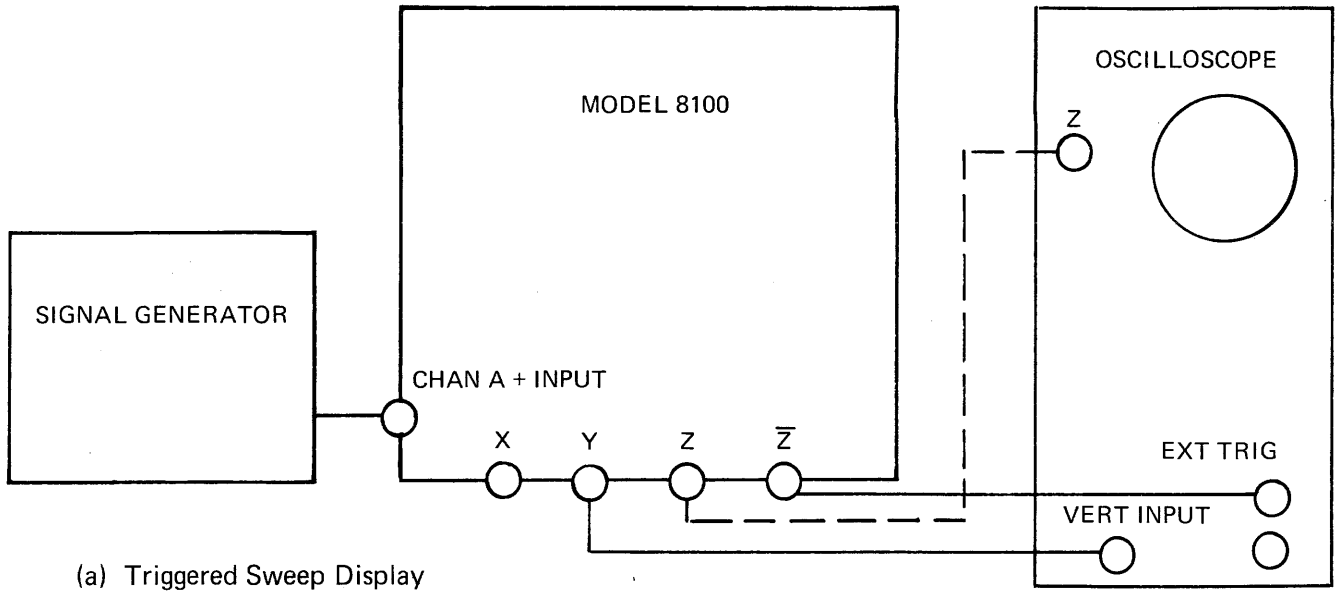
Set the oscilloscope and function generator as follows:

Vertical sensitivity	0.1 V/div., dc coupled
Vertical position	Middle of display
Horizontal sweep	0.1 ms/div. (Fig. 4.3a)
Horizontal sensitivity	0.1 V/div., dc coupled (Fig. 4.3b)
Trigger input	+, dc coupled, External (Fig. 4.3a)
Function Generator	5 KHz, 2 volts peak-to-peak

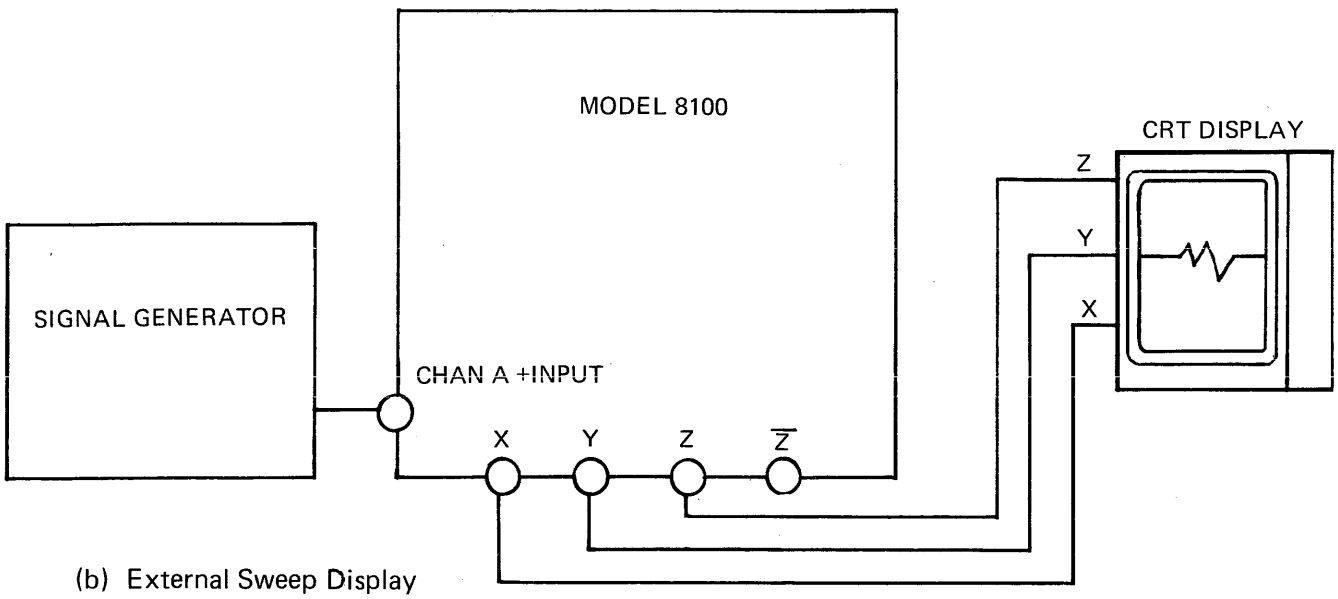
Set the Model 8100 as follows:

CHAN A

SIGNAL INPUT	+INPUT 50Ω
COUPLING	DC (in)
±INPUT RANGE	1V
INPUT OFFSET	0.00
INPUT/OFF	INPUT (upper switch in)



(a) Triggered Sweep Display



(b) External Sweep Display

Figure 4.3 Display Interconnections

CHAN B

INPUT/OFF	OFF (lower switch in)

Other CHAN B settings are arbitrary since the channel is off.

ARM

DELAY	0.00
MODE	AUTO (in)
ARM	Momentarily depress to initiate Auto operation

All other ARM settings are arbitrary since arming is now automatic.

TRIGGER

DELAY	0.00
MODE	INPUT (out)
SOURCE	INT (in)
INTERNAL	CH A (out)
SLOPE	+ (out)
COUPLING	dc (out)
LEVEL	+0.10

TIME BASE

SAMPLE INTERVAL	0.2 μs
SOURCE	INTERNAL (both switches out)

OUTPUT	OFF (in)
DISPLAY	X1

RECORD MODE

NORM/PRETRIG	NORM (out)
DUAL TIME BASE	OFF (out)

Depress the CAL button.

Adjust the HORIZ and CH A VERT and/or the scope display position controls to center the full scale square wave.

Release the CAL button. Two complete periods of the 5 KHz input signal should be displayed on the CRT. If the signal is not full scale (same amplitude as the CAL square wave), see Section VI on Calibration and Maintenance Procedures.

4.5 Operating Procedures

In this section several modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command and able to drive a 50 ohm load is required.

Set the generator to give repetitive pulses 100 µs wide, going from 0 V to slightly over +1 V and occurring at a 2 KHz rate.

4.5.1 Normal Mode

Set the Model 8100 and oscilloscope exactly as described in Section 4.41 above. The + OFFSCALE lamp will be lit. Reduce the amplitude of the input pulse to just under +1 V. The + OFFSCALE light should go out and the display should resemble Fig. 4.4.

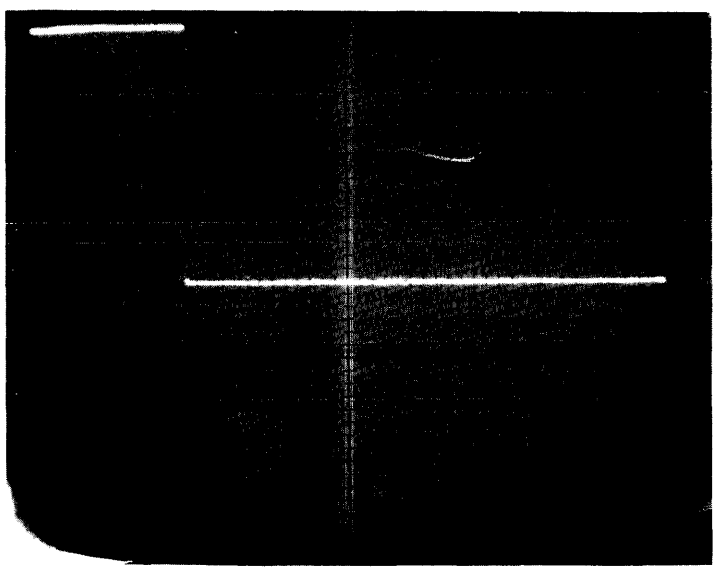


Figure 4.4 Zero Centered Measurement Signal

Change the INPUT RANGE to 0.5 V and the INPUT OFFSET to -0.99. The display should now resemble Figure 4.5.

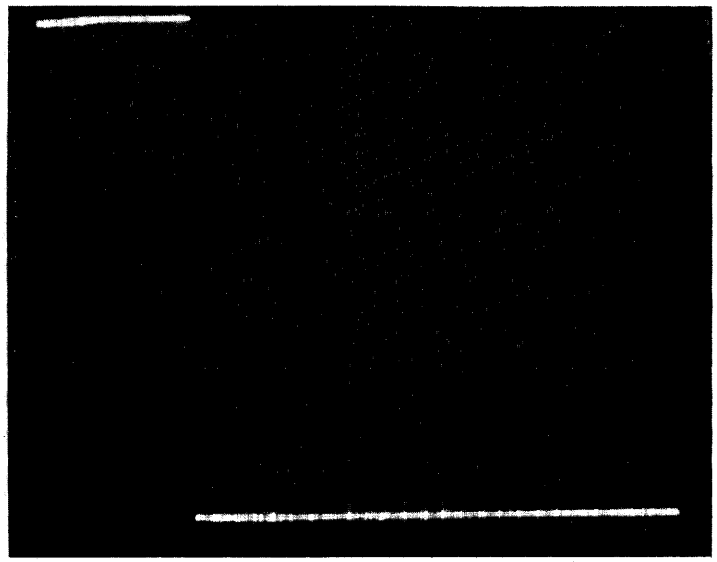


Figure 4.5 Offset Measurement Signal

4.5.2 Pretrigger Mode

Make the following setting changes in the controls:

ARM

DELAY	1.00
MODE	INPUT (out)
SOURCE	EXT (out)

TRIGGER

DELAY	1.10
RECORD MODE	PRETRIG (in)

Press the TRIGGER push button then press the ARM push-button. The display should resemble Fig. 4.6. The pulse will be in the center of the screen. 1100 readings were taken after the trigger, and about 900 were retained from before the trigger.

For a more graphic example, change the Pulse Generator settings for a pulse width of approximately 100 ms and Single Pulse operation. Change the 8100 Sample Interval to 1 ms. Press the ARM button to cause recording to begin (see Section 3.33). The unit is now taking data, and a display of the base line will be shown. Produce a single pulse from the Pulse Generator. The pulse will move onto the display screen from right to left and stop at the center.

NOTE: In Pretrigger Recording, recording begins at Arm and terminates when the Trigger Delay has run out. Trigger is prohibited until the arm delay has run out. To insure that the memory contains continuous meaningful data, always make the sum of Arm and Trigger Delays greater than 2.05 so that at least 2048 new samples will be stored before recording is terminated.

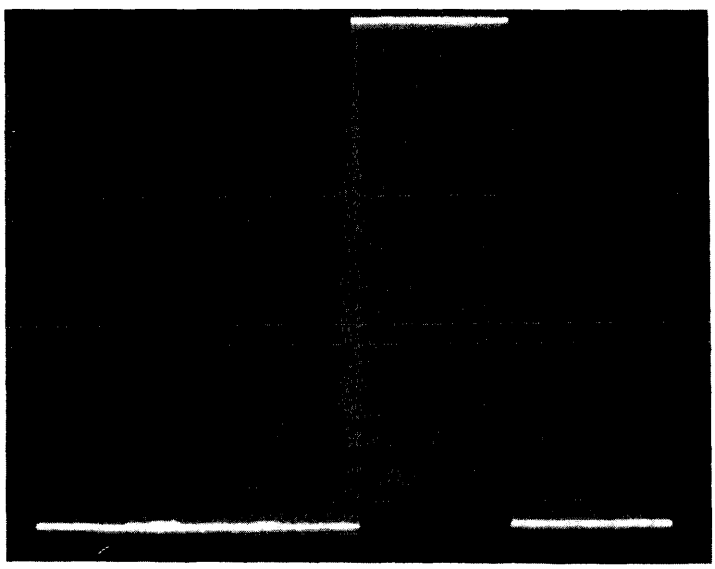


Figure 4.6 Pretrigger Recording, Illustrating about One-Half of Recorded Signal Contains "Prior-Event" Data.

4.5.3 Switched Time Base Mode

Return the settings to those used in paragraph 4.41 (except set the Channel A Input Offset to -0.99). The Switched Time Base mode will be used to illustrate a pulse at 50 ns per point (Time Base A), and after 400 samples will change time base to the 0.2 µs per point (Time Base B) as used in paragraph 4.41.

Set the generator for 50 µsec repetitive pulses of 1.5 V amplitude at a 20 KHz rate. Change Sample Interval switch to 0.2 µs per point. Press the SET ALT INTERVAL. Set Sample Interval switch to 50 ns per point. The A and B time bases are now set. Set Trigger Delay to 0.40. Set Dual Time Base pushbutton to ON (in). The display should change to show one wide pulse and about 6 narrow pulses. Change the Trigger Delay and observe the shifting of the point of change in the sampling rate.

SECTION V

Digital Control Interface

5.1 Introduction

The Model 8100 provides a versatile and comprehensive digital monitoring and control interface for remote and/or automatic operation and readout. This interface is designed to be especially convenient for operation with a digital computer (or computer terminal). In addition, the Model 8100 contains the necessary control, isolation and timing circuitry to allow it to be connected in parallel on a time-share "port" of a digital controller along with other like or similar devices. Conversely, the digital control interface can be hard-wired to simply output the data in the digital memory of the Model 8100 upon front panel and/or remote commands.

The digital control is effected via a bit-parallel, word-serial data exchange. That is, digital control functions are executed by successive digital "words" made up of a number of parallel bits. The versatility of this interface is greatly enhanced by a field of pins in the interface connector which allows the user (or system designer) to independently assign the logical definition of each sub-field of bits in the control "word". This is readily done with appropriate ground straps on the mating connector.

This field of hard-wire programming pins also contains three pins for assigning the "address" of the unit. Thus, a number of units can be connected in parallel on a digital "bus" and individually controlled.

Virtually all front panel control functions (except the power-on switch and the display positioning controls) can be exercised via the digital interface. However, not all of these controls need be under remote control at any one time. The remote control can be applied to the functions by control groups (such as the Arm or Trigger control groups). Thus, any control group or combination of control groups may be under remote digital control. Also, control of a control group or groups can be released for manual front panel operation and/or put under remote operation with the proper digital instruction.

Note that none of the front panel controls include an External or Remote position. This is because the digital interface has the ability to usurp control from the front panel without regard to the physical position of the manual buttons and knobs.

5.2 Connector Definitions

The 50-pin rear panel connector, J1, provides the physical interface for digital output and control. The connector is an Amphenol Micro-Ribbon 57-40500. The mating connector is an Amphenol part number 57-30500.

The pin assignments for the digital interface are listed in the following table:

Pin #	Mnemonic	Description	
1	B0	Input Data 2^0 (Least Significant Bit)	Input Operand
2	B1	Input Data 2^1	
3	B2	Input Data 2^2	
4	B3	Input Data 2^3	
5	B4	Input Data 2^4	
6	B5	Input Data 2^5	
7	B6	Input Data 2^6	
8	B7	Input Data 2^7	
9	B8	Input Data 2^8	Operator (Function Code)
10	B9	Input Data 2^9	
11	B10	Input Data 2^{10}	
12	B11	Input Data 2^{11}	
13	B12	Input Data 2^{12}	
14	B13	Input Data 2^{13}	Address
15	B14	Input Data 2^{14}	
16	B15	Input Data 2^{15} (Most Significant Bit)	
17	CMD	Command - An input used with Flag to regulate the data exchange.	
18	FLG	Flag - An output used with Command to regulate the data exchange.	
19	Logic Definition Field	Defines Pos or Neg logic for Inputs B0 thru B12	
20		Defines address state for B13	Address Assignment
21		Defines address state for B14	
22		Defines address state for B15	
23		Defines Pos or Neg logic for CMD input.	
24		Defines Pos or Neg logic for FLG output.	
25		Defines Pos or Neg logic for Outputs D0 through D7	
26	D0	Output Data for 2^0 (LSB)	Output Operand
27	D1	Output Data for 2^1	
28	D2	Output Data for 2^2	
29	D3	Output Data for 2^3	
30	D4	Output Data for 2^4	
31	D5	Output Data for 2^5	
32	D6	Output Data for 2^6	
33	D7	Output Data for 2^7 (MSB)	
34		+5 V DC	
35-50	Ground	Signal Common and Chassis	

5.3 Signal Specifications

This section describes the electrical and timing characteristics of the input and output signals for digital output and control of the Model 8100.

5.3.1 Inputs

The inputs comprise 16 input data connections (B0 through B15) and one control line (CMD). Each of these lines accepts standard TTL digital signals (2.4 to 5.0 V high, 0 to 0.4 V low) and presents a load approximating that of one and one-half TTL gates, i.e. each input line requires a nominal current sink of 2 mA to input a "low". The inputs can be positive or negative true (Pos or Neg Logic), depending upon the ground-strapping of the appropriate pins in the Logic Definition Field (pins 19 and 23, see 5.33 below.)

5.3.2 Outputs

The outputs comprise eight output data connections (D0 through D7) and one control line (FLG). The FLG output is a supervisory data exchange bit used in conjunction with the CMD input. The output data lines are only active when the unit is correctly "addressed". That is, the outputs do not present any signal nor place any load on the output lines unless the address code on the input address lines (B13, B14, B15) corresponds to the code as programmed on the address definition pins in the Logic Definition Field (20, 21 and 22). Each of the output lines is capable of driving up to 30 standard TTL loads (maximum fan-out = 30). The outputs will be positive or negative true (Pos or Neg logic), depending upon the connections in the Logic Definition Field (pins 24 and 25, see below).

5.3.3 Logic Definition Field Connections

The Logic Definition Field of pins in the interface allows the user to define the "polarity" or "sense" of the digital input and output lines, and to define the "address" to be assigned to the unit for digital control. Each sub-field of digital information bits (lines) can be independently assigned to be positive or negative true (Pos or Neg logic).

Positive true is defined to be the representation of a binary "one" by a positive (high) signal and the representation of a binary "zero" by a zero (low) signal. Conversely, negative true or negative logic is defined to be the representation of a binary "one" by a zero (low) signal and the representation of a binary "zero" by a positive (high) signal.

Positive true or positive logic signals are defined for a selected group of data bits by leaving the appropriate pin in the Logic Definition Field open-circuited. Conversely, negative logic will be defined by connecting the appropriate pin to ground. For example, negative logic inputs will be accepted on the B0 through B12 inputs providing that pin 19 is connected to ground.

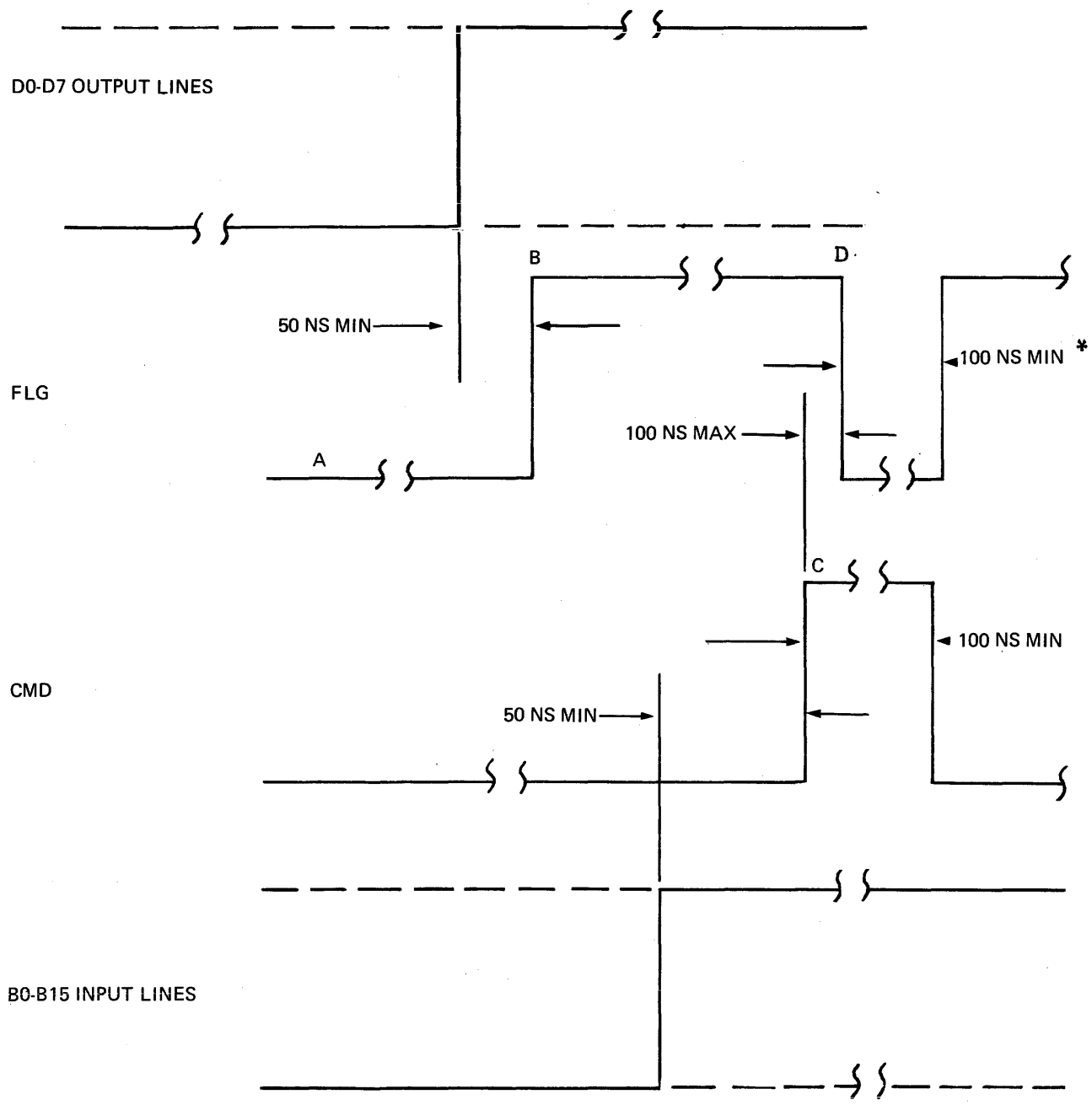
Similarly, the "address" that will be required in order to input digital control information to the unit is defined by appropriate ground connections. For each "address" input bit that is to be recognized as "high", the corresponding address definition pin in the Logic Definition Field should be left open-circuited. Conversely, each "address" input bit that is to be recognized as "low" must have its corresponding address definition pin grounded. For instance, if the desired address of the unit is to be "101" (assuming a positive logic convention), the address definition pin number 21 should be connected to ground denoting the "0" or low signal is to be recognized and pins 20 and 22 should be left disconnected. Note that positive or negative logic convention for the address is purely a matter of the definition of the convention used in describing the connections to the Logic Definition Field in terms of the logic to be used. Thus, if all three pins in the Logic Definition Field are left ungrounded (open), this defines an address of "111" using the positive logic definition and "000" when the negative logic definition is used.

5.3.4 Control Timing

All digital inputs and outputs from the Model 8100 are regulated by two control signals: the output flag (FLG) signal and the input command CMD) signal. The FLG output signal indicates the output data status of the Model 8100 and acknowledges the acceptance of input data. The CMD input signal initiates the input data function. This is sometimes referred to as "data request-request honored" data exchange control.

In the following discussion, defining the FLG and CMD signals and their interrelationships, binary logic notation will be used, i.e. binary 0 (zero) and 1 (one) will be used to define the signals. The representation of these binary values as positive (high) or low electrical signals will be dependent upon the logic definitions on the appropriate pins in the Logic Definition Field (see discussion above).

The timing and transitions for the FLG and CMD signals as well as their interrelationships and timing with respect to the input and output data are described in the following subparagraphs and the Data Exchange Timing Diagram, (Fig. 5.1).



A. CMD signals not accepted when FLG is low.
B. Record or previous instruction completed, ready for next instruction.
C. Causes 8100 to execute the input (B0-B15) instruction and/or fetch the new (next) data output (D0-D7) word. Assumes that present 8100 data output has been read and/or a new data input word is ready.
D. CMD accepted, 8100 busy.

*Note: Nominal FLG width is 200 to 250 nanoseconds. Last FLG (2048th) in AUTO output mode is 100ns wide. Also the FLG low time may be as much as 1 millisec (latency) when data output interval exceeds 100 µsec.

Figure 5.1 Data Exchange Timing Diagram

5.3.4.1 FLG level 1

When the FLG signal is a binary 1, a CMD can be input (0 to 1 transition) and it will be accepted and the input data instruction will be executed.

5.3.4.2 FLG 1 to 0 transition

The 1 to 0 transition of the FLG signal denotes that the CMD input has been accepted. The CMD signal may be returned to 0 (subject to a minimum "dwell" time of 100 nsec, see 5.346 below).

5.3.4.3 FLG level 0

When the FLG signal is a binary 0, the unit is "busy" and no command signals (CMD 0 to 1 transitions) or input data instructions will be accepted.

5.3.4.4 FLG 0 to 1 transition

The 0 to 1 transition of the FLG signal denotes that the input data instruction has been executed and that the unit is ready for another command. Any output data as a result of the input instruction is applied to the output data lines 50 nsec prior to this transition and the output data will be held as long as the input instruction data (which enables or "gates" the appropriate output data) is maintained and the next CMD (0 to 1 transition) has not occurred. If no output data is required, the input data may be changed. The CMD signal may be held at a binary 1 or it may be returned to 0 during this period with no effect on the output data.

5.3.4.5 CMD 0 to 1 transition

Causes the action or instruction defined by the input data to be executed (or initiates the specified action). The input data should be applied at least 50 nsec prior to the CMD transition and the data should be held until the resulting FLG 0 to 1 transition and until the resulting output data (if appropriate) has been received and stored by the digital controller.

5.3.4.6 Minimum pulse width

The minimum "dwell" time in either the binary 1 or 0 state for the CMD signal is 100 nsec. Narrower pulse width may result in failure of the unit to recognize the signal. Similarly, the FLG output signal will not be produced with binary 1 or 0 pulses of less than 100 nsec duration.

5.3.5 Output Data Rates

The signal data in the memory of the Model 8100 can be output asynchronously at rates up to 2×10^6 words/sec under the control of the Flag and Command signals. The output rate is influenced by the internal clock frequency and the need to refresh the memory between output words at low read rates. The former is evidenced by a 0.5 µsec latency in the output with respect to a 2 MHz synchronous clock. This latency does not reduce the average data rate of the unit but it does cause a cyclic "grouping" of the data which is particularly noticable at rates near the maximum rate of 2×10^6 words/sec. For instance, at an average output rate of 1.5×10^6 words/sec, the words would be spaced in time by alternating periods of 0.5 µsec and 1.0 µsec.

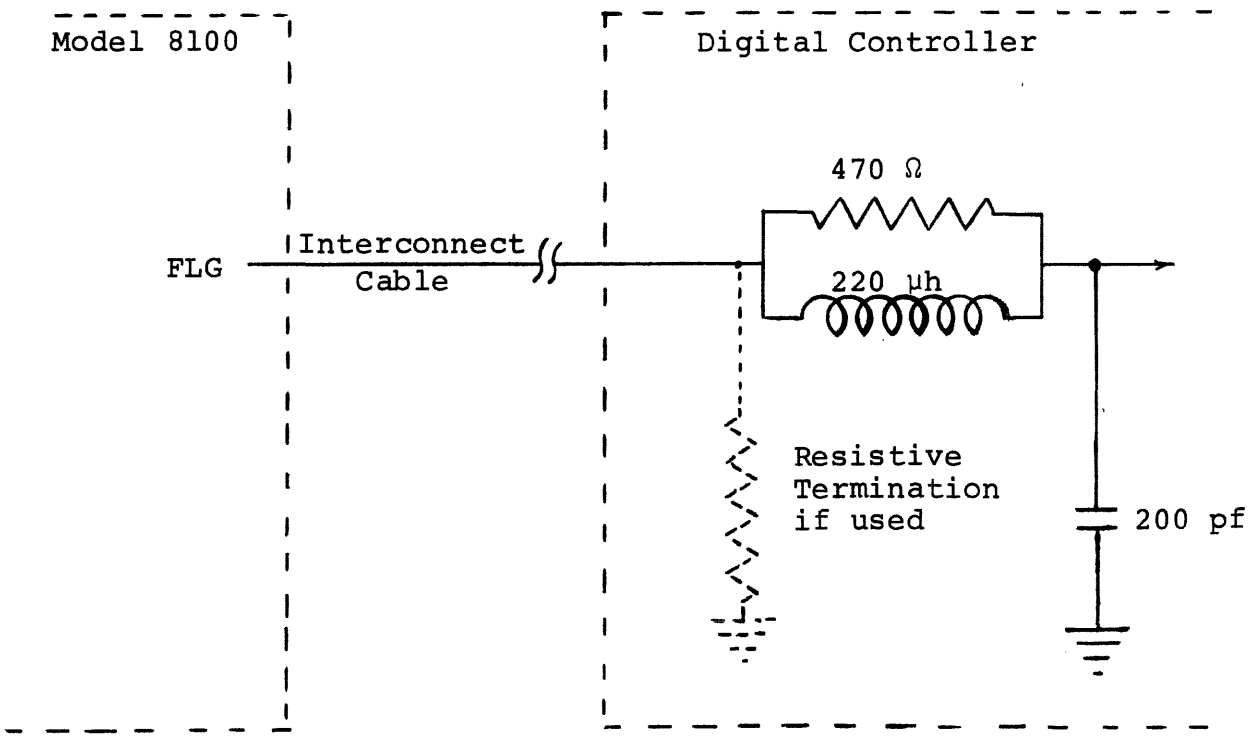
As the digital memory in the Model 8100 is made up of MOS shift registers, the memory must be cycled periodically in order to prevent loss of data. Thus, protective circuitry is provided in the unit to detect the need for cycling the memory and cause this to occur during the digital output whenever the output rate is low. During the time that the memory is being cycled, no additional output data is available. This leads to an output latency of up to the full memory cycle time (1 ms) whenever the output rate is at or below 10 KHz. This phenomenon is evidenced as follows: Average data rates are continuous from 1×10^4 to 2×10^6 words/sec. Data rates less than 1×10^4 words/sec will exhibit up to 1.0 ms latency, i.e., if more than 100 µsec. occurs between data request commands, delays of up to 1.0 ms will occur between output data words.

5.3.6 Cable Parameter Compensation

The Model 8100 is designed to facilitate rapid digital data transfer. For cable lengths up to about six feet between the Model 8100 and the digital controlling device, no special shielding, terminations or compensation is required on the data input or output lines. Any reflected signals, ringing and/or cross-coupling will normally be attenuated and "settled out" well within the 50 nsec settling time delay between the output data and the FLG signal or during the 50 nsec delay (specified above) between the input data word presentation and the CMD "zero" to "one" transition.

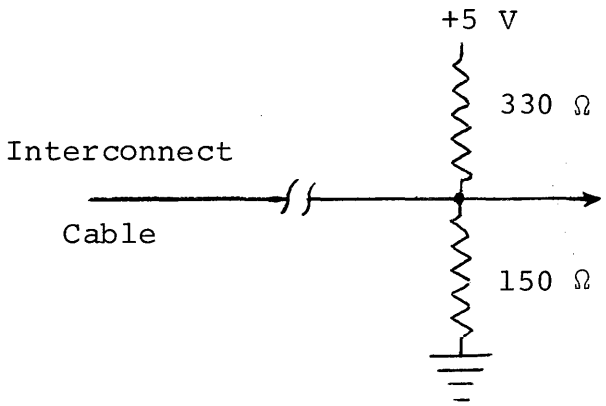
The FLG and CMD signals do, however, require some considerations in order to insure immunity from line ringing and/or cross-talk phenomenon. For these reasons, the Command input to the unit incorporates a line filter which effectively prevents false or multiple signals due to cross-talk.

Similarly, it is recommended that a simple filter be utilized on the Flag signal at the cable termination on the digital controller. The circuit shown in the following sketch has been found to be particularly effective for this use.



Cable lengths in excess of about six feet may require special considerations in order to insure error-free data transfer at high data rates. This is most easily accomplished by terminating the signal lines (twisted pairs) with 100 ohms.

The following recommended biased load network may be connected to each output line at the load end of the cable to provide a 100 ohm termination while preserving full fan-out (30 TTL) capability.



The inputs on the digital input lines of the Model 8100 provide high impedances so that long cable lengths with data transfer rates near the maximum possible may require input line terminations. In these instances, the above network is recommended on each data input line at the digital interface connector of the unit (+5 V is provided on pin 34).

5.3.7 Memory Data Output Code

When the data in the digital memory of the Model 8100 is transferred to the digital output (under control of the FLG signal and input signals), it is output in a binary code called "2's (two's) complement". This code is particularly useful and convenient for representing values which may range over positive and negative scales. Such is the case in the Model 8100. The value represented by each word in the memory represents an instantaneous voltage level of the input signal and the input signal may be any value between plus and minus the fullscale selected on the input attenuator (depending on the amount of input offset selected).

The "2's complement" binary code is arranged such that 00000000 is at midscale representing zero input volts (with no input offset). All positive values are scaled directly with pure binary digit weighting and a resolution of 1 in 128 (the most significant bit is always zero for positive polarity input values). All negative values are coded such that the most significant bit is always "one" and the absolute magnitude is obtained by complementing the binary number (changing all 1's to 0's and vice-versa) and adding a binary "1". This results in an output code that is very convenient and efficient for computation and/or analysis by a digital computer.

The following table presents representative examples of the "2's complement" output code.

	2's Complement	Decimal Value	Equiv. Volts (±1 V Scale)
Positive Full Scale	01111111	+127	+0.992
	01111110	+126	+0.984
	01111101	+125	+0.976
	.		
Positive Half Scale	01000000	+64	+0.500
	.		
	.		
	.		
	00000011	+3	+0.023
	00000010	+2	+0.016
Positive One Count	00000001	+1	+0.008
Zero	00000000	0	0.000
Negative One Count	11111111	-1	-0.008
	11111110	-2	-0.016
	11111101	-3	-0.023
	.		
	.		
	.		
Negative Half Scale	11000000	-64	-0.500
	.		
	.		
	.		
	10000010	-126	-0.984
	10000001	-127	-0.992
Negative Full Scale	10000000	-128	-1.000

The decimal value in the above table is obtained by direct binary to decimal conversion for all positive values and by converting the negative values as described above and then conducting the binary to decimal conversion. The equivalent voltage is obtained by multiplying the ratio of the decimal value to 128 (the full scale count) by the full scale voltage. For instance, the negative half scale voltage is -64/128 x 1.0 V = -0.5 V for a full scale voltage range of ±1 V.

5.4 Data Output Only Operation

The Model 8100 can be readily configured to output digital data without resorting to complete computer control. This type of operation is particularly useful when it is desired to simply transfer the digitized signal data in the memory of the unit to another device or memory. Examples of this application include output of the digital data to punched tape or directly into the storage cells of a signal averager. The procedures to accomplish this type of operation are described in this section.

The connection of a few jumpers on the mating connector for the digital control interface (J1) will configure the Model 8100 to output the digital data under simple strobe type control. These jumpers should be connected as follows:

(a) Connect jumper connections between pins 11, 13 and ground (pins 35-50).

(b) Determine whether positive or negative logic is to be defined for the digital output, the FLG output and the CMD input and add the appropriate jumpers (if any) as described above for the Logic Definition Field connections (see 5.33). CAUTION: do not connect the Logic Definition Field to define negative logic for the data inputs (B0 to B15) as this will negate the jumpers in (a) above. In other words, pin 19 must be left open-circuited.

With these jumper connections in the digital interface mating connector, the digital data in the memory will be available through the digital output lines D0 through D7. Two conditions must be met in order to output the data: (1) the unit must not be recording an input signal, and (2) the digital output must be initiated. Note also that once the digital output has been initiated, the Record mode will be inhibited until the digital output has been completed or terminated.

The FLG output signal indicates the end of the Record mode with a 0 to 1 transition. The FLG signal will be a 1 at the beginning of the Record cycle and throughout the Record period, but it will always transition to a 0 at the end of the Record cycle and then transition back to a 1 state in 5μsec.

The digital output can be initiated automatically or on demand by front panel or remote inputs, depending on the output mode selected (refer to the group of front panel controls labeled OUTPUT). NOTE: Although the memory size is 2048 words, only the first 2024 words are specified to contain good data. The following statements describe the operation for each of the output mode conditions:

5.4.1 OFF

If the Off output mode has been selected, no subsequent output of the digital data can be made unless another mode is selected. The unit will automatically switch to the Display mode at the end of recording and the FLG output signal will indicate that recording is complete, as described above.

5.4.2 AUTO

Selection of the Auto output mode will cause the unit to automatically switch to the output mode at the end of the Record cycle and the transition of the FLG signal from 0 to 1 will indicate that recording is complete and the Output mode established. Each word of the digital data is strobed through the D0-D7 output lines by the CMD and FLG signals as described in the Control Timing discussion above. Record and Display modes are inhibited in AUTO operation until after the entire memory contents (2048 words) has been output in this manner or until the OFF output mode is selected. Either of these events will cause the unit to revert to the Display mode. No further output in the AUTO mode is possible until after the next Record cycle.

5.4.3 EDIT

Use of the Edit output mode permits the user to observe the reconstructed signal in the memory on the display prior to the transfer of the data through the digital interface. With Edit mode selected, the unit will go into Display mode after the end of the Record mode (denoted by the 200 ns 1 to 0/0 to 1 transition of the FLG signal). The digital output can be initiated by one of two ways: (1) by momentarily depressing the front panel Digital Output pushbutton, or (2) a 0 to 1 transition on the CMD input line. Either of these two actions will cause the FLG signal to go to zero

for approximately 250 nsec to a maximum of about 1 msec (depending upon the instantaneous relationship between the initiation signal and the Display cycle) and then the FLG signal will transition back to a "1", indicating that the first word in the memory is available on the output data lines. Subsequent words of the digital data are strobed through the D0-D7 output lines by the CMD and FLG signals as described in the Control Timing discussion in paragraph 5.34 above. The 2048th Flag pulse width will be only about 100 nsec. Unlike the Auto output mode, care may be necessary in the Edit mode to apply exactly 2048 CMD pulses in strobing the digital data out of the unit. After the 2048th CMD strobe, the unit will automatically revert to the Display mode and the Record mode will no longer be inhibited. The very next CMD 0 to 1 transition (the 2049th) will, however, again initiate the data Output mode resulting in the inhibition of the Record mode. Switching to the Off output mode will, however, at any time terminate the digital output and cause the unit to go to the Display mode. Therefore, rather than clocking exactly 2048 CMD pulses, it may be more convenient to switch to the Off mode after the desired number of data words (or more) have been output.

5.5 Full Digital Control Operation

The digital control interface for the Model 8100 consists of a bit-parallel, word-serial data exchange arrangement. Sixteen parallel input data bits plus one input control bit and eight output data bits plus one output control bit comprise this interface. The physical and electrical characteristics of these bits have already been defined. This section will define their information states and the interrelationships by which the monitoring and/or control of any or all functions of the unit may be accomplished.

5.5.1 Instruction Timing

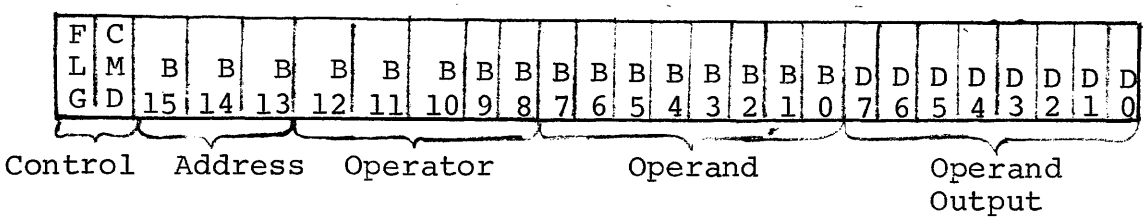
The preceding Control Timing section discussed the timing relationships between the CMD and FLG control bits and the data exchanged across the digital interface. Those relationships are arranged for rapid data exchange and for most control instructions the unit will accept, act upon, and be ready for any new (or the logical next) instruction as rapidly as indicated by the return of the FLG signal to a logic one. There are, however, certain control functions in the unit which, when exercised, must have additional time to assure the completion of the function prior to operation of the unit, i.e., prior

to initiation of the Record function. These control functions are: Input Range, Input Coupling, Input Offset, Trigger Level, Trigger Source, and Trigger Coupling. After execution of instructions which cause any of these parameters to change, at least 10 msec should elapse before "arming" of the unit preparatory to recording input data. One convenient way to minimize this delay is to execute the instructions involving these functions as early as possible in a series of instructions. It is not necessary to delay the next instruction following a change in one of these functions as long as the next instruction does not result in the imminent initiation of the Record mode. An internal delay generator is provided in case the controlling system does not have real-time capability. A "reset" command (see 5.531b) will result in a flag approximately 10 msec later. NOTE: The "reset" instruction resets all delay counters and the memory counter and causes all "ready" status lines to go to zero. The Flag signal also is returned to zero and the memory contents are disturbed. This instruction is also useful to terminate a long record sweep or arm or trigger delay. It is also highly recommended that the unit not be programmed into AUTO ARM or given an ARM instruction until all other program instructions have been input to the 8100.

5.5.2 Word Definition

In the following discussion, all signals will be referred to by their mnemonic as defined in the table given under the Connector Definitions section. In addition, binary logic notation will be used when referring to the states of each signal, i.e. binary zero (0) or one (1) will be used in referring to the state of a binary signal. The electrical representation of these binary values will be dependent upon the logic definition connections in the Logic Definition Field (see discussion above).

The logical structure or format of the digital interface may be viewed as successive digital words or instructions with or without resultant response data. It is convenient to describe the various parts of each instruction in much the same terms as used for computer instructions, i.e. each instruction contains data fields called "Address", "Operator" and "Operand". In addition, there are two special supervisory control bits, the output FLG signal and the input CMD bit. The following figure illustrates the digital instruction or word arranged by its data fields:



The control and address fields have been defined and their operation described in the Signal Specification section above. Therefore, their function will not be detailed in this section. Rather, the operator and operand fields will be defined and described. The B0-B7 input operand and the D0-D7 output operand can, under certain circumstances, be connected in parallel (see discussion below for this type of connection).

5.5.3 Instruction Formats

The operator/operand instruction formats are arranged in logical groups by the type of action or operation involved. In each of the groups, not all possible combinations of the data bits are used. For these unused or unassigned combinations, two types of action are possible. In some cases, use of the unassigned bit structure will result in

no operation or no action by the unit - this is notated in the following discussion as NOP. In other instances, use of an unassigned bit structure of sequence is undefined, i.e. the result of using it may vary depending on other variables. This type of bit structure will be notated as UND in the following discussion. Obviously care should be taken to avoid inadvertent instructions with UND structures.

The operator data field is that part of the instruction which defines the type of action or operation to be performed. Other terms often used for this field are opcode or function code. The operator may also define the form or structure of the operand or operands.

An operand contains the specific information or data required to implement a particular operation or the data resulting from the execution of the instruction.

The first three operator bits (B12, B11 and B10) in the digital instruction for the Model 8100 define the type of instruction. The remaining two operator bits (B9 and B8) define the specific instruction and define the operand (s) if required. The following instruction types are defined by the B12, B11 and B10 operator bits:

B12	B11	B10	Instruction Type
0	0	0	NOP
0	0	1	NOP
0	1	0	Control Functions
0	1	1	Output Mode, Time Base & Record Mode
1	0	0	Channel A Functions
1	0	1	Channel B Functions
1	1	0	Arm Functions
1	1	1	Trigger Functions

The following list defines the specific instructions and operands for each of the instruction types:

5.5.3.1. Control Functions:

(a) Set program mask

B12	B11	B10	B9	B8
0	1	0	0	0

This operator defines the group or groups of front panel control functions that, upon execution of this instruction, will be under remote digital control. An input operand is required but no output operand will result from this operation. The input operand structure is:

B7	Trigger control group.
B6	Arm control group.
B5	Channel B control group.
B4	Channel A control group.
B3	Time base, output mode and record mode groups.
B2/B1/B0	NOP

Setting the appropriate operand bit (s) to a "one" causes the corresponding control group (s) to be disabled and subsequent input data for these variables to be accepted. Setting the appropriate bit to a "zero" retains or returns the corresponding front panel control group (s) to an enabled condition.

(b) Set function

B12	B11	B10	B9	B8
0	1	0	0	1

This operator defines a control action to be initiated upon the execution of the instruction. An input operand is required but no output operand will result from the operation. The input operand structure is:

B7	Clear and update "status" word.
B6	Plot.
B5	NOP.
B4	Arm.
B3	Trigger.
B2	NOP.
B1	Switch to alternate time base.
B0	Reset.

Setting the appropriate operand bit to a "one" causes the corresponding control action upon the execution of the instruction providing that only a single "one" is set in any single instruction. The operand becomes undefined (UND) if more than a single "one" is set.

(c) Read status

B12	B11	B10	B9	B8
0	1	0	1	0

This operator enables the status of the unit to be reported upon the initiation of the instruction. No input operand is required but an output operand is produced. The operator must be present until the output operand has been "read" and its information is no longer required. The output operand structure is:

D7	Recording in process.
D6	Output data ready (goes low after output mode is established).
D5	Ready for arm.
D4	Ready for trigger.
D3	Offscale Channel A (+).*
D2	Offscale Channel A (-).*
D1	Offscale Channel B (+).*
D0	Offscale Channel B (-).*

*These events are stored during a recording interval.

A "one" in the appropriate operand bit defines the corresponding function to be true and a "zero" defines the function to be false.

(d) Enable output data

B12	B11	B10	B9	B8
0	1	0	1	1

This operator enables the output of the data in the memory of the unit. No input operand is required but an output operand is produced if the unit is in the AUTO or EDIT output mode (see 5.5.3.2 (c) below) and the unit is not recording. See also section 5.4 for a description of the output modes.

Note: A CMD pulse is not required to input Read Status and Enable Output Data. Therefore, to avoid, for instance, inadvertently initiating digital output during EDIT mode (see para 5.4.3), a CMD should not be issued with these two operators.

Thus, the operator must be held at the input while each of the desired data in the memory (the successive words of data) is being transferred through the output operand field. The FLG signal will transition from 0 to 1 at the end of the Record cycle. The first word of the data will be available in the operand field upon the next FLG 0 to 1 transition as requested by a CMD 0 to 1 transition (assuming the output mode has been initiated, see 5.51). The output operand structure is:

D7	Output data 2^7
D6	Output data 2^6
D5	Output data 2^5
D4	Output data 2^4
D3	Output data 2^3
D2	Output data 2^2
D1	Output data 1^1
D0	Output data 2^0

Refer to the Memory Data Output Code section for the definition of the output operand.

5.5.3.2 Output Mode, Time Base & Record Mode

(a) Main time base

B12	B11	B10	B9	B8
0	1	1	0	0

This operator defines the parameters for remote selection of the main time base for input sampling. An input operand is required but no output operand is produced. The input operand structure is:

Source	B7	B6
Internal	0	0
External <.25 msec	1	0
External >1 msec	0	1
External .25 msec - 1 msec	1	1

Units	B5	B4
useconds	0	0
mseconds	0	1
seconds	1	0
NOP	1	1

Range	B3	B2	B1	B0
.01	0	0	0	0
.02	0	0	0	1
.05	0	0	1	0
0.1	0	0	1	1
0.2	0	1	0	0
0.5	0	1	0	1
1.0	0	1	1	0
2.0	0	1	1	1
5.0	1	0	0	0
10.0	1	0	0	1
	1	0	1	0
	.			
UND	.			
	1	1	1	1

(b) Alternate time base

B12	B11	B10	B9	B8
0	1	1	0	1

This operator defines the parameters for remote selection of the alternate time base for input sampling. An input operand is required but no output operand is produced. The input operand structure is identical to 5.532(a) above.

(c) Output mode

B12	B11	B10	B9	B8
0	1	1	1	0

This operator defines the parameters for remote selection of the output mode for the signal in the memory. Refer to Section 5.4 for an operational description of the output modes. An input operand is required but no output operand is produced. The input operand structure is:

B7	B6	B5	B4	B3	B2
N	O	P			

B1	B0	
0	0	Off
0	1	Auto
1	0	Edit
1	1	UND

(d) Record mode

B12	B11	B10	B9	B8
0	1	1	1	1

This operator defines the parameters for remote selection of the signals which control the Record mode of the unit. Refer to Sections 3.32 and 3.33 for an operational description of these functions. An input operand is required but no output operand is produced. The input operand structure is:

NOP	B7	B6
Start Record	**B5**	**B4**
Arm	0	0
Delayed Arm	0	1
Trigger	1	0
Delayed Trigger	1	1
Switch to Alternate Time Base	**B3**	**B2**
NOP	0	0
Delayed Arm	0	1
Trigger	1	0
Delayed Trigger	1	1
Stop Record	**B1**	**B0**
End of Sweep	0	0
NOP	0	1
Trigger	1	0
Delayed Trigger	1	1

5.5.3.3 Channel A functions

(a) Range and coupling

B12	B11	B10	B9	B8
1	0	0	0	0

This operator defines the parameters for remote selection of the input voltage range and input coupling for Channel A. An input operand is required but no output operand is produced. The input operand structure is:

+ Input Coupling	B7	B6
Off	0	0
AC	0	1
DC	1	0
NOP	1	1

- Input Coupling	B5	B4
Off	0	0
AC	0	1
DC	1	0
NOP	1	1

Range	B3	B2	B1	B0
±.05 V	0	0	0	0
±0.1 V	0	0	0	1
±0.2 V	0	0	1	0
±0.5 V	0	0	1	1
±1.0 V	0	1	0	0
±2.0 V	0	1	0	1
±5.0 V	0	1	1	0
	0	1	1	1
UND	.	.	.	.
	1	1	1	1

(b) Input offset magnitude

B12	B11	B10	B9	B8
1	0	0	0	1

This operator defines the parameters for remote selection of the magnitude of the input offset for Channel A. An input operand is required but no output operand is produced. The input operand structure is:

Most Significant Digit	B7	B6	B5	B4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
UND	1	0	1	0
	.	.	.	.
	1	1	1	1

Least Significant Digit	B3	B2	B1	B0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
UND	1	0	1	0
	.	.	.	.
	1	1	1	1

(c) Input mode and offset sign

B12	B11	B10	B9	B8
1	0	0	1	0

This operator defines the parameters for remote selection of the input mode and offset polarity for Channel A. An input operand is required but no output operand is produced. The input operand structure is:

NOP	B7	B6	B5	B3	B2	B1
Mode	B4					
Off	0					
Input	1					
Polarity	B0					
Minus	1					
Plus	0					

(d) The following operator is a Channel A function NOP combination:

B12	B11	B10	B9	B8
1	0	0	1	1

5.5.3.4 Channel B Functions

All Channel B operators and operands are identical with the respective Channel A instructions with the exception that the B10 bit is a one in all Channel B operators, i.e. all Channel B operators begin:

B12	B11	B10
1	0	1

5.5.3.5 Arm Functions. Minimum delay between Arm and Trigger and between Trigger and start of sweep, is 10 sample intervals. See p 65B.

(a) Delay magnitude - second and least digits

B12	B11	B10	B9	B8
1	1	0	0	0

This operator defines the parameters for remote selection of the second and least digits for the delay magnitude for the arm function. An input operand is required but no output operand is produced. Note that two instructions are required to set this function. The input operand structure is:

Second Digit	B7	B6	B5	B4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

9	1	0	0	1
	1	0	1	0
	.			
UND	.			
	1	1	1	1

Least Digit	B3	B2	B1	B0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	0
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
	1	0	1	0
	.			
UND	.			
	1	1	1	1

(b) Delay magnitude - most significant digit

B12	B11	B10	B9	B8
1	1	0	0	1

This operator defines the parameters for remote selection of the most significant digit of the delay magnitude for the arm function. An input operand is required but no output operand is produced. The input operand structure is:

NOP	B7	B6	B5	B4
MSD	B3	B2	B1	B0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
	1	0	1	0
	.			
UND	.			
	1	1	1	1

(c) Level magnitude

B12	B11	B10	B9	B8
1	1	0	1	0

This operator defines the parameters for remote selection of the level magnitude for the arm function. An input operand is required but no output operand is produced. The input operand structure is:

MSD	B7	B6	B5	B4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
UND	1	0	1	0
	.	.	.	.
	1	1	1	1

LSD	B3	B2	B1	B0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
UND	1	0	1	0
	.	.	.	.
	1	1	1	1

(d) Arm mode, source, slope, coupling and level polarity

B12	B11	B10	B9	B8
1	1	0	1	1

This operator defines the parameters for remote selection of the arm mode, source, slope, coupling and level polarity. An input operand is required but no output operand is produced. The operand structure is:

Mode	B7
Input	0
Auto	1
NOP	B6
Source	B5
External	0
Internal	1
Internal Source	B4
Channel A	0
Channel B	1
Slope	B3
Negative	0
Positive	1
Coupling	B2
DC	0
AC	1
NOP	B1
Level Polarity	B0
Minus	1
Plus	0

5.5.3.6 Trigger Function

All Trigger Function operators and operands are identical with the respective Arm Function instructions with the exception that the B10 bit is a 1 in all Trigger Function operators, i.e. all Trigger Function operators begin:

B12	B11	B10
1	1	1

5.5.4 Parallel Operation

The digital interface of the Model 8100 is arranged to facilitate the operation of up to eight like or similar units on the same set of digital I/O lines. This is done simply by connecting each line or bit in the digital interface of all of the units in parallel with the respective line in the controlling device. Each of the units can then be separately controlled by supplying its unique address (as assigned on each unit) along with the desired digital instructions to that unit.

Parallel operation of the Model 8100 is aided by the use of so-called "tri-state" logic driving all of the unit's digital output lines. This type of logic presents essentially no load (or voltage) on the output lines when it has not been enabled by the specified "address" combination inputs. Thus, the output of paralleled units do not "fight" each other and no signal degradation is caused by the parallel connection. This is only true, of course, if all paralleled units have different assigned addresses. Identical addresses on two or more paralleled units will cause contention.

The Model 8100 may be paralleled with similar devices which do not have "tri-state" output but use the more common "open-collector" logic for their digital output lines providing the common load resistor for the open-collectors on each output line is returned to +5 V and the outputs of any of these units are arranged to "go high" when they are not "addressed".

5.5.5 Parallel Input/Output Operands

The output operand of the digital interface for the Model 8100 can be connected in parallel with the input operand without affecting the operation of the unit. Examination of the Instruction Format Definitions above reveals that no instruction requires both an input and an output operand. Thus, no contention or "lock-up" conditions exist within the unit. Therefore, this type of operation is feasible if the controlling device has the capability to use the same lines for inputs and output as a function of its normal operation.

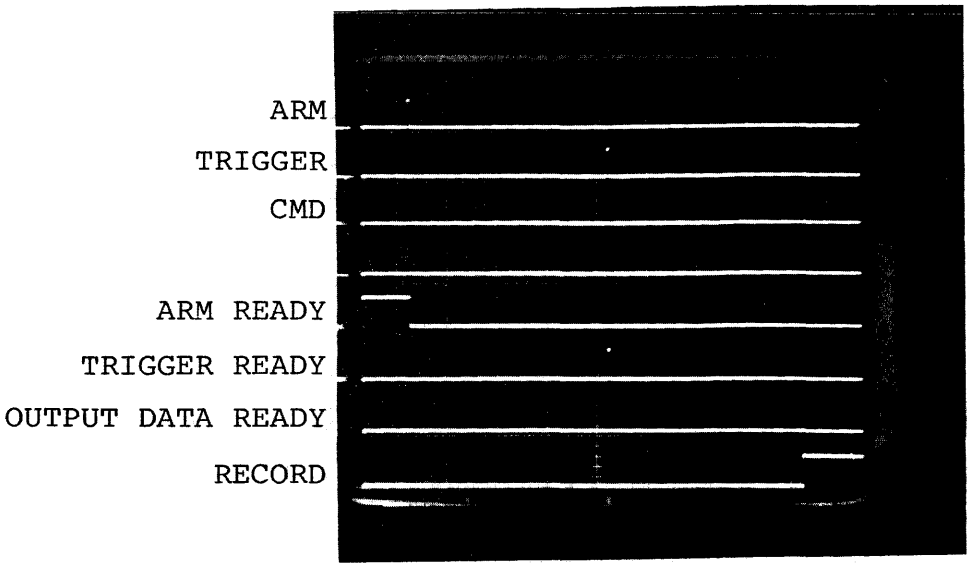
5.6 Interface Timing Diagrams

The timing diagrams that follow describe various output modes for the 8100. The times displayed and noted are typical values and are not to be taken as absolute values.

The photos were taken from a CRT, which was displaying the output of our Model 810-D Digital Logic Recorder. Using this instrument allowed the convenient capture and display of the one-time events that are presented.

In most cases that follow, various signals are shown for reference only. Not all the signals are simultaneously available at the rear panel connector, J1. For instance, the Record signal (Recording In Process) is available at the rear panel connector by issuing the operator "Read Status." For Photos 1, 2, and 3, this was done. In Photos 4 and 5, the status bits were obtained internally, and the data bits were obtained through J1 by using "Enable Output Data."

Start Record Sweep



TIME: 2.5 µS/Div.

Photo 1 illustrates the timing relationships of the period of time where the 8100 accepts an Arm signal (Arm Ready), a Trigger signal (Trigger Ready), and begin a record sweep (Record). The 8100 operating modes were as follows:

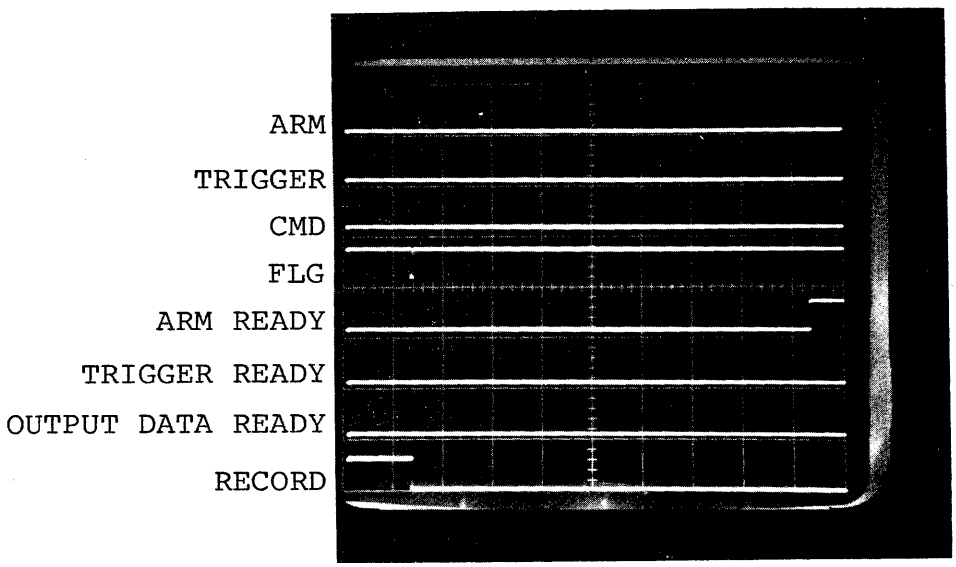
Arm:	Manual
Trigger:	Auto
Record:	Normal
Output:	Off
Sample Interval:	1 µS

Prior to the time period of this photo, the 8100 was in the Display Mode.

Each major division of the CRT equals 2.5 µS. The 10 samples delay between the Arm pulse and Trigger Ready, and between the Trigger pulse and start of Record, are readily apparent.

In the Auto Trigger mode, as soon as Trigger Ready goes high, a Trigger pulse is generated inside the 8100. Ten sample intervals later, the unit starts recording.

End Record Sweep; Output Mode: Off



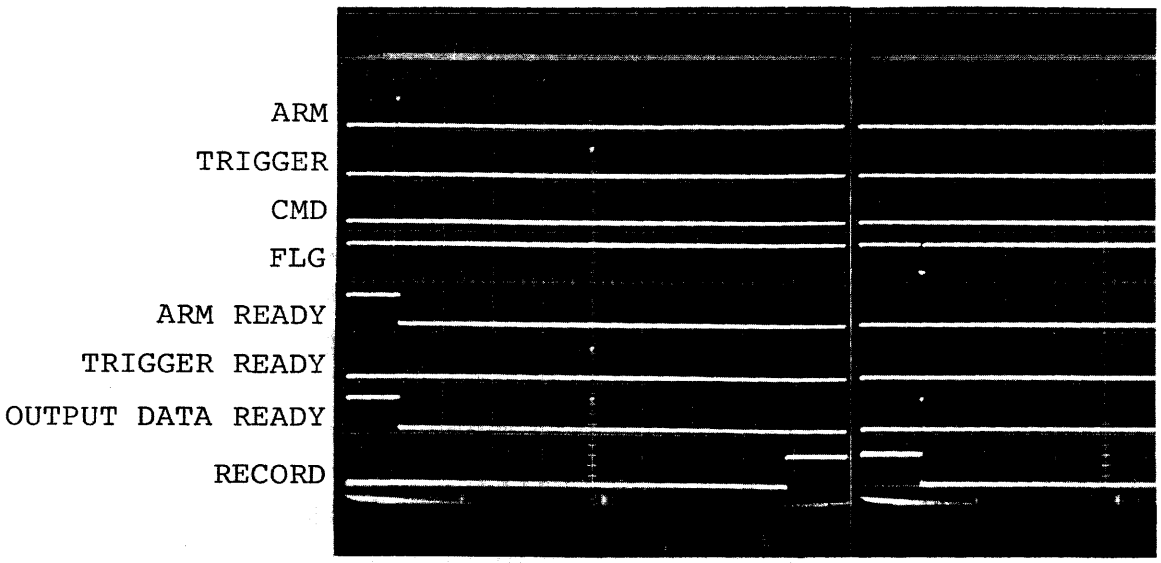
TIME: 250 µS/div.

Photo 2 shows the relationship between the End of Sweep (EOS), Flg, and Arm Ready signals. Each division of the CRT equals 250 µS.

The Flg is high during Record. When Record goes low, signalling EOS, the Flg goes low for 200 nS (5 µS for S/N 2085 and higher) and then goes high. Two display sweeps (8 div X 250 µS = 2 mS; one display sweep is 1 mS long.) after EOS, Arm Ready goes high. At this point, the unit is ready to accept an Arm pulse.

Prior to the time period of this photo, the 8100 was in the Record Mode. Other conditions of the 8100 were the same as for Photo 1.

Begin/End Record Sweep; Output Mode: Auto



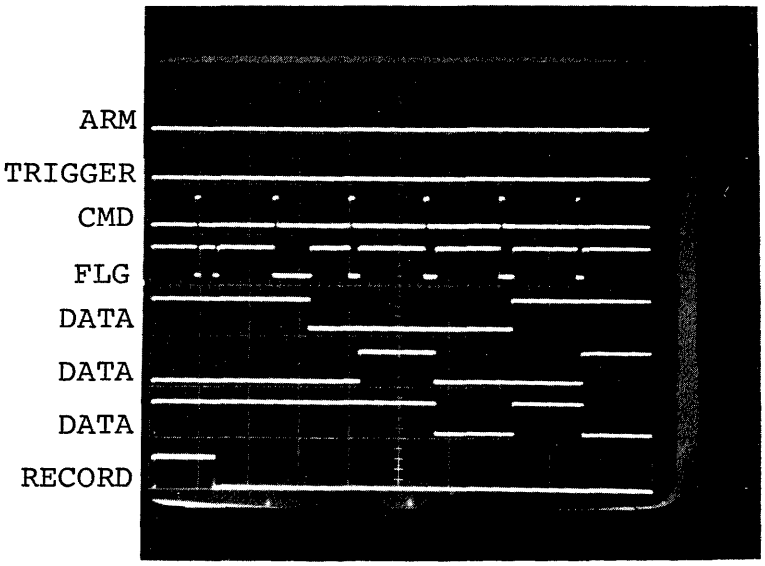
TIME: 2.5 µS/div

Photo 3 shows the activity of the Output Data Ready signal before and after a record sweep when the 8100 is in Output Mode: Auto. All other 8100 conditions are the same as in Photo 1. Photo time is 2.5 µS/division.

The AUTO OUTPUT button was pressed prior to the time period of the photo. Thus, the Output Data Ready line is high before the Arm pulse. When the Trigger pulse is received, Output Data Ready responds with a short pulse. Also, at EOS, Output Data Ready outputs a pulse of approximately 50 nS.

When the Flg goes high again, the first data word is in the output register. Since no Cmd pulses are issued to the 8100, no Flg transitions occur after EOS.

End Record Sweep; Output Mode: Auto with Cmd Pulses



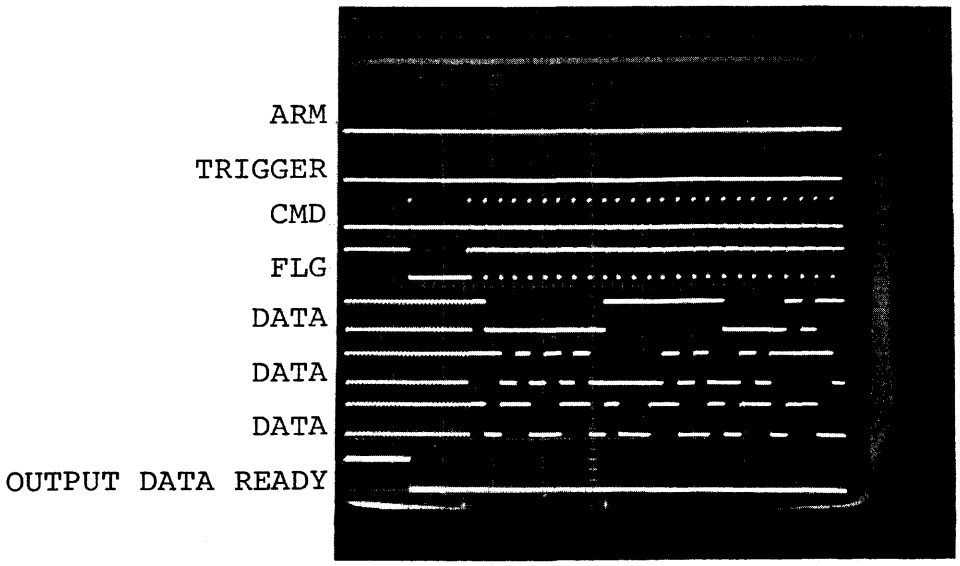
TIME: 2.5 µS/div.

Photo 4 shows what occurs after EOS when in the Auto Output mode, and Cmd pulses are inputted to the 8100. The photo time is 2.5 µS/division.

Three of the eight data lines are shown. Bits 1 and 3 are high before EOS, since "ones" happened to be stored in the output register before EOS. The first Cmd/Flg "handshake" is meaningless, except that it illustrates that whenever the Flg is high, and a Cmd is input, the Flg will go low and then high again, acknowledging the Cmd.

The second Cmd results in the Flg going low for 2 µS and then going high. Valid output data is available on the rising edge of the Flg. The first Flg low state response to the first Cmd is typically longer than subsequent Flg low states, as shown above. Close examination of the data bit state changes reveals that the data changes just prior to the rising edge of the Flg.

End Record Sweep; Output Mode: Edit With Cmd Pulses



TIME: 125 µS/div.

Photo 5 illustrates the Edit Mode. The photo time is 125 µS/div. In this case, the Digital Output Mode is initiated by the first Cmd pulse. Output Data Ready goes low when digital output is established (by front panel button or Cmd pulse). The Flg responds to the Cmd pulse by going low.

In the Edit Mode, the 8100 goes into Display Mode immediately after Record. Prior to the first Cmd, it can be seen that the data bits are changing at a fast rate. This illustrates the Display Mode.

When the first Cmd was issued, the memory had not yet completed a display sweep. A wait of 125 µS, in this case, occurred before the Flg went up to signal the first word being available. Subsequent data words were then output in response to the Cmd pulses, issued here at 40 µS intervals.

5.7 Fast Turn Around Program

This program, or variations of it, is helpful when the user wishes to output less than the full memory contents of the unit, and return to a ready for record mode.

Set output mode on front panel to AUTO

Set ARM to AUTO

B 12	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0	
0	1	0	1	1	N	N	N	N	N	N	N	N	Enable output data

When flag goes up after Record, "Handshake" out the desired number of data words, then set in the following sequence of instructions with proper Flag/CMD "Handshakes:"

0	1	0	0	0	0	0	0	0	1	N	N	N	Set program mask; output
0	1	1	1	0	N	N	N	N	N	N	0	0	Output mode; off
0	1	1	1	0	N	N	N	N	N	N	0	1	Output mode; auto
0	1	0	0	0	0	0	0	0	0	N	N	N	Set program mask; front panel
0	1	0	1	1	N	N	N	N	N	N	N	N	Enable output data

Note that a program register needs only five bits to change.

0	1	X	X	X	0	0	0	0	X	N	0	X

The arm function can also be supplied externally in a setup where such a signal is available.

SECTION VI

Calibration Procedures

6.1 Calibration of Display Output

Adjustments are provided to calibrate X and Y display outputs to a specific display unit. Connect the unit as shown in Figure 4.3b on page 32. Some X-Y displays such as the TEKTRONIX Model 604 and the DUMONT Model 1000 require a Zener diode clamp across the "X" input of the display to limit the X ramp to 3 V. If this diode is not used, viewing of the complete stored waveform in the X5 and X10 expand modes will not be possible. Install the zener diode as shown in Figure 6.1.

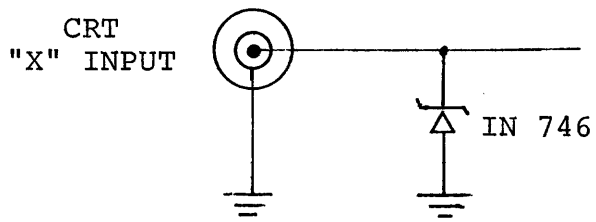


Figure 6.1 Installation of the Zener Diode

Depress the CAL button and make the adjustments shown below:

NOTE: All adjustments are made on the "D-A" board located just in front of the power supply section. The appropriate adjustments are easily made from the top. Refer to Figure 6.2.

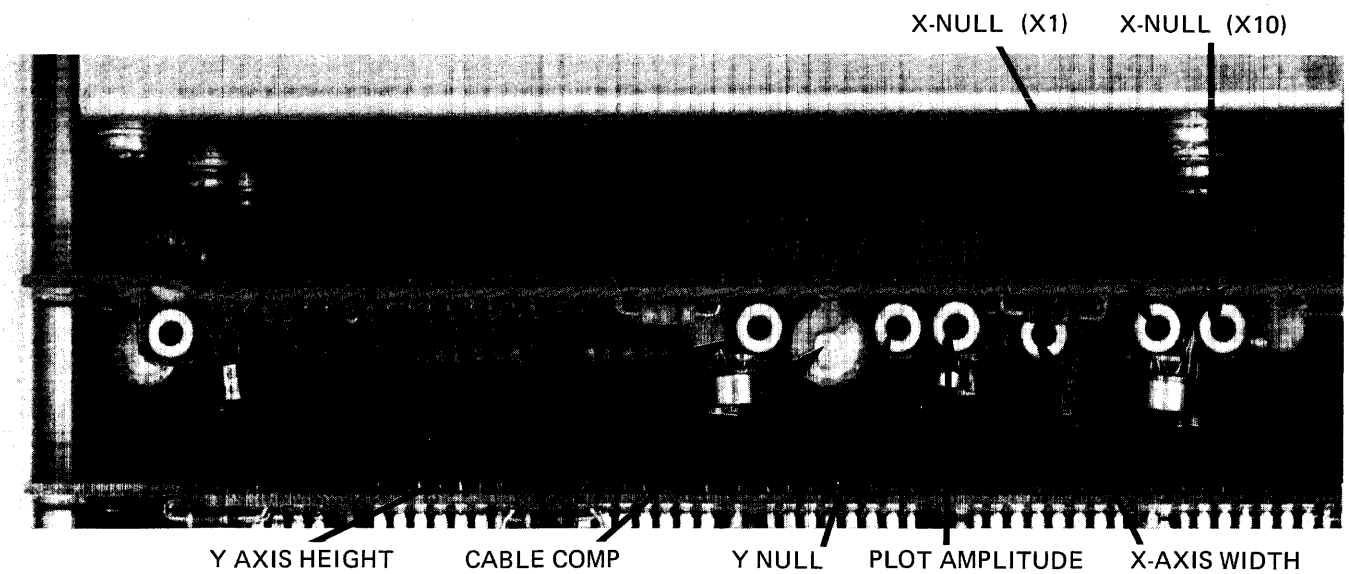


Figure 6.2

1. With Calibrate signal displayed, adjust "Y-axis height" (R1) to give full-scale display (adjustable from 0.4 to 1.2 V full scale).

2. Adjust "X-axis width" (R2) to give full-scale display. Be sure Display Expansion is in X1 position.

3. Adjust "Y-NULL" (R3) to give minimum up-and-down jitter.

4. Adjust "X-NULL (X1)" (R4) to give minimum horizontal jitter.

5. Expand display to X10 Display mode. Adjust "X-NULL (X10)" (R5) for minimum horizontal jitter.

6. Adjust "Cable Compensate" (C5) for clearest square wave presentation.

6.2 Recalibration of the Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the 8100. The entire instrument was calibrated before shipment and should not require any recalibration for at least six months.

Since the input amplifier gain calibration will be used as a reference for the other adjustments, it is recommended that this be performed first.

6.3 Required Test Equipment and Test Aids

The following test equipment will be required to calibrate the Model 8100.

1. DC Standard or Precision Power Supply capable of driving a 50 ohm load with a voltage range of 0 to 5 V.

2. Digital Voltmeter: DC range 0-10 V, 3-½ digit minimum.

3. Function generator: Output 10 V, peak-to-peak into a 25 ohm load (2-50 ohm inputs in parallel). Frequency range 0.01 Hz to 1 MHz.

4. X-Y Display or Oscilloscope.

5. (1) Amphenol #57-3050 connector, (8) 150 Ω ⅛W resistors, (8) Til 209 LEDs.

6.4 Input Amplifier Gain Adjustment

This section describes the "digital" calibration procedure for the input amplifier gain and balance adjustments. This method produces a more accurate gain adjustment, and is easier to perform than the supplemental procedure.

In addition to the test equipment listed in Section 6.3, a digital readout device, Figure 6.3, is required. Also, the "enable output data" instruction must be programmed on the rear panel connector at all times during this calibration.

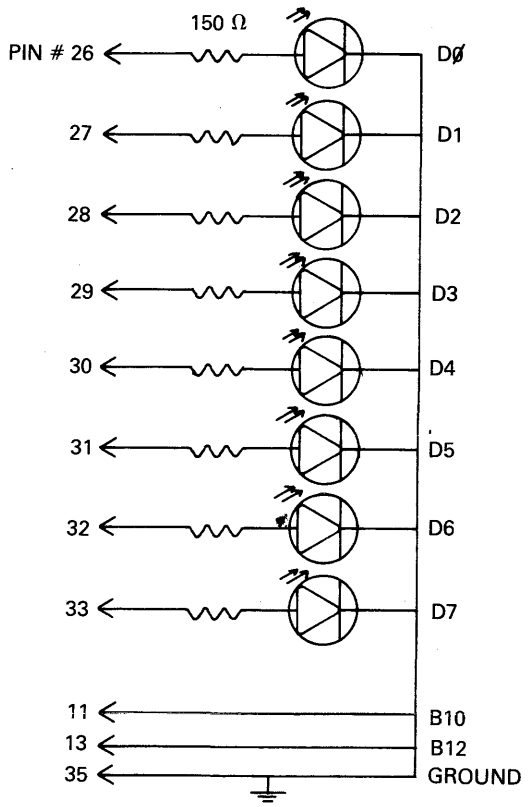


Figure 6.3

6.4.1 Set up the test equipment and 8100 as in Section 6.8. Perform the crossover adjustment on both channels.

6.4.2 Remove the Function Generator from the input and change the front panel controls as follows:

CONTROL	SETTINGS
Arm Delay	0.00
Trigger Delay	0.00
Record Mode	Normal
Trigger Mode	Auto

6.4.3 Press manual arm and manual trigger to initiate the Auto Mode. Connect the digital output device to J1.

6.4.4 With no input connected, the digital number on the output should be "00000000". If it is not, adjust "Balance" Pot, see 6.6 for location, until the output registers all zeroes.

6.4.5 With the input range set to ± 5 V, connect the output of the adjustable 5 V power supply to the + input of CHA.

6.4.6 Adjust the power supply output to equal +4.92 ±0.01 V. The digital output should read 01111110 ± 1 LSB.

6.4.7 If the digital output does not read 01111110, adjust the CHA gain pot until output reads 01111110.

6.4.8 Remove DC supply from the input. Digital output should register all zeroes. If it does not, readjust the Balance Pot and repeat gain adjustment.

NOTE: This procedure can be used to adjust accurately the gain for any input range that is desired. Calibrating the 5 V range does give an overall calibration but users who wish much greater accuracy on only one range may use this method to achieve it.

6.4.9 Repeat above procedure for channel B.

6.5 Input Amplifier Gain Adjustment (supplemental)

There are three adjustments associated with each channel of the input amplifier. These adjustments are located in the right portion of the input amplifier circuit board. The exact location of these adjustments is shown in Figure 6.6.

1. Remove the four screws from the top cover.

2. Remove the PC Board hold down bracket (1 screw).

3. Remove the "0 Bit" and the "1-6 Bit" PC Cards, see Figure 9.25, page 139 for procedure.

4. Connect one end of an 18 inch piece of insulated wire to test point "a" located on the mother board (see Figure 6.4). Thread the wire out between the front panel and the top of the chassis. Make sure the unconnected end of this wire does not short to the chassis or ground when the instrument is in operation.

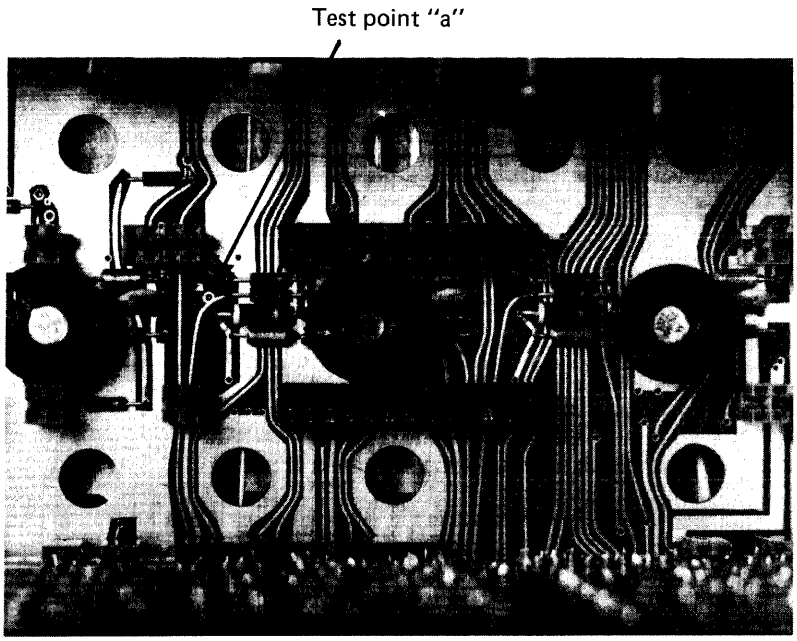


Figure 6.4

5. Re-install the "O Bit" and the "1-6 Bit" PC Cards.

6. Replace top cover, but do not replace screws.

7. Connect the 8100 to a display device - use Figure 4.3b for X-Y display - use Figure 4.3a for oscilloscope.

8. Connect Power cord to the 8100 and turn on power. Allow to stabilize for 10 minutes before making any adjustments.

9. Connect the DC Source to the input shown in Figure 6.5.

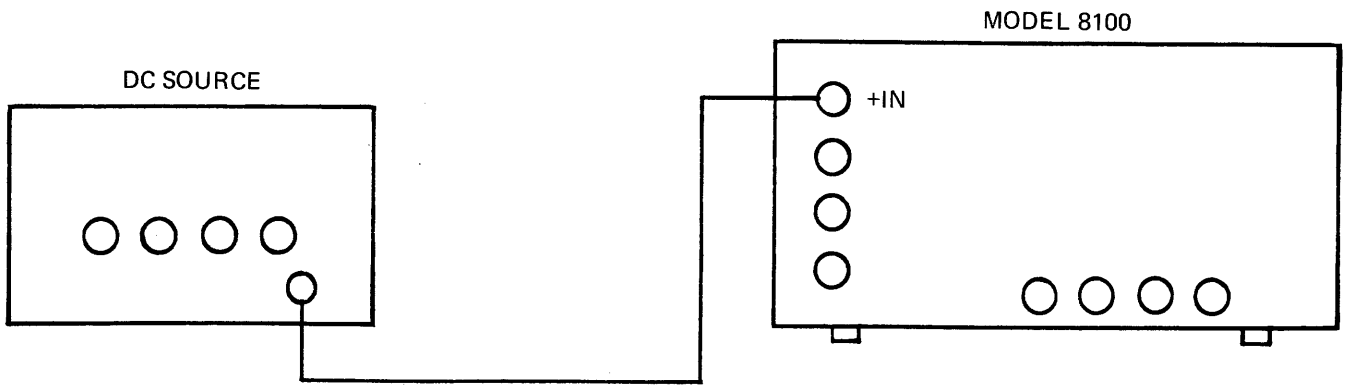


Figure 6.5

10. Connect the digital voltmeter between the wire from test point "a" and chassis ground.

11. Set up front panel controls as follows:

CHAN A Group

+ INPUT - DC	INPUT OFFSET - +.00
± INPUT RANGE - 5	INPUT/OFF - INPUT

CHAN B Group

INPUT/OFF - OFF

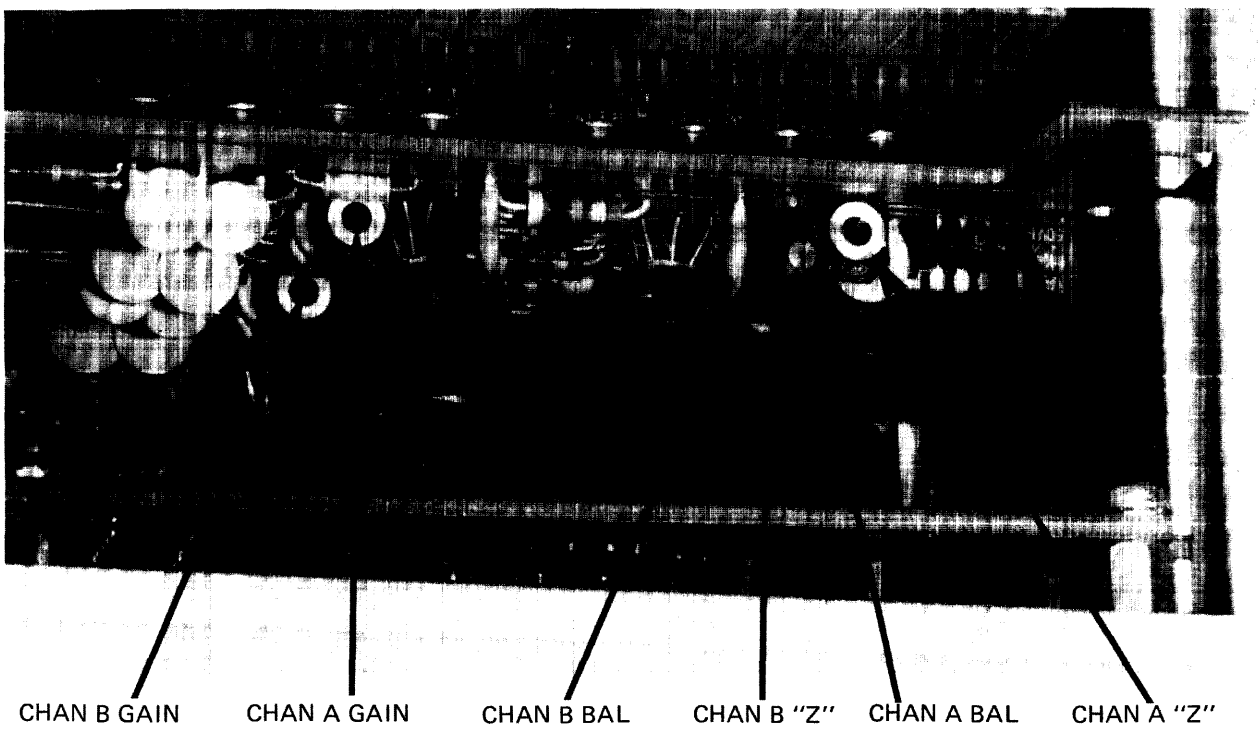


Figure 6.6

12. Set DC source output to 0.00 V. Lift front of cover and adjust CHAN A BAL (see Figure 6.6) control for minimum DC value R60 on voltmeter. Close cover.

13. Set DC source output to +0.10 V.

14. Lift cover and adjust CHAN A "Z" -R58 control (see Figure 6.6)until output at test lead is -0.138 V, close cover.

15. Set DC source output to +5.00 V.

16. Lift cover and adjust CHAN A GAIN control until output at test lead is -6.40 V, close cover.

17. Repeat steps 13 through 16 until there are no changes and both values are correct.

18. Set up front panel controls as follows:

    CHAN A Group

    INPUT/OFF - OFF

    CHAN B Group

    + INPUT - DC INPUT OFFSET - +.00

    ± input range - 5 INPUT/OFF - INPUT

19. Connect DC source to + INPUT of CHAN B.

20. Repeat steps 12 through 17 for CHAN B.

21. Remove DC source from input and remove test lead from Mother Board.

6.6 Offset Level Calibration (Digital)

Set CHAN A to INPUT with INPUT OFFSET of -0.99, CHAN B to OFF, ARM MODE to AUTO, TRIGGER MODE to AUTO and TIME BASE SAMPLE INTERVAL to 0.1 µs; SOURCE to INTERNAL. Press Manual Arm or Trigger. Lift cover and adjust CHAN A - Potentiometer on D-A Board until digital output reads 10000001. NOTE: See Page 141 for location of Potentiometers. Close cover. Set CHAN A offset level to +0.99. Lift cover and adjust CHAN A + Potentiometer on D-A board until digital output reads 01111110.

Repeat above procedure for Channel B.

6.7 Arm and Trigger Level Calibration

6.7.1 Arm Calibration

Connect the Function Generator output to the inputs of the 8100 as shown in Figure 6.7.

Set the output of the Function Generator to a 5 kHz triangle wave. Set up 8100 front panel controls as follows:

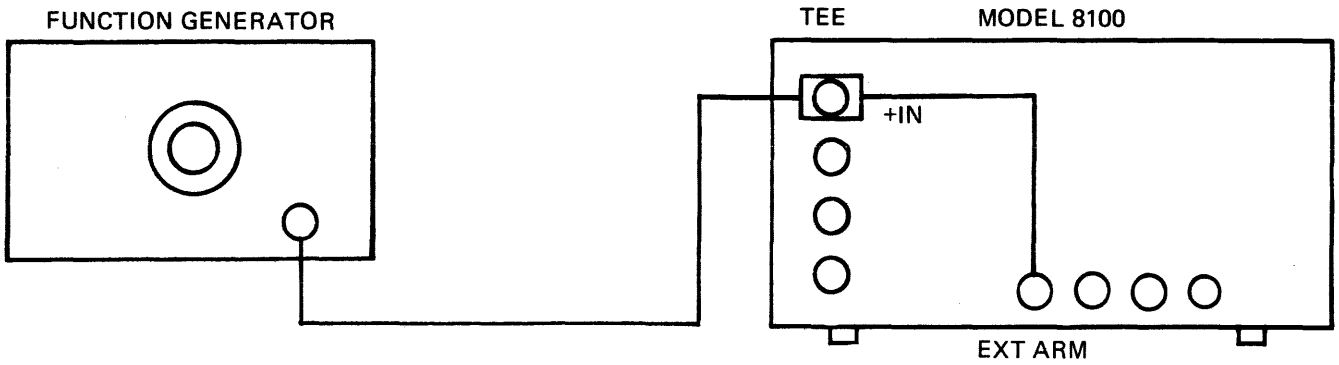


Figure 6.7

CHAN A Group

+ INPUT Coupling - DC

± INPUT RANGE - 5

INPUT OFFSET - +.00

INPUT/OFF - INPUT

CHAN B Group

INPUT/OFF - OFF

TRIGGER Group

MODE - AUTO

ARM Group

DELAY - 0.00

MODE - INPUT

SOURCE - EXT

INTERNAL - CHA

SLOPE - +

COUPLING - DC

LEVEL - +.00

TIME BASE Group

SAMPLE INTERVAL - .1μs

SOURCE - INTERNAL

OUTPUT

OFF

RECORD MODE

NORM/PRETRIG - NORM

DUAL TIME BASE - OFF

Set output level of Function Generator so that a full-scale signal is at the input and that both offscale lights flicker intermittantly. Also note that display should be as shown in Figure 6.8.

Set ARM level to +0.99.

Lift cover and adjust "+ARM" potentiometer until 8100 intermittantly arms. Close cover. (Refer to page 141.)

Set ARM level to -0.99.

Lift cover and adjust "-ARM" potentiometer until 8100 intermittantly arms. Close cover.

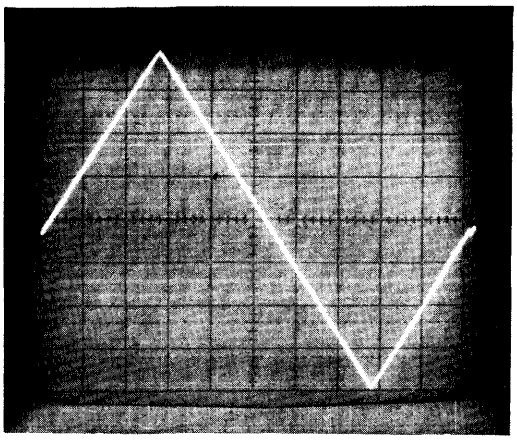


Figure 6.8

Connect Function Generator output to 8100 inputs as shown in Figure 6.9.

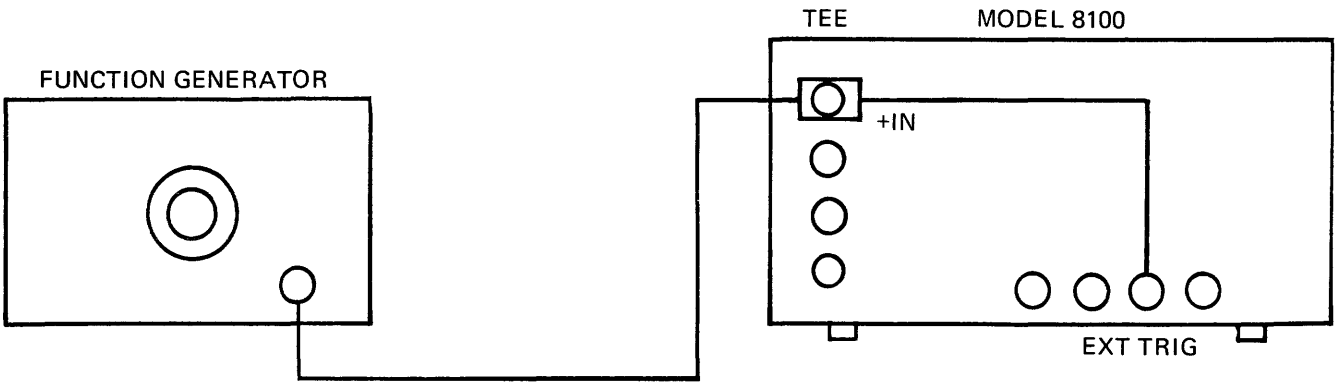


Figure 6.9

Change the following front panel controls:

ARM Group

INPUT/AUTO - AUTO

TRIGGER Group

DELAY - 0.00

MODE - INPUT

SOURCE - EXT

INTERNAL - CH A

SLOPE - +

COUPLING - DC

LEVEL - +.99

6.7.2 Trigger Calibration

Repeat 6.7.1 substituting Trigger functions and adjustments for the Arm functions, etc.

6.8 Internal Arm/Trigger Level

This section describes the procedure for adjusting the internal trigger circuit on the front panel of the 8100. For location of adjustments, see Figure 6.10.

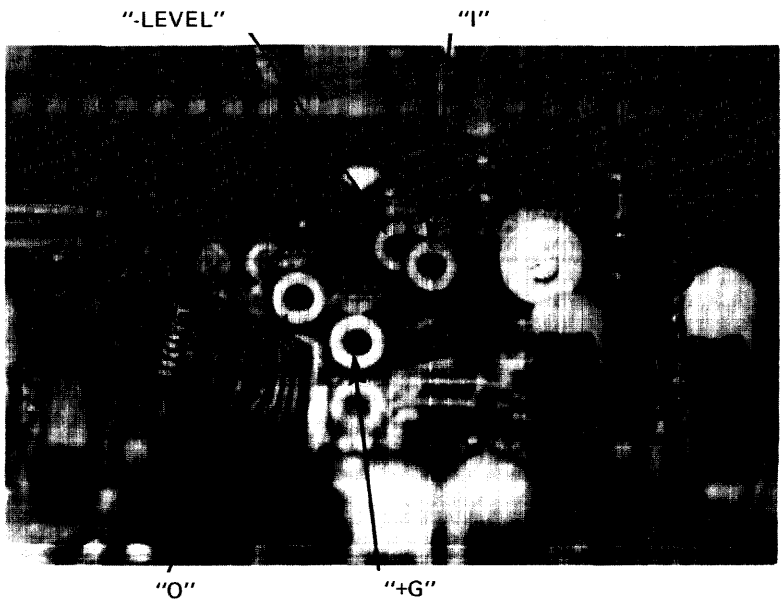


Figure 6.10

6.8.1 See Figure 6.8 and connect the Function Generator as shown. Adjust the input signal for a triangle 5 kHz, 10 V pp waveform.

6.8.2 Set controls on 8100 as follows:

CHAN A Group		
+ INPUT	-	DC COUPLING
INPUT RANGE	-	± 5
INPUT OFFSET	-	0.00
INPUT/OFF	-	INPUT
CHAN B Group		OFF
ARM Group		
MODE	-	AUTO

TRIGGER Group

MODE	-	INPUT
SOURCE	-	INTERNAL
LEVEL	-	-0.00
SLOPE	-	+
COUPLING	-	DC
DELAY	-	0.00

TIME BASE Group

SAMPLE INTERVAL	-	0.1 µs
SOURCE	-	INTERNAL

OUTPUT Group OFF

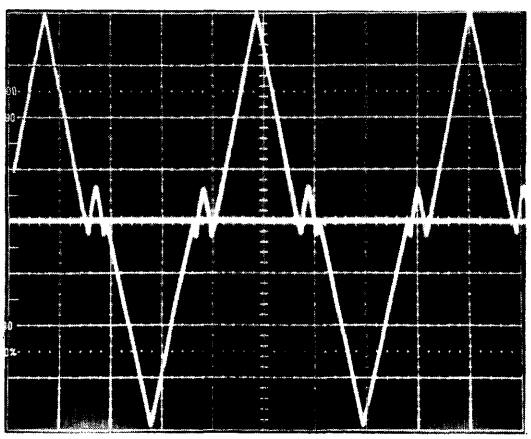
RECORD Mode Both buttons out

EXPAND - X1

6.8.3 Connect scope probe to junction of R71, R72, R73 and R74, see page 114 of manual.

6.8.4 Set input of scope to ground and establish a ground reference on X-axis. Set scope controls as in Figure 6.11.

6.8.5 Adjust Level Pot (R21),I-Pot (R18), G-Pot (R22) and O-Pot (R19) to mid range. Observe a waveform on the scope similar to that in Figure 6.11



Scope: Vert. 0.5 V/div., Horiz. 50 µs/div., Trig. Int + Auto

Figure 6.11

6.8.6 Set vertical switch on scope to 1 V/div. Adjust Level Pot on Front Panel for maximum signal level on scope.

6.8.7 Set scope to 0.5 V/div. Adjust G-Pot for a pattern as in Figure 6.12.

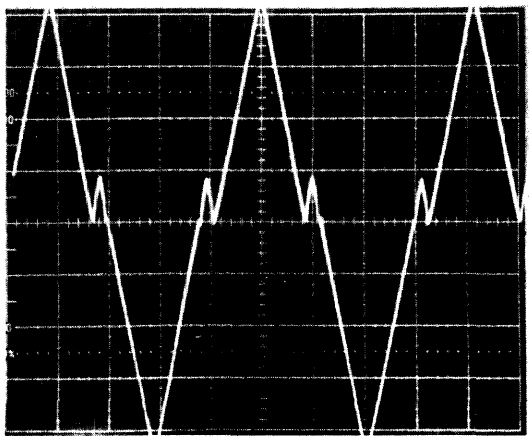


Figure 6.12

6.8.8 Adjust I-Pot to set the positive excursion that rises just above the X-axis between 0.2-0.4 V from the reference. See Figure 6.13.

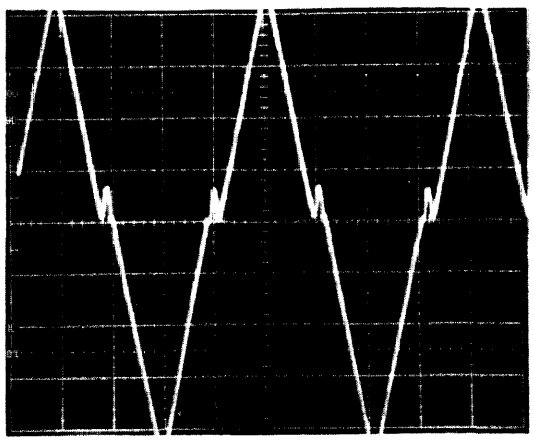


Figure 6.13

6.8.9 Adjust G-Pot to increase gain of the positive-going portion of the waveform. See Figure 6.14. Figure 6.15 shows the effect of the G Pot being incorrectly adjusted.

6.8.10 Set the scope's vertical control to 1 V/div. Adjust "O"-Pot to make the waveform on the scope symmetrical. See Figure 6.16.

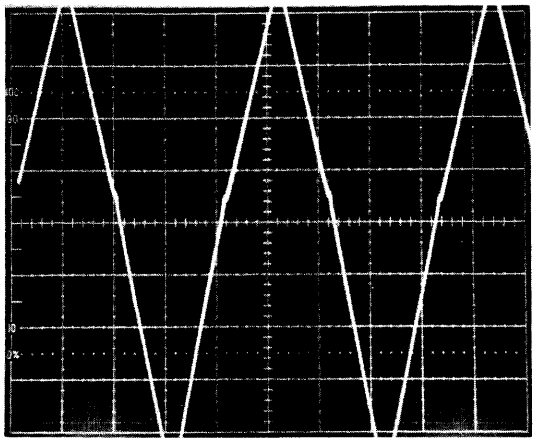


Figure 6.14

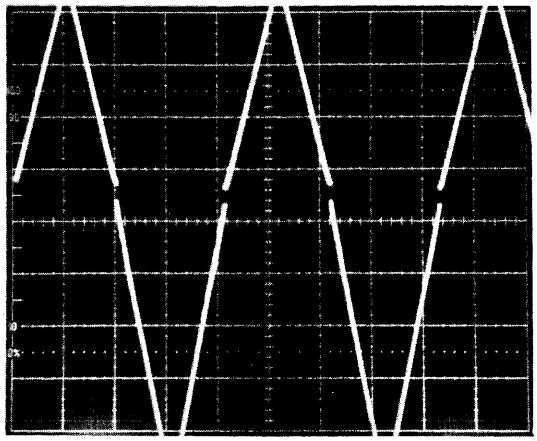


Figure 6.15

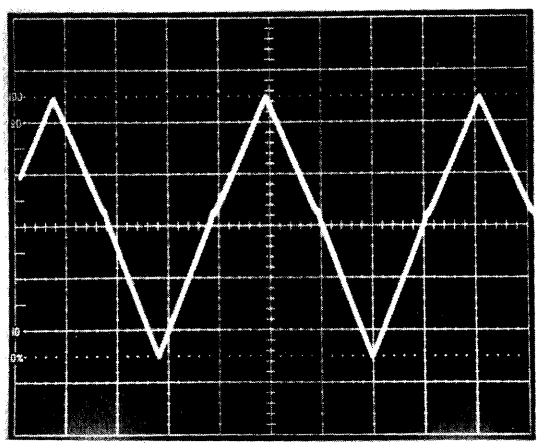


Figure 6.16

6.8.11 Adjust the input waveform to a 50 kHz square wave signal.

6.8.12 Observe Figure 6.17. Adjust C6 to minimize the overshoot at the top of the square wave.

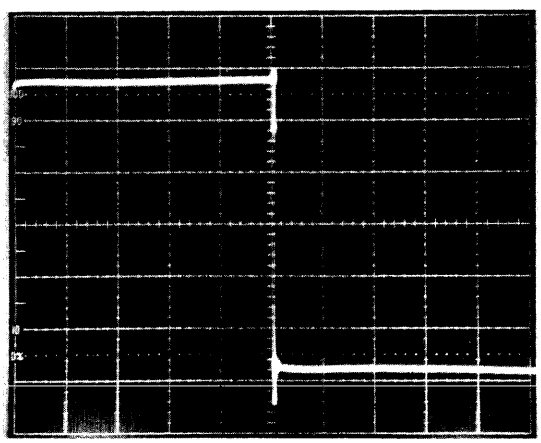


Figure 6.17

6.9 Crossover Adjustment

The crossover adjustment controls the relative position of the "folding" input amplifier signal output in relation to the input range of the Analog to Digital converter. If this control is not in proper adjustment a "gap" or flat spot will occur in the center or "zero volts" of the stored data. This adjustment can be made without affecting the gain adjustment and if necessary can be made without performing the Input Amplifier Gain adjustment, paragraph 6.5.

The location of the crossover adjustment "Z" is shown in Figure 6.6.

Connect the Function Generator as shown in Figure 6.18 and adjust for a 5 kHz triangle wave output.

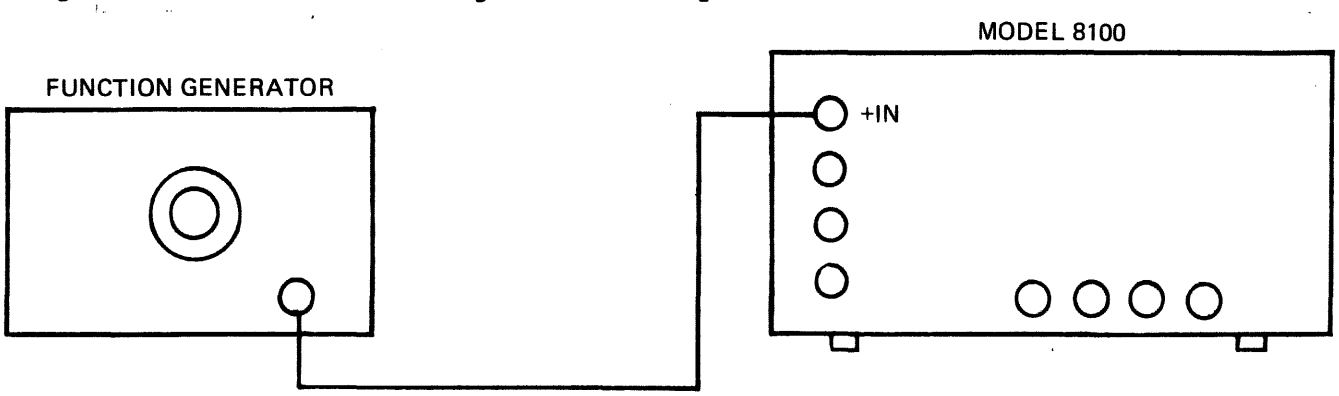


Figure 6.18

Set front panel controls of 8100 as follows:

CHAN A	CHAN B	RECORD MODE
+ INPUT COUPLING - DC	INPUT/OFF - OFF	NORM/PRETRIG - PRETRIG
INPUT RANGE - 5		DUAL TIME BASE - OFF
INPUT OFFSET - +.00	ARM	
INPUT/OFF - INPUT	DELAY - 2.00	
TRIGGER	MODE - AUTO	
DELAY - 1.10	All other ARM buttons out	
MODE - INPUT		
SOURCE - INT	TIME BASE	
SLOPE - +	SAMPLE INTERVAL -0.1µs, INTERNAL	
COUPLING - DC	OUTPUT	
LEVEL - +0.00	OFF (in)	

Set the Function Generator's 5 kHz triangle wave output level so that the peak-to-peak amplitude exceeds the input range by 5 to 10%. The output display should appear as shown in Figure 6.19.

Set the interval to 0.01 μs.

The display should appear as shown in Figure 6.20.

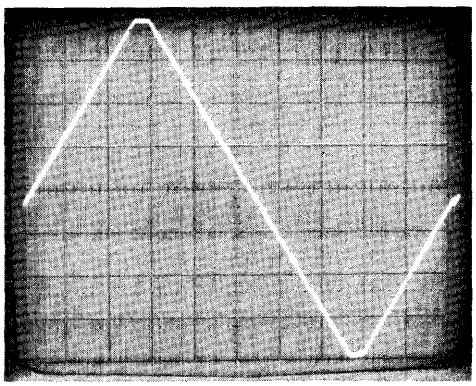


Figure 6.19

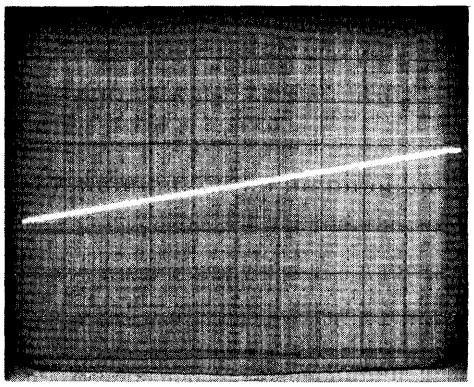


Figure 6.20

Figures 6.21 and 6.22 show the output with the Z pot incorrectly adjusted.

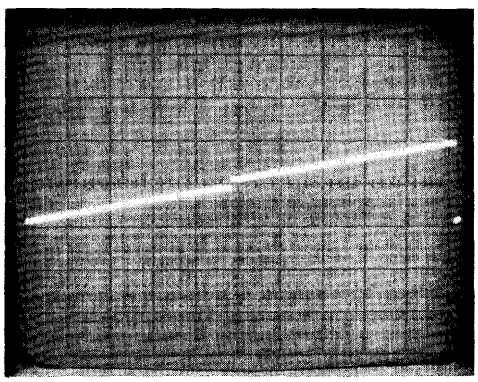


Figure 6.21

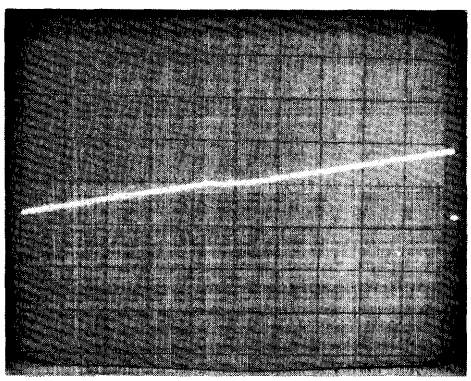


Figure 6.22

Lift front of cover and quickly re-adjust "Z" pot for correct crossover. Close cover and re-check after 5 minutes. If crossover has drifted, re-adjust "Z" pot. Close cover. Re-check after 5 minutes.

Repeat above procedure for CHAN B. Be sure to turn CHAN A OFF.

6.10 Analog-to-Digital Converter Alignment

The alignment of the A/D converter is not described in this manual. Precision test equipment and special test jigs and devices are required to perform this alignment.

The 8100 was properly aligned prior to shipment from the factory and further alignment of the A/D converter is not normally required for the life of the instrument. However, if realignment becomes necessary, the unit should be return to the factory or Regional Service Center to ensure the accuracy of the recalibration.

SECTION VII

TECHNICAL DESCRIPTION

7.1 General Functional Description

This section presents the technical description of the Model 8100 and is intended to give service personnel an overview of the circuits in the unit. This section is divided into two major divisions. The first section is comprised of the data flow, internal-external program function, and the control function block diagrams. The second part gives a detailed description of each circuit on a board-by-board basis.

7.2 Data Flow

7.2.1 Analog Data Flow

Refer to Figure 7.1. The input signal is coupled from the Front Panel BNC connectors to the Input Amplifier Coupling and Attenuator Network. Output from the attenuator network is applied to a video amplifier that provides differential outputs. These outputs from A2 or C2 (Single Channel operation) or A2 and C2 (Dual Channel operation) are applied to a folding circuit (E6). The Folding Circuit (E6) provides a folded version of the input waveform that is fed into the Line Driver (D5), and level changes that switch ON/OFF comparator D4, generating the sign bit.

Line Driver output A out is applied simultaneously to the "0" and "1-6" bit ADCs. The outputs from the "0" and "1-6" bit ADCs are in Gray code. The "0", "1-6", and sign bit are applied in parallel to the prememory.

At the prememory, the data experiences its first clocking. On the prememory the data is time multiplexed eight ways. Data from the prememory is clocked to the post memory by a four of eight ring counter.

On the post memory data is clocked into data cells MT0-MT7. Each data cell is 8 bits by 256 words, giving a total of 2048 words of storage.

The outputs of the eight memory cells are coupled to the inputs of an Output Buffer. The output from the buffer being converted back to binary is clocked at 0.5 µs (display rate) to the D/A converter.

At the D/A converter the binary representation of the waveform is converted to an analog value that is outputted as Y-out and P-out as selected via Front Panel controls.

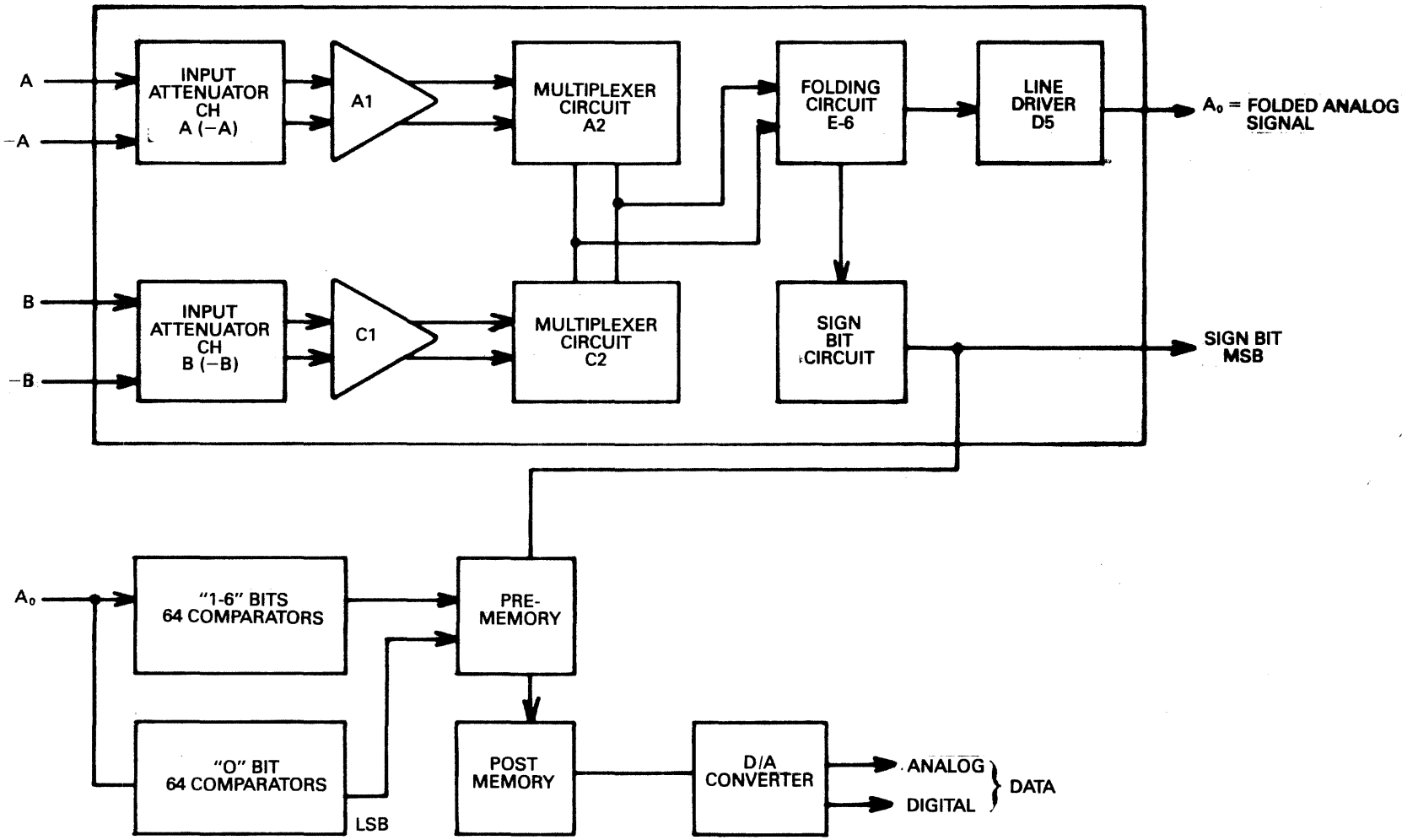


Figure 7.1 Analog Data Flow

Digital representation of recorded data is available by selecting the Output mode of the 8100. It passes through the D/A via a Data Selector and appears at connector J1 as D0-D7.

7.3 Internal/External Program Functions

Refer to Figure 7.2

7.3.1

The 8100 is capable of being externally programmed by a digital computer. To facilitate this function, the controls have been divided into groups. These groups are: TRIGGER Control Group, ARM Control Group, CHAN B Group, CHAN A Group, and the TIME BASE Group. To accomplish the programming function, a series of timing signals are used in conjunction with the 8 "operand" (see Section 5.5) bits to set data in a series of latches that control the operation and functions of the 8100. When the unit is not under program control, a 1 ms time base is used to set up the control timing signals to the front panel. The two control functions are called the "S-G" Group and the "I-F" Group. Both of these functions are decoded from the "operator" inputs under external control. The first instruction that must be given to the 8100 under external control is a "set program mask" command. This determines which control group(s) will be under external control and which will remain under internal (front panel) control. When a control group has been set to external control, the timing signals from the front panel are no longer operative, but the word command (CMD) is used to clock that data into the latches. The S-G signals and the I-F signals (in the form of "I-G" signals) are logically combined as a function of the "set program mask" instruction by the front panel circuitry to provide the timing pulses to the individual selector switches. The S-G and I-F signals are gated and used as the clock inputs of the individual latches to clock the data into the latch registers.

7.4 Control Functions

7.4.1 Time Base

Refer to Figure 7.3

The Time Base for the 8100 is a 100 MHz crystal oscillator followed by a series of seven synchronous divide-by-10 counters. There are two control latches associated with selecting the Time Base output rate. One is referred to as the "Main Time Base" (MTB), the other is referred to as the "Alternate Time Base" (ATB). These latches are used to store the two sample intervals used in the Dual Time Base mode of operation. A switch is used to determine which time base will control the sample interval output. Several other rates are used throughout the 8100 and are fed directly from the time base output.

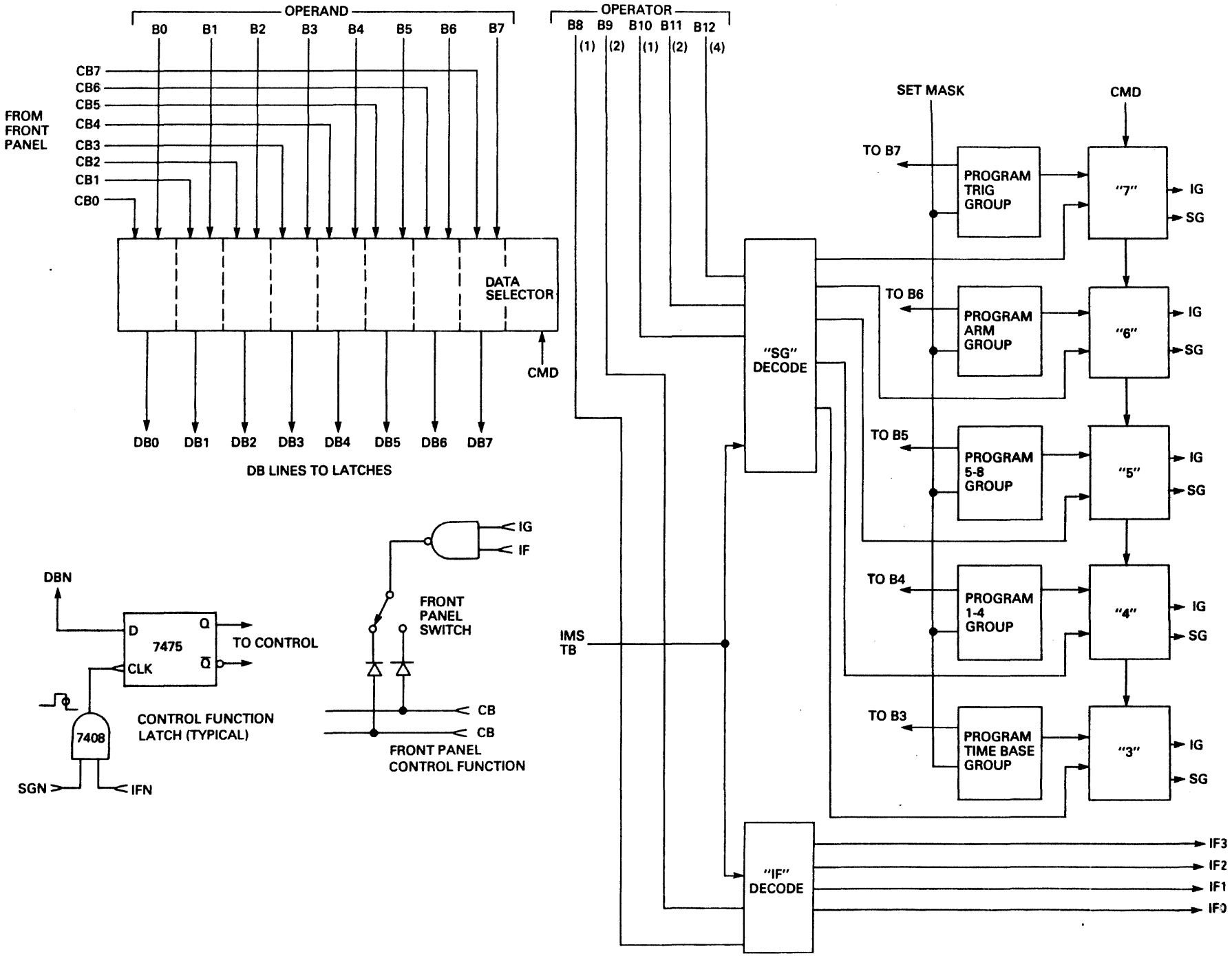


Figure 7.2 Front Panel/External Programming Functions

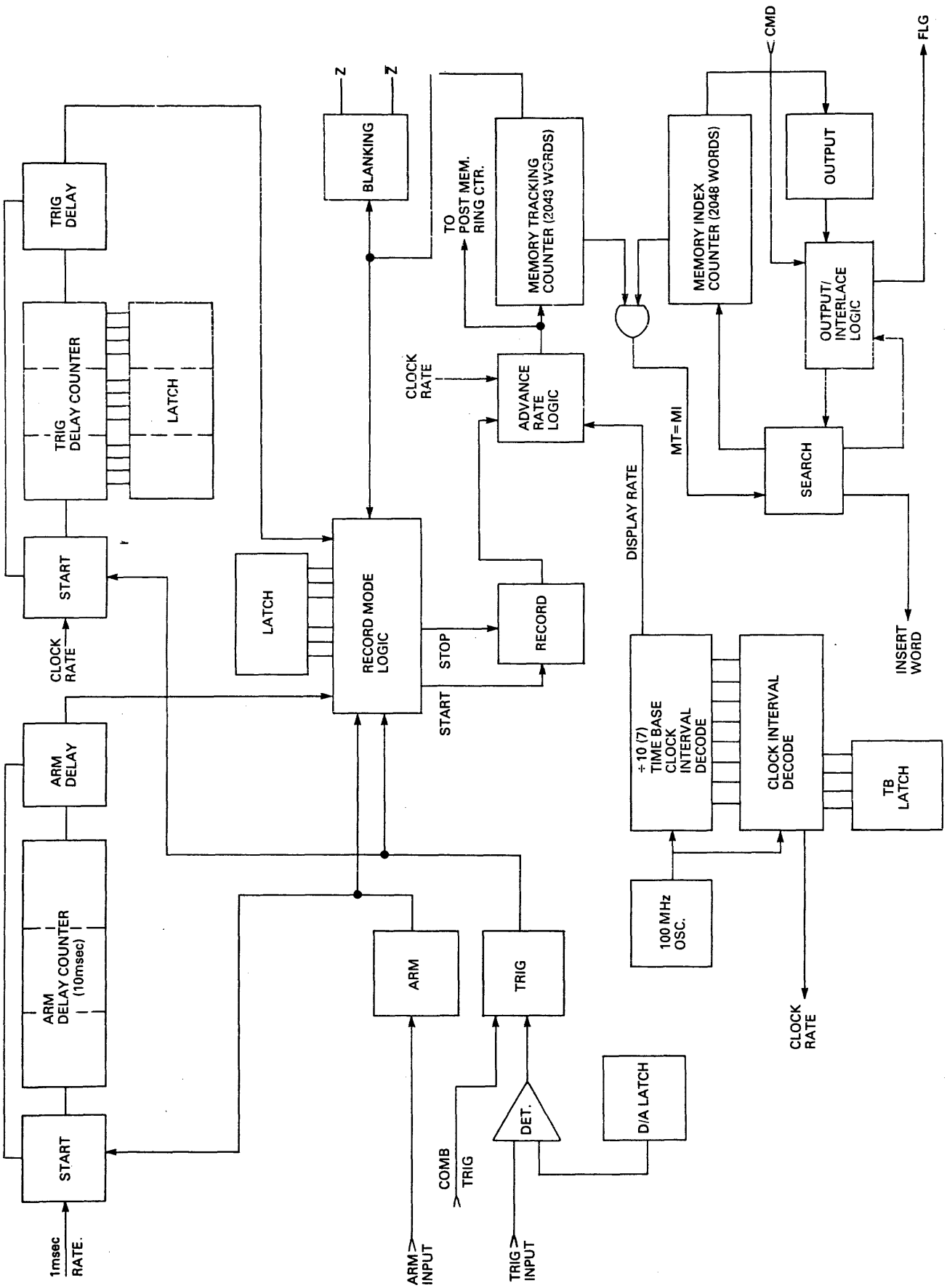


Figure 7.3 Control Functions Block Diagram

7.4.2 Memory Counters

There are two counters associated with the memory tracking operation, each is a 2048 word counter. One is labeled "memory tracking," the second is labeled "memory index." The memory tracking counter is constantly in step with the ring counter located on the post-memory. The roll-over of this counter is used to determine the blanking outputs. The memory index counter is used during interlace recording (Sample Interval 0.5 ms) to count the number of revolutions of the memory tracking counter. There is a series of gates between the two counters to determine coincidence. When both counters are equal, a new word is inserted into the memory board during interlace. A similar operation occurs during the output when the word command rate is less than 10 kHz.

7.4.3 Record Functions

Refer to Figure 7.4.

Consider what occurs within the 8100 when data is recorded and then displayed. In the Normal mode of operation, the instrument is ARMED. With ARM delay set to 0.00, 10 sample intervals after receipt of ARM, the instrument can accept a TRIGGER signal. The start of record is also delayed by a minimum delay of 10 sample intervals from receipt of TRIGGER. Recording will continue until all of the 2048 words of memory have been filled with new data. Recording will then stop.

The TRIGGER circuits located on the front panel circuit board are used to detect a Triggering event from an external or internal source. Following each Trigger coupling network is a trigger detector discriminator. This discriminator compares the DC trigger level output from the trigger level D to A converter with the input signal to give an output trigger pulse when the trigger input level exceeds the reference level. This trigger pulse is input to the trigger delay circuit. The trigger delay circuit consists of a series of presettable count-down counters. If the delay has been set to 0.00, a minimum delay of 10 sample intervals will occur before the trigger pulse is directed to the record logic. See P. 65B. The trigger pulse will be coupled through the "start" line and initiate the recording cycle. During the recording cycle, data will be stored in the memory at a word (sample) rate determined by the sample interval control or external Time Base Input. When all 2048 words of memory have been stored, a roll-over pulse is received from the memory tracking counter and the "STOP" or End-of-Sweep (EOS) command is initiated.

In the Pretrigger Record mode of operation, the ARM signal initates the ARM Delay. Here again, presettable count-down counters are used to control the amount of delay. If the delay has been set to 0.00, a minimum delay of 10 sample intervals will occur, and the ARM signal will start a recording cycle. As soon as a trigger signal has been received the trigger signal will start the trigger delay circuit. If a trigger delay is selected, logic will be initialized and recording will end. Again, with a delay of 0.00, the minimum trigger delay is 10 sample intervals.

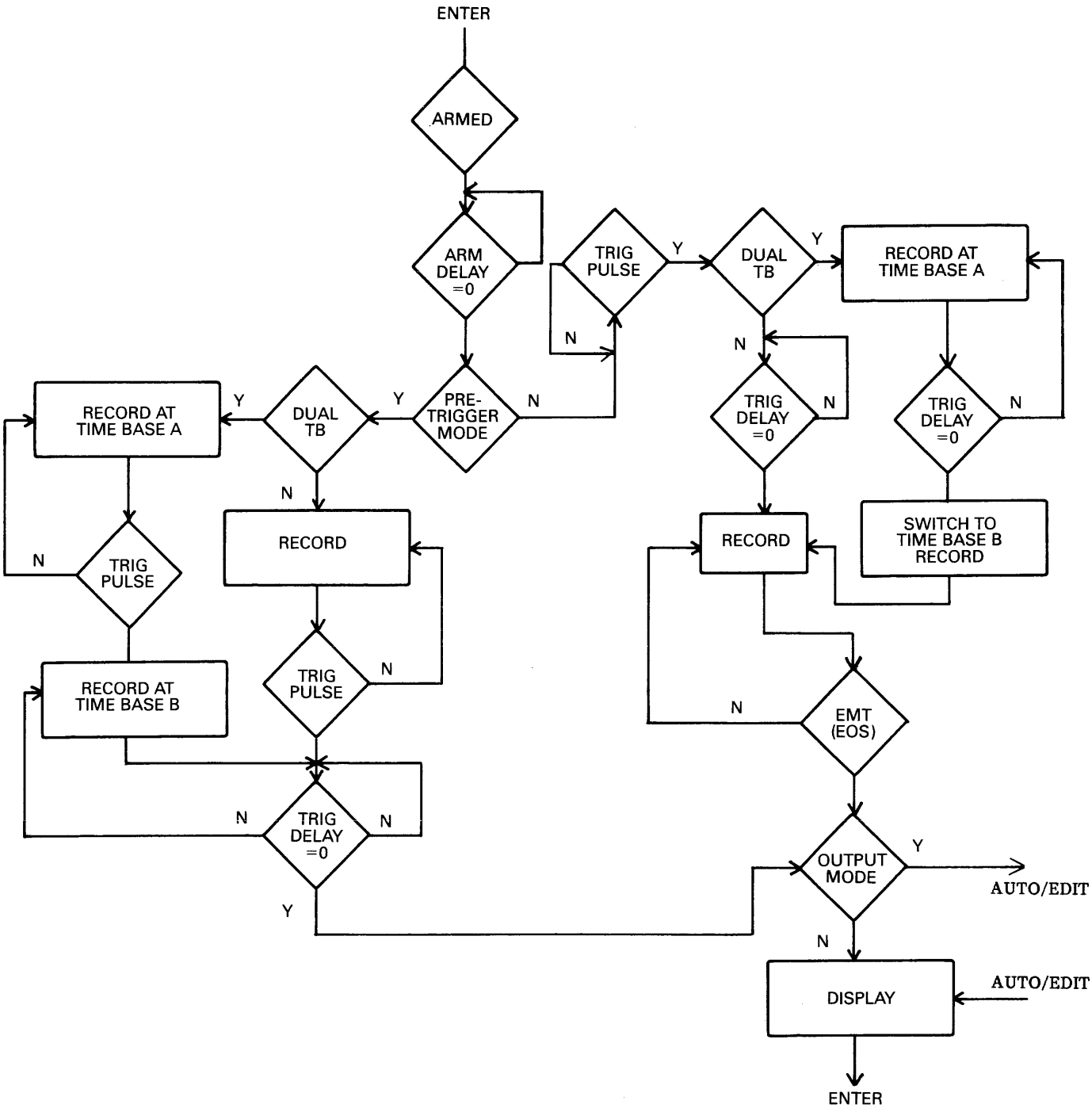


Figure 7.4 Record Function Flow Chart

In the Dual Time Base mode of operation, which is available with either the Normal or Pretrigger record mode, a "change" signal is sent to the "alternate time base control" and the sample interval will be changed to the rate stored in the alternate time base control latch at the time of the occurrence of the Trigger or Trigger delay depending on the record mode selected (NORM or PRETRIG), see Section III.

7.5 Circuit Description

The following subsections comprise the technical description of the 8100 using a board-by-board approach. Refer to each respective board schematic for reference during the description.

7.5.1 Front Panel

The Front Panel provides control of the various operating modes of the instrument by providing external switches and push buttons that enable the user to control internal circuit functions, thereby controlling the different operating modes.

There are six major areas of circuitry that will be described. These areas are: Switch Decode Logic, Internal Trigger Circuit, Arm Logic, Trigger Logic, Control Group Latch Logic, and Offscale Indicator Logic.

Switch Decode Logic (SDL) along with other logic to be discussed, make it possible to control the operation of the instrument by the switches available on the Front Panel or by computer control. This capability is implemented by making the switch logic programmable. Whether control is by front panel switches or by computer control the internal commands generated are the result of internal programmed commands, SG, IF, and DB.

SDL is found at the top portion of the Front Panel schematic, Figure 9.3. Programming of the various switches is accomplished by placing the wiper of each switch in series with a NAND gate. Each of the gates driving a particular control wiper has for its input one IF signal and one IG signal. The switch contacts are connected to diode cathodes, which in turn are "OR" tied to the CB lines, eight in total.

For example S17, which controls the Output Group (Front Panel Control), is strobed on IF2 and IG3. The output CB0 or CB1 will be low depending on which mode, Auto or Edit is selected. The CB lines go over to the I/O board through a data selector/multiplexer and becomes DB0-DB7, which will be discussed shortly.

Internal Trigger Circuit

The Internal Trigger Circuit produces basically a reconstruction of the input signal. The output from the Internal Trigger circuit provides stimulus for the ARM and Trigger circuits, as selected via Front Panel/Computer control.

Q2 and related circuitry at the left-hand edge, middle portion of that edge make up the Internal Trigger Circuit.

The folded version of the input signal comes into the ITC as In=(A out Input Amplifier). Also, the sign bit appears at the base of Q1. When the Sign bit is high representing the negative excursion of the input signal, Q1 conducts,grounding the collector of Q2. Q2 then functions as an emitter follower. Q2's output follows the input signal at its base. This signal goes through Q4 and Q5, which are complementary emitter followers, and appears at Q5-E as a negative-going signal. When the input signal at the Input Amplifier goes positive, the Sign bit goes low. Q1 turns off allowing Q2 to function as a rectifier. Again Q2's base follows the **input** signal. Q2's collector voltage rises as a result of Q2's base being reversed biased by the input (In) signal. Q3 conducts and its emitter goes positive. The summing junction at R27/R25 see's a greater positive value than negative value. Q4's base is reversed biased and the voltage at Q4-E goes positive. Q5-B becomes forward biased and Q5-E goes high thereby reconstructing the folded analog signal appearing as Ao (In) from the Input Amplifier. The "I" pot provides offset compensation for the output signal; the level pot R21 controls the input signal level to Q2; the "O" functions as R21 for Q3, the "G" pot adjusts the gain of Q2 when it operates as a rectifier.

Arm Logic

There are two Arm modes available, the Auto mode and the Input mode. If the unit is in the Auto mode, arming occurs Automatically when the Arm ready condition occurs at the end of each display cycle of 2048 words. Internal, manual, and external arming capabilities are disabled in the Auto mode. If the unit is in the Input mode arming can be accomplished by the arm push button on the front panel, or placing the source switch in the external position and apply an external arming signal to either the 5 V or 50 V BNC inputs on the Front Panel. In addition, the arm can be programmed through the I/O Interface.

On the schematic, Arm logic is located directly below the SDL. In the Auto mode the unit is armed each time ARY goes high as evidenced by the Arm Ready Lamp being lit. When ARY goes low the unit has been armed and the Arm Ready lamp will go out. When ARY is high B7 is preset via gate B8-12. B7 functions as a 50-ns one-shot. The output of B7 drives Q6 an emitter follower, producing ARP that initiates the arm function.

In the Input mode and with the Source set to internal, the unit will arm on the input signal. Preliminary arming conditions are established by setting the Internal CH A/CH B, slope +/-, and coupling DC/AC to the desired position. If the Internal CH A position, positive slope, and DC coupling has been selected, arming will occur in the following manner: the input signal will be coupled through K3 and K1 into comparator B4-3. When the input signal exceeds the reference level at B4-2=ALV as set by the level switch,

the output of B4-7 will go low. B5-3 will then go high causing B7 to be preset. With ARY high, the low-to-high transition at B7-11 produces a pulse at Q6 (ARP). If dual channel operation is selected, ICP clocks B7. CR122, 123, limits the input signal swing ± 3V.

When the source is set to external, the unit can be armed manually. When the ARM button is pressed (S13) a pulse is produced from A4 (set-reset flip-flop). The output from A4-12 NANDED with ARY (high) a low pulse is produced at A4-8 that presets B7 producing ARP.

Arm Logic

External Arming is implemented by connecting the signal source to either the 5 V or 50 V BNC(50 Ω)inputs. Explanations for external arming are essentially the same as for internal arming.

Trigger Logic

The Trigger Logic circuit analysis is the same as the Arm Logic description.

Control Group Latch Logic

Control Group Latch Logic (CGLL) is located beneath the Trigger Group Logic. CGLL is made up of D4, D5, D6, and associated components. The Arm and Trigger Group functions are controlled by the CGLL. The Arm and Trigger Group Switch positions are decoded and received by the CGLL as DB3-DB7. Data is latched on SG6 and SG7.

For example the ARM Source Internal/External mode is controlled by D4-9,8. If the Arm Group Source Switch is in the Internal position, DB5 will be pulsed low. On SG6 high to low, the low level will be latched. D4-9 will be low and K3 will close enabling the internal trigger signal to Arm the unit. In a like manner K1, K4, K2, K5, and K6 are energized.

Offscale Indicator Logic

The Offscale Indicator Logic (OSIL) is located in the lower left hand portion of the schematic. OSIL indicates the channel and direction of offset.

Comparator A32 on the "1-6" bit ADC provides ALI, which when high represents an offscale occurrence of the input signal. Direction (+/-) of the offset is determined by the sign bit ($\overline{SIN}$). INA and INB indicate when high, which channel is being used as the input. Otherwise, if either one is low, it disables its corresponding latch.

For example, if CH A is ON and CH B is OFF, and the input signal exceeds the input range limit, ALI will go high. If the input signal exceeds the range in the positive direction, the Sign bit will be high ($\overline{SIN}$). A low will be present at D1-12 and a high

present at D1-2. On SSI (Ø2), which is a two phase synchronized clock, D1-5 will go high and D1-9 low. As a result, the (+) offscale indicator LD2 will be on. CH B offscale indicators will be disabled as a result of highs being at their cathodes.

The offscale indication monitored represents the first offscale occurrence during that record. The OSIL will remain in that state until cleared by $\overline{\text{RIL}}$ (another Arm condition) or by an external program command to clear and update status.

7.5.2 Input Amplifier

The Input Amplifier has two major sections, the Input Attenuator and the Amplifier Circuitry.

The Input signal is coupled from the front panel BNC connectors to the input coupling network. This network, using relays, determines which type of coupling, AC or DC, will be used. Following the input coupling networks, the signal goes to the input attenuator which has a 50 ohm input impedance. Here again relays are used in determining the amount of attenuation selected by the range control. There are two identical attenuators, one for the "noninverting" input, and one for the "inverting" input. The outputs of the attenuators are DC coupled to the differential inputs of a fixed gain video amplifier. The offset voltage is also coupled to the inputs of the video amplifier. CR30-33 clamp the input signal swing to $\pm$6.2 V.

A3 (C3) and Q1 are constant current sources for A2 (C2) and E6 respectively. A3 is connected in such a manner as to provide temperature compensation for itself thereby regulating the current to A2 (C2). Q1 primarily functions as a constant current source. At the same time D4 (comparator) produces level changes at the zero cross-over point of the input waveform. Therefore, on the positive half, D4-6 will be on and the Sign bit out will be high. On the negative portion of the input signal, D4-5 will be on and the Sign bit out will be low. The Sign bit experiences level changes between 0.8 - 2.0 V.

When the input signal goes positive, A1-7 follows and A1-6 complements. As result, the collectors of A2 are out of phase (180^{o}). When A2-6 goes low, E6-1 goes high, and the emitter of E6 goes negative. When A2-5 starts negative the collector starts positive, at the same time A2-1, 2 are going just the opposite. The emitter of E6 starts and reaches $\sim$ 0 V before it is pulled back negative by E6-5 going negative. As a result, the positive and negative portions of the input waveform are folded and seen at the emitter of E6 as a folded version of the input signal.

CH A and CH B circuitry are duplicated up to multiplexing circuit A2 (C2). For single channel operation either A2 or C2 will operate. In the Dual Channel mode A2 and C2 will operate alternately as clocked by ICP and $\overline{\text{ICP}}$.

The folding amplifier output is fed to D5 (line driver) that provides the input to the "0" Bit and "1-6" Bit analog to digital converters via buffers BF1-BF8 on the Mother Board. The folding amplifier can also be called a "full-wave rectifying" amplifier and provides the most significant or "sign" bit of the A/D converter as well as reduces the dynamic range requirement for the remainder of the conversion by a factor of two.

7.5.3 "0", "1-6" Bit ADC

The analog-to-digital converter used in the Model 8100 is a "simultaneous sample and conversion" or "parallel comparator" type with 128 discriminators (comparators) used to convert the "folded analog signal to gray code digital information. This is accomplished on two separate printed circuit boards. The "0" bit board generates 64 of the total 128 transitions and this is the least significant or "0" bit. The 1 to 6 bit converter card generates 63 bits of digital information, and the seventh bit , or most significant bit, is generated on the input amplifier in the "folding" process as mentioned above. These 8 bits of digital information are applied in parallel to the input buffer section of the memory board in gray code.

To simplify the discussion of the ADC used in the 8100, an analogy will be made utilizing a 3-bit parallel converter. Keep in mind that the comparator outputs in the 8100 are "wired ORed" to provide digital data in a Gray code format. The 3-bit converter presented in the following discussion uses NOR gates to represent the "wired ORed" function. Folding the input signal and using the sign bit to define the positive and negative portions of the waveform reduces the over all range of the ADC (8100) by half. This concept will not be used in the following analogy, but should be kept in mind to better understand the 8100 ADC.

Parallel ADC

Figure 7.5 shows a parallel 3-bit converter with Gray code output. It has $2^n - 1$ comparators, biased 1 LSB apart. For an input level more negative than point 1, the output from the "OR" gates will be "000". See Figure 7.6 as it shows the Gray code output from the converter. As the input increases the comparators sequentially change states. The manner in which the reference inputs on the comparators are connected determine whether the output of the comparators will be high or low when the input level is more negative than point 1.

The comparator A/D converter is capable of great speed because the entire conversion process occurs simultaneously rather than sequentially. Immediately on presentation of the analog input voltage and after a short delay in the comparators, a digital representation of the analog voltage is available.

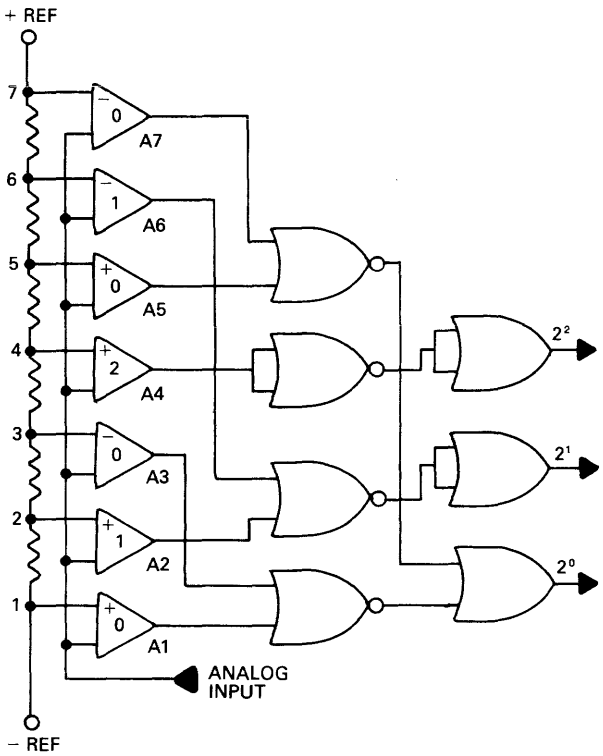


Figure 7.5

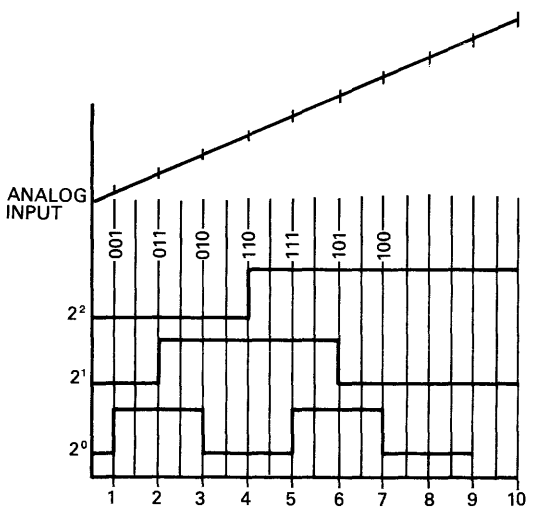


Figure 7.6

Figure 7.7 shows the basic comparator minus the frequency stabilization resistors in the base circuit of the transistors. Figure 7.8 depicts the state of Q1 through Q4 and the resultant output of Q5 during the input level swing. The two diodes clamp the signal swing seen on the base of Q5 (emitter follower). Q6 and 7 are current sources. Their current drive is regulated by the "ER" voltage applied to their bases.

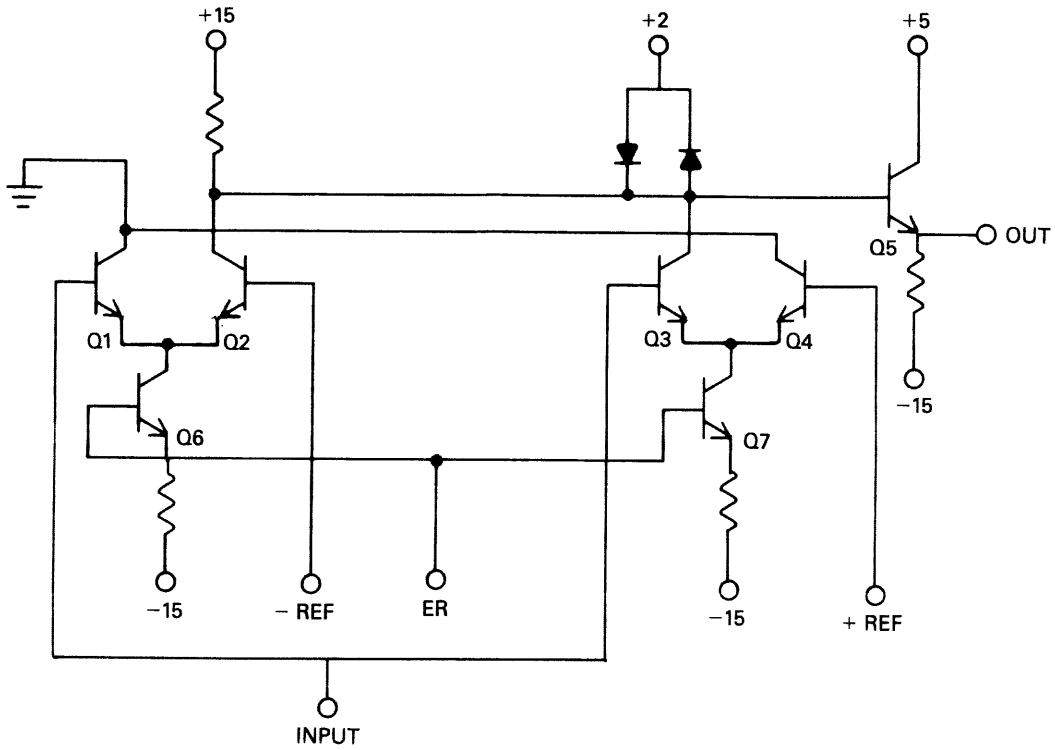


Figure 7.7

INPUT	Q1	Q2	Q3	Q4	Q5
<− Ref	Off	On	Off	On	Low
>− Ref <+ Ref	On	Off	Off	On	High
>+ Ref	On	Off	On	Off	Low

Figure 7.8

When the input level is more negative than the -Ref threshold, Q1 is off, Q2 is on with its collector at a low potential. The output of Q5 is low. When the input level exceeds the -Ref level (becomes less negative) Q1 is on, Q2 is off with its collector at a high potential. Q5 will now have a high output. Q3 during this time will be off, and Q4 will be on. This condition remains until the input level crosses the +Ref threshold. When the input level crosses the +Ref level Q3 conducts, its collector goes to a low potential, the output of Q5 goes low, and Q4 is off. When the input level becomes less positive than the +Ref level Q3 is off, its collector goes high, the output of Q5 goes high, and Q4 is on. When the input level crosses the -Ref level Q3 and Q4 remain in their last state, Q2 is on, its collector goes to a low potential, the output of Q5 goes low and Q1 is off.

The output of the ADC in Gray code represents the analog input signal as it changes from its most negative level to its most positive level. Wire "ORing" more comparators together and constructing the logic to provide more bits out enhances the resolution of the ADC without sacrificing speed. The number of elements increases geometrically with resolution. For a 4-bit converter, fifteen comparators are required with the respective logic to decode the comparator outputs.

The "1-6" bit ADC provides the ALI signal that indicates an over range condition. Comparator A32 supplies this signal.

7.5.4 Memory

The memory system is made up of two independent sections, the prememory and post memory. Prememory contains the converter reference logic, clock logic, input data latches, data transfer latches, and other control logic. The post memory contain the memory cells MT0-MT7, gray code to binary converter, output data buffer, and control logic.

D5 and D6 on the prememory provide temperature compensation regulation for the CA 3049 comparators on the ADC boards.

D6 is used as a differential line driver. Temperature compensation is implemented using D6 to track the temperature of E9, F10 (10124) chips on the prememory. If the threshold levels on the 10124s change due to a temperature shift, a similar change should also occur to D6. CB will be adjusted by D6 to maintain the correct threshold levels to assure correct transfer of data from the ADC's to the prememory PCB.

D5 is used in a similar fashion as D6 to regulate the "ER" reference voltage for the CA 3049 comparators on the ADC PCB's.

The prememory serves to multiplex the data being clocked as high as 100MHZ eight ways so that the memory chips only have to run at 1/8 of clock frequency.

Digital data from the ADCs is applied to the inputs at F10, E9 as DI0-DI7. The data at the inputs of F10, E9 is at T^2L levels. F10, E9 are T^2L to ECL translators. Data experiences its first clocking at F9, F8 latches on $\overline{TBS}$, which may be as fast as 100 MHZ. F8, E7 are ECL to T^2L translators. The $\overline{TBS}$ clock is steered through delay lines consisting of C3 and D4 to allow proper set up and hold times for the clock/data relationship. $\overline{TBS}$ clocks E2, E1 which provides symmetrical square wave output in 4 different phases (Ø1-Ø4). Ø1-Ø4 clock F7/E6, F6/E5, F5/E4, and F4/E5, respectively.

Ø1-Ø4 also clocks the 4 of 8 counter F2, F3 that clocks data over to the post memory and clocks MT0-MT7. The clock out from F3 and F2 is delayed through B6, B5, B4 and associated circuitry to allow the data at the D inputs of the 2802 memory cells on the Post Memory to hold beyond the corresponding clock pulse to the 2802.

The MCP Counter provides two functions; it forces E2 to clock in a walking ring counter mode, and it provides the ICP, $\overline{ICP}$ signals that switches the multiplexers on the input amplifier off and on in dual channel operation.

The post memory is divided into eight cells indicated by MT0 through MT7 on the schematic. An inset at the very right-hand edge of the schematic drawing shows detailed schematic of each block. The upper box R74 is a data selector that selects either the outputs of the memory M74 or the inputs coming from the prememory. During the time that the instrument is in the display mode, the contents of memory are recirculated from its output to its input via R74. The 1402/2802 memory is a 4 X 256 word dynamic shift register with a two-phase clock. It should be noted that DB7-DB4 are stored in the upper memory cell, and DB3-DB0 are stored in the lower memory cell. The circuitry in between the two cells is a control logic and clock generation circuitry. Flip-flop OCC is operated in two different modes of operation. During display a clock rate of 2 MHz is applied to the clock input pin 3 and the D inputs. The Q outputs of each successive flip-flop are interconnected to make a 1 of 8 shift register. Flip-flop MCP is connected in a divide by two configuration to provide the two-phase clock necessary for the dynamic shift registers. MCO, which is an NH0013, is a clock driver that is capacitively coupled to the 74H40 outputs. A clock output is also provided by the 74S00 to give an enable pulse to the 7403 open collector"NAND"gates.

Now let us consider what occurs in the memory during the record operation. As you will remember, prememory is operating continuously at all times when the instrument is on and is being clocked at the clock interval rate set on the front panel. Each of the eight groups of premememories is being clocked 1/8 of this rate. When the control logic indicates that a record of new data is to be taken, the following occurs in the postmemory.

First, the data selectors change from looking at the output of the postmemory 1402/2802 and switch to the position of looking at the outputs of the prememory. In addition, pin 5 of the 74S00

goes to a high state, now allowing the clock coming from the prememory to pulse through the preset input of 74S74. Line C, the clear input to all of the 74S74's, is held in a clear state so that now the 74S74 is literally jammed into a set and reset condition by the prememory clock. Each time this occurs, a level change occurs at the outputs of MCP, which produces the clock for the memory. Adequate delays have been included to provide for correct set-up and hold time of the data into the 1402/2802 memory. Once the control logic indicates that all words have been stored in memory, a pulse is produced by the control logic, which is input to the prememory clock driver through the IBH line. The IBH line momentarily shuts off the time base clock to the prememory 4 of 8 ring counter. This stops the prememory clock and the postmemory clock. During this time, the postmemory data selectors are switched from the prememory inputs to look again at the postmemory outputs, and the 74S74 ring counters OCC's then begin to count in a 1 of 8 sequence.

The data is then demultiplexed one word at a time from each of the 7403 NAND gates and is applied to the data input of the output buffer latches OB0 through OB7. A clock is provided at a 0.5-μs rate during normal display, and the data is output to the D/A converter. During times when interlace record mode is being used, the data continues to recirculate through the memory while we are in the record mode. However, when coincidence occurs between the memory tracking counter and the memory index counter, an insert pulse labeled INS on the schematic momentarily shifts the inputs of the data selectors to look at the output of the prememory and stores this new word into the 1402/2802 postmemory. Diodes CR17, 18, 19 and 20 and 74S00A1 ensure that the postmemory ring counter always counts in a 1 of 8 sequence.

7.5.5 Time Base

The time base contains the oscillator and the divide by 10 chains, arm delay circuit, the trigger delay circuit, the record mode logic, and the memory tracking counters.

In the lower left hand portion of the schematic is the time base logic. Crystal Y1 supplies 100 MHZ to AA1, which then divides by 10; providing 10 MHZ to clock the divide by 10 chain. Gate A2 and A3 provide steering for the various time base intervals as enabled by gates A4, B4, C4 and D9. These gates are selected by D4, D6, and D7 as they decode the front panel sample time base switch data that is fed through MTB, ATB, C15, C9, and C12. AA2 is a BCD decade counter. When the sample interval switch is in the 0.05, 0.5, or 5 position AA2 functions as a divide by five counter.

Gates B8, C8, D5, B10, B12, B13 and A12 in conjunction with C15 and C12 determine the interval multiplier; i.e, microsecond, millisecond, seconds etc. position. C6 in combination with the time base logic and control logic operates as a divide by two and divide by five counter. During a normal record sequence (not interlace) C6 is disabled and $\overline{\text{ICL}}$ is a static high. When EOR occurs, C6 is allowed to count and provides a 2MHZ (0.5ms) display

clock (ICL). During interlace C6-6 will be low enabling C6 to count. F1-8 will be 2 MHZ or 5MHz depending on the time base sample interval rate $\overline{ICL}$, therefore, will clock D2, which represents the LSB for the MTC. $\overline{MCH}$ provides a means of synchronizing the MTC and memory during the output mode. When a command is received to output data, $\overline{MCH}$ will go high to enable the MTC on the next ICL clock. CHS will be high if not in dual channel. If in dual channel, CHS will toggle at the 1 of 8 ring counter rate (Post Memory) and control the MTC count Mode, thereby keeping track of which channel is outputting data. C5 is a divide by 10 counter and supplies a 10ms plot clock. By option a jumper can be wired to clock C5 with a 10ms clock causing the plot clock to be 100 ms.

The Arm Delay Logic is located in the upper left hand portion of the schematic. ARP via F12 presets B14 (ARD). Prior to being preset ARD's Q output low enables D10, D12, D14, which are decade up/down counters, to be loaded. Loading is accomplished using D11, D13, and D15 latches that monitor the DB0-DB7 lines. On IF0 and SG6 the LSB of the arm delay switch setting is latched, and on IF1 and SG6 and MSB is latched. When B14 (ARD) is preset, what ever arm delay value was present at the record event. ARD's Q output enables AA3 clocked at the time base sample interval rate to count. Its output pulses the count down input of D10-4. The borrow output of D14-13 resets ARD indicating the end of arm delay.

The arm pulse and delayed arm pulse are used in the record mode logic and goes over to the I/O PCB to produce a TRY pulse that initiates a trigger delay sequence.

Circuit description for the trigger group is the same as for the Arm group.

Record mode logic can be best explained in terms of record cycle. Refer to Figure 7.9 (truth table for correct outputs from the latches storing the record mode logic).

		B15						B16											
		PTR			PTR DTB			DTB OFF			DTB OFF			PTR OFF			PTR OFF		
		$\overline{Q}$		Q	$\overline{Q}$		Q	$\overline{Q}$		Q	$\overline{Q}$		Q	$\overline{Q}$		Q	$\overline{Q}$		Q
OFF	OFF	1		16	14		15	11		10	8		9	14		15	1		16
PTR	DTB	H		L	H		L	L		H	L		H	L		H	L		H
ON	OFF																		
PTR	DTB	L		H	L		H	L		H	L		H	H		L	H		L
OFF	ON																		
PTR	DTB	H		L	L		H	H		L	H		L	L		H	L		H
ON	ON																		
PTR	DTB	L		H	L		H	H		L	L		H	H		L	H		L

Figure 7.9 Record Mode Truth Table

Now let us consider what occurs during a typical record cycle in the normal record mode. Referring to the timing diagram shown in Figure 7.10, a start pulse is generated by the end of trigger delay and gated through the start gate to the preset input of the ESS and Record flip-flops. The Record flip-flop is then set producing a Beginning-of-Record "BOR" pulse. This also produces a "RMC" or Reset Memory Counter pulse. The Memory Tracking Counter then starts counting up from 0 until it reaches the count of 2048, at which point the end-of-memory tracking signal goes high, which is inverted by gate F11 and resets the Record flip-flop. At this time an additional RMC pulse is generated, resetting the memory tracking counter for the display cycle.

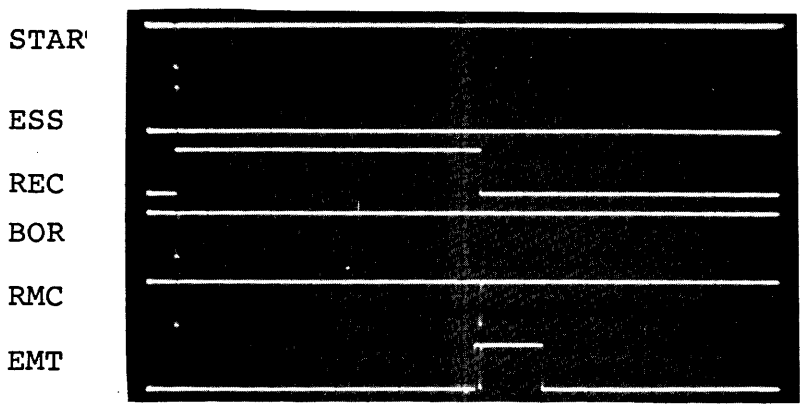


Figure 7.10

Now let us consider what occurs during a Pretrigger Record mode. Referring to Figure 7.11, again a start pulse is produced, but this time the start pulse originates at the beginning of the arm delay. This pulse is gated through the start gate and again presets the ESS and record flip-flops. This also produces a beginning of record pulse and a reset memory counter pulse. Recording now continues until the end of trigger delay, at which time a stop pulse is gated through the stop gate. This pulse resets the ESS flip-flop, which in turn resets the PTR flip-flop, which in turn resets the Record flip-flop. Again a RMC (Reset Memory Counter) pulse is generated to reset the Memory Tracking Counter. The unit then returns to display mode until another record cycle begins.

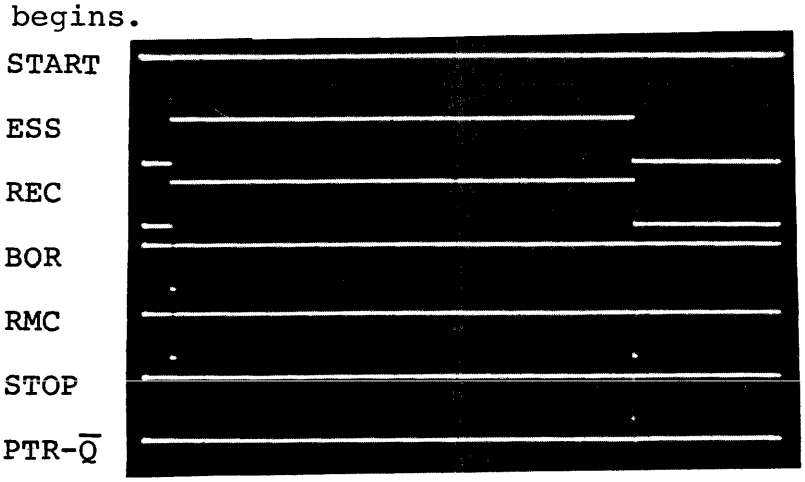


Figure 7.11

In Dual Time Base/Normal mode, recording is initiated by the trigger pulse at gate A13-8. Pressing set alternate interval prior to recording causes the sample interval set on the front panel to be latched in C13, and C14, on IF1 and SG3. When recording occurs on the trigger pulse data is sampled at the main time base rate, when the trigger delay pulse occurs, which can be a minimum of 10 sample intervals with a trigger delay of zero, a change pulse is produced at A14-8. The low-going pulse from C16-6 will cause the ATB (F15) to set on the positive clock edge. This high level causes the data selectors C12 and C15 to switch to their alternate inputs there by switching to the alternate interval rate.

Pretrigger and Dual Time Base is basically the same as Dual Time Base and Normal mode. The Arm pulse at gate A13-12 starts the record sequence. The trigger pulses initiates a change command via gate A14-6. STB, through gate A15-12 provides a means of changing the time base rate through computer interface.

At the beginning of record the MTC is cleared to zero representing the origin of memory. In the Normal Record mode, i.e, SI $<$.5ms, the MIC is not clocked. Recording terminates after 2048 words have been entered by EMT going high. To allow the logic to switch from the record mode to the display mode, the MTC on EOR is loaded to 2032. The display in memory begins to recirculate at the display rate-2MHZ. Since the MTC and MIC are not in coincidence MAC will be low as a result of F12-12, 13 being high. After the MTC counts to its terminal count, the next count will be zero. During this time the MIC is disabled by AMI being low. When MTC-MIC, MAC goes high enabling an output buffer clock, clocking the first to be displayed data out of memory and allowing AMI to go high, enabling the MIC to count on ICL. MTC and MIC count in sequence and MAC will be high.

During the Interlace Record mode, the MIC counter increments on AMI, which occurs when MTC-MIC, causing MAC to go high. Therefore, each revolution of the MTC + n is counted by the MIC counter. The same time that AMI occurs a new word is inserted into memory. When MTC $\neq$ MIC the memory is being recirculated.

7.5.6 Input/Output Board

The I/O board is the major control element in the 8100. All the inputs and outputs from the unit and its control functions originate on this board. The major logic blocks are the Arm/Trigger, Channel Select, IF/SG decode, Output Group, and Origin Logic.

During a record sequence in the Normal mode (not pretrigger) arming is disabled by keeping the ARH (arm hold) flip-flop reset. In the Display mode the MTC counts and its TC=EMT every 1024 words clocks ARH. At 2048 B9-9 goes high, and produces a ARY pulse. ARY initiates an arming sequence involving circuitry on the Front Panel PCB and the Time Base PCB. In the Auto mode, ARD occurs almost immediately after TRY. A minimum of 10 sample intervals later a DAP is produced that sets the Arm/Trigger flip-flop producing

a TRY pulse. If the 8100 is in dual channel and the SI is 0.01, 0.02, or 0.05 μs, $\overline{IMA}$ will be low. At gate A8-8 a low will be present disabling the ARH flip-flop and the trigger ready gate B14-8. Otherwise, TRY will initiate a triggering sequence involving the Front Panel and Time Base PCBs. TRD high will extinguish the trigger ready lamp lit when TRY went high, indicating a trigger event. DTP high resets the Arm/Trigger flip-flop and starts a record mode. REC high at gate B12-10, and $\overline{SES}$ high (not in Pretrigger) causes ARH to be cleared again disabling arming.

The arm trigger flip-flop is initialized by the reset generator to the arm ready condition after power-on. Also, if a programmed reset command is fed into the 8100, the flip-flop will return to the arm ready state. Because we have already mentioned it, let us take a look at the reset generator, which is located in the upper-right quadrant of the schematic and consists of gates B1 and divide by 10 counter C1. The signal coming from the connector labeled PON is the power-on reset signal. This signal reaches a high level only after about 1 or 2 s of power-up condition. Until this time, the reset outputs of B1 called RES are held to a low state. After the PON reaches potential of approximately 1.5 V, RES goes to its high state condition.

When a program reset command is received by the control logic, counter C1 is cleared bringing the carry output to a low level, which in turn allows the P input to be enabled, and the counter begins counting up at a 1-msec rate. After 10 counts, carry out goes high disabling the counter and also turning off the reset generator. Therefore, each time a program reset command is received, the reset line is held low for 10 ms.

Channel select logic is comprised of B13 and A10, which are latches. DB4 and DB5 are the inputs to B13. On IF2/SG4 and IF2/SG5 data is latched. Channel Mode as set on the Front Panel or programmed is decoded at B13 as INA, INB, or dual channel operation. In dual channel B10 (DMS) toggles at 1MHZ. Gated with ICL at gate C6-8 it produces a 1MHZ $\overline{IOC}$ to clock data out of the buffer on the post Memory PCB. A10 (DCS) in dual channel toggles at 1024 ms rate outputting DCS and $\overline{DCS}$ to switch the D/A logic from outputting channel A data to outputting channel B data.

The next section of I/O board that we wish to consider is the IF decode timing. The IF decode is accomplished by 74193 counter E8 and a two-line to four-line decoder 9321 D9 and its associated 7404 output drivers E10. Figure 7.12 shows the timing diagram for the clock input and the IF0 through IF3 timing phase.

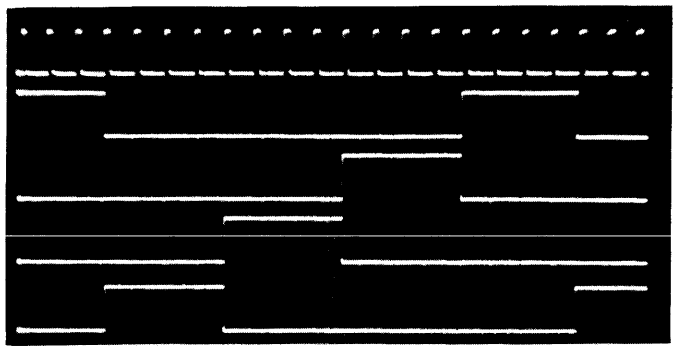


Figure 7.12 If Decode Timing

Just above the "IF" (Input Function) counters and decoders is another 74193 E7. This counter is used to decode the SG signal. In addition a 7442 BCD decoder is used to provide the SGD code. The SG signals are gated through the 74H11S, D13, and E12. Timing diagram Figure 7.13 shows the SG decode timing in relationship to the clock input. Both clocks have a 1-ms rate.

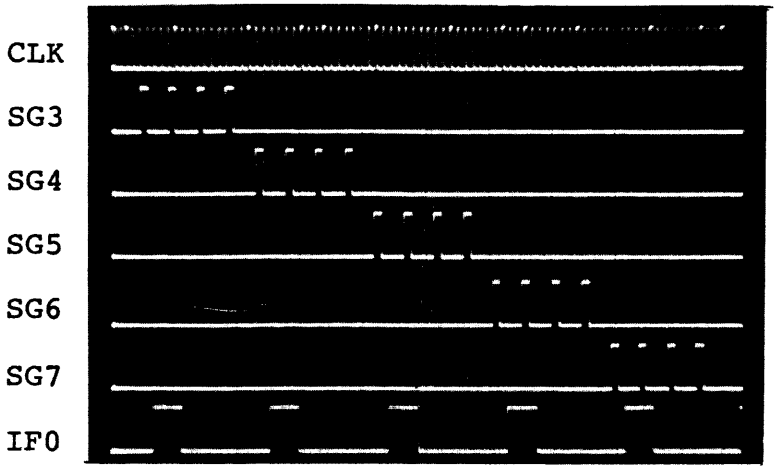


Figure 7.13 SG Decode Timing

The next area to consider in the timing relationship is the command and flag flip-flop and gating networks. Figure 7.14 shows the command flag timing. On the positive going edge of the command line a pulse is produced by "AND" gate D3. At the same time the positive going edge of the command pulse sets the command flip-flop and the flag is brought low. After the control circuit has acted upon the command pulse, the command flip-flop is reset and the flag is brought back up high again, indicating that data is ready or command has been received.

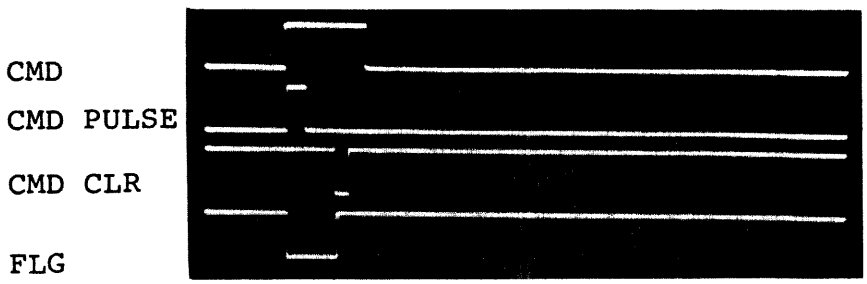


Figure 7.14 CMD/FLG Timing

Additional circuitry that is utilized in the remote programming front panel control are the data selectors E13 and E14 located at the bottom right portion of the I/O schematic. These data selectors select between the CB lines coming from the front panel and the B0 through B7 lines coming from the rear panel connector and direct this data onto the DB lines for the data inputs to all of the latches.

Figure 7.15 is a timing diagram representation of what occurs during a programming sequence. A command is issued to the 8100 and the flag responds. The command then switches the data selectors from the CB lines to the DB lines. In our example, DB0 has changed from a 1 to a 0 value during this time. Also gated through is an SG3 signal, and the IF2 line is high producing a latch clock pulse. The latch output changes state to the new value and retains that value until either it is reprogrammed or the front panel control is returned.

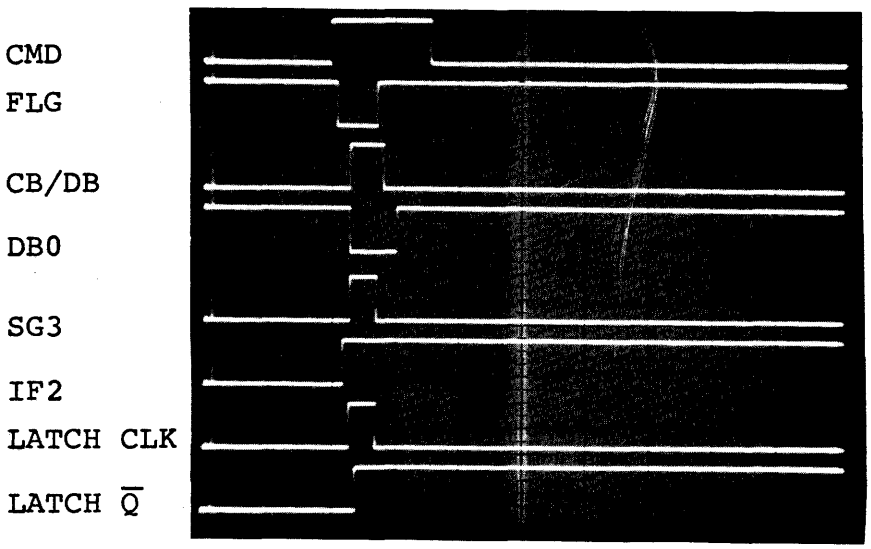


Figure 7.15 CMD/Program

The circuitry located in the upper left-hand quadrant of the I/O schematic diagram is primarily associated with the outputting of data in both noninterlace and interlace modes of operation and also with interlacing data into memory during the interlace record mode. This would be clock intervals of 0.5 ms or slower. Again, let us consider what occurs during an output mode using the timing diagram shown in Figure 7.16.

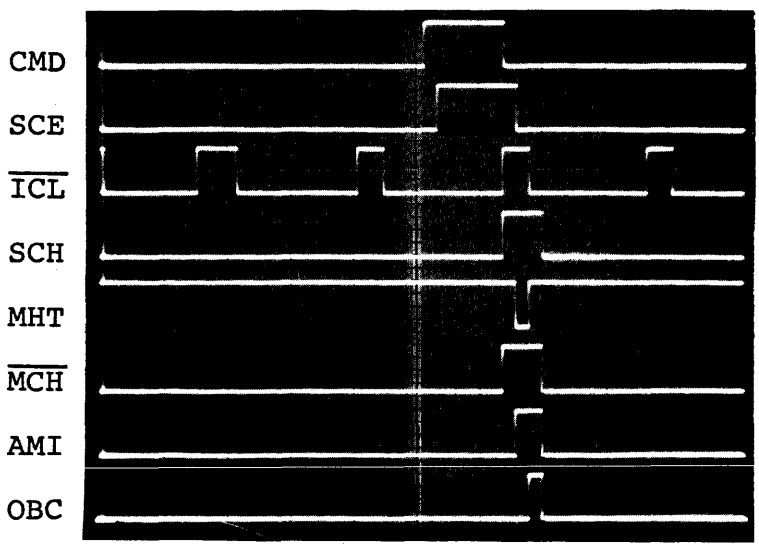


Figure 7.16 Output Mode Noninterlace

This will be for Noninterlace mode of operation; that is, command rates that are less than 100 s between commands. The command pulse is received and is gated through gate B4 to the clock input of flip-flop B5, which is the search enable flip-flop. This search enable flip-flop is then set, which in turn provides a logic 1 at the D input of the search flip-flop. At the next positive transition of the $\overline{ICL}$ clock, the search flip-flop will be set.This then clears the MHT flip-flop and produces a $\overline{MCH}$ pulse that advances the AMI counter and produces an output buffer clock. This condition is only true as long as two things occur: 1)the MAC (memory address coincidence) is always true and 2)the command occurs at a rate more frequent than 100 S.

Now let us consider the same circuitry using the timing diagram shown in Figure 7.17 in the interlace output mode. During interlace the time between commands will be greater than 170 s. A command pulse is received and the search enable flip-flop is set. At the next ICL clock the search flip-flop is set. When the memory tracking counter and the interlace index counter are equal, the MAC line will go high. Simultaneously, the MCH bar line will go low, producing an AMI pulse that advances the memory index counter. Also at this time, an Output Buffer Clock "OBC" pulse is produced, which then latches the next output word in the output buffer on the memory board.

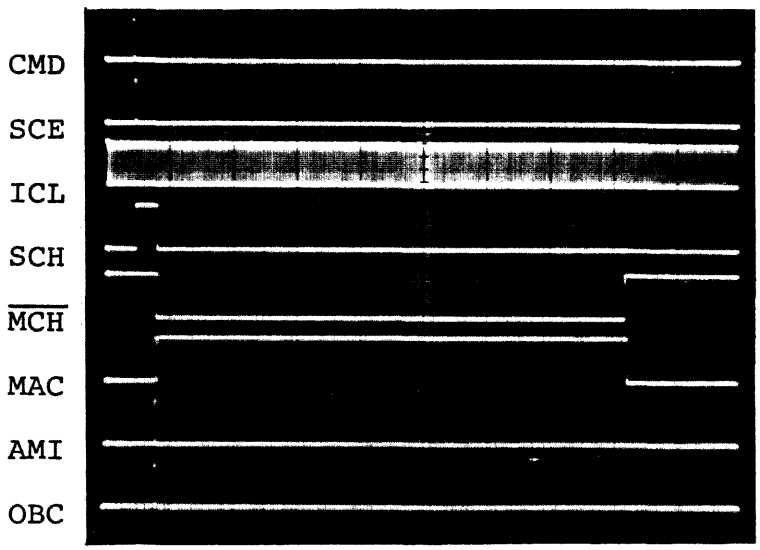


Figure 7.17 Output Mode Interlace

The OBC pulse resets the SCH flip-flop and sets the MHT flip-flop. $\overline{MCH}$ goes low and the memories halt, waiting for the next CMD pulse. CMD's $\geq$ 170 μs enable A5/A4 to reach the TC. On the next ICL clock MHT is reset and $\overline{MCH}$ goes high permitting the memories to refresh.

During the Interlace record mode of operation, the function of this circuit are very similar to the output mode interlace. However, during the record function an insert INS pulse is produced, which changes the data selectors on the memory board from the recirculate mode to the input mode, and a new word of data is stored in memory.

In the very upper left-hand corner of the schematic is the ORG origin flip-flop. This flip-flop uses the EMT End-of-Memory Tracking and the ICL clock to produce the origin pulses for use in generating the synchronous "X" rampand also for generating the Z and $\overline{Z}$ blanking signals.

During a Normal Record mode, the ORG flip-flop is preset by ICM going low on the on-set of record. Therefore, blanking occurs. POR-9 will be high from the Display mode, and the preset pulse as a result of EMT high at gate C10 performs no function at this time. A6 will function as a divide by 16 counter in the record mode. ICM low during record keeps the C0 of A6 low. The ORG flip-flop keeps itself jam preset. When REC goes low at the end of record blanking still exist. ICM high enables A6 to count at ORC = SI/¼. When Co goes high the jam preset condition of ORG is defeated and B6-9 is allowed to be clocked low on the next ICL clock. This allows time for the control logic to switch from the record mode to the display mode permitting correct display of data.

In the Interlace Record mode A6 functions as a divide by 9 counter and count enable is provided by POR. MAC high at gate D6-5 provides a high to the ORG control and on ICL causes POR to be low disabling A6 from counting. A6 is loaded to 7, waits for the load input and P enable input to go high on the next ICL clock. When A6-9 goes high blanking occurs at the same time a new word is being inserted into memory and the MIC advances. MAC goes low and on the next ICL POR enables A6 to count. Meanwhile ORG is jam preset.When A6=TC the ORG can clock enabling a display of data.

7.5.7 Digital-to-Analog Board

The D/A board encompasses the following circuits: the "Y"-D/A converter, Data Output Buffer, "X"-Ramp Generator, Power-on reset generator, and the Offset CHA/B, Arm/Trigger Level D/A converters.

Digital data from the memory is applied as OB0-OB7 to the Y-D/A.

In addition to the data inputs, there is also an analog input to the D/A converter via the vertical position control in the front panel. This DC level is applied to operational amplifier B1 and in turn coupled to the mode of the D/A converter. The D/A converter used is a current mode switching type. The output of this converter is coupled to the inverting input of operational amplifier A1 which is a CA3100. The gain of this amplifier is adjustable and provides the Y output gain adjustment. The output of this operational amplifier is coupled to the input of an LH0002 line driver. The output of the line driver is then connected to the BNC output connector via a resistor/divider network. The shield of the Y output BNC is returned to ground via a 10 Ω resistor R71. Any noise pickup in the shield is fed back through a resistor potentiometer labeled "VN", R68, to the noninverting input of the CA3100 operational amplifier. This is used to cancel

out any noise or stray pickup induced in the cable from the 8100 to the display device.

The x-ramp is generated from the ORG pulse, which is gated and shaped by gate D6. The output of this gate pin 11 drives the base of switching transistor Q3. Q1, which is a dual PNP transistor, provides a current source to capacitor C11 charges at a linear rate. At the next ORG pulse, transistor Q3 is turned on, discharing capacitor C11; resistor R62 provides a current limiting path for the discharge of the capacitor. The charge current is controlled by the HG potentiometer R58. This charge voltage is then coupled to the noninverting input of a 531T operational amplifier. The output of this amplifier is fed to a resistor network, which is used to provide the various expansion rates used on the 8100. Operational amplifier B2 provides a compensation for any stray pickup that in induced in the shield of the horizontal cable connected to the display. It has two adjustments, HNH and HNL.

There are three additional D/A converters found on the D/A board. These are all identical D/A converters. One is shown in the schematic diagram and the other two are shown in block diagram form. These again are current mode switching types of D/A converters.

The digital number selected by the front panel control of the most significant and least significant digits are stored by the input latches. These latches in turn enable the current switches and switch a proportional amount of current to the bit weight to a summing node, which in turn is connected to the inverting input of operational amplifier A5. An offset null circuit is provided at the noninverting input of A5. A gain adjustment is provided for the output of A5.

The second half of operational amplifier A5 is used in two ways, either as a noninverting unity gain operational amplifier or as an inverting adjustable gain operation amplifier, depending on the selection of the polarity switch on the front panel. The latch, which is driven by the polarity switch, enables the forward bias condition to occur on Q9, which in turn causes FET Q8 to go to a very low impedance, thus grounding the positive or noninverting input of operational amplifier A5.

The calibration signal is generated by C1 and C2, which divide ORC by 100. Pressing the CAL button disables the digital data to the Y-D/A and enables C1/C2 to count, outputting a square wave signal.

One additional circuit needs to be mentioned on the D/A board, and that is the power-on circuit. This circuit consists of two transistors, Q6 and Q7, that are used in the emitter/follower mode of operation and their associated circuitry. When the power is first turned on to the 8100 and the +5 V supply comes up, capacitor C19 starts charging coupled through the emitter of Q6 to resistor/

divider network R93, R94 and POT R95. Potentiometer R95 is set so that after 10 sec the output level at PON is +2.5 V.

7.5.8 Power Supply

The power supply used in the 8100 is a special design. It is called a "peak-clipped regulation" type power supply. Refer to the simplified block diagram and the schematic diagram for the power supply. The power transformer for the power supply is a special three-winding type consisting of a primary (energized by the AC line), multiple secondaries connected to the rectifiers and filtering elements, and a special feedback winding (so-called third phase) for control. The current in this control winding determines how much flux is coupled from the primary to the secondary. The +5 V, -5 V, and -10 V supplies are directly regulated in this manner. The ±15 V supplies have additional series regulators and control circuits.

Regulation of the main power supplies is accomplished by feeding back a proportional voltage from the +5 V output to control transistors Q3 and Q4. These transistors in turn drive transistors Q1 and Q2, which control the amount of base current provided to the MJ 3001 power Darlington transistors determining the current through the control winding. A thermal switch S1 provides for shutdown of the entire power supply if the heat sink exceeds a temperature of 95°C. This could only occur if the cooling system in the 8100 failed to operate and a malfunction occurred to cause excessive power dissipation.

The +5 V supply is also "current limited" in that should a dead short occur across the output grossly exceeding the normal output current of the supply, the power supply will shut down within one second after the short occurs. The -5 and -12 supplies have 0.1- resistors in series with their outputs. These resistors act as fuses if these supplies are shorted out, preventing extensive damage to the circuitry. The ±15 V power supplies employ common series regulator circuits with current limit feedback protection. The collectors of the series pass elements are at ground potential. The +15 power supply tracks the -15 power supply, providing stable voltages for the operational amplifiers used in the 8100. The output voltages and nominal current drains for each supply voltage under normal operating conditions are indicated in the table below.

Supply	Normal Volts	Current
+5 V	5.00 V 0.25 V Ripple	10.0 A
-5 V	5.80 V ±10%	2.0 A
-10 V	12.00 V ±10%	0.50 A
+15 V	15.00 V	0.26 A
-15 V	15.00 V	0.32 A

SECTION VIII

Maintenance

This section covers maintenance and disassembly procedures for troubleshooting and repair of the Model 8100. Troubleshooting is performed with the aid of a diagnostic procedure for the front panel controls and functions, and a diagnostic program for the digital control section. Both of these procedures provide sufficient detail to isolate a problem to the circuit board or module level.

A PC board exchange program has been set up with the factory for use by customers within the continental United States, and with regional service centers in foreign countries. In addition, waveform photographs have been included with the schematics to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800 TWX 910-338-0509 .

In summary, there are three methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Trace the problem to the defective PC board and obtain a replacement board from the factory, or service center.

3. Troubleshoot the problem to the component level with the aid of the diagnostic procedure and schematics or with the aid of factory personnel.

8.1 Diagnostic Procedure

The following test equipment will be required to conduct the diagnostic procedure:

1. A function generator capable of sine, triangle and square wave functions over the frequency range of 0.01 Hz to 1 MHz and with a variable output of up to 10 V peak-to-peak into a 25 ohm load, (two 50 ohm loads in parallel).

2. An oscilloscope: Two channel DC to 100 MHz input bandwidth.

If a display device is not normally used with the Model 8100,

an additional oscilloscope or CRT display will be required during the testing period. This latter oscilloscope need only have a 2 MHz input bandwidth.

Connect the display device to the 8100 per Figure 4.3, page 32. Turn on the equipment and allow them to stabilize for approximately 10 minutes. Before beginning the diagnostic procedure, the maintenance technician should read Sections III through VI of this manual. NOTE: All Section VIII Figures are on the foldout, page 110.

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
8.1.1 Display Group	
With the "CAL" button in, adjust the horizontal and vertical position controls for a full-scale output in both the X and the Y axis. (See Section 6.1 for the procedure.)	
No vertical deflection and/or no horizontal deflection.	Check front panel controls as follows: RECORD MODE: Both NORM/PRE-TRIG and DUAL TIME BASE buttons should be out. OUTPUT Group: OFF TIME BASE SOURCE INTERNAL, (Both out) CHAN A Group INPUT; CHAN B Group INPUT. Check power supplies, see Figure 9.26. Check all connections between 8100 and output device. Place D to A board on card extender. Check waveforms 1, 2, 3, and 4, (see D to A schematic). If waveform 1 is not present, place D to A board back down in unit and place I/O board on extender card. Check for waveforms 1, 2, and 3. (See I/O board schematic.) If waveform 3 is not as shown, place I/O board back down in unit and place Time Base board on extender

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
	card. Check waveforms 1,2, and 3 (see Time Base schematic). If 3 is not present, replace or repair Time Base board.
8.1.2 ARM/TRIGGER/RECORD	
This diagnostic procedure will determine the condition of the ARM, TRIGGER and RECORD functions. Set the ARM and TRIGGER Delays to 0.00. Set the time base SAMPLE INTERVAL control to 1 µs. The ARM mode switch to INPUT; TRIGGER mode switch to INPUT. All other buttons out in ARM and TRIG Group. The ARM "ready" light should be on. Press the ARM button: The TRIGGER "ready" light should come on. Press the TRIGGER button and the ARM "ready" should come on. This indicates that the ARM/TRIGGER and RECORD functions are functioning.	Check to make sure that both Record mode switches are in their OUT positions. TIME BASE: Check that both source switches are in their OUT position. OUTPUT Grcup should be OFF (in). CHAN A should be INPUT. CHAN B should be OFF (or vice versa).
ARM "ready" light will not go out when ARM button is pushed.	Place time base board on extender card and check waveform 4 (see Time Base schematic), there should be a 50 ns wide pulse every time ARM button is pushed. Also check waveform 5 on the Time Base schematic for proper shape.
If TRIGGER "ready" light will not go out when TRIGGER button is pushed.	Check waveforms 6, 7, 8, and 10 on the Time Base board schematic.
If ARM light will not come on after TRIGGER button has been pushed.	On Time Base board, check waveforms 2 and 10 (see Time Base schematic). Check waveforms 1 and 2, (trigger the 'scope on the positive transition of the waveform at testpoint 10) and check waveform 11. Also, on I/O board, check waveform 4 (see I/O schematic).

8.1.3 Data Storage

Set up controls on the front panel of the 8100 as follows:

CHAN A Group	
+ INPUT	DC COUPLING
INPUT RANGE	± 5
INPUT OFFSET	0.00
INPUT/OFF	INPUT
CHAN B Group	OFF
ARM Group	All buttons OUT
TRIGGER Group	All buttons OUT
TIME BASE Group	
SAMPLE INTERVAL	0.1 μs
SOURCE	INTERNAL
OUTPUT Group	OFF
RECORD Mode	Both buttons out

Connect the function generator output to the 8100 + CHAN A INPUT, as shown in Figure 8.1. Set the output level of the function generator to 10 V peak-to-peak. Use a triangle waveform and a frequency of 5 KHz. Press ARM button, press TRIGGER button, the display should be as shown in Figure 8.2. Since the signal itself was not used for Triggering, the waveforms stored in the 8100 may show a different start and end point than that shown in Figure 8.2. Inspect the waveform on the display closely, it should be a smooth, continuous triangle waveform with no large steps, gaps or extraneous data shown on it. If the waveform stored is not as shown in Figure 8.2, proceed with the Troubleshooting portion.

DIAGNOSTIC PROCEDURE

If Figure 8.2 is a straight line, instead of a triangle, place the Input Amplifier board on an extender card and jumper the inputs from the front panel BNC connectors to the connectors on the Input amp board.

TROUBLESHOOTING PROCEDURE

Check the Input Amplifier PCB waveforms 1 through 4 as shown on its schematic. If waveforms are correct, place the Input Amplifier back into the chassis.

Place memory board on extender boards. CAUTION: The extender cards (there are two) for the memory board must be positioned correctly for the memory board to operate on the extender cards. The front extender card has a full set of contacts and should be inserted with the ground side (this is the continuous finger side) to the front. The second card should be inserted with the ground side to the rear. The contacts of these two extenders must be aligned properly with the connector contacts. On the Memory board, check waveforms 1 through 8. If no data is observed from the A to D converter, (straight lines for waveforms 1 through 8), check reference supplies ER, CB, -6.4, and -3.2. The schematics for these supplies are shown on the Pre Memory regulator schematic. If data is present at the inputs to the memory, (waveforms 1 through 8), then check the following waveforms and voltages on the memory board: Check waveforms 9 through 13, the -5 V supply, and the -10 V supply. The -5 V supply should measure $\sim$ 5.87 V and the -10 V supply should measure $\sim$ 12.05 V.

If the above checks are positive, check waveforms 14 through 23 as shown on the memory board schematic.

8.1.4 CHAN A Functions

With the unit still connected to the function generator as shown in Figure 8.1, set up the 8100 front panel controls in the following manner:

ARM Group

MODE	AUTO

TRIGGER Group

MODE	INPUT
SOURCE	INTERNAL
LEVEL	+0.1
SLOPE	+
COUPLING	DC

DIAGNOSTIC PROCEDURE		TROUBLESHOOTING PROCEDURE
DELAY	0.00	
SAMPLE INTERVAL	0.1 μs	
OUTPUT Group	OFF	
RECORD MODE	Both out	

Once the above controls have been set to the positions indicated, the 8100 should continuously trigger, store new data, re-arm, and trigger again. If it does not, use the manual ARM and manual TRIGGER buttons, proceeding with the checkout given above to diagnose the problem in the ARM or TRIGGER Group under that procedure. Change the coupling on the +Input from DC to AC, the output waveform should change to that shown in Figure 8.3.

With the output of the function generator connected to the (minus) Input of CHAN A and the coupling switch in the DC position, the output waveform should be as shown in Figure 8.2. Select AC coupling. The output display should be as shown in Figure 8.3.

Reconnect the output of the function generator to the +Input of CHAN A. Select DC coupling. Set the function generator controls and the input range switch as follows:

FUNCTION GEN. OUTPUT LEVEL VOLTS P-P	± INPUT RANGE	TROUBLESHOOTING PROCEDURE
		Check Input amp board.
		Check Range switch on front panel.
10	5	
4	2	
2	1	
1	0.5	
0.4	0.2	
0.2	0.1	
0.1	0.05	

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
The output waveform should be the same amplitude with each input and the respective input range.	
Repeat the above steps with the function generator connected to the - (minus) input of CHAN A.	
Return the output of the function generator to 10 V peak-to-peak, the input range to ± 5 V and the input to + DC. Set the input offset to +0.02. The plus OFFSCALE light should light. Set the INPUT/OFFSET to -0.02. The minus offscale light should light.	If, with 0.02 offset, the lamp(s) don't work, increase the offset to 0.10. Check again and see if the OFFSCALE lights work. If they do, it indicates that the unit requires recalibration on the offset range, see Section 6.5 for the procedure. If the OFF-SCALE lights still do not work, refer to the schematics and check for ALI Output on 1 to 6 BIT board. Also check for the $\overline{SSI}$ input to the Front Panel circuit board and check the Front Panel circuits and LED drivers.
Disconnect the input from CHAN A and change the front panel controls as follows: TRIGGER Group MODE AUTO INPUT/OFFSET 0.00 A straight line should be visible across the center of the display output. Advance the 100ths selector on the OFFSET control for CHAN A one step (0.01) at a time. This should move the flat line 1% of half scale with each movement on the display. Reset the 100th selector to 0.00. Advance the 10ths selector 0.1 at a time. The display trace should move 10%	Place the D to A board on an extender card and check the CHAN A Offset D to A converter for proper operation. Refer to the schematics for the D/A board and measure the voltage at "OCA" as a function of the OFFSET control. This should be as follows: -0.99 = + 7.10 V +0.99 = - 7.10 V

of half scale with each step.

8.1.5 CHAN B Functions

Change front panel controls as follows:

CHAN A

INPUT/OFF	OFF

CHAN B

INPUT/OFF	INPUT

ARM

MODE	AUTO

TRIGGER

MODE	INPUT

All other front panel controls remain the same as they were the step above. Repeat the procedures for the CHAN B Group as outlined above for the CHAN A Group. All functions and troubleshooting are the same except for the CHAN B designations.

DUAL CHAN OPERATION

Connect the output of the function generator to the inputs of CHAN A and CHAN B of the 8100 as shown in Figure 8.4. Set up front panel controls as follows:

CHAN A

+ INPUT	DC coupling
INPUT RANGE	5 V

DIAGNOSTIC PROCEDURE		TROUBLESHOOTING PROCEDURE
INPUT/OFFSET	0.00	
INPUT/OFF	INPUT	
CHAN B		
+ INPUT	DC coupling	
INPUT RANGE	5 V	
INPUT/OFFSET	0.00	
INPUT/OFF	INPUT	
ARM Group	AUTO	
TRIGGER Group	INPUT	
DELAY	0.00	
SOURCE	INTERNAL	
INTERNAL	CHAN A	
SLOPE	+	
COUPLING	DC	
LEVEL	+0.10	
TIME BASE		
SAMPLE INTERVAL	0.1 μs	
SOURCE	INTERNAL	
OUTPUT Group	OFF	
RECORD		
MODE	Both out	

Using CAL button make sure that both CHAN A vertical position and CHAN B vertical position are lined up exactly, one on top of the other. The output wavefrom should be as shown in Figure 8.5. Some readjustment of the function generator output level

If the unit fails to operate in dual channel operation, check the INA and INB lines coming off of the I/O board. Also check the ICP and $\overline{\text{ICP}}$ signals coming off of the memory board. The ICP signal should be as shown in waveform 24 on the prememory board schematic.

DIAGNOSTIC PROCEDURE

may be necessary to give a full-scale output on the display.

Set the CHAN B INPUT OFFSET sign to +0.0 and advance the OFFSET control on CHAN B 0.1 at a time. The CHAN B stored signal should move positive. It should move about half the total range of the output with an offset of +0.90.

Change the input range control on CHAN B and the stored signal should approach that of a square wave as the range sensitivity is increased. This is shown in Figure 8.6 and Figure 8.7. NOTE: Some distortion between the two waveforms is normal at this sample interval rate.

8.1.6 ARM Control Functions

Set up the front panel controls in the following configuration.

CHAN A Group

+ INPUT	DC COUPLING
RANGE	5 V
OFFSET	0.00
INPUT/OFF	INPUT

CHAN B Group

+ INPUT	DC
INPUT RANGE	± 5

TROUBLESHOOTING PROCEDURE

Also check the multiplex signal on the input amp board schematic waveform 5. NOTE: If a triggered oscilloscope is being used for the display, check that any "trigger holdoff" delay in the oscilloscope's sweep trigger controls is set at minimum.

DIAGNOSTIC PROCEDURE		TROUBLESHOOTING PROCEDURE
INPUT OFFSET	+0.30	
INPUT/OFF	OFF	
ARM Group		
MODE	AUTO	
TRIGGER Group		
MODE	AUTO	
TIME BASE		
SAMPLE INTERVAL	0.1 μs	
SOURCE	INTERNAL	
OUTPUT	OFF	
RECORD		
MODE	Both out	
With the 8100 in this configuration, the output waveform on the display should be a moving triangle waveform--it may move from either right to left or left to right across the face of the CRT, since both the ARM and the TRIGGER Groups are in AUTO mode. Place the ARM mode selector to INPUT. The display should stop moving. Press the manual ARM button. Each time the manual ARM button is pressed, new data should be stored in the 8100 and displayed on the display. Place the ARM SOURCE switch in INTERNAL. The 8100 should now continuously store data. The ARM "ready" light should be out or flicker very dimly at a constant rate.		If the Internal ARM fails to work, check waveform 1, 4, 5, 6, and 7 on the Front Panel schematic.
Set the ARM level to +0.00 and advance the level in steps of 0.1		If the ARM level fails to reach either +0.99 or -0.99, recalibrate

at a time. This should advance the arming point positive from 0 (midscale) on the waveform. Change the ARM level to -0.00, advance the ARM level again as above. The beginning point should move down the positive slope of the waveform. Reconnect the output of function generator to the inputs of Model 8100 as shown in Figure 8.8. Change the ARM source button from INTERNAL to EXTERNAL. The unit should still ARM and TRIGGER continuously. With a full-scale signal input, the ARM range should be +0.99 to -0.99.

Change the ARM input from the external 5 VFS to the 50 VFS input. With the ARM level at 0.00, the unit should ARM continuously. The range of the level control should be about one tenth that measured with the 5 VFS input.

Reconnect the inputs as shown in Figure 8.4. Set CHAN B Group INPUT/OFF to INPUT and the INPUT OFFSET to +0.30. Set ARM Group SOURCE to INTERNAL. Set the ARM LEVEL Control to +0.10. The unit should be continuously arming and triggering and storing data. Note the arming point on CHAN A. Change the ARM INTERNAL switch from CHAN A to CHAN B. The arming point should stay the same but the CHAN B information should be at the relative amplitude point, as shown in Figure 8.9 and Figure 8.10. Change the ARM SLOPE from (+) to (-). The waveform should be as shown in Figure 8.11. Set the CHAN B INPUT/OFF to OFF. In the ARM Group, change the COUPLING from DC to AC. A slight change in arming location should take place.

the ARM level calibration per Section 6.6. If the ARM level is not a smooth progression, up and down the slope of the waveform, check the ARM D to A converter on D to A board. Also check front panel level switch for proper operation. The nominal range of the ARM D/A OUTPUT "ALV" as a function of ARM level is:

+0.99 = +8.20 V
-0.99 = -8.20 V

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
If this is not noticeable,lower the frequency of the function generator to 1 kHz. At this point, an approximately one-half inch displacement of the trace should occur between the DC and AC ARM coupling selections. Return the coupling selector to the DC position.	
Step the ARM delay hundredths selector one digit at a time, each step should move the signal to the left on the display (10 words each step to 90 words). Return the 100ths selector to 0. Advance the 10ths delay position one digit at a time, each step will represent 100 words of memory. Again the trace should move to the left, but 100 words per step to 900 words total. Return the 10ths digit to zero position. Advance the units delay selector one digit at a time. Each time the units selector is advanced, the signal should invert, (or appear to invert). Each digit represents 1000 words (1/2 the total number of words stored in the memory). The total range of this delay selector is 9000 words.	
If the delays are improper or do not function at all, check the latches and the presettable count-down counters on the Time base board.	Check the operation of the front panel ARM DELAY switches.
Change the front panel controls as follows:	
ARM Group	
MODE AUTO	

8.1.7 TRIGGER Functions

The Trigger Control Group is

checked out in an identical manner as the ARM Group. Repeat the procedures for the ARM Group using TRIGGER in place of ARM on all notations. The hook-up will be as shown in Figure 8.12. After diagnosing the TRIGGER functions, please make the following front panel control changes:

TRIGGER Group

MODE	INPUT
SOURCE	INTERNAL
SLOPE	+
COUPLING	DC
LEVEL	+0.10
DELAY	0.00

8.1.8 TIME BASE GROUP

Set the output of the function generator to a 50 kHz triangle waveform and connect the function generator to the 8100 as shown in Figure 8.1. Set the sample interval time to 0.01 us. The output should be as shown in Figure 8.13. Using the following table, set the function generator to each frequency shown and the 8100 sample interval control to the indicated setting and check that the display is correct as listed.

Sample Interval Setting	Function Generator Freq. Setting	Complete Cycles on Display
0.01 µs	50 kHz	1
0.02 µs	50 kHz	2
0.05 µs	50 kHz	5
0.1 µs	5 kHz	1
0.2 µs	5 kHz	2
0.5 µs	5 kHz	5
1 µs	500 Hz	1

All of the troubleshooting for the sample interval rates are found on the Time Base board and the Time Base controls. Check to make sure that the 7442 IC (C-9) properly decodes the 0.01 to 10 sequence from the sample interval control and be sure that the latch (C-12) stores the milliseconds and seconds rates--microseconds are derived from the Boolean Equation: us=$\overline{ms}$ and $\overline{s}$.

Sample Interval Setting	Function Generator Freq. Setting	Complete Cycles on Display
2 µs	500 Hz	2
5 µs	500 Hz	5
10 µs	50 Hz	1
0.01 ms	50 Hz	1
0.02 ms	50 Hz	2
0.05 ms	50 Hz	5
0.1 ms	5 Hz	1
0.2 ms	5 Hz	2
0.5 ms	5 Hz	5
1 ms	0.50 Hz	1
2 ms	0.50 Hz	2
5 ms	0.50 Hz	5
10 ms	0.50 Hz	1
0.01 s	0.50 Hz	1
0.02 s	0.50 Hz	2
0.05 s	0.50 Hz	5

From this last sample interval setting on to 10 s, it is not recommended that the person doing the checkout wait for the complete 2048 word recording to take place because, very shortly, the time required to do this will approach half-hours and hours, rather than just a few seconds. It is recommended that the function generator be left at 0.05 Hz and that the remaining sample intervals be checked with a stop watch or a sweep second hand on an accurate time piece, rather than waiting for the entire record sweep to take place.

EXTERNAL TIME BASE INPUTS

Connect a short coaxial cable (approximately 18" in length) between the "Time Base Out" BNC and the "Time Base In" BNC connectors on the rear panel. Set the source switch INTERNAL/ EXT <0.25ms to the "EXT <0.25ms" position, set the SAMPLE INTERVAL control to 0.02 µs, input a 50 kHz

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
triangle wave from the function generator. Two complete waveforms should be continuously stored and displayed on the display device. Change SAMPLE INTERVAL to 0.2 ms. Change function generator rate to 5Hz. Two complete cycles should be stored in the 8100. Change the INTERNAL/EXT >1 ms button to the "EXT >1 ms" position. Change the SAMPLE INTERVAL to 0.5 ms: Five complete waveforms should be stored. Change the source switch INTERNAL/EXT <0.25 ms to the INTERNAL position (out). Change SAMPLE INTERVAL to 1mS: Ten complete cycles should be stored in the 8100.	
8.1.9 OUTPUT Group	
Change front panel controls as follows:	Check I/O board if output group tests fail.
ARM Group	
INPUT/AUTO INPUT	
TIME BASE Group	
Both source switches to INTERNAL. Set SAMPLE INTERVAL to 0.1 ms.	
OUTPUT Group	
OUTPUT AUTO	
Manually ARM the unit. As soon as recording has ended, the display should return as a straight line, and both output "ready" lights should be OFF, indicating that the 8100 is in the output mode and ready to output digital data. If the 8100 is normally connected to a digital computer or other digital storage device, exercise this device to ensure that the data will be output from the 8100.	If the data is not correct, i.e., bits missing, check the D/A board and the Memory board.

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
Set the OUTPUT control to OFF then set the OUTPUT control to EDIT, with no word commands present at the rear panel connector. Both ready lights should come on. Press the DIG OUT pushbutton and the trace should drop to a straight line, indicating that the 8100 is in the output mode ready to output data. Set output mode to OFF.	
Change front panel controls as follows:	
CHAN A Group	
± RANGE 2 V	
TIME BASE 0.2 ms	
TRIGGER SLOPE -	
Manually ARM unit. Output should be as shown in Figure 8.14. Set output group to EDIT. Connect scope to plot out BNC connector. Press plot button and unit should go into plot output, presenting analog data at a 10 ms per point rate. The total time to complete the output cycle should be 20.4 s for the standard unit or an optional rate if the unit was configured for one of the optional plot sweep times.	
Plot level at the scope should be 1 V full scale. At the end of the first plot cycle, connect the scope to the pen output BNC connector. Press the plot button. A 1 ms positive pulse should be present at the pen output at the start of the plot for the standard unit-see optional specifications for other outputs.	If the plot output will not follow the stored data, check the Time Base-"PCC" output and check the I/O board and D/A board. If the 1 ms pulse is not present, check I/O board.

8.1.10 Record Mode

Set up the front panel controls in the following manner:

CHAN A Group

+ INPUT	DC COUPLING
INPUT RANGE	± 5
INPUT OFFSET	0.00
INPUT/OFF	INPUT

CHAN B Group

INPUT/OFF	OFF

ARM Group

DELAY	2.00
MODE	INPUT
SOURCE	EXTERNAL
INTERNAL	CHAN A
SLOPE	+
COUPLING	DC
LEVEL	0.00

TRIGGER Group

DELAY	1.10
MODE	INPUT
SOURCE	INTERNAL
INTERNAL	CHAN A
SLOPE	+
COUPLING	DC
LEVEL	0.00

DIAGNOSTIC PROCEDURE		TROUBLESHOOTING PROCEDURE
TIME BASE Group		
SAMPLE INTERVAL	0.1 ms	
SOURCE	INTERNAL	
OUTPUT Group	OFF	
RECORD Mode		
NORM/PRETRIG	PRETRIG	
DUAL TIME BASE	OFF	
Set the function generator to a square wave output with 10 V peak-to-peak amplitude. Set the output frequency of the function generator to 0.5 Hz. Press the ARM button. The display should be as shown in Figure 8.15. The positive transition of the square wave should be directly in the center of the display on the X axis. Change the front panel controls as follows:		If the pretrigger record does not function properly, check "PTR" and "DTB" latches on Time Base board.
SAMPLE INTERVAL	1 ms	
Press the ARM button, the display should be the same as in Figure 8.15. Change the front panel controls as follows:		
RECORD MODE		
NORM/PRETRIG	NORM	
DUAL TIME BASE		
OFF/ON	ON	
TIME BASE Group		
SAMPLE INTERVAL	1 µs	
Set the ALT INTERVAL button. Change the SAMPLE INTERVAL to 0.1 us. Change the output of the function generator to a		

DIAGNOSTIC PROCEDURE

triangle wave. Set the output frequency to be 5 kHz. Set the Trigger Delay to 1.00. All other front panel controls remain the same. Press the ARM button. The output waveform should be as shown in Figure 8.16. Change the front panel controls as follows:

TIME BASE Group

SAMPLE INTERVAL 1 ms

Press the ALT INTERVAL button.

SAMPLE INTERVAL 2 ms

All other front panel controls remain the same.

Change the frequency of function generator to 0.5 Hz. Press the ARM button. The output should be as shown in Figure 8.17. Change the front panel controls as follows:

ARM Group

DELAY 1.00

TRIGGER Group

DELAY 1.10

TIME BASE Group

SAMPLE INTERVAL 2 ms

Set ALT INTERVAL button. Change the SAMPLE INTERVAL to 1 ms.

RECORD MODE

NORM/PRETRIG PRETRIG

DUAL TIME BASE ON

Set the output rate of the function generator to 0.5 Hz. Press

TROUBLESHOOTING PROCEDURE

If the pretrigger record does not function properly, check "DTB" and "PTR" latches on Time Base board.

the ARM button. The output on the display should be as shown in Figure 8.18.

8.2 External Program Diagnostic Procedure

If the 8100 is normally used with a digital computer, or another digital control device, use the following diagnostic program for checking out and troubleshooting that portion of the 8100. This program should be loaded into the rear panel connector in the order given using the data exchange methods described in Section V. Connect the output of the function generator to the input of the Model 8100 as shown in Figure 8.19. Set the output rate to a 1 kHz sign wave with a peak-to-peak amplitude of 2.5 V.

Step	Function	B0 through B12 Program Inputs												
		12	11	10	9	8	7	6	5	4	3	2	1	0
1.	Set Program Mask-TRIGGER Group, ARM Group, CHAN B Group, CHAN A Group, TIME BASE, OUTPUT, and RECORD Group.	0	1	0	0	0	1	1	1	1	1	0	0	0
2.	Main Time Base = INT, 2.0 us	0	1	1	0	0	0	0	0	0	0	1	1	1
3.	OUTPUT = OFF	0	1	1	1	0	0	0	0	0	0	0	0	0
4.	RECORD - Start, Trigger; Stop, End of Sweep.	0	1	1	1	1	0	0	1	0	0	0	0	0
5.	CHAN A - +INPUT; AC COUPLING; Range, $\pm$ 1.0 V	1	0	0	0	0	0	1	0	0	0	1	0	0
6.	CHAN A - INPUT OFFSET = 0.00	1	0	0	0	1	0	0	0	0	0	0	0	0
7.	CHAN A - INPUT/OFF = INPUT; OFFSET sign = minus	1	0	0	1	0	0	0	0	1	1	0	0	0
8.	CHAN B - INPUT = DC COUPLING; Range=1.0 V	1	0	1	0	0	0	0	1	0	0	1	0	0
9.	CHAN B - INPUT OFFSET = 0.25	1	0	1	0	1	0	0	1	0	0	1	0	1
10.	CHAN B - INPUT/OFF = INPUT; OFFSET sign = minus	1	0	1	1	0	0	0	0	1	0	0	0	1
11.	TRIG DELAY, 2nd digit = 0 LSD = 0	1	1	1	0	0	0	0	0	0	0	0	0	0
12.	TRIG DELAY, MSD = 0	1	1	1	0	1	0	0	0	0	0	0	0	0
13.	TRIG LEVEL = 0.25	1	1	1	1	0	0	0	1	0	0	1	0	1

Step	Function	B0 through B12 Program Inputs												
		12	11	10	9	8	7	6	5	4	3	2	1	0
14.	TRIG MODE = INPUT, SOURCE = INT, INT SOURCE = CHAN A, SLOPE = +, COUPLING = DC, LEVEL polarity = +	1	1	1	1	1	0	0	1	0	1	0	0	1
15.	ARM DELAY, 2nd digit = 0, LSD = 0	1	1	0	0	0	0	0	0	0	0	0	0	0
16.	ARM DELAY, MSD = 0	1	1	0	0	1	0	0	0	0	0	0	0	0
17.	ARM LEVEL = 0.00	1	1	0	1	0	0	0	0	0	0	0	0	0
18.	ARM MODE = INPUT, SOURCE = EXT, INT SOURCE = CHAN A, SLOPE =(-), COUPLING = DC, LEVEL polarity = +	1	1	0	1	1	0	0	0	0	0	0	0	0
19.	Reset instruction	0	1	0	0	1	0	0	0	0	0	0	0	1
20.	Set Function - ARM	0	1	0	0	1	0	0	0	1	0	0	0	0
21.	Read status-(Display should be as shown in Figure 8.20.)	0	1	0	1	0	0	0	0	0	0	0	0	0
	If output mode is used, proceed as follows:													
22.	OUTPUT MODE - AUTO	0	1	1	1	0	0	0	0	0	0	0	0	1
23.	Set Function - ARM	0	1	0	0	1	0	0	0	1	0	0	0	0
24.	Enable output data	0	1	0	1	1	0	0	0	0	0	0	0	0
	After data is output, front panel control can be restored by:													
25.	Set Program Mask - Front Panel control.	0	1	0	0	0	0	0	0	0	0	0	0	0

8.2.1 Troubleshooting the External Programming

Check the interface cable connectors and grounds between the 8100 and the digital control device and check or change the I/O board.

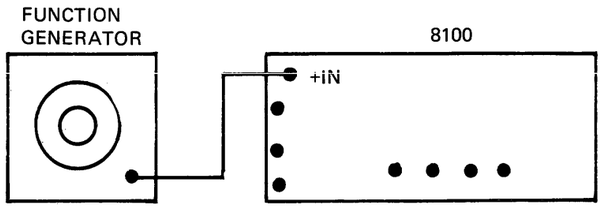


FIGURE 8.1

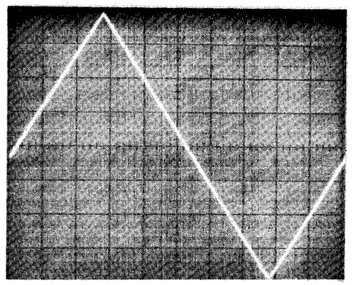


FIGURE 8.2

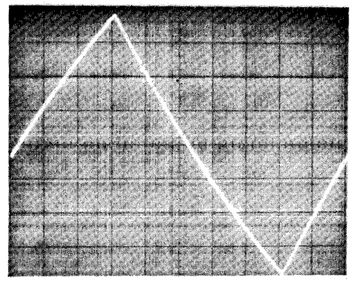


FIGURE 8.3

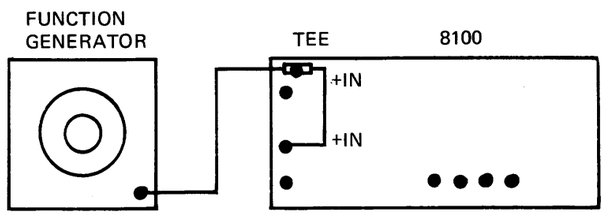


FIGURE 8.4

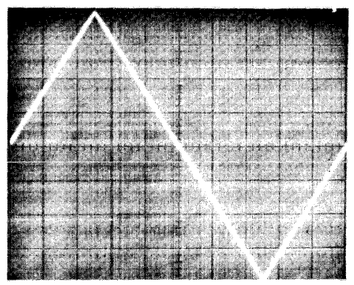


FIGURE 8.5

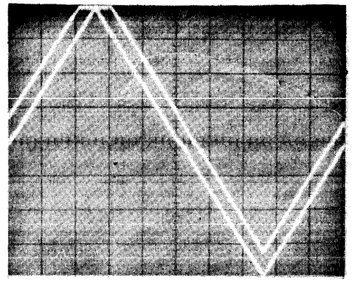


FIGURE 8.6

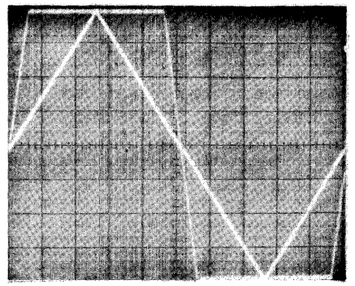


FIGURE 8.7

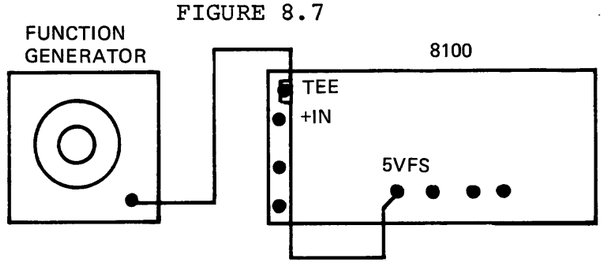


FIGURE 8.8

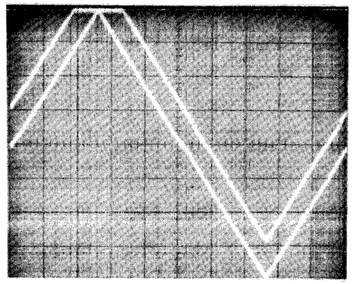


FIGURE 8.9

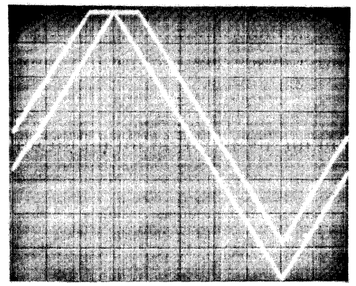


FIGURE 8.10

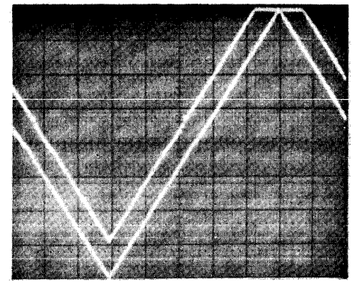


FIGURE 8.11

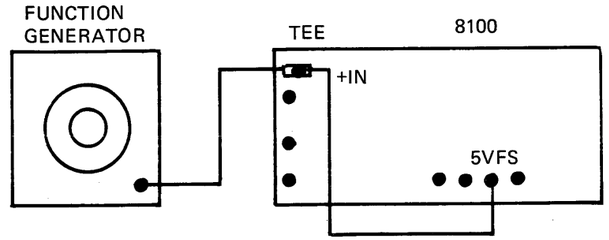


FIGURE 8.12

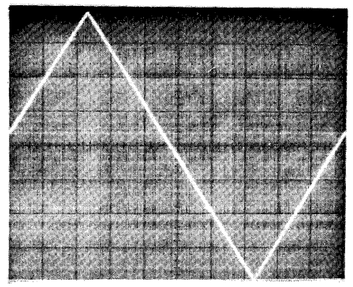


FIGURE 8.13

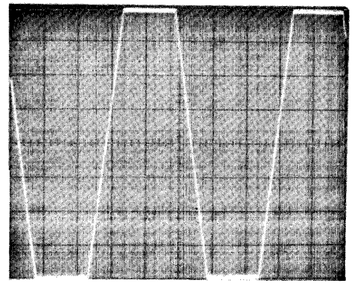


FIGURE 8.14

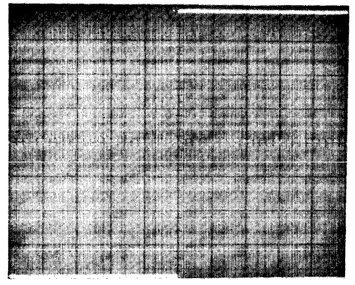


FIGURE 8.15

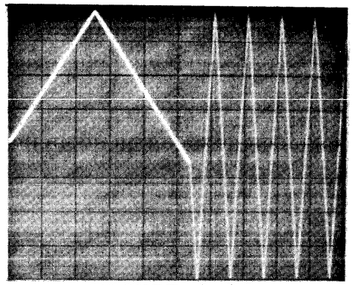


FIGURE 8.16

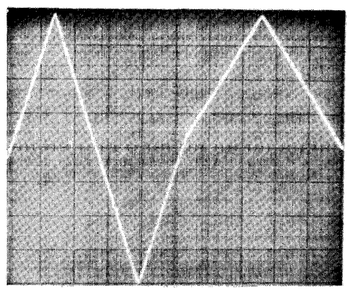


FIGURE 8.17

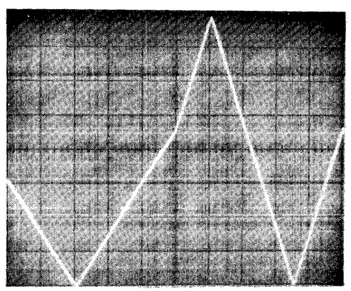


FIGURE 8.18

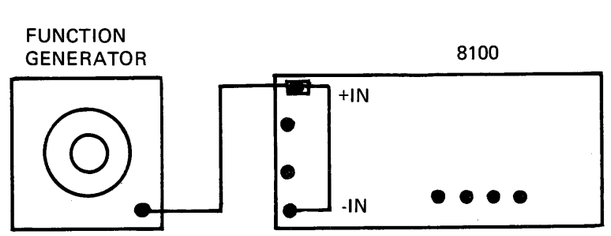


FIGURE 8.19

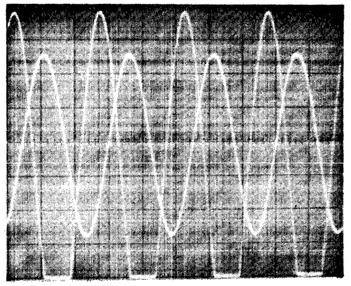


FIGURE 8.20

SECTION IX

Schematics, Mechanical Drawings and Maintenance Diagnostic Illustrations

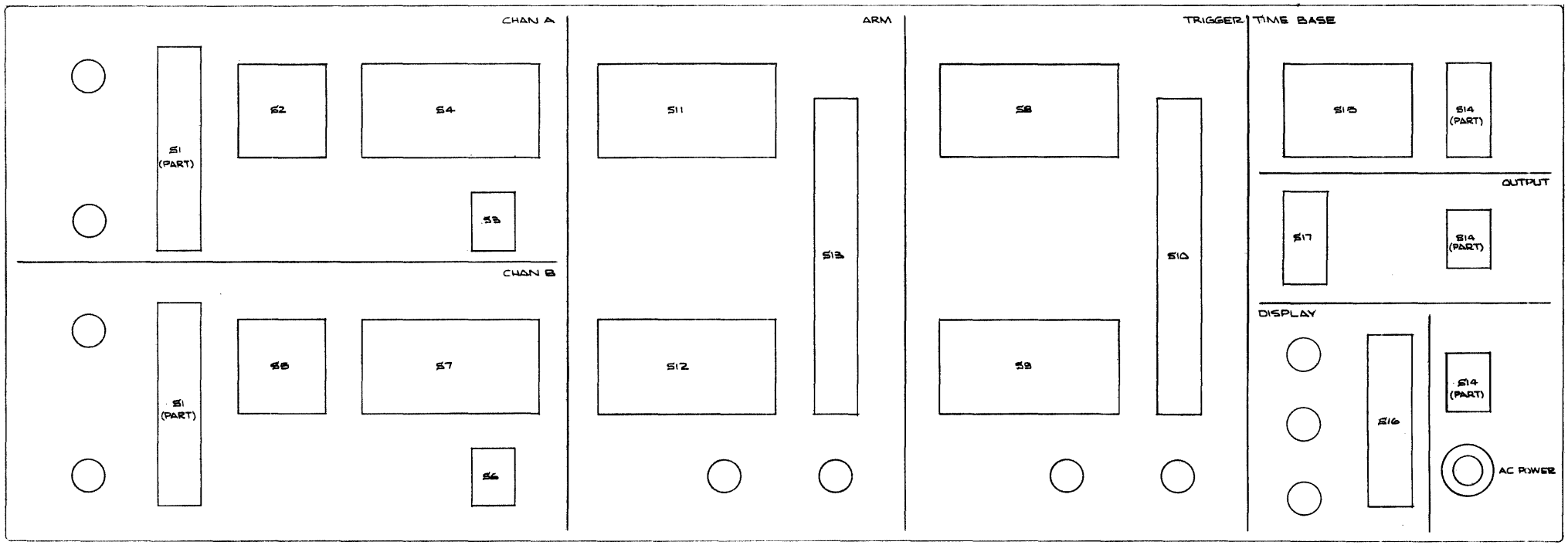


FIGURE 9.1 Front Panel Switch Layout, Front View

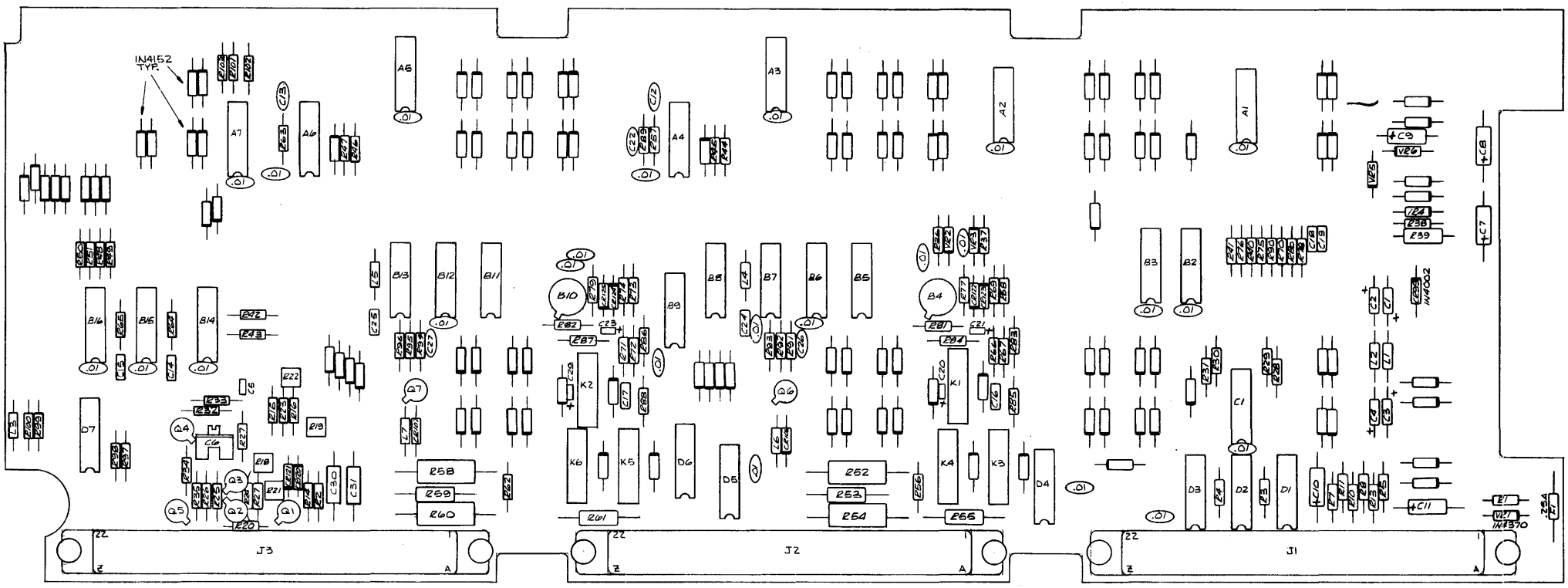


FIGURE 9.2 Front Panel Circuit Board Layout

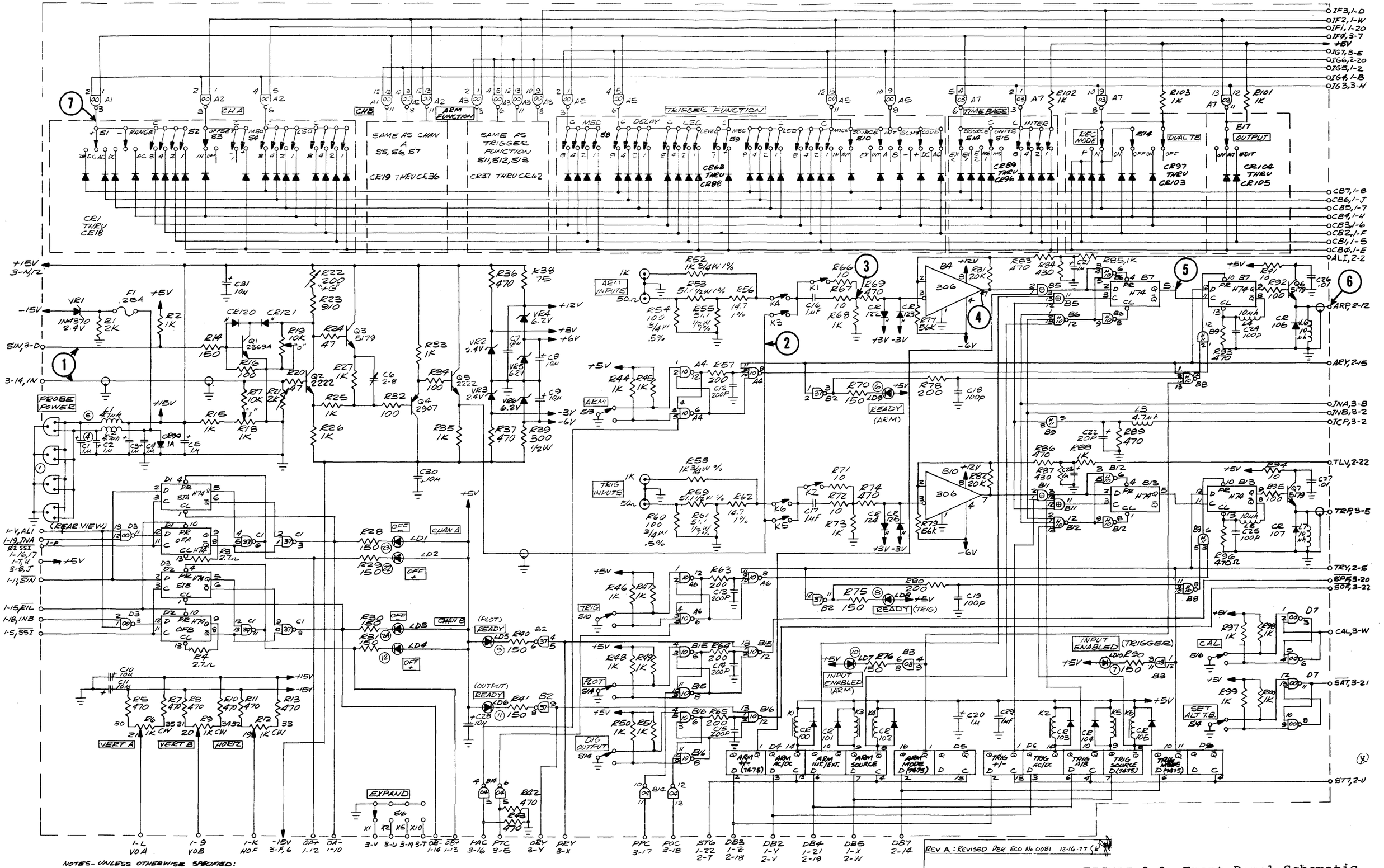
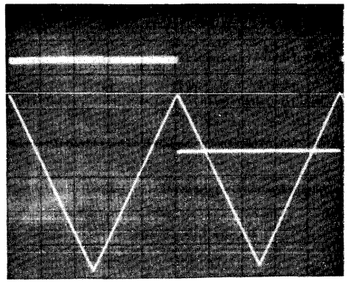
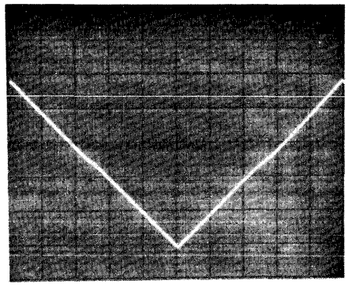


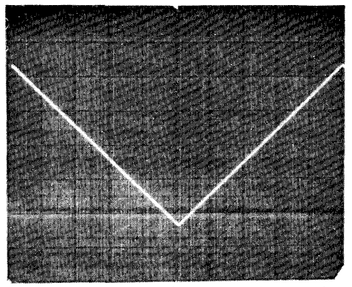
FIGURE 9.3 Front Panel Schematic



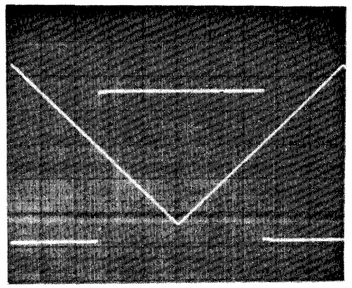
1. Scope: Vert 1V/div, Horz 20μ sec/div, Trigger internal.
   8100: Input 10V PP 5kHz Triangle



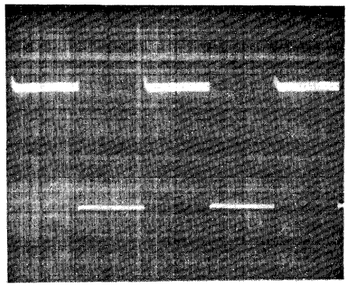
2. Scope: Vert 1V/div, Horz 20μ sec/div, Trigger external-generator sync.
   8100: Input 10V PP 5kHz Triangle



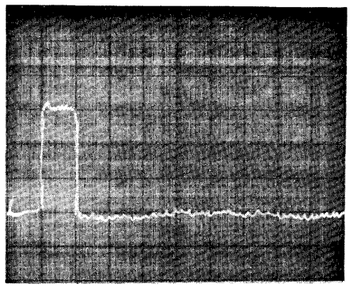
3. Scope: Vert 1V/div, Horz 20μ sec/div, Trigger external-generator sync.
   8100: 10V PP 5kHz triangle input to 5VFS
   ARM input, ARM Group Source-EXT.



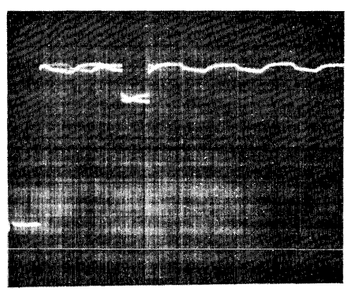
4. Scope: Vert 1V/div, Horz 20μ sec/div, Trigger external-generator sync.
   8100: 10V PP 5kHz triangle input to 5VFS
   ARM input, ARM Group Source-EXT.



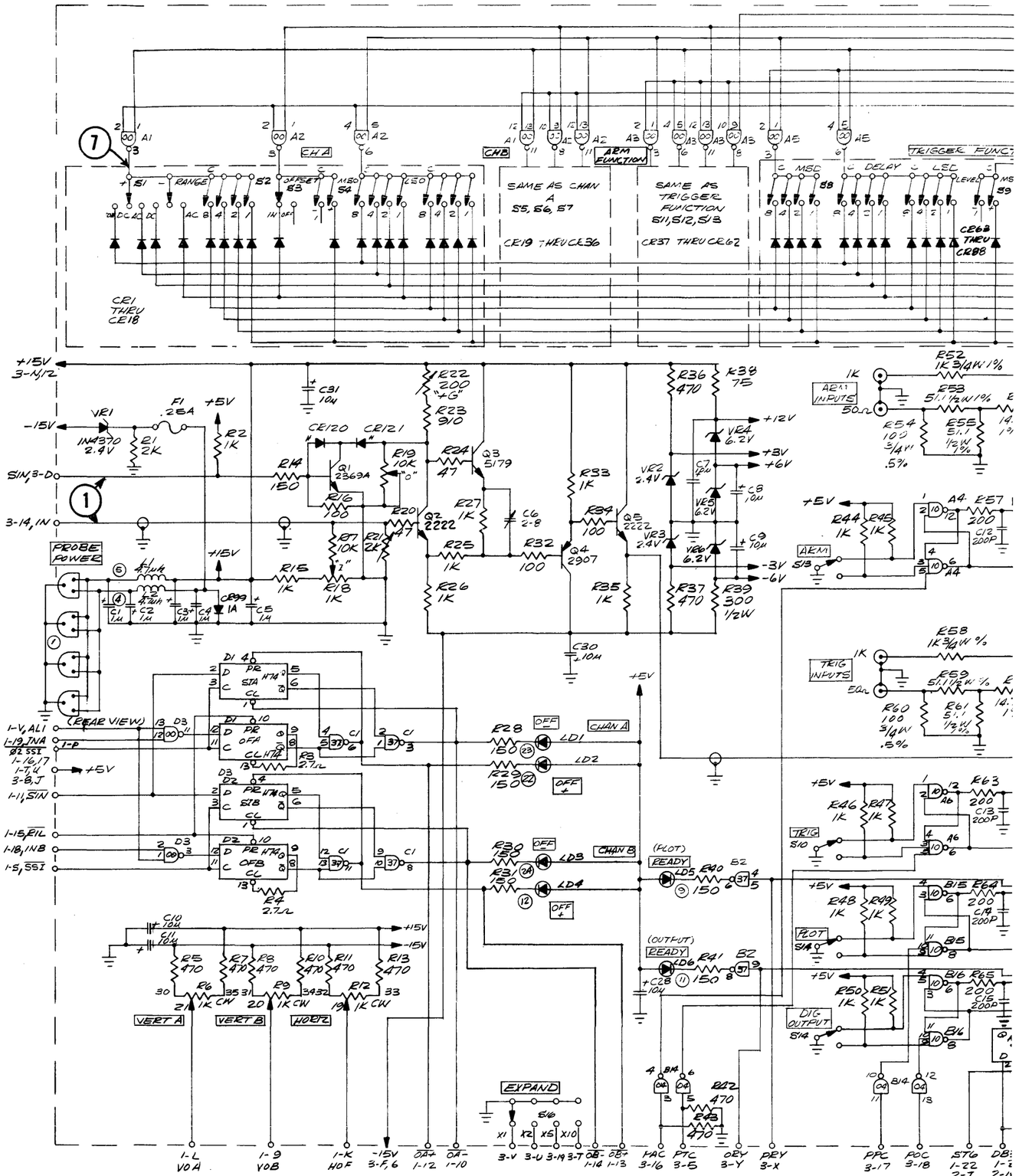
5. Scope: Vert 1V/div, Horz 50μsec/div, Trigger external-generator sync.
   8100: 10V PP 5kHz triangle input to 5VFS
   ARM input, ARM Group Source-EXT.



6. Scope: Vert 1V/div, Horz .05μsec/div, Trigger internal.
   8100: 10V PP 5kHz triangle input to 5VFS
   ARM input, ARM Group Source-EXT



7. Scope: Vert 1V/div, Horz 5ms/div, Trigger internal - slope.
   8100: Front Panel Control (no program inputs)



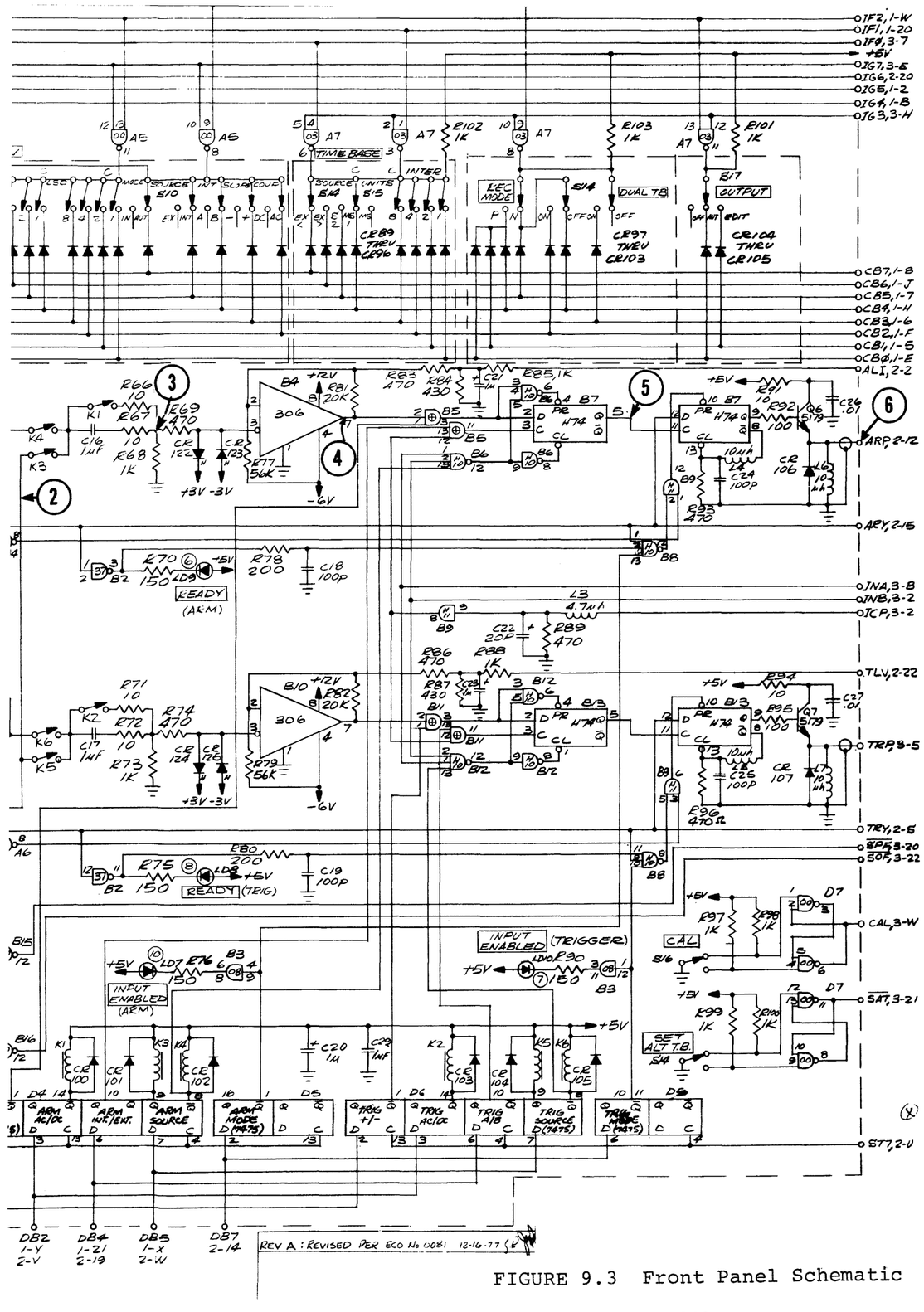
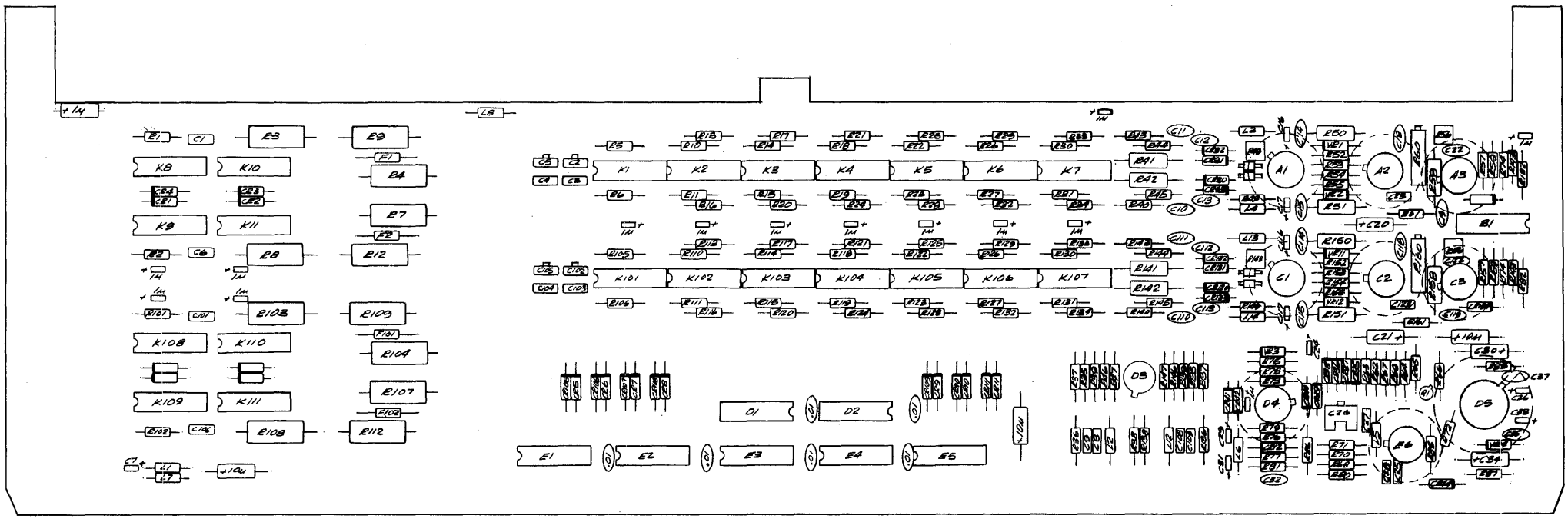
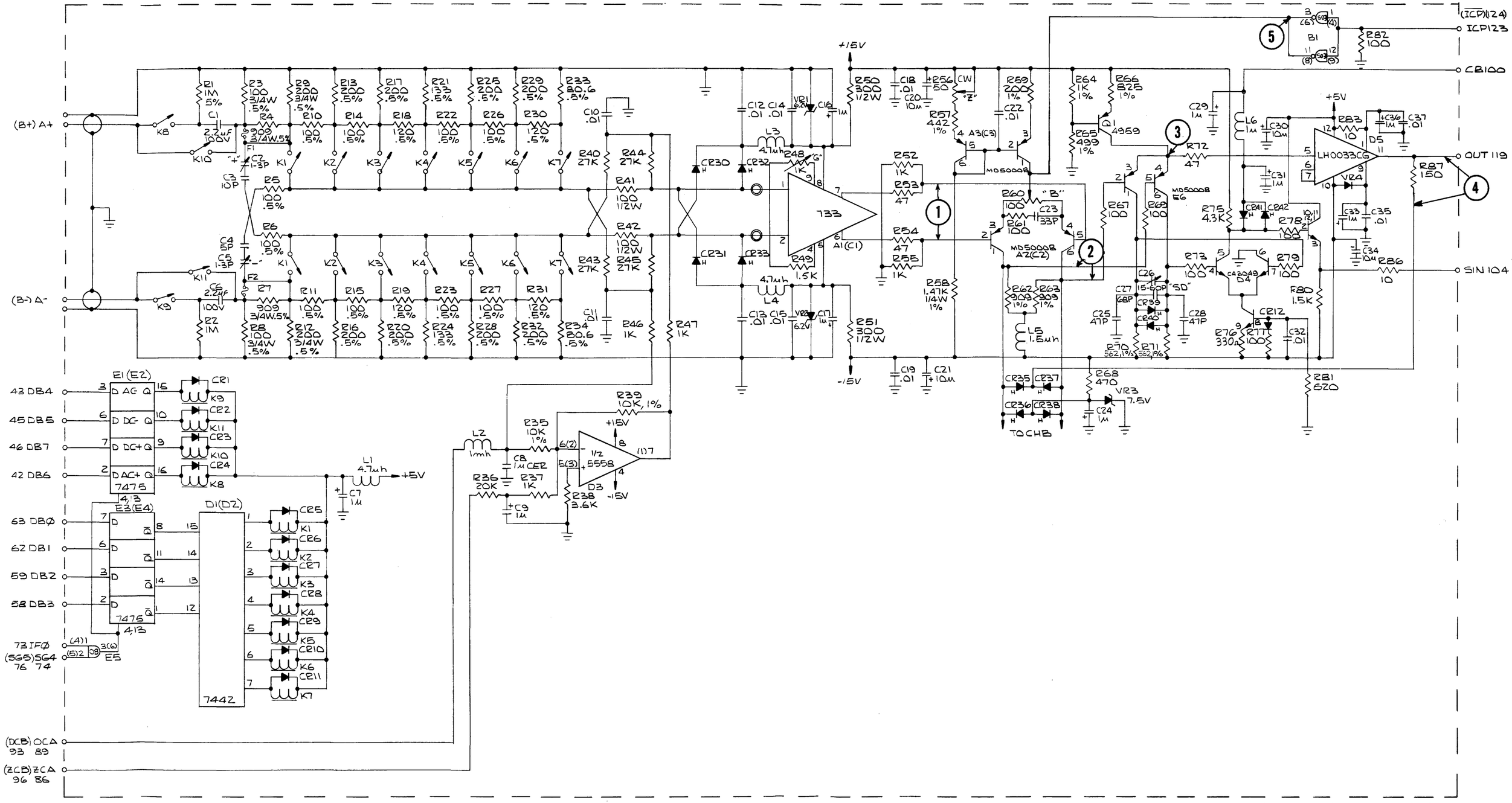


FIGURE 9.3 Front Panel Schematic



NOTES-UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/4W, 5%
2. DIODES ARE HEWLETT PACKARD 5082-2811

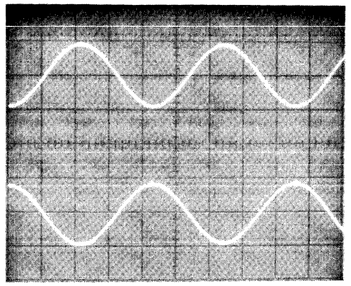
FIGURE 9.4 Input Amplifier Circuit Board Layout



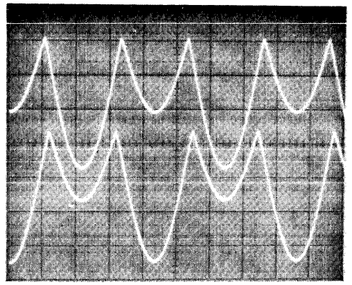
NOTES - UNLESS OTHERWISE SPECIFIED
RESISTORS .5% AND 1% TOL. ARE 1/8 WATT
ALL OTHERS ARE 1/4W, 5%

REV A - DELETE RBS, R74, 170, CR39, 138, (R93, 143, 44
REV B - REVISED PER ECO No 1143 11-30-77
RE C - REVISED PER ECO No 0112 12-1-77 2-2-73

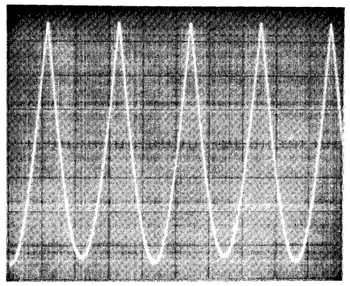
FIGURE 9.5 Input Amplifier Schematic



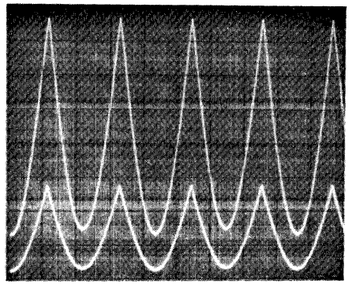
1. Scope: Vert .5V/div, Horz 50μsec/div,
   Trigger EXT on generator sync output.
   8100: input 5kHz sine wave in fullscale.



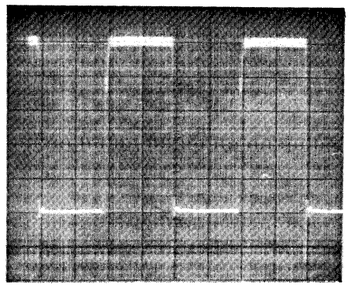
2. Scope: Vert 2V/div, Horz 50μsec/div,
   Trigger EXT on generator sync output.
   8100: Input 5kHz sine wave in fullscale.



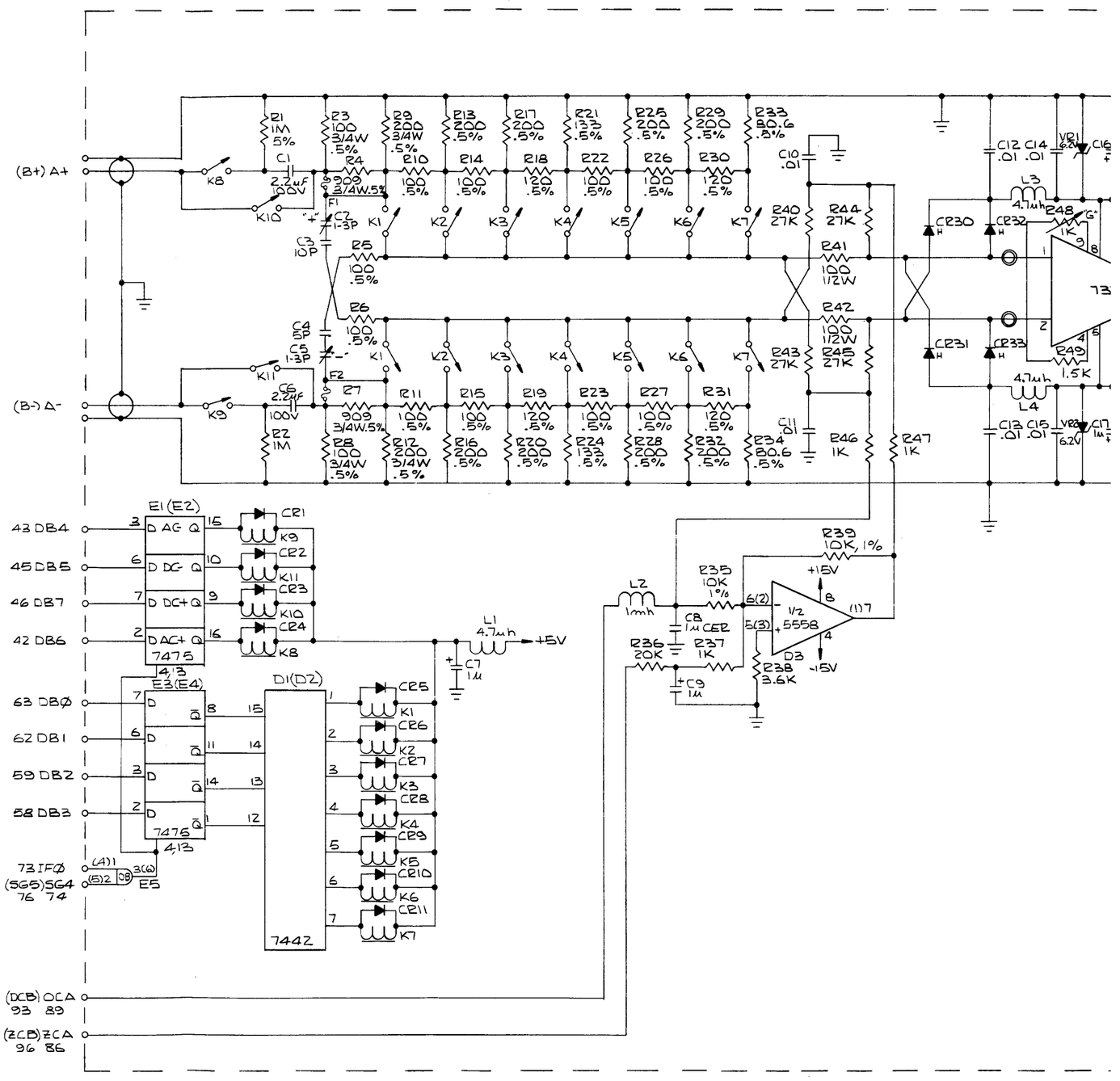
3. Scope: Vert 1V/div, Horz 50μsec/div,
   Trigger EXT on generator sync output.
   8100: Input 5kHz sine wave in fullscale.



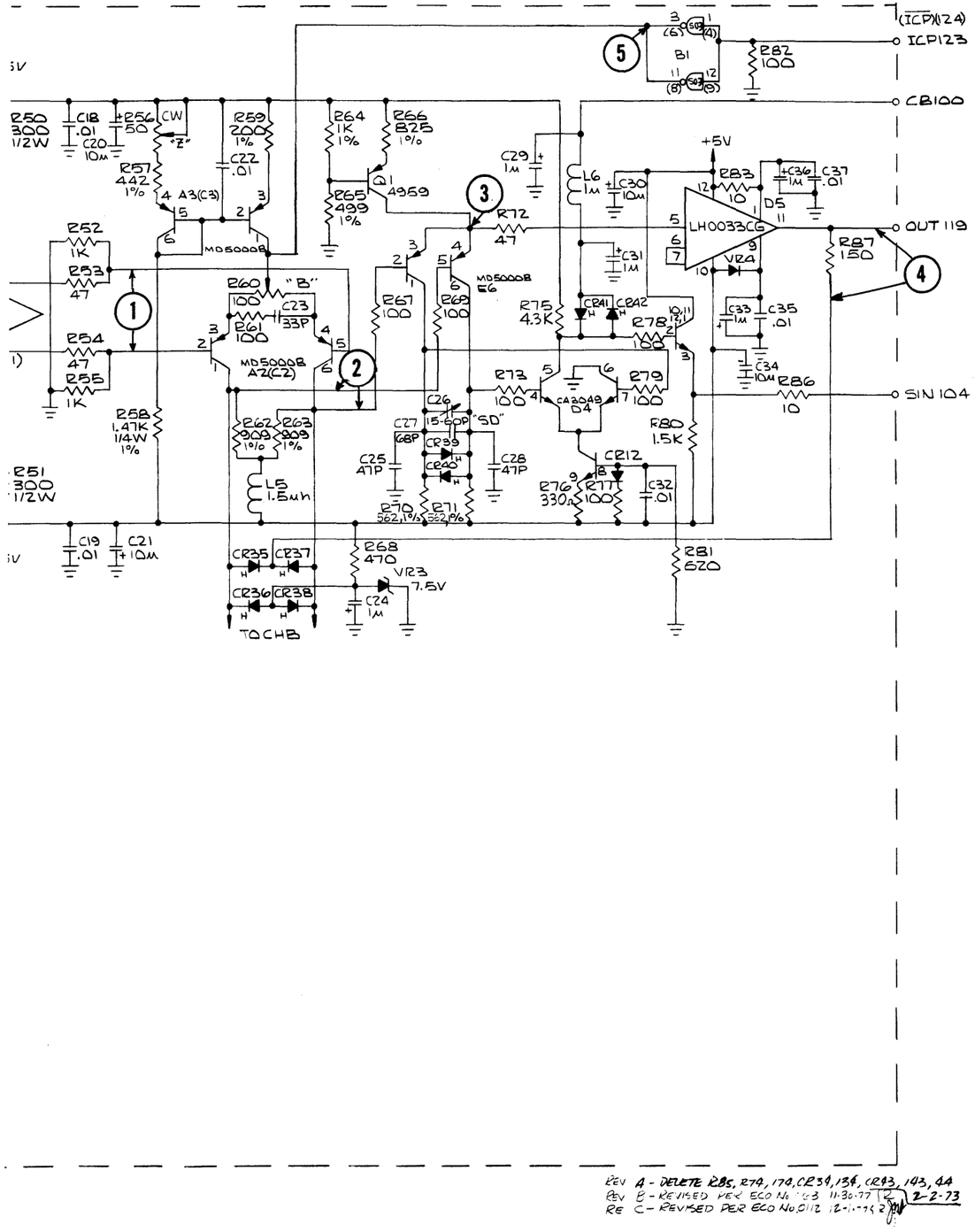
4. Scope: Vert 1V/div, CHA A, 2V/div
   CHA B, Horz 50μsec,
   Trigger EXT on generator sync output.
   8100: input 5kHz sine wave in fullscale.



5. Scope: Vert 1V/div, Horz .1μsec/div,
   Trigger Internal -/slope.
   8100: Sample interval .2μsec,
   CHA A: INPUT, CHA B: INPUT.

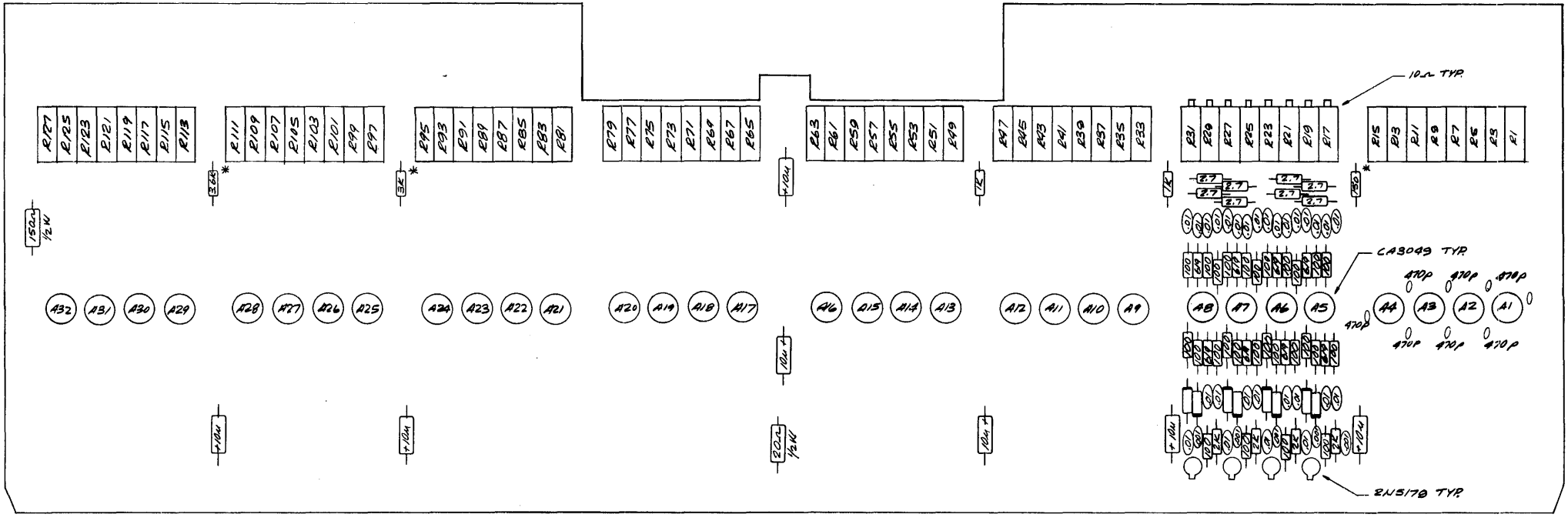


NOTES - UNLESS OTHERWISE SPECIFIED
RESISTORS .5% AND 1% TOL. ARE 1/8 WATT
ALL OTHERS ARE 1/4W, 5%



REV A - DELETE R85, R74, 170, CR39, 138, CR93, 143, 44
REV B - REVISED PER ECO No. 1163 11-30-77
RE C - REVISED PER ECO No. 0112 12-1-78 2-2-73

FIGURE 9.5 Input Amplifier Schematic



NOTES-UNLESS OTHERWISE SPECIFIED:
1. DIODES ARE HEWLETT PACKARD 5082-2811
2 * FACTORY SELECTED VALUE 618Ω AND 2K ARE 1/8 WATT, 1% OTHER RESISTORS 1/4WATT, 5%

FIGURE 9.6 "o" Bit Circuit Board Layout

REV A: REVISED PER ECO No. 061 11-30-77 SR.

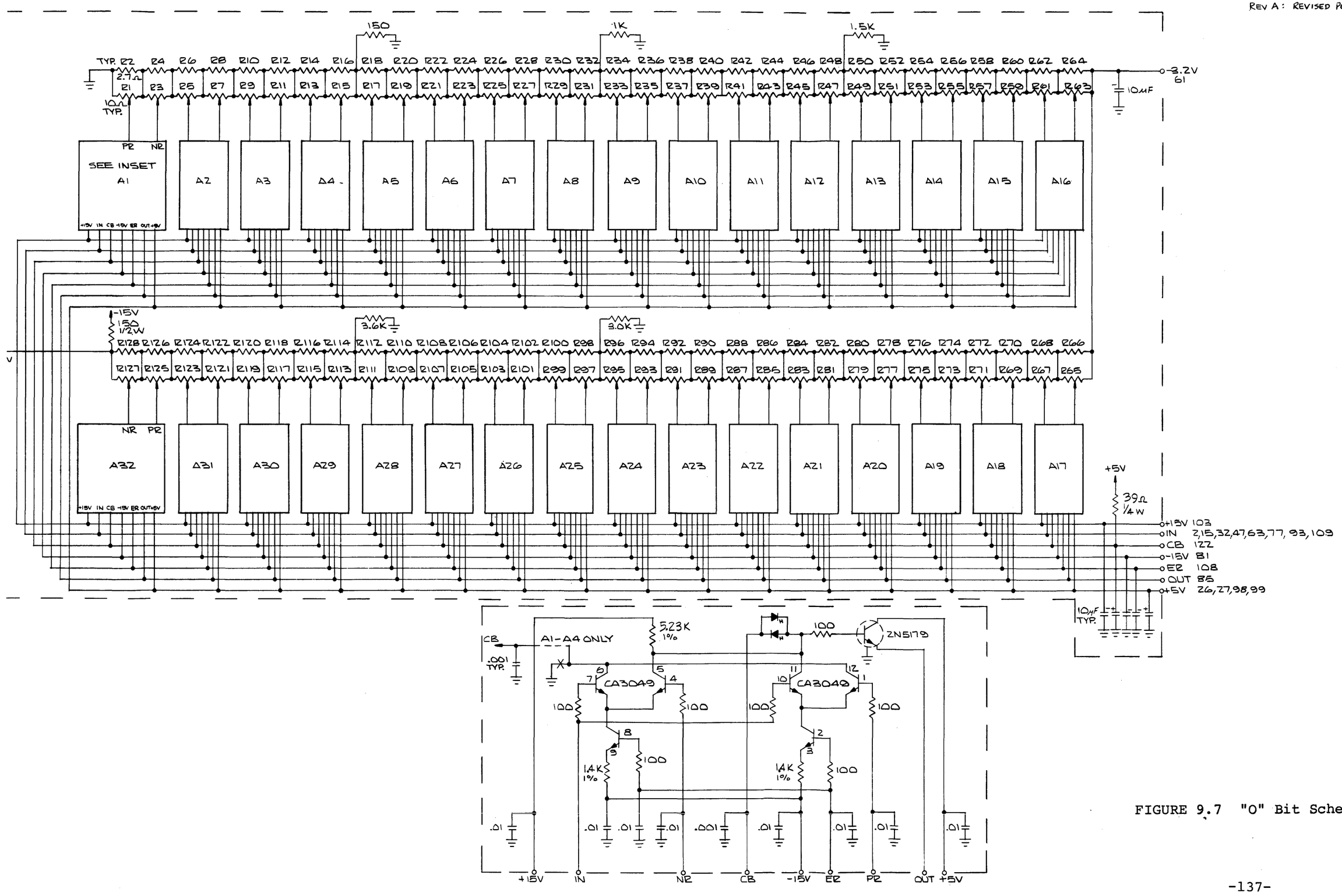


FIGURE 9.7 "O" Bit Schematic

150
1K
TYP. R2
2.7Ω
R1
10Ω TYP.
R4 R6 R8 R10 R12 R14 R16 R18 R20 R22 R24 R26 R28 R30 R32 R34 R36 R38 R40 R42 R44 R46
R3 R5 R7 R9 R11 R13 R15 R17 R19 R21 R23 R25 R27 R29 R31 R33 R35 R37 R39 R41 R43 R45
PR NR
SEE INSET
A1
A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
+15V IN CB -15V ER OUT+6V
-15V
150
1/2W
-6.4V
3.6K
3.0K
R128 R126 R124 R122 R120 R118 R116 R114 R112 R110 R108 R106 R104 R102 R100 R98 R96 R94 R92 R90 R88 R86 R84
R127 R125 R123 R121 R119 R117 R115 R113 R111 R109 R107 R105 R103 R101 R99 R97 R95 R93 R91 R89 R87 R85 R83
NR PR
A32
A31 A30 A29 A28 A27 A26 A25 A24 A23 A22 A21
+15V IN CB -15V ER OUT+6V
CB
.001 TYP.
A1-A4 ONLY
5.23K 1%
CA3049
100
1.4K 1%
.01
.001
+15V
IN
NR
CB
-15V

REV A: REVISED PER ECO No. 061 11-30-77 SR.

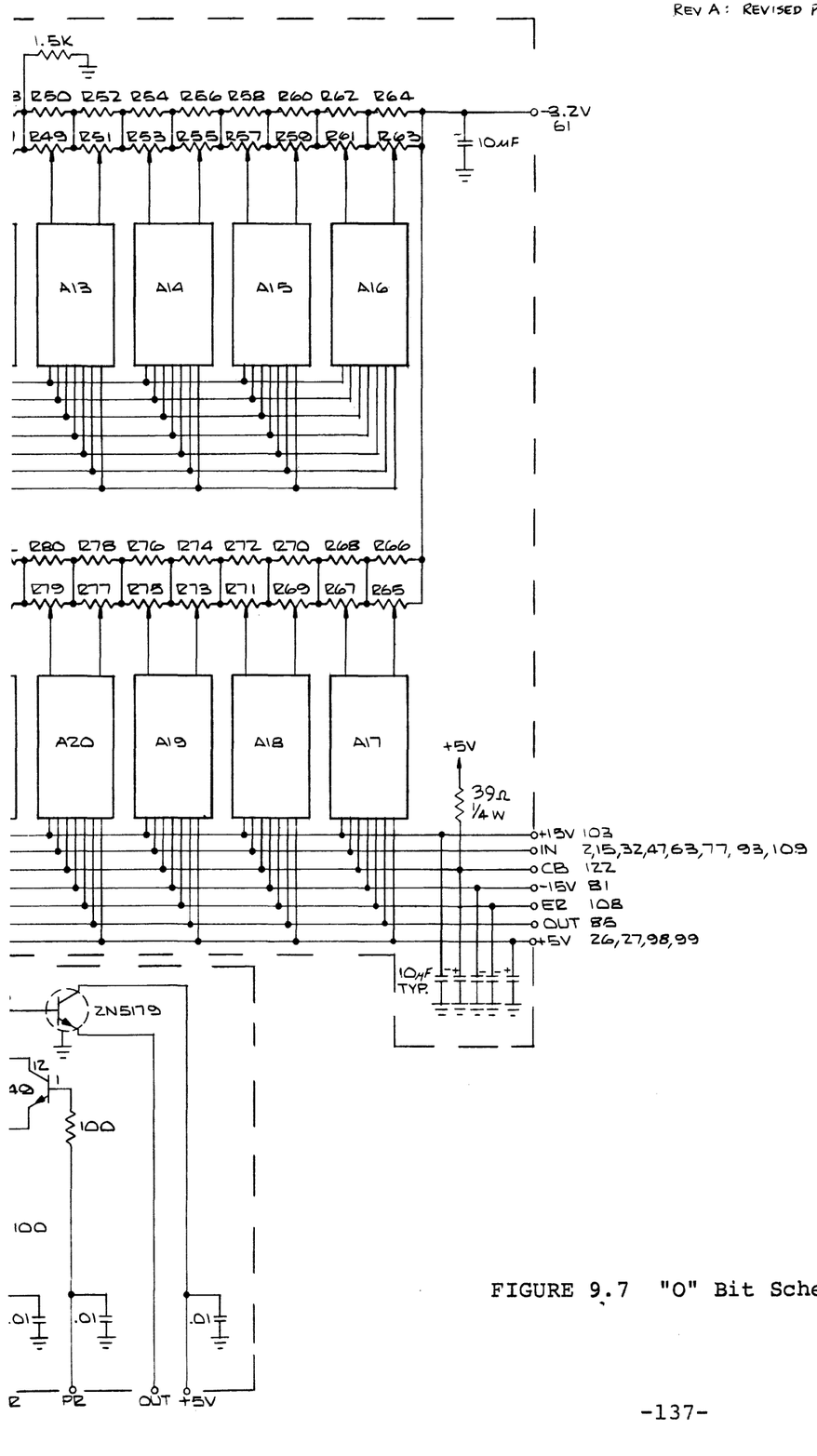
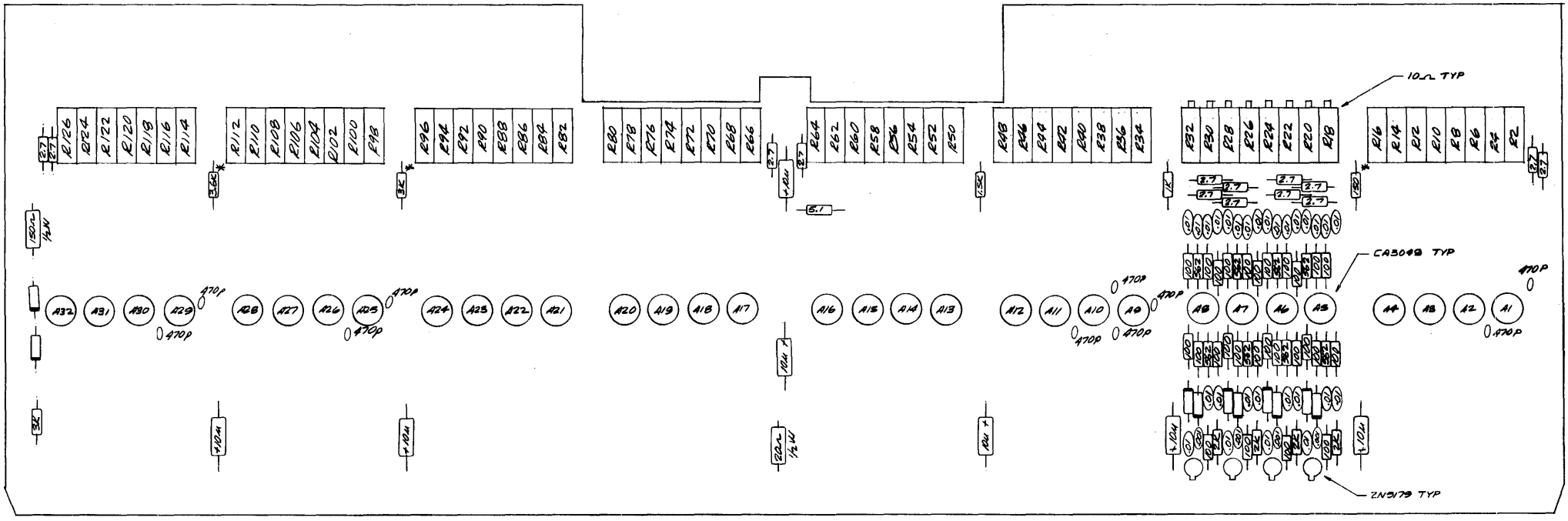


FIGURE 9.7 "O" Bit Schematic



NOTES-UNLESS OTHERWISE SPECIFIED:
1. DIODES ARE HEWLETT PACKARD 5082-2811
2. * FACTORY SELECTED VALUE 562Ω AND 2K ARE 1/8 WATT, 1% ALL OTHERS ARE 1/4 WATT, 5%

FIGURE 9.8 "1-6" Bit Converter Circuit Board Layout

REV A: REVISED PER ECO#062
11-30-77 SR

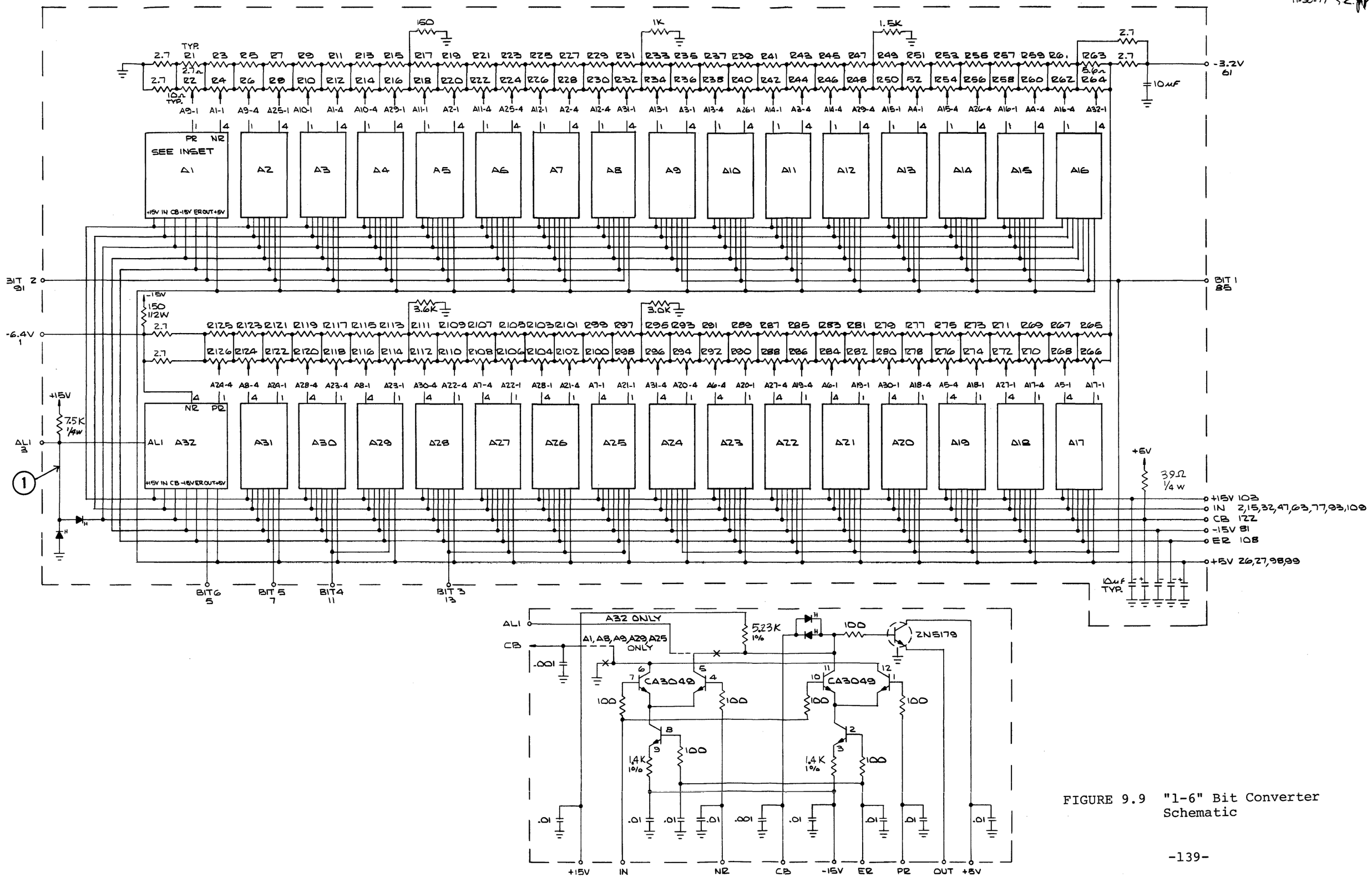
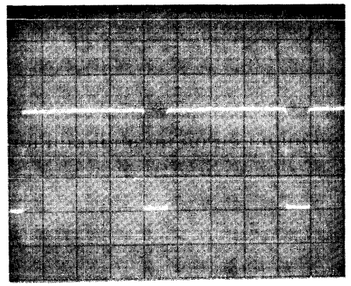
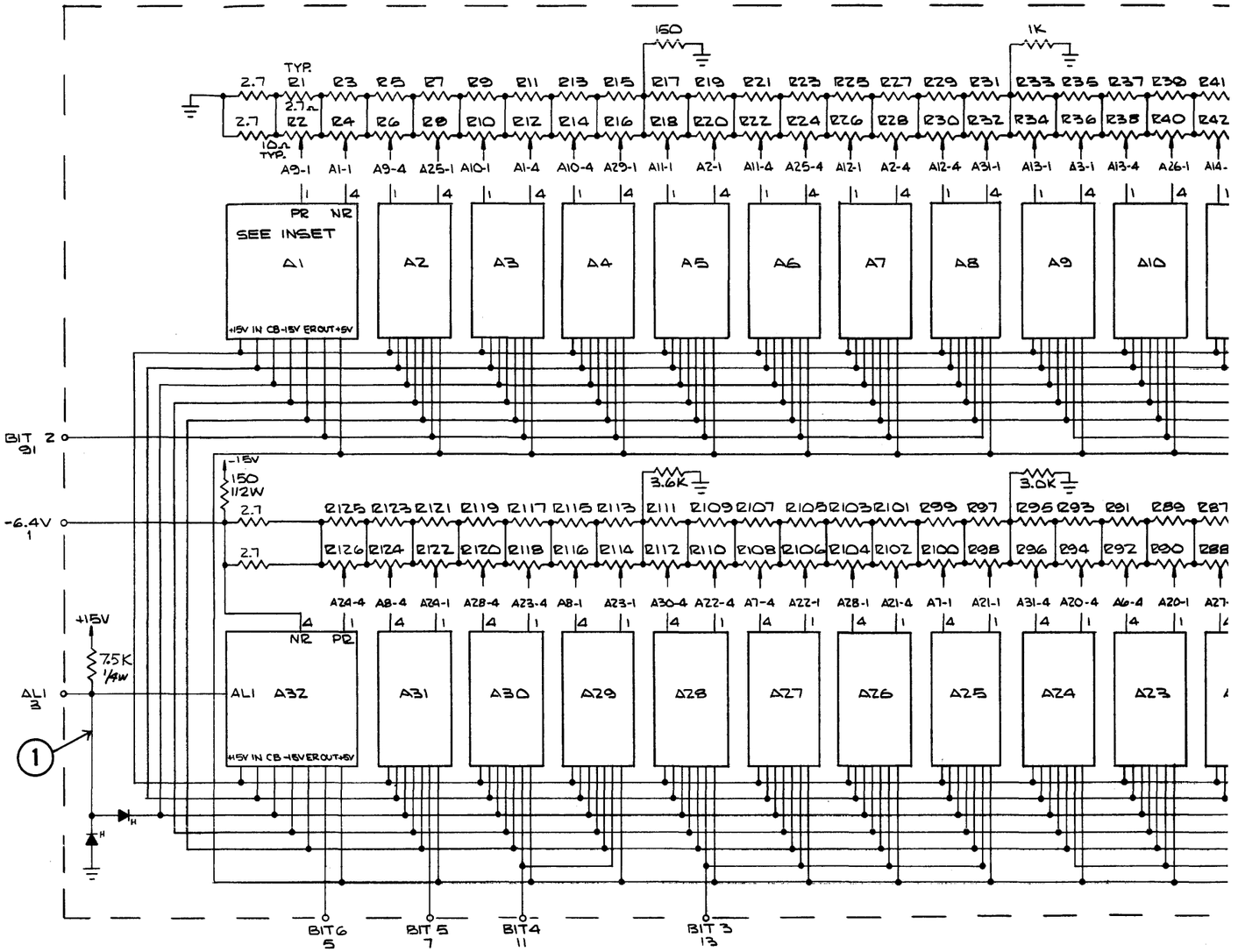


FIGURE 9.9 "1-6" Bit Converter Schematic



1. Scope: Vert 1V/div, Horz 50μ sec/div, Trigger external - generator sync
   8100: Input 5kHz Sine 11V PP, INPUT Range± 5V.



REV A: REVISED PER ECO#062
11-30-77 S.R.

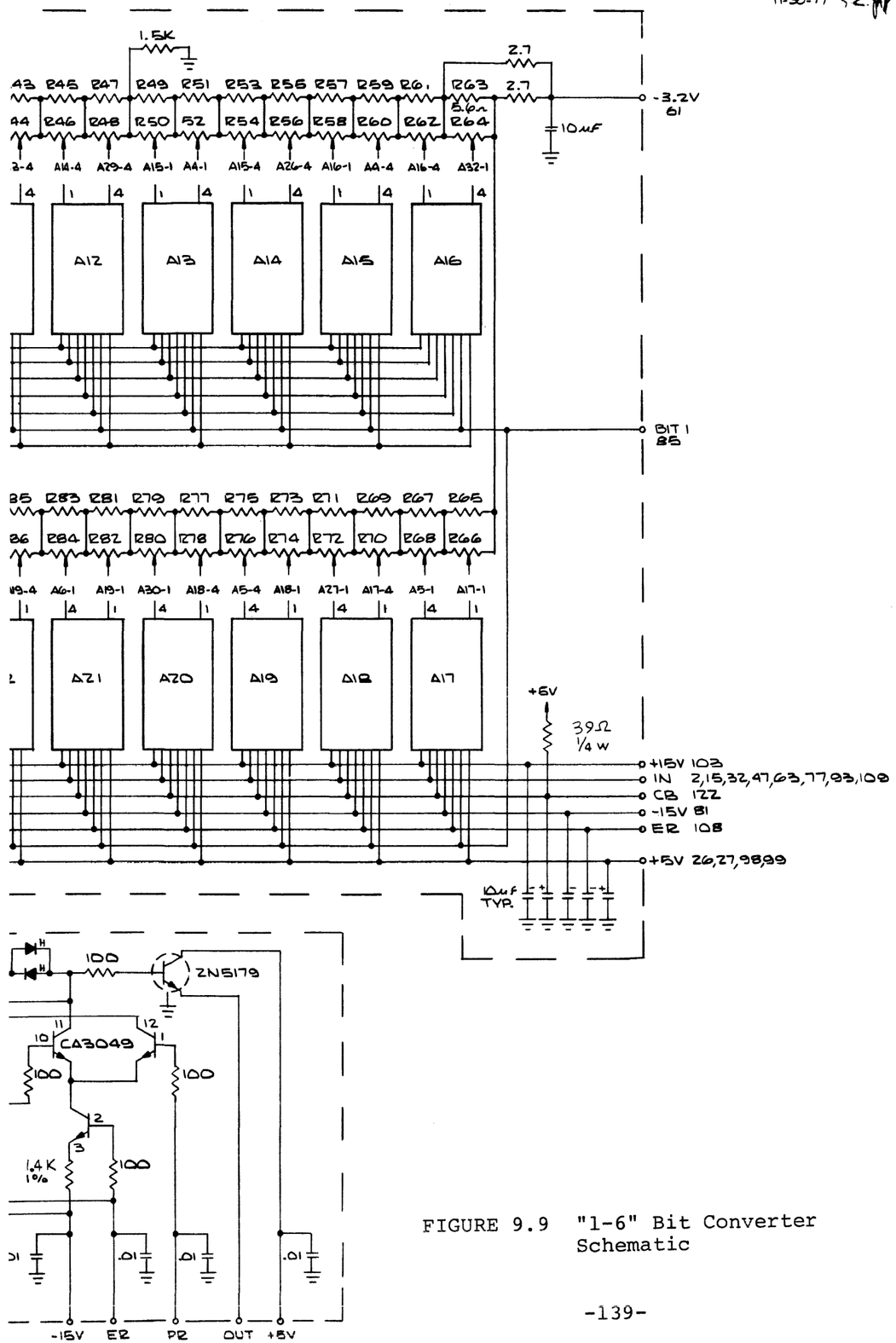


FIGURE 9.9 "1-6" Bit Converter Schematic

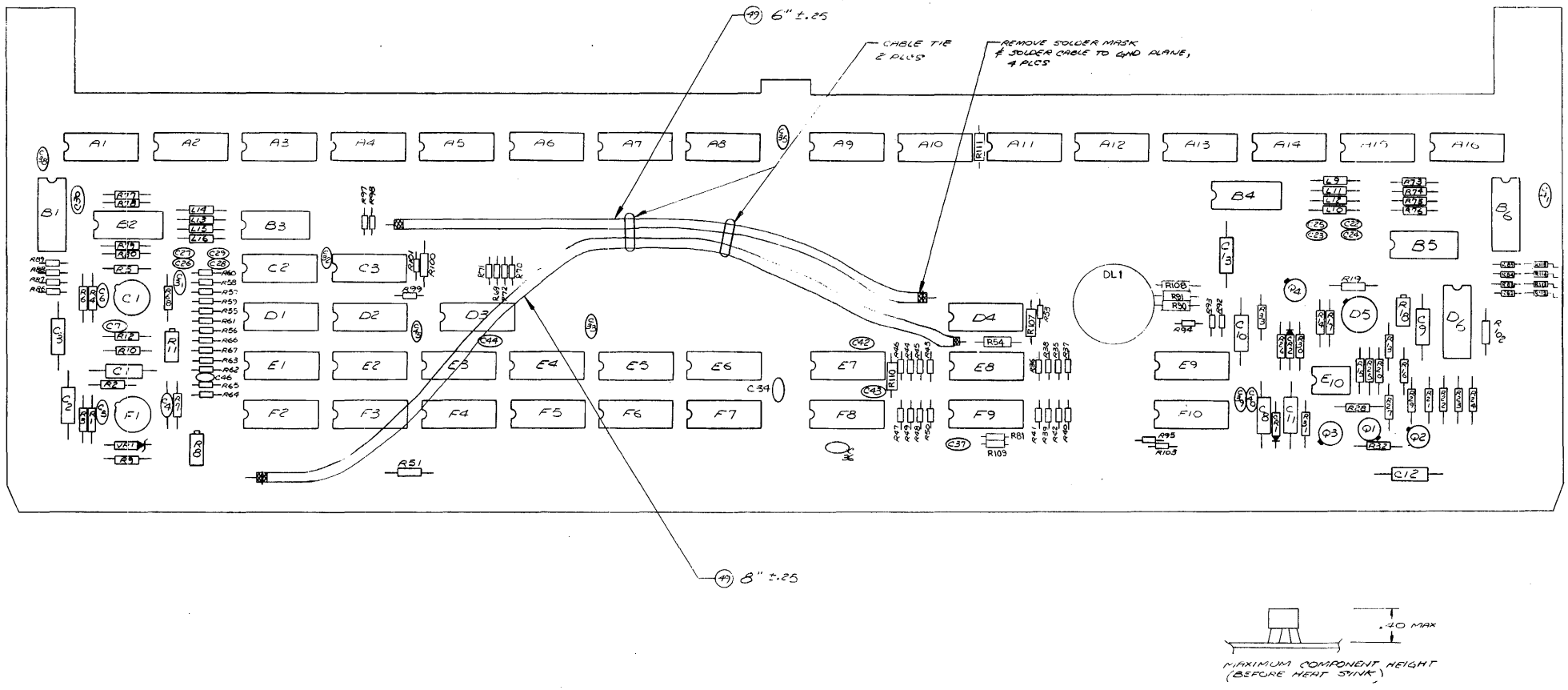
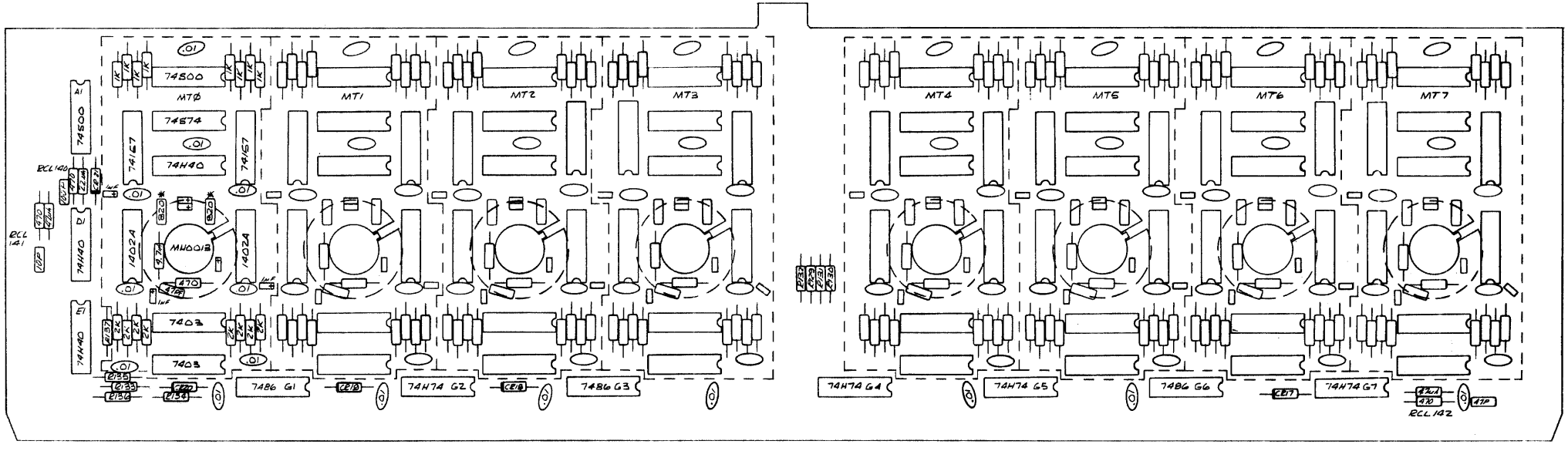
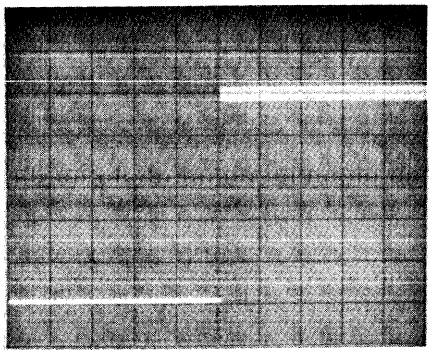


FIGURE 9.10 Pre Memory Circuit Board Layout

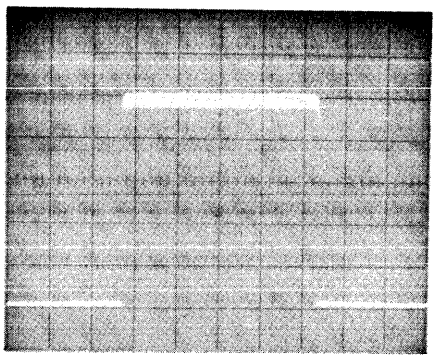


NOTES-UNLESS OTHERWISE SPECIFIED:
1. * VALUE SELECTED COMPONENT
2. RESISTORS ARE 1/4 WATT, 5%

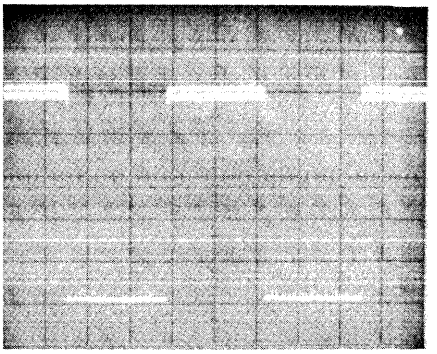
FIGURE 9.11 Post Memory Circuit Board Layout



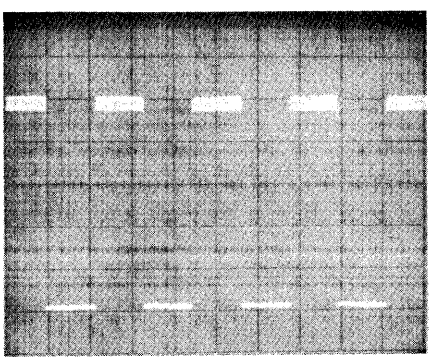
1. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: Input 5kHz triangle fullscale.



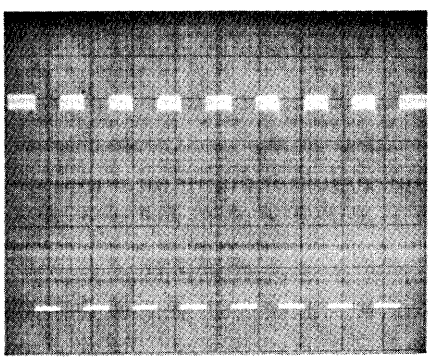
2. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



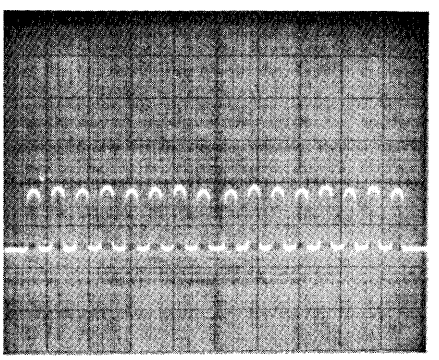
3. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



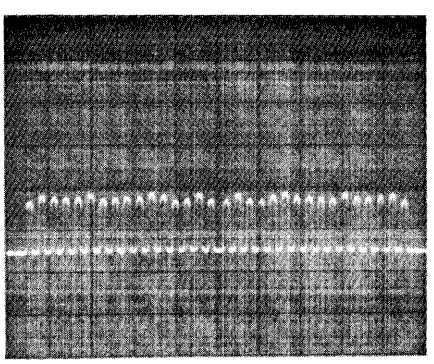
4. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



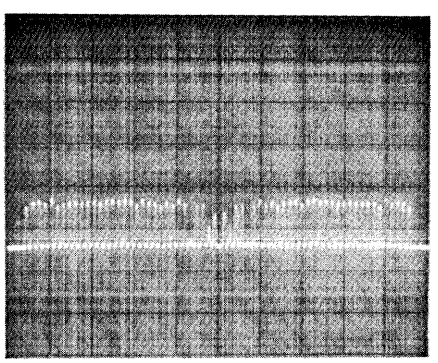
5. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



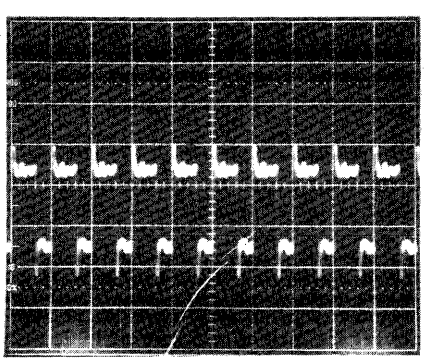
6. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



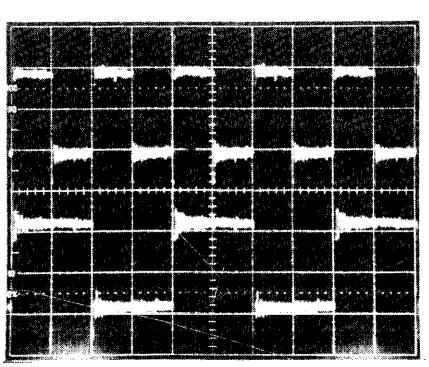
7. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



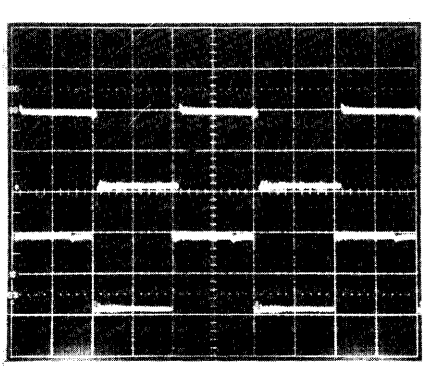
8. Scope: Vert 1V/div, Horz 10μsec/div, Trigger EXT on generator sync output. 8100: input 5kHz triangle fullscale.



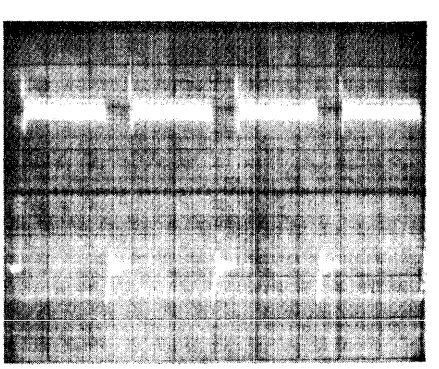
9. Scope: Vert 0.5V/div, Horz 0.1 μsec/div, Trigger Internal +, E8-9 at ECL.



10. Scope: Vert 0.5V/div, Horz 0.2 μsec/div, Trigger Internal, CH 2 (+), CH 1=F2 -11, CH 2=F2-14.

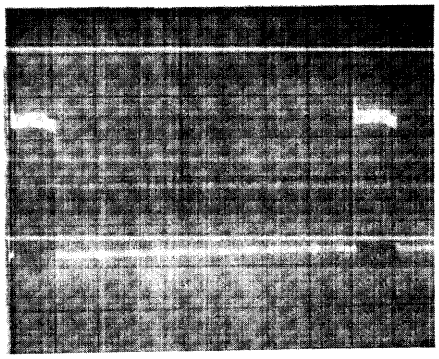


11. Scope: Vert 2V/div, Horz 0.2 μsec/div, Trigger Internal, CH 1 (+), CH 1=A1-9, CH 2 =B1-5.

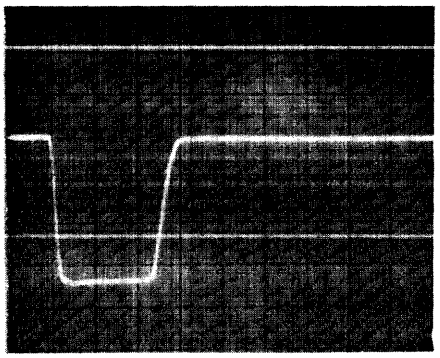


12. Scope: Vert 1V/div, Horz .2μsec/div, Trigger internal -/slope.

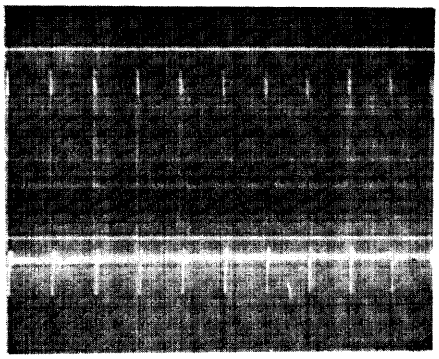
FIGURE 9.12A Signal Photos for the Memory Circuit Board



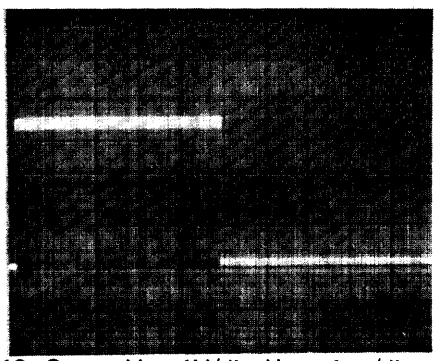
13. Scope: Vert 1V/div, Horz .5μsec/div,
Trigger internal +slope
8100: in display mode



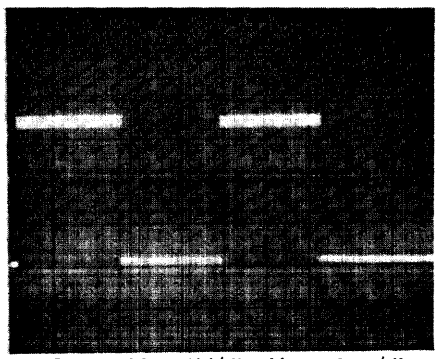
14. Scope: Vert 5V/div, Horz .05μsec/div,
Trigger: internal -slope
8100: in display mode.



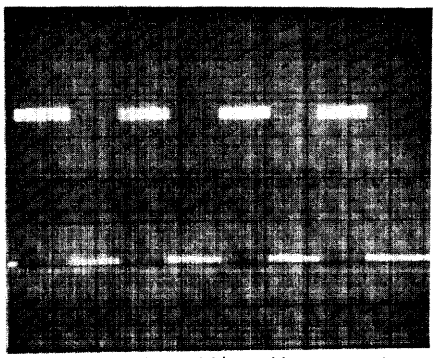
15. Scope: Vert 1V/div, Horz .5μsec/div,
Trigger: internal 3 3 +slope.
8100: in display mos mode.



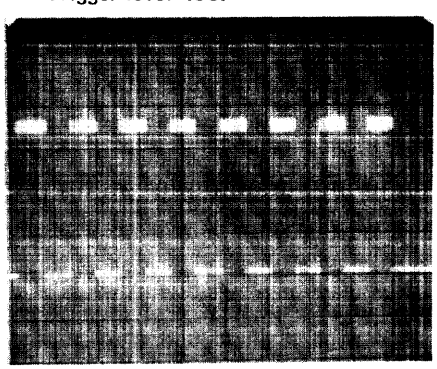
16. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



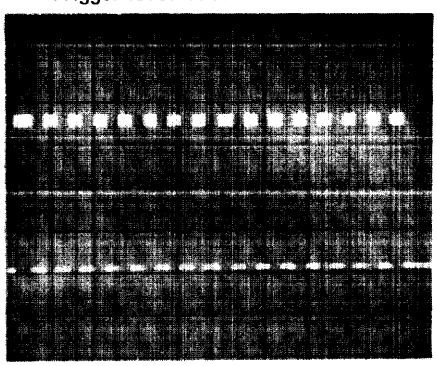
17. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



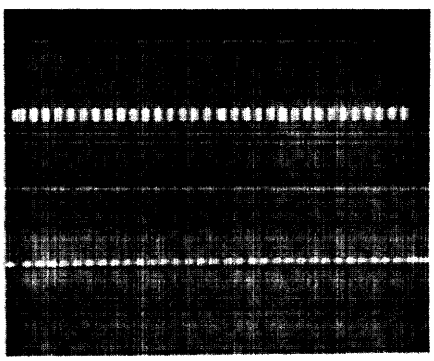
18. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



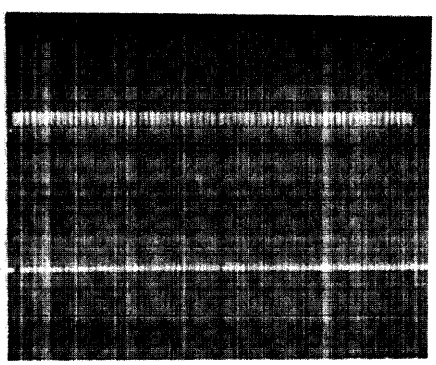
19. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



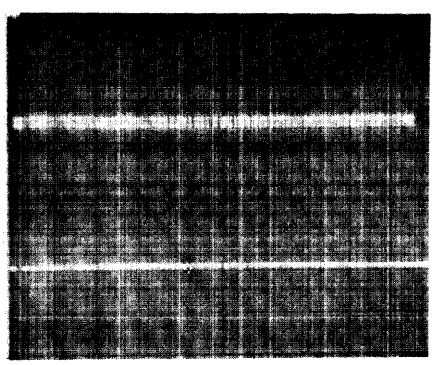
20. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



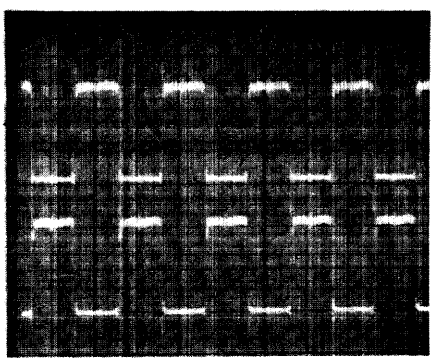
21. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale.
Sample interval .05μsec,
Trigger level -.95.



22. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



23. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 "Z" output.
8100: input 5kHz triangle fullscale,
Sample interval .05μsec,
Trigger level -.95.



24. Scope: Vert 2V/div, Horz .1 sec/div,
Trigger INT -slope CH A.
8100: CHA A - INPUT, CHA B -
CHA B - INPUT
Sample interval .1μsec.

REV B: INCORP. E.N. #623 8-18-77 mg
REV C: INCORP. E.N. #650 9-2-77 mg
NEW DRAWING - OBSOLETES 0810-0031.
REV D: ECO-0071 10-20-77 mg

TYPICAL CONNECTION FOR MTØ THRU MT7.

NOTE: THESE CONNECTIONS MATE WITH POST-MEMORY BD. - 0810-0026

TO MTØ & MT4 | TO MT1 & MT5 | TO MT2 & MT6 | TO MT3 | TO MT7

SEE NOTE #6

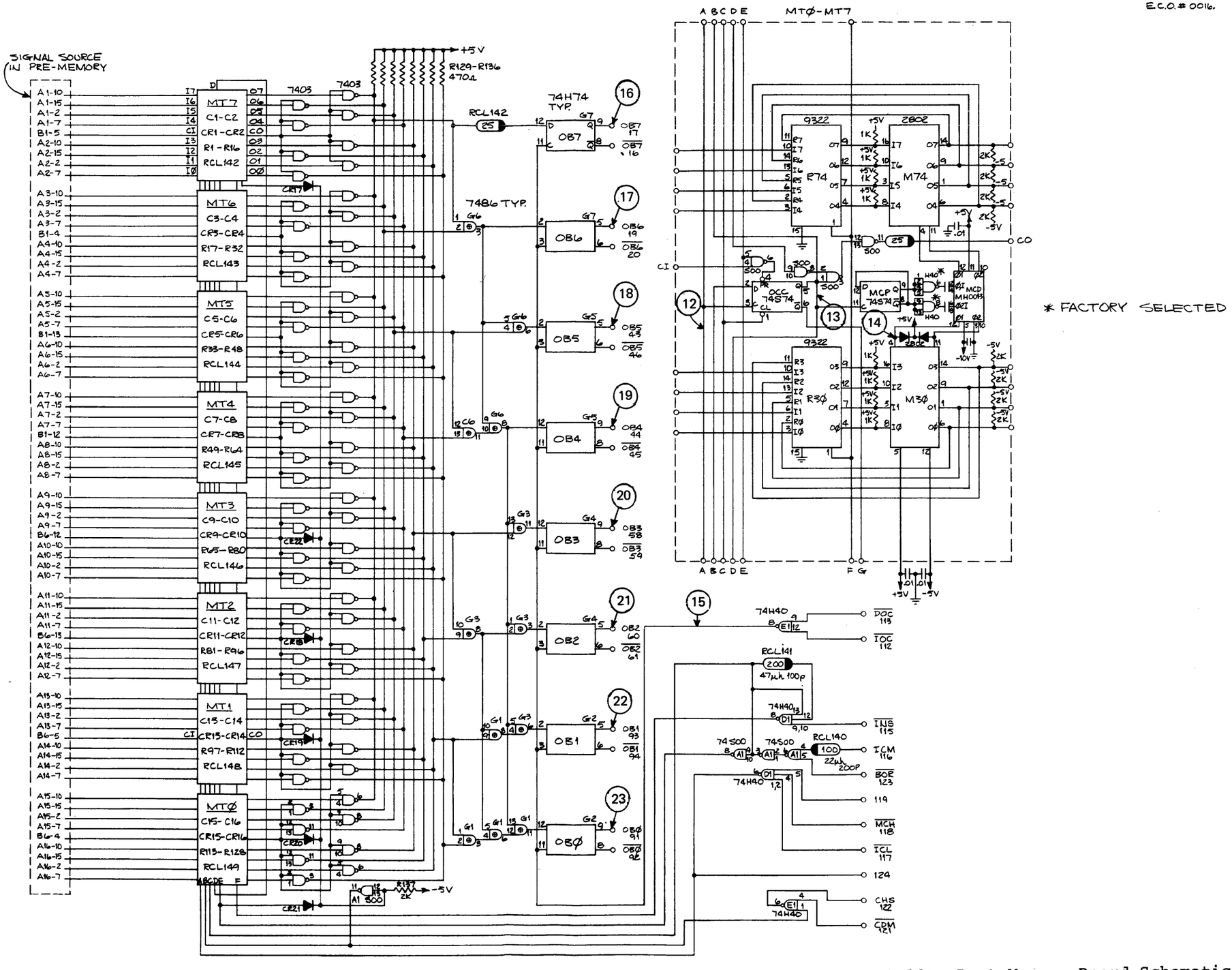
TO CI OF MTØ | TO CI OF MT4 | TO CI OF MT1 | TO CI OF MT5 | TO CI OF MT2 | TO CI OF MT6

NOTES:

1. C14-21 NORMALLY Ø.
2. L1-8 NORMALLY Ø.
3. ALL RESISTORS TO BE TERMINATED AT -5.2V UNLESS OTHERWISE SPECIFIED.
4. * FACTORY OPTION (RES. R97,98).
5. ALL RESISTORS 1/8W 5% UNLESS NOTED.
6. B2,B3,B4 & B5 ARE 74H04; B1 & B6 ARE 10125.
7. ↗ = TRIGGER

Figure 9.12A Prememory Board Schematic

REV A: NEW DRAWING - OBSOLETES 0B10-0031. ADDED CR22 FROM E.C.O.# 0016. 9-6-77 ng



* FACTORY SELECTED

Figure 9.12B Post-Memory Board Schematic

REV — PROTOTYPE
REV A - EN # 604 # 621

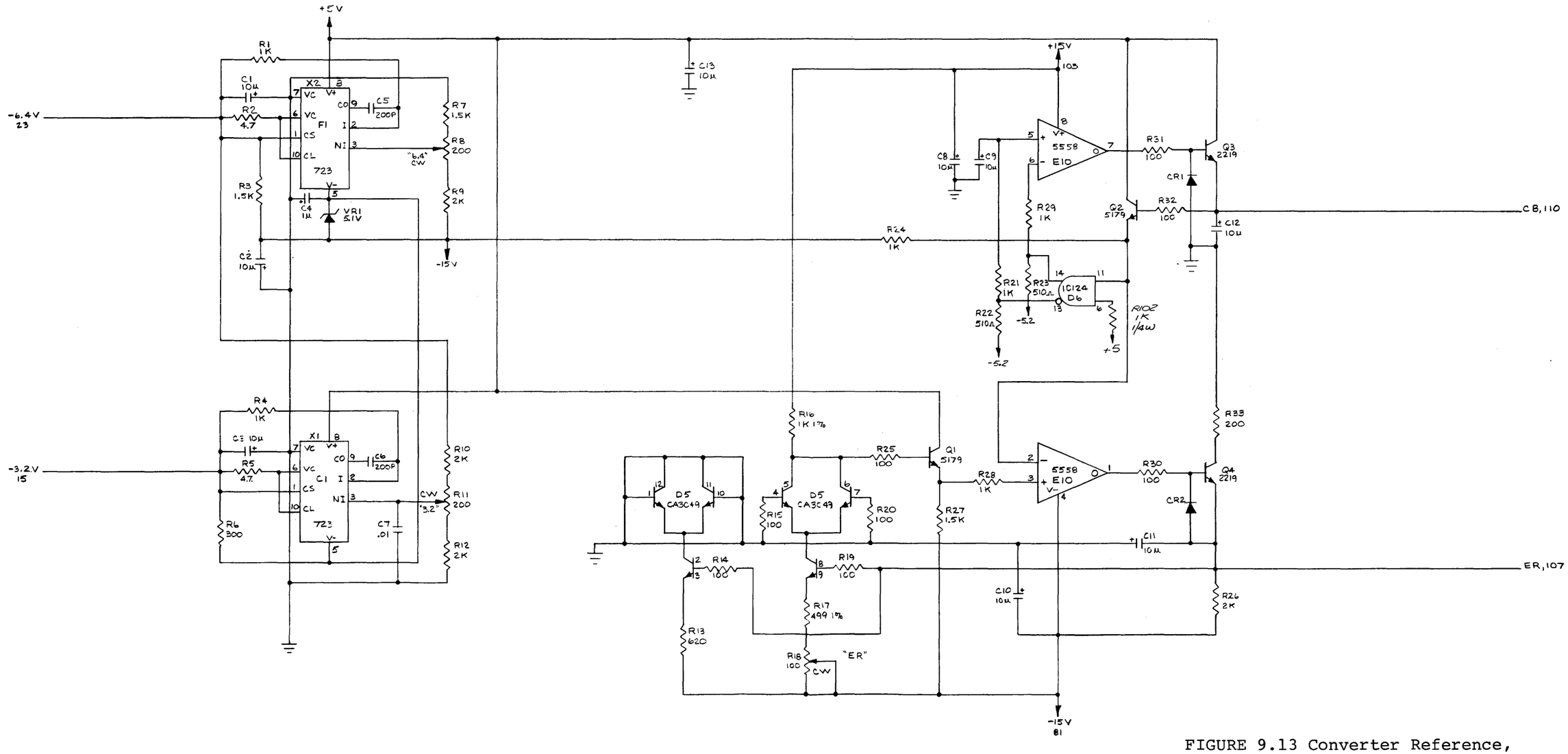
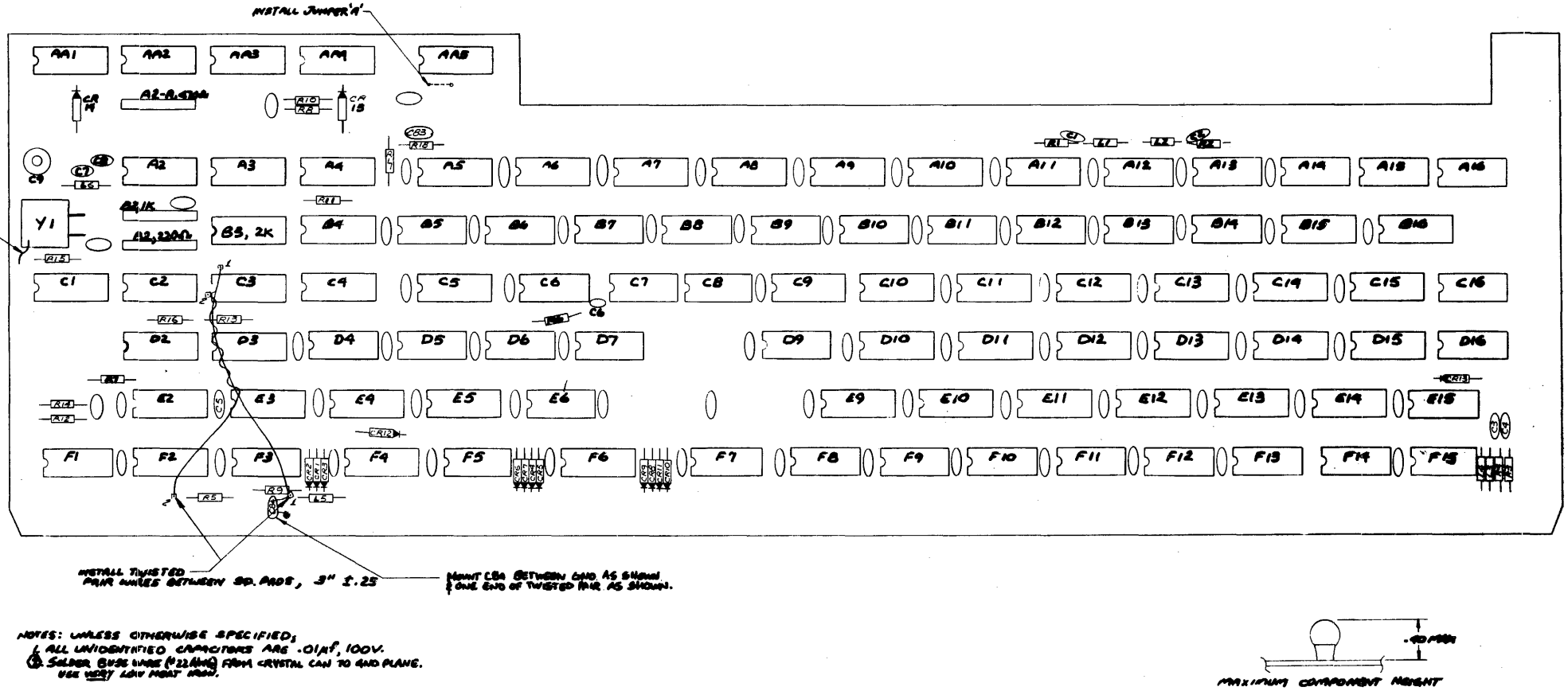
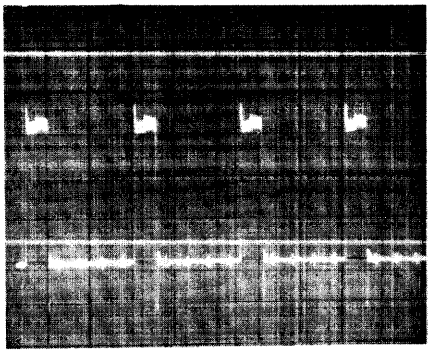


FIGURE 9.13 Converter Reference, Prememory Schematic

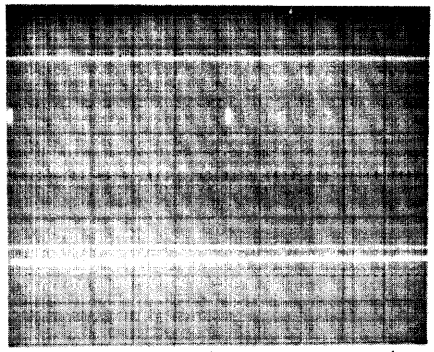


NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL UNIDENTIFIED CAPACITORS ARE .01μF, 100V.
2. SOLDER BUSS WIRE (#22 AWG) FROM CRYSTAL CAN TO GND PLANE. USE VERY LOW HEAT IRON.

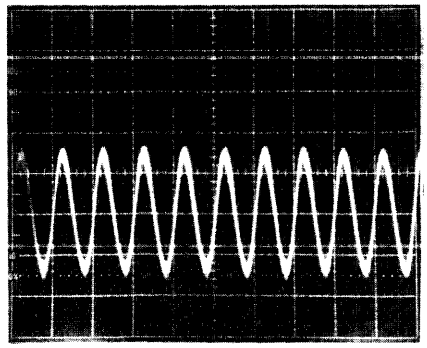
FIGURE 9.14 Time Base Circuit Board Layout



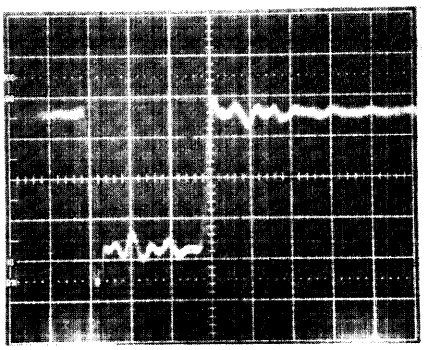
1. Scope: Vert 1V/div, Horz .2μsec/div, Trigger Internal +slope. 8100 in display mode.



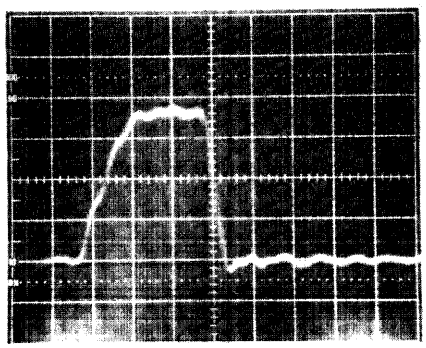
2. Scope: Vert 1V/div, Horz .2msec/div, Trigger Internal +slope. 8100 in display mode.



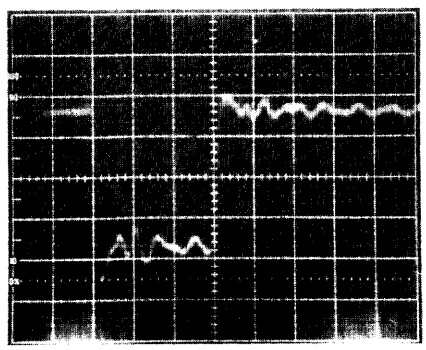
3. Scope: Vert 0.5V/div, Horz 0.01 μsec/div, Trigger Internal +.



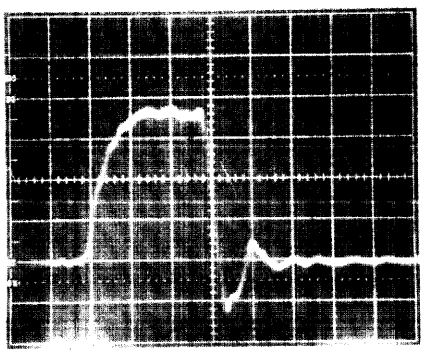
4. Scope: Vert 1V/div, Horz 0.02 μsec/div, Trigger Internal −, F12-11.
8100: ARM Group, INPUT/AUTO - AUTO
TRIGGER Group, INPUT/AUTO - AUTO



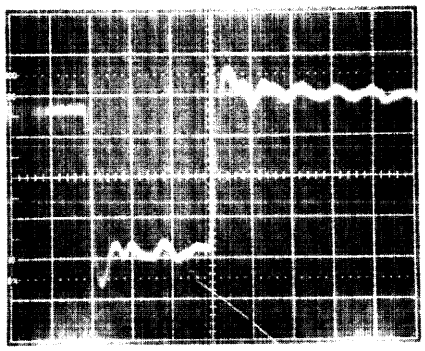
5. Scope: Vert 1V/div, Horz 0.02 μsec, Trigger Internal +, A12-6=DAP.
8100: ARM Group, INPUT/AUTO - AUTO;
TRIGGER Group, INPUT/AUTO - AUTO.



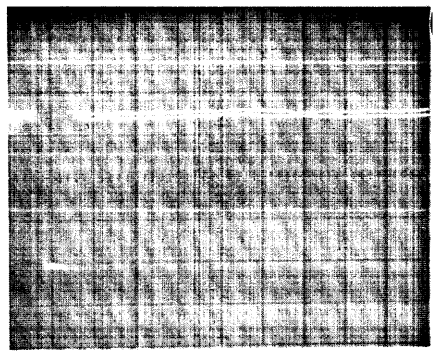
6. Scope: Vert 1V/div, Horz 0.02 μsec/div, Trigger Internal −, F12-8=TRP.
8100: ARM Group, INPUT/AUTO - AUTO;
TRIGGER Group, INPUT/AUTO - AUTO.



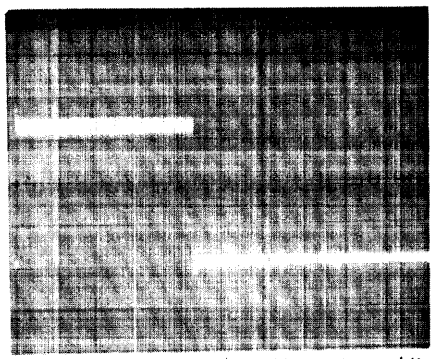
7. Scope: Vert 1V/div, Horz 0.02 μsec/div, Trigger Internal +, F7-9=DTP.
8100: ARM Group, INPUT/AUTO - AUTO;
TRIGGER Group, INPUT/AUTO - AUTO.



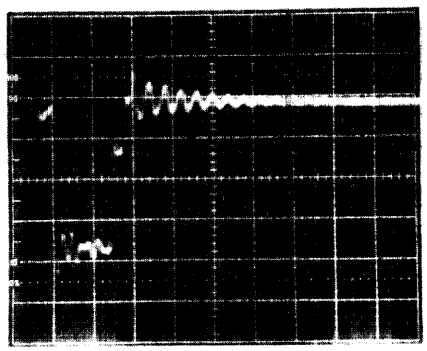
8. Scope: Vert 1V/div, Horz 0.02 μsec/div, Trigger Internal −, E15-4 Start.
Group, AUTO/INPUT - AUTO; TRIGGER Group, INPUT/AUTO - INPUT; Source - INT; Sample Interval 0.1 μsec: 51 kHz sine input signal.



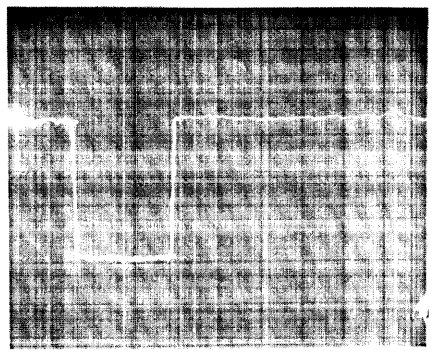
9. Scope: Vert 1V/div, Horz .1μsec/div, Trigger Internal -slope.
8100: Same as 8 except PRETRIG/NORM - PRETRIG.



10. Scope: Vert 1V/div, Horz .1μsec/div, Trigger Internal +slope. 8100: ARM Group, AUTO/INPUT- AUTO; TRIGGER Group, Source-INT; Sample Interval -.01μsec; 50kHz sine input signal.



11. Scope: Vert 1V/div, Horz 0.05 μsec/div, Trigger Internal −, F11-6=$\overline{\text{EOR}}$.



12. Scope: Vert 1V/div, Horz .1μsec/div, Trigger Internal -slope.
8100: same as 10.

FIGURE 9.15A Signal Photos for the Time Base Circuit Board

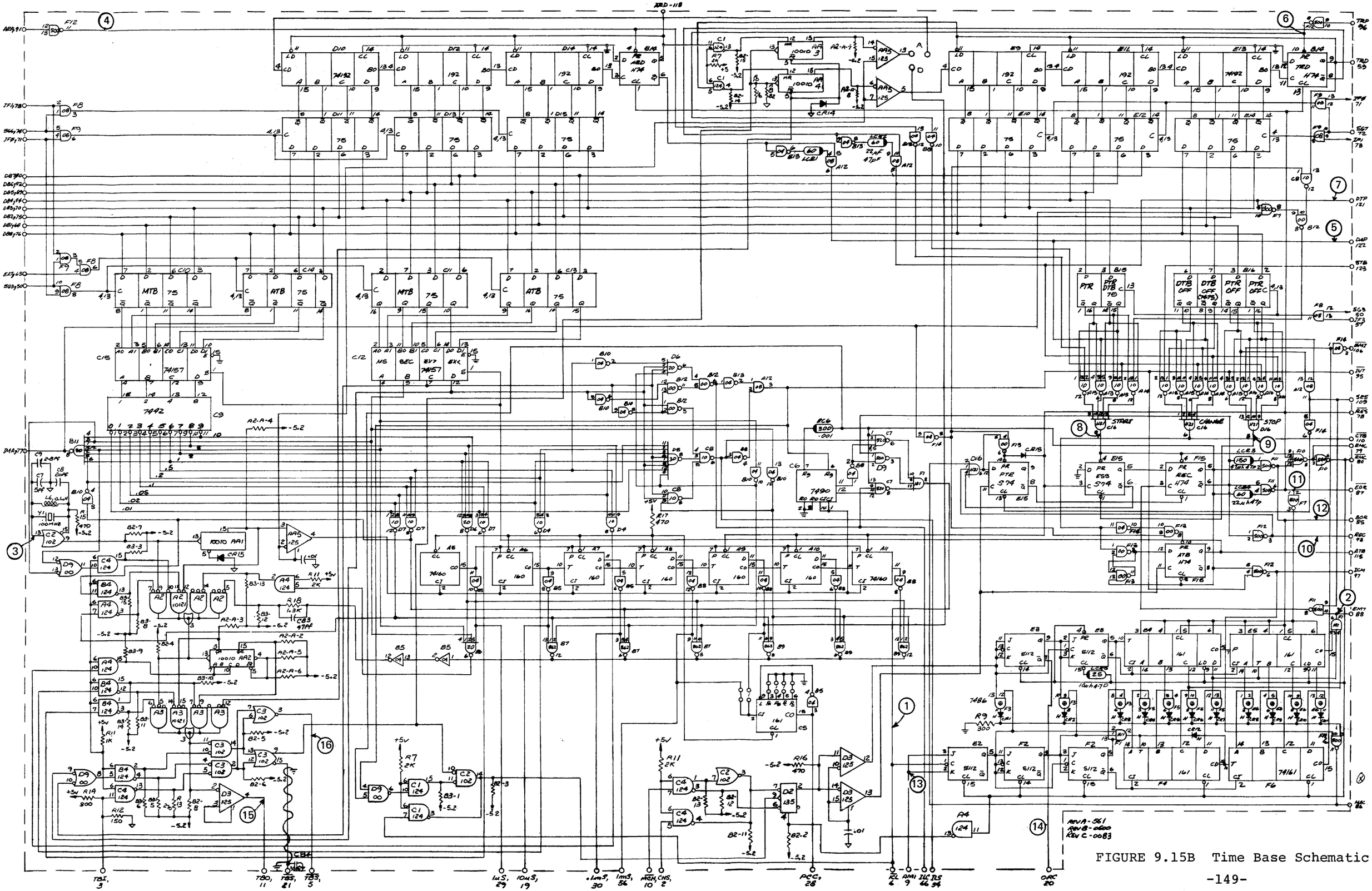
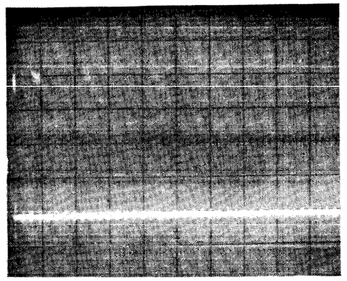
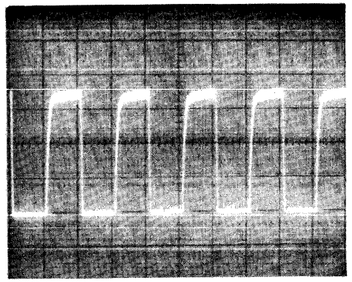


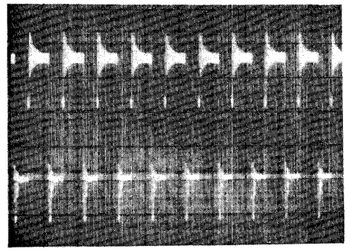
FIGURE 9.15B Time Base Schematic



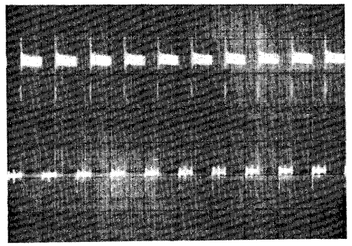
13. Scope: Vert 1V/div, Horz 2μsec/div, Trigger Internal + slope. 8100: ARM Group INPUT/AUTO-INPUT, TRIGGER Group INPUT/AUTO-INPUT; Mode - PRETRIG; Sample Interval - 1ms.



14. Scope: Vert 1V/div, Horz 1μsec/div, Trigger Internal - slope. 8100 in Display Mode.



15. Scope: Vert 1V/div, Horz .5μsec/div, Trigger Internal - slope. 8100: Sample Interval - .5μsec.



16. Scope: Vert 1V/div, Horz .5μsec/div, Trigger Internal - slope. 8100: Sample Interval - .5μsec.

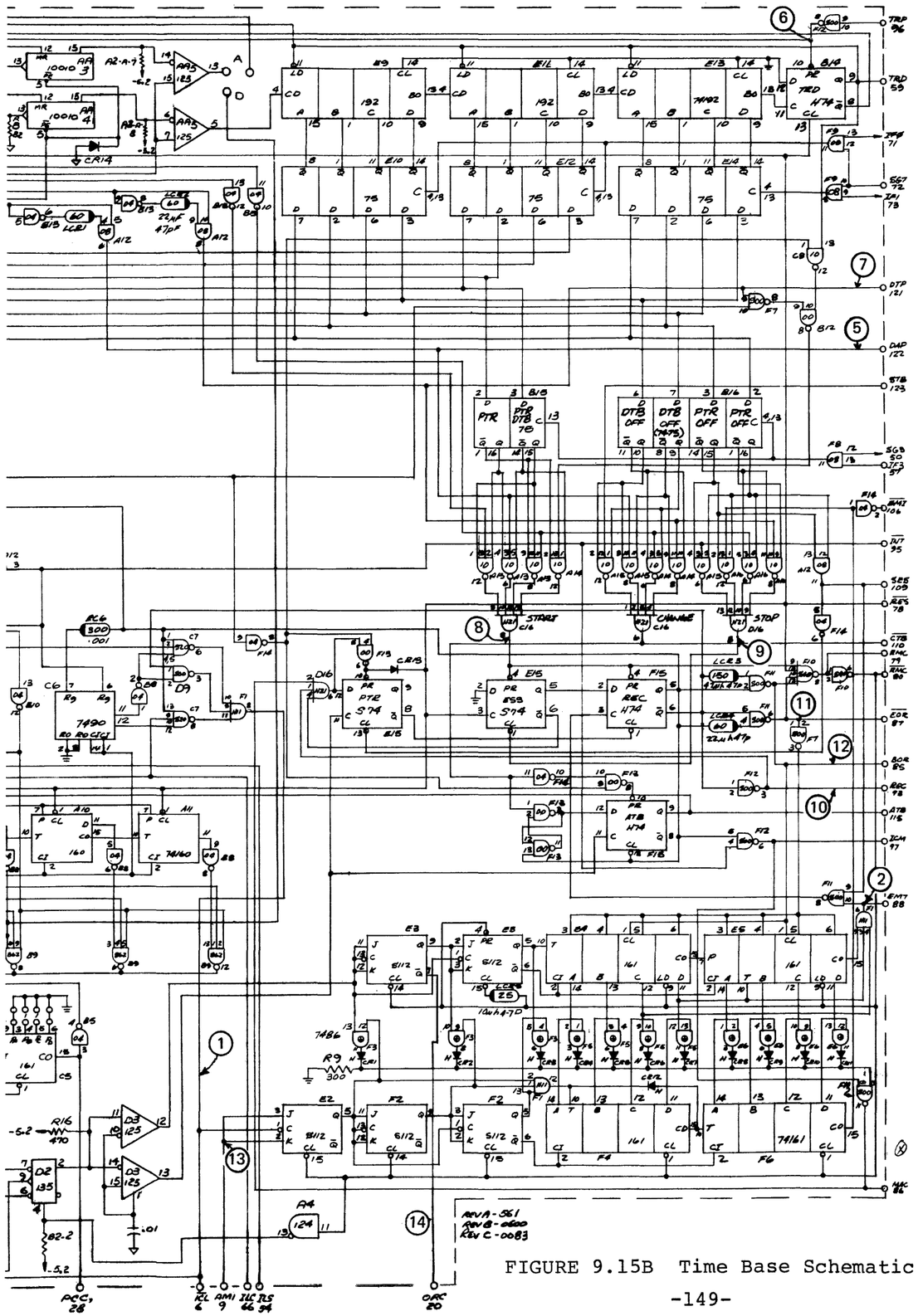
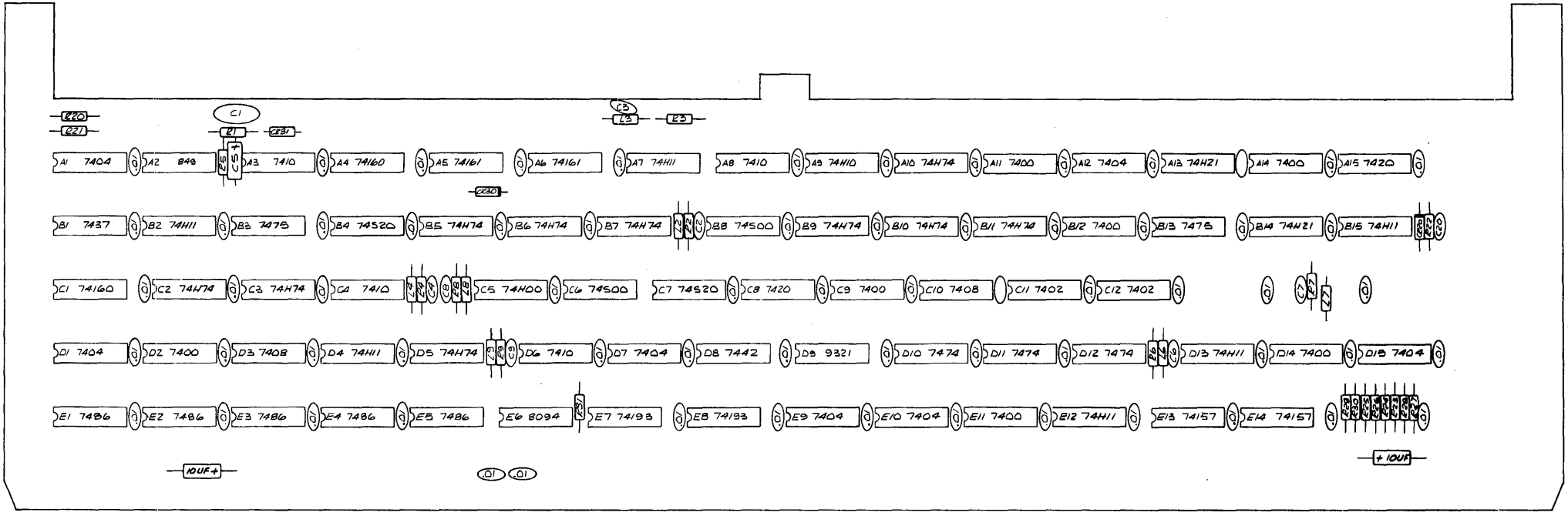


FIGURE 9.15B Time Base Schematic



NOTES - UNLESS OTHERWISE SPECIFIED:

1. RESISTORS ARE 1/4 WATT, 5%
2. DIODES ARE HEWLETT PACKARD 5082-2811

FIGURE 9.16 I/O Circuit Board Layout

.5msec,

5ms/div,

ol.

ms/div,

Arm,
ns.

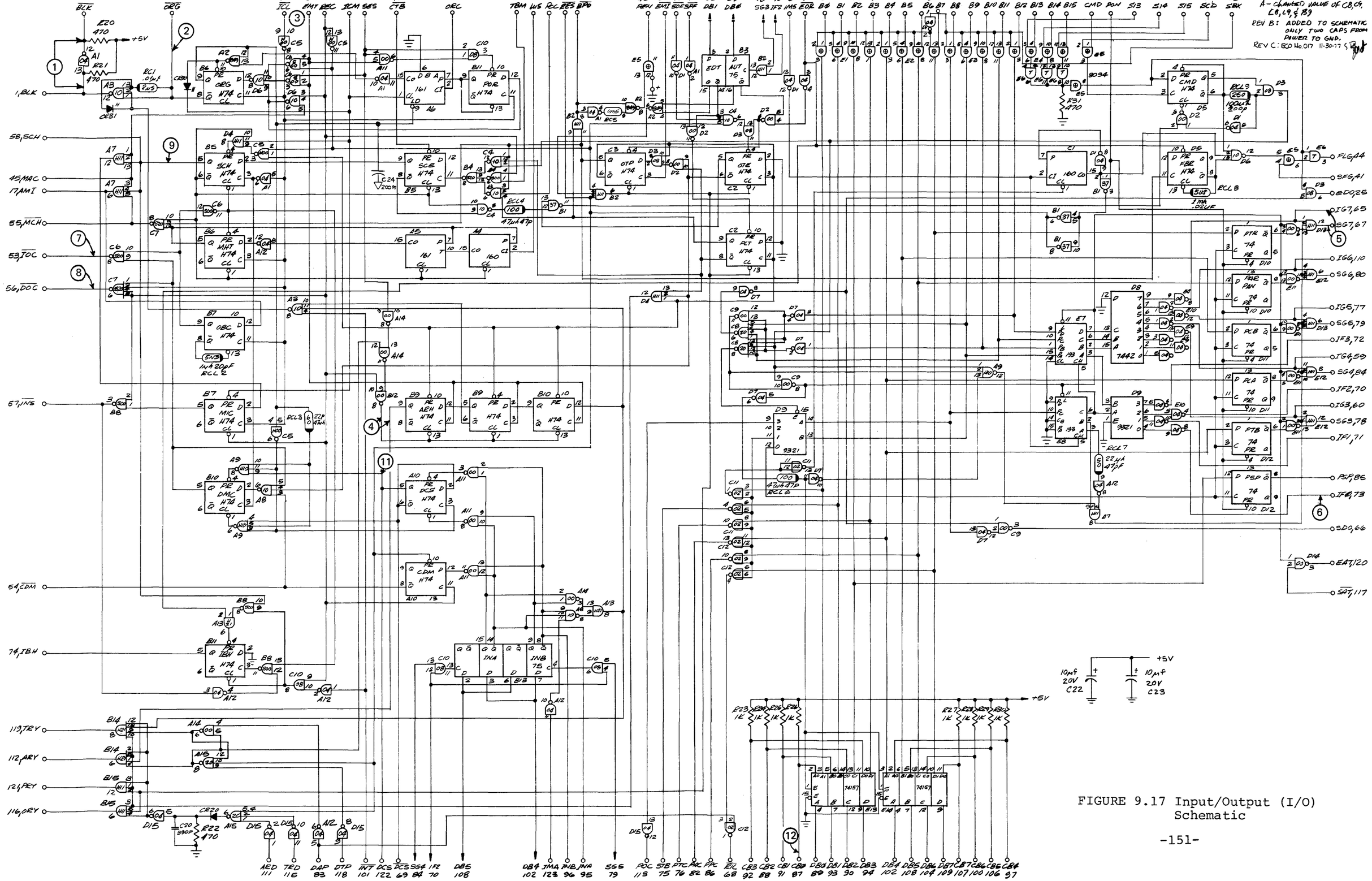
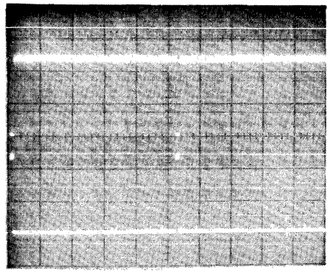
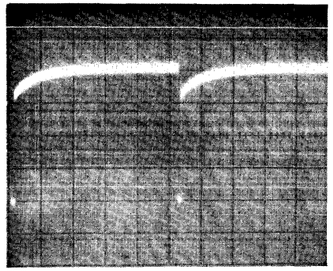


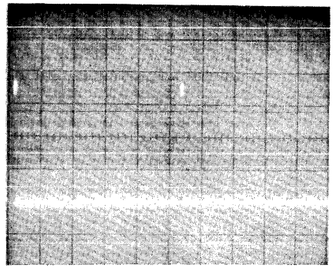
FIGURE 9.17 Input/Output (I/O) Schematic



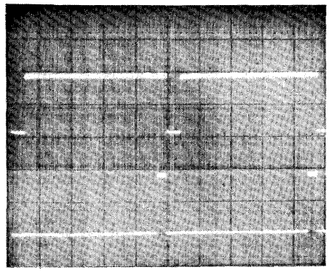
1. Scope: Vert 2V/div, Horz .2ms/div, Trigger Internal - slope. 8100 in display mode.



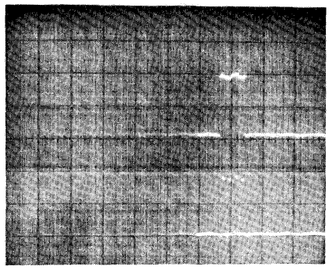
2. Scope: Vert 1V/div, Horz .2ms/div, Trigger Internal - slope. 8100 in display mode.



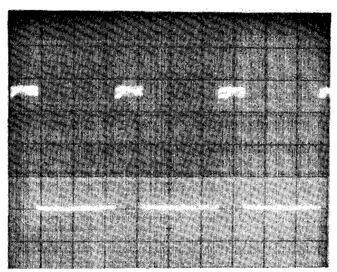
3. Scope: Vert 1V/div, Horz .5msec, Trigger Internal + slope. 8100 in display mode.



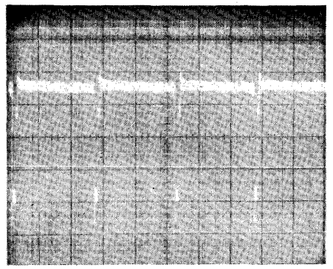
4. Scope: Vert 1V/div, Horz .5msec, Trigger Internal - slope (B12 pin 8). 8100: Normal mode, Auto arm, Trig int, Sample interval .1μsec.



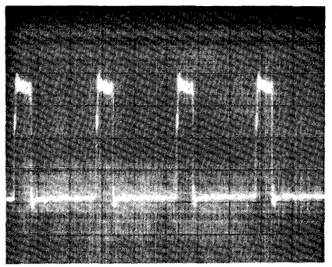
5. Scope: Vert 2V/div, Horz 20ms/div, Trigger Internal + slope. 8100: in Front Panel Control.



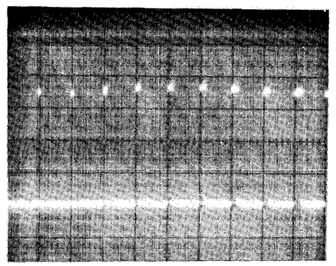
6. Scope: Vert 1V/div, Horz 5ms/div, Trigger Internal + slope. 8100: in Front Panel Control.



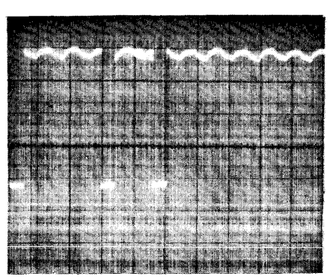
7. Scope: Vert 1V/div, Horz .2μsec/div, Trigger Internal - slope. 8100: Display Mode.



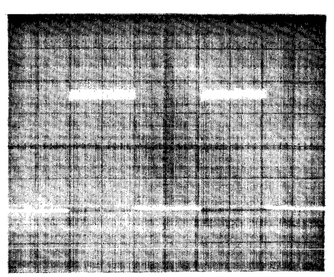
8. Scope: Vert 1V/div, Horz 2μsec, Trigger Internal + slope. 8100: Normal mode, Auto Arm, Trig int, Sample interval 1ms.



9. Scope: Vert 1V/div, Horz 1ms/div, Trigger Internal - slope. 8100: Normal mode, Auto Arm, Trig int, Sample interval 1ms.



10. Scope: Vert 1V/div, Horz 10ms/div, Trigger Internal - slope. Typical, "CB" signal pulses will vary with settings of Front Panel Controls.



11. Scope: Vert 1V/div, Horz .5ms, Trigger Internal - slope. 8100: CHAN A INPUT , CHAN B INPUT and in display mode.

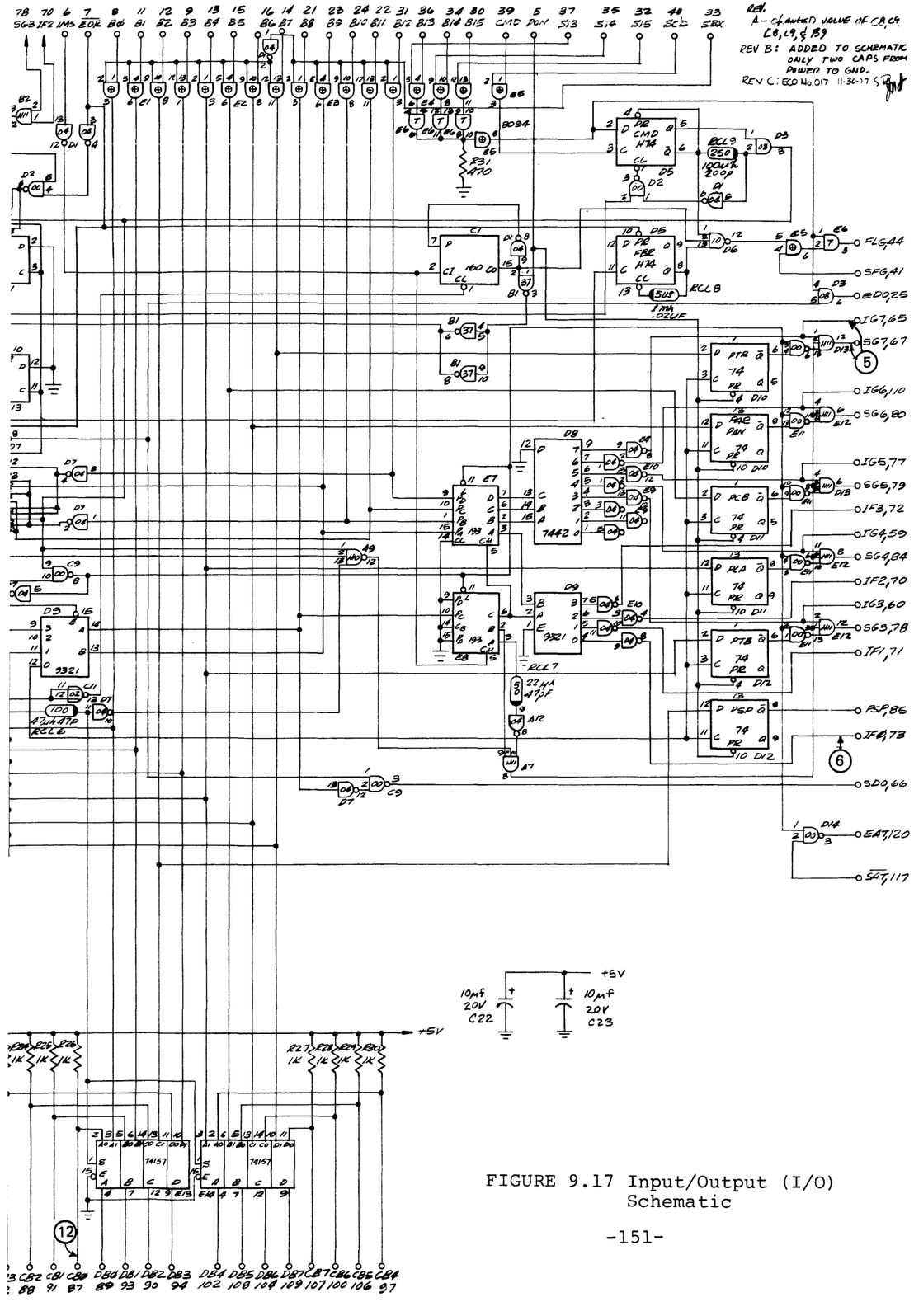
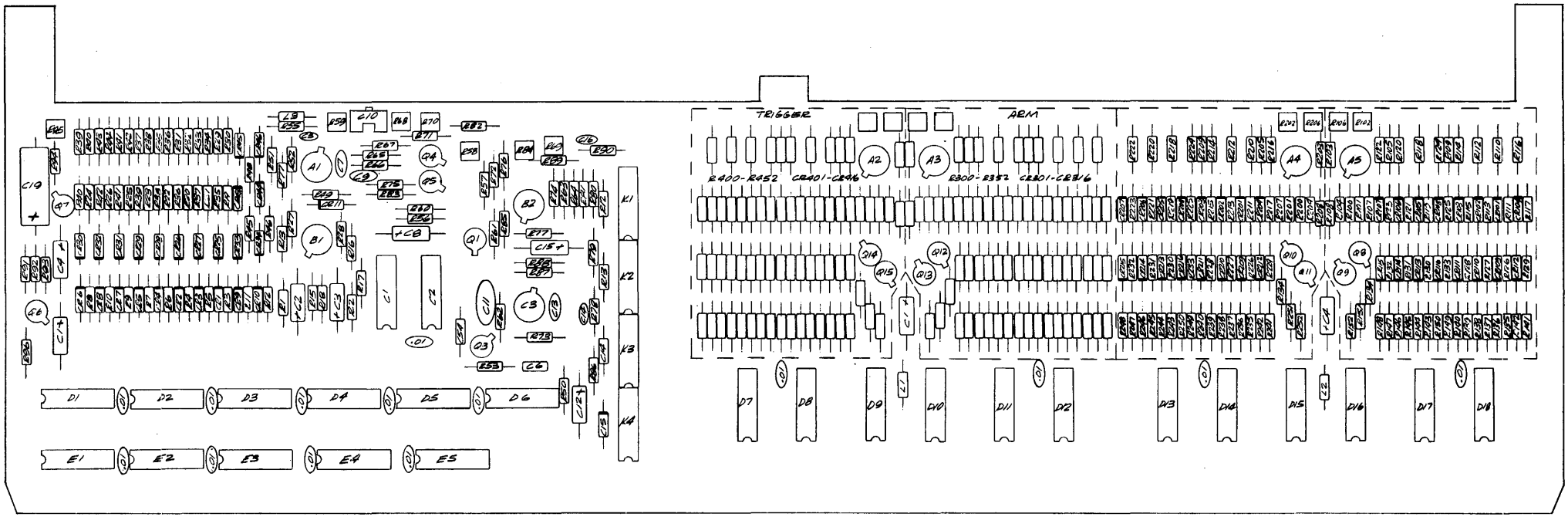
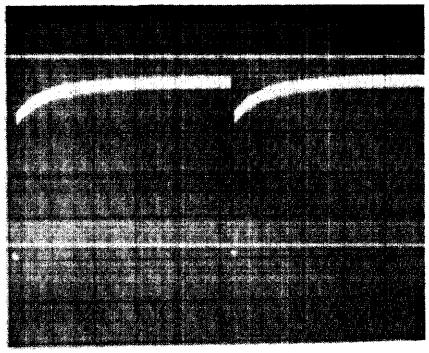


FIGURE 9.17 Input/Output (I/O) Schematic

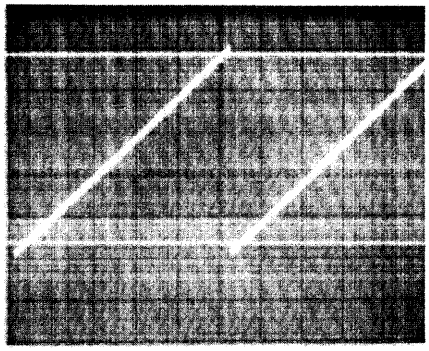


NOTES-UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/4WATT, 5%
2. DIODES ARE HEWLETT PACKARD 6082-2811

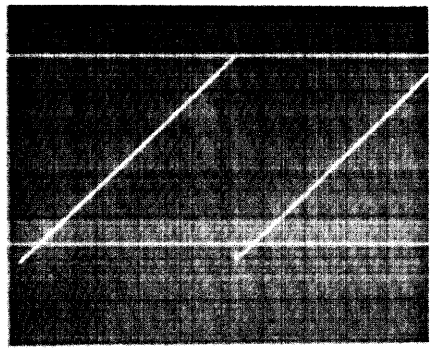
FIGURE 9.18 D/A Circuit Board Layout



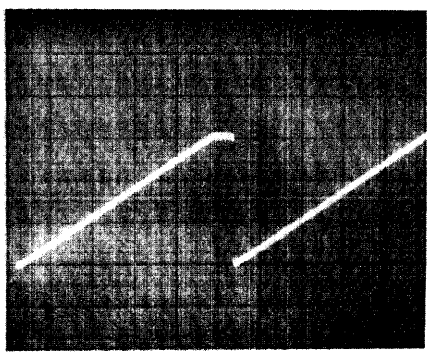
1. Scope: Vert 1V/div, Horz .2ms/div
Trigger Internal - slope.
8100: in display mode.



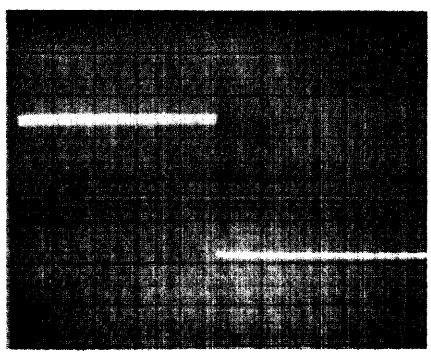
2. Scope: Vert .2V/div, Horz .2ms/div,
Trigger EXT on 8100 Z output.
8100: in display mode.



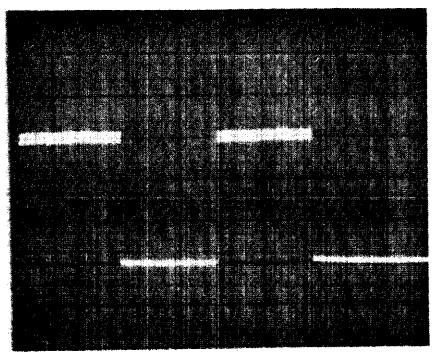
3. Scope: Vert 2V/div, Horz .2ms/div
Trigger EXT on 8100 Z output.
8100: in display mode.



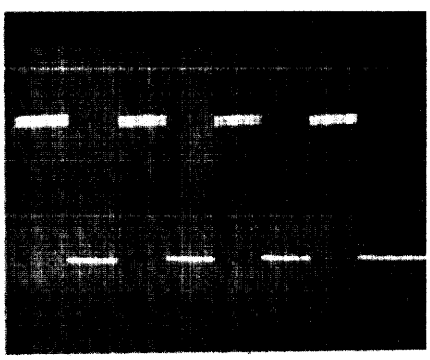
4. Scope: Vert .5V/ div, Horz .2ms/div,
Trigger EXT on 8100 Z output
8100: Input 5 kHz triangle fullscale,
Sample interval .05μ sec, Trigger level -.95.



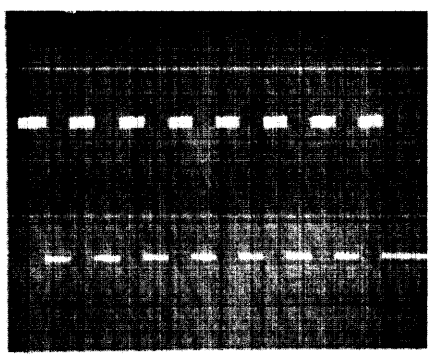
5. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level -.95.



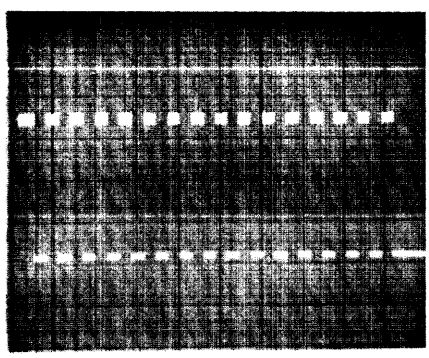
6. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level -.95.



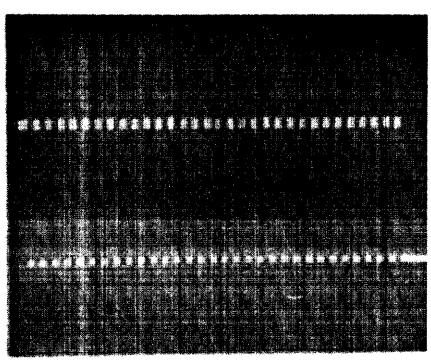
7. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level -.95.



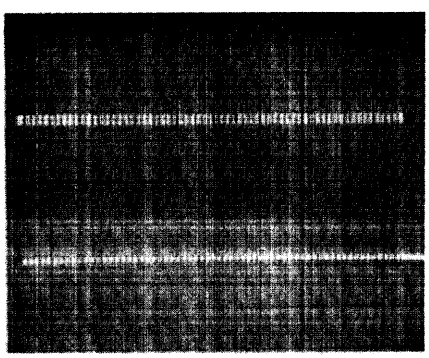
8. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level -.95.



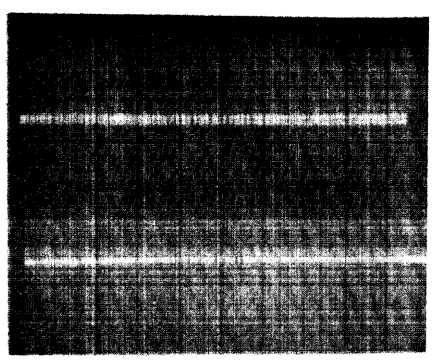
9. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level -.95.



10. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale
Sample interval .05μsec, Trigger level
-.95.



11. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale,
Sample interval .05μsec, Trigger level
-.95.



12. Scope: Vert 1V/div, Horz .1ms/div,
Trigger EXT on 8100 Z output.
8100: Input 5kHz triangle fullscale
Sample interval .05μsec, Trigger level
-.95.

FIGURE 9.19A Photos of D/A Board Signals

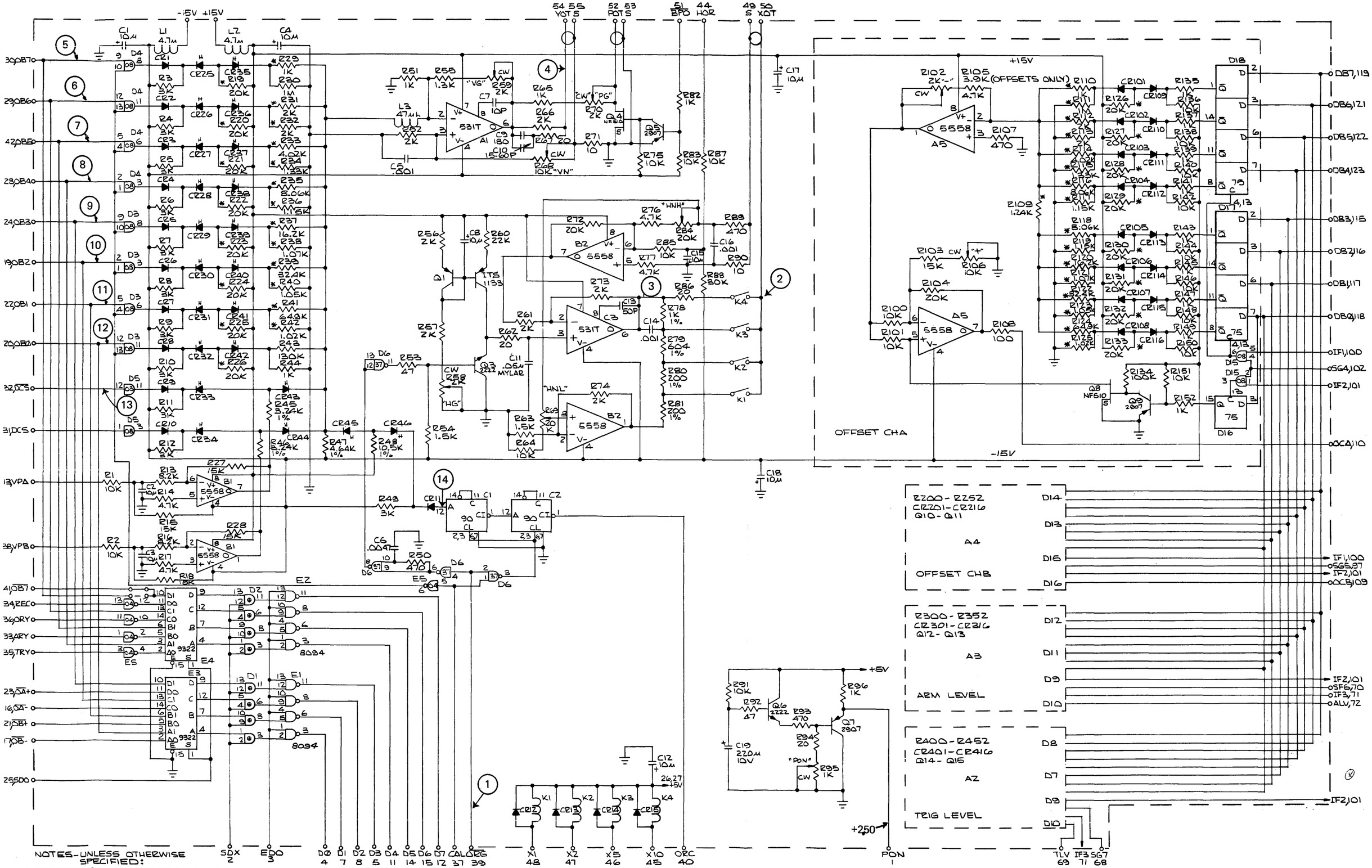
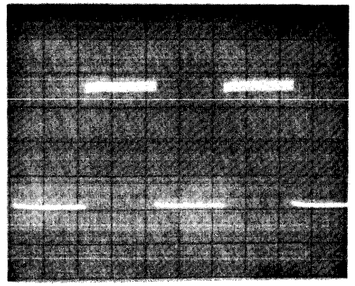
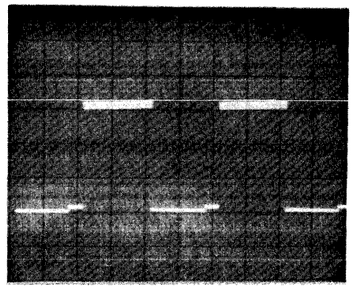


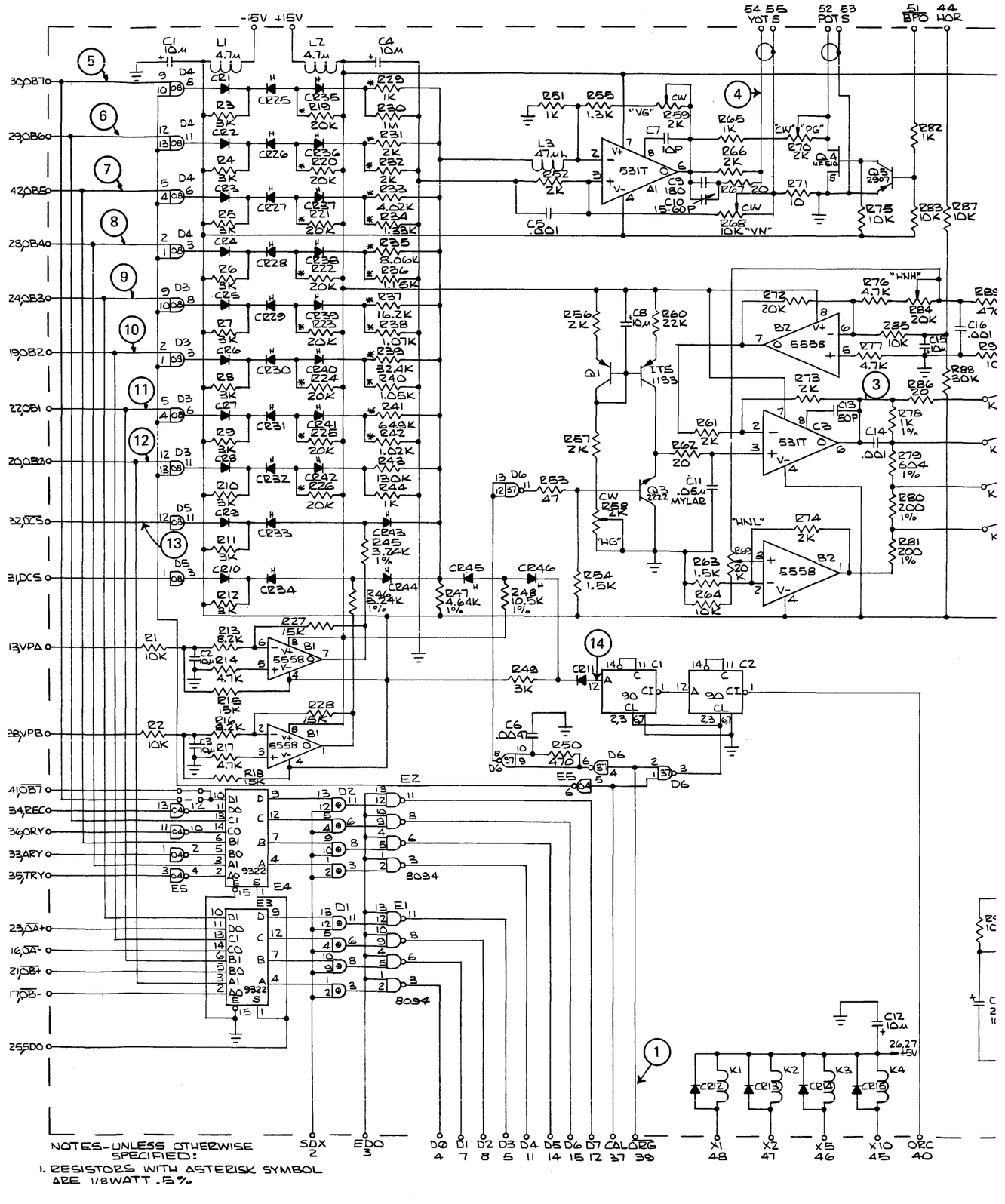
FIGURE 9.19B D/A Board Schematic



13. Scope: Vert 1V/div, Horz .5ms/div, Trigger INT - slope.
8100: CHA A - INPUT, CHA B - INPUT, and in display mode.



14. Scope: Vert 1V/div, Horz 50μsec/div, Trigger internal - slope.
8100 in display mode, CAL button pressed in.



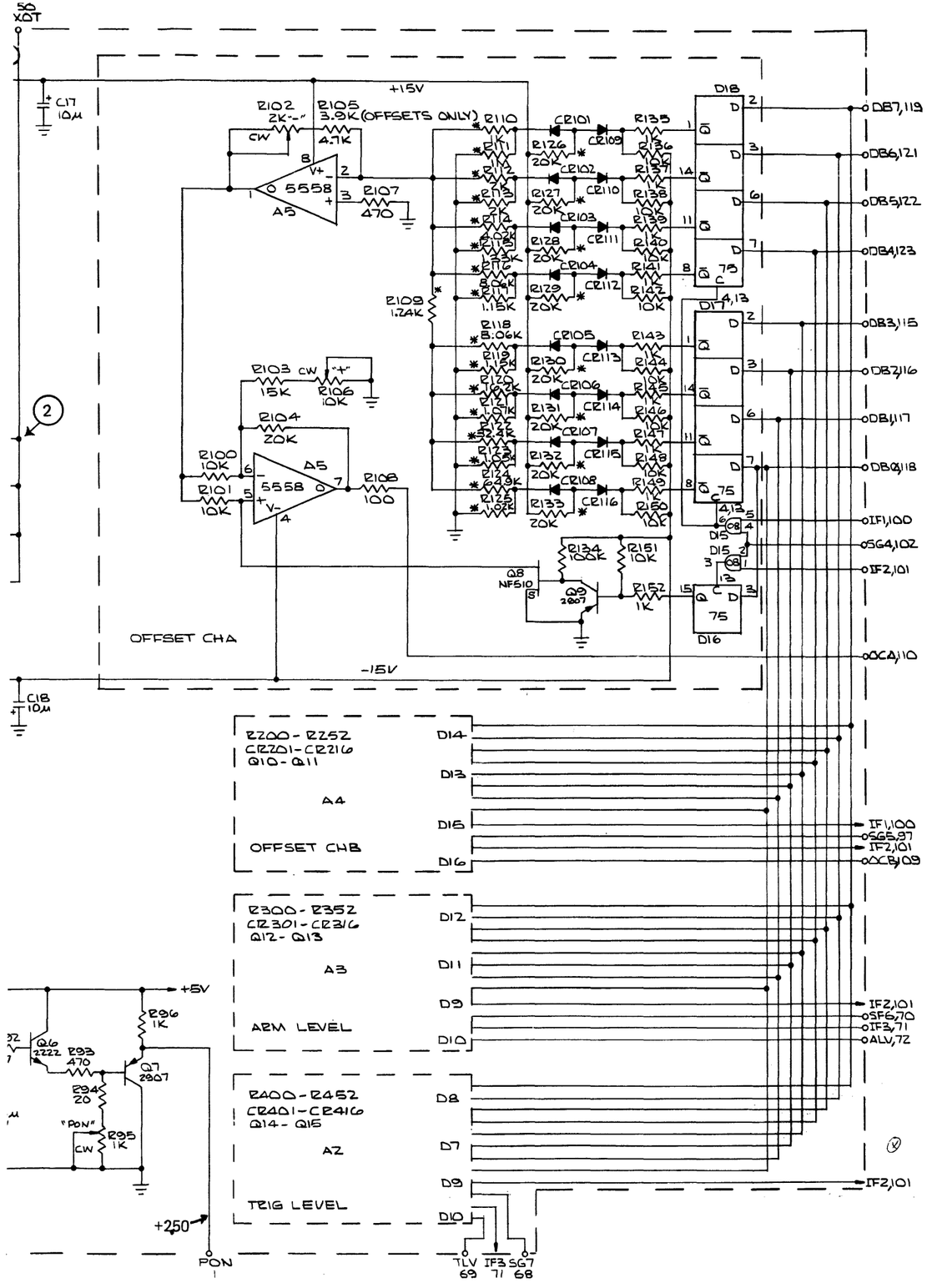


FIGURE 9.19B D/A Board Schematic

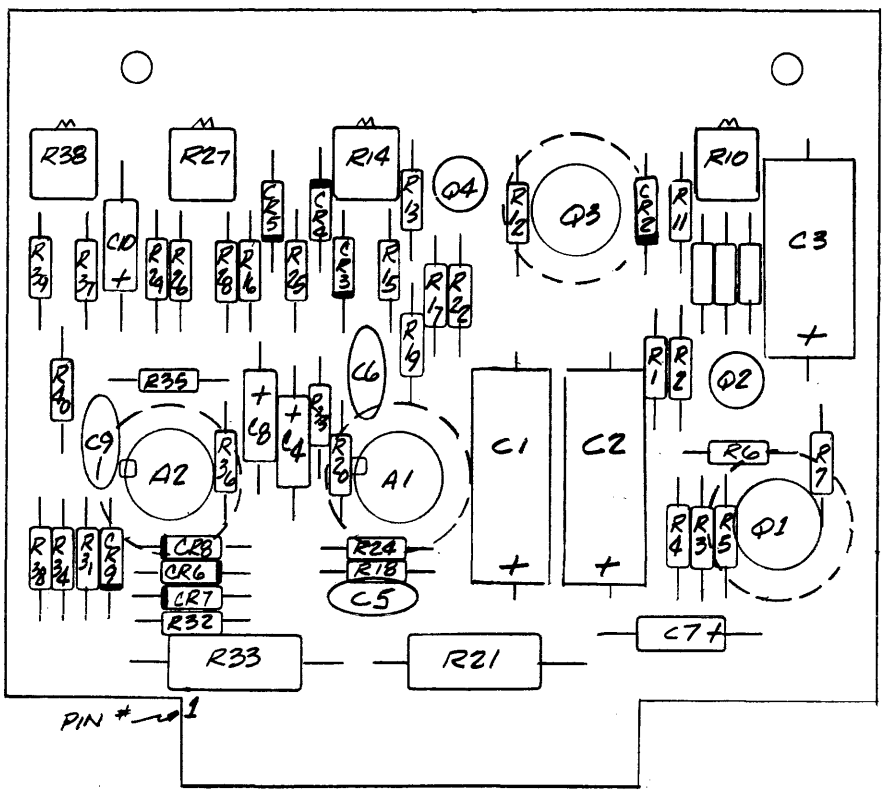
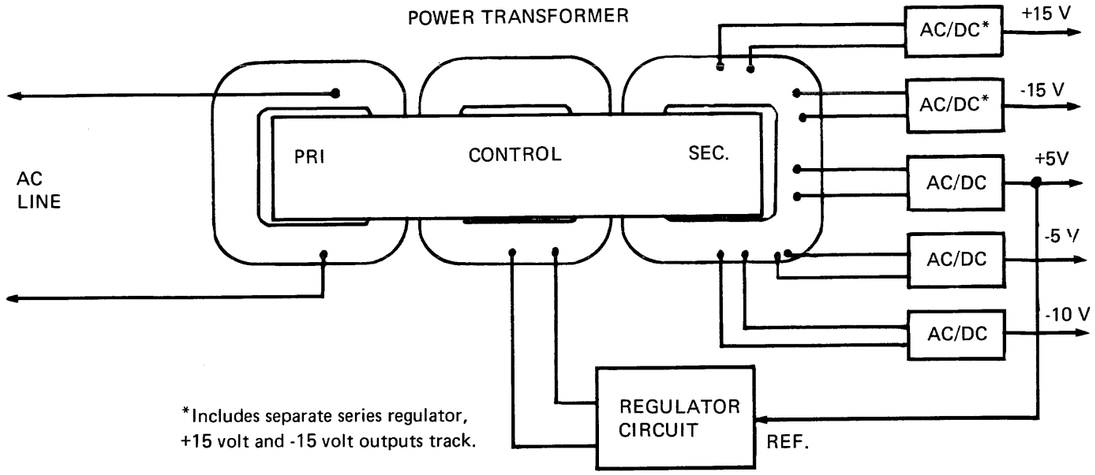
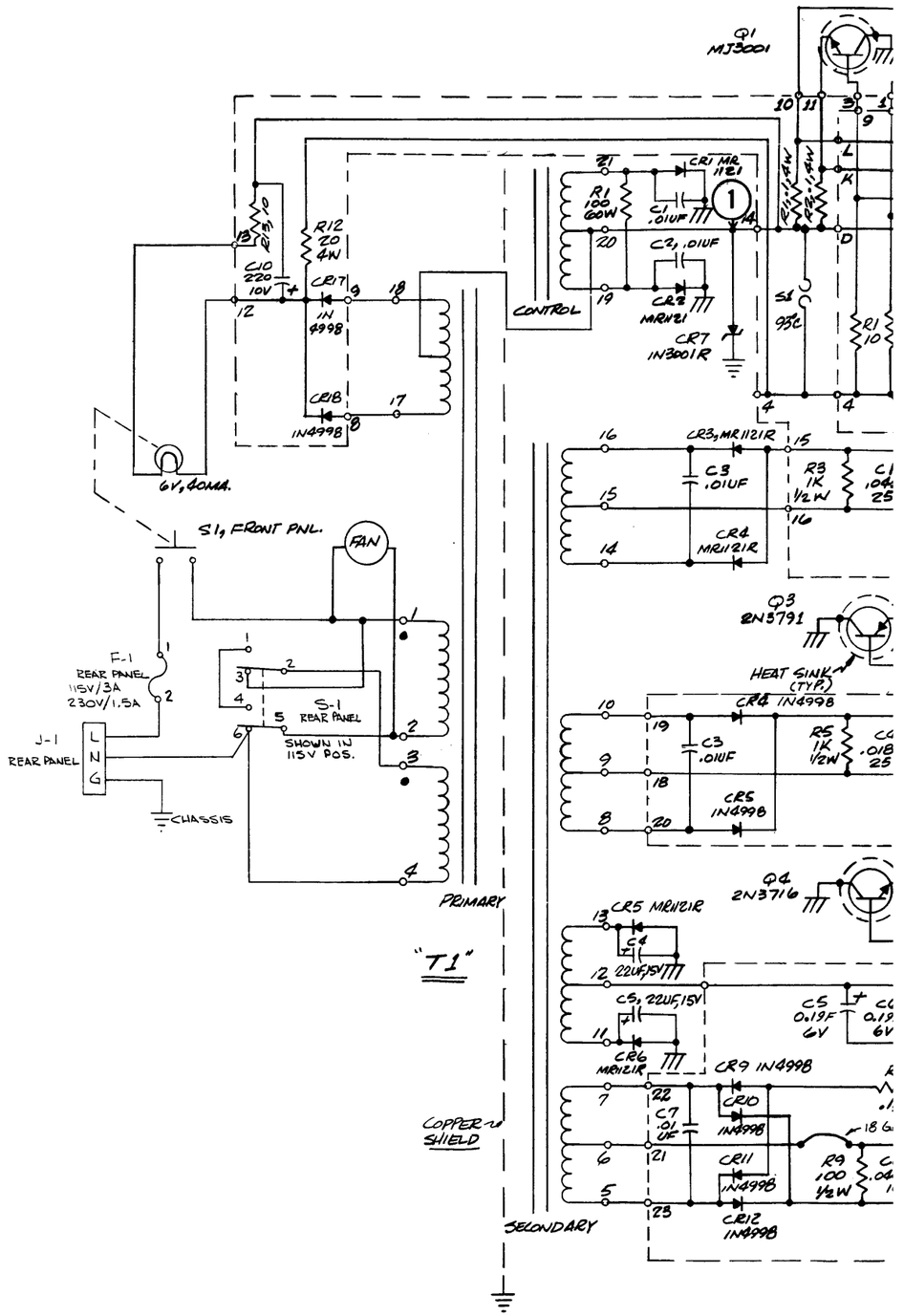
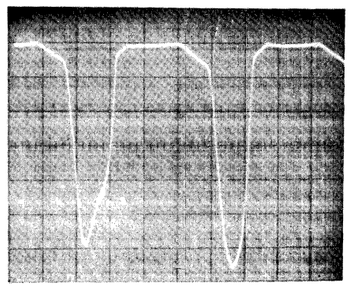


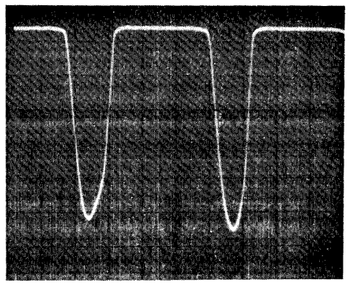
FIGURE 9.20 Power Supply Regulator Board Layout



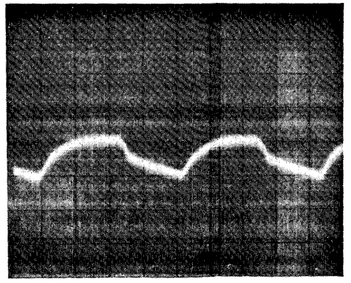




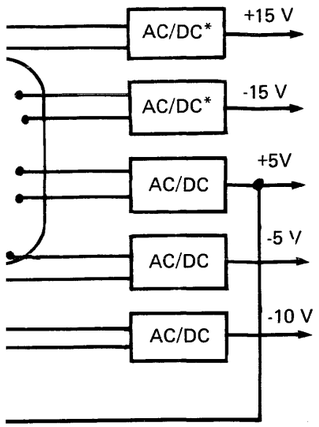
1. Scope: Vert 2V/div, Horz 2ms/div, Trigger internal on line sync. 8100: 117 volts AC in.



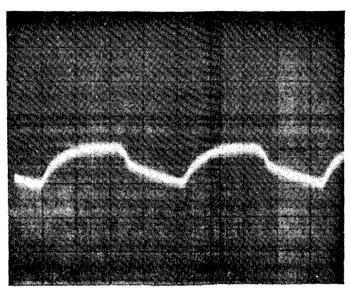
2. Scope: Vert 2V/div, Horz 2 ms/div, Trigger internal on line sync. 8100: 117 volts AC in.



3. Scope: Vert .2V/div, Horz 2ms/div, Trigger internal on line sync. 8100: 117 volts AC in.

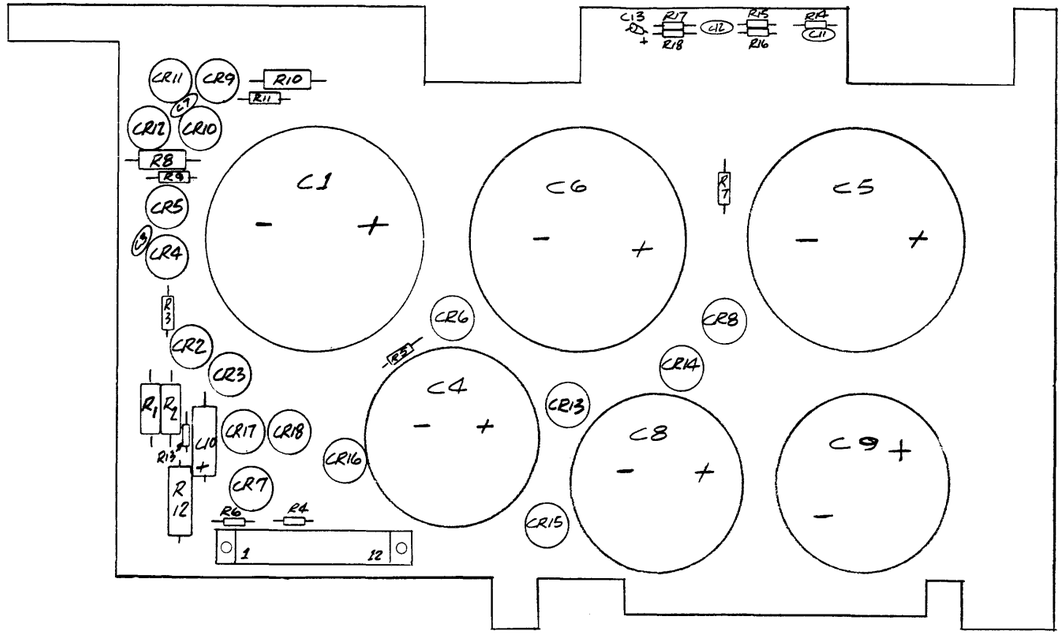


EF.

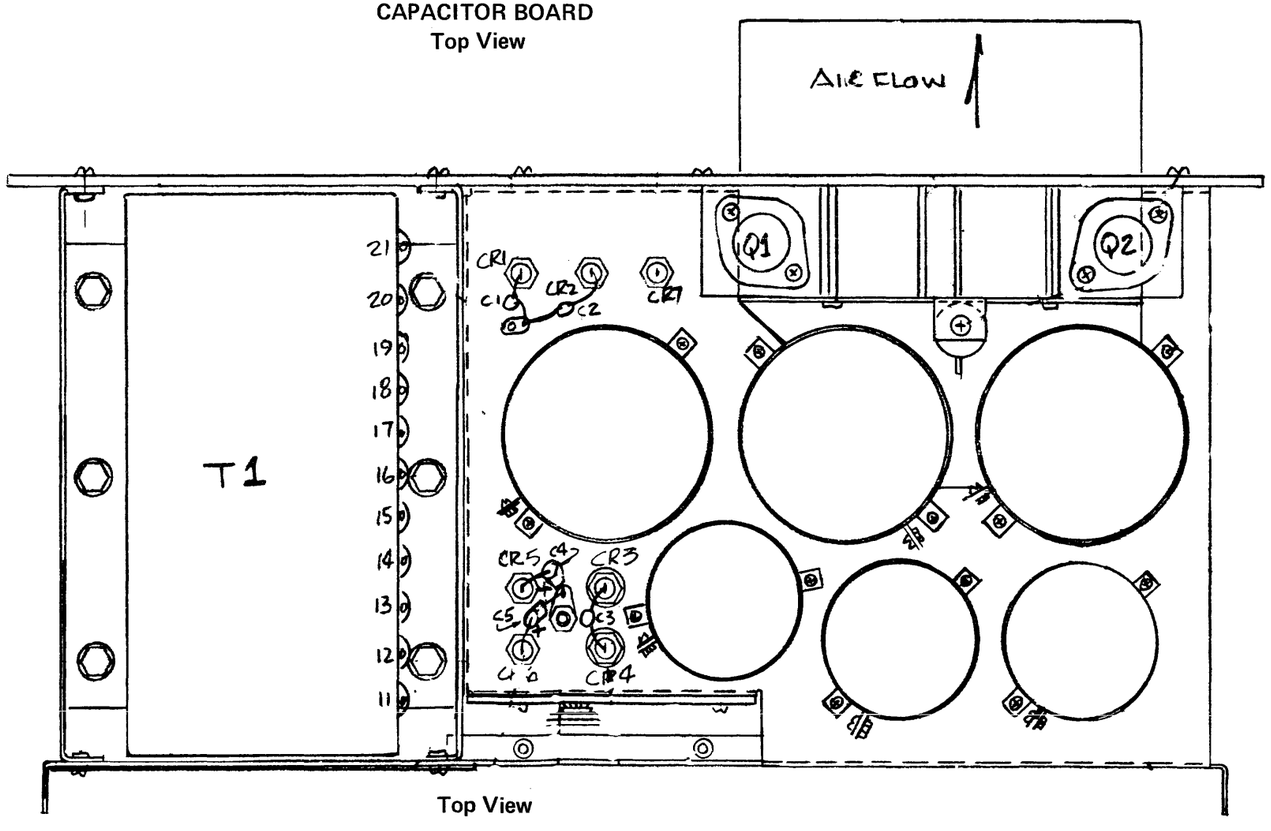


3. Scope: Vert .2V/div, Horz 2ms/div, Trigger internal on line sync. 8100: 117 volts AC in.

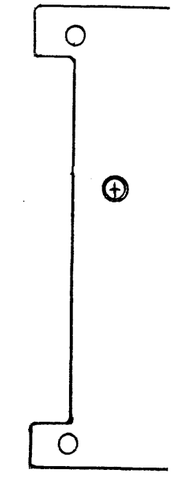
FIGURE 9.21 Power Supply Schematic



CAPACITOR BOARD
Top View



Top View



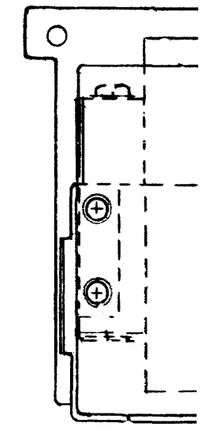
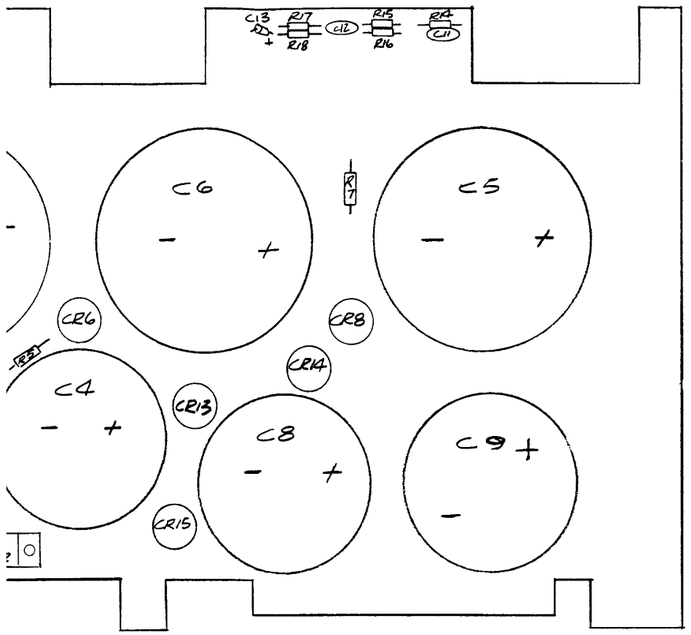
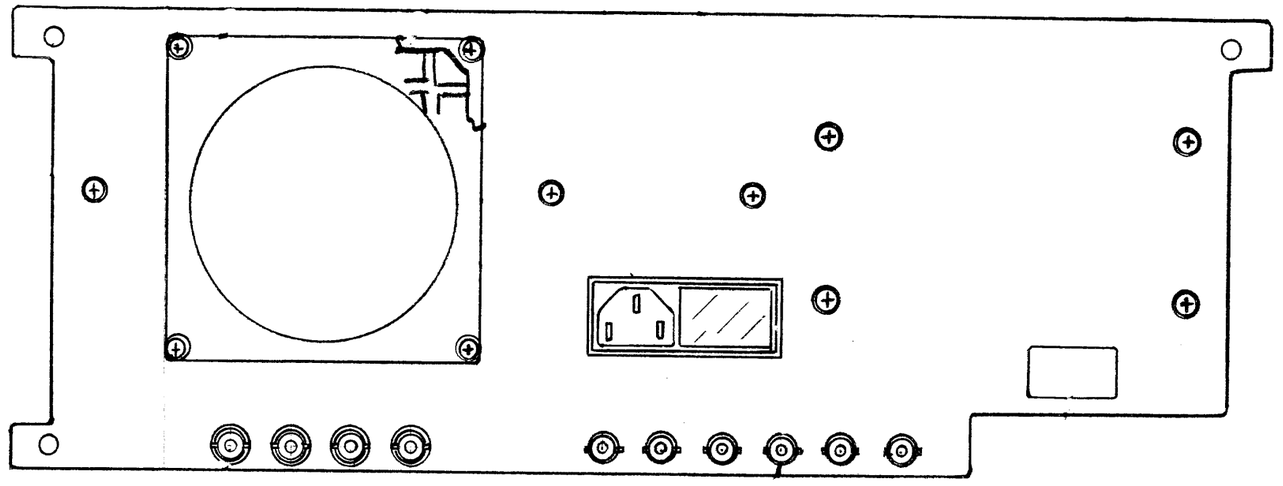


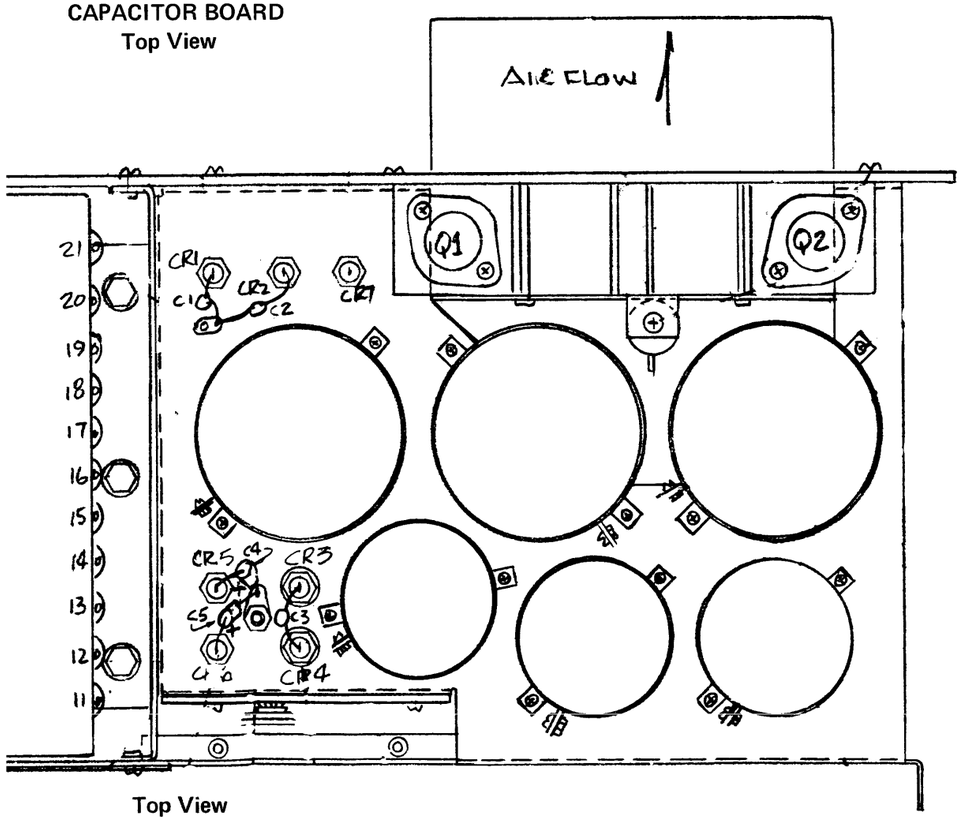
FIGURE 9



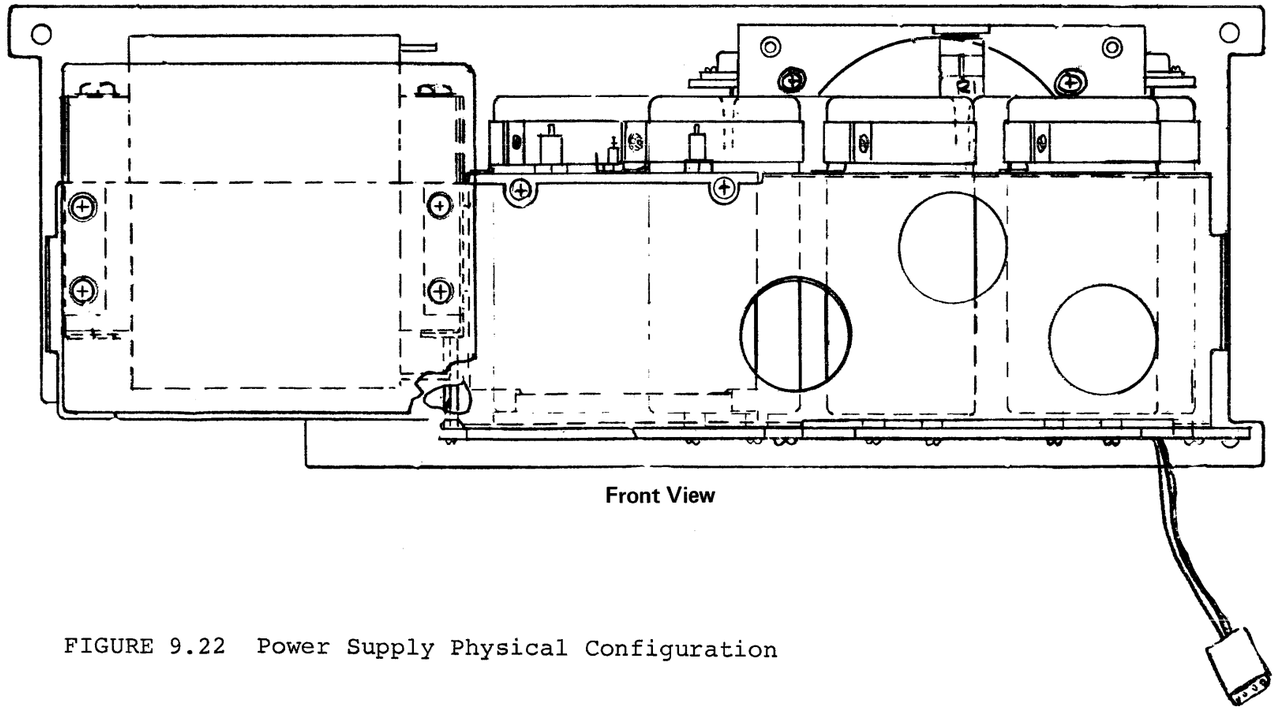
CAPACITOR BOARD
Top View



Rear View

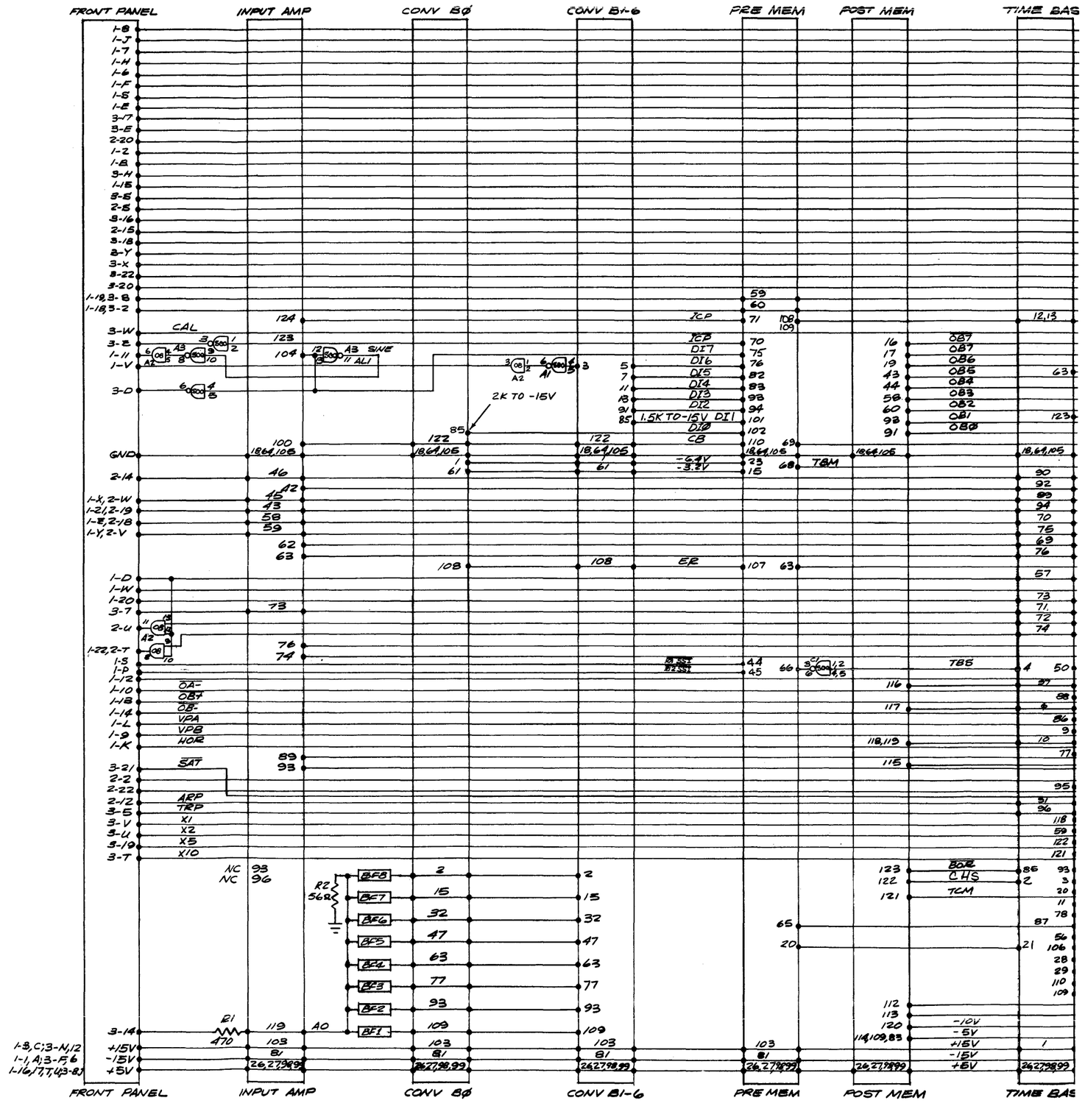


Top View



Front View

FIGURE 9.22 Power Supply Physical Configuration


FRONT PANEL
INPUT AMP
CONV BØ
CONV B1-6
PRE MEM
POST MEM
TIME BAS
CAL
A3 SINE
11 ALI
2K TO -15V
1.5K TO-15V DII
ICP
DI7
DI6
DI5
DI4
DI3
DI2
DIØ
CB
-6.4V
-3.2V
EP
TBM
TBS
GND
+15V
-15V
+5V
OA-
OBT
OB-
VPA
VPB
HOR
SAT
ARP
TRP
X1
X2
X5
X10
R1 470
R2 56Ω
BF8
BF7
BF6
BF5
BF4
BF3
BF2
BF1
BOT
CHS
TCM
FRONT PANEL
INPUT AMP
CONV BØ
CONV B1-6
PRE MEM
POST MEM
TIME BAS

A - CHANGED VALUE OF R4 - WAS: 470 IS: 390

B- E.C.O#018 6-7-77 mg

C- E.C.O#020 1.5K TO -15V mg 6-10-77
APPLIES ONLY TO DI1
BETWEEN PRE-MEM & CONV BI-6.

D- ECO#0030: A1-9,10 CHANGED
FROM BOTH GOING TO PRE-MEM
PIN #44 TO A1-9 TO PRE-MEM
45 & A1-10 TO PRE-MEM 44. mg
8-3-77

E- REVISED PER ECO No. 080
11-30-77 S. Riddell

F- REVISED PER ECO#0110, 12-1-77 SR

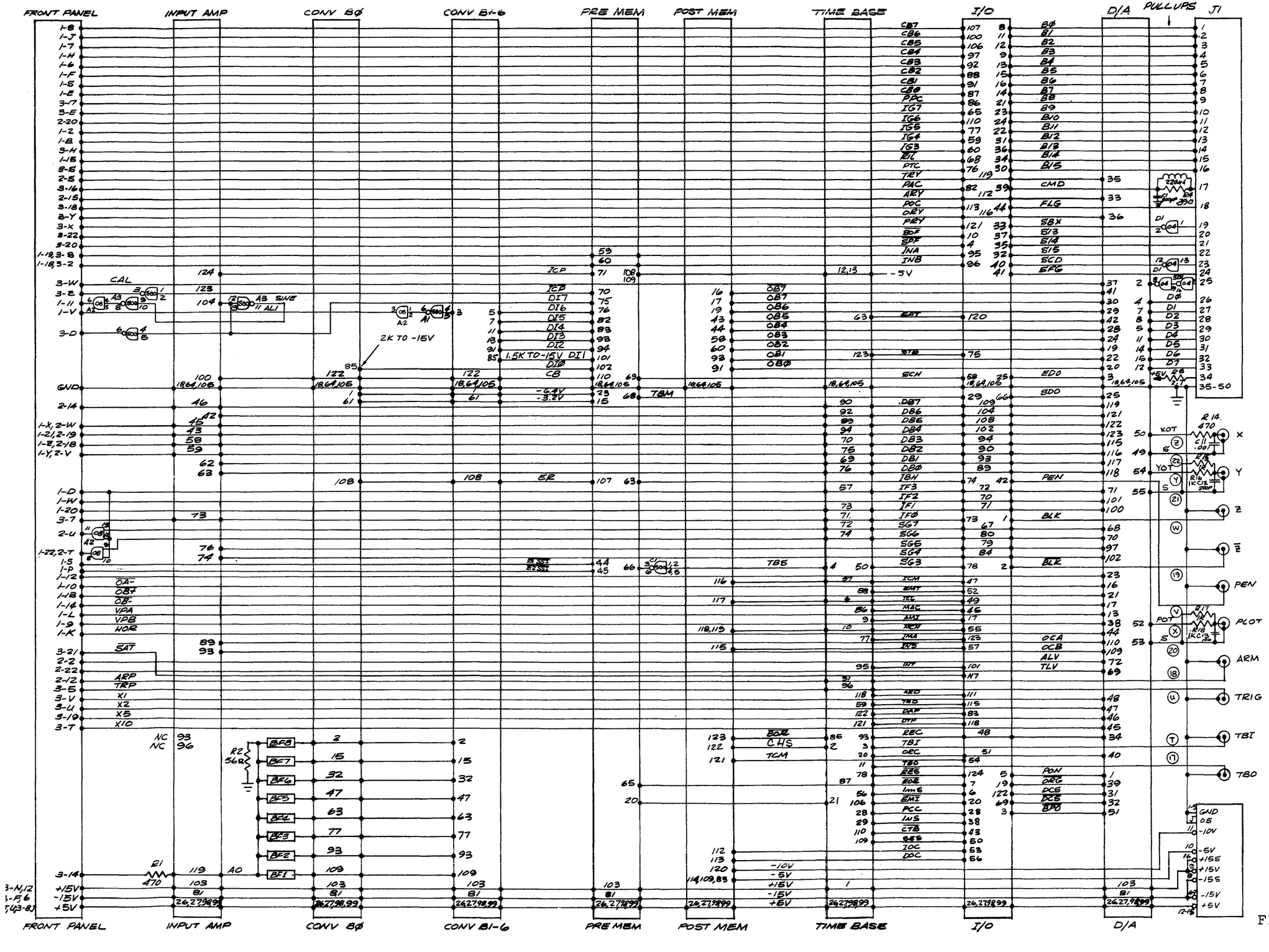


FIGURE 9.23 Mother Board Diagram

Power Supply Removal

Step 1. Remove top and bottom covers.

Step 2. Remove D/A, I/O and Time Base Boards, Fig. 1.
Remove top transformer shield if required, Fig. 1.

Step 3. Remove 4 screws--2 each side as shown, Fig. 2.

Step 4. Remove 4 screws as shown, unplug AC power connection, Fig. 3.

Step 5. Remove 6 screws from rear panel, Fig. 4.

Step 6. With chassis standing on rear panel and fan cover, lift chassis clear of power supply, Fig. 5.

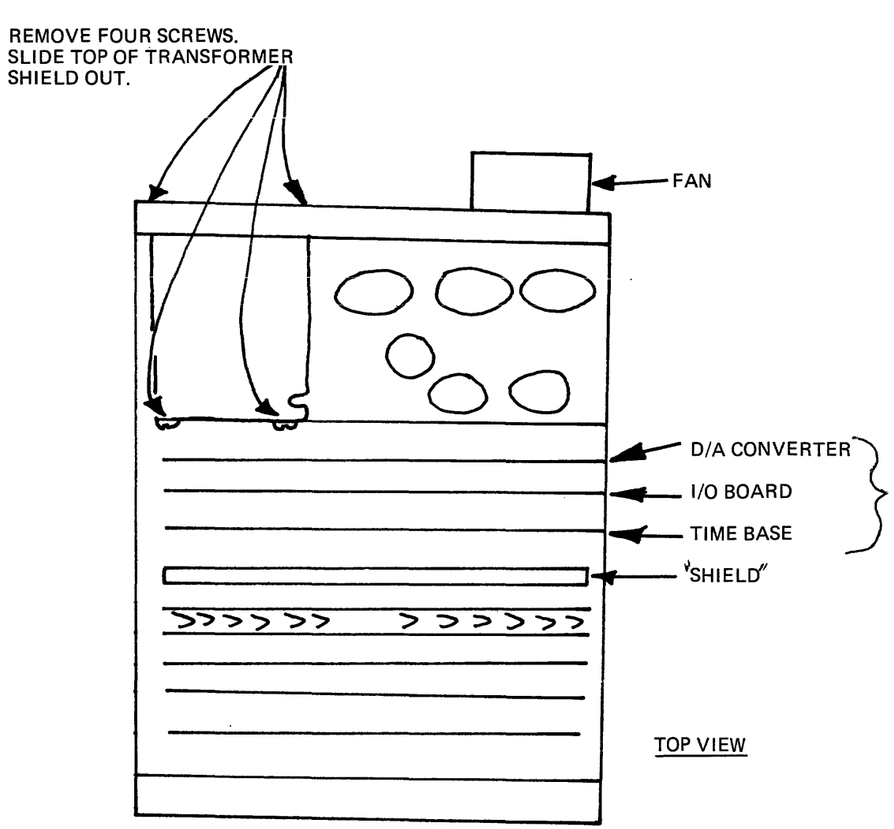


FIG. 1

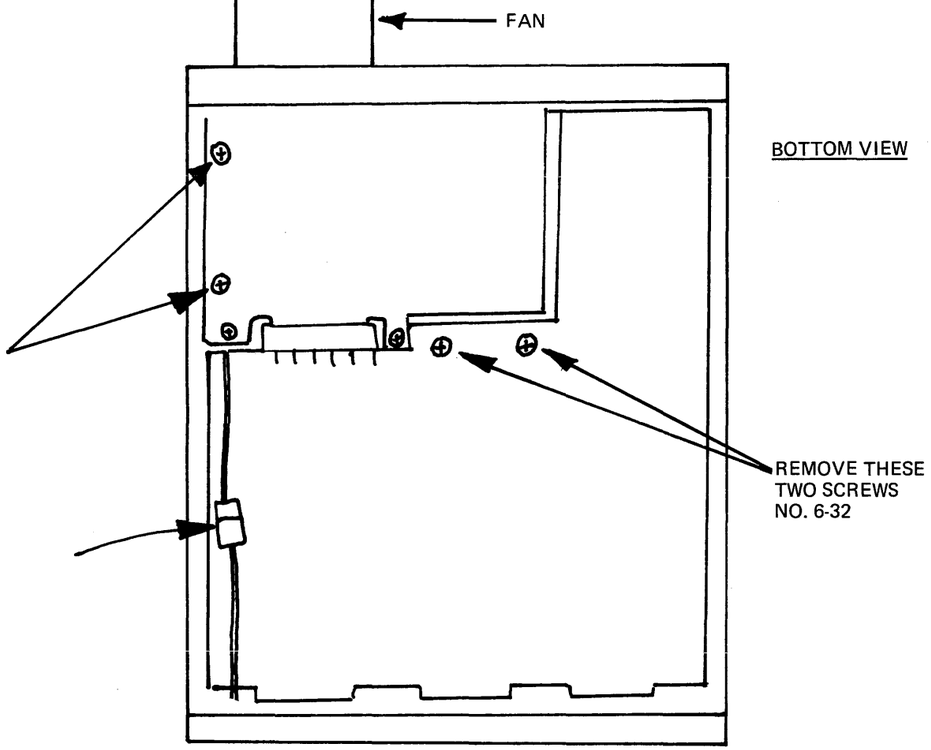
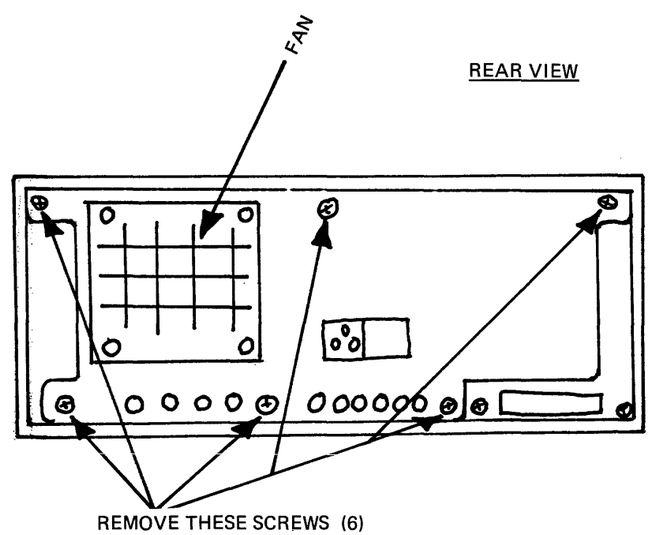


FIG. 3



WATCH THES
WHEN REMO

FIG. 4

1.

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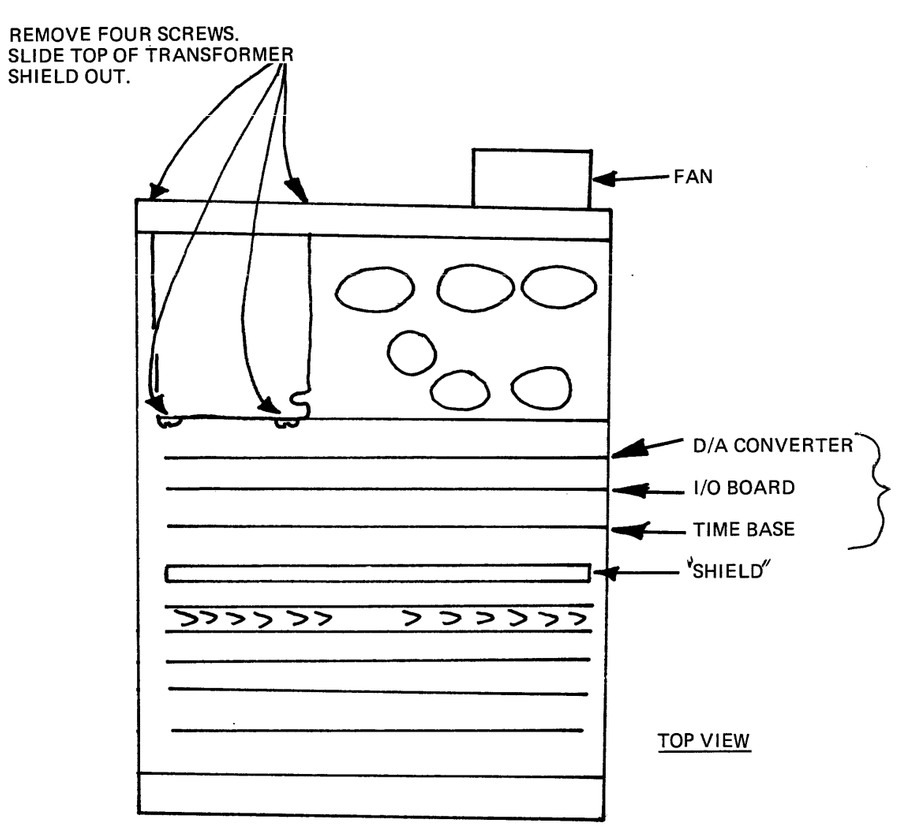
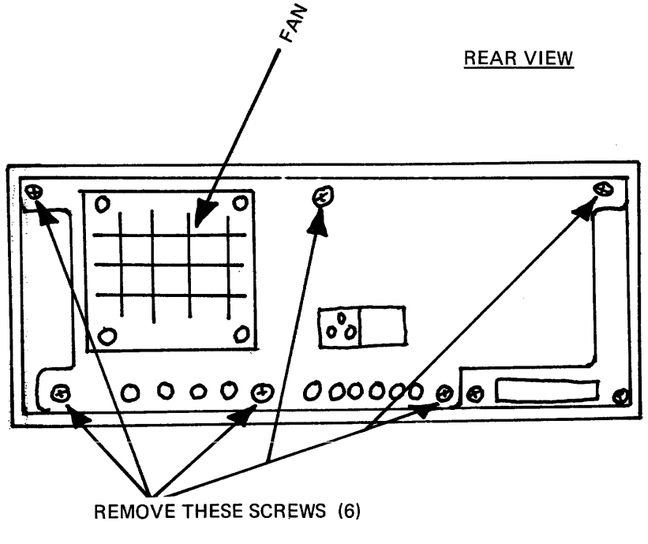


TOP VIEW

FIG. 1

BOTTOM VIEW

REMOVE THESE
TWO SCREWS
NO. 6-32



REAR VIEW

FIG. 4

FIG. 2

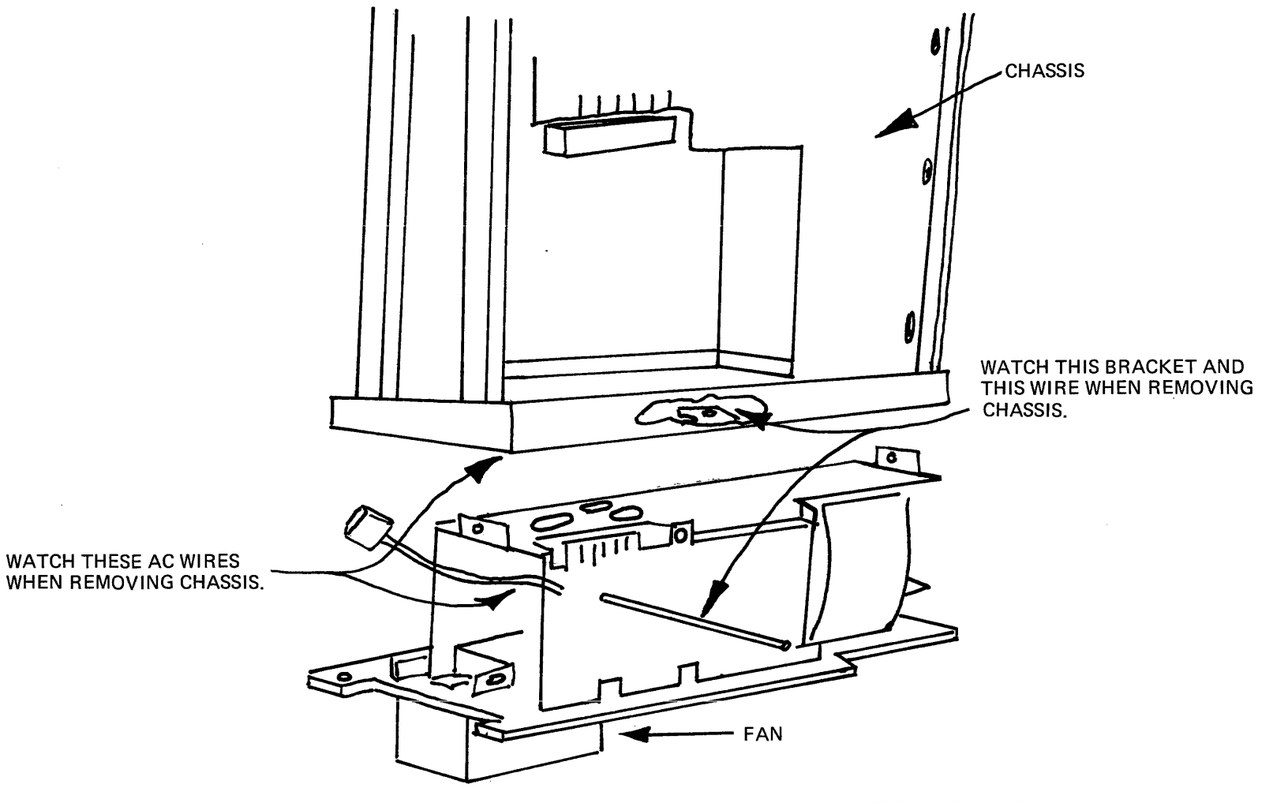


FIG . 5

FIGURE 9.24 Disassembly Procedure Power Supply Removal

PC CARD REMOVAL

1. Remove 4 screws from top cover. 2. Remove top cover. 3. Remove Hold-down bracket, 1 screw. 4. Using two flat bladed screwdrivers, lift cards as shown in Fig. 1. NOTE: For Input Board, move finger board to the left with finger, Fig. 2. 5. Re-install cards by aligning card over slot in connector and prying cards back with screwdrivers or push firmly with hands on top edge of card.

USE OF THE EXTENDER CARDS

There are three (3) extender cards provided with the 8100. The small extender card is for use with the Power Supply Regulator board. The remaining two long extender cards are for use with the plug in PC cards.

Power Supply Extender Card: 1) Remove two (2) screws holding Regulator card in the unit. 2) Unplug the Regulator card using the finger hole in the top edge. 3) Insert extender card (part #0810-0136) with topped side to the rear of unit. 4) Insert Regulator card into extender card (component side to the front).

Universal Extender Card
The Universal extender card (part #0810-0081) is the card with connec-
running continuously over the full width of the card. Note that on one side there is a full continuous foil--this is the ground side of the card. The extender card must be placed in the unit with this side toward the front of the 8100. Make sure the contacts of the connector line up with the fingers of the back side of the card. Align the card over the connector and using the palms of both hands, press the card into the mating connector. Align the contacts of the extender card with the figures on the back side of the PC board and push the PC card into the extender board. After insertion recheck the alignment of the contacts. To separate the cards, remove the entire PC card and extender board from the unit. Use two flat bladed screwdrivers in the slots on the edge of the extender card and the top edge of the chassis to remove the extender card. Grasp the side edge of the extender card in one hand and the PC card in the other hand. Pull the two cards apart. Use care to avoid damage to the extender card.

Post Memory Extender Card
The Post Memory card (part #0810-0133) is the extender card with only a partial row of connectors on the top edge. This card is only used with the Post Memory board. It is inserted with the continuous ground side to the rear of the unit. Again check the alignment of the extender card contacts with the Mother board connector.

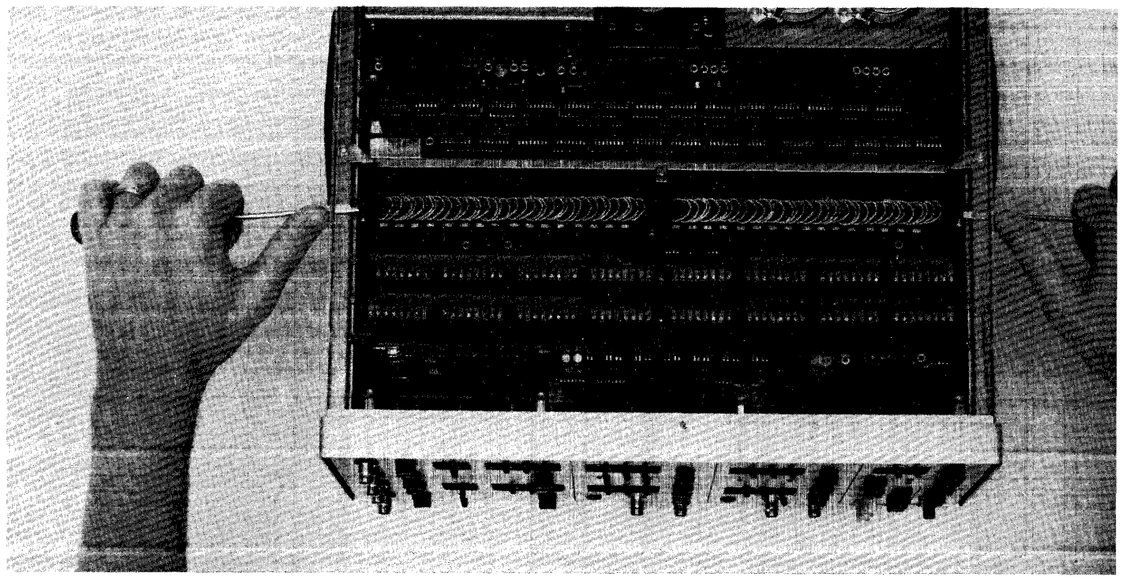


FIGURE 1

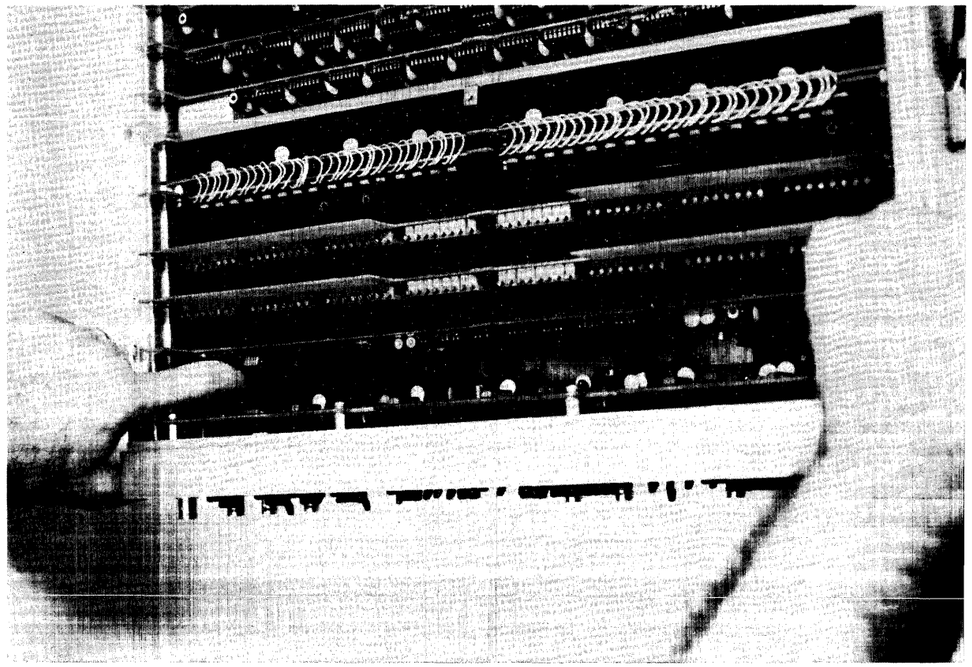


FIGURE 2

3. Remove
drivers,
e finger
by align-
crewdrivers

The small
rd. The
in PC cards.

ng Regulator
inger hole
with top-
o extender

th connec-
Note that
und side
ith this
f the con-
.. Align
s, press
he extender
ush the PC
lignment
C card and
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he chassis
ender card
cards

with only
nly used
ous ground
the exten-

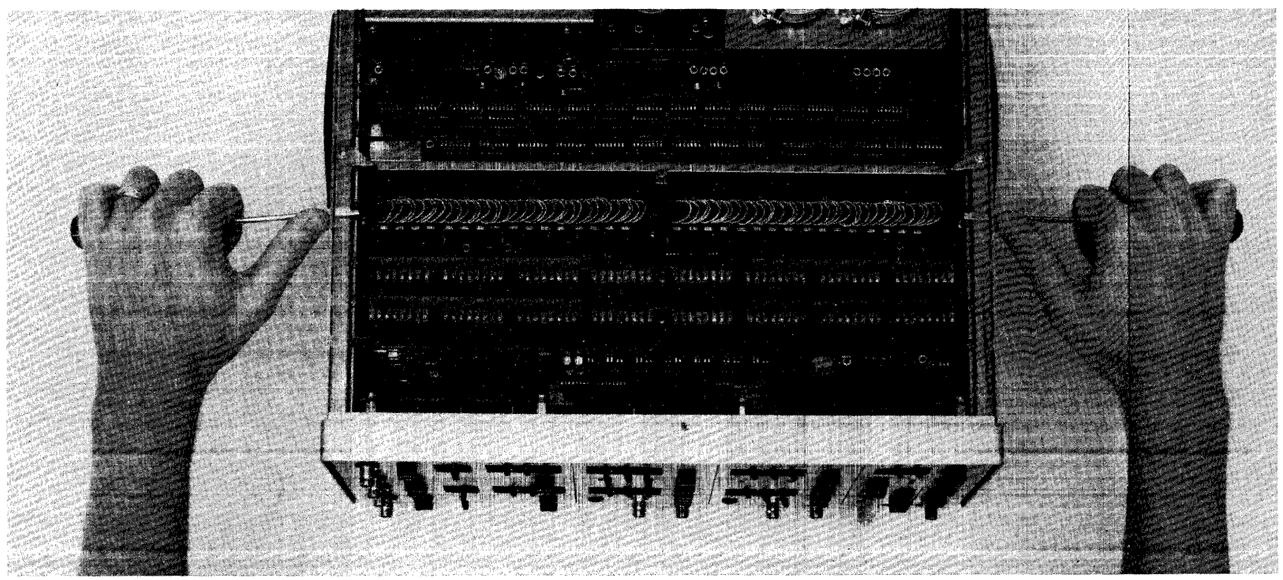


FIGURE 1

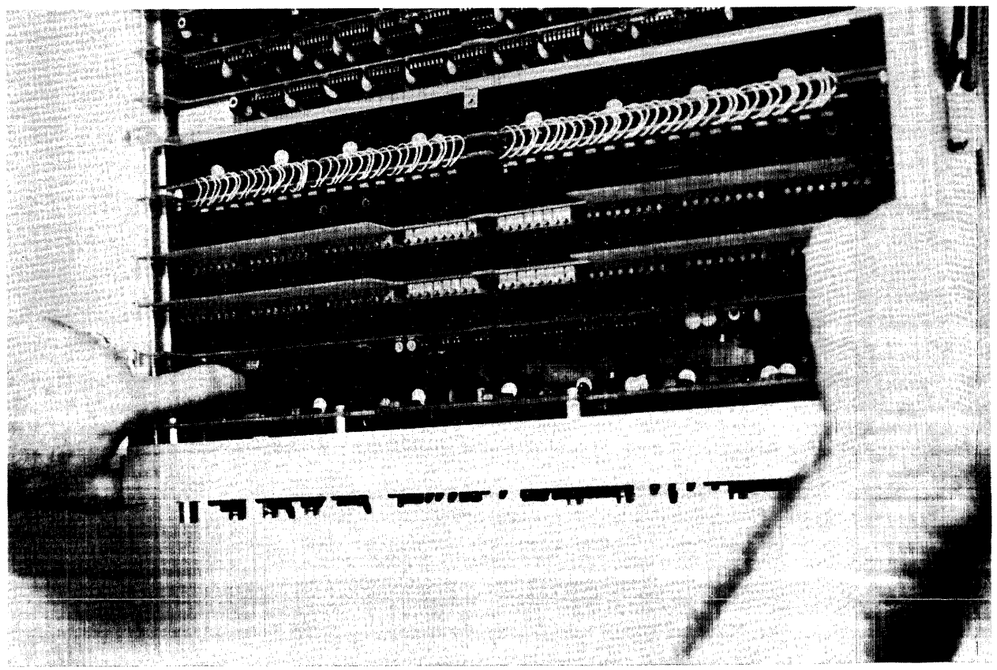


FIGURE 2

Front Panel Removal

1. Remove top cover (4 screws).

2. Remove bottom cover (4 screws).

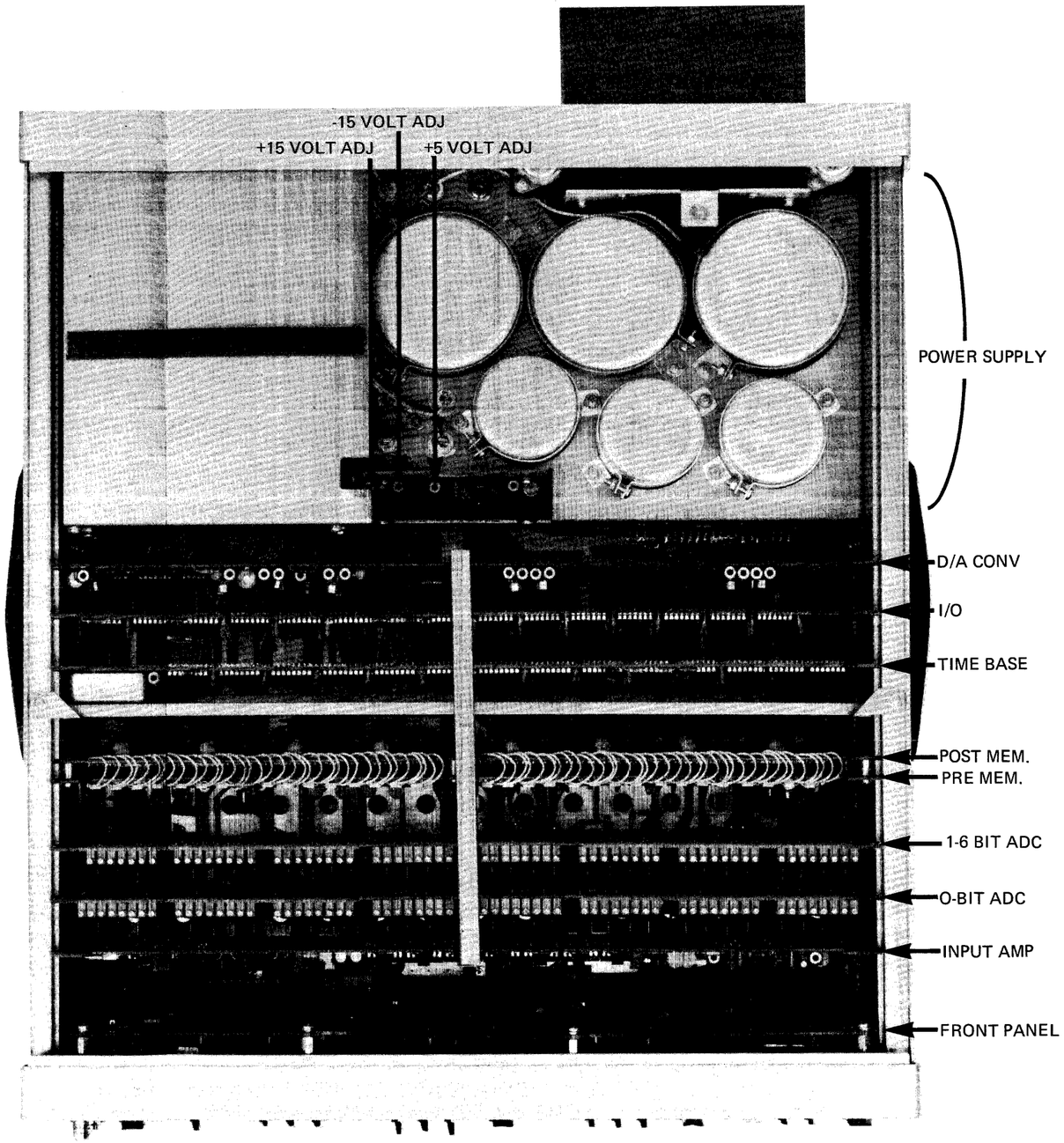
3. Place unit on its rear.

4. Unplug Power switch connector.

5. Using long 1/4" "spintite", remove 8 Hex nuts from front panel studs (4 top & 4 bottom).

6. With thumb on edge of front panel PC Board, push front panel out front of unit.

FIGURE 9.25 Disassembly Procedures PC Cards and Front Panel



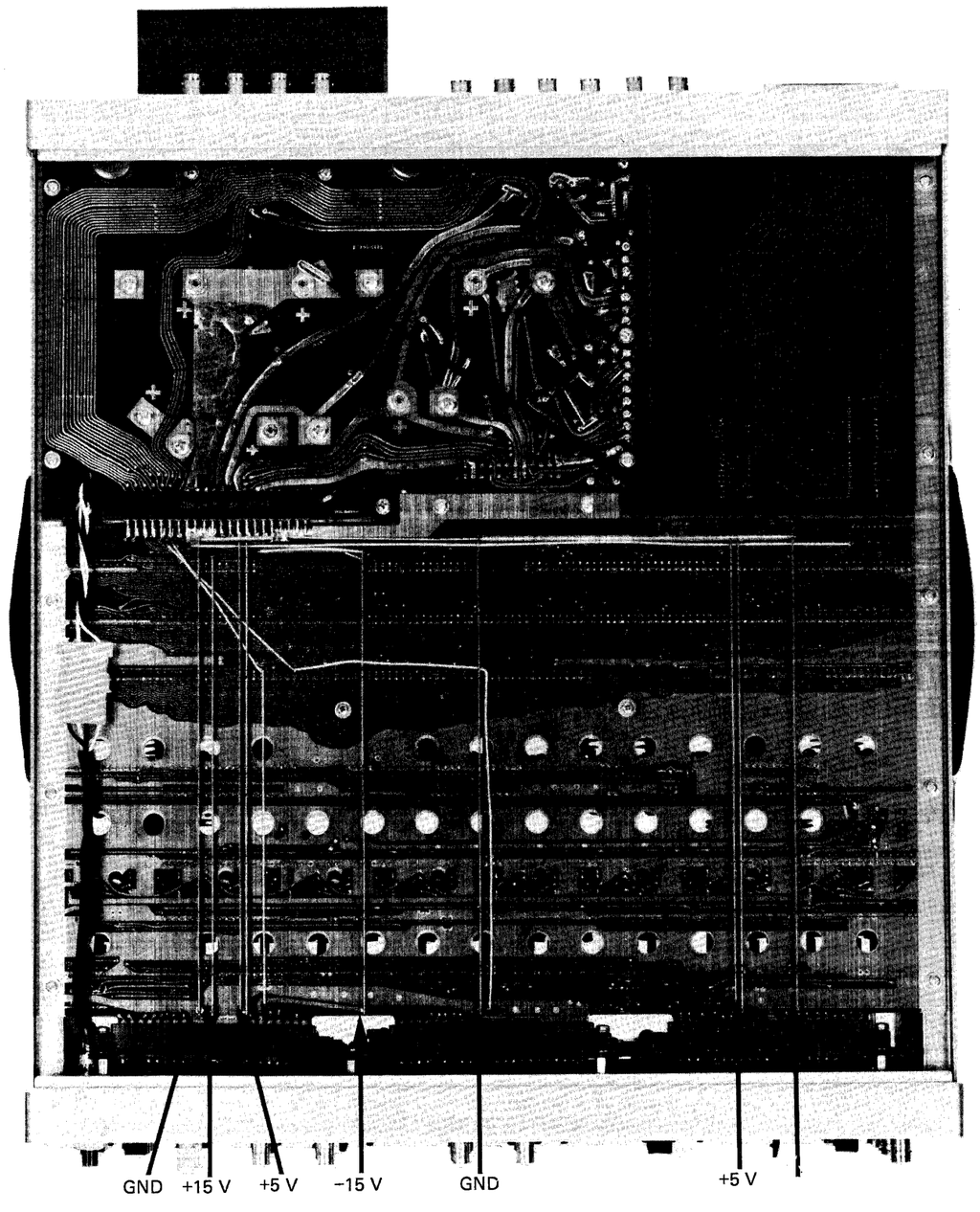


FIGURE 9.26 Top/Bottom Internal View

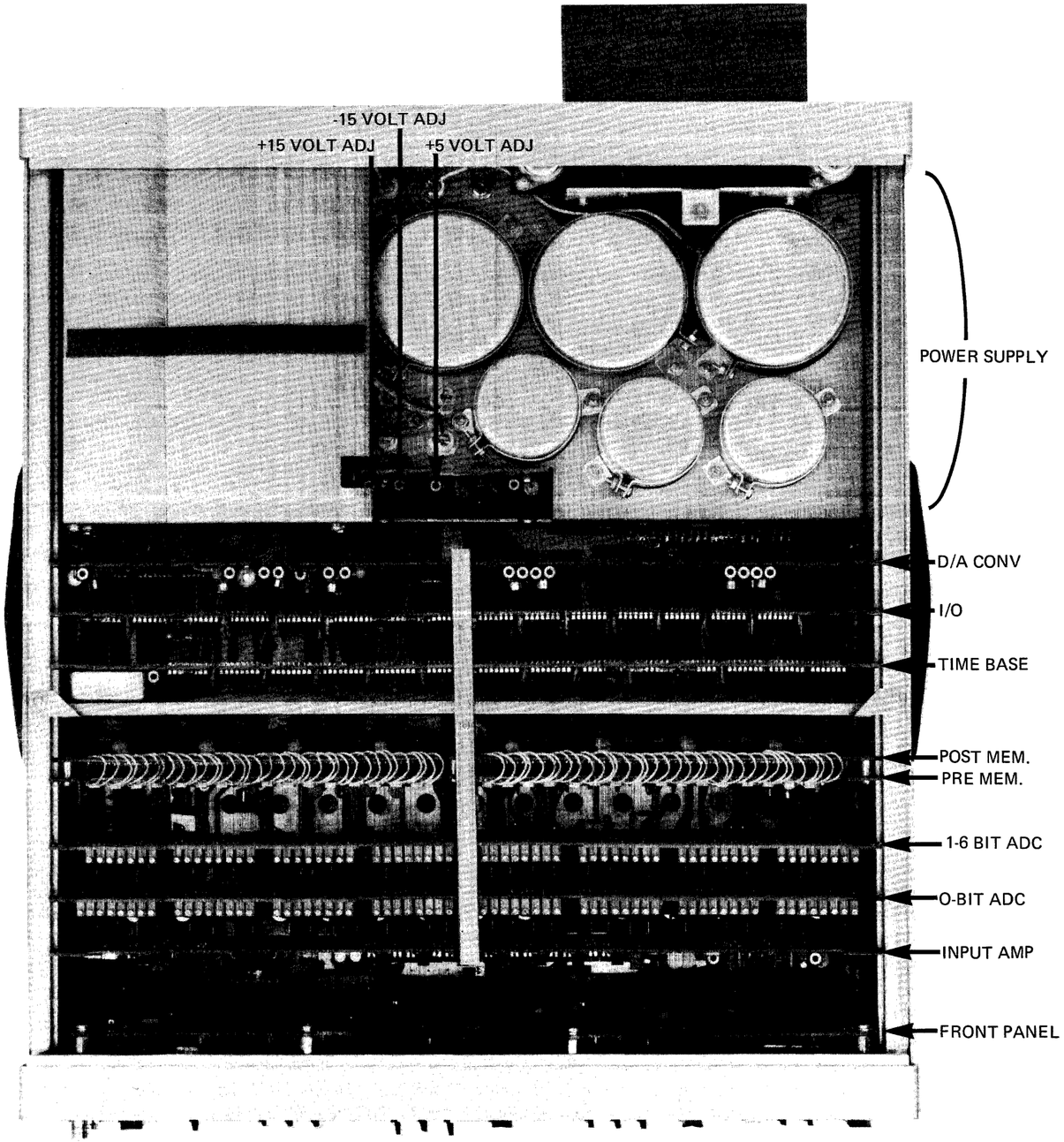
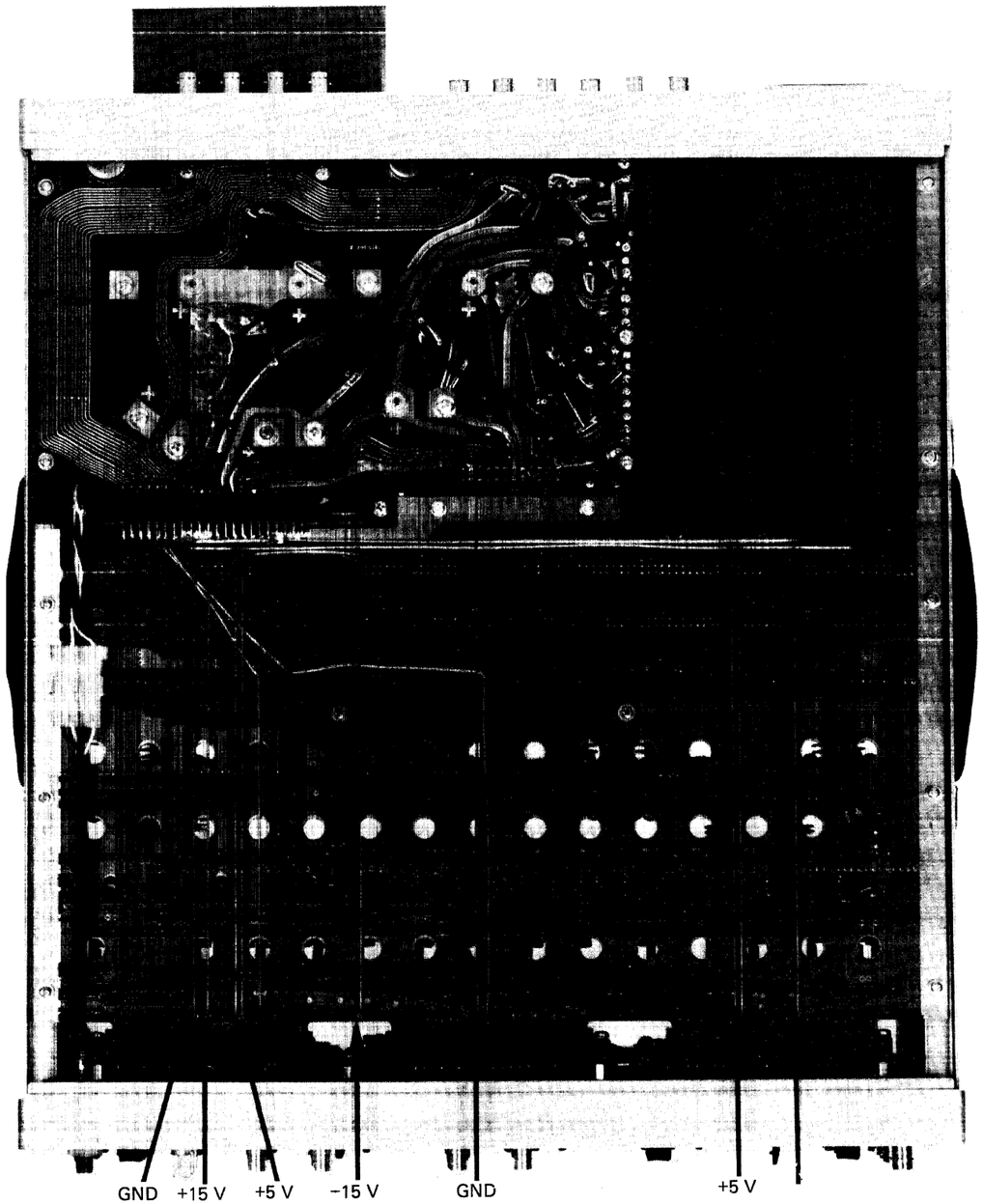


FIGURE 9.26 Top/Bottom



ıternal View

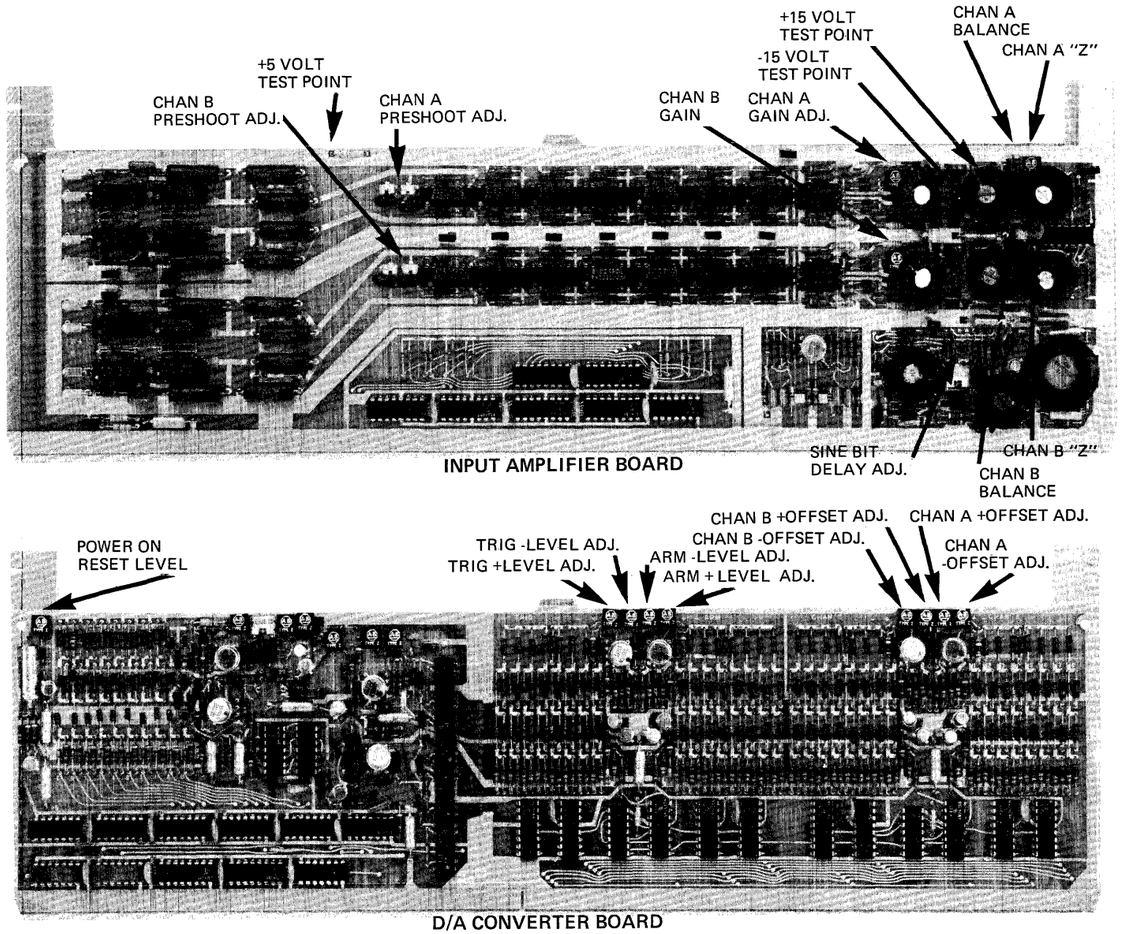


FIGURE 9.27 Voltage and Adjustment Locations

FIGURE

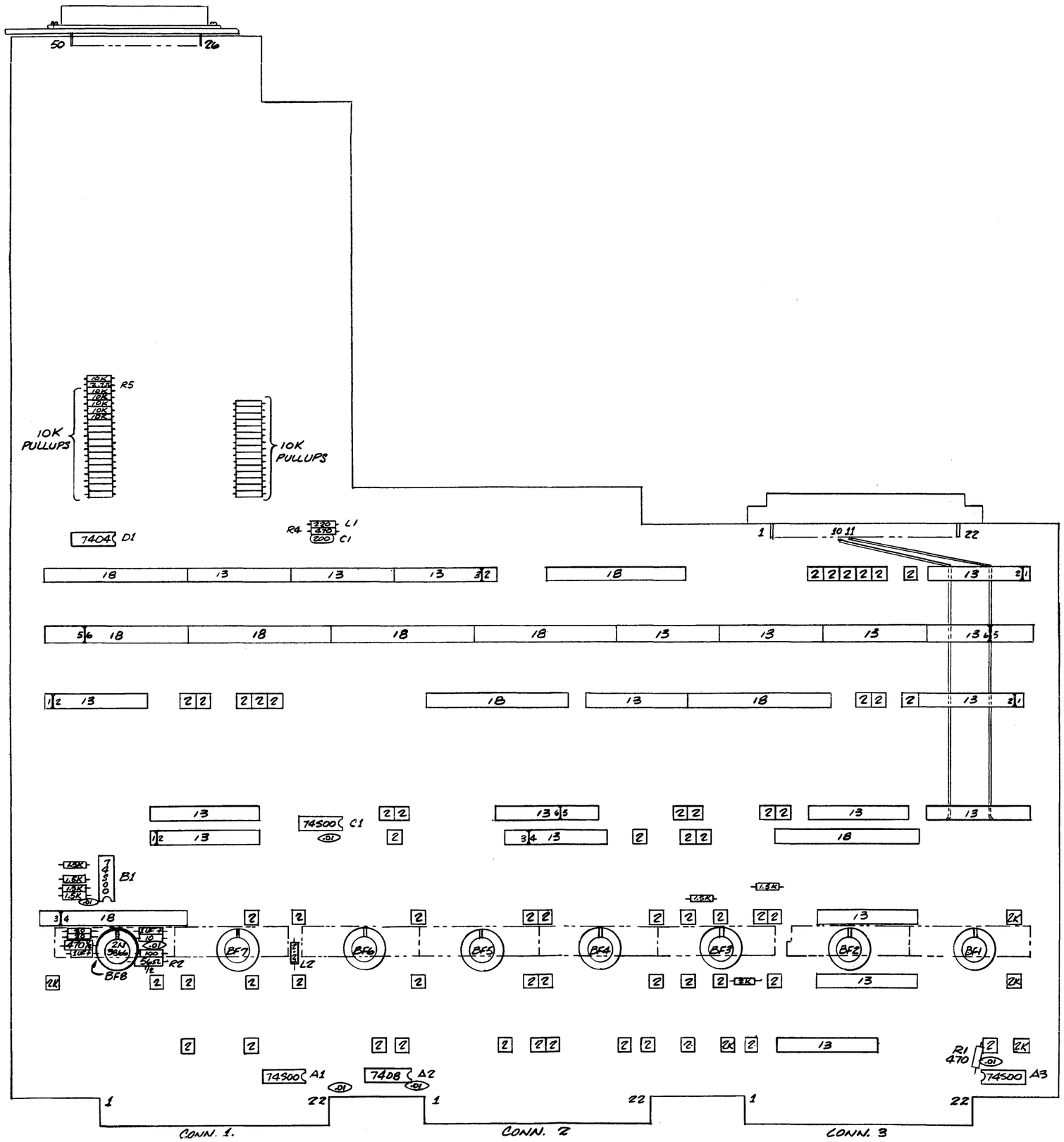

50
26
10K PULLUPS
R5
10K PULLUPS
7404 D1
R4 220 470 200 C1 L1
1
10 11
22
18
13
2
74500 C1
01
74500 A1
7408 A2
74500 A3
R1 470
BF8
BF7
BF6
BF5
BF4
BF3
BF2
BF1
R2
LZ
B1
CONN. 1.
CONN. 2
CONN. 3
GRD
+5V
-15V

FIGURE 9.28 Motherboard Layout