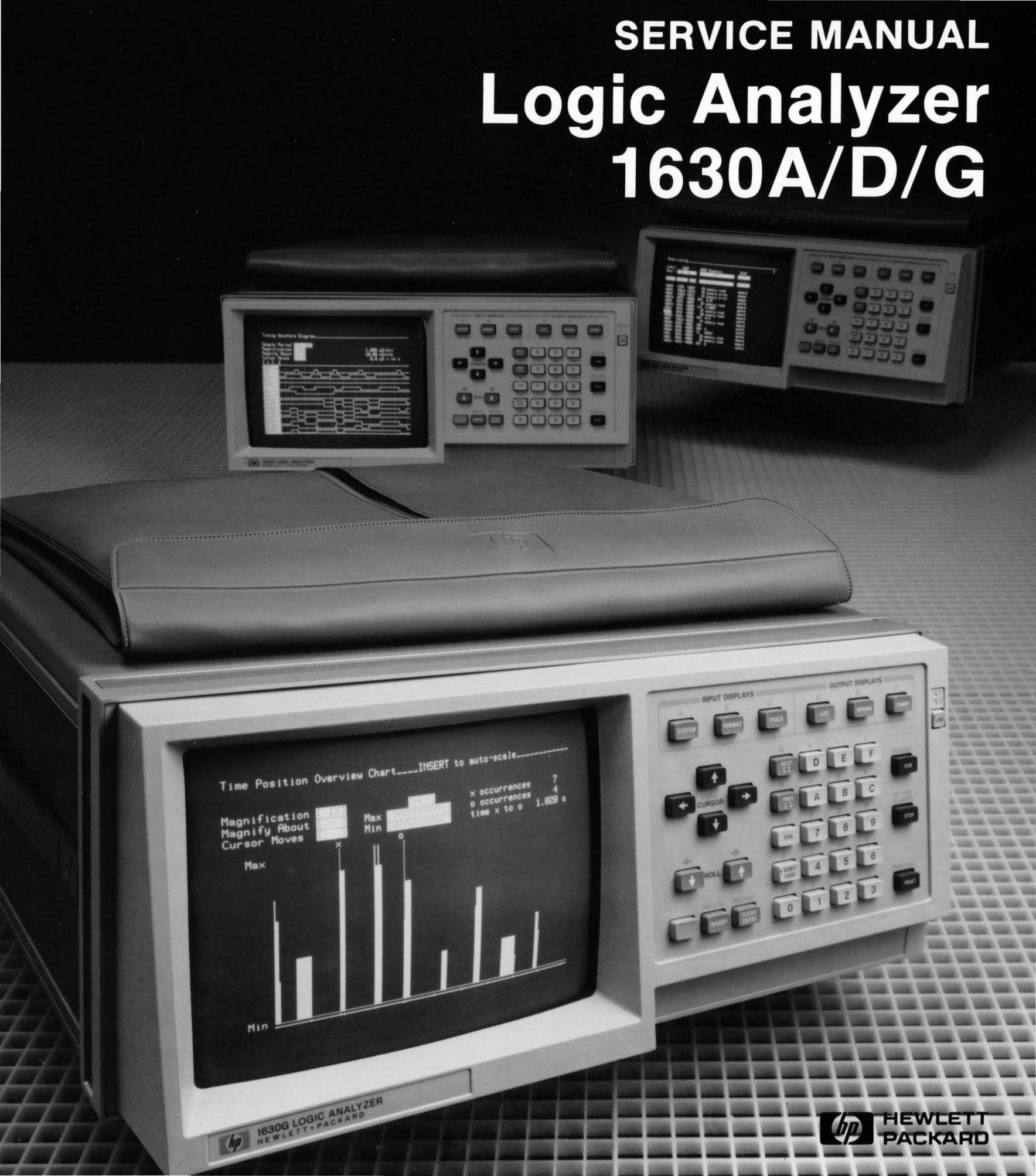
SERVICE MANUAL

Logic Analyzer 1630A/D/G



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SERVICE MANUAL

MODEL 1630A/D/G LOGIC ANALYZER

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

1630A; 2412A
1630D; 2412A
1630G; 2415A

With changes described within, this manual also applies to instruments with serial prefixes:

1630A; 2242A and 2311A
1630D; 2234A and 2311A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

Manual Part No. 01630-90910
Manual with Binder Part No. 01630-90905
Microfiche Part No. 01630-90810

PRINTED: JUNE 1984

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

C W & A 5/84

SAFETY CONSIDERATIONS

GENERAL – This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION – BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

* Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
* BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
* If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
* Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
* Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
* Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
* Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
* Do not install substitute parts or perform any unauthorized modification to the instrument.
* Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
* Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
* Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

NOTE

Service and circuit information for the individual assemblies is located in separate sections. Tables of Contents for each section are located at the front of the section. The sections are divided as follows:

SECTION	ASSEMBLY
8A	Power Supply and Motherboard
8B	CPU and Keyboard
8C	State Master
8D	Timing Master
8E	Timing Slave
8F	State Slave

APPENDICES

The appendices provide additional information for instrument service. A Table of Contents is provided at the front of each appendix.

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I
GENERAL INFORMATION

WARNING

The information in this manual is for the use of trained service personnel. To avoid electrical shock, do not perform any procedures in the manual or do any servicing to the 1630A/D/G unless you are qualified.

1-1. INTRODUCTION

This manual contains technical information concerning the installation, operation, maintenance, and servicing of the 1630A, 1630D, and 1630G Logic Analyzers. When information concerns more than one model the system will be referred to as 1630A/D, 1630A/D/G, etc.

1-2. MANUAL ORGANIZATION

SECTION I, GENERAL INFORMATION. This section contains a description of this manual and the 1630 family. This section also gives specifications and recommended test equipment for the 1630A/D/G Logic Analyzer.

SECTION II, INSTALLATION. Section II explains how to prepare the 1630A/D/G Logic Analyzer for use.

SECTION III, OPERATION. Operation of the 1630A/D/G is outside the scope of this service manual. Section III does give a brief description of front panel controls and information about configuration of the 1630A/D/G for HP-IB and HP-IL operation. For complete operating instructions see the Operating Manual.

SECTION IV, PERFORMANCE TESTS. This section concerns the execution of software-based function verification Self Test (ST) tests, which includes the interpretation of status codes to verify correct operation.

SECTION V, ADJUSTMENTS. The 1630A/D/G requires several adjustments that can be done with an oscilloscope, voltmeter, and HP85; these are covered in this section.

SECTION VI, REPLACEABLE PARTS. This section contains ordering information and a parts list for all models of the 1630.

SECTION VII, INSTRUMENT CHANGES. This section has information which describes changes to the instrument and how to find proper documentation for the instrument being serviced.

SECTION VIII, SERVICE. The Service section is divided into seven subsections. The first subsection covers the overall system. This includes system theory, and which service group to reference with a failure. The service groups focus on individual subsystems. Information in these groups includes block and component level theory, mnemonics, and schematics relating to that subsystem. Each subsystem and its service group designator is as follows:

8 - Introduction and General Information
8A - Power Supply and Motherboard
8B - CPU, Keyboard, and Display
8C - State Master
8D - Timing Master
8E - Timing Slave
8F - State Slave

APPENDICES. Several appendices provide additional information for servicing the 1630 family. Appendices A and B provide Guided Probe troubleshooting information for the 1630A/D and 1630G respectively. Guided Probe is a software driven troubleshooting technique used to find faults in the 1630A/D/G systems. Appendix C provides supplementary special-case testing which accompanies Guided Probe. Appendix D contains retrofit instructions for converting a 1630A or 1630D to a 1630G, and converting a 1630G to a 1630D. Appendix E provides miscellaneous service information which has been distributed through other channels and is included in this manual for reference and convenience.

1-3. INSTRUMENTS COVERED BY THIS MANUAL

Attached to the instrument is a serial number sticker. The serial number is in the form 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five are the suffix. The prefix is the same for all identical instruments; it only changes when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual applies to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. The supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available on request.

Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. DESCRIPTION

The Hewlett-Packard 1630A, 1630D, and 1630G Logic Analyzers are interactive state and timing analyzers for use in the design and troubleshooting of digital systems. Many functions of the systems are the same. The most obvious difference is that the width of the 1630A is 35 channels, the 1630D is 43 channels, and the 1630G is 65 channels. All models feature a menu system for defining measurements which simplifies setup time by reducing the number and complexity of front panel keys. Following is a listing of the key measurement features of the 1630A/D/G systems.

STATE ANALYSIS. The state analysis function of each model features:

* Continuous trace until compare "equal to" or "not equal to" is provided. The compare file is the width of the analyzer, and has depth of up to 16 words with the 1630A/D and in the edit compare mode of the 1630G. The 1630G has a full compare mode in which the entire trace may be compared.

* Three ORed clocks given in single-phase or two-phase demultiplexing modes.

* Data sampling up to 25 MHz.

* 1024 states available in memory after a trace.

* A State Chart of any user-defined label can be displayed.

* State analysis can be armed by the timing analysis section.

* A State Histogram of any user-defined label can be shown.

* A Time Interval Histogram of the time software takes to execute from one selected point in software to another.

* Time Positional measurements for the occurrences of an event per unit time may be made. (1630G only)

* Linkage measurements which show the relative frequency of occurrence of a set of events. (1630G only)

TIMING ANALYSIS. The timing analysis function of each system features:

* Sampling ranges from 10 nS to 500 mS, in increments of 1, 2, and 5.

* Timing waveforms that can be magnified from X1 to X40 in 1, 2, and 4 increments.

* Time between dual cursors (x and o) can be displayed to within 1 sample period.

* 1024 samples available in memory after a trace.

* Timing analysis can be armed by the state analysis section.

* Timing can be triggered by an asynchronous pattern, ANDed with a glitch or edge on any channel, and patterns that exceed or fall short of a specified time limit.

1-5. ACCESSORIES SUPPLIED

The following accessories are supplied with the 1630:

1630A: Three 10-bit 10271A State Probes and one 8-bit 10272A State/Timing Probe.
1630B: Three 10-bit 10271A State Probes and two 8-bit 10272A State/Timing Probes.
1630G: Three 10-bit 10271A State Probes, three 10-bit 10273 State Probes, and one 8-bit 10272A State/Timing Probe.
ALL: One 2.3 meter (7.5 ft) power cord.
One Hewlett-Packard Interface Loop (HP-IL) cable.
One Operating Manual.

1-6. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics, not specifications but typical characteristics included as additional information for the user.

Table 1-1. Input Specifications

CLOCK REPETITION RATE:

Single Phase: 25 MHz with single clock and single edge specified. 20 MHz with any ORed combination of clocks and edges.
Multiplexed: Master clock must follow slave clock by at least 10 nS and precede next slave clock by 50 nS or more.

CLOCK PULSE WIDTH: >= 20 nS at threshold.

SETUP TIME: Time data must be present prior to clock transition, >=20 nS

HOLD TIME: Time data must be present after clock transition, 0 nS

INPUT RC: 100K ohms +/- 2% shunted by approximately 5 pf at probe body.

MIN SWING: 600 mV p-p

MIN INPUT OVERDRIVE: 250 mV or 30% of input amplitude, whichever is greater.

MAX VOLTAGE: +/- 40 volts peak

THRESHOLD RANGE: -9.9 to +9.9 volts in 0.1 volt increments, Accuracy 2.5% +/-120 mV.

DYNAMIC RANGE: +/- 10 volts about threshold.

GLITCH: Minimum detectable glitch is 5 nS width at threshold. With glitch detection ON, number of timing channels is halved.

Table 1-2. Supplemental Characteristics

POWER:

115 VAC: -22% to +10% (90 - 127 VAC)
230 VAC: -22% to +10% (180 - 253 VAC)
Frequency Range: 48 to 66 Hz
275 Watts Maximum

OPERATING ENVIROMENT:

TEMPERATURE: 0 to +55°C (32 to 131°F)
HUMIDITY: Up to 95% relative humidity at +40°C (non-condensing)
ALTITUDE: To 4600 meters (15 000 feet)
VIBRATION: Vibrated in three planes for 15 minutes each with 0.3mm excursions at 5 to 55 Hz.

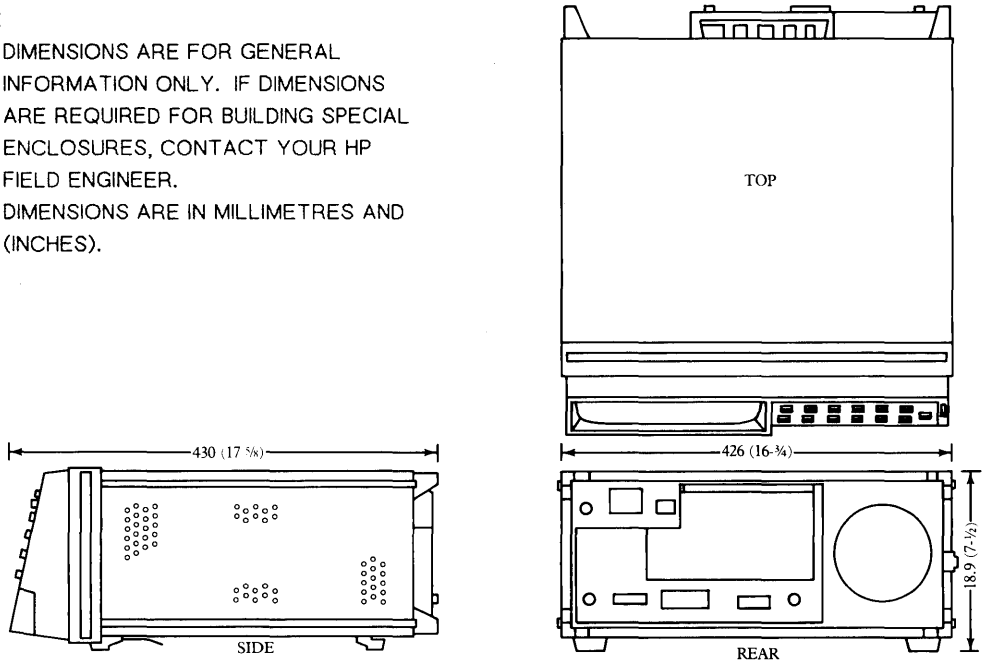
WEIGHT:

1630A: net 12.6 kg (28 lbs); shipping 17 kg (38 lbs).
1630B: net 13.2 kg (29 lbs); shipping 17.7 kg (39 lbs).
1630G: net 13.6 kg (30 lbs); shipping 18.1 kg (40 lbs).

DIMENSIONS:

NOTES:

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



1-7. RECOMMENDED TEST EQUIPMENT

Table 1-3 lists the equipment required to adjust and troubleshoot the 1630A/D/G. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 1-3.

Table 1-3. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE *
Desktop Computer	HP 85A-Compatible BASIC HP-IB Interface	HP 85F Interfacing System + 82903A 16K memory module	P,A,T
Signature Multimeter	HP-IB Controllable, with DVM Range: -50V to +50V DC Accuracy: +/- 0.01%	HP 5005B	P,A,T
Oscilloscope	Dual channel, delayed sweep. Bandwidth: dc to 275 MHz. Time Interval Measurements with 10 picosecond resolution and +/-50 picosecond accuracy	HP 1726A With standard HP 10017A probes (10:1)	P,A,T
Current Tracer		HP 547A	T
Electronic Tool	No substitute	ET19776	P,T
Portable Fan	Supplies moving air to cool PC Boards in the service slot. (REQUIRED)		A,T

* P=Performance Testing, A=Adjustments, T=Troubleshooting

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section contains the initial operation information for the Model 1630A/D/G. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

2-2. PREPARATION FOR USE

2-3. POWER REQUIREMENTS. The 1630A/D/G requires a power source of either 115 or 230 VAC -22% to +10%; single phase, 48 to 66 Hz; 275 watts maximum.

CAUTION

The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input line voltage.

2-4. LINE VOLTAGE SELECTION. Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage. The 6 Amp fus installed satisfies both voltage settings of 115 and 230 VAC.

2-5. POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See figure 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are listed in the parts list in Section VI.

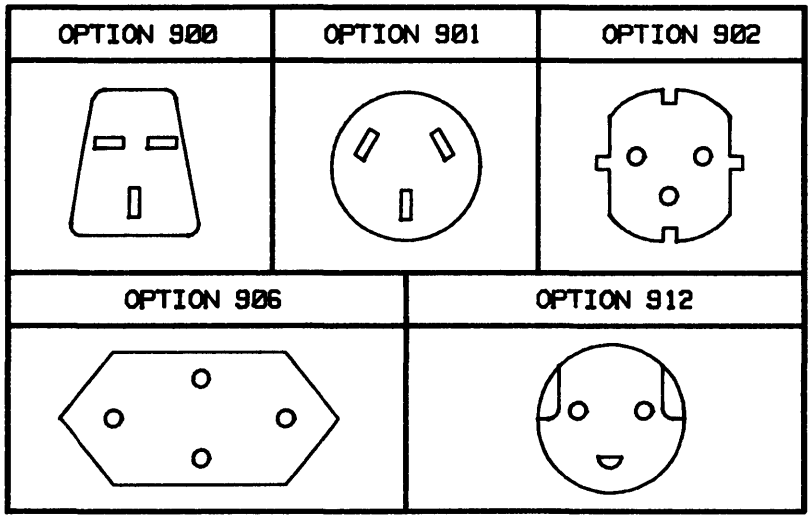


Figure 2-1. Power Cord Configurations

2-6. OPERATING ENVIRONMENT

The operating environment is noted in table 1-2. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

The 1630A/D/G will operate to all specifications, within the temperature and humidity range given in table 1-2. However, reliability is enhanced by operating the instrument within the following ranges:

Recommended Temperature: 20 to 35°C (68 to 95°F)

Recommended Humidity: 20 to 80% non-condensing

High temperature/humidity combinations should be avoided.

2-7. CLEANING REQUIREMENTS

When cleaning the 1630A/D/G, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys.

2-8. STORAGE AND SHIPMENT

2-9. Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature:	-40°C to +75°C
Humidity:	Up to 90% at 65°C
Altitude:	Up to 15 300 metres (50 000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

2-10. Packaging

2-11. TAGGING FOR SERVICE. If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-12. ORIGINAL PACKAGING. If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-13. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III
OPERATION

3-1. INTRODUCTION.

The operation of the 1630G is outside the scope of this service manual. However, a brief explanation of the operation of each key is given below. For more complete operating instructions refer to the Operators Manual.

❶ **BLUE KEY**: This key activates the blue **SHIFT** function assigned to each keyboard key. A momentary press activates the **SHIFT** function for the next keystroke. The **SHIFT** function continues if the key is kept depressed.

❷ **INPUT DISPLAYS**: Three keys that select menu sets. **SYSTEM** calls up menus that define instrument configuration, set up secondary configurations and outputs for peripherals, and control disk or tape operations (if connected and active). **FORMAT** has three menus that determine how data is collected and interpreted on the display. **TRACE** is a series of menus that specify the measurement mode and parameters for collecting data.

❸ **OUTPUT DISPLAYS**: Three keys that select a state display (**LIST**) timing display (**WFORM**), or performance overview chart (**CHART**).

❹ **LINE** turns on operating power.

❺ **RUN** initiates a new measurement. **RESUME** continues an incomplete measurement that was halted by the **STOP** key.

❻ **STOP** terminates a measurement. **RETURN TO LOCAL** overrides an HP-IB or HP-IL controller to return control of the 1630 to the keyboard.

❼ **PRINT** commands the current display to be printed on a graphics printer. **PRINT ALL** prints the entire contents of the displayed menu or list, including all on- and off-screen information.

❽ Hex keyboard for data entry.

❾ **NEXT** [] and **PREV** [] keys cycle through all the menu selections available for fields enclosed in brackets, [].

❿ **CHS** is used to change +/- signs when specifying memory locations in either direction from the trigger event, and when specifying polarities. **CHS** prints a dash when used in a text field.

⓫ **DON'T CARE** enters an "X" in lieu of a number, to indicate "any value will serve".

⓬ **CURSOR**: These keys move the cursor from field to field in the menus. The blue **SHIFT** function allows these keys to rearrange the order of labels in the menus, and to move the cursor from pod to pod in the lable lines of the FORMAT [Assignment] menu. The **CURSOR** keys can also move the configuration bar in the SYSTEM [Configuration] menu, and the "x" and "o" markers on the waveform and chart displays.

⓭ **ROLL** keys move timing displays left or right, state lists up or down, and the configuration bar in the SYSTEM [Configuration] menu.

⓮ **INSERT/DELETE** are used to add or delete fields and labels.

⓯ **CLEAR ENTRY**: This is the field eraser key. **DEFAULT** returns all fields in the displayed menu to power-up conditions.

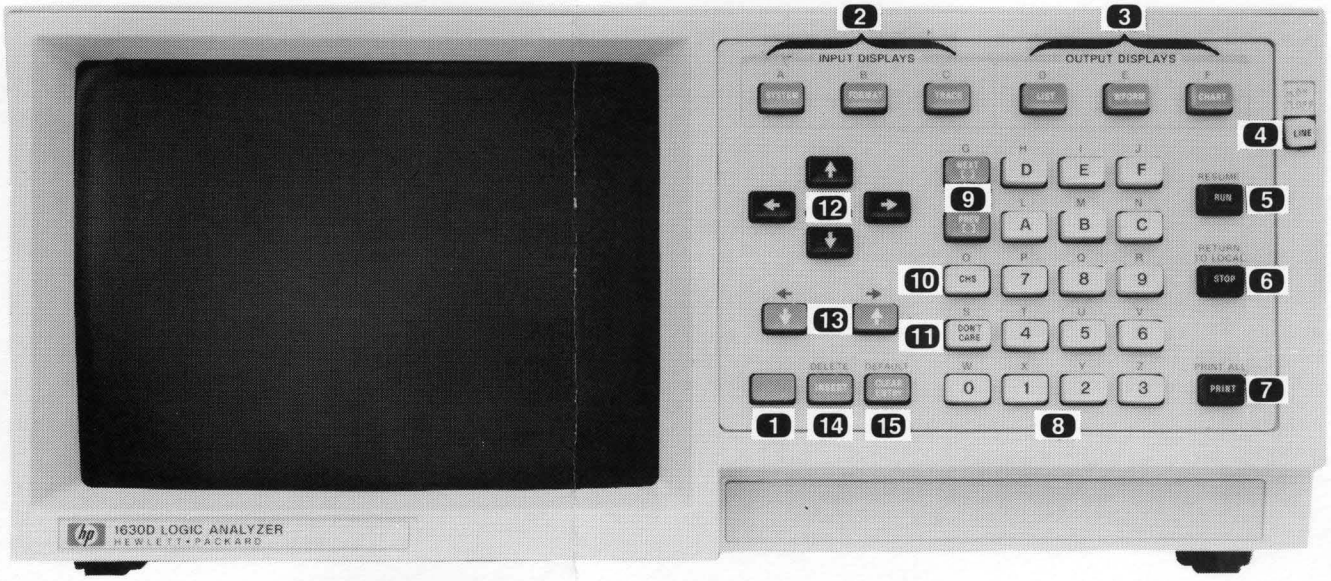


Figure 3-1. Front Panel Controls

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

This section will acquaint the user with the 1630A/D/G Self Tests (ST). ST is a series of tests, resident in ROM, that confirms correct operation of the mainframe hardware and firmware. The ST tests do not verify all of the critical input specifications given in table 1-1 of Section I. These tests check the basic functions of the system. For complete Performance testing, perform the Operation Verification Tests in Appendix A and the Parametric Verification Tests in the ET19776 Manual.

Note: The terms MPU or processor, and MMU will be used throughout this manual in reference to the Microprocessor Unit and the Memory Management Unit used on the CPU board.

4-2. EQUIPMENT REQUIRED

Equipment required for the self tests is listed in table 1-3, Recommended Test Equipment, Section I.

4-3. SELF TEST FUNCTION VERIFICATION

4-4. Initiating 1630A/D/G Self Test (ST)

ST can be initiated by setting the rear panel Self Test switch into the "1" or open position and cycling power OFF/ON.

NOTE

The processor samples the setting of the system status switches ONLY during turn-on. Changing SW1 to "1" after turn-on will not initiate SELF TEST. Cycling the power OFF/ON will reset the switch status. After ST is executed, however, the ST switch may be set to a "0" allowing the System Specification menu to be displayed without cycling power.

After power is cycled OFF/ON and an initialization routine is executed, the ST routine will begin. The ST test sequence is as follows:

a. RAM test.

b. ROM test.

c. Acquisition test.

d. Internal Storage test (1630G only).

e. HP-IB test (1630G only).

4-5. 1630A/D/G ST RAM Test Procedure

PURPOSE:

The RAM test verifies the MPU's and MMU's ability to read and write from all 64K RAM locations on the CPU board.

CIRCUITRY TESTED:

RAM, MPU and MMU interaction, RAM refresh by the CRT controller, RAM strobe timing circuitry, and ROM selection and data transfer.

OPERATION:

a. Before the RAM test begins, an initialization routine is done for the CRT controller (CRTC). This initialization routine reads the rear panel switches, etc.

b. The processor configures the memory management unit (MMU) to map a 2K (800H) block of RAM.

c. The processor (MPU) writes a 01, 02, 03, ... 80, 00 hex pattern sequentially through each 2K block of RAM. The pattern used is derived by shifting-left the contents of the A accumulator.

d. After all 64K of RAM is mapped, the processor sequentially reads back the contents of RAM. The value stored is compared to the present value of the A accumulator.

e. If the value stored does not match the present value of the A accumulator, then an "Error in RAM" message is displayed.

f. If after all 64K of RAM is tested and no compare error exists, then a ROM and Acquisition test is performed.

ERROR MESSAGE INTERPRETATION:

If an "Error in RAM" message is displayed, check RAM inputs and outputs for bad signals. If this does not fix the problem, refer to the Guided Probe Troubleshooting Procedure in Appendix A of this manual.

4-6. 1630A/D/G ST ROM Test Procedure

PURPOSE:

The ROM test verifies that all of the firmware is good. The test also checks that the processor (MPU) and memory management unit (MMU) can address and retrieve data from ROM.

CIRCUITRY TESTED:

All ROMs, MPU and MMU interaction, ROM selection and data transfer, and RAM.

OPERATION:

a. Before the ROM test begins, the RAM test must have passed.

b. The processor configures the MMU to map an 8K block of ROM.

c. Information is read from ROM and a checksum routine is done for each ROM. The checksum for each ROM is compared to a stored checksum value of that ROM in ROM #7 (U4H).

d. If the checksums do not match, then a "Error in ROM #X Expected XX Was XX" message is displayed.

e. If all of the checksums match, then an Acquisition test is performed.

ERROR MESSAGE INTERPRETATION:

If an "Error in ROM #X(0-7) Expected XX Was XX" message is displayed, it is interpreted as follows:

Error in ROM #X(0-7) - X indicates the faulty ROM number given as:

U3K = ROM #0	U4K = ROM #4
U3J = ROM #1	U4J = ROM #5
U3I = ROM #2	U4I = ROM #6
U3H = ROM #3	U4H = ROM #7

Expected XX - indicates the stored checksum value in ROM #X for that ROM (given in hex).

Was XX - indicates the checksum tabulated for that ROM during the test (given in hex).

If after replacing the suspect ROM, the failure still exists, refer to the Guided Probe Troubleshooting Procedure in Appendix A of this manual.

4-7. 1630A/D ST Acquisition Test Procedure

PURPOSE:

This test verifies the processor's ability to configure the system to take a state measurement. It also verifies that all pod channels can sample data between -9.9 and +9.9 volts.

CIRCUITRY TESTED:

This test checks the processor, system timing control, state and timing boards, and the probes.

OPERATION:

a. Both RAM and ROM tests must have passed before this test begins.

b. The processor configures the system for a Trace Specification of <don't care start-on any state, trace all states>.

c. System starts tracing with pods 4, 2, 0 thresholds set at +9.9 volts and pods 3 and 1 set at -9.9 volts. "0s" should be sampled on pods 4, 2, 0 and "1s" should be sampled on pods 3 and 1.

d. 512 states are clocked in and sampled at this threshold pattern.

e. A sample is taken for "measurement complete". It should be false.

f. The pod threshold voltages are reversed, making the sample pattern of step (c) reversed.

g. 511 states are clocked in and sampled at this threshold pattern.

h. A sample is taken for "measurement complete". It should be false.

i. The memory counter is sampled for words remaining; one should remain.

j. The last word is clocked in, making the "measurement complete" status true. The trace is then halted.

k. Any acquisition errors are summarized and the self test determines if a Timing Slave board is in the instrument. If a Timing Slave board is not in the system, errors are ignored for the Timing Slave channels.

l. If no errors occurred "Self Test Passed Reset Rear Panel Switch to xxxx xOxx to continue" message should be displayed. When the switch is reset the System Specification menu should be displayed.

m. If an error occurred, a "Acq Error XX XX XX XX XX XX XX" message will be displayed in hex. See the error message interpretation on the next page.

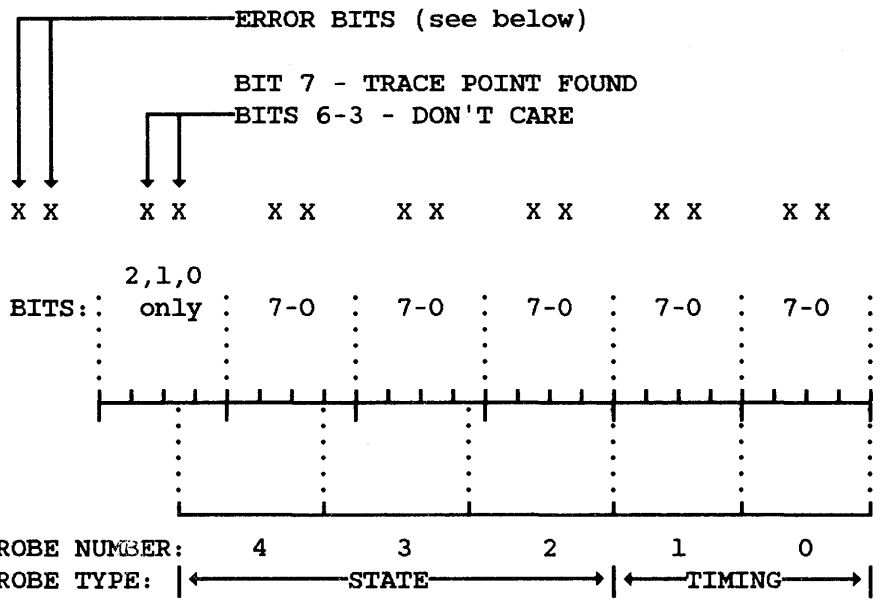
1630A/D ERROR MESSAGE INTERPRETATION:

The acquisition error (Acq Error) is a series of hex digits. The binary equivalent of these digits can be interpreted with the following table.

The series of XXs (in hex code) follows the phrase "Acq Error" on the 1630A/D display.

*****KEY*****

1 = Error (except Don't Cares)
0 = No Error



POD 1 SPECIAL CASE: If a Slave Timing board is not in the instrument (1630A), the test will show channels 16-9 as passing.

Bit 0 - Incorrect acquisition data acquired.

Bit 1 - "Measurement Complete" true when it should be false.

Bit 2 - "Measurement Complete" IRQ true when it should be false.

Bit 3 - Words remaining. State Master board counter incorrect.

Bit 4 - "Measurement complete" on State Master board false when it should be true.

Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.

Bit 6,7 - Don't Care Bits

1630A/D ERROR MESSAGE INTERPRETATION (CONT):

Two examples of an Acquisition error are given below:

Example 1:

"Acq Error 01 80 00 00 00 00 03"

a. This example states that incorrect Acquisition data was acquired.

b. Trace point was not found.

c. All channels passed except Timing Master Channels 1 and 0.

Example 2:

"Acq Error 02 0F FF FF FF 00 FF"

a. This example states that measurement complete was true when it should be false.

b. Trace point was found.

c. All Channels failed except the Timing Slave Channels. Note that if a Timing Slave board is not in the instrument (1630A) these channels will pass.

4-8. 1630G ST Acquisition Test Procedure

PURPOSE:

This test verifies the processor's ability to configure the system to take a state measurement. It also verifies that all pod channels can sample data between -9.9 and +9.9 volts.

CIRCUITRY TESTED:

This test checks the processor, system timing control, state and timing boards, and the probes.

OPERATION:

a. Both RAM and ROM tests must have passed before this test begins.

b. The processor configures the system for a Trace Specification of <don't care start-on any state, trace all states>.

c. System starts tracing with pods 7, 5, 3, and 1 thresholds set at +9.9 volts and pods 6, 4, and 2 set at -9.9 volts. "0s" should be sampled on pods 7, 5, 3, and 1 and "1s" should be sampled on pods 6, 4, and 2.

d. 512 states are clocked in and sampled at this threshold pattern.

e. A sample is taken for "measurement complete". It should be false.

f. The pod threshold voltages are reversed, making the sample pattern of step (c) reversed.

g. 511 states are clocked in and sampled at this threshold pattern.

h. A sample is taken for "measurement complete". It should be false.

i. The memory counter is sampled for words remaining; one should remain.

j. The last word is clocked in, making the "measurement complete" status true. The trace is then halted.

k. Any acquisition errors are summarized and the self test determines if a Timing Slave board is in the instrument. If a Timing Slave board is not in the system, errors are ignored for the Timing Slave channels.

l. If no errors occurred "Self Test Passed Reset Rear Panel Switch to xxxx x0xx to continue" message should be displayed. When the switch is reset the System Specification menu should be displayed.

m. If an error occurred, a "Acq Error XX XX XX XX XX XX XX XX XX XX" message will be displayed in hex. See the error message interpretation on the next page.

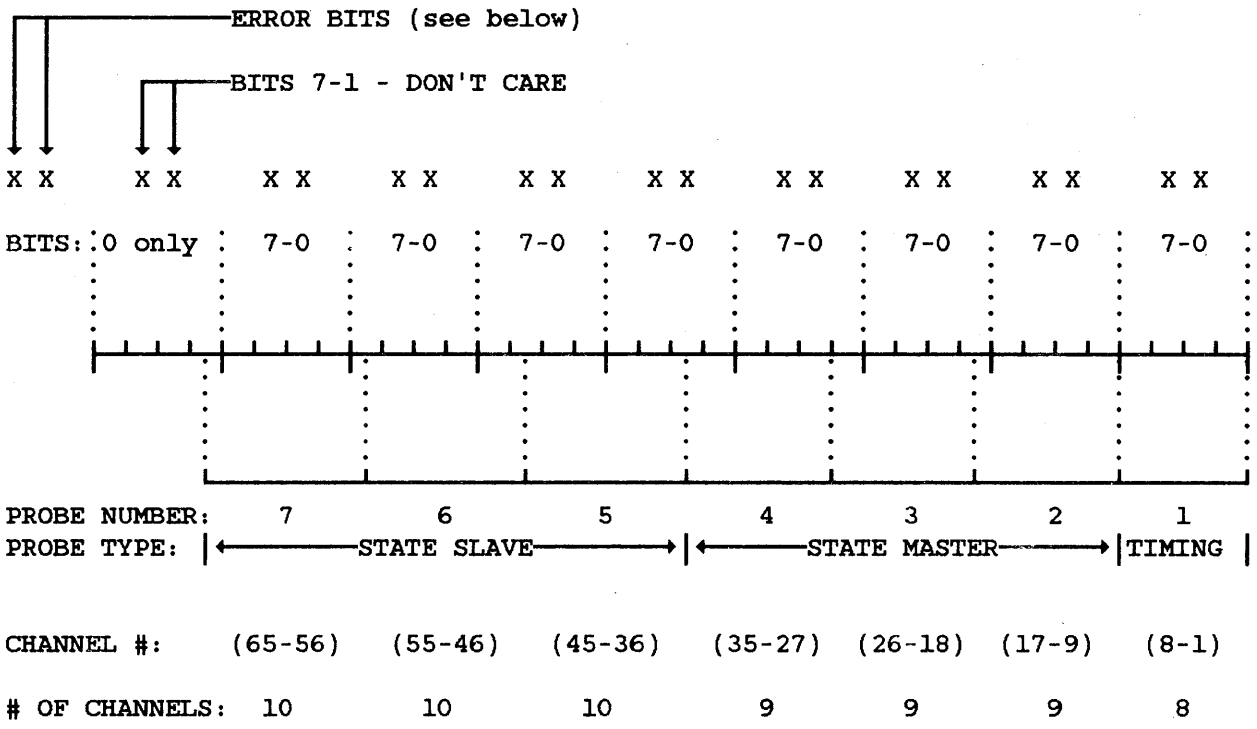
1630G ERROR MESSAGE INTERPRETATION:

The acquisition error (Acq Error) is a series of hex digits. The binary equivalent of these digits can be interpreted with the following table.

The series of XXs (in hex code) follows the phrase "Acq Error" on the 1630G display.

*****KEY*****

1 = Error (except Don't Cares)
0 = No Error



CHANNEL #:	(65-56)	(55-46)	(45-36)	(35-27)	(26-18)	(17-9)	(8-1)
# OF CHANNELS:	10	10	10	9	9	9	8

Bit 0 - Incorrect acquisition data acquired.

Bit 1 - "Measurement Complete" true when it should be false.

Bit 2 - "Measurement Complete" IRQ true when it should be false.

Bit 3 - Words remaining. State Master board counter incorrect.

Bit 4 - "Measurement complete" on State Master board false when it should be true.

Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.

Bit 6,7 - Don't Care Bits

1630G ERROR MESSAGE INTERPRETATION (CONT):

Two examples of an Acquisition error are given below:

Example 1:

"Acq Error 01 80 00 00 00 00 00 00 00 03"

a. The "1" indicates that the measurement completed prematurely.

b. The "8" indicates that the trace point was not found.

c. All channels passed except Timing Master Channels 1 and 0.

Example 2:

"Acq Error 02 0F FF FF FF FF FF FF FF FF"

a. The "2" indicates that the measurement complete was true when it should be false.

b. Trace point was found.

c. All Channels failed as indicated by the "F"s.

4-9. 1630G Internal Storage Test and Reset

When an error is found in internal storage the following will be displayed on the screen:

"Internal checksum error"

It is necessary then for the 1630G to reset internal storage. This will be done automatically by the 1630G and the message "WAIT Resetting internal storage" will be displayed. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed.

To manually reset internal storage, toggle switch 1 of the HP-IB address switch. The message "WAIT Resetting internal storage" will appear on-screen while the reset is taking place. When the reset has been completed successfully, the message "Internal storage reset successful" is displayed. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed on-screen.

The analyzer may be used without the internal storage and the rest of the performance of the analyzer is not affected.

4-10. 1630A/D/G KEYBOARD TEST PROCEDURE

The Keyboard test is not part of the Self Test routine. Data must be loaded in from an external controller to run this test.

a. Refer to the 1630A/D PROGRAM TAPE LOADING PROCEDURE in Appendix A.

b. Check that the 1630 under test is in the System Specification menu.

c. Press the < KEYBRD > softkey. The 1630A/D display should display the keyboard pattern shown in figure 4-1.

d. Press the keyboard switches shown on the display; the key pressed will erase from the screen as it is pressed if the board is working correctly.

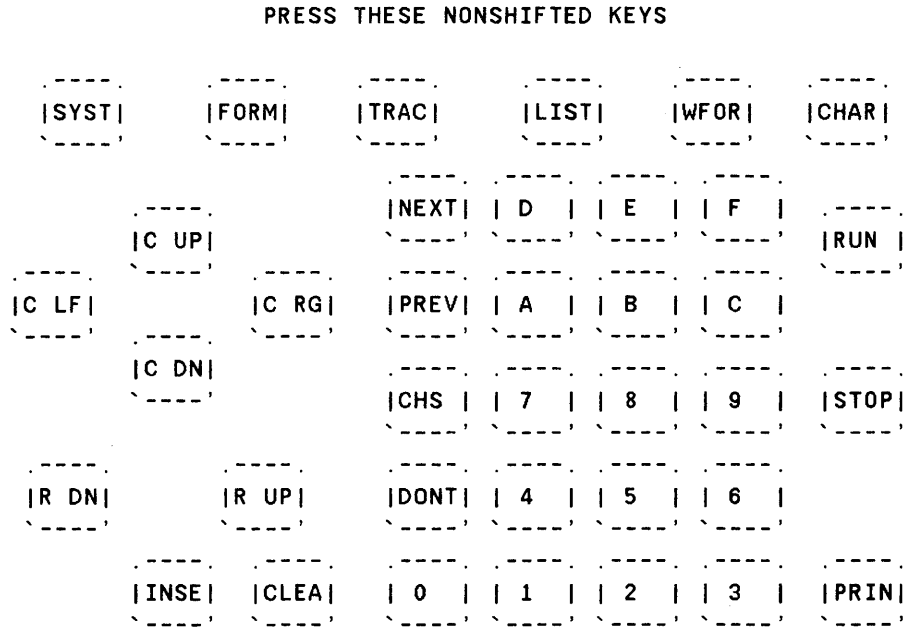


Figure 4-1. Keyboard Test Pattern

b. When all the keys have been pressed, the display will change to look like figure 4-2. While holding down the blue key, press each of the indicated keys.

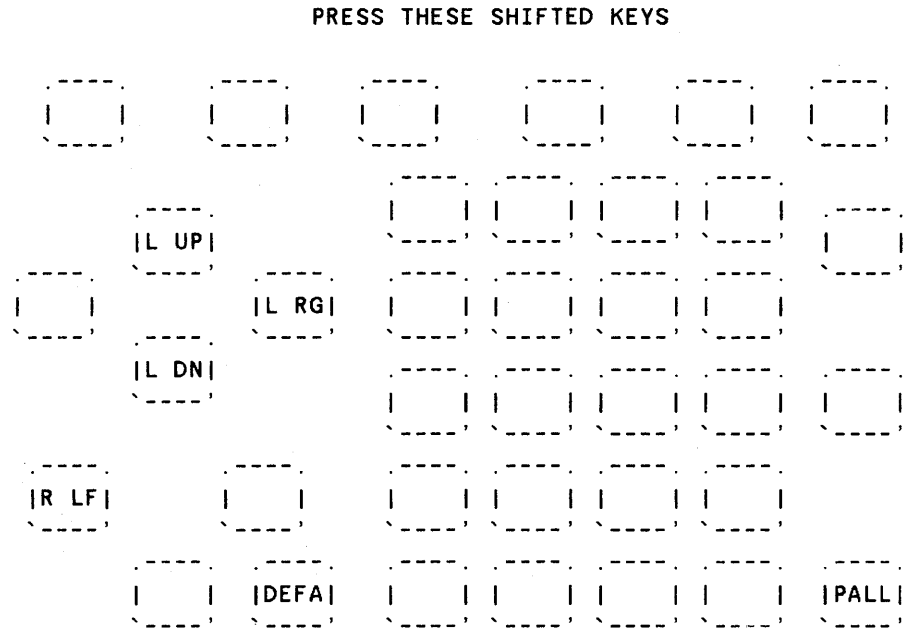


Figure 4-2. Keyboard Test Pattern Part 2

c. When all of the keys have been sucessfully pressed, the display will indicate "KEYBOARD TEST PASSED". Then, after a short pause the 1630A/D/G display will return to the System Specification menu.

d. If a key is bad it will not be erased from the display. Cycle power to abort the test if a key fails.

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

This section contains adjustment procedures for the power supply, display driver, and the Timing Master board. Perform the adjustment procedure only after instrument repairs. The adjustments can be made separately. The adjustment procedures used apply to all instruments.

Board removal procedures, necessary before installing boards into the service connector, can be found in Section VIII. An auxiliary fan must be used to cool boards being run in the service connector.

WARNING

Read the safety summary at the front of this manual before performing adjustment procedures.

CAUTION

The adjustments are performed with the top and side covers removed. Use care to avoid shorting or damaging internal parts of the instrument.

5-2. EQUIPMENT REQUIRED

A list of recommended test equipment is provided in Section I, table 1-3.

5-3. POWER SUPPLY ADJUSTMENT

a. Turn OFF 1630A/D/G and remove power cord.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover. Remove cover.

c. Connect an external DVM to measure volts between GND and -5.2V on test connector TP2 (bottom-left of board).

d. Plug in power cord and turn ON the 1630A/D/G.

e. Adjust trimpot R34 (labelled VOLT ADJ) until the measured value of -5.2V reads between -5.0 and -5.4 volts. Measure the +5.0V supply; it should be between +4.8 and +5.2 volts.

f. Adjustment complete. Replace covers.

5-4. CPU ADJUSTMENT

a. Refer to the CPU Board Removal procedure in Section VIII and perform the removal procedure.

b. With power OFF, install the CPU board into the upright Service connector J1.

c. Connect the cables from the keyboard and display driver.

d. Place the intrument's top cover over the exposed power supply to prevent tools from dropping onto the power supply, and to maintain proper air flow.

e. Connect a DVM to one of the following locations depending on the CPU board under test:

01630-66503 CPU board: U100 pin 6 and GND on U100 pin 4.

01630-66512 CPU board (and later CPUs): TP4 "+5V REF" and TP GND on the CPU test connector located at the top-left of the board.

f. Turn ON the 1630A/D/G.

g. Adjust trimpot R37 (located at the bottom-right) until the voltage at TP4 reads +5.00 volts +/-5 mV.

h. Adjustment complete. Replace board and covers.

5-5. DISPLAY SYSTEM ADJUSTMENTS

This adjustment procedure is in two parts; yoke and display driver. The Yoke Adjustment Procedure must be performed if any part of the Display System is replaced (CRT, display driver, or yoke) or if a display cannot be aligned on the CRT screen. If the Yoke Adjustment Procedure is performed then the Display Driver Adjustment Procedure must also be done; if not, then the latter may be done alone. It is good practice to discharge the CRT before beginning.

YOKE ADJUSTMENT PROCEDURE

a. Turn OFF 1630A/D/G.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove cover.

c. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

d. Remove the two yoke connectors.

e. Insure that the yoke is firmly pressed against the flange of the CRT. If not, loosen the yoke neck screw that attaches the yoke to the CRT and slide the yoke against the CRT. Gently tighten the screw until firm.

f. While holding a flexible straight edge from the lower-left corner to the upper-right corner of the CRT (facing the CRT), make a mark about one inch long with a water soluble felt pen across the center of the CRT. See figure 5-1.

g. Repeat the above step for the upper-left corner and the lower-right corner forming an "X" in the center of the CRT. See figure 5-1.

h. Adjust BRIGHTNESS control pot to minimum (full counter-clockwise). See figure 5-2 for the display adjustment locations.

i. Turn ON the 1630A/D/G.

j. Adjust BRIGHTNESS control pot until a dot appears on the CRT.

k. The dot should appear within a .3 cm (1/8 inch) radius of the intersection of the two lines. If this does not occur, align the dot using the centering rings on the yoke. See figure 5-1.

l. Turn OFF the 1630A/D/G and clean the CRT screen with mild soap and water.

m. Reconnect the two yoke connectors from the display driver.

n. Perform the Display Driver Adjustment Procedure.

DISPLAY DRIVER ADJUSTMENT PROCEDURE

a. Turn OFF the 1630A/D/G.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove cover.

c. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

d. Refer to the 1630A/D/G PROGRAM TAPE LOADING PROCEDURE in Appendix A at the back of this manual.

e. Activate the Display Test Pattern as shown in figure 5-3 by pressing the < DISPLAY > softkey on the HP85.

f. Adjust the BRIGHTNESS control pot until the Display Test Pattern is visible. See figure 5-2 for the display adjustment locations.

g. Adjust the HEIGHT and VERT PHASE (position) until the Test Pattern fills the screen vertically. See figure 5-3.

h. Adjust HORIZ LINEARITY until the width of each square is the same.

i. Adjust HORIZ WIDTH until the total picture width is the same as the width of the outer boundary marks given in figure 5-3. Note that the outer edges of the display may NOT align with the outer boundary marks.

NOTE

The adjustments in steps (h) and (i) interact. Therefore reiteration of these two steps may be necessary for best results.

j. Now adjust the horizontal position by rotating the centering rings on the yoke. Adjust the rings for horizontal movement while minimizing the vertical movement of the display. The left and right edges should NOW align with outer boundary marks described in the previous step.

k. Adjust VERT PHASE to vertically align the Test Pattern. This should only require minor adjustments. See figure 5-3 for this measurement.

l. Set the CRT intensity in the "INTENSITY ADJUST AREA" of the test pattern to a comfortable level. However, if a photometer is available adjust the BRIGHTNESS control until the reading is 20 +/- 1 foot Lamberts.

m. Adjust FOCUS control to achieve the best display in the area of the test pattern labeled "FOCUS AREA".

n. Verify that the area of the test pattern labeled "BLINKING CURSOR" does contain a blinking rectangular cursor flashing several times per second. If there are two different video levels but no flashing, the CPU board is defective. If there is no difference in video levels, the display board is defective. Refer to the CPU, Keyboard and Display Service Group 8B for troubleshooting information.

o. The HOR HOLD adjustment has been pre-adjusted by the manufacturer and should not need to be changed.

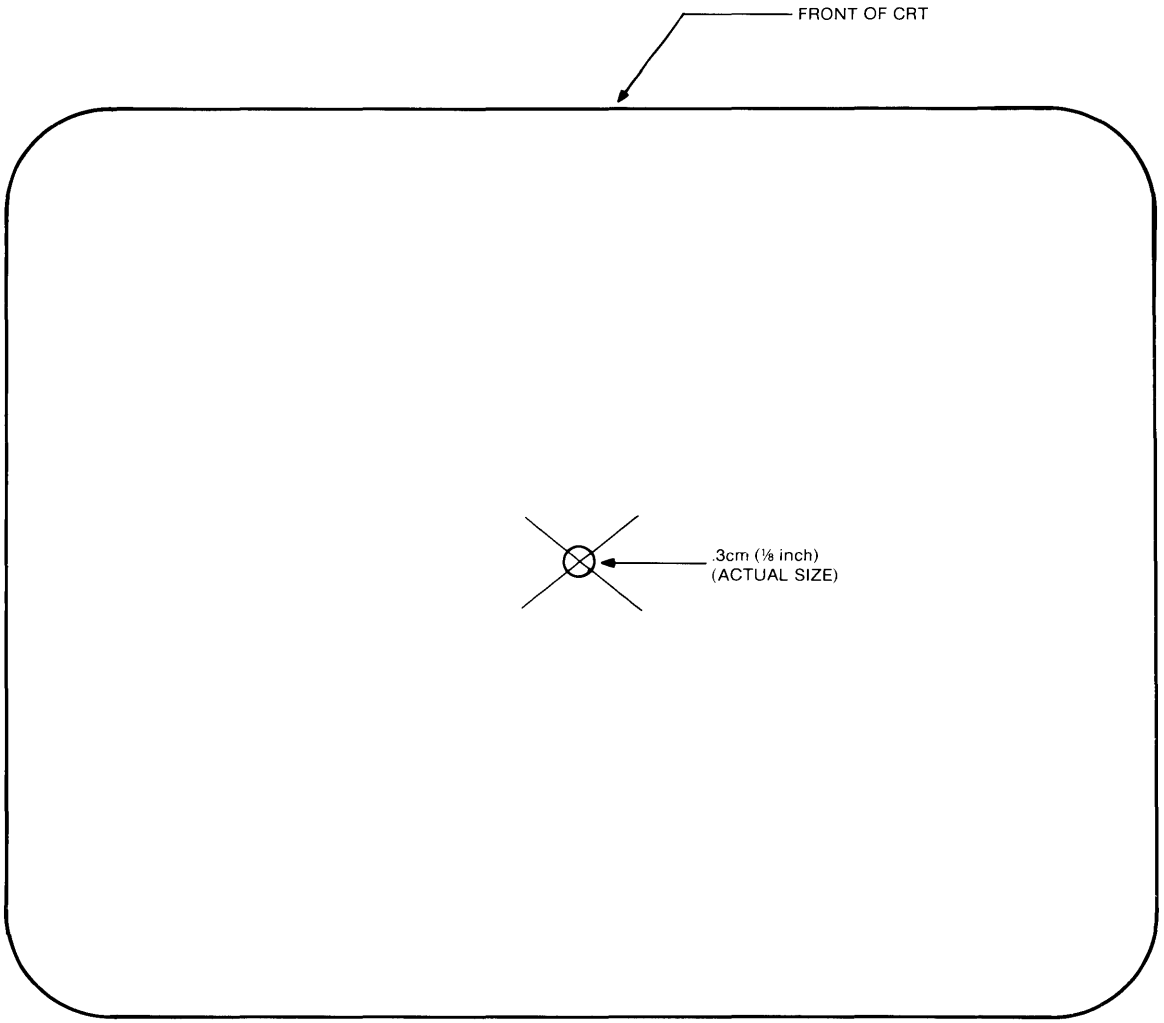


Figure 5-1. Yoke Centering Adjustment

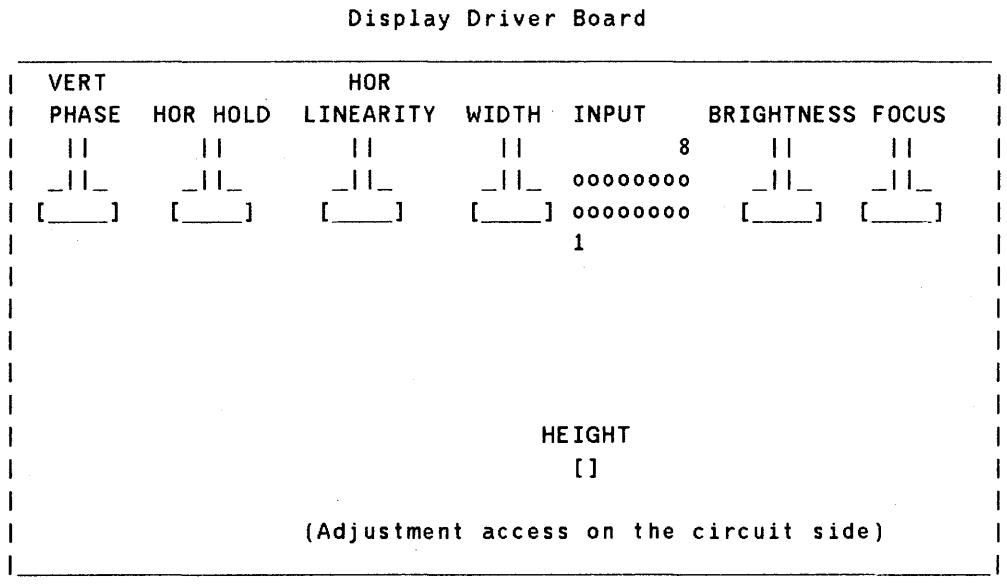


Figure 5-2. Display Adjustment Locations

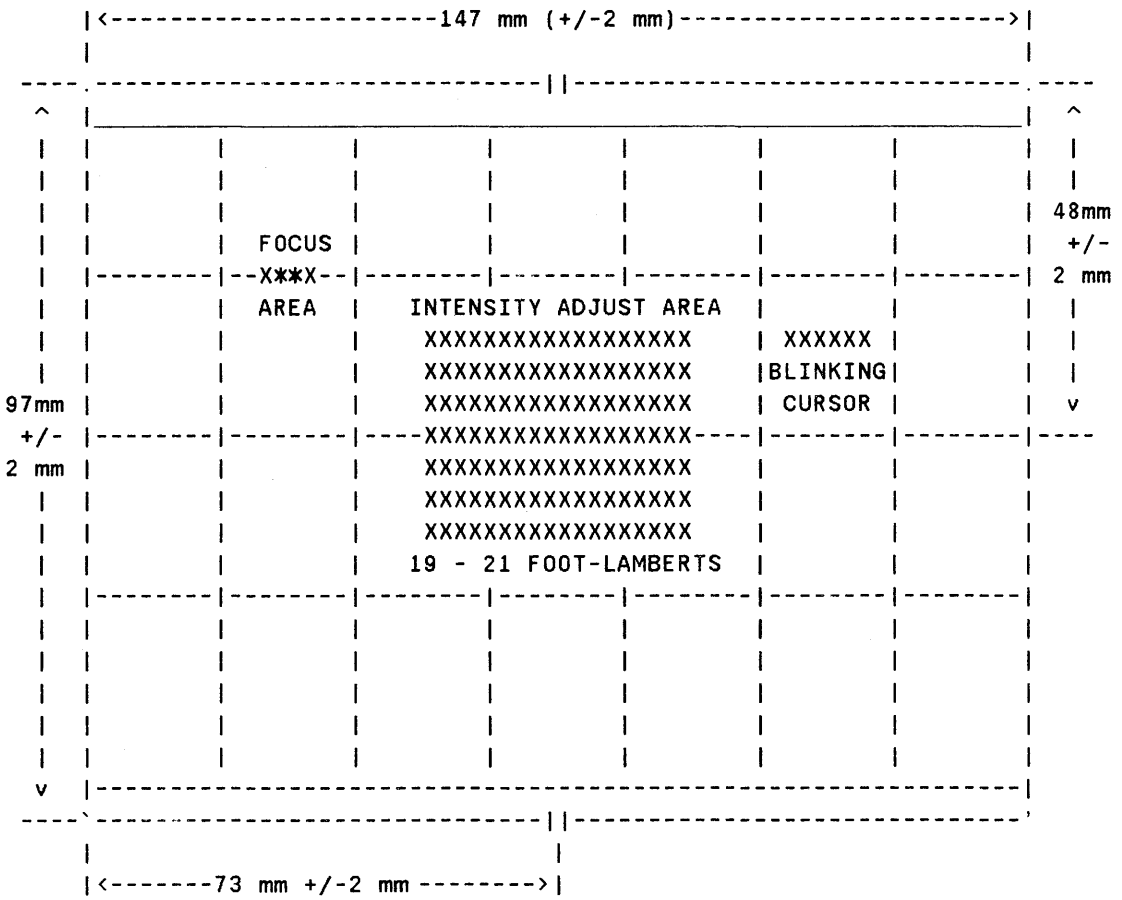


Figure 5-3. Display Test Pattern

5-6. TIMING MASTER ADJUSTMENT (200 MHz OSCILLATOR)

NOTE

A portable fan must be used to maintain airflow across the macrocells.

a. Refer to the Acquisition Board Removal procedure in Section VIII and perform the removal procedure for the Timing Master board.

b. With the power OFF, install the Timing Master board into the upright Service connector J1. A probe doesn't need to be connected.

c. Connect Channel A of the oscilloscope to TP1 on the Timing Master board (located at the left-middle of the board) and adjust the scope as follows:

Set Volts/div to .01 V/div AC coupled.
Set MAIN Time Base to .01 uS/div. MAG X10.
Set TRIGGER to Channel A.
Set DISPLAY to ALT.
Use MAIN triggering.

d. Turn ON 1630A/D/G and check for the presence of a 200 MHz signal (+ or - .01% tolerance) at TP1.

e. If the 200 MHz signal doesn't exist, adjust trimcap C26 until a 200 MHz signal appears.

f. Continue adjusting trimcap C26 until the 200 MHz oscillation shows maximum amplitude.

g. Discontinue the oscillations by touching a screwdriver to the collector of the high-frequency transistor Q1. Remove the screwdriver and verify that the oscillator locks again to 200 MHz.

h. If the oscillations do not re-occur after being discontinued, adjust C26 until the oscillations begin again. Leave C26 at this setting and repeat step (g).

i. Adjustment complete. Replace board and covers.

5-7. STATE MASTER BOARD ADJUSTMENT

a. Refer to the Acquisition Board Removal procedure in Section VIII and perform the removal procedure for the State Master board.

b. With the power OFF, install the State Master board in the upright Service connector J1.

c. DO NOT connect any state probes to the board. The Timing Master board must be installed.

5-8. 1726A Scope Setup

The scope probes must be calibrated at the beginning of each calibration session to eliminate timing errors due to different electrical lengths in the scope probes.

a. Connect both A and B channels of the HP 1726 scope to the front panel CAL signal on the scope.

b. Select ALTERNATE display mode. Position both A and B grounds to the uppermost graticule line.

c. Set scope controls to the following:

VOLTS/DIV: 0.5 V/div for both channels, DC COUPLED.
Select DELAYED Time Base.
Set DLYD Time Base to .01 uS/div.
Set MAIN Time Base to .1 uS/div.
Turn Time Interval START knob fully CCW.
Set TRIGGER to Channel A.

d. Adjust the Time Interval STOP knob until the delay between channels is ZERO on the scope digital readout. Adjust the Time Interval START knob if necessary. Two waveforms will appear on the scope display.

e. Use a small screwdriver to adjust the SIGNAL OVERLAP calibration trimmer so that the signal waveforms overlap directly.

f. The HP 1726A oscilloscope is calibrated when the digital readout displays ZERO Delta-T and the two scope waveforms directly overlap.

5-9. Width Adjustment

a. Connect Channel A of the 1726A to TP1 on the State Master board. Connect Channel B to TP2 on the State Master board.

b. Refer to the 1630A/D PROGRAM TAPE LOADING PROCEDURE in Appendix A of this manual. Press the < strobe > softkey on the HP85.

c. Set the scope controls to the following:

VOLTS/DIV: .05 V/div, DC coupling.
DISPLAY: Channel B.
TRIGGER: Channel B, rising edge.
Set DLYD Time Base to 10 nS/div.
Set MAIN Time Base to 20 nS/div.
Delta Time Trigger: Overlap Mode, START LVL=STOP LVL.
Time Interval Start: Rising Edge, knob fully CCW.
Time Interval Stop: Falling edge.
Switch Delta-T ON.
Switch Fast Mode ON.

d. Set both ground lines on the scope to 2.6 divisions above the center line of the display. With this setup, -1.30 volts is at the center line of the display.

e. Adjust the trigger level until a complete pulse appears on the scope.

f. Adjust the Time Interval Stop knob until the LED display reads 17.00 ns +/- 50 ps.

g. Select Delayed Trigger. The scope CRT should show two pulses overlapping on one edge.

h. Press MAG X10. If necessary, the Horizontal Position knob can be adjusted to center the crossing point of the signals on the scope display.

i. Adjust trimpot R4 (TOP of the two trimpots located on the right-middle side of the board) so that the crossing point of the two scope traces is at -1.3V (center line of the CRT).

h. This portion of the State Master board is calibrated when the pulse width is 17.0 ns at -1.30V.

5-10 Delay Adjustment

a. Connect Channel A of the HP1726A to TP1 on the State Master board. Connect Channel B to TP2 on the State Master board.

b. Set the scope controls to the following:

Set Volts/div to .05, Coupling to DC.
Set DISPLAY to ALT.
Set TRIGGER to Channel A, rising edge.
Set DLYD Time Base to 10 nS/div.
Set MAIN Time Base to 20 nS/div.
Delta Time Trigger: Overlap Mode, START LVL=STOP LVL.
Time Interval Start: Rising Edge, knob fully CCW.
Time Interval Stop: Falling edge.
Switch Delta-T ON.
Switch Fast Mode ON.

c. Set both ground lines on the scope to 2.6 divisions above the center line of the display. With this setup, -1.30 volts is at the center line of the display.

e. Adjust the trigger level until two complete pulses appear on the scope.

f. Adjust the Time Interval Stop knob until the LED display reads 36.00 ns +/- 50 ps.

g. Select Delayed Trigger. The scope CRT should show two pulses overlapping on one edge.

h. Press MAG X10. If necessary, the Horizontal Position knob can be adjusted to center the crossing point of the signals on the scope display.

i. Adjust trimpot R5 (BOTTOM of the two trimpots located on the right-middle side of the board) so that the crossing point of the two scope traces is at -1.3V (center line of the CRT).

h. This portion of the State Master board is calibrated when the time between the rising edge of TP1 and the falling edge of TP2 is 36.0 ns at -1.30V.

5-11 STATE SLAVE BOARD ADJUSTMENT

a. Refer to the State Slave Board Removal procedure in Section VIII and perform the removal procedure.

b. With power OFF, install the State Slave board into the upright Service connector J1.

c. Place the intrument's top cover over the exposed power supply to prevent tools from dropping onto the power supply, and to maintain proper air flow.

d. Connect a DVM to TP1 and TPGND on the State Slave board under test.

e. Turn ON the 1630A/D/G.

f. Adjust trimpot R4 until the voltage at TP1 reads +5.00 volts +/-5 mV.

g. Adjustment complete. Replace board and covers.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering parts. Table 6-1 lists the abbreviations used in the parts list and throughout this manual. Figure 6-1 shows the locations of the mainframe mechanical parts (MP). Table 6-2 lists all replaceable parts for the 1630A/D/G. Table 6-3 contains the names and addresses that correspond to the manufacturers' code numbers.

6-2. ABBREVIATIONS

Table 6-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-3. PARTS LIST

Table 6-2 is a list of replaceable parts and is organized as follows:

a. Mainframe parts are listed first, by reference designator.

b. Following that, individual assemblies are listed, again in reference designator order, with the components of each assembly listed in reference designator order.

c. If an assembly has more than one part number because it has been changed, all part numbers for that assembly are listed within the assembly group, in part number order. Individual part information distinguishing an assembly part number is given with it, in reference designator order.

The information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) on each assembly.

c. Description of the part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 6-3 for a code to manufacturer breakdown.

e. The manufacturer's number for the part.

The total quantity for each part is given only once, at the first appearance of the part number in the list.

6-4. ORDERING INFORMATION

To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-5. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

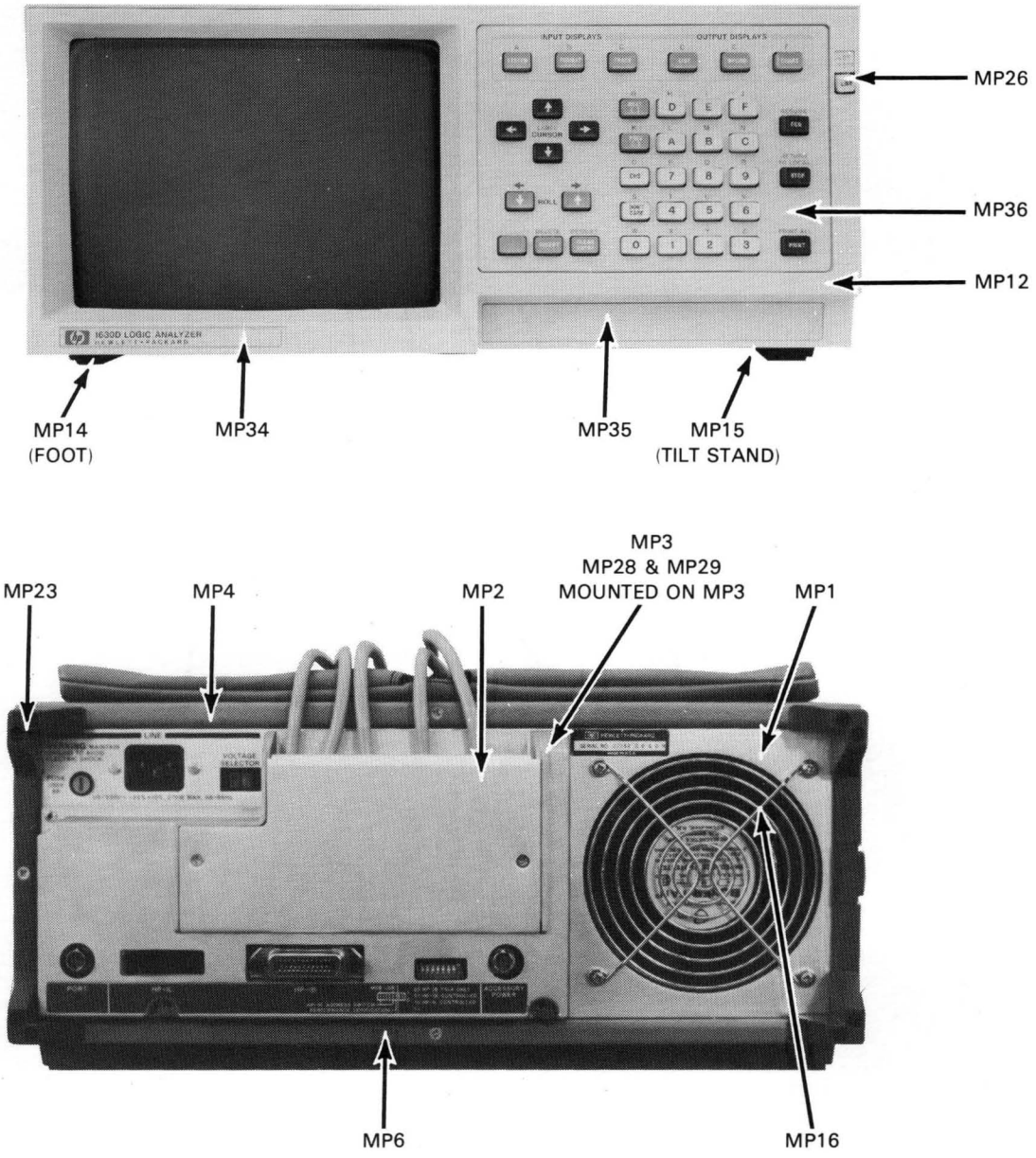
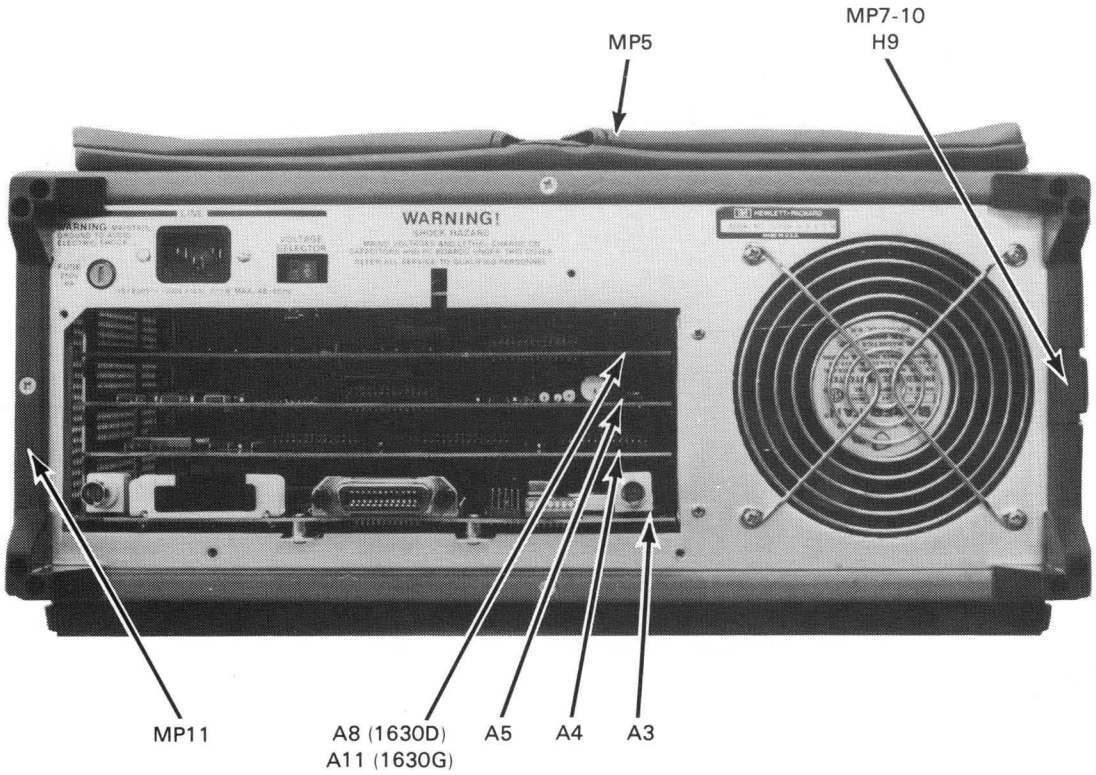


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 1 of 4)



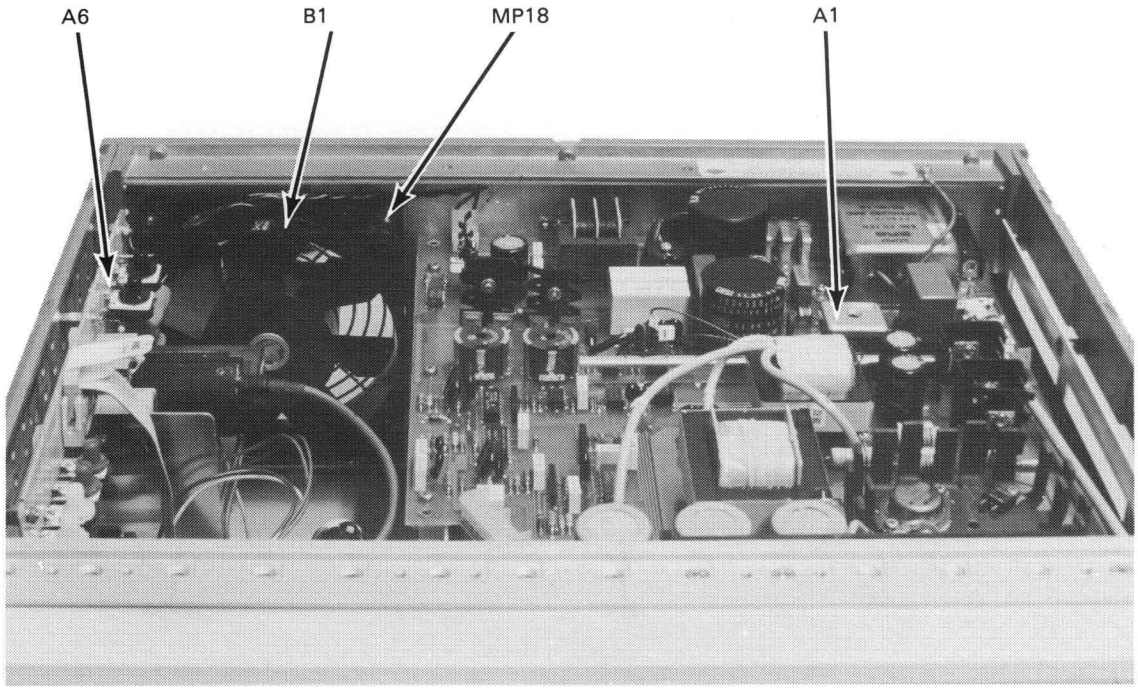


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 2 of 4)

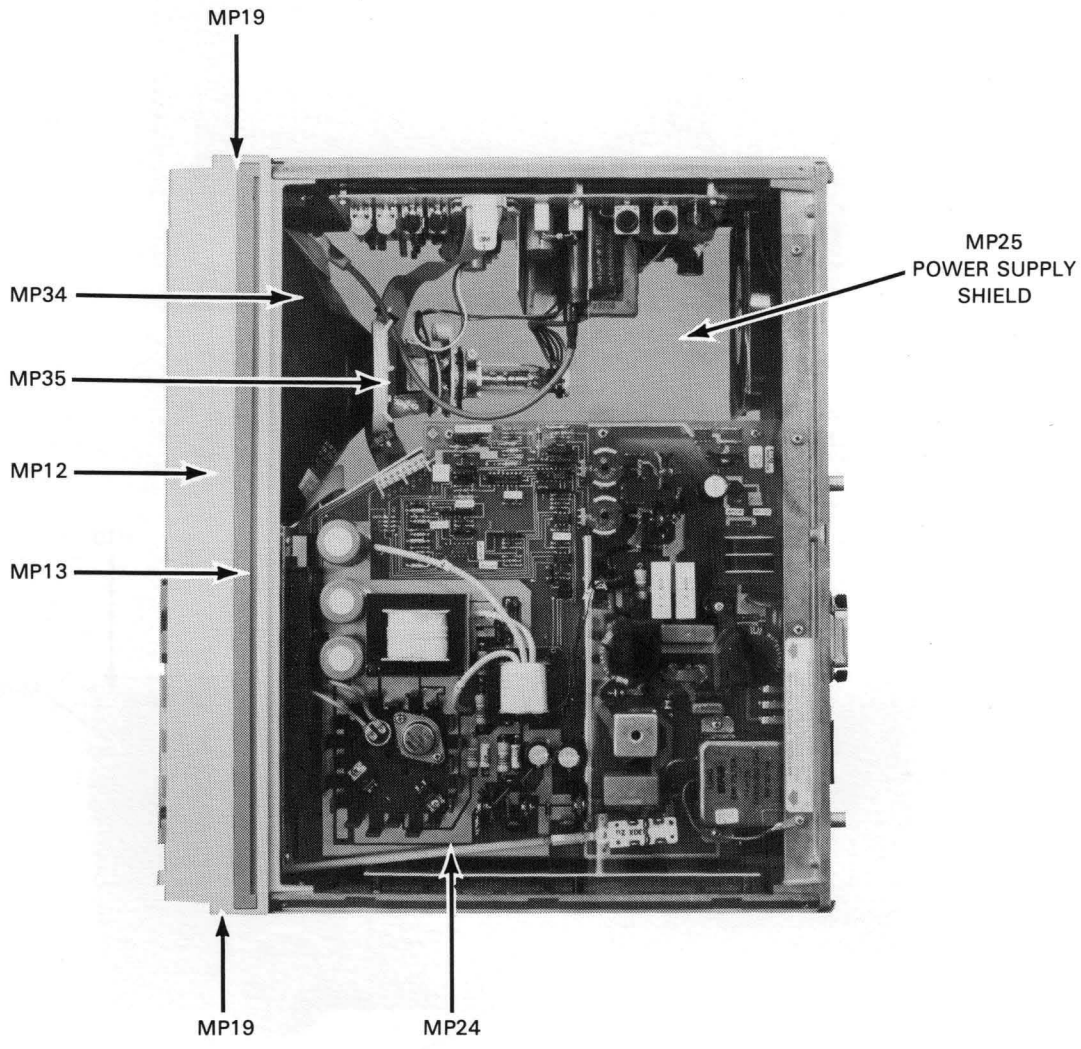


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 3 of 4)

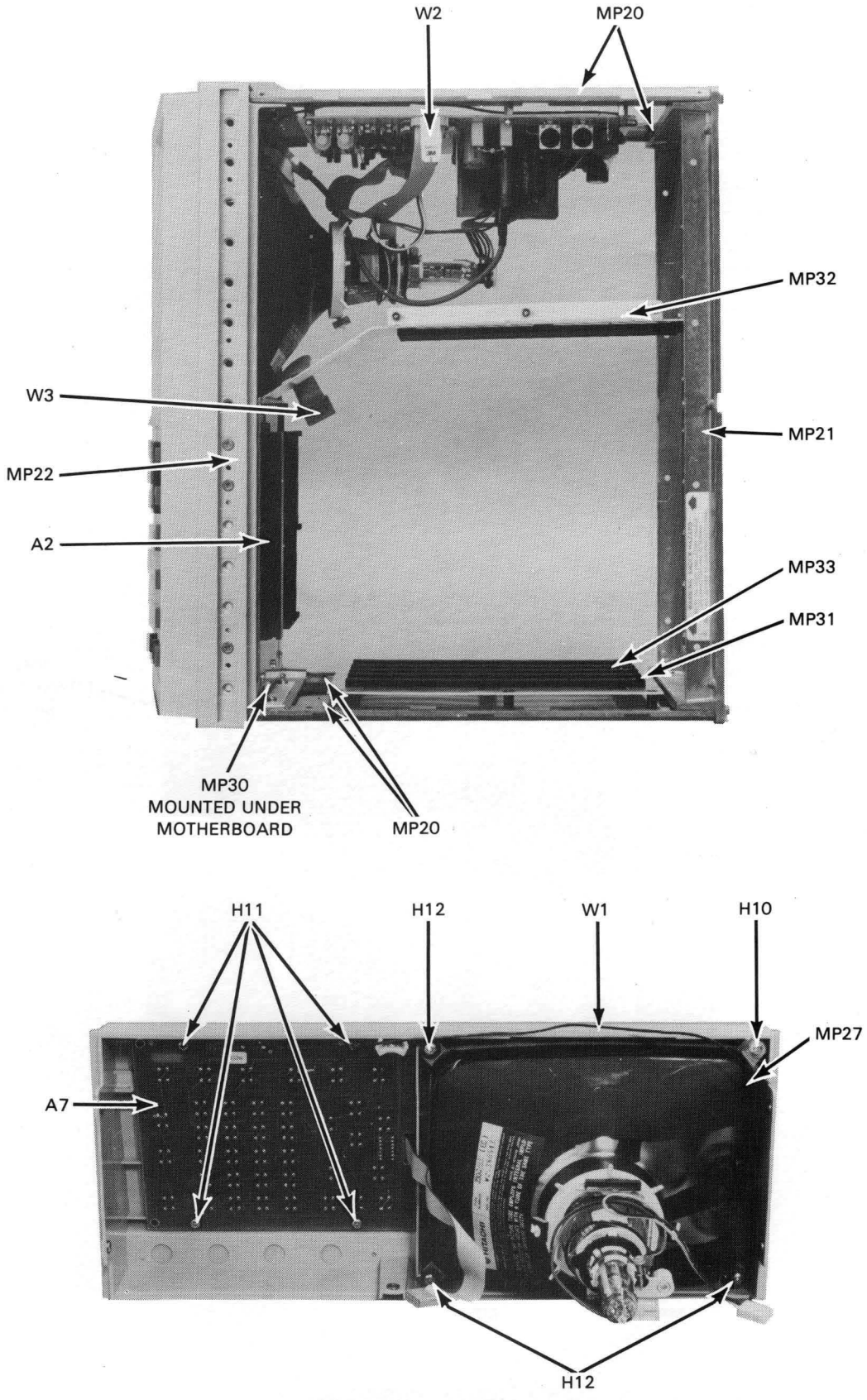


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 4 of 4)

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	1630A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2242A (1630A) 2234A (1630D) ARE THE SAME AS FOR PREFIX 2412A WITH THE FOLLOWING EXCEPTIONS		
A1	01630-66502	5	1	POWER SUPPLY BOARD	28480	01630-66502
A3	01630-66503	6	1	CPU BOARD (1630A AND 1630D)	28480	01630-66503
A4	01630-66505	8	1	STATE MASTER BOARD	28480	01630-66505
A5	01630-66506	9	1	TIMING MASTER BOARD	28480	01630-66506
B1	3160-0252	7	1	FAN 128V 50/60-HZ	28480	3160-0252
MP1	01630-00201	3	1	PANEL-REAR	28480	01630-00201
MP2	01630-04102	1	1	COVER PROBE CONNECTOR	28480	01630-04102
MP3	01630-44101	4	1	COVER CARD CAGE	28480	01630-44101
MP4	01630-04101	0	1	TOP COVER	28480	01630-04101
MP5	1540-0807	2	1	POUCH	28480	1540-0807
W5	01630-61603	7	1	CABLE-FAN	28480	01630-61603
	1630A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2311A (1630A/D) ARE THE SAME AS FOR PREFIX 2412A WITH THE FOLLOWING EXCEPTIONS		
A1	01630-66502	5	1	POWER SUPPLY BOARD	28480	01630-66502
A3	01630-66503	6	1	CPU BOARD (1630A AND 1630D)	28480	01630-66503
A4	01630-66509	2	1	STATE MASTER BOARD	28480	01630-66509
B1	3160-0252	7	1	FAN 128V 50/60-HZ	28480	3160-0252
MP1	01630-00201	3	1	PANEL-REAR	28480	01630-00201
MP2	01630-04102	1	1	COVER PROBE CONNECTOR	28480	01630-04102
MP3	01630-44101	4	1	COVER CARD CAGE	28480	01630-44101
MP4	01630-04101	0	1	TOP COVER	28480	01630-04101
MP5	1540-0807	2	1	POUCH	28480	1540-0807
W5	01630-61603	7	1	CABLE-FAN	28480	01630-61603
	1630A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL NUMBERS: 2311A00231 (1630A) 2311A00791 (1630D) TO SERIAL PREFIX 2412A (1630A/D) ARE THE SAME AS FOR PREFIX 2412A WITH THE FOLLOWING EXCEPTIONS		
A1	01630-66502	5	1	POWER SUPPLY BOARD	28480	01630-66502
A3	01630-66512	7	1	CPU BOARD (1630A AND 1630D)	28480	01630-66512
A4	01630-66509	2	1	STATE MASTER BOARD	28480	01630-66509
B1	3160-0252	7	1	FAN 128V 50/60-HZ	28480	3160-0252
MP1	01630-00201	3	1	PANEL-REAR	28480	01630-00201
MP2	01630-04102	1	1	COVER PROBE CONNECTOR	28480	01630-04102
MP3	01630-44101	4	1	COVER CARD CAGE	28480	01630-44101
MP4	01630-04101	0	1	TOP COVER	28480	01630-04101
MP5	1540-0807	2	1	POUCH	28480	1540-0807
W5	01630-61603	7	1	CABLE-FAN	28480	01630-61603
	1630A/D/G			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2412A (1630A/D) 2415A (1630G)		
A1	01630-66514	9	1	POWER SUPPLY BOARD	28480	01630-66514
A2	01630-66501	4	1	MOTHER BOARD	28480	01630-66501
A3	01630-66522	9	1	CPU BOARD (1630A AND 1630D)	28480	01630-66522
A3	01630-66519	7	1	CPU BOARD (1630G)	28480	01630-66519
A4	01630-66518	3	1	STATE MASTER BOARD	28480	01630-66518

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	01630-66510	5	1	TIMING MASTER BOARD (1630A/D)	28480	01630-66510
A5	01630-66524	7	1	TIMING MASTER BOARD (1630G)	28480	01630-66524
A6	0950-0894	5	1	DISPLAY BOARD ASSEMBLY	28480	0950-0894
A7	01630-66504	7	1	KEYBOARD	28480	01630-66504
A8	01630-66508	1	1	TIMING SLAVE BOARD (1630D ONLY)	28480	01630-66508
A9	10271A	6	3	STATE MASTER PROBE	28480	10271A
A10	10272A	7	AR	TIMING PROBE(1630A/G QTY 1, 1630D QTY 2)	28480	10272A
A11	01630-66517	2	1	STATE SLAVE BOARD (1630G ONLY)	28480	01630-66517
A12	10273A	8	3	STATE SLAVE PROBE (1630G ONLY)	28480	10273A
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
H1	0515-0211	8	29	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H2	0515-0396	0	13	SCREW-MACH M4 X 0.7 10MM-LG	00000	ORDER BY DESCRIPTION
H3	0515-0406	3	4	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H4	0515-0413	2	8	SCREW-MACH M4 X 0.7 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H5	0624-0400	8	4	SCREW-TPG 6-19 .5-IN-LG PAN-HD-POZI STL	00000	ORDER BY DESCRIPTION
H6	2360-0125	6	4	SCREW-MACH 6-32 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H7	2360-0195	0	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H8	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H9	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H10	3050-0002	2	1	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0002
H11	3050-0003	3	4	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H12	3050-0006	6	3	WASHER-SHLDR NO. 10 .5-IN-OD	28480	3050-0006
H13	0624-0441	7	4	SCREW-TPG 8-16 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
L1	9140-0720	8	1	YOKE	28480	9140-0720
MP1	01630-00202	4	1	PANEL-REAR	28480	01630-00202
MP2	01630-64103	8	1	COVER PROBE CONNECTOR	28480	01630-64103
MP3	01630-44102	5	1	COVER CARD CAGE	28480	01630-44102
MP4	01630-04104	3	1	TOP COVER	28480	01630-04104
MP5	01630-84501	2	1	POUCH	28480	01630-84501
MP6	5060-9845	2	1	BOTTOM COVER	28480	5060-9845
MP7	5060-9882	7	1	COVER-SIDE	28480	5060-9882
MP8	5060-9802	1	1	STRAP HANDLE 12 INCH	28480	5060-9802
MP9	5040-7219	8	1	CAP-STRAP HANDLE (FRONT)	28480	5040-7219
MP10	5040-7220	1	1	CAP-STRAP HANDLE (REAR)	28480	5040-7220
MP11	5060-9915	7	1	COVER-SIDE PERFORATED	28480	5060-9915
MP12	7101-0694	1	1	BEZEL-FRONT	28480	7101-0694
MP13	5040-7202	9	1	TRIM STRIP-TOP	28480	5040-7202
MP14	5040-7201	8	4	FEET	28480	5040-7201
MP15	1460-1345	5	2	TILT STAND	28480	1460-1345
MP16	3160-0092	3	1	FINGER GUARD	28480	3160-0092
MP17				NOT USED		
MP18	2420-0001	5	4	FASTENING NUT-HEX (FAN)	28480	2420-0001
MP19	5001-0440	1	2	TRIM-SIDE	28480	5001-0440
MP20	5020-8835	4	4	STRUT-CORNER	28480	5020-8835
MP21	5020-8806	9	1	FRAME-REAR	28480	5020-8806
MP22	5020-8805	8	1	FRAME-FRONT	28480	5020-8805
MP23	5040-7221	2	4	STANDOFF R PANEL	28480	5040-7221
MP24	5041-3170	4	1	SWITCH SHAFT	28480	5041-3170
MP25	01630-00601	7	1	SHIELD-POWER SUPPLY-PLASTIC	28480	01630-00601
MP26	5041-2799	1	1	KEYCAP-LINE	28480	5041-2799
MP27	0360-2109	8	1	GROUND LUG	28480	0360-2109
MP28	0363-0040	8	8	RFI STRIP-FINGERS BE-CU ZINC PLATED	28480	0363-0040
MP29	0403-0179	0	3	BUMPER FOOT-ADHESIVE MOUNTING	28480	0403-0179
MP30	01630-01201	5	1	BRACKET MOTHER BOARD	28480	01630-01201
MP31	01630-01202	6	1	BRACKET CARD GUIDE	28480	01630-01202
MP32	01630-01203	7	1	BRACKET CENTER GUIDE	28480	01630-01203
MP33	0403-0445	3	10	PC CARD GUIDE	28480	0403-0445
MP34	7121-3936	2	1	LABEL-IDENTIFICATION (1630A ONLY)	28480	7121-3936
MP34	7121-3934	0	1	LABEL-IDENTIFICATION (1630D ONLY)	28480	7121-3934
MP34	01630-94306	5	1	LABEL-IDENTIFICATION (1630G ONLY)	28480	01630-94306
MP35	7121-3935	1	1	LABEL-BLANK	28480	7121-3935
V1	2090-0066	1	1	TUBE-CRT	28480	2090-0066
W1	8120-1521	6	1	POWER CORD 115V USA/CANADA	28480	8120-1521
W1	8120-1703	6	1	POWER CORD OPTION 900 UNITED KINGDOM	28480	8120-1703
W1	8120-0696	4	1	POWER CORD OPTION 901 AUST/NEW ZEALAND	28480	8120-0696
W1	8120-1692	2	1	POWER CORD OPTION 902 EUROPEAN CONTINENT	28480	8120-1692
W1	8120-2296	4	1	POWER CORD OPTION 906 SWITZERLAND	28480	8120-2296
W1	8120-2957	4	1	POWER CORD OPTION 912 DENMARK	28480	8120-2957
W2	8120-3785	8	1	CABLE DISPLAY-16	28480	8120-3785
W3	8120-3784	7	1	CABLE KEYBD-14	28480	8120-3784
W4	82167-60002		1	CABLE HP-IL INTERFACE	28480	82167-60002

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01630-66502	5	1	POWER SUPPLY ASSEMBLY SAME AS 01630-66514 WITH THE FOLLOWING EXCEPTIONS: CHANGE P2 QTY TO 2 DELETE TP3	28480	01630-66502
A1	01630-66514	9	1	POWER SUPPLY ASSEMBLY	28480	01630-66514
A1C1	0180-0291	3	14	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C2	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C3	0180-2946	9	3	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1C4	0160-5473	1	10	CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C5	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C6	0160-5347	8	3	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C7	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C8	0140-0180	5	7	CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C9	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C10	0180-3224	8	2	CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C11	0180-3224	8		CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C12	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1C13	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
A1C14	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C15	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C16	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C17	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C18	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C19	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A1C20	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C21	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C22	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C23	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C24	0160-0164	7	3	CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C25	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C26	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C27	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C28	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C29	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C30	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C31	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C32	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C33	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C34	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 3000VDC MICA	72136	DM19F202G0300WV1CR
A1C35	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C36	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C37	0160-2202	8	1	CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A1C38	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C39	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C40	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C41	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C42	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C43	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C44	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C45	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C46	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C47	0180-3046	2	3	CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C48	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C49	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1CR1	1906-0006	9	1	DIODE-FW BRDG 400V 1A	18546	VE48
A1CR2	1901-0719	1	2	DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A1CR3	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A1CR4	1906-0224	3	1	DIODE-FW BRDG 600V 25A	04713	MDA2506
A1CR5	1901-0028	5	1	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1CR6	1901-0050	3	10	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR10	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A1CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR15	1906-0079	6	1	DIODE-FW BRDG 100V 10A	18546	VJ148X
A1CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR18	1906-0239	0	1	DIODE-CT-RECT 45V 30A	01281	SD-241

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1CR19	1906-0263	0	1	RECT VSK 12	28480	1906-0263
A1CR20	1906-0262	9	1	RECT USE 2402	28480	1906-0262
A1DS1	1990-0652	8	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
A1E1				SEE SERVICE NOTE-APPENDIX E		
A1E2				SEE SERVICE NOTE-APPENDIX E		
A1E3	2110-0642	3	1	FUSEHOLDER	28480	2110-0642
A1F1	2110-0056	3	1	FUSE 6A 250V NTD 1.25X.25 UL IEC	75915	312006
A1FL1	9135-0175	6	1	FILTER-LINE	28480	9135-0175
A1H1	01830-23201	3	1	COUPLER-SW EXTN	28480	01830-23201
A1H2	0403-0285	9	1	BMPR FT-ADH MTG	28480	0403-0285
A1H3	0515-0211	8	8	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H4	0515-0412	1	1	SCREW-MACH M3 X 0.5 25MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H5	0515-0406	3	4	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H6	2190-0005	0	12	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A1H7	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A1H8	3050-0003	3	1	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
A1L1	9140-0624	1	1	INDUCTOR 270UH 10% .725DX.818LG	28480	9140-0624
A1L2	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192
A1MP1	1205-0490	9	4	HEAT SINK 6022BS	28480	1205-0490
A1MP2	2110-0565	9	1	FUSEHOLDER CAP 12A MAX FOR UL	28480	2110-0565
A1MP3	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP4	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP5	1600-1330	6	1	STIFFENER-PCB	28480	1600-1330
A1MP6	1205-0489	6	2	HEAT SINK 6021BS	28480	1205-0489
A1MP7	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP8	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP9	1205-0486	3	1	HEAT SINK	28480	1205-0486
A1Q1	1854-0827	1	2	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1Q2	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1P1	1251-7864	2	1	CONNECTOR-50 CONTACT (MALE)	28480	1251-7864
A1P2	1251-7826	6	3	CONNECTOR-MALE	28480	1251-7826
A1R1	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R2	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R3	0698-3615	8	1	RESISTOR 47 5% 2W MO TC=0+-200	27167	FP42-2-TOO-47R0-J
A1R4	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R5	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R6	0757-0059	4	1	RESISTOR 1M 1% .5W F TC=0+-100	28480	0757-0059
A1R7	0757-0409	8	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R8	0757-0415	6	2	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R9	0757-0409	8		RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R10	0757-0415	6		RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R11	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R14	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R15	0757-0397	3	1	RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-6BR1-F
A1R16	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1R17	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R19	0698-8959	3	1	RESISTOR 619K 1% .125W F TC=0+-100	28480	0698-8959
A1R20	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R21	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2741-F
A1R22	0757-0441	8	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-TO-8251-F
A1R23	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R24	0757-0795	5	1	RESISTOR 75 1% .5W F TC=0+-100	19701	MF-1/2-TO-75R0-F
A1R25	0698-3603	4	3	RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R26	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R27	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R29	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-9091-F
A1R30	0757-0468	9	2	RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1303-F
A1R31	0757-0450	9	1	RESISTOR 22.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2212-F
A1R32	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R34	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R35	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A1R36	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A1R37	0757-0459	8	2	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R39	0757-0459	8		RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1R40	0757-0468	9		RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1303-F
A1R41	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R42	0757-0479	2	1	RESISTOR 392K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-3923-F
A1RP1	1810-0488	8	3	NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP2	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP3	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RT1				SEE SERVICE NOTE-APPENDIX E		
A1RT2				SEE SERVICE NOTE-APPENDIX E		
A1RT3	0837-0172	2	1	THERMISTOR DISC 2.5-OHM	15454	SG-3
A1RV1	0837-0120	0	1	VARISTOR-130VAC	28480	0837-0120
A1RV2	0837-0261	0	1	VARISTOR-220VAC	28480	0837-0261
A1SW1	3101-2582	6	1	SWITCH-SLIDE	28480	3101-2582
A1SW2	3101-2150	4	1	SWITCH-PB DPDT ALTNG 5A 250VAC	28480	3101-2150
A1SW3	3103-0091	2	1	SWITCH-THRM FXD +110C 6A OPN-ON-RISE	28480	3103-0091
A1T1	9100-4271	8	1	TRANSFORMER-CONT	28480	9100-4271
A1T2	9100-4265	0	2	TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T3	9100-4265	0		TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T4	9100-4163	7	1	TRANSFORMER	28480	9100-4163
A1T5	9100-4266	1	1	TRANSFORMER-POWER	28480	9100-4266
A1T6	9100-4267	2	1	CHOKE-COUPLED	28480	9100-4267
A1TP1	1251-3618	6	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-3618
A1TP2	1251-3900	9	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3900
A1TP3	1251-7826	6		CONNECTOR-MALE	28480	1251-7826
A1U1	1826-0718	0	1	IC-MC1404	28480	1826-0718
A1U2	1820-2111	9	1	IC DRVR TTL INV	01295	SN75468N
A1U3	1826-0468	7	2	IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U4	1826-0468	7		IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U5	1826-0565	5	1	IC-TL494	28480	1826-0565
A1U6	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MLM324P
A1VR1	1826-0147	9	2	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR2	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
A1VR3	1826-0147	9		IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR4	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	01630-66501	4	1	MOTHERBOARD ASSEMBLY	28480	01630-66501
A2C1	0160-5298	8	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2J1	1251-7867	5	1	CONNECTOR-100 CONTACT (MALE)	28480	1251-7867
A2J2	1251-7865	3	2	CONNECTOR-50 CONTACT (MALE)	28480	1251-7865
A2J3	1251-7866	4	4	CONNECTOR-100 CONTACT (MALE)	28480	1251-7866
A2J4	1251-7866	4		CONNECTOR-100 CONTACT (MALE)	28480	1251-7866
A2J5	1251-7866	4		CONNECTOR-100 CONTACT (MALE)	28480	1251-7866
A2J6	1251-7866	4		CONNECTOR-100 CONTACT (MALE)	28480	1251-7866
A2RP1	1810-0619	7	4	RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP2	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP3	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP4	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	01630-66503	6	1	CPU ASSEMBLY SAME AS 01630-66522	28480	01630-66503
A3	01630-66512	7	1	CPU ASSEMBLY SAME AS 01630-66522 EXCEPT: CHANGE A3XU6I QTY TO 1 DELETE A3XU6M	28480	01630-66512
A3	01630-66519	7	1	CPU ASSEMBLY (1630G ONLY) SAME AS 01630-66522 EXCEPT:	28480	01630-66519
A3U3H	01630-80027	9	1	PROM 3 27128-3	28480	01630-80027
A3U3I	01630-80026	8	1	PROM 2 27128-3	28480	01630-80026
A3U3J	01630-80025	7	1	PROM 1 27128-3	28480	01630-80025
A3U3K	01630-80024	6	1	PROM 0 27128-3	28480	01630-80024
A3U4H	01630-80031	5	1	PROM 7 27128-3	28480	01630-80031
A3U4I	01630-80030	4	1	PROM 6 27128-3	28480	01630-80030
A3U4J	01630-80029	1	1	PROM 5 27128-3	28480	01630-80029
A3U4K	01630-80028	0	1	PROM 4 27128-3	28480	01630-80028
A3	01630-66522	9	1	CPU ASSEMBLY	28480	01630-66522
A3C1	0160-5311	6	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-5311
A3C2	0160-5311	6		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-5311
A3C3	0160-5298	8	40	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C5	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C7	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C9	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C12	0160-5474	2	6	CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C13	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C26	0160-3508	9	7	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C27	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C28	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C29	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C34	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C36	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C37	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C38	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C39	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C40	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C41	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C43	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C44	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C45	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C46	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C47	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C48	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C49	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C50	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3C51	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C52	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C53	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A3C54	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C55	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C56				NOT USED		
A3C57	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C58	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C59	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C60	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C61	0180-0228	6	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3C62	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3CR1	1902-0186	8	4	DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR2	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR3	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR4	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3H1	0515-0211	8	4	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A3H2	0624-0306	3	2	SCREW-TPG 2-28 .5-IN-LG PAN-HD-POZI STL	28480	0624-0306
A3H3	01630-01208	2	1	GROUND BRACKET	28480	01630-01208
A3J1	1250-1774	9	2	CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM	28480	1250-1774
A3J2	1251-7162	3	1	CONNECTOR 24-PIN F MICRO-RIBBON	28480	1251-7162
A3J3	82169-60007	3	1	CONNECTOR HP-IL	28480	82169-60007
A3J4	1250-1774	9		CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM	28480	1250-1774
A3J5	1251-7666	2	1	CONNECTOR-16 PIN	28480	1251-7666
A3J6	1251-7664	0	1	CONNECTOR-14 PIN	28480	1251-7664
A3LS1	9164-0209	8	1	AUDIO TRANSDUCER	28480	9164-0209
A3MP1	01630-01204	8	1	BRACKET - HP-IL	28480	01630-01204
A3MP2	1251-5595	2	2	POLARIZING KEY-POST CONN	28480	1251-5595
A3MP3	1251-5595	2		POLARIZING KEY-POST CONN	28480	1251-5595
A3P1	1251-7868	6	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-7868
A3R1	0757-0283	6	8	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R2	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R3	0757-0446	3	2	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1502-F
A3R4	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-TO-383R-F
A3R5	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-TO-383R-F
A3R6	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1502-F
A3R7	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R8	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R9	0698-4002	9	5	RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R10	0757-0389	3	3	RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-TO-33R2-F
A3R11	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R12	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R13	0757-0389	3		RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-TO-33R2-F
A3R14	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R15	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A3R16	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A3R18	0757-0480	5	1	RESISTOR 432K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-4323-F
A3R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3R20	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A3R21	0757-0451	0	1	RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2432-F
A3R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3R23	0698-4439	6	1	RESISTOR 3.24K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3241-F
A3R24	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R25	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R26	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1102-F
A3R27	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A3R28	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R29	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3R31	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R32	0699-1000	3	2	RESISTOR-FXD 4.25K OHM .1%	28480	0699-1000
A3R33	0699-1000	3		RESISTOR-FXD 4.25K OHM .1%	28480	0699-1000
A3R34	0757-0389	3		RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-TO-33R2-F
A3R35	0698-6360	6	2	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A3R36	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A3R37	2100-2655	1	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A3RP1	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3RP2	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
A3RP3	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3RP4	1810-0382	1	2	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A3RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A3RP6	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A3SW1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
A3TP	1251-5395	0	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-5395
A3U1E	1820-2024	3	8	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U1H	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
A3U1I	1820-2547	5	1	IC RCVR TTL LS OCTL	01295	SN75162N
A3U1J	1820-1198	0	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A3U1K	1820-1198	0		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A3U1L	1820-1730	6	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U1M	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U2A	1820-2701	3	2	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
A3U2B	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A3U2C	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U2D	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U2E	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A3U2G	1820-2548	6	1	IC-TMS 9914	28480	1820-2548
A3U3A	1818-3005	7	8	IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3005
A3U3B	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3005
A3U3C	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3005
A3U3D	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3005
A3U3E	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U3F	1820-2096	9	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U3H	01630-80011	1	1	PROM 3 D2764-3	28480	01630-80011
A3U3I	01630-80010	0	1	PROM 2 D2764-3	28480	01630-80010
A3U3J	01630-80009	7	1	PROM 1 D2764-3	28480	01630-80009
A3U3K	01630-80008	6	1	PROM 0 D2764-3	28480	01630-80008
A3U3N	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U3O	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U3P	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U4A	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3005
A3U4B	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3005
A3U4C	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3005
A3U4D	1818-3005	7		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3005
A3U4F	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U4G	1820-1278	7	1	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
A3U4H	01630-80015	5	1	PROM 7 D2764-3	28480	01630-80015
A3U4I	01630-80014	4	1	PROM 6 D2764-3	28480	01630-80014
A3U4J	01630-80013	3	1	PROM 5 D2764-3	28480	01630-80013
A3U4K	01630-80012	2	1	PROM 4 D2764-3	28480	01630-80012
A3U4N	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U4O	1820-1238	9	3	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U4P	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U4Q	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U5A	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5B	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
A3U5C	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U5E	1820-1439	2	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A3U5F	1820-1309	5	4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U5G	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U5J	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U5N	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U5O	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5P	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5Q	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U6A	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U6B	1820-1457	4	1	IC SHF-RGTR TTL S D-TYPE PRL-IN PRL-OUT	01295	SN74S299N
A3U6C	1818-3074	0	1	IC MEMORY ROM	28480	1818-3074
A3U6D	1820-2853	6	1	IC-MC68A45L	28480	1820-2853
A3U6E	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A3U6F	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U6G	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U6I	1820-2854	7	1	IC-MPU MC68B09EL	28480	1820-2854
A3U6J	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A3U6L	1820-2911	7	1	IC-MMU MC68829L	28480	1820-2911
A3U6M	1820-2604	5	1	IC NMOS 16-BIT	34335	AM9513CC
A3U6N	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U6O	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U6P	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U7A	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U7B	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A3U7C	1820-1191	3	3	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U7D	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
A3U7F	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U7G	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U7H	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A3U7I	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U7K	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U7L	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U7M	1820-1173	1	5	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A3U7N	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U7O	1826-0609	8	1	IC MULTIPLXR ANLG 16-DIP-C PKG	06665	MUX08FQ
A3U7P	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A3U8C	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U8D	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U8F	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U8G	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U8H	1820-1287	8	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS37N
A3U8I	1820-0697	2	1	IC DRVR TTL S NAND LINE DUAL 4-INP	01295	SN74S140N
A3U8J	1820-1052	5	3	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A3U8K	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A3U8L	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A3U8O	1826-0753	3	2	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A3U8Q	1826-0753	3		IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A3U9D	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U9E	1820-2150	6	1	IC MICPROC-ACCESS NMOS	34649	D8279-5
A3U9F	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U9G	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U9H	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
A3U9I	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A3U9J	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A3U9K	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A3U9L	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A3U9M	1820-1990	0	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A3U9N	1826-0856	7	1	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A3U10O	1826-0718	0	1	IC-MC1404	28480	1826-0718
A3UR4E	1810-0301	4	1	NETWORK-RES 16-DIP51.0 OHM X 8	01121	316B510
A3UR9O	1810-0613	1	5	RESISTIVE NETWORK	28480	1810-0613
A3UR9P	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR9Q	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR10P	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR10Q	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UT1	9100-4226	3	1	TRANSFORMER	28480	9100-4226
A3UY1D	1813-0275	7	1	OSCILLATOR-40 MHZ	28480	1813-0275
A3UY6Q	1813-0174	5	1	OSCILLATOR-4.00 MHZ	28480	1813-0174
A3XU3H	1200-0567	1	8	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3I	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3J	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3K	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4H	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4I	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4J	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4K	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU6I	1200-0654	7	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU6M	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XUY1D	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3A1	01630-66513	8	1	ESD ASSEMBLY	28480	01630-66513
A3A1C1	0160-5246	6	1	CAPACITOR-FXD .1UF 50VDC	28480	0160-5246
A3A1CR1	1901-0050	3	4	DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1R1	0683-4705	8	1	RESISTOR-FXD 47 OHM .25W CC	28480	0683-4705
A3U2O	1LB3-0003	8	1	IC HP-IL	28480	1LB3-0003
A3A1XU1	1200-0567	1	1	SOCKET-IC 28-PIN	28480	1200-0567

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	01630-66505	8	1	STATE ACQ. ASSEMBLY	28480	01630-66505
				SAME AS 01630-66518 WITH THE FOLLOWING EXCEPTIONS:		
A4U2B	1820-1788	4	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2C	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2E	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2F	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2G	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2H	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2I	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U4L	1820-2451	0	1	IC LCH ECL D-TYPE NEG-EDGE-TRIG COM	04713	MC10168P
A4	01630-66509	2	1	STATE ACQ. ASSEMBLY	28480	01630-66509
				SAME AS 01630-66518 WITH THE FOLLOWING EXCEPTIONS:		
A4U2B	1820-1788	4	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2C	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2E	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2F	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2G	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2H	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2I	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4	01630-66518	3	1	STATE ACQ. ASSEMBLY	28480	01630-66518
A4C1	0160-5298	8	70	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C5	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C7	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C9	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C12	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C13	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C18	0160-5309	2	7	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C26	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C27	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C28	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C29	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C34	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C36	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C37	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C38	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C39	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C40	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C41	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C43	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C44	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C45	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C46	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C47	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C48	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C49	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C50	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C51	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C52	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C53	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C54	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C55	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C56	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C57	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C58	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C59	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C60	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C61	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C62	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C63	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C64	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C65	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C66	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C67	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C68	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C69	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C70	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C71	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C72	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C73	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C74	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C75	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C76	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C77	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4C78	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C79	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A4DL1	1810-0602	8	1	DELAY LINE- 7NS	28480	1810-0602
A4J1	1251-7705	0	3	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4J2	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4J3	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4P1	1251-7868	6	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-7868
A4R1	0757-0418	9	6	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R2	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R3	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R4	2100-3123	0	2	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A4R5	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A4R6	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R7	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A4R8	0698-3441	8	2	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A4R9	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R10	0757-0408	7	2	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-TO-243R-F
A4R11	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24946	C4-1/8-TO-215R-F
A4R12	0757-0408	7		RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-TO-243R-F
A4R13	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R16	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4RP1	1810-0272	8	6	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP2	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP3	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP4	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP5	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP6	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP7	1810-0382	1	28	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP10	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP14	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP16	1810-0219	3	1	NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A4RP17	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP18	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP19	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP20	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP21	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP22	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP23	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP24	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP25	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP26	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP27	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP28	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP29	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP30	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP31	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP32	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP33	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP34	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP35	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RT1	0037-0046	9	2	THERMISTOR DISC 2K-OHM	28480	0037-0046
A4RT2	0037-0046	9		THERMISTOR DISC 2K-OHM	28480	0037-0046
A4TP1	1250-1737	4	2	COAXIAL TEST POINT	28480	1250-1737
A4TP2	1250-1737	4		COAXIAL TEST POINT	28480	1250-1737
A4U1A	1820-2848	9	11	IC-MC10H131P	28480	1820-2848
A4U1B	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1C	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1D	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1E	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1F	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1H	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1I	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1J	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U1K	1820-1944	4	1	IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
A4U1L	1820-0802	1	5	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U1M	1820-2450	9	1	IC INV ECL HEX	04713	MC10189P
A4U1N	1820-0827	0	1	IC DCDR ECL BIN 3-TO-8-LINE	04713	MC10161P
A4U2B	1820-3102	0	18	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2C	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2D	1820-1225	0	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A4U2E	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2F	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2G	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2H	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2I	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016
A4U2J	1820-0817	8	4	IC FF ECL D-M/S DUAL	04713	MC10131P
A4U2K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U2L	1820-1831	8	2	IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A4U2M	1820-0806	5	3	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U3A	1816-1591	8	7	IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3B	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3C	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3E	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3F	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3G	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3I	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3J	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U3K	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U3L	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U3M	1820-0809	8	1	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A4U3N	1820-2193	7	3	IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A4U4K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U4L	1820-2959	3	2	IC-MC10H158P	28480	1820-2959
A4U4M	1820-2860	5	1	IC-MC10H130P	28480	1820-2860
A4U5A	1820-1359	5	4	IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5B	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5C	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5D	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5E	1816-1555	4	1	IC-RAM 10422-6	28480	1816-1555

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U5F	1816-1544	1	3	IC-RAM 10422	28480	1816-1544
A4U5G	1816-1544	1		IC-RAM 10422	28480	1816-1544
A4U5I	1816-1544	1		IC-RAM 10422	28480	1816-1544
A4U5K	1820-2822	9	1	IC-MC10H105P	28480	1820-2822
A4U5L	1820-2849	0	8	IC-MC10H131P	28480	1820-2849
A4U5M	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U5N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U6A	1820-3128	0	5	IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U6B	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U6C	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U6D	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U6E	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U6F	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A4U6G	1820-0804	3	1	IC GATE ECL NOR TPL	04713	MC10106P
A4U6H	1816-1554	3	1	IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10H145
A4U6I	1820-2962	8	1	IC-MC10H103P	28480	1820-2962
A4U6J	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U6K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U6L	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A4U6M	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A4U6N	1820-2848	9		IC-MC10H131P	28480	1820-2848
A4U7B	1820-2823	0	1	IC-MC10H102	28480	1820-2823
A4U7C	1820-1831	8		IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A4U7D	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U7E	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U7F	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U7G	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U7H	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A4U7I	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U7J	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U7K	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U7L	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U7M	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U7N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8C	1820-2451	0	1	IC LCH ECL D-TYPE NEG-EDGE-TRIG COM	04713	MC10168P
A4U8D	1820-1400	7	1	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U8E	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8F	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8G	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8H	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8I	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U8J	1820-2891	2	1	IC-MC10H101P	28480	1820-2891
A4U8K	1820-2963	9	1	IC-MC10H210	28480	1820-2963
A4U8L	1820-2959	3		IC-MC10H158P	28480	1820-2959
A4U8M	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8O	1820-2849	0		IC-MC10H131P	28480	1820-2849

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	01630-66506	9	1	TIMING MASTER ASSEMBLY	28480	01630-66506
				USES THE SAME PARTS AS 01630-66524 WITH THE FOLLOWING EXCEPTIONS:		
				DELETE;		
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
				CHANGE;		
A5C25	0160-3879	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
				ADD;		
A5C26	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A5C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C29	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5L1	9100-2248	5	1	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A5L2	9100-2252	1	1	INDUCTOR RF-CH-MLD 270NH 10% .105DX.26LG	28480	9100-2252
A5L3	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5Q1	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A5R7	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A5R8	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A5R10	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A5R11	0698-4426	1		RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5Y1	0410-1335	7	1	CRYSTAL-QUARTZ 200 MHZ HC-18/U-HLDR	28480	0410-1335
A5	01630-66510	5	1	TIMING MASTER ASSEMBLY USES THE SAME PARTS AS 01630-66524 WITH THE FOLLOWING EXCEPTIONS:	28480	01630-66510
				DELETE;		
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
				CHANGE;		
A5C25	0160-3879	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
				ADD;		
A5C26	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A5C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C29	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5L1	9100-2248	5	1	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A5L2	9100-2252	1	1	INDUCTOR RF-CH-MLD 270NH 10% .105DX.26LG	28480	9100-2252
A5L3	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5Q1	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A5R7	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A5R8	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A5R10	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A5R11	0698-4426	1		RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5Y1	0410-1335	7	1	CRYSTAL-QUARTZ 200 MHZ HC-18/U-HLDR	28480	0410-1335
A5	01630-66524	7	1	TIMING MASTER ASSEMBLY	28480	01630-66524
A5C1	0160-5298	8	51	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C4	0160-5341	2	1	CAPACITOR-FXD 4UF 50VDC	28480	0160-5341
A5C5	0160-5342	3	1	CAPACITOR-FXD .4UF 50VDC	28480	0160-5342
A5C6	0160-5475	3	1	CAPACITOR-FXD PC .04UF 50VDC	28480	0160-5475
A5C7	0160-5415	1	1	CAPACITOR-FXD 3600PF 50VDC	28480	0160-5415
A5C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C9	0160-5506	1	3	CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C12	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C13	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C15	0160-5506	1		CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C26				NOT USED		
A5C27				NOT USED		
A5C28	0160-3874	2	2	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C29				NOT USED		
A5C30				NOT USED		
A5C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C34	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C36	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C37	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C38	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C39	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C40	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C41	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C43	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C44	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C45	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C46	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C47	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C48	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C49	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C50	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C51	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C52	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C53	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C54	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C55	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C56	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C57	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C58	0160-5506	1		CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C59	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C60	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C61	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C62	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C63	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C64	0180-0229	7	2	CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A5C65	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A5C66	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5C67	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5321
A5J1	1251-7705	0	1	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A5MP1	1205-0484	1	2	HEAT SINK SOCKET	28480	1205-0484
A5P1	1251-7868	6	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-7868
A5R1	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-TO-681R-F
A5R2	0698-6735	9	1	RESISTOR 1.71K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1711-F
A5R3	0698-4426	1	1	RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5R4	0757-0407	6	2	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-TO-201-F
A5R5	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-TO-201-F
A5R6	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R7				NOT USED		
A5R8				NOT USED		
A5R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R10				NOT USED		

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R11				NOT USED		
A5R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5RP1	1810-0382	1	24	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP2	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP3	1810-0270	6	1	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
A5RP4	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP6	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A5RP7	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP10	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP14	1810-0350	3	2	NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A5RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP16	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP17	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP18	1810-0350	3		NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A5RP19	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP20	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP21	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP22	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP23	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP24	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP25	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP26	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP27	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP28	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5TP1	1250-1737	4	1	COAXIAL TEST POINT	28480	1250-1737
A5U1J	1820-1831	8	1	IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A5U1K	1820-3102	0	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U1L	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U2A	1858-0058	8	2	TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	MPQ3906
A5U2D	1820-0810	1	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A5U2G	1820-0825	8	1	IC SHF-RGTR ECL D-TYPE PRL-IN PRL-OUT	04713	MC10141L
A5U2H	1820-1225	4	3	IC FF ECL D-M/S DUAL	04713	MC10231P
A5U2I	1820-0820	3	3	IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A5U2J	1820-0806	5	2	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A5U2K	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U2L	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U3A	1858-0021	5	2	TRANSISTOR ARRAY 16-PIN PLSTC	3L585	CA3083
A5U3B	1858-0021	5		TRANSISTOR ARRAY 16-PIN PLSTC	3L585	CA3083
A5U3C	1858-0058	8		TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	MPQ3906
A5U3D	1820-0802	1	6	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U3E	1820-1400	7	2	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U3F	1820-2848	9	5	IC-MC10H131P	28480	1820-2848
A5U3G	1820-2849	0	7	IC-MC10H131P	28480	1820-2849
A5U3H	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A5U3I	1820-1788	4	1	IC CNTR FCL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A5U3J	1820-1359	5	5	IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U3K	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U3L	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U4C	1820-2193	7	3	IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A5U4D	1820-0827	0	1	IC DCDR ECL BIN 3-TO-8-LINE	04713	MC10161P
A5U4E	1820-2848	9		IC-MC10H131P	28480	1820-2848
A5U4F	1810-0610	8	2	DELAY LINE- 19NS X 4	28480	1810-0610
A5U4G	1820-2823	0	1	IC-MC10H10Z	28480	1820-2823
A5U4H	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A5U4I	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U4J	1820-0817	8	2	IC FF ECL D-M/S DUAL	04713	MC10131P
A5U4K	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U4L	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
A5U5C	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A5U5D	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U5E	1820-2848	9		IC-MC10H131P	28480	1820-2848
A5U5F	1810-0610	8		DELAY LINE- 19NS X 4	28480	1810-0610
A5U5G	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U5H	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5U5I	1820-0804	3	1	IC GATE ECL NOR TPL	04713	MC10106P
A5U5J	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U5K	1820-2475	8	2	IC LCH ECL GATED D NEG-EDGE-TRIG COM	04713	MC10133P
A5U5L	1820-2475	8		IC LCH ECL GATED D NEG-EDGE-TRIG COM	04713	MC10133P
A5U6A	1820-2848	9		IC-MC10H131P	28480	1820-2848
A5U6B	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A5U6C	1820-2847	8	1	IC-MC10153P	28480	1820-2847
A5U6D	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A5U6F	1820-2905	9	2	IC-SC25647	28480	1820-2905
A5U6I	1816-1462	2	8	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6K	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6L	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U7A	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U7B	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U7C	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U7D	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U8B	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U8C	1820-2875	2	2	IC-MC10H164P	28480	1820-2875
A5U8D	1820-2875	2		IC-MC10H164P	28480	1820-2875
A5U8F	1820-2905	9		IC-SC25647	28480	1820-2905
A5U8I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8K	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8L	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U9B	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U9C	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U9D	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U9E	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U9F	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A5U9G	1820-2848	9		IC-MC10H131P	28480	1820-2848
A5U9H	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A5U9I	1820-2821	8	1	IC-MC10159P	28480	1820-2821
A5U9J	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A5U9K	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5U9L	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A5XU6F	1200-1001	0	2	SOCKET-68 PIN	28480	1200-1001
A5XU8F	1200-1001	0		SOCKET-68 PIN	28480	1200-1001

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	01630-66504	7	1	KEYBOARD ASSEMBLY (INCLUDES KEYCAPS)	28480	01630-66504
	1200-0474	9	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
	3101-2603	2	38	KEY SWITCH-SPST	28480	3101-2603
	5041-0433	6	1	KEY CAP (BLUE)	28480	5041-0433
	5041-0655	4	1	KEY CAP-INSERT	28480	5041-0655
	5041-0900	2	1	KEYCAP-A	28480	5041-0900
	5041-0901	3	1	KEYCAP-B	28480	5041-0901
	5041-0902	4	1	KEYCAP-C	28480	5041-0902
	5041-0903	5	1	KEYCAP-D	28480	5041-0903
	5041-0906	8	1	KEYCAP-0	28480	5041-0906
	5041-0907	9	1	KEYCAP-1	28480	5041-0907
	5041-0908	0	1	KEYCAP-2	28480	5041-0908
	5041-0909	1	1	KEYCAP-3	28480	5041-0909
	5041-0910	4	1	KEYCAP-4	28480	5041-0910
	5041-0911	5	1	KEYCAP-5	28480	5041-0911
	5041-0912	6	1	KEYCAP-6	28480	5041-0912
	5041-0913	7	1	KEYCAP-7	28480	5041-0913
	5041-0914	8	1	KEYCAP-8	28480	5041-0914
	5041-2777	5	1	KEYCAP-PREV	28480	5041-2777
	5041-2778	6	1	KEYCAP-NEXT	28480	5041-2778
	5041-2779	7	1	KEYCAP-CHART	28480	5041-2779
	5041-2780	0	1	KEYCAP-WFORM	28480	5041-2780
	5041-2781	1	1	KEYCAP-SYSTEM	28480	5041-2781
	5041-2782	2	1	KYCP-ARROW UP LT	28480	5041-2782
	5041-2783	3	1	KYCP-DON'T CARE	28480	5041-2783
	5041-2784	4	1	KEYCAP-E	28480	5041-2784
	5041-2785	5	1	KEYCAP-F	28480	5041-2785
	5041-2786	6	1	KYCP-ARROW SIDE DK	28480	5041-2786
	5041-2787	7	1	KYCP-ARROW UP DK	28480	5041-2787
	5041-2788	8	1	KEYCAP-RUN	28480	5041-2788
	5041-2789	9	1	KEYCAP-STOP	28480	5041-2789
	5041-2790	2	1	KEYCAP-PRINT	28480	5041-2790
	5041-2791	3	1	KYCP-CLEAR ENTRY	28480	5041-2791
	5041-2792	4	1	KEYCAP-LIST	28480	5041-2792
	5041-2793	5	1	KEYCAP-FORMAT	28480	5041-2793
	5041-2794	6	1	KEYCAP-TRACE	28480	5041-2794
	5041-2795	7	1	KEYCAP-CHS	28480	5041-2795

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	01630-66508	1	1	TIMING SLAVE ASSEMBLY (1630D ONLY)	28480	01630-66508
A8C1	0160-5298	8	35	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C5	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C7	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C9	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C12	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C13	0160-5506	1	1	CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A8C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C26	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C27	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C28	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C29	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C34	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C36	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A8C37	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A8C38	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A8J1	1251-7705	0	1	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A8MP1	1205-0484	1	2	HEAT SINK SOCKET	28480	1205-0484
A8P1	1251-7868	6	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-7868
A8R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A8RP1	1810-0382	1	13	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP2	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP3	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP4	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP6	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP7	1810-0350	3	2	NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A8RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP10	1810-0350	3		NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A8RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP14	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8U1C	1820-2848	9	4	IC-MC10H131P	28480	1820-2848
A8U1D	1820-2848	9		IC-MC10H131P	28480	1820-2848
A8U2C	1820-2848	9		IC-MC10H131P	28480	1820-2848
A8U2D	1820-2821	8	1	IC-MC10159P	28480	1820-2821
A8U2F	1820-0820	3	2	IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A8U2H	1820-3102	0	3	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A8U2I	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A8U3A	1820-1831	8	1	IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A8U3B	1820-0802	1	3	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U3C,U3D	1810-0610	8	2	DELAY LINE- 19NS X 4	28480	1810-0610
A8U3E	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U3F	1820-1400	7	2	IC GATE ECL AND QUAD 2-INP	04713	MC10104P

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8U3H	1820-2023	2	1	IC GATE ECL AND HEX 2-INP	04713	MC10197P
A8U3I	1820-2847	8	1	IC-MC10153P	28480	1020-2847
A8U3J	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U4C	1820-2905	9	2	IC-SC25647	28480	1820-2905
A8U4F	1816-1462	2	8	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4G	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5C	1820-2905	9		IC-SC25647	28480	1820-2905
A8U5F	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5G	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U6A	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A8U6B	1820-2849	0	1	IC-MC10H131P	28480	1820-2849
A8U6C	1820-2848	9		IC-MC10H131P	28480	1820-2848
A8U6D	1820-1225	4	2	IC FF ECL D-M/S DUAL	04713	MC10231P
A8U6E	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A8U6F	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A8U6G	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A8U6H	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A8U6I	1820-1788	4	1	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A8XU4C	1200-1001	0	2	SOCKET-68 PIN	28480	1200-1001
A8XU5C	1200-1001	0		SOCKET-68 PIN	28480	1200-1001

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	10271A	6	3	STATE MASTER PROBE	28480	10271A
A9MP1	10271-61601	9	1	CBL ASY-TERMINATED	28480	10271-61601
A9MP2	5041-3185	1	1	POD-BOTTOM DARK	28480	5041-3185
A9MP3	5041-3189	5	1	POD-TOP DARK	28480	5041-3189
A9MP4	10271-63201	9	1	CLIP ASY-10 CHAN	28480	10271-63201
A9MP5	10230-62101	7	11	GRABBER ASSY	28480	10230-62101
A9U1	1NB7-8023	0	1	10 CHAN-HYB	28480	1NB7-8023
	7121-3655	2	1	LABEL-STAT POD 3	28480	7121-3655
	7121-3656	3	1	LABEL-STAT POD 2	28480	7121-3656
	7121-3660	9	1	LABEL-STAT POD 4	28480	7121-3660
	7121-3738	2	1	LABEL-ID 10271A	28480	7121-3738
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901
A10	10272A	7	AR	TIMING PROBE (1630A QTY 1, 1630D QTY 2)	28480	10272A
A10MP1	10271-61601	9	1	CABLE ASSY-TERMINATED	28480	10271-61601
A10MP2	5041-3188	4	1	PCD-BOTM LIGHT	28480	5041-3188
A10MP3	5041-3187	3	1	PCD-TOP LIGHT	28480	5041-3187
A10MP4	10272-63201	0	1	CLIP ASSY-8 CHAN	28480	10272-63201
A10MP5	10230-62101	7	9	GRABBER ASSY	28480	10230-62101
A10U1	1NB7-8022	9	1	8 CHAN-HYB	28480	1NB7-8022
	7121-3661	0	1	LBL-ST/TIM POD 0	28480	7121-3661
	7121-3662	1	1	LBL-ST/TIM POD 1	28480	7121-3662
	7121-3737	1	1	LABEL-ID 10272A	28480	7121-3737
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	01630-66517	2	1	STATE SLAVE ASSEMBLY (1630G ONLY)	28480	01630-66517
A11C1	0160-5298	8	80	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C5	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C7	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C9	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C12	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C13	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C26	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C27	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C28	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C29	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C34	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C36	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C37	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C38	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C39	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C40	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C41	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C43	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C44	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C45	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C46	0160-3508	9	3	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C47	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C48	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C49	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C50	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C51	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C52	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C53	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C54	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C55	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C56	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C57	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C58	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C59	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C60	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C61	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C62	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C63	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C64	0160-5309	2	1	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A11C65	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C66	0160-5329	6	1	CAPACITOR-FXD 47PF +-5% 200VDC CER	28480	0160-5329
A11C67	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C68	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C69	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C70	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C71	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C72	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11C73	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C74	0180-0228	6	2	CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X9015B2
A11C75	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C76	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C77	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C78	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C79	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C80	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C81	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C82	0180-0228	6		CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X9015B2
A11C83	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C84	0180-0229	7	3	CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A11C85	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C86	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A11C87	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C88	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A11C89	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C90	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11CR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W	28480	1902-3002
A11DL1	1810-0602	8	1	DELAY LINE 7NS	28480	1810-0602
A11J1	1251-7705	0	3	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11J2	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11J3	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11P1	1251-7868	6	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-7868
A11Q1	1853-0006	6	1	TRANSISTOR PNP SI TO 5 PD=600MW	04713	2N3134
A11R1	0757-0401	0	3	RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R2	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0 +-100	24546	C4-1/8-TO-51R1-F
A11R3	0757-0446	3	1	RESISTOR 15K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1502-F
A11R4	2100-2655	1	1	RESISTOR TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A11R5	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1002-F
A11R6	0698-3226	7	1	RESISTOR 6.49K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-6491-F
A11R7	0699-1000	3	4	RESISTOR 4.25K .1%	28480	0699-1000
A11R8	0699-1000	3		RESISTOR 4.25K .1%	28480	0699-1000
A11R9	0699-1000	3		RESISTOR 4.25K .1%	28480	0699-1000
A11R10	0698-6360	6	4	RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R11	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R12	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R13	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R14	0699-1000	3		RESISTOR 4.26K .1%	28480	0699-1000
A11R15	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0 +-100	24546	C4-1/8-TO-681R-F
A11R16	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1001-F
A11R17	0757-0404	3	1	RESISTOR 130 1% .125W F TC=0 +-100	24546	C4-1/8-TO-130R-F
A11R18	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-5111-F
A11R19	0757-0401	0		RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R20	0757-0401	0		RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1001-F
A11RP1	1810-0272	8	7	NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP2	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP3	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP4	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP5	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP6	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP7	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP8	1810-0382	1	14	NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP9	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP10	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP11	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP12	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP13	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP14	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP15	1810-0411	7	1	NETWORK RES 10-SIP 50 OHM X 9	56289	256CK500X2PD
A11RP16	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP17	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP18	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP19	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP20	1810-0275	1	3	NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP21	1810-0275	1		NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP22	1810-0275	1		NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP23	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP24	1810-0277	3	2	NETWORK RES 10-SIP 2200 OHM X 9	01121	210A222
A11RP25	1810-0277	3		NETWORK RES 10-SIP 2200 OHM X 9	01121	210A222

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11RP26	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9100	01121	210A33
A11RP27	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9100	01121	210A33
A11U1A	1820-3461	4	9	IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1B	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1C	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1D	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1E	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1F	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1G	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1H	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1I	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1K	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A11U1L	1820-2508	8	2	IC GATE ECL EXCL-OR QUAD 2-INP	04713	MC10113P
A11U1M	1820-2508	8		IC GATE ECL EXCL-OR QUAD 2-INP	04713	MC10113P
A11U2B	1820-3102	0	11	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2C	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2D	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2E	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2F	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2G	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2H	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2I	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2J	1820-2193	7	4	IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176L
A11U2K	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2L	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U2M	1820-3102	0		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016
A11U3A	1816-1591	8	13	IC RAM 1K X 4	28480	1816-1591
A11U3B	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3C	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3D	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3E	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3F	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3G	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3H	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3I	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3J	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3K	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3L	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3M	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U4A	1826-0718	0	1	IC VOLTAGE REGULATOR	28480	1826-0718
A11U4B	1816-1555	4	4	IC RAM 10422-6	28480	1816-1555
A11U4D	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4F	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4H	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4J	1NB4-5009	0	1	IC COUNTER 20 BIT GRAY CODE	28480	1NB4-5009
A11U4M	1826-0271	0	1	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A11U5K	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176L
A11U5L	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176L
A11U5M	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176L
A11U6B	1826-0753	3	1	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MS34004BL
A11U6C	1826-0856	7	2	IC CONV 8-BIT-D/A 20-DIP-PKG	34335	AM6080APC
A11U6D	1826-0856	7		IC CONV 8-BIT-D/A 20-DIP-PKG	34335	AM6080APC
A11U6E	1816-3366	9	4	IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1816-3366
A11U6G	1816-3366	9		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1816-3366
A11U6H	1816-3366	9		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1816-3366
A11U6I	1816-3366	9		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1816-3366
A11U6K	0960-0530	7	1	IC OSCILLATOR 25MHZ	28480	0960-0530
A11U6L	1820-1173	1	3	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A11U6M	1820-1052	5	4	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A11U7B	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A11U7C	1820-1216	3	1	IC DC DR TTL LS 3-TO-8-LINE 2-INP	01295	SN75LS138N
A11U7D	1820-3299	6	1	IC BFR TTL HC LINE DRVR DUAL-QUAD	28480	1820-3299
A11U7E	1820-3399	7	1	IC FF TTL HC D-TYPE OCTAL	04713	74HC273
A11U7F	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U7G	1820-1917	1	1	IC BFR TTL LS LINE DRVR DUAL-QUAD	01295	SN74LS240N
A11U7H	1820-2096	9	2	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A11U7I	1820-0802	1	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A11U7J	1820-3400	1	1	IC GATE ECL NOR DUAL 3-INP 3-OUT	04713	MC10H211
A11U7K	1820-0817	8	4	IC FF ECL D-M/S DUAL	04713	MC10131P
A11U7L	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U7M	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U8C	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A11U8D	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A11U8E	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11U8F	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A11U8G	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A11U8H	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A11U8I	1820-0810	1	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A11U8J	1820-2891	2	1	IC MC10H101P	28480	1820-2891
A11U8K	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U8L	1820-0803	2	1	IC GATE ECL OR-NOR TPL	04713	MC10105P
A11U8M	1820-0827	0	2	IC DCDR ECL BIN 3-TO-8 LINE	0713	MC10161P
A11U8N	1820-0827	0		IC DCDR ECL BIN 3-TO-8 LINE	0713	MC10161P
A11UR5A	1810-0613	1	2	NETWORK RES 8-DIP	28480	1810-0613
A11UR6A	1810-0613	1		NETWORK RES 8-DIP	28480	1810-0613

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	10273A	8	3	STATE SLAVE PROBE (1630G ONLY)	28480	10273A
A12MP1	10271-61601	9	1	CABLE ASSY-TERMINATED	28480	10271-61601
A12MP2	5041-3185	1	1	POD BOTTOM DARK	28480	5041-3185
A12MP3	5041-3189	5	1	POD TOP DARK	28480	5041-3189
A12MP4	10273-63201	1	1	CLIP ASSY-10 CHANNEL	28480	10273-63201
A12MP5	10230-62101	7	11	GRABBER ASSEMBLY	28480	10230-62101
A12U1	1NB7-8027	4	1	HYBRID-10 CHANNEL	28480	1NB7-8027
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
C0633	RIFA	BROMMA	SE	
S0167	FUJITSU LTD	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
18546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92806
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	N.V. PHILIPS-ELCOMA DEPARTMENT	EINDHOVEN	HL	02876
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52763	STETTNER ELECTRONICS INC	CHATTANOOGA	TN	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON	CA	92634
75915	LITTELFUSE INC	DES PLAINES	IL	60016

SECTION VII
INSTRUMENT CHANGES

7-1. INTRODUCTION

This section contains information describing how this manual documents changes in the instrument. Because of the service philosophy for this instrument, this service manual is not shipped with every instrument. This service manual is therefore required to cover all versions (serial prefixes) of the 1630A/D/G family simultaneously. As a result, the organization of change information is different in this manual than it is in most Hewlett-Packard service manuals.

7-2. MANUAL CHANGES

This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, adjustments to the information provided will have to be made. An attempt has been made to put change information in close proximity to the information it replaces. For example, changes to an assembly part list are located in Section VI next to the section of the part list affected (see Section VI). Differences in schematics due to changes are located on the schematic changed or in close proximity to it. The purpose chosen for this section, Section VII, is to provide a synopsis of the prefix changes made in the instrument and also document some changes not covered directly by different prefixes.

7-3. INSTRUMENT CHANGES

Table 7-1 shows the relationship between serial prefixes and the complement of boards in an instrument as shipped from the factory. Since many boards are directly upgradable to the most recent version, a given instrument may have different boards than it was originally shipped with.

Table 7-1. Board Complements vs. Serial Prefixes.

	BOARD COMPLEMENTS[1]					
SERIAL PREFIXES	1630A/D A - 2247A B - 2234A	1630A/D 2311A	1630A/D NOTE 2	1630A/D 2412A	1630G 2415A	
A1 - Power Supply	66502	66502	66502	66514	66514	
A2 - Motherboard	66501	66501	66501	66501	66501	
A3 - CPU	66503	66503	66512	66522	66519	
A4 - State Master	66505	66509	66509	66518	66518	
A5 - Timing Master	66506	66510	66510	66510	66524	
A6 - Display[3]	0950-0894					
A7 - Keyboard	66504	66504	66504	66504	66504	
A8 - Timing Slave	66508	66508	66508	66508	-----	
A11- State Slave	-----	-----	-----	-----	66517	

NOTES:
1. All board numbers should be prefixed with "01630-".
2. Serial numbers: 1630A, 2311A00231 and up; 1630D, 2311A00791 and up.
3. The display board is supported as a complete replacement part only.

Instruments are also up and down-gradable to other versions within the family. For example, A 1630A can be converted to a 1630D or 1630G and the 1630G can be converted to a 1630D. This can cause different relationships between model numbers, serial prefixes, and board complements, than is shown in this manual.

7-4. INSTRUMENT FAMILY HISTORY

The following is a history of the major changes in the 1630 models. The first serial prefixes were 2242A for the 1630A and 2234A for the 1630D. The first prefix for the 1630G was 2415A.

1. Parts were changed, on the Master State and Master and Slave Timing boards, to a preferred part. Most (not all) 1820-1788 were changed to 1820-3102. Parts involved were:

   a) On State Master A4; U3J-L; U6B-E; U7E-H.
   b) On Timing Master A5; U1K,L; U2K,L; U7C; U9K,L.
   c) On Timing Slave A8; U2H,I.

2. An RFI problem necessitated isolating part of the HP-IL circuitry on the CPU board A3. Several parts were removed from the main board, 01630-66503, and mounted on al small board piggy-backed to the main board. There was no serial prefix change.

   a) Effective instruments were:
      1) 1630A - serial number 2242A00121 and up.
      2) 1630D - serial number 2234A00241 and up.

   b) Parts affected were:
      1) Removed from 01630-66503 were C1,2; CR1,2; T1.
      2) Piggy-back board was 01630-66511 loaded with the parts listed above.

3. Serial prefix change from 2234A (1630A) and 2242A (1630D) to 2311A (1630A/D)

   a) State Master board changed from 01630-66505 to 01630-66509. The 66509 directly replaces the 66505.

      1) U4L changed from 1820-2451 to 1820-2959.
      2) U4L circuitry layed out to accomodate the new part (schematic 8C-7).
      3) Traces removed between U3N-14 and U4M-4 (schematics 8C-2 and 8C-7).
      4) Traces removed between U3N-15 and U4L-10/U6K-5 (schematics 8C-2 and 8C-7).
      5) Traces to U6G-12, 13, 14, and 15 removed (schematic 8C-4).
      6) U8K changed from 1820-2495 to 1820-2963 (prefered part).

   b) Timing Master board changed from 01630-66506 to 01630-66510. The 66510 directly replaces the 66506.

      The gate of U7D comprised of pins 9, 12, 13 and 15 was swapped with the gate of U7D comprised of pins 2, 4, 5. See Schematic 8D-3.

4. An electrostatic discharge (ESD) problem with the HP-IL chip on the CPU board, A3 01630-66512, necessitated the addition of protective parts. A small PC board was made to hold the HP-IL chip, U2O, and the added parts and that was plugged into the HP-IL chip socket. There was no instrument serial prefix change.

   a) Effective instruments were:
      1) 1630A - serial number 2311A00232 and up.
      2) 1630D - serial number 2311A00792 and up.

   a) The parts added were:

1) PC board, A3A1	01630-66513(includes all parts)
2) Resistor, A3A1R1	0683-4705
3) Capacitor, A3A1C1	0160-5246
4) Diodes, A3A1CR1-4	1901-0050
5) Socket	1200-0567
6) 14 pin post set (2)	1251-5064

   b) Schematic documentation for this change is on schematic 8B-7.

5. This change incorporated the final fix for the RFI problem on A3 CPU which was corrected without prefix change (#2 above). It also incorporated a change to the reset timing circuitry on the CPU. There was no instrument serial prefix change.

   a) A3 CPU changed from 01630-66503 to 01630-66512.

   b) The small piggy-back board was deleted and the parts on it were moved back to the main board.

   c) The new A3 incorporated a re-layout which moved the connection of U3 pin 11 from U7 pin 1 to U7 pin 7. Schematic changes are noted on schematic 8B-2.

   d) U2O pin 2 was pulled up to +5V using RP2 pin 9, schematic 8B-7.

6. A turn-on surge problem when running the instrument with 240VAC input was corrected on A1, Power Supply. Transient suppressor RV2 was changed to a higher voltage value. This is a prefered part change and the new part should be used for all replacements.

7. Serial prefix change from 2311A (1630A/D) to 2412A (1630A/D).

   a) Several mainframe parts were changed to allow more direct retrofit of the 1630A and 1630D to the new 1630G. Changes are noted in the parts list.

   b) To eliminate turn-on surge problems the fan was changed from a 120V type to a 120/240V model. This also necessitated the change of the power supply board from 01630-66502 to 01630-66514. Schematic changes are on Schematic 8A-1.

c) The CPU board was changed from 01630-66512 to 01630-66522. This allows this board to be used in a 1630G. Schematic changes are noted on Schematic 8B-1.

d) The Master State board was changed from 01630-66509 to 01630-66518. Schematic changes are noted on Schematic 8C-7. Parts changes are noted in the Parts List.

NOTE: The primary parts changed were U3A-C,E-G,I from 1816-1492 to 1816-1591 and U2B-C,E-I from 1820-1788 to 1820-3102. When replacing any of these parts it should be noted that the new RAM, 1816-1591, will work with the old counter, 1820-1788, but the new counter, 1820-3102, will not work with the old RAM, 1816-1492. Any replacement of counters on older boards must use the older part number.

8. Ineffectiveness and reliability problems necessitated the removal of several parts on the power supply board. Neon bulbs A1E1 and A1E2 have been removed from the circuit. In addition, RT1 and RT2, in series with E1 and E2 respectively, have been removed. See the appropriate service note in Appendix E.

a) Effective instruments were:
1) 1630A - serial number 2412A00809 and up.
2) 1630D - serial number 2412A03411 and up.
3) 1630G - serial number 2415A00172 and up

SECTION VIII

SERVICE

8-1. INTRODUCTION

The service section provides theory, block diagrams, and schematics for troubleshooting the 1630A/D/G.

This section consists of six sections or service groups:

8A - Power Supply and Motherboard
8B - CPU, Keyboard, and Display
8C - State Master Acquisition
8D - Timing Master Acquisition
8E - Timing Slave Acquisition
8F - State Slave Acquisition

Each service group contains its own table of contents, theory, block diagrams, and schematics pertaining to that subsystem.

8-2. SAFETY CONSIDERATIONS

Read the Safety Summary at the front of this manual before servicing this instrument. Before performing each procedure, review it for cautions and warnings. For example, when working around the power supply and display circuitry, caution should be taken to avoid potentially lethal voltages.

CAUTION

An external cooling fan is required to cool PC boards inserted into the service connecter. An adequate fan should be available to any service organization.

8-3. BLOCK DIAGRAM THEORY (see figure 8-1)

POWER SUPPLY BOARD. The power supply board supplies +15, +12, -12, +5, -2.4, and -5.2 V to the different boards in the analyzer. The power supply uses the "switching technique" for converting AC to the six DC voltages.

CPU BOARD. The CPU board is the interface between the operator and the system. The CPU board provides measurement programming of the state and timing boards, keyboard control, display generation, HP-IB and HP-IL interfacing, and waveform formatting.

STATE MASTER BOARD. The State Master board receives 27 bits of data and three clocks from Pods 2, 3, and 4. State may also receive either 8 or 16 more bits of data if one or both of the two timing boards are in the State mode.

TIMING MASTER BOARD. The timing master board receives 8 bits of data from a timing pod for timing and glitch analysis. Timing master may be run in the State mode.

TIMING SLAVE BOARD. The Timing Slave board is only supplied in a 1630D. The timing slave receives 8 bits of data from its own pod, allowing Timing Analysis to be as much as 16 bits wide. Slave timing may also be run in the State mode. For 35-bit wide state analysis, only the Timing Slave board can be run in the State mode. In the 35-bit mode the Timing Master must be used for timing, since it contains the timing qualification circuitry.

STATE SLAVE BOARD. The State Slave board is provided only in the 1630G. The State Slave board takes the place of the Timing Slave in the block diagram. Full coverage of this board is covered in Section 8F. It receives thirty channels of data from the target system and stores it under control of the State Master. Relative and absolute counting of stored states and time is provided by this board. The State Master board also provides non-volatile storage of one instrument set-up and microprocessor disassembler.

EXTERNAL INTERFACE. The CPU board may communicate with compatible external devices via HP-IB and HP-IL. HB-IB is a parallel bi-directional form of communication, whereas, HP-IL is a bit-serial unidirectional loop. Devices connected to HP-IB and HP-IL may be either talkers, listeners, or controllers. The 8 switch dip SW1 configures the 1630A/D/G on one of these buses.

The rear panel Port BNC can supply six acquisition signals on a multiplexed basis. An additional BNC supplies a +5 volt output for accessories such as a pre-processor option.

DISPLAY BOARD AND CRT. The display driver is an OEM assembly, not serviced by HP. The display assembly receives video and timing information from the CPU board.

SYSTEM BLOCK DIAGRAM

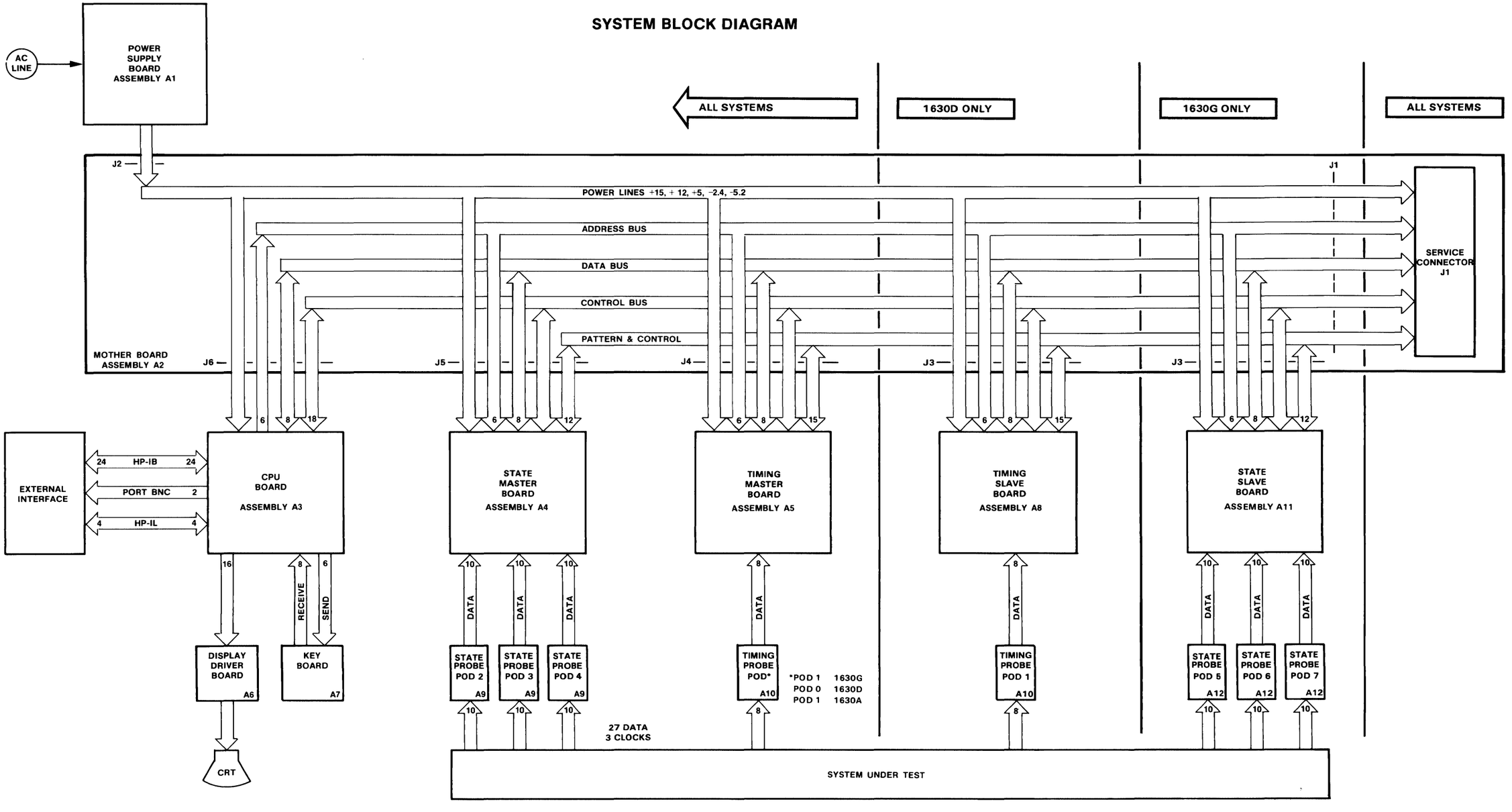


Figure 8-1. System Block Diagram

8-4. LOGIC CONVENTION

Logic states are defined as follows:

0----------False, negated, inactive, or unasserted state.

1----------True, active, or asserted state.

Voltage levels representing logic states:

LOW (L)--------The more negative of two voltage levels.

HIGH (H)-------The more positive of two voltage levels.

Signals may be either HIGH true, or LOW true, as indicated by the mnemonics on the schematics.

The 1630A/D/G includes both TTL and ECL ICs. Worst case voltage levels for troubleshooting and signature analysis purpose are as follows (IC data sheet specifications may be more accurate):

TTL Voltage Levels

Level	Voltage
LOW	less than 0.8 V
HIGH	greater than 2.0 V

ECL Voltage Levels

Level	Voltage
LOW	less than -1.50 V
HIGH	greater than -1.10 V

8-5. ECL ATTRIBUTES

Because ECL inputs are pulled down inside the IC, an unconnected ECL input is LOW.

ECL outputs may be tied together in the same way as open-collector TTL outputs. Thus, they may be wire-ANDed or wire-ORed.

Table 8-1. Logic Symbols, (sheet 1 of 3)

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

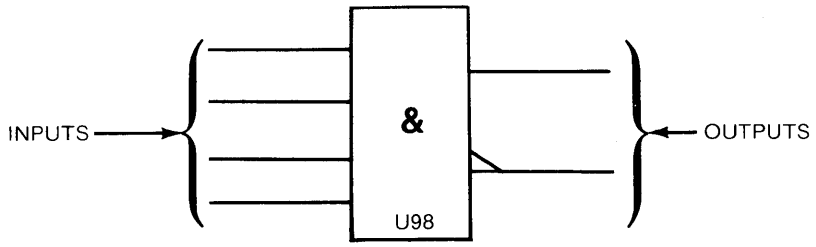
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

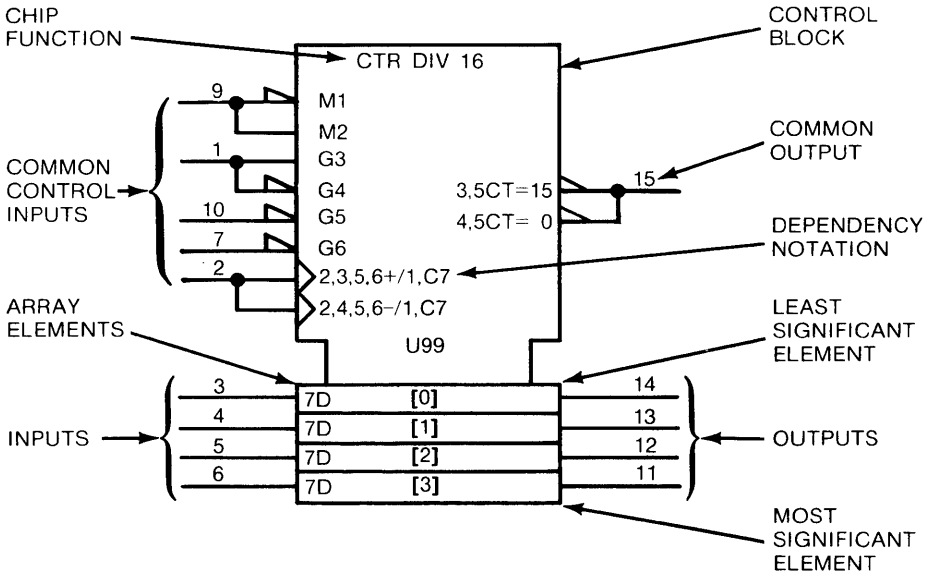
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-1. Logic Symbols, (sheet 2 of 3)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-1. Logic Symbols, (sheet 3 of 3)

OTHER SYMBOLS

∩ Analog Signal	◺◿ Inversion	→ Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
} { Bit Grouping	—✕— Nonlogic Input/Output	▽ Tri-State
▷ Buffer	◇ Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	◇ Open Circuit (external resistor)	
▷ Dynamic	≥1 OR	( ) Used for factoring terms using algebraic techniques.
=1 Exclusive OR	▽ Passive Pull Down (internal resistor)	[ ] Information not defined.
⊓ Hysteresis	△ Passive Pull Up (internal resistor)	Φ Logic symbol not defined due to complexity.
? Interrogation	⌐ Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	−	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

⎍⎍	Astable
100 ns	Delay
1⎍	Nonretriggerable Monostable
NV	Nonvolatile
⎍⎍	Retriggerable Monostable

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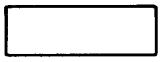
Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD



FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

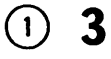
SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO.

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.



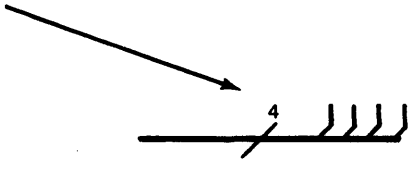
NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

SOURCE (DESTINATION) OF A SINGAL FROM (TO) ANOTHER ASSEMBLY. LETTER GIVES SERVICE GROUP AND NUMBER REFERENCES SCHEMATIC WITHIN THAT GROUP.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) **WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE**

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

8-6. REMOVAL AND INSTALLATION OF MAINFRAME COMPONENTS

This section contains removal instructions for the system PC boards and the CRT. Read the Safety Summary at the front of this manual before servicing this instrument. All removal procedures are based on the 1630D system. The removal procedures also apply to the 1630A and 1630G systems except the 1630A contains one less board.

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and display driver boards to discharge before servicing this instrument. Wear safety glasses!!!

CAUTION

Never install or remove any circuit board with the power switched ON. Component damage may occur!!!

NOTE

When a board is installed verify that it is fully seated into the connector.

8-7. Acquisition Board Removal (State and Timing)

a. Switch power OFF and disconnect the AC power cord.

b. Completely remove the two screws that secure the rear door. See figure 8-2.

c. Carefully remove the probe cable plugs by their plastic housing. See figure 8-3.

d. Remove the four screws that secure the rear cover and remove cover. See figure 8-3.

e. Carefully remove the desired acquisition board by inserting the "board puller" into the removal holes located at the top-center of the board. See figure 8-4.

An acquisition board can be installed by reversing the removal procedure.

8-8. CPU Board Removal

a. Follow steps (a) through (d) of the Acquisition board removal procedure.

b. Completely remove the two screws securing the CPU board to the rear panel. See figure 8-5.

c. Remove the two plastic standoffs and loosen the screw that secures the bottom cover. See figure 8-5.

d. Carefully tilt the instrument on its side and remove the bottom cover.

e. Disconnect the cables from the CPU board that go to the keyboard and the display driver board. See figure 8-6.

f. Carefully remove the CPU board by inserting the "board puller" into the appropriate removal holes located at the rear of the board. See figure 8-4.

The CPU board can be installed by reversing the CPU board removal procedure.

8-9. Power Supply Board Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

CAUTION

Be certain that the perforated side cover is installed on the right-hand side of the instrument (as you face the front of the unit). If the side covers are mis-installed, insufficient air flow will result and component damage may occur.

a. Follow steps (a) through (d) of the Acquisition board removal procedure.

b. Completely remove the two screws securing the CPU board to the rear panel. See figure 8-5.

c. Remove the four plastic standoffs and loosen the two screws that secure the top and bottom covers and remove the covers. See figure 8-7.

d. Loosen the screw that secures the perforated side panel and remove. See figure 8-7.

e. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

f. Carefully tilt instrument on its side and remove the four screws holding the rear panel to the bottom of the frame. See figure 8-8.

g. Disconnect the cables from the CPU board to the keyboard and display driver boards. See figure 8-6.

h. Lay the instrument back on its base. Carefully remove all of the boards from the frame by inserting the "board puller" into the appropriate removal holes located at the rear of each board. See figure 8-4.

i. CAREFULLY remove the power switch shaft with a 1/4 inch wrench. See figure 8-9.

j. Remove the two screws by the line plug and the two screws securing the rear panel to the card cage. See figure 8-10.

k. Remove the four screws that attach the plastic power supply cover and ground strap to the top of the frame. See figure 8-9.

l. Unplug the fan from the power supply and gently push out on each corner from the inside of the rear panel. The rear panel and the fan assembly should remove as one unit.

m. Remove the three screws securing the power supply board to the card cage bracket. See figure 8-11.

n. Pull the power supply board straight back from the motherboard connector and remove from the frame.

The power supply board can be installed by reversing the removal procedure. See figure 8-4 for the card cage slot for each board.

8-10. Motherboard Removal

a. Follow steps (a) through (n) of the power supply board removal procedure.

b. Remove the six screws that secure the motherboard to the keyboard cover. See figure 8-12.

The motherboard can be installed by reversing the removal procedure.

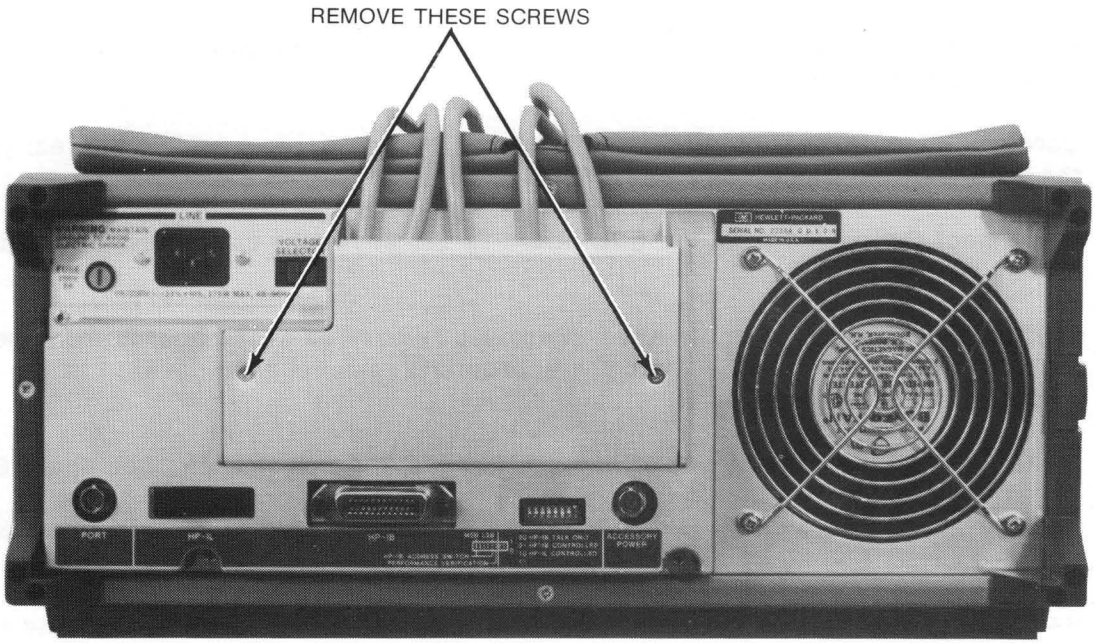


Figure 8-2.

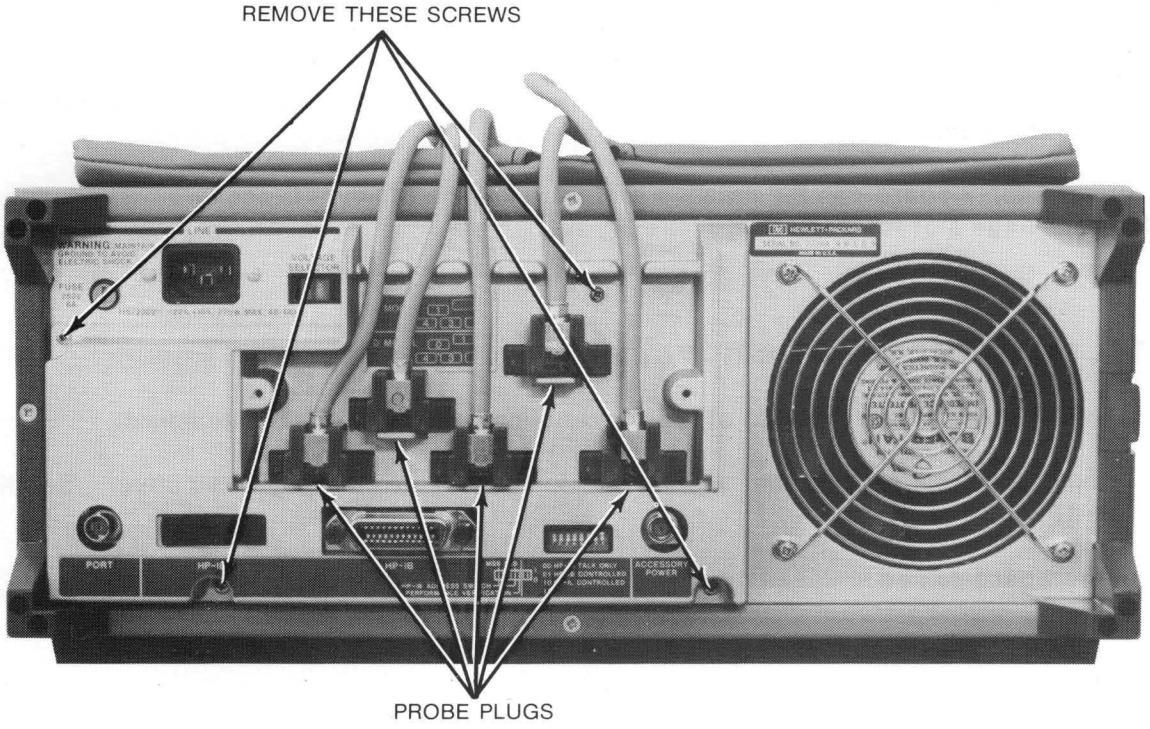


Figure 8-3.

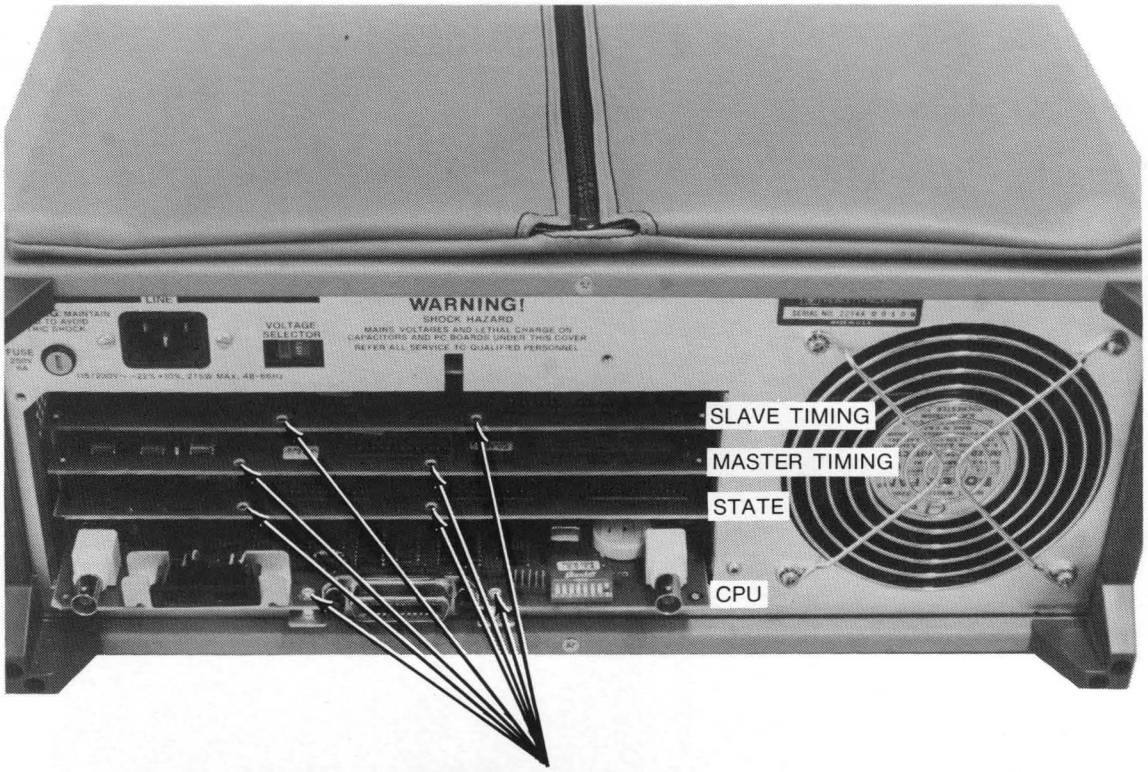


Figure 8-4.

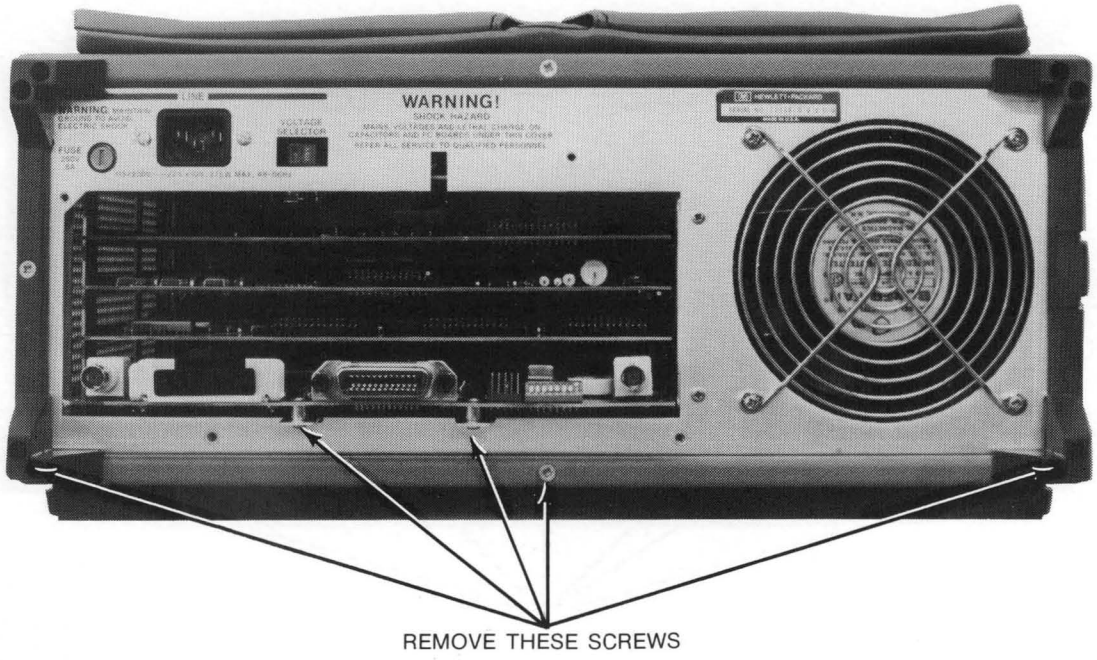


Figure 8-5.

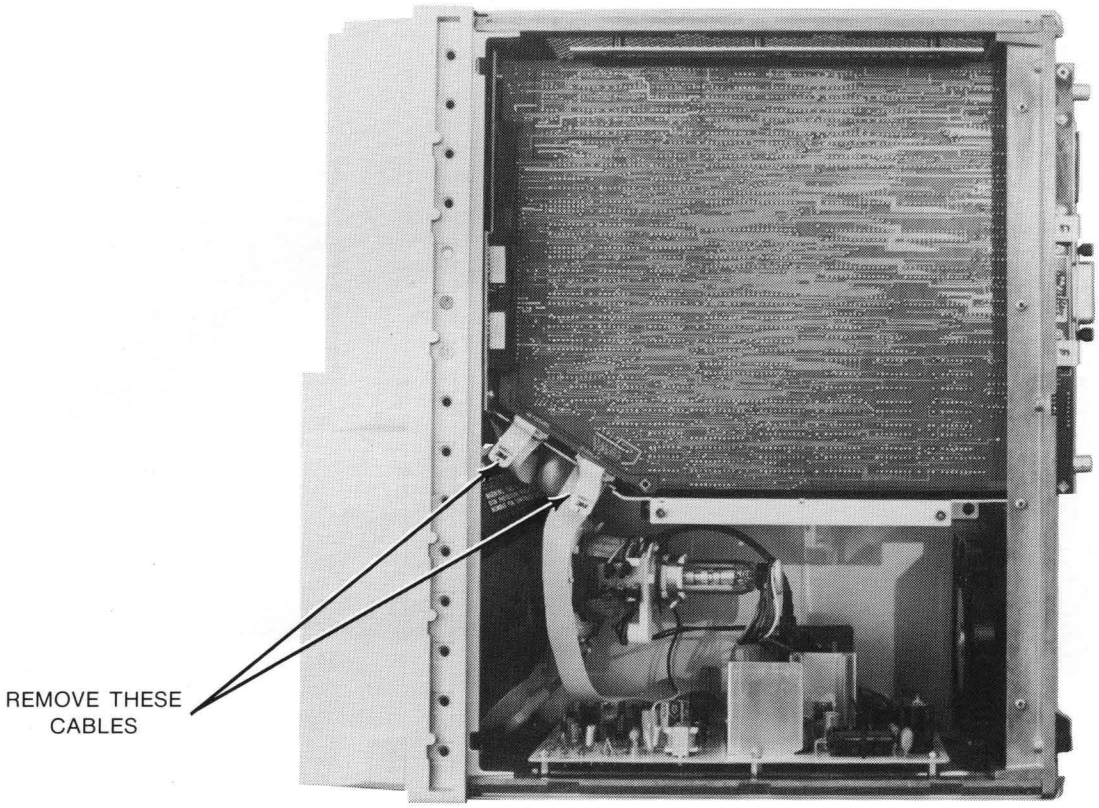


Figure 8-6.

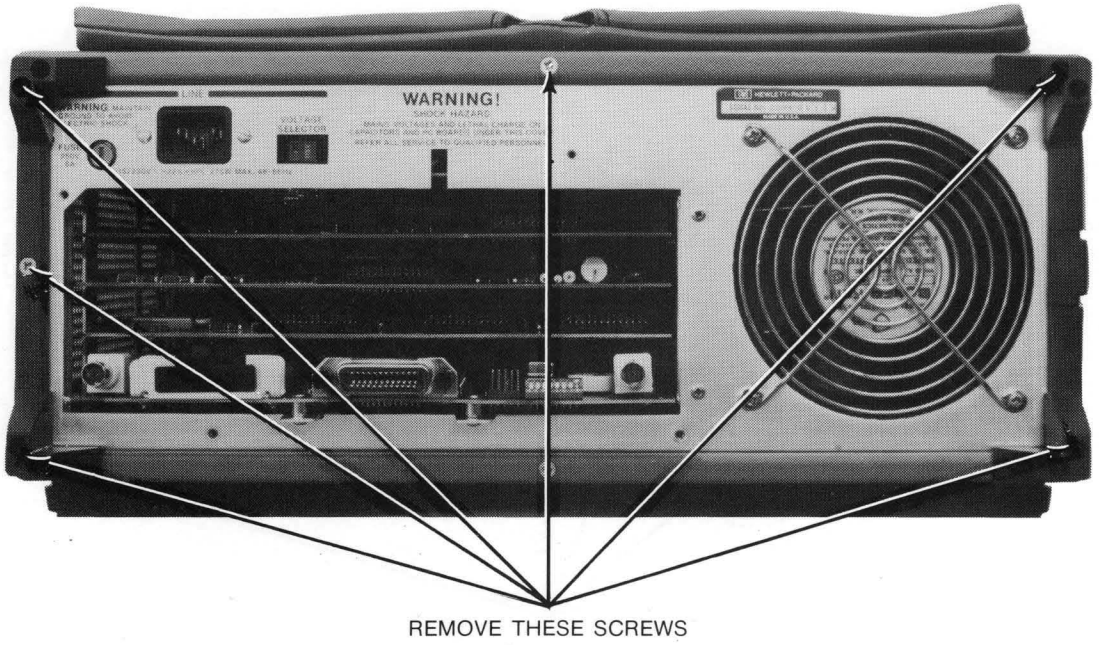


Figure 8-7.

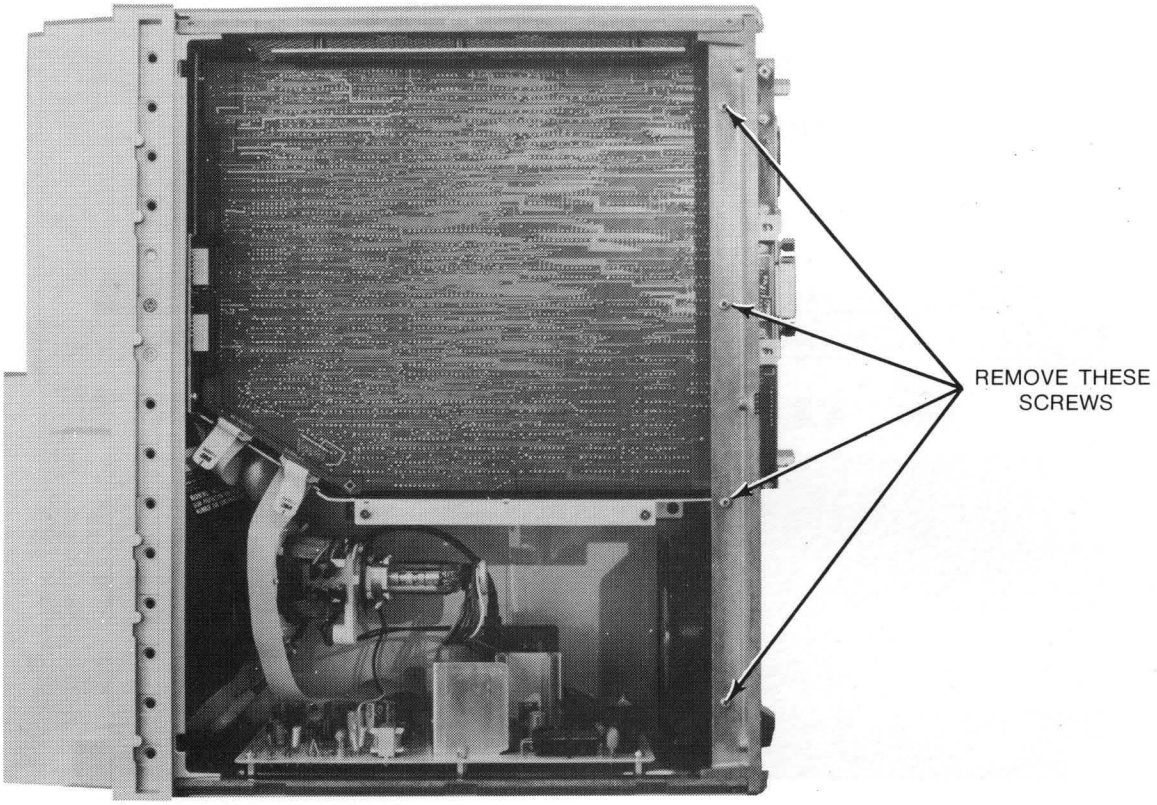


Figure 8-8.

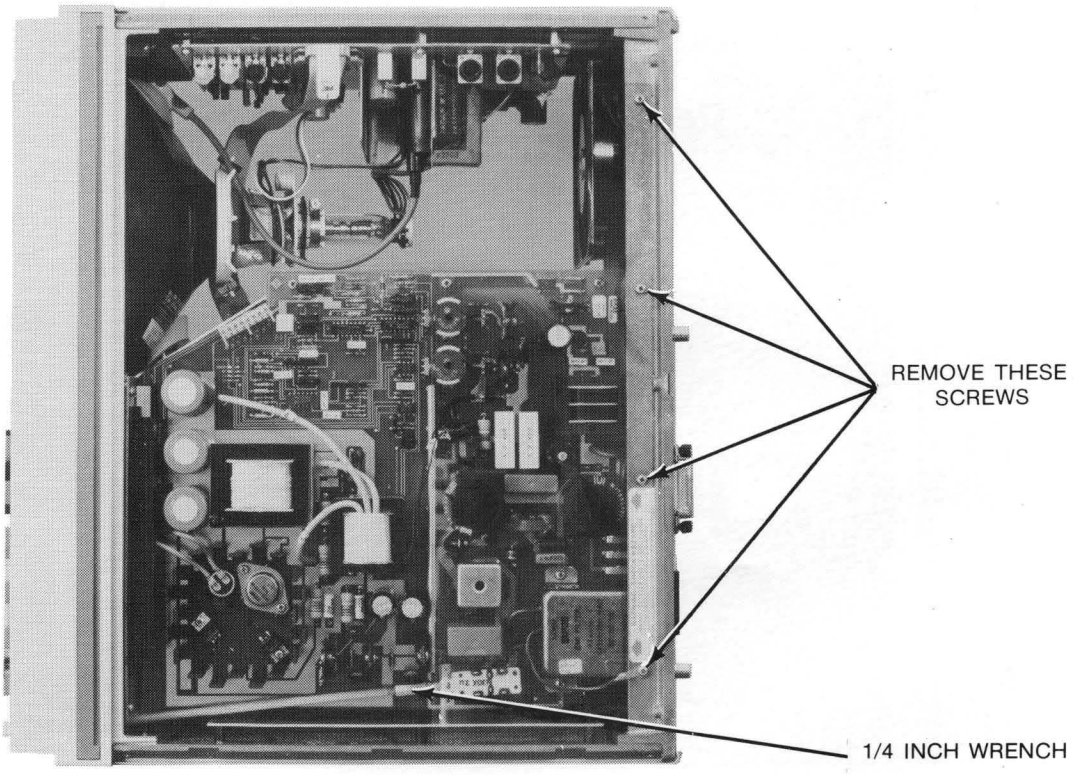


Figure 8-9.

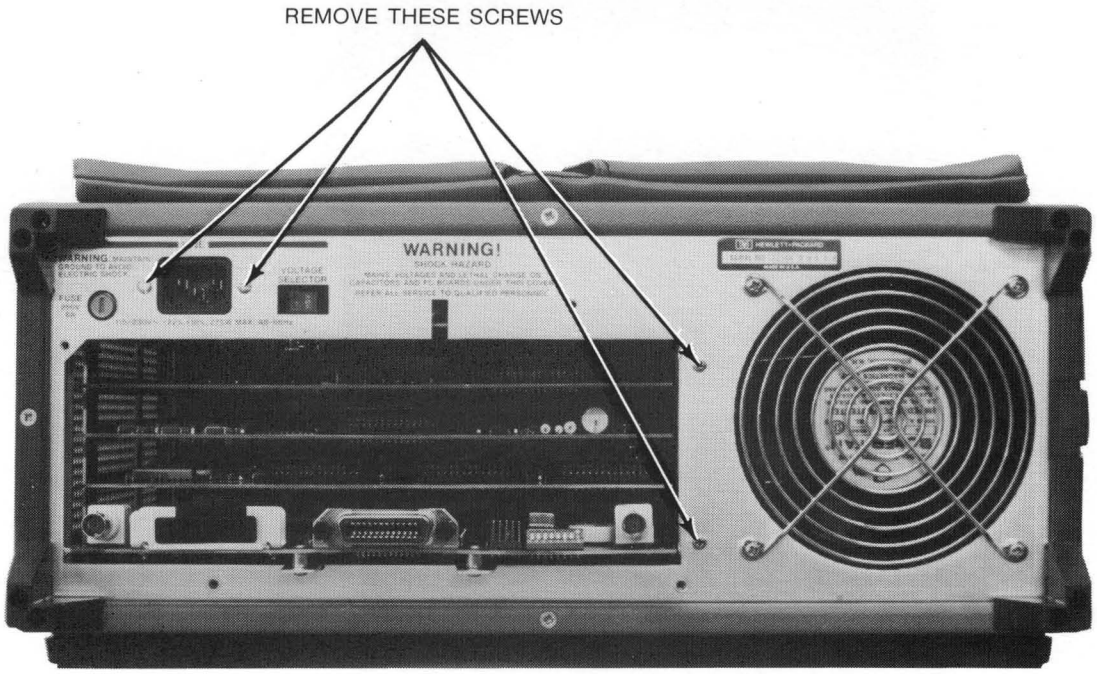


Figure 8-10.

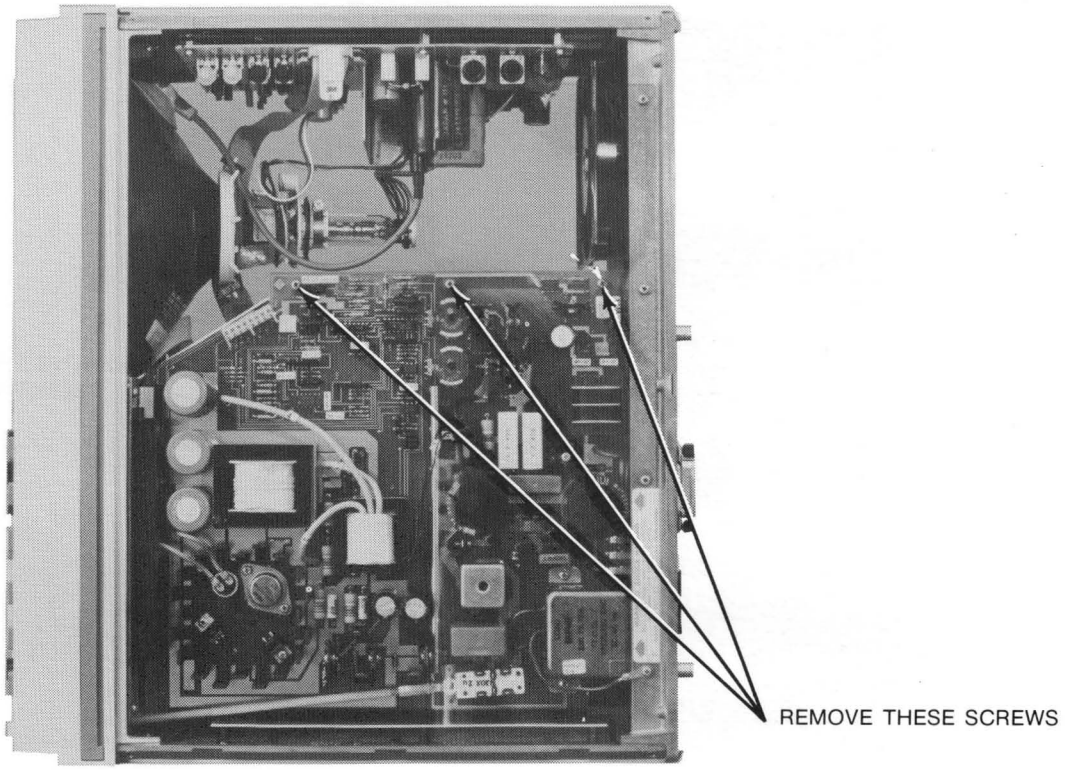


Figure 8-11.

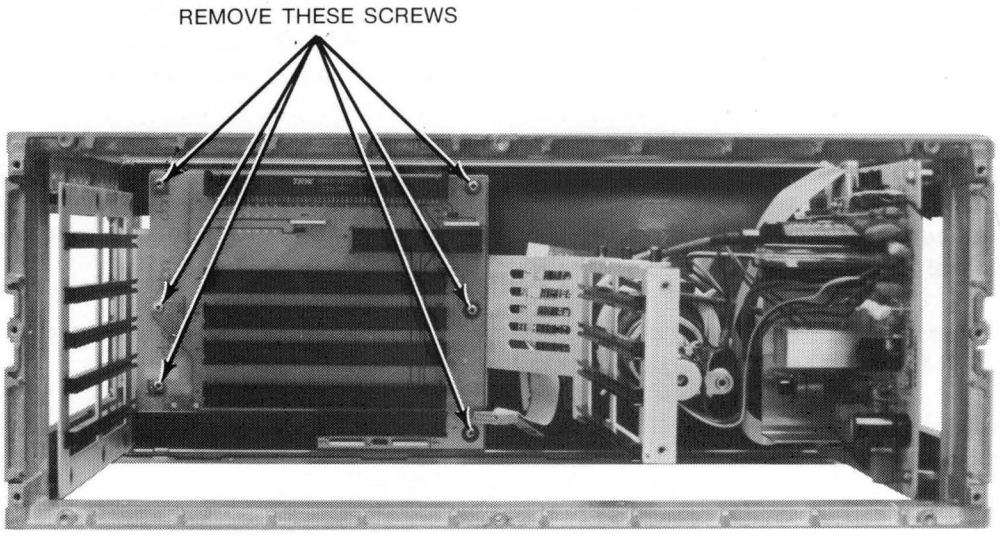


Figure 8-12.

8-11. Keyboard Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

a. Remove the four plastic standoffs and loosen the two screws that secure the top and bottom covers. See figure 8-7.

b. Tilt the instrument on its side and remove the screw indicated in figure 8-13 and the bottom cover.

c. Carefully lay unit in its proper bottom down position and remove the top cover.

d. Carefully pry up and remove the top plastic trim strip and remove the screw indicated in figure 8-14.

e. Slowly peel the two side vinyl adhesive trim strips being careful not to tear them.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

f. Short out the charge on the CRT by connecting a jumper lead between the ground lug of the CRT and the shaft of a screwdriver. Slip the screwdriver under the protective rubber cup of the post accelerator lead and then momentarily touch the screwdriver to the metal clip of the post accelerator lead. See figure 8-14.

g. Disconnect the post accelerator lead from the CRT by firmly squeezing on the rubber cup until the metal clip disengages from the CRT.

h. Disconnect the cable connecting the cathode of the CRT to the display driver. See figure 8-14.

i. Disconnect the two cables connecting the CRT yoke to the display driver. See figure 8-14.

j. Carefully pull and remove the black wire connecting the CRT ground lug to the display driver. See figure 8-14.

k. Remove the four side screws (two screws to a side) that secure the front bezel to the frame. These are located under the adhesive side trim strips. See figure 8-15.

l. Carefully pull the front bezel away from the frame being careful not to scratch the bezel or break the line switch shaft.

m. Remove the four screws and washers connecting the keyboard to the front bezel. See figure 8-16.

To install a keyboard reverse the removal procedure.

8-12. CRT Removal

a. Follow steps (a) through (l) of the keyboard removal procedure. All WARNINGS and CAUTIONS apply for the CRT removal procedure.

b. Remove the four screws and washers securing the CRT to the front bezel. See figure 8-16.

To intall a CRT, reverse the removal procedure.

8-13. Display Driver Removal

a. Turn OFF instrument and remove AC power cord.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove top cover. See figure 8-7.

c. Remove the two screws that connect the handle and the side panel to the frame. Remove side cover.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

d. Short out the charge on the CRT by connecting a jumper lead between the ground lug of the CRT and the shaft of a screwdriver. Slip the screwdriver under the protective rubber cup of the post accelerator lead and then momentarily touch the screwdriver to the metal clip of the post accelerator lead. See figure 8-14.

e. Disconnect the post accelerator lead from the CRT by firmly squeezing on the rubber cup until the metal clip disengages from the CRT.

f. Disconnect the cable connecting the cathode of the CRT to the display driver. See figure 8-14.

g. Disconnect the two cables connecting the CRT yoke to the display driver. See figure 8-14.

h. Carefully pull and remove the black wire connecting the CRT ground lug to the display driver. See figure 8-14.

i. Remove the six screws that mount the display driver on the frame and remove board. See figure 8-17.

To install a display driver board reverse the removal procedure.

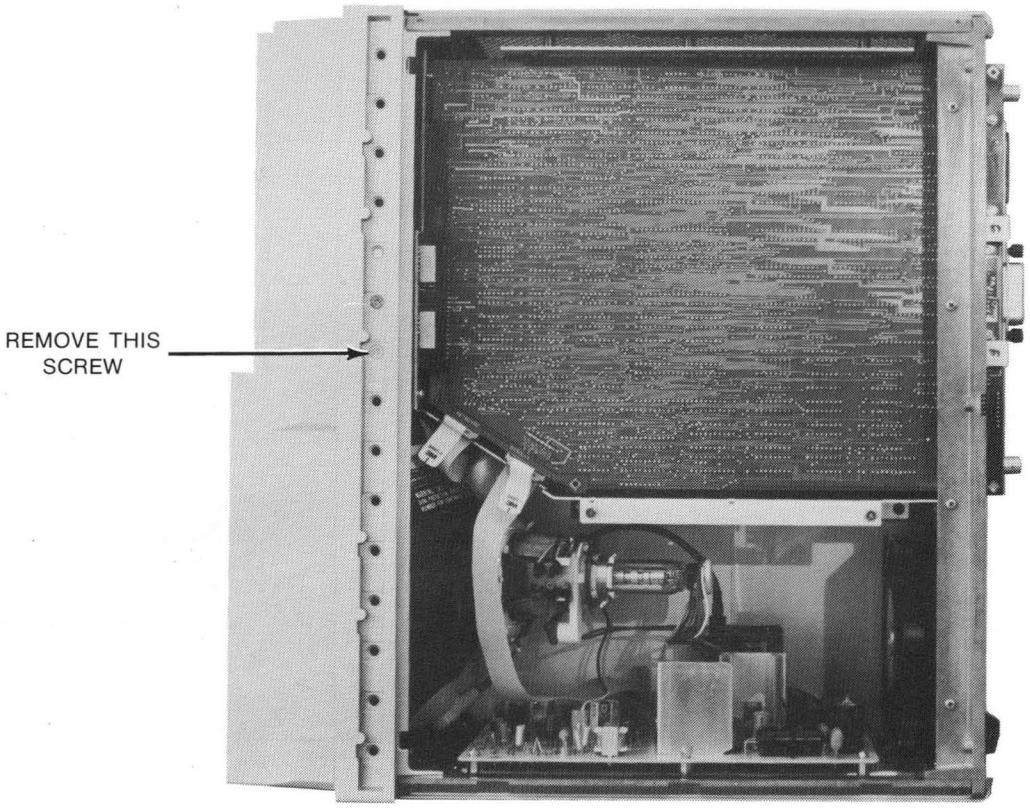
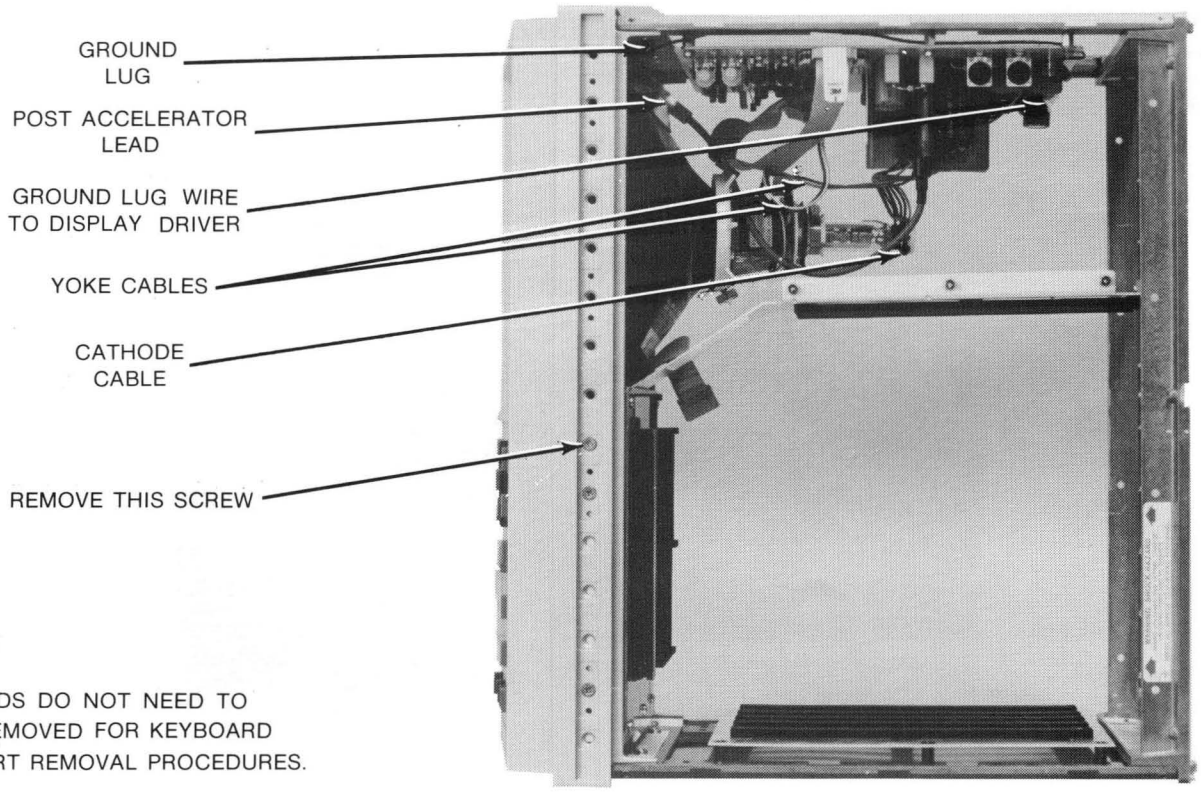


Figure 8-13.



NOTE

BOARDS DO NOT NEED TO
BE REMOVED FOR KEYBOARD
OR CRT REMOVAL PROCEDURES.

Figure 8-14.

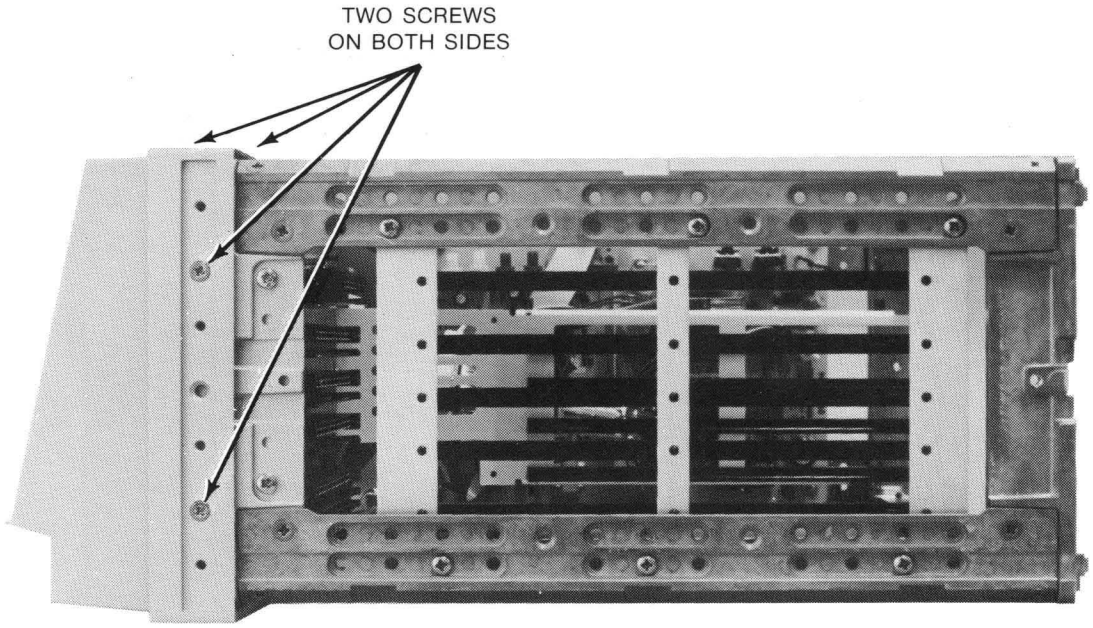


Figure 8-15.

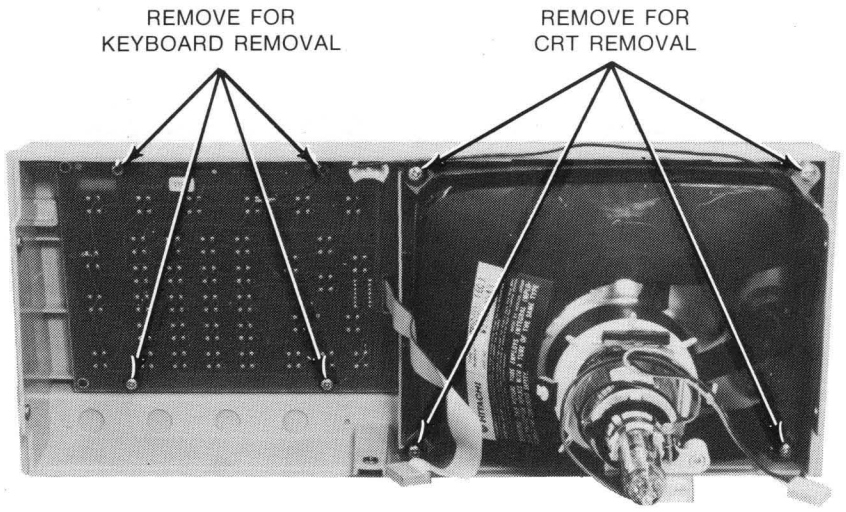


Figure 8-16.

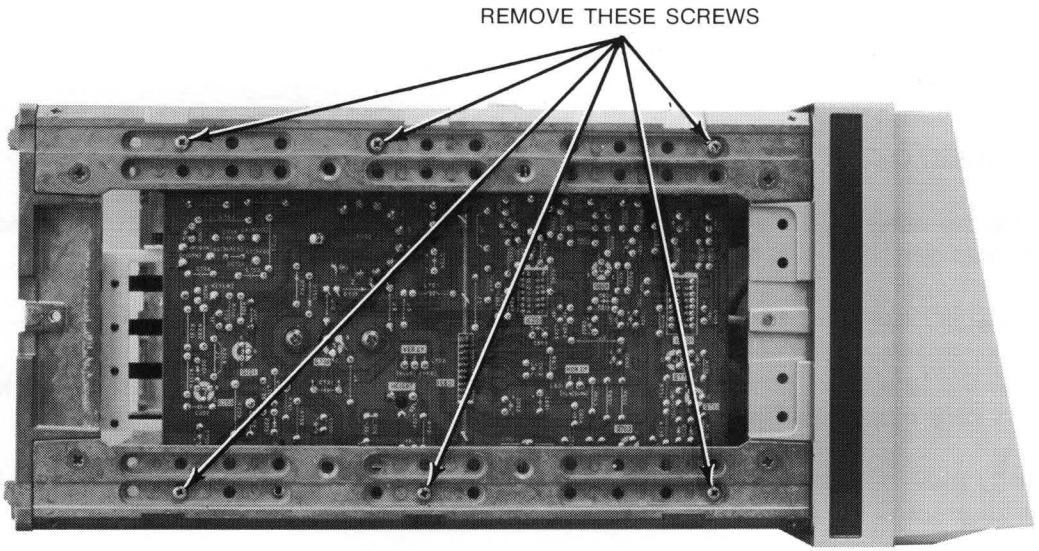


Figure 8-17.

8-14. Probe Disassembly (Hybrid Chip From Cable)

This procedure applies to both 10271A, 10272A, and 10273A probes.

a. Remove the faulty probe cable from the back of the instrument.

b. Remove the clip assembly from the probe housing.

c. With the label facing down insert six toothpicks under the clips that hold the top of the probe housing to the bottom. See figure 8-18.

d. Gently pull the bottom of the probe housing from the top.

e. Remove the cable assembly and the hybrid chip from the top housing. See figure 8-19.

f. While holding the hybrid chip gently pull up on the cable connector and pry the connector away with a screwdriver. Avoid excessive pulling on the cable wires. See figure 8-20.

NOTE

When connecting the probe cable to the hybrid chip make sure that the black wire is in the position indicated on the hybrid chip.

A probe hybrid chip or cable may be installed by reversing the removal procedure.

8-15. Macrocell Removal

a. Gently pry ~~the~~ socket retaining clip away from the heatsink.

b. Carefully pull the heatsink sideways away from the socket. The macrocell chip may come away with the heatsink.

c. Remove the macrocell chip if it is still in the socket.

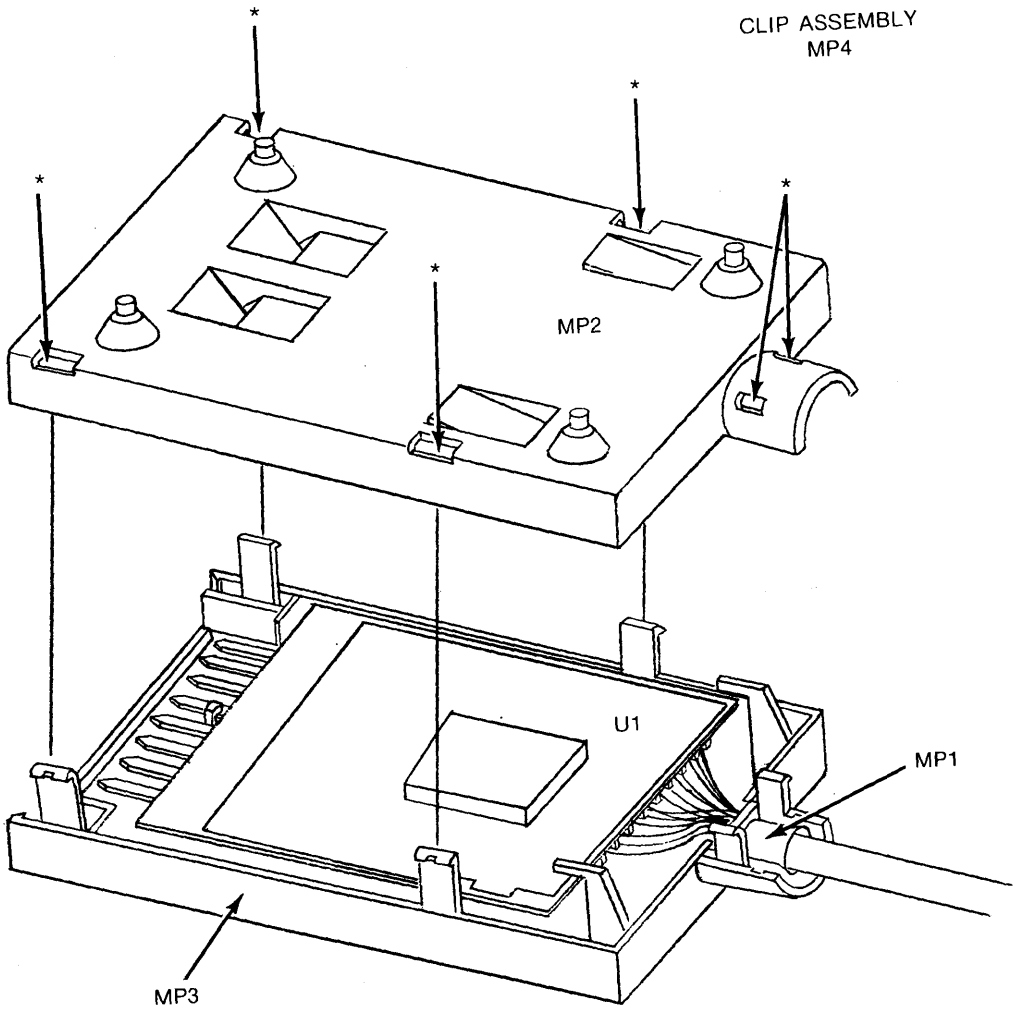
8-16. Macrocell Installation

a. Place the macrocell chip (circuit side down) in the socket. The socket is keyed so that the macrocell chip will fit only one way.

b. Put a thin coating of thermal compound on the back of the macrocell chip.

c. Place the two small guide pins on the heatsink into the socket. The heatsink is keyed so it fits only one way.

d. Gently push down on the heatsink and flip the socket retaining clip up and over the large heatsink guide pins.



*INSERT TOOTHPICKS AT THESE POINTS

Figure 8-18.

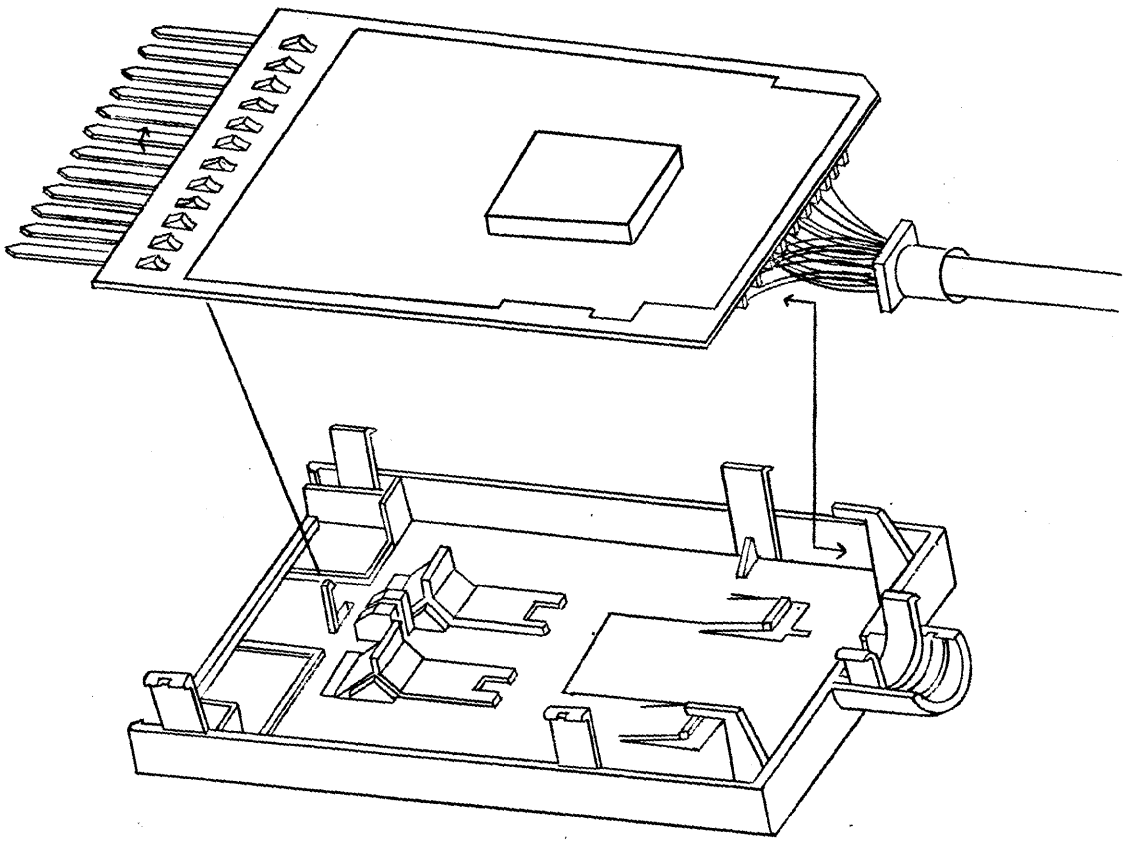


Figure 8-19.

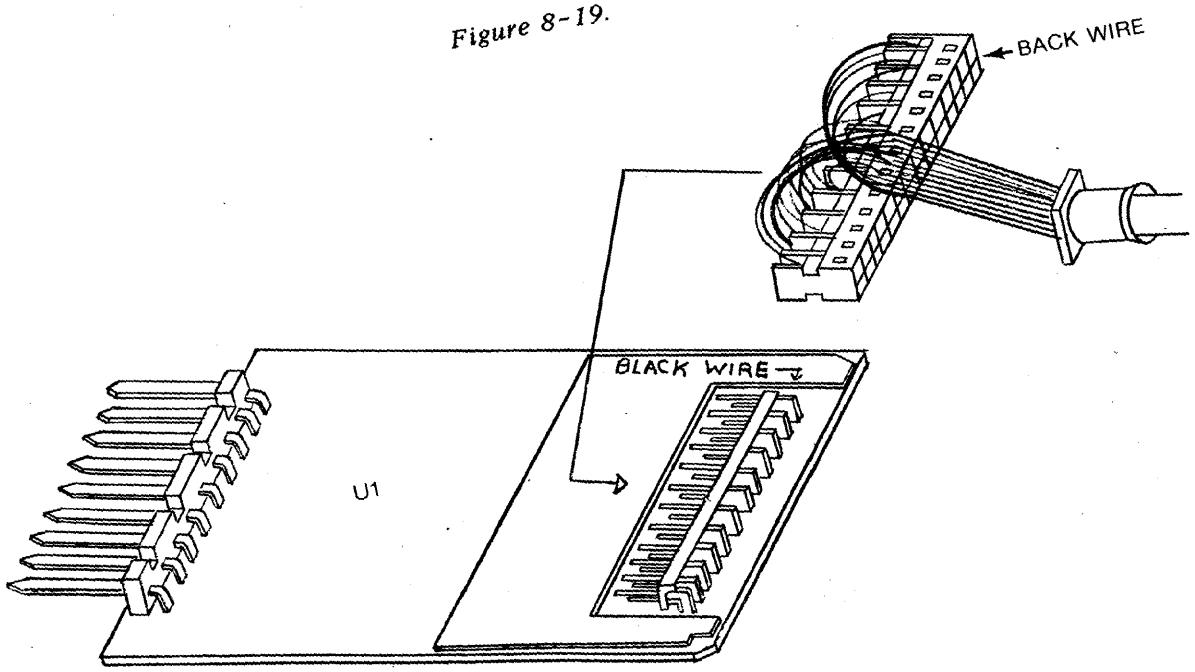


Figure 8-20.

Service Group 8A Table of Contents

List of Illustrations

List of Tables

SERVICE GROUP 8A
POWER SUPPLY AND MOTHERBOARD

8A-1. INTRODUCTION

This Service Group contains block and component level theory, troubleshooting and schematic information necessary to service the 1630A/D/G power supply and motherboard. Service group 8A is separated into two sections: theory and troubleshooting.

8A-2. SAFETY CONSIDERATIONS

Several parts of the power supply have lethal voltage and current potentials associated with them. Primary filter capacitors C10 and C11 are very large and have 300 volts across them, + or - 150 Vdc to ground. This provides a great deal of potential energy. With their respective bleeders R4 and R5, the discharge time constant is 60 seconds so even with the supply turned OFF it can be dangerous! Therefore, wait at least three minutes for the supply to discharge before servicing.

8A-3. SPECIFICATIONS

The power supply used in the 1630A/D/G is a switching power supply that converts the AC line input to six regulated DC voltages. Table 8A-1 contains individual specifications for each voltage.

Table 8A-1. Power Supply Specifications

INPUT

115 volt range: 90 to 127 VAC Input Imax = 4 Amps
230 volt range: 180 to 253 VAC Input Imax = 2 Amps
Frequency Range: 48 to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
+15	5	0.8
+12	5	0.25
+5	5	6.0
-2.4	1	8.0
-5.2	-5, +10	25.0
-12	5	0.25

8A-4. POWER SUPPLY BLOCK DIAGRAM (see Figure 8A-1)

The 1630A/D/G power supply is separated into three basic sections; Primary, Control and Secondary. The following is a brief outline of each section.

PRIMARY SECTION. The primary section is responsible for providing a rectified and conditioned switching source of approximately plus and minus 150 VDC, along with transformation for control power. The primary section also provides protection to the supply from AC input surge current and overvoltage conditions. This section also drives the internal cooling fan.

CONTROL SECTION. Control voltage generation, modulation and switching are the main functions of the control section. However, LED failure indication and failure execution is also a function of this section.

SECONDARY SECTION. The secondary section is responsible for filtering, rectification and feedback for the DC power supplies. Also, this section outputs all of the supplies to the test connector and the motherboard.

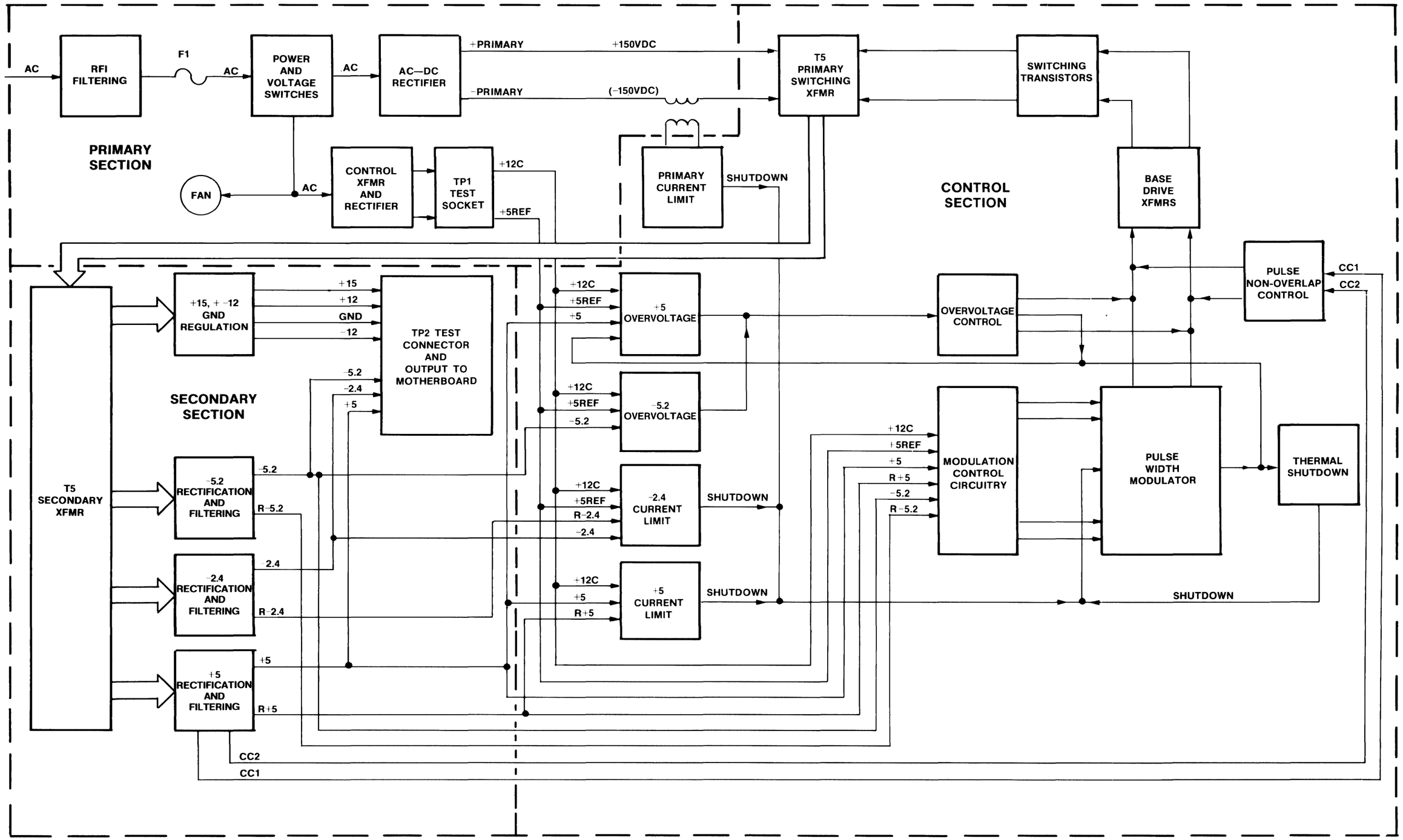


Figure 8A-1. Power Supply Block Diagram

NOTES

8A-5. POWER SUPPLY THEORY OF OPERATION

The theory of operation gives detailed operation of the circuitry on the power supply board. Refer to power supply schematic figure 8A-6 while reading.

8A-6. Primary Section

The power supply begins operation when the power switch (SW2) is turned ON providing AC line to FL1 which filters the AC for radio frequency interference (RFI). According to the setting of the line select switch (SW1), the primary section will operate in two modes, either 115 VAC or 230 VAC.

8A-7. 115 VAC OPERATION. Notice the way that the neutral line is wired to the primary output of the bridge rectifier (CR4), only two of the diodes of CR4 are used. These are the two that connect to the AC line input of CR4. This configuration produces ~300 V across the + and - ouputs of CR4. During the 115 VAC mode this circuitry forms a half wave voltage doubler. Furthermore, while in the 115 VAC mode the primaries of T1 are in parallel so there is 115 VAC across each primary. The outputs of T1 are in parallel and have the same voltage across them during either the 115 or 230 VAC modes.

8A-8. 230 VAC OPERATION. When SW1 is in the 230 VAC mode, all four diodes in the bridge rectifier (CR4) are used. However, the voltage across the + and - outputs of CR4 is still ~300 V. During the 230 VAC mode this circuitry forms a full wave rectifier. While in the 230 VAC mode the primary inputs of T1 will be in series and still have 230 VAC across each primary winding.

The fan, in either the 115 VAC or 230 VAC mode will always have 115 VAC driving it. The varistors RV1 and RV2 on the primary side of T1 are for transient suppression. The thermistor, RT3, provides surge current protection for CR4.

8A-9. SURGE CURRENT PROTECTION. Because input filter capacitors C10 and C11 are connected directly across the rectified line, a form of surge current protection is provided to limit line surges during turn on. RT3 provides this protection.

8A-10. OVERVOLT PROTECTION. During an AC overvolt situation E1, E2, RT1, RT2 provide protection to the supply. When the neon bulbs (E1 and E2) reach their maximum voltage limit (~240 V), they drop to a low impedance and draw current through the thermistors (RT1 and RT2) and discharge C10 and C11. Note that due to a thermistor's high negative temperature coefficient of resistance, a thermistor presents a fairly high resistance when cold (during turn on) and a very low resistance when hot.

NOTE: This circuitry has been removed on later instruments. Please see the appropriate Service note at the back of this manual.

8A-11. RFI SUPPRESSION. RFI is generated by unwanted frequency energy caused by the switching components in the power supply. Inductors L2 (balun) and L1 prevent this radio frequency interference from being conducted back into the AC line.

8A-12. Control Section

The control section mainly consists of the circuitry needed to control the operation of the pulse width modulator (PWM). Also covered is the error detection and execution circuitry needed to control modulation.

8A-13. PWM OVERVIEW (see Figure 8A-2). A pulse width modulator (PWM) requires four signals for proper modulation: a reference voltage, a feedback from the output to compare with the reference voltage for error detection, feedback current from the output for output current limiting, and a predetermined switching frequency.

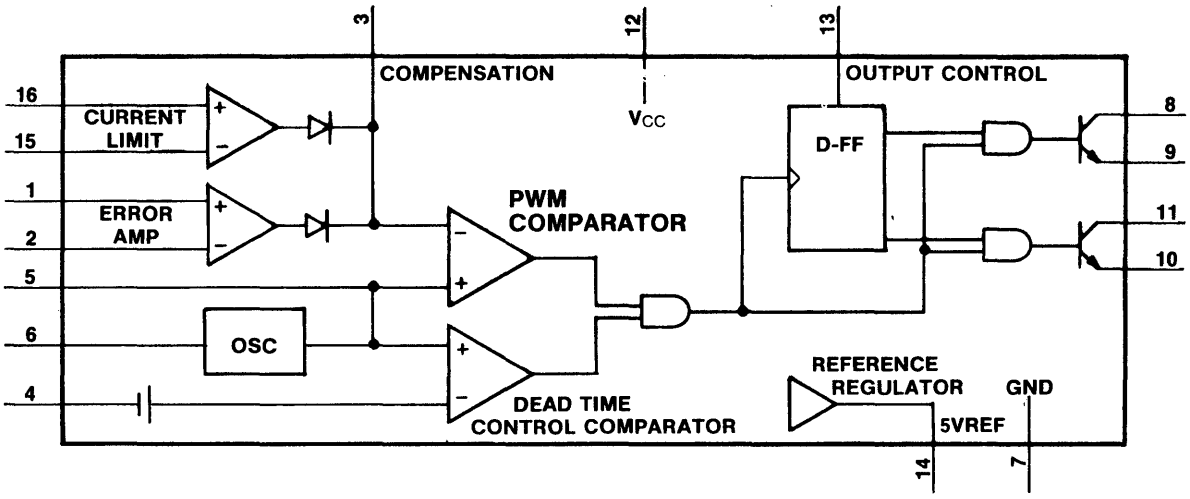


Figure 8A-2. Functional Block Diagram of a PWM

A PWM modulates it's output transistors pulse width (ON time) according to the demands of the system. In this manner it controls the amount of current each switching transistor delivers and therefore controls the power. The PWM configuration used by this supply is for push-pull modulation. Push-pull modulation means that each internal open collector output transistor is turned ON alternately by the pulse-steering flip-flop. This configuration is determined by the output control input (OC) pin 13 being tied to the PWM's internal 5V reference regulator, pin 14.

8A-14. MODULATION CONTROL. If the +5V feedback voltage at pin 1, U5, is higher than the reference voltage at pin 2, the PWM determines that the output voltage is too high. It then reduces its output transistors pulse widths to within limits.

8A-15. PWM SOFT START. When AC is switched ON, capacitor C21 has not charged. This forces the dead-time control input, pin 4 of U5, to follow the 5V reference regulator output, pin 14. Note, when dead-time is high, both outputs are disabled (100% dead-time). While C21 is charging through RP2 (pins 5 and 6), the cutput pulse widths are allowed to modulate slowly until dead-time is low and 100% modulation is allowed. Soft start is used to prevent large current surges which may occur on power up. Also, a soft start prevents a false signal, possibly created by the control circuitry, from resetting the PWM during power up.

8A-16. PWM SWITCHING FREQUENCY. The 42 KHz internal oscillation frequency of the PWM is determined by the RC time constant of R21 and C22 connected to pins 6 and 5 of U5. Therefore, each open collector output transistor (pins 8 and 11) is turning ON and OFF alternately at about 21 KHz.

8A-17. CURRENT SWITCHING OPERATION (see figure 8A-6). The open collector outputs, pins 11 and 8 of U5, are complementary and non-overlapping. For zero on-time (zero modulation time), both outputs are high. As demand increases, each output stays low (at different times, non-overlapping) for a longer period until one is going high as the other is going low or until one of the feedback signals limits the pulse duration. Each output is inverted through U2F,G, another open collector device, and alternately causes changing current through the primaries of T2 and T3. These transformers alternately turn Q1 and Q2 ON and OFF which causes the current in the primary of T5 to alternate.

The signals CC1 and CC2 (from U2B,C) prevent or delay the switching of Q1 and Q2. For example, suppose the following condition exists. The power supply is experiencing a heavy demand and must allow close to 100% modulation to meet it. Q1 has turned ON per the request of the PWM and has pulled the one node of T5 to the + primary voltage. Then the PWM tells Q1 to turn OFF and Q2 to turn ON. Q2 can turn ON immediately, but Q1 cannot turn OFF that quickly because of charge storage. The CC2 signal is a feedback signal from the secondary of T5 senses this condition and and will not allow Q2 to turn ON until Q1 turns OFF and the voltage on the secondary of T5 stabilizes. To allow Q2 to turn ON sooner would have the effect of shorting the + primary voltage to the - primary voltage for a short period of time (an enormous waste of power not to mention damage to components).

8A-18. Control Power Supply

As soon as AC is switched ON, CR1 rectifies AC and starts charging C3, a ripple filter for the 12 volt regulator VR1. The output of VR1 lags the input by about 1 V on power up until it stabilizes at +12 V. VR1 is the power supply for +12C (a control power supply used only on the power supply board). +12C supplies U1 which is the +5 reference source (+5REF).

8A-19. PWM Failure Modes

8A-20. PWM FAILURE EXECUTION. There are seven failure execution circuits in the 1630A/D/G power supply. One of these failures, -5.2 current limit, affects the current limit input, U5 pins 15 and 16, of the PWM. Four of the failures affect the Compensation/PWM Comparator input (COMP) pin 3, U5. The COMP input must be allowed to float during normal operation. If an error occurs with the +5 or -2.4 current limit, primary current limit, or thermal shutdown pin 3 will be pulled high and the PWMs' output transistors will be shut OFF. Two of the failures, +5 and -5.2 overvoltage act directly on the drive lines to the Primary Base Drive Transformers.

Several of these failures have LED indicators which indicate the nature of the failure.

8A-21. PWM CURRENT LIMITING. This power supply uses fold-back current limiting. The actual current limit value is determined by sensing the DC voltage developed across the internal resistance of T6 pins 2,11 and 3,10 (T6 contains six internal inductors). Current limiting of the -5.2V supply works by developing a voltage across C20 that is equivalent to the maximum load current times the internal resistance of T6 pins 2,11 and 3,10. The voltage across C20 is then compared to the reference voltage at pin 15 of U5. The foldback of the maximum current limit value is determined by the decrease in the voltage across R17. When the voltage across R17 decreases, the voltage required across C20 also decreases. The decrease across C20 causes the PWMs internal comparator to go more positive and reduce modulation until the -5.2 output voltage across R16 increases, allowing C20 to charge to the value of the reference voltage. See figure 8A-3 below.

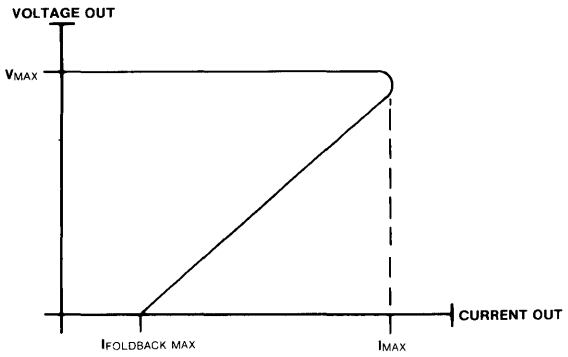


Figure 8A-3. Foldback Current Limiting

8A-22. +5 CURRENT LIMIT. This circuit also operates similarly to the PWM except: the DC component is taken from T6 pins 1 and 12; C43 sets the current limit value; R36 sets the foldback limit; and P/O RP3 pins 4 and 3 adjust the foldback limit. When current limit occurs, pin 14 of U6D goes high and biases CR17, which makes pin 3 of U5 more positive and reduces modulation.

8A-23. -2.4 CURRENT LIMIT. This circuit operates similarly to the PWM except: the DC component is taken from T6 pins 4 and 9; C45 sets the current limit value; P/O RP3 pins 5 and 6 set the foldback limit; and R40 adjusts the foldback limit. When a current limit occurs, pin 8 of U6C goes high and biases CR16, which makes pin 3 of U5 more positive and reduces modulation.

8A-24. U3 AND U4 OPERATION. U3 and U4 are overvoltage sensors. U3 and U4 will turn ON LEDs if an error condition is detected, and both will generate SHUTDOWN. U3 and U4 work in the following manner. When the voltage at pin 2 exceeds the voltage at pin 7 by 2.6 volts, the output pin 8 latches high to turn ON the failure LED and generate SHUTDOWN. The capacitor on pin 3 and pin 4 of U3 and U4 determine the minimum amount of time that an error must exist before they turn ON, thus providing transient protection.

8A-25. PRIMARY CURRENT LIMIT. U4 detects an error via T4. The primary side of T4 is in the return loop of the minus primary voltage for the switching transistors. The change of current through the primary of T4 establishes a voltage drop in the secondary, rectified by CR10, divided by R14 and R15, and detected at pin 2 of U4. If the voltage at pin 2 of U4 is greater than 2.6 volts, (a slight delay is provided by C19), U4 latches and turns ON the primary current limit LED "PL" and sets SHUTDOWN high which turns OFF U5.

8A-26. THERMAL SHUTDOWN. The circuitry for U3 detects an over temperature condition and generates SHUTDOWN. A normally closed thermal switch (SW3) is mounted on heatsink MP9. When the heatsink exceeds 105 C, the thermal switch opens and U3 detects an error. When pin 8 latches high, the thermal shutdown LED "TH" is turned ON. Then SHUTDOWN is generated and U5 is turned OFF.

8A-27. +5 OVERVOLTAGE. An overvoltage failure occurs when the +5 volt supply exceeds 6 volts making the voltage at pin 3 of U6A greater then the 5V reference on pin 2. This in turn makes pin 1 of U6A go high forcing two operations to occur. The first operation biases CR13 which keeps pin 3 of U6A high regardless of the overvolt condition. The second operation biases CR11, thus making the outputs of U2A, U2D and U2E low. With U2E low, the "OV" (overvoltage) LED (P/O DS1) goes ON indicating an overvoltage failure. Furthermore, with U2A and U2D low, U2F and U2G are be unable to deliver a switching frequency to the base drive transformers. This turns OFF the supplies. Note, that if an overvoltage failure occurs, the power must be cycled OFF/ON in order to reset the overvoltage circuitry.

8A-28. -5.2 OVERVOLTAGE. Except for polarity considerations, the -5.2 overvoltage circuitry operates the same as the +5 overvoltage circuit. This circuit turns OFF at -6.2 volts.

8A-29. Secondary Section

8A-30. +5, -5.2, AND -2.4 SECONDARIES. Three of the four switching supply secondaries operate relatively the same. The +5 supply will be used as an example of their operation.

The alternating voltage in the center tapped secondary of T5 is full wave rectified by two Schottky diodes (CR20) mounted on a heatsink (MP9). The R27/C28 combination is a snubber network that limits the dv/dt to protect the diodes. CC1 and CC2 (cross conduction 1 and 2) prevent both switching transistors from being ON at the same time and shorting the + and - primary voltages together. P/O T6 and C49 are the filter for the supply. The LED "NORM" being ON indicates that the supply is operating properly.

Except for polarity and the lack of an LED indicator, the -2.4 and -5.2 supplies are the same as the +5 supply.

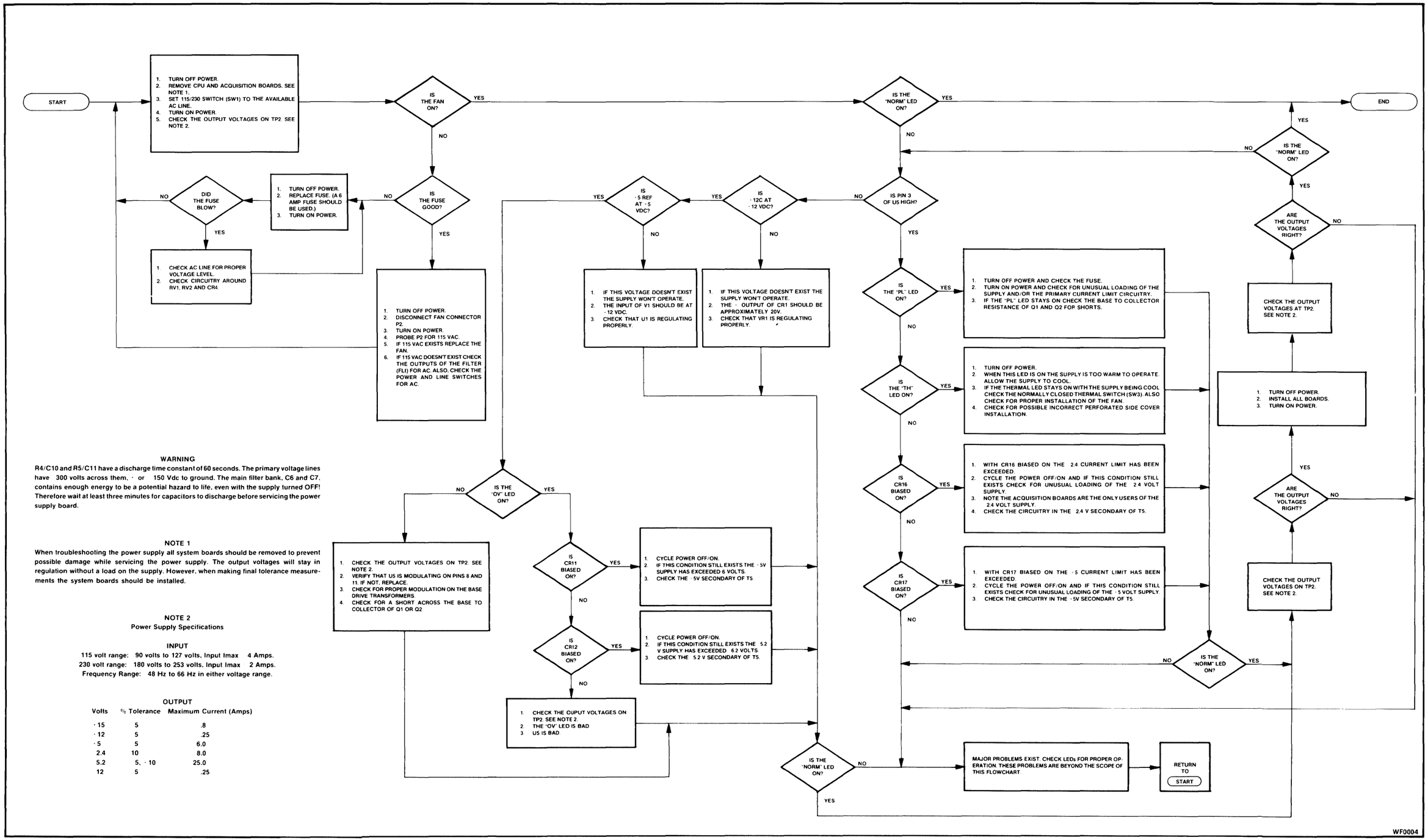
8A-31. +15, +12, AND -12 SECONDARIES. The alternating voltage of T5 is full wave rectified by CR15. R24 and C23 form a snubber network to protect CR15. P/O T6, C25 and C26 filter the outputs of CR15 before they are regulated by VR2, VR3 and VR4. The outputs of the regulators are filtered by C29-31 before the +15, +12 and -12 voltages are supplied to the motherboard.

8A-32. LED FAILURE INDICATIONS

Figure 8A-4 is a flow chart that guides the user to the faulty circuit(s) indicated by a power supply failure LED.

8A-33. MOTHERBOARD INFORMATION

The motherboard connects and distributes all of the signals from the power supply, CPU, and State and Timing boards. Figure 8A-7 is a component locator for the parts on the motherboard. Table 8A-3 gives the motherboard connections and instrument signal distribution.



WARNING

R4/C10 and R5/C11 have a discharge time constant of 60 seconds. The primary voltage lines have 300 volts across them, - or 150 Vdc to ground. The main filter bank, C6 and C7, contains enough energy to be a potential hazard to life, even with the supply turned OFF! Therefore wait at least three minutes for capacitors to discharge before servicing the power supply board.

NOTE 1

When troubleshooting the power supply all system boards should be removed to prevent possible damage while servicing the power supply. The output voltages will stay in regulation without a load on the supply. However, when making final tolerance measurements the system boards should be installed.

NOTE 2

Power Supply Specifications

INPUT

115 volt range: 90 volts to 127 volts, Input Imax 4 Amps.
230 volt range: 180 volts to 253 volts, Input Imax 2 Amps.
Frequency Range: 48 Hz to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
-15	5	.8
-12	5	.25
-5	5	6.0
2.4	10	8.0
5.2	5, -10	25.0
12	5	.25

Figure 8A-4. Troubleshooting Flow Chart For LED Failure Indicators

NOTES

8A-34. MNEMONICS

Signals on the 1630A/D/G power supply board have been assigned mnemonics that describe the function of the signal (see table 8-1. Logic Symbols). A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. An "H" prefix indicates that the function is active in the "high" state; an "L" prefix indicates that the function is active in the "low" state. The following table is a listing of the mnemonics used on the schematic.

Table 8A-2. Mnemonics

Mnemonic	Description
+12C	+12 V Control. This is the control voltage used throughout the supply. If +12C is not in regulation, the supply will not operate properly.
CC1,2	Cross Conduction 1 and 2. Complementary signals used to prevent both switching transistors from being ON at the same time.
NORM	Normal. When this LED is ON, the power supply is working correctly.
OV	Over Voltage. When this LED is ON, either the +5 or -5.2 volt supply has exceeded its voltage limits. When asserted, the PWM U5 will be shut OFF.
PL	Primary Limit. When this LED is ON, a non-linear surge in current has occurred in the primary section. When asserted, the PWM U5 will be shut OFF.
PWM5VREF	Pulse Width Modulator 5 V Reference. A +5 volt reference from U5's internal reference regulator.
R+5	Return +5. The voltage on this line is the DC component of the +5 volt supply. It is used to set the current foldback limit of the +5 current limit circuit.
R-2.4	Return -2.4. The voltage on this line is the DC component of the -2.4 volt supply. It is used to set the current foldback limit of the -2.4 current limit circuit.
R-5.2	Return -5.2. The voltage on this line is the DC component of the -5.2 volt supply. It is used by the PWM U5 to set the foldback current limit of the -5.2 volt supply.
SHUTDOWN	This signal is generated in several places and is responsible for turning OFF the PWM U5 by pulling pin 3 high.
TH	Thermal. Thermal switch SW3 opens when the internal temperature of the supply is greater than 105 degrees C. When the TH LED is ON, PWM U5 is turned OFF.

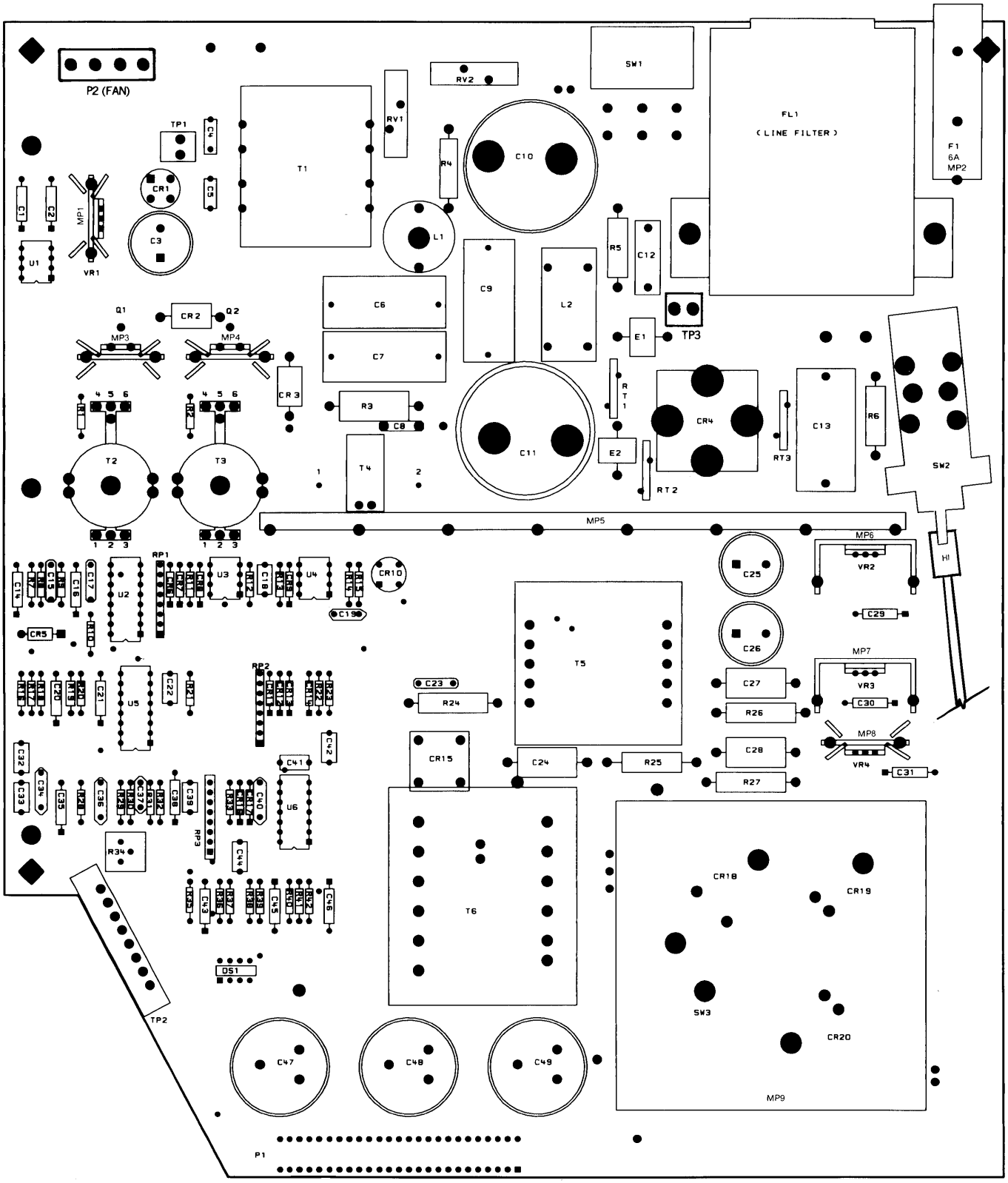
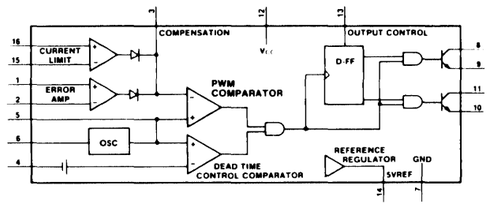


Figure 8A-5. Power Supply Component Locator

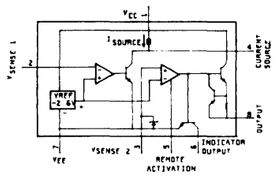
NOTE 1

FUNCTIONAL DIAGRAM FOR U5
1826-0565 TL494



NOTE 2

FUNCTIONAL DIAGRAM FOR U3 AND U4
1826-0468

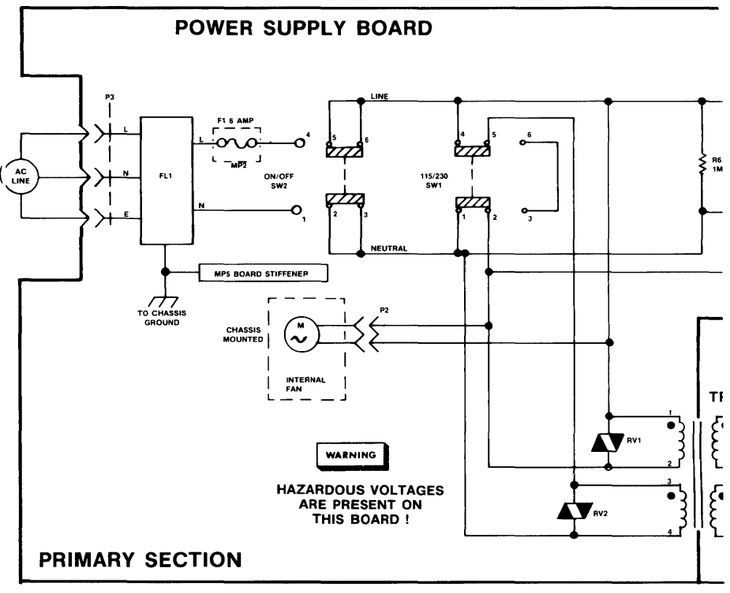


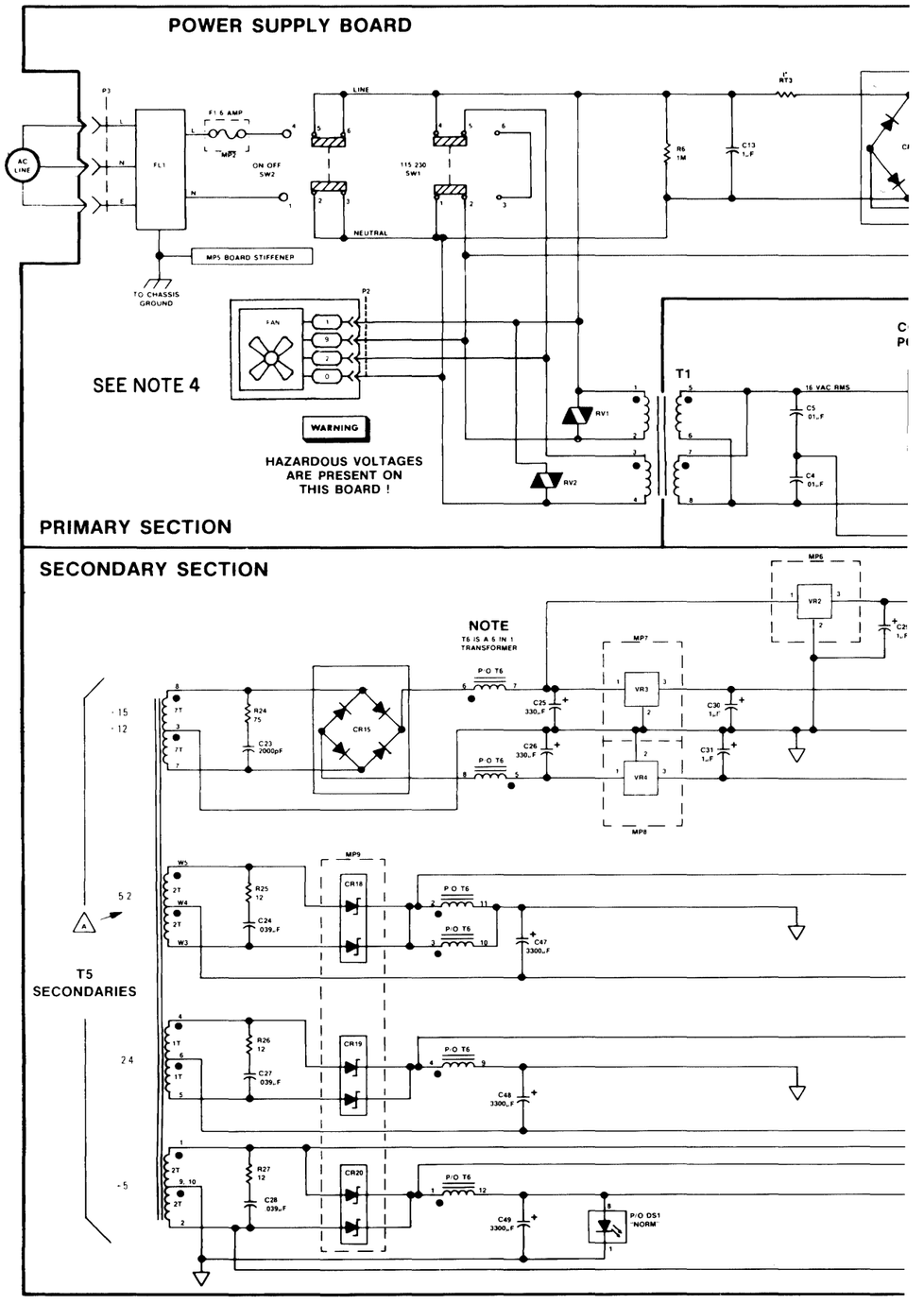
NOTE 3

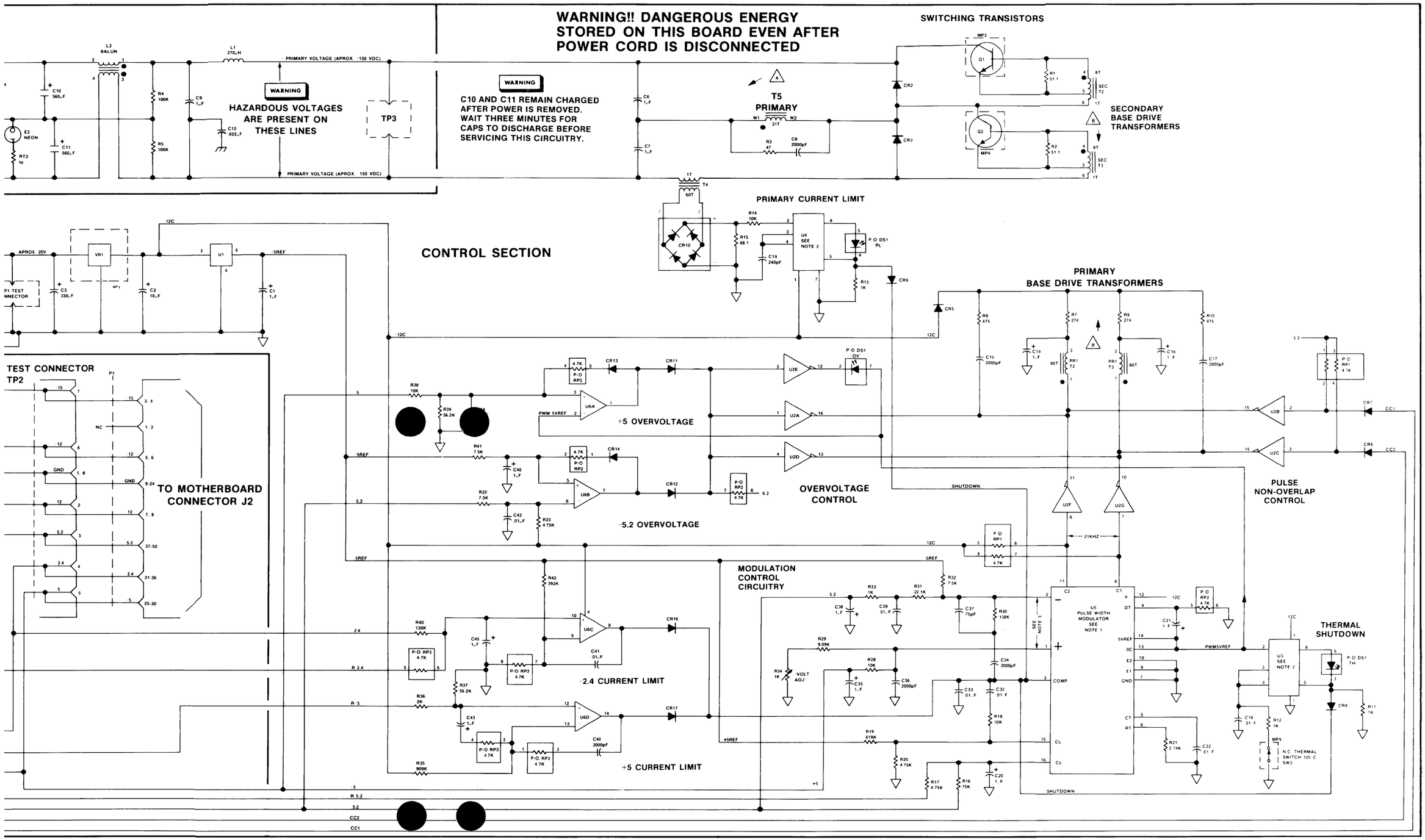
PROBING THESE PINS MAY CAUSE UNWANTED SYMPTOMS.

NOTE 4

BELOW IS THE 120V FAN CIRCUIT USED IN SERIAL PREFIXES BEFORE 2412A.







8A-1

Figure 8A-6. Power Supply Schematic

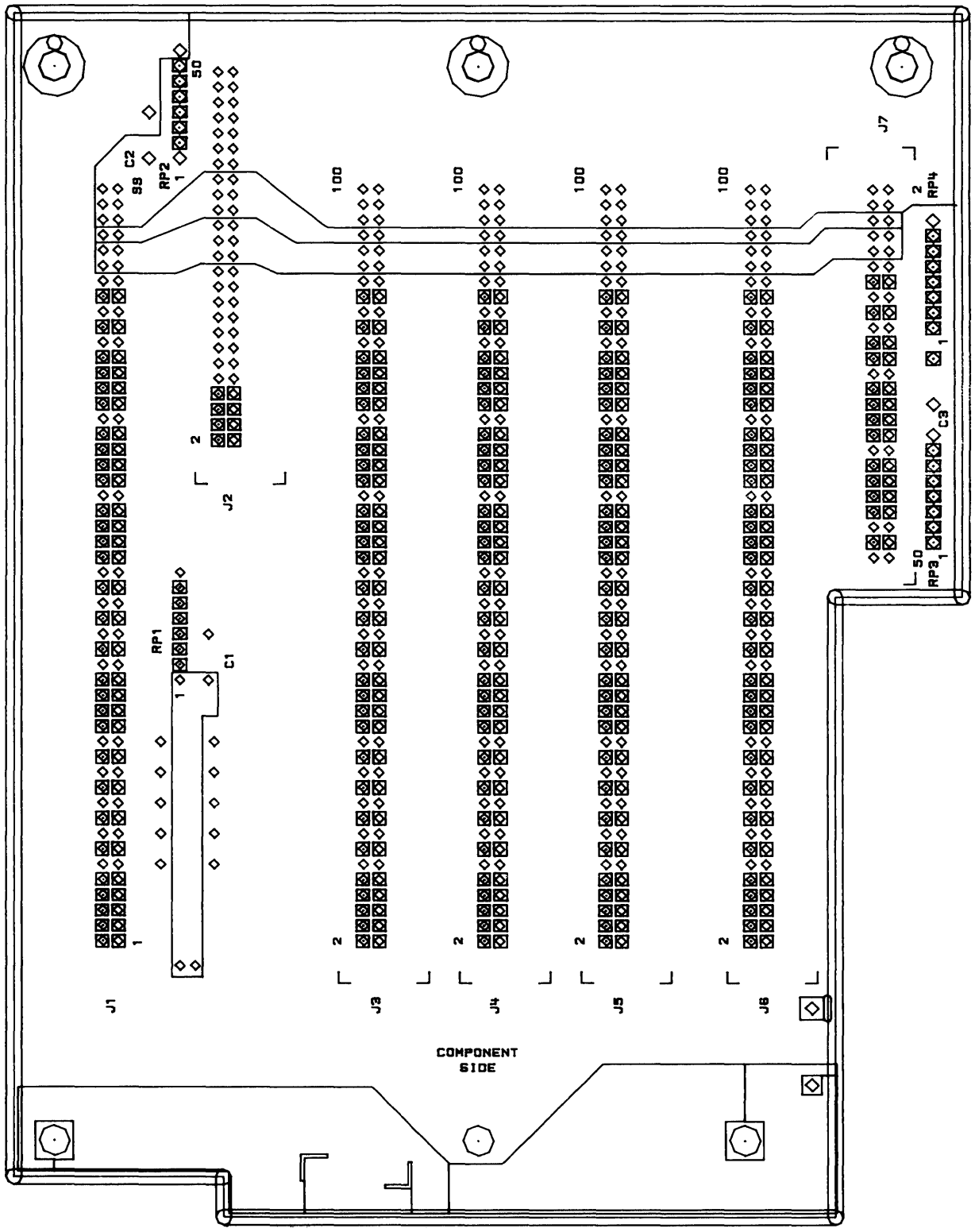


Figure 8A-7. Motherboard Component Locator

Table 8A-3. Motherboard Connections & Signal Distribution.

MOTHERBOARD CONNECTIONS & SIGNAL DISTRIBUTION							
SIGNAL	PIN	CPU J6	STATE MASTER J5	TIMING MASTER J4	TIMING SLAVE J3	STATE SLAVE J3	TERM LOCATION (NOTE 3)
GS4	1	B-7	[C-1]				
THR4	2	[B-7]	C-1				
GS3	3	B-7	[C-1]				
THR3	4	[B-7]	C-1				
GS2	5	B-7		[D-1]			
THR2	6	[B-7]		D-1			
GS0	7	B-7			[E-1]		
THR0	8	[B-7]			E-1		
GS1	9	B-7				[F-1]	
THR1	10	[B-7]				F-1	
GND	11,12						
NOT USED	13						
NOT USED	14						
GND	15,16						
HGS	17	NC	NC	D-2	[E-1]		
LTS	18	NC	NC	D-2	[E-1]		
GND	19,20						
HSWS	21	NC	[C-7]		E-2	F-3	F-3
HSWM	22	NC	[C-7]	D-4			
GND	23,24						
HSCS	25	NC	[C-6]		E-1	F-3	F-3
HSCM	26	NC	[C-6]	D-1			
GND	27,28						
LDS	29	NC	C-3		[E-1]	[F-2]	C-3
LDM	30	NC	C-3	[D-1]			C-3
LCS	31	NC	C-3		[E-1]	[F-2]	C-3
LCM	32	NC	C-3	[D-1]			C-3
LBS	33	NC	C-3		[E-1]	[F-2]	C-3
LBM	34	NC	C-3	[D-1]			C-3
LAS	35	NC	C-3		[E-1]	[F-2]	C-3
LAM	36	NC	C-3	[D-1]			C-3
GND	37,38						
LSTP	39	NC	NC	[D-4]	E-2		
HSQ3	40	B-1	[C-4]				1-3,3-2
GND	41,42						
LTCK	43	[B-1]		[D-3]	E-2		1-5,3-4
HTCK	44	[B-1]		[D-3]	E-2		1-4,3-3
GND	45,46						
HACK	47	[B-1]		[D-3]		F-3	1-7,3-6
LACK	48	[B-1]		[D-3]		F-3	1-6,3-5
GND	49,50						

NOTES: 1) ALL PINS OF CONNECTORS J1 (SERVICE CONNECTOR), AND J3 THRU J6 ARE BUSED TOGETHER, WITH THE EXCEPTION OF THOSE MARKED "NC".
2) X-X (LETTER-NUMBER) INDICATES THE SECTION (BOARD) AND SCHEMATIC THAT A SIGNAL IS FOUND, WITH [] INDICATING THE SOURCE OF THE SIGNAL.
3) TERMINATION LOCATION SHOWS WHERE A SIGNAL IS PULLED LOW (ECL) WITH X-X (LETTER-#) GIVING SCHEMATIC AND (#-#) GIVING MOTHERBOARD RP# AND PIN#.

Table 8A-3. Motherboard Connections & Signal Distribution (cont.).

SIGNAL	PIN	CPU J6	STATE MASTER J5	TIMING MASTER J4	TIMING SLAVE J3	STATE SLAVE J3	TERM LOCATION (NOTE 3)
HD7	51	[B-2]	C-8	D-5	E-2	F-5	B-2
HD6	52	↑	↑	↑	↑	↑	↑
HD5	53	↕	↕	↕	↕	↕	↕
HD4	54	↕	↕	↕	↕	↕	↕
HD3	55	↕	↕	↕	↕	↕	↕
HD2	56	↕	↕	↕	↕	↕	↕
HD1	57	↕	↕	↕	↕	↕	↕
HD0	58	[B-2]	C-8	D-5	E-2	F-5	B-2
GND	59,60						
HA5	61	[B-2]	C-8	D-5	E-2	F-5	B-2
HA4	62	↑	↑	↑	↑	↑	↑
HA3	63	↕	↕	↕	↕	↕	↕
HA2	64	↕	↕	↕	↕	↕	↕
HA1	65	↕	↕	↕	↕	↕	↕
HA0	66	[B-2]	C-8	D-5	E-2	F-5	B-2
HR/LW	67	[B-2]	C-8	D-5	E-2		
NOT USED	68						
GND	69,70						
NOT USED	71						
NOT USED	72						
+15	73	B-1					
+15	74	B-1					
+12	75	B-1				F-4	
+12	76	B-1				F-4	
-12	77	B-1				F-4	
-12	78	B-1				F-4	
GND	79,80						
LSTB	81	[B-2]	C-8	D-5	E-2	F-3	2-5,4-3
LMCI	82	B-6	[C-4]	[D-2]			2-6,4-2
GND	83,84						
HARM	85		C-4	D-1			2-2,4-5
HBNC	86	B-7	[C-4]	[D-2]			2-3,4-4
GND	87,88						
+5	89,90	B-1	C-8	D-5	E-1	F-4	
+5	91,92	↑	↑	↑	↑	↑	
-2.4	93,94	↕	↕	↕	↕	↕	
-5.2	95,96	↕	↕	↕	↕	↕	
-5.2	97,98	↕	↕	↕	↕	↕	
-5.2	99,100	B-1	C-8	D-5	E-1	F-4	

NOTES: 1) ALL PINS OF CONNECTORS J1 (SERVICE CONNECTOR), AND J3 THRU J6 ARE BUSED TOGETHER, WITH THE EXCEPTION OF THOSE MARKED "NC".

2) X-X (LETTER-NUMBER) INDICATES THE SECTION (BOARD) AND SCHEMATIC THAT A SIGNAL IS FOUND, WITH [] INDICATING THE SOURCE OF THE SIGNAL.

3) TERMINATION LOCATION SHOWS WHERE A SIGNAL IS PULLED LOW (ECL) WITH X-X (LETTER-#) GIVING SCHEMATIC AND (#-#) GIVING MOTHERBOARD RP# AND PIN#.

Service Group 8B Table of Contents

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SERVICE GROUP 8B
CPU, KEYBOARD, AND DISPLAY

8B-1. INTRODUCTION

This service group contains block and component level theory, service and troubleshooting information necessary to service the CPU and keyboard. Service group 8B is separated into two sections; theory and troubleshooting.

The Display System used by the 1630A/D/G is an OEM assembly and is not serviced by HP. The Display Driver, yoke, and CRT are each given a separate HP part number and should be ordered that way. The DISPLAY SYSTEM OPERATION VERIFICATION AND TROUBLESHOOTING section of this Service Group will aid the service person in determining whether or not the Display System or the CPU system is failing.

Note, the terms MPU and processor will be used throughout this manual in reference to the MC68B09E MICROPROCESSOR used on the CPU board.

8B-2. BLOCK DIAGRAM THEORY (see Figure 8B-1)

The block theory for service group 8B is focused at the CPU board because the control circuitry for the keyboard and display board is located on the CPU board. The order in which each block is described is also the order that each block is functionally described in the detailed theory of operation.

CONTROL TIMING. The control timing section provides the CPU board with fifteen timing waveforms. Each waveform and its complement has a frequency of 1.27 MHz and the delay between each adjacent phase group is 50 nS. For example PH1N and PH1 lead PH2N and PH2 by 50 nS.

SYSTEM TIMING CONTROLLER. The system timing controller (STC) is a processor programmable timer. It also provides a 2 MHz clock for the HP-IL controller, synchronization for a real-time clock, measurement time for the acquisition system, and a signal source for an audio feedback speaker.

CONTROL LATCHES. The processor uses these latches to control and/or enable eleven functions on the CPU board.

MICROPROCESSOR UNIT (MPU). The processor uses the 8-bit bi-directional data bus HDRW0-7 to communicate with and control devices in this system. Addresses A11-15 are used to select tasks from the Memory Management Unit (MMU). Physical Addresses 0-10 (HPA0-10) combine with addresses HPA11-20 from the MMU to form the Physical Address bus. Clocking of the MPU E and Q clock inputs is provided by the Control Timing Section.

MEMORY MANAGEMENT UNIT (MMU). Expanding the 64K addressable space of the processor, write protection, mapping and allocation of memory are some of the functions of the MMU. The MMU, controlled by the processor, outputs the Physical Addresses 11-20.

ACQUISITION ADDRESS INTERFACE. The processor uses this block to convert TTL logic address and control information into ECL logic for the all-ECL acquisition boards.

ACQUISITION DATA INTERFACE. In order for the processor to send data to or from the ECL logic aquisition boards, the data must be converted from TTL-to-ECL, or from ECL-to-TTL. This block also forms the 8-bit write only data bus labeled HDW0-7.

POWER UP MASTER RESET. The purpose of this block is to keep certain key devices on the CPU board OFF while the power supply is turning ON. Different reset logic levels are provided.

FULL-FIELD SCANNING GENERATION AND GRAPHICS MUX. This block provides the X and Y scanning information for RAM when graphics information is required in the full-field graphics area of the display. Also, RAM refresh is provided during retrace.

WAVEFORM FORMATTER. The purpose of the Waveform Formatter circuitry is to sample state and/or timing data and convert it into waveform information. The data is sampled for a high or low level, an edge, or a glitch. The information or symbols that make a waveform are then displayed in the full-field graphics area via RAM and the graphics buffer.

ROM AND ROM SELECTION. The eight 8K word x 8 bit ROMs used by this system are each selected by an addressable 1 of 8 demultiplexer.

MPU ADDRESS MULTIPLEXER. This block multiplexes the first 16 Physical Addresses into 8 RAM address lines HRAA0-7. This allows the processor to address RAM during the proper processor cycle.

RAM TIMING CONTROL. This block generates the timing signals (LCAS and LRAS) necessary to read and write from RAM. The Address Multiplexer Select (AMS) signal allows one group of devices, either MPU, graphics, or CRT controller, to address RAM at a given time. Also generated is a 20 MHz clock used to clock control timing, the display data shift register and display data latches.

RAM. The CPU board uses eight 64K word x 1 bit dynamic RAMs. RAM is addressed by three groups of devices (MPU, Graphics, or CRTC) during a processor cycle time. The data from the eight RAM data lines (HRAD0-7) is used by the CRT Controller (CRTC), Character ROM, and graphics buffer.

CRT CONTROLLER (CRTC) AND CRT CONTROL MUX. The CRTC is the interface between the Display System and the processor. Controlling CRT scanning, retrace execution, and cursor positioning are some of the functions of the CRTC. Like the MPU, and the full-field scanning generator the CRTC is only allowed to address RAM at the proper time in a processor cycle. This is determined by the ON time of the CRT control multiplexers.

CHARACTER ROM. The Character ROM converts the ASCII code for a given character into the 9 x 16 dot pattern used by this system to display characters. The data output is loaded into the display data shift register where it is serialized and sent to the display.

DISPLAY DATA SHIFT REGISTER AND DISPLAY DATA LATCHES. This block takes parallel display information from the character ROM and the graphics buffer. The information is converted into a serial data stream and mixed with cursor and video brightness information. This data is then captured by the display data latches and supplied as video information to the display driver.

GRAPHICS OUTPUT BUFFER. The graphics output buffer routes graphics information from the waveform formatter (via RAM) into the display data shift register. When scanning of the full-field graphics area is occurring this circuit will be ON and the character ROM will be OFF.

DISPLAY CONTROL. Video brightness, cursor timing, and enabling and disabling of the character ROM and graphics output buffer are the functions of this block.

I/O DECODING. Input/output operations function in two separate levels according the amount of memory reserved to execute an I/O operation; these are macro and micro. A macro operation reserves thirty-two Physical Addresses to execute an I/O operation and a micro operation reserves two or less Physical Addresses. This circuit controls read and write operations of I/O devices.

INTERRUPT PROCESSING. This circuitry is responsible for sampling and masking interrupts. The status of all interrupting devices is available to the processor. The processor sets the priority of each interrupt, masks out lower priority interrupts, and services the interrupt with the highest priority. The priority and masking of each interrupt is determined by firmware.

HP-IB AND SYSTEM STATUS SWITCHES. Communication between separate systems is done over a high speed communications link called HP-IB. The Hewlett-Packard Interface Bus requires a device address, and a talk-only or a controlled status on the bus. The status is determined by the settings of the system status switches.

BNC OUTPUTS. Two BNC ports are provided for the user. The BNC labeled PORT supplies one of seven signals from the acquisition system on a multiplexed basis. The other labeled ACCESSORY POWER is a regulated +5 volt supply for use by a preprocessor option.

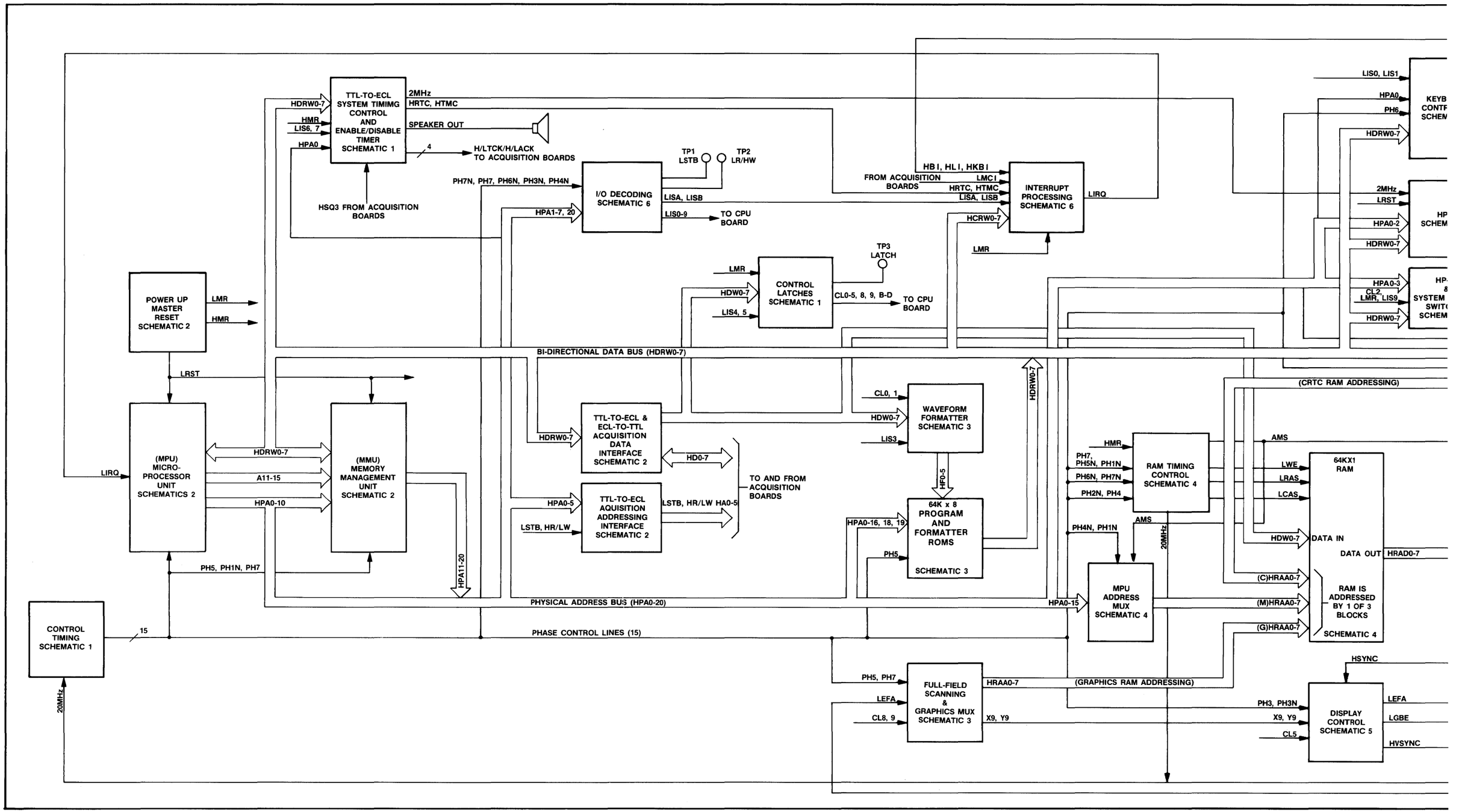
HP-IL. The Hewlett-Packard Interface Loop is used as a low speed form of communication between separate systems. Whether the 1630A/D/G is HP-IL controlled or not is determined by the settings of the system status switches.

PROBE REFERENCE VOLTAGE ADJUST. User data can be sampled at voltage levels ranging from plus to minus 9.9 volts. This block adjusts the comparator switching point (threshold) of each probe hybrid chip so that data is sampled at the specified voltage threshold. The return ground sense lines adjust the threshold level so that data is sampled with respect to the ground level of the user's system. The processor adjusts the probe reference voltages via the keyboard controller.

KEYBOARD CONTROLLER. Scanning the keyboard and controlling probe reference voltage adjustments is the function of this block. The keyboard controller scans each row and column of the keyboard for a closed switch. When a closed switch is found the processor is sent an interrupt request.

KEYBOARD SWITCH PAD. The keyboard is a switch pad consisting of 38 keys, or switches, wired in a 6 x 8 row/column matrix.

NOTES


TTL-TO-ECL SYSTEM TIMIMG CONTROL AND ENABLE/DISABLE TIMER SCHEMATIC 1
HDRW0-7
HMR
LIS6, 7
HPA0
2MHz
HRTC, HTMC
SPEAKER OUT
4
H/LTCK/H/LACK TO ACQUISITION BOARDS
HSQ3 FROM ACQUISITION BOARDS
TP1 LSTB
TP2 LR/HW
PH7N, PH7, PH6N, PH3N, PH4N
I/O DECODING SCHEMATIC 6
LISA, LISB
LIS0-9
TO CPU BOARD
HPA1-7, 20
HB I, HL I, HKB I
FROM ACQUISITION BOARDS
LMC I
HRTC, HTMC
LISA, LISB
INTERRUPT PROCESSING SCHEMATIC 6
LIRQ
HCRW0-7
LMR
TP3 LATCH
CONTROL LATCHES SCHEMATIC 1
HDW0-7
LIS4, 5
CL0-5, 8, 9, B-D
TO CPU BOARD
POWER UP MASTER RESET SCHEMATIC 2
LMR
HMR
LRST
BI-DIRECTIONAL DATA BUS (HDRW0-7)
LIS0, LIS1
HPA0
PH6
HDRW0-7
2MHz
LRST
HPA0-2
HDRW0-7
HPA0-3
CL2, LMR, LIS9
HDRW0-7
(CRTC RAM ADDRESSING)
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LIS3
WAVEFORM FORMATTER SCHEMATIC 3
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HDRW0-7
TTL-TO-ECL & ECL-TO-TTL ACQUISITION DATA INTERFACE SCHEMATIC 2
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TTL-TO-ECL AQUISITION ADDRESSING INTERFACE SCHEMATIC 2
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LSTB, HR/LW
LSTB, HR/LW HA0-5
64K x 8 PROGRAM AND FORMATTER ROMS SCHEMATIC 3
HPA0-16, 18, 19
PH5
(MPU) MICRO-PROCESSOR UNIT SCHEMATICS 2
LIRQ
HDRW0-7
A11-15
HPA0-10
(MMU) MEMORY MANAGEMENT UNIT SCHEMATIC 2
HPA11-20
PH5, PH1N, PH7
PHYSICAL ADDRESS BUS (HPA0-20)
HMR
PH7, PH5N, PH1N
PH6N, PH7N
PH2N, PH4
RAM TIMING CONTROL SCHEMATIC 4
AMS
LWE
LRAS
LCAS
64KX1 RAM
PH4N, PH1N
AMS
20MHz
HDW0-7
DATA IN
DATA OUT
HRAD0-7
(C)HRAA0-7
(M)HRAA0-7
(G)HRAA0-7
RAM IS ADDRESSED BY 1 OF 3 BLOCKS
SCHEMATIC 4
MPU ADDRESS MUX SCHEMATIC 4
HPA0-15
CONTROL TIMING SCHEMATIC 1
15
PHASE CONTROL LINES (15)
20MHz
PH5, PH7
LEFA
CL8, 9
FULL-FIELD SCANNING & GRAPHICS MUX SCHEMATIC 3
HRAA0-7
X9, Y9
(GRAPHICS RAM ADDRESSING)
HSYNC
PH3, PH3N
X9, Y9
CL5
DISPLAY CONTROL SCHEMATIC 5
LEFA
LGBE
HVSYNC

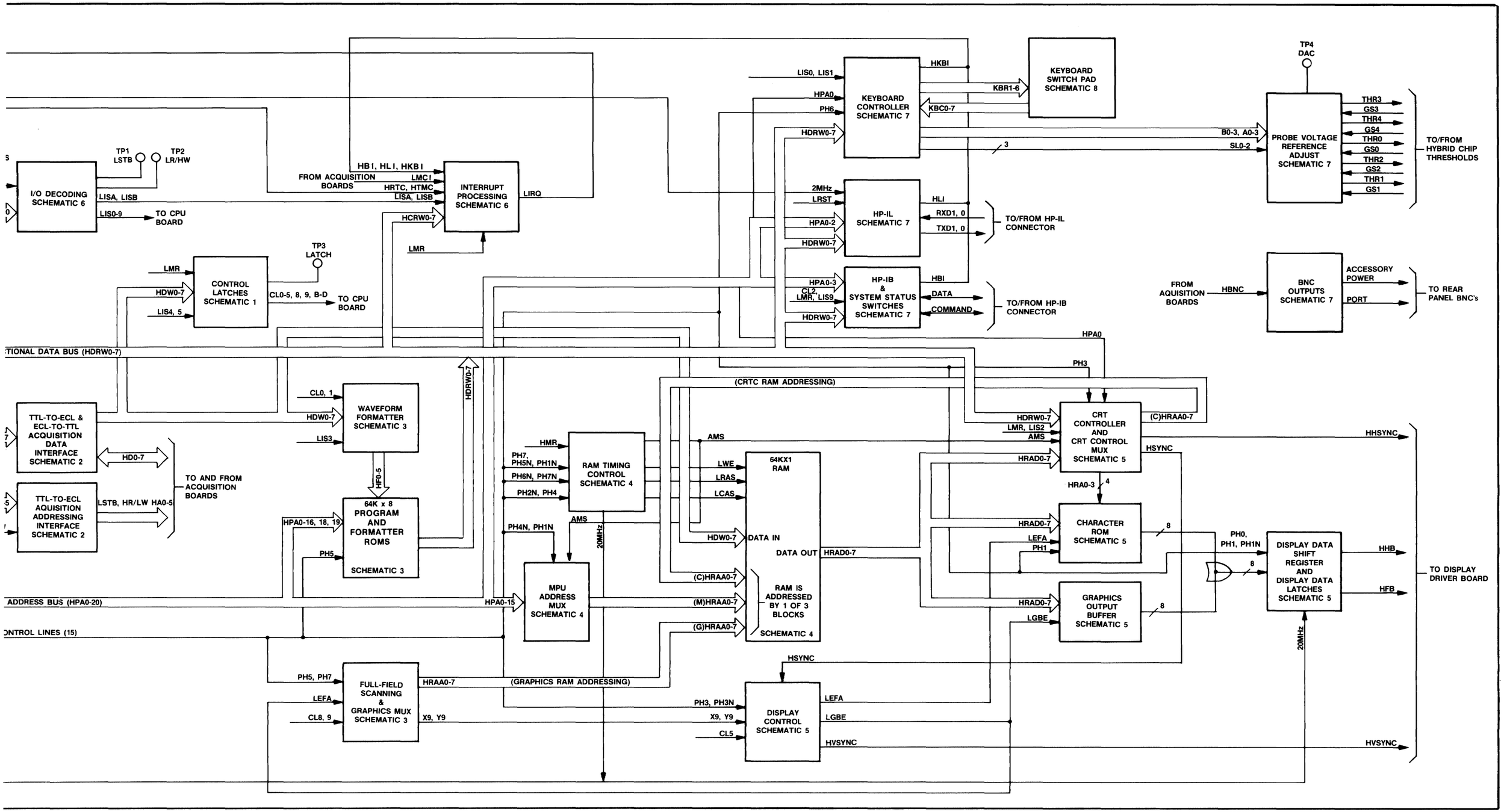


Figure 8B-1. CPU Block Diagram

NOTES

8B-3. THEORY OF OPERATION

The Theory of Operation for this Service Group pertains to the CPU, which includes the interfacing of the keyboard and Display System to the CPU. Refer to the schematic referenced by the secondary heading while reading the Theory of Operation. The theory will begin with the circuitry drawn on the first CPU schematic and continue contiguously to the last.

8B-4. Control Timing (see schematic 8B-1)

The circuit configuration of U7F and U8F is that of an 8-bit twisted-ring shift register. This circuit operates as follows: eight ones and then eight zeros are shifted through the register by a 20 MHz clock. The Q output of each phase is the input for the next phase, thus the output of PH0 is the input of PH1, PH1's output feeds PH2....and PH7N's output feeds back to the PH0 input. Each phase and it's complement are used to control various operations on the CPU board. The frequency of each phase is 1.27 MHz and the delay between adjacent phases is 50 nS. U2D forces this circuit to power up in a twisted-ring configuration.

8B-5. System Timing Controller (see schematic 8B-1)

U6M, a System Timing Controller (STC) chip, is a programmable timer that is configured in the 8-bit mode for reading and writing with the processor. The STC provides the 1630 with a 2 MHz clock for HP-IL, interrupt for a real-time clock, a timing measurement clock for the timing board, and a signal source for the piezoelectric speaker LS1.

UY6Q is an external 4 MHz TTL oscillator that drives the STC. FOUT is a continuous 2 MHz clock used by the HP-IL chip. OUT1 is a 20 mS variable width pulse (HRTC) that the processor synchronizes on for the real-time clock display.

The enable/disable timer circuit provides the time count from the first enable to the first disable of a measurement. An interrupt to the processor is generated at the time of the first disable. The time reference is a 32-bit binary counter clocked at 4 MHz by UY6Q.

The operation of the enable/disable timer circuit occurs as follows: Prior to a timing measurement, HSQ3 and LIS8 are low making the G2 and G2A inputs of U6M high. This in turn disables U6M, allowing the MPU to configure U6M and enable the control latch output CL3 of U6P. When the processor is ready, HSQ3 and LIS8 are pulled high making G2 and G2A of U6M low enabling the STC output OUT4 to be ON for the desired measurement time. When a measurement is complete, HSQ3 and LIS8 are pulled low disabling U6M. Then HTMC, an interrupt request, is sent to the processor via the interrupt processing circuit to indicate a measurement was completed. The processor will then interrogate the STC to determine the time it took for a measurement.

U7M is a TTL-to-ECL translator and U9M is an ECL NOR gate. Note, all of the parts on the acquisition boards are high speed emitter-coupled logic (ECL) parts.

8B-6. Control Latches (see schematic 8B-1)

The processor loads control information into U6P and/or U6O with data from the HDW0-7 bus and clocks the desired part via LIS4 and/or LIS5. The resultant outputs are then used to control various system functions. Each control latch bit assignment is given in table 8B-1.

Table 8B-1. Control Latch Bit Assignments

Data Bit	Bit Name	Logic Level	Function
HDW0	CL0 U6P	L	Enables MPU to address ROM 0 instead of W Formatter.
HDW1	CL1 U6P	H	Enables W Formatter to address ROM 0 instead of MPU.
HDW2	CL2 U6P	H	Allows 1630 to be an HP-IB controller.
HDW3	CL3 U6P	H	Enables MPU to drive low speed timing sample clock.
HDW4	CL4 U6P	H	Not Used
HDW5	CL5 U6P	H	Enables graphics display area.
HDW6	CL6 U6P	X	Spare
HDW7	CL7 U6P	X	Spare
HDW0	CL8 U6O	*	Graphics Page LSB
HDW1	CL9 U6O	*	Graphics Page MSB
HDW2	CLA U6O	X	Spare
HDW3	CLB U6O	H	Enables HVSYNC (Delays HVSYNC until CRTC is loaded)
HDW4	CLC U6O	**	CRT controller (CRTC) page LSB
HDW5	CLD U6O	**	CRT controller (CRTC) page MSB
HDW6	CLE U6O	X	Spare
HDW7	CLF U6O	H/L	Used for signaure analysis LATCH test point.

* or ** - The combination of these two lines determine which 16K byte segment of 64K bytes of RAM is displayed.

MSB	LSB	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

8B-7. Microprocessing Circuitry (see schematic 8B-2)

The processor used by the 1630 Analyzer is a MC68B09E microprocessor unit (MPU). The MPU is an 8-bit processor capable of addressing 64K bytes of memory. However, along with the MC68B29 Memory Management Unit (MMU), another 64K bytes of memory is addressable. Table 8B-2 is the Physical Address-to- function allocation (memory map).

8B-8. MPU OPERATION. The MPU U6I communicates and controls the system via an 8-bit bi-directional data bus HDRW0-7. The processor addresses the system via 16 output lines. The first 8 address lines (A0-7) are latched by U6J to provide hold considerations and buffering for these lines. The next 3 lines (A8-10) are buffered by P/O U5J. The remaining 5 address lines from U6J are then used as the 7 register select lines (RS0-6) for the MMU U6L. HPA7-10 are also used to address ROM, RAM, and I/O.

The clock inputs to the MPU are Q and E. The 1.27 MHz quadrature clock Q leads the E clock by approximately 200 nS. These clocks are also used by the MMU for synchronization.

The read/write output indicates the direction in which data is being transferred on the HDRW0-7 data bus. When this line is high, data is being read on the bus. When the read/write output is low, the MPU is writing to the bus.

The Bus Available (BA) and Bus Status (BS) outputs from the MPU provide the MMU with information about the class of bus operation for each cycle. The following is the MPU state truth table for the BA, BS outputs:

BA	BS	Definition of MPU States
0	0	Normal Running Mode
0	1	Interrupt Acknowledge (LRST or LIRQ)
1	0	SYNC Acknowledge (not used by the 1630A/D)
1	1	HALT or Bus Grant (not used by the 1630A/D)

The NMI, FIRQ, and HALT interrupt inputs to the processor are not used. However, the Interrupt Request line (LIRQ) to the processor is. When an interrupt is detected in the interrupt mask circuitry, the LIRQ line is pulled low. With LIRQ low, the processor then initiates an interrupt sequence, provided the condition code register mask bit (I) is clear.

The LRST input to the processor, when asserted low, will RESET the processor until the LRST line is high. Note, the processor will execute the present bus cycle before going to a RESET state.

Table 8B-2. Physical Address-to-Function Allocation

Physical Address	Function
000000H 05FFFFH	Not Used
060000H 07FFFFH	I/O
080000H 11FFFFH	Not Used
120000H 13FFFFH	ROM
140000H 15FFFFH	RAM
160000H 1FF7FFH	Not Used
1FF800H 1FFEFFH	ROM
1FFF00H 1FFF7FH	MMU
1FFF80H 1FFFFFH	ROM

8B-9. MMU OPERATION. The Memory Management Unit (MMU) U6L is used to expand the 64K byte addressable space of the processor. Expansion is done by applying the upper five address lines from the processor (A11- 15), along with the contents of a 5-bit task register, to an internal mapping RAM. The MMU outputs ten Physical Address lines (PA11-20) which are combined with HPA0-10 from the processor to form the address bus HPA0-20.

The bi-directional data bus HDRW0-7 is used when the MMU registers are written to or read from. The register and byte of information to be selected is determined by RS0-6. Furthermore, the location of the MMU registers is determined by a low on the Register Access (RA) line, providing the current task number is zero and A11-15 are all ones.

Clocking and resetting of the MMU is synchronous with the processor via the E, Q, and reset inputs. Also, the processor determines read/write status of the MMU via the Low Write/High Read (LW/HR) input.

8B-10. Power-Up Master Reset (see schematic 8B-2)

The purpose of this circuit is to keep some key circuitry on the CPU board OFF while the power supply is turning ON. Upon power up U7P pin 5 is at essentially zero volts and charging through R17,19 and C26, whereas U7P pin 4 is at or near 4.55 volts. This keeps U7P pin 2 and 1 low, holding the reset mode ON. When U7P pin 5 exceeds 4.75 volts, pin 2 will go high, charging C35 for 10 mS. As the voltage on U7P pin 7 exceeds the voltage on pin 6, pin 1 will go high thus removing the reset mode.

The Low Reset line (LRST) is for MOS devices requiring a higher set voltage. The High/Low Master Reset (HMR, LMR) lines are used for other devices requiring a certain reset level. Note that all clocks are turned OFF until the reset mode is removed.

8B-11. Acquisition Interface (see schematic 8B-2)

8B-12. ACQUISITION ADDRESSING. U9I and U9J are TTL-to-ECL translators that convert the HPA0-5, LSTB and HR/LW signals to ECL logic levels. This allows the processor to address and control circuitry on the ECL acquisition boards.

8B-13. ACQUISITION DATA. The processor communicates with the acquisition system via a bi-directional data bus HD0-7. A data read occurs when: there is a high on the High Read/Low Write line (HR/LW), a Low Strobe (LSTB) occurs, and the Enable Data Transfer line (ENDT) is asserted low. With these qualifications met, converted data (ECL-to-TTL) from U8K and U9K, seen at the inputs to U7K, is then read onto the bi-directional data bus HDRW0-7. The processor will do a data write when: there is a low on the HR/LW line, LSTB is asserted, and ENDT is low. Write data is then seen on the outputs of U7L (HDW0-7). This information is then converted to ECL levels by U8L and U9L and used on the acquisition boards. See figure 8B-2 and 8B-3 for the timing waveforms between the acquisition system and the MPU during read/write operations.

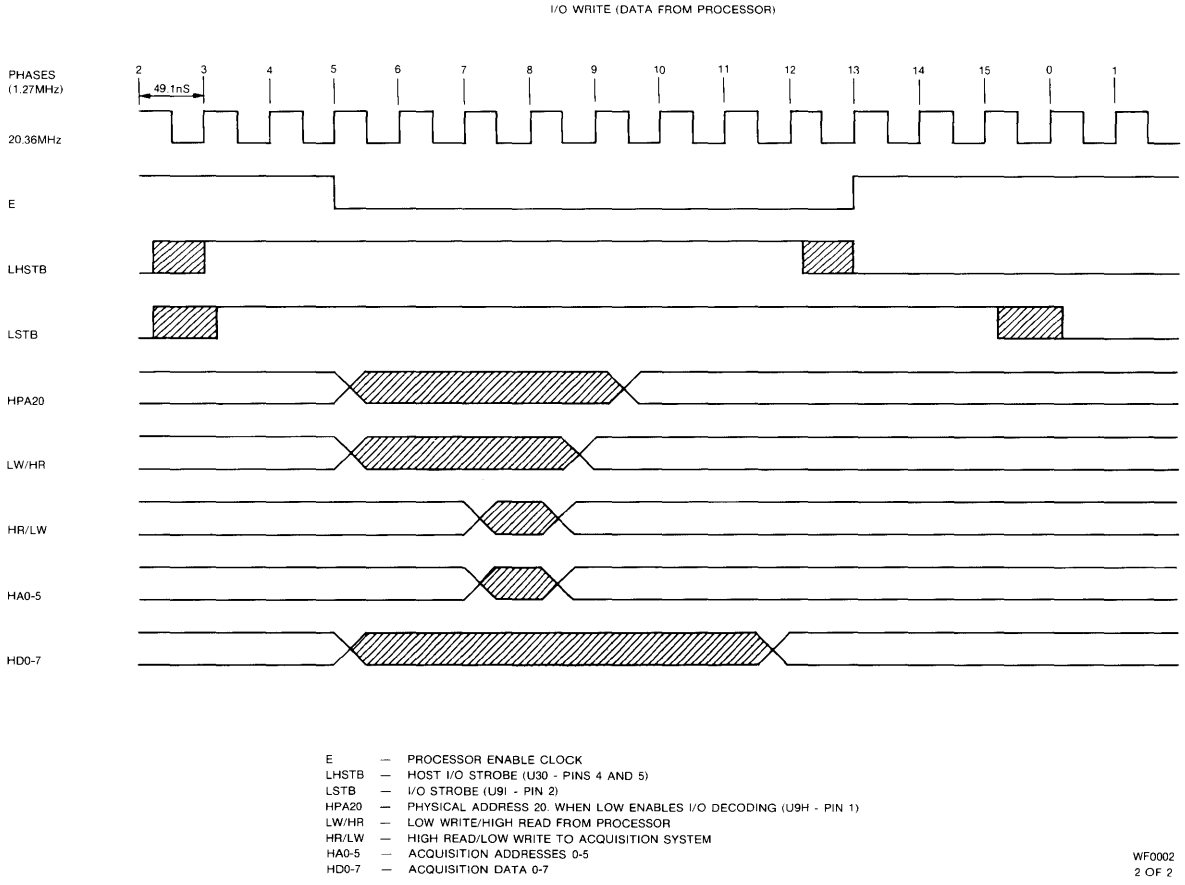
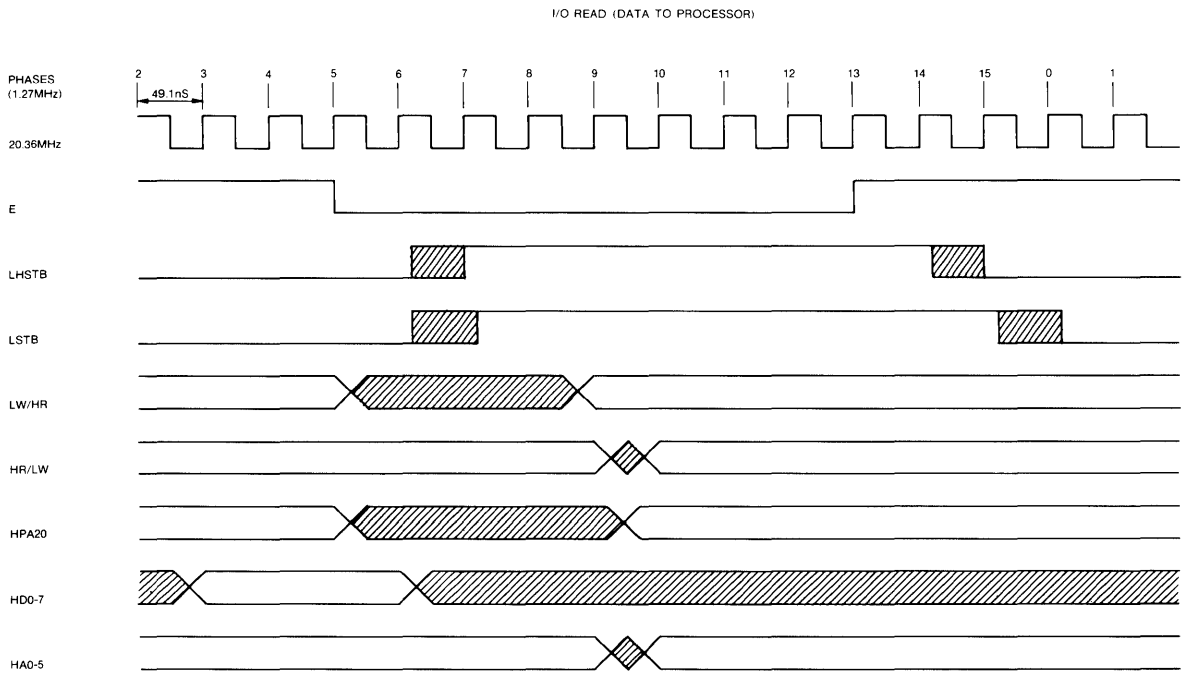


Figure 8B-2. Acquisition Write Timing Waveforms



E — PROCESSOR ENABLE CLOCK
LHSTB — HOST I/O STROBE (U30 - PINS 4 AND 5)
LSTB — I/O STROBE (U9I - PIN 2)
LW/HR — LOW WRITE/HIGH READ FROM PROCESSOR
HR/LW — HIGH READ/LOW WRITE TO ACQUISITION SYSTEM
HPA20 — PHYSICAL ADDRESS 20. WHEN LOW ENABLES I/O DECODING (U9H - PIN 1)
HD0-7 — ACQUISITION DATA 0-7
HA0-5 — ACQUISITION ADDRESSES 0-5

WF0002
1 OF 2

Figure 8B-3. Acquisition Read Timing Waveforms

8B-14. Full-field Scanning Generation and Graphics MUX (see schematic 8B-3)

The full-field scanning generator provides scanning information necessary to display graphics in the 16K bit graphics area shown in figure 8B-5. Display timing waveforms are given in figure 8B-6.

8B-15. SCANNING. Scanning of the full-field graphics display area is done five binary counters (U3F-A,B, U4F-A,B, and U4G) that are cascaded together in a ripple carry configuration. U3F is the high speed Y counter that provides the vertical sweep speed and character frequency of 1.27 MHz (PH5), whereas U4F and U4G form the slow speed X counter that produces the horizontal frame frequency of 60 Hz.

Y counter U3F is cleared by HCY (the decoded display enable (DE) output of the CRT controller) at the end of a line (every 27.5 uS). The Y8 output, pin 11 of U3F-B, indicates the end of a line and is also used to clock U7A-A.

The X counter U4F is cleared by HCX at the end of a frame, as indicated by the X9 output from U4G. The load X counter (LLX) input to U4G is used to load 07 hex into the counter while low, and count from 07 hex when high. The LLX line is the complement of the high clear X counter (HCX) line.

8B-16. GRAPHICS MUX. The multiplexers, U6F and U5F, are used to generate RAM addresses while in the graphics mode and provide RAM refresh during retrace. These devices are enabled by a low level on the low enable full-field display line (LEFD). The input that is selected is determined by the logic level of the address MUX select line (AMS).

The combination of the CL9 and CL8 inputs to U6F determine which 16K byte segment of 64K bytes of RAM is displayed as shown below:

CL8	CL9	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

8B-17. Waveform Formatter (see schematic 8B-3)

Basically, the Waveform Formatter (Formatter) is responsible for taking state and/or timing waveform information from the acquisition system and generating waveform display symbols. The hardware portion of the Formatter generates addresses that are referenced to fourteen, 256-byte look-up tables in the Formatter ROM. The Formatter ROM then outputs the proper waveform display symbol either a high or low level, an edge, or a glitch. The Formatter is used to increase the waveform display update rate.

When a waveform display is requested by the user, the processor clocks acquisition data stored in RAM into data latches U5D, U5P and U5Q. The processor then enables multiplexers U4O, U4P, and U4Q with control latch line CL1; at the same time disabling U3N (via CL0) allowing the Waveform Formatter to address the Formatter ROM, U3K. Then, according to: the users choice of magnification (X1, X2, or X>2); number of channels to be processed; glitch or no glitch; the processor will address a look-up table stored in U3K, and set the multiplexers to mask out the non-effective bits. The look-up table chosen then samples the data from the Waveform Formatter (HF0-5 and HPA0,1), and generates the proper waveform display symbols. The processor then puts this display information into RAM where it is later routed through the graphics buffer, U6AZ, and shifted out of the display data shift register, U6B, to the display.

8B-18. ROM and ROM Selection (see schematic 8B-3)

U4N, a 1 of 8 addressable demultiplexer, is used to enable one of eight 8K word x 8-bit program ROMs for addressing. U7I and U8D determine if U4N is selected and the combination of HPA13-15 select which ROM is enabled.

8B-19. RAM Timing Control and RAMs (see schematic 8B-4)

8B-20. RAM TIMING CONTROL. This circuitry is responsible for creating the R and Column Address Strobes (RAS and CAS) needed for RAM data transfers. LRAS and LCAS, generated by the gating action of U2E, U2C, U2B, and U2A, are needed during read, write, and page mode read cycles of RAM. Figure 8B-7 shows the timing relationships of these signals.

The Address Multiplexer Select (AMS) signal lags LRAS by 25 nS and is used to enable the right group of RAM address multiplexers (MPU, graphics or CRTC) at the proper time during a processor cycle time. The 20 MHz output of U2A, used to clock the control timing circuit and U2C, is half the frequency of the master clock UY1D.

8B-21. RAM. The CPU board uses eight 64K word x 1 bit dynamic RAMs. The RAMs require three external control signals LRAS, LCAS and LWE in order to insure proper data transfers. RAM is controlled by three different cycles; read, write, and page mode read. Note, the page mode read pulse is imbedded in the LCAS waveform and is used while in the graphics mode when two page reads from RAM are needed. The LWE signal controls read/write operations. See Figure 8B-7 for these timing waveform relationships.

Outputting data from RAM occurs as follows: When LCAS is high, the data-out lines from the RAM go to the high impedance state. Note that as LCAS goes high, RAM data latch U5B outputs previously stored data. When LCAS is low the inputs to U5B will be OFF and data will be output from RAM.

RAM refresh is done during a memory cycle at each of the 128 contiguous row addresses within a 2 mS time interval.

8B-22. CRT Control (see schematic 8B-5)

This system uses the vertical scanning method to display information. With this type of scanning, the electron beam scans from top to bottom and from left to right. After each vertical scan the beam is moved horizontally to display another 23 characters. The non-interlace mode is the type of raster scanning used. This means that one field per frame is scanned before the electron beam is returned to the top left hand corner of the display.

For resolution the characters generated on a frame must be continually repeated in order to display them on the CRT. The character code stored in ROM and loaded into RAM is in ASCII and must be converted for use on the CRT. Since ASCII characters cannot be directly displayed, a character ROM (U6C) is used to convert the ASCII codes into the 9 x 16 dot pattern used to generate characters. See figure 8B-4 for a typical dot pattern for a character.

8B-23. CRT Controller (CRTC) Operation (see schematic 8B-5)

The CRTC is the interface between the MPU and the display system. The CRTC U6C contains nineteen programmable registers. These registers are initialized by the processor via the HDRW0-7 data bus. The MPU configures the CRTC to generate horizontal and vertical sync, raster addresses for the character ROM, a display enable signal, and a cursor asserted signal. However, there are several control inputs whose signals contribute to the initialization process. These are described in the following paragraphs.

8B-24. CRTC INTERFACING. The bi-directional data bus D0-7 is used for data transfers between the MPU and one of the internal registers of the CRTC. The high read/low write (HR/LW) line is used to determine whether a register is written to or read from. The register selected is determined by the state of HPA0 that is tied to the register select (RS) line. When HPA0 is low the address register is selected. When HPA0 is high, one of the data registers can be accessed. The enable (E) input is used to clock data to and from the data input/output buffers. The processor controls the E input with LIS2 which is the read/write CRTC line.

The clock (CLK) input is used mainly to synchronize the horizontal sync registers. The clock rate input is equal to the character rate of 1.27 MHz.

The low master reset (LMR) line is tied to the reset input of the CRTC. When a low level is on this line, the CRTC is forced into the following state:

a. The display operation stops and all CRTC counters are cleared.
b. All outputs go low.
c. The control registers remain unchanged and unaffected.

8B-25. HORIZONTAL AND VERTICAL SYNC. The sync signals are generated by the CRTC timing registers. The horizontal registers are programmed in character time (785.79 nS) units with respect to the left-most displayed character. Note that the horizontal sync (HSYNC) signal from the CRTC is NANDed with the control latch bit B (CLB) signals. CLB will go high when the processor is finished initializing the CRTC. The HSYNC signal then becomes the vertical sync (HVSYNC) for the display driver board. The CRT's vertical sync timing registers are programmed in character line time (27.5 uS) and are referenced to the top character position. Note that the vertical sync (VSYNC) signal from the CRTC becomes the horizontal sync (HHSYNC) signal for the display driver board. See figure 8B-6 for the timing relationships of these signals.

8B-26. DISPLAY ENABLE AND CURSOR OUTPUTS. Display enable (DE) is an active high output that indicates that addressing in the active display area is being provided by the CRTC. The cursor (CUR) output signal is determined by the initialization of the CRTC cursor registers. CUR is an active high signal that is exclusive-ORed with HRAD7 to provide inverse/non-inverse display blinking on a character.

8B-27. RAM ADDRESSING. The 14 memory addresses, MA0-13, from the CRTC are multiplexed together by U6E and U5E and used to address a 16K byte segment of dynamic RAM. The combination of the CLD and CLC inputs to U6E determine which 16K byte segment of RAM is available to the CRTC.

CLD	CLC	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

8B-28. RASTER ADDRESSES. The CRTC provides 4 outputs, RA0-3, to be used by the character ROM U6C as the column address (1 of 9) for a character. In other words, RA0-3 position the Character ROM so that the correct character dots are displayed in the correct location on the raster.

8B-29. CHARACTER GENERATION (see Figure 8B-12, schematic 5).

The circuitry responsible for the final processing of a character is the Character ROM, graphics output buffer, the display data shift register, display control circuitry, and the display data latches.

8B-30. CHARACTER ROM. The 121-bit Character ROM address consists of a 7-bit binary ASCII code (HCRA 0-6) that represents a standard symbol, i.e., a letter, number, or a symbol. Also, a column address (HRA0-3) that corresponds to the dot column that is to be output, and a timing qualifier, PH1. When character ROM U6C is enabled by LRE and the low output of U8D pin 6, the proper 8 dot segment for a given character is output to the display data shift register. A dot represents one logical bit.

The dot matrix size for each character is 9 dots wide by 16 dots high. The following is an example of how a single character is displayed on the CRT. Note that there are 23 characters to a character column on the raster (refer to figure 8B-5). The output dot sequence for a character is in 8 dot segments from top to bottom, left to right. The character ROM outputs the first 8 bits to the shift register U6B. When U6B serializes these, another 8 bits is loaded. Then the character ROM is given a new dot column address and the dot output routine is repeated. This is done 9 times for each character. Thus, the 9 x 16 character dot pattern. Note that a high from U6C is equal to a dot being on. See figure 8B-4 for a typical dot pattern.

8B-31. DISPLAY DATA SHIFT REGISTER. This device is responsible for converting parallel display information into a serial data stream. U6B can be configured for either shift left or parallel loading operations. This is determined by the level on pin 1.

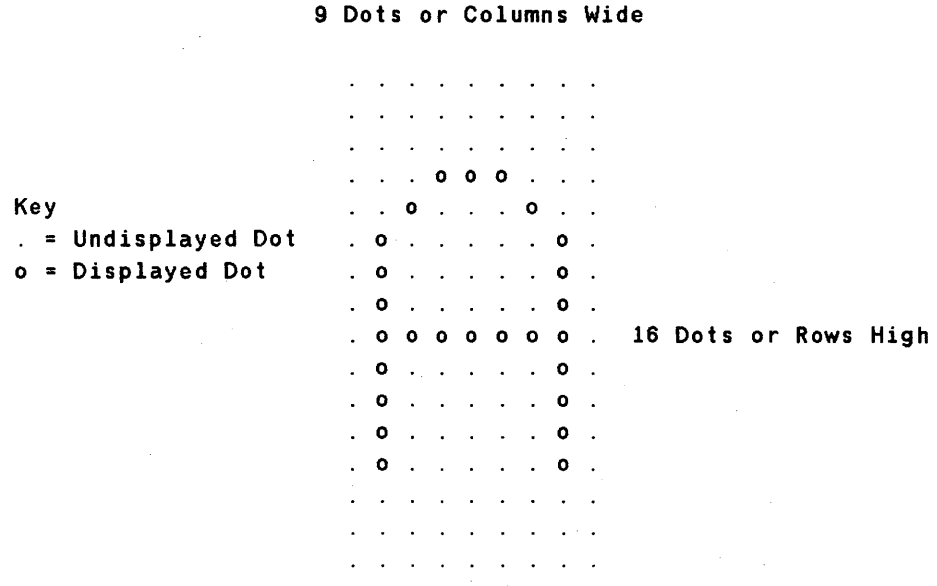


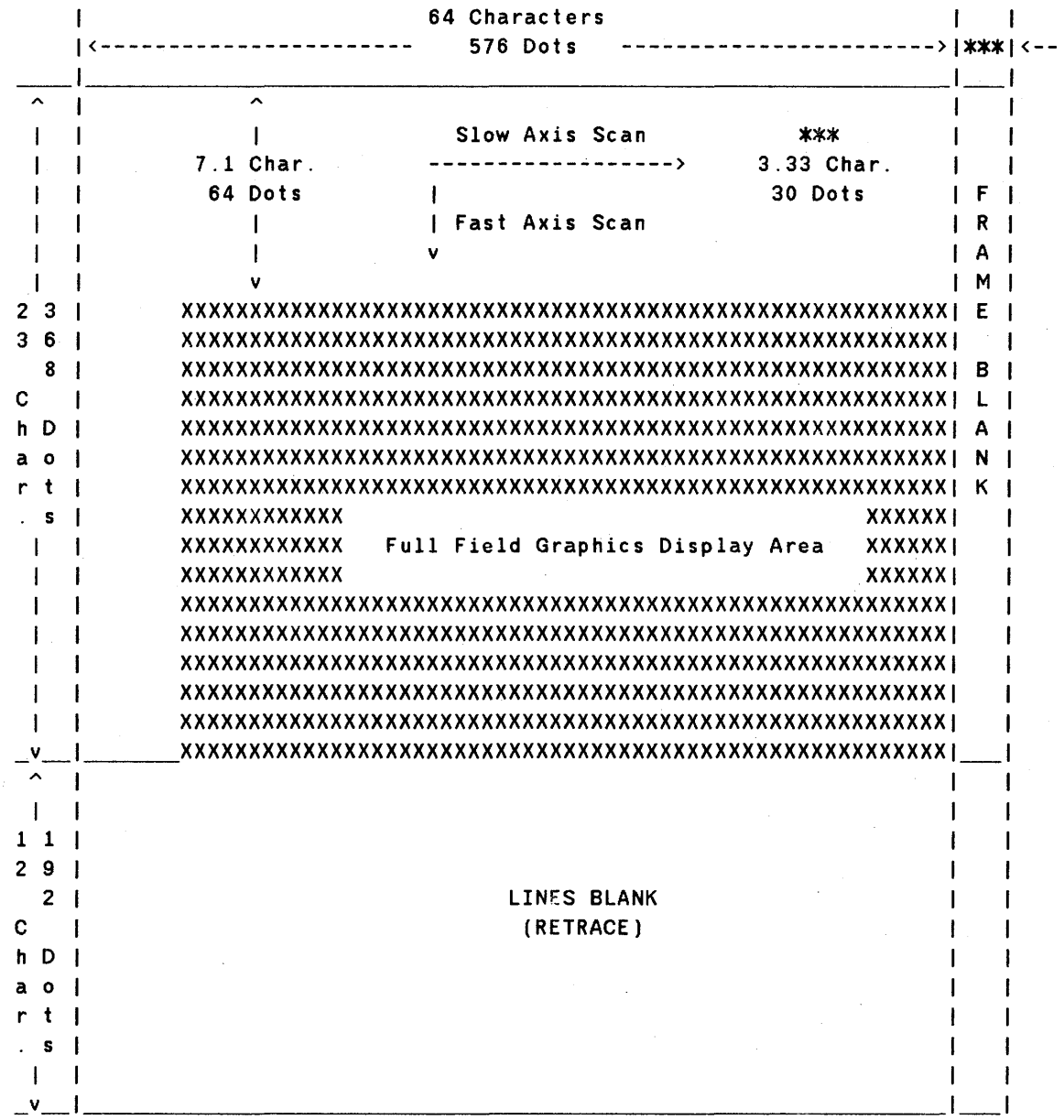
Figure 8B-4. A Typical 9 x 16 Dot Pattern for a Character.

8B-32. GRAPHICS OUTPUT BUFFER. While in the graphics mode the Character ROM is disabled and U6A is enabled. Graphics information is then loaded into U6B and displayed in the full-field graphics display area.

8B-33. DISPLAY DATA LATCHES. The display data latches U8C-A,B provide the video data to the display driver board. These latches are clocked at 20 MHz making a 50 nS dot rate, whereas the combination of the outputs of U7B-A,B determine the brilliance of the video displayed. The following is the output of U8C-A,B which is the truth table for video information.

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

8B-34. DISPLAY CONTROL. This circuitry is responsible for controlling display operations. For instance, the outputs of U7A and U9D-B control which device group access RAM and which devices are ON or OFF during a fast axis retrace. U7C provides timing for the cursor and enables the video brightness circuitry, U7B-A,B. Also, this circuitry enables and disables the character ROM, full-field scanning generator, and graphics buffer during the proper time in a processor cycle.



For more information see table 8B-6.

Figure 8B-5. Display Character Area

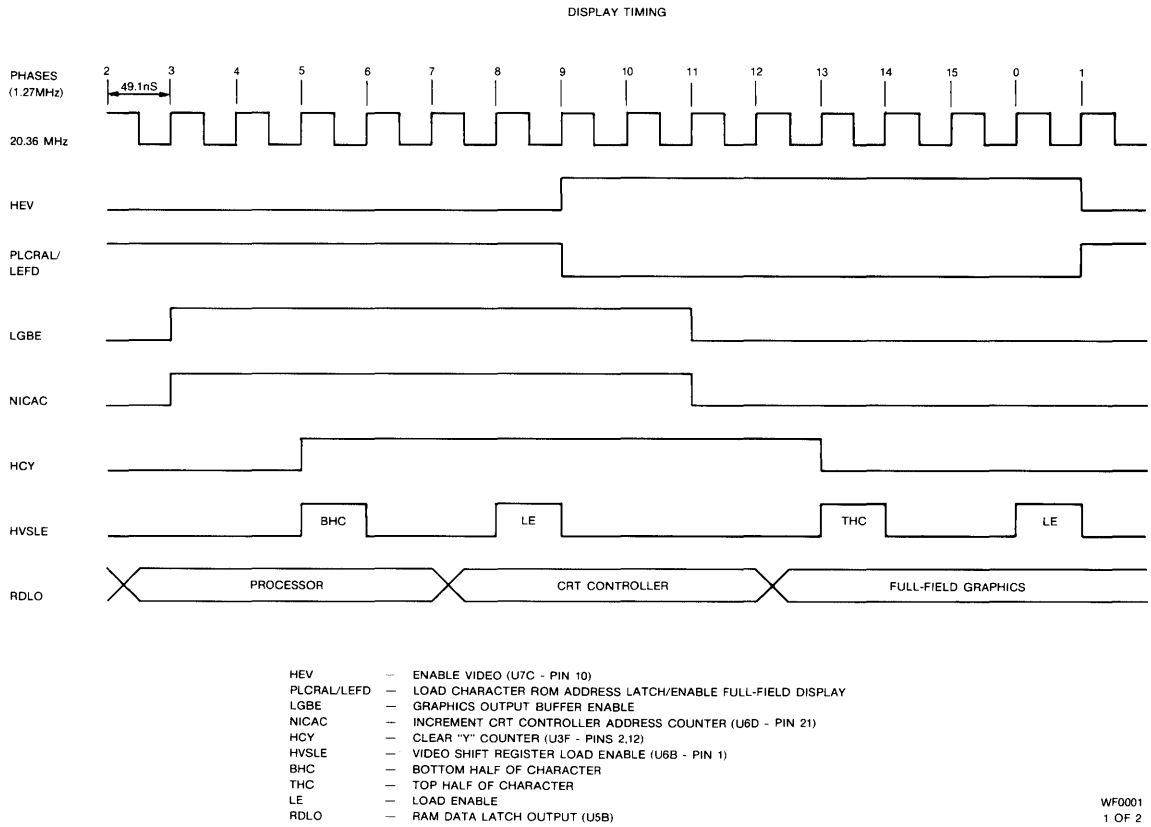


Figure 8B-6. Display Timing Waveform For One MPU Cycle

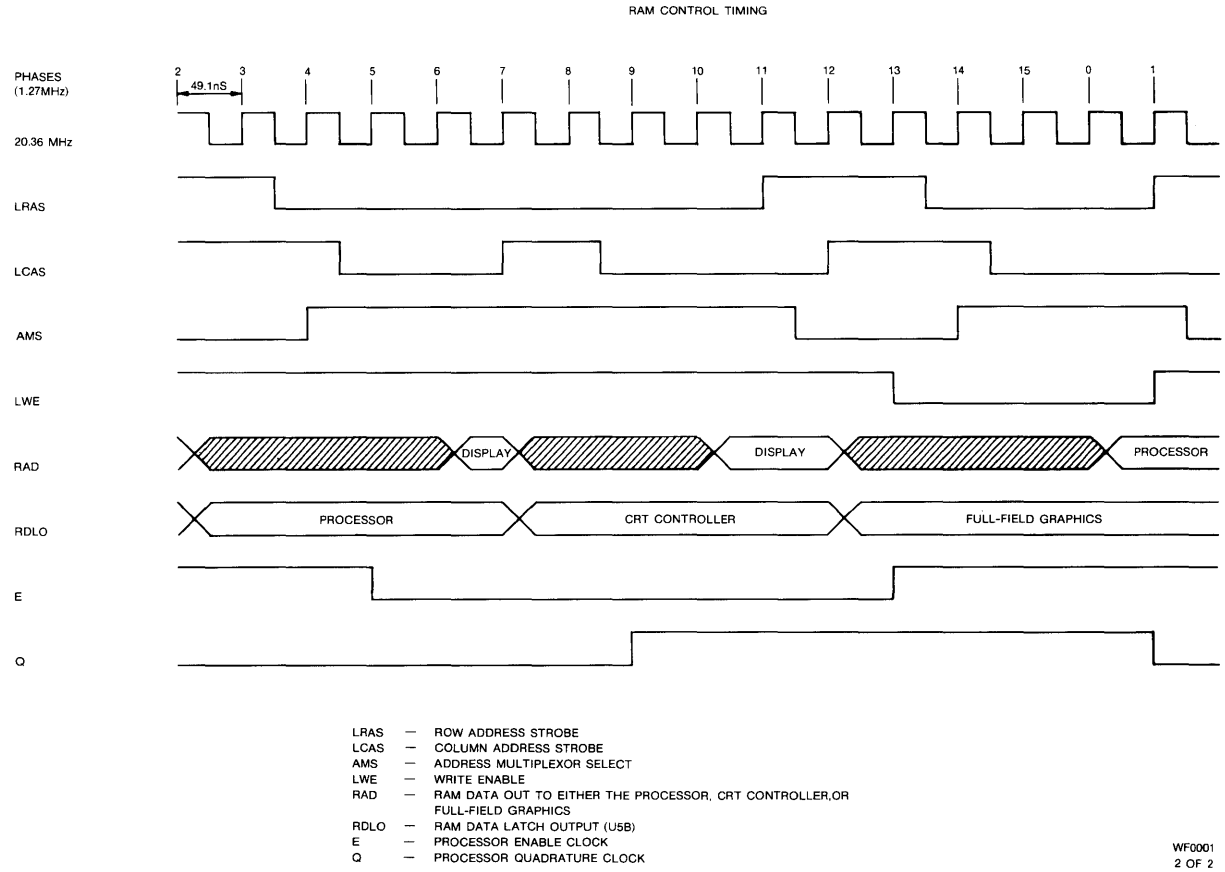


Figure 8B-7. RAM Timing Waveforms For One MPU Cycle

8B-35. I/O Decoding (see schematic 8B-6)

The Input/Output decoding circuitry is separated into two levels of decoding; macro and micro. I/O operations are enabled by a low level on the HPA20 address line from the MMU. Each level of decoding is outlined in the following.

8B-36. MACRO I/O DECODING. Macro decoder U30 is a 1 of 8 addressable demultiplexer. U30 is used to select, or enable, an I/O device that requires more than 2 Physical Addresses to perform a specific I/O function, i.e., read or write operations. Macro I/O is memory mapped into a 256 word space as shown in table 8B-3. Each macro I/O function, when selected by U30, is given 32 words of ROM space. However, the acquisition system is given a total of 64 words, two outputs from U30 which are ORed together by U71-A to form Low Strobe (LSTB).

Table 8B-3. Macro I/O Physical Address-to-Function

Physical Address	I/O Function	Strobe Mnemonic
06XX00H	Acquisition Sys.	LSTB
06XX40H	Micro I/O	
06XX60H	HP-IL Write	LHLW
06XX80H	HP-IL Write	LHLR
06XXA0H	HP-IB	LHBS
06XXC0H	Spare	
06XXE0H	Not used	LSS

8B-37. MICRO I/O DECODING. Micro decoders U5N and U6N are 1 of 8 addressable demultiplexers. U5N and U6N are used to select, or enable, an I/O operation and/or device that requires 2 Physical Addresses or less to perform an I/O operation. The I/O strobe line to function is given in table 8B-4.

Table 8B-4. Micro I/O Physical Address-to-Function

Physical Address	I/O Function	Strobe Mnemonic
06XX40H	Keyboard Read Data	LIS0
06XX41H	Keyboard Read Status	LIS0
06XX42H	Keyboard Write Data	LIS1
06XX43H	Keyboard Write Status	LIS1
06XX44H	Read/Write CRTC	LIS2
06XX46H	Write Formatter	LIS3
06XX48H	Write Control Latch U6P	LIS4
06XX4AH	Write Control Latch U6O	LIS5
06XX4CH	Read Counter U6M	LIS6
06XX4EH	Write Counter U6M	LIS7
06XX50H	Reset Enable/Disable Timer FF	LIS8
06XX52H	Read HP-IB Address	LIS9
06XX54H	Read Interrupt Status	LISA
06XX56H	Write Interrupt Mask	LISB
06XX58H	Spare	LISC
06XX5AH	Spare	LISD
06XX5CH	Spare	LISE
06XX5EH	Spare	LISF

8B-38. Interrupt Processing (see schematic 8B-6)

When an interrupt is generated by a device, a high will be sensed at the inputs to the interrupt mask and the read interrupt status buffer U1M. The interrupting device(s) is determined by the output of U1M. Each interrupt is given a specific firmware priority so that if two interrupts occur simultaneously, one will be serviced before the other. Interrupt priority is done by masking out the lower priority interrupts with a zero, from U1L, on the other input of their respective interrupt mask NAND gate. The highest priority interrupt is given a one (thus, making the low interrupt request (LIRQ) line low to the processor). The processor will then service the interrupt, clear the device's interrupt request line, read the interrupt status buffer, and change the interrupt mask to sample the next highest priority interrupt.

8B-39. HP-Interface Bus (HP-IB) Circuitry (see schematic 8B-7)

The Hewlett-Packard Interface Bus transfers data and commands between systems via 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect systems. The cables connect all instruments, controllers, and other components of the system in parallel. The following is a description of the inputs to the HP-IB controller, and the outputs as they relate to interface operations.

8B-40. MPU TO HP-IB INTERFACE. HP-IB controller U2G communicates via thirteen memory mapped registers. Six of the registers are read from, and seven are written to. The registers are used to pass control data to, and status information from, a system component. HPA2-0, connected to the register select (RS2-0) lines, are used to select a particular register. A low on the chip enable line (CE) indicates that the processor is doing either a read or write from the selected register. Note that each combination of RS2-0 can indicate one of two different registers depending on whether a read or write operation is occurring. For example, a write operation with RS2-0 = 110 indicates a Parallel Poll register access, but a read to the same location indicates a Command Pass Through register access.

Reading or writing to a register is indicated by the level of HPA3. A high indicates an MPU read and the Data Bus In (DBIN) line will be asserted. When low, the Write Enable line (WE) is asserted and the MPU will write to a register. Data transfers are via the bi-directional data lines HDRW0-7 attached to the D0-7 lines of U2G.

8B-41. HP-IB INTERFACE LINES AND OPERATIONS. The eight data I/O lines (DIO1-8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and is coordinated by three handshake lines: Data Valid (DAV), Not Ready For Data (NRFD), and Not Data Accepted (NDAC). The other five lines are for management of bus activity. See figure 8B-8 for HP-IB signal lines.

Devices connected to the bus may be talkers, listeners, or controllers. The controlling device dictates the role of each of the other devices on the bus by setting the ATN (attention) line true (low true) and sending talk or listen addresses on the data lines.

The MPU reads the rear panel switches to determine its device bus address and loads this into the HP-IB controller. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data; all others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers are automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines (DAV, NRFD and NDAC). No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently. For HP-IB handshake timing, see figure 8B-9.

The ATN line is one of the five management lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII codes. When ATN is false, any code of 8 bits or less understood by both talker and listener(s) may be used. The Interface Clear (IFC) line places the interface system in a known quiescent state via the abort message. The Remote Enable (REN) line is used with the remote, local and clear lockout/set local messages to select either local or remote control of each device. Any active device can set the Service Request (SRQ) line true. This indicates to the MPU that the device on the bus wants attention. The End Or Identify (EOI) line is used by a device to indicate the end of a multiple-byte transfer sequence. When the controlling device sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

The Interrupt (INT) line indicates an interrupt request when low. This signal is then inverted by U3P-B and routed to the interrupt mask where the MPU branches to a subroutine to service this interrupt.

8B-44. HP-IB TRANSCEIVERS. All of the input/output signals from the HP-IB controller are routed through two octal bus management transceivers U1I, and U1H. These devices are controlled by CONT (controller), TE (talk enable), and CL2 (system controller). U1I controls the direction of command and data transfer signals. The direction of the command signals ATN, SRQ and EOI is determined by the CONT line, but IFC, and REN are directed by CL2. Data transfer signals NRFD, NDAC, and DAV are controlled by TE. The direction of data flow through U1H is determined by ATN or EOI, while TE controls whether U1H is tri-stated or in the open-collector (enabled) mode.

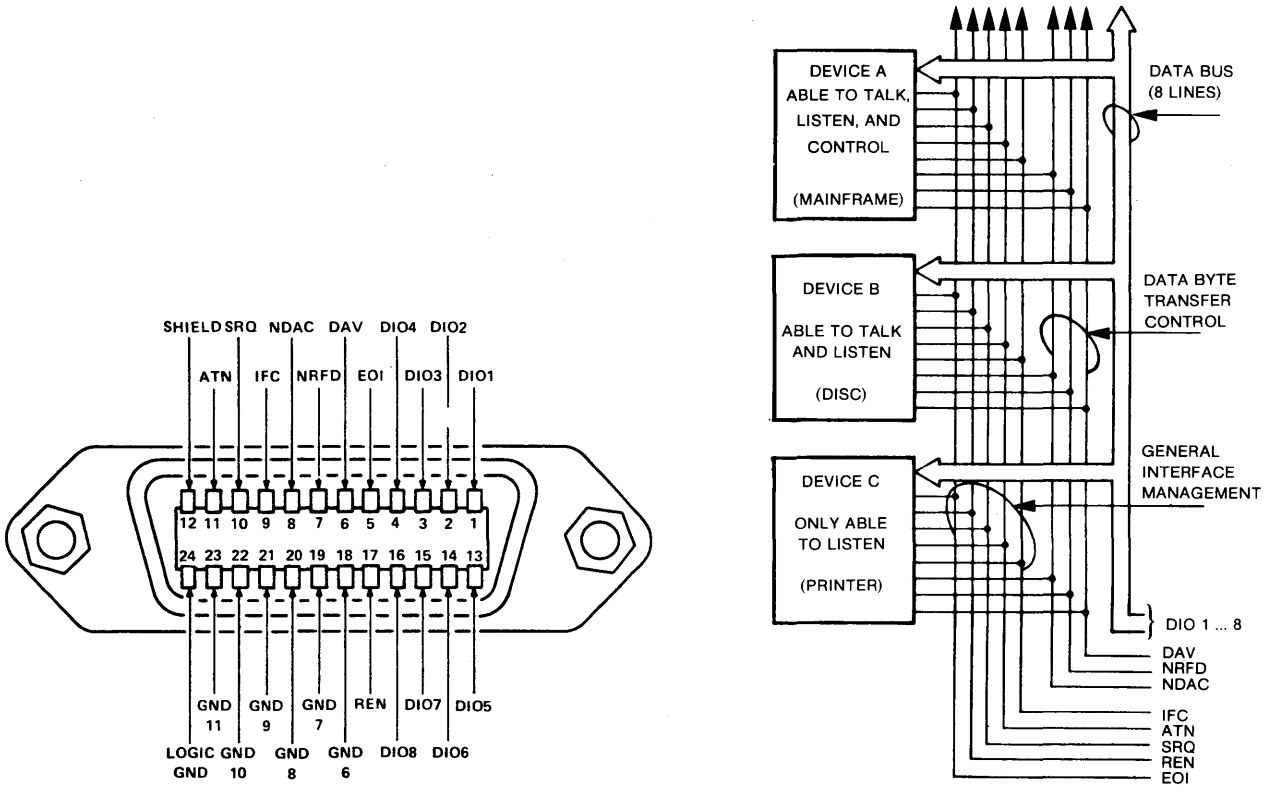


Figure 8B-8. HP-IB Signal Lines

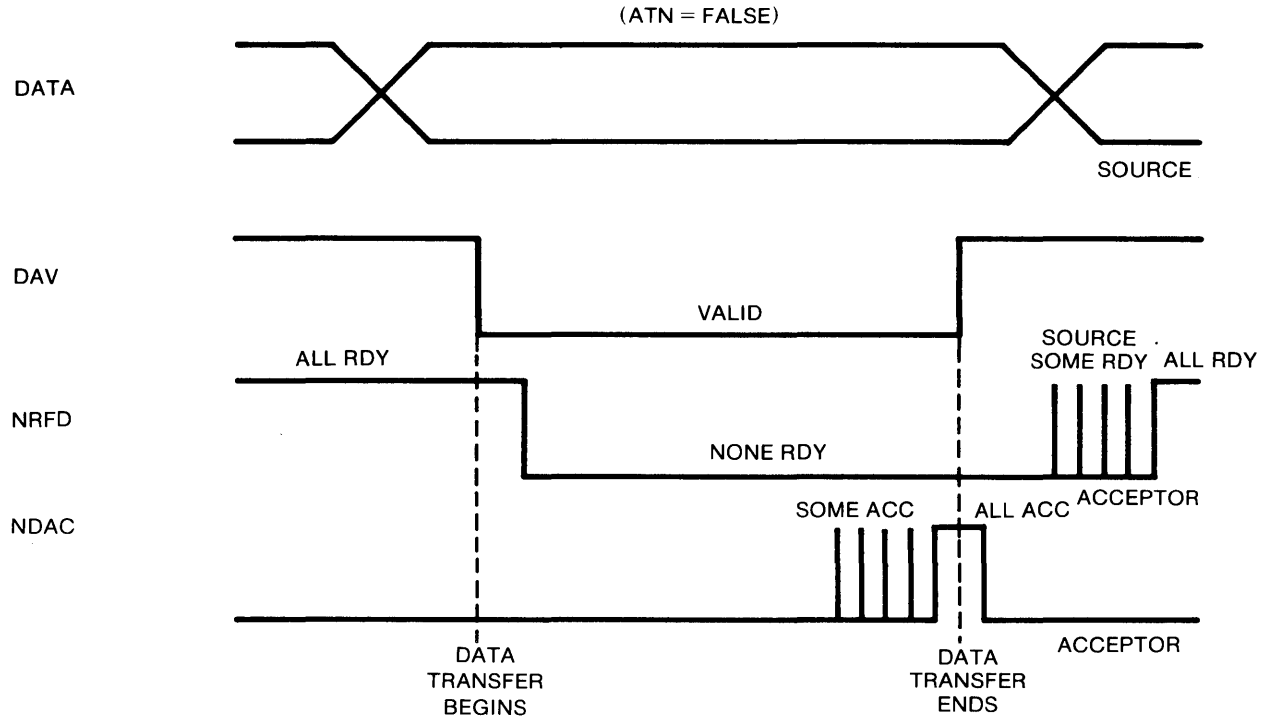


Figure 8B-9. HP-IB Handshake Timing For One Talker And Multiple Listeners

8B-43. System Status Switches (see schematic 8B-7)

SW1, an 8 switch dip package, is mainly used to configure the 1630 on a system bus, i.e., HP-IB and HP-IL. Switch 6 of 8 is used to access a self test (ST) routine for testing some of the functions of the 1630. See Section 3 (Operation) for configuring the 1630 for HP-IB and HP-IL operations and Section 4 (Performance Tests) for initiating ST.

Switches 1 through 5 of 8 are used to select an address on the HP-IB interface bus. The combination of switches 7 and 8 select HP-IB talk only, HP-IB controlled, HP-IL controlled.

During power-on, the processor reads the status of SW1 by enabling U1E via LIS9. Then according to the switch settings the processor will either initiate self test (ST), write the HP-IB address and status into the HP-IB controller, or indicate to the HP-IL controller whether or not it is to be controlled by an outside device.

NOTE

The processor samples the setting of the system status switches ONLY during turn-on. Changing SW1 to "1" after turn-on will not initiate SELF TEST. Cycling the power OFF/ON will reset the switch status. After ST is executed, however, the ST switch may be set to a "0" allowing the System Specification menu to be displayed without cycling power.

8B-44. BNC Outputs (see schematic 8B-7)

The rear panel BNC labeled PORT is used to supply the following seven signals from the acquisition system on a multiplexed basis. The other BNC labeled ACCESSORY POWER provides a regulated + 5 volt power supply for use by a preprocessor option.

Signal to BNC

a. Pulse on State Trace Point
b. High until State Trace Point
c. Low until State Trace Point
d. High on last Sequence
e. Constant High
f. Constant Low
g. High on Timing Pattern

8B-45. HP-Interface Loop (HP-IL) Circuitry (see schematic 8B-7)

8B-46. GENERAL INFORMATION. HP-IL is a bit-serial, uni-directional loop. Information is re-transmitted by each device; each device supplies only enough power to drive the message on to the next device. Also, HP-IL protocol provides for excellent error detection (meaning that commands and data make a complete circuit of the loop.) The originating device receives the information back after all other loop devices have received and transmitted it. By comparing returning information with what was sent out, errors along the loop are automatically detected.

HP-IL is capable of transmission speeds of up to 5,000 bytes per second. This speed is equivalent to about one printed page per second.

Three different roles are defined for HP-IL devices: Controller, talker and listener. Any device not assigned one of these roles is inactive. The controller is the one device in the loop that can designate the roles of devices and control the loop's operation. The system controller is the device that controls and initiates loop communication. It can transfer control to another device, which then becomes the controller on the loop (the active controller). Likewise, an active controller can transfer control to another device.

In order to distinguish between devices in the loop, each device must have an address (a number from 1 to 30). The controller uses the addresses to specify and control the devices. Even though each HP-IL device has a built-in address, the system controller always assigns new sequential addresses to each loop member. These addresses begin with address one for the device that follows the controller. Each device then stores its assigned address internally.

Information is in two categories: commands and data. Each piece of information, a command or data, is initiated by a device and sent around the loop. Each subsequent device, in turn, receives the information and either sends the information to the next device, or processes the information and then sends the information on to the next device.

8B-47. MPU TO HP-IL INTERFACE. The HP-IL controller U2O is used to interface the 1630 to devices that work at relatively low data rates, i.e., a digital cassette drive. U2O serves the purpose of converting signals back and forth from HP-IL to the MPU. The processor communicates with U2O through memory or I/O read and write cycles. The HP-IL chip has a Chip Select line (CS) and three address lines (RS0-2) to permit data transfers to and from eight internal registers. Note that some of the register bits are read-only, or write-only while some have bits that are both.

A write operation occurs when Low HP-IL Write (LHLW) from the macro decoder goes low, then the register selected by RS0-2 will be written to by the processor via the HDRW0-7 data bus. Read operations operate the same as a write operation except the Low HP-IL Read (LHLR) line will be asserted low.

The 2 MHz clock from the system timing controller provides the clock for the HP-IL chip. A low reset (LRST) from the power up master reset circuit will shut off the internal oscillator allowing the processor to initialize the chip.

8B-48. HP-IL INTERFACE LINES AND OPERATIONS. The signals from the previous device come into the receive data inputs RXD0 and RXD1 through a small pulse transformer in UT1 which provides a voltage step-up and isolates this device from the loop. R3 and R6 from the receiver inputs provide the proper load for the loop.

Each of the transmitter outputs TXD0 and TXD1 pass through a low-pass filter and impedance matching network consisting of C2, R5 and C1, R4. The signals then go through a pulse transformer which steps down the voltage to the proper loop level and isolates this device. Zener diodes CR1-4 are provided for transient suppression.

Whenever one or more of the interrupt bits together with the corresponding enable bit in the interrupt register is high, the interrupt request line HLI will be low. This signal is then inverted by U3P and seen in the interrupt mask. The MPU will respond, clearing or masking the bit, and IRQ will return to its normal high state. Unless the interrupt flag bit is cleared or masked, no further interrupts can occur since the interrupt line will remain in its low state.

8B-49. Probe Reference Voltage Adjust (see schematic 8B-7)

The thresholds (THR0-4) for each pod are reference power supplies that specify the comparator switching points on the pod hybrid chip. Each of the five processor programmable supplies consist of a sample/hold circuit selected by U7O, and adjusted by U9N, a programmable DAC. Data can be specified in ranges of plus to minus 9.9 volts in 0.1 volt increments.

8B-50. PROBE THRESHOLD SELECTION. The following is a brief example of this circuit's operation for selecting one probe threshold: The user can request a specific threshold for sampling data on each pod, either TTL, ECL, or a level equal to or less than +/- 9.9 volts (this system defaults to TTL sample levels). After a threshold is selected the processor will program U9N (via U9E), a digital-to-analog converter (DAC) for a current level proportional to the threshold. This current level is then converted by U8O to a voltage level proportional to the required threshold. A probe threshold driver is selected by U7O. The selected reference threshold level is then used by the pod hybrid chip. The probe threshold driver will hold a reference level until it is refreshed or updated.

8B-51. ADDITIONAL INFORMATION. The DAC is configured for write only operation. The processor writes information into the DAC via the keyboard controller U9E. When BD is high, write information is presented to the DAC, and a probe threshold driver is selected by U7O (via the scan line outputs SL0-2 of U9E). Then, when BD goes low it is delayed in the voltage reference circuitry. When U7P pin 13 goes low, the DAC latches the data on its input, converts it, and presents it to U7O. When U7P pin 14 goes high, the selected probe threshold driver samples the converted data. Then, in 100 mV increments, a reference voltage (THR0-4) proportional to the user threshold sample voltage is output. The reference voltage is refreshed or updated every keyboard scan time. A keyboard scan time is 5 mS or every time BD goes low.

The ground sense lines, GS0-4, compensate for the difference in ground levels between systems. For example, if the voltage on GS0 was able to form a voltage drop across R4 of UR9P then the voltage on THR0 would increase proportionally. This insures that data is being sampled at the user selected threshold level with respect to the users system ground.

The Voltage Reference circuit provides a precision +5 volt supply for the DAC and a voltage reference (VR) for U7P in the Power-Up Master Reset circuit.

8B-52. Keyboard Scanning (see schematic 8B-7)

The keyboard controller, U9E, is used to scan the keyboard and control probe reference voltage adjustments. U9E is programmed and controlled by the processor for each of these functions. The following will describe the keyboard scanning functions of U9E.

8B-53. MPU TO KEYBOARD CONTROLLER INTERFACE. The I/O control section of U9E uses four signals to control data flow to and from several internal registers and buffers via the HDRW0-7 data bus. With chip select (CS) tied, low bi-directional data flow is always enabled. A high on the A0 line indicates that the information going in or out to the MPU is command or status. whereas a low means the information transferred is data. When LIS0 is low, data or status is read (RD) into U9E. When LIS1 is low, data or status is written (WR) into U9E.

The 1.27 MHz PH6 signal ties to the clock (CLK) input of U9E. By programming U9E, this frequency is divided internally to 100 KHz which yields a 5 ms keyboard scan time or a 200/sec scan rate.

The Reset Line (RST) is tied to the power up master reset circuit via the High Master Reset line (HMR).

8B-54. KEYBOARD SCAN OPERATIONS. The keyboard controller uses the sensor matrix mode for scanning the keyboard. This means that each switch is given a specific sensor matrix location in an 8 bit x 8 bit sensor RAM on U9E. Thus, the sensor RAM keeps an image of the state of the switches in the sensor matrix. In this mode debouncing of the switches is not done. However, the advantage is that the MPU can determine how long a switch is depressed. The interrupt request line (HKBI) will go high, and stay high at the end of a sensor matrix scan if a location has changed value.

The following is an example of a sensor matrix scan: Scanning the rows of the sensor matrix, or keyboard, is done with the combination of the encoded scan lines, SL0-2. These lines will count from zero to seven in binary enabling U9F, a 1 of 8 demultiplexer. U9F will low select the proper row (KBR1-6) of switches that corresponds to the proper row, or byte, in the sensor RAM matrix. Then, while each row is asserted, each column (KBC0-7) in the sensor matrix is sampled and loaded into their respective bit locations in the sensor RAM. If a low was sensed on a column line, then the intersection of that row and column indicates a switch closed in the sensor matrix. The IRQ line will then go high indicating to the processor that a switch was pressed. The processor will service the interrupt and IRQ will go low. See figure 8B-10 for the keyboard switch to sensor matrix address locations.

BYTE ROWS ↓ BIT COLUMNS →

	KBC7	KBC6	KBC5	KBC4	KBC3	KBC2	KBC1	KBC0
KBR0	row not used							
KBR1		CHART	WFORM	LIST	TRACE	FORMAT	SYS.	CURSOR ↑
KBR2				F	E	D	[] NEXT	CURSOR →
KBR3		RUN	C	B	A	[] PREV	CURSOR ↓	CURSOR ←
KBR4		STOP	9	8	7	CHS		ROLL ↑
KBR5		PRINT	6	5	4	DON'T CARE	ROLL ↓	
KBR6	BLUE	3	2	1	0	CLR ENTRY	INSERT	
KBR7	row not used							

NOTES

a. Keys do not exist for blank spaces above
b. KBC0-7 = Keyboard column 0-7
c. KBR0-7 = Keyboard row 0-7

Figure 8B-10. Keyboard Switch to Sensor Matrix Address Locations

8B-55. Keyboard Switch Pad (see schematic 8B-8)

The keyboard is a 6 x 8 matrix consisting of 6 rows labeled KBR1-6 that are enabled one at a time, and 8 columns (KBC0-7) that are sampled each row time for a closed switch. The 38 keys used are single-pole single-throw switches. The keyboard interfaces with the keyboard controller, U9E, on the CPU board.

8B-56. DISPLAY SYSTEM OPERATION VERIFICATION AND TROUBLESHOOTING

The following procedure and information is used to determine if the CPU, Display Driver, or CRT is faulty. The first section determines if the CPU board is bad, the second determines if the CRT or Display Driver is faulty.

CPU INTERFACE OPERATION VERIFICATION

NOTE

The following procedure assumes that there is NO video information being displayed on the CRT.

a. Turn OFF the 1630A/D.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover. Remove cover. For more information refer to the installation and removal procedures in Section II.

c. At the Display Driver board disconnect the 16-pin ribbon cable (W2) going to the CPU board.

d. See table 8B-5 for cable pin assignments. Probe these pins while referencing tables 8B-5 and 8B-6.

e. See table 8B-6 for applicable electrical specifications if problems exist.

Table 8B-5. CPU To Display Driver Cable Pin Assignments

Pin 1 is the red wire

(VER. SYNC)	HVSYNC	1		2		GROUND
(HOR. SYNC)	HHSYNC	3		4		GROUND
(VIDEO B)	HFB	5	P	6		GROUND
(VIDEO A)	HHB	7	I	8		GROUND
(SOURCE)	+5V	9	N	10		GROUND
(SOURCE)	+12V	11	S	12		GROUND
(SOURCE)	+15V	13		14		GROUND
(SOURCE)	+15V	15		16		GROUND

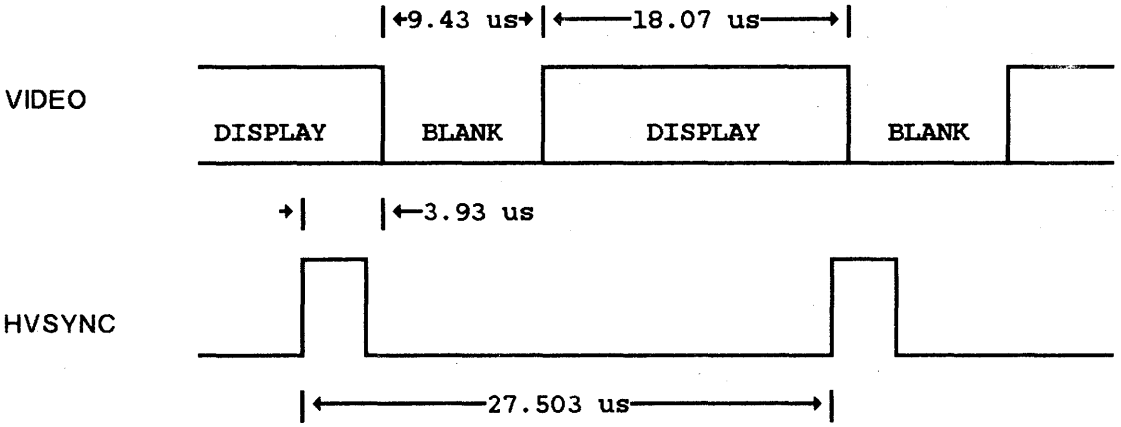
Table 8B-6. Applicable Electrical Specifications

Vertical Sync. (fast axis)

a. Single-ended TTL input: HVSYNC

b. Sync signal timing characteristics.

Pulse width and position relative to the video. Timing is indicated below:



c. Scan direction is top to bottom.

Horizontal Sync. (slow axis)

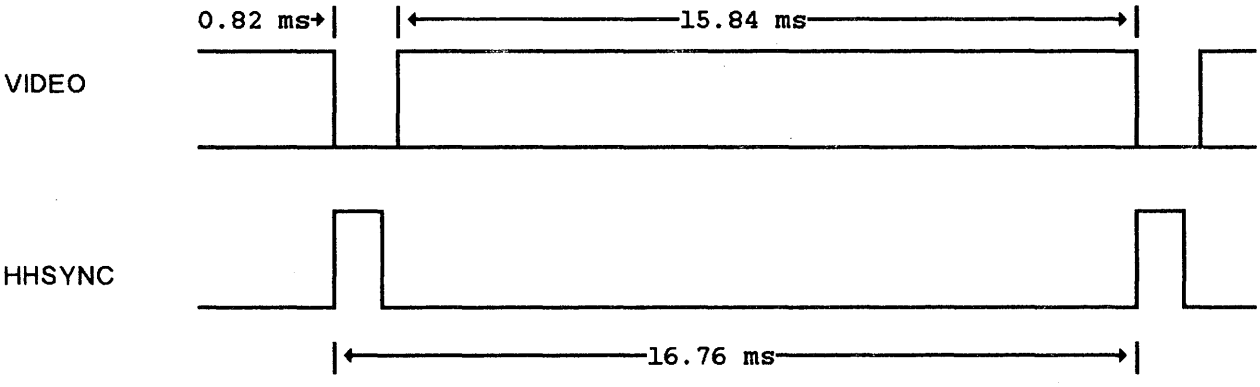
a. Single-ended input: HHSYNC

1. Low level signal is less than or equal to 0.4 volts.

2. High level signal is 5.0 volts +/- 5%.

b. Sync signal timing characteristics.

Pulse width and position relative to the video. Timing is indicated below:



c. Scan direction is left to right.

Table 8B-6. Applicable Electrical Specifications (cont'd)

Video information

a. Single-ended TTL inputs

1. Half-bright: HHB
2. Full-bright: HFB

b. Truth Table

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

c. Dot period is 49.1ns

Power Supplies

a. +5 volts +/-5%

b. +12 volts +/-5%; Imax is 0.085 Amps
(+12 volts used only for CRT filament)

c. +15 volts +/-5%; Imax is .8 Amps average
1.5 Amps peak
.65 Amps typical

(+15 volts used for horizontal and vertical deflection)

DISPLAY DRIVER OPERATION VERIFICATION

The following procedure will help determine if the Display Driver or the CRT is faulty.

a. Verify that the 16 inputs from the CPU board meet the specifications given in table 8B-5 and 8B-6.

b. If there is correct video information on the CRT, perform the Display System Adjustments procedure given in Section V (Adjustments). If any display adjustment cannot be performed, check the typical operating voltages for the CRT given in the table 8B-7. Use a HIGH VOLTAGE PROBE for these measurements.

c. If the voltages to the CRT are correct, the Display Driver is bad and should be replaced.

d. If there is incorrect video information on the CRT, check the display generation circuitry on the CPU board, i.e., CRT Controller, Character ROM, etc.

e. If there is NO video information on the CRT and the typical operating voltages for the CRT (see table 8B-7) are correct, then the CRT and Display Driver are suspect.

Table 8B-7. Typical Operating Voltages For The CRT

NOTE

Unless otherwise specified, voltage values are positive with respect to Grid 1*.

NAME	CRT BASE PIN #	CRT BASE CONNECTOR WIRE COLOR	TYPICAL OPERATING VOLTAGES
Grid 4	7	blue wire	0 to 400 Vdc
Grid 2	6	red wire	500-800 Vdc; Typ. 700 Vdc
Grid 1	5	not connected	
Heater	4	black wire	0 V
Heater	3	brown wire	12 Vdc; 13.2 Vdc Max.
Cathode	2	yellow wire	48-82 V
Grid 1 *	1	green wire	0 V
Anode		red post accelerator lead	8-12 KVdc; Typ. 10 KVdc

8B-57. MNEMONICS.

Signals on the 1630 CPU board have been assigned mnemonics in alphabetical order that describe the active state and function of the signal (see table 8-1 Logic Symbols). A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. A "H" prefix indicates that the function is active in the "high" state; a "L" prefix indicates that the function is active in the "low" state. Table 8B-8 is a listing of the mnemonics used on the schematics.

Table 8B-8. Mnemonics

Mnemonic	Description
20MHZ	20 MHz clock used to derive the 1.27 MHz clock rates of the control timing circuit. This signal also determines the dot rate for character generation.
2MHZ	2 MHz clock from the system timing controller for use by the HP-IB control chip.
4MHZ	4 MHz clock from the system timing controller for use by the HP-IB control chip.
AMS	Address MUX Select. AMS selects which group of RAM address multiplexers control the RAM address lines during an MPU cycle. Multiplexers isolate each functional group (MPU, CRTC, or Graphics) from the RAM address bus HRAA0-7.
ATN	Attention. Ties to HP-IB ATN line via transceiver. Defines type of data on the data bus (addresses/commands or data).
CL0-CLD	Control Latch 0-D. Used by the MPU to control various system functions. See table 8B-1 for the Control Latch Bit assignments.
D0-7	Data outputs from the Character ROM and graphics output buffer to the display data shift register.
DAV	Data Valid. Ties to the HP-IB DAV line via transceiver chip. Indicates availability and validity of data on the data bus.
DIO1-8	Data I/O Bits 1-8. Connected to HP-IB I/O lines via transceiver.
ENDT	Enable Data Transfer. When high, allows data to be written to the acquisition system. When low, allows data to be read from the acquisition system.
EOI	End Of Identify. Bi-directional line that ties to the HP-IB EOI line via transceiver. Indicates end of data transfer or identifies initiation of polling operation.
GS0-4	Ground Sense 0-4. Return ground sense lines adjust the threshold level so that data is sampled with respect to the user's system ground.
HA0-5	Address 0-5. ECL level address lines from the CPU system to the acquisition system.
HACK	Address clock. Increments memory address counters on State Slave.

Table 8B-8. Mnemonics (Cont'd)

Mnemonic	Description
HBI	HP-IB Interrupt to the processor via interrupt mask.
HBNC	Signal from the acquisition system to the rear panel BNC labeled PORT.
HCRA0-7	Character ROM Address 0-7. ASCII code from RAM via ROM.
HCX	Clear X. This signal clears the X counter at the end of a frame.
HCY	Clear Y. This signal clears the Y counter at the end of a line.
HD0-7	Data 0-7. ECL level bi-directional data lines to/from the CPU system and the acquisition system.
HDR0-7	Data Read 0-7. Data read from the acquisition system.
HDRW0-7	Data Read/Write 0-7. Bi-directional CPU system data bus.
HDW0-7	Data Write 0-7. Write only data from the processor.
HF0-5	Formatter 0-5. Waveform information from the waveform formatter used to address the formatter ROM.
HFB	Full Bright. The combination of this signal and the HHB signal determines the brilliance of the video displayed.
HHB	Half Bright. The combination of this signal and the HFB signal determines the brilliance of the video displayed.
HHSYNC	Horizontal Sync. Used by the display driver.
HKBI	Keyboard Interrupt to the processor via the interrupt mask indicating a key was pressed.
HLI	HP-IL Interrupt to the processor via the interrupt mask.
HMR	High Master Reset. This signal will be high until the +5 volt supply exceeds approximately 4.75 volts.
HPA0-20	Physical Address 0-20. This is the CPU systems Physical Address bus.
HRA0-3	Raster Addresses 0-3. Used by the Character ROM as the column address for a character.
HRAA0-7 (C,G,M)	RAM Address 0-7. Only one of three functional groups are allowed to address RAM at a given time. The functional groups are: CRTC, Graphics, or MPU. See figure 8B-4 for timing waveforms.
HRAD0-7	RAM Data 0-7.

Table 8B-8. Mnemonics (Cont'd)

Mnemonic	Description
HR/LW	High Read/Low Write. ECL level read/write control signal to the acquisition system.
HRTC	Real Time Clock. This signal is an interrupt from the system timing controller. The processor syncs on this interrupt for a real time clock display.
HR/WL	High Read/Write Low. Signal from the I/O decoding circuitry to the CRT Controller.
HTCK	High Timing Clock. ECL timing clock for under 5 MHz.
HTMC	Timing Measurement Complete. Indicates a measurement has been completed and that acquisition memory can be read by the processor.
HVSYNC	Vertical Sync. Used by the display driver.
IFC	Interface Clear. Ties to the HP-IB IFC line via transceiver. Places I/O system into known quiescent (idle) state.
KBC0-7	Keyboard Column 0-7. Return sense lines to the keyboard controller.
KBR1-6	Keyboard Row 1-6. Keyboard stimulus lines from the keyboard controller.
LACK	Complement of HACK.
LCAS	Column Address Strobe. Needed for RAM data transfers.
LCRE	Character ROM Enable.
LCS0-7	Chip Select 0-7. Selects which ROM is being addressed.
LECB	Enable CRTC Buffer. When low, the CRTC buffer is enabled allowing RAM to supply data to the CRT Controller (CRTC). When high, the processor supplies data to the CRTC.
LEFD	Enable Full-field Display. When low, this signal disables addressing of the Character ROM and enables the graphics address multiplexers. This allows scanning of the full-field graphics area.
LGBE	Graphics Buffer Enable. When asserted, the graphics information is loaded into the display data shift register.
LHBS	HP-IB I/O Strobe. HP-IB chip enable from the macro decoder.
LHLR	HP-IL Read. Processor controls HP-IL read operations via the macro decoder.
LHLW	HP-IL Write. Processor controls HP-IL write operations via the macro decoder.
LIRQ	Interrupt Request. Signal from the interrupt mask to the processor.

Table 8B-8. Mnemonics (Cont'd)

Mnemonic	Description
LIS0-9	I/O Strobe 0-9. Signals from the micro decoder used for read\write operations. See table 8B-4, micro I/O physical address-to-function.
LLX	Load X Counter. When low the X counter is loaded with 07 hex.
LMCI	Measurement Complete Interrupt. Interrupt to the processor via the interrupt mask.
LMR	Low Master Reset. This signal will be low until the +5 volt supply exceeds approx. 4.75 volts.
LRA	Register Access. Indicates that the MMUs registers are being accessed by the processor.
LRAS	Row Address Strobe. Needed for RAM data transfers.
LR/HW	Low Read/High Write. Control signal from the I/O decoding circuitry used to form HR/LW.
LRST	Low Reset. This signal will be low until the +5 volt supply exceeds approx. 4.75 volts.
LSTB	Low Strobe. ECL level control signal to the acquisition system that is used with HR/LW to indicate a data transfer.
LTCK	Low Timing Clock. ECL timing clock for under 5 MHz.
LWE	Write Enable. When asserted, allows data to be written into RAM.
LW/HR	Low Write/High Read. Indicates the direction in which data is being transferred on the HDRW0-7 data bus.
MA0-13	Memory Address 0-13. Used for RAM refreshing.
NDAC	Not Data Accepted. HP-IB handshake line indicating acceptance of data by all devices.
HRFD	Not Ready For Data. HP-IB handshake line indicating that devices are ready to accept data.
PH0-PH7	Phase 0-7. Each phase is a 1.27 MHz signal from the control timing circuit. Adjacent phases are separated by 50 mS.
PH1N-7N	Phase 1-7 Not. Complement of the PH0-7 signals.
REN	Remote Enable. Ties to HP-IB REN via transceiver. Enables alternate devices to provide programming data.
RXD0-1	Receive Data 0-1. HP-IL return data from the previous device.

Table 8B-8. Mnemonics (Cont'd)

Mnemonic	Description
SRQ	Service Request. Ties to the HP-IB SRQ line via transceiver. Indicates a need for service; causes an interrupt of the current sequence to the processor.
THR0-4	Threshold 0-4. An adjustable sample threshold for the pod hybrid chip comparator.
TXD0-1	Transmit Data 0-1. HP-IL transmit information to the next device.
VR	Voltage Reference. A precision +5.00 volt reference supply.
X0-9	X coordinates for the full-field graphics display area.
Y4-9	Y coordinates for the full-field graphics display area.

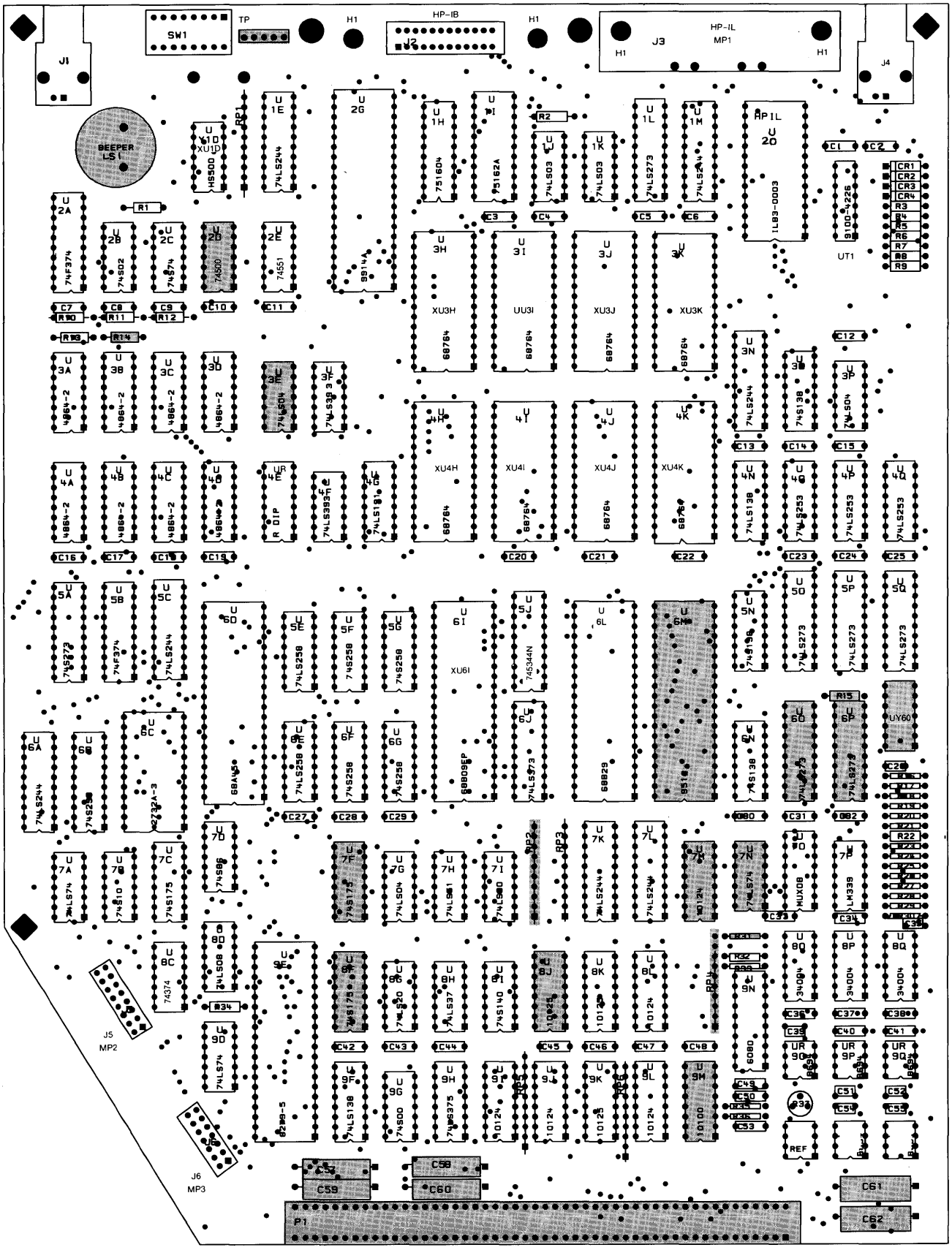


Figure 8B-11. CPU Component Locator (1 of 7)

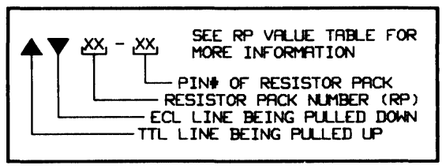
NOTE I

CPU BOARDS 01630-66503 AND 01630-66512 ORIGINALLY HAVE U6M PIN 25 AS "NC". BOARDS MAY BE MODIFIED TO RUN IN A 1630G AND HAVE PIN 25 JUMPERED TO +5V.

POWER CONNECTIONS

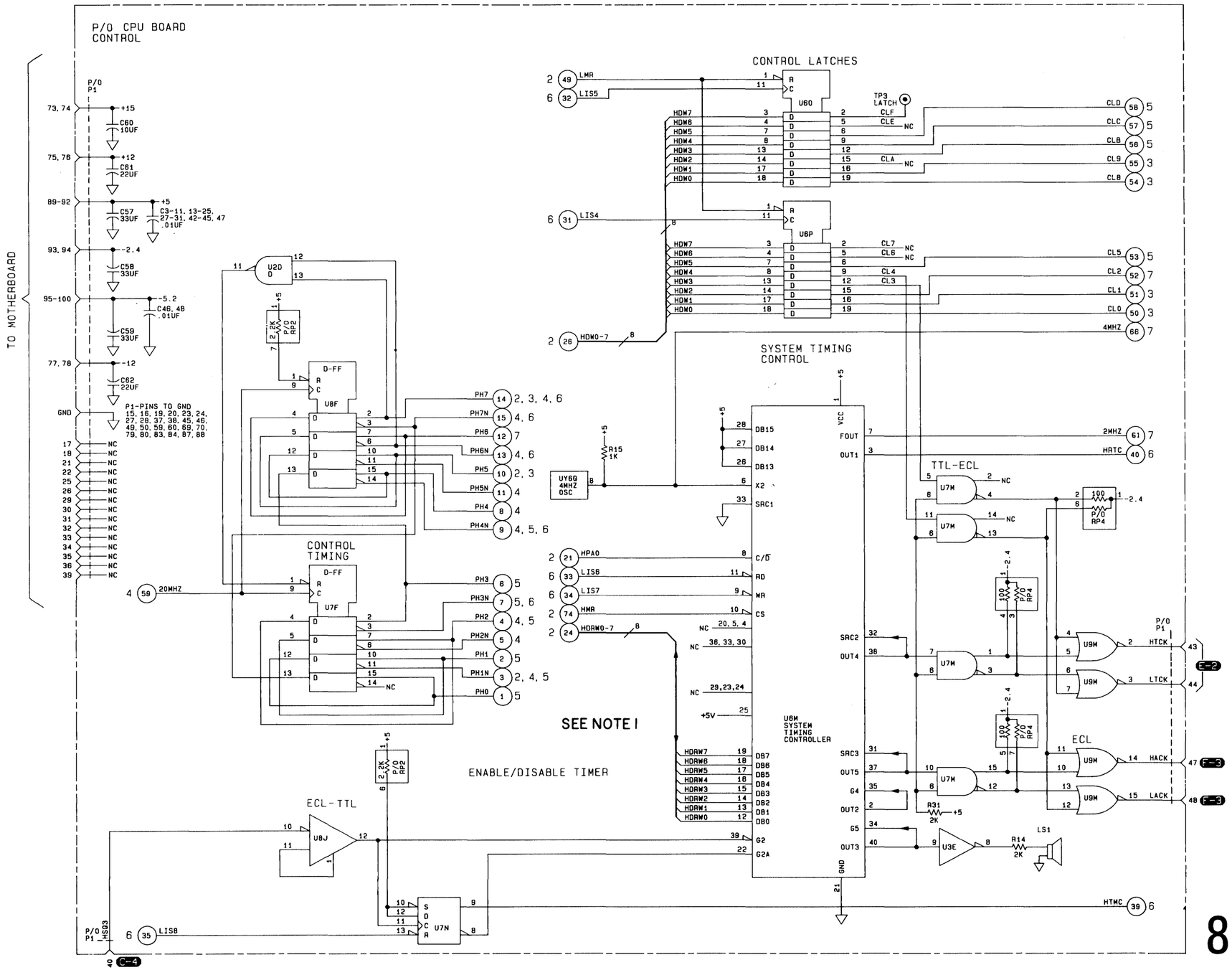
SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U6O,P
+5 GND	14 7	U2D,3E,7N
+5 GND	1 21	U6M
+5 GND	16 8	U7F,8F
+5 -5.2 GND	9 8 16	U7M,8J
+5 -5.2 GND	1 8 16	U9M

RESISTOR PACK DESCRIPTIONS:



PARTS ON THIS SCHEMATIC

U2D,3E,6M,O,P, U7F,M,N,8F,J,9M C3-11,13-25,27-31, 42-48,57-62 LS1 R14,15,31 RP2,4 TP3	



8B-1

Figure 8B-12. CPU Schematic (1 of 8)

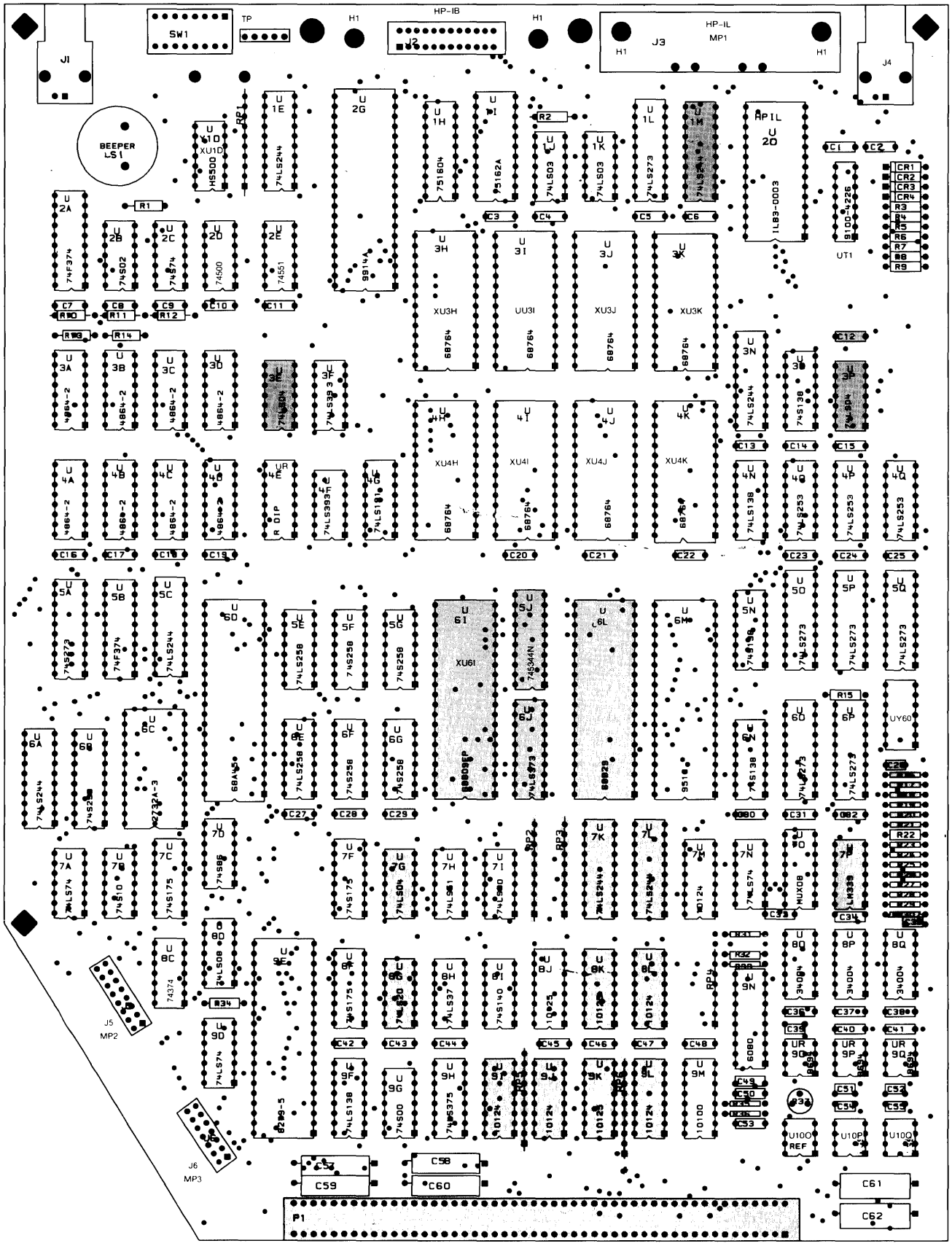
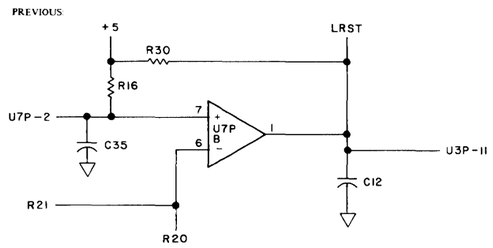


Figure 8B-11. CPU Component Locator (2 of 7)

NOTE 1

FOR CPU BOARD 01630-66503, THE FOLLOWING CIRCUIT CHANGES SHOULD BE MADE.

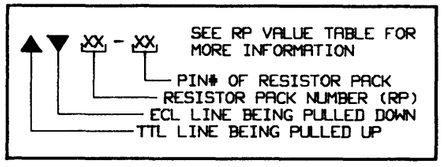
PREVIOUS



IC DEVICE POWER CONNECTIONS

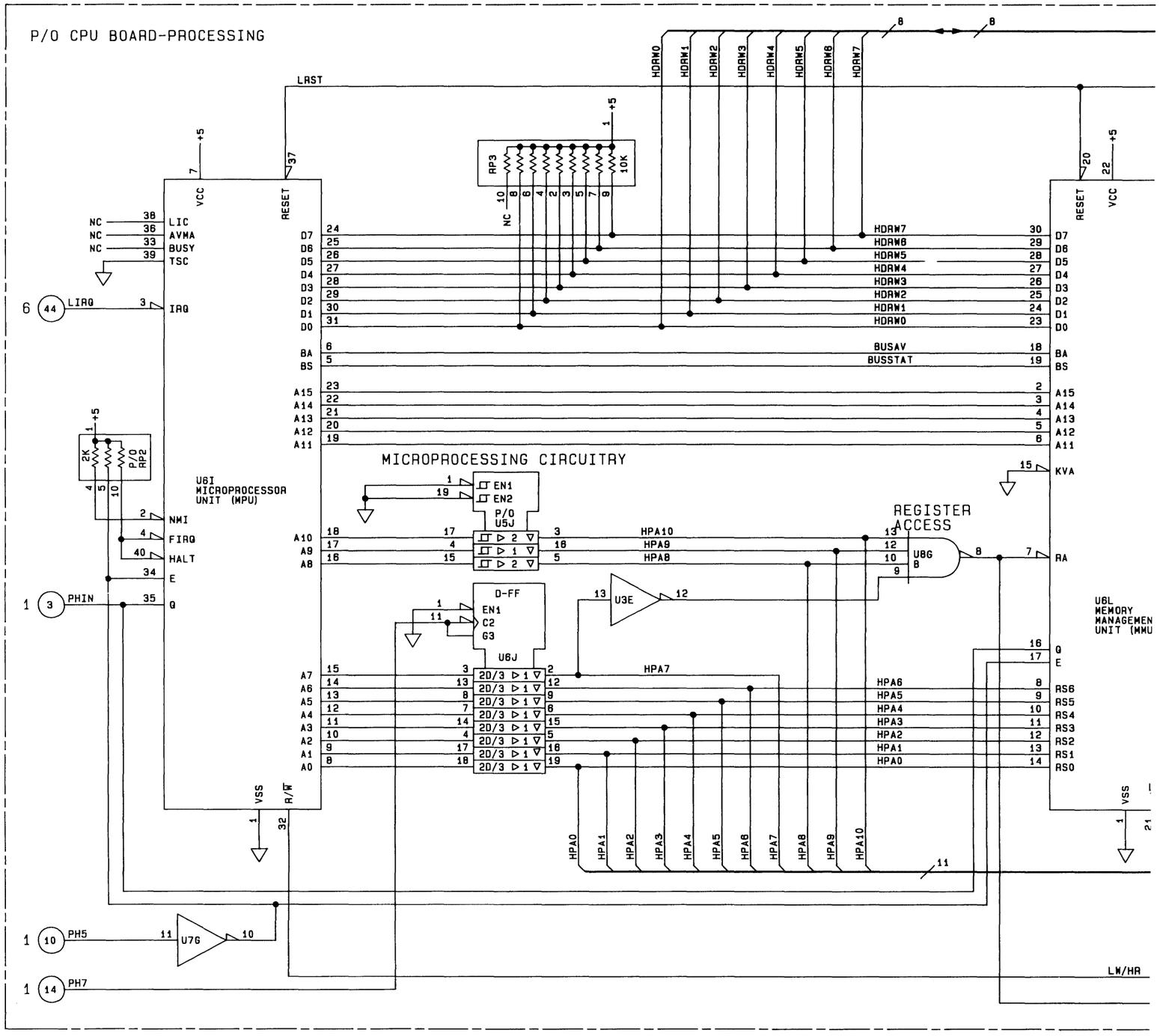
SUPPLY	PIN NO.	IC GROUP
+5V GND	20 10	U1M,5J,6J,7K, U7L
+5V GND	14 7	U3E,3P,7G,8G
+5V GND	7 1	U6I
+5V GND	22 1	U6L
+12V GND	3 12	U7P
+5V -5.2V GND	9 8 16	U8K,8L,9I,9J, U9K,L

RESISTOR PACK DESCRIPTIONS:



PARTS ON THIS SCHEMATIC

U1M,3E,P,5J,6I,J U6L,7G,K,L,P, U8G,K,L,9I-L C12,26,33,35 R16-21,26,30 RP2,3,5,6	



DATA WRITE BUFFER

DATA WRITE TTL-ECL

DATA READ

DATA READ BUFFER

DATA

SEE NOTE I

POWER UP MASTER RESET

TTL-ECL

ACQUISITION DATA

ECL ACQUISITION INTERFACE

ADDRESS AND CONTROL

U6L MEMORY MANAGEMENT UNIT (MMU)

Figure 8B-.

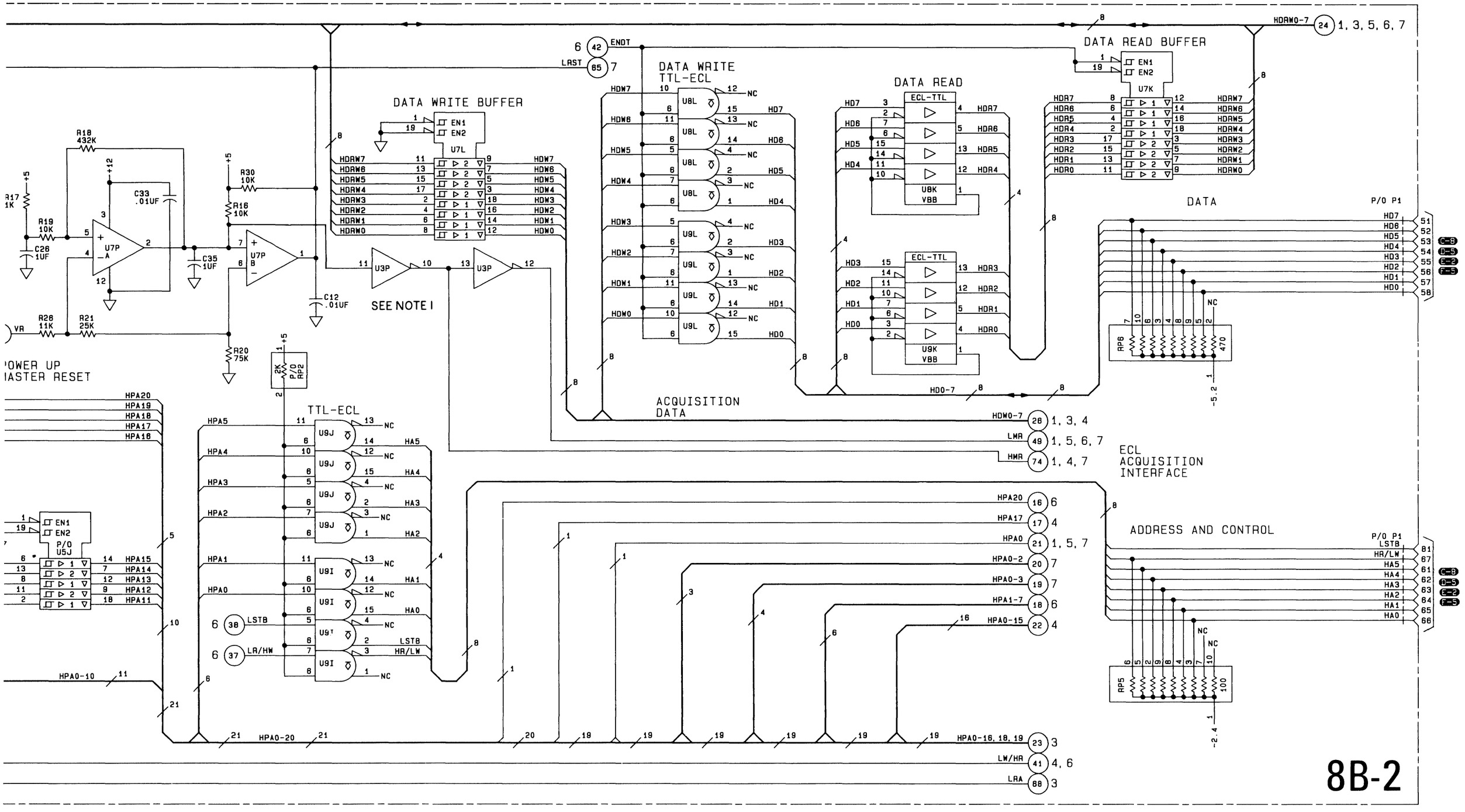


Figure 8B-12. CPU Schematic (2 of 8)

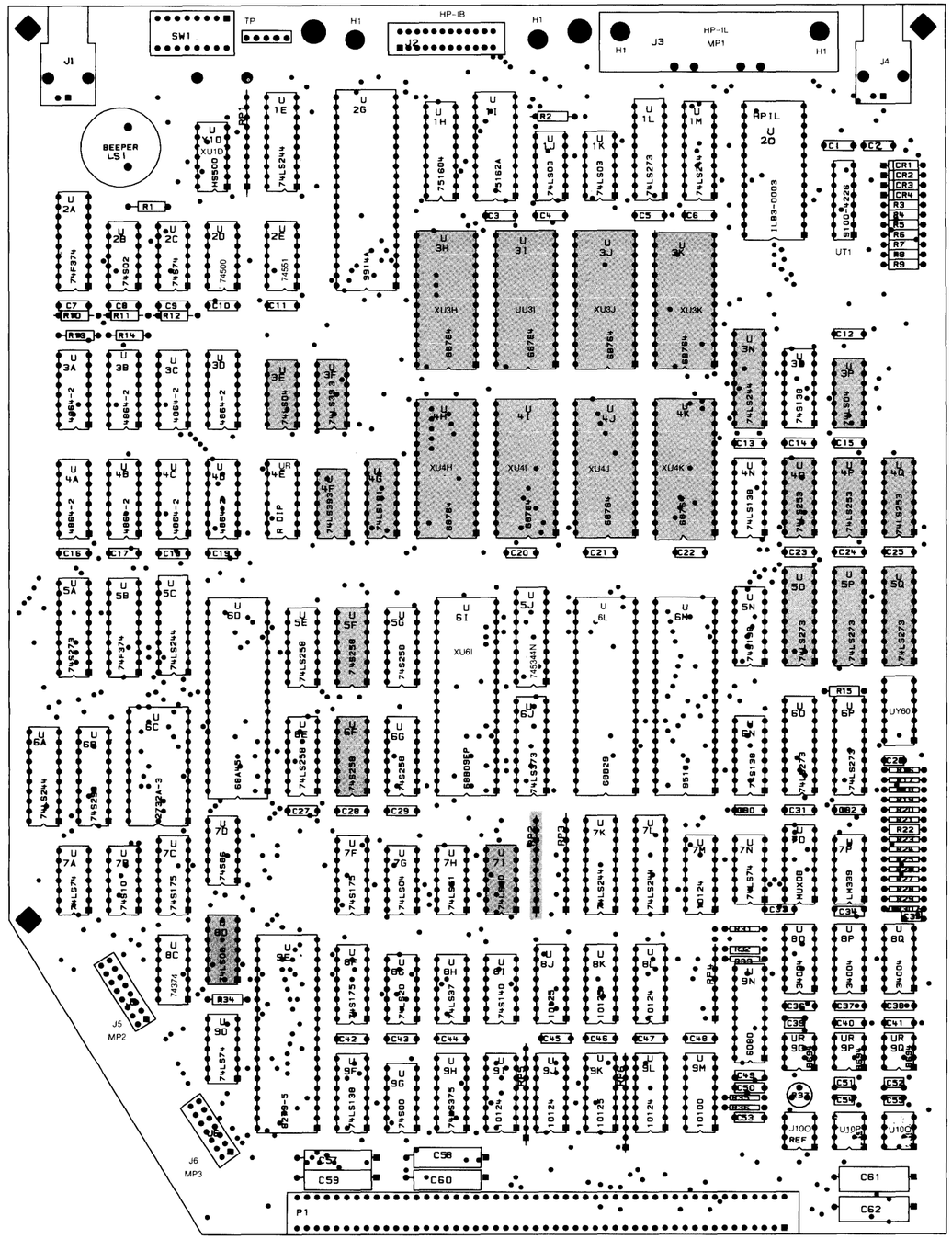
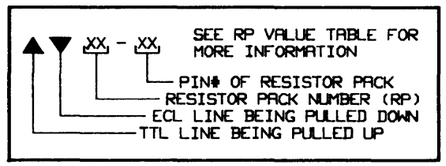


Figure 8B-11. CPU Component Locator (3 of 7)

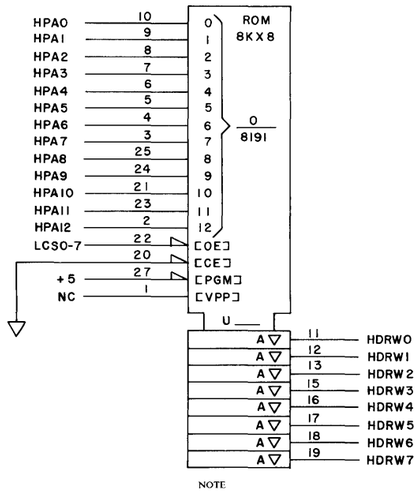
IC DEVICE
POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5V GND	14 7	U3E,3F,3P,4F, U7I,8D
+5V GND	28 14	U3H,3I,3J,3K, U4H-K
+5V GND	20 10	U3N,5O-Q
+5V GND	16 8	U4G,4O-Q,5F,6F

RESISTOR PACK DESCRIPTIONS:



NOTE A - ROM Information for U3H-K and U4H-U4K

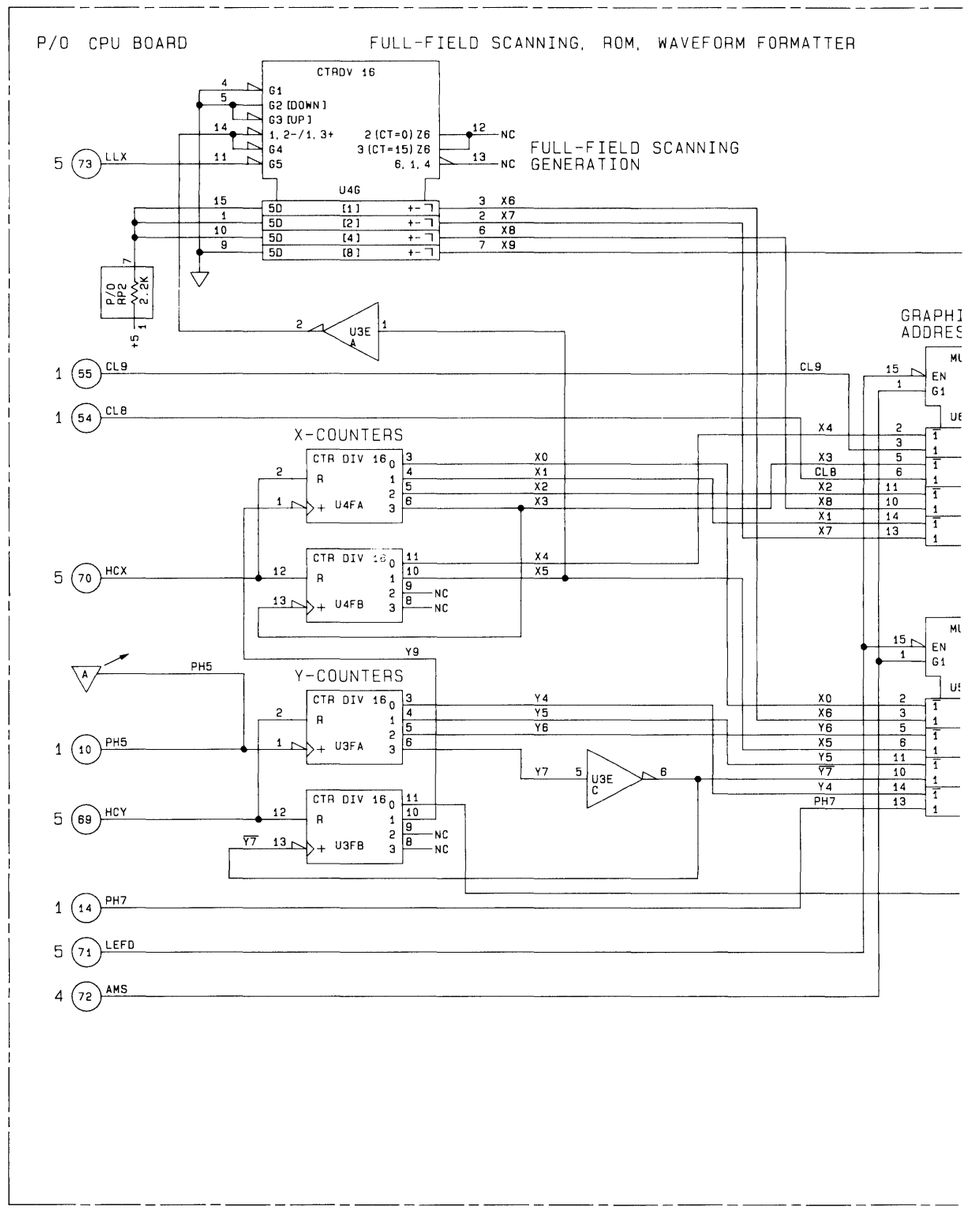


NOTE

Pin 26 of an Intel 2764 EPROM is not connected internally for pin compatability with an Intel 2732 EPROM.

PARTS ON THIS SCHEMATIC

U3E,F,H-K,N,P, U4F-K,4O-Q,5F, U5O-Q,6F,7I,8D RP2	



RMATTER

NOTE
ROMS U3H, I, J AND U4H-U4K SHARE THE SAME
ADDRESS AND DATA LINES. SEE NOTE A FOR ROM INFORMATION.

ROM SELECTOR

PROGRAM ROMS

GRAPHICS ADDRESS MUX

WAVEFORM FORMATTER

FORMATTER ROM

SEE NOTE A

Figure 8B-

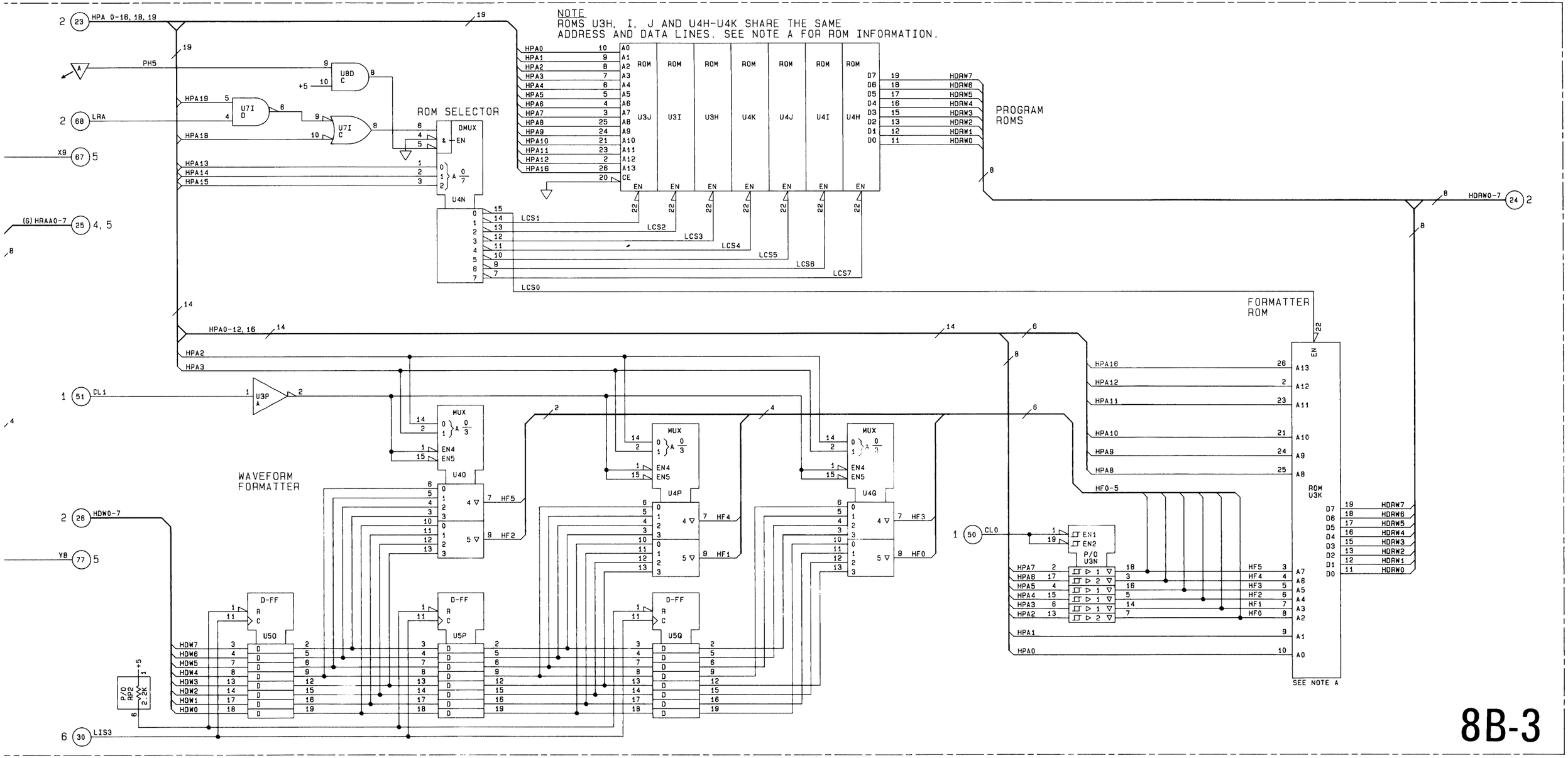


Figure 8B-12. CPU Schematic (3 of 8)

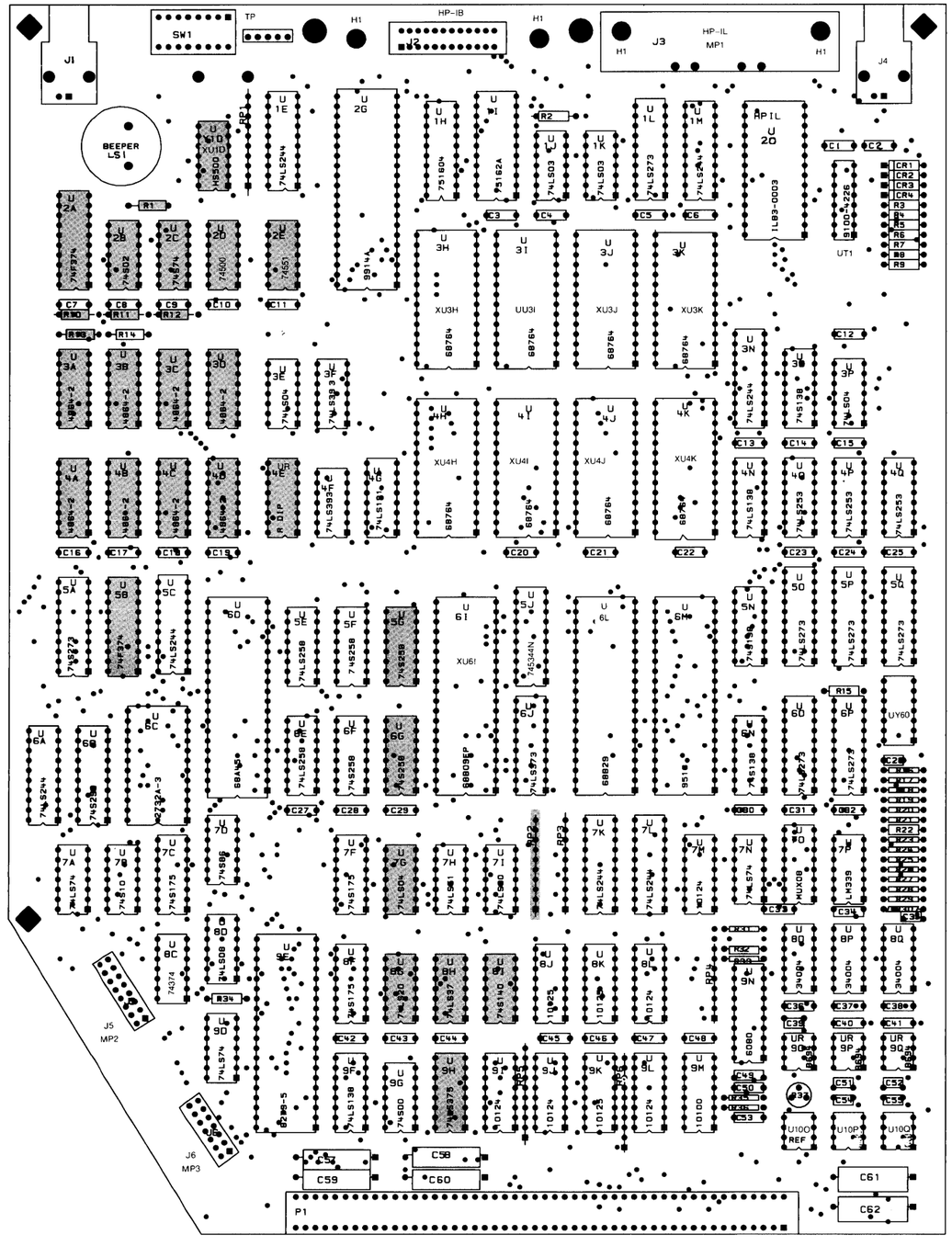
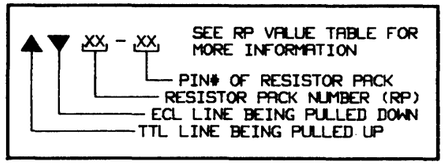


Figure 8B-11. CPU Component Locator (4 of 7)

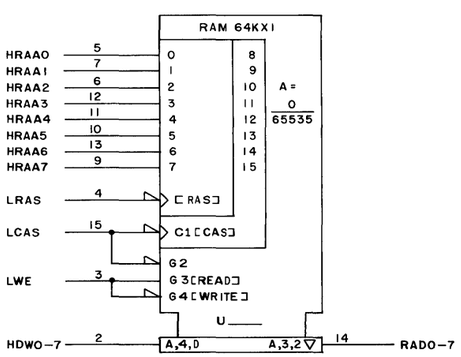
IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U2A,5B
+5 GND	14 7	U2B-E,7G,8G-I
+5 GND	16 8	U5G,6G,9H
+5 GND	8 16	U3A-D,4A-D

RESISTOR PACK DESCRIPTIONS:



NOTE 1 - RAM Information for U3A-D and U4A-U4D

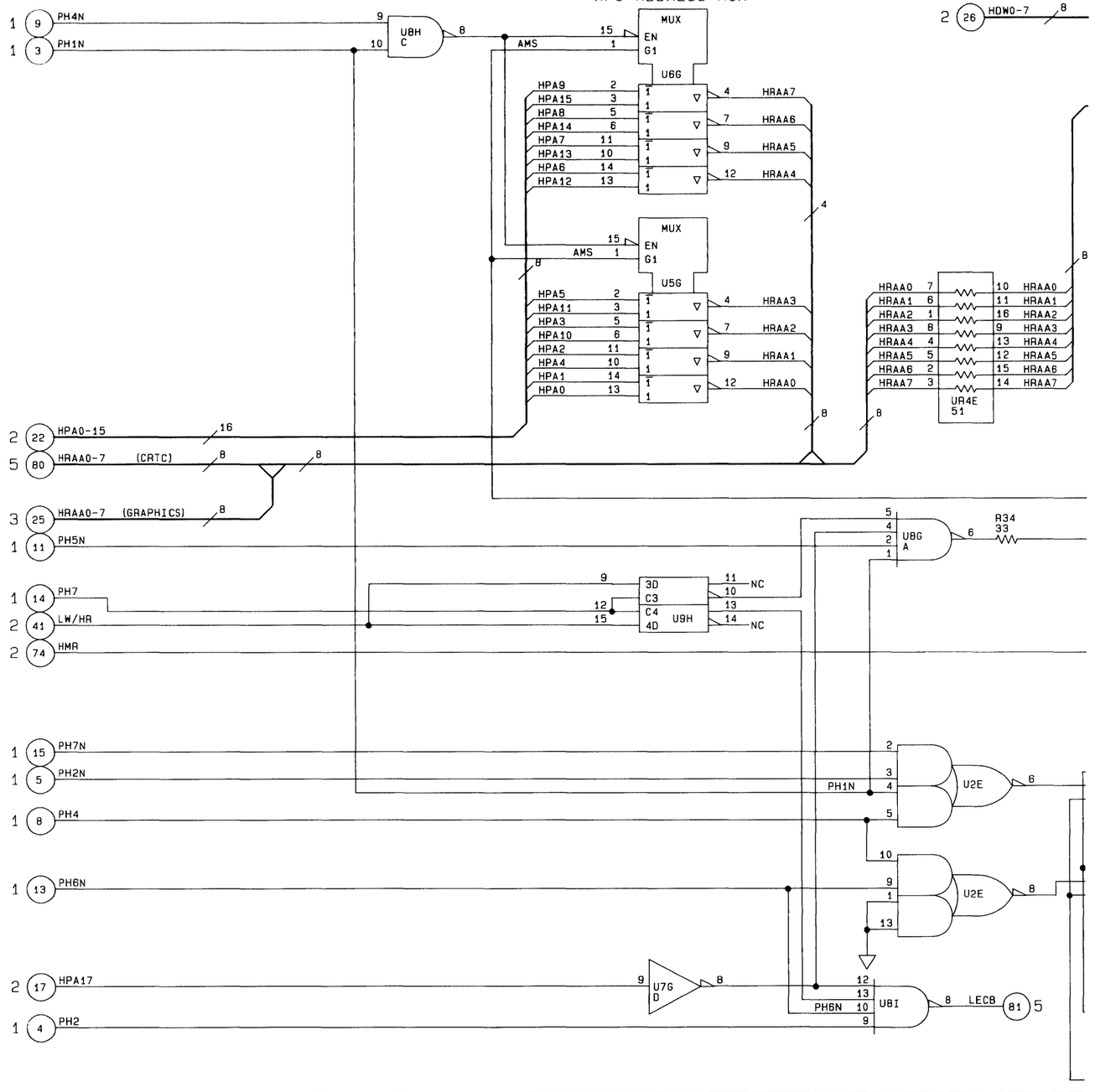


PARTS ON THIS SCHEMATIC

U2A-E,3A-D,4A-D, U5B,G,6G,7G, U8G-I,9H R1,10-13,34 RP2 UR4E AND UY1D	

P/O CPU BOARD - RAM TIMING

MPU ADDRESS MUX



RAM TIMING

MPU ADDRESS MUX

U8H C

MUX EN G1 U6G

HPA9 HPA15 HPA8 HPA14 HPA7 HPA13 HPA6 HPA12 → HRAA7 HRAA6 HRAA5 HRAA4

MUX EN G1 U5G

HPA5 HPA11 HPA3 HPA10 HPA2 HPA4 HPA1 HPA0 → HRAA3 HRAA2 HRAA1 HRAA0

AMS

HRAA0 HRAA1 HRAA2 HRAA3 HRAA4 HRAA5 HRAA6 HRAA7 — UR4E 51 — HRAA0 HRAA1 HRAA2 HRAA3 HRAA4 HRAA5 HRAA6 HRAA7

(CRTC)

GRAPHICS)

U8G A — R34 33

U9H 3D C3 C4 4D — NC

U7G D — U8I — PH6N — LECB (81) 5

U2E — PH1N

U2CB — U2CA — R12 2K +5 — 2.2K P/O RP2

RAM TIMING CONTROL

2 (26) HDW0-7

HDW0 HDW1 HDW2 HDW3 HDW4 HDW5 HDW6 HDW7

HRAA0-7

LWE LRAS LCAS

A0-7 DIN D0 D1 D2 D3 D4 D5 D6 D7 WE RAS CAS DOUT U3A U3B U3C U3D U4A U4B U4C U4D

RAD0 RAD1 RAD2 RAD3 RAD4 RAD5 RAD6 RAD7

RAM SEE NOTE 1

RAM DATA LATCH

FF EN C1 U5B

RAD0 RAD1 RAD2 RAD3 RAD4 RAD5 RAD6 RAD7 → HRAD0 HRAD1 HRAD2 HRAD3 HRAD4 HRAD5 HRAD6 HRAD7

HRAD0-7 (82) 5

R10 33 LCAS

AMS (72) 3, 5

HMR

R13 33

MASTER CLOCK

UY10 40.72 MHZ OSC +5

FF EN C1 U2A

R1 2K +5

R11 2K +5

LRAS LCAS 20MHZ

U2B B U2B A U2B D U2D C U2B B U2D B U2D A

20MHZ (59) 1, 5

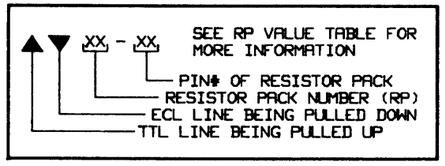
8B-4

Figure 8B-12. CPU Schematic (4 of 8)

IC DEVICE POWER CONNECTIONS

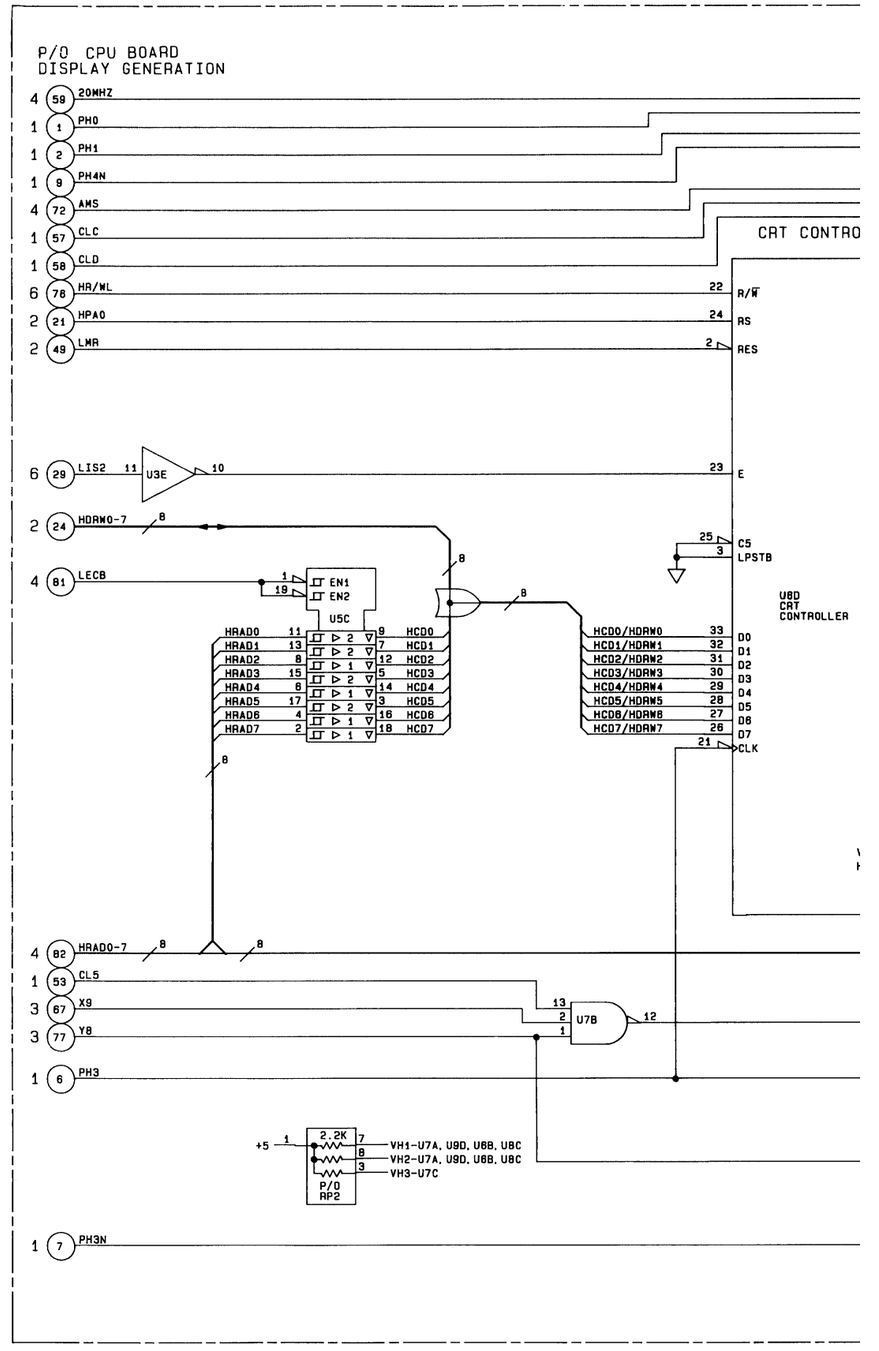
SUPPLY	PIN NO.	IC GROUP
+5 GND	14 7	U3E,7A,B,D,G,I, U8C,D,H,9D,G
+5 GND	20 10	U5A,C,6A,B
+5 GND	16 8	U5E,6E,7C
+5 GND	24 12	U6C
+5 GND	20 1	U6D

RESISTOR PACK DESCRIPTIONS:



PARTS ON THIS SCHEMATIC

U3E,5A,C,E,6A-E, U7A-D,G,I,8C,D,H, U9D,G J5 RP2	



CRT CONTROL

U8D
CRT
CONTROLLER

R/W
RS
RES
E
C5
LPSTB
D0
D1
D2
D3
D4
D5
D6
D7
CLK

MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13

RA0
RA1
RA2
RA3
RA4
NC

HRA0
HRA1
HRA2
HRA3

CLC
CCD

CRTC ADDRESS MUX

U5E
U8E
MUX
EN
G1
AMS
AM5

MA1
MA0
MA2
MA4
MA3
MA10
MA5
MA11
MA6
MA12
MA7
MA13
MA8
MA9

HRAA0
HRAA1
HRAA2
HRAA3
HRAA4
HRAA5
HRAA6
HRAA7

(CRTC) HRAA0-7

PH1

LEFD

U5A
D-FF
R
C

HRAD0
HRAD1
HRAD2
HRAD3
HRAD4
HRAD5
HRAD6
HRAD7

HCRA0
HCRA1
HCRA2
HCRA3
HCRA4
HCRA5
HCRA6
HCRA7
HCRA8

U8D

LCRE

CHARACTER
ROM

ROM
4K X 8
0
4095

HRA0
HRA1
HRA2
HRA3

U8C
EN

GRAPHICS
OUTPUT BUFFER

U6A
EN1
EN2

U8D

U70

DISPLAY DATA
SHIFT REGISTER

SR68
3EN13
U8B
C4/1→/2
M 0/3

VH1
VH2
VH3
20MHZ

U7D
A

1, 4D
3, 4D
5, 13
Z5
6, 13
Z6
12, 13
Z12
2, 4D

HEV

U7B
A

U7D
B

DISPLAY
CONTROL FF

PH1N

U7C
D-FF

HCRA7
CUR
HEV

NC

Truth Table for Video Information

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

DISPLAY
DATA LATCHES

U8CB
U8CA
U9DA
S
D
C
R

U8H
CLB

U7G
F

U7AB
U7AA
U9DB

LGBE
LCRE
HEV

DE

U7G
U7I
U8D
U9G

DISPLAY CONTROL

PH2

LEFD
HCX
LLX
HCY

Figure 8B-

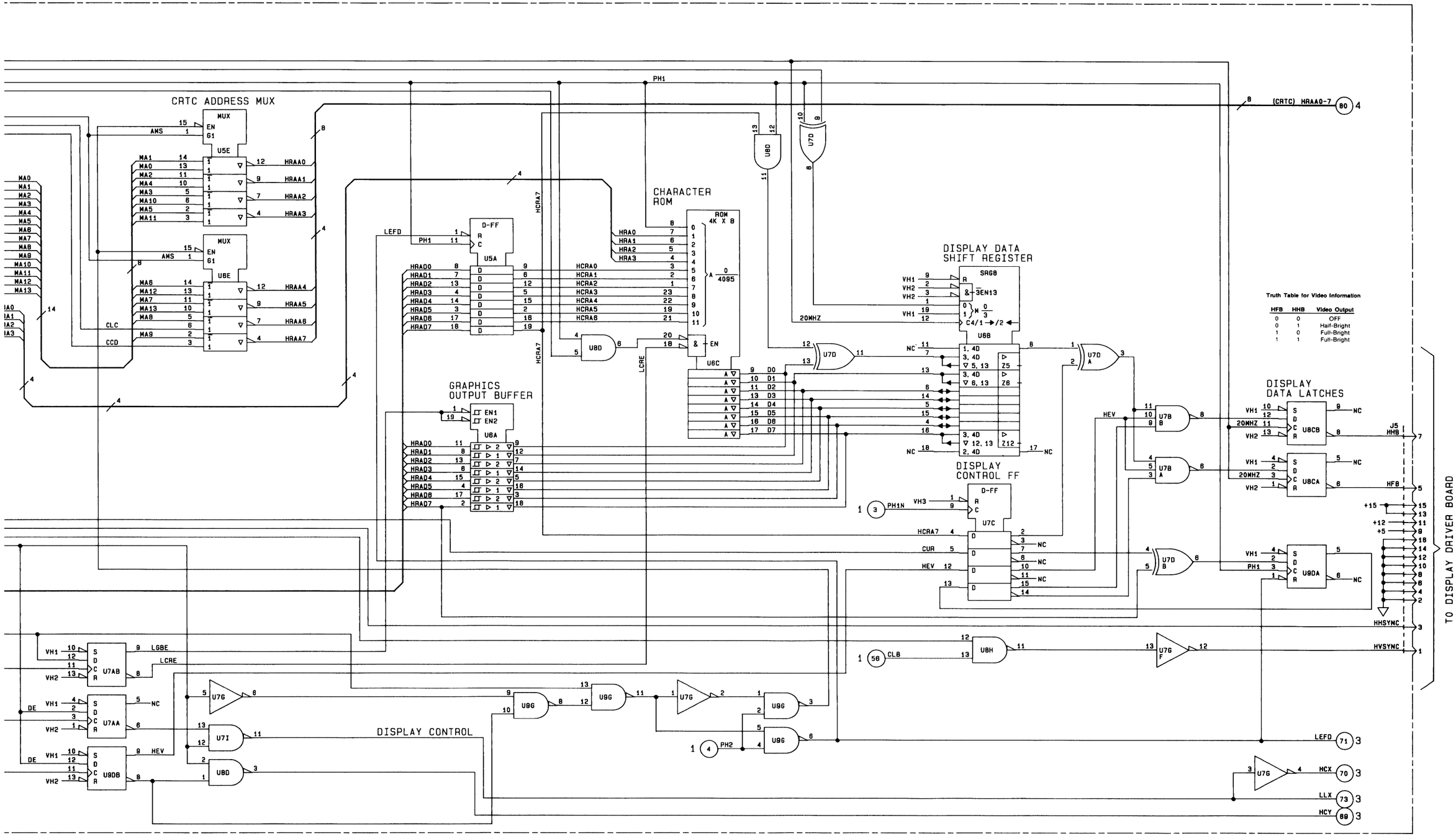


Figure 8B-12. CPU Schematic (5 of 8)

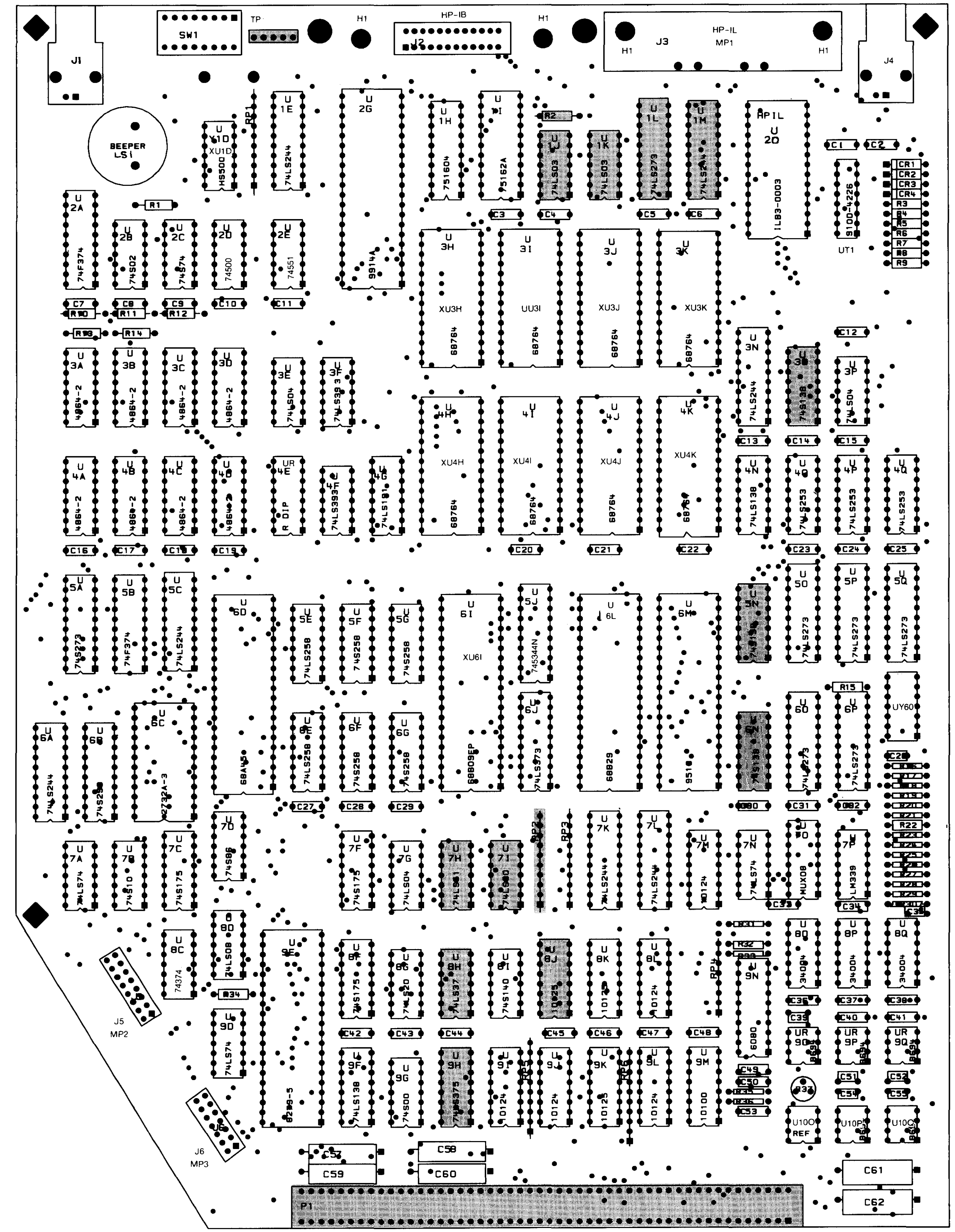
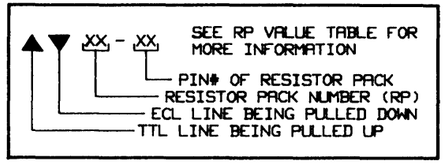


Figure 8B-11. CPU Component Locator (6 of 7)

IC DEVICE POWER CONNECTIONS

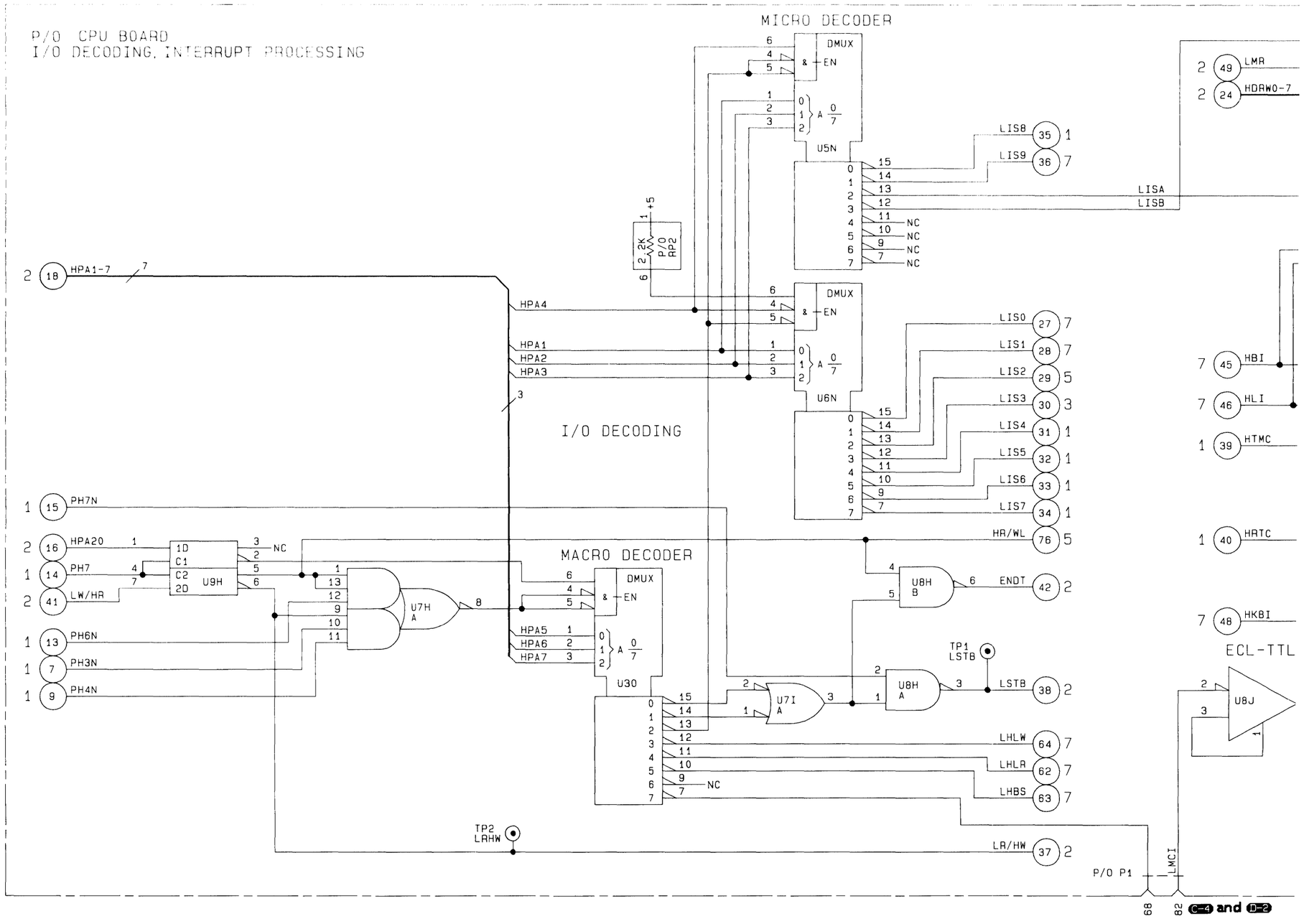
SUPPLY	PIN NO.	IC GROUP
+5 GND	14 7	U1J,K,7H,I,8H
+5 GND	20 10	U1L,1M
+5 GND	16 8	U30,5N,6N,9H
+5 -5.2 GND	9 8 16	U8J

RESISTOR PACK DESCRIPTIONS:



PARTS ON THIS SCHEMATIC

U1J-M,30,5N,6N, U7H,I,8H,J,9H R2 RP2 TP1,2	



MICRO DECODER

DMUX

U5N

U6N

LIS8 35 1
LIS9 36 7
LIS0 27 7
LIS1 28 7
LIS2 29 5
LIS3 30 3
LIS4 31 1
LIS5 32 1
LIS6 33 1
LIS7 34 1
HA/WL 76 5
ENDT 42 2
LSTB 38 2
LHLW 64 7
LHLR 62 7
LHBS 63 7
LA/HW 37 2
LISA
LISB
NC
+5
2.2K R/O RP2
HPA4
HPA1
HPA2
HPA3
I/O DECODING
MACRO DECODER
HPA5
HPA6
HPA7
U30
U8H A
U8H B
U7I A
TP1 LSTB
TP2 LRHW
P/O P1
LMCI
68
82
C-4 and D-2

LISB
2 49 LMR
2 24 HDRW0-7 8
HDRW7 HDRW6 HDRW5 HDRW4 HDRW3 HDRW2 HDRW1 HDRW0

READ INTERRUPT STATUS BUS
EN1
EN2
U1M

WRITE INTERRUPT MASK LATCH
D-FF
U1L

INTERRUPT MASK
U1K D
U1K A
U1K C
U1K B
U1J A
U1J D
U1J B
U1J C
R2 2K
LIRQ 44 2

7 45 HBI FROM HP-IB CONTROLLER
7 46 HLI FROM HP-IL CONTROLLER
1 39 HTMC FROM ENABLE/DISABLE TIME MEASUREMENT COMPLETE
FROM ACQUISITION MEASUREMENT COMPLETE
1 40 HRTC FROM REAL TIME CLOCK (SYSTEM TIMING CONTROL)
NOT IMPLEMENTED
7 48 HKBI FROM KEYBOARD CONTROLLER
NOT IMPLEMENTED

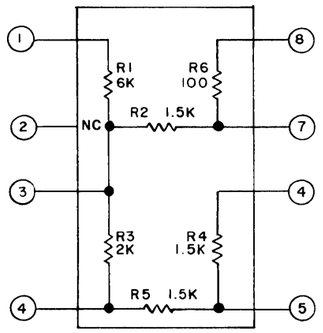
ECL-TTL
U8J

INTERRUPT PROCESSING

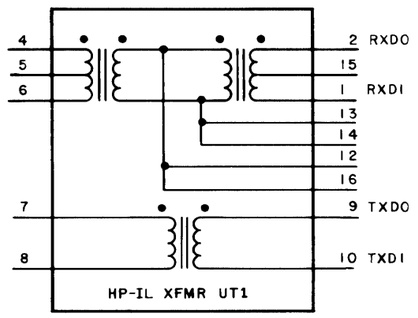
8B-6

Figure 8B-12. CPU Schematic (6 of 8)

NOTE 1



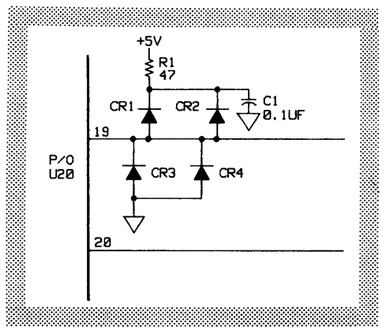
NOTE 2



FUNCTIONAL DIAGRAM OF UT1

NOTE 3

THE PARTS COVERED IN THIS NOTE WERE ADDED TO PREVENT AN ESD (ELECTROSTATIC DISCHARGE) PROBLEM. THE 01630-66512 CPU BOARD HAS THESE PARTS PLUS U20 MOUNTED ON AN ADDITIONAL SMALL BOARD PLUGGED INTO THE SOCKET FOR U20. LATER CPU BOARDS WILL HAVE THE PARTS ON THE MAIN BOARD.

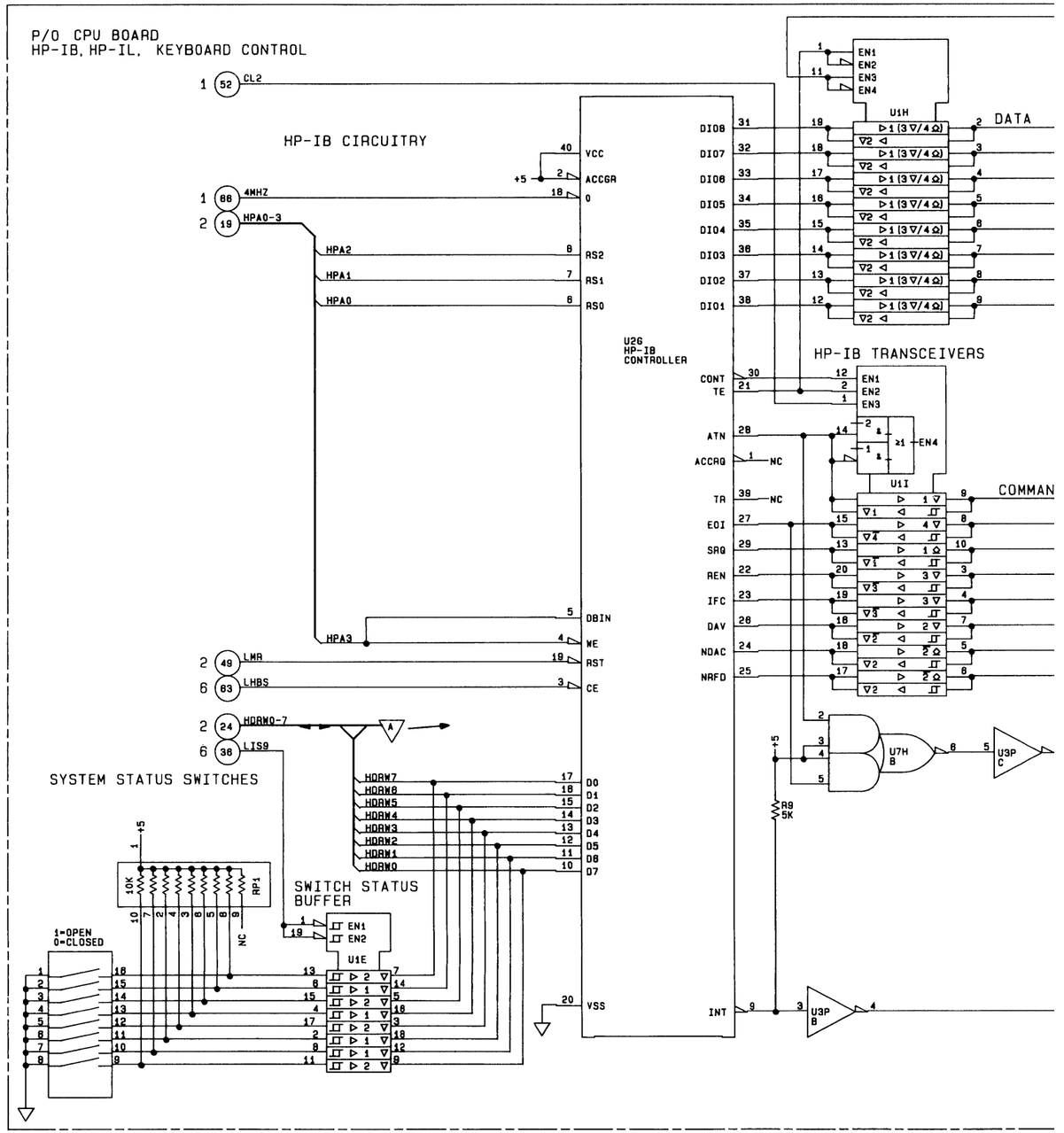


IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U1E,1H
+5 GND	14 7	U3P,7H,8I
+5 -5.2 GND	9 8 16	U8J
+12 -12 GND	20 17 10	U9N
+5 GND	22 11	U1I
+5 GND	40 20	U2G,9E
+12 -12 GND	13 3 14	U70
+12 GND	3 12	U7P
+12 -12	4 11	U80,8P,8Q
+5 GND	16 8	U9F
+12 GND	2 4	U100
+5 GND	1 10	U20

RESISTOR PACK DESCRIPTIONS:

PARTS ON THIS SCHEMATIC	
C1,2,32,34,36-41, 49-56 CR1-4 J1-4,6 R3-9,22-25,27-29, 32,33,35-37 RP1,2 SW1	TP4 UR90,9D,9Q,10P,10Q UT1 U1E,H,I,2G,O,3P, U7H,O,P,8I,J, U8O-Q,9E,F,N, U100



TO/FROM KEYBOARD B-8

J8

KBR1 KBR2 KBR3 KBR4 KBR5 KBR6 KBC7 KBC6 KBC5 KBC4 KBC3 KBC2 KBC1 KBC0

KEYBOARD SCANNING

THRESHOLD DAC

PROBE THRESHOLD DRIVERS

PROBE SELECT

VOLTAGE REFERENCE

DATA

COMMANDS

TRANSCEIVERS

TO/FROM HP-IB

BNC OUTPUTS

ECL-TTL

U8E KEYBOARD CONTROLLER

ROW DMUX

U9F

U9N

U8Q

U8P

U7P

U20 HP-IB CONTROL

HP-IL

XFMR UT1

SEE NOTE 3

SEE NOTE 2

U100 VOLTAGE REGULATOR

SEE NOTE 1 FOR UR8Q

SEE NOTE 1 FOR UR10Q

SEE NOTE 1 FOR UR8P

SEE NOTE 1 FOR UR10P

SEE NOTE 1 FOR UR8O

TO/FROM HP-IL

Figure 8B-

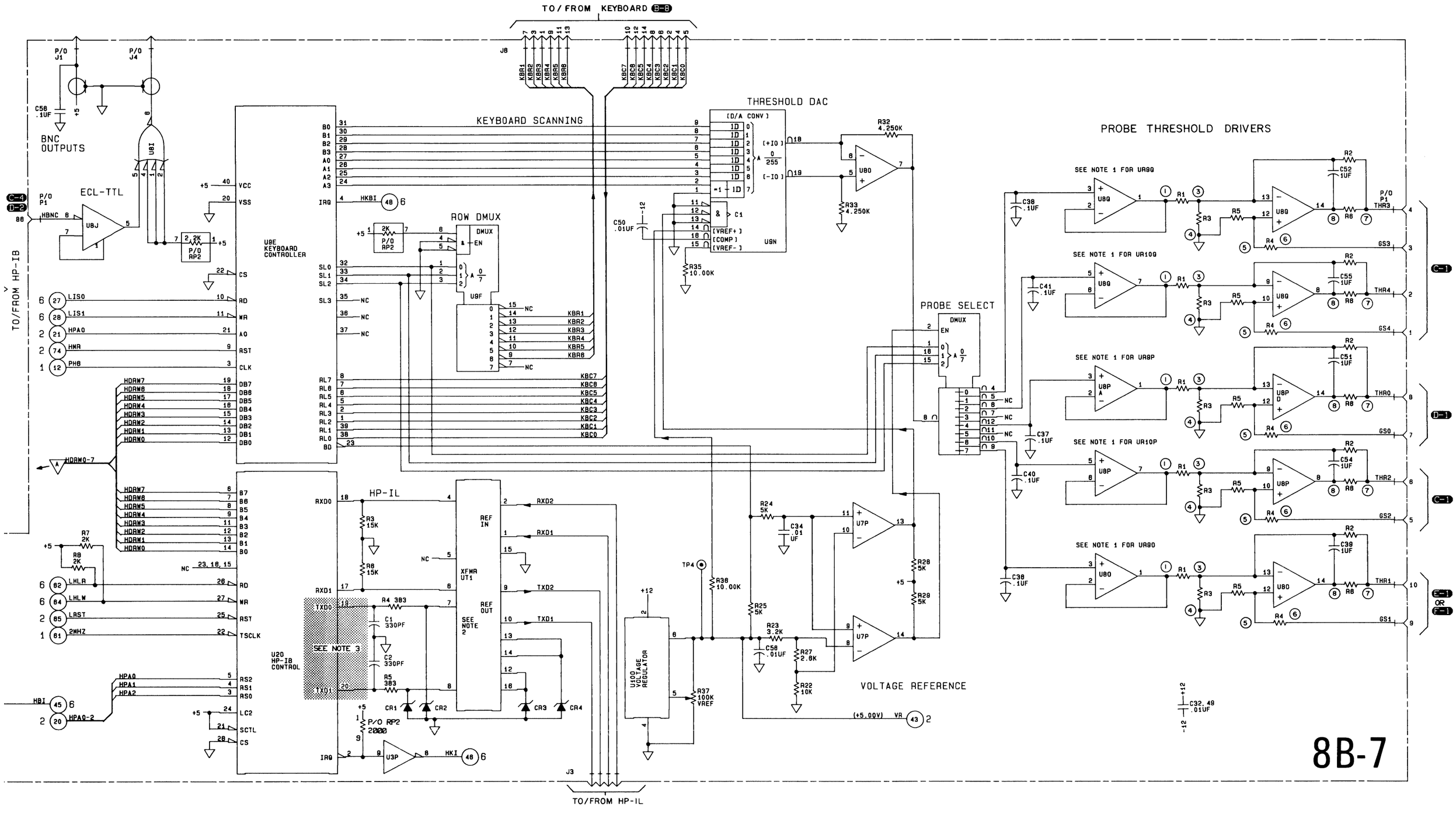


Figure 8B-12. CPU Schematic (7 of 8)

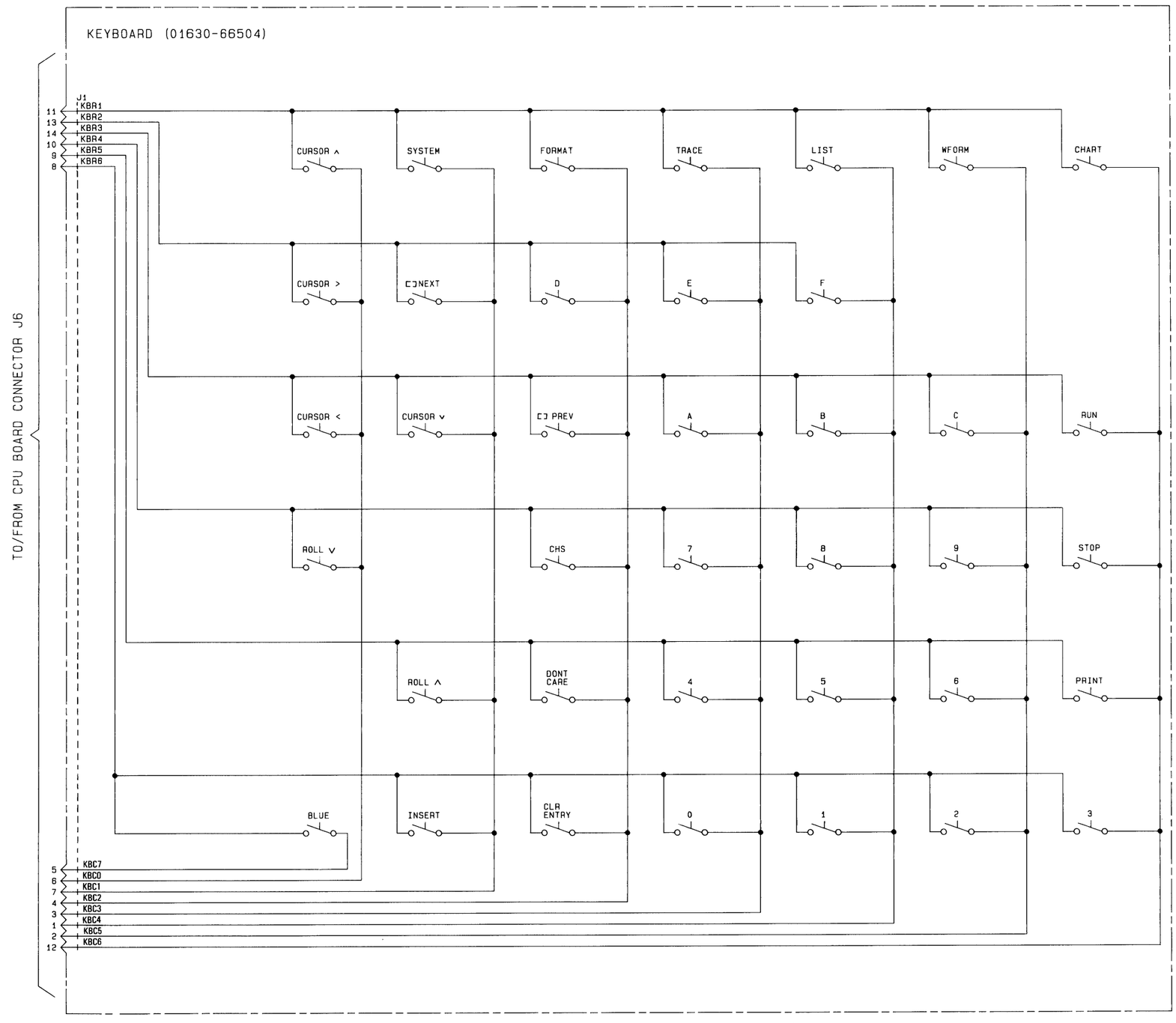


Figure 8B-12. CPU Schematic (Keyboard)(8 of 8)

Service Group 8C Table of Contents

List of Illustrations

List of Tables

SERVICE GROUP 8C
STATE MASTER

8C-1. INTRODUCTION

The following paragraphs highlight the features of the State Acquisition Board.

1. SAMPLING. The state board accepts 27 channels from three pods. The timing master and optional timing slave may also be run in state mode, adding either 8 or 16 more state channels.

2. SAMPLE RATE. Sampling is synchronous with the user system in a state analysis system. The maximum sample rate for a single clock is 25 MHz.

3. PATTERN RECOGNITION. The analyzer may be programmed before a run to look for a combination of highs or lows on the parallel 27-bit input word. The 1630 will allow up to four different patterns to be specified.

4. SEQUENCE. The operator may specify that a particular sequence of patterns must occur before the analyzer can trigger. Up to four sequence terms are allowed.

5. OCCURRENCE. The operator may specify that the last sequence pattern must repeat a certain number of times. Up to 59999 occurrences can be specified.

6. TRACEPOINT. Trigger plus delay--A valid trigger pattern has been detected and any qualifications such as delay, occurrence, and sequence have been satisfied.

7. POSTSTORE. The operator may specify tracepoint position in memory. The choices are Start, Center, or End.

8C-2. STATE BLOCK THEORY (See Figure 8C-1)

POD INTERFACE. Input data from up to three 9-bit pods is taken at the user's sample rate. Each pod has its own clock, one or more of which may be chosen as the synchronous state sample clock.

ACQUISITION MEMORY. Width is 28 to accommodate the 27 input data channels--one bit in each word is allocated for possible tracepoint. Depth is 1024 on each channel.

MEMORY ADDRESS COUNTER. Holds the address of the next location in acquisition memory to be filled. The CPU uses the memory address counter to find the position of tracepoint in memory.

PATTERN RECOGNITION RAM. Input width is 27 bits and output width is 4 bits. The CPU pre-loads the RAM so that a particular 27-bit data pattern will address a 4-bit word corresponding to one of the four specified patterns.

SEQUENCER. Determines the next analyzer state after receiving current status from the occurrence counter and pattern recognition RAM. The CPU preloads the sequencer RAM to implement the State Trace Specification sequence.

CLOCK SELECTION. Synchronizes data sampling to one or more user clocks. Selects edges and master/slave clocking for multiplexed buses.

OCCURRENCE COUNTER. Counts pattern occurrences. The counter is preloaded by the CPU with up to 59999 occurrences. Terminal count goes to the sequencer.

POSTSTORE COUNTER. Determines tracepoint position in memory. The counter is preloaded by the CPU with the amount of memory to be filled with new data after tracepoint.

CLOCK DELAY/WIDTH CONTROL. Allows adjustment of the state analyzer internal write cycle timing.

CPU INTERFACE. Allows the CPU to read the memory address counter, the poststore counter, and stored data. Also enables the CPU to clock various state analyzer functions.

TIMING SLAVE

TIMING MASTER

STATE ACQUISITION

SYSTEM UNDER TEST

8-BIT DATA

POD 1 (1630D) 8-CHANNEL TIMING POD

16-BIT DATA

(8) DIFF. RCVRS

8-BIT STATE MODE DATA

DELAY

8-BIT TIMING MODE DATA

PHASE A, C

MACROCELLS (2)

VALID SLAVE GLITCH

VALID SLAVE TIMING

PATTERNS A-D

TIMING CLOCK (TCK)

MEASUREMENT COMPLETE(MC)

STATE WRITE SLAVE

8-BIT DATA

POD 0 (1630D) 8-CHANNEL TIMING POD

16-BIT DATA

(8) DIFF. RCVRS

8-BIT STATE MODE DATA

DELAY

8-BIT TIMING MODE DATA

PHASE A, C

MACROCELLS (2)

VALID MASTER GLITCH

VALID MASTER TIMING

PATTERNS A-D

(HGS)

(HGM)

(LTS)

(LTM)

PATTERN DURATION FILTER AND TRIGGER SYNC.

SYCHRONIZED TRIGGER

DELAY/POSTSTORE COUNTER

TIMING CLOCK (TCK)

MEASUREMENT COMPLETE (MC)

STATE WRITE MASTER

FROM THE CPU BOARD

SLOW CLOCK (BELOW 5MHz)

200MHz OSCILLATOR

DIVIDERS

5

SAMPLE RATE SELECTION

9-BIT DATA

EXTERNAL CLOCK

POD 2 10-CHANNEL STATE POD

L CLOCK

(10) DIFF. RCVRS

POD 3 10-CHANNEL STATE POD

K CLOCK

POD 4 10-CHANNEL STATE POD

J CLOCK

COUNTER/LATCH

27-BIT DATA

PATTERN RECOGNITION RAM

PATTERNS A-D

4

SYCHRONOUS CLOCK SELECTION

SAMPLE CLOCK

CLOCK DELAY AND WIDTH CONTROL

STATE WRITE SLAVE (HSWS)

STATE WRITE MASTER (HSWM)

WRITE ENABLES (LEW1, LEW2)

2

MEASUREMENT COMPLETE

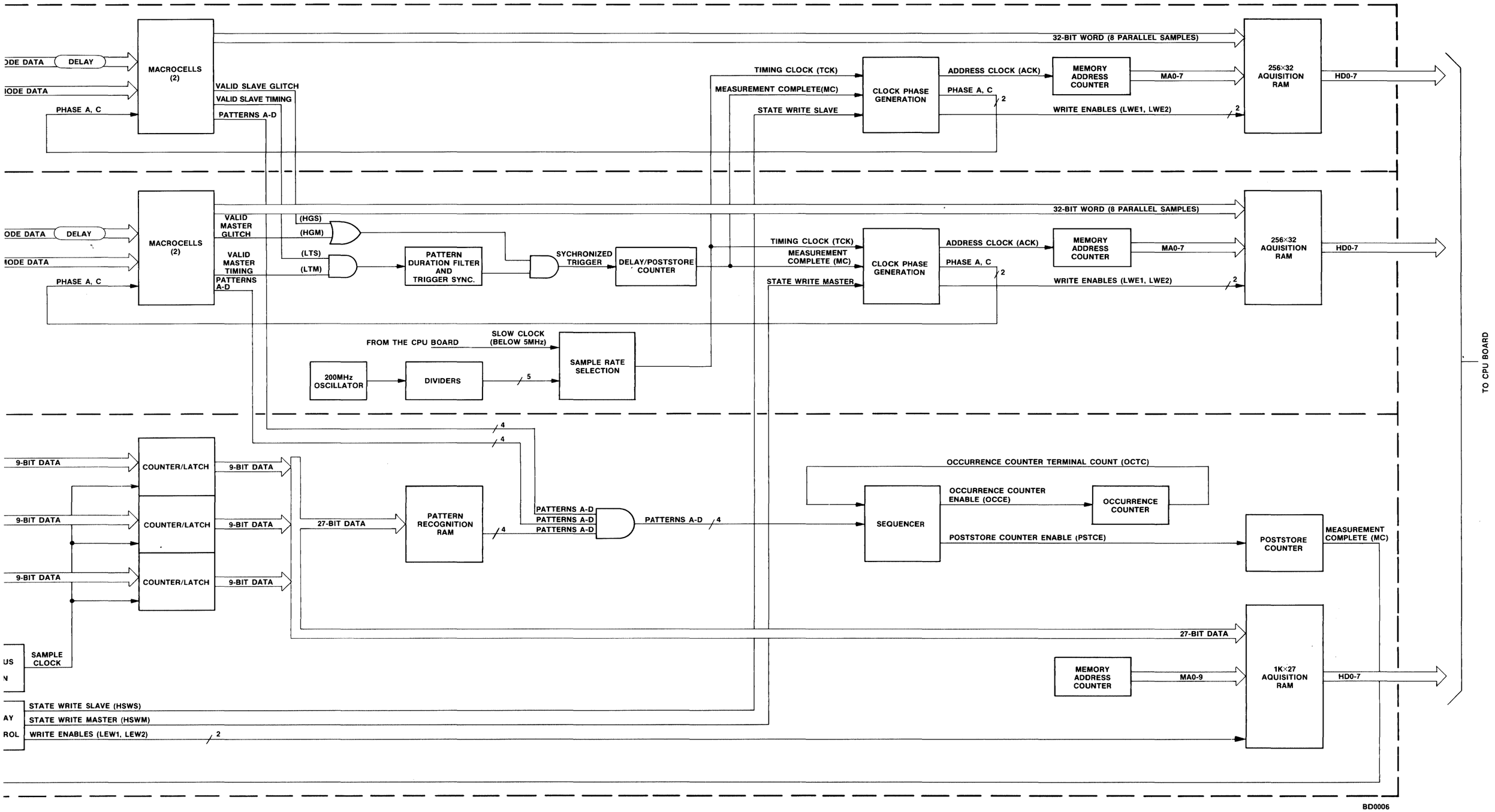


Figure 8C-1. 1630A/D Acquisition System

NOTES

8C-3. THEORY OF OPERATION

8C-4. State Pods and Pod Interface (see schematic 8C-1)

Three pods (2, 3, 4) each supply nine channels and one clock to the line receivers. The operator may choose any one--or an ORed combination--of the three clocks (J,K,L) to synchronize incoming data.

Twenty-seven channels are allocated for state analysis alone. Additionally, the master and optional slave Timing Boards can each supply eight channels, making possible a total width of 43 State channels.

The nine channels from each pod go from line receivers into 4-bit counters (U2B, U2C, 2E-2I). The counters act as sample latches during a run, or as binary counters for programming Pattern Recognition RAM before a run.

The CPU board supplies ground sensing and precision thresholds to each pod via the motherboard.

8C-5. Acquisition Memory (see schematic 8C-2)

The acquisition RAM is organized as 28 bits wide by 1024 words deep--27 bits for data storage, with 1 bit in each word to indicate tracepoint location. The 27 data channels are written into memory in parallel. When the write signals (LWE1,2) are false, or high, the CPU may read the RAM.

An octal latch (U3N) selects 1K x 8 blocks of RAM for reading, or all blocks for writing.

8C-6. Memory Address Counter (see schematic 8C-2)

The MAC consists of three 4-bit counters of which ten bits are used. The CPU reads the MAC to determine tracepoint position in memory.

8C-7. Wrap-Around Flip-Flop (see schematic 8C-2)

The Wrap-Around Flip-Flop signals that memory has been filled at least once when it receives terminal count from the MAC. This tells the CPU that the memory is filled with valid data.

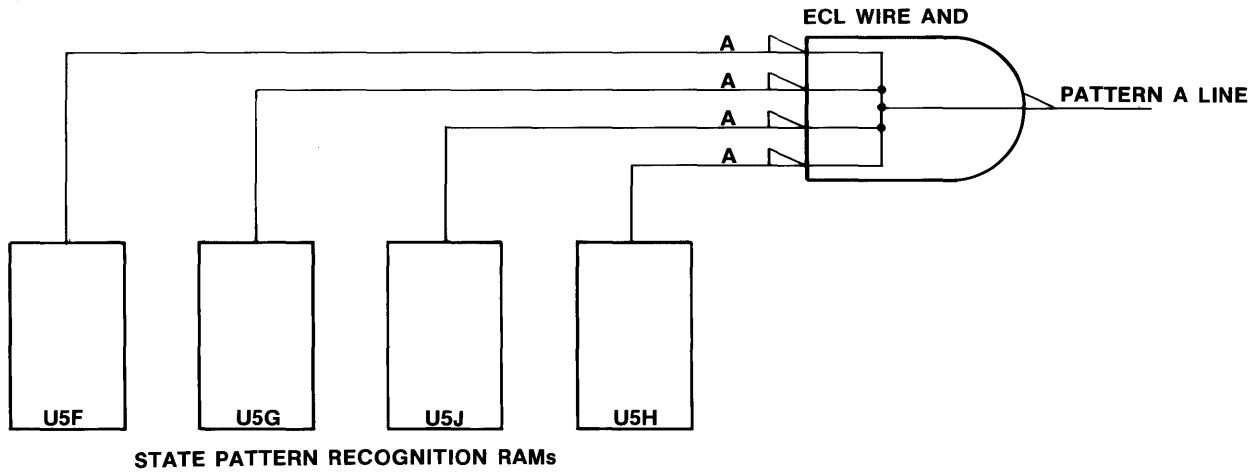


Figure 8C-2. State Recognition RAM

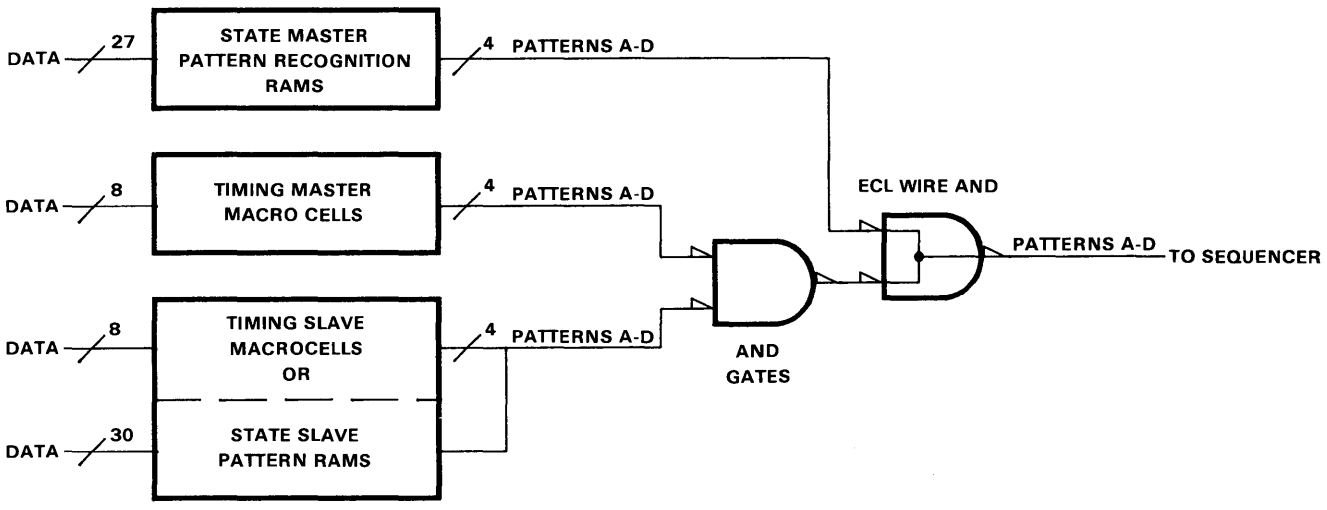


Figure 8C-3. Acquisition Pattern Recognition

8C-8. Pattern Recognition RAM (see schematic 8C-3)

Pattern Recognition RAM consists of three 256 x 4 ECL RAM chips and one 16 x 4 RAM chip connected in parallel, allowing an addressing width of 28 bits. Input width is 27 bits--since one of the address lines is not used--and output width is 4 bits. The 27-bit incoming sample from the data pods addresses Pattern Recognition RAM. The four bits from each RAM location go out over the pattern lines, LPAT A-D, to the sequencer.

Before a run, the CPU pre-loads each 4-bit RAM location. During a run, when a RAM location is addressed by the incoming sample, its four bits are output on the four pattern lines A-D. When one or more of these four bits is low, the corresponding pattern line will be driven low. A 27-bit incoming data sample that forms a pre-specified pattern of highs, lows, and don't-cares will address one of those RAM locations that was pre-loaded with at least one low.

For example, if the eight input sample bits to a single RAM chip are 00000000, then the first location will be addressed. If the four bits stored in that location are 1100, then pattern output lines A and B--corresponding to the two lows--from that RAM will try to go low.

However, as shown in figure 8C-2 each of the four output bits from each pattern RAM are ECL wire ANDed (ECL outputs may be connected together like open-collector TTL outputs). Thus, a pattern line can be active only when all four RAMs have a low on the same output.

As shown in figure 8C-3, four pattern lines also come into the state board from the timing master and timing slave boards. When the timing boards are in the state mode, their macrocells act like pattern recognition RAM. The four pattern lines from the timing boards are wire ANDed with the four state pattern lines. Thus, for a single pattern line to be driven low, the two timing boards and all four RAM chips on the state board must agree. (When a timing board is not in the state mode, its pattern lines will be normally low.)

If more than one of the pattern lines is low at the same time, the sequencer will select the one required for the next analyzer state according to the trace specification.

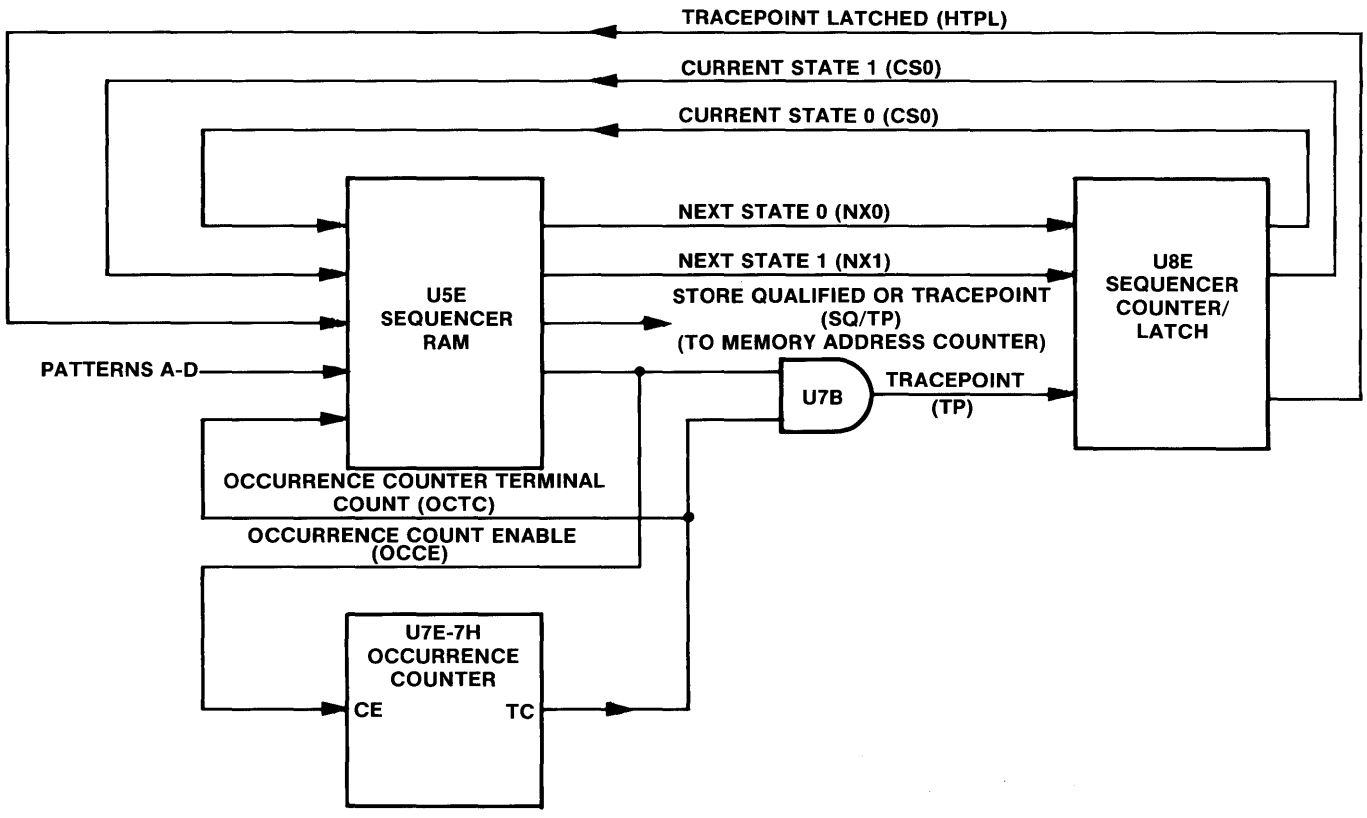


Figure 8C-4. Sequencer

8C-9. Sequencer (See schematic 8B-4)

The CPU programs the sequencer to determine the next state the analyzer will enter. Eight input control bits represent the Current State. Given a set of Current input bits, the sequencer emits six output bits representing the Next State.

The heart of the sequencer is a 4-bit binary counter (U6E) and a 256 x 4 RAM (U5E). Before a run, the counter addresses RAM locations for loading by the CPU. The CPU pre-loads the RAM locations with sequences which will occur when those locations are addressed by the eight input control bits. During a run, the counter acts as a latch for the 2-bit Current State.

Tracepoint is when: (1) The occurrence counter is enabled, and (2) it reaches terminal count. Tracepoint indicates that the specified patterns have been found, and that the last pattern has occurred the correct number of times. The ANDing of Occurrence Counter Enable (OCCE) and Occurrence Counter Terminal Count (OCTC) at U7B produces Tracepoint (TP), which is latched in the sequencer latch (U6E).

SEQUENCER INPUTS. The eight bits that drive the sequencer are:

a. Patterns A to D from Pattern Recognition RAM.
b. HOCTC----Occurrence Counter Terminal Count.
c. HTPL-----Trace Point Latched from the sequencer latch.
d. CS0,CS1--The 2-bit code representing Current State.

SEQUENCER OUTPUTS. The six sequencer outputs are:

a. NS0,NS1--The 2-bit code representing Next State.
b. LOCCE----Occurrence Count Enable, which increments the Occurrence Counter.
c. LSQ/TP---Store Qualified or Trace Point, which increments the Memory Address Counter, allowing incoming data to be stored.
d. LPSTCE---Post Store Count Enable, which enables the Poststore Counter.
e. HSQ3-----Sequence State 3, which the CPU uses for time interval measurements.

Figure 8C-5 on the next page shows an example of sequencer action for one trace format. The operator has directed the analyzer to find pattern A, then pattern B, then pattern C. If these patterns occur in the proper order, the analyzer will then look for ten occurrences of pattern D. If these specifications are satisfied, tracepoint will occur. The analyzer will store the first three sequencer states, tracepoint, and 1K of subsequent data. Tracepoint will be seen on line 0000 at the beginning of the display.

SEQUENCER STATES	TRACE FORMAT
	[single] Trace Mode
	In sequence
0	find [a]
1	then [b]
2	then [c]
	then [start] Trace at [0010] Occurrences of
3	[d] then store [allstates]
0	Sequence Restart on [no state]

Figure 8C-5. Trace Format Example

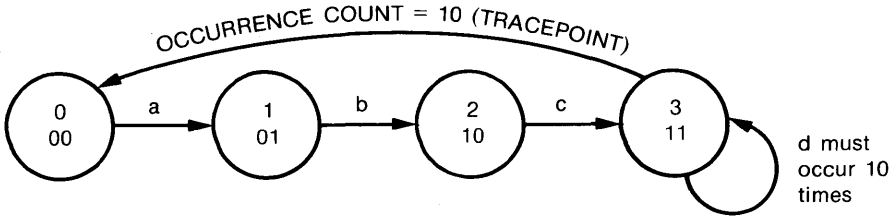


Figure 8C-6. State Diagram Example

SEQUENCER STATES	SEQUENCER INPUTS								SEQUENCER OUTPUTS			
	CS1	CS0	TPL	TC	[a]	[b]	[c]	[d]	NX1	NX0	OCCE	SQTP
0	0	0	0	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	0	0	1	0	0	0	0	1	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	0	1	0	0	0	1	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
2	1	0	0	0	0	0	1	0	1	1	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
3	1	1	0	0	0	0	0	1	1	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	d occurs n−1 times			
.	.	.	.	.	.	.	.	.	.	.	.	.
.	1	1	0	0	0	0	0	1	1	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	1	1	1	1	0	0	0	1	← d occurs 10 times →	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	1	0	0	0	0	0	0	0	0	1

Figure 8C-7. Sequencer Signals

The state diagram, figure 8C-6, shows the flow from one sequencer state to the next. The 2-bit Current State code (CS0,CS1) indicates the four possible sequencer states. If one of the terms--for example, C--were not specified in the trace format, the sequencer would jump from state 1 to state 3.

Figure 8C-7 shows the sequencer input and output signals when the events specified in the above trace format occur. The sequencer Current State is given by CS0 and CS1. As can be seen by the Store Qualified signal (SQ/TP), the first three patterns are also stored by the analyzer, even though tracepoint has not yet occurred.

8C-10. ARM CONTROL FLIP-FLOPS (U1K,7J). These control the arming of the State analyzer which may either arm or be armed by Timing. The output, LARMEN, enables Occurrence Counter terminal count to the sequencer, and the Next State outputs from the Sequencer. Without occurrence counter terminal count, tracepoint cannot occur.

8C-11. STATE/TIMING Flip-Flop (U1K). Selects either State or Timing as the master. When state is the master, both inputs to the AND gate U8D will be high when tracepoint occurs, allowing the state analyzer to arm the timing analyzer via the motherboard (P85).

8C-12. TRACEPOINT ONE-SHOT (U6J,3M). Generates a 20 ns pulse when tracepoint occurs. This is provided to the BNC output connector.

8C-13. BNC LATCH (U8C). Selects one of four different sequencer outputs to go out to the external BNC connector:

Tracepoint Pulse (U8C-5)	A 20ns negative-going pulse when trace-point occurs.
Timer (U8C-4)	Low level on Current State 3 (CS0,CS1=1); This is equivalent to HSQ3, which is sent to the CPU for the Overview Time measurement.
Tracepoint High (U8C-12)	This BNC output will stay low as long as the analyzer is looking for tracepoint, then go high until another measurement is begun.
Tracepoint Low (U8C-10)	This BNC output will stay high as long as the analyzer is looking for tracepoint, then go low until another measurement is begun.

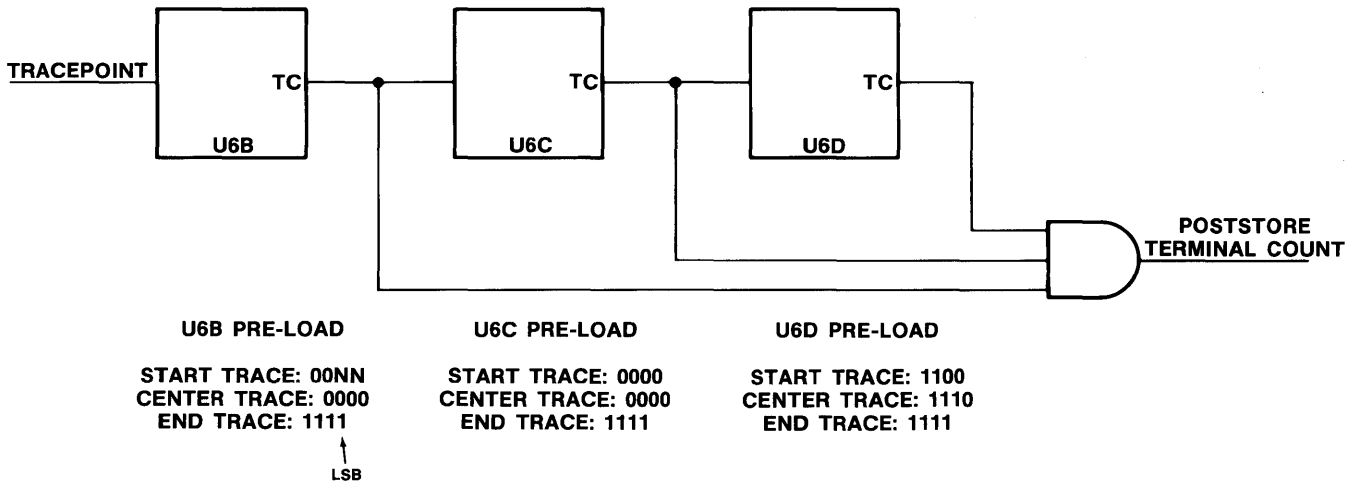


Figure 8C-8. Poststore Counter

8C-14. Poststore Counter (See schematic 8B-5)

The state analyzer provides three different measurement techniques:

Start-Trace — Memory is completely filled with new data after tracepoint; tracepoint is displayed at the beginning. (If a sequence is specified, the sequence patterns--up to three--will be stored before tracepoint.)

End-Trace — Displayed memory consists entirely of pre-tracepoint data; tracepoint is displayed at the end.

Center-Trace — Displayed memory consists of half pre-tracepoint data and half post-tracepoint data; tracepoint is displayed in the center.

The poststore counter counts out the amount of data to be stored after a start, center, or end-trace measurement. The poststore counter is enabled by the sequencer (LPSTCE) when tracepoint occurs. The counter is then incremented on every store-qualified state following tracepoint. The following signals must be true:

LTPL (U6F-3) — Tracepoint Latched: occurs at occurrence counter terminal count and occurrence counter enable; and stays set.

LSQ/TP (U6F-12) — Store-qualified or Tracepoint: indicating that data is available for memory storage. This will always be true out of the sequencer when more data is to be post-stored.

During a measurement, the CPU reads the poststore counter's output to determine the number of words to completion of the state measurement. Terminal count from the poststore counter goes to the sequencer where it enables End of Measurement (HEOM) and Measurement Complete (LMC), which stop the data collection process by shutting down the write strobes and the memory address counter, respectively. Measurement Complete signals the CPU via interrupt that the memory is full, and the state measurement is complete.

8C-15. Occurrence Counter and Load Latches (see schematic 8B-5)

The occurrence counter (U7E-7H) counts repetitions of the last pattern to be found. Although up to four patterns may be specified, only the last pattern may have an occurrence specification.

When the operator specifies the pattern repetitions required to produce tracepoint, the CPU loads sequencer RAM to recognize that pattern, and presets the occurrence counter with the number of repetitions. Then, whenever that pattern occurs, the sequencer increments the occurrence counter. The sequencer enables the occurrence counter, clocked by the index clock (ICK), on every Occurrence Count Enabled state (LOCCE).

The sequencer is always restarted after every tracepoint. CPU Master Reset (HMR) presets the counter initially during operator setup. Whenever tracepoint occurs, the sequencer restarts, going to Sequence State Zero, and begins looking for the original sequence again.

Immediately after tracepoint is found, or before the sequencer is restarted, the next sequencer state will be 0. This is decoded by U7B as HPE, which reloads the occurrence counter to the original preset value. The Load Latches (U8E-8H) store the original occurrence counter preset value, allowing the counter to be reloaded after every tracepoint or sequence restart. This is so the tracepoint pulse can be continually sent out over the BNC after it is found the first time.

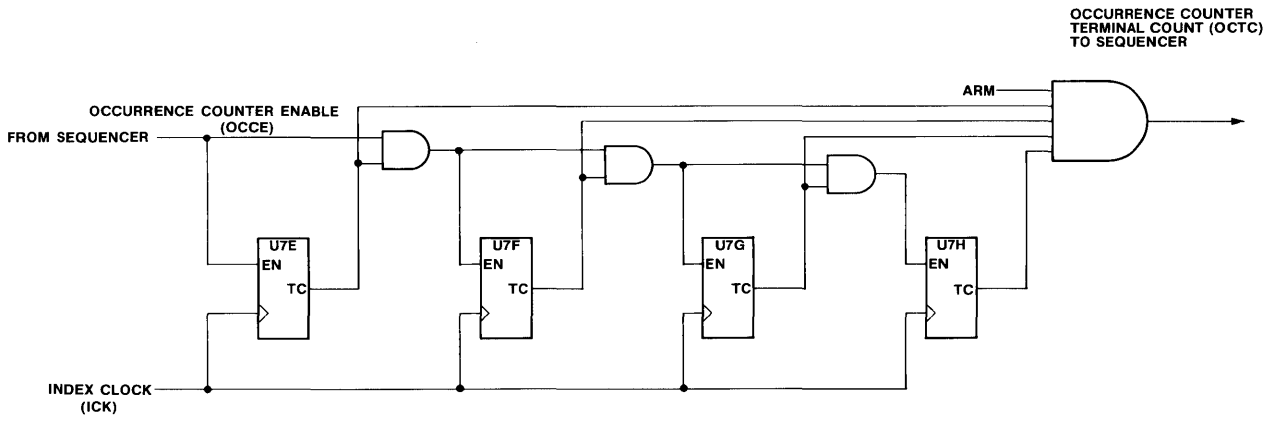


Figure 8C-9. Occurrence Counter and Load Latches

Tracepoint is the ANDing of LOCCE and LOCTC. That is, the occurrence counter must be enabled and it must reach terminal count for tracepoint to occur. All the other sequence terms must be satisfied before the sequencer can begin incrementing the occurrence counter. For example, if three other patterns were specified, the analyzer will look for these before counting the repetitions of the fourth pattern. An occurrence search is always the last process in a sequence. See figure 8C-10 below.

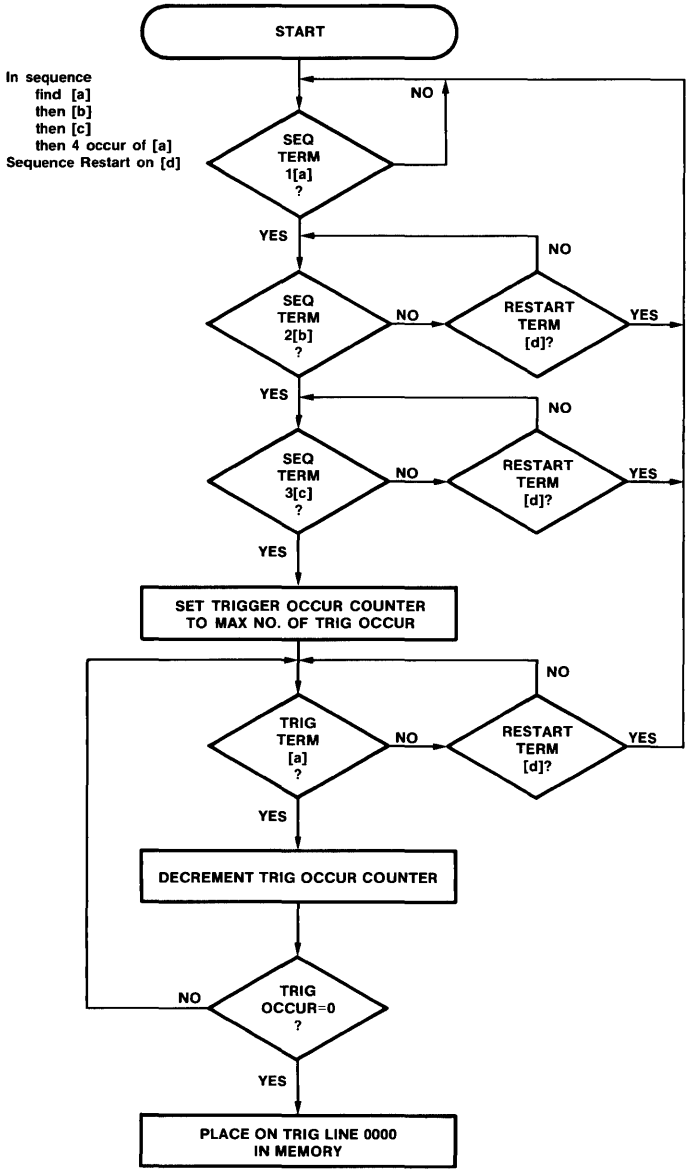


Figure 8C-10. Sequence Flow Chart

8C-16. Clock Selection (See schematic 8B-6)

A state analyzer is synchronous: sampling must be in step with the external clock from the system being analyzed.

Each of the three state pods (2,3,4) provides a clock input (L,K,J). The operator selects one or more of these clocks to synchronize the analyzer to the user system. Up to three clocks can be ORed together. For multiplexed user busses, one clock can be chosen as the master and another as the slave. Positive, negative, or both edges of any of these clocks may be selected.

As shown in figure 8C-11 below, each clock input is associated with four flip-flops whose D inputs are loaded by the CPU with the clock and edge selections. For example, if the J clock's negative edge is to be selected as master, the MJN input (U7M-10) will be programmed high. When the J clock transitions from high to low, the flip-flop output (U7M-15) will go high, causing the master one-shot to pulse and reset the flip-flop. The master clock will then consist of pulses whose positive edges are synchronized with the incoming negative J clock from Pod 2.

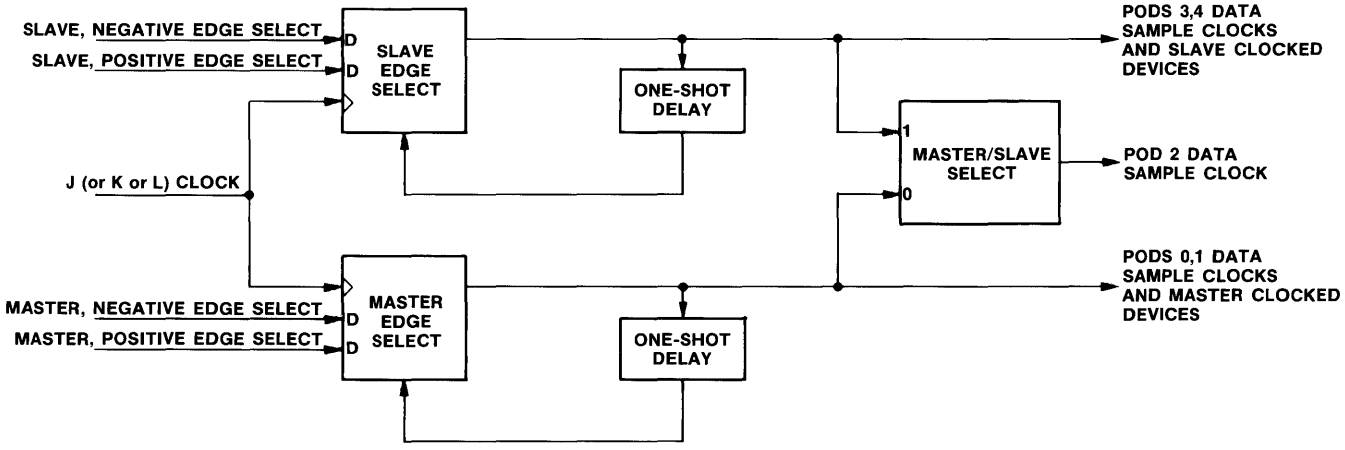


Figure 8C-11. J, K, or L Clock Path

As shown in figure 8C-12 below, any edge of any clock, or an ORed combination, may be chosen as the master or slave. The same clock may be both master and slave if different edges are used. In the non-multiplexed mode both master and slave clocks are identical.

The Delay/Width Control and the Timing Boards--when in the State Mode--are always clocked by the master clock. The Run/Halt Control and the Pod 3 and 4 data latches are always clocked by the slave clock. The Pod 2 data latches may be clocked by either the master or slave.

The Master-Slave Selector (8L) allows the Pod 2 data latches (U2B,2C,2D) to be clocked by the master or the slave clock selections.

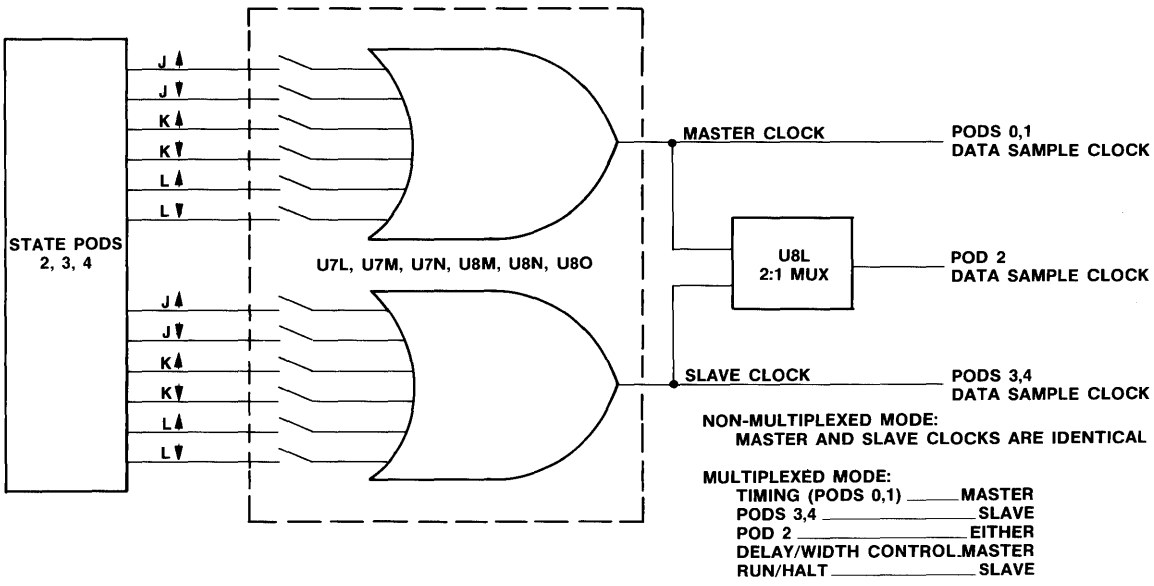


Figure 8C-12. Clock Selection

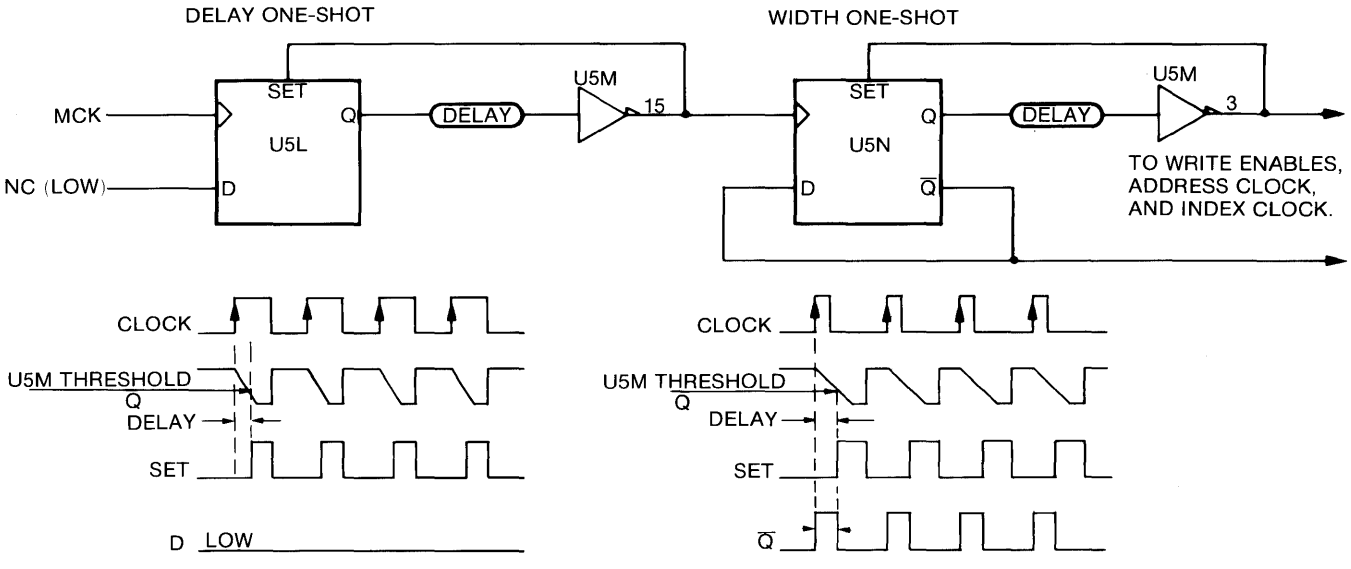


Figure 8C-13. Clock Delay and Width Control

8C-17. Clock Delay and Width Control (see schematic 8B-7)

The master clock (MCK) from the clock selector is shaped and delayed by two one-shots, which make up the heart of this circuit.

Clock delay is varied in the Delay One-Shot (U5L,5M). The output of the delay one-shot is then fed to a Width One-Shot (U5M,5N), which adjusts clock width.

Since both circuits work the same, only the delay one-shot will be described. An ECL output must be pulled down to produce a low. The pulldown for flip-flop U5L-2 is the resistor network R7 and the adjustable R5. Capacitor C4 has a quick charge path through the flip-flop on high- going signals, but must charge through the resistor network for lows. The delay for low-going signals is therefore adjustable.

Figure 8C-13 shows the timing relationship for the circuit. Since disconnected ECL inputs are internally pulled low, the D input is always low. In this type of flip-flop, D is clocked on a positive transition and S is active high. Because of the delay caused by the capacitor, the flip-flop cannot go low immediately. When it does go low the inverter, which has positive feedback, sets the flip-flop again for the next cycle.

8C-18. CLOCK CONTROL.

The shaped and delayed clock output eventually becomes four clocks:

ACK	Address Clock.
ICK	Index Clock.
LWE1, LWE2	Write Enable signals for acquisition memory.

ACK increments the memory address counter; ICK increments the occurrence, poststore counters, and the sequencer. The memory address and poststore counters are incremented only for store-qualified states, i.e., when data is to be stored in memory. During programming mode, the CPU substitutes its own clocks, HRDCK and HLDCK for ACK and ICK.

The Write Enable signals, LWE1 and LWE2, enable data acquisition RAM for the storing of data. Except for being delayed by 6ns to allow for RAM hold time, ACK and ICK are similar to the write enable signals.

LRUN, from the RUN/HALT FF (U5L), causes the pod interface counters (U2B- 2I) to go into the preset mode and act like latches, so they can latch in new probe data. When LRUN is high, the pod interface counters act as address counters, allowing the CPU to load Pattern Recognition RAM during programming mode.

8C-19. CPU Interface (See schematic 8B-8)

The CPU interface allows the CPU to read the contents of the memory address counter, the post-store counter, and state acquisition memory. Because the CPU loads the contents of state RAM into CPU RAM, it needs to reference data and tracepoint to these counters in order to correctly position the display. Counter and memory information is multiplexed onto the data bus by the Read Selectors (U5A-5D).

The CPU writes to the analyzer, providing clocks and enable signals for different analyzer funtions, by means of the Write Strobe Demultiplexer (U1N). The following is a list of the clocks coming out of the demux:

BKCK	Block Clock. Loads the data storage RAM block selector (U3N).
OCK1,OCK2	Occurrence Clock. Loads CPU data into occurrence counter latches.
LCCK	Counter Clock. Enables preset of occurrence and post-store counters.
LP1WE,LP2WE	Pattern recognition RAM write enables.
SLCK	Loads slave clock edge selector and pod 2 master/slave clock selector. Generates CPU controlled clocks for loading pattern recognition RAM.
MSCK	Loads master clock edge selector.

Instead of using the internal clocks, the CPU itself may clock the memory address, occurrence, and post-store counters. HCCK clocks the memory address counter, and HLDCK clocks the post-store and occurrence counters.

The Run Control Latch (U1K) sets the RUN or HALT mode. Its output, HRNCTL, controls LRUN, which enables the pod interface and sequencer latches.

The pre-run and pre-halt signals from U1L control the operation of the BNC output latch (U8C) in the Sequencer.

8C-20. MNEMONICS

The following signals, listed in alphabetical order, are used on the State Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing and State boards are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8C-1. Mnemonics

Mnemonic	Description
ACK	Address clock to the memory address counters.
BKCK	Block clock to the acquisition memory chip selector.
CS0,1	Two-bit code for the current state used by the sequencer.
D0-7	Data outputs from acquisition memory.
GS2-4	Ground sensing to the three State pods.
HA0-7	Motherboard address bus.
HARM	Arm. Allows State to arm Timing, or vice versa.
HBRK1-3	Signals to break feedback paths for signature analysis.
HD0-7	Motherboard data bus.
HEOM	End of measurement. Stops the memory address counters.
HLDK	Load clock. CPU clocks the poststore and occurrence counters.
HMR	Master reset. Resets sample latches and occurrence counter.
HOCTC	Occurrence counter terminal count.
HPE	Preset enable. Presets occurrence counters on Next State 0.
HPREHALT	Pulse that occurs just before a halt.
HRDK	Read clock. CPU clocks the memory address counter.
HRDRST	Read reset. Allows the CPU to cause End of Measurement (EOM).
HRLW	High read low write. Enables reading and writing to the CPU.
HRUN	Enables sample and sequencer counters as latches during a run.

Table 8C-1. Mnemonics (Cont'd)

Mnemonic	Description
HSQ3	Sequencer state 3. Used by CPU for time interval measurements.
HSWM	State write enable master. State writes data into Master Timing RAM.
HSWS	State write enable slave. State writes data into Slave Timing RAM.
HTPL	Tracepoint latched from the sequencer.
ICK	Index clock. Clocks the occurrence counter, poststore counter, and all sequencing functions.
LARMEN	Arm enable. Enables occurrence counter terminal count.
LAM LAS LBM LBS LCM LCS LDM LDS	Pattern recognition lines from master and slave timing boards.
LMC	Measurement complete. Stops the write-enables to memory.
LMF	Memory-full signal from the memory address wrap-around FF.
LOCCE	Occurrence counter enable. Increments the occurrence counter.
LPAT A-D	Pattern lines from pattern recognition memory to the sequencer.
LPRERUN	Pulse that occurs just before a run.
LPSTC	Poststore counter terminal count.
LPSTCE	Poststore counter enable. Increments the poststore counter.
LRNCTL	Run control. Controls HRUN to the sample latches.
LSQTP	Store Qualified or Tracepoint. Enables data storage in RAM.
LSQWE	Sequencer RAM write enable. Used for programming the sequencer.
LSTB	Strobe. Strobes data and status into the CPU from the analyzer.
LWE1,2	Write enable signals to acquisition memory.

Table 8C-1. Mnemonics (Cont'd)

Mnemonic	Description
MA0-9	Memory address counter output.
MCK	Master clock. Source of the address and index clocks.
MSCK	Master select clock. Selects positive or negative edge.
NS0-1	Two-bit code for the next state from the sequencer.
OCK1,2	Enables the occurrence and sequencer latches for programming.
P1WE, P2WE	Write enable signals to pattern recognition RAM.
RUNSEL	Run select. Selects memory address or poststore outputs to CPU.
SCLK1,2	Slave clocks to the sample latches.
SD0-26	Twenty-seven channel data lines from the sample latches.
SLCK	Slave select clock. Selects positive or negative edge.
SMCK	Master clock to the sample latches.
THR2-4	Thresholds to the three state pods.

NOTES.

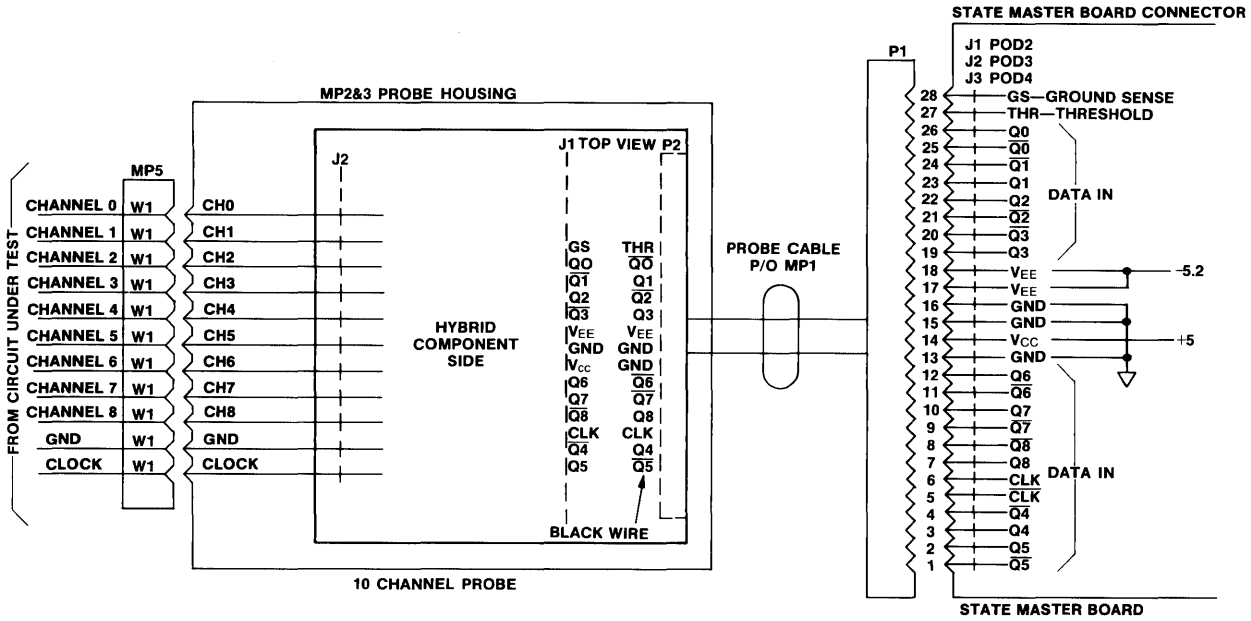


Figure 8C-14. State Pod

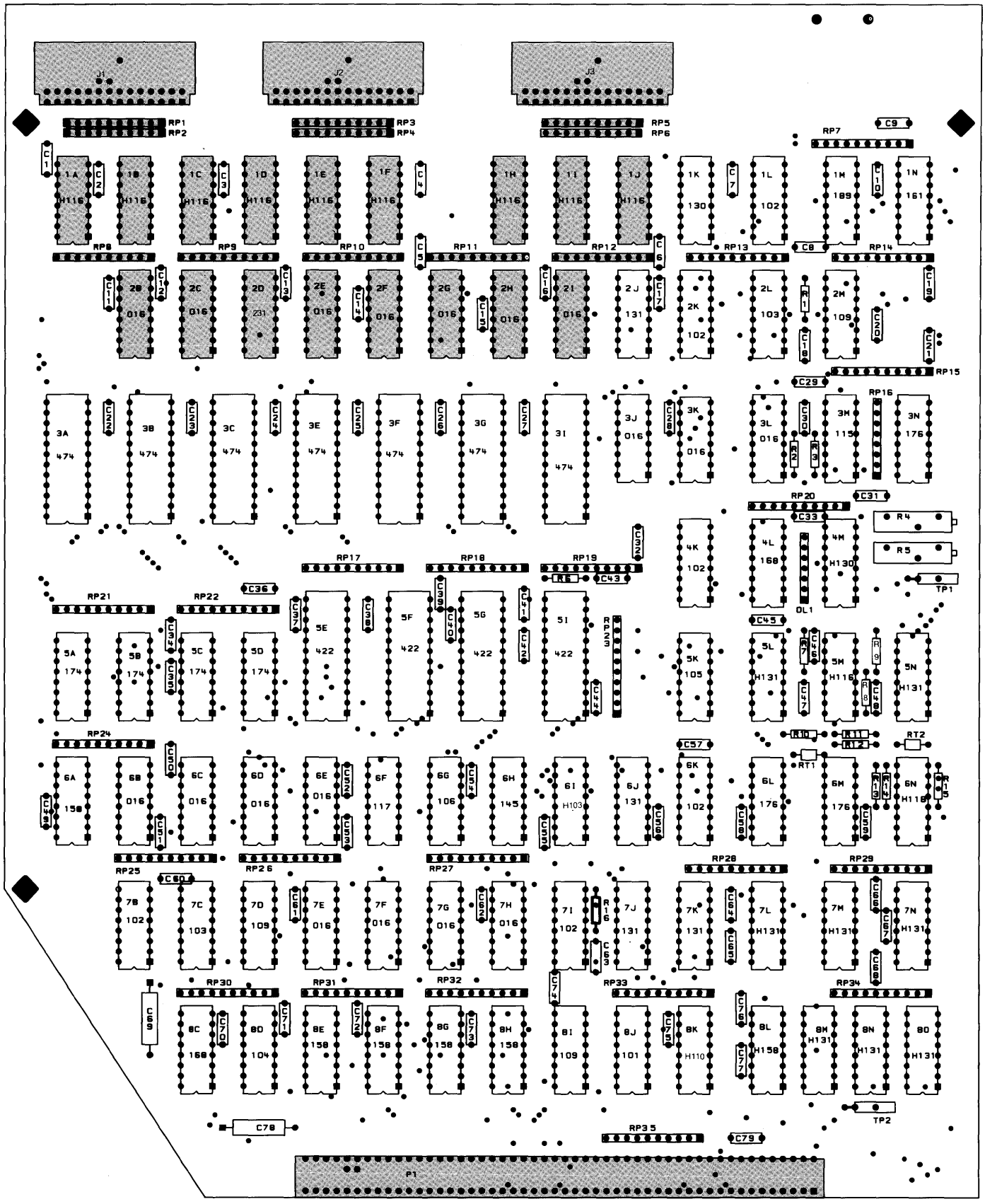
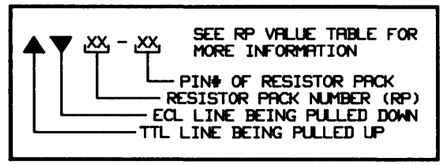


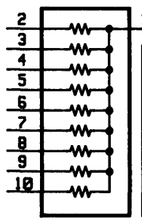
Figure 8C-15. State Board Component Locator

IC DEVICE
POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1A-F,1H-J, U2B-2I

RESISTOR PACK DESCRIPTIONS:

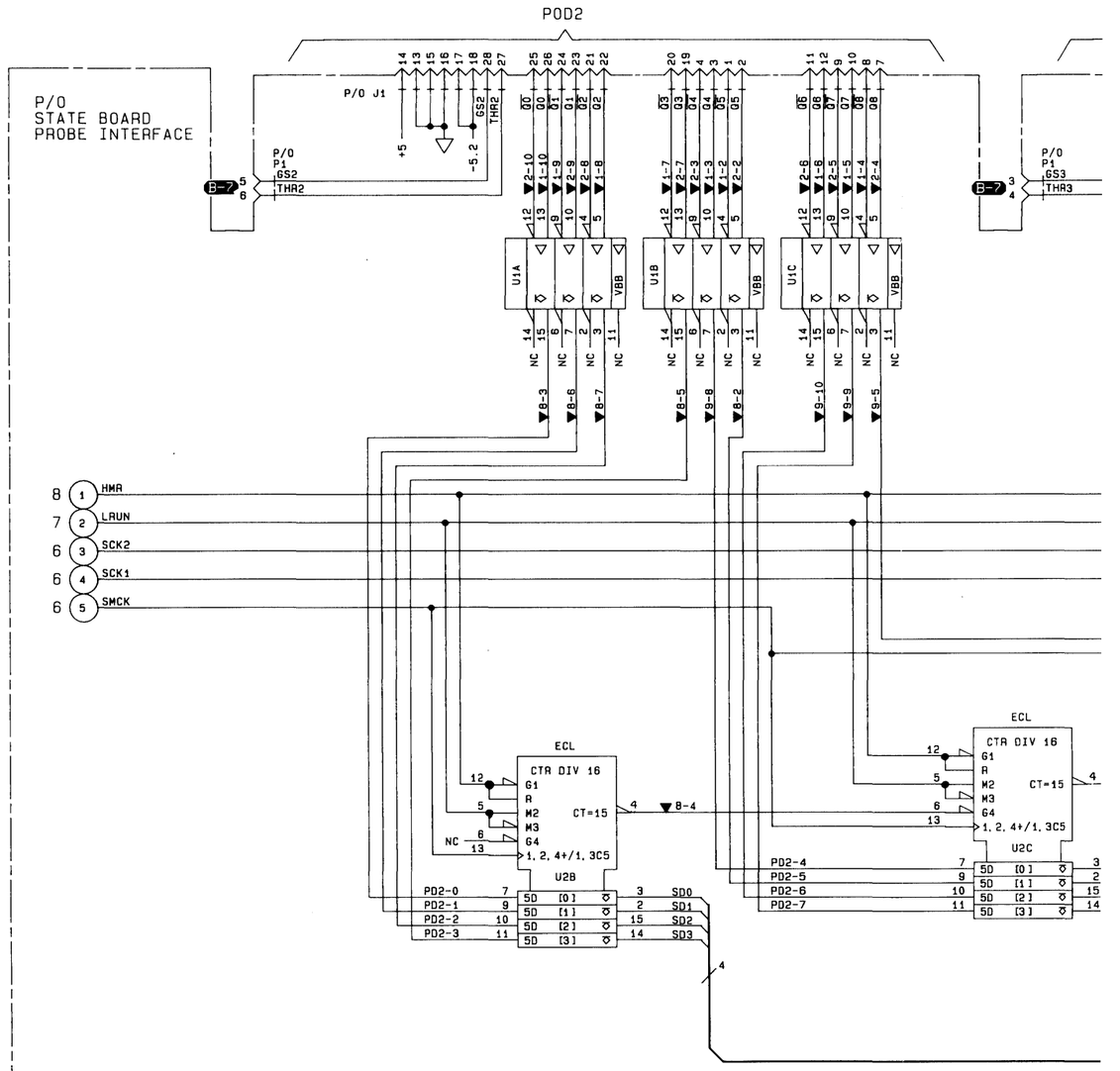




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U1A-F,1H-J,2B-I, J1,2,3 RP1-6,8-12 J1,2,3	



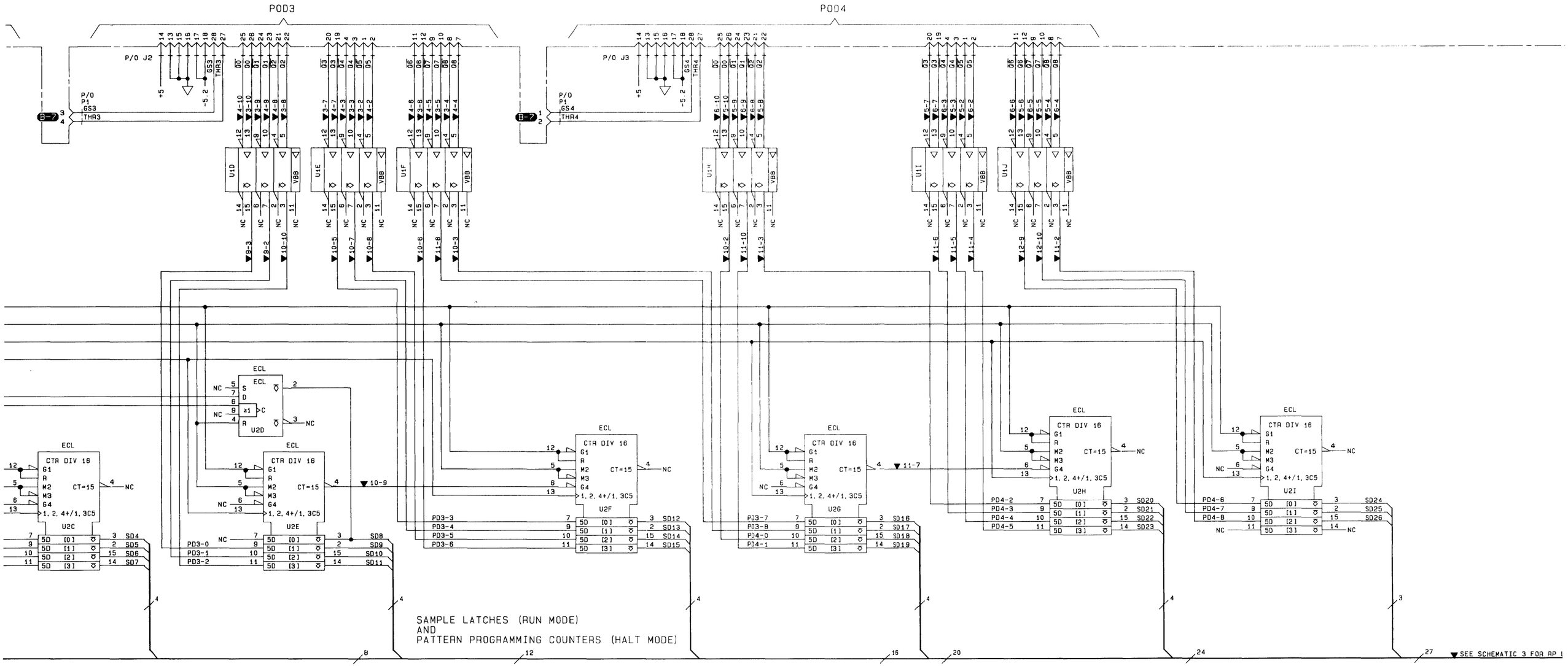

POD3
POD4
P/O J2
P/O J3
P/O P1 GS3 THR3
P/O P1 GS4 THR4
B-7
+5
-5.2
U1D
U1E
U1F
U1H
U1I
U1J
VBB
NC
ECL
CTR DIV 16
G1
R
M2
M3
G4
CT=15
1, 2, 4+/1, 3C5
U2C
U2D
U2E
U2F
U2G
U2H
U2I
5D [0]
5D [1]
5D [2]
5D [3]
≥1
S
D
C
SAMPLE LATCHES (RUN MODE)
AND
PATTERN PROGRAMMING COUNTERS (HALT MODE)
SEE SCHEMATIC 3 FOR RP I

Figure 8C-1

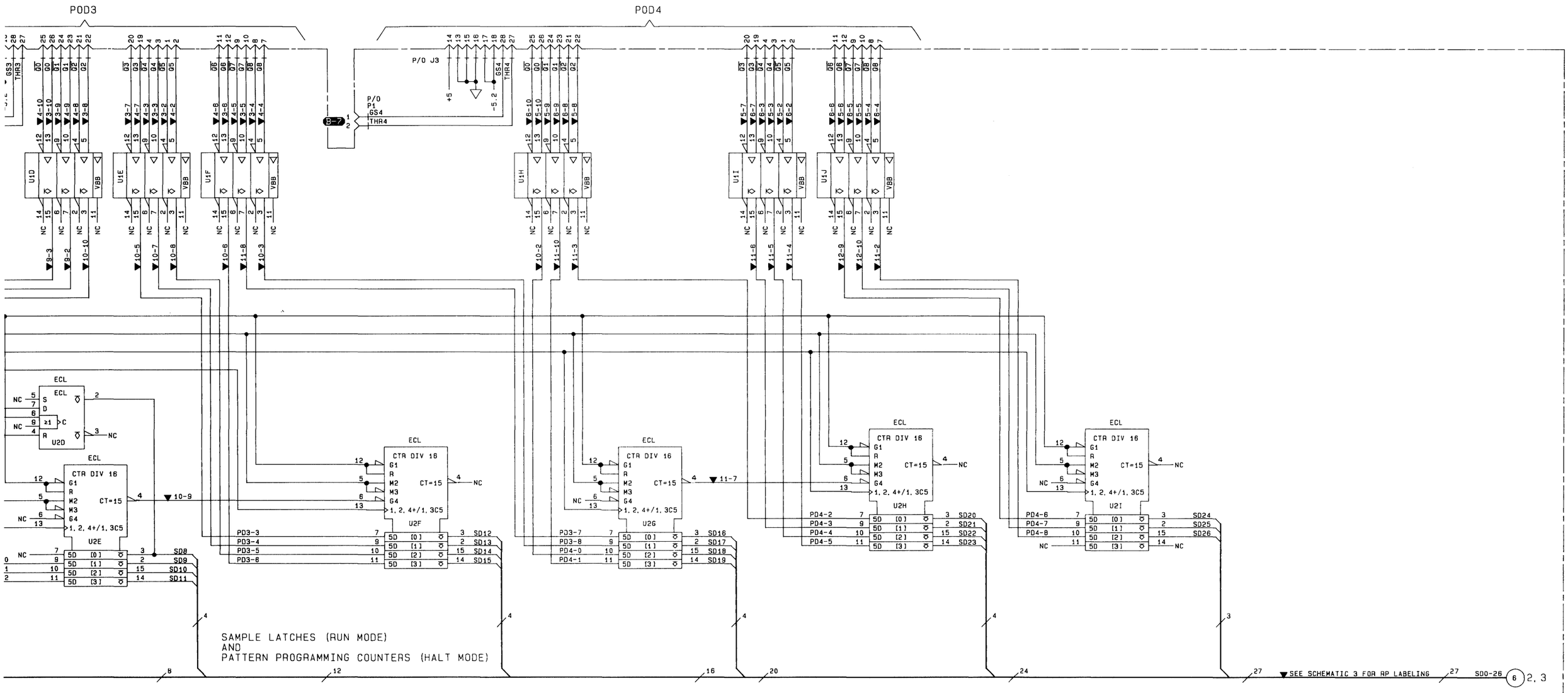


Figure 8C-16. State Schematic (1 of 8)

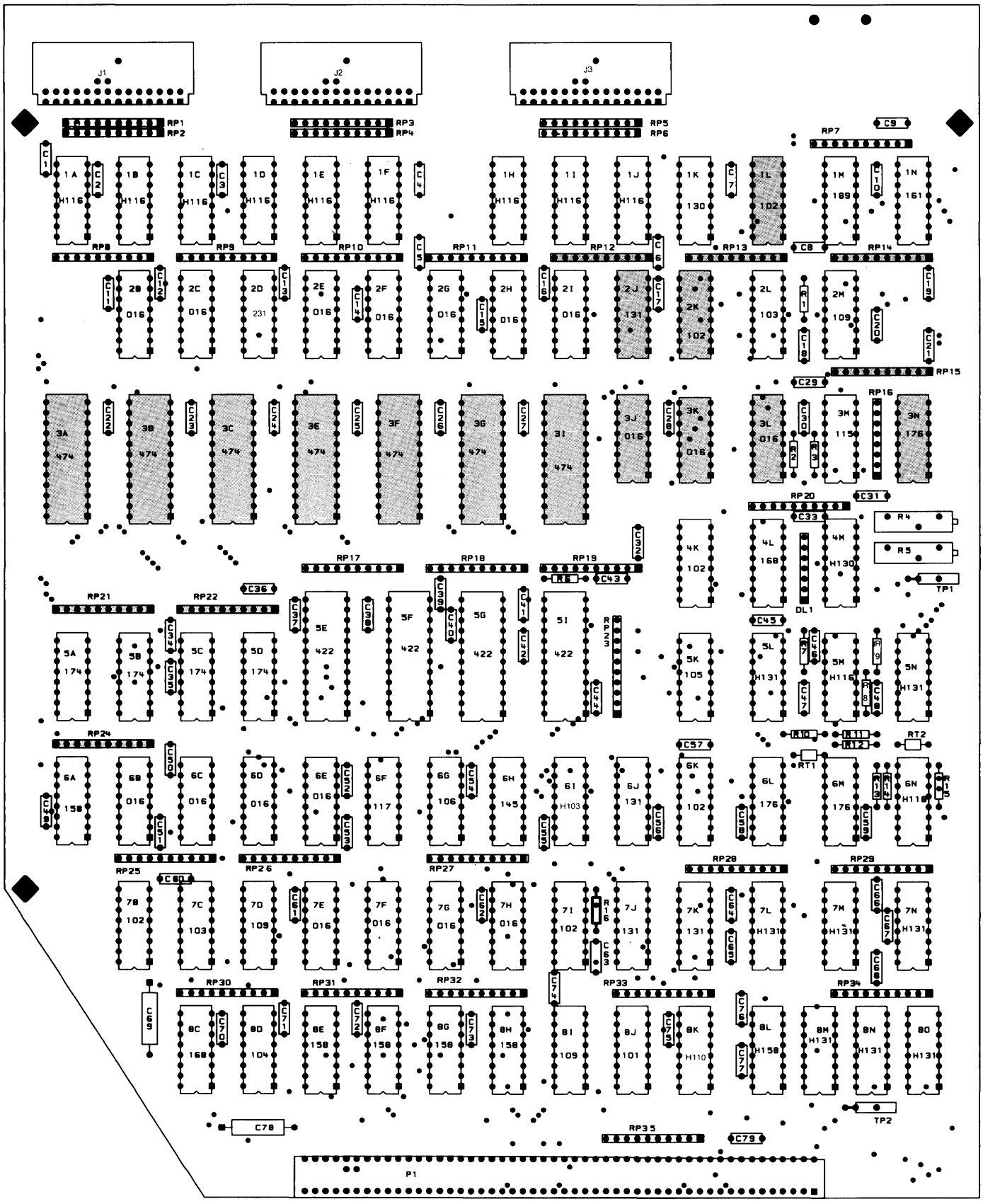


Figure 8C-15. State Board Component Locator

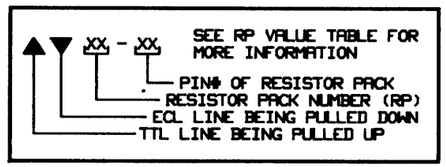
NOTE I

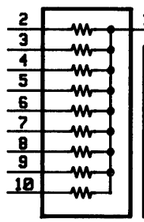
ON STATE MASTER BOARD 01630-66505, U3N PINS 14 AND 15 ARE CONNECTED TO U4M PIN 4 AND U6K PIN 5 RESPECTIVELY (8C-7). THESE LINES ARE ALSO PULLED DOWN BY PARTS OF RP-15.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1L,2J,2K 3J-3L,3N
Vcc(gnd) Vcca(gnd) Vee(-5.2)	24 1 12	U3A-3C,3E-3G, 3I

RESISTOR PACK DESCRIPTIONS:



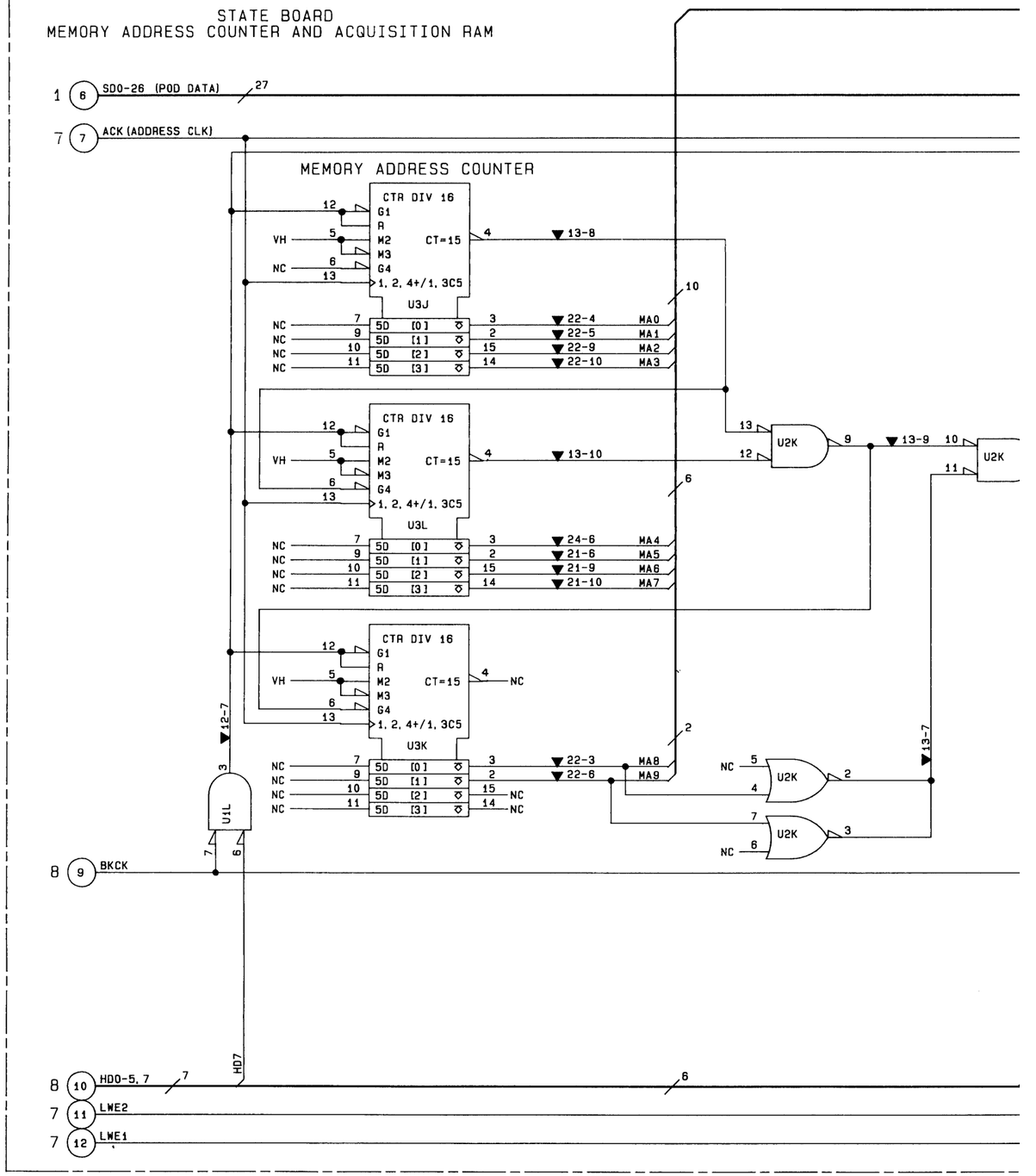


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U1L,2K,2J,3A-3C U3E-3G,3I,3J-3L,N RP12-15,21-22,24	

STATE BOARD
MEMORY ADDRESS COUNTER AND ACQUISITION RAM



ACQUISITION RAM

WRAP AROUND FF

BLOCK SELECT FF

FOR U3N SEE NOTE 1

Figure 8C-

ACQUISITION RAM

LOCK SELECT FF

IRAP AROUND FF

FOR U3N SEE NOTE 1

Figure 8C-16. State Schematic (2 of 8)

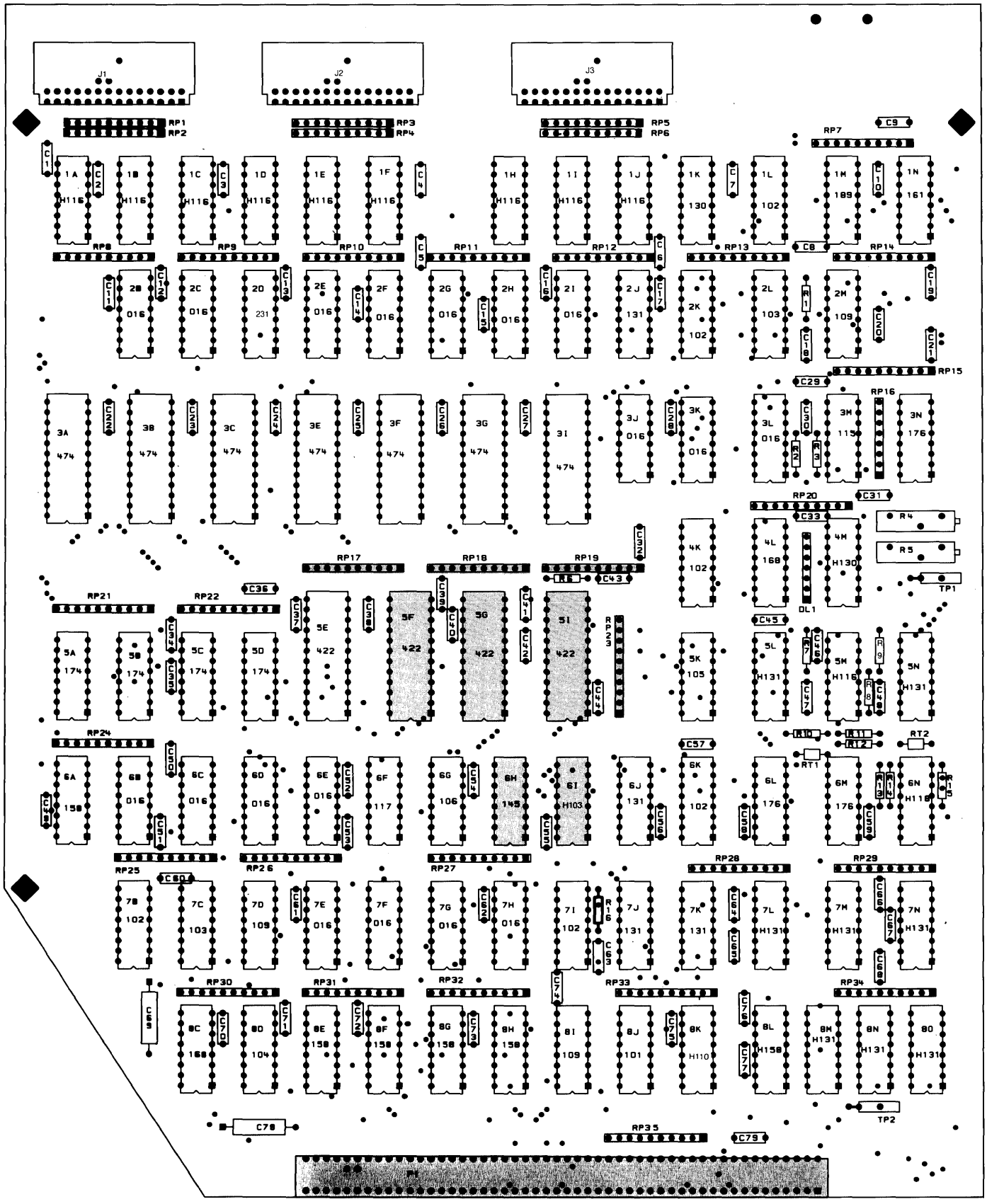
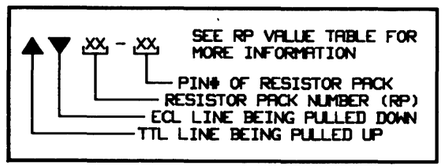


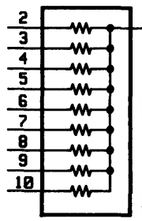
Figure 8C-15. State Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U6I
Vcc(gnd) Vcca(gnd) Vee(-5.2)	24 1 12	U5F,5G,5I
Vcc(gnd) Vee(-5.2)	16 8	U6H

RESISTOR PACK DESCRIPTIONS:

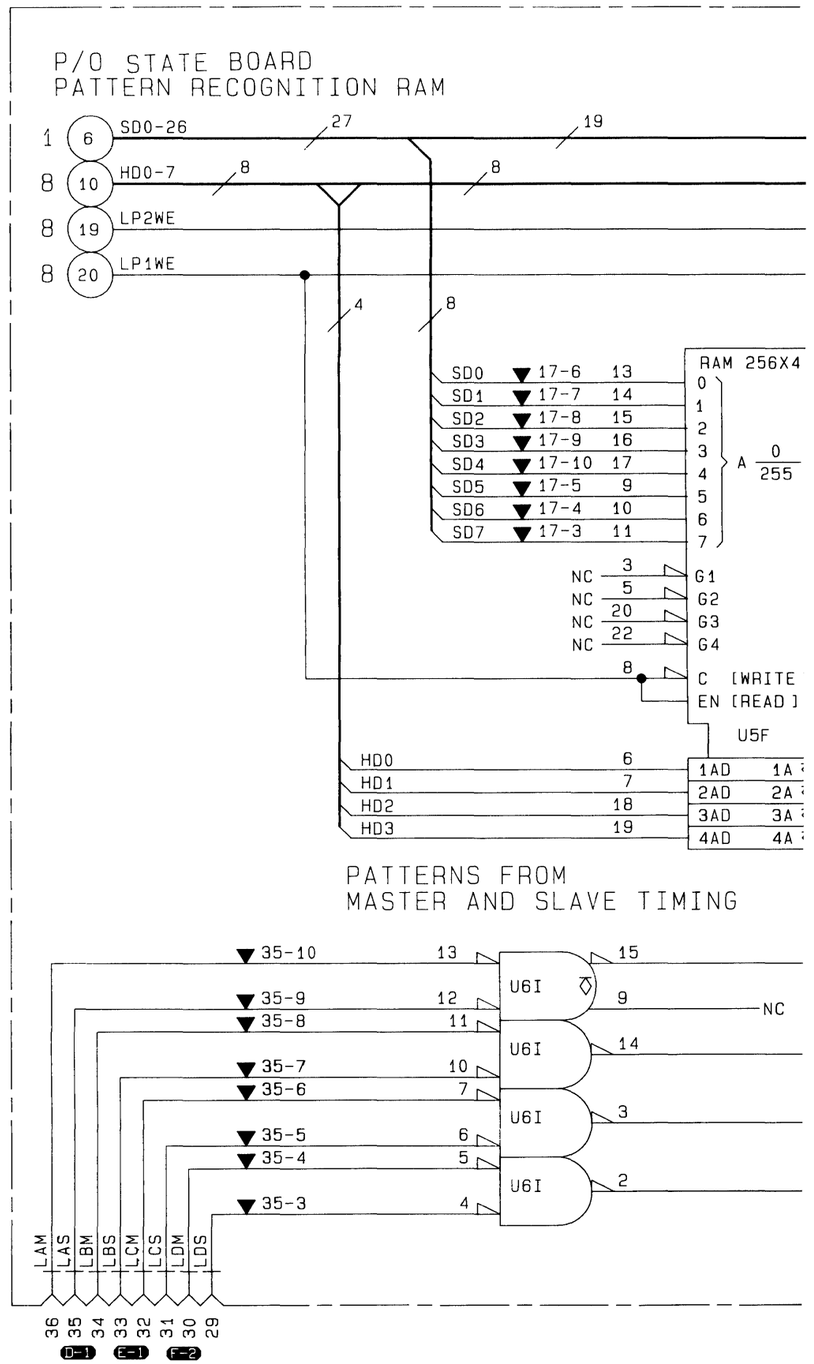




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U5F,5G,5I,6H, U6I RP17-19,23,35	



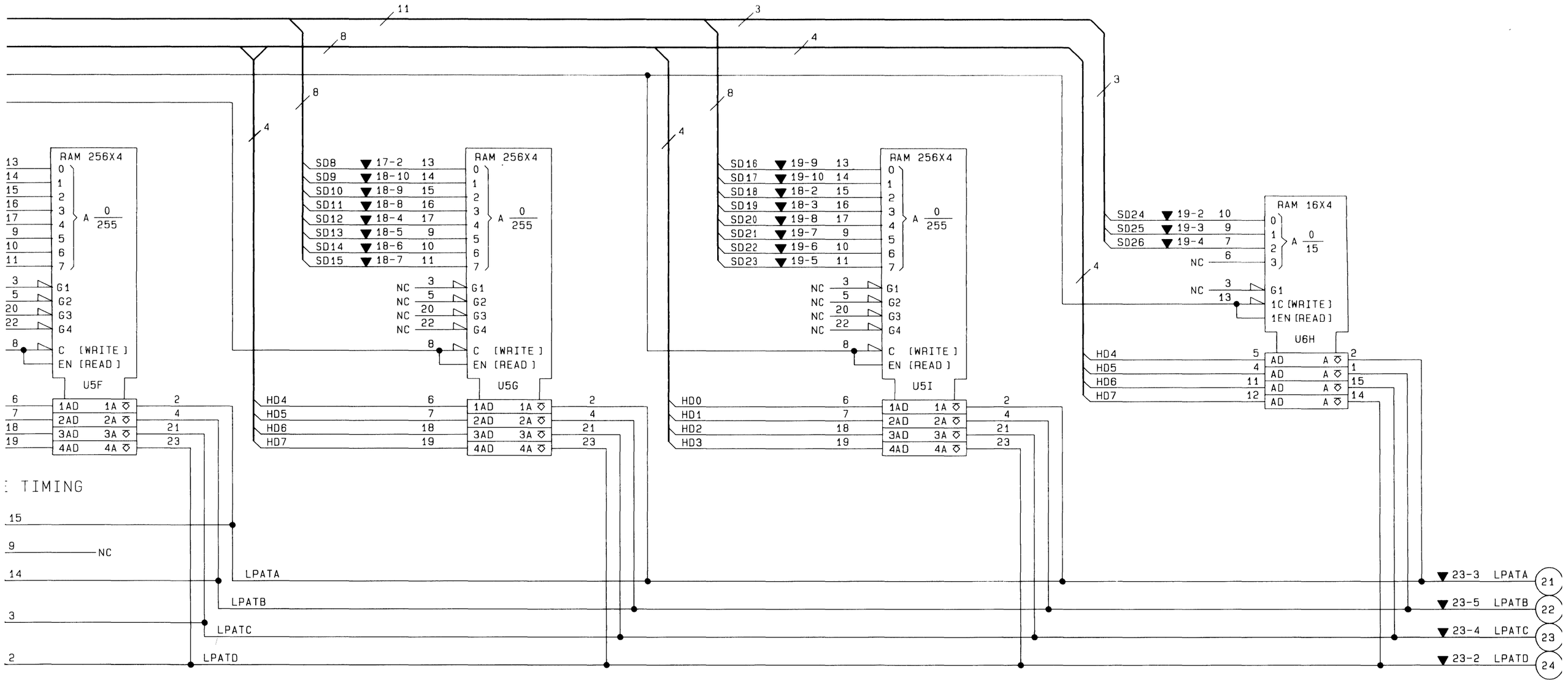

RAM 256X4
U5F
U5G
U5I
RAM 16X4
U6H
A 0/255
A 0/15
G1
G2
G3
G4
C [WRITE]
EN [READE]
1AD 1A
2AD 2A
3AD 3A
4AD 4A
AD A
SD8 17-2 13
SD9 18-10 14
SD10 18-9 15
SD11 18-8 16
SD12 18-4 17
SD13 18-5 9
SD14 18-6 10
SD15 18-7 11
SD16 19-9 13
SD17 19-10 14
SD18 18-2 15
SD19 18-3 16
SD20 19-8 17
SD21 19-7 9
SD22 19-6 10
SD23 19-5 11
SD24 19-2 10
SD25 19-3 9
SD26 19-4 7
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
NC
1C [WRITE]
1EN [READ]
TIMING
LPATA
LPATB
LPATC
LPATD
23-3 LPATA
23-5 LPATB
23-4 LPATC
23-2 LPATD

Figure 8C-

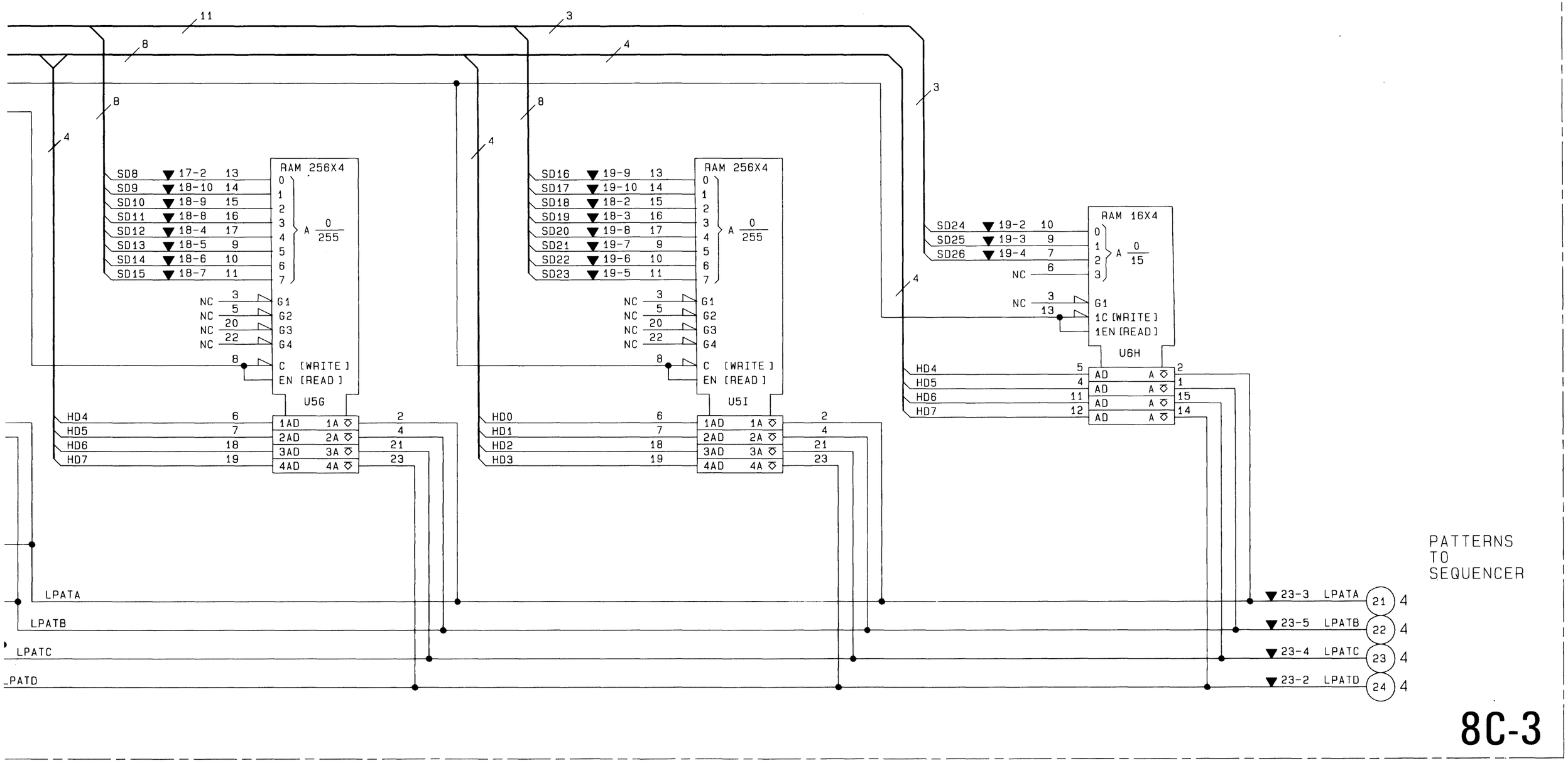


Figure 8C-16. State Schematic (3 of 8)

Figure 8C-15. State Board Component Locator

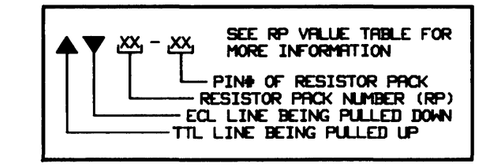
NOTE 1

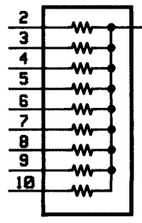
ON STATE MASTER BOARD 01630-66505, U6G PINS 12, 13 AND 14 ARE CONNECTED TO PINS OF U6G AND U6F. U6G PINS 12, 13, 14 AND 15 HAVE NO FUNCTION IN ANY 1630.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1K,1M,2J,2L, 3M,6E-6G,6J, 7B,7I,7J,8D
Vcc(gnd) Vca(gnd) Vee(-5.2)	12 1 24	U5E

RESISTOR PACK DESCRIPTIONS:





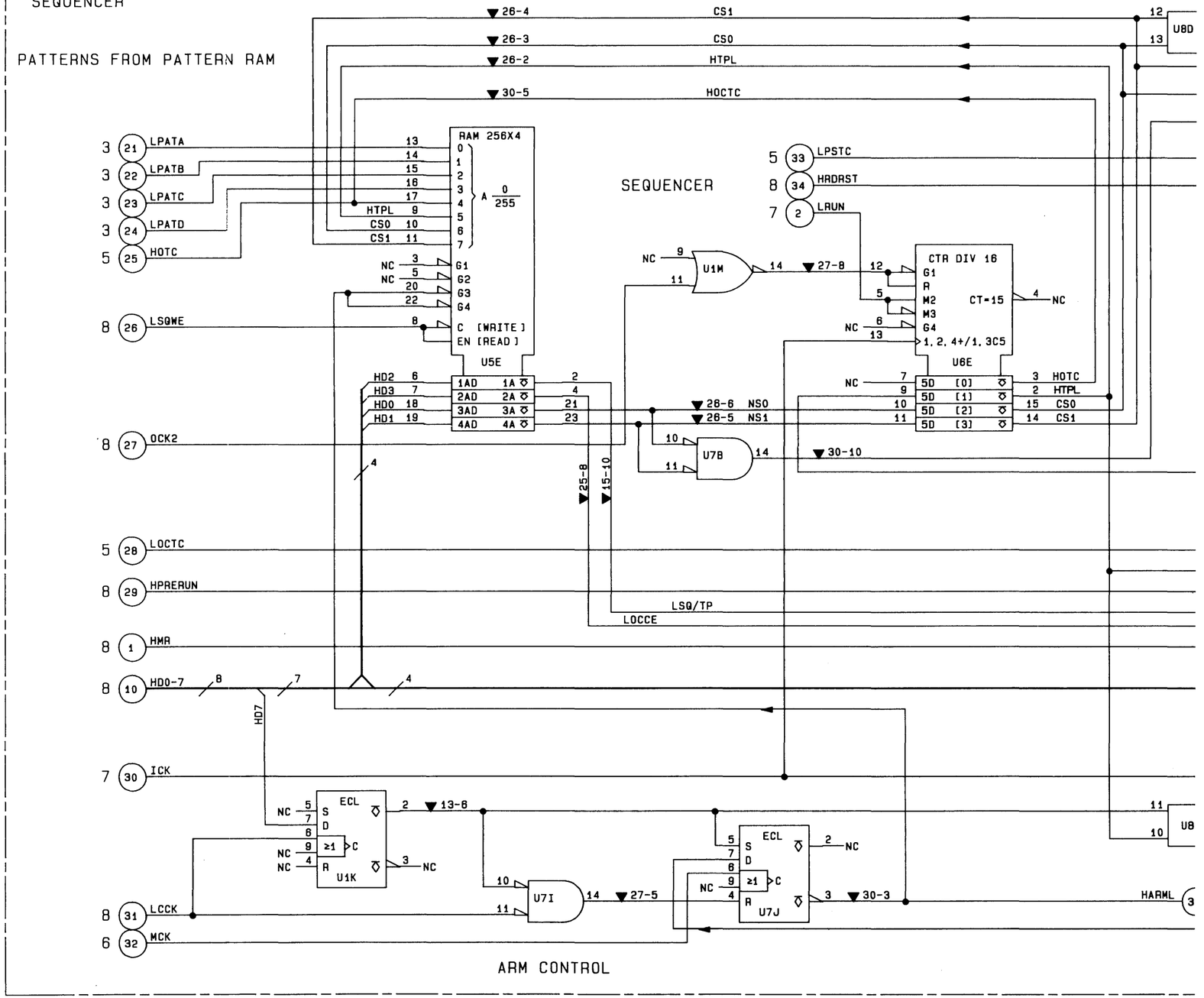
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U1K,M,2J,L,3M, U5E,6E-G,J,7B, U7I,J,8C,D C56 R3 RP12-15,17,25-28 30,33	

P/O STATE BOARD SEQUENCER

PATTERNS FROM PATTERN RAM



ARM CONTROL

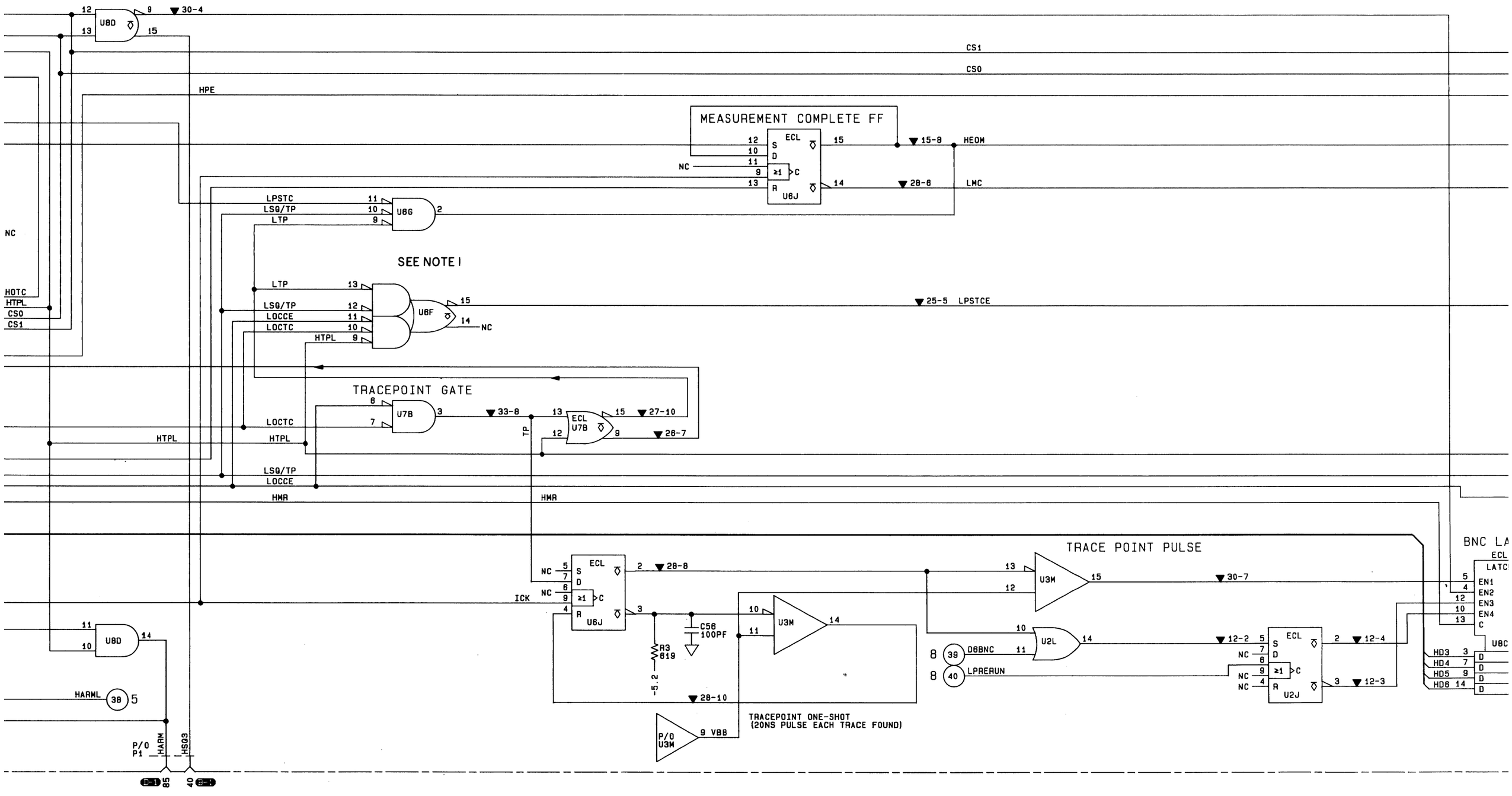

MEASUREMENT COMPLETE FF
ECL
U6J
U8D
U6G
U6F
SEE NOTE 1
TRACEPOINT GATE
U7B
ECL U7B
TRACE POINT PULSE
U3M
U2L
U2J
U8D
C56 100PF
R3 619
-5.2
TRACEPOINT ONE-SHOT (20NS PULSE EACH TRACE FOUND)
P/O U3M
P/O P1
CS1
CS0
HPE
HEOM
LMC
LPSTCE
HOTC
HTPL
LOCTC
LSQ/TP
LOCCE
HMR
ICK
TP
HARML
HARM
HSQ3
D6BNC
LPREARUN
BNC LA
ECL
LATC
EN1
EN2
EN3
EN4
HD3
HD4
HD5
HD6
U8C
NC
30-4
15-8
28-8
25-5
33-8
27-10
28-7
28-10
30-7
12-2
12-4
12-3

Figure 8C-

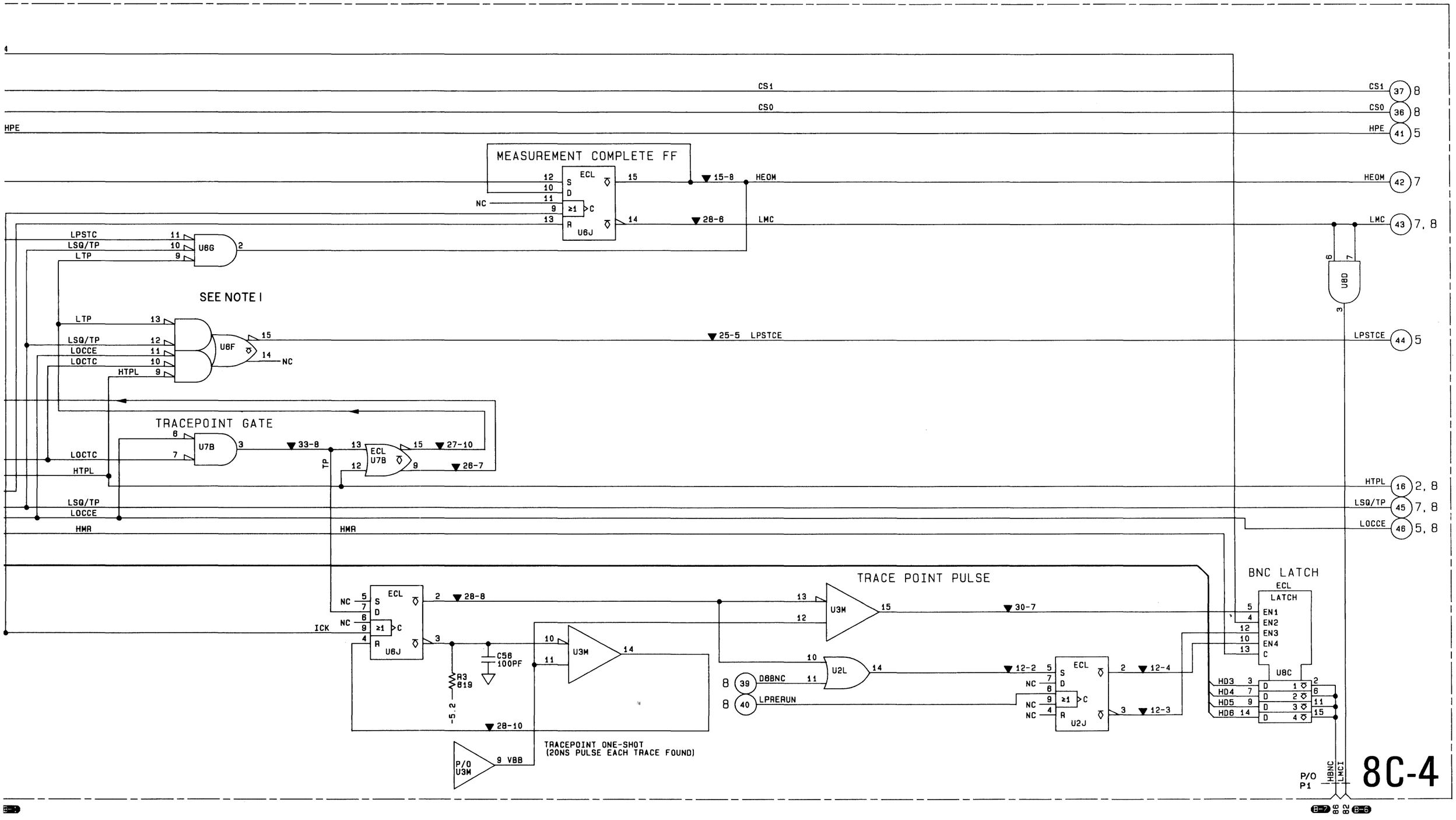


Figure 8C-16. State Schematic (4 of 8)

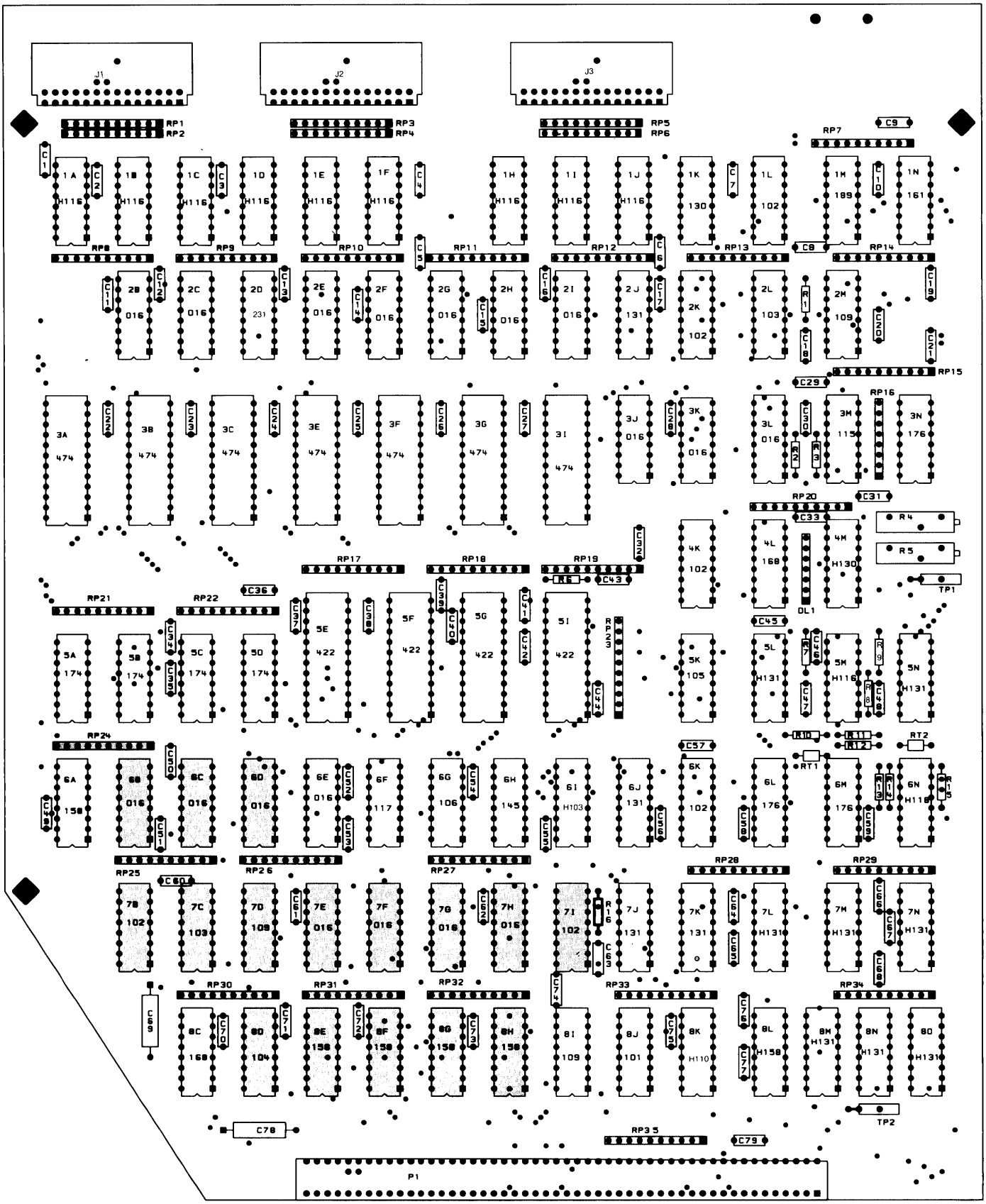
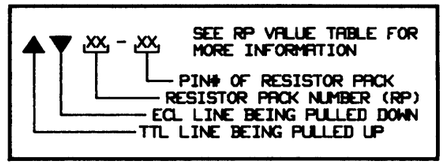


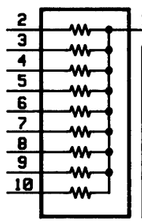
Figure 8C-15. State Board Component Locator

IC DEVICE
POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U6B-6D,7B-7I 8D
Vcc(gnd) Vee(-5.2)	16 8	U8E-8H

RESISTOR PACK DESCRIPTIONS:

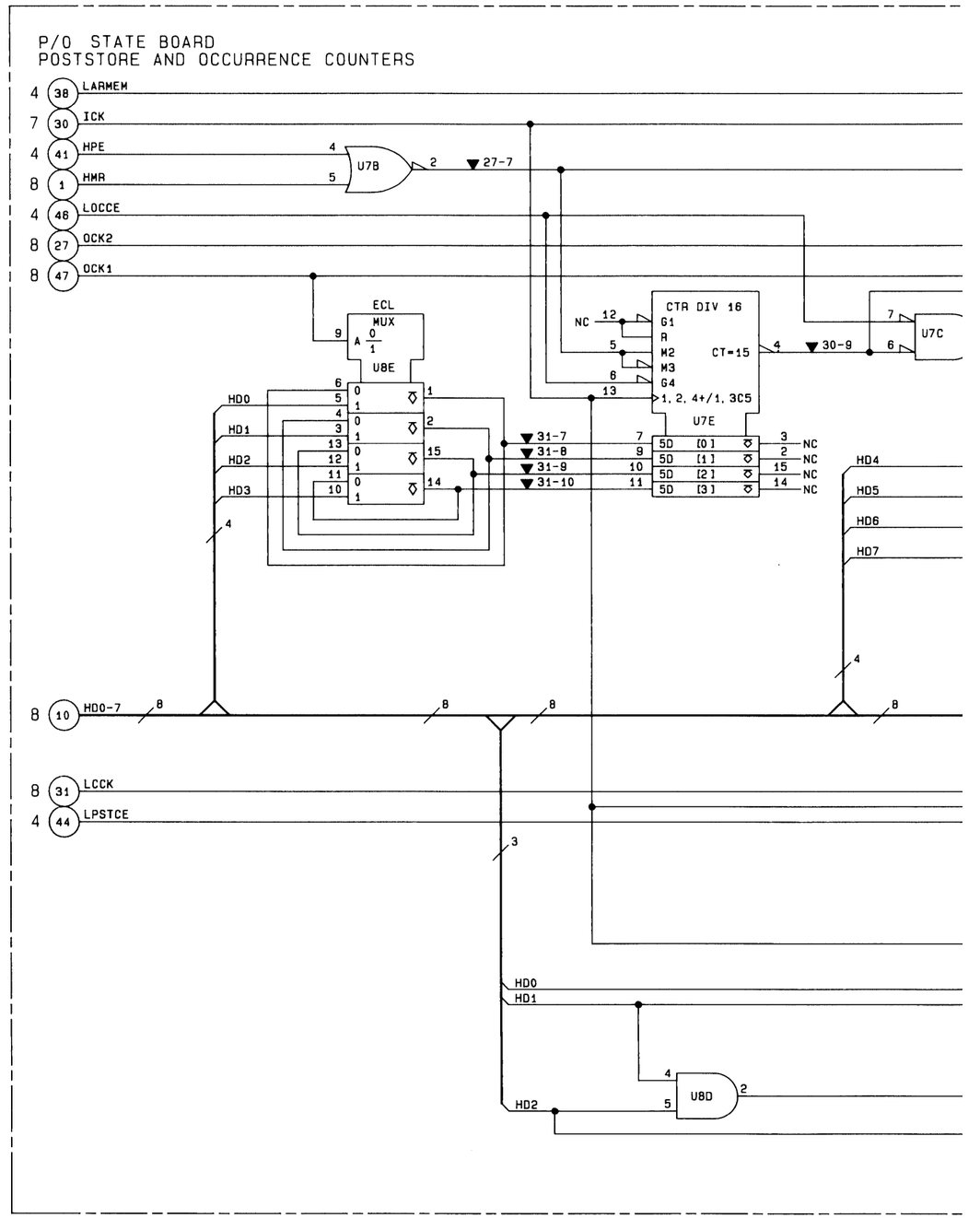




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U6B-D,7B-I, U8D-H RP24-27,30-32	



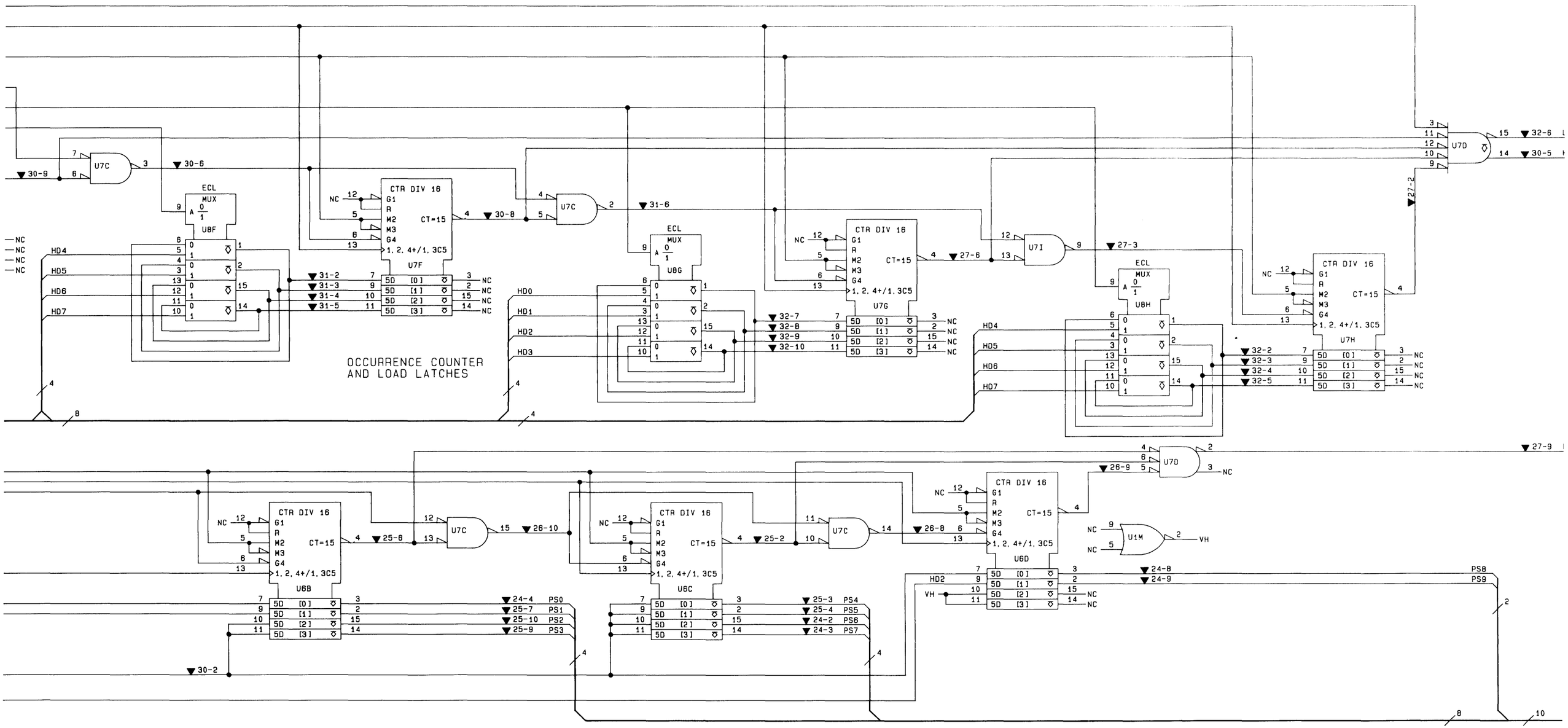

OCCURRENCE COUNTER
AND LOAD LATCHES
CTR DIV 16
ECL MUX
1, 2, 4+/1, 3C5
U7C
U7D
U7I
U7F
U7G
U7H
U8F
U8G
U8H
U6B
U6C
U6D
U1M
30-9
30-6
30-8
31-6
27-6
27-3
27-2
32-6
30-5
31-2
31-3
31-4
31-5
32-7
32-8
32-9
32-10
32-2
32-3
32-4
32-5
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
NC
27-9
26-9
26-8
26-10
25-8
25-2
30-2
24-4
25-7
25-10
25-9
25-3
25-4
24-2
24-3
24-8
24-9
PS0
PS1
PS2
PS3
PS4
PS5
PS6
PS7
PS8
PS9
VH

Figure 8C-

OCCURRENCE COUNTER
AND LOAD LATCHES

Figure 8C-16. State Schematic (5 of 8)

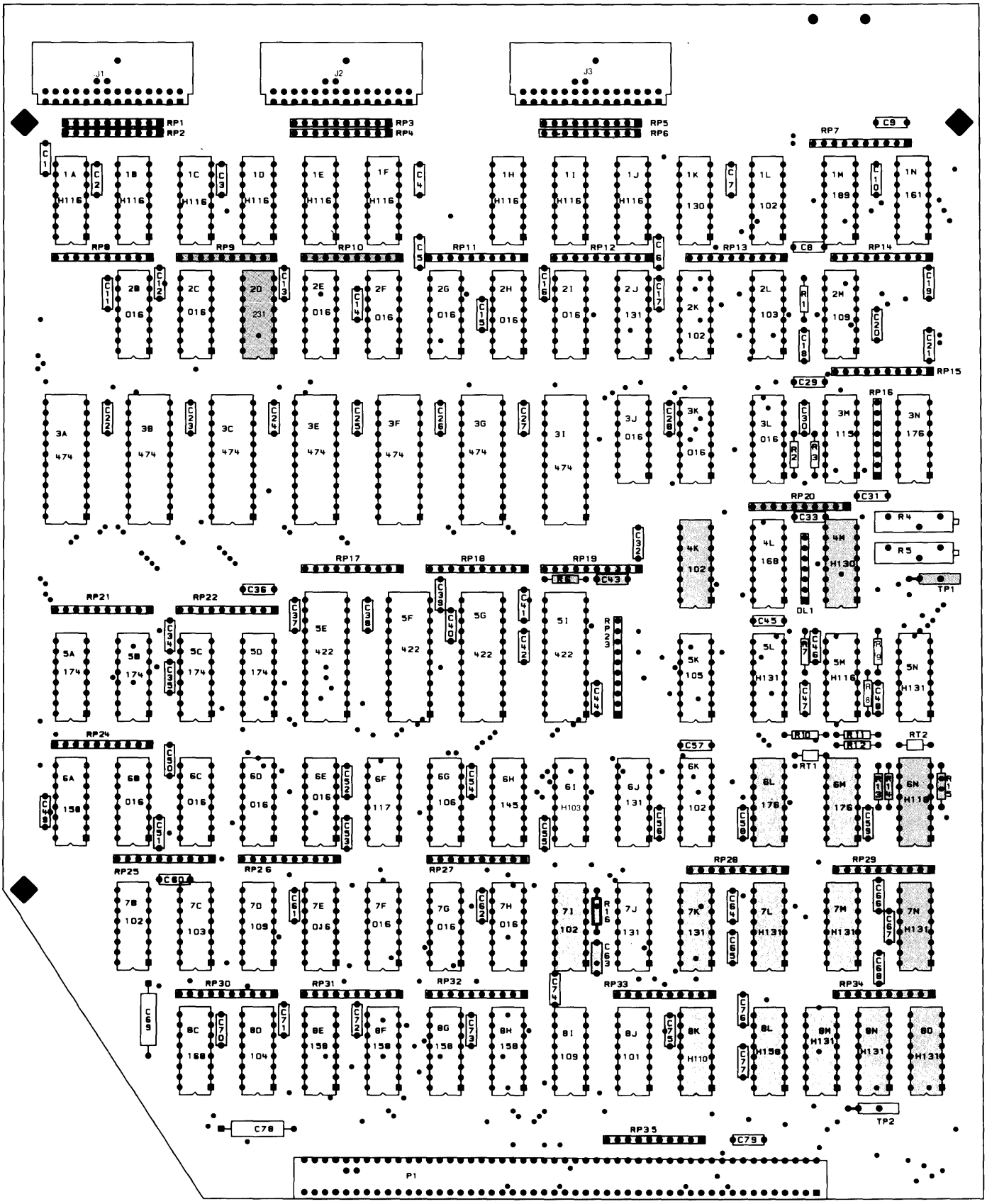
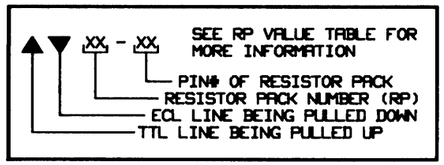


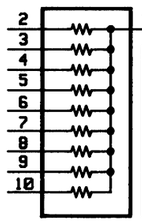
Figure 8C-15. State Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2D,4K,4M,6L-N, 7I,7K-N,8M-8D
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1,15 16 8	U8K
Vcc(gnd) Vee(-5.2)	16 8	U8L

RESISTOR PACK DESCRIPTIONS:

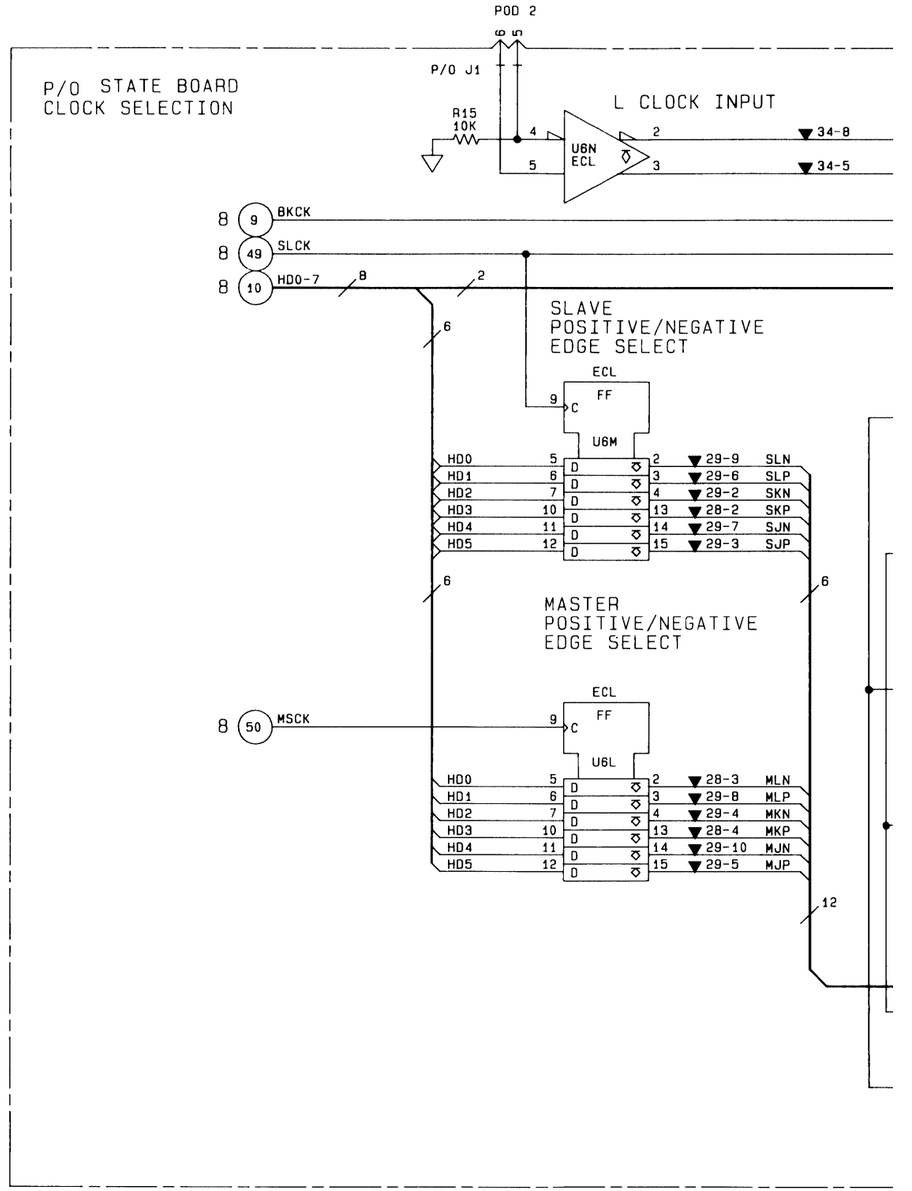




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U2D,4K,M,6L-M, U7I,K-N,8K-O C43,63 J1,2,3 R6,13-16 RP9,10,20,27-29, 33-35	



POD 3
P/O J2
INPUT
34-8
34-5
R14 10K
K CLOCK INPUT
U8N ECL
34-2
34-9
POD 4
P/O J3
R13 10K
J CLOCK INPUT
34-10
34-3
L CLOCK SELECT
K CLOCK SELECT
J CLOCK SELECT
U8M
U8O
U7M
U8N
U7L
U7N
SLN
SKN
SJN
MLN
MKN
MJN
SLP
SKP
SJP
MLP
MKP
MJP
29-9 SLN
29-6 SLP
29-2 SKN
28-2 SKP
29-7 SJN
29-3 SJP
28-3 MLN
29-8 MLP
29-4 MKN
28-4 MKP
29-10 MJN
29-5 MJP
HD6
HD7
U4M
U2D
U7K
POD 2 MASTER/SLAVE SELECTOR
U8L
9-7
33-3
SLAVE CLOCK OUT
U8K
9-4
10-4
28-9
CPU CLOCK FF
MASTER CLOCK OUT
20-2
TP1 MASTER CLOCK PULSE
27-4
33-2
34-4
34-7
33-4
MASTER ONE-SHOT RETURN
U4K
R16 619
-5.2
U7I
C6C 100PF
35-2
SLAVE ONE-SHOT RETURN
HSCS
HSCN
E-1 OR F-3
D-1

Figure 8C-

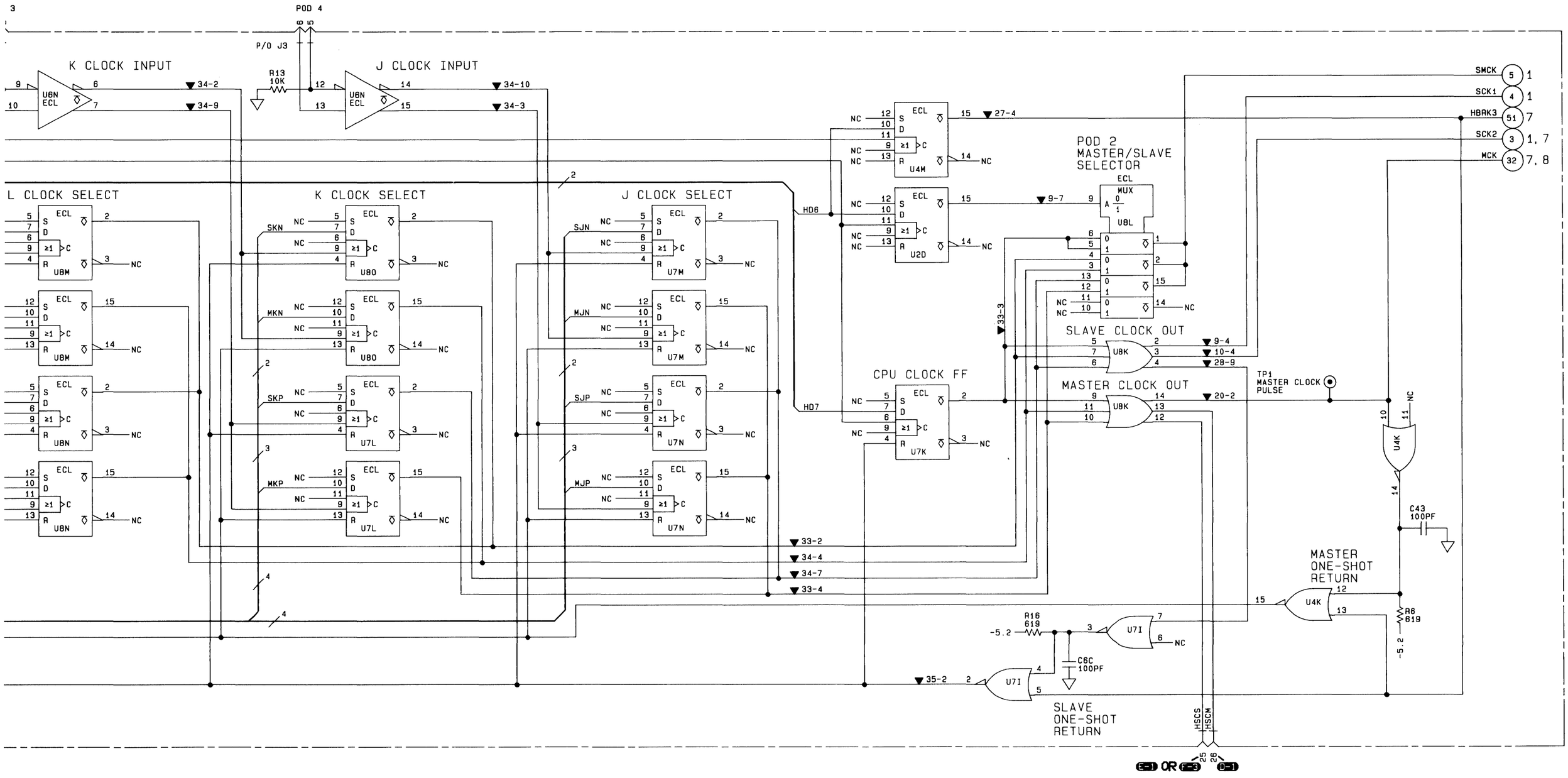
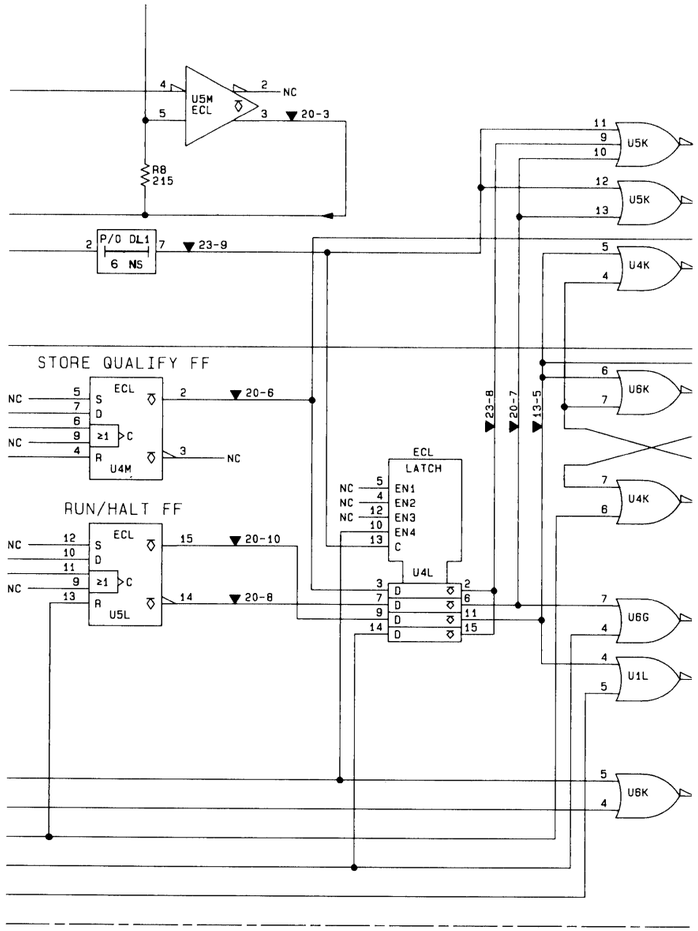


Figure 8C-16. State Schematic (6 of 8)

Figure 8C-15. State Board Component Locator

NOTE 1

ON STATE MASTER BOARD 01630-66505, THE SCHEMATIC BELOW REFLECTS THE USE OF A DIFFERENT PART 1820-2451 (MC10168P) FOR U4L, AND THE CIRCUIT DIFFERENCES THAT ACCOMMODATE THAT PART.



NOTE 2

ON STATE MASTER BOARDS 01630-66505 AND 01630-66509, DELAY LINE DL1 IS MADE 7ns BY MAKING THE OUTPUT CONNECTION TO PIN 7 RATHER THAN PIN 6.

NOTE 3

ON STATE MASTER BOARD 01630-66505, U4M PIN 4 IS CONNECTED TO U3N PIN 14 (8C-2) AND U6K PIN 5 IS CONNECTED TO U3N PIN 15 (8C-2).

IC DEVICE POWER CONNECTIONS

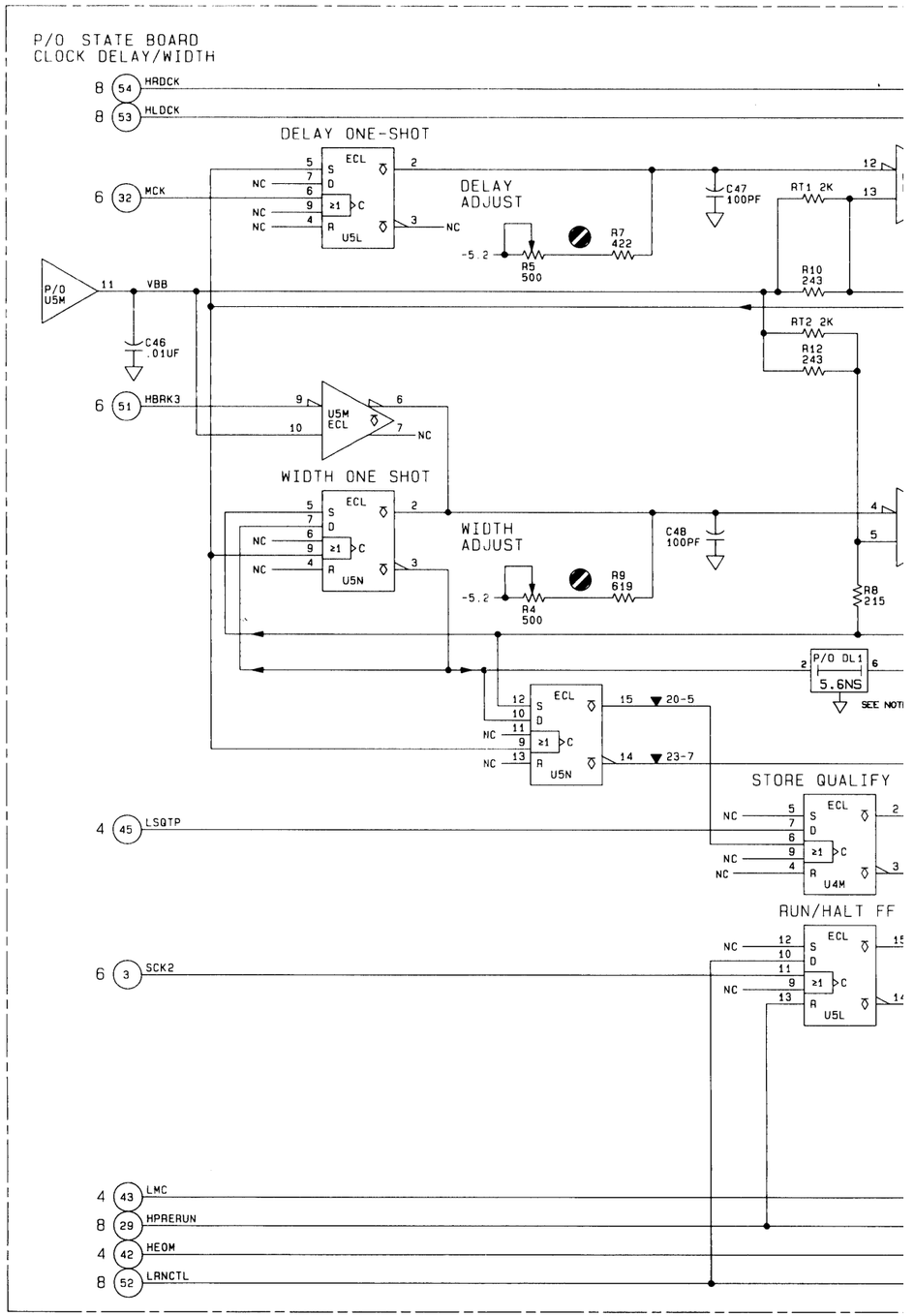
SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1L,4K-4M, 5K-N,6G,K, 7J

RESISTOR PACK DESCRIPTIONS:

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

C46-48,65 DL1 R4-5,7-12 RP8,11-14,20,23-24, 28,33 RT1,2 TP2	U1L,4K-M,5K-N, U6G,8J



CE
CTIONS

IC GROUP
U1L, 4K-4M, 5K-N, 6G, K, 7J

SCRIPTIONS:

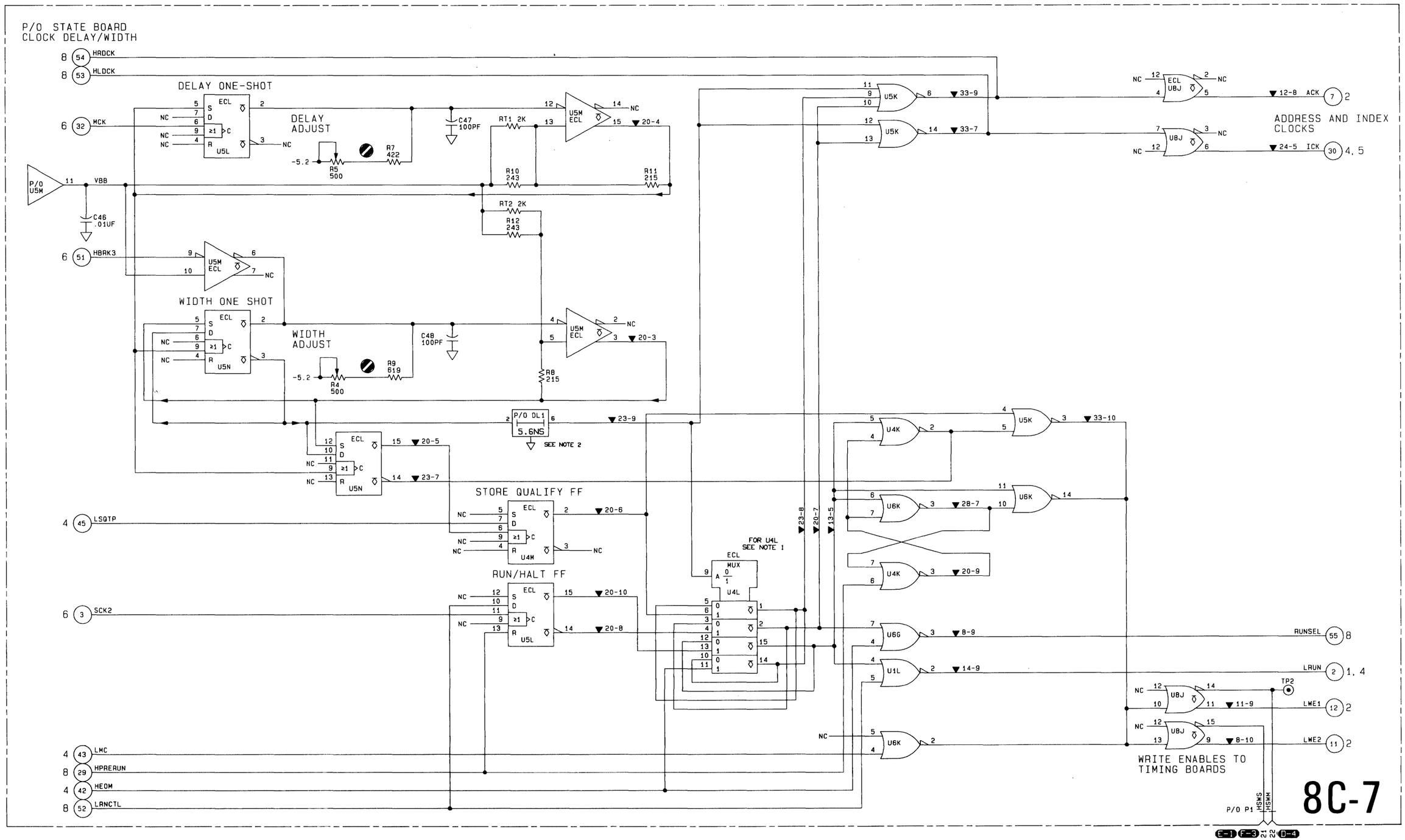
VALUE TABLE FOR FORMATION

RESISTOR PACK PACK NUMBER (RP) ING PULLED DOWN NG PULLED UP

R	POWER PIN	VOLTAGE
	1	-5.2
	1	-2.4

SCHEMATIC

L, 4K-M, 5K-N, G, 8J



8C-7

Figure 8C-16. State Schematic (7 of 8)

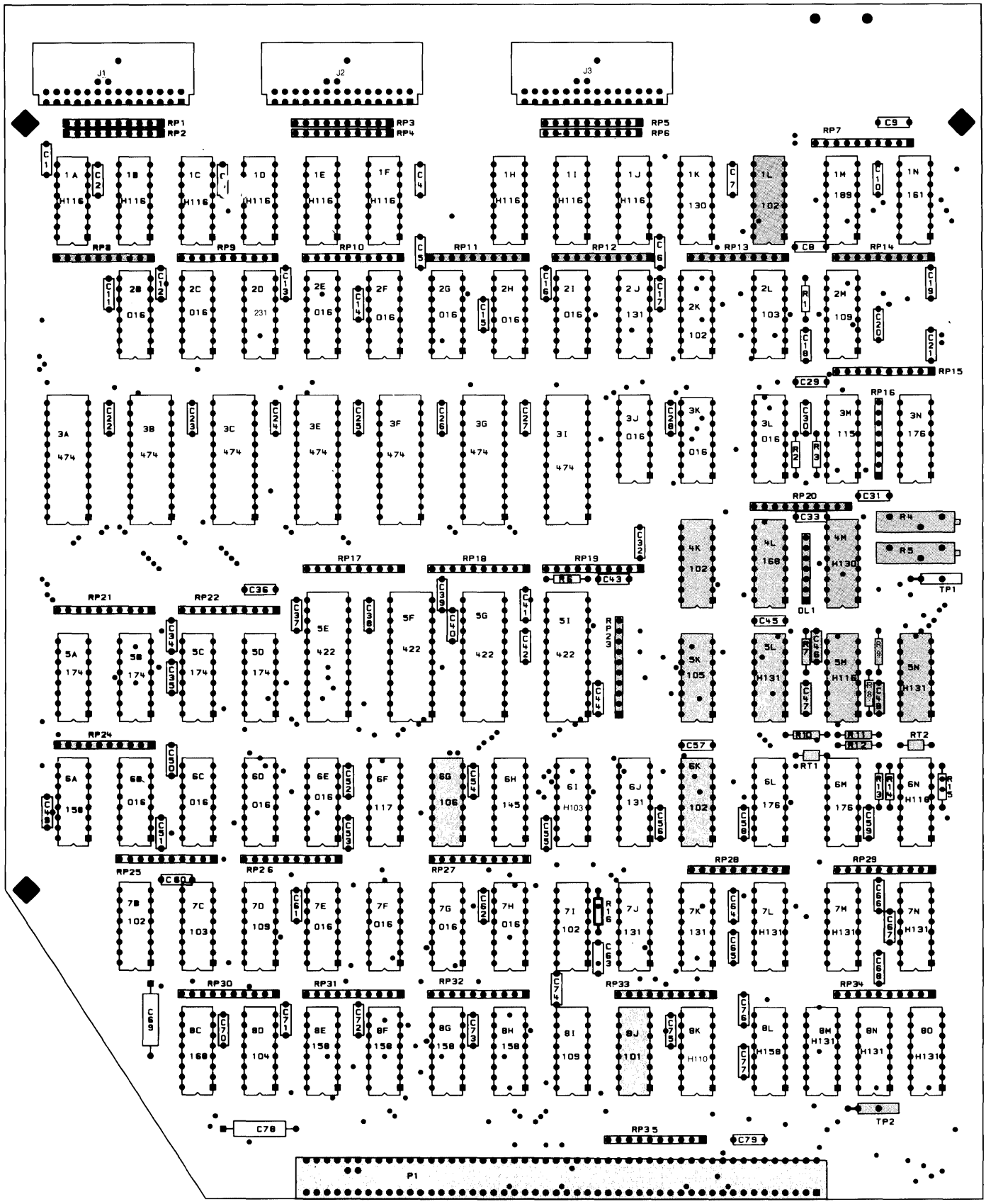
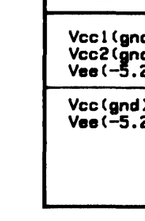


Figure 8C-15. State Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1K-1N,2L-2N, U3M,5A-5D,6K, 7J-7K,8I
Vcc(gnd) Vee(-5.2)	16 8	U6A

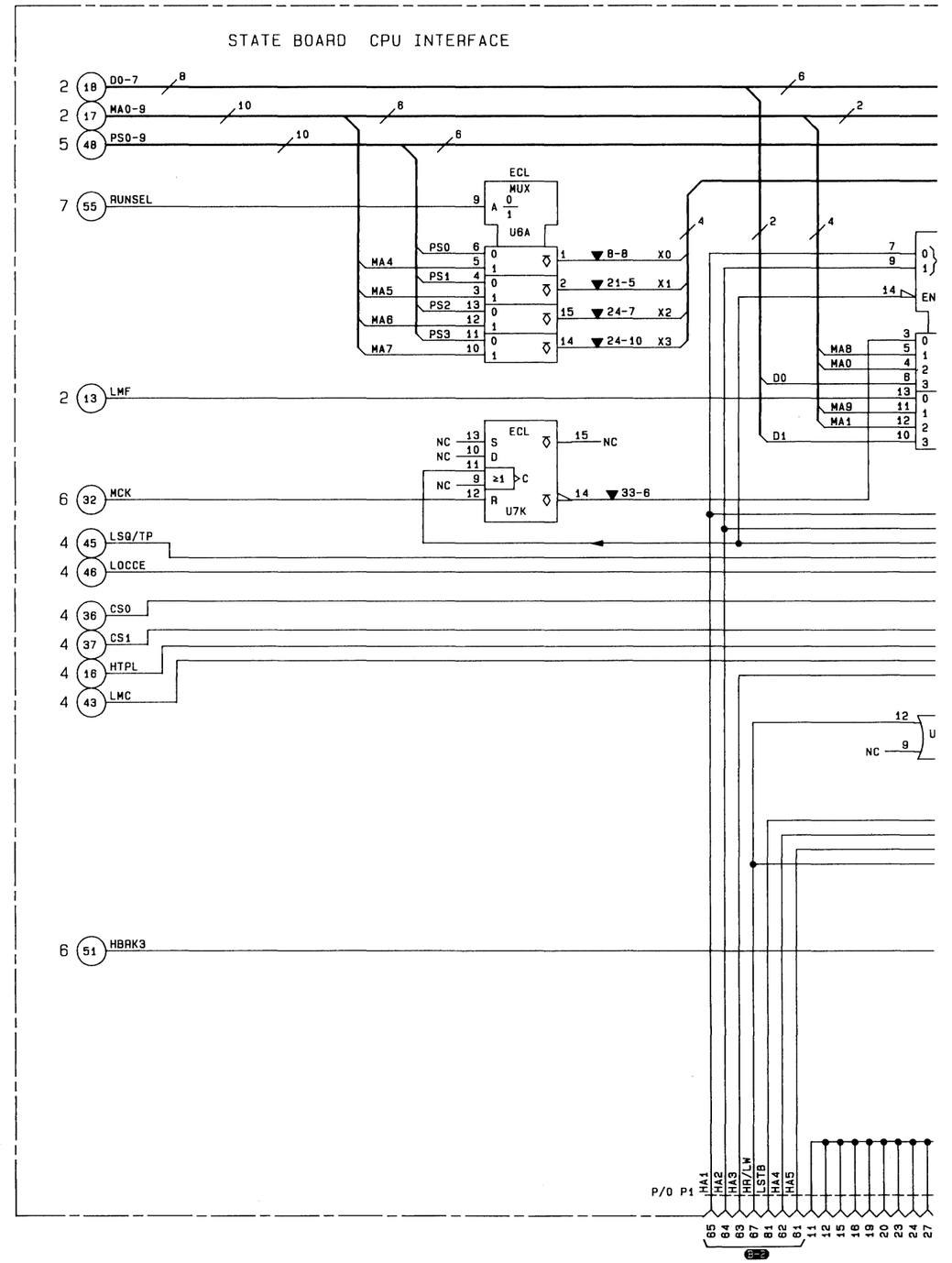
RESISTOR PACK DESCRIPTIONS:



RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U1K-1N,2L-2M;3M, 5A-5D,6A,K,7J,K,8I C1-42,44-45,49-55, C57-62,64-79 R1,2 RP7-8,13-16,21, RP23,24,28,33,34	



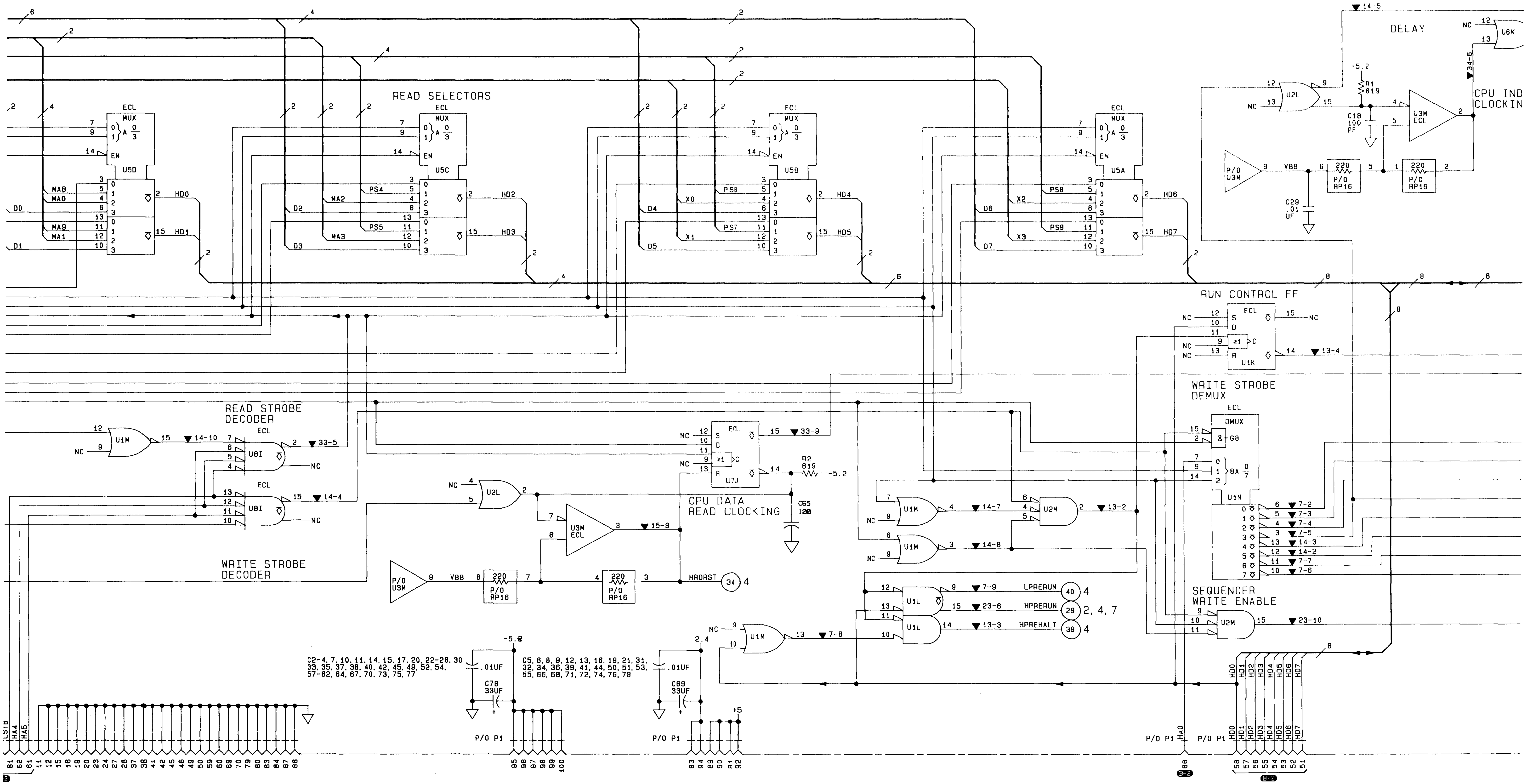

READ SELECTORS
DELAY
CPU IND
CLOCKIN
RUN CONTROL FF
WRITE STROBE
DEMUX
READ STROBE
DECODER
CPU DATA
READ CLOCKING
WRITE STROBE
DECODER
SEQUENCER
WRITE ENABLE
LPRERUN
HPRERUN
HPREHALT
HADRST
P/O P1

Figure 8C-

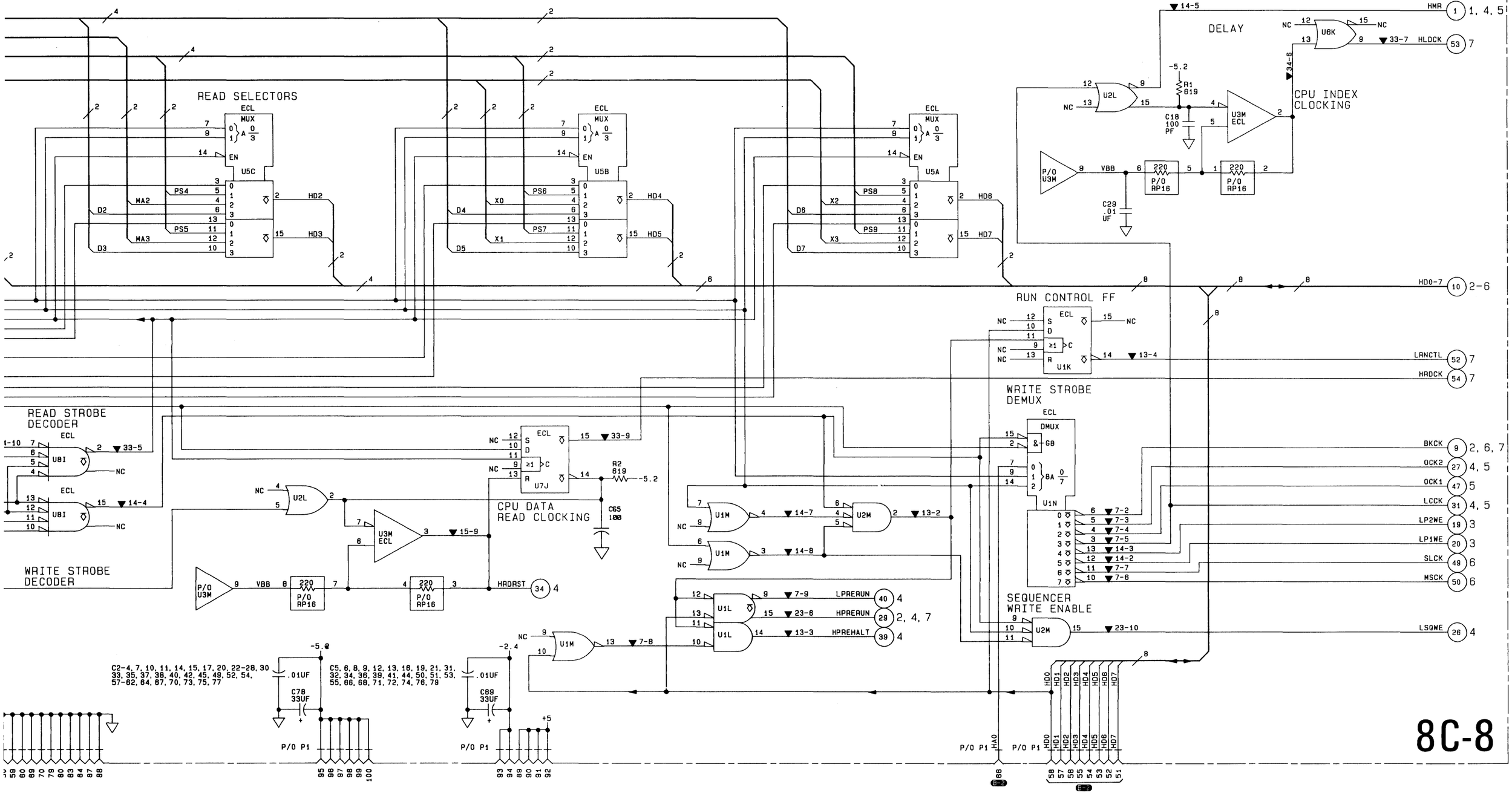


Figure 8C-16. State Schematic (8 of 8)

Service Group 8D Table of Contents

List of Illustrations

List of Tables

SERVICE GROUP 8D
TIMING MASTER

8D-1. INTRODUCTION

SAMPLING. The timing master board accepts eight channels from the timing probe. Samples come in as an 8-bit parallel word. Data is compared with thresholds from the CPU board: sampled levels above threshold are high; levels below are low. Storage capacity is 1024 8-bit words. Then, if no trigger pattern has been found, new data will continue to write over old.

SAMPLE RATE. The timing analyzer provides its own sample clocks, which may be varied for different resolutions. Sampling is therefore asynchronous with the system being measured.

TRIGGERING. Before a run the analyzer is programmed to look for a certain pattern of highs or lows on each parallel 8-bit sample. Four of the eight channels may also be programmed to trigger on glitches, or rising or falling edges. When a correct pattern of the proper duration occurs, the analyzer produces a trigger.

TRACEPOINT. The trigger may be delayed while information continues to be stored. Trigger + Delay is defined as Tracepoint.

POSTSTORE. The amount of new data stored after tracepoint determines tracepoint position in displayed memory. Start, Center, or End are the options. For End-on, measurement is stopped immediately after tracepoint, causing about 1K of pre-tracepoint data to be displayed. For Start-on, almost 1K of new data is stored before stopping the measurement, causing tracepoint to be displayed at the beginning.

ARMING. The timing analyzer may be prevented from looking for the trigger pattern until enabled by the state analyzer. The timing trigger may also arm the state analyzer.

8D-2. TIMING BLOCK DIAGRAM THEORY (Figure 8D-1)

PROBE INTERFACE. Collects data from eight pod channels.

MACROCELL. There are two of these custom chips on both the master and slave timing boards. Four of the eight pod channels go into each macrocell. After storing four parallel 4-bit samples, each macrocell outputs a 16-bit word to the RAM at one-fourth the sample rate. Besides this data encoding function, the macrocells contain data and glitch pattern detectors: when an 8-bit sample contains proper pattern, the macrocells emit a trigger signal.

ACQUISITION RAM. This is a 256 x 32 RAM, which is loaded by a 32-bit word from the macrocells (each macrocell sends out 16 bits). The 32-bit word from the two macrocells contains four 8-bit samples. Effective memory size is 1K x 8.

MEMORY ADDRESS COUNTER (MAC). An 8-bit counter which increments at one-fourth the sample rate, as each 32-bit macrocell word is stored in acquisition RAM.

TRACEPOINT LATCH. Saves the contents of the Memory Address Counter when tracepoint occurs.

MEMORY BLOCK SELECT. Chip Select signals for acquisition RAM.

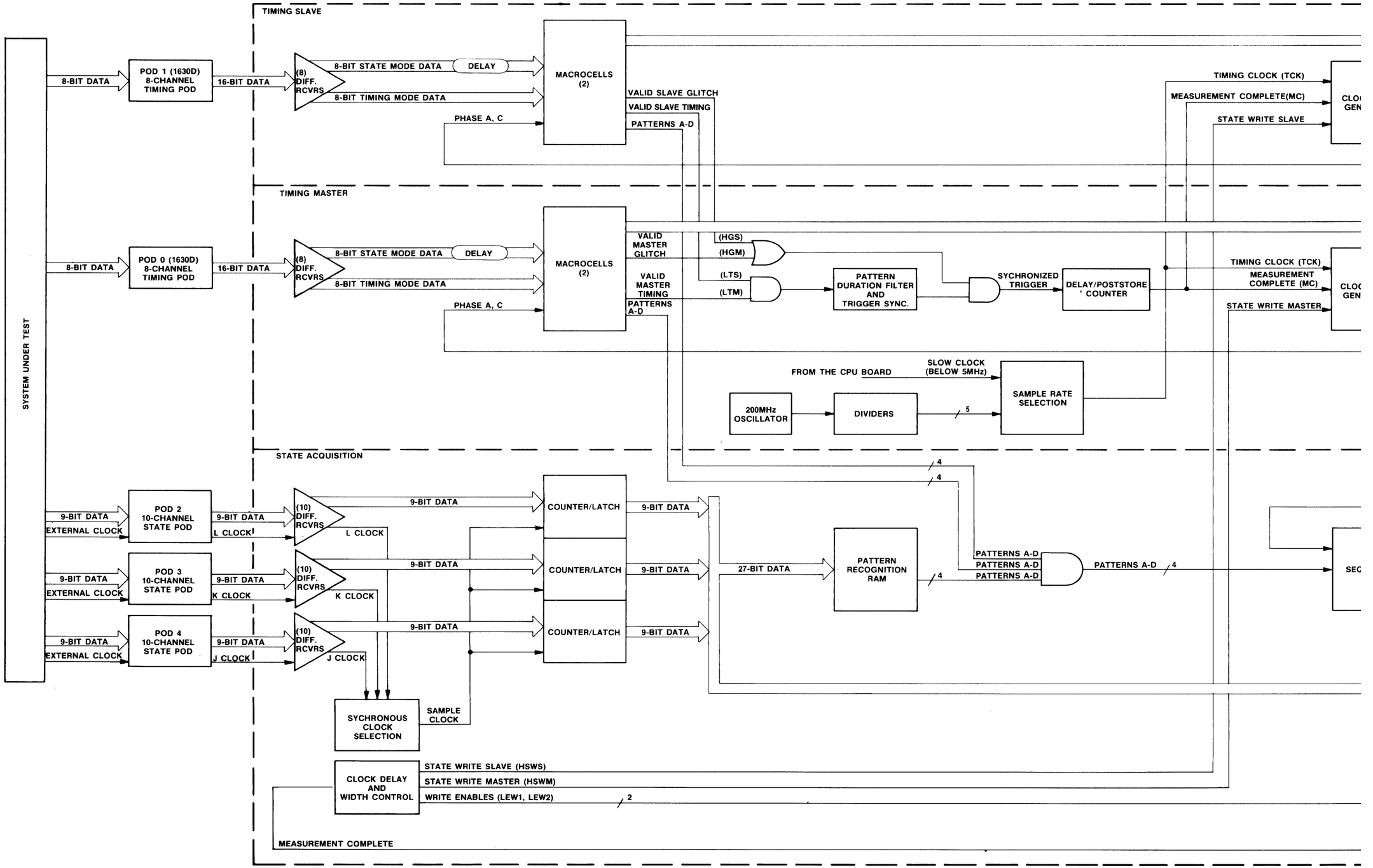
PATTERN DURATION FILTER. Determines whether a trigger pattern lasts long enough.

DELAY/POSTSTORE COUNTER. A 16-bit counter for delaying the trigger by as much as four times 59,999 sample states. Five of the counter outputs are decoded for Poststore. The amount of data stored after the trigger determines trigger position in displayed memory for Start, Center, or End measurements. Terminal count becomes Measurement Complete (MC). The selected decoded output becomes Tracepoint (TP).

CLOCK GENERATION/SELECTION. Contains a 200 MHz oscillator, and frequency selection multiplexers for choosing sample rate. The CPU supplies frequencies below 5 MHz.

PHASE GENERATOR. Divides the timing clock into four phases for running various analyzer functions. For example, to allow for settling time, memory is written on Phase D, and the Memory Address Counters are incremented on Phase B.

CPU INTERFACE. Allows CPU programming and interrogation.


TIMING SLAVE
SYSTEM UNDER TEST
8-BIT DATA
POD 1 (1630D) 8-CHANNEL TIMING POD
16-BIT DATA
(8) DIFF. RCVRS
8-BIT STATE MODE DATA
DELAY
8-BIT TIMING MODE DATA
PHASE A, C
MACROCELLS (2)
VALID SLAVE GLITCH
VALID SLAVE TIMING
PATTERNS A-D
TIMING CLOCK (TCK)
MEASUREMENT COMPLETE(MC)
STATE WRITE SLAVE
TIMING MASTER
8-BIT DATA
POD 0 (1630D) 8-CHANNEL TIMING POD
16-BIT DATA
(8) DIFF. RCVRS
8-BIT STATE MODE DATA
DELAY
8-BIT TIMING MODE DATA
PHASE A, C
MACROCELLS (2)
VALID MASTER GLITCH
VALID MASTER TIMING
PATTERNS A-D
(HGS)
(HGM)
(LTS)
(LTM)
PATTERN DURATION FILTER AND TRIGGER SYNC.
SYCHRONIZED TRIGGER
DELAY/POSTSTORE ' COUNTER
TIMING CLOCK (TCK)
MEASUREMENT COMPLETE (MC)
STATE WRITE MASTER
FROM THE CPU BOARD
SLOW CLOCK (BELOW 5MHz)
200MHz OSCILLATOR
DIVIDERS
5
SAMPLE RATE SELECTION
STATE ACQUISITION
9-BIT DATA
EXTERNAL CLOCK
POD 2 10-CHANNEL STATE POD
L CLOCK
POD 3 10-CHANNEL STATE POD
K CLOCK
POD 4 10-CHANNEL STATE POD
J CLOCK
(10) DIFF. RCVRS
COUNTER/LATCH
27-BIT DATA
PATTERN RECOGNITION RAM
PATTERNS A-D
SYCHRONOUS CLOCK SELECTION
SAMPLE CLOCK
CLOCK DELAY AND WIDTH CONTROL
STATE WRITE SLAVE (HSWS)
STATE WRITE MASTER (HSWM)
WRITE ENABLES (LEW1, LEW2)
2
MEASUREMENT COMPLETE

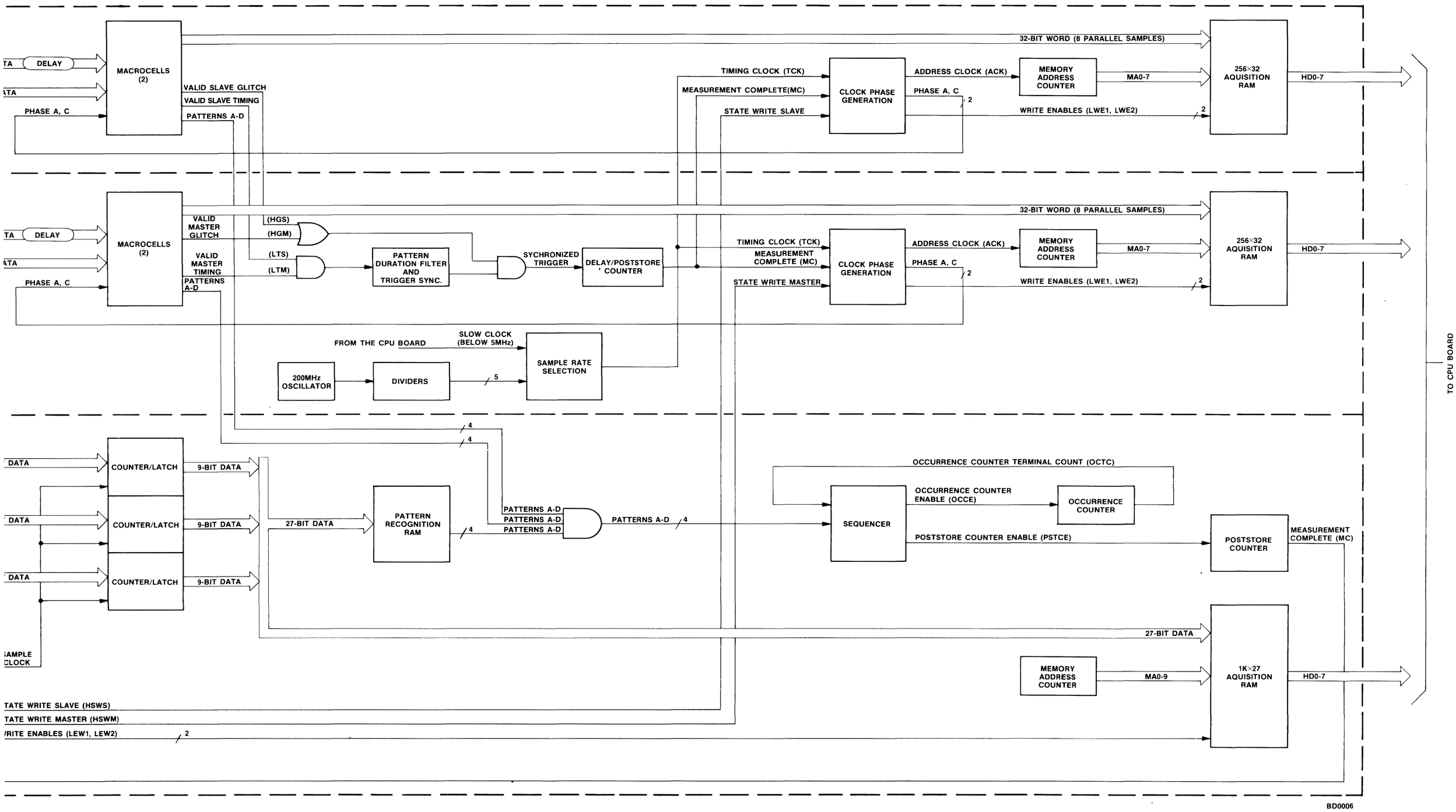
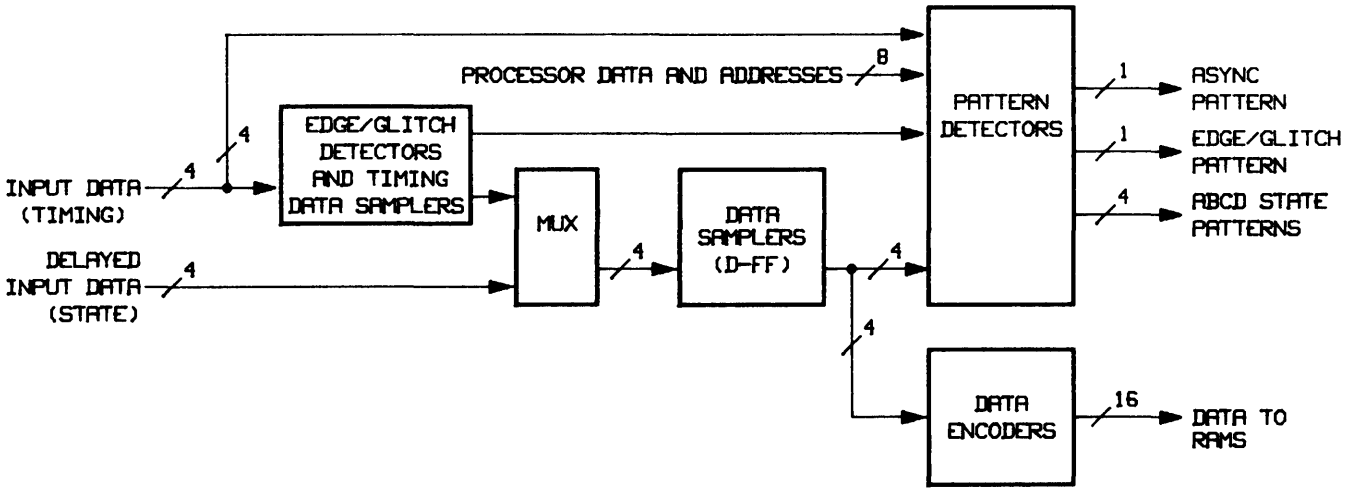


Figure 8D-1. 1630A/D Acquisition System



CAUTION

Refer to Paragraph 8-15 and 8-16 for removal and installation of macrocells and their heat sinks.

CAUTION

When either master or slave timing boards are installed in the service slot in the upright position, forced air must be maintained across the macrocell heat sinks.

Figure 8D-2. Macrocell Block Diagram

8D-3. THEORY OF OPERATION

8D-4. Timing Pod and Pod Interface

8D-5. TIMING POD (see Figure 8D-10). The timing pod compares eight data channels against a single threshold, and converts each single input to two complementary ECL inputs for transmission to the timing board.

8D-6. LINE RECEIVERS (see Figure 8D-12, schematic 1). The Line Receivers convert the differential ECL signals from the pod to two single-ended outputs. One set of outputs is delayed by 19 ns to guarantee zero hold time on data in the State Mode. The other set of outputs goes directly into the macrocells for use in the Timing Mode.

8D-7. Macrocells (see schematic 8D-1)

There are two macrocells, each handling four channels, on both the primary and optional secondary timing boards. The macrocells are a custom gate array. The design can be broken down into four functional blocks:

1. Data Samplers.
2. Edge Detectors.
3. Data Encoders.
4. Pattern Detectors.

8D-8. DATA SAMPLERS. The Data Samplers clock in data for State, Time, or Glitch Modes.

8D-9. EDGE DETECTORS. The Edge Detectors find edges in the Timing Mode by looking for a transition on data between sample clocks. Two of the four macrocell input channels have edge detectors, allowing 4-channel glitch detection and triggering on each group of eight timing channels. For each data input with glitch detection, there are two positive and two negative edge detectors.

8D-10. DATA ENCODERS. The Data Encoders convert four parallel bits of high speed sampled data into 16 parallel bits of low speed data for writing into acquisition RAM. In State Mode the data encoders pass the sampled data directly to the 16 outputs, each bit of sampled data being output on four pins.

8D-11. PATTERN DETECTORS. The Pattern Detectors look for 1/0/X on each of the data inputs. During Halt, the CPU programs the specified pattern into the macrocells' internal registers. When the proper combination of highs, lows, don't cares, or glitches occurs, the macrocells will emit either LTM or HGM. LTM goes true when the preselected pattern is valid at the pod input. HGM is true whenever the correct glitch pattern appears on the selected data channels.

8D-12. STATE MODE. In State Mode the macrocells serve the same purpose as Pattern Recognition RAM on the state board. Four patterns, A-D, may be stored in the macrocells internal registers. The state pattern detectors look at the sampled data, while the timing pattern detectors look directly at the input data (and at the edge detector outputs, when in Glitch Mode).

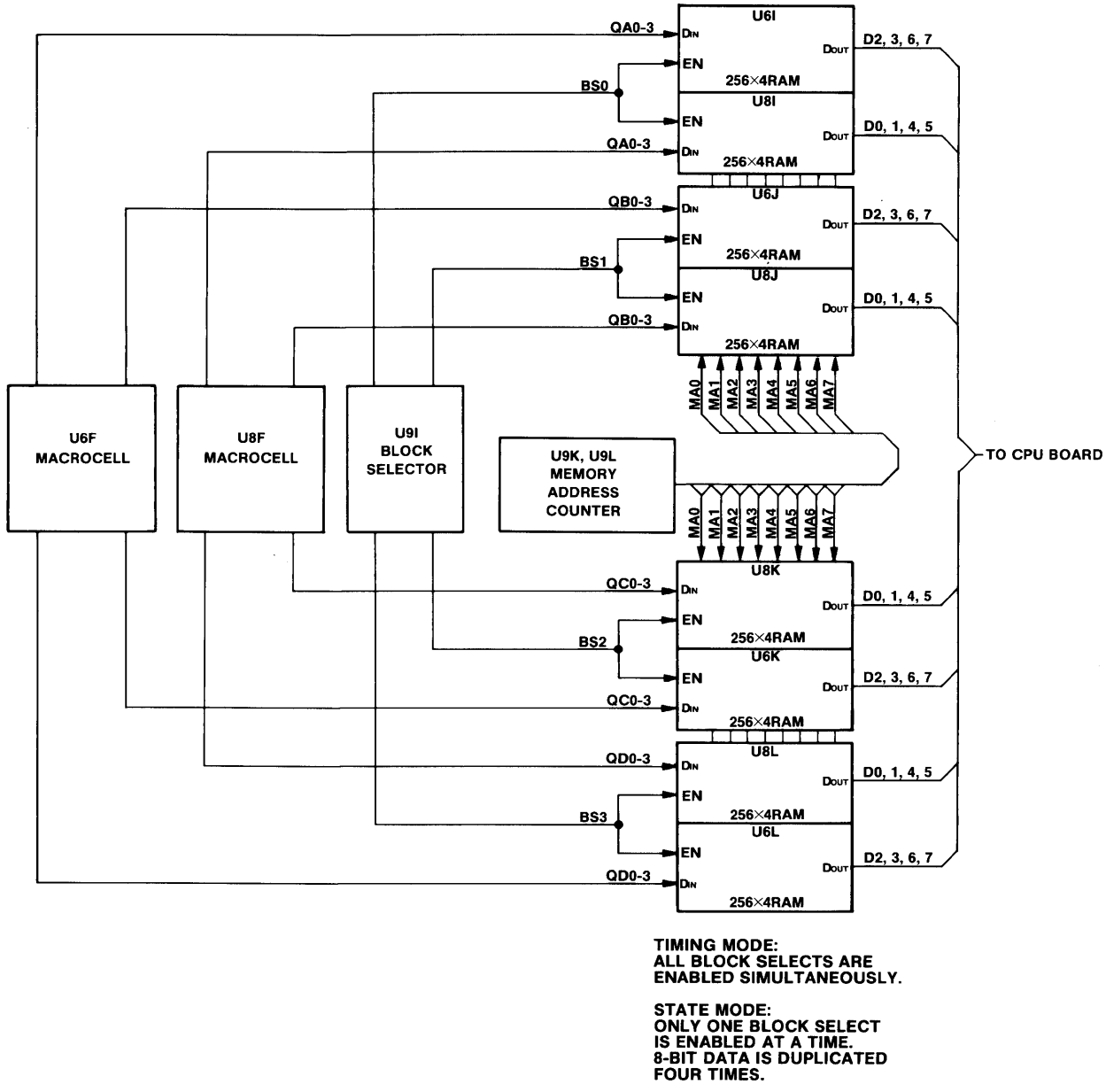


Figure 8D-3. Acquisition Memory and Memory Address Counter

8D-13. Acquisition RAM (see schematic 8D-1)

The RAM is organized 32 bits wide by 256 words deep. Since the 32-bit output data from the two macrocells is demultiplexed or fanned out to four times its width of eight channels, it is loaded into RAM at one-fourth of the sample speed, 32 bits at a time.

Each 16-bit parallel word from one macrocell contains four 4-bit data samples. The RAM for each macrocell is therefore, in effect, 1K x 4. With two macrocells and two groups of RAM, the effective memory size is 1K x 8.

8D-14. Memory Address Counter (see schematic 8D-1)

The Memory Address Counter is an 8-bit counter which keeps track of where data is being stored. Since memory is loaded 32 bits at a time, to a depth of 256, the counter only needs to count to 256 in order to store 1024 8-bit samples.

The Phase Generator increments the Memory Address Counter when writing during acquisition. The CPU increments the counter during reads.

The Memory Address Counter has three decoded outputs: MACTC1 (terminal count from the low order counter, U9K); MA7, the eighth, or most significant address bit; and MACTC2 (terminal count from the high order counter, U9L). These outputs indicate when the counter has counted 15, 128, or 240, i.e., the Start, Middle, or End of the 32 x 256 word memory.

8D-15. Block Select (see schematic 8D-1)

Memory chip-selects (U9I,9J) are controlled differently for State Mode, Timing Mode, and CPU Read Mode.

Timing Mode	All chip-selects are true. Four 8-bit samples are stored simultaneously as a 32-bit word.
State Mode	The 8-bit data word is now duplicated in four places on the macrocell outputs. At sample time, the Block Selector holds one chip-select true, enabling two 4-bit wide RAMs to store one byte. After four 8-bit samples, the Block Selector increments the Memory Address Counter. (see figure 8D-9).
CPU Read	Since RAM outputs are bussed 8 wide, two 4-bit RAMs at a time are enabled for reading. The Block Selector now enables two RAMs, as in State Mode; but now the Block Selector is clocked by the CPU clock, instead of the state sample clock.

8D-16. Memory Address Latches (see schematic 8D-1)

These latches hold the current memory address, allowing the CPU to unload memory at the end of a run. When Measurement Complete goes true, the CPU reads the latches to determine tracepoint position in acquisition memory.

8D-17. Memory Full Flip-Flop (see schematic 8D-1)

In the Run Mode the Memory Address Counter is continually running. When the counter has gone around once, reaching terminal count, the Memory-Full FF emits LMF, indicating memory has been completely filled at least once. The Memory Full FF is not reset until master reset occurs at the end of a run. The Memory Full FF ensures that the memory has been filled only with valid data.

8D-18. Prestore Valid Flip-Flop (see schematic 8D-1)

A trigger cannot occur until the Memory Address Counter indicates that memory has been sufficiently filled: For a Center-on measurement, half of memory must be filled; for End-on, all of memory; and even in Start-on, 56 samples are taken to allow a pre-trigger display.

Depending on whether the measurement is Start, End, or Center, one of the three memory address counter decoded outputs--MACTC1, MACTC2, or MA7--is selected to arm the trigger. This ensures a full load of prestore in the Timing Mode.

8D-19. Pattern Duration Filter (see schematic 8D-2)

The operator can specify minimum pattern durations. The Pattern Duration Filter determines whether the pattern trigger (LTM) from the macrocell satisfies a selected minimum time interval.

The Pattern Duration Selector (U4C) chooses the minimum pattern duration. Depending on the duration selected, one or more of its outputs will turn on differential pairs in the transistor arrays (U2A,3A,3B). The transistors switch in different RC time constants, causing the output of U2D-14 to ramp down at different rates. The ramp must decline fast enough to reach Schmitt Trigger threshold before the input signal goes low again.

As shown in Figure 8D-4, the transistors are merely switches which connect different sets of resistors and capacitors into the circuit. The resistors provide an "R" multiplier of 2, 5, or 10; and the capacitors provide a "C" multiplier of powers of 10. As shown in Table 8D-1, the "R" multiplier times the "C" multiplier gives the time duration.

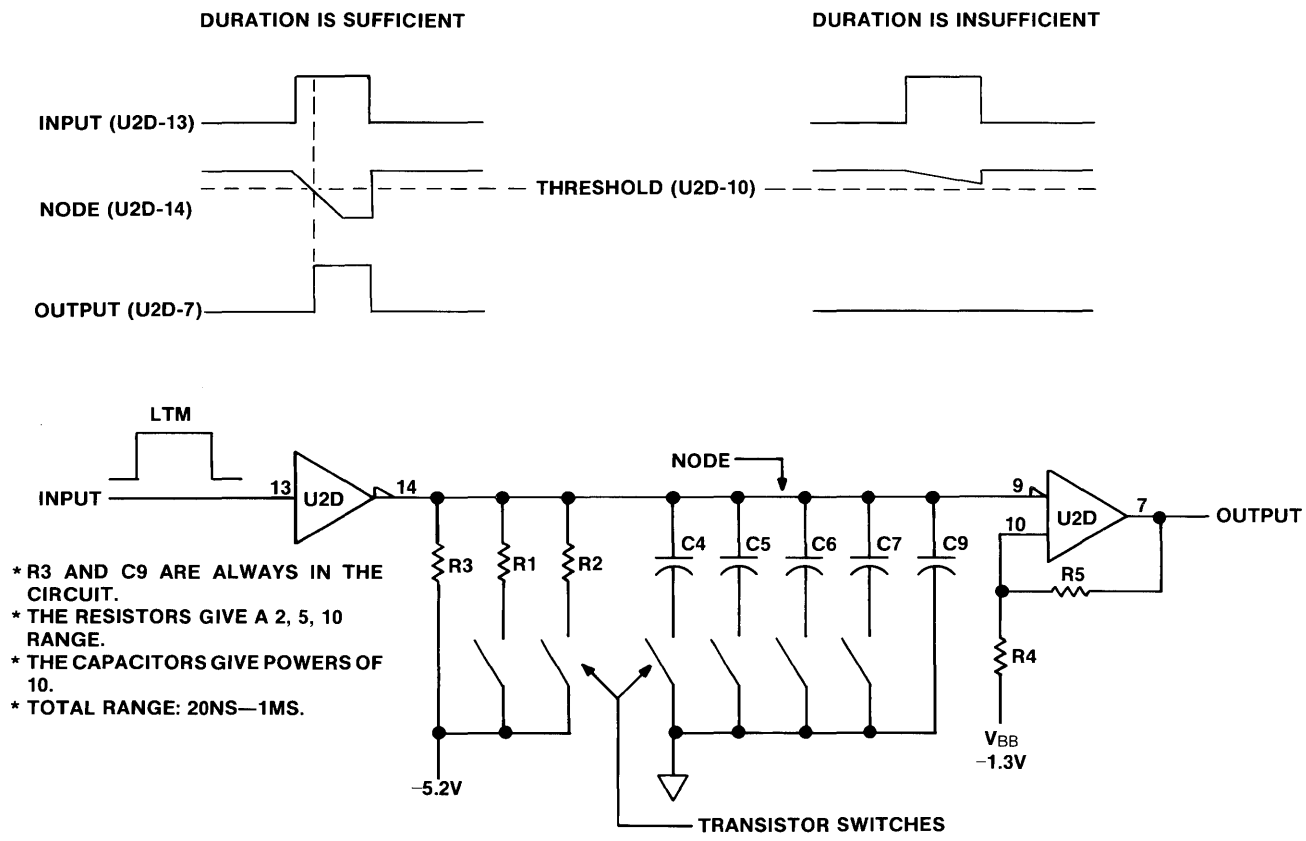


Figure 8D-4. Simplified Pattern Duration Filter

Table 8D-1. Resistor-Capacitor Combinations

RESISTORS	R MULTIPLIER
R3 (1.58K)	10
R1 || R3 (1.71K || 1.58k)	5
R1 || R2 || R3 (1.71k || 681 || 1.58k)	2
CAPACITORS	**C MULTIPLIER**
C9 (300pf)	10^{-8}
C7 (3600pf)	10^{-7}
C6 (.04µf)	10^{-6}
C5 (.4µf)	10^{-5}
C4 (4µf)	10^{-4}

R multiplier × C multiplier = seconds

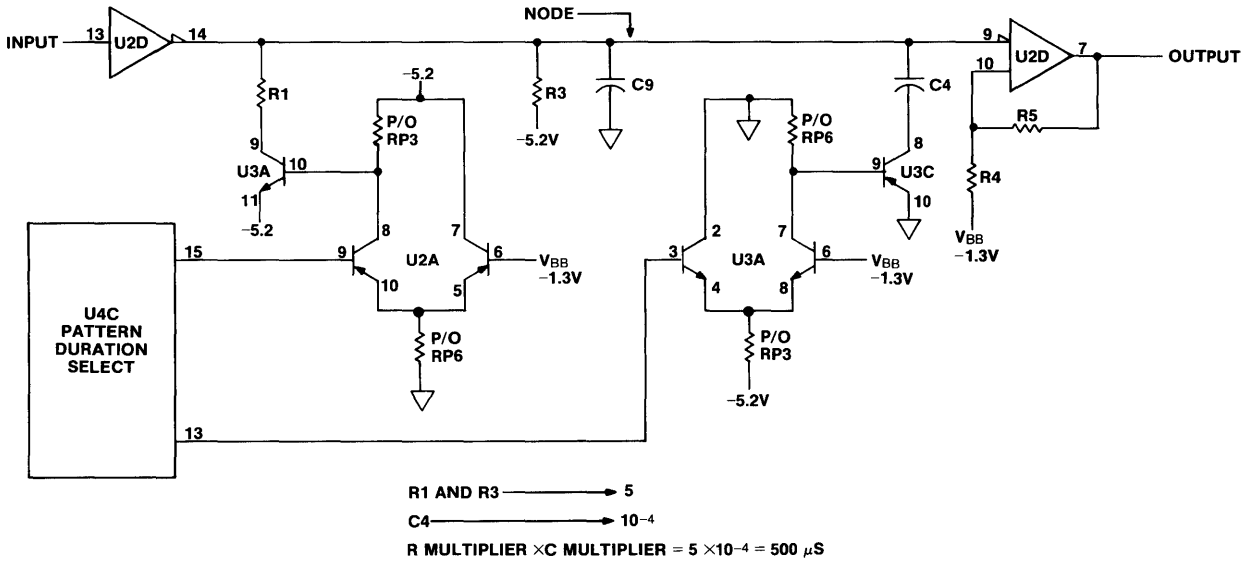


Figure 8D-5. Pattern Duration Path for 500 us

For the following Pattern Duration detailed theory see figure 8D-5 and table 8D-1.

Let's assume the operator has selected a minimum time interval of 500 us. We need a resistor multiplier of 5 and a capacitor multiplier of .0001. As shown in table 8D-1, R1 in parallel with R3 gives the resistor multiplier; and C4 gives the capacitor multiplier.

Pin 15 of the Duration Selector must go low to switch in R1; pin 13 must also go low to switch in C4.

A low on pin 15 turns on the left side of U2A, which then turns on U3A. R1 is now connected directly to -5.2V, putting it in parallel with R3. This gives us a resistor multiplier of 5.

A low on pin 13 turns on the right side of U3A, which turns on U3C. C4 is now connected to ground in parallel with the much smaller C9, which it swamps out. We now have C4 in series with the parallel combination of R1 and R3, which gives us a duration of 500 us.

8D-20. Glitch Flip-Flop (see schematic 8D-2)

The Glitch FF synchronizes the glitch trigger HGM, from the output of the macrocell, with the timing clock TCK2.

8D-21. Pattern Latch (see schematic 8D-2)

The Pattern Latch synchronizes the asynchronous pattern trigger from output of the pattern duration filter with the timing clock TCK2.

8D-22. Pattern Trigger Delay Shift Register (see schematic 8D-2)

Because the glitch trigger HGM is delayed in the macrocell relative to the pattern trigger LTM, the two need to be re-aligned before they can be ANDed at the input to the Combination FF (U3G-10). The Delay Shift Register delays the pattern trigger by four sample clocks to synchronize it with the glitch trigger.

8D-23. Trigger Flip-Flop (see schematic 8D-2)

LTM and HGM are wire-ANDed at the input to the Trigger FF (U3G-10), which synchronizes the ANDed trigger with the timing clock TCK2. The second half of the FF (U3G-7) latches the trigger high even after the pattern goes away.

8D-24. Sync Trigger Flip-Flop (see schematic 8D-2)

The Sync Trigger FF sychronizes the trigger with Phase C (LPHC), which is one fourth the sample rate (the rate that data is stored in memory).

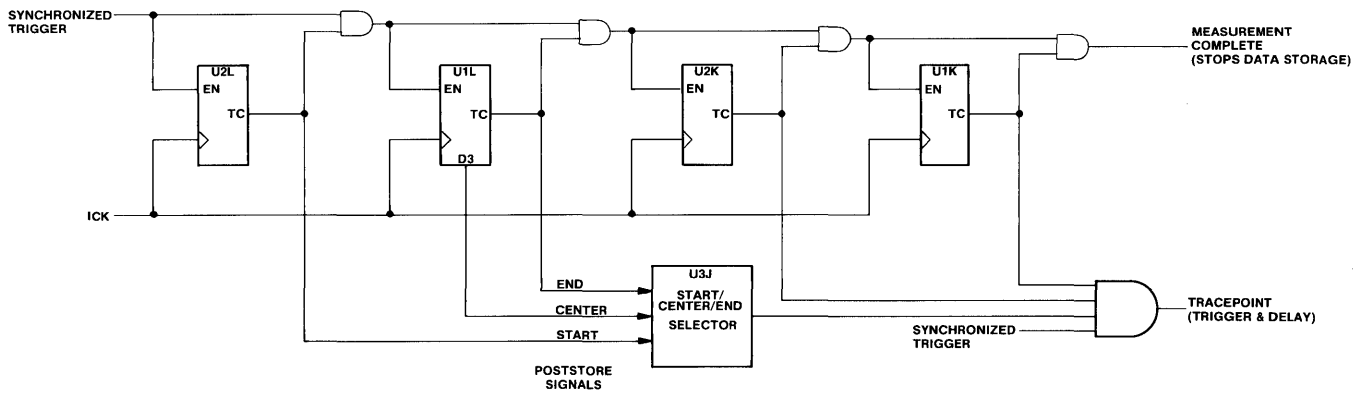


Figure 8D-6. Delay/Poststore Counter

8D-25. Delay/Poststore Counter (see schematic 8D-2)

When a valid trigger pattern is recognized, data will still continue to be stored. The trigger may be delayed by some amount. This delayed trigger is called Tracepoint--trigger + delay. And even when tracepoint occurs, the measurement may still not be stopped. The additional data stored after tracepoint is called Poststore--the distance in memory between Tracepoint and Measurement Complete. Poststore determines where tracepoint will be displayed--at the Start, Center, or End. Measurement Complete, then, equals trigger + delay + poststore.

8C-26. DELAY. When the operator wishes to observe data downstream from a valid trigger pattern, the CPU will pre-load the delay counter with the amount of delay desired before data storage is to be stopped. The valid trigger signal starts the delay counter. When the counter reaches terminal count (FFFFH), it stops further data storage--Measurement Complete.

For maximum delay, the CPU would load the counter to 0000H: then the counter must count all the way to FFFFH to reach terminal count. Minimum delay would be a pre-load of FFFFH, since terminal count then occurs immediately. Because the counter runs at one-fourth the sample rate, maximum possible delay, plus poststore, is four times 65,536 samples.

8D-27. POSTSTORE. Assuming no delay, the counter would be loaded to the following values for Start, Center, or End trace.

START: FF0FH

CENTER: FF80H

END: FFF0H

For Start, Center, and End, display memory will therefore contain the proportions of prestore and poststore data shown in figure 8D-7.

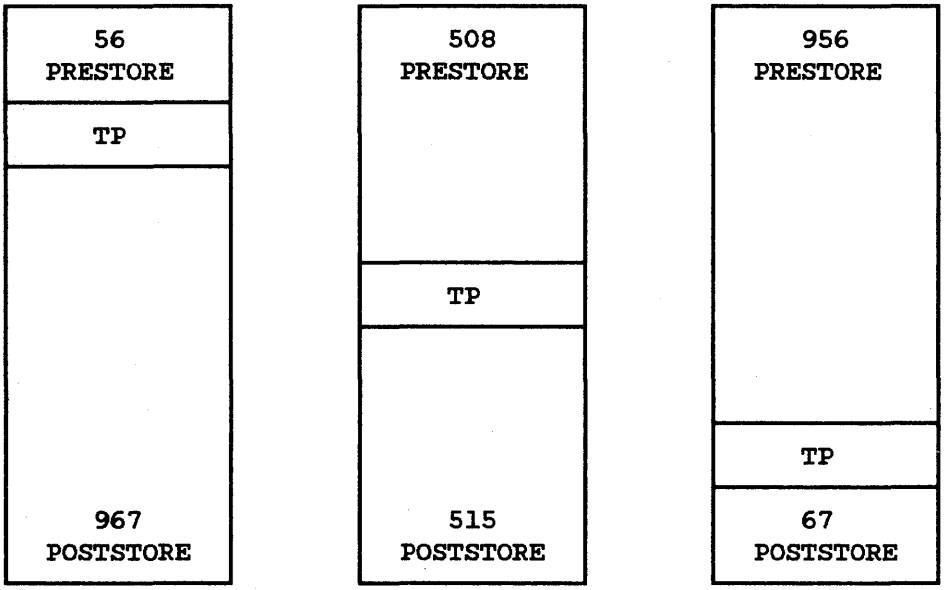


Figure 8D-7. Start/Center/End Proportions

8-28. START-TRACE. For Start-Trace, the counter is preloaded to FF0FH, but it cannot begin counting until the trigger has been armed by the Prestore Valid FF, which ensures a minimum prestore. This allows the trigger to be observed even when it it occurs at the beginning of the display. In the case of Start-Trace, minimum prestore is 56 samples.

For Start-Trace, The CPU has previously programmed the Start/Center/End Selector (U3J) to select the terminal count of the least significant counter (U2L). For a preload of FF0FH, this terminal count will be true as soon as the delay counter begins counting. Tracepoint Latched will then occur immediately. Tracepoint will be stored in one of the next four positions after the prestore of 56 samples.

For poststore after a start-trace, the delay counter must now count from FF0FH to its terminal count, FFFFH, before the measurement is stopped. Poststore is then approximately four times the subtraction of FFFFH minus FF0FH.

When delay is desired, it is subtracted from the Start-Trace preload, FF0FH. For example, a delay of 60 sample clocks would require the delay counter to be loaded with FF0FH minus 15--since the counter counts at 1/4 the sample rate--or FF00H. The counter must then count 15 additional times to reach FFFFH and stop the measurement.

8-29. END-TRACE. Now the delay counter is preloaded to FFF0H, and the Start Center/End Selector selects the terminal count of the second counter (U1L). The Prestore Valid FF arms the trigger after approximately 956 samples have been stored. If a trigger has occurred, the delay counter is started and reaches terminal count after approximately 60 samples of poststore.

Any desired delay is subtracted from the End-Trace preload of FFF0H. For a delay of 960 sample clocks, for example, the counter preload would be FF00H. The counter must then count an additional 240 times (at 1/4 the sample rate) before it can stop the measurement.

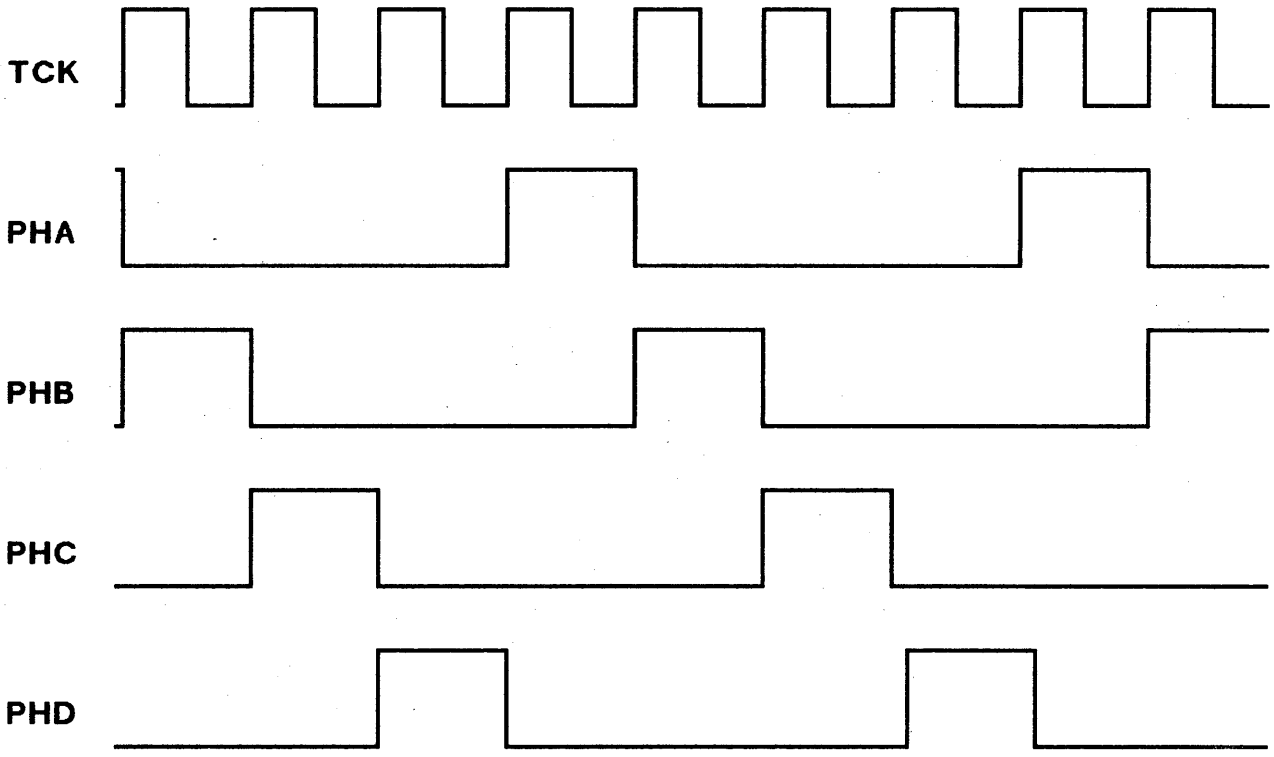


Figure 8D-8. Phase Waveforms--Timing Mode

8D-30. Clock Generation (see schematic 8D-3)

The Clock Generator consists primarily of a 200 MHz oscillator, dividers, and multiplexers which select sample rates for the timing analyzer.

The timing clock is selected by the CPU at the multiplexer (U8C). The multiplexer selects 10 MHz, 20 MHz, 40 MHz, 100 MHz, 200 MHz, or the CPU clock. The CPU clock is used fo Self-Test. The frequency selected by the multiplexer is further divided in the final flip-flop (U9D) and sent to the motherboard and other parts of the timing system.

The Start Synchronizers are two flip-flops (9C) making up a shift register which allows the clock to start cleanly.

8D-31. Phase Generation (see schematic 8D-4)

The phase generator uses the timing clock (TCK) to generate four phases which ensure the proper relationship between different parts of the timing analyzer.

Phase A drives the macrocells.

Phase B drives the address and index clocks, which clock the memory address counter and the poststore counter, respectively.

Phase C drives the macrocells. The trigger signal from the pattern duration filter is synchronized to Phase C.

Phase D drives the Write Enable Selector (U9H), which writes incoming data samples into RAM (via LWE1, LWE2). Also clocks the Memory Address Latches (U5K,5L), which store the current address of the Memory Address Counters when Tracepoint goes true.

8D-32. Hold/Encoder State Counter (see schematic 8D-4)

This counter performs a dual function.

8D-33. HOLD. At the beginning of a run, the counter counts to 16 before de-activating the HOLD line. As long as the HOLD line is active, no data is clocked into memory. This clears the macrocells of old data from past runs, so that only new data is stored.

8D-34. ENCODER. The two least significant counter bits track the macrocell encoders, which store four bytes at a time in memory. The latched trigger stops the counter. When the counter is stopped, the CPU reads the code, and uses this and the Memory Address Counter output to determine exactly where in memory the trigger is stored.

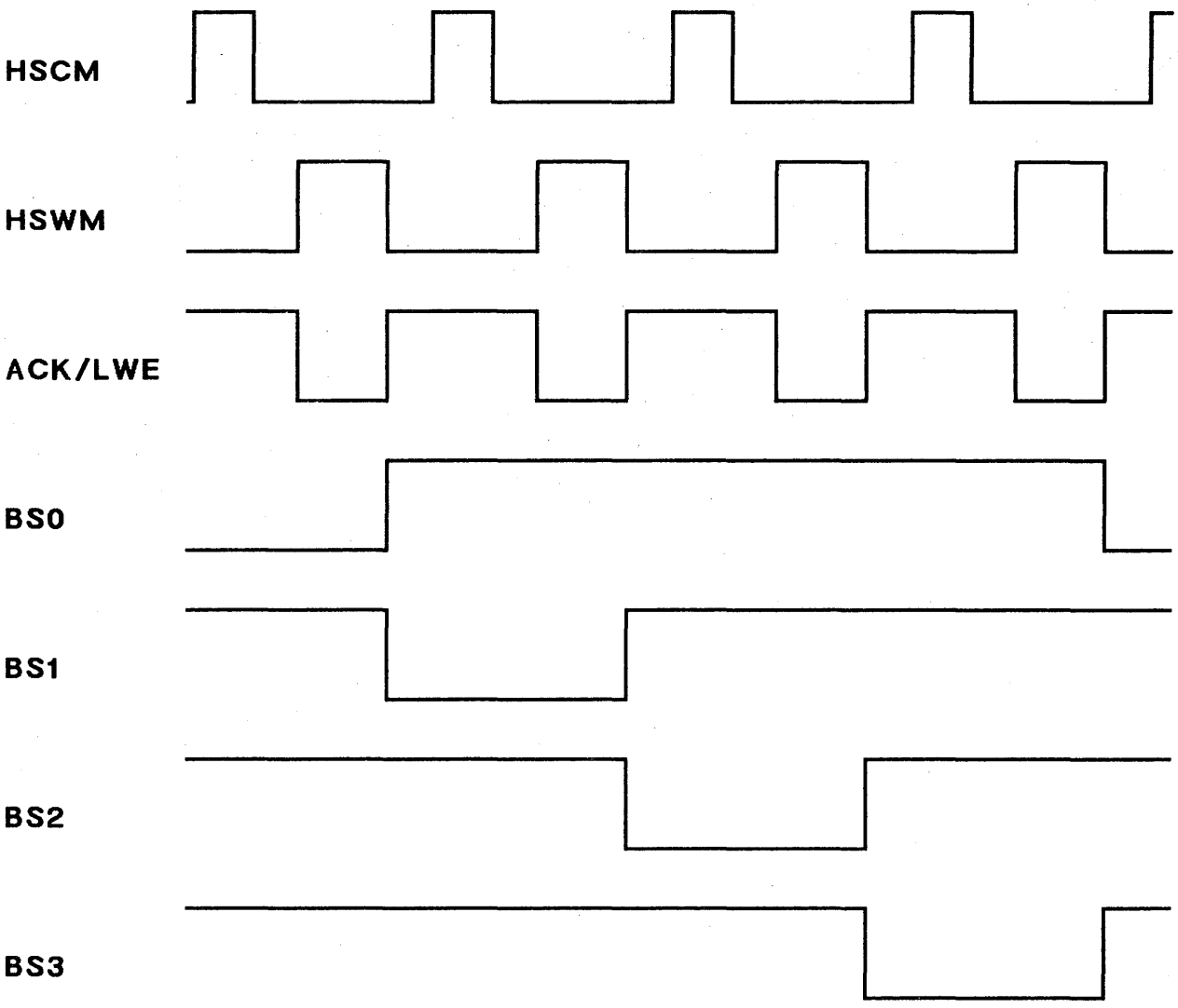


Figure 8D-9. Memory Write Waveforms--State Mode

8D-35. CPU Interface (see schematic 8D-5)

8D-36. READ SELECTORS (U3k-4K, U3L-4L). By multiplexing Status, Data, and Address bits, the Read Selectors allow the CPU to interrogate the timing analyzer. The CPU uses the address information to load all the timing acquisition memory data into its own RAM on the CPU board. The tracepoint address and the two encoder bits (ENC0, ENC1) tell the CPU where to find tracepoint in acquisition memory. HMEMFUL, another status bit, tells whether all the data in timing aquisition memory is valid, in case case of a partial run.

8D-37. MODE SELECT LATCH (U5C). The CPU programs some of the analyzer via the Mode Select Latch. By means of PS0 and PS1, it can select Start, Center, or End Trace. When HARMD is high, the Timing Analyzer can arm the State Analyzer; when it is low, State arms Timing. HBNCD sends the trigger from the output of the Pattern Duration Filter to the BNC connector. HSSEL determines whether the timing board is in the State or Timing mode. HGL selects Glitch Mode.

8D-38. WRITE STROBE DEMULTIPLEXER (U4D). The CPU writes to the timing analyzer, providing clocks and enable signals for different analyzer functions, by means of the Write Strobe Demultiplexer. The following is a list of clocks coming out of the demux:

LPE1,LPE2	Parallel enable signals for the Delay/Poststore Counter.
CPUCK	Timing clock from the CPU for PV purposes.
SCK	Allows the CPU to abort a run, to generate HRST, or to break the measurement complete loop for Self-Test.
LMACRST	Resets the Memory Address Counter.
PCK	Loads the Pattern Duration Selector.
SELCK	Programs the sample rate.
HRST	Master Reset for the timing analyzer.
LOADCK	Loads the index clock to the poststore counter.
READCK	Loads the address clock to the memory address counter.

8D-39. STATE MODE. The timing master board can be run in the state mode as a part of the state analyzer. In this case HSCM (State Clock Master) and HSWM (State Write Master) are supplied by the state board. Figure 8D-9 shows the relationship between the different memory write signals in the state mode. Unlike the timing mode, where all block selects are active at the same time for writing the 32-bit word, only one block select at a time is active in the state mode.

8C-40. MNEMONICS

The following signals, listed in alphabetical order, are used on the Timing Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing Master board are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8D-2. Mnemonics

Mnemonic	Description
A0-7	Address outputs from the memory address latches.
ACK	Memory Address counter clock. Increments the address counters.
CPUCK	CPU clock. Sample clock during Self-Test.
D0-7	Memory data outputs.
ENC0,1	Two-bit code pointing to the RAM where tracepoint is stored.
GS1	Ground sensing from the timing probe.
HA0-7	Motherboard address bus.
HABORT	Abort. Allows a user to stop a run.
HARMD	Arm drive. Timing arms State. When low, State arms Timing.
HBNCD	BNC drive. Enables pattern trigger to drive BNC output.
HD0-7	Motherboard data bus.
HGL	Glitch. Allows glitch detection and triggering on 4 channels.
LBRK	Break. Used in Self Test to break the Measurement Complete loop.
LAM LBM LCM LDM	State patterns from Timing Master to State.
HGM	Glitch trigger (master), from the macrocells.
HMACRD	Memory address counter read. Enables MAC read.
HMC	Measurement complete. Stops data sampling and storage.
HMSS	Macrocell State select. Puts macrocells in the State Mode--with HSSEL puts the Timing Master board in the state mode.
HOLD	Prevents data storage (MAC counting) until 16 sample clocks pass.

Table 8D-2. Mnemonics (Cont'd)

Mnemonic	Description
HPHA-D	Four timing clock phases for different analyzer funtions.
HPVD	Prestore valid. Enables trigger to occur after minimum prestore.
HR/LW	High read/low write. The CPU either programs or reads analyzer.
HRST	Reset. Master reset derived from the CPU.
HSCM	State clock (master). State sample clock to the macrocells.
HSSEL	State select. With HMSS puts Timing in the State Mode.
HTPL	Tracepoint latched. Trigger + Delay Latched.
HTRIG	Latched trigger. From the ANDed glitch and pattern triggers.
HTSEL	Timing select. Selects Timing block select mode (all true).
ICK	Index clock. Increments the delay/poststore counter and the run- status latches.
LARM	ARM. Allows the valid timing pattern from the macrocells to pass on to the pattern duration filter.
SELCK	Select clock. Allows the CPU to select the sample rate.
TCK1-3	Timing sample clock.
THR1	Threshold to timing probe.
LE2	Macrocell programming enable.
LMACRST	Memory address counter reset derived from the CPU.
LMCI	Measurement complete interrupt to the CPU.
LMF	Memory full (at least once) from the Wrap-around FF.
LOADCK	Load Clock. The CPU loads the delay/poststore counter.
LPE1,2	Poststore enables. Enable delay/poststore counter for loading.
LSTB	CPU strobe to read or write to the analyzer.
LTM	Valid timing pattern (master), from the macrocells.
LWE1,2	Write enables to acquisition RAM, from timing clock (phase D).

Table 8D-2. Mnemonics (Cont'd)

Mnemonic	Description
MA0-7	Memory address counter outputs.
MA7	Memory address counter output indicating count 128 to the Start/Center/End Selector.
MACTC1	Memory address counter terminal count (15) from first counter to the Start/Center/End Selector.
MACTC2	Memory address counter terminal count (255) from second counter to the Start/Center/End Selector.
PCK	Pattern clock. Clocks the pattern duration selector.
PS0,1	Selects poststore decoded states for Start/Center/End.
READCK	Read clock. Increments the memory address counter each time the CPU reads memory.
SCK	Stop clock. Allows the CPU to abort or break operation.

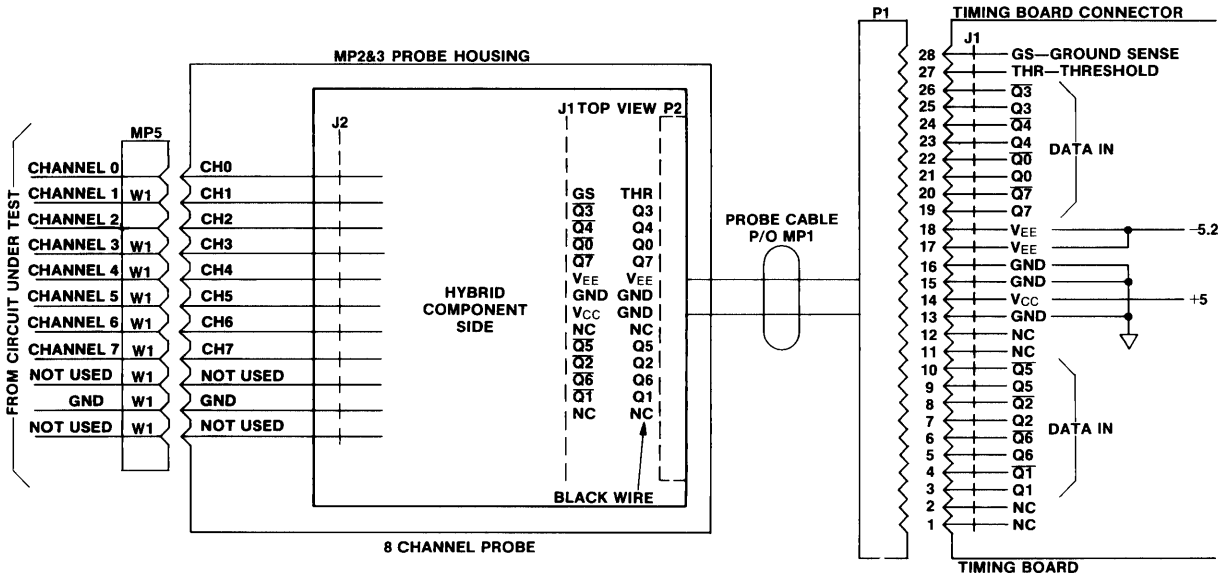


Figure 8D-10. Timing Pod

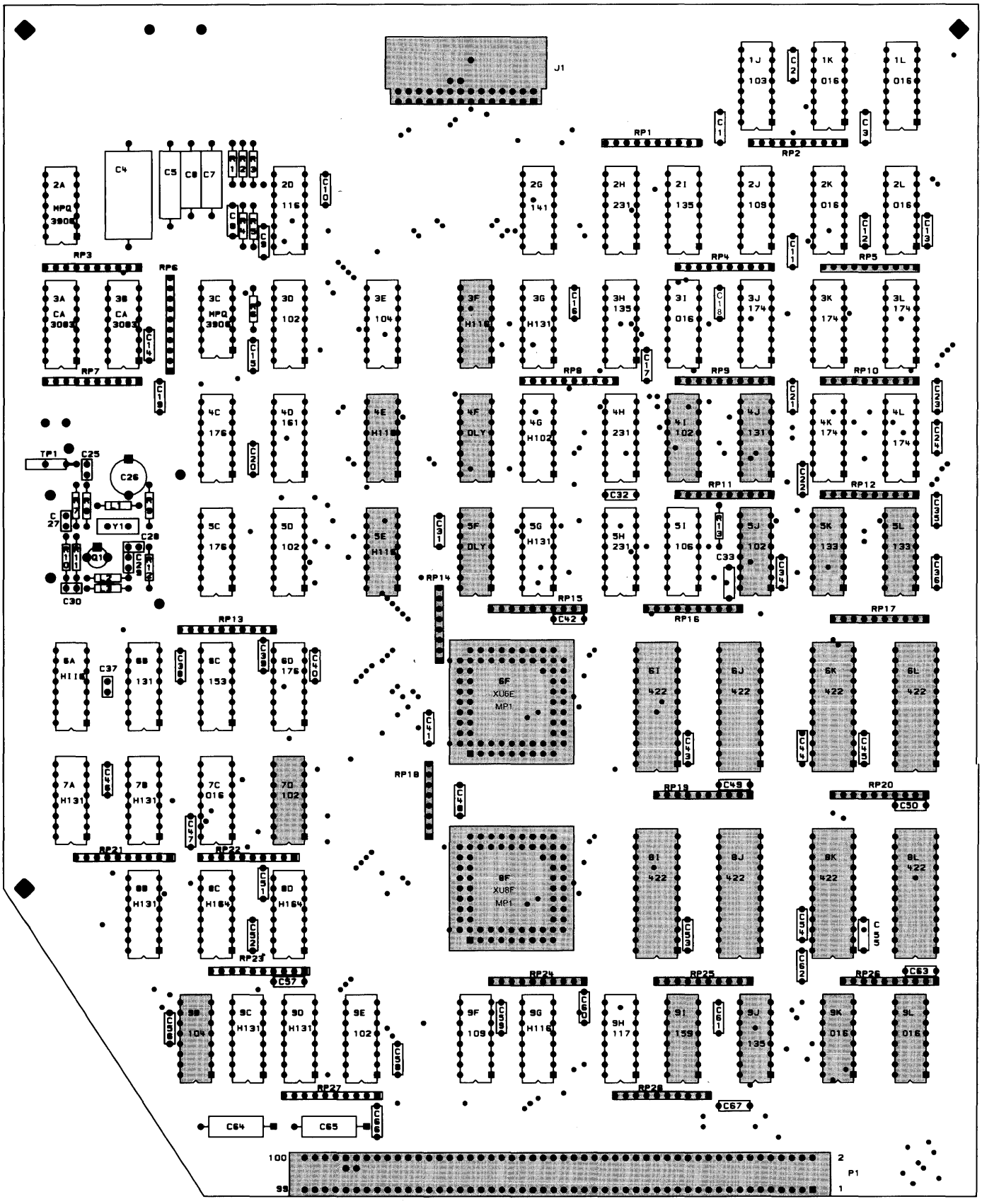
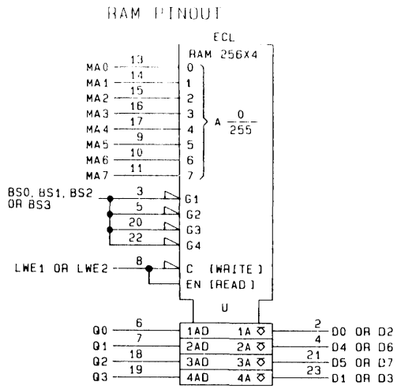
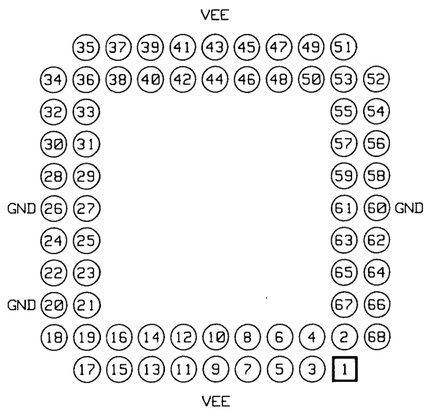


Figure 8D-11. Timing Master Component Locator

NOTE I



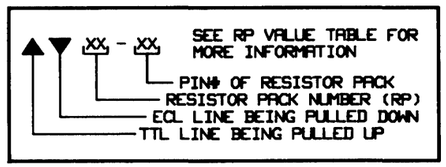


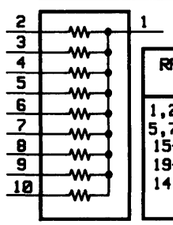
Macrocell Pin-out Diagram

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U3F,4E,4I,4J, 5E,5J-L,7D,9B, 9J-L
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 24 12	U6I-6L,8I-8L
Vcc(gnd) Vee(-5.2)	16 8	U9I
-5.2 GND	9,43 20,26,60	U6F,8F

RESISTOR PACK DESCRIPTIONS:

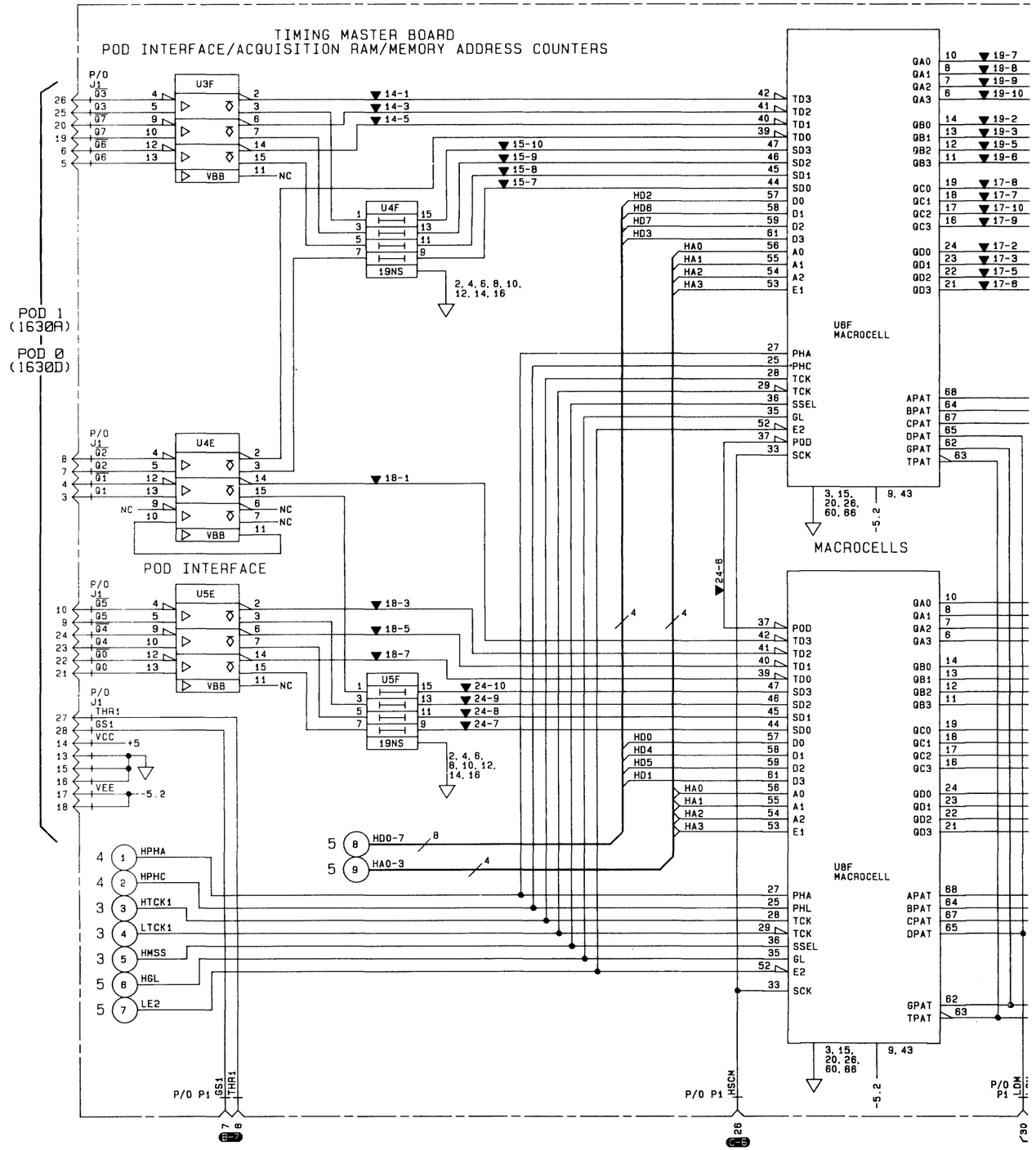




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2,4, 5,7-13 15-17, 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

U3F,4E,F,4I,4J,5E, 5J-L,6F,6I-L,7D, 8F,8I-L,9B,I-L J1 P1 RP5,9-12,14-20, 24-26,28	



MEMORY ADDRESS LATCHES

ACQUISITION RAM (SEE NOTE 1)

RAM BLOCK SELECT

MEMORY ADDRESS COUNTER

MEMORY FULL FF

PRESTORE VALID FF

PATTERNS TO STATE BOARD

Figure 8D-12. Timin

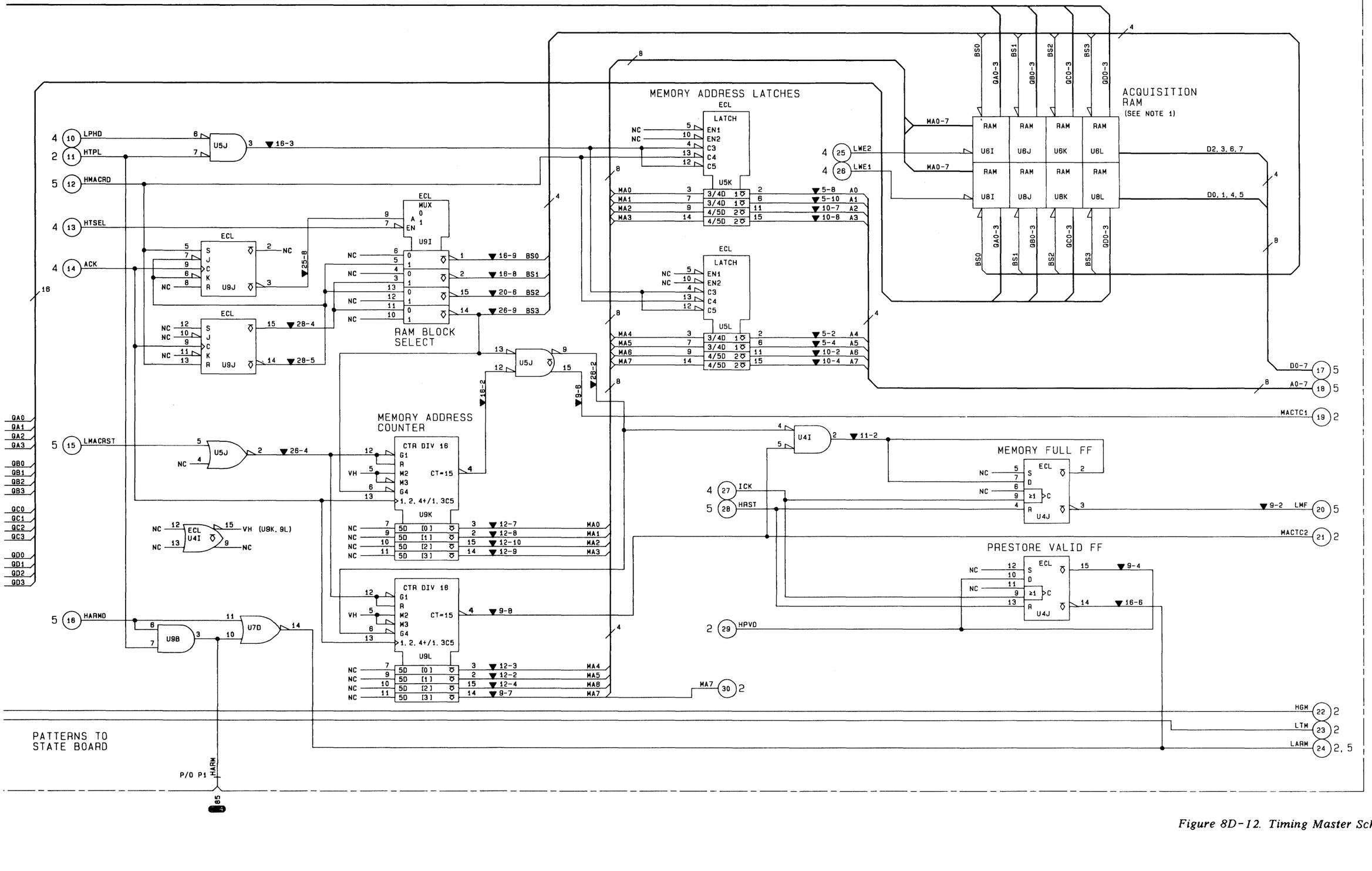


Figure 8D-12. Timing Master Schematic (1 of 5)

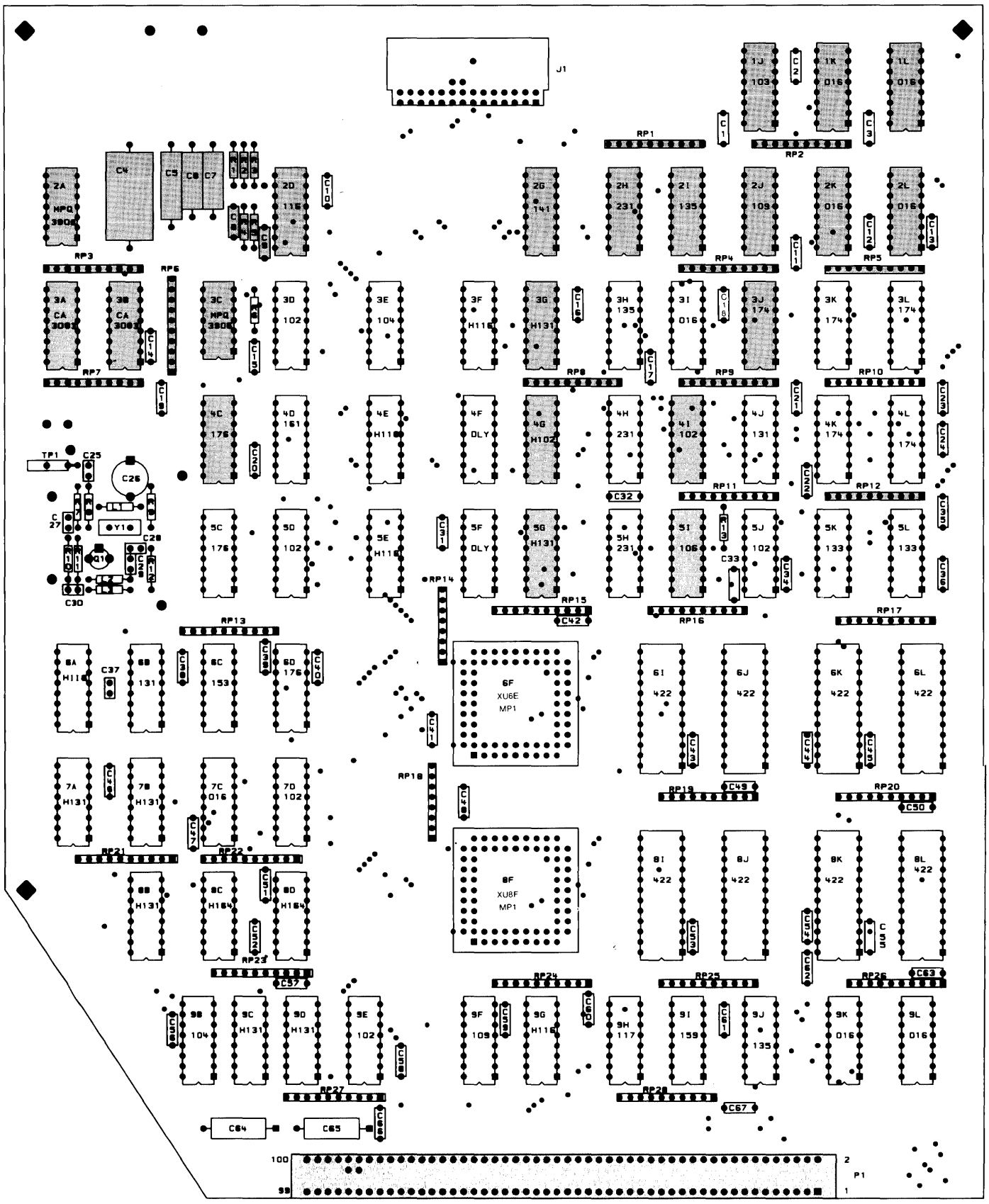
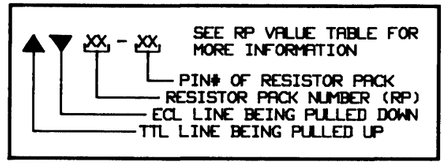


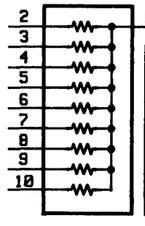
Figure 8D-11. Timing Master Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1J-L,2G-L, 3G,3J,4C,4G, 4I,5G,5I

RESISTOR PACK DESCRIPTIONS:

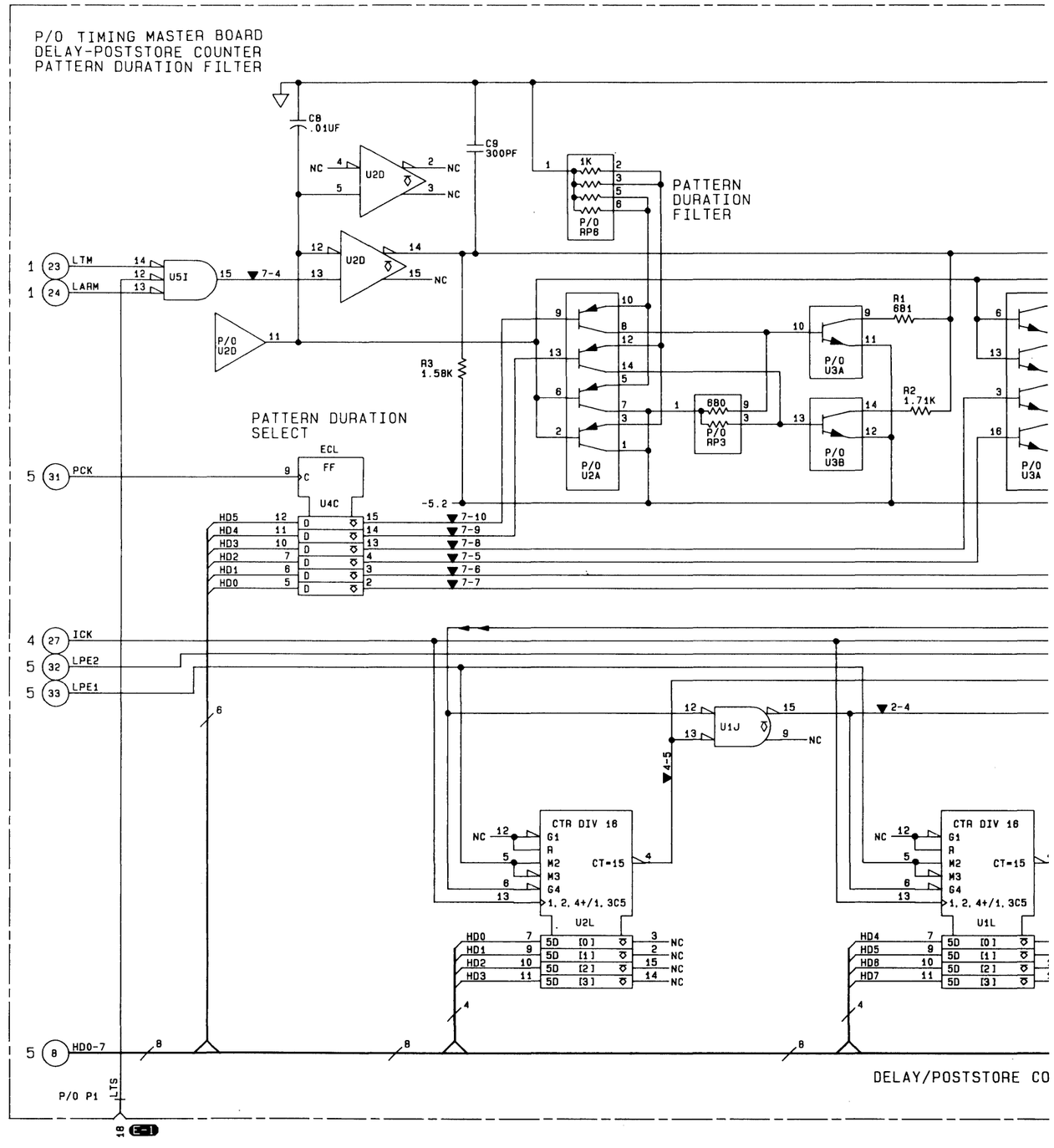




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

U1J-L,2A,2D,2G-L, U3A-C,3G,3J,4C, 4G,4I,5G,5I C4-9 P1 R1-5 RP1-9,12,23	



GLITCH FF

TRIGGER FF

PATTERN LATCH

PATTERN TRIGGER DELAY SHIFT REGISTER

SYNC TRIGGER FF

MEASUREMENT COMPLETE FF

TRACE POINT

START/CENTER/END SELECTOR

LAY/POSTSTORE COUNTER

P/O P1 HGS

Figure 8D-12. Timin

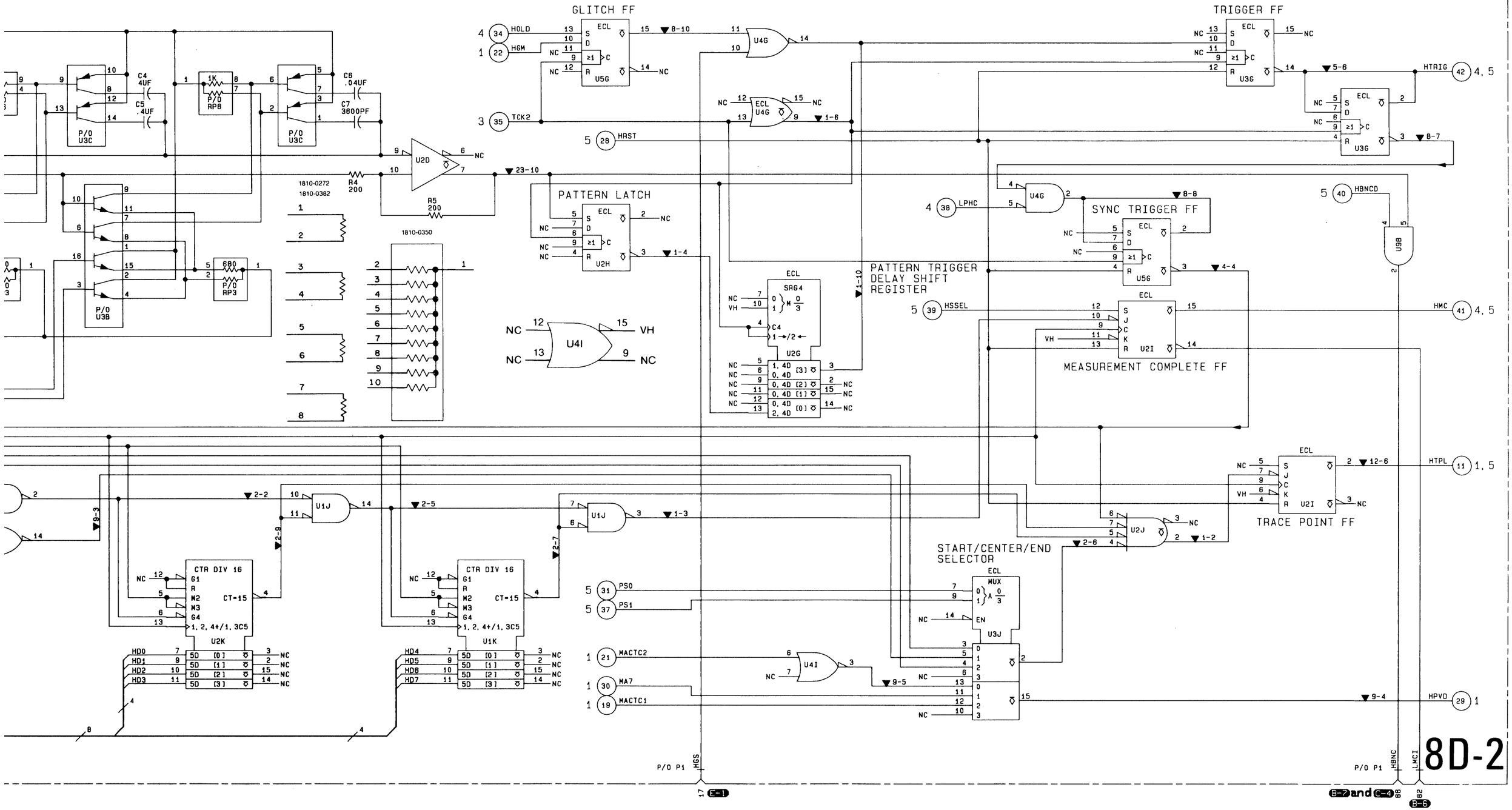


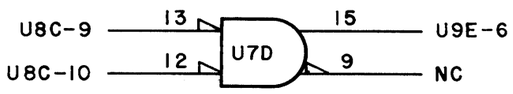
Figure 8D-12. Timing Master Schematic (2 of 5)

Figure 8D-11. Timing Master Component Locator

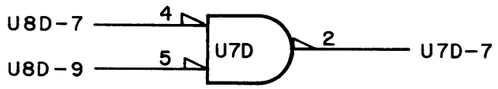
NOTES 1 & 2

ON TIMING MASTER BOARD 01630-66506, GATES U7D A and U7D D ARE SWAPPED. THESE ARE THE CIRCUITS ON THAT BOARD:

NOTE 1:

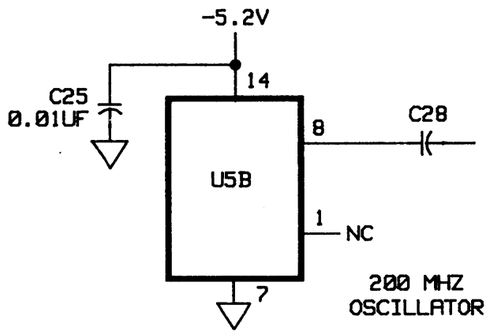


NOTE 2:



NOTE 3

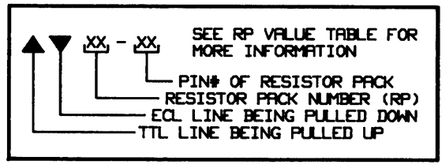
OSCILLATOR CIRCUIT FOR TIMING MASTER BOARD 01630-66524.

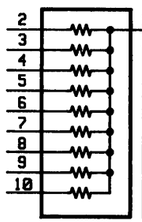


IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U6A-6D,7A-7D, 8B-8D,9C-9E,9G

RESISTOR PACK DESCRIPTIONS:

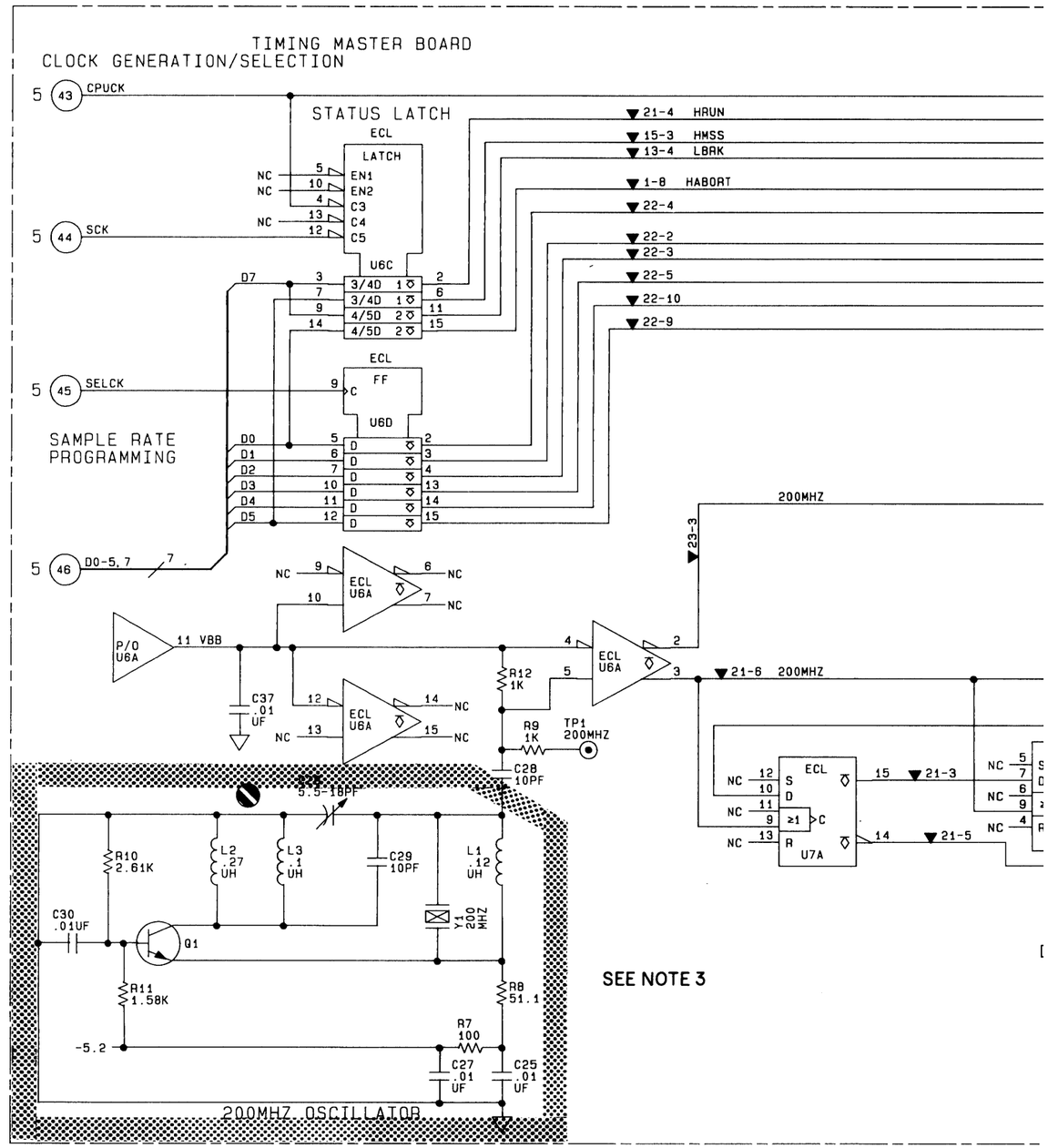




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

U6A-6D,7A-7D, U8B-8D,9C-9E,9G C25-30,37 L1-3 P1 R7-12 TP1 Q1	Y1 RP1,4,8,13,15, 21-23,27



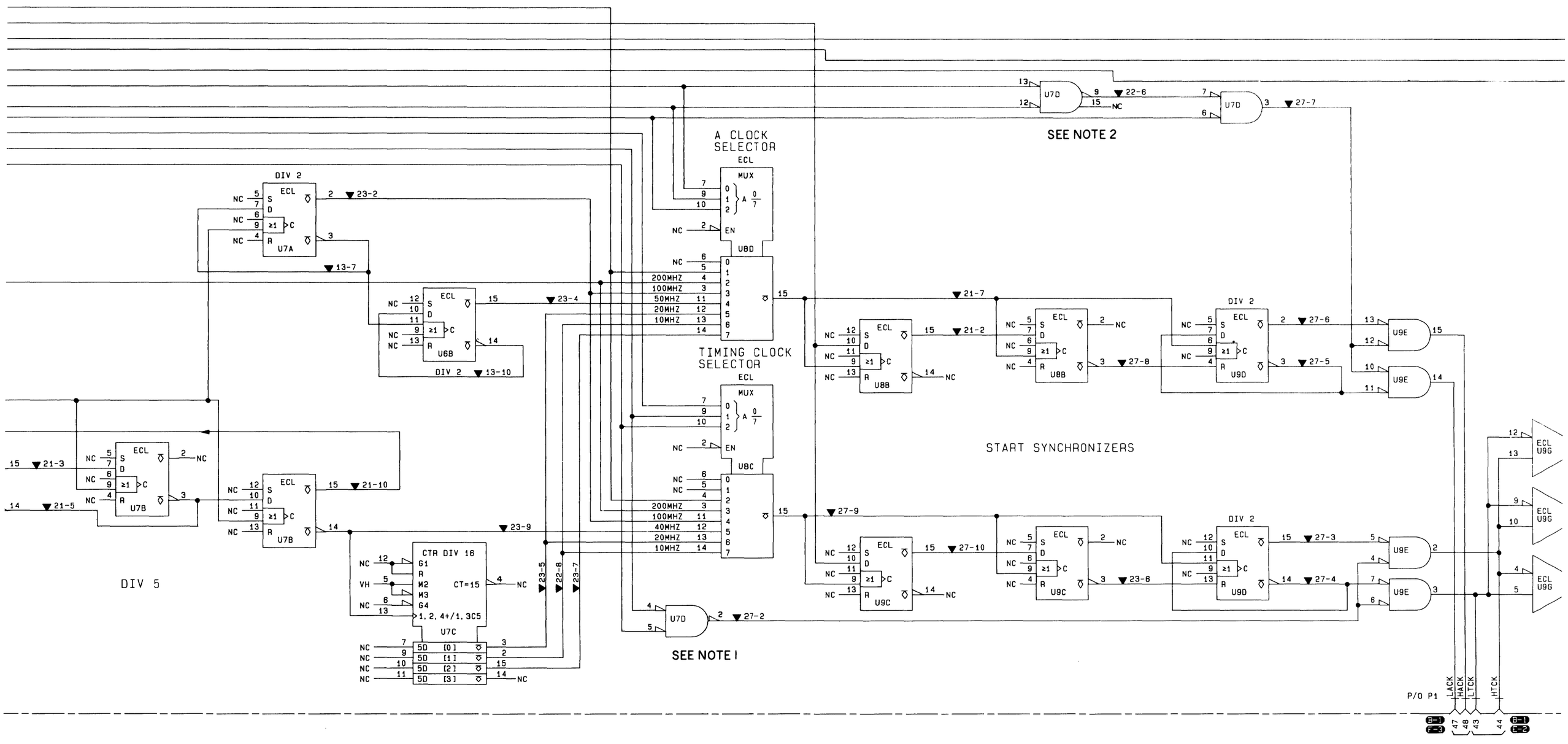


Figure 8D-12. Timi

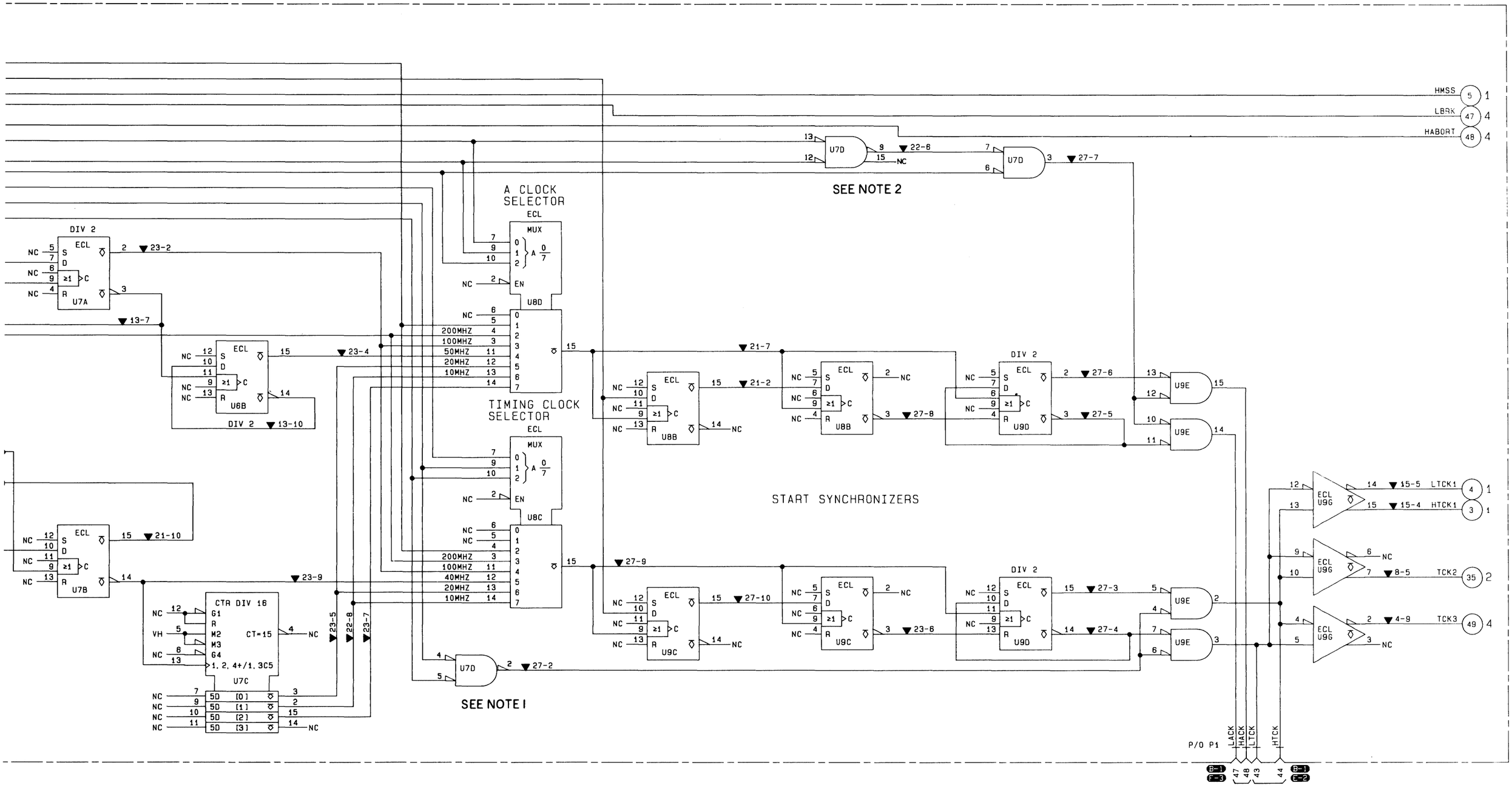


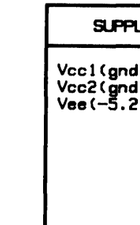
Figure 8D-12. Timing Master Schematic (3 of 5)

Figure 8D-11. Timing Master Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2H,3E,3H,3I, 4H,5H,5I,5J, 9H

RESISTOR PACK DESCRIPTIONS:

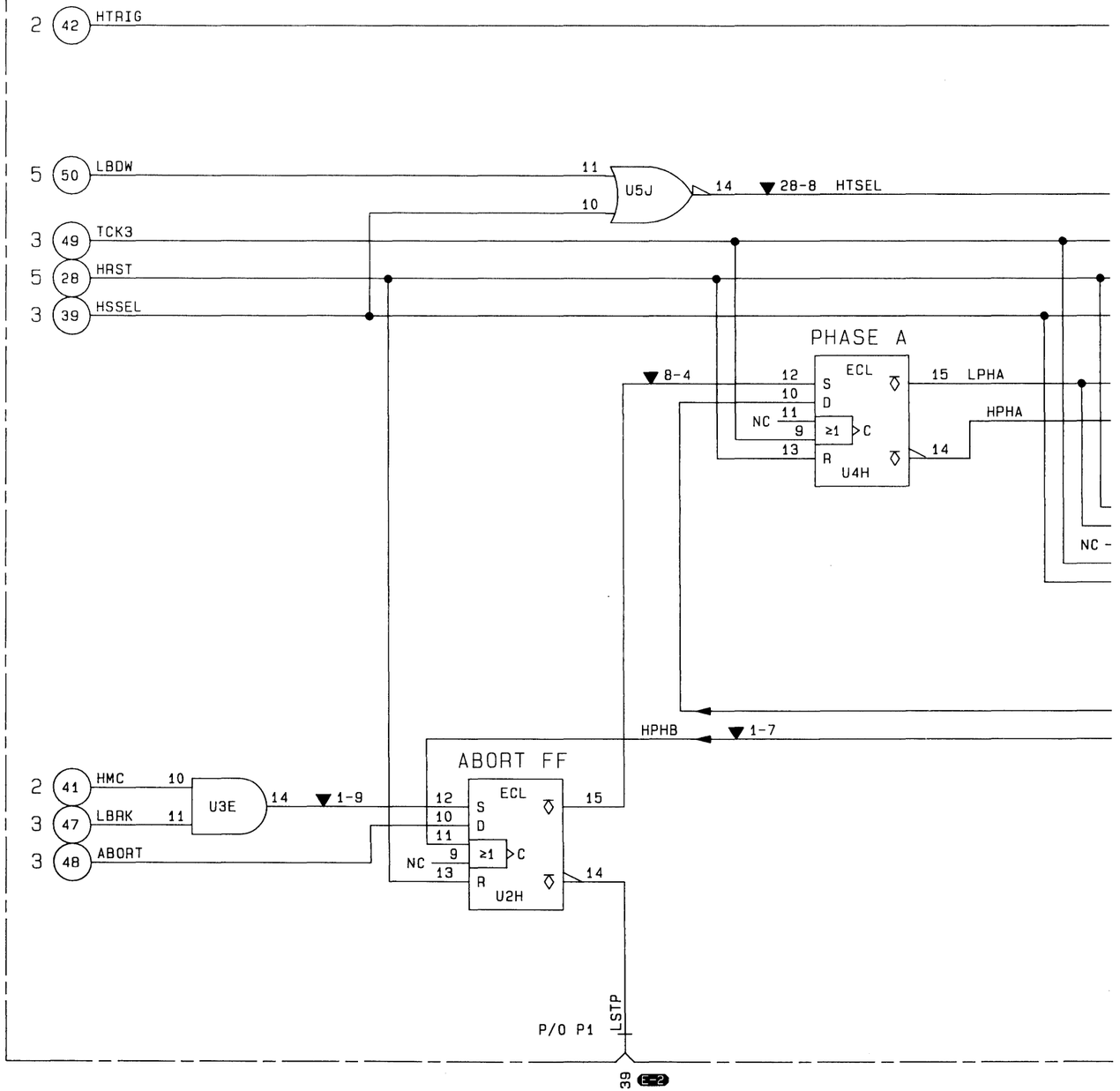


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

U2H,3E,3H,3I,4H, U5H-J,9H C64,65,37 P1 RP1,2,4,7-11,16, 17,24,26,28	

P/O TIMING MASTER BOARD
PHASE GENERATION



HOLD/ENCODER STATE COUNTER

CTR DIV 16
U3I
1, 2, 4+/1, 3C5
CT=15
▼8-2
▼4-8
▼10-9
NC
HTSEL
TCK3
HRST
HSSEL

ECL
HOLD FF
S
J
C
K
R
U3H
▼11-9

LPHA ▼9-9
HPHA ▼24-4

PHASE B
ECL
U4H
▼11-8

PHASE C
ECL
U5H
LPHC
HPHC
▼8-6
▼24-3

PHASE GENERATION

ECL
U5H
▼11-3
▼28-7
LPHD
HPHD
HSSEL

PHASE D

WRITE ENABLE SELECT
U9H
▼26-3

OR PHD STATE
U9H
▼17-4
▼7-3
U3E
▼16-5
U5I
READ-CK
LOAD-CK
LPHB
HSWM
22 C-7

Figure 8D-12. Timi

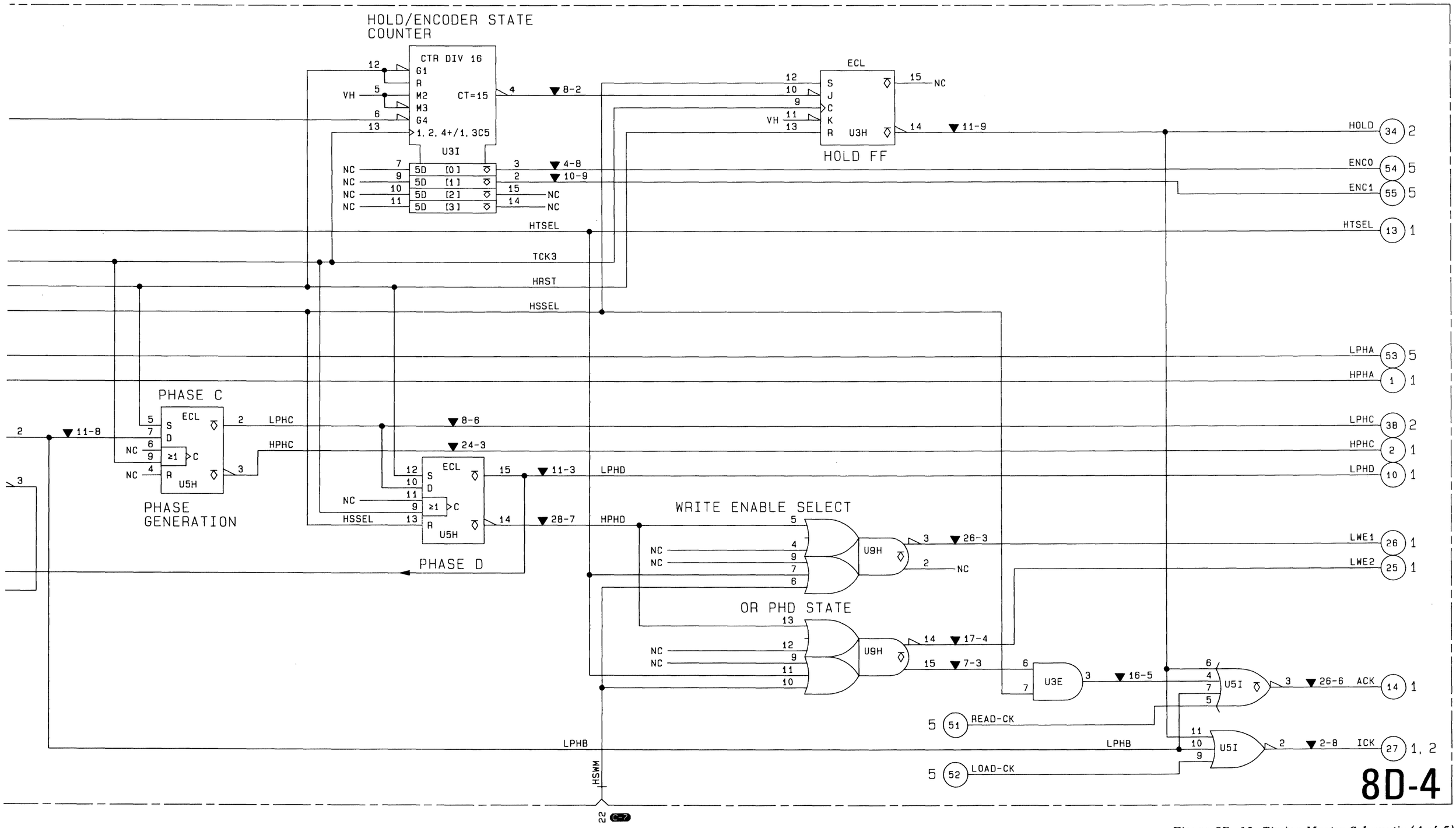


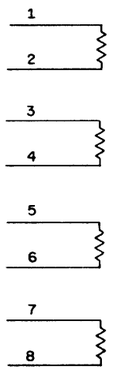
Figure 8D-12. Timing Master Schematic (4 of 5)

Figure 8D-11. Timing Master Component Locator

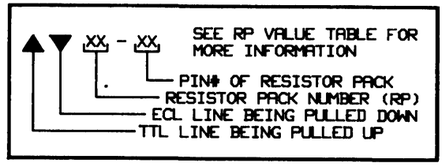
IC DEVICE POWER CONNECTIONS

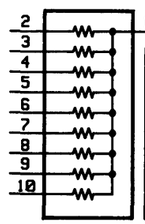
SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2J,3D,3K,3L, 4D,4I,4K,4L, 5C,5D,9F

NOTE I



RESISTOR PACK DESCRIPTIONS:

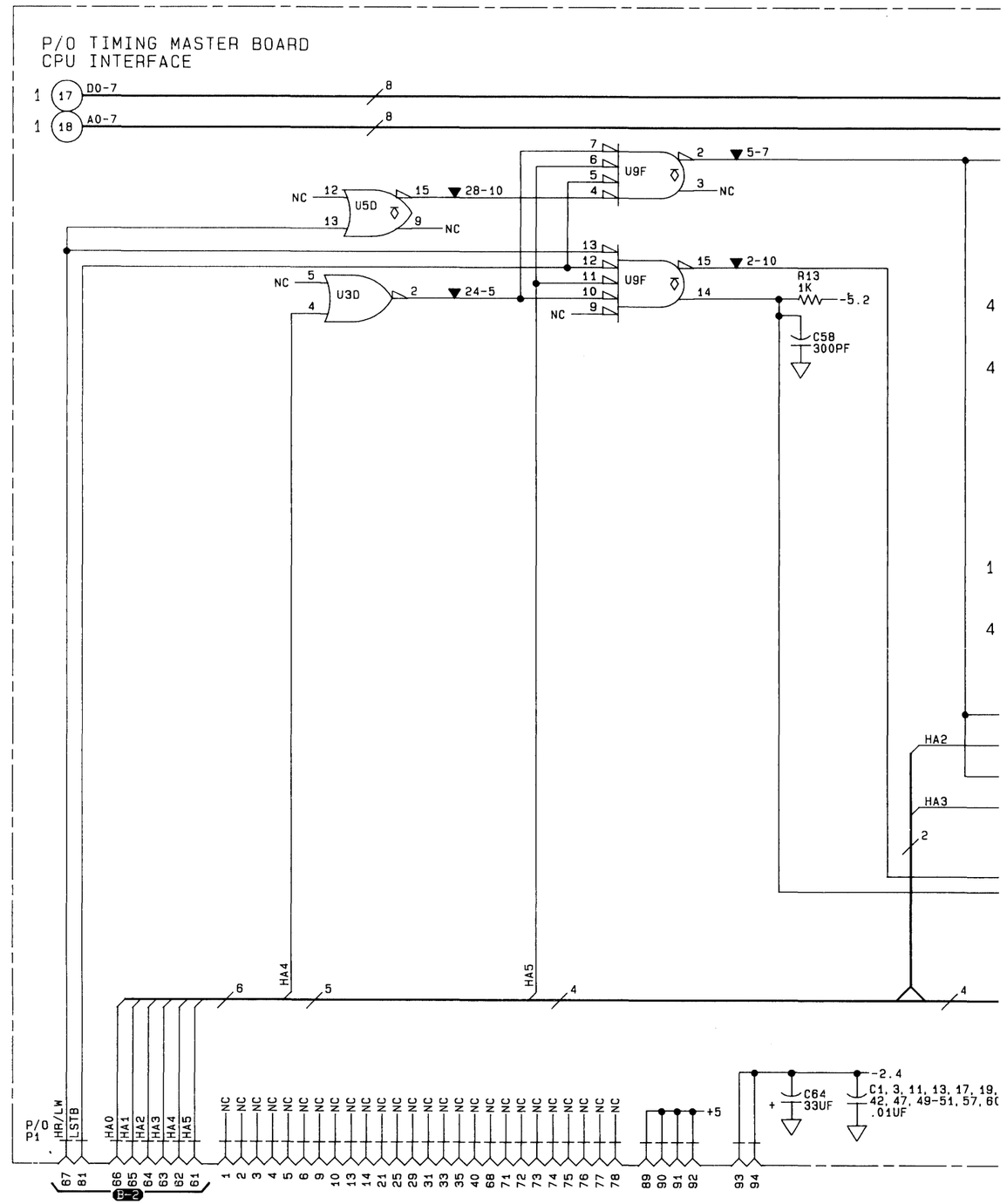




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

U2J,3D,3K,3L,4D, U4I,4K,4L,5C C1-3,8,10-24,31-36, 38-63,66,67 P1 R6,13 RP2,4,5,7,10,11, 13,22,24,26,28	



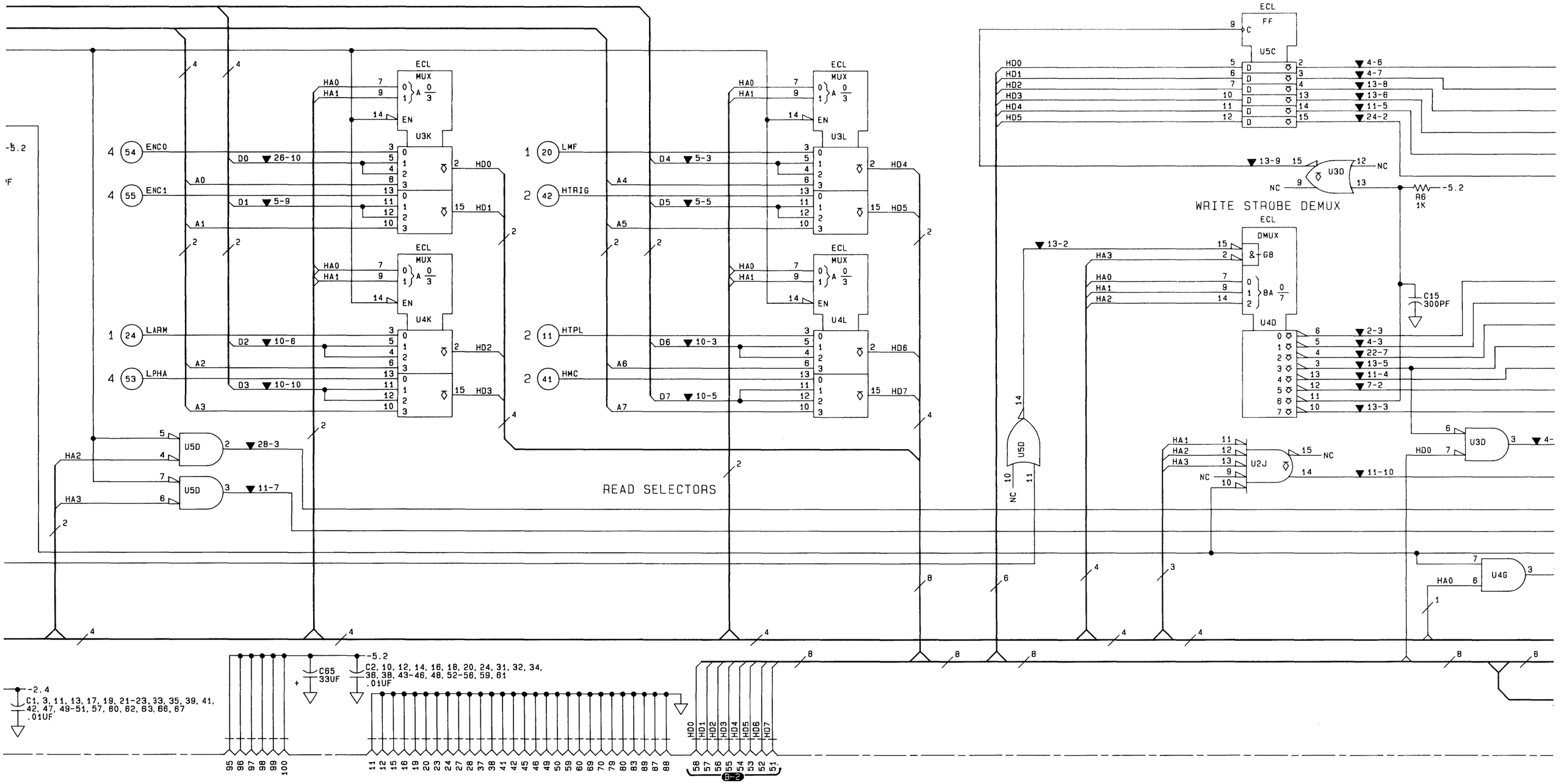


Figure 8D-12. Timin

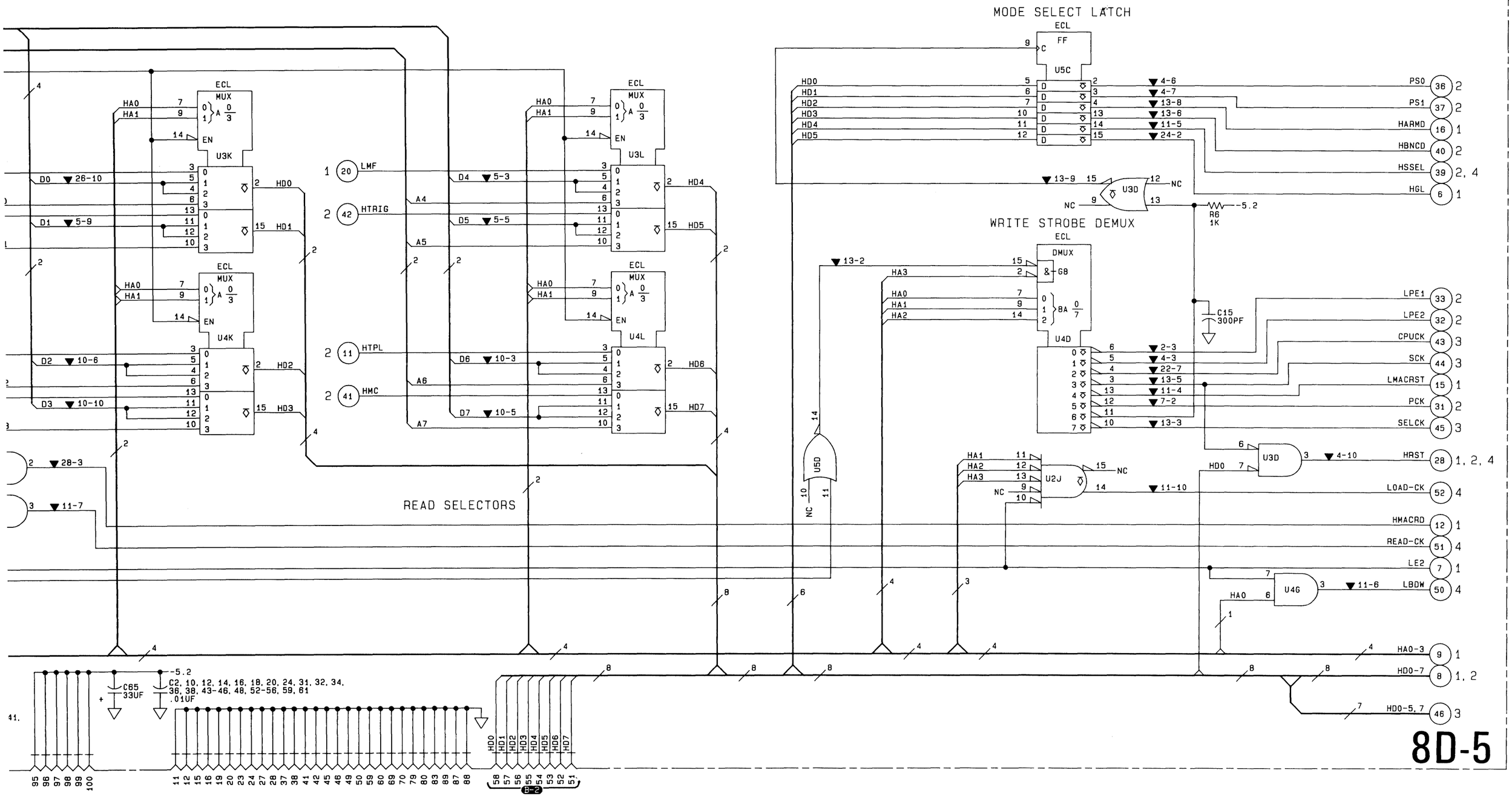


Figure 8D-12. Timing Master Schematic (5 of 5)

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NOTES

SERVICE GROUP 8E
TIMING SLAVE

8E-1. INTRODUCTION

8E-2. GENERAL. The optional Timing Slave board is similar to the Timing Master board in that it contains two macrocells, 1K x 8 RAM, a memory address counter, and clock phasing circuitry. Unlike the master board it does not contain a clock generator, and must receive its clock from either the Timing Master or State Master.

The valid timing or glitch pattern signals from the slave macrocells go to the Timing Master, where they are ANDed with timing and glitch pattern signals from the master macrocells. In the State Mode, the pattern signals from the timing boards are ANDed on the state board with the state pattern signals.

Table 8E-1. Timing Master and Slave Board Comparisons

TIMING MASTER BOARD	TIMING SLAVE BOARD
Pod Interface (8-bit)	Pod Interface (8-bit)
Macrocells (2)	Macrocells (2)
Acquisition RAM (1K x 8)	Acquisition RAM (1K x 8)
Pattern Duration Filter	
Delay/Poststore Counter	
Clock Generation	
Clock Selection	
Clock Phasing	Clock Phasing

8E-3. STATE MODE. With the optional slave board and its pod, timing width is increased to 16 channels. The timing slave board may also be used with the master timing board in the State Mode as an extension to the state analyzer, effectively increasing the width of state analysis to 43 bits.

When the 35-bit State/8-bit Timing combination is chosen in the format specification, only the timing slave board can be used with the state board for 35-bit state analysis. This is because only the timing master board has the pattern duration and clock circuitry needed for timing analysis.

In the State Mode the macrocells perform the same function as pattern recognition circuitry on the state board: both the master and slave board send a pattern bit for each of the four possible patterns that can be specified in state analysis. The two bits from master and slave for each pattern are ANDed on the state board.

8E-4. MEMORY ADDRESS COUNTER. The slave board's memory address counter is the same as that on the timing master board: An 8-bit counter selects one of 256 8-bit locations in a block of RAM; and a Block Selector chooses one of four 256-blocks.

8E-5. GLITCH MODE. As with master timing, glitches may be specified for detection or triggering on four of the eight timing slave board channels.

8E-6. CLOCK PHASING. A ring counter driven by the master timing board clock generates the four phases needed to synchronize the different functions on the board. For example, write-enable pulses for the memory are synchronized to phase "D" of the generator when the timing analyzer is in the timing mode. When the timing analyzer is being run as an adjunct of the state analyzer, the write-enable pulses are synchronized to a state control signal. The memory address clock is derived from Phase B. Phases A and C are sent to the macrocells.

8E-7. MNEMONICS.

The following signals, listed in alphabetical order, are used on the State Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing and State boards are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8E-2. Mnemonics

Mnemonic	Description
ACK	Address Clock. Increments memory address counter.
BS0-3	Block Select. Selects a block of RAM for reads or writes.
GS1	Ground Sense. Reference ground from user system.
HA0-5	Motherboard address bus.
HBRS	Break Reset. Sets BS0 high and other Block Selects low.
HD0-7	Motherboard data bus.
HGL	Glitch. Sets the glitch mode on four slave channels.
HGS	Glitch Slave. Glitch trigger from slave board to master.
HMSS	Macrocell State Select. Selects the State mode for slave.
HOLD	Prevents data storage (MAC counting) until after 16 clocks.
HPHA-D	Four timing clock phases for different analyzer functions.
HR/LW	High read/low write. The CPU programs or reads status.
HRST	Reset. Resets the memory address counter.
HSCS	State Clock Slave. State clock to macrocells in State Mode.
HSWS	State Write Slave. State write enable to RAM in State Mode.
HTSEL	Timing Select. Enables the block selector.
LAS LBS LCS LDS	Patterns from the macrocells when in the State Mode.
LE2	Enable line to the macrocells.
LSTB	Strobe. CPU strobe for reading and writing to timing slave.

Table 8E-2. Mnemonics (Cont'd)

Mnemonic	Description
LTS	Valid Timing Pattern. From slave macrocells to master board.
LWE1-2	Write Enable. Write enables to acquisition RAM.
MA0-7	Memory Address. Memory Address Counter lines to RAM.
LTCK, HTCK	Timing Clock. From motherboard.
TCK1 TCK2 TCK3	Timing Clocks derived from LTCK and HTCK.
THR1	Threshold to the pod from the CPU board

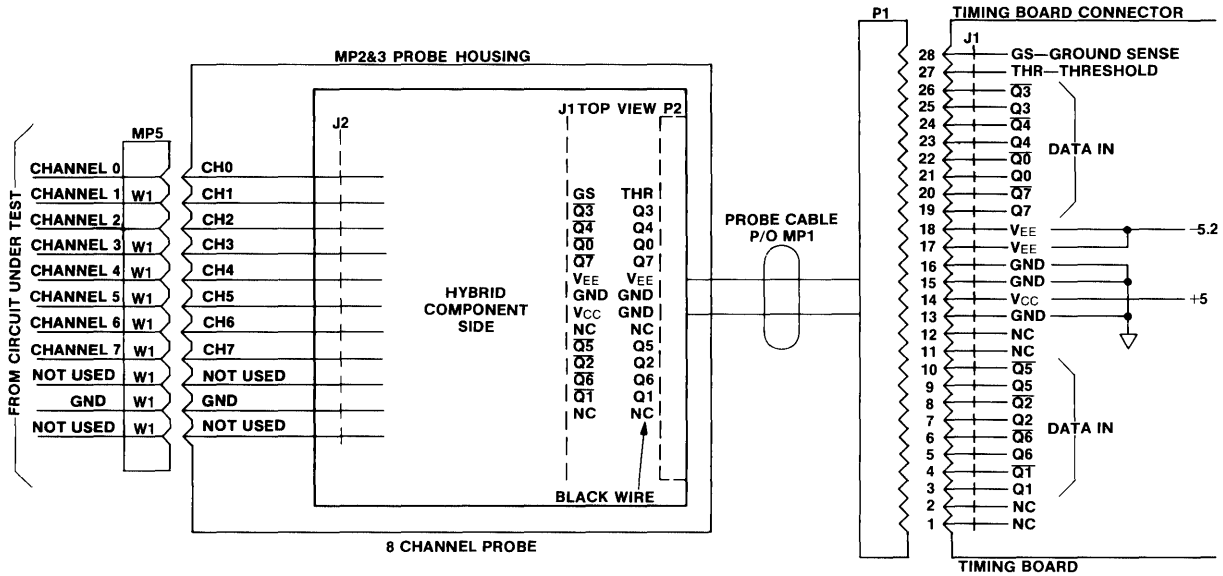


Figure 8E-1. Timing Pod

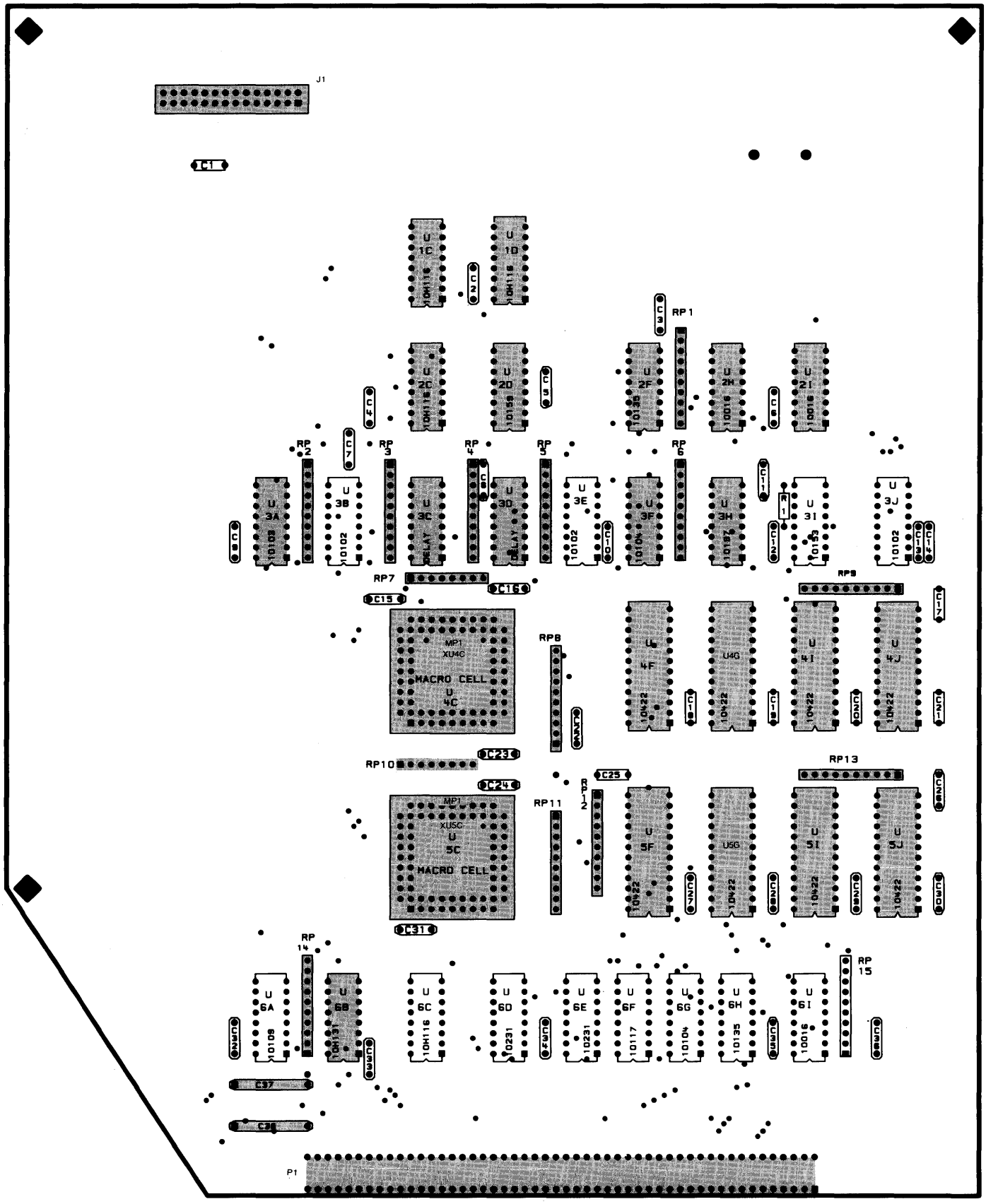
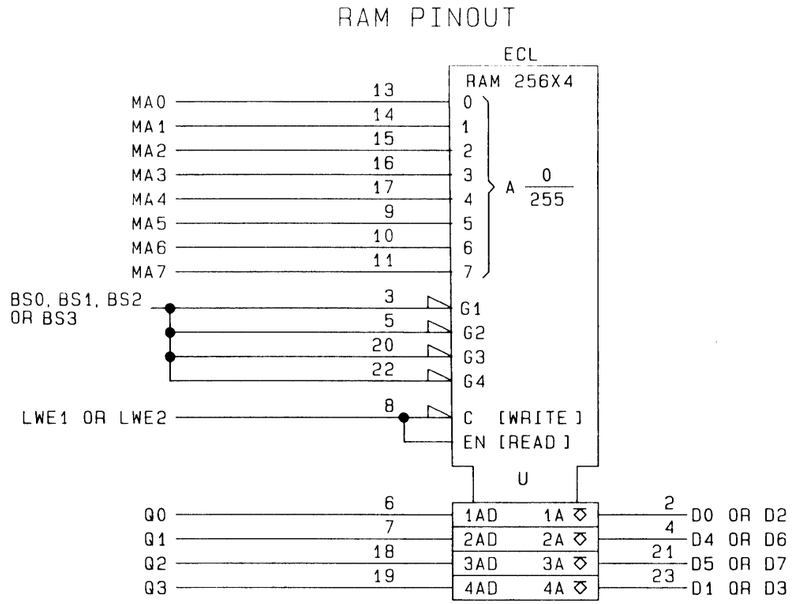
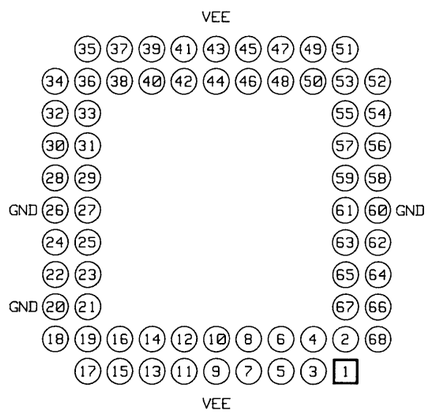


Figure 8E-2. Timing Slave Component Locator

NOTE I



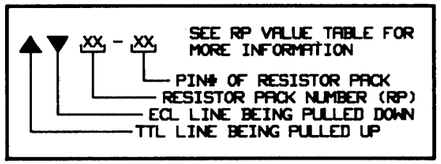


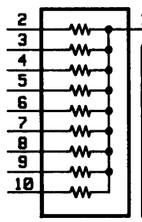
Macrocell Pin-out Diagram.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1C,D,2C,F,H, U2I,3A,F,H,6B
Vcc(gnd) Vee(-5.2)	16 8	U2D
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 24 12	U4F,G,I,J, U5F,G,I,J
-5.2 GND	9,43 20,26,60	U4C,5C

RESISTOR PACK DESCRIPTIONS:

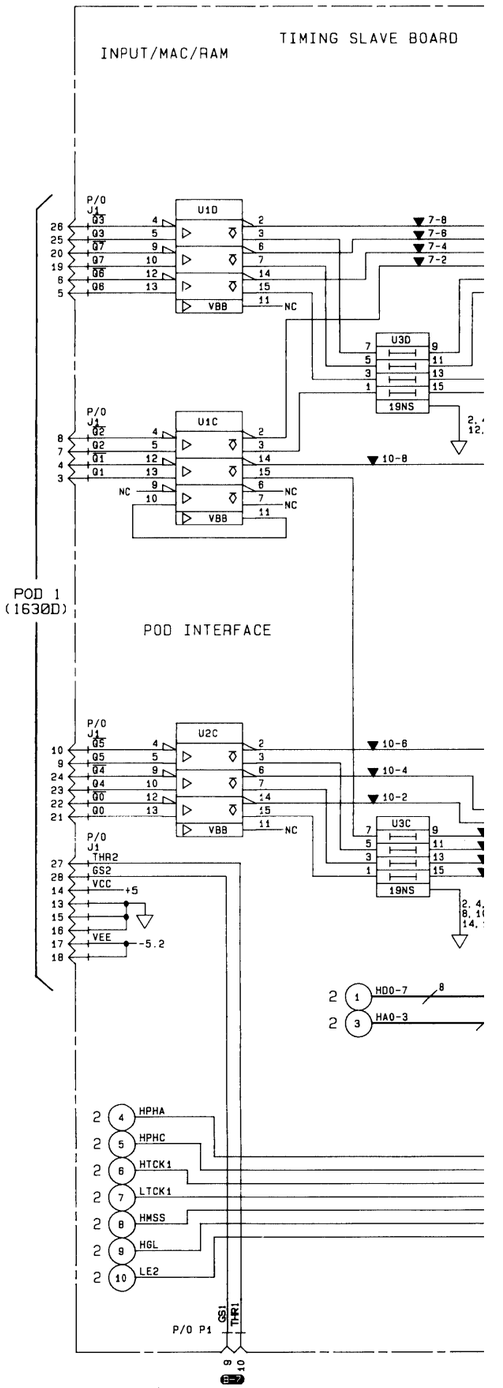




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 8,9 11-15 7,10	100 X 9 100 X 4	1 2,4,6,8	-2.4 -2.4

PARTS ON THIS SCHEMATIC

U1C,D,2C,D,F,H,I U3A,C,D,F,H,4C,F,G, U4I,J,5C,F,G,I,J U6B C1-12,14-38 J1 RP1-14	



TIMING SLAVE BOARD

MEMORY ADDRESS COUNTERS

BLOCK SELECT

DATA STORAGE RAM (SEE NOTE 1)

CPU INTERF

MACROCELLS

GLITCH FF

U4C MACROCELL

U5C MACROCELL

U2D

U2H

U2I

U3A

U3E

U3C

U3D

U2F

U6B

CTR DIV 16

MUX

RAM U4F U4H U4I U4J U5F U5H U5I U5J

U3F U3H

C37, 33UF

C38 33UF

C3, 7, 8, 11, 16, 17, 22, 23, 25, 28, 33, 36, 37 .01UF

C2, 4-6, 9, 10, 12, 14, 15, 18-21, 24, 27-32, 34, 35 .01UF

U2I PIN 5
U2H PIN 5
U6H PIN 6
U6I PIN 5
U6G PIN 13

Figure 8E-4. Tim

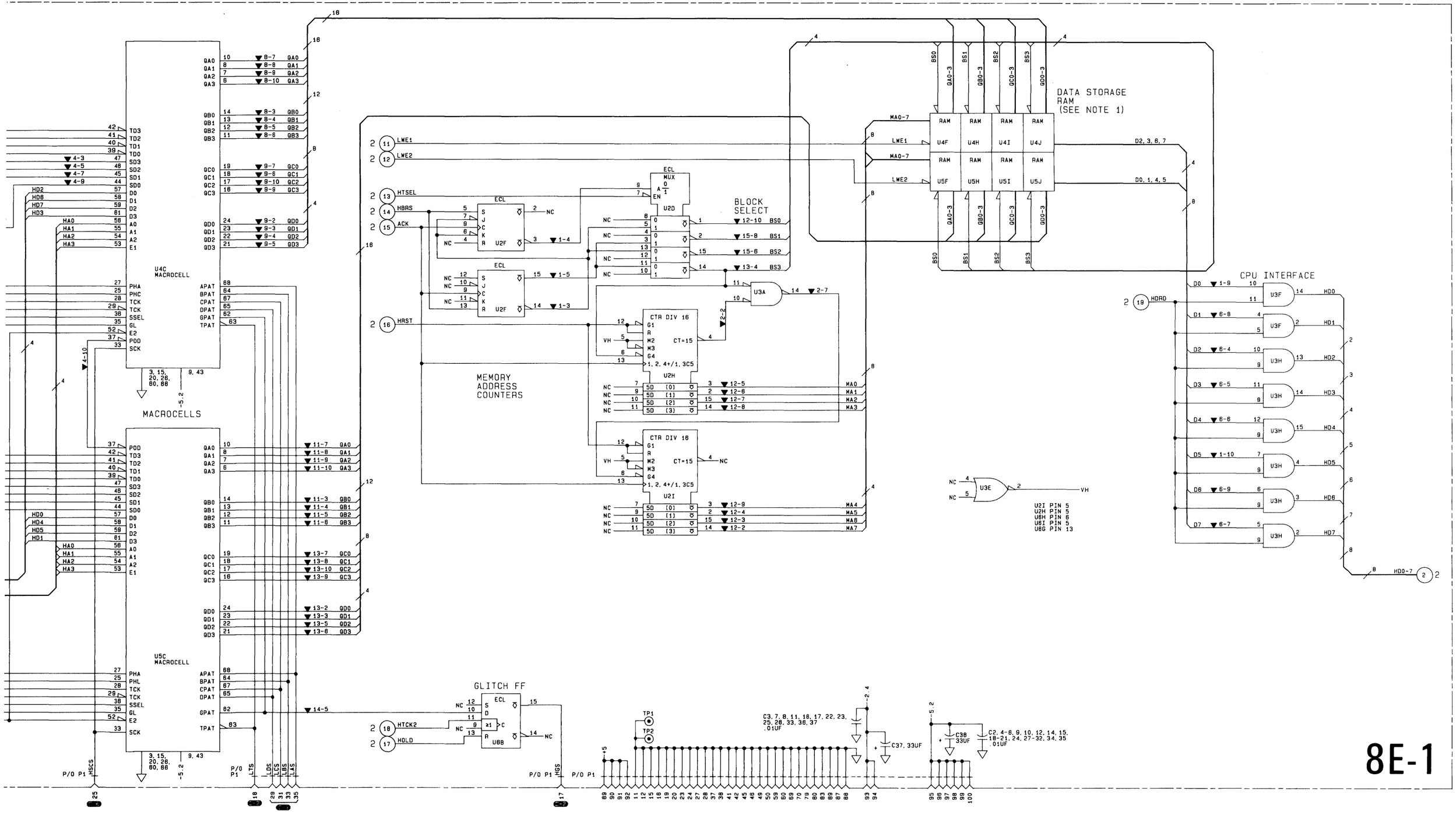


Figure 8E-4. Timing Slave Schematic (1 of 2)

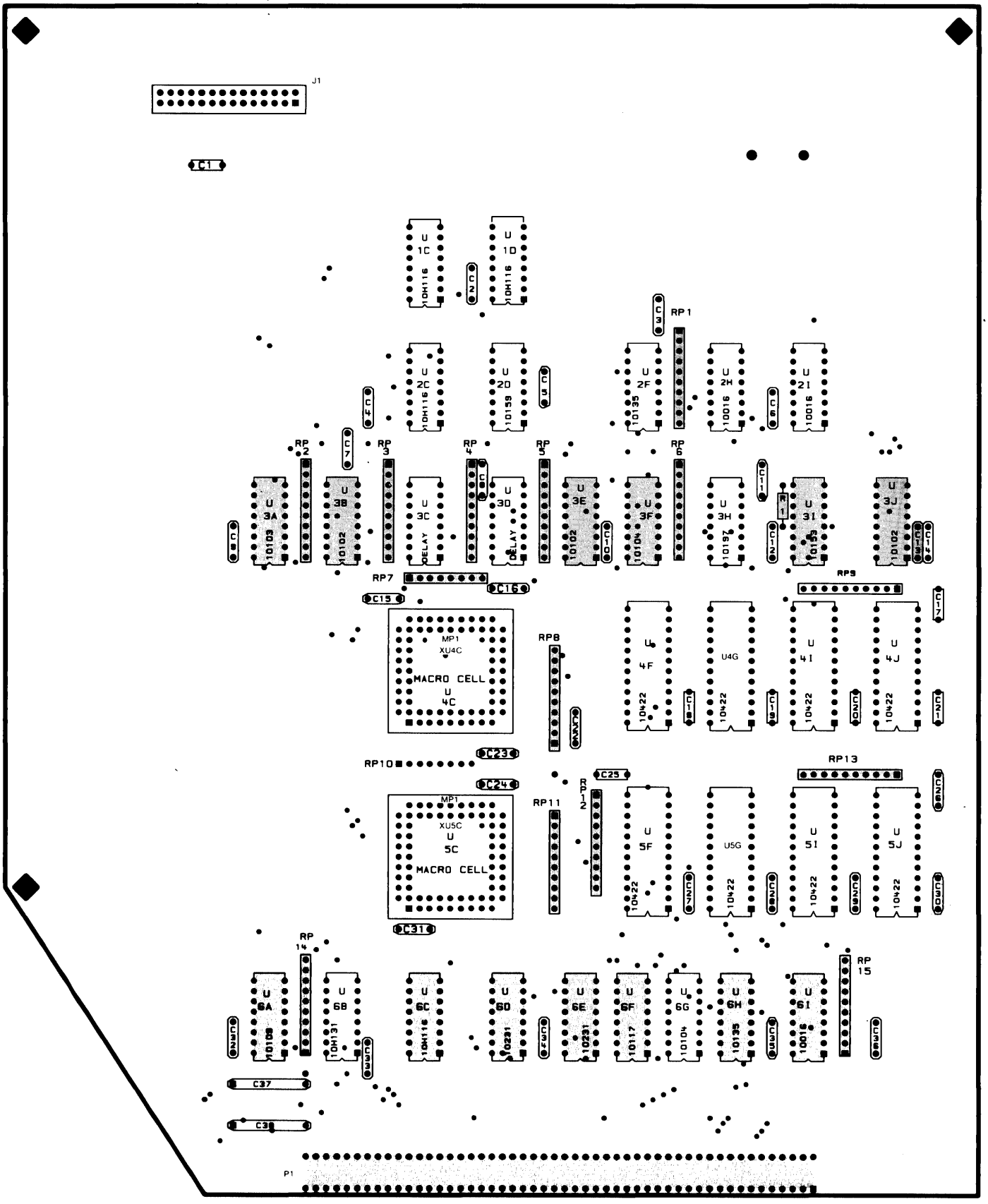
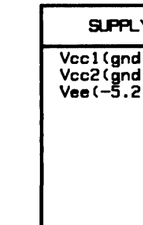


Figure 8E-2. Timing Slave Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U3A,B,E,F,I,J, U6A,C-I

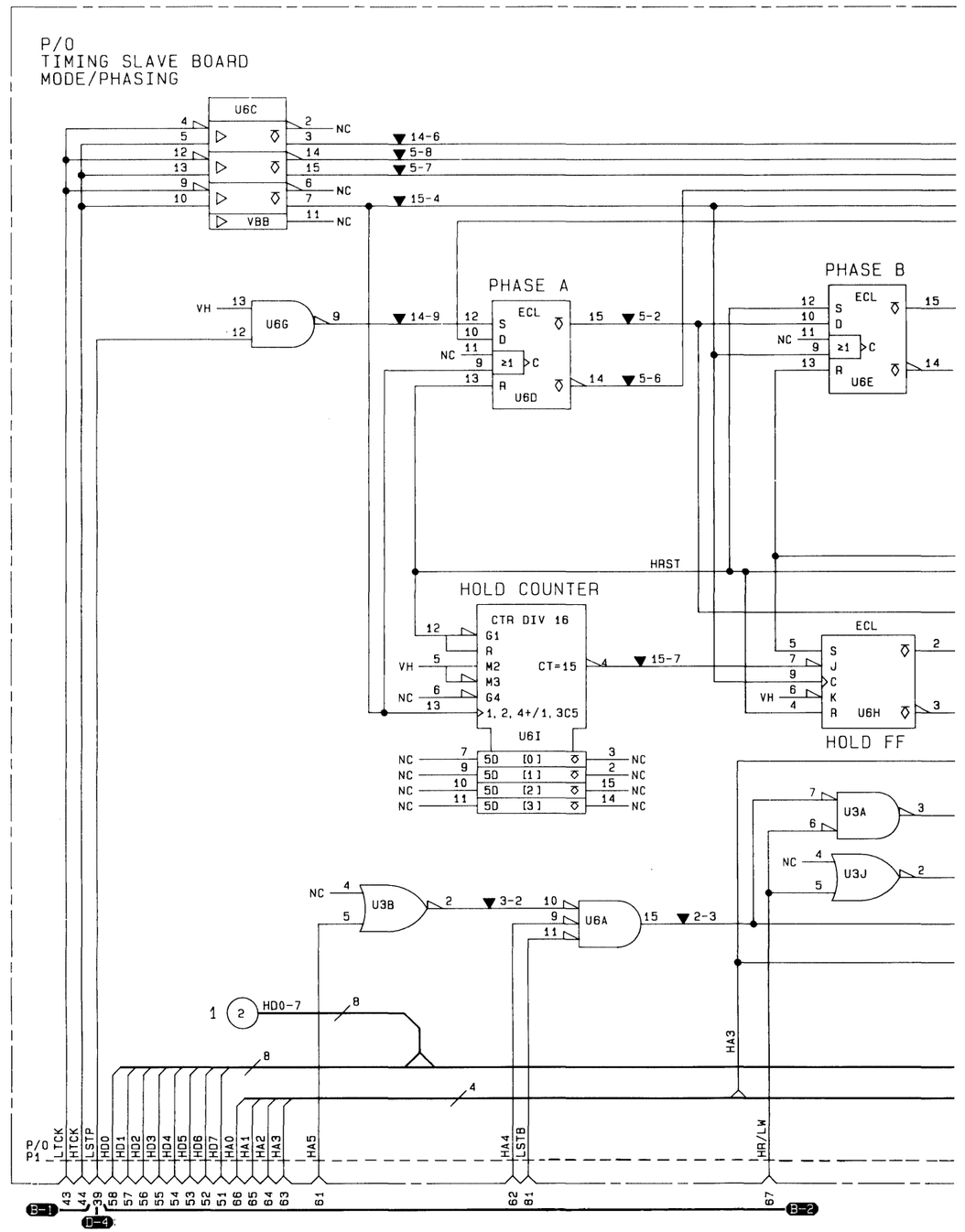
RESISTOR PACK DESCRIPTIONS:



RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6, 8,9, 11-15	100 X 9	1	-2.4
7,10	100 X 4	2,4,6,8	-2.4

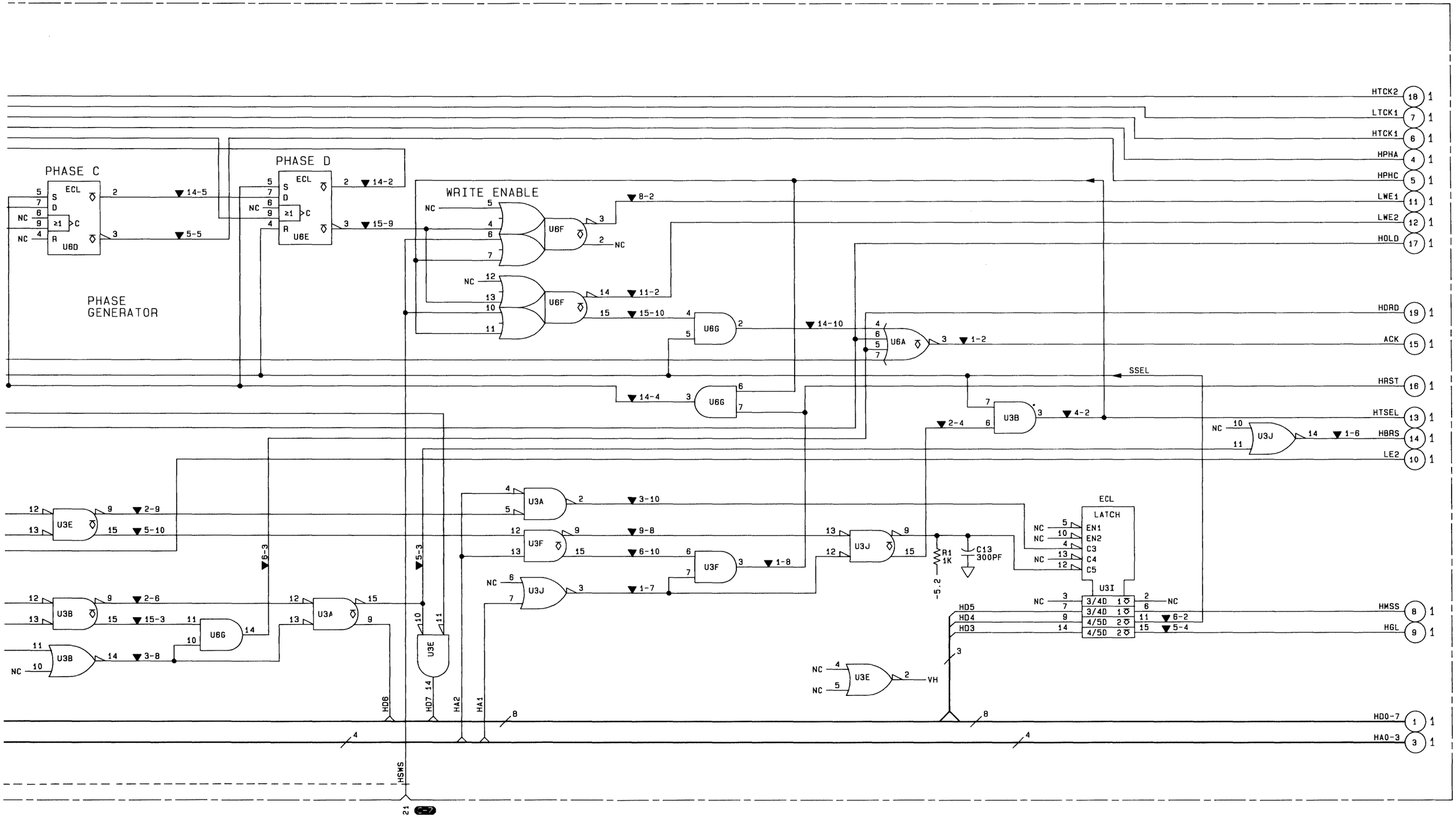
PARTS ON THIS SCHEMATIC

U3A,B,E,F,I,J,6A, U6C-I C13 R1 RP1-8,11-15	



PHASE B
PHASE C
PHASE D
PHASE GENERATOR
WRITE ENABLE
HOLD FF
LATCH
U6E
U6D
U6F
U6G
U6H
U3A
U3B
U3E
U3F
U3J
U3I
R1 1K
C13 300PF
LPHB
SSEL
HSWS
HD6
HD7
HA2
HA1
HD5
HD4
HD3
VH
ECL
NC
B-2
C-7

Figure 8E-4. Tim



8E-2

Figure 8E-4. Timing Slave Schematic (2 of 2)

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SERVICE GROUP 8F
STATE SLAVE

8F-1. INTRODUCTION

The optional state slave board adds thirty channels of state data to the 1630A. A 1630D can be upgraded to replace eight timing/state channels with thirty state channels. The 1630G thus provides fifty-seven state channels and eight timing/state channels.

The State Slave board adds state count and time count for state listings. It also provides non-volatile memory for storing instrument setup and microprocessor program disassemblers.

Table 8F-1. Master and Slave State Board Comparison

STATE MASTER BOARD	STATE SLAVE BOARD
Three Data Clock Inputs	
27 Data Inputs	30 Data Inputs
Acquisition RAM (1K x 28)	Acquisition RAM (1K x 32)
Pattern RAM	Pattern RAM
Measurement Control Circuitry	
Data Clock Processing	
	State and Time Counter
	Two Threshold Circuits
	EEPROM Memory for CPU

8F-2. STATE SLAVE BLOCK DIAGRAM (see Figure 8-1)

POD INTERFACE. Input data from up to three 10-bit pods is taken at the user's sample rate.

ACQUISITION MEMORY. The width of the acquisition memory is 32 bits. Thirty bits are used for data from the system under test and two bits are used to send the condition of two flags to the 1630 microprocessor.

MEMORY ADDRESS COUNTER. Holds the address of the next location in acquisition memory to be filled. This counter also addresses the time interval RAM.

PATTERN RECOGNITION RAM. Input width is 32 bits and output width is 4 bits. Two of the input bits are unused. The CPU pre-loads the RAM, so that a particular 30-bit data pattern will address a 4-bit word corresponding to one of the four specified patterns.

GRAY CODE COUNTER. The Gray Code Counter is a 20-bit counter used to count stored states, time intervals, or the number of occurrences of a particula event over a period of time. It has a 20-bit gray code output.

COUNTER RAM. This RAM stores the output of the Gray Code Counter. Both time counts and state counts are stored, depending on the instrument setup.

ADDRESS DECODERS. The address decoders, two in the control circuitry and one in the EEPROM circuitry, split the available addressing into two sections, one for the primarily ECL control circuitry and the other for the primarily TTL EEPROM circuitry. Further decoding controls latching of data onto and off of the microprocessor data bus.

25 MHZ OSCILLATOR. The 25 MHz oscillator clocks the Gray Code Counter. The 25 MHz signal is also used to synchronize other control signals for the counter.

CONTROL CIRCUITRY. The control circuitry provides the various control lines and clocks.

THRESHOLD CIRCUITRY. The threshold circuitry provides threshold to pods 6 and 7. Ground sense lines provide the ground level of the system under test.

EEPROM CIRCUITRY. EEPROM memory is used to store the inverse assembler data loaded from tape or disc. It is also used to store instrument setups. Only the microprocessor has access to EEPROM. None of the storage space is used for data from this board.

EEPROM is a non-volitile memory that operates on TTL levels, therefore requires the accompanying buffers and translators. An address counter is also included.

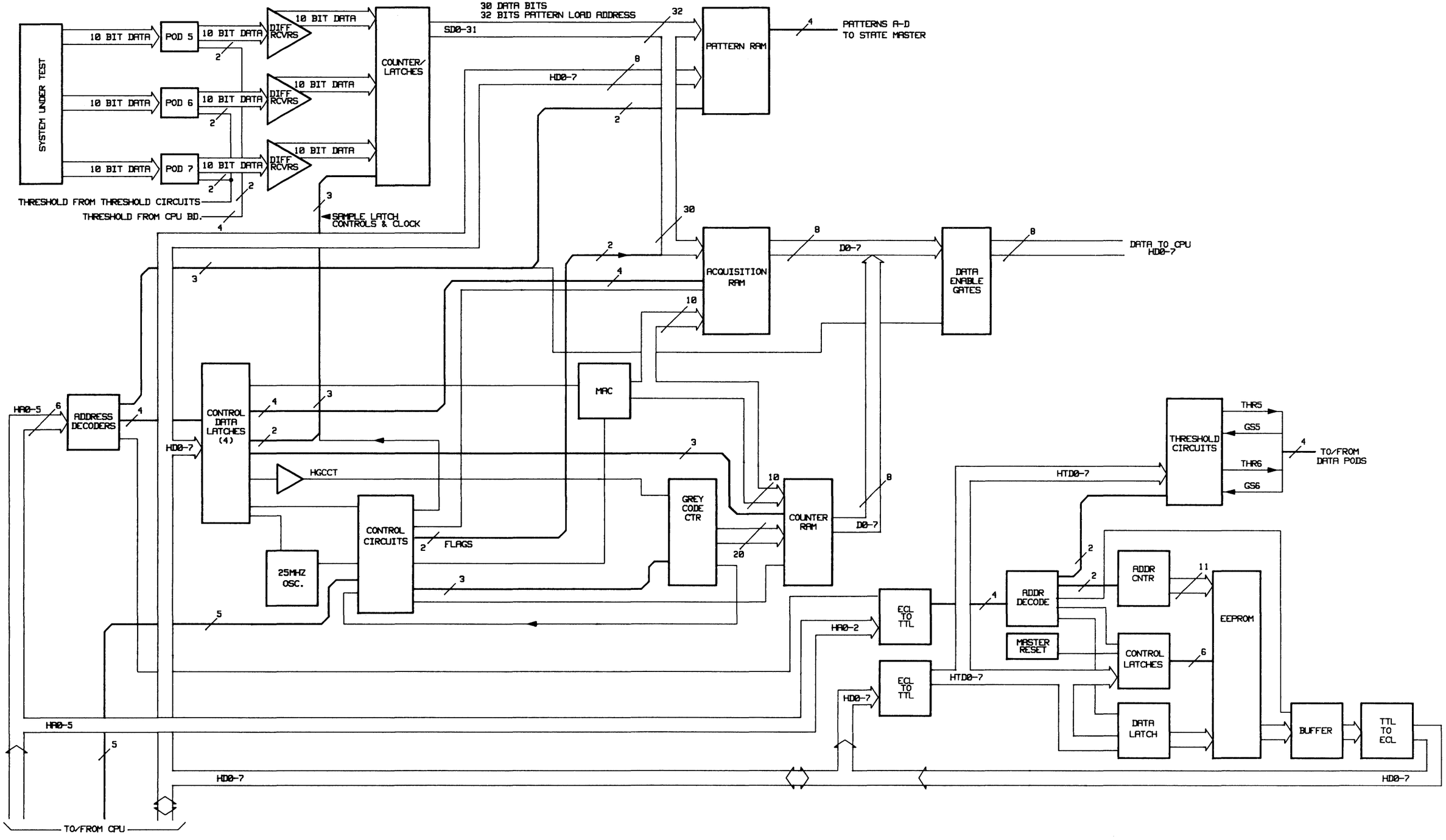


Figure 8-1. 1630G State Slave System Block Diagram

NOTES

8F-3. THEORY OF OPERATION

8F-4. Data Acquisition Interface (see schematic 8F-1)

Three pods (5, 6, 7) each supply ten channels to the line receivers. The ten channels from each pod go from line receivers into 4-bit counters, (U2B-U2I). The counters work as data sample latches during a run and as address counters for programming Pattern Recognition RAM before a run. SLM selects either the latch mode or counter mode. It is low in the latch mode. SLCLK clocks data through the latches in the run mode and toggles the counters to address the pattern rams when the microprocessor is loading patterns. HSLR resets the counter/latch with a high.

The CPU board supplies ground sensing and precision threshold for pod 5. Pods 6 and 7 thresholds are provided by circuitry on this board (schematic 8F-5).

8F-5. Acquisition and Pattern Memory (see schematic 8F-2)

8F-6. ACQUISITION MEMORY. The acquisition RAM is organized as 32 bits wide by 1024 words deep--30 bits for data storage, with 2 bits used to send the condition of two flags to the microprocessor. The 30 data channels are written into memory in parallel. During an acquisition cycle all four select lines (LARS1-4) are pulled low. The write enble line (LARWE) is also pulled low. When a qualified state is present on the data lines LARWE is put high, the memory address counter is incremented and LARWE put low again.

To read data from RAM, LARWE is put high and the select lines select RAM pairs to output eight-bit data on to the bus.

8F-7. MEMORY ADDRESS COUNTER. The Memory Address Counter consists of three 4-bit counters, of which ten bits are used. It addresses both the acquisition RAM and the counter RAM (schematic 8F-4). HMACR is the reset line and MACCLK is the clock.

8F-8. PATTERN RECOGNITION RAM. Pattern Recognition RAM consists of four 256 x 4 ECL RAM ICs connected in parallel, allowing an addressing width of 32 bits. Input width is 30 bits--two of the address lines do not carry data. Output width is 4 bits. The 30-bit incoming sample from the data pods addresses Pattern Recognition RAM. The four bits from each RAM location go out over the pattern lines, LAS-LDS, to the State Master board where they are ANDed with pattern lines from the State Master board and Timing board.

Before a run, the CPU pre-loads each 4-bit RAM location. The locations are addressed by the sample latches working in the counter mode. During a run, when a RAM location is addressed by the incoming sample, its four bits are output on the four pattern lines A-D. When one or more of these four bits is low, the corresponding pattern line may be driven low. A 30-bit incoming data sample that forms a pre-specified pattern of highs, lows, and don't-cares will address one of those RAM locations that was pre-loaded with at least one low.

For example, if the eight input sample bits to a single RAM chip are 00000000, then the first location will be addressed. If the four bits stored in that location are 1100, then pattern output lines A and B--corresponding to the two lows--from that RAM will try to go low.

However, each of the four output bits from each pattern RAM are ECL wire-ANDed. (ECL outputs may be connected together like open-collector TTL outputs.) Thus, a pattern line can be active only when all four RAMs have a low on the same output.

As shown in figure 8C-3, four pattern lines also come into the State Master board from the Timing Master board. (The State Slave board takes the place of the Timing Slave board.) When the Timing Master board is in the state mode, the macrocells act like pattern recognition RAM. The pattern lines from the Timing Master and State Slave boards are gate-ANDed, then wire-ANDed with the four State Master pattern lines. Thus, for a single pattern line to be driven low, the Timing Master and State Slave boards and all four RAM chips on the State Master board must agree. (When the timing board is not in the state mode, its pattern lines will be low).

If more than one of the pattern lines are low at the same time, the sequencer will select the one required for the next analyzer state, according to the trace specification.

8F-9. Acquisition and Counter Control (see schematic 8F-3)

This circuitry provides control for most of the ECL circuitry on the board. the Address Decoders and Control Data Latches allow the CPU to control measurements. A 25 MHz oscillator is used as a time reference for timing measurements. The Reset Flip-Flops are used to reset the Gray Code Counter.

8F-10. ADDRESS DECODERS. The Address Decoders (here and on schematic 8F-5) split the 16 available addresses into two groups of eight, one group for ECL control and one for TTL control. The eight low order addresses of the two groups are decoded here by U8N and U8M. LTTL, from U8N pin 11, is used to select the TTL group on schematic 8F-5. The outputs of U8M control output of acquisition data onto the bus (HADE), writing of data into pattern RAM (LPRWE1,2), and latching of data into the control circuitry.

8F-11. CONTROL DATA LATCHES. These latches control configuration of the circuitry for making the specific measurements. Performance and operation verification signals are also outputs into the control circuitry.

8F-12. 25 MHZ OSCILLATOR. The 25 MHz Oscillator clocks the Gray Code Counter (schematic 8F-4) in the time count mode. The oscillator is also used to synchronize part of the counter reset circuit.

8F-13. TIME COUNT CLOCKING. The 25 MHz path through the control circuitry is from U8I pin 6, through U7I pins 7 and 3, and U8I pins 5 and 3 onto the GCCCLK line. A high at U5M pin 14 will disable the oscillator so that the CPU can clock the counter for test purposes.

The 25 MHz signal is gated by U8K pin 2. A high on the set input, pin 5, inhibits the 25 MHz with the resulting low at pin 2. When the set is removed, the clock signal at pin 6 will synchronize the return of pin 2 to a high level so that only complete clock pulses will be gated.

8F-14. STATE COUNT CLOCKING. When the counter is used to count states the 25 MHz line, GCCCLK, is put high by U5L pin 13. The GCCSI line, which must be high for 25 MHz clocking, is now used as a clock. The source of the clock is HSCS which is derived on the State Master board. Forms of it are used there to clock data and address counters.

8F-15. GRAY CODE COUNTER RESET. Five flip-flops synchronize the reset of the Gray Code Counter. U7KA catches the overflow from the MSB of the counter when the count has reached about 350K. U7LA synchronizes the output of U7KA with the control system The output from pin 2 is also used to flag the CPU that the counter is resetting (HCRF). U7LB resets the counter after a qualified state has been stored. U7MA/B sequence the reset of the counter. The output of U7MA is also used to reset the reset flip-flops.

8F-16. Gray Code Counter and Memory (see schematic 8F-4)

8F-17. GRAY CODE COUNTER. The Gray Code Counter is a 20-bit counter with a 17-bit mantissa (bits 0-16) and 3-bit exponent (bits 17-19). The CPU uses algorithms to convert the gray code to the count figure.

U4M and Q1 are a power supply which provides -3.25V +/-3%. U8L is part of the reset circuit. The reset signal HGCCR resets the counter. U8L provides a complementary signal that is delayed by C64. The delayed signal terminates reset at pins 34 and 35.

8F-18. COUNTER RAM. The Counter RAM is addressed by the Memory Address Counter (schematic 8F-2). A count can be stored for each valid state stored. LCRS1-3 gate the RAMs and allow them to be read onto the data bus eight bits at a time. LCRWE is the write enable. It goes high at the termination of write when the valid state has been stored.

8F-19. EEPROM and Threshold Circuitry (see schematic 8F-5)

The Electrically Erasable PROM is used by the CPU for storage of one instrument setup and storage of inverse assemblers written to the 1630G from disc or tape.

8F-20. ADDRESS DECODER. The address decoder decodes the eight high order addresses alloted to the state slave board. The LTTL signal, decoded in U8N (schematic 8F-3), allows decoding of HA0-2 by U7C. The decoded signals primarily control latching of data into and out of EEPROM and latching of data into the Threshold DACs. Two lines clock and reset the Address Counter.

U6L is part of a board identifier. The CPU does a read from address hex 10 which outputs, through U6L, a hex 20 onto the data bus. That identifies this board as a state slave. The CPU therefore knows the configuration of the instrument.

8F-21. ELECTRICALLY ERASABLE PROM. The EEPROM is controlled very much like a comparable CMOS RAM. However, it is non-volitile but can be erased by writing over data previously stored. CPU data is converted to TTL from the ECL on the data bus. It is latched onto a bus connecting all EEPROMS. The EEPROMs have inputs that also serve as outputs but are shown separately on the schematic.

When the EEPROMS are read, the data is gated onto the data bus by U7G. The pull-ups on the output of U7G provide additional drive to the TTL-ECL converters. This ensures that when the data buffer is disabled and has high outputs the TTL-ECL inputs will be high enough to ensure low outputs. This allows other devices to drive the bus.

8F-22. ADDRESS COUNTER. The Address Counter consists of three 4-bit counters of which 11 bits are used. A fourth counter is connected but not used. The counter is clocked and reset by the CPU.

8F-23. MASTER RESET. The Master Reset holds off the write circuitry from the EEPROMS when the power supply voltage is out of tolerance. All outputs of U7E are low in the reset mode. U7D functions only as an inverter to keep the control inputs of the EEPROMS high to prevent writing erroneous data upon power-up.

8F-24. THRESHOLD CIRCUITRY. The Threshold DACs are programmed by the data bus to provide a current level proportionate to the threshold level required. The current level is converted to a voltage level by U6B. The ground sense lines compensate the threshold for differences in ground level in the target system.

8F-25. MNEMONICS.

The following signals, listed in alphabetical order, are used on the State Board. Active high signals have "H" as the first letter; active low signals have "L".

Table 8F-2. Mnemonics

Mnemonic	Description
D0-7	Data from counter RAM.
GCCCLK	GRAY CODE COUNTER CLOCK/Enable. Clocks the Gray Code Counter in the time count mode. Must be high to enable state count clock, GCCSI.
GCCSI	GRAY CODE COUNTER STATE INCREMENT/Enable. Clocks the Gray Code Counter in the state count mode. Must be high to enable time count.
GS5,6	GROUND SENSE. Ground level voltage sense from target system.
HA0-5	CPU Address Bus from 1630 CPU board.
H/LACK	Address Clock. Increments memory address counter.
HADE	ACQUISITION DATA ENABLE. Enable for acquisition RAM data onto system data bus.
HCRF	COUNTER RESET FLAG. Flags the 1630 CPU when the Gray Code Counter is resetting.
HD0-7	1630 System Data B to CPU board.
HGCCOF	GRAY CODE COUNTER OVERFLOW.
HGCCR	GRAY CODE COUNTER RESET. Positive edge initiates counter reset.
HGCCT	GRAY CODE COUNTER TEST. During performance verification is used to divide the counter into two 10-bit sections for faster testing.
HMACR	MEMORY ADDRESS COUNTER RESET.
HSCS	State Clock Slave. State clock for State Mode.
HSLR	SAMPLE LATCH RESET. Resets the Data Sample Latch/Pattern Programming Counters.
HSWS	State Write Slave. State write enable to RAM in State Mode.
LARS1-4	ACQUISITION RAM SELECT. Select acquisition RAM pairs. All lines go low during data run. Enables RAM pairs during reads onto the system data bus.

Table 8F-2. Mnemonics (Cont'd)

Mnemonic	Description
LAS, LBS, LCS, LDS	Patterns from the Pattern Recognition RAM.
LARWE	ACQUISITION RAM WRITE ENABLE. Low during an acquisition run. Goes high when data on input lines is valid so data is stored. Put low to read data onto system data bus.
LCRS1-3	COUNTER RAM SELECT. Selects Counter RAM pairs to read data onto the system data bus.
LCRWE	COUNTER RAM WRITE ENABLE. Enables write to Counter RAM. Low-to-high edge terminates write when counter data is valid.
LCRZF	COUNTER RAM ZERO FLAG. When set, tells the CPU that the contents of the Counter RAM is to be interpreted as zero.
LPRWE1,2	PATTERN RAM WRITE ENABLE. Allows writing of pattern data from CPU into Pattern RAM.
LSTB	Strobe. CPU strobe for reading and writing to slave boards.
LTTL	Decoded address that selects TTL circuitry for addressing.
MA0-9	MEMORY ADDRESS. Addressing bus for Acquisition RAM and Counter RAM.
MACCLK	MEMORY ADDRESS COUNTER CLOCK. Clocks Memory Address Counter during acquisition using clock derived from target system. CPU clocks counter during read from RAM.
SD0-31	SAMPLE DATA. Data from target system that has been latched for use by Acquisition RAM and Pattern RAM.
SLCLK	SAMPLE LATCH CLOCK. Clock derived from target system during run mode. CPU clocks latch/counters during programming mode for Pattern RAM.
SLM	SAMPLE LATCH MODE. Selects latch or count mode for latch/counters.
THR5,6	THRESHOLD. Threshold voltage for Pods 6 and 7.

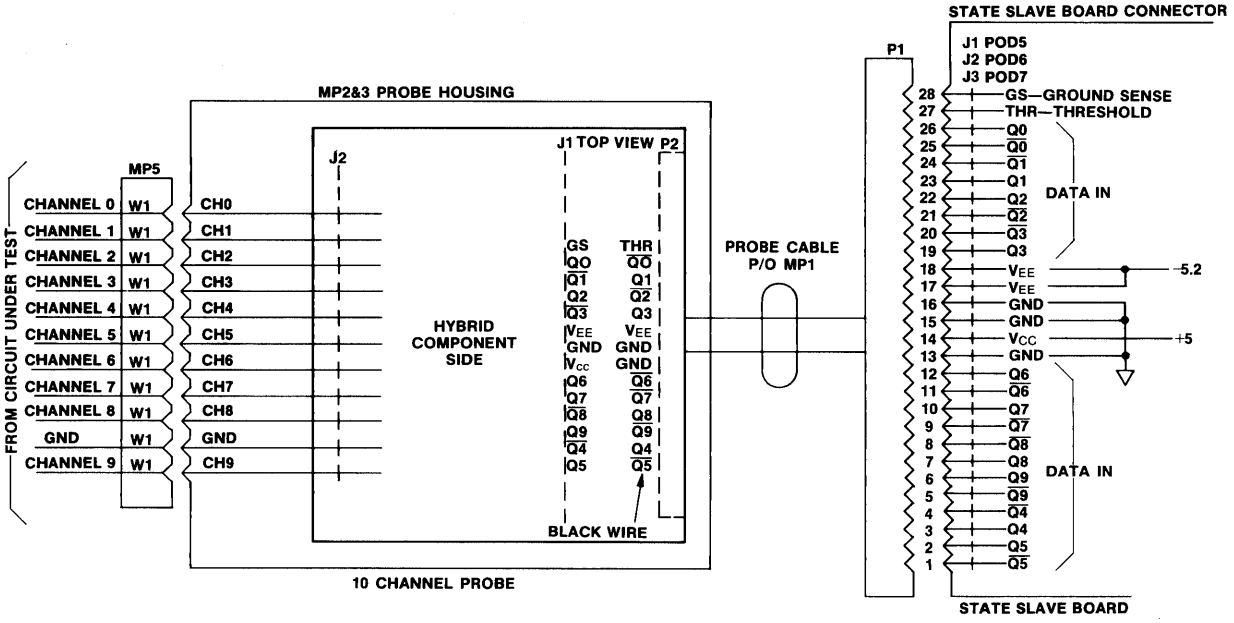


FIGURE 8F-2. State Slave Pod

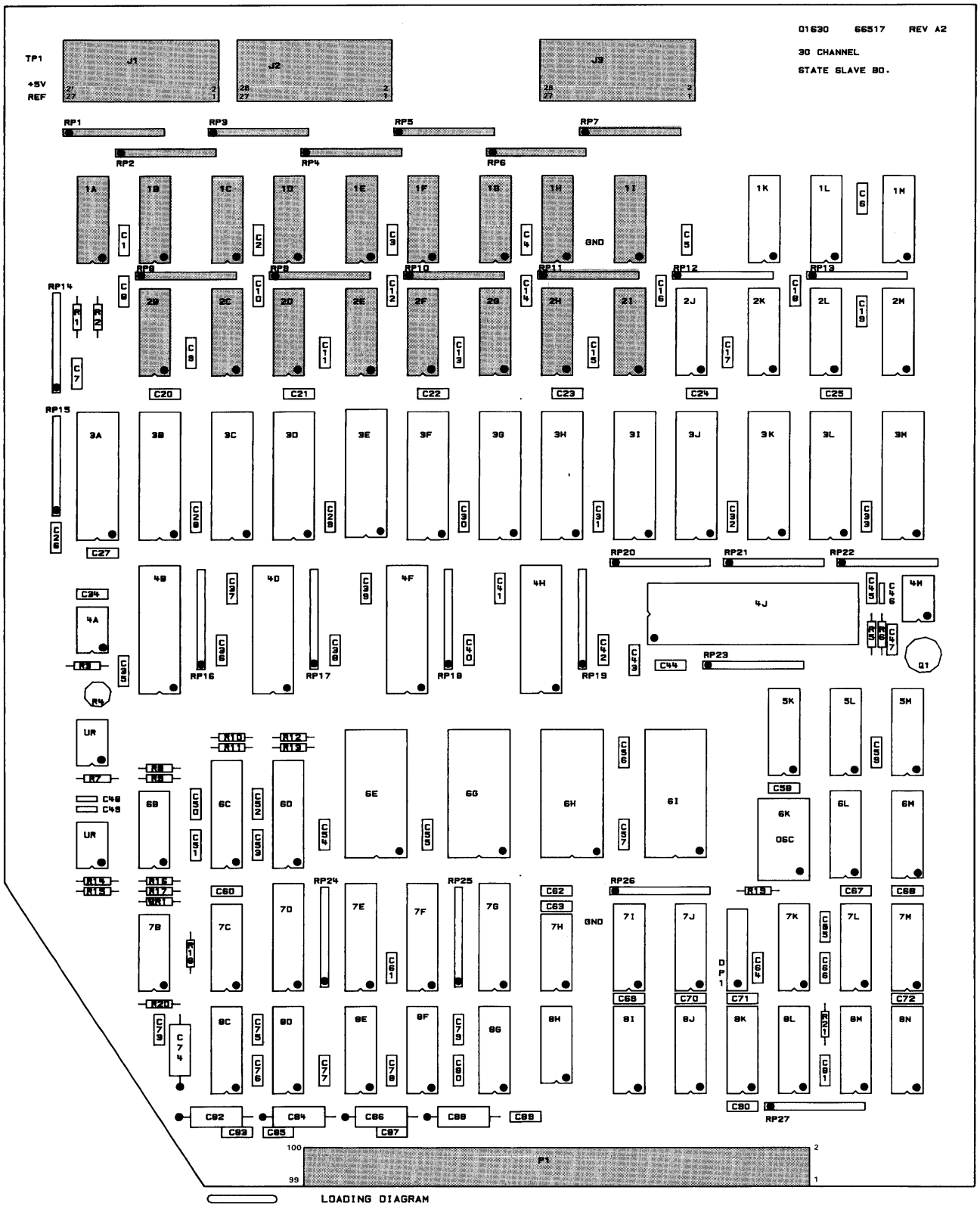


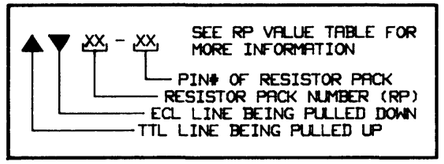
Figure 8F-3. State Slave Board Component Locator

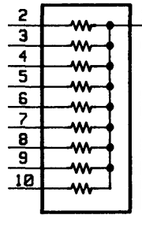
DATA AQUISITION INTERFACE

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:

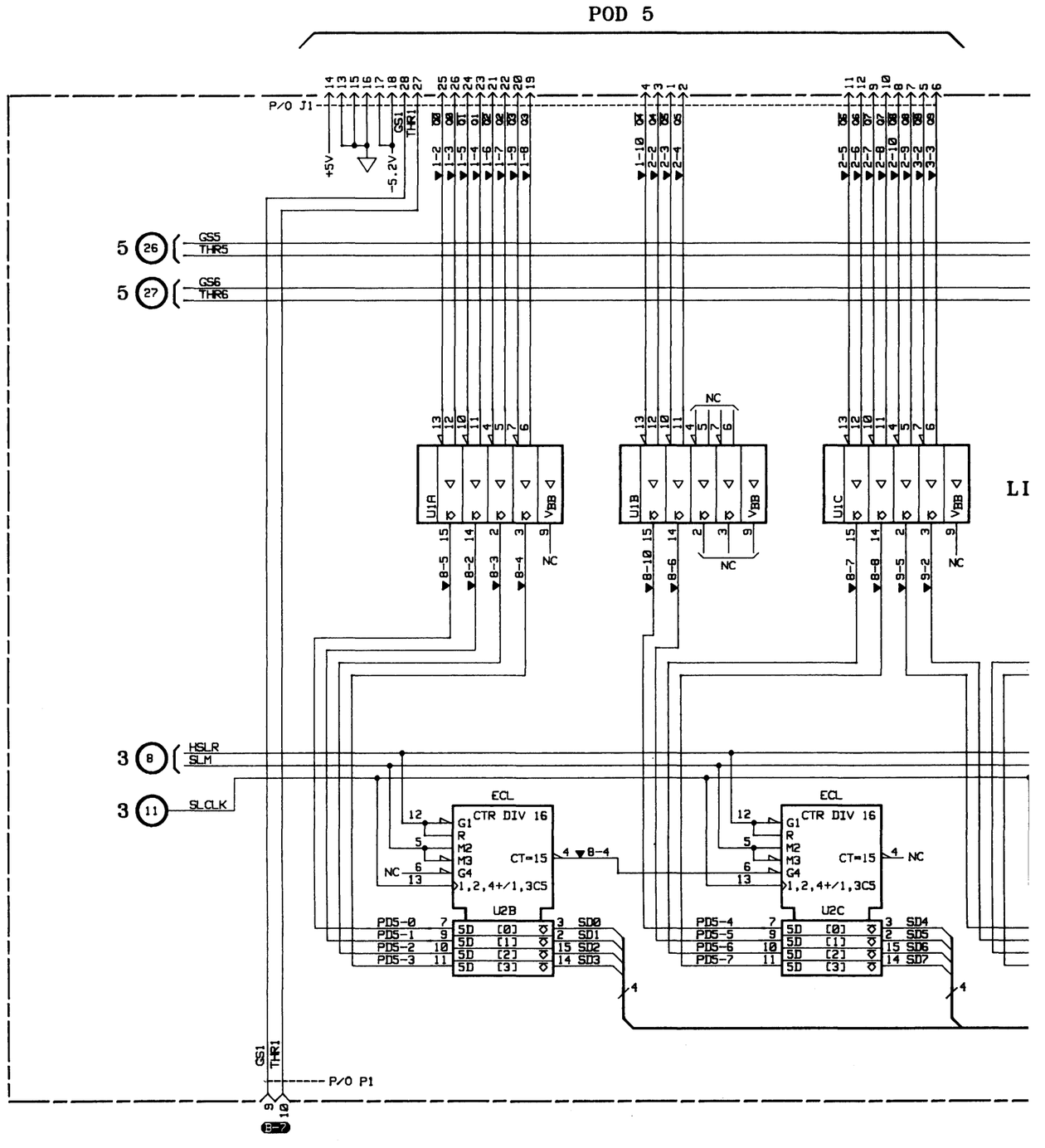


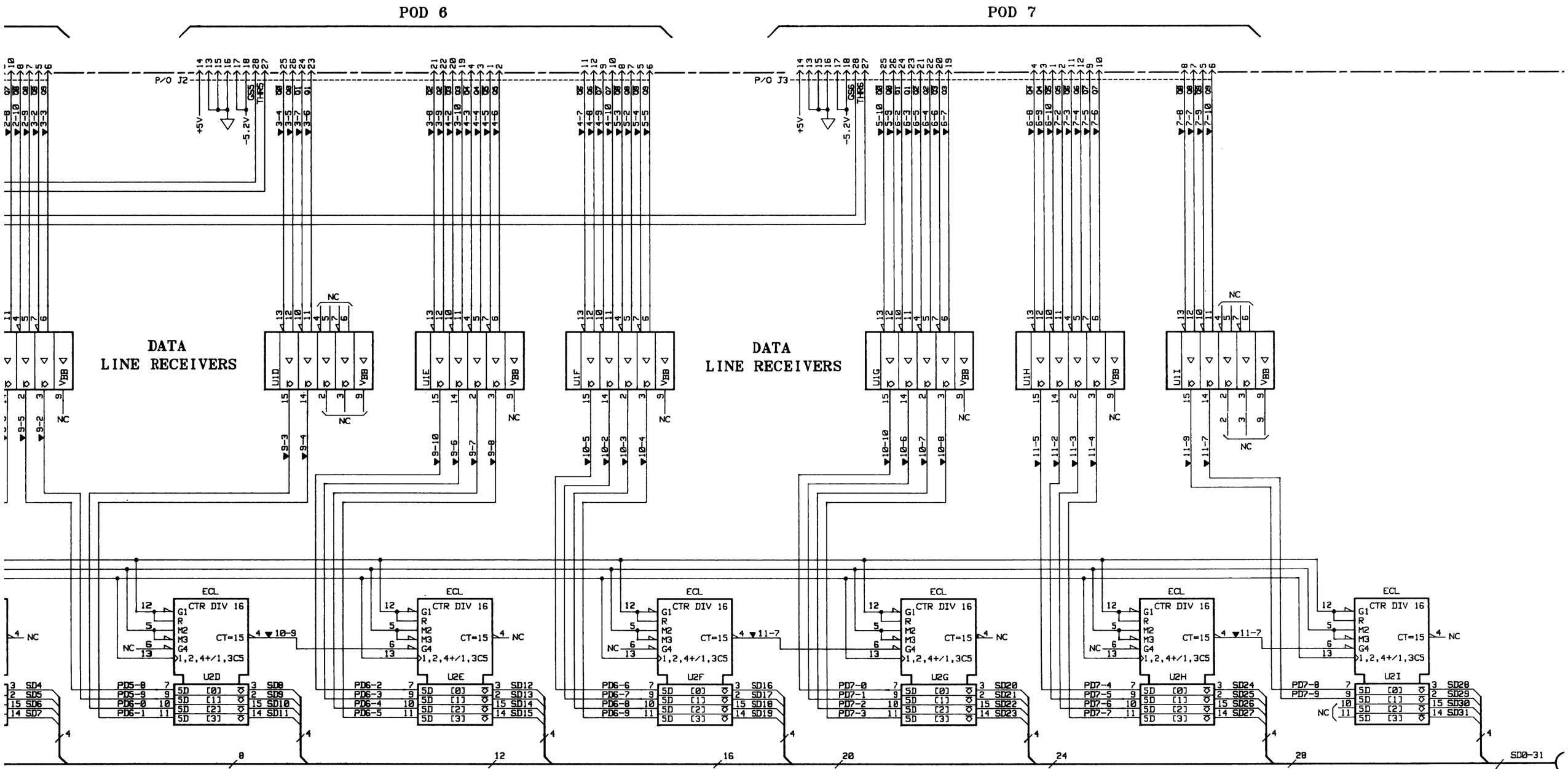


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

J1-3 P/O P1 RP1-11 U1A-I U2B-I	

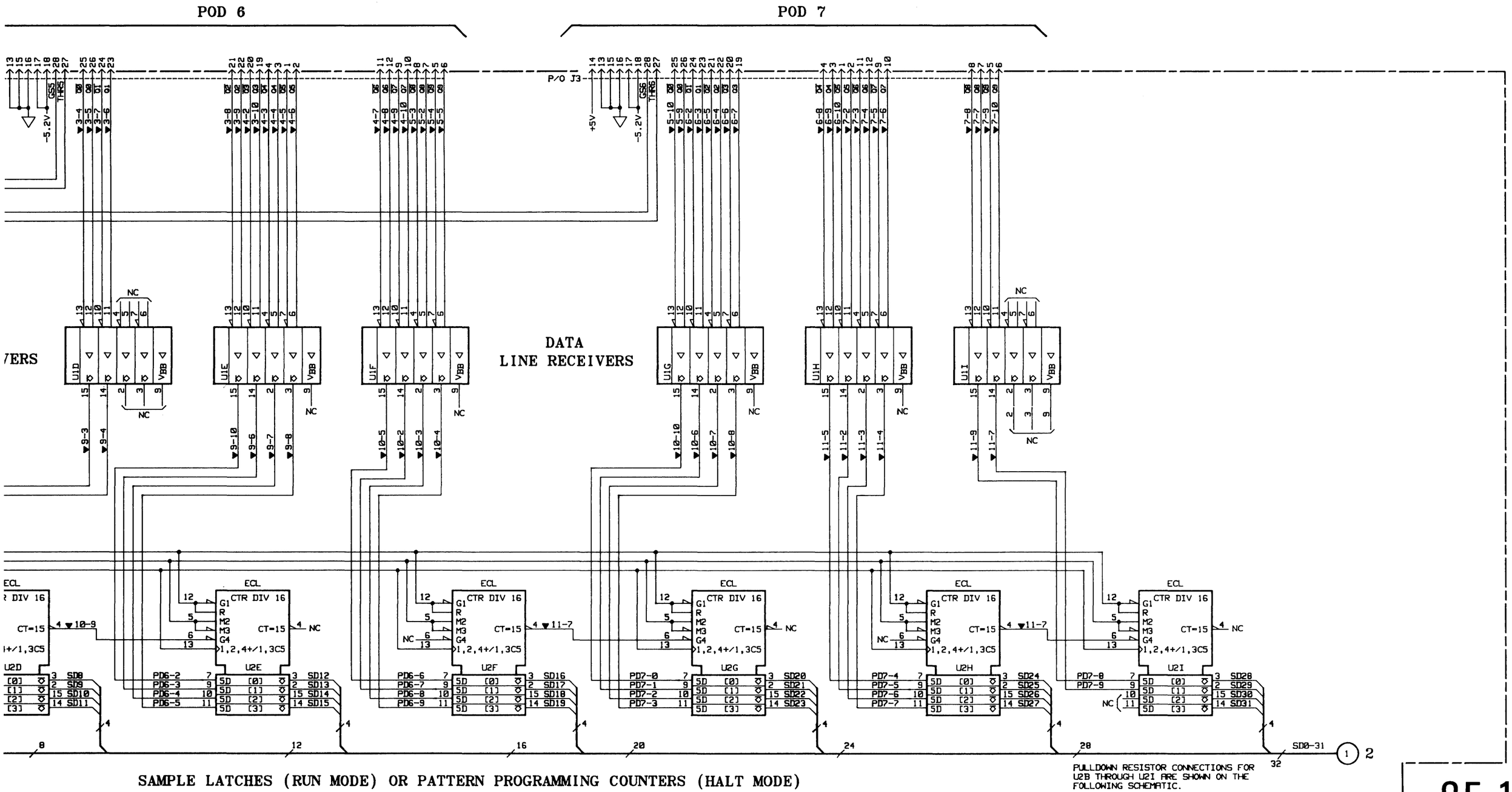




SAMPLE LATCHES (RUN MODE) OR PATTERN PROGRAMMING COUNTERS (HALT MODE)

PULLDOWN RESISTOR CONNECTIONS FOR U2B THROUGH U2I ARE SHOWN ON THE FOLLOWING SCHEMATIC.

Figure 8F-4. St



SAMPLE LATCHES (RUN MODE) OR PATTERN PROGRAMMING COUNTERS (HALT MODE)

8F-1

Figure 8F-4. State Slave Schematic (1 of 5)

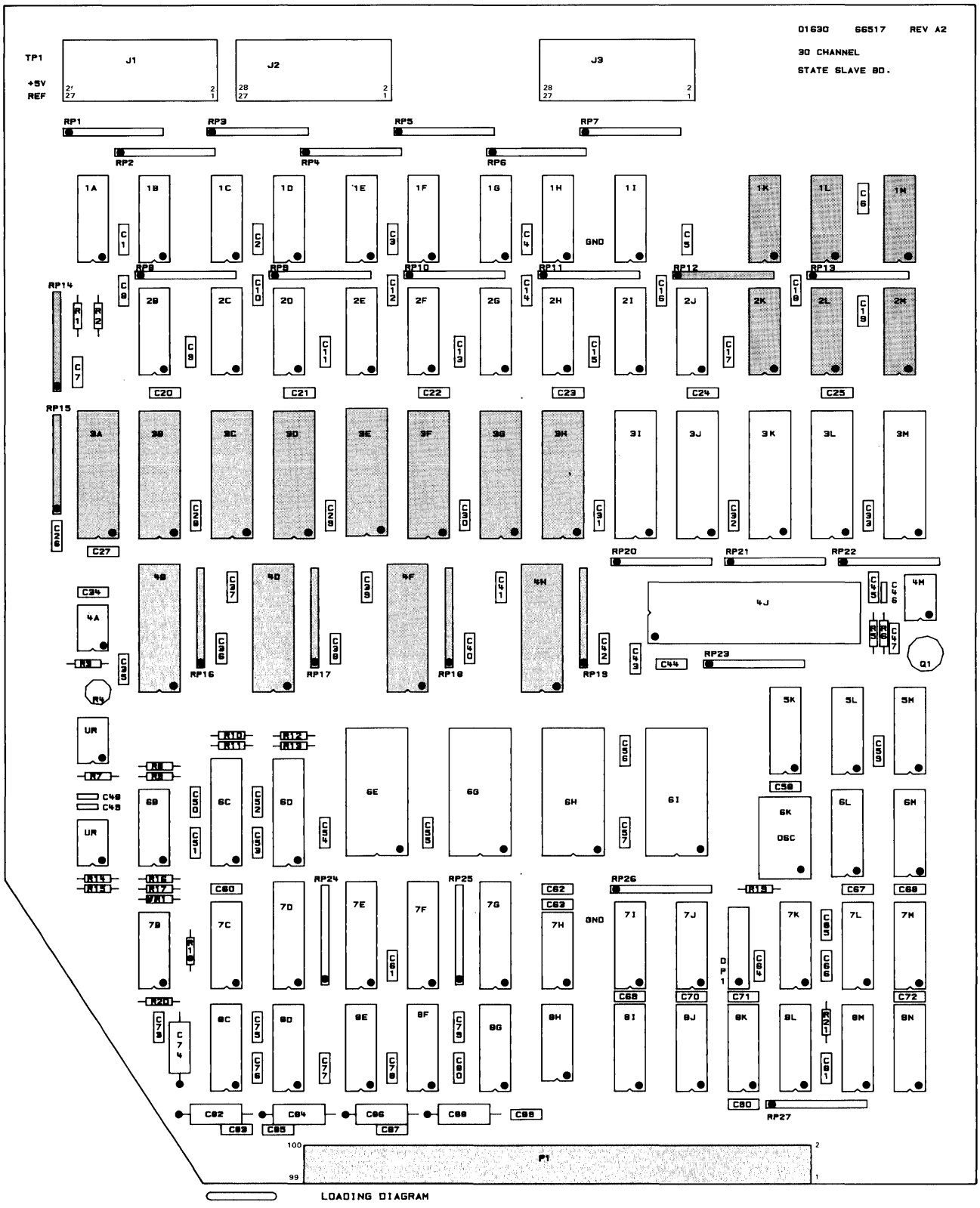
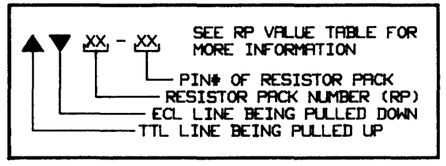


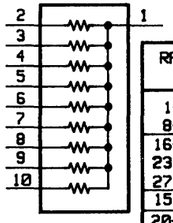
Figure 8F-3. State Slave Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:





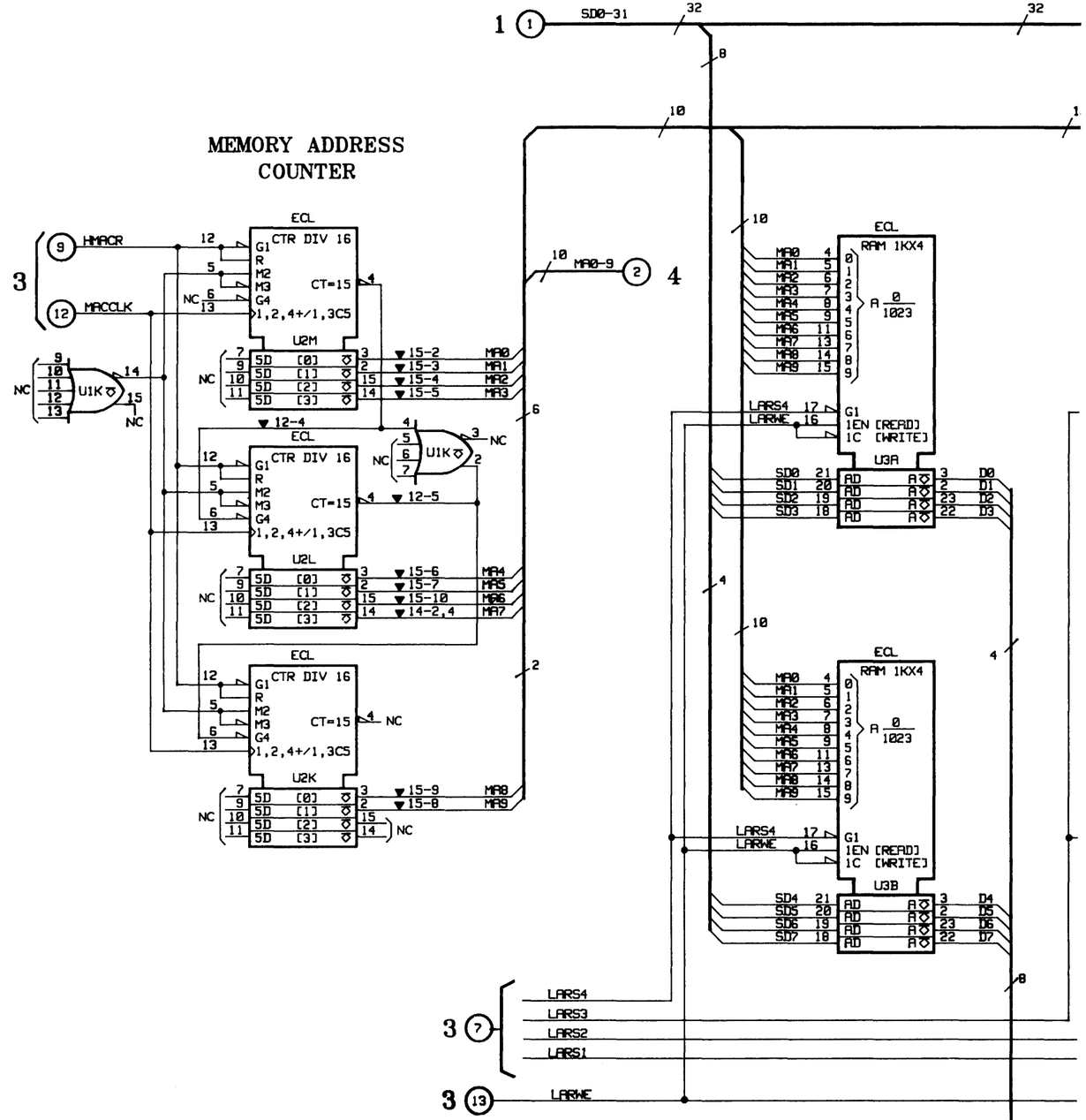
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

P/O P1 RP12,14,15,16-19 U1K-M,U2K-M,U3A-H, U4B-H	

ACQUISITION AND PATTERN MEMORY

MEMORY ADDRESS COUNTER



ACQUISITION RAM

PATTERN RAM

DATA ENABLE GATES

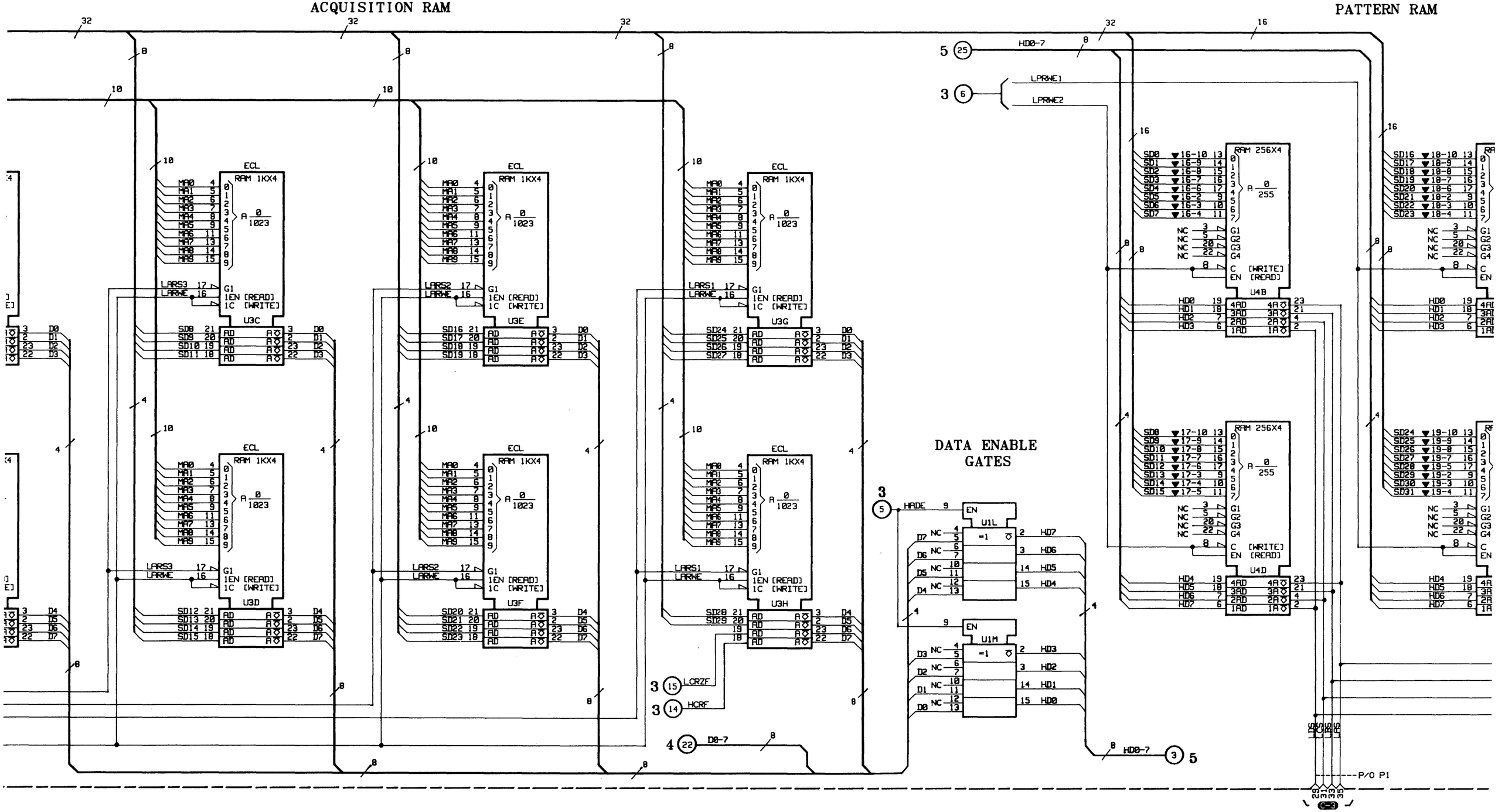


Figure 8F-4. St

ACQUISITION RAM

PATTERN RAM

DATA ENABLE GATES

P/O P1

Figure 8F-4. State Slave Schematic (2 of 5)

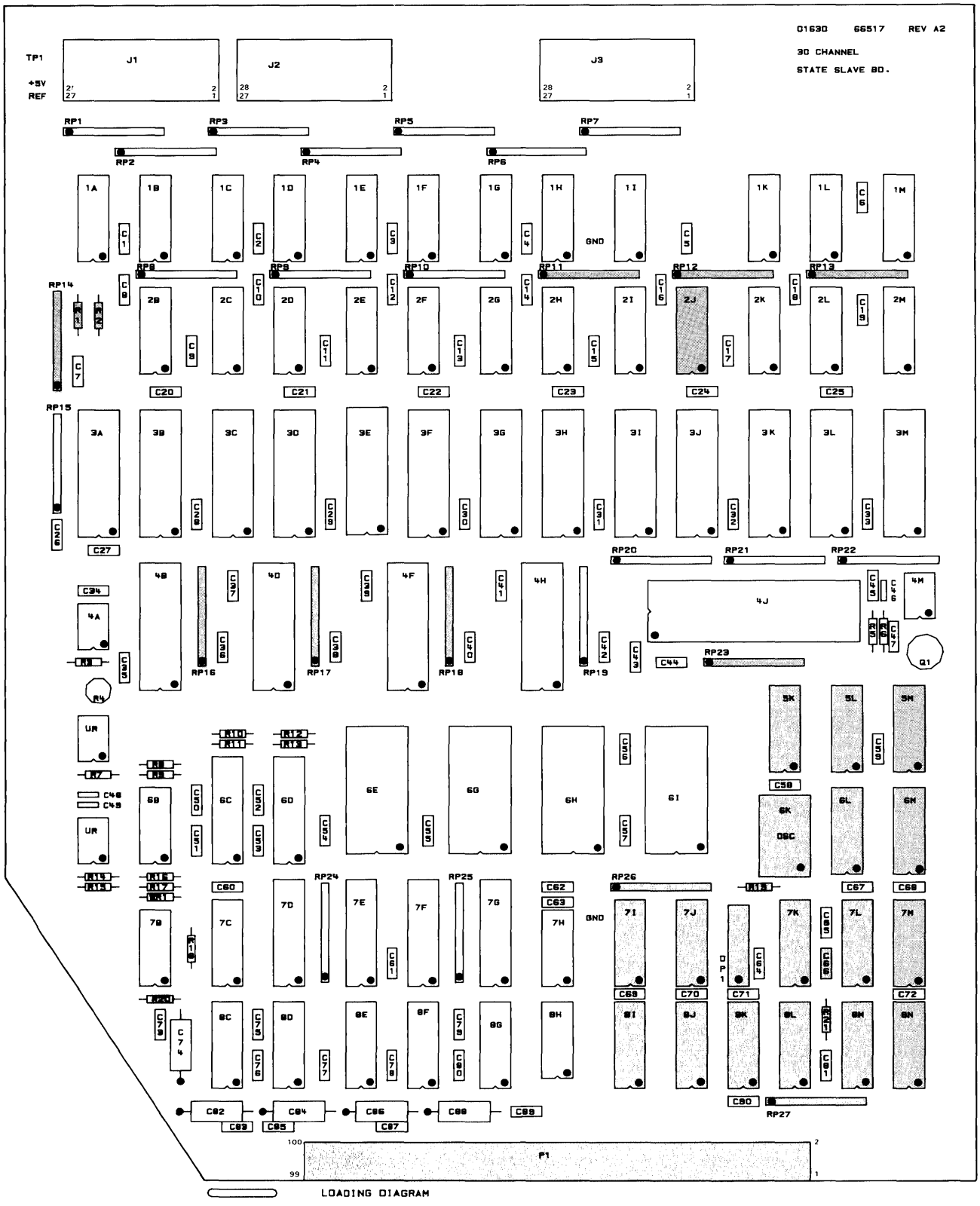
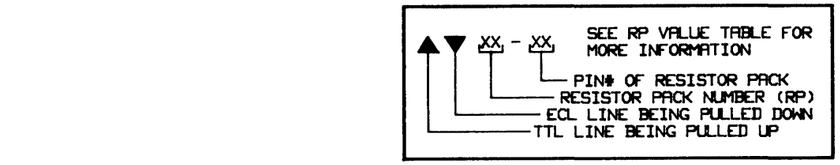


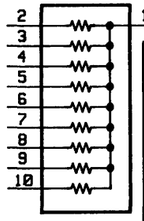
Figure 8F-3. State Slave Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:

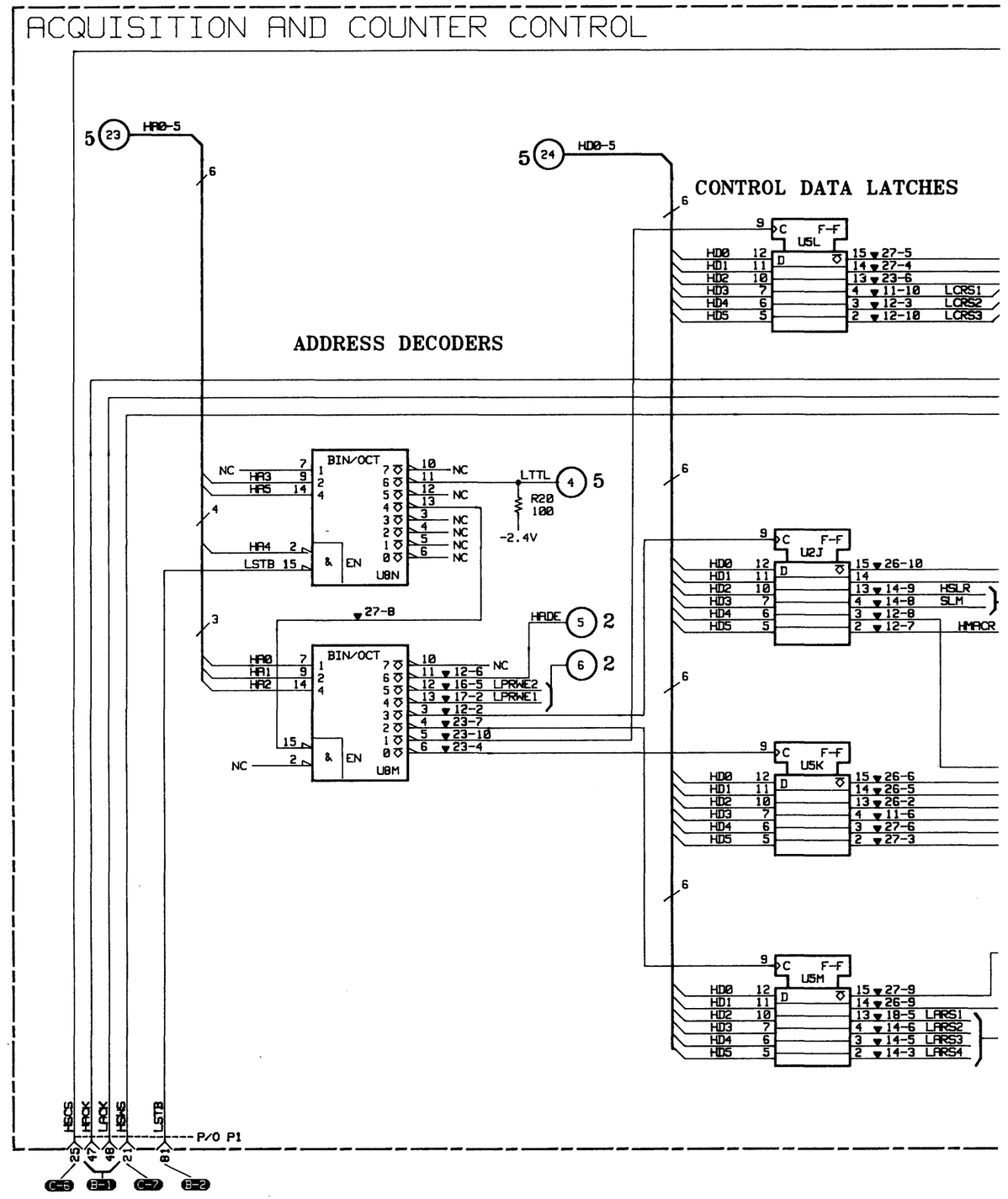




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

C66 P/O P1 R1,2,19-21 RP11-14,16-18,23, 26,27 U2J,5K-M,6K-M, 7I-M,8I-M	



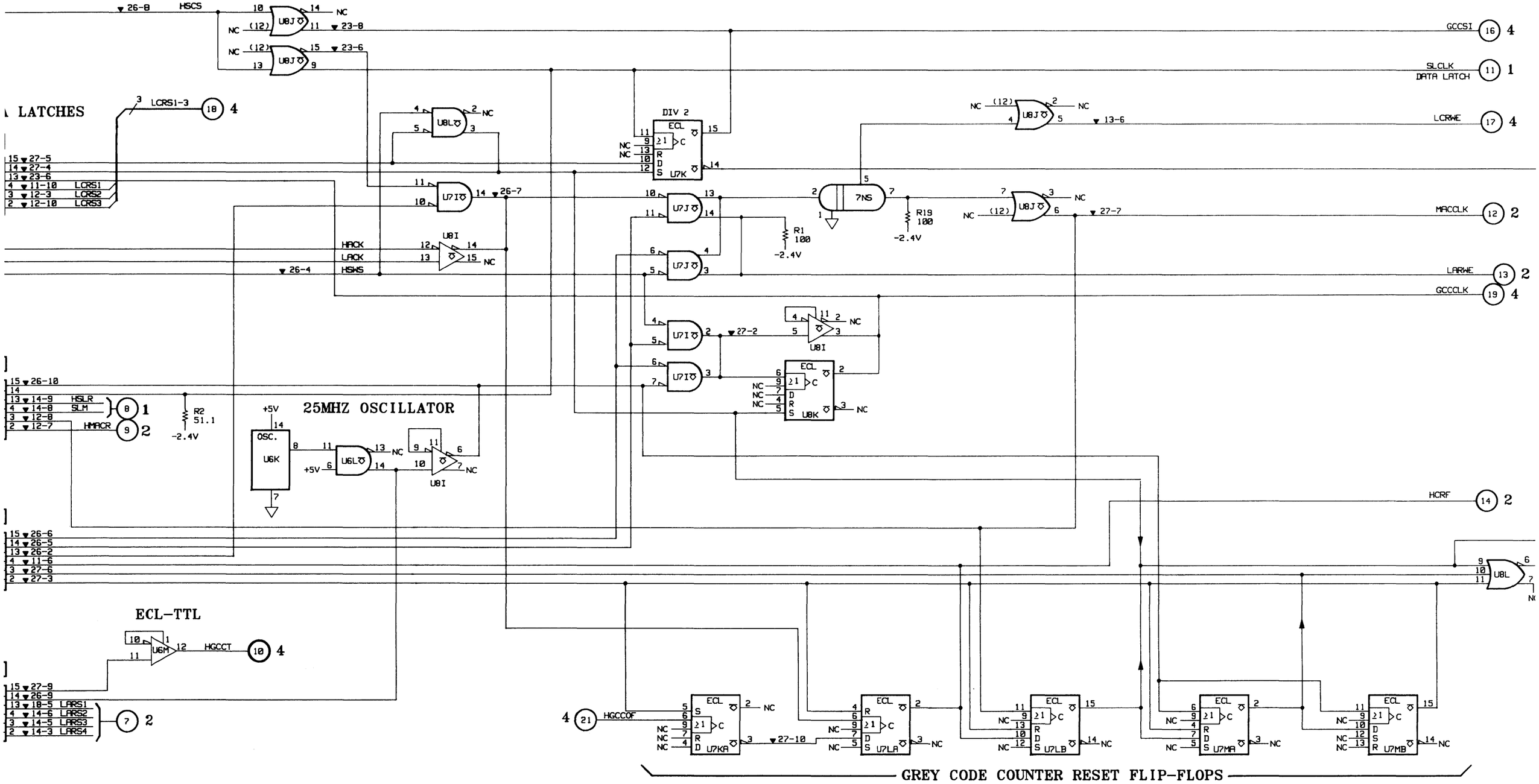
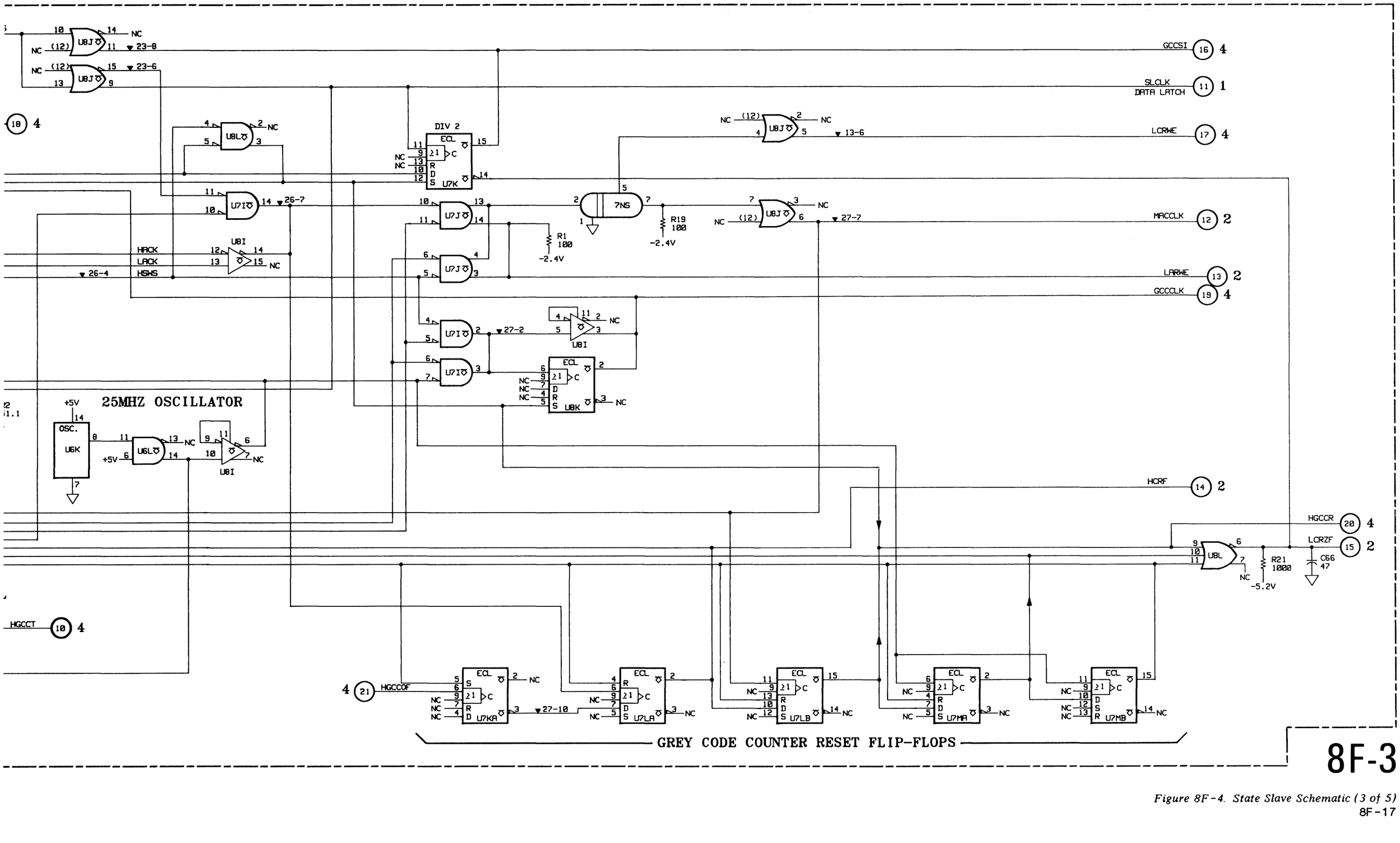


Figure 8F-4. St



8F-3

Figure 8F-4. State Slave Schematic (3 of 5)

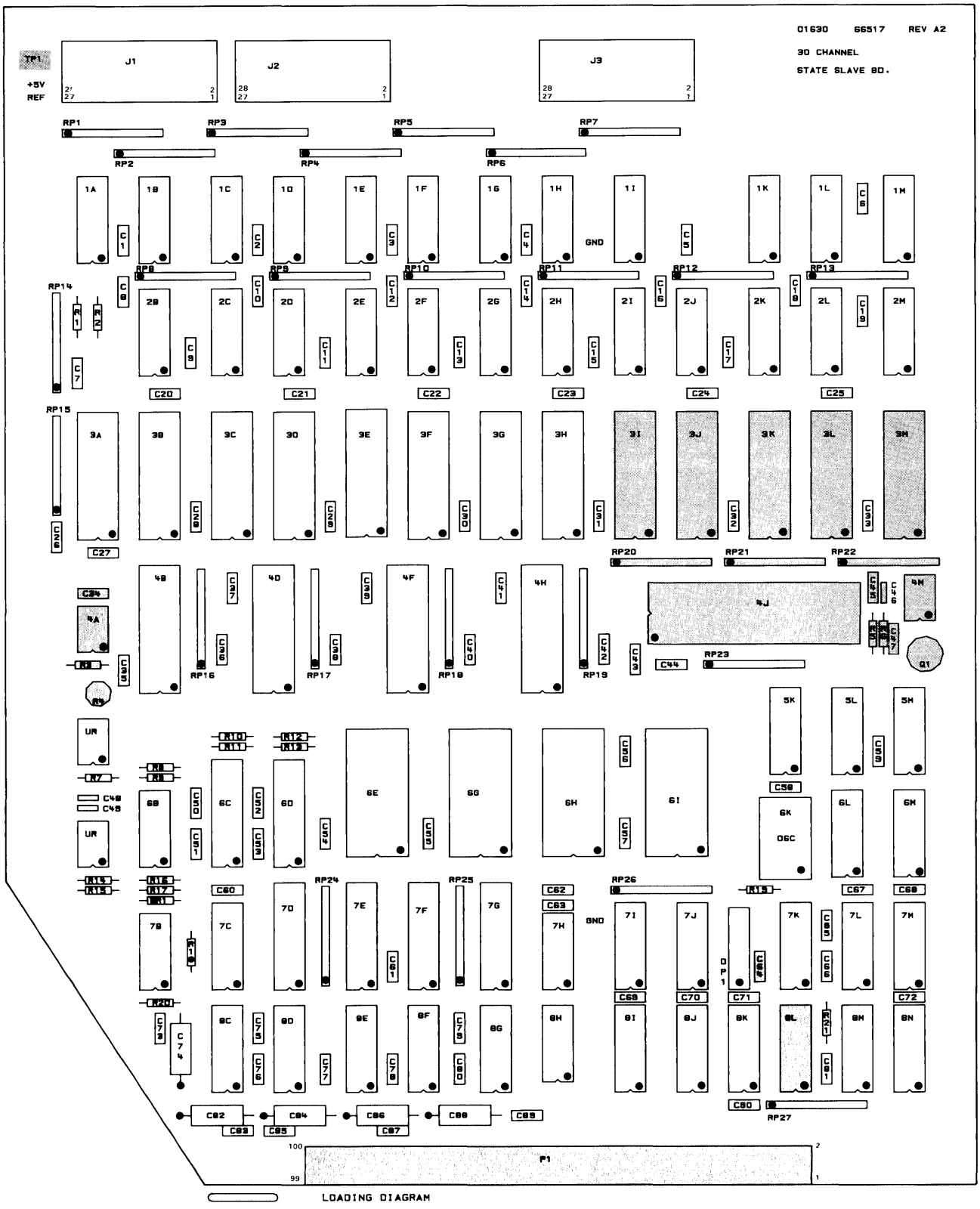
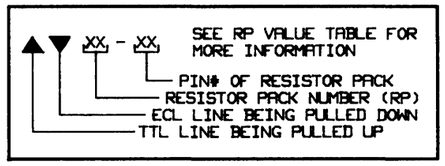


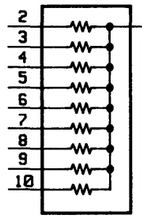
Figure 8F-3. State Slave Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:





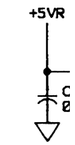
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

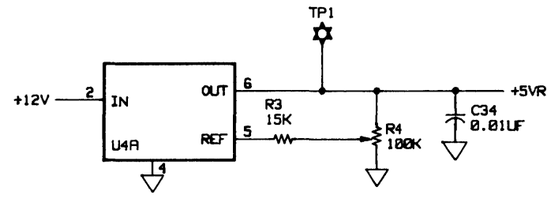
C1-47,54-65,67-90 P/O P1 Q1 R3-6 RP20-22 U3I-3M,4A,4J,4M U8L	

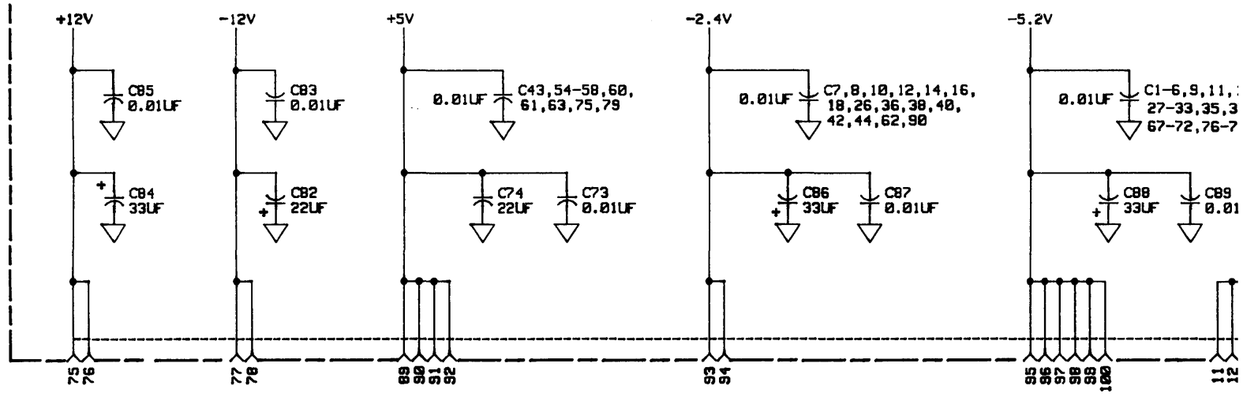
GREY CODE COUNTER AND MEMORY

-3.25 VOLT POWER SUPPLY



+5V REFERENCE SUPPLY





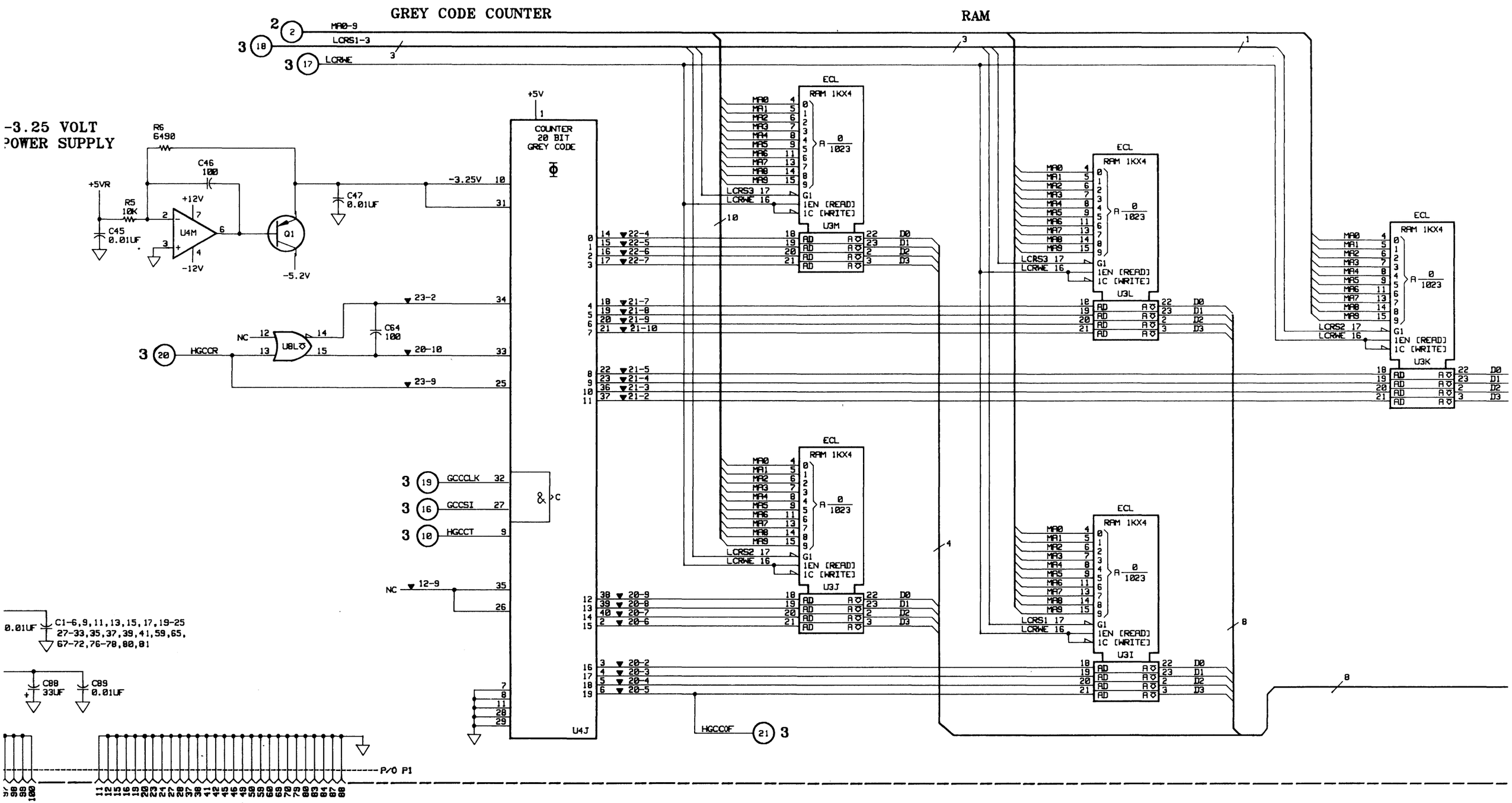
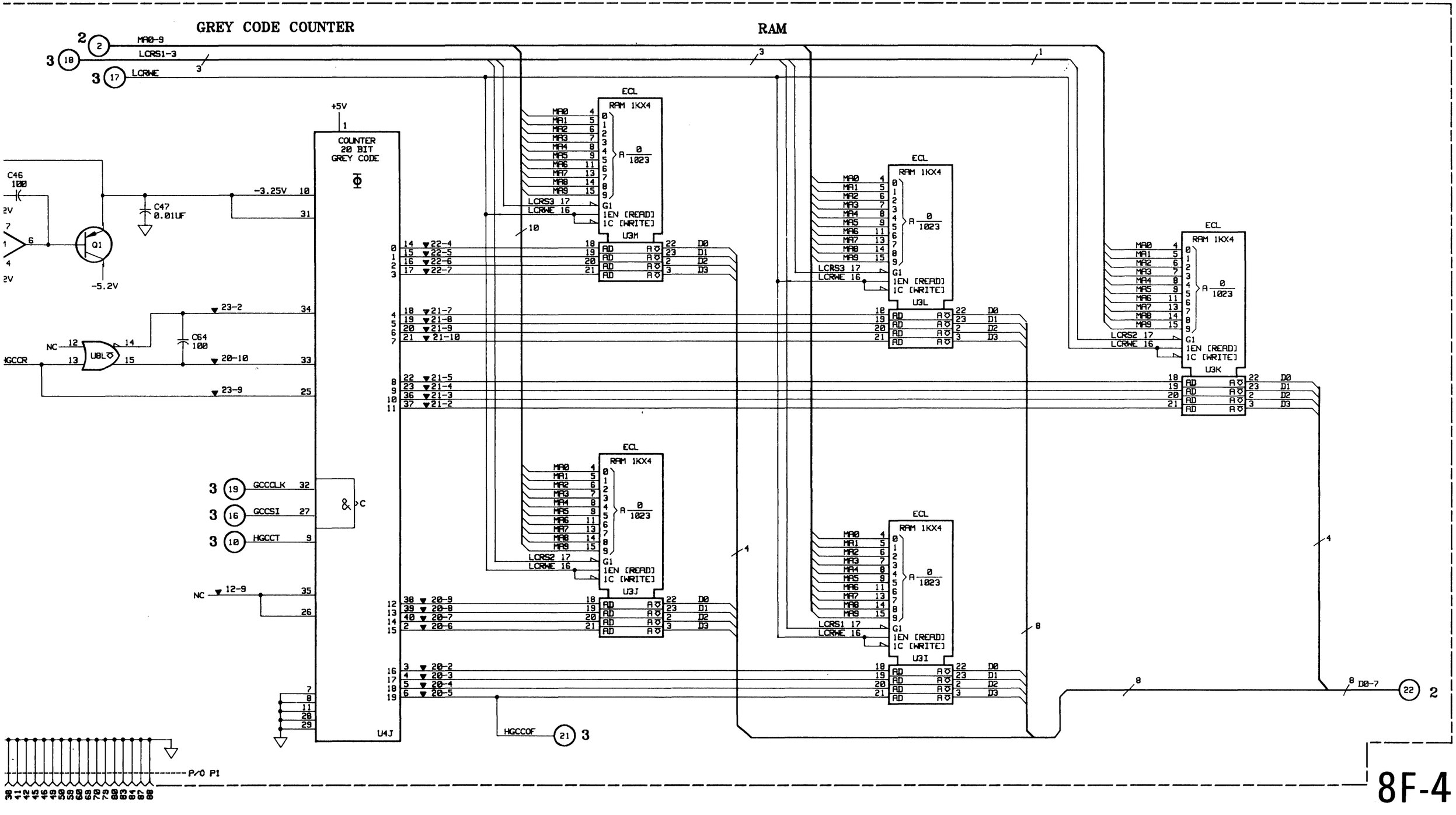


Figure 8F-4. Sto



8F-4

Figure 8F-4. State Slave Schematic (4 of 5)

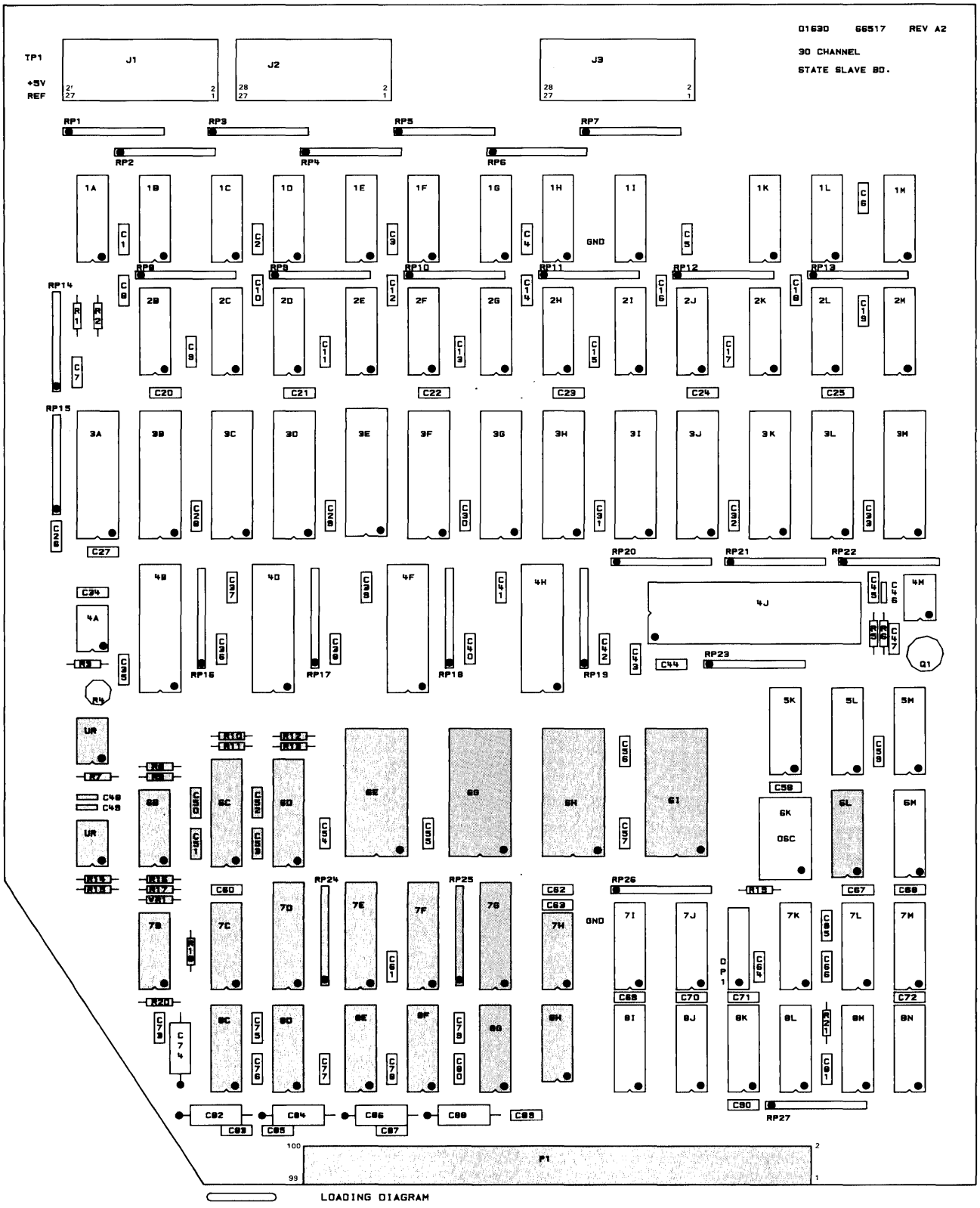
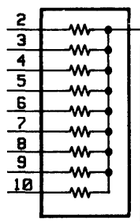


Figure 8F-3. State Slave Board Component Locator

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

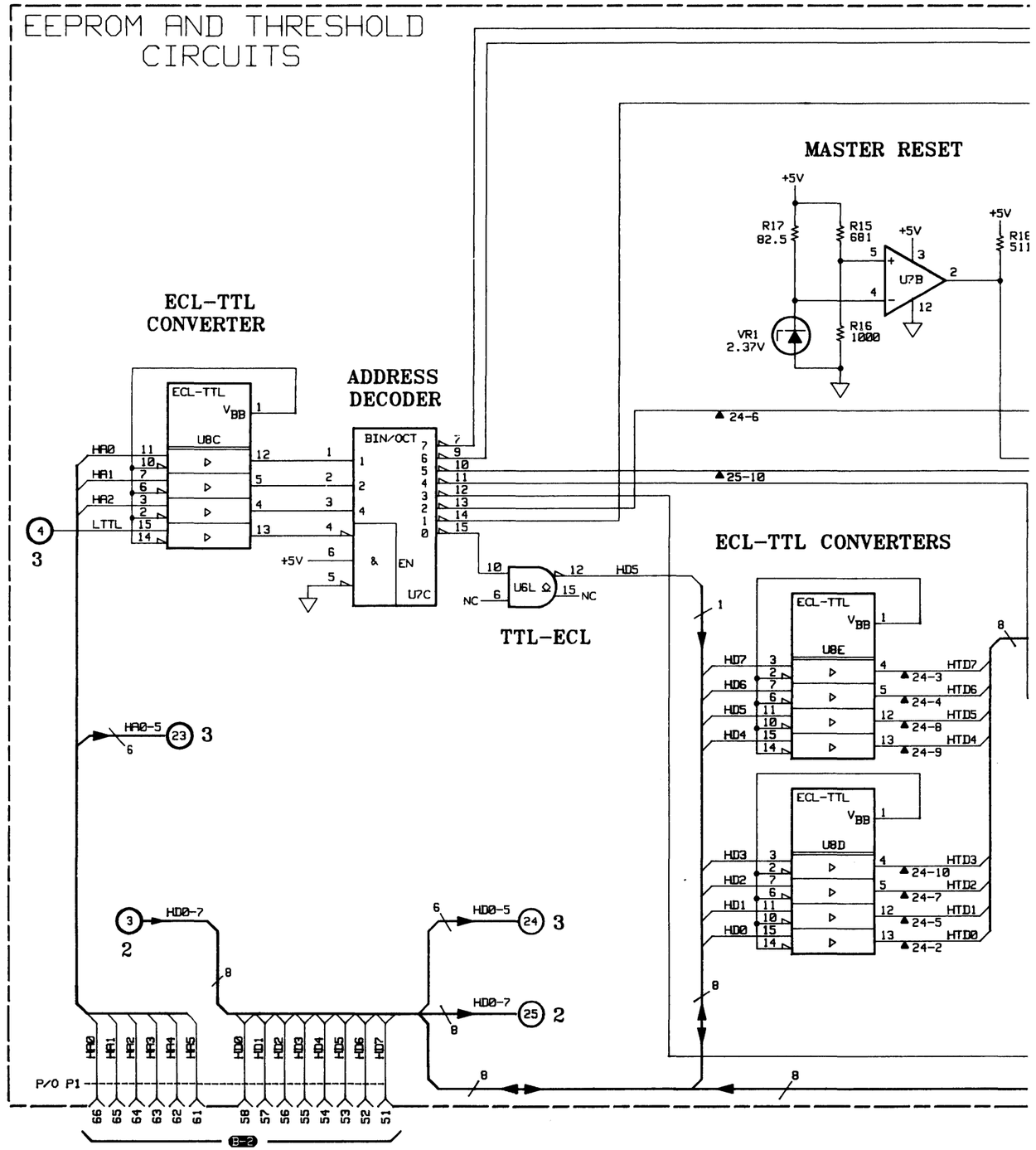
RESISTOR PACK DESCRIPTIONS:



RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

C48-53 P/O P1 R7-17 RP24,25 U6B-I,6L,7B-H,8C-H, UR5A,6A VR1	



THRESHOLD DACS

ELECTRICALLY ERASABLE PROM

ADDRESS COUNTER

CONTROL LATCH

INVERTER

DATA LATCH

OUTPUT DATA BUFFER

TTL-ECL CONVERTORS

Figure 8F-4. St

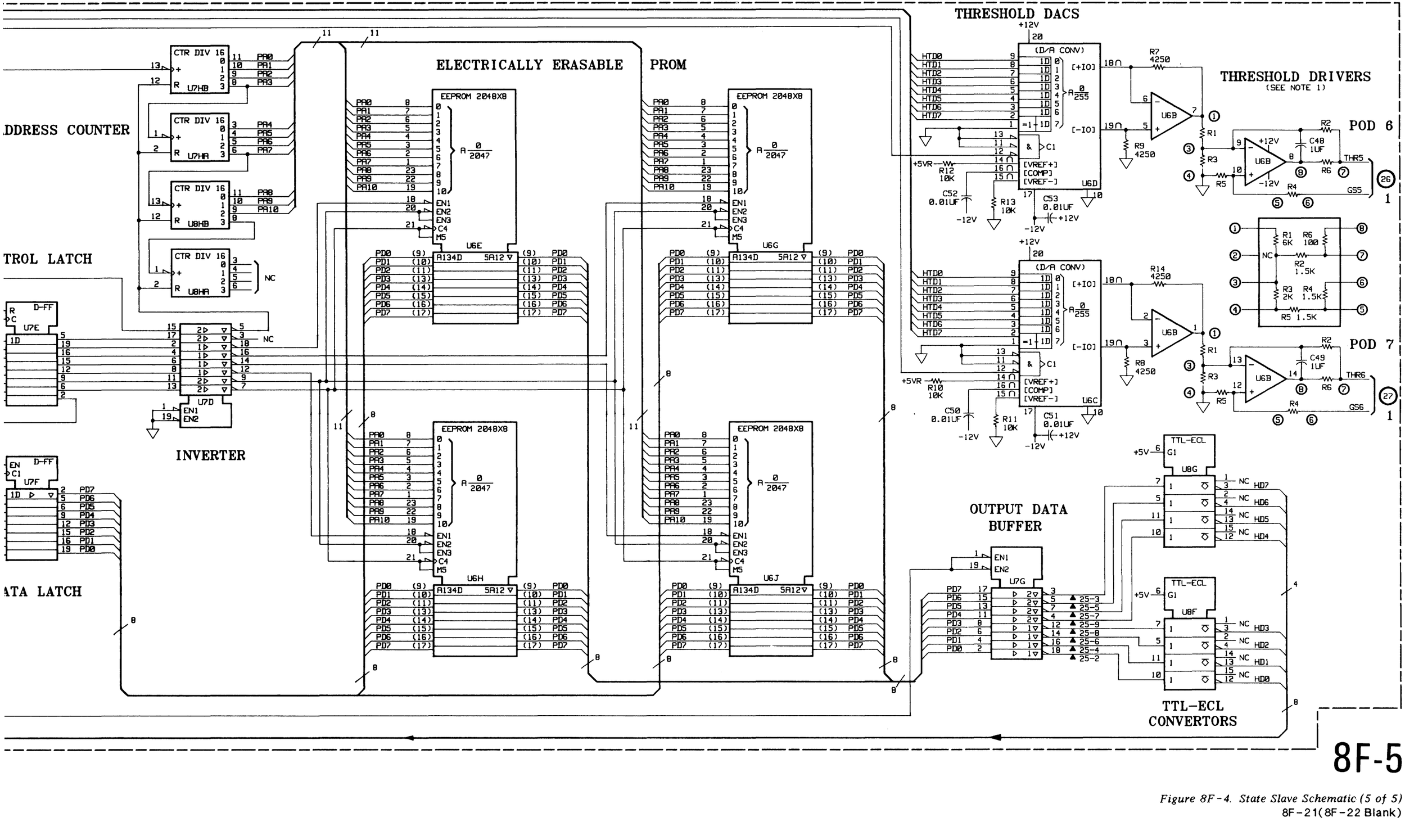


Figure 8F-4. State Slave Schematic (5 of 5)

APPENDIX A
1630A/D
REPAIR AND VERIFICATION PROCEDURES

A-1. INTRODUCTION

This section consists of the Operation, Guided Probe, and Calibration tests that are downloaded into the 1630A/D via a controller. Operation Verification tests determine which subsystem is faulty (CPU or Acquisition). Guided Probe tests determine which node is bad in the faulty subsystem. The remaining tests are used for Timing and State calibration adjustments in Section V (Adjustments) of this manual. Note that all tests are stored on one tape and are written in BASIC.

Note: For complete Performance Testing of the 1630A/D, perform the Operation Verification Tests in this Appendix, the Parametric Verification Tests in the ET19776 Manual, and the Timing and State calibration adjustments in Section V of this manual.

A-2. GUIDED PROBE TROUBLESHOOTING - GENERAL INFORMATION

The main program allows either Operation Verification or Guided Probing on the subsystem level. System verification is accomplished by executing Operation Verification tests on the CPU and Acquisition subsystems. In the Operation Verification mode, the actual tests are downloaded into the 1630A/D under test over HP-IB from the controller. The controller then instructs the 1630A/D to begin execution of the Operation Verification tests (a single pass or continuous execution can be specified). If a failure is encountered, the program displays the test number that failed. At this point, the System-Level Guided Probe program should be run to assist in determining the actual board that failed.

Once a failure is isolated to a board, then the Single Board Guided Probe function is selected. The board in question is loaded into the 1630A/D's service slot, a right angle connector on the top end of the motherboard. (NOTE: A fan must be used to keep air moving across the PC boards that are under test in the service slot.) Then the functional tests are downloaded into the 1630A/D and run until the hard failure is isolated. The particular test that failed automatically keeps executing, the program references signature databases (additional files on the tape) and indicates where to begin probing. Both the topology of the board and nodal information are contained in the signature database files. The controller steps through the database, comparing the actual signatures measured with the information found in the database.

If a bad node is found, the program prompts the user to begin checking all related inputs. If one of those inputs is found to be bad, the program will "re-define" the current bad node and continue checking all related inputs for the most recent bad node. When all inputs are determined to be good, the bad node has been isolated. At this point, as with standard signature analysis, the actual part must be isolated since either a driver or receiver could be at fault. If the node includes wired-ORs, then a current tracer and possibly a logic pulser can be used to isolate the failed part.

Provisions are also made in the probing program to determine if the failure includes a group of ICs. This may occur, for example, if a feedback loop has not been broken in the design implementation of signature analysis. In this case, the controller will indicate all inputs to the component group; then the actual bad component in the group must be determined by conventional troubleshooting methods.

A-3. 1630A/D PROGRAM TAPE LOADING PROCEDURE

After referring to the desired hardware configuration procedure (Operation, Guided Probe, or calibration), use the following procedure to load and run tests from the controller.

a. Turn OFF the 1630A/D under test.

b. Set the 1630A/D rear panel address switches (1-8) to "00000001".

c. Turn ON the 1630A/D. The System Specification menu should be displayed.

d. Turn OFF the controller and insert the 1630A/D Program Tape.

e. Turn ON the controller. Note that upon power-up the controller will look for a program named "Autost" which will be automatically loaded into memory and executed.

f. The following softkeys should appear on the controller. If they don't, repeat the procedure.

SOFTKEY	TEST	TEST USE
< ACQvfy>	Acquisition subsystem	Operation Verification
< CPUvfy>	CPU subsystem	Operation Verification
< Keybrd >	Keyboard test pattern	Operation Verification
< Probe > *	Guided Probe	Troubleshooting
< Disply >	Display test pattern	Adjustment
< Strobe >	State board strobe	Adjustment

* If the < Probe > test is chosen, refer to the Guided Probe Hardware Configuration procedure.

g. Select the desired test.

A-4. OPERATION VERIFICATION HARDWARE CONFIGURATION

This section is concerned with the hardware configuration necessary to execute any of the calibration or subsystem tests. See Guided Probe Hardware Configuration for information about configuring the hardware for Guided Probe Troubleshooting. The hardware required is as follows:

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. One 1630A or D (unit under test).

The hardware configuration is as follows:

a. Connect the HP-IB cable from the controller to the 1630A/D.

b. Follow the 1630A/D Program Tape Loading Procedure.

A-5. RUNNING THE OPERATION VERIFICATION TESTS

After loading the Program Tape, the following tests should be executed in order to determine if a subsystem is operating properly. If a test should fail then Guided Probe should be used to find the faulty node.

TEST	
< ACQvfy >	This test determines if the acquisition portion of the 1630A/D is faulty.
< CPUvfy >	This test determines if the CPU board is faulty.
< Keybrd >	This test displays a keyboard test pattern on the 1630A/D display. Refer to the Keyboard Test Procedure in Section IV (Performance Tests).

A-6. ACQUISITION VERIFICATION; TEST #9, FAILURES

Test 9 of the Acquisition Verification checks the Trigger Duration circuitry on the Timing Master board. To troubleshoot this section of circuitry, first ensure that the 1630 passes Acquisition Verification tests 1 to 8.

When Test 9 fails, an 8-bit failure code is displayed. By interpreting this failure code, the failure area of the trigger duration circuit may be isolated. The bits of this code correspond as follows:

BIT	Test
00000001	1 us
00000010	10 us
00000100	20 us
00001000	50 us
00010000	100 us
00100000	200 us

The following resistor and capacitor combinations are used for these tests.

Test	Resistor(s)	Capacitor(s)
1 us	1.58 K	300 pF, 3600 pF
10 us	1.58 K,	300 pF, .04 uF
20 us	1.58 K, 1.71 K, 681	300 pF, .4 uF
50 us	1.58 K, 1.71 K	300 pF, .4 uF
100 us	1.58 K,	300 pF, .4 uF
200 us	1.58 K, 1.71 K, 681	300 pF, 4 uF

R1 = 681, R2 = 1.71 K, R3 = 1.58 K
C4 = 4 uF, C5 = .4 uF, C6 = .04 uF, C7 = 3600 pF, C9 = 300 pF

NOTE: The 200 MHz oscillator on the Timing Master board is used as a time base for these tests. A failure code of 00111111 may be due to a failure of this oscillator.

Signatures can be taken for some of the digital ICs in this circuit. To generate stimulus for this signature analysis, use Guided Probe for the Timing Master board, Test #6. This will automatically set up the 5005B signature analyzer. Take signatures at the following points without additional prompting from the software:

U5I:	pin 12	0097	U4C:	pin 2	8P7A
	pin 13	F2AA		pin 3	8P7A
	pin 14	FA32		pin 4	8P7A
	pin 15	P719		pin 9	8A4U
				pin 13	8P7A
U2D	pin 7	P719		pin 14	0000
	pin 14	6963		pin 15	0000

A-7. GUIDED PROBE HARDWARE CONFIGURATION

The hardware necessary to execute Guided Probe Troubleshooting is as follows:

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. One HP 5005B Signature Multimeter.

d. One additional HP-IB cable (10833A). This cable connects the HP 5005B to the 1630A/D under test.

e. One 1630A or D (unit under test).

The hardware configuration is as follows:

a. Connect the HP-IB cable from the controller to the 1630A/D under test.

b. Connect the additional HP-IB cable from the 1630A/D to the 5005B.

c. Set the 5005B HP-IB address switches for "ADDRESSABLE" and select a unique address on the HP-IB bus.

d. Refer to the 1630A/D Program Tape Loading Procedure.

A-8. RUNNING THE GUIDED PROBE TESTS

After selecting the < Probe > softkey the controller will execute the Guided Probe program. The user will then be asked the level of troubleshooting - System or Board Level. The program will then direct the user through a troubleshooting procedure.

a. Select the softkey labeled < Probe > on the controller. Remember, always read the entire screen before proceeding.

b. The user is then asked which level to troubleshoot - System Level or board level. Select System Level unless it is known that a particular board is at fault.

c. The system level program may direct the user to a particular board at fault. If so, the program will prompt the user for the board part number and direct them to load a Data Base Tape for that board.

d. If the testing leads to a "special case node", then reference to appendix C in this manual. Remember, always read the entire screen.

A-9. CALIBRATION TEST HARDWARE CONFIGURATION

This section is concerned with the hardware configuration necessary to execute the programs necessary to do Timing and State calibration adjustments. The Calibration Hardware Configuration is the same as the Operation Verification Hardware Configuration.

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. One 1630A or D (unit under test).

The hardware configuration necessary is as follows:

a. Connect an HP-IB cable from the controller to the 1630A/D.

b. Follow the 1630A/D Program Tape Loading Procedure.

A-10. RUNNING THE CALIBRATION TESTS

After loading the Program Tape the following tests should be executed as directed in Section V (Adjustments) of this manual.

TEST	
< Disply >	Loads a display test pattern on the 1630A/D CRT for adjusting the Display Driver board.
< Strobe >	Strobes the State board for adjusting pulse width and delay.

A-11. 1630A/D TROUBLESHOOTING SUMMARY

The following flow chart and text summarizes troubleshooting of the 1630A and D.

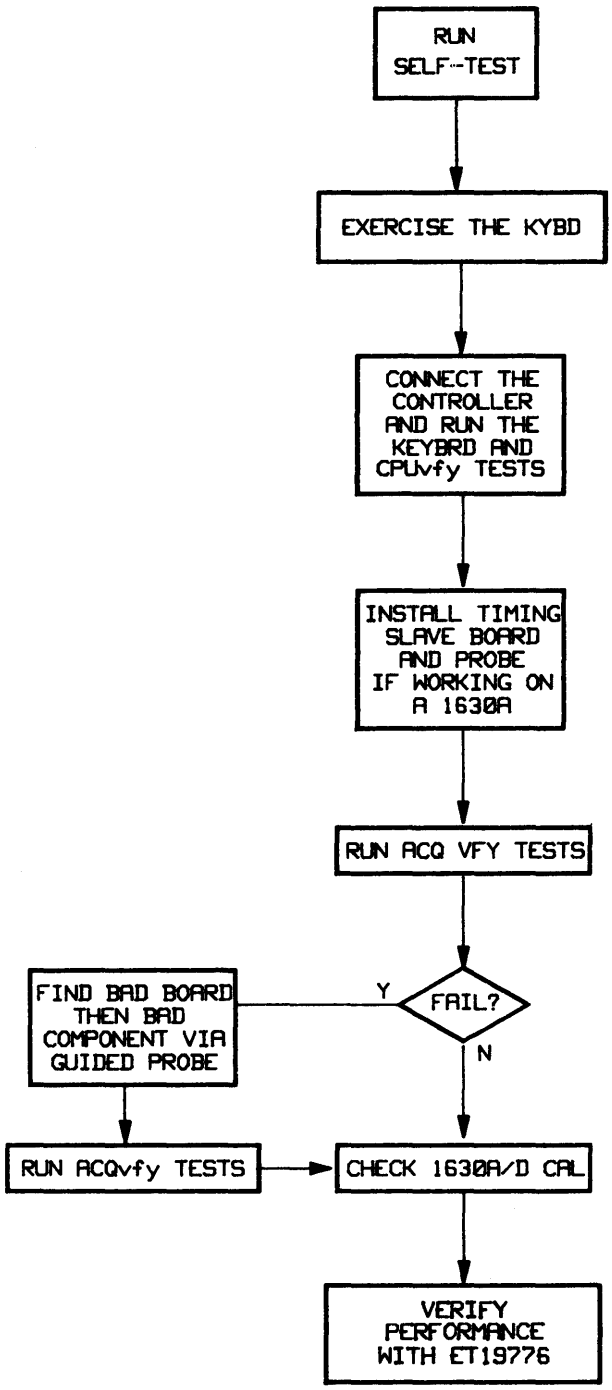


Figure A-1. 1630A/D Troubleshooting Flow Chart.

a. RUN SELF-TEST This is described in Section IV, paragraph 4-3.

b. EXERCISE THE KEYBOARD

1. If the State Format Specification is displayed on the 1630A/D, then the threshold levels of the pods can be tested for "stuck at" faults in the following manner:

   Select a pod then change the threshold level from TTL to ECL or vice-versa. If a line does not show a change in activity level, then it is stuck and should be checked. The pin could possibly be bent.

2. Do a Timing Trace. If the 1630A/D prompts you, "Waiting for timing trigger", then check the 200 MHz oscillator; it may have failed.

c. CONNECT THE CONTROLLER... This is described in part A-4 of this appendix.

d. INSTALL TIMING SLAVE... Install a Timing Slave board and probe into a 1630A to convert it to a 1630D for further testing.

e. RUN < ACQvfy > TESTS. These are explained in part A-5 ofthis appendix.

f. Guided Probe. This is explained in part A-8 of this appendix.

g. CHECK 1630A/D CAL. Calibration procedures are explained in part A-10 of thi appendix.

h. VERIFY PERFORMANCE... See Section III of the Operating and Service manual for the ET19776 1630A/D Test Tool.

Appendix B Table of Contents

List of Illustrations

NOTES

APPENDIX B
1630G
REPAIR AND VERIFICATION PROCEDURES

B-1. INTRODUCTION

This section consists of the Operation, Guided Probe, and Calibration tests that are downloaded into the 1630G from a controller. Operation Verification tests determine which subsystem is faulty (CPU or Acquisition). Guided Probe tests determine which node is bad in the faulty subsystem. The remaining tests are used for Timing and State calibration adjustments in Section V (Adjustments) of this manual. Note that all tests are stored on one tape and are written in BASIC.

Note: For complete Performance Testing of the 1630G, perform the Operation Verification Tests in this Appendix, the Parametric Verification Tests in the ET19776 Manual, and the Timing and State calibration adjustments in Section V of this manual.

B-2. GUIDED PROBE TROUBLESHOOTING - GENERAL INFORMATION

The main program allows either Operation Verification or Guided Probing on the subsystem level. System verification is accomplished by executing Operation Verification tests on the CPU and Acquisition subsystems. In the Operation Verification mode, the actual tests are downloaded into the 1630G under test over HP-IB from the controller. The controller then instructs the 1630G to begin execution of the Operation Verification tests (a single pass or continuous execution can be specified). If a failure is encountered, the program displays the test number that failed. At this point, the System-Level Guided Probe program should be run to assist in determining the actual board that failed.

Once a failure is isolated to a board, then the Single Board Guided Probe function is selected. The board in question is loaded into the 1630G's service slot, a right angle connector on the top end of the motherboard. (NOTE: A fan must be used to keep air moving across the PC boards that are under test in the service slot.) Then the functional tests are downloaded into the 1630G and run until the hard failure is isolated. The particular test that failed automatically keeps executing, the program references signature databases (additional files on the tape) and indicates where to begin probing. Both the topology of the board and nodal information are contained in the signature database files. The controller steps through the database, comparing the actual signatures measured with the information found in the database.

If a bad node is found, the program prompts the user to begin checking all related inputs. If one of those inputs is found to be bad, the program will "re-define" the current bad node and continue checking all related inputs for the most recent bad node. When all inputs are determined to be good, the bad node has been isolated. At this point, as with standard signature analysis, the actual part must be isolated since either a driver or receiver could be at fault. If the node includes wired-ORs, then a current tracer and possibly a logic pulser can be used to isolate the failed part.

Provisions are also made in the probing program to determine if the failure includes a group of ICs. This may occur, for example, if a feedback loop has not been broken in the design implementation of signature analysis. In this case, the controller will indicate all inputs to the component group; then the actual bad component in the group must be determined by conventional troubleshooting methods.

B-3. 1630G REPAIR PROCEDURES OVERVIEW

The 1630G and 1630A/D differ mainly with respect to the available number of data channels. This fact simplifies the test software requirements for the 1630G. It enables the use of existing 1630A/D service software by first checking the Keyboard Verification and then the CPU Verification. The 1630G is then converted to a 1630D to run the Acquisition Verification tests. The conversion is straightforward and is accomplished by replacing the State Slave board of the 1630G with a Timing Slave board. This board is supplied with the K01 Self-Support package. After testing the instrument as a 1630D it is converted back to a 1630G and the State Slave board is tested using new 1630G software.

B-4. 1630G PROGRAM TAPE LOADING PROCEDURE

The following is a general procedure for loading a tape and running tests on the 1630G with a controller. However, the proper hardware configuration must be set up first.

a. Turn OFF the 1630G under test.

b. Set the 1630G rear panel address switches (1-8) to "00000001".

c. If an Acquisition test from the Operation Verification program is being made, replace the State Slave board and probes of the 1630G with the Timing Slave board and probe from the K01 kit.

d. Turn ON the 1630G. The System Specification menu should be displayed.

e. Turn OFF the controller and insert the 1630G Program Tape.

f. Turn ON the controller. The wait should be a few seconds for the controller to automatically load the tape. If not, try LOAD"AUTOST".

g. The following softkeys should appear on the controller. If they don't, repeat the procedure.

SOFTKEY	TEST	TEST USE
< ACQvfy>	Acquisition subsystem	Operation Verification
< CPUvfy>	CPU subsystem	Operation Verification
< Keybrd >	Keyboard test pattern	Operation Verification
< G-PROBE >	Guided Probe	Troubleshooting
< Disply >	Display test pattern	Adjustment
< Strobe >	State board strobe	Adjustment

g. Select the desired test.

B-5. OPERATION VERIFICATION HARDWARE CONFIGURATION

This section deals with the hardware and hardware configuration necessary to run calibration and subsystem testing. (Guided Probe troubleshooting requires a different configuration. See paragraph B-8.) The hardware requirements are:

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. One 1630A or D (unit under test).

d. Timing Slave board (from K01 package).

e. Timing Probe (from K01 package).

The hardware configuration is as follows:

a. Be sure the I/O ROM and ROM drawer are in the HP85.

b. Connect the HP-IB cable from the controller to the 1630G.

c. Follow section B-4 procedure.

d. Follow section B-6 procedure.

B-6. RUNNING OPERATION VERIFICATION TESTS

This section describes the chronology of the Operation Verification tests. If any test should fail, the Guided Probe testing should be used to find the fault.

TEST	
< ACQvfy >	This test should be conducted on a 1630G after it has been converted to a 1630D. It tests operation of the Acquisition Subsystem.
< CPUvfy >	This test determines if the CPU board is faulty.
< Keybrd >	This test displays a keyboard test pattern on the 1630G display. Refer to the Keyboard Test Procedure in Section IV (Performance Tests).

B-7. ACQUISITION VERIFICATION; TEST #9, FAILURES

Test 9 of the Acquisition Verification checks the Trigger Duration circuitry on the Timing Master board. To troubleshoot this section of circuitry, first ensure that the 1630 passes Acquisition Verification tests 1 to 8.

When Test 9 fails, an 8-bit failure code is displayed. By interpreting this failure code, the failure area of the trigger duration circuit may be isolated. The bits of this code correspond as follows:

BIT	Test
00000001	1 us
00000010	10 us
00000100	20 us
00001000	50 us
00010000	100 us
00100000	200 us

The following resistor and capacitor combinations are used for these tests.

Test	Resistor(s)	Capacitor(s)
1 us	1.58 K	300 pF, 3600 pF
10 us	1.58 K,	300 pF, .04 uF
20 us	1.58 K, 1.71 K, 681	300 pF, .4 uF
50 us	1.58 K, 1.71 K	300 pF, .4 uF
100 us	1.58 K,	300 pF, .4 uF
200 us	1.58 K, 1.71 K, 681	300 pF, 4 uF

R1 = 681, R2 = 1.71 K, R3 = 1.58 K
C4 = 4 uF, C5 = .4 uF, C6 = .04 uF, C7 = 3600 pF, C9 = 300 pF

NOTE: The 200 MHz oscillator on the Timing Master board is used as a time base for these tests. A failure code of 00111111 may be due to a failure of this oscillator.

Signatures can be taken for some of the digital ICs in this circuit. To generate stimulus for this signature analysis, use Guided Probe for the Timing Master board, Test #6. This will automatically set up the 5005B signature analyzer. Take signatures at the following points without additional prompting from the software:

U5I:	pin 12	0097	U4C:	pin 2	8P7A
	pin 13	F2AA		pin 3	8P7A
	pin 14	FA32		pin 4	8P7A
	pin 15	P719		pin 9	8A4U
				pin 13	8P7A
U2D	pin 7	P719		pin 14	0000
	pin 14	6963		pin 15	0000

B-8. GUIDED PROBE HARDWARE CONFIGURATION

This paragraph describes the hardware and hardware configuration necessary to run Guided Probe Troubleshooting on the 1630G. The hardware necessary is as follows:

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. HP 5005B Signature Multimeter.

d. Additional HP-IB cable (10833A).

e. 1630G (unit under test).

The hardware configuration is as follows:

a. Connect one HP-IB cable between the controller and the 1630G under test.

b. Connect the other HP-IB cable from the 1630G to the HP5005B.

c. Set the HP5005B HP-IB address switches for "ADDRESSABLE" and select a unique address on the HP-IB bus.

d. Refer to paragraph B-4 for program tape loading instructions.

B-9. RUNNING THE GUIDED PROBE TESTS

The following describes how to use the Guided Probe program.

a. Select the softkey labeled <G-PROBE> on the controller. Remember, always read the entire screen before proceeding.

b. The user is then asked which level to troubleshoot - system level or board level. Select system level unless it is known that a particular board is at fault.

c. The system level program may direct the user to a particular board at fault. If so, the program will prompt the user for the board part number and direct them to load a Data Base Tape for that board.

d. If the testing leads to a "special case node", then refer to appendix C in this manual. Remember, always read the entire screen.

B-10. STATE SLAVE BOARD TESTING

The following deals with the testing of the State Slave board in the 1630G. After completing the Keyboard, CPU, and Acquisition tests with the 1630G set up as a 1630D, the instrument is converted back to a 1630G and the State Slave board and probes are tested with the following procedure.

a. Make sure the instrument is configured as a 1630G. (State Slave board and pods installed.)

b. Turn the 1630G ON. The System Specification menu should be displayed.

c. Turn the controller OFF and insert the 1630G program tape.

d. Turn on the controller. The wait may be a few seconds, but the controller should automatically load the program. If it does not, type in LOAD"AUTOST".

e. The program will now test the State Slave board. If a failure is isolated it will be noted on the screen of the controller. Be sure to read the entire screen for prompts and such.

B-11. CALIBRATION TEST HARDWARE CONFIGURATION

The following describes the hardware and hardware configuration necessary for state and timing adjustments.

Hardware requirements.

a. One HP 85F which includes an HP-IB Interface, a 82936A ROM Drawer, and a I/O ROM.

b. One 82903A 16K Memory Module.

c. One 1630G (unit under test).

The hardware configuration is as follows:

a. Connect the HP-IB cable from the controller to the 1630G.

b. Follow the Program Tape Loading Procedure in paragraph B-4.

B-12. RUNNING THE CALIBRATION TESTS

After loading the Program Tape the following tests should be executed as directed in Section V (Adjustments) of this manual.

TEST	DESCRIPTION
< Disply >	Loads a display test pattern on the 1630G CRT for adjusting the Display Driver board.
< Strobe >	Strobes the State board for adjusting pulse width and delay. The parameters are displayed on the screen.

B-13. 1630G TROUBLESHOOTING SUMMARY

The following flow chart and text summarizes troubleshooting of the 1630G.

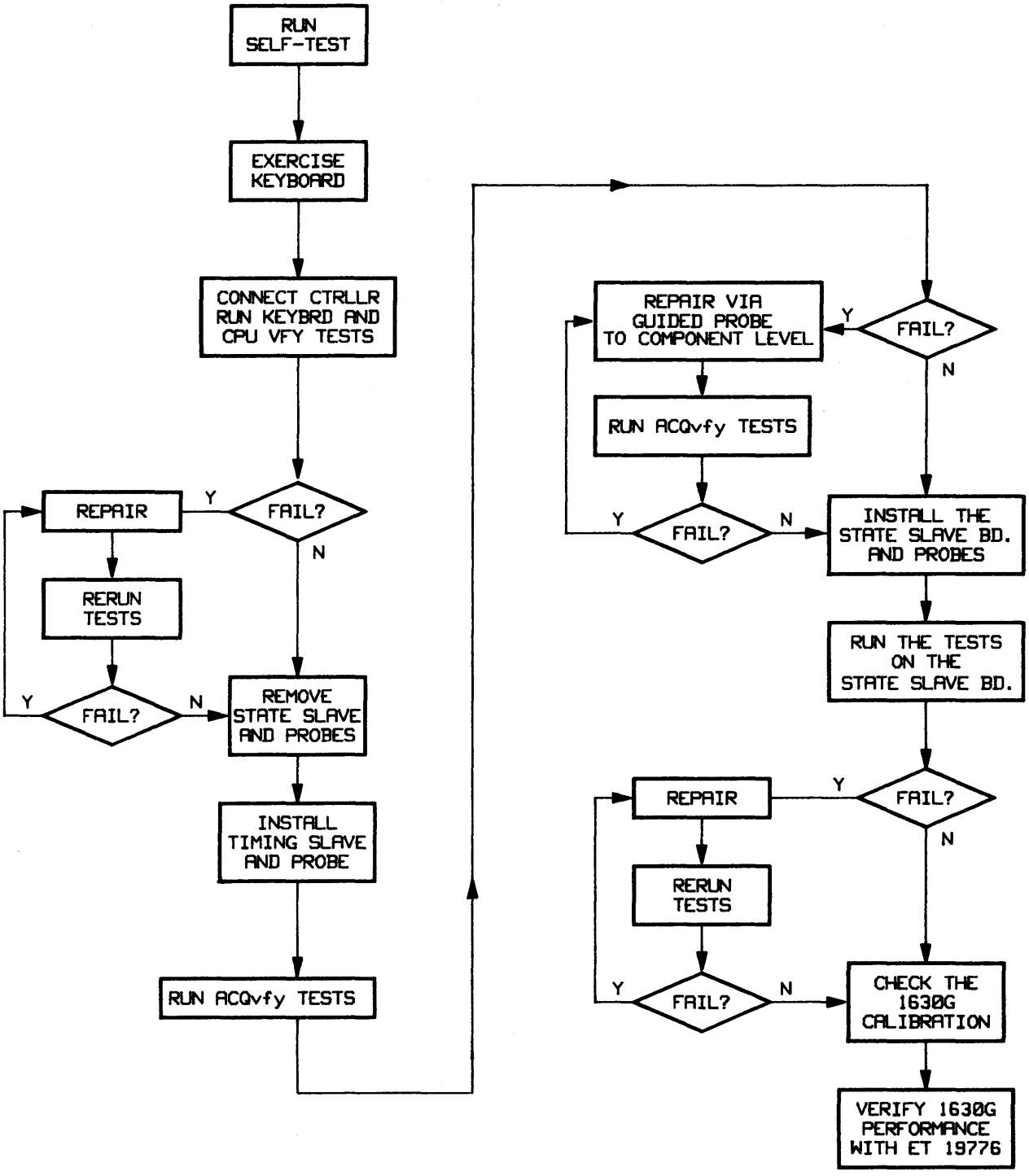


Figure B-1. 1630G Troubleshooting Flow Chart.

a. RUN SELF-TEST. This is described in Section IV, paragraph 4-3.

b. EXERCISE THE KEYBOARD.

1. If the State Format Specification is displayed on the 1630G, then the threshold levels of the pods can be tested for "stuck at" faults in the following manner:

   Select a pod then change the threshold level from TTL to ECL or vice-versa. If a line does not show a change in activity level, then it is stuck and should be checked. The pin could possibly be bent.

2. Do a Timing Trace. If the 1630G prompts you, "Waiting for timing trigger", then check the 200 MHz oscillator. It may not have self-started.

c. CONNECT THE CONTROLLER... This is described starting at B-4 of this appendix.

d. REMOVE STATE SLAVE..., INSTALL TIMING SLAVE... Install a Timing Slave board and probe into a 1630A to convert it to a 1630D for further testing.

e. RUN < ACQvfy > TESTS. These are explained at B-6 in this appendix.

f. Guided Probe. This is explained at B-9 in this appendix.

g. Test State Slave. This is explained at B-10 in this appendix.

h. CHECK 1630G CAL. Calibration procedures are explained starting at B-11 in this appendix.

i. VERIFY PERFORMANCE... See Section III of the Operating and Service manual for the ET19776 1630A/D Test Tool.

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APPENDIX C
1630A/D/G
SPECIAL CASE NODE TESTING

C-1. INTRODUCTION

This special case testing is for nodes that do not fit into the normal flow of guided probe testing. The operator of Guided Probe is prompted to make special measurements, while the tests are in progress in order to verify proper operation of the instrument under test.

C-2. SPECIAL CASE TESTING FOR STATE MASTER BOARDS

a. State Master board 01630-66505 uses tape 01630-90010.

b. State Master board 01630-66509 uses tape 01630-90026.

The following Special Case Nodes should be measured manually when prompted by the controller during a guided probe session. Use a 1726A on the fastest sweep speed to view narrow (less than 10 ns) pulses. Reply to the controller with PASS if the signal appears as described below.

A Small swing is about 200 mV each direction above and below Vbb (-1.3V) and a Narrow pulse is approximately 10 ns.

C-3. Special Case Nodes In All Tests

SPECIAL CASE NODES		SHOULD BE	MEASURE WITH
U1A,B,C: U1D,E,F: U1H,I,J:	pins 4,5,9, 10,12,13	NON ECL level signatures	5005B : set HI & LO signature thresholds to -1.5V
		Pins 4,9,&12 should read "C05A". Pins 5,10,13 should read "0000". (At threshold of -1.5H, -1.5L)	
U3M:	pin 5	Small swings @ -1.3V	SCOPE
	pin 6	Small swings @ -1.3V	SCOPE
	pin 9	-1.3V DC Voltage	DVM (5005B)
	pin 14,15	Narrow pulse in ALL tests	SCOPE
U5L:	pin 2	Narrow pulse in ALL tests	SCOPE
	pin 5	Narrow pulse in ALL tests	SCOPE
U5M:	pin 5	Small swings @ -1.3V	SCOPE
	pin 11	-1.3 DC Voltage	DVM (5005B)
	pin 12	Narrow ramp in ALL tests	SCOPE
	pin 13	Small swings @ -1.3V	SCOPE
	pin 15	Narrow pulse in ALL tests	SCOPE
U5N:	pin 9	Narrow pulse in ALL tests	SCOPE
U6J:	pin 2,3	Narrow pulse in ALL tests	SCOPE

C-4. Special Case Nodes ONLY In Test #4

SPECIAL CASE NODES		SHOULD BE	MEASURE WITH
U2B,C:	pin 2,3, 14,15	unstable in Test #4	NO SOLUTION
U2E-I:	pin 2,3, 14,15	unstable in Test #4	NO SOLUTION
U3A-I:	pin 2,3, 22,23	unstable in Test #4	NO SOLUTION
U6N:	pins 4,5,9 10,12,13	Alternate threshold	Manually set both 5005B thresholds to -1.5V.

Signatures for U6N should be:

U6N/4 -- H68C	U6N/9 -- 8HAU	U6N/12 -- UAC6
U6N/5 -- 47UC	U6N/10 - 1FHU	U6N/13 -- 6CF6

C-5. Special Case Nodes ONLY In Test #5

In Test #5 only, the following nodes will provide valid signatures, but in order for the node signal to be TOTALLY correct these narrow pulses (approximately 10 ns) must exist. Therefore, if one of these nodes occurs in a G.P. printout, verify the TOTAL accuracy of the node with a SCOPE by viewing the pulses.

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U2L: pin 2	Narrow pulses ~10nS	SCOPE
U3M: pin 3	"	"
U4K: pins 2,14,15	"	"
U5K: pins 3,6,14	"	"
U5M: pins 3,6	"	"
U5N: pins 2,3,14,15	"	"
U6K: pins 2,9,14	"	"
U7J: pins 14,15	"	"
U7K: pin 2	"	"
U7I: pins 2,3	"	"
U8J: pins 5,6,9,11 14,15	"	"
U8K: pins 2,3,4 12,13,14	"	"
U8L: pin 1,2,15	"	"

C-6. SPECIAL CASE TESTING FOR TIMING MASTER BOARDS

a. For Timing Master board 01630-66506 use tape 01630-90011.

b. For Timing Master board 01630-66510 use tape 01630-90027.

The following Special Case Nodes should be measured manually when prompted by the controller during a guided probe session. Use a 1726A on the fastest sweep speed to view narrow (less than 10 ns) pulses. Reply to the controller with PASS if the signal appears as described below.

A Small swing is about 200 mV each direction above and below Vbb (-1.3V) and a Narrow pulse is approximately 10 ns.

C-7. Special Case Nodes Only For Timing Master Board 01630-66506

a. U8F/47 is listed as a special case node in the data base, but it is NOT. When asked for user input, probe the node and read the signature.

   If SIG = 4H94 the node passes.
   If SIG ≠ 4H94 the node fails.

b. An error has been found in the 01630-66506 data base. U4G is not properly stored on the data base tape. When instructed to probe U4G/7, the operator should also manually probe U4G/6. The following are the stable signatures for each test:

TEST #	SIGNATURE AT U4G/7
1	151C
2	F4F2
3	PU59
4	1525
5	HU12
6	CF02
7	0H2P
8	48H2

C-8. Special Case Nodes In ALL Tests

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U8C: pin 3	200 MHz	SCOPE
pin 11	100 MHz	"
pin 12	40 MHz	"
pin 13	20 MHz	"
pin 14	10 MHz	"
U8D: pin 3	100 MHz	SCOPE
pin 4	200 MHz	"
pin 11	50 MHz	"
pin 12	20 MHz	"
pin 13	10 MHz	"
pin 14		
U4E: pin 10	-1.3V	DVM
pin 11	-1.3V	"
U2D: pin 5	-1.3V	DVM
pin 11	-1.3V	"
pin 12	-1.3V	"
pin 10	small swings	SCOPE

C-9. Special Case Nodes ONLY In Test #5

The following nodes will provide valid signatures, but in order for the node signal to be TOTALLY correct these narrow pulses must exist. Therefore, if one of these nodes occurs in a G.P. printout, verify the TOTAL accuracy of the node with a SCOPE by viewing the pulses.

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U8C: pin 3	200 MHz	SCOPE
P1: pin 22	Narrow pulses ~10nS	SCOPE
pin 26	"	"
U9H: pin 3	"	"
pin 14	"	"
pin 15	"	"
U3E: pin 3	"	"
U5I: pin 3	"	"

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APPENDIX D
1630A/D/G
RETROFIT INSTRUCTIONS

D-1. INTRODUCTION

Any 1630A/D Logic Analyzer can be converted to a 1630G using the 1630G Retrofit Kit, P/N HP 10340A. This retrofit can be performed by the customer or by the local HP Sales and Service Center.

Hewlett-Packard recommends conversion by experienced service personnel. Any damages to the instrument caused by the customer attempting the conversion can not be covered under warranty.

D-2. PARTS LIST

The HP 10340A Retrofit Kit consists of the following parts:

Rear Panel
Top Cover
Rear Casting
Rear Door
State Slave Board
1630G PROM SET
Accessary Pouch
1630G Operating Manual
1630G Front Panel Label
Rear Cover Label
Installation Instructions
10273A 10-Channel State Data Probe (Qty 3)

NOTE: The part numbers of these parts may change from time to time so they are not listed here. Contact an HP sales and service office for further information.

D-3. INSTALLATION INSTRUCTIONS

These instructions are divided according to the serial prefix of the 1630A/D. Use the instructions that apply to the instrument being converted.

D-4. Instruments With Serial Prefix 2234A and 2242A

1) Remove rear feet.

2) Remove bottom cover.

3) Disconnect two cables at the front of the CPU board (bottom board in the instrument).

4) Remove rear door.

5) Disconnect Acquisition probes.

6) Remove rear casting.

7) Remove two screws beneath HP-IB connector.

8) Remove CPU Board.

9) Remove the eight program ROMs from the sockets in the center of the board.

10) Install the eight program ROMs from the retrofit kit. Figure 1 shows the proper order of installation.

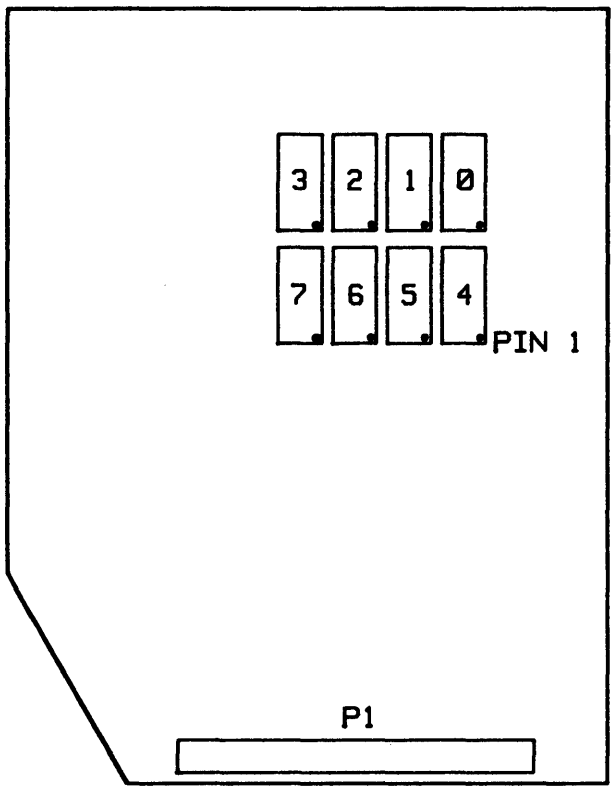

Figure D-1. PROM Locations

11) With a small piece of wire, connect pins 25 and 26 together on U6M.

12) Remove the remaining boards in the card cage.

13) Remove the top cover.

14) Remove the rear panel from the instrument. There are four screws on the top, four screws on the bottom and eight screws on the rear panel that hold it in place. Note that four of the screws on the rear panel hold the fan and fan guard in place.

15) Replace the rear panel with the new rear panel included in the retrofit kit.

16) Install the CPU board in the bottom slot of the card cage by reversing steps 3, 7, and 8.

17) Install the State Master board in the slot directly above the CPU board.

18) Install the Timing Master board in the slot directly above the State Master board.

19) Install the State Slave board from the retrofit kit in the service slot directly behind the keyboard. The component side of the State Slave board should face toward the front of the instrument.

20) Turn on the instrument.

21) Measure the DC voltage between TP1 and TP GND. Adjust R4 until the voltage is +5.0 volts +/-5 mV.

22) Turn off the instrument.

23) Remove the State Slave board from the service slot and install in the top slot in the card cage.

24) Install the bottom cover.

25) Install the top cover from the retrofit kit.

26) Install the accessory pouch from the retrofit kit onto the top cover.

27) Install the rear casting from the retrofit kit.

28) Affix the small connector label to the rear casting.

29) Connect the three 10271A probes to the State Master board. The label shows the proper orientation of the probes.

30) Connect a 10272A probe to the Timing Master board.

31) Connect the three 10273A probes in the retrofit kit to the State Slave board.

32) Install the rear door in the retrofit kit to the rear casting.

33) Replace the rear feet.

34) Remove the label from the front of the instrument and replace with the 1630G label in the retrofit kit.

35) To verify proper operation, run the power-on self-test described in Section IV of this manual.

D-5. Instruments With Serial Prefix 2311 and 2318A

1) Remove rear feet.

2) Remove bottom cover.

3) Disconnect two cables at the front of the CPU board (bottom board in the instrument).

4) Remove rear door.

5) Disconnect Acquisition probes.

6) Remove rear casting.

7) Remove two screws beneath HP-IB connector.

8) Remove CPU Board.

9) Remove the eight program ROMs from the sockets in the center of the board.

10) Install the eight program ROMs from the retrofit kit. Figure 1 shows the proper order of installation.

11) With a small piece of wire, connect pins 25 and 26 together on U6M.

12) Remove the State Master board. The State Master board is directly above the CPU board in the card cage.

13) Cut the trace between U4l and DL1 (see figure 2).

14) With a small piece of wire, connect U4L pin 9 to DL1 pin 6 (see figure 2).

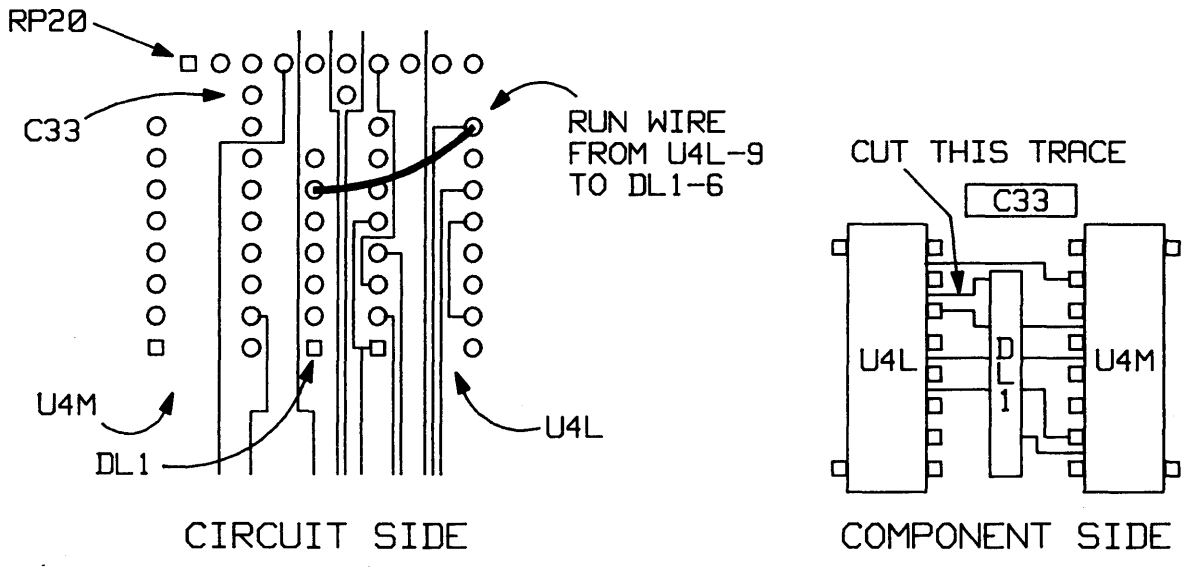

Figure D-2. PC Board Corrections

15) Remove the remaining boards in the card cage.

16) Remove the top cover.

17) Remove the rear panel from the instrument. There are four screws on the top, four screws on the bottom and eight screws on the rear panel that hold it in place. Note that four of the screws on the rear panel hold the fan and fan guard in place.

18) Replace the rear panel with the new rear panel included in the retrofit kit.

19) Install the CPU board in the bottom slot of the card cage by reversing steps 3, 7, and 8.

20) Install the State Master board in the slot directly above the CPU board.

21) Install the Timing Master board in the slot directly above the State Master board.

22) Install the State Slave board from the retrofit kit in the service slot directly behind the keyboard. The component side of the State Slave board should face toward the front of the instrument.

23) Turn on the instrument.

24) Measure the DC voltage between TP1 and TP GND. Adjust R4 until the voltage is +5.0 volts +/-5 mV.

25) Turn off the instrument.

26) Remove the State Slave board from the service slot and install in the top slot in the card cage.

27) Install the original bottom cover and the top cover from the retrofit kit.

28) Install the accessory pouch from the retrofit kit onto the top cover.

29) Install the rear casting from the retrofit kit.

30) Affix the small connector label to the rear casting.

31) Connect the three 10271A probes to the State Master board. The label shows the proper orientation of the probes.

32) Connect a 10272A probe to the Timing Master board.

33) Connect the three 10273A probes in the retrofit kit to the State Slave board.

34) Install the rear door in the retrofit kit to the rear casting and replace the rear feet.

35) Remove the label from the front of the instrument and replace with the 1630G label in the retrofit kit.

36) To verify proper operation, run the power-on self-test described in Section IV of this manual.

D-6. Instruments With Serial Prefix 2412 and Above

1) Remove rear feet.

2) Remove bottom cover.

3) Disconnect two cables at the front of the CPU board (bottom board in the instrument).

4) Remove rear door.

5) Disconnect Acquisition probes.

6) Remove rear casting.

7) Remove two screws beneath HP-IB connector.

8) Remove CPU Board.

9) Remove the eight program ROMs from the sockets in the center of the board.

10) Install the eight program ROMs from the retrofit kit. Figure 1 shows the proper order of installation.

11) Install the CPU board in the bottom slot of the card cage by reversing steps 3, 7, and 8.

12) If the instrument is a 1630D, remove the Timing Slave board. The Timing Slave board is in the top slot in the card cage.

13) Remove the top cover.

14) Install the State Slave board from the retrofit kit in the service slot directly behind the keyboard. The board should face with the components toward the front of the instrument.

15) Turn on the instrument.

16) Measure the DC voltage between TP1 and TP GND. Adjust R4 until the voltage is +5.0 volts +/-5 mV.

17) Turn off the instrument.

18) Remove the State Slave board from the service slot and install in the top slot in the card cage.

19) Install the top and bottom covers.

20) Install the rear casting.

21) Connect the three 10271A probes to the State Master board. The label shows the proper orientation of the probes.

22) Connect a 10272A probe to the Timing Master board.

23) Connect the three 10273A probes in the retrofit kit to the State Slave board.

24) Install the rear door to the rear casting.

25) Replace the rear feet.

26) Remove the label from the front of the instrument and replace with the 1630G label in the retrofit kit.

27) To verify proper operation, run the power-on self-test described in Section IV of this manual.

D-7. CONVERTING A 1630G BACK TO A 1630D

Any 1630G can be converted back to a 1630D using the following procedure.

D-8. Required Parts

Timing Slave Board
1630D PROM SET
10272A 8 Channel State/Timing Probe

NOTE: The part numbers of these parts may change from time to time so they are not listed here. Contact an HP sales and service office for further information.

D-9. Instructions

1) Remove CPU board (see steps for removing CPU board in the instructions for retrofitting to a 1630G).

2) Replace the ROM's on the CPU board with the ROMs listed above. Figure 1 shows the locations of the ROMs.

3) Replace the State Slave board with the Timing Slave board.

4) Reassemble instrument.

5) Run the power-on self-test to check operation.

Note: It is not necessary to remove jumpers on the CPU or State Master board to convert a 1630G to a 1630D.

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APPENDIX E
1630A/D/G
MISCELLANEOUS SERVICE INFORMATION

E-1. INTRODUCTION

This appendix covers miscellaneous service information that has been distributed through other channels but is included here for convenience.

E-2. CPU BOARD - BLUE STRIPE/TROUBLESHOOTING

This section addresses the fact that the present CPU boards cannot be troubleshot to the component level using Guided Probe. There are plans to replace the present boards, 01630-66503, 01630-66512, 01630-66519 (1630G), and 01630-66522, with a board and software allowing troubleshooting with Guided Probe.

Presently, the CPU boards are supported by the Blue-Stripe board exchange program. The part number for the Blue-Stripe board is 01630-66512.

The flow chart on the next page may be useful for troubleshooting common CPU problems and repairing to the component level, therefore avoiding replacement of the entire board.

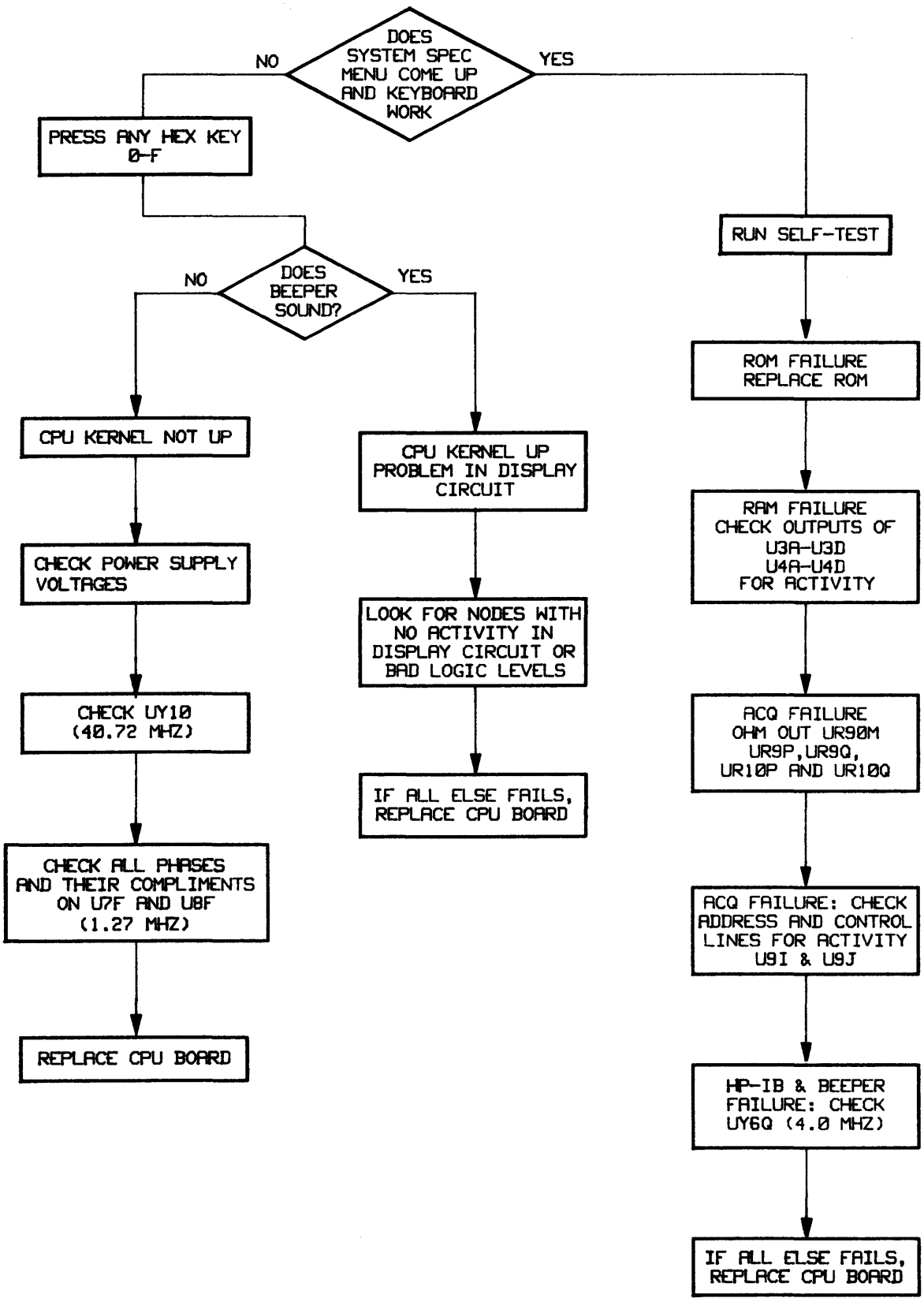

Figure E-1. CPU Board Troubleshooting Flow Chart.

E-3. 1630A/D/G SERVICE NOTE INDEX

1630A/D-0

SUPERCEDES:

NONE

HP 1630A/D LOGIC ANALYZER

SERVICE NOTE INDEX

1630A/D-0	MAY 83	WN	Service Note Index (This Note)
1630A/D-1	MAY 83	WA	ESD Protection for the HP-IL Interface
1630A/D-2	MAY 83	WA	200 MHz Oscillator Rework
1630A/D-3	MAY 83	WO	Display Adjustment
1630A/D/G-4	MAY 84	WA	Overvoltage Protection Design Change

I/-WN

5/83-D2/DA

E-4. ESD Protection for the HP-IL Interface

1630A/D-1

SUPERCEDES:

NONE

HP 1630A/D LOGIC ANALYZER

Serial Numbers: 2311A00231 and Below (1630A)
Serial Numbers: 2311A00791 and Below (1630D)

ESP PROTECTION FOR THE HP-IL INTERFACE

The 1630A/D Logic Analyzers indicated above may require additional protection from Electrostatic Discharge on the HP-IL Interface. Without this change, ESD may damage the HP-IL Controller IC and prevent the operator from using the HP-IL interface. However, this failure will not present a safety hazard to the user, nor will it affect the performance of the rest of the analyzer.

FAILURE IDENTIFICATION::

If the HP-IL controller is damaged by ESD, the 1630A/D will not recognize a cassette drive connected to the HP-IL. To positively identify this problem, remove the CPU board (01630-66503 or 01630-66512) as described in the Service Manual. Visually inspect U20; a damaged controller will have a small (1/4" diameter) circular distortion in the center of the IC.

PARTS REQUIRED:

DESCRIPTION	HP PART NUMBER	QTY.
Board-Assy ESD	01630-66513	1

MODIFICATION INSTRUCTIONS:

1. REMOVE THE POWER CORD FROM THE INSTRUMENT.
2. Remove the CPU board from the 1630A/D as described in the Service Manual.
3. Remove U20 by unsoldering.
4. Install the ESD board with the HP-IL chip where U20 was installed.
5. Re-assemble the 1630A/D.

Repair Time: 1.25 hours

D/0F/WA

5/83-D2/DA

E-5. 200 MHz Oscillator Rework

1630A/D-2

SUPERCEDES:

NONE

HP 1630A/D LOGIC ANALYZER

Serial Numbers: 2311A00213 and Below (1630A)
Serial Numbers: 2311A00769 and Below (1630D)

200 MHz OSCILLATOR REWORK

The 1630A/D Logic Analyzers indicated above may require a rework of the 200 MHz oscillator on the 01630-66506 or 01630-66510 Master Timing board. This oscillator may not self-start reliably. Although the analyzer will not function properly when a fast sample rate is requested for the Timing Analyzer, this failure will not affect the performance of the rest of the analyzer.

FAILURE IDENTIFICATION:

If the 200 MHz oscillator is not self-starting, the Timing Analyzer will display "Waiting for Timing Trigger" for any acquisition with a sample rate of less than 500 nSec. The Timing Analyzer will work properly for sample rate of 500 nSec. and above.

PARTS REQUIRED:

Description	HP Part Number	Qty.
Cap. Variable 2 to 8 pF	0121-0060	1

MODIFICATION INSTRUCTIONS:

1. REMOVE THE POWER CORD FROM THE INSTRUMENT.
2. Remove the Timing Master board from the 1630A/D as described in the Service Manual.
3. Replace C26 with the part specified above.
4. Adjust the oscillator as described in the Service Manual. Note: Adjust the oscillator for reliable self-starting, not for frequency!
5. Re-assemble the 1630A/D.

Repair Time: 1.25 hours

D/OF/WA

5/83-D2/DA

E-6. Display Adjustment

1630A/D-3

SUPERCEDES:

NONE

HP 1630A/D LOGIC ANALYZER

Serial Numbers: 2311A00223 and Below (1630A)
Serial Numbers: 2311A00790 and Below (1630D)

DISPLAY ADJUSTMENT

The 1630A/D Logic Analyzers indicated above may require display adjustment. This adjustment will prevent part of the display from disappearing off of the screen. A mis-adjusted screen will not harm the 1630A/D in any way, but this procedure is recommended anytime a unit comes in for service.

MODIFICATION INSTRUCTIONS:

1. Perform the Display Adjustment Procedure in the 1630A/D Service Manual.
2. Adjust the horizontal size to 146.6 mm and the vertical size to 96.5mm.

D/NS/WO

5/83-D2/DA

E-7. Overvoltage Protection Design Change

1630A/D/G-4

SUPERCEDES:

NONE

HP 1630A/D/G LOGIC ANALYZER

Serial Numbers: 2311A00808 and Below (1630A)
Serial Numbers: 2412A03410 and Below (1630D)
Serial Numbers: 2415A00171 and Below (1630G)

OVERVOLTAGE PROTECTION DESIGN CHANGE

The 1630A/D/G Logic Analyzers make use of a set of neon bulbs which act as spark-gap to provide some degree of protection against the accidental application of 230 VAC when the unit is configured for 115 VAC. However, this circuit has not been totally effective in preventing damage to the instrument. In addition, there are some reliability problems associated with the neon bulbs.

FAILURE IDENTIFICATION:

If the power supply has failed, the CRT screen will not come up when the unit is switched on. Neon bulbs that have failed are black in color.

PARTS REQUIRED: None

MODIFICATION INSTRUCTIONS:

1. REMOVE THE POWER CORD FROM THE INSTRUMENT.
2. Remove top cover of instrument.
3. Clip out E1 and E2 without damage to other connections.
4. Replace top cover.

Repair Time: 0.25 hours

D/PM, OF/WA

5/84-08/SW