Technical specifications 333Mb/s

E4841A 333 Mb/s Generator/Analyzer Module

This module holds any combination of up to four analyzer front-ends (E4847A) and generator front-ends (E4846A). These dual channel front-ends make two channels out of each slot, so eight channels per module. The E4841A is orignally a 667 MHz module, with the use of the dual frontends the maximum data rate is limited to 333 Mb/s. For 675 Mb/s operation the E4832A is recommended.

Segment length resolution:
This is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4841A can be set in steps of 8 bits up to a length of 512 Kbit. If the 8-bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 18.

Sub-frequencies:
For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2,4,8. This influences the dependency between segment length resolution and maximum memory depth (see table 18).

Using the Analyzer, in error capture mode the memory is half of the value shown. (table 18)

Table 15: E4841A Data Generator Timing Specifications
(@ 50 % of amplitude, 50 Ohm to GND and fastest transition times)

Frequency range*		1.000 kHz to 333.333 MHz
	Delay range	0 to 3.0 s (not limited by period).
		For f < 333.334 kHz" max. delay is 1 period.
	Resolution	2 ps. For f < 170 kHz 0.05% of period
	Accuracy	±50 ps ± 100 ppm relative to the zero delay
		placement. For f < 170 kHz the tolerance increases to +/- 0.1%
	Skew	50 ps typ. after deskewing at customer levels
Pulse width		Can be specified as width or % of duty cycle
	Range*	750ps to [Period-750ps]
	Resolution	2 ps
	Accuracy*	± 200 ps ± 0.1 %
Duty Cycle		1 % to 99 %, subject to width limits

* See tables for front-end deratings

Table 16: E4841A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50 Ω to GND

Sampling rate*	Same as generator
Sampling delay range*	Same as generator limited to 1 system period within one front-end.
Accuracy	Same as generator
Resolution	Same as generator
Skew*	Same as generator

*See tables for front-end deratings

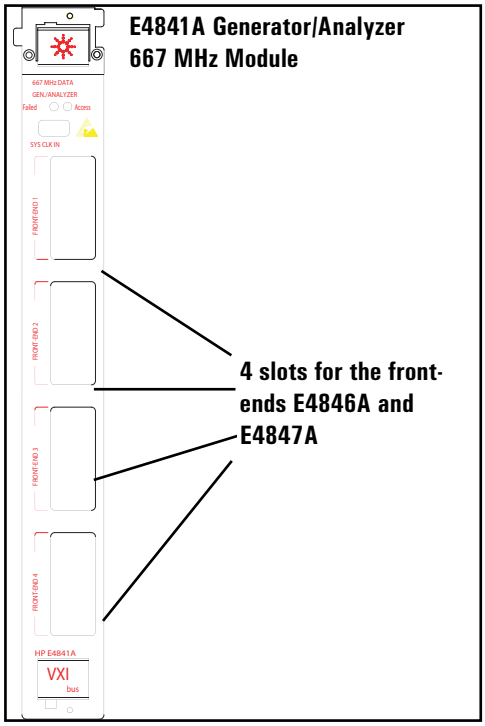

Figure 16

Table 17: Pattern and Sequencing features of E4841A	
Patterns:	
Memory based	**up to (1Mbit) see table 23**
PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, (16)
User	Data editor, file import

Table 18: Data rate range, segment length resolution, available memory for synchronisation and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
20.834...41.666	1 bits	65,504
41.667...83.333	2 bits	131,008
83.334...166.666	4 bits	262,016
166.667...333.333	8 bits	524,032

In general it is possible to set higher values for the segment length resolution at lower frequencie than is indicated in the table

Table 19: Level Parameters for dual Generator Front-End E4846A 200 Mbit/s

	E4846A
Outputs/Source Resistance	2, single-ended 50 Ohm
Maximum Frequency (and Data Formats)	200 Mbit/s (NRZ, DNRZ)
Output Voltage Window	-1.75 to +3.50 V doubles into open)
Addressable Technologies	TTL, ECL (terminated with 50Ω to 0 V/-2 V), PECL (terminated to + 3 V)
Amplitude/Resolution	0.30 to 3.50 Vpp / 10 mV doubles into open)
Accuracy	Levels: ± 5% ± 100 mV
Short Circuit Current	+70 mA max., -35 mA max.
Maximum External Voltage and Termination Voltage Range	-2 to +5 V
Transition Times **20-80% at ECL levels** **10-90% at 2.5 Vpp ampl**	Constant slew rate < 1.2 ns, 700 ps typ. < 2.5 ns, 1.8 ns typ.
Overshoot/Ringing **Droop**	< 5% + 120 mV 2.5 Vpp < 20%, ECL < 10%
Minimum Pulsewidth	ECL: < 1.5 ns, 1 ns typ. 2.5 Vpp: < 4.0 ns, 3 ns typ.

Table 20: Parameters for Analyzer Front-End E4847A 333 MSa/s, dual channel

Analog Bandwidth	**350 MHz typ.**
Number of Channels	**2, independent levels**
Typical Impedance	**50 Ω /10 k Ω parallel < 5 pF**
Termination Voltage	**-2.1 to +3.1 V (50 Ω selected)**
Number of Thresholds	**one per input**
Threshold Voltage Range (into 50 Ω)	**-2.10 to +5.10 V**
Threshold Resolution	**5 mV**
Threshold Accuracy	**±20 mV ± 1%**
Input Sensitivity	**200 mVpp**
Minimum Detectable Pulsewidth	**1 ns typ. at ECL levels**

Input/Output

Addressable technolgies TTL, 3.3V CMOS, (P)ECL

Analyzer Output
-single-ended
-50 Ohm
-High impedence (10K)

The sampling point of the dual channel analyzer input can be individually adjusted within one system period.

Generator output
-single ended outputs
-enable/disable realais

The Delay range of the two channels within one front-end can be sued over the full range. The output can be use into 50 Ohm or open. Into open the voltage range doubles

Compatibilty

The E4841A can be used with E4843A, E4844A, E4837A, front-ends up to 667MHz with up to 1 meg of memory.

I/O Pin Stimulation/Measurement

The E4847A high-impedance analyzer front-end assists measurements on bidirectional ports. In parallel with a generator front-end, the impedance presented to the pin is 50 Ω. A SMA tee connector 15440A (4 Parts) is required.