



# Am78C201A

## InterWave™ Interactive Audio and Wavetable Solution

### •DISTINCTIVE CHARACTERISTICS

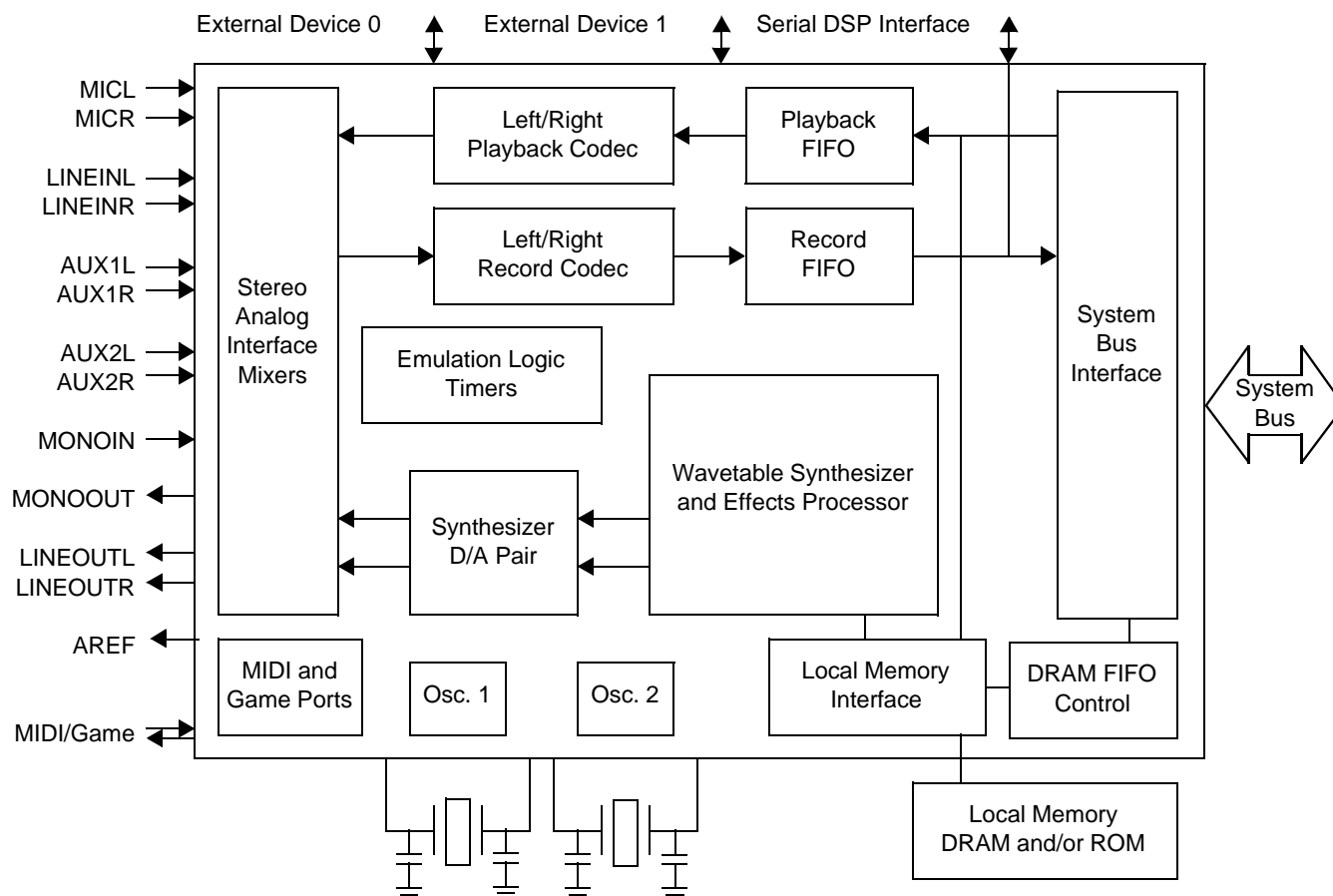
- 32-voice stereo wavetable synthesizer
- Integrated effects processor
- Up to 32 channels of digital mixing
- Stereo 16-bit audiophile codec with IMA ADPCM 4:1 compression/decompression
- MPC-compliant analog mixer
- ISA plug and play
- MIDI and game ports
- Power management, 3.3 V and 5 V
- System expansion through a serial DSP interface

### • Supports multiple standards:

- Sound Blaster compatible applications
- MPU-401
- MPC2, MPC3
- General MIDI
- Microsoft® Windows®95, DirectSound™\*
- Windows 3.x API, Win32 API\*
- Miles AIL API\*
- HMI SOS API\*
- UltraSound\*
- Lucas Arts iMUSE API\*

\* Appropriate software drivers required

### BLOCK DIAGRAM



## GENERAL DESCRIPTION

The InterWave audio IC provides a complete audio sub-system that meets all major business and entertainment audio standards. The Am78C201A device has an ISA Plug and Play interface. It integrates a 32-voice stereo wavetable synthesizer, a 16-bit stereo audiophile codec and audio mixer, both MIDI and game ports, and legacy FM sound card emulation hardware into a single device.

### Analog Interface, Mixers

The Am78C201A device includes stereo analog inputs provided for microphone, line, and, on the Am78C201A device, two auxiliary inputs. These signals are combined with the outputs of the left and right playback codecs to produce the stereo and monaural outputs. The gain of each of these channels is controlled by internal registers, which are loaded through the system bus interface.

### Playback and Record Codec

The full duplex 16-bit audiophile stereo codec is a register compatible super-set of the CS4231 and AD1848. The codec provides: independently programmable sample rates for the playback and record paths; a variety of data types and compression schemes; on board 16-sample playback and record FIFOs; and a serial port that allows an external DSP engine to connect directly to the record and playback paths.

### Wavetable Synthesizer

The wavetable synthesizer offers 32 16-bit stereo voices, all running at a 44.1 kHz frame rate. Each voice supports address generation, envelope generation, tremolo, vibrato, panning, and volume control. Any combination of the 32 synthesizer voices can be used to play or mix digital audio files. Additionally, all of the voice processing power can be used to modify the signals, including volume, pan, frequency shift, reverb, chorus, flanging, echo, tremolo, and vibrato.

The synthesizer includes an on-chip effects processor that provides up to eight channels of reverb, echo, chorus, and flanging capability. Effects can be assigned to individual voices or to any combinations of voices.

The wavetable memory can be either DRAM or ROM, or a combination of the two. When DRAM is used, musical instrument “patches” can be swapped in and out as

needed. This swapping allows for a smaller, lower-cost wavetable memory. The IC supports up to 16 Mbytes each of DRAM and ROM. Wavetable patches can be 8-bit, 16-bit, or 8-bit  $\mu$ -law compressed.

The stereo digital output of the synthesizer is converted into analog form by two on-chip 16-bit digital-to-analog converters (DACs).

### Bus Interface

The bus interface of the Am78C201A device is fully compliant with the Plug and Play standard with no external logic. The Plug and Play interface can be either an 8-bit or a 16-bit ISA interface. The IC supports connecting an external device, such as a CD-ROM drive, to the ISA bus through the Plug and Play interface.

### Local Memory Interface

The local memory control module (LMC) transfers data between local memory and the synthesizer, the system bus interface, and the codec. Local memory can include up to four banks of DRAM and up to four banks of ROM. The IC contains support for implementing external FIFOs using DRAM, and for a serial EEPROM that in turn supports the Plug and Play interface.

### MIDI and Game Ports

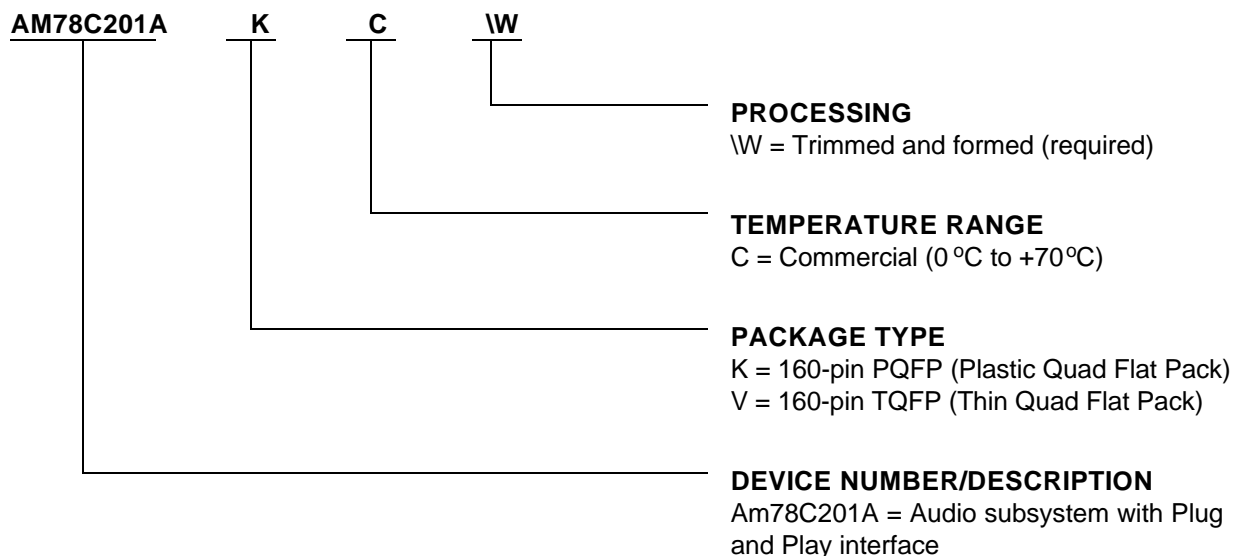
The MIDI (Musical Instrument Digital Interface) port provides data to a user-supplied external interface between the InterWave IC and a MIDI-compatible Local Area Network (LAN). The MIDI port is built around a UART with a 16-byte receive FIFO.

The game port of the InterWave IC provides the functions found in standard game ports in PCs. The Am78C201A device supports connection of up to two joysticks with a total of four buttons. Trim DACs are provided to adjust the offset voltage for calibration.

## ORDERING INFORMATION

### Standard Products

AMD® standard products are available in several packages and operating ranges. The order numbers (Valid Combination) are formed by a combination of the elements below.



Valid Combinations	
Am78C201A	KCW
Am78C201A	VCW

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## PIN ASSIGNMENTS AND CONNECTION DIAGRAMS

The InterWave audio IC is packaged in a 160-pin plastic quad flat pack (PQFP). Figure 1 shows the package layout and Table 1 lists the pin assignments. AVCC and AVSS are analog power and ground pins; VCC and VSS are digital power and ground pins.

# CONNECTION DIAGRAM

## 160 Pin Top View

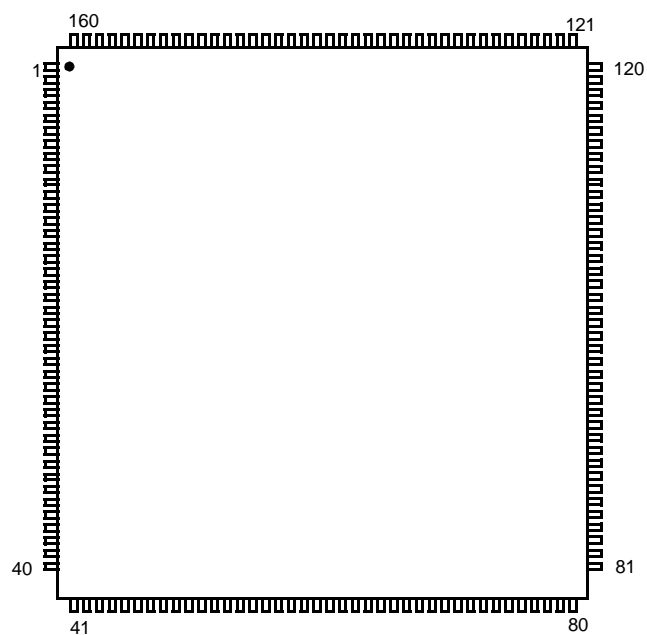


Table 1. Pin Assignments

160 Pin	Signal Name	160 Pin	Signal Name	160 Pin	Signal Name	160 Pin	Signal Name
1	SA7	41	EX_DRQ	81	MD7	121	SD11
2	SA8	42	GAMIN3	82	VCC	122	SD10
3	GPOUT0	43	GAMIN2	83	DRQ7	123	SD9
4	RESET	44	GAMIN1	84	$\overline{\text{DAK7}}$	124	SD8
5	GPOUT1	45	GAMIN0	85	$\overline{\text{ROMCS}}$	125	TC
6	VCC	46	GAMIO3	86	$\overline{\text{RAHLD}}$	126	DRQ1
7	AVSS	47	GAMIO2	87	$\overline{\text{RAS}}$	127	$\overline{\text{DAK1}}$
8	AVSS	48	GAMIO1	88	$\overline{\text{MWE}}$	128	AEN
9	IREF	49	GAMIO0	89	RA20	129	IOCHRDY
10	CFILT	50	VSS	90	RA21	130	IRQ2/9
11	AVSS	51	VSS	91	VCC	131	IRQ3
12	AVCC	52	MA0	92	IRQ15	132	$\overline{\text{IOR}}$
13	AREF	53	MA1	93	IRQ12	133	VSS
14	AUX1L	54	$\overline{\text{EX\_DAK}}$	94	$\overline{\text{BKSEL0}}$	134	VCC
15	MICL	55	VCC	95	$\overline{\text{BKSEL1}}$	135	$\overline{\text{IOW}}$
16	AVSS	56	MA2	96	VSS	136	$\overline{\text{IOCS16}}$
17	AVCC	57	MA3	97	$\overline{\text{BKSEL2}}$	137	SD0
18	AVSS	58	MA4	98	$\overline{\text{BKSEL3}}$	138	SD1
19	AUX1R	59	MA5	99	IRQ11	139	SD2
20	MICR	60	EX_IRQ	100	XTAL1I	140	SD3
21	AUX2R	61	$\overline{\text{EX\_CS}}$	101	XTAL1O	141	VSS
22	LINEINR	62	VSS	102	VSS	142	SD4
23	AVSS	63	MA6	103	XTAL2O	143	SD5
24	LINEINL	64	MA7	104	XTAL2I	144	SD6
25	AUX2L	65	MA8	105	VCC	145	SD7
26	AVCC	66	MA9	106	MIDIRX	146	VCC
27	LINEOUTR	67	MA10	107	MIDITX	147	VSS
28	AVSS	68	$\overline{\text{DAK5}}$	108	C32KHZ	148	IRQ5
29	LINEOUTL	69	MD0	109	$\overline{\text{SUSPEND}}$	149	IRQ7
30	MONOOUT	70	MD1	110	VSS	150	$\overline{\text{IOCHK}}$
31	MONOIN	71	MD2	111	$\overline{\text{SBHE}}$	151	SA0
32	AVSS	72	MD3	112	DRQ0	152	SA1
33	AVCC	73	VSS	113	$\overline{\text{DAK0}}$	153	SA2
34	AVSS	74	DRQ5	114	VCC	154	SA3
35	PNPCS	75	VCC	115	VCC	155	SA4
36	SA9	76	$\overline{\text{DAK6}}$	116	SD15	156	SA5
37	SA10	77	DRQ6	117	SD14	157	VSS
38	SA11	78	MD4	118	SD13	158	DRQ3
39	VCC	79	MD5	119	SD12	159	$\overline{\text{DAK3}}$
40	VSS	80	MD6	120	VSS	160	SA6

## PIN SUMMARY

**Table 2. Am78C201A Pin Designations**

System Control		Codec		Local Memory		Ports, Crystals	
Pin Name	# Pins	Pin Name	# Pins	Pin Name	# Pins	Pin Name	# Pins
SD15–SD0	16	MIC[L,R]	2	MA10–MA0	11	XTAL1I	1
SA11–SA0*	12	AUX1[L,R]	2	MD7–MD0	8	XTAL1O	1
→SCS[1,0], SA[3–0]		AUX2[L,R]	2	BKSEL[1–0]	4	XTAL2I	1
SBHE	1	LINEIN[L,R]	2	ROMCS	1	XTAL2O	1
DRQ[7,6,5,3,1,0]	6	LINEOUT[L,R]	2	RAHLD	1	MIDIRX	1
DAK[7,6,5,3,1,0]	6	MONOIN	1	RA21–RA20	2	MIDITX	1
TC	1	MONOOUT	1	MWE	1	GAMIN[3–0]	4
IRQ[15,12,11]	3	IREF	1	RAS	1	GAMIO[3–0]	4
IRQ[7,5,3,2/9]	4	CFILT	1	BKSEL[3–2]*		IBTNI[1–0]	
IRQ10, IRQ4*	2→	GPOUT[1–0]	–				
IOCHK	1	AREF	1				
IOR	1						
IOW	1						
IOCS16	1						
IOCHRDY	1						
AEN	1						
EX_IRQ*	1→	ESPCLK	–				
EX_DRQ*	1→	ESPDIN	–				
EX_DAK*	1→	ESPSYNC	–				
EX_CS*	1→	ESPDOUT	–				
RESET	1						
SUSPEND*	1→			FRSYNC	–	TELCS	
C32KHZ*	1→			EFFECT	–	TELIRQ	
PNPCS	1						
Power & Ground	37						

**Notes:**

1. These pins have multiple functions as indicated.
2. The arrow (→) identifies the common pin

## PIN DESCRIPTIONS BY FUNCTIONAL GROUP

Table 3 through Table 8 list pins by function and describes each pin.

**Table 3. System Bus Interface Pins**

Pin Name	Pin (201)	Type	Description
AEN	128	I, T	<b>Address Enable</b> from the ISA bus, used to distinguish between DMA and I/O cycles. This signal must be driven Low when the bus performs an I/O access to the IC.
$\overline{\text{DAK0}}$ , $\overline{\text{DAK1}}$ , $\overline{\text{DAK3}}$ , $\overline{\text{DAK5}}$ , $\overline{\text{DAK6}}$ , $\overline{\text{DAK7}}$	113, 127, 159, 68, 76, 84	I, T	The selectable <b>DMA Acknowledge</b> lines from the ISA bus. $\overline{\text{DAK0}}$ , $\overline{\text{DAK1}}$ , and $\overline{\text{DAK3}}$ are used for 8-bit DMA transfers and $\overline{\text{DAK5}}$ , $\overline{\text{DAK6}}$ , and $\overline{\text{DAK7}}$ are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
DRQ0, DRQ1, DRQ3, DRQ5, DRQ6, DRQ7	112, 126, 158, 74, 77, 83	3S, T	The selectable <b>DMA Request</b> lines to the ISA bus. DRQ0, DRQ1, and DRQ3 are used for 8-bit DMA transfers and DRQ5, DRQ6, and DRQ7 are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
IOCHRDY	129	OD, T	<b>I/O Channel Ready</b> to the ISA bus is used to extend the I/O bus cycle when deasserted. IOCHRDY High indicates that the device is ready to complete the current I/O bus cycle.
$\overline{\text{IOCS16}}$	136	OD, T	<b>I/O Chip Select 16</b> is asserted Low by the device during an I/O Read or Write operation to indicate that a 16-bit port is supported at the current address.
$\overline{\text{IOR}}$	132	I, T	<b>I/O Read</b> on the ISA bus is driven Low by the host to indicate that an input/output Read operation is taking place. $\overline{\text{IOR}}$ is valid only if the AEN signal is also Low.
$\overline{\text{IOW}}$	135	I, T	<b>I/O Write</b> on the ISA bus is driven Low by the host to indicate that an input/output Write operation is taking place. $\overline{\text{IOW}}$ is valid only if the AEN signal is also Low.
IRQ2/9, IRQ3, IRQ5, IRQ7, IRQ11, IRQ12, IRQ15	130, 131, 148, 149, 99, 93, 92	3S, T	The selectable <b>Interrupt Requests</b> to the ISA bus. The device can select up to three of the nine supported interrupts; the allocation of interrupt signals is fully programmable using the Plug and Play registers. Internally, interrupt sources can be assigned to the available interrupt request signals as required by software.
IRQ4, IRQ10	3, 5	3S, C	See description for <b>Interrupt Requests</b> . These pins are multiplexed with GPOUT0 and GPOUT1. IRQ4 and IRQ10 are selected by IEIRQI[7] = 0 ( $\overline{\text{EX\_DAK}} = 0$ at reset). While in this mode, these pins can be programmed to be open drain using the IEIRQI register. See the <i>InterWave Programmer's Guide</i> .
$\overline{\text{IOCHK}}$	150	OD, T	<b>I/O Check</b> . Channel or I/O channel check on the ISA bus. $\overline{\text{IOCHK}}$ is asserted Low by the device to generate an NMI (non-maskable interrupt).
PNPCS	35	B, T	<b>Plug and Play Serial EEPROM Chip Select</b> . Active High output used as chip select for the Plug and Play serial EEPROM. This is an input during reset; its state is latched by the trailing edge of reset to determine whether the IC is in PNP-compliant mode (Low) or PNP-system mode (High).
RESET	4	I, T	<b>Reset</b> from the ISA bus. When RESET is asserted High on the ISA bus, the device performs an internal system reset. The RESET pin must be asserted for at least 10 ms before being deasserted. While in the reset state, the device ignores all ISA bus activity and no local memory cycles take place. On the trailing edge of RESET, the state of some I/O pins are latched to determine the configuration of certain multifunction pins.
$\overline{\text{SBHE}}$	111	I, T	The <b>System Byte High Enable</b> signal indicates the High byte of the system data bus is to be used. When connecting to an 8-bit ISA bus, this pin must be disconnected.

Table 3. System Bus Interface Pins (continued)

Pin Name	Pin (201)	Type	Description
SD15–SD0	116–119, 121–124, 145–142, 140–137	B, T	The ISA <b>System Data Bus</b> is used to transfer data to and from the device. The entire data bus, SD15–SD0, is active during 16-bit I/O access. During 8-bit I/O accesses, the lower data bus, SD7–SD0, is active when accessing an even byte, and the upper data bus, SD15–SD8, is active when accessing an odd byte.
TC	125	I, T	<b>Transfer Complete</b> or <b>Terminal Count</b> is driven active High by the master or slave DMAC when the word or byte transfer count for a DMA channel is complete.

**Note:**

Pin Type: A = analog signal, B = digital bi-directional, C = CMOS compatible, I = digital input, O = digital output, OD = digital open drain output, P = power or ground, T = TTL compatible, 3S = digital 3-state output

Table 4. Codec/Mixer Pins

Pin Name	Pin (201)	Type	Description
AREF	13	A	The <b>Analog Reference</b> pin provides a reference voltage which can be used by external circuitry. AREF can be placed into High-impedance mode, as controlled by the Mono Input and Output Control (CMONOI) register. See the <i>InterWave Programmer's Guide</i> .
AUX1L, AUX1R	14, 19	A	The <b>Stereo Auxiliary 1 Inputs</b> provide an alternative input path and are multiplexed with the synthesizer DAC outputs. Only one of these sources can be mixed and supplied to LINEOUT as selected in Configuration Register 3 (CFG3I). See the <i>InterWave Programmer's Guide</i> . Either of these sources can be selected for analog-to-digital conversion through the Record Multiplexer. The AUX1 input impedance is at least 20 k $\Omega$ .
AUX2L, AUX2R	25, 21	A	The <b>Stereo Auxiliary 2 Inputs</b> can always be independently mixed or muted. Typically, these inputs are used for mixing analog CD stereo audio. The AUX2 input impedance is at least 20 k $\Omega$ .
CFILT	10	A	The <b>Capacitor Filter</b> input must be connected to analog ground through a 0.1 $\mu$ F capacitor and a 10 $\mu$ F capacitor.
GPOUT0, GPOUT1	3, 5	3S, T	The <b>General Purpose Digital Outputs</b> are two general purpose digital outputs controlled by bits located in the External Control (CEXTI) register. These pins are multiplexed with IRQ4 and IRQ10. GPOUT0 and GPOUT1 are selected by IEIRQI[7] = 1 ( $\overline{\text{EX\_DAK}}$ = 1 at reset). See the <i>InterWave Programmer's Guide</i> .
IREF	9	A	The Current Reference input pin must be connected to analog ground through a 61.9 k $\Omega$ 1% tolerance resistor.
LINEINL, LINEINR	24, 22	A	The <b>Stereo Line Inputs</b> can always be independently mixed or muted. These inputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these inputs are used for mixing or recording analog stereo audio from a variety of external stereo audio sources. The LINEIN input impedance is at least 20 k $\Omega$ .
LINEOUTL, LINEOUTR	29, 27	A	The <b>Stereo Line Outputs</b> are stereo single-ended line drivers which can drive 5-k $\Omega$ loads. These outputs are the sum of the left and right mixer channels respectively. The LINEOUTs can be independently attenuated or muted and these mixer outputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these outputs are used for driving powered speakers or connected to speaker or headphone drivers.



Table 4. Codec/Mixer Pins (continued)

Pin Name	Pin (201)	Type	Description
MICL, MICR	15, 20	A	The <b>Stereo Microphone Inputs</b> can be independently mixed or muted. These inputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these inputs are used for mixing or recording a preamplified signal from a stereo microphone. The MIC input impedance is at least 20 k $\Omega$ .
MONOIN	31	A	The <b>Mono Input</b> can always be independently mixed or muted and feeds both the left and right mixer output paths. Typically, this input is used for mixing PC speaker audio. The MONOIN input impedance is at least 20 k $\Omega$ .
MONOOUT	30	A	The <b>Mono Output</b> is a single-ended line driver which can drive a 5 k $\Omega$ load. It provides the sum of the left and right LINEOUT signals and is independently mutable. Typically, this output is connected to a speaker driver for a PC speaker.

Table 5. Local Memory Controller Pins

Pin Name	Pin (201)	Type	Description
BKSEL0–BKSEL3	94, 95, 97, 98	O, C	The <b>Bank Select</b> signals are used to control the $\overline{\text{CAS}}$ input of each DRAM bank or the Output Enable input of each ROM bank. BKSEL[2,3] can also be used as IBTNI[0,1], which are inputs to a software readable register. (See Table 6 and the <i>InterWave Programmer's Guide</i> .)
MA3–MA10	57–59, 63–67	B, C	The <b>Memory Address</b> signals are multiplexed row-column address lines for DRAM cycles. For ROM access cycles, they are time multiplexed ROM Latched Address[10:3] outputs and ROM High Byte Data Bus[15:8] inputs. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal.
MA0–MA2	52, 53, 56	O, C	<b>Memory address</b> . The multiplexed row-column address bits for DRAM cycles, and the RLA[2,1,19] outputs for ROM access cycles.
MD7–MD0	69–72, 78–81	B, C	The <b>Memory Data Bus</b> for DRAM cycles. For ROM access cycles, they are time-multiplexed ROM Latched Address[18:11] outputs and ROM Low Byte Data Bus[7:0]. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal. For Plug and Play Serial EEPROM accesses, MD[2] is the Serial Data Clock (SK), MD[1] is the Serial Data Input (DI), and MD[0] is the Serial Data Output (DO).
$\overline{\text{MWE}}$	88	B, C	The <b>Memory Write Enable</b> output controls the $\overline{\text{WE}}$ pin of all the DRAM banks and determines whether a DRAM cycle is a Read or Write. This pin remains High during all refresh cycles.
RA20–RA21	89, 90	B, C	The High <b>ROM Address</b> lines during ROM accesses. At the trailing edge of RESET, these signals become inputs that are used to determine the mode of certain multiplexed function pins.
$\overline{\text{RAHLD}}$	86	O, C	The <b>ROM Address Hold</b> output is used to latch the state of ROM Latched Address lines, MD[7:0] (RLA[18:11]), and MA[10:3] (RLA[10:3]), in external latches during ROM accesses.
$\overline{\text{RAS}}$	87	O, C	The <b>Row Address Strobe</b> is asserted Low during DRAM accesses and is connected directly to the $\overline{\text{RAS}}$ input of each DRAM in all of the DRAM banks.
$\overline{\text{ROMCS}}$	85	O, C	The <b>ROM Chip Select</b> output is asserted Low during ROM accesses and is connected directly to the Chip Select/Enable input of each ROM in all of the ROM banks.

**Table 6. Additional Multiplexed Function Pins**

Pin Name	Pin (201)	Type	Description
$\overline{\text{BKSEL}}[2,3]/\text{IBTN}[0,1]$	97, 98	O, C I, C	The <b>Bank Select</b> signals $\overline{\text{BKSEL}}[2,3]$ can also be used as flag inputs to the IBTN register. The function of these pins is controlled by the IEIRQ register. (See the <i>InterWave Programmer's Guide</i> .)
C32KHZ / $\overline{\text{EFFECT}}$ / TELIRQ	108	I, C O, C I, C	The <b>Suspend Mode Refresh Clock</b> input (C32KHZ) is used for refreshing local memory DRAM when the InterWave IC is in Suspend mode.  This pin can also be the <b>Synthesizer Effect Local Memory Writes</b> output ( $\overline{\text{EFFECT}}$ ), which is asserted Low during writes to local memory DRAM involving synthesizer delay-based effects.  It can also be TELIRQ, an interrupt input from an external device.  The mode of this pin is determined by the state of RA[21] at the trailing edge of RESET. If RA[21] is High at the trailing edge of RESET, either C32KHZ or TELIRQ is selected via the PTACTI register. (See the <i>InterWave Programmer's Guide</i> .); if RA[21] is Low, then $\overline{\text{EFFECT}}$ is selected.
$\overline{\text{SUSPEND}}$ / $\overline{\text{FRSYNC}}$ / $\overline{\text{TELCS}}$	109	I, C O, C O, C	When the <b>Suspend</b> input is asserted Low, all chip activity becomes frozen, the oscillators are turned off, the C32KHZ input clock is used to refresh local memory DRAM, and most of the ISA bus inputs and outputs are isolated from the IC.  This pin can also be used as the <b>Frame Sync</b> output, which is asserted Low at the start of each synthesizer data frame.  This pin can also be used as $\overline{\text{TELCS}}$ , a decode of the address bus for external function control.  The operation mode of this pin is determined by the state of RA[21] at the trailing edge of the RESET signal. If RA[21] is High at the trailing edge of RESET, either the $\overline{\text{SUSPEND}}$ input function the $\overline{\text{TELCS}}$ output signal is selected via the PTACTI register. (See the <i>InterWave Programmer's Guide</i> .); if RA[21] is Low, the $\overline{\text{FRSYNC}}$ output signal is selected.
$\overline{\text{EX\_CS}}$ / ESPDOUT	61	B, T O, T	The <b>External Device Chip Select</b> consisting of the decode of AEN deasserted (Low) and the address specified in the PNP CD-ROM Address High/Low (PRAHI and PRALI) registers.  Optionally, this pin can be configured as the <b>External Serial Port Data Out</b> signal (ESPDOUT) through the Compatibility (ICMPTI) register.
$\overline{\text{EX\_DAK}}$ / ESPSYNC	54	B, T O, T	The <b>External Device DMA Acknowledge</b> output to the external device.  Optionally, this pin can be configured as the <b>External Serial Port Sync</b> signal (ESPSYNC) through the Compatibility (ICMPTI) register.
EX_DRQ / ESPDIN	41	I, T I, T	<b>External Device DMA Request</b> .  Optionally, this pin can be configured as the <b>External Serial Port Data In</b> signal (ESPDIN) through the Compatibility (ICMPTI) register.
EX_IRQ / ESPCLK	60	I, T O, T	<b>External Device Interrupt Request</b> .  Optionally, this pin can be configured as the 2.1168MHz <b>External Serial Port Clock</b> output signal (ESPCLK) through the Compatibility (ICMPTI) register.
SA11–SA6  SA5–SA0/ SCS1–SCS0, SA3–SA0	38–36, 2, 1, 160 156–151	I, T I, T	<b>System Address Bus</b> . During Internal Decoding mode, these inputs are the 12 lower lines of the ISA System Address Bus which are used along with AEN to generate decodes for internal device resources. During External Decoding mode, the System Address Bus is redefined as follows: SA[11:6] are not used, SA[5:4] are redefined as <b>System Chip Selects</b> (SCS[1:0]), and the lower address lines SA[3:0] are unchanged.  The decoding mode is determined by the state of RA[20] at the trailing edge of the RESET signal. If RA[20] is Low at the trailing edge of RESET, Internal Decoding mode is selected; if RA[20] is High, External Decoding mode is selected.

Table 7. Game and MIDI Port Pins, Crystal Pins

Pin Name	Pin (201)	Type	Description
GAMIN3– GAMIN0	42–45	I, C	The <b>Game Inputs</b> are used to monitor the state of buttons on external joystick(s). The state of these inputs can be read from the Game Control (GGCR) register. These pins are internally pulled up through a nominal 6 k $\Omega$ resistance.
GAMIO3– GAMIO0	46–49	A	The <b>Game I/O</b> pins are used to determine the state of potentiometers on an external joystick to obtain the joystick's X-Y position.
MIDITX	107	B	The <b>MIDI Transmit</b> output is used to send serial digital data from the internal Motorola MC6850-compatible UART.
MIDIRX	106	I	The <b>MIDI Receive</b> input is used to receive serial digital data into the internal Motorola MC6850-compatible UART.
XTAL1I	100		<b>Crystal 1 Input</b> . Input from the 24.576 MHz crystal. The clock used by the codec module to support select sampling rates is derived from the 24.576 MHz crystal attached to the XTAL1 pins. An external 24.576 MHz CMOS-compatible clock is not supported.
XTAL1O	101		<b>Crystal 1 Output</b> . Output from the 24.576 MHz crystal.
XTAL2I	104		<b>Crystal 2 Input</b> . Input from the 16.9344 MHz crystal. The main clocks used throughout the IC are derived from the 16.9344 MHz crystal attached to the XTAL2 pins. An external 16.9344 MHz CMOS-compatible clock is not supported.
XTAL2O	103		<b>Crystal 2 Output</b> . Output from the 16.9344 MHz crystal.

Table 8. Power Supply Pins

Pin Name	Pin (201)	Type	Description
AVCC	12, 17, 26, 33	P	<b>Analog Power</b> . Supplies power to analog portions of the InterWave IC. To avoid latch up, AVCC must be within 0.5V of VCC at all times. To guarantee this, AVCC and VCC should be driven from the same source.
VCC	6, 39, 55, 75, 82, 91, 105, 114, 115, 134, 146	P	<b>Digital Power</b> . Supplies power to digital portions of the InterWave IC.
AVSS	7, 8, 11, 16, 18, 23, 28, 32, 34	P	<b>Analog Ground</b> . Supplies ground reference to analog portions of the InterWave IC.
VSS	40, 50, 51, 62, 73, 96, 102, 110, 120, 133, 141, 147, 157	P	<b>Digital Ground</b> . Supplies ground reference to digital portions of the InterWave IC.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . .  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
Ambient Temperature Under Bias .  $-65^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Supply Voltage VCC to VSS . . . . .  $-0.5\text{ V}$  to  $+7\text{ V}$   
All digital inputs within  
the range . . . . .  $-0.5\text{ V}$  to  $\text{VCC} + 0.5\text{ V}$   
All analog inputs within  
the range . . . . .  $-0.5\text{ V}$  to  $\text{AVCC} + 0.5\text{ V}$   
Supply voltage . . . . .  $\text{AVCC}$  to  $\text{AVSS} - 0.5\text{ V}$  to  $+7\text{ V}$   
Supply voltage . . . . .  $\text{VCC}$  to  $\text{AVCC} \pm 0.5\text{ V}$   
Supply voltage . . . . .  $\text{VSS}$  to  $\text{AVSS} \pm 0.5\text{ V}$

*Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Ambient Temperature . . . . .  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$   
VCC . . . . .  $4.75\text{ V}$  to  $5.25\text{ V}$  or  $3.0\text{ V}$  to  $3.6\text{ V}$   
AVCC . . . . .  $4.75\text{ V}$  to  $5.25\text{ V}$  or  $3.0\text{ V}$  to  $3.6\text{ V}$

## ELECTRICAL CHARACTERISTICS over COMMERCIAL operating ranges

Table 9. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
TTL-Compatible Input Voltage ( $\text{VCC} = 4.75\text{ V}$ to $5.25\text{ V}$ ) All Digital Inputs ( $\text{VCC} = 3.0\text{ V}$ to $3.6\text{ V}$ )						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.0		$\text{VCC} + 0.5$	V
CMOS-Compatible Input Voltage ( $\text{VCC} = 4.75\text{ V}$ to $5.25\text{ V}$ )						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		3.7		$\text{VCC} + 0.5$	V
Digital Output Voltage						
VOL	Output Low Voltage				0.5	V
VOH	Output High Voltage		2.4			V
Digital Leakage Current						
IIX	Input Leakage Current		$-10$		10	$\mu\text{A}$
IOZL	Output Low Leakage Current		$-10$			$\mu\text{A}$
IOZH	Output High Leakage Current				10	$\mu\text{A}$
Crystal Input						
FCK1	Crystal 1 Frequency			24.576		MHz
FCK2	Crystal 2 Frequency			16.9344		MHz
Power Supply Current						
	Total Operating Current (Digital and Analog)	Note 2		140	TBD	mA
	Analog Operating Current	Note 1		65	TBD	mA
	Digital, Suspend	Note 1	100	200	500	$\mu\text{A}$

### Notes:

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. All applicable output pins are three-stated.

**Table 10. Maximum Drive Table For VOL and VOH Specifications, VCC = 5 V**

Signals	Load Cap. (pF)	IOL (mA)	IOH (mA)	Notes
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	240	24	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	120	12	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	60	3	-3	1, 2
DRQ[7:5,3,1:0], IRQ[15,12,11,7,5,3,2], GPOUT[1:0]	120	5	-3	2
PNPCS, $\overline{\text{CD\_CS}}$ , $\overline{\text{CD\_DAK}}$ , CD_IRQ, MIDITX, $\overline{\text{RAHLD}}$ , $\overline{\text{EFFECT}}$ , $\overline{\text{FRSYNC}}$	50	3	-3	3
MA[10:0], MD[7:0], $\overline{\text{BKSEL}}[3:0]$ , $\overline{\text{ROMCS}}$ , RA[21:20], $\overline{\text{MWE}}$ , $\overline{\text{RAS}}$	120	3	-3	

**Notes:**

1. The maximum drive capability for these signals is selectable via programmable register. See the InterWave Programmer's Guide.
2. There is no IOH value for the open collector outputs.
3.  $\overline{\text{EFFECT}}$  and  $\overline{\text{FRSYNC}}$  are multiplexed with the  $\overline{\text{SUSPEND}}$  and C32KHz inputs. Also, CD\_IRQ can be selected as the output ESPCLK.

**Table 11. Maximum Drive Table For VOL, VOH Specifications, VCC = 3.3 V**

Signals	Load Cap. (pF)	IOL (mA)	IOH (mA)	Notes
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	60	TBD	TBD	2
DRQ[7:5,3,1:0], IRQ[15,12,11,7,5,3,2], GPOUT[1:0]	60	TBD	TBD	2
PNPCS, $\overline{\text{CD\_CS}}$ , $\overline{\text{CD\_DAK}}$ , CD_IRQ, MIDITX, $\overline{\text{RAHLD}}$ , $\overline{\text{EFFECT}}$ , $\overline{\text{FRSYNC}}$	50	TBD	TBD	3
MA[10:0], MD[7:0], $\overline{\text{BKSEL}}[3:0]$ , $\overline{\text{ROMCS}}$ , RA[21:20], $\overline{\text{MWE}}$ , $\overline{\text{RAS}}$	80	TBD	TBD	

**Notes:**

1. The maximum drive capability for these signals is selectable via programmable register. See the InterWave Programmer's Guide.
2. There is no IOH value for the open collector outputs.
3.  $\overline{\text{EFFECT}}$  and  $\overline{\text{FRSYNC}}$  are multiplexed with the  $\overline{\text{SUSPEND}}$  and C32KHz inputs. Also, CD\_IRQ can be selected as the output ESPCLK.

**Table 12. Electrical Characteristics**

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
A/D							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range		80	85		dB	
THD	Total Harmonic Distortion				0.02	%	
	Signal-to-Intermodulation Distortion			90			1
	Offset Error				TBD	bits	1
	Gain Error				TBD	%	
Mixer Inputs							
	Full Scale Input Voltage			2.9		Vp-p	
	Input Resistance		20			k $\Omega$	1
	Input Capacitance				15	pF	1

Table 12. Electrical Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
	Interchannel Isolation						
	Line-Line		75	80		dB	
	Line-Mic		75	80		dB	
	Line-Aux1		75	80		dB	
	Line-Aux2		75	80		dB	
	Interchannel Gain Mismatch				±0.5	dB	
	Programmable Gain Range (CLICI)			22.5		dB	3
	Programmable Gain Step Size (CLICI)			1.5		dB	3
	Programmable Gain Range (CLOAI)			46.5		dB	3
	Programmable Gain Step Size (CLOAI)			1.5		dB	3
	Programmable Gain Range (CMONOI)			45.0		dB	3
	Programmable Gain Step Size (CMONOI)			1.5		dB	3
Mixer Outputs							
	Full Scale Output Voltage, OFVS = 1	measured at LINEOUT		2.9		Vp-p	
	Full Scale Output Voltage, OFVS = 0	measured at LINEOUT		2.0		Vp-p	
	External Load Impedance	LINEOUT, MONOOUT	5.0			kΩ	2
	External Load Capacitance				100	pF	
	Audible Out-of-Band Energy 0.6 Fs to 20 kHz	measured at Fs = 8 kHz		-70		dB	1
	Mute Attenuation		80			dB	
	AREF Drive		-0.25		3.0	mA	
	AREF Level			2.5		V	
	Programmable Gain Range (CLCI, CLDACI)			94.5		dB	3
	Programmable Gain Step Size			1.5		dB	
	Line-to-Line Interchannel Isolation	measured at LINEOUT	75	80		dB	
	Interchannel Gain Mismatch				±0.5	dB	
Synthesizer D/A							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range			85		dB	1
THD	Total Harmonic Distortion			0.01	0.02	%	1
	Signal-to-Intermodulation Distortion			85			1
	Gain Error				±0.5	dB	1
Codec D/A							
	Resolution			16		bits	
IDR	Instantaneous Dynamic Range		80	85		dB	
THD	Total Harmonic Distortion			0.01	0.02	%	

**Table 12. Electrical Characteristics (continued)**

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
	Signal-to-Intermodulation Distortion			85			1
	Gain Error		−0.5		0.5	dB	
	Deviation from Linear Phase			1	Degree		1
Game Port							
	Joystick Trim DAC Threshold				TBD	V	
	Joystick Trim DAC Step Size				TBD	V	

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. Outputs AC coupled.
3. See *InterWave Programmer's Guide*.

**Table 13. Digital Filter Characteristics—Playback**

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		±0.1	dB	1
	Transition Band		.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		−107	dB	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

**Table 14. End-To-End Frequency Characteristics—Playback (Measured at LINEOUT)**

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	±0.2	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

**Table 15. Digital Filter Characteristics—Record**

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		0.1	dB	1
	Transition Band		0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		–100	dB	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

**Table 16. End-To-End Frequency Characteristics—Record**

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	±0.2	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1



Table 17. Switching Characteristics

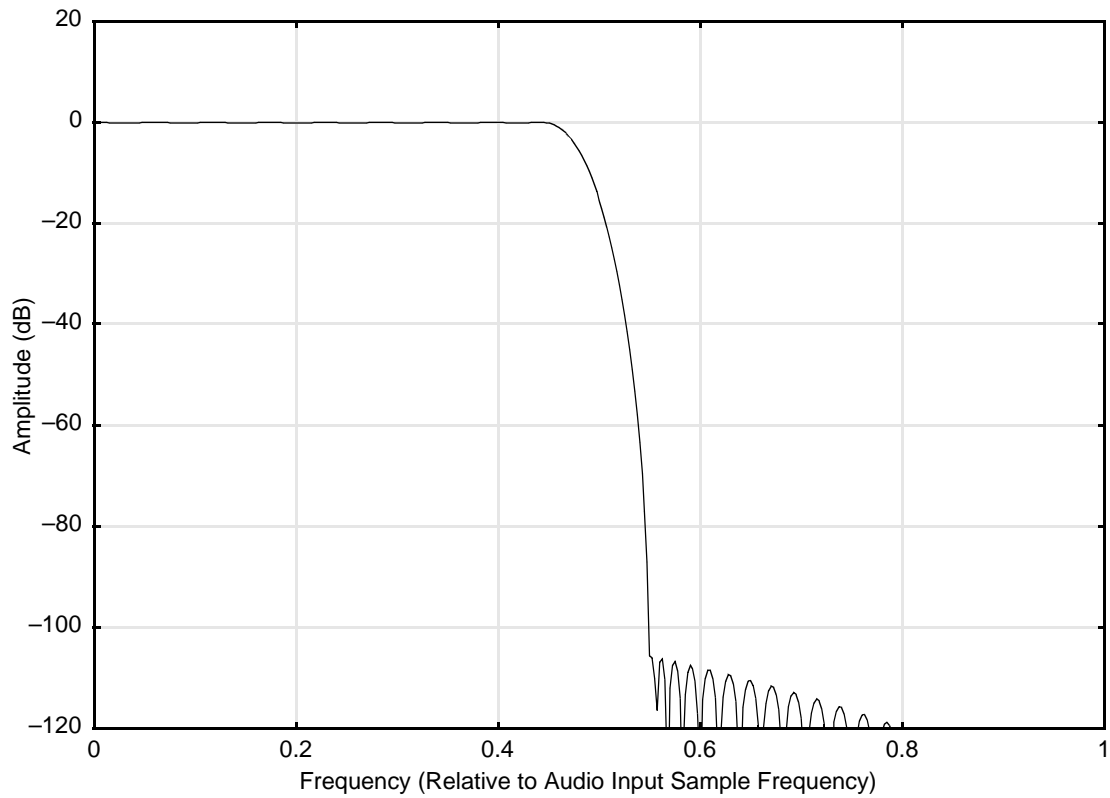
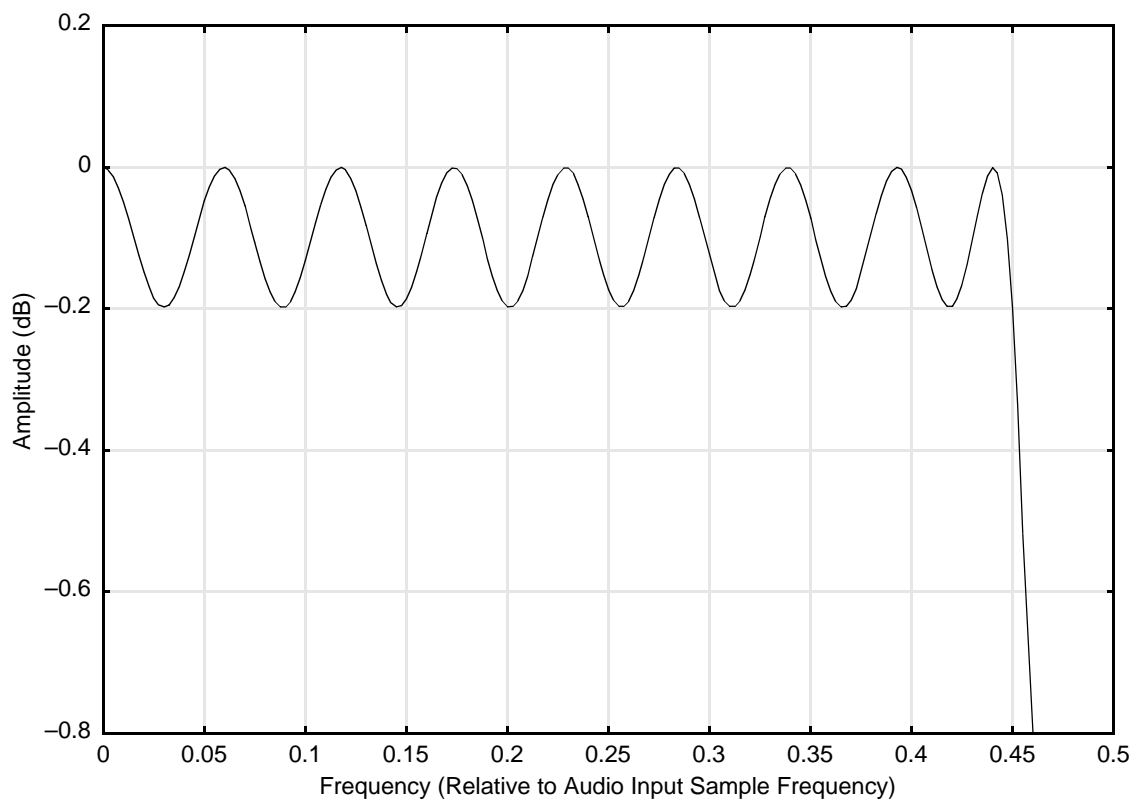
Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit	Notes
System Control						
$t_{AS}$	Address Setup		88		ns	
$t_{AH}$	Address Hold		32		ns	
$t_{AR}$	Address Recovery		152		ns	
$t_{SW}$	Read or Write Strobe Width		TBD		ns	
$t_{DDW}$	Data Delay (Write)			61	ns	
$t_{DHW}$	Data Hold (Write)			25	ns	
$t_{DDR}$	Data Delay (Read)			103	ns	
$t_{DHR}$	Data Hold (Read)		0		ns	
$t_{RD}$	Ready Delay			76	ns	
$t_{ID}$	I/O Delay			116	ns	
$t_{IDD}$	I/O Delay (Read)			59	ns	
Serial Interface						
$f_{SF}$	Serial Clock Frequency			2.1168	MHz	
$t_{SC}$	Serial Clock Period			472	ns	
$t_{SH}$	Serial Clock High		$t_{SC}/2-15$		ns	
$t_{SK}$	Serial Clock Low		$t_{SC}/2-15$		ns	
$t_{SSS}$	Serial Sync Setup		10		ns	
$t_{SSH}$	Serial Sync Hold		10		ns	
$t_{SDS}$	Serial Data In Setup		TBD		ns	
$t_{SDH}$	Serial Data In Hold		TBD		ns	
$t_{SDD}$	Serial Data Out Delay		TBD		ns	
Local Memory Control						
$t_{RAS}$	$\overline{RAS}$ Pulse Width		177		ns	2
$t_{RC}$	Read or Write Cycle Time		236		ns	2
$t_{RP}$	$\overline{RAS}$ Precharge Time		59		ns	2
$t_{RCD}$	$\overline{RAS}$ to $\overline{BKSEL}$ Delay Time			58	ns	2
$t_{RSH}$	$\overline{RAS}$ Hold Time			119	ns	2
$t_{ASR}$	Row Address Setup Time		31		ns	2
$t_{CAS8}$	$\overline{BKSEL}$ Pulse Width		146		ns	2
$t_{RAH}$	Row Address Hold Time		29		ns	2
$t_{ASC}$	Column Address Setup Time		30		ns	2
$t_{CAH}$	Column Address Hold Time		147		ns	2
$t_{RAL}$	Column Address To $\overline{RAS}$ Rising Edge		149		ns	2
$t_{RCS}$	Read Command Setup Time		83		ns	2
$t_{RCH}$	Read Command Hold Time from $\overline{BKSEL}$		59		ns	2
$t_{CRP}$	$\overline{BKSEL}$ to $\overline{RAS}$ Precharge Time		32		ns	2
$t_{DCS}$	Read Data Setup Time		37		ns	
$t_{DCH}$	Read Data Hold Time		50		ns	
$t_{WP}$	Write Pulse Width		179		ns	2
$t_{WCS8}$	Write Command Setup Time		26		ns	2
$t_{WS8}$	Write Data Setup Time		88		ns	
$t_{WH}$	Write Data Hold Time		118		ns	
$t_{CAS16}$	$\overline{BKSEL}$ Pulse Width		60		ns	2
$t_{WCS16}$	Write Command Setup		26		ns	2

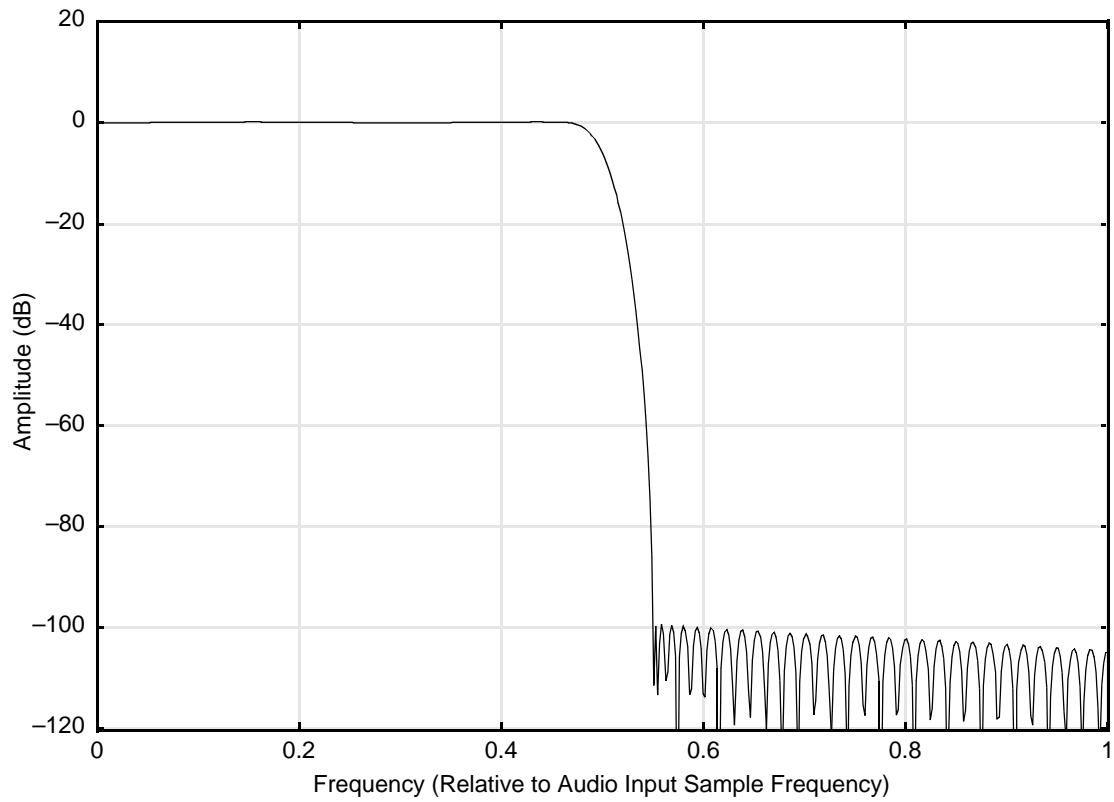
Table 17. Switching Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit	Notes
$t_{WS16}$	Write Data Setup		88		ns	2
DRAM Refresh						
$t_{RPC}$	$\overline{RAS}$ Precharge $\overline{BKSEL}$ Hold Time		61		ns	2
$t_{CP}$	$\overline{BKSEL}$ Recharge Time		32		ns	2
$t_{CSR}$	$\overline{BKSEL}$ Setup Time (Refresh)		50		ns	2
$t_{CHR}$	$\overline{BKSEL}$ Hold Time (Refresh)		60		ns	2
DRAM Suspend Mode Refresh						
$t_{SCD}$	Suspend to $\overline{BKSEL}$ Delay		160		ns	1, 2
$t_{CRD}$	$\overline{BKSEL}$ to $\overline{RAS}$ Delay		31.25		$\mu s$	2
$t_{RW125}$	$\overline{RAS}$ Pulse Width		31.25		$\mu s$	2
$t_{RI125}$	$\overline{RAS}$ Pulse Interval		124.8		$\mu s$	2
$t_{RW62}$	$\overline{RAS}$ Pulse Width		31.2		$\mu s$	
$t_{RI62}$	$\overline{RAS}$ Pulse Interval		62.4		$\mu s$	
ROM Read						
$t_{AS1}$	Address Setup Time (bits 19, 2, 1)		24		ns	2
$t_{AS2}$	Address Setup Time (bits 10–3)		55		ns	2
$t_{AS3}$	Address Setup Time (bits 18–11)		24		ns	2
$t_{AS4}$	Address Setup Time (bits 21–20)		24		ns	2
$t_{AH1}$	Address Hold Time (bits 19, 2, 1)		237		ns	2
$t_{AH2,3}$	Address Hold Time (bits 18–3)		80		ns	2
$t_{RC}$	Read Cycle Time		102		ns	2
$t_{DF}$	Output Disable Time		29		ns	2
$t_{ACE}$	Chip Enable Access Time			239	ns	
$t_{OE}$	Output Enable Access Time			161	ns	
$t_{RDS}$	Read Data Setup Time		58		ns	
$t_{RDH}$	Read Data Hold Time			70	ns	

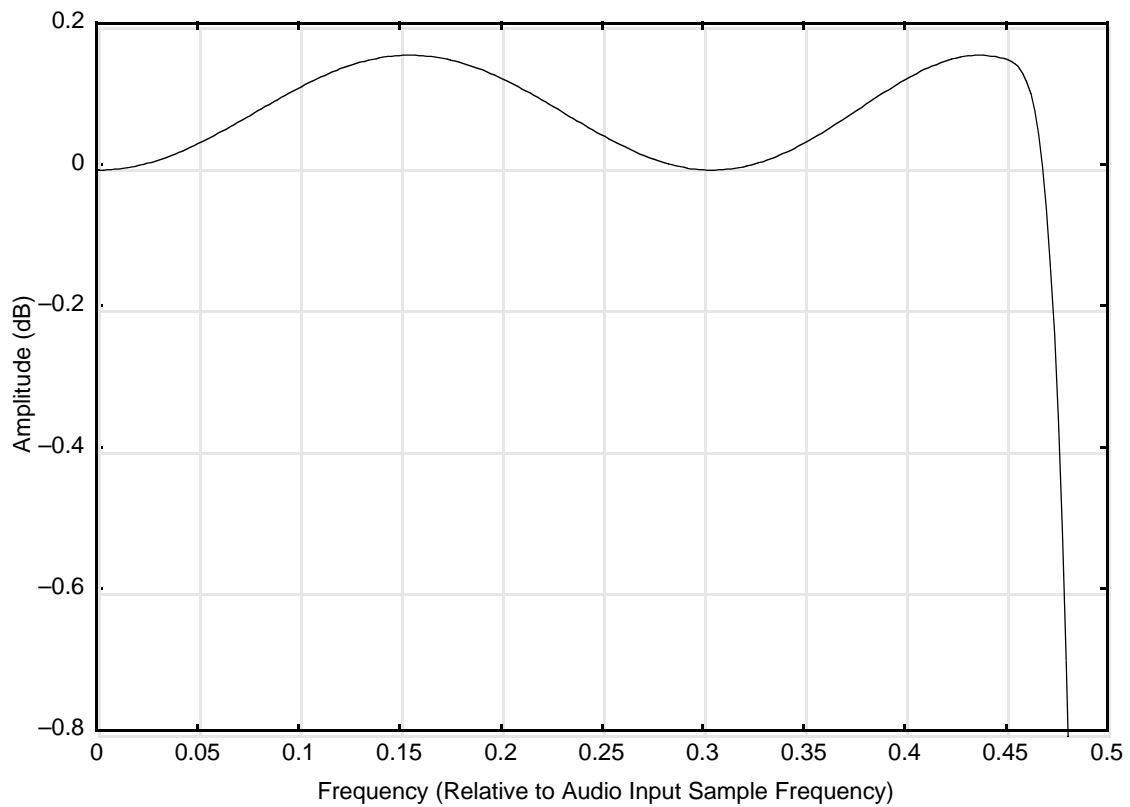
VCC = 5.0 V; Ambient temperature = 25°C.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. XTAL2 frequency = 16.9344 MHz.

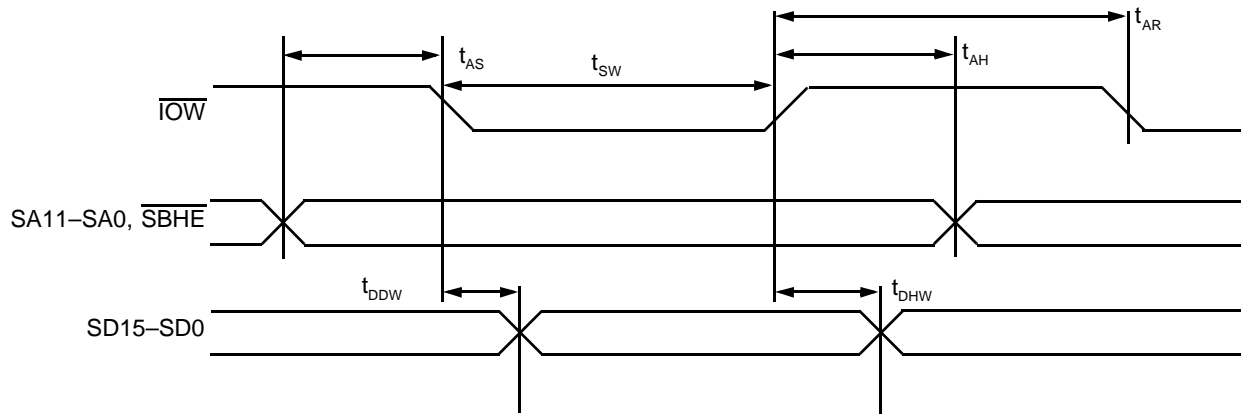
**FILTER RESPONSE****Figure 1. DAC Filter Response****Figure 2. DAC Filter In Band Response**



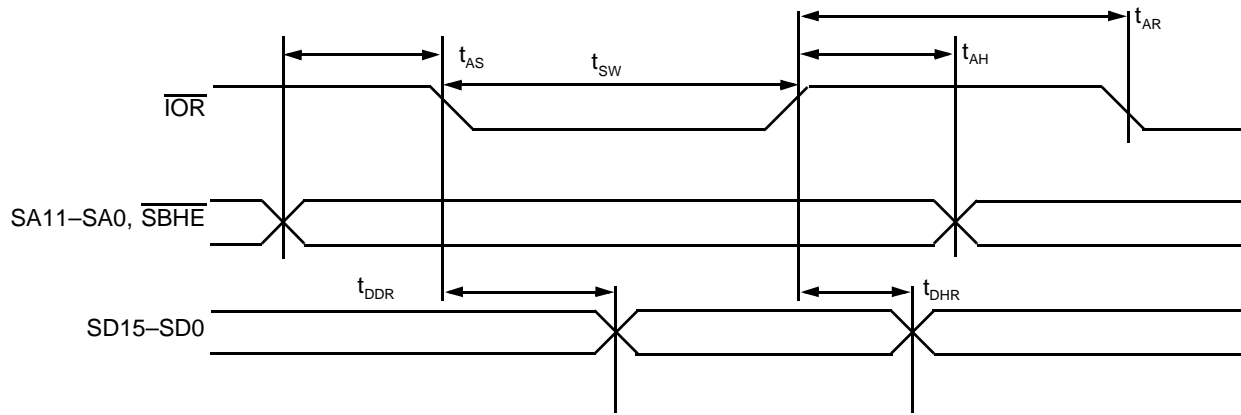
**Figure 3. ADC Filter Response**



**Figure 4. ADC Filter In Band Response**

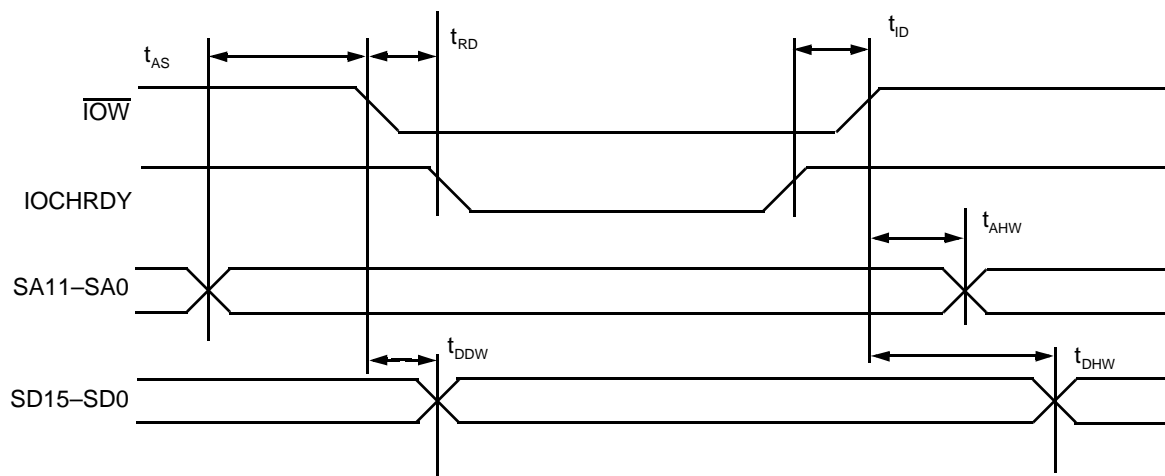


ISA Bus Write Cycle Timing

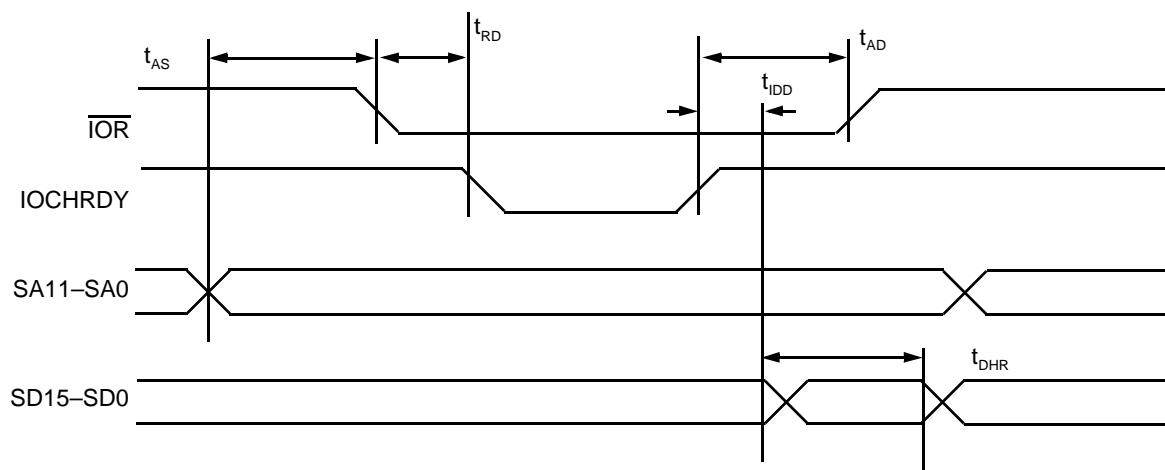


ISA Bus Read Cycle Timing

Figure 5. ISA Bus Cycle Timing

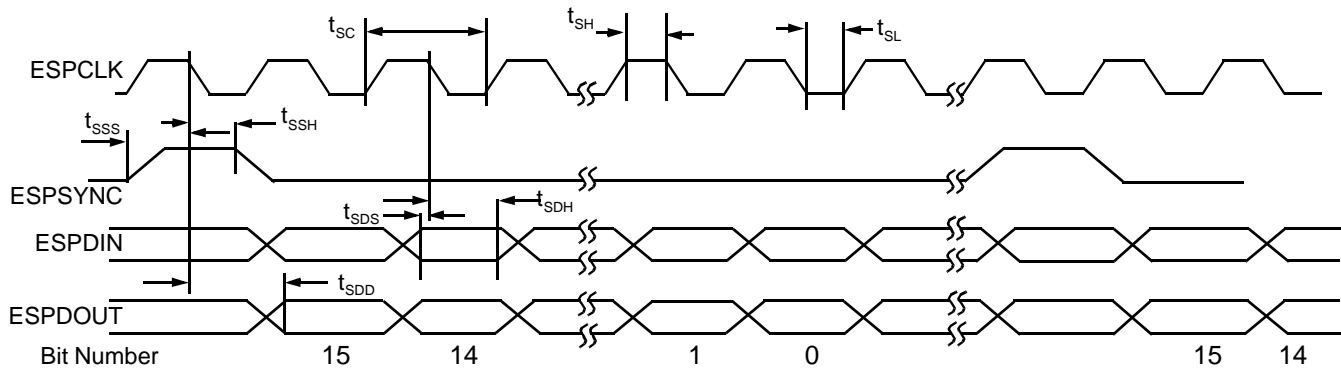


ISA Bus Extended Write Cycle Timing

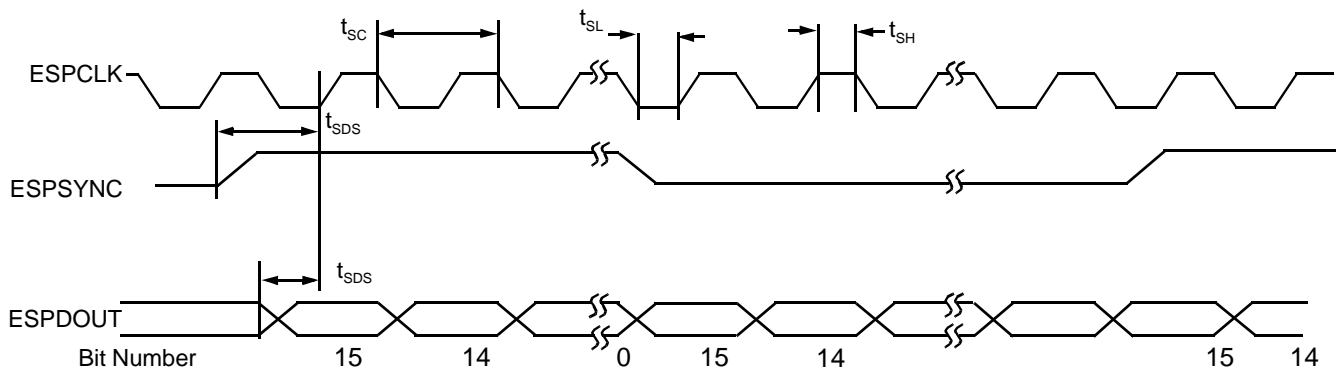


ISA Bus Extended Read Cycle Timing

Figure 6. ISA Bus Extended Cycle Timing



**Figure 7. Serial Port Timing: Record FIFO Output, Playback FIFO Input**



**Figure 8. Serial Port Timing: Synthesizer Output**

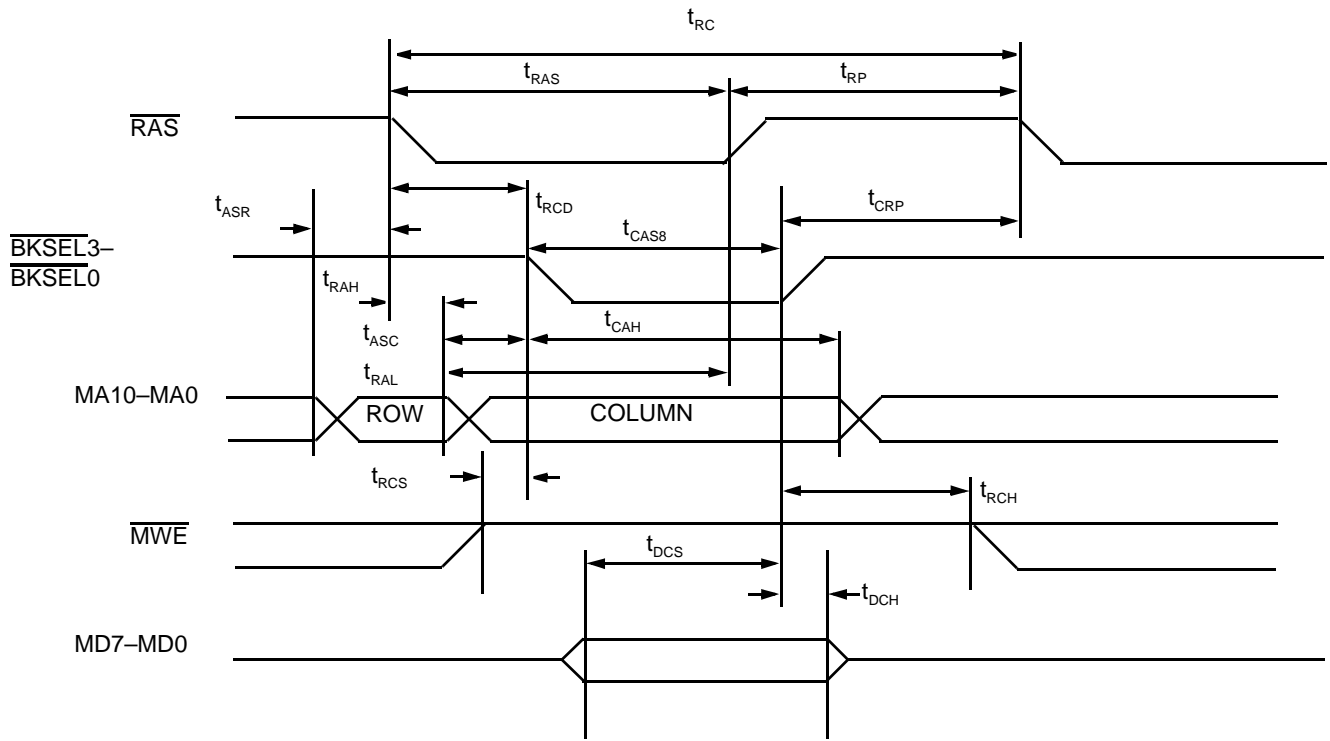


Figure 9. Local Memory: DRAM Read—8 bit

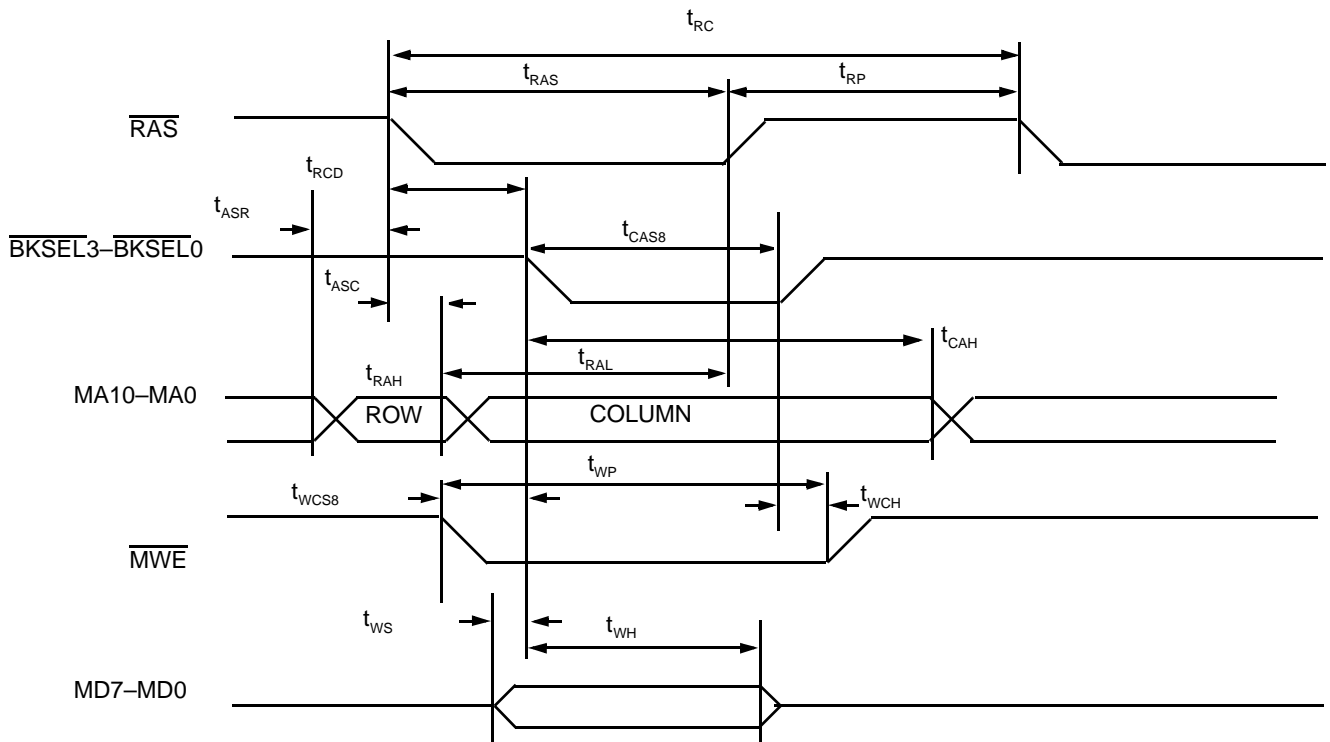


Figure 10. Local Memory: DRAM Write—8 bit



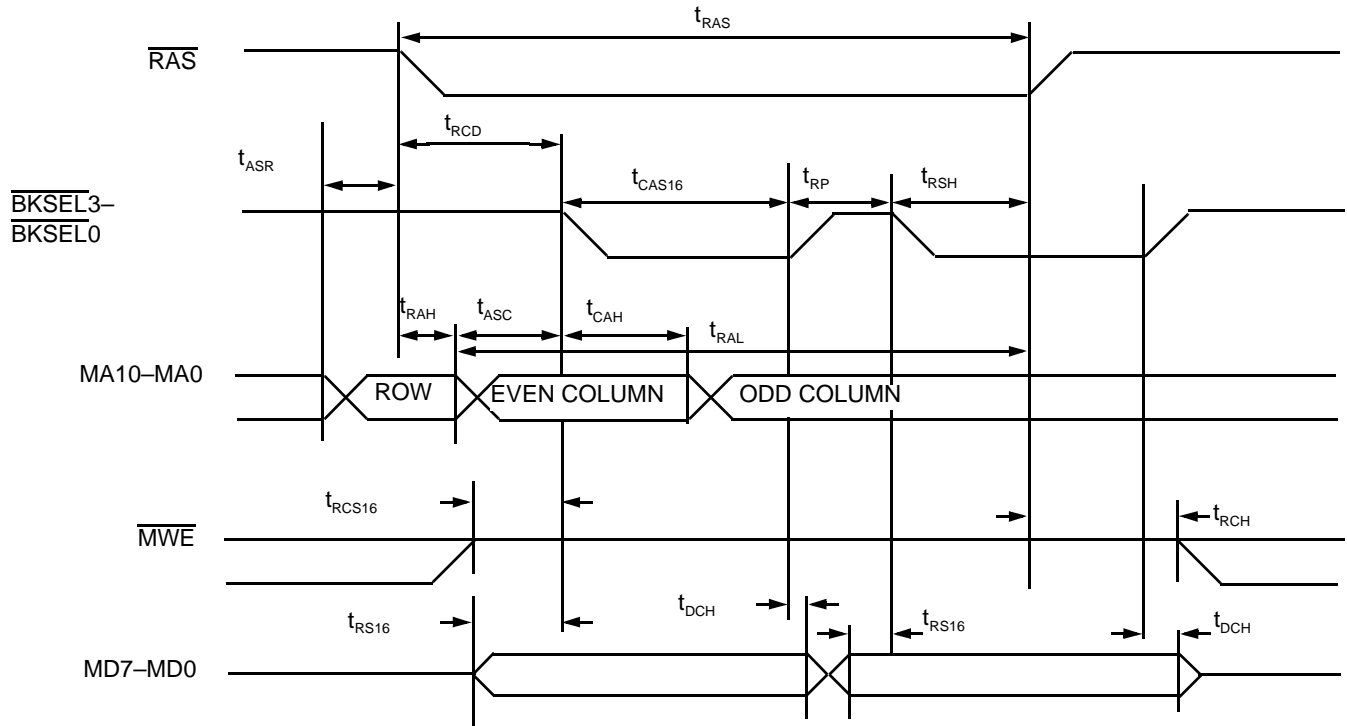


Figure 11. Local Memory: DRAM Read—16 bit

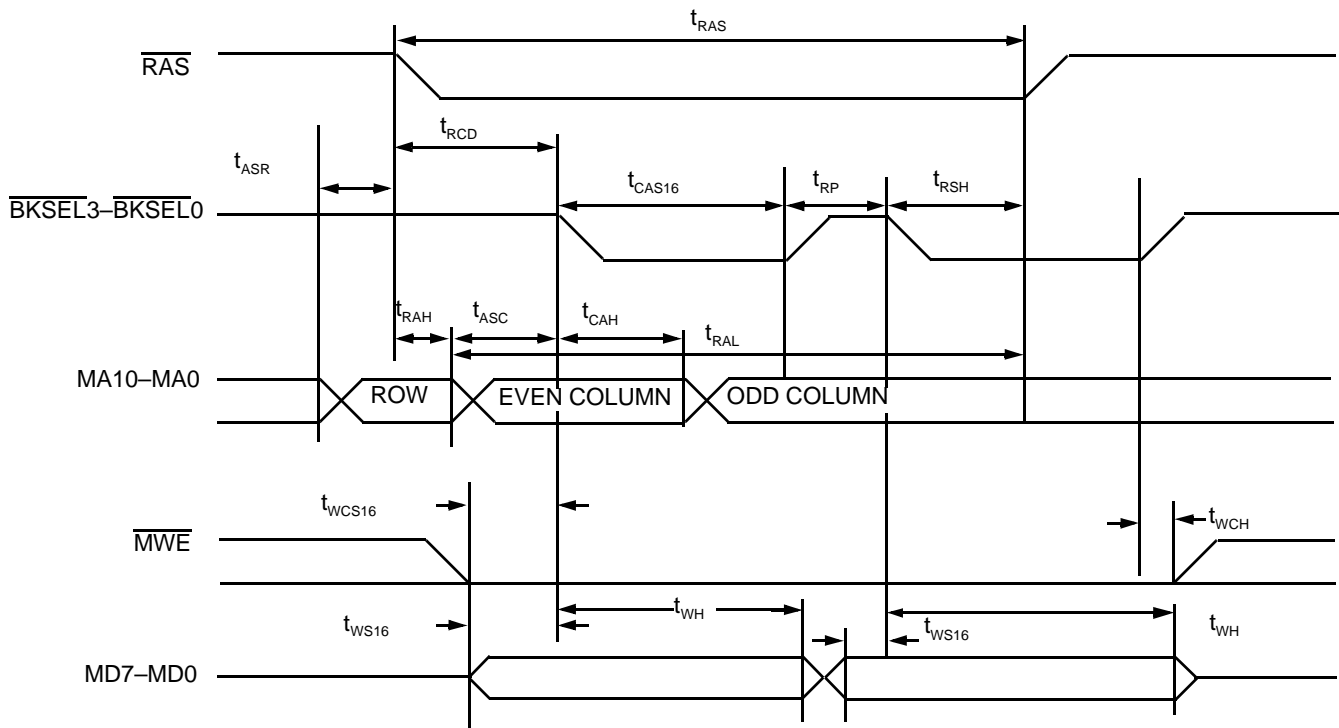


Figure 12. Local Memory: DRAM Write—16 bit

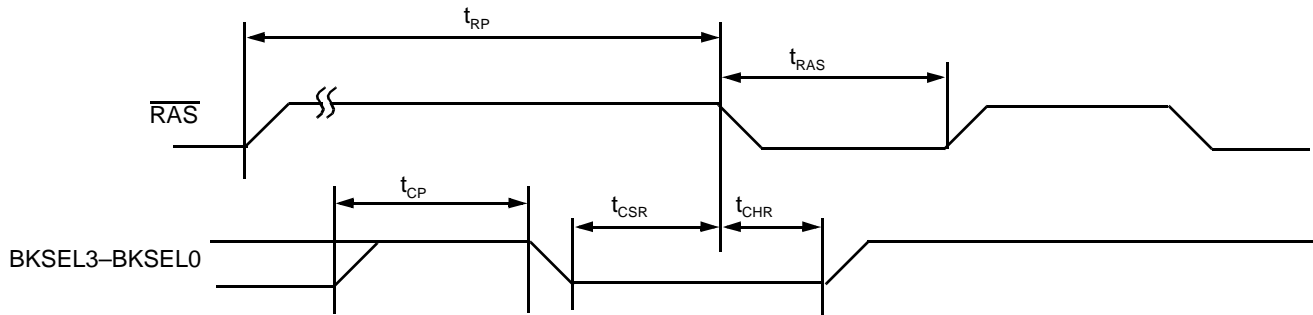


Figure 13. Local Memory: DRAM Refresh ( $\overline{CAS}$  Before  $\overline{RAS}$ )

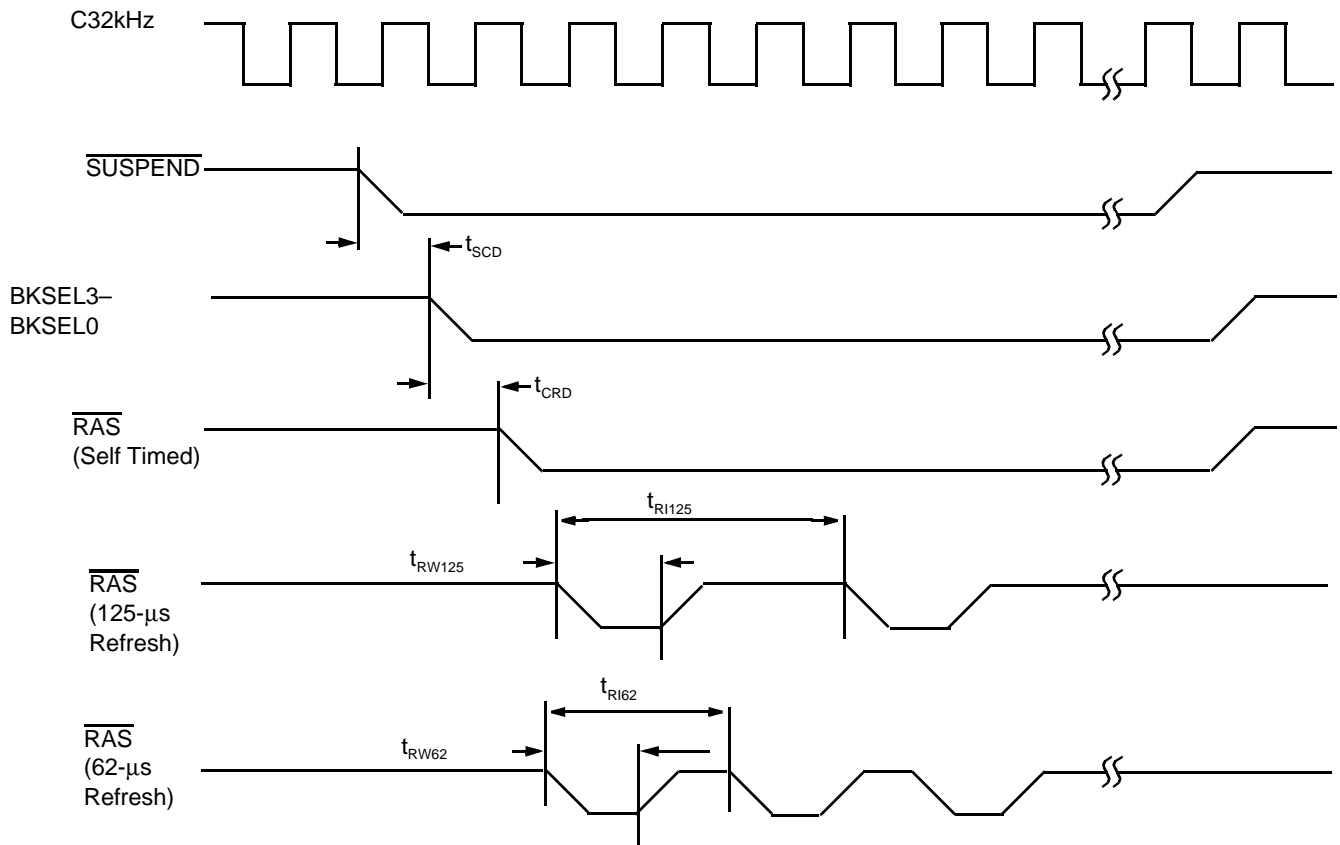


Figure 14. Local Memory: DRAM Refresh (Suspend and Shut Down Modes)

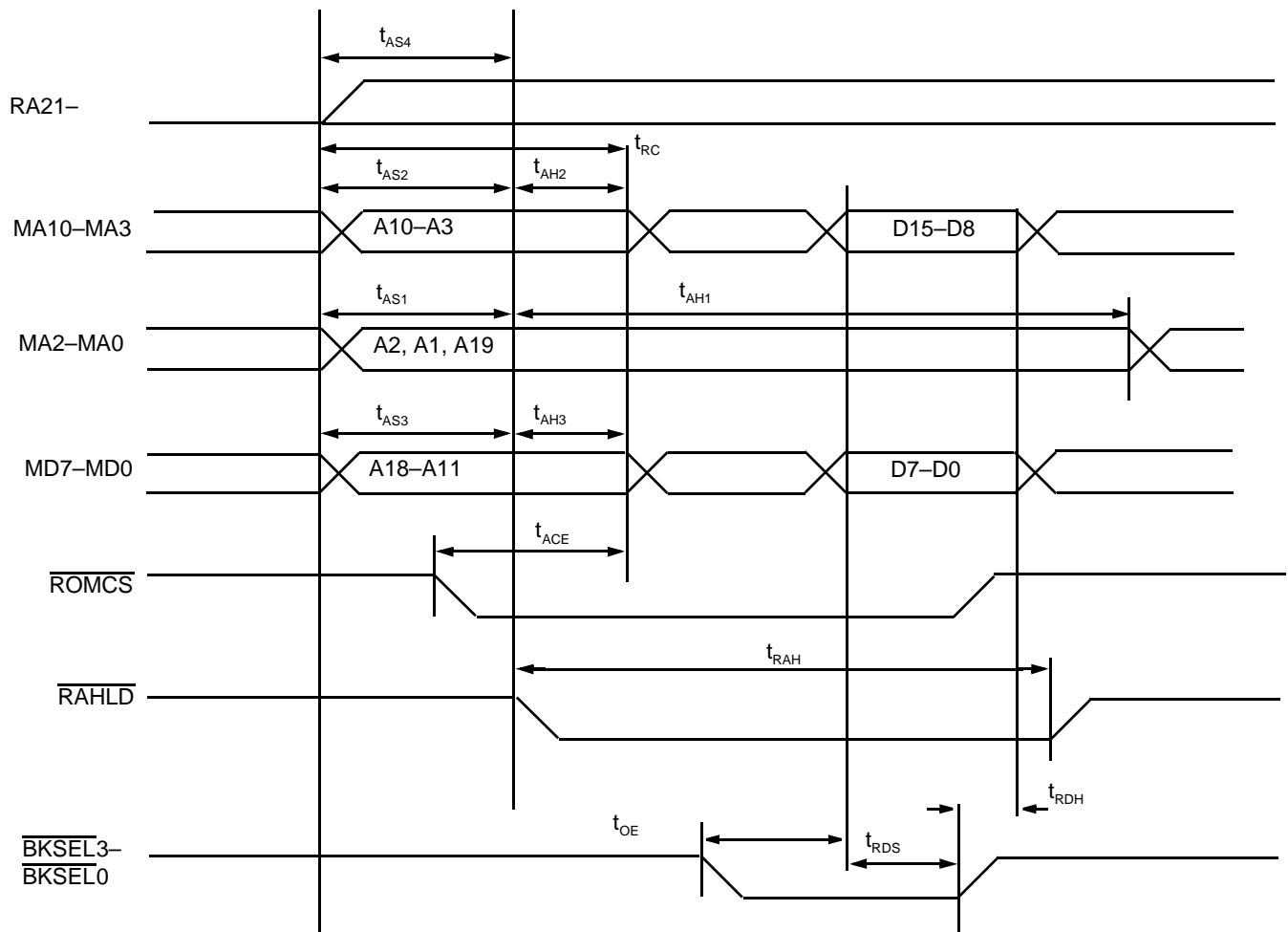
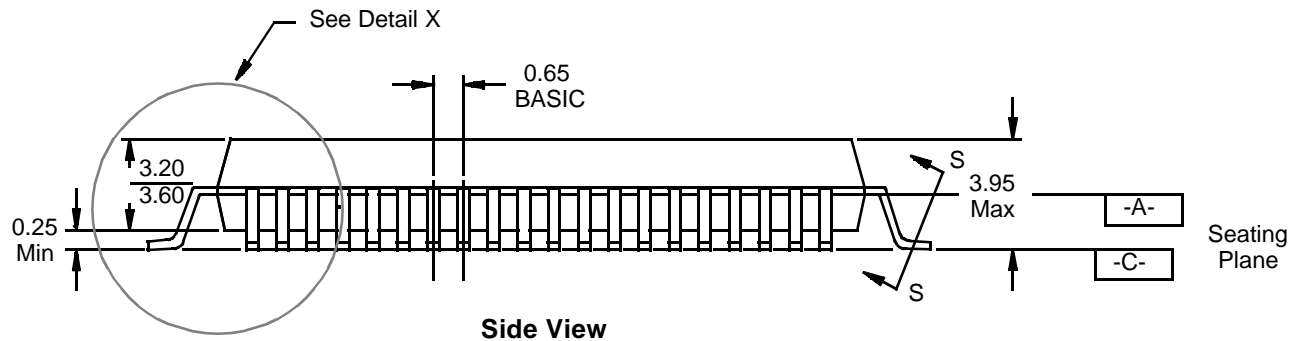
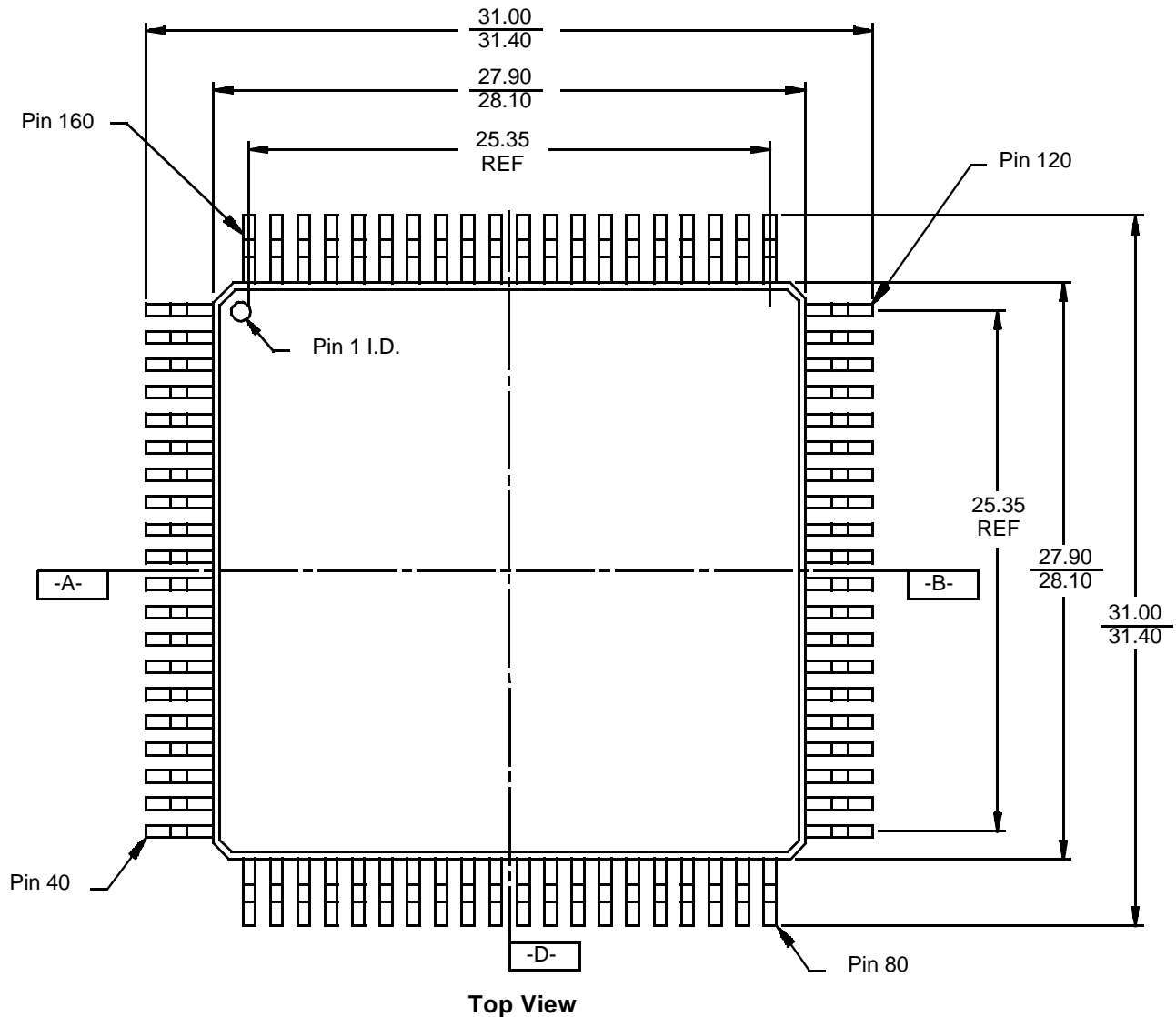


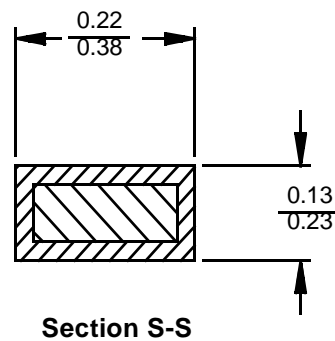
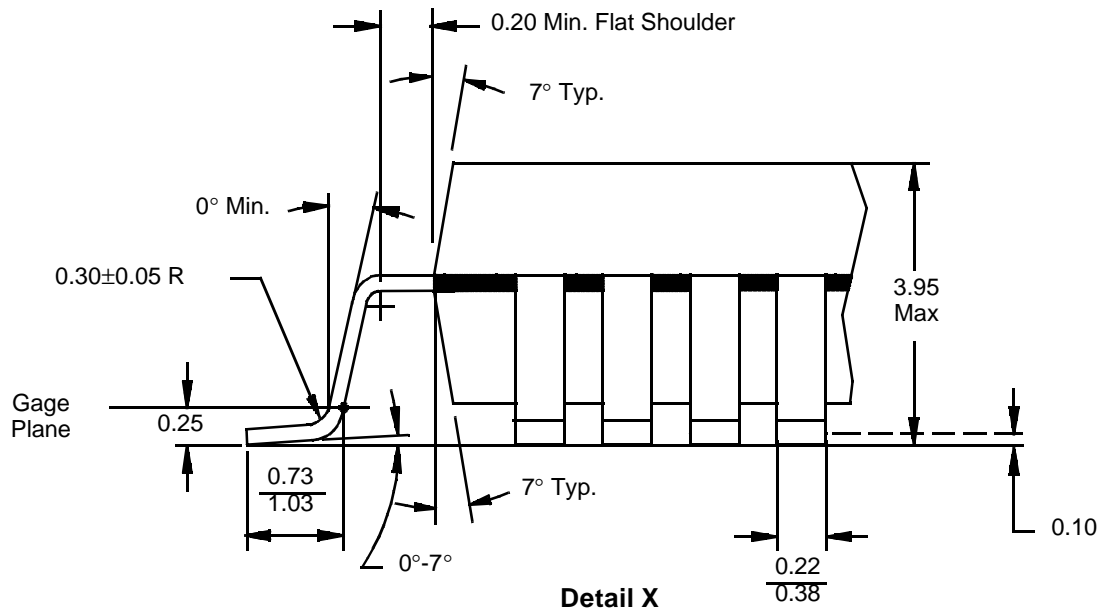
Figure 15. Local Memory: ROM Access

# PQR 160, Trimmed and Formed Plastic Quad Flat Pack



## Notes:

1. All measurements are in millimeters unless otherwise noted.
2. Not to scale; for reference only.

**PQR 160 (continued)****Note:**

1. Not to scale; for reference only.

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