SPECTRUM DIGITAL INCORPORATED

XDS510USB PLUS JTAG Emulator

Technical Reference

2007 ***DSP Development Systems***

XDS510USB PLUS
JTAG Emulator
Installation Guide

509405-0001 Rev. A
January 2007

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TRADEMARKS

Windows 2000, and Windows XP are registered trademarks of Microsoft Corp.

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About This Manual

This document describes the module level operations of the XDS510USB PLUS JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The XDS510USB PLUS JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The XDS510USB PLUS JTAG Emulator will sometimes be referred to as the XDS510USB PLUS, JTAG Emulator, or Emulator.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer and Code Composer Studio Users Guide

Chapter 1

Introduction to the XDS510USB PLUS JTAG Emulator

This chapter provides you with a description of the XDS510USB PLUS JTAG Emulator along with the key features.

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1.0 Overview of the XDS510USB PLUS JTAG Emulator

The XDS510USB PLUS JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate with +1.8 to +5 volt levels on the JTAG interface This emulator is powered from USB line. This means no power is drawn from the target system.

1.1 Key Features of the XDS510USB PLUS JTAG Emulator

The XDS510USB PLUS JTAG Emulator has the following features:

- Supports Texas Instrument's Digital Signal Processors (C2xxx, C54xx, C55xx, C67xx, C64xx, TMS470, OMAP) with JTAG interface (IEEE 1149.1)
- Compatible with Spectrum Digital XDS510 USB and XDS510 USB Galvanic JTAG emulators, and SDConfig, SDFlash, and other Spectrum Digital utilities.
- Advanced emulation controller provides higher performance.
- Compatible with USB 1.x and USB 2.0 (high speed)
- Power provided by host USB port or USB hub
- Supports USB interface with host PC, no adapter card required.
- Supports +1.8 to +5 volt JTAG interfaces.
- Replacable cables (compatible with Spectrum Digital's XDS560R).
- Reset switch.
- Programmable TCK frequency up to 32 Mhz.
- ARM Ltd. style Adaptive Clocking support.
- Programmable EMU0/1 pins support for boundary scan test support.
- One status LED for operational status.
- Compatible with Texas Instruments Code Composer Studio
- Compatible with Spectrum Digital's Flash programming utility
- Compatible with Windows 2000, and Windows XP Operating Systems

1.2 Key Items on the XDS510USB PLUS JTAG Emulator

Figure 1-1 shows the XDS510USB PLUS. The key items identified are:

- Status LEDs
- JTAG connector
- Tail - XDS560R compatible
- USB connector to the host PC or hub
- Reset switch

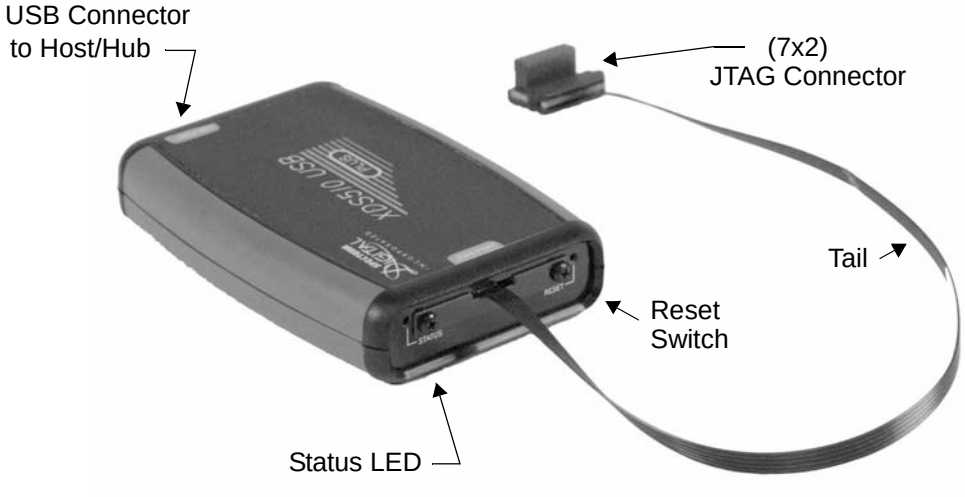

Figure 1-1, KEY ITEMS ON THE XDS510USB PLUS

Chapter 2

Installing the XDS510USB PLUS JTAG Emulator

This chapter helps you install the XDS510USB PLUS JTAG Emulator. For use with specific software packages such as the TI's Code Composer Studio refer to their respective documentation.

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2.1 What You'll Need

The following checklists detail items that are shipped with the XDS510USB PLUS JTAG emulator and additional items you'll need to use these tools.

Hardware checklist

__	**host**	An IBM PC/AT or 100% compatible PC or laptop with a hard-disk system and CD-ROM disk drive with a USB port
__	**memory**	Minimum of 32MB
__	**display**	Color VGA or LCD
__	**emulator module**	XDS510USB PLUS JTAG emulator
__	**target system**	A board with a TI DSP or Microcontroller and power supply
__	**connector to target system**	14-pin connector (two rows of seven pins) --- see Chapter 3 for more information about this connector

Software checklist

__	**operating system**	Windows 2000, Windows XP
__	**software tools**	Compiler/assembler/linker for DSP or Microcontroller
__	**debugger**	Code Composer or Code Composer Studio
__	**drivers**	Spectrum Digital drivers for TI Code Composer (included with XDS510USB PLUS emulator or available from Spectrum Digital's website)

2.2 Installing the XDS510USB PLUS JTAG Emulator

This section contains the steps for installing the XDS510USB PLUS JTAG Emulator.

WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

2.2.1 XDS510USB PLUS Installation Checklist

To install the XDS510USB PLUS JTAG emulator execute the following checklist:

❏ Turn off the power to your target board.

❏ Insert the Spectrum Digital USB Driver CD-ROM in the computers CD-ROM drive and install the device drivers. Code Composer/Studio should be installed already.

❏ Connect the supplied USB cable to your PC or laptop. If you connect the USB cable to a USB hub be sure the hub is connected to the PC or laptop and power is applied to the hub.

❏ Connect the supplied USB cable to your XDS510USB PLUS emulator.

❏ Your system configuration should now look like that in Figure 2-1or Figure 2-2 After a few moments windows will detect new hardware and prompt you with "New Hardware Found" screens. Follow the instructions on the screens and let Windows find the USB driver files "sd540u2.inf" and sdusbemu.sys" on your CD-ROM drive.

If you want to verify a successful USB driver install, right mouse on Control Panel, then select Properties -> Hardware -> Device Manager. You should see a new class "SD USB Based Debug Tools" and one Spectrum Digital XDS510USB PLUS emulator installed.

❏ Now connect the tail of the emulator to the 2 x 7 header on your target board. Apply power to the target board

Figures 2-1 and 2-2 show two typical configurations in which the XDS510USB PLUS can be used with a host PC and target board.

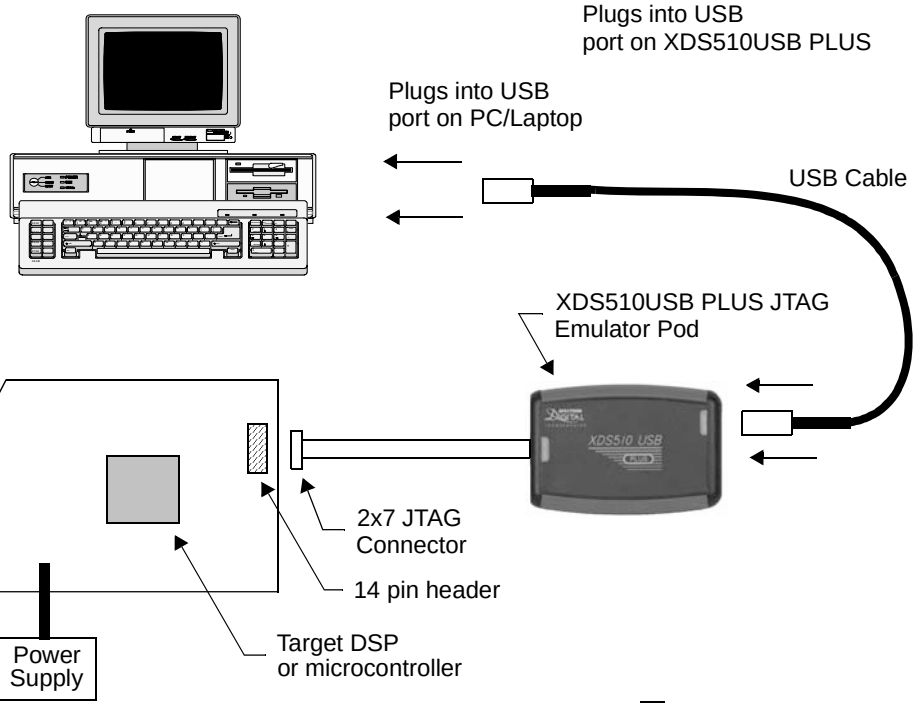

Figure 2-1, Connecting the XDS510USB PLUS To Your Target System

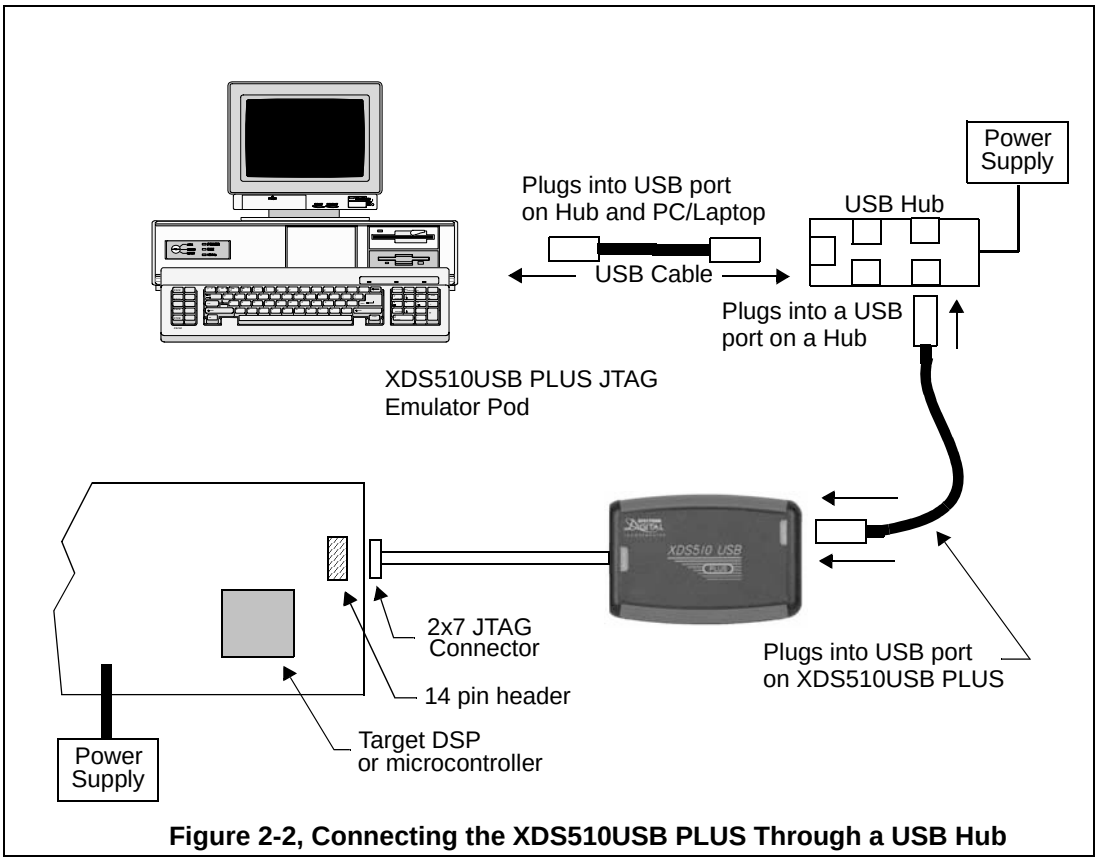

Figure 2-2, Connecting the XDS510USB PLUS Through a USB Hub

2.3 XDS510USB PLUS LED

The XDS510USB PLUS has one (1) red Light Emitting Diode (LED). This LED provides the user with the status of the emulator. The meaning of the LED is described in the table below.

Table 1: XDS510USB PLUS LEDs

LED Name	Function
Status	Indicates activity over the USB Bus

Chapter 3

Specifications For Your Target System's Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14-pin connector for proper communication with the emulator.

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3.1 Designing Your Target System's Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin (2x7) or 20-pin CTI (2x10) connector with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.

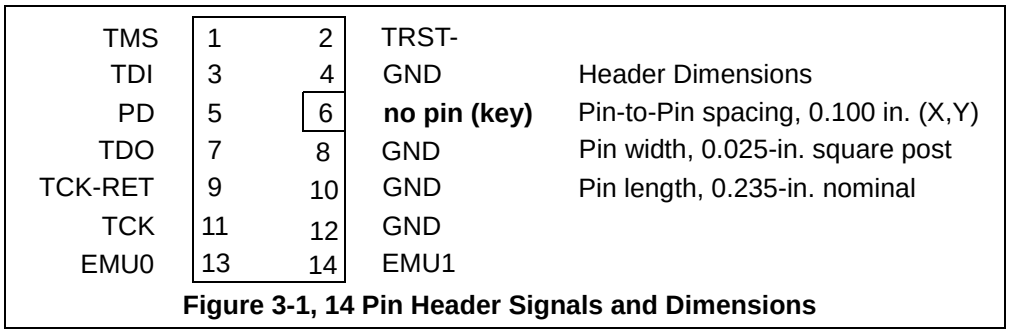

Figure 3-1, 14 Pin Header Signals and Dimensions

Although you can use other 14 pin target headers, recommended parts include:

straight header, unshrouded — DuPont Connector Systems, part # 67996-114
right-angle header, unshrouded — DuPont Connector Systems, part # 68405-114

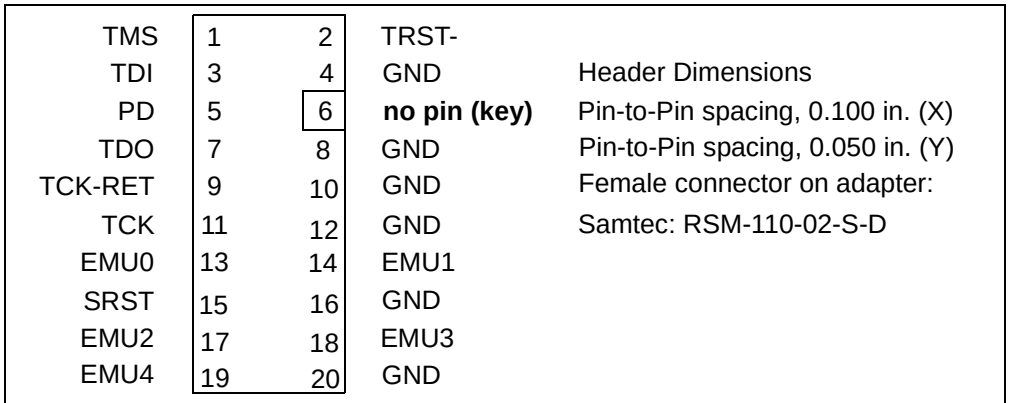

Figure 3-2, 20 Pin Header Signals and Dimensions

A recommended target based 20 pin connector is, SAMTEC part # FTR-110-03-G-D-06

Table 1: 14/20-Pin Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode select.	Output	Input
3	TDI	JTAG test data input.	Output	Input
4,8, 10,12	GND			
7	TDO	JTAG test data output.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
2	TRST-	JTAG test reset.	Output	Input
13	EMU0	Emulation pin 0.	I/O	I/O
14	EMU1	Emulation pin 1.	I/O	I/O
5	PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor's I/O pins Vcc.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output
15	SRST *	ARM style target reset	I/O	Open drain
16	GND			
17	EMU2 *	Emulation pin 2.	I/O	I/O
18	EMU3 *	Emulation pin 3.	I/O	I/O
19	EMU4 *	Emulation pin 4.	I/O	I/O
20	GND			

* Reserved for future emulation software support

3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

- The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

- The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

3.3 Emulator Cable Pod Logic

Figure 3-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

__ Signals TMS and TDI are generated from the rising edge of TCK_RET.

__ Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.

__ A programmable test clock source is provided, you may also provide your own test clock for greater flexibility.

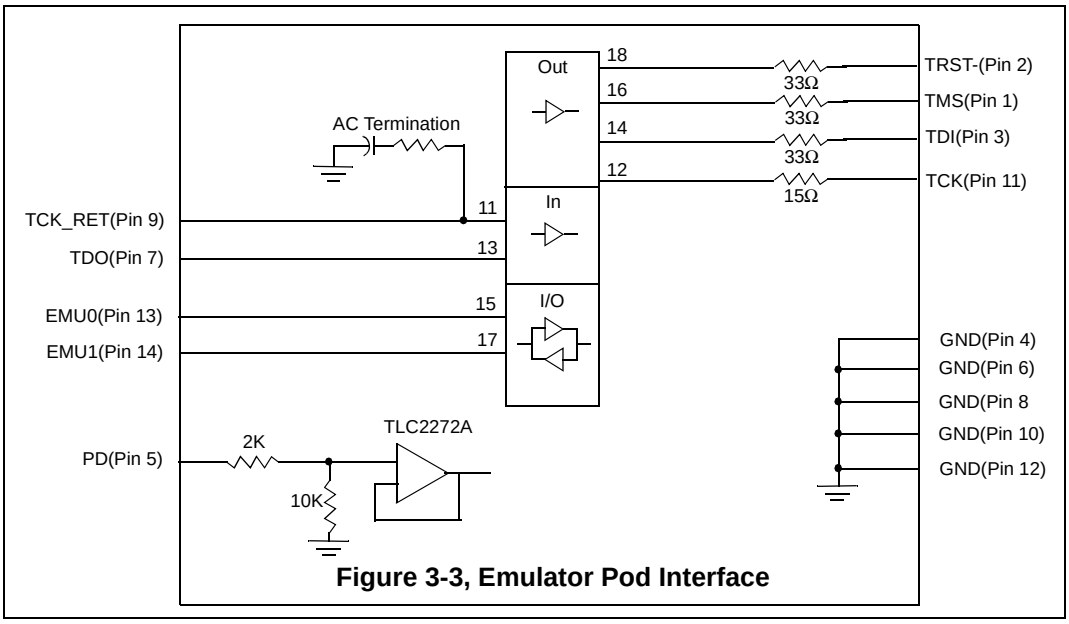

Figure 3-3, Emulator Pod Interface

3.4 Emulator Cable Pod Signal Timing

Figure 3-4 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test or guarantee these timings.
The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

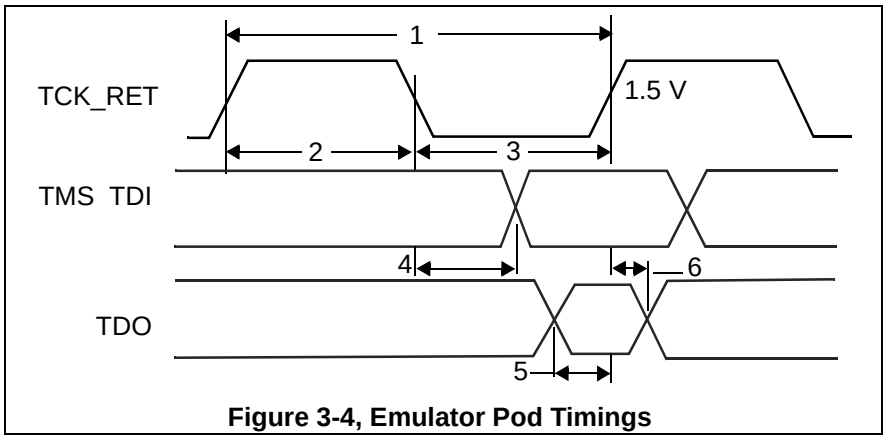

Figure 3-4, Emulator Pod Timings

Table 2: Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	50	10000	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	15		ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	15		ns
4	$td_{(XTMX)}$	TMS/TDI valid from TCK_RET low	5	22	ns
5	$tsu_{(XTDOmin)}$	TDO setup time to TCK_RET high	5		ns
6	$thd_{(XTDOmin)}$	TDO hold time from TCK_RET high	5		ns

3.5 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

__ **No signal buffering.** As shown in figure 3-5, the distance between the header and the target device should be no more than 6 inches.

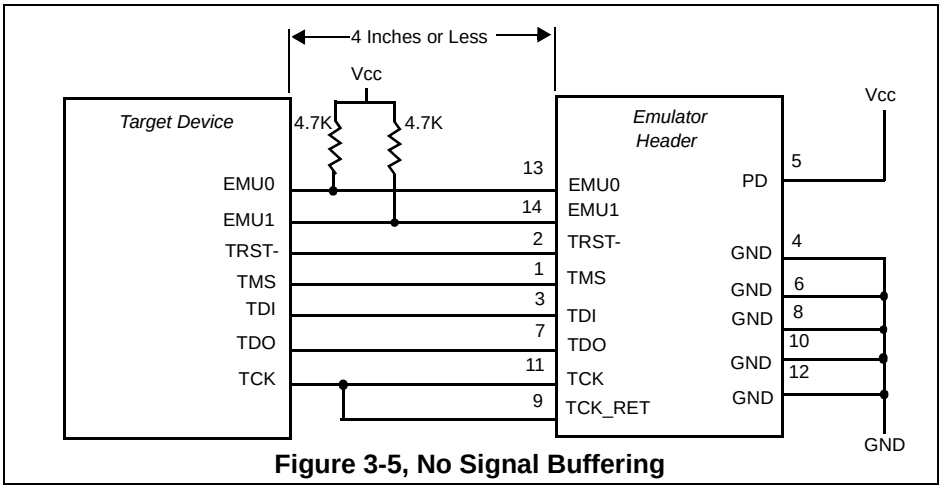

Figure 3-5, No Signal Buffering

__ **Buffered emulation signals.** Figure 3-6 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.

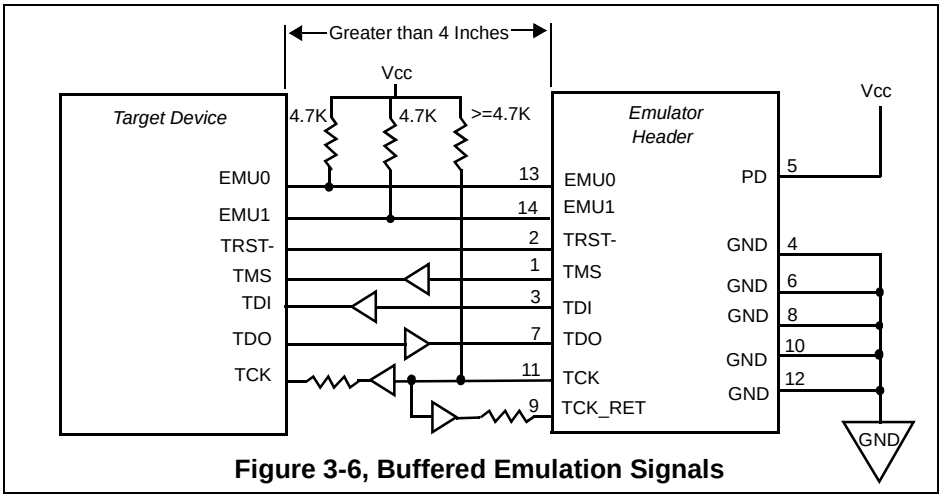

Figure 3-6, Buffered Emulation Signals

— The EMU0 and EMU1 signals must have pullups to Vcc. The pullup resistor value should be chosen to provide a signal rise time less than 10 uS. A 4.7k ohm resistor is suggested for most applications. EMU0-1 are I/O pins on the target device, however, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.

— It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 3-7 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.

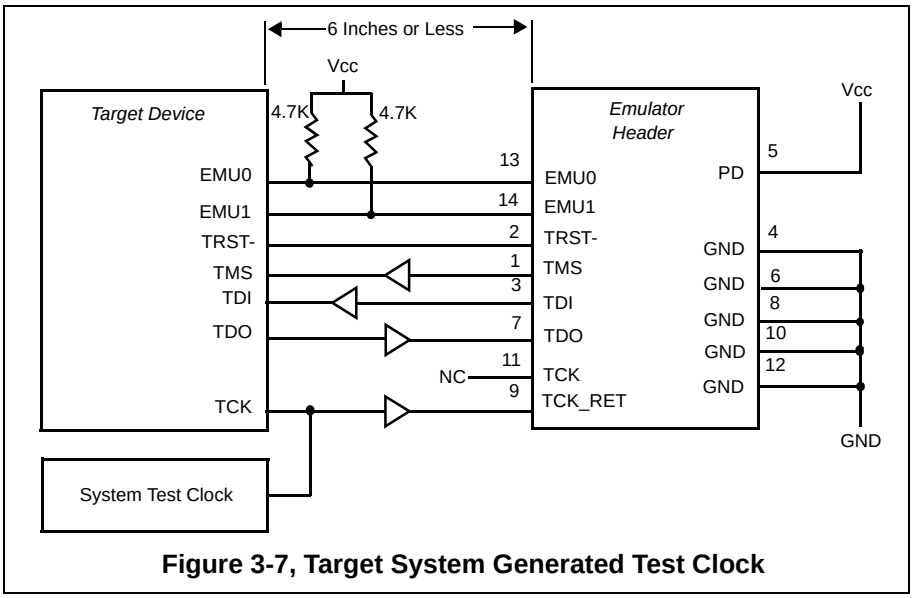

Figure 3-7, Target System Generated Test Clock

There are two benefits to having the target system generate the test clock:

— The emulator provides programmable test clock (default is 12.28 Mhz). If you generate your own test clock, you can set the frequency to match your system requirements.

— In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.

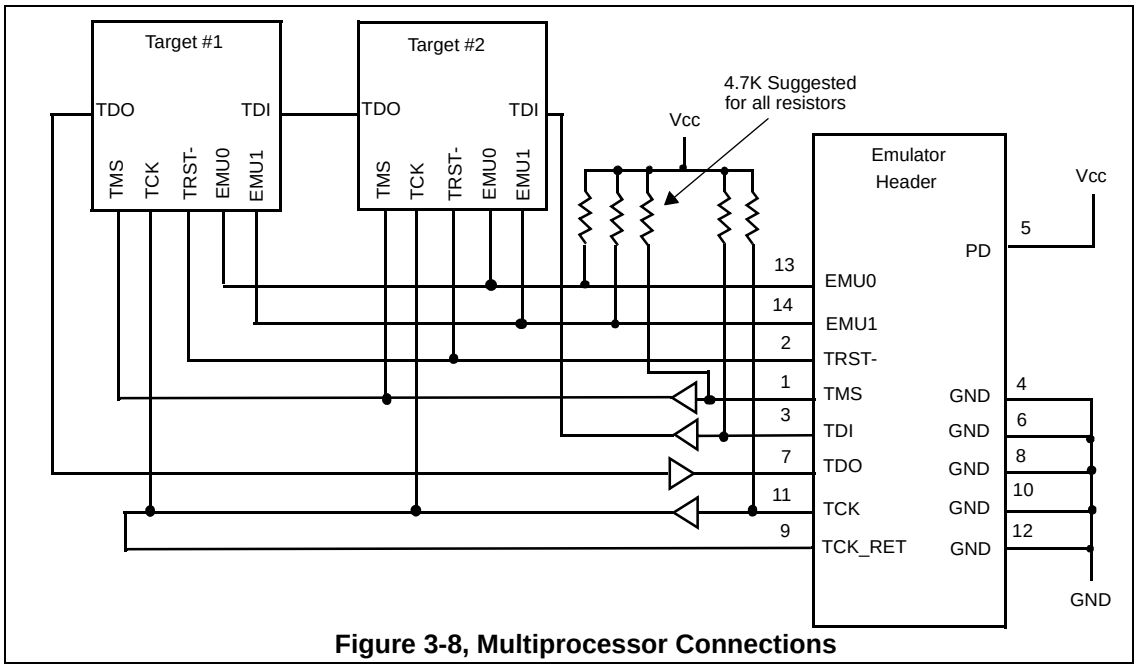

Figure 3-8, Multiprocessor Connections

Figure 3-8 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multiprocessor support are as follows:

- The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.
- The input buffers for TMS, TDI, and TCK should have pullups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pull up resistor of 4.7k ohms is suggested.

3.6 Emulation Timing Calculations

The following are a few examples on how to calculate the emulation timings in your system. For actual target timing parameters, see the appropriate device data sheets.

Assumptions:

$t_{su(TTMS)}$	Target TMS/TDI setup to TCK high	5	ns
$t_{h(TTMS)}$	Target TMS/TDI hold from TCK high	5	ns
$t_{d(TTDO)}$	Target TDO delay from TCK low	10	ns
$t_{d(bufmax)}$	Target buffer delay maximum	7	ns
$t_{d(bufmin)}$	Target buffer delay minimum	1	ns
$t_{(bufskew)}$	Target buffer skew between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}] \times 0.15$	.9	ns
$t_{tckfactor}$	Assume a 40/60 duty cycle clock		0.4

Given in Table 2:

$t_{d(XTMSmax)}$	Emulator TMS/TDI delay from TCK_RET high, max	22	ns
$t_{su(XTDOmin)}$	TDO setup time to emulator TCK_RET high	5	ns

There are two key timing paths to consider in the emulation design:

__ the TCK_RET/TDI(t_{prdtck_TMS}) path, and
__ the TCK_RET/TDO(t_{prdtck_TDO}) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.

Case 1: Single processor, direct connection, TMS/TDI timed from TCK_RET.

t_{prdtck_TMS} = $(t_{d(XTMSmax)} + t_{su(TTMS)}) * 2$
= (22ns + 5ns) * 2
= 54ns (18.5 MHz)

t_{prdtck_TDO} = $[t_{d(TTDO)} + t_{su(XTDOmin)}] / t_{tckfactor}$
= (10ns + 5ns) / 0.4
= 37.5ns (26.6 MHz)

In this case, the TCK/TMS-TDI path is the limiting factor.

Case 2: Single/multiple processor, TMS/TDI buffered input; TCK_RET/TDO buffered output, TMS/TDI timed from TCK_RET.

t_{prdtck_TMS} = $(t_{d(XTMSmax)} + t_{su(TTMS)} + 2t_{d(bufmax)}) * 2$
= (22ns + 5ns + 2(7ns)) * 2
= 82ns (12.2 MHz)

t_{prdtck_TDO} = $(t_{d(TTDO)} + t_{su(XTDOmin)} + t_{bufskew}) / t_{tckfactor}$
= (10ns + 5ns + 0.9 ns) / 0.4
= 39.8ns (25.1 MHz)

In this case, the TCK/TMS-TDI path is the limiting factor.

3.7 Changing Target Cables

Damaged target cables may need replacement or as new processors are developed different JTAG headers will be required. The XDS510USB PLUS has a removable target cable (tail) to accommodate these requirements. To change the target cable use the following steps:

❏ Turn off the power to the target board.

❏ Remove the USB cable from the XDS510USB PLUS emulator.

Figure 3-9, Remove USB Cable From XDS510USB PLUS

❏ Remove the JTAG header from the target board.

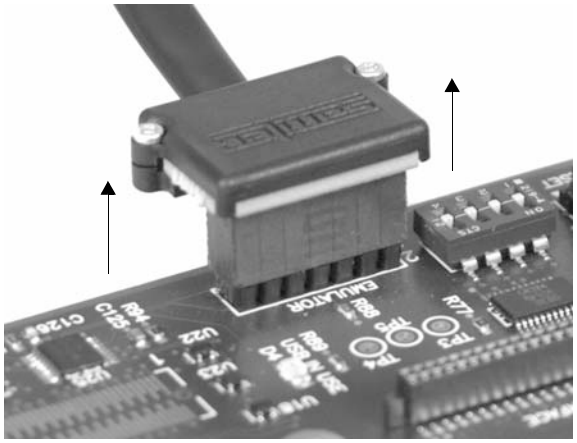

Figure 3-10, Remove JTAG Header From Target Board

❑ Remove the two front panel screws from the XDS510USB PLUS emulator.

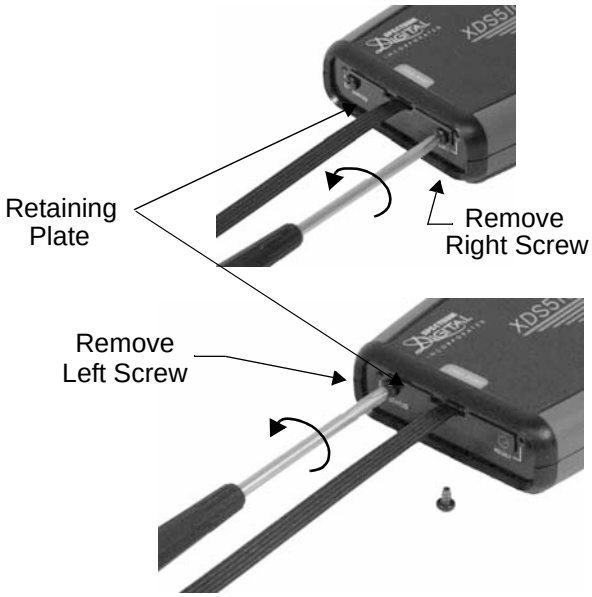

Figure 3-11, Remove Front Panel Screws from XDS510USB PLUS

❑ Remove the cable retaining plate.

Figure 3-12, Remove Cable Retaining Plate

❑ "Gently" remove the cable.

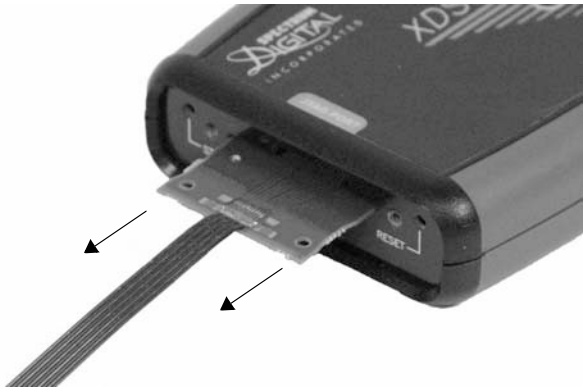

Figure 3-13, "Gently" Remove the Cable

❑ "Gently" insert the new cable with the gold tabs up.

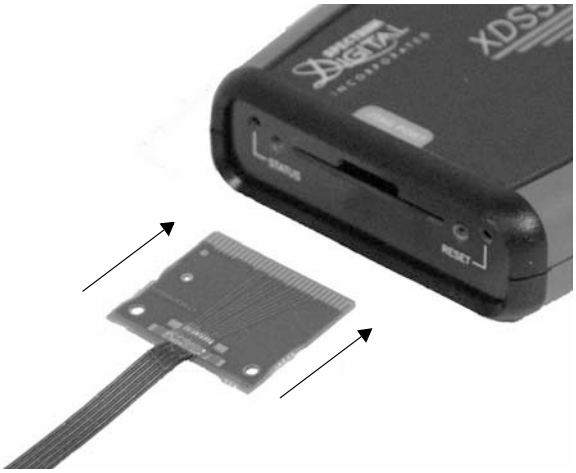

Figure 3-14, "Gently" Insert New Cable

❑ Replace the cable retaining plate by securing the two front panel screws on the XDS510USB PLUS emulator. If installed properly the retaining plate should not be bowed or bent.

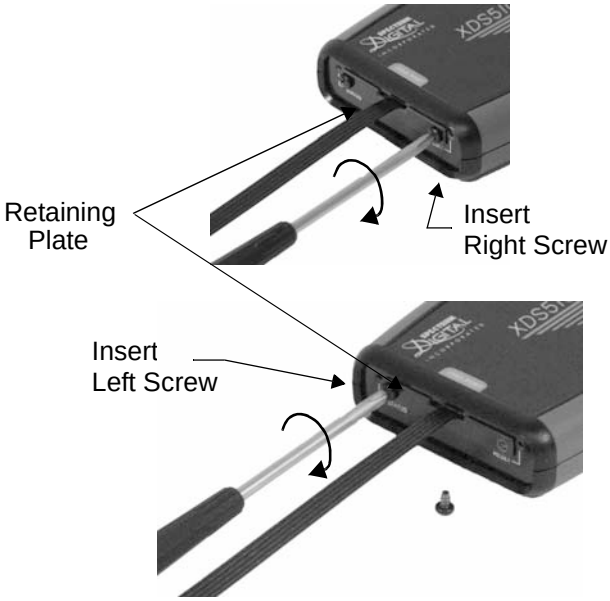

Figure 3-15, Replace Cable Retaining Plate On XDS510USB PLUS

❑ Insert the JTAG header onto the target board.

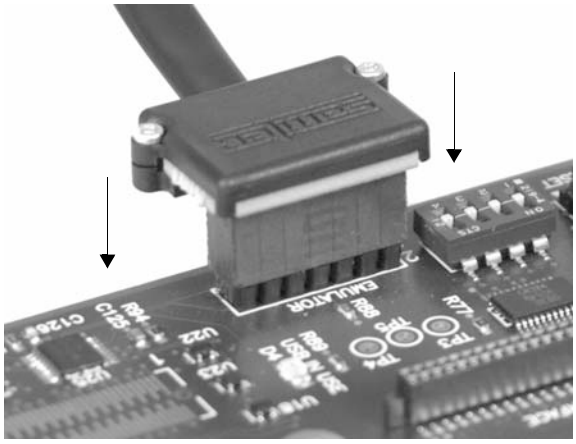

Figure 3-16, Insert JTAG Header Onto Target Board

❑ Attach the USB cable to the XDS510USB PLUS emulator.

Figure 3-17, Attach USB Cable To XDS510USB PLUS

❑ Apply power to the target board.

❑ At the host system you may launch the debugger.

3.8 Target Cables

The XDS510 USB PLUS uses modular target cables that can interchanged for use with specific target JTAG headers. The pin spacing in the cable header may vary from target cable to target cable based on the mating connector on the target board. Refer to the specification of the mating connector part numbers identified in Section 3.1 for the exact spacing of the pins on the board header used in your system. The mechanical information for two of these target cables is shown below. All dimensions are in inches and are nominal dimensions, unless otherwise specified.

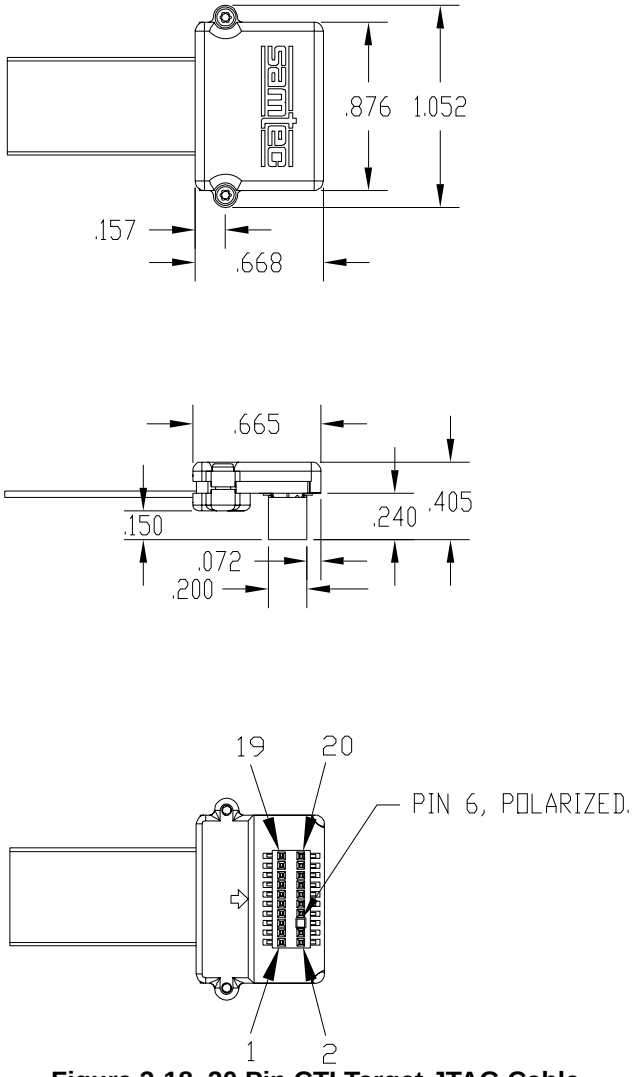

Figure 3-18, 20 Pin CTI Target JTAG Cable

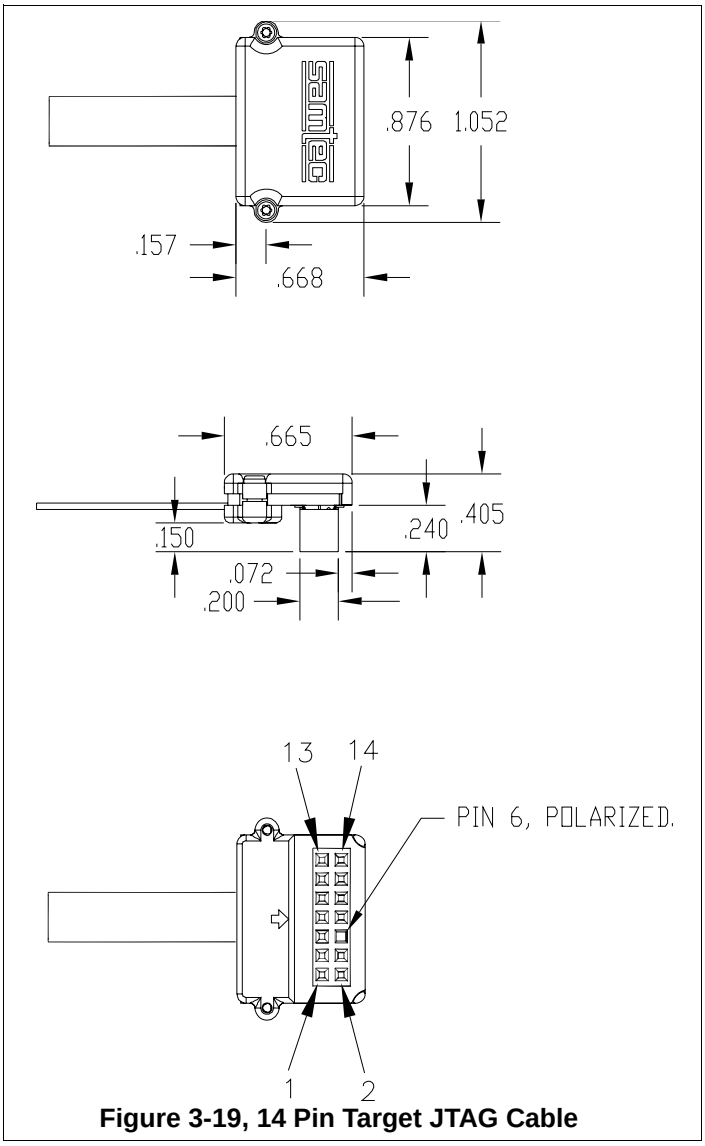

Figure 3-19, 14 Pin Target JTAG Cable

The target cable is flexible and about 13 inches long. It is made from micro coax cable. This type of cable has the following flex/bend limitations.

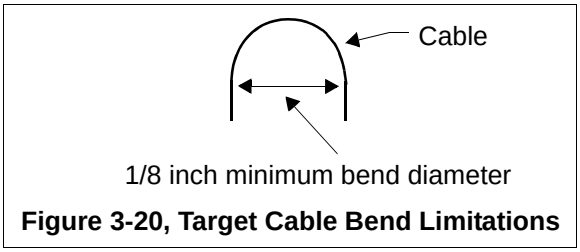

Figure 3-20, Target Cable Bend Limitations

Appendix A

Mechanical Information

This appendix contains the mechanical information about the XDS510USB PLUS JTAG Emulator produced by Spectrum Digital.

The XDS510USB PLUS JTAG Emulator consists of a 6-foot USB cable, the XDS510USB PLUS emulator pod, and a section of cable (tail) that connects to the target system. The overall emulator/cable length is approximately 7 feet, 6.5 inches. Figure 3-8 shows the mechanical dimensions for the XDS510USB PLUS 14 pin header. The XDS510USB PLUS JTAG emulator enclosure is nonconductive plastic with two recessed metal screws.

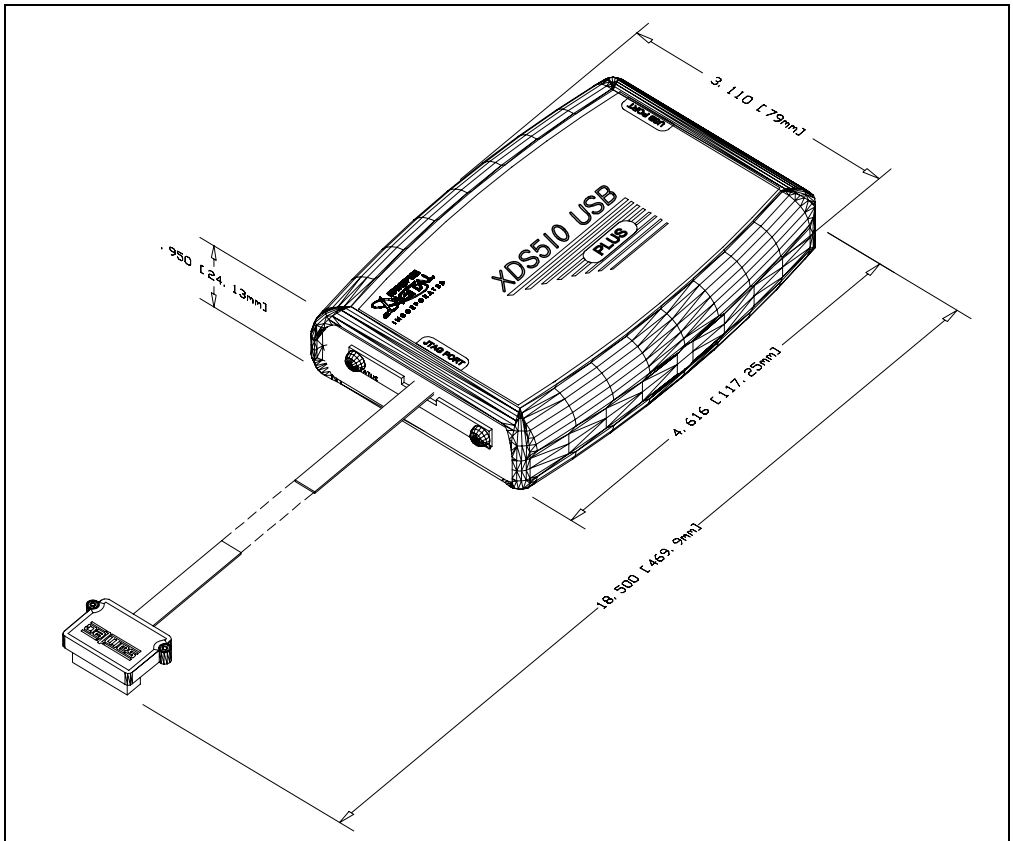

Figure A-1, XDS510USB PLUS Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

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Printed in U.S.A., January 2006
509405-0001 Rev A