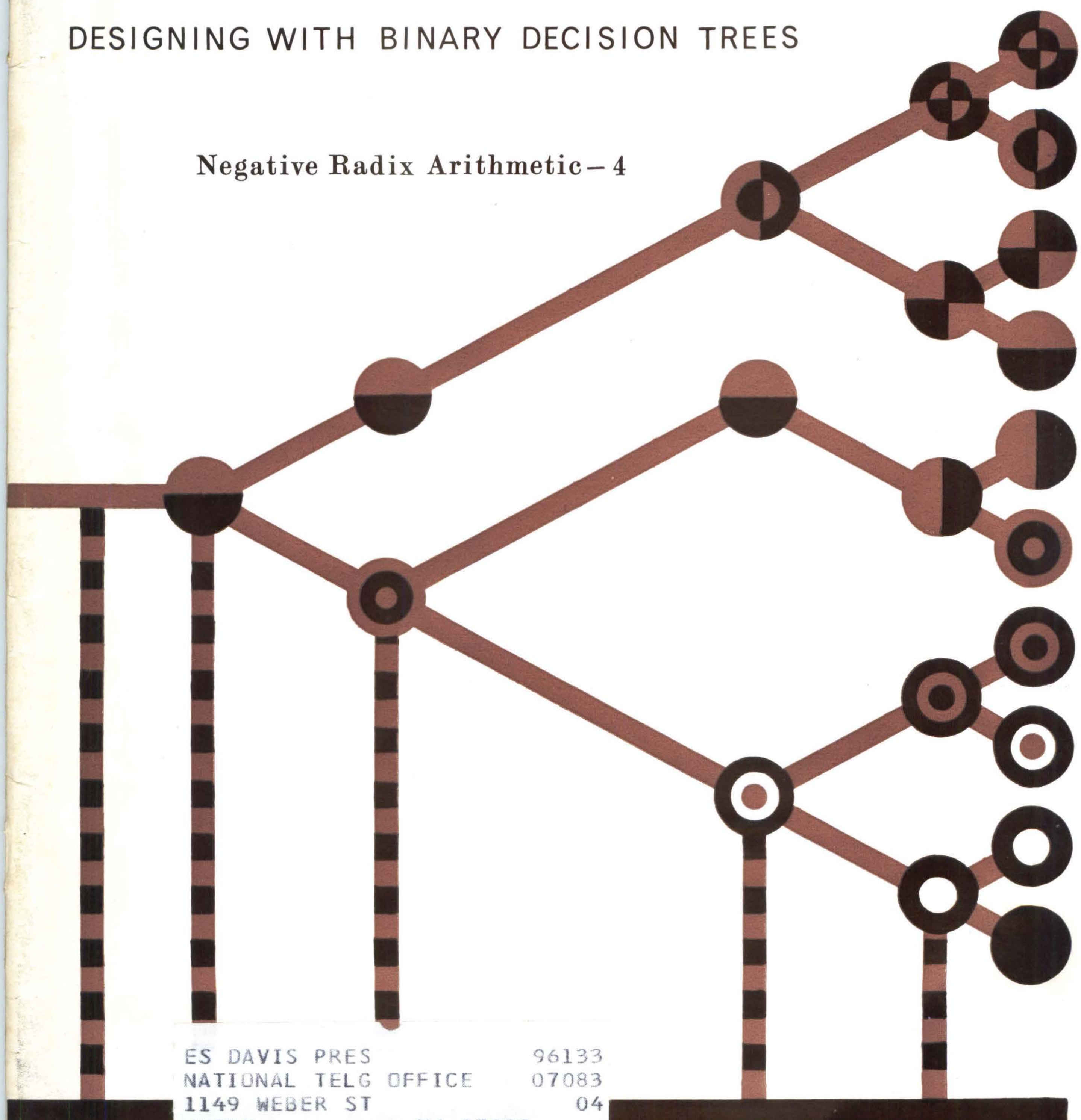
COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

AUGUST 1967

DESIGNING WITH BINARY DECISION TREES

Negative Radix Arithmetic—4



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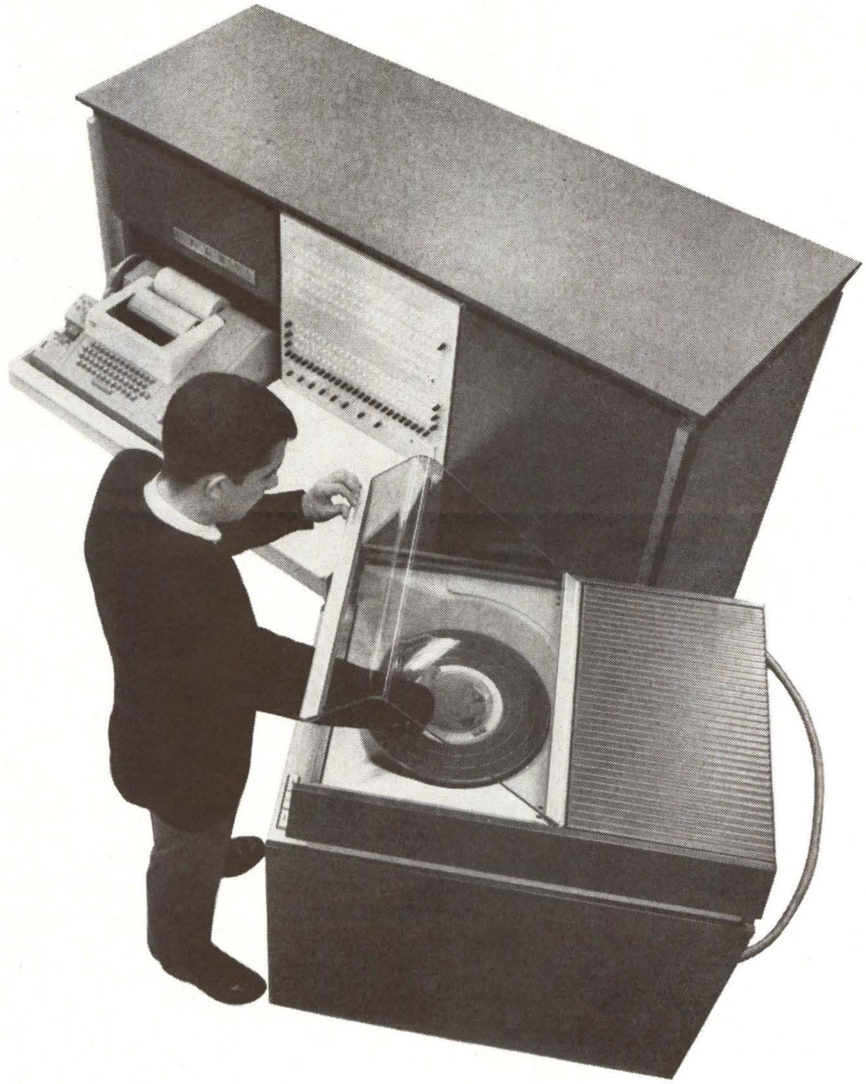

Only our SEL-840A general-purpose computer has it. A unique monitor permits time-sharing execution, including batch processing of background programs, task scheduling of foreground programs and on-line debugging. And the complete package delivers in only 60 days!

Twenty percent less expensive and with twice the throughput (572K words/sec.) of its nearest competitor, the SEL-840A is also the only 24-bit real-time computer with an independent, concurrent floating-point arithmetic unit. Price: $54,500.

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CIRCLE NO. 2 ON INQUIRY CARD

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AUGUST 1967 • VOLUME 6 • NUMBER 8

COMPUTER DESIGN

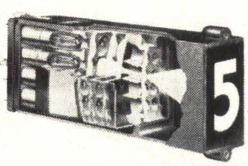
THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

FEATURES

DEPARTMENTS

TAKE ONE

If your work has anything to do with visual readout, there's something in this IEE Catalog for you. It contains the most complete, up-to-date information available on rear projection readouts. If you design, manufacture, market or use products requiring visual display, you should become familiar with current developments in rear projection display. It's in this catalog. The catalog explains the operating principles of rear projection readouts. It also describes the unique results you get with this product. You will easily see why it is specified for applications requiring readability, appearance and versatility. One of these applications could be yours. In addition to specifications on the complete line of IEE projection readouts, the catalog includes information on displays, assemblies, accessories, lamps and prices. It's complete. Ask us for a copy now.



The Rear Projection Readout: When one of the 12 lamps at the rear of the readout is lighted, it illuminates one of 12 film messages, focuses it through a lens system, and projects it onto the non-glare viewing screen at the front. The displayed message is clearly and distinctly projected on a single plane, with no obstruction from unlighted filaments. There is a wide viewing angle and a minimum of interference from ambient light. It is extremely versatile, since anything that can be put on film can be displayed on an IEE readout. That includes any combination of colors, symbols, numbers, letters and words. A total of five different models offering character sizes ranging from ⅛″ to 3⅜″.

"I double-E," the world's largest manufacturer of rear projection readouts.
Industrial Electronic Engineers, Inc., 7720 Lemona Ave., Van Nuys, Calif. **IEE**

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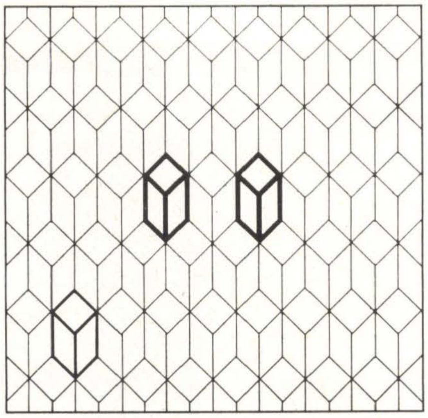


How to build one-of-a-kind or the first of many systems: multi-function MOS ultra logic

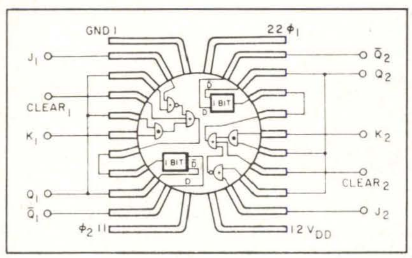
With AMI Ultra-Logic I and II, plus compatible shift registers, you can put together any digital electronic system which will operate up to one megahertz over the full military temperature range. AMI's UL I, Gating & Storage Element and UL II, Expandable Gate Array multiply out to virtually unlimited design opportunities. With Ultra-Logic I, different and usable arrangements up to 23^n can be accomplished. Ultra-Logic II can be interconnected to provide interface with bipolar devices. Take a look. Imagination is the only limitation.

Because interconnection of functions contained in a single circuit is performed externally, you can use Ultra-Logic I and II as breadboard tools over and over again, then easily convert a breadboarded system to large scale integrated microelectronics without loss in performance or expensive redesign. They're also the low cost way to build one-of-a-kind systems.

A minimum lab stock of AMI MOS elements puts versatility in your hands—removes limitations to systems thinking, and keeps the number of different type parts in the storeroom way down. AMI is delivering over a dozen MOS circuits and devices off the shelf, including Ultra Logic I and II. Proof? If your order is in today, we'll ship this week—in either sample or production quantities.

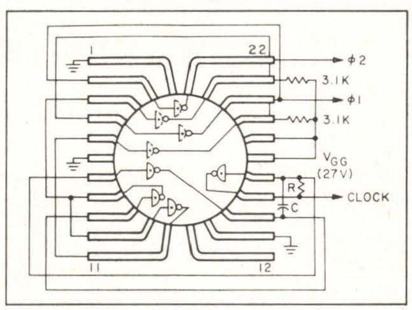
Ready to move into custom large scale arrays? At AMI, MOS technology is not a "someday" capability. It's on-stream, in depth, right now—in a customer-vendor environment that allows you to accomplish your objectives. Your inquiry invited.

Ultra Logic I—Gating and Storage Element
(Shown as: Dual J-K/Clear Flip-Flop)



Functions: One Bit Delay ▫ Binary Counter (T Flip-Flop) ▫ J-K/Clear Flip-Flop ▫ J-K/Load Flip-Flop ▫ RS Flip-Flop with R Override and Clear ▫ Sample & Hold ▫ Complemented Data Sample & Hold Flip-Flop with Clear ▫ AB Comparator ▫ Two Stream Select Gate ▫ Two input NOR ▫ Two input AND ▫ Pre-charge to Level

Ultra Logic II—Expandable Gate Array
(Shown as Clock Generator)



Functions: 1 to 8 Channel Analog Switch ▫ Dual One to Four-Channel Analog Switch ▫ Dual Single Device ▫ Single Dual Device ▫ Multi-Purpose Expandable Four-Gate Array ▫ Single high gm transistor (gm $\approx$ 30,000) ▫ Quad inverter and a 4-input expander gate ▫ NOR gate varying in width from 1 term (inverter) to a maximum of 5 terms, and a triple inverter ▫ Quad 2-input gate ▫ Dual inverter and dual 3-input gate ▫ Two single inverters and a dual 3-input gate ▫ Series shunt chopper ▫ Clock generator

Write for complete data on AMI's full line of compatible MOS building blocks

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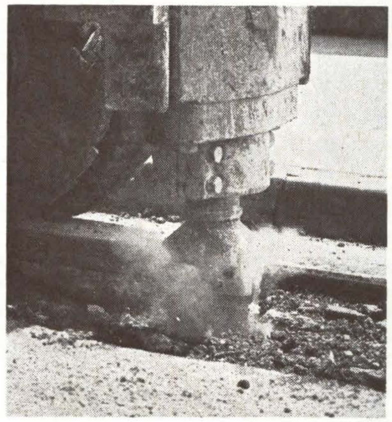

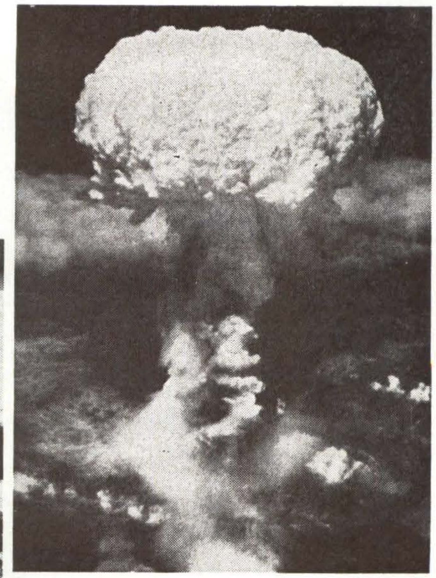

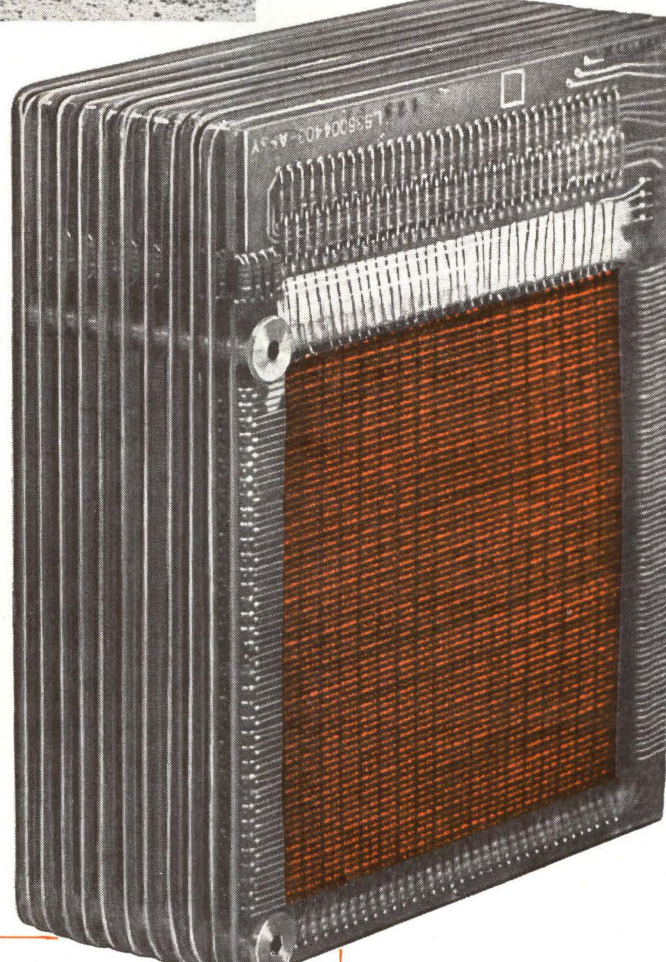

When an irresistible force met a nondestructive (woven plated wire) memory . . .

38,880 NDRO bits took a 1000-G shock and emerged not one bit different.

This custom-woven nondestructive readout memory stack has an unshakeable story: zero readout error, zero physical degradation. Interrogated during and after severe environmental testing, data stored was data retrieved. Using minimal power. With all required memory exercises completed (equivalent to MIL-E-16400 and MIL-E-5400), these aerospace applications loom large on our horizon: program & instruction storage / look-up tables / executive programs / digital simulators / character generator storage / back-up memory. Write for detailed brochure and authenticated test results: General Precision Systems Inc., Librascope Group, Components Division, 808 Western Avenue, Glendale, California 91201.

GP GENERAL PRECISION SYSTEMS INC.
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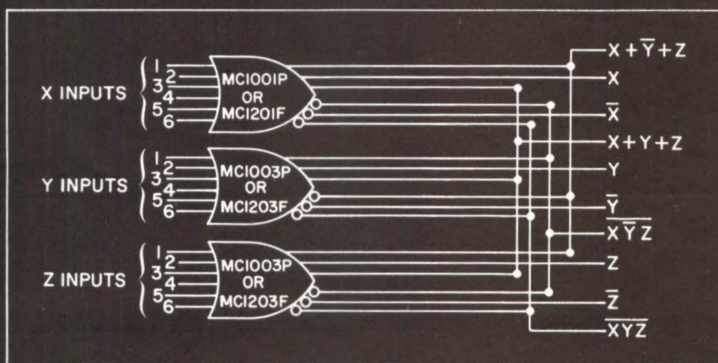
CIRCLE NO. 9 ON INQUIRY CARD →

MECL II High-Speed LOGIC DESIGN IDEAS . . . one of a series

...in just 4 nanoseconds! YOU CAN GENERATE ANY OF THESE: $X, Y, Z; \bar{X}, \bar{Y}, \bar{Z}; X+\bar{Y}+Z; \overline{X+Y+Z}; \overline{X\bar{\bar{Y}}Z}; \overline{XYZ}$



(where X, Y, Z each stands for six variables "ORed" together)

(MECL II MAKES IT POSSIBLE!)

Yes, you can do it easily with MECL II, in just 4 ns with 3 gates and a total power dissipation of 250 mW. The unique wired "OR" feature of MECL II allows you to obtain the OR function of two or more gate outputs by tieing the outputs together. As a result, you save delay time, power dissipation, extra gates and design headaches. More importantly, the flexibility of this system allows for an almost infinite number of logic design possibilities!

The Family for Logic Designers

The growing MECL II family of digital integrated circuits already has 24 members and is designed for easy use from audio frequencies to above 100 MHz. The gates shown, MC1001P, 1003P and MC1201F, 1203F are all Six-Input Gates in the new MECL II series. Each provides three simultaneous "OR"/"NOR" or "AND"/"NAND" output functions. By omitting all or part of pulldown resistors, three emitter follower output options are provided on basic MECL II gates.

These 6-input gates (MC1000 & MC1200 series) feature 4.0 ns propagation delay at a fan-out of 3 and a total fan-out of 25 (min) per output. The limited-temperature-range 1000 series (0° to +75°C) is available in the 14-pin dual in-line plastic package, while the full-temperature-range 1200 series (—55° to +125°C) is in the 14-pin ceramic flat package.

For complete details about the fastest, most flexible logic family available, write for complete data sheets and application notes. Then, see how many high-speed gate functions you can synthesize!

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-where the priceless ingredient is care!

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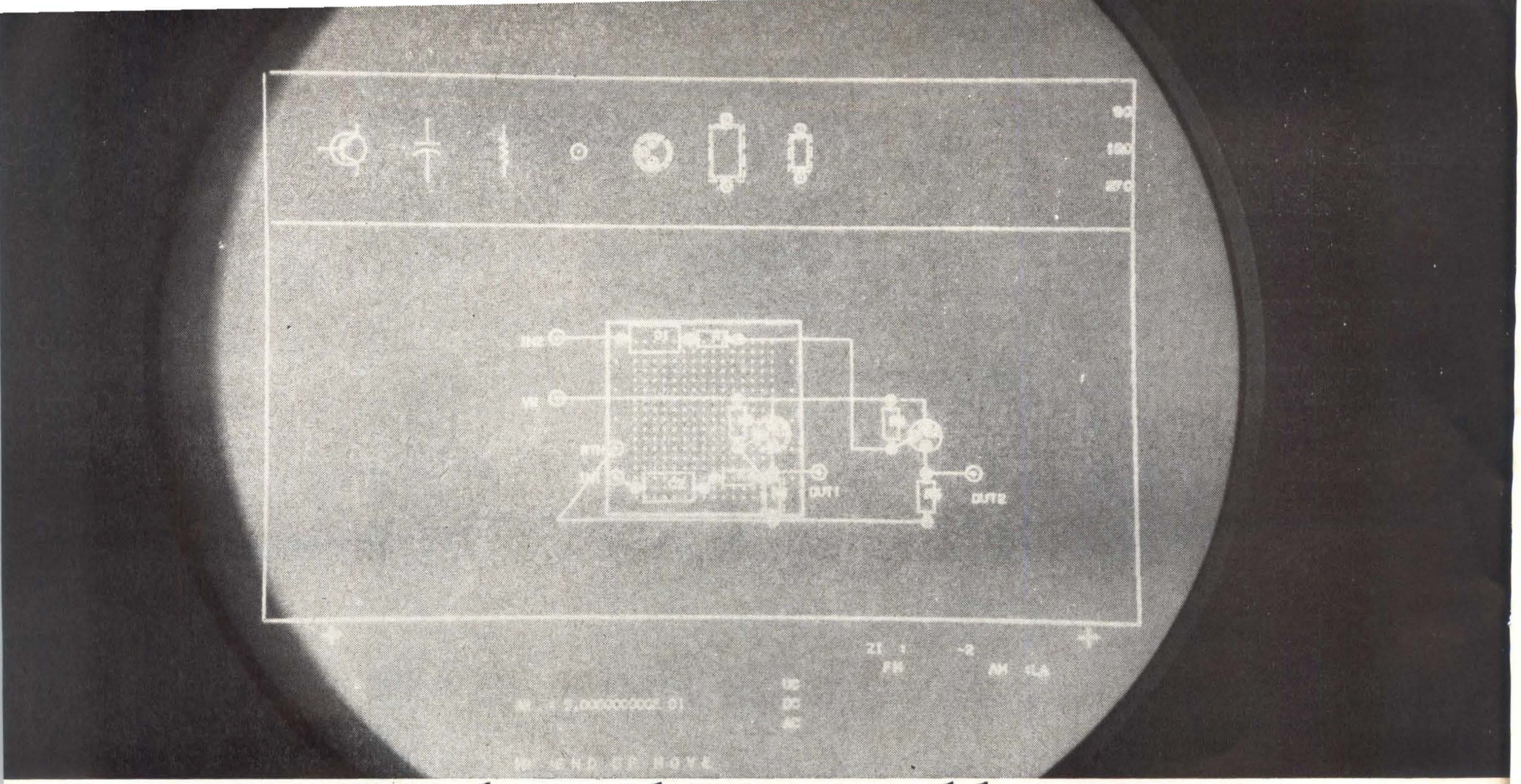
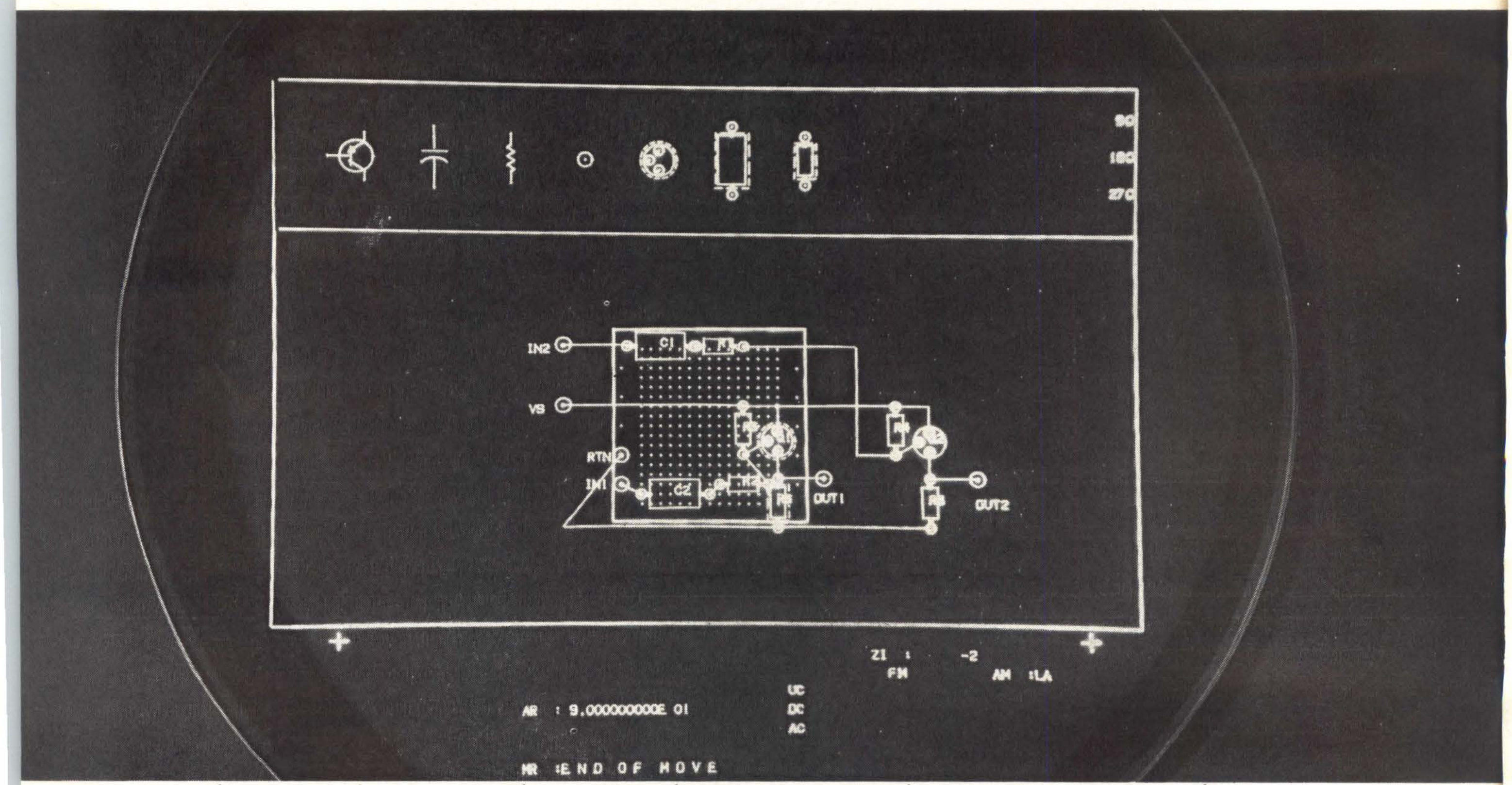


Readouts clear up problems.



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commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL. Contributing Editor.**

HOW COMPUTER WORD SIZE AFFECTS PERFORMANCE

John Thron

One of the most common ways of characterizing a computer is by **word size** — the number of binary digits that can be retrieved from, or stored in, the computer memory in a fixed time interval. Although there is nothing intrinsically valuable in one or another word size, it is often a major indicator of computer capability. In fact, in most cases, the memory cycle time word and word size alone constitute data upon which a fair guess of performance can be based. This is because performance is primarily memory access limited (if it is not input-output limited), and therefore depends upon the rapidity of memory-access and upon the **value** which accrues to memory-access.

The positive contribution of increased word size to performance is related to the value of retrieving or storing a larger quantity of data at a single memory access. This is a contribution which naturally pays diminishing returns. For one thing, the sequential character of the computer program results in frequent decisions which alter the course of procedure and thus alter the requirements for data. For another thing, too big a piece of information is nearly as useless as too small a piece — the computer must process a specific unit of information with each operation. Thus, a word equal in size to the unit of information to be processed would represent the optimum choice: exactly the correct quantity of data would be accessed at each memory cycle. When word size is very small relative to information-unit size, an increase in word size brings a proportional increase in performance. When word size is greater than information-unit size, wasted transfer of data is the result. Not surprisingly, no fixed size can be assigned to the "information unit," and thus performance ultimately depends upon a more or less good match between word size and "typical" information-unit size.

The author of this month's CD Commentary, John Thron, is a staff engineer at Honeywell's Computer Control Division. He is responsible for computer systems design.

On first examination, it might seem impossible to typify the data processed by a general purpose computer. In data processing, every problem has its own characteristic units — characters and fields of widely varying lengths. In scientific computation, a similar condition exists — different problems deal with numbers of differing precision, and arrays of varying dimensions. No simple average of the measures of all these **problem-related** data provides a meaningful guide to determining optimum word length.

However, memory-access is required for another category of data — program-related data. These include operation codes, addresses, indices, counters, and a variety of data used for "housekeeping" purposes in the typical program. The classical single-address computer (whose word size was related to requirements for precision) makes more than half of its memory references for instructions. Empirical studies have shown that typical programs expend more than half of their energy doing housekeeping; thus, perhaps a quarter of the memory references are to program-related data.

The ratios are not much different for the "character organized" systems. An instruction that references two 3-character fields might itself typically be six characters long, and the housekeeping overhead remains. The conclusion is inescapable that the **typical** data processed by computers are operation codes, addresses, etc.

This being the case, instructions and addresses are the units of information whose size can most beneficially be related to word size in a general-purpose processor. Special features for processing longer or shorter units of data, appropriate to certain types of problems, can be incorporated in a computer, and may make impressive improvements in the performance. But with few exceptions, these features have been found to be difficult to define, and when they have been permitted to govern word size, at the expense of efficient instruction and address access, the effect on performance per dollar has not been attractive.

Now, the larger the word size of the computer, the larger the address, operation code, instruction, or combination of these data that can be accessed with a single memory reference. Increasing the **number** of each of these program-related units of

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70% to 90% efficiency? ?	Instant fault repair by plug-in module replacement? ?	Add-on power capability by using more modules? ?	Ability to handle full load steps while maintaining out put in regulation band? ?

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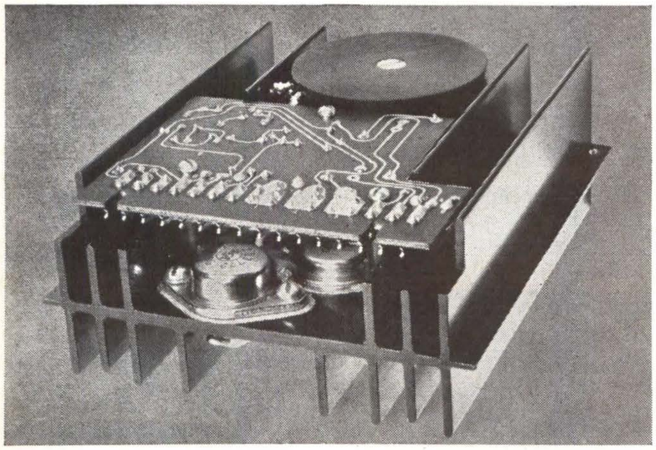
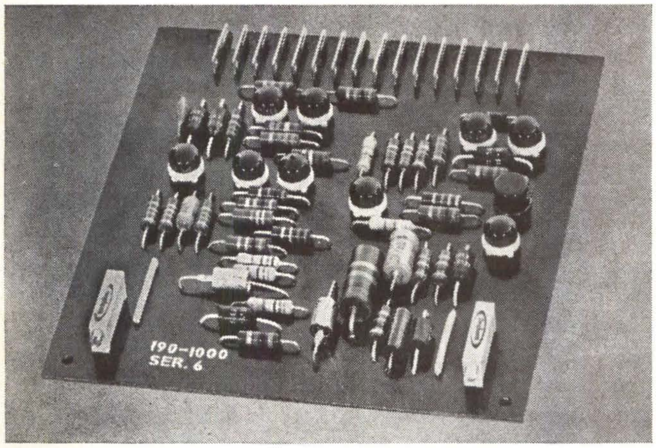


Omnimod power control module.



Omnimod control amplifier.

OMNIMOD gives you all these features—*and* more—*and* at a lower price! Want to know more?

OMNIMOD is a dc to dc converter using transistors in a CONSTANT PULSE WIDTH, variable repetition rate switching mode to regulate output voltage or current. Two small plug-in units make-up the OMNIMOD concept—a power control module and a control amplifier.

Output can be regulated between $\pm$ 2 and $\pm$ 60 dc at up to 20 amperes using the OMNIMOD family of modules WITHOUT MODIFICATION OR ADJUSTMENT. Higher current ratings are obtained by paralleling power control modules.

Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

To design a custom power supply, one must simply

1. design one input power converter to change unregulated line ac power to unregulated dc power

2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output

3. package these elements with filter capacitors and a plug-in amplifier module for each output

All the power used by every element in a typical data processing system could be supplied by custom power supplies constructed with interchangeable OMNIMOD modules.

Isn't this enough to consider OMNIMOD for your custom requirement? We will design an OMNIMOD custom power supply to your specs, or will help you design your own system using our plug-in OMNIMOD modules.

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information accessed with a single memory-reference has some benefits; however, a substantial amount of register storage (to hold waiting instructions and temporarily unused addresses) and other logic circuitry is required to obtain improved performance in this way. But such benefits are confined to program access; no benefits are obtained in the accessing of addresses and instructions themselves as the operands to be processed. Increasing the **size** of each of these program-related units of information, on the other hand, has a substantial, although conditional, effect on performance. Increasing the address size is of great value if the memory to be addresses required a larger address. Increasing the instruction size permits a larger variety of instructions, and thus opens the way to more special-purpose features. These benefits may or may not be significant, depending upon the job to be performed. A large word permits efficient access of the large address required to span a voluminous memory, and/or the extensive array of operation codes contributing to a variety of special jobs. If these are application requirements, they pay off handsomely. Otherwise, they do not.

Thus, in the final analysis, word size is appropriately related to the **scope** of the application, through the instruction and addressing requirements, more than to the specific type of data to be processed. The performance, in turn, of a processor with large word size is not likely to be significantly better than that of a processor with small word size, unless the scope of the problem is suitably great.

NEW BOOKS

THE COMPUTER IN AMERICAN EDUCATION

The first definitive statement on the potentialities and limitations of computer technology in education is how the publisher describes this new book. Edited by Don D. Bushnell, Brooks Foundation, and Dwight W. Allen, Stanford University, and written by leading educators and outstanding practitioners in the field of educational data processing, The Computer in American Education presents a dialogue between technically and non-technically-oriented persons interested in the growing problems of education. Critical issues and promising trends in application of computer technology to education are viewed within the context of evolving social and educational goals and the movement toward reform in school structure and curriculum. The authors examine current applications in educational management and planning; the potentialities of automation for individualizing instruction and enhancing learning; and the expediting of information handling for the realization of long-held goals in education. Some guidelines for the introduction of computer sciences into the curriculum are suggested. Commissioned by The Association for Educational Data Systems, the book has been published in two editions — a clothbound ($5.95) and a paperbound ($3.95). The book contains 300 pages. Order from:

John Wiley & Sons, 605 Third Ave., N.Y., N.Y.

DC OUTPUT

from our man in Washington

An 11 percent increase, projected by the Marketing Service Department of the Electronic Industries Association for electronic industrial products to a level of $5.5 billion in sales during 1967 can chiefly be ascribed to continuing strides in shipments of computing and EDP equipment. While sales to domestic users have grown rapidly in recent years, EIA concludes, the overall computer market has been additionally enhanced by large shipments to foreign countries. With U. S. superiority in developing highly-sophisticated computers, the demand for such equipment in foreign markets is expected to continue for some years. EIA states: "Computer manufacturers, with their extensive facilities, modern equipment, and dependable sources of financing, help provide leadership in the development of advanced technology and in marketing techniques."

Electronic computers and parts accounted for 52.8 percent of U. S. exports of business machines in 1966, totaling $295.3 million. Chief customers, according to statistics compiled by the Commerce Department's Business and Defense Services Administration, were Canada, France, United Kingdom, West Germany, and Japan. Computing and other data processing machines accounted for 7.8 percent of 1966 business machine imports, an increase of 353.6 percent to $14.9 million. Principal suppliers were France, Italy, Canada, United Kingdom, and Japan.

By the year 2,000, Secretary of Agriculture Orville L. Freeman predicts that computer-controlled machines will plant the crops, fertilize by prescription, determine when produce is ready for market, harvest on order, and grade and package the commodities for delivery by supersonic cargo planes to fully-automated warehouses.

Postal officials have asked Congress to pass legislation (S. 1693) to provide that bills and statements of accounts prepared by EDP equipment be classified as first-class mail. Presently the Post Office allows bills and statements of accounts produced by any photographic or mechanical process, other than typewriting, to be mailed at third-class rates if they are presented in 20 or more identical copies — this includes materials prepared by computers. Post Office General Counsel Timothy J. May, in urging passage before the Senate Post Office Committee, estimated that POD would gain about $20 million annually if the bill passed. Enactment, he said, would keep large mailers from obtaining an advantage over small mailers. Computer use, he said, is very expensive and large numbers of bills must be mailed to make it worthwhile to use computers. Because of the cost, small mailers are less likely to use computers.

In view of the growing importance of computers, all engineering students, at an early stage in their education, should receive training in numerical methods, statistics, and probability theory, concludes a recent report of the Organization for Economic Co-operation and Development. The fourth report of the 21-member, international group, "Applied Mathematics for Engineers," examines the influence of modern computer techniques on mathematical training given to students in all branches of engineering and on a number of related specialized subjects. The last part of the report covers the use of computers in engineering schools and discusses machine languages, digital-computer simulation, decision problems, and project analysis. A copy of the report is available for $5.50 from OECD Publications Center, Suite 1305, 1750 Pennsylvania Ave., N. W., Washington, D. C. 20006.

Recent Government Contracts

BENDIX CORP., Davenport, Iowa, has been awarded a $2,860,791 fixed-price contract for production of airborne computer components. Work will be done in Denver, Colo. The Aeronautical Systems Division (Air Force Systems

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The DATA/620-I integrated circuit computer is the newest member of the DATA/620 family of system computers. DATA/620-I fills the gap between general purpose and special purpose computers. It belongs in a system, and solves problems previously considered too difficult or expensive for computer solution.

Designed for faster problem solution the DATA/620-I has a bigger instruction set, integrated circuit reliability, is smaller, has one-half the components, and costs less than any computer in its class.

DATA/620-I comes complete with software, field-proven and refined on the DATA/620.

Extremely compact, the DATA/620-I requires only 10″ of 19″ rack space. It's available with memory modules from 1024 to 32,768 words of 16 or 18 bits, and with a selection of control, arithmetic and I/O facilities, including our unique Micro-Exec.

Price: $13,900 with 4096 words of 16 bit memory, including ASR 33 teletype. Please write.

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Command), Wright-Patterson AFB, Ohio, is awarding the contract.

SPERRY RAND CORP., St. Paul, Minn., has been issued a $1,590,280 letter contract for production of fire control digital computers and related equipment for TALOS missiles for the Navy.

GENERAL ELECTRIC CO., Syracuse, N. Y., has been awarded a $2,635,000 fixed-price contract for one van-mounted digital computer for use in automating data collection and data reduction in support of war games field experimentation. The contract is being awarded by the Army Electronics Command, Fort Monmouth, N. J.

CARNEGIE INSTITUTE OF TECHNOLOGY, Pittsburgh, Pa., has been awarded a $1,717,000 contract for research in EDP equipment information processing. The Office of Scientific Research is the contracting agency.

GOVERNMENT REPORTS ★★

LARGE-ANGLE DEFLECTION TECHNIQUE FOR LASER DISPLAY

Based on a study to develop an improved coherent light beam scanning technique for use in a real-time, projection display system using a laser light source, this report reviews the basic features of the selected approach and translates the required system performance into component parameters. Progress in techniques critical to the design of a successful system such as torsionally resonant light beam scanners is described. Included also are an analysis of system performance and a discussion of future potential.

Order from Clearinghouse, U.S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-651301. Price $3.00 (microfiche 65 cents).

A BRIEF SURVEY OF PREPROCESSING FOR PATTERN RECOGNITION.

Literature survey in which 35 papers treating the preprocessing problem in pattern recognition are summarized and reviewed. Papers of an analytical and practical nature are included as well as a bibliography of 97 entries.

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A COMPUTER SYSTEM FOR INFERENCE EXECUTION AND DATA RETRIEVAL

Describes the Relational Data File, a computer-based data retrieval system which is capable of storing millions of facts and of retrieving data both directly and through logical inference. The system operates on an IBM 7044 computer.

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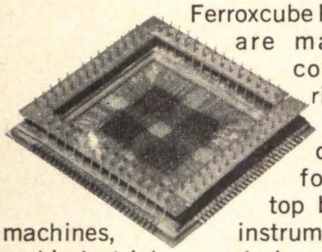
Now an instant Core Memory ...just plug in and solder



Ferroxcube Platrices are magnetic core matrices specially designed for desktop business machines, instrumentation and industrial control equipment. Not only are they priced far below conventional core memory planes; they save you even more money on assembly costs.

Platrices are provided with plug-in connection pins for quick and simple direct mounting on printed circuit boards. You mount a Platrix as you would a transistor: push the leads through the board and solder. To illustrate, we built this mockup out of clear plastic so you can see both the pins and the Platrix itself.

The expensive cut frames of conventional planes are eliminated by a simplified yet rigid frame of glass-epoxy laminate. For high resistance to shock and vibration, the cores are fixed to a base plate of this material by a special lacquer.

Stacks of up to four Platrices can be supplied with series connected drive lines terminated at the bottom of the stack. Low drive currents allow use of simple drive and selection circuits. Platrices are available in 8 standard configurations with bit capacities from 256 to 1,024, but we can be persuaded to make other sizes if you really need them.

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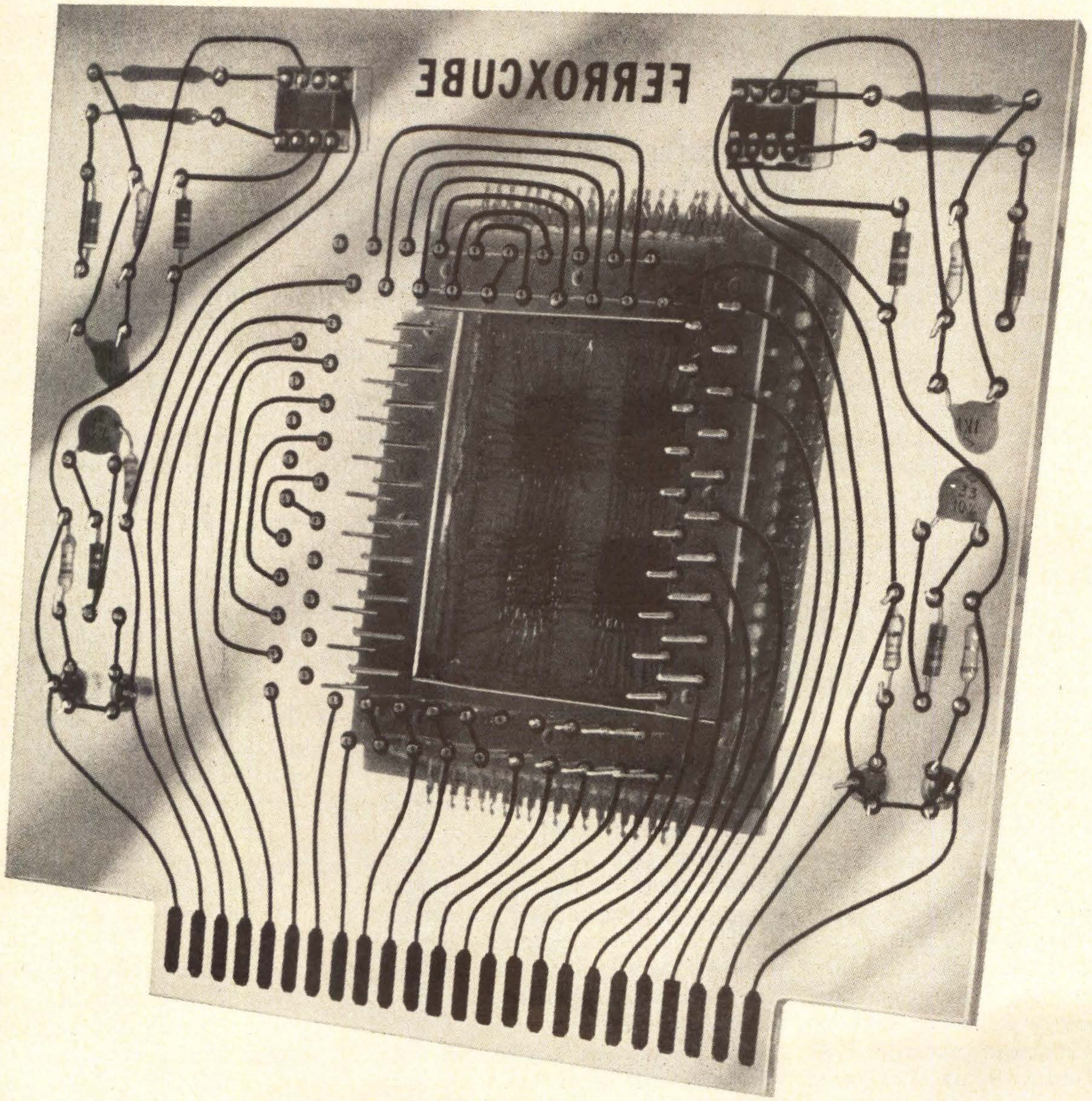

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what do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

THE ENGINEER'S JOB SECURITY

Editor's Note: Since its creation two years ago, CD Readers' Forum has been occupied with the area of standardization. The majority of our coverage and consequent response from our readers has been in the area of logic symbols standards, although we have also devoted space to other topics in the standards field.

The mission of the Forum is to provide space and format for the discussion of any subject which is properly a concern of our readers, and on which there is opportunity for an exchange of opinions and arguments. In each of the next three months we shall be introducing a new topic which we think should be of concern to our readers, and on which we invite our readers' comments. Our interest is not to abandon the logic symbols standards discussions, but to use the Forum for the concurrent discussion of several topics.

This month we present a letter by Mr. Jay Freeman in which he discusses the problem of the engineer's job security and proffers two programs which he believes would increase the engineer's security. CD Readers' Forum invites your comments.

TO CD READERS' FORUM:

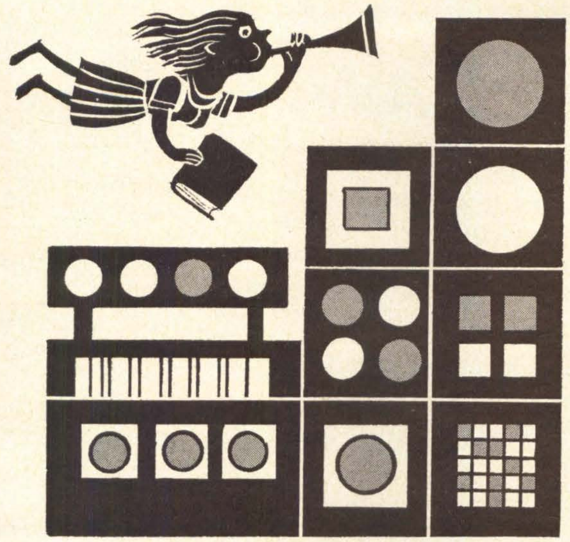
The problem of an engineer's job security haunts him throughout his career. In 1963, twenty to thirty thousand engineers were laid off in the United States because of cutbacks in government spending. Should the war in Vietnam end, the employment picture for engineers would be very bleak. Over 70% of research and development in the United States is government supported and this expenditure would surely be reduced if peace were declared.

Unlike law or medicine where job security increases with the years, in engineering it decreases. An engineer over forty-five will find it harder and harder to obtain or retain a job. Though most of these conditions are well known by engineers, little has been suggested to improve the stability of our careers.

Here are two programs which I believe would increase the engineer's security. A national pension fund should be established. This fund would be contributed into, either partially or fully, by companies employing engineers. A large insurance company would establish rates and coordinate the operation. Whenever an engineer changed his job, payments into his pension fund would be transferred and continued. At present, if an engineer loses his job, he generally loses all or most of his retirement income; his pension is not transferable to another company, and this could be a financial disaster if he is over forty-five.

If this national pension fund for engineers were implemented, as long as an engineer had worked for the prescribed minimum number of years, for any number of companies, he would be eligible for full benefits when he reached retirement age, (for example, 50% of his best five year-average) since his pension would be transferable. Because engineering places such a high demand on creative, state-of-the-art abilities, an early retirement is often advisable. The national pension fund would recognize this with early retirement options, for example starting at 54 years of age, with full benefits paid at 62 years of age.

The second proposal is a national unemployment insurance paid for, partially or fully, by companies employing engineers. This unemployment insurance would augment the small state unemployment payments while an engineer is seeking another job, and would be a per-



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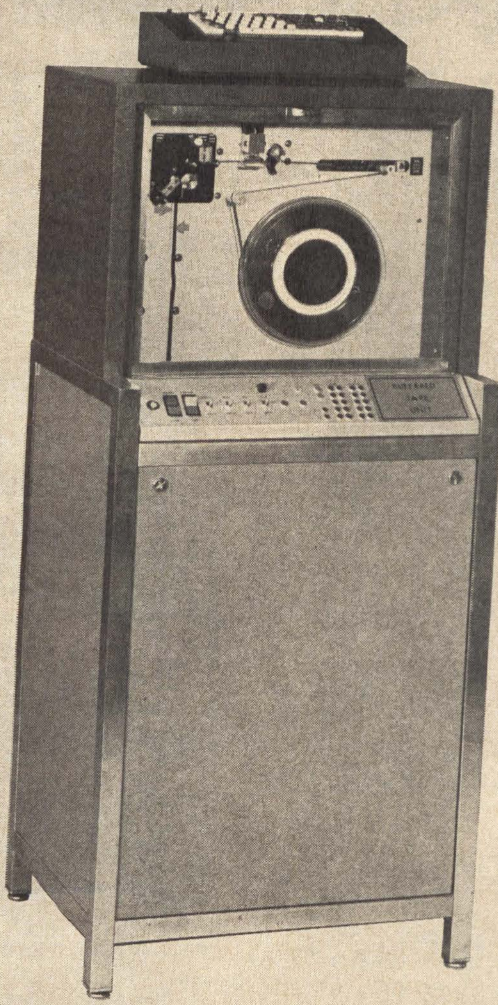

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Write-out and acceptance of data *at electronic speed* are made possible by the core memory in the "700". In READ mode, records are read from magnetic tape into the core memory then transferred to your output device. In WRITE mode, data goes from core memory to magnetic tape. Accuracy is assured by read-after-write check. Data is received in or released from memory in complete record format.

The "700" features the exclusive Mohawk method of key-transcribing data direct to magnetic tape, and verifying on the same machine. Data is entered on tape as 80-character records (optional up to 180 characters), on 7 channels, with nominal inter-record gap. Density is 200 characters per inch.

• The "700" *writes* up to 200 eighty-character records per minute . . . *reads* up to 400 eighty-character records per minute • Each written record is completely checked for parity, and bit-for-bit against core buffer • Less down-time and maintenance with the "700's" solid state electronic elements than with electro-mechanical equipment • Interface: asynchronous, bit parallel, character serial.

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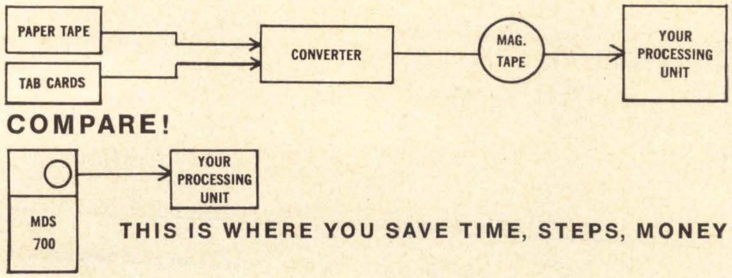

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centage of his current salary. A large national insurance company would establish the rates and coordinate payments.

These two proposals would, of course, benefit engineers greatly. Even those who never used the unemployment insurance because they were always working, or those who never used the national retirement plan because they did not live long enough, would benefit in knowing throughout their careers that the spectre of financial ruin did not forever lurk just over the horizon.

These proposals would also benefit companies employing engineers. Young people would be more likely to choose engineering as a career knowing that a more secure future awaited them. Thus, the engineering shortage which periodically afflicts the industry would be reduced. The problems of conscience and a bad reputation which face an employer forced to lay off would be greatly reduced. The morale of the engineering profession would be lifted, increasing productiveness. Should the industry adopt this program on their own initiative, the threat of engineering unionization would be greatly reduced.

Assuming then, that these two proposals are desirable, how are they to be achieved? There are three possibilities:

1. The existing engineering organizations, e.g., the Engineers Joint Council or the National Society of Professional Engineers, could exert their influence to establish these proposals.

2. Companies employing engineers could establish the proposals through their business associations or other coordinating bodies.

3. Engineers could organize a professional association or union to achieve these goals.

Although I am sure engineers differ strongly on how they may improve our profession, I am curious as to the interest and support given to these basic concepts of improving job security. If, we, as engineers, can first agree on goals, then perhaps the means will follow.

Jay Freeman
Flushing, New York

INDUSTRY NEWS

THE INSTITUTE FOR COMPUTERMATION MANAGEMENT ANNOUNCES THE SCHEDULING OF COURSE INSTRUCTION FOR THE OPERATION, IMPLEMENTING, AND CONTROL OF COMPUTER-BASED TOUCH-TONE SYSTEMS. Emphasis will be placed on case studies of citywide order-entry, credit authorization, and bank management information systems, and includes managerial planning aspects. Live demonstrations will be presented, and price performance evaluations of Touch-Tone, audio response, and translator devices will be given to contrast external utility services with in-house systems. Data base development and updating, and other software techniques will also be studied. The Institute is sponsored by a group of unilaterally involved companies recognizing that applied education is vital to corporate growth. The sponsors are Comput-A-Credit Inc.; Computer Telephone Corporation; and Photo Magnetic Systems, Inc. Currently, seminars are planned for the following dates and locales: Monday, August 21, 1967, San Francisco; Thursday, September 14, 1967, New York City; Tuesday, October 3, 1967, Chicago; Tuesday, November 7, 1967, Boston; Monday, November 13, 1967, Los Angeles (Preceding the Fall Joint Computer Conference). Further information is available from the Registrar, Institute for Computermation Management, 400 12th Street, Washington, D.C.

SYLVANIA ELECTRIC PRODUCTS INC. HAS DEVELOPED FOR THE AIR FORCE AN ELECTRONIC DEVICE WHICH REDUCES SUBSTANTIALLY THE TIME REQUIRED TO SEND CODED DIGITAL INFORMATION between satellite communications ground stations. Known as an optical correlator, the device speeds the synchronization of equipment that detects digital messages. Developed under a $150,000 contract from the Rome Air Development Center, Griffiss Air Force Base, N.Y., the correlator is expected to be tested with satellites now orbiting the earth. Leonard E. Gough, Director of Engineering at the central operation of Sylvania Electronic Systems, a division of the company, said, "By minimizing the time span within which a transmitter and receiver match codes, ground station personnel can significantly increase message traffic when communicating via satellites." The optical correlator reduces by a factor of 1000 the time required by present correlators to examine a series of coded bits of information. The new device identifies simultaneously up to 500 such code bits by converting them to light waves and displaying them as a group.

A NEW COMPUTER LANGUAGE THAT IS EXPECTED TO CUT TIME SPENT IN TECHNICAL INFORMATION SEARCHES FROM HOURS OR DAYS DOWN TO MINUTES — OR EVEN SECONDS — has been developed by Lockheed Missiles & Space Co. Completion of the new information retrieval language, known as DIALOG, was announced by the firm's Information Sciences group at the LMSC Palo Alto Research Laboratory. Dr. Roger K. Summit is developer of DIALOG and project leader for its implementation at Ames Research Center under a contract from NASA. Since May 1, Ames has been equipped with a DIALOG-fed remote terminal linked by telephone lines to a computer at LMSC. The system gives each user a new degree of control over the computer. Technical librarians in industries throughout the United States spend thousands of hours annually combing indexes for references to technical information required by scientists and engineers. But using DIALOG, the same librarians could query a computer system — in layman's terms — and receive the references they need in a matter of minutes . "DIALOG operates in what we call 'random-access' fashion," says Summit. "The system can be operated in 'on-line' manner. If queried with a few key words or phrases, it can find the proper references almost instantly. Use of appropriate terms permits retrieval of information in areas as narrow as "thrust vector control systems for large chemical rockets" or as broad as "radio." Subjects as specialized as "Interaction of the Magnetosphere and Solar Winds" and "Vibrational Excitation of Carbon Dioxide" also can be developed through use of DIALOG. By successively refining his commands, the user can subdivide and browse through the computer's files until he finds as specific and satisfying a group of references as he needs. Summit forsees a wide range of applications for DIALOG.

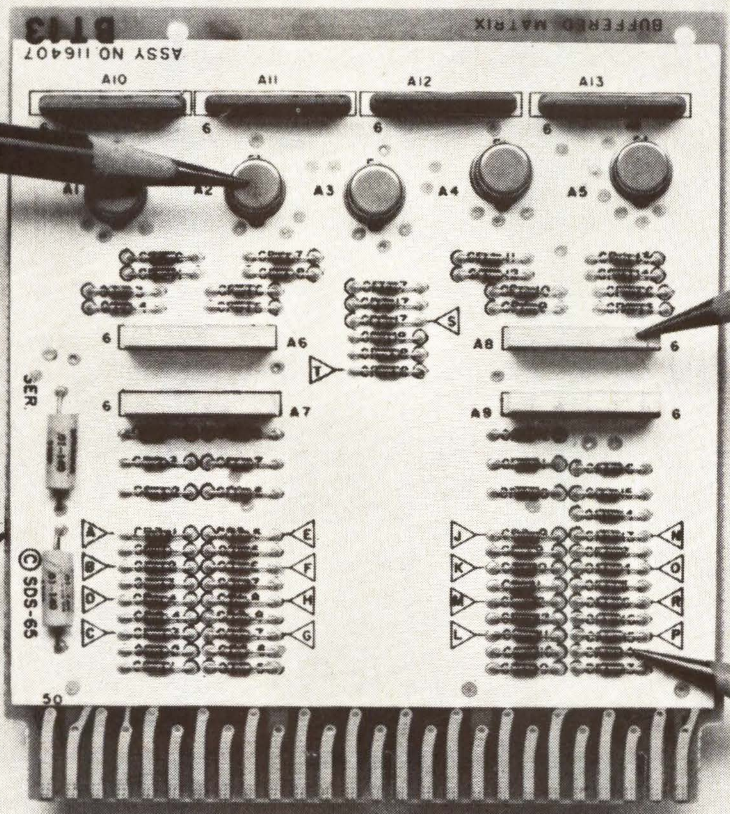
Our I.C. digital modules reject more noise than anybody's.

Integrated flip-flops, inverters and buffer amplifiers in T Series modules are made to our proprietary design and hermetically sealed in TO-5 cans.

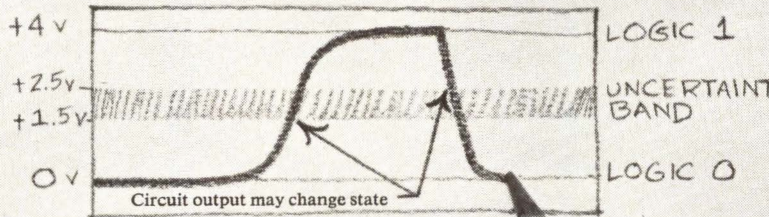
T Series input and load resistors, made to much tighter tolerances than can be attained with integrated components, are mounted outside the integrated circuit containers, eliminating power dissipation problems.

Full-width copper ground plane sandwiched between epoxy-glass boards minimizes circuit inductances and discourages noise spikes. Mounting cases also have full-width shield planes to retard noise coupling between logic wiring.

Discrete input diodes enable us to place the switching threshold right in the middle of the logic swing.



The payoff.



T Series logic levels are 0 and +4 volts, and noise rejection is 1.5 volts minimum, leaving a maximum uncertainty band only one volt wide within which noise can trigger the circuit output. This uncertainty band of 25% is far narrower than those of other I.C. modules on the market.

SDS

Scientific Data Systems, Santa Monica, California

FET MULTIPLEXER SENSING SCHEME FOR CORE MEMORIES

Low-level field-effect-transistor multiplexer is described as a new technique for significantly simplifying sense amplifier design.

The bit plane of a large high-speed core memory is usually divided into a number of sensing sections, each with a separate sense line. This provides a good signal/noise ratio. In order to accept information from any one of these sense lines, one of the schemes shown in Fig. 1 is normally used. This article presents a new sensing technique which uses a low level field effect transistor (FET) multiplexer (Fig. 2) to switch in signals from various sense lines into a single sense amplifier. This technique was employed with the 15,000 word, 1 us, 3D core memory used as a central memory in Burroughs' B3500/B2500 computer systems.

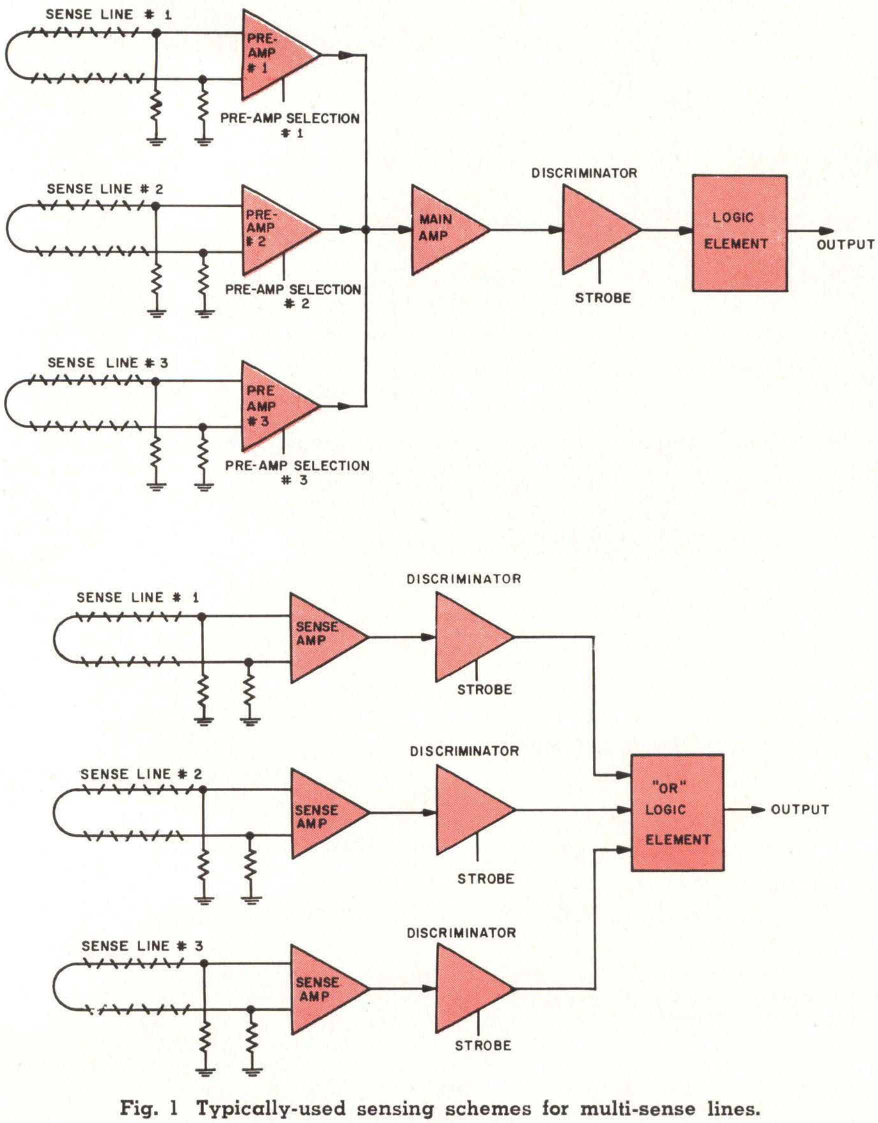


Fig. 1 Typically-used sensing schemes for multi-sense lines.

Low-Level FET Multiplexer

In the sensing scheme depicted in Fig. 2, the multiplexer consists of seven pairs of FET switches; six pairs for six sense lines plus an additional pair. Each sense line requires a pair of FET switches, since sense signals are balanced. During read time of the memory cycle, one pair of switches is turned ON, thus accepting information from the corresponding sense line. During write time, all of the sense line switches (six pairs) are open, thus blocking entry of any inhibit noise into the sense amplifier. This opening of all sense line switches, during write time, eliminates sense amplifier inhibit recovery problems. The additional pair of switches (called dummy) with short input is essential as a means for preventing the sense preamplifier input from floating during non-read time. This pair of switches is turned ON only during the non-read time.

Fig. 3 shows the equivalent circuit of the FET multiplexer during read time. For a typical memory 1 signal, which may be a ($\sin^2$) pulse, with a duration of 200 nsec, a very small amount of attenuation is offered. However, this only occurs if the differential amplifier input impedance is high. Also present during read time is the coupled noise due to read currents. This noise is in the form of common mode ringing at approximately 10 MHz. The r_{ds} (ON) of the switches, and the capacity of all OFF switches, provide an attenuation to this high frequency noise.

This attenuation, though small at high frequencies (10 MHz), can convert common mode noise into differential noise if there is variance in the attenuation of the switches which comprise the pair being used, thus deteriorating signal/noise ratio. To achieve common mode rejection in the range of 25 at 10MHz, r_{ds} (ON) is matched within 20 ohms. Capacity balance, to a degree, is to be expected since it is summation of capacities due to several OFF switches.

The positive inhibit noise pulse that can be blocked will be the gate-source breakdown voltage (30V) minus applied OFF bias (12V) while the negative inhibit noise pulse that can be blocked will be the applied OFF bias (12V) minus gate cut-off bias (8V). As shown in Fig. 4(a), inhibit noise voltages of as much as 3 volts can be blocked in the present scheme. Fig. 4(b) shows typical switching transients as compared to a typical 1 signal.

When any pair of switches is turned ON or OFF, charging or discharging of gate capacities produces transients. These transients are mostly common mode in nature and are, for the most part, rejected by the differential preamplifiers. Amplitude and time constants (of switching transients) can be further reduced by overlapping gate switching waveforms in such a way that one pair of switches is always ON while the other is switching as shown in Fig. 5.

Sense Amplifier

The differential preamplifier shown in Fig. 6 not only provides differential gain but also converts bipolar sense signals into positive polarity signals, thus eliminating the need for a dual comparator. Its high input impedance makes attenuation of sense signals in switches negligible. Further, it reduces the discrimination uncertainty window of the differential comparator by the factor of gain. Since the preamplifier is not exposed to inhibit recovery problems, it is ac-coupled. This eliminates the problem of zero shift and the need for individual adjustment usually required for typical dc sense amplifiers.

The differential preamplifiers output goes to one of the inputs of the high-speed differential comparator

RAMAN SARDA

Mr. Raman Sarda received a B.E. (Honors) degree from Engineering College, Jabalpur, India, and a M.S.E.E. from Stanford University. In 1964, he joined Burroughs Corp. in Pasadena, Calif. where he was engaged in B2500 systems memory development. Currently, he is with Lockheed Electronics Co. in Los Angeles, Calif.

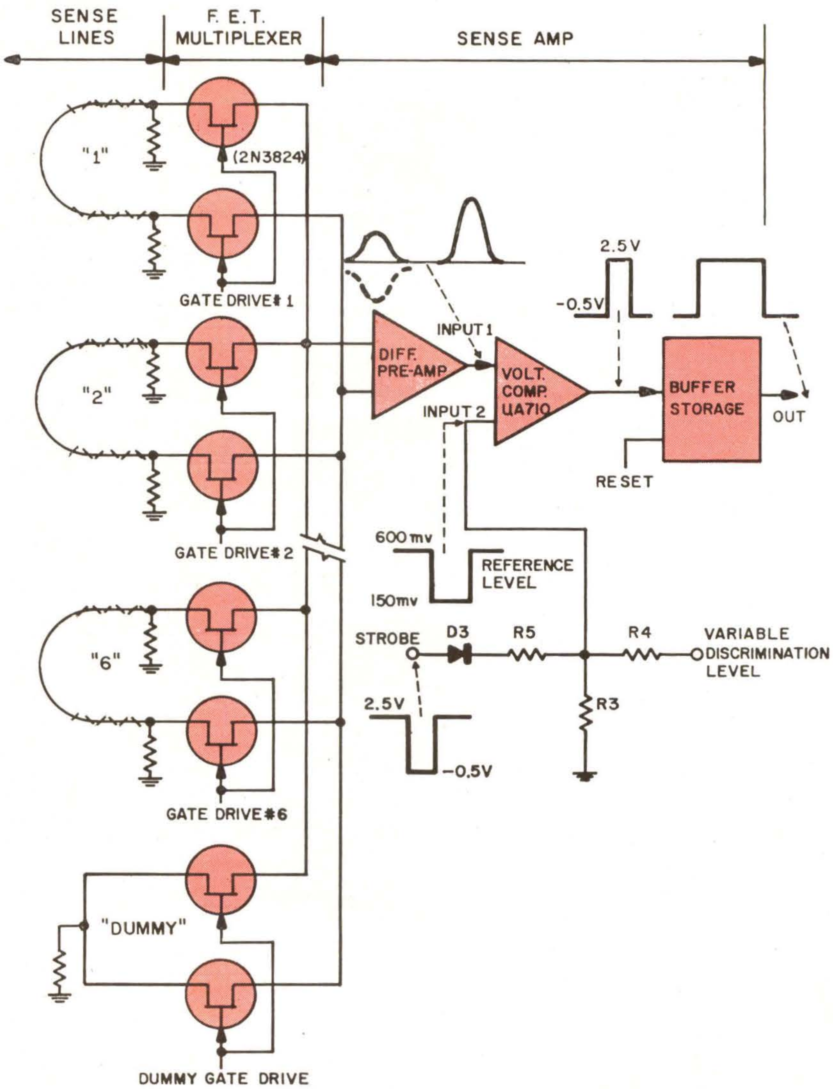


Fig. 2 Schematic of the FET multiplexer sensing scheme.

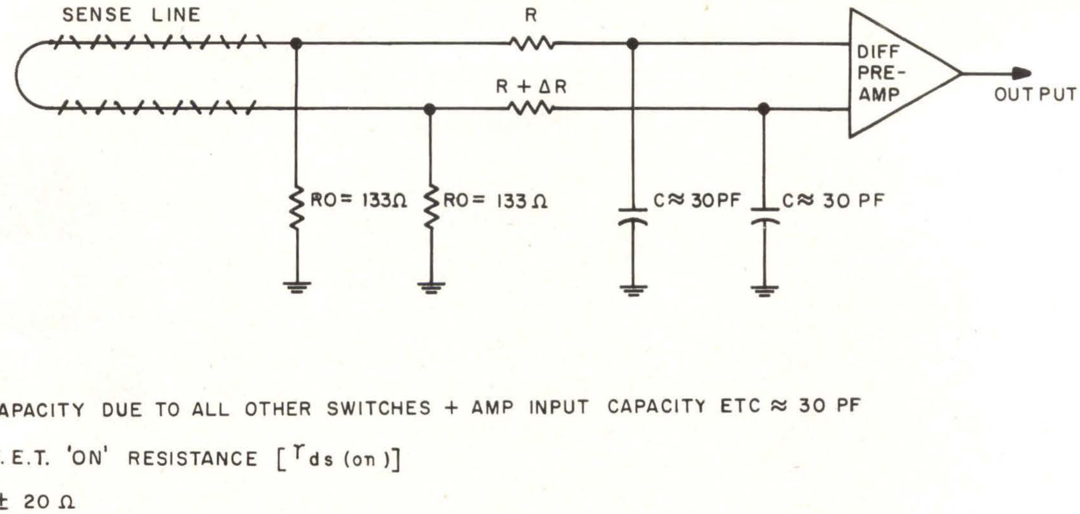


Fig. 3 Equivalent circuit of ON switch.

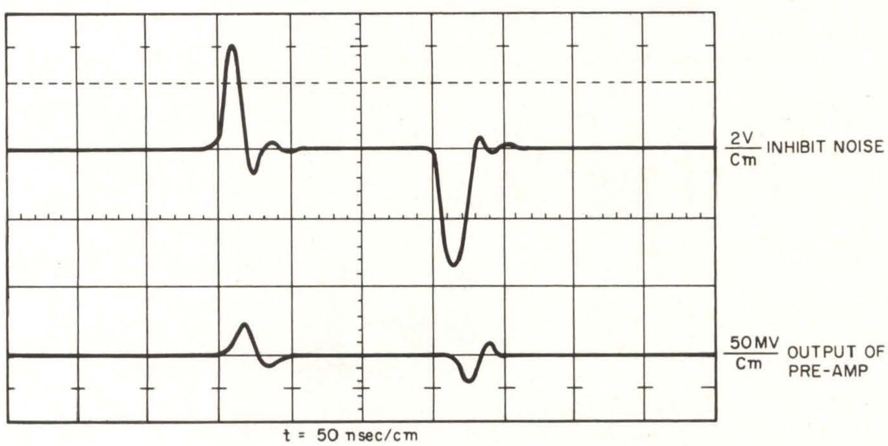


Fig. 4(a) Inhibit noise blocking.

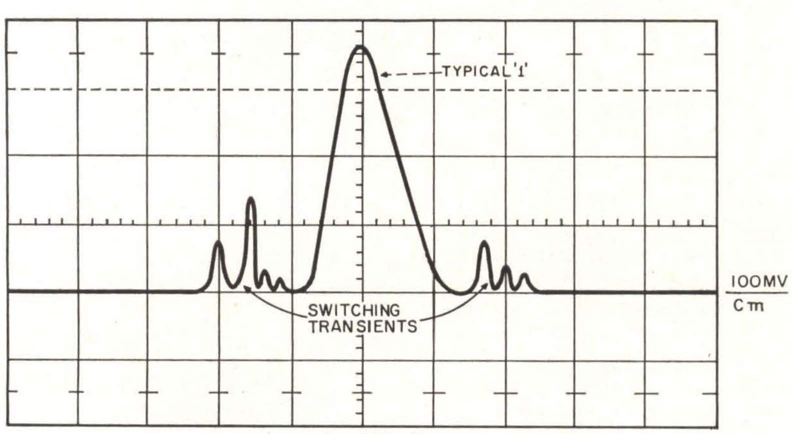


Fig. 4(b) Typical 1 signal and switching transients.

(Fairchild ua710) where it is compared with the reference level fed to the other input. If the signal level exceeds the reference level, then a pulse of 3.0 volts (typical 1) results at the output of the differential comparator. As was shown in Fig. 2, the strobe pulse is fed to diode D3, thus clamping the reference level to +0.6 volt during non-strobe time. This blocks the firing of the differential comparator due to switching transients or core delta noise peaks. During strobe time, D3 is cut off and the reference level decreases to a normal discrimination level. Timing of the strobe pulse edge is selected around the peaking time of the sense 1 signal so as to provide discrimination at a maximum signal/noise point. The output of the differential comparator, which is a narrow pulse, is further stretched and buffered before it goes to the memory output terminals.

Conclusion

FET multiplexing provides an excellent technique for selecting sense lines. Inhibit noise is blocked from the sense amplifier thus eliminating inhibit recovery problems, and therefore, simplifying sense amplifier design considerably. Problems of switching transients and of high-frequency common mode transmission along switches can be overcome satisfactorily. Though this technique was developed for a 1 us memory, it has potential usage at even faster speeds. ■

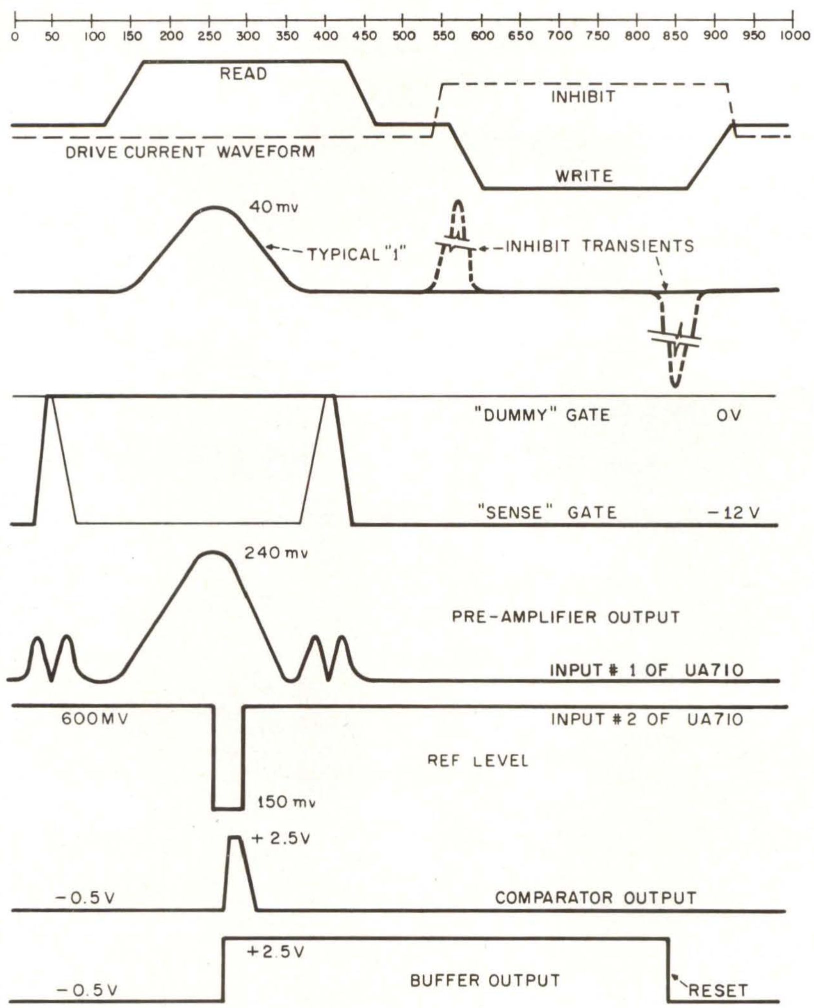


Fig. 5 Timing waveforms in a typical memory cycle.

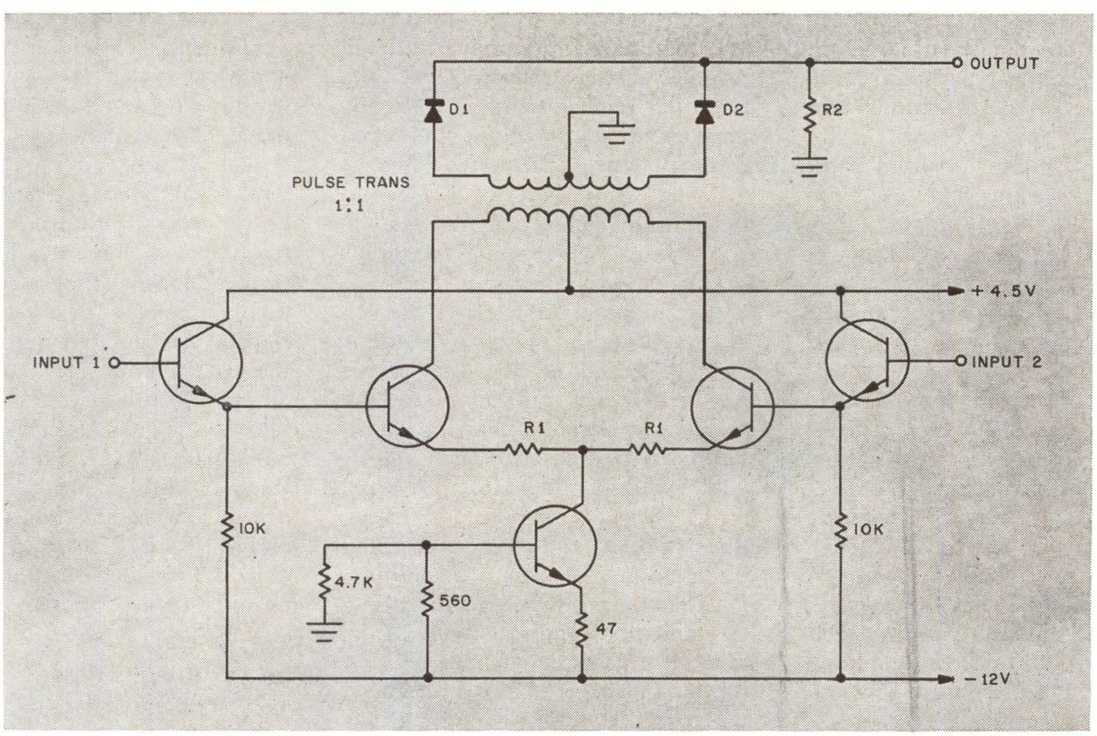
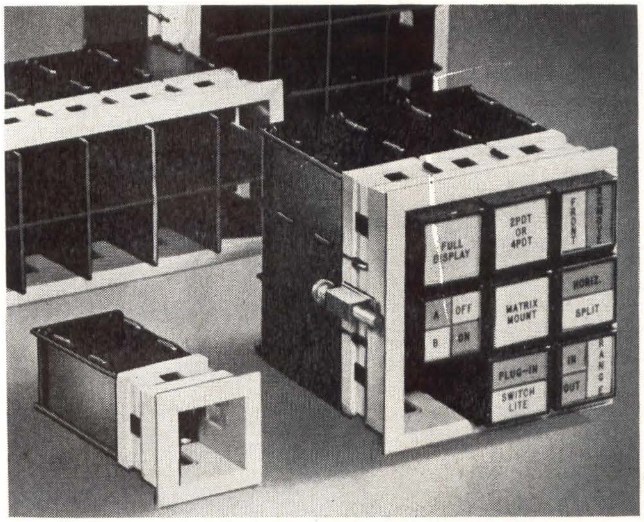


Fig. 6 Schematic of differential preamplifier.

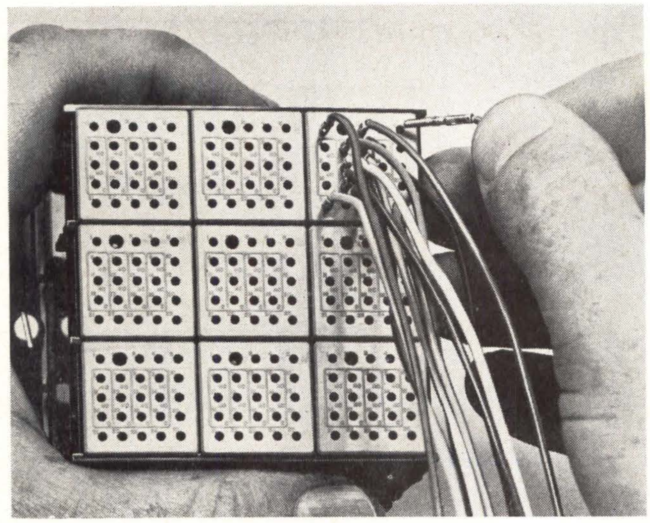
Special New Product Announcement

LIGHTED PUSHBUTTON SWITCHES

Plug-in switch modules feature pre-assembled mounting racks and crimp-type wiring terminals



Master Specialties' new lighted pushbutton switches are said to be the first to offer pre-assembled mounting racks and terminal band assemblies. The racks only require one front panel cutout per assembly.



The use of crimp-type wiring terminals allows faster installations.

Claimed to be an entirely new concept in plug-in lighted pushbutton switches, a new line of modules offers increased display area-to-switch size ratios, more efficient use of front panel space, crimp-type wiring, and pre-assembled custom mounting racks that will hold up to 144 switches in a single panel cutout, secured without visible hardware. The new unit, designated the 800 Square Tellite Switch by Master Specialties of Costa Mesa, California, gets its name from the square display and module dimensions that allow mounting on 0.800" centers.

Housed in a module reduced to the smallest possible size compatible with finger tip operation, the lighted pushbutton switch employs a 0.750" lens frame and a display face that may be used for displays from full to four-way splits, easily accommodating up to four lines of legend. Four T-1 ¾" miniature incandescent or neon lamps provide illumination and remain stationary during switch actuation.

Another exclusive feature claimed for the new switch is the finger tip plug-in or removal of the module from the mounting rack. The unit has integral and well-marked pin-type terminals which mate with the terminal blocks secured into the mounting rack assembly. Both terminals and mating block are keyed to an integral guide post to prevent erroneous installation. Accidental loosening of connections or removal is prevented by engaging the unit's locking device.

The manufacturer states that a wide proliferation of component part choice has been developed. Switches may be designed to fulfill almost any specific application requiring an illuminated pushbutton switch. Variables available are: lamp selection, display screen configurations, lenses, filters, colors, and choice of lamp illumination sequence. In addition, if switches are not needed, they may be eliminated, allowing the unit to be used as an indicator only.

Highlighting the newly-introduced switch are the custom mounting rack and terminal block assemblies, supplied completely assembled. Racks house from one to 144 switches in maximum matrix configurations of 12 x 12 or 5 x 20. The entire switch/mounting rack assembly requires only one panel cutout to mount from one to 144 switches. The crimp-type terminals are intended to reduce installation time and produce long term reliability. These terminals may be crimped onto harness wires in a fraction of the time required by other conventional methods, according to the company. Once installed, terminals are inserted into the well-marked terminal block on the back of the mounting rack, enabling the plug-in module to be placed into immediate service. However, should the need arise, these universal terminals may be soldered onto a wide range of wire sizes and still retain their ability to be installed into the terminal blocks rapidly.

For more information on these new switches:

Circle No. 108 on Inquiry Card

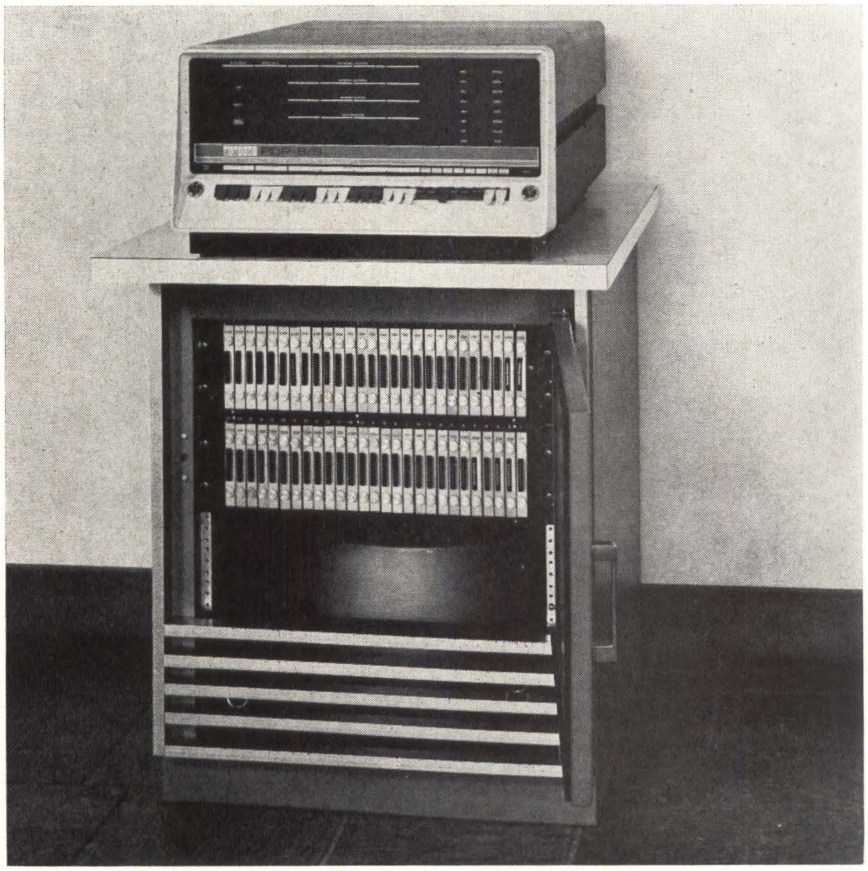
A MEMORY-EXPANDER DRUM

Drum system developed for the PDP-8/S increases computer power 33 times while just doubling the price

The PDP-8/S computer, introduced by Digital Equipment Corporation about ten months ago, has proved to be so popular that nearly 600 have been ordered. As a single-address, 12-bit-word-length serial computer with 4096 word core memory, the PDP-8/S is relatively slow (36 usec. add time) but well-suited to a wide variety of control applications. The price, at around $10,000, makes it one of the least expensive general-purpose computers available. In addition to low cost, the PDP-8/S uses a bus I/O system which permits interfacing with up to 64 peripheral devices on an effectively time-shared basis.

Full utilization of these capabilities, in most practical cases, requires program and data storage far beyond the basic 4096-word core memory provided. Additional stacks may be obtained (up to 32,768 words), but a far less expensive technique, which also offers greater capacity, is the use of an external magnetic surface memory system. Such a system has been designed which can be plugged into the PDP-8/S for immediate use, offering 131,072 word capacity, complete interface hardware, and all necessary drum routines pre-recorded on the drum, at a cost of only $9,950. The drum systems, designated the 1104S, were developed by Vermont Research Corporation, of North Springfield, Vermont, and are being manufactured and marketed by this firm. Versions are available for other small computers. Systems software was developed under a VRC contract, by Bedford Associates, Inc., of Bedford, Mass.

The extended capacity is equal to 32 additional 4K stacks, and can serve as data or program storage. A number of programs and subprograms may be stored, and called for as a part of the program being run, with transfer on an individual-page basis, at 138 msec. per page, or in 6- or 7-page groups. The entire replacement of a core requires 4.4 seconds. The drum may be operated under interrupt mode, thus allowing the computer to process other data while transfer is being accomplished. Word transfer is at the rate of one word per millisecond, which allows time for the PDP-8/S to accomplish some processing between drum interrupts. The drum can be easily modified to achieve rates up to one word every 17 microseconds, for use with a PDP-8 with data break.



Vermont Research Corp.'s 1104S-8/S drum system is housed in a specially-designed cabinet with easy access to interface electronics.

Program and data transfers may be made a part of the object program, or called for by external inputs. A complete package of software routines is provided to allow read and write transfers to and from the drum. For example:

- A routine that transfers all but the last page of core (tape loaders and the counters of the transfer routine use the last page)
- Routines to effect transfer of a selected number of pages with or without program interrupt
- A drum diagnostic routine.

Normally, exchange of programs in the PDP-8/S requires running in the object tape on the ASR-33 tape reader, which may require as much as 13 minutes; with the 1104S drum system, this transfer can be accomplished in less than 5 seconds. This quick-change feature reduces non-productive computer time. In the assembly of new programs, which can require several hours of read-in and punch-out operations, the time-saving can amount to over 75%. Changes and corrections are also speeded and simplified. The ability to switch programs, and even assemblers, in a few seconds under program control will allow the computer to be used in many more applications than previously thought feasible. Longer, more sophisticated programs may be used, increasing the usefulness of the computer in all applications. In machine and process control, or when used as a peripheral computer in a EDP complex, the 1104S-8/S unit can monitor and direct up to 62 I/O devices, with complex processing. As a substitute for a time-sharing terminal, it is cost-competitive and requires no cabling. As a time-shared instructional computer, it is economically feasible for schools. The overall effect is that of a computer, capable of limited time-sharing and general multiprocessing, operating at speeds suitable for nearly all process control applications, with capacity for more than 128K words and up to 62 additional I/O devices, and available at a total cost of less than $20,000.

Three models of the 1104S serial drum system are currently available to interface to computers using program-controlled transfers (I/O channel); data channel transfers (3-cycle data break); and direct memory access channel (single-cycle data break). For more information on these systems:

Circle No. 102 on Inquiry Card

negative radix arithmetic

Part 4 Multiplication and Division

Editor's Note: This series of articles on negative radix arithmetic was introduced in the May issue followed by Parts 2 and 3 in the June and July issues, respectively. To date, the advantages, terminology, conventions, and properties of negative radix systems were discussed and addition and subtraction operations in negative decimal arithmetic were illustrated.

The major obstacle in learning negative radix arithmetic is remembering — consistently — to change the signs of the carries. A lifetime habit is not easily bypassed and remembering to change the sign of the carry, each and every time one occurs, is very difficult to do. Most readers will by this time have found that virtually all of their errors were in failing to follow this rule. Before progressing from the simple two-operand operations, discussed in Part 3, to multiplication and division, it would be appropriate to study multiple-operand addition briefly. In two-operand addition, carries are 0, 1, and N; in multiple-operand addition, the possibility of carries greater in magnitude than unity arises. This is true also in multiplication.

The fact that addition of numbers expressed in negative radix notation is pure addition is of some potential importance in machine computation, since the addition of such numbers is accomplished by forming the true sum of all of the operands; by contrast, in positive radix notation the addition of numbers of mixed signs is done by forming separate sums for the positive numbers and the negative numbers, and then taking the difference of the two sums. Therefore, the digit-oriented operation of negative radix notation again offers advantages over the operand-oriented operations of positive radix notation, and single-stage, multiple-operand adders are quite feasible. These properties can be illustrated here by means of examples.

A purist might protest that rigor demands that tables similar to those in Part 3, including carries of magnitude greater than unity, be presented for the execution of these examples. Fortunately, this is not a rigorous presentation and we can assume that the reader will have no trouble dealing with larger magnitude negative carry digits, either operationally or conceptually. The problem does not arise at all in machine computation, since only one digit product at a time is added to the partial product in normal multiplication, and the so-called simultaneous multiplication is a special and distinct problem. We shall, therefore, not present special addition tables for negative carry digits; the procedure can be considered to be identical to subtracting positive carry digits.

In the following examples, the examples on the left are in negadecimal, and those on the right are in decimal; the underlined digits on the top represent the carries-in. Note that, as in Part 1, we are denoting negative digits by bold-face type.

• Example 1 Add:

2321	1211
821	+ 781
1934	− 126
18974	+ 2834
56035	+ 43975
9862	− 8258
41206	+ 39206

M. P. deRegt

• Example 2 Add:

12432	**1011**
48971	+32831
5854	− 4246
6342	− 5738
1775	− 365
795	+ 615
184915	−23105
000012	−00008

These examples should illustrate quite clearly the superiority of negative radix arithmetic where addition of more than two operands is concerned. In manual multiplication, of course, mixed polarities do not occur in the addition phase; this is taken up in the next section.

MULTIPLICATION

Multiplication of negadecimal numbers is exactly the same as multiplication of unsigned decimal numbers, except, of course, for changing the sign of the carry. In negadecimal arithmetic, however, the same algorithm is used regardless of the polarities of the operands and the proper product polarity is automatically produced.

The difference between decimal and negadecimal multiplication of numbers of mixed polarity is shown in Fig. 1 which is a combined flow chart of the operations. The end of the operation is reached for negadecimal as soon as the multiplication proper is complete; for decimal, it is still necessary to develop the sign of the product by comparing the signs of the operands according to the law of signs for multiplication.

Following the pattern set in the previous article, for addition and subtraction, the multiplication table for negadecimal would look exactly like the corresponding decimal table, except the sign of the carry digit (the left-hand digit of the two-digit product) is negative or zero. For example, 4 x 7 = **2**8 for negadecimal, and +28 for decimal. The proper negadecimal product, of course, is 188, but it is much easier to add a −2 (subtract 2) than to add 18 for the carry.

In fact, there is a tendency to write down at the same time **both** of the two product digits which might be formed by a multiplier digit and the most significant multiplicand digit. This is all right in decimal; in negadecimal, however, it will not work. Only one digit at a time can be set down; the higher order digit of a pair **must** be considered a carry digit, with the sign appropriately changed. This is illustrated in the second multiplier digit of the following example where, as usual, the negadecimal example is on the left and the decimal on the right.

- Example 3 Multiplication of two positive numbers (+, +):

267	+ 147
374	+ 234
628	+ 588
19189	+ 441
561	+294
046418	+34398

In this example, let us compute the second partial product line formed by the multiplier digit "7."

(1) 7 x 7 = 9, carry −4;
(2) (7 x 6) −4 = 8, carry −3;
(3) (7 x 2) −3 = 1, carry −1;
(4) 0 − 1 = 9, carry +1; **not** (7 x 2) −3 = 11
(5) 0 + 1 = 1

Other examples follow for the remaining combinations of operand polarities.

- Example 4 (+, −):

267	+ 147
1846	− 234
922	− 588
628	− 441
19236	−294
267	−34398
0175602	

- Example 5 (−, +):

1953	− 147
374	+ 234
1592	− 588
1031	− 441
1659	−294
175602	−34398

- Example 6 (−, −):

1953	− 147
1846	− 234
1298	+ 588
1592	+ 441
2984	+294
1953	+34398
0046418	

Multiplication and Division Nomenclature

Negative radix multiplication, addition, and subtraction are easier from any point of view than the corresponding conventional operations simply because intrinsically fewer steps are involved; this is true as a direct consequence of the fact that in each case knowledge of sign is incidental to the procedure rather than intrinsic to the operation.

In division, however, knowledge of sign or polarity is intrinsic to the operation. Intuitively, division, as an operation, may be referred to a number line, the object being to determine how many times a given interval (the divisor) can be stepped off from the starting point (the dividend) without crossing zero. Therefore, by definition, the process is complete when the next step would cross the zero point to land in the number sequence of opposite polarity from the starting point. In short, the test for completion of the operation, as defined, is a comparison of the polarity of the remainder with the polarity of the dividend. Therefore, the property of negative radix notation which is advantageous in addition, subtraction, and multiplication is a disadvantage in division. However, this disadvantage applies primarily to manual arithmetic, where it is of no particular importance; in automatic computation, easy polarity detection substantially reduces the importance of the disadvantage.

In fact, manual negaradix division is much more involved in virtually all ways than the automatic variety. At the same time, a study of manual arithmetic is important for the insight it provides into the requirements for automatic division. There is no getting around the fact, however, that manual negative radix division is an intricate, difficult, and exasperating experience. However, it is a fascinating one, and a successfully-completed long division can be counted as a genuine achievement.

Since a division operation is so intricate, it will be useful to define carefully all of the various quantities occurring in the course of it. Because multiplication and division are indeed processes with identical quantities appearing in reverse order, the terms will be defined reciprocally, using a common set of symbols. This will simplify any algebraic analysis that might be useful.

Again, rather than concentrating on a rigorous presentation, we will make use of the reader's knowledge of division, existing conventions, and his intuition, by using examples to define terms. Accordingly, the terms are used in Figs. 1 and 2, flow charts for multiplication and division. Their reciprocal relationships and symbols are shown in Table 1, and their identities in Tables 2 and 3. As may be expected, the i subscripts refer to the standard polynomial position numbers, which are identical to the corresponding radix superscripts; r is the radix. Note that the division operation (Table 3) illustrates the performance of 154398 ÷ 263, the result of which is 587 with remainder 17, and the multiplication operation (Table 2) illustrates the operation 263 × 587 + 17, the result of which is 154398. The initial partial product of 17 in Table 2 is not a proper part of a normal multiplication but is included to represent the analogous quantity in division — the remainder.

The relationship and identity of the quantities and their names for the two operations can readily be traced in these tables. It should be remembered, in the discussions which follow, that a subscript **always** refers to the position number as used in the standard polynomial, and **not** to the order or sequence in which the corresponding digit or number is used or generated. Capital letters generally refer to entire numbers, and lower case to individual digits.

One further distinction can usefully be made; it acknowledges the fact that some division algorithms may produce a non-zero remainder opposite in polarity to that of the dividend when the procedure is complete. Such a quotient or remainder, and the division algorithm itself, will be called "improper"; when the remainder is zero or of the same polarity as the dividend, the quotient, remainder and algorithm will be called "proper." Although such a fine distinction is more germane to a discussion of machine arithmetic, it will be found useful here, too.

INTRODUCTION TO DIVISION

Manual negative radix division is not only intricate and difficult, as stated earlier, it is downright frightful. Any hope of using negadecimal in manual calculation which might survive the many other valid objections withers completely when division is approached. Fortunately this frightfulness does not apply to machine division; in fact, machine negative radix division has all of the advantages of normal division using sign-and-magnitude notation, and none of the disadvantages of division using complementary notation. It also has some advantages and some disadvantages unique to itself.

This contrast between the complexity of manual and the ease of machine division stems from the contrast between the ways in which people and machines compute, together with the many steps and sub-operations of virtually any successful division algorithm. In manual decimal division, these include multiplication and comparison of magnitude. Comparison of polarities is easy because of the presence of explicit-polarity indicating symbols. In manual negadecimal, comparison of numbers of even the same polarity is difficult; where the polarities are opposite, it is well-nigh impossible. Although a modest amount of mental calculation can be used, this is a far more complex process than the simple comparison of symbols possible in normal decimal. Comparison of polarities requires essentially counting the number of digits in each of the two operands. In machine computation, the problems for the two notations are very similar although polarity detection is somewhat more complex in negative radix devices.

The importance of explaining and developing manual negative radix division lies in the fact that the key to the design of efficient, simple machine algorithms is

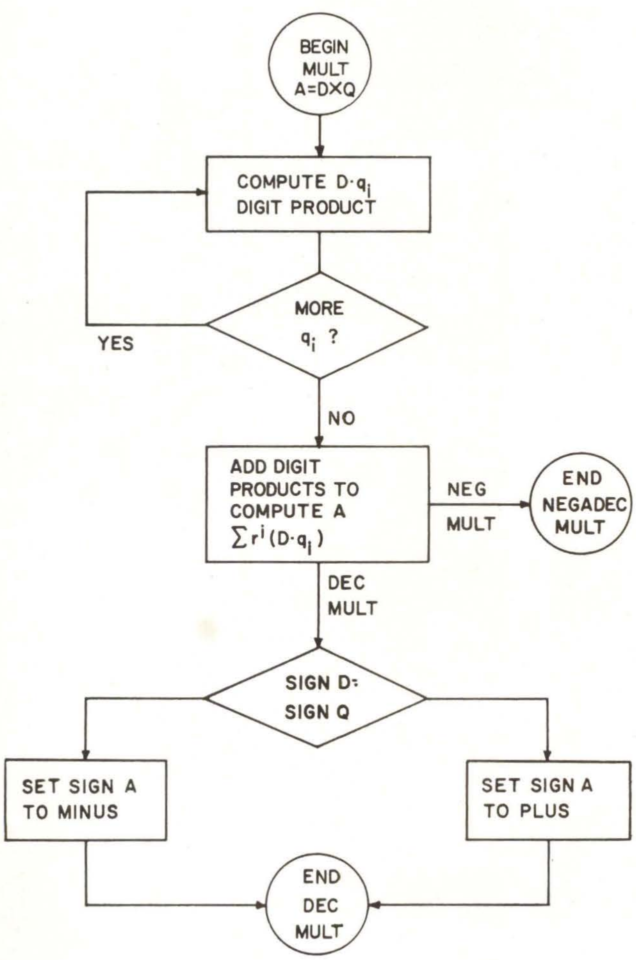


Fig. 1. Flow chart for decimal and negadecimal multiplication.

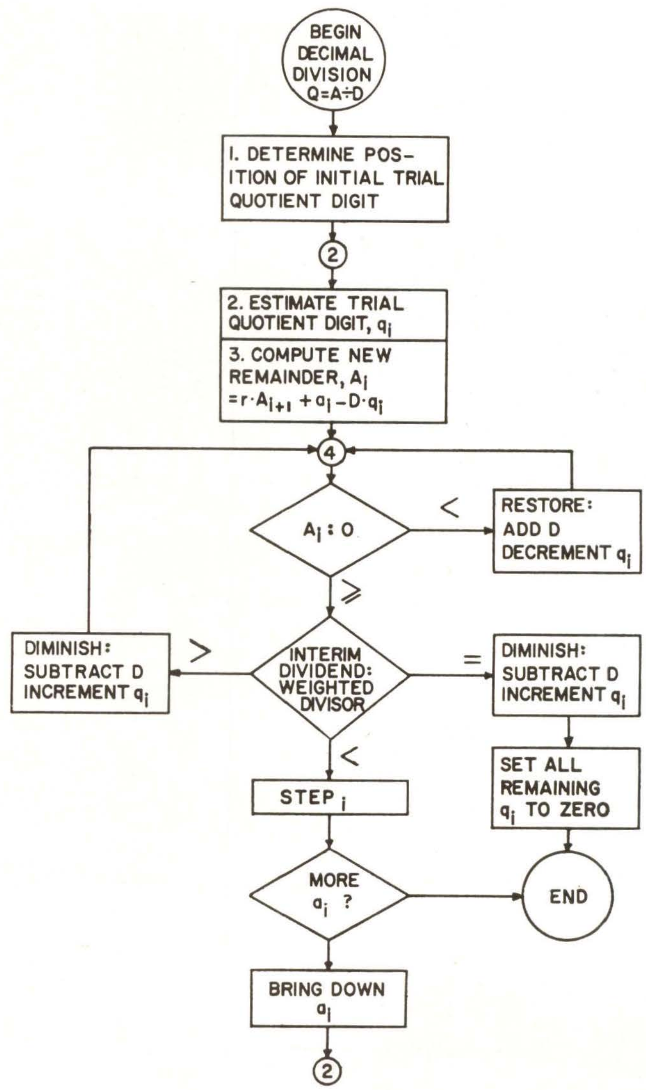


Fig. 2. Flow chart for manual decimal division of unsigned numbers.

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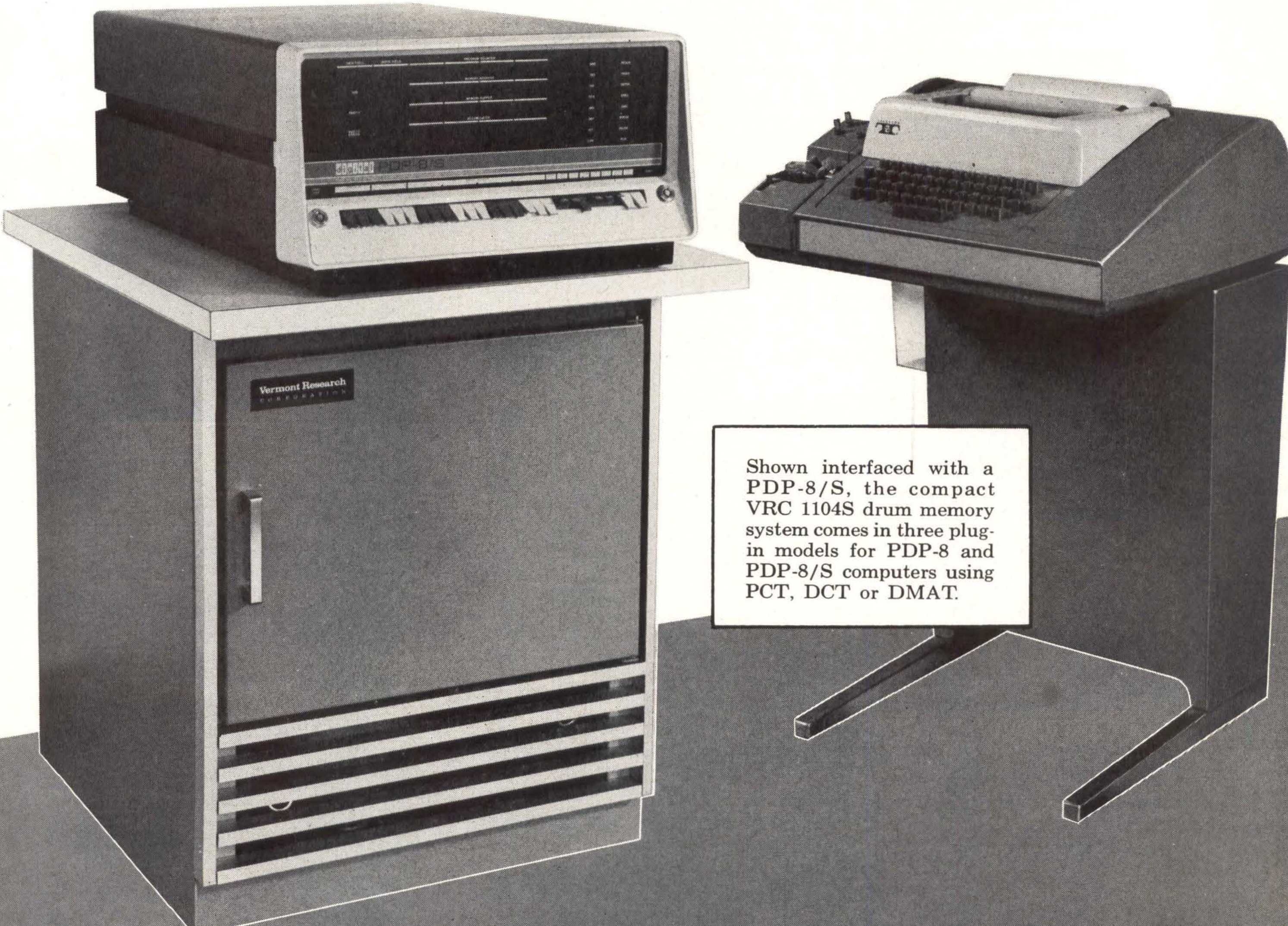


Shown interfaced with a PDP-8/S, the compact VRC 1104S drum memory system comes in three plug-in models for PDP-8 and PDP-8/S computers using PCT, DCT or DMAT.

negative radix arithmetic

continued

more a matter of familiarity with the inherent idiosyncracies of negative radix division than a precise mathematical analysis of the operation. As stated earlier, such familiarity is much more easily achieved through examples in negadecimal than in negabinary.

Since we do decimal division without being conscious of the many human capabilities on which this operation draws, it would be fruitful first to analyze a division operation. The flow chart of Fig. 2 makes it clear that the manual algorithm is really a combination of several relatively-independent algorithms. The steps corresponding to these algorithms are as follows:

(1) Determine initial trial quotient digit position.

(2) Determine trial quotient digit.

(3) Compute the new remainder.

(4) Test remainder and adjust quotient and remainder if necessary.

(5) Obtain next partial dividend (bring down next digit). Repeat steps (2) to (5).

As an example of the relative independence of these steps, the decision as to which of several algorithms will be used for step (4) may be made without regard to the other steps in the division process. Assuming that the test of step (4) shows the trial quotient digit to be incorrect, the quotient may be adjusted by any of several methods. One is to substitute a new trial quotient, and then to repeat step (3); this procedure is not really a very good one. A second method is to estimate an incremental quotient based on the new remainder and then to repeat steps (2) and (3) using the increment. A third method, which will minimize the agony all around, is to add or subtract the divisor to or from the remainder and to make corresponding unit adjust-

TABLE 1

MULTIPLICATION AND DIVISION NOMENCLATURE AND SYMBOLS

SYMBOL	MULTIPLICATION	DIVISION
D	Multiplicand	Divisor
Q	Multiplier	Quotient
A	Product	Dividend
q_i	i^{th} multiplier digit	i^{th} quotient digit
$D \cdot q_i$	i^{th} digit product	i^{th} digit product
a_i	i^{th} product digit	i^{th} dividend digit
A_i	i^{th} partial product	i^{th} remainder
$r \cdot A_{i+1} + a_i$	i^{th} sum	i^{th} partial dividend
$r^i \cdot A_i + \sum_{0}^{i-1} r^i a_i$	Interim product	Interim dividend
$r^i (D \cdot q_i)$	Weighted digit product	Weighted digit product
$r^i (r \cdot A_{i+1} + a_i)$	Weighted sum	Weighted partial dividend

TABLE 2

MULTIPLICATION NOMENCLATURE

Symbol	Quantity to left of Vertical Line	Multiplication	Quantity on Entire Line	Symbol
D	Multiplicand	+263	Multiplicand	D
Q	Multiplier	+587	Multiplier	Q
A_0	Partial Product (initial)	+17	Interim Product (initial)	A_0
$D \cdot q_0$	Digit Product	+1841	Weighted Digit Product	$D \cdot q_0$
A_1 $10A_1 + a_0$	Sum Partial Product	+1858 +185 8	Interim Product	$10A_1 + a_0$
$D \cdot q_1$	Digit Product	+2104 0	Weighted Digit Product	$10 \cdot D \cdot q_1$
A_2 $10A_2 + a_1$	Sum Partial Product	+2289 8 +228 98	Interim Product	$10^2 \cdot A_2 + 10a_1 + a_0$
$D \cdot q_2$	Digit Product	+1315 00	Weighted Digit Product	$10^2 \cdot D \cdot q_2$
A_3 $10A_3 + a_2$	Sum Partial Product	+1543 98 +154 398	Product	A

TABLE 3

DIVISION NOMENCLATURE

Symbol	Quantity to left of Vertical Line	Division	Quantity on Entire Line	Symbol
		+263	Divisor	D
		+587	Quotient	Q
A_3	Remainder (initial)	+154 398	Dividend	A
$10A_3 + a_2$	Partial Dividend	+1543 98	Dividend	A
$D \cdot q_2$	Digit Product	+1315 00	Weighted Digit Product	$10^2 \cdot D \cdot q_2$
A_2 $10A_2 + a_1$	Remainder Partial Dividend	+228 98 +2289 8	Interim Dividend	$10^2 \cdot A_2 + 10a_1 + a_0$
$D \cdot q_1$	Digit Product	+2104 0	Weighted Digit Product	$10 \cdot D \cdot q_1$
A_1 $10A_1 + a_0$	Remainder Partial Dividend	+185 8 +1858	Interim Dividend	$10A_1 + a_0$
$D \cdot q_0$	Digit Product	+1841	Weighted Digit Product	$D \cdot q_0$
A_0	Remainder (final)	+17	Final Remainder	A_0

ment to the quotient digit. This procedure is essentially that of reverting to a mechanical repeated subtraction algorithm applied only to quotient adjustment.

Each of the above steps will be explained separately and illustrated by examples.

• **Step 1: Determine the initial trial quotient digit position.** As taught in the good old days, this step consisted of covering up some of the lower order dividend digits, leaving as many high order dividend digits uncovered as there are divisor digits. This uncovered part is what we are calling the remainder, and is thus the "initial remainder." The position of the lowest order digit of the initial remainder establishes the position of the first trial quotient digit. If this initial remainder is less than the divisor, then the first quotient digit is zero. The next dividend digit is then included in the high-order group of digits to form the first partial dividend. The effect of this possibility is then merely to establish that the next lower order position is the location of the first non-zero quotient digit. On the other hand, if the initial remainder is greater than or equal to the divisor, then the position of the trial quotient digit is correct, and the initial remainder is the first partial dividend. In either case, the first quotient digit can then be determined.

In negadecimal division, things are not so straightforward. Consider the following multiplications:

$$\begin{aligned} 1909 \times 1909 &= 12321 \\ 909 \times 1909 &= 123321 \\ 909 \times 909 &= 1234321 \end{aligned}$$

The first product has five digits; in normal decimal, two four-digit factors result in a product of no fewer than seven digits. The third product has seven digits; in normal decimal, there would be no more than six digits. By posing these examples as divisions, the reader can establish for himself that the position of the highest-order digit can vary in either direction from that which would result from the algorithm described for normal decimal division.

However, it can be shown that this position is still a good one to start from and that it will, in many cases, be the correct one. As in decimal division, subsequent steps in the algorithm comprise automatic corrective action. It should be noted that this rule will provide a position which is correct from a polarity point of view; therefore if it is not numerically correct, the correct position will be two positions to either left or right.

• Example 7 Divide 321726 by 823 (step 1 only):

$$\begin{array}{r} \text{x} \\ 823\overline{)321726} \end{array}$$

• Example 8 Divide 1234321 by 909 (step 1 only):

$$\begin{array}{r} \text{x} \\ 909\overline{)1234321} \end{array}$$

• Example 9 Divide 12321 by 1909 (step 1 only):

$$\begin{array}{r} \text{x} \\ 1909\overline{)12321} \end{array}$$

• **Step 2: Determine the initial trial quotient digit.** Having established the place to put it, we can now try to establish what it might be. In decimal division, we do this by using our solidly-ingrained knowlegde of multiplication tables to estimate how many times, less than ten, that the divisor will go into the partial dividend. If the numbers are very large, we simplify the estimating process by considering only the first few divisor digits and cover up a corresponding number of partial divi-

TABLE 4

NEGADECIMAL DIVISION TABLE

	Quotient Digits															
Divisor Digits	17	18	19	00	1	2	3	4	5	6	7	8	9	190	180	170
19	003	002	001	00	19	18	17	16	15	14	13	12	11	10	20	
18	006	004	002	00	18	16	14	12	10	28	26	24	22	20	40	
17	009	006	003	00	17	14	11	28	25	22	39	36	33	30	60	
15	195	190	005	00	15	10	25	20	35	30	45	40	55	50	1900	
13	181	194	007	00	13	26	39	32	45	58	51	64	77	70	1940	
11	187	198	009	00	11	22	33	44	55	66	77	88	99	90	1980	
29	173	182	191	00	29	38	47	56	65	74	83	92	1901	1910	1820	
27	179	186	193	00	27	34	41	68	75	82	1909	1916	1923	1930	1860	
24	168	172	196	00	24	48	52	76	80	1904	1928	1932	1956	1960	1720	
21	157	178	199	00	21	42	63	84	1905	1926	1947	1968	1989	1990	1780	
37	149	166	183	00	37	54	71	1908	1925	1942	1979	1996	1813	1830	1660	
32	124	156	188	00	32	64	96	1928	1940	1972	1804	1836	1868	1880	1560	
47	119	146	173	00	47	74	1901	1948	1975	1802	1849	1876	1703	1730	1460	
42	294	136	178	00	42	84	1926	1968	1990	1832	1874	1716	1758	1780	1360	
57	289	126	163	00	57	94	1931	1988	1825	1862	1719	1756	1793	1630	1260	
52	264	116	168	00	52	1904	1956	1808	1840	1892	1744	1796	1648	1680	1160	
67	259	106	153	00	67	1914	1961	1828	1875	1722	1789	1636	1683	1530	1060	
62	234	296	158	00	62	1924	1986	1848	1890	1752	1614	1676	1538	1580	2960	
77	229	286	143	00	77	1934	1991	1868	1725	1782	1659	1516	1573	1430	2860	
87	399	266	133	00	87	1954	1821	1708	1775	1642	1529	1596	1463	1330	2660	
82	374	256	138	00	82	1964	1846	1728	1790	1672	1554	1436	1318	1380	2560	
98	366	244	122	00	98	1976	1854	1732	1610	1508	1586	1464	1342	1220	2440	
94	358	232	126	00	94	1988	1862	1756	1630	1524	1418	1492	1386	1260	2320	
90	330	220	110	00	90	1980	1870	1760	1650	1540	1430	1320	1210	1100	2200	

negative radix arithmetic

continued

dend digits.

Since our knowledge of the negadecimal multiplication is, at best, derived from our knowledge of the decimal tables, we have put the negadecimal tables in the form of Table 4. In this form, the table can be used directly to select a trial quotient digit.

The first two digits of the divisor are placed in the first column, marked "Divisor Digits." The first 2, 3, or 4 dividend digits are given in the body of Table 4, and the trial quotient digit (or digits) is read from the top line. Actually, each pair of adjacent partial-dividend columns represents a range so that the quotient digit should be selected which straddles the two columns. If the actual partial-dividend digits exactly match a table entry, then the quotient digit selected might be either of the two over that column. In any case, the digit is an estimate and its correctness is subject to subsequent tests on the new remainder which results.

The possibility that the trial position, determined in step 1, may be off by two positions to the left is reflected in the two right most columns, and is analogous to the situation in decimal where the trial digit is 9. If the trial quotient "digits" turn out to be 190 or 180, that really means that the initial trial position should have been two positions to the left, using a 1 as the trial digit. The second digit of 9 or 8 should not immediately be put down; it should be determined as a separate digit after the test on the 1.

The possibility that the initial trial position should be two positions to the right is analogous to the situation in normal decimal in which the initial trial digit is zero. It is not as clear cut in negative radix division, however, not only because the numbers are confusing, but also because division is naturally non-restoring. Thus a trial quotient digit of 1 might be correct, even if the divisor appears to be too large. The correctness must be tested in a later step, after computing the remainder.

The second, third, and fourth columns of Table 4, containing 3-digit numbers, have been provided for those cases where there are fewer digits in the dividend than there are in the divisor. An example is 6 divided by 18 (+6 ÷ −2). In this case, two zeroes should be placed before the dividend, in order to establish the initial remainder. The result is a dividend of 006, with a trial quotient of 17 or 18. The 1 is taken, over the second zero, as the trial quotient digit.

The use of Table 4 will be made clearer for step 2 by the following examples:

- Example 10 Perform step 2 for Example 7;

$$823\overline{)321726}\quad (\text{quotient } x)$$

Having established the position in step 1, we now look at the first two divisor digits, 82, and the first two partial dividend digits, 32. The divisor digits are in the left-hand column of the table, and 32 lies (in magnitude) between 00 and 82 in the 5th and 6th columns. Therefore, we select 1 as the trial quotient digit. In general, the larger of two possible digits should be selected, since we are dealing with non-restoring division, and also, if we have to adjust, it is easier to add than to subtract the divisor. We therefore have:

$$823\overline{)321726}\quad (\text{quotient } 1)$$

- Example 11 Continue Example 8 (step 2):

$$909\overline{)1234321}\quad (\text{quotient } 1)$$

The procedure and reasoning here are exactly the same as in Example 10.

- Example 12 Continue Example 9 (step 2):

$$1909\overline{)12321}\quad (\text{quotient } x)$$

In this case, looking on the "19" line, we find "12" between column headings 8 and 9. We select the "9", using the reasoning of the preceding examples:

$$1909\overline{)12321}\quad (\text{quotient } 9)$$

- **Step 3: Compute the new remainder.** This step is comparatively easy and straightforward. It actually comprises two sub-steps, as follows:

(3a) Compute digit product

(3b) Subtract digit product from partial dividend.

The result is the new remainder. Applying this step to the previous examples, we have the following:

- Example 13 Continue Example 10 (step 3):

$$\begin{array}{r} 1 \\ 823\overline{)321726} \\ \underline{823} \\ 1518 \end{array}$$

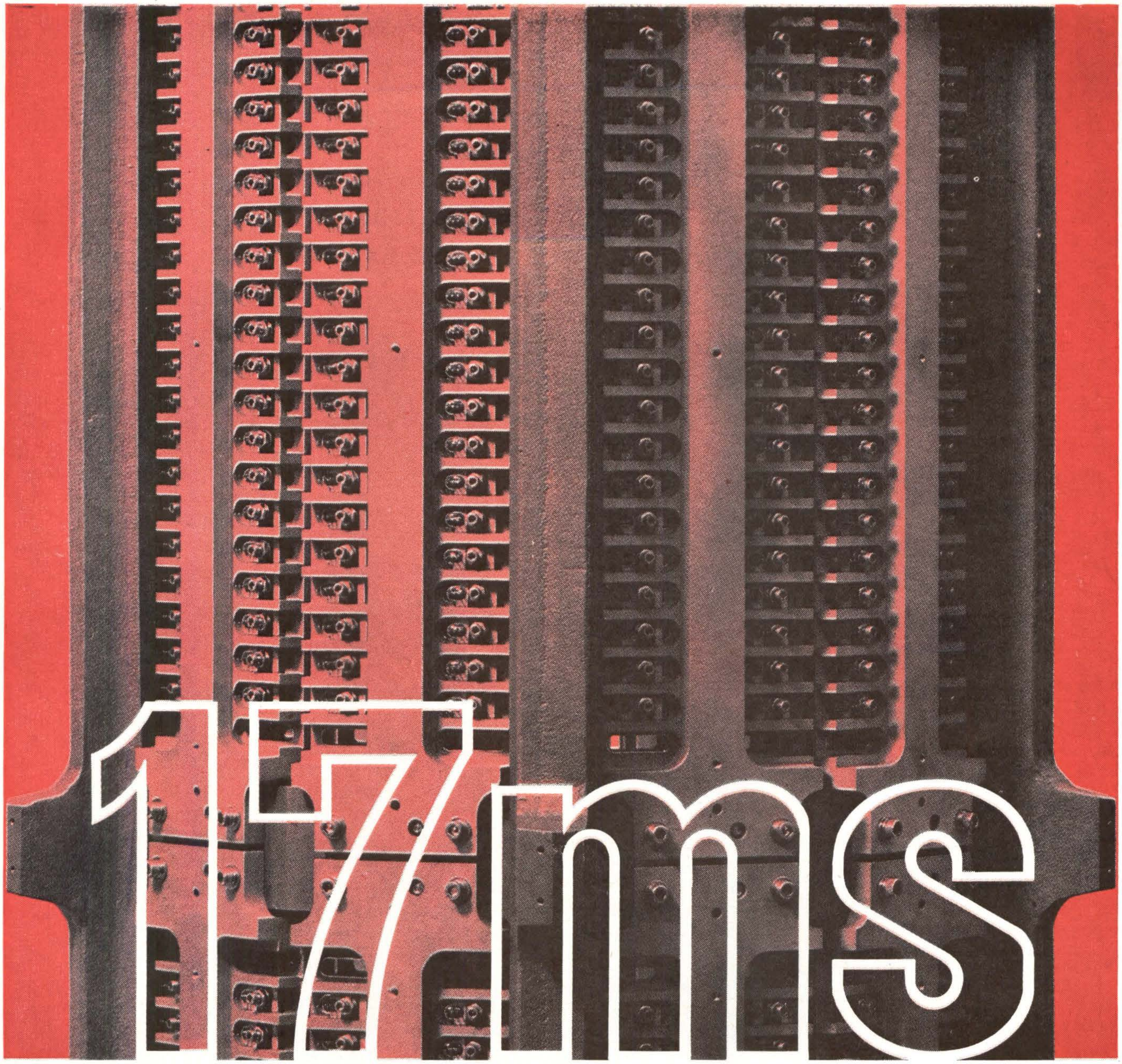
- Example 14 Continue Example 11 (step 3):

$$\begin{array}{r} 1 \\ 909\overline{)1234321} \\ \underline{909} \\ 1234 \end{array}$$

- Example 15 Continue Example 12 (step 3):

$$\begin{array}{r} 9 \\ 1909\overline{)12321} \\ \underline{1221} \\ 11 \end{array}$$

- **Step 4: Test remainder and adjust quotient and remainder if necessary.** The differences between normal division and negative radix division so far have been rather superficial. When we come to test the remainder, we come to the truly significant differences. Rather than forge ahead using normal division as a guide, we must take a long hard look at what happens in negative radix division. This topic requires a large part of an entire article and so it will be taken up in next month's issue. In the meantime, the intrepid reader can try negadecimal division for himself and prepare a flow chart corresponding to Fig. 2, remembering that it is naturally non-restoring.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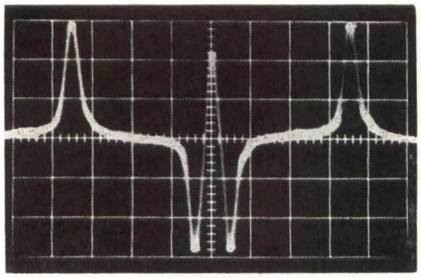
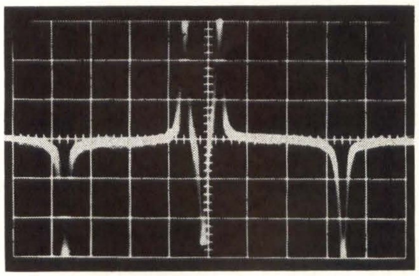


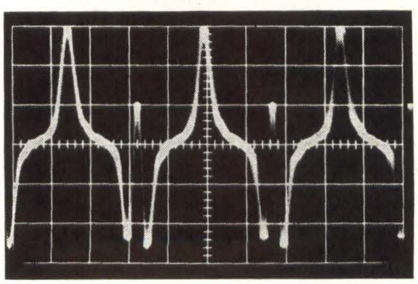
WAVEFORM NO. 1

Waveform photograph taken from a standard 800 bpi compatible computer system using 500/250 microinch write/read heads. This sequence of three ones imposes a crowded condition on the center pulse so that its peak height is depressed to about 70 per cent of that of the isolated pulses as indicated. This pattern is from standard iron oxide computer tape.



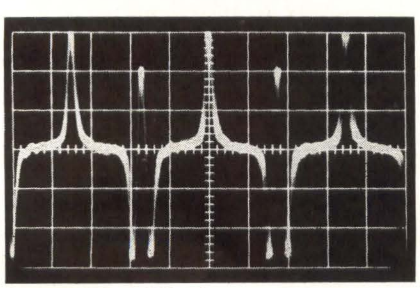
WAVEFORM NO. 2

For the same pattern on Crolyn magnetic tape, the crowded pulse retains 90 per cent of the peak value, as opposed to only 70 per cent for iron oxide tape as shown in Waveform No. 1.



WAVEFORM NO. 3

This sequence illustrates the result of increasing the system packing density of iron oxide tape from 800 to 1600 bpi using the same 500/250 head configuration. The height of the crowded pulse has been reduced to approximately 30 per cent of the isolated pulse level.



WAVEFORM NO. 4

In contrast to the iron oxide tape (waveform No. 3), the height of the crowded pulse from Crolyn magnetic tape at 1600 bpi has been reduced to only 70 per cent — the level for iron oxide tape at 800 bpi (waveform No. 1).

NEWLY-DEVELOPED MAGNETIC TAPE

Chromium Dioxide Magnetic Tape Offers The Same Performance At 1600 BPI As Iron Oxide Tape At 800 BPI

The Du Pont Company announced that it will manufacture and market a new, high-performance magnetic recording tape incorporating chromium dioxide as the magnetic medium. Chromium dioxides were developed as part of an extensive research program in magnetic materials and magnetism. Patents have been issued to Du Pont that cover the chromium dioxides, the processes by which they are made, and the magnetic recording products containing them.

Trademarked Crolyn, the new magnetic tapes have significant advantages over conventional iron oxide tapes in computer, instrumentation, and video recording applications, according to Dr. Maurice L. Ward, magnetic tape manager of the Du Pont Photo Products Department.

"Stated simply, chromium dioxides offer two principal advantages: higher signal output at the same degree of resolution, and better resolution at any given signal output level," Dr. Ward said. "These advantages accrue from the greater magnetic strength of chromium dioxides and from precise control of particle size and shape."

Crolyn magnetic tapes have been tested extensively at Du Pont and in cooperative programs with manufacturers of equipment in the areas of potential use. Results indicate that the new tapes will accept more information per inch and will record and reproduce high-frequency signals with greater fidelity than present gamma iron oxide tapes. In addition, reduction of tape speed for longer playing time or economy appears possible with Crolyn magnetic tapes in a number of applications.

Crolyn can be used interchangeably with iron oxide tapes in many applications, but greater performance benefits are usually obtained on recording equipment adapted for use with the new tapes. Du Pont reports that several manufacturers — particularly in the computer and the industrial and home video areas — have been actively working either to modify existing equipment or to develop new equipment to take advantage of the superior properties of Crolyn.

According to Du Pont, the superior magnetic characteristics of chromium dioxide allow Crolyn magnetic tape, with half the coating thickness of current commercial computer tapes, to provide the same peak-to-peak signal amplitude when recorded on conventional computer transports. Such a compatible Crolyn magnetic tape exhibits less pulse crowding and less peak shift even at the currently-used information packing densities of 800 bits per inch NRZI. As a result of the greater resolution capability of the new magnetic tape, it has been demonstrated to be technically-feasible to extend the tape packing density beyond 800 bits per inch on existing transports. Crolyn magnetic tape is also said to offer substantial performance advantages over commercial iron oxide computer tapes in high-density digital recording systems employing phase encoding.

Only limited quantities of the tapes are available at present, but Dr. Ward pointed out that the manufacturing facility at Newport, Del., has the potential capacity to meet marketing needs for the near future. For more information on the new tape:

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SOLID-STATE LAMPS

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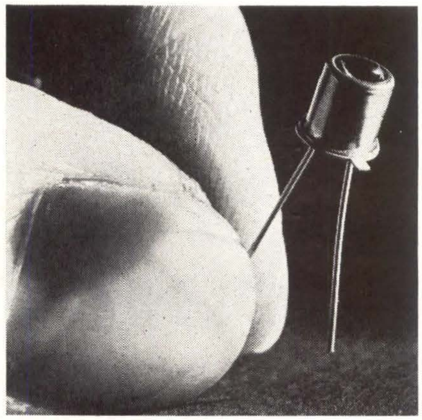


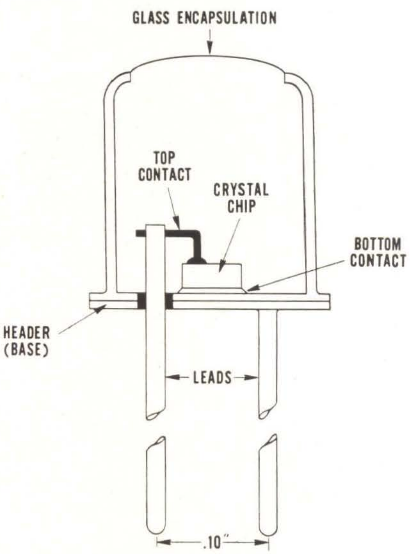
New solid-state lamp can operate at full brightness for years, theoretically.

The General Electric Co. announced recently that it has begun production of tiny solid-state lamps (light-emitting diodes) with the ability to operate indefinitely as indicator and action-triggering lamps in spaceships, aircraft, and computers. A spokesman for the company's Miniature Lamp Department said, "Laboratory samples of our first solid-state lamp, the SSL-1, have operated continuously for more than 10,000 hours — a little more than a year — and so far show no sign of deteriorating. Theoretically, they might operate at full brightness for years, perhaps a lifetime, in applications such as earth-orbiting weather stations."

Heart of the SSL-1 is a pinhead-size crystal "grown" at high temperature in industrial ovens from powdered silicon carbide. Resulting crystals have a hardness that rivals diamonds. When lighted at low voltage, they glow brightly with a whitish yellow light. GE engineers described the SSL-1 as a "high visibility" lamp with more useable light than any other solid-state lamp. Its peak light wavelength (about 5,900 Angstroms) is very close to that to which the human eye is most responsive. Visibility is also enhanced by the fact that the entire top surface of the lamp, an area one millimeter square, is used as the light source. The edges of the SSL-1 give off even brighter light, and this narrow, but more concentrated brightness, may make them useful as "readout" lamps, seven-part lamps which can form any letter or number.

The SSL-1 is "just a beginning in a series of possible types of solid-state lamps or light-emitting diodes which will be offered by the General Electric Company," according to Gomer F. Davis, Marketing Manager of the company's Miniature Lamp Department. "Subsequent models will be built around different packaging concepts for the crystal chips; some will look like subminiature lamps, but others will look even less like conventional lamps than the SSL-1. For use in card reader computers, for instance, the chip might be mounted vertically in order to use the edge light to best advantage. This would be true, too, of readout lamps," the GE spokesman said.

Unlike any other lamp, the crystal chips operate effectively in any environment, even when they are unenclosed. This feature, and their shock and vibration resistance, make them ideal for aerospace applications. The new GE SSL-1 lamp is mounted on a standard transistor base and capped by a "tophat" capsule and a lens. Individual sample lamps that will fit any standard transistor socket are available at \$9.50, while lamps in production quantities will be priced at about \$6.60.



Semiconductor crystal lamp is mounted on a standard transistor header and capped by a tophat and lens. The lamp operates at from 2 to 5 volts and draws 50 to 75 milliamps.

Each sample lamp is tested photometrically, and its own unique and slightly different electrical "personality" rating is given to the purchaser to facilitate design work of equipment using the lamp. Information includes the light output, intensity and color, and electrical characteristics. The latter are particularly important, according to GE engineers, since most SSL-1's will be used with solid-state circuits.

Production of the lamp begins when silicon carbide granules are heated in a high temperature furnace. Temperatures up to 2600°C cause the granules to vaporize then crystalize into a form somewhat like rock candy. The resulting crystals are ground smooth on both sides and coated with a semiconductor layer. The crystals are then diced into tiny chips, each about the size of a pinhead. Finally, gold lead wires are attached top and bottom to each chip and a lamp is born. For more information:

Circle No. 105 on Inquiry Card

NASA TECH BRIEF

A SUMMARY OF A SPECIFIC TECHNICAL INNOVATION DERIVED FROM THE SPACE PROGRAM. ISSUED BY THE TECHNOLOGY UTILIZATION DIVISION OF NASA.

Point-Source Detection System Rejects Spatially Extended Radiation Sources

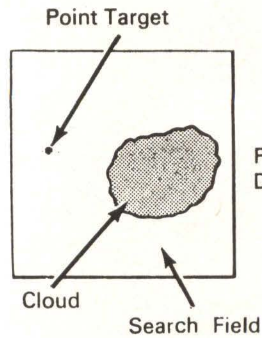


FIGURE 1

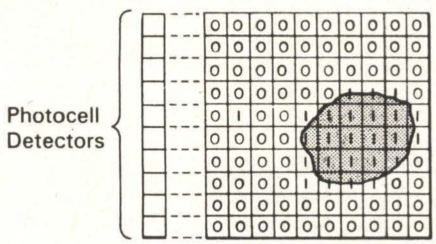


FIGURE 2

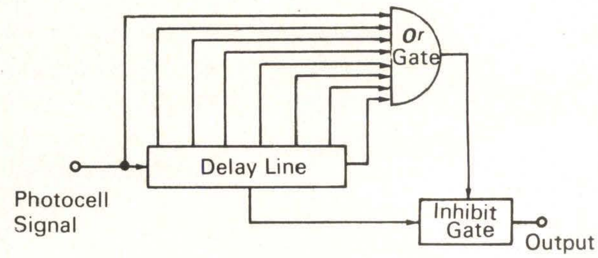


FIGURE 3

THE PROBLEM:

To devise a reliable method for discriminating a distant (point source) target from false (spatially extended) targets in the field of view of an infrared detection system or tracking device. Various spatial discrimination methods (spacial filtration, pulse-length discrimination, area cancellation, and analog space correlation) that have been used to distinguish characteristic differences between the signals from a point target and those from large-area targets require generally complex circuitry and are not entirely suitable for tracking a reentering space vehicle.

THE SOLUTION:

A system employing digital space correlation to suppress false target signals in a point-target tracking device.

HOW IT'S DONE:

The search field (Figure 1), containing the point target to be tracked and a cloud representing an extended-area false target, is divided into a matrix of rows and columns of elemental fields of view. As shown in Figure 2, digital values are assigned to the matrix elements. That is, the elements containing no target radiation are designated by zeroes, and the elements in which target radiation appears are designated by ones. In accordance with the method described below, adjacent elements (such as those corresponding to the cloud) having targets are eliminated. Only the individual element corresponding to the point target is accepted.

Photocells mounted in a column are moved across the field matrix to scan the elements sequentially. When target radiation of sufficient intensity (above a threshold value) impinges on a photocell that is sampling a particular matrix element, the photocell will emit a signal pulse. If no radiation, or only a very low amount of radiation impinges on the photocell, the cell's output will be rejected. The pulses are fed to an **or** gate and to a delay line having seven outputs that are also applied to the **or** gate (Figure 3). The output from the **or** gate is applied to the inhibit input of an inhibit gate, and an eighth signal output from the delay line is coupled to the signal input of the inhibit gate. When there is a signal correspondence between one input to the **or** gate and the signal output from the delay line to the inhibit gate, no signal will pass through the inhibit gate. This correspondence occurs only for signals from photocells that sample an array of adjacent matrix elements intercepting an extended area target.

NOTE:

Inquiries concerning this system and modifications that will resolve certain ambiguous cases may be directed to: Technology Utilization Officer, Goddard Space Flight Center, Greenbelt, Maryland 20771. Reference: B66-10622

PATENT STATUS:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546. **END**

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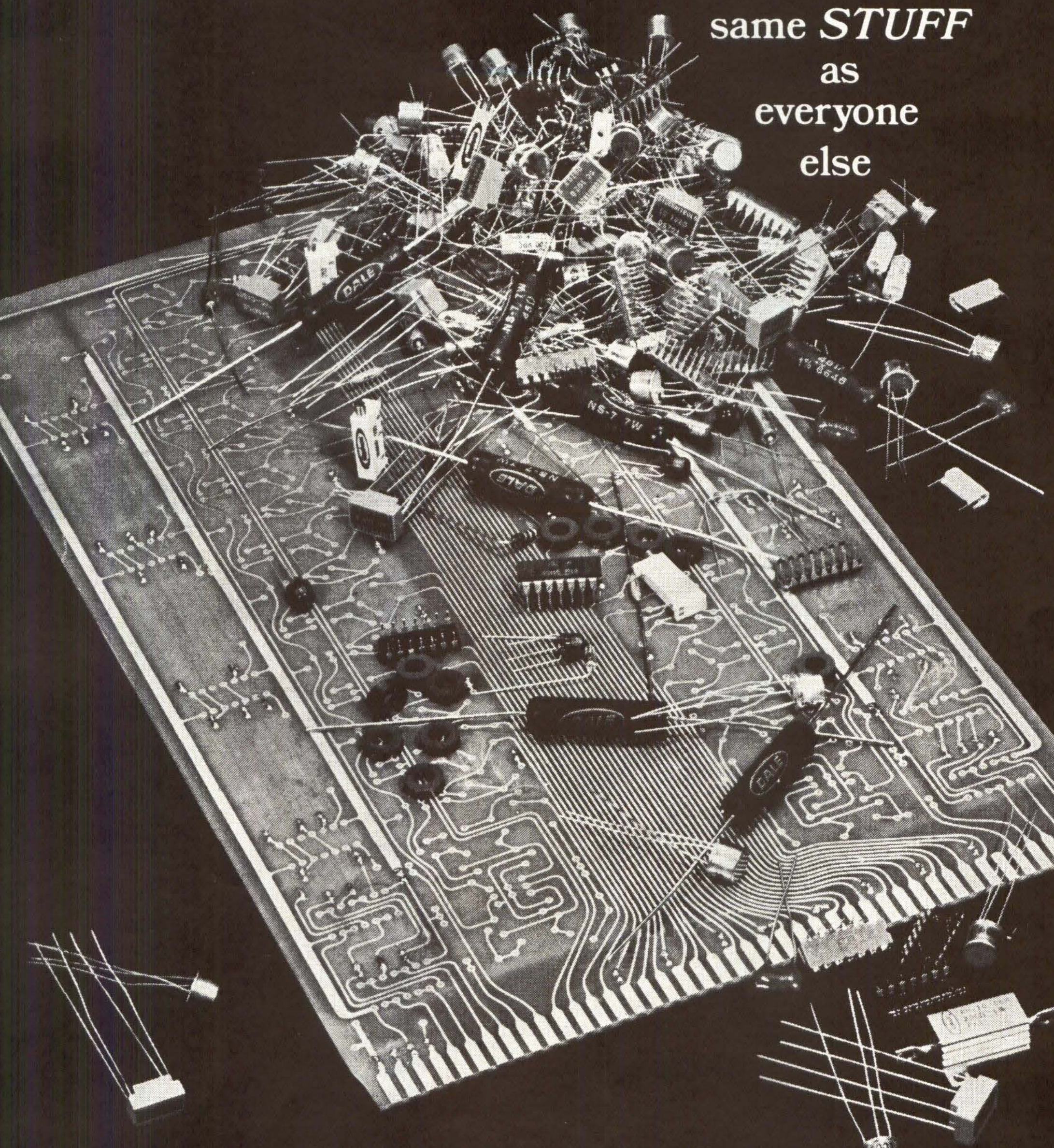

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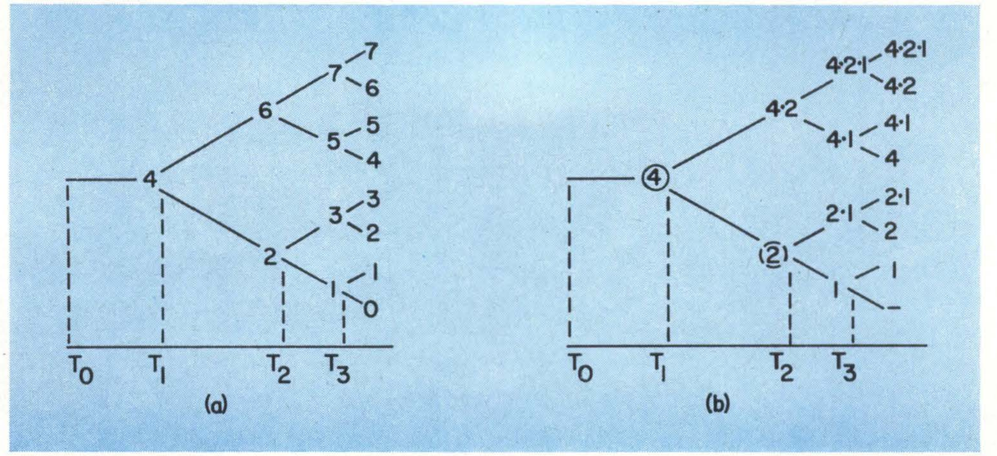

Fig. 1 Binary tree: (a) showing absolute values; (b) showing flip-flop weights.

DESIGNING WITH BINARY DECISION TREES

This article illustrates the use of the binary decision tree, a technique which may be more useful in some sequential design problems than the more common methods such as the Karnaugh map.

MONTY WALKER

Design Engineer, Dynamics Instrumentation Company, Monterey Park, Cal.

A binary decision tree is a graph of a network of lines and nodes that have the characteristics that (1) each line is directed with respect to time, and (2) each node will have one input line and a maximum of two output lines. (It is possible to generalize further, but for the purposes of this article we will restrict our dicussion to these definitions. For those interested in digging deeper, see Ref. 1.) A symmetrical tree (pure binary) is the simplest to design. To illustrate this type of tree, let us suppose that an unknown voltage (E_x) is to be measured as in an A-D converter. The usual method is to compare E_x with a precision reference voltage (E_{Ref} that is divided down in successive time periods. E_{Ref} will be equal to the maximum allowable input. At the first time period (T_0), E_x is compared to $\frac{1}{2}E_{Ref}$. If E_x is greater than $\frac{1}{2}E_{Ref}$, an accept pulse is generated and at the second time period (T_1) a comparison is made with $(\frac{1}{2} + \frac{1}{4})E_{Ref} = \frac{3}{4}E_{Ref}$. If at T_0, E_x is less than $\frac{1}{2}E_{Ref}$, a reject pulse is generated and at T_1, a comparison is made with $(0 + \frac{1}{4})E_{Ref} = \frac{1}{4}E_{Ref}$. The same idea is continued for each succeeding time period. The geometry of the tree is shown in Fig. 1 (wherein an upward line indicates an accept and a downward line indicates a reject).

To mechanize this tree, we will first show the flip-flop weights at each node, see Fig. 1(b). We observe that weight 4 is unconditionally set after time T_0 and it is never set again, and may thus write: Set $4 = T_0$. Weight 4, if it is to be cleared, will be cleared after T_1 and then only if a reject pulse is generated. We may write: Clear $4 = T_1 \cdot \text{Rej}$. In a similar manner: Set $2 = T_1$

Clear $2 = T_2 \cdot \text{Rej}$
Set $1 = T_2$
Clear $1 = T_3 \cdot \text{Rej}$

Of course, the same equations can be obtained by using a Karnaugh map, but it is necessary to consider eight variables (i.e., Acc/Rej, T_0, T_1, T_2, T_3 ,4, 2, 1). To illustrate the full 8-variable map method, Fig. 2 shows the derivation of Clear 2. Note that we have entered X (don't care) in the squares that have two time periods occurring together, since these are impossible conditions. The Clear 2 entries together with the don't care conditions (X) affects $T_2 \cdot 2 \cdot \text{Rej}$. Since the Set 2 equation does not contain a T_2 input we can simplify to: Clear $2 = T_2 \cdot \text{Rej}$, which is identical to the visual equa-

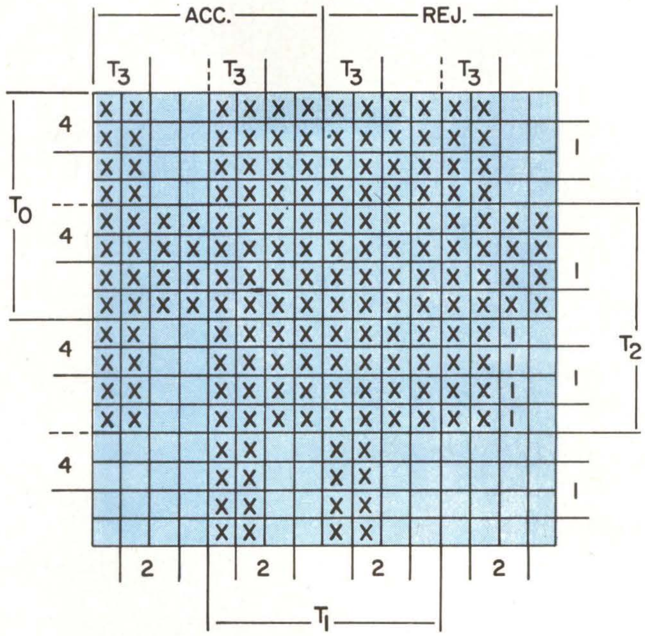

Fig. 2 8-variable Karnaugh map derivation of Clear 2.

tion. In most cases, it is far more convenient to use the visual method for deriving the flip-flop equations.

Fig. 3 shows the flip-flop mechanization of the tree. Since T_0 is our start period, we must clear flip-flops 2 and 1 at the same time that flip-flop 4 is set. The flip-flop implementation of the pure binary tree follows a pleasing symmetry. The general scheme can be extended to any number of elements with each flip-flop having a weight equal to half the preceding one. Note that the accept pulse is not needed in this particular circuit.

It should be pointed out, at this time, that although the binary tree has been developed from the standpoint of weighted elements and flip-flops as in an A-D converter, this is by no means the only interpretation possible. It could represent, for example, a serial encoder or a block translator.

Binary Codes

A particular set of binary digits that is used to represent a symbolic quantity is said to be a binary code. For example, a set can be chosen to rep-

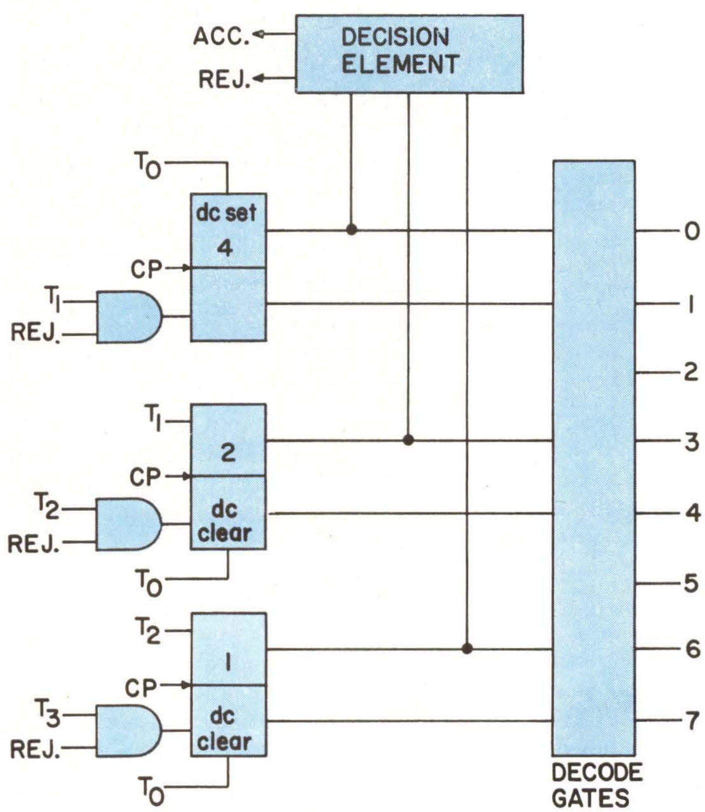

Fig. 3 Implementation of the binary tree.

4	2*	2	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	1	0	4
1	0	0	1	5
1	0	1	0	6
1	0	1	1	7
1	1	1	0	8
1	1	1	1	9

(a)

4	2*	2	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
1	0	0	0	4
1	0	0	1	5
1	0	1	0	6
1	0	1	1	7
1	1	1	0	8
1	1	1	1	9

(b)

Fig. 4 Two examples of 4-2-2-1 BCD codes.

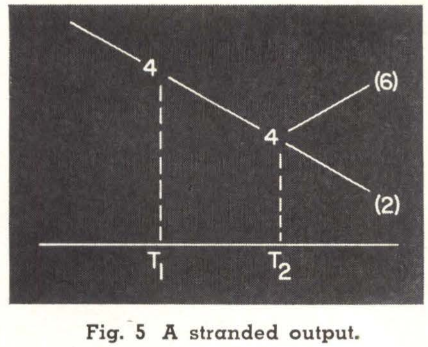

Fig. 5 A stranded output.

resent the letters of the English alphabet or the positive decimal integers (0-9). In the latter case, the code is called BCD. In many codes, less than the full set is actually used. For example with 4 bits, 16 unique binary numbers can be generated but in the case of a BCD code only 10 will actually be used. Since most digital instruments (and many computing machines) use some form of BCD code (and to keep the range of our discussion reasonable), we will consider only BCD weighted codes. A weighted code has the characteristic that each decimal integer is formed by combining one or more weights.

Although there exist 17 possible 4-bit, positive weighted BCD codes, in practice, only the 8421 and 4221 codes are used to a great extent. The 8421 code is unique; that is, there is only one way to obtain each decimal digit by combining these weights. The 4221 code, on the contrary, has 32 different possible ways (sub-codes) of obtaining the digits, e.g., decimal 5 can be obtained by combining 4 and 1 or by combining 2 and 2 and 1. When a BCD code is used, the tree will be asymmetrical, and certain complications set in. We may divide the design process into four parts:

- Choosing the code to be used
- Choosing the sub-code to be used
- Designing the tree geometry
- Implementing the final tree.

To illustrate the design process let us suppose that we are to quantize an unknown voltage (E_x) in a decimal (0-9) representation, using a 5-step process. Let us further suppose that the 4221 code has been decided upon.

We might, as a beginning, choose the sub-code as shown in Fig. 4(a), which is a self-complementing code sometimes used in computers. (2* is used to differentiate one 2 from the other.)

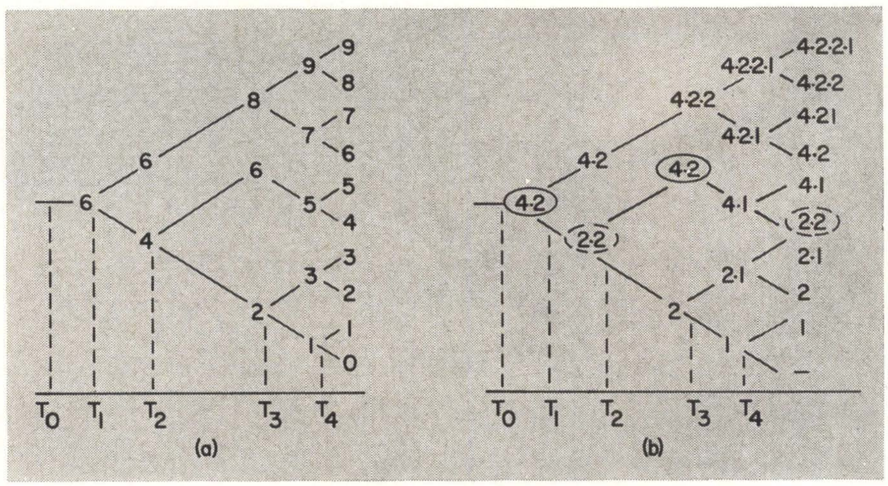

Fig. 6 Tree using 4-2-2-1 code.

In designing the tree geometry, it must be kept in mind that it must be possible to reach every output, and that only one path should lead to each output. For example, in Fig. 5, it will not be possible to reach output (6) because if 4 is rejected at T_1 it will also be rejected at T_2 and the output must be (2). A practical consideration is to keep the changes of each flip-flop (as far as is possible) to a minimum. Fig. 6(a) shows a first attempt at a tree; 6(b) shows the same tree with the weighted flip-flop values shown at the nodes.

To obtain the Boolean equations for flip-flop 4, we start by circling the nodes where 4 changes state. The solid circles in Fig. 6(b) show 4 being set and the dotted circles show it being cleared. The 4 is unconditionally set at time T_o (Set $4 = T_o$). In addition, 4 is set after time T_2. We note that 4 is already set in the top branch but in the bottom branch it is in the clear condition. The common factor of the upper two branches is the accept pulse so we may write: Set $4 = T_o + T_2 \cdot \text{Acc}$. The Clear 4 condition also occurs at two positions. The first, we can easily write as Clear $4 = T_1 \cdot \text{Rej}$. The second condition requires a bit more thought: we note that the nodes at T_4 which lead to 6 and 8 each contain 2*, but the node leading to decimal 4 does not, and may thus write: Clear $4 = T_1 \cdot \text{Rej} + T_4 \cdot \overline{2^*} \cdot \text{Rej}$. A careful check of all nodes reveals that T_4 in $T_4 \cdot \overline{2^*} \cdot \text{Rej}$ is redundant and it may be dropped. By the same methods, the equations for flip-flops 2*, 2, and 1 may be derived:

Set 4	$= T_o + T_2 \cdot \text{Acc}$
Clear 4	$= T_1 \cdot \text{Rej} + \overline{2^*} \cdot \text{Rej}$
Set 2*	$= T_o + 4 \cdot \text{Rej}$
Clear 2*	$= \overline{4} \cdot \text{Rej} + T_2 \cdot 4$
Set 2	$= T_1 \cdot \text{Rej} + T_2 \cdot 4$
Clear 2	$= T_3 \cdot \text{Rej}$
Set 1	$= T_3$
Clear 1	$= T_4 \cdot \text{Rej}$

Since time T_o is our start period we must clear flip-flops 2 and 1 at the

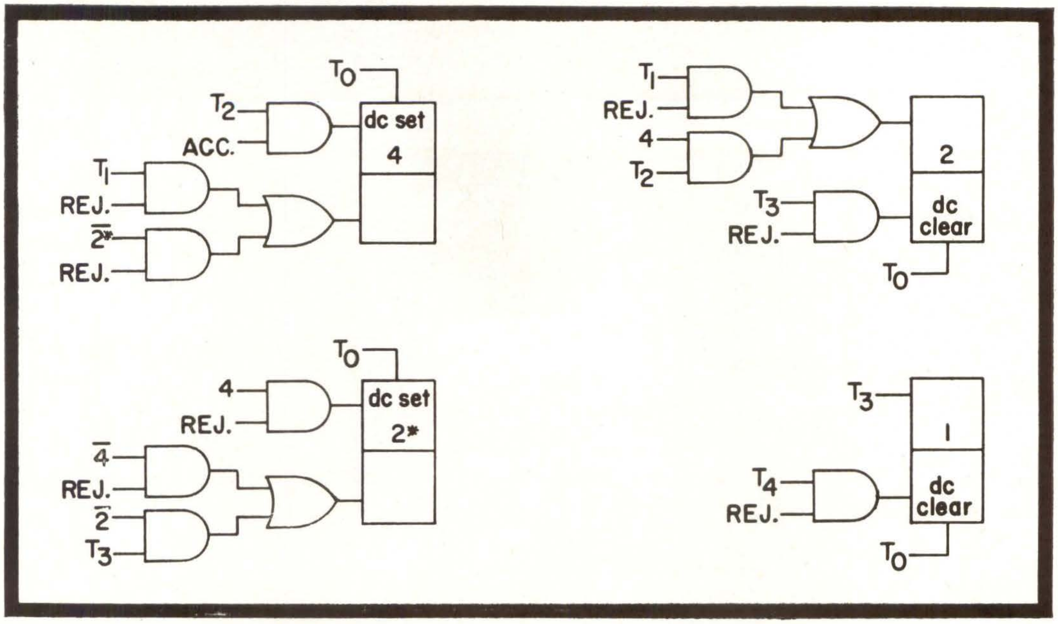

Fig. 7 Implementation of the 4-2-2-1 BCD tree.

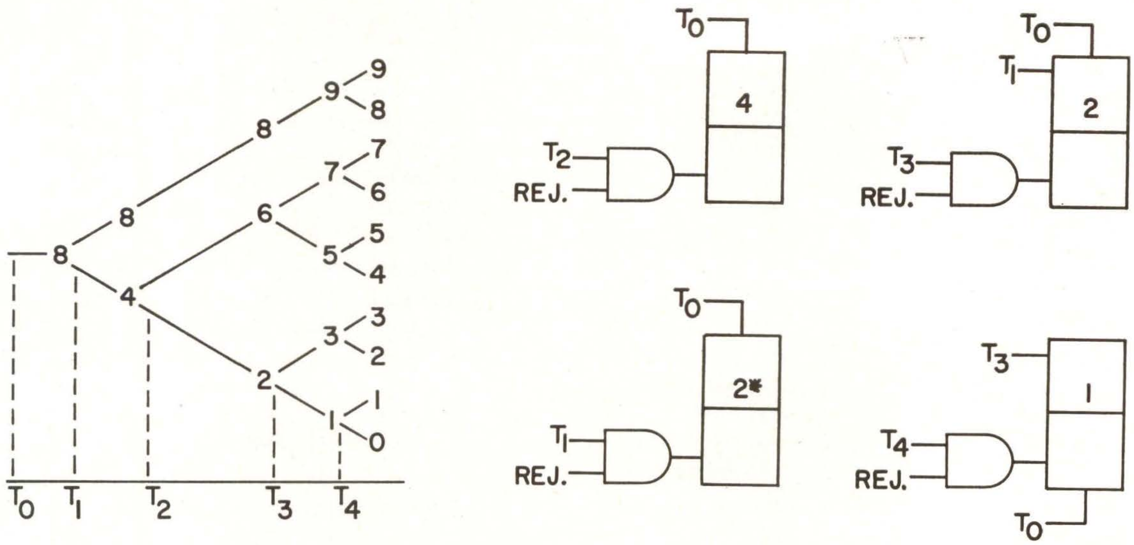

Fig. 8 Unbalanced tree using 4-2-2-1 code.

same time flip-flops 4 and 2* are set. Fig. 7 shows the flip-flop mechanization of these equations; since we have used 13 two-input gates to implement the tree of Fig. 6, it need hardly be said that this is no logic masterpiece.

If we examine the sub-code that we have chosen, it becomes apparent that from several criteria we could have done better. For example, in the transition between decimal 4 and 5 we invert all binary weights. This is not a natural transition for binary numbers. Our problem seems to be that weight 4 is sometimes, but not always, formed by combining 2 and 2. Fig. 4(b) shows a sub-code that removes this difficulty. By using this sub-code, and the tree of Fig. 6(a), we can reduce our circuit gate requirement from 13 to 7, a savings of almost fifty percent; however, even this can be improved upon.

Our procedure to this point has been to choose a tree geometry that is possible to realize and to vary the sub-code to effect simplification. By now, varying the tree geometry but holding the sub-code constant, we can usually simplify the final realization. Figs. 8 and 9 show two alternate tree geometries for the code of Fig. 4(b), and their flip-flop implementations. In Fig. 8, five gates are used to mechanize the tree, and in Fig. 9, four gates are used; the same number that is used in a straight binary tree. This is probably the minimum for a 4221 code. If minimum parts were the only criterion, this tree would surely be preferred; however, in several respects it is definitely inferior. (A simple algorithm for designing a tree that is to be mechanized using minimum hardware is to draw the complete symmetrical tree then eliminate the branches that are unwanted. The resulting tree will be highly unbalanced but easy to mechanize.)

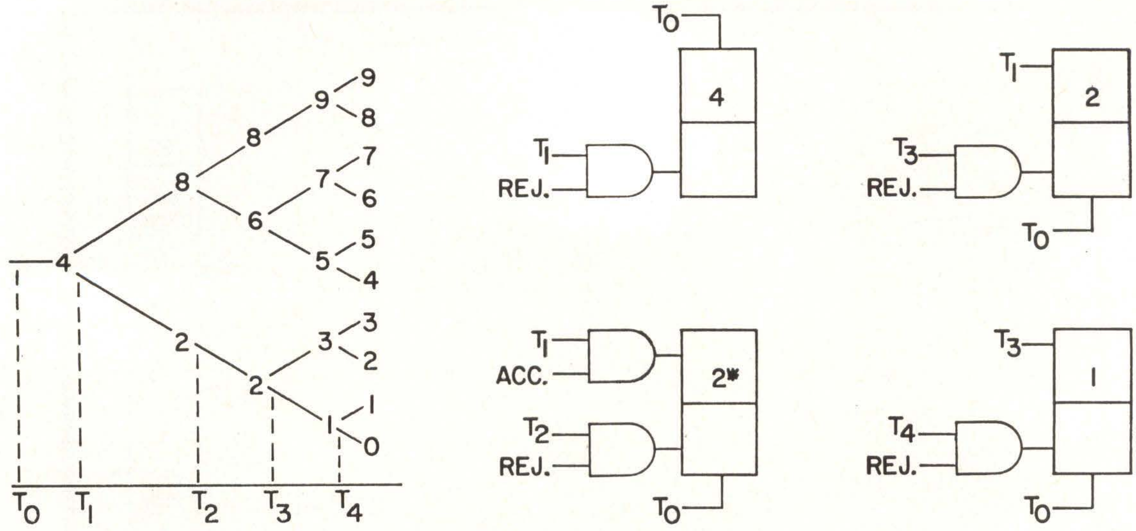

Fig. 9 Balanced tree using 4-2-2-1 code.

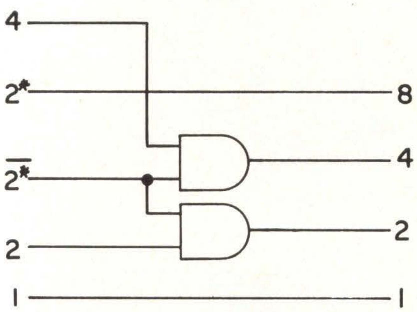

Fig. 10 A 4-2-2-1 to 8-4-2-1 code translator.

In all of the examples used thus far, there have been the implicit assumptions that the actual mechanized instrument would be operating under ideal noise-free conditions, that the input signal would not change during the tree logic time, that all propagations and voltage swings would occur in zero time, etc. Of course in the real world none of these conditions exist and it is well to consider the probable performance of the instrument under less than ideal conditions. Let us suppose, for instance, that because of noise or other effects, an erroneous decision is made at some node. The final output will be erroneous, but if our tree is chosen properly, the maximum error will be minimized.

Consider now the tree shown in Fig. 8: suppose an E_x with an actual quantization of decimal zero is erroneously accepted at time T_1. The final output reading will be decimal 4, an error of 4. If the same conditions were to occur in the tree shown in Fig. 9, the final reading would be decimal 8, an error of 8. Also, because the reference voltage must rise to 8 instead of 4 at T_0, the maximum "wait" time will be greater and our maximum measuring speed will be reduced from that possible with the tree of Fig. 8. For these and other reasons we can state that for system performance the Fig. 8 tree is to be preferred over that in Fig. 9.

Many times when a particular code or sub-code is specified for the output of a particular instrument, the designer will, as a matter of course, use this code internally, when in many cases the actual total hardware can be reduced and the system performance improved by using a simpler code internally and encoding the output. The actual encoding circuitry is usually not excessive: for example, Fig. 10 shows the circuit to translate the sub-code of Fig. 4(b) to 8421 BCD code.

Conclusion

There are usually many options open to the designer both in choosing the sub-code to be used and in the actual geometry of the decision tree. A help in reducing the total number of options is to choose a sub-code with the transitions of each bit at a minimum, and those transitions occurring at the natural binary transition points. This tree, if speed and noise are not a problem, should be partially symmetrical (a portion of the natural binary tree). If system performance is of more than passing interest then the tree should divide the output digits into equal parts as nearly as is possible at each node. For instance, in a BCD tree, the first node should be either 4 or 6. (If 5 is chosen the succeeding divisions are more difficult.)

Not all decision trees are as simple as the ones illustrated and, of course, BCD codes are by no means the only type of geometry the designer is apt to encounter. However, by keeping in mind the possibility of internal options both in the code and the tree geometry (even if it means encoding the output), the likelihood of a simpler and better performing instrument is greatly enhanced. ■

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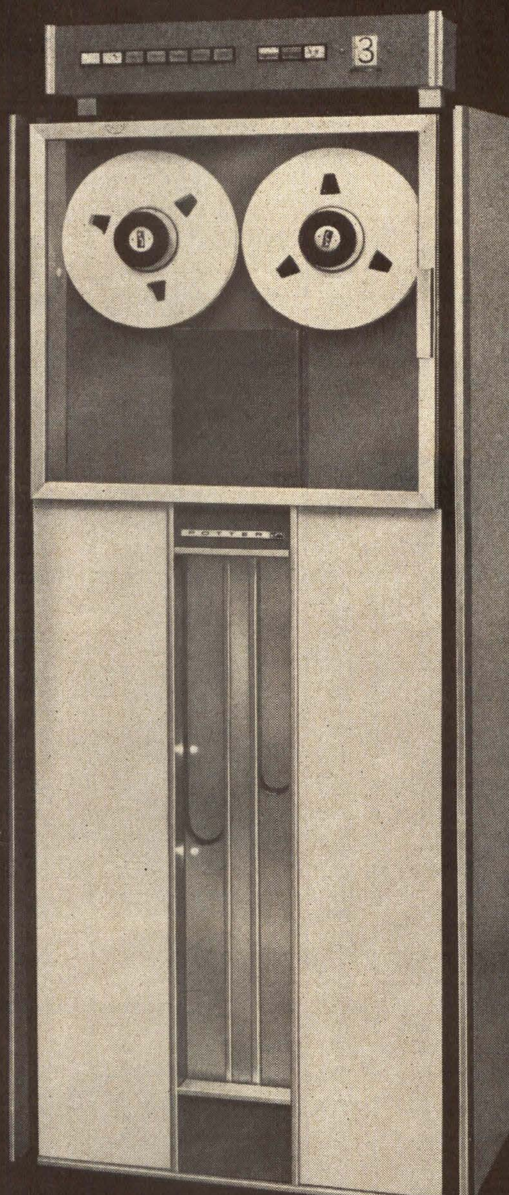

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2. Automatic tape loading
3. Oxide contact with only the head

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3. The tape path is designed so that only the head touches the oxide surface. During rewind the head is retracted and *nothing* touches oxide. The SC-1080 operates up to 150 ips in all industry compatible formats including 1600 bpi, phase modulated recording. Rewind speed is 290 ips average, less than 100 seconds for a 2400 foot reel.

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CIRCLE NO. 30 ON INQUIRY CARD

NEW PRODUCTS

CHART DIGITIZER

A digitizer is a new device for reducing analog graphical data from large maps and charts to digital magnetic tape for computer processing and analysis. The Model 480 features variable interval programmed digitizing, a solution to the limitation on graphical data reduction speed imposed by the relatively low speed of available output devices. As the operator manually traces the graphical data with a stylus, the movements of the stylus are converted to digital signals for recording on the output (computer-compatible, 7-channel, 556 bpi) magnetic tape recorder. The system monitors the output recorder and outputs a data point as often as the recorder can accept and record data. Because data is recorded at a fixed maximum rate (500 characters per second, on the Model 480), and the tracing stylus is moved at varying speeds, the size of the intervals along the traced curve at which data points are recorded varies with stylus velocity. Actually, the digitizing system generates and processes a data point for every 0.005 inch of stylus movement along the X or Y axes. But, when these points are being generated too quickly for the output recorder to accept them, the points are counted and stored in an electronic register. The contents of the register are taken out as soon as the recorder is free to accept them. The sampling interval, therefore, varies (from 0.005 to 0.075 inch) proportionately with stylus velocity. The speed of tracing varies, however, with the complexity of the data being digitized. The digitizing system allows an overall maximum digitizing speed of 937 inches per minute with a resolution of 0.005 inch. Calma Co., Santa Clara, Cal.

Circle No. 259 on Inquiry Card

GENERAL-PURPOSE RELAYS

General-purpose, comb-actuated relays with plug-in, solder, or printed circuit terminals include low-level models with bifurcated contacts, and high-voltage and high-frequency versions. The relays were designed for use in transistorized systems where space requirements and operational longevity are of prime importance. All relays occupy less than one cubic inch of space. Other features include a life expectancy of up to 100 million operations, and a balanced spring-held armature that allows for the same operating data in any mounting position. American Zettler, Inc., Costa Mesa, Cal.

Circle No. 221 on Inquiry Card

MAGNETIC RECORD HEADS

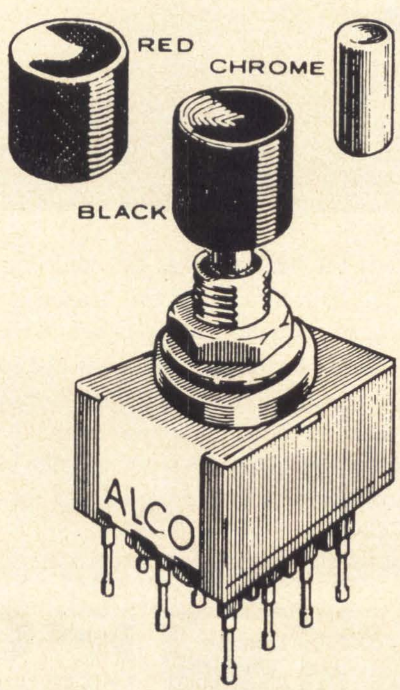
Complete line of combination erase-record/play heads includes 2-track mono and stereo, 4-track mono and stereo, and 8-track stereo versions. Double hyperbolic face design permits use of heads with or without pressure pads. Design features include sintered brass body construction, ultra-thin laminations (0.0039 inch in thickness), vacuum-deposited glass gaps, and high temperature stability. Magnetic Heads, Inc., Minneapolis, Minn.

Circle No. 250 on Inquiry Card

DECODER DRIVER

A BCD-decimal decoder driver contains 21 semiconductors and a thin film passive network interconnected as a hybrid assembly in a molded package. The unit decodes 4-line data in BCD format and provides 10-line decimal outputs suitable for driving medium size incandescent lamps and other universal readout devices. Noise immunity is in excess of 3.5 volts. Intellux, Inc., Goleta, Cal.

Circle No. 238 on Inquiry Card



MINIATURE PUSHBUTTON SWITCH

A new miniature 4 PDT pushbutton switch is said to be smaller than conventional, multiple-stacked pushbutton switches. This new switch features a 1-piece body construction, has an unusually high current rating, and is capable of handling multiple circuits simultaneously. The miniature switch is said to also feature high voltage barriers between terminals and contacts, low loss and high impact case material, and new turret type terminals to simplify wiring. Rated 6 amps at 115 vac, the unit is available in two 4PDT types, either as a momentary pushbutton or push-to-make and push-to-break. Alco Electronic Products, Lawrence, Mass.

Circle No. 242 on Inquiry Card

CAPACITOR INSERTS

New, smaller capacitor inserts for use in micro-miniature and integrated circuits can be supplied in sizes from 0.020 in. square and up to 180 pf, to the specific requirements of customers. Available electrodes include palladium-gold, platinum-gold, gold, and silver. The diced capacitors are produced from thin sections of high-K and temperature-compensating ceramic materials. Dielectric constants range from 6 to 9000. Accuracy of the control of capacitance varies with design, the company states, but tolerances are generally available from ±20 percent to GMV. Titania Div., American Lava Corp., Chattanooga, Tenn.

Circle No. 218 on Inquiry Card

PUNCHED TAPE READER

A new ruggedized "transit case" photo-electric punched tape reader uses plug-in electronic modules and stepping motor tape drive. Reading speed is 200 char/sec. There are no ratchets or pinch rollers. A flanged, deep drawn, front panel is used to facilitate mounting the reader in a small transit case. The operating temperature range is −40°C to 85°C. The unit meets MIL-E-16400 shock and vibration requirements. Dimensions are 10″ x 16″ x 8½″; weight is 17½ pounds. Electronic Engineering of California, Santa Ana, Cal.

Circle No. 222 on Inquiry Card

COMPARATOR MODULE

Designed specifically for applications requiring fast response and high sensitivity, a new comparator module features a resolution-speed-product of 2 mv/2 usecs, typical. It also offers fast over-load recovery guaranteed over a full 10v input range. Input impedance is 100K ohms minimum differential; 10 megohm minimum common mode. Accuracy is obtained by 100db of open-loop gain at dc. Package size is only 1.4 cubic inches. Redcor Corp., Canoga Park, Cal.

Circle No. 209 on Inquiry Card

NEW PRODUCTS

LOGIC RELAY

An ultra-sensitive logic relay with a rated life of 10 million operations consists of an integrated solid-state amplifier and a reed switch output. Size is only 1⅜" x ⅝" x ¾". Weight is 0.3 ounce. Standard units are for operation on 6, 12, or 24 volts dc consuming less than 200 milliwatts. They do not require standby current. Nominal signal pull-in voltage is 0.7 dc at 50 microamperes. Output configurations includes SPST, DPST, and SPDT. The output is electrically isolated from either the power or signal source. Contact power ratings are 15 watts ac or dc up to 135 volts. The response time is better than 1 millisecond, making the relay particularly useful as a logic relay, time delay relay (either slow acting or slow release), temperature controller, meter relay, etc. It may also be used as an ac detector from Hz to MHz with a suitable signal rectifier and bypass capacitor. Sensitak Instrument Corp., Manchester, N.H.

Circle No. 265 on Inquiry Card

BALL SENSING TAPE READER

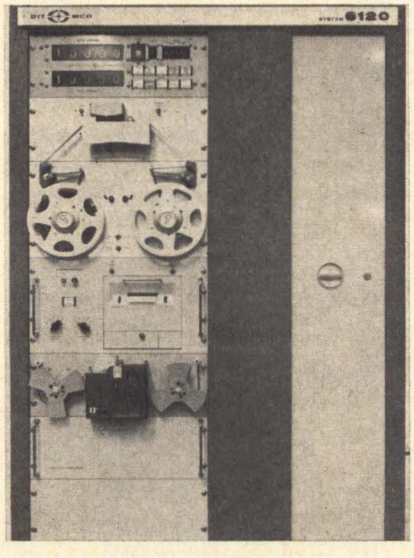
A punched tape reader utilizes a unique "reading" method, "ball sensing," and accommodates 5, 6, 7 or 8 channel tapes (paper, Mylar and aluminized Mylar) at speeds up to 60 characters per second. The tape transport mechanism is positive-indexing, solenoid-actuated, and operates asynchronously from 12, 26, or 48 volt dc sources. The reader is available as a separate component, mounted on a 19" panel, or with a panel-mounted tape handler. Invac Corp., Waltham, Mass.

Circle No. 206 on Inquiry Card

HIGH RELIABLE CAPACITORS

Featured in a complete line are sintered mica capacitors that offer 0.1% life stability, lower series resistance, and tolerances to ±½%. They are available in a capacitance range from 4 pf to 2 uf. Results of 15 year life tests indicate no catastrophic failures and a failure rate of only 0.0004% per 1000 hours (with a ½% capacitance change considered to be a failure). Transitron Electronic Corp., Wakefield, Mass.

Circle No. 234 on Inquiry Card



NEW WIRING ANALYZER

A new wiring system analyzer was developed especially for makers and users of electronic computers. Designated the System 6120, the tester operates from a fully automatic taped program input and printout concept and is capable of performing insulation and continuity tests at the rate of 2400 per minute and 2800 per minute, respectively. It is capable of verifying correct wiring in a wide variety of interconnect systems such as computer back-planes, cables, printed circuit assemblies, etc. The machine has a termination capacity of 50,000, expandable in increments of 500. The manufacturer states that a wide variety of optional features are available, including a special self-testing system which verifies correct wiring in the testing unit itself prior to the performance of testing functions. DIT-MCO International, Kansas City, Mo.

Circle No. 202 on Inquiry Card

MAGNETIC CORE NEEDLES

Needle and wire assemblies from 2.5 to 4 mil diameter were developed for magnetic core memories with the use of a new automatic machine designed to carefully and precisely handle extra-small wires, exactly-aligned buttweld assemblies can be produced at a relatively high rate of speed. Tests have shown that the 4 and 3 mil assemblies meet or exceed existing industry specifications. And, although unusual wire characteristics and a lack of specifications has limited work with the 2½ size to prototypes only, early work indicates a production capability nearly equal to that of the larger sizes. A sample package of twenty-five needle and wire assemblies for testing and evaluation will be sent free to any qualified organization upon request. E & M Industries, Inc.

Circle No. 226 on Inquiry Card

MOS FET SWITCHES

P-channel enhancement-type MOS FETs are single and dual devices designed for analog and digital switching applications. The potential problem of oxide breakdown, due to static-charge accumulation on the gate, is said to be eliminated by a built-in Zener diode between gate and body. Gate protection is assured because the 90-volt diode breakdown is much lower than the oxide destructive voltage. Drain leakage current is 0.2 na at room temperature and since it approximately doubles for every 10°C increase, it is important that the initial value be very low. Commutator applications usually have several drains tied together, therefore, the combined leakage current from each drain flows across the one ON device and becomes a significant source of error. Drain-source ON resistance is 150 ohms typical at a gate-source bias of −20 volts. Drain-source, gate-source, and gate-drain breakdown voltages are all 30 volts minimum. Gate threshold voltage is 6 volts maximum. Siliconix, Inc., Sunnyvale, Cal.

Circle No. 211 on Inquiry Card

NEW PRODUCTS

REGULATED POWER SUPPLIES

Three new convection-cooled, all-silicon regulated power supplies offer voltages up to 60 vdc and current ratings up to 66 amps. These are believed to be the only convection-cooled power supplies to offer such high current in a package only 7 inches high. The 0 to 60 vdc model LK 362FM. has a current rating of 0-25 amps at 40C, 0-24 at 50C, 0-22 at 60C, 0-19 at 71C. Current ratings apply over the entire voltage range. These new power supplies are remotely programmable over the voltage and current range. Adjustable, automatic electronic current limiting circuits limit the output current to the preset value upon external overloads including direct short, thereby providing protection for load as well as for power supply. Current limiting is settable to 105% of load. Lambda Electronics Corp., Melville, L. I., N. Y.

Circle No. 249 on Inquiry Card

SUBMINIATURE BUTTON SWITCH

A new subminiature pushbutton switch measures 0.360″ dia. by 0.468″ long, mounts from the rear with a knurled nut in a ¼″ hole on mounting centers as close as ⅜″ and will fit 1/16″ to 3/16″ thick panels. The pushbutton switch is conservatively rated for one million cycles of operation while carrying its full rated design current of 100 ma at 115 vac, non-inductive load. Gold finished brass turret terminals are electrically-isolated from the switch body. Plastic pushbuttons are offered in seven different colors and may be hot stamped with one character up to ⅛″ high. Operating and storage temperature range is from −40C to +65C at 95% humidity, maximum. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 251 on Inquiry Card

TIME-SERIES ANALYZER

A new time-series analyzer provides real-time analysis for oceanography, biomedicine, geophysics, aerospace, and other scientific fields. The two-channel, all-digital processor provides pushbutton selection of the basic set of algorithms for Fourier transformation, auto and cross spectra, auto and cross correlation, convolution, amplitude and time histograms, ensemble averaging, and real and complex multiplication. Analog or digital data can be processed with results available in analog or digital form, and on the built-in scope display. The unit is a self-contained analyzer which operates as a stand-alone device or as a peripheral to general-purpose computer. Called the Time-Data 100, it is a wired-program machine with unique organization resulting in high-speed operation which allows real-time processing for the on-line user, as well as economic processing of bulk data. For example, a 2000-point Fourier transformation can be obtained in less than 1.5 seconds. Other standard features include built-in A/D and D/A conversion, manual keyboard, and digital interfaces. Processed results are displayed in rectilinear or phase-plane form, and are available for readout on to oscillographs, x-y plotters, computers, digital tape, etc. Time-Data Corp., Palo Alto, Cal.

Circle No. 240 on Inquiry Card

SUBMINIATURE DELAY LINE

Measuring only 0.46 in. wide, 1.10 in. long, and 0.2 in. high, a new subminiature molded delay line has a maximum rise time of 10 nanoseconds, a 50 nanoseconds delay time, a temperature coefficient of 140PPM/C, and an impedance of 300 ohms. Unit's small size and operating characteristics are said to make it suitable for applications in printed circuit boards, radar, as well as automation, computer, and instrumentation systems. Valor Electronics, Inc., Gardena, Cal.

Circle No. 255 on Inquiry Card

DIGITAL DRAFTING SYSTEM

A digital drafting system operates at speeds over 700 inches per minute, with an overall system accuracy of 0.002-inches. Resolution is 0.001-inches. Large printing format of standard models (60″ x 60″) enables high accuracy at scale and dimension impossible for engineering draftsmen to attain with mechanized system control. Operation of the drafting system may be on-line under computer control, or off-line via magnetic tape or punched card input. Either 7-track or 9-track mag tape may be used for input. Punched paper tape input, optionally available, is compatible with numerical control tape coding. Benson-Lehner Corp., Van Nuys, Cal.

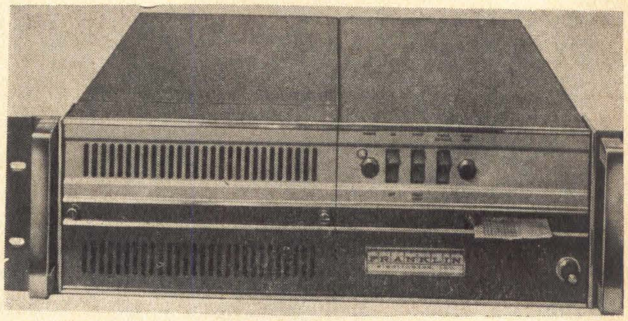
Circle No. 256 on Inquiry Card

NEW PRODUCTS

TIME CODE GENERATOR

A timing system for rapid editing of TV video tapes and controlling the starting and stopping times of TV recorders records a time code on the cue track of the 2" video tape. This time, read from the tape at any speed — playback or rewind — in either direction — is used to start and stop automatically the recorder or other equipment in accordance with the setting of time selector switches. The control panel for the system is mounted in the console of a video tape recorder. The time code generator can be used with any number of recorders. Precise "electronic" splicing can be done with the system, thereby eliminating almost all tape cutting. Electronic Engineering Co., of Cal., Santa Ana, Cal.

Circle No. 253 on Inquiry Card



MINIATURIZED DIGITAL PRINTER

New digital printers give full-size printout and performance in a compact package measuring only 5¼ in. high. The printers, which are available in column widths of 4 to 10 digits, print at a rate of 12 lines per second. One of the features of these new printers is a practical modular construction that permits great flexibility in matching the printer to the physical environment. In addition to the standard 19 in. rack mounting, the printer mechanism and the operating electronics can be separated for half-rack mounting, stacking, remote operation, or other physical requirements. Print capability includes the numerals 0 through 9, and a choice of any one of three sets of six symbols. The choice can be made in the field, at any time, by means of a simple mechanical adjustment. Character input is BCD 8421. Another feature claimed for the printers is a low-operating noise level. This low noise level is said to be achieved by a unique hammer suspension system with a high-resistance noise path into the frame. However, there are no shock mounts or other interposed noise absorbing devices. The sound is absorbed in the air surrounding the hammers. Franklin Electronics, Inc., Bridgeport, Pa.

Circle No. 278 on Inquiry Card

DIGITAL ACQUISITION SYSTEM

A new digital acquisition and compositing system is made up of four units: a PCM unit; a power supply; a magnetic tape recorder; a tape loop; and a digital summer. The system is available in a 7- or 9-track IBM compatible format, or a TIAC compatible 21-track format. It accommodates up-to-63 input channels of analog data. A complete data acquisition system, it quantitizes, encodes, and records analog signals and converts them into the required digital format. Data can be digitized and recorded directly onto a master tape, or, by using the compositor, consecutively generated records are stacked in proper time relation onto a tape loop. Upon completion of the compositing process, the composited (summed) data stored on the tape loop is transferred to the master tape. The system's low power consumption permits it to be operated from storage batteries. Leach Corp., Azusa, Calif.

Circle No. 292 on Inquiry Card

DECODER/DRIVER MODULES

Complete family of universal decoder/driver modules includes 4 line BCD to 7 line and decimal to 7 line decoders in both plug-in and chassis mount configurations. Compactness of the solid-state circuit construction and inherent compatibility with all available 7-segment, incandescent type readouts are said to make the units readily adaptable to meet the diverse requirements of a great variety of applications. With an input signal current as low as 1.4 milliamps, the integrated circuit decoder section accommodates a wide range of logic levels. Units are available with or without a memory capability. Where a memory capability is incorporated, the external access to the memory outputs is provided for the purpose of data-logging, computer input, and other types of information display. Discon Corp., Ft. Lauderdale, Fla.

Circle No. 243 on Inquiry Card

BUSSING STRIP

A bussing strip is a new device for power or ground bussing to which terminated wires may be connected and disconnected without tools. Standard male contacts may be crimped or soldered to wires from size AWG 16 to AWG 24. Connection to the strip is made by pushing the contact into place. Each contact is held by a self-locking retainer. Connections are vibration and shock proof and resist high pulling loads. Any connection may be released, without disturbing the others, with any small diameter probe; a pencil point is a good example. The strips are available in any length to connect 5 or more wires. All connections may be common, regardless of the number; or, each set of five may be separate from the others in the same strip. B. W. Olson & Co., Fullerton, Cal.

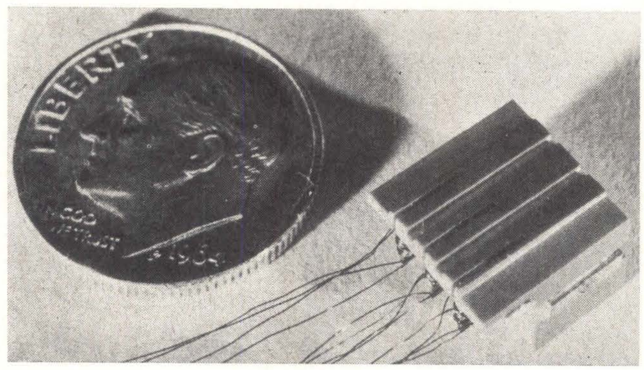
Circle No. 228 on Inquiry Card

NEW PRODUCTS

HIGH-SPEED MEMORY

New core memory system has a cycle time of 0.5 usec. The system features a building block construction where each basic module is either 4092 words or 8192 words by 20 bits. Larger systems can be accommodated by building up the word capacity and bit length in any combination. The 2½ D core stack, sense amplifiers, driver circuits, and information registers are an integral part of the system. An associated memory control module includes timing circuits, address register, and decode logic. Monolithic integrated circuits are used for all logic and registers and hybrid circuits are used for the driver circuits and sense amplifiers. The basic memory module and associated control module is 26¾″ high (including mounting slides) by 20½″ deep (including mating connectors) by 4¼″ wide. The modules are front access slide mounted units. Four of these modules will mount in a standard 19″ rack. Burroughs Corp., Electronic Components Div., Plainfield, N.J.

Circle No. 280 on Inquiry Card



DISC RECORDING HEAD

A new magnetic recording head for flying disc data recording applications flies as low as 50 microinches above the surface of the disc. This minute clearance between head and disc is believed to be unprecedented in a standard head (flying distance varies, of course, with disc speed loading and track configuration). The very low altitude and high packing density capabilities of the head were achieved through a new case design with improved aerodynamic characteristics and company's proprietary glass-bonding technique. Reduced flying distance permits higher outputs by minimizing space losses. Drive requirements are also correspondingly lower. Resolution of the new head is 1,500 flux changes per inch, and it is available on a standard basis in 1 to 12 tracks. Also available are custom versions of this head with shorter gap lengths to provide resolution up to 5,000 flux changes per inch. Ferroxcube Corp., Saugerties, N.Y.

Circle No. 282 on Inquiry Card

LOW IMPEDANCE DELAY LINE

Said to be used in wide variety of transistorized circuitry where small size and reliability are necessary requisites, a new ultra-miniature delay line features a delay time of 100 nanoseconds, a rise time of 35 nanoseconds, and an impedance of 20 ohms. Measuring an even inch in length, the unit is only 0.375 in. wide and 0.25 in. high. Direct current resistance is 5 ohms, max. With a maximum attenuation of 10% and working voltage of 50 VDC, the delay line operates in an environmental temperature range from −55 to +125C. Valor Electronics, Inc., Gardena, Cal.

Circle No. 232 on Inquiry Card

CARD-EDGE RECEPTACLE

A new card-edge receptacle features standard telephone equipment design and incorporates 18 wire-wrap contacts spaced on 0.150″ centers. It accommodates a 1/16″ pc card. Made of phosphor bronze with a gold flash over a nickel underplate, the contacts are of the double-cantilever, bifurcated-nose type with −.045″ square wire-wrap tails available in two lengths to accommodate different numbers of wraps. The insulator is molded of glass-filled diallyl phthalate per MIL-M-14F, type SDGF. A stainless steel clip, which fits between contacts and mates with a pc card cutout, provides polarization. Elco Corp., Willow Grove, Pa.

Circle No. 284 on Inquiry Card

BCD DATA SCANNER

A BCD data scanner accepts up to 10 digital words, with up to 8 BCD characters each. It sequentially scans these input words and presents them, together with channel identification, for recording on a digital printer, paper tape punch, incremental magnetic tape recorder, or any other suitable digital recording device. The input words may be derived from a digital counter, digital voltmeter, or other data source which provides parallel BCD information. The scanner consists of standard silicon solid-state logic modules which make extensive use of integrated circuits. Three standard modes of operation are provided: single scan; sequential scan; and random scan. In the single scan mode, the scanner steps once through the selected inputs upon receipt of a scan command, and stops at the end of a cycle. In the sequential scan mode, the scanner interrogates the selected inputs in sequence, stopping at each channel until a data ready command is received. This process continues until the scanner is commanded to stop. In the random scan mode, the scanner continuously interrogates the selected inputs, in sequence, but stops only on a channel which presents a data ready indication. In each mode the BCD data is presented to the output whenever the data ready command is present. Ten toggle switches are provided on the front panel to bypass unused channels. Instrumentation Technology Corp., Van Nuys, Cal.

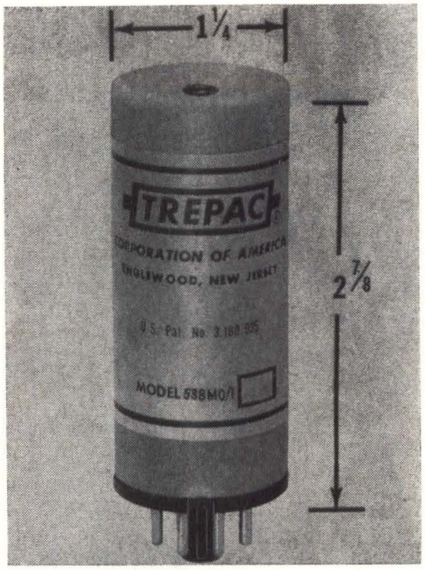
Circle No. 277 on Inquiry Card

NEW PRODUCTS

PRINTED CIRCUIT CONNECTOR

A new printed circuit card-edge connector features terminations designed for wire-wrapping. This unit is available with 28 dual contacts providing 56 wiring terminals on 0.125" center-to-center spacing. Contact terminals are 0.025" square to permit most effective wire-wrapping procedure for up to three, #26 AWG wires on each. The dual readout, bifurcated contacts are patented "Bellow-form" design providing added reliability to any printed circuit interconnection using a 1/16" printed circuit board. A polarization key is available for insertion between any two adjacent contacts, when required. Continental Connector Corp., Woodside, N.Y.

Circle No. 217 on Inquiry Card



COMPUTER INTERFACE

A transistorized polar interface was specifically designed to provide isolated keying of a neutral or polar teletype writer line from a low level polar signal available from a computer or other signal-generating devices. The Model 538-MO/1 combines unique transistorized input circuitry with a special high-speed mercury wetted-contact capsule to provide operation which is essentially bounce and distortion free. Tested life expectancy is rated in excess of several billion operations. The unit has a keying speed of 200 bits/sec with less than 2% distortion. It will operate with signals as low as 0.5 milliamperes. An electronic bias balancing control permits equalizing keyed output despite input signal variations of up to 30% from unequal driving signals or supply voltages. An internal suppressor network permits the output contacts to handle safely any voltage up to 140V on each contact and currents up to 140 ma. Trepac Corp. of America, Englewood, N.J.

Circle No. 275 on Inquiry Card

FREQUENCY COUNTER

A new frequency counter designed as either a rack or bench-mount test instrument for measuring frequency or totalizing the number of input cycles or events, features 1¾″ panel height and plug-in transistors. Numerical indicator tubes provide bright in-line, long-life display. Maximum input sensitivity is 10 mv rms for frequencies from cps to 200 KC, permitting direct operation from low level sine wave signals. Gate times of 0.1, 0.6, 1.0, 6.0, and 10 seconds are derived from a 60 cps line frequency. Variable display time is from 0.2 seconds to 6 seconds and hold. Plug-in transistors in the circuit boards are said to result in simplified trouble shooting and maintenance. Anadex Instruments Inc., Van Nuys, Cal.

Circle No. 229 on Inquiry Card

COMPUTER PERIPHERAL POWER

A new hydraulic servo power package, featuring extremely low noise level and elimination of external leakage, was designed for use with computers in office environments. The unit is used to power discs, drums, actuated read-write heads and removable media systems in environments where standard units would produce annoying noise and where oil leaks would be unsightly and hazardous to personnel. Noise has been minimized through design of components to eliminate pulsations, special LSC tuning techniques, and reduction of velocities. Suspension of the moving elements from the main frame with vibration isolators prevents mechanical vibration from being transmitted. Although the unit is virtually leakproof, any seeping oil runs back into the reservoir to eliminate the possibility of leakage onto the floor. The hydraulic servo package comes as an integral, completely self-contained unit. To insure single responsibility for the complete hydraulic system, the manufacturer provides a line of low friction, high-speed electrohydraulic actuators to position read-write heads on moveable-head disc systems. Lawrence Systems Corp., Willow Grove, Pa.

Circle No. 267 on Inquiry Card

NEW PRODUCTS

DATA DISTRIBUTORS

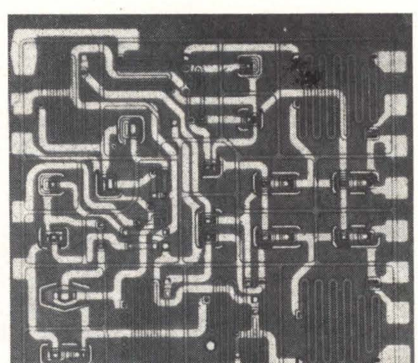
New data distributors are complete half-duplex serial/parallel converters with integral control circuits to connect digital processing devices to serial communications subsets and teleprinters. In the transmit mode, one model accepts parallel data from the user in 5, 7 or 8 bit characters. Five level units output serial baudot code with 1 start and 1½ stop bits. Seven and 8 level units output serial characters with 7 level having 1 stop and 1 start bit, while 8 level ASC format has 1 start and 2 stop bits. The serial output is in polar form in compliance with RS232B. In the receive mode, units accept incoming serial data at RS232B levels in 5 level baudot, 7 level start-stop or 8 level ASC. Deserialized output is presented in parallel with control signals and parity check. An automatic impulse noise discriminator rejects line pulses less than ½ data bit in width. Parity check is provided as well as control circuits specifically designed to flag and load from processor I/O buffers. Western Telematic, El Monte, Cal.

Circle No. 223 on Inquiry Card

GRAPHIC DATA PROCESSOR

A new graphic data processor is said to be capable of digitizing oscillographs, slides, and arbitrary graphic forms; mathematically scaling and operating on digitized curves; and displaying or recording the resulting forms on an associated CRT or X-Y plotter. Basic software, or programming, to operate upon the curves or functions that have been entered into the processor, is an integral part of the system. The digital graphic input component of the new system consists of a 10" x 10" writing surface which is based on the Rand Tablet, and a pen-like stylus for selecting a point on the two-dimensional electronic surface. Before the curve is "loaded" into the processor, the program leads the operator through a calibration procedure when minimum and maximum graphic locations are designated and their values typed in. The relative position of the curve on the writing surface is held by the processor, permitting all subsequent curve data to be "deskewed" before processing. Once stored, a second curve may be loaded in the same manner or from the typewriter keyboard or punched paper tape reader. The system can then perform analyses involving both curves, such as calibration corrections. Bolt, Beranek and Newman, Inc., Data Equipment Div., Santa Ana, Cal.

Circle No. 266 on Inquiry Card



IC OPERATIONAL AMPLIFIER

A new integrated circuit operational amplifier is said to offer extremely low current offset, and current offset drift vs. temperature. Offset voltage is adjustable to zero with external potentiometer, ±10 V common mode voltage, 15 na differential input offset current, 175 pa/°C (max.) differential input offset current drift, 10 uv/°C (max.) input offset voltage drift. Other significant parameters are 5 mv (max.) input offset voltage, 50 na (max.) input biasing current, 2 ma (min.) output current drive, and 35,000 (typ.) open loop voltage gain. The circuit is packaged in JEDEC TO-101, and operates over a temperature range of −55°C to +125°C. Union Carbide Electronics, Mt. View, Cal.

Circle No. 203 on Inquiry Card

BCD ENCODER

New brush-type encoder provides a 1000 count cyclic BCD output for a single turn input. Higher count multi-turn input units are also available, all having an accuracy of ±1 bit. The encoder is provided with a size 30 servo mounting arrangement and is designed to meet the environmental requirements of MIL-E-5272 with an operating temperature range of −55° to ±125C. The wiper circuits are rated for 100 ma. resistive loads with 28 vdc operating voltage. The contact resistance is less than one ohm per circuit. Collectron Corp., New York, N.Y.

Circle No. 201 on Inquiry Card

PATTERN RECOGNITION

Pattern-recognition system, called Socrates, was designed to meet the varied and diversified requirements of many research facilities and computer service centers. Its capability to separate, identify, classify, analyze, reject or select at a high rate of speed after a simple learning process permits the researcher to save considerable time in experimental programs that involve distinguishing among patterns that can be presented in graphic form. Depending upon the complexity of the problem, Socrates can be programmed to have between 2 and 504 classes or subclasses. For the uncomplicated training process, samples of the desired information are presented to the system in graphic form. The system is then placed in the "recognize" mode. New patterns can be submitted as "unknowns," and Socrates will identify the class or grouping to which the new pattern belongs, indicating the "level of confidence" of the class assignment. Normal operations are stored internally and selected by control-panel switches. The learning and recognition program can be applied to any pattern-separation problem reducible to 35mm transparency form. In addition, patterns generated or processed on a general-purpose computer can be directly introduced to Socrates, allowing experimentation with complex reference-function operations. Scope Inc., Reston, Va.

Circle No. 225 on Inquiry Card

NEW PRODUCTS

TAPE READER

Photoelectric tape reader reads translucent and opaque tapes at speeds up to 150 lines per second. The tape is transported through the reader on a unique sprocket drive which allows reading of 5, 6, 7, or 8 level tape without adjustment of the reader. Tapes with leading sprocket holes may also be read without reader adjustment. The tape drive allows starting and stopping of the tape for several thousand passes through the reader with no discernible tape wear. There are no wearing parts on the reader so no routine maintenance is required. Tape is read in a protected area free from external light and dirt. A single lamp with a rated life of over ten years delivers essentially constant light over the entire sensing array. Phototransistors, used as the sensing elements, produce large signal-to-noise ratio and eliminate drift problems. This allows remote operation of the reader from its logic without fear of spurious signals. Decitek, Inc., Worcester, Mass.

Circle No. 272 on Inquiry Card

OPTO-ELECTRONIC RELAYS

In a new line of opto-electronic switching devices, input and output circuits are isolated electrically by means of lamp-to-photocell light-beam coupling. Insulation resistance is in the order of 10^9 ohms with smooth turn-on and turn-off. Input and output voltages may be ac or dc. Voltage gain is high, with signals as low as 6 volts capable of controlling output circuits rated to 250 volts. Functions include isolation interface switching, logic switching (AND/OR gate, inverter, and latch circuits), audio switching, multiplexing, data sampling, feedback gain control, and noiseless potentiometer. Designed for high-density printed-circuit packaging, the devices occupy only a quarter cubic inch and weigh a quarter ounce. An aperture at either end showing light or no-light permits visual checking of on-off states. Input signals of 6, 12, 24, or 150 volts ac or dc cause resistance to change, typically from an off level of 10 megohms to an on resistance of less than 500 ohms, a switching ratio of 10^5 achieved smoothly without transient effects or bounce. Output cells are suitable for switching from millivolts to 250 volts dc or peak ac, and single-cell power dissipation is as high as 500 milliwatts. Sigma Instru, Inc., Braintree, Mass.

Circle No. 204 on Inquiry Card

PLUG-IN MEMORY PLANES

A new core memory storage plane is said to feature both low-cost and substantial saving of assembly time. Called "Platrices," they are expected to find wide application in memory systems for desk-top business machines, digital instrumentation and many types of control equipment. A stack of Platrices is mounted on a printed circuit board as simply as a transistor or other component. Connection pins at the bottom of the stack are pushed through the board and these leads are then soldered in the usual manner. Low cost of the Platrix itself, according to the manufacturer, is achieved by special construction utilizing frames of conventional planes. For high resistance to shock and vibration, the cores are fixed to a base plate of the same material by a special lacquer. Frames and protection plates of paper base laminate can be supplied if desired. Stacks of up to four Platrices can be furnished with series connected drive lines terminated in the plug-in connections at the bottom of the stack. Low drive currents (190 ma) allow use of simple drive and selection circuits. The planes are wired in 4-wire coincident current scheme. Units are available in 8 standard configurations with bit capacities from 256 to 1,024. Nonstandard sizes can be supplied on special order. Ferroxcube Corp., Saugerties, N.Y.

Circle No. 231 on Inquiry Card

SAMPLING OSCILLOSCOPE

A 7 gigahertz sampling oscilloscope consists of a main frame, verticle plug-in, and horizontal plug-ins. Specifications on the dual trace unit include the 7Ghz bandwidth; 7Ghz trigger bandwidth; less than 20 picoseconds trigger jitter; risetime of less than 50 picoseconds; and less than 10mv of noise, peak-to-peak. Operational features of the scope include a beam finder; easily accessible operator controls; no external sampling head requirements; and completely solid state with the exception of the CRT. E-H Research Laboratories, Oakland, Cal.

Circle No. 216 on Inquiry Card

TIME-SHARING ENCODERS

A new shaft encoder was designed for multi-point digital display. With a single set of electronics, called the display module, many shaft encoders are used to transmit digital data sequentially. Considerable cost savings result since only one display module need be used in a complete system. Each encoder is constructed so that there is no interaction from the other parallel-connected encoders. The new encoder also features a direct-decimal code, rather than conventional computer codes, so that its output can directly energize display and data-logging devices without affecting performance. Theta Instrument Corp., Fairfield, N.J.

Circle No. 208 on Inquiry Card

INTERFACE MODULES

Two dry reed relay interface modules — in 6, 12, 24, and 48 vdc — are used for two-voltage systems, circuit isolation, power amplification, inversion, or mainframe to software connections. The modules are built on standard 1/16 inch glass epoxy printed circuit boards with 2 ounce copper circuits. The boards have a life expectancy of 20×10^6 under full load and 500×10^6 under light load. Module 900-1000 consists of 10 normally-open, single pole, single-throw relays. Module 900-1001 contains 10 single pole, double-throw Form C relays. Wabash Magnetics, Inc., Wabash, Ind.

Circle No. 262 on Inquiry Card

LITERATURE

Printed Circuit Manual

Techniques for the design/production of printed circuits and assemblies are detailed in a 16-page technical booklet. It covers such critical design/production considerations as: various manufacturing methods, with advantages and/or disadvantages of each; how to select electroplates to enhance electrical or mechanical properties; hints for specifying dielectric base materials best suited for intended applications; eyelet versus plated-through holes in two-sided circuit patterns; and a discussion of general design, production, and functional parameters of multi-layer circuit boards. Extensive charts illustrate such data as current carrying capacities of given circuit pattern thicknesses, performance characteristics of base materials, an easy-to-read table giving applications and properties of plated coatings, cutaway renderings of various multilayer termination alternatives, etc. Industrial Circuits Co., Fairfield, N.J.

Circle No. 317 on Inquiry Card

Real-Time System Computer

A 12-page brochure describes a general-purpose 24-bit parallel binary computer, the SEL 840A. The IC computer's basic configuration includes 4K memory, hardware index registers, hardware multiply and divide, and a Teletype input/output typewriter with paper tape reader and punch. Internal memory full cycle time is 1.75 microseconds. An optional extended arithmetic unit performs hardware, single and double precision, fixed point, and floating point arithmetic. Typical applications to date include rolling mill process control, aircraft brake and wheel testing, space vehicle vibration testing and jet aircraft simulation. Systems Engineering Labs, Ft. Lauderdale, Fla.

Circle No. 324 on Inquiry Card

Germanium Transistors

A comprehensive germanium transistor application guide lists over 130 transistor types. The guide keys individual transistor types to product family, performance range, and specific circuit application. General Instrument Corp., Hicksville, N.Y.

Circle No. 307 on Inquiry Card

Data Communications

Detailed descriptions, specifications, and applications of a new series of data communications equipment are provided in a new 16-page brochure. Both character-oriented and message-oriented modular units are described. The character-oriented units are for applications requiring a large number of low-speed lines (up to 150 words per minute) or applications requiring character-by-character processing. The message-oriented units control high-speed message transmission without programmed inspections of each character. Scientific Data Systems, Santa Monica, Cal.

Circle No. 318 on Inquiry Card

Test Instruments

A new 16-page condensed catalog describing a complete test instrument line is sectionalized for convenience into four major categories: Semiconductor test systems, digital voltmeters, oscilloscopes, and components. The first section includes test equipment for transistors, integrated circuits, printed circuit boards, welded modules, and complex arrays. The oscilloscope section describes a full line of high and low frequency, and special-purpose oscilloscopes as well as transistor curve tracers, oscilloscope cameras, and accessories. The component section includes differential and operational amplifiers. Fairchild Instrumentation, Mt. View, Cal.

Circle No. 314 on Inquiry Card

Stepping Motors

Latest data on a patented "Cyclonome" stepping motor, which directly converts digital pulse inputs to analog shaft output motion, is available in a new 12-page booklet. This line of electro-magnetic instrument stepping motors has been expanded to include 8 uni-directional models and four bidirectional models. All offer 20-steps-per-revolution operations, in precise 18-degree increments, at speeds to 450 steps a second, and at torques ranging to 350 gram-centimeters. Only successive dc pulses of alternating polarity, as provided by simple oscillators, flip-flops relay circuits, commutators, or manual switches, are required to actuate the motor. Such pulses, applied to the motor coil, shift the direction of the powerful magnetic force field generated by the motor's two permanent magnets. Location of these magnets in the stator — not in the rotor, as in other stepping devices — frees the motor from inertia-induced limitations and assures true high-speed motion. Sigma Instruments, Braintree, Mass.

Circle No. 305 on Inquiry Card

Electronic Counters

A six-page catalog contains complete specifications and prices for solid-state counters, including counter-timers, bi-directional counters, variable time base counters, and preset counters. Over thirty standard and special application counters are described. Anadex Instruments Inc., Van Nuys, Cal.

Circle No. 311 on Inquiry Card

Cordwood Modules

Brochure describes company capabilities for the development and fabrication of high-density electronic cordwood modules and components. The publication includes a description and photographs of company's facilities for production and photographs of components the company is manufacturing for the lunar module. Arma Division, American Bosch Arms, Garden City, N.Y.

Circle No. 328 on Inquiry Card

Automated Measurement System

An automated digital measurement system is capable of more than 100 dynamic tests per second. The system consists of an analog display unit, a digital measuring unit, and special sampling units. System measuring instruments and peripheral equipment are programmed digitally utilizing a rotating-disc memory, programming control circuitry, and serial-to-parallel registers. Programming can be accomplished easily on or off line. Self-calibration can be programmed into the system, providing 1% accuracy. Devices under test are fed through a test station and categorized by a new automatic handler and sorter. Booklet describes the system. Tektronix, Inc., Beaverton, Oregon.

Circle No. 331 on Inquiry Card

Electronic Hardware

A new 36-page catalog of electronic hardware covers electronic terminals in the following categories: single, double, and triple turret; tubular; split and milled; proto-board; pin-type; threaded and printed circuit. It also includes standard and miniature terminal boards, handles, panel and chassis hardware. It lists applicable mil specs for the hardware and the types of finishes available. Also included are cross reference sheets showing that the company stocks the equivalent standard terminal of major U.S. manufacturers of those terminals specified by MIL-T-55155 and also terminals to NASA specs. Concord Electronics Corp., New York, N.Y.

Circle No. 303 on Inquiry Card

Woven Plated Wire Memory

The latest in woven plated-wire memories is described in a data sheet. The high-capacity memories are available in both complete memory planes and multi-plane stacks. Access speeds are less than 100 nanoseconds. Special features and methods of packaging are described and a typical stack schematic as well as read and write waveforms are provided. General Precision, Librascope Group, Glendale, Cal.

Circle No. 309 on Inquiry Card

Power Supplies

A 14-page catalog lists more than 62,000 different power supplies. Both single and dual plug-in power supplies are listed. Nominal output voltages range from 1 to 900 volts with output currents to 3.0 amps. Applications include operational amplifiers, logic circuits, test equipment, IC's, and lamp and relay circuits. A continuously-variable 1 to 30 volt laboratory power supply is also described. Acopian Corp., Easton, Pa.

Circle No. 302 on Inquiry Card

Power Supply Selection

Vest-pocket guide was devised to help the engineer easily and quickly specify and select power supplies from company's line of 125 models. Prepared in flow chart form, this guide presents four basic parameters of power supply operation, making it possible for the engineer to narrow down his choices on the basis of output regulation, voltage output, programming speed, and power output. Other characteristics that enter into selection, such as constant voltage, constant current, physical configuration, range, etc., are also taken into consideration and can be accepted or rejected as the reader scans the guide. Hewlett-Packard/Harrison Div., Berkeley Heights, N.J.

Circle No. 301 on Inquiry Card

Pushbutton Switches

Catalog sheet presents complete data on momentary action switches for mounting in 3/8" clearance hole on 19/32" centers. Designed to meet the application needs of the computer, data processing, and automation industries, this switch series is available illuminated or non-illuminated. Illuminated push-button switches accommodate permanently mounted T-2 neon lamp with or without the required current-limiting resistor. The catalog sheet contains drawings and catalog number charts to facilitate selection of the required pushbutton switch. Dialight Corp., Brooklyn, N.Y.

Circle No. 312 on Inquiry Card

LITERATURE

Circuit Card Files

A 4-page brochure provides a complete description — including assembly instructions — of a firm's new precision circuit card and connector mounting file kits. Among the highlights of the brochure are illustrations and tables demonstrating the kits' high degree of flexibility in providing secure, rigid mounting for almost any size circuit card, as well as for connectors of virtually any type and size. Included, also, is a series of illustrations depicting the step-by-step assembly of the kits, as well as full ordering information based on card and connector size. The file kits feature precision-molded nylon card guides and connector mounting feet to provide automatic connector/card alignment. Units are capable of housing up to 27 circuit cards per file, in card sizes from 6-to-8″ in length and from 0.75″ to 6.25″ in width. Scanbe Manufacturing Corp., Monterey Park, Cal.

Circle No. 320 on Inquiry Card

Time-Code Generator

An airborne time-code generator with modified IRIG B code and designed to meet Mil E-5400 for shock and vibration requirements is described in a data sheet. The unit provides serial dc level shift time-of-day code (hours, minutes, and seconds) in modified IRIG B 20 bit, 100 pps form as well as a 20 bit 10 pps slow code. Pulse rate outputs of 10 pps, 5 pps, 4 pps, and 1 pp2s are provided as solid state switch closures. Two parallel time code outputs are also available. One is in BCD form to operate an aircraft instrument size display and the other is in decimal form for use by a Nixie display showing time in hours, minutes, seconds, 1/10 seconds, and 1/100 of seconds. Electronic Engineering of Cal., Santa Ana, Cal.

Circle No. 325 on Inquiry Card

Wire Harness Accessories

A 12-page brochure describes a complete line of wire/cable harnessing, wire/cable marking, and wire/cable accessory products. Included are three different types of harnesses, adjustable P-clips, three different types of markers and grommet strip. Each is fully described and illustrated with dimensional drawings and tables providing complete physical properties, chemical properties, applications, ordering data and applicable specifications. The differences and application advantages of each of the different products are explained. Components Equipment Div., Electrovert, Inc., Mt. Vernon, N. Y.

Circle No. 319 on Inquiry Card

Subminiature Lamps

Specifications and ordering information on a series of subminiature indicator lites, either neon or incandescent, are contained in a 2-page bulletin. The series was developed to meet the demand for high density indicator display on small console panels. The light is contained in a body only 0.360″ diameter by 0.250″ long, and mounts in a one-quarter inch hole on center as close as 3/8″. Lenses are offered in several colors, both transparent and translucent. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 322 on Inquiry Card

Magnetic Tape Maintenance

32-page booklet, entitled "Magnetic Tape Maintenance for Computer Managers" contains the following sections: "The Tape Management Program," "The Technology of Tape Preventive Maintenance," "The Tape Preventive Maintenance and Rehabilitation Process," and "Why is Tape Preventive Maintenance Needed?" The text deals with tape problems faced by computer tape users and offers a defined program to reduce both operating cost and new tape procurements. General Kinetics Inc., Arlington, Va.

Circle No. 308 on Inquiry Card

You'll have countless opportunities for career growth as an IBM programmer

Pictured above is the tape library for Gemini/Apollo missions showing taped data acquisition which could help you as a Programmer in IBM's Federal Systems Center.

In the area of space exploration, IBM Programmers have written hundreds of instructions for the most sophisticated real-time systems in the world, for instance, guidance and on-board computers for Gemini spacecraft and Apollo launchings.

As an IBM Programmer in the Federal Systems Division, you could become involved with some of the new ideas—new techniques—new systems—such as ballistic missile re-entry programs, communications traffic or survivability programs. IBM Programmers *decide* the best rational approach to problems, *specify* necessary steps, and *test* results. There are countless opportunities for your career growth.

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LITERATURE

Reed Relays

Four types of sealed-contact reed relays, designed specifically for printed circuit boards, are described in an engineering bulletin. Complete electrical, environmental and mechanical characteristics for the following relay types are given: Type CRT — standard terminal reed relays; Type CRTN — narrow terminal reed relays; Type CHT — mercury-wetted reed relays; Type CRT — high voltage reed relays. Standard part numbers and coil characteristics for the various contact forms available are also included. The relays provide high switching capacity per package and ample switching speed in the low millisecond range for most industrial control systems. These switching devices also provide isolated switching from low level to power ac to dc and are insensitive to transient noise. C. P. Calre & Co., Chicago, Ill.

Circle No. 310 on Inquiry Card

Cathode-Ray Tube Guide

A quick reference guide lists a complete line of military and industrial cathode-ray tubes for radar display, computer readout, and oscilloscope applications. The 12-page guide gives physical and electrical characteristics, including dimensions, typical operating conditions, and resolution capabilities. Tube types are categorized as electrostatic focus and deflection, magnetic deflection in round sizes from one to sixteen inches, magnetic deflection in rectangular sizes from eight to twenty-three inches, rugged tube-yoke-shield packages and tube and component assemblies. Typical pin connection diagrams are illustrated for 24 different basic electron gun types. Westinghouse Electronic Tube Div., Elmira, N. Y.

Circle No. 326 on Inquiry Card

Stepping Servomotors

Two-page bulletin provides technical information on five 28-volt stepping servomotors that have holding torques from 0.3 to 6.0 ounce-inches. There are descriptions of the characteristics of these 90-degree stepping servomotors and some typical applications. The larger stepping servomotors will step at rates of 125 pps, or better; the smallest model will step at rates of 230 pps. Slewing speed is 150 pps for the largest and 1400 pps for the smallest. These rates are attributable to the low inertia of the permanent-magnet rotor. Diehl Div., The Singer Co., Somerville, N.J.

Circle No. 306 on Inquiry Card

Electronic Counters

A 6-page catalog covers a complete line of electronic solid-state counters and frequency instruments. It contains complete specifications and prices of solid-state counters, including counter-timers, bi-directional counters, variable time base counters, and pre-set counters. Over forty standard and special application counters are described. In the section devoted to frequency instruments are descriptions and prices on dc-to-frequency converters, frequency-to-dc converters, frequency detecting switches, frequency meters, and frequency deviation meters. Anadex Instruments, Inc., Van Nuys, Cal.

Circle No. 300 on Inquiry Card

Electronic Calculator

A new 10-page brochure describes an electronic printing calculator that offers expanded programming capability — up to 42 steps — combined with a line-by-line printed record of all calculations, electronic speed, and simplicity of operation. The unit can "learn" complex mathematical routines and thereafter perform them automatically as the operator enters variables. The brochure briefly explains design features and gives sample program instructions for solving quadratic equations and percent change problems. Monroe International, Inc., Orange, N. J.

Circle No. 327 on Inquiry Card

Diode Matrix Applications

Applications of monolithic diode matrices to EDP systems are described in a new 60-page manual "Diode Matrices-Technical Information and Applications." Prepared as an aid to the systems designer, the manual explains the dielectric isolation principle and metalized fuse link interconnection technique as applied to the integration of custom-patterned diode matrices. The manual provides detailed information on matrix configurations, electrical characteristics as well as applications, featuring matrices used with new low and high voltage monolithic interface circuits. Radiation Inc., Melbourne, Florida.

Circle No. 315 on Inquiry Card

IC Readouts

Data sheet describes a complete line of transistor-controlled indicators and readouts designed to operate from typical integrated circuit logic levels. The indicators simplify design by providing lamp control logic within the indicator, eliminating the cost of designing, assembling, and testing external lamp control circuits. They offer integral, isolated switches, press-to-test feature, RFI shielding, and replaceable lamps. Information is also included on digital readout devices for integrated circuits. They are designed to operate from decimal input or from 4-wire 1,2,4,8 BCD input. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 321 on Inquiry Card

Plug-In Memory System

A 4-page brochure describes a new controller that is a complete universal plug-in memory system for use with almost any computer system. Operating in either serial or parallel mode, the unit features word transfer rates of from 50 microseconds per word to 900 nanoseconds per word, and can transfer information to and from two computer central processors. The system is also supported by a comprehensive operating subroutine package. Bryant Computer Products, Walled Lake, Mich.

Circle No. 323 on Inquiry Card

Tape-To-Tape Equipment

A new 12-page brochure describes how a paper tape-to-tape system transmits and receives data at speeds of 105 characters per second (1050 words per minute). Used for a wide variety of high-speed data communications applications, the equipment can transmit the paper tape output of Teletype ASR (automatic send-receive) sets, self-contained paper tape punches, computers, and other business machines. Tape output of the receiver can be converted to page copy by other Teletype equipment, or can be used directly with computers and business machines. The sets operate on any 5, 6, 7, or 8-level code. Teletype Corp., Skokie, Ill.

Circle No. 332 on Inquiry Card

Wire/Cable Chart

A new wall chart is said to have condensed all necessary data for the proper selection of interconnecting wire and cable used in process instrumentation. It contains two handy tables. One table classifies signal wire by application according to type of electrical signal, sensor, electrical noise, and receiving element. The other table specifies the proper instrument wire for economically delivering a "clean" signal in each application. Types of electrical noise — static, magnetic, common mode, and cross talk — are defined, and examples of relative noise levels in various environments are presented. Samuel Moore & Co., Dekoron Div., Mantua, Ohio.

Circle No. 316 on Inquiry Card

For more information on editorial items

Circle No. on Reader Inquiry Card opposite Back Cover

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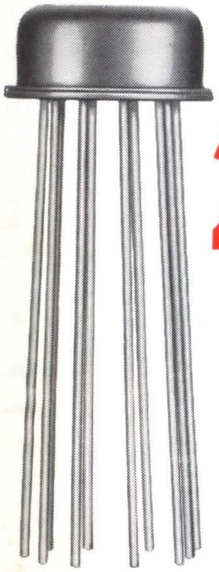
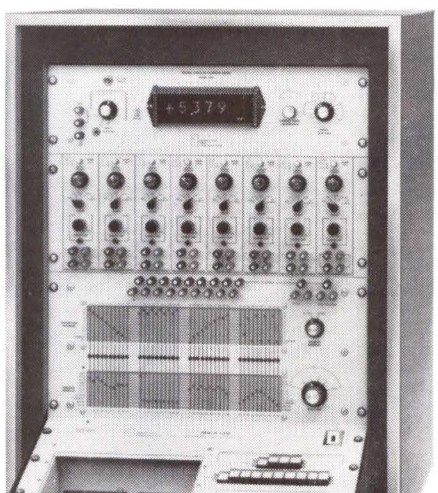
ADVERTISERS' INDEX



now you can test 24 parameters of a 10-pin microcircuit in 2 minutes flat...

with this new semi-automatic IC analyzer

MICA 150



Now even a non-technical operator can speed through comprehensive DC tests on all types of IC packages with from 2 to 40 pins. Test conditions are easily set up on the programming switches of MICA-150 and pushbutton sequencing of the test from pin-to-pin of a device is simple and fast with test results indicated by direct digital readout. On a typical 10-pin, 5-input gate circuit, as many as 24 parameters of the device can be checked within two minutes without changing a single crossbar switch.

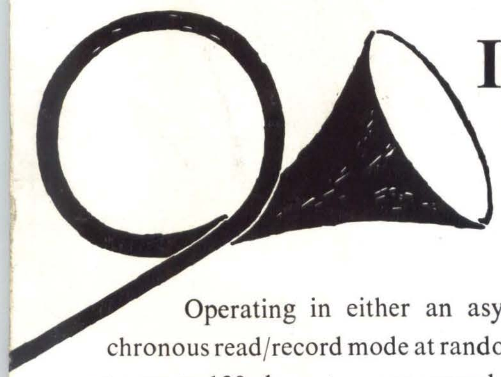
For additional information on applications of MICA-150 for DC or high frequency testing, contact W. Leo McBlain, (609) 424-2400

COMPUTER TEST CORPORATION

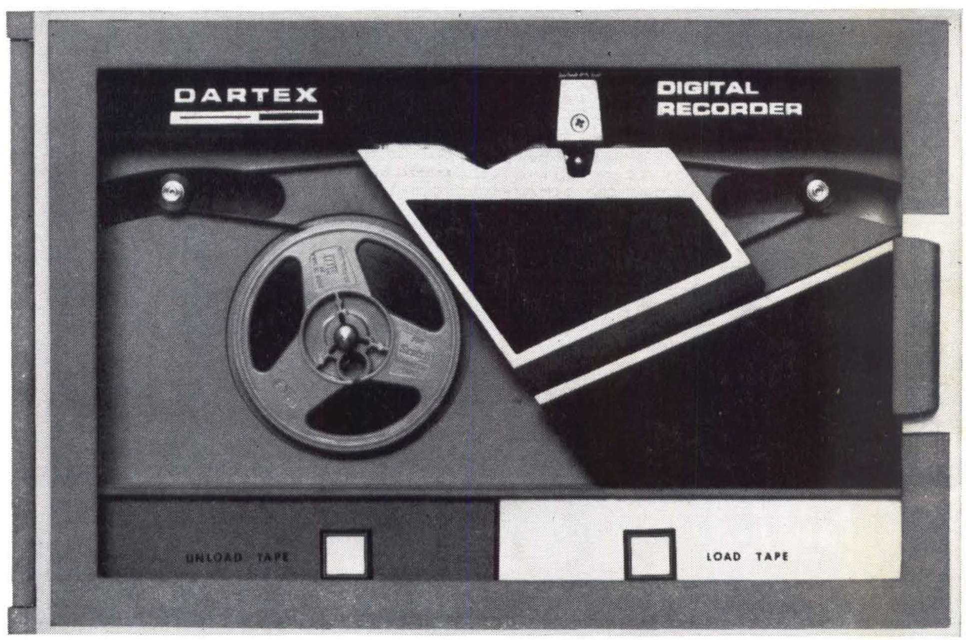
CHERRY HILL, NEW JERSEY

CIRCLE NO. 50 ON INQUIRY CARD

Tally-Ho!



Introducing the highly reliable Dartex 1020 incremental digital mag tape transport.



Operating in either an asynchronous read/record mode at random rates up to 120 characters per second or in a continuous read/record mode of 1600 characters per second, the new Dartex 1020 read/write transport features the ability to accept eight bit parallel characters from various slow input devices for fast output.

Using an advanced tape drive technique, the 1020 features a single capstan that engages the tape constantly, thus wear to the tape and transport mechanism is minimized. Capacity is up to 240,000 characters on each reel of tape.

The compact size of the low cost Dartex 1020 allows easy mounting into a console, rack mount, or desk top enclosure. Other features include gentle tape handling, precise control of tape motion, backspace and re-record, and a design which minimizes and simplifies maintenance. A broad line of interfaces is available—from basic tape transport through telephone line and typewriter options.

Applications for the Dartex 1020 include data transmission, data logging, numerical control of machine tools and graphic arts machines, low cost computer input/output, and auxiliary storage for digital displays. The development of the Dartex 1020 is just one more step in Tally's plan to provide peripheral equipment using the right media at the right time for the right cost.

For complete information, please write Tom Tracy, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) MA 4-0760. In Europe and the U.K., address Tally/APT, Ltd., 6a George Street, Croydon, Surrey, England. Phone: MUN 6838.

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