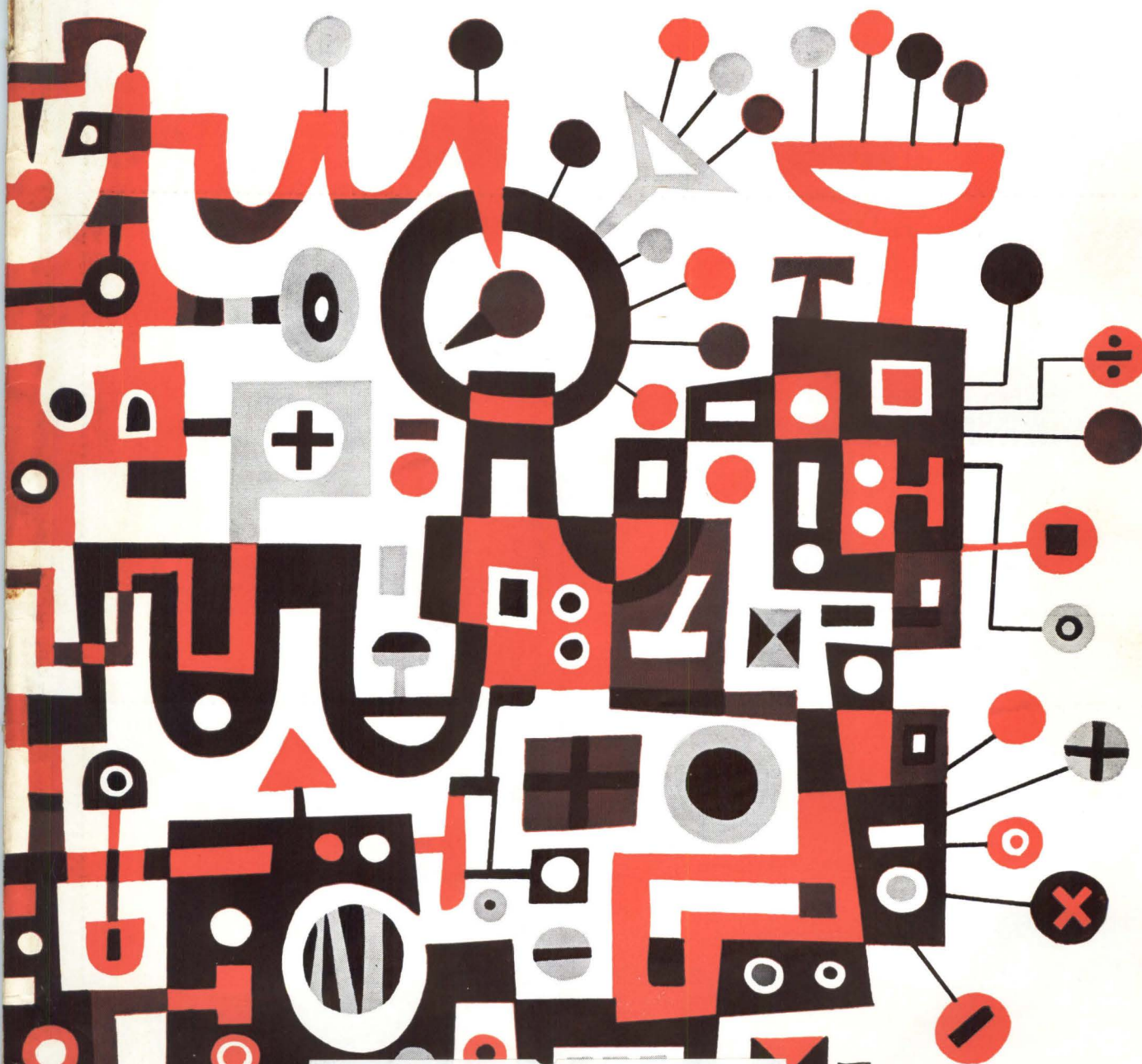


COMPUTER DESIGN

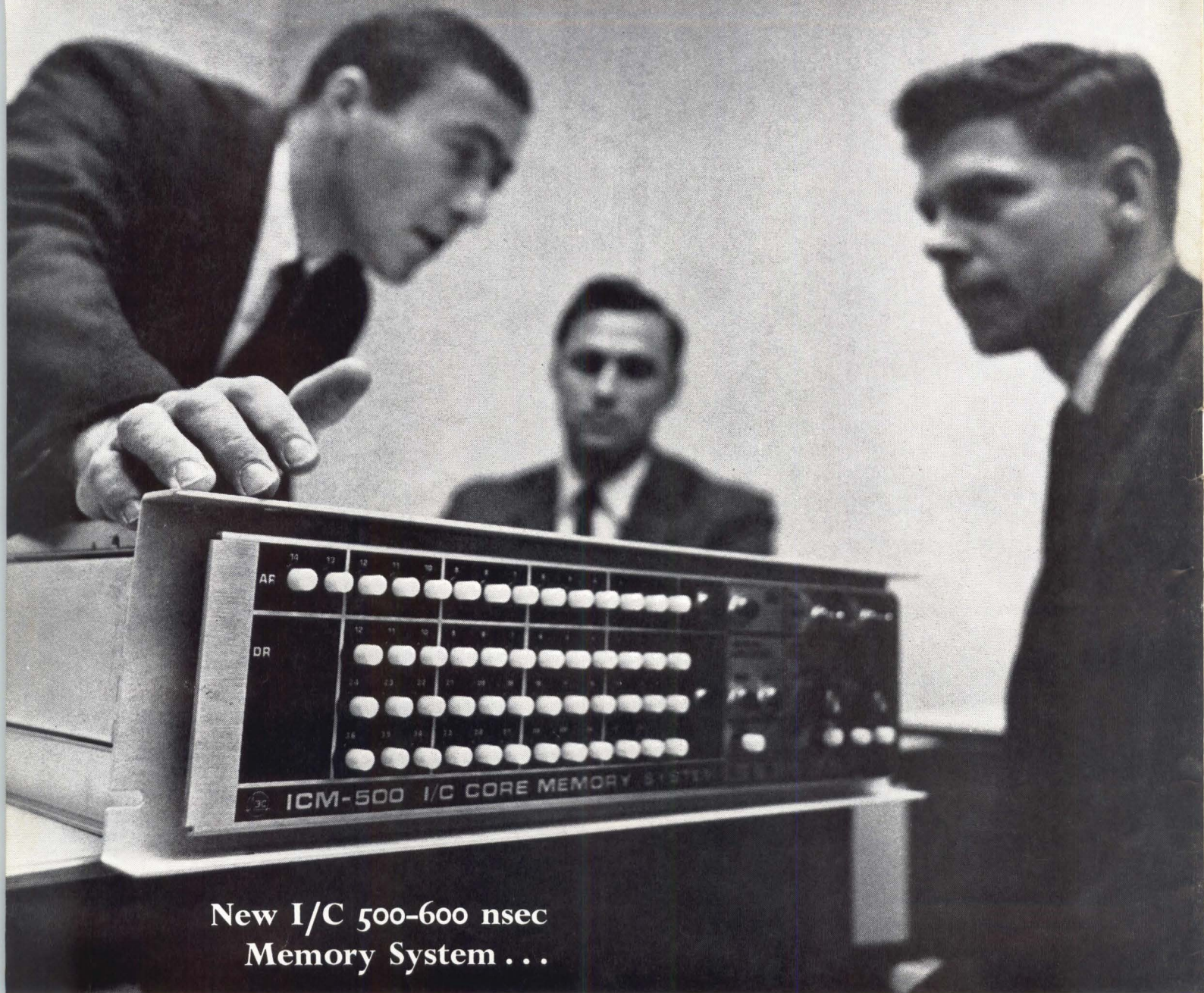
THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

NOVEMBER 1967



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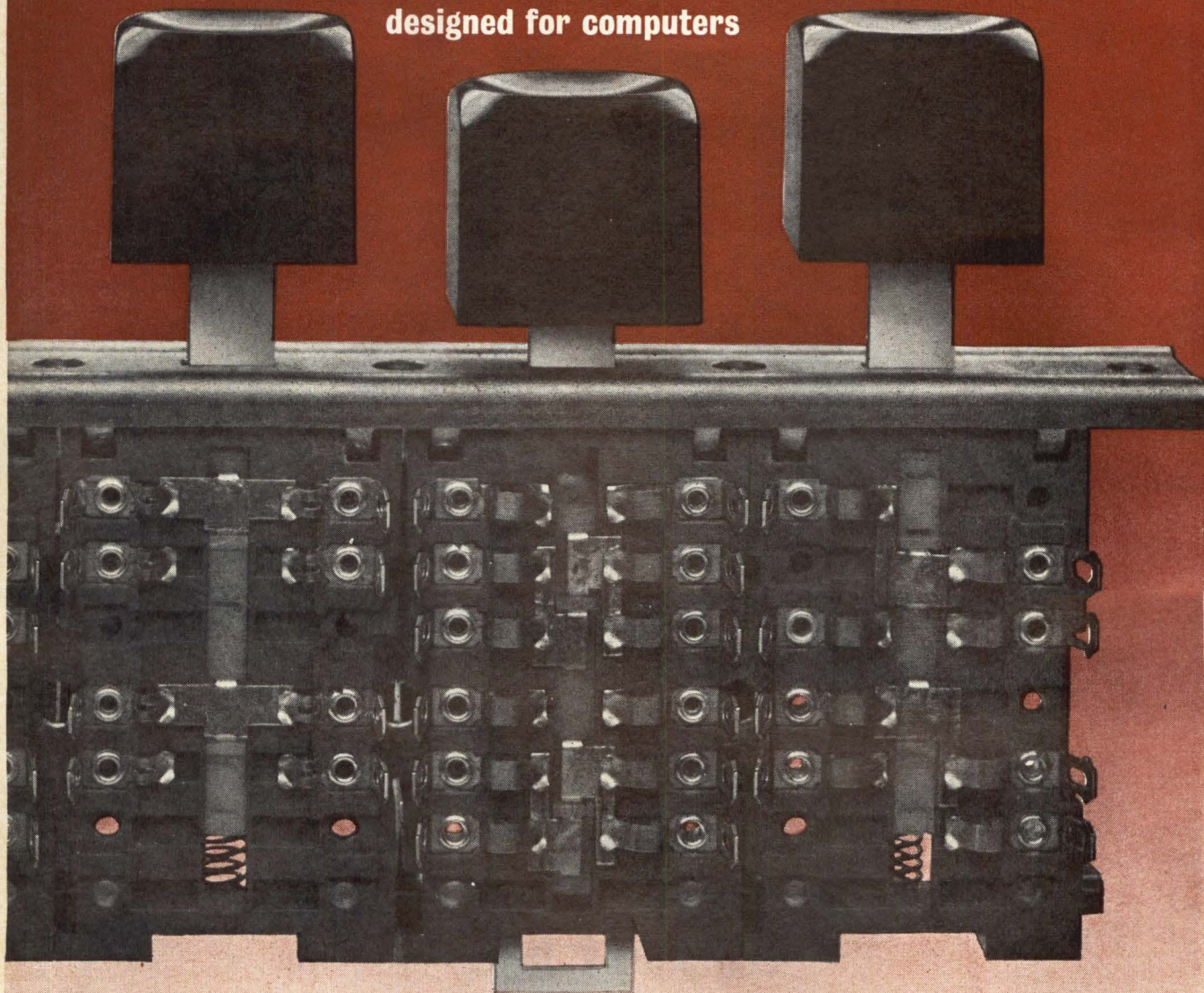
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CIRCLE NO. 1 ON INQUIRY CARD

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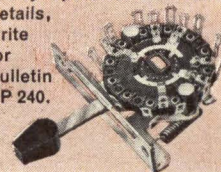
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COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

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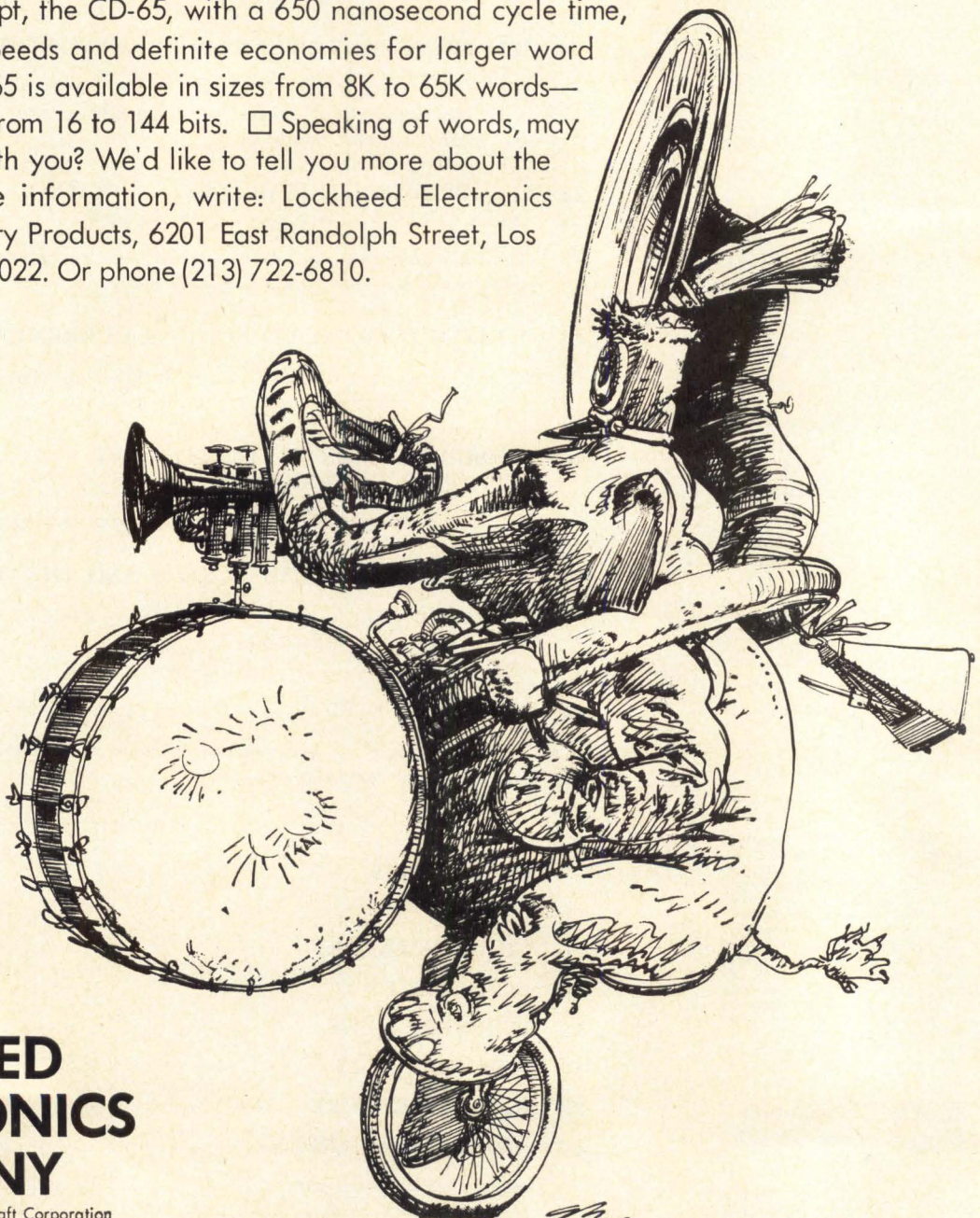
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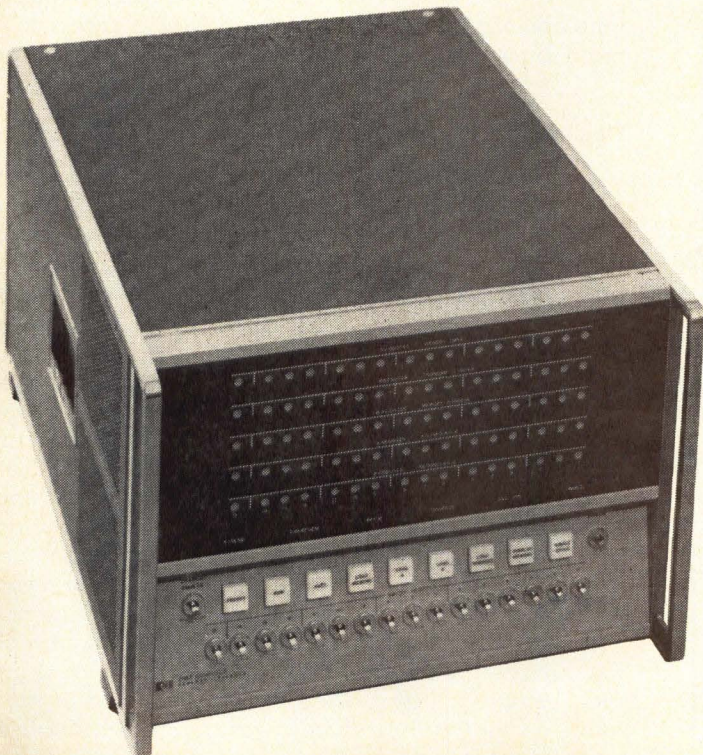


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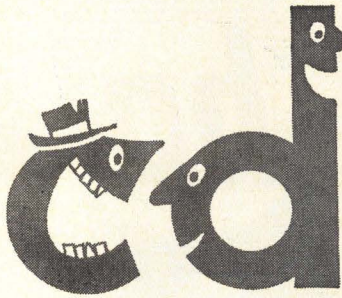
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CIRCLE NO. 5 ON INQUIRY CARD



commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

Effect of Microelectronics On Error Diagnosis

Richard D. Eldred

Hardware Errors Hard To Diagnose

The problems of diagnosis of hardware errors in computers is one which has never really been effectively solved, particularly in those portions of computers that are primarily electronic. Effective, albeit tedious, methods have been developed for producing test programs that will, if painstakingly written, guarantee the detection of an error if it exists. But the problem of producing a program to locate the error, once detected, has not really been satisfactorily solved. This is particularly true in the central processor where the ratio of control logic to data logic is far greater than in data-oriented areas such as memories and input/output units.

The author of this month's CD Commentary, Richard D. Eldred is the Manager of Equipment Analysis Dept. within the Programming Activity at Honeywell, Computer Control Div. He is responsible for test routines, design automation programs, and approving equipment specifications for programming.

The basic problem has been that the test programmer has not had access to the input and output of individual logical functions. He cannot present a test pattern to one or a small number of logical functions and test the output immediately of that small group of functions. Rather, he must first present an input pattern to a very large logical array and then check the output at the end of the array. A recent attempt has been made to do immediate testing, but the total effort involved might be more than most organizations would care to muster, and, as of the moment, the returns are not in as to its degree of success.

Another problem: the field engineer is given increasingly less time for preventive maintenance, and when an error does occur during a customer run, he is under great pressure to get the computer back into condition almost immediately. If the diagnostic procedure is too cumbersome or complicated or time-consuming, he may discard it and resort to a more bushwhacking approach.

Neanderthal Days, Here We Come

If one looks into the future and believes, to whatever degree one wishes, the form of the final implementation of computers using large-scale-integration techniques, one can with a fair degree of seriousness envision a dramatic effect on the diagnostic procedures to be followed, and indeed, a possible return to the Neanderthal days of computers.

The problem of diagnosis obviously revolves around what is the largest replaceable module, since this is the level to which one must diagnose the error. In the beginning of time, the replaceable module, on the average, contained one logical function. This has moved through the five or ten functions per module area and in some recent machines is getting into the fifty to a hundred area. The hypothetical limit is, of course, one module equals one central processor. Even though this may be unrealistic, it should be considered for purposes of argument, since it may be the only case using present methods that will produce a major breakthrough in error diagnosis.

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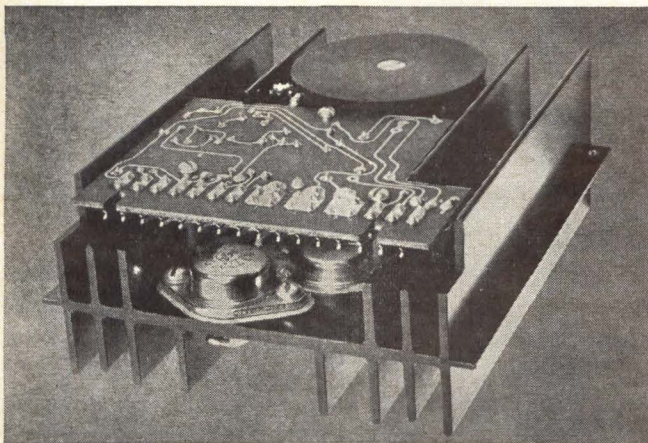
Add-on power capability by using more modules?

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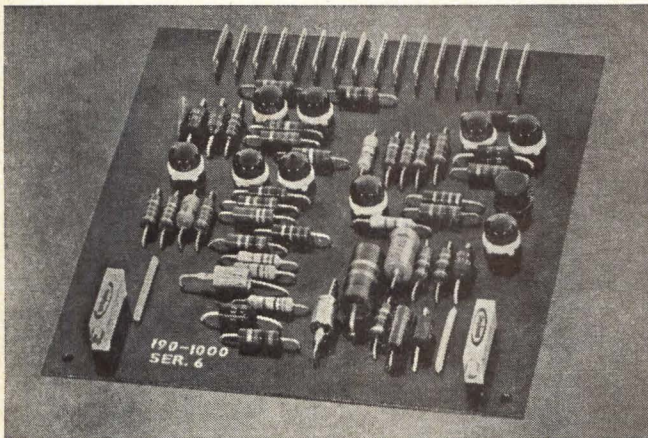
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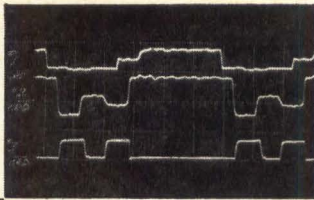
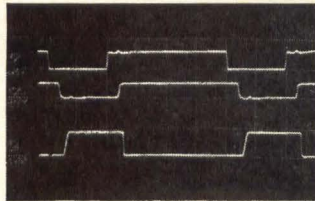
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*Scope photo shows (top) transmitter output into 40-foot twisted pair; (middle) output of line; (bottom) output of gate. Reflections return to transmitter output, produce distortion in line, erroneous pulses at gate output.

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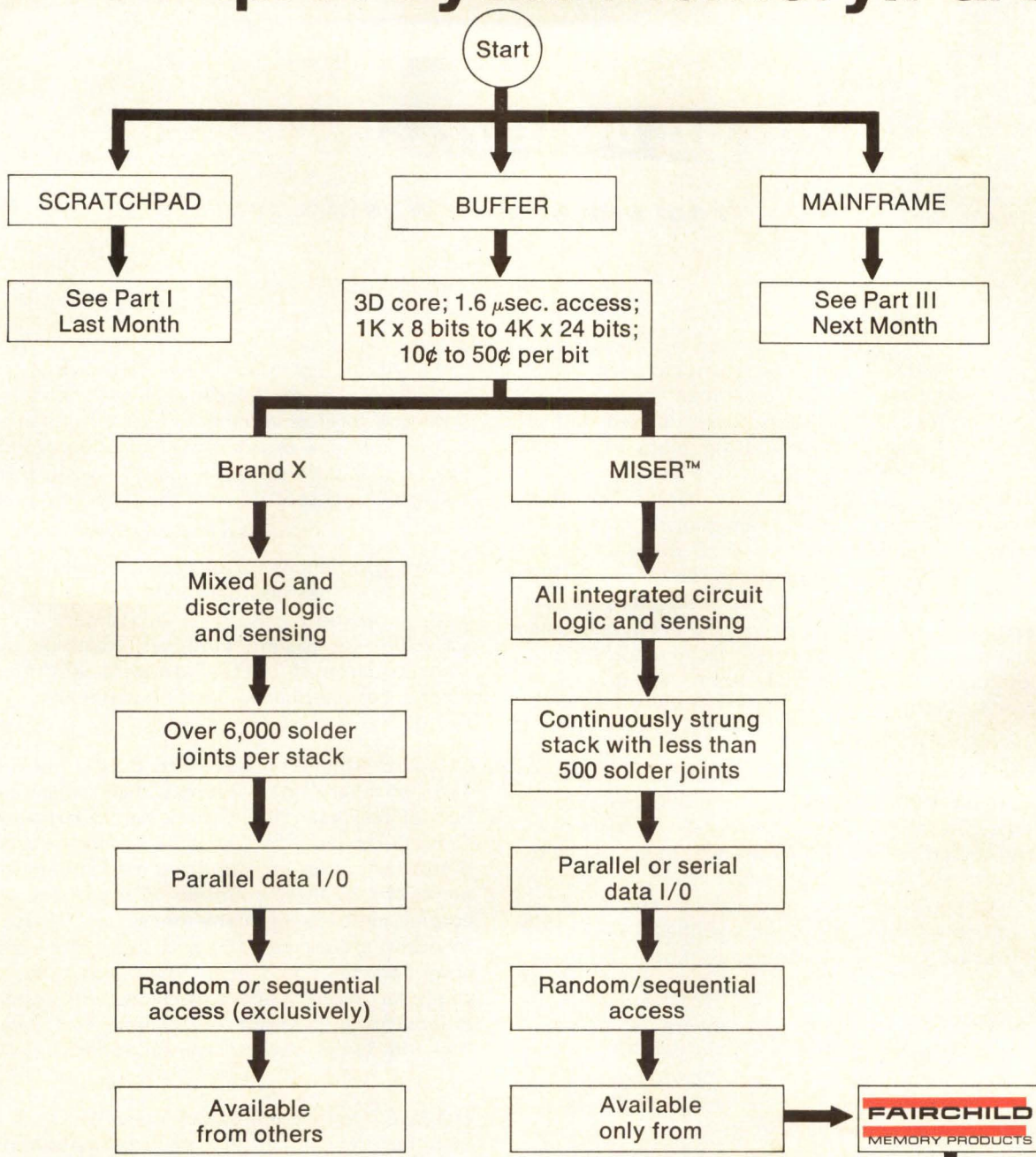
One would think that the more logical functions one can put on a replaceable module and therefore the fewer number of replaceable modules in a computer, the easier the job becomes for the diagnostic programmer to indicate the module that contains the fault, once detected. Unless, however, there has been a strong attempt on the part of the logical designer to partition his logic in a manner that easily allows program access to prime inputs and outputs of each replaceable module, there is no advantage whatsoever to the diagnostic programmer. If there is no strong relationship between the logic on a module and its function in the operation of the computer — such that direct programmable access is provided to prime inputs and outputs either by natural implication of the design or by fairly simple additional circuitry — diagnosis must still be attempted at the gate level. Then, in essence, it must work backwards to determine which replaceable module contains the faulty gate. This is true even to the somewhat ridiculous point where the processor consists of two modules. The problem is not really solved until the extreme case of one module equals one processor is reached, in which case, only a good test or error detection program is needed and the diagnosis consists of replacing the processor.

Whatever Happened To Diagnostic Programmers?

Since I, at least, have little faith in logic designers directing their efforts towards partitioning logic to aid maintainability, other than by company dictum, the chances of large-scale integration helping the diagnostic programmer appear slim. However, if there is a strong effort made towards reducing the number of module types at the same time that more and more components are placed on a module, then it appears that the only problem the diagnostic programmer will have is what he is going to do with his leisure time. If the number of module types becomes small and the total number of modules per processor becomes small, hopefully in the 200 or less area, then the problem is reduced to the level of an untrained homeowner fixing his TV set. Starting in the upper left hand corner he systematically replaces or tests each tube until the set works or he hits the bad tube. Providing a good error-detection program exists, and this can be produced presently, the field engineer can do exactly the same thing. If module types are kept few enough so that backup for each type can be kept on hand, then the replacement method can be used. Since the amount of logic on a module will be large, the test of an individual module obviously can become a problem in itself.

The point, then, is that the module replacement method of error diagnosis which was practiced in the early years of commercial computers — primarily due to customer pressure rather than its incidence of success — may become the recommended procedure for error diagnosis in the future, thereby solving the diagnostic programmer's problem by eliminating it and him.

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Skill requirements for computer manufacturing have been examined by the U. S. Department of Labor. It found that white collar workers make up half of the employment in plants manufacturing electronic computers and about 1 worker in 4 is in a position which usually requires a college degree or its equivalent in experiences. Performance or management of R & D was the primary function of about 60 percent of the scientists and engineers. Labor breaks down the 24.7% of scientists, engineers, and related technicians as follows: engineers 13.7%, mathematicians 3.4%, chemists .4%, physicists .3%, electronic and electrical technicians 4.5%, draftsmen 1.8%, and other technicians .6%. The data refer to 1966.

Computer aided predictions and projections of election results are not now misleading the public, the Senate Commerce Committee has concluded. The Senate group expressed satisfaction in the way networks and broadcasters are taking appropriate steps to clearly label voting projections and predictions, and there is no immediate emergency and no qualified experience to predicate a change in the present system at this time.

The Advisory Commission in Intergovernmental Relations would be authorized to study the feasibility of a computer system to help State and local governments participate more effectively in federally assisted programs under a proposal in Congress sponsored by Sen. Edward Kennedy (D. Mass.). The computer system would, Sen. Kennedy told the Senate, further provide Congress and the President with a better measure of State and local needs and performances under these programs. The system would make use of ADP equipment and other forms of advanced information technology to serve our States and localities. Sen. Kennedy said he had "long been impressed by the enormous potential of computer and information retrieval technology, and its possible application to the development of an intergovernmental information system."

It is imperative that we begin now to plan for the great technological revolution which is almost upon us, Sen. Howard H. Baker, Jr. (R. Tenn.) told the Washington meeting of the Association for Computing Machinery. He urged the creation of a Select Committee of the U. S. Senate for Technology and Human Environ-

ment. According to Sen. Baker "we lack in the Senate, in Congress, in the Executive Branch, and among our State and local governments . . . a mechanism for inquiring into the broad impact of science and technology on man's thinking, his health, work, living habits and individual security over the next fifty years."

License applications for electronic computers, data processing machines and peripherals valued at \$4 million were approved by the U. S. Department of Commerce for export to Eastern European countries during the second quarter of 1967. They were sent principally to Poland, East Germany, and Czechoslovakia.

Computer shipments advanced during the first half of 1967 at a rate nearly double that registered in each half of last year, the Commerce Department reports. "Strong demand for versatile, general-purpose computers in foreign industrialized markets largely reflects the efforts of these countries to modernize their managerial methods in many phases of industrial, commercial, governmental, and scientific operations," according to Commerce. They add, "this country's computer industry offers machines with superior capabilities for high-speed calculations and data transfer and with larger data storage capacities."

The U. S. Department of Commerce believes American manufacturers should find good business opportunities in Britain for desk-top computers and calculators; data-logging devices and other data-gathering equipment; liquid scintillators; x-y plotters; digital voltmeters; visual output devices, and special output printers.

A speedy new IBM 9020 computer is going into operation at the Federal Aviation Administration's Cleveland Air Route Traffic Control Center (ARTCC), permitting more expeditious handling of the increasing number of aircraft in the busy New York-Chicago air corridor. The Cleveland installation's computer is the first to become operational in an FAA center. The agency eventually plans to use this equipment as the central computer complex in all of its ARTCCs. It is a key component in the semi-automated National Airspace System now being developed. Capable of making up to 200,000 calculations a second, the IBM 9020 can

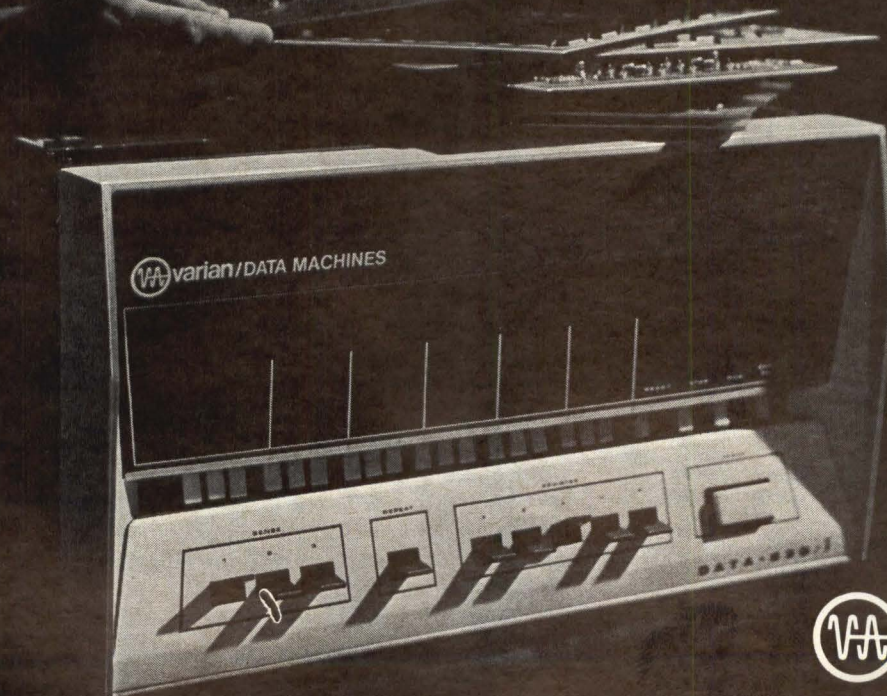
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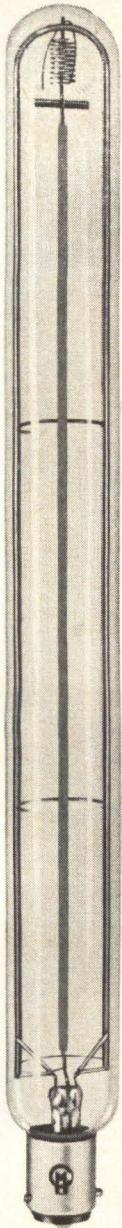
Data 620/i has speed—1.8 microseconds cycle time, arithmetic power—long 16 or 18 bit words and 4K-32K word memories, control and I/O facilities, multi-level priority interrupts, and field-proven software.

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perform some calculations 500 times faster than the equipment it replaces. As currently configured, the new computer can process over 500 flight plans an hour, and this can be expanded as necessary to keep pace with traffic increases. Initially, the computer will be used to relieve controllers of routine clerical and coordination duties such as processing flight data, calculating flight progress and relaying flight plan information. Eventually, as automation of the National Air-space System progresses, even more of the routine, time-consuming clerical flight DP tasks will be accomplished by the computer. It also will be used to detect potentially hazardous traffic conditions and suggest remedial controller actions.

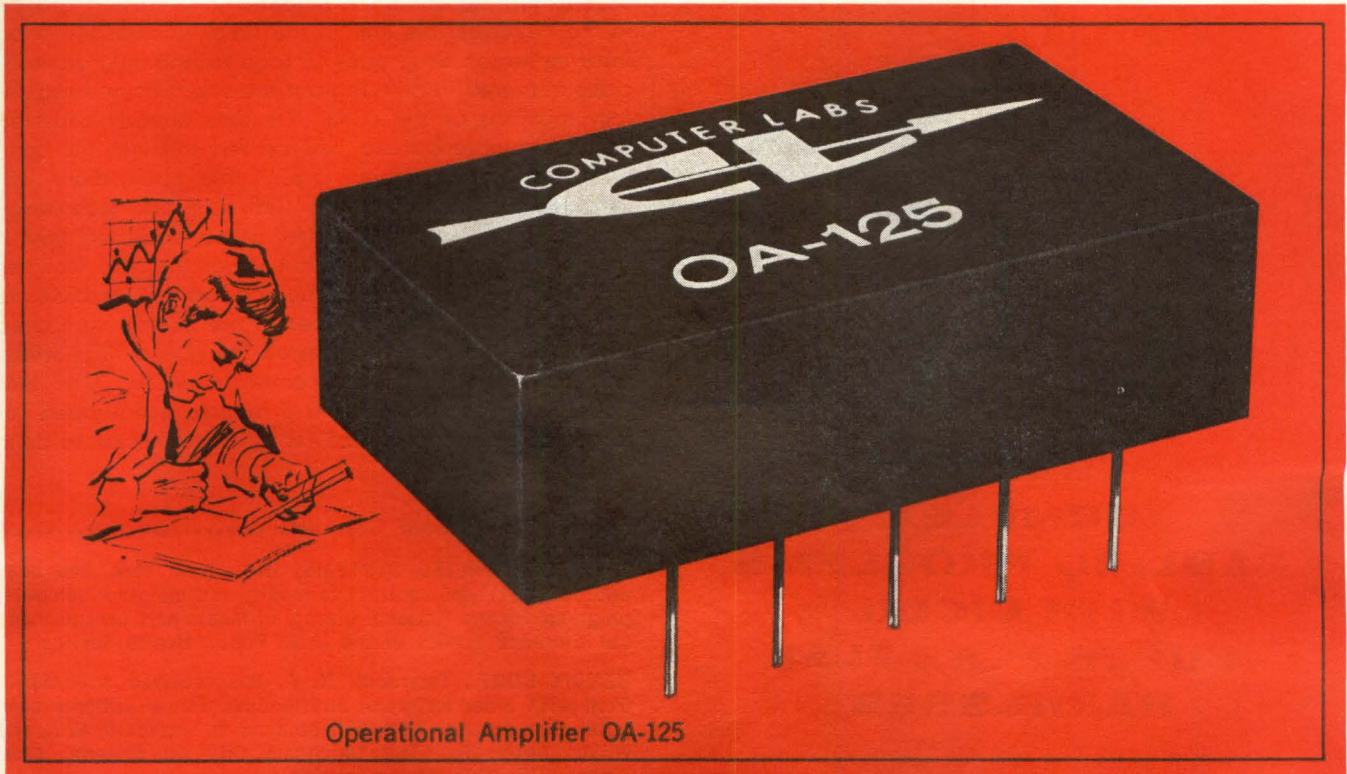
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Computer safety units might eliminate mid-air collisions. The Federal Aviation Administration has before it a plan for an airborne collision avoidance system. Basically, the system, costing \$30,000 to \$50,000 a unit would work like this: Each plane would carry a special digital computer, transmitting and receiving equipment, antennas, and a timekeeping device synchronized to world observatory standards. The planes, one at a time, would send out electronic signals lasting a fraction of a second while all other planes in the area listened. The time taken to complete one such count-off, called an epoch, would be about three seconds, during which as many as 2000 planes would send their positions to each other. Transmission times for each plane would be fixed and known by the computers, which would figure the time between when a signal was sent and when it was received. The computers would use the apparent time difference to calculate an approaching plane's altitude and the rate at which it was drawing closer. When two planes were 60 seconds apart, their pilots would be alerted about the situation, and 20 seconds later, the computers would direct the pilots to maneuver higher or lower to avoid one another.

.....
The National Agricultural Library has asked Control Data Corp. to convert 5,000 herbicide records into machine readable form. CD will have responsibility for modification of the Pesticides Information Center computer programs to accommodate the informational requirements of the Agricultural Research Service in the area of herbicides.

.....
A two-year program for indexing finding aids to archival and manuscript materials by computer is underway at the National Archives and Records Service, a part of the General Services Administration. It is hoped the project will make a significant contribution to the solution of a growing problem in the control of basic research materials. The project calls for major modification and development of existing computer indexing programs in order to take into account the unique nature of source materials in archival and manuscript collections. Tests on more than 25 manuscript and archival collections indicate the feasibility of developing one program that could be used for all collections, and yet allow enough variation for the unique problems of each.

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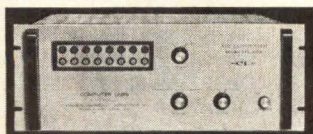
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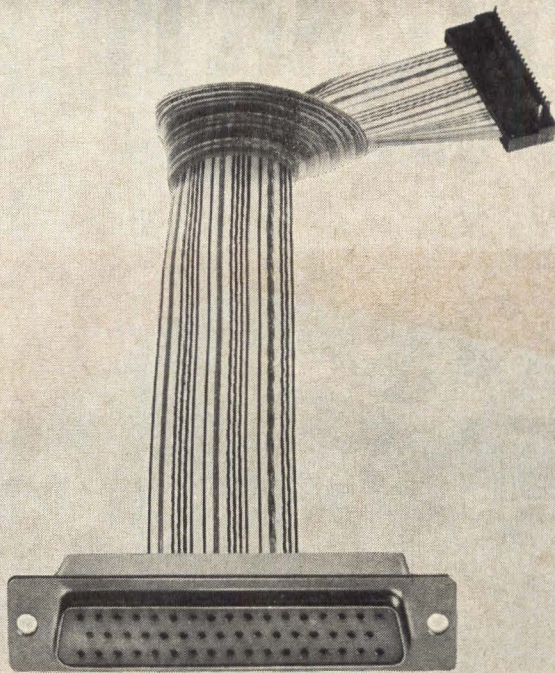


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CIRCLE NO. 12 ON INQUIRY CARD

.....

The Food and Drug Administration, Washington, D. C., has installed an EDP system to serve the entire agency. The facility is the result of five years' work to manage more effectively the storage and retrieval of the great volume of data currently flowing into FDA. The heart of the new system is an IBM 360-30 located in FDA's main headquarters that has been specifically adapted to permit access to files established primarily for one user group by all other potentially interested groups in the headquarters and in the field. Included will be information on drug quality, food technology, or pesticides gathered in carrying out the scientific and regulatory missions of the FDA. The data already collected within a single bureau will be fed through the computer system for agency use. Other applications will be developed as rapidly as staff time and technology permit. The computer system is so designed that it may be connected by lines to each of the field facilities of FDA. Work is now proceeding, on a pilot basis, to link one of the district offices to the central computer. Ultimately it is expected that all the FDA district offices will be connected to the central computer. The IBM 360-30, rented for \$21,000 a month, is equipped for large scale storage of and rapid, direct access to data.

Recent Government Contracts:

BRANDON APPLIED SYSTEMS, INC., New York, has been awarded a \$111,000 contract to modify and maintain computer programs for the National Library of Medicine's central medical reference service of the U. S. Public Health Service.

BENDIX CORP., Teterboro, N. J., has received a \$1,453,783 fixed-price order for repair and modification of airborne computer components. Work will be done at Teterboro, N. J., and Wilkes Barre, Pa. The Oklahoma City Air Materiel Area, Tinker AFB, Okla., is the issuing agency.

GRUMMAN AIRCRAFT ENGINEERING CORP., Bethpage, Long Island, N. Y., has been issued a \$3,000,000 fixed-price letter contract to provide the initial design effort for an improved search radar, a new digital computer system, and a weapons release system in the A-6A aircraft. The Naval Air Systems Command issued the contract.

SPERRY RAND CORP., Long Island City, N. Y., has received a \$4,200,000 letter contract for production of computers to be installed in the subsystem of gunfire control systems. The Naval Ordnance Systems Command is the contracting activity.

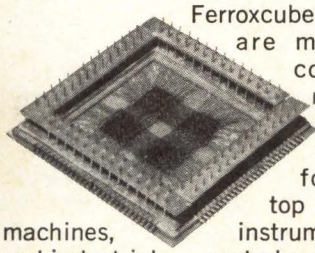
CONTROL DATA CORP., Minneapolis, Minn., has been awarded a \$1,800,000 fixed-price contract to increase the capacity of the basic CD 6400 Computer Systems at the Fleet Numerical Weather Facility, Monterey, Calif. Work will be done at Arden Hills, Minn. The Naval Postgraduate School issued the contract.

CONTROL DATA CORP., Minneapolis, Minn., has been awarded a \$1,750,947 contract order for the rental of automatic data processing equipment at Patrick AFB, Fla. The contract was issued by the Air Force Eastern Test Range Base Procurement Office, Patrick AFB.

LEAR SIEGLER, INC., Grand Rapids, Mich., has been issued a \$1,779,400 initial increment to a \$4,400,000 contract for manufacture of airborne computer components. The Aeronautical Systems Division (Air Force Systems Command), Wright-Patterson AFB, Ohio, is issuing the contract.

RCA, Burlington, Mass., has received a \$2,798,995 initial increment to a \$4,370,000 contract for development of an airborne data automation system. The Electronic Systems Division (Air Force Systems Command), L. G. Hanscom Field, Mass., is the contracting agency.

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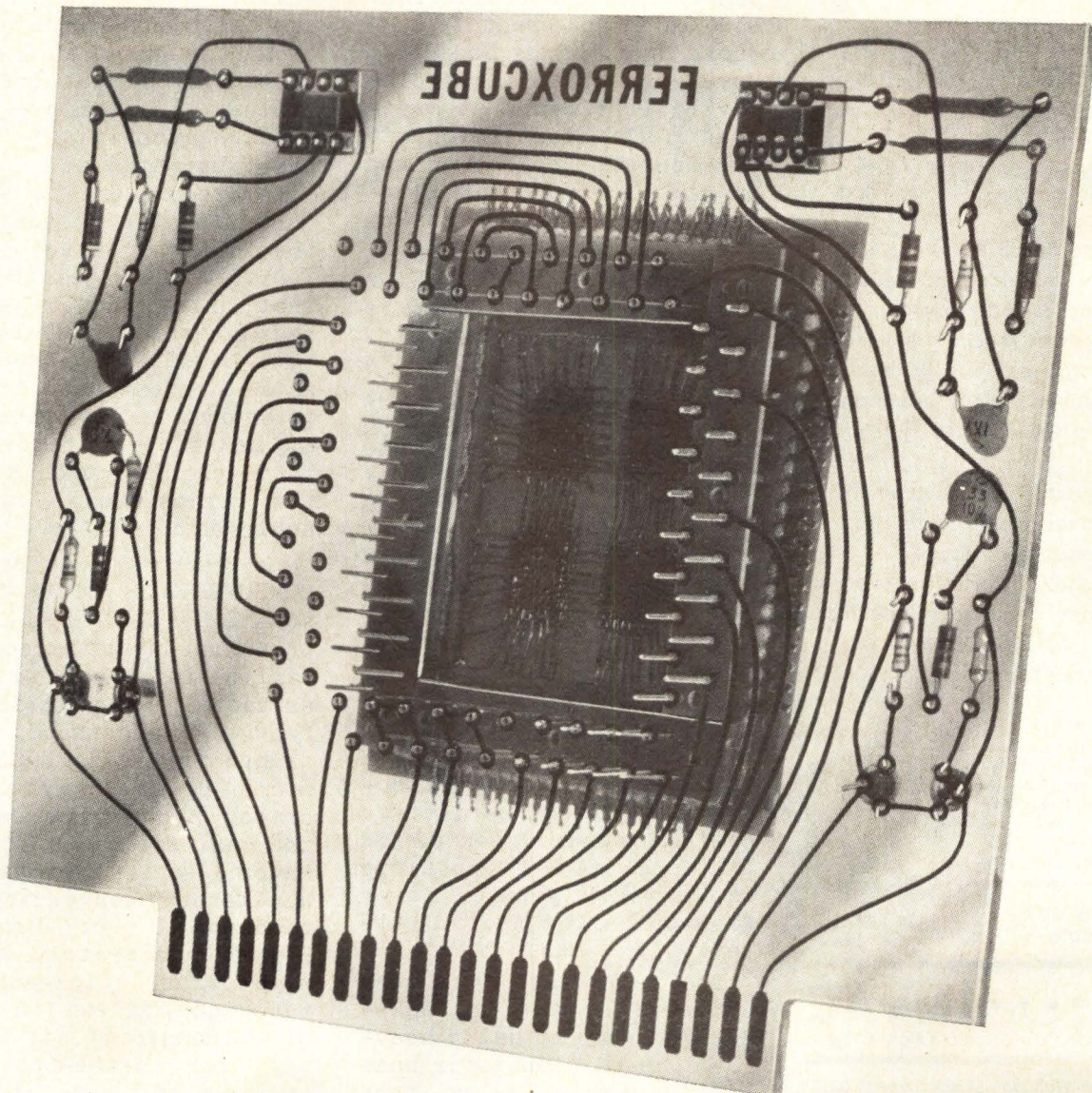
connection pins for quick and simple direct mounting on printed circuit boards. You mount a Platrix as you would a transistor: push the leads through the board and solder. To illustrate, we built this mockup out of clear plastic so you can see both the pins and the Platrix itself.

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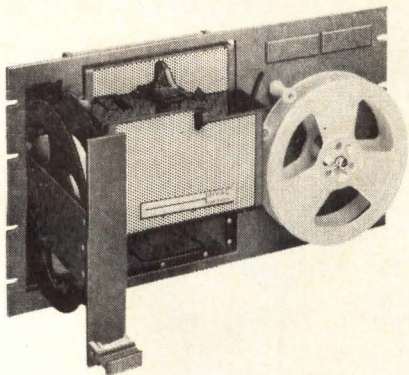
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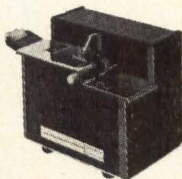
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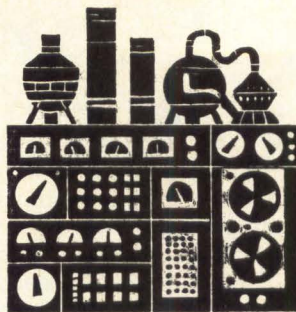


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INDUSTRY NEWS

"WIDE GAP EFFECT" IN TRANSISTORS DEMONSTRATED—Scientists at Carnegie-Mellon University have announced a breakthrough in the design and construction of transistors, which, they say, has the possibility of making these devices ten times more effective. Professor Donald L. Feucht and Arthur G. Milnes, and graduate students D. K. Jadus and H. J. Hovel described their discovery last month at meetings of the Electromechanical Society in Chicago and of the Institute of Electrical and Electronics Engineers in Washington.

Although predicted for several years in electronic theory, the "Wide Gap Effect" has proved impossible to achieve in actual transistors until the successful demonstration by the Carnegie-Mellon team. Perhaps most important of the improvements that may be expected in transistor performance will be increased gain in high frequency ranges; more even distribution of current flow through the device, thus preventing overheating or partial breakdown of the transistor; and improved effectiveness of photo-electric cell action which would, for instance, make it possible to get much greater power from so-called "solar batteries".

The effect has been achieved by the Carnegie-Mellon group by using heavily "doped" transistor base regions, which means that controlled amounts of "impurities" have been introduced into the crystals to

facilitate transfer of electrons through the device. Working with gallium arsenide and zinc selenide layers on germanium, the experimenters kept their laboratory apparatus in a state of surgical cleanliness—only instead of concentrating on germ-free sterility, they managed to keep out any trace of contamination from unwanted chemical elements. It was probably failure to achieve such "clean" conditions which had frustrated all earlier attempts to create structures capable of achieving the wide-gap effect.

Dr. Milnes pointed out that, although the effect has been achieved in laboratory conditions, there remains a great deal of work to be done in the technology of manufacture before effective production of the new transistors can be achieved on a large scale.

.....
COMPUTERIZED VOICES—An ultra-high-speed computer that can convert speech into digital information as fast as the words are spoken was recently announced. Designed and built by Sylvania's Applied Research Laboratory, the system analyzes the basic elements of sound waves, as it performs its accelerated conversion, according to Dr. James E. Storer, laboratory director. The quick-analysis technique, called "fast fourier transform", is necessary for on-the-spot processing of low frequency audio signals, including sonar and speech, into digital data, Dr. Storer says.

Known as the Advanced Computational Processor (ACP), the computer selects only fundamental sound components and by-passes portions which do not destroy the signal if eliminated. Moreover, it allows reduction of the bandwidth necessary to transmit the information digitally. The smaller bandwidth permits simultaneous secure transmission of several signals over a channel that otherwise would handle only one unprocessed message.

Constructed entirely of integrated circuitry, the device is said to perform an average computation in one three-millionth of a second, about five times faster than digital equipment now employed for this purpose. According to Dr. Storer, "digital models currently in operation are unable to attain circulation rates necessary to computerize signals without a delay in processing; only complex, special-purpose analog circuitry previously has analyzed sound at input speeds."

The fast computation rate of the ACP is said to be due principally to its integrated circuit memory element, which replaces the slower, conventional core storage. In addition to its increased speed, the ACP, as a digital computer, has built-in versatility. It takes instructions from relatively uncomplicated programming rather than requiring separate wiring or specialized equipment for each of its jobs as does the analog process.

.....

FIRST POSITIVE ISOTOPE EFFECT DISPLAYED BY SUPERCONDUCTING URANIUM—In the current issue of "Physical Review Letters," Dr. Robert Fowler and co-workers at the Los Alamos Scientific Laboratory, New Mexico have reported the first positive isotope effect. The physi-



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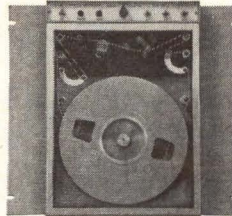
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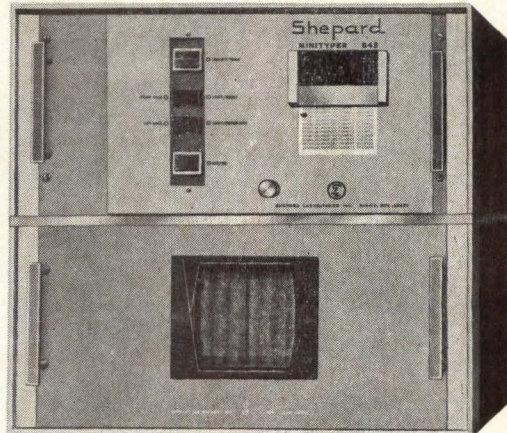
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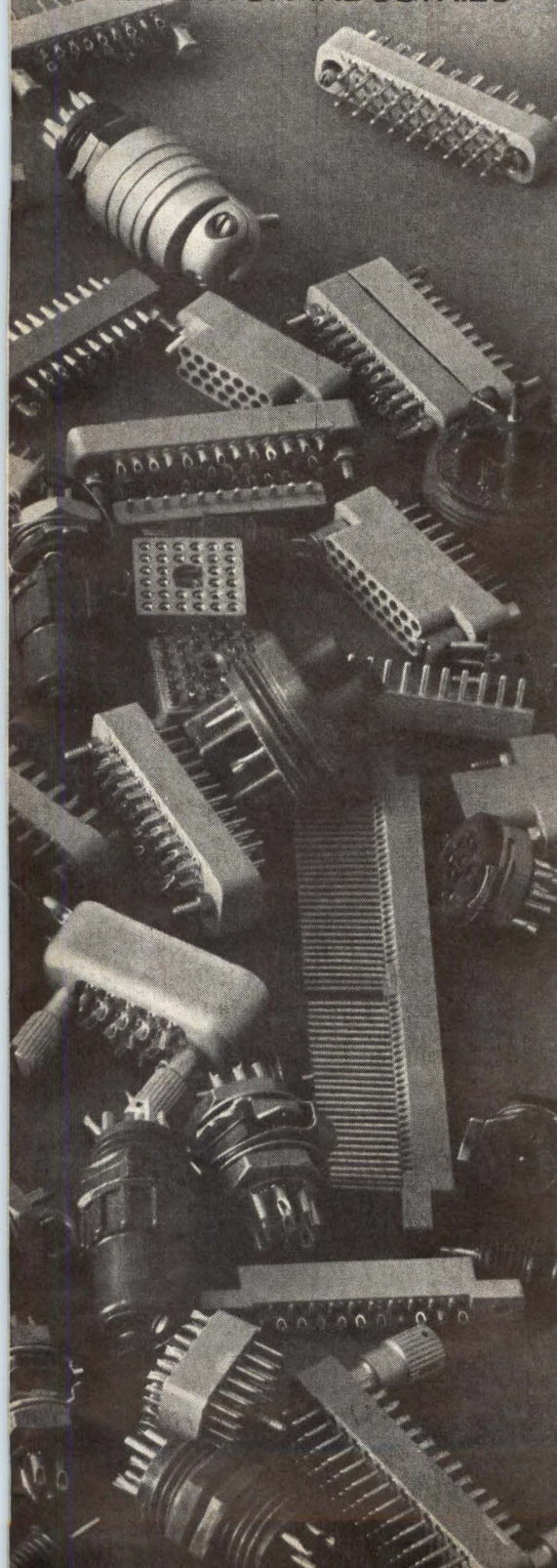
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cists are of the opinion that their work is "final proof" that the phonon-electron theory of superconductivity is inadequate.

Theoretical physicists have had difficulty explaining the strange behavior of superconductors since they were first observed in 1911. In fact, a satisfactory explanation was not formulated until 1957.

The current theory, called the BCS theory, explains superconductivity in terms of phonons (heat units) and electrons. BCS stands for the authors of the theory John Bardeen, Leon Cooper, and J. R. Schrieffer. Since its birth in 1957, the BCS theory has encountered new trouble each year.

One problem is that the theory implies that the critical temperature—the temperature at which a substance becomes superconducting—should be lower for the heavier isotope of a substance. This relationship between critical temperature and isotope mass is known as the negative isotope effect. It has been observed for a number of substances, but in several cases the temperature was not as low as the theory predicted.

Dr. Fowler's group began studying isotopes of uranium as a further check on the theory. They have measured critical temperatures for uranium-235 and its heavier isotope, uranium-238.

Samples of high-purity uranium were cooled below 2.5° Kelvin (degrees centigrade above absolute zero) with liquid helium. Although trace contaminants in the samples made precision difficult, there was no doubt that in every case U-235 had a lower critical temperature than U-238. These results constitute a positive isotope effect, a phenomenon that had not been observed previously.

On the basis of other work with critical temperatures, the Los Alamos physicists had expected the positive isotope effect. The results, although somewhat higher than they had anticipated, confirmed their expectations.

"Physical Review Letters" is published by The American Physical Society.

.....
COMPUTER DESIGNED MULTI-LAYER CIRCUIT BOARDS—Production-proven computer programs and processing techniques for designing and fabricating multi-layer circuit boards for subsystems was recently announced by the Systems Division of Librascope Group, General Precision Systems Inc. According to J. L. Deitz, Chief Engineer, the programs and processing techniques are perfected, and have been effective in reducing design time and costs in producing circuit boards for various applications.

Librascope is now making the programs and techniques available to the general electronic industry. Mr. Dietz says they are ideal for prototype, short run, or large-scale production programs requiring fast-reaction design and fabrication of functional subsystems.

The technique, long used at Librascope, employs a computer programmed to process schematics or logic equations. The computer controls an X-Y plotter which automatically produces the art work for printed circuit board masters. Librascope is successfully using the process for designing and producing up to 12-layer multi-layer boards. Additional computer proven, production proven, also provide wire lists, parts lists, maintenance documentation and tapes for automatic hole drilling. These too are said to offer great savings in time, design, and documentation costs.

Please don't call EMR's 6130 Computer

s m a l l



If you think the *ADVANCE* 6130 computer from EMR is just another "little" computer, take a closer look. You could be fooled by the price—low enough to compete with any small machine—or by the 16-bit word length, characteristic of small-scale systems. But that's where the comparison ends.

Analyze the 6130 and you'll realize it's the most productive system available. The instruction repertoire and internal architecture put it in a class by itself.

SMALL SCALE

To the potential buyer of a small-scale computer, there are a number of capable machines which are available to "do the job." However, aren't you looking for a system that can "do the job—plus"? The plus being able to expand to accommodate your next requirement. Many of the small-scale computers (under \$35,000) that are being sold cannot provide the user with any realistic approach to expansion.

The 6130 is in a different class, it is designed for expansion. With the 6130 you can add a second processor easily, with no operational software problems. This additional processing power is relatively inexpensive when compared to installing larger systems.

This built-in capability for growth insures that you won't be looking for another new system next year and have to face the re-programming problem.

HIGH PRODUCTIVITY

Next, how about the buyer who has a problem that actually requires a large-scale machine, but does not

have the funds? The 6130 has a capability that stretches into this high-productivity market.

Historically in the computer field, the user's main problem is to justify a large financial investment to his management. Once the computer is installed, and the user can demonstrate to management what can be accomplished, he can build a good argument for expansion. The expansion is normally in the way of adding more peripheral equipment and additional core memory. This is further indicative that, with the large-scale approach, the user has started out with more "computer-power" than needed—and is paying for features that he cannot use or can do without. As the load increases, a point is reached where he has all of the options that use the software to the limit, but by that time, he runs out of "computer-power."

In the case of the *ADVANCE* 6130, the high-productivity user may run out of computer-power sooner but would be in a position to add another 6130 processor to immediately increase his computer power at a small financial addition. One 6130 can handle background processing while the second handles preprocessing and input/output. If this would not be an acceptable approach, a more powerful processor could be added and the 6130 retained as a satellite.

The 6130 alone can successfully offer this approach as competitive

small computers are just not powerful enough to handle the general purpose requirements.

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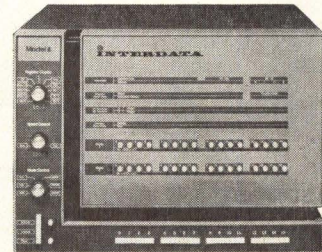
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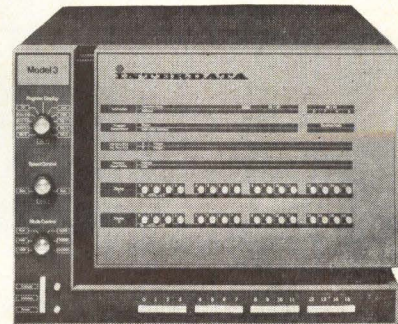
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- 1.8 μ s memory cycle time

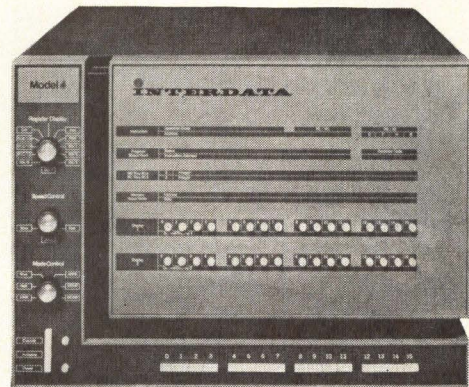


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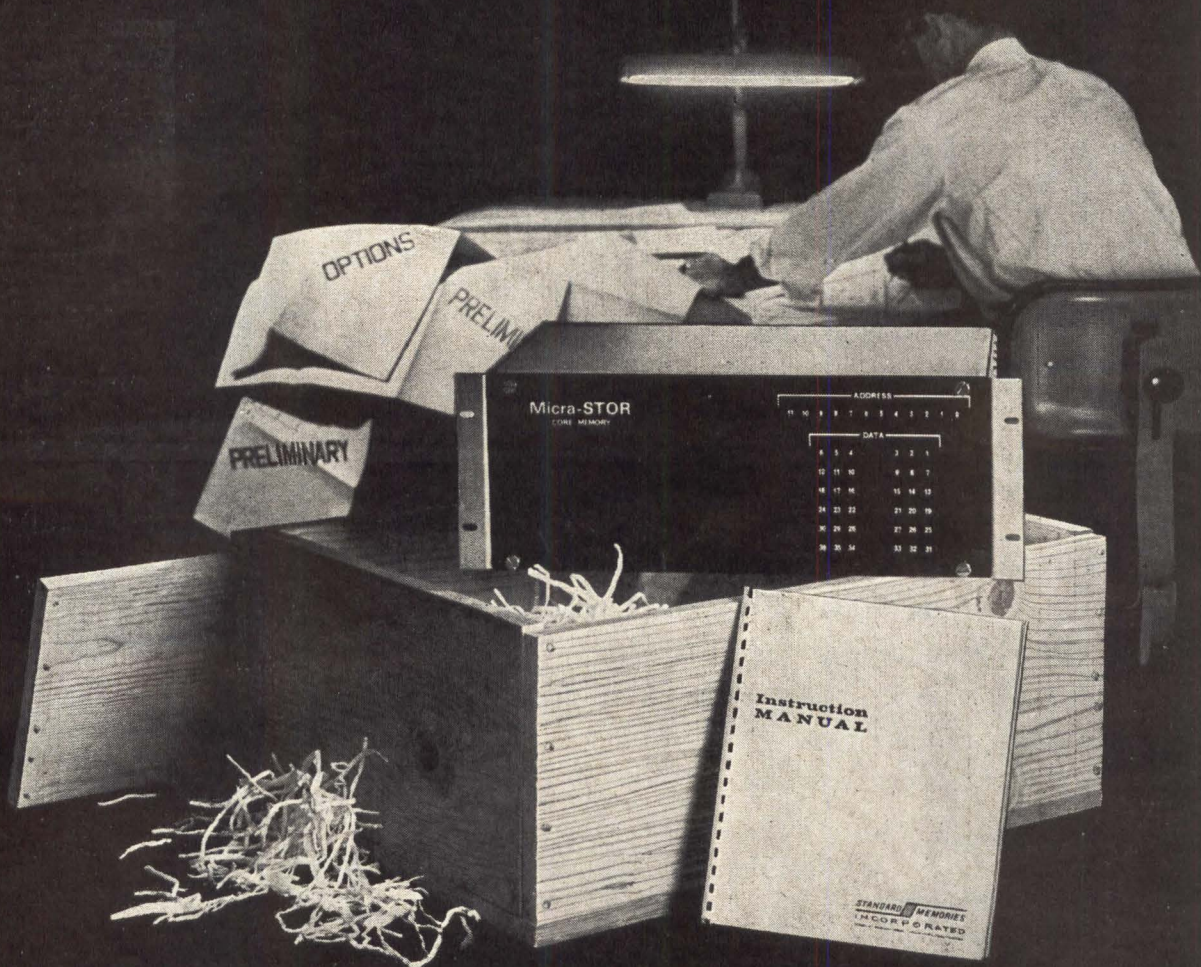
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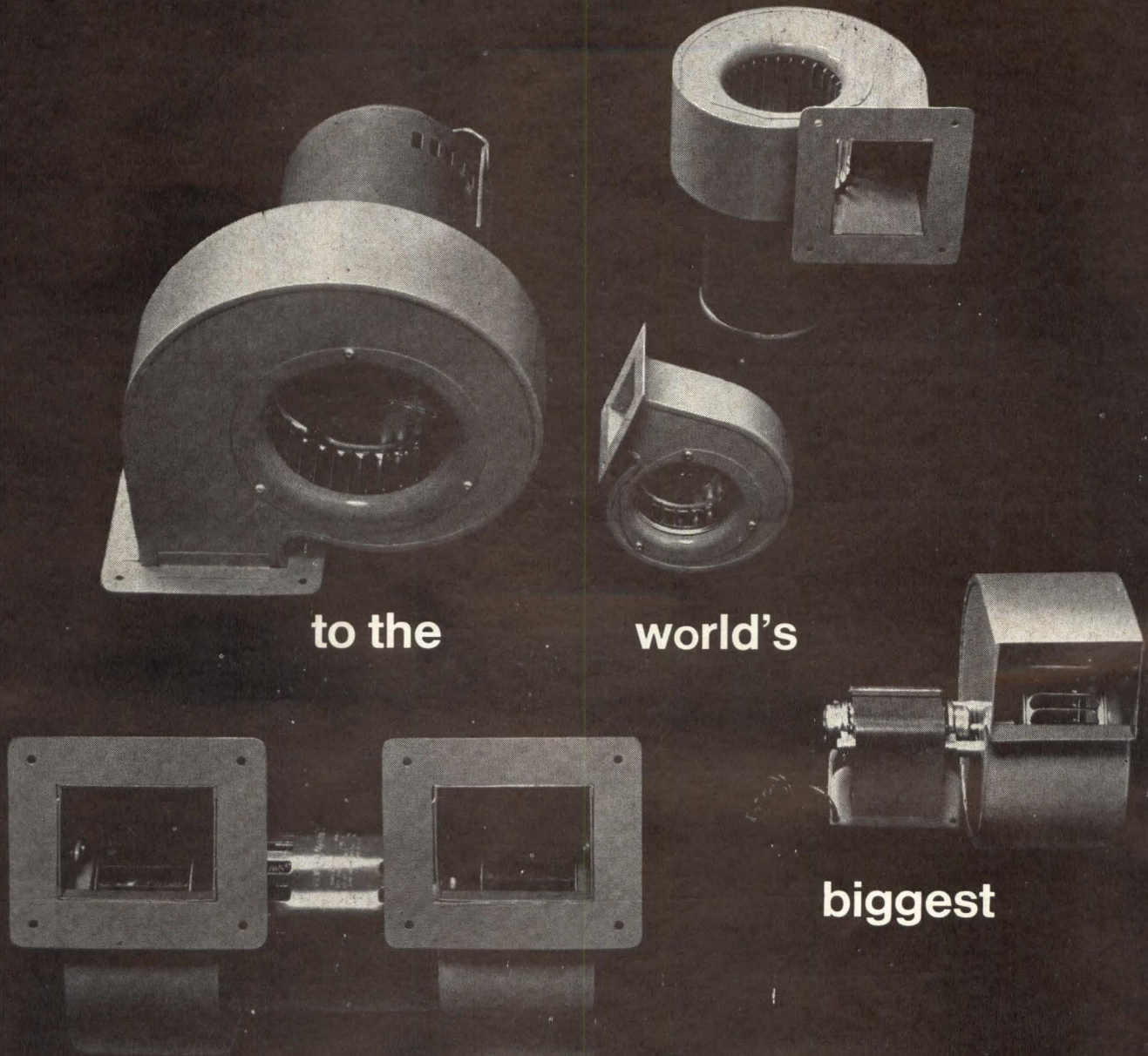
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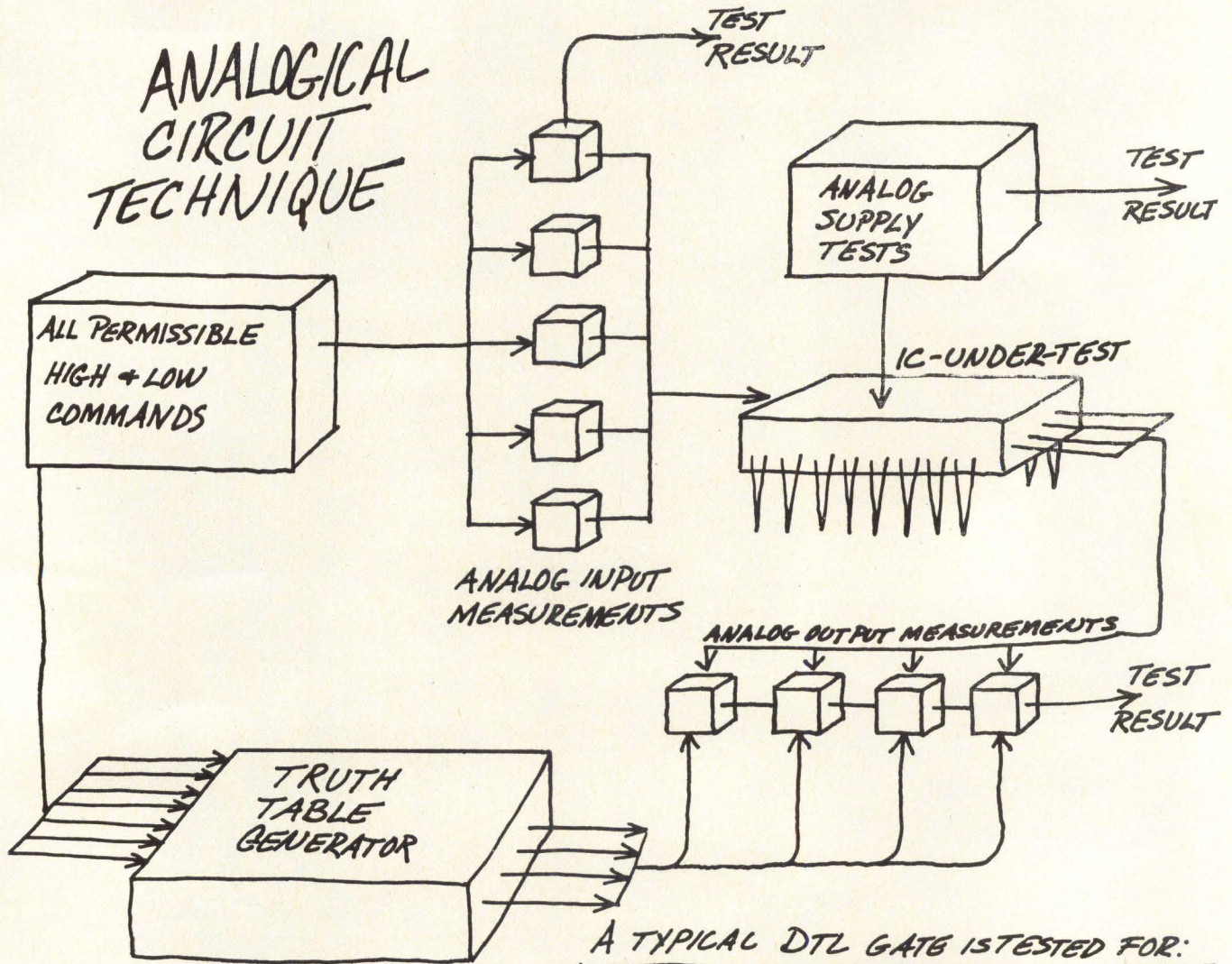
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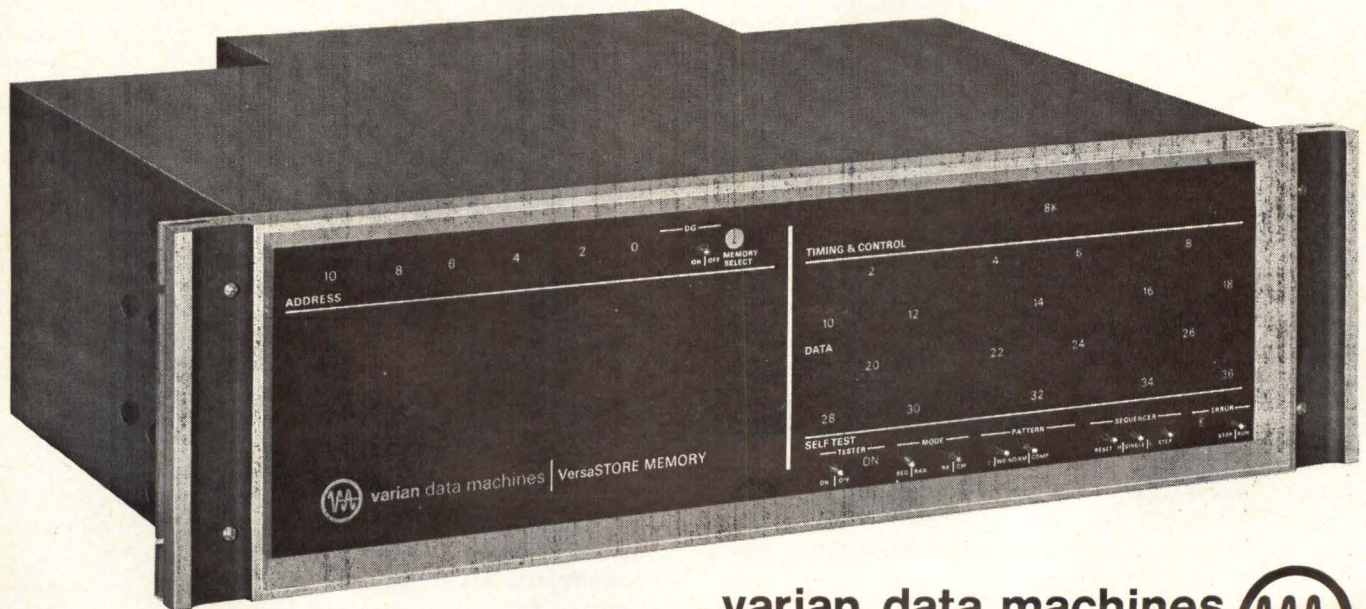
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CIRCLE NO. 23 ON INQUIRY CARD

DIGITAL DATA TRANSMISSION

G. P. Hyatt, Head, Computer Design Advanced System Division,
Teledyne System Company, Hawthorne, California

Synchronous data transmission results in higher speed operation and hardware economy, by eliminating resynchronizing hardware and delays. Synchronous techniques require special propagation delay and clock pulse skew considerations. Signal degradation is also a factor. Selection of the proper transmission cable, line drivers, and line receivers minimizes potential problem areas. Clock pulse fanout and transmission line routing contribute to hazard free operation.

Digital data transmission is accomplished on macroscopic and microscopic levels; data transmission between spacecraft and the earth over millions of miles of space and data transmission between logic functions on a single integrated circuit substrate illustrate these extremes. This article describes a range of digital data transmission that will permit synchronous transmission and operation. This range is characterized by the primary constraint that the complete path propagation delay must be less than the clock period, covering a range from the microscopic to the intermediate length transmission line. Of particular interest is the intermediate length transmission, which will permit synchronous communication for high data rates over short distances (10 mc clock and 25 feet) or low data rates over long distances (10 kc and 5 miles). A second constraint, that the clock pulse propagate to all flip-flops prior to the data change propagation, will eliminate critical races associated with a large clock pulse skew condition.

The synchronous data transmission technique will result in hardware economy and speed advantages when compared to an asynchronous digital communication link.

Communication within a centralized system is the trivial case of asynchronous data communication, while communication between a central unit and various remote units is the generalized case. A baseline system will be described to illustrate the important considerations, using synchronous design techniques within each unit and between units. A system that deviates from the primary constraint, where the propagation delays can exceed the clock pulse period, will require different design considerations involving asynchronous transmission of data between the various units, necessitating extra hardware. The baseline system is shown in functional form in Fig. 1, with characteristics listed in Table 1. The central unit will transmit the synchronizing clock pulses and digital data to the remote units, while the remote units will transmit synchronous digital data to the central unit and other remote units. All data trans-

mission is synchronized with the central unit clock pulses. The transmission propagation delays are shown as D for the data lines and δ for the clock lines.

Transmission of digital data involves design considerations pertaining to signal degradation, propagation delays, and clock pulses skew affects. Sub-categories involve impedance matching and waveform restoration considerations. A detailed description of these considerations and the resultant hardware implementation will be presented.

Signal Degradation

Transmission of digital data on long transmission lines results in degradation of the signal waveform, as a function of the characteristics and length of the transmission line. There are two predominating signal degradation mechanisms, defined as the frequency insensitive and frequency sensitive degradation affects.

The frequency insensitive degradation of the digital signals are termed the attenuation characteristic of the transmission line, and are primarily caused by the resistance in the non-ideal conductor. (When projected to higher frequencies in the hundred megacycle region, the "skin effect" will tend to produce a slightly frequency-sensitive attenuation characteristic, but in the low megacycle frequency region, the "skin effect" is not significant and the attenuation will be relatively frequency insensitive. The attenuation characteristic of the baseline transmission line is listed in Table 2, where the attenuation at 400 mcps is approximately 10 db per 100 feet and the attenuation at one megacycle is approximately 2 db per 100 feet. In the neighborhood of several megacycles and below, the attenuation parameter is virtually constant.)

The attenuation characteristic of the transmission line will degrade the amplitude of the digital data without significantly affecting the shape of the digital pulse. The relationship between attenuation and voltage amplitude

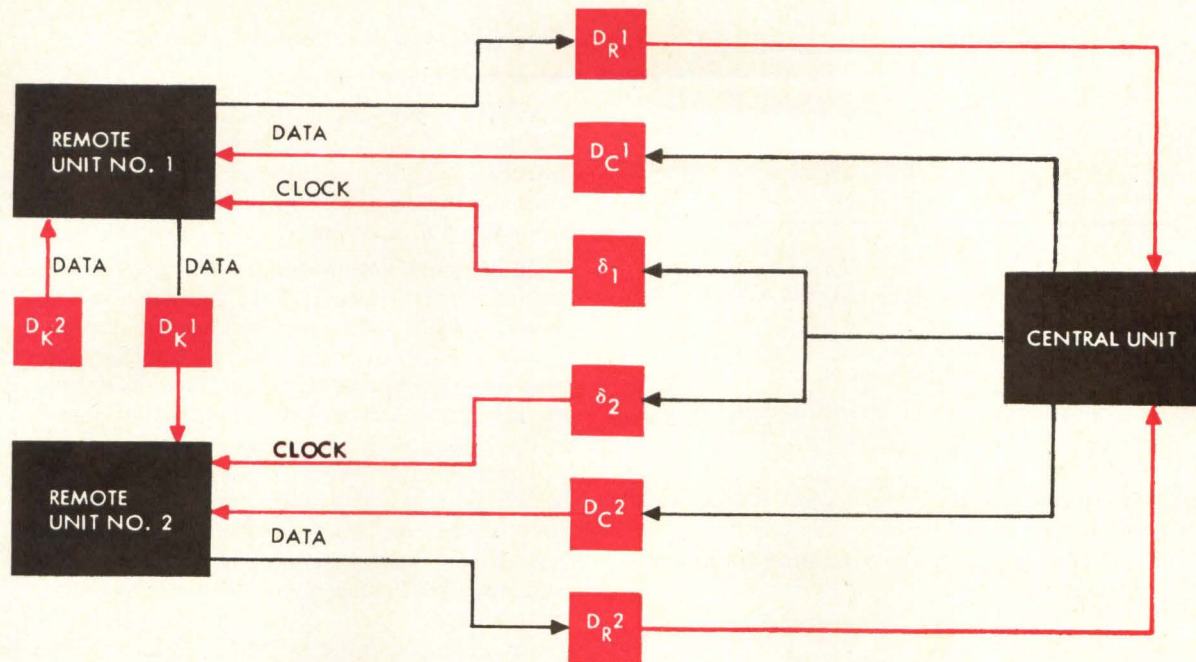


Fig. 1. Data flow functional diagram

degradation is illustrated in Equation 1, while the total attenuation for a 250 foot transmission line is calculated in Equation 2.

$$\text{Attenuation} \equiv 20 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right) \text{ db} \quad (\text{Eq. 1})$$

$$\text{Attenuation} = (-2 \text{ db}/100 \text{ ft.}) (250 \text{ ft.}) = -5 \text{ db} \quad (\text{Eq. 2})$$

Substituting Equation 2 into Equation 1 yields:

$$\text{Attenuation} = 20 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right) = -5 \text{ db} \quad (\text{Eq. 3})$$

$$V_{\text{out}} = \frac{V_{\text{in}}}{10^{0.25}} \approx 0.6 V_{\text{in}} \quad (\text{Eq. 4})$$

Therefore, the pulse amplitude at the remote end of the transmission line will be attenuated to approximately 60% of the amplitude of the original pulse. This amplitude degradation will necessitate line drivers and line receivers to permit the restoration of the pulse amplitude for proper operation of the digital equipment.

The frequency sensitive degradation of the digital pulses is primarily caused by the capacitance associated with the transmission line. This capacitance is listed in Table 2 as 13 pf per foot. The total line capacitance for a 250 foot transmission line is, therefore, 3250 pf. A Fourier analysis of the digital pulse will illustrate that the higher frequency components result in the sharp rise and fall times, therefore the relatively greater attenuation of the higher frequency components will cause a larger degradation of the leading and trailing edges than of the peak pulse amplitude, resulting in more of a degradation of pulse shape than of pulse amplitude.

The capacitance parameter of the transmission line is distributed along the line length, but a good approxima-

tion of the frequency sensitive degradation can be obtained by assuming a lumped parameter transmission line, illustrated in Fig. 2. This lumped parameter equivalent transmission line schematic describes a voltage divider network with the characteristic impedance (Z_o) and capacitive impedance (Z_c) of the line forming the voltage divider. The characteristic impedance is relatively constant, independent of frequency, line length, and other parameters. The capacitive impedance parameter decreases with increased line length and frequency; therefore, the output signal amplitude is inversely proportional to the line length and the frequency of the Fourier frequency component. The capacitive impedance for the fundamental frequency component of the pulse is calculated in Equation 5.

$$Z_c = 1/(2\pi fc) = 1/[(2\pi) (10^6) (0.325 \times 10^{-8})] = 50 \Omega \quad (\text{Eq. 5})$$

Table 1. Baseline System Considerations

Clock Rate	1 mcps
Transmission Line Length (max)	250 feet
Rise-Fall Time	20 ns

Table 2. Transmission Line Characteristics

Brand-Rex Coaxial Cable	T-267
Characteristic Impedance	95 Ω
Capacitance	13 pf/ft
Attenuation at 400 mc	10 db/100 ft
Attenuation at 1 mc	2 db/100 ft
Propagation Velocity	80%

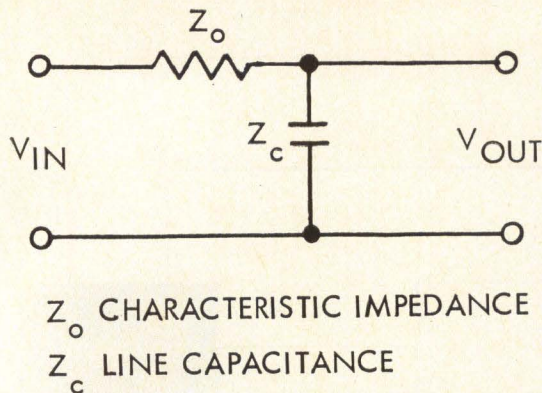


Fig. 2. Lumped parameter transmission line

The frequency sensitive degradation for the fundamental frequency component of the pulse is calculated in Equation 6 with respect to the lumped parameter approximation, illustrated in Fig. 2.

$$\frac{V_{out}}{V_{in}} = \frac{Z_c}{Z_c + Z_o} = \frac{50}{50 + 95} = 0.34 \quad (\text{Eq. 6a})$$

$$V_{out} = 0.34 V_{in} \quad (\text{Eq. 6b})$$

Therefore, the output amplitude of the fundamental frequency component is 34% of the input pulse amplitude. Under the assumption that a sharp leading edge can be obtained with a ten megacycle Fourier frequency component, the leading edge will be degraded to an amplitude 5% of the fundamental amplitude. This frequency sensitive degradation of the pulse results in a pulse shape that is significantly rounded at the edge with poor rise and fall times.

The total degradation of the peak amplitude of each pulse is proportional to the attenuation and frequency sensitive degradation of the pulse. The output pulse amplitude is calculated in Equation 7.

$$\text{Degradation} = \frac{V_{out}}{V_{in}} \approx (0.6) (0.34) = 0.2 \quad (\text{Eq. 7a})$$

$$V_{out} = 0.2 V_{in} \quad (\text{Eq. 7b})$$

The pulse degradation is illustrated in Fig. 3, with an input pulse of unity amplitude and sharp edges and an output pulse reduced to 20% amplitude with degraded edges.

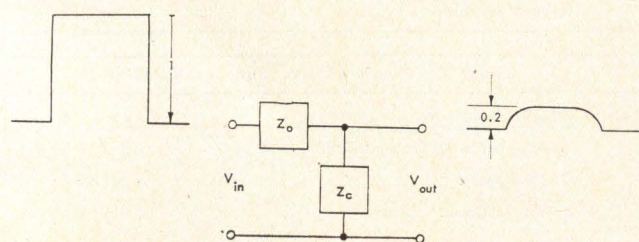


Fig. 3. Pulse degradation

Propagation Delay Considerations

Propagation delay of digital pulses is generally caused by the delay through logic functions, determined by switching speed of the logic, and the delay through interconnections, determined by the velocity of propagation through the medium and settling of the signal due to impedance mismatches.

Interconnections in electronic systems are often treated as simple conductors. This approach is valid only in relatively slow speed, small dimensional systems. In applications with clock periods that approach the transmission propagation delays, the interconnections must be considered as transmission lines. High speed switching of the digital logic can introduce Fourier frequency components in the hundred megacycle frequency range, which is in the low radar band. Much of the theory associated with electromagnetic fields and waves as applied to radar systems is directly applicable to these systems. The criterion for the treatment of interconnections as either conductors or transmission lines is based upon a comparison of the clock periods and transmission propagation delays. If the propagation delay down a line is in the order of magnitude of the clock period, the interconnections should be treated as transmission lines. An electrical signal will propagate at approximately one foot per nanosecond for a nominal permittivity (ϵ) and permeability (μ) of the surrounding median. A transmitted signal will propagate along a line to an impedance mismatch interface, where a portion of the energy will be reflected. This reflection will propagate down the line in the reverse direction to another impedance mismatch interface, being reflected back and forth until the signal in the line stabilizes at the excitation level. The number of reflections that will occur prior to the signal stabilizing at an acceptable level is a function of the impedance mismatch. For larger mismatches, a larger number of reflections will occur prior to stabilization. For long transmission lines or lower propagation velocities, the delay for each reflection will be longer. Therefore, the propagation delay through a wire is a function of the impedance mismatch in addition to the line length and propagation velocity.

For short lines and relatively long clock periods, successive reflections will stabilize in a relatively short period compared to the clock period. For long interconnections or fast clock rates, line stabilization periods may become significant. Relatively long interconnections can be better tolerated if impedance matching is implemented. Integrated circuits typically contain a low output impedance and a relatively high input impedance to enhance noise immunity and fan-out. The transmission line selected for the baseline system has a low characteristic impedance, as listed in Table 2. This value provides a good impedance match with typical line driver output impedances, but provides a moderate impedance mismatch with typical line receiver input impedances. Impedance matching should generally be accomplished by adding terminating resistors to the high impedance end of long interconnections to minimize reflections and the resulting propagation delays. Pulse transformer techniques can also be used to satisfy the impedance matching considerations, but with a slightly higher hardware complexity than with resistive termination.

The propagation velocity of the transmission line for the baseline system is 80% of the propagation velocity of light, as listed in Table 2. The velocity of light is approximately 1 foot per nanosecond. Therefore, the transmission of the digital data will require approximately 300 ns to propagate along the line for a distance of 250 feet. The 600 nanosecond two-direction propagation delay is very close to the 1 μ s clock period, requiring impedance matching techniques to be implemented. A slower data rate or shorter transmission lines would reduce the impedance matching requirements.

The logic propagation delay, characterized by the delay in switching the electronic elements, is typically in the range of tens of nanoseconds. It is generally important that the propagation delay due to the logic elements be large compared to the difference in propagation delays between the various paths in order to minimize the clock pulse skew considerations. For the baseline system, the line propagation delays are an order of magnitude greater than the logic element propagation delays. This condition could result in clock pulse skew problems, requiring insertion of predetermined propagation delays to insure proper operation.

Clock Pulse Skew Considerations

The clock pulse skew affect is caused by unequal propagation delay paths for the data and the clock pulses. This condition may cause the data changes to propagate through the system more rapidly than the clock pulses, resulting in critical race conditions that can cause erroneous or ambiguous data to be set into the flip-flops. A data flow functional diagram, illustrated in Fig. 4, will be used to describe the clock pulse skew affect. The state of the flip-flop will be set to the input state with each clock pulse, which arrives at the τ intervals. Therefore, the input data must propagate through the system and stabilize at the flip-flop input at time $(n\tau - k)$, which is prior to the arrival of the clock pulse, defined as time $n\tau$. The clock pulse will cause the flip-flops to change state, resulting in new data propagating through the system. In an application where the clock pulse must propagate to remote parts of the system through long propagation delays, a race condition will result, where the new state of the earliest clocked flip-flops will propagate to the more remote flip-flops simultaneously with the clock pulse. If the clock pulse arrives first, the flip-flops will be set to the state of the present data prior to the new data propagating to the flip-flop inputs, but if the clock pulse is excessively delayed, where the new data arrives at the remote flip-flop first, the new data will be erroneously clocked into the flip-flop.

Synchronous digital systems operate with non-critical race conditions, where the flip-flop propagation delay (Δ) is long enough to insure proper operation. For systems in which the flip-flop propagation delay is small compared to the transmission propagation delay, transmission line length and velocity differences may permit the new data to arrive at the remote flip-flops prior to the clock pulse, resulting in a hazard condition.

The waveforms in Fig. 5 illustrate shift register operation for a non-critical race condition with waveforms V and VI and a critical race condition with waveforms VII and VIII. Each clock pulse will cause the state of the flip-flop to be set to the input condition, with the

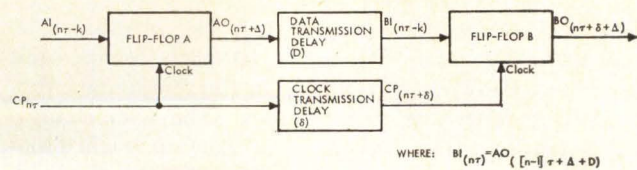


Fig. 4. Clock pulse skew diagram

change propagating to the flip-flop output after a Δ propagation delay. The data will then propagate through the D delay to the input of the B flip-flop, to await the next clock pulse. If the delay of the clock pulse is less than the $\Delta + D$ delays, illustrated in waveform V, the proper data will be clocked into the B flip-flop, illustrated in waveform VI. If the δ delay of the clock pulse is greater than the $\Delta + D$ delays, illustrated in waveform VII, the new data will have arrived at the B flip-flop input before the clock pulse, resulting in this improper data being clocked into the flip-flop. The hazard associated with the clock pulse skew condition is prevented with the incorporation of controlled delays introduced into the data line receivers to insure that the clock pulse propagation delays are less than the data propagation delays.

System Mechanization And Considerations

A functional diagram of a typical system is illustrated in Fig. 1, where a central unit communicates with various remote units through relatively long transmission lines. The D and δ parameters pertain to the propagation delays through the corresponding transmission lines. Communication is accomplished between the central unit and each of the remote units, where data is transmitted to and from each remote unit. Communication can be accomplished directly between the various remote units, with a minimum of constraints for synchronous transmission. The central unit will generate clock pulses to synchronize the digital data transmission and operation within units and will control the data transmitted between units.

The clock pulses are generated in the central unit, then fanned out to the various remote units. Therefore, the central unit will be clocked first, and the clock pulse will propagate to the remote units, and be followed by

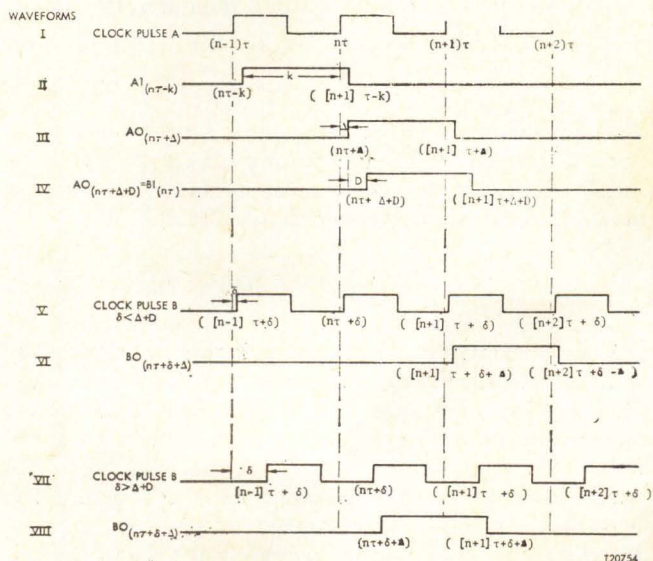


Fig. 5. Waveforms

the data change. The system will be constrained so that the clock pulse will arrive at each remote unit before the data change, resulting in the remote unit flip-flops being set to the proper states. The data changes due to flip-flops transitions in the remote units will propagate to the central unit and other remote units with an inherently non-critical race condition.

The clock pulse fanout from the central unit should be in a radial manner, where a different clock line is routed directly to each remote unit. A "daisy chain" clock pulse fanout, where a single clock line is strung out from unit to unit, should be avoided to minimize clock pulse skew. The technique will also insure that clock pulse skew need only be considered for data transmissions from the central unit. Data transmissions from remote units will be inherently of a non-critical race type, because the propagation delays insure that data transmitted from the remote unit will not be available at the central unit until after the clock pulse has arrived.

This discussion will neglect certain propagation delays within the central unit and remote units which are of a trivial nature compared to a predominating propagation delay.

The primary system constraint for proper operation is that the largest sum of the data propagation delays must be less than the clock pulse period. The longest delay may be composed of data or clock pulses transmitted from the central unit propagating to a remote unit, data propagating to various other remote units, then data propagating back to the central unit. It should be noted that transmission will be between flip-flops, where the delay is the sum of the logic and transmission propagation delays, to be summed from the output of each flip-flop to the input of other flip-flops.

The primary constraint is described in Equation 8 as an inequality, where the clock period must be greater than the combined propagation delays for:

- a. The clock pulse from the central unit to the particular remote unit (δ).
- b. The data between the various remote units (ΣD_K).
- c. The data between the remote unit and the central unit (D_R).

The longest propagation delay must satisfy Equation 8 regardless of the combinations of path components. To satisfy this constraint, a compromise must be achieved between clock rate and transmission distance.

$$\text{Clock Period} > \delta + \Sigma D_K + D_R \quad (\text{Eq. 8})$$

The secondary system constraint is that the clock pulse must propagate to each remote unit prior to the data. Transmission lines from the central unit to a specific remote unit should be routed together to insure that they are of the same general length, so that the D_C and δ transmission delays will be approximately equal. The logic delay, Δ , in the data propagation path will improve the clock skew condition by increasing the data propagation delay with respect to the clock pulse delay.

The considerations for clock pulse skew non-critical race conditions can be illustrated with the inequalities of Equation 9.

$$\Delta + D_C + \alpha > \delta \quad (\text{Eq. 9a})$$

$$\delta + D_R > \epsilon \text{ where: } \epsilon \ll \delta, D_R \quad (\text{Eq. 9b})$$

$$\delta^k + D_K > \delta l \quad (\text{Eq. 9c})$$

The condition for hazard free synchronous transmission from the central unit to a remote unit is defined in Equation 9a, where the sum of the data propagation delays must be greater than the clock pulse propagation delay. The Δ parameter is the logic delay, the D_C parameter is the transmission delay, and the α parameter is a calibrated delay introduced in the line receiver to insure that the inequality will be satisfied. This α delay is necessary because the D_C and δ delays are approximately equal and the Δ delay is relatively very small.

The condition for hazard free synchronous transmission from each remote unit to the central unit is defined in Equation 9b, where the local clock pulse transmission delay within the central unit, ϵ , must be less than the clock pulse transmission delay to the remote unit, δ , and the data transmission delay from the remote units to the central unit, D_R . The condition is inherently met because ϵ is very much less than either δ or D_R .

The condition for hazard free synchronous transmission between remote units is defined in Equation 9c where the clock pulse propagation delay to the l^{th} remote unit, δl , must be less than the clock pulse delay to the k^{th} remote unit, δk , and the data propagation delay between those two remote units, D_K . This condition is inherently satisfied if the radial clock pulse fanout technique is used. For a system with a "daisy chain" clock pulse fanout, precautions must be taken in the clock pulse routing and α delays should be introduced in the data transmission lines with line receivers.

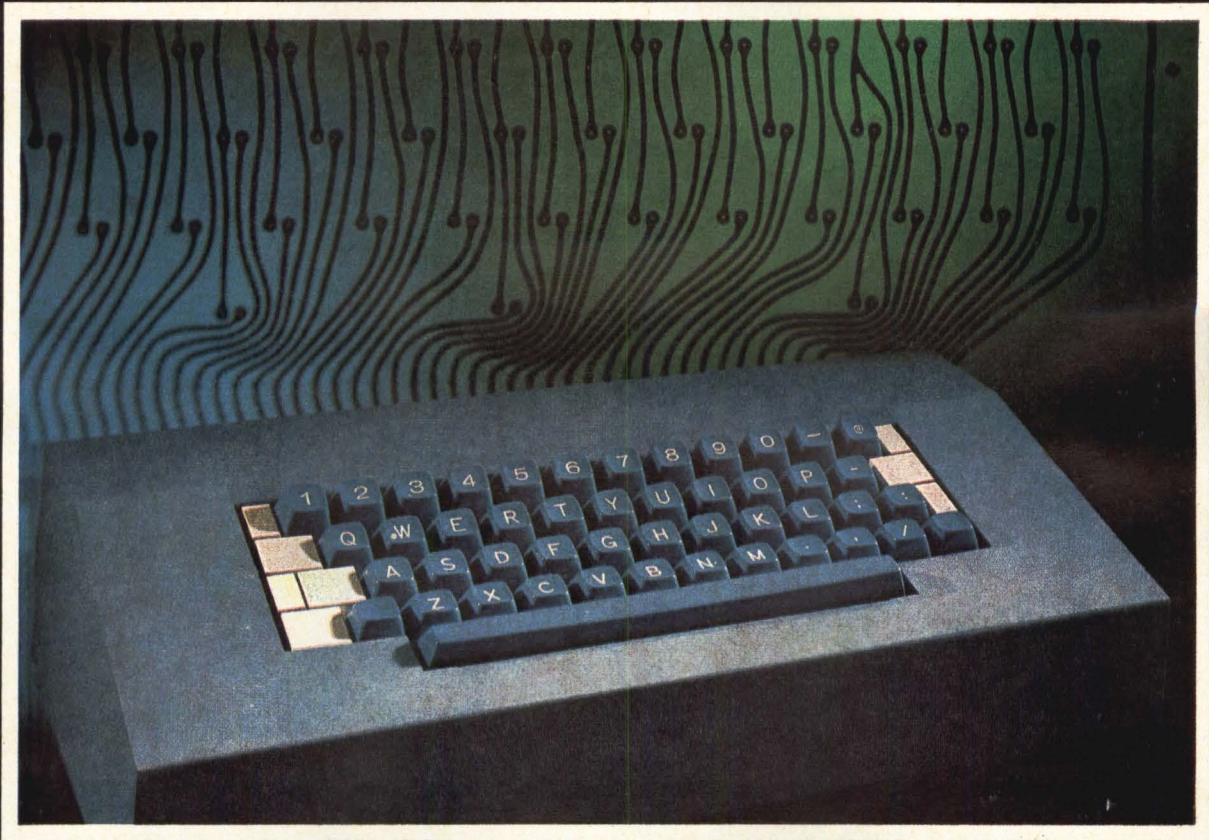
The transmission cable type selected for the baseline system is described in Table 2. It was selected for low capacitance and attenuation characteristics and high velocity of propagation. In addition, the relatively small size and weight of this transmission line yields packaging advantages.

Line drivers are required in the central unit and remote units in order to increase the signal level to minimize the effects of transmission line degradation of the signals. Line drivers are used to generate the proper signal amplitude and source impedance for transmission.

The line receiver should be similar to the Sylvania SG80 pulse shaper and delay integrated circuit, which is a monolithic circuit containing a Schmidt trigger for rise and fall time reconstruction and an externally adjustable integration delay for noise reduction and clock pulse skew compensation. This line receiver will sense the pulses on the transmission line, delay the pulse, then generate a precise output square wave. An external capacitor will be used in conjunction with this circuit to introduce a calibrated delay in the transmission line, defined as α , to insure non-critical race conditions associated with the clock pulse skew affect.

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A departure from conventional keyboard operating principles contributes to error-free code generation. Resultant simplicity provides secondary benefits ranging from transmission security to lower system cost.



ELECTRONIC KEYBOARD

A novel approach to keyboard code generation, which provides a simple, but reliable means of rejecting both external and internal noise, including jamming signals, has resulted in a keyboard design that eliminates coding errors in the circuit and reduces the likelihood of operator error. This new keyboard (patents pending), developed by engineers at IKOR, Inc. in the Northwest Industrial Park, Burlington, Mass., is said not only to retain the advantages of the photo-electric systems (no mechanical crossbars or other interconnections), but also to eliminate other problems associated with both photo-electric and electro-mechanical keyboards.

Coding In The Keys

Code functions are incorporated into each key as in photo-electric systems. But here the unique principle introduces system simplification. Transmit and receiver bars, which have a universal function within the system, run between key rows thus servicing more than one row in every case but the top and bottom rows.

Depressing a key produces an AC couple between the transmit-receiver bars and generates a code unique to that key (Figure 1). A closed-loop circuit is effected as each key is depressed, permitting discrimination against any noise not in phase with the keyboard signal generator. As the illustration shows, this technique eliminates the need for mechanical connections between individual keys and other portions of the keyboard. So, in addition to the reduction of coding errors, this system makes it possible to add or replace code functions at any time without any modification whatsoever of the basic circuitry. The transmit and receiver bars perform the same function for **all** keys within the given code format (8-level ASC II code is standard, but others may be employed).

Not only may keys be added at any time, they may be added in any position since the only requirement is that they fall within the keyboard arrangement provided and between the transmit/receiver bar rows.

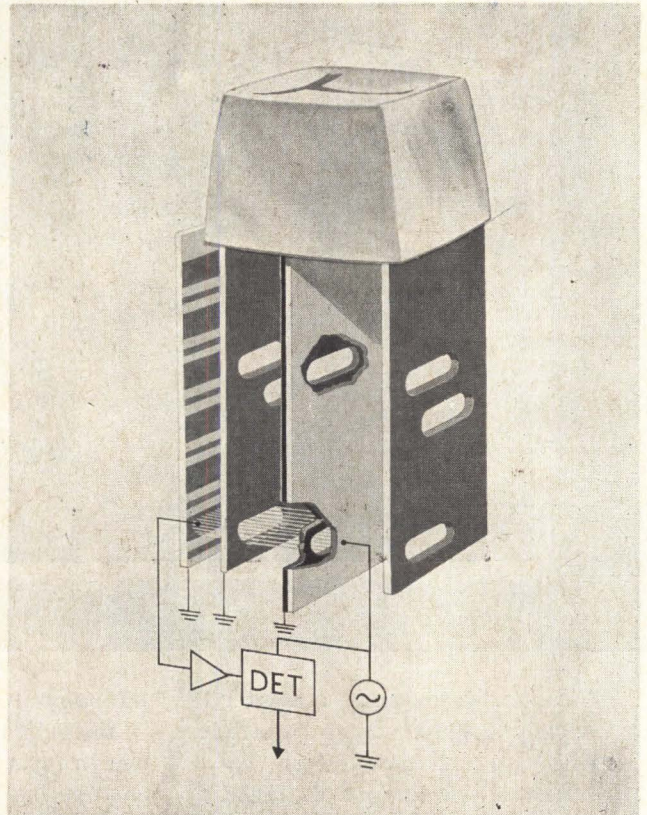


Fig. 1 Principle of Operation: Depressing key produces an AC couple between transmit and receiver bars generating a code unique to that key. A closed-loop circuit permits rejection of noise not in phase with keyboard current generator. Transmit and receiver bars run length of and between key rows. Elimination of mechanical connection to all key positions and the "universal" function of transmit and receiver bars permit any key to be assigned to any position at any time. No change in basic circuitry is involved.

System Compatibility

The IKOR keyboard, with clocked output, interfaces directly with any digital printer, CRT, tape recorder, computer or other information storage system and can provide either serial or parallel inputs to these systems. The basic keyboard contains eleven data and three control channels.

Shift or control keys permit selection of the 7 channels assigned to those modes. Normally, activation of a key generates a 7-bit code plus 1 bit for odd or even parity. A strobe output (flag) is provided at the interface connector in the form of a voltage change so that only when all character bits have reached equilibrium can the information be "cleared" for transmission.

Independent upper-case code generation permits keyboard users to specify and utilize only those functions desired with the provision for addition (or changes) at any subsequent time.

Virtues Of Simplicity

Although the principal objective was to reduce coding errors, the simplicity of the system allows some equally significant secondary benefits:

- **Keyboard arrangements** are exceptionally flexible since the complete coding function is delegated to the

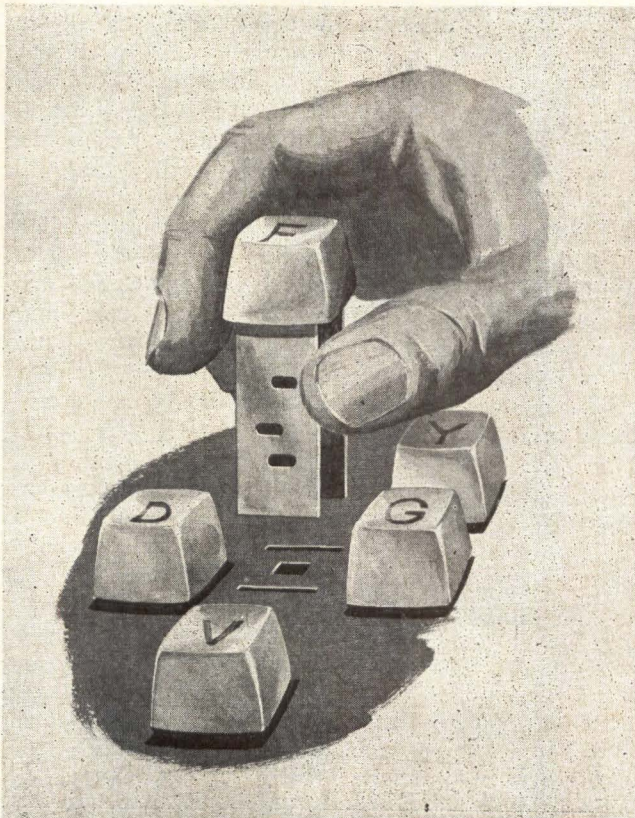


Fig. 2 Key Replacement/Addition: Since each key is its own code generator, simple addition or modification of functions (keys) can be made economically at any time. New key is merely snapped into position. All key positions on standard keyboard are filled with "dummy" keys and dustcaps so that full key capability may be utilized whenever desired. Illustration also indicates how new principle permits key mounting without wobble or play.

key itself. Typical keyboard arrangements, shown in Figure 2, range from 44 keys plus space bar, to over 80 keys. Standard alphanumeric arrangements are used to capitalize on operator familiarity, but any arrangement is possible. Numerical (or adding machine) functions can be conveniently grouped separately. This can be of advantage when keyboard entries are made by operators who are not familiar with touch-typing of numbers or when adding machine operations are to be performed. System cost is lower in terms of initial keyboard price and also because of minimal maintenance requirements. Mechanical wear is limited to sliding of the keys in their guide and to the life of the return spring (rated at 1×10^7 operations, minimum). Also, there is inherent zero "bounce" in the key, comparable to high performance keys that cost approximately \$10 per key (thus involving close to \$500 for a 44 to 50 key system over and above cost of any other components). In production quantities, the basic keyboard is marketable at under \$200 and in small quantities is only slightly more than \$300.

- **Mechanical design** is said to approximate the most desirable electric typewriters currently available. Ideal key spacing, solid-feel and responsiveness were designed into the system to reduce coding errors due to operator error as well as to circuitry. Similarity in handling between the new keyboard and electric typewriters eliminates the need for special operator training.

The new electronic operating principle plus the key mechanism permit speeds not common with other keyboards. At a demonstration for COMPUTER DESIGN, the keyboard "drove" a standard Teletype printer at approximately 90 words per minute, illustrating its capability for tie-in with other "hard copy" or visual display systems. The keyboard is electronically interlocked to prevent transmission of errors that result from striking more than one key at a time or striking keys at rates in excess of 40 characters per second.

- **Transmission security** is provided as a result of the system's low power drain and low radiation level. Only milliwatts of power are utilized by the keyboard so there is no longer any definable spike to signal the beginning of code generation. In an era of sophisticated "bugging" (between companies as well as countries) this improved security factor may be a most important secondary benefit.

Low radiation level and ability to reject spurious signals also means that when these keyboards are used in multiple station complexes or as part of a time-shared system they will not "talk" to each other or to other equipment.

Code Lockout For Multiple Code Format Use

The IKOR keyboard (Model 6000) is normally supplied without its housing for direct incorporation into specific system packages. Since the keyboard is compatible with basic ASCII code or can be supplied to any truth table within the limits of the eleven (11) channels available for coding, provision is made for mechanical lockout of selected keys. This can be accomplished with a mask plate when more than one coded output is provided and it is desired to prevent transmission of codes not acceptable to the receiver.

Circle No. 100 on Inquiry Card

IBM PROPOSES TRIPLE-REDUNDANT AEROSPACE COMPUTER

Michael Ball,
Fred Hardie
IBM Corporation
Owego, New York

Computer systems are called upon to perform one or more of the following basic functions: data management, data processing, and control. The complexity and criticality of these functions generally increase from data handling to control, and the optimum machine organization is highly sensitive to the functions to be performed.

Every computer mission is composed of either time critical phases or non-critical phases or both. Time critical phases are defined as periods within the over-all mission during which real time operations cannot be interrupted without seriously degrading the success of the mission; maintenance actions are not permitted. During non-critical phases, computer operations may be suspended for reasonable periods of time without degrading the mission. Maintenance actions are permitted during these down periods, which may be scheduled or random.

Availability can be defined as the probability that the computer system is in operating condition when operation is required. Availability unlike reliability, permits a system failure during non-critical periods providing that operation can be restored in time for critical phase operations or under other imposed mission constraints.

The objectives of the computer configuration discussed here are:

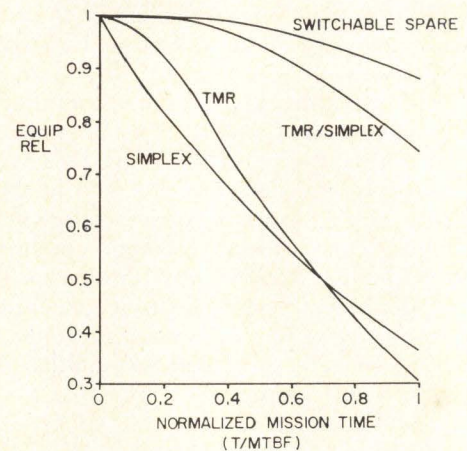
- High mission availability
- Extremely high critical-phase reliability
- Large data management and multiprocessing capability.

Design Objectives

The proposed design is intended to provide a multimode computer tailored to perform the variety of operations required on long aerospace missions. The architecture of this proposed design is compatible with the IBM System/360 but features the innovations of triple modular redundancy (TMR). The evolution of the computer architecture has included several important systems concepts:

- Adaptation to multiple uses within the same mission by means of operator controlled repartitioning.
- Ability to respond to external stimulation by dynamic reconfiguration under program control, to adapt more precisely to specialized functions or to provide graceful degradation.
- Ability to supervise itself, without manual intervention, for real time applications.
- Adaptation to inflight maintenance by means of automatic failure detection and fault isolation, and automatic self-repair.

With the increase in complexity of computer functions required in aerospace missions, the training and experience required for efficient maintenance has already exceeded that of the skilled specialist. Even the computer designer himself experiences difficulty analyzing the performance of a malfunctioning computer system. Inflight maintenance, especially, requires automatic error detection and self-diagnosis to the level of the replaceable module as a basic



function of the computer. Replacement of the failed module should be feasible without the need for special tools and should be automated wherever practical.

Although mission requirements may dictate equipment redundancy, aerospace applications generally require that the amount of redundancy be held to a minimum. Two techniques that seem to satisfy the availability requirements are correcting codes and TMR circuitry, both of which require approximately the same amount of hardware redundancy. A TMR/Simplex mode of operation will improve the availability of the computer subsystem in both critical phases and over-all mission. In this mode the subsystem may operate with one or more modules simplex and the remaining modules TMR.

Organization studies resulted in a computer configuration partitioned in a manner to provide optimum maintenance features. Simulation of this organization indicated a 99 percent efficiency in error detection by means of built-in test circuitry and normal operational programming. Automatic fault isolation to a replaceable module level was proven to be feasible. Logic investigations also indicated that on-line repair is feasible with the TMR computer, i.e., a module replacement could be made without interrupting normal computer operation. Manual and automatic switching techniques were studied and found to be practical for instrumentation in the TMR/Simplex mode or for module replacement by wired-in spares.

Qualitative availability comparisons of the various modes available in a TMR computer organization are shown in Fig. 1. The availability of the basic TMR organization (without maintenance) crosses the simplex curve at somewhat less than the MTBF of the simplex configuration indicating that the normal application of TMR is in missions where the mission time is short compared with the MTBF of the computer. In the TMR/Simplex mode, the availability of the redundant machine always exceeds the availability of the simplex machine by an appreciable margin regardless of the length of the mission. (In the TMR/Simplex mode, a good module is switched off along with the failed module leaving one good module in operation. If provisions are made to utilize the switched-off good module as a spare, then even greater availability is possible, as indicated by the switchable spare curve.) The specified availability for the critical phase of a mission was 0.999999, which calculations indicate would be achieved by a TMR/Simplex configuration. The specified mission availability, for a 90-day mission, was 0.9994, which is not quite achievable by the TMR/Simplex mode, but which could be met by the switchable spare mode or by selected spare modules. For exceptionally long missions, this wired-in spares capability can be supplemented by a set of manually replaceable spares.

Multimode Operation: Cerberus

The multimode Cerberus computer derives its potential flexibility and capability from a compatible mix of TMR machine organization, IBM System/360 power, automatic switching techniques, and organizational concepts derived during the course of the TMR/Simplex study. The various operational modes available in the proposed computer are listed in Table 1. Each mode is a variation of TMR or simplex operation, or a combination of both. The simplex modes are particularly applicable to the noncritical phases of the mission while the redundant modes are applicable to the critical phases.

In the **Simplex mode** two channels are turned off and the mission requirements are handled by the remaining channel. The computer is modularized, however, and modules

Table 1 CERBERUS OPERATIONAL MODES

PRIMARY MODE	SUB-MODE
SIMPLEX	SIMPLEX (WITH 2 WIRED IN SPARES) TRIPLE SIMPLE (INDEPENDENT CHANNELS) CORRELATED SIMPLEX (IND. CHANNELS)
TMR	TMR TMR/SIMPLEX TMR/SIMPLEX SWITCHABLE SPARE TMR/SELF REPAIRING

are available as wired-in spares from the off channels by means of module switching. This mode provides the highest mission availability for a given amount of hardware.

In the **Triple Simplex mode** all three channels are operating independently of the other two. This mode provides a simple multiprocessing capability. In space experimental systems, for example, one channel could provide data management for the experiments, a second channel provide data management for the life support system, and the third channel provide control of the vehicle.

In the **Correlated Simplex mode** all three channels are operating interdependently with the other two. This mode provides a high degree of simultaneity in the three channels, which operate in parallel with the state of the channels not easily related in any one machine cycle. One read-only store unit is used for controlling each of the three channels with synchronization and cross-channel control provided by common status registers and branch conditions. The mode provides a powerful system for complex computations and data management of large quantities of related material.

In the **TMR mode** the three channels perform in parallel and simultaneously on the same operation resulting in a highly reliable system compared to the equivalent simplex system providing that the operational period is short compared to the mean time to fail of the simplex system. This mode is especially applicable to the critical phases of an aerospace mission since component failures can

be tolerated without causing a system failure.

In the **TMR/Simplex mode** the redundant system automatically reorganizes itself to bypass a failed component. As a result of this reorganization one or more modules may operate simplex while the remainder of the machine operates TMR. This mode provides a highly reliable system compared to the equivalent simplex system regardless of the operational period (length of the critical phase).

The **TMR/Simplex/Switchables Spare mode** is similar to the TMR/Simplex mode but provides an even greater reliability improvement over the equivalent simplex system. An additional switching function is instrumented so that, in case a failure occurs in a TMR module which has already switched to simplex due to a previous failure, the remaining simplex channel of the module is made available to the system.

The **TMR Self-Repairing mode** requires a fourth channel to be built into the computer system. The system operates normally in a TMR manner with the fourth or spare channel turned off. On occurrence of a failure in the system, the computer automatically detects the error, isolates the failure to the specific channel and module, and switches in the appropriate spare from the fourth channel. The TMR-Self-Repairing would take priority over the TMR/Simplex and TMR/Switchable Spare modes; that is, the redundant system would not reorganize itself to partially simplex operation until the spare from the fourth channel had been used.

Table 2 — Cerberus Features

MISSION AVAILABILITY	<ol style="list-style-type: none"> 1. Simplex operation with inflight maintenance. 2. Automatic error detection. 3. Automatic failure isolation. 4. Wired-in, switchable spares. 5. Provisions for manually replacing failed modules.
TIME-CRITICAL RELIABILITY	<ol style="list-style-type: none"> 1. Modified TMR machine organization. 2. Automatic error detection and failure isolation. 3. Automatic reorganization to bypass failed components. 4. On-line repair.
MULTIPROCESSING	<ol style="list-style-type: none"> 1. Repartitioning of TMR computer to three simplex computers under operator control. 2. Cross-channel control and data transfer capability.

All four redundant modes are mutually inclusive; that is, one module of the system may be operating TMR (no failures), another TMR/Self-Repairing (one failure), another TMR/Simplex (two failures in the same module), and another TMR/Switchable Spare (three failures in the same module). If the TMR/Self-Repairing mode is instrumented, the Simplex mode contains three built-in spares rather than two, the Triple Simplex mode becomes Quadruple Simplex (providing independent operation of four channels), and the Correlated Simplex mode provides interdependent operation of four channels.

The specific features of the Cerberus computer which adapt it to the primary mission requirements are listed in Table 2. The primary mission requirements are high mission (long-term) availability, extremely high time-critical (critical-phase) reliability, and a multiprocessing capability.

High mission availability is achieved with simplex operation and inflight maintenance. The Simplex mode with wired-in spares provides the greatest availability potential of any simplex or redundant system for relatively long missions. Automatic failure detection is provided by a reasonable mix of built-in test circuitry and test routines. Failure isolation can be achieved in the Simplex mode by diagnostic programming or can be achieved by switching to the TMR mode and utilizing the built-

in disagreement detector network, which not only detects an error between the three operating channels but isolates the failure to a replaceable module. Physical design features such as modular packaging, replaceability, and connector sealing techniques allow manual replacement of failed modules with additional (non-built-in) spares, if required.

An extremely high time-critical reliability is achieved by means of the modified TMR machine organization. Automatic failure detection and fault isolation is achieved by means of the disagreement detector network without need for special test routines or diagnostic programming. Automatic reorganization of the computer system to bypass failed components is provided by the TMR/Self-Repairing, TMR/Simplex, and TMR/Switchable Spare operating modes, assuring uninterrupted operation during critical phases of the mission. On-line repair further extends the time-critical reliability capability by permitting the manual replacement of a failed module without interrupting system operation.

A multiprocessing capability is provided by repartitioning the TMR computer system into three simplex computers under operator control for non-critical phases of the mission. These simplex computers may be organized to perform independently on separate operations or to perform interdependently on different phases of the same operation.

Status

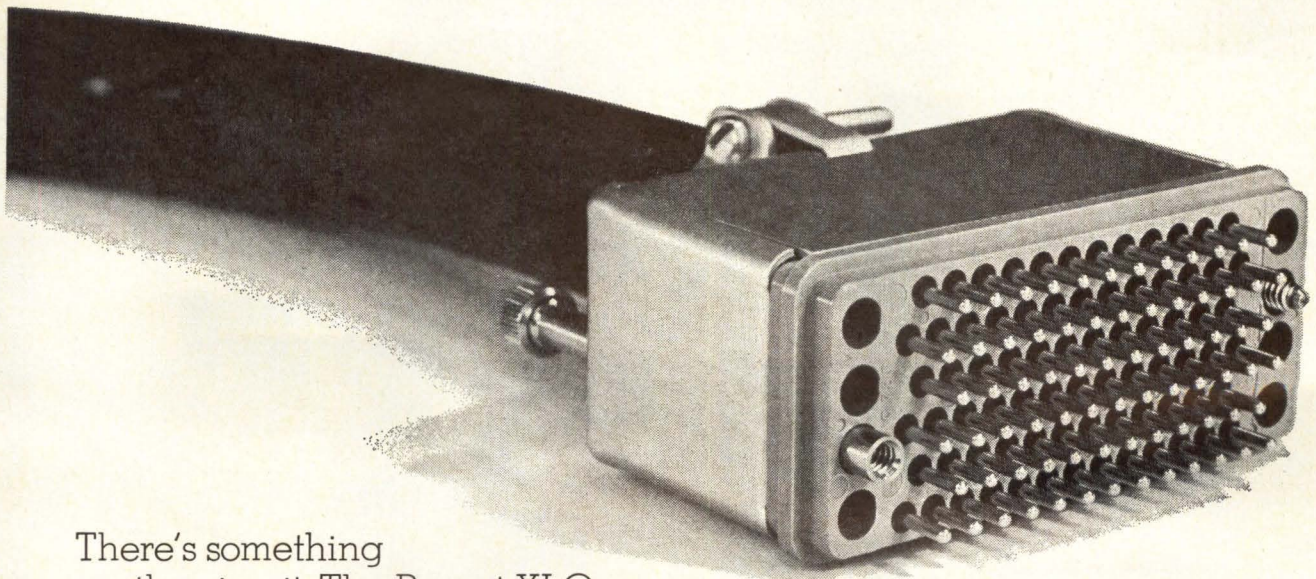
The critical element of the proposed computer design is the switchable voter. An automatic switching feature has been developed in which the voting circuit will detect a logic error, isolate the failure to a module and a channel, switch off the failed channel and one of the good channels, effectively forcing the TMR module containing the failure into a simplex mode. The automatic TMR/Simplex mode is therefore immediately feasible to instrument.

If an error is detected in a module that has previously switched to simplex operation due to a failure in one of the three channels, a manual switching capability is feasible to switch out this channel and switch in the remaining good channel of the TMR module. Further switching studies are necessary to automate this feature.

A slight modification to the present switching scheme would cause the switching circuit to switch in a wired-in spare rather than switch down to simplex mode. The TMR/Self-Repairing mode is therefore also immediately available. The Simplex mode with wired-in spares is presently available through the same switching methods.

Further work is required to develop switching approaches that will permit decoupling of the TMR channels rather than simple on-off switching. This type of circuit development will provide the necessary techniques for the Triple Simplex mode and Correlated Simplex mode.

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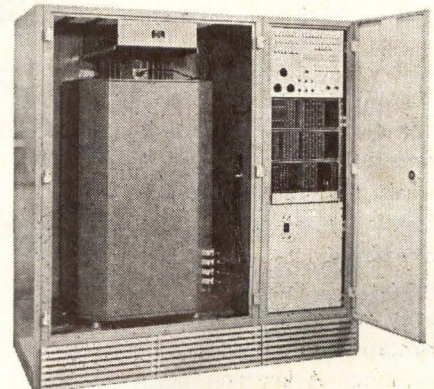


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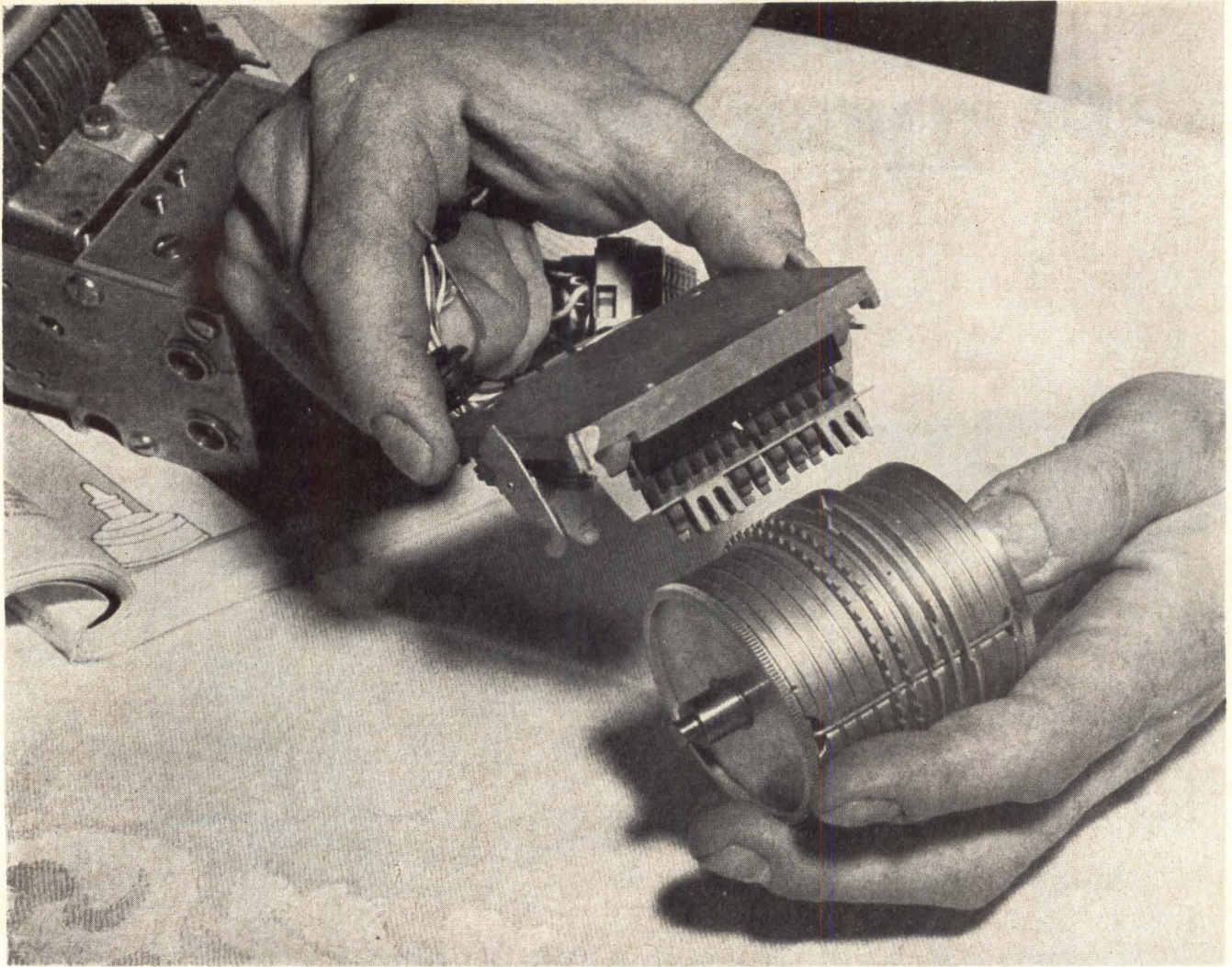


Fig. 1 Relationship of the switched or "memory head" to the coded drum in Giannini's Mem-O-Tizer.

Adrian Phillips, Systems Manager, Flight Research Division,
Giannini Scientific Corp.

ELECTRO-MECHANICAL DIGITAL TRANSDUCER RETAINS DATA UNTIL NEW SAMPLE IS TAKEN

Measuring the exact amount of each ingredient in the mix of a glass factory, determining the water level of a dam serving a hydroelectric plant, simultaneously reading out the level of each of the 100 oil tanks in a petroleum "tank farm," these operations, although their sources of information differ, have one thing in common. A key component in each system is a Mem-O-Tizer, a compact, completely non-electronic, one-step subsystem which converts a stepless, continuously variable analog function to a parallel, memorized, non-

ambiguous and electrically-expressed set of digits that can be read out immediately or hours later. The conversion from analog-to-digital values is made without buffers, amplification, decoding, translating or storage equipment. No operator is required to record the information, decode it and put it in form for a computer or other readout. The unit can handle up to 1 KW on each output line, and can be easily installed on existing meter systems, converting them from visual presentations to digit transducers with memory and electrical output.

Manufactured by the Flight Research Division, Giannini Scientific Corp., Richmond, Va., the Mem-O-Tizer can read out into any modern business recording or transmission equipment such as a printer, punched tape or punched cards for a computer, adding machine, or visual display. The digital information created by the Mem-O-Tizer can be fed singly into one machine, simultaneously into several machines, or consecutively into one machine after another.

The Mem-O-Tizer can "sample and hold" information indefinitely.

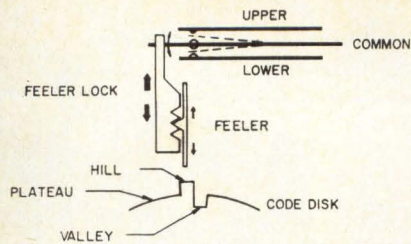


Fig. 2 Code Sensing in the Mem-O-Tizer.

This means that data is stored in the encoder until another sample is taken, and can be read at any time between the first and second sampling. The Mem-O-Tizer is non-ambiguous and is also absolute; it provides a precise digital value for each angular position of its input shaft. It can be driven directly-coupled, through a gear train or a rack and pinion, or it can be driven by magnetic coupling. Measurements of temperature, time, level, flow, rotation, position length, thickness and pressure are some of the areas where the Mem-O-Tizer is being used. Because of its low break-away torque (it is rated at 0.003 inch ounces) the input shaft revolves at the slightest movement. For example, blowing slightly on an inch-long piece of scotch tape, fixed to the shaft, will cause the shaft to rotate. The Mem-O-Tizer can be located a few inches or many miles from the recording or data display equipment.

Components of the Mem-O-Tizer include an input shaft, one or more drum assemblies, (the heart of its data coding system), one or more rows of sensing switches and a plug or terminal strip. Each drum assembly is made up of stacks of disks (Fig. 1). The outside perimeters of the disks are notched to three different depths (hills, valleys, and plateaus) and the disks are positioned to match the units assigned to specific input data. Each drum shaft is mounted on instrument ball bearings to provide low breakaway torque. As the input shaft turns, either clockwise or counter-clockwise, the drum disks revolve to ever-changing relative positions. The input data is reflected by the positions assumed by the notches on the disks. Designed for 10,000 rpm, the input system measures operations which may vary by one million units in a minute.

Upon interrogation, a solenoid-operated detent finger is vibrated into a detent gear mounted on the first drum. To eliminate ambiguity (the chance that the finger will strike the top of the ring and prevent read-out), half-wave rectified ac power vibrates the solenoid until the detent finger actually enters the gear.

During the momentary stopping of the drum, the solenoid moves the three position switch feelers to sense the codes as represented by the height of the disks (Fig. 2). The switches instantaneously sense and record the digits indicated by the coding disk profiles. These recorded values may be read through the output cable at any time or as many times as required until a new sampling demand is received. New demands reactivate the switches, thereby erasing previous readings. Interrogations may be made at the rate of 12,000 per minute.

A spring-loaded clutch or centering device allows the Mem-O-Tizer to be interrogated dynamically; the input shaft continues to rotate while the drum is momentarily sensed or read out, causing the drum to lag behind the shaft. As soon as the sensing action is completed, the drum resynchronizes or catches up to the shaft, and there is no loss of information.

Output codes can be decimal, binary, modified binary, binary decimal, grey, 5 bit, 6 bit, 7 bit and 8 bit, duo decimal, etc. In most applications, straight decimal coding is the simplest, eliminating decoders. Many special codes, such as counting in multiples of 3 or 5, can be readily produced.

For ranges of more than 128 counts, a second drum increases the counts to 10,000. This drum, geared 100:1 down from the first, uses a cam control technique to eliminate precision gearing and errors during transfer from 99 to 100. Changing the gearing between the first and second drum increases ranges and codes. A third drum increases the counts to 1,000,000.

A Typical Application

The Mem-O-Tizer's many advantages are illustrated by a new and simplified tank level measuring system introduced by Portland Pipeline, Portland, Me., for use on a single tank or on a "multi-tank farm."

This system consists of a fuel tank float, and a Mem-O-Tizer encased in an explosion-proof housing. The float follows the level inside the tank and, through a cable and pulleys, rotates a magnet outside the explosion proof housing, which, in turn, rotates the Mem-O-Tizer inside the housing. Using the tank level measuring system, it is possible to freeze the level data of an infinite number of tanks at widely separated locations, at any given instant. Tank level measurements are taken, digitized, and stored in 1/20 of a second, and is then held until needed or until the transmission equipment is available. Readings can be taken on demand or they can be programmed to be sampled and held at a desired time.

When other, non-storing, tank level measuring methods are used, 11 to 33 minutes may elapse from first readout to last on a 100 "tank farm"; the resulting total measurement is not precise for the *desired* instant because a change in value may occur between the successive readings. The Mem-O-Tizer registers the complete measurement at one time; readings are taken simultaneously, regardless of how many tanks are involved.

The Mem-O-Tizer's built-in memory enables an operator to interrupt his readout of one tank, switch to another, and then come back to the first reading without losing the data. Using tank measuring techniques with no memory, it is necessary to record or read the measurement at the precise time it is taken or to build costly and sophisticated memorizing equipment to hold the information.

The data stored in the Mem-O-Tizer after an interrogation is the information as of the pre-determined sampling time. Assuming that an analysis is needed every 60 minutes, an entire hour is available to transmit this information to the computer, to re-transmit it, to verify the correctness of the information, to check for transmission errors, to re-examine each point in the 200 station line. If the encoders had no memory and the operator wanted to know what the station conditions were at a given time, lightning fast and costly telemetry equipment would be needed.

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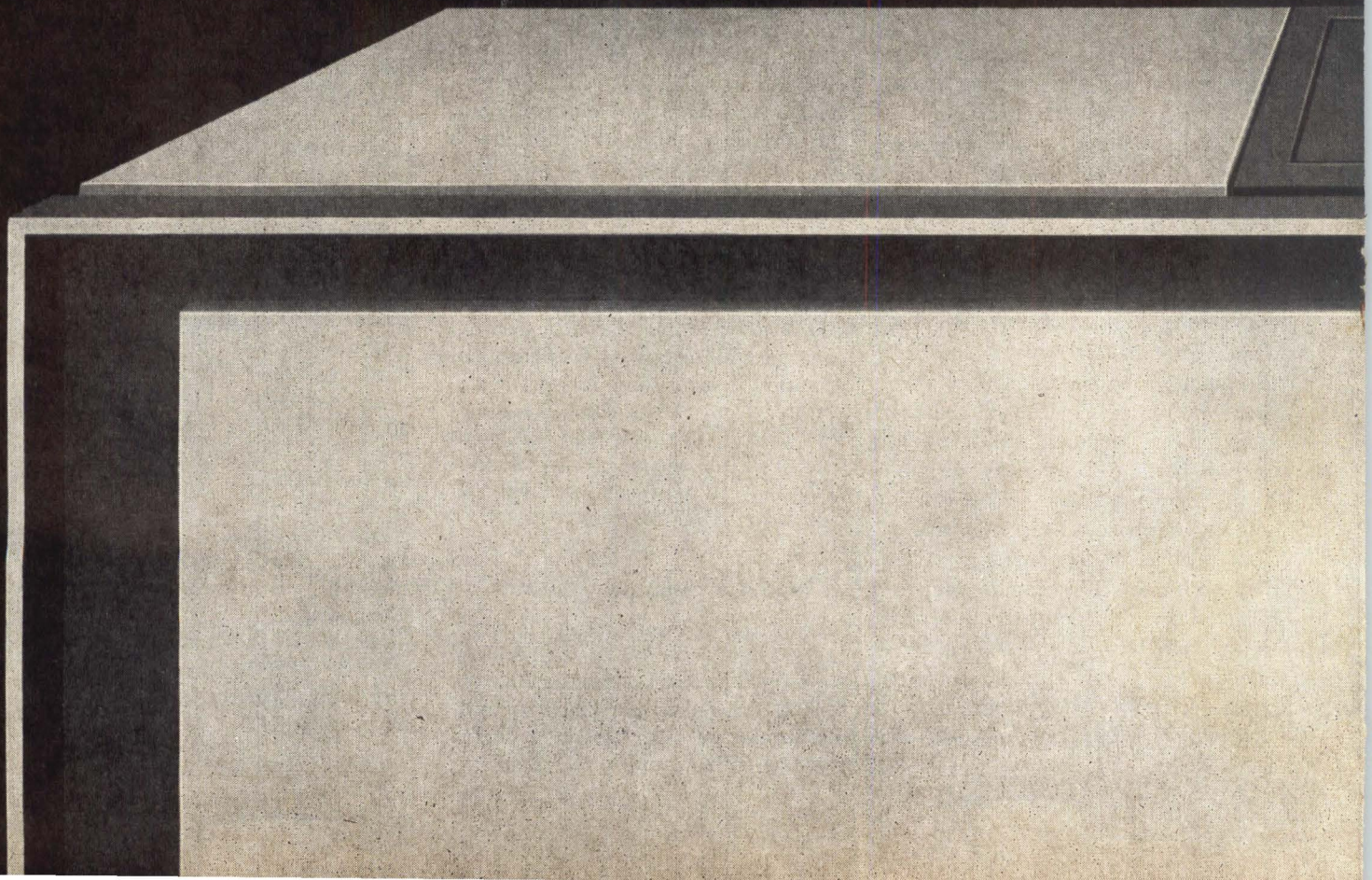
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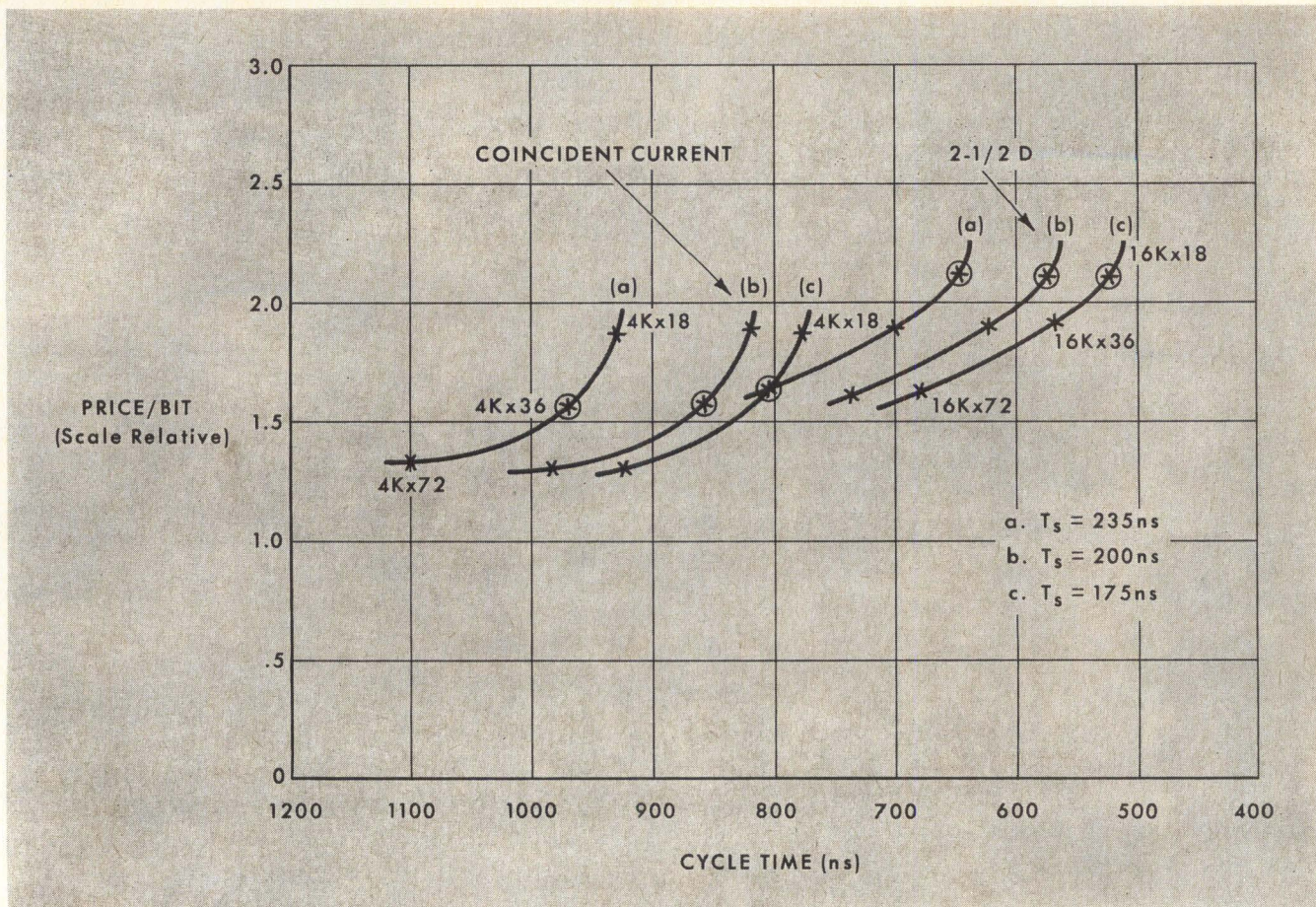


Fig. 1. Price/Performance Curves for 16 K x 72 bit System

A FRESH LOOK AT COINCIDENT CURRENT CORE MEMORIES

Delbert E. Elder, Manager of Engineering and Roy H. Norman, Senior Staff Engineer, Computer Products Div., Ampex Corporation.

The oldest core memory organization is regarded in a relatively new, seldom-discussed context: three-wire configuration. Certain advantages of 3-D and a new sense/digit circuit design for three-wire coincident current memories are discussed.

In the past two years, most of the literature devoted to core memory organizations has emphasized the comparatively new $2\frac{1}{2}$ -dimensional design. Much less attention has been paid other methods, such as 3-dimensional (coincident current), the oldest core memory organization.

A reason for this concentration on $2\frac{1}{2}$ -D is that the design uses three-wire and two-wire configurations, enabling the memory manufacturer to take advantage of the smaller cores with their faster switching time. In fact, such articles have often tended toward the implication that for the memory manufacturer who wants to use a 3-wire design, $2\frac{1}{2}$ -D is the most advisable approach.

The point often neglected is that 3-D, generally assumed to be a 4-wire organization, can be — and has been — designed with three wires. Thus the memory designer looking for a 3-wire approach should not automatically abandon coincident current in his thinking.

This article first will examine the economy and flexibility of 3-D and, second, will outline a new sense/digit circuit design for a 3-wire 3-D memory.

Study of Relative Economy

In the research that produced the speed-related economy graph in Figure 1, a cost-per-bit table was constructed which contrasted cost against word capacity and against word length.

The table was based upon these assumptions: 1.) A 4K-sense winding in each organization; 2.) A sufficient constancy in magnetic assembly and material; and 3.) A schedule of *relative* component prices, which would affect the electronics cost — i.e., stack diodes, balun transformers, drive transistors, etc. Thus only one variable exists: the number of components used as the memory capacity increases or the organization changes.

Figure 1 makes it possible to view the costs of 2½-D and 3-D memory organizations across a wide range of basic module sizes. Each level of crosses on the curves represents a different module size. It is clear that on any given module size, coincident current is the more economical in these terms.

Also notable is the progress of the economy of 2½-D, the cost decreasing as the word length is reduced, a dramatic drop evident from 72 bits to, say, 18 bits. The economy of 2½-D continues to rise when only the word capacity increases, and eventually would surpass that of 3-D; but that economy cannot hold if the word length also continues to rise.

It should be noted, too, that linear select (2-D) was shown to be more expensive than either 3-D or 2½-D, and extremely expensive at small word length. As the word length increases, there is a cross-over point where the economy of linear select would surpass even that of 3-D. But that cross-over point would be at or beyond the 100-bits-per-word mark; thus it tends to be a theoretical question since computer word lengths are generally 80 bits or less.

Optimum Configurations

Figure 1 shows the relative economy, in cost per bit, of 3-D and 2½-D memory organizations (both 3-wire) as related to speed. (Use of 4-wire 3-D would be marginally more expensive due to increased magnetic

costs, and faster in cycle time than 3-wire by no more than 50 nanoseconds, if that much, due to the slightly longer recovery time of the common sense wire in the 3-wire design.) The figure is plotted to provide an accurate picture of the price/performance points at which the economy of each organization is at its optimum. Results of our study are plotted for three different cores: 22-mil ($T_s = 235$ ns.), 18-mil ($T_s = 200$ ns.), and 18-mil ($T_s = 175$ ns.). The optimum module size in each case appears at the "knee" of the curve.

The comparison curves were plotted for a 16K x 72 bit system.

Findings from the study indicate the optimum configuration for a

speed-competitive memory to be a 2½-D 3-wire scheme using a 16K x 18 bit module, but the optimum configuration for a *price-competitive* memory to be a 3-D 3-wire scheme using a 4K x 36 bit module.

Even at these optimum configurations, the magnetics and drive-sense electronics would be approximately 30 percent more expensive for 2½-D than for coincident current 3-wire. This also substantiates the general statement that 2½-D finds its greatest economy in large word capacity and small word length; and that 3-D does so in smaller word capacity and greater word length — a point generally known but worth re-emphasizing here.

The importance of flexibility to a memory supplier serving many cus-

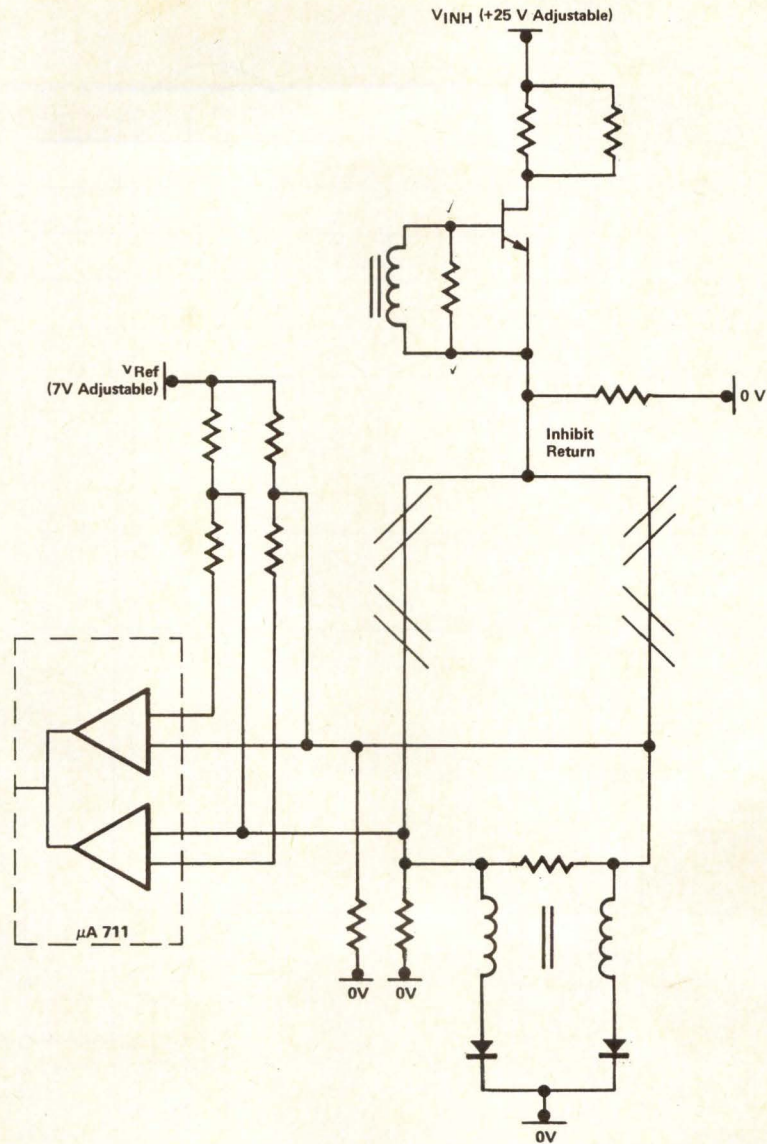


Fig. 2 Sense/Digit Circuit

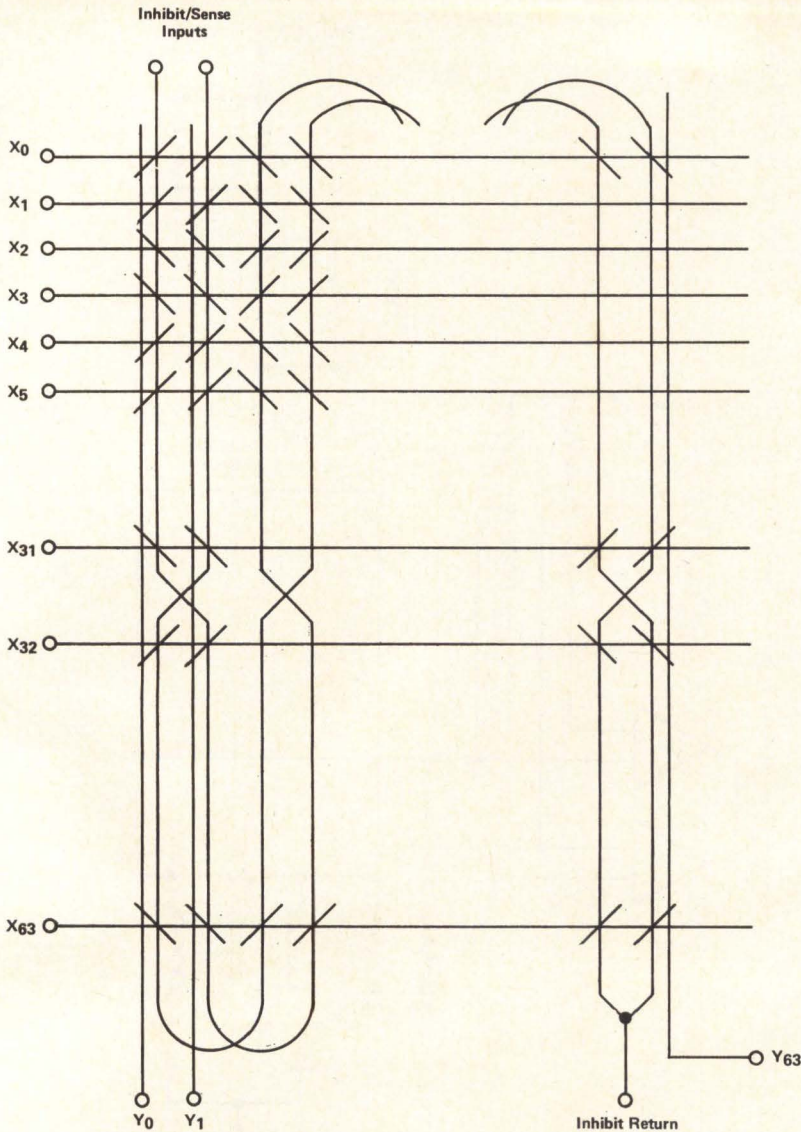


Fig. 3 Wire 3D Plane

tomers (as opposed to a computer manufacturer designing his own memory), and the advantages here of the modular 3-D design, have been explored previously by Gilligan/Persons (COMPUTER DESIGN, May 1966) and will not be repeated here.

But it is important to add that if 3-D flexibility has helped the memory supplier meet customers' widely varying initial requirements in word-lengths, capacities and speeds, its advantages have become even more obvious with respect to customer requirements *after* the initial sale. *Economical* field-expandability, in commercial and military systems alike, is an increasingly common requirement among customers — such as the customer who wants an 8K x 36 bit memory now but foresees expanding to 16K words a year from

now to meet the anticipated growth of his computer system.

New Circuit Design for 3-Wire 3-D

The desire, in a largely economy-oriented industry, for a memory with the price competitiveness and flexibility of coincident current, yet able to utilize the smaller cores, has led us to a new type of 3-wire, 3-D design. Practical laboratory test data support the claim of a common sense digit configuration in a coincident current system which circumvents such historic problems as recovery time and circuit cost limitations. The scheme in addition achieves some system cost reduction when compared with a 4-wire system, due to reduced magnetics manufacturing costs.

A "building block" approach was

taken to yield 1.) a magnetic module containing a drive/sense system; 2.) a compatible decoding capability; 3.) compatible registers for data and address; and 4.) compatible logic for timing and control. Thus either a complete memory system or any part of one would be available.

For the stack design, a "double box" array was chosen; it is shown in Figure 2. The sense digit circuit, perhaps the key component in such a design, is illustrated in Figure 3. (Possibilities of a circuit for such a system were mentioned by Rumble (COMPUTER DESIGN, February 1967) and by Gilligan/Persons (C.D., May 1966).)

The transformer is connected in an antibalun configuration. This presents a low common mode impedance and a high differential impedance to the sense line. The primary inductance of the transformer is essentially non-critical, the only limitation being the leakage inductance that appears in series with the stack. The transformer obviously provides for equalization of the currents in the array.

The purpose of the diodes is to present a very high impedance in series with the differential recovery circuit. If the diodes were not present, it would impose an unreasonable specification on the DC resistance matching of the stack lines and transformer windings.

The circuit has been shown to operate successfully, with excellent recovery time characteristics. Also, the circuit is sufficiently simple to effect an over-all cost reduction. The main disadvantage is that the inhibit power dissipation is doubled.

Final Note

It is readily agreed that each memory organization has its ideal applications; this is reflected, for example, in the use of 2½-D by many manufacturers, including Ampex, in cases of particular speed or capacity requirements. But it is to the memory designer's interest to bear in mind that there are more instances than might generally be assumed in which 3-D continues to be the most practical approach.

That statement is now reinforced by the fact that, as we have shown, means can be established to use smaller cores in a coincident current organization.

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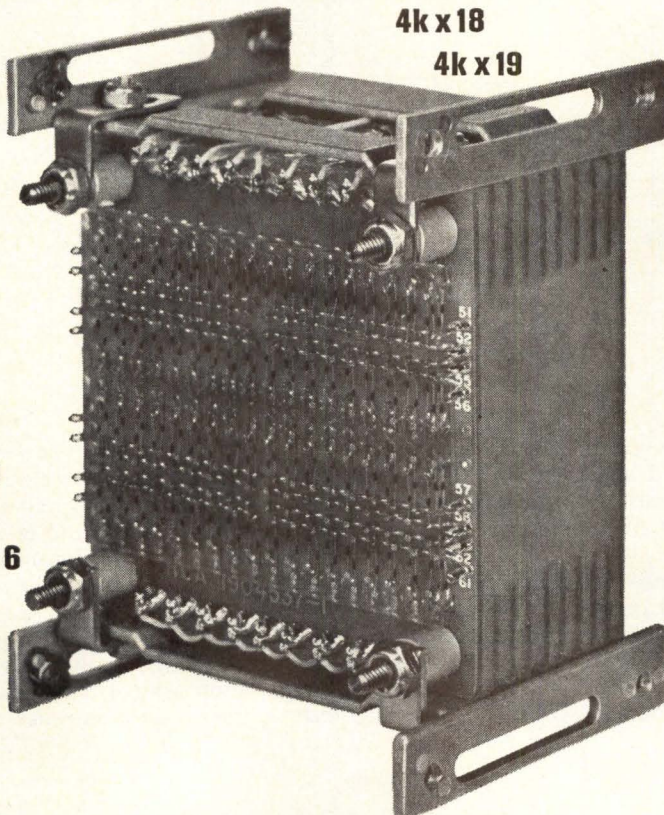
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4k x 15
4k x 14

4k x 17
4k x 18
4k x 19



4k x 20
4k x 23
4k x 24
4k x 25

4k x 10
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CIRCLE NO. 26 ON INQUIRY CARD

.... NOISE PROBLEMS IN FERRITE CORE COINCIDENT CURRENT MEMORIES

Edmund B. Daly, Bell Telephone Laboratories, Naperville, Ill.

This article was prepared while the author was a Member of the Technical Staff at the Automatic Electric Co., Northlake, Ill.

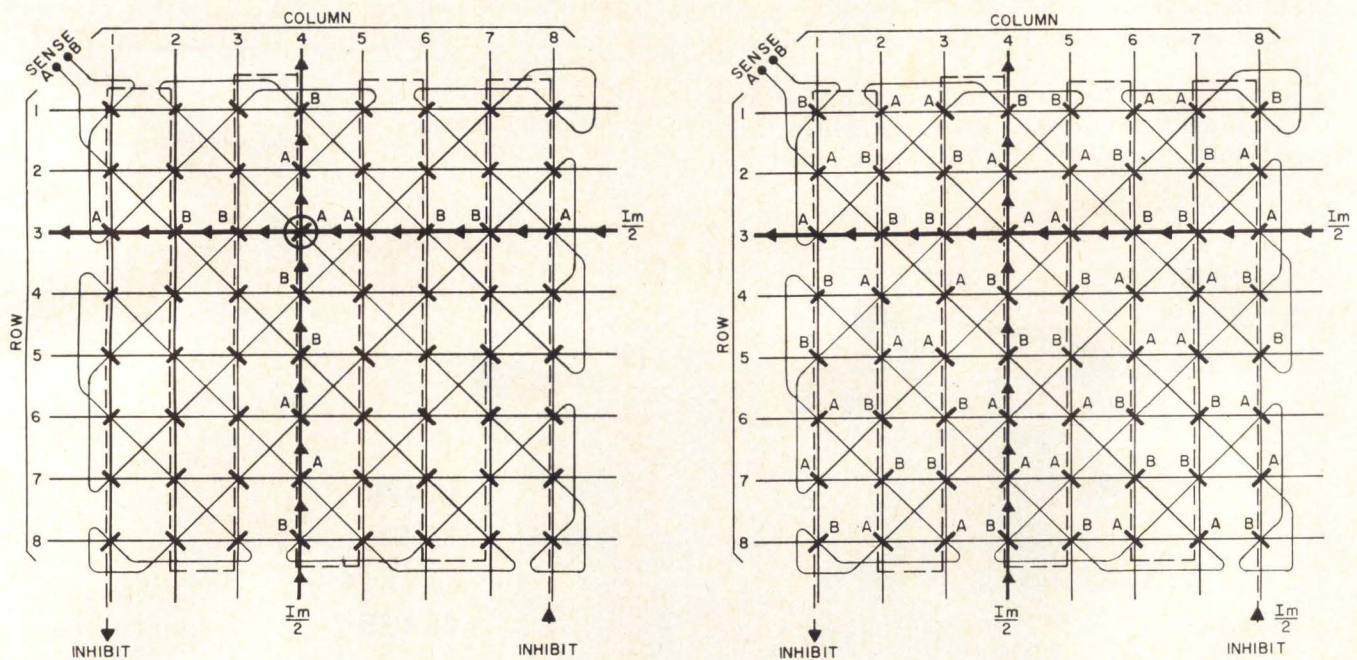


Fig. 1 A memory core is half-selected when it is excited by a driving field $I_m/2$. Figs. 1 (a) and (b) illustrate the two most common occurrences. In Fig. 1(a), information is being extracted from the bit located in row 3 and column 4 (3, 4); all cores in row 3 and column 4, other than the selected core (3, 4) receive a half-select read current ($I_m/2$). Due to the flux change in each half-selected core, a noise voltage is induced into the sense line. This noise is held at a minimum by stringing the sense line in such a manner to cause maximum difference mode noise cancellation: all "A" cores tend to force sense line terminal A positive with respect to sense line terminal B; all "B" cores tend to force sense line terminal B positive with respect to sense line terminal A. In Fig. 1(b), a zero is being written into (3, 4); the passage of inhibit current causes all cores in the plane, except those in row 3 or in column 4, to receive a half select read current (inhibit current is in the same magnetizing direction as read current). Each partially selected core induces noise into the sense line. The designations used in Fig. 1(b) are the same as those used in Fig. 1(a). The sense line again is wound to give maximum difference mode noise cancellations.

1. Cooke, P. and Dillistone, D. C.: "Measurement and Reduction of Noise in Coincident-Current Core memories," *Proc. IEEE*, vol. 109, pt. B. September 1962, pp. 383-389.

2. Raffel, J. I.: "Sense Winding Geometry and Information Patterns;" **Memorandum M-2919**, Lincoln Laboratory, M. I. T., July, 1954.

One important factor that tends to set an upper limit on the size and speed of a memory system is the noise that can be tolerated on its sense lines. This noise is generated either within the memory stack itself or within the wiring configuration connecting the memory stack to its associated sense amplifiers. A vast amount of information is presently available describing correct wiring procedures that should be followed when interconnecting memory systems, however, limited information is available describing the sources of sense line noise existing within the memory stack itself. This article, therefore, is concerned with the latter problem. A coincident current core memory has been chosen for purposes of analysis, but the principles developed should be applicable to other memory schemes.

Sense line noise, which increases with the size and speed of a memory system, is especially troublesome in coincident current configurations. That portion of the noise generated within the memory stack itself is caused by three factors: flux change in half-selected cores, electrostatic interference, and magnetic interference.

Sense line noise appears at the sense line terminals as either common mode noise or differential mode noise. Common mode noise causes the potential of both sense line terminals to change in the same direction and with the same magnitude. Differential mode noise causes the potential of one sense line terminal to change with respect to the potential of the other sense line terminal.

Noise Generated by Half Selected Cores

Half selected core noise occurs during both write and read phases of coincident current memory operation. During the write phase it is responsible for extremely large differential mode noise appearing on the sense line. During the read phase it is responsible for a smaller, but usually more troublesome, differential mode sense line noise. (See Figs. 1(a) and 1(b)).

Before proceeding into a mathematical analysis of half-selected core noise, a distinction must be made between reversible and irreversible flux changes that occur when a memory core is half selected. Even though both changes take place due to the creation and motion of 180° domain walls, the reversible change returns to its original magnetization state after the external field is removed, while the irreversible change causes a net change in the cores induction. Fig. 2 illustrates these two types of flux change: The movement from "a" to "b" and back to "a" is an example of reversible flux change, while the movement from "c" to "d" and back to "e" is an example of irreversible flux change.

The noise voltage induced on a sense line by a half-selected core can be approximated by:

$$V_t = n (d\Phi/dt) \quad (1)$$

where "n" equals the number of turns the sense line makes around the core ——— in our case $n = 1$. $d\Phi/dt$ is the rate of change of both reversible and irreversible core flux.

By definition:

$$\Phi = BA; \text{ total flux equals induction times effective core area.}$$

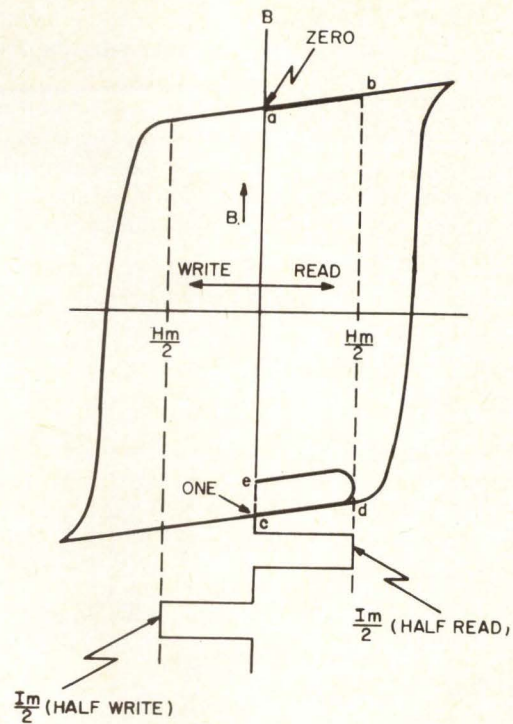


Fig. 2. Flux changes in half-selected cores

$\mu_{\Delta} = B_{\Delta}/H_{\Delta}$; Incremental permeability equals the ratio of incremental induction to incremental magnetizing force.

Substituting these quantities into Eq. 1:

$$V_t = \mu_{\Delta} A (dH/dt) \quad (2)$$

The factor dH/dt can be replaced by $H_m/2tr$, where $H_m/2$ is the half drive field and tr is the rise time of current producing the field H_m . The substitution of $H_m/2tr$ for dH/dt assumes that the total positive change in core flux takes place during the rise of the driving current; while this is true for the reversible flux (since the core acts as a linear ferrite until the knee of the B-H loop is exceeded) it is not true for the irreversible flux. To bypass this difficulty, only the maximum value of V_t (\bar{V}_t) will be considered. (\bar{V}_t is used since the calculated output voltage will be larger than the actual output voltage, i.e., we are assuming a larger rate change of flux.)

Taking "A" to be the cross-sectional area of core in cm^2 , tr to be the rise time of the driving current in seconds, $I_m/2$ to be the half drive current in amperes and r to be the mean radius of the memory core in cm , eq. 2 may be restated, in volts, as:

$$\bar{V}_t = \mu_{\Delta} \frac{(2A \times 10^{-7}) I_m/2}{r \quad tr} \quad (3)$$

Due to the dependence of V_t on μ_{Δ} , the value of V_t is subject to two core conditions: digit stored and previous history.

A distinction must now be made between $\mu_{\Delta-}$ and $\mu_{\Delta+}$. Referring to Fig. 2, $\mu_{\Delta-}$ is the incremental permeability of a core which is in the ONE state and goes through the irreversible transition $c \rightarrow d \rightarrow e$. $\mu_{\Delta+}$ is the incremental permeability of a core which is in the ZERO state and goes through the reversible transition $a \rightarrow b \rightarrow a$. $\mu_{\Delta+}$ acquires a minimum value $\underline{\mu}_{\Delta+}$ if, previous to its measurements, the core is disturbed by

a series of half read pulses. $\mu_{\Delta-}$ acquires a maximum value $\bar{\mu}_{\Delta-}$ if, previous to its measurement, the core is disturbed by a series of half write pulses.

The difference between $\mu_{\Delta-}$ and $\mu_{\Delta+}$ is important to the memory noise problem because the sense winding links all cores in a matrix such that half-select voltages tend to cancel. The maximum cancellation error per cancelling pair depends on the maximum difference between $\mu_{\Delta+}$ and $\mu_{\Delta-}$. Defining:

S = maximum cancellation error per pair of cancelling memory cores due to stored information and previous history.

$$S = \bar{\mu}_{\Delta-} - \mu_{\Delta+}$$

During the read interval, a square $n \times n$ matrix has one core receiving a full read current and $2n-2$ cores receiving a half-select read current. Of these $2n-2$ cores, two do not belong to cancelling pairs. The maximum delta noise is then caused by the following factors:

- Induction change of the two uncanceled cores $-2\mu_{\Delta}$.
- "S" unbalance of the $n-2$ core pairs $-(n-2)S$.

Therefore:

$$V_t(\text{delta noise}) = [2\mu_{\Delta} + (n-2)S] \times \frac{[2A \times 10^{-7}]}{r} \times \frac{I_m/2}{t_r} \quad (4)$$

Write Operation

When a ZERO is written into a word bit, both inhibit and write currents flow through the bit plane. All cores in the plane, except those on the driven X and Y lines, receive a half-read current (inhibit current). The half-selected cores cause a large noise signal to appear on the sense wire; this noise can paralyze the sense amplifier.

The worst case sense line noise occurs when the digit plane contains both information and disturb asymmetry, each cancelling pair of cores having a cancellation error equal to S . In practice, however, this worst case pattern is impossible to achieve. Cooke and Dillstone¹ point out that the worst case realizable noise pattern occurs when half the plane contains information and disturb asymmetry, while the other half plane contains only information asymmetry.

Defining S^* = maximum cancellation error per pair of cancelling memory cores due only to information asymmetry.

$$S^* = \mu_{\Delta-}^* - \mu_{\Delta+}^*$$

$\mu_{\Delta-}^*$ is the effective incremental permeability of a core in the ONE state previously disturbed by a series of half-write currents. $\mu_{\Delta+}^*$ is the effective permeability of a core in the ZERO state previously disturbed by a series of half-write currents.

If only inhibit current flows through the memory plane, the half plane containing both information and disturb asymmetry produces a maximum sense line noise:

$$\bar{V}_t' = (n^2/4) (S) [(2A \times 10^{-7})/r] [(I_m/2)/t_{r(\text{inhibit})}]$$

The half plane containing only information asymmetry produces a maximum sense line noise of:

$$\bar{V}_t'' = (n^2/4) (S^*) [(2A \times 10^{-7})/r] [(I_m/2)/t_{r(\text{inhibit})}]$$

However, in addition to inhibit current, write current also flows through the plane in question; this current tends to cancel the effective of inhibit current through those cores located on the selected X and Y drive lines. The resultant sense line noise due to both inhibit and write currents can be represented by:

$$\bar{V}_{\text{noise}} = \left\{ (n^2/4) (S + S^*) [(I_m/2)/t_{r(\text{inhibit})}] - [(n-2)/2] (S + S^*) [(I_m/2)/t_{r(\text{write})}] \right\} \times [(2A \times 10^{-7})/r] \quad (5)$$

If $t_{r(\text{inhibit})} = t_{r(\text{write})}$, Eq. 5 can be approximated by:

$$\bar{V}_{\text{noise}} \approx [(1/2) (n-1)^2 (S + S^*) (I_m/2)/t_r] [(2A \times 10^{-7})/r]$$

The first term in Eq. 5 represents the noise due only to the flow of inhibit current. The second term introduces the effect of write current; this term is taken from Eq. 4 by assuming $2\mu_{\Delta} \ll (n-2)S$.

There are three methods that can be used to reduce the noise caused by half selected cores:

- Split the sense winding into a number of smaller sections, thereby reducing the number of partially-selected cores per sense line.
Cost: additional complexity of the sense amplifier inputs.

- Stagger the X and Y read drive currents. The first half-drive current to be turned on is the one which generates half-select core noise; sense line noise will then be maximally separated from the information strobe.
Cost: loss in cycle time.

- Post write disturb pulse is applied immediately after the write operation. This current eliminates all disturb asymmetry from the memory cores, thereby making the double checkerboard (information asymmetry) the worst case noise pattern.
Cost: loss in cycle time.

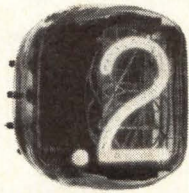
Noise Generated by Electrostatic Interference

If, as in Fig. 1(a), diagonal sense windings are used, a relatively large common mode noise is picked up when a drive line is excited. This noise is caused by electrostatic coupling between the sense line and the activated drive line. Even though common mode noise is not particularly troublesome, it can give rise to a sense line differential ring. This difference mode ring is caused by two factors:

- Coupling of common mode noise from one section of the sense line to another section.
- Unequal lengths of sense line between the point of noise generation and the two sense line terminals.

To eliminate the problem of difference mode ring a rectangular sense winding can be used. This winding threads each plane in such a manner that capacitive coupling from each drive line is equal for all points an equal distance from the ends of the sense line. The proximity relationship between the rectangular sense winding and the X-Y drive lines make it necessary to use read current staggering: Fig. 3, which illustrates a rectangular sense winding, shows that the X drive line runs parallel to the sense line, while the Y drive line runs

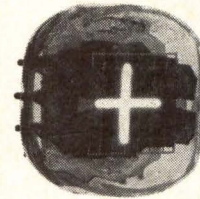
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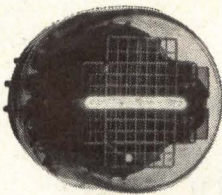
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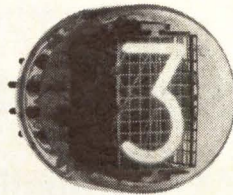
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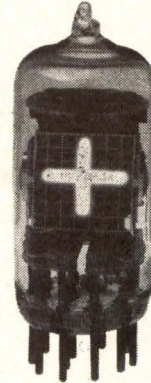
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CK1901—Interchangeable with B5016 and NL5016; CK1902—Interchangeable with B5032, NL5032, B50911 and NL50911.



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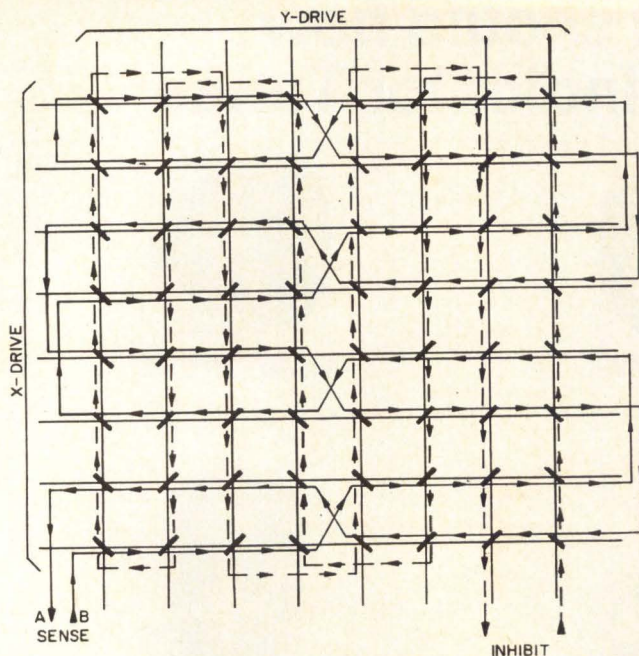


Fig. 3. Rectangular sense winding

perpendicular to the sense line. There is, therefore, a maximum electrostatic pickup from the X line and a minimum pickup from the Y line. To achieve minimum sense line noise during the signal strobing period, it is necessary to excite the X line prior to the Y line.

Noise Generated by Magnetic Interference

When considering the problem of inductive pickup, the memory cores can be completely neglected and only the closed loops of wire comprising the sense winding need be considered. Referring to Fig. 4, the requirement for a non-inductive winding is that the net area be zero.² Further, every length of sense line which has a component of direction parallel to the X or Y drive wires must have in close proximity to it a similar wire which travels in the opposite direction and which has the same components with regard to the X and Y wires. Neglecting end effects, both diagonal and rectangular windings give nearly perfect cancellation and are considered non-inductive.

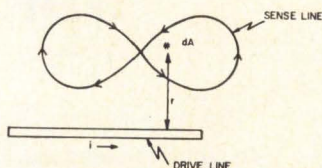


Fig. 4. Inductive pickup on sense winding

Conclusion

The origin of sense line noise has been traced to three sources: magnetic radiation, electrostatic radiation, and flux change in half-selected cores. In large memories, the third source is probably the most troublesome and therefore has been given the greatest attention. When considering noise caused by flux change in half-selected cores, two conditions were stressed: maximum cancellation per pair of cancelling cores, and previous history of noise-producing cores. A thorough grasp of these two concepts should enable the engineer to establish "worst case" noise patterns for any memory geometry.

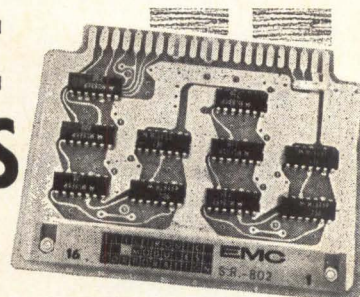
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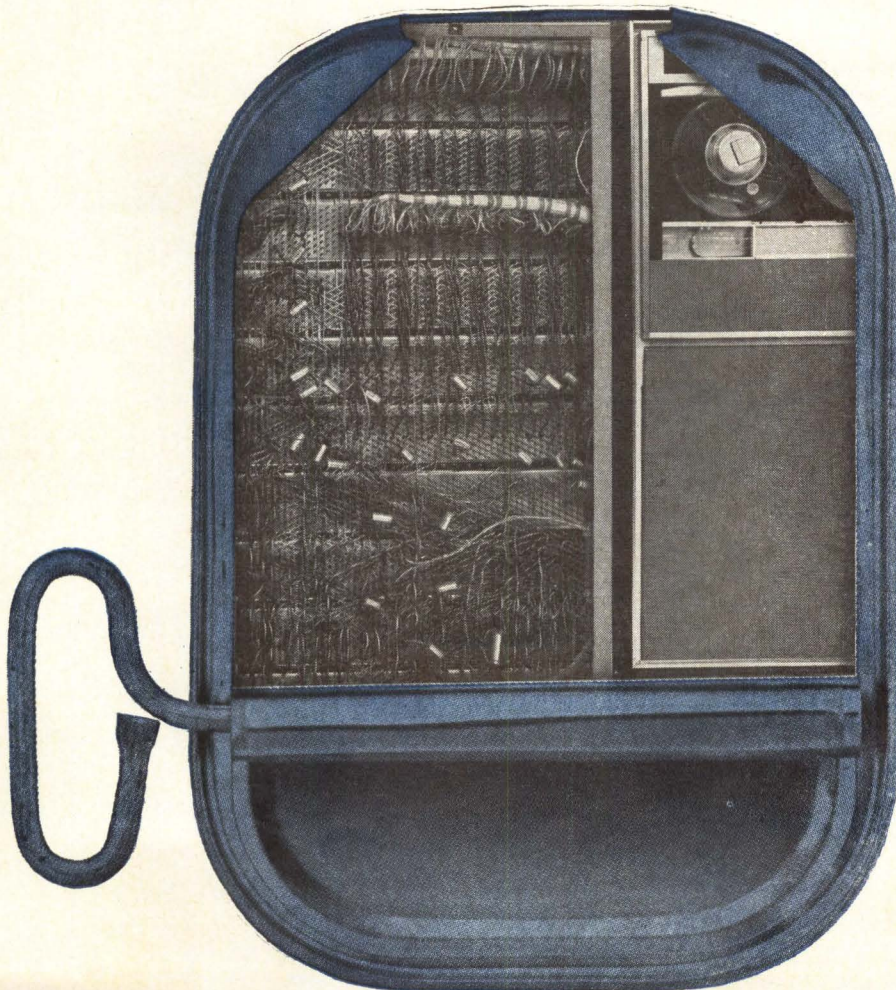
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THE DESIGNER THE SYSTEM AND THE "IC-MIX"

Walter A. Collymore
Arinc Research Corp.

Examples of Gains in System Size, Reliability and Cost Through Intelligent Selection of IC's for Specific Tasks.

Technological advances are often forestalled because the engineer is unwilling or unable to discard the shackles of old ideas and allow his mind to survey the potential avenues of change freely. Never was this more clearly seen than in the development of digital integrated circuits. The early designs were nothing more than an attempt to duplicate their discrete forerunners in terms of circuit configuration, with a blinding desire to minimize circuit component count. However, after several years of less than enthusiastic industrial acceptance, semiconductor manufacturers modified their design philosophy to maximize the inherent advantages of IC's; as a result, many different circuit configurations have developed based on the use of wide tolerances and a substitution of active for passive elements wherever practical.

Table 1 — IC-Mix Fan-Out Chart*
(Read chart top to bottom, left to right)

Driving Gate	Driven Gate	Fairchild		Motorola		Philco		Signetics		Sylvania	TI (Series)		Transitron		
		9R 0T 3L	9D 3T 0L	2R 0T 1L	M 3E 0C 1L	9R 0T 3L	9R 0T 3L	9D 3T 0L	1D 0T 1L	4D 1T 6L	S 8T 4T 5L 5	SG 4T 0T L	R 5C 1T 4L	5 4T 2T 0L	TNG 3T 1T 1L 1
Fairchild	903	5	4	2	5	5	5	4	2	6	5	3	5	2	3
	930	9	7	4	9	9	9	7	5	11	10	5	9	4	5
Motorola	201	10	8	5	10	10	10	8	5	14	13	7	10	5	7
	301	25	8	4	25	25	25	8	5	13	12	6	20	5	6
	903	5	4	2	5	5	5	4	2	6	5	3	5	2	3
Philco	903	5	4	2	5	5	5	4	2	6	5	3	5	2	3
	930	9	7	4	9	9	9	7	5	11	10	5	9	4	5
Signetics	101	10	8	5	10	10	10	8	5	13	12	6	10	5	6
	416	6	5	2	6	6	6	5	2	8	3	3	6	3	3
	8455	20	14	13	20	20	20	14	14	21	20	20	20	16	20
Sylvania	40	20	18	10	20	20	20	18	11	20	20	15	20	12	15
TI	514	5	4	2	5	5	5	4	2	6	5	3	5	2	3
	5420	20	15	8	20	20	20	15	8	20	20	12	20	10	12
Transitron	3111	20	18	10	20	20	20	18	11	20	20	15	20	12	15

*(DC Fan-out only)

The time has come for another bold step forward. The efficient utilization of the many IC designs available to the systems architect requires imagination and technical fortitude to ward off the "NIH" (Not Invented Here!) resistance. The next generation of digital systems will use an "IC-Mix" to optimize the majority of their requirements for low operating power, small physical size, high processing speeds, high noise margins, and above all, low cost. To accomplish this formerly unrealistic feat, the designer will use several circuit configurations, from possibly different manufacturers, connect different circuits together and similar circuits in groups to satisfy the overall system operational requirements. As an example, consider a system requirement for two additional levels of logic in an area which uses RTL circuitry to minimize power. Since TTL circuits have a propagation delay in the order of 10 nanoseconds, two TTL logic gates could be added, in the same logic chain with the RTL circuitry, with only a fractional increase in the overall delay time. The addition of these two TTL gates could very well mean the savings of five or six RTL gates and one or two flip-flops which would be needed to regenerate the function for use in a second shorter logic chain. The power requirements of the two solutions are approximately the same; however, the economic trade-off of fewer packages (with concomitant smaller volume and increased reliability) versus higher priced circuitry must be analyzed.

A second example of the use of an "IC-Mix" would be in the high-speed selection circuitry of a local data processor memory; here, minimum logic propagation delay time is required for short memory cycle times, and high noise immunity is necessary due to the close proximity of the logic gates to the memory stack. As a result a TTL gate configuration might be selected. Since our main concern is minimizing logic propagation delay time, we would naturally keep the number of logic gates between flip-flops to an absolute minimum. If we are required to generate the function $F = \overline{A} + B \cdot C$ we can accomplish this most easily through use of "collector OR-ing" or tying the output of two logic gates together, thereby gaining speed since implementation

of the function requires only one level of logic. However, memory selector circuitry mechanized using TTL gates cannot utilize "collector OR-ing" because of the active "pull-up". To generate the function $F = \overline{A} + B \cdot C$ using only TTL gates would result in a design that would utilize an additional level of logic over a mixed configuration using DTL gates where the "collector-OR" function is required, and TTL in the remainder of the logic.

Other areas of the data processor which lend themselves naturally to the use of an "IC-Mix" are the input/output and arithmetic sections. Here, a general requirement is for several registers to store data temporarily; usually these storage registers are mechanized with IC flip-flops or magnetic devices such as cores or delay lines. However, the MOS shift registers presently being manufactured by Philco, Microelectronics, and General Instruments are compatible with all popularly used IC's and have the advantages of smaller size, lower power consumption, higher reliability, and lower cost than either flip-flop or magnetic registers. All that need be added for general purpose use are discrete transistors for driving in and amplifying out of the MOS register. Dynamic logic MOS shift registers are presently limited to several megahertz operations; however, with the addition of discrete transistors to buffer external capacitance and the use of multi-phase clocking, much higher operating frequencies are possible.

Table 1 lists the most commonly used IC's and shows the fan-out capability of each circuit when connected to any other circuit. Table 1 is read from left to right and from top to bottom. For example, if the designer needs to know how many TI Series 5420 TTL gates can be driven by a Fairchild μ L930 DTL gate, he locates the Fairchild μ L930 "driving gate" on the second line from the top and follows this row horizontally until he intersects the vertical column containing the TI Series 5420 TTL "driven gate". At the intersection of the DTL row and the TTL column is the number 4, indicating a dc fan-out of 4 for the Fairchild μ L930 gate driving TI Series 5420 gates.

Listed below are a series of tasks that illustrate the types of analysis with which the circuit designer must

become familiar to guarantee proper selection of a system "IC-Mix".

1. Define overall systems requirements that influence IC selection, for example:

- Operating frequency
- Available power and maximum number of voltage levels
- Operating and storage temperatures
- Physical size limitations and projected packaging scheme
- Maintainability requirements
- Reliability goals
- Cost objectives

2. Subdivide the system into its major physical and/or electrical subsystems (i.e., for a computer the subsystems would be input/output, control, arithmetic, and memory).

3. Define subsystem requirements based on the items in (1) above and rank them in order of importance.

4. Select "IC-Mixes" for each subsystem that will optimize its major requirements.

5. Analyze the overall system in terms of the subsystem "IC-Mixes" and modify the "IC-Mix" to maximize major system requirements.

Items 1, 2, 3, and 5 are tasks normally performed on systems containing a single IC line and the approach is widely known and well understood; however, item 4 is unique to the "IC-Mix" philosophy and the analysis, depending on the subsystem complexity, may require use of subsystem computer models to make the decisions for final "IC-Mix" selection. The model would generally apply to any subsystem and would make decisions based on the general worst case or statistical limitations listed below plus other specific subsystem requirements.

1. Propagation delay time based on a specified maximum number of logic levels.
2. Power input and voltage levels required.
3. Package type and estimated physical size.
4. Fan-out/in limitations.
5. Reliability — (projected failure rate).
6. Cost objectives.

The output of the "IC-Mix" analysis would be several subsystem configurations based on different IC combinations; thus the designer would retain as much flexibility as desired to interconnect various subsystems and thereby maximize the overall system requirements.

COMPUTER DESIGN

. . . . SOME PITFALLS TO AVOID

G. D. Smoliar, Staff Engineer, Electronic Data Processing Division, RCA, Camden, N. J.

To know about and to avoid some of the pitfalls facing the computer engineer can save both time and money. Certain blind alleys cannot be avoided, and certain unfruitful approaches may be profitable the second time around; however, this is a decision that the well-informed engineer can make most efficiently after reviewing prior art (both failures and successes). This article reviews and reflects on some engineering decisions of historical interest.

For more than twenty years, engineers have been writing articles about progress in digital computer development at an ever increasing rate. Milestone after milestone has been well-documented and the innocent reader might get the impression that mistakes were never made. Now, as a second generation (men, not computers) heads for the same blind alleys that were explored in the forties and the fifties, it is fitting to write about what we did wrong in those early days. This is not a record of what was done at RCA or is it confined to industry. Universities contributed their share of boners, and goofs were probably made all over the world, although this article is confined in scope to this country.

System Design

One of our first wrong assumptions was that punched cards were obsolete. We couldn't believe that people would continue to store, on twenty-square inches of card, information that would easily be accommodated by half a square inch of magnetic tape. Having convinced ourselves of this, we did not concern ourselves with the trivial problems of transferring data from cards to the computer: tape was the chosen medium. We then faced the problem of preparing tape directly from a keyboard. That problem is now solved; however, when the first business computers were being designed, such seemingly trivial details as back spacing and selective erasing made life miserable.

The original idea of manual preparation of magnetic tape for data input to a computer dates back to the first electronic business machines. It was dropped after a few years only to be revived recently, thus completing the full cycle.

Computer Organization

Megahertz pulse rates seemed so unbelievably fast that we convinced ourselves we had more computer speed than we could possibly use. This incorrect premise resulted in the equally wrong conclusion that only a pure serial machine was justified. All of the bits of a computer word flowed along a single path in sequence.

Later, when we began to realize the error of our ways the pendulum swung to the other extreme and pure parallel systems (whose costs were exorbitant) were the order of the day. It took approximately six years for the industry to realize there were advantages in a less extreme approach.

Memories

Probably no single element of the digital computer has been through as many upheavals as its main store. Some of the first machines, taking a cue from MTI (moving target indication) radar used mercury-column acoustic delay lines. Construction of these "tanks" never really advanced from art to science during the years

they were used. Now as we look back, they seem to have had every possible disadvantage: their attenuation was approximately 60 dB and the stored information was volatile (that is, it was lost when power went off). Furthermore with long lines in the pure serial machine one could easily spend more time in waiting for the information than in actual data processing.

Since the velocity of sound varies with the temperature of the medium and the coefficient is quite large for mercury, something had to be done to keep the number of pulses stored in a tank constant. An interesting wrong approach was AFC (automatic frequency control). The basic pulse rate of the computer could be varied to make the tank hold the correct number of pulses. Unfortunately, this solution did not account for the tanks being at different temperature! In due time, computers with constant-frequency oscillators and controlled heaters on the mercury tanks were designed and built.

The acoustic line has seen many improvements. Solid quartz has replaced the temperamental mercury, but long before that change these devices were abandoned by the computer industry.

A second attempt to solve the memory problem was the electrostatic storage tube. This barely got to be used before it, too, was replaced. In its most popular form, it was an attempt to store binary information as a matrix of two different types of charge patterns on the face of an ordinary cathode ray tube. Among its various disadvantages were the need for dangerously high voltage, extreme susceptibility to noise, and the requirement for precise deflection circuits in a system that otherwise contained no critical amplitude sensitive devices.

Probably the next main memory was the magnetic drum. This seemed to be a reasonable solution. It was non-volatile and inexpensive and its storage capacity was adequate. We told ourselves that by "minimum latency coding" (selectively placing the information in storage) we could program around the long wait for the right word to come up. If that had been true we might still be using drums as main memories. It was not, and we finally arrived at core storage.

Meanwhile, at the other end of the memory-size spectrum, the single-bit

storage element, the flip-flop, was being re-examined. It seemed extravagant to continue to use two tubes for this circuit which has not changed in the years since Eccles and Jordan. So, in the early fifties, the dynamic flip-flop or "Ring-around-the-Rosy" circuit came into use. It had a single tube which drove a one-pulse delay line whose output was returned to the tube input. Its two stable states were: no signal, and a steady stream of pulses. It was indeed a one-tube flip-flop. Unfortunately it had no other advantages. In fact, measured by the usual criteria of cost, speed and what we now call fan-out, it was decidedly inferior. It seems to have passed into oblivion.

The three-stable-state flip-flop should also be mentioned. Aside from being a departure from standards, there is nothing fundamentally wrong with this idea. In each computer there seem to be a few places where hardware could be saved with this gadget. Usually it does not pay to use it, because it is special; therefore it is discarded only to be reinvented on the next project! We have been down that road before, several times.

Circuits

Looking back, it could almost be said that the digital computer was developed too early. It certainly seems pathetic to have built those five-thousand-tube, fifty-kilowatt monsters (which frequently failed due to the failure of a single tube heater) while the transistor was just around the corner. Had we waited just a few years a lot of hardware that was doomed to obsolescence would not have been built. However, using tubes by the hundreds was not our only weakness.

For a while AC coupling was popular. This meant that because of capacitors, or similar interstage coupling elements, there was a lower limit to the frequency components of the signals we could transmit. We found ourselves in the ridiculous position of having to investigate, at each point in the equipment, the exact nature of the normal pulse pattern. Of course, failure to take into account the abnormal pulse pattern gave us a generous helping of trouble-shooting problems.

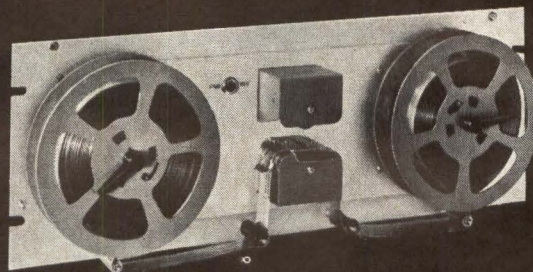
But in some ways our cure for this unfortunate situation was worse than the sickness. When we needed re-

NEW!



60 Series

Photoelectric Paper Tape Readers



LOWEST COST
RELIABLE PERFORMANCE
MINIMUM MAINTENANCE

General Electric's new, low-priced 60 Series photoelectric paper tape readers have only one moving part. Sealed bearings are used on the ultra-compact 60 Series readers and require no maintenance.

Simplicity is the key word in design and operation.

The GE 60 Series are fast. All units read asynchronously at up to 125 characters per second. Other features are:

- Silicon solid-state components used throughout
- Reads opaque and translucent tapes
- Simple loading
- No adjustments required
- Unidirectional and bidirectional models

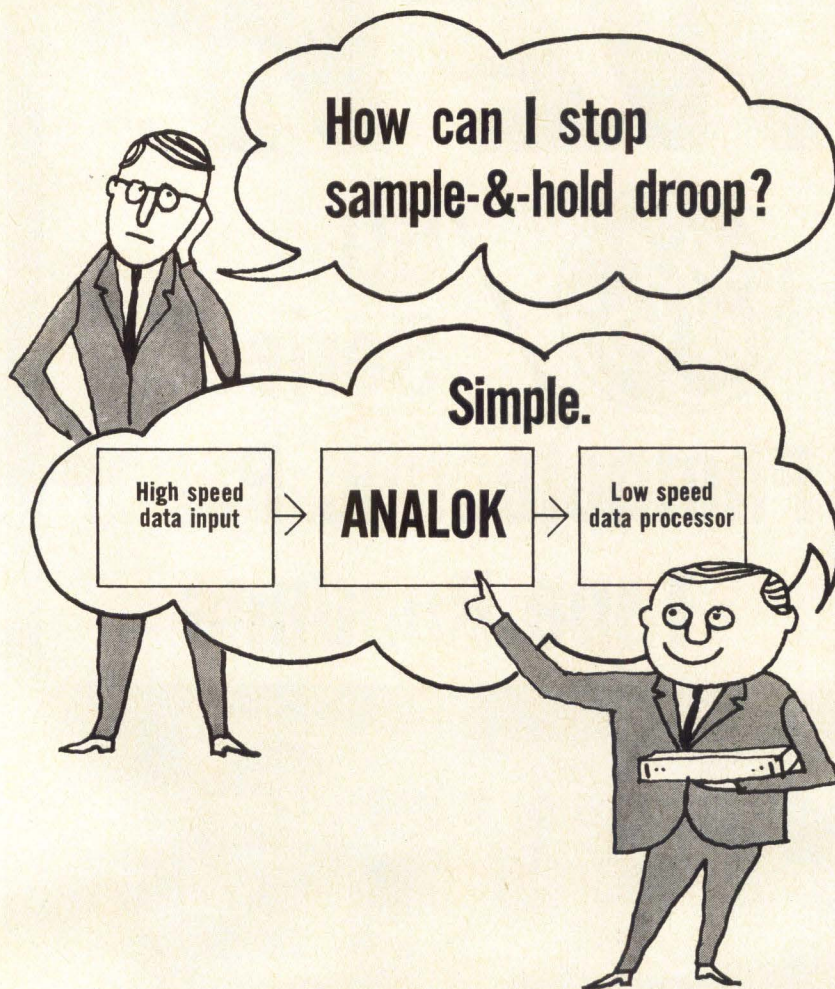
GE photoelectric paper tape readers are also available with matching reels. Get all the details on the GE 60 Series, write: Sales Manager, GE Printer-Reader Business Section, 511 N. Broad St., Philadelphia, Penna. Ask for GEA-8480. 837-01

PRINTER-READER BUSINESS SECTION

GENERAL  **ELECTRIC**

PHILADELPHIA, PENNA.

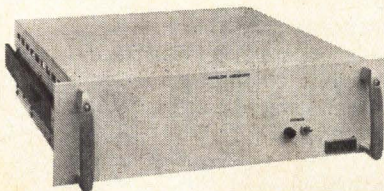
CIRCLE NO. 30 ON INQUIRY CARD



Forget about droop with ANALOK because it doesn't. What it *does* do is give you a simpler, less expensive system with greater flexibility.

Here's how. ANALOK is a multichannel unity gain track-and-hold amplifier with *zero* decay. It can retain stored values *in an analog state* indefinitely. This unique memory capability gives you greater flexibility because there's no time restriction between acquisition and use of sampled values. Check these applications:

- Use ANALOK as a high speed data buffer. Sample multiple functions simultaneously, or transient phenomena in a programmed sequence. Transfer the data to your low speed data processor as slowly or rapidly as you wish. No matter how much time you take, the stored values won't droop.
- Decommuration with one DAC and a multichannel ANALOK eliminates the need for periodic updating necessary when using conventional sample-and-hold channels. The result of using ANALOK is optimum use of your computer since it need only address each ANALOK channel when it has *new* information.
- Provide the information storage capability in your analog system with ANALOK. You may not have to go hybrid.



Get complete specifications. Write to ANALOK Sales, Dept. 223, Analog-Digital Systems Division, Control Data Corporation, 4455 Eastgate Mall, La Jolla, California 92037. Or phone 714/453-2500.

CONTROL DATA
CORPORATION

4455 Eastgate Mall, La Jolla, Calif.

CIRCLE NO. 31 ON INQUIRY CARD

sponse all the way down to DC we used direct-coupling; that is, input to a tube grid and output at a plate some sixty volts higher. If our logic took us through several of these stages we had signals whose base lines were hundreds of volts apart and our power supply requirements were such as to make strong men (and power supply designers) weep.

It is almost obvious that in this unhappy state standard circuits, as we now know them, were virtually non-existent. At times we seemed to have more circuit designs than tubes in those computers.

One interesting approach during the AC coupling, dynamic flip-flop days was based on maximum power output. Each device (tube, in this case) has a load impedance to which it will deliver maximum power. Therefore, computers were designed in which pulse transformers coupled the tube outputs to the low-impedance loads. (One part of that scheme is still in use.) It was realized then that the complement of a signal is used as frequently as the signal itself. For that reason each transformer had two secondary windings and the "barred" and "unbarred" signals were always available.

Another abandoned system was that of pulse magnetic amplifiers. After we tired of constantly replacing burned out tubes and before transistors were adequate and inexpensive, magnetic amplifiers were given a whirl. These tape-wound toroids could be set to "positive" or "negative" remanence by the signal. Then a power pulse interrogated the core. Depending upon the polarity of the state in which it had been left, it looked like either a high or a low impedance to the power pulse. This device amplified, delayed, and, if necessary, inverted the signal. Combined with diode gating it provided all necessary logic functions. Unfortunately it was slow (under 1 MHz) and expensive. As transistor prices decreased and speeds increased, the pulse magnetic amplifier went out.

Human Engineering

During the design of the first computers, the engineers watched for all places where manual switches would be helpful in trouble-shooting. They also looked for points in the circuit whose state could be observed with

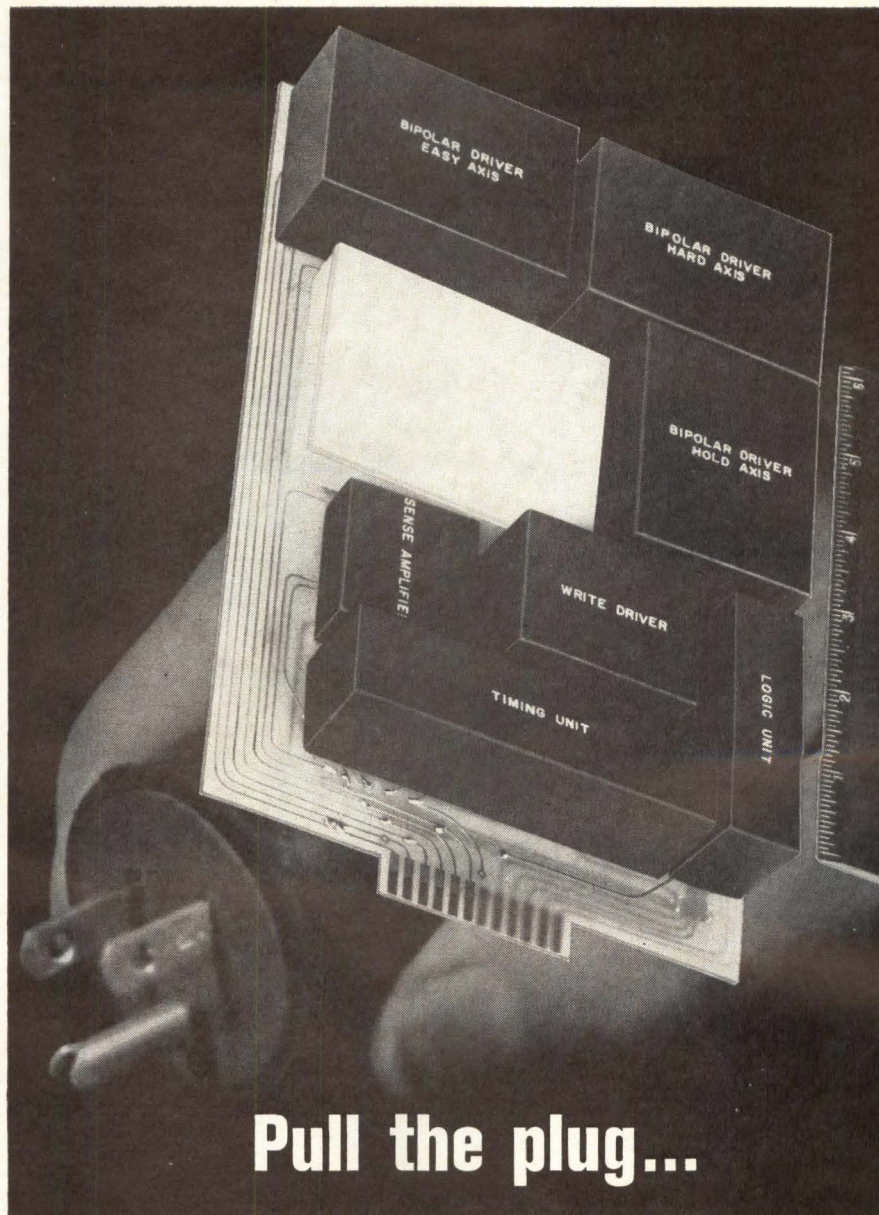
indicator lamps. For example, all of the bits of the instruction being executed were brought out to energize neon bulbs, and at each lamp a lever switch could modify that bit (before the era of the lighted pushbutton) and could even fix its state to prevent its being changed in the course of the program. This collection of lights and switches told the operator everything he needed to know and maybe even more. The console became so big that it became impossible to keep track of everything that was displayed. Furthermore twenty-five square feet of that sort of complexity could frighten away prospective customers who were looking for machines that their clerical employees could master.

The pendulum swung and simplicity became the key word. The designer was permitted to use no more than a dozen lights and switches. He took advantage of the fact that several functions could be combined in one illuminated switch assembly; nevertheless, there was considerable overflow from the simple console and so the "maintenance panel" was born. In theory, this second panel displayed information that would only interest the repair man; in fact, the operator learns to use every control and indicator that is available and regardless of popular opinion, they make his job easier.

Conclusion

It seems that computer designers in the past would frequently take an extreme position and stick with it until forced to change. This article is a plea for moderation. Product design is not so simple that it is governed by universal truths.

Another lesson can be learned from this brief account: we frequently become so enamoured of our own ideas and value originality so highly that we neglect to study the past. Engineers could think even before the days of the sampling scope. Use what is good even if it is old and try to avoid making the same mistakes that have been made before. I do not say that every abandoned idea is now worthless. The important point is to know why certain approaches were tried and dropped. Then you will be able to consider them as possible solutions to new problems when many of the old restrictions may have disappeared.



Pull the plug...

The New DTPL* Shift Register won't lose your data

The unique LFE Model 1487 Shift Register retains information even if the input power should fail. It is also capable of functioning without standby power. Its quiescent condition draws only 1.2 watts. Actually, the lower the bit rate the lower the power drain.

Data can be fed and stored in the Model 1487 at rates down to, and

even below, one bit every eight hours . . . and up to as high as 250,000 bits per second.

Voltage transients or electrostatic charges have no effect on the shift register, so that burn out or failure due to these maladies are virtually eliminated. Get full technical information by writing or calling Product Manager, Commercial Products.

* The new Model 1487 Shift Register uses a thin magnetic film process, Domain Tip Propagation Logic, which makes it non-volatile.

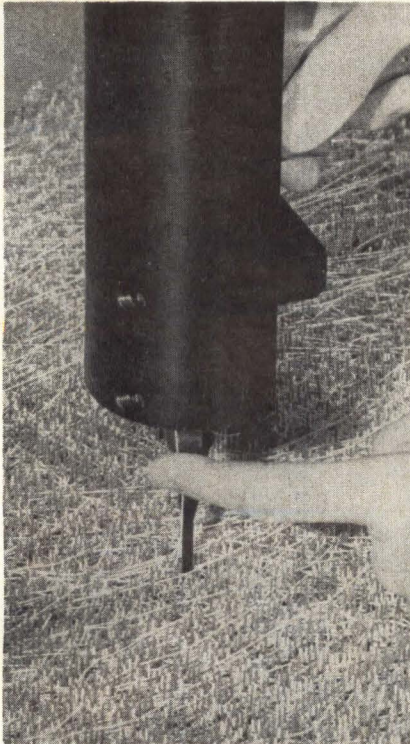


ELECTRONICS DIVISION

A Division of Laboratory for Electronics, Inc.
1075 COMMONWEALTH AVE., BOSTON, MASS. 02215
CIRCLE NO. 32 ON INQUIRY CARD



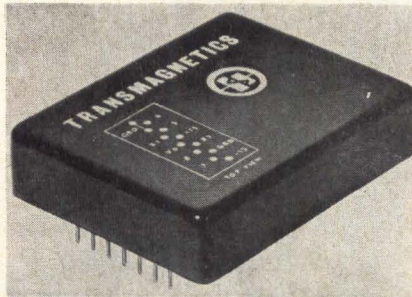
NEW PRODUCTS



POINT-TO-POINT WIRING SYSTEM

Increased reliability and reduced production costs are said to be now possible by a new point-to-point, operator-actuated wiring system. Automatic positioning with pre-programmed tape instructions eliminates positioning error and is said to increase wiring production over 700% compared to manual techniques. Features of the system designed to give users maximum production flexibility include: choice of wire wrap or termpoint connection techniques; use of solid stranded tinsel and printed wire twisted pairs; color coding; and either path or true point-to-point wire routing. Two hundred wires per hour is a reasonable production rate and "up-time" is assured through simplicity of design, combined with a rugged low-friction system. Product Improvement Corp., Santa Ana, Calif.

Circle No. 215 on Inquiry Card



ANALOG MULTIPLIER

A recently introduced analog multiplier, model 384, that offers a frequency response of DC to 4 MHz makes possible performance and economies not previously achieved in multiplexing telemetry data, video signals and scope presentation drives.

Gain of the new unit is flat to 0.8 db at 1 MHz and 3 db at 4 MHz. Phase is less than 1° at 1 MHz and 30 degrees at 4 MHz. Other specifications include: input level, both inputs: 0 to ± 10 V; input impedance: 10 K ohms resistive shunted by 50 pf max.; output: ± 1 V into 1 K ohms min. resistive, 20 pf max.; linearity $\pm 1\%$ FS; operation is over 0 to 70°C. Transmagetics, Inc., Flushing, N.Y.

Circle No. 217 on Inquiry Card

SOCKET FOR 16 LEAD PLUG-IN IC'S

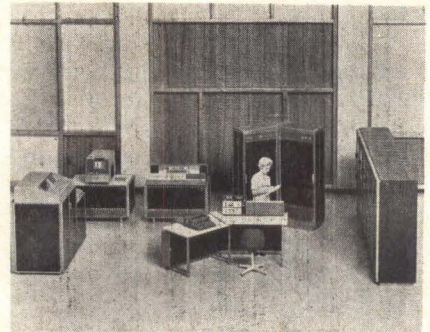
New 16 contact low profile printed circuit socket permits packaging on $\frac{1}{2}$ inch centers. Socket terminals have same dimension as IC leads. The socket accepts packages with flat or round leads. Wiping type beryllium copper contacts permit easy IC insertion. Available in Diallyl Phthalate or black phenolic with gold or tin-plated contacts. Dimensions: .89L x .49W x .31H. Price Range: \$.32 to \$.83 each, depending on quantity and type. Augat Inc., Attleboro, Mass.

Circle No. 209 on Inquiry Card

TEST PROBE RECEPTACLE FOR P.C. CARDS

Series 6505 is a test probe receptacle designed for p.c. board mounting. Incorporating 18 jacks on 0.125" centers, the receptacle provides convenient multiple test points on the p.c. board and facilitates monitoring, testing, and troubleshooting circuit operation. The jacks, made of phosphor bronze with gold flash over nickel underplate, are rated at 5 amps. They accept .040" diameter test probes and have tabs for soldering directly to p.c. pads. The insulator, made of glass-filled nylon, is 3" x .385" x .350", and has two .065" mounting holes. Elco Corporation, Willow Grove, Pa.

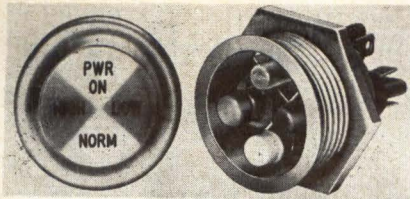
Circle No. 200 on Inquiry Card



MEDIUM-SCALE COMPUTER

The GE-405, recently announced as the latest and smallest member of the GE-400 "family" of medium-scale computers, is said to afford exceptional growth potential by permitting users to "build" their computer installations as their workloads increase. As the user feels a need for more memory and/or faster processor speeds, he may move upward to one of the other, larger members of the GE-400 series. If his needs include time-sharing, he may move into GE's newly-announced GE-420 time-sharing system. Programs produced for any of the GE-400's are fully operational on larger systems in the family. With a memory capacity of 8,000 words (32,000 characters) and an access speed of two microseconds, the GE-405 leases for approximately \$5,120 a month and sells for about \$196,420. Availability of the GE-405 is 4 months, with first deliveries scheduled for February, 1968. General Electric, Phoenix, Arizona.

Circle No. 223 on Inquiry Card



SEGMENTED INDICATOR LAMP

A four-lamp indicator with a 1" diameter lens, which can provide up to four different messages on a single face, now replaces four single-bulb indicators. Each S600 unit consists of a housing in which four separate and independent sockets are mounted. Partitions in the lens cap provide for the segments. The unit mounts in a 1 3/8" dia. hole and bulbs are replaceable from the front. Lamp bulbs are available from 6V. to 120V., eliminating the need for external voltage dropping devices. Use of colored silicon rubber filters furthers the design possibilities. The H. R. Kirkland Co., Morristown, N.J.

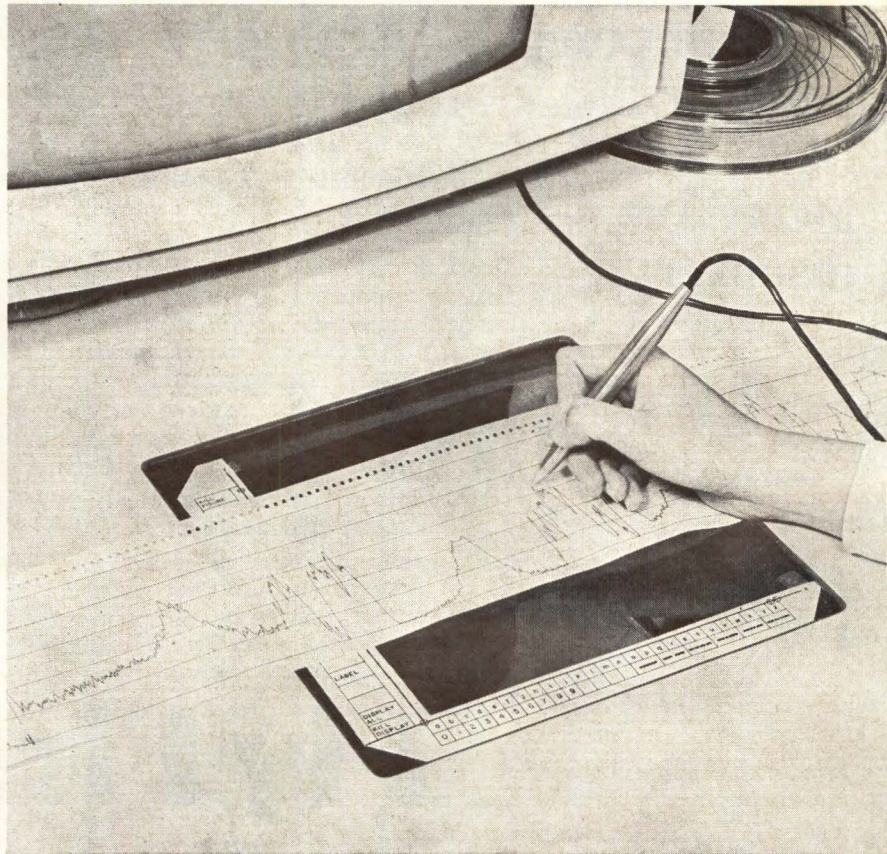
Circle No. 222 on Inquiry Card

DUAL TT_μL FLIP-FLOP

A dual TT_μL flip-flop microcircuit for military and industrial systems that require more than two flip-flops is now available for general purpose storage, shifting and counting registers and other applications where high speeds are necessary. Called the 9020, it is actually a dual design of Fairchild's well established 9001, featuring a common clock, separate J, K, \bar{K} inputs and 50 MHz operation. A member of Fairchild's CCSL family (Compatible Current Sinking Logic), the new unit offers advantages over competitive products by reason of its high speed performance, its logic flexibility and its drive capability. It has a common J-K input that can be used for gating clock waveforms and can result in an improved logic design by minimizing clock skew problems. Other features of the element include a master-slave design, input-diode clamping, and a type "D" capability. The 9020 is available off the distributor's shelf in a ceramic Dual-In-Line package, hermetically sealed. Fairchild Semiconductor, a division of Fairchild Camera and Instrument Corporation, Mountain View, Calif.

Circle No. 212 on Inquiry Card

here's a quick and simple way to graphically input data into your computer...



it's called GRAFACON and here's how it works...

Place a chart—a sketch—or project from the rear on GRAFACON's 10" x 10" surface (which has a built-in 1024 x 1024 matrix for 100-line-per-inch resolution), trace it with GRAFACON's stylus, and GRAFACON converts the stylus position to 20 bits of X and Y coordinate data ready for computer processing. Or, digitize as you sketch at 45 inches per second. GRAFACON is a production version of the famous Rand tablet, and operates directly on/line or off/line.

GRAFACON accessories include keyboards—for annotating data, CRT displays—for monitoring, off/line tape and card converters, and on/line converters for most computers, including System 360.

We have a technical brochure and applications data on dozens of GRAFACONS in use today; yours for the asking—just write to:



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DATA EQUIPMENT DIVISION

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CIRCLE NO. 33 ON INQUIRY CARD

**Any day now
you computer
people will
make an
incredible
discovery:**



Nobody has made custom power supplies longer than Varo.

Or with a better performance record.

Or to tougher mil specs. Funny we haven't crossed paths with you folks.

Funny?
It's incredible!
Let's discover each other.
Write Rex Carter, Varo, Inc., Static Power Division, 1600 Dallas North Parkway, Plano, Texas 75074.
TWX 9108605640



CIRCLE NO. 34 ON INQUIRY CARD



PUNCHED TAPE DIGITIZING SYSTEM

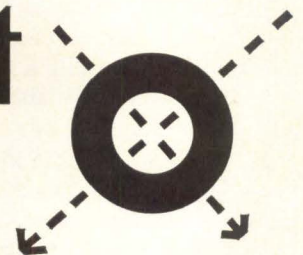
A graphical input system recently developed for off-line digitizing of graphic data from strip chart records, topographic maps, etc., or from projected slide or film images — where batch processing of data is desirable — consists of a Grafacon 1010A digital tablet — a 10¼" square (104 sq. inches of surface area) production version of the famous RAND Tablet graphic input device — with a pen-like stylus, and a tape punch and associated electronics. In operation, the data to be

digitized is placed or projected on Tablet surface and pinpointed with the stylus. The position of the stylus is digitized to a precision of 10 X bits and 10 Y bits. The stylus position information and any identification characters are then processed and punched on an 8-level tape for future computer processing.

Called the Grafacon 206-1, the system operates in either point or continuous trace modes. In the point mode, data indicated by the operator are digitized as discrete points each time the stylus is depressed; in the continuous-trace mode, the system continuously digitizes the stylus position as it is moved. Data screening allows the system to record up to 30,000 X-Y coordinate pairs on 1,000 feet of tape. Resolution is within 0.005 inches. A unique feature of the system — an audible or light indication warning that automatically occurs if an error is made inputting graphic data — allows the 206-1 System to be operated by an untrained operator. Bolt Beranek & Newman/Data Equipment Div., Santa Ana, Cal.

Circle No. 219 on Inquiry Card

Fly First Class at Tourist Prices



WITH A RAYTHEON MEMORY...

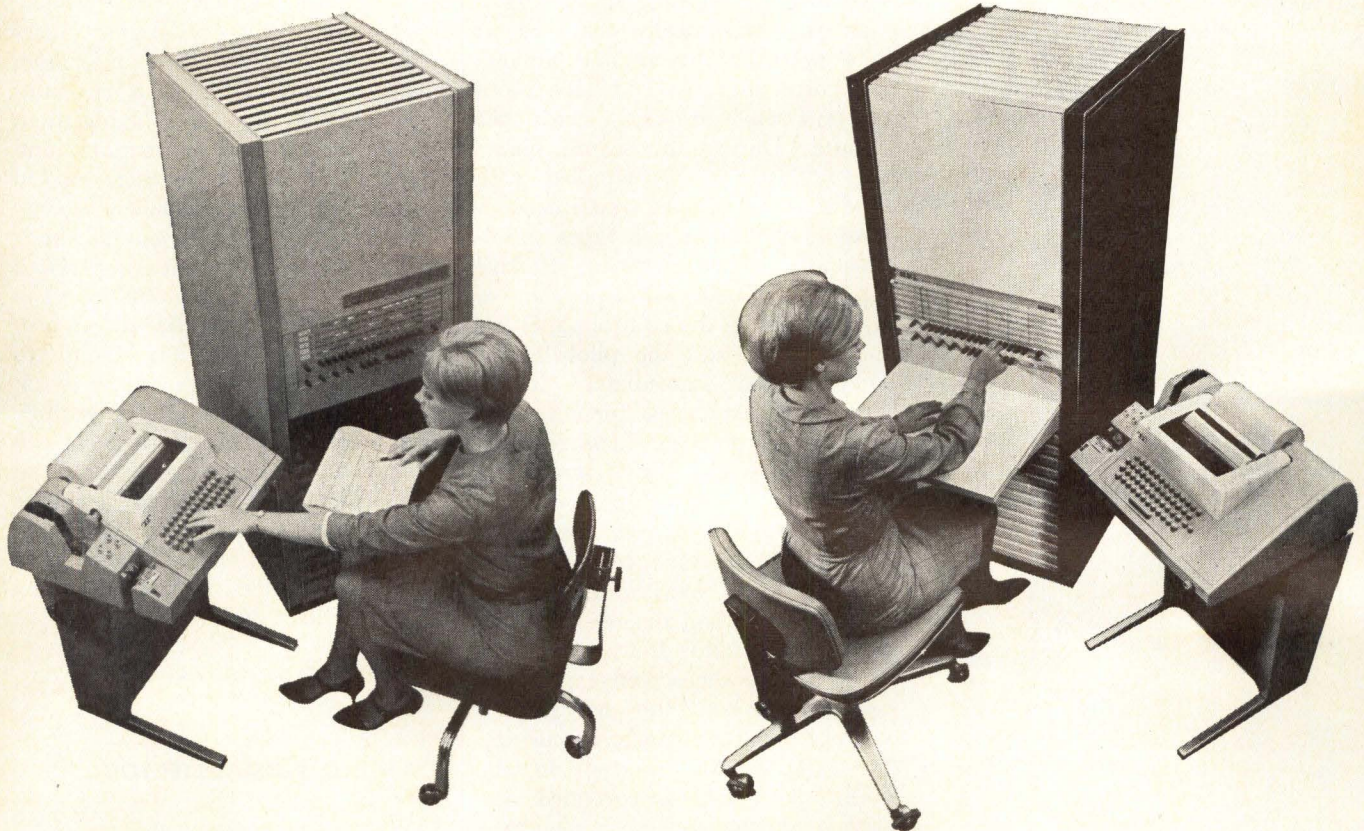
Raytheon Computer's new Model 300 memory is now available at more attractive prices and in a wider range of sizes due to expanded production capacity. ■ The Model 300 is a 2½D core memory with full cycle time of 900 nanoseconds. Typical access time is 350 nanoseconds. A single vertical drawer houses a complete memory module including stack and electronics. There are two basic modules—8K by 36 bits and 16K by 18 bits—and memories up to 8K by 144 bits or 16K by 72 bits are readily assembled. Best of all, production units will soon be available on a 60-90 day basis. ■ Complete technical, pricing and delivery data is yours in not quite 900 nanoseconds, but almost as fast. Write or call today. Raytheon Computer, 2700 S. Fairview St., Santa Ana, California 92704. Phone (714) 546-7160.



CIRCLE NO. 51 ON INQUIRY CARD

**Anything
the SEL 810A
can do,**

**the new
SEL 810B can do
twice as fast.**



Over 50 SEL 810A, 16-bit computers have been supplied for data acquisition and control. Now meet the SEL 810B, with twice the speed of the A. Yet only about 20% more in price. Same great features: all integrated circuits, 2 levels of priority interrupt, memory expandable to 32K, I/O typewriter, high-speed hardware multiply and divide, and real-time I/O structure. And the software package of the 810B has been proven in the A.

Fixed point execution times of the B are: add/subtract—1.58 microseconds; multiply—4.74 microseconds; divide—6.32 microseconds; cycle time—790 nanoseconds. If you don't need the speed of the SEL 810B, buy the A. For either, call or write: Systems Engineering Laboratories, 6901 West Sunrise Blvd., Fort Lauderdale, Fla. 33310. Area Code 305 587-2900.

Systems Engineering Laboratories

At high frequencies, modern computers require coaxial cable that can take a lot of physical punishment and still give consistently top performance, without break-down or need for repair. But ordinary multi-coaxial cable can only withstand 5,000 flexures. However, Times has designed a special cable that has passed 90,000 flexures without breaking and still performs at top reliability.



To find out what Times Multi-conductor Coaxial cable can do for your computer, write or call our Product Engineering Dept.

TIMES
WIRE & CABLE
DIVISION OF THE INTERNATIONAL SILVER CO.
Wallingford, Conn.

CIRCLE NO. 36 ON INQUIRY CARD

PAPER TAPE SYSTEM

A new tape system permits quick changes in teletype messages at torn-tape communications centers. The Model 6704 Tape Recall Unit permits the operator to locate a specific message within a reel of tape, display the message on a CRT screen for visual checks, add a pilot header if required, enter any corrections or additions and make a perforated copy for retransmission of the message to the requesting station. The tape is automatically searched at 3000 words a minute and, following corrections, is punched out on new tape at 1200 words per minute. During the search phase, the system can be supplied with tandem read stations which make it possible to search two tapes simultaneously. This gives an effective input rate of 6000 words per minute. A keyboard on the control panel lets the operator add the pilot header to the message immediately. It also gives him fast access for inserting, deleting or correcting message characters. The CRT display screen has a capacity for 416 message characters. When a desired message is located on the tape reel, the first 256 characters immediately appear on the screen and the operator can subsequently add 160 more characters before the screen capacity is reached. When the operator is satisfied with the message, he punches the "MESSAGE" button on the control panel and the corrected message is punched out on a new tape for retransmission. Radiation Inc., Melbourne, Fla.

Circle No. 253 on Inquiry Card

POWER SUPPLIES

Two new high power output, low voltage supplies feature remote programming, remote error sensing, and low output impedance. Transient recovery time is less than 50 microseconds to within 10 millivolts. The new models include internally-adjustable pre-regulator voltage limit and continuously-variable output voltage and current with no range switching. They also feature automatic restoration of normal operation following removal of overload, constant voltage/constant current

operation with automatic crossover, front panel coarse and fine voltage, and current controls. Output voltage ranges from 0-10 to 0-60 and output current ranges from 0-3 to 0-100. Hewlett-Packard/Harrison Division, Berkeley Heights, N. J.

Circle No. 214 on Inquiry Card

MICROMINIATURE CAPACITORS

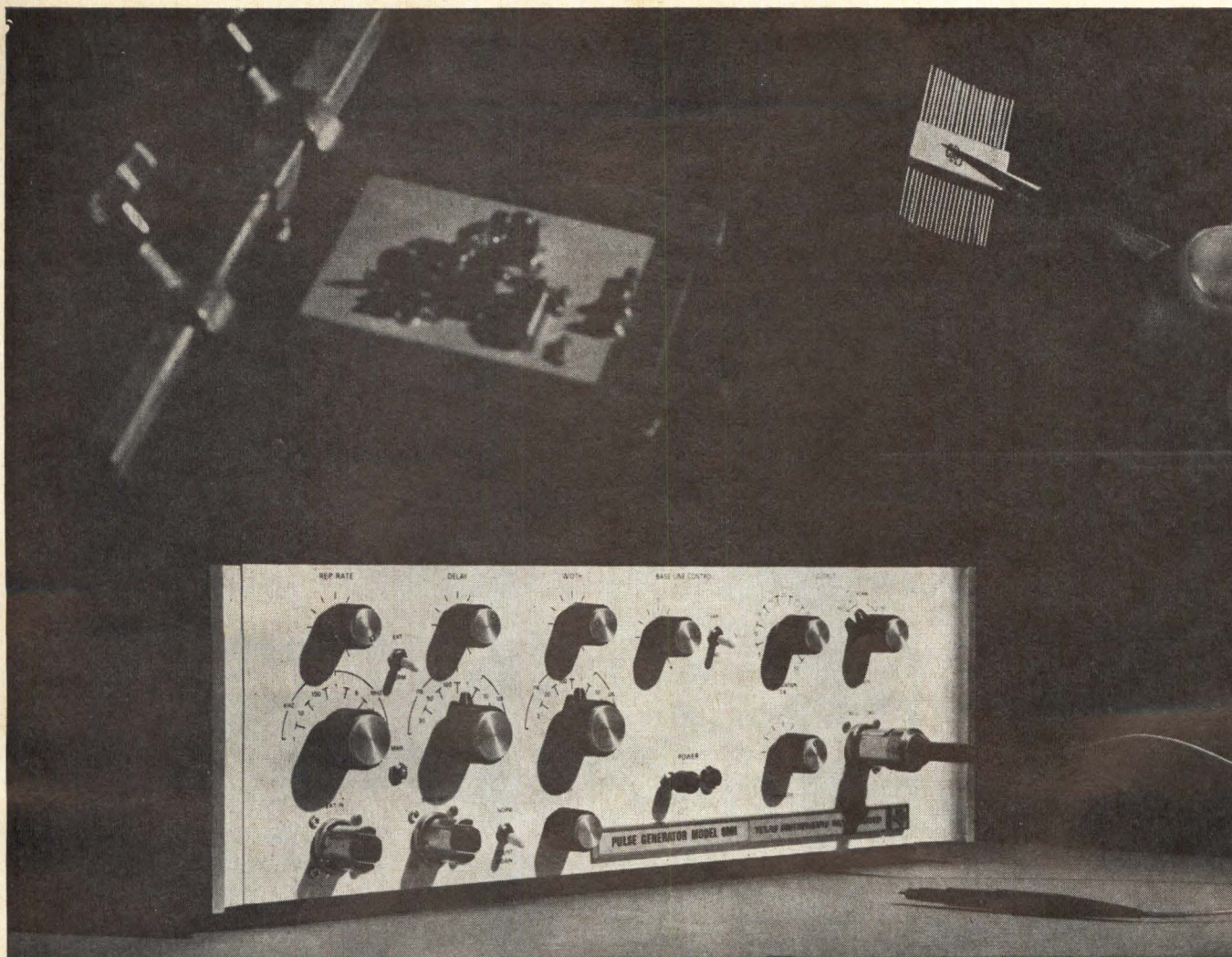
Microminiature epoxy-coated capacitors are said to offer maximum volumetric efficiency. The new units are designed for use in applications where space is at a premium and where the use of the more rugged molded styles are precluded because of size. The basic monolithic body of the units is inherently impervious to moisture and contamination. The epoxy coating provides added protection during handling. Units are available with voltage ratings of 25, 50, and 100 and are offered in three temperature coefficient ratings with capacitances ranging from 0.5 to 340,000 pF. The units range in size from 0.135" x 0.060" x 0.040" for the smallest to 0.225" x 0.065" x 0.060" for the largest. Aerovox Corp., Olean, N.Y.

Circle No. 274 on Inquiry Card

MISSING PULSE DETECTOR

Designed for breadboard and final system applications, a new circuit module delivers a fault pulse whenever a system or subsystem pulse repetition frequency drops below a predetermined threshold frequency. The lower threshold is 200Hz for an unmodified module. However the module can monitor system/subsystem pulse frequencies down to 100 Hz quite easily, by the addition of an external capacitor. Alternatively, the monitoring threshold of the module can be raised up to 15,000 Hz by the use of an external resistor. Other pertinent specifications include a pulse signal input of 2 to 5 volts at 0.5 microseconds or greater; fault pulse output of +3 volt peak (min.) with pulse width of 0.4 microseconds at the 2 volt level. MCG Electronics, Bay Shore, N.Y.

Circle No. 218 on Inquiry Card



Why You Need a Special Pulse Generator for State of the Art Circuit Design



With high speeds and critical design parameters, you need the best test instruments to be sure your designs will be optimum. The TI Model 6901 Pulse Generator gives outputs from 1 KHz to 0.1 GHz; independent amplitude and baseline controls; jitter less than 0.1% of period + 50 psec; and countdown synchronization output.

The 6901 makes your designing simpler, too. Because the pulse amplitude of the generator can be changed without affecting DC offset, you can use the offset instead of an external bias supply for your circuit.

All this, and a price of only \$1950. For more information, contact your TI Field Office, or the Industrial Products Group, Texas Instruments Incorporated, P. O. Box 66027, Houston, Texas 77006.

TEXAS INSTRUMENTS
INCORPORATED

CIRCLE NO. 37 ON INQUIRY CARD

827

63

Bargain price memories for people suspicious of bargains



Data Disc can deliver this 6,400,000-bit disc memory for \$6,400 when you buy ten, \$7,400 when you buy two, and \$9,400 for one alone.

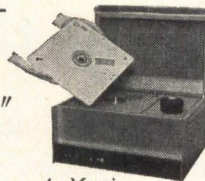
We can offer this low price per bit without sacrificing quality because our "in-contact" recorders store twice as many bits per inch as older "floating head" recorders. We don't try to cut the cost of discs, drives, heads or electronics. All components are built for maximum reliability—and cost accordingly. But simply because it takes fewer components to store any given number of bits, you get the storage capacity you need at a lower cost.

The F-series head-per-track system pictured above comes with storage capacities of 6.4, 3.2 and 1.6 million bits. It has an average access time of 16.7 ms, and stores 100,000 bits on each track —

enough to fill the core memory of a small computer. Data can be entered and retrieved very rapidly — at three megabits per second. And the whole system fits in $8\frac{3}{4}$ " of rack space.

When a large data library is needed, we supply an interchangeable-disc memory system with an average access time of $\frac{1}{3}$ second. Each disc, which holds 13,000,000 bits, is permanently encased in a protective cartridge so you can store as many discs as you need.

For complete information contact Data Disc, Incorporated, 1275 California Ave., Palo Alto, California 94304. Phone (415) 326-7602.



An M-series interchangeable-disc system.



DATA DISC

CIRCLE NO. 38 ON INQUIRY CARD

NATURAL BINARY ENCODER

Parallel natural binary encoder system uses a photoelectric absolute position, direct reading, single-turn encoder with a lamp life in excess of 50,000 hours. The new system has a capacity of 11-bits per turn, outputs compatible to most integrated circuit logic, and requires only two supply voltages including the lamp voltage. Specifications include +4.5vdc $\pm 0.5v$ for a binary "1", output impedance 6000 ohms, 0.5vdc or less for a binary "0" with a maximum sinking current of 7.0ma. Power requirements are +5vdc $\pm 5\%$ at 410 ma nominal. Baldwin Electronics Corp., Little Rock, Ark.

Circle No. 205 on Inquiry Card

MERCURY-WETTED REED RELAYS

New mercury-wetted miniature reed relays in low profile modular printed circuit packages are rated 28VA maximum at 1.0 ampere maximum or 100 VAC maximum, resistive load. Life expectancy is 25 million operations at rated load. Operate time and release time are 1 millisecond (average) with no contact bounce. SPST-NO packages are $\frac{3}{8}$ " above circuit board x $1\frac{1}{8}$ " x $13\frac{32}{32}$ "; DPST-NO packages are $\frac{3}{8}$ " x $1\frac{1}{8}$ " x $39\frac{64}{64}$ ". Class 131MPC SPST-NO and DPST-NO Relays are stocked for immediate delivery with operating coils for commonly used DC voltages. Magnecraft Electric Co., Chicago, Ill.

Circle No. 243 on Inquiry Card

IC TEST SYSTEM

A new IC test system performs pulse, dc, and function tests. Simplicity of operation is a key feature: test programming is accomplished with a digit switch register that selects the matrix connections, and a series of programmable pushbuttons. Most tests require less than 60 seconds. The system also features power supply accuracy of 0.1% ± 1 mv. Measurement accuracy of 1% is provided in the standard unit and 0.1% with optional digital readout. Redcor Corp., Canoga Park, Cal.

Circle No. 264 on Inquiry Card

HIGH-SPEED CORE MEMORY SYSTEM

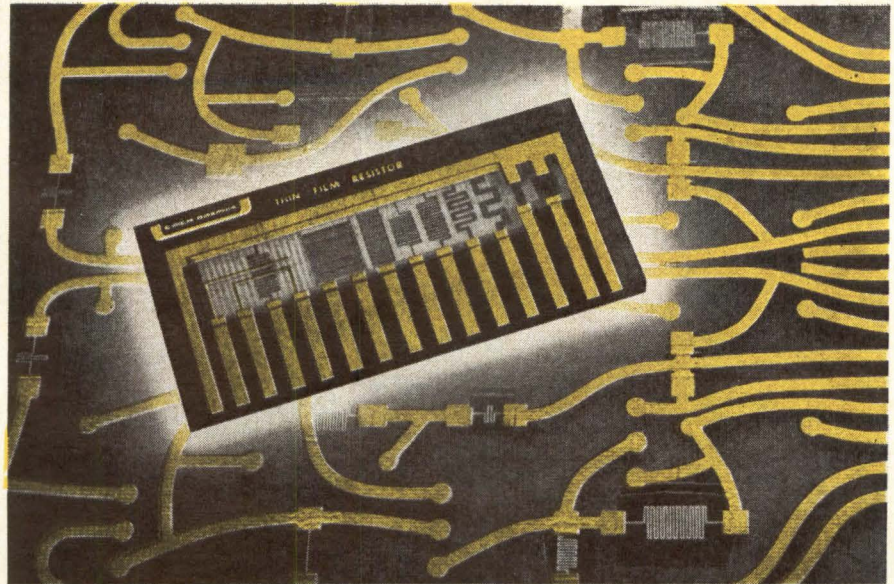
Versastore II, the newest addition to Varian Data Machines' computer memories, is said to be faster, smaller, more reliable, and substantially less expensive than previous models. It operates asynchronously at 1.7 microseconds with 750 nanosecond access time. Improved packaging design packs 50% more core memory in the same 5¼" rack-mounted package. It is available in increments to 4096 words of 36 bits, and can also be provided as an 8K word memory of up to 18 bits. Several options are available: party line — which enables basic Versastore memories to be used in multiples, a built-in self-test feature for quick and easy testing of memory contents and operation, and a variety of timing and control flags. Designed for high reliability, it uses integrated circuits and silicon components. Short-circuit-proof test points are provided. Varian Data Machines, Newport Beach, California.

Circle No. 203 on Inquiry Card

SQUARE LAW FUNCTION GENERATOR

A simple, accurate and economical device for obtaining a large class of nonlinear mathematical functions when employed as an input or feedback element with conventional, high-gain operational amplifiers was recently announced. The device, called the Quadratron, represents over a decade of experimentation and research into the unconventional electrical characteristics of silicon carbide. The 10-volt version, measuring 5/8" diameter and 21/64" high, and the 100-volt version, measuring 5/8" diameter and 35/64" high, provide low-cost application over a wide dynamic range. They require no reference voltages, are bi-directional and provide origin symmetry and zero output for zero input. The Quadratron is capable of generating a variety of functions, including square root, sine, cosine, tangent and many more. Bourns, Inc., Riverside, California 92507.

Circle No. 208 on Inquiry Card



Now... Thin Film Resistors from Cinch-Graphik

Now you can order thin film resistors as an integral part of the world's finest printed circuits. This Cinch-Graphik innovation offers packaging design flexibility and economy never before possible. These electronically deposited resistance patterns are only 2 millionths of an inch thick. They occupy virtually no space, weigh practically nothing, and are competitive in price and performance with discrete resistors. In addition, Cinch-Graphik's thin film resistors are stable, reliable and have electrical characteristics as good as ordinary resistors. Available in resistance values from 10Ω to 150KΩ, these resistors can be utilized in single or multilayer circuits on standard printed circuit laminates. Other components or conductor paths can be placed directly on top of the thin film resistors.

Specifications:

Value Range on Single Resistivity	10 ohms-150,000 ohms	(5000 hours @ 75°C @ 2 watts/in ²)	Drift	always positive
Sheet Resistivity	10 ohms-50 ohms/sq.	Resistor line width and spacing		Less than 2%
Resistor Tolerances	5%, 10%, 20%	Resistor thickness		5 mils min.
Temperature coefficient of Resistance	+80 ppm	Power dissipation		600 angstroms @ 50 ohms sheet resistivity.
				2-4 watts/in ²

For additional details or specifications, call, write or wire:

CINCH-GRAFIK

DIVISION OF UNITED-CARR

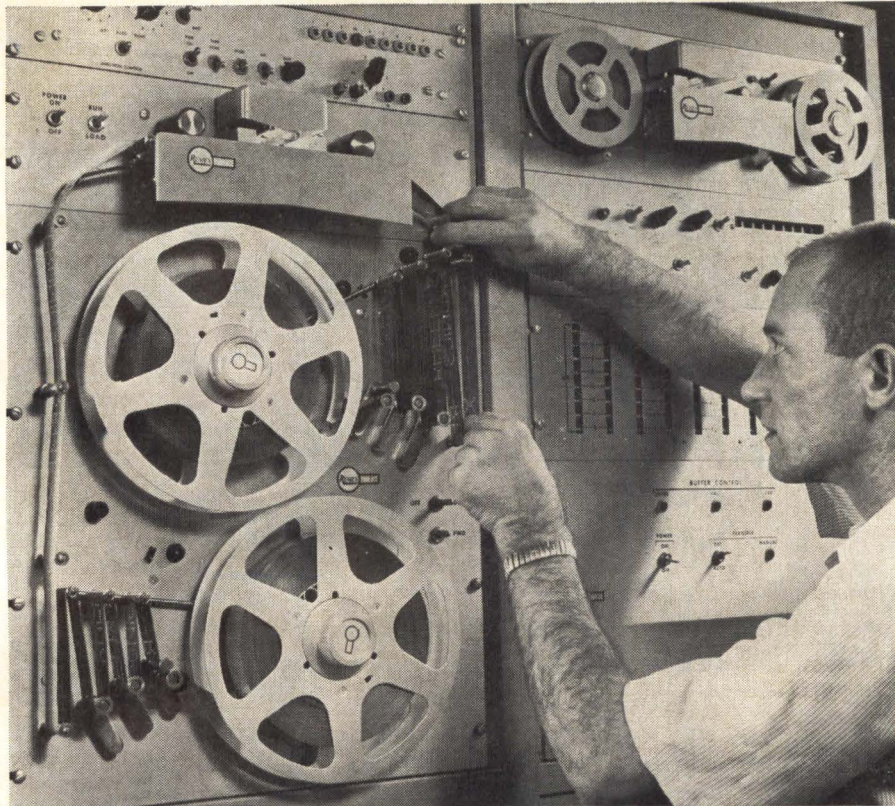


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REMEX ELECTRONICS

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CIRCLE NO. 40 ON INQUIRY CARD

COUNTER/REGISTER MODULE

A new 8-bit, 10 megacycle IC digital logic module was designed for implementation of independent or time-shared counter/registers. With back panel connections, the module functions in any one of 14 modes including: storage register; parallel or serial, in or out shift register; and reversible up or down counter, binary or BCD. Other modes include dual 4-bit combinations of shift, count, and store. Functions can be changed under logic control with no loss of data. Scientific Data Systems, Santa Monica, Cal.

Circle No. 273 on Inquiry Card

DIPPED SOLID TANTALUM CAPACITORS

A new polar solid tantalum capacitor uses a dip coated, high moisture resistant, hard epoxy encapsulation process. Leads spacing is 0.200 and 0.250 in straight leads for point-to-point wiring and in preformed stand-off leads for easy mounting on printed circuit boards. The capacitor is available in working voltages of 6 (330uf maximum), 10, 15, 20, 25, 35, and 50 (15uf maximum) volts. Units operate from -55°C to $+85^{\circ}\text{C}$, with no voltage derating. Positive polarity identification is printed on the capacitor. Union Carbide Corp., Electronics Div., Long Island City, N.Y.

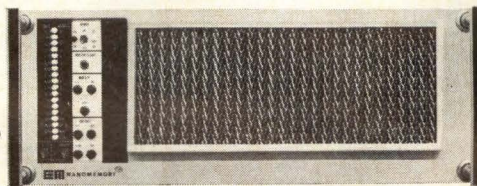
Circle No. 207 on Inquiry Card

IC OPERATIONAL AMPLIFIERS

A new series of hybrid integrated circuit operational amplifiers was designed so that low noise input stages, internal frequency compensation, and excellent thermal characteristics are an integral part of the unit. All of them are also completely short-circuit-proof so that any lead can be shorted to any other without danger of damage to the component or its circuit. Open-loop gain is to 100,000 min; temperature range is -25°C to $+85^{\circ}\text{C}$; noise voltage is 5 uv, max. A high-gain unit offers an open-loop gain of 200,000, min with a gain bandwidth product of 2MHz. Ampere Electronic Corp., Slatersville, R. I.

Circle No. 201 on Inquiry Card

**This new memory may not
do everything better.
But it does everything.
And it takes up
less space doing it.**



All together, the specs on our medium capacity memory systems are unsurpassed. Some systems may have slightly faster cycle times, but they don't offer speeds of 650 nanoseconds in a unit that's so small you'll be surprised to find a power supply and tester also included—just like the I.C. electronics and 2½ D magnetics. All are contained in only 2⅝ cubic feet (7"x19"x21.5").

Capacities range up to 295,000 bits per unit. Multiple module capability is available for larger capacity requirements.

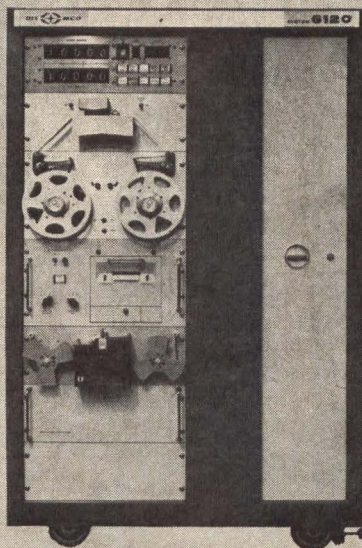
Compact as it is, the design doesn't get in the way of maintenance. The systems are extremely easy to repair. Stacks, electronics and tester are on plug-in modules—all are accessible and slip in and out easily.

Information on both the Nanomemory 2650 (650 nsecs cycle time) and Nanomemory 2900 (900 nsecs) are in our compact (8½x11") brochure. Write for Litpak 200.

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CIRCLE NO. 41 ON INQUIRY CARD



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CIRCLE NO. 42 ON INQUIRY CARD

CARD READER

An electronic control card reader for automated special machine and process control, data processing, and simulator control applications, translates pre-punched, programmed cards into the desired electronic readout. It has a capacity of 200 terminals which can be pre-wired and bussed in any number of combinations to meet specifications. Bifurcated, gold-plated beryllium copper contact springs are precisely positioned in glass reinforced diallyl phthalate molding blocks containing 25 spring contacts each. Assembled blocks are located above the cam operated card tray and printed circuit board in the lower housing. Number of assembly block segments can be increased to any suitable quantity. Flexible construction permits many variations that can accommodate unlimited card reader requirements. Continental Connector Corp., Woodside, N.Y.

Circle No. 276 on Inquiry Card

HIGH-SPEED CORE MEMORY

Versastore II, a new high-speed core memory system to be displayed at the Fall Joint Computer Conference in Anaheim in November, is said to offer higher speed, smaller size, and higher reliability than Versastore I at substantially lower costs. It operates asynchronously at 1.7 microseconds with 750 nanoseconds access time. Improved packaging design packs 50% more core mem-

ory in the same 5¼" rack-mounted package. Available in increments to 4096 words of 36 bits, the system can also be provided as an 8K word memory of up to 18 bits. Several options are available: party line — which enables basic memories to be used in multiples, a built-in self-test feature for quick and easy testing of memory contents and operation and a variety of timing and control flags. Designed for high reliability, Versastore II used integrated circuits and silicon components. Short-circuit-proof test points are provided. Varian Data Machines, Newport Beach, Cal.

Circle No. 213 on Inquiry Card

LIGHTED PUSHBUTTON SWITCHES

New line of lighted pushbutton control consists of four-lamp lighted panel controls designed to meet the requirements of MIL-S-22885. Unique features include single screw mounting, two-step relamping, and factory-installed internal lamp bussing. Units are offered with customized messages in a wide range of display styles and color coding. They are available with two, three, or four-pole momentary or alternate action switching. Ordering system permits the switches to be chosen by component groups, whether for a complete assembly or for a separate sub-assembly. Unimax Switch Div., Maxson Electronics Corp., Wallingford, Conn.

Circle No. 257 on Inquiry Card

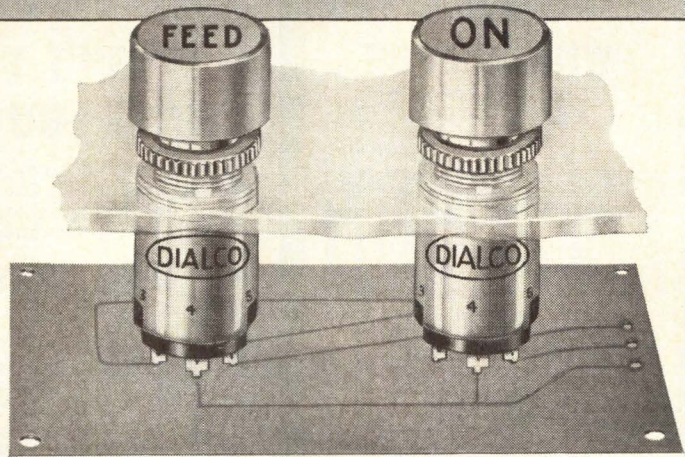
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Switches are of the silent, momentary type. Contact arrangements are: S.P.S.T. normally open or normally closed; S.P.D.T. two circuit (one N.O.; one N.C.). Ratings: 3 amps, 125V AC; 3 amps, 30V DC (resistive load). Button travel is 3/32"; operating forces are: N.O. — 20 ozs. (approx.), N.C. — 10 ozs. (approx.).

The switch is completely enclosed and independent of the light circuit. The light source is the T-1 3/4 incandescent lamp, available in a range of voltages from 1.35 to 28V. Switches are made for single hole (keyed) mounting in panels up to 3/16" thick and mount from back of panel in 1/2" clearance hole. Switches are also available for dry circuits.

Other features: 1/2" or 3/4" interchangeable caps, round or square, rotatable or keyed, in a choice of 7 cap color combinations.



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ANOTHER NEW
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CIRCLE NO. 43 ON INQUIRY CARD

METALLIC CASED CAPACITORS

Precision capacitors featuring a thin metallic outer case have been introduced with a choice of three terminal configurations. The manufacturer claims that the outer metallic case reduces moisture penetration to the extent that the units approach the characteristics of hermetically sealed models. Typical applications include high gain coupling and low RFI transmission. Called "Silvercaps," the new units are available from stock in dielectrics of polycarbonate, mylar and polystyrene in capacitance values from .01 MFD to 20 MFD. Quantity prices range from \$.75 to \$2.00 depending on capacitance and tolerance. Del Electronics Corp., Mt. Vernon, New York.

Circle No. 242 on Inquiry Card

IC MODULES FOR GATING AND LOGIC

High-speed, functional, TTL monolithic, integrated circuit modules designed for both gating and logic have recently been introduced that feature high speed (up to 10MHz), high fan out, large capacitance drive capability, and excellent noise margins. According to the manufacturer, TTL integrated circuits were chosen because "they give more power at high speeds than either RTL or DTL circuits and they provide the high capacitance drive needed in large systems." The new M Series modules are fully compatible with the manufacturer's new K Series industrial control modules, and, through the use of level converters, are compatible with all the manufacturers standard FLIP CHIP modules. To sim-

plify the use of M Series modules, input loading or output drive capability has been specified in terms of a unit load. In logic 0 state (0 to 0.4v), the driver sinks a maximum 1.6 milliamps from the driven load. In the logic 1 state (+2.4 to +3.6v), only the leakage current of the driven load must be supplied. The M Series is said to exhibit excellent noise margins. Typical DC noise margin is 1 volt at either the logic 1 or logic 0 level. Absolute worst case noise margin is 400 millivolts at either level. Prices, delivery, and complete specifications on the new M Series line are available on request. Digital Equipment Corporation, Maynard, Mass.

Circle No. 237 on Inquiry Card

PRECISION WIREWOUND RESISTORS

Subminiature precision wirewound resistors, known as Series 4R12A featuring $\pm 0.01\%$ accuracy and rugged, epoxy encapsulated construction are now available with standard temperature coefficients of $\pm 5\text{PPMC}$ and $\pm 1\text{PPMC}$. Documented performance history is said to indicate an MTBF of over 10 million hours. Other features include an operating temperature range of -55C to $+145\text{C}$, minimum resistance of 25 ohms with maximum resistance to 250K and a stability of $\pm 40\text{PPM}$ per year. Price for 1-4 pieces — \$2.80 (25ohm) to \$4.20 (250K). Under \$1.00 for production quantities. Delivery — two weeks ARO. General Resistance, Inc., Bronx, New York.

Circle No. 235 on Inquiry Card

READOUTS

We also make indicators, switches, keyboards, panel displays, in-line displays and CRT displays.

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Neon Display Tube Segmented Display Projection Display

(shown 1/4 size)

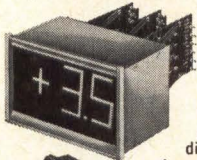
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CIRCLE NO. 44 ON INQUIRY CARD

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TBL Series—Combines neon lamp indicator with integral isolated 100 ma. SPDT switch. For I-C or discrete component circuitry. As low as \$4.35*.

TIB Series—Same as TBL but with replaceable incandescent lamp. As low as \$6.60*.

ABL-ABS Series—Alternate action two circuit, double break, 100 ma. switch for controlling separate circuits. Switch only, or with replaceable neon or incandescent lamp. As low \$5.40*.



RBL Series—Independent SPDT momentary contact switch combined with replaceable neon or incandescent lamp. As low as \$2.60*.

MBS Series—SPDT momentary 100 ma. switch. MBL Series has neon or incandescent lamp. MBS as low as \$1.45; MBL as low as \$1.88*.



SBS Series—Subminiature (.360" body) SPST n.o. momentary contact switch. SBL Series offers integral incandescent T-1 lamp with switch. SBS as low as \$1.26; SBL as low as \$3.10*.

For complete information, contact
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*in 100-499 quantities



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CIRCLE NO. 45 ON INQUIRY CARD

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Go together,
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Subminiature STL Series .360" dia. body. Controls neon or incandescent lamp from logic levels. As low as \$7.45* MSTL for I-C.

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TIB Series Integral, isolated switch plus TIL function. Price: As low as \$6.60.* MTIB Series for I-C.



TML Series Turns on with a 2µsec pulse, remains on until cleared. Integral clear switch optional. Price: As low as \$10.35.* MMTL Series for I-C.

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CIRCLE NO. 46 ON INQUIRY CARD

LOW-COST DATA SIMULATOR

A digital data simulation system capable of producing variable parameter RZ and NRZ formats is now available for a total cost of \$1075. The system provides 16-bit cycle lengths, bit rates to 10 MHz, RZ and NRZ outputs to 10V, variable baseline offset to $\pm 10V$, and continuous or command recycle. Applications include a variety of simulation tests on components, circuits, memory elements, or data transmission links. The system is also useful as a programmer for the development of time related sequential signals to command systems operations. By interconnecting additional data generators, the system can be economically expanded for applications requiring longer serial words or additional parallel channels. Such requirements include setting up programs for core testing, driving gate arrays from zero to 10V, and producing true complementary outputs which may be used to drive adders or shift registers. The pulse generator used in the system may be selected by the user for the desired output characteristics. An asynchronously-gated pulse generator is required for RZ formats. The 201/101 Data Simulation System provides continuously variable widths from 35 ns to 10 ms, continuously variable delays from 40 ns to 10 ms, outputs from 0.5V to 10V into 50 ohms, and rise time of less than 5 ns. Dimensions: 3½" H x 19" W x 11" D. Weight: 16 lbs. Datapulse Incorporated, Culver City, Cal.

Circle No. 241 on Inquiry Card

NEW OPTIONS FOR IC MEMORY

Six new options for the model CE-100 core memory are now available which further enhance the operation of this 1 microsecond system: data save, address indicator lights, sequential operation, self testing for the memory, overvoltage protection and DC voltage metering for the power supply. The memory is available in sizes up to 4096 words by 36 bits and any or all options may be incorporated into any size. Delivery is usually less than 60 days. Memory Products, Lockheed Electronics Company, Los Angeles, Cal.

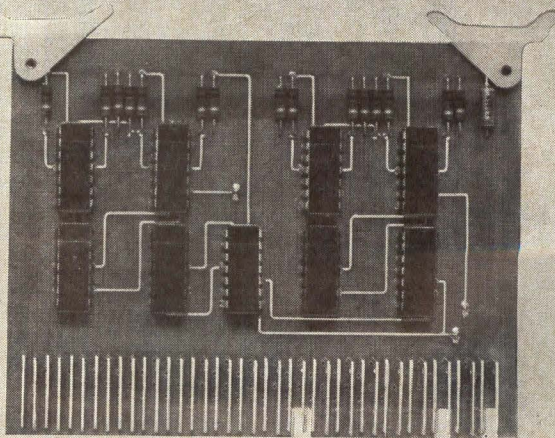
Circle No. 244 on Inquiry Card

PULSE GENERATOR FOR IC TESTING

A pulse generator module of radically new design, for use with its Model 800 IC Test system, has been announced by The Birtcher Corporation. Control functions of the Model 842 Pulse Generator module are specially designed for ease of operation in measuring pulse parameters in digital logic IC testing. Output of each of the dual channels is independently adjustable; pulse width and delay are adjustable as a percent of period (15-80%) regardless of frequency; and output switching levels are independently adjustable between +10v and -10v. Four fixed frequencies of rep rate, between 1 and 1000 KHz. A system of BNC connectors and selector switches permits pulses with either 10 nsec or 100 nsec rise times to be applied to the IC under test. Birtcher Corp., Instrument Div., Monterey Park, Cal.

Circle No. 239 on Inquiry Card

reduce system size 7:1 with MicroVersaLOGIC IC Modules



The complete MicroVersaLOGIC line gives you all the ready-made building blocks you need for anything from a register to an entire digital system—with a 7:1 size reduction because of MicroVersaLOGIC's high density IC packaging.

MicroVersaLOGIC also means increased reliability over discrete components, lower power requirements, greatly reduced costs. MicroVersaLOGIC features NAND, NOR logic with wired OR capacity at the collector, operates to 5v. logic levels, has excellent noise rejection of over 1v. There are over 20 basic module types, all meticulously designed and assembled to give you utmost reliability.

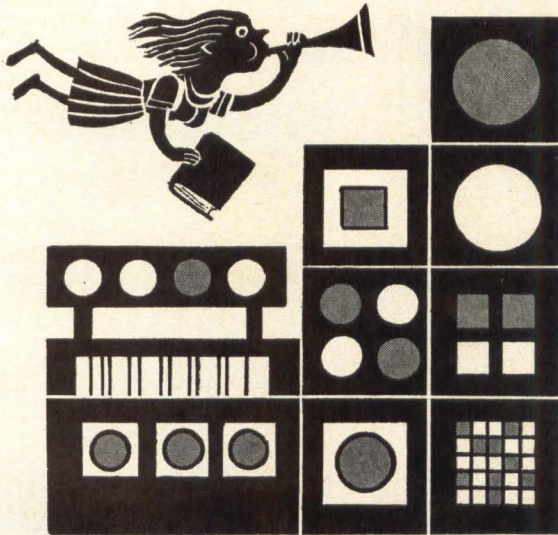
Our new MicroVersaLOGIC brochure will show you how easy and economical it is to design digital systems with MicroVersaLOGIC IC Modules. Write or call.



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CIRCLE NO. 47 ON INQUIRY CARD



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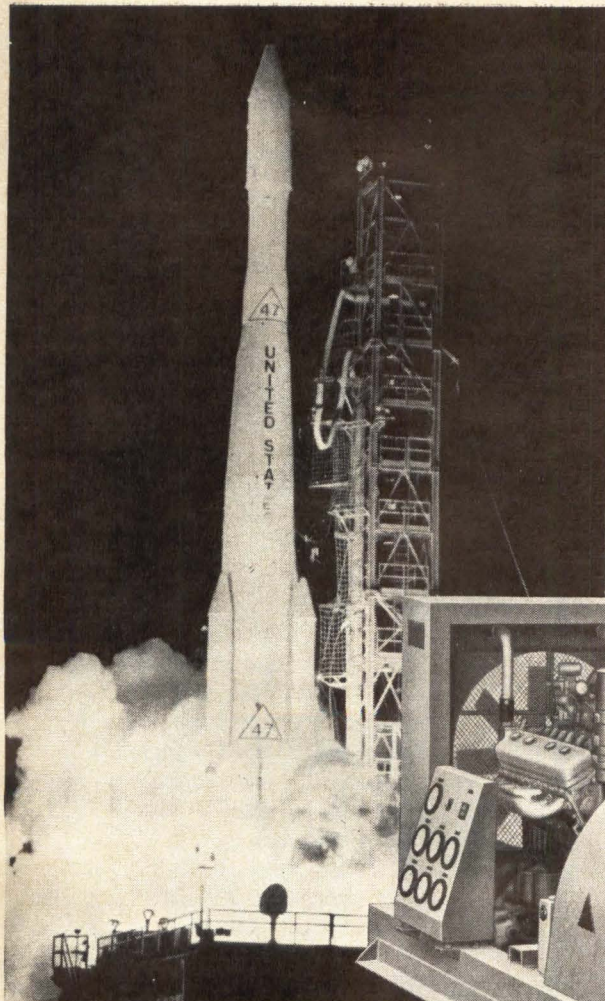
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Continuous clean power for communications at Cape Kennedy supplied by Kato as part of UPS system



Typical UPS unit installed at Cape Kennedy incorporates 250 H.P. Consolidated Diesel Engine that will start instantly, in event of prime power failure. Flywheel, mounted on shaft extension between motor and engine, would maintain constant generator speed during engine start-up to prevent even slightest power interruption. KATO Motor is 250 H.P., 208 volt, 3-phase, synchronous type with brushless excitation. KATO Generator continually feeds 150 kw of pure 120/208 volt, 60-cycle, power to communications system.

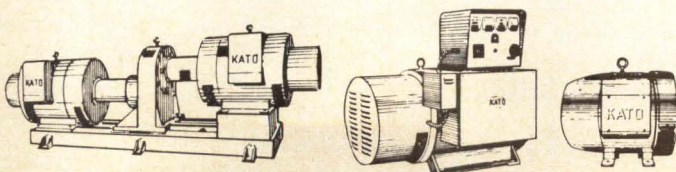
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LITERATURE

Oil Tight Pushbuttons

A sixteen-page, full color brochure describes all of the components of a new line of heavy duty oil tight pushbuttons. In addition, the manual describes in detail both heavy duty and electronic duty contact blocks, selectors, selector-push devices, indicators, enclosures, potentiometers, abbreviated legending information and optional accessories. Legend plates are available in two types: standard aluminum etched with black enamel fill, and epoxy coated nylon in a variety of colors including aluminum to blend with the standard plates. A choice of two sizes of plates is offered: 2¼" square size which fits commercially available enclosure cutouts, and 1⅞" square size said to provide 20% reduction in panel space in either rows or columns for minimum center mounting. Micro Switch, a Division of Honeywell, Freeport, Ill.

Circle No. 323 on Inquiry Card

Printed Circuits

Capabilities of Scientific Data Systems to manufacture custom-designed printed circuit boards for industrial and military applications are described in a new 12-page brochure. The SDS Printed Circuits organization has produced boards of varying complexity and size to meet the standards of various government agencies. Facilities are available to provide all the required printed circuits services including screen and photo printing, precious metal plating, hot-oil fusing, through-hole plating, and back-etching. Scientific Data Systems, Santa Monica, Calif.

Circle No. 325 on Inquiry Card

Edge Lit Indicators

Six-page catalog, No. 67-100, gives details on 26 models of edge lit indicators from tiny instrument readouts to large mimic diagram indicators. K.G.M. indicators are of particular interest to design engineers because of their flexibility which permits many custom features to be provided at reasonable cost. Inter-Market, Inc., Glenview, Illinois.

Circle No. 302 on Inquiry Card

Stepping Motors

Data sheets describe two new models of Stepping Motors — Responsyn Stepping Motors HDUM-30-100 and HDUM 9-60-5. In these motors, a primary power source and the unique Harmonic Drive flexible rotor are combined to provide a compact, high-torque stepping motor. A high speed rotating radial magnetic field is converted directly into a mechanical, rotary output having greatly reduced speed and high torque. Model HDUM 9-60-5 performance features are: high resolution (480 steps per revolution), high torque (12 in.-oz. to 2400 PPS) capability of driving large, directly coupled inertia loads to 1000 steps per second. The manufacturer claims that these features make the HDUM-9 highly suited for incremental recorder drives and X-Y axis pen drives. Model HDUM-30-100 performance features are: high resolution (800 steps per revolution) high torque (90 inch lbs.) large inertia loads (100 lb. in² to 200 Steps Per Sec.). Harmonic Drive Div., United Shoe Machinery Corporation, Beverly, Mass.

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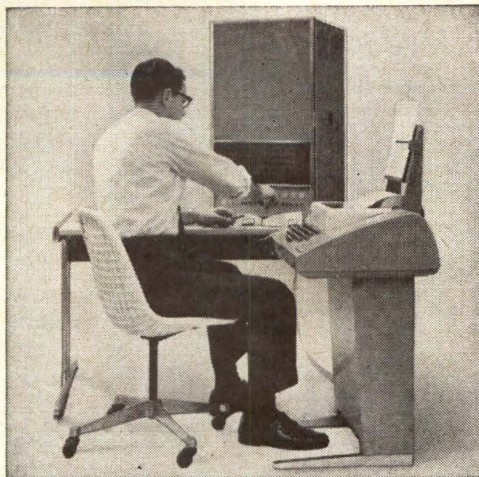
Flat Cable Assemblies

Data file outlines application information and specifications on Cicoil "Super-Flex" flat cable assemblies. The file also contains test samples of the silicone tape in which various types of conductors are encapsulated. Based on a unique process, which allows the combination of shielded cable and twisted pairs with bare copper or insulated wire in a single, flat cable, the assemblies are furnished only with connectors and are designed for maximum flexibility under a wide range of environmental characteristics. Test Data included outlines the results of life tests in which the silicone-encapsulated cable was subjected to over 70 million flexures at the rate of 300 flexures per minute, under varying temperatures from -300°F to +500°F. Cicoil Corporation, Van Nuys, Calif.

Circle No. 304 on Inquiry Card

Drum Memory Systems

Eight-page technical brochure, SB-



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6708, describes standard VRC drum memory systems that provide large capacity, self-interfacing external data and program storage for PDP-8 and 8/S computers. Included are details of software supplied for transfer and diagnostic routines, and a discussion of 1104S system suitability for time-sharing. The brochure deals with three basic standard system types: program controlled transfer; data channel transfer; and direct memory access transfer. There are also brief descriptions of special VRC systems, as well as standard memory drums. Vermont Research Corporation, North Springfield, Vermont.

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Digital Data Systems

Eight-page brochure describes a wide range of custom and standard digital data systems and components. It offers systems application information on interface buffering and data processing as well as specification summaries on digital to synchro converters, digital range simulators and other standard components. Canoga Electronics Corporation, Canoga Div., Chatsworth, Calif.

Circle No. 306 on Inquiry Card

New Lighting Concept

Four-page catalog introduces a unique concept for indicator lights, edge-lighted panels and instrument lighting. Products featured are designed for use with a "Pogo" lamp, which contains a spring loaded center contact that eliminates the requirement for moving contacts in the permanently mounted light socket assemblies. Units are offered in a wide range of indicator light colors and lens cap styles. Lamps are available in both long-life and high brilliancy types, in rated voltages from 1.5 through 28 and neon. Western Indicator Co., Inc., So. El Monte, Calif.

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Plastic Encapsulated Transistor Reliability

Twelve-page brochure reports that Motorola small signal plastic encapsulated transistors meet or exceed military environmental and mechanical requirements, and exhibit a life test performance equivalent to similar devices in hermetically sealed packages. The report summarizes re-

sults after two years and 10 million device hours of testing in a continuing reliability program investigating operating and storage life, parameter stability, resistance to moisture, and the effects of mechanical and thermal stress. Test methods and techniques used in the analysis, as well as quality control testing information, are included. The test results are presented in the form of graphs and histograms. Motorola Semiconductor Products, Inc., Phoenix, Arizona.

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Operational Amplifier

Specifications and 42 schematics in two loose-leaf sheets explain applications of the Model 4009 opamp. The external circuitry is specified, with component values, for use of the amplifier as an oscillator, voltage regulator, modular, demodulator, active filter, power amplifier, instrumentation amplifier, temperature controller, pulse-width modulator, and other applications. OpAmp Labs, Los Angeles, Cal.

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IC Logic Circuits

A 32-page handbook gives complete descriptions of a family of integrated circuits for GSE and industrial/commercial use. In addition to the text which presents circuit descriptions and characteristics, more than 100 illustrations present design information and detailed application examples in the form of schematic and block diagrams. The IC logic series offers 800 mv minimum noise margins, fan-outs of up to 17 from gates and J-K binary and high capacitive drive capability. Signetics Corp., Sunnyvale, Cal.

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Electromagnetic Shielding Design Manual

Comprehensive 40-page design manual, "Shielding for Electromagnetic Compatibility," provides basic information on proper design of electromagnetic shielding including permeability and attenuation curves for commonly used ferro-magnetic alloys. Manual gives helpful design data on selection of materials, heat treatment, effect of shield configuration and thickness on magnetic shielding performance, and formulas for calculation of field attenuation in deci-



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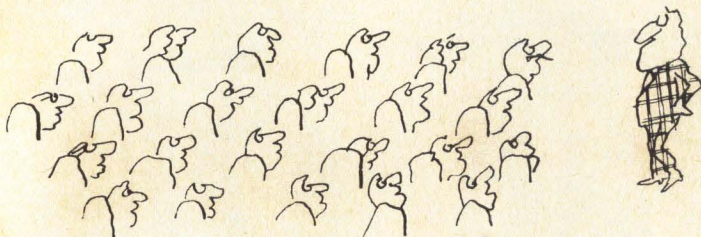
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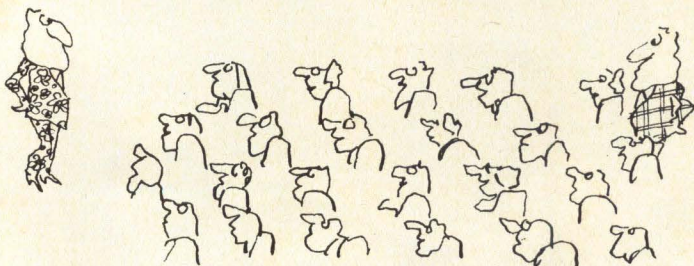
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bels. All important factors, both mechanical and electrical, that must be evaluated in designing effective electromagnetic shields are discussed. New manual is available at \$1.50 per copy. Order directly from Magnetic Metals Company, 2108 Hayes Avenue, Camden, N.J. 08101.

Circle No. 309 on Inquiry Card

Tape-Reel Drive Motors

Two-page technical data sheet describes direct-current, fractional horsepower motors for use as computer tape transport drives. Included are dimensions, performance curves and technical data on 10 models. General Electric, Schenectady, N.Y.

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Integrated Relay/Lamp Driver

Data sheet contains schematic and connection diagrams, typical applications, ratings and electrical characteristics on a new integrated relay lamp driver. Also included are performance curves and definitions of terms. Identified as NS7673, it is designed to accept standard DTL or

TTL logic levels and drive a load of up to 300 mA at 28 volts. National Semiconductor Corporation, Santa Clara, Calif.

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Dipped Silvered-Mica Capacitors

Four-page bulletin describes a new family of single-film capacitors, Type 434M, 440M, and 446M. Application of ceramic capacitor manufacturing techniques to mica capacitors has resulted in low-cost capacitors which offer excellent stability and retrace characteristics yet are significantly more economical. Type 434M covers the capacitance range of 10pF through 51pF; Type 440M, from 52pF through 200pF; and Type 446M, from 201pF through 360pF. All three types are rated for operation at 500 WVDC and are designed for operation over the temperature range of -55 C to +85 C. Standard capacitance tolerance is $\pm 5\%$ or $\pm 0.5pF$ (whichever is greater), although other tolerances are available on special order. Sprague Electric Co., North Adams, Mass.

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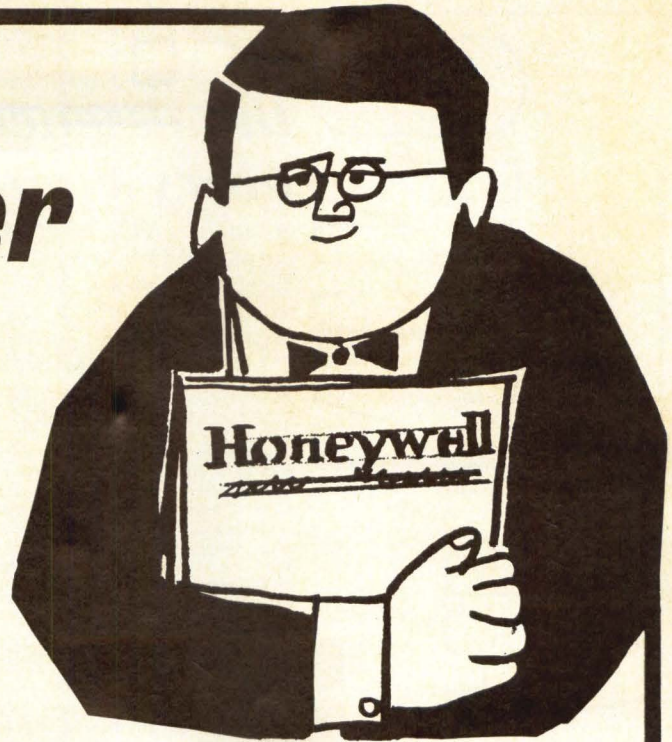
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To do advanced research in improving the technology concerning electro-magnetic heads. This will involve design and development and new concepts in head development. 3-5 years of related experience would be necessary.

ELECTRONICS ENGINEERS

To perform design of circuits and logic for manufacturable equipment, to design and evaluate sensor systems, position transducers, and actuators. Related experience in all or any of these areas would be helpful. Qualified BSEEs will find a selection of opportunities to further their experience and careers.

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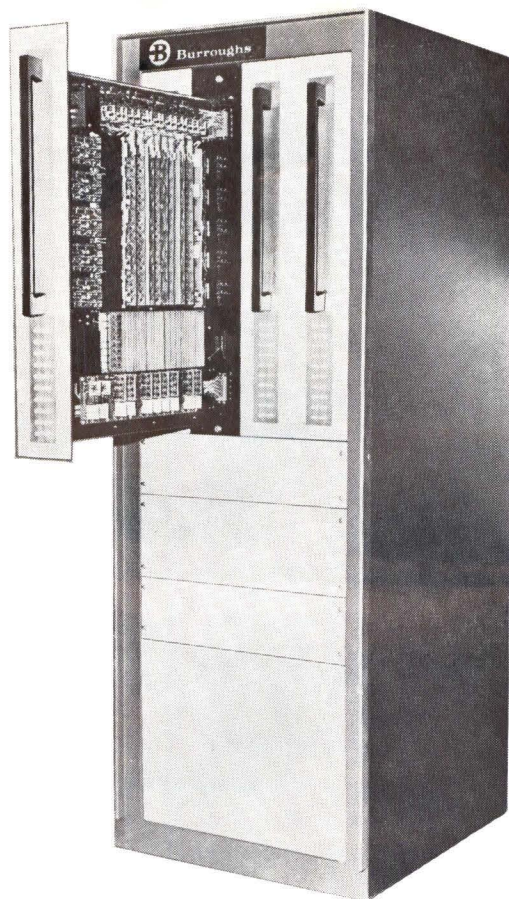
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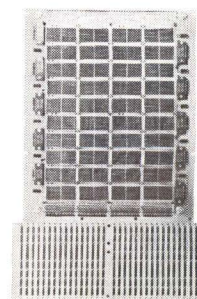
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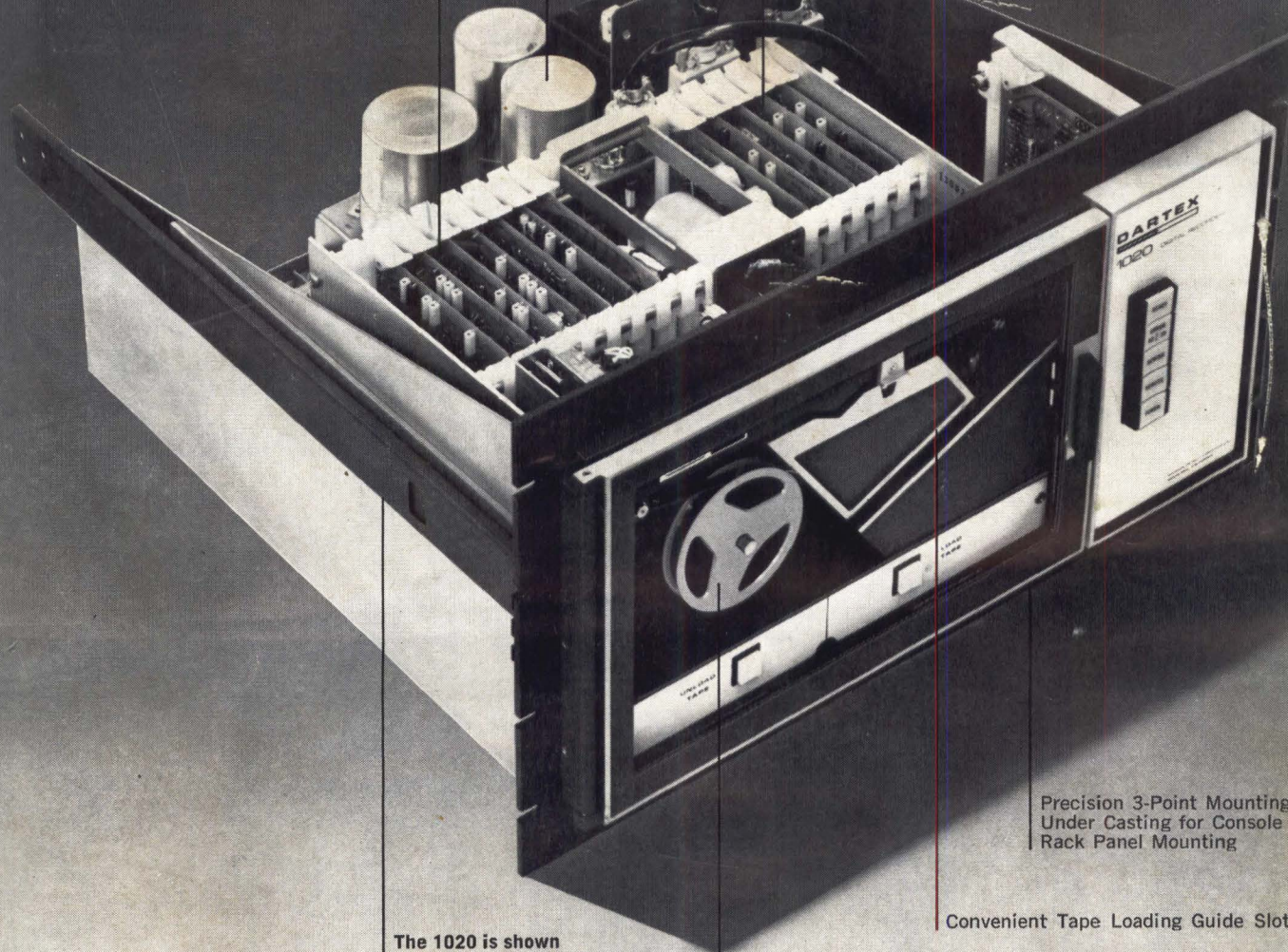
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