COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

APRIL 1978

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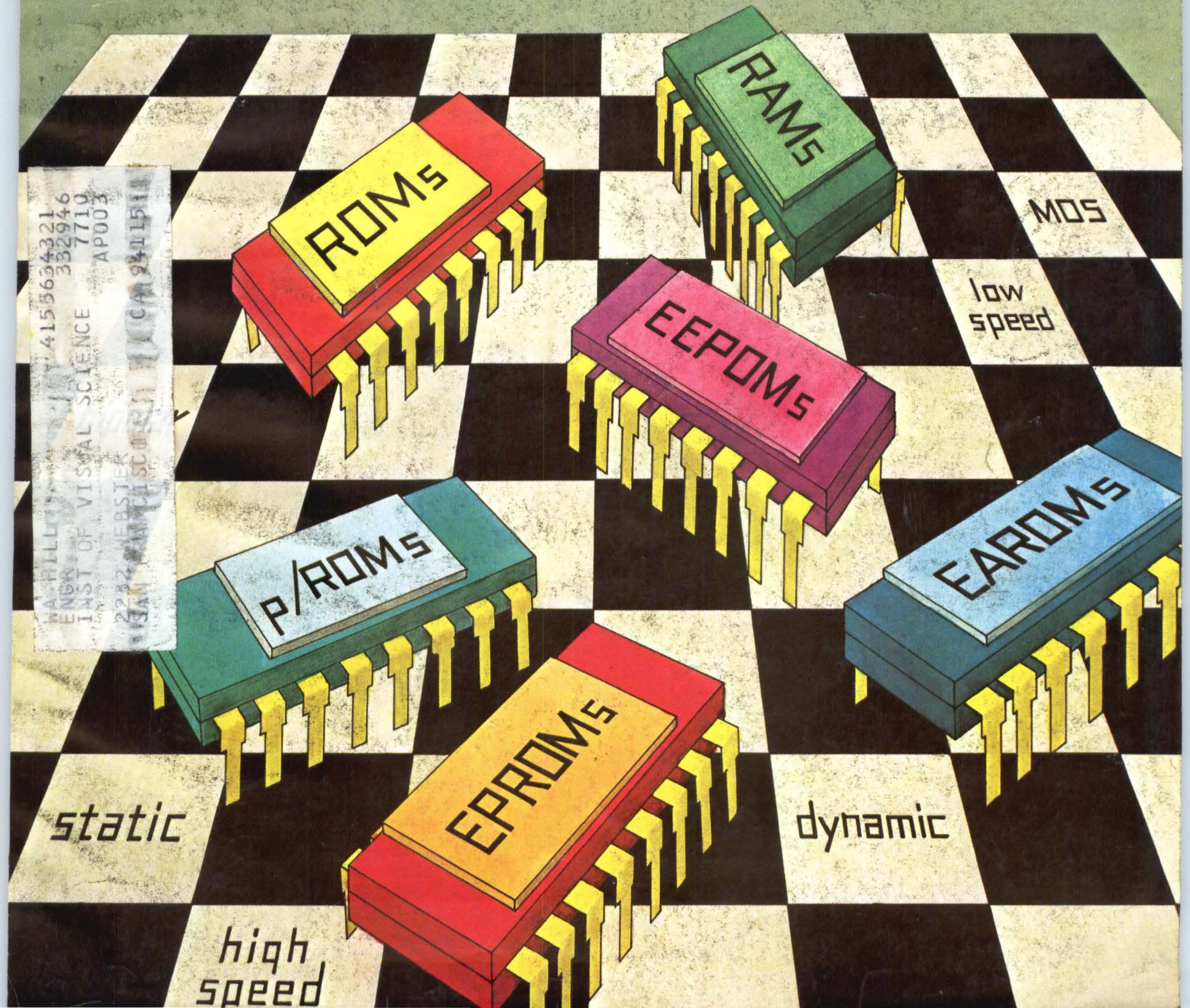

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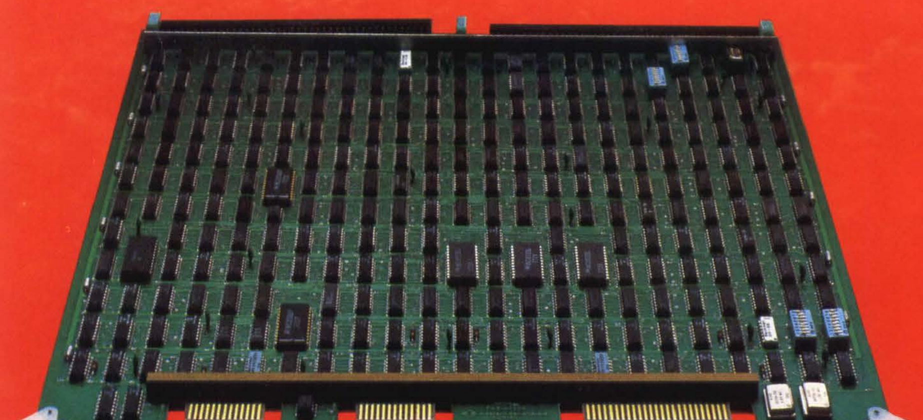

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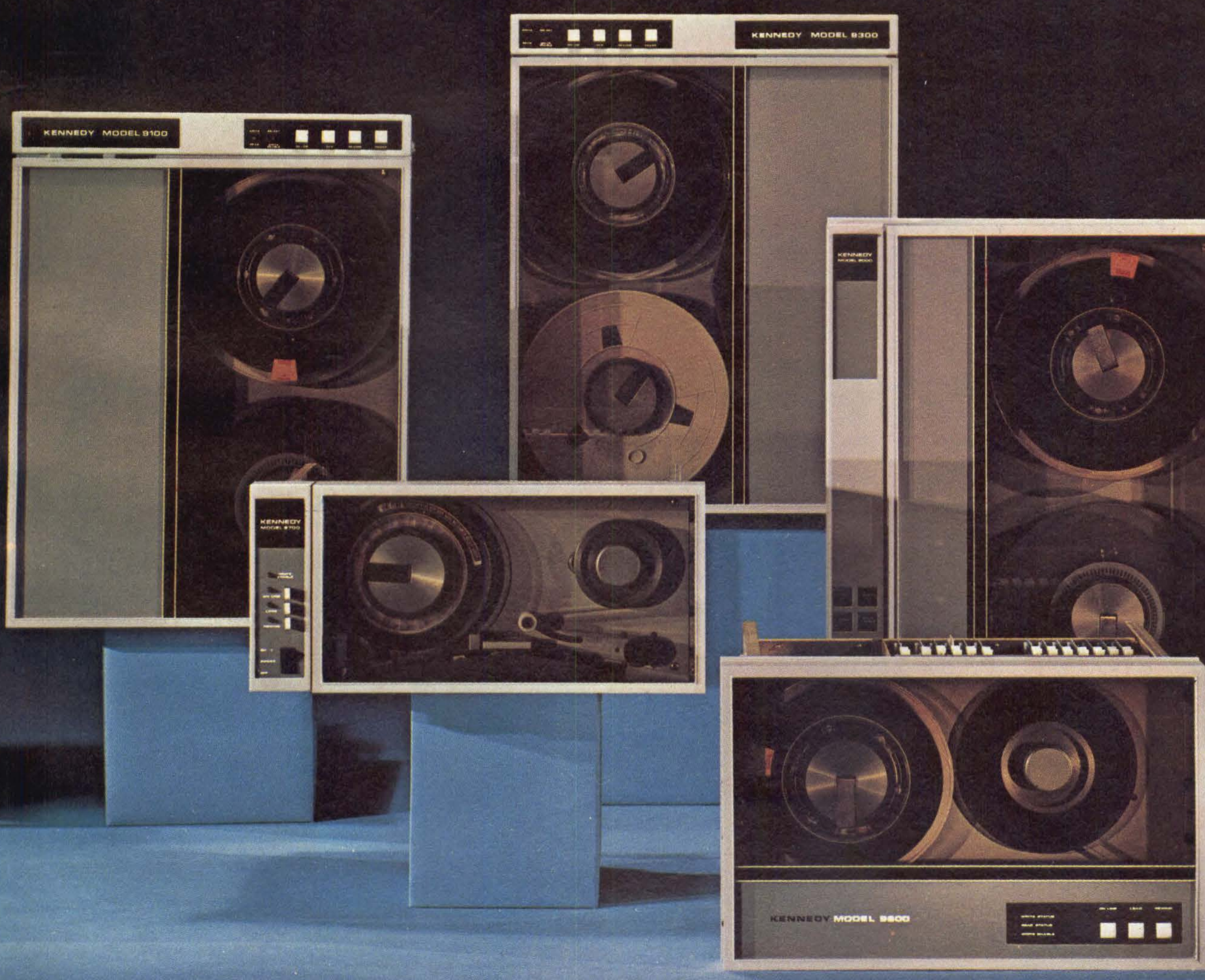

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

APRIL 1978

VOLUME 17, NUMBER 4

DEPARTMENTS

BPA **CIRCULATION OVER 58,000 (JUNE 1977)**

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FEATURES

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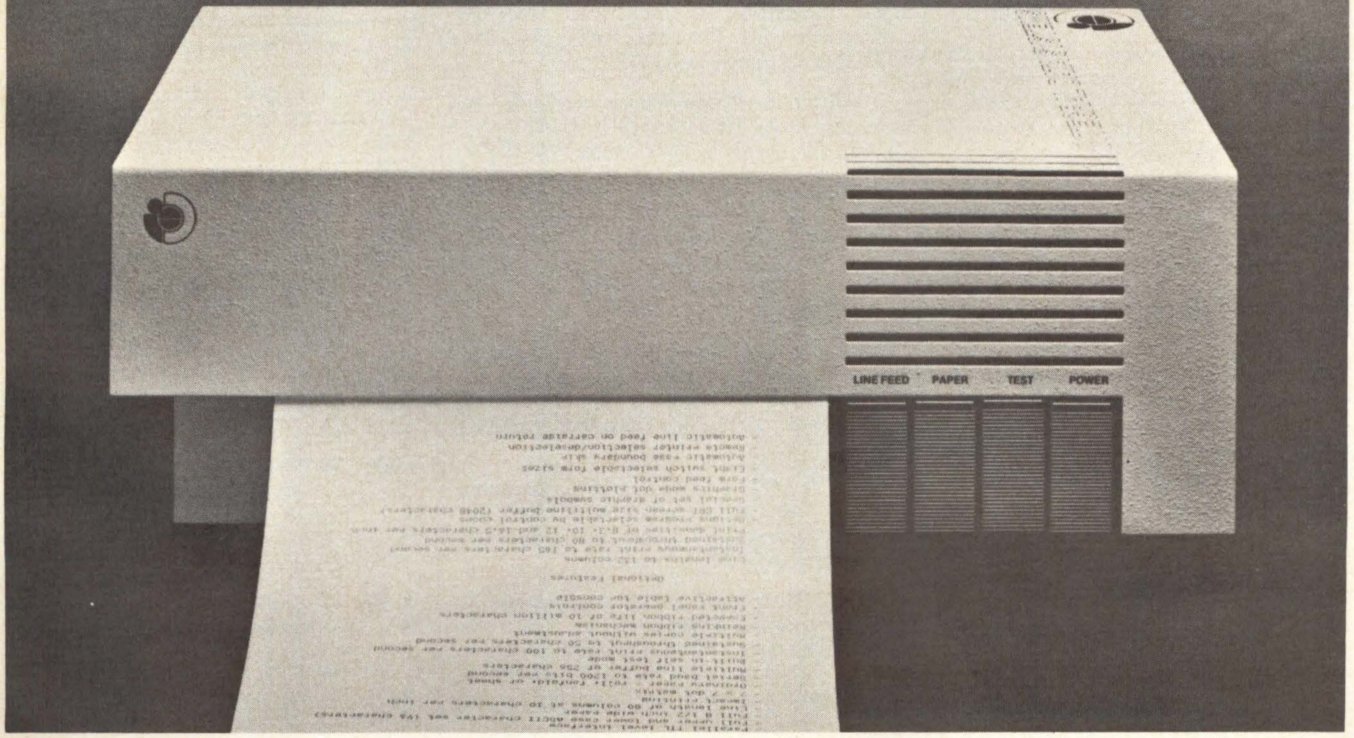

CALENDAR

CONFERENCES

APR 18-20—Mini/Micro Computer Conf and Expo, Philadelphia, Pa. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807. Tel: (714) 528-2400

APR 28-30—PERCOMP '78, Long Beach Conv Ctr, Long Beach, Calif. INFORMATION: Royal Exposition Mgmt Corp, 1833 E 17th St, Suite 108, Santa Ana, CA 92701. Tel: (714) 973-0880

MAY 10-12—3rd Internat'l Conf on Software Engineering, Hyatt Regency Hotel, Atlanta, Ga. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 15-17—Data Entry Conf, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Dept PR, AIIE Seminars, PO Box 3737, Santa Monica, CA 90403. Tel: (213) 450-0500

MAY 17-19—IEEE Internat'l Sym on Circuits and Systems, Roosevelt Hotel, New York, NY. INFORMATION: Dr Kenneth R. Laker, Bell Laboratories, Holmdel, NJ 07733. Tel: (201) 949-5075

MAY 18—Trends and Applications: Distributed Processing, Gaithersburg, Md. INFORMATION: Distributed Processing, PO Box 639, Silver Springs, MD 20901

MAY 19-21—Personal and Small Business Computer Expo—"South," Exposition Pk, Orlando, Fla. INFORMATION: Felsburg Associates, Inc, 12203 Raritan Ln, PO Box 735, Bowie, MD 20715. Tel: (301) 262-0305

MAY 22-23—Lightwave Communication Trade Show, Park Plaza Hotel, Boston, Mass. INFORMATION: Fiber Optic Con, c/o Conventures, Inc, 11 Newbury St, Boston, MA 02116. Tel: (617) 267-0055

MAY 22-25—2nd Minnesota Electronics Manufacturing and Assembly Conf and Expo (Minnex II), St Paul Civic Ctr, St Paul, Minn. INFORMATION: Kevin Miller, Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500, X417

MAY 22-26—7th Annual Sym on Incremental Motion Control Systems and Devices, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Prof B. C. Kuo, Dept of Electrical Engineering, U of Illinois at Urbana-Champaign, Urbana, IL 61801. Tel: (217) 333-4341

MAY 23-25—ELECTRO '78, Boston-Sheraton, Hynes Auditorium, Boston, Mass. INFORMATION: W. C. Weber, Jr, IEEE ELECTRO, 31 Channing St, Newton, MA 02158. Tel: (617) 527-5151

MAY 24-26—8th Internat'l Sym on Multiple Valued Logic, Sheraton O'Hare Motor Hotel, Chicago, Ill. INFORMATION: A. S. Wojcik, Dept of Computer Science, Illinois Institute of Technology, Chicago, IL 60616. Tel: (312) 567-5153

JUNE 4-7—Internat'l Conf on Communications, Sheraton Hotel, Toronto, Ontario, Canada. INFORMATION: F. J. Heath, Power System Operation Dept, Ontario Hydro Electric Power System, 700 University Ave, Toronto M5G 1X6, Canada

JUNE 5-7—Conf on Pattern Recognition and Image Processing, Chicago, Ill. INFORMATION: K. Preston, Jr, Dept of EE, Carnegie-Mellon U, 5000 Forbes Ave, Pittsburgh, PA 15213

JUNE 5-8—1978 Nat'l Computer Conf (NCC), Anaheim Conv Ctr, The Disneyland Hotel Comp, Anaheim, Calif. INFORMATION: AFIPS, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

JUNE 12-13—Microcomputer-Based Instrumentation Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Dr Helmut Hellwig, Nat'l Bureau of Standards, Rm A-1002 Administration, Washington, DC 20234. Tel: (301) 921-3181

JUNE 15—17th Annual Technical Sym of ACM and NBS, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: U.S. Dept of Commerce, Nat'l Bureau of Standards, Washington, DC 20234

JUNE 21-23—Internat'l Sym on Fault Tolerant Computing, Toulouse, France. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

JUNE 26-28—Design Automation Conf, Las Vegas, Nev. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901

JUNE 26-28—36th Annual Device Research Conf, U of California, Santa Barbara, Calif. INFORMATION: Dr James C. McGroddy, 1978 DRC Chm, IBM T. J. Watson Research Ctr, Yorktown Heights, NY 10598. Tel: (914) 945-1228

AUG 6-9—3rd Jerusalem Conf on Information Technology (JCIT), Jerusalem, Israel. INFORMATION: Anthony Ralston, SUNY at Buffalo, 4226 Ridge Lea Rd, Amherst, NY 14226

AUG 28-SEPT 1—8th Australian Computer Conf, Canberra, Australia. INFORMATION: ACS-8 Programme Committee, PO Box 448, Canberra, ACT 2601, Australia

SEPT 19-22—Conf on Microprocessors in Automation and Communications, U of Kent at Canterbury, England. INFORMATION: Conf Secretariat, Institution of Electronic and Radio Engineers, 99 Gower St, London WC1E 6AZ, England

SEMINARS

MAY 22-24 and JUNE 12-14—Plastic Part Design, Holiday Inn, San Francisco Airport, San Francisco, Calif; and Holiday Inn/O'Hare-Kennedy, Chicago, Ill. INFORMATION: Plastic Design Form Seminars, 1701 N Damen Ave, Chicago, IL 60647. Tel: (312) 278-9311

JUNE 13-15—Automated Testing For Electronics Manufacturing (ATE) Seminar/Exhibit, Boston Park Plaza Hotel, Boston, Mass. INFORMATION: Sheila Goggin, ATE Seminar/Exhibit Coordinator, Circuits Manufacturing Magazine, 1050 Commonwealth Ave, Boston, MA 02215. Tel: (617) 232-5470

SHORT COURSES

MAY 1-3—Applications of Microcomputers in Control Systems; and Finance for Engineers; MAY 15-19—Structured Programming and Software Engineering; MAY 24-26—Microprocessors and Microcomputers Workshop, George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

MAY 1-5—Microprocessor Fundamentals, MAY 8-12—8060 SC/MP Applications, MAY 15-19—8900 Pace Applications, MAY 22-24—Complex Peripherals; and MAY 1-5—Microprocessor Fundamentals, and MAY 8-10—Complex Peripherals, Bedford, Mass; and Santa Clara, Calif. INFORMATION: Al Jefferis, Manager Training Ctr, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Tel: (408) 737-6453

MAY 17-19; JUNE 21-23; JULY 12-14—The Man-Computer Interface; and MAY 22-24; JUNE 26-28; JULY 17-19—Software/Hardware Tradeoffs in System Development, Cumberland Hotel, London, England; Quality Inn-Pentagon City, Arlington, Va; and Amsterdam Hilton, Amsterdam, Holland. INFORMATION: Marie Saunders, Technology Service Corp, 2811 Wilshire Blvd, Santa Monica, CA 90403. Tel: (213) 829-7411

MAY 18-19—Program Testing Tutorials, San Francisco, Calif. INFORMATION: Dr E. F. Miller, Jr, Software Research Associates, PO Box 2432, San Francisco, CA 94126. Tel: (415) 921-1155

JUNE 12-16—Machine Vision, Automatic Assembly, and Productivity Technology, Mass Institute of Technology, Cambridge, Mass. INFORMATION: Director of Summer Session, Rm E19—356, Mass Institute of Technology, Cambridge, MA 02139

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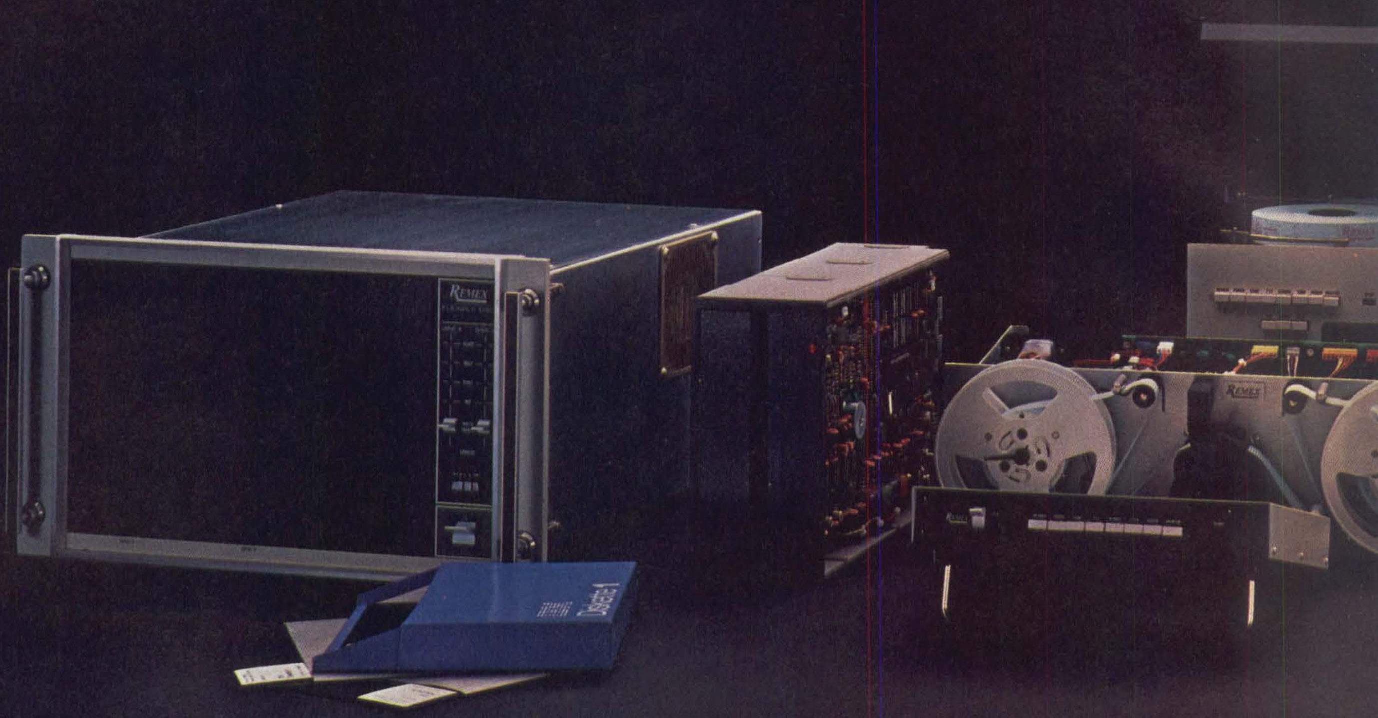

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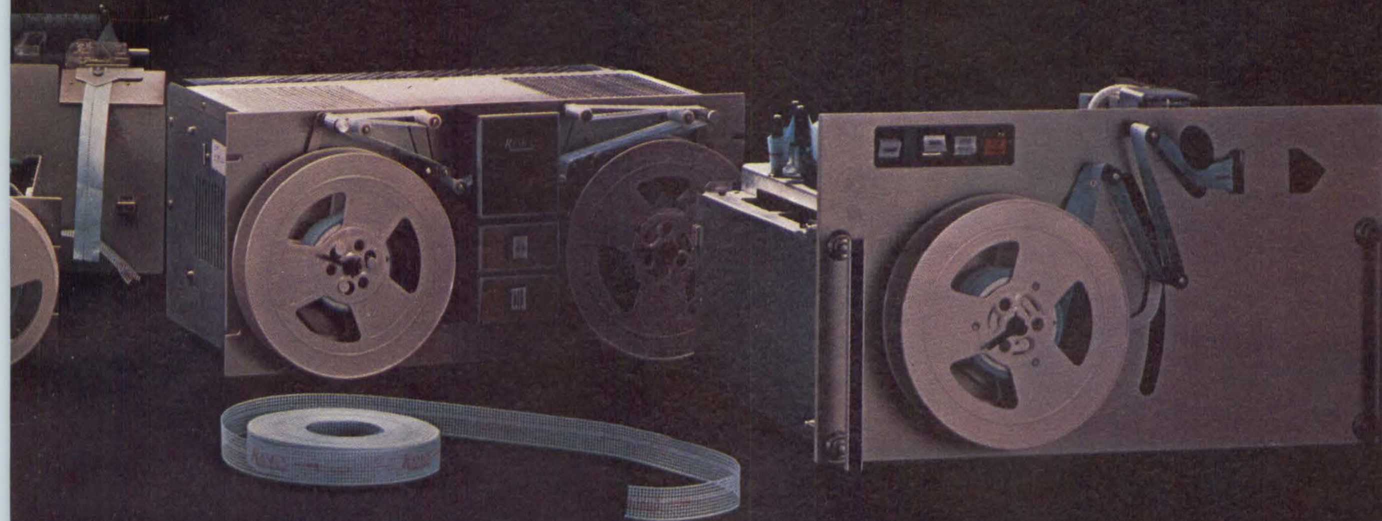

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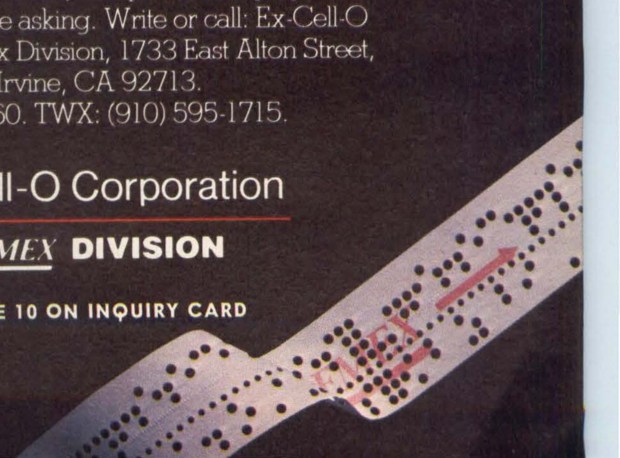

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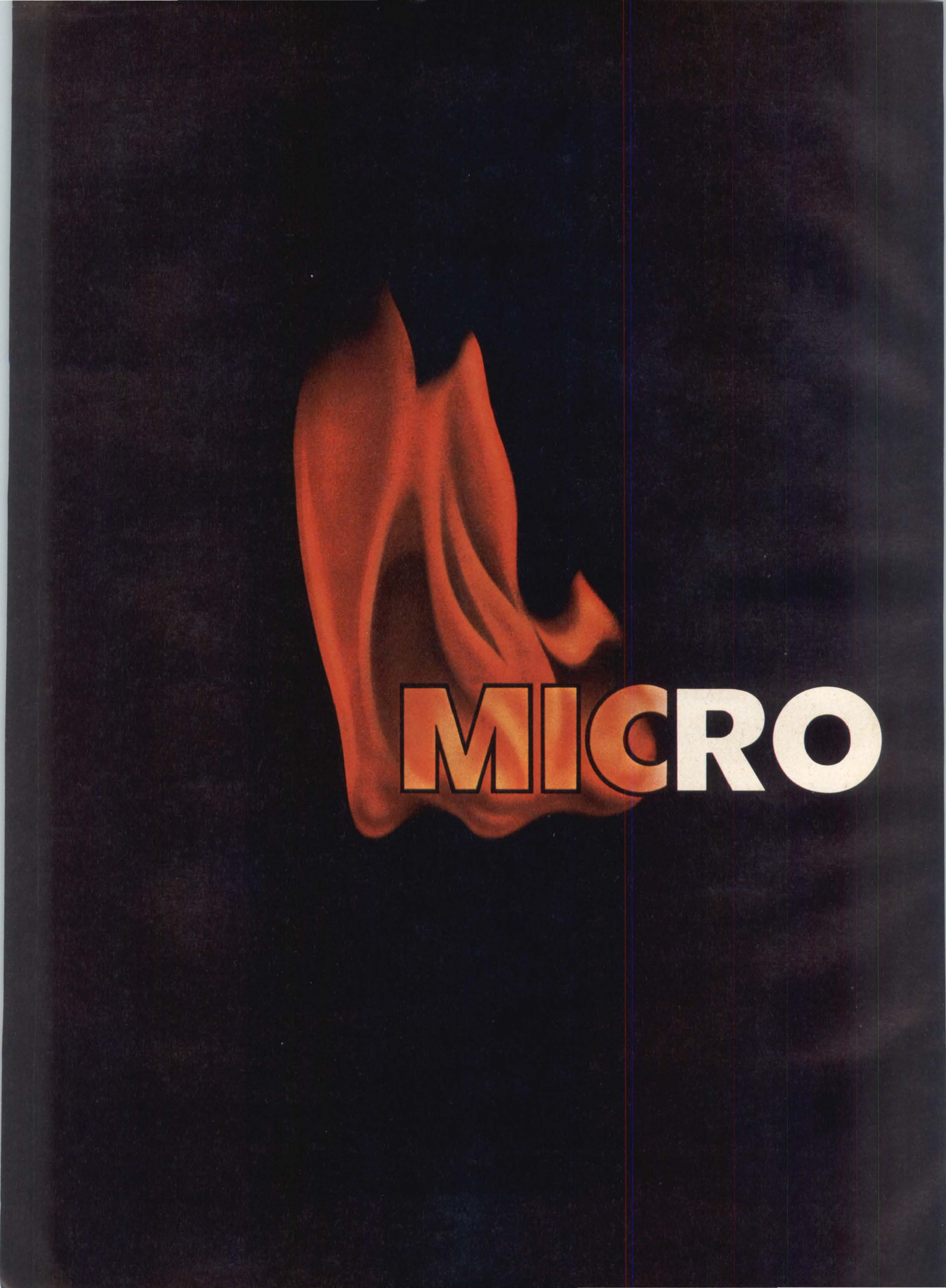
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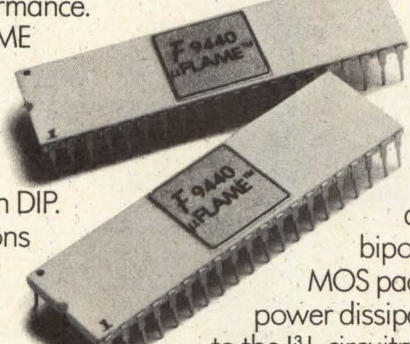

Major applications for the new device include OEM data processing in a variety of computing control and instrumentation environments; telecommunications PBX and PABX switching installations; and distributed intelligence, distributed multi-processing and front-end (terminal) processing.

Where there's flame there's fire.

Fairchild is also introducing its FIRE™ (Fairchild Integrated Real Time Executive) software. FIRE I is an initial software package for the 9440 that includes the required development aids: diagnostics, a bootstrap and binary loader, and an interactive entry and debugging program.

In addition, the μFLAME microprocessor can execute the Data General NOVA 1200 instruction set. FIRE software such as text editor, symbolic debugger and business BASIC are also available now.

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Only the beginning.

More sophisticated FIRE software, board level hardware and LSI support circuits will become available throughout the year. The software will include a floppy disc operating system, disc operating system and a FORTRAN compiler. New LSI circuits will include a 16K TTL dynamic RAM; a memory control with control, refresh and DMA capabilities; an I/O control, and a hardware multiply and divide capability.

We put the whole 9440 story in a brochure for you. Just write us and we'll send you a copy. For kits and data sheets, contact your Fairchild representative or sales office. Or order direct from Fairchild Camera and Instrument Corporation, MICROFLAME Mail Stop 22-240, 464 Ellis Street, Mountain View, California 94042. Tel: (415) 962-4626. TWX: 910-379-6435.

NOVA is a trademark of Data General Corporation.

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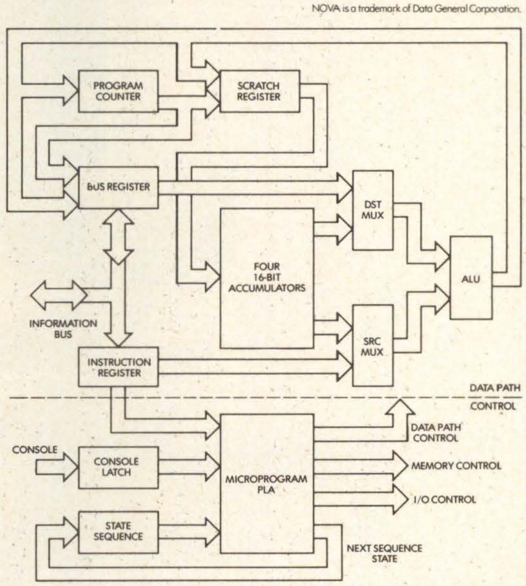

9440 Block Diagram

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LETTERS TO THE EDITOR

To the Editor:

We are one of the original manufacturers of local modems and are familiar with the difficulty of explaining their functional advantages and limitations. Although Mr Buckley (see "Local Modems," *Computer Design,* Jan 1978, pp 14-17) has done well in terms comprehensible to both management and engineering, I would like to add the following comments.

Local modems do not emit "40 to 50 mW . . . to achieve reliable data transmission." Even at the lower data rates, where hf line response is not a problem, the maximum output power allowed by Bell System PUB 43401 is less than 1 mW. At higher frequencies, permitted power falls off rapidly and virtually no energy can be emitted above 15 kHz. The higher powered line drivers can be used only on privately owned cable.

An inherent characteristic of the unloaded line gives rise to the range limitation. A typical 26 gauge metallic circuit exhibits a loss of about 0.5 dB/kft at 1 kHz and about 1.6 db/kft at 10 kHz. Hence, range is limited by the receiver's ability to recover the weaker high frequency signal components from the noise. If the use of these higher frequencies is avoided altogether, the operating range can be increased. Our patented encoding method achieves such a bandwidth reduction and permits up to 100% greater ranges than those shown in the table.

Also, a new trend is emerging in the telephone industry. The proliferation of carrier systems in dense urban areas is making unloaded metallic circuits more difficult to get. This has led to the introduction of the "medium-range" modem. Somewhat more sophisticated than short-haul units, these devices operate over 3002 type facilities. At the same time, cost-effective design has held their cost well below that of the traditional long-haul modem.

G. Brian Hick
Gandalf Data Communications Ltd
Ottawa, Ontario, Canada

To the Editor:

I read with interest Mr John Buckley's article "Certification in 1977" (*Computer Design,* Dec 1977, pp 11-14). He did a fine job of summarizing the confusing and conflicting events that have transpired while the FCC struggles toward an effective certification program. Although the details were not final at the time of this writing, I was considerably heartened by Mr John D. Butts' earnest pledge to "make certification work."

In his article, Buckley wrote that "a second technical factor is that most customer-owned systems and equipment were designed to interface to a connecting arrangement, not directly to telephone lines." If this broad description of "customer-owned systems and equipment" is referring to PBX and key telephone systems, he may be in error. The only PBX telephone system designed for and dependent upon an interface device is the TeleResource TR-32. All other PBX systems can be directly connected.

Charles R. Boggs
International Communications
Management, Inc
San Francisco, Calif

Letters to the Editor should be addressed:

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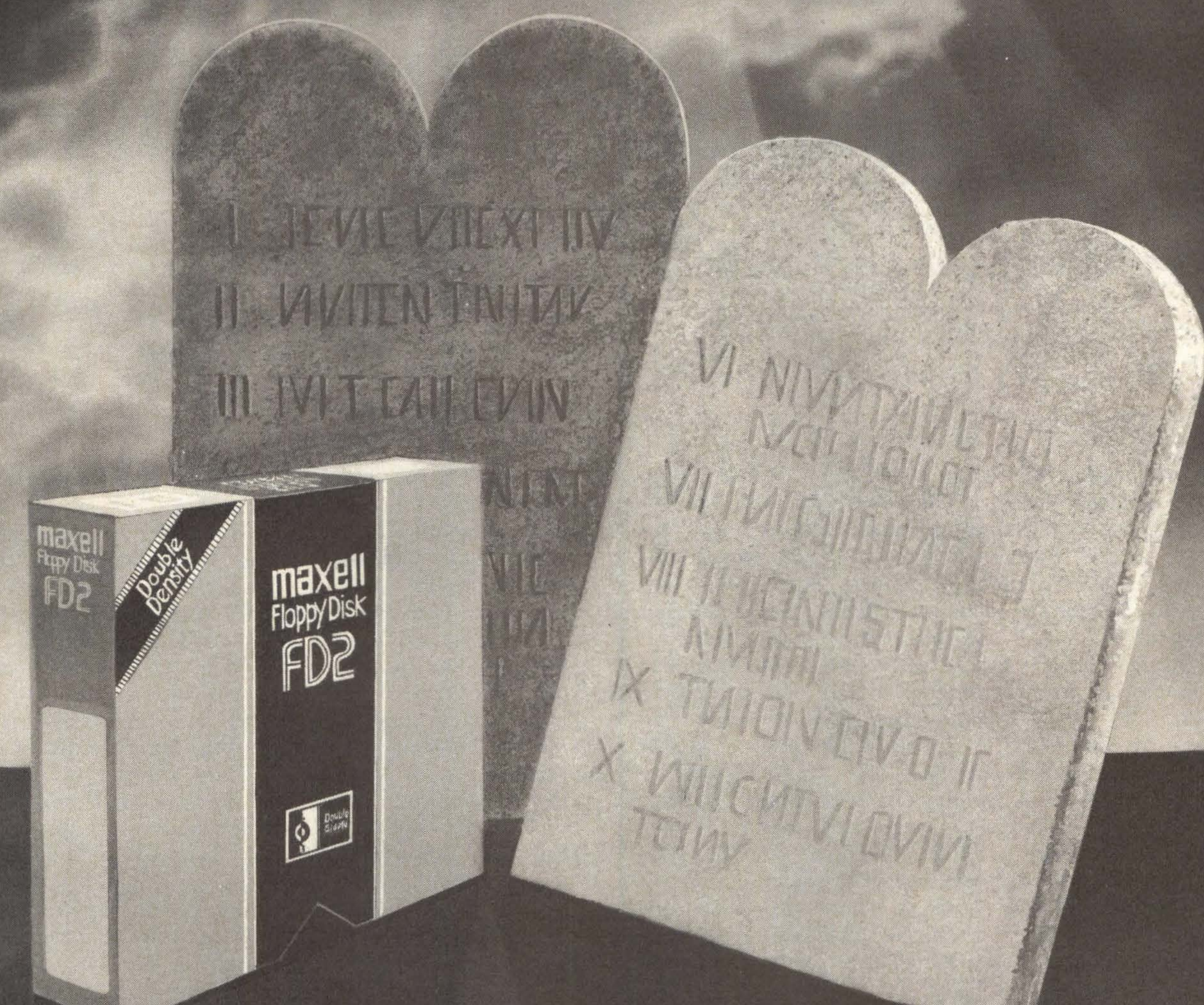
Maxell double density floppys. When the data is too important to lose.



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CIRCLE 13 ON INQUIRY CARD

SWITCHED NETWORK SERVICE ALTERNATIVES

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

In January the United States Supreme Court issued another decision whose ramifications will radically influence future telecommunications applications and systems. The legitimacy of the Execunet service provided by MCI was upheld by the Supreme Court's refusing to hear an appeal on a lower court decision. The appeal by AT&T centered around the fact that MCI's original charter as a specialized communications common carrier was to provide leased communications facilities, not switched communications services as exemplified by Execunet. It is reasonable now to expect renewed marketing of Execunet by MCI as well as the introduction of a number of competing switched network services from other specialized communications common carriers such as SPCC, USTS, et al.

This third major telecommunications action of the current Supreme Court session encourages new competition and continued erosion of the traditional communications common carrier's control of the telecommunications marketplace. The fact that approximately 60% of AT&T's annual revenue is derived from switched network services indicates the intensity with which AT&T opposed the MCI Execunet service.

Telecommunications is rapidly becoming used by the data processing community. The primary application area prompting this growth has been interactive data processing and its associated database management applications. Short randomized data communications between the remote interactive terminals and a centralized database-oriented processing center characterize these uses. A switched network access is more desirable than a more rigid leased network access when the parameters of network reliability and dynamic load balancing capability are considered.

Under today's communications tariffs, the leased line still provides the lowest potential cost per transmission unit for data or voice communications. To capitalize on this cost factor, many interactive systems utilize multiplexed leased lines that can be reached at the remote end using the localized portion of the switched network; this combination has been prompted by the limited tariff options available with an exclusive switched network usage. Current interstate switched network tariffs from AT&T include only toll and WATS services, and provide only voice grade communications channels. Both of these tariff alternatives have economic limitations that restrict their exclusive use as a remote terminal access network. As a result, many of these types of applications have elected to implement the multiplexed leased line network with remote local dial access. Reliability and lower cost are provided by the local switched network coupled with redundant leased line channels.

Today's specialized common carriers were originally authorized by the Federal Communications Commission to provide leased communications services. Besides a few experimental attempts to provide switched communications services under the guise of "shared leased lines," the specialized common carriers have concentrated their service offerings on the leased line marketplace. They have attempted recently to compete directly with AT&T for the considerably larger and more lucrative switched network service such as MCI Execunet.

These specialized communications common carrier switched network services are based on the use of the local switched network to reach communications channels of the specialized common carriers. Actual long distance transmission utilizes non-AT&T facilities to the remote destination city where the local switched network is connected to the desired remote location. The only revenue telephone companies will realize would be for local telephone calls if those areas use local usage sensitive rates such as message units. Actual long distance revenue will be realized exclusively by the specialized common carrier.

CABLEGRAMS FROM

Now you can mass terminate twisted pair cables.

Spectra-Strip's Twist 'N' Flat Cable is great when you need reduced crosstalk and fast, low-cost, mass termination. In applications like high speed computer and communication equipment using digital techniques.

Our standard Twist 'N' Flat comes with 26 solid or 28 stranded AWG wire. The twisted section is 18" and parallel section is 2" with conductors on .050" centers. Custom configurations are available that vary the wire gauge, pitch and length of the twisted and parallel sections. You also get the same crosstalk characteristics of our Twisted Pair Cable.

Twist 'N' Flat. Another unique idea patented by Spectra-Strip.

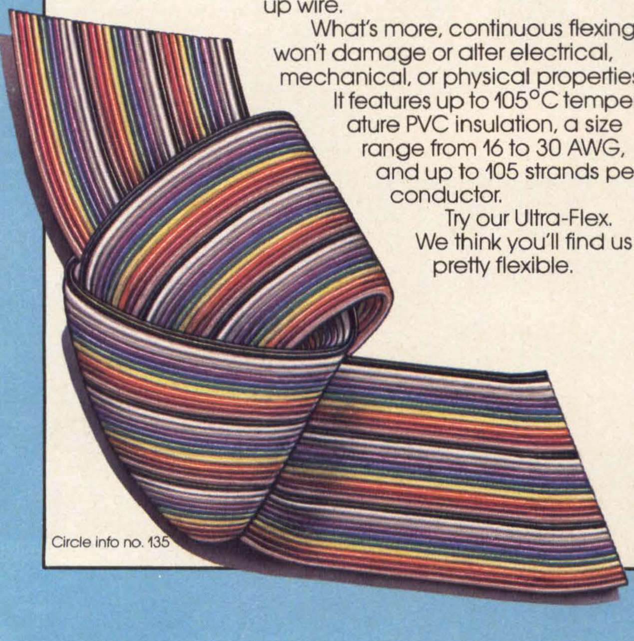
Circle info no. 130

Ultra-Flex Bonded Cable bends with your needs.

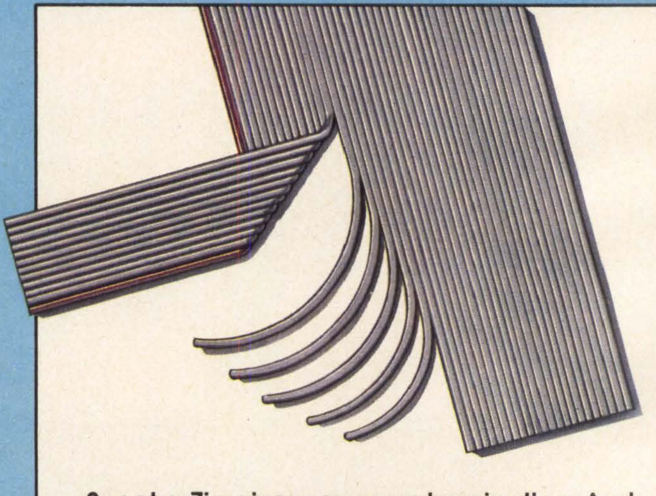
Our Ultra-Flex Bonded Planar Cable is designed for constant or frequent flexing. With all the advantages of our standard Bonded Planar Cable—excellent controlled bonding, easy separation for breakouts, and standard termination techniques used for hook-up wire.

What's more, continuous flexing won't damage or alter electrical, mechanical, or physical properties. It features up to 105°C temperature PVC insulation, a size range from 16 to 30 AWG, and up to 105 strands per conductor.

Try our Ultra-Flex. We think you'll find us pretty flexible.



Circle info no. 135



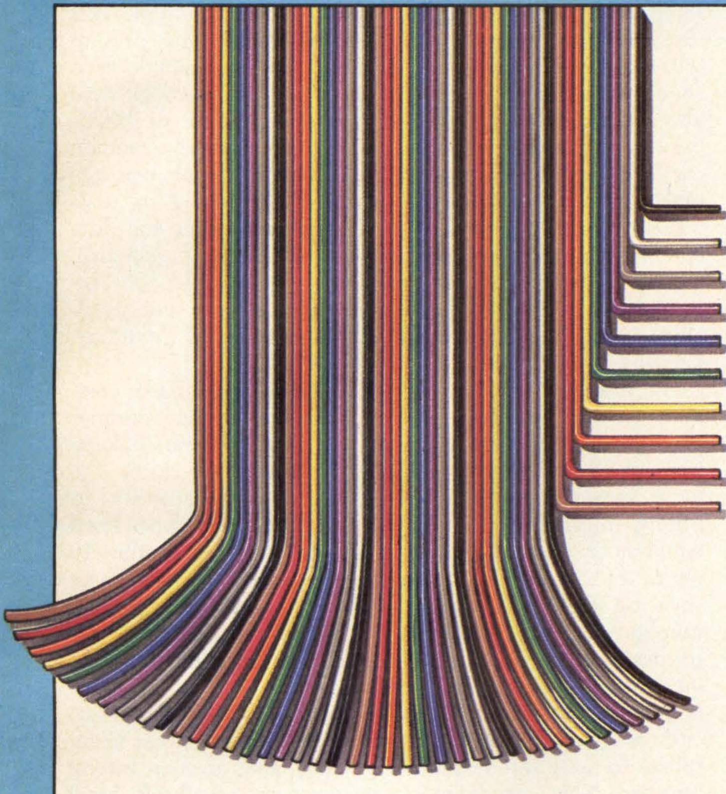
Spectra-Zip gives you mass termination. And fast, easy breakouts.

For general purpose interconnection from calculators to computers, Spectra-Zip Laminated Planar Cable offers you economy. Reliable performance. Weight and space savings. Controlled electrical characteristics. And low-cost termination.

Spectra-Zip's convenient double contour feature lets you assemble IDC connectors on either cable surface. And assures you of easy, uniform breakouts. Every time.

Circle info no. 132

SPECTRA-STRIP.



Our 3C Color Coded Cable gives you predictable performance.

Our 3C Color Coded Cable is just right for digital and signal transmission applications. It's designed for use with many labor-saving termination techniques, including Spectra-Strip IDC Connectors.

3C Cable's precise control of critical design and manufacturing parameters provides important predictable electrical benefits—such as impedance, capacitance, crosstalk, and attenuation. Cable comes in sizes up to 64 conductors, with a tear feature for easy conductor breakouts.

And it's brought to you in living color.

Circle info no. 134

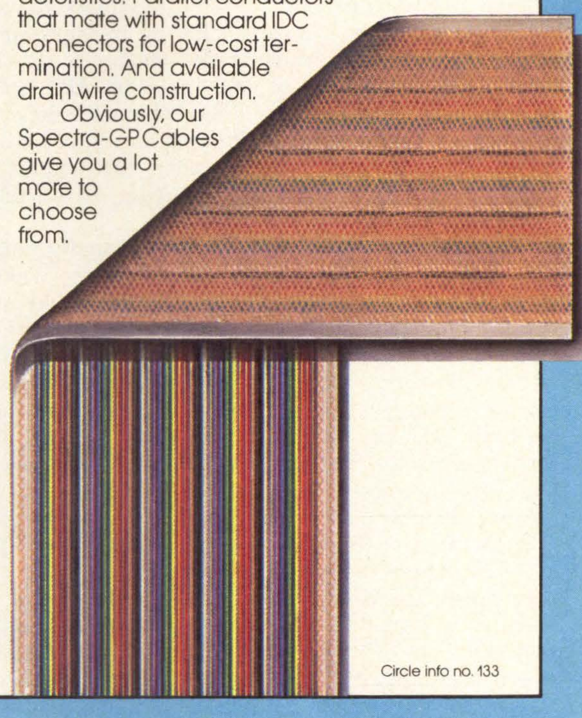
Spectra-GP Ground Plane Cables. For reduced crosstalk and increased shielding.

Our Spectra-GP Ground Plane Cables give you the greatest variety of configurations available anywhere. You can choose our standard Gray Cable. Or our Color Coded Cable. You can even get it in a Twisted Pair configuration.

Spectra-GP is perfect for interconnection applications where reduced crosstalk and increased shielding is needed. And it's perfect for computer and communications equipment that use high-speed techniques for switching and data transmission.

Add to this features like precise conductor spacing for controlled electrical characteristics. Parallel conductors that mate with standard IDC connectors for low-cost termination. And available drain wire construction.

Obviously, our Spectra-GP Cables give you a lot more to choose from.



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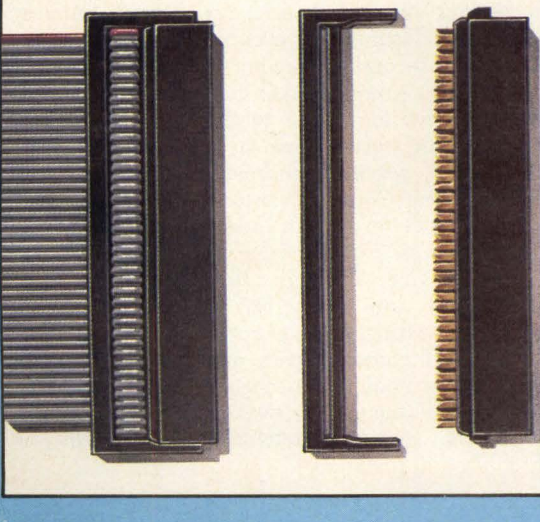

At Spectra-Strip, we'll give you the right connection.

We also make a lot more than ribbon cables

We make a wide range of IDC connectors, headers, and other ribbon cable connectors. Complete planar systems, including standard interconnects and custom assemblies, are our specialty.

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Nobody has a greater variety of ribbon cables and connectors than we do. Nobody.

And we intend to keep it that way.

Circle info no. 131

SPECTRA-STRIP

ALL WE DO IS KEEP EVERYTHING TOGETHER.

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an Eltra company

Several switched network service offerings, which will initially emulate existing AT&T switched networks such as long distance toll and WATS, can soon be expected from various specialized common carriers. Primary uses will be for voice communications such as the Execunet service; however, limited data communications at low speed will be feasible. It is foreseeable that some specialized carriers will specifically address the growing demand for reliable switched data communications services, following two general patterns. First, charges will be structured on a selected bandwidth basis similar to the concept of the Western Union Broadband Service. Secondly, discount arrangements based on geographical areas, calling volumes, and/or time of day will be provided, such as those available with WATS.

A forerunner of these services, the Western Union Broadband Switching System, developed in 1960, structured charges on the basis of distance between dialed locations, call connection duration, and selected channel bandwidth. The major distinction between this switched data service and traditional switched voice services is that the latter provides only the "choice" of a single bandwidth—the nominal voice-grade channel.

Data communications system designers have long anticipated having a wide choice of transmission bandwidths. Traditional voice-grade channels provide an operational bandwidth of 600 to 3000 Hz. Some improvement of the relative delay characteristics can be realized with channel conditioning or equalization, but it would be minimal at best since the nominal bandwidth of 4 kHz is fixed by the nature of the telephone carrier systems.

This restricted bandwidth has profoundly influenced the design of modulators/demodulators (modems), since all modems intended for a switched network application must "fit" the bandwidth limitations of the nominal voice-grade channel. Higher data transmission rates, therefore, required the development of more complex multilevel synchronous modems that increased not only the cost but also the error rate probability. To compensate for the reliability degradation, many high speed voice-grade channel modems also include forward error correction procedures.

Specialized common carriers occasionally have planned to offer various bandwidths to the marketplace. While previously discussed only in the context of leased lines, it is imminent that the evolution of competitive switched network services will provide users with selective bandwidths and corresponding rates. This form of communications service will most likely evolve slowly since higher speed, wider bandwidth modems must be developed to realize the complete economic advantages of such a future switched network service.

Usage discount tariffs will probably be offered first by the specialized common carriers. WATS tariffs are basically volume discount services. AT&T contends that WATS is separate from toll service and therefore warrants a separate tariff. Presently, regulatory agencies and AT&T are examining the basic nature of the WATS service to determine this. In either case, WATS users are offered a potentially lower cost if the calling volume to or from a specified geographic area is concentrated over a limited number of switched network access lines. Similar anticipated services would be expected initially to follow the geographic volume discount concept of the WATS tariffs. The specialized common carriers usually service specific urbanized centers as opposed to broad geographic areas serviced by AT&T. A specialized common carrier discount service probably will be concentrated in urban centers. For example, unlimited calling might be permitted from city A to city B for a fixed charge per month, which would be analogous to a usage-sensitive, multichannel, foreign exchange service between the two cities.

Other potential variations would be a single 2-way service permitting calls between two designated cities to originate from either city, with both included in the same rate package. Evening and night communication discount rates might be offered, similar to the present toll interstate charges. A dedicated leased channel used at either or both ends of the switched network will also be a common configuration. Comparable to MCI's Service 12, direct access to the specialized common carrier's switched network would avoid local message unit charges and simplify required addressing or dialing procedures. It would also be advantageous for data communications applications in that wider bandwidth, and/or 4-wire channel configurations would be required. Such local channel configurations are not available from the telephone companies' local switched networks.

An inherent disadvantage of current specialized common carrier switched network services is the number of digits that a user must dial to reach a remote location. A 7-digit local number is dialed to reach the local switched network access location; a security or billing number must be dialed for the specialized common carrier to properly bill the call; and the 10 digits of the desired remote telephone number must then be dialed. Assuming a 5-digit security or billing number, a total of 22 digits must be dialed in order to use this service. Not only is the number of digits inconvenient, but the probability of a dialing error is greatly increased. Concerning security, any unknown call originator could generate calls and have them billed to a different party by using that party's billing number. This disadvantage is overcome easily if local leased lines are installed between the customer's location and the specialized common carrier's local switched access location.

A limitation of future specialized common carrier services will become obvious with the growth of computerized automatic call routing PBXs. Telephone systems such as the Western Electric Dimension and the Rolm CBX enable the user to route calls automatically over predesignated facilities and services. These computerized telephone systems presently cannot respond to secondary dial tones to complete the desired dialed digits. When the local switched network is seized, a dial tone is recognized which results in the automatic dialing of the local telephone number of the specialized common carrier's switched network access. Once this access is connected, a second dial tone occurs to permit the dialing of the security or billing number and the desired destination number. Unfortunately, recognition of the second dial tone is not within the capabilities of today's computerized PBX systems. Again, local dedicated leased line access to the specialized common carrier's switched network can bypass this limitation.

Switched network service offerings forthcoming as a result of the Supreme Court's decision will provide data and voice communications with additional alternatives for achieving optimum calling value. As with any new communications service offerings, this improved value is never guaranteed but is merely potential. The individual user organization must assure that the expected calling volumes and characteristics are compatible with the service's value potential; incompatibility among these factors could incur an even greater cost. All advantages of the switched network services will be proven only in their application.

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Fully Automated Diagnostic and Control System Offers Unattended Monitoring of Data Communications Networks

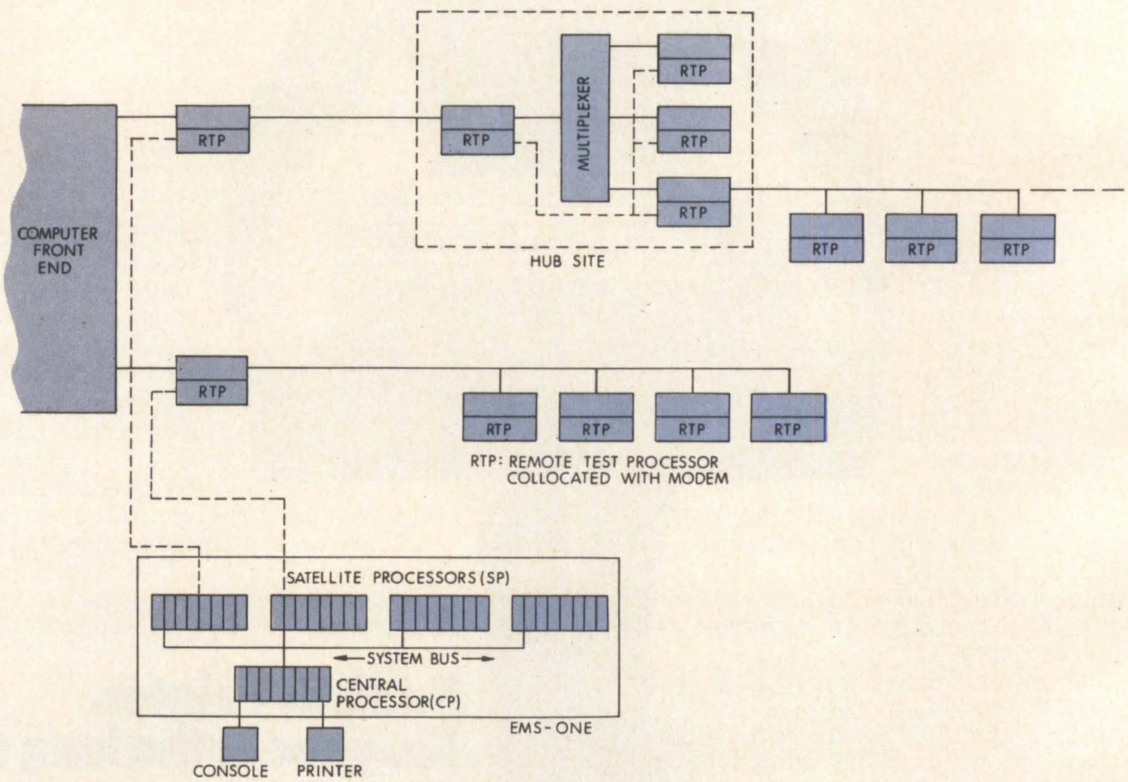
As a third generation of network control systems for users of real-time interactive data networks, the EMS-One event-oriented control facility delivers faster performance with greater line and drop capacity. Use of real-time monitoring for identifying network problems overcomes a weakness of many real-time distributed data processing networks. The system continuously monitors the entire data network by distributing its own power in the same way that interactive EDP systems do. Continuous network monitoring is obtained without dedicating the task to an expensive frontend processor or customized software.

Intertel, Inc, 6 Vine Brook Pk, Burlington, MA 01803 has designed the system to control up to 160 lines and 6400 drops of data networks containing point-to-point, multipoint, or multiplexed transmission facilities, as well as distributed processors. Most combinations of 4-wire transmission facilities can be serviced by the company's modems, options, and diagnostic system.

Four operating modes are automatic network configuration learning (self-learn), background monitoring (auto monitoring—AM), programmed in-depth testing (auto predictive maintenance—APM), and a comprehensive, manually initiated test and control capability (manual mode). In self-learn, a processor at the central site can query the system automatically, learn its configuration, and build a directory without operator intervention.

The system can operate on an unattended basis with automatic monitoring mode, continuously checking status of all lines and drops in the network to determine what changes are taking place. Scanning of a network with 10 lines and 20 drops/line occurs in less than 60 s. In pinpointing problems, the system makes diagnoses, based on events or status changes, and displays full details in English, with data simultaneously recorded as a printout.

In APM mode, the system is user programmed to automatically initiate on and offline testing at specific times of the day. Results are recorded by the printer, allowing completely unattended operation during off-hours. Hardcopy records can be used as an indicator of trends in equip-



EDP system configuration is combined with Intertel's EMS-One control system for network monitoring and diagnostic testing of data communications networks. Architecture of system is structured with CP for operator I/O, and SPs connected to system bus. SPs acting as frontend processors perform inquiry/response polling of RTPs located downstream in data network

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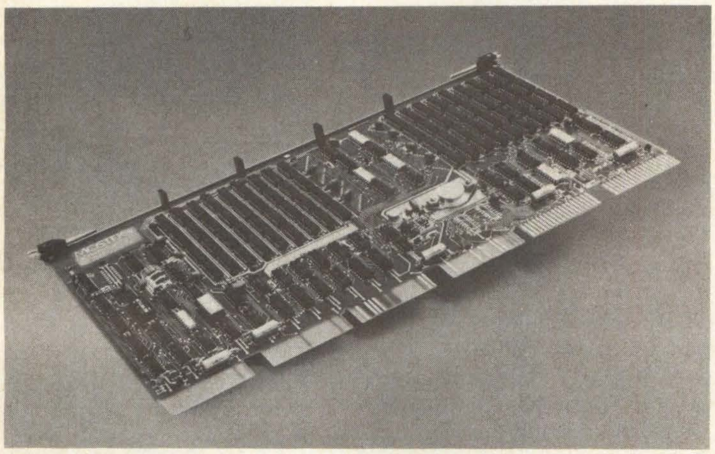

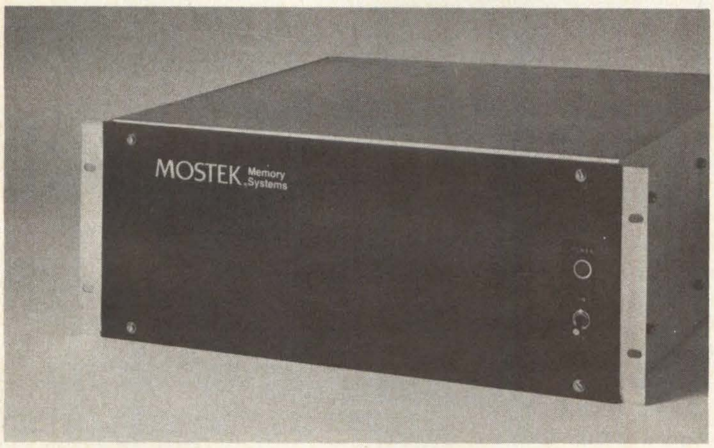

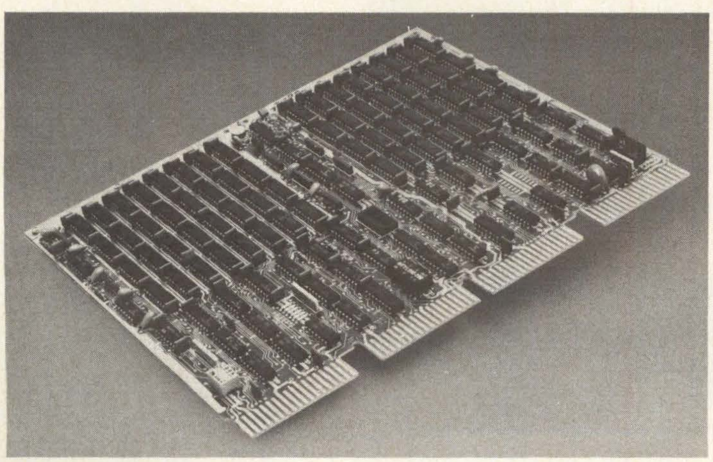

Mostek Memory Systems provides a complete line of super-dense memory boards with performance and reliability to match our industry-standard dynamic RAMs. Each board undergoes extensive burn-in and testing prior to shipment and comes with a full one-year warranty. In addition, you get highly competitive prices, OEM discounts, and immediate availability.

PDP-11* The Mostek 8001 has a number of capacity options that include 16K, 32K, or 64K words by 18 bits on a single hex board. And it's fully hardware and software compatible with Digital Equipment Corporation memory modules.

PDP-11/70* The Mostek 8601 memory system in a 7-inch chassis provides up to 1 megabyte of storage with ECC and logging. It's the most compact 11/70 add-on memory available, making possible upgrades from 128K bytes to 4 megabytes of total storage.

LSI-11* The Mostek 8002 is a totally hardware and software compatible card for LSI-11/PDP-11/03. This add-in memory system ranges in capacity from 8K to 32K words x 16 bits on a quad card allowing you to place the maximum capacity on a single card.

Call now for the complete story. Either the Eastern office 201/842-5100, Western office 408/287-5081, or Memory Systems Marketing at 214/242-0444, extension 2552. Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. In Europe, contact Mostek GmbH, West Germany; telephone (0711) 701096.

MOSTEK. Memory Systems

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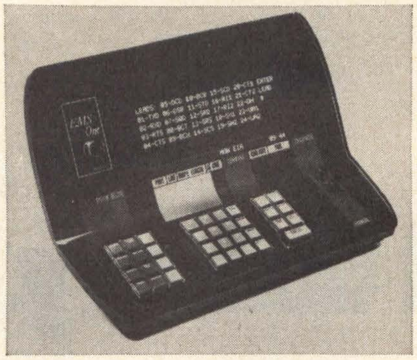


Operator's console of Intertel EMS-One event management system contains keyboard and display. Prompting aids guide operator through command input steps; tests and sequences are called forth by simple keystrokes. No programming language is involved; console communicates in English and numerics. Printer is also supplied for use in all logging functions; together they comprise desktop workstation, housing all central site electronics

ment performance for predictive failure analysis. In manual operation, the user initiates a test directly by keystrokes on the console keyboard; results are shown on the console display and may be recorded by the printer.

The EMS-One's architecture, like that of a distributed data processing system, has a central (CP), satellite (SP), and remote test (RTP) processors. By keeping processing as close to the source data as possible, data transmission efficiencies and speeds are improved. The controller is based on a firmware-driven, multiple processor design; the central controller consists of a CP connected to a system bus. Operator I/O devices connect directly to the CP through serial interface ports.

Also connected to the system bus are multiple SPs, which control operations in self-learn and AM modes, and also serve as interface to the user's network. Each SP behaves much like a frontend processor, and is responsible for inquiry/response polling of all RTPs, which are connected directly or indirectly over telephone lines to its ports. The RTP continuously performs 14 tests at each remote drop to accomplish status check.

Polling of all lines occurs simultaneously in parallel, thus the longest time to scan a network is governed by the line with the most drops, not by the number of lines. The modular structure, processor power, memory capacity, and I/O support are upgradeable.

Primary system interface is through an operator console, from which operations for all ports, lines, and drops can be controlled. It comprises a keyboard and display. The console, together with a record-only printer, constitute the workstation. Scheduled for delivery in early 1979, the systems will have prices ranging from approximately $125k for small systems having 10 lines with 55 total drops to approximately $375k for large systems having 30 lines with 160 total drops.

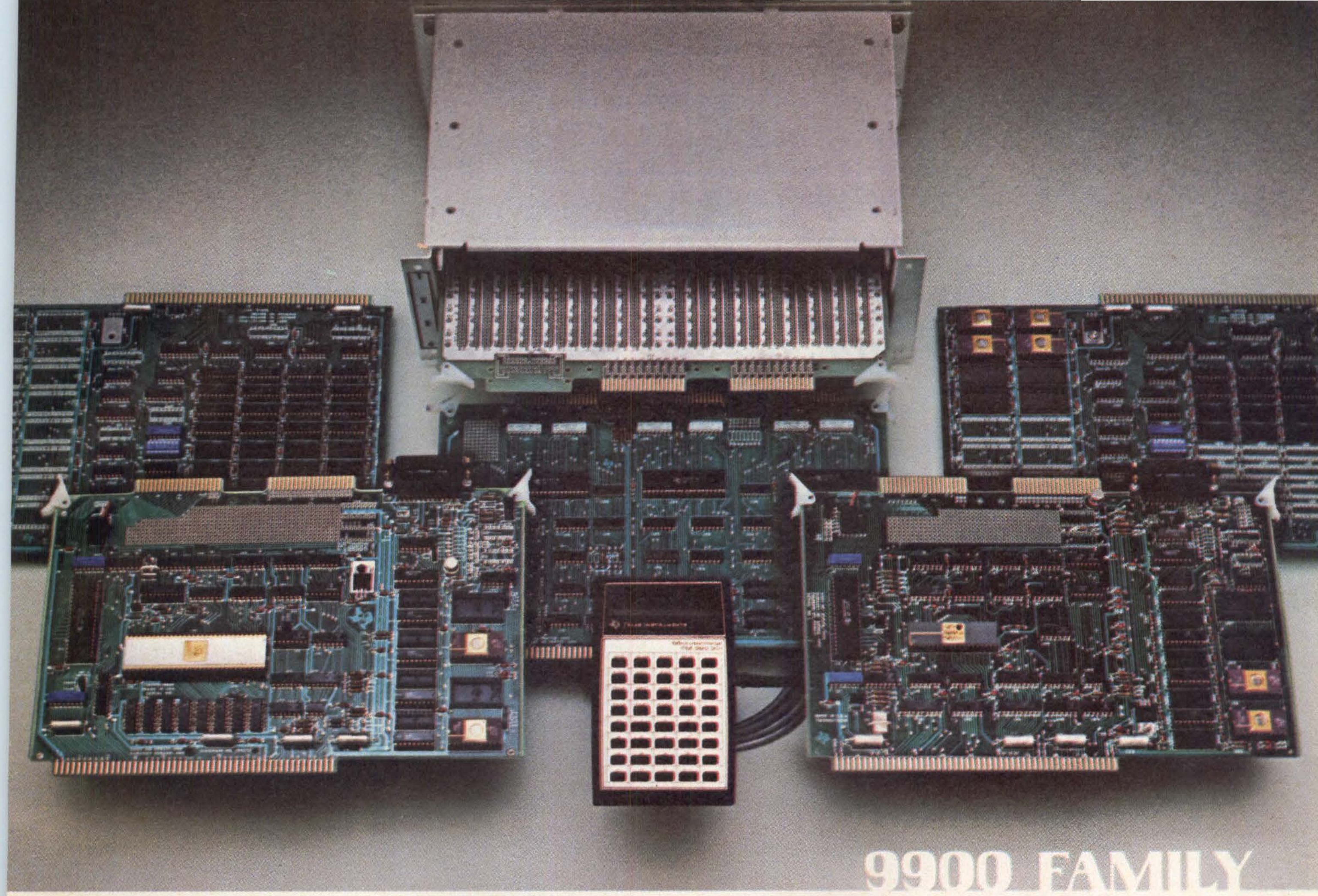
Circle 400 on Inquiry Card

Short-Haul Multispeed Modem Operates Over Doubled Distance

Operation of the Com-Link III short-haul modem over 19 to 26 gauge wire circuits up to 125 miles (40 km) long, rather than the previous 10 miles (16 km), is possible with the addition of automatic adaptive equalization and delay modulation features. The equalizer compensates for circuit amplitude variances, providing initial line equalization in less than 2 ms. Transmission is facilitated with delay modulation by allowing operation in a narrower bandwidth at higher power. Error rates are better than one in 100k bits.

The standalone 1.75 x 8 x 12" (4.4 x 20 x 30-cm) modem operates at strap-selectable synchronous data rates from 2400 to 19.2k bits/s. Suited for use in point-to-point and multipoint data communications systems where many terminals are close to a central computer, this unit may be used with a multiport modem to allow local terminals up to several miles apart to economically share a common long-haul circuit.

Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166 has built in expanded test capability. Remote test



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- TM 990/402–Line-by-line assembler preprogrammed into the EPROM. $100.00*.
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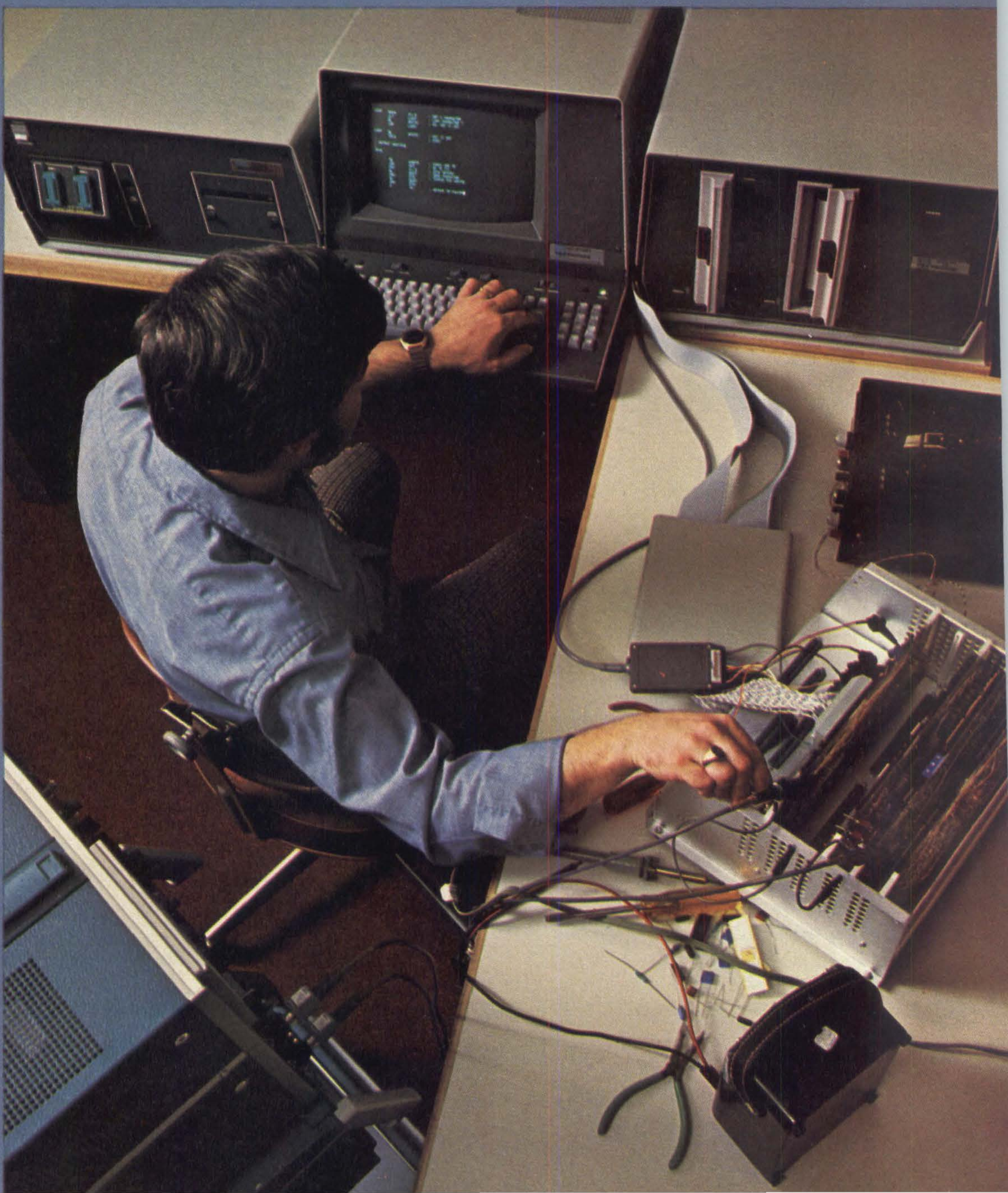

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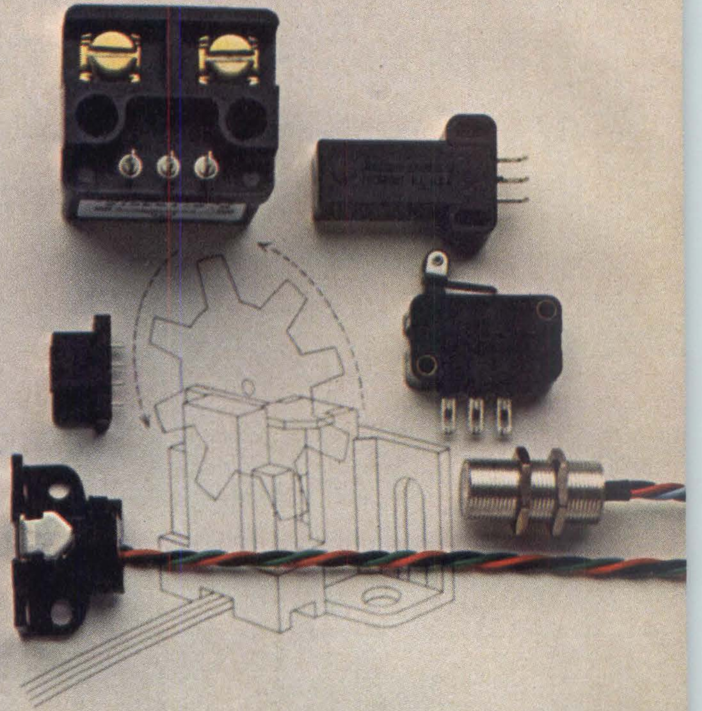
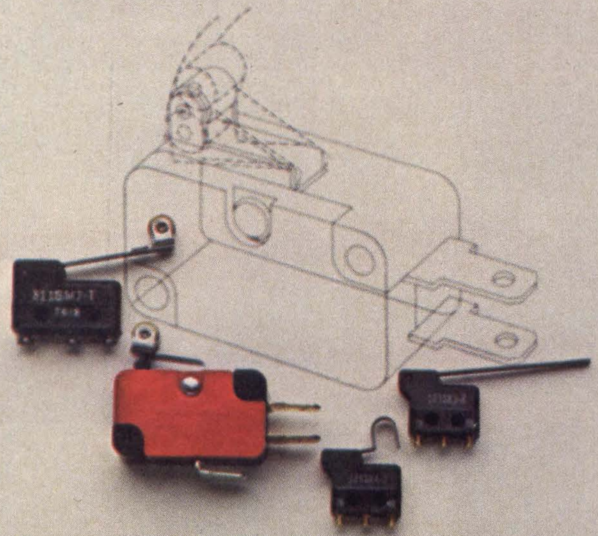
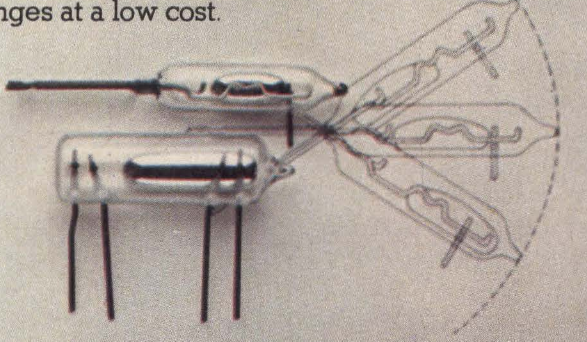




Snap-action V3, SM and SX switches offer wide variety of actuators, electrical capacity and termination.

Mercury switches offer hermetic sealing, a variety of electrical capacity and broad temperature ranges at a low cost.



AML manual devices for low installed cost, electrical flexibility and attractive panel appearance. Series 8 miniature manual switches provide small size and wide variety of operators. DM offers inexpensive snap-in panel mount design.

Solid state keyboards provide high reliability no mechanical keyboard can offer. Panel sealed versions also available.

allows an operator at either end of a point-to-point line to place the unit into a DTE loopback mode for fault isolation and testing. A self-test feature allows onsite checking using a built-in test pattern generator and error detector. Multicolor LED status displays provide a visual indication of modem operation including power, testing, error detect, RTS, DCD, and transmit/receive data status. Power is provided by a 4-W wallmount transformer that operates on 105 to 125 Vac.

Circle 401 on Inquiry Card

Telecommunications Bank System Uses CCITT Compatible Modems

A reliable data transmission network based upon IBM's System Network Architecture concept is in use at Multibanco Comermex of Mexico City to connect the system's branches for better daily service. Containing an IBM-3600 financial system, the Multitronic system has an IBM 370/125, 370/135, and two 3704 communication processors for complete backup, online operation. The system's 140 data terminals are linked by 1200-bit/s modems used at the branch level and 2400-bit/s modems used at the data processing center level.

General de Telecommunicaciones S.A. supplied the modems manufactured in Mexico under license from Vadic Corp, 222 Caspian Dr, Sunnyvale, CA 94086. The two types are VA1200L CCITT V.23 compatible 1200-bit/s modems, and VA2400L CCITT V.26 compatible 2400-bit/s modems. Each processor manages the entire network because of data divider bridges following the 2400 modems; the bridges accept four 360 terminal controls, backing up both types of modems, which are housed in 16-channel multiple mounting racks.

Single-Chip Circuit Controls Communications Peripherals and Data

Control of communications peripherals and formatting of data in communications networks are key capa-

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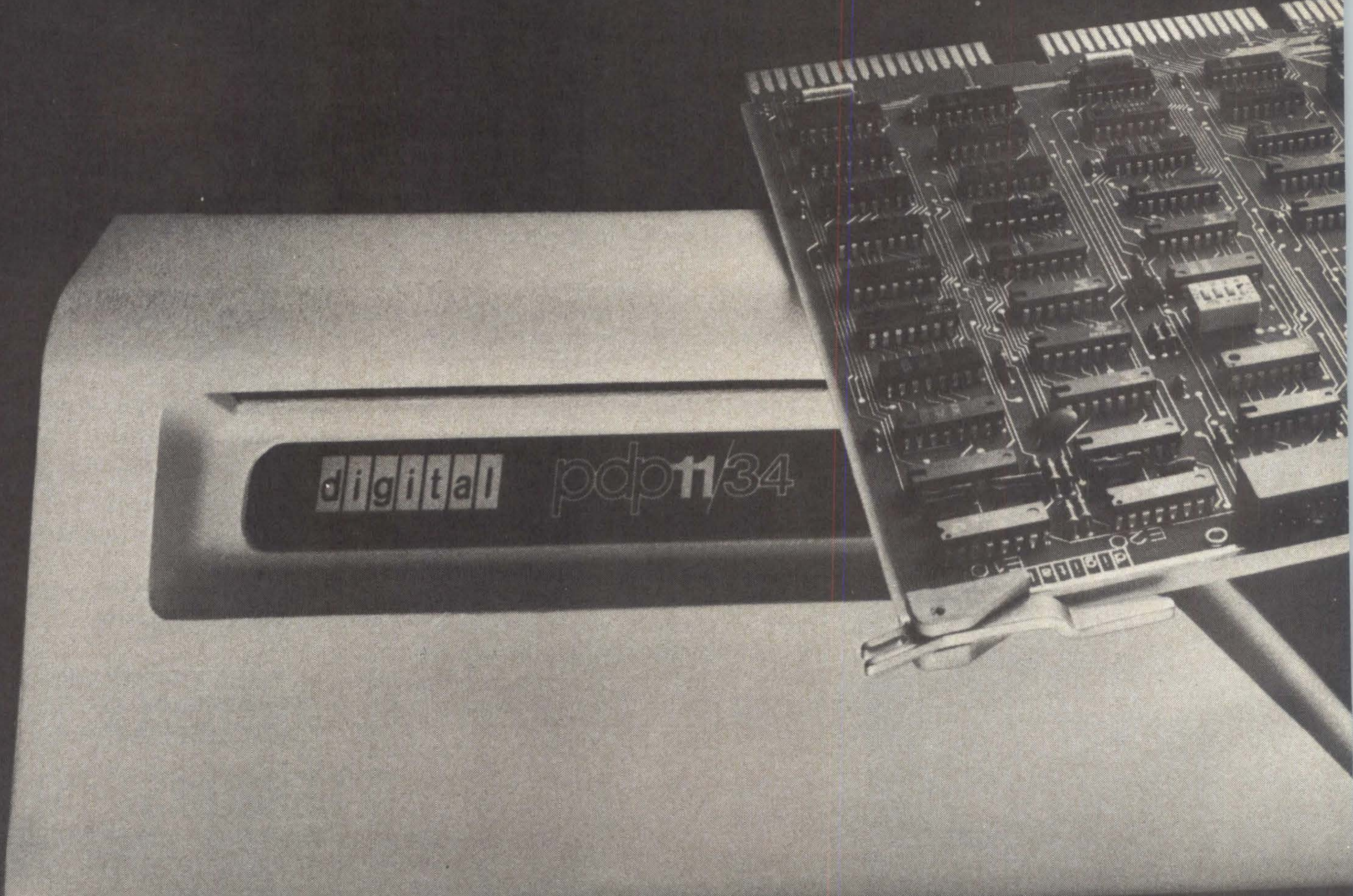
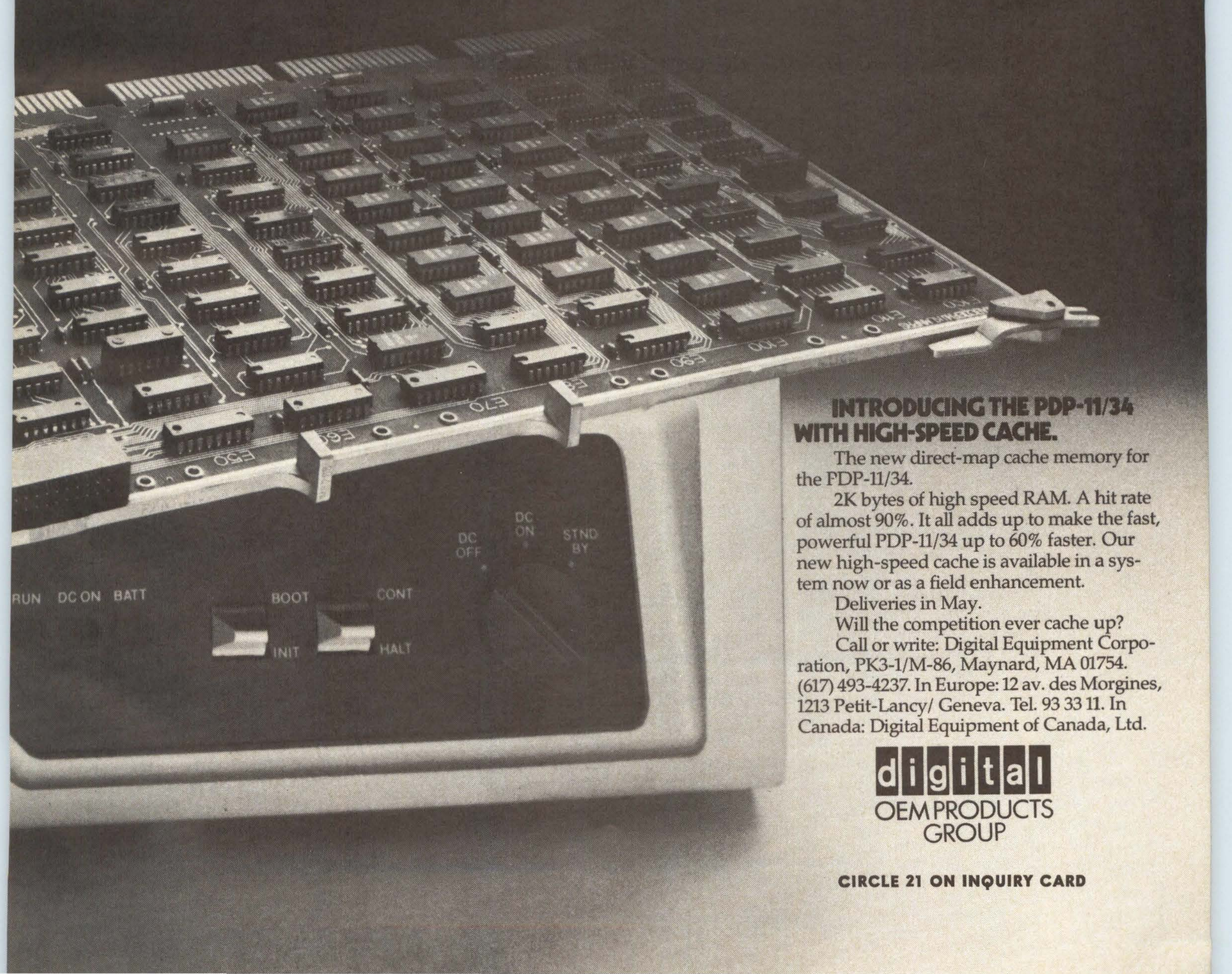
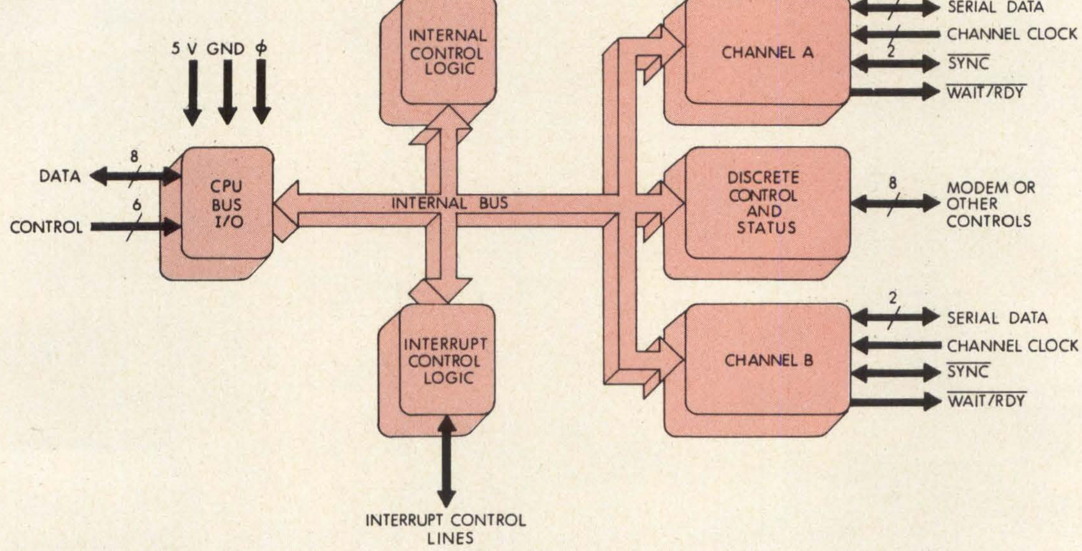




RUN DC ON BATT
BOOT
INIT
CONT
HALT
DC OFF
DC ON
STND BY



Block diagram of internal structure of Zilog's Z80-SIO serial I/O controller circuit. Designed to work with Z80 microcomputer family, it can also interface with most other 8- and 16-bit processors to provide communications capabilities

bilities of the single-chip Z80-SIO, which is said by Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 to be the first high speed, dual-channel, multiprotocol serial data communications controller circuit for advanced LSI microcomputer systems. Data rates for the 40-pin serial input/output (SIO) peripheral component are claimed to be 10 to 15 times faster than comparable devices, suiting it to such high speed applications as fiber-optics, microwave transmission, and satellite communications. For systems with a 2.5-MHz CPU clock rate, the data rate goes up to 550k bits/s; for a 4-MHz system it is 880k bits/s.

Using n-channel-gate depletion load technology, the chip achieves high levels of logic density and functional integration. Components are a Z80 CPU bus interface, internal control and interrupt logic, and two full-duplex channels. The structure also holds a single 5-V power supply and single-phase 5-V clock. In small quantities the chip costs $54 in a ceramic package and $49 in a plastic DIP.

The circuit works with the Z80 microcomputer family and interfaces easily with most 8- and 16-bit processors. In a system with several chips, the others may be included in the daisy chain interrupt structure with either higher or lower priority than the SIO channels. Fast, powerful interrupt processing occurs without added hardware overhead.

The chip can handle asynchronous, synchronous, and synchronous bit-oriented protocols such as IBM Bi-Sync, HDLC, SDLC, and other serial protocols. CRC codes are generated in any synchronous mode and can be programmed by the CPU for asynchronous format.

Each channel has five 8-bit control registers, two 8-bit status registers, and two 8-bit sync character registers. The receiver has three 8-bit buffer registers in FIFO arrangement, in addition to the 8-bit input shift register. The transmitter has one 8-bit buffer register with an 8-bit output shift register.

The serial-parallel, parallel-serial converter/controller contains eight registers that are programmed by the system software to optimize functions for communications applications. Three registers can be read to obtain the status of each channel, including error conditions, interrupt vector, and standard communication interface protocol signals.

For programming, the system's software issues a series of commands that initialize the basic mode of operation desired and other commands to qualify conditions within the selected mode. The circuit's command structure benefits from the Z80's block I/O instructions to simplify programming, reduce overhead, and optimize CPU interaction activities.

Circle 402 on Inquiry Card

Fiber-Optic Data Link Introduces Optical Communications System

A fiber-optics data link designed for use in digital data computer links, digital telephony, secure communications, process control, and high voltage optically isolated data systems is the initial response of RCA Electro-Optics and Devices, New Holland Ave, Lancaster, PA 17604 to provide customers with a complete fiber-optic communications system. Model

The price you pay for success just went down. Way down.

You pay a price to be successful with computers. A high price.

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For more information, write Perkin-Elmer Data Systems Sales and Service Division, 106 Apple Street, Tinton Falls, New Jersey 07724 or telephone toll-free (800) 631-2154.

PERKIN-ELMER
Data Systems

C86003E was developed by scientists of RCA Laboratories in Princeton, NJ who worked with engineers of RCA Electro-Optics and Devices. The transmitter, receiver, and connector are $850. Fiber-optic cables varying in length from several meters to 1 km can be used depending on fiber characteristics.

The transmitter of the 20M-bit/s digital data system contains one of the company's GaAlAs LEDS with associated electronics for the drive circuit. A cable is coupled internally from the emitting region of the GaAlAs chip to an optical bulkhead connector. The transmitter operates from 5 V ±5.0% (typ) and 250 mA. Peak optical power output is 100 μW min.

The receiver uses the company's silicon p-i-n photodiode with amplifier and threshold drive circuits to convert input light pulses to standard electrical output signals. Positive and negative voltages are 6 V (typ); positive and negative currents are 30 and 20 mA, respectively; and positive diode bias is 6 to 45 V (typ). Optical sensitivity is 2 μW. Transmitter and receiver are housed in compact modules each measuring approximately 2 x 2 x 1" (5.1 x 5.1 x 2.5 cm).

Circle 403 on Inquiry Card

Three Models Offer Various Desktop Switching Functions

Expanding the series 8500 MiniTech[R] desktop switching modules, International Data Sciences, Inc, 100 Nashua St, Providence, RI 02904 has introduced three additional models which require no power and have all connections made at the rear panel. Model 8506-D A,B selector switch is used to switch the 25-pin EIA RS-232 or CCITT V.24 interface to either of two outputs. A modem can be switched to one of two frontend processor data channels or to either of two data terminals. A data channel may be switched from an online to backup modem or from a leased line to dialup modem.

A spare modem backup switch, model 8509-D switches the combined EIA RS-232 and telephone line interface of a faulty online modem to a backup system. A "chaining" feature, which allows a single spare modem to be switched in to replace any of a group of online modems, eliminates the need to immediately replace a faulty modem.

The final addition is the 8574-D A,B,C,D,E,F CRT selector switch. The user manually selects any of six CRT displays. A 6-position rotary switch on the front panel instantly switches any 2-wire input from a rear panel to any one of six 2-wire outputs. The unit is suited to switching the IBM 3270 interface or any 2-wire telephone line.

Circle 404 on Inquiry Card

X.25 Interconnection Permits Linking of Packet Networks

The interconnection of Canada's Datapac network with TYMNET, a U.S. public packet network developed by Tymnet, Inc, 10261 Bubb Rd, Cupertino, CA 95014 is claimed to mark the first commercial linking of packet networks using the international X.25 protocol. The interconnection allows communication between data terminals and host computers in both countries. Typical applications include variations of timesharing and database access.

Charges for the 110- to 300-baud service vary according to terminal type and access location. Dialup terminal access in Canada to U.S. host computers ranges from about $4 to $10/h of usage.

Facsimile Systems and Network Advance Use of Electronic Mail

Full-scale development of fast and accurate facsimile equipment, which transmits text, photographs, and graphics over telephone lines or via satellite, for electronic mail use has been hampered by the lack of compatibility among equipment, and the lack of universally accepted specifications for facsimile communication. Graphic Sciences, Inc, Corporate Dr, Commerce Pk, Danbury, CT 06810 has taken a step toward easing this problem with their dex 1100 and 5100 facsimile transceivers. Compatibility among systems provides the DEXNET communications network with greater capabilities for facsimile use.

The 1100 series of three microcontroller-based systems can communicate with other dex models which operate in the am mode, with other machines that meet CCITT technical specs, with fm facsimile equipment, and with the dex 5100. They print by means of a controlled-voltage stylus operating on electrosensitive paper. Scanning is done by a mobile head moving along a rotating drum.

All three operate at 96 lines/in (38/cm) at 6 min/page, and 64 lines/in (25/cm) at 4 min in the fm mode. Vertical resolutions of the 1102 and 1103 are 88 lines/in (35/cm) at 3 min, and 62 lines/in (24/cm) at 2 min in dex am mode; and 96 lines/in (38/cm) at 3 min in CCITT am mode. Features include bidirectional editing indices, automatic electronic handshake, and operator interrupt capability. Acoustic couplers are built into the 1101 and 1103.

The 5100 digital system can send or receive a full page of information at subminute rates over voice grade telephone lines. It consists of a modular microprocessor architecture, automatic document feed, unattended operation, and copying capability. Automatic dialing from internal electronic telephone directory, and compatibility with high speed analog devices are optional, as is a 9600-bit/s CCITT model that sends and receives simultaneously.

An array of 1728 styli print transmitted information on electrosensitive paper. Each scanning element transmits one, two, or three points depending on degree of vertical resolution desired: 65, 98, or 196 lines/in (26, 39, or 77/cm). The system utilizes a CCITT 4800/2400-bit/s send or receive modem, CCITT compression technique, and CCITT T30 protocol for control signaling.

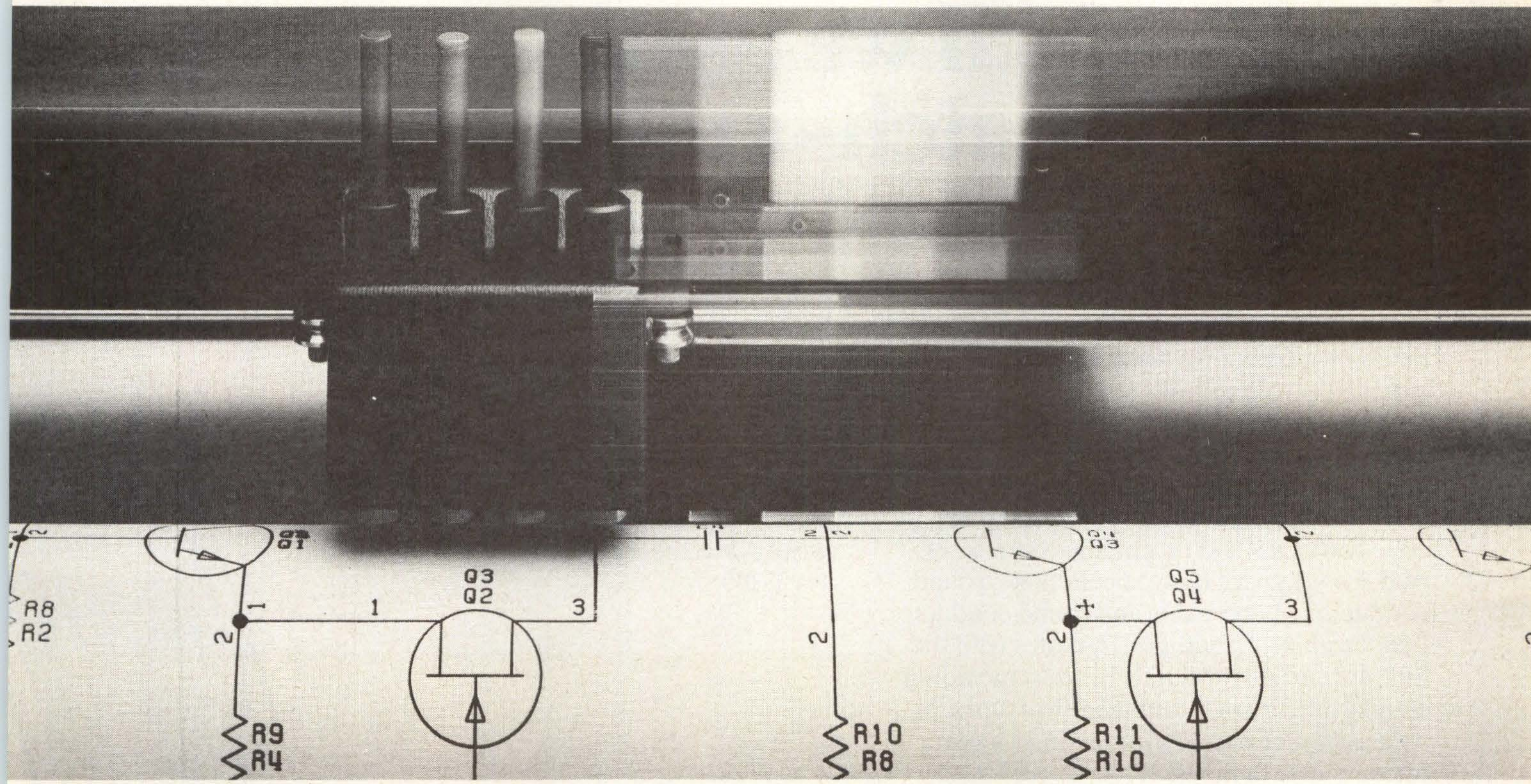
Circle 405 on Inquiry Card

Large-Scale Distributed Processing System Expands Capabilities

Providing users with the flexibility to configure computer network components to fit their organizations, the Level 66/distributed processing system (DPS) is a large-scale computer system with central processor configurations that expand to five performance levels. Honeywell Information Systems, 200 Smith St, Waltham, MA 02154 is aiming the system at heavy communications requirements where high system availability is needed; it is suited to distributed processing uses in the company's distributed systems environment.

(*Continued on p 38*)

How to drum-up superior graphics in record time.



There's nothing to it.

Not when you start with the best. And that's exactly what the new CalComp 1055 high-performance drum plotter is – the best. In fact, it easily surpasses everything we – and our competitors – have created to date.

There's simply no other 36-inch, roll-fed drum plotter with specs like these. Plotting speed is an unprecedented 30 inches-per-second (762 mm-per-second) on axis. Complemented by a 4G acceleration ramp and 10MS pen-down time. The results are unbeatable quality and throughput.

What's more, you get the versatility that only four pens can provide and a practical, roll-fed design that keeps operator intervention to a minimum.

But that's not all. For increased accuracy, we made the 1055 completely d.c. servo-motor driven. And we gave it a special linear pen drive mechanism to help maintain consistently superior line quality. In every application.

The bottom line is this: Our new Model 1055 creates an entirely new set of standards for all would-be, high-performance drum plotters. In terms of speed, accuracy and line quality. And in terms of good old-fashioned price/performance, too.

Of course, you may not need the sophistication of a 1055 right now. In that case, our new 1051 is the answer. You get 10-ips performance today, and the ability to field upgrade to a 1055 tomorrow – when your needs have expanded.

One thing hasn't changed, though.

CalComp service and support. It's still worldwide and second to none. For field service personnel. For in-place field systems analysts. And for the kind of help you expect from the world leader in digital plotters.

All of which proves, when it comes to high-performance drum plotters, CalComp's really drawing away from the competition. Again.

To arrange a special preview demonstration of the new 1055, please call your local CalComp sales representative in the following areas:

CALCOMP

2411 W. La Palma Avenue, Anaheim, California 92801

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CIRCLE 22 ON INQUIRY CARD

"All we got for our connector dollar were connectors.

Until we used AMP Latch-and AMP."

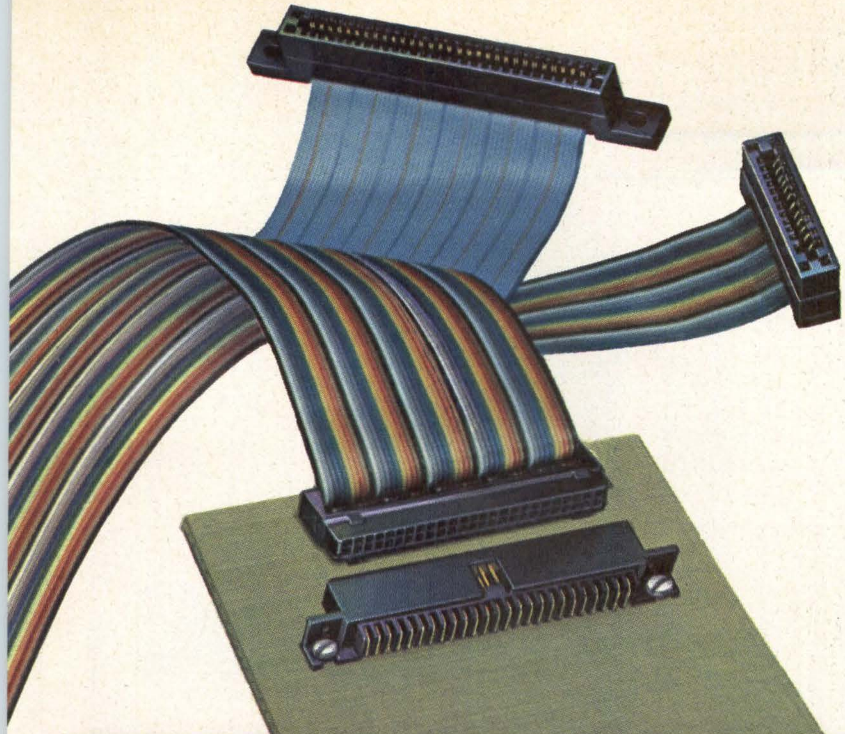
Too many times you may select a connector that does the job—but that's all it does. You can't expand with it. With AMP Latch connectors we make sure that won't happen.

The complete approach. Every AMP Latch connector is designed as part of a larger approach to packaging. For example, AMP Latch is available in cable-to-cable, edge card, DIP and receptacle connectors. And it works with twisted pair cable, round conductor ribbon cable and round conductor bonded cable. In addition, it mates with the full range of AMPMODU headers including standard right angle and feed-thru types, as well as header barriers for mixing a variety of connector families.

The quality approach. AMP Latch connectors are built to meet extra-ordinary requirements. They incorporate extra features such as redundant, duplex-plated contacts and heavy-duty strain relief covers for reliable electrical and mechanical performance. Polarization and positive latching assure accurate mating to headers. They have built-in inspection ports to facilitate inspection, test and repair. And they are quickly terminated by AMP Latch tooling so you have the capability of using virtually all popular types of round conductor flexible cable as efficiently as possible.

The AMP approach. Of course, AMP Latch connectors, and all AMP products, are backed by AMP technical service. Not just ordinary service, but the kind that says we'll help you with system design. Application tooling. Training your people. And more.

We invite you to find out more about AMP Latch and the AMP approach. Just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

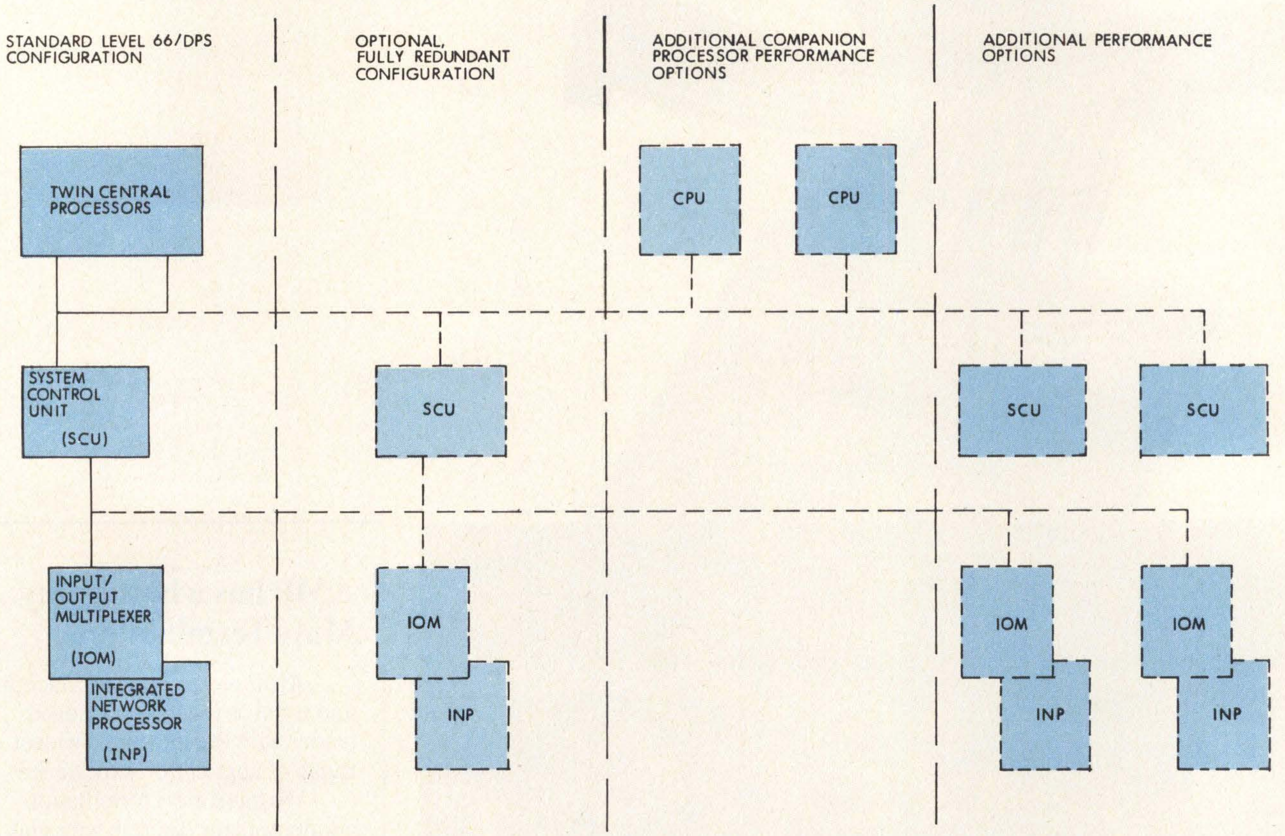


AMP has a better way... Mass Termination.

AMP pioneered the concept and today is the acknowledged leader with the industry's widest range of application experience.

We have mass termination connectors for discrete wire and virtually any type of cable: ribbon coaxial, flat etched, twisted pair, round conductor, flat flexible. All have preassembled contacts, eliminate costly wire preparation and offer productivity savings and benefits never before possible. If you would like details on any of our Mass Termination ideas, call Customer Service at (717) 564-0100.

AMP
INCORPORATED



Level 66/DPS gives increased performance and flexible central system configuration necessary for communications-intensive applications. Functional diagram of Honeywell's system indicates five levels of performance options which can be added to standard architecture

The first three levels will be available in October 1978; two higher performance levels will be available in January 1979. These optional additions expand performance up to 4½ times that of the base level, which is comparable to the current 66/60 system. Increases up to the third level are obtained with performance options added to the central system. Companion processors are available for levels four and five.

The base level system includes twin information processors in one cabinet, a single systems control unit, I/O multiplexer, and 1M bytes of 4k MOS memory. A single GCOS operating system controls both information processors. Also included is a 64k-byte minicomputer-based integrated network processor (INP) that accepts as many as 96 communication lines.

The system will function in its native mode using byte-oriented ASCII code; BCD data modes are optional. Main memory can be increased in 512k-byte increments to the 2M-byte level, and then in 1M-byte increments to a maximum of 8M bytes.

Separately priced software for the central system and communications processors includes General Remote Terminal Supervisor/II (GRTS/II), Network Processing Supervisor (NPS), a database-oriented FORTRAN, COBOL 74, and a new version of PL/1.

Circle 406 on Inquiry Card

Voice and Data Bridging Applications Are Served By Plug-In Circuits

The CB12 and 13 conference bridges each provide two independent 2-wire, 6-port, passive, resistive bridging circuits. Most common use is in 4-wire multipoint data communications networks in which master data set transmits only to remotes and remotes transmit only to the master; communication between remotes is not possible.

A single module from Rixon, Inc, 2120 Industrial Pkwy, Silver Springs, MD 20907 serves one master and up to five remotes. Tandem connections are used with larger networks. Fewer than five remotes require unused bridge ports to be terminated. Connections are brought to the card edge so that the mounting shelf can be wired to provide the terminating jumper if desired.

In addition, the CB13 features 12 front-panel jacks for access to each port of the dual bridge. Normal-through type jacks are wired to disconnect the line and to provide access to the bridge's port when a plug is inserted. □

Circle 407 on Inquiry Card

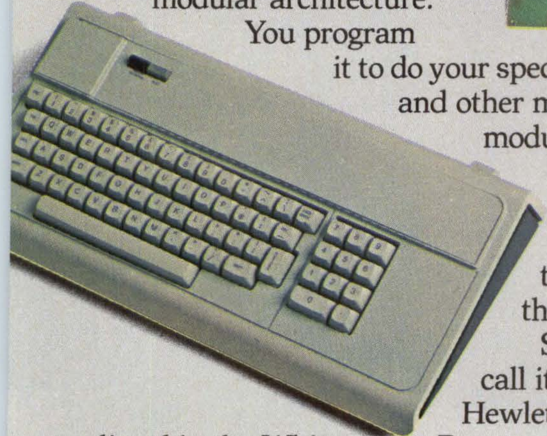
The HP 2649A is what *you* make it.

A controller. *It's a natural. Just program the built-in 8080 microprocessor to do your thing, and get it into your system. The HP 2649A has a variety of synchronous, asynchronous, serial and parallel interfaces (including HP-IB, our IEEE Interface Standard 488). This makes it easy to hook up with instruments and peripherals. In short, it's a complete controller system in a single package.*

A terminal. *Terrific! Great editing ability, a choice of keyboards, flexible data communications, and a variety of baud rates make it an excellent fit in an RJE situation. Preprogrammed firmware is available to get you off to a head start.*

A microcomputer. *Why not? The microprocessor gives you a lot of power. Then you can add ROM memory, interface with a disc, control peripherals, and access other systems via a modem. So the HP 2649A acts like a small computer, even if it doesn't look like one.*

A graphics display station. *Sure. You can put a window in your system and see exactly what's going on. Alphanumerics, auto-plot, and full graphics, including Area Shading, Pattern Definition and Rubber-band line, give you the whole picture.*



You can really make a lot with the HP 2649A.

You start with the basics — a CRT, power supply, backplane, I/O cards, MPU, and versatile, modular architecture.

You program it to do your specific job, and pick only the memory, keyboard, I/O, breadboard, and other modules you need. These include RAM (up to 32K bytes on one module), ROM, and PROM boards, which all simply slip into the chassis. (There are slots for your own boards as well.) You can also add 220K bytes of mass storage on dual plug-in cartridges.

To top it off, we have documentation, development tools, and a one week training course in programming and customizing the HP 2649A.

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HEWLETT hp PACKARD

CIRCLE 24 ON INQUIRY CARD

I'm interested in your microcomputer/controller/graphic display station/terminal.

- ☐ Have your representative contact me.
- ☐ Send me technical literature.
- ☐ Send me OEM information.

Name ______ Title ______

Company ______

Address ______

City/State/Zip ______

Mail to: Ed Hayes, Marketing Manager, Hewlett-Packard Data Terminals Division, 19400 Homestead Road, Dept. 1218, Cupertino CA 95014.

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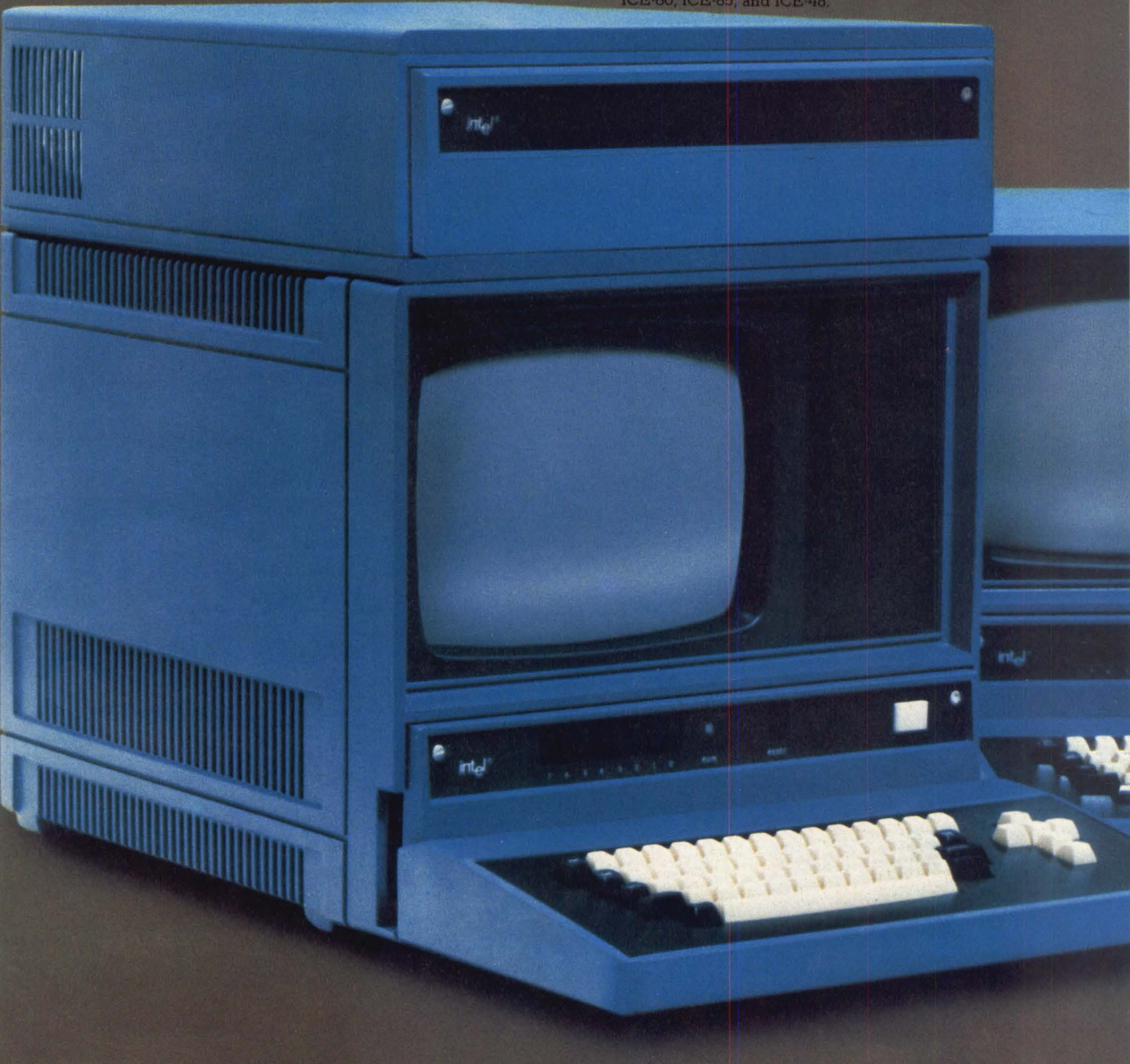

...NOW...

For medium-scale system development, you can rent the Model 220. Now.

The Intellec Model 220 is also a complete packaged development system. It has an interactive, 2,000 character CRT with typewriter-style keyboard and a full-sized 256K byte floppy diskette drive and 6-slot MULTIBUS card cage in one compact unit. Model 220 gives you 32K bytes of RAM program memory and 4K bytes of ROM. The ISIS-II Diskette Operating System has a relocating 8080/8085 assembler, and the new system interfaces directly to the ICE In-Circuit Emulators.

The Intellec Model 210 rents for the lowest price of any packaged, full support development system available—anywhere.

Model 210 gives you the minimum system required for the rapid, efficient development of microcomputer software. It has a ROM-based editor/assembler combination which allows the development of small 8080 or 8085 programs completely in RAM memory, which minimizes your use of paper tape. Plus, you can also rent a ROM assembler/editor for Intel's family of MCS-48 single-chip microcomputers. The compact Model 210 has 32K bytes of RAM, 24K bytes of ROM and its own microprocessor. Self-test diagnostics capability is built-in. And it's easy to get started, too. All you have to do is interface the Intellec 210 to your terminal.

You can extend the powerful resources of an Intellec Series II system into your own prototype for fast and efficient software debug in your product's final hardware environment. Just put your product on ICE . . . ICE-80, ICE-85, or ICE-48, all off-the-shelf at REI.

To emulate your own CPU or your entire prototype system in real-time or single-step mode, simply rent the appropriate In-Circuit Emulator module to match your system's microprocessor. And you can begin software debugging as soon as your prototype has a processor socket and bus structure.

Capability-enhancing peripherals are available for short-term rental, too.

You can add to the already extensive capabilities of the Intellec Series II system with a variety of immediately available peripherals. These include two Intellec Printers, two diskette-based peripherals (one single-density with ½-million bytes of storage, the other double-density with 1-million bytes of storage). You can also choose a high-speed paper tape reader and a universal PROM programmer . . . all of which are for rent today from REI.

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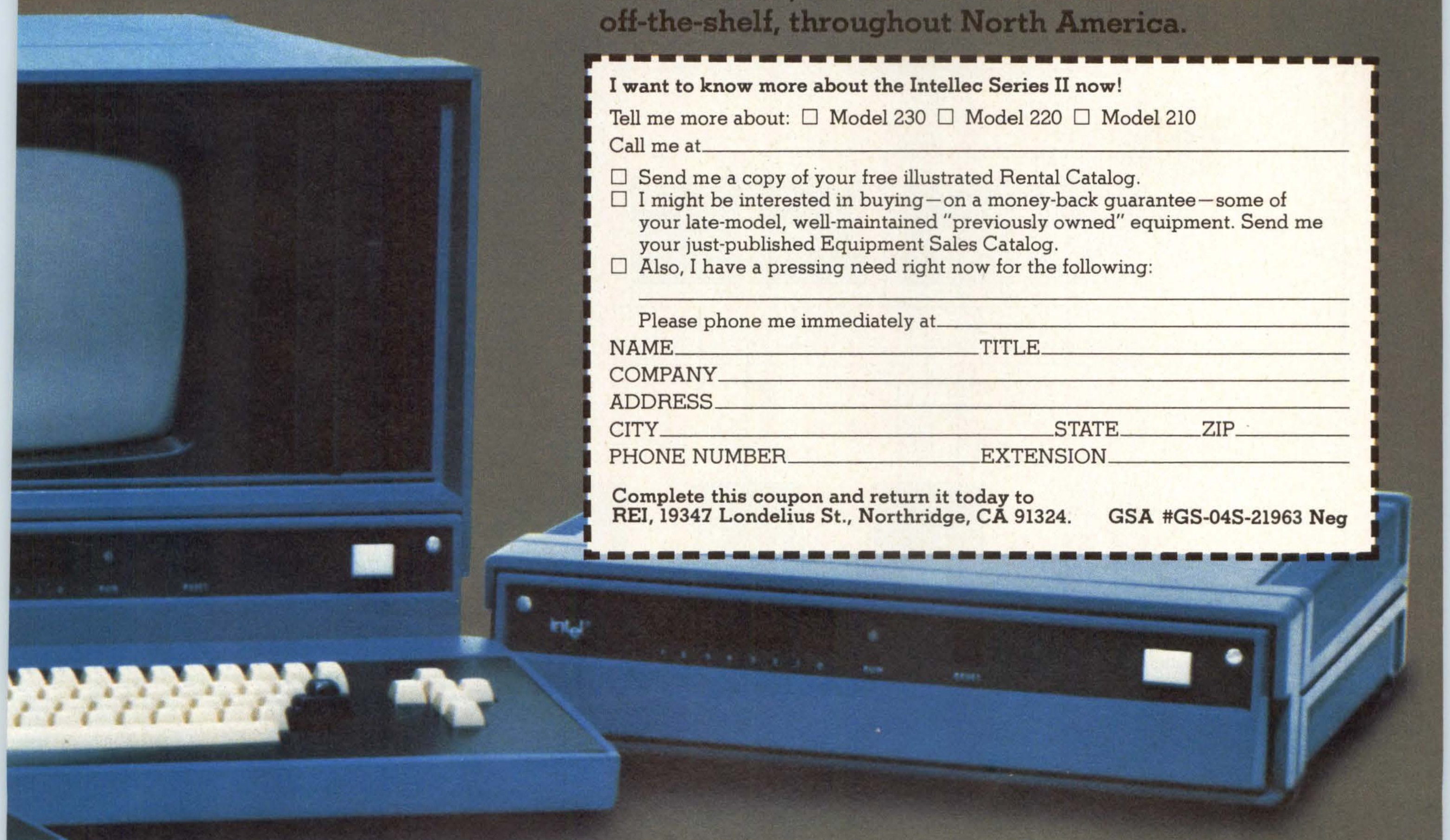

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CIRCLE 25 ON INQUIRY CARD

Multiword Architecture Tailors Computers to Realtime Environments

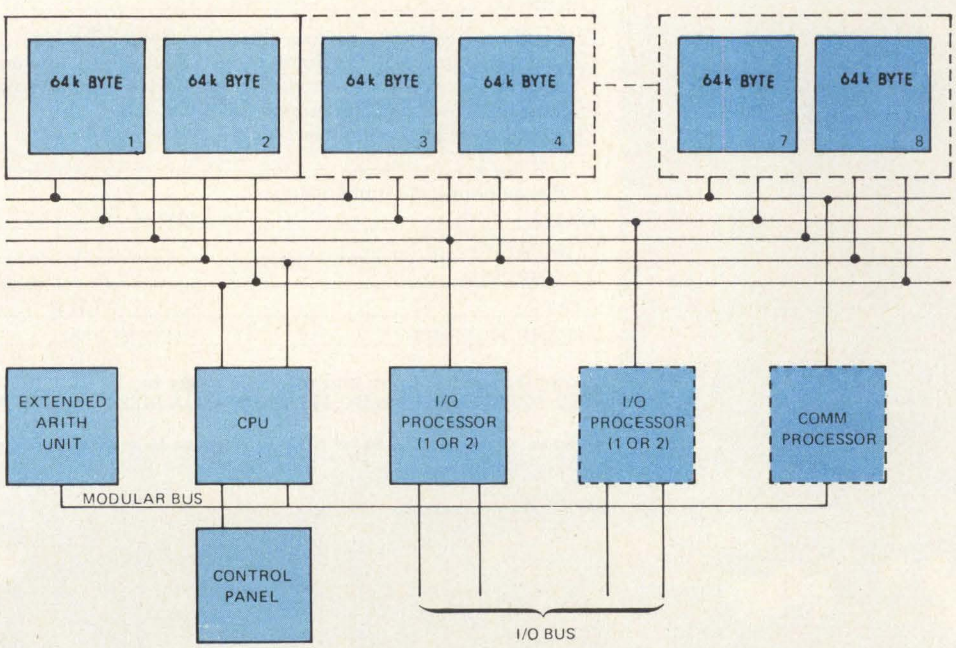
First of the Classic family to be introduced by Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33309, series 7860 computers provide superminiperformance at low cost. Multiword architecture is intended to provide efficient processing for formats ranging from single to 64 bits in real-time environments. Forthcoming members of the family will cover the rest of the range from low-end microprogrammable units to medium-scale minicomputers. All are program and I/O compatible with previous systems and use the MAX IV operating system.

To optimize the efficiency of this operating system, the processors include a context register file which contains 16 banks of general-purpose registers; each bank has 15 registers. This enables context switching within several resident tasks without having to save and restore register contents. In addition four address mapping files, expanded control instruction set, direct memory processor I/O channels, and fast interrupt response time reduce system overhead to a minimum. The processor can fetch up to four additional instructions while the current instruction is being executed, resulting in an effective instruction cycle time of 200 ns.

These processing capabilities are complemented by up to 512k bytes of local memory consisting of either core or solid-state error correcting MOS, or a combination of the two. All memory is either 2- or 4-way interleaved for effective cycle times as low as 150 ns. Memory addressing is handled by a memory management system that includes four 128k-byte virtual memory mapping files.

Five memory access paths provide concurrent CPU and I/O access capability. Two are utilized by the CPU: one for the instruction pipeline, the second for the operand pipeline. Remaining paths are used by the I/O processors, by the optional communications processor, or by external users. Each path has switch selectable priority, allowing the system to be optimized in certain applications.

Two forms of memory protection are implemented. In the memory management system, a 4-level protect code is assignable to each 512-byte page. In the extended memory addressing system, upper and lower boundaries are established and ac-



Functional block diagram of Modular Computer's Classic 7860 series computer shows relationship of options to major system elements. Five memory access paths allow I/O operations to proceed at high throughput rates, affecting CPU operations only when both attempt to access same memory module at same time

C.P. CLARE'S μP KEYBOARD WITH REEDS. THE BEST OF THEM ALL.

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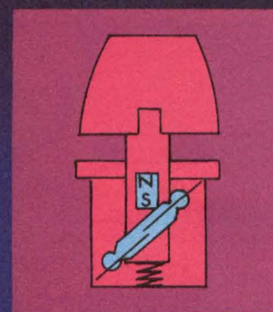
Couple this μP with the unique low-profile reed switches we manufacture and you've got the best of two technologies — an unbeatable keyboard system. You know reed contacts are sealed against hostile environments. You know reeds are extremely dependable and stable. They'll switch faultlessly over 10^8 times. They are low in power consumption. And zero in power drain. Another key point: they've got the feel operators like, so speed and accuracy increase.

Best keytops.
C. P. Clare's keytops are non-glare, 2-shot molded. The legends sharp and clear for life. The colors lab-quality, 3-dimensionally controlled. Yes. 3-dimensionally controlled.

Best advice.
C. P. Clare's μP keyboard is the best of them all. But is it best for you? Call the C. P. Clare sales office nearest you and arrange to talk to a keyboard expert. He'll tell you honestly if it is, or if you'd be better off with another C. P. Clare keyboard design. Talk to him today. Or, if you prefer, write C. P. Clare and Company, 3101 W. Pratt Avenue, Chicago, IL 60645. Or call 312-262-7700.

We help you compete

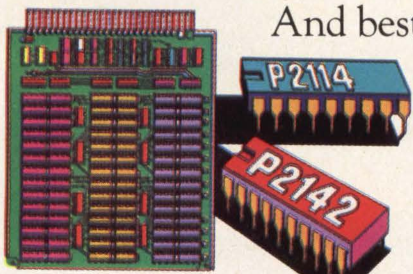


Height with keytop: 1 5/16"

C. P. CLARE & COMPANY
GENERAL INSTRUMENT CORPORATION

Intel delivers the
Make the move now

Now's the time to replace those 2102 1K designs with Intel's higher density 2114, the most widely sourced 4K static RAM. The 2114 is already less expensive at the board level than the 2102. You'll save power without compromising speed.



And best of all, we're delivering the 2114 in volume. We can ship up to 10,000 parts within one week of receipt of order.

There's a full range of design solutions in the 2114 family. It starts with our 1Kx4 2114, for the highest possible density and modularity in an 18-pin 4K static RAM. Then there's the 2114L. Same pin-out. Just as fast. But 30% lower power.

For simplified designs in microcomputer-based systems, we're delivering the 20-pin 2142. It's the way to go when you want 2114 performance, but need an extra chip select and output enable. The output enable function cuts parts requirements in microcomputer systems by eliminating bus contention.

All our 4K static RAMs inherit the ease of use and low overhead of our industry-standard 1K 2102. You don't need a clock, refresh or set-up timing. You don't even need

2114 in volume. to 4K static RAMs.

pullup resistors or output gating. Our 4K static RAMs operate at TTL levels on a single +5V supply, and have buffered three-state outputs.

We guarantee identical access and cycle times on these parts, so you can surpass the performance of clocked static RAMs. For example, you can achieve a data rate of 20 megabits per second with the 200 nanosecond 2114-2 or 2142-2 parts. That's twice the data rate of clocked RAMs with a 200 ns access time. Intel specs guarantee that even at high throughput rates you'll need less than half the power of first generation static RAMs.

You can take advantage of 2114 and 2142 economy and Intel's production availability by ordering directly from: Almac Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah or Zentronics.

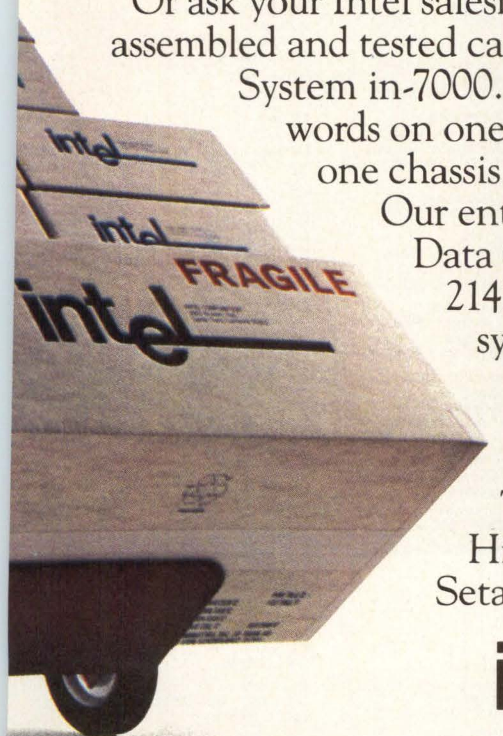
Or ask your Intel salesman how you can get an assembled and tested card, the Intel Memory System in-7000. It gives you up to 16K words on one card, up to 528K in one chassis.

Intel 1K x 4 MOS STATIC RAMs

	Access Time & Cycle Time (max) 0-70°C	Icc (max) @Vcc (max) 0-70°C
2114-2		100mA
2114L-2	**200ns**	70mA
2142-2		100mA
2142L-2		70mA
2114-3		100mA
2114L-3	**300ns**	70mA
2142-3		100mA
2142L-3		70mA
2114		100mA
2114L	**450ns**	70mA
2142		100mA
2142L		70mA

Our entire selection of static RAMs are in the Intel 1977 Data Catalog. For individual data sheets on the 2114 or 2142 components or the in-7000 static RAM memory system write: Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051.

In Europe: Intel International, Rue du Moulin a Pápier, 51-Boite 1, B-1160 Brussels, Belgium. Telex 24814. In Japan: Intel Japan K.K., Flower Hill-Shinmachi East Building 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.



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Circle 27 for information.

cesses outside them generate a protect violation.

The four 256-register map files in the memory management system enable several programs to remain mapped concurrently. Only the file belonging to the lowest priority program is switched when a program is loaded from disc. Noncontiguous page allocation enables memory to be allocated from a large pool rather than from partitions. Among the benefits which the memory mapping system offers are low hardware overhead and efficient memory utilization.

Basic element of the I/O system is the I/O processor which is made up of either a single plug-in board with one I/O bus or another plug-in board with two I/O buses. Basic I/O structure consists of a partyline bus capable of transferring words or characters between any 63 peripheral devices and any 15 general registers.

Standard on all models is an integral high speed floating point processor which performs operations on 32-, 48-, and 64-bit operands. This processor is contained on one of the CPU boards, resulting in fewer interfaces and signal paths for increased reliability.

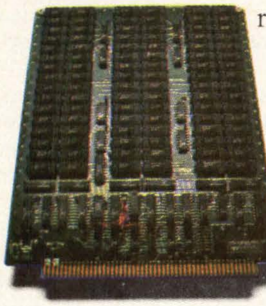
A plug-in option, the communications processor consists of a logic board which extends the hardware instruction set and provides an external multiplexed data path between main memory and the universal communications subsystem. The external multiplexed direct memory interface (DMI) is independent of the CPU and provides for memory mode transfers concurrently on up to 256 full-duplex communications lines.

Software available for use on the system includes the MAX IV real-time multiprogramming operating system with several compatible high level languages including FORTRAN IV compiler (FR5), COBOL, and TOTAL. In Europe, CORAL 66 and RPG2 are also offered. The operating system supports all standard company-supplied peripherals as well as communications controllers and process I/O subsystems. An extension to MAX IV, the MAXNET network operating system allows multiple computers to be linked into distributed network configurations. A library of system processors and utilities are provided for support of software development; remote job entry emulators for large mainframes are also available.

Representative prices are $37k for a model 7861, which includes 128k

Intel's new in-7000 static memory system with Word/Byte Control delivers speed, convenience and design flexibility. It's the easiest way to get our high-density 2114 4K static RAMs into your system.

The in-7000 is a complete static memory with interface and control logic contained on a single 10.8" x 8.175" printed circuit card. The system requires only a +5V power supply, is TTL compatible, and needs no refresh. You can choose from two versions, differing only in speed: the 7000, with a read and write cycle time of 250 ns; and the 7001 (350 ns).



The basic in-7000 card is available in four 16K configurations: 16K x 12, 16, 20 or 24 bits. Two chassis models are also available. The in-Minichassis can house six in-7000 circuit cards, and the in-Unichassis has a 32-card capacity.

A unique feature called Word/Byte Control gives you the design flexibility to standardize on the in-7000 for all your systems applications. Word/Byte Control allows the Byte Control inputs to be used either for reconfiguration or byte data control. In the Word mode, the Byte Control inputs select either or both halves of a word, effectively reconfiguring a 16K x 24 card to 32K x 12; a 16K x 16 card to 32K x 8; and so on. In the Byte mode, any combination of three bytes in a 24-bit word may be selected by the Byte Control inputs.

Get Intel 4K static RAMs into your system now with our in-7000. Phone your local Intel sales office or use the coupon below.

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Phone (408) 734-8102

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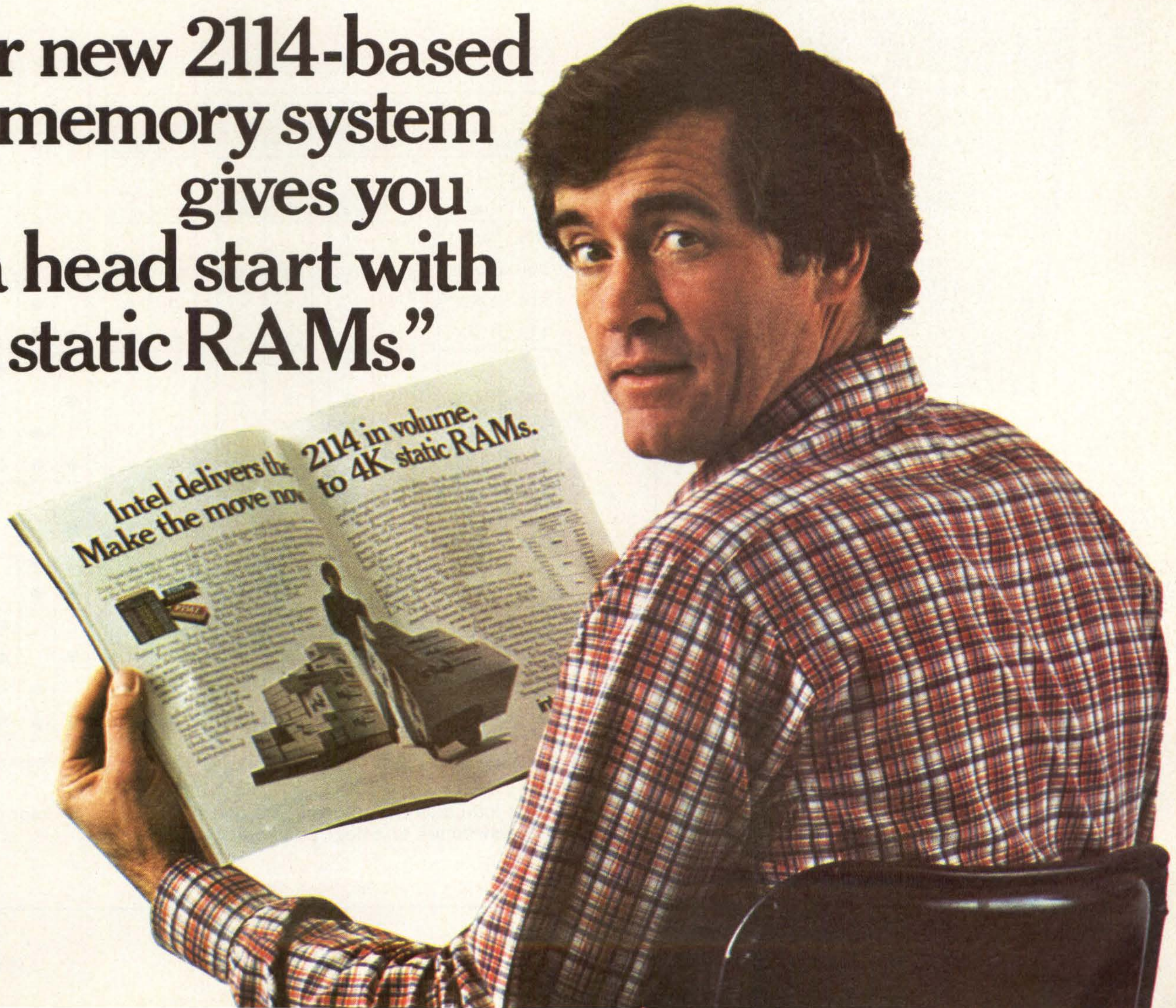


bytes of solid-state memory and one I/O processor, and $42k for the 7860 which has 128k bytes of core memory and one I/O processor. Models 7863 and 7862 differ from these units only in that they provide a second I/O processor. Also offered are six packaged systems ranging in price from $58,700 to $124,430. These packages include various CPU models with console controller, disc controller, and operating system, along with various memory sizes and I/O processor configurations.

Circle 170 on Inquiry Card

Typing Keyboard Provides 128 ASCII Characters Using One Hand

Small, light, and portable, the Writehander™ permits users to type all 128 ASCII characters with one hand, while holding a telephone or papers with the other. It can also be used by those with an injured or disabled hand, which makes conventional typing impractical.

The unit's hemispherical shape conveniently accommodates the human hand, with fingers naturally locating themselves on the switches. Logic arrangement and physical convenience simplify learning how to use the keyboard.

To use the keyboard, four fingers of one hand are placed on four press-switches and the thumb is located on one of eight press-switches. The four finger switches operate as the lower four bits of the 7-bit ASCII code, selecting the group of characters (out of 16 groups) that contains the desired character. The thumb is then used to select one of the eight characters in the group by pressing a particular switch (see chart for code).

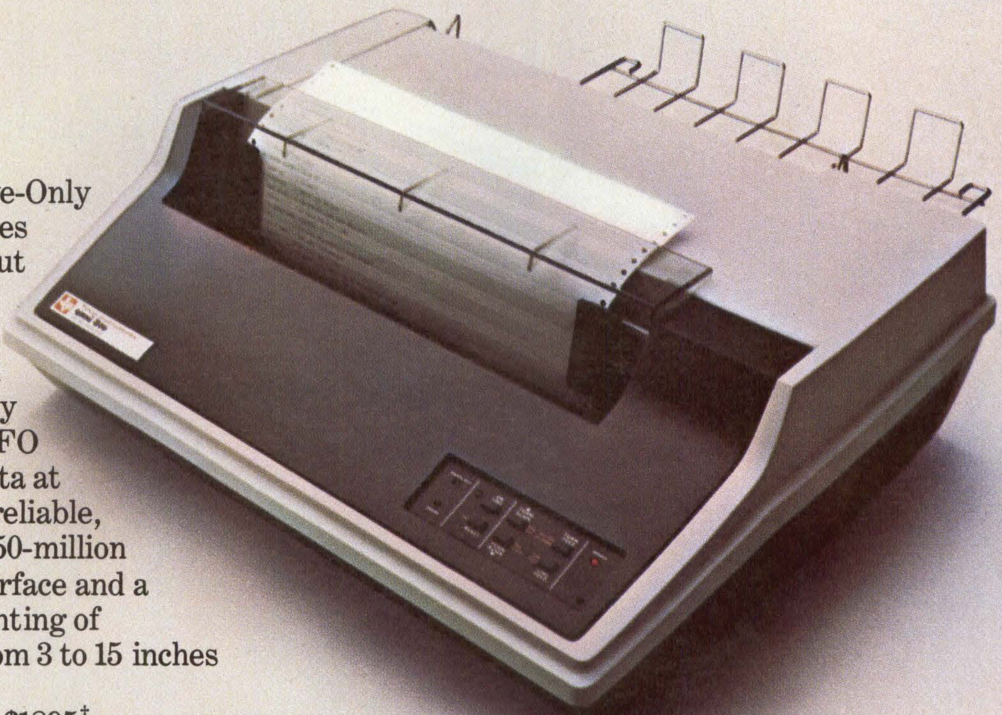
THUMB SWITCHES (COLUMN SELECTED BY PRESSING SWITCH) WHITE		GRAY		RED		BLUE					
FAR	NEAR	FAR	NEAR	FAR	NEAR	FAR	NEAR	INDEX	MIDDLE	RING	LITTLE
NUL	DLE	Ø	SP	`	p	@	P				
SOH	DC1	1	!	a	q	A	Q	●			
STX	DC2	2	"	b	r	B	R		●		
ETX	DC3	3	#	c	s	C	S	●	●		
EOT	DC4	4	$	d	t	D	T			●	
ENQ	NAK	5	%	e	u	E	U	●		●	
ACK	SYN	6	&	f	v	F	V		●	●	
BEL	ETB	7	'	g	w	G	W	●	●	●	
BS	CAN	8	(	h	x	H	X				●
HT	EM	9	)	i	y	I	Y	●			●
LF	SUB	:	*	j	z	J	Z		●		●
VT	ESC	;	+	k	{	K	[	●	●		●
FF	FS	<	,	l	¦	L	\			●	●
CR	GS	=	-	m	}	M	]	●		●	●
SO	RS	>	.	n	~	N	Λ		●	●	●
SI	US	?	/	o	DEL	O	_	●	●	●	●

● DENOTES PRESSED KEY

Chart indicates how four fingers and thumb operate color-coded press-switches to select character on keyboard

(Continued on p 52)

TI's Model 810 Printer can make a big impact on your printer costs.



OMNI 800* Model 810 Receive-Only Printer has standard features designed for high throughput and reliability.

Features like bi-directional 150-cps printing of an original and five high-quality copies. A 256-character FIFO buffer so you can receive data at speeds up to 9600 baud. A reliable, low-cost printhead with a 150-million character life. An EIA interface and a self-test capability. Plus printing of reports, tickets or forms from 3 to 15 inches in width.

These and more … for $1895.†

For added flexibility, there are options such as vertical forms control with compressed print, expanded print, international character sets, a tear bar and five different interfaces.

Add it all up and you can see why the 810 is the price/performance leader. For more information about how the 810 can impact your printer costs, fill out and mail the coupon. Or call your nearest TI sales office, or Terminal Marketing at (713) 491-5115, ext. 2124.

Yes! I am interested in the Model 810 Printer.

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electronic data terminals

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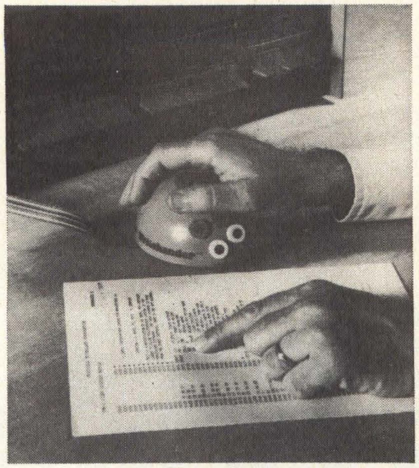

Directly operating a terminal, the Writehander, a portable keyboard, requires only one hand to generate full 128 ASCII character set

The device connects to terminal or computer through a ribbon cable that has lines for the 7-bit ASCII code, a 1-bit fixed parity, strobe and acknowledge signals, and power and common lines. Terminals such as the Diablo HyType and Teletype ASCII-modified Selectric, or a video monitor can be operated directly. Power is obtained from the terminal. Required power is 200 mA from 5-Vdc regulated.

Two versions of the unit with different switch spacings to accommodate large and small hands are available from NewO Co, 246 Walter Hays Dr, Palo Alto, CA 94303. Price is $98.

Circle 171 on Inquiry Card

Four Models Extend Minicomputers' Power and Flexibility

Models 33, 43, 47, and 53 serve to extend both power and flexibility of the Level 6 minicomputer family. Introduced by Honeywell Information Systems, 200 Smith St, Waltham, MA 02154, along with higher density semiconductor memories, reduced prices on current memories, and added large capacity peripherals and communications capabilities, the systems provide modular growth to more powerful models through the simple change of central processor board or addition of performance modules.

Model 33, with main memory ranging from 16k to 128k bytes, supports the full range of family peripherals and communications capabilities. The system can run several online tasks concurrently with batch processing and program development. It may serve as a freestanding system or in a distributed network.

With 1.6 times the speed of the 33, the 43 accommodates up to 2M bytes of directly addressable main memory. An optional scientific instruction processor enables the unit to perform FORTRAN-based scientific programs up to 10 times faster. Memory segmentation and Multics-like storage protection with separate read, write, and execute rings are offered with an optional memory management unit. Applications include use as a freestanding processor with a network of online terminals doing transaction processing, data-base management, and timesharing.

Twice as fast as the 33, the model 53 includes a new central processor board and 4k words of cache memory. Typically it will be used where faster processing of a general mix of standalone or data entry, remote batch, or timesharing programs are encountered.

Model 47 is a commercial minicomputer that processes COBOL programs seven times faster than the model 33. It takes full advantage of multifunctional software capabilities for standalone or network systems.

All systems provide throughput at up to 6M bytes/s on the bidirectional asynchronous Megabus communications path. Cycle time with both 4k and 16k MOS memories is 550 ns.

High level languages include entry level and intermediate COBOL, RPG, and entry level and advanced FORTRAN. The variety of compatible modules available in the GCOS operating system enables configuration of software support ranging from entry level systems to sophisticated multifunctional commercial systems.

Four communications pacs provide higher transmission speeds and support distributed systems environments with HDLC capabilities. Included are broadband pacs for HDLC Bell 301/303 and CCITT/V.35 that operate at speeds to 72k bytes/s and an HDLC MIL-188C interface for speeds to 19.2k bytes/s.

Connecting two or more minicomputers to form powerful multiprocessor or redundant systems, an optional intersystem link (ISL) transfers commands, interrupts, and memory accesses from any unit on another identical path. A device address table in the ISL determines which commands should be transferred through to devices on the link. Two duplicated sets of all registers allow for simultaneous bidirectional operation. When one element is accessing memory on a linked bus, a memory map in the ISL provides both protection and address translation.

A writable control store option is an extension to the central processor's microprogram space that allows a user to define his own instructions or implement time-critical algorithms directly in high speed machine level firmware. This feature is invoked by special operation codes and provides software up to 16 unique entry points. A microinstruction assembler and optional plug-in microcode analyzer support users who want to write their own firmware routines.

Circle 172 on Inquiry Card

32-Bit Business Computer Systems Fill Transaction Processing Needs

Business systems introduced by Perkin-Elmer's Interdata Div, 2 Crescent Pl, Oceanport, NJ 07757 provide the key to successful transaction processing. Integrating existing 32-bit hardware and transaction processing software, 700 and 800 Business Systems are designed to match system size to job size.

A basic 700 system includes model 7/32 processor with 256k bytes of memory, four editing CRTS, one 80M-byte disc drive, one 45-in/s magnetic tape drive, and a printing console terminal. The system expands to 512k bytes of memory with 16 CRTS, two disc drives, and two tape drives. Optional are one communication line, two card readers, and two 300- to 600-line/min printers.

Based on the 8/32 processor with 256k bytes of memory, the 800 system consists of four editing CRTS, one 80M-byte disc drive, one 1600/800-char/in, 75-in/s magnetic tape drive, and a printing console terminal. This system expands to 1M bytes of memory with up to 32 CRTS, as many as eight 80M- or 300M-byte disc drives, and up to six tape drives. Options include a communication line, two card readers, and four 300- to 600-line/min printers.

Transaction processing software for the 32-bit machines includes the Dy-

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CIRCLE 35 ON INQUIRY CARD

namic OS/32 MT operating system which supports a multiprogramming environment with up to 255 user tasks. Multi-Terminal Monitor provides a time-sliced interactive programming environment for up to 16 concurrent terminal users, making full program development facilities of the operating system available to each user, and supporting 16 concurrent background batch jobs. COBOL is packaged with the ISAM enhanced file management system. ISAM utilities provide capability for allocation and dedication of up to 32 contiguous files on each of 32 different disc volumes.

The transaction controller features complete compatibility with COBOL, interactive screen formatting, and online screen form-testing capability. A transparent control module is provided for interfacing with ITAM, which initiates automatic error recovery routines, provides automatic message queuing for busy periods, and schedules incoming messages on a priority basis.

Circle 173 on Inquiry Card

Distributed Processing System Expands Multitask Capabilities

Hardware and software enhancements to the XL40 distributed processing system broaden user capabilities in interactive communications and transaction processing. Among the added features are 3270 mode, station printers, remote subsystem, 2000-char video display terminals, increased disc capacity, and an expanded fast random-access memory.

To extend the existing COSAM (COBOL shared access method) information retrieval package, Pertec Computer Corp's CMC Div, 12910 Culver Blvd, Los Angeles, CA 90066 has provided 3270 mode compatibility. This feature allows requests for information not resident in the local data base to be automatically passed to the host computer, completely transparent to the operator. As a result operators can dynamically interrogate either local disc files or a remote central data base with no change of procedure.

Station printers rated at 60 to 120 char/s can be logically associated with specific terminals through dynamic assignment and are designed to be located separately from the terminals. In addition to terminal display hardcopy, the printers will provide hardcopy for keyed data under program control, which is combined with previously stored disc file information. In this case, they produce, interactively with keyboard transactions, formatted reports or complete printing of multicopy preprinted forms.

Using remote subsystem capability, all system terminals and station printers can be connected to dial-up or leased telephone lines. Users may cluster terminals and printers where transaction volume is high or locate them separately where volume is limited although essential to timely operations.

The system's flexibility in multitasking applications is augmented with 2000-char video display terminals. The top two 80-char display lines are reserved for status data and operator guidance; yet a full page of 1840 characters is retained for application information.

Disc capacity is increased to 70M bytes. Up to four 17.6M-byte disc drives can be attached to the system, providing storage for large scale indexed files. Expansion of addressable memory from 128k to 512k bytes increases the system's applications flexibility in multiterminal, multitasking environments.

Circle 174 on Inquiry Card

Low Cost Tape and Disc Units For Distributed Systems

A 10M-byte disc drive and a tabletop tape drive extend storage capacities of Series 21 distributed data processing systems while maintaining their simplicity. Introduced by Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054, model 2174 quadruples disc storage capacity of the System 21/40, while models 2181 and 2182, 25-in/s tape drives, provide 800- and 1600-bit/in density, respectively.

In addition to capacity, the fixed disc drive offers high reliability and easy maintenance. Average access time is 87 ms, and transfer occurs at 889k bytes/s.

The 12.12 x 19 x 30" (30.18 x 48 x 76 cm) tabletop tape drive is a 9-track unit that can be used on System 21/40, fully programmable in MOBOL; or on System 21/20, preprogrammed for data entry/validation under user-specified formats.

Circle 175 on Inquiry Card

Computer System Fills Needs of Insurance/Leasing Firms

Made up of microprocessor, floppy discs, and keyboard/display monitor, the CADOSystem 40 is a general-purpose computer system designed to offer security and ease of use. Business application processing is provided by Cado Systems Corp, 2730 Monterey St, Torrance, CA 90503 with preprogrammed ready-to-implement software packages.

System processor has a basic instruction time of 2.5 μs. Memory consists of ROM and RAM. Two double-density flexible disc drives offer storage capacity for 1.23M bytes of data. Four additional drives may be attached to give total capacity of 3.70M bytes.

Keyboard/display monitor is a Bell System Teletype model 40 which provides high resolution display of 72 lines of 80 characters each, typewriter style keyboard with 10-key numeric pad, and 300-line/min 80- or 132-col printer. Communication is provided through an EIA RS-232 interface at synchronous or asynchronous speeds from 110 to 9600 baud.

Implemented on the system are an accounting and management system for insurance agencies and fleet management system for automotive leasing firms. These systems offer complete automatic data processing, providing billing and timely financial data. Software supporting these applications includes a comprehensive operating system, the CADOL Basic programming language, and a full range of system utilities for batch and communication processing.

Circle 176 on Inquiry Card

Data Acquisition System?

It happens constantly. You buy a DAS, install it and then spend a lot of time, energy and money de-bugging the hardware, creating some specialized software, burdening the host computer and finding that you bought a 12-bit A/D system that doesn't stay a 12-bit A/D system very long.

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We're an ultra engineering-oriented company with a strong commitment to product reliability, integral accuracy, stability over time and temperature and innovative solutions to customer problems. And we know, that to really solve your problem it takes more than block diagrams. It takes experience; it takes what you might call a "green-thumb" in data acquisition systems.

Superior Data Acquisition Systems must provide solutions to customer problems, measurement techniques and specific microcomputer requirements and purposes. And that is what Analogic does, provides solutions qualitatively and innovatively over a broad line of products. Maybe that's why Analogic is, by far, the world's largest designer and manufacturer of microcomputer Data Acquisition Systems.

A call to our Data Acquisition Technical Support Team is the shortest route to years of accumulated experience and solutions to any of your data acquisition problems.

Another Innovation from Analogic – A DAS for the TI TM990/100M Microcomputer with "Program-Transparent I/O"

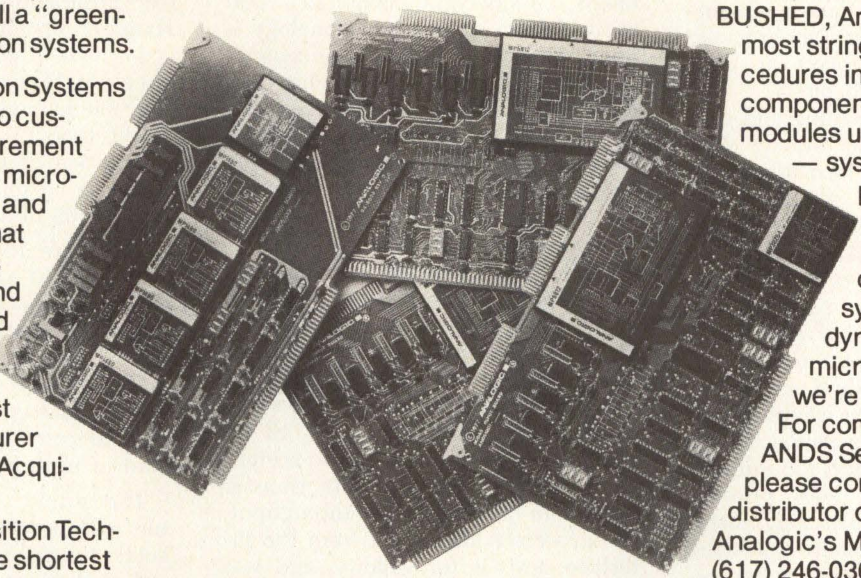
Our ANDS Series of 12-bit input/output DAS boards was specifically designed for the Texas Instruments TM990/100M. Whether you must accommodate either hi-level or low-level signals, you will find this DAS clearly accommodates and enhances the unique capabilities of the TM990/100M.

Analogic's innovative "PROGRAM-TRANSPARENT I/O" allows the user, in one instruction to (a) initiate the conversion (b) collect the data (c) operate on that data and (d) store the resultant data. To you, the user, this adds up to sharply reduced software costs and rapid system implementation.

In addition, our low-level DAS provides for Thermocouple Cold Junction Compensation and direct Linearization, thereby unburdening the host computer from the overhead and program code required to perform such linearization.

... AND TO AVOID BEING AMBUSHED, Analogic exercises the most stringent quality control procedures in the industry. All components are 100% inspected — modules undergo extensive testing — systems are burnt-in and power cycled for 48 hours in a special environmental chamber — and all systems undergo final dynamic tests in a TI microcomputer. All this, and we're competitive, too.

For complete data on our ANDS Series of I/O boards please contact your closest distributor or call or write Analogic's Marketing Department (617) 246-0300. Analogic Corporation, Audubon Road, Wakefield, Massachusetts 01880.



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CIRCLE 38 ON INQUIRY CARD

Word Processing System Allows 24 Operators to Share Central Data Base

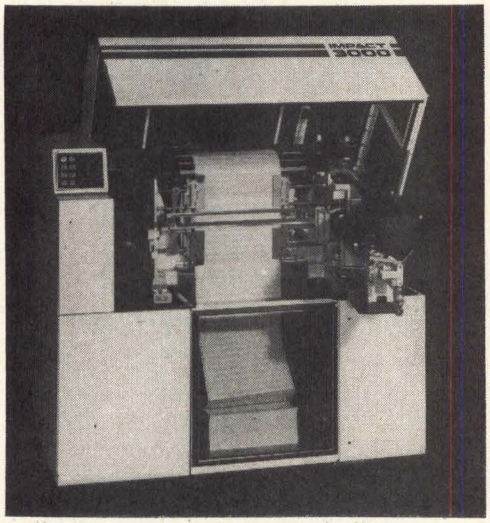
Wordplex 7, a shared logic word processing system, allows up to 24 operators to perform word processing and text editing functions, sharing a single central data base. Designed around a minicomputer with up to 128k words of main memory, the system from Dennison Office Systems, 300 Howard St, Framingham, MA 01701, can handle up to four 40M-byte or four 80M-byte disc drives, and up to 24 word stations.

Word station terminals have a 24-line CRT display with a 44-key standard typewriter keyboard. Output printers operate bidirectionally at 45 or 55 char/s. The daisywheel printers accept paper up to 15" (38 cm) wide and provide a 13.2" (33.5 cm) wide line. Also available for attachment are OCR input devices and data communications in asynchronous, synchronous, or bisynchronous protocols at data rates from 150 to 9600 bits/s.

In addition to text editing and disc operating software, the system supports Management Information System (MIS) software which allows managers to monitor the productivity of individual terminal operators as well as the costs of word processing operations. Software automatically measures total amount of productive keyboard time and total number of keystrokes entered by each of as many as 12 operators. It then compiles and prints out selected information by operator. This data may include minutes worked, keystrokes, lines printed, pages printed, and type of assignment. In addition to productivity statistics, the system provides security by requiring that operators sign on and off using a password.

Circle 177 on Inquiry Card

3000-Line/Min Printer Achieved By Combining Technological Advances



Printing at 3000 lines/min, Documation's model 3000 incorporates microprocessor controller that communicates with host system, decodes commands, controls print mechanism and reports errors and status. Lightweight hammer material and precision machining also contribute to increased speed

An impact line printer that operates at speeds of 3000 lines/min, the Impact 3000 is claimed by Documentation Inc, PO Box 1240, Melbourne, FL to be 50% faster than comparable units. The machine's design results from advances in materials, manufacturing techniques, and electronics—a tough lightweight material that evolved from space age technology is used in the print hammers, numerically controlled machining centers produce the precision mechanical parts, and a microprocessor serves as the integrated printer controller.

Speed is achieved in part through the integrated microprocessor controller, which is optimized for a 50-ns cycle time, resulting in an average instruction time of 350 ns. Provision of separate program and data memory address space allows the processor fetch cycle to occur during the execute cycle. An additional speed advantage is obtained by using all 32 processor registers as a classic accumulator. To prevent the data transfer rate from affecting the throughput, the processor loads data from the interface, tests it for validity, and sets up the hammer fire buffers before printing each line. A channel throughput rate of 70k bytes/s requires less than 5 ms for line loading and associated housekeeping.

Another contributor to speed is the special hammer material—50% lighter than steel—which reduces impact times to less than 17 μs. Added benefits of lower mass hammers and reduced contact time on the band are the resultant decrease in character smear, improved print quality, and increased band and ribbon life.

The unit is a backside printer, with hammers mounted behind the paper; the ribbon separates paper and printband. Printing is accomplished when a hammer strikes the paper from behind and forces it into contact with the printband through the ribbon. Hammer fire mechanism includes a coil which, when energized, forces an armature to move a pushrod which hits the hammer driving it forward. Flight time (1.360 ms) is critical as a variation of 0.18 ms will result in character displacement of approximately 10% of a character width.

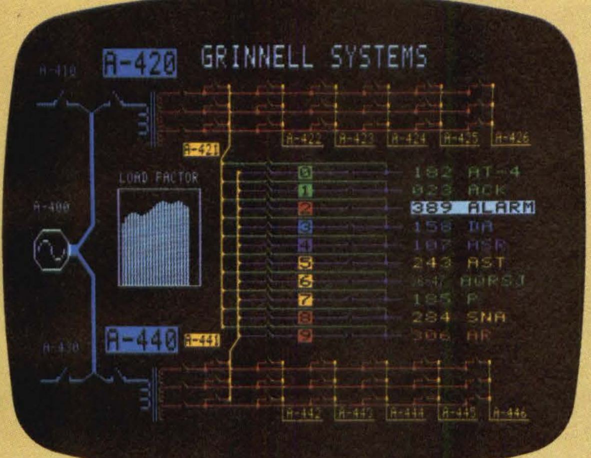
There are 150 hammers spaced on 0.100" (2.54-mm) centers, one per print position. The print band contains 432 characters, several repetitions of one array, and moves at 489 in (12.42 m)/s. Print time for one line is equal to the time necessary for all characters in an array to pass in front of each hammer—13.36 ms.

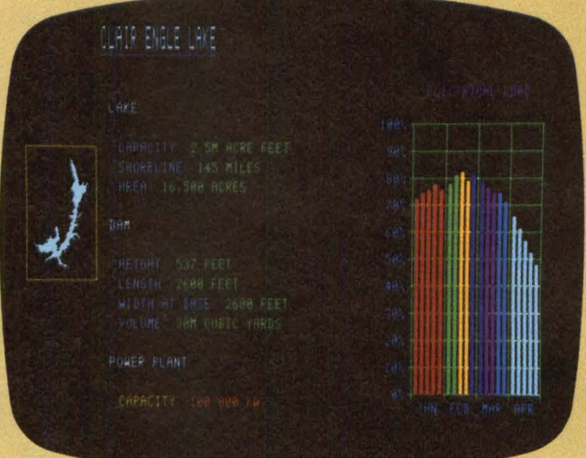
The printer produces 3000 lines/min with a 48-char set, at 6 lines/in. Total throughput rate is enhanced with a slew rate of 35 in (0.89 m)/s for skips up to seven lines; beyond seven lines, the rate increases to 100 in (2.54 m)/s.

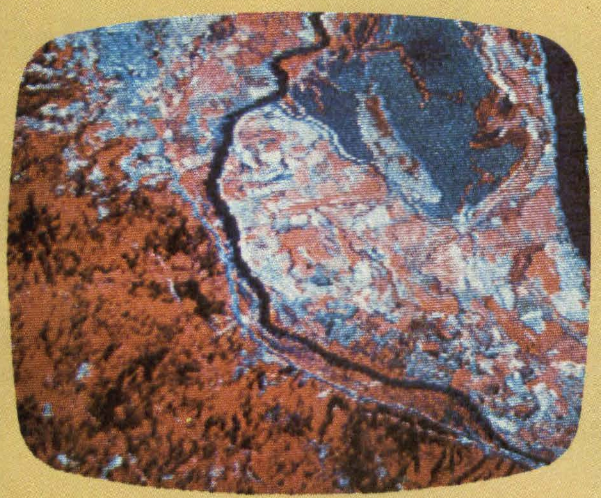
Convenience features incorporated in the unit include a power-operated hood that can be operated manually, and operator-adjustable power stacker for multipart forms, and operator controlled print density and character phasing adjustments. The interchangeable printband coupled with the universal character set buffer allow character sets and print styles to be changes in less than 2 min. Available fonts include PLI, commercial, scientific, ASCII, and text fonts. □

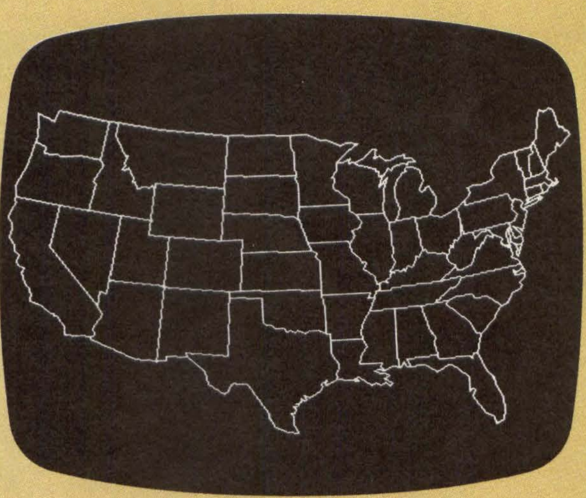
Circle 178 on Inquiry Card

GRINNELL DISPLAYS:









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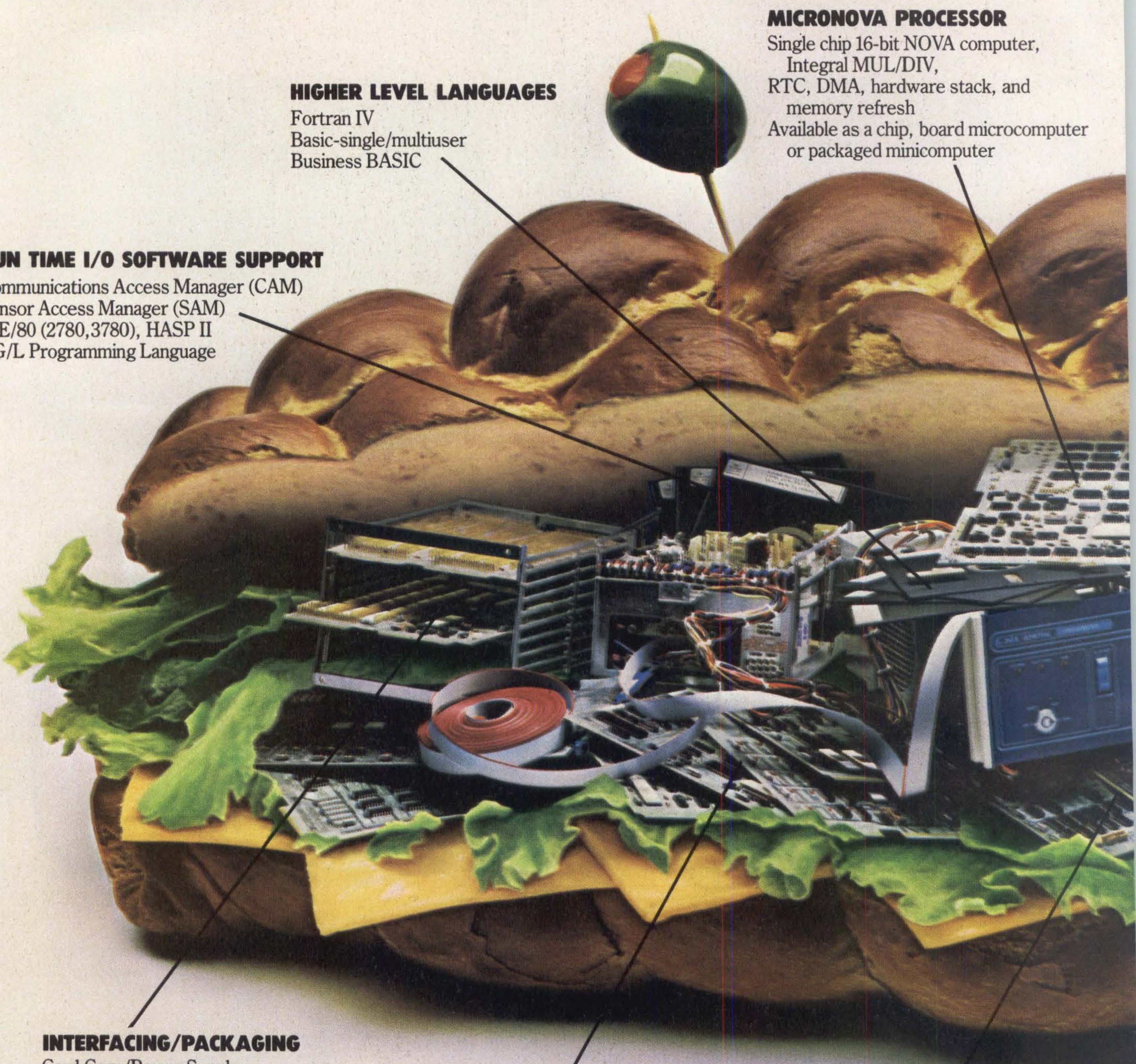

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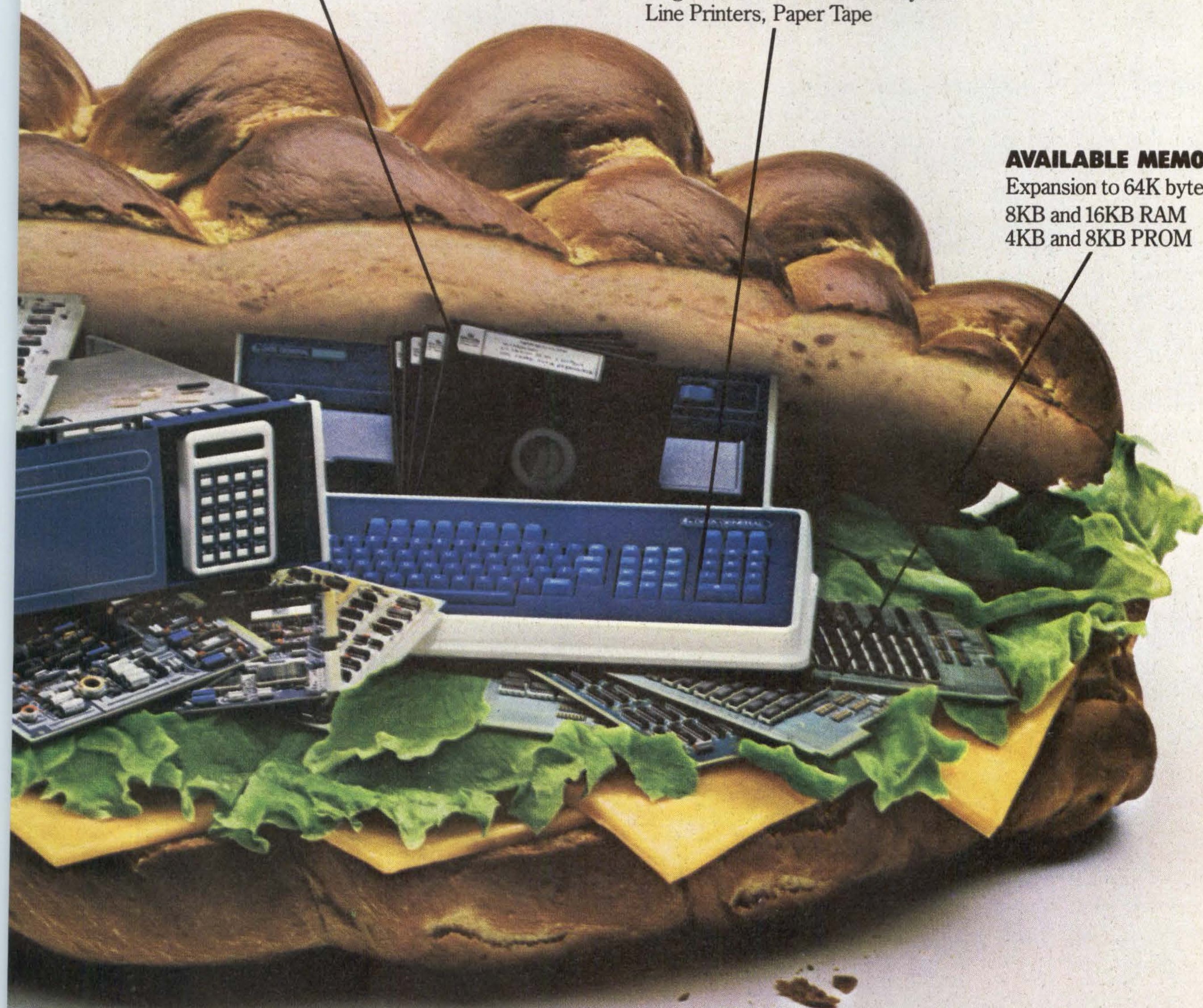

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CIRCLE 39 ON INQUIRY CARD

Microcomputer Controls Eye's Focus and Measures Refractive Error

To persons not closely associated with health fields, it would appear that of all applications where the capabilities of a digital computer might be of greatest help, medical diagnosis seems to have been least accepted. Certainly that may be a false impression. Digital computers perform many duties in medical laboratories and in hospitals, but that is not evident to persons not directly associated with such facilities.

Assuming that digital computers can be used in the diagnosis of medical ailments, the reason that they apparently are not in evidence may be two-fold. Full responsibility cannot be placed on any reticence on the part of the medical profession. The inherent fear held by some persons that computers are "dangerous" devices that are merely waiting to take control of the world must be considered—and also many otherwise fully knowledgeable people lack confidence in anything but the personal concern of the doctor when their own health situations are involved.

An example of a successful bypassing of all reticence to the use of a digital computer in at least one type of medical diagnosis is the Dioptron[R]. That device is a fully automatic computerized instrument for measuring the objective refraction of the eye. Complete control of the instrument, other than adjustments made by an operator to align it for each eye, is maintained by a microcomputer.

However, the patient need not necessarily know that a computer is involved. Even more important, the instrument basically serves only as an aid for the eye care practitioner. He can depend on it as much or as little as he wishes. In any event he will personally check the specified corrective lenses on the patient before writing a final prescription.

General Functions

The optical system of a normal eye focuses directly on the retina at the back of the eye. If the focus occurs either in front of or in back of the retina, as would be the case for an abnormal eye, correction is required in order to recover normal vision.

Most past attempts to measure the refractive state of the eye automatically were based on servosystems. Error signals caused the servosystems to drive lenses to positions that set up a balanced state.

Initially, such systems were designed to track a subject's accommodation (focus of the eye from a distant object to a near point) as various stimuli were presented. Normally tests had to be repeated several times in order to obtain useful readings.

The Dioptron automatic objective refractor controls accommodation first, then records data to determine each eye's refractive error. Coherent, Inc, Medical Div, 3210 Porter Dr, Palo Alto, CA 94304 claims that this automatic refractor is the only one to utilize the retinal image formation technique of auto-refraction.

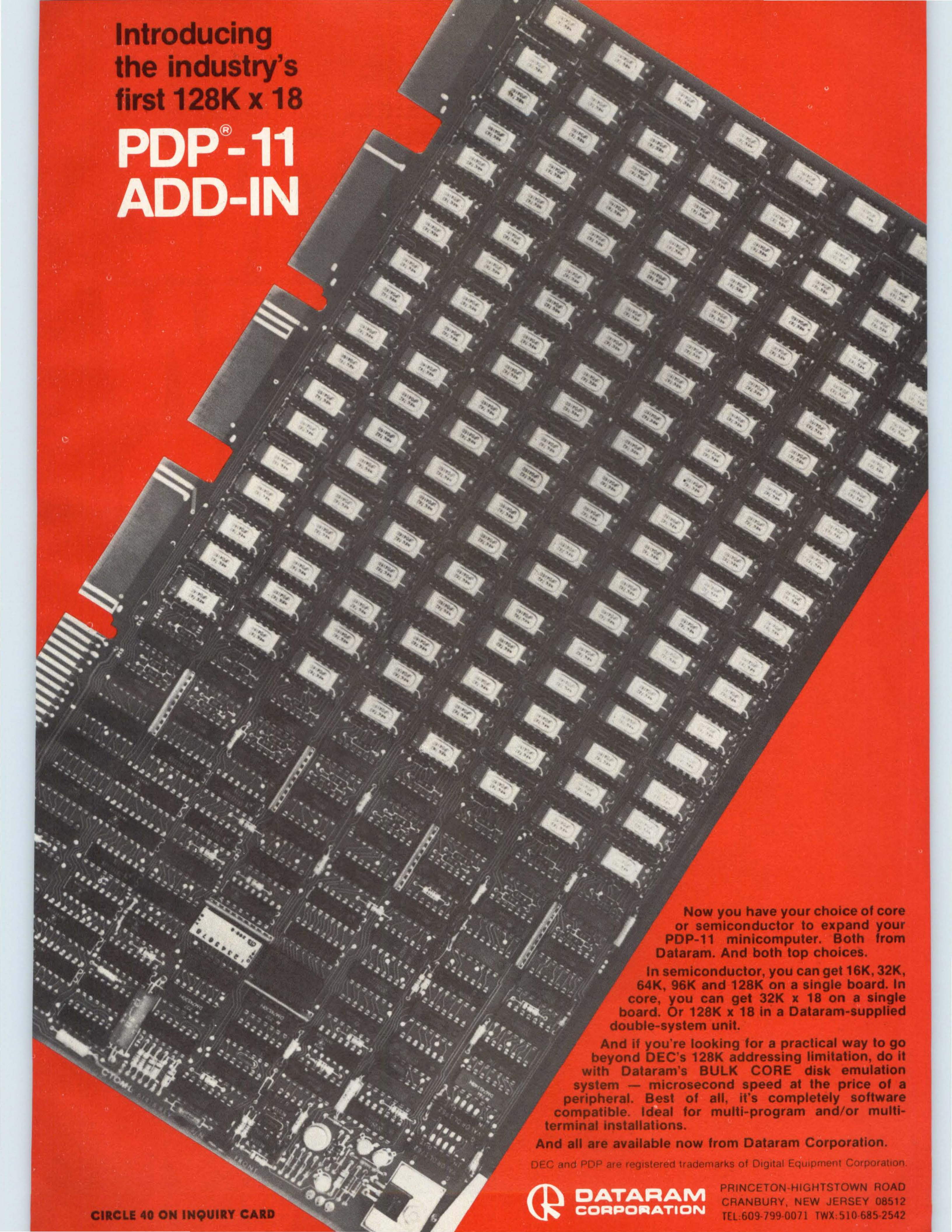
Basically, a precision optical system projects an image on the retina of the patient's eye through use of movable lenses and a second optical system measures sharpness of the image on the retina. Microcomputer control drives the movable lenses back and forth along the eye's optical axis until best focus occurs. To determine astigmatism the same measurement is repeated in several meridians. Analysis of measurements and calculation of refraction are maintained by the computer's program.

Once the patient is properly positioned in front of the instrument, the operator aligns the image on one of the patient's eyes. The computer automatically senses which eye is being aligned and is ready to make measurements as soon as alignment is complete. After the operator presses a start button, the computer controls all movements and measurements.

When measurements of one eye are complete, the operator realigns the system on the patient's other eye. Since the computer earlier determined which of the patient's eyes was being measured first, it automatically adjusts for the second eye. This assures that when the results are printed out automatically on the patient's file card the prescription for each eye will appear in the proper location. These results are presented in terms of sphere, cylinder, and axis, the common elements of vision correctable by prescription lenses.

There are two main sections in this automatic objective refractor: optical and computer. The optical section is made up essentially of lenses which are moved relative to the eye; position of these lenses indicates optical error of the eye being tested. Stepping motors which drive the lenses are operated directly from the computer.

Actually every function of the instrument is run by the built-in microcomputer. Rather than handling certain data computations, the microcomputer programs every activity of the instrument. Every light that comes on, every action resulting from closing of a switch,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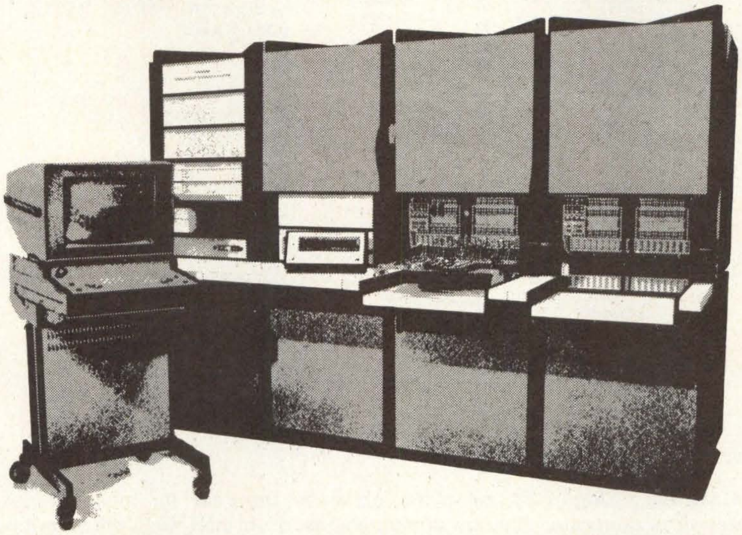
CIRCLE 40 ON INQUIRY CARD

AND IT'S LOADED.



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CIRCLE 41 ON INQUIRY CARD

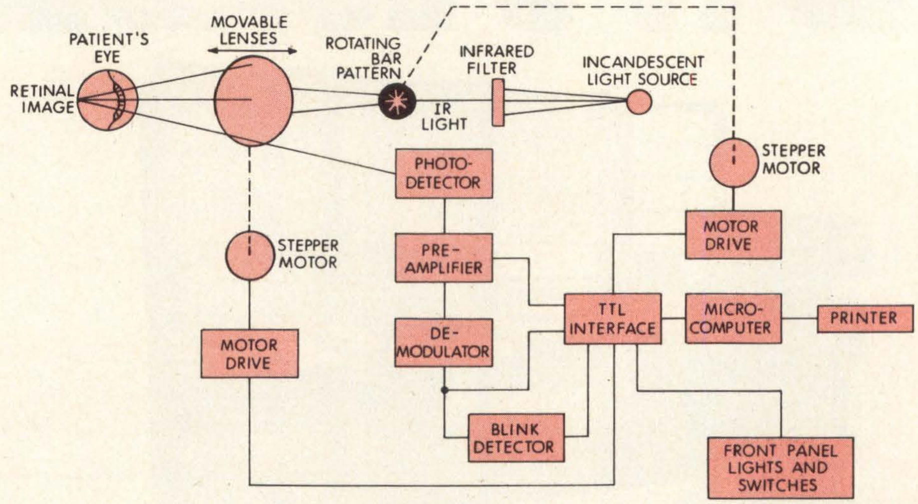


Diagram of Coherent's Dioptron® automatic objective refractor for measuring vision defects. Operation is controlled fully by computer based on Intel 4040 microprocessor. Incandescent light is filtered to allow only infrared light to pass. IR light is invisible to patient but white light target is projected to provide visible object on which to focus. IR light projects through optics into eye and is reflected back from retina where it is picked up by photodetector. Stepper motor moves lenses back and forth until location is found which provides proper vision—usually within one quarter diopter, an amount comparable to sheet of window glass. Six measurements are made of each eye, requiring about 20 s for each set. If patient blinks, computer stops measurements for 150 ms, then restarts without loss of accuracy. Prescription is provided as hardcopy printout on file card

and every signal to the stepping motors to move the lenses is controlled by the microcomputer. In addition, the microcomputer handles all measurements of lens position which indicate corrective requirements for achieving normal vision, all computations, and finally the hardcopy printout of the patient's prescription. It even decides and notifies the doctor if there are certain abnormalities about the particular patient's eyes that prevent accurate diagnosis.

Microcomputer Control Functions

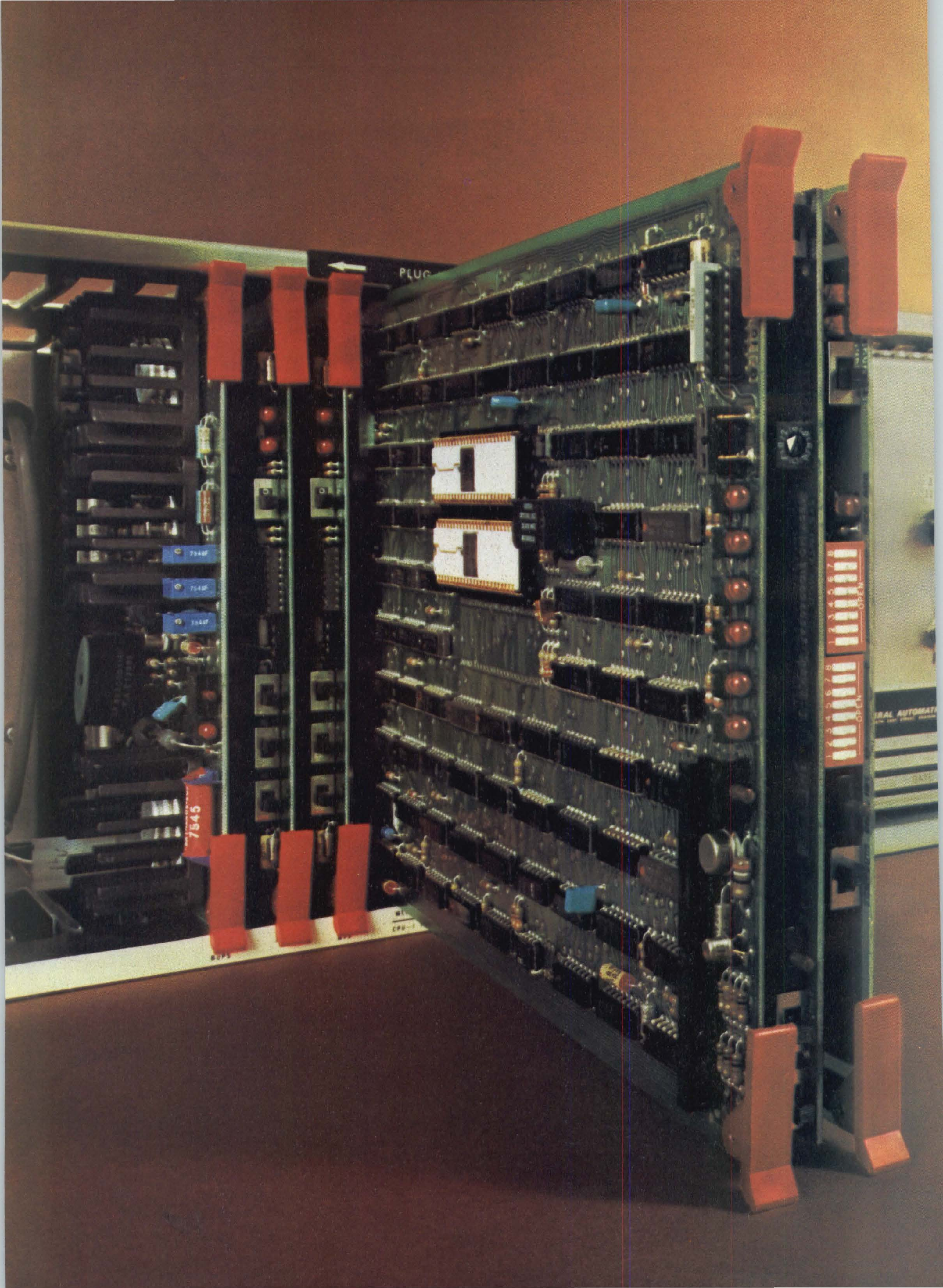
Central elements of Dioptron are an Intel 4040 microprocessor and its interface to most of the other system components. Original instruments had the computer cabinet separate from the optical head. The microcomputer was on three printed circuit boards and other components required five more. In all, there were 865 pins and connectors. Memory was on erasable p/ROM so that program changes could be made if necessary.

Dioptron II contains the microprocessor and other portions of the microcomputer on a single board and uses only one other board for their system components. There are only 430 pins and connectors, and four 1k-word x 8-bit, type 4308 metal mask ROMs fulfill all memory requirements.

Accuracy of the system in measuring corrective requirements of a patient's eyes is said to be within one quarter diopter for 75% of the cases. (One quarter diopter would look like a piece of window glass; it would be difficult for a patient to know that a quarter-diopter lens had been placed in front of his eye if he wasn't told.) However, the doctor normally works with the patient to determine how closely the instrument's prescription should be met. Some patients differ on the degree of correction with which they feel comfortable. Therefore, the doctor may decide not to prescribe lenses to the quarter-diopter corrective point.

Initially the operator aligns the instrument on one of the patient's eyes, requesting that the patient look at a starburst grating pattern of white light. This pattern serves merely as a focusing device; it has no other purpose in the measuring sequence. Actually, infrared light, which the patient cannot see, is used in the diagnosis procedures.

(Continued on p 72)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CIRCLE 43 ON INQUIRY CARD

Microcomputer-controlled Dioptron II in use. Only required operator adjustments are in aligning instrument to each of patient's eyes by moving joystick. Infrared imaging system, which is invisible to patient, allows operator to determine when eye is centered on target. Operator then pushes start button to initiate measuring procedure. Computer directs lenses to move in various patterns necessary to obtain at least six sequential measurements. All circuit boards and power supply are in cabinet behind switch panel

The computer takes six sequential measurements of the eye and fits the six data points into an algorithm that uses essentially a sine square curve fit. From that the computer determines near- or farsightedness, astigmatism, and angle of astigmatism—in about 20 s.

If the patient blinks during any test sequence, the computer senses the eyelid coming down and stops the measurement procedure for the duration of the blink, about 150 ms, after which it restarts measurement without having picked up information that might confuse the diagnosis. Even if several blinks occur, no data are lost. The computer also determines if some pathology or abnormality in a patient's cornea or lens is likely to lower measurement accuracy beyond an acceptable limit. The computer can order remeasurements to assure accuracy, or in some cases will produce a blank ticket. However, for cases where a doctor's practice includes a lot of patients with eye pathologies, the program can be set up to force a printed ticket on every patient. In that case, the ticket includes information on how many data scans were made, the rms deviation from a sine square curve fit, and other diagnostic information.

Circle 168 on Inquiry Card

Computers Have Large Role in Future of Robots for Factory Automation

Whatever influence the computer has had on the various manufacturing processes during past decades will be considered minor compared to the part it will play in the next few years. It has been used extensively in both design and data processing phases, but until now—for a number of reasons—has not been used to anywhere near its full potential in the manufacturing phase.

The Movement Toward Factory Automation

According to Elliott M. Estes, president of General Motors Corp,[1] the computer is one of the most valuable tools presently available—one whose use in manufacturing will increase by as much as 400% over the 1977 level by the end of 1982. (Already highly computerized, design functions will increase uses of computers by 40%, data processing by 9% in that same period.) "Within 10 years," according to Mr Estes, "computers will control about 90% of all the new machines in GM's manufacturing and assembly plants."

GM has relied heavily on computer aided design, particularly in its program to reduce the weight of its vehicles and to do so without overdependence on unconventional materials. However, the incorporation of increasing amounts of expensive, lightweight materials is necessarily occurring; and with these materials, economy of machining attains even greater importance.

For a 3200-pound automobile, nearly 1000 pounds of material were removed as waste in the production processes. GM's manufacturing groups, therefore, are studying the use of modular, integrated machining systems made up of numerically controlled (NC) centers under minicomputer control and mainframe computer supervision. Such systems would be used for low and medium volume production, or as backup to high volume production lines, but would not replace those rigid, automated lines. Flexibility and ability to be quickly reprogrammed to work on different parts would characterize the smaller NC centers.

Another element in this movement toward factory automation is the production line robot. Universal transfer devices, a more technical synonym for robots, have been used in automotive manufacturing processes for several years, but mostly in environmentally dangerous areas or where brute strength was needed.

Robots have been used routinely, for instance, in paint shops, but they were programmed to paint simple objects of relatively uniform shapes. Mr Estes pointed out, however, that to paint something as complex as the outside and inside of a car body, each NC painting system would have to be made up of at least 12 machines under constant, simultaneous control. In addition, it would have to be able to adapt to a continuously changing order of 2-door, 4-door, and station wagon bodies.

Reliability necessary for just this task would have to exceed what is available today. An assembly line cannot function if failure of any component causes

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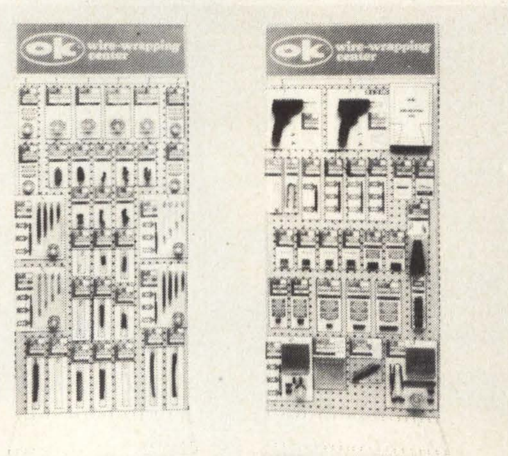
CIRCLE 44 ON INQUIRY CARD

wire wrapping center



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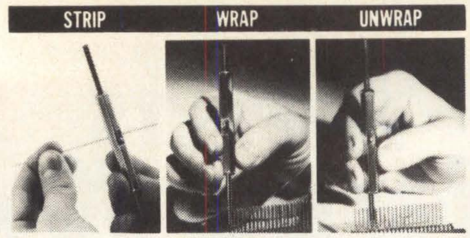

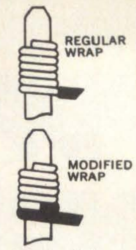

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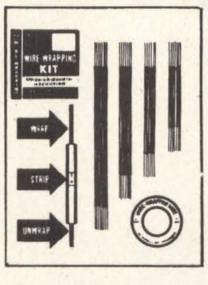

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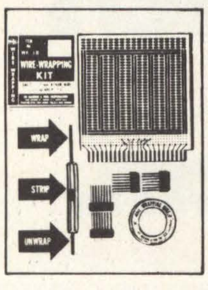

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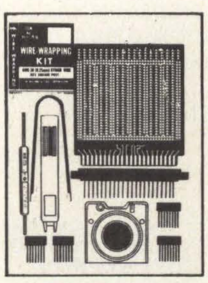

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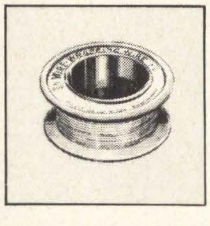
Contains: Hobby Wrap Tool WSU-30 M, Wire Dispenser WD-30-B, (2) 14 DIP's, (2) 16 DIP's, Hobby Board H-PCB-1, DIP/IC Insertion Tool INS-1416 and DIP/IC Extractor Tool EX-1

Wire-Wrapping Kit	WK-4B (Blue)	$25.99



ROLLS OF WIRE

Wire for wire-wrapping AWG-30 (0.25mm) KYNAR® wire, 50 ft. roll, silver plated, solid conductor, easy stripping.

30-AWG Blue Wire, 50ft. Roll	R-30B-0050	$1.98
30-AWG Yellow Wire 50ft. Roll	R-30Y-0050	$1.98
30-AWG White Wire, 50ft. Roll	R-30W-0050	$1.98
30-AWG Red Wire, 50ft. Roll	R-30R-0050	$1.98

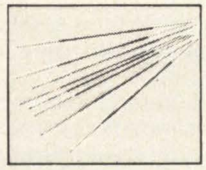
WIRE DISPENSER

- With 50 ft. Roll of AWG 30 KYNAR® wire-wrapping wire.
- Cuts the wire to length.
- Strips 1" of insulation.
- Refillable (For refills, see above)

Blue Wire	WD-30-B	$3.95
Yellow Wire	WD-30-Y	$3.95
White Wire	WD-30-W	$3.95
Red Wire	WD-30-R	$3.95

PRE CUT PRE STRIPPED WIRE

Wire for wire-wrapping, AWG-30 (0.25mm) KYNAR® wire, 50 wires per package stripped 1" both ends.



30-AWG blue Wire, 1" Long	30-B-50-010	$.99
30-AWG Yellow Wire, 1" Long	30-Y-50-010	$.99
30-AWG White Wire, 1" Long	30-W-50-010	$.99
30-AWG Red Wire, 1" Long	30-R-50-010	$.99
30-AWG Blue Wire, 2" Long	30-B-50-020	$1.07
30-AWG Yellow Wire, 2" Long	30-Y-50-020	$1.07
30-AWG White Wire, 2" Long	30-W-50-020	$1.07
30-AWG Red Wire, 2" Long	30-R-50-020	$1.07
30-AWG Blue Wire, 3" Long	30-B-50-030	$1.16
30-AWG Yellow Wire, 3" Long	30-Y-50-030	$1.16
30-AWG White Wire, 3" Long	30-W-50-030	$1.16
30-AWG Red Wire, 3" Long	30-R-50-030	$1.16
30-AWG Blue Wire, 4" Long	30-B-50-040	$1.23
30-AWG Yellow Wire, 4" Long	30-Y-50-040	$1.23
30-AWG White Wire, 4" Long	30-W-50-040	$1.23
30-AWG Red Wire, 4" Long	30-R-50-040	$1.23
30-AWG Blue Wire, 5" Long	30-B-50-050	$1.30
30-AWG Yellow Wire, 5" Long	30-Y-50-050	$1.30
30-AWG White Wire, 5" Long	30-W-50-050	$1.30
30-AWG Red Wire, 5" Long	30-R-50-050	$1.30
30-AWG Blue Wire, 6" Long	30-B-50-060	$1.38
30-AWG Yellow Wire, 6" Long	30-Y-50-060	$1.38
30-AWG White Wire, 6" Long	30-W-50-060	$1.38
30-AWG Red Wire, 6" Long	30-R-50-060	$1.38

® KYNAR-PENNWALT

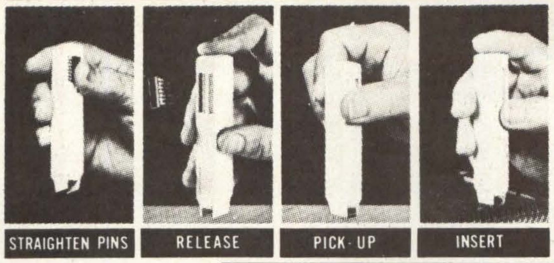
MINIMUM ORDER $25.00, SHIPPING CHARGE $1.00, N.Y. CITY AND STATE RESIDENTS ADD TAX

OK MACHINE & TOOL CORPORATION

3455 Conner St., Bronx, N.Y. 10475 ■ (212) 994-6600 ■ Telex 125091

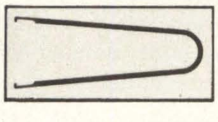
ok®

DIP/IC INSERTION TOOL WITH PIN STRAIGHTENER



14-16 Pin Dip IC Inserter	INS-1416	$3.49

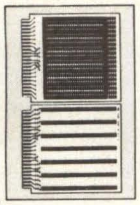
DIP/IC EXTRACTOR TOOL



The EX-1 Extractor is ideally suited for hobbyist or lab engineer. Featuring one piece spring steel construction. It will extract all LSI, MSI and SSI devices of from 8 to 24 pins.

Extractor Tool	EX-1	$1.49

P.C. BOARD



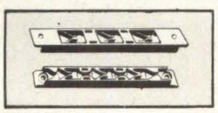
The 4 x 4.5 x 1/16 inch board is made of glass coated EPOXY Laminate and features solder coated 1 oz. copper pads. The board has provision for a 22/44 two sided edge connector, with contacts on standard .156 spacing. Edge contacts are non-dedicated for maximum flexibility.

The board contains a matrix of .040 in. diameter holes on .100 inch centers. The component side contains 76 two-hole pads that can accommodate any DIP size from 6-40 pins, as well as discrete components. Typical density is 18 of 14-Pin or 16-Pin DIP's. Components may be soldered directly to the board or intermediate sockets may be used for soldering or wire-wrapping.

Two independent bus systems are provided for voltage and ground on both sides of the board. In addition, the component side contains 14 individual busses running the full length of the board for complete wiring flexibility. These busses enable access from edge contacts to distant components. These busses can also serve to augment the voltage or ground busses, and may be cut to length for particular applications.

Hobby Board	H-PCB-1	$4.99

PC CARD GUIDES

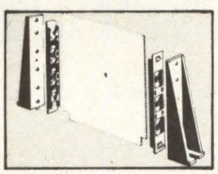


QUANTITY – ONE PAIR (2 pcs.)

TR-I consists of 2 guides precision molded with unique spring finger action that dampens shock and vibration, yet permits smooth insertion or extraction. Guides accommodate any card thickness from .040-.100 inches.

Card Guides	TR-1	$1.89

PC CARD GUIDES & BRACKETS

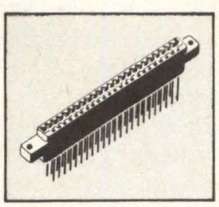


QUANTITY – ONE SET (4 pcs.)

TRS-2 kit includes 2 TR-1 guides plus 2 mounting brackets. Support brackets feature unique stabilizing post that permits secure mounting with only 1 screw.

Guides & Brackets	TRS-2	$3.79

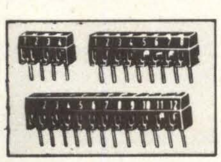
PC EDGE CONNECTOR



44 Pin, dual read out, .156" (3,96 mm) Contact Spacing, .025" (0,63 mm) square wire-wrapping pins.

P.C.. Edge Connector	CON-1	$3.49

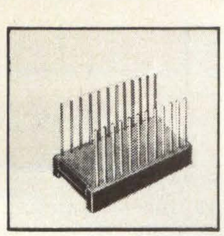
P.C.B. TERMINAL STRIPS



The TS strips provide positive screw activated clamping action, accommodate wire sizes 14-30 AWG (1, 8-0, 25mm). Pins are solder plated copper, .042 inch (1mm) diameter, on .200 incn (5mm) centers.

4-Pole	TS- 4	$1.39
8-Pole	TS- 8	$1.89
12-Pole	TS-12	$2.59

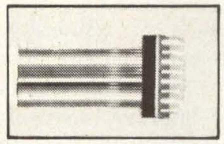
DIP SOCKET



Dual-in-line package, 3 level wire-wrapping, phosphor bronze contact, gold plated pins .025 (0,63mm) sq., .100 (2,54mm) center spacing.

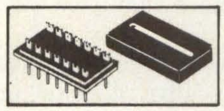
14 Pin Dip Socket	14 Dip	$0.79
16 Pin Dip Socket	16 Dip	$0.89

RIBBON CABLE ASSEMBLY SINGLE ENDED



With 14 Pin Dip Plug 24" Long (609mm)	SE14-24	$3.55
With 16 Pin Dip Plug 24" Long (609mm)	SE16-24	$3.75

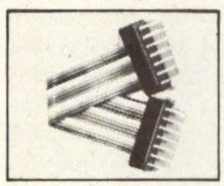
DIP PLUG WITH COVER FOR USE WITH RIBBON CABLE



14 Pin Plug & Cover	14-PLG	$1.45
16 Pin Plug & Cover	16-PLG	$1.59

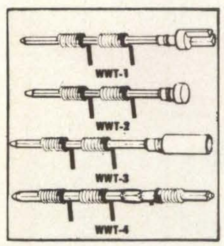
QUANTITY: 2 PLUGS, 2 COVERS

RIBBON CABLE ASSEMBLY DOUBLE ENDED



With 14 Pin Dip Plug - 2" Long	DE 14-2	$3.75
With 14 Pin Dip Plug - 4" Long	DE 14-4	$3.85
With 14 Pin Dip Plug - 8" Long	DE 14-8	$3.95
With 16 Pin Dip Plug - 2" Long	DE 16-2	$4.15
With 16 Pin Dip Plug - 4" Long	DE 16-4	$4.25
With 16 Pin Dip Plug - 8" Long	DE 16-8	$4.35

TERMINALS

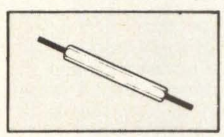


- .025 (0,63mm) Square Post
- 3 Level Wire-Wrapping
- Gold Plated

Slotted Terminal	WWT-1	$2.98
Single Sided Terminal	WWT-2	$2.98
IC Socket Terminal	WWT-3	$3.98
Double Sided Terminal	WWT-4	$1.98

25 PER PACKAGE

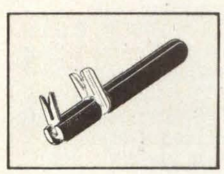
TERMINAL INSERTING TOOL



For inserting WWT-1, WWT-2, WWT-3, and WWT-4 Terminals into .040 (1,01mm) Dia. Holes.

INS-1	$2.49

WIRE CUT AND STRIP TOOL



Easy to operate . . . place wires (up to 4) in stripping slot with ends extending beyond cutter blades . . . press tool and pull . . . wire is cut and stripped to proper "wire-wrapping" length. The hardened steel cutting blades and sturdy construction of the tool insure long life.

Strip length easily adjustable for your applications.

DESCRIPTION	MODEL NUMBER	ADJUSTABLE "SHINER" LENGTH OF STRIPPED WIRE INCHES TO INCHES	Price
24 ga. Wire Cut and Strip Tool	ST-100-24	1⅜" — 1⅝"	$ 8.75
26 ga. Wire Cut and Strip Tool	ST-100-26	1⅜" — 1¹¹⁄₁₆"	$ 8.75
26 ga. Wire Cut and Strip Tool	ST-100-26-875	⅞" — 1⅛"	$ 8.75
28 ga. Wire Cut and Strip Tool	ST-100-28	⅞" — 1⅛"	$11.50
30 ga. Wire Cut and Strip Tool	ST-100-30	⅞" — 1⅛"	$11.50

THE ABOVE LIST OF CUT AND STRIP TOOLS ARE NOT APPLICABLE FOR MYLENE OR TEFLON INSULATION

MINIMUM ORDER $25.00, SHIPPING CHARGE $1.00, N.Y. CITY AND STATE RESIDENTS ADD TAX

OK MACHINE & TOOL CORPORATION

3455 Conner St., Bronx, N.Y. 10475 ■ (212) 994-6600 ■ Telex 125091 the entire line to shut down. Therefore, the NC painting systems must be able to redistribute work if one of the 12 machines fails; the painting must continue without interruption.

Cost of overcoming the present lack of reliability, however, is estimated to be much lower than the cost might be if GM were required to convert whole plants to water-based paints in order to improve environmental conditions for workers. In fact, with the NC robots, even stronger solvents could be used in the painting processes—which would trigger additional savings in the production procedures.

Overall economic backup for these statements has been offered by George Kuper, executive director of the National Center for Productivity and Quality of Working Life.[2] He pointed out that average productivity improvement in the U.S. during the past 10 years was less than 3% a year—and in some periods actually was negative—while that of Western Germany, Japan, and a few other countries was 6 to 14%. Forecasts for this rate through 1990 range from 2 to 2.4% for the U.S., but 3.8% for Western Europe and 6% for Japan.

According to Mr Kuper, new technology alone is not sufficient to support gains in productivity; that technology must be developed and put to work. He pointed out that a 1973 survey showed that 67% of America's metalworking equipment was over 10 years old—compared to 59% for the U.K., 50% for Italy, and 33% for Japan and West Germany; yet the value of NC tools shipped in 1974 was only 18% of the total. The Society of Manufacturing Engineers estimates that by 1986 the number of NC tools will reach 50% of new metalcutting tools produced. If that Delphi Study estimate is to be met, a huge number of NC tools will have to be produced and online in the next few years.

Ford Motor Co has found that robots or universal transfer devices (UTDs) retain basic problems as well as advantages, particularly when units are first installed.[3] One such problem is management—at every level. A statement of interest made by a general manager, for instance, might cause overreaction by middle management members and result in incorporation of UTDs before all groundwork had been carried out and before all education processes had been completed at lower levels.

In addition, it is extremely important that the first application be the "right" one, that there is a definite need that can be filled better by a robot than by some other device. Sometimes a temporary installation can be set up to allow both skilled trades and engineering personnel to become familiar with the robot—and actually operate it—before it is placed online. Just as important is choosing the right robot. If the one installed can't solve the problem, it might deter future installations.

There must be proper production backup capabilities built into the system. As mentioned previously, lack of reliability could force shutdown of an assembly line if other systems could not take over when a unit could no longer do its job. Other points to consider are special tooling requirements, the adequacy of plant layout and service facilities, and test equipment.

A particularly important consideration is safety. Experience at Ford Motor Co indicates that steps must be taken to protect nearby workers, many of whom may be curious and could inadvertently get into range of an "inoperative" robot that was merely waiting for a start signal. Stop devices should be installed to permit power to the robot to be cut in emergency situations—but without cutting power to other robots. The latter occurrence could cause additional safety problems depending on the sequence step at the time power was removed.

A great deal of research into additional capabilities for robots is underway,[4] but possibly one of the greatest concentrated efforts is being conducted in Japan.[5] There may already be as many as 56,000 robots in use in Japan for paint spraying, assembly of

TEKTRONIX
Portable Oscilloscopes

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Here's how to choose the TEKTRONIX Portable that's right for your application.

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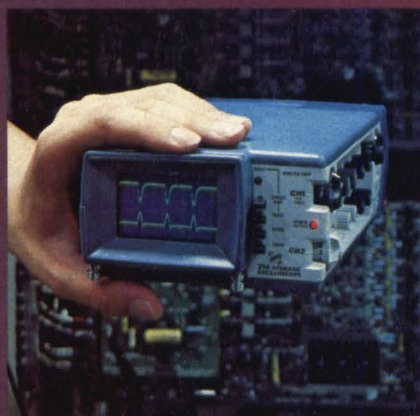
Take lab quality into the field with TEKTRONIX 400-Series Portable Oscilloscopes. Choose from nine models, including the 350-MHz 485, the widest bandwidth portable available today.

If you need to capture fast, non-repetitive events, the TEKTRONIX 466 is the only portable that can store a single-shot waveform at its full 100-MHz bandwidth. For military applications, consider the 465M, the new commercial equivalent of the AN/USM 425 triservice standard 100-MHz Oscilloscope.

The factory-installed DM44 Delta Delayed-Sweep Option adds a direct numerical readout to five TEKTRONIX 400-Series Scopes. At $445,* it's the least expensive, most accurate way to make digital-voltage, current, temperature and differential-time measurements. In the photograph, the DM44 is shown with the high-performance 475A, our new, moderately priced 250-MHz oscilloscope.

Each TEKTRONIX 400-Series Portable weighs less than 26 pounds.



200-Series Miniscopes

These go-anywhere miniscopes are the perfect traveling companions. Powered by internal batteries or external ac, and weighing less than 3.7 pounds, 200-Series Portables fit easily into your briefcase or toolbox. Four models, with bandwidths to 5 MHz, are available. If you need to make numerical-voltage and current measurements, select the unique 1-MHz 213 DMM/Oscilloscope.

All 200-Series Miniscopes are ruggedized to withstand the high-shock conditions and extreme temperatures of remote locations.

300-Series Portables – Excellent Size/Weight/Performance Combinations

Four models from SONY/TEKTRONIX make up the 300-Series Family. All weigh less than 11 pounds, yet offer bandwidths to 35 MHz (the SONY/TEKTRONIX 335). Various oscilloscopes feature dual trace, delayed sweep, battery operation, and long-term storage.

Take SONY/TEKTRONIX 300-Series Portables with you for servicing industrial control systems, on-board ship equipment and remote computer terminals–wherever light-weight, medium-bandwidth scopes are required.

T900-Series Low-Cost Oscilloscopes

Priced from $695,* T900 Scopes are ideal for cost-sensitive education, servicing, and manufacturing applications. Choose from five bench-top models including four dual-trace and one delayed-sweep oscilloscope.

If your requirements call for a versatile, low-cost, 35-MHz scope, examine the two newest members of our T900 family –the T932A and the T935A. Both feature composite triggering and differential while retaining all the popular features of their predecessors (the T932 with variable trigger-holdoff and the T935 with delayed sweep). We've even kept the prices the same.

All T900-Series Oscilloscopes are designed for ease-of-operation, simple maintenance, reliability and long life. They're the quality, low-cost scopes from Tektronix.

Service and Support Programs

Purchasing a TEKTRONIX Oscilloscope means more than buying an instrument from the industry leader. Applications assistance, training programs, worldwide service, and a large family of probes and accessories are available to help you get the most out of your TEKTRONIX Instrument. Classes in product theory and maintenance are also offered. The Long-Term Support Program insures continued parts availability. And your Tektronix Field Engineer will work with you to solve even the toughest servicing problems.

Here's How To Purchase a TEKTRONIX Portable.

To order a TEKTRONIX Portable Oscilloscope, contact your Tektronix Field Engineer. He can also arrange for a demonstration and provide complete specifications. Or for our latest Portable Oscilloscope Brochure, write: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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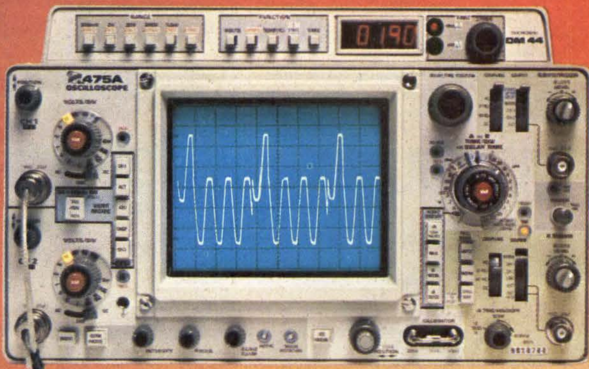
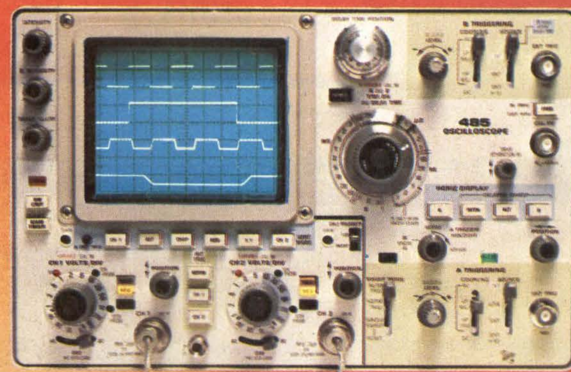
For technical data, circle 48 on Inquiry Card.
For a demonstration, circle 49 on Inquiry Card.

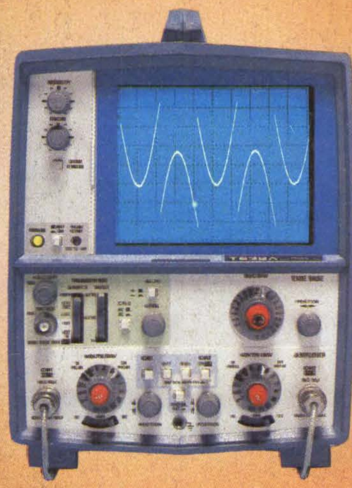


475A DM44



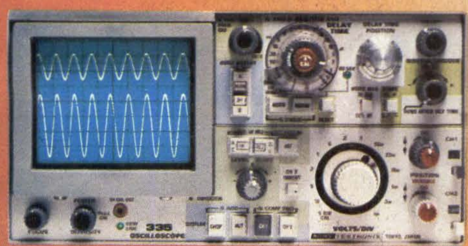
485

213



T932A

T935A



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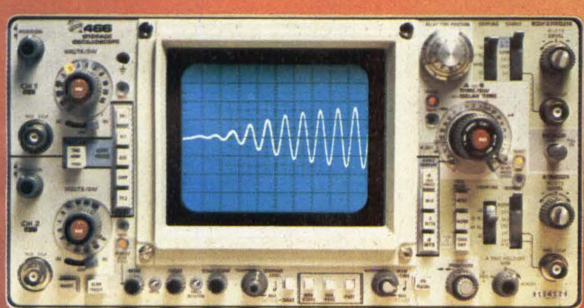

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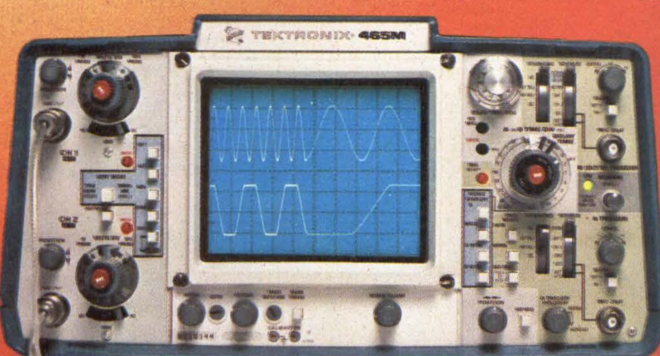

465M

	Product	Bw	Dual Trace	Delayed Sweep	Fastest Sweep Rate	Other Special Features	Price*
Storage Models	466	100 MHz @ 5 mV/div	yes	yes	5 ns/div	3000 div/μs stored writing speed	$4895
	464	100 MHz @ 5 mV/div	yes	yes	5 ns/div	110 div/μs stored writing speed	4120
	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	3245
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)	2385
	214	500 kHz @ 10mV/div	yes		1 μs/div	Only 3.5 lbs (1.6 kg)	1520
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	1350
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	5225
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable	3555
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable	3195
	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	2295
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Triservice standard 100-MHz scope	2345
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw	1850
	335	35 MHz @ 10 mV/div	yes	yes	20 ns/div	Only 10.5 lbs (4.8 kg)	1925
	326	10 MHz @ 10 mV/div	yes		100 ns/div	Internal battery	2180
	323	4 MHz @ 10 mV/div			500 ns/div	Only 7 lbs (3.2 kg)	1445
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs (1.6 kg)	1025
	213	1 MHz @ 20 mV/div			400 ns/div	DMM/Oscilloscope @ 3.7 lbs (1.7 kg)	1520
	212	500 kHz @ 10 mV/div	yes		1 μs/div	Low cost for dual trace & battery	1080
	T935A **(New)**	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Variable trigger-holdoff and differential	1435
	T932A **(New)**	35 MHz @ 2 mV/div	yes		10 ns/div	Delayed sweep and differential	1155
	T922	15 MHz @ 2 mV/div	yes		20 ns/div	Low-cost dual-trace scope	850
	T922R	15 MHz @ 2 mV/div	yes		20 ns/div	Rackmount version of T922	1220
	T921	15 MHz @ 2 mV/div			20 ns/div	Lowest-cost TEKTRONIX Portable	695
Time Interval Readout	DM44	Optional, factory-installed, direct numerical readout of time intervals and DMM functions for the 464, 465, 466, 475, and 475A					445

*U.S. sales prices are F.O.B. Beaverton, OR. For price and availability outside the United States, please contact the nearest Tektronix Field Office, Distributor or Representative. Prices are subject to change without notice.

Our logic tester's guided probe is smart.

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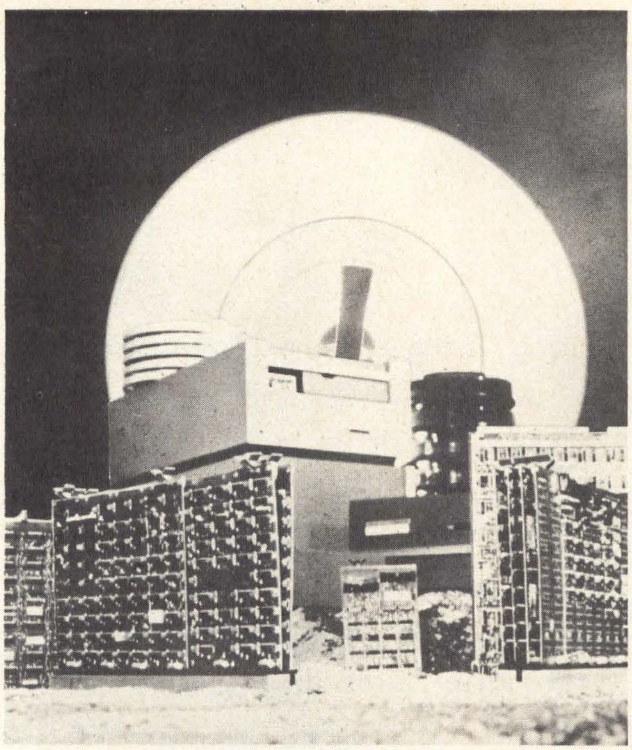

parts, servicing machine tools, welding, and die casting. In addition, the Japanese government might set up a national project to build a totally automated, completely unmanned factory. An assembly robot in this factory might have vision capability.

Seventy laboratories in Japan are conducting research on robots. All are either funded by the government or attached to universities. Projects range from pure research into vision and manipulation to pattern and voice recognition.

In the U.S., the National Bureau of Standards has pressed the concept of industrial robots coupled with machine tools as a step toward an automatic factory.[6] This study has been in addition to its sponsored research into sensors and computer control systems for industrial robots.

Several control hierarchies, each involving feedback, would be involved in an industrial robot for the automated factory. Lowest level would involve servocontrol of joint functions. Next, primitive function routines would be sequenced to perform more complicated tasks at the second level. At the third level, the last in the "lower" group of the control hierarchy, elemental move commands would serve as inputs.

Two higher control levels complete the hierarchy. Input task commands plus sensory feedback from the robot and the workstation cause the fourth level to send sequences of elemental move commands back to the third level. Finally, the fifth or top level of control would be responsible for assigning tasks to different workstations. This hierarchical partitioning of control problems into subproblems is expected to ease the use of sensory feedback in real-time control systems for robots and computer integrated manufacturing systems.

Summary

Such activities as listed here and discussed more thoroughly at the SME conferences are expected to have considerable impact on the future of practical robots. The overall picture is far too extensive to be covered other than briefly in a survey such as this. Reports on research into relevant areas can be located in various scientific media.

References

1. E. M. Estes, "The Challenge: Pack Four Decades of Change Into One," Plenary Session Paper presented at Autofact I, Society of Manufacturing Engineers Conference, Oct 31, 1977
2. G. Kuper, "The Automated Factory—Key Management Considerations," Plenary Session Paper presented at Autofact I, SME, Oct 31, 1977
3. G. C. Macri, "Analysis of First UTD Installation Failures," Technical Paper MS77-735, presented at Autofact I, Robots II Conf, Oct 31-Nov 3, 1977. Copyright SME
4. S. F. Shapiro, "Digital Technology Enables Robots to 'See'," *Computer Design*, Jan 1978, pp 43-59
5. R. A. Gonsalves and S. Kurlat, "Robotics in Japan from an American Perspective," Technical Paper MS77-754, Robots II. Copyright SME
6. J. Albus, *et al*, "Control Concepts for Industrial Robots in an Automatic Factory," Technical Paper MS77-745, Robots II

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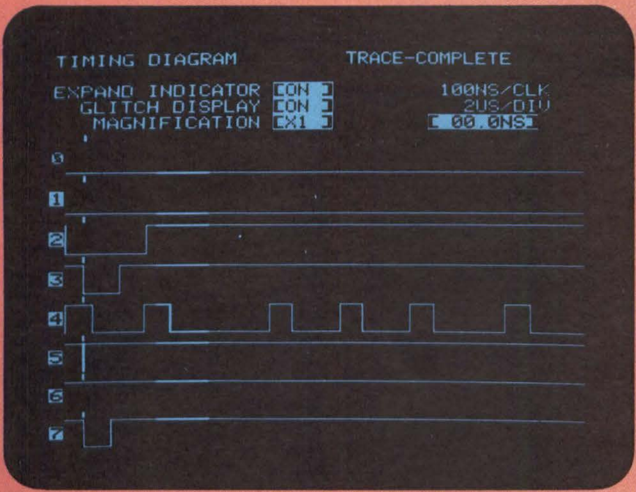
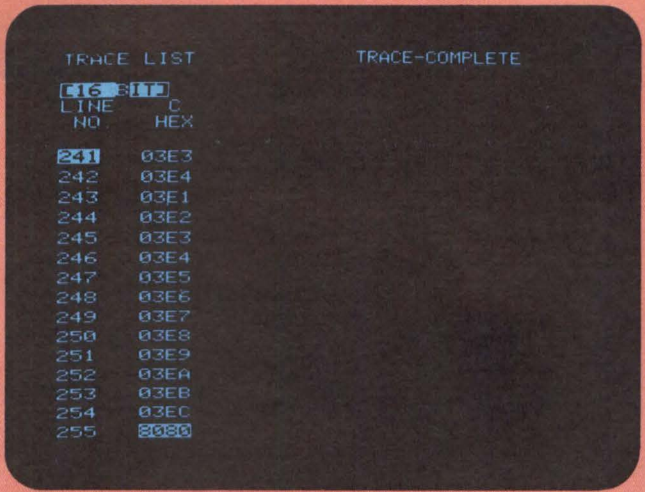
Timing Analysis—The hardware approach

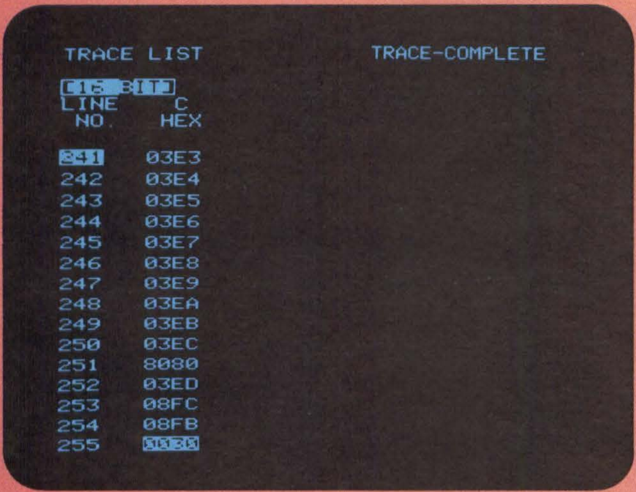


Trigger on glitches. A glitch on an input to a one shot (channel 5) is causing a false interrupt (channel 7). This glitch (which is intensified to distinguish it from data) can be used to trigger state as well as time displays.

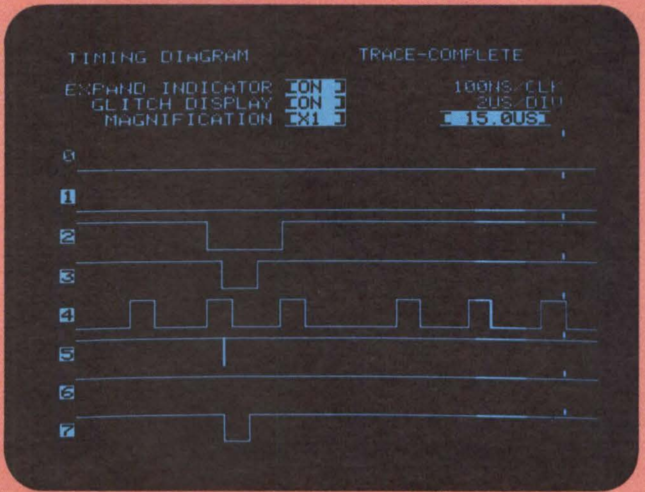


Observing state display shows address flow at the moment the glitch occurs and reveals that the I/O port address 8080 always occurs at the same time. This would lead you to observe I/O related signals for transitions occurring simultaneously with the glitch.

State Analysis—The "Software" approach



Trigger on state. The interrupt vector (0030) can be used as the trigger point to observe address flow prior to the false interrupt. Evaluation shows that the I/O port address 8080 always appears four machine cycles prior to the interrupt vector.



Observing timing display of signals on I/O and one-shot shows that the glitch on the input to the one shot (channel 5) occurs four machine cycles before the trigger point and is coincident with the transition on I/O read (line 3) indicating possible capacitive coupling.

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Electro/78

Electronic Show and Convention / May 23-25
Hynes Veteran's Auditorium / Sheraton Boston Hotel

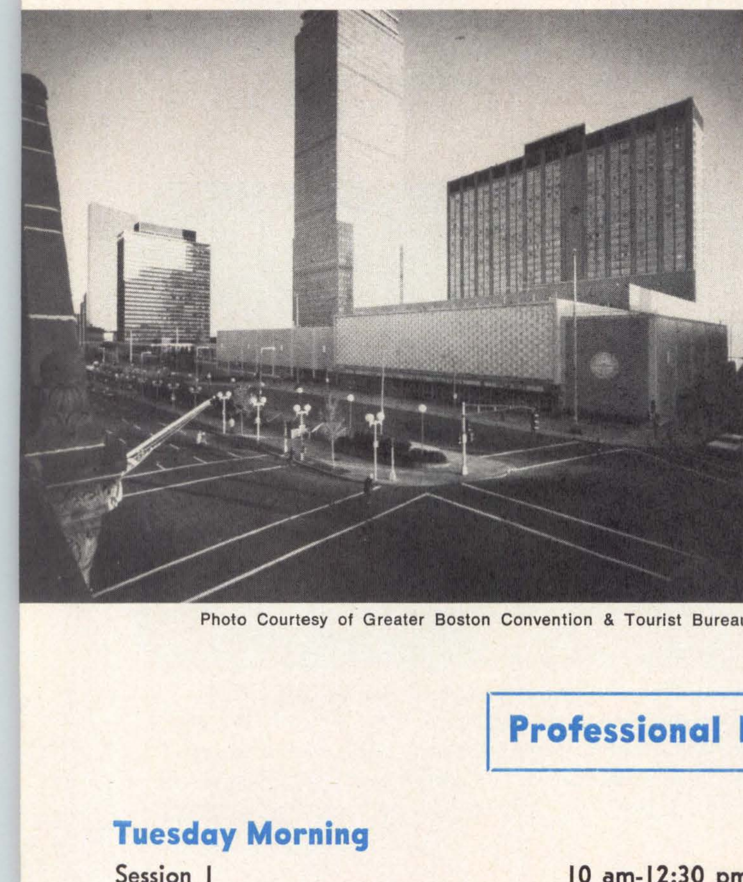

Photo Courtesy of Greater Boston Convention & Tourist Bureau

Electro '78, to be held in Boston's Hynes Auditorium, will be a 3-day exposition including a wide range of conferences, product exhibitions, and special attractions, all directed toward the theme, "Look Ahead." The show, as in previous years, is co-sponsored by the New England and New York sections and chapters, respectively, of the Institute for Electrical and Electronic Engineers and the Electronic Representatives Association.

The Convention Committee, under the direction of Convention Manager, Harold S. Goldberg, Data Precision Corp, Wakefield, Mass, has designed a professional program consisting of 34 half-day technical sessions. All will address here-and-now trends, needs, and applications on subjects ranging from automatic test equipment and home computing, to fiber-optic data links. Beginning at 10 am each day, sessions will run concurrently during both the morning and afternoon. In addition, a special evening session devoted to "A New Beach-Head for Scientific Discovery: The Human Energy Field," will begin at 8 pm on Wednesday. Convention exhibits will encompass new high technology electronics products and systems. Exhibit hours will be from 9:30 am to 6 pm on Tuesday, 9:30 am to 8 pm on Wednesday, and 9:30 am to 5 pm on Thursday.

Special attractions on Monday, May 22, the day prior to the Electro '78 opening, will include an all-day marketing conference and the Keynote Luncheon. The latter will be held in the Boston-Sheraton Convention Ballroom at noon. Keynote speaker will be Bernard Gordon, President of Analogic Corp. This luncheon also will be the platform for presentation of the Omega Achievers Award for Television/Radio to General David Sarnoff. An acceptance speech will be made by Robert Sarnoff. The annual All-Industry Reception will take place on Tuesday from 6:30 to 8:30 pm in the Grand Ballroom.

A film theater, from 10 am to 4:30 pm each day, will exhibit the latest films, which have been screened by the co-sponsors, on new technology advances.

Registration fees for Electro '78 are $6 for IEEE members and $9 for nonmembers. Deadline for advance registration is May 5.

The following excerpts cover sessions of interest to *Computer Design* readers, and evolve from information available at press time.

Professional Program Excerpts

Tuesday Morning

Session 1 — **10 am-12:30 pm**

Looking Ahead at High Density Packaging

Organizer/Co-chairman: Stanley M. Stuhlbarg, Hughes Aircraft Co, Newport Beach, Calif

Co-chairman: Walter Vilkelis, International Business Machines, Inc, Hopewell Junction, NY

1960's-style DIPs have shortcomings in the 1970's, and as the 1980's are approached, ceramic wiring board packaging technologies and hybrid microcircuits are emerging. Future semiconductors will most likely be packaged in leadless chip carriers and/or assembled to microcircuits from pretestable tape chip carriers. This session will encompass such packaging problems and solutions from the user's viewpoint.

"LSI Package Standardization," Daniel I. Amey, Sperry Univac Computer Systems

"Computer Memory Density And Its Packaging Implications," Bruce G. Tenpas, Control Data Corp

"Memory Systems—An Ultimate In Packaging Density," Emory Garth, Texas Instruments, Inc

"LSI In Computers—A Systems Approach," Don Seraphin, International Business Machines, Inc

"High Density Packaging Applied To A Mainframe Computer," Lin C. Wu, Amdahl Corp

Session 2 — **10 am-12:30 pm**

Software for Microprocessors

Organizer/Chairman: Max Schindler, *Electronic Design*, Rochelle Park, NJ

User-oriented systems and applications software expand microprocessor utilization even faster than improvements in hardware. The session opens with a survey and comparison of the most

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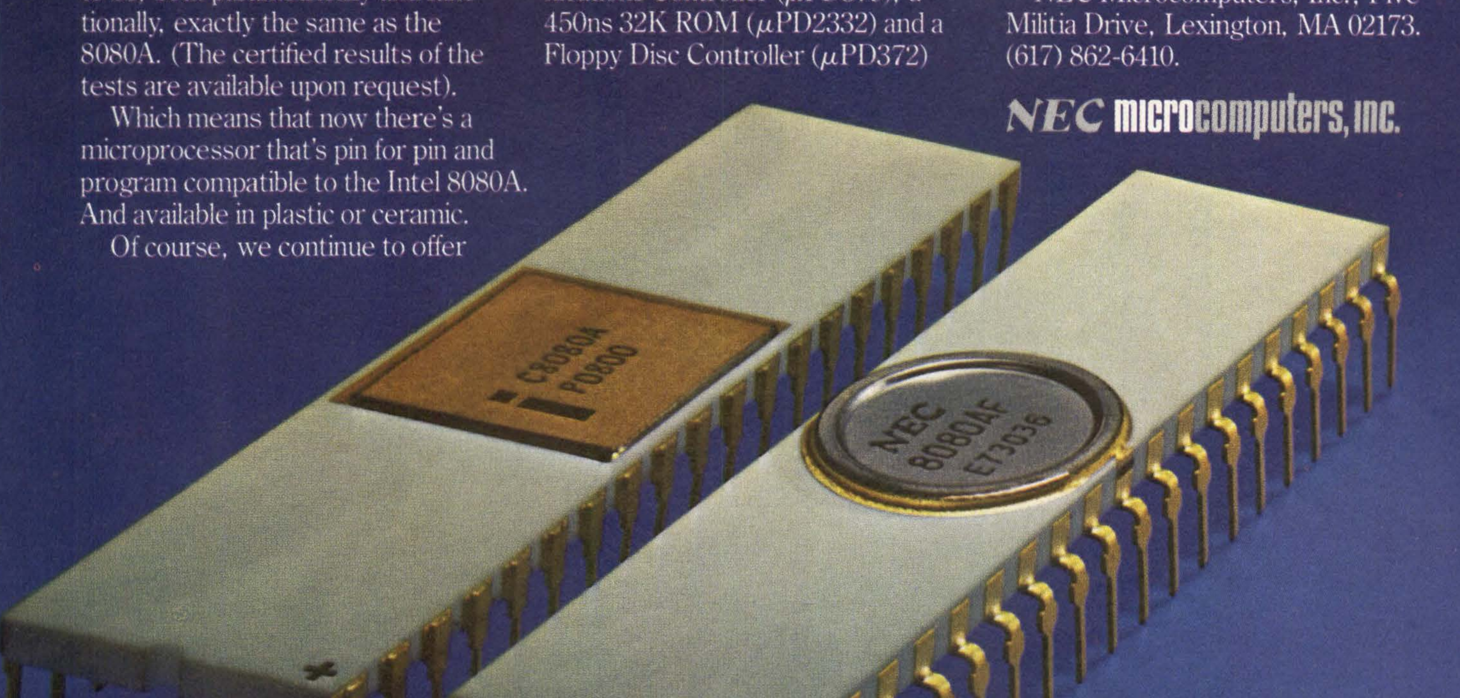

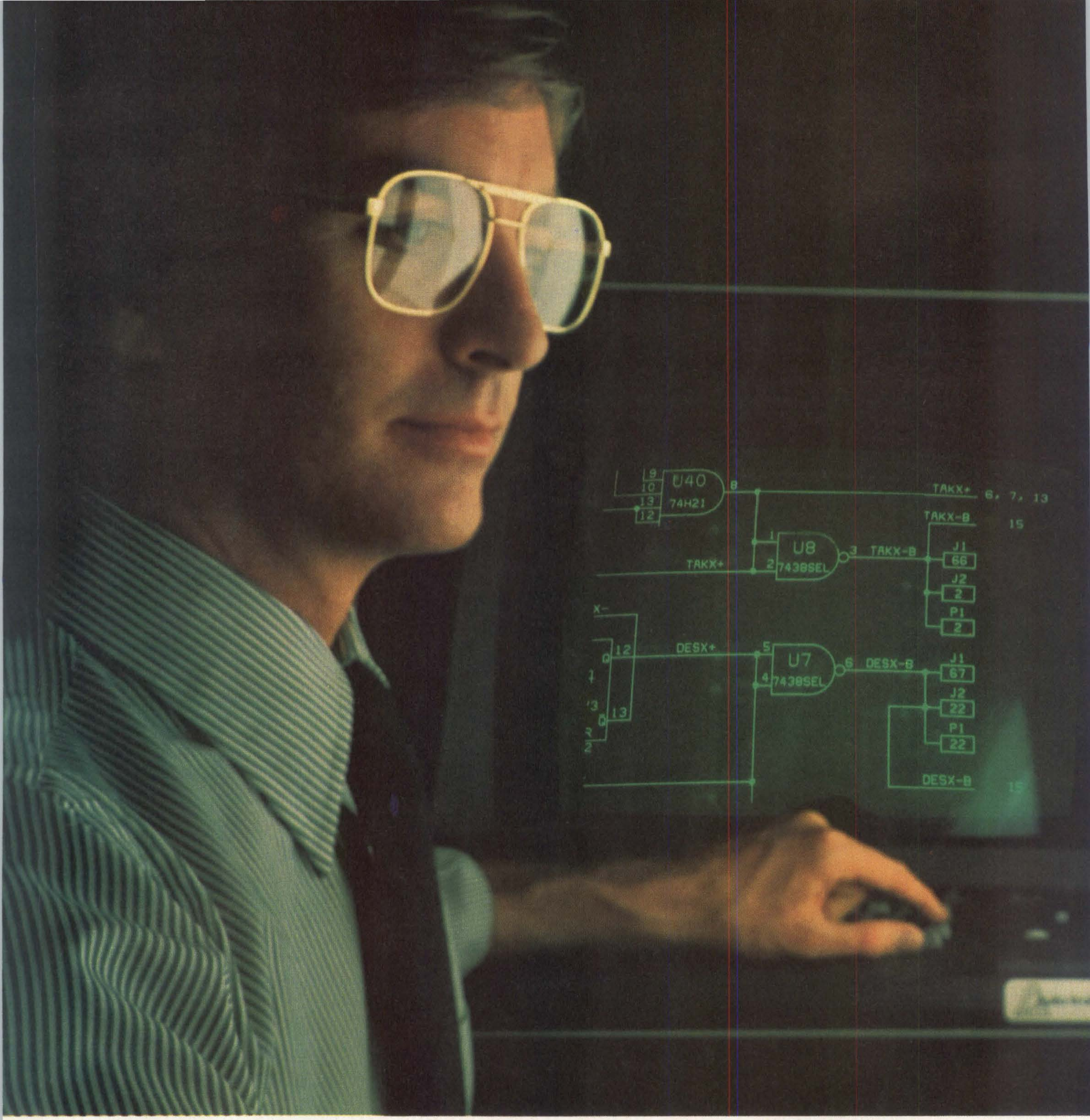

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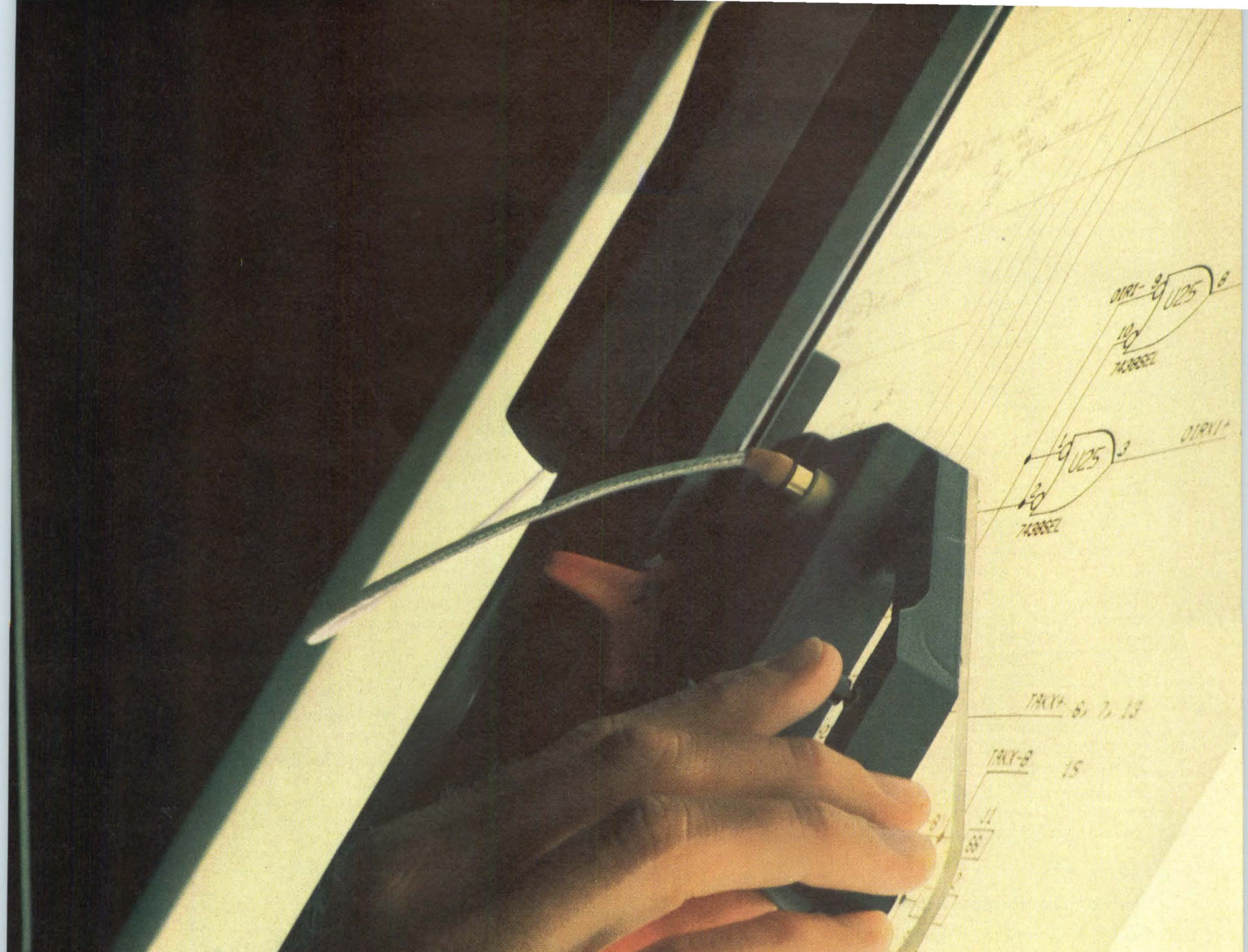

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prominent microprocessor software and instruction sets, then presents several novel software systems.

"Software Capabilities of Prominent Microprocessors," William E. Augustine, Datapro Inc

"Configuration Software for Interactive Applications," Edward Jay Kleban, ECD Corp

"Microprocessor Development Tools Have Come of Age," Mike Kane, Intel Corp

"TAL-80, a High Level Language for the 8080," David Benevy, CM Software, Inc

"Tradeoffs in the Development of Microprocessor Software," Michael Rooney, Boston Systems Office

Session 3 10 am-12:30 pm

Testing Microprocessor-Based Boards

Organizer/Chairman: Jack Holland, Harris Corp, Ft Lauderdale, Fla

Literature available to aid the designer in developing microprocessor based boards shows that with a "system" on a PC board, the manufacturing labor costs are greatly dependent on the test costs. This session gives several approaches of attacking problems associated with testing microprocessor based boards.

"A User Look at On-Board Functional Testing," Nick Wells, Digital Equipment Corp

"A Test Strategy for Microprocessor-Based Boards," Peter Hansen, Teradyne, Inc

"Simulation Aids for Complex PCBS," David Schneider, Instrumentation Engineering

"Structured Testing," Burnell West, Data Test Corp

Session 4 10 am-12:30 pm

Bridging the Analog-to-Digital Gap

Organizer/Chairman: Robert Morrison, Burr-Brown Research Corp, Tucson, Ariz

In the past, components and techniques have existed to bridge the gap from the linear world to the digital environment of the microprocessor. It has been necessary to revamp traditional analog approaches through size and price reduction. This session provides material to guide an engineer in designing with these new components. Circuits, software, and architecture specifically intended for microprocessor analog interfaces will be discussed.

"A Monolithic Data Acquisition System—Its Design and Application," John Jorgensen, National Semiconductor

"Hybrid Data Acquisition System," Jeffrey R. Riskin, Analog Devices Inc

"Update Your Analog Designs for Today's Microcomputer World," Steve Harward, Burr-Brown Research Corp

"Simplify Analog I/O System Design—Design It With Low Cost Microprocessor Compatible Components," Bob Calkins, Micro Networks

Session 5 10 am-12:30 pm

Recent Advances in Computer Aids to Circuit Design

Organizer/Chairman: J. J. Golembeski, Bell Laboratories, Holmdel, NJ

Talks include the major interest areas of modeling and characterization, hybrid and logic analyses, tolerance analysis, and future direction for tolerancing. This session is oriented toward applications and presents much breadth.

"Statistical Modeling for Circuit Design," E. M. Butler, Bell Laboratories

"SCAMPER—A New Simulator for Circuit Analysis," J. Miller and M. Blostein, McGill University, Canada

"Hybrid Simulation for LSI Design," A. R. Newton and D. O. Pederson, University of California at Berkeley

"Yield Maximization and Tolerance Assignment Via Simplicial Approximation," L. M. Vidigal, G. Hachtel, and R. Brayton, Carnegie-Mellon University

"A Multi-Level Simulation Strategy," Harold Shichman, Bell Laboratories

Session 6 10 am-12:30 pm

Entrepreneuring with New Applications for Electronics

Organizer/Chairman: Thomas Jones, Massachusetts Institute of Technology, Cambridge, Mass

Identifying real-world problem areas which are amenable to solution by the application of electronic technologies requires a variety of approaches. The need for the innovator to be present at the site of the problem seems to be a fundamental prerequisite for the identification of new applications. Case histories involving the identification problem, the application of the electronic technology to it, and marketing implications are presented in this session.

"An Overview of 'Search for Future Electronic Applications,'" Alberto Socolovsky, *Electronic Business*

"An Industry Searches for Future Electronic Applications," Dave Beaubien, EG & G, Inc

"The Role of a Component Manufacturer," Fredrico Faggin, Zilog, Inc

"Venture Capital for Future Electronic Applications," John Mahor, Exxon Enterprises

Tuesday Afternoon

Session 8 2-4:30 pm

High End Microcomputer Applications

Organizer/Chairman: Joe Austin, Digital Equipment Corp, Marlboro, Mass

This session will define the high end microcomputer as being a single-board, 16-bit computer. The applications described will illustrate the basic concept of microcomputer small package/large performance and will discuss choosing system components.

"Microcomputer Network for Manufacturing and Process Control," Dick Pleau, Data General Corp

"High End Microcomputer for Multi-Terminal Applications," John Cohen, Quandex Corp

"16-Bit Microcomputer in the Control Environment," Greg Golian and Deene Ogden, Texas Instruments, Inc

"The America's Cup Yacht Race—An Example of 16-Bit Microcomputer Power and Flexibility," David Schanin, Digital Equipment Corp

Session 9 2-4:30 pm

Using ATE More Effectively

Organizer/Chairman: Dick Stein, Computer Automation, Irvine, Calif

When automatic test equipment (ATE) is utilized to test electronic subassemblies, a manufacturing focal point is created, which is often overlooked. By datalogging and fault-trend analysis, the full measure of payback can be realized. This session will describe a means of implementing various testing and design feedback functions at this testing focal point.

"In-Circuit Test System Data Logging," Tom Coleman, Faultfinders, Inc

"Computer-Aided Design Supports Automatic Test Systems," Robert Gothie, Computervision Corp

"Utilizing the ATE System for More Than Just Go/No-Go Testing," Michael W. Salter, GenRad, Inc

"A Distributed Processing System for Manufacturing Information," David A. Smith, Computer Automation, Inc

Session 10 — 2-4:30 pm

μP-Interfacing Today and Tomorrow

Chairman: Narpat Bhandari, Signetics Corp, Sunnyvale, Calif

Panelists Paul Brokaw, Analog Devices; Tom Frederickson, National Semiconductor Corp; Dan Dooley, Precision Monolithics Inc; John Titus, Tychon, Inc; Bernie Gordon, Analogic Corp; and Kent Simcoe, Intel Corp will focus on analog and digital interfacing in μP-based systems through describing the role of new peripherals, converters, and other related products. Systems interfacing problems such as accuracy, speed, partitioning, hardware/software tradeoffs, and price/performance will be examined.

Wednesday Morning

Session 14 — 10 am-12:30 pm

Microprocessor Applications in NASA

Organizer/Chairman: Fred Lesh, California Institute of Technology, Pasadena, Calif

NASA is continually discovering myriad uses for microprocessors. This session explores interesting NASA microprocessor applications on the ground, in space, and in the sea.

"A Microprocessor-Controlled Solid-State Recorder," William M. Howle, Jr, NASA Langley Research Ctr

"Microprocessor Networks for Spacecraft Support," Tony Villasenor, Goddard Space Flight Ctr

"Escort—A Data Acquisition and Display System to Support Research Testing," Robert L. Miller, Lewis Research Ctr

"A Microprocessor-Based Nimbus 6 Ground Station," William E. Holmes, Goddard Space Flight Ctr

"A Distributed Microprocessor System for Topographic Imaging of the Ocean Floor," George R. Hansen, Jet Propulsion Laboratory

Session 16 — 10 am-12:30 pm

Peripherals for Home Computers: A Look Into the Future

Organizer/Chairman: Clark E. Johnson, Jr, Micro Communications Corp, Waltham, Mass

This session will present an overview of home computers and look at peripheral requirements over the next five years. Included will be systematization of the peripheral interface bus; memory requirements and how new technologies may satisfy them; the manufacturer's view of peripheral requirements; and the future role of large mainframe manufacturers.

"The Home Computer in the Next Five Years: A Fad or a Revolution?" Jerry Wassermen, Arthur D. Little, Inc

"A System Approach to I/O," Robert Glorioso, Digital Equipment Corp

"Where It's At—Low Cost Data Storage for Memory Intensive Systems," Dennis Speliotis, Micro Bit Corp

"What Role Will the Big Guys Play?" John R. Morrison, Control Data Corp

"What's Needed in Peripherals? From the Users' Point of View," Steven Leininger, Tandy Advanced Products

Session 18 — 10 am-12:30 pm

Logic Measurement and Development Products

Organizer: Bill Furlow, Tektronix, Inc, Beaverton, Ore
Chairman: James Geisman, Tektronix, Inc, Beaverton, Ore

This session will look at test equipment for logic measurement and development, including manufacturer details on availability. Knowledgeable engineering users of this equipment will describe their point of view and requirements; and an analyst will review future trends in the market.

"Data Domain Analysis—Where From and Where To?" Charles House, Hewlett-Packard Co

"Logic Measurement and Development Tools for the Engineer," Bruce Hamilton, Tektronix, Inc

"The Use of Microprocessor Design Aids," Warren Saltz, Digital Equipment Corp

"What New Equipment Do You Need for Logic Development Tasks?" Marshall Kidd, General Electric Co

"The Future Market for Logic Measurement and Development Products," John O'Boyle, Gnostic Concepts, Inc

Wednesday Afternoon

Session 20 — 2-4:30 pm

Examining Single-Chip μP Products

Organizer/Chairman: V. K. L. Huang, Bell Telephone Laboratories, Holmdel, NJ

With increasing LSI capabilities, one-chip microcomputer systems provide cost-effective solutions to systems design. This session will examine the state-of-the-art in the development of single-chip microcomputer products, by emphasizing performance tradeoffs as the optimum single-chip design for cost sensitive segments of the microcomputer market.

"Low End Processors Reviewed and Projected," Phil Hughes, National Semiconductor Corp

"Single-Chip Microcomputers: Lowering Systems Cost Through Higher Integration," Jeff Miller, Intel Corp

"TMS 9940—Single-Chip Microcomputer," John Bryant, Texas Instruments Inc

"Sophisticated One-Chip Microcomputer and a Powerful Microprocessor," Bernard Peuto, Zilog, Inc

"Single-Chip Microcomputers," Jim Vittera, Mostek Corp

Session 21 — 2-4:30 pm

Computer Applications in Public Utility Control Centers

Organizer/Chairman: Kjell Carlsen, General Electric Co, Schenectady, NY

This session will include descriptions of computer system architecture, application programs required to control the system, the data base required to support online computer codes, and man-machine interfaces. In addition, aspects of system operation training will be covered.

"The Architecture and Functions of Control Computer Installations," Tomas E. Dy Liacco, Cleveland Electric Illuminating Co

"Application Programs in a Control Center Environment," N. Peterson, Systems Control, Inc

"Data Base Requirements and Designs for Control Centers Operation," Ralph Masiello, Autocon Industries, Inc

"Utility Control Center Man-Machine Interfaces," Harold Pantis, Philadelphia Electric Co

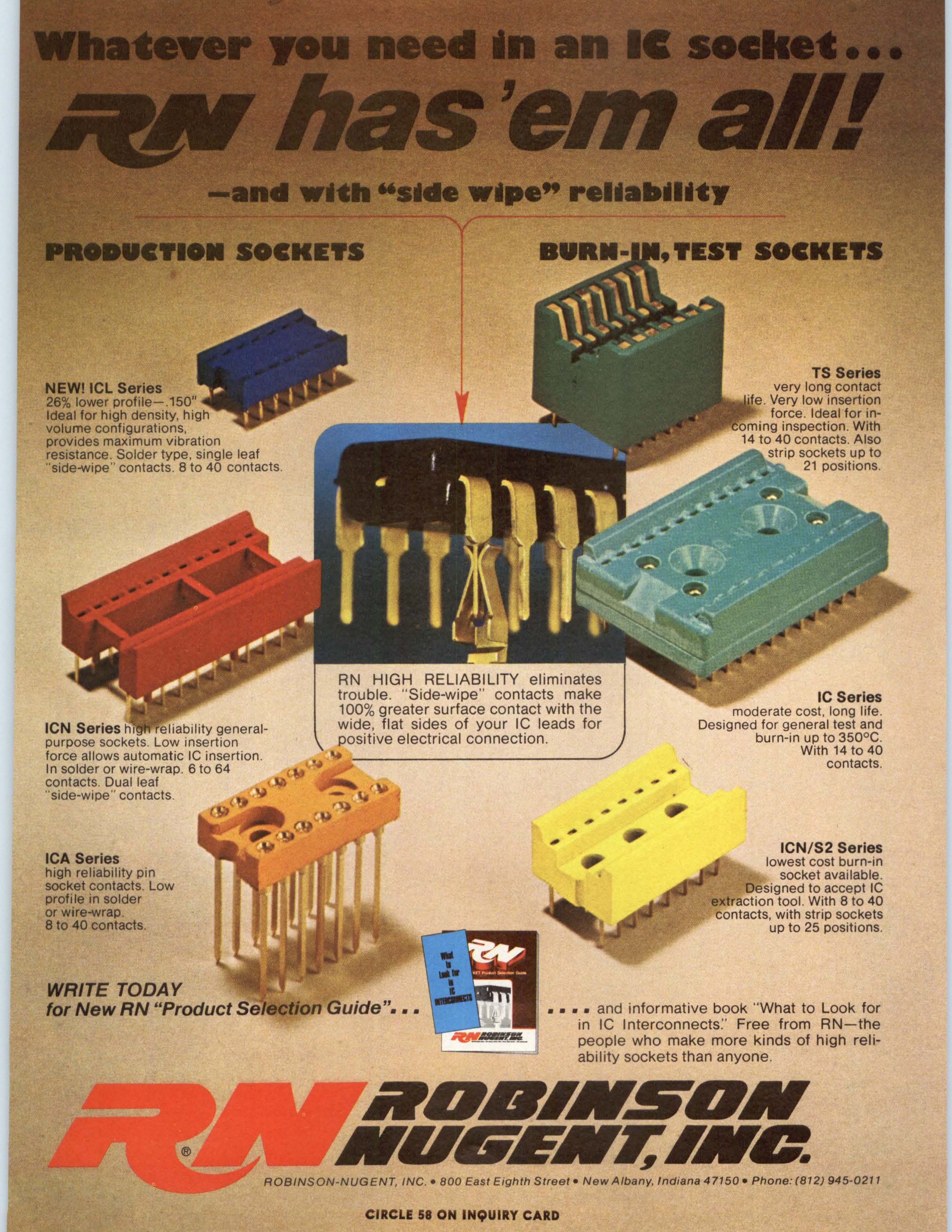
"System Operator Training, Today and in the Future," Max Anderson, University of Missouri

Session 22 — 2-4:30 pm

μP Applications in Instrumentation. How Smart is Smart?

Organizer/Chairman: Henry P. Hall, GenRad, Inc, Concord, Mass

Early microprocessor-based instruments received a lot of publicity. They used the microprocessor's power in several ways—



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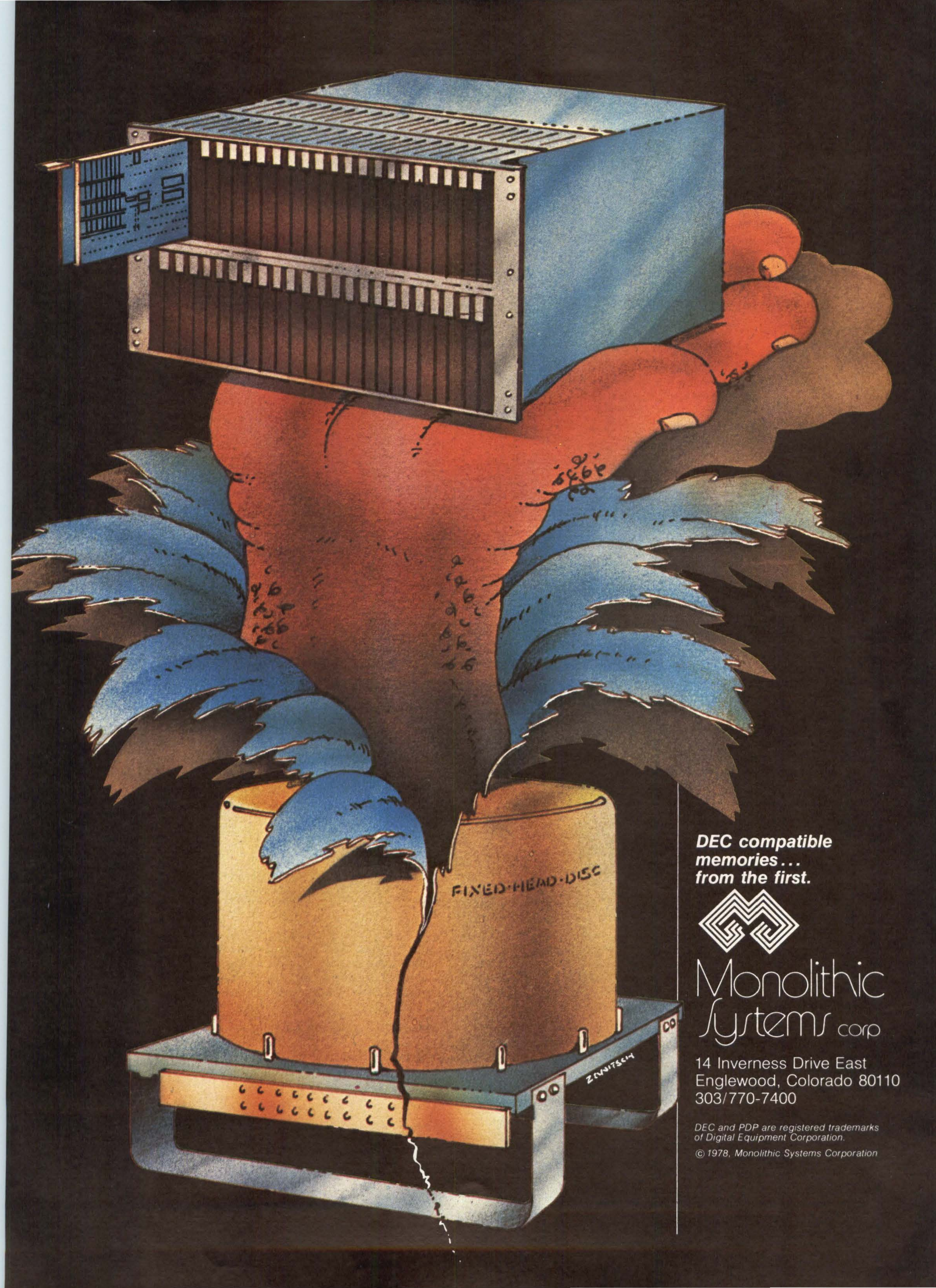
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simplifying the circuitry, giving better performance, and adding new features. Several "smart" analog instruments will be discussed in this session, showing how these instruments advantageously use the microprocessor.

"The Application of a Microprocessor to an Atomic Absorption Spectrophotometer," S. B. Smith and R. G. Schleicher, Instrumentation Laboratory, Inc

"A Microprocessor-Based 1-MHz Impedance Meter," W. F. Byers, H. P. Hall, and R. C. Sullivan, GenRad, Inc

"Dual-Slope A-D Conversion with a Microcomputer," John M. Lund, John Fluke Manufacturing Co

"An Automatic IEEE-Compatible Digitizing Oscilloscope Using Multiple-Microprocessor Techniques," Robert Bretl, Tektronix, Inc

Session 23 — 2-4:30 pm

Computer Graphics

Organizer: Ed Torerro, *IEEE Spectrum*, New York, NY
Chairman: Carl Machover, Machover Associates Corp, White Plains, NY

Highlighting recent advances in the field of computer graphics, this session reviews the progress of a decade, discusses the burgeoning field of digital television, presents a technique for automatically digitizing engineering drawings, and scans the important area of hardcopy output devices.

"Computer Graphics—A Decade of Progress," Carl Machover, Machover Associates Corp

"Digital TV Systems," Michael Neighbors, B-K Dynamics

"Automatic Digitizing of Engineering Drawings," Norman Altman, Altman Associates Inc

"Digital Hardcopy Techniques," Alan J. Dawes, Versatec, a Xerox Co

Thursday Morning

Session 26 — 10 am-12:30 pm

Microprocessors as Manufacturing Support Tools

Organizer/Chairman: John Trombly, Hewlett-Packard Co, Andover, Mass

Microprocessor benefits include cost effectiveness, fewer human errors, better control, and more efficient use of labor. This session will include papers discussing various approaches to hardware and software development, including cost and performance of a microprocessor-based test system. Microprocessor functioning in test, diagnostic, and inventory control will also be discussed.

"Microprocessors in Manufacturing—An Overview," John E. Trombly, Hewlett-Packard Co

"Microprocessor-Based Test Stations," John Lang and Pablo Roth, Analog Devices Inc

"Microcomputers on the Production Floor," Laurie Barber, Digital Equipment Corp

"Using Microprocessors in Test, Diagnostic, and Inventory Control," Don Kesner, Motorola Semiconductor Products

Session 27 — 10 am-12:30 pm

New Generation Memory Devices: Their Technology and Applications

Organizer/Chairman: Sam Young, Mostek Corp, Carrollton, Tex

In the past, IC memories were targeted at mainframe applications to displace core. Recent cost and product breakthroughs have opened up many new markets; new technologies and products are leading manufacturers into broader market areas. This session will discuss major technologies, including present and future products and applications.

"The Impact of VMOS on Semiconductor Memories," Chris Peterson, American Microsystems, Inc

"Applying the New Bipolar RAMS," Tom Goodman, Fairchild Semiconductors

"New Generation Memory Devices," Ward Parkinson, Mostek Corp

"Charge-Coupled Device Memories," Kirk F. MacKenzie, Intel Corp

"Bubble Memories," Bill Mavity, Rockwell International Corp

Thursday Afternoon

Session 31 — 2-4:30 pm

Latest Techniques and Design for Solid-State Communication

Organizer/Chairman: Lewis G. McCoy, American Radio Relay League, Newington, Conn

Many developments in the field of solid-state and communications have not been covered at recent conferences. The session will present the latest techniques used with vertical MOSFETS for high frequency applications in communications; and the use of solid-state solar-electric cells in practical applications for communications will be discussed.

"High Frequency VMOS Power Transistors Come of Age," Ed Oxner, Siliconix, Inc

"Modern IC Applications in Communications Systems," M. V. Hoover, RCA Solid State Div

"Low Cost Microwave," Dana W. Atchley, Microwave Associates, Inc

"Solar Electric Power," Doug DeMaw, American Radio Relay League, Inc

Session 32 — 2-4:30 pm

Minis and Micros—Convergence on the Same Market

Organizer/Chairman: Bryan Knox, Mostek Corp, Carrollton, Tex

The semiconductor industry is introducing more 8- and 16-bit machines with fully integrated system logic elements and software support. The minicomputer industry, however, is capitalizing on present architectures by partially integrating computing elements of existing minis. This session will deal with the extent of market overlap, as a function of technological advantages/disadvantages.

"Minis vs Micros: Tradeoffs and Considerations," Bob Reynolds, Zilog Inc

"Modular Solutions to Complex Problems," Wayne Garten, Intel Corp

"Micros vs Minis: Are They Really Converging on the Same Markets?" Jack McKeen, Digital Equipment Corp

"Micro/Mini System Tradeoffs and Market Segments," Ed Zander, Data General Corp

Session 35 — 2-4:30 pm

Industrial Applications of Optical Communications

Organizer/Chairman: David Medved, Meret Inc, Santa Monica, Calif

This session will emphasize current uses of short-haul, ruggedized fiber-optic, and free space systems for transmission of high speed digital or analog data in high EMI environments. It will also cover industrial and practical applications of optical data communications systems, and problems encountered in field testing and siting.

"Geophysical Measurements Using Fiber Optics," J. Van Der Laan, Roger S. Vickers, and Robert Morgan, Stanford Research International

"Fiber Optics Video Systems," F. Daby and R. Chesler, Times Wire & Cable Co

"Free Space Optical Data Links," R. Gray, Meret, Inc

"Optical Waveguide Subsystem Design and Component Selection," A. Fairzal and E. Loytty, Siecor Optical Cables, Inc

"Practical Applications in Fiber Optics," R. Anderson, Galileo Electro Optics

"Fiber Optics in Harsh Environments," N. Marshall and D. Thomas, Hughes Research Laboratory □

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AYDIN CONTROLS' new Model 5217 Keyboard Generator has it all in the case—dual asynchronous RS232C interface (to 25K Baud), power supply, a complete single channel display generator and of course the keyboard!

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The Model 5217 low cost keyboard generator, is software compatible with AYDIN CONTROLS' high communications speed (up to 600K bytes/sec.) multi-channel Model 5215 color graphics display generator. Now you have a choice—the 5217 for small systems and remote applications or the 5215 for large system applications.

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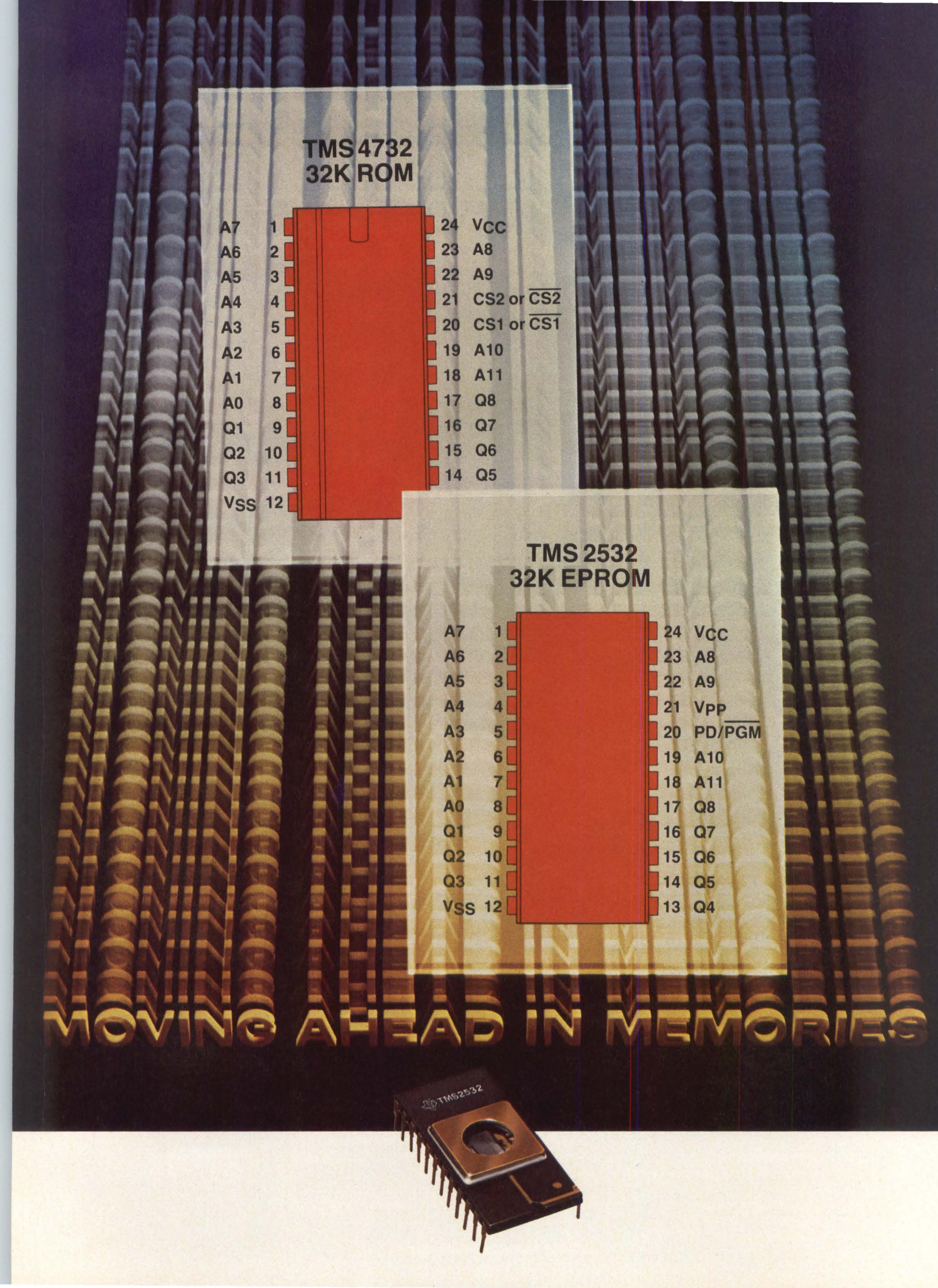


TMS 4732
32K ROM
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q1 9
Q2 10
Q3 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 CS2 or $\overline{CS2}$
20 CS1 or $\overline{CS1}$
19 A10
18 A11
17 Q8
16 Q7
15 Q6
14 Q5
TMS 2532
32K EPROM
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q1 9
Q2 10
Q3 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 V_{PP}
20 PD/$\overline{PGM}$
19 A10
18 A11
17 Q8
16 Q7
15 Q6
14 Q5
13 Q4
MOVING AHEAD IN MEMORIES
TMS2532

Introducing the first 32K EPROM.

Single 5-volt supply. Fully static. Biggest ever. From Texas Instruments.

Four 8Ks in a single 24-pin package. Or two 16Ks. TI's new TMS 2532 – a 32K 5-volt EPROM (erasable programmable read-only memory). The first and the biggest of its kind.

With applications now demanding more and more memory in the same size space, the new TMS 2532 is both practical and economical. Because TI offers a plug-in 32K ROM for volume production. Because system upgrading is a snap – the TMS 2532 is pin-compatible with 8K and 16K 5-volt models.

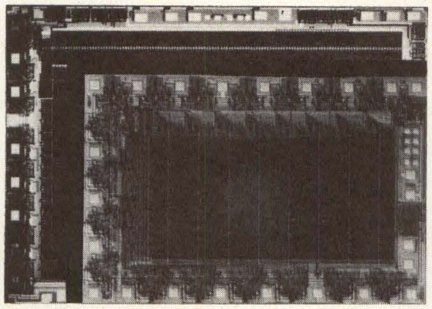
In addition, there is less assembly cost. Greater board density. Improved reliability. And, the TMS 2532 is a dollar saver compared to 8Ks and 16Ks.

Easy programming

Designed for facilitating rapid program changes in high-density, fixed-memory applications, the new TMS 2532 features speedy programming. A single TTL level pulse is all that's needed for simple in-system programming.

Any location can be programmed in any order. Either individually, in blocks, or at random. Which cuts programming time to a minimum. Existing EPROM programmers can do the job.

Erasing is simple, too. All you do is just expose the chip to high intensity ultra-violet light through the quartz window exactly as you would with any other EPROM.



***MORE MEMORY CAPACITY** results from state-of-the-art design techniques that keep the TMS 2532 EPROM chip only slightly larger than an 8K chip (foreground).*

Fully static operation

Like all EPROMs from TI, the new TMS 2532 continues the fully static tradition that makes designing much easier. There are no clocks. No timing signals. No hassles. Cycle time equals access time.

Low-power operation

The TMS 2532 also sets new standards in energy saving. At 840 mW maximum power (worst case – $T_A = 0°C$), it uses less power than a 2708. Yet has four times the memory capacity. And when the TMS 2532 is deselected, it automatically assumes a low power mode – 50 mW typical.

Matching 32K ROM

When programming is finalized and you're set for volume production, you can readily switch over to TI's TMS 4732, a 32K mask-programmable, production-proven read-only memory.

It's a direct plug-in for the TMS 2532. Note on the illustration that they utilize practically identical pin configurations. In fact, when you order the TMS 4732, merely specify that Pin 20 be active low ($\overline{CS1}$) and Pin 21 be active high (CS2) to achieve plug-in compatibility.

Wide-choice EPROM family

With the addition of the TMS 2532, TI now offers you a broad selection of compatible EPROMs. All available in 24-pin packages. All having speeds of 450 ns. All sharing the same production-proven N-channel process. All having the same basic pin configuration. Which paves the way for increasing memory capacity in the future should your needs so dictate.

This wide-choice EPROM family includes the 8K TMS 2708, the low-power 8K TMS 27L08, and the cost-effective 16K TMS 2716 (see table below). And more members are on the way.

For additional information on the first 32K EPROM, as well as on other family members, write Texas Instruments Incorporated, P. O. Box 1443, M/S 669, Houston, Texas 77001.

TI's Growing EPROM Family

Device	Complexity	Organization	Operating Supplies	No. of Pins
TMS 2708	8K	1K x 8	+12 V, ±5 V	24
TMS 27L08	8K	1K x 8	+12 V, ±5 V	24
TMS 2716	16K	2K x 8	+12 V, ±5 V	24
TMS 2532	32K	4K x 8	+5 V	24

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CIRCLE 61 ON INQUIRY CARD

Mini/Micro 78

April 18-20

Civic Center
Philadelphia, Pennsylvania

Over a half mile of product displays and an array of mini/microcomputer systems, peripherals, and industry services will be presented at the Mini/Micro Computer Conference and Exposition to be held at the Philadelphia Civic Center. All 24 conference sessions will take place in meeting rooms near the exposition floor. Each will end with an informal interchange between session speakers and attendees on topics including microcomputer software development, distributed processing, troubleshooting, computer graphics, microcomputers and the energy crisis, and small business systems and users.

In addition to the regular sessions there will be two special seminars entitled "Mini/Microcomputer Applications" and "Step-by-Step Design of Microprocessor Systems," respectively. The first will take place on Monday, April 17 at The Holiday Inn. Sponsored by the Institute of Electrical and Electronics Engineers (IEEE), this applications course will build a knowledge of basic hardware configurations, memory systems, I/O schemes, and debugging methods. The course will emphasize microcomputer applications and the hardware and software development processes. The second, sponsored by the International Society for Mini and Microcomputers (ISMM), will take place on Wednesday, April 19 in the Civic Center. The aim of this course will be to expose participants to step-by-step procedures for the design and implementation of microprocessor systems using wait/go, test-and-go, interrupts, and direct memory access as modes of operation.

Advanced registration fee for Mini/Micro '78, including all three days of the conference and show, is $60 ($75 at the door). One-day conference and show price is $25; one-day show-only price is $5. The IEEE-sponsored seminar will require an advance fee of $70 (members), $85 (nonmembers), and $30 (students). At the door, fees will be $85, $105, and $35, respectively. The ISMM seminar will be priced at $40 (advance) or $50 (at the door). Further inquiries concerning the Mini/Micro Computer Conference and Exposition should be sent to 5528 E La Palma Ave, Suite 1, Anaheim, CA 92807, or call (714) 528-2400.

The following program is limited to information available at press time. Only sessions of particular interest to *Computer Design* readers are covered.

Technical Program Excerpts

Tuesday Morning

Session 3 — 9:30 am-12 noon

Microcomputer Software Development: Choosing Among the Different Methods

Organizer/Chairperson: Carol Anne Ogdin, Software Technique, Inc

Session 4 — 9:30 am-12 noon

Distributed Processing

Organizer/Chairman: Roger Billings, Billings Computer Corp

Tuesday Afternoon

Session 5 — 1:30-4 pm

Small Business Systems

Organizer/Chairman: Don Schnitter, Basic/Four Corp

Session 6 — 1:30-4 pm

Philosophy of Computer Network Troubleshooting

Organizer/Chairman: Frank Urban, Hewlett-Packard Co

Session 7 — 1:30-4 pm

16-Bit Microcomputers

Organizer/Chairman: Edward J. Zander, Data General Corp

Session 8 — 1:30-4 pm

Design Approaches to Selecting Prefabricated Packages

Organizer/Chairman: George Benoit, Zero Corp

Wednesday Morning

Session 9 — 9:30 am-12 noon

Industrial Microcomputer Networks: Fact or Fiction

Organizer/Chairman: Dwight Carlson, Process Computer Systems

Session 10 — 9:30 am-12 noon

Minicomputer Application Languages

Organizer/Chairman: Michael Lebeda, Computer Automation Inc

Session 11 — 9:30 am-12 noon

Assessing the Economic Feasibility of Minicomputers: Business, Tax, and Financial Considerations

Organizer/Chairman: John Daley, Arthur Young & Co

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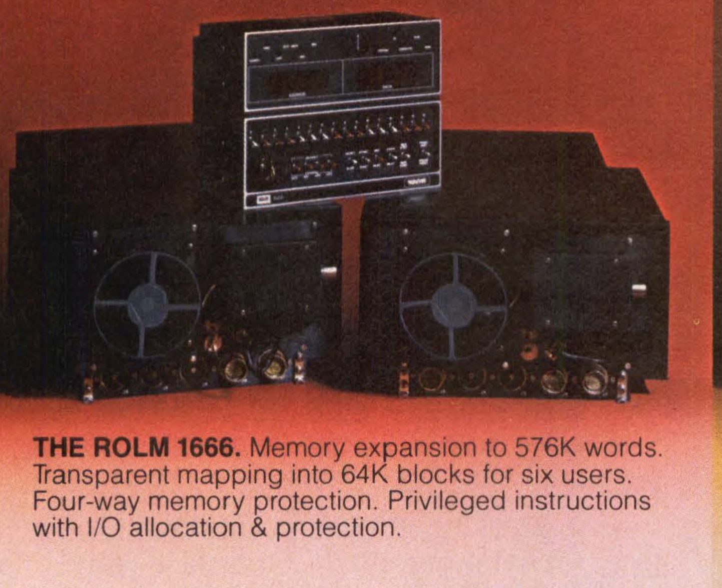

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8278/8279 Programmable Keyboard/Display Interfaces. Keyboard/sensor array input scan, and output scan for LED, incandescent and other displays. 128-key or 64-key input.

8251A Programmable Communications Interface. Industry standard USART for synchronous or asynchronous serial data transmission, including bisync.

8253 Programmable Interval Timer. Contains three independent 16-bit counters, programmable modes from dc to 2MHz.

8255A Programmable Peripheral Interface. General purpose I/O interface with 24 individually programmable I/O pins.

8257 Programmable DMA Controller. Provides four-channel, high speed direct memory access independent of CPU.

8259 Programmable Interrupt Controller. Handles eight levels of vectored priority interrupt. Expandable to 64 levels.

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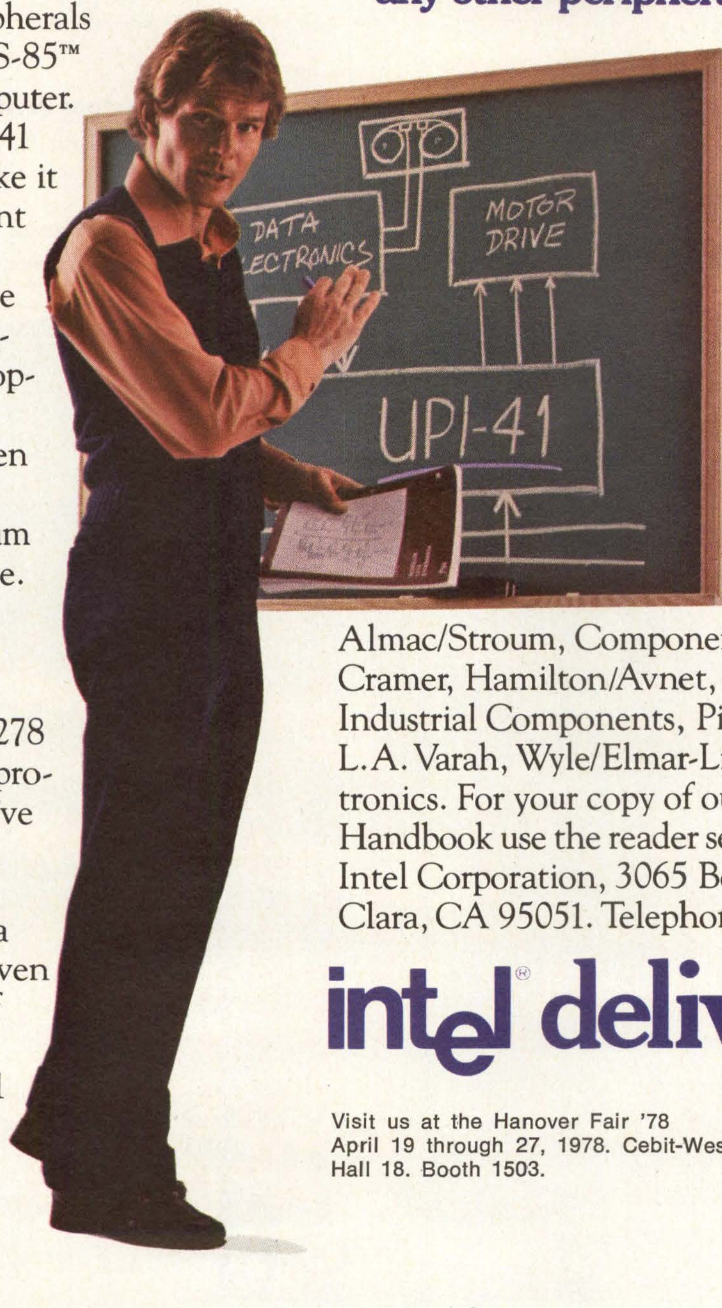
Because UPI-41 is a microcomputer, we've given it the same high level of support we give all our microcomputers. UPI-41 is supported by our Prompt™ 48 Design Aid, the Intellec® microcomputer development system with resident UPI-41/MCS-48 Macro Assembler. Plus applications assistance worldwide, full documentation, training classes, design seminars and a rapidly expanding users' software library.

"And, for my special I/O requirements, Intel's UPI-41 Universal Peripheral Interface is user programmable to control nearly any other peripheral device."



Intel's peripheral components, and the MCS-80, -85 and -48 microcomputers they support, are available through: Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey Electronics, Industrial Components, Pioneer, Sheridan, L.A. Varah, Wyle/Elmar-Liberty and Zentronics. For your copy of our Peripheral Data Handbook use the reader service card or write: Intel Corporation, 3065 Bowers Ave., Santa Clara, CA 95051. Telephone: (408) 987-8080.

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Session 12 — 9:30 am-12 noon

Criteria Used in Selecting and Evaluating a Minicomputer

Organizer/Chairman: John P. Gallager, A. O. Smith Corp

Wednesday Afternoon

Session 13 — 1:30-4 pm

Microcomputers and the Energy Crisis

Organizer/Chairman: Al Vitale, Control Logic Corp

Session 15 — 1:30-4 pm

The Microcomputer Software Crisis

Organizer/Chairman: Andrew A. Allison, Consultant

Session 16 — 1:30-4 pm

Computer Graphics With Minis/Micros

Organizer/Chairman: Carl Machover, Carl Machover Associates, Inc

Thursday Morning

Session 17 — 9:30 am-12 noon

The Emerging Role of the Microprocessor in Material Handling

Organizer/Chairman: John M. Hill, Computer Identics Corp

Session 18 — 9:30 am-12 noon

Alternative Minicomputer System Architectures

Organizer/Chairman: Malcolm Stiefel, Mitre Corp

Session 20 — 9:30 am-12 noon

Small Disc Memory Trends

Organizer/Chairman: Robert Hagen, California Computer Products, Inc

Thursday Afternoon

Session 21 — 1:30-4 pm

Mini/Micro Interface Testing

Organizer/Chairman: Frank Urban, Hewlett-Packard Co

Session 22 — 1:30-4 pm

Fixed Disc Technology Files Vs Removable Disc Technology Files

Organizer/Chairman: Bud Bleiniger, Microdata Corp

Session 23 — 1:30-4 pm

Micro-Based Custom Terminals and Systems

Organizer/Chairman: Martin S. Albert, Custom Terminals Corp

Session 24 — 1:30-4 pm

New Directions for Small Systems Users

Organizer/Chairman: Ed Bride, Hewlett-Packard Co □

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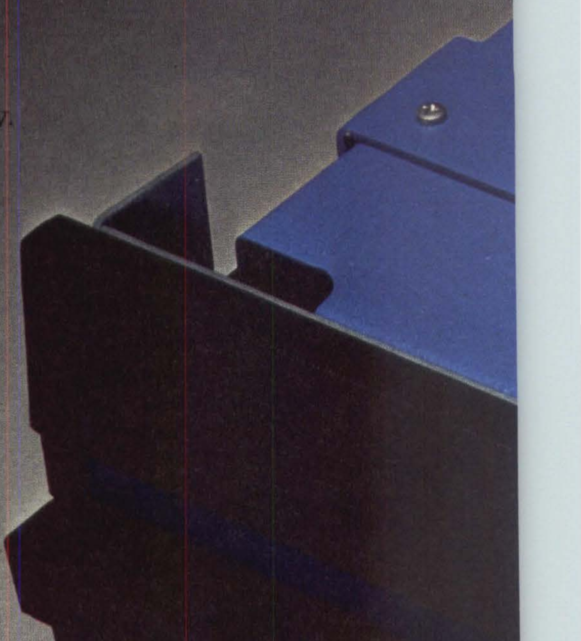

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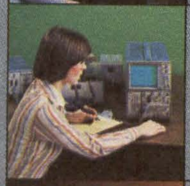

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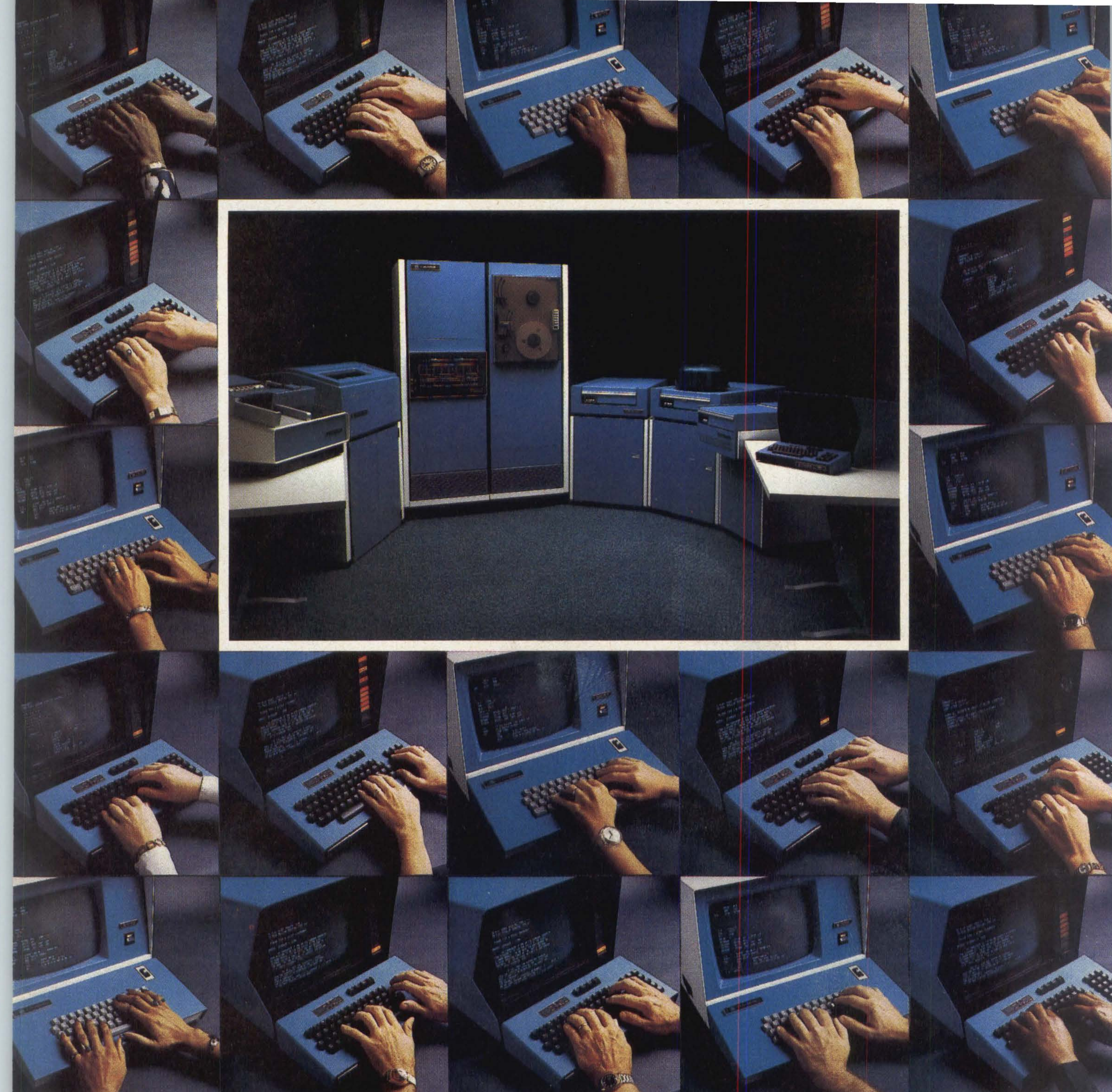

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CURRENT SEMICONDUCTOR MEMORIES

Increasingly rapid improvements in density, storage, and fabrication of semiconductor memories confront the designer with an everchanging spectrum of products and capabilities. A comprehensive overview of various technology options assures reliable, efficient, and cost-effective memory implementations

Eugene R. Hnatek Monolithic Memories, Incorporated, Sunnyvale, California

The advent of the 4k dynamic metal-oxide semiconductor random-access memory resulted in the adoption and proliferation of semiconductor memories in lieu of ferrite core for bulk storage applications. This choice was based on device reliability, performance, and cost, and the potential for further dramatic price reduction. Additionally, the microprocessor has provided a spur to increased usage of semiconductor memories. In fact, industry experts predict that the total dollars spent on semiconductor memories in the form of programmable read-only memory, read-only memory, electrically programmable read-only memory, and static and dynamic read-write random access memory will be eight times that spent on microprocessors during 1978.

Differing system applications have spawned various categories of semiconductor memories, each with peculiar advantages and disadvantages, and thus have exerted a major influence on end-system configuration and performance. Until recently, most system designers have devoted their design efforts almost entirely to microprocessors—with cursory attention to add-on memory. Today, semiconductor memories offer a multitude of capabilities and costs; thus, the choice of memory is critical to overall computer system performance.

Different categories of semiconductor memories and specific data storage applications where they find primary use provide system designers a wide range of options. In general, metal-oxide semiconductor (MOS) electrically programmable read-only memories (EPROMs) and dynamic random-access memories (RAMs) are extensively used in micro and minicomputer applications, while the slow electrically alterable read-only memories (EAROMs) are more suited to peripherals, at present. In addition, dense dynamic MOS RAMs are used in large volume in small and large mainframe computers for bulk storage. Bipolar programmable read-only memories (p/ROMs) provide high speed microprogram capability to microcomputers, minicomputers, peripherals, and small and large mainframe computers. Bipolar RAMs are used as scratchpad and file memories in minicomputers and small and large mainframe computers. The most recent category of memory that is receiving considerable attention is the MOS static RAM, which is challenging the bipolar RAM from performance and cost viewpoints both in buffer and cache applications and in microcomputer and peripheral applications. Magnetic bubble memory, charge-coupled device (CCD) memory, and high density (32k and 64k) MOS ROMs find extensive applications as tape, disc, and drum memory replacements.

Memory Technology Background

Clearly, integrated circuit (IC) technology has made the semiconductor memory a viable product. Literally thousands of cells, each consisting of one or more transistors, plus resistors or capacitors, and in some cases diodes, can be placed on a single chip along with driving and decoding circuits. Some technologies make it easier and cheaper to form additional transistors in the cell than others, but transistors occupy area and consume power. A complex cell may take more time to react than a simple cell; therefore, tradeoffs are involved.

Discussion of the relative merits of semiconductor memories centers on packaging density (maximizing the number of bits or cells per chip), speed of the memory system in terms of access time (the faster the speed, the shorter the access time), and cost per bit of storage. Usage confusion results from the existence of many different memory categories. Imprecise and misleading terminology further confounds the problem. Not only are the acronyms intimidating, but also, they are inconsistently applied. Three separate categories—read-write scheme, permanence of data entered, and process technology—are discussed here to diminish the confusion.

A prime distinction between memories is the manner in which information is stored (written) and accessed (read). Random-access memories involve column and row matrices which allow information to be stored in any cell and accessed in approximately the same time. By contrast, "serial access" means that information is stored in column order, and access time depends on where the desired bit is with respect to the sensing station.

Shift registers are examples of serial-access memories. On a larger scale, CCDs and magnetic bubble memories are types of shift registers that are gaining in popularity for low speed applications. They are not, however, based on transistor-cell configurations.

Permanence of information entered is indicated by the designations read-write memory and read-only memory. A read-write memory permits data to be entered or read out at any time. In contrast, a ROM may have data entered either permanently or semipermanently, mainly for readout purposes. Thus, in ROMs a permanent program is fixed or unchangeable, while a semipermanent program is reversible and may be changed.

As for process technology, memories employ the same manufacturing processes and variations as digital logic systems. These include the bipolar technologies—transistor-to-transistor logic (TTL), emitter-coupled logic (ECL), and such variations as Schottky TTL and integrated injection logic (IIL)—and the MOS technologies—p-channel MOS (p-MOS), n-channel MOS (n-MOS), and complementary MOS (CMOS). Performance qualities that distinguish products built in each of these technologies (see Semiconductor Process Technology Summary) carry over to their applications in memory devices. Technologies that permit fast logic also permit fast memories; those that permit high density logic permit high density memories, and those that permit low power-consuming logic permit low power-consuming memories. Accordingly, there is a direct carryover of principal characteristics from logic medium- and large-scale integration (MSI and LSI) to memory products. Memories and logic fabricated by the same process are also easiest to interface because of similarity of electrical characteristics.

Speed-power product (SPP) tradeoffs exist for memories just as they do for logic families. The fastest memories are bipolar ECL and Schottky TTL devices. Such devices have access times of about 5 to 100 ns; however, power consumption tends to be higher. MOS memories have access times that overlap those of bipolar devices (from about 80 ns to 5 μs), but power drain is generally lower and regulation is less critical. Presently, most semiconductor memories have shifted from p-MOS to n-MOS because of increased speed and packing density. CMOS devices have lower power consumption, but are more expensive.

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Mixes speed of bipolar with packing density of MOS

*Excerpted from *A User's Handbook of Semiconductor Memories* by E. R. Hnatek, with permission of the publisher, John Wiley & Sons, Inc, New York, NY

Obviously static and dynamic memory cells differ. Static memories are internally regenerative. They are designed to protect against false or ambiguous operation. Conversely, dynamic memories require refreshing at periodic intervals but cost less, are simpler, and need less silicon area. Moreover, less standby power is required.

Important, but confusing, distinctions exist in the ROM class. These memories are set to yield the same output at all times unless altered to change the data placed within them. The term ROM generally refers to a memory programmed during a final mask step as part of the factory fabrication process. Factory programmed ROMs are likely to function as decoders, translators, or even as libraries of universal or standard data. Factory programming is most economical if medium to large quantities of memories with set patterns are desired, and if the circuit design is fixed. Where programs are subject to change or engineering alteration, however, some form of programmable ROM (p/ROM) may be used. In these devices permanent changes in the cell interconnects are produced either by electrically destroying or "burning out" fusible metal links or by deforming a transistor junction with an overvoltage.

Bipolar p/ROMs

The majority of bipolar or fusible-link p/ROMs use Schottky TTL technology to achieve address access times (T_{AA}) of 30 to 90 ns (max), depending on memory size and organization, typically 32 to 2048 words in either 4- or 8-bit formats. Power supply currents (I_{cc}) range from 65 to 180 mA (max).

p/ROMs with both open-collector and 3-state outputs are readily available. The 3-state output offers two major advantages over open-collector types. First is that a low impedance driver is available for driving capacitance on the memory output, resulting in faster low to high transition. Second is that no pullup resistor is required.

Differences in bipolar p/ROMs occur in fusing technology and methods for programming p/ROMs. Fusible materials in widespread use are nichrome, polysilicon, and titanium-tungsten. Nichrome-fused p/ROMs have been proven reliable, and are well understood, but use high voltage programming techniques; polysilicon-fused p/ROMs utilize low voltage programming techniques. While titanium-tungsten fuses provide high speed p/ROMs with low programming voltages (high reliability), they do not have high usage history. The type of fuse selected by the system designer depends upon the method of programming, which is very important, and documented reliability.

Once programmed, bipolar p/ROMs cannot be changed. Thus, they provide nonvolatile/nonalterable storage and are useful for prototype systems. Many bipolar p/ROMs are completely interchangeable (electrically and pin compatible) with an equivalent ROM. In addition, there is upward compatibility of devices, ie, the ability to replace a 512 x 8-bit 24-pin p/ROM with a 1k x 8-bit 24-pin p/ROM using the same socket and without redesigning the printed circuit (PC) board. This upward compatibility exists for other devices as well.

Bipolar p/ROMs are high speed devices, and are incorporated in systems using high performance microprocessors, such as the Z80, where it is not feasible to use slow speed MOS memories that require the CPU to wait for the memory. Some bipolar p/ROMs are designed to replace an MOS equivalent product; the MMI 6385 and Signetics 82S2708 are direct, high speed, bipolar equivalents to the popular Intel 2708 MOS EPROM. Other bipolar p/ROMs are pin-compatible with static MOS RAMs, such as the MMI 6353, Intel 2114, and TI TMS4045 for use as writable control stores in microprocessor-based equipment. However, differences occur in power dissipation—especially since the 2114 and 4045 can be operated in a power-down (low power dissipation) mode, but the 6353 cannot—as well as in speed of operation. Interchangeability among these three memories provides the designer with flexibility and with ability to change from an essentially fixed program device (p/ROM) to a read-write memory device (static RAM) without a major PC board redesign.

Today's state-of-the-art in density for bipolar p/ROMs is 8192 bits, organized as 1024 x 8-bit and 2048 x 4-bit words. In the near-term future, 16,384-bit p/ROMs should become available in 2048 x 8-bit and 4096 x 4-bit organizations. Two performance areas are being stressed: high speed [low address access time (T_{AA})] and low power dissipation. Since these two characteristics cannot be obtained concurrently, several versions of the same organizations will exist—a speed enhanced version and a low power consumption version—all with both open-collector and 3-state outputs. In addition, power switched and synchronous and asynchronous registered p/ROMs will soon be available in both Schottky TTL and low power Schottky TTL technologies.

Although bipolar p/ROMs traditionally have been used for programming writable control stores, this situation will change in the near-term future. MOS ROMs and p/ROMs will become available and will impact this market. One such device, the Mostek 120-ns, 150-mW 64k MOS ROM, which should have a T_{AA} of 80 ns, should be available by 1980.

Bipolar ROMs

Bipolar ROMs are available with speeds of from 25 to 40 ns and with capacities up to 16,384 bits (Table 1). Work on 32k and 64k density storage devices is in process.

Bipolar ROMs duplicate MOS ROMs in (1) memory cell array, (2) X address decode or row select circuitry, and (3) Y address or column select circuitry. Output drivers are used to provide the degree of output drive desired for off-chip load circuits. Since bipolar devices have much lower impedance than MOS, more drive capability is required throughout the bipolar ROM circuitry. An input buffer inverter should be fast and capable of driving the multiple row-select gates.

Bipolar ROMs are fabricated using Schottky TTL technology to obtain low access times and low power requirements. By eliminating the programming circuitry, smaller die size and higher reliability monolithic

TABLE 1
Typical Commercially Available Bipolar ROMs

Organization	Part Number*	T_{AA} max	I_{CC} max
32 x 8 bits	6230/6231-1	50 ns	125 mA
256 x 4 bits	82S226/82S229 6200/6201-1 93457/93467	45 ns	125 mA
256 x 8 bits	82S214	60 ns	175 mA
512 x 4 bits	82S230/82S231 6205/6206-1 93431/93441	70 ns 60 ns	135 mA 130 mA
512 x 8 bits	82S215 6240/6241-1 93432/93442	90 ns	170 mA
1024 x 4 bits	6250/6251-1 6252/6253-1 8228	60 ns 60 ns 70 ns	175 mA 175 mA
1024 x 8 bits	82S280/82S281 6280/6281-1 6282/6283-1	100 ns	170/180 mA
	6282/6283-2 6280/6281-2	55 ns	170 mA
	93454/93464	45 ns	170 mA
1024 x 9 bits	6260/6261-1	100 ns	165/175 mA
1024 x 10 bits	6255/6256-1	100 ns	165/175 mA
2048 x 8 bits	6275/6276-1	110 ns	190 mA

*62XX—Monolithic Memories, 82SXXX—Signetics, 934XX—Fairchild

devices are obtained. These ROMs offer a low cost solution to program memory for high volume usage. A major deterent to their use, however, is their inflexibility to change. This precludes their use in prototype or very low production quantity systems. As mentioned before, bipolar ROMs that are interchangeable with bipolar p/ROMs are available.

MOS EPROMs

The MOS EPROM is both field programmable and reprogrammable. Some typical commercially available EPROMs (Table 2) use floating gate avalanche injection MOS (FAMOS), although other EPROMs use metal alumina dielectric oxide semiconductor (MAOS) gates. "Floating" refers to the fact that the gate of each transistor is left unconnected, or electrically floating in an insulating layer of silicon dioxide. MOS EPROMs are typically five to ten times slower than bipolar types; they need multiple power supplies for operation (with the exception of the single supply Intel 2716) and are volatile to the extent that sunlight or fluorescent lighting can cause charge loss and thus erasure. These disadvantages are offset in many applications by their flexibility (field programming) and low cost. They can be programmed for a certain content, used, and then reprogrammed with a different content. Thus, they are ideal for prototype product development and applications with constantly changing data requirements.

Reprogramming capability is gained by use of a trapped electronic charge technique for programming, instead of the destruction of a fusing element as in bipolar memories. Application of a high voltage across the transistor causes a "tunneling" of high energy carriers that open a conducting channel. However, exposure of the chip for several minutes to an intense, low frequency ultraviolet light source reverses the process and returns the gate to its floating state. The device may be reprogrammed and erased indefinitely. Erasure must be performed properly to ensure programmability and to avoid dropping bits with age and temperature. There are no reprogrammable bipolar EPROMs in existence today because the trapped charge technique cannot be implemented easily in bipolar technology.

The industry standard 2708 8k EPROM has been replaced by the 16k 2716, a state-of-the-art version from both TI and Intel, and the AMI S4216B VMOS version. Presently, TI is redesigning its 2708 pin-compatible ver-

TABLE 2

Typical Commercially Available MOS EPROMs (UV Type)

Vendor	Model No.	Interchangeable ROM	Size	Organization	Access Time (max)	Power Supply	Maximum Current (mA) Active	Standby
Intel	1702A	1302	2k	256 x 8	1 μs	5, −9 V	65	65
Intel	2704	—	4k	512 x 8	450 ns	12, ±5 V	65, 45, 10	65, 45, 10
Intel	2708	2308	8k	1024 x 8	450 ns	12, ±5 V	65, 45, 10	65, 45, 10
Intel	2716	2316E	16k	2048 x 8	450 ns	5 V	100	100
TI	2716*	—	16k	2048 x 8	450 ns	12, ±5 V	45, 17, 6	45, 17, 6
Intel	2732	2332	32k	4096 x 8	300 ns	5 V	40	15
TI	2532	4732	32k	4096 x 8	450 ns	5 V	168	10

*Interchangeable with Intel 2708, but being redesigned to be compatible with Intel 2716

TABLE 3

Typical Commercially Available n-MOS EAROMs

Vendor	Model No.	Organization	Max Access Time	Alterability
Nitron	NC7033	16 x 16	2 to 5 μs (serial)	—
Nitron	NC7035	16 x 18	2 to 5 μs (serial)	—
Nitron	NC7040	64 x 4	2 to 5 μs (parallel)	—
Nitron	NC7050	256 x 4	2 to 5 μs (parallel)	—
Nitron	NC7051	1024 x 1	2 to 5 μs (serial)	—
GI	ER1105	256 x 4	2 μs	Block
GI	ER1400	100 x 14	—	Word
GI	ER2050	32 x 16	6 μs	Word
GI	ER2401	1024 x 4	2 μs	Chip
GI	ER3401	1024 x 4	0.95 μs	Word
GI	ER2800	2048 x 4	2.6 μs	Chip

sion to be identical to the Intel 2716, which uses only one 5-V TTL supply rather than three. The recently introduced TI 2532 and Intel 2732 32k EPROMs are organized as 4k x 8 and operate from a single 5-V supply. A 64k unit should be appearing within the next 12 to 18 months. In addition Intersil offers a low power CMOS EPROM in two versions: 1k x 4 (6603) and 512 x 8 (6604), which are twice as fast as the n-MOS EPROM (200 ns).

n-MOS EAROMs

Electrically alterable n-MOS p/ROMs—or EAROMS (Table 3)—are useful in reduced power applications where data loss is intolerable, ie, in severe noise environments or where recurring power interruptions are likely to occur. Such EAROMs permit complete or selective writing of bits into either state. This means that the memory can be programmed electrically while it is still in the circuit and that alterations may be made without wiping out the remainder of the memory.

Nitride EAROMs are slow (with read times of 0.95 to 5 μs) for most realtime program storage applications and, at present, are costly. However, since they provide almost infinite store times, they are being used increasingly as auxiliary memory in applications where remote systems are inaccessible for routine field change, and in aerospace (satellite) systems.

MOS ROMs

High density MOS read-only memories (ROMs) of 32k and 64k bits are emerging as a critical member of the microprocessor chip set, expanding the instruction capacity of microprocessor-unit based systems and holding immediate promise for fixed programs in larger hierarchies. In addition, high density ROMs are generally viewed as the most cost-effective of all semiconductor memories and may well impact tape and disc storage.

New MOS p/ROMs will not be EPROMs; instead they will be more like the inexpensive Motorola MCM2708P, which is programmable only once, similar to a bipolar p/ROM. MOS EPROMs require high injection voltages, which cuts down on density and speed. However, the nonerasability capability will provide high density and speed with low programming voltages.

The next generation of microprocessors—perhaps 16-bit versions—will use ROM extensively for software storage. By 1980, 80-ns 64k ROMs and 256k MOS ROMs and p/ROMs are expected.

Bipolar RAMs

Bipolar TTL RAMs using oxide-isolation technology in combination with various processing techniques provide high density, high speed writable stores for buffer, cache, and scratchpad memory applications. Shallow and controlled ECL junctions provide even faster (7-ns) access times. Again, as with bipolar p/ROMs, with newer high speed microprocessors emerging, no longer can slow MOS RAMs be tolerated nor can various functions, such as refresh intervals, be buried in the microprocessor overhead without impairing system performance—high speed RAM is mandatory. At present, the Fairchild 93415A 1024 x 1-bit, 30-ns and 93412/93422 256 x 4-bit, 45-ns RAMs are dominant. They use an oxide-isolation technique to obtain greater chip density and faster operating speed (lower address access time, T_{AA}).

The transistorized flip-flop forms the bipolar RAM memory cell, resulting in ultrahigh speed performance, large die size (compared with MOS), higher power supply current (I_{cc}), and higher cost. However, the Fairchild 93481A 4k dynamic I^3L (isoplanar integrated injection logic) RAM represents the future technology trend. It has a die size of only 11,176 mil^2, which is much smaller than competitive 4k dynamic n-MOS memories, thereby providing more die per wafer, higher yield, and lower unit cost (even though more masks are required) than MOS devices. Its performance characteristics are superior to those of the latest 4096-bit dynamic MOS RAM, the MK4027, (100-ns T_{AA} for 93481A versus 150 ns for the MK4027-2, and 450-mW power dissipation versus 462 mW for the MK4027).

Static n-MOS and VMOS RAMs, however, are making a direct frontal attack on the domain of bipolar RAMs—

TABLE 4

Typical Bipolar RAMs

Organization	Part Number*	T_{AA} max	I_{cc} max
16 x 4 bits	6560/6561	35 ns	125 mA
	L6560/6561	80 ns	40 mA
	85S68**	40 ns	100 mA
	27S02A/S03A	25 ns	100 mA
	27LS02/LS03	55 ns	35 mA
256 x 1 bit	6530/6531	55 ns	130 mA
	L6530/6531	95 ns	75 mA
256 x 4 bits	93412/422	45 ns	155 mA
	93L412/L422	60 ns	80 mA
	74S207/208**	40 ns	120 mA
	74LS207/208**	75 ns	40 mA
1024 x 1 bit	93415A/25A	30 ns	135 mA
	93L415/L425	60 ns	65 mA
4096 x 1 bit	93470/71	55 ns	155 mA
	93481A	100 ns	100/9 mA
	74S400/401	75 ns	100 mA
	74LS400/401	150 ns	60 mA
16,384 x 1 bit	93483	100 ns	NA

* 65xx, L65xx—Monolithic Memories; 85Sxx—National Semiconductor; 27Sxxx, 27LSxxx—Advanced Micro Devices;—93xxx, 93Lxxx—Fairchild Semiconductor; 74Sxxx, 74LSxxx—Texas Instruments

**Edge triggered write

high speed cache and scratchpad applications. Devices, such as the Intel 2147, with a 70-ns T_{AA} and a deselected (standby) I_{cc} of 20 mA, and the AMI S4015 45-ns VMOS RAM should provide stiff competition and should push the performance level for a 4k MOS RAM to 35 ns by 1980. Table 4 summarizes the popular bipolar RAMs by memory organization, maximum access time, and power supply current. Bipolar RAMs are available with both open-collector and 3-state outputs.

Fairchild plans to introduce the 93483, a 16k bipolar RAM, that will occupy less than 25,000 mil^2, offer 100-ns maximum access time, and provide pin-compatibility with the 93481A 4k RAM. Later, the 93485 65k RAM is expected. VMOS 4k RAMs should push performance levels to 35 ns by 1980. However, ECL RAMs will lead in performance with 1k devices having 10-ns maximum T_{AA} and 1k x 4-bit and 4k x 1-bit devices having 25-ns maximum T_{AA}; these RAMs will be used with high speed computers. Cache and buffer memory applications will be taken over by MOS RAMs.

MOS RAMs

MOS RAMs are available in both static and dynamic varieties with access times that overlap those of bipolar RAMs and even rival those of bipolar RAMs (Intel 2115A, Intel 2147, AMI S4015), but with generally lower power drain. Dynamic MOS RAMs are used in peripheral and buffer applications, as well as in small and large mainframe computers. Both static and dynamic MOS RAMs are used in applications in which power is at a premium, such as battery-powered portable equipment and small terminals.

In static MOS RAM cells, information is stored on the bistable flip-flop (as with bipolar RAMs), whereas information is stored as an electrical charge on a capacitor of a single transistor cell for a dynamic MOS RAM. Static memories are internally regenerative; they are designed to protect against false or ambiguous operation and are faster than dynamic RAMs. Dynamic memories require refreshing at periodic intervals, but cost less, are simpler, and need less silicon real estate. Moreover, less standby power is required.

Dynamic 4k RAMs provide a cost-effective solution to main memory and data heavy (4k to 6k byte) applications. Initially, confusion existed because of the promulgation of three different package types and pinouts, as each IC vendor attempted to have its 4k RAM accepted as the industry standard. Further confusion was added when the focus changed from 4k RAMs to 16k dynamic RAMs before volume production of 4k units was achieved, and just as most designers were incorporating them.

The future trend in MOS RAMs will result in devices with higher speed and density, such as the NEC 65-ns 16k RAM. MOS RAMs are impacting high speed minicomputer applications and by 1980 will impact medium performance large computers by means of parallel processors. Cache and buffer memories will soon see 35-ns static 4k RAMs. In addition, 1k x 8-bit MOS RAMs will be pin-compatible with 2708 EPROMs for writable stores, and should achieve speeds of 80 ns soon, and 50 ns by 1980.

16k dynamic RAMs provide a further cost incentive for semiconductor main memory usage, with specifications comparable to those of 4k dynamic RAMs. Tables 5 and 6 summarize salient electrical characteristics of some popular 4k and 16k dynamic n-MOS RAMs, respectively. Since only primary sources are listed, the information does not provide comprehensive data for all available memories in that category, nor list second sources.

Static RAMs are vying with dynamic RAMs as design activity increases and product announcements proliferate. At present, static RAMs outperform their dynamic counterparts in terms of speed (access time) and power dissipation (by virtue of powerdown operation and/or dynamic clocking of the newer n-MOS RAMs), but they do not have the density of dynamic RAMs—8k (static) versus 16k (dynamic). Hitachi Research Labs has developed a 4k CMOS RAM that has 43-ns access time and power dissipation of less than 100 mW. Scaled high performance n-MOS and VMOS technologies are providing very high speed RAMs which are attacking the domain of bipolar RAMs—high speed cache and scratchpad appli-

TABLE 5

Typical Dynamic 4k n-MOS RAMs*

Vendor/Model No. / Parameter	22-pin Package						18-pin Package		16-pin Package	
	Intel 2107B	TI TMS4060	NEC μPD411	Motorola 6605	National 5280	Fujitsu 8215	TI TMS4050	National 5270	Mostek MK4096	Mostek MK4027
Access time (ns)	200	200	150	230	200	100	150	150	250	150
Read cycle time (ns)	400	400	380	350	400	220	400	400	375	325
Write cycle time (ns)	400	400	380	450	400	200	400	400	375	325
Read-modify-write cycle time (ns)	520	580	470	470	520	300	600	520	515	—
Power dissipation (mW)	600	585	775	465	465	380	420	280	441	440**
Power supplies (V)	12,±5	12,±5	12,±5	12,±5	12,±5	12,7,−5.2	12,0,−5	12,0,−5	12,±5	12,±5

Note: All devices come in various speed versions

*Excerpted from *A User's Handbook of Semiconductor Memories* by E. R. Hnatek, with permission of the publisher, John Wiley & Sons, Inc, New York, NY

**1.3 mW standby power

TABLE 6

Typical 16k Dynamic n-MOS RAMs*

Manufacturer	Intel	Texas Instruments	Mostek	Motorola
Part number	2116	TMS4070	MK4116	MCM6616
Access time (ns)	150/250/300/350	150/250/300/350	120/150/200	250/300/350
Read cycle time (ns)	375/425/500	550	375	375/425/500
Write cycle time (ns)	375/425/500	550	375	375/425/500
Read-modify-write cycle time (ns)	525/615/700	730	375	540/620/700
No. of refresh cycles	64/128 (three refresh modes)	128	128	128
Refresh time (ms)	2	2	2	2
Power supply voltages	12, ±5 V	12, ±5 V	12, ±5 V	12, ±5 V
Operating power (mW)	720	550	600	500
Number of pins	16	16	16	16
Outputs	Latched, 3-state, TTL compatible	Unlatched, 3-state, TTL compatible	Unlatched, 3-state, TTL compatible	Latched, 3-state, TTL compatible
Special operating conditions	Page mode operation	Full TTL compatibility on all inputs	Page mode operation	Data out concontrolled by column and strobe
Data I/O	On-chip latches, TTL compatible	On-chip latches, TTL compatible	On-chip latches TTL compatible	On-chip latches, TTL compatible, common I/O

*Excerpted from *A User's Handbook of Semiconductor Memories*

cations. The variety of new 4k static RAM products with a 256 x 4-bit organization (Table 7), and a 1k x 4-bit organization (Table 8) shows the results of increased design activity. 65k dynamic and 16k static RAMs can be fabricated using present photolithographic techniques as demonstrated by Nippon Telephone and Telegraph's announced 200-ns, 150-mW (10-mW standby) 65k MOS RAM (16k x 4), which uses a single level, polysilicon gate process with molybdenum interconnects. Prototype parts should be available within 12 to 18 months.

VMOS ROMs and RAMs

Designers are utilizing V-groove MOS (VMOS) technology to obtain high density and high performance in lower cost devices. VMOS is an n-channel MOS logic

TABLE 7

Typical 256 x 4-Bit Static RAMs*

Part No./ Manufacturer	Technology	Power Supplies	TTL I/O	Power Dissipation	Access Time (ns)	Cycle Time (ns)	DIL Package	3-state/ OR-tie	Notes
2101/Intel	Si-gate	5 V	Yes	150 mW typ	1000 max	1000 min	22-pin	Yes	Separate I/O via output disable
2111/Intel	Si-gate	5 V	Yes	150 mW typ	1000 max	1000 min	18-pin	Yes	Common I/O and output disable
MM2112/ National	Si-gate	5 V	Yes	150 mW typ	1000 max	850 to 1050 min	16-pin	Yes	Common data I/O
MM5269/ National	Si-gate	5 V	Yes	350 mW max	1000 max	1000 min	22-pin	Yes	Fully decoded with on-chip address and enable register
2606/ Signetics	Si-gate	5 V	Yes	200 mW	750 max	750 min	16-pin	Yes	Common data I/O
2606-1/ Signetics	Si-gate	5 V	Yes	200 mW	500 max	500 min	16-pin	Yes	Common data I/O
35L38/ Fairchild	Isoplanar	5 V	Yes	184 mW max	400 max	400 min	22-pin	Yes	Power-down standby mode, fully decoded
3538/ Fairchild	Isoplanar	5 V	Yes	350 mW max	350 max	350 min	22-pin	Yes	Fully decoded
TMS4039/TI	Si-gate	5 V	Yes	175 mW typ	1000 max	1000 min	22-pin	Yes	Fully decoded, 2-chip enable inputs for OR-tie
TMS4042/TI	Si-gate	5 V	Yes	175 mW typ	1000 max	1000 min	18-pin	Yes	Common I/O with output enable
7101/AMS	Si-gate	5 V	Yes	300 mW max	250	250	22-pin**	Yes	Data retention to 1.6 V
7040/AMS	Si-gate	5, 12 V	Yes		200 typ	350 typ	22-pin	Yes	Separate chip select, on-chip address, input latches
HM-6551/ Harris	CMOS	5 V	Yes	15 mW	215/375	335/585	22-pin	Yes	
HM-6561/ Harris	CMOS	5 V	Yes	15 mW	215/375	335/585	18-pin	Yes	
5101/Intel	Si-Gate CMOS	5 V	Yes	135 mW	650 max	650 min	22-pin	Yes	Separate data I/O

*Excerpted from *A User's Handbook of Semiconductor Memories*
**Also available in 16- and 18-pin versions

structure integrated on a 3-dimensional surface in which the transistor elements are arranged vertically up the sides of a V-groove. Device speed for a VMOS device is maximized by the short channel length. VMOS cell size can be the same width as the connector lines to it, rather than larger, as in n-MOS. Net result is a considerable increase in circuit density over both standard n-MOS and bipolar technologies. VMOS can easily provide more circuitry for a given chip area, or a smaller chip area for a given circuit. Its density is increased because the n+ substrate also serves as the common source for all transistors, thereby eliminating the ground "lines" required on n-MOS circuits. The saving in surface area is consequently substantial. Circuit density on such a chip exceeds that from any competing technology available or projected, primarily because of the additional vertical dimension. Using VMOS, for example, the AMI S4264, a 65k ROM on a 28,000 mil^2 chip, has been achieved. In addition, because VMOS uses the same basic cell design for ROM, p/ROM, and dynamic RAM, very high density ROMs, p/ROMs, and RAMs are in design or prototype stages.

Already available is the AMI S4015 1k x 1-bit RAM that has a specified access time of 45 to 65 ns and power dissipation of 625 mW. High speed (30 ns) and low power versions (300 mW) are on the drawing board. Other products in the design stage include several 4k static RAM chips that are about one-half the size of a comparable n-MOS 4k RAM; these chips include the S4016/2114 1k x 4 200-ns devices and 4017/4019/2147 4k x 1 70-ns devices. EPROMs such as the 16k S4316/2716 devices have a low 15-V programming voltage. The AMI S4264/S4016B 65k ROMs have an access time of 250 ns.

TABLE 8

Typical 4k-Bit Static n-MOS RAMs*

Part No./ Manufacturer/ Organization	Power Supplies	I/O Logic Levels	Power Dissipation	Maximum Access Time (ns)	Minimum Cycle Time (ns)	DIP Package	Data Retention	Notes
9130/AMD (1k x 4)	5 V	TTL	550 mW max	500, 400, 300, 200	840, 690 530, 370	22-pin		Contains memory status signal that simplifies timing and has 400-mV noise
91L30/AMD (1k x 4)	5 V	TTL	350 mW max	500, 400, 300, 200	840, 690 530, 370	22-pin		
9135/AMD (4k x 1)	5 V	TTL	675 mW max	80, 100, 120, 150	130, 160, 190, 235	18-pin		
SEMI 4104/ EMM (1k x 4)	±5, 12 V	TTL	450 mW max	200	300/400	22-pin	to V_{DD} = 4 V	
SEMI 4804/ EMM (1k x 4)	5 V	TTL	500 mW max	400/600	400/600	18-pin	to V_{DD} = 1.5 V	
SEMI 4402/ EMM (4k x 1)	−5, 12 V	TTL	500 mW max	100, 150 200	100, 150 200	22-pin		
5255/National (1k x 4)	5 V	TTL	400 mW max	250	400	18-pin		Nonselect, common I/O
5256/National (1k x 4)	5 V	TTL	400 mW max	250	400	22-pin		
2114/Intel (1k x 4)	5 V	TTL	500 mW max	200, 300, 450	200, 300, 450	18-pin		Low power version with 350-mW max power dissipation; no clock required
2147/Intel (4k x 1)	5 V	TTL	500 mW max	200, 300, 450	200, 300, 450	18-pin		Low power versions with 350-mW max power dissipation
TMS4045/TI (1k x 4)	5 V	TTL	400 mW max	150, 200, 300, 450	150, 200, 300, 450	18-pin		Standby power dissipation of 25 mW
TMS4047/TI (1k x 4)	5 V	TTL	400 mW max	150, 200, 300, 450	150, 200, 300, 450	20-pin		Standby power dissipation of 25 mW

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Magnetic Bubbles

The physical feasibility of magnetic bubbles has been proved. Bubbles can be created and destroyed, moved reversibly in two dimensions, magnetized for presence or absence of charge, and mutually repulsed to perform logic.

Micro-sized bubbles can be supported in magnetic rare earth garnets grown epitaxially on nonmagnetic matching substrates. Since the number of similar process steps is much fewer than for silicon, the cost per area should be lower. Shift registers 1000 bits long, at densities of 1.6M bits/in^2, should be routine. Mask size, not defect density, is the present size limitation.

Electron beam processing should benefit bubble technology: smaller bubbles for higher packing densities and lower costs should result.

Although bubble technology scores high on adaptability, it is different in this respect from IC memories. Partitionability is about the same, but garnet chips carry more bubbles. Lower defect densities, smaller cells, and simpler processes allow economical integration to levels higher than are possible with silicon. Logic, memory, and switches can be intermixed on a finer scale within the garnet because no restructuring is needed. Bubble serial bit speed is slower, about 1 μs, but system throughput may approach that of the highest speed silicon RAMs, where associative and parallel processing can be used.

Magnetic bubble memories combine most of the outstanding capabilities of solid-state and mechanical magnetic storage; however, they perform better against some of these competing technologies than against others. In comparison with fixed-head and floppy discs, bubbles have a higher reliability and a lower error rate, since they employ no moving parts. Other assets are faster access time, lower power consumption, smaller physical size, simple interfacing, and lower entry price—all resulting from the elimination of mechanical elements. However, data transfer rates are lower than those of fixed-head discs, and their per-bit cost at present is much higher than that of floppy discs, except in small systems.

A comparison with semiconductor memories is somewhat unfair since bubbles will probably work in conjunction with random-access memories. RAMs, which have dramatically better access times, higher data transfer rates, and simpler interfacing requirements, will hold their ground as main memory, transferring data into and out of bubble mass storage. In relation to charge-coupled devices, bubble chips have the advantage of nonvolatility and high packing density, but suffer from slower access times and data transfer rates.

Presently, the Texas Instruments TIM 0103 (Table 9) is the only commercially available bubble memory, packing 92,384-bits of nonvolatile storage into a 1 in^2 14-pin dual inline package (DIP). Initial applications of this device will be in microcomputer storage, where at most a few megabits are required. Much work is taking place in this area; bubble density is forecast to increase to 5 x 11^7 bit/cm^2 and 4 x 10^8 bit/cm^2 by 1980 and 1985, respectively, from 5 x 10^5 bit/cm^2 today. Magnetic bubble memories represent a totally new frontier in IC technology. Such manufacturers as IBM, National Semiconductor, Intel, Signetics, and Rockwell are emphasizing bubble research for future use.

TABLE 9

Electrical Characteristics of TIB 0103 92k Bubble Memory

Parameter	Value
Useful capacity (bits)	92,304
Register organization	641 x 144
Drive field rate (max)	100 kHz
I/O data rate (max)	50k bits/s
Minor-loop data rate (max)	100k bits/s
Average access time (first bit)	4.0 ms
Average cycle time (144-bit block)	12.8 ms
Power (100% duty cycle)	0.6 W
Size	1 x 1.1 x 0.4" (2.5 x 2.8 x 1.0 cm)
Package	14-pin DIP
Max permissible external magnetic field in any direction	40 Oersteds

Charge-Coupled Devices

Magnetic bubbles and charge-coupled devices (CCDs) are related in concept. However, while magnetic domains are manipulated in bubbles, in CCDs regions of charge are moved. CCDs require very little host material restructuring. The fundamental difference between CCDs and ICs is that charge remains in the CCD substrate; it is not routed from place to place, through windows, by way of conductors.

Area per bit for a CCD can be a few square mils and will shrink further with electron-ion processing. Volatile charge packets imply periodic regenerators, which increase effective bit area and add process steps. They also tend to limit versatility, since they hamper the asynchronous operation easily attainable with bubbles. Because charge packets do not interact with each other, logic is not intermixed with memory as easily as in bubbles; however, charge packets are intrinsically many times faster and will have no trouble competing on power per bit.

Considering all factors, CCD and bubble memories will cost less than IC memories in the future—on the order of millicents per bit. Magnetic bubbles will probably have the lowest cost, although currently they are slower and cost more. All three technologies rank high in adaptability in different, but perhaps complementary, ways. The gains in service effectiveness to be achieved are only a small fraction of potential possible when system innovators take advantage of the new levels of adaptability. Available CCD memories, the largest of which has a density of 65k bits, are summarized in Table 10.

Predictions are that the 65k CCD will decide the future of CCD memories—prime requirements being producibility and low cost. For example, both the TI TMS 3064 and Fairchild F464 are organized in 16 4k loops, while the Intel 2464 is organized as 256 256-bit loops. However, the F464 uses four clocks while the 3064 and 2464 require only two. CCDs will serve different applications than dynamic MOS RAMs—replacements for mass data storage tapes, discs, and drums that require low cost/bit. During 1980, 256k- and 1M-bit CCD memories should become available.

Summary

The vast number of different types of semiconductor

TABLE 10

Typical Commercially Available CCD Memories*

Model/ Manufacturer	Size	Organization	Operating Modes	Power Supplies	External Clocks
CD460/ Fairchild	16k	4 blocks of 32 128-bit registers, 4 data I/O	Read, write, read/modify/ write, recirculate	±5, 12 V	1 at 120 pF 1 at 15 pF
2416/Intel	16k	64 256-bit registers, 1 data I/O	Read, write, read/modify/ write, shift	−5, 12 V	2 at 500 pF 2 at 700 pF
CC16M1/ Bell Northern Research	16k	4 4096-bit registers, 4 data I/O	Read, write, recirculate	±5, 12 V	2 at 60 pF
CD450/ Fairchild	9k	9 1024-bit registers, 9 data I/O	Read, write, read/modify/ write, recirculate	−2.5, 5, 12 V	2 at 400 pF
F464/ Fairchild	65k	16 4096-bit registers, 16 data I/O	Read, write, read/modify/ write, recirculate	±5, 12 V	2 at 90 pF** 2 at 30 pF***
2464/Intel	65k	256 loops at 256 bits/loop	Page mode (2.5 MHz), serial (1 MHz), refresh, search	−5, 12 V	2 at 10 pF
MN-64/ Mnemonics	65k	16 blocks of 4k bits	Read, write, recirculate	12, −7.5 V	10 (150 to 1000 pF) (HF-LF)
TMS 3064/ Texas Instruments	65k	16 blocks of 4k bits	Read, write, read/modify/ write, shift	±5, 12 V	20 at 160 pF

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**High speed clock
***Low speed clock

(*Continued on p* 126)

memories available to the system designer is increasing steadily. Technological advances, such as projection printing, electron beam, x-ray masking, plasma dry etch, and automation of diffusion steps, should provide a continuous flow of new products (such as 64k dynamic RAMs). This makes it necessary for the designer to thoroughly evaluate various tradeoffs in selecting the particular memory(s) best suited for the application. Speed (as expressed by access and cycle times), power dissipation, and cost are usually the major considerations. To minimize cost, the designer should not implement a level of speed higher than that required by the application.

High density devices are advantageous because they conserve space and, perhaps more important, because they help simplify system design. Interconnections are reduced and overall reliability is improved.

Frequently, trading off speed for power is necessary. With all other factors equal, designing for high speed means utilizing more power. Requirements must be viewed with regard to temperature rise and reliability, as well as number and rating of the power supplies needed. With memory prices per bit steadily declining, power supplies constitute an appreciable portion of overall future system cost.

Dynamic memories operate at higher speeds and consume less power than static memories. However, they may necessitate more costly auxiliary components, such as a variety of power supplies or critical clock control. In the past, memories generally used more than one clock with critical phasing requirements and relatively large voltage swings, although some recent devices feature single clocks. (Clocks requiring both positive and negative swings are the least convenient.) The latest dynamic RAMs possess simpler clock and timing characteristics than earlier models, narrowing the gap in application simplicity between themselves and static devices.

Input/output compatibility is important, if expensive level changers and buffers are to be avoided. The latest high density memories offer TTL compatibility, substantially enhancing applicability.

TABLE 10 (Continued)

Model/ Manufacturer	Data Rate (per I/O)	Average Access Time	Refresh Time (ms)	Power (mW) Chip	Standby	Interface	Package
CD460/ Fairchild	0.5 to 5.0 MHz	12.8 μs	2 (halt) 10 (recirc)	200 (max)	50	All TTL except clocks	22-pin DIP
2416/Intel	0.1 to 2 MHz	96 μs	1.2 (9 μs max shift interval)	300 (max)	24	All 12-V except enhanced TTL data in	18-pin DIP
CC16M1/ Bell Northern Research	1 to 10 MHz	200 μs	4	340 (max)	200	All TTL except clocks and write enable	16-pin DIP
CD450/ Fairchild	0.05 to 3 MHz	170 μs	2.5	265 (max)	31	All TTL except clocks	18-pin DIP
F464/ Fairchild	4 MHz	500 μs	2	400 (max)	70	All TTL except clocks	16-pin DIP
2464/Intel	1 to 2.5 MHz	300 ns access 128 μs latency	2 to 10	Depends on operating mode		All I/O TTL	18-pin DIP
MN-64/ Mnemonics	5 MHz	2.14 to 214 μs	4 at 1 MHz 0.8 at 5 MHz	65 (1 MHz)		All I/O TTL	22-pin DIP
TMS 3064/ Texas Instruments	1 to 5 MHz	819 μs	4	260 (max)	10	All I/O TTL	16-pin DIP

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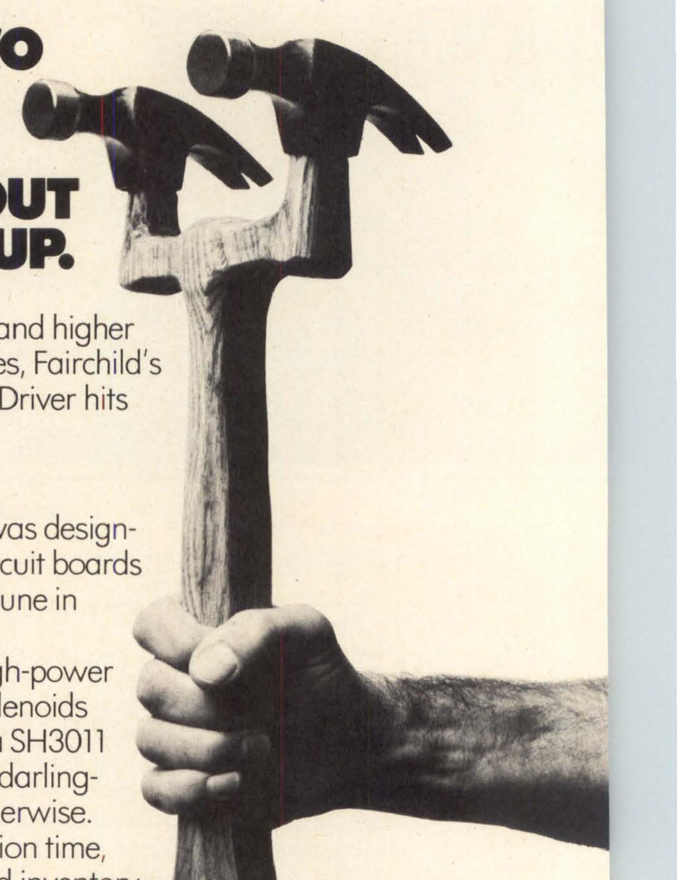

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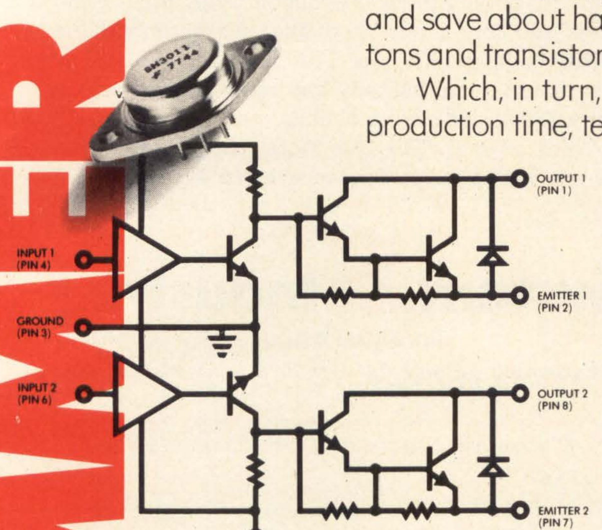

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Peter F. Conklin and David P. Rodgers Digital Equipment Corporation, Maynard, Massachusetts

Design and production of a high technology, interactive minicomputer are the end results of hundreds of architectural and implementation tradeoffs. Alternatives ranging from instruction encoding to processor-memory interconnection, and from high level language procedure call conventions to fault location techniques were weighed. Coping with this multitude of decisions required a design evaluation—or pruning—process encompassing minicomputer motivation factors, the design selection process, and major tradeoffs.

Architecture Alternatives

The need for large addressing capabilities in a minicomputer was perceived several years ago, but it has been only the recent combination of cost and technology trends resulting in high volume availability of semiconductors at a low price that could justify the development of a minicomputer system like the VAX-11/780.™ These trends have been especially emphasized in the area of large memory systems at a low cost per bit, allowing storage and execution of large programs. The market revolved primarily around the ever-increasing acceptance of the interactive, distributed minicomputer, which has been viewed by industry as a viable alternative to the large centralized mainframe and as a corollary to the demand for increased machine functionality at reasonable cost.

Faced with these market and technology trends, the primary design alternatives taken into account for an advanced minicomputer were an enhanced 16-bit architecture with its inherent addressing limitations; a smaller version of existing 36-bit systems; and a wide word length machine with ease of use, speed, and flexibility similar to the PDP-11,™ but with the functionality and power of a clean 32-bit architecture, including large virtual memory software and extensive reliability, availability, and maintainability features.

System Interconnect

Before these directions were established, a group of hardware implementers was examining structures for interactive systems with particular focus on the interconnection among processors, memories, and secondary storage or swapping media. This group set out to design a system bus with high bandwidth, data integrity, and reliability, and with versatile capability for supporting multiple processors. Drawing on past experience, they met those objectives by specifying the Synchronous Backplane Interconnect (SBI™) that is the main control and data path of the minicomputer (Fig 1).

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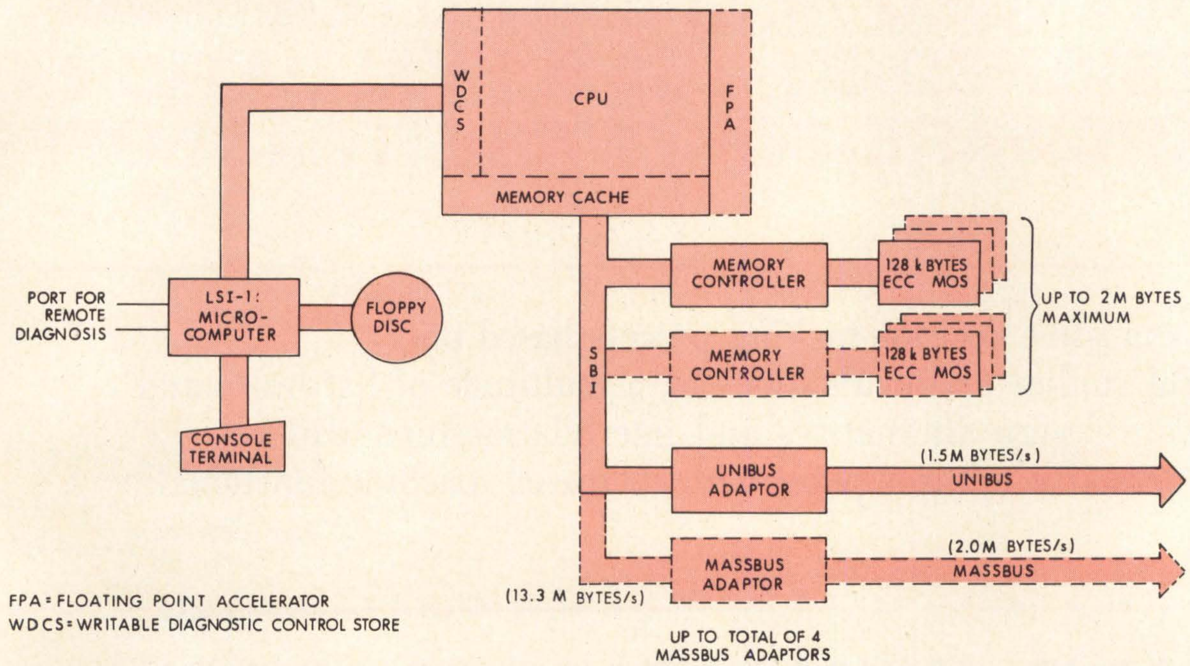

Fig 1 Simplified system block diagram. Major elements of VAX-11/780 system communicate via SBI. CPU performs logical and arithmetic operations programmed by user. Two error detecting and correcting memory controllers store and retrieve data at request of CPU or I/O system. I/O system consists of UNIBUS adaptor that connects lower speed devices to processor, and up to four MASSBUS adaptors that connect high speed devices. LSI-11 console microcomputer communicates with and through CPU using internal data bus

Among the tradeoffs considered in the design of the SBI were synchronous versus asynchronous operation, bandwidth versus access time, distributed versus centralized arbitration, bus length versus bus cycle time, complexity of control versus number of lines, data integrity versus interface cost, serviceability versus interface cost, etched signal paths versus cable connections, and custom large-scale integration (LSI) versus off-the-shelf components. To provide data on which to base these tradeoffs, a computer simulation model was developed. This model allowed hypotheses about cache performance, memory speeds, peripheral controller buffering, multiprocessor interaction, and system saturation to be explored, from which parameters for the bus and other system components were determined. Although many simplifying assumptions were made in constructing the model, only the supposition that processor write cycles were randomly distributed caused the model to predict behavior at variance with the actual usage.

All of the tradeoffs were made to achieve cost-effective design goals. Synchronous operation was chosen to simplify system design in a pipelined environment (for high bandwidth) at the cost of some additional buffering in the interface. Bandwidth was favored over access time in selection of the bus protocol since the cache provides fast effective access time. Distributed arbitration improved system availability and operated more rapidly with less complex logic.

Selection of three meters as the maximum bus length was influenced more by packaging considerations than by bus cycle time since the 200-ns cycle was dictated by other system component delays. With only slight increase in control complexity, the number of lines required for the SBI was reduced significantly, decreasing overall interface cost as well. Data integrity and serviceability were considered so important that a significant fraction of interface cost was allocated to features that enhanced them.

By designing the SBI around the characteristic impedance of etched lines on fiberglass laminate, improvements in electrical and mechanical integrity over cable connections were achieved at the cost of additional development expenditure. Combining several of the interface functions into a pair of custom LSI components provided considerable space and time savings over an interface comprised of off-the-shelf components. Additionally, the LSI components were designed to allow individual interfaces to remain connected to the bus while unpowered.

Architecture Team

A team of computer architects—hardware and software engineers—was assembled simultaneously with hardware and software implementation teams that included logic designers, microcoders, operating system designers, and compiler writers. These teams evolved a carefully plotted minicomputer design in which the architecture and implementations were iterated until an optimal balance was obtained.

The following summarizes the design principles that emerged. Architecturally, the minicomputer has much in common with the PDP-11 while providing significant 32-bit word length functionality, with 2M bytes of physical memory and more than 4M bytes of virtual addressing space. The set of 243 basic instructions are not bit-for-bit identical to the PDP-11, but an experienced programmer could learn the set rapidly; exploitation of the instruction set by higher level language compilers is straightforward. Most of the PDP-11/70 user mode instruction set is provided in an additional compatibility mode that is selected dynamically by software on a process-by-process basis.

A proven, stable Schottky transistor-transistor logic family is utilized in the design. Attachments to the internal SBI are highly buffered; the pipelined bus structure can attain a throughput of 13.3M bytes/s. Both principal PDP-11 external buses (UNIBUS™ and MASSBUS) are used for peripheral attachments. A single state-of-the-art, all purpose operating system is included that fully exploits the 32-bit architecture. Hardware data formats and software record and file formats are compatible with those of the PDP-11 hardware and RSX-11 software, respectively. In addition, a FORTRAN IV-PLUS compiler exploits the instruction set, including the ability to manipulate character strings.

Pruning Process

At several points in the design process, hardware/software tradeoffs were decided during "pruning" meetings, which were instrumental in designing a well-balanced architecture. In general, this process was divided into three major phases: structural design, feature selection, and final tuning. During the structural design phase, a liberal addition of features was allowed to ensure that all feasible ideas were considered. Approximately twice as many features were specified as were justified economically. A formal meeting was held with both the implementers and users of the features. At this meeting performance estimates, historical statistics, and consistency rules were aired, cutting the items almost to final feature specifications. The architecture team then composed the final list of features to ensure that it was consistent and symmetrical. Additional features could be requested later by any implementer or user, but the addition required a detailed justification.

Instruction Set

Basic format of the instruction set was chosen during the architecture design process (Fig 2). Two key design points were that the instructions would have a varying number of operands and that the opcode would be encoded within a single byte. However, it was decided that more than 256 opcodes might be necessary in the future; therefore, certain opcodes were defined as escapes to a second byte. Since each opcode could have from zero to six operands, more than 400 well-specified instructions were accumulated as candidates for the final machine design, based on previous experiences, other architectures, and suggested concepts. Many instructions were simply optimizations of others (Fig 3). For example, the "Clear

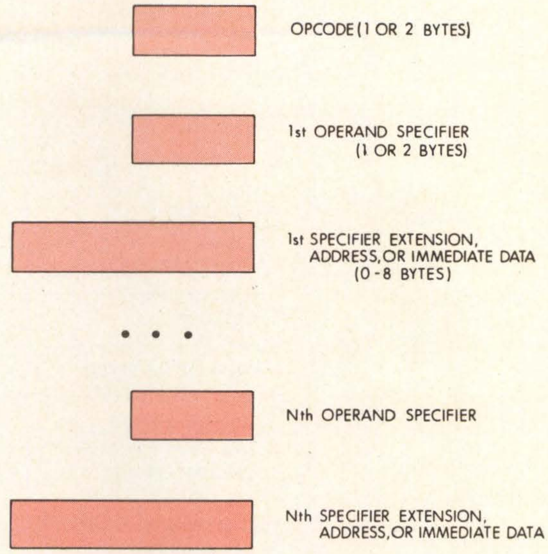

Fig 2 Instruction format. Variable length format can be as short as one byte (eight bits) or as long as needed, depending on type of instruction. Each instruction consists of opcode, which indicates operation, followed by zero to six operand specifiers, which identify operands. Consisting of address mode, which determines calculation used to produce value or address of operand, and other information such as register numbers, displacements, and immediate data, operand specifiers may be 1, 2, 3, 4, 5, 6, 9, or 10 bytes in length depending on address mode and type of operand

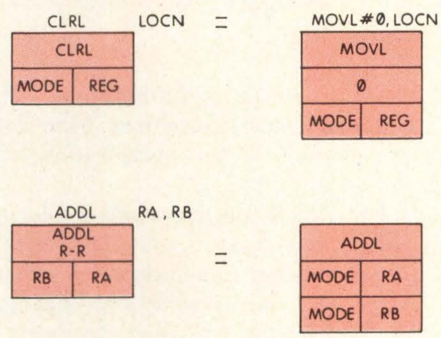

Fig 3 Instruction optimizations. Clear longword (CLRL) instruction accomplishes same function as move longword (MOVL) instruction when data moved are zero. CLRL is shorter because it requires one less operand specifier. When operating on operands contained in registers, add longword (ADDL) instruction could be contained in one less byte if address mode were implied by opcode

TABLE 1

Memory Addressing Modes

Mode	Specification	
Literal (Immediate)	{S ↑, I ↑} # constant	
Register	Rn	
Register Deferred	(Rn)	
Autodecrement	− (Rn)	
Autoincrement	(Rn) +	
Autoincrement Deferred (Absolute)	at (Rn) + at # address	Indexed [Rx]
Displacement	{B ↑, W ↑, L ↑} displacement (Rn) address	
Displacement Deferred	at {B ↑, W ↑, L ↑} displacement (Rn) address	

n = 0 through 15; x = 0 through 14; S = Short; I = Immediate; R = Register; B = Byte; W = Word; L = Long word

Location" instruction is an optimization of "Move 0 to Location." Similarly, many machines have included a register-register format as an optimization of general addressing.

Designers of the logic and microcode implementations, operating system, and various compilers met with the architecture team and key management to examine each proposed instruction. Only instructions that satisfied a unique feature requirement, provided symmetry, or had a performance benefit of greater than 1% on the aggregate system performance were retained. It was pointed out that hardware would be somewhat less expensive and performance significantly better if the final instruction count were below 250 so that opcodes could be encoded in one byte, leaving escape codes for future growth. Thus, the instruction count was reduced to 236. Subsequently, only seven instructions—those needed for multiprocessor interlocks, two additional converts for COBOL strings, and a subscript calculation and validation instruction estimated to save as much as 5% on the size of COBOL programs—were added.

Addressing Modes

Originally the most powerful addressing modes were derived from recursive specifications of other addressing modes. Most of the designers disagreed with the result because it was hard to explain and difficult to implement; concern existed that compilers would not take advantage of the features. Finally, the operating system and compiler designers derived a list of the most probable addressing needs; this included a detailed estimate of the allowable length of each type of addressing, enabling the architecture team to eliminate several modes that were contributing to the complexity. A simpler addressing mode design evolved that retained flexibility and was more tightly encoded for several important general addressing forms. When proposed, this form won complete acceptance for its balance of functionality, simplicity, and performance.

Each operand of a VAX-11 instruction starts with a byte that contains a 4-bit mode designator and usually a 4-bit register number. Nine addressing modes specify the way in which the operand location is determined (see Table 1). Register mode indicates an operand located in a general register, literal mode indicates an operand that is part of the instruction, and register deferred mode specifies an operand whose address is in a general register. Autodecrement and autoincrement modes not only locate an operand whose address is in a register, but also subtract or add the size of the operand (in bytes) to the register; respectively, they alter the register before and after use as an address. Autoincrement deferred mode uses the 32-bit quantity whose address is in the designated register as the address of the desired operand; the register is incremented by four after the register contents are used as an address. When the designated register is the program counter, the address is included in the instruction following the address mode.

Three variations of displacement mode add an 8-, 16-, or 32-bit signed integer to a register before using the result as the operand address. Three corresponding displacement deferred address modes determine the address of the 32-bit operand address by adding the signed displacement to the register. Indexed mode may be applied as a prefix to any of the above modes except literal or register; it adds the contents of a register, after multiplying by the operand size, to the address computed by the address mode that immediately follows.

Memory Management

Choice of memory management design was one of the most difficult; there was little unanimity as to the best form. Many systems have a protection relocation arrangement, possibly with a straightforward paging mechanism added, and have been proven to be efficient, understandable, and reliable. Two other schemes are prevalent in the academic environment. The first is the segmentation and ring system used on MULTICS,[1] a commercially viable mainframe system; the second is the capabilities model used in several research systems. The latter has found particular favor because of its theoretical properties for guaranteeing protection.

Each model was explored for memory management. Selection of the final design was based on good performance, ability to build a complete set of languages and operating system, and ability to understand and predict the resulting performance. Because a durable architecture was desired, implementation of the capabilities model was examined initially. Unfortunately, none of the academic implementations had the necessary speed characteristics. Several alternatives were designed that came close; however, fundamental problems discovered with using the capabilities model for subroutine calls were that no current applications language is prepared to deal with a dynamically changing address space, and copying of all arguments (not just pointers to them) is required. Both prohibited its use for FORTRAN, COBOL, and BASIC. The capabilities system is an excellent method of controlling communications between processes, which is essentially the way it is used in the HYDRA system.[2]

The segmentation model has various benefits; however, general segmentation tended to require several overhead memory references (three to five in this case) for each real memory reference. To a certain extent this can be compensated for by a hardware translation buffer that remembers recent translations. In fact, the final result is very close to this model. Concern existed that system performance would be unacceptable at minicomputer prices in an interactive environment. Pricing required that the size of the translation buffer and its associated logic be constrained. The interactive environment required that the system perform well in an environment of frequent context switches between processes; either each context switch must discard the contents of the translation buffer or the translation buffer must be system wide. In the former case, the buffer is not much help with frequent context switching; in the latter, the maintenance cost becomes excessive when pages are moved in and out of memory.

The solution was to decrease the number of overhead references required to make a real reference. A group of software and hardware designers then trimmed the design needs of memory management to a practical level of overhead. The resulting set of changes had all useful features of the segmentation design, while reducing overhead by more than a factor of two. The ring structure pioneered by MULTICS was kept. The solution was constrained to four access modes, two for the operating system nucleus and two for the application/user, enabling protection information to be encoded well into the two most size-sensitive data structures (the Program Status Longword and each Page Table Entry).

Most reductions, which were in the overhead references required to map a page of virtual memory to real memory, consisted of giving up the generality of full segmentation and combining the best features of relocation registers and paging. Concerning general segmentation, it was observed first that the addressing modes encouraged all compilers to generate position independent code, and secondly that practical applications have only two types of dynamic data structures. One type is the extremely regular behavior of the stack used to allocate variables in a recursive environment and to make procedure calls. The other is the completely irregular needs of a "heap" storage for dynamic allocation of data structures such as strings and list structures, since a heap has no predefined pattern for allocation and deallocation strategies. This suggested a need for only two points at which data structures could grow independently.

A relocation type of system is utilized to control these storage regions. In particular, each region of a process is described by a pair of registers. A length register specifies how many pages are currently allocated in the region (whether in physical memory or paged out on the disc). The other register specifies the base of a page table that describes the location and access protection of each page in the region. Since the page table for a process region could be lengthy, it is actually paged in system virtual memory. This virtual memory is described by a similar page table in physical memory. The precise result is two overhead references that access a process location—one that finds the process page table entry in the system region and one that examines the page table entry itself, allowing the design of a cost-effective translation buffer that would ensure good performance even in a very interactive or time-critical environment.

RAMP Features And Implementations

Early in the design of both hardware and software, emphasis was placed on a reliability, availability, and maintainability program (RAMP). Representatives of field service, software support, manufacturing, marketing, documentation, diagnostic engineering, and hardware and software engineering proposed features, tools, and strategies expected to improve the overall minicomputer quality. In a manner similar to the design of the instruction set, these proposals were detailed and reviewed by both implementers and users in a series of meetings. Each feature or strategy had to be cost-justified either directly through reduced support costs or indirectly through increased value to the customer.

Although RAMP features were included in every element of the system, the insistence on payback from each feature caused the majority of allocated product cost to be concentrated in a few high leverage areas: system bus and bus interfaces, error correcting and error logging memory controllers, and the diagnostic console. Even in these areas, features with marginal value were eliminated.

The SBI and its attached interfaces achieved high reliability and data integrity through a combination of conservative electrical design, data checking, protocol checking, and tolerance for transient failures. They allowed the SBI to continue to handle system traffic even though an individual unit might be malfunctioning. Maintainability is assured through the use of a bus history silo and error status bits present in every interface. These error log facilities operate in such a way that the exact environment leading up to the time of a failure may be recorded. Additional proposed features were eliminated by reasoning that errors resulting from multiple points of failure were highly unlikely so that detection or recovery was unwarranted. For example, deviations from bus protocol are recorded, but those resulting from two or more independent failures are not checked.

Similar evaluation of empirical data on semiconductor memory components lead to the error correction scheme implemented in the memory controller that transparently corrects single-bit errors, detects double-bit errors, and may or may not detect errors in three or more bits. Thus, the software does not include routines for reconstruction of single-bit failures, as is the case with simple memory parity schemes. The memory controller records the location of the failing component—in the case of correctable errors—for software error logging. However, in the event that the error rate exceeds the ability of the software to record the occurrences, only a lost error indication is recorded.

The diagnostic console has extensive facilities for system control of operating and maintenance conditions. These include timing margin control and the ability to force the execution of diagnostic microprograms. Diagnostic feature implementation was nevertheless guided by cost. Although the diagnostic console has access to every module in the processor through the internal communication path and a special "diagnostic visibility" bus, it cannot examine the contents of the microcontrol storage random-access and read-only memories. The large number of wires and interface circuits hampers direct access. These memory elements must be verified by checking the parity bits associated with them. Machine check error logging, unattended restart, disc error correction code,

TABLE 2

Summary of Edit Pattern Operators

Name	Operand	Summary
Insert:		
EO$INSERT	ch[1]	Insert character, fill if insignificant
EO$STORE_SIGN	—	Insert sign
EO$FILL	r[2]	Insert fill
Move:		
EO$MOVE	r	Move digits, filling insignificant
EO$FLOAT	r	Move digits, floating sign
EO$END_FLOAT	—	End floating sign
Fixup:		
EO$BLANK_ZERO	len[3]	Fill backward when zero
EO$REPLACE_SIGN	len	Replace with fill if negative zero
Load:		
EO$LOAD_FILL	ch	Load fill character
EO$LOAD_SIGN	ch	Load sign character
EO$LOAD_PLUS	ch	Load sign character if positive
EO$LOAD_MINUS	ch	Load sign character if negative
Control:		
EO$SET_SIGNIF	—	Set significance flag
EO$CLEAR_SIGNIF	—	Clear significance flag
EO$ADJUST_INPUT	len	Adjust source length
EO$END	—	End edit

[1]ch = one character
[2]r = repeat count in the range 1 through 15
[3]len = length in the range 1 through 255

online diagnostics, and remote diagnosis offer a balance between costs incurred and benefits received.

Edit Operators

Design of an instruction that would perform picture editing for COBOL and PL/1 started by researching needs both as documented in the appropriate American National Standards and as found in the actual implementations of the languages for various manufacturers. Based on this approach, a design was established for an edit instruction that would support all of the high frequency needs of the languages (Table 2). In this case, confirmed data were available that showed the frequency of various picture operators.

An instruction was needed that would run efficiently, without requiring a large amount of microcode to implement. The initial proposal, which required an excessive amount of state for special character variables, was reworked by the architecture team to a more reasonable state. However, it was not until the architecture team and hardware implementers met that the pattern operators were reduced from over 25 to the current 16. This also resulted in a microcode reduction of over 40%. Despite this trimming, the space to store patterns and the time to execute them were unchanged for any important usage.

Major Design Tradeoffs

After the major architectural and implementation decisions had been made, the design remained relatively stable. However, as use and further studies brought out additional facts, specific portions of the architecture were revised. Following are accounts of other major design tradeoffs made.

Procedure Call Instructions. This approach investigated the needs of many current languages; concentration was directed specifically on FORTRAN, COBOL, and BASIC, and in general, on the needs of ALGOL, PL/1, APL, and PASCAL. The study showed that it was feasible to design a single interface between routines that would be efficient while also allowing any one language to call another. Critical needs for operating system and implementation language calls so that one interface could be used between all subsystems and languages were also taken into account.

As the architectural design proceeded, the microcode requirements grew drastically. The number of options involved in creating the argument list was very large with many choices of location of data, location of descriptors, and types of data. Although all this information could be encoded, the results were becoming progressively less optimal. In particular, most calls were generated by languages such as FORTRAN or COBOL for which the compiler can precompile the argument lists; thus, after several design reviews, the implementation was limited to that which needed to be created dynamically in all cases.

Two important cases of calling are one in which the entire list could be precompiled, and one in which the list could be created dynamically. Two call instructions were included with a common result so that each compiler could generate calls in its optimal fashion. The call also included setup and cleanup steps common to all languages. Left to the individual compilers were language dependent choices of creating the argument list and allocating local stack storage. The resulting instructions do more, faster than their precursors, and yet support the general interfacing needs of all languages and subsystems (Fig 4).

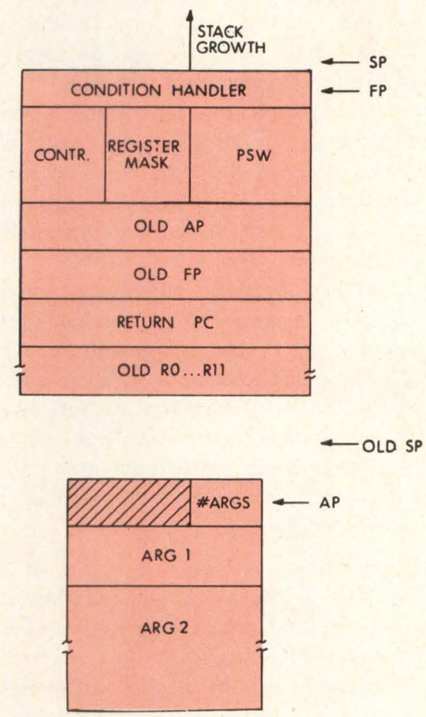

Fig 4 Procedure call frame. Call instructions save environment of calling procedure on stack and establish new environment for called procedure; corresponding return from procedure instruction restores saved environment, removing it from stack, before returning control to calling procedure. Call instructions always save program status word (PSW) containing trap enable bits, general registers containing addresses of procedure's argument list and caller's state, and instruction following call. If called procedure indicates intention to use any other general registers, these are saved along with bit mask denoting those saved. Trap enable bits for called procedure are set to canonical state and pointer to its condition handler is set to zero. Finally, frame pointer (FP) and argument pointer (AP) general registers are loaded with addresses of newly created stack frame and caller's argument list, respectively. Argument list is data structure containing number of arguments and combination of argument values, address, and descriptors as determined by calling and called procedures

Context Switching. Originally, the goal was to include all task scheduling in microcode. As the design progressed, the defined mechanisms grew. A few specific tuned mechanisms were needed for task scheduling and synchronizing. Theoretical primitives, such as Djikstra's P and V operators,[3] needed to be complemented with some higher level "primitives" in order to achieve compact code and high performance at the system level. Common event flag blocks, mailboxes, and asynchronous system traps (ASTs) were implemented by the operating system in addition to the traditional semaphores. Furthermore, semaphores were used for both resource counters and mutual exclusion. Each of these, as well as several other mechanisms, had to interface to the scheduler, providing a constantly growing set of interfaces and special cases for the microcode to handle.

During an interactions and scheduling policies meeting, several recurring code sequences were noted that represented over 90% of the time the operating system spent in "scheduling" overhead. These sequences were incorporated into the architecture as instructions. The interfaces and policies were left to software.

Net effect, which could be tuned and modified for several years, was a very clean implementation that achieved virtually all that was possible in "complete" microcoding (Fig 5). The benefit of this approach was that as performance measurements of the system were available, the speed of the scheduler was increased substantially by changing its algorithms and coding. This could never have been done if the scheduler had been committed to microcode.

Math Function Library. A significant goal of the architecture was to help create a standard mathematics function library having good performance without sacrificing accuracy. Many FORTRAN programs have execution times that depend primarily on the performance of the math library, especially sine, cosine, arctangent, exponential, and logarithm functions. Usually the algorithm selected to approximate the function is a sequence of multiplies and adds of the powers of the argument and a table of coefficients. Multiply is used rather than divide because multiply algorithms are faster than divides for any reasonable bounds on cost. For the formula to produce a result with reasonable error bounds in a short time, the user's argument is first reduced to a normal range.

To help general math functions, two special operations are provided. The first performs argument normalization as accurately as possible, and the second performs the iteration of multiply-add via Horner's method (ie, repetition of intermediate is replaced by coefficient plus argument times intermediate).[4,5] The latter requires attention to rounding of the intermediate values.

In general, argument reduction is done mathematically by taking the remainder upon division by some constant. For example, the trigonometric functions could be normalized by dividing the argument by 2π to bring the argument into the range of one rotation. Actually, the trigonometric functions will divide by a fraction of 2π and use one of several different approximations, depending upon which quadrant or octant is involved. In any case, multiplication is faster than division; thus, the range reduction instruction does a multiply by a program supplied constant that is the reciprocal of the "divisor." In order to obtain maximum accuracy if the input is accurate, this instruction takes a multiplier that is eight bits longer than the normal floating-point operand. This ensures that no error is introduced by the expression of the reciprocal of 2π, or whatever multiplier is used.

The second instruction introduced for the math library is the "polynomial" instruction; it is given a table of coefficients and a polynomial order, and it applies Horner's method to the reduced argument to produce a series value. The polynomial

$$a(0) + a(1)x + a(2)x^2 + \ldots + a(n)x^n,$$

where a(0) through a(n) are constant coefficients of the powers of the variable x, can be evaluated with a minimum number of arithmetic operations if rewritten as

$$a(0) + x(a(1) + x(a(2) + \ldots + xa(n)) \ldots).$$

Evaluation consists of alternate additions of constants and multiplications by the variable with the result accumulating; this process begins with constant a(n) and terminates with addition of constant a(0).

Because the table could be lengthy (even an order 5 evaluation would be noticeable in a real-time environment), the instruction is interruptible. It turns out that in practical cases, there is no rounding issue between terms, so that normal floating-point rounding can be performed. However, it is desirable that extra rounding bits be carried from the multiply to the corresponding add. In some cases, this extra rounding can save a term in the polynomial, thus improving performance for a given level of accuracy.

The final design aspect concerned where the result of the polynomial instruction was to be left. Most other instructions store the destination in a location specified by a distinct operand. For this instruction, that would have required saving an extra register to remember the destination address across any interrupts. This, in turn, would have slowed down the math library by a noticeable amount, in some cases as much as 5 to 10%. However, it was detected that every application of this instruction always left the final result in R0 (the function value register); therefore, an extra performance benefit was gained.

Cyclic Redundancy Check Instruction. Traditionally, various schemes have been used to double check a sequence of data to be sure the data have not deteriorated in the presence of possible sources of corruption. Cyclic redundancy checks (CRCs)[6,7] have been used frequently because they involve a binary feedback method unlike most sources of noise. Thus, a CRC is likely to catch data corruption. Most discs, tapes, and communications lines include some form of CRC in the hardware. For this minicomputer design, it was desirable to provide a similar capability for software. An instruction was designed that would allow the calculation of specific CRCs for those applications when it was impractical to include a CRC box in hardware (Fig 6).

In this minicomputer architecture, the CRC instruction allows efficient calculation of any CRC polynomial up to order 32. At current machine speeds, this is sufficient to protect data with the probability of undetected corruption being less than once in several years. In many cases, the data to be protected do not reside in one location or string. The instruction was designed so that several CRC calculations could be chained to produce one check value.

ENTER ON RESCHEDULE INTERRUPT:

1. SAVE OLD PROCESS CONTEXT
2. GET O. P. (OLD PROCESS) PRIORITY
3. BIT MARK O. P. PRIORITY QUEUE AS NONEMPTY
4. SET O. P. STATE TO "COMPUTE"
5. INSERT QUEUE TO TAIL OF O. P. PRIORITIES QUEUE
6. BIT FIND HIGHEST PRIORITY NONEMPTY QUEUE
7. REMOVE QUEUE FROM HEAD OF NEW PROCESS PRIORITY QUEUE
8. IF LAST ENTRY,
   BIT MARK N. P. (NEW PROCESS) PRIORITY QUEUE AS EMPTY
9. SET N. P. STATE TO "CURRENT)"
10. IF N. P. CURRENT PRIORITY = N P. BASE PRIORITY,
    DECREMENT CURRENT PRIORITY
11. REMEMBER N. P. CURRENT PRIORITY
12. MOVE N. P. PROCESS CONTEXT BLOCK ADDRESS TO HARDWARE
13. LOAD N. P. CONTEXT
14. RETURN TO USER TASK, CHECKING FOR ASTs

Fig 5 VMS process scheduler. Software consists of very small number of instructions as result of implementing, as instructions, basic operations required for task. Each step in algorithm is accomplished by one instruction. Scheduling policy is not implemented in these basic operations, which allows policies to be changed in response to performance or installation requirements

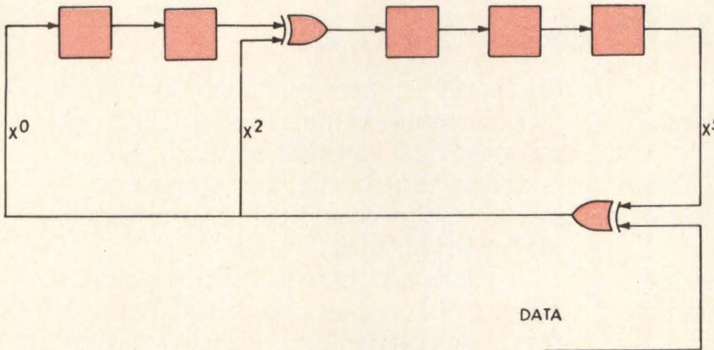

Fig 6 Linear feedback shift register. Typical hardware implementation of CRC circuitry uses shift registers and Exclusive-OR elements to accomplish serial division of data stream by $P_5(x) = x^3 + x^2 + 1$ check polynomial. Polynomial and number of check bits are built into circuit

It can calculate CRCs at a rate approximately 10 times faster than the equivalent instruction sequence, and faster than most hardware CRC boxes.

The CRC of a data string can be calculated by taking several bits at a time, shifting the result, and Exclusive-ORing in a value calculated from the bits shifted out. This calculated value can be precomputed so that the CRC instruction takes a table of such values. The principal design issue was how many bits to shift at each step—if the number is too small, it takes more iterations and the instruction runs slower; if it is too large, the precomputed table gets large and is unlikely to be in the cache, so that the instruction runs slower. The optimum choice is four bits. This results in only two steps per byte of input and uses a table of 16 entries that can remain in the cache; thus, the instruction executes very quickly. Since the CRC is usually coded as a function, it was decided to place the result in R0 for the same reasons stated for the polynomial instruction in the math library.

Conclusions

The VAX-11/780 resulted from the application of a systematic design process that stressed careful specification of alternatives, no *a priori* rejection of features, evaluation of alternatives in a pruning forum that included both implementers and users, unification of the architectural design along simple principles formulated by a small group of hardware and software experts, and implementation by individuals involved in the design. The detailed technique considered each of these hardware and software tradeoffs to successfully create a viable, interactive minicomputer.

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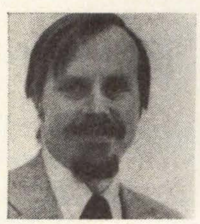

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Serving as the VAX-11/780 engineering manager, David Rodgers has also been a systems engineer and a member of the VAX-11 architectural design team since joining Digital Equipment Corp. His previous experience was as a system programmer, hardware designer, and director of hardware systems. He received his BSEE from Carnegie-Mellon University.

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APPLICATIONS OF VECTOR PROCESSING

The vector-scalar processor, a unified supercomputer system that has very high speed computation capabilities, can execute 140 to 200 million operations per second in scientific and industrial vector signal processing applications. Analysis of algorithms associated with various applications leads to successful implementations

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Scalar and vector signal processing and related algorithms, as implemented on the CRAY-1™ computer system, are applicable to many powerful general-purpose processing systems and illustrate the techniques used to code pipeline or array processors, as well as vector-scalar systems.

Two dichotomies of signal processing applications exemplify the spectrum of powerful supercomputer techniques. The first is active/passive; many signal types are reflections (usually) of signals that are transmitted, then received. Petroleum exploration seismology, radar, active sonar, and atmospheric sounding systems are in the active signal processing category. Typical passive signals are found in earthquake seismology, radio signal processing, passive sonar, radio telescopy, electroencephalography, and electrocardiography. The second dichotomy is acoustic/electromagnetic; acoustic signals are typified by those in seimology and sonar, while electromagnetic signals include radar and radio.

A large number of common computational procedures are used in many of these applications to process the signals received from multiple sensors. These procedures generally fall into one of several categories: direction finding and signal enhancement, frequency analysis and separation, and a plethora of "downstream" routines that are dependent on signal type, such as signature detection, analysis, and cataloging; clutter elimination; and resource scheduling.

Ed Note: This article complements "An Introduction to Vector Processing," by Paul M. Johnson, which appeared in *Computer Design*, Feb 1978, pp 89-97. While the previous article established basic principles of parallel vector processing, this follow-up demonstrates several real-world implementations as performed on a supercomputer system.

Computer Architecture

The vector-scalar signal processor contains both a very high speed vector processing unit and a very high speed scalar processing unit. It is difficult to characterize the raw computing power of a powerful general-purpose computer capable of extremely high processing rates; however, speeds of approximately 140 million floating-point operations per second (MFLOPS) are attainable when multiplying large matrices, and 200 MFLOPS are possible in bursts. These rates are achieved by combining scalar and vector capabilities into a single central pro-

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cessor which is joined to a large, fast, bipolar memory. Vector processing—performing iterative operations on sets of ordered data—provides result rates that greatly exceed those of conventional scalar processing. Scalar operations complement the vector capability by providing solutions to problems not readily adaptable to vector techniques.

Basic organization of a CRAY-1 computer system is discussed and illustrated in Johnson's article (see Bibliography). The central processor unit (CPU) is a single integrated processing unit consisting of a computation section, a memory section, and an input/output (I/O) section. Memory is currently expandable from 0.25 million 64-bit words to 1 million words (2M to 8M bytes). The 12 full-duplex I/O channels in the I/O section connect to a maintenance control unit (MCU), a mass storage subsystem, and a variety of I/O stations or peripheral equipment. The MCU provides for system initialization and for monitoring system performance. The mass storage subsystem provides secondary storage and consists of one to eight disc controllers, each with one to four disc storage units. Each storage unit has a capacity of 2.424×10^9 bits, so that a maximum mass storage configuration could hold 9.7×10^9 8-bit bytes.

Computation section consists of an instruction control network, operating registers, and functional units. The instruction control network performs all decisions related to instruction issue and coordinates activities for three types of processing—vector, scalar, and address. Associated with each type of processing are registers and functional units that support the processing mode. For vector processing, these include a set of 64-bit multi-element vector registers (V0 to V7), three functional units—add, logical, and shift—dedicated to vector applications, and three floating-point functional units—add, multiply, and reciprocal approximation—supporting both scalar and vector operations. For scalar processing, there are two levels of 64-bit scalar registers (S0 to S77 and T0 to T77) and four functional units—add, logical, shift, and population/leading zero count—dedicated to scalar processing, in addition to the three floating-point functional units shared with vector operations. For address processing, there are two levels of 24-bit registers (A0 to A7 and B0 to B77) and two integer arithmetic functional units—add and multiply.

Vector and scalar processing are performed on data as opposed to address processing, which operates on internal control information such as addresses and indexes. Data flow in the computation section is generally from memory to registers and from registers to functional units. The flow of results is from functional units to registers and from registers to memory or back to functional units. Data flows along either the scalar or vector path depending on the mode of processing.

Flow of address information is from memory or control registers to address registers. Information in the address registers can then be distributed to various parts of the control network for use in controlling the scalar, vector, and I/O operations. Address registers can also supply operands to the two integer arithmetic functional units. These units generate address and index information and return the result to the address registers. Address information can also be transmitted to memory from the address registers.

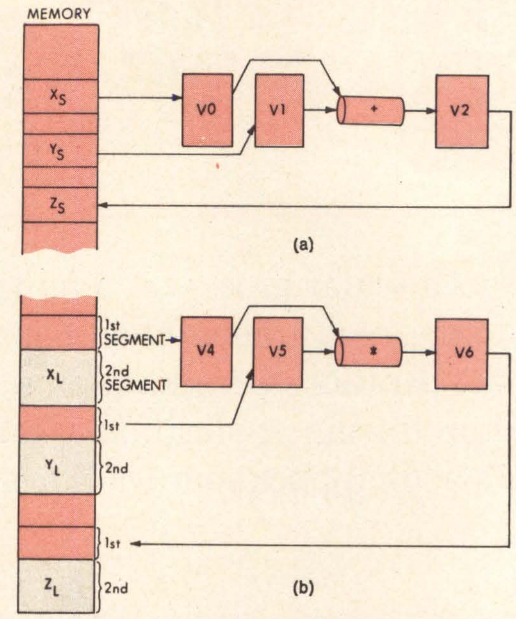

Fig 1 Vector segmentation. Segmenting of vector operations involves vectors of more than 64 elements. This processing procedure is required for computers with hardware limitations on vector length. The programmer never sees this segmentation. In short vector addition (a), $X_s + Y_s \rightarrow Z_s$, no segmenting is required. Long vector multiplication (b), $X_L * Y_L \rightarrow Z_L$, however, does require segmenting. In this diagram, the shaded segment is processed after the unshaded segment

Processing Techniques

All processing operations are performed between registers, allowing prefetching of operands and poststoring of results, as well as fast access to intermediate results. Since each of the eight V registers holds up to 64 elements (each is a 64-bit word) of a vector, long vectors are processed in blocks of 64 elements and a remainder, as shown in Fig 1. Here the sum of two 40-element vectors and the product of two 100-element vectors are illustrated. The 40-element vectors are added in one operation, while the 100-element vectors require two steps (this is transparent in FORTRAN, of course).

During most calculations, the scalar processor performs bookkeeping operations, such as indexing, counter incrementing, and checking to determine what code is next, while floating-point operations are streaming through the vector processor. Since these scalar operations do not involve floating-point operations, they proceed in parallel with vector processing. For codes that are "vectorizable", bookkeeping is generally done in a small fraction of the time required for vector operations; thus, there is no delay in starting a vector operation after the previous operation has finished.

Because of the independence and parallelism of the functional units, the processing of V1 + V2 * V3 proceeds as follows:

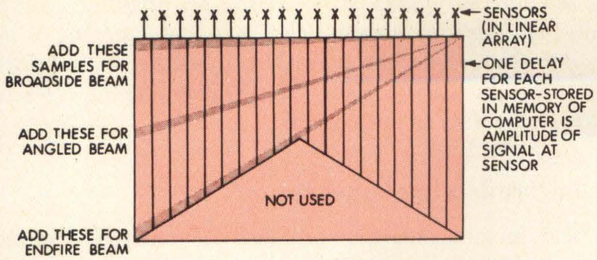

Fig 2 Beamforming. Delay line for each sensor is shown as a vertical subrectangle of the total beamformer memory. Each time a new set of amplitude samples is collected, all samples in the beamformer are logically moved down one row to make room for the next set of samples

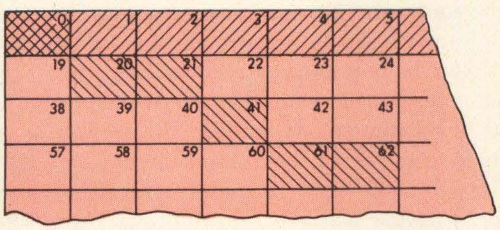

Fig 3 Broadband digital beamforming. Shaded cells (0 to 5) form the broadside beam and the beam value is computed using a vector memory fetch. Shaded cells (0, 20, 21, 41, 61, and 62) form an oblique beam and must be fetched serially because of nonlinearity of their subscript sequence. Vertical columns of boxes represent delay lines of Fig 1; each box shows one memory cell. Number in each box is its relative address in memory

Process Step			Comment
LOAD	V1		Load 1st operand into register V1
LOAD	V2		Load 2nd operand into register V2
LOAD	V3	Chain	Load 3rd operand into register V3
MULTIPLY	V2 * V3 → V4	Chain	Multiply V2 by V3 and place result into V4 (temporarily)
ADD	V1 + V4 → V5	Chain	Add V4 to V1 and place result into V5
STORE	V5		Store result from V5

A delay exists in getting each pipe† started (memory accessing pipe, multiply pipe, and add pipe), but once started, all operations proceed together at a computational rate of 160 MFLOPS. Pipe startup time is eight or nine clock cycles, and the above operation takes 81 clock periods for vectors with 64 elements (eight clocks for add startup plus nine clocks for multiply startup plus 64 clocks for 64 elements). Concurrent vector operations are called "chaining," and 81 clock periods are equal to one chain time. Because of the short startup time of the vector functional units, there is little loss of speed when using short vectors. For typical operations, vector lengths of three elements or less run faster in scalar mode, while those of four elements or more run faster in vector mode. In addition, vector mode is about five times faster than scalar mode on long vectors such as those that must be segmented into blocks of length 64 or less. Transfers between memory and vector registers all proceed at one word per clock period, unless the increment between successive memory locations, which is arbitrary, is a multiple of ±8.

Clearly any vector operation can be processed as an iterated scalar operation, as it is on any scalar processor. The "scalar mode" referred to previously is for the operation performed in an iterated scalar loop instead of in a vector operation.

Application Algorithms

Several common algorithms that perform the operations required to process signals received from a seismic or passive sonar system using multiple sensors are presented as the type of application readily handled by a supercomputer. Usually, these signals are enhanced first by beamforming; then, they are filtered and frequency analyzed. Frequency analysis is normally accomplished with a fast Fourier transform (FFT). After the FFT, interpolation and signature analyses are usually performed.

Beamforming Operation

The initial signal-processing operation performed in a multiple-sensor system is the formation of a beam or beams. This operation provides two types of information enhancement on the signals: determine signal directional information and increase signal-to-noise ratio. For application simplicity, an equally spaced linear array of sensors is discussed. Fig 2 shows an array of sensors, each attached to a delay line so that its output signal is stored for a short period of time. If the delay line for each sensor is long enough for a signal to propagate to the farthest end of the sensor array in the time that a sampling signal passes down the delay line, beams can be formed in all directions. Beams in three directions—broadside, at an oblique angle, and end-on—are formed by adding the elements from the delay line, as shown by the shaded areas.

Computationally, it is necessary to be able to add the elements of a vector with as few as 12, or as many as several thousand, elements because arrays of such disparate numbers of elements are used. Furthermore, especially for large sensor arrays, it is frequently necessary to weight the signals (multiply by a weighting coefficient before summing) from some sensors more heavily than others so that the required operation is an inner product.

$$\sum_i w_i * x_i\,(t_{i_\alpha})$$

where

w_i = weight for shaping
x_i = ith datum
t_{i_α} = delay for beam at angle α for ith sensor

†The term "pipe" is used for a functional unit because it is pipelined.

```
CASE 1: NO SHAPING
LOAD ADDRESSES FOR BEAMS INTO REGISTERS
A1 <---- 1ST ADDRESS
S1 <---- (A1) 1ST BEAM ELEMENT
COMMENT: "INDIRECT" ADDRESSES AND 1ST
SUMMAND ARE NOW LOADED
FOR       i   <---- 2 TO M
          A1  <---- iTH ADDRESS
          S2  <---- (A1)
          S1  <---- S1 + S2
COMMENT: THIS LOOP SUMS ALL BEAM ELEMENTS
TO PRODUCE BEAM

CASE 2: SHAPED BEAM
LOAD ADDRESSES FOR BEAMS INTO REGISTERS
FOR       K   <---- 1 TO M/64 + 1
          i   <---- 1 to MIN (M, 64)
          A1  <---- iTH ADDRESS
          S1  <---- (A1)
          V1i <---- S1
*V4 <---- SHAPING WEIGHTS, SEGMENT k
 V5 <---- V4 * V1
 V5 <---- V5 + V4
COMMENT: HERE THE SHAPING MULTIPLY
IS DONE WITH A VECTOR OPERATION TO
SAVE TIME
RECURSIVE ADD OF V5
V5 <---- (V5 + V1) OR (V5 + V3)
COMMENT: THE RECURSIVE SUM ADDS THE
64-ELEMENT VECTOR ABOVE TO AN 8-ELEMENT
VECTOR

S2 <---- V5_56 56TH ELEMENT OF V5          } SUMS
FOR       i   <---- 57 TO 63               } OUTPUT OF
          S1  <---- V5 iTH ELEMENT OF V5   } RECURSIVE
          S2  <---- S1 + S2                } SUM

COMMENT: THIS LOOP SUMS THE LAST
EIGHT ELEMENTS
STORE     S2 = Σ(i=1 to N) xi INTO SUM
```

Fig 4 Beamforming codes. Both shaped and unshaped beamformers are shown. Each case is for an oblique beam that requires irregular addressing of memory

The subscript i varies over all the sensors; weights may depend on the angle, be equal for all directions, or be unity. An additional complication is that indexing is not regular throughout the array, ie, i_a values do not form a linearly increasing sequence (Fig 3). Thus, a vector fetch of the data is not possible.

Beamforming Implementation

In beamforming, the first problem encountered is storing data in memory. It is assumed that data are stored as received; in other words, during each time interval, one datum from each sensor is stored in sensor order in a circular buffer. Beams are formed by computing the sum of a sample for each sensor, such as those samples shown by the shaded areas in Fig 3. Irregular accessing of data is required except for the case of very rapid sampling, when the increment between beam samples is uniform or when only one beam is formed, as in seismic operations. Fig 4 shows both implementations of this algorithm. In the first or unshaped beam case, a fast scalar loop is used because the arithmetic is simple; the second or shaped beam case uses vector operations because of the more complicated arithmetic. Irregular addressing and very high speed of the scalar processor, causes samples to be serially fetched from memory. If the beam is not being shaped, these samples can be added as they are fetched (Case 1); otherwise, they are loaded into a vector register for multiplication by shaping factors, and then added using the recursive-add operation (Case 2). For the special case where data accessing is regular, vector operations can be used throughout. This load chains into the shaping and summing operations; ie, it is concurrent with them.

Filtering Operation

Once beams are formed, it is common practice to filter the signals so that the sampling rate can be reduced; sampling at a rate more than double that of the highest

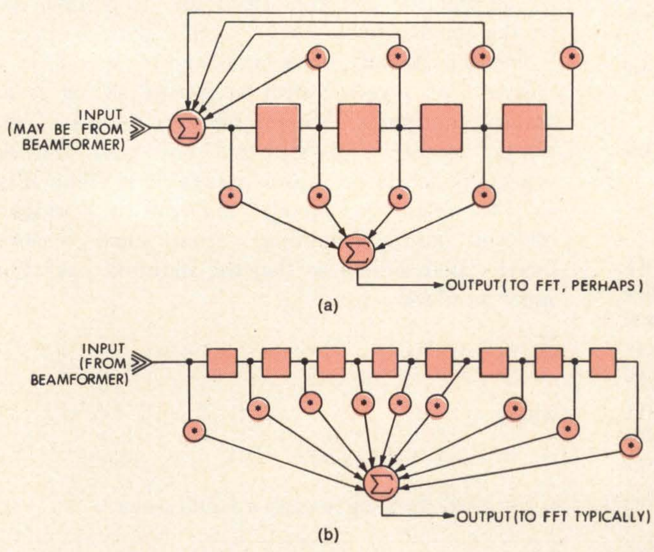

Fig 5 Two common types of digital filters. Efficient short vector operations allow easy implementation of both (a) recursive or infinite impulse response filter and (b) explicit or finite impulse response filter. Each box represents a unit time delay, each circled asterisk represents multiplication by a filter coefficient, and each circled Σ represents summation of all inputs

frequency in the signal yields no additional information. Reduction of the sample rate, called down-sampling or decimation, decreases the volume of data to be processed by succeeding operations. Fig 5 shows signal flow diagrams (not flowcharts) for two common filter types. The first type is called a recursive filter; it is the digital implementation of an analog infinite impulse response filter. Just as an analog filter can ring, this type of digital filter continues producing an output long after the input has gone to zero because of the recursive nature of the processed signal; once impulsed, this filter produces an output indefinitely. The second type is computationally explicit and, because no initial excitation will cause it to ring, is referred to as a finite impulse response or explicit filter.

The recursive filter cannot be calculated for large numbers of data points in parallel because each filter output value is used as an input for the next computation of the next filter output. In other words, computations of output n+1 cannot be initiated until that for output n is completed. Thus, the short vector capability is necessary for efficient recursive filter implementation.

However, the explicit filter can be calculated on large numbers of inputs or for large numbers of outputs at the same time. For this reason, it is often preferred to the recursive filter for digital implementations. Although not shown in Fig 5, the coefficients are frequently symmetrical about the midpoint of the delay line and, if the output is being down-sampled by a factor of two, the filter computation is performed on only half of the input points. Thus, even though the recursive filter is generally more efficient in terms of multiplies per input, the nonrecursive filter is both more efficient and easier to compute when down-sampling and symmetric filter coefficients are used. The explicit or nonrecursive filter is a running inner product:

$$\sum_i f_i x_{i+j} \qquad j = 0,1,2,\ldots,n$$

where f_i are filter coefficients and x_k is datum k.

Filtering Implementation

There are two major approaches to producing high order filters: cascading several low order filters (ie, processing the signal output from one through the next in a chain of filters) or using a filter with many poles and zeroes. In signal processing systems with short word lengths, cascading is preferred because it reduces computational errors; highly parallel systems run more efficiently with high order filters.

In a recursive filter (Fig 6), short vector operations allow efficient implementation even for the 4-pole, 4-zero filter illustrated, making cascading filters feasible. In this case, there are four poles plus four zeros or eight coefficients, ie, vector length (VL) = 8. For high order filters, ie, those with many segments for the delay line, processing is more efficient because of the longer vectors that can be used in the processor. Cascading low order filters is not necessary because of the accuracy of the 48-bit mantissa floating-point arithmetic in the computer system. Fig 6 shows that each pole coefficient is multiplied by a recursed output and each zero coefficient is multiplied by an input datum; then the products are summed to produce an output.

In the program for the nonrecursive filter (Fig 7), to preserve generality, no decimation of the output is shown nor is any symmetry of the filter coefficients used, even though both of these may be used at times. Particularly noteworthy in this implementation are the large number of chained operations and the low rate of data transfers from memory to processing unit. This results directly from using multiple registers in the vector processor.

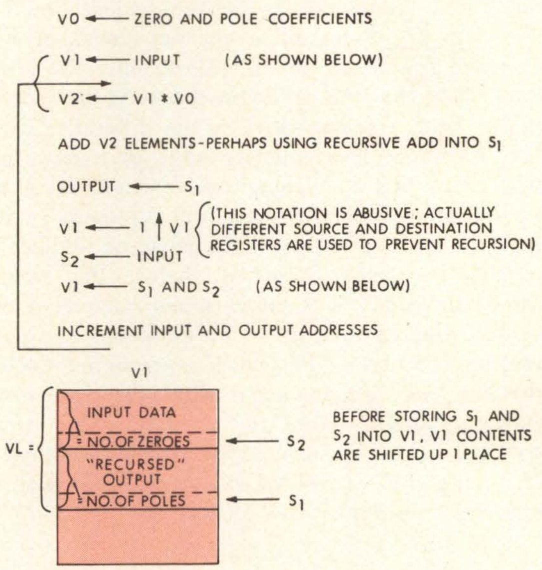

Fig 6 Code for infinite impulse response or recursive filter. A shift of V1 ← 1 ↑ V1 is shown; however, actual code requires ping-ponging between two registers. Code multiplies each input by a zero coefficient and each recursed output by a pole coefficient and sums products for next output

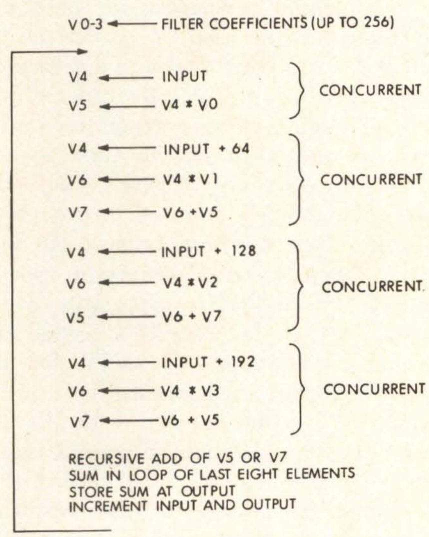

Fig 7 Code for finite impulse response filter. Large number of concurrent vector operations allows a 100-million operation per second execution rate of this code. Each input is multiplied by a coefficient and products are added to form an output

Fig 7 shows that each coefficient is multiplied by an input datum and the products are summed to produce an output.

Fast Fourier Transform Operation

Frequency analysis is generally applied to the filter output signals and is most commonly performed by an FFT algorithm. Figs 8 and 9 show an FFT algorithm similar to the original by Cooley (see Bibliography); however, Fig 9 shows the input amplitude samples on the left. The complicated signal routing and processing required for an FFT are illustrated in two equivalent signal flow graphs, with Fig 9 merely a rearrangement of Fig 8. Outputs and processing are identical; only the order is different. Note that the difference between the indices of successive input signals, which is the difference between memory locations, is usually divisible by a large power of two. Thus, this FFT algorithm tends to have many memory conflicts because there are 16 memory banks in the system. In addition, data must be shuffled into "bit-reverse" ordering (Fig 8), before the algorithm can be performed. Fig 9 shows a rearrangement of the signal flow diagram of Fig 8 with all inputs and outputs in numerical order, which saves rearranging the data; for this flow only, weights occur with subscript sequences that are separated by large powers of two. Operations in the FFT algorithm are all complex, except for those few that have weights of ± 1 or $\pm i = \pm\sqrt{-1}$. For these weights, the "multiplies" are all by ± 1.

FFT Implementation

For the typical FFT algorithm, a number of computationally equivalent procedures exist, some of which are much easier to implement on a vector processor than others (see Gold and Rader). The FFT algorithm shown in Fig 8 requires bit-reverse ordering of input data (left hand indexes), others generate bit-reverse ordered results. For a sequential processor, one of a number of special techniques can be used to reorder the data, such as a table lookup; however, these are not vectorizable, in general. Thus, as shown in Fig 9, the ordered-in, ordered-out FFT implementation is more straightforward. All data are accessed in natural order, in time sequence, and vectors in the processor are relatively long (more than 10 elements). Weights are accessed in groups where the exponents (subscripts, in effect, because the weights are precomputed) differ by large powers of two. In actual implementation, this difficulty is partially overcome by storing a small set of the weights a second time. This duplicate storing of weights is useful for those FFT stages where weights are used repeatedly.

The actual FFT is implemented with the first three stages (shown in Fig 8) done as special cases. In the first two stages, multiplication is not needed, thus saving computation; the third stage is also performed as a special case, because there is only one nontrivial coefficient, $\sqrt{2}$, ie, only one "multiplier" is different from ± 1 and $\pm i$.

By the fourth stage, there are four nontrivial weights, and it is easier to carry out the full multiplication. However, notice that the weights are used eight times over for 64-element vectors. Thus, the multiplication requires: (a) vectors of length eight, (b) serial fetching of weights and storing them repeatedly into a vector register, or (c) a block of weights repeated eight times. Because only a few weights are used in this stage, the solution is to repeat a few of the weights eight times and to use this set of repeated weights for the next two stages as well.

Memory accesses whose addresses are multiples of four proceed at full speed, thus the use of four times as many weights as necessary, each repeated eight times, allows all processing to be vectorized and all vector lengths to be a multiple of 64. With this scheme, the extra or repeated weights are used for the fourth, fifth, and sixth stages.

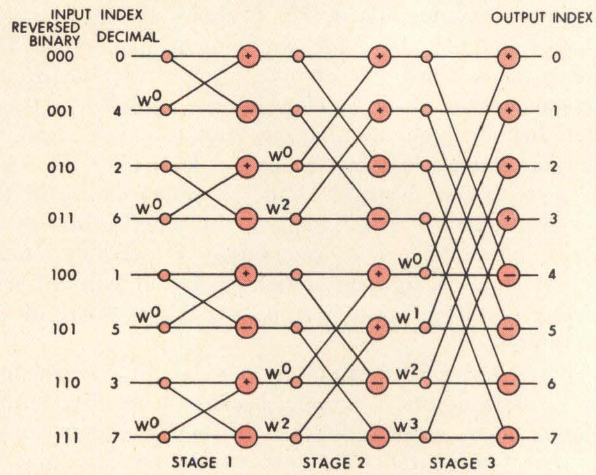

Fig 8 Original FFT signal flow diagram. Input indices differ by large powers of 2, producing frequent memory conflicts. For 2^n-point FFT, input indices differ by 2^{n-1} for every other pair of inputs, where w = 4th root of 1 = $e^{2\pi i/4}$

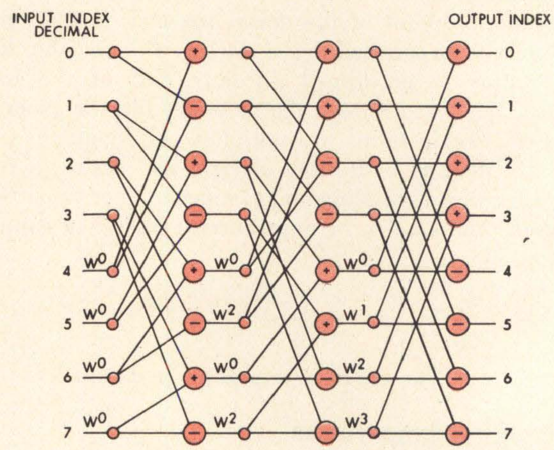

Fig 9 FFT with ordered-in, ordered-out arrangement. Inputs and outputs are in easy memory access locations and no preshuffling of data is required, where w = 4th root of 1 = $e^{2\pi i/4}$

FORTRAN Usage

A FORTRAN programmer coding for a vector processor can take advantage of a number of possible techniques to increase code vectorizability. Loops that have all result names different from the operand names are likely to be vectorized by all FORTRAN compilers. Beyond this, compilers will vectorize depending on their sophistication and on the relative speeds of vector and scalar operations, which determine the importance of vectorization. For example, vector computer systems with poor short vector performance are more likely to have compilers that interchange program loops so that vector lengths are maximized; on vector-scalar computers this is not generally necessary. In any program, vectorizing compilers will attempt to code inner loops of programs as vector operations.

The following list presents inner loop constructs in order of increasing difficulty (approximately) for vectorization by compilers.

(1) Same variable names as operands and results
(2) Complicated subscript expressions
(3) Loop increments other than 1
(4) Functions with mixture of vector and scalar arguments, such as ATAN2 (X, Y(I))
(5) Scalar temporaries in loop
(6) Dependent or ambiguous subscripts
(7) Transfer out of loop
(8) Forward transfer in loop
(9) Subscripts defined before a numbered statement before a loop, yielding possibly nonlinear recursion, as

```
      IONE = 1
        .
        .
        .
50    CONTINUE
        .
        .
        .
      DO 100 I = 1, N
100   A(I) = A(I + IONE) * . . .
```

(10) Subroutine calls in loop (other than ones that are known to the compiler to be vectorized)
(11) Transfer into loop
(12) Backward transfer in loop

In item 9, the compiler cannot easily know whether the loop is nonlinearly recursive and, therefore, nonvectorizable.

Currently, the CRAY-1 FORTRAN compiler, (CFT), vectorizes loops that include items 1 to 5 and in some cases item 6. At this time, CFT generally produces better code for a few large loops rather than many small ones because there are only a few loop "overheads" instead of many. CFT recognizes common subexpressions and uses registers to avoid recomputation wherever possible. Using vector temporaries reduces speed by requiring more memory references; thus

```
      DO 100 I = 1,200
      TEMP(I) = A(I) * B(I) * SQRT (SIN (A(I) + K))
      X(I) = TEMP(I) + 1.0
200   Y(I) = TEMP(I) - 1.0
C     This code sets Xi = Ai*Bi*√sin(Ai+k) + 1 and
C     Yi = Ai*Bi*√sin(Ai+k) -1 for i=1,2, . . . 200.
```

will execute more slowly than:

```
      DO 100 I = 1,200
      X(I) = A(I) *B(I) * SQRT(SIN(A(I) + K)) + 1.0
100   Y(I) = A(I) * B(I) *SQRT(SIN(A(I) + K)) -1.0
C     The same result as the previous case
```

The compiler will compute the common subexpression only once in either case but, in the second, it does not store this temporary result, resulting in faster execution.

Summary

Several signal processing algorithms and their implementations on a powerful vector-scalar processor have been described. Vector-scalar supercomputers are ideally suited to digital signal processing because of the very high processing rates that are required in scientific and industrial applications. These applications presently include energy, weather, and timesharing computations.

Because of tremendous speed requirements for vector signal processing applications, a final recapitulation of operating speeds for a vector-scalar supercomputer follows. Measurements are in millions of floating-point operations pei second. Only required operations are counted; those needed by hardware or software are not included.

Operation	CRAY-1 Speed, MFLOPS
FFT	75
Nonrecursive filter	100
Recursive filter	60
Matrix multiply	140
Dot product	75
Constant Q interpolation	35
Search largest	30M compares/s

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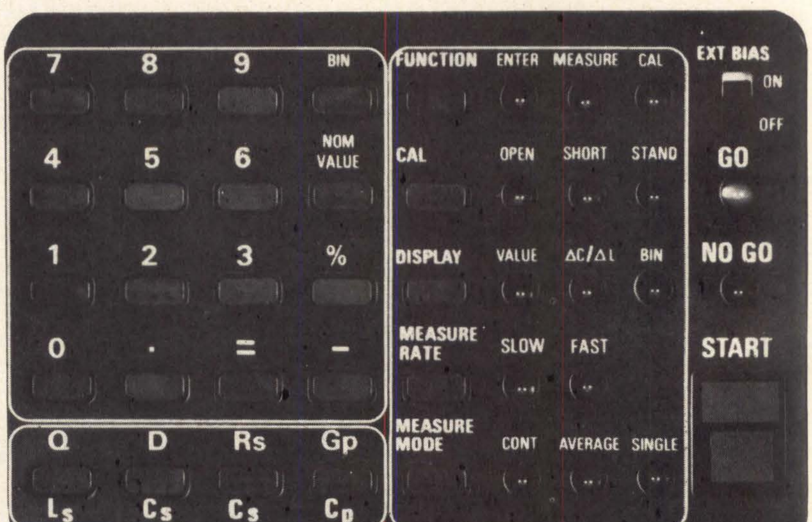

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DESIGN NOTE

Digital Display of Stepper Motor Rotation

Incorporating readily available ICs, a low cost, highly accurate, digital logic circuit numerically displays both the instantaneous step angle and revolutions traveled by a stepper motor shaft

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Since a stepper motor is a discrete motion device that converts a train of digital input pulses into analog output shaft angular-step rotations, a digital display circuit can be readily designed for tracking stepper motor shaft movements. For example, the Slo-Syn™ bifilar-type stepper motor takes 200 steps to complete one shaft revolution—or 1.8 deg/incremental step. By counting the number of input pulses to the stepper motor over a specific time period and using a multiplier constant to accommodate the fixed 1.8-deg step angle, a digital display circuit can easily and accurately track the instantaneous—as well as total—travel angle rotation of the stepper motor shaft.

A simple, flexible, and inexpensive digital display circuit uses versatile and readily available up/down decade counters to read out five binary coded decimal (BCD) digits. Four digits display the travel angle (000.0 to 360.0) in degrees, while the fifth indicates the number of completed revolutions (0 to 9). This stepper motor display can monitor the relatively slow and deliberate movements of incremental plotters, precision film camera drives, and numerical control machines, in general, and can track the precision start-stop motions of fuel control rods within a nuclear reactor, in particular.

Although adaptable to stepper motor applications, commercial digital panel meters are more expensive, have a restricted range of readings, consume high power, and possess limited flexibility. The described digital display circuit overcomes all of these restrictions while operating from a single power source (5 Vdc at 1.2 A).

Circuit Design Requirements

The logic circuit design comprised two main tasks: driving the stepper motor, and measuring and displaying the motor shaft angle rotation. A state generator [Fig 1(a)] has been designed to generate high current waveform pulses and to provide the correct switching sequence for exciting the stepper motor. Input pulses to the state generator can be connected to the output of a square wave generator or a microprocessor, such as the MOS Technology KIM-1. If the latter is used, the speed and direction of motor rotation can be controlled by programming the period and level of the output pulses. Because the KIM-1 input/output pins are transistor-transistor logic compatible, interface circuitry is not needed.

Square wave generator pulses are used as clock signals to trigger a J-K flip-flop (SN7473N), which changes the ON-OFF states of QA1 and $\overline{Q}$A2 or QB1 and $\overline{Q}$B2. The direction of motor step rotation is controlled by the state of input gate G1—a high level for clockwise (CW) rotation and

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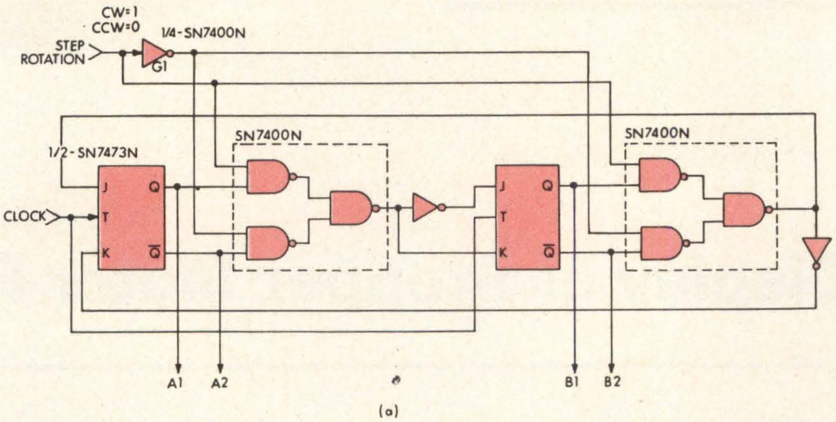

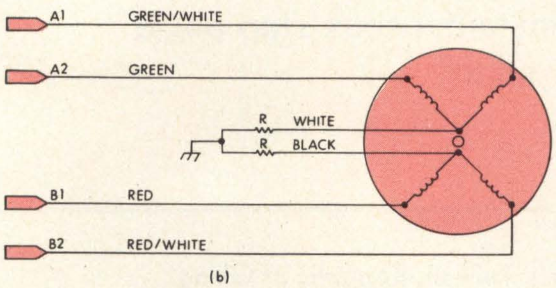

Step Sequence	A1	A2	B1	B2	Binary Code
1 CW	ON	OFF	ON	OFF	1010
2	ON	OFF	OFF	ON	1001
3	OFF	ON	OFF	ON	0101
4	OFF	ON	ON	OFF	0110
CCW 1	ON	OFF	ON	OFF	1010

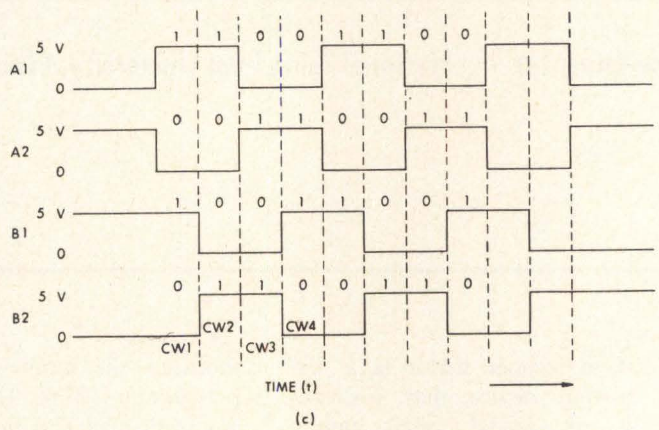

Fig 1 Stepper motor drive requirements. State generator circuit (a) supplies current waveform pulses and switching sequence for exciting stepper motor. Input pulses from square wave generator (or microprocessor) serve as clock pulses that control direction of stepper motor rotation and triggering of J-K flip-flop. In Slo-Syn motor wiring (b), resistance R equals 10 Ω for this application. Ground return can be via chassis or separate wire. 4-step sequence drive (c) is pulse coded for repeating clockwise or counterclockwise rotation

a low level for counterclockwise (CCW) rotation. The stepper motor wiring is shown in Fig 1(b) and the sequence of phase currents is shown in Fig 1(c). All four current combinations are amplified through power stages before delivery to the respective windings of the stepper motor.

Circuit Operation

The digital display circuit (Fig 2) is designed to connect directly to either a square wave generator or a microprocessor. This circuit mounts on a 6 x 11" (15 x 28-cm) printed circuit board and weighs 1.2 lb (0.5 kg), excluding power supply. Complete hardware cost including power supply is less than $20.

Output from the square wave generator or microprocessor connects to the input of monostable multivibrator IC1 for triggering the digital display. The positive-going transition of the square wave drives the motor shaft through a rotational angle of 1.8 deg/pulse, and simultaneously triggers one of the two monostable multivibrators in IC1. A negative pulse—produced at pin 4 $(\overline{1Q})$ of IC1—enables gate 3 (G3) to load the input data into IC3 and IC4. These two programmable up/down decade counters have been previously set in BCD code to $0001\ 1000_2$ (or 18_{10}) for 1.8 deg/step. Gate G4 is enabled by OR gate OR1.

The second monostable multivibrator in IC1 is triggered by the trailing edge of the positive pulse output (T_w) of pin 13 (1Q), which is connected to pin 9 (2A) when pin 10 (2B) is set high. Thus, a positive-going pulse is produced at pin 5 (2Q), which enables gate G1. The values of the resistance-capacitance (RC) circuit between pins 6 and 7, and 14 and 15 of IC1 are selected so that the clock output pulse width (T_w) at pin 13 (1Q) is wide enough to allow a proper timing sequence. For example, if $C = 0.1\ \mu F$ and $R = 10\ k\Omega$, then


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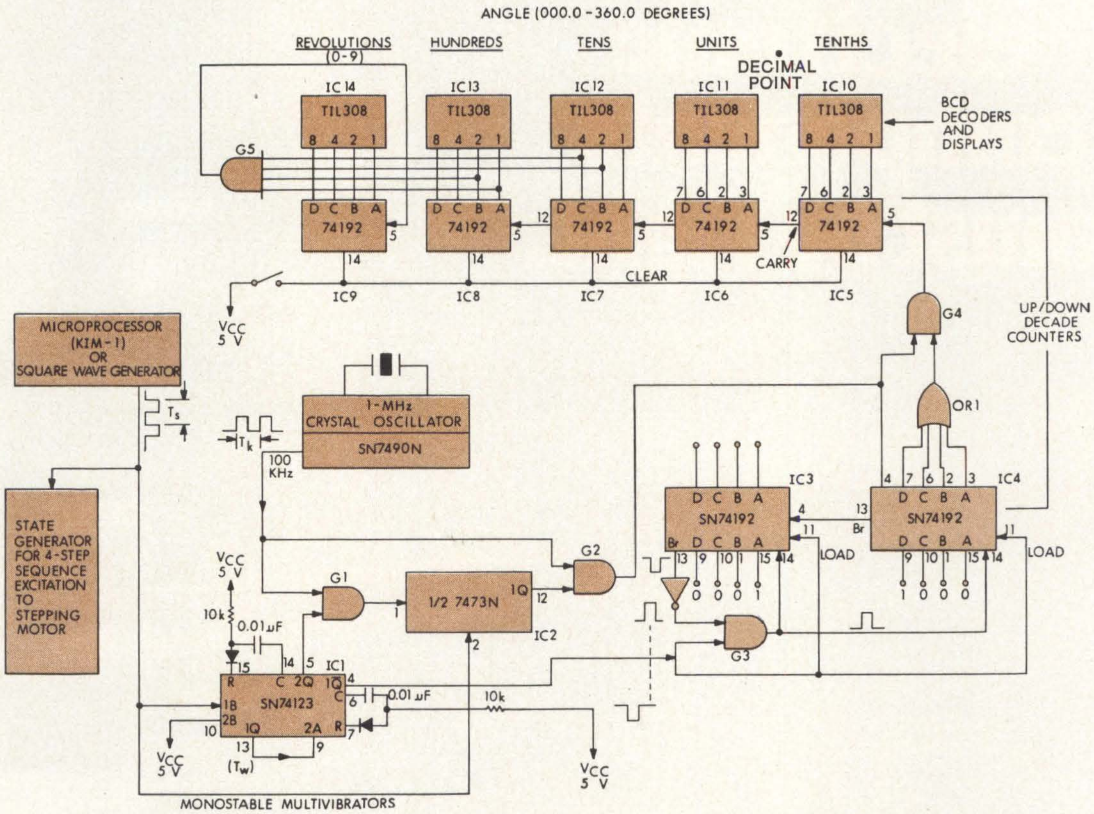

Fig 2 Digital display circuit. Since stepper motor has ±3% accuracy for each step, positional accuracies of ±0.054 deg for 1.8-deg/step case and ±0.027 deg for the 0.9-deg/step case are attainable. Circuit can be used for either open- or closed-loop stepper motor control systems with high accuracy

$$T_w = K \times R \times C \left[1 + \frac{0.7}{R}\right]^{\dagger}$$

where $R = k\Omega$, $C = pF$, $K = 0.32$ for SN74122 or 0.28 for SN74123, and $T_w = ns$.

Therefore,

$$T_w = 0.28 \times 10^5 \ (1 + 0.07) = 3.0 \times 10^4 \text{ ns.}$$

Also, if $C = 330$ pF and $R = 10$ kΩ, then $T_w = 1000$ ns.

Flip-flop IC2 is set by enabling gate G1 coincidently with a clock pulse. In turn, IC2 sets and then resets up/down decade counters IC3 through IC9. Clock pulses are divided down to 100 kHz from the 1-MHz crystal-controlled oscillator and pass through gate G2 to the input countdown of IC4. Then, IC4 starts counting down from 18_{10} ($0001\ 1000_2$) to 0_{10} ($0000\ 0000_2$). However, since gate G4 is enabled by OR1, the clock pulses also pass through G4 to the input of IC5, which starts counting up from 0_{10} to $0001\ 1000_2$ in the opposite direction. Each count is added to the previous value in IC5 through IC9. When the contents of IC3 and IC4 both reach 0 a stop signal (negative pulse) is produced by the borrow (Br) output of the last stage of IC3, which resets IC3 and IC4 through an inverter and gate G3.

Note that AND gate G3 is previously enabled by pin 4 ($\overline{1Q}$) of IC1, while AND gate G4 is inhibited by the output of OR1 as long as the content of IC4 is 0. Furthermore, when the square wave input is negative-going, gates G1 and G2 are inhibited by the output of IC1 (pin 5) and IC2 (pin 12). This guarantees that up/down counters IC3 through IC9 are completely stopped and that the circuit is reset to initial conditions. The circuit starts counting again when the square wave output is positive-going.

The decimal point is set at the left of the first digit of BCD decoder

†*The TTL Data Book for Design Engineers*, Texas Instruments, Inc, pp 21-33, 138.

IC10 (least significant digit). Thus, the readout display shows an increment of 1.8 deg for each rotational step of the motor shaft. After 200 steps, the rotor has moved one complete revolution, and all the step increments are summed by the circuit to display 360.0 deg.

A carry is produced by AND gate G5 for IC9 when IC13 and IC12 read 36, which adds one count to the previous revolution's value. The maximum display for the circuit of Fig 2 is nine revolutions plus 358.2 deg. Circuit response can be expanded if necessary. Data input into IC3 and IC4 can be changed or preset accordingly as the angle per step of the stepper motor is changed.

Since the stepper motor's rotational speed is relatively slow, typically 100 steps/s, system operation is possible as long as the following condition is met:

$$T_s \geq m\, T_k + T_w$$

where

T_s = time period of output square wave from signal generator or microprocessor

T_k = time period of clock pulse from crystal-controlled oscillator

m = number of pulses equivalent to integer value of rotational angle per step (step angle) of stepper motor. For example, when step angle = 1.8 deg, m = 18; when step angle = 0.9 deg, m = 9.

T_w = pulse width produced at pin 13 of IC1 for triggering IC2. For example, if $T_k = 10\ \mu s$, then m = 18 for 1.8 deg/step, and T_w = 30,000 ns or 30 μs. Therefore, the period (T_s) of the output square wave from the signal generator must be equal to, or greater than, 210 μs.

Summary

A factor that may cause display of incorrect readings is that in open loop schemes the total number of steps taken by the motor may not equal the total number of pulses supplied to the stepper motor drive. In this case, the starting and stopping rates should be carefully studied and should not be operated out of the normal range, which is 100 to 400 steps/s. □

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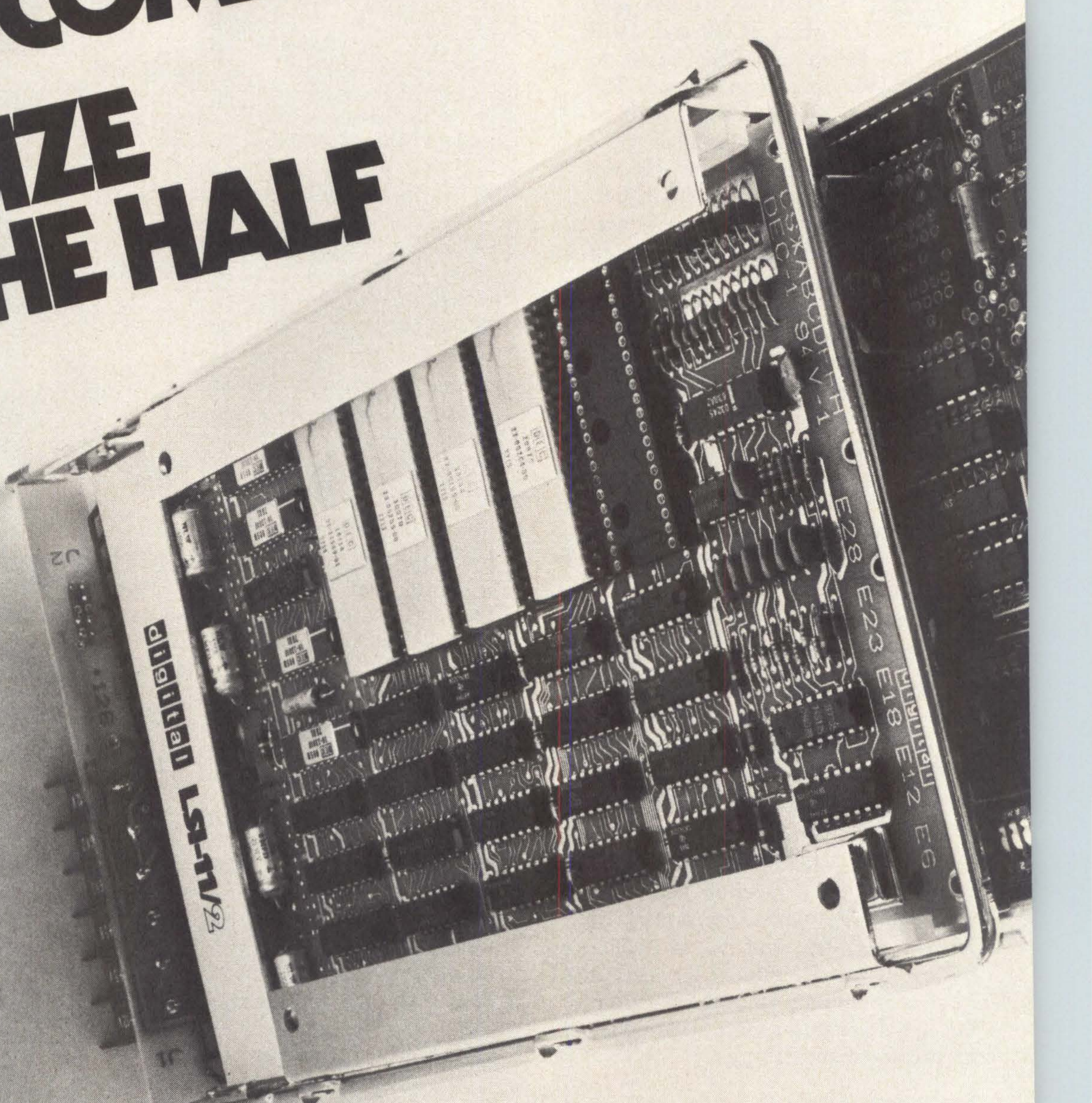

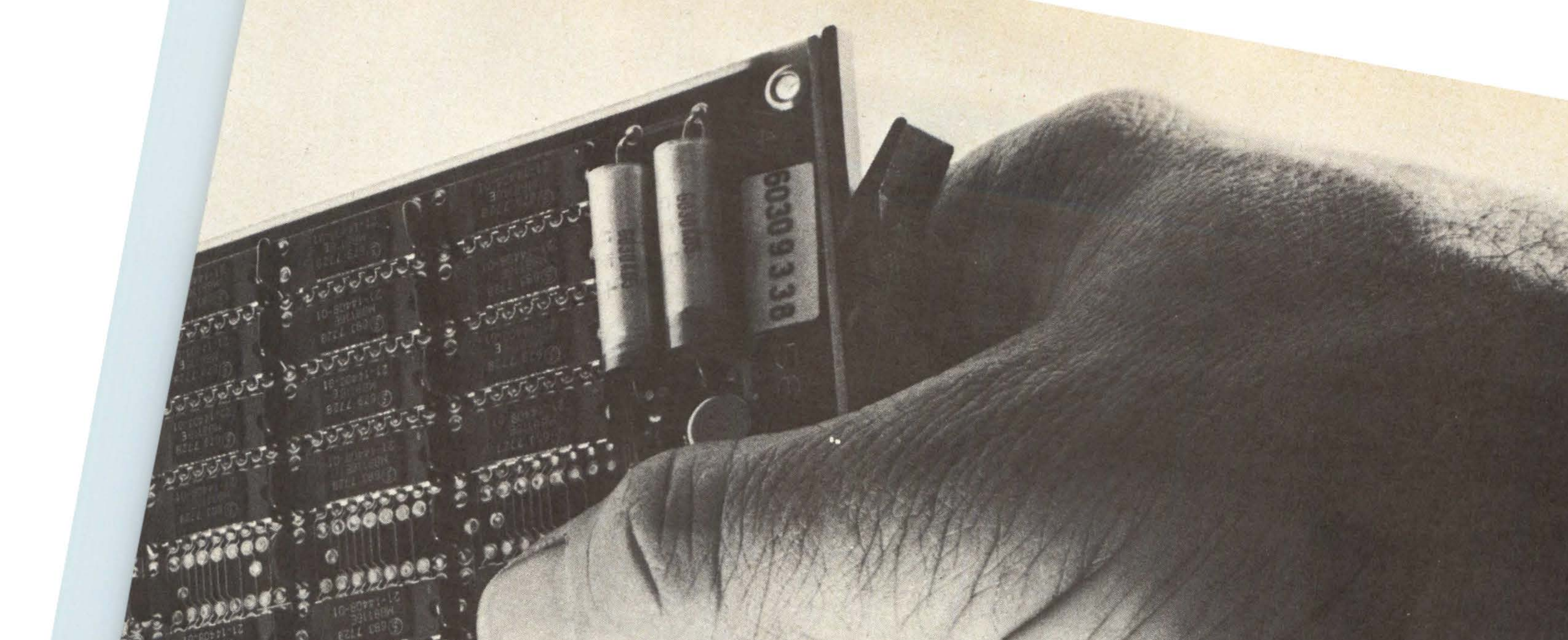
digital

One-Step Programmable Arbiters for Multiprocessors

When processors in a multiprocessor system demand service from a shared bus in an asynchronous mode, a synchronous state arbiter resolves conflicts and allocates resources. Independent of the combination of requests, only one state transition is required from a free to an allocated resource with arbiter structure and priority rules programmed into state machine memory

K. Søe Højberg Risø National Laboratory, Roskilde, Denmark

In a parallel system, two or more devices may simultaneously request use of a shared resource. During the time that one request is being handled and the second is waiting, others may appear. Thus, it is necessary to resolve request conflicts and to allocate the shared resource according to priority rules. Plummer[1] describes a multirequest arbiter with asynchronous logic. Many serial events in port and priority networks are involved in a request-to-grant transaction. Pearce,[2] et al, describes a multirequest arbiter tree based on asynchronous logic arbiter modules. A request-to-grant transaction causes signal flow through at least two basic modules. Ref 3 describes a synchronous arbiter with request-dependent speed, including examples such as a hardwired structure with fixed priority rules.

In this synchronous state-machine arbiter, structure and rules are programmed into permanent or semipermanent storage [read-only memory (ROM) or programmable read-only memory (p/ROM)], or into a random-access memory (RAM) which can be changed dynamically. Since digital computer simulation of a state machine is straightforward, design and verification procedures for the arbiter can be simplified.

Functional Principles

The arbiter [Fig 1(a)] consists of a memory and input and output latches. One or both latches may be integrated with the memory in a chip. Device i requests the shared resource by raising its request line R_i [Fig 1(b)], where $i = 1 \ldots n$. Devices initiate requests only when grant line G_i is low. The arbiter allocates the shared resource to requesting device i by raising its grant line, G_i. When device i has finished using the resource, it resets its request line, R_i, which causes the arbiter to reset the corresponding grant line, G_i.

Arbiter states can be divided into grant and wait states. During static conditions, no grant is issued in a wait state and one grant is issued in a grant state. Request input signals in addition to the next state number are stored in latch 1 until a clock 1 impulse occurs. In the arbiter diagram [Fig 1(a)], internal requests and grants (for instance $\mathbf{R}_1$ and $\mathbf{G}_1$) are in boldface* for easy identification. Outputs from latch 1($\mathbf{R}_1 \ldots \mathbf{R}_n$ and P) are used as an address in memory. In this manner, the memory address is well-defined, independent of fluctuations in asynchronous request inputs and memory outputs.

One byte of the addressed memory cell is used for storage of the next state number, N, which can be implemented by binary representation. Another byte contains the grant information $\mathbf{G}_1 \ldots \mathbf{G}_n$. A 1 bit represents a grant for a corresponding request/grant channel. At most, one grant is present. At a clock 2 impulse, the grant byte is stored in latch 2. Fluctuations initiated at memory addressing time, clock 1, can be avoided at grant outputs by proper separation of clock 1 and 2 impulses.

In Fig 1(b), it is assumed that no requests are initially present. Shaded areas of R_i and R_{i+1} between succeeding clock 1 impulses indicate possible request arrival or departure times with identical grant responses. Note that, on the average, only one clock 2 period is required for setting or resetting a grant G_i. Detection of request R_i occurs at the first clock 1 impulse following the request transition from logic level 0 to 1. At the succeeding clock 2 impulse, grant G_i is issued. When request R_i arrives within the same clock period as another request (eg, R_{i+1}), the request having the highest priority (R_i) is honored with a grant. If a request (R_{i+1}) is waiting when a grant is released, a new grant (G_{i+1}) is issued after one clock period only. If more than one request is waiting, the highest priority request releases a grant.

A set of priority rules is established for conflict cases described above, as well as for single-request and no-request cases. On this basis, the state transitions grant-to-wait and wait-to-grant are described. The arbiter uses a table that is set up for determining the next state number N as a function of input and present state number P [Fig 1(a)].

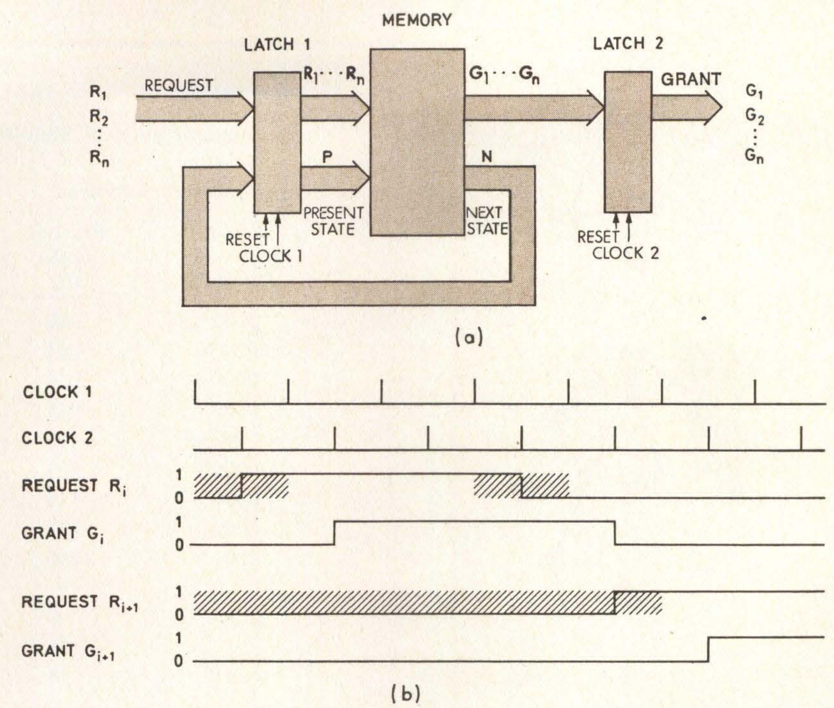

Fig 1 Asynchronous arbiter implemented as synchronous state machine. In (a), $R_1 \ldots R_n$ are request lines and $G_1 \ldots G_n$ are grant lines connected to devices 1 . . . n. In (b), device initiates requests by issuing logic 1 signal on request line. Arbiter allocates resource to device by answering with logic 1 signal at corresponding grant line. Grant is reset and resource released by device when logic 0 signal is issued on request line. Shaded areas indicate possible request arrival or departure times with identical grant responses

Arbiter Example

A ring priority arbiter with four request/grant channels serves requests around a ring structure. Advantageously, no single request can prevent others from getting service by continually setting up requests. A grant state is assumed for each request/grant channel, and a wait state is needed when no requests are present. In a ring priority wait state, the arbiter must remember which grant has just been served by introducing a specific wait state for each grant state. The number of states (Q) is then $Q = 2C$, where C is the number of request/grant channels. Wait states are designated by even numbers (0, 2, 4, and 6), while grant states are odd numbered (1, 3, 5, and 7). Corresponding request and grant signals 1, 3, 5, and 7 are denoted by R_1, R_3, R_5, and R_7 and G_1, G_3, G_5, and G_7, respectively.

An address in state machine memory (Table 1) is composed of the present state number in binary representation and a sampled request byte that includes one bit for each request input. The addressed memory cell contains the corresponding grant to be sampled and the next state to be entered. All combinations (in the example, 128) of request and present state signals should be listed to serve as memory addresses; remaining addresses can be evaluated by comparing any possible address with the corresponding request bit pattern and source state number in Fig 2. If the next state is identified as a grant state, the corresponding grant bit is set to logic 1. Fig 2 shows the state diagram resulting from the application of rules established here.

In Fig 2 wait states are described by shaded circles, grant states by nonshaded circles. Lines going from circle to circle indicate state transitions. Note that source and destination states for a transition can be identical. Fig 2(a) shows all possible

*Boldface **R** or **G** denotes an internal signal that is nearly equal to R or G, respectively, only displaced in time.

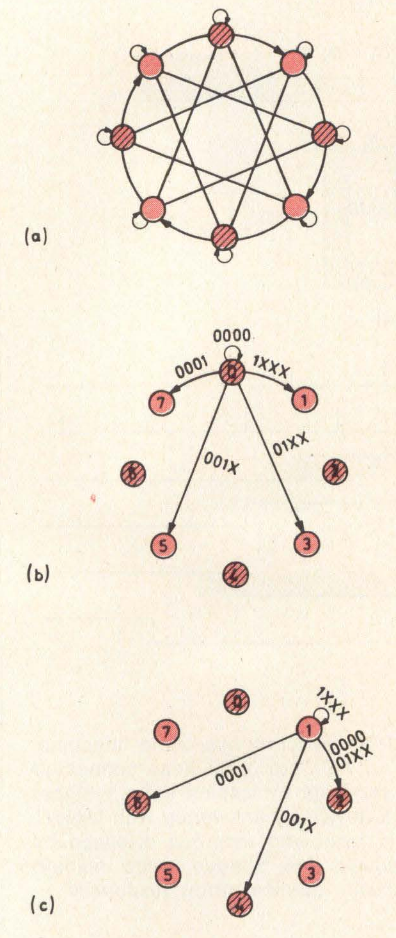

Fig 2 Ring priority arbiter. In (a), all state transition paths are shown. Parts (b) and (c) show departures from wait state and grant state, respectively. Corresponding request bit patterns are specified on transition lines—X indicates 0 or 1. Multirequest patterns detected in wait state lead to selection of first corresponding grant state met by following circle in clockwise direction

TABLE 1

Determination of State-Machine Arbiter Memory

Memory Address		Memory Content		
Sampled Requests ($R_1R_3R_5R_7$)	Present State (P)	Preliminary Grants ($G_1G_3G_5G_7$)	Next State (N)	
0000	000	0000	000	
0000	001	0000	010	
0000	010	0000	010	
0000	011	0000	100	
0000	100	0000	100	
0000	101	0000	110	
0000	110	0000	110	
0000	111	0000	000	
0001	000	0001	111	
•	•	•	•	128 − 10 = 118 states
•	•	•	•	
•	•	•	•	
1111	111	0001	111	

TABLE 2

Memory Requirements for Ring-Priority State-Machine Arbiter

Request/Grant Channels	Memory Words	Memory Word Length
2	16	4
3	64	6
4	128	7
5	512	9
6	1024	10
7	2048	11
8	4096	12

state transition paths. Unidirectional paths are marked with arrows. Figs 2(b) and (c) illustrate ring priority rules. State transitions are divided into two groups: departures from wait states [Fig 2(b)] and departures from grant states [Fig 2(c)]. For clarity, only one source state with transitions is shown in each figure. Numbers inside the circles are decimal state numbers. Numbers on state transition lines are binary request bit patterns. The most significant bit in a pattern indicates the logic level of request R_1, while the least significant bit represents request R_7. A request bit with no influence on a transition is denoted by X.

If the present state is a wait state [for instance 0 in Fig 2(b)] and at least one request is at logic 1, the first corresponding grant state found by moving clockwise around the circle is entered. "Corresponding" means that the new state number (1, 3, 5, or 7) is equal to the index of one of the requests given. For instance, grant state number 1 is entered if $R_1 = 1$, regardless of the level of other requests; grant state number 3 is entered if $R_3 = 1$, while $R_1 = 0$, $R_5 = 0$ or 1, and $R_7 = 0$ or 1, etc. If all requests are logic 0 in a wait state, the state is not changed.

When the present state is a grant state [Fig 2(c)] and the request corresponding to the grant state is at logic 1, no state change is made. If this request, however, is at logic 0, the first feasible wait state found by moving clockwise around the circle is selected. As an example, the present state is assumed to be number 1, a grant state. When the request with

index 1 disappears ($R_1 = 0$), a transition to a wait state takes place in the following way. If all requests are at logic 0, the present state number plus 1 (in the example, state 2) is selected. If a request is at logic 1, a corresponding grant state number minus 1 is used. Thus, if $R_1 = R_3 = 0$, $R_5 = 1$, and $R_7 = 1$, grant state number 5 is used as a basis as it precedes number 7 on the circle. Thus, the wait state destination becomes $5 - 1 = 4$. The same principle applies for the other transition lines in Fig 2(c). By using a temporary wait state in this way, a proper time spacing is ensured between grants. When the next state number N becomes a grant state number, a corresponding grant G_N is issued immediately. Since the next state is used as a basis for grant issue, rather than the present state, one clock period of delay is avoided by setting or resetting a grant.

Memory capacity requirements for two to eight channels are given in Table 2. In essence the number of memory words increases exponentially with the number of request/grant channels. In general, an arbiter with a certain number of channels can also be applied to a decreased number of channels by setting inputs to logic 0.

Conclusion

The type of arbiter described is well suited as a bus controller in a multiprocessor system. Safe transition from one grant to another is obtained by the introduction of intermediate pause states. In this way safety margins can be increased simply by clock frequency adjustments. To summarize, the described method for implementation of asynchronous arbiters by synchronous techniques can lead to reliable and flexible systems.

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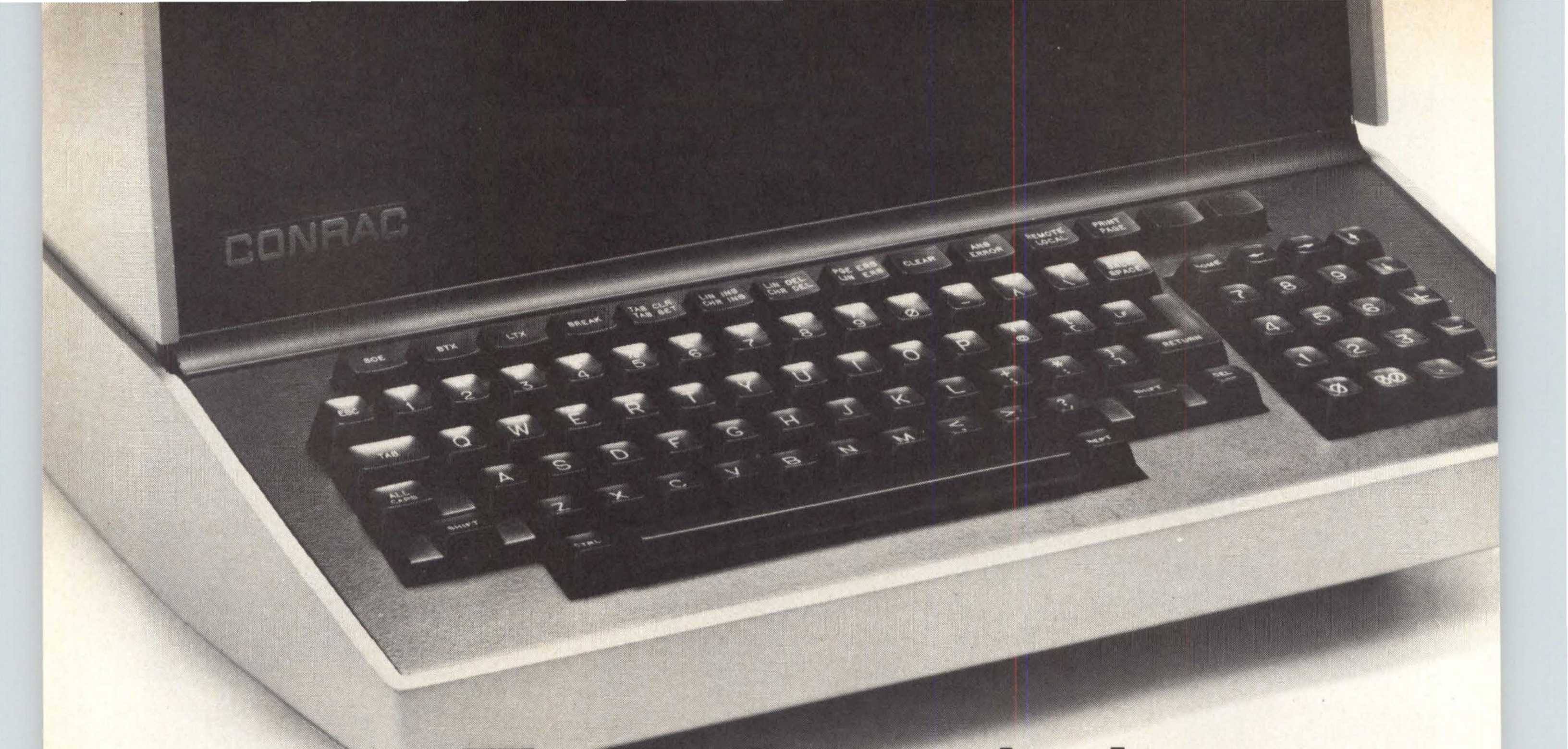

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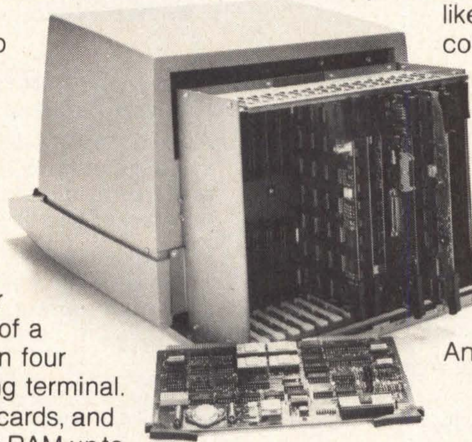

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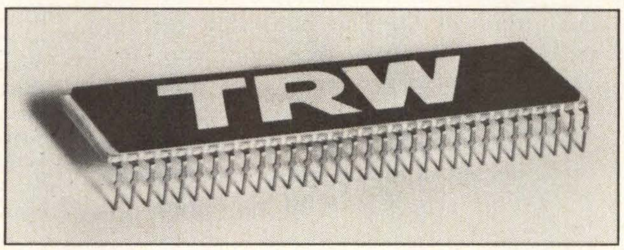

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Hybrid Digital-Analog Implementation of Digital Filters

Lower precision allows higher speed

This hybrid device is a modification of a counting digital filter (see *Computer Design*, Feb 1978, p 132) permitting a new set of tradeoffs. The speed of the counter in the filter is a major design parameter. In the hybrid device, high speed is obtained through lower precision rather than through higher cost. This is mainly effected by substituting an analog device for the digital counter, thus obtaining inherent lower precision.

The device is shown in the Figure, in which the A register holds the filter coefficients a_i. It can be shown that the filtered output sample y_m is given by

$$y_m = \sum_{r=0}^{J-1} h_{mr}(-2)^r$$

in which h_{mr} is simply a count of the TRUE gates in the figure and J is about double the number of bits per word. Each gate controls the analog switch shown below it (closed when TRUE). Switch S_0 feeds the resistor network with a voltage proportional to $(-2)^r$. With h_{mr} of the switches closed, the current through point Q is proportional to $h_{mr}(-2)^r$.

Switch S_0 is synchronized with the shifting of the X shift register, so that all J terms comprising y_m are generated sequentially as currents through Q. The integrator fed by these currents then performs the mathematical operation of summing (accumulating), so that when all J currents have been generated, the voltage at the integrator output point P is proportional to y_m. Switch S_b should then close momentarily, feeding the output low-pass filter with a pulse proportional to y_m.

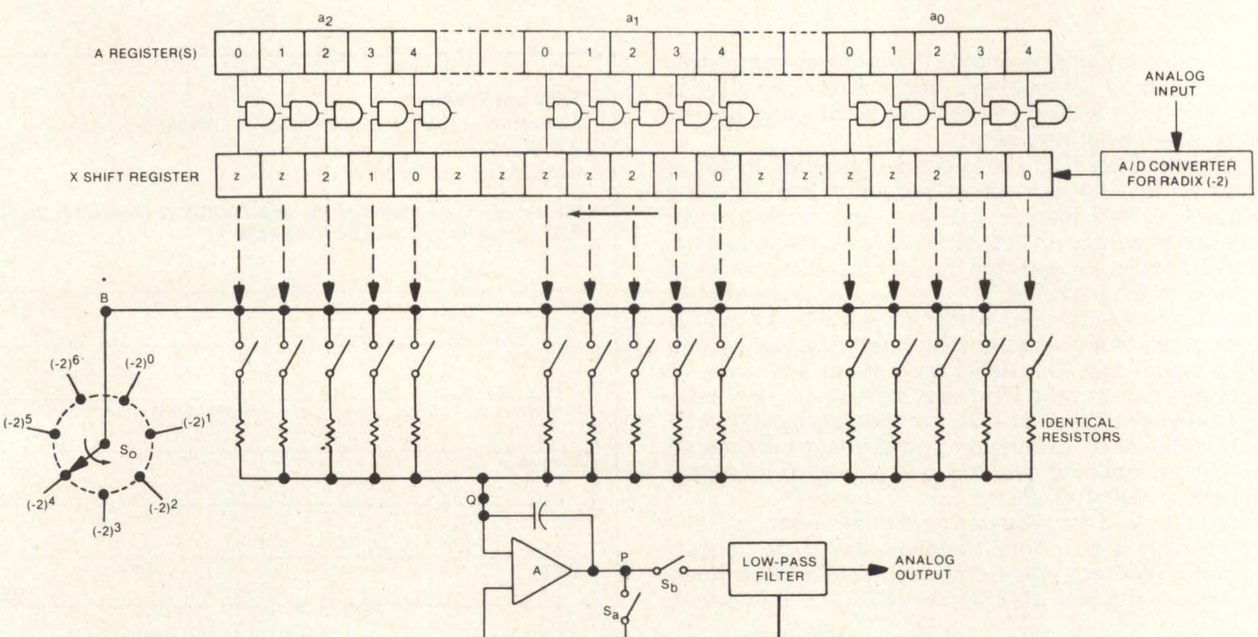
The new cycle for the generation of y_{m+1} starts with the opening of S_b, momentary closing of S_a to discharge the integrator capacitor, and feeding of the new sequence of J currents comprising y_{m+1}.

Note

This work was done by Shalhav Zohar of Caltech/JPL. For further information, write to: John C. Drane, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103.

Patent Status

This invention has been patented by NASA (U.S. Patent Number 3,732,409). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to: Monte F. Mott, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. Refer to NPO-11833.



Filter illustrates general principles of operation. Switches shown refer to logic-controlled semiconductor devices

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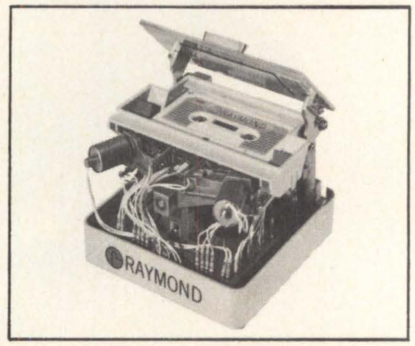

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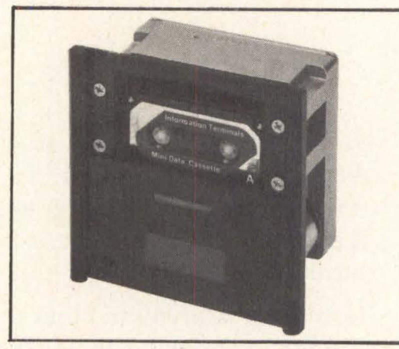

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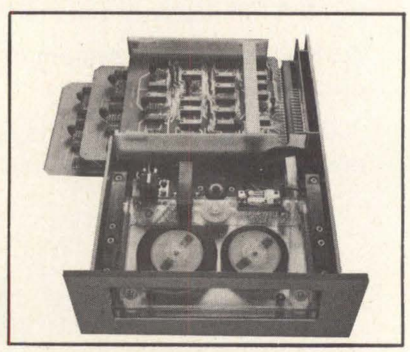

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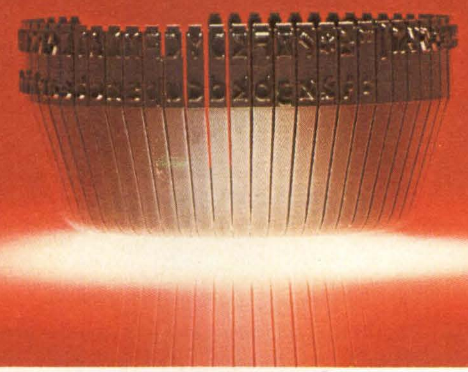

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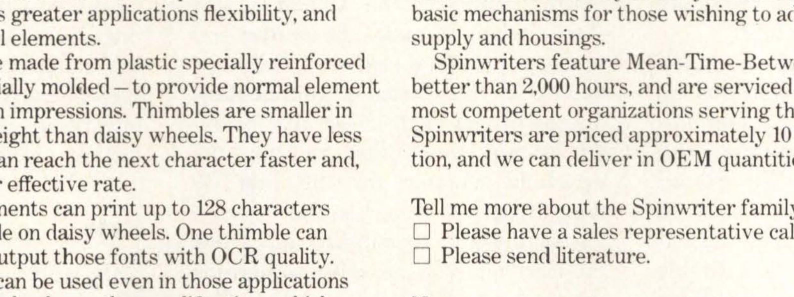

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TECH BRIEF

Signal Processing and Display for Electrochemical Data

A compact and inexpensive system automatically measures metabolic byproducts during micro-organism detection

An electrochemical method for detecting micro-organisms, based on a linear relationship between initial cell concentration and time of molecular hydrogen (H_2) detection, is efficient and accurate, yet it does have drawbacks. In routine use, the recorder is expensive and bulky, and an operator must read and manually record the reaction end point.

A compact and inexpensive signal-processing and display apparatus alleviates these drawbacks by automatically determining the reaction end point and displaying the lag period in hours and minutes or directly in cell concentration. A multiplexed analog signal output, which is suitable for display on a strip-chart recorder or similar device, permits the operator to check out all channels and provides a permanent record of events. The unit can also be interfaced with a computer.

Two electrodes, a standard pH reference electrode and a platinum cathodic electrode, are required by the system. Alternatively a combination redox electrode can be used in a container with a nutrient medium suitable for microbial growth along with the sample to be tested. Samples could be from a variety of sources where interest is in detecting and enumerating the number of micro-organisms (eg, a sample of water for coliforms or a urine sample from a case of suspected urinary tract infection).

Electrodes are connected to an amplifier which provides the required high impedance electrode interface. The amplifier voltage gain is needed to drive the analog-to-digital converter (ADC), the up/down binary counter, and the digital-to-analog resistance ladder. A clock provides operating pulses to the ADC at a rate slow enough to make the system immune to a noise spike. (This low operating rate forms a rudimentary digital filter.) The clock also drives an 80-min timer that inhibits the threshold counter for the first 80 min of operation. This time period allows the ADC to capture and track the electrode voltage and also permits the electrode voltage to stabilize after insertion into the broth medium.

A special electronic circuit was designed to sense and record the end point. A counter determines the equivalent number of digital pulses that correspond to 10 mV of input voltage change. When this time is reached, the signal from the counter reverses the timer, which is started when the broth medium is inoculated with the sample; the timer then runs backward until a count equivalent to 30 mV of electrode voltage is detected by the counter. At this time, the timer stops and displays a time equal to the length of time required for the inoculum to begin the production of measurable amounts of H_2 after inoculation.

Examination of a large number of strip-chart records reveals that the baseline (voltage level after stabilization) occasionally exhibits a slow, steady rise. Such a case can cause the 10-mV counter to reach its count earlier than it would with a flat baseline. To circumvent this problem, a circuit has been added that subtracts one digital count from the 10- to 20-mV counter often enough to prevent the observed nonsteady baseline from adversely affecting the correct detection of 10 and then 30 mV.

Note

This work was done by Richard N. Young and Judd R. Wilkins of Langley Research Center. For further information, write to: John Samos, Langley Research Center, Mail Stop 139A, Hampton, VA 23665.

Patent Status

Inquiries concerning rights for the commercial use of this invention should be addressed to: Howard J. Osborn, Langley Research Center, Mail Code: 313, Hampton, VA 23665. Refer to LAR-11922.

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CIRCLE 89 ON INQUIRY CARD

MICROCOMPUTER INTERFACING: INTEGER ADDITION AND SUBTRACTION

Christopher Titus and Jonathan A. Titus
Tychon, Inc

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

Most 8-bit microprocessors such as the 8080A, Z80, 6800, 6502, and F8 can add and subtract only 8-bit numbers, which represent only those decimal quantities between 0 and 255. This is not enough resolution or dynamic range for many applications; consequently, multiple-precision and floating-point numbers are used. Multiple precision refers to the use of two or more computer words to represent a numeric quantity. In the above mentioned microprocessor chips, a computer word—a byte—is eight bits long. A double-precision number, therefore, contains two bytes, or 16 bits, and can represent any unsigned integer number between 0 and 65,535. Similarly, a triple-precision number contains three bytes (24 bits), representing any unsigned integer number between 0 and 16,777,216. Despite this ability to represent very large numbers, multiple-precision numbers do have their limitations, especially when units such as picograms, liters per second, and kilograms all appear in a single equation.

Floating-point numbers are used frequently for scientific and engineering calculations, because they can represent quantities that vary greatly in magnitude. The term floating-point number refers to a computer quantity that usually is composed of two parts: a mantissa and an exponent. For 8-bit microprocessors, a floating-point number is often represented by a 16-bit mantissa and an 8-bit exponent. Since the exponent and mantissa may be either positive or negative, one bit in each is used as a sign bit. Thus, the 3-byte floating-point number (15-bit mantissa plus sign bit, 7-bit exponent plus sign bit) can represent numbers between $32,767 \times 2^{-127}$ and $32,767 \times 2^{127}$, which correspond to the decimal number range, 1.93×10^{-34} to 5.58×10^{42}. It is quite common for the mantissa to contain an implied binary decimal point, covering binary numbers between 0 and 1.000 or between 0.500 and 1.000.*

Unfortunately, a floating-point package, which is a collection of subroutines that perform addition, subtraction, multiplication, and division of floating-point numbers, is a complex program. The Intel 8080 floating-point package,* written by O. C. Juelich, had its origin in an earlier 8008 floating-point package written by C. E. Ohme; it requires 865 bytes of read-only memory and 24 bytes of read/write memory. Few programmers write floating-point packages, because they are available from computer manufacturers or their respective user's groups.

Integer or fixed-point mathematical programs are relatively easy to write. For 8080A-based microcomputers, the add (ADD) and add-with-carry (ADC) instructions are used to write integer addition subroutines and programs. These instructions are used to add not only 8-bit numbers, but also 16-bit, 24-bit, and larger numbers. The ADC instructions are particularly useful in this regard, since they add the content of the carry bit to the sum of two 8-bit bytes. The carry bit also is either set or cleared as a result of this addition.

A typical triple-precision integer-addition subroutine for an 8080A microcomputer is shown in Example 1. The subroutine adds two 3-byte (24-bit) numbers stored in memory and returns the sum back to memory. When subroutine ADD3 is called, register pair D must contain the memory address where the least significant byte of one of the numbers is stored. The more significant bytes of the 3-byte number must be stored in consecutive memory locations at the next two higher memory addresses. At location ADD3, the C register is loaded with the number

*O. C. Juelich, "Elementary Function Package," Insite™ (Intel Corp User's Library), Intel Corp, Santa Clara, Calif, 1975

EXAMPLE 1

Triple-Precision Integer-Addition Subroutine

```
ADD3,     MVIC     /Load the C register with the
          003      /number of 8-bit bytes to be added.
          LXIH     /Load register pair H with the
          IACC     /memory address where one of the
          0        /arguments is stored.
          XRAA     /Clear the A register and carry
ADDAGN,   LDAXD    /Get one argument into A
          ADCM     /Add the other argument to it
          MOVMA    /Save the result back in memory
          INXD     /Increment one memory address and
          INXH     /then increment the other.
          DCRC     /Decrement the byte count in C
          JNZ      /If the count is nonzero,
          ADDAGN   /perform the addition again
          0
          RET      /Otherwise, return from the subroutine
```

EXAMPLE 2

Triple-Precision Integer-Subtraction Subroutine

```
SUB3,     MVIC     /Load the C register with the
          003      /number of 8-bit bytes to be
                    subtracted.
          LXIH     /Load register pair H with the
          IACC     /memory address where one of the
          0        /arguments is stored.
          XRAA     /Clear the A register and carry
SUBAGN,   LDAXD    /Get one argument into A
          SBBM     /Subtract the other argument from it
          MOVMA    /Save the result back in memory
          INXD     /Increment one memory address and
          INXH     /then increment the other.
          DCRC     /Decrement the byte count in C
          JNZ      /If the count is nonzero,
          SUBAGN   /perform the subtraction again
          0
          RET      /Otherwise, return from the subroutine
```

of bytes that are to be added, in this case, three. Register pair H is then loaded with the memory address where the other 24-bit number is stored. The first of the three memory locations used for this storage is assigned the symbolic address IACC (integer accumulator). It should be noted that it is always possible to use a group of consecutive bytes in memory to create a multibyte accumulator, which contains one of the operands and in which the final result of an arithmetic or logical operation is stored.

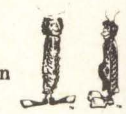
The next instruction that the 8080A executes, XRAA, clears the carry to a logic 0. This instruction must be included in the subroutine since there is no way of knowing what the state of the carry is when the subroutine is called. Otherwise, the carry from some previous operation might be added into the 24-bit result.

At ADDAGN (add again), a single byte is moved to the A register from the memory location addressed by register pair D. The content of the memory location addressed by register pair H is added to the content of register A, and this result is copied into the memory location addressed by register pair H. Both register pairs D and H are then incremented by 1 with the aid of the INXD and INXH instructions, respectively. The byte count contained in the C register is decremented by 1.

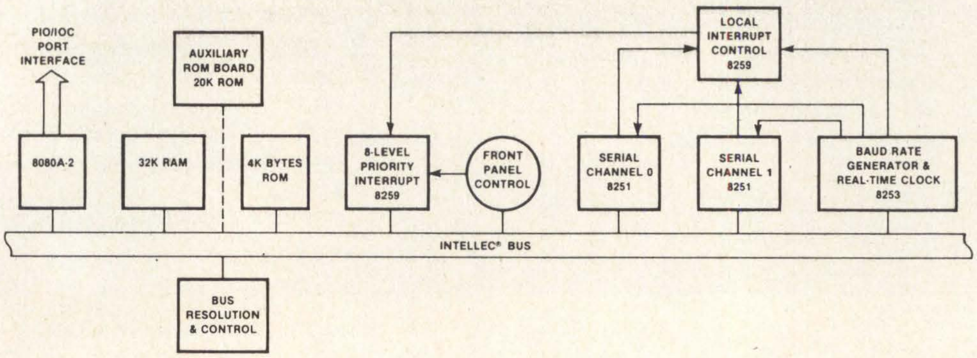
When the content of register C is decremented to 0, the 8080A returns from the subroutine. If the content of that register is not 0, the 8080A jumps back to ADDAGN and adds the next two bytes in sequence. The XRAA instruction is used to clear the carry to a logic 0 only when the subroutine is first called. Subroutine ADD3 can be easily modified to add a 4-, 7-, or even a 200-byte number simply by changing the immediate data byte of the MVIC instruction. Of course, if 4-byte numbers are to be added, a 4-byte integer accumulator must be provided to store the accumulated result.

A triple-precision integer-subtraction subroutine program for an 8080A microcomputer, listed in Example 2, is almost identical to that given in Example 1; the ADCM instruction in Example 1 is replaced by SBBM. The content of the integer accumulator is subtracted from the content of memory addressed by register pair D, with the result of the subtraction stored in the integer accumulator. In the succeeding column, integer multiplication and division subroutines will be analyzed. A later column will describe the application of these subroutines to smoothing or filtering of data acquired from an analog-to-digital converter.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.



Series of Fully Integrated Microcomputer Development Systems Covers Wider Range With Improved Price/Performance



IPB board contained in Intel's family of Intellec Series II microcomputer development systems contains major components. Serial channels are RS-232 compatible, capable of running asynchronously from 110 to 9600 baud and synchronously from 150 to 56k baud. Second board handles remainder of system I/O activity for all three systems, and holds UPI-41 peripheral controller for interfacing with printers, paper tape readers/punches, and p/ROM programmers

The Intellec[R] Series II is a family of compatible microcomputer development systems that provide a wide range of capability from a low cost ROM-based software development system to a high performance floppy disc-based system. Enabling hardware and software development coverage to be implemented as early in the development cycle as possible, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 has created the systems to support a variety of that company's microprocessors; in addition, the systems will support new microprocessors as they are introduced.

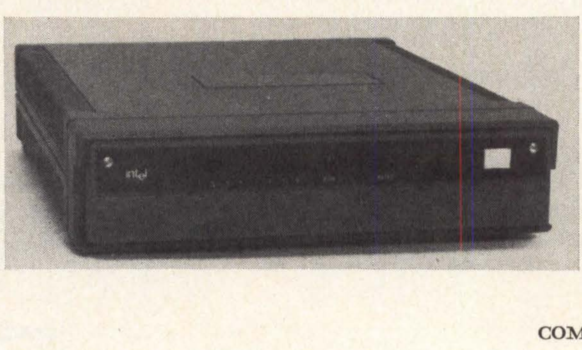
The three models feature modular configurations, allowing the user to choose the system that best meets price, performance, and throughput needs. As these needs expand, the systems can be upgraded easily. They are all compatible with standard Intellec/iSBC expansion modules, and are software compatible with previous Intellec systems. They also implement the standard Multibus™ with multiprocessor and DMA capabilities.

At the low end of the product line, the model 210 is a fully supported system providing hardware and software support for development of products based around the MCS-80 and 85; with optional software, the capability can be extended to MCS-48 based products. The 4" (10-cm) tabletop chassis holds the 4-slot card cage, power supply, and two PC cards.

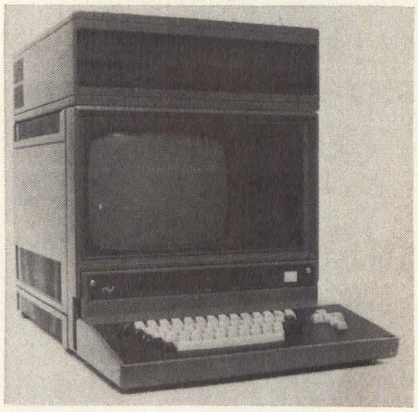
Located on the integrated processor board (IPB) is an n-MOS 8-bit 8080A-2 microprocessor; 32k bytes of RAM; 4k of ROM, preprogrammed with system bootstrap, self-test diagnostics, and system monitor; 8-level vectored priority interrupt system; and the company's 8259 interrupt controller. The I/O subsystem consists of two serial channels on the IPB card, as well as additional interface logic on the parallel I/O board (PIO), which is mounted on the rear panel. The ROM-based editor/assembler combination allows development of microprocessor programs in RAM, thus minimizing usage of paper tape.

Integrated into one package for medium-scale development, the model 220 includes the same IPB. The chassis holds a 2k-char CRT, 6-slot card cage, power supply, fans, cables, single 256k-byte floppy diskette drive, and two PC boards. A detachable full ASCII keyboard with cursor controls and upper/lower case capability is attached with a cable.

The second card is a slave CPU, responsible for all remaining I/O control, including the CRT and keyboard interface, and floppy disc. Mounted on the rear panel, this I/O controller (IOC) also contains its own microprocessor, RAM, ROM, and I/O inter-



Low cost, 4-slot chassis model 210 is minimum system required for rapid development of microcomputer software. Built-in interface allows connection to user's terminal. Option permits upgrading to diskette-based system



Integral CRT, 64k bytes of RAM, and 1M bytes of online data storage with dual floppy discs are incorporated in Intel's model 230 with detachable keyboard. System has access to operating system, system monitor, and software to combine all tools necessary for comprehensive software and system microprocessor-based development work

face, thus creating a dual processor environment. The IPB and IOC cards communicate over an 8-bit bidirectional data bus.

ISIS-II diskette operating system with relocating 8080/8085 macro assembler, linker, and locater allows this system to be used to debug and assemble programs for the MCS-80, 85, or 45 families without the need for handling paper tape; it performs all file handling operations. The system also interfaces directly to the company's in-circuit and "in-system" emulator modules.

Most powerful member is the model 230. Similar to the 220 with the LSI IPB and IOC cards, this unit in addition has 64k bytes of RAM and a second chassis (stacked vertically) containing two floppy disc drives along with a separate power supply, fans, and cables. Capable of double-density operation, the drives can store 1M bytes (expandable to 2.5M). Two additional boards in the card cage are used to control the drives. Designed for the 80, 85, and 48 families, the system also uses ISIS-II software. It supports PL/M-80 and FORTRAN-80 languages, as well as a line of macro assemblers, thus providing access to all necessary software and system development tools.

In-circuit emulator modules (ICE™) provide a design tool that allows debugging of system software in real time, in the hardware prototype environment, while using debug aids built into the host system. It allows symbolic debugging using actual program labels. Modules are available for the 8080, 8085, 8048, and series 3000 systems. ICE-85 external trace module captures trace information of 18 external signals for true in-system emulation.

Prices for the three models are $3250, $7450, and $12,900, respectively. Available peripherals include a 4-slot expansion chassis, two printers, two diskette-based peripherals, 200-char/s paper tape reader, universal p/ROM programmer, enhancement kit for upgrading the 210 to a 220, and any of the Multibus expansion boards. Software, documentation, and membership in the INSITE™ User's Library are standard support offerings.
Circle 420 on Inquiry Card

Bus Compatible 64k RAM Board Conserves Space

Compatible with Intel's SBC 80/10 backplane, the 10046 64k RAM board is a direct replacement for four Intel or National Semiconductor 16k boards, freeing space for boards with other functions. It provides all logic and circuitry to perform accessing, reading, writing, transparent refresh, time out refresh, and DMA. Access time is 475 ns and refresh is 650 ns.

GSI Systems, 223 Crescent St, Waltham, MA 02154 will supply two serial I/O ports for RS-232-C or current loop interfaces. Required voltages are ±5 and ±12 Vdc. The board can be strapped for 16k operation.
Circle 423 on Inquiry Card

Microprocessor Gains 2's Complement Multiply And Divide Capability

Capability added by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086 to the second-generation Am2903 4-bit bipolar microprocessor eliminates the need for additional hardware for signed or unsigned multiplication, and performs signed division using a nonrestoring algorithm. Containing logical and arithmetic shifts, the device can perform normalization on single- and double-length words, and automatically converts between sign-magnitude and 2's complement notation. It can increment by 1 or 2 on a single cycle and has internal parity generation.
Circle 424 on Inquiry Card

Microcomputer Series Expands To Add Control Unit

Designed as a low cost/high volume control unit, the MN1403 is a 50-instruction microcomputer packaged in an 18-pin DIP. Features include 2-level subroutine stack, one 4-bit parallel input port, one input sense line, four discrete output lines, and a 5-V power supply operation. Panasonic, One Panasonic Way, Secaucus, NJ 07094 has manufactured the device with an n-channel MOS process. Offering a 10-μs instruction cycle, it incorporates a clock generator, ALU, 16-word RAM, and 512-word ROM.
Circle 421 on Inquiry Card

Microprocessor-Based Boards Meet Standard European Specifications

Two versions of the Z80-MCB/E microcomputer board and Z80-MDC/E memory/disc controller have been introduced by Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 to meet standard specifications commonly adopted in West Germany, the United Kingdom, France, and Switzerland. Featuring the same basic capabilities as their domestic counterparts, the boards sell for $595 and $895, respectively. The company's domestic and European sales networks will market the pair.
Circle 422 on Inquiry Card

System Memory Interface Forms Powerful 2-Chip Microcomputer

A single monolithic IC, the 2656 system memory interface (SMI) combines with the company's 2650 microprocessor (or those of other manufacturers) to create a 2-chip microcomputer with system flexibility. Aside from this configuration, the unit serves as an interface chip to expand memory and I/O capability of any microprocessor, or may be used with a peripheral interface chip to drive

Many engineers are resisting fiber optics. We know why.

Most good engineers can't resist a good idea. (And fiber optics is a compelling idea, after all: optical communication cables carry more information in less space with less weight, and eliminate electrical interference, just for starters.)

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We offer the most complete line of optical communication cable in a range of attenuations, mechanical strengths and cost to meet your application requirements. In fact, you can probably find whatever Galileo Galite® fiber optic cable configurations you need from stock (not just our highly versatile Galite 3000).

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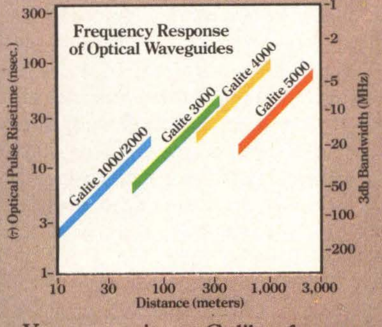

You can write to Galileo for a detailed information package that will give you a good idea of what fiber optics can do for you today. Or you can call Galileo's applications engineers at (617) 347-9191 for specific personal help on how... and where... fiber optics could fit into what you're doing today.

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Galileo Park, Sturbridge, Massachusetts 01518

Progress made practical.

CIRCLE 92 ON INQUIRY CARD

additional circuits from a microprocessor bus.

Signetics, 811 E Arques Ave, PO Box 9052, Sunnyvale, CA 94086 incorporates into the mask-programmable circuit a 2k x 8 p/ROM, 128 x 8 static RAM, eight I/O pins for external chip selects or I/O data port bits, an 8-bit latch for output data, and an internal clock generator programmed with crystal, RC, or external input. A 3-state bidirectional 8-bit bus transceiver acts as a buffer to handle data transfers between the chip and a CPU. The 40-pin DIP operates from a 5-V power supply.

A single-card emulator is offered as a system designer's aid to duplicate all of the chip's functional capabilities. All mask programmable options of the chip, together with test system parameters and architecture, can be emulated.

Circle 425 on Inquiry Card

File Management System Maximizes Use of Fast Random Access

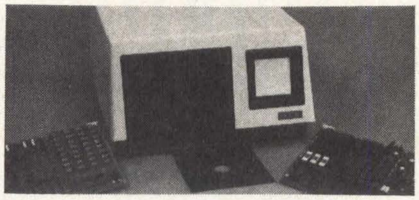
A keyed sequential access method is offered by Efficient Management Systems Co, PO Box 24766, Oakland, CA 94623 in the form of KSAM80, together with utility programs. Designed for floppy disc microcomputer systems, this file management system handles large files with fast random access.

Also supported are sequential access starting at any point within a file, random access by partial key, and random access by relative record number; these commands may be intermixed. Other features include self-reorganizing files and buffering techniques. Developed under Zilog's Z80 OS 2.0, the software package can be implemented in many microcomputer operating systems.

Circle 426 on Inquiry Card

μComputer System With Floppy Discs Contains Development Tools

A microcomputer with powerful software, Z80 power, and floppy disc versatility, the AID-80F system provides tools for hardware/software development and debugging. Organized



around the family of development boards offered by Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, the $5995 system contains hardware consisting of an SDB™-80, which provides the power of the Z80 plus 16k bytes of onboard RAM; the memory and I/O expansion board RAM-80, which includes 16k bytes of RAM and four 8-bit I/O ports; and the FLP-80 disc-drive controller board, which interfaces the SBD-80 with up to four drives with soft sector format.

An optional board, AIM™-80, allows real-time in-circuit emulation with debug, trace, and diagnostic capabilities. Software consisting of a monitor, editor, assembler, relocating loader, and debugger is designed to accelerate the programming rate, thus allowing concentration on the application problem.

Circle 427 on Inquiry Card

Personal Computers Replace Costly Edit Code Readers

The introduction of the first of a proposed series of operating systems written by J. S. Wiener, 4440 N Kedzie Ave, Chicago, IL 60625 is aimed at firms using audio/visual communications. SMPTE (Society of Motion Picture and Television Engineers) READ program will allow time-coded indexing for editing, assembling, and other uses formerly subjected to the judgement of technicians.

Written in 8080 assembler, the program uses any 8080-based microcomputer to read time-coded films and tapes. The display handles up to eight sources simultaneously. The package, supplied on punched paper tape with manual, source listing, and interface module, sells for $49. The program resides in 3k of contiguous memory, requires two parallel input ports, and operates with a variety of video display modules having onboard screen memory.

Circle 428 on Inquiry Card

Expansion Board For 9900-Based μComputer Provides I/O Flexibility

The model 990-110 memory and I/O expansion board is physically and electrically bus compatible with the TI TM 990/100M microcomputer. The board provides sufficient RAM/EPROM and I/O to satisfy many complex control applications. Specifically, it has 2k 16-bit words of EPROM expandable to 4k, 1k 16-bit words of static RAM, and memory addresses which are selectable on 1k boundaries for RAM and 4k boundaries for EPROM.

Three TMS 9901 programmable systems interface chips provide input, output, and interrupt lines. The 48 I/O lines, programmable as inputs or outputs in groups of two, may be buffered or power inverted, and have pull ups, pull downs, or standard terminations. There are 18 additional inputs, 12 of which have optional input latches for edge-triggered signals.

Other features include 15 possible interrupt inputs on each 9901 chip, and a CRU base selectable on 128-bit boundaries. Digital Interface Systems, Inc, PO Box 1446, Benton Harbor, MI 49022 will offer low quantity prices ranging from $395 for a board with unbuffered I/O and no memory, to $635 for a buffered and fully populated board.

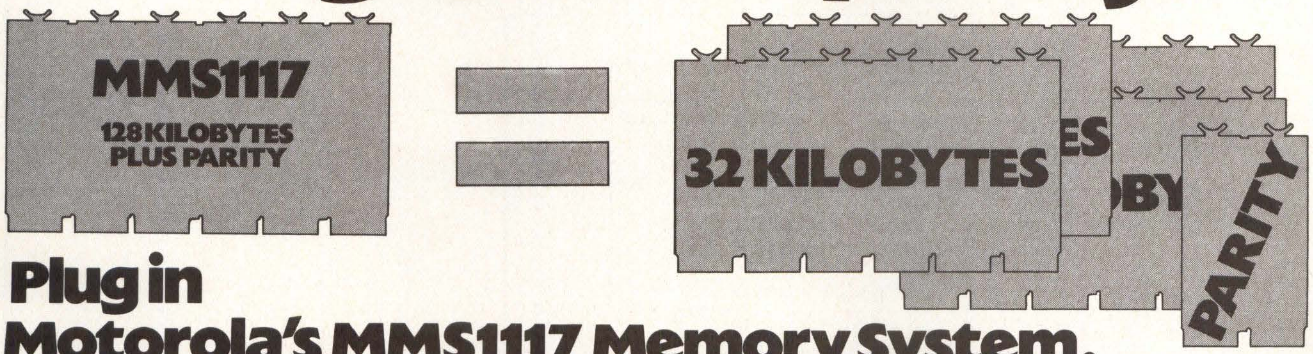
Circle 429 on Inquiry Card

Bit Slice Family Combines Increased Speed With Low Power

No longer having to sacrifice power for speed, systems designers can have both ECL-type speeds and LSI bipolar power consumption and interface capability. National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has developed a family of 2900-type 4-bit-slice microprocessor components that are 30 to 50% faster than similar designs.

The IDM 2900 family uses a process called SCL that joins low power Schottky peripheral circuitry with proprietary high speed Tri-State[R] emitter coupled logic circuitry for interface. One circuit innovation uses Tri-State translator circuitry to transform ECL voltage levels to low power Schottky TTL levels and back, allow-

For high-density "universal" PDP-11* storage, with parity...



Plug in Motorola's MMS1117 Memory System.

Now it's easy and inexpensive to add in high-density, high-speed PDP-11 compatible memory with parity features. Motorola's MMS1117 memory system provides total electrical and mechanical compatibility with 10 different UNIBUS* PDP-11 processors; the new 11/60, plus 11/04, 11/05, 11/10, 11/34, 11/35, 11/40, 11/45, 11/50, and 11/55. Just plug it into any new "Hex SPC" slot.

MOTOROLA SEMICONDUCTOR MEMORY SYSTEMS

System	Organization	Description
MMS1110 MMS1110-1 MMS1110-2 MMS1110-3	16K x 16 12K x 16 8K x 16 4K x 16	Add-in for LSI-11 systems
MMS1116	16K x 16	Add-in for PDP-11/05, 11/10, 11/35, 11/40 and 11/45 systems
MMS1118 MMS1118-1 MMS1118-2	16K x 18 12K x 18 8K x 18	Add-in for PDP-11/04, 11/34 systems
MMS3400	32K x 18 or 64K x 9	For 3400N systems
MMS68102 MMS68102-1 MMS68102A MMS68102A-1	16K x 8 8K x 8 16K x 9 8K x 9	Battery backup for M6800 and other synchronous systems; pin compatible with EXORciser† micromodule
MMS68103 MMS68103-1 MMS68103A MMS68103A-1	16K x 8 8K x 8 16K x 9 8K x 9	Hidden refresh for M6800-based systems.
MMS68104	16K x 8	For MEK6800D2 Kit
MMS80810 MMS80810-1	32K x 8 16K x 8	For 8080A-based systems; pin-compatible with SBC 80/10

A fully populated MMS1117 is a whopping 128 kilobytes, and options include systems of 96, 64, and 32 kilobytes, priced appropriately lower. Parity options are on-board parity plus controller, parity data only, or no parity. All are available for each of the three system speed options.

128 Kilobyte MMS1117

Read Access Time Typical	Price 1—5
370ns	$4,305
420ns	$3,920
470ns	$3,530

The MMS1117 interfaces to all 18 bus address lines. Starting address can be selected, via switches, to fall on any 4K word boundary between 0 and 124K. The MMS1117 imposes one UNIBUS load regardless of memory size or parity option. Despite the density and speed of the MMS1117, power requirements are low. A fully populated 128 kilobyte system with parity and controller operates at the following rates: 5 V ±5% @ 3.0 A (typ), +15 V @ 0.2 A standby and 0.7 A continuous maximum access, −15 V @ 0.03 A.

Motorola's line of standard memory systems is heavily augmented with custom projects. We take great pride in the fact that you get really fast delivery and leadership pricing on both standards and custom systems.

The fastest way to get information on Motorola memory systems is direct contact with your Motorola sales office, or we'll respond promptly to qualified inquiries on the coupon below. For a copy of the MMS1117 data sheet, write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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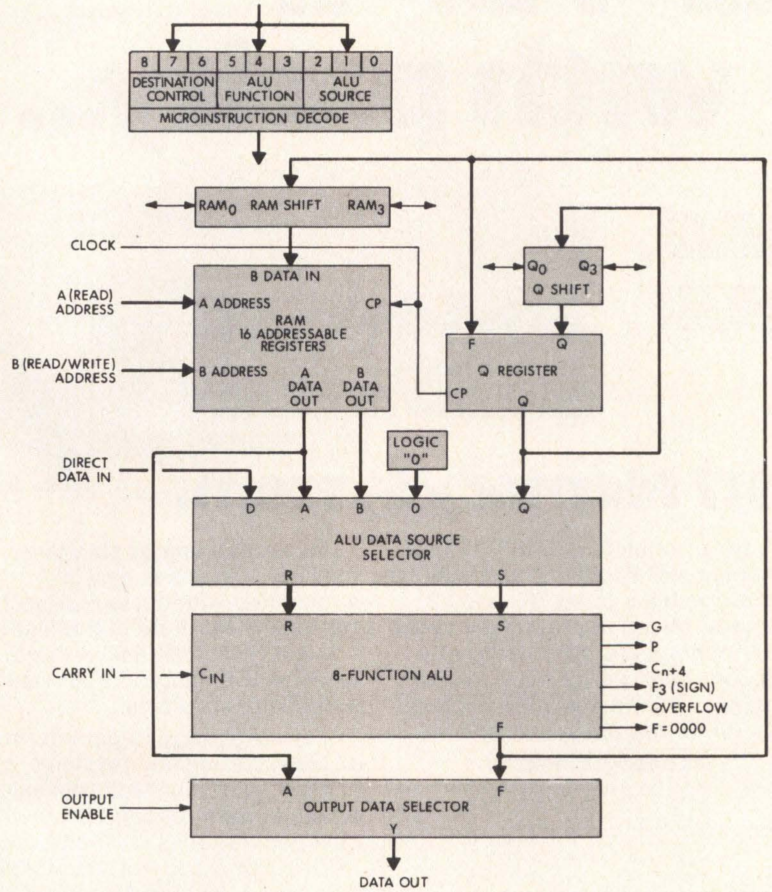


SCL technology is implemented in National Semiconductor's IDM2900 series. Higher performance devices feature improved timing parameters and high drive current capability. Indicative of the entire family, the diagramed IDM2901A 4-bit MPU with RAM, ALU, and associated shifting, decoding, and multiplexing circuitry has typical 60-ns microcycle time and 800-mW power consumption

ing translators to drop off to one-third their active power.

The company is second sourcing most of the major components in the industry standard 2900 family. This includes the 2901A 4-bit slice with 16-word x 4-bit 2-port RAM and 8-function ALU; the 2902 high speed look-ahead carry generator; the 2909A/2911A address controllers for sequencing through a series of microinstructions in ROM or p/ROM; the 29702/03 inverting 64-bit RAMs; and 29750/51 and 29760/61 field programmable 32-word x 8-bit and 256 x 4-bit p/ROMs, respectively. All are pin and functionally compatible with current devices.

New components being added are the 29803 16-way branch controller, 29811 next address controller, 29901 octal Tri-State register, 29902 priority encoder, 29903 16-word x 4-bit clocked RAM, and 29908 quad-gated flip-flop. They improve throughput and efficiency of existing bit-slice systems. All devices are now available in sample quantities.

Representative of the family, the IDM2901A MPU has a basic microcycle time in the 60- to 70-ns range. Execution of a typical operation is in the 60- to 120-ns range. Power consumption for the single 5-V device is about 800 to 900 mW; speed-power product is 6 pJ.

Improved Assembler/ Editor Resides in 4k of RAM or ROM

The MCS 6502 resident assembler/text editor and relocating loader produce relocatable object code on tape and store directly executable code in memory during assembly. Object code can be reloaded at most locations. Less than 4k of RAM or ROM are required by the assembler/editor. Features include 17 editor commands, 16 assembler pseudo-ops, assembler listing, 18 error codes, and ability to assemble source programs from tape or memory.

Preconfigured for TIM-based systems, this software supports up to two tape decks, CRT and keyboard, and optional printer. Hexadecimal listing and operator's manual, costing $25, are available from Carl W. Moser, 3239 Linda Dr, Winston-Salem, NC 27106.

Circle 430 on Inquiry Card

Output Capability of 120 Vac Is Added To Microcomputer System

The standard industrial microcomputer of Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI

Quick Change Artist.

Our OEM 600 lpm printer has a replaceable character cartridge as fast and easy to change as a typewriter ribbon.

How fast?
Less than a minute.
How easy?
Easy enough for anyone with the strength to pick up 10 lbs. and the skill to change a typewriter ribbon.

Data 100 knows what an OEM wants in a line printer.

Like fast and easy character set interchangeability. A capability that's standard on our 600 lpm printer.

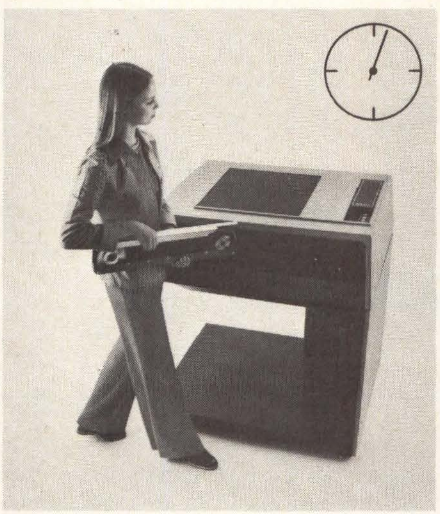
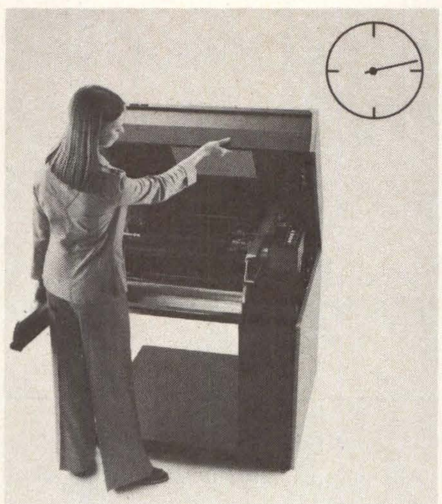
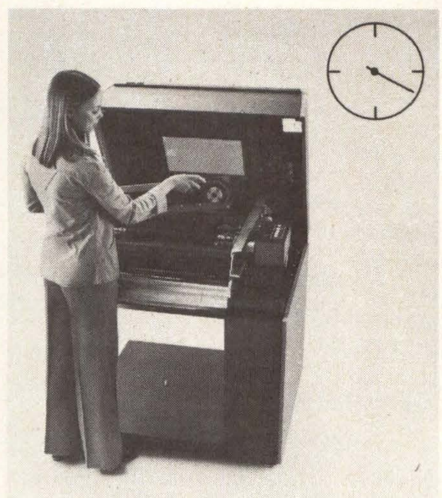
It not only gives the user greater flexibility, but also eliminates the need to buy two line printers just to satisfy that requirement.

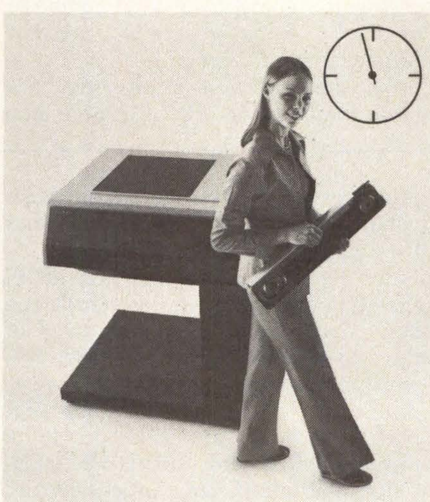
Make good sense to you?

It should. We're adding this Quick Change Printer to our Data 100 systems, too.

DATA 100
CORPORATION

Data 100 knows what an OEM wants in a line printer.

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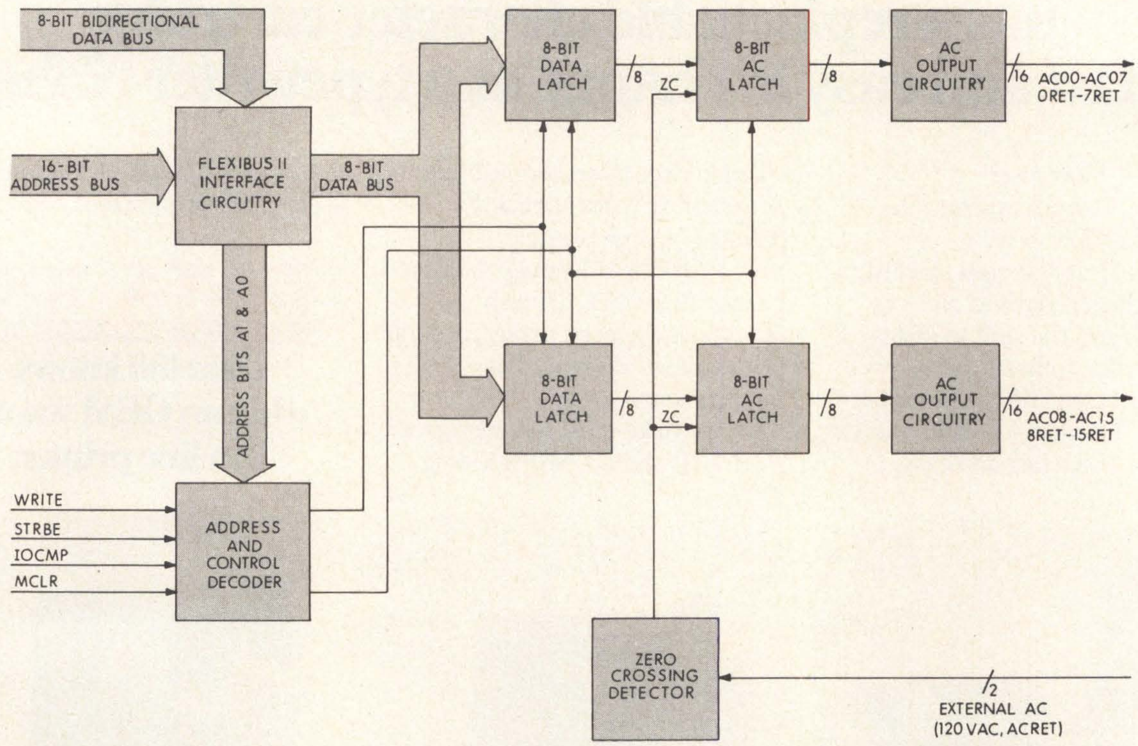


Model 1825 optically isolated, 16 ac output port module from Process Computer Systems has high power output with low power consumption to actuate solenoids, relays, alarms, motors, valves, and lamps

48176 can now be used to drive ac devices in machine and process control applications. Model 1825 is a self-contained 120-Vac output module which provides 16 optically isolated ac output ports, thus minimizing feedback, cross-talk, and ground loops. All outputs are latched, and zero cross-over switching of all outputs is provided automatically by the module to inhibit noise generation, current surges, and part stress.

An optional version includes the basic module plus 16 card edge LED indicators to show the status of each output and to aid in troubleshooting. A switch also is provided to lamp test the LED indicators. The $425 (quantity one) module is Flexibus II system bus compatible.

Circle 431 on Inquiry Card

μProcessor Simulators Aid Development of ATE Programs

Two simulation systems that incorporate capabilities for emulating logical operations of high density LSI components have been introduced by Computer Automation's Industrial Products Div, 18651 Von Karman, Irvine, CA 92713, concurrently with emulation packages for the Intel 8080A and Motorola 6800. Memory systems up to 2M bytes can be accommodated. Register transfer notation—a high level processor that permits users to define parts (like microprocessors) in terms of transfers involving one or more registers—has been implemented in the systems.

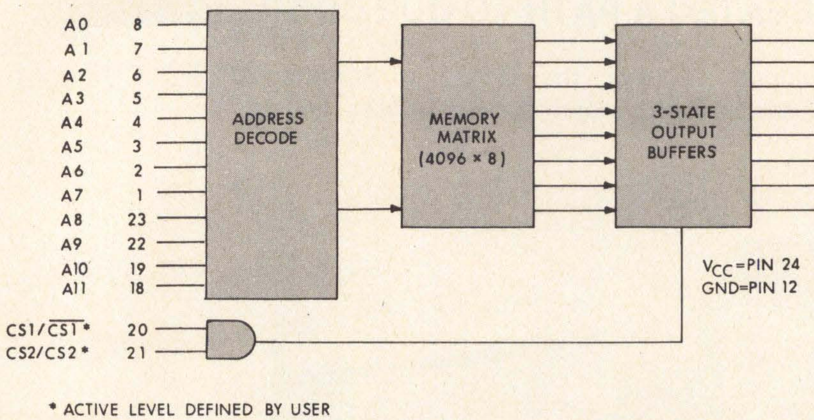
An expanded version of the 4810, the Capable 4812 is a standalone logic simulation system comprised of the company's minicomputer, 96k words of memory, emulation software, disc drive, documentation, and support. The 4852, an expanded 4850, provides lower cost simulation capability through sharing processor and memory with a testing system; it incorporates emulation software and expansion of the tester memory to 96k words.

Circle 432 on Inquiry Card

Operation of 32k ROM for Bus-Organized Systems Is Fully Static

A 4096 x 8-bit ROM is a mask-programmable, byte-organized memory designed for use with such systems as the M6800 or other 8-bit microprocessor families. Static operation eliminates the need for clocks, refreshing, and address setup and hold times.

The Integrated Circuit Div of Motorola Semiconductor Products, Inc, 3501 Ed Bluestein Blvd, Austin, TX



Programmable n-MOS memory with fully static operation is compatible with Motorola Semiconductors' M6800 microcomputer family, providing read-only storage in byte increments

78721 has fabricated the device with n-channel silicon-gate technology. It is TTL and DTL compatible, uses a single ±10% 5-V supply, and dissipates less than 440 mW with access and cycle times of 350 ns. The 24-pin packaging is either plastic or ceramic.

Memory expansion is provided through multiple chip select inputs. The active level of these inputs and the memory content are user defined. Also provided is 3-state data output for OR-ties.

Circle 433 on Inquiry Card

Unit Programs EPROMs for KIM-1 Microcomputer

A programmer for the KIM-1 microcomputer (see *Computer Design*, April 1976, p 138) is capable of programming both 2708 and 2716 (5 V only) EPROMS. By using the computer's monitor, any RAM starting address may be specified up to 65k; any p/ROM starting address may be specified along with the number of bytes to be programmed. Verify mode confirms that all bits are programmed correctly.

The programmer, offered by Optimal Technology, Inc, Blue Wood 127, Earlysville, VA 22936 for $59.95, is furnished on a single PC board with a connector. The program runs on all computers that use the MOS Technology 650X microcomputer and have I/O ports 1700 to 1703 available.

Circle 434 on Inquiry Card

Mid-Level Compiler Blends Features of Assembly/ High Level Languages

A systems implementation language, CSL/65, has been developed by Computer Application Corp, 413 Kellogg, Ames, IA 50010 for the 6500 microcomputer family. It resembles PL/1 and ALGOL in general form, but has been specifically designed for microcomputer users to simplify development of programs normally written in assembler. As a mid-level language, it has the power and flexibility of assembler and the structuring potential of a high level language.

Versions are available for Rockwell's System 65 and any DEC PDP-11 using the RT-11 operating system; others will be announced later this year. Assembler code rather than object code is produced. Output is passed to the assembler which is part of the System 65 monitor or to the MINmic assembler which is available from the company for the PDP-11.

Circle 435 on Inquiry Card

Isolated, Digital Input System Operates With Three Microcomputers

The MP810 and MP810-NS are 24-channel, optically isolated, digital input microperipheral boards that are electrically and mechanically compatible with Intel SBC-80, Intellec MDS, and National BLC-80 microcomputers. With onboard power supply, the 810 operates with dry relay contacts; the 810-NS has voltage inputs and operates with wet relay contacts.

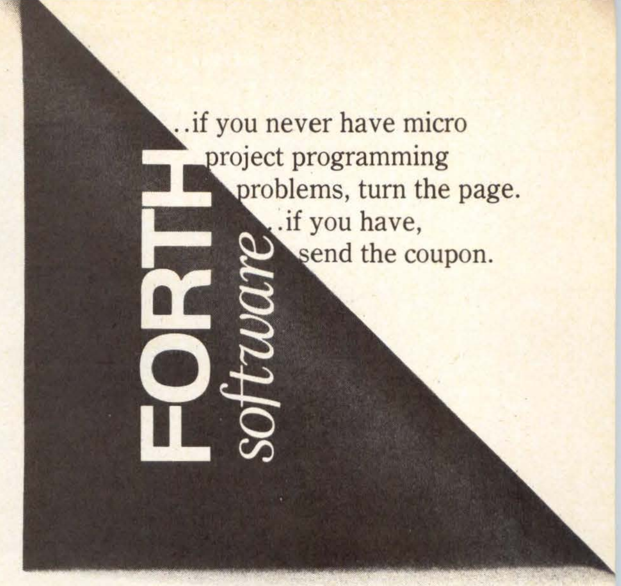
Each group of eight inputs is isolated from other input groups and from the computer bus to 600 Vdc. Isolation between inputs of the NS version is 300 Vdc. Voltage supplied to each line, therefore, is not critical, and ground loops are avoided. Isolation protects the microcomputer from voltage transients and other malfunctions.

The boards, available from Burr-Brown, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734, are programmed as memory locations. Each input uses one memory bit so that any read command may be employed. Each command inputs the status of eight channels.

Input impedance is 15 kΩ; input delay is 25 μs max, open to closed, and 100 μs max, closed to open. Maximum voltage that can be applied across the 810 input is 120 Vac rms or 60 Vdc; across the 810-NS inputs, 168 Vac rms or 84 Vdc. They are priced respectively at $355 and $295 in quantities of one to nine.

Circle 436 on Inquiry Card

Don't give up on your micro project: just put less into it.



. .if you never have micro project programming problems, turn the page.
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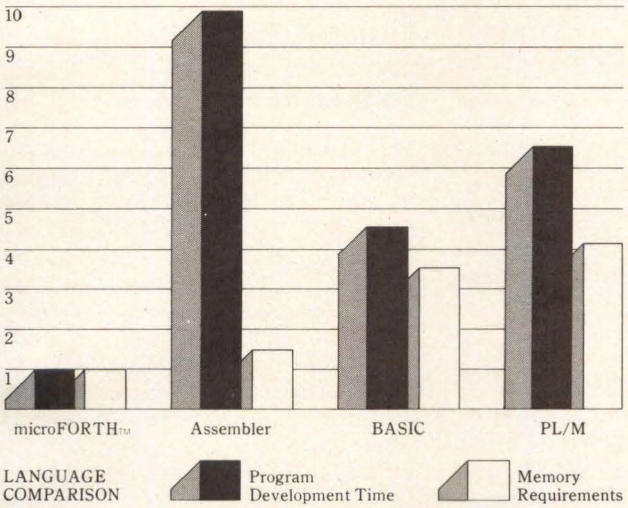

Units of time and memory required are averages provided by microFORTH users, based on actual application experience and/or specification estimates.

Find it hard to believe that FORTH software tools can short-cut microsystem development that much? Or that you don't have to give in to those old time/memory trade-offs which bog down so many microprocessor projects?

Skeptics, take note: microFORTH software has turned the corner in microsystem implementation, for the likes of AT&T, G.E., Monsanto, RCA and Hughes as well as the U.S. Army and Navy (and more).

Fully user-proven, microFORTH provides much more than an interactive multi-level language: a disk-based operating system, plus assembler, compiler, interpreters, text editor (and your entire program) are all concurrently resident. The more we could put in the package, the less you're put out.

Less program development time. Save 60-90% in manhours, to get from drawing board to working prototype. microFORTH permits you to go directly to the point—instruct machines on your own terms—because it's fundamentally an extensible dictionary including a vocabulary *you* define for your specific application. And you debug interactively as you go, without the need for breakpoints and software traces.

Less memory required: half the bite of assembler code; 60-80% less than other high-level languages. microFORTH's dictionary structure provides modularity of coding and uses precompiled definitions via indirect threaded code.

Less overhead. microFORTH run time is not only faster than other high-level languages, it's controllable too—with full machine-speed capability available when you need it. Intersperse machine-code subroutines without calling sequence expense.

And more transportable programs. microFORTH provides a consistent software interface between you and a broad range of different manufacturers' hardware. Application programs are easy to transfer to a variety of μP systems.

But no matter whose microprocessor is in place, microFORTH minimizes your hardware investment, since it requires less memory capacity, permits simpler hardware logic.

In short, FORTH softens your total investment. Off-the-shelf microFORTH is package-priced at $2500, plus options. (Contract application programming services are also available.)

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MICRO PROCESSOR/COMPUTER DATA STACK

Business Software Program Applies To Microcomputers

The Grimes Business Information System (GBIS) is a low cost, general business software package for microcomputers. Developed by Larry G. Grimes & Associates and Computer Products of America, the system is intended for small businesses; it is offered by Computer Mart, 633 W Katella Ave, Orange, CA 92667 for $200.

Requiring only 24k of memory, the software is an interactive system where receivables decrease book inventory, payables increase book inventory, and general ledger accounts are updated automatically with extensive and valid accounting controls. Payroll and data entry also are covered. It is written in North Star BASIC; other disc BASIC languages may be used for listings. Features include no multiple statements on a line; logic flows from top to bottom; no user-defined functions; data files (no data statements); and indented lines at strategic places.

The package has 51 programs with 21 pages of documentation. A users group has also been formed. The first update that may be purchased will include subsidiary journals for cash receipts and disbursements, extended payroll, checkwriting, and some manufacturing applications.

Circle 437 on Inquiry Card

Minifloppy Disc System Boosts Operating System Performance

Providing fast access, online storage economically for Z80/8080 microcomputer users, the V80 floppy disc system contains a minifloppy drive with dc regulator board, S-100 bus controller card to control up to three drives, I/O connection cable, and VOS and BASIC-E compiler. Vista Computer Co, 2807-FS Oregon Ct, Torrance, CA 90503 has included such features as instantaneous program loading and dumping, file management and storage, context editing, dynamic debugging, program assembly, and batch processing.

Circle 438 on Inquiry Card

What kind of permanent magnet DC motor do you need?

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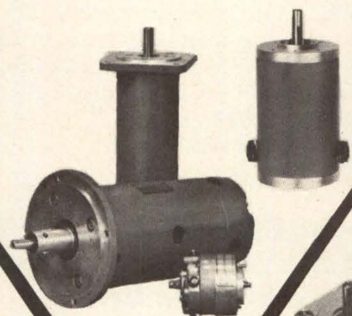
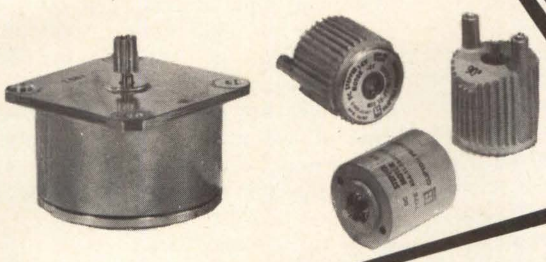
Advanced magnetic materials
Cartridge brushes



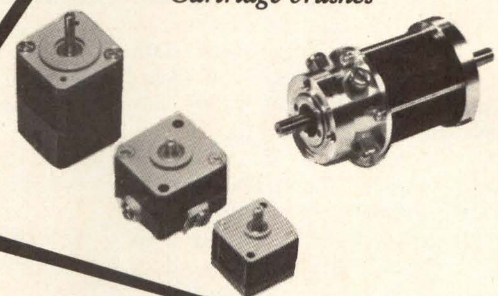
PM STEPPER MOTORS

Step angles 7.5°, 15°, 30°, 45°, 90°
1.1 inch to 2.8 inch O.D.
Ceramic or rare earth magnets



MINIATURE DC PM INSTRUMENT MOTORS

Torques from 2 to 50 oz-in.
.75 inch cube to 1.25 inch O.D.
Alnico or rare earth magnets
Cartridge brushes



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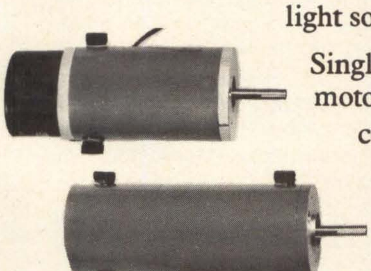
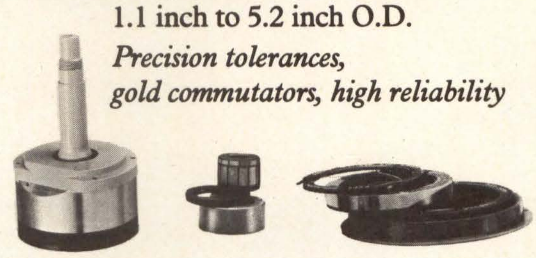


DC PM HOLLOW SHAFT TORQUE MOTORS

Torques from 6 to 500 oz-in.
1.1 inch to 5.2 inch O.D.
Precision tolerances, gold commutators, high reliability



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CIRCLE 101 ON INQUIRY CARD

Floppy Disc Drive Series Is Aimed At Retail Microcomputer Market

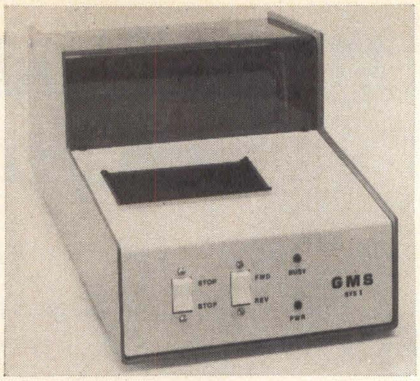
Two versions of fully packaged and assembled disc drives are available with software, S-100 bus compatible controller, and 143k-byte capacity. Intended for integration into any 8080A or Z80 microcomputer chassis, model 1041 has a drive, enclosure, cabling, connectors, disc operating system, and disc extended BASIC for a suggested retail price of $695. Model 1042 of the Macrofloppy series, with a suggested price of $795, adds a power supply and dc regulators for desktop use.

To insure accurate reading and writing of the greater number of tracks needed for large-scale data storage, Micropolis Corp, 7959 Deering Ave, Canoga Pk, CA 91304 has incorporated an all-steel head positioner system using a precision-ground, stainless steel lead screw with steel follower, rather than plastic. A referencing technique used in the drive layout minimizes the effect of any outside distortion introduced into the drive's chassis. Wide dynamic ranges enable valid reading of data even when signal strength from the diskette is weak.

Features include file protect and built-in ROM bootstrap. The drives have 16 sectors each 256 bytes long, with a total of 35 tracks/surface. Both offer transfer rates of 250k bits/s at an average rotational latency time of 100 ms. Access time track-to-track is 30 ms, and recording density is 5162 bits/in (2032/cm).

Circle 439 on Inquiry Card

High Efficiency Is Achieved With Low Cost Mass Storage Drives



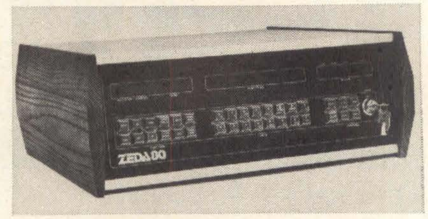
Providing mass storage for microcomputers, the SYS I tape drive subsystem records bi-phase Manchester code at 1600 bits/in (630/cm) on ANSI specified data cassettes with a transfer rate of 2000 char/s at 10 in (25 cm)/s. General Micro-Systems, 12369 W Alabama Pl, Lakewood, CO 80228 offers the units in both single- and dual-drive versions.

Tape record (block) is variable length. The user program may dynamically load the next record, operating as a batch data processing system, with an unlimited amount of data. Over 700k bytes may be recorded on one side of a cassette using large records.

Rewind time is less than 30 s at over 120 in (305 cm)/s. Search is accomplished at over 120 in (305 cm)/s by counting interblock gaps, getting to any record in an average time of less than 15 s. One to four drives may be connected to the computer through the synchronous serial interface board.

Circle 440 on Inquiry Card

Z80-Based µComputer Features Intelligent Control Panel



A 4-MHz, Z80-based microcomputer for OEM, small business, and industrial control markets has a control panel for implementing memory functions whose execution is transparent to the user. It displays and alters contents of registers or memory, reads input ports, writes to output ports, searches memory, sets multiple breakpoints, and bootstrap loads floppy disc or cassette operating systems.

Data entry and display are done in hexadecimal. Operation modes of the device from Zeda Computer Systems, 666 N 380 W, Provo, UT 84601 are run, slow execute, single instruction, and trace.

Circle 441 on Inquiry Card

µComputer Family Gains Memory Support From RAM/EPROM Card

The 6.75 x 12" (17 x 30.5-cm) MLZ-MEM 832 has been introduced by Heurikon Corp, 700 W Badger Rd, Madison, WI 53713 for its MLZ-80 microcomputer family. It contains up to 32k of static RAM and sockets for 4k (2708) or 8k (2716) EPROMS (either Intel or Texas Instruments). Starting address is switch selectable to any one of 16 4k blocks of memory. Card may be purchased with or without memory; single unit price with sockets is $450.

Circle 442 on Inquiry Card

CRT Terminal Connects To Horizon Computer For 24 x 80 Display

The model IQ 120 CRT terminal, manufactured under agreement with Soroc Technology, can be connected to the I/O port of a Horizon-1 or -2 computer operating at baud rates up to 9600 (see *Computer Design*, Aug 1977, p 134). The terminal is offered by North Star Computers, Inc, 2547 9th St, Berkeley, CA 94710 for $995. Features include an addressable cursor, upper and lower case ASCII character set, and numeric keypad.

Circle 443 on Inquiry Card

Reliable Microcomputer Serves Industrial Applications Uses

The model 300 microcomputer is offered by Labtest Equipment Co, 11828 LaGrange Ave, Los Angeles, CA 90025 for use in dedicated industrial systems and control applications. The 8080-based unit has no front panel switches, is self-contained in a metal rfi enclosure, and includes rfi and noise filtering. It comes assembled and tested with 10k memory, one I/O board, power panel, cables and connectors, two fans, power supply, I/O ports, and a 22-slot motherboard. The model operates with TTY or CRT and keyboard options.

Circle 444 on Inquiry Card

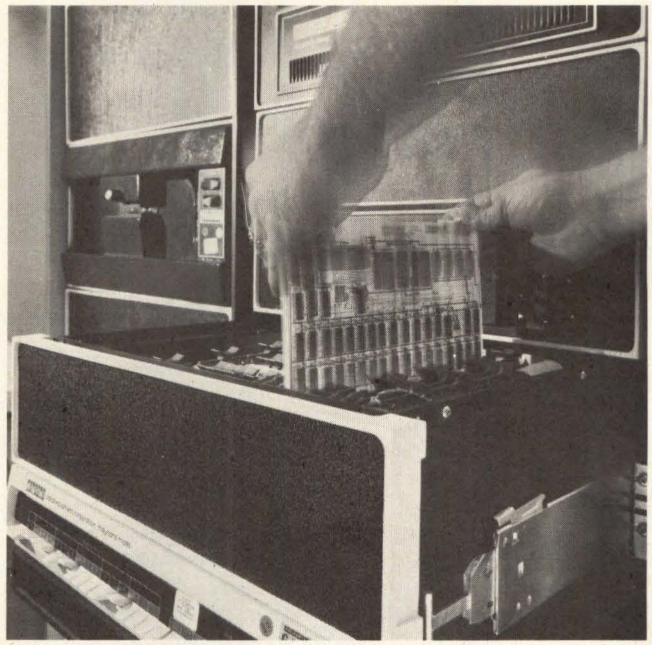
Videotaped Courses and Seminars Explain Microprocessors

Four user-oriented "how to" seminars and three courses on microprocessors are available on video tapes with associated workbooks and texts from Genesys Systems, Inc, 1121 E Meadow Dr, Palo Alto, CA 94303. Dr Rodnay Zaks of Sybex leads the seminars on "Microprocessors, The Basic Hardware Course"; "Military Microprocessor Systems, Overview of Techniques and Systems Available"; "Microprocessor Interfacing Techniques"; and "Bit Slice, Building an Actual CPU with Slices." The three courses conducted at Colorado State University are "How Do I Master Microprocessors?"; "Logic Design of Digital Systems for Implementation with a Microprocessor"; and "Designing with the 6800." □

Circle 445 on Inquiry Card

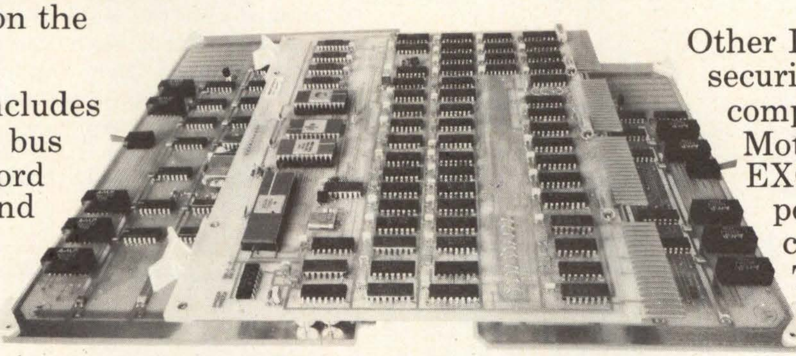
Another data security first from Motorola

A single plug-in board secures PDP-11* data



The latest in the line of Info-guard™ data security modules adds hardware encryption/decryption to the PDP-11 family of minicomputers. The single plug-in board, using the National Bureau of Standards' algorithm, allows quick retrofit for transmission security... even for multiple lines.

The microprocessor-based module includes Direct Memory Access (DMA) control and minimizes software impact on the PDP-11 C.P.U.



The DMA logic includes address selection, bus master control, word counting, input and output buffering, and interrupt control. Encryption control includes key transfer, initial fill of RAM buffer; encryption, and parity error checks.

After encrypting data blocks of up to 1K x 16 bits, the data is DMA-transferred back to the PDP-11 memory.

Other Info-guard data security modules are compatible with Motorola's M6800 EXORciser and other popular microprocessor systems. These modules are available off-the-shelf and make it easy for users to add encryption.

For more information, contact James Booth at 602/949-4735 or write to him at Motorola's Government Electronics Division, Dept. F-6, P.O. Box 2606, Scottsdale, AZ 85252.

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MONOLITHIC DATA CONVERSION DEVICES PART 2: ANALOG-TO-DIGITAL CONVERTERS

Eric R. Garen

Integrated Computer Systems, Inc
Santa Monica, California

Part 1 of this discussion of data conversion devices presented the status of digital-to-analog converters (*Computer Design,* Mar 1978, pp 152-158). This month the fundamental principles of analog-to-digital conversion are reviewed, followed by a discussion of several typical monolithic converters available today.

Two fundamental techniques typically are employed in monolithic analog-to-digital (A-D) conversion. One is based on comparison, the other on integration. Both have advantages and disadvantages that must be considered when choosing an A-D converter (ADC) for a specific application.

Comparison-Type ADCs

In the comparison technique, a digital-to-analog converter (DAC) creates a known analog voltage which is compared with the unknown input signal (Fig 1). Then the known voltage is varied digitally until it matches the input signal.

One basic procedure for varying the digital word to create the analog voltage is to count the digital value from zero until the analog value produced matches the analog input. This counting procedure is extremely simple, since the control unit can be just a counter which is turned off when the comparator produces a positive result. At that time the count becomes available on the digital output pins, and a "conversion complete" signal indicates to the external world that the digital value is ready. Note, however, that this counting procedure requires a maximum of 2^n clock periods to match the analog input value. For an 8-bit counter the maximum number of clock periods is 256, and for a 12-bit counter the maximum number is 4096. Thus this procedure, while simple and straightforward, is rather slow.

To speed things up, successive approximation can be used. In this procedure, the control unit is slightly more complex, but can complete an n-bit conversion in n clock periods. To accomplish this the control unit first outputs a digital value which is one-half full scale (Fig 2). Depending on the result of the comparison, the second most significant bit of the control unit is turned on or off. As shown in the example, the analog input value is higher than the half-scale voltage so the second bit is turned on, producing a three-quarter full scale signal. This is again compared with the analog input. In this case, the analog is lower than that produced by the DAC so the second bit is turned off and the third bit turned on, creating a five-eighths full scale voltage. Again, this is compared, and the process is repeated until the required number of bits of accuracy has been attained. Such control units are known as successive approximation registers, and are readily available as single chips or as sub-units within monolithic ADCs as discussed below.

Counter type ADCs have the advantage of being medium speed, typically converting analog signals in

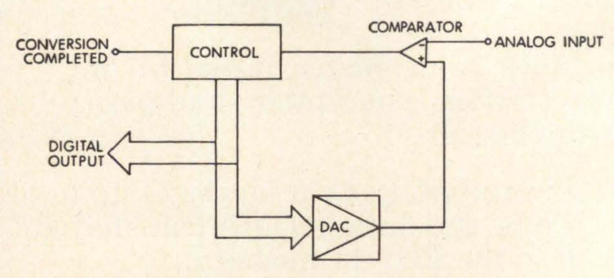


Fig 1 Analog-to-digital conversion utilizing D-A converter and comparator. Control unit generates series of digital values, by either counting or successive approximation, until analog input value has been matched

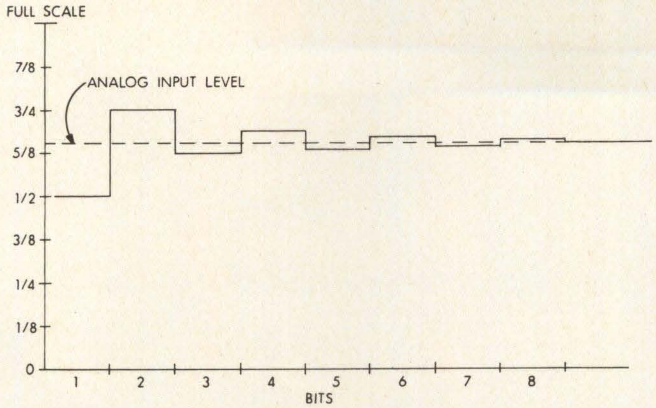


Fig 2 Successive approximation of analog value. Comparison process is repeated until required number of bits of accuracy is achieved

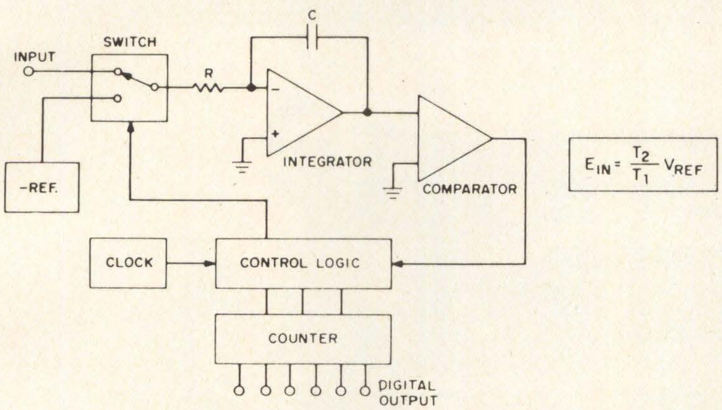


Fig 3 Dual slope integrating ADC. Conversion starts with unknown input voltage switched to integrator input. Long conversion time is main drawback (Courtesy Datel Systems, Inc)

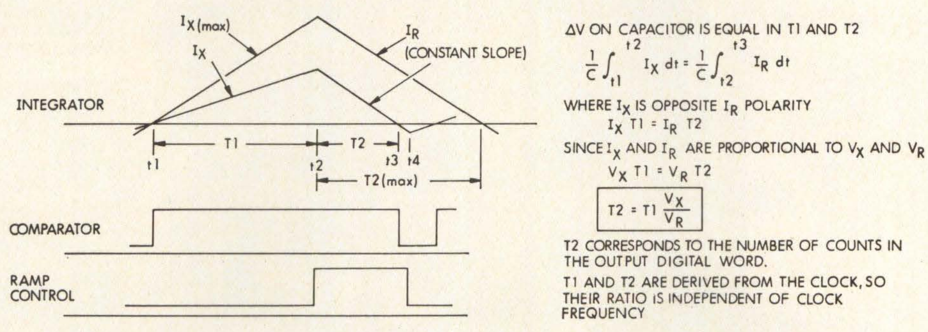
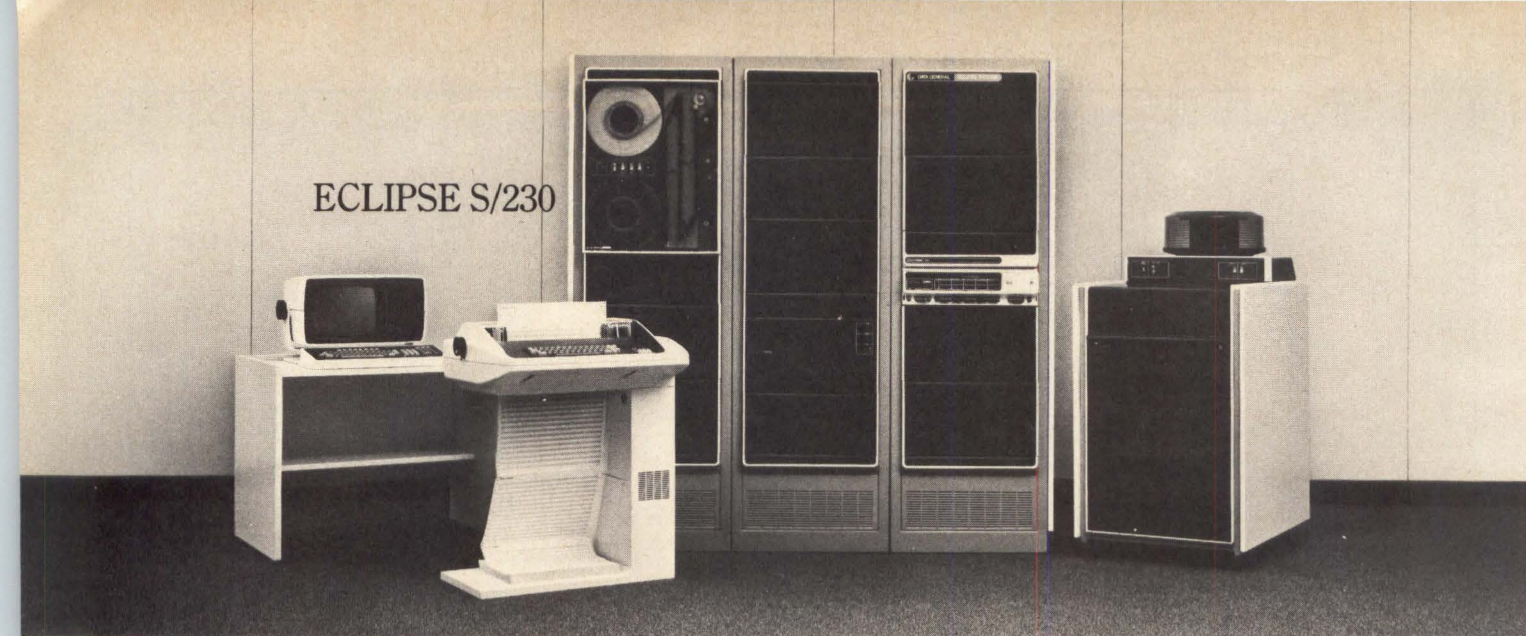


Fig 4 Principle of dual slope A-D conversion (Courtesy Motorola Semiconductor Products)

anywhere from 80 to 500 μs, depending on the precision. The control logic has medium complexity and cost. Successive approximation type ADCs produce the highest speeds of each of these types, and monolithic devices typically convert 8 to 12 bits in 2 to 100 μs. However, high speed monolithic units are being developed with submicrosecond conversion times.

Integrating-Type ADCs

The most common integrating ADCs utilize the dual slope method. To implement this technique the control logic initially switches the unknown analog input voltage to the integrator's input (Fig 3). The integrator begins charging the capacitor and continues to charge for a fixed time period, ie, until the counter reaches a predetermined value. At this time the integrator is switched to the negative reference voltage and the counter is reset to zero. The integrated voltage is decreased by this negative input until the comparator sees that it has reached the comparator threshold. At this time the count is stopped, as shown in Fig 4. The input voltage is then the ratio of the number of counts during T2 to the number of counts during T1. Naturally this division need not actually be performed since T1 simply acts as a scaler of the reference voltage and T2 is thus proportional to the ratio of the input voltage to this scaled reference.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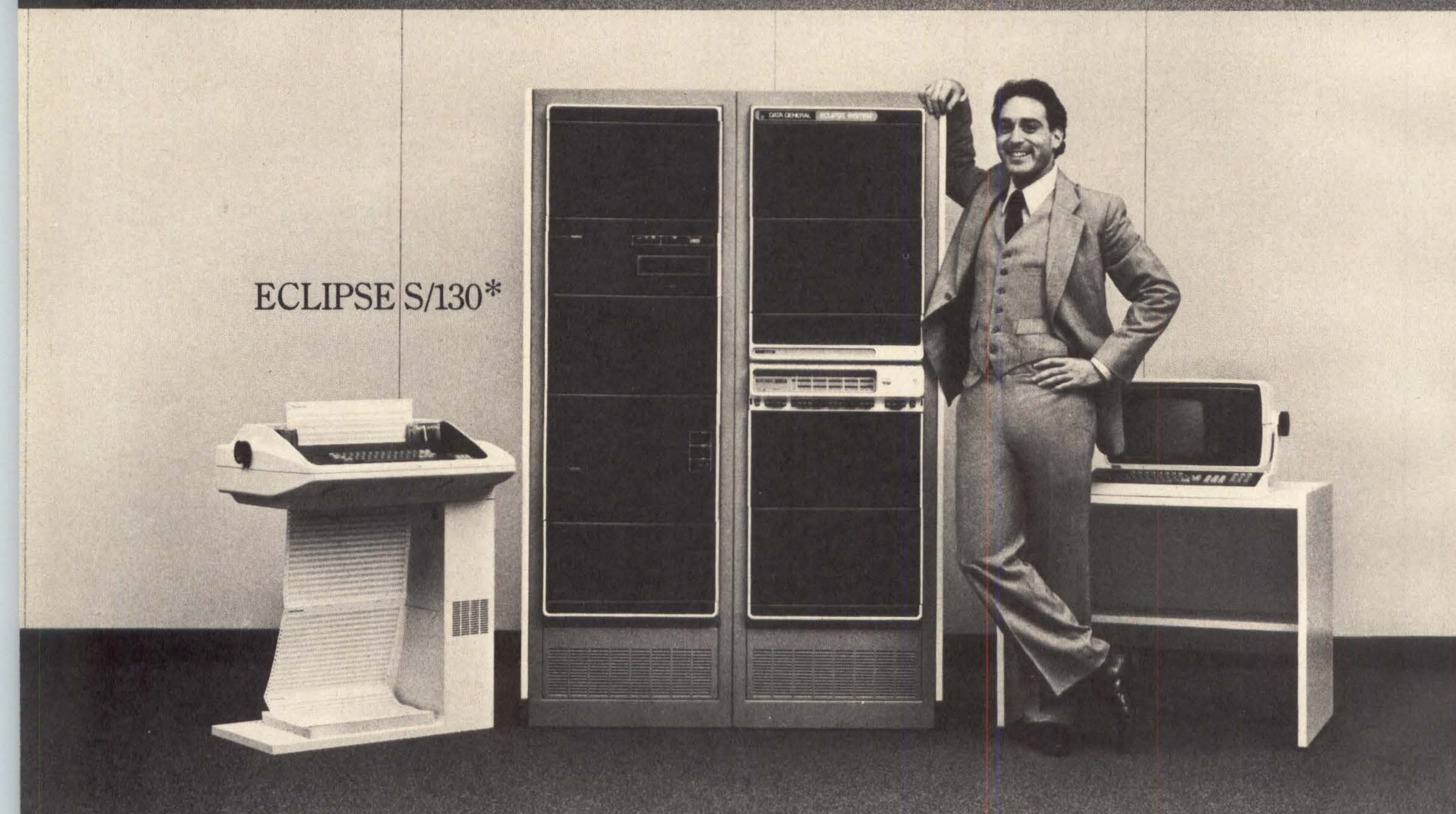
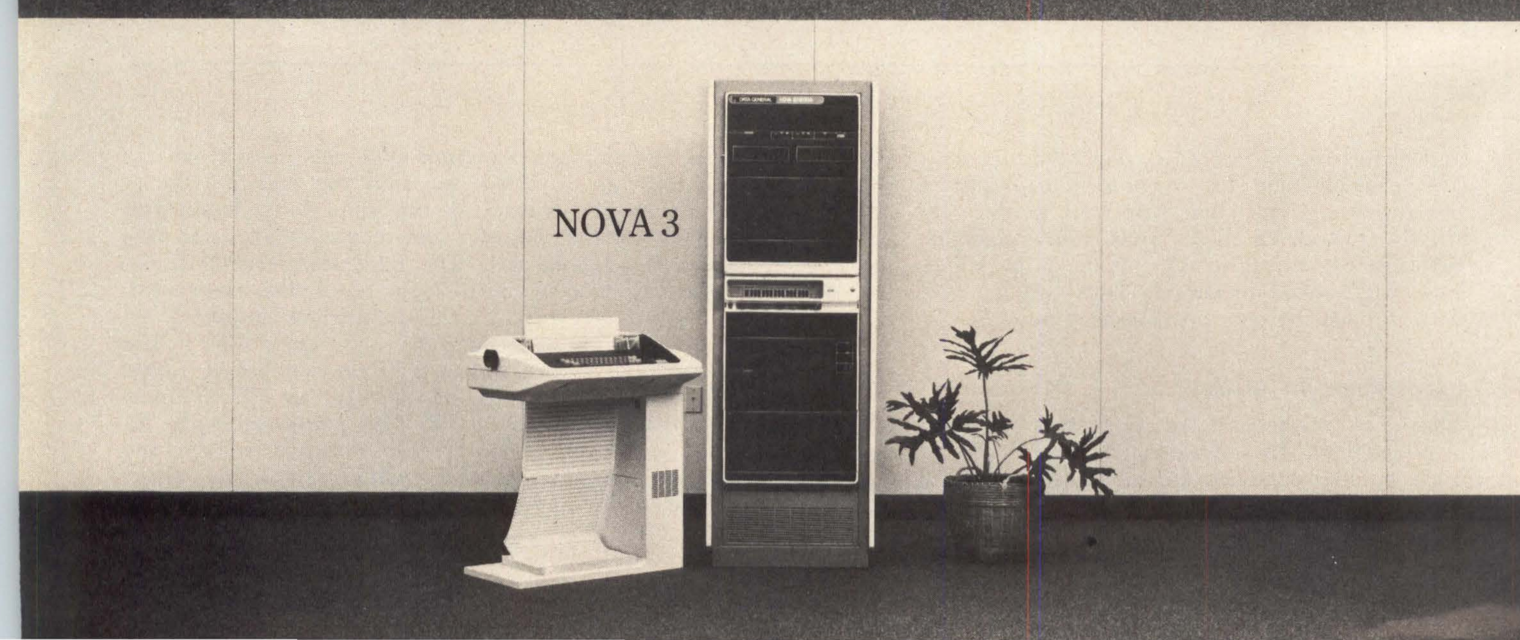

ECLIPSE S/130*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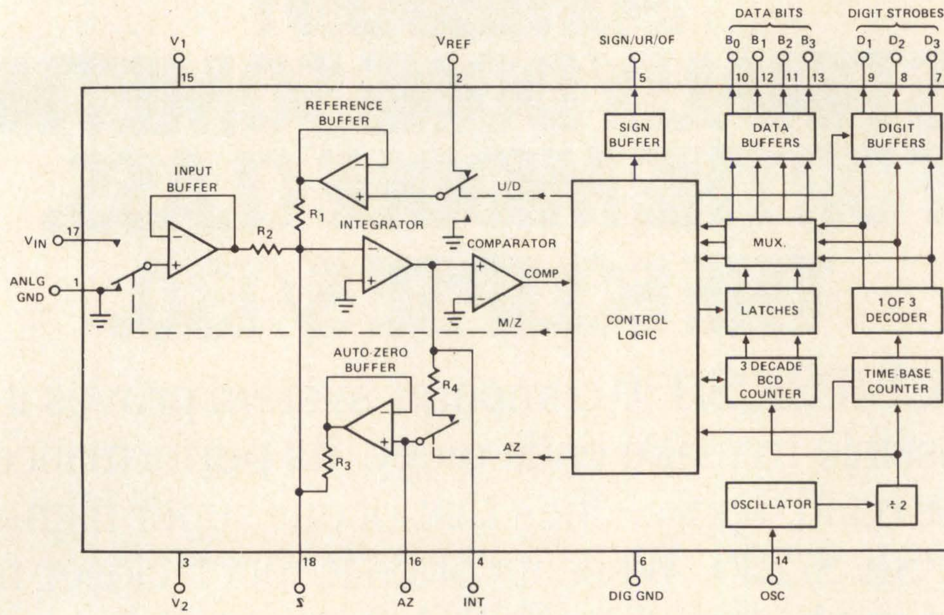


Fig 5 LD130 ADC (Courtesy Siliconix Inc)

Principal advantage of the integrating-type ADC is a very low cost coupled with the potential for high resolution. Low cost is attributable principally to the absence of the precision ladder network which requires an expensive trimming process. These devices have high resolution and are typically three to four BCD digits, which is equivalent to 11 to 14 binary bits. Furthermore, because of the integration of the input signal, they are highly immune to noise. They are also highly linear and have guaranteed monotonicity; ie, there will be no missing codes because of the nature of the conversion process. Basic limitation of these devices is speed. The integration process is slow, typically 1 ms for 8-bit devices to as much as 20 or more milliseconds for 12-bit and 3+ digit BCD converters.

Two examples of integrating ADCs are the Motorola MC1505L/MC14435 2-chip set and the Siliconix LD130. The monolithic 1505 chip has all of the analog functions required to perform an integration conversion function. This includes the precision voltage reference as well as the switching network, integrator, and comparator. Only an external integrating capacitor is required, along with meters for full scale calibration and zero adjust. The 14435 chip contains the digital section of this converter including counters, latches, clock, and control circuitry. Together the chip set produces a ±3½-digit voltmeter function. With other control circuitry the 1505 has the accuracy necessary to produce a 4½-digit result, which is extremely good compared with other DACs.

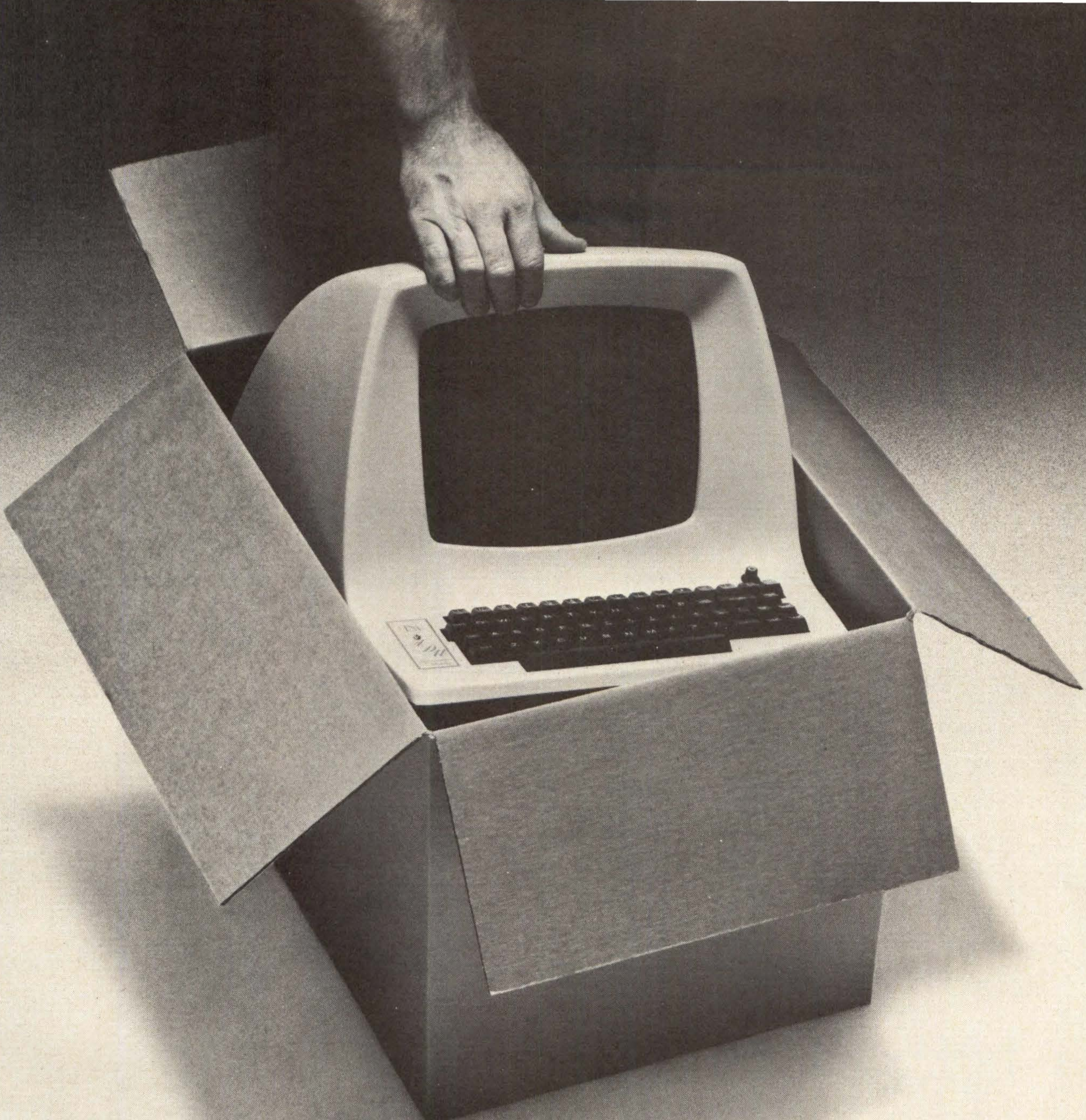
The LD130 ± 3-digit ADC is a monolithic device except that it requires an external precision voltage reference and the integrating capacitor, as shown in Fig 5. When the conversion is complete, the digits are strobed one at a time out of the data buffers on four lines, and an indication is made of the particular digit by strobe lines D1, D2, and D3. This is organized for use with digital panel meter displays but also creates an easy interface to a microprocessor system. A separate line indicates the sign of the result and also indicates if the input voltage was under or over range. These three indications are multiplexed, one each during the 3-digit output intervals. Other integrating converters are available from Datel in ADC-EK 8B/10B/12B converters which have 8, 10, and 12 bits of resolution, respectively. These devices cost between $10 and $35 in single quantities. High quantity pricing is literally a few dollars for integrating converters.

A variation of this process, known as "quad" slope integration, is utilized by Analog Devices in the AD7550 monolithic 13-bit integrating converter. This converter is specifically organized to multiplex the output bias on 3-state lines with 3-state gates for microprocessor compatibility. These integrating devices are particularly useful for applications requiring only low speed conversion and inexpensive conversion circuitry. They are easily used with any microprocessor.

Counter-Type ADCs

Of the several counter-type ADCs on the market today, two of the most interesting are the Ferranti ZN425E and the virtually identical Datel ADC-MC8. As shown in Fig 6, these devices incorporate a DAC together with a binary counter and input selector switch control circuit. They can be used as 8-bit DACs with 1-μs typical settling time by selecting the input from the eight external data input lines.

To utilize these devices as a building block for an ADC the input selector switch is set high, which puts



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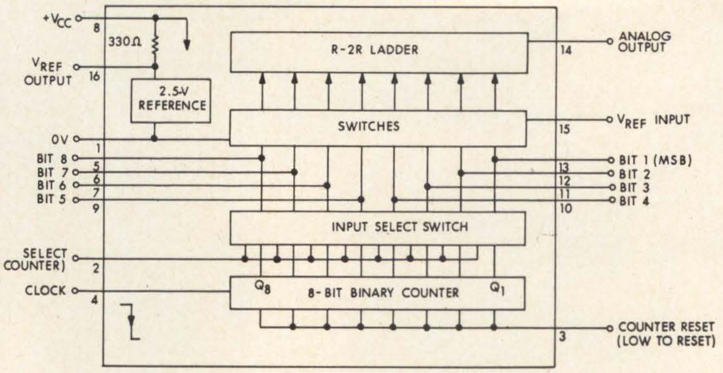

Fig 6 ZN425E counter-type ADC (Courtesy Ferranti Electric, Inc)

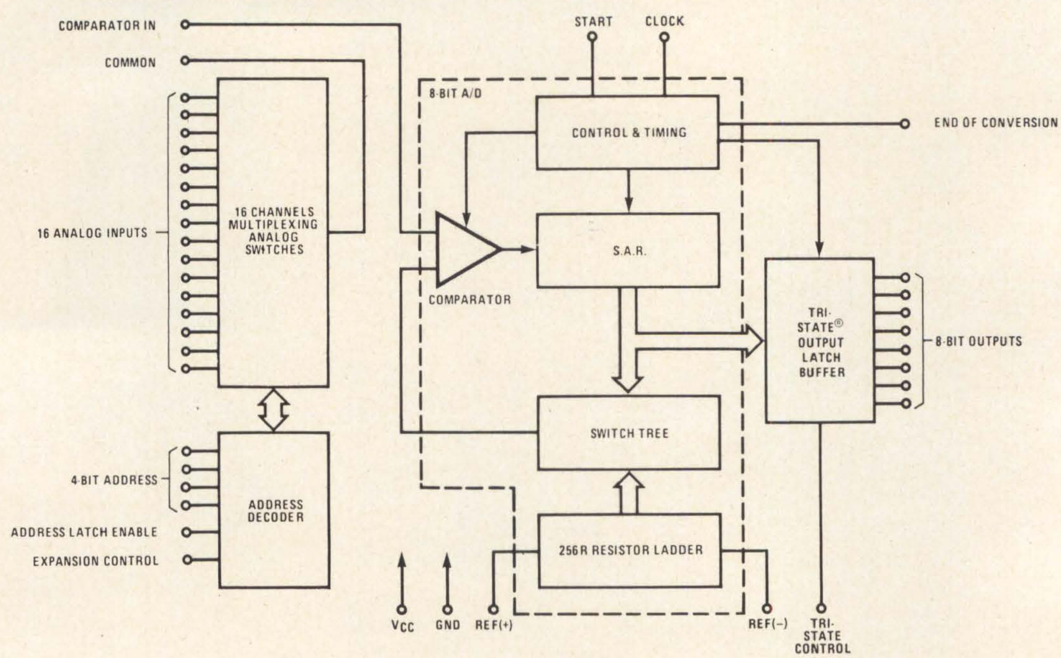

Fig 7 ADC0816-0817 single-chip data acquisition system (Courtesy National Semiconductor Corp)

the 8-bit binary counter as the control R2R network. The counter receives an external clock and an external reset control. The external clock causes it to reset to zero and begin counting, thereby creating an analog output which is a ramp function. By utilizing an external comparator circuit, this ramped analog output can be compared with the unknown analog input until a match occurs. At this time a simple TTL circuit gates the clock off, which holds the binary counter. The count is available on the count lines to read the digital value. To employ this device with a microcomputer to create an inexpensive ADC the output of the comparator would be used to trigger the microcomputer interrupt signal. The microcomputer would then input the data bits through an input port. The microprocessor could, under software control, reset the counter and start the count operation once again. These devices are extremely inexpensive, $8 in single quantities and $6 in hundreds, and can be utilized to implement inexpensive microprocessor compatible 8-bit ADC systems with conversion times of under 300 μs.

For still higher speeds, however, several monolithic successive approximation register (SAR) type ADC units are available. The Analog Devices AD7570 is a CMOS 10-bit monolithic SAR type ADC with a 20-μs conversion time. It is microprocessor compatible in that the 10-bit output of this device is available from two groups of 3-state output lines. The low order eight bits and high order two bits are enabled by two separate enable signals, thereby easing direct connection to the data bus without the need for an intervening input/output port. The device does not include a precision voltage

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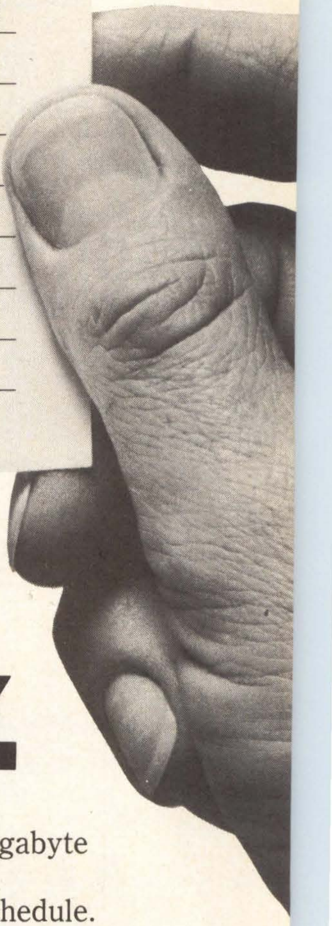
MTBF (hours x 1000)	4	4	4	4	4	4	4	4	4
SMD (differential) interface			■	■	■	■	■	■	■
TTL interface	■	■	■	■	■				
Subsystems available	■	■	■	■	■				
Contract service available	46 cities					Less than 13 cities			
Lowest price/qty. 200	$4097					More than $4400			
Availability (typical)	30 days ARO					?			



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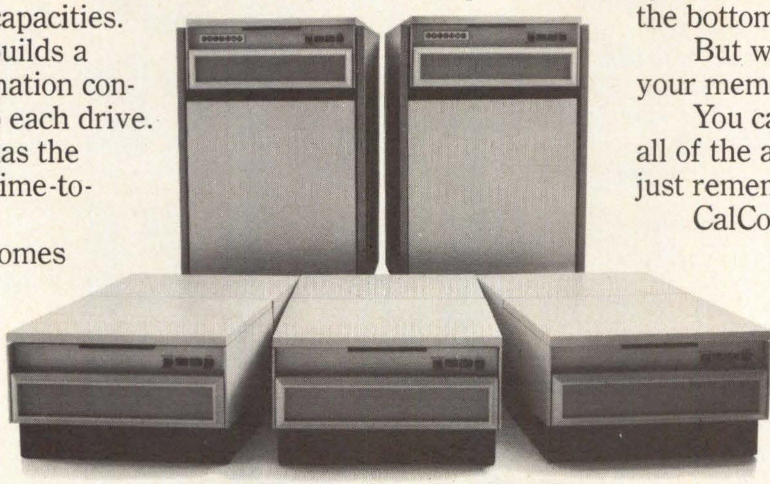

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reference because many microprocessor applications do not require an absolute voltage measurement. Instead ratiometric operation is used, in which each input is recorded as a percent of the full scale for that particular input channel. Many processor control applications require only ratiometric conversion and, therefore, the added expense of a precision voltage reference is not warranted. However, one can be added externally at slight expense if absolute voltage measurements are required.

ADCs for 1978

A particularly impressive development in monolithic ADCs is TRW's TDC1001. This 8-bit monolithic converter utilizes bipolar technology and successive approximation techniques to perform extremely high speed conversion (400 ns). The device is quite linear, ±½ LSB over the full temperature range (not just at room temperature). The converter has guaranteed monotonicity (no missing codes) and is ideal for high speed data acquisition requirements as well as radar and video data conversion. Still higher speed devices planned for introduction by the end of 1978 include an announced TDC1007 model with a conversion time of only 80 ns. This device will dissipate 4 W in a 64-pin chip with built-in heatsink and cooling fins.

Perhaps the most important development in monolithic converters is the National Semiconductor ADC0816/0817 single-chip data acquisition system. As shown in Fig 7, this device incorporates not only a full 8-bit ADC but also a 16-channel, externally expandable analog multiplexer. It is specifically designed for easy use with microprocessor systems. The 8-bit output signal is held in a 3-state buffer for direct attachment to the data bus. In addition, the 4-bit input address to select one of 16 input channels is latched into the address decoder, so that the microprocessor can perform an output instruction and have the data acquisition system hold the address of the channel that has been selected. Note that the output of the multiplexer is not connected directly to the input of the comparator, but is brought to an external pin. At this point it could be jumpered directly to the comparator input pin. Alternatively, it could first be routed to other external signal conditioning circuitry, eg, instrumentation amplifiers or sample and hold circuits. This device has a guaranteed linearity of less than ±½ LSB, guaranteed monotonicity with no missing codes, and a relatively fast conversion time of 100 μs.

As with the AD7570, the ADC0816/0817 does not incorporate a built-in voltage reference; it relies on ratiometric conversion, but an external reference could be provided for absolute measurements. Furthermore, because this chip is implemented with CMOS technology, it requires only 15 mW. Perhaps the most exciting news of all is the low price—$20 in quantities of 100.

Summary

These devices and those described in last month's column indicate the progress that has been made within the last two years in monolithic data conversion devices. They spell the beginning of an era of low price conversion from the analog to the digital domain. Perhaps the next step that we might expect within the coming year would be integrating some of these devices directly onto a microprocessor or single-chip microcomputer.

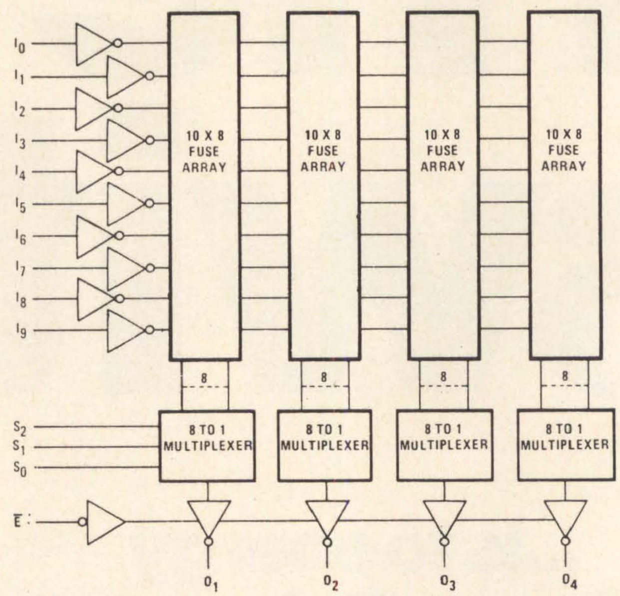
Field Programmable Multiplexer Offers Data Routing Flexibility for Prototype Systems

Much as a p/ROM provides flexibility for a designer when organizing memory in a prototype system, a PMUX (programmable multiplexer) offers flexibility in the routing of signals in that system via electrically programmable data routing. The 29693, introduced by Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94040, contains four 8-line-to-1-line multiplexers with common Select and Enable lines. Ten buffered TTL input lines form a matrix with 32-bit lines to provide 320 nichrome fusible links on the chip.

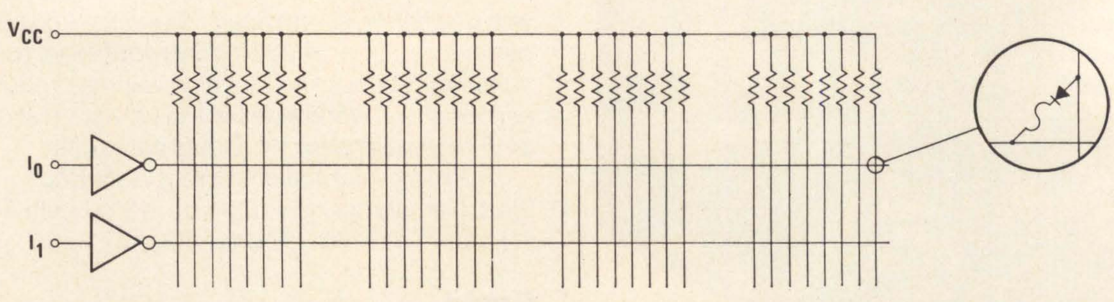
As shown on the diagram, 10 inputs (I_0-I_9) feed through four 10 x 8 fuse arrays, and eight lines from each array feed into the 8-to-1 multiplexers. Each of the four multiplexers has a single 3-state, 16-mA output (O_1-O_4).

The device, equivalent to four 74LS151 multiplexers, can be a FLPA replacement in many applications. It is shipped with each multiplexer input connected to all 10 device inputs through isolation diode-fuses or links, resulting in a logical OR of the input signals. To remove unwanted connections, short, high current pulses are passed through corresponding fusible links. These pulses open the links, changing them from conductive to nonconductive states. In a typical case nine of the ten links on each multiplexer input will be opened, except where the designer wants logical OR of two or more input signals.

Programming is achieved by applying the desired multiplexer select code, taking the input to be disconnected to a TTL high with all other inputs low, and applying programming pulses on the Enable input and the multiplexer/device output. If all fusible links on a multiplexer input are programmed, the multiplexer output will always be low when that input is selected. If more than one link is left unprogrammed on a multiplexer



Block diagram of Raytheon Semiconductor 10-input programmable multiplexer (PMUX). Any device input (I_0-I_9) can connect to each of eight multiplexer inputs through fusible link in 10 x 8 array. Each of four multiplexers has single 3-state output (O_1-O_4)

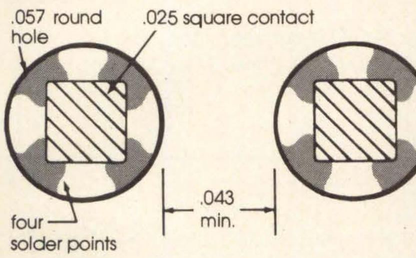


Internal construction of fuse arrays in PMUX. Each of 10 device inputs (only I_0 and I_1 are shown here) is initially connected to each of 32 multiplexer inputs (four multiplexers times eight inputs each) through isolation diodes (insert), providing total of 320 fusible links on each chip. PMUX can be programmed much like p/ROM by standard 29660 compatible p/ROM programmer and adapter card

No more square tails in round holes.

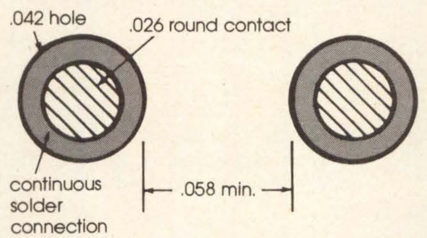
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example — converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what...it works.

At last — The obvious answer



Our own design engineers, not afraid of doing the obvious and simple thing, have done just that. They've taken a series of our PC wire wrap connectors — and given them .026" round tails. Everything else stays the same: the insulator, semi-bellows contacts, pin and row spacing.

So what?

So — the .026" round pin slips into a .042" round hole in your PC board for an excellent solder connection. So — you can now get multiple tracings between rows.

We have two tail lengths: a .200" short one and a .250" longer one to take the AS400 Solderpak** System. These are available in connectors with contacts on .100", .125" and .156" centers, and in layouts from 6 to 50 positions.

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CIRCLE 110 ON INQUIRY CARD

input, the output will be the logical OR of the two corresponding input signals.

The 29693 PMUX is compatible with programming pulses used on the 29660 (256 x 4) p/ROM. Therefore, the PMUX can be programmed using a standard p/ROM programmer capable of programming that p/ROM. An adapter card is required to convert address signals from the programmer into signals for the Select and input lines at the PMUX. The five most significant bits of the p/ROM address drive a decoder which selects one PMUX input line; the three least significant p/ROM bits drive the Select lines. Because the PMUX output structure is similar to that of the p/ROM, the adapter unit allows each PMUX fuse to be identified for programming as with p/ROM fuses.

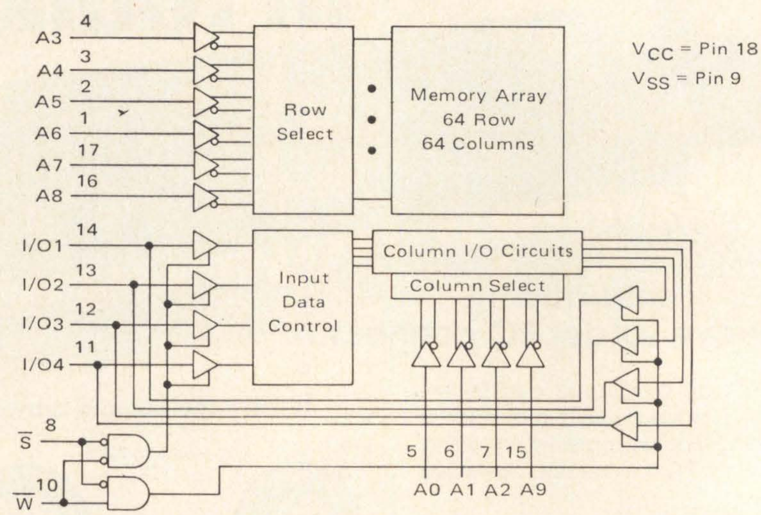
Absolute maximum ratings for the 20-pin device include dc input voltage, −0.5 to 5.5 V; dc input current, −30 to 5 mA; dc voltage applied to outputs except during programming, −0.5 to 5 V; storage temperature, −65 to 150°C; and ambient temperature under bias, −55 to 125°C. During programming, dc voltage applied to outputs is 26 V and output current into outputs is 125 mA. Operating temperature ranges are 0 to 75°C for the commercial version and −55 to 125°C for the military.

Circle 350 on Inquiry Card

1024-Word x 8-Bit Static RAM Enables Simple Interfacing

Four speed ranges—200, 250, 300, and 450 ns—are available in the MCM2114 static RAM, a 1k x 4-bit n-channel device. The standard chip has a 550-mW power requirement while a 21L14 version dissipates only 385 mW max. Both use a single 5-V supply with ±10% tolerance; are directly compatible with DTL and TTL; and require no clocks, timing strobes, or refreshing since operation is fully static.

Industry standard 18-pin DIPs are available in plastic or lid-seal ceramic from Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721. Data access is simplified since address setup times are not required. Data out and data in have the same polarity.



Motorola Semiconductor 4k-bit static RAM. Four versions allow choice of 200-, 250-, 300-, or 450-ns access/cycle times. Only single 5-V supply is required

Recommended dc operating conditions for the 2114 include 10-μA max input load current; 10-μA max I/O leakage current; 95-mA max, 80-mA nom power supply current (65-mA max for the 21L14); 100-mA max power supply current (70-mA max for the 21L14); 0.8-V max, −0.5-V min input low voltage; 6-V max, 2-V min input high voltage; 6-mA nom, 2.1-mA min output low current; −1-mA max, −1.4-mA nom output high current; and 40-mA max output short-circuit current. Absolute maximum ratings are −10 to 80°C temperature under bias, 5-mA dc output current, 1-W power dissipation, −0.5- to 7-Vdc on any pin with respect to the source supply, 0 to 70°C operating range, and −65 to 150°C storage range. Ac operating conditions and characteristics include 0.8- to 2-V input pulse levels, 10-ns input rise and fall times, and 1.5-V input and output timing levels.

Circle 351 on Inquiry Card

4-Bit Slice Processors Offer Built-In Computational Algorithms

Two Schottky TTL 4-bit expandable binary micro/macroprogrammable processor element building blocks are intended for upgrading hardware performance while maintaining full software compatibility. The SN74S481 performs at a typical clock cycle time of 90 ns at 345 mA of supply current; the low power SN54LS/74LS481 has a typical clock cycle time of 120 ns but requires only 220 mA of supply current. Both versions are available now from Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 in 48-pin quad-in-line ceramic packages; at a later date commercial versions will be available in plastic DIPS.

Quad-port computer architecture provides full parallelism as well as fast throughput rates in either a memory-to-memory or register-to-memory system. The number of general-purpose registers is limited only by the size of the directly accessible memory locations.

A memory-to-memory system places the register file function in main memory and is said to be able to handle interrupts or context switches faster

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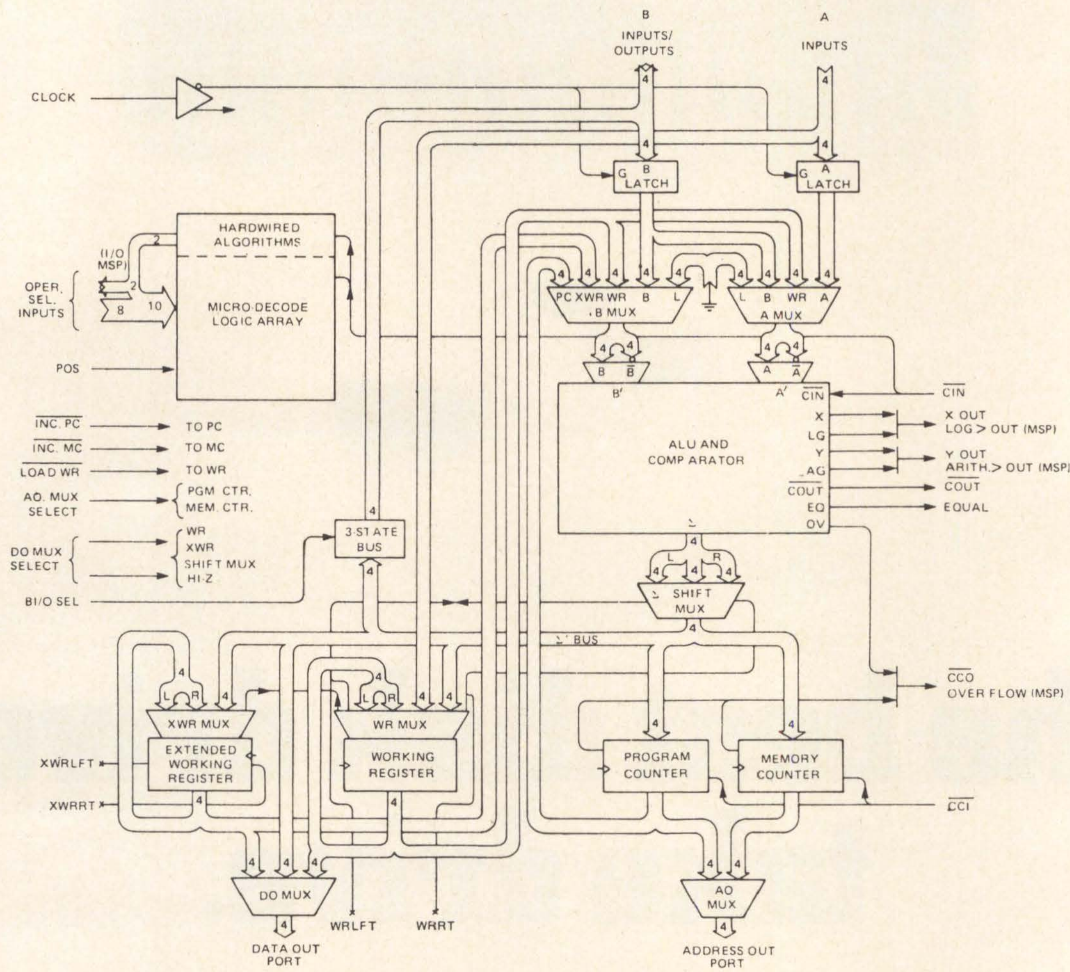
CIRCLE 111 ON INQUIRY CARD



Texas Instruments 4-bit slice processor. Two versions are said to be first to offer built-in computational algorithms. Main element can recognize, decode, and execute any of 24,780 instructions within single 100-ns clock cycle

and more efficiently than conventional register-to-memory systems. Chief architectural features include microprogrammable, bit-slice design expandable in 4-bit multiples, full parallel dual I/O ports, full function ALU with carry look-ahead, magnitude, and overflow decision capabilities, double-length accumulator with full shifting capability and sign-bit handling, and dual memory address generators on-chip.

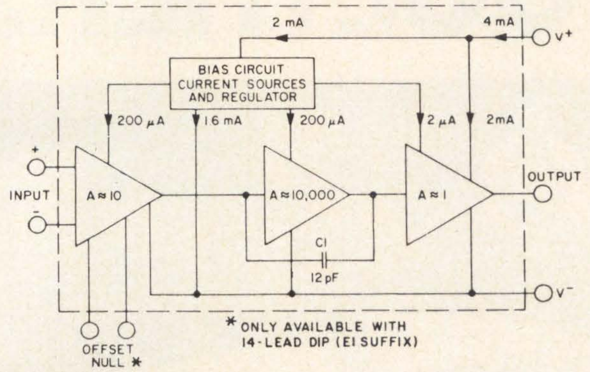
The architecture also features asynchronous access to data routing and counter updating controls. Simultaneous compound operations in the form of an ALU function with shift, destination selection with address/iteration updating, plus address and present data to memory can be accomplished in a single microcycle. Other operational features include simultaneous 1-clock compound operations, preprogrammed CRC and double precision multiply/divide algorithms, double length accumulator with full bidirectional single/double precision arithmetic/logical/circulate shift capabilities, full micro-operational control provided for programming, and relative position control defining bit-slice rank and sign handling in n-bit applications.

Circle 352 on Inquiry Card

Op Amps Combine MOS And Bipolar Advantages

Dual BiMOS operational amplifiers, said to combine the advantages of MOS and bipolar transistors on the same chip, have been announced by RCA Solid State Div, Rt 202, Somerville, NJ 08876. The CA3240 and 3240A operate from 4- to 36-V single or dual supplies and are characterized for ±15-V operation as well as TTL supply systems with operation down to 4 V.

Gate-protected MOS FET (p-MOS) input transistors provide very high input impedance (1.5 TΩ typ), very



Block diagram of one half of CA3240 series BiMOS op amp from RCA Solid State Div. Dual versions of standard CA3140 op amps feature 1.5 TΩ input impedance and 10-pA input current

low input current (10 pA typ at ±15 V), and a wide common-mode input voltage range (can be swung to 0.5 V below negative supply rail). Bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

Both devices are produced in 8- or 14-lead plastic DIPs and are pin-compatible with industry standard 747/1458 types in similar packages. Unmounted chips are also available.

Some electrical characteristics of the CA3240 devices (at 25°C) are 5-mV typ, 15-mV max input offset voltage (2-mV typ, 5-mV max for the 3240A); 0.5-pA typ, 30-pA max input offset current (20-pA max for the A); −15.5- to 12.5-V typ common-mode input voltage range; 0.4-V min, 0.13-V typ maximum output voltage; 8-mA typ, 12-mA max supply current; and 240-mW typ, 360-mW max total device dissipation. Bandwidth is 4.5 MHz unity gain at ±15 or 30 V and high voltage slew rate is 9 V/μs. Maximum operating range is −40 to 85°C; storage range is −65 to 150°C.

Circle 353 on Inquiry Card

8-Bit Data Acquisition Components Feature Word Rates to 900 kHz

A hybrid video sample/hold amplifier and a hybrid analog-to-digital converter, both high speed 8-bit data acquisition system components, are capable of word rates up to 900 kHz. The SH-8518 S/H amplifier features 25-ns acquisition time, 60-ps aperture uncertainty, and 20-MHz sampling rate. Linearity error is 0.05% and droop rate is 1 mV/μs. The unit is self-contained and includes an FET buffer amplifier. The ADH-8512 ADC uses successive approximation to achieve linearities of ±0.2% with a conversion time of 1 μs. Pin programmable inputs accept six different input voltage ranges, and the buffered digital output is available in either parallel or serial form.

Both of the matched pair of modules are hermetically sealed in 24-pin double width DIPs. Each is processed to MIL-STD-883, Class C; screening to Class B is a standard option. Temperature ranges are 0 to 70°C and −55 to 85°C. Base prices are $255 for the SH-8518 S/H amplifier, and $310 for the ADH-8512 ADC in quantities of 1 to 9 from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716.

Circle 354 on Inquiry Card

64k ROM Has 200-ns Access Speed, Uses Only 200-mW Active Power

Edge-Activated™ circuit design concept enables the MK 36000 ROM to operate at faster speeds than traditional ROM designs, but with much lower power dissipation and smaller chip area according to Mostek Corp, 1215 W Crosby Dr, Carrollton, TX 75006. The 8k-word x 8-bit device operates at a 200-ns access time but requires only 200-mW max active power and 25-mW standby power. It operates from a single 5-V power supply with ±10% tolerance. Other system features include fully TTL compatible inputs and outputs. Its 3-state output can drive two TTL loads and 100 pF.

The device is pin compatible with existing EPROMs and its 24-pin configuration allows it to be used as an upgrade from 8k and 16k ROMs. Each increase in bit density requires that a chip select input be replaced by the necessary address pin.

Circle 355 on Inquiry Card

IIL, Linear, and Digital Technologies Combined On Monolithic ADC Chip

A successive approximation type analog-to-digital converter, the AD571 includes DAC, voltage reference, clock, comparator, successive approximation register, and output buffer on a single 120 x 150-mil chip. Two versions execute a complete conversion to 10-bit accuracy ±½ LSB with no missing codes in 25 μs over the specified temperature range (0 to 70°C for the 571K, −55 to 125°C for the 571S). A third version, the 571J provides 10-bit performance at 25°C, and 9 bits over the 0 to 70°C operating range.

Integrated-injection logic (IIL) technology is used in chip design and production to provide very high circuit densities. According to Analog Devices Semiconductor, 829 Woburn St, Wilmington, MA 01887, this application is the first time in bipolar technology that linear and digital circuitry are combined on a single IC chip. The device is also said to be the first monolithic ADC to be laser wafer trimmed.

(Continued on p 206)

DEEC

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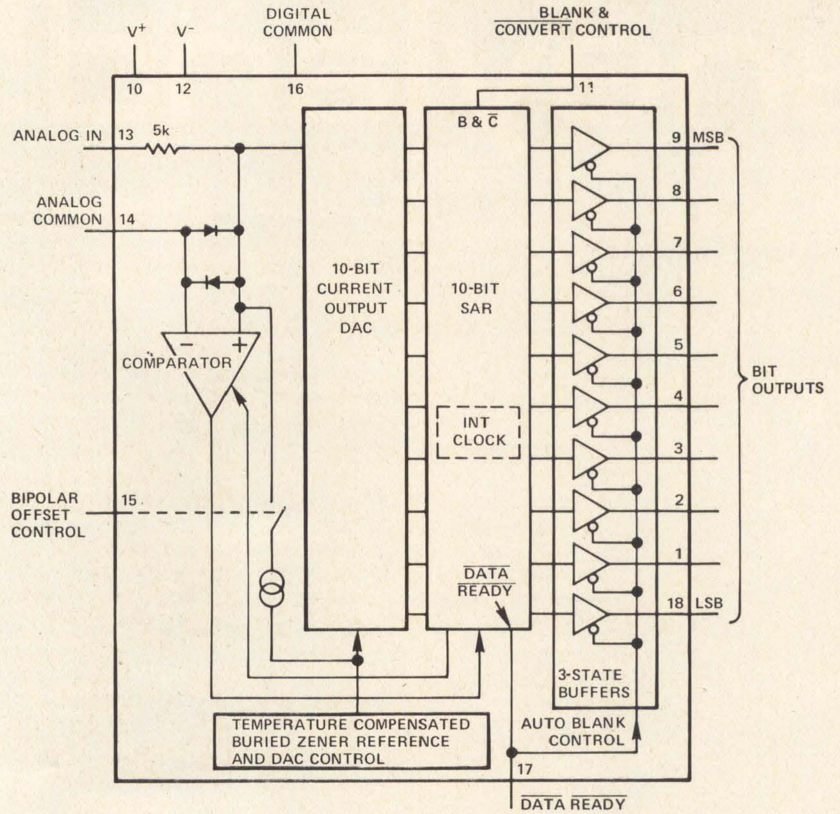


Analog Devices 10-bit ADC. Very high circuit density results from IIL technology. Linear and digital circuitry are combined on bipolar chip

Guaranteed full scale temperature coefficients for the J, K, and S versions, respectively, are 88, 44, and 40 ppm (comparable to tempco errors of all components in the circuits). Precision, temperature-compensated, buried zener references insure long term device stability.

Prices of the J, K, and S devices, respectively, are \$25, \$36, and \$52 in 100 quantities. For 1000 quantities the respective prices are \$21.50, \$34.50, and \$49.50. S versions are also available fully processed to MIL-STD-883A, Class B.

Circle 356 on Inquiry Card

Op Amps Feature Matched JFET Inputs on Single Monolithic Chip

Three series of operational amplifiers featuring matched JFET input structures on the same monolithic chip as bipolar devices are designed for low noise applications. They feature low input bias and offset currents as well as low offset voltage and offset voltage drift, plus offset adjust which does not degrade drift or common mode rejection. The series use either high or low impedance sources for precision high speed integrators, fast A-D or D-A converters, high impedance buffers, or as wideband, low noise, low drift amplifiers.

Common features for all three series, available from Signetics, PO Box 9052, Sunnyvale, CA 94086, are an input bias current of 30 pA, input offset current of 3 pA, input impedance of 1 TΩ, input offset voltage of 1 mV, V_{OS} temperature drift of 3 μV/°C, and input noise current of 0.01 pA/Hz^{-2}.

Specific features for the LF155, 156, and 157 series, respectively, include settling times of 4, 1.5, and 1.5 μs; slew rates of 5, 12, and 50 V/μs; bandwidths of 2.5, 5, and 20 MHz; and input noise of 20, 12, and 12 nV/Hz^{-2}. Operating temperature ranges for the three series are −55 to 125, −25 to 85, and 0 to 70°C. Absolute maximum power supply voltages are ±22, ±22, and ±18 V; power dissipations are 670, 570, and 500 mW.

Circle 357 on Inquiry Card

Plastic Package Op Amp Features Low Offset Voltage and Low Drift

OP-07CP ultra-low offset voltage op amp, in an epoxy 8-lead mini-DIP for use with automated component insertion equipment, is capable of maintaining an input offset voltage below 250 μV over an ambient temperature range of 0 to 70°C. This performance is achieved without resorting to an external trimming potentiometer. Maximum long term input voltage drift is 2.0 μV/month.

Available from Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050, the low noise, chopperless bipolar device is intended for integrators and precision summing amplifiers or for ultra-precise voltage threshold detector applications. Input noise voltage is 0.65 μV or less from 0.1 to 10 Hz.

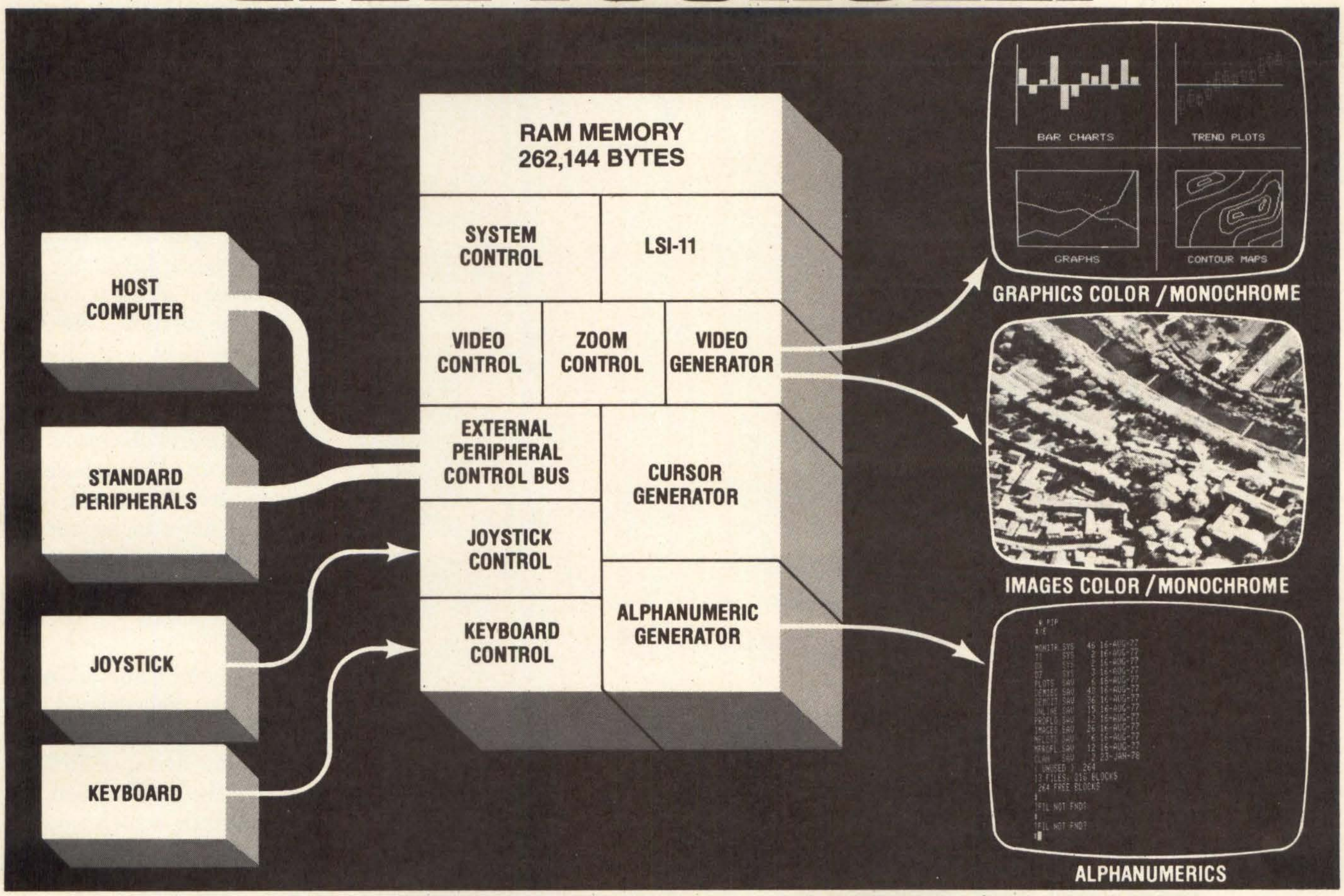
Because of the low input voltage, this device can replace either modular or monolithic chopper-stabilized amplifiers at lower cost, noise, size, and power consumption. Both manufacturing and field calibration are eliminated since no external nulling is required.

Stable operation is maintained with load capacitances up to 500 pF and input voltage swings of ±10 V. Supply voltage requirement ranges from ±3 to ±18 V.

The device is a direct replacement for the 725, 108A/308A, and OP-05 amplifiers. It also can be used to replace 741 series devices by simply disconnecting the 741 nulling potentiometer. □

Circle 358 on Inquiry Card

GIVE YOURSELF



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Microcomputer Digital Equipment Corporation LSI-11 microcomputer provides high speed capability and has an instruction set compatible with the PDP-11 series. The system provides a powerful stand-alone computer capability.

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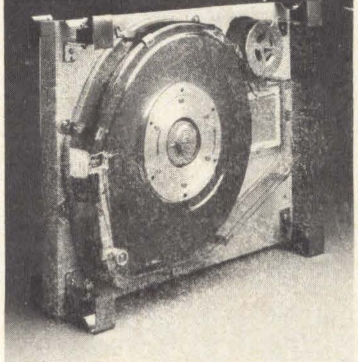
PRODUCT FEATURE



See at NCC Booth 2445.

Winchester-Technology Hard Disc Drives Interface With Floppy Drives for Increased Mass Storage

Its first rigid disc drive products have been announced by Shugart Associates, known until now as an independent manufacturer of floppy disc drives. The company claims that its drives are more compact and less expensive than any comparable fixed disc units available to OEMs today yet are compatible with IBM Systems 32 and 34 and Series 1. Industry-proven Winchester technology is utilized in the 35-lb (16-kg) units which fit 19" (48-cm) RETMA racks with 5.25" (13.3 cm) of panel space.

Two configurations are available: one disc and four heads (model 4004) and two discs and eight heads (model 4008). Eight optional fixed heads provide an additional 144k bytes of head-per-track storage. Full compatibility permits mass storage capacity to be provided to present floppy disc systems at low cost. For instance, because voltage requirements for the fixed disc drive are the same as for the company's IBM compatible floppy drives, the same power supply can be used for both drives in the system. Also, a single intelligent controller can handle up to four floppy drives and four fixed disc drives. (A data separator/encoder is included in the fixed disc drive to provide normalized NRZ read/write data because the fixed disc drive has a higher transfer rate than the floppy drives.)

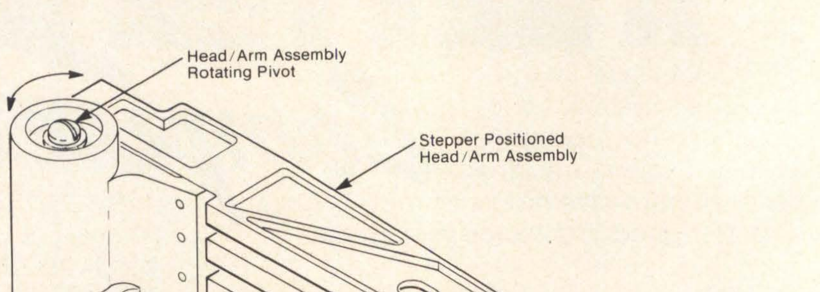


Diagram showing Fasflex II™ band actuator and relationship to arm assembly and read/write heads. Precision stepping motor drives capstan. Virtually wearproof stainless steel actuator produces very little friction or heat

Design Features

The SA4000 fixed disc drive is made up of read/write and control electronics, VFO (variable frequency oscillator) data separator, MFM (modified frequency modulation) encode/decode electronics, read/write heads, track positioning mechanism, drive mechanism, discs, and air filtration system. Electronics are packaged on four printed circuit boards: read/write, actuator driver, control, and data separator. A drive motor rotates the disc spindle at 2964 r/min through a belt drive system that is changeable to accommodate 50- or 60-Hz power.

Fasflex II™, a band actuator based on the same design concepts as the actuator used in the company's double-sided floppy drive, eliminates the more expensive voice coil or slower lead screw type actuator mechanism used in most Winchester technology drives. A stainless steel band (see diagram) wraps around a capstan which is driven by a precision stepping motor. In turn, the actuator precisely positions an arm containing the Winchester-type read/write heads.

Data are written on or read from each disc surface by two read/write heads, each of which accesses 202 tracks. A separate read/write head mounted on the base casting reads a prerecorded track which provides the master clock for the drive as well as the clock for write clock generation. Optional fixed heads are mounted on an assembly which is mounted directly on the base casting.

A clean environment for the module enclosing discs and read/write heads is attained by use of an integral recirculation air system with an absolute filter. A separate filter breather permits equalization of pressure with ambient air without contamination.

Specifications

Encoding method for these fixed disc drives is modified frequency modulation. Storage capacities are 18k bytes/track and 7.3M bytes/surface unformatted; 60 sectors/track, 256 bytes/sector, 15.4k bytes/track, and 6.2M bytes/surface formatted. Models 4004 and 4008, respectively, have total unformatted capacities of 14.5M and 29.0M bytes and formatted capacities of 12.4M and 24.8M bytes. Other performance specifications, identical for both models, include transfer rate of 889k bytes/s and seek times of 20 ms track to track, 87 ms avg, and 220 ms max.

Functional specifications include 2964-r/min rotational speed, 5600-bit/in (2200/cm) recording density, 5600-fc/in (2200/cm) flux density, and 172-track/in (68/cm) track density. There are 202 cylinders and 808 tracks, and physical sectors are programmable. Environmental limits are 50 to 105°F (10 to 41°C), 8 to 80% relative humidity, noncondensing.

Ac power requirements are 50/60 Hz ±0.5 Hz and 90 to 127 V at 1.5 A typ for 100/115-V installations (180 to 253 V at 0.8 A typ for 200/230-V installations). Dc requirements are 24 V ±10% 2.5 A typ, 5 V ±5% 2.5 A typ, and −7 to −16 V (optional −5 V ±5%) 0.1 A typ.

Mechanical dimensions, exclusive of front panel, are height 5.1" (12.95 cm), width 16.6" (42.16 cm), depth 21.9" (55.63 cm), and weight 35 lb (15.9 kg). Heat dissipation is 682 BTU/h (200 W) typ. Predicted reliability specifications are MTBF of 5000 power-on hours typical usage, MTTR of 30 min, and component life of 5 yr. Soft read errors are 1 per 10^{10} bits read, hard read errors are 1 per 10^{12} bits read, and seek errors are 1 per 10^{6} seeks.

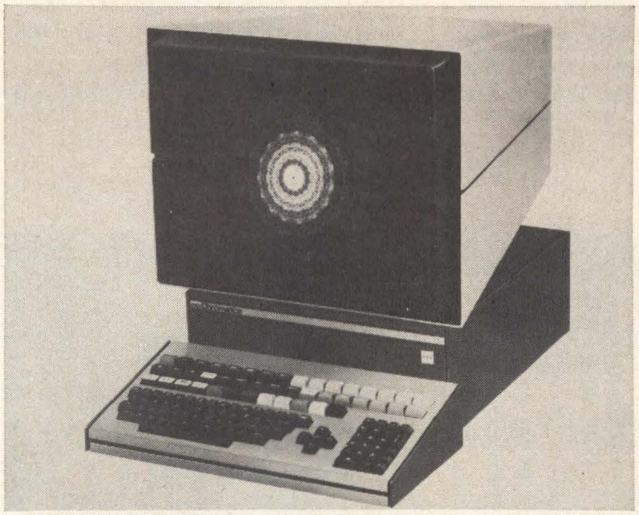
Price and Delivery

The model 4004 14.5M-byte drive sells for $2550 in single quantity and $1450 in 100 quantity. Prices for the model 4008 29M-byte drive are $3500 and $2000 for similar quantities. Full OEM discounts are available. Delivery is 120 days ARO. Shugart Associates, 415 Oakmead Pkwy, Sunnyvale, CA 94086. Tel: 408/733-0100.

For additional information circle 199 on inquiry card.

PRODUCTS

Line of Single-Package Graphic Display Systems Supplies High Resolution Color Capability



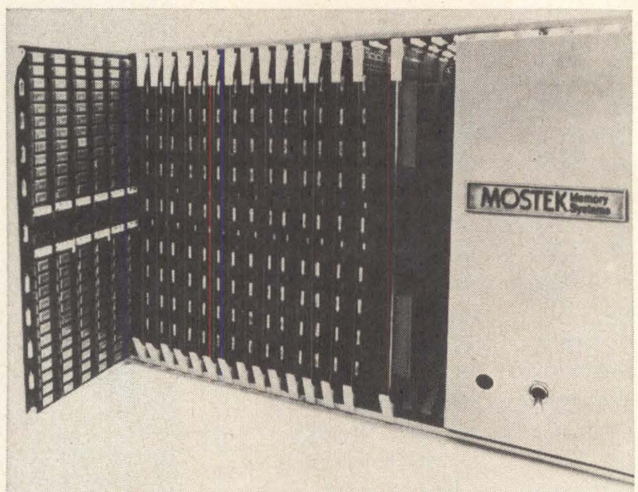
The CG line of 8-color graphic and alphanumeric readout systems consists of models employing a Z80 CPU with full memory and I/O structure. The low cost devices are available in 13, 15, and 19" (33-, 38-, and 48-cm) color screens with high resolution shadow mask tubes. Graphics functions include automatic generation of circles, arcs, rectangles, solid-filled objects, and vectors, with resolutions of 512 x 256 and 512 x 512 individually selectable and color definable dots. Alphanumerics may be placed at any point on the screen and multiplied to any integer size. Std ASCII set is provided along with 96 separate user definable graphic symbols. Std interfaces include 128-key keyboard, synchronous and asynchronous variable baud rate serial I/O with TTL and RS-232-C. A windowing capability is also included. Software, interfaces, graphic symbols, and peripherals are optional. **Chromatics, Inc**, 3923 Oakcliff Industrial Ct, Atlanta, GA 30340.

See at NCC Booth 1726
Circle 200 on Inquiry Card

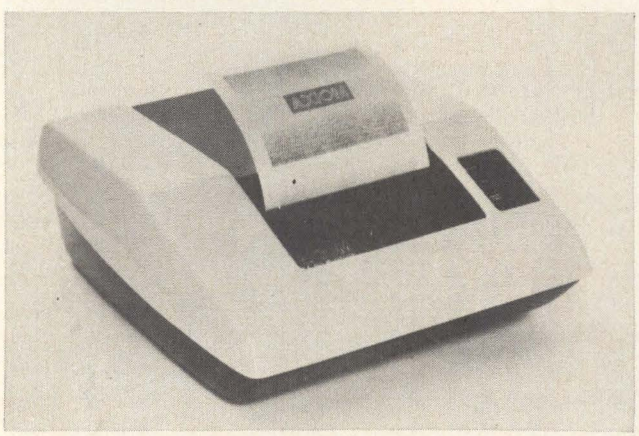
Versatile 5M-Byte Add-On Memory System Serves Mass Storage Applications

A general-purpose 12.25" (31-cm) memory chassis with total capacity of 5M bytes, the MK 8600 is suited to such uses as mainframe add-on memory and disc replacement. The company's MK 8000 memory card is used, featuring from 16k x 18 to 128k x 24 words of storage. Std access time is 250 ns with a cycle time of 450 ns. Dynamic RAMs reduce overall power consumption and board temp for high reliability. Configuration of the chassis with power allows for up to 16 of the boards, plus ECC; 4 additional slots are available for specific customer I/O needs. Other features include byte control, busable address and data, and inverting or noninverting data. For smaller needs, the MK 8601 7" (18-cm) chassis with 1M-byte capacity is offered. **Mostek Corp, Memory Systems Div,** 1215 W Crosby Rd, Carrollton, TX 75006.

See at NCC Booth 3415
Circle 201 on Inquiry Card



Electrosensitive Standalone Printer/Plotter Combines Graphics and Alphanumerics



Using an electrosensitive printing technique, the EX-820 desktop MicroGraphics printer allows high resolution graphics and full 96-char ASCII alphanumerics to be mixed on any line. Software commands permit the user to define the size of each graphic field, and choose from 4 preprogrammed horizontal dot resolutions up to 128 dots/in (50/cm). Vertical dot resolution is fixed at 65 dots/in (26/cm). There also is provision for automatic histogram generation. Driven by an Intel 8048, the printer uses 5" (13-cm) wide electrosensitive paper for permanent, high contrast printouts. Std features include RS-232-C/20-mA serial input as well as parallel ASCII, 512-char multiline asynchronous input buffer, and software selection of 3 char sizes for 80, 40, or 20 cols, as well as reverse printing. Optional 2k-byte p/ROM allows input data to be formatted automatically to user specs. **Axiom Corp,** 5932 San Fernando Rd, Glendale, CA 91202.

See at NCC Booth 52
Circle 202 on Inquiry Card

When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is its cost; at $1,095 in quantities of 100 or more, it's the most versatile terminal for the price you can get your hands on.

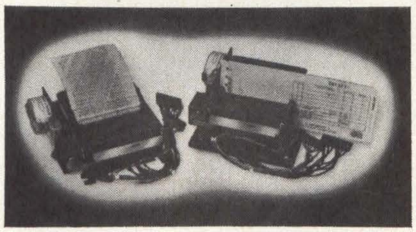
More information on the I-400 is quickly within your grasp. Call Infoton toll-free at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth at Infoton, Second Avenue, Burlington, MA 01803.

Infoton 400

Prepared by Chickering/Howell, Los Angeles.

CIRCLE 115 ON INQUIRY CARD

ALPHANUMERIC PRINTER CONTROL INTERFACE



Model 4-621-9205, designed for use with the company's PR series 15- and 21-col impact printing mechanisms, uses an F8 3-chip microcomputer set consisting of 3850 CPU, 3853 SMI, and 3851 PSU. Designed to accept ASCII serial, ASCII parallel (8-bit), RS-232-C, and BCD parallel (4-bit) data entry formats, the control/interface board contains a ROM character generator, full line buffer, timing control, full handshaking facilities, selectable parallel or serial baud rates to 2400 char/s. **Sheldon-Sodeco Printer, Inc, a Landis & Gyr co,** 4 Westchester Plaza, Elmsford, NY 10523.

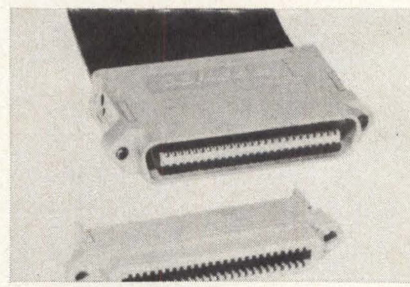
Circle 203 on Inquiry Card

HYBRID SOLID-STATE RELAY

Featuring a reed relay which operates on 5-V DTL or TTL input without relay driving buffers and a triac output which handles high power ac loads of 10 and 25 A at 120 or 240 Vac, relay is housed in an industry std power package using a high temp thermoset plastic. Min life is rated at 20M operations for 120-Vac models and 10M for 240-Vac operations. Relays incorporate a heavy duty dv/dt filter and are designed to control a variety of loads. **C P Clare & Co,** 3101 W Pratt Ave, Chicago, IL 60645.

Circle 204 on Inquiry Card

IEEE-488 STANDARD RIBBON CONNECTORS



Capable of being mass terminated in seconds to std 50-mil pitch flat cable without wire stripping or soldering, 1-piece male and female Blue Macs[R] ribbon connectors feature insulation displacing Tulip[R] contacts on 0.050" (0.127-cm) centers, and I/O mating ribbon contacts on std 0.085" (0.216-cm) centers. Current rating is 3 A, insulation resistance is >1 x 10^9 Ω, and dielectric strength is >500 Vac at sea level. Temp rating is −55 to 105°C. **T & B/Ansley Corp,** 3208 Humboldt St, Los Angeles, CA 90031.

Circle 205 on Inquiry Card

PUNCHED TAPE READERS

Step/Mate reader 2001-2 is designed for microprocessor software development, p/ROM programming, phototypesetting, and machine control applications. Features include punched tape reading at 150 char/s, complete tape drive electronics, and TTL compatible output/handshake signals. Wide-opening read head reduces read errors due to out-of-tolerance and skewed tapes; it is also bidirectional and self-cleaning. Compact reader is easily connected to system electronics. **EECO,** 1441 E Chestnut, Santa Ana, CA 92701.

Circle 206 on Inquiry Card

For Intelligent Family Planning

Think Ontel

Buying intelligent terminals . . . think Ontel! We've planned and engineered our family of intelligent terminal systems to meet maximum OEM user needs. With the recent introduction of the Ontel OP-1/R, the first truly user-programmable intelligent terminal in its price range, we've broadened our product family. We now offer powerful cluster systems. Master terminals coupled with intelligent slaves provide unique distributive processing capabilities.

Ontel terminals are more than just well-designed, flexible and reliable . . . they're low-cost total systems all engineered to complete *your* systems family.

Buying Intelligent Terminals? Think Ontel!

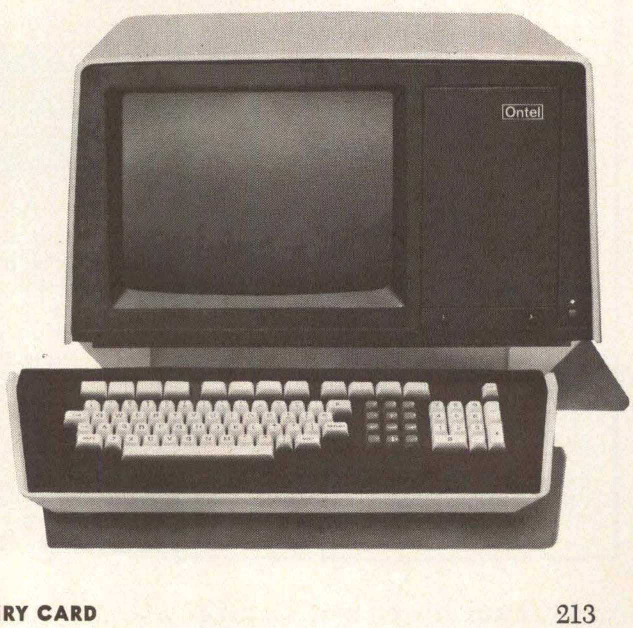
Supplying the software you need is a must. We offer 3 high level languages, forms generation, word processing, text editing, extensive utilities and diagnostics . . . all running under Ontel's Disk or Diskette Operating System. Ontel software enables our users to reduce their development costs for a multitude of different applications.

A few more facts. Ontel terminals have a modular structure with up to 64K of memory and are designed for field upgrade. They're easily programmed and have a full range of controllers including communications, mass storage and printer interfaces.

Contact Us Today For the Intelligent Answer

Edward J. Heinze
National Sales
Manager

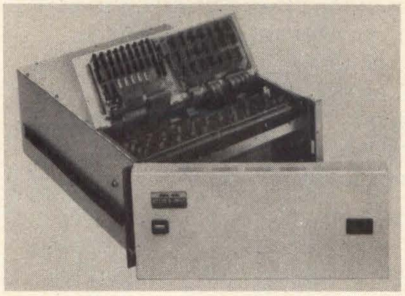
Ontel Corporation
250 Crossways Park Dr.
Woodbury, NY 11797
(516) 364-2121



CIRCLE 117 ON INQUIRY CARD

PRODUCTS

LOW COST HEAD-PER-TRACK DISC MASS MEMORY SYSTEM



The MODEL EIGHTY has a capacity range of 2 to 8 megabytes on one spindle with an average access time of 8.5 milliseconds. It employs a patented field-proven, fail-safe, retractable head design. The heads are locked up during non-operating modes. This substantially increases equipment reliability by allowing it to survive without damage the critical phases of transportation, installation, and handling.

The MODEL EIGHTY employs a field-proven, sealed disc/head chamber design that eliminates contamination from the external environment. It does not use or require filtered air or pressurization with an inert gas.

The MODEL EIGHTY features totally new head/disc magnetics, highly efficient data coding, modern electronic read-back signal equalization, balanced line/driver receivers in the external signal interface for maximum noise immunity, and advanced packaging concepts to minimize equipment size while maximizing ease of access to all replaceable parts.

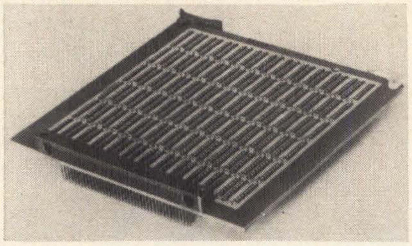
The MODEL EIGHTY is compatible with ALPHA DATA's computer controllers for Data General and DEC computers. A simple change of one interface card permits emulation of other manufacturers' products.

Liberal OEM discounts are available.

ALPHA DATA, 20750 Marilla Street, Chatsworth, CA 91311 • (213) 882-6500 TWX (910) 494-4914

PRODUCTS

IC WIREWRAPPABLE PANEL

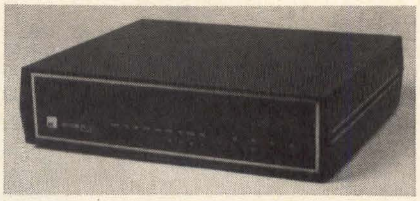


Pluggable IC wirewrappable packaging panels accept every IC size. High density 6000 series accommodates pin/socket style I/O connectors (120-pin male supplied with each panel) with 60 or 72 patterns std. Measuring 6.950 x 7.353 x 0.125 or 0.625" (17.653 x 18.677 x 0.3175 or 0.15875 cm), panels are double-sided with ground and power. 1-, 2-, or 3-level socket pins are gold or tin plated. **Excel Products Co, Inc,** 401 Joyce Kilmer Ave, PO Box 168, New Brunswick, NJ 08903.
Circle 207 on Inquiry Card

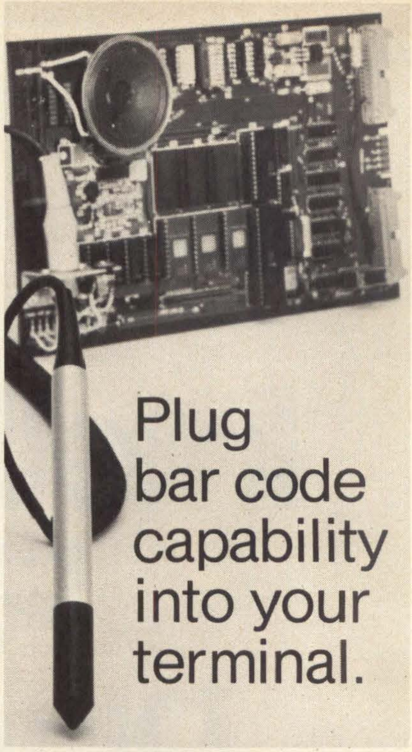
COMPUTER SYSTEM AIR CONDITIONERS

Compact Lobay[R] units with capacities of 5000, 6000, and 7000 BTUs are available in 9 models with choice of 115, 230, and 230 V, at 60, 60, or 50 Hz, respectively, in door or rack mounted versions. Using a closed-loop system to recirculate and cool the cabinet interior, the systems deliver a constant supply of air. 20k-h continuous duty is assured in a wide range of environments with ambient temps up to 52°C. **McLean Engineering Midwest,** 9560 85th Ave N, Maple Grove, MN 55369.
Circle 208 on Inquiry Card

2400-BIT/s MODEMS



Operating at 2400 bits/s 24 LSI Mark II modems provide a std range of pushbutton test features. Included are internal error, receive, and analog and digital loopback testing capability. Nine LEDs provide continuous indication of key EIA interface signals and modem status. Dial models are registered so that users can connect directly to switched telephone networks through standardized data jacks, without special access devices. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.
Circle 209 on Inquiry Card



Save engineering time and expense. Take advantage of Intermec's years of expertise. The Intermec Model 9200 is a completely designed bar code reader that's ready to integrate into your system. All the programming needed is on the card. Read the code of your choice; Code 39, Codabar, UPC or another popular bar code. The reliable RUBY WAND® Light Pen is included in the low, low price of under $400 in OEM quantities.

Features you'll get include bidirectional scanning, ASCII code transmission, and RS-232-C interface with dual connectors for operation with other devices. Parallel data interface boards and custom communications protocol are available or can be developed to meet your exact requirements.

For more information, write or call:
Interface Mechanisms, Inc.
P.O. Box N
Lynnwood, WA 98036
Phone (206) 743-7036

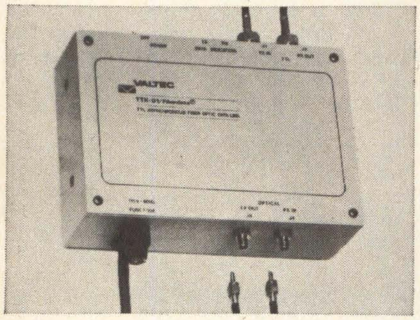
INTERMEC®

CIRCLE 65 ON INQUIRY CARD

OFFICE COMPUTER SOFTWARE/HARDWARE

Operating on System IV/90 processors with expanded memory, Multifunction Executive MFE/IV lets users independently perform data entry, COBOL processing, word processing, and interactive 3270 inquiry to an IBM 360/370 mainframe. Computer provides instant selectivity of any function up to 16 1920-char video displays. Software packages operate concurrently and independently under unit which allocates CPU and I/O resources to optimize system performance. Two added memory modules extend system capacity from 192k to 288k or 384k bytes. **Four-Phase Systems,** 10700 N DeAnza Blvd, Cupertino, CA 95014.
Circle 210 on Inquiry Card

FIBER-OPTIC, DUPLEX, LARGE BANDWIDTH LINK

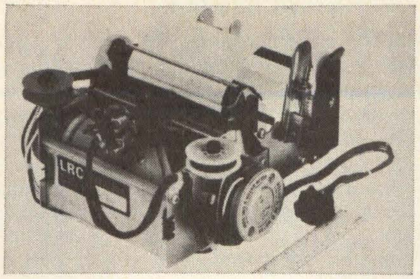


Fully engineered, asynchronous TTL data link has a self-contained optical transmitter, optical receiver, and power supply in each end. Electrical signal input and output is through std BNC connectors. Users need only plug the system into ordinary wall current and connect electrical and optical cables. Transmission capability from dc to 10M bytes/s over distances up to 3000 ft (1 km) is built-in. **Valtec Corp,** West Boylston, MA 01583.
Circle 211 on Inquiry Card

HIGH SPEED TABLETOP PUNCH

P 8075/A runs at 75 char/s. Sprocket-fed for positive tape advance, punch is designed to reduce slippage with Mylar tape, giving positive punching and retraction of punch pins on 5- through 8-level data on 0.875 or 0.6875" (4.76- or 1.746-cm) wide paper or Mylar tape, resulting in cleaner perforations and a tape that reads better with less chance of error. Parallel or RS-232 interface is provided. **Digitronics, Comtec Information Systems, Inc,** 53 John St, Cumberland, RI 02864.
Circle 212 on Inquiry Card

MATRIX IMPACT PRINTERS

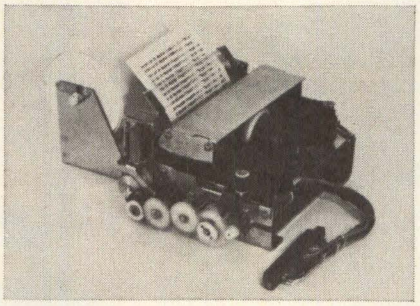


7000 series units use a drive cam for the printhead which results in uniform char width at extreme ends of print line as well as increased MTBF. Available in ticket printer as well as roll paper models, all units have multicopy capability with the print line capacity of 40 col (at 12 char/in). Ticket printer versions are available in 22-col models. 1- or 5-line document validation is optional on roll paper models. **LRC, Inc,** Technical Research Pk, Riverton, WY 82501.
Circle 213 on Inquiry Card

DOT MATRIX LIQUID CRYSTAL DISPLAY

An 8-digit 5 x 7 dot matrix, the SX147 has a 0.25" (0.64-cm) character height. Displays are 2.5" (6.4 cm) long and 0.8" (2.0 cm) high and can be stacked end-to-end or vertically to make larger displays. Power consumption is 16 μW typ. Other features include 20:1 contrast ratio, −10 to 80°C temp range, and 50,000-h expected life. Units are packed in DIPs and allow CMOS interfacing. **Crystaloid Electronics Co,** PO Box 628, Hudson, OH 44236.
Circle 214 on Inquiry Card

DOT MATRIX IMPACT JOURNAL PRINTER

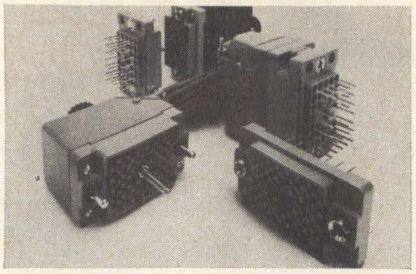


Model 512, a serial-entry dot matrix printer, prints 3 lines/s on 40-col lines. Heads are warranteed for 100M char continuous duty. Mechanism life is guaranteed for 5M print lines. The unit produces the 64-char ASCII set on 3.5" (8.8-cm) wide, friction-fed, fanfold or rolled paper, inked by ribbon or impact paper. Measuring 6 x 7 x 9.6" (15 x 18 x 24.4 cm), the unit is powered by a 24-Vdc motor and 35- to 40-V solenoid. **C Itoh Electronics, Inc,** 280 Park Ave, New York, NY 10017.
Circle 215 on Inquiry Card

CIRCLE 119 ON INQUIRY CARD →

PRODUCTS

HERMAPHRODITIC RACK AND PANEL CONNECTORS



Series 8027 2-piece I/O connectors use the company's Varicon™ hermaphroditic contacts in the same type insulators; they mate with themselves. Shrouded insulator design assures contact protection; center jackscrew assures fast mating, unmating, and locking. Series has 15-A rating with #14 to 16 AWG wire. Connectors include 30 contacts and withstand voltage of 2500 V rms at sea level. Applications cover electrical power distribution and control equipment, and power circuits of computer mainframes and peripherals. **Elco Corp, a Gulf + Western Manufacturing Co,** 2250 Park Place, El Segundo, CA 90245.
Circle 216 on Inquiry Card

MASS STORAGE OPERATING SYSTEM

MSOS II operating system for DG NOVA or NOVA emulating computers supports from 1 to 9 mass storage devices, high speed reader and punch, line printer, and system console in any combination. Unit is suited to applications program development and file management. System resident software occupies 350 words; overlays occupy an additional 1800 words during execution of system commands. Std system includes editor, relocatable assembler, linker, and extended BASIC. **Rela Systems, Inc,** 303 Canyon Blvd, Boulder, CO 80302.
Circle 217 on Inquiry Card

DISC CONTROLLER

Fully software and media compatible with DEC PDP-11, complete subsystems, including a selected disc drive or controller only with cable, are equivalent to the DEC RK05 disc system. When software compatibility is not required, the model 14XX controller will interface up to 4, 10M-byte dual-disc drives, either 5440 or 2315 system (40M bytes total online storage). Controller is supplied with a system unit suitable for installation in the PDP-11 computer chassis. **Rianda Electronics, Ltd,** 2535 Via Palma, Anaheim, CA 92801.
Circle 218 on Inquiry Card

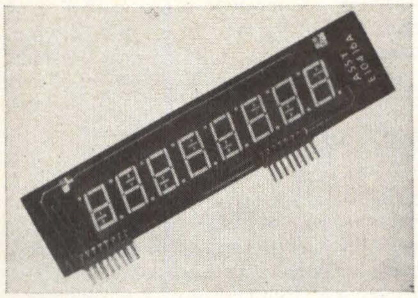
PDP-11 BUSINESS SOFTWARE COMPILER

Developed as a feature of the DIBEX operating system, compiler enables users to program in, or to utilize existing DIBOL™ routines. Compiling and editing can be carried out at any or all terminals while the user continues to run his business applications on 3, 4, or more other terminals. Operating system and compiler are fully compatible with DEC documentation and programs written in DIBOL. **Information Access Systems, Inc,** 1140 Bloomfield Ave, West Caldwell, NJ 07006.
Circle 219 on Inquiry Card

I/O PROCESSING BOARD

General-purpose board APU100 with onboard 8080 processor provides a high performance interface to std S-100 bus. Unit operates asynchronously with the computer system's CPU, transfers information in full DMA, and uses bus system clock to provide internal timing for system synchronization. All 8192 bytes of dynamic RAM storage operating at 300-ns access time are used for file management I/O programs and buffering; 1024 bytes of 2708-type EPROM storage are used for device initialization routines. **Extensys Corp,** 380 Bernardo Ave, Mountain View, CA 94040.
Circle 220 on Inquiry Card

8-DIGIT LED DISPLAY MODULE

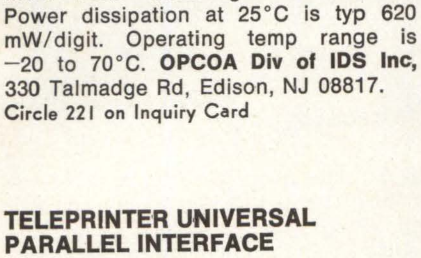


An 8-digit, with right-hand decimal point, red LED display, 600 series features a 0.6" (14-mm) high char. Designed for common-cathode multiplex configuration at low power consumption levels, unit is suitable for battery operation and portable applications. Typ operating conditions are 20 mA peak for a luminous intensity of 0.250 mcd. Peak wavelength is 630 nm. Power dissipation at 25°C is typ 620 mW/digit. Operating temp range is −20 to 70°C. **OPCOA Div of IDS Inc,** 330 Talmadge Rd, Edison, NJ 08817.
Circle 221 on Inquiry Card

TELEPRINTER UNIVERSAL PARALLEL INTERFACE

Model 40 interface generates a universal handshake routine, permitting line printers having similar operations specs to be replaced with the Teletype[R] model 40. Capable of using a buffered serial interface, device permits a serial data flow in TTL, EIA, or 20-mA current loop modes, and use of the line printer as a remote peripheral receive only unit. Printer motor is either manually or automatically controlled. **Tel-Tex, Inc,** 3203 Audley St, Houston, TX 77098.
Circle 222 on Inquiry Card

DIRECT-CONNECT AUTO ANSWER MODEM

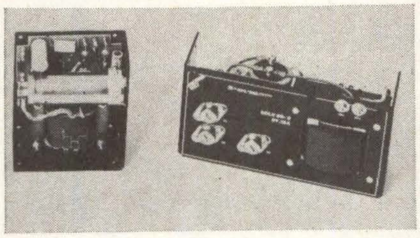


A half/full-duplex, Bell compatible modem for automatic answering of a computer callup interfaces to 2-wire dial network through 97A or 97B jack; DAA is not required. P-113D is connected to the switched network in programmable, fixed loss, or permissive modes. Specs include a 0- to 300-bit/s serial binary asynchronous data format; −3- to −12-dBm transmit levels; −48-dBm receiver sensitivity; and FSK modulation. Mark and space frequencies are 2225 and 2025 Hz ±1%. **Prentice Corp,** 795 San Antonio Rd, Palo Alto, CA 94303.
Circle 223 on Inquiry Card

CASSETTE CLEANER

Model 100 allows for easy Phillips' style cassette maintenance by using a long lasting blade which removes partially imbedded or surface particles of foreign contamination. Cleaner also uses a cleaning/conditioning solution and pad which remove oils and submicron size particles from tape surface and also condition tape for error-free operation. Unit measures 10 x 8 x 5" (25.4 x 20.3 x 12.7 cm) and weighs <10 lb (4.5 kg). **Innovative Computer Products,** 18360 Oxnard St, Tarzana, CA 91356.
Circle 224 on Inquiry Card

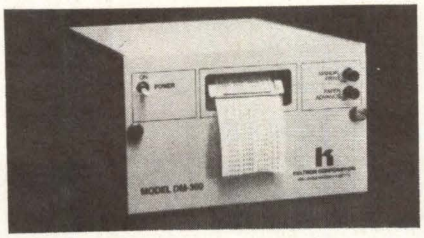
OPEN FRAME, LOW VOLTAGE POWER SUPPLIES



Series of std power supplies includes 15-, 30-, and 60-output units, all UL recognized per 478. SOLV 15 is equipped with overvoltage protection circuit, which is optional on the 30 and 60 units. Availability factor ranges from 5 V, 12 A to 48 V, 2 A. Features include isolated outputs for positive or negative protection; full rated output from 0 to 55°C, precision IC regulation, remote sensing programming, and foldback current limiting. **Elpac Power Systems,** 3131 S Standard Ave, Santa Ana, CA 92705.
Circle 225 on Inquiry Card

18-COL SERIAL INPUT PRINTER

DM300 series input is available in serial form at TTL levels in BCD code. An internal shift register is provided, and input is stepped through the register on receipt of a clock or strobe signal. Column blanking is easily done for mating purposes. The units provide 3 lines/s, up to 18 col. Print drums come with 13 positions/col and can print 40 different char and numbers. Print motor drum operates either continuously or on demand. Timing circuits are built-in. **Keltron Corp,** 225 Crescent St, Waltham, MA 02154.

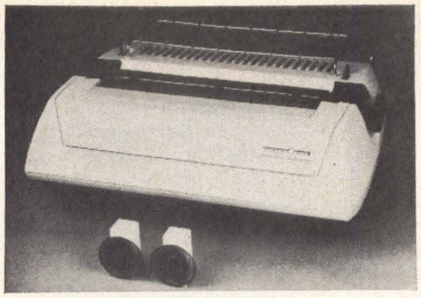


Circle 226 on Inquiry Card

CIRCLE 123 ON INQUIRY CARD →

PRODUCTS

DAISY WHEEL PRINTER



A letter-quality unit designed for use with microcomputer systems, printer operates under control of an internal microprocessor and communicates with host microprocessor over a high speed asynchronous parallel interface, printing bidirectionally at 45 char/s. Carriage can be positioned left or right in increments of 0.008" (0.211 mm) and platen can be rolled forward and backward in steps of 0.021" (0.529 mm). 28 type styles are available on plastic and metal wheels. **Algorithmics Inc,** Box 56, Newton Upper Falls, MA 02164.
Circle 227 on Inquiry Card

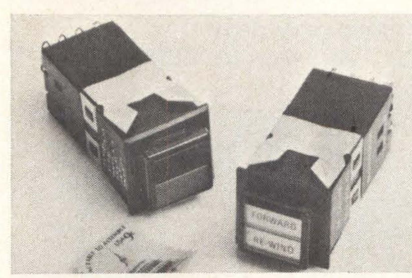
ASYNCHRONOUS LINE DRIVER

The "zero downtime" limited distance ALD is comprised of a single unit housing two asynchronous line drivers. One driver remains in a ready state as an onsite backup unit while the other is in operation. Conforming to Bell spec 43401 and using an EIA RS-232-C or 20-mA interface, 4 standalone or rack-mounted units feature 0- to 9600-bit/s asynchronous transmission, 2-wire half duplex or 4-wire full duplex, point-to-point or multidrop, and LED performance indicators. **Ven-Tel, Inc,** 2360 Walsh Ave, Santa Clara, CA 95050.
Circle 228 on Inquiry Card

PROGRAMMABLE PULSE GENERATOR

Model 1012 features complete programmability through 3 rear panel connectors. Programming can be done by providing a ground closure or an open circuit in a std 8-4-2-1 BCD format. Repetition rate is from dc to 20 MHz, pulse width can be varied from <40 ns to 9.99 ms, and amplitude range is from 0 to ±14.8 V depending on options selected. Units are available for rack mounting or as cabinet enclosed units. **Velonix, div of Varian,** 560 Robert Ave, Santa Clara, CA 95050.
Circle 229 on Inquiry Card

SPLIT-SCREEN ILLUMINATED PUSHBUTTON SWITCHES



All electrical and mechanical options of the company's 554 series are offered by the 330 and 331 series, which have the same mounting and back of panel dimensions. They use two incandescent lamps and provide a horizontally (330) or vertically (331) split display to maximize display and legend information. The T-1¾ lamps, available for from 5 to 28 V, can be energized together or by separate circuits. Models are available for panel or snap-in bezel mounting. **Dialight, a North American Philips co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 230 on Inquiry Card

MEMORY BOARD/ SYSTEM TESTER

Optimized for dynamic testing of memory boards and complete memory systems, unit tests semiconductor, core, plated wire, and bubble memories. The 10-MHz system features a variety of user-oriented software packages for performing automatic shmoo plotting, datalogging, and statistical analysis. Hardware includes a programmable split-cycle clock generator with up to 32 independently programmable edges. **Macrodata Corp, a Cutler-Hammer Co,** 21135 Erwin St, PO Box 1900, Woodland Hills, CA 91365.
Circle 231 on Inquiry Card

AC POWER CONDITIONER

Voltector series 5 provides both common and transverse mode protection against rf noise and destructive surges, spikes, and transients that enter a building on the primary power line. The unit is equipped with a green pilot light to indicate "ready." It limits 2500-V spikes to safe levels. Internally fused, the device is rated 5, 10, 15, and 20 A at 120 V, from 50 to 400 Hz. **Pilgrim Electric Co,** 29 Cain Dr, Plainview, NY 11803.
Circle 232 on Inquiry Card

MAGNETIC TAPE CLEANER

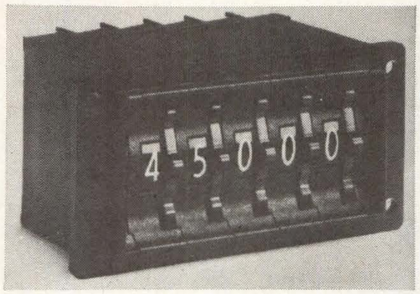
Dual 200 features double cleaning efficiency by incorporating 2 patented self-sharpening cleaning blades in 1 machine, providing 4 separate cleaning phases during each cycle. Cleaner also offers LED footage counter to record exact footage between EOT and BOT markers, simplified solid-state electronics design ensuring reliable continuous operation, straight-line tape loading path for efficient operation, and heavy-duty construction. **Data Devices International,** 6301 DeSoto Ave, Woodland Hills, CA 91367.

Circle 233 on Inquiry Card

ADC POWER SUPPLIES

Offered for PC or chassis mounting, packages have all voltages required for powering A-D converter modules in 1 miniature supply. They provide ±15 or ±12 V at 100 mA and 5 V at 500 mA. Specs include operating temp from −25 to 71°C and line voltages of 100, 115, or 220 Vac at 50 to 400 Hz. Size of supplies is 1.25 x 2.5 x 3.5" (3.175 x 6.4 x 8.9 cm); units weigh 18 oz (0.5 kg). **Calex Mfg Co, Inc,** 3305 Vincent Rd, Pleasant Hill, CA 94523.
Circle 234 on Inquiry Card

THUMBWHEEL SWITCHES WITH LED LIGHTING



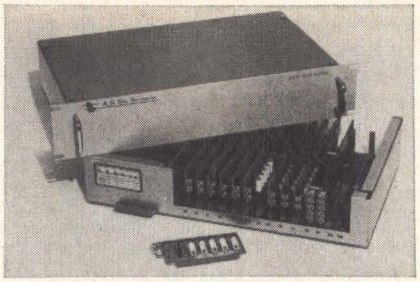
Available with direct solder or optional PC mount terminations, digital miniswitches feature snap-together assembly. Rearmounted 43000 series is interchangeable with most 0.500" (12.7-mm) switches; 44000 (frontmounted) and 45000 (rearmounted) are interchangeable with 0.315" (8-mm) switches. All have 10 std dial positions and an operating life of >1M detent operations at 25°C. Available in red or clear lighting, LED lights only the number on the dial. **The Digitran Co, div of Becton, Dickinson and Co,** 855 S Arroyo Pkwy, Pasadena, CA 91105.
Circle 235 on Inquiry Card

6-DIGIT SYNCHRO ANGLE INDICATOR

Converting synchro or resolver signals to BCD and displaying them with 5 digits to an accuracy of ±0.03 deg or with 6 digits to ±0.005 deg, the SR-103 automatically adjusts to signal voltage levels of 10 to 100 V and reference levels of 10 to 150 V without switching. Carrier frequency range is broadband 47 to 1000 Hz and signal-to-reference phase shift can be as much as ±50 deg. The half-rack wide instrument can be programmed by logic levels applied to the rear connector. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
Circle 236 on Inquiry Card

CIRCLE 125 ON INQUIRY CARD →

PRODUCTS



SWITCHING MATRIX WITH IEEE-488 INTERFACE

Capable of switching stimuli and measuring instruments to units under test from any IEEE-488 controller, series 56A matrices are designed with a mainframe and plug-in modules. Mainframe has all necessary logic to interface directly with any 16-bit I/O bus. Different modules allow signals including high frequency, low level, or high current to be switched. Each module has 20 crosspoints so that systems from 20 to 10,000 crosspoints can be formed. **A D Data Systems, Inc,** 200 Commerce Dr, Rochester, NY 14623.

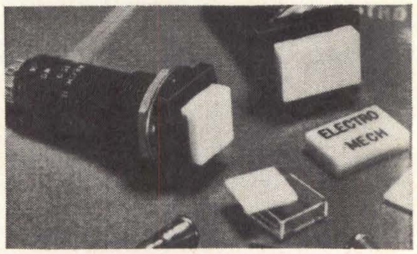
Circle 237 on Inquiry Card

VARIABLE CONSTANT CURRENT POWER SUPPLIES

AV-100 is a line-powered (110 V, 60 Hz), short-circuit proof, metered (output current) unit that provides a variable constant current output in the range of 10 to 50 mA to a load voltage in the range of 0 to 100 V. -101 is identical except that it requires a 15 Vdc input. -102 is a miniaturized version requiring a 115-Vdc input. **Avtech Electrosystems, Ltd,** PO Box 11426 Sta H, Ottawa, Ontario, K2H 7V1 Canada.

Circle 238 on Inquiry Card

LOW PROFILE PUSHBUTTON SWITCH

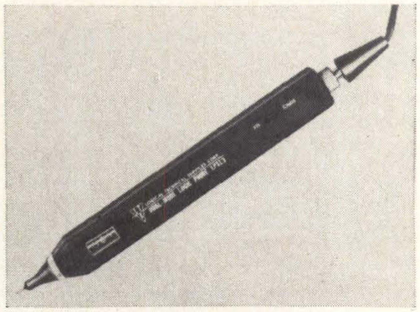


Lighted switches are available in 0.5" (1.27 cm) square or 0.5 x 0.75" (1.27 x 1.91 cm) rectangular sizes, with mounting design. Series 20 miniature models are packaged in unitized housing, combining 0.625" (1.588-cm) dia round switch body with square or rectangular bezel and interchangeable filter/lens. High performance internal circuitry, low bounce, and 21 std multiple-switching functions (spst-dpst) are provided in 30/115-Vac, 2-A resistive, 1-A inductive models. **Electro-Mech Components, Inc,** 1826 N Floradale Ave, South El Monte, CA 91733.

Circle 239 on Inquiry Card

DUAL MODE LOGIC PROBES

LP313 offers 2-MΩ, 12.5-pF input impedance and has a 5-ns, 200-MHz response, making it ideal for use with microprocessors. A 3-color LED display and compact packaging make this TTL/CMOS probe easier to use with hard-to-reach chips. Pulses are stretched to 100 ms and displayed by a transition LED, or may be latched-on using memory. Signal input overload protection is ±100 Vdc or 115 Vac continuous, 250 Vdc or ac for 30 s. **Logical Technical Services,** 71 W 23rd St, New York, NY 10010.



Circle 240 on Inquiry Card

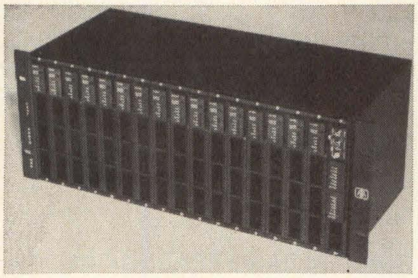
HARDWARE PRINTER SWITCH

Users of the company's System I and II word processing equipment can maintain system throughput while reducing costs with a printer switch that allows 2 typists to share 1 printer. System efficiency is improved when another typing station is linked to the same underutilized, output printer. The electronic switch and all required cabling typically link 30-, 40-, and 55-char/s daisywheel printers. **NBI Inc,** 5595 E Arapahoe Ave, Boulder, CO 80303.
Circle 241 on Inquiry Card

FIBER-OPTICS DESIGNERS KIT

Containing an assortment of emitter and detector, splice, and polishing bushings; several sizes of connector ferrules; polishing plate; hand tool for terminating optic cable; and sample lengths of cable, kit accommodates most common sizes and types of fiber optic cables, emitters, and detectors. Enough components are included to house 25 emitters or detectors, make 5 free-hanging and 5 bulkhead mounted splices, and terminate 20 fiber-optic cables. **AMP Inc,** Harrisburg, PA 17105.
Circle 242 on Inquiry Card

STATUS/ALARM SYSTEMS



Combining RS-232/V.24 jack sets and status and alarm displays in one assembly, DPS-3-1 and -2 data patch status/alarm systems consist of 16 channel modules including a power supply module. Each module accommodates the full EIA RS-232/V.24, 25-conductor interface. Major control leads (RTS, CTS, TD, RLSD, and RD) are monitored with indicator LEDs. One may also be connected to an alarm. Power module status is displayed on an additional lead. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 243 on Inquiry Card

HIGH DENSITY CARTRIDGE DRIVE

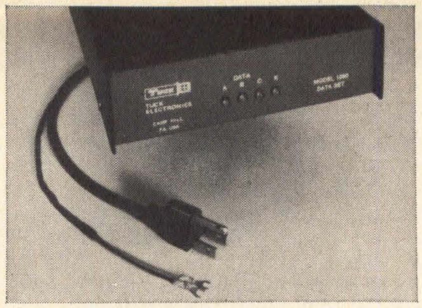
Designed to load and unload fixed discs, the "Funnel" cartridge tape drive offers a cost-effective approach to removable media to back up fixed discs. Featuring 4-track serial recording, the device utilizes a 300-ft (91-m) cartridge, recording at 6400 bits/in (2520/cm) in MFM or other high density code for a 11.5M-byte capacity. Data transfer rate is 192k bits/s. Four units can provide over 46M bytes of online storage in a 7" (17.8-cm) panel. **Data Electronics, Inc,** 370 N Halstead St, Pasadena, CA 91107.
Circle 244 on Inquiry Card

HIGH RESOLUTION GRAPHICS BOARD

Fully compatible with any S-100 bus computer, board operates in one of two modes: digital output or 16-level gray scale. It requires 8 Vdc and a min of 8k RAM and will produce digital graphic displays of 256 x 240 screen elements or 128 x 120 gray scale elements. Video output conforms to RS-170 and will interface to std raster scan monitors. Memory remains available for general use when not being used for graphic display. **Vector Graphic Inc,** 790 Hampshire Rd, Westlake Village, CA 91361.
Circle 245 on Inquiry Card

DATA TRANSMITTER

Replacing Bell Telephone's 401A/E, the 1880, used in manual call originating mode only, serves as the link between the IBM 1001A data transmission system and IBM 24/26 card punch. Retaining all electrical characteristics of the Bell units, the transmitter operates on commercial power. Housed in a tabletop unit, the device measures



2 x 12 x 6" (5 x 30.5 x 15 cm). **Tuck Electronics,** 4409 Carlisle Pike, Camp Hill, PA 17011.
Circle 246 on Inquiry Card

SUCCESSIVE APPROXIMATION A-D CONVERTER

ADC593-12 operates in 3.5-μs (typ) and 4.0-μs (max) conversion time, and provides an accuracy of $\pm$0.0125% in digitizing analog signals. A 250-kHz throughput rate is guaranteed. Four selectable input ranges and three digital output codes provide versatility. Gain tempco is $\pm$30 ppm/°C. Differential linearity of $\pm$½ LSB is monotonic over the 0 to 70°C temp range. The unit is complete with a precision thin-film D-A converter, clock, comparator, reference, and successive approximation register. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.
Circle 247 on Inquiry Card

COOLING FAN

Muffin® XL fan moves approximately 10% more cooling air at free delivery and works against roughly 50% higher static pressures, yet offers the same reliability as other models in the line. Designed for electronic applications including mini and microcomputers, fan operates at noise levels as low as NC-45 while producing up to 115 ft^3/min (54.3 L/s) at free delivery. Unit measures 4.69" (119.1 mm) sq and 1.53" (38.9 mm) deep. **Rotron Inc, Commercial Div,** Woodstock, NY 12498.
Circle 248 on Inquiry Card

38.4G-BIT DISC SUBSYSTEMS

Incorporating 819-11 and -21 disc storage units and model 7639-21 and -22 single and dual access controllers, subsystems are designed for use with Cyber 176, Cyber 76, and 7600 systems. A fixed media device that records at 6000 bits/in on 40 disc surfaces, the -21 stores 4.8G data bits. -11, a 2.4G bit version can be upgraded in the field to a -21. Both subsystems transfer data between drive units and host computer at a rate of 37.2M bits/s. **Control Data Corp,** Box O, Minneapolis, MN 55440.
Circle 249 on Inquiry Card

SOLDERLESS BREADBOARD

EXP4B quad bus strip provides 4 rows of interconnected tiepoints, 40 tiepoints/row. Molded with tongue-and-groove sides, multiple strips can be assembled into larger arrays. Buses are provided for signal, power, and bias lines. Measuring 0.375 x 6 x 1" (0.95 x 15.2 x 2.5 cm), the strip has a vinyl insulated back which permits mounting anywhere without danger of shorting. Molded-in mounting holes facilitate permanent or semipermanent mounting to flat surfaces. **Continental Specialties Corp,** 44 Kendall St, PO Box 1942, New Haven, CT 06509.
Circle 250 on Inquiry Card

EXTENDED MEMORY CASSETTES

Containing 450 ft (137 m) of tape instead of 300 ft (91 m) and requiring no changes to cassette machine or system, cassette provides 50% greater capacity. A thinner Mylar tape with a special carbon coating assures recording accuracy. Tape has proved to have the same tensile strength as standard tape in tests which included a life test of more than 10,000 passes. **Magnetic Information Systems,** 415 Howe Ave, Shelton, CT 06484.
Circle 251 on Inquiry Card

MULTIPLE OUTPUT SWITCHING REGULATOR

DS series fully regulated dual, triple, and quad outputs total 800 W, and can range from 2 to 24 V and up to 80 A. A typical digital requirement of 5 V at 80 A, −5 V at 60 A, and 12 V at 5 A can be provided while still maintaining protection from overtemperature, overvoltage, overcurrent, and brownout conditions. Conservative power ratings are available at 50°C and in any mounting plane. All outputs remain within regulation at full load for one cycle after removal of nominal ac power. **Switching Power, Inc,** 19 Daell Lane, Centereach, NY 11720.
Circle 252 on Inquiry Card

REQUEST-TO-SEND SIGNAL EMULATOR

Switched network operation up to 4800 bits/s is possible with emulator which provides the necessary HDX interface protocol for passive terminals and computer ports. No secondary channel or modem slaving technique is needed. Normal operating procedures are maintained since there is no loss of data during RTS-CTS delay. The unit can interface with synchronous as well as asynchronous modems, and permits computer frontend to use a single dial-up connection to less active terminals. **Com/Tech Systems Inc,** 44 Beaver St, New York, NY 10004.
Circle 253 on Inquiry Card

16-PORT SERIAL I/O BOARD

With from 2 to 16 serial ports, the CA10-X features RS-232 and high speed synchronous interfaces which can be mixed in any combination. Communications transfer rate of each serial port is jumper-selectable from a crystal control clock circuit which will support operations from 75 to 19,200 baud asynchronous or 250k to 500k bits synchronous. All 16 ports can be jumpered to be continuously addressable memory or to be paged at the same address. **Ohio Scientific,** 1333 S Chillicothe Rd, Aurora, OH 44202.
Circle 254 on Inquiry Card

SHIELDED AND UNSHIELDED CABLE

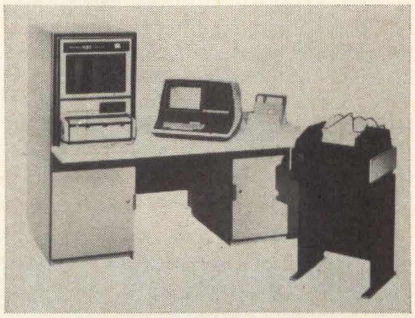
Featuring a stranded tinned copper conductor with 0.010" (0.254-mm) color-coded 105°C PVC insulation manufactured to MIL-W-16878 D Type B, and UL Style 1061, unshielded cable is available either single or paired in AWG sizes 20, 22, 24, and has a gray vinyl jacket overall. Shielded cable has all these features plus a braided tinned copper shield. All items are UL listed under styles 2343 and 2344 for computer usage and are rated at 80°C, 300 V. **Columbia Electronic Cables,** 11 Cove St, New Bedford, MA 02744.
Circle 255 on Inquiry Card

SINGLE/MULTISTRIKE PRINTER RIBBONS

Multistrike ribbon, designed to reduce ribbon costs in high volume print environments, advances ⅓ char/strike. Each cloth ribbon is saturated with high density black ink which provides clear char impressions; total capacity is 200k char. Single-strike carbon ribbon offers crisp, high-density print quality which is resistant to chemicals used in offset reproduction. Char capacity is 46k. Both are added to the line of HyType II daisywheel printer supplies. **Diablo Systems, a Xerox Co,** 24500 Industrial Blvd, Hayward, CA 94545.
Circle 256 on Inquiry Card

PRODUCTS

AUTOMATIC LOGIC BOARD TESTER



Model 3700 offers automatic and processor-controlled pattern generation, up to 256 3-state bidirectional pins, programmable dual drive level and receiver threshold settings to ±20 V, and MHz pin execution rates under DMA control with optional 4k-pin memory. Hardware features a Z80 microprocessor, floppy disc storage up to 1.2M bytes, 24-line CRT with keyboard, and 32k RAM. Software includes interactive test program development and support programs. **Systron-Donner Corp, Data Products Div,** 935 Detroit Ave, Concord, CA 94518.
Circle 257 on Inquiry Card

DC MOTOR

MB200 provides 0.1 hp and is especially suited for computer tape drives, laboratory instruments, and industrial process equipment. Design features include diamond-finished commutators made of hard drawn copper alloys, ceramic permanent magnets, and long life easily replaceable brushes. Motor brushes made of copper graphite offer a min of 5000 h of operation at 1000 r/min. Typ specs include 30-Vdc input with a speed of 5500 rpm at 20 oz-in (0.14 N•m) continuous rated torque. **Dynetic Systems, Inc,** 19128 Industrial Blvd, Elk River, MN 55330.
Circle 258 on Inquiry Card

ELECTROSTATIC PRINTER/PLOTTER

Capable of producing C- and D-size drawings, the 5300 plots with a resolution of 5 mils (0.005" or 0.127 mm) both horizontally and vertically at paper speeds of up to 0.72 in/s (183 mm/s) on 22" (56-cm) wide paper. Online DMA interfaces are available for PDP-11, HP 2100 and 21MX, Nova and SuperNova, Eclipse, and IBM 360/370 computers. Offline operation is possible with IBM 360/370, Univac 1100 series, and CDC 6000, 7000, and Cyber series systems. **Gould Inc, Instruments Div,** 3631 Perkins Ave, Cleveland, OH 44114.
Circle 259 on Inquiry Card

PRINTER TERMINAL UPGRADE BOARD

Designed to replace existing digital electronics in the DECwriter II teleprinter, the SuperDEC throughput optimizer installs in minutes, upgrading the terminals to 1200-baud operation. It also provides features which were either optional or not available on the std LA36 teleprinter. These include bidirectional printing, double-wide char set, full forms control, RS-232-C interface, and 32 user-programmable chars. **Intertec Data Systems Corp,** 1851 Interstate 85 S, Charlotte, NC 28208.
Circle 260 on Inquiry Card

HIGH DENSITY WIREWRAP PANEL

Designed for high density packaging of DIPs, 323 series panels accommodate 60 ICs and measure 8.375 x 4.50" (21.273 x 11.43 cm). 324 series handles 108 ICs and measures 8.375 x 9.700" (21.273 x 24.638 cm), and 326 accommodates up to 200 ICs and measures 8.900 x 13.300" (22.606 x 33.782 cm). All can be intermixed in one rack assembly to provide logical subdivision of functions. Interpin ground plane provisions of IC socket patterns insures high speed operation and high noise immunity. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 261 on Inquiry Card

LSI DATA SET

Offering complete compatibility with the Bell 212A and with all Bell and Rixon 100-series data sets (103, 113), the T212A provides full-duplex serial data communications over the 2-wire DDD switched network at either 0 to 300 bits/s asynchronous or 1200 bits/s synchronous or char asynchronous. Originating speed selection is made via a front panel switch, or the terminal interface. At the answering station, the device automatically adjusts to the speed of the originating station data set. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.
Circle 262 on Inquiry Card

SUPER BRIGHT LEDS

Variable terminal spacing is possible with UB181 series LEDs which replace unbased incandescents. This allows for LED placement on PC boards where holes are up to 0.625" (1.588 cm) apart. Drive current is 20 mA. They put out typically 50 (red), 35 (amber), and 24 mcd (green), with clear tinted encapsulation. Operation is either pulsed or continuous for at least 10 yr at 20 mA. LEDs are available with built-in resistors for voltages from 2.4 to 28 Vdc. **Data Display Products,** 303 N Oak St, Inglewood, CA 90301.
Circle 266 on Inquiry Card

PDP-11 COMPATIBLE 32-WORD ROM

ROM11-32 contains 32 16-bit words and is functionally equivalent to the DEC M792 p/ROM. Configured around two fusible link 32-word by 8-bit type 8223 p/ROMs, memory system is mounted on a quad board that plugs directly into one DD11 small peripheral controller slot in the CPU, and operates from existing 5-V power supply. Access time is 100 ns. A combination of units (up to 8 max) can be used. **Computer Extension Systems, Inc,** 17311 El Camino Real, Houston, TX 77058.
Circle 267 on Inquiry Card

GRAPHIC DATA TERMINAL

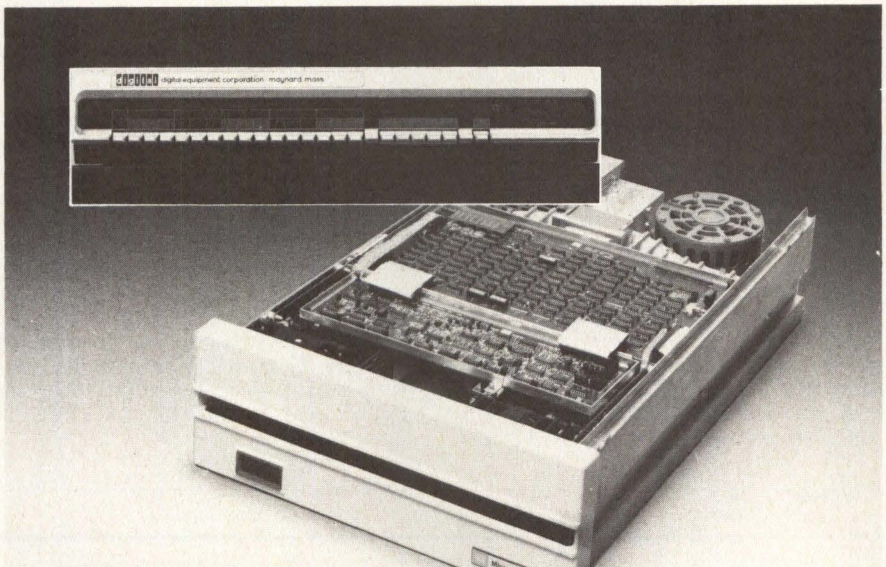
Intecolor 8001G, a 48-line x 80-char/line display system has a complete graphics package (160 x 192 grid area), 19" (48-cm) screen with 8-color foreground and background, a set of 64 ISA char, all editing functions, and an industrial type keyboard with cursor control and color cluster. Baud rate is selectable to 9600; RS-232-C connection is provided. Graphic software allows users to plot bar graphs in both horizontal and vertical directions, and to plot lines, points, and vectors. **Intelligent Systems Corp,** 5965 Peachtree Corners E, Norcross, GA 30071.
Circle 263 on Inquiry Card

MINIATURE EXTENDED RANGE POLYESTER CAPACITORS

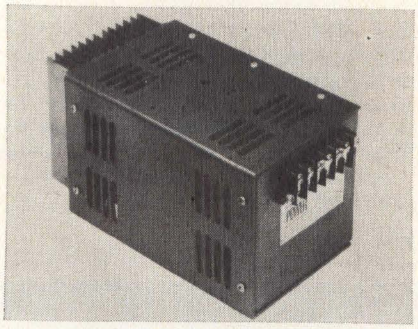
SMMKO metallized-polyester capacitors intended for PC board or hand wiring, have radial leads at 0.3" (7.5-mm) std DIP spacing. Solvent resistant molded case is SE-0 flame rated. Capacitance ratings range from 0.001 to 0.1 mF with 10% and 20% tolerances std. Working voltages are 100 Vdc and 63 Vac. Devices have a low loss factor, op temp range of −40 to 100°C, and excellent mechanical integrity. **Seacor Inc,** 598 Broadway, Norwood, NJ 07648.
Circle 264 on Inquiry Card

COMPACT CRT TERMINAL

TTY compatible model 400E, using the company's Smart Monitor, is the size of a std 15" (38-cm) monitor, measuring 15 x 14 x 13.6" (38 x 35.5 x 34.5 cm) plus keyboard. 2000-char memory is std. Display format is 24 lines x 80 char with an additional line of memory that can be accessed in roll or scroll mode. 72-key detachable keyboard generates the full 128-char ASCII set, and has a separate numeric pad and individual cursor control keys. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.
Circle 265 on Inquiry Card



COVERED DC POWER SUPPLIES

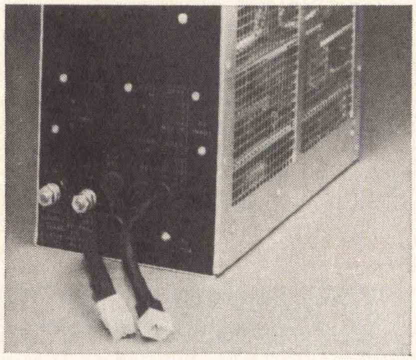


Designed for computers, microprocessors, and industrial applications, CPS series has anodized aluminum covers. Features include terminal strip connection, and voltage and current limit adjustment. Specs are 115/230 Vac input, with 47- to 440-Hz frequency. Line and load regulations are ±0.1% with 0.1% typ ripple. Units have foldback type current limiting for short-circuit protection, and response time of 50 ms. Available in 29 models from 30 to 500 W, supplies cover 5- to 48-V range. **Standard Power, Inc**, 1400 S Village Way, Santa Ana, CA 92705.

Circle 268 on Inquiry Card

MULTIPLE OUTPUT SWITCHING POWER SUPPLY

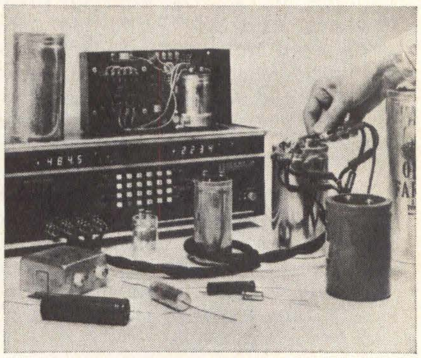
Model 8D436 ac-dc switcher provides ±10% adjustable output voltages of 5, 12, and −5 Vdc at rated currents of



50, 10, and 1 A, respectively. All outputs may be loaded from 0 to 100% of rated current. The device accepts 93 to 126 Vac for 115-Vac inputs, or 176 to 253 Vac for 230-Vac inputs. Regulation band limits provide outputs within ±1.5% of the voltage setting when subjected to input voltage and line frequency variations, temp range of from 0 to 55°C, and static load current variations. **Powertec, Inc**, 9168 DeSoto Ave, Chatsworth, CA 91311.

Circle 269 on Inquiry Card

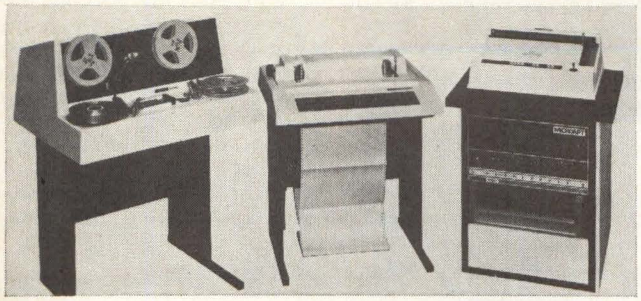
uP-CONTROLLED LRC METER



Model 296, with either 10- or 20-kHz test frequency combined with 120 Hz or 1 kHz, helps test for low equivalent series resistance (ESR) at operating frequency. Meter is controlled by programmable calculator or special program to provide simultaneous display of 2 different frequency measurements. Usable as benchtop tester or for sorting when interfaced with high speed automatic parts handler, wide range meter tests ESR over a range of 0.01 MΩ to 1.0 MΩ. Capacitance measurements to 2 F are possible at the 120-Hz test frequency. **Electro Scientific Industries, Inc**, 13900 NW Science Park Dr, Portland, OR 97229.

Circle 270 on Inquiry Card

COMPUTER-BASED NC PART PROGRAMMING SYSTEM



MICROAPT[c] is a minicomputer-based hardware/software system with 30-char/s keyboard impact/printer. Functioning within the user's own facility, it features a modular design with 3- to 5-axis expandability to increase machine tool efficiency and reduce time and cost of programming and tape preparation. Error checks, diagnostics, and edit features are performed. The system supports FORTRAN IV, BASIC, and ALGOL, and includes floating-point hardware; it operates with the user's FORTRAN IV APT postprocessors or those from the company's library. System controller is the company's DPS-4000 tape preparation center; processor unit is a Data General Eclipse minicomputer with floating point hardware and 96k-byte memory. **LeBlond NC Systems,** 6761 Bramble Ave, Cincinnati, OH 45227.
Circle 271 on Inquiry Card

60- TO 600-BAUD ACTIVE MODEM FILTERS

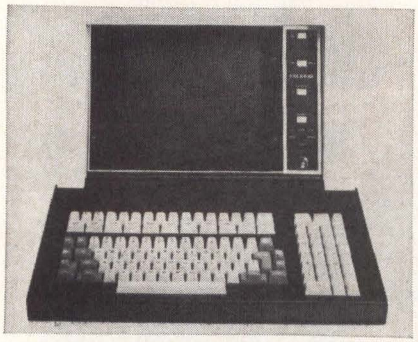
Family of fixed frequency, precisely defined bandpath filters have identical pinouts and packages. They operate from a single-ended 10- to 30-Vdc power supply. At filter center frequency, the 534 series has inverting midband gain of 0 ±0.5 dB. Fixed center frequencies are between 365 to 965, 1075 to 1875, and 2000 to 3600 Hz in 100-Hz increments for 35 std CCITT 60-baud models; between 420 and 3660 Hz in 120-Hz increments for 28 75-baud models; between 425 and 3655 Hz in 170-Hz increments for 20 110-baud units; between 480 and 3600 Hz in 240-Hz increments for 14 150-baud models; between 915 and 3315 Hz in 600-Hz increments for 5 300-baud models; and at 1815 Hz for 600-baud unit. Space and mark frequencies above and below selected center frequency are 25, 30, 42.5, 60, 120, and 240 Hz, respectively. **Frequency Devices, Inc,** 25 Locust St, Haverhill, MA 01830.
Circle 272 on Inquiry Card

ASYNCHRONOUS DATA DISPLAY TERMINALS

For use in small business systems, computer timesharing, and with mini/microcomputers, VC404/Standard terminal features a detachable u/lc keyboard, 1920-char display, data rates to 19.2k baud, cursor addressing, RS-170 composite video output, and transparent/tape mode switch to allow display of all 128 ASCII char. VC414/Editor display terminal is microprocessor-based and offers added features of char-by-char, line, or page mode transmission; line/char insert and delete; editing; horizontal tabs; format mode; protected data fields; multilevel video display; and line drawing capability. In addition, the VC424/Termulator adds polling capability and independent printer port. **Volker-Craig Ltd,** 266 Marsland Dr, Waterloo, Ontario N2J 3Z9, Canada.
Circle 273 on Inquiry Card

PRODUCTS

CRT TERMINAL



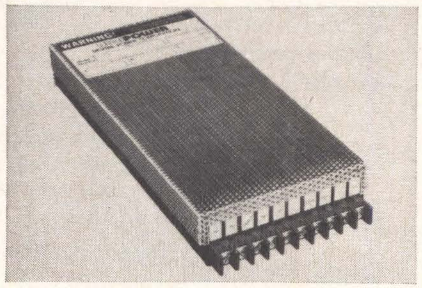
Model 4041B has Burroughs TD-830 std protocol, polling, and line discipline compatibility, and functions with std Burroughs network software with no modifications. Features include 2 pages of buffer (3840 char), 1920-char display, 103/113/202 modem interfaces, full edit typewriter-style keyboard, u/lc, 15 function keys, and forms (protected data). Nonpolling point-to-point and char mode operations are std switch-selectable for multipurpose applications. **Teleray, Div of Research Inc,** Box 24064, Minneapolis, MN 55424.
Circle 274 on Inquiry Card

2.5k-VA POWER INVERTER

Pulse width modulated high efficiency systems delivering 90% at full load and better than 85% at half load, Taurus™ series inverters form the basic building block for 2.5k-VA frequency changers and uninterruptible power systems. Std features include under- and overvoltage protection, phase and frequency synchronization, slow turn-on, and an input circuit breaker. Typ specs include input voltage of 22 to 32 Vdc, 42 to 54 Vdc, and 105 to 150 Vdc; and output of 115 Vac or 230 Vac. **Nova Electric Manufacturing Co,** 263 Hillside Ave, Nutley, NJ 07110.
Circle 275 on Inquiry Card

SWITCHING POWER SUPPLIES

Designed for small computers and products utilizing nonvolatile memories, DS151 series features power fail signal



which warns computer of a loss in primary ac power if a half-cycle failure occurs. This provides for storing program in nonvolatile memory, while energy flow continues during the transfer period (ms). Models are available in 5 V at 30 A, 12 V at 12 A, or 15 V at 10 A. Short-circuit and overvoltage-protected units operate within input voltage range of 100 to 130 Vac at a typ efficiency of 75%. **Digital Power Corp,** 2060 The Alameda, San Jose, CA 95126.
Circle 276 on Inquiry Card

IEEE-488 DATA BUS CABLES

Featuring molded-on stackable 24-contact male/female connectors, the 24-conductor general-purpose interface bus (GPIB) performs general interface management using 8 conductors, data byte transfer control using 6, data I/O with 8, and uses 1 each for logic and earth grounds. As many as 15 programmable devices having IEEE-488 interfaces may be interconnected simultaneously. Max transmission path is 20 m. Electrical specs include 5.2 ns/m time delay, 115 pF/m capacitance nom for single conductors and 116 pF/m nom for pairs. **Belden Corp, Electronic Div,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 277 on Inquiry Card

DIGITAL DATA RECORDER

A portable solid-state recorder for data compression and editing has a storage capacity of up to 64 x 10^{10} bits. The ASCII/IEEE interfaced ADASTOR™ recorder and associated readout device present a histogram analysis of stored data

for CRT display or a hardcopy listing in seconds. For use in remote or mobile testing, the device has an operating temp range from −40 to 60°C, relative humidity from 9 to 95%. Power is supplied by internal long-life rechargeable batteries, allowing continuous operation for 80 to 1800 h; memory circuits maintain data in standby for min of 3 yr. Auxiliary power sources, including a solar cell panel, are available for unlimited continuous operation. **Sun Systems, Inc**, PO Box 182, Sun Valley, ID 83353.

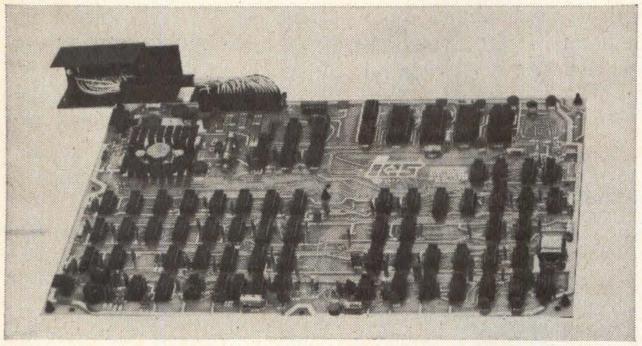
Circle 278 on Inquiry Card

PARALLEL TRANSFER DISC DRIVE

The PTD-9300 disc drive offers an 8- or 9-bit parallel transfer capability and 300M-byte storage capacity for rapid processing of large amounts of data for OEM random access and wide bandwidth applications. The self-contained, single spindle, direct access storage unit utilizes a std IBM 3336 Mod 11-type removable disc pack containing 815 cylinders of 19 data tracks. The device provides the control unit with concurrent access to a group of disc tracks permitting simultaneous writing or reading of all tracks within the group; data transfer rates are up to 87M bits/s. Std configuration contains 2 groups of 9 tracks/disc cylinder. Both 4- and 6-track/group configurations also are available. Data interface is in NRZ format. **Ampex Corp**, 401 Broadway, Redwood City, CA 94063.

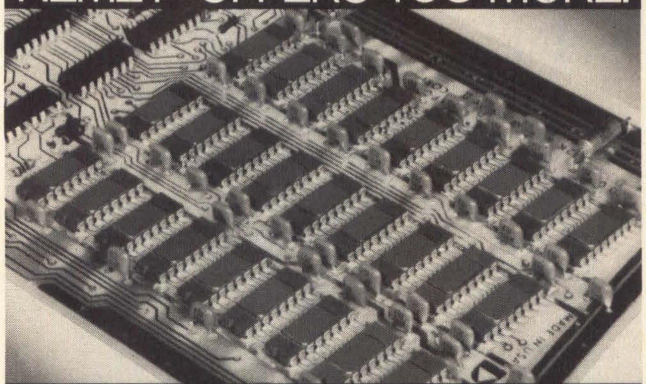
Circle 279 on Inquiry Card

TELEPRINTER INTERFACE



C/D-40 interface board allows the 300-line/min Teletype Corp model 40 printer to connect to a host computer or terminal that offers a Centronics or Dataproducts interface. Complete hardware/software transparency is provided. Self-contained device derives power from the printer when mounted within the cabinet. It may also be mounted inside the host system, allowing computer/printer separation via 2-wire pairs up to 2k ft (610 m). Std features include a 160-char FIFO buffer, selectable control char code conversion, parity selection, extended ASCII, and variable motor time out after last char received. Options are bell/alarm, elapsed time indicator, manual select switch, and programmable code converter. **Innovative Electronic Systems, Inc**, 15200 NW 60th Ave, Miami Lakes, FL 33014.

Circle 280 on Inquiry Card



PRODUCTS

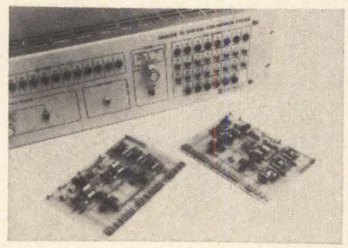
PRINTER/CARD READER SYSTEM

A high speed I/O system functionally compatible and software transparent with IBM System 360/370 and 303X, model 4800 I/O set consists of a controller, 1 or 2 1200-line/min printers and an optional 1000-card/min card reader. The system attaches to selector or multiplexer channels through the controller for simultaneous operation. The 132-col line printer, using the Chaintrain printing technique, includes a sound-deadening cabinet, static eliminator, paper puller, single line memory buffer, and EBCDIC 48-char lower case set and coding. Card reader features a LED/phototransistor read station, patented vacuum pick mechanism, 1000-card hopper, and straight through card track. **California Computer Products, Inc,** 2411 W La Palma Ave, Anaheim, CA 92801.

Circle 281 on Inquiry Card

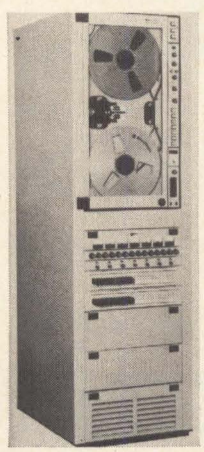
MULTICHANNEL ADC SAMPLE AND HOLD AMPLIFIER

Developed for use with the GM series of high speed A-D conversion systems, the model GMSH-4A amplifier combines hold aperture jitter (10 ns), droop (max of 1 mV over a hold period as long as 1 ms), and hold aperture duration (100 ns including interchannel scatter) to achieve 0.03% accuracy over the full range of input frequencies and signal amplitudes. The card can be used with a wide range of input signals. Input impedance is >10 MΩ; input voltage range and gain has unity gain at input voltage up to ±10 V; output voltage is ±10 V; and output impedance is <1 Ω. Std model accepts normal single-ended input signals with 1 side grounded. Differential input buffer amplifier is optional. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.



Circle 282 on Inquiry Card

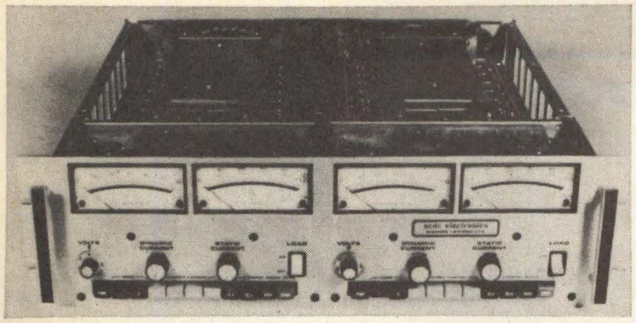
LAB MAG TAPE RECORDER/ REPRODUCER



Bidirectional capability in 9 speeds is featured in the 3700E laboratory device to save time by recording data signals in the forward direction, then reproducing within all specs in reverse, with a fidelity of ±1 dB. Tracks may be recorded and reproduced simultaneously. Full phase adjustable equalization allows accurate analog data reproduction without phase distortion. Both 7- and 14-track versions function with tapes recorded at std, ½, or twice IRIG frequencies. Data signals over bandwidths from 100 Hz to 2 MHz can be handled at speeds up to 240 in (610 cm)/s. Serial and parallel enhanced-NRZ electronics record at any rate up to 3.5M bytes/s track. **Bell & Howell, Datatape Div,** 300 Sierra Madre Villa Ave, Pasadena, CA 91109.

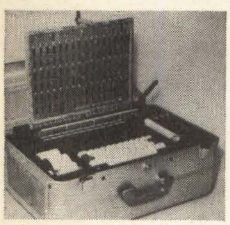
Circle 283 on Inquiry Card

DUAL PROGRAMMABLE ELECTRONIC LOAD



A dual, 19" (48-cm) rackmounted version of the EL-750 load can verify dc power supply outputs as high as 1500 W. Operating in the constant resistance mode, the unit is used to test performance of dc power sources by static or dynamic resistance loading; in the constant current mode, it simulates the constant current discharge of batteries and capacitor banks. It can become an adjustable constant current supply in conjunction with a dc power source. Load current programming and dynamic loading can also be accomplished. Three internal fault indicators identify overtemps, overvoltage, or overcurrent, and load saturation (undervoltage) conditions. Max voltage is 50 Vdc, with min of 3 Vdc. **ACDC Electronics, div of Emerson Electric Co,** 401 Jones Rd, Oceanside, CA 92054.
Circle 284 on Inquiry Card

COMPONENT LEVEL PORTABLE PC BOARD TESTER



With automatic guided-probing fault isolation and interactive programming, the portable service processor provides high speed testing on digital PC boards. Field test functions include exercising and simulating peripherals, programming p/ROMs and EAROMs, loading nonresident diagnostics, and testing communications channels. Hardware elements consist of a 400-ns processor with 2k words of ROM; 2k x 16-bit p/ROM; 32k bytes of RAM; and 3M mag tape cartridge drive for 2.5M bytes of storage. Also included are EIA RS-232 and V24 interfaces, LED and hardcopy displays, full alphanumeric keyboard, DMM, driver/sensor pin subsystem, probe, and fully programmable power supplies. System software is written in micro and macrocode, and higher level languages. **Omnicomp, Inc,** 5150 N 16th St, Suite 253, Phoenix, AZ 85016.
Circle 285 on Inquiry Card

8k-BYTE CMOS RAM BOARD

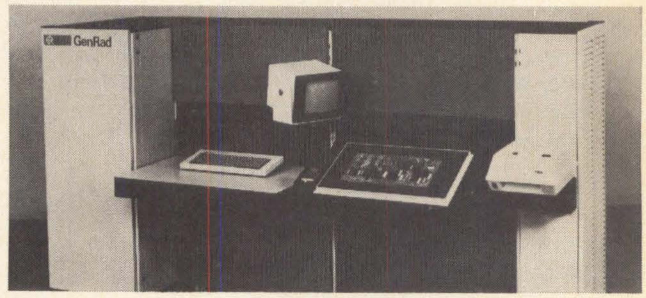
The high density, low power 1814 module features an 8k-byte RAM with a 450-ns memory cycle which insures that it will run at CPU speeds. Built-in battery backup and charging circuitry retain information for min of 7 days. The module also provides for an external battery. Switch selectable write protect aids development and debugging. Modules may be used in the same SuperPac 180 series microcomputer system. Basic module has 4k bytes of RAM, with sockets provided for an additional 4k bytes. Base starting address is switch selectable; another switch allows disabling of the upper 4k bytes of RAM. A second version has a full 8k bytes of RAM installed. **Process Computer Systems, Inc,** 750 N Maple Rd, Saline, MI 48176.
Circle 286 on Inquiry Card

PRODUCTS

DATA/VOICE COUPLING TRANSFORMERS

Hybrid, coupling, and impedance matching transformers meet part 68 FCC and telephone requirements for interconnecting to std telephone lines. Hybrids allow terminal to line interconnect; matching devices give proper subsystem performance. Units feature high potential insulation, balanced and split windings for broad frequency response, performance testing, low leakage current, and precision longitudinal balance. Hybrid parts are rated for 600-to-600 Ω split, and coupling/matching transformers are designed for 600:600 or 600:900. All are rated for 0-, 60-, 100-, and 120-mA dc unbalance. Holding coils are rated at 1.3 H, 100 mA dc, 180 Ω; 0.8 H at 25 mA dc, 225 Ω; and 0.8 H at 40 mA dc, 115 Ω. **Magnetico, Inc,** 182 Morris Ave, Holtsville, NY 11742.
Circle 287 on Inquiry Card

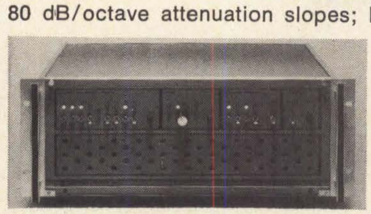
IN-CIRCUIT PC BOARD TESTER



The 2270 functional test system performs cost-effective diagnosis of digital, analog, and hybrid PC board assembly faults through automatic electrical inspection. Solder shorts, opens, and wrong, missing, backwards, incorrectly seated, and out-of-tolerance parts are identified in a single pass and described in English by a printed board-repair message. Software generates 75 to 80% of the test program from table-formatted circuit topology descriptions. Interaction with the system during testing is through a relocatable keypad. The computer is an LSI-11 with floating-point math processing, ROM bootstrap loading, power up/down protection, and a 32k x 16 memory; 768k bytes of disc storage are included. Other features are an ASCII strip printer, 9" (23-cm) CRT display, and 4-line scanning. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.
Circle 288 on Inquiry Card

16-CHANNEL PROGRAMMABLE FILTER SYSTEM

Multichannel filter system 616 features programmable gain and cutoff frequency. Plug-in high and low pass Cauer filters in the 0.01-Hz to 150-kHz frequency range are offered with 80 dB/octave attenuation slopes; low pass, time delay filter



is offered with linear phase response for use with pulse or transient waveforms. Unit has precisely controlled 6-pole, 6-zero elliptic filters with 0.1 dB pk-pk passband ripple; typ phase match between two channels is < 0.5 deg from dc to cutoff frequency. Interface options are for the GPIB, EIA RS-232-C or 20-mA current loop, and buffered I/O card. System is comprised of a plug-in control module and up to 16 filters in a 7" (18-cm) high rackmounting mainframe. **Precision Filters, Inc,** 303 W Lincoln, Ithaca, NY 14850.
Circle 289 on Inquiry Card

LITERATURE

Personal Computing Systems

Contents of 104-pg catalog include full display and description of personal computing systems, radio products, and electronic test instrumentation. **Heath Co,** Benton Harbor, Mich.
Circle 300 on Inquiry Card

Flexible Disc Drives

Brochure highlights features and specs of four flexible disc drives, all having a max storage capacity of 6.4M bits and ferrite R/W heads. **Pertec Computer Corp, Pertec Div,** Chatsworth, Calif.
Circle 301 on Inquiry Card

Automatic Test Equipment

Booklet points out features, software, and stimulus and measurement modules for model 331 computerized ATE system with analog and digital capability. **SIR Atlanta, Inc,** Atlanta, Ga.
Circle 302 on Inquiry Card

Synchronous Mag Tape Systems

Tape transport specs, features, capabilities, and compatibilities are discussed in product catalog presenting Mini-, Midi-, and Maxidek magnetic tape transports. **Digi-Data Corp,** Jessup, Md.
Circle 303 on Inquiry Card

Generators and Synthesizers

Containing detailed specs for each function and waveform generator, and frequency synthesizer, catalog supplies short-form and comparison charts. **Exact Electronics, Inc,** Hillsboro, Ore.
Circle 304 on Inquiry Card

VMOS Power FETs

Literature consists of brochure, design catalog, and selector guide featuring data sheets, application notes, and design aids for line of VMOS power FETS. **Siliconix inc,** Santa Clara, Calif.
Circle 305 on Inquiry Card

Data Communications' Buzzwords

Total of 183 data communications and processing terms are defined in 1978 edition of booklet, with addition of words currently in common usage. **Racal-Milgo, Inc,** Miami, Fla.
Circle 306 on Inquiry Card

TWX/DDD Modem

Brochure details operation of model 4700 modem that replaces the Bell 101C data set, with features such as auto/answer, half-duplex switching, auto/answer back, and call abort timer. **Omnitec Corp,** Phoenix, Ariz.
Circle 307 on Inquiry Card

Planar Gas Discharge Displays

Tables of specs and operating conditions, diagrams, and photos illustrate catalog on raised cathode, screened image, and self-contained planar gas discharge modules and accessories. **Beckman Instruments, Inc, Information Displays Operations,** Scottsdale, Ariz.
Circle 308 on Inquiry Card

High Speed A-D Converters

Data sheet outlines 2813 family of ADCS with throughput rates to 1.33 MHz by presenting block and timing diagrams, operating specs, and connection and mechanical notes. **Dynamic Measurements Corp,** Winchester, Mass.
Circle 309 on Inquiry Card

Computer Compatible Interface Modules

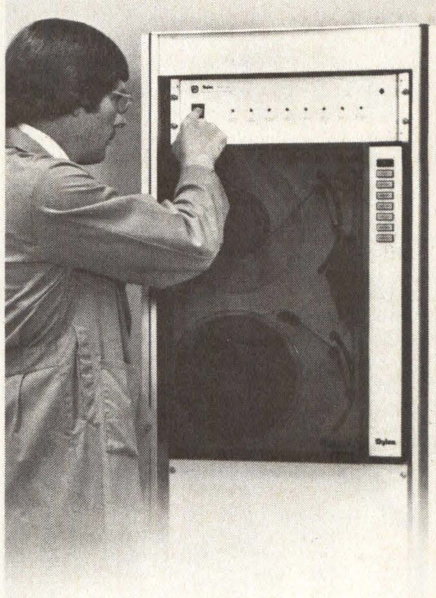
Features and tables on MP-System 1000 digital voltmeters, timer counters, and logic distribution panels are included in data sheet giving information on modules for A-D and D-A interfacing. **Pacific Photometric Instruments, McKee-Pederson Instruments,** Emeryville, Calif.
Circle 310 on Inquiry Card

Direct Reading Tape Programmer/ Control Systems

Diagrams and photos in 8-pg booklet show configuration and operating characteristics of modification options, direct reading tape programmers, and custom-designed control systems. **Industrial Timer Corp,** Parsippany, NJ.
Circle 311 on Inquiry Card

Computer Network Interconnection

Report identifies barriers to interconnection and surveys solutions by offering organizational and technical background, bibliography, glossary, and listing of relevant data communications standards. Price of SD No. 003-003-01757-4 is $1.45. **Superintendent of Documents, U.S. Gov't Printing Office,** Washington, DC 20402.



LITERATURE

Image Processing

Illustrated brochure covers image enhancement, information extraction, and quantitative restoration for diverse areas of computer-aided scanning and writing techniques. **Optronics International, Inc,** Chelmsford, Mass.
Circle 312 on Inquiry Card

Connectors

Featuring spec charts, catalog provides photos of application board mountings as well as line and dimensional drawings of Term-Acon[R] series 1000, 2000, and 3000 miniature PC card and cable-to-cable connectors. **Methode Electronics, Inc,** Rolling Meadows, Ill.
Circle 313 on Inquiry Card

LED Display-Microprocessor Interfacing

Application note 9A details methods of interfacing the model DL-1416 4-char LED alphanumeric display module with microprocessors such as the 8080, Z80, and 6800. **Litronix, Inc,** Cupertino, Calif.
Circle 314 on Inquiry Card

Microprocessor-Controlled Display Subsystems

Self-Scan[R] displays, featuring microprocessor control, are explained in brochure that specifies how they reduce time required to design and build frontend circuitry. **Burroughs Corp, Electronic Components Div,** Plainfield, NJ.
Circle 315 on Inquiry Card

Computer-Based Analysis

Application note discusses advantages and potential obtained by interfacing the TF 2370 spectrum analyzer to a computer's computational power and analysis. **Marconi Instruments, Div of Marconi Electronics Inc,** Northvale, NJ.
Circle 316 on Inquiry Card

Precision Digital Voltmeter

Catalog exhibits graphically illustrated voltage and resistance specs and photos highlighting function and control of model 9577 radical 7½-digit DVM. **Guildline Instruments, Inc,** Elmsford, NY.
Circle 317 on Inquiry Card

Monitor Scopes/Meters

Application areas, detailed specs, and theory of operation are highlighted for monitor oscilloscopes, meters, and tape recorder analyzers in a short-form catalog. **Data Check Corp,** San Diego, Calif.
Circle 318 on Inquiry Card

Integrated Circuit Design

Three application notes, APN-2, -3, and -4, discuss methodology of designing ICs using worst case performance parameters; log/linear circuit, which achieves low noise and distortion; and crystal oscillators, which can be combined with semicustom IC technology. **Interdesign, Inc,** Sunnyvale, Calif.
Circle 319 on Inquiry Card

Thumbwheel Switches

Supplying truth tables, functional descriptions, and ratings, catalog covers Snap'n Mount™ no-hardware thumbwheel switches with up to 16 positions, voltage dividers, and resistance decade switches. **Unimax Switch Corp,** Wallingford, Conn.
Circle 320 on Inquiry Card

Computers and Communications

"Communications: Toward a Global Community" explains interactions between computers and communications through articles covering networks, facilities, and contributions to national defense. **Computer Sciences Corp,** El Segundo, Calif.
Circle 321 on Inquiry Card

Database Management Systems

Brochure facilitates application of database management techniques and outlines operation, organization, languages, and resource utilization requirements of the company's system. **International Data Base Systems, Inc,** Philadelphia, Pa.
Circle 322 on Inquiry Card

Centrifugal Blowers

Updated catalog, including sections on technical notes and std connection diagrams, covers ac and dc motor driven blowers meeting a range of cooling requirements. **IMC Magnetics Corp,** Westbury, NY.
Circle 323 on Inquiry Card

Microelectronic Data Acquisition Systems

Color brochure details electrical and mechanical parameters, pin connections, timing diagrams, calibration procedures, applications, and performance data for models HDAS-16 and -8 12-bit data acquisition systems. **Datel Systems, Inc,** Canton, Mass.
Circle 324 on Inquiry Card

 CIRCLE 148 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

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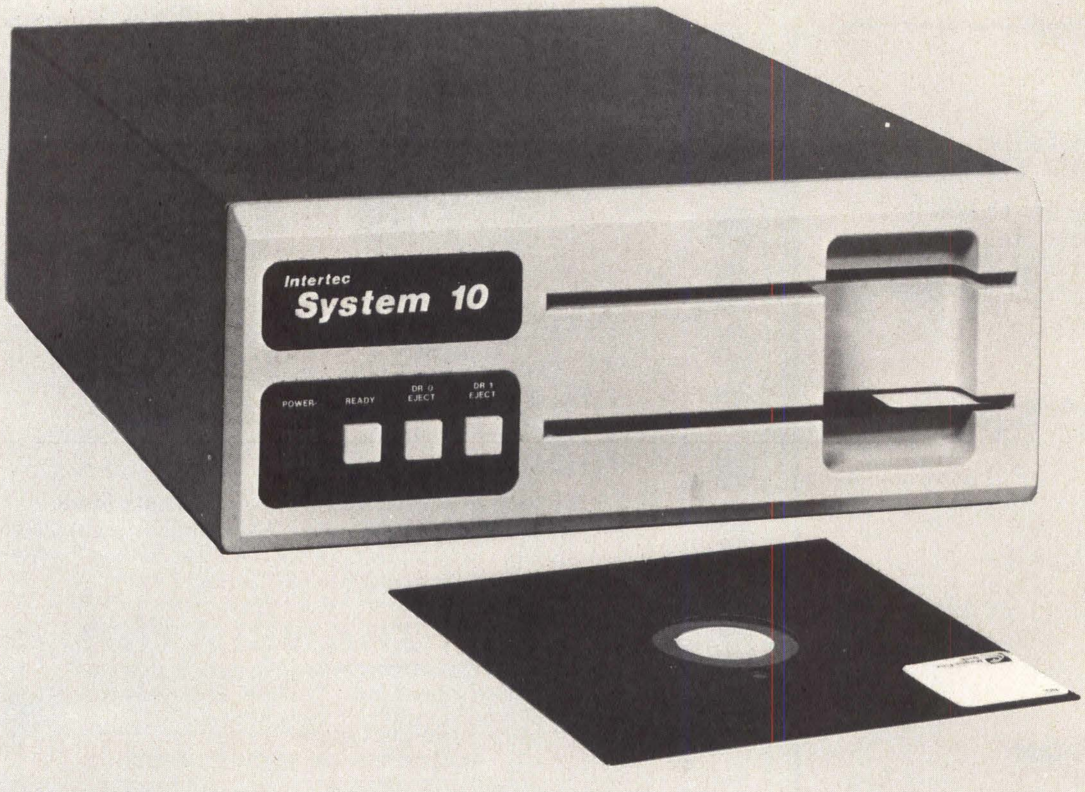
Introducing
INTERTEC's New Small Business Computer



TOP PERFORMANCE - BOTTOM DOLLAR

Top performance from your small business computer doesn't have to mean you pay top dollar. Intertec's new **System 10** Computer combines extraordinary performance with a moderate price to bring you all the flexible computing power you've always wanted. The **System 10** Computer is a complete integrated data processing system consisting of a dual flexible disk drive for on-line storage, a general purpose digital computer for control, two serial I/O ports, a parallel I/O interface and a complete disk operating system.

Every **System 10** Computer features a voice-coil driven dual flexible disk drive. This drive represents the latest in state-of-the-art technology and provides a faster "track seek" than any other comparable drive on the market today. In addition, the **System 10** drive features a sophisticated electronic disk loading and handling system which helps to insure long diskette life and minimum diskette wear.

The processor used in our Intertec **System 10** Computer is the Z80 – a super-set of the Intel 8080 with many enhancements such as a dual register set and numerous additional instructions including indexed addressing. The Z80 processor provides all control functions and includes an 8 bit memory word length and an automatic power-up restart system.

Each **System 10** comes equipped with two serial RS–232C compatible I/O ports. Both of these ports are included in the standard price of the **System 10** and may be used to connect the computer with an external modem, a terminal and/or a line printer. **System 10** also features a complete parallel I/O system interface which can be used to interface with external devices and communications facilities.

System 10's Disk Operating System (DOS) provides the user with extensive file handling capability and greatly facilitates the design and execution of user programs. Our DOS uses IBM compatible flexible disks for backup storage. The DOS provides an excellent environment for program construction, storage, editing and assembly and program checkout capabilities. The DOS provides rapid access to programs through a comprehensive file management package. Using this system, a large number of distinct programs can be stored in both source and machine code. DOS also supports a powerful context editor, an 8080 compatible assembler and a debugger subsystem.

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704/377-0300

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CIRCLE 158 ON INQUIRY CARD

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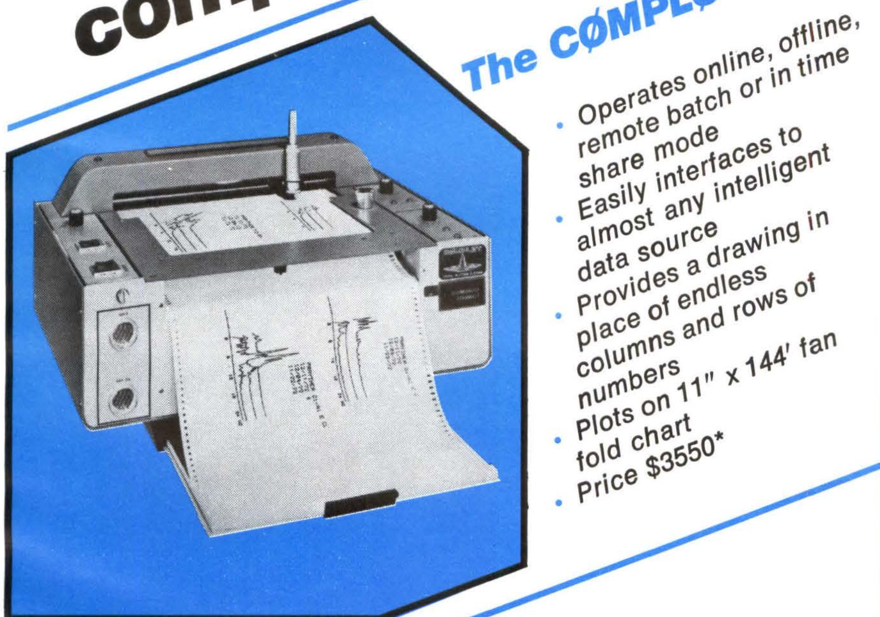

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- Easily interfaces to almost any intelligent data source
- Provides a drawing in place of endless columns and rows of numbers
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"The recorder company"

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...systems flexible enough to use in a wide variety of applications. Systems easy to build, easy to service. Systems in which every part—the microprocessor, every semiconductor, every connector, every miscellaneous component—is or soon will be a second-sourced industry standard.

Card	PLS 881	PLS 888	PLS 858	PLS 868	PLS 898
Processor	8080A	8080A	8085	6800	Z-80
PROM* Capacity	4K (2708)	8K (TMS2716)	8K (2716)	8K (2716)	8K (2716)
RAM** Capacity	1K	2K	2K	2K	2K
Input Ports (8 lines)	2	2	2	2	2
Output Ports (8 lines)	3	3	3	3	3
100 Piece Price	$165	$185	$185	$185	$185

*PROM not included. **1K of RAM included.

Our comparison guide helps you avoid the pitfalls of microprocessor design.

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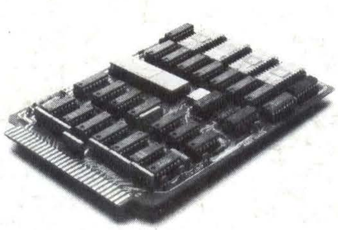

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