

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

OCTOBER 1979

**BIT SLICE TECHNIQUE MINIMIZES
MICROCONTROLLER COST/COMPLEXITY**

**ADD-IN CACHE MEMORY DOUBLES
MINICOMPUTER PROCESSING SPEED**

**LSI CHIPS EASE IEEE
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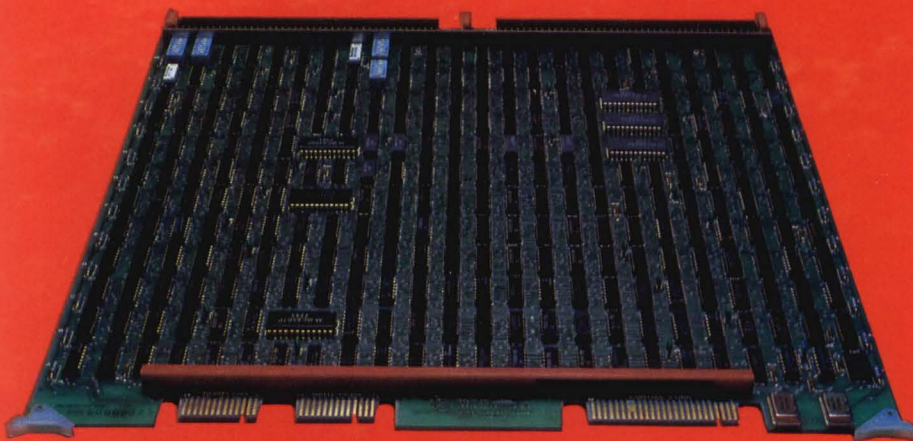
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CIRCLE 3 ON INQUIRY CARD



DEPARTMENTS

6 CALENDAR

8 LETTERS TO THE EDITOR

10 COMMUNICATION CHANNEL

Interest in teletext and videotex is growing all over the world. Features of Prestel, ANTIPOE, and Telidon, as exemplars of these systems, are briefly examined

34 DIGITAL TECHNOLOGY REVIEW

An understanding of the factors that influence IC manufacturing costs, and hence prices, helps today's designer to maintain the necessary awareness to develop cost effective systems

74 DIGITAL CONTROL AND AUTOMATION SYSTEMS

Monitoring and control system for batch or continuous blending operations incorporates a specially designed small, bit slice, stack processor

142 TECH BRIEFS

147 MICRO DATA STACK/COMPUTERS, ELEMENTS, AND SYSTEMS

A multi-application system configuration of the 6800 microprocessor interfaces to external devices using a minimum of hardware

168 AROUND THE IC LOOP

Substantial improvements in throughput of bit slice implementations result from the use of pipelined prediction techniques coupled with variable microcycle timing

193 PRODUCT FEATURE

Signal processing capabilities of a single-chip programmable, realtime, analog/digital microcomputer are equivalent to 100 times those of a standard 8080

234 LITERATURE

238 GUIDE TO PRODUCT INFORMATION

246 ADVERTISERS' INDEX

Reader Service Cards
pages 249-252

FEATURES

BIT SLICE TECHNIQUE MINIMIZES MICROCONTROLLER COST/COMPLEXITY 105
by David Hooley

Bit slice control elements exhibit performance, architecture, and cost advantages over small scale control logic in a digitally controlled measurement process

ADD-IN CACHE MEMORY DOUBLES MINICOMPUTER PROCESSING SPEED 115
by Ronald N. Monroe

Cache memory design accommodates dual bus architecture of a minicomputer CPU so that most fetch requests are handled by add-in cache for significantly higher processing speed

LSI CHIPS EASE IEEE STANDARD 488 BUS INTERFACING 123
by Ronald M. Williams

GPIB peripheral pair implemented in LSI chip set simplifies the design effort and reduces overall cost of coupling a microprocessor based system to the IEEE Standard 488-1978 interface bus

THERMAL PRINthead TECHNOLOGY AND DESIGN 134
by William Boles

Three current thermal printing technology concepts are examined in arriving at an advanced thermal printhead design

CONFERENCE

MIDCON 100
New concepts in high technology electronics provide the focus of this year's Midcon, covering such areas as microcomputer, microprocessor, memory, and control trends and applications



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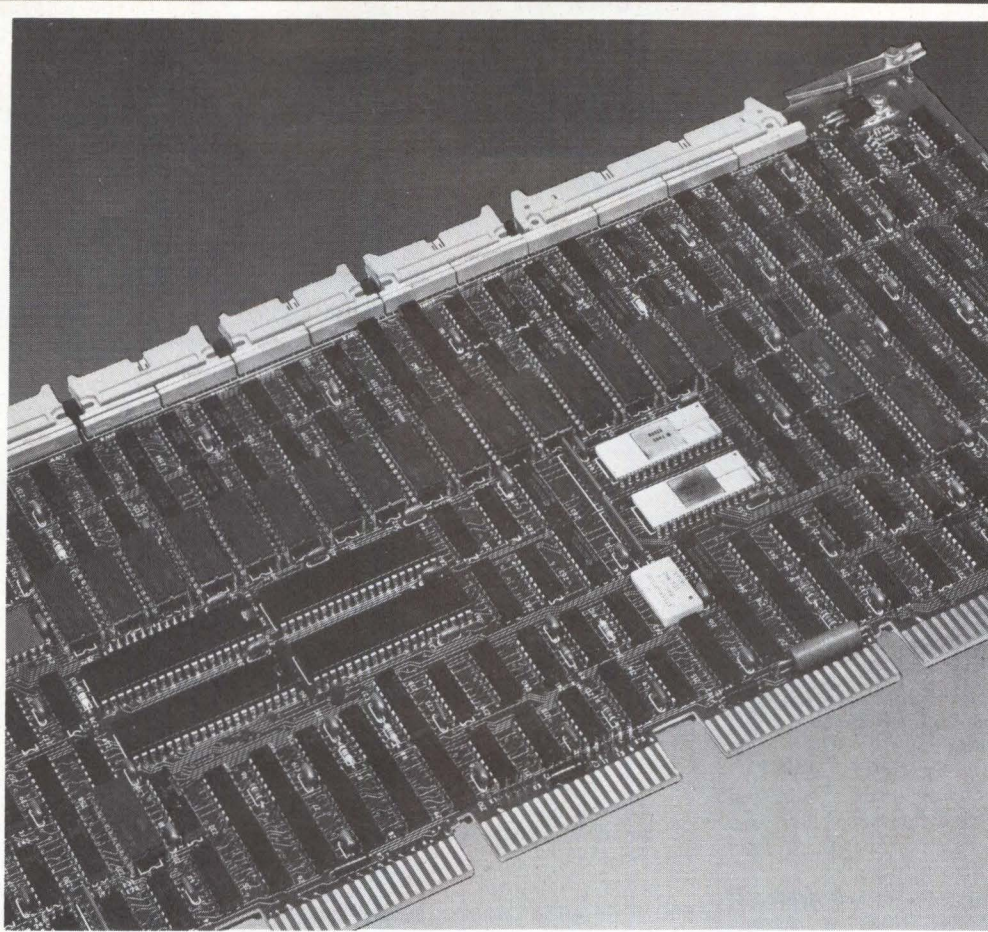
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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

OCT 30-NOV 1—CAD/CAM VII at Automated, Integrated, Factory of Tomorrow Conf, Cobo Hall, Detroit, Mich. INFORMATION: Jeff Spire, SME Technical Div, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500, X405

OCT 30-NOV 1—Interface West, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

NOV 1 AND 15—Invitational Computer Conf, Cherry Hill, NJ; and Southfield, Mich. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 5-7—Asilomar Conf on Circuits, Systems and Computers, Asilomar Hotel and Conf Grounds, Pacific Grove, Calif. INFORMATION: Donald E. Kirk, Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-2081

NOV 5-8—Computer Software and Applications Conf (COMPSAC), The Palmer House, Chicago, Ill. INFORMATION: Dr William Smith, Bell Laboratories, Naperville, IL 60540. Tel: 312/690-2389

NOV 6-8—Federal Computer Conf, Sheraton-Park Hotel, Washington, DC. INFORMATION: Federal Computer Conf, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181

NOV 6-8—MIDCON, O'Hare Convention Ctr and Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 9-11—Midwest Small Business and Consumer Expo, O'Hare Exposition Ctr, Chicago, Ill. INFORMATION: Louise Garcia, 1453 Rio Rancho Dr SE, Rio Grande, NM 87124. Tel: 505/897-1971

NOV 14-16—Micro and Mini Computer Conf, Astro Village, Houston, Tex. INFORMATION: Dr Sam Lee, School of Electrical Engineering and Computer Science, U of Oklahoma, 202 W Boyd, Norman, OK 73019. Tel: 405/325-4721

NOV 18-21—Micro 12, Hershey, Pa. INFORMATION: Harry Hayman, Micro 12, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

NOV 26-29—Data Communications Sym and Tutorial, Asilomar Conf Grounds, Pacific Grove, Calif. INFORMATION: Kenneth J.

Thurber, Sperry Univac, U2U19, PO Box 3525, St Paul, MN 55165. Tel: 612/456-3806

NOV 26-29—Internat'l Telecommunications Energy Conf (INTELEC), Sheraton Park Hotel, Washington, DC. INFORMATION: R. H. Jones, ITT North Electric, PO Box 688, Galion, OH 44833. Tel: 419/468-8525

NOV 27-29—Nat'l Telecommunications Conf, Shoreham-Americana Hotel, Washington, DC. INFORMATION: John N. Birch, Dept of Defense, 3311 Marlborough Way, College Pk, MD 20740. Tel: 301/935-0684

DEC 3-5—Internat'l Electron Devices Meeting (IEDM), Washington Hilton Hotel, Washington, DC. INFORMATION: Sarah M. Cooper, Courtesy Assoc, Inc, 1629 K St, NW, Suite 700, Washington, DC 20006

DEC 10-11—Internat'l Sym on Mini & Microcomputers in Control, Galt Ocean Mile Hotel, Ft Lauderdale, Fla. INFORMATION: The Secretary, Computers in Control Sym, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

DEC 10-14—IEEE Computer Society Tutorial Week, Hotel Del Coronado, San Diego, Calif. INFORMATION: Tutorial Week 79, PO Box 639, Silver Spring, MD 20901

DEC 12—Computer Networking Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JAN 7-10—ATE Seminar/Exhibit, Pasadena Convention Ctr, Pasadena, Calif. INFORMATION: Karen Knope, ATE Seminar/Exhibit, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JAN 23-25—Internat'l Microcomputers, Mini-computers, Microprocessors (IMMM)—Japan '80, Harumi Exhibition Ctr, Tokyo, Japan. INFORMATION: Industrial & Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

JAN 30-FEB 1—MIMI'80 Asilomar (Internat'l Sym on Mini & Microcomputers), Asilomar Conf Grounds, Pacific Grove, Calif. INFORMATION: The Secretary, MIMI'80 Asilomar, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

FEB 13-15—Internat'l Solid State Circuits Conf, Hilton Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 19-22, 26-29, AND MAR 5-7—TechEx America, Europe, and Asia, Atlanta, Georgia, U.S.A.; Copenhagen, Denmark; and Singa-

pore, Republic of Singapore. INFORMATION: Dr Dvorkovitz & Assoc, PO Box 1748, Ormond Beach, FL 32074. Tel: 904/677-7033

FEB 25-28—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

MAR 4-6—Internat'l Zurich Sem on Digital Communications, Zurich, Switzerland. INFORMATION: Prof P. E. Leuthold, Eidgenossische Technische Hochschule Zurich, Institut fur Hochfrequenztechnik, Sternwartstrasse 7, Zurich, Switzerland

MAR 24-28—Eurocon'80 (European Conf on Electrotechnics), Stuttgart, Germany. INFORMATION: Prof Dr W. E. Proebster, IBM Deutschland GmbH, Postfach 80 08 80, D-7000 Stuttgart 80, Germany

SEMINARS

NOV 1 AND 2—NC Machine Control Maintenance Sems, Holiday Inn/Airport North, Dallas, Tex, and Airport Marina Hotel, Los Angeles, Calif. INFORMATION: Elaine Skott, Numerical Control Soc, 1800 Pickwick Ave, Glenview, IL 60025. Tel: 312/724-7700

NOV 7-9, JAN 14-16, AND MAR 3-5—Mini-computers and Distributed Processing Sem, Miami, Fla; San Francisco, Calif; and Washington, DC. INFORMATION: Heidi E. Kaplan, Dept 20NR, The University of Chicago Conf Ctr, 360 Lexington Ave, New York, NY 10017. Tel: 212/953-7262

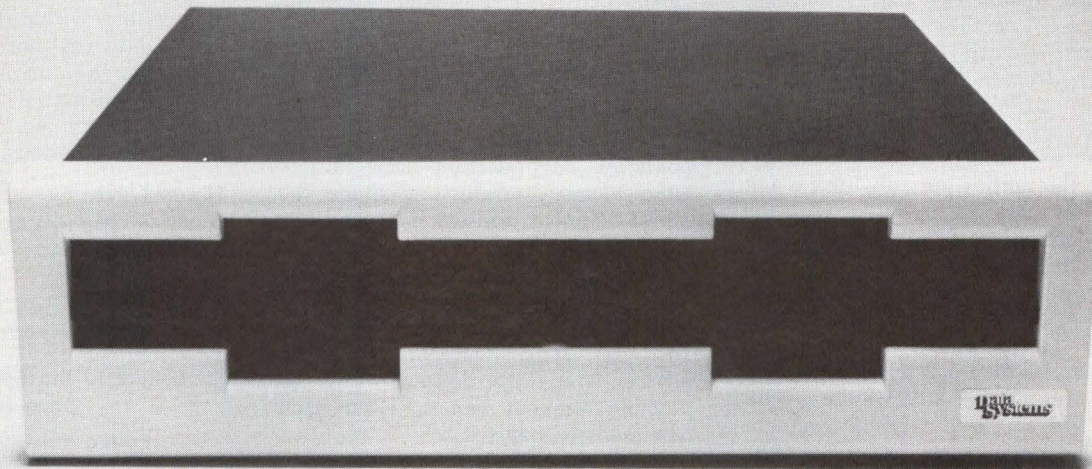
SHORT COURSES

3-Day Microprocessor Course, Assembly Language Program for Microprocessor, Microprocessor Seminar, Fiber Optics, and Computer Automated Measurement & Control. INFORMATION: Vincent J. Giardina, Mgr of Continuing Education, 445 Hoes Ln, Piscataway, NJ 08854. Tel: 201/981-0060, X174

DEC 10-12—Project Management for Computer Systems, Chicago, Ill. INFORMATION: University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago, IL 60637

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CIRCLE 6 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

I must object to the technical errors contained in the article "Comparing Architectures of Three 16-Bit Microprocessors" (by Henry A. Davis, pp 91-100) in the July issue of *Computer Design*.

In particular, the first paragraph on page 97 of that issue makes this statement regarding the 8086: "The actual address—called the physical address—is formed by adding a 4-bit effective address to a 16-bit segment register, resulting in a 20-bit address." Where the author got this idea is not clear. Compare his statement with the correct statement from Intel's MCS-86 User's Manual: "Bytes or words within a segment are addressed using 16-bit offset addresses, or effective addresses (EA), within the 64k-byte segment. A 20-bit physical address is constructed by adding the 16-bit offset address to the 16-bit segment address with four low-order zero bits appended [to the segment]. That is, they are left-shifted four places." The author also makes another peculiar

statement within that paragraph: "... the code segment usually begins at FFFFF₁₆ to handle the reset vector." Since FFFFFH is the end of maximum memory directly supported by the 8086, it appears that the author is suggesting that a code segment be placed in never-never land. The fact of the matter is as follows: after the RESET pin has been held high, the processor sets CS = FFFFH and IP = 0000H so execution will begin at FFFF0H.

Furthermore, this author failed to point out an important basic fact of 8086 memory addressing. Since the 16-bit segment address is shifted left 4 bits before being added to the offset, there are actually 2¹⁶ possible segments within 1M bytes of memory; ie, a segment boundary occurs every 16 bytes. This fact confuses 8086 novices who think there are only 16 possible segment values, 1 for each 64k memory page.

Edward Arnold
STC Communications Corp
Broomfield, Colo

The Author Replies:

The errors pointed out by Mr Arnold crept into the paper during the editing and revision of over 60 typed pages of original manuscript, and are entirely my responsibility as its author. Since the paper provided as fair a comparison of the three processors as possible within the space limitations and was not intended as an exhaustive treatment of each processor, the omission of the final details of 8086 memory addressing does not strike me as serious.

Henry Davis
American Microsystems, Inc
Santa Clara, Calif

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4	30B-040	30W-040	30Y-040	6.75	28B-040	28W-040	28Y-040	7.50	26B-040	26W-040	26Y-040	8.50
4.5	30B-045	30W-045	30Y-045	7.07	28B-045	28W-045	28Y-045	7.87	26B-045	26W-045	26Y-045	8.98
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6	30B-060	30W-060	30Y-060	8.00	28B-060	28W-060	28Y-060	9.00	26B-060	26W-060	26Y-060	10.35
7	30B-070	30W-070	30Y-070	8.63	28B-070	28W-070	28Y-070	9.75	26B-070	26W-070	26Y-070	11.25
8	30B-080	30W-080	30Y-080	9.25	28B-080	28W-080	28Y-080	10.50	26B-080	26W-080	26Y-080	12.18
9	30B-090	30W-090	30Y-090	9.88	28B-090	28W-090	28Y-090	11.25	26B-090	26W-090	26Y-090	13.55
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VIDEOTEX AND TELETEX SYSTEMS

J. W. Hughes

Associate Editor

Some enthusiasts in the field, while admitting that "videotex" and "teletext" are not, presently, household words, anticipate that they or some trademarked derivatives may become as common as the terms "telephone," "radio," and "television." These system concepts are not exactly new, but technological advances, especially those that have made available the low cost large scale integration chip, and thereby an economically feasible decoding system, have brought their realization into the realm of practicality for broader applications. Videotex and teletext systems are undergoing increasing interest, scrutiny, and promotion. These systems are designed to display a wide variety of useful information on the screen of a television set located in the home or at a business office, using different transmission media as carriers.

Teletext is a 1-way broadcast system that transmits digitally coded information, inserted into the lines in the vertical flyback interval of the TV signal, that carry no picture information. Pages of text and rudimentary graphics, selected by the broadcaster, are sent in a cyclically repetitive manner. At the receiving end, a viewer operated decoder selects the pages of particular interest, using frame-grabber techniques.

Videotex, on the other hand, is an interactive, on-demand data retrieval service that uses the switched telephone network as a transmission medium to display on the receiver screen information requested by the user by means of an appropriate keypad.

British Systems

Probably the most advanced implementation of teletext and videotex systems is to be found in the United King-

dom. By way of historical interest, the teletext system arose from efforts by the British Broadcasting Company (BBC) and the Independent Broadcasting Authority (IBA) to accommodate digitally encoded alphanumeric data on field flyback television lines. Two teletext services resulted: CEEFAX ("see facts") from BBC, and ORACLE (optical reception of announcements by coded line electronics) from IBA.

Concurrently with these developments, work being carried out by the British Post Office (BPO) on Viewphone led to further investigations into using the narrow band dial-up telephone network for transmission of the same type of digital information, and using the home television (TV) receiver as the display. These investigations led to the development of the Viewdata system, now known as Prestel.*

CEEFAX, ORACLE, and Prestel are off and running in Britain. Standards have been adopted that allow user access to all services, since the memory, character generator, and display unit of the decoder are common to them all. The standards have established a 960-character display page of 40 char/line by 24 lines. Characters are in a 5 x 7 matrix, upper and lower case, with effectively identical character codes. There is a choice of seven colors. Table 1 highlights and compares the features offered by the three services.¹

Three major organizations participate in the Prestel service: BPO, which manages the computer system and the communications network; information providers (IPs), independent organizations supplying the data base with information pertinent to various fields of

*Prestel is the registered trademark of the BPO videotex service.

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TABLE 1
Teletext and Videotex Services

<u>Features</u>	<u>Teletext (Ceefax, Oracle)</u>	<u>Videotex (Prestel)</u>
Transmission medium	Broadcast	Telephone network
Information retrieval	Yes (limited)	Yes (unlimited)
Information sources	Broadcast/program companies only	Open-ended; about 160 organizations ^a
Message service	No	Yes (store-and-forward)
Calculations	No	Yes
Programmed learning	No	Yes
Enquiry page	No	Yes
Reservation mode	No	Yes
Problem solving	No	Yes
Facilities for deaf	Yes	Yes
Usage charge	No (currently)	Yes (where applicable)
24-h service	No	Yes
Response time	12.5 s avg (for 100-p system)	2 s avg (for 60k-p system)

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interest; and the TV manufacturers who supply videotex/teletext-compatible receivers.

Prestel operates over the 4-kHz bandwidth telephone network. Data are transmitted from computer to terminal at 1200 bits/s and on the return path at 75 bits/s. Standard 1200/75-bit/s limited distance modems are used, since operation is normally over short local network distances. This allows the modem to be integrated into the terminal and enables a simple plug and jack connection to the network. Where longer distances from the data bank are involved, separate standard modems may be needed.²

The system is accessed by a 12-digit keypad. Dial-up is programmed into the terminal, so no conventional "phone call" is necessary. With the TV set turned on, the local Prestel center is called by operation of a keypad button. Another button calls out a master index of main headings of available information. The viewer is guided by means of a "tree search" routine, which narrows the displayed information from the broad to the particular, by selecting via the keypad one numbered item from each frame on the tree until the required information is received. Where location of the desired page is known in advance, such as through a printed directory, direct access may be made, bypassing the tree search procedure.

Charges entailed by the user are on a per page information access basis, determined by the IP. This access may, in such cases as advertising or corporate image promotion, be free. There is a charge for normal local telephone usage. A page-handling charge covers system management costs. Charges are kept low compared to conventional timesharing and database access rates in order to insure the attractiveness of Prestel to a mass market, and to achieve the economies of scale that are essential to the success of the system.³

TABLE 2
Characteristics of ANTIOPE Teletext System

	525-line NTSC color	625-line PAL color	625-line SECAM color
Blanking lines	12	17	8
Useful bytes/line	20	32	32
Useful capacity— bits/s	9600	12800	12800
Pages/s for one line of data*	1.8	2	2
Max capacity on program channel (pp/s)	21	34	16
Max capacity on clear channel (pp/s)	450	610	610

*An average page includes 800 bytes

ANTIOPE

ANTIOPE, the French teletext system, is an acronym for "l'Acquisition Numérique et Télévisualisation d'Images Organisées en Pages d'Écriture," or paraphrased as "digital signal processing conversion to printed page images on home tv sets." It was developed at the Television and Telecommunications Research Center (CCETT) and has undergone field trials on the TDF network. It is currently implemented on two kinds of networks, the data broadcasting network DIDON, and public switched telephone and data networks.^{4,5} ANTIOPE is designed to give a broadcast, interactive, or mixed service, depending on the transmission medium.

The ANTIOPE system, while not nearly as advanced in implementation as Prestel, has such interesting features as an advanced communications protocol, a non-synchronous communications transmission scheme suited to all tv formats: PAL, SECAM, and NTSC (Table 2). The associated interactive system TITAN conforms to the same protocol.

Figure 1 shows a functional block diagram of the system. Composed and edited "magazines" (pages of related information) are converted into digital form, stored in a computer or floppy disc, and cyclically transmitted to a multiplex system (DIDON) where the data are separated into packets of 32 bytes and inserted into the free scan lines of the tv signal. Bit frequency is 397 times the line frequency, 6.203 MHz for France or 4.2 MHz for NTSC systems. Each packet is preceded by an 8-byte header: two for clock run in, one for framing synchronization, and five Hamming code protected bytes, as follows: three for source identification, one for packet continuity check, and one for the packet format.

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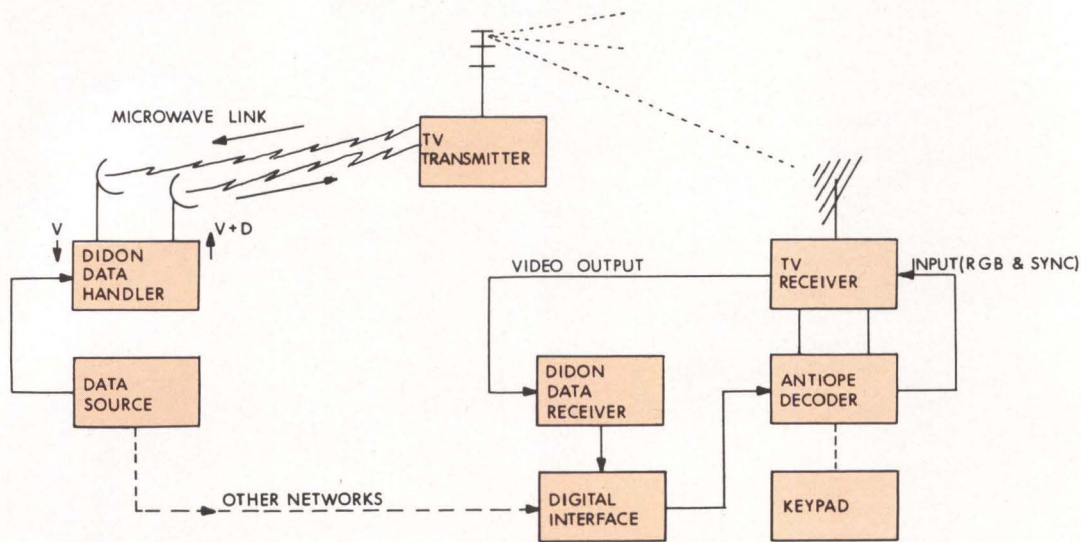


Fig 1 ANTIOPE system. Devices for editorial processing, layout, and updating of material are connected to data source, essentially minicomputers storing digital information. DIDON data handler inserts pulses from source into picture signal. At receiver, DIDON receiver strips data from video signal. When keyboard selects desired page, corresponding data are translated by processor in decoder into displayable characters, stored in decoder page memory, and displayed on screen. Interface unit permits data reception from other networks (interactive) or retrieval of data from DIDON receiver

The system can be expanded to use the full TV channel when the station is off the air in order to transmit large quantities of additional data which can be coded for proprietary access by special interest groups. By lowering the data rate to accommodate the transmission channel, ANTIOPE signals can be sent over telephone lines or FM radio stations.

Telidon

This is the Canadian videotex system developed at the Communications Research Centre (CRC) of the Department of Communications. Telidon is a public access information system, said to be a "second generation" approach to the design of videotex systems, that provides improved graphic images, and a method of describing images in the data base that is independent of terminal design and transmission media.^{6,7}

Both Prestel and ANTIOPE are fixed format, character oriented systems that produce rudimentary graphic images in an "alphanumeric" pattern on the display. In the European 625-line systems this display comprises 24 rows of 40 characters, or 960 character spaces, while in North America the 525-line system accommodates 20 rows of 40 characters for a character space area of 800. Images are built up in these spaces from

specially identified coded graphic characters, pieced together as individual sections of a complete image, as in a mosaic. This technique makes it impossible to send higher resolution images without knowing the display capabilities of the terminal; also, data bases might have to store many versions of each image in order to suit advances in terminal technologies and to satisfy a demand for improved graphics.

Telidon meets these problems by using a method of describing images at data banks that is independent of access arrangements at the central computer, of the communications medium, and of display terminal configuration and capability. The system incorporates a concept known as picture description instruction (PDI) codes.

PDI codes describe images in terms of commands to draw geometrical primitives such as line, arc, rectangle, and polygon at specific positions in the overall picture. The format enables sufficient resolution for monitors capable of displaying up to 960 x 1280 picture elements, or about four times that required for television screens. Practically all images can be described by seven basic instructions which are contained in 8-bit bytes. One bit is for parity to conform to current standards for data transmission. A shift-in (SI) com-

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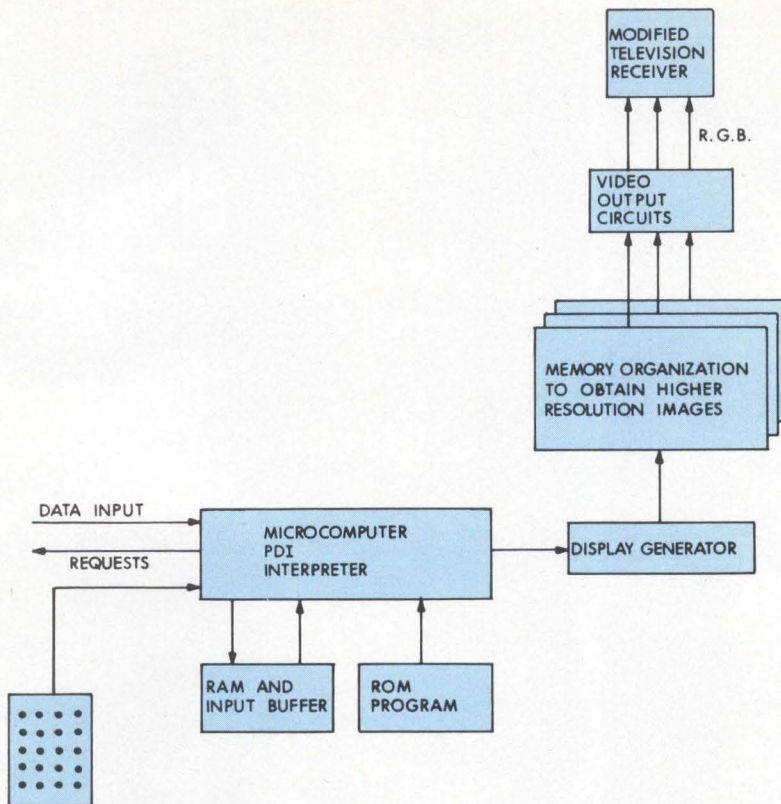


Fig 2 Telidon terminal with bit-map memory. Terminal can display photographic-like, as well as alphanumeric and graphic, images. Terminal independent PDI codes must be interpreted before contents of display memory are generated. Therefore, microprocessor is included to generate display memory code

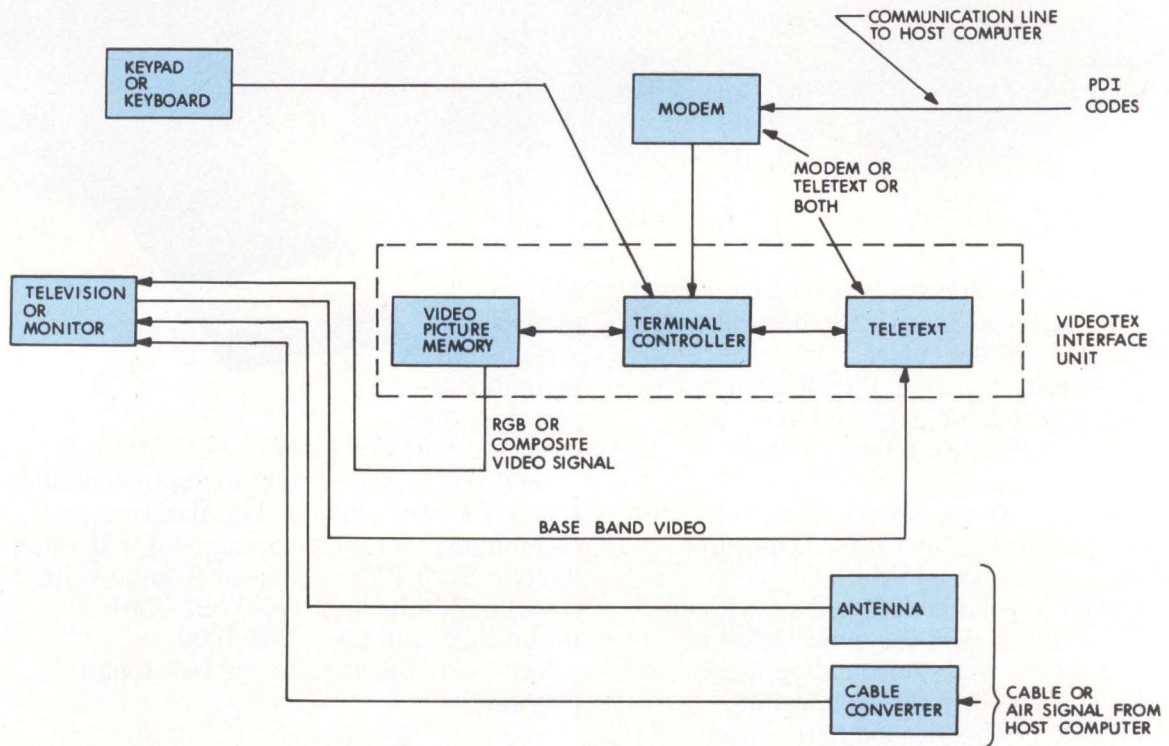


Fig 3 Block diagram of typical Telidon terminal (Norpak Ltd). PDI codes are in firmware. Facilities are provided to draw points, areas, polygons, arcs, text, and bit- or run-length encoded pictures. Data, text, and commands are embedded in 7-bit ASCII code

mand changes from graphic to text mode, and shift-out (so) back to graphics. A subset of the PDI code may be used for simple terminals which may respond only to textual information.

The Telidon terminal design has a bit-map memory for high definition graphics (Fig 2). A less costly and less functional character oriented terminal based on display memory of 800 8-bit words is also possible. A variety of terminals based on the PDI concept can be produced. Fig 3 shows one of these from Norpak Ltd, Pakenham, Ontario, Canada.

The PDI concept is applicable to already installed older type systems, and it includes extensions for future developments in an evolving service. The concept is being considered as a possible standard by the International Organization for Standardization (ISO) and by the International Telegraph and Telephone Consultative Committee (CCITT).

Future Potential

Interest in teletext and videotex systems has been growing rapidly. Prestel has successfully marketed its technology in the U.S., Germany, the Netherlands, and Switzerland. ANTIOPE has come into the U.S. with a marketing subsidiary.⁸ Systems tests have been implemented at KSL-TV, Salt Lake City⁹ and the CBS television network is conducting field tests on a teletext system at KMOX-TV, St Louis.¹⁰ In Japan, a system called "Captains," which can handle the full character set of the Japanese language, has been implemented by Nippon Telephone and Telegraph.

Full fruition of these systems depends ultimately on the growth of the marketplace for these services. Implementation of a "public" system in the U.S. is, at the moment, highly unlikely due to regulatory structures. More probable is the further development of teletext and videotex for proprietary needs within individual organizations.

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21A

National Bureau of Standards Implements Local Packet Data Network

National Bureau of Standards (NBS) computer scientists have designed and developed a new system to link computer terminals, data acquisition equipment, laboratory minicomputers, and mainframe computers at the NBS Gaithersburg, MD facility.

A study of data communications needs at the complex identified about 700 user devices, consisting of two major and some 60 smaller computers, and 300 to 500 terminals, all dissimilar units operating at different data rates. The network linking them would require the following capabilities:

- Full connectability for terminals, micro-, mini-, and major computers, and laboratory instruments

- Speed conversion over a minimum range of 110 to 9600 baud, with required flow control

- Addressing at least 2000 user nodes, a few hundred simultaneously

- Coverage of a 1.5-km long site having about 20 buildings

- Ease of user access

- Provision of data encryption, if required

- Tolerance of a large number of user interface node failures

The system developed to provide these capabilities is an adaptive time division multiple access cable system with fully-distributed control. Existing coaxial cables used as part of the NBS standard frequency distribution system form part of the network. The Table summarizes the network characteristics. Data are transmitted by packets; a typical packet is shown in Fig 1.

Heart of the system is a micro-processor based node called terminal interface equipment (TIE). These units interconnect user devices of differing signal speed requirements, and control flow of data on the network. Other features provided are error detection, automatic retransmission capability, certain line editing functions, and, with the addition of a data encryption chip, data en-

NBS Network	
Coaxial cable bit rate	1M bits/s
Signaling method	On/off, Manchester
Max packet size	136 bytes
Max packet duration	1.088 ms
Data bytes per packet	0 to 128
Number of addresses in packet	2 (destination, source)
Size of address fields	16 bit (65k addresses) One address is reserved for broadcast messages which are accepted by all TIES
Error control	16-bit error control CRC
Basic contention protocol	Ethernet
Connection to user equipment	Serial asynchronous, RS-232-C or RS-449; parallel possible
Bit rate to user equipment	Common speeds up to 9600 baud
Flow control	End-to-end, in-band or out-of-band to suit user equipment

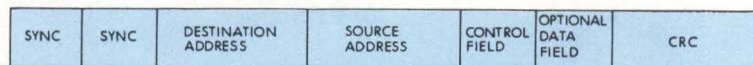
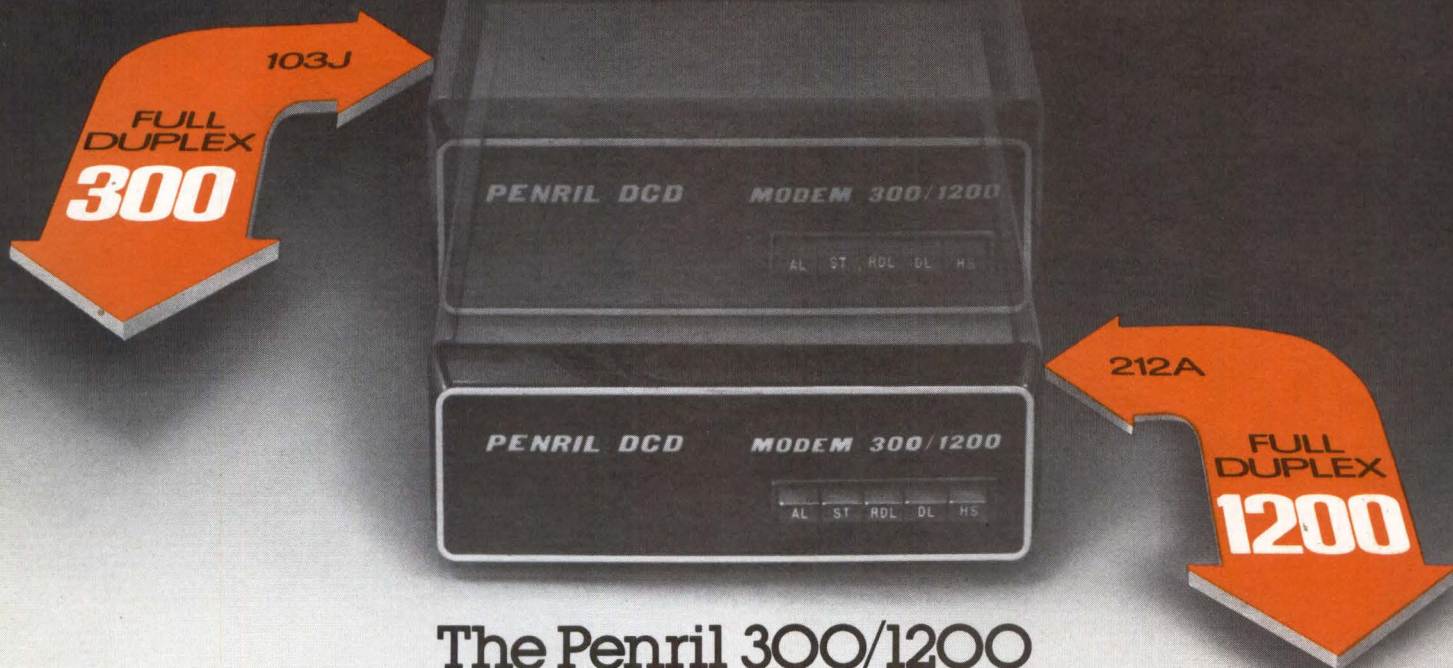


Fig 1 Typical packet structure. End to end flow control allows user stations operating with different bit rates to communicate with each other

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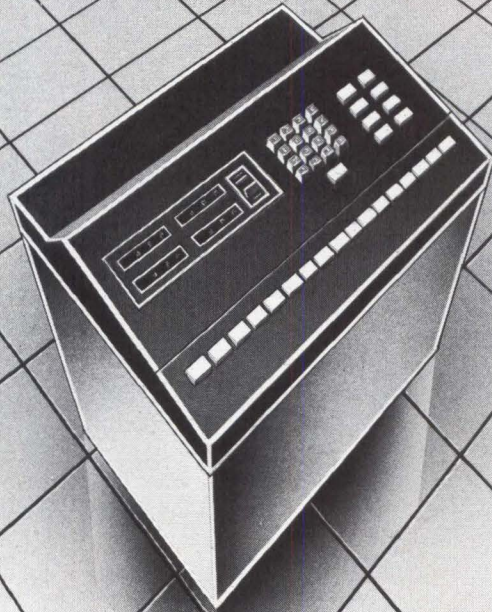
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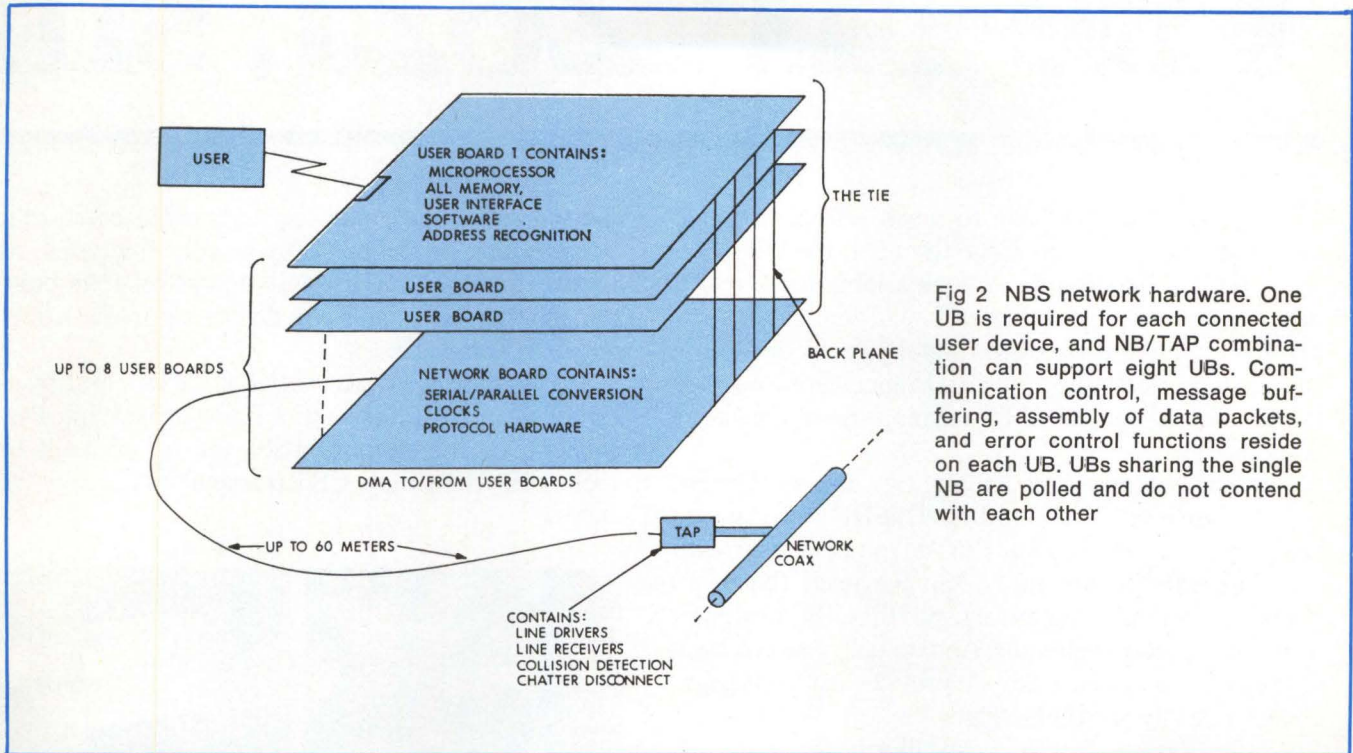


Fig 2 NBS network hardware. One UB is required for each connected user device, and NB/TAP combination can support eight UBs. Communication control, message buffering, assembly of data packets, and error control functions reside on each UB. UBs sharing the single NB are polled and do not contend with each other

ryption and decryption. The TIE is shown in Fig 2. Major sections are the network board (NB) and user board(s) (UB), managed by a microprocessor and associated erasable programmable read only memory (EPROM). Output from NB is coupled to the coaxial distribution cable by a tap.

The TIE is designed to provide efficient control of data through the network. Before transmitting, the

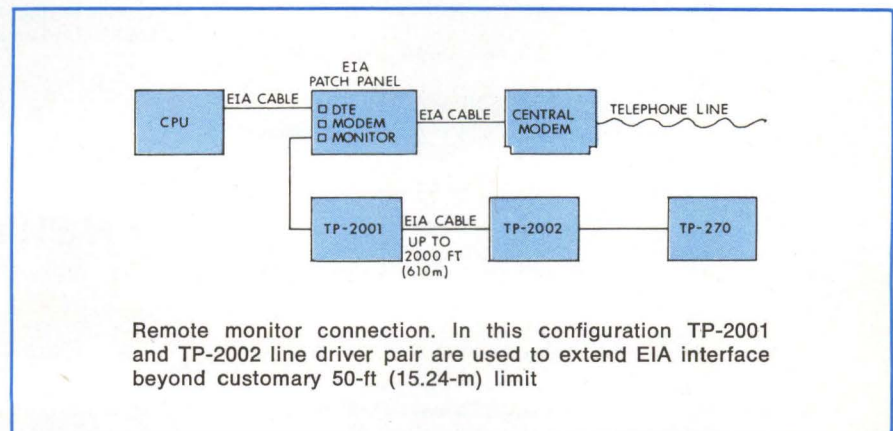
TIE checks to be sure that the cable is free. However, if two TIEs start to use the cable at the same time, each will immediately detect packet collisions. At this point, each party involved will truncate the packet being transmitted and impose a random waiting period before trying to regain control of the cable. This type of contention for the cable with detection and delay before retransmitting results in highly efficient use

of the cable channel's data transmission capacity.

User-to-user protocol is built on the user-to-TIE, TIE-to-TIE, and TIE-to-user protocols. Implementation of user-to-TIE and TIE-to-user protocol takes into account differences in the requirements of different user terminals, processors, and mainframes. Differences are recognized and the software is personalized to the local user devices.

Analyzer Measures Online Network Performance

TP-270 remote network analyzer measures system response time in a 3270 network and provides specific measurements of the effects of hardware and software changes on the system. The microprocessor based unit, located at the central computer site, can detect and measure minimum and maximum response times for each terminal location. It will display actual measurements of the elements contributing to the response times, such as poll to poll, poll to



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The HP 2621: sim

Simple doesn't have to mean unsophisticated. The proof is in our new CRT terminal, the HP 2621.

Before building it, we took a long, hard look at the way you use a simple terminal. Then we took the knowledge gained in more than 10 years designing computer products and applied it to engineering an interactive character-mode CRT terminal from the user's point of view.

The outcome was actually two models. The HP 2621A, which sells for \$1450. And the HP 2621P, which has a built-in printer, costs \$2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

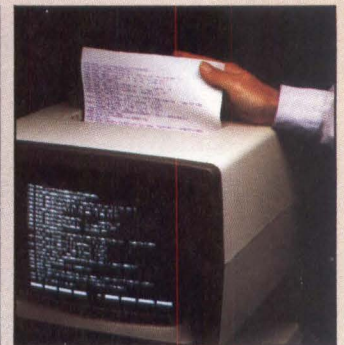
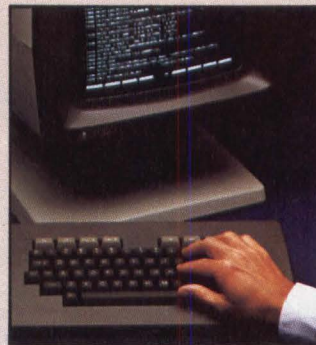
Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and

able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.



Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard. And the 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

- I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
- I'd like to see HP's new 2621A and 2621P with built-in hard copy.
- I'd like to know more about HP's complete family of terminals.

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Title _____

Company _____

Address _____

Phone _____

Mail to Hewlett-Packard, Attn: Ed Hayes,
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19400 Homestead Road, Cupertino CA 95014.

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CIRCLE 17 ON INQUIRY CARD

ple sophistication.



INTERFACE PRODUCTS from **MDB**

for Data General** or similar type computers

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- Device Controllers for most major manufacturer's
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- Communications/Terminal Modules
 - Multiple I/O board for two TTY and/or RS232 Controllers; other options include Real Time Clock and Modem Control
 - Multiplexor, four or eight channel with full modem control; 4060 compatible with additional program controlled features. Optional

multiplexor or panel provides for 25-pin connectors for each channel

- Chassis Assemblies
 - Front loading expansion chassis, six slots with 3/4" spacing
 - Terminator Modules
 - Extender Board
- Power Supplies

MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 30 days ARO or sooner.

MDB places an unconditional one year warranty on its controllers and tested products.

MDB also supplies interface modules for PDP*-11, LSI-11, IBM Series/1 and Interdata computers. Product literature kits are complete with pricing.

* TM Digital Equipment Corp.

response, and CPU wait times, as well as the duration of inquiry and response messages. Event counts, such as ACKS, NAKS, WACKS, and messages are displayed to show direction of origin. The TP-270 is available from TeleProcessing Products, Inc, 4565 E Industrial St, Bldg 7K, Simi Valley, CA 93603.

While not intended as a diagnostic tool, the unit provides the sophisticated user with inferences which are an aid in network trouble shooting. When equipped with an optional printer interface card, a hardcopy printout of individual functions or a complete status report will be produced on a user-provided printer.

The TP-270 will handle synchronous data rates up to 9600 bits/s. Codes are switch-selectable, ASCII or EBCDIC. Size is 5.25 x 17 x 11.5" (13.3 x 43 x 29.2 cm), weight, 13 lbs (5.85 kg). Power requirement is 115 Vac, 60 Hz, 1 A.

Circle 400 on Inquiry Card

Intelligent Processor Improves Computer Communications

An intelligent network processor (INP) relieves CPU congestion, enables computer to computer communications at speeds to 56k bits/s, and improves distributed systems network (DSN) operations as well as remote job entry functions via 2780 links. The INP was recently introduced by Hewlett-Packard General Systems Div, 19447 Pruneridge Ave, Cupertino, CA 95014.

The INP is applicable to all HP 3000 computer systems. It uses a proprietary silicon on sapphire (SOS) microprocessor and 32k bytes of on-board RAM to relieve the CPU of communications management tasks such as character handling and buffer storage. The processor uses IBM binary synchronous communications protocol, and is compatible with HP 32210T, 37220T, and Bell 201, 208, and 209 modems.

Interface is EIA RS-232-C, CCITT V24/28, V.35, or hardwired. Data rates are 19.2k bits/s using modem, half or full duplex, or to 56k bits/s with V.35 or a hardwired link. Data buffer capacity is as much as 2k bytes/buffer; buffered data are protected in case of power failure. Self-test capability and a comprehensive diagnostic program for troubleshooting are included.

Circle 401 on Inquiry Card

**Data General is a computer manufacturer unrelated to MDB.

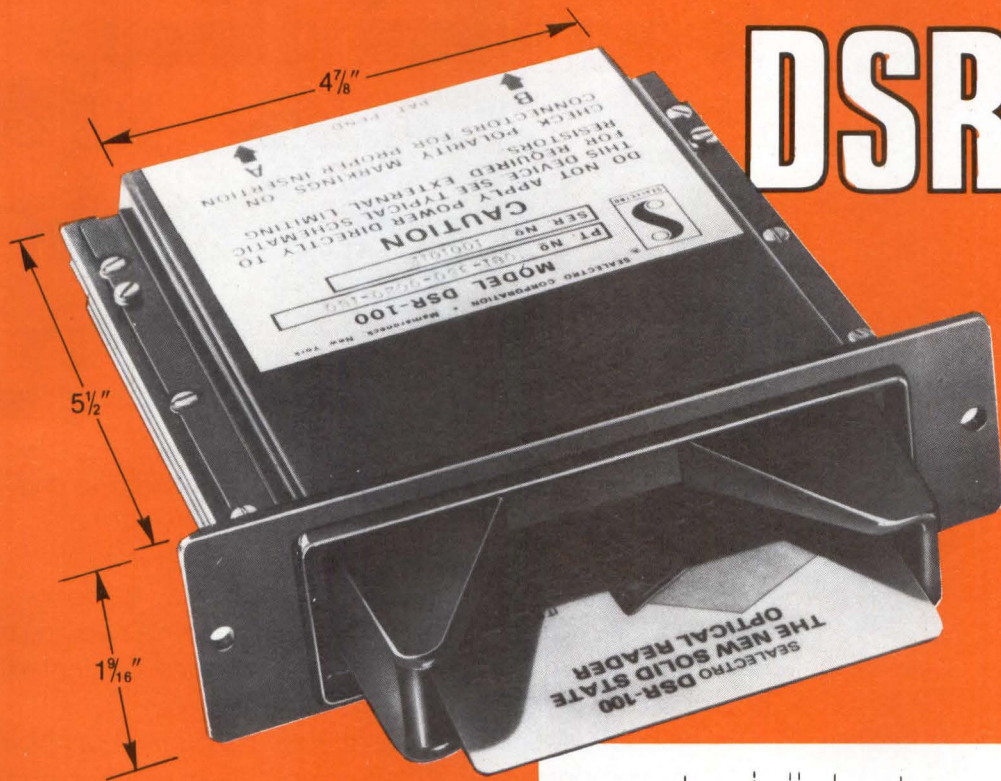
MDB 1995 N. Batavia Street
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SYSTEMS INC. TWX: 910-593-1339

Circle 168 for DG; 169 for PDP; 170 for LSI; 171 for IBM; 172 for Interdata

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EVERYONE AGREES... IT'S THE**

DSR-100

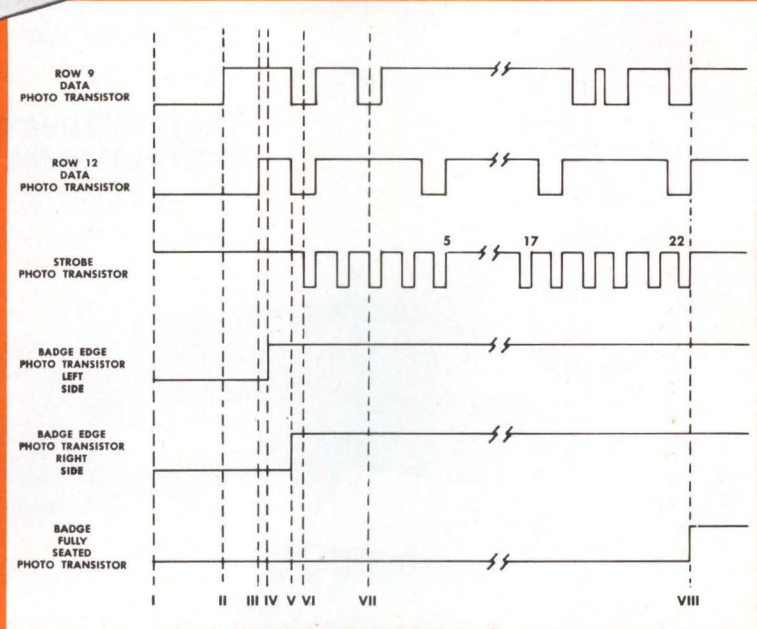
BADGE READER



- ★ Completely solid state—maximum reliability and long-life.
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- ★ Reads complete alpha-numeric code.
- ★ Complete validity check.
- ★ Absolute column count—regardless of punched data.
- ★ Low cost, small size.

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F6800 SERIES

We've just added two hard-hitting rookies to our winning lineup.



Now that the new F6802 microprocessor and F6846 combo chip have joined Fairchild's F6800 team, you've got a minimum, microprocessor-based-system solution to your design problems. One that's low cost and easy to work with too. Like the rest of our F6800 family, these two great new NMOS products are made using Fairchild's patented Isoplanar™ process.

The F6802 and F6846 are already becoming big hits in the microcomputer field. When you put them on your team, they're bound to score some winning runs for you.

The F6802 microprocessor. It sends your design problems to the minors.

And that's where they'll stay, thanks to this enhanced version of the F6800 central processing unit. The F6802

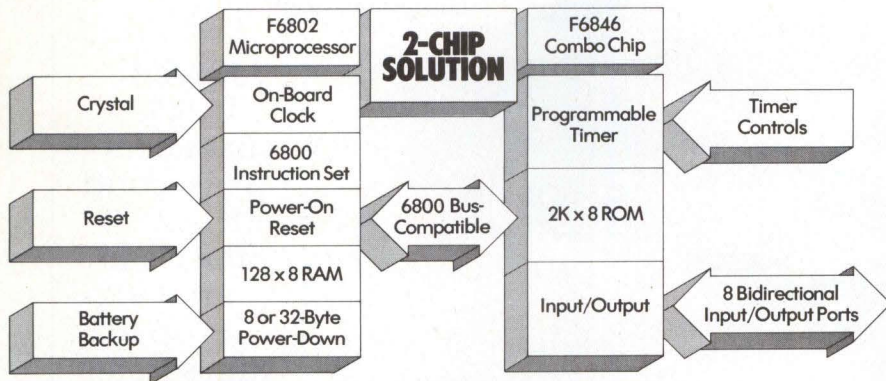
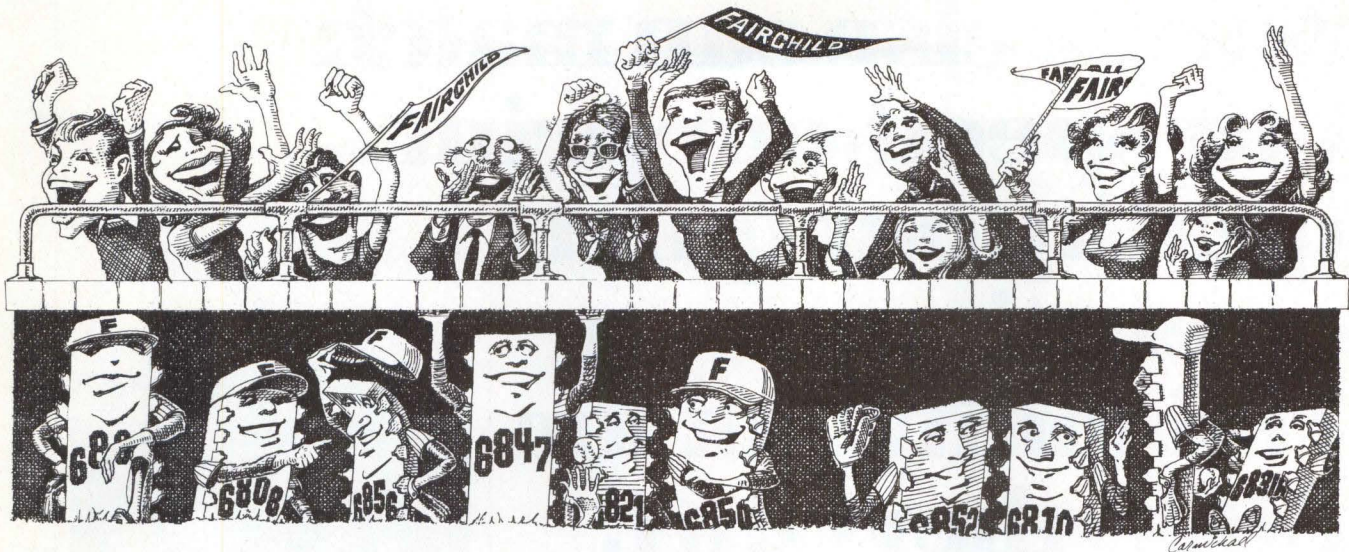
offers an on-chip power-on reset function, on-board clock for easier use and on-board 128 x 8 RAM with options of 8-byte or 32-byte power-down. Now you no longer need an additional RAM with battery backup systems.

The F6802 features a memory-ready line for slow or fast memory. So you can use memories in synchronous or asynchronous mode. And the F6802 is bus-compatible for easy use with all of the other F6800 peripherals.

The F6846 combo chip. It's a memorable teammate.

The F6846 is a user-defined ROM-based peripheral element. It features 2K x 8 ROM, a powerful programmable binary timer, and eight bidirectional input/output ports on the same circuit. It's also F6800 series bus-compatible.





We're a major-league supplier.

Some of the biggest OEM customers come to us. Including names like General Motors, Ford, H.P. and Lear-Siegler, to mention a few. They know we're one of the biggest suppliers and one of the best sources for F6800 microcomputer products in the industry. We offer the entire F6800 family, including peripherals, memory and communication circuits. And we can get them to you when you need them because we're in high-volume production. We also have some great new circuits coming up soon from training camp — the F6856 SPCC, F6808 CPU, F6847 VDG controller and F6801 single chip.

We support your team.

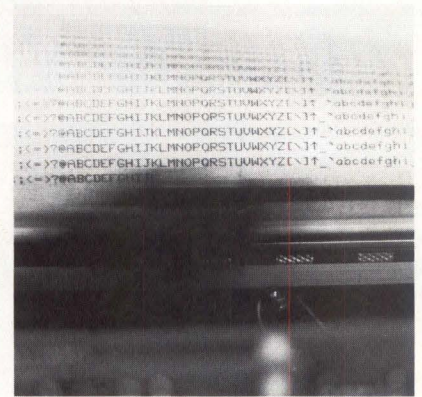
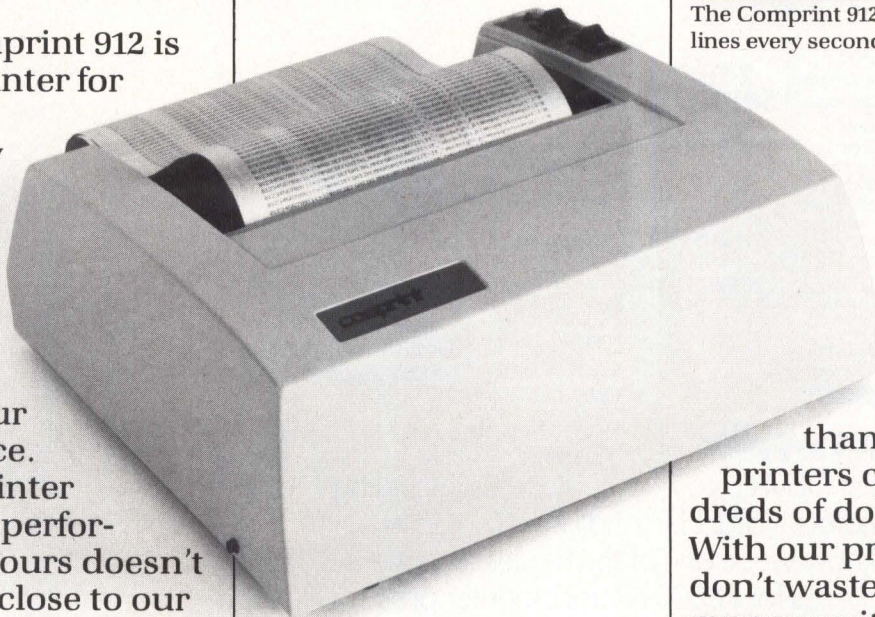
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When you need some heavy-hitting microprocessor circuits for your team, give us a call and we'll hit you with our winning lineup. Just ask for our Microprocessor Group at (408) 224-7000. Or write Fairchild Camera and Instrument Corporation, P.O. Box 880A, Mountain View, California 94042. TWX: 910-379-1227.

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The Comprint 912 printer. No one else can match our speed, our print quality, our quiet operation, or our reliability. Not for \$660 they can't.

Our Comprint 912 is the best printer for the money. Period. Any printer that can match our price can't even begin to match our performance. And any printer that boasts performance like ours doesn't even come close to our price. No matter what your application; computer reports, listings, CRT hard copy, message



The Comprint 912 prints nearly 3 lines every second.

Speed.
At 225 characters per second (170 LPM) the Comprint 912 is up to 4 times faster

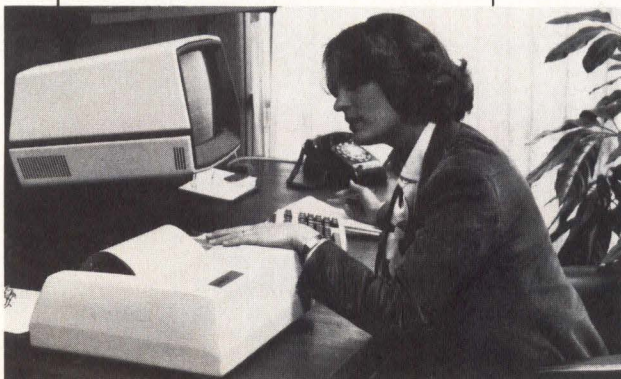
than impact printers costing hundreds of dollars more. With our printer you don't waste time and money waiting for your print-out.

Print Quality.

Our 9x12 matrix provides sharp, crisp characters. Compare that with our competition. Their very best is a 9x7 matrix, which means no lower case descenders and cramped letters. With the Comprint 912 you don't have to put up with the irritation of fuzzy, hard to read computer printing. This

receiving, scientific/ industrial data logging, or anything you can think of, the Comprint 912 is **the** performance leader in printers under \$1000.

First consider our performance.



CRT hardcopy is an excellent application for the Comprint 912.

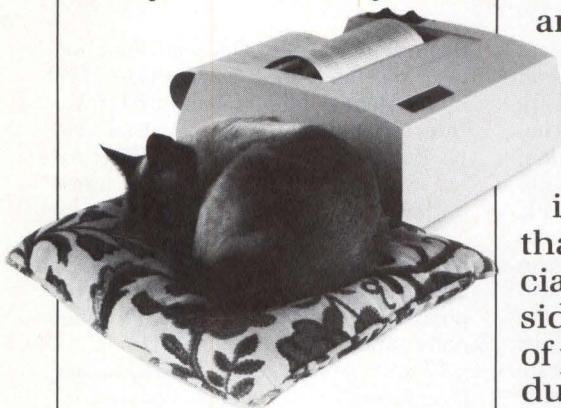
exceptional print quality in
ly by the Comprint 912 in 7
nless reliability, 6 month
parallel I/O and 8 1/2" wide
been shipped to happy custo

The superior print quality provided by the Comprint 912 is obvious in this actual size sample.

means increased productivity. And because the Comprint 912 makes better originals, our originals make better Xeroxes.

Quiet Operation.

Most computer printers are irritatingly noisy. They can disrupt concentration and reduce the efficiency of anyone working near them. They're noisy because they're



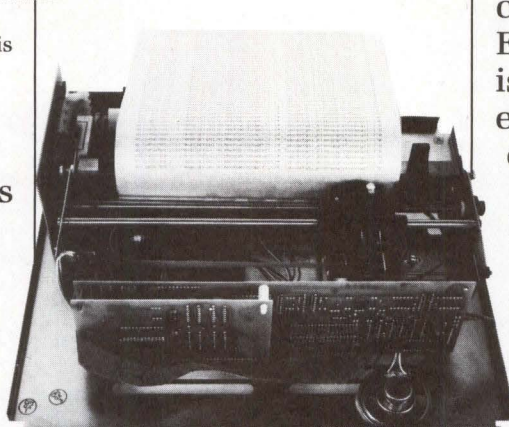
The Comprint 912 is quiet because it's electronic not mechanical.

impact. The Comprint 912 has no mechanical print head banging on the paper. It's electronic. It's quiet.

Reliability.

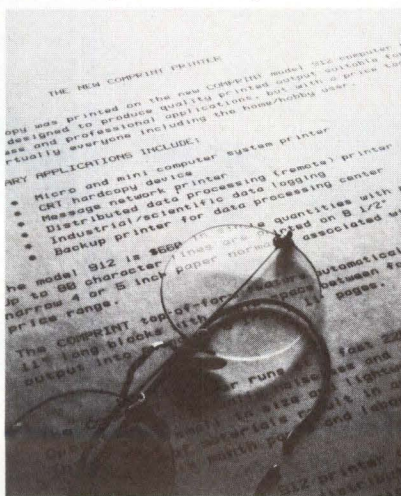
Since the Comprint 912 prints electronically, rather than mechanically like ordinary impact printers, we have fewer moving parts and less vibration. The Comprint 912 has fewer things to go wrong and less wear. That's why we

offer a 6 month warranty, twice the industry standard. The key to all this superior performance is our special



Fewer moving parts in the Comprint 912 mean greater reliability.

paper. This aluminized "silver paper" works just like ordinary paper. It won't fade or discolor and actually costs less than plain paper and one time ribbons. For the vast majority of printing applications it's just plain better than plain paper. Especially when you consider the hidden costs of plain paper printers due to their inferior performance compared to the Comprint 912. And on those rare occasions when you really do



need a plain bond paper copy, just run your Comprint 912 printout through your plain bond copy machine and you've got it. Even though our paper is special, it's available everywhere; from your dealer or distributor, or from us. Now consider our price.

The Comprint 912.

\$660 with parallel interface, \$699 with serial interface.

We could talk about our other advantages, like our 80-character lines on 8-1/2" wide paper, or our compact, light-weight size, and the fact that the Comprint 912 has no ribbons to mess with, no chemicals, nothing to add but paper.

But you have to see for yourself. Before you buy any printer, insist on seeing the Comprint 912, the performance leader, at your local computer store or industrial distributor. Or contact us for a descriptive brochure, a sample print-out, and applications literature.

comprint

The performance leader.

Computer Printers International, Inc.
340 E. Middlefield Rd.
Mountain View, California 94043
415 969-6161

Work Station Incorporates IATA Protocol

Basic software package of the 2001 work station now incorporates the 83B3 communications protocol, allowing operation in this communications medium because it takes into account special International Air Transport Association (IATA) format and specific communications restrictions. The work station combines an 83B3 communications terminal and

a complete word processing system. The 2001 is manufactured by Megadata Corp, 35 Orville Dr, Bohemia, NY 11716.

Word processing and communications functions occur simultaneously. Total number of messages in line queue can amount to about 245k characters. The system comprises a 64k RAM, dual floppy discs, a letter quality printer for word processing, and a separate printer for incoming and outgoing messages.

A file of "canned" phrases allows 1-time entry of commonly used text, with a 6-char code used to call up the phrases. IATA forms control is included to perform complete check of outgoing messages and insure validity of header information. Communications are fully supported with all output messages queued up on a disc. Automatic header checking, message blocking, and reject message handling are included.

Circle 402 on Inquiry Card

Fiber Optic Data Link Operates to 250k Bits/s

High sensitivity, medium speed 3713 data link is designed to provide signal isolation in electrically noisy environments, and is compatible with many process and control configurations. Made up of the 3713T transmitter and 3713R receiver connected by a suitable fiber optic cable, the 3713 provides a 250k-baud NRZ data link capable of operation to 1.7 km. An AMP Optimate single-fiber connector system simplifies interfacing

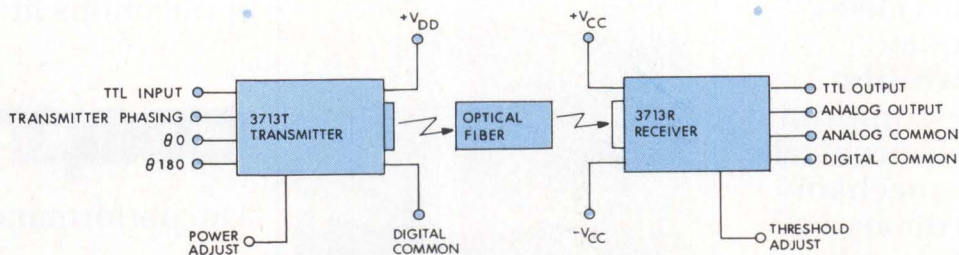
modules and fiber and minimizes problems of source/fiber/detector alignment. Metal packages of both transmitter and receiver provide immunity to electromagnetic radiation, and direct PC board mounting without need of an additional heat sink.

The integral connector system also permits choice of a variety of cables to match specific needs, with maximum cable length depending on the type of fiber optic cable used. Units operate with 10^{-9} bit error rate (BER) and 20-dB aggregate cable and connector loss when used with a 200- μ m fiber. When low loss silica

fiber is used, the link can function over distances to 2.5 km. The 3713 link system is offered by Burr-Brown, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85374.

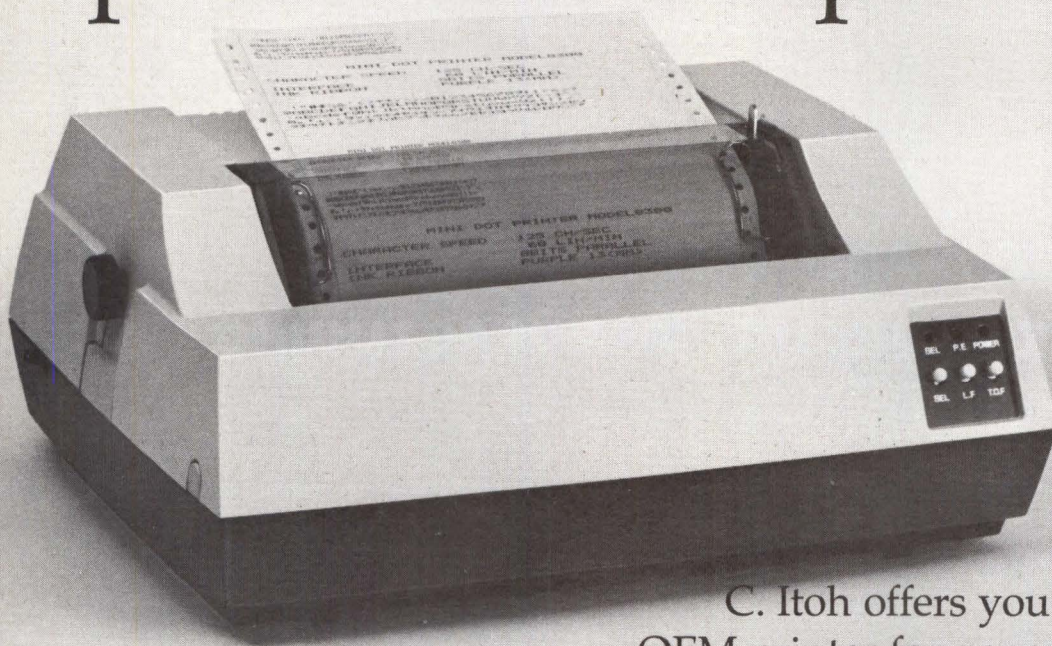
Power requirement for the transmitter is 5 V; optical power may be adjusted with a single resistor. The receiver takes a ± 15 -V supply. An automatic threshold circuit is incorporated in the receiver for maximum noise immunity. Package size is 41 x 77 x 16 mm. Direct PC board mount is enabled by seven pins located on the bottom of each unit.

Circle 403 on Inquiry Card



3713 fiber optic data link. Transmitter converts TTL level inputs to optical pulses via LED light source at data rates from dc to 2M baud NRZ. Receiver converts light input via PIN photodiode to TTL output, with receiver sensitivity of 15 nW and data rates to 250k baud NRZ

C. Itoh's Model 8300 printer looks superb.



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C. Itoh offers you the perfect OEM printer for general purpose computers, communication terminals, data loggers and micro computers: the Model 8300. This quiet and low-cost unit features a straightforward, reliable design and a continuous-duty 7-wire head with a life expectancy of 100 million characters. Designed with a 7-bit parallel interface, the 80-column, dot matrix Model 8300 prints bi-directionally at 125 CPS. Its sprocket paper feed mechanism accepts multi-pin-feed paper in any width from 4.5" to 9.5"; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 8300 works even better than it looks.

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CIRCLE 73 ON INQUIRY CARD

TECHNOLOGY AND ECONOMICS: INTEGRATED CIRCUIT MANUFACTURING COSTS

Montgomery Phister, Jr

Systems Consulting
Santa Monica, California

When engineers were designing the first commercial digital computers, a system flipflop occupied one-third of a cubic foot and cost over \$100 (see Table 12, p 117 of *Computer Design*, Oct 1978). Designers therefore were interested in logic minimization, and devoted time and effort to finding structures which shared registers and eliminated superfluous gates.

Today a system flipflop costs 80¢ and occupies 2 in³ (33 cm³) of cabinet volume. The integrated circuit, unimaginable by early computer engineers who struggled with vacuum tubes and dreamed of transistors, has turned the designer's world upside down. He is still interested in elegant structures, but his bricks are ALUS,

decoders, P/ROMS, and microprocessors rather than gates and flipflops. Furthermore, because the lion's share of a system's cost is in its components, he has an abiding interest in IC prices and price trends.

Prices in a free market are of course complicated entities. They depend on the price of functionally equivalent, existing alternative parts. They depend on the demand from the marketplace, and on the supply of parts available. But ultimately they are limited by the manufacturing cost of the parts. Design engineers interested in prices and price trends therefore must have some understanding of the factors which influence IC manufacturing cost.

NEC Spinwriters. Tailored printers.

**Printers for every job.
Terminals for every line.**

NEC Spinwriter™ character printers and terminals can be configured in as many varieties as there are jobs to do.

They start as basic 55-cps printer mechanisms for some OEM buyers who want to add their own value. Then they grow and change to fit your precise letter-quality output needs.

Each of our 10 models is surrounded with features and options that make customizing easy.

Eight industry-standard interfaces, serial and parallel,

let you add Spinwriter printers quickly to your current system. Ten form-feed options—most operator changeable—provide unparalleled document handling flexibility. Dozens of 10 or 12 pitch and Proportional Space thimbles—with up to 128 characters—solve your technical and language output requirements.

That's not all. Spinwriter printers and terminals lead the industry in reliability, with a more than 2000-hour MTBF. And in serviceability, with a 30-minute MTTR.

When you want hard-working printers that are tailored to your individual needs, call the NEC Spinwriter regional representative nearest you. He'll assure a perfect fit.

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the perfect printer.**



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NEC Information Systems, Inc.

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Western Region: 8939 S. Sepulveda Blvd., Los Angeles, CA 90045, (213) 670-7346
Southern Region: 2965 Flowers Rd., South, Atlanta, GA 30341, (404) 458-7014

CIRCLE 23 ON INQUIRY CARD

The more you demand the more you should

Chances are, you'll find that the performance you need is already there.

At HP, our long experience in developing instruments for engineering and manufacturing has given us a real good idea of what's needed in computer systems for technical applications. That's why Hewlett-Packard's family of computer products can meet your needs so closely in the lab or on the factory floor.

Matching the computer to the job.

Take our 9800 Series Desktop computers. For single-station interactive computing, they're in a class by themselves. With up to 449K bytes of memory, enhanced BASIC, graphics capabilities, and a built-in keyboard and display, you get the power of a minicomputer in one complete, integrated package. And there's easy interfacing with HP instruments and peripherals for jobs like control and testing, statistical analysis, and even engineering design.

For more complex multi-processing tasks, the HP 1000 computer has the power and flexibility to meet your needs. You can choose from a broad range of computation power to process your data, from the low-cost M-Series to the high-speed floating point F-Series. All of the configurations use upward-compatible RTE operating systems, so you don't have to rewrite your programs when you change

jobs or move up to another model. And if you need additional storage, you can expand the systems to two megabytes of main memory starting at only \$18K/per megabyte.

The HP 1000 system also comes with a number of applications tools to minimize your programming costs. HP's new DATACAP/1000 software, for example, lets you design a real-time factory data collection system according to your shop floor needs. And to help you manage vast quantities of technical data, we developed our powerful IMAGE/1000 data base management system. Just a few simple keystrokes give you up-to-the-minute information on inventory levels or instrument check-out status. If you'd like a really clear picture of your information, HP's GRAPHICS/1000 will plot your data in a way you can understand.



nd from a computer, ould look at HP.

Communication made simple.

General purpose interface cards let you adapt the HP 1000 to a variety of tasks, including A/D conversion and multi-point communications. What's more, with the plug-in HP-IB (interface bus), you can process and control data from over 200 sophisticated measurement and testing instruments.

Talking to the computers is easy, too. The HP 1000 uses BASIC and FORTRAN as well as assembly and micro-code languages. And our powerful communications software, DS/1000, lets you hook HP 1000 computers together in any network configuration you want—across your plant or around the world.

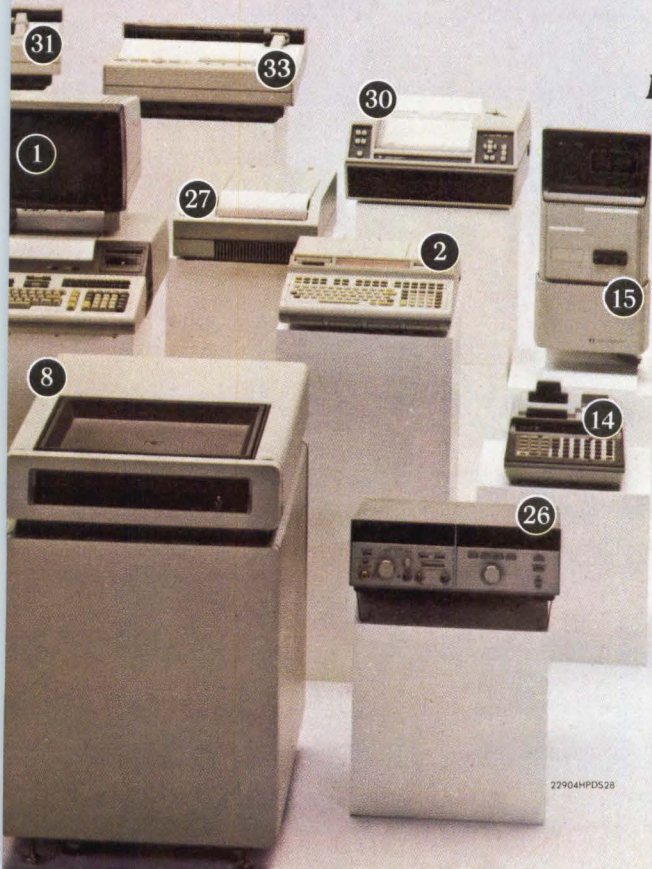
A continuous growth plan.

HP's family of computer products is constantly growing to meet your scientific, engineering, and manufacturing needs. Whether it's instrumentation front ends, CRT terminals, plotters or digitizers, HP's compatible products let you add to your system at any time without writing new software. And of course, you get HP's full support, service, training and documentation.

Go ahead and ask your own computer some tough questions. Then ask ours and see the difference. For a hands-on demonstration of the HP 1000, just call your nearest HP sales office listed in the White Pages. Or for more information write Hewlett-Packard, Attn: Roger Ueltzen, Dept. 1259, 11000 Wolfe Road, Cupertino, CA 95014.

Here are just a few of HP's range of products for manufacturers and engineers:

1. HP 9845 Desktop Computer.
2. HP 9825 Desktop Computer.
3. HP 1000 Model 45 Real-time System with HP 7906 Disc Drive and HP 2648A Graphics Terminal.
- 4-6. HP 1000 F-, E-, and M-Series Computers.
7. HP 2108 Board Computer.
8. HP 7925 Mass Storage Unit.
9. HP 2240 Measurement & Control Processor.
10. HP ATS Automatic Test System.
11. HP 12050 Fiber Optics.
12. HP-IB Link IEEE-488 Standard Interface.
13. HP 2621 CRT Terminal.
14. HP 3075 Data Capture Terminal.
15. HP 3077 Time Reporting Terminal.
16. HP 3455 Voltmeter.
17. HP 3495 Scanner.
18. HP 5328A Universal Counter.
19. HP 5342 Microwave Frequency Counter.
20. HP 436A Power Meter.
21. HP 4262 LCR Meter.
22. HP 8566A Spectrum Analyzer.
23. HP 8754A Network Analyzer.
24. HP 3325A Synthesizer/Function Generator.
- 25-6. HP 8660A & HP 8672A Synthesizer/Signal Generators.
- 27-8. HP 9876A & HP 2608A Printers.
29. HP 2635 Printer.
30. HP 7245A Thermal Plotter/Printer.
31. HP 7221A Plotter.
32. HP 7225A Graphics Plotter.
33. HP 9872A Programmable Graphics Plotter.
34. HP 9874A Digitizer.
35. HP keeps it coming.



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CIRCLE 24 ON INQUIRY CARD



IC Manufacturing Process

Briefly, IC manufacture begins with a sequence of alternating optical and chemical steps carried out on a thin wafer of silicon.¹ The optical operation transfers circuit patterns from a set of masks to the wafer, and the chemical (or physical/chemical) processes create appropriate conducting, semiconducting, and insulating paths in the silicon locations specified by the masks. The masks typically contain patterns for tens or hundreds of identical circuit components, or chips (the actual number depends on wafer and chip dimensions). When the manufacturer finishes the processing steps on a batch of wafers, he tests the individual chips and marks the bad ones. The ratio of good chips to total chips on the wafer is called the *wafer yield*, and is a most important parameter.

Next, the manufacturer separates the chips, discarding the bad ones. He mounts each good chip on a package "header," and bonds it in place. Then he attaches the chip terminals to the package leads, and inspects the result. The ratio of good circuits to total circuits at this point is the *packaging yield*.

The last steps in the manufacturing process call for the mounted chips to be capped and marked, and to undergo a final test, which cycles the finished product

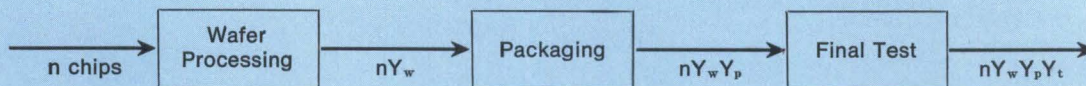
through a sophisticated test appropriate to its complexity. The ratio of good units to total units here is the *final test yield*.

Cost Influencing Factors

"A Model for Integrated Circuit Manufacturing Costs" provides a simplified model^{2,3,4,5} for this entire process. Total cost is the sum of processing, packaging, and testing costs. The latter two costs are assumed constant, and dominate manufacturing cost for small chips. As chip size increases, however, both wafer yield and the number of chips per wafer fall, and the first term, processing cost, becomes dominant. Fig 1 shows how wafer yield varies with chip area, and Fig 2 illustrates how the number of chips per wafer varies, for two common wafer sizes. [The 3-in (7.6-cm) wafer is the most widely used in the U.S. today, but it is being superseded by the larger wafer.]

The resulting chip manufacturing cost is shown in Fig 3. To put things in perspective, note that Intel's 16k dynamic RAM, the 2116, has an area of 0.034 in² (0.219 cm²), and IBM has announced that their 64k RAM has an area of 0.0625 in² (0.403 cm²). The model predicts that the former would have a manufacturing cost of about \$1.50, and that the latter would cost about

A Model for Integrated Circuit Manufacturing Costs



IC Manufacturing Cost/Chip = Processing Cost + Packaging Cost + Final Test Cost

$$\begin{aligned} \text{Processing Cost} &= \frac{\text{Cost of Processed Wafer}}{(\text{Chips/Wafer}) \times (\text{Wafer Yield}) \times (\text{Packaging Yield}) \times (\text{Test Yield})} \\ &= \frac{C_w}{\left[\frac{\pi D^2}{4e^2} - \frac{1.77D}{e} \right] \times \left[\frac{0.8}{(1 + ke^{2A})^3} \right] \times Y_p Y_t} \end{aligned}$$

where

D = Wafer Diameter (inches)

e = Edge of square chip (inches)

k = Silicon wafer defect density

$$\begin{aligned} \text{Packaging Cost} &= \frac{(\text{Cost of IC Package}) + (\text{Cost of IC Connections})}{(\text{Packaging Yield}) \times (\text{Test Yield})} \\ &= \frac{P + C}{Y_p Y_t} \end{aligned}$$

$$\text{Final Test Cost} = \frac{\text{Cost of Testing Finished IC}}{\text{Test Yield}} = \frac{T}{Y_t}$$

$$\text{IC Manufacturing Cost/Chip} = \frac{A(1+kA)^3 C_w}{0.8 Y_p Y_t (\pi D^2/4 - 1.77D\sqrt{A})} + \frac{1}{Y_t} \left[\frac{P + C}{Y_p} + T \right]$$

where

A = e² = Chip Area

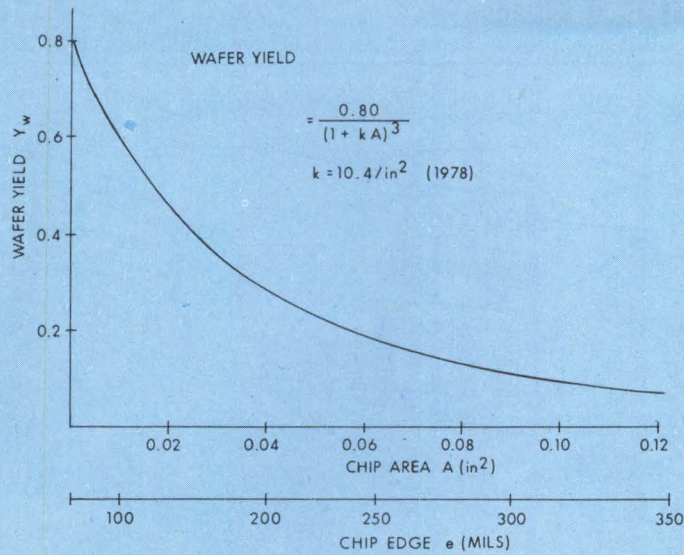


Fig 1 Wafer yield vs chip area. Wafer yield is ratio of good chips, at point where wafer processing is complete, to total number of chips on wafer. Bad parts typically result from defects in wafer or aberrations in optical system. Yield falls off rapidly with increasing area

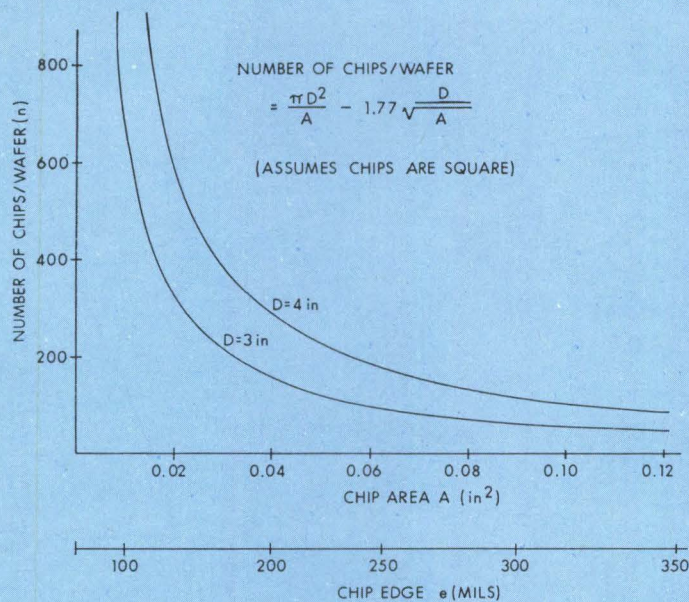


Fig 2 Chips/wafer vs chip area. Number of rectangular chips which can be laid out on circular wafer is function of wafer and chip dimensions. Formula shown is fairly accurate for square chips

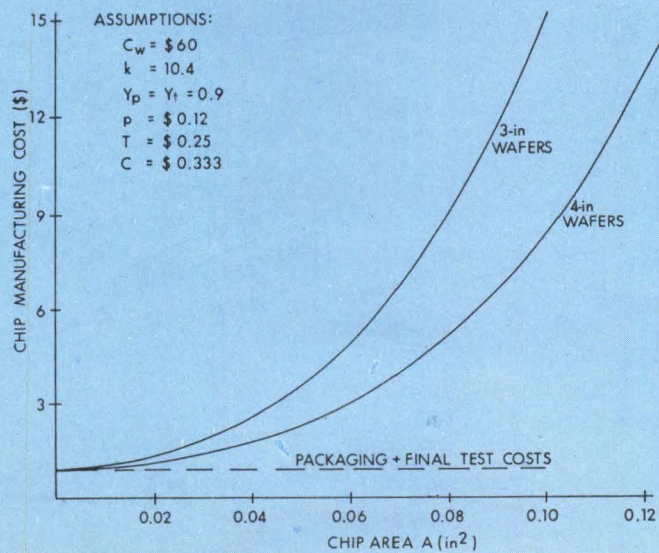
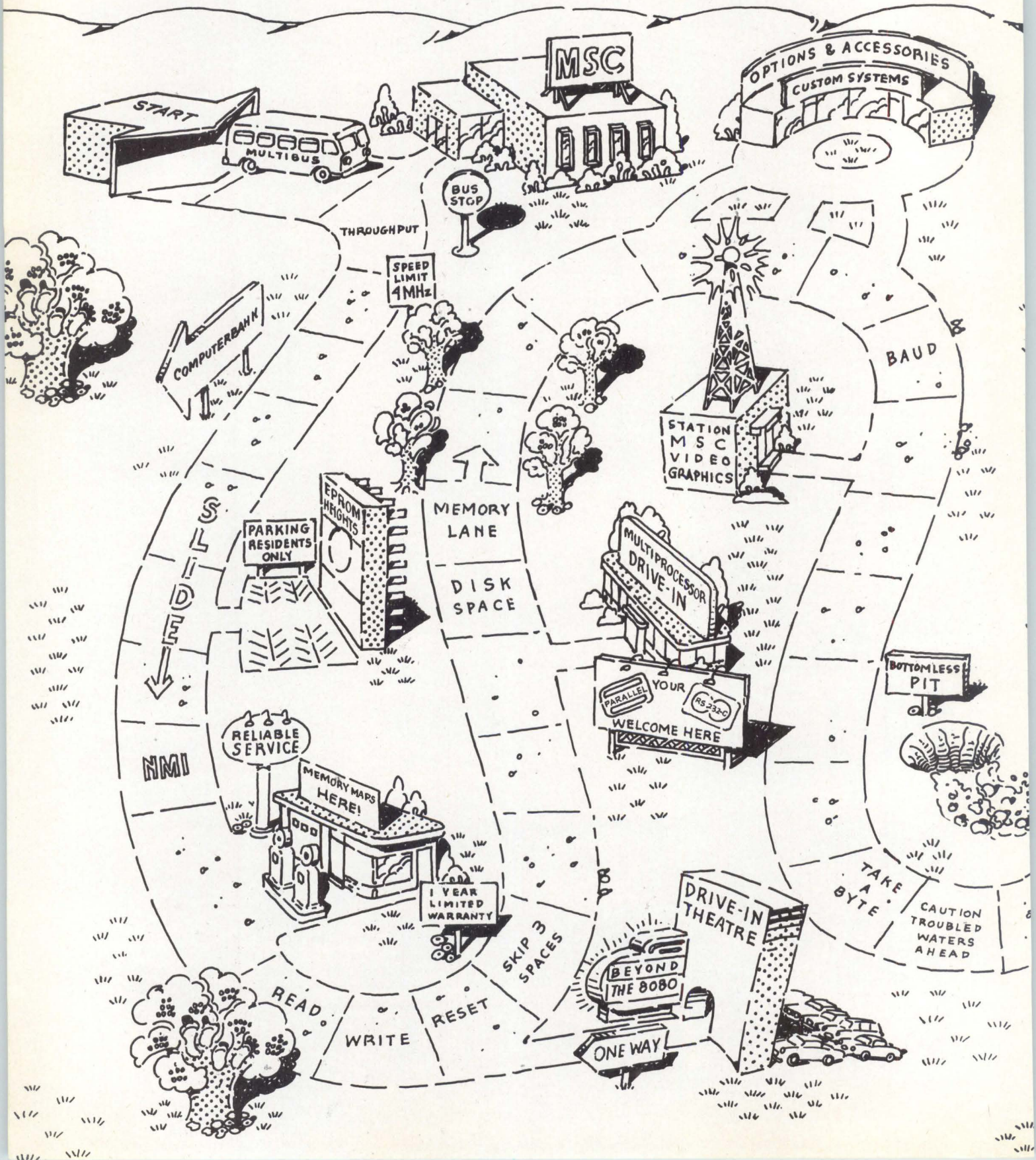
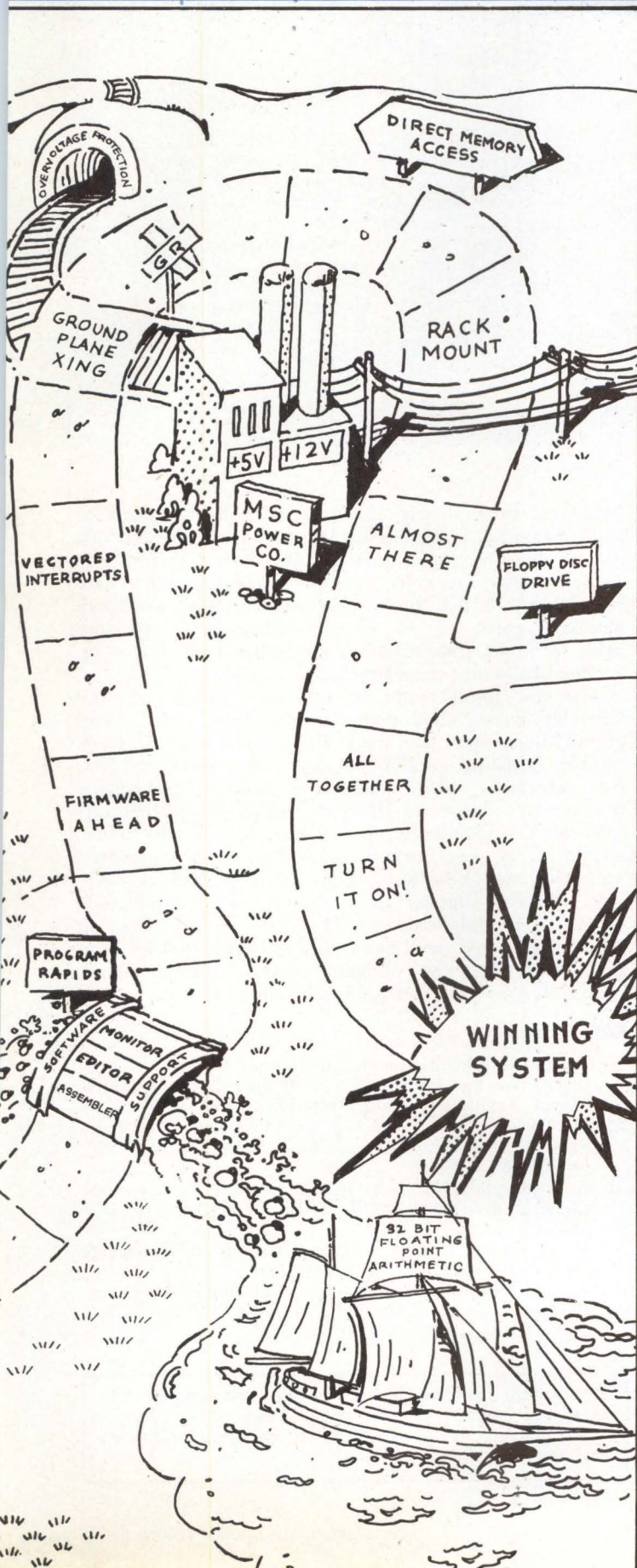


Fig 3 Chip manufacturing cost vs chip area. "Model for Integrated Circuit Manufacturing Costs" predicts that total manufacturing cost is sum of fixed packaging-plus-test cost and processing cost which increases sharply with area. IC prices are typically two to four times manufacturing costs

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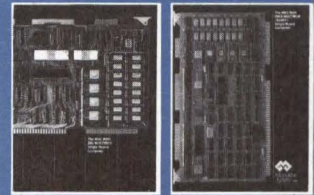
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CIRCLE 25 FOR LITERATURE
CIRCLE 189 FOR QUOTATION

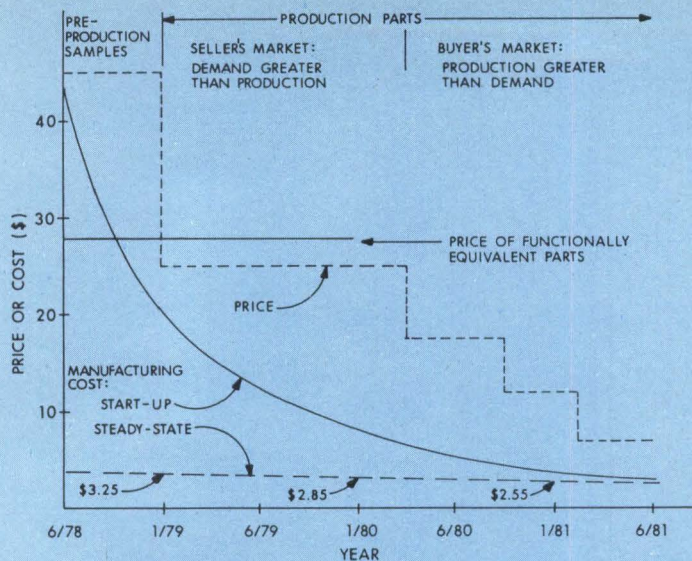


Fig 4 Cost/price history of 0.0625-in² chip on 4-in wafer. In idealized picture, manufacturing cost (solid line) starts much higher than that predicted by model (dashed line), and drops as manufacturing problems are identified and solved. Steady state, model predicted price falls slowly as defect density k drops. Selling price (dotted line) depends on market conditions

\$3.25. The equation and graphs show very clearly that cost increases faster-than-linearly with area—for large enough areas, cost increases with the *cube* of area, other things being equal. If we were to modify the model to accommodate the fact that packaging and test costs also increase with chip area to some extent, the increase would be even greater.

The model predicts steady-state manufacturing cost in some given year. As time passes and technology improves, defect density k drops, wafer yield increases, and cost falls off somewhat. But more important, from the equipment designer's point of view, are the manufacturer's start-up problems. When an ic first enters manufacturing, its cost is far higher than that predicted by the model. Typically all yields are lower than their steady-state values, and wafer, connection, and test costs may be higher than standard while the plant learns how to make the part. Wafer yield in particular may be slow to reach its predicted value, and manufacturing may have to make changes in masks and/or in process chemistry and physics to solve the yield problems.

Actual manufacturing cost for a 0.0625-in² (0.403-cm²) chip may thus follow a curve like the solid line in Fig 4, and prices might change as shown by the dotted line. During the first six months, manufacturing costs are very high, yields are low (perhaps 2% or less), parts correspondingly scarce, and production samples are available at a premium price. After this six month period, wafer and other yields have improved somewhat, and there are enough wafers in process for the manufacturer to supply parts in quantity. He then lowers the price to the point where the part will be attractive in comparison to functionally equivalent parts. His yields, however, though improving, are still low, keeping parts in relatively short supply compared with the demand. During the next months there is thus a sellers' market and the price holds steady.

Ultimately yield increases further, alleviating the part shortage. In addition, the success of the ic attracts competitors, and their yields increase to the point that production capacity exceeds demand. Users can get parts from any of several vendors, and make a choice

based on price. There thus ensues a buyers' market, and prices fall with increasing frequency. Meanwhile the steady-state manufacturing cost (dashed line in Fig 4) falls slowly as defect density improves, and actual costs approach that limit. However, to cover overhead and sales costs, and to recover development costs and make a profit, the manufacturer must hold prices at a value two to four times his costs.

The cost trend might be somewhat better, or considerably worse, than that shown in Fig 4. It is not at all uncommon to read that manufacturers have trouble initiating production on a new and complex part, especially when some new facet of technology is being introduced. In this case, yields may stubbornly hold at disappointingly low values for months while engineers try new circuits, new masks, new process variations, and new tests. The supply of parts is very low, and the supplier loses money even at premium prices. Meanwhile, users must scramble for parts, or must employ old and more expensive technology. For this reason the wise designer is very cautious about introducing new components into his designs.

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The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—Ed.

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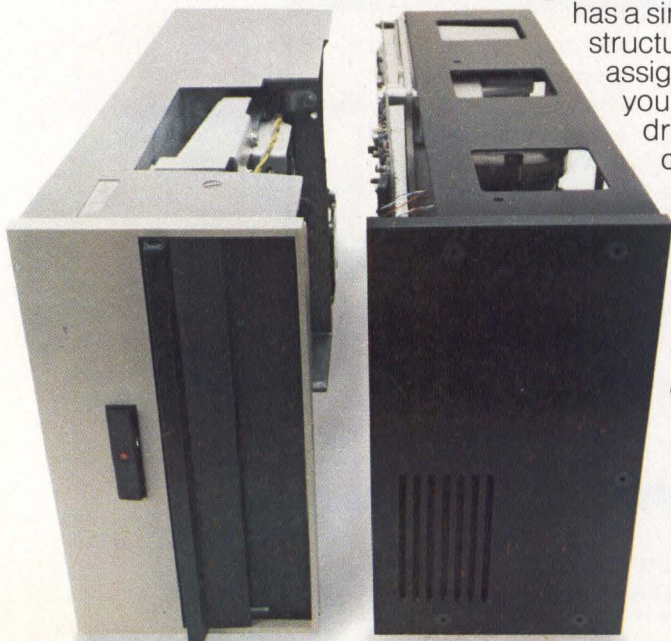
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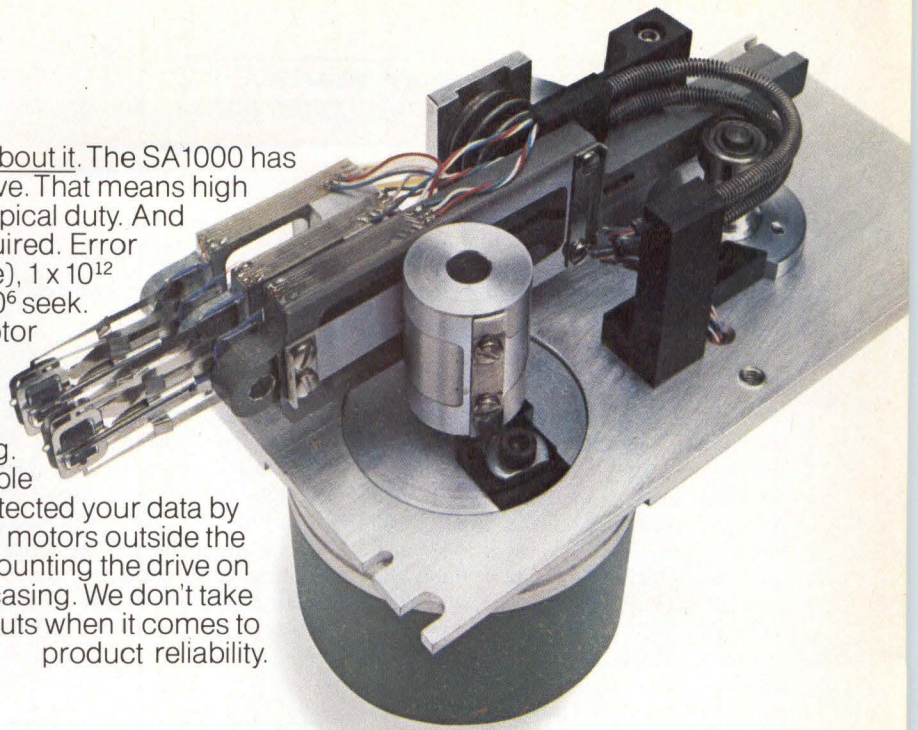
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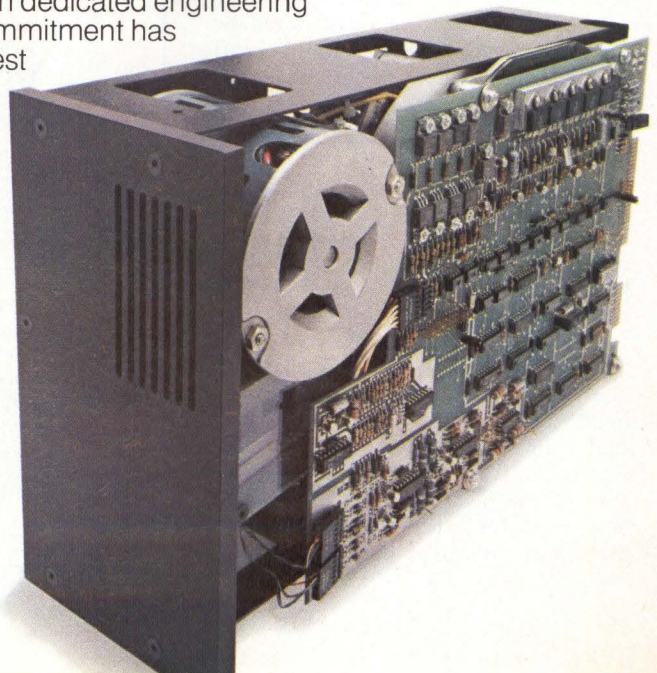
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CIRCLE 26 ON INQUIRY CARD



Single-Channel, Positionable Magnetic Tape Head Records 16 Tracks with 12k-Bit/in Density

A positionable bidirectional read-after-write head can double the bit density and significantly increase track density of tape systems. Developed by Nortronics Co, Inc, 8101 Tenth Ave, N, Minneapolis, MN 55427, the head combines the best of disc and tape head technologies to reduce the cost of backup storage for rigid disc systems.

Increased use of rigid discs in various sizes for high speed access to data has created the need for low cost backup systems. Such systems do not require the high performance characteristics of large tape drives because they normally run in a streaming mode—you turn on the drive and let it run—continually recording data with no start or stop. To do this economically, however, both high track density and high bit density are necessary to provide the needed capacity. Current backup storage—floppy discs and 7-track 0.25" (0.635-cm) tape drives—are either too expensive or lack the necessary capacity.

The single-channel positionable head permits high track and bit density recording, at a fraction of the cost of heads in existing backup systems. Capable of writing up to 16 data tracks (see Fig 1) on 0.25" magnetic tape and increasing bit density to 12,000 bits/in (4724/cm), approximately twice what is currently possible, the head is constructed of ferrite and ceramic to extend head and tape life, and to permit increased bit density.

In use (see Fig 2), the single-channel head is first positioned to record one track near the tape edge. When the tape has run its length, the head automatically reverses itself, moving and recording data in the opposite direction. This recording process continues in a serpentine manner.

Read-after-write capability (Fig 3), automatically reversed when the tape is reversed, is a key feature of the head, according to Matthias Grundtner, director of engineering for Nortronics. When tape is reversed the area of the head that was reading is now used for writing, and the area that was writing begins reading.

"While the tape is written in one direction, the same track will have a symmetrical assembly on the other end that is used to read back. Thus, as the tape moves across the head, it is written, erase trimmed, and read back immediately after writing." This feature permits data to be transferred from disc to tape with minimum error. A second important feature of the

head is the symmetrical tunnel erase system which permits close track spacing, and therefore more tracks with reduced noise.

Prototype units are currently being built; manufacture of the heads will begin early in 1980. In high production quantities, the 1-track positionable head will cost approximately \$75.

Circle 175 on Inquiry Card

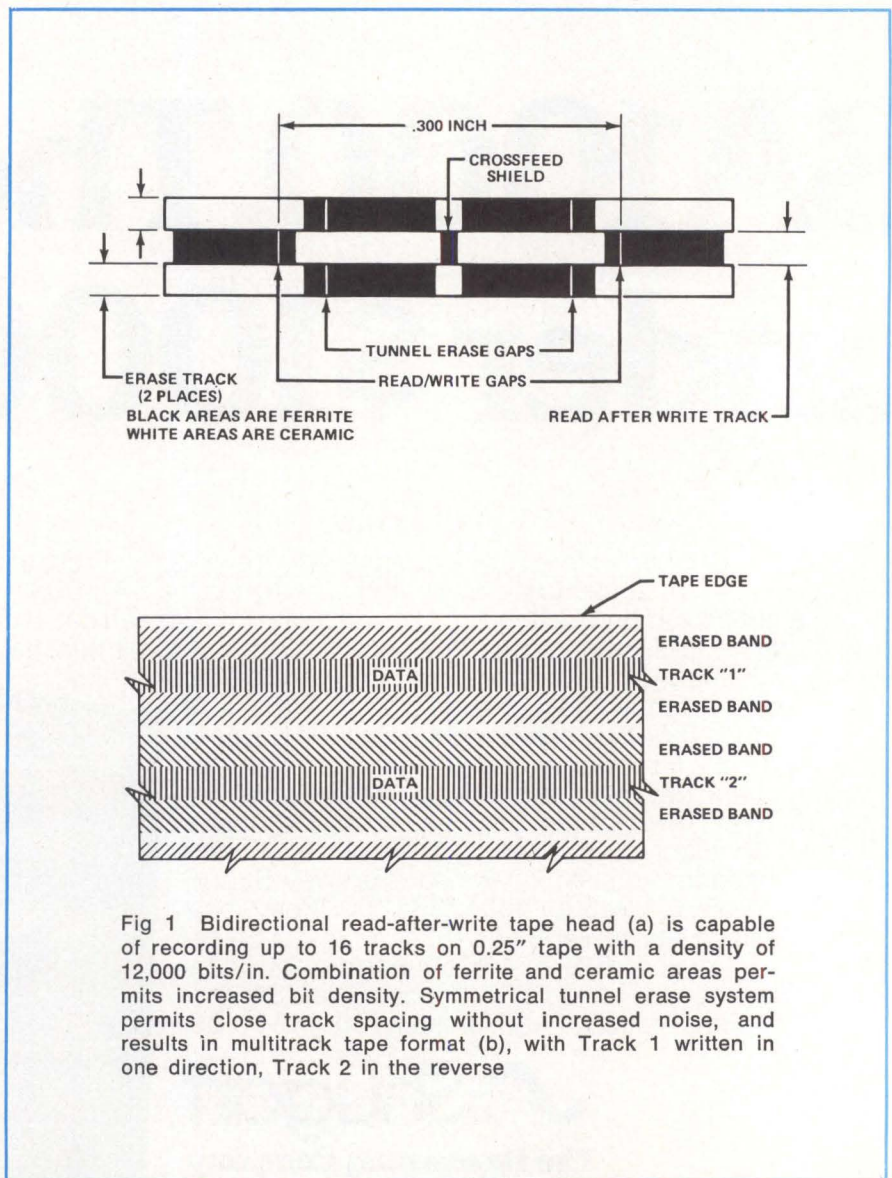


Fig 1 Bidirectional read-after-write tape head (a) is capable of recording up to 16 tracks on 0.25" tape with a density of 12,000 bits/in. Combination of ferrite and ceramic areas permits increased bit density. Symmetrical tunnel erase system permits close track spacing without increased noise, and results in multitrack tape format (b), with Track 1 written in one direction, Track 2 in the reverse

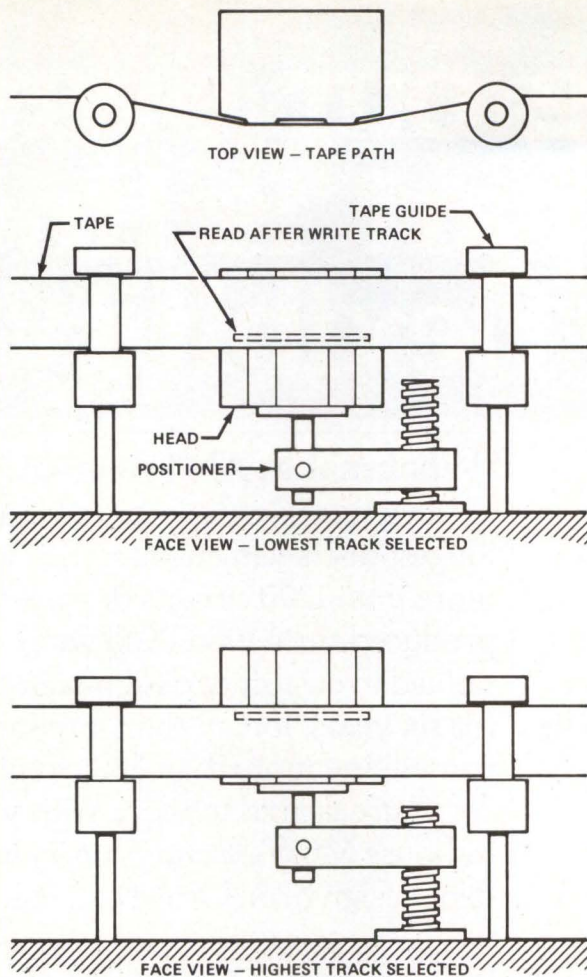


Fig 2 Positionable single-channel magnetic tape head assembly combines disc and tape head technologies to provide high track and bit density at low cost

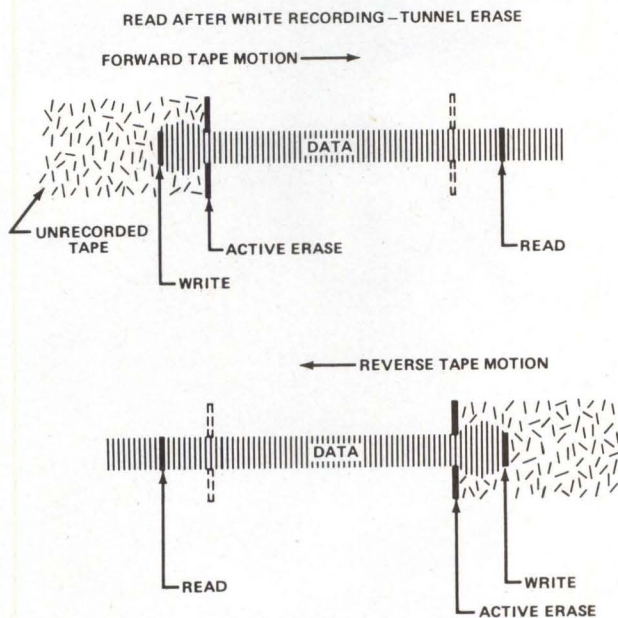
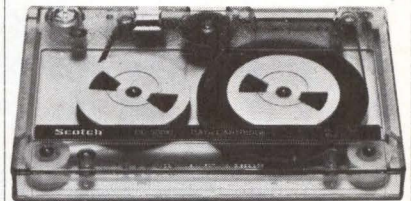


Fig 3 Read-after-write capability that is automatically reversed when tape is reversed results in serpentine recording on tape

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Speed (per unit area)	6	4	5	3	2	3	1	0
Power Consumption (low speed)	6	2	4	5	1	5	3	3
Area (per logic function)	4	3	3	2	5	2	1	0
Noise Immunity	4	2	5	5	1	4	3	3
Logic Flexibility	3	1	3	3	1	2	1	1
On-Chip Clock Generation	4	2	5	4	1	3	2	2
Bipolar Compatibility	5	2	3	1	1	1	1	0
Power Supply Latitude	4	2	4	4	1	3	2	3
Process Simplicity	1	2	2	2	6	3	4	6

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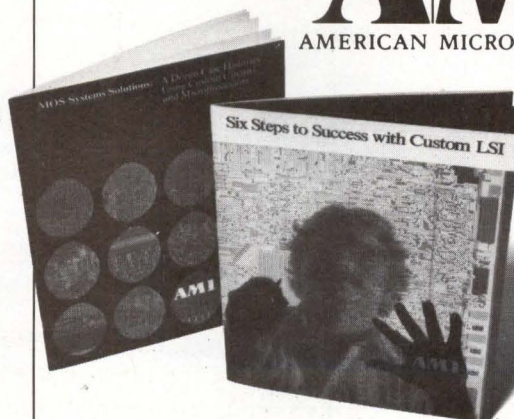
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MOS Memory Option For Mainframes Increases Execution Speeds

Doubling memory capacity of earlier MOS configurations and making semiconductor memory available on the DECsystem 1091-S, the MOS memory option, announced by Digital Equipment Corp, Large System Group, Maynard, MA 01754, provides a factor of 14 improvement in availability. Expansion of primary memory made possible with the option decreases the reliance on secondary memory devices and thus increases system execution speeds.

Because the MOS memory modules used for both the DECsystem 1091-S and DECsystem 2040 and 2060 incorporate error correction logic capable of correcting single-bit errors and detecting double-bit errors, an improvement in reliability can be seen over core memory systems. In addition, 64k-byte segments of memory can be mapped out dynamically to allow for deferred corrective maintenance.

Up to 12M bytes of MOS memory can be installed in the 1091-S configuration; the first 6M in the basic system cabinet, with a separate cabinet necessary for additional increments. The same type of cabinet is used to expand capacity of 2040 and 2060 configurations to the system maximums of 12M bytes.

Basic system configurations of 2040, 2060, and 1091-S, including 1M byte of memory, are priced from \$324,600,

\$399,100, and \$440,700, respectively. Deliveries of MOS memory and memory expanded versions are scheduled for early next year.

Circle 176 on Inquiry Card

Mid-Range Computer Meets Short Term Demands With Accelerator Option

A mid-range addition to the 470 series of high performance computers made by Amdahl Corp, 1250 E Arques Ave, Sunnyvale, CA 94086, the 470V/7A gives users high performance at lower cost with the option of increasing capacity through upgrades. 470/Accelerator hardware provides ability to meet short term increases in demand without having to support expensive idle capacity over the long term.

With performance rated between that of the V/6-11 and the V/7 and slightly higher than that of the IBM 3033, a minimum configuration V/7A consists of 4M bytes of memory, 12 I/O channels, 32k-byte high speed RAM buffer, console display, and independent console processor. Machine cycle time is 29 ns. This configuration expands to 16M bytes of memory and 16 I/O channels. Optional are 470/Accelerator, channel to channel adapter, and 2-byte interface.

The 12 I/O channels can be configured by the user into any combination of block multiplexer, byte multiplexer, or selector channel

mode. 2048 subchannels are provided. Using high performance bipolar RAMs to speed access, the buffer is organized as a set associative cache memory with eight sets.

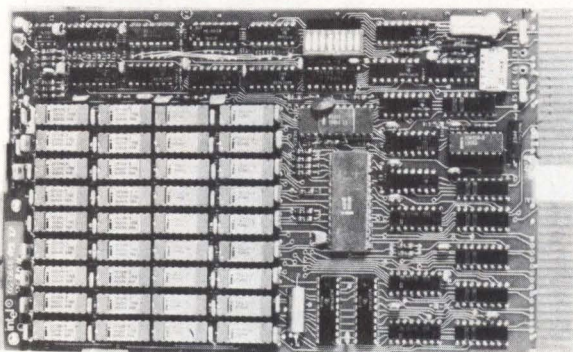
The independent console processor, an internal minicomputer, performs service diagnostics, monitors important CPU functions, and interfaces to the company's diagnostic assistance center to obtain remote maintenance support for the system.

Available on a time metered rental basis, the 470/Accelerator when activated by user command increases processor performance. It operates with V/5 and V/5-11, raising their performance to V/6 and V/6-11 levels, respectively; and increases performance of a V/7A to the V/7 level—approximately 20%.

Consisting of special console processor software command and LSI hardware, the option installs within the existing system. A single accelerator command brings the unit on-line; another turns the unit off. Software is not affected either in the transition or while the CPU is in accelerator mode. Similarly, jobs are not disrupted by either on or off command.

A hardware meter to measure CPU time spent in accelerator mode is included in the system as a usage meter, not an elapsed time meter. In minimum configuration the V/7A will sell for \$2,450,000. The Accelerator option will rent for \$1800/mo for 20-h usage, plus \$90/h beyond the 20-h minimum.

Circle 177 on Inquiry Card

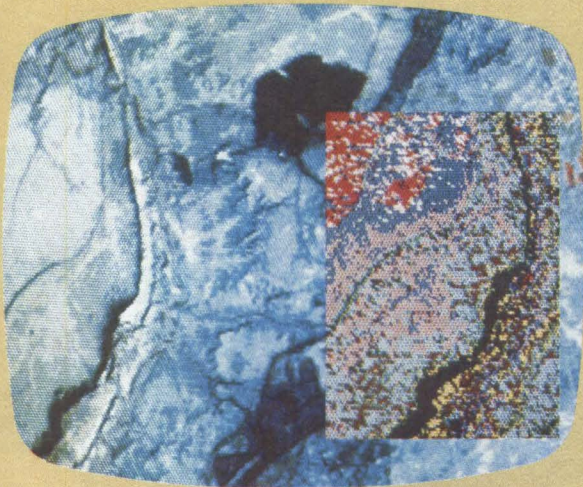
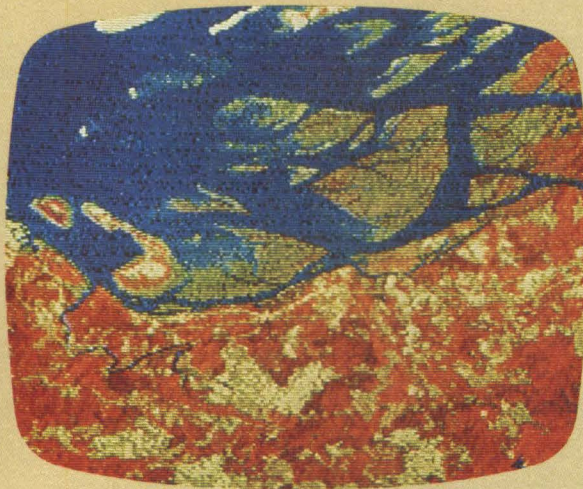


LOW PRICES ON INTEL'S LSI-11 & PDP-11 COMPATIBLE MEMORY

Model in 5004 Memory For LSI-11, LSI 11/2 & PDP 11/03 5004-624 48KBytes (24K X 16) \$732.00 5004-632 64KBytes (32K X 16) \$820.00	Model in 5034 Memory For PDP - 11/04 & PDP - 11/34 5034-832 64KBytes w/Parity (32K X 18) \$1062.00 5034-864 128KBytes w/Parity (64K X 18) \$1606.00	Model in 1670 Memory For PDP 11/70 (Price upon request)
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ORDER FROM: SECO Sales, Inc., 111 S. Maitland Ave., Suite 202,
P. O. Box 1475, Maitland, FL 32751 - Phone 305-645-3444

Image processing. Your way.



Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
- Image multiplication and ratioing
- Zoom and pan
- 512 x 512 panning window on a 1024 x 1024 image
- Function memories
- Pseudo-color tables
- Video digitizers with frame averaging
- Split screen and image toggling
- Full graphics and alphanumerics
- Up to four overlay memory planes
- Independent cursors
- Trackballs and joysticks
- External synchronization
- Plug compatible interfaces for most minicomputers

In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

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WHAT SPERRY UNIVAC IS DOING IN THE MINICOMPUTER BUSINESS.

WE'RE BUILDING HARDWARE THAT HELPS CUT THE COST OF SOFTWARE.

The Sperry Univac V77-600 and V77-800 minicomputers with SUMMIT don't just speak Pascal, they were designed and assembled with it.

At Sperry Univac Mini-Computer Operations, we understood that Pascal was a giant advance in computer technology when other manufacturers still considered it a passing fancy.

And now that they are just beginning to recognize Pascal as the cost saving, time saving solution to the spiraling expense of software, we've already perfected our Pascal designed systems.

MAKES PROGRAMMERS 10 TIMES AS PRODUCTIVE.

Pascal is a high level, general purpose language, composed in orderly steps so it's easy and efficient to write. It provides for excellent documentation so that software errors can be reduced by as much as 90% over Cobol.

But most important, Pascal dramatically cuts the time necessary for programming — a major consideration when most programming staffs spend nearly 75% of their time just maintaining existing software.

COST CUTTING PORTABILITY.

Although Pascal is frequently used as a system development language, unlike an assembly language, it can be transported between computers that support Pascal with minimal reprogramming.

This advantage alone means that the existing software can be used on newer, state-of-the-art systems. It's not necessary to write a whole new program for the new computer.



**ALL THE TOOLS
FOR COMPLETE PASCAL SUPPORT.**

The Sperry Univac Structured Programming System (SPS) running under our SUMMIT operating system, includes several powerful program development tools available for Pascal support.

Pascal Compiler conforms to recognized industry standards and provides concurrent compilation for from one to 32 terminals.

Pascal Debugger allows the terminal user to monitor execution of Pascal code on a program, procedure, or line-within-procedure basis.

Pascal Program Formatter accepts Pascal program source code in an unstructured form and produces indented source output, conforming with generally accepted practice for structured programs.

SPS Text Editor allows the terminal user to enter and edit Pascal source code in an efficient manner.
SPS Document Formatter provides for the

efficient generation of documentation.

Pascal Concordance program sorts and outputs all symbols and symbol-references within a Pascal source file.

**WE'RE COMMITTED
TO SOLVING YOUR PROBLEMS.**

That's why we're committed to Pascal. We know a major concern of our customers involves curbing and controlling the high cost of programming and maintaining software.

At Sperry Univac Mini-Computer Operations, we feel that with Pascal and our Pascal adapted systems we're helping our customers solve those problems.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, Marketing Communications.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

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CIRCLE 31 ON INQUIRY CARD

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ICEMAN delivers the Never-Say-Die supply!



400 W, PSN1801, Single-Output
ICEMAN Switching Power Supply

Now you have reliability that won't melt away.

Just like our line of ICEMAN™ linear supplies, long-term reliability in a switcher begins with how it's made. Fewer components, fewer connections, less wiring, reduced failure points and modes.

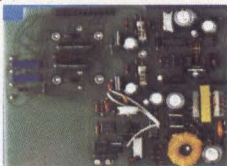
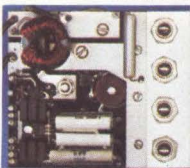
That was our design goal.

By actual count, this Motorola PSN1801 switcher contains only 143 electrical parts—about 25% less than the nearest comparable. It employs only 22 wires. Others have 200 or more. It uses just one connector. Some use as many as 20.

Two boards and MTBF.

There's more protective circuitry, in less space, in a Motorola ICEMAN switcher than anyone else offers. Just two circuit boards do it all.

The control board measures only 24 square inches and contains the latest multifunction ICs in place of dozens of discrete parts. The board



furnishes remote turn-on/turn-off, overcurrent and short-circuit protection, soft-start to limit overshoot voltage, automatic reset of OVP, primary current limit and capacitor bleed-off circuits.

The 18 square inch main output board combines OVP, soft-start for inrush current limiting and all output supply components.

ICEMAN keeps his cool.

All the way through. Longer. More efficiently.

Four paralleled, 60 A, high-temperature Switchmode™ Schottkys, with a maximum of 240 A capability, are used to achieve the 5 V, 80 A output. In other words, they're run at just 33% of total capability. And the Schottkys and the low-sat, high-speed Switchmode power transistors run at no more than 65% and 60%, respectively, of maximum rated junction temperatures, minimizing thermal stress.

Specifications

PSN1801, 5 V/80 A
PSD1802, 5 V/60 A, 12 V/8 A
PST1803, 5 V/60 A, 12 V/4 A, 12 V/4 A

Input. 100-130 Vac/200-260 Vac (Selectable), 45-440 Hz Single Phase

Output. Floating, isolated from each other and from ground, 600 Vdc max

Regulation. Line: $\pm 0.1\%$ Output, for 100-130 or 200-260 Vac. Load: $\pm 0.29\%$ Output, no load to full load

Ripple and Noise. Less than 10 mV RMS, 50 mV p-p, as measured with 50 MHz scope

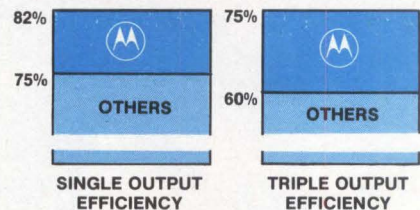
Temp. Coefficient. Less than $0.2\%/^{\circ}\text{C}$

Switching Frequency. 25 kHz (Pulse width modulated)

Transient Response. 500 μs to within 1% after a 25% load change at 5 A/ μs , main output

The standard warranty period for all Motorola linear and switching power supplies is 1 year.

The heat sinking is up to 100% thicker than others, ensuring even thermal gradients with all the heat quickly going where it's supposed to go . . . out. We've even special-wound the transformer to cut losses.



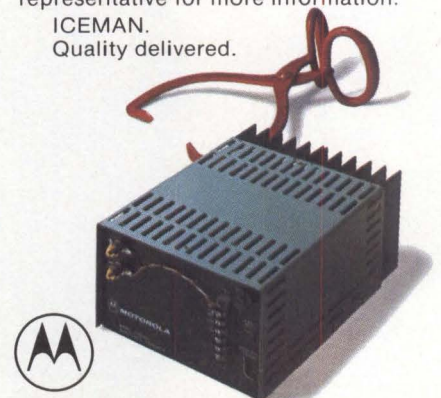
You also get minimum 30 ms hold-up time so the regulated 5 V supply is retained after interruption under full load.

Cost is cool, too.

Prices for the three models range from \$530 to \$675, 1 to 9 quantity.

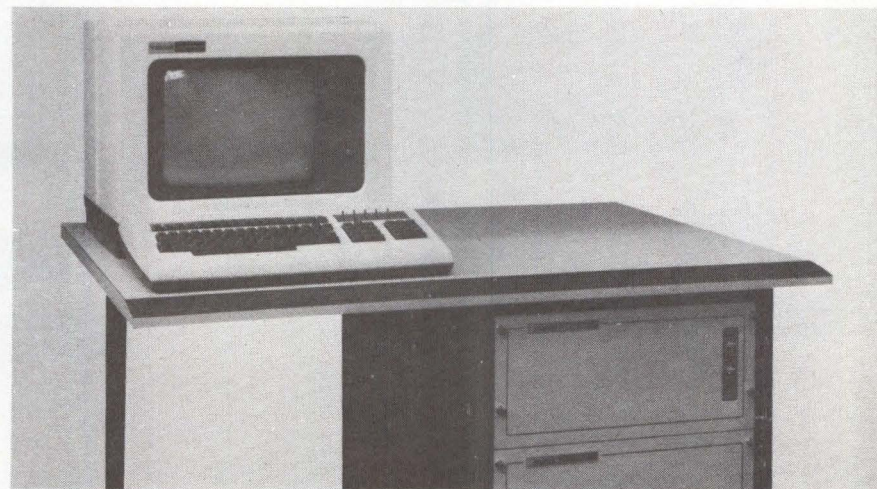
Contact Motorola Subsystem Products, P.O. Box 20912, Phoenix, AZ 85036, (602) 244-3103 or your authorized Subsystem distributor or representative for more information.

ICEMAN.
Quality delivered.



MOTOROLA INC.

Color Graphics Computer Programmable In Pascal/Assembly Language



Fully integrated RM-6114 color graphics computer system from Ramtek is programmable in Pascal or assembler language, can operate as either standalone system or with host computer, and provides color data presentation as well as data storage and manipulation

The 6114 Colorgraphic computer provides a means for graphic presentation, a programming language that allows users to manipulate data, and a standalone system for storage of data files. The fully integrated color graphics computer system from Ramtek Corp, 2211 Lawson Lane, Santa Clara, CA 95050 gives users a range of choices not previously available in a low cost, medium resolution display system. While previous systems have concentrated on data entry and manipulation problems, this system uses programmable graphics capabilities to accommodate instant interpretation by presenting data visually and in color.

In its Pascal configuration the system consists of Z80 central processor operating at 4 MHz with 64k programmable memory, floppy disc controller, 250k-byte single-density floppy disc drive, and pedestal display unit. Graphics refresh memory is 256 x 320 with 240 x 320 displayable pixels (picture elements). RGB output may be used with NTSC encoder to drive a video cassette recorder. The format also provides square pixels since the CRT screen itself is a 4:3 aspect ratio as is the displayable pixel array. The display features a full screen crosshair cursor and eight standard colors. Alphabetic memory will display 96 characters each.

The Pascal system is a licensed version of UCSD Pascal, permitting

any Pascal source programs written on an UCSD system to be transferred to the 6114 and the reverse. This use of standard operating system software permits software to be transferred from one computer to another and enables the use of standardized computer graphics procedures.

The large amounts of memory and large number of peripheral devices sometimes necessary with a graphics system are handled with the hardware/software RAMOS (Ramtek operating system) package. RAMOS provides hardware memory management and protection up to 512k bytes, special user/system switching control, and I/O interrupt vectoring. Multi-tasking and virtual space features in the operating system allow users to add software in assembly language.

The system's CRT oriented editor creates and updates text files, which are edited on the console CRT using a file window concept. A file manager allows files to be created and controlled on the floppy discs. Access to assembly language programming is supplied by Z80 Assembler and linker.

Optional interfaces for the system include RS-232 communications, color printer/plotter, black/white printer, and graphics tablet. Price for the basic system is approximately \$12,000. With a monochrome display (upgradable to color), the system is available for about \$1000 less.

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ICEMAN'S Available

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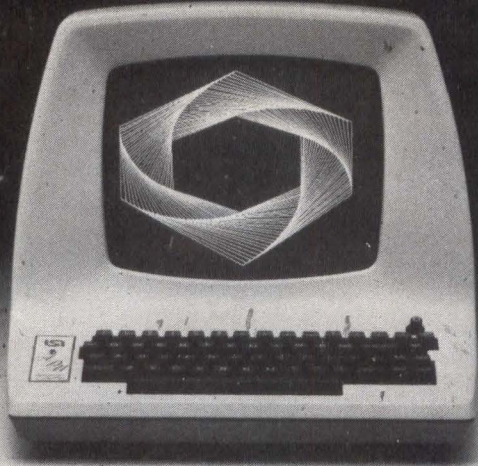
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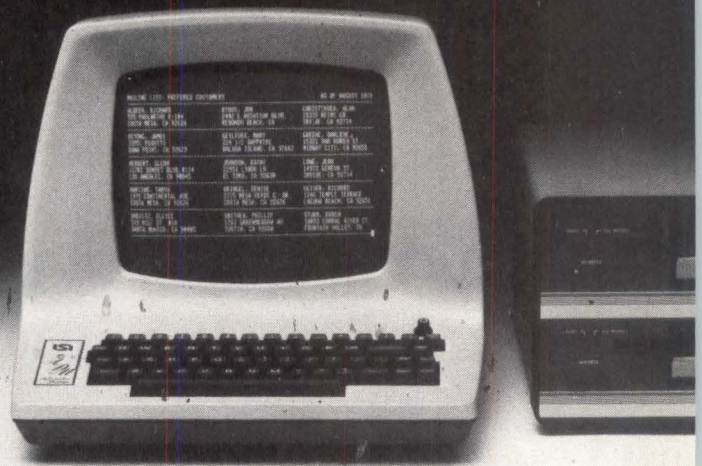
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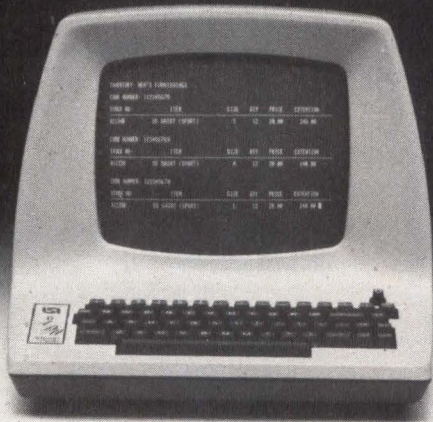
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INVENTORY CONTROL



PORTABLE I/O DEVICE



HOME COMPUTER SYSTEM



VERSATILE DATA TERMINAL



What could anyone possibly do with 85,000 Dumb Terminals?

That's how many ADM-3A's there are out in the field working right now. And more being shipped each day. Now just what accounts for such remarkable popularity?

Sure, it's the definitive dumb terminal, adaptable enough to fit a host of applications. It has a 12-inch diagonal screen. Full or half duplex operation at 11 selectable data rates. 1920 easy-to-read characters in 24 rows of 80 letters. 59 entry keys. An RS232C interface extension port. And direct cursor addressing.

But we wondered if all 85,000 Dumb Terminals were being used for just everyday data entry. So we checked around.

And found that people are using Dumb Terminals for things even we never thought of.

THE ADM-3A GOES INTO BUSINESS.

More and more OEM's are putting the Dumb Terminal into small business systems. They assemble a package that usually contains a disk, memory, a printer, and a video display terminal — the adaptable ADM-3A.

So the chances are that when you buy a small business system from someone, it'll contain, you guessed it, the amazing Dumb Terminal.

IT TAKES STOCK OF THE SITUATION.

Many businesses are using the Dumb Terminal, along with a light pen (Universal Product Code Decoder), to keep track of their inventory. The decoder is interfaced to the Dumb Terminal, and when a piece of merchandise imprinted with a Universal Product Code passes under it, the item is entered into a computer for tallying.

Simultaneously, the item is also displayed on the ADM-3A's screen — so it's instantly available for quick double-checking.

PROGRAMMERS LIKE IT, TOO.

Surprisingly enough, many computer programmers use the ADM-3A as an effective, portable I/O device. They can take it into a back room or, along with an acoustic coupler, to their homes if they wish, and compile programs nearly anywhere.

By using telephone lines, they can have direct access to a computer. Or, with the addition of an inexpensive cassette, the programmer can store the program on tape and enter it into the mainframe at a later date — with no loss of data.

THE DUMB TERMINAL PUTS ON A NEW FACE.

Some of our more ambitious customers have transformed their ADM-3A's into sophisticated graphics terminals. Simply by installing another PCB, they've enabled their terminals to perform complex plotting, graphics, and even draw charts.

And the Dumb Terminal is so adaptable that these industrious people had no trouble with installation — the graphics PCB required not the slightest cutting or soldering. It simply slipped right in and started working, all in a matter of minutes.

YOU CAN EVEN TAKE IT HOME TO MEET THE FAMILY.

We discovered that many computer buffs are using the Dumb Terminal as an inexpensive way to upgrade their systems. After all, the equipment found on most microcomputers leaves a lot to be desired. Such as the tiny five or six-inch screen, for instance.

By upgrading to the ADM-3A, they get a full 12-inch screen that's easy on the eyes. Not to mention

a lot of capabilities they wanted, but just didn't get on their systems.

All for only \$895.

THE DUMB TERMINAL. THE HALLMARK OF VERSATILITY.

When you get right down to it, the Dumb Terminal's applications are pretty amazing.

It can be interfaced with a staggering variety of RS232 devices. Such as cassettes, disks, floppy disk drives, printers, paper tapes, and readers, to mention just a few.

In fact, the ADM-3A is compatible with just about any RS232 device you can name. Even other video terminals, if you wish.

And people call this a "dumb" terminal?

WHAT WILL THEY THINK OF NEXT?

Who knows? But it seems that as long as there are Dumb Terminals, people will find new, unsuspected uses for them.

Of course, the ADM-3A will continue to be the same dependable data entry terminal that's made it an industry legend.

With good, reliable features and a minimum of frills. Nothing could change that. The fact is, we think that's probably the main reason that so many people have come up with so many uses for the ADM-3A.

Who said you can't teach a Dumb Terminal new tricks?

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803. (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 968-0112. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (4867) 80666.

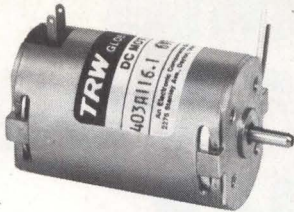
DUMB TERMINAL SMART BUY



LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

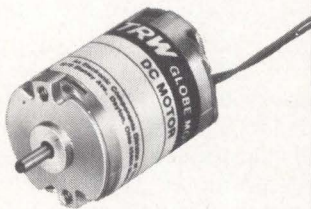
Dumb Terminal® terminal is a registered trademark of Lear Siegler, Data Products Division.

CIRCLE 33 ON INQUIRY CARD



New 1½" DC motor-tach cuts noise in your system

With the new EM-15 motor-tach, you don't have to run AC power lines into noise-sensitive areas of your system. Rated voltage: 6 to 24 v.d.c. Tach frequency: 8 cycles/rev. AC tachometer is brushless. You get accurate speed at low cost.



Low-cost DC PM motor only 1¼" in diameter

Our economy EM-13 motors have many of the features of our quality military motors. Torque constant: 2.6 oz. in./amp for 12 v.d.c. version. Voltage constant: 1.92V/K rpm. Available in 6, 12, or 24 v.d.c. versions. Tooled for high-volume production.



In a hot spot? Cool it with our fans and blowers

Cool your critical components with our miniature DC fans and blowers. Power source 12 to 115 v.d.c. 10 to 315 cfm free air. Propeller, centrifugal, tubeaxial, vaneaxial, and propaxial types. Diameters 1.25" to 5.75".

TRW GLOBE MOTORS

Dayton, Ohio. (513) 228-3171.
Distributed by Arrow, Hall-Mark,
Hamilton/Avnet, Jaco, Pioneer.

Compact Computer System Broadens Range Within Compatible Family

Reducing the entry level price of the 3000 family to \$49,750, the HP 3000 series 30, introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, is a full function machine capable of batch operation, program development, data entry, and data communications. In addition to a lower price, the unit provides a more compact package and an intelligent network processor (see p 26) that relieves CPU congestion and enables communication at speeds to 56k bits/s.

Compact design and low power requirements of the system stem from the application of proprietary silicon on sapphire technology. The CPU is based on three SOS chips (ICF-25A) that are integrated at the 15k gate level. Memory is composed of 16k RAMS. Packaged within a cabinet measuring 24 x 30 x 18" (61 x 76 x 46 cm) the unit is accompanied by a separate system/maintenance console and system disc. It runs on standard 120-V power, uses only 15 A, and needs no special air conditioning.

The system is a full function HP 3000 capable of batch operation, program development, data entry, and data communication. Differences

between it and Series 33 and III lie in performance and expandability. Since it uses the MPE-III operating system, applications programs written for those machines will run without reprogramming, recompiling, or relinking. Among the application areas are as standalone business data processing systems and as stations within 3000 networks. Like the series 33, the series 30 incorporates a self-test feature and remote system verification program.

Series 30 systems can execute programs written in COBOL, BASIC, FORTRAN, RPG, or SPL, (the company's systems level programming language). Bundled in with the machine are IMAGE/3000 database management with QUERY, VIEW/3000 business forms generating software, and KSAM/3000 keyed sequential file access method.

List prices for the systems begin at \$49,750 for a base level unit that has 256k-bytes error correcting semiconductor memory, 1M-byte flexible disc, four asynchronous terminal ports, system/maintenance console, 20M-byte system disc, and eight powered I/O expansion slots. This configuration can be expanded to include 1024k-byte main memory, 960M-byte disc capacity, up to 32 terminal ports, 4 magnetic tape drives, and 2 line printers. Up to two communications lines can be added, each replacing four terminal ports.

Circle 179 on Inquiry Card



Hewlett-Packard's application of SOS technology in its 3000 family compatible series 30 reduces power and cooling requirements as well as package size

“Frankly, IDC connectors used to be a pain in the neck.”



“My problems were monstrous.

When I could find the connectors I needed, I would have to go digging around for the cable. If the price was right, the products weren't. And on and on, eon after eon.

Until one day my doctor suggested Spectra-Strip.

Of course! They've been making flat cable longer than anybody, so they would have to know how to make ends meet!

They do, and now I get all my IDC receptacles, headers, DIP plugs and sockets, PCB transitions and card-edge connectors from a single, reliable source: Spectra-Strip.

When things get really busy at the lab, I even have them or one of their value-added distributors provide completely terminated and tested jumpers and custom assemblies.

Their products are just what the doctor ordered, their Q.C. has real teeth in it, and their prices never put the bite on my budget.

For the name and number of your nearest distributor or rep, write Spectra-Strip, 7100 Lampson Avenue, Garden Grove, CA 92642, telephone (714) 892-3361. In the East, call (203) 281-3200.

And tell them Frank sent you.”



When you're down to the wire.

Family of Systems Offers Distributed Processing Benefits to All Users

600/X5 series distributed data processing systems, announced by Nixdorf Computer Corp, 168 Middlesex Tpk, Burlington, MA 01803, offer increased processing power, configuration flexibility, and concurrency. Each system in the series—consisting of 600/15, /25, /35, /45, and /55—can perform batch and interactive communications, local file processing, data entry, word processing, and local data base inquiry and update using DBMS.

All models provide virtual memory multiterminal operations, synchronous batch and interactive communications, character and line printers, and extensive mass storage capabilities. Operating under the control of the Distributed Processing Executive (DPEX) operating system, the machines have a virtual architecture that allows performance of multiple concurrent tasks without real-memory constraints. Communications protocols include 3741, 2780, 3780, and HASP multileaving remote batch communications, as well as 3270 transaction processing emulation.

Intended to serve in remote applications where small volumes of data are entered and processed locally before transmission to another system within a network, the 600/15 is a diskette based distributed processing system with 1100-ns processor. It can perform any two of the following operations concurrently: batch or interactive communications, local file processing, data entry, local data base inquiry and update, or word processing. Support is provided for a 2-terminal, 2-diskette configuration with 300k bytes of virtual memory.

Designated as a remote terminal system for larger members of the family, the 600/25 has a 1100-ns processor and offers the same concurrency as larger models. It provides support for up to six terminals, two diskette units, 4.8M-bytes fixed disc capacity, and 1M-byte virtual memory.

Among the larger configurations, the 600/35 serves in small remote offices where concurrent operations are required but cost must be kept low. This unit has a 1100-ns proces-

sor and supports up to eight terminals, two diskettes, two fixed discs, magnetic tape unit, and 2M-byte virtual memory.

Providing a mix of processor power and configuration flexibility that meets demands for multiple concurrent operations, the /45 has a 700-ns processor. It supports up to 16 terminals, two diskettes, magnetic tape, virtual memory of 8M bytes, and up to 132M bytes of fixed disc storage.

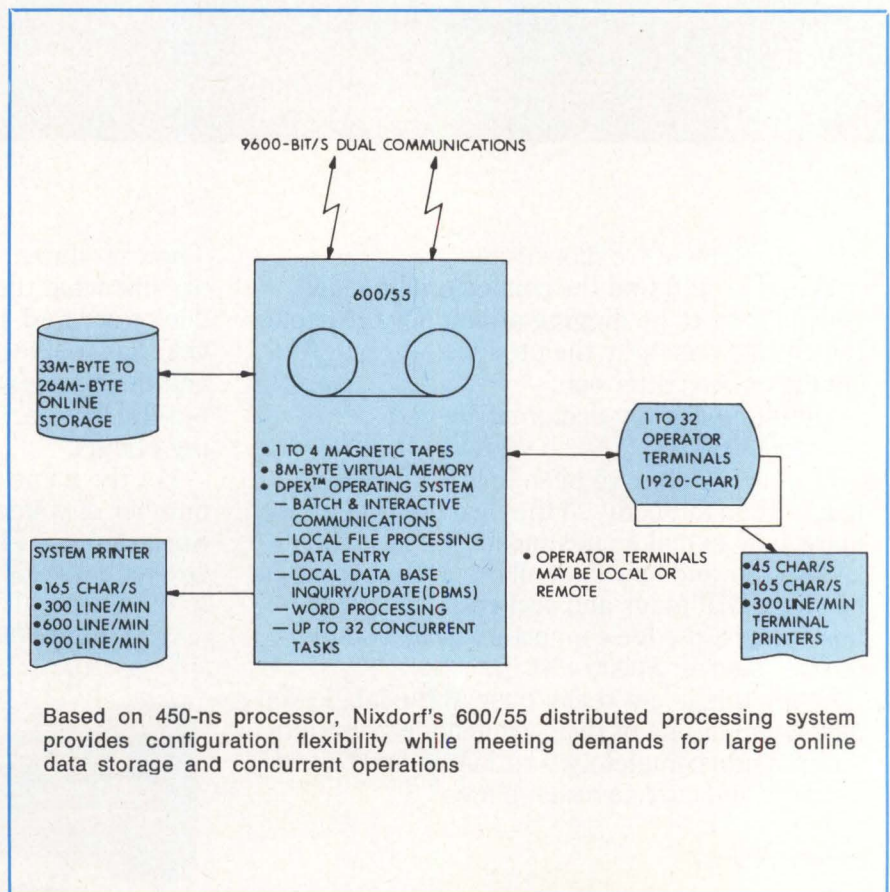
The top of the line /55 is designed for operation where large volumes of information must be locally stored, interrogated, and maintained. Incorporating a 450-ns processor, this system handles up to 32 terminals, 2 diskettes, magnetic tape unit, 8M-byte virtual memory, and 264M bytes of online storage.

A terminal oriented, multitasking virtual memory operating system, DPEX provides a combination of high level data processing and communications capabilities. To provide opera-

tional simplicity for both operator and programmer, the system manages all aspects of virtual memory allocation, application program relocatability, and sharability, and simultaneous data base access. In addition to data processing capabilities, it provides a range of communications emulators. Features include file inquiry, retrieval and update capabilities, terminal and system security, sort/merge, batch and interactive communications, and data entry capability. Word processing is an optional software package that allows operators to enter, store, correct, manipulate, and output document style text. The word processing system operates concurrently with other functions and may be used by multiple operators simultaneously.

Prices for the systems in basic configurations start at \$31,450 for the 600/15 and range upward to \$69,670 for the 600/35. A top level 600/55 has a price of \$159,050.

Circle 180 on Inquiry Card



Datacom Interfaces. 5 chips... 1 socket.

Signetics' family of UARTs/USARTs lets you design up—not out.

Specify a socket for one of our five programmable datacom controllers . . . and you've specified it for all of them. Design your PC board for today's needs, then design up with the same board tomorrow.

Simply plug in the Signetics UART or USART that's right for the job. With all the same pinouts, your datacom options stay open.

If you want asynchronous *only* data transfer, insert our 2641 UART. It's fully programmable, with an on-chip baud-rate generator.

Need both synchronous and asynchronous flexibility? Choose our industry-standard 2651 USART. Same socket.

Baud-rate table changes? Pick one of our enhanced USARTs: 2661-1, 2661-2 or 2661-3. Same socket, again.

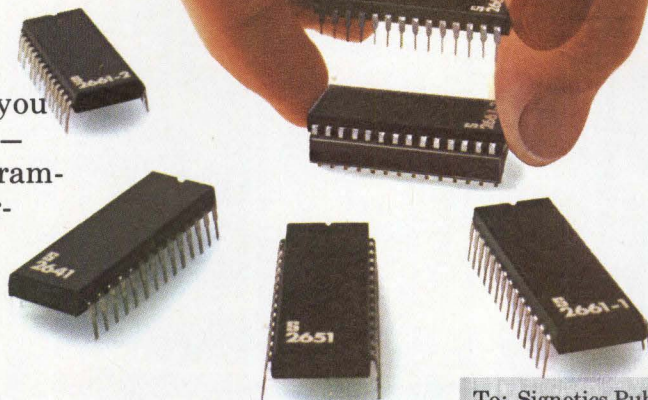
A quick plug-in replacement shifts you to the desired range—where you can program-select from 16 different baud rates.

Want to support bisync operation? Team any of our pin-compatible USARTs with the Signetics 2653 Data Integrity Controller for a fast firmware solution. Add our 2652 Multi-

Protocol Communications Controller and extend your system to include SDLC, HDLC and ADCCP.

Datacom controllers. Five pin-compatible UART/USARTs. Plus two unmatched LSI solutions for data integrity and protocol control.

Start putting 7-chip convenience into your datacom design today. Contact us, your nearby Signetics sales office or authorized distributor.



Signetics

a subsidiary of U.S. Philips Corporation

Signetics Corporation
811 East Arques Avenue
P.O. Box 409
Sunnyvale, California 94086
Telephone 408/739-7700

Learn more about LSI for Data Communications. Signetics and its Hamilton/Avnet distributor are co-sponsoring data communications seminars in 24 cities. Call us or Hamilton/Avnet for your admission ticket and program details.

To: Signetics Publication Services, 811 E. Arques Ave.,
P.O. Box 409, Sunnyvale, CA 94086

() Please send complete specifications on Signetics' socket-compatible family of datacom controllers.

() Send me the above plus data sheets on the 2652 and 2653. CD1079

Name _____ Title _____

Company _____ Division _____

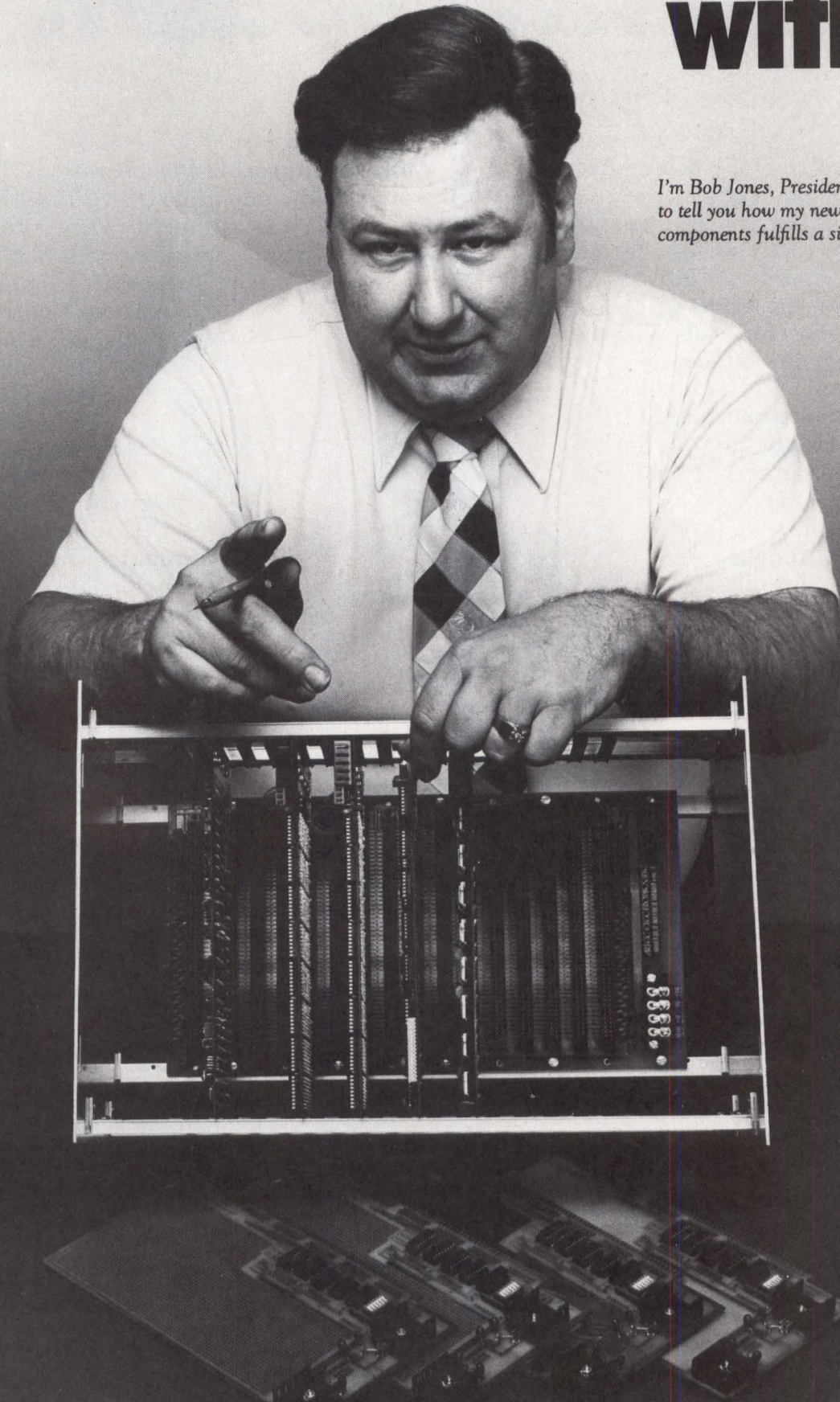
Address _____ MS _____

City _____ State _____ Zip _____

() My need is urgent. Please have a datacom specialist phone me at once: () _____

"I can cut your control without

I'm Bob Jones, President of Artec. I'd like to tell you how my new system of computer components fulfills a six year ambition of mine.



system CPU costs 40% sacrificing quality”

You may think I'm crazy now. You won't after you find out more about this system.

Ever since I started Artec Electronics, I've wanted to build a computer system that was better than the ones built by the computer industry's giants. As you can see from the comparison chart, I've done it.

The Artec Centurion System not only offers more features than the popular 8-bit microcomputer board families built by Intel and Vector Graphic, but substantial savings too.

The key to lowering costs without lowering quality was choosing the S100 bus. This major innovation allows smaller PC boards, fewer chips and more compact cabinets. All features that reduce system costs. But the level of quality is superior to any board family anywhere.

Consider this 5 MHz CPU with monitor, math chip and on-board memory for \$850.

Using the Intel 8085A2, this CPU card has been specially designed to do what you want it to. Hardware floating point lets you perform math four times faster than you can on the other CPUs. To get this kind of performance before, you probably had to buy a mini.

The board also comes with a powerful, but simple to use, monitor in PROM memory. This monitor lets you test memory, debug software and check the status of your program at any time.

For a scratch pad, the CPU uses 3K of PROM memory and 1K of RAM. For simple control applications you may not even need add-on memory.

If that isn't enough to convince you, how about this? This card also has four vectored interrupts, switch-selectable I/O ports, variable clock frequency (2 and 5MHz) and a phantom line.

16K PROM Memory Card for just \$300.

Everything in this card is the best you can find. The PROMs are reliable, 2708-type designed by TI. The board is high-quality FR4 glass epoxy with fully-buffered address and data lines and plated-through holes. You can choose from 0-4 wait states (selectable by DIP switch). You can also address any 4K group of memory to any 4K boundary. This bank select feature allows you to control up to 8 banks of memory.

A SIDE BY SIDE COMPARISON—INTEL, VECTOR GRAPHIC AND ARTEC

Feature	Intel SBC/8030	Vector Graphic MZ	Artec Centurion
Clock speed	2.7 MHz	4MHZ	5MHz
Onboard monitor	yes	no	yes
Hardware floating point	no	no	yes
Onboard memory	8K PROM 16K RAM	none	3K PROM 1K RAM
Onboard regulators	no	yes	yes
Board size	6.75" x 12"	5.3" x 10"	5.3" x 10"
Onboard ports for keyboard and RS232	yes	no	yes
Price	\$1298	\$215	\$850

No question about it, this is a tremendous card for the money. The card without memory is just \$125 with all the sockets in place. The EPROM chips alone are \$11 each.

8K-32K Expandable RAM memory just \$175-\$620.

We've used a fine, Texas Instrument designed chip, the 4044. Start with the board and 8K of memory and then add on as your application grows. The board holds up to 32K of fully static memory. It has bank select and the same high-quality PC board construction techniques as the PROM card.

The 8K board costs just \$175; 16K is \$315; 24K is \$475; and the 32K board is \$620. 8K add-on kits are \$135. Single TI 4044 chips are \$7.

A rugged card cage built around Artec's Totally Silent Motherboard

Some people argue for passive termination, others for active termination. All I know is that we have the motherboard that is totally free from spurious noise at 2MHz, 4MHz, or 5MHz.

More than twice as thick as most motherboards you can find for the S100 bus, this is the best possible start for a reliable control system.

The card cage itself is made out of 12 gauge anodized aluminum for solid support and protection of your investment. Available in 6, 8, 10, 12, or 16 slots.

Breadboards for people who like to do it themselves— \$20

For just \$20 each these breadboards are incredible. You can find every board you need including copper clad boards with no holes, wire wraps, and two with plated-through holes that are set up for different pin arrangements.

Call me and let me tell you more about this system

If you still have questions about this system, call Artec Electronics, Inc. at (415) 592-2740. Ask for Bob Jones, and tell the person who answers you want to talk about his computer system. Or use the coupon if you don't have time to call. Our address is 605 Old County Rd., San Carlos, CA 94070.

Either way, don't sit there wondering if I'm crazy or not. Find out for yourself by calling or writing today.

ARTEC

O.K. Bob, convince me, get in touch with me and tell me more about your computer system.

Name/Title _____

Address _____

Company _____

City _____ State _____ Zip _____

Phone _____

Mail to: Artec Electronics, Inc.
605 Old County Rd., San Carlos, CA 94070

THE MICROPROCESSOR INTRODUCED NEW KINDS OF BOARD TEST PROBLEMS.

Old ways of testing IC boards don't work very well on MPU-based products. So far, attempts to fill the testing gap have proved expensive or inadequate. Or both. And they usually need an engineer to run them.

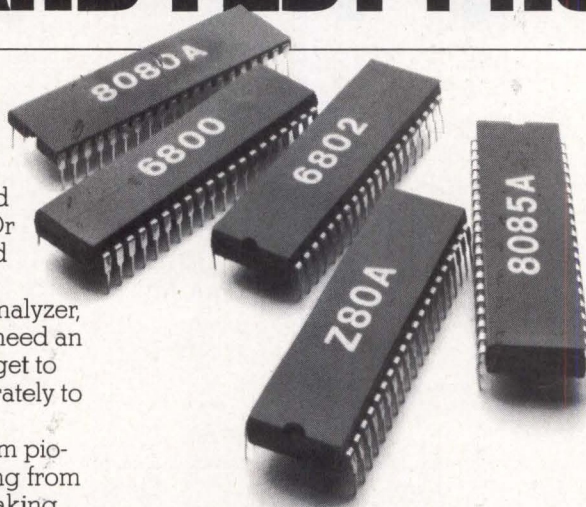
The MicroSystem Analyzer, on the other hand, doesn't need an expert or a five-figure budget to troubleshoot fast and accurately to the node level.

To do this, Millennium pioneered the concept of testing from the inside out. Instead of making edge connections or using a bed of nails, you unplug your microprocessor and plug our system right into your MPU socket. To test any board or node with which the μ P can communicate, just push a couple of buttons, and you're off and running at system speed up to 5 MHz—so you catch more faults. And in a true system environment.

Simple programming; exhaustive testing.

It doesn't take much preparation to run complete system testing. In a short time, using your system's microprocessor language, programs can be ready to do Go/No testing of your digital and hybrid boards, and with a Signature Analysis, trace a fault down to a defective node.

To make things even easier, you can easily modify your existing diagnostics to run on the MicroSystem Analyzer.



The low price of success.

This new approach to testing also breaks some cost barriers. With a starting price of \$4000, you can afford to share your test, QA and maintenance loads. And, when you change to a different microprocessor, all you do is change the low-cost personality cards in the Analyzer.

For factory-field compatibility, your service force can also take it right to the customer, replace only defective boards on-site, spearhead repairs at your local office, using factory level diagnostics to reduce that board float problem. The MicroSystem Analyzer also has an optional RS232 capability, making it ideal as a test station or for remote field service.

Millennium's filling the gap.

The MicroSystem Analyzer is a significant first step in making the MPU-based product easier to test.

For μ Ps and μ Cs past, present and future.

Here Today	More Tomorrow
8080A	8048
8085A	8049
6800	8035
6802	8039
Z80A	8748
	8021
	and more

Our other two products, the MicroSystem Designer and MicroSystem Emulator, will help engineers get their jobs done better, faster and cheaper, too. So you can look to Millennium for the new ways to solve the new microprocessor problems—all the way from MPU evaluation and product development to system test and field service trouble-shooting.

Get your hands on.

It's easy to see whether the MicroSystem Analyzer is all it's cracked up to be. We'll arrange a hands-on demonstration for you. Just call or write to Barney Hordos, Millennium Systems, Inc., 19020 Pruneridge Avenue, Cupertino CA 95014. Phone (408) 996-9109. We'll send you complete information, including our new 24-page "**Guide to Testing Microprocessor-Based Systems and Boards**".

With all the new microprocessors around, the MicroSystem Analyzer is the only true test.

MILLENNIUM

a subsidiary of American Microsystems, Inc.

CIRCLE 38 ON INQUIRY CARD

MILLENNIUM INTRODUCED A NEW KIND OF BOARD TEST SOLUTION.

The 20-character alphanumeric display can be programmed to lead the operator step-by-step through your test, and tells what's happening in simple statements like "RAM error LOC 0802."

Status indicator lights let you know things like: "Is your system clock working?"

You can do long distance trouble shooting by phone with our remote communications option.

Run your test program at full clock rate, or single step through a program. Or loop on a special subtest for those hard-to-find intermittent faults.

Most tests only need a couple of keys to run. The other keys are there to give you greater flexibility for more in-depth testing.

Take out your MPU, plug us in, and your test is underway.

In-circuit Emulation is the key to our system's universality. To test a different MPU-based system just change the Emulator.

Probe detects faults using Signature Analysis, transition counting and time domain analysis.



Multiprocessing Adds Flexibility to Business Computer Family

BC/7-900 uses a different processor to provide 1.5 times the speed of the /7-800, and offers 262,144 bytes of MOS memory, compared to 131,072 bytes for the /7-800. Adding power to the BC/7 family from Sperry Univac, PO Box 500, Blue Bell, PA 19424, the 900 model performs in a multiprocessing environment, handling four jobs concurrently to supply flexibility particularly at peak processing periods.

Secondary storage capacity of 40M bytes is available on two 20M-byte disc drives, a further 4M-bytes from diskettes. The 20M-byte capacity drive offers removable disc cartridge

capability and requires only one cabinet for the 40M configuration, reducing floor space, electric power, and heat dissipation.

The unit is compatible with the -800, which can be upgraded in the field. All software presently in use on the -800 and all existing peripheral equipment can be used on the -900 model without modification. Additional benefits of the system include printer spooling transparent to application, a file sharing feature that extends to all users, and user program size up to 48,152 bytes.

A typical system consists of 262,144 bytes of main storage, 40M-bytes disc capacity, diskette unit, and four workstations. Purchase price is \$76,587. First deliveries are planned for second quarter 1980.

Circle 183 on Inquiry Card

Text Processor/Editor Packages Run On Portable Computer System

Software that simplifies the preparation, editing, and production of documents on the Miniterm[®] model 1206/dos portable computer system includes text processor and editor packages. The system, introduced by Computer Devices, Inc, 25 North Ave, Burlington, MA 01803, combines text manipulation features with random access storage in a portable unit that provides transmission over dial-up telephone lines to final production system.

User prompting messages allow persons having no computing experience to perform various interactive tasks in addition to text processing. Text processor and editor software permit documents and blocks of text to be stored and retrieved using user specified labels. Stored material can be merged into a primary document automatically to generate personalized correspondence.

Dynamic margin adjustment, tabulation, text centering, and text justification routines accommodate requirements for multiple column widths. Page lengths can be specified and headers and numbers inserted automatically. A single keyboard command adjusts left margins and page header (number) locations to left and right of page. The system can also generate indexes and tables of contents under user command and can drive any RS-232-C compatible printers.

System hardware includes a 64k processor programmable in BASIC, 128-char ASCII keyboard, 80-/132-col 50-char/s thermal printer, disc controller, and communications interface. All are enclosed in a carrying case small enough to fit under an airplane seat. The disc controller supports up to four Minifloppy double-density minifloppy disc drives to provide up to 1.44M bytes of random access storage. The unit is priced at \$7075.

Circle 185 on Inquiry Card

Packaged Systems Lower Cost of Dispersed Data Processing Operations

ARCPAC systems increase the attractiveness of dispersed data processing by offering complete computer systems at substantial savings. Available only as complete units, the attached resource computer system packages are composed of modular ARC system components (see *Computer Design*, Feb 1978, p 28) and differ only in the amount of disc storage provided. Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284 provides system and timesharing software, industry standard programming languages, and all necessary cabling with each unit.

Model 4724 includes 20M-bytes cartridge disc storage while the 4754 has 120M bytes. Both systems include five 3810 Dispersed Processors, one 6600 Advanced Business Processor, and the necessary interprocessor bus components—six 9483 Resource

Interface Modules plus a 9484 Active Hub, and cabling.

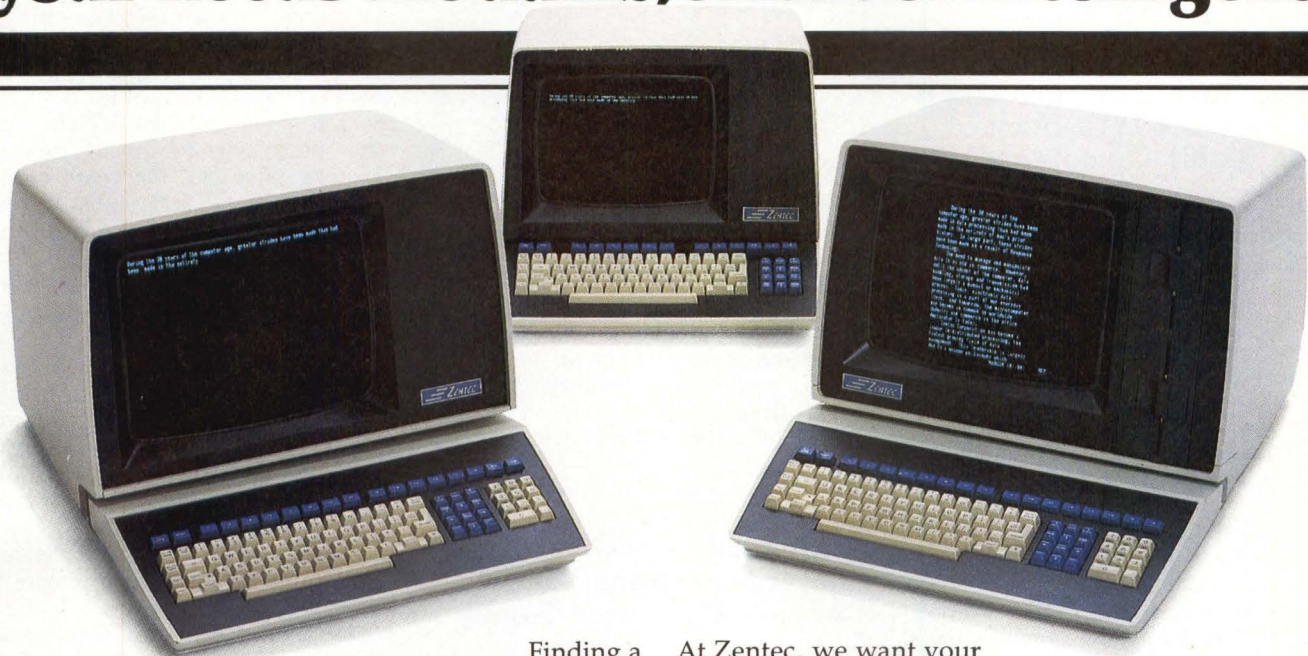
The 3810s are the applications processors of the system and feature 60k-bytes user memory, 1920-char video display screens and typewriter style keyboards. The 6600, with 120k-bytes user memory, 960-char screen, and typewriter keyboard, acts as the system's file processor.

Software is comprised of ANSI Interactive and batch COBOL, BASICPLUS, and RPGPLUS, along with the DATABUS[®] business programming language, and DATASHARE[®] business timesharing language. Also part of the software package is the DOS disc operating system plus DOS utility programs including EDIT, LIST, SORT, and INDEX. Additional software telecommunications support is provided by DATAPOLL[®] for datapoint to datapoint networks.

Model 4724 has a purchase price of \$58,950; price for the 4754 is \$84,950. These prices include software license fees.

Circle 184 on Inquiry Card

Considering alphanumeric terminals? Our I.Q. test can determine whether your needs are dumb, smart or intelligent.



Finding a source for alphanumeric terminals is relatively easy. Finding the right terminal isn't necessarily so easy.

That's where our I.Q. Test can help.

Numerous questions must be answered before you can specify the optimum terminal for your data or word processing system. Should it be dumb? Smart? Or intelligent? Clustered or stand alone? Do you need local processing capability? Expansion RAM, ROM or PROM? Should it be user programmable? Or can you pre-program it to satisfy your system's requirements? The handy I.Q. Test inside our new ZMS Family brochure can help us help you find the

	Dumb	Smart	Intelligent	Your Requirements
Local CPU Processing	No	No	Some	
User Programmability	No	No	Some	
Expansion RAM	No	No	Some	
Expansion ROM/PROM	No	Some	Yes	
Displayable Characters	64	64-96	128-256	
Video Attributes	Limited	Some	Some	
Screen Character Matrix Resolution	5x7	7x8	7x9	
"Soft-Font"	No	No	Some	
Down Load Capability	No	No	Some	
Printer Capability	Some	Some	Yes	
Mass Storage Capability	No	No	Some	
Protected Data	No	Some	Yes	
Higher Level Languages	No	No	Some	

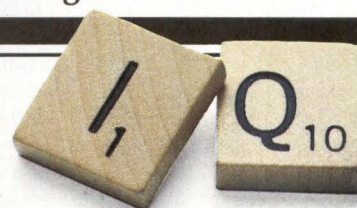
answers to these basic questions. And more. Here, you'll also find detailed information on our new ZMS Family of intelligent terminals: the ZMS-50, ZMS-70 and ZMS-90 . . . three intelligent solutions to your system design problems.

At Zentec, we want your first terminal choice to be your most intelligent choice. So we'd like to assist you in reviewing your basic requirements. And help you analyze your system needs. If intelligent terminals are the answer, we'll help you determine which ZMS terminal best fits your system requirements. Or how you can best modify our modular designs to satisfy your specific application. We'll also help you weigh other selection criteria than just hardware. Like custom configurations. Customized firmware and software. And specialized interfaces and protocols. All to insure that the terminals you specify offer you the best price/performance ratio money can buy.

Looking for an intelligent alternative?

If you'd like to find out more about how Zentec intelligent terminals can provide intelligent solutions to your data

or word processing problems, send for our free ZMS Family brochure. Then take the I.Q. Test. Write: Zentec Corporation, 2400 Walsh Avenue, Santa Clara, CA 95050. Or call (408) 246-7662. It may be one of the smartest moves you've ever made.



CIRCLE 159 ON INQUIRY CARD



... the last word in intelligent terminals.

SOFTWARE

FORTRAN Compiler Meets ANSI X3.9-1978, Runs On 32-Bit Computers

Part of a FORTRAN product family introduced by Systems Engineering Laboratories, Inc, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313, FORTRAN 77+ meets ANSI X3.9-1978 standards, supports MIL-STD-1753, and provides comprehensive structured FORTRAN. Developed to run on the company's series 32 line of 32-bit computers, the FORTRAN family is supported by RTM and MPX-32 realtime operating systems, and is designed to exploit 32 series hardware capabilities to improve total system performance.

Primary features of the FORTRAN 77+ compiler include FORTRAN based, Pascal based, realtime based, and industry based extensions that improve program efficiency while reducing development costs. Extensions are highlighted by structured programming features like DO UNTIL and BEGIN-END constructs. In addition to filling ANSI X3.9-1978 requirements, the compiler also meets or exceeds MIL-STD 1753 and ISA S61.1 and S61.2 standards.

In addition to FORTRAN+ the family incorporates an integrated hardware/firmware/software version of the scientific runtime library (Scientific Accelerator) and two Softool performance analyzers. When combined with FORTRAN 66+, a highly optimized 3-pass processor that supports a superset of ANSI X3.9-1966 FORTRAN IV, and with the software runtime library, these products form a comprehensive family that satisfies users' performance requirements while protecting software investments.

A comprehensive set of subroutines that provide operating system services, the scientific runtime library supplies mathematical library routines, and language extensions for FORTRAN 66+ and 77+. It is available as a standalone product for execution-only systems without a FORTRAN compiler.

The scientific accelerator provides all scientific RTL features plus fully integrated hardware, software, and firmware to significantly improve FORTRAN program execution speeds. Performance up to 30% better can

be obtained by linking to accelerator routines rather than RTL.

Softool Instrumentor Utilities aid in optimizing and debugging programs. Reporting on execution times and usage frequency of FORTRAN programs, they operate on the source program to determine how much time each statement or subroutine has spent executing. This enables realtime users to pinpoint most critical performance bottlenecks and logic flaws.

Circle 181 on Inquiry Card

Extended Pascal Implementations Execute Across Computer Family

In implementing Pascal for use with Data General computers running under the Advanced Operating System (AOS) Rational Data Systems, 245 W 55th St, New York, NY 10019 has provided a structured language that is compatible with the entire line—from Eclipse to microNova. All versions are source compatible and each can cross-compile for any of the other systems.

The compilers generate code for a hypothetical computer with an architecture optimized for Pascal execution. The instruction set for this computer is based on 8-bit bytes which are executed by the computer's interpreter. Each 8-bit instruction expresses a high level operation, greatly reducing memory space requirements. By using a dense byte oriented code to represent programs, the implementations can significantly increase the number of users and size of programs that may remain memory resident before swapping occurs. This results in less system overhead and quicker response times.

Five distinct implementations are included in the family. Each is optimized for a particular environment but is source compatible with and capable of cross-compilation for execution by any other implementation. Each can be configured to take advantage of specific hardware and software available. Such options include Eclipse, Nova, or microNova processor; hardware or software multiply/divide; hardware or soft-

ware floating point; and Eclipse character or commercial instruction sets.

AOS, the first available implementation, is a high speed, single-pass recursive descent design that includes compile time source text "include" facility. Runtime facility is in the shared code partition. This means that no matter how many users are running programs, there will be only one copy of the interpreter in memory. No binding or loading is required. Output of the compiler is immediately ready for execution, thereby significantly reducing program development time.

This version includes these extensions to standard Pascal: string variables and intrinsics similar to those within PL/1; decimal variables for business applications; and terminal files to simplify interactive programs. Ability to randomly access files easily extends to ISAM and VSAM. Segment procedures and functions within the compiler permit a program to be divided into as many as 16 pieces that are handled automatically by a load-on-call mechanism, thus permitting execution of programs too large to fit into main memory. Another extension provides access to the host operating system facilities via a generalized SYSCALL procedure.

Implementations that complete the family are: RDOS/DOS single-user that requires a minimal system configuration; RDOS/DOS multiterminal in which all terminals execute common code (for dedicated applications such as order entry); and RDOS/DOS multiuser via swapping which provides a low cost system, typically for turnkey systems. In addition, RDOS multiuser via extended memory is a higher performance system that adapts to number crunching applications with many users and fast response time requirements.

Speeds of the compilers vary depending on version and host system environment, but all are faster than most language processors available for Data General computers. As an example, using an S/130 processor running AOS with a 10M-byte disc, the compiler can compile itself in 8 min. A typical 1-page program (50 lines) compiles in less than 11 s.

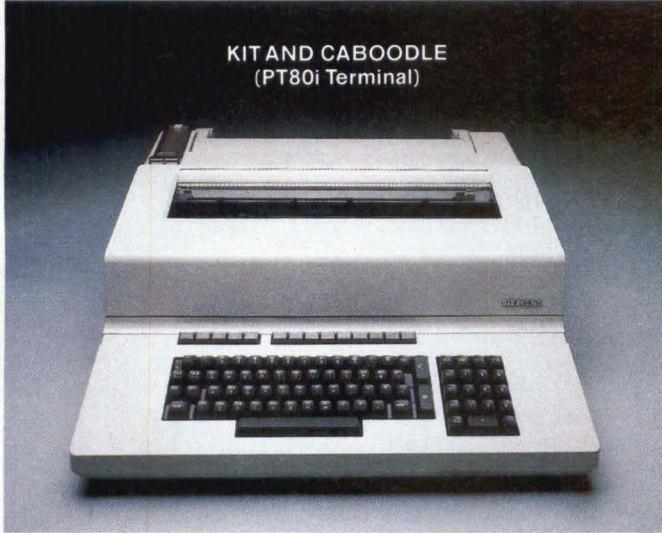
All implementations are provided on Data General compatible floppy discs or 9-track magnetic tape. The AOS version is priced at \$3500. Copies may be obtained on 5M-byte top loading cartridges for an additional \$200/copy.

Circle 182 on Inquiry Card

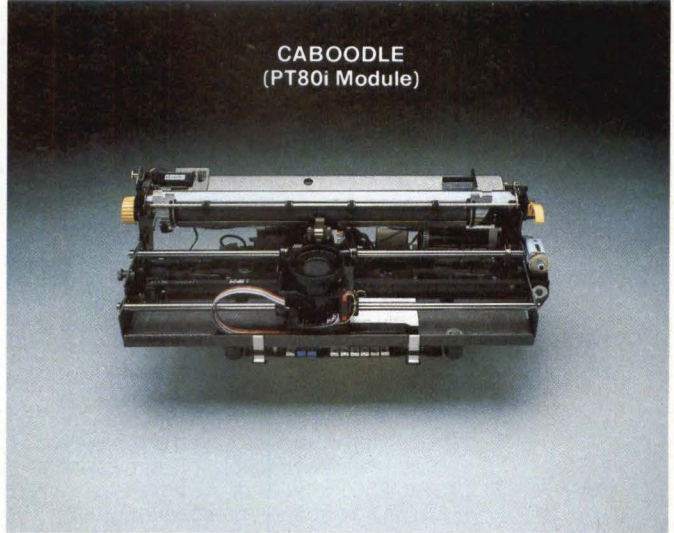
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When it comes to data acquisition systems, there is nothing quite like the ADAC System 1000 and the new System 2000.

Both systems can operate as low cost peripheral expanders to any UNIBUS computer. When incorporating a DEC LSI-11/2 or 11/23 microcomputer the systems operate as stand alone control systems or as remote intelligent terminals.

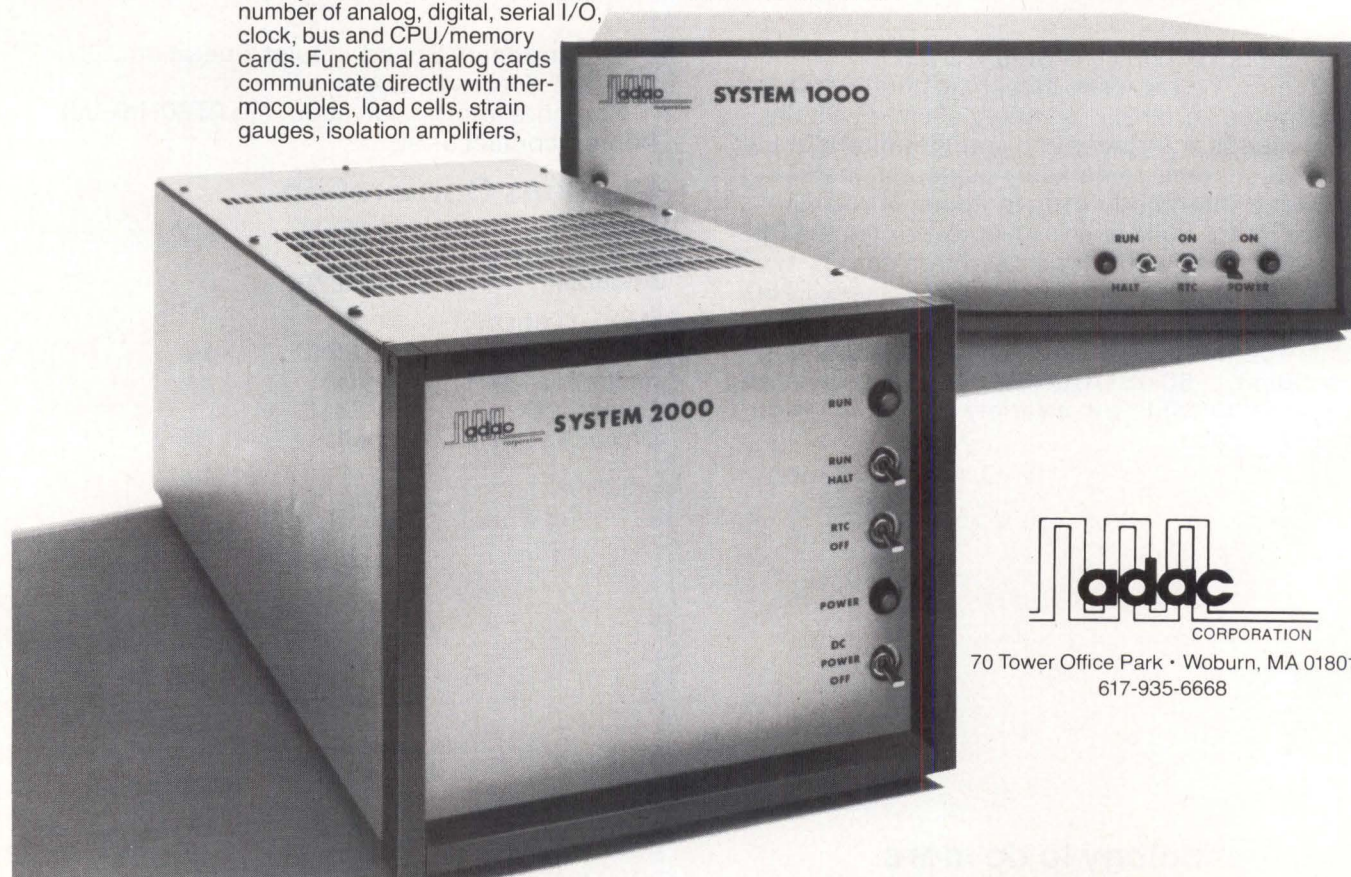
The compact System 2000 is built to hold 13 half quad cards. If you need greater capacity, slave units can be utilized or you can go to the larger System 1000 which accommodates any combination of 11 quad size cards or 22 half quad size cards. Both systems can be bench top or rack mounted and have a universal power supply that can support up to 256 kilobytes of memory.

The real heart of both System 1000 and System 2000 is their incredible number of analog, digital, serial I/O, clock, bus and CPU/memory cards. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers,

transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and other devices. All cards can be purchased as separate items.

A single System 1000 can be supplied with up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. A typical System 2000 contains a CPU, 64 kilobytes of memory, floppy disc controller, 16 channel A/D, 4 channel D/A, 32 TTL I/O lines, two serial I/O ports plus room for another six cards of your choice.

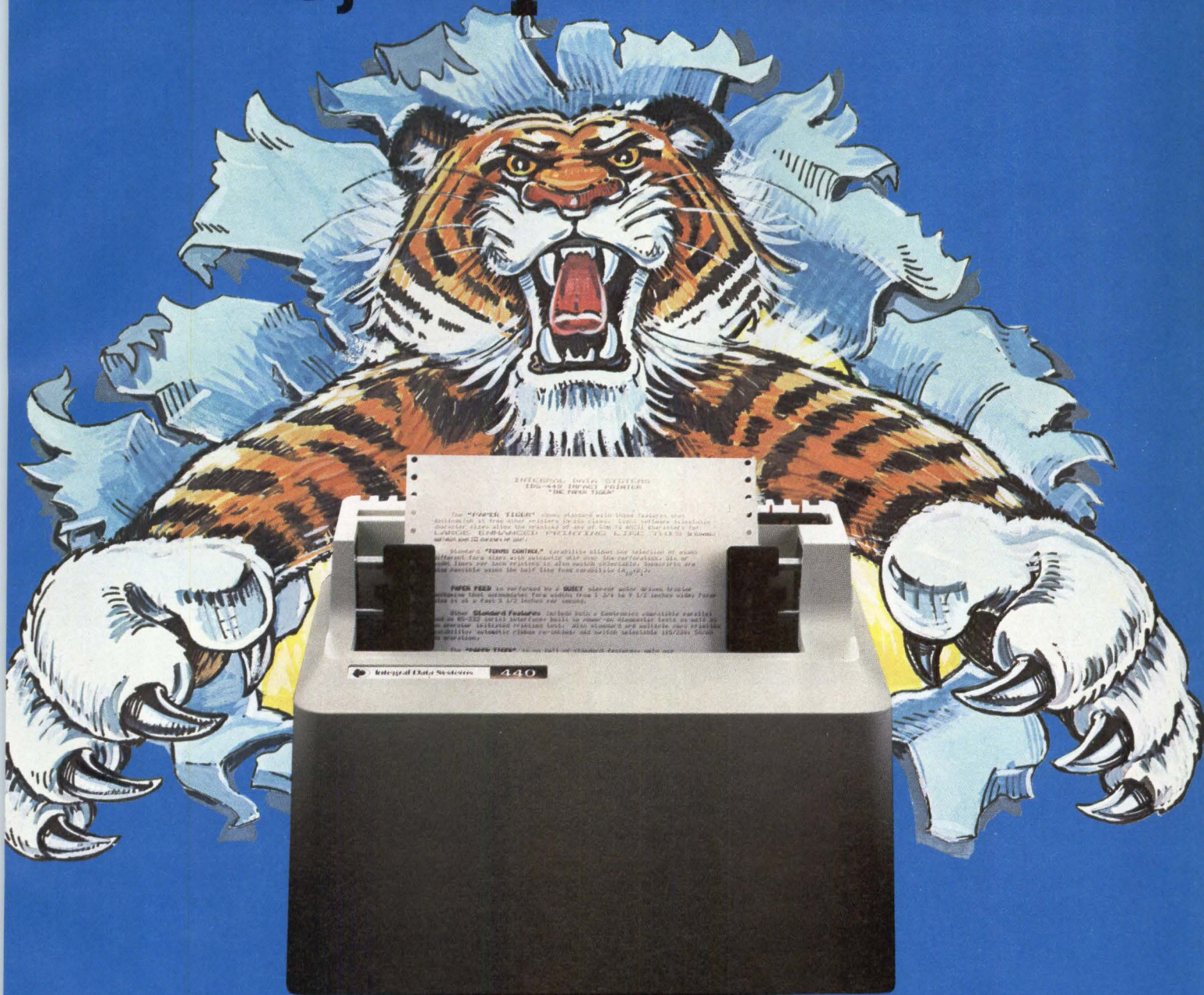
Another nice thing about both systems is their prices. They start at \$995 for the System 2000 and \$1550 for the System 1000. So you can choose the combination of price and capability that's just right for your application. Contact ADAC for full details.



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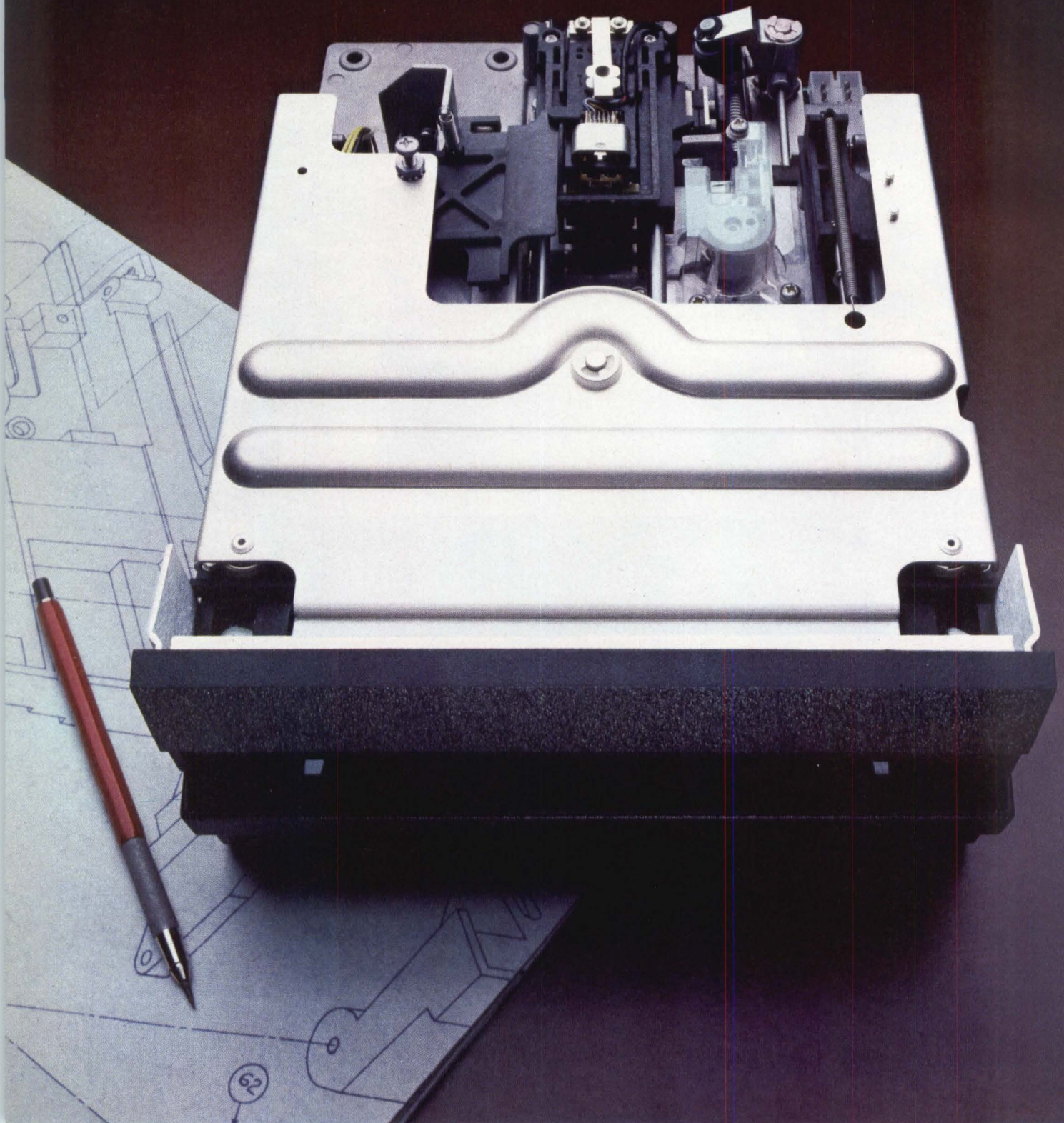


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When diskettes went double-density, and later double-sided, drive manufacturers tried to adapt their original single-sided technology.

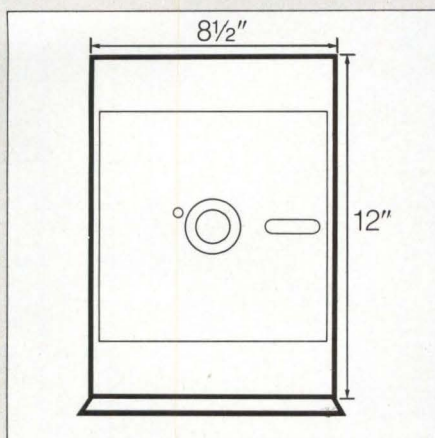
But at MFE, we saw that the old technology would simply be stretched to its limits. It was time to start again.

So based on where diskettes already were, and where they were headed in the future, we designed an entirely new disk drive from the ground up. For totally new levels of precision.

And the results are dramatic.

Our drive not only handles double-sided diskettes with ease, it even anticipates still greater disk densities — such as double-track and quad-density designs.

SMALLER IS BETTER.



The smaller package is a more stable base for high density disks.

We started with the packaging scheme.

If you lay a standard 8" diskette on top of the MFE drive, you'll discover that the drive is barely larger than the diskette itself. It actually approaches the theoretical minimum size for a drive.

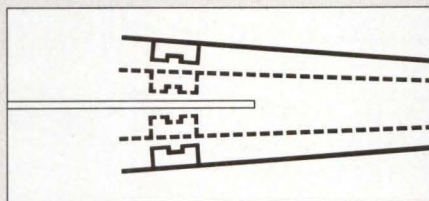
By keeping internal dimensions small, we achieved the tightest mechanical tolerances of any drive on the market. For example, only 3.4" separate the disk spindle from the stepper capstan, a reduction of 54% over the largest selling drive. And the baseplate, on which everything else is built, is a full 2 1/2" to 3" shorter. So no moving part in the drive moves further than it has to.

And since we were designing from scratch, we made the entire drive

modular. You can get to all the important components easily, and remove them without scraping your knuckles or taking apart the drive.

The new packaging alone yielded significant improvements. But we went much further.

THREE KEY INNOVATIONS.

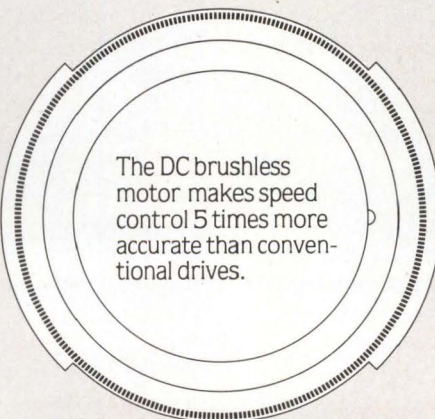


IBM-compatible head eliminates scoring. Both heads move when unloaded.

1. To handle the double-sided problems, we designed a true IBM-compatible head, including tunnel erase. Both heads, when unloaded, move completely away from the diskette surface, eliminating any head or media wear.

2. We introduced a unique half-step positioning motor that drastically reduces error tolerances in track registration. Because the motor takes 154 steps per diskette side, instead of the usual 77, it operates far more smoothly and more accurately. In fact, it is 3 1/2 times more accurate than the largest selling drive. And it's designed to be able to handle twice the number of tracks per inch.

3. Finally, we developed an optional DC brushless motor. In one stroke, we reduced speed variation of the disk spindle from 2% to a mere 0.4%. We decreased power consumption by 30 watts, and increased drive efficiency by



The DC brushless motor makes speed control 5 times more accurate than conventional drives.

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Bit Slice Approach for Small Stack Processor Aids Design of Blending System

Gene A. Cummings

The Foxboro Company, Foxboro, Massachusetts

Gerald S. Miller

California Automation, Incorporated, San Diego, California

Control systems for high speed process operations often necessitate design of dedicated processors in order to provide the required power and flexibility. Often, of course, the manpower costs of such designs can be spread out since the resultant processors might fit the needs of other systems built by the company.

In the case of a high speed blending system for handling up to 24 components in either batch or continuous organization, the processor design was based on a bipolar bit slice approach. By utilizing microprogramming techniques, useful features could be incorporated from higher level systems and applications software.

Basic requirements—common to such process control and automation applications—include efficient use of program and data memory space; support of byte, word, and floating point data; and adequate computational power, including floating point. In addition, the system must provide efficient realtime input/output (I/O); support for multitask programming and interrupt handling;

and a means for sharing system resources such as buffers, I/O devices, and the central processing unit (CPU) between tasks.

To meet these requirements, and yet do so with a relatively small processor, a microprogrammable bit-slice approach using the AMD2900 family of circuits was chosen. The decision was made in part because The Foxboro Co already utilized those circuits in several of its other processors and thus company personnel were familiar with them.

System Design Features

Model 99S micro-BlendTrol™ monitoring and control system (Fig 1) was designed specifically for batch or continuous blending operations. Basic portions are an input section that conditions pulse input signals from flowmeters, converts analog input signals into digital format, and reads digital (contact closure) inputs; a computation section that receives these data as input to



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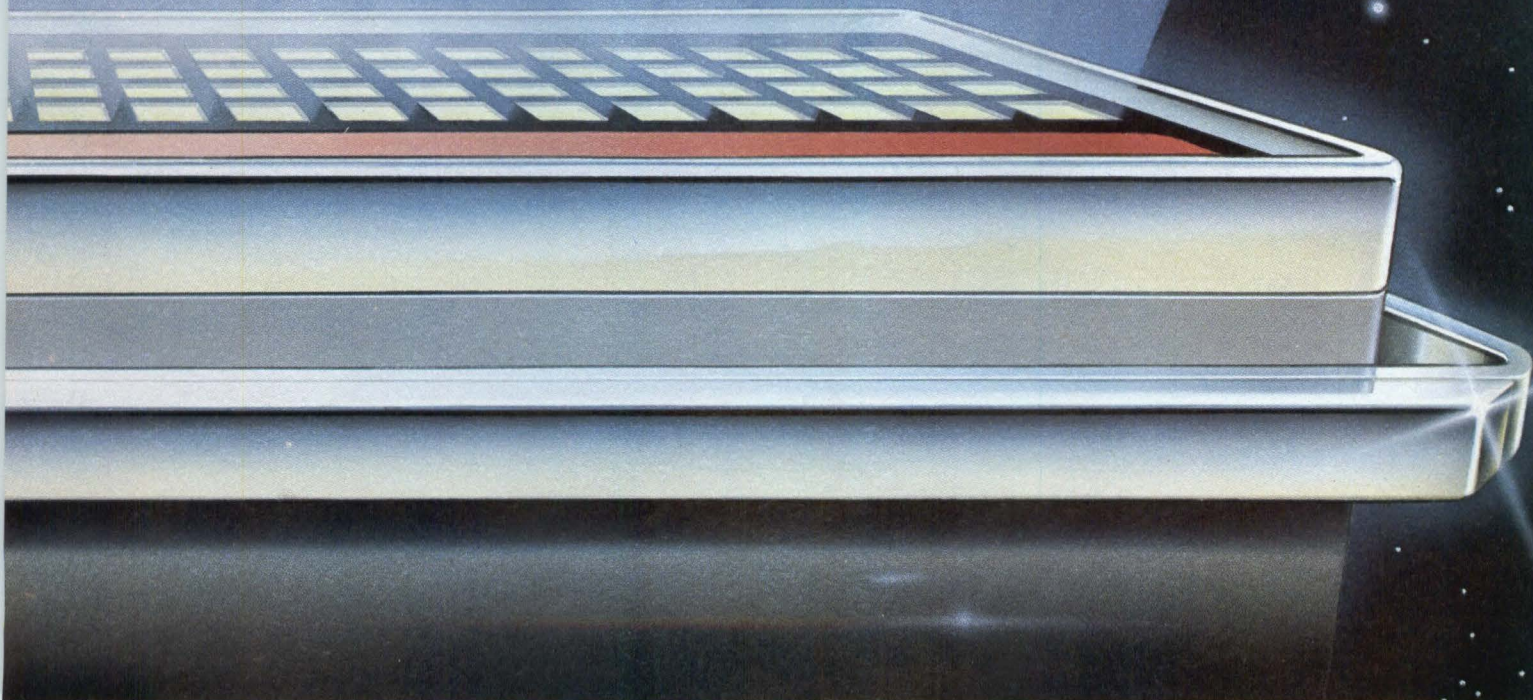
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control algorithms in the programmable read only memory, calculates a new output value for continuous comparison to demand rates, and outputs alarm and blend status signals; and an output section that converts the new digital value to an analog signal for control purposes so that automatic adjustments can be made to maintain total blend specifications, and that drives alarm and blender status indicators. An operator's control panel enables the operator to enter tuning constants, to read or set the process variables, to define system and loop options, and to control the blender; a video display allows operators to monitor and evaluate the principal parameters more easily; and a communication interface enables loop data to be uploaded to a host or downloaded to a blender.

Core of the system is a microcoded processor (Fig 2) which drives a 16-bit data bus serving both memory and I/O devices. A 16-bit address bus allows either 8-bit byte or 16-bit word addressing on even byte boundaries. Address space is either 64k 8-bit bytes (at words 0 to 32k) or 64k 16-bit words (words 0 to 64k).

The arithmetic unit is 16 bits wide, made up of four AMD2901 arithmetic logic unit (ALU) bit slices. In addition to internal registers, a memory address register doubles as the instruction register and a mode register

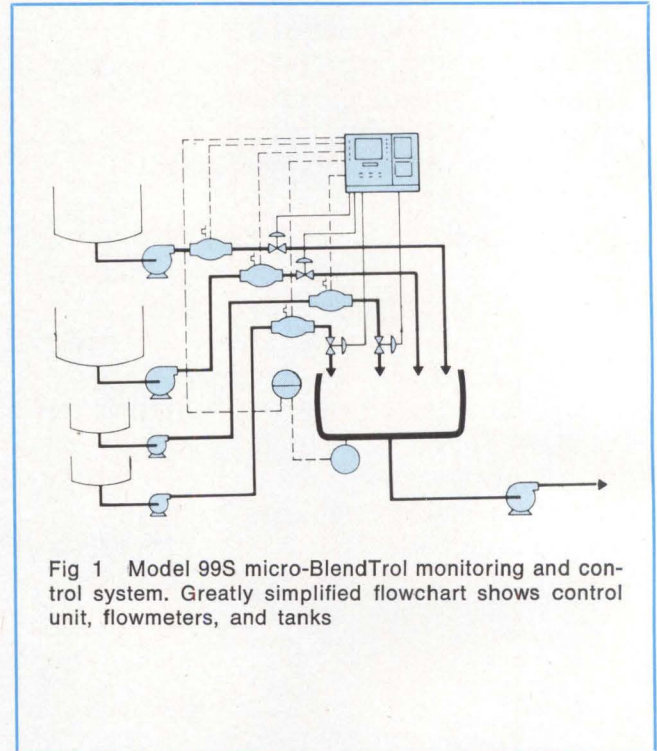


Fig 1 Model 99S micro-BlendTrol monitoring and control system. Greatly simplified flowchart shows control unit, flowmeters, and tanks

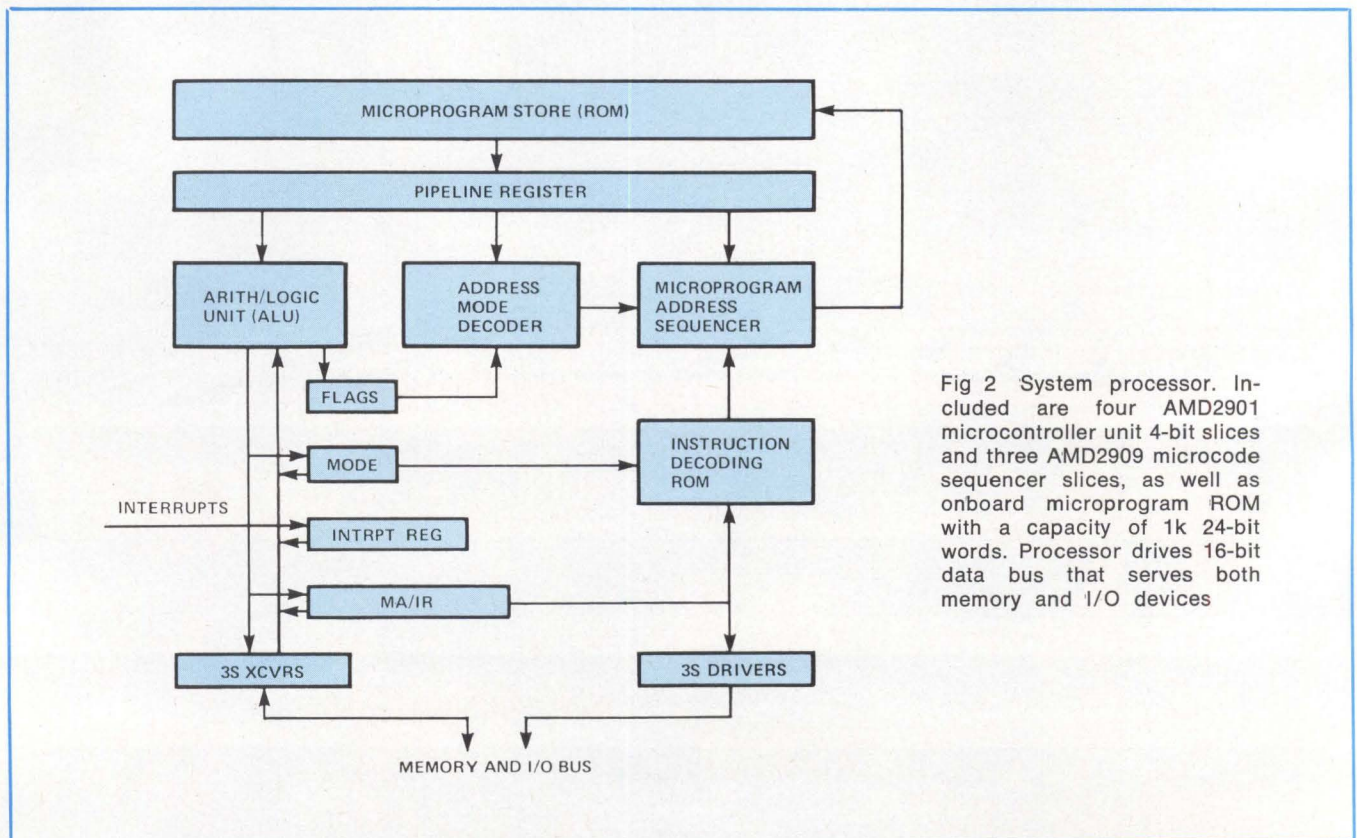


Fig 2 System processor. Included are four AMD2901 microcontroller unit 4-bit slices and three AMD2909 microcode sequencer slices, as well as onboard microprogram ROM with a capacity of 1k 24-bit words. Processor drives 16-bit data bus that serves both memory and I/O devices



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provides an additional two bits to the instruction decoding as a function of the current data type being processed. Three AMD2909 microcode sequencers and a programmable logic array (PLA) generate addresses for the 1k of onboard microcode read only memory (ROM).

A 7 x 11" (18 x 28-cm) printed circuit board contains the entire processor. By also packaging memory and I/O on similar boards, the entire system was contained in a small enclosure similar to a cathode ray tube (CRT) terminal.

Organization of the microcode instruction format is designed primarily to permit the speed of simultaneous data and branching operations while minimizing the width of the microprogram control store required. Encoding of the 24-bit microinstruction, shown in Fig 3, accomplishes this through four different formats specified by a 2-bit field at the leftmost end of the word.

One format is devoted entirely to unrestricted arithmetic operations and another entirely to full address range branches. Of the two remaining formats, one allows a limited subset of the arithmetic operations while branching within a local page and the other permits similar operations as well as a multiple return to the macroinstruction fetch routine. The latter uses a separate mapping ROM to decode the machine language instructions (as modified by the arithmetic mode register) and branch directly to the proper microcode for their execution.

One advantage made of the microcoded machine is aimed at reducing the I/O hardware by substituting microcoded operations for the battery of pulse counters normally required for the flowmeters. The counters are kept instead in main memory and updated by high speed I/O routines triggered by interrupts serviced directly in microcode. Thus the microlevel machine is shared be-

tween the macrolevel instruction execution and these transparent counter routines.

Because of the flexibility and power inherent in microprogramming, a number of "wish list" features from higher level software could be added to its machine language operations. The choice of a stack architecture for the macrolevel machine was a fundamental part of this.

For example, use of the stack as a working space for temporary data and an implicit address for instructions allows control algorithms to be coded directly in Polish notation. Operands either are pushed onto the stack from other memory locations or reside there as the result of the previous operation. An operation such as ADD then adds the two data words on the top of the stack and replaces both words with the resultant sum. This becomes an operand for further operators or may be returned to a regular memory location. The generality of such operations permits identical instruction coding for variable byte, word, or floating point data types.

As a complement to its stack architecture, the processor also includes a higher level means of accessing data via descriptor tables. The descriptor is a location containing an address pointing to the actual data as well as a 2-bit field specifying its data type. Since the 6-bit descriptor table index can be packed into the 1-byte instructions pushing data onto the stack, data can be more efficiently addressed by this means. Also, by using such data references, the CPU can be automatically set for the appropriate arithmetic mode (byte, word, or floating point) according to the data type placed on the stack.

Perhaps the most outstanding feature incorporated in the firmware is the multitask program scheduler and interrupt handler, normally a part of operating system software (Fig 4). This feature is particularly useful in

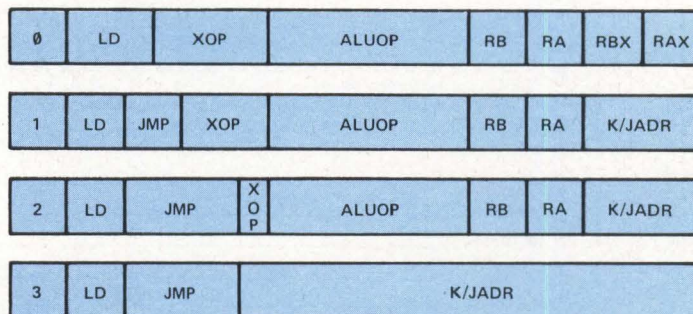


Fig 3 Microinstruction encoding. Four different microcode formats are determined by coding of 2-bit field at leftmost end of word. Sharing microcode fields in specialized combinations of functions minimizes microprogram storage



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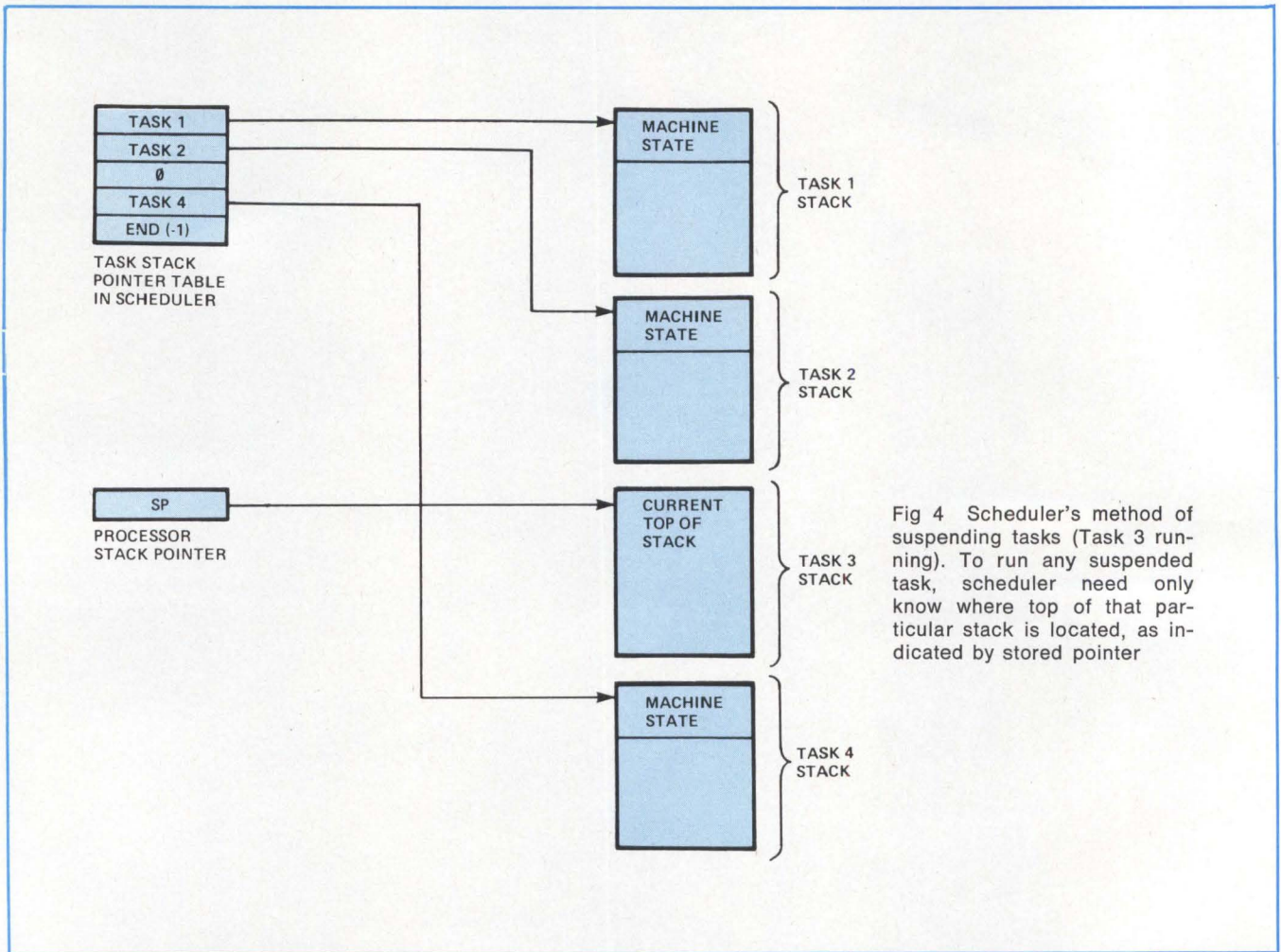


Fig 4 Scheduler's method of suspending tasks (Task 3 running). To run any suspended task, scheduler need only know where top of that particular stack is located, as indicated by stored pointer

realtime control systems to allow independent programming of the various activities that must take place—and interact with each other—in real time. The firmware scheduler automatically resolves their conflicts based first upon the system resources they require and then upon task priorities, and schedules their shared use of the processor. One task program will always be running in the processor at any time and the remainder will be suspended, their context stored as if interrupted, in various stages of completion.

Once these resource dependencies are programmed into each task, the programmer can treat them independently and the scheduler will handle their realtime interaction. Tasks are normally released from suspension either by the other tasks or by the interrupts which make the resources for which they are suspended available. Even the realtime clock can be treated as such a resource, thus allowing tasks to be run at regularly scheduled intervals such as once a second.

Controller Tasks

A standalone multiloop controller in the blender system contains keyboard, CRT display, communications inter-

face, and analog and digital I/O. Individual tasks of the software configuration (Fig 5) are assembled as independent programs. A short initializer links the tasks to the scheduler, turns on the interrupts, and places the system in run mode.

The communications task is interrupt driven from the communications I/O interface. Multiple blenders can be connected to one communications line. Each blender is given a number by the user, which is entered using the blender keyboard. All blenders on a line listen to commands from the host, but the only blender which responds is the one having the identification number matching that in the command from the host.

A communications I/O driver buffers all messages to and from the host. The driver does not request the communications task to run until a complete message has been received or sent. At this time, the communications task either processes the message received from the host if waiting for a command, or sends the next line of the reply (if any) for the command it is currently processing.

Possible commands from the host include downloading, uploading, requests for selected data from a specified loop, requests for selected data from all loops, and



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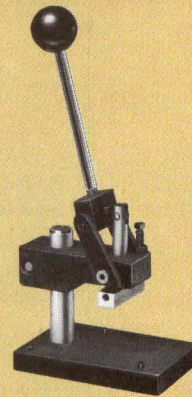
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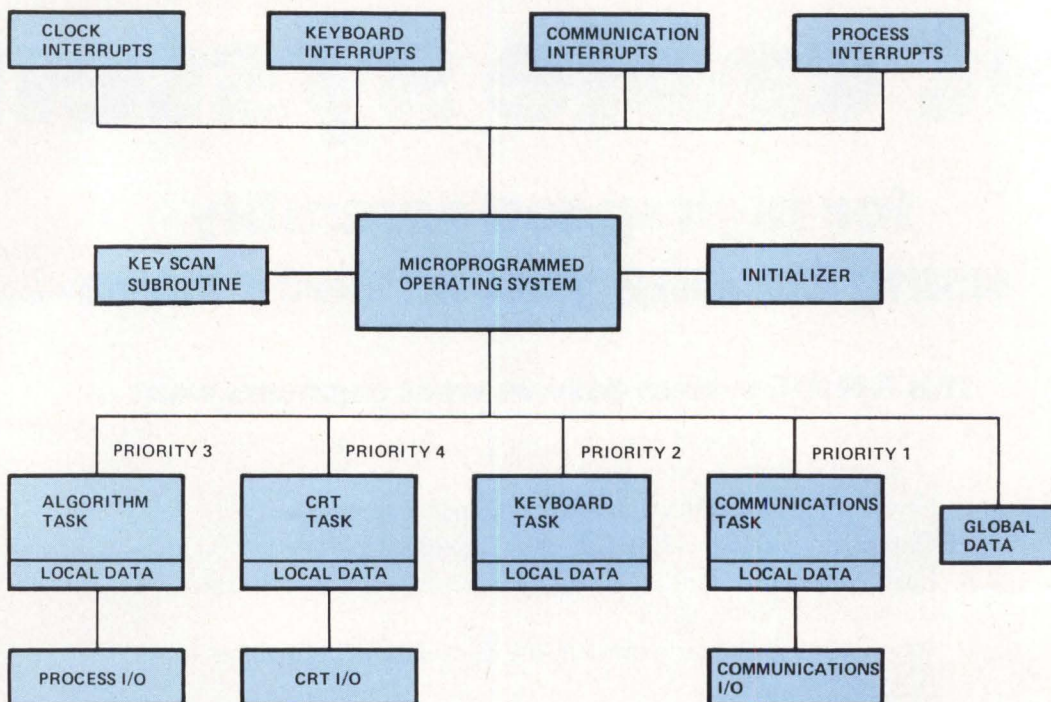


Fig 5 Software configuration. Individual tasks are assembled as independent programs, each competing for system resources according to its priority. CRT task—with lowest priority—runs only in free time

changing selected data in a specified loop. Download and upload data messages are sent as strings of hexadecimal ASCII characters in which two characters represent the binary value of one byte of data. Each download or upload record contains the record number, 60 hexadecimal characters, and a checksum.

The addressed blender always responds to each command from the host, either with an ACK for successful execution, a NAK for unsuccessful execution, or the requested data for those commands which request data. A total of 20 main commands is provided.

A keyboard task runs only when a complete command has been entered by the user at the blender keyboard, as determined by the keyboard scanning subroutine. This subroutine is called from the clock interrupt and executes a 3-state algorithm to identify a valid key, accept the key, and proceed to identify the next key. When a complete command has been entered (which can be a single key for some commands) the keyboard task is requested, through the microcoded executive, to run.

The keyboard task parses the commands, checks the parameters (if any), and makes context checks. If legal, the keyboard task then executes the command. Some commands have two cycles, in which the first cycle selects data to be displayed and the second cycle accepts

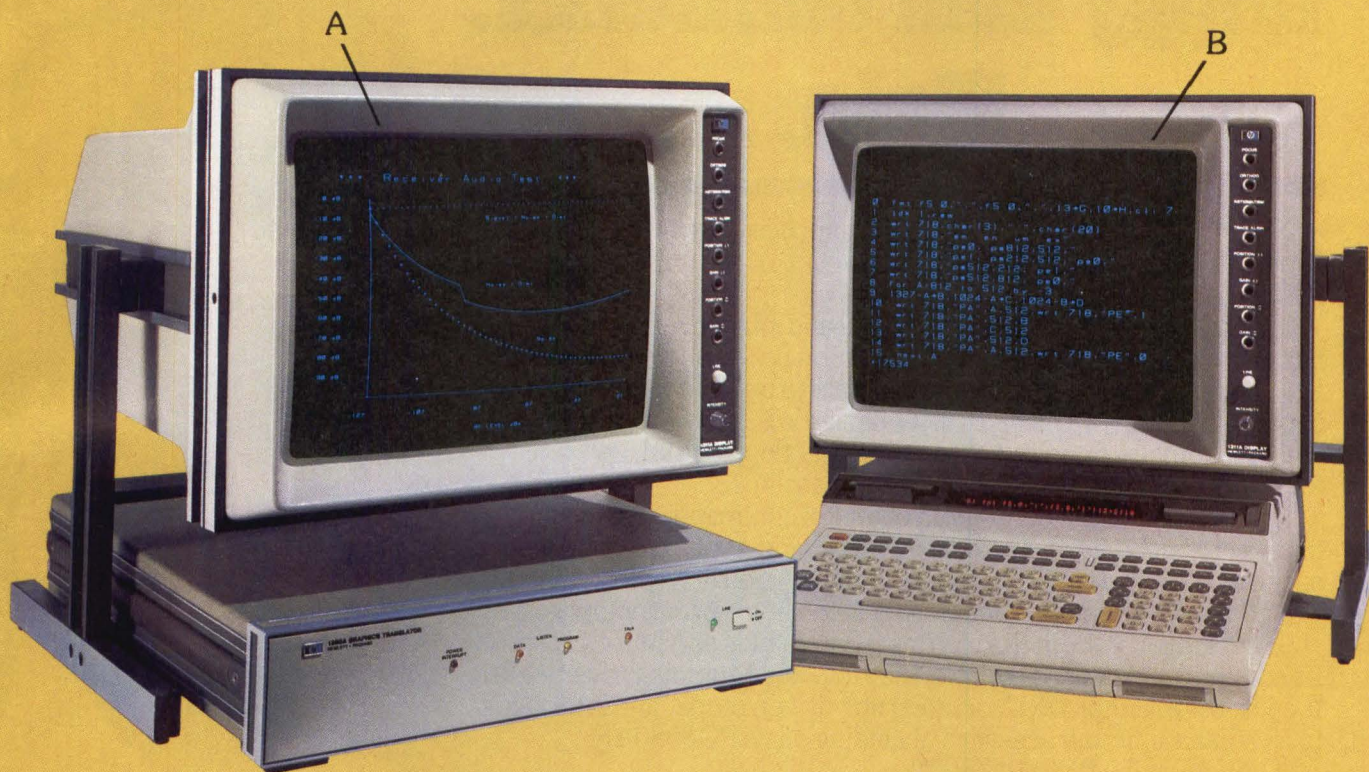
a new value to store for the selected data. All of the program codes and loop address functions are 2-cycle commands. Data types which can be displayed and entered are binary masks, integer and floating point numerics, and ASCII strings.

All blender loops and control blocks are created and parameterized through the keyboard task. Also, all of the blend control buttons such as START, STOP, LOCAL, and COMP are processed by the keyboard task. A total of 116 program functions is provided, in addition to the dedicated key functions.

The algorithm task periodically processes all of the active blender loops and calculation blocks defined in the blender system. Each blender loop is executed every 0.1 s, and each calculation block is executed at the period assigned by the user. The algorithm task itself is requested to run each 0.1 s by the clock interrupt.

For each active blender loop, a transformation from turbine meter counts to control valve position is computed. The turbine meter counts used are those which have accumulated in the most recent 0.1-s period, and thus represent the flow rate increment received by that loop for that period. Variables which may be displayed or changed from the keyboard include loop name, loop engineering units, specific gravity, loop turbine meter K

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088/12

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It's powerful too, executing 15 complex commands including many subroutines usually found in a disk handler software package. Plus it controls up to four double-sided drives.

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For board applications, you get all the capabilities above and more. The BP-2190 board includes the 765 and 16K of dual-ported RAM (expandable on-board to 48K), along with priority and refresh logic. Disk-to-RAM transfers are under DMA control



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CD-2

factor, loop normalization factor, proportional gain, integral (reset) gain, high and low flow alarm limits, plus and minus quantity error alarm limits, plus and minus quantity error shutdown limits, loop pacing parameters, and valve position. All values and variables are entered in engineering units or customarily used units such as proportional band (PB).

For each active calculation block, an algorithm corresponding to the block type is executed. The block types include analog input, proportional/integral control, analog switch, contact input, equation, and constant. All parameters can be entered or displayed through the keyboard, in customarily used units, and the blocks may be linked together or to blender loops by keyboard selection. General parameters include period, block name, block units, and on/off status. Other parameters specific to the block type include hardware address, proportional gain, reset time, contact number, input designations, operands, and operators.

The CRT task selects and formats all of the displays presented on the CRT. It also checks the blend loop alarm limits and shutdown conditions, and calculates the rates for blend ramp up and ramp down.

This task is requested once each second by the clock interrupt. Each CRT display contains a static and a dynamic part. The static part contains those fields which do not change once they have been output, such as loop

names and engineering unit labels; it is output only when a new display is selected. The dynamic part is output with the static part, and then each 1 s thereafter.

Other Processor Applications

The small stack processor originally designed for the micro-BlendTrol application has also been used in the company's other products. For example, it controls the universal field multiplexer, a data acquisition system used in the SPECTRUM™ distributed process control system; and the same hardware emulating another instruction set appears in the MICROSPEC™ unit controller module.

While the loss of some speed owing to the extra memory accesses required for stack and descriptor operations makes it unsuitable for certain applications, the processor easily regains the advantage in any application that makes effective use of its higher level machine code. Obviously such code runs much faster than similar software programmed in a more conventional machine language. Such considerations would make it very adept at running higher level language interpreters, for example. Its use in products to date, however, has been limited to applications where dedicated machine language programming of small realtime process control systems has made its minimal use of memory and multitask operating system its most useful features. □

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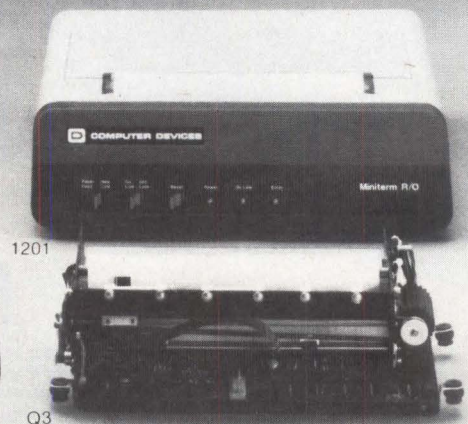
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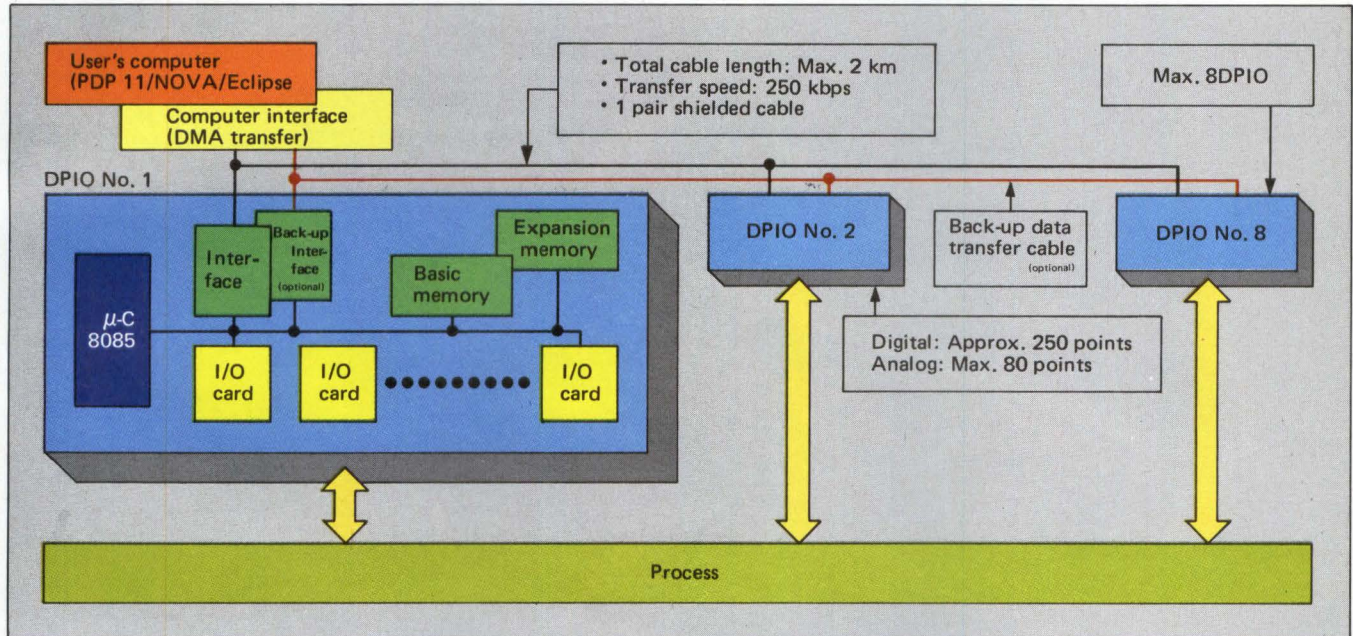
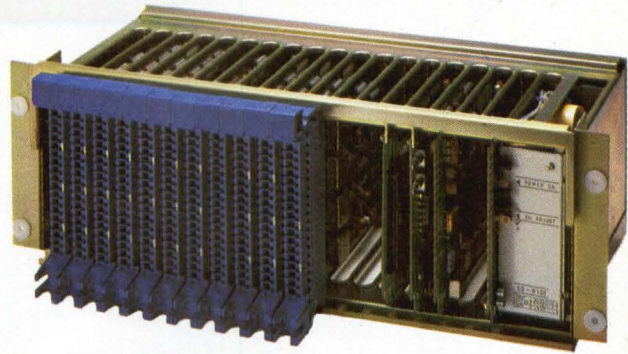
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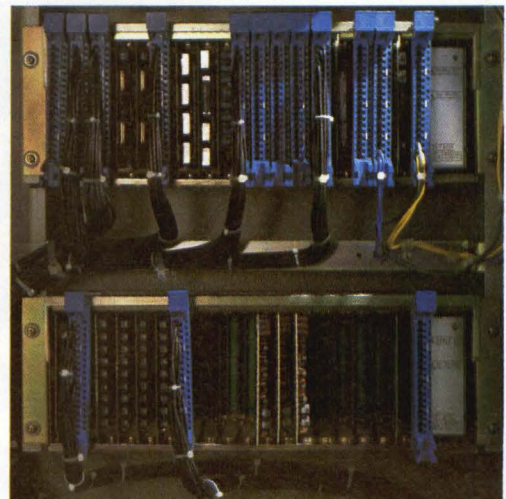
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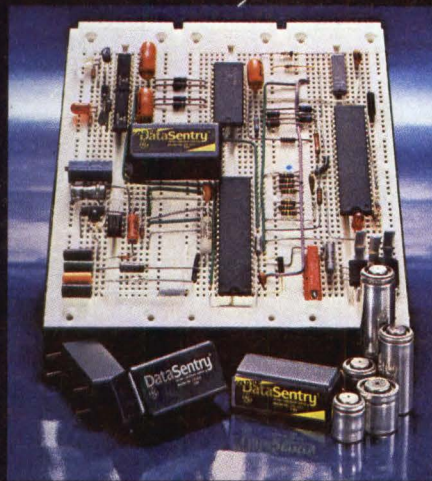
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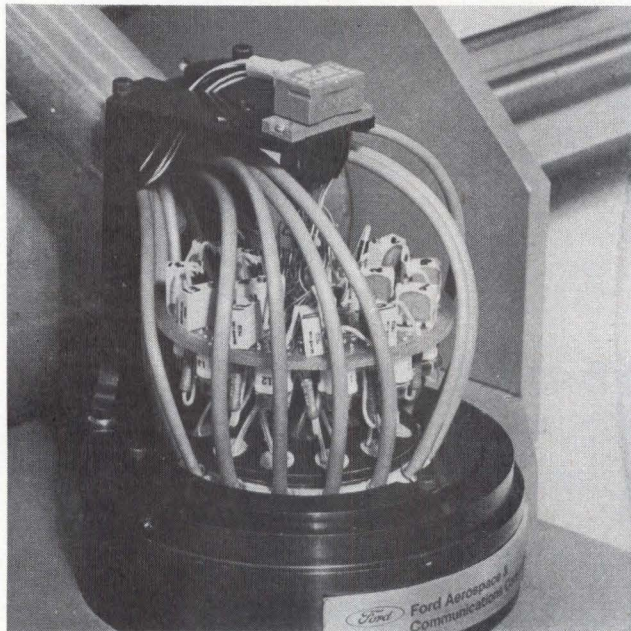
Spectrophotometer System Analyzes Fabric Dye Shades Online

"On-the-run" adjustments to dye ranges—while the fabric is moving through the processing equipment at over 100 yd (91 m)/min—are possible with the Qualscan system installed at Greenwood Mills' Orangeburg, SC finishing plant. During a period of several months of continuous operation, over 10M yd (91M m) of cloth have been scanned.

In standard industry practice for textile dye house operations, 18" (46-cm) swatches of fabric are removed periodically, sewn together, and examined in a specially lighted area—by a human—for color shade acceptability. Because the production and material handling equipment is stopped only once every 2000 or 3000 yd (1800 or 2700 m), all cloth between stops might be defective.

The computerized online color analyzer, introduced by Ford Aerospace & Communications Corp, Process Control Products Operation, Charlotte, NC, electronically scans moving fabric and spots off-shade colors. There is no stopping of equipment, human-element decisions and possible variations in interpreting standards are eliminated, and color deviations are noted immediately.

Designed to provide color measurement by large scale fabric finishers for use on continuous dye ranges, the digital abridged spectrophotometer system contains a precision scanning color head that traverses the width of the cloth as it leaves the dye range. Within the head



Scanning color head (cover removed to show detail) in Ford Aerospace's fabric color analyzer. Data from 16 color sensitive silicon detectors are compared to shade tolerance thresholds in computer memory. Fabric illumination is provided via fiber optic light pipes

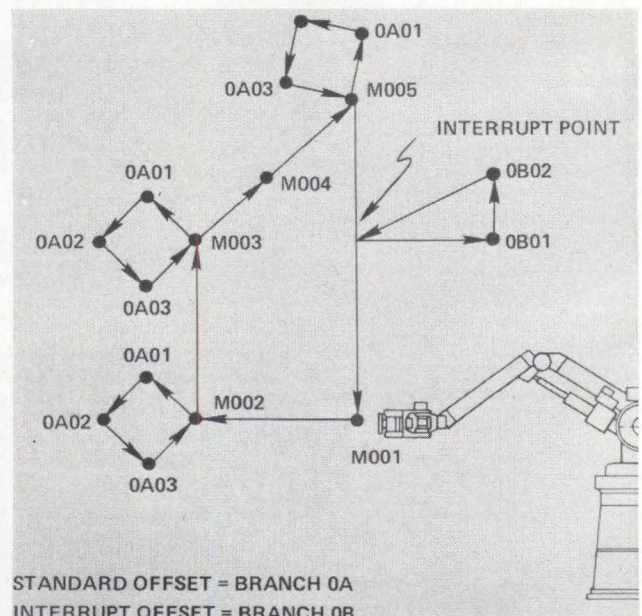
are 16 color-sensitive silicon detectors behind precision color filters of very selective bandwidths. To eliminate drift and instability in the color detection circuitry caused by heat from the light source, a remotely located quartz halogen lamp uses fiber optic light pipes to illuminate the fabric inspection area. Built-in reference standards check scanning head accuracy every 30 min.

In the procedures to locate shading inconsistencies, the system scans long runs of dyed fabric in side-center-side (across the fabric) as well as end-to-end procedures. Color information is presented to the dyer as a continuous CRT readout and as hardcopy on a high speed printer. Deviations from color shade values assigned by the dyer and placed in computer memory as shade tolerance thresholds are automatically flashed on the screen for immediate action.

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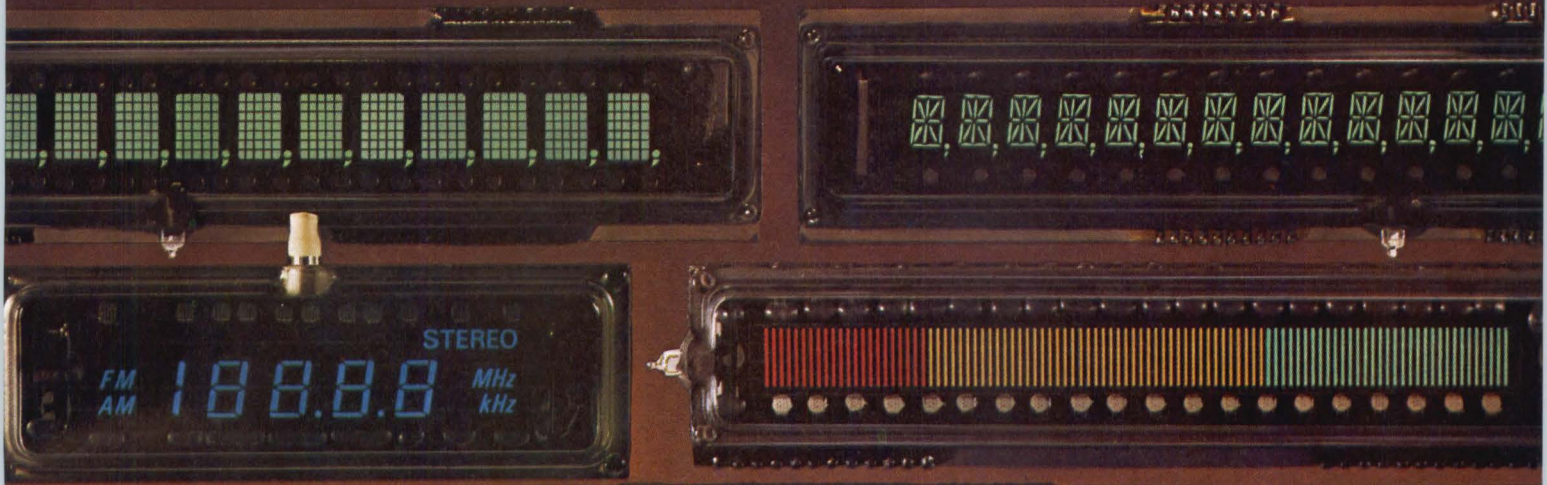
General Purpose Robot Taught to React to Unpredictable Deviations

Teaching a computer controlled T³ industrial robot to perform its repetitive duties—but yet be able to deviate for changes in normal sequences—is greatly simplified by "walking" the robot through the intended sequence of events. Cincinnati Milacron, Cincinnati, OH 45209, has found that what might otherwise become a tedious



Offset branching programming for robot cycle. At each point where offset branch is programmed, proper input signal is checked and branch is entered if input is active. Interrupt offset allows for "anywhere, anytime" shifts in cycle to allow reaction to expected but unpredicted deviations

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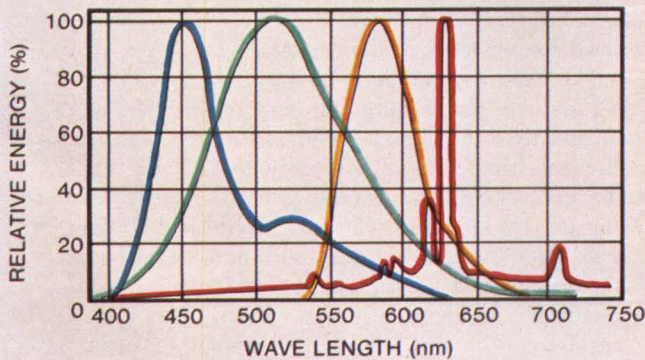
And you'll realize all the advantages offered by Itron Fluorescent units over ordinary digital displays. Their cost-effective pricing and simple, fast installation will save you time and trouble, as well as a great deal of money. Interfacing with peripheral circuits is easy too; further reducing costs. They operate at low voltage and consume little power. Their bright fluorescent output and flat-glass packages make for easy readability, at a distance and at wide viewing angles, even under high ambient light conditions.

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procedure not only eases teaching but also simplifies operation.

An example of this is shown in the robot's "branching" ability. Three types of branching—conditional, offset, and interrupt offset—enable the robot to perform secondary functions: add, change, and delete. Such ability to make decisions based on input conditions permits tailoring of a general purpose robot to specific applications.

For conditional branching, a signal from an associated equipment would cause the robot to deviate from its normal sequence and to perform one of the secondary functions. For example, if the robot were loading parts into a turning center and a signal from that center indicated that the part was not ready, that the door on the machine was closed, that the spindle was still in motion, or that the previous part was not completed, the robot would not move forward in its sequence and load another part. Instead, it would either wait or go on to another step.

Teaching offset branching is simplified by software available in the robot control. In an example where the robot is loading or unloading parts onto or from skids and pallets, repetitive moves are taught as a subroutine. After one instruction period, the robot control remembers the subroutine (including such moves as stop above pallet, move down, release part, move up) and calls it up as needed during an actual job.

Interrupt offset, known as a utility branch, can be entered anywhere in the robot cycle after being triggered by an external signal. It is actually a contingency program for reaction to expected but unplanned events. For example, if welding tips stick and weld themselves to the workpiece—an expected occurrence in a spotwelding application, but one that is impossible to predict in time span—the robot would cause the welding tips to move in a series of previously taught twisting motions to free the tips. It could also simultaneously signal the operator that the welding tips require attention.

Circle 161 on Inquiry Card

Energy Management System Reduces Natural Gas Fuel Costs by Half

Decreased consumption of natural gas and/or propane during a 6-month test period—resulting directly from the installation of an energy management system—reduced fuel bills by 50% in the most energy inefficient building in Winnebago Industries' Forest City, Iowa

complex. The company estimates that the cost savings during that period alone exceeded the cost of software development, hardware purchase, and installation. As a result, the system—designed by Billings Computer Corp, 2000 E Billings Ave, Provo, UT 84601—will be extended to the remaining 11 buildings.

In the full system, there will be at least one controlling microcomputer in each building, with very large buildings having several satellite computers connected to a master computer in order to simplify wiring to sensors and peripheral devices. All buildings will be monitored and controlled from a single keyboard in the maintenance building. Each master computer will function independently, managing its building according to a program and instruction tables and schedules loaded in from the central keyboard. Upon request each master computer will transmit status tables to the maintenance building.

At present, the system monitors temperatures at various locations in the building as well as flow rate of natural gas and/or propane into the building. All unit heaters, exhaust fans, and air make-up units are controlled according to predefined production schedules and schedules for the temperature setpoint of the building. Software also provides for error handling with alarm signals sent back to the maintenance building.

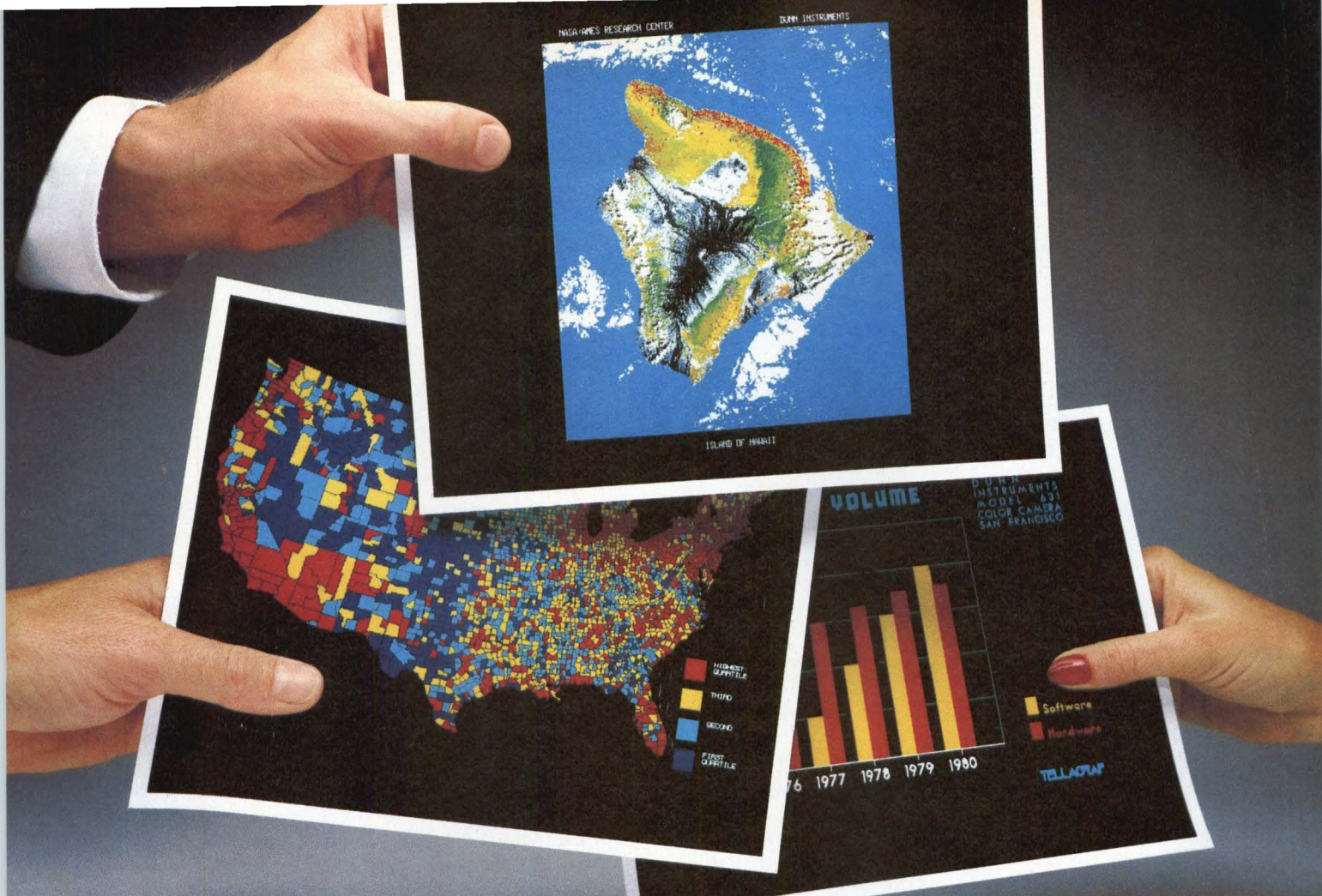
Data accumulation features in system software include current value tables, selectable accumulators, automatic accumulators, and weather station history. Requested data are summarized and saved in memory awaiting retrieval. More than 1 yr of information is accumulated in summary form of last month, last week, last day, last hour, and last 15-min intervals. As the tables fill up, the oldest information is summarized to form an element of the next higher table of the cascade.

Selectable data accumulators obtain high, low, integral, and average of a sensor output from a prespecified starting day and time to a prespecified ending day and time. The allowable time interval is 5 min to 110 yr.

Master control consists of a 64k-byte Microsystem with an external, 1M-byte, 8" (20-cm) double-sided floppy disc drive, X-Y plotter, warning light, and alarm buzzer. The system addresses 16 separate inputs (monitoring devices) with measurement accuracy within 0.1%.

A parallel I/O board allows the system to open or close circuits to 24 separate devices or sense their operating modes. A relay section attached to the board contains an equal number of amplifiers and can drive signals over twisted pair cable for up to 500 ft (180 m). For applications with remote controlling requirements, a multiple input/output board containing four high current amplifiers will drive signals over twisted pair cable for up to 2 mi (3 km).

Circle 162 on Inquiry Card

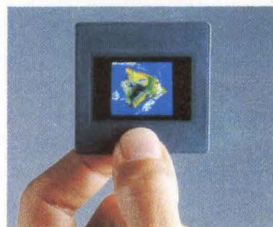


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The 631 COLOR CAMERA SYSTEM

DUNN INSTRUMENTS

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CIRCLE 56 ON INQUIRY CARD

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The PS-401 features thermal overload protection and short-circuit current limiting. Operating ambient temperature is from 0°C through 40°C. Storage is from -22°C to 50°C.

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Self-learning process modeling and dual-channel output for independent control of two process variables are features of the MPC 3030 microcomputer programmer/controller. Introduced by Thermotron Industries, Automatic Control Systems Div, 468 Cleveland Ave, Holland, MI 49423, the unit offers 50 program intervals with independent transition rate control for each channel. By continuously updating its information through monitoring the previous control action and the current process variable level, the unit optimizes control response for a setpoint change and tailors the control response to the programmed profile. Program instructions are resident and are system prompted for ease of programming and editing. Selectable Celsius or Fahrenheit temperature scales, 25-char keyboard, eight on/off TTL compatible event outputs, and failsafe protection for power transients and/or power failure are included in the unit. Options include EPROM profile storage, emergency power back-up, event relays, and keyboard lockout. Power requirements are 115 Vac, 50/60 Hz, 50 VA max. Overall dimensions are 8.75 x 19 x 17.75" (22 x 48 x 45 cm). Ambient operating temperature is from 32 to 131 °F (0 to 55 °C); standard temperature range is -125 to 375 °F (-87 to 190 °C).

Circle 163 on Inquiry Card

Interface System Based On Snap-In I/O Modules

An I/O interface system announced by Teledyne Relays, 12525 Daphne Ave, Hawthorne, CA 90250, consists of a mounting panel and up to 16 ac and dc input and output modules. Logic circuitry interconnect wiring in the mounting panel terminates in a choice of ribbon, edge card, or D-type connectors compatible with most microcomputer systems. Solid state modules for the model 674 I/O system snap into the panel without any wiring connections. Their features include optical isolation, noise immunity, and LED status indicators for troubleshooting. Output ratings are 4 A at 20 to 250 Vac, and up to 3 A at up to 250 Vdc.

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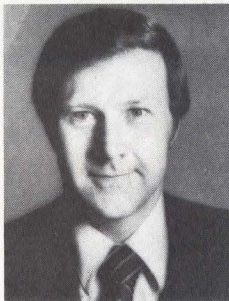
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CIRCLE 58 ON INQUIRY CARD

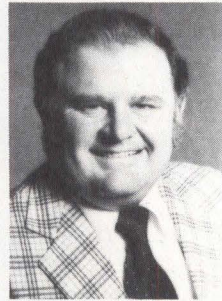


Midcon/79



James Ralston
Convention Director

Electronics Convention and Exhibition Chicago O'Hare Exposition Center and Hyatt Regency O'Hare Hotel November 6-8



Robert Betten
Program Chairman

How can the electronics industry meet the needs of manufacturing production and industrial design concerns, and what available technology can these companies utilize? With more than 40% of the United States' industrial production within a 500-mi (800-km) radius of Chicago, these questions represent an important aspect of Midcon/79. The O'Hare Exposition Center will function as the exhibit hall, and the Hyatt Regency O'Hare will be the site of more than 120 professional presentations for the 3-day convention.

Professional sessions will be held at 10 am and 2 pm, Tuesday, Nov 6 through Thursday, Nov 8. Those of interest to *Computer Design* readers deal with trends, applications, and present technology of microcomputers and microprocessors, of memories, and in control.

Featured in "Trends in High Performance Single-Chip Microcomputers" will be Synertek's sy6500/1, Motorola's mc6801, Zilog's Z8, and Texas Instrument's TMS 9940. These VLSI chips are enhanced CPUs surrounded with the elements necessary to offer a stand-alone microcomputer system on one chip. Although more expensive than their stripped down counterparts, the single-chip microcomputers offer a cost savings due to part count reduction in the overall system, and can be configured into more demanding applications.

The 16-bit microprocessor based systems to be discussed in another session are the mc68000 from Motorola, the 9445 Microflame II from Fairchild Camera

and Instrument Corp, the 16-bit microprocessor family from Zilog, and the PDP-11/23 from Digital Equipment Corp. Since some of the 16-bit system vendors are minicomputer manufacturers and others are semiconductor manufacturers, this will afford a perspective on the evolution and revolution in 16-bit microprocessor architecture.

Software for many of these systems will be discussed in "Advanced Software Tools for Microprocessor Based Systems." These include the C high level programming language for Z80 and 8080 based microprocessor systems, the IDRIS operating system, Pascal for Motorola 6809 and 68000 microprocessors with support for commercial and industrial microprocessor applications, and the Pascal MICROENGINE processor.

Strides have been made to meet the demand for nonvolatile memories—during 1979 several manufacturers will be introducing memories that allow realtime system reconfigurations of nonvolatile storage. To be presented are trends in nonvolatile memories, the device technology, an overview of the market, and applications of electrically alterable memories.

Current solutions to the problem of providing nonvolatile storage for micro and miniprocessors and for small systems will be delivered in another session. Solutions include EPROM, NMOS, battery backup of semiconductor memories, bubbles, minicassettes, and minifloppies. A third session will present advances in static, CMOS, and static and dynamic NMOS RAMs that

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have been directed toward the development of memory systems with battery backup power to retain data during power down.

Until recently, low power CMOS devices were also low speed and low performance. Advances in CMOS technology have resulted in memory components, microprocessors, and supporting components that meet low power requirements without sacrificing speed.

Although bubble memories have been promised as a usable technology for several years, current status indicates that it is just finally becoming a practical reality. Bubble memory subsystems, scaling down bubble memory devices, and contiguous disc bubble devices are the topics that will be presented.

Computer use in manufacturing processes varies from direct machine control to information handling, and the hardware to implement these applications ranges from microprocessors to large scale data processing computers. Applications that will be detailed include a distributed manufacturing information system, distributed numerical control, minicomputers for furnace control, and an information display system for a manufacturing operation.

Industrial robots, using open-loop control systems, are an accepted element in industry today. The addition of sensors and "intelligence" from the incorporation of mini or microcomputers will expand their range of applications. State of the art development in robot

control, sensors, programming language, the augmentation of man in space, and the problems of legged locomotion for robots will be expounded in the session entitled "Robots in Industry and Space."

Personal computers are finding applications in engineering, scientific, and industrial fields. Those to be discussed include a time clock/job accounting data entry system, data acquisition and control system for laboratory experiments, medical data acquisition, testing manufactured goods, establishing readability indices, and high capacity mobile telephone systems.

Computer graphics in computer aided design and manufacturing has demonstrated significant industrial productivity gains. Presented will be current computer graphics applications and considerations from the viewpoint of industrial research, hardware manufacture, the turnkey industry, and the university.

Three other sessions will present technology and trends in switching power supplies, data conversion, and CRT controllers. The present state of switching power supply technology is still not mature. New technologies include power FETs, and integration. Further developments may be necessary while safety specs call for higher isolation voltages, and emi pollution controls call for lower levels of conducted and radiated emi. A high speed bipolar DAC and a high speed microprocessor compatible ADC are among the trends in A-D interfacing to be covered. Other developments in this technology are IIL data converters, monolithic bipolar video speed data converter circuits, and high resolution low power CMOS data converters. "Directions in CRT Controllers" will present ics now available and designs being readied for production.

The 500 booths in the O'Hare Exposition Center will be color-coded into specific exhibit areas. The four color groups encompass components, microelectronics, and fiberoptics; instrumentation and control systems; production, packaging, and test equipment; and mini/microcomputers and EDP peripherals. Exhibition hours will run from 9:30 am to 6 pm, Tuesday, Nov 6 and Wednesday, Nov 7; and from 9:30 am to 5 pm, Thursday, Nov 8. A free shuttle from the Caravelle Inn in Rosemont and the Horizon parking facility near the Sheraton O'Hare will service both the Hyatt Regency and the exposition center.

The all-industry reception, "Fun and Games with Electronics at Midcon," will be held Tuesday evening, Nov 6, from 6:30 to 8:30 pm in the Hyatt Regency's International Ballroom. Refreshments and an array of electronic games will be featured. Tickets can be purchased at the door for \$10 apiece. Also to be a part of this year's Midcon is the Film theater which will screen scientific and engineering motion pictures from 10 am to 4 pm the three days of the show.

Registration for the conference will be \$5 at the door; registration before Oct 22 is \$3. For more information contact the Midcon office, 999 N Sepulveda Blvd, Suite 410, El Segundo, CA 90245, tel: 213/772-2965. Midcon is sponsored by regional and local chapters of the Institute of Electrical and Electronic Engineers and the Electronic Representatives Association. □

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MSLI-DRV11C Parallel Line Interface
MLSI-SMU System Monitoring Unit
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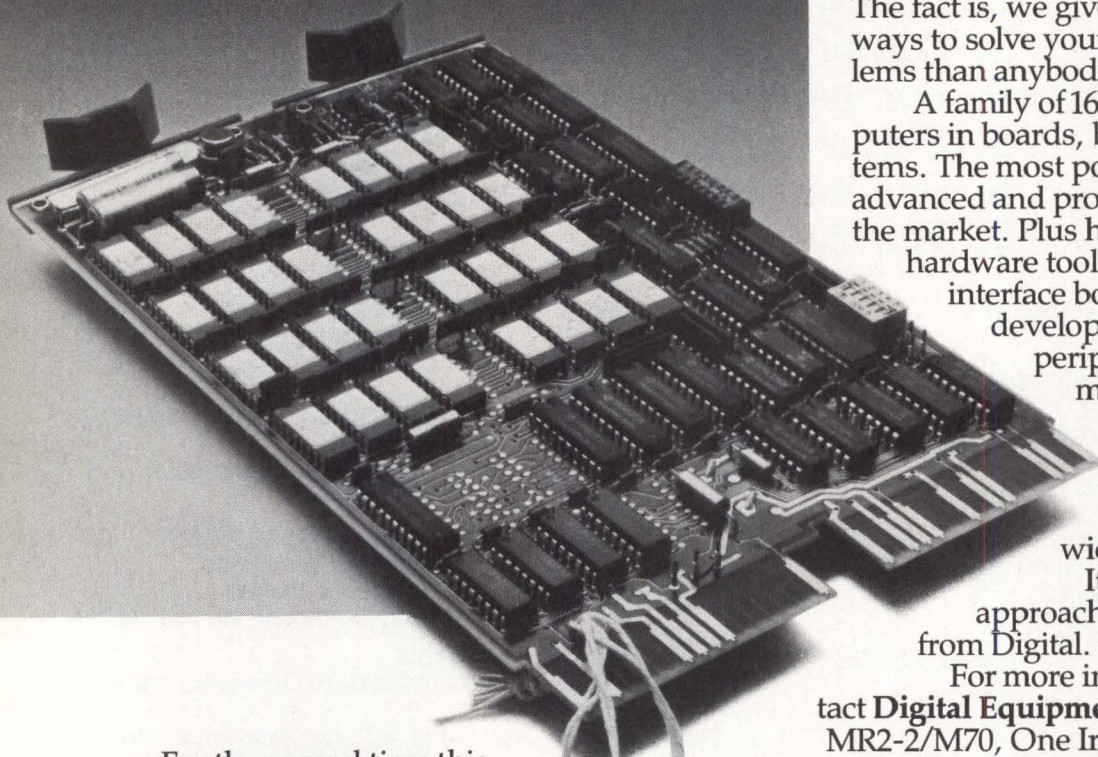
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BIT SLICE TECHNIQUE MINIMIZES MICROCONTROLLER COST/COMPLEXITY

A bipolar LSI bit slice microcontroller bridges the performance/cost gap between metal oxide semiconductor microprocessors and discrete logic in a microprogrammable digital to analog system design

David Hooley Virginia Polytechnic Institute, Blacksburg, Virginia

Many control tasks require higher speed, wider data path, or more powerful computation than is provided by metal oxide semiconductor microprocessors. In applications such as mass storage controllers, minicomputers programmed in assembly language either cannot respond fast enough or should not be burdened with low level control tasks. Other applications, such as repetitive display or waveform generation, may be relatively simple, but require an excessive amount of processor time. Designers prefer a more general purpose solution to these problems than a specialized, discrete logic system, but without the expense of a full microprogrammed bit slice processor. A suitable controller design would provide a limited instruction set with subroutine and conditional jump capabilities, a large number of bits in the instruction word that are available for control of external registers, very fast instruction execution, read/write memory for the development phase, and the ability to use read only memory or programmable read only memory after completely debugging the system.

Control tasks which fit in this category of relatively fast operation with a few simple decision points can be efficiently implemented with a versatile, straight-

forward, microcontroller design. This controller consists of a large microprogram memory for storage of microinstructions and a next address generator that supervises the conditional branching indicated by external control bits. Cost and complexity of the microprogram sequencer are minimized by restricting its instruction set and addressing capabilities to meet particular application tasks. System design time is reduced considerably because physical hardware changes are seldom made, the designer does not need to thoroughly understand all the system details before starting the design, and similar applications may require only a minor software change to enable use of common hardware designs.

Microcontroller Characteristics

A microcontroller or microprogram sequencer furnishes addresses to control memory, which then presents a sequence of logic levels to the control lines of the microprogrammed device. The microcontroller has the capability of altering program flow based on conditions generated in the microprogrammed device; thus, the

microcontroller can be viewed as a primitive processor that governs external logic.

Several types of instructions for the microcontroller are needed to efficiently control such external logic as an arithmetic logic unit (ALU) of a minicomputer, a disc or tape interface, or a digital to analog converter (DAC) used for waveform generation. Conditional jumps or branches alter the microprogram flow depending upon selected conditions in the external logic. Subroutine control instructions allow the repeated use of a group of instructions which perform a commonly used function. In this manner, the number of words in an expensive microprogram memory can be reduced in comparison with straight-line programming methods. Also, the microcontroller may need to present a number of sequential logic levels to the external device without any control decisions being made; therefore, a next instruction or a no operation instruction is needed. In addition, unconditional jump instructions provide for convenient control of the program flow.

During the development phase, a read/write (R/W) microprogram memory enables the designer to try different microprogram approaches to the control problem more rapidly than if programmable read only memories (P/ROMs) were used. After the development phase is completed and the system is debugged, the ability to store the microprogram in nonvolatile memory is necessary to avoid the need to reload microprogram memory every time power is turned off. Therefore, a practical microprogram sequencer and microprogram memory would include the capability to use both R/W and read only memory (ROM). Loading of R/W memory under the control of an external computer system is probably the most practical method of entering a microprogram into microprogram memory.

System Design Requirements

A system application for a microcontroller involves a programmable waveform generator. A repetitive, stable, analog waveform with several simultaneous digital control signals is needed to control a measurement process (Fig 1). The obvious solution to this design problem is to program the waveforms in a P/ROM, whose contents are then sequentially applied to a DAC. Extra P/ROM output lines could be used for the required digital control signals.

Before committing the waveforms to P/ROM, a considerable amount of experimentation with the timing of the waveforms and the control pulses is required; thus, R/W memory rather than P/ROM is needed for the design phase. A microcontroller design is more powerful than needed for this application, but it has the exact architecture required for a waveform generator and related control tasks. R/W memory can be loaded by a minicomputer. If a program consisting of a series of absolute next (ANXT) instructions with an absolute jump (AJMP) instruction to address 0000 at the end of the ANXT instructions is loaded, the contents of the R/W memory are continuously accessed. If a DAC is attached to the controller memory output lines, the desired analog waveforms are easily generated. Furthermore, an off the shelf microcontroller

large scale integration (LSI) chip is immediately available, whereas other devices would require extended design and construction time and cost.

In Fig 1, a 12-bit DAC is attached to the controller memory output lines. Several microcontroller external control lines (CL) furnish required control signals. Since control memory can be programmed for single-step operation, an external variable frequency clock is connected to an external reply line to control the rate of waveform generation. After the optimum rate and waveforms needed are determined, control memory can be set for continuous operation, and an appropriate crystal controlled clock and up/down counter can be applied.

The minicomputer is capable of loading microcontroller memory with the required waveform generation program and data by asserting the write enable line and loading the proper write data into controller memory, after which the program is automatically resumed by pulsing the microsequencer clear line. Obviously, the high speed capability of the microcontroller cannot be fully utilized in this situation since a 10- μ s/step clock rate is needed due to the several microsecond settling time of the DAC, rather than applying the microcontroller's maximum clock rate of 100 ns.

Microcontroller Implementation

LSI circuits which perform the function of microprogram sequencers are readily available with varying levels of software support.^{1,2} The Texas Instruments SN74S482 4-bit slice expandable control element has straightforward architecture and provision for relative addressing due to its full adder inputs.³ Although microprogram controllers can be implemented with other available circuits, the SN74S482 was chosen because of its adder characteristics.

The microsequencer consists of three 4-bit wide elements, a full adder, a 4-word first in, last out (FILO) stack, and a clocked output address resistor or latch (Fig 2). Data flow through the sequencer is directed by two select control lines for each of the three elements. The clocked output register ensures that the data output lines are stable between rising edges of the clock. Likewise, addresses are transferred to or from the FILO stack only on a rising clock edge. Information on the data input lines can be loaded directly into the output address register or can be added to the contents of the output register via the full adder and multiplexer. It is also possible to push the current contents of the output address register onto the FILO stack via the full adder while loading the output register from the data input lines, thus implementing a jump to subroutine microinstruction.³

The complete microcontroller system design (Fig 3) comprises a microprogram control memory, microprogram sequencer, instruction decoder, clock synchronizer, and input source selector. Microprogram memory contains the control bit sequences for the external device under control, as well as the control program for three cascaded bit slice elements, which are used to generate 12 address bits for the next address to control memory. The architecture is purpose-

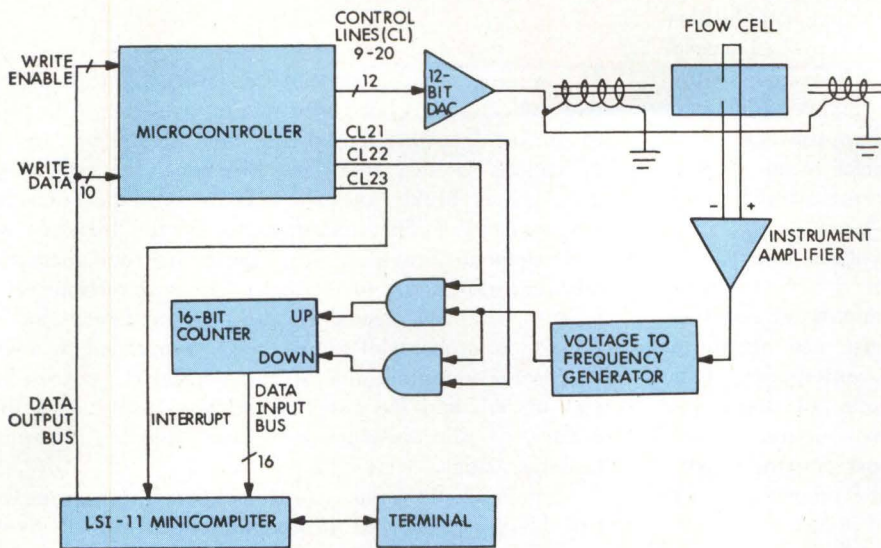


Fig 1 System design requirements. Microcontroller is applied as programmable waveform generator to relieve minicomputer of simple, but time-consuming, task of continuously generating analog signals. Several bits of micro-program memory are needed to control logic which generates digital number representing response of experimental system to various analog signals

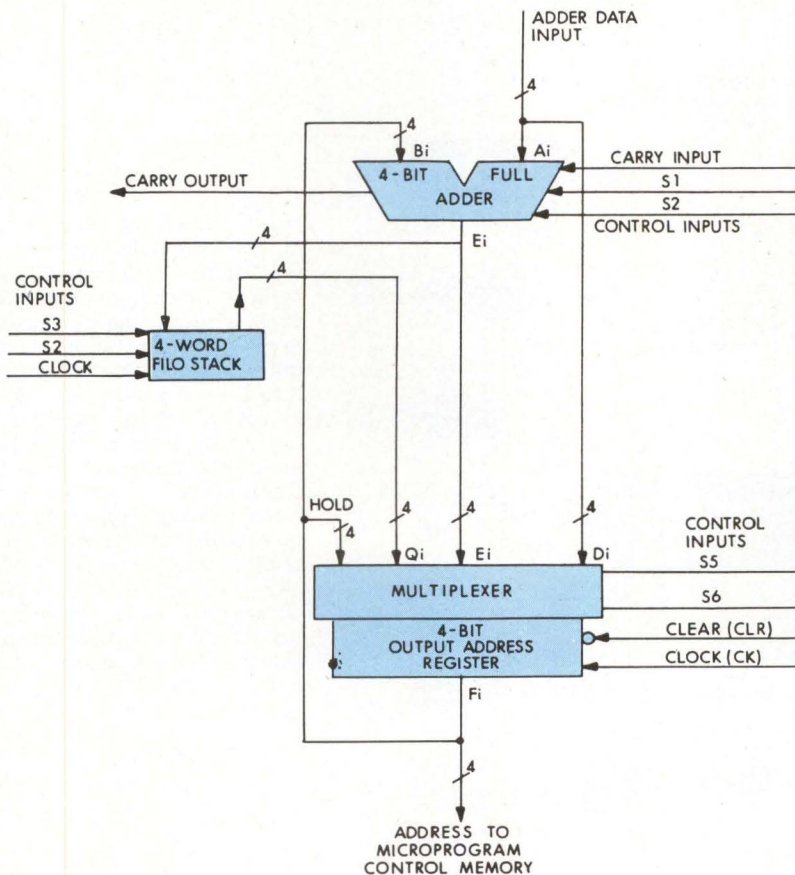


Fig 2 Functional block diagram of microsequencer. Four sources of data are delivered to 4-bit output address register. Addresses to control memory can be obtained directly from adder data input bus, output address register latch, and 4-word FILO stack. In addition, current address can be added to 4-bit full adder data on adder data input bus, as determined by control lines S_1 to S_6

ly designed to be straightforward, resulting in easier programming and debugging. The extensive capabilities of the bit slice control elements and the fast speed of the microprogram memory array often allow competitive performance with more complex pipelined architectures. Output lines of the microprogram memory control external logic systems, select input sources for the control elements, and specify microinstructions to be executed.

Full adder carry-input and carry-output lines allow cascading of the 4-bit slices. System design requires three cascaded slices, yielding a maximum address range of 2^{12} or 0000 to 4095, because use of up to 1024 words of control memory is anticipated. This system design resulted from tradeoffs of hardware implementation versus software restructuring, design time versus construction time, and cost considerations. The simple instruction repertoire of the microsequencer can often implement the functions of controllers with larger instruction sets by careful selection of the instructions available in combination with the full adder input. Since this system configuration can operate at 100-ns cycle times while using fast bipolar memories, the added speed of a complex pipeline structure is not necessary, thus considerably simplifying the overall microcontroller design.

Instruction Set

The microcontroller presents a desired series of control bits to the hardware under control. An ability to make decisions based on the results of previous operations is also required. Provision for repeating a sequence is highly useful; thus, a subroutine mechanism is needed. The manufacturer of the bit slice control element provides only hardware documentation, allowing designers to configure an instruction set to meet specialized needs. Therefore, an instruction set for the microcontroller has been formulated from the six useful combinations of the six select control lines (S1 to S6) and the carry input line, resulting in three groups of microinstructions—jump, next, and subroutine operations.

The first, or jump, group results in program control being transferred to the address specified by the source input selector. The second, or next, group adds one to the current address as calculated by the jump group. The third, or subroutine, group allows storage of the current address while a sequence of instructions is being executed, after which execution is resumed at the instruction following the address that called the subroutine.

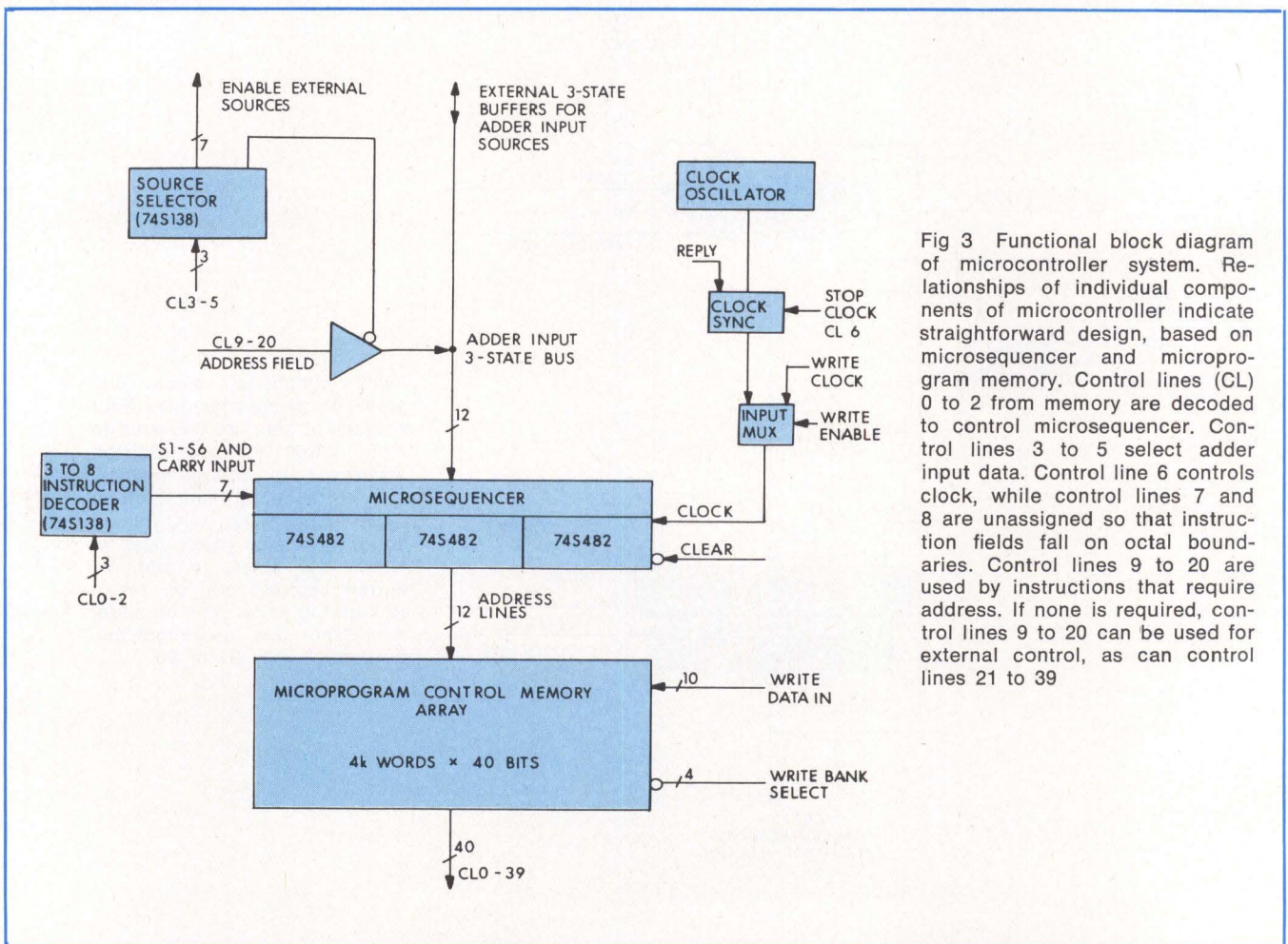


Fig 3 Functional block diagram of microcontroller system. Relationships of individual components of microcontroller indicate straightforward design, based on microsequencer and microprogram memory. Control lines (CL) 0 to 2 from memory are decoded to control microsequencer. Control lines 3 to 5 select adder input data. Control line 6 controls clock, while control lines 7 and 8 are unassigned so that instruction fields fall on octal boundaries. Control lines 9 to 20 are used by instructions that require address. If none is required, control lines 9 to 20 can be used for external control, as can control lines 21 to 39

A jump to subroutine (JMSA) microinstruction (Table 1) pushes the current contents of the output register plus 1 onto the 4-word internal FILO stack, and the output register is loaded from the data input lines. Execution of the microprogram then proceeds from the absolute address presented on the data input lines.

Nesting of subroutines beyond four levels must be avoided because the pushing of a fifth address onto the FILO stack will cause a stack overflow, losing the address at which execution will resume after returning from the first subroutine. To return from a subroutine (RETS), the top address on the stack is loaded into the microsequencer output register, allowing execution to resume at the next microinstruction after the call to the subroutine in the main microprogram. This operation pops the stack one position, making the address stored by a previous subroutine call available on top of the stack.

Jump and next microinstructions have two forms, relative and absolute. The relative form adds the contents of the output register to the data input lines, while the absolute form loads the output register directly from the data input lines. Thus, the absolute jump (AJMP) microinstruction can jump to the address in microcontroller memory which is presented on the data input lines. The absolute next (ANXT) microin-

struction does not completely follow form because it merely increments the output register, causing the next microinstruction to be accessed.

The relative jump (RJMP) and relative next (RNXT) microinstructions allow alteration of the microprogram flow based on data presented on the data input lines. RNXT operates in exactly the same manner as the RJMP, except that the address loaded into the output register is one greater than that loaded by a corresponding RJMP microinstruction. RJMP adds the data input lines to the contents of the output register and then loads this sum into the output register. This microinstruction is used in a situation where a constant control bit pattern is desired until some quantity being tested assumes a nonzero value.

An external flag, which assumes a logic 1 value when the external device under control is ready for further operations, can be connected to the data input lines. At the point when the microprogram cannot proceed until the operation is done, an RJMP microinstruction is encoded to select this flag for the data input lines. As long as the flag is a logic 0, RJMP continuously repeats itself. Only when the flag goes to a logic 1 does the microprogram proceed to the next microinstruction. Naturally, the opposite condition could be selected by inverting the flag signal.

TABLE 1
Microcontroller Instruction Set

Octal Code	Mnemonic	Adder		Stack			Latch		Carry-In Line		
		S1	S2	Operation	S3	S4	Operation	S5		S6	
0	Jump Absolute AJMP	0	0	---	0	0	Hold	0	0	Di	0
1	Jump Relative RJMP	0	0	a + b + c	0	0	Hold	0	1	Si	0
2	Jump to Subroutine JMSA	1	0	b + c	1	1	Push	0	0	Di	1
3	No Operation NOOP	0	0	---	0	0	Hold	1	1	Hold	0
4	Return from Subroutine RETS	0	0	---	1	0	Pop	1	0	Qi	0
5	No Operation NOOP	0	0	---	0	0	Hold	1	1	Hold	0
6	Next Absolute ANXT	1	0	b + c	0	0	Hold	0	1	Si	1
7	Next Relative RNXT	0	0	a + b + c	0	0	Hold	0	1	Si	1

a—adder input
b—address output register contents
c—carry-in line
Di—adder input
Si—top value on stack
Qi—address output register

Complementing the data input lines would result in jumping backward one microinstruction in the microprogram. If the device flag is connected to a bit other than the least significant bit (LSB) on the data input lines, a jump of more than one microinstruction could be made. In fact, this mechanism is a particularly convenient method to implement a jump table. The offset into the table is impressed on the data input lines, and a relative jump or next microinstruction is executed. For example, the designer may be able to encode the major types of a computer's instruction set into several bits. When the microcontroller is ready to execute the next computer instruction, it selects the output of the instruction type encoder and does a relative next microinstruction. This instruction directs the microprogram through the jump table to the microinstructions which perform the function of the computer instruction encoded earlier.

Table 1 summarizes the microinstruction set, indicating the octal code assigned to each microinstruction, the states of the microsequencer control bits, and their results for the adder, stack, and latch sections of the control element. Microinstructions obtained from bits 0 to 2 of microprogram memory are translated by the instruction decoder into control signals S1 to S6 for the microsequencer. Operation columns indicate the instruction's effect on respective elements of the microsequencer. The state of the carry-in line is also indicated. Because the relative forms of the subroutine microinstruction have no useful result, they are called

no operation (NOOP). However, these are critical microinstructions since they loop on themselves indefinitely. The only practical way to recover from a no operation microinstruction is to assert the clear line of the microsequencer, thus forcing address 0000 into the output register.

By comparing the microinstruction set in Table 1 with that of other microsequencers, the relative next and jump microinstructions can be used to implement conditional microinstructions present in most other microsequencers. Conditional jump to subroutine and return from subroutine instructions are not available, but these functions can be implemented by the sequence of a relative jump or next instruction, and then the desired subroutine microinstruction. Loop-until-count-goes-to-zero microinstructions could be implemented by testing the NOR function of an external counter output with a relative jump microinstruction. The relative jump microinstruction is repeated until the external counter output goes to zero, thus incrementing the microinstruction counter in the output register of the microsequencer. Except in cases where microprogram memory words must be conserved, control of such loops might be done more easily by repeating the complete microinstruction bit pattern using the absolute next microinstruction until the desired small number of operations are completed. The lack of conditional subroutine microinstructions may also require use of a few extra microprogram memory words. A short listing of the system application (waveform generator) program (Table 2) demonstrates the

TABLE 2
Waveform Generation Program

Address	Octal Instruction				Mnemonic	Comment
	ECB	ADDF	W	S I		
0	0000	0000	1	0 6	ANXT WAIT	
1	0000	0200	1	0 6	ANXT 200 ADDF WAIT	(Start waveform ramp up)
2	0000	0400	1	0 6	ANXT 400 ADDF WAIT	
3	0000	1000	1	0 6	ANXT 1000 ADDF WAIT	(Max amplitude reached)
4	0001	1000	1	0 6	ANXT 1000 ADDF 1 ECB WAIT	(Enable count up
5	0001	1000	1	0 6	ANXT 1000 ADDF 1 ECB WAIT	(to integrate response)
— similar instructions through address 371 —						
371	0000	1000	1	0 6	ANXT 1000 ADDF WAIT	
372	0000	0400	1	0 6	ANXT 400 ADDF WAIT	(Start ramp down)
373	0000	0200	1	0 6	ANXT 200 ADDF WAIT	
374	0000	0000	1	0 6	ANXT WAIT	
375	0002	0000	1	0 6	ANXT WAIT 2 ECB	(Enable count down for
376	0006	0000	1	0 6	ANXT WAIT 6 ECB	(baseline subtraction, set flag)
377	0000	0000	1	7 0	AJMP 0 ADDF CMEM WAIT	(Jump to contents of ADDF)

ECB—external control bits of microprogram memory

ADDF—address field

W—clock control bit

S—source select field

I—instruction select field

utility of the microcontroller instruction set. Partial listing of the waveform generator program shows the microprogram address, instruction, and source mnemonics. In this program, the address field is used for jump addresses and values for the DAC. Mnemonics ANXT and AJMP set the I field, ADDF sets the ADDF field, WAIT sets the W field to a 1, and CMEM sets the S field to 7 which selects the ADDF field as the source of addresses for the microsequencer. ECB sets the ECB field which controls external logic in this application.

Microprogram Memory

The 40-bit wide microprogram memory is arranged in six fields to facilitate software and conserve memory bits (Fig 4). The three LSBs (2, 1, and 0) select the desired microinstruction (Table 1). The next three bits (5, 4, and 3) select one of seven external sources for the data input lines. The eighth possible coding (bits 5, 4, and 3 are all 1s) selects the 12-bit address field of microprogram memory (bits 9 through 20). This field may be shared with other external control functions, in which case, care must be taken to avoid destroying data in the external device under control. Bit 6 is the clock control bit. Bits 7 and 8 are available for external control or may be used to expand the number of sources for the data input lines. Bits 21 through 39 are available for external control functions.

Space is available in microprogram control memory for both P/ROM and bipolar R/W memory depending on designer requirements. The capacity of memory installed is determined by the application requirements of a particular system.

Up to two banks of P/ROM may be installed in the current system design—256-word by 4-bit or 512-word by 4-bit memory units may be used by selecting the proper address lines from the control element output register and the chip select decoder. Similarly, one bank of 256-word by 1-bit or 1024-word by 1-bit bipolar

R/W memory units may be installed with wiring modifications. The smallest implementation of microprogram memory would consist of 256 words of P/ROM or R/W memory, while the largest implementation would consist of 1024 words of R/W memory and 1024 words of P/ROM for a maximum microprogram of 2048 words by 40 bits wide. Larger configurations would require additional printed circuit area or another 4-bit slice if 4096 words are exceeded.

R/W memory is used as a writable control store, particularly to test microprograms before they are dedicated to P/ROM. To accomplish the writing process for test purposes, external logic asserts the write enable line (Fig 3), which stops the execution of the microprogram. This external logic then places the address to be written into on the data input lines and pulses the write clock, which loads the microsequencer output register with the desired address. Then, external logic applies proper data to the 10 write input lines for each of the four banks of R/W memory, pulsing the proper bank select line to conclude the writing operation. This procedure is repeated for all addresses that must be written into memory; after this, microprogram execution is restarted in an orderly fashion at microprogram address 0000 by deactivating the write enable line and pulsing the control element clear line.

Clock Synchronization Logic

In the clock synchronization logic (Fig 5), the enable flipflop (FF) is cleared by the rising edge of the wait signal generated from bit 6 (CL 6) of control memory. When the current clock pulse is completed, no more pulses are generated until the enable flipflop is set by the positive transition of the externally generated reply signal. Setup time with respect to the rising edge of the microsequencer clock is about 40 ns, which is the same period of time as the sum of the decode instruction and setup times (Table 3). Thus, setting bit 6 in the current microinstruction to 1 halts the

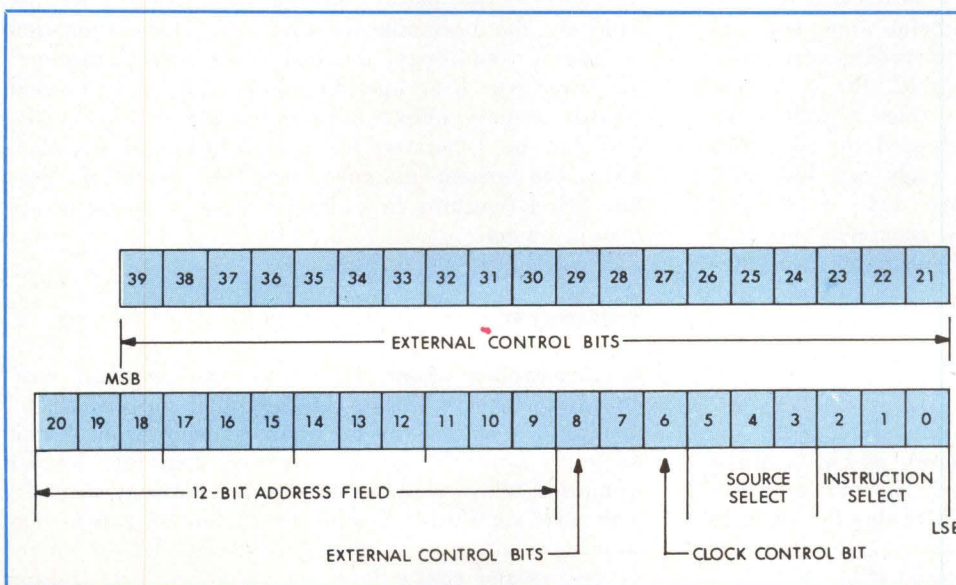


Fig 4 Microprogram memory control fields. Encoding of control fields in microprogram memory reduces number of bits required in memory. Bits 0 to 2 select one of eight possible instructions, of which six are used. Bits 3 to 5 select one of eight adder input data sources. Bit 6 halts microcontroller clock when high to allow synchronization with external logic. Bits 7 and 8 are unassigned so that address field (9 to 20) falls on octal boundaries, allowing easier programming. Address field of 12 bits may be used to control external logic as do external control bits (20 to 39), if it is not selected by source select field

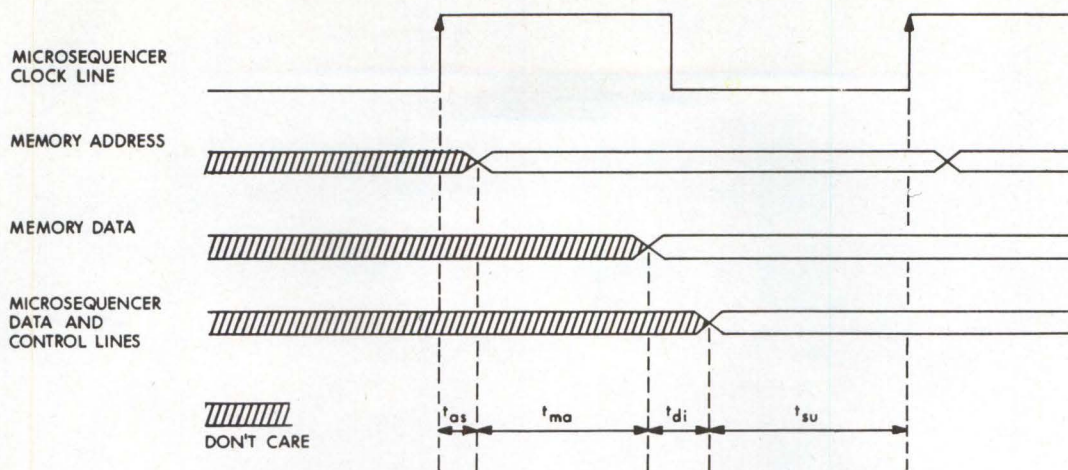


Fig 6 Microcontroller timing diagram. Timing is referenced to rising edge of microsequencer clock. Time parameter t_{as} is address setup time for microsequencer. Note that memory address lines are valid a short time after rising edge of clock. Memory data are valid after memory access time, t_{ma} , has elapsed. Microcontroller instructions are decoded during time t_{di} . Microsequencer instruction and data lines must be valid by start of setup time t_{su} . Table 3 lists typical time values

TABLE 3
Microcontroller Timing Parameters

Time Parameter	Observed	Typical	Maximum
t_{as}	15	12	25
t_{ma} (74S206)	40	35	55
t_{di}	10 (30)	12 (27)	21 (47)
t_{su}	30 (15)	30 (15)	30 (15)
Total	95 (100)	89 (89)	131 (142)

t_{as} —microsequencer address set time from rising edge of clock
 t_{ma} —memory access time
 t_{di} —instruction decode time
 t_{su} —setup time required for control signals (or data) before rising edge of microsequencer clock

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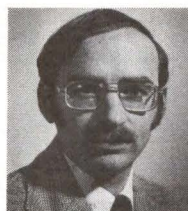
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of a carefully structured instruction set results in an efficient microcontroller system.

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Regardless of particular application or variations in specific organizational details, cache memories rely on the basic concept that, in the step-by-step execution of a large program, a central processing unit originated fetch at an address has a high average probability of being repeatedly accessed. Fundamentally, a cache provides a small, high speed scratchpad overlay buffer memory, typically implemented in bipolar technology. Its capacity is only a fraction of that of main memory, which is generally of magnetic core or metal oxide semiconductor technology. Addresses and corresponding contents most frequently accessed by the central processing unit are automatically stored in cache memory, which significantly reduces the number

of accesses to slower main memory, and increases the processing speed of the entire system.

The same result could probably be achieved by simply replacing slow core with high speed semiconductor main memory, but the relatively high cost and inherent volatility of the latter limit the performance/cost ratio. Replacing existing core memory systems is even more economically unattractive.

Minicomputer Selection

The PDP-11/45 minicomputer was chosen for a cache memory design because of several factors; however,

the central processing unit (CPU) selection process can be applied to other similar minicomputers:

1. This minicomputer has a basic CPU cycle time of 330 ns, three times faster than the speed of its main core memory/Unibus* combination.
2. It also has Fastbus*, a separate high speed bus that allows the CPU to run at its fastest speed. In addition, the timing relationship between the two buses neatly facilitates the application of a pluggable cache memory.
3. There are unassigned slots in the CPU backpanel in which to plug the cache with no mechanical or electrical modifications required. Power can be derived from either of two sources: from a separate 5-V power supply within the minicomputer power supply chassis, or from an existing supply. The entire installation can be accomplished in 10 to 15 min.
4. Cache in conjunction with core memory yields important advantages. There is a system speed advantage of Fastbus metal oxide semiconductor (MOS) memory throughout its entire 124k-word address range, without incurring its 32k-word limitation and volatility. In a mixed memory system of different cycle speeds, cache tends to minimize such differences; the slower the core memory, the greater is the percentage benefit from buffering with a cache. Also, the programmer need not allocate faster portions of memory to certain programs in order to optimize system speed.

Selection of Cache Memory Algorithm

Several alternative cache memory algorithms were considered and evaluated by means of computer simulation. A write through (WT) algorithm, conceptually the simplest, was selected as having the most favorable advantages. All write requests are referred directly to main memory with cache memory updating itself in parallel if it contains the specified address. The benefit of this concept is that the contents of addresses stored in main memory and in cache are always identical. This characteristic is especially valuable in systems with independent input/output data paths, such as in the PDP-11/45, and also for coping with an unplanned power interruption. A WT limitation concerns the fraction of reads ratio (FR), defined as the number of CPU read requests divided by the total number of CPU requests; for most programs, this ratio is approximately 0.7 to 0.8.

While considering various alternative algorithms, it was decided that the cache would have to be a pluggable board requiring no modification of the minicomputer. After carefully studying the architectural and physical design of the minicomputer, it became apparent that only the WT algorithm would allow the

physical construction necessary to satisfy this design constraint.

Analytical results indicated that the WT algorithm could cut effective machine cycle time approximately in half, ie, double the average CPU processing speed. Theoretically, the maximum possible goal would be to triple the processing speed, due to the speed limitation of the CPU, if the program did no write operations and all fetches were satisfied out of cache.

The use of the WT algorithm turned out to be further justified because of the relative ease in dealing with direct memory address (DMA) and interrupt activities on the Unibus. In addition, this algorithm allows the cache to share Fastbus and be completely compatible with up to 16k words of MOS or bipolar memory.

Selection of Cache Size

Studies have shown that a cache memory size of at least 512 words is necessary for typical minicomputer programs in order to maintain an acceptably high hit ratio (HR), defined as the ratio of the number of times that the desired address is in the cache divided by the number of CPU fetch requests. Typically, HR equals 0.88 ± 0.03 . The final cache memory size was chosen as 1k words (or 2k bytes) to significantly improve the HR while drastically decreasing chip count and halving power consumption by using 1k-bit Schottky bipolar RAM chips.

Cache Memory Architecture

The internal block diagram of the cache is shown in Fig 1. The control circuitry mainly provides the proper interfacing between Unibus, Fastbus, and the rest of the cache. The address multiplexer switches either the Unibus, Fastbus or internal initialization address into the memory section. The initialization circuitry, comprising a 10-bit counter that drives the internal address bus to the memory, initializes the cache by clearing all 1024 bits in the valid bit register (VBR). The memory is organized as a 1k-x 27-bit array. The 27 bits are comprised of 16 bits for the data, 7 for the directory, 1 for the VBR, and 3 for parity checking.

The compare circuitry compares the output of the directory to the bits <17:11> of the incoming address to determine a cache hit/miss. The parity error detection and display circuitry checks for parity errors on CPU fetches. If an error occurs, this section causes a CPU trap, disables the cache, turns on an LED, and sets the error bit in the control/status register (CSR). The CSR also has a bit which allows software or front panel enable/disable of the cache, and a diagnostic parity error flag disable bit.

Organizationally, the WT cache adapts to the PDP-11/45 as shown in Fig 2. Notice that the cache plugs

*PDP-11/45, Unibus, and Fastbus are registered trademarks of Digital Equipment Corp, Maynard, Mass

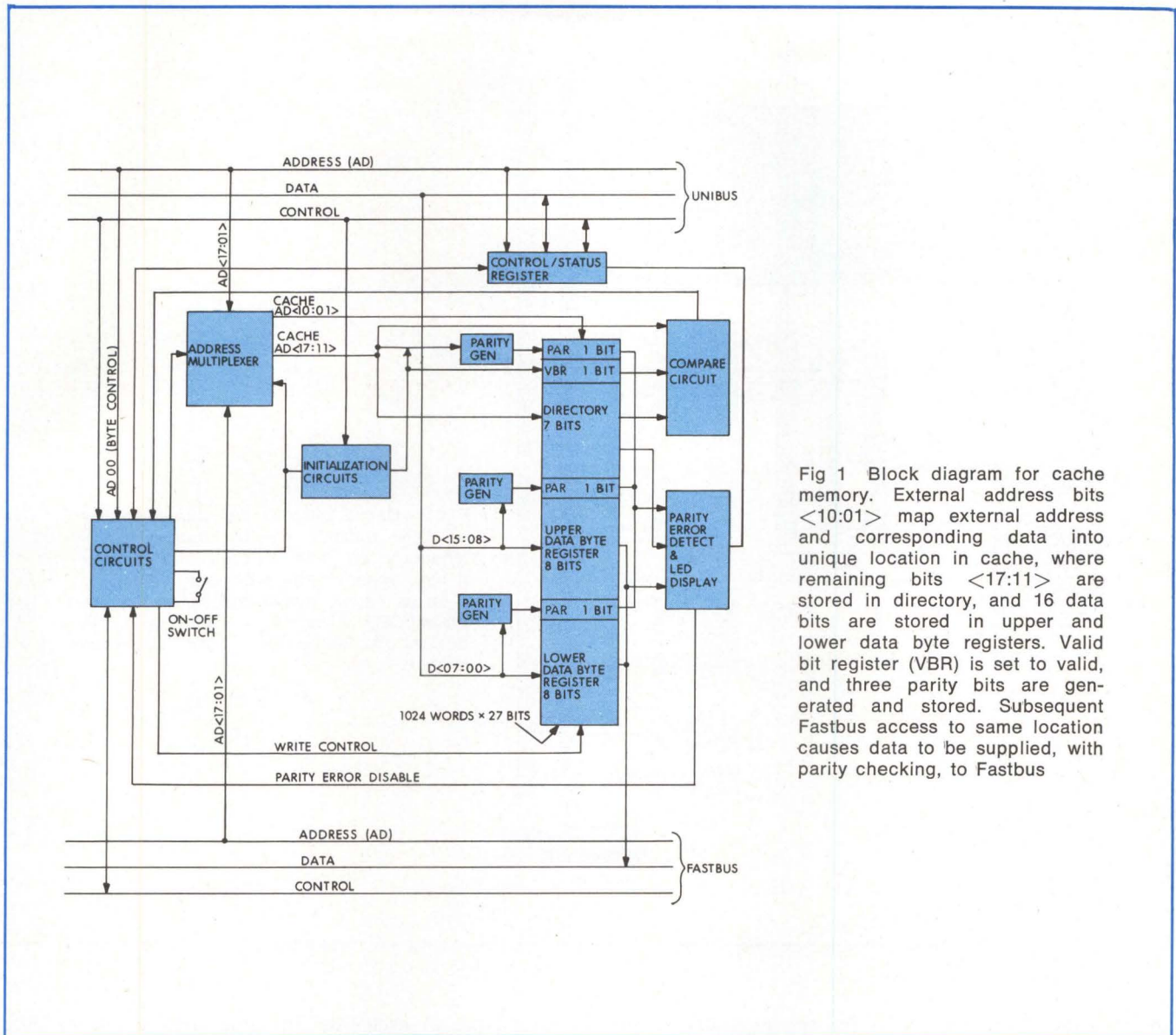


Fig 1 Block diagram for cache memory. External address bits <10:01> map external address and corresponding data into unique location in cache, where remaining bits <17:11> are stored in directory, and 16 data bits are stored in upper and lower data byte registers. Valid bit register (VBR) is set to valid, and three parity bits are generated and stored. Subsequent Fastbus access to same location causes data to be supplied, with parity checking, to Fastbus

into both Unibus and Fastbus. Thus, the cache is a dual-port memory, with certain differences. The cache is completely passive on the Unibus port; it can only receive Unibus signals, but not drive them. Conversely, the Fastbus port cannot receive data, but can drive the Fastbus data signals.

CPU Fetch Requests

Normally, the CPU initiates all memory requests on both buses simultaneously by asserting the specified address on the address lines for both. While waiting the required minimum time of 150 ns on Unibus before starting a core memory cycle, the cache is ready to accept a signal on Fastbus, indicating that the specified address is located within the cache. Figs 3 and

4 illustrate fetch read and write request responses, respectively. If the address is in cache and if the CPU memory request is a fetch, the cache transmits a response signal, causing the CPU to cancel the remaining Unibus cycle, which means that no core memory cycle will take place either. Data are available on Fastbus and the CPU is ready to start the next request 330 ns later, compared to about 1000 ns if the request had been filled from core memory.

If the specified address is not in cache, the CPU does not receive the Fastbus response signal, continues the Unibus cycle in the usual manner, and obtains the desired data from core. When data are available on the Unibus, the cache automatically copies and stores this information and the top portion of the corresponding address via the Unibus port; then, data

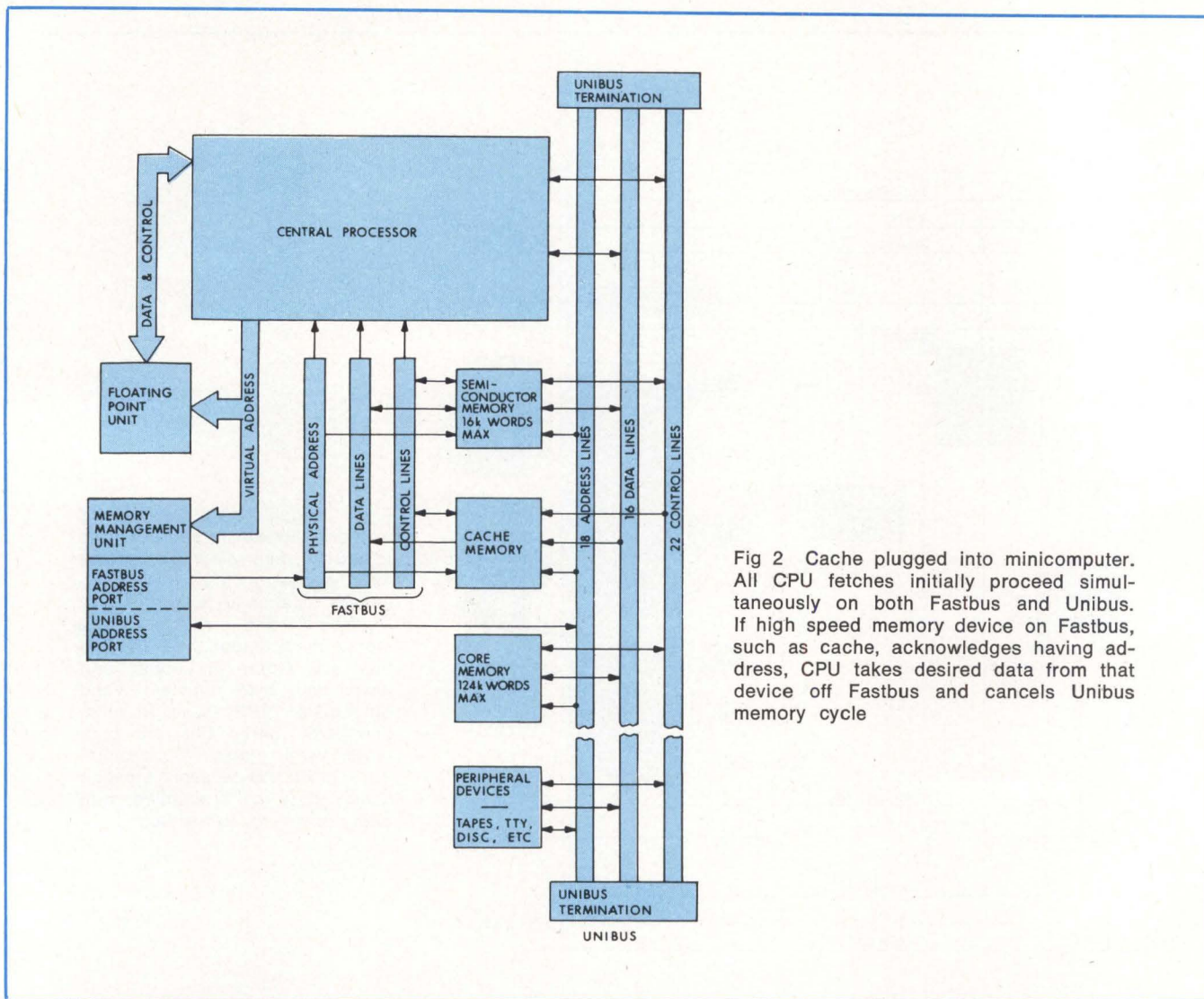


Fig 2 Cache plugged into minicomputer. All CPU fetches initially proceed simultaneously on both Fastbus and Unibus. If high speed memory device on Fastbus, such as cache, acknowledges having address, CPU takes desired data from that device off Fastbus and cancels Unibus memory cycle

are available from the cache for the next CPU fetch to that address.

CPU Write Requests

CPU write requests to core memory are filled on the Unibus just as if the cache were not present. However, when the address is in cache, new data are written into cache in parallel with core memory. This condition ensures that data in core memory are always current with those in cache, and that the inherent non-volatility of the core memory will guarantee against loss of data resulting from power failure. It also facilitates handling DMA activity.

DMA and Interrupts

DMA and interrupt cycles are entirely Unibus operations and do not involve the Fastbus. Consequently,

these types of cycles do not insert new addresses into the cache; only CPU fetch cycles do that. However, if a DMA cycle should update an address in core that is also in cache, the new data are simultaneously written into cache also.

Cache Address Replacement Strategy

The many-to-one correspondence principle involved in a simple direct mapping scheme is illustrated in Fig 5. The address space of the PDP-11/45 is 131,072 words specified by 17 bits <17 : 01>. This address space can be divided into 128 blocks, each consisting of a block number and the lower address bits <10 : 01> that specify the position, or memory cell, of the address within the block. These same lower address bits also specify one of 1024 individual memory cells within the cache.

When an address is stored in cache, only the block number is physically stored in a 1k x 7-bit register

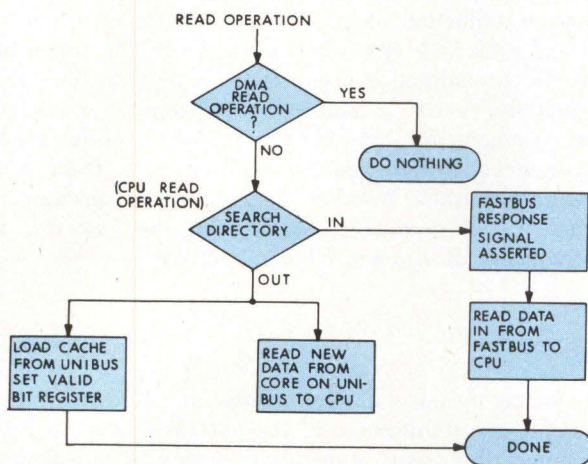


Fig 3 Cache response to memory fetch. Ignoring all DMA fetches, cache searches its directory only in response to CPU fetches. If hit occurs, cache acknowledges and supplies desired data on Fastbus. If it is a miss, cache does not acknowledge, and desired data are supplied by main memory to both CPU and cache simultaneously on Unibus

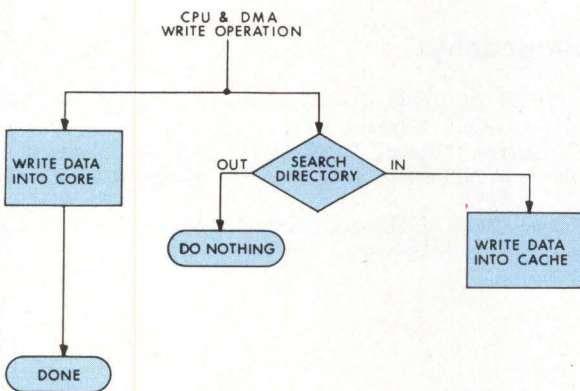


Fig 4 Cache response to write operation. Since cache does not acknowledge CPU writes on Fastbus, all writes, both CPU and DMA, occur on Unibus and are handled identically by cache. If address is in cache, its data are updated in parallel with that of main memory, and if not, contents of cache remain unchanged

called the directory. This directory is organized as a content addressable memory (CAM), meaning that when the cache is accessed, the 7-bit word readout of the directory memory cell specified by address bits <10 : 01> is compared bit-by-bit with the top seven bits of the incoming address bits <17 : 11>. If there is an equal compare, the address is said to be in cache, or that there is a hit.

Initialization Scheme

In order to clear out invalid contents in the cache, the cache automatically initializes itself by clearing all 1024 bits in the VBR. The process of initialization sets all the associated flag bits in the VBR for each of the 1024 locations in the cache back to zero. This condition has the effect of forcing "misses" from the cache; hence, the CPU will be satisfied only by the core memory until the cache is once again "reloaded" with valid data.

Initialization, which requires about 500 μ s to complete, takes place automatically whenever either the dc power is restored to the computer system after a power interruption or when the Unibus initialization (INIT) signal is deactivated. This activity is completely transparent to the system.

The cache can be switched on or off, either mechanically or by software, to inhibit it from supplying data to the CPU. In this state, the system would run just as if no cache were installed; however, the cache would continue to load itself with current information. This on-off capability is useful for benchmarking and system debugging.

Parity Error Detection

Parity error (PE) detection is provided on the cache to improve overall system reliability. The method used is to divide the basic 1k x 24-bit memory array of the cache into three 8-bit bytes and add a parity bit to each byte, resulting in a 1k x 27-bit memory array. Three LED indicators provide visual indication not only of a parity error but also of the defective byte. In addition, bit 15 in the Unibus-addressable CSR is set, and bit 1 (on-off bit) is cleared when a parity error occurs. Furthermore, the cache automatically turns itself off line and flags the CPU with a dedicated PE line.

An addressable cache CSR provides the following error bits/functions:

Bit 15—normally clear, but is set if cache parity error occurs. Read-only capability.

Bit 1—on-off line control is cleared automatically if cache parity error occurs. May also be used to disable cache. (Can be overridden in ON state by mechanical switch.) Read/write capability.

Bit 0—normally set; when cleared, cache is inhibited

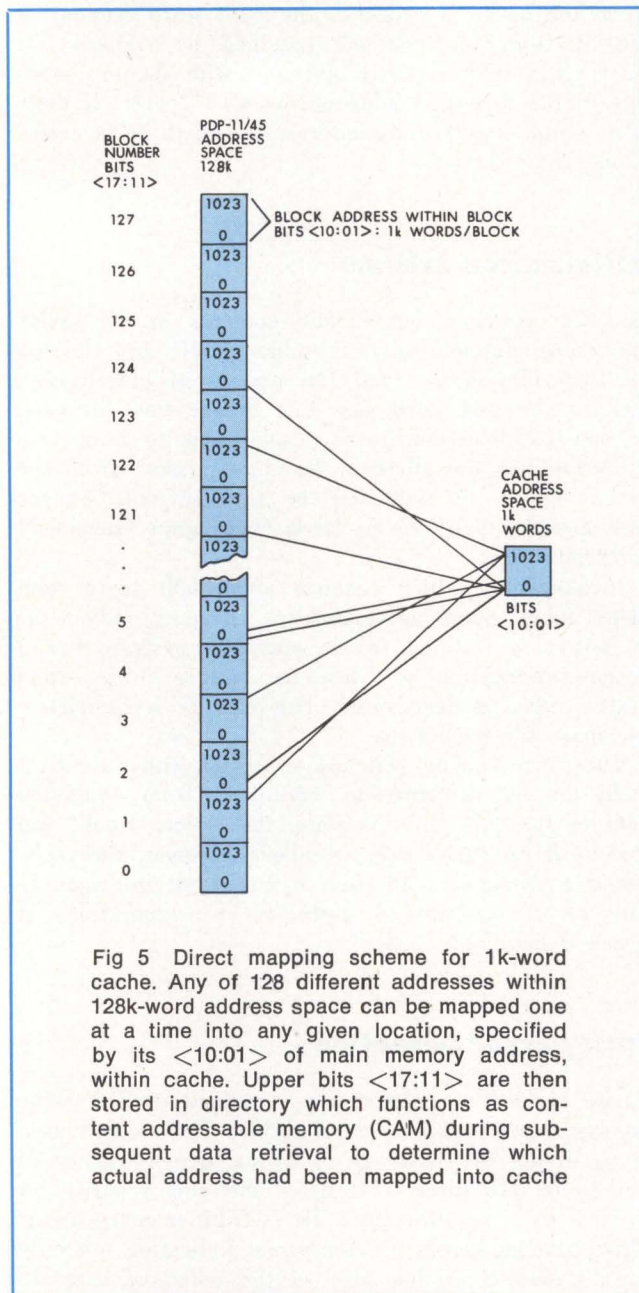


Fig 5 Direct mapping scheme for 1k-word cache. Any of 128 different addresses within 128k-word address space can be mapped one at a time into any given location, specified by its $\langle 10:01 \rangle$ of main memory address, within cache. Upper bits $\langle 17:11 \rangle$ are then stored in directory which functions as content addressable memory (CAM) during subsequent data retrieval to determine which actual address had been mapped into cache

from transmitting PE flag to CPU. (Used for diagnostic purposes only.) Read/write capability.

Benchmark Data

Benchmark tests have been run on large minicomputer systems using a wide variety of programs. For many programs, it was found that the cache could effect an increase in overall system processing speed of 30 to 70%, with more than 100% having been measured in some applications. It is important to note that reduction

in runtime is not the same numerically as performance (throughput) increase. The runtime reduction ratio (RRR) is the inverse of the throughput ratio (TR). Thus, a runtime reduction of 40% (0.40) results in a $RRR = 0.60$ and a $TR = 1/RRR = 1/0.60 = 1.67$. The actual increase in throughput or productivity is 67% in this case.

Generally, cache memories are program sensitive, which accounts for some of the spread in performance improvement. Parameters HR and FR vary from program to program. Another factor, which can have a strong, if not dominant, bearing on the outcome, is the frequency of DMA and interrupt activity.

Summary

This cache memory design utilizes the 2-bus (Fastbus and Unibus) architecture of the PDP-11/45 CPU in such a manner that most CPU fetch requests are satisfied by the cache on the Fastbus (a hit) instead of by the core memory on the Unibus. When the address is not in cache (a miss), the CPU fetches it directly from core memory via the Unibus, from which the cache automatically incorporates it into itself, making it available on the Fastbus for the next fetch. All write operations are done on the Unibus to core memory and simultaneously to the same address (if present) in cache, thus guaranteeing power-failure data protection. If a parity error occurs, the cache will flag the CPU (causing it to trap to parity error vector at address 114), turn off the cache on the Fastbus, turn on the appropriate PE LED, and set bit 15 in the CSR.

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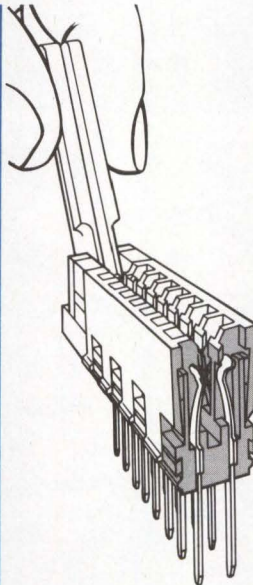
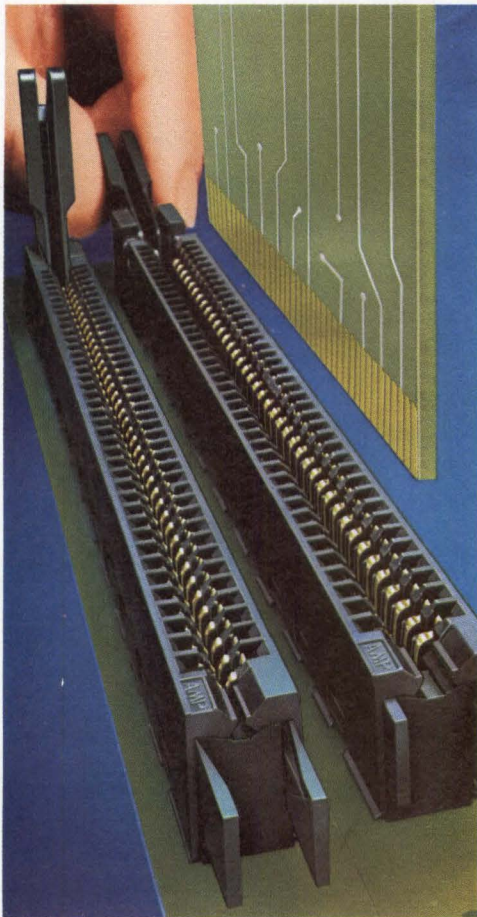


Ronald N. Monroe has had wide experience as a designer of digital and analog circuitry related to the computer industry. Before taking on the presidency of Minntronics Co, Inc, he designed the first commercially successful cache memory for the PDP-11/45 while at Fabri-Tek, Inc, as project engineer. Mr Monroe holds a BSEE from the University of Minnesota.



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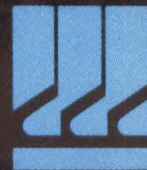
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LSI CHIPS EASE STANDARD 488 BUS INTERFACING

Time and cost disadvantages of interfacing to the IEEE Std 488 bus are overcome with a dedicated LSI chip set that incorporates most of its functional and electrical specifications

Ronald M. Williams Intel Corporation, Santa Clara, California

Historically, interface techniques proliferated as designers evolved customized links among instruments, controllers, and processors for realtime test measurements or data communications, resulting in excessive and expensive codes, formats, signal levels, and timing factors. Obviously, interface standardization was mandatory to save design costs for engineers, development costs for manufacturers, and system integration costs for users. Thus, IEEE Standard 488-1978 (a revision of ANSI/IEEE Std 488-1975) offers a universal instrumentation system approach to automatic operating measurement configurations that provides compatibility, versatility, and flexibility. This system approach establishes

a suitable standard bus for interfacing programmable devices from different manufacturers. Outstanding advantages of the standard bus include byte serial, bit parallel digital data handling, synchronized communication among devices at varying data rates, and hardware interchangeability and interconnection in daisy-chained fashion. However, some restrictive disadvantages that have hindered implementation are highly complex logic protocol, time consuming design analysis, and lack of low cost components to perform the intricate logic control functions. To overcome these drawbacks, a large scale integrated (LSI) chip set has been designed with built-in IEEE Std 488 logic controls. Thus,

interfacing has been significantly simplified for properly connecting processor buses and programming system protocols.

Interface Overview

The IEEE Standard 488-1978 bus interface includes electrical, mechanical, and functional specifications* for interconnecting both programmable and nonprogrammable electronic measuring apparatus with other apparatus and accessories necessary to assemble instrumentation systems. The functional specifications occupy about 80% of the document and involve a proportional amount of system design time to imple-

*This article deals with the functional aspects (interface signals that exist on the physical bus) of IEEE Std 488-1978, and is not intended as a complete dissertation on the major elements of the standard. For detailed definitions of the mechanical (physical cable connections), electrical (timing, voltages, and currents), and operational (application software routines) technicalities, interested readers should consult the *IEEE Standard Digital Interface for Programmable Instrumentation*, IEEE Std 488-1978, Institute of Electrical and Electronics Engineers, Inc, New York, NY 10017, Nov 30, 1978—Ed.

ment. Bus functions encompass 16 active signal lines, 10 interface functions, the protocol by which interface functions send and receive messages, and logical and timing relationships between signal states.

Functional requirements of the standard can be incorporated in either hardware, software, or a combination of both. Some designers have chosen the hardware approach to incorporate all the interface functions, using about 200 medium scale integrated (MSI) and small scale integrated (SSI) packages. This technique costs about \$1000 for a complete interface board. As a result, many cost sensitive implementations of the bus interface use only a subset of its functions custom tailored to the requirements of the devices involved, thereby reducing package count and expense by curtailing the interchangeability advantages.

Other designers have selected the software approach to implement the bus interface. One disadvantage of this approach is that programming is an expensive and extended project; another is that a subroutine has to be executed with each transferred byte. This overhead not only burdens the microprocessor within a device, but also reduces the overall speed of the bus. This approach costs about \$200 for the interfacing functions.

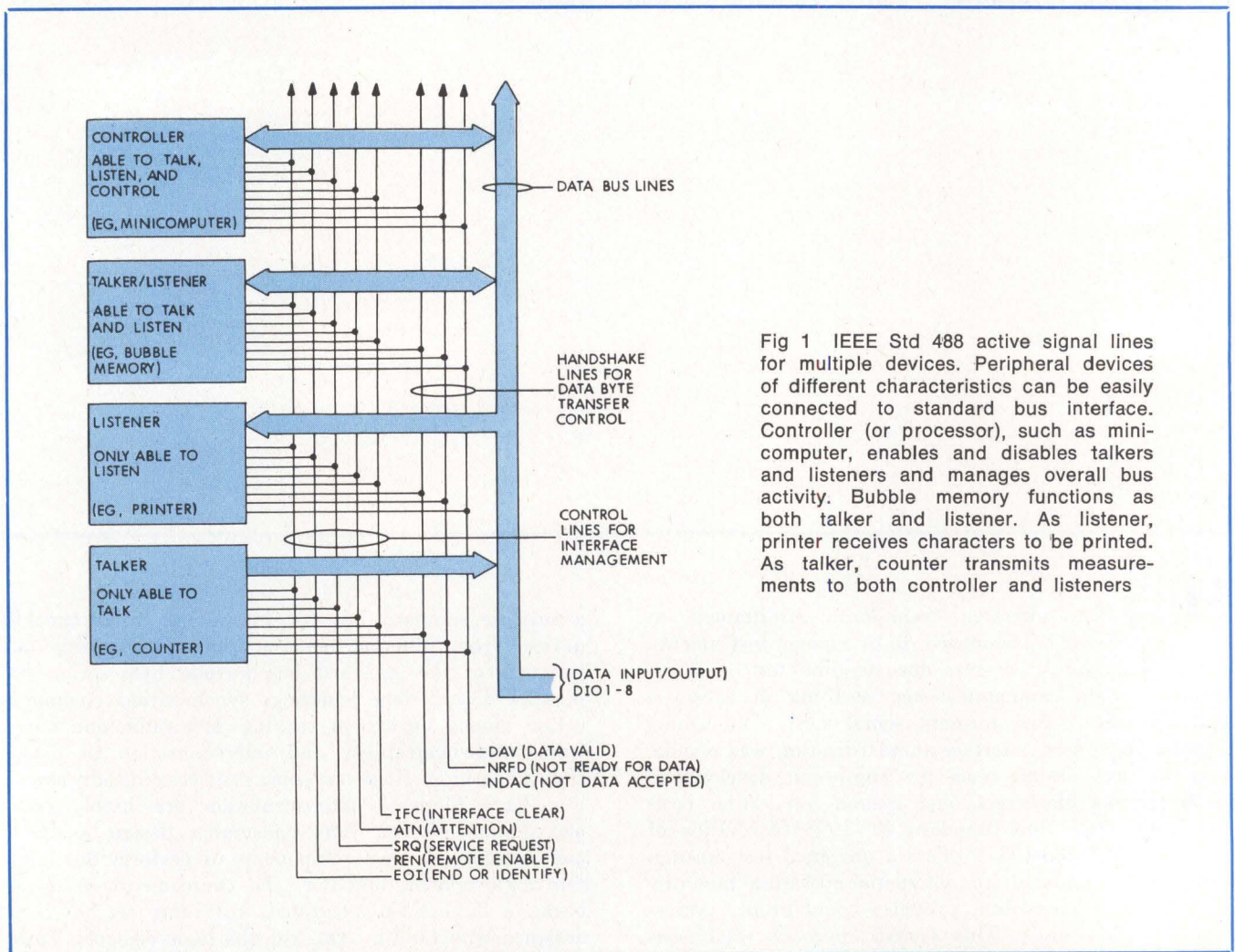


Fig 1 IEEE Std 488 active signal lines for multiple devices. Peripheral devices of different characteristics can be easily connected to standard bus interface. Controller (or processor), such as minicomputer, enables and disables talkers and listeners and manages overall bus activity. Bubble memory functions as both talker and listener. As listener, printer receives characters to be printed. As talker, counter transmits measurements to both controller and listeners

Combinational hardware/software approaches, although faster than direct software implementations, still require enormous design time and cost about \$1000 for a typical interface board.

With a recent alternative approach, however, the bus interface is easier and less expensive to incorporate in instrument designs. LSI circuit chips now include as built-in capabilities most of the functional and some of the electrical portions of the Standard's specifications, significantly reducing design time and costing about \$50 for bus interfacing. Additionally, Intel's 8291/8292 General Purpose Interface Bus (GPIB) peripheral chip set also incorporates capabilities for bus monitoring, data rate manipulation, and addressing to further simplify bus interface designs.

Bus Signal Definitions

The IEEE Std 488 signals are defined as negative true, where the high state (0 = false, ≥ 2.0 V) and the low state (1 = true, ≤ 0.8 V) are based on standard transistor-transistor logic (TTL) levels. Of the 16 active signal lines, 8 are data lines, 5 are interface manage-

ment lines, and 3 are handshake lines (Fig 1). Data input/output lines (DIO1-DIO8) carry ASCII-coded information, as well as device addresses, universal commands, or program instructions. Interface management lines help to supervise the data lines. The primary management line—Attention (ATN)—determines how data lines are processed. When ATN is true, data lines are interpreted as addresses or universal commands by all bus connected devices. When ATN is false, only those devices addressed can use the data lines; in this case, data transmitted are typically device-dependent. With another management line, Interface Clear (IFC), the bus controller returns the system to a known quiescent state. The Service Request (SRQ) line can be used by any device on the interface bus when it has data to send (talker) or needs to receive data (listener). The Remote Enable (REN) line determines whether the system is under front panel or program control. The End Or Identify (EOI) line can be used as a delimiter by a talker (sending) device to indicate an end of message, or by the controller as a polling line.

Handshake lines control the timing relationship of the interface bus (Fig 2). The Data Valid (DAV) line

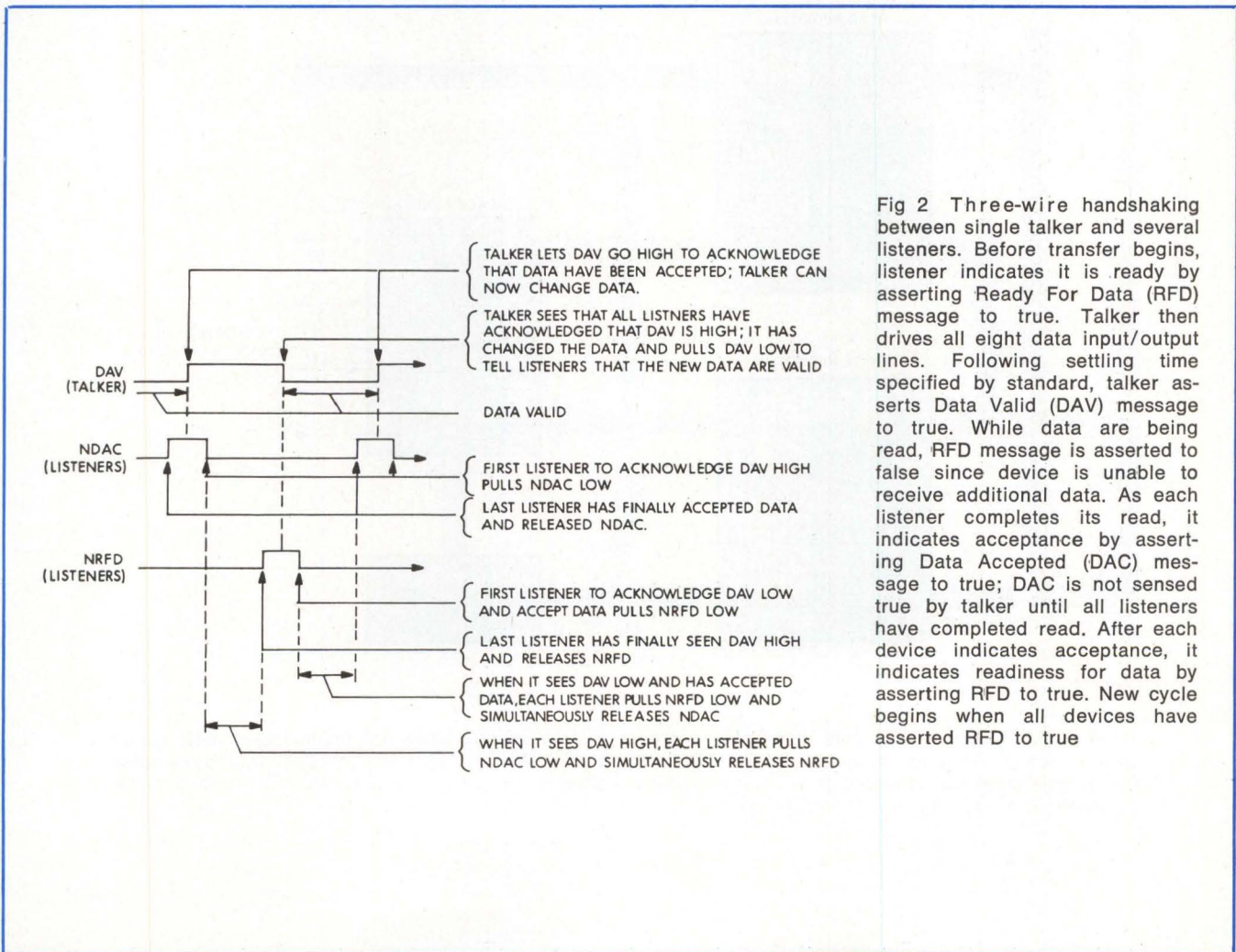


Fig 2 Three-wire handshaking between single talker and several listeners. Before transfer begins, listener indicates it is ready by asserting Ready For Data (RFD) message to true. Talker then drives all eight data input/output lines. Following settling time specified by standard, talker asserts Data Valid (DAV) message to true. While data are being read, RFD message is asserted to false since device is unable to receive additional data. As each listener completes its read, it indicates acceptance by asserting Data Accepted (DAC) message to true; DAC is not sensed true by talker until all listeners have completed read. After each device indicates acceptance, it indicates readiness for data by asserting RFD to true. New cycle begins when all devices have asserted RFD to true

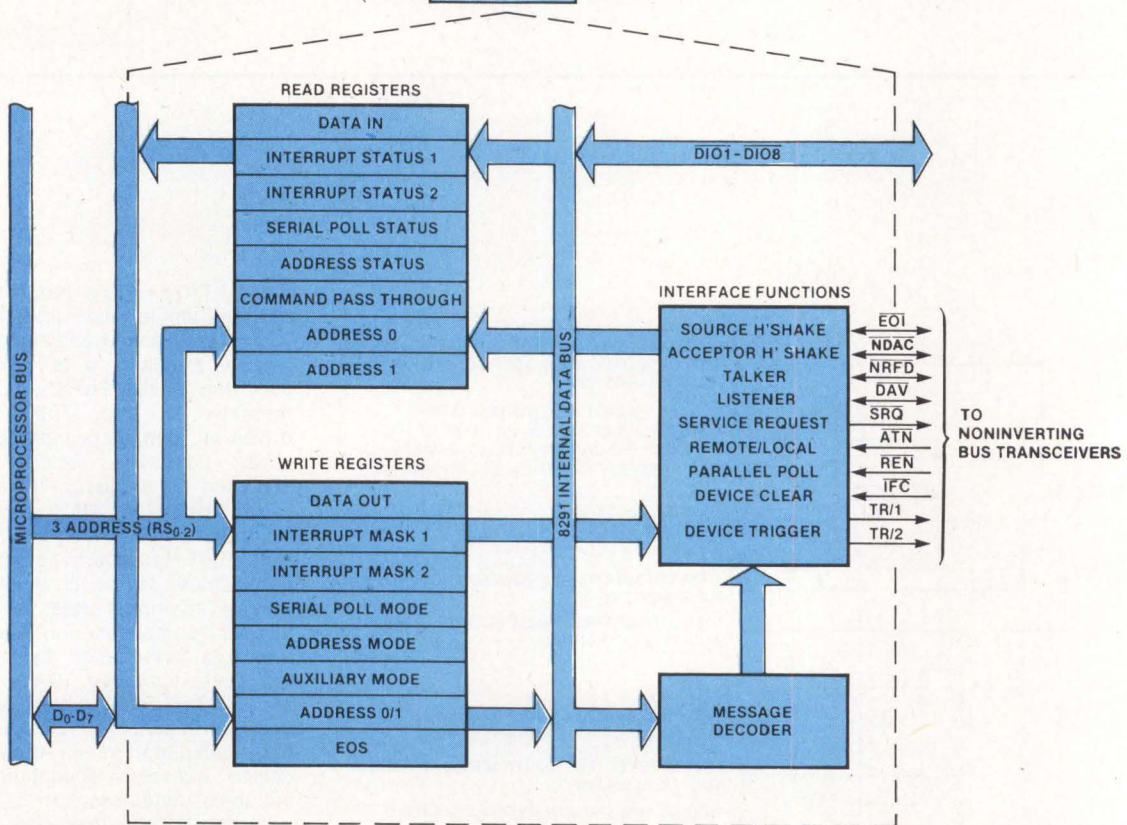
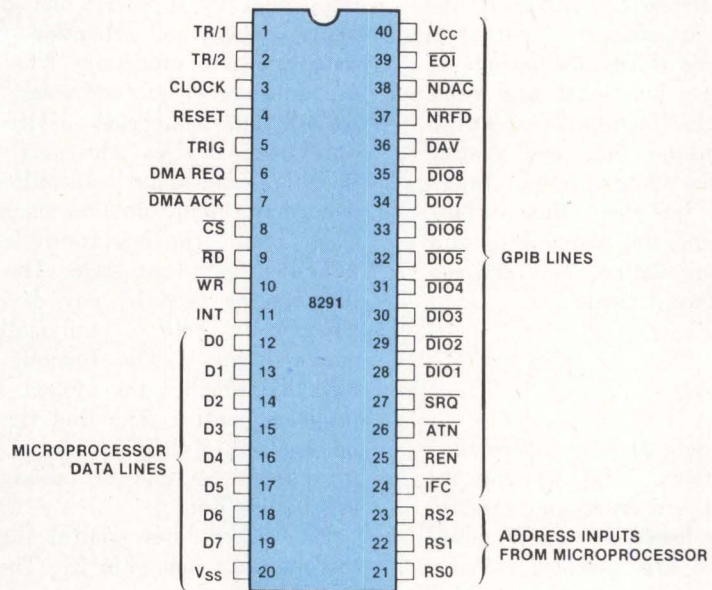
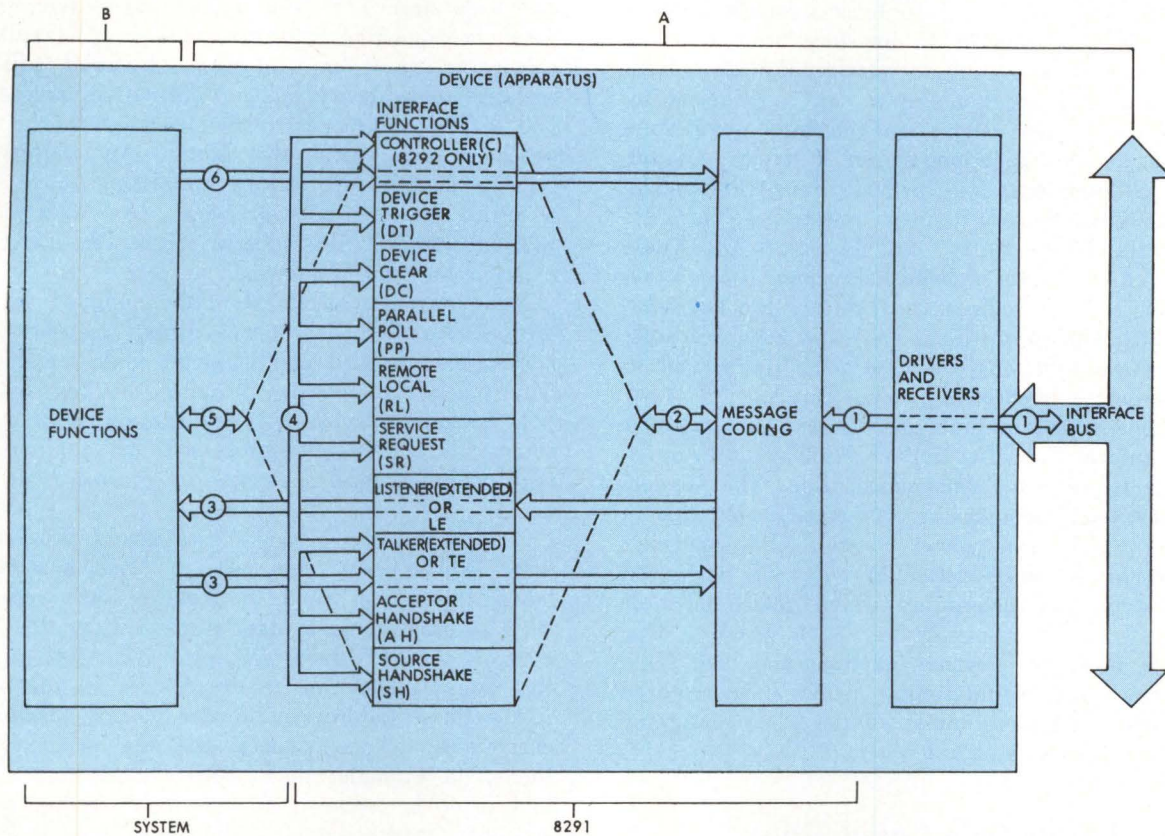


Fig 3 GPIB talker/listener chip. 8291 chip connects 8-bit microprocessor to noninverting bus transceivers, which, in turn, connect to IEEE Std 488 bus. Microprocessor manipulates data bytes after receipt or before transmission, and monitors talker/listener status. Single chip handles all IEEE Std 488 interface functions, except controller functions



- A - CAPABILITY DEFINED BY 488-1978 STANDARD
 B - CAPABILITY DEFINED BY DESIGNER
 1 - INTERFACE BUS SIGNAL LINES
 2 - REMOTE INTERFACE MESSAGES TO AND FROM INTERFACE FUNCTIONS
 3 - DEVICE DEPENDENT MESSAGES TO AND FROM DEVICE FUNCTIONS
 4 - STATE LINKAGES BETWEEN INTERFACE FUNCTIONS
 5 - LOCAL MESSAGES BETWEEN DEVICE FUNCTIONS AND INTERFACE FUNCTIONS
 (MESSAGES TO INTERFACE FUNCTIONS ARE DEFINED; MESSAGES FROM INTERFACE FUNCTIONS EXIST ACCORDING TO DESIGNER)
 6 - REMOTE INTERFACE MESSAGES SENT BY DEVICE FUNCTIONS WITHIN CONTROLLER (8292)

Fig 4 Bus interface functions. Messages received from interface bus can cause state transitions, just as state transitions can cause messages to be sent on bus (1 and 2). Device dependent data are transferred automatically to microprocessor, without affecting state transitions (3). State changes in one function can cause state changes in another function, resulting in message to be sent (4). Microprocessor can also send local messages to interface functions (5) or remote messages to interface (6)

is used by a talker device to indicate that data are ready to transmit. The Not Ready For Data (NRFD) and Not Data Accepted (NDAC) lines are used by a listener to indicate readiness to receive data and receipt of data, respectively. As a result, a talker knows when all listeners on the bus have received an 8-bit byte of information. Thus, the transmission rate of the bus is only as fast as the slowest listener.

Messages conveyed by all 16 lines are true or false, depending on the states of 10 interface functions. The standard defines each of these interface functions with state diagrams. A function's state can be changed by a controller, another device on the bus, or a state change in another function within a device. Of the 10 interface functions, four provide basic communication capabilities: Source Handshake (SH), Talker (T), Acceptor Handshake (AH), and Listener (L). These functions affect the three handshake lines (DAV, NRFD, and NDAC), eight data lines (DIO1-DIO8), and EOI management line. The Device Clear (DC) and Device Trigger (DT) interface functions are used to initialize and to trigger a device, respectively. The Parallel Poll (PP) function acts with the EOI line to send a single bit of status information. The Service Request (SRQ) function controls the SRQ management line. The Remote Local (RL) interface uses the REN management line in conjunction with front panel control. The Controller (C) function, which is active in only one device on the bus at a time, determines which device talks or listens.

To date, these 10 interface functions and their intricate interrelationship and timing factors have required difficult and time consuming efforts when designing the interface bus into a digital system.

Talker/Listener Chip Capabilities

The 8291 GPIB talker/listener chip, a 40-pin LSI device (Fig 3), performs the inversion necessary to connect an 8-bit microprocessor bus to the negative true IEEE Std 488 bus. In addition, this chip implements most of the Standard's required functions. The microprocessor sets the talker/listener chip to an initial state, manipulates bytes before or after transmission, performs interrupt service routines, causes state changes, monitors other state changes, and enables and disables chip capabilities.

Without microprocessor involvement, the talker/listener chip implements all interface functions, except controller performance, such as handling data transfers, handshake protocols, listener/talker address procedures, device clearing and triggering, service requests, and parallel and serial polling schemes (Fig 4).

Within the chip architecture are eight read (output) and eight write (input) registers. One input register holds the data that are to be moved from the bus to the microprocessor when a device is listening. An output register holds the data byte that is to be

transferred to the bus when a device is ready to talk. The other seven write and seven read registers control various chip functions.

Interrupt status registers 1 and 2 store 12 different interrupt flags. For example, one bit in the Interrupt Status 2 register reflects changes in a device's addressed state. The microprocessor can poll both registers to determine which flag caused the interrupt, and can then branch to the appropriate service routine. Two corresponding interrupt mask registers allow designers to mask any interrupt. A serial poll status register holds device status information, and a serial poll mode register is available so that the microprocessor can verify this status. An address mode register contains a device's addressing mode, as determined by the microprocessor. An address status register monitors the address status (ie, active talker or active listener) of a device.

Two address registers store the assigned device addresses. An End-Of-Sequence (EOS) register contains a designer specified end of string code for delimiting data block transfers by flagging the last byte with EOI. A command pass-through register feeds non-GPIB commands to the microprocessor. An auxiliary mode register holds local messages to control reset, power on, etc.

Among the chip's capabilities are a programmable data transfer rate from 62k to 525k bytes/s, three addressing modes, and an EOS message recognition. With a programmable data transfer rate, the designer controls the handshake rate of the interface to match the data transfer rate to the devices on the bus.

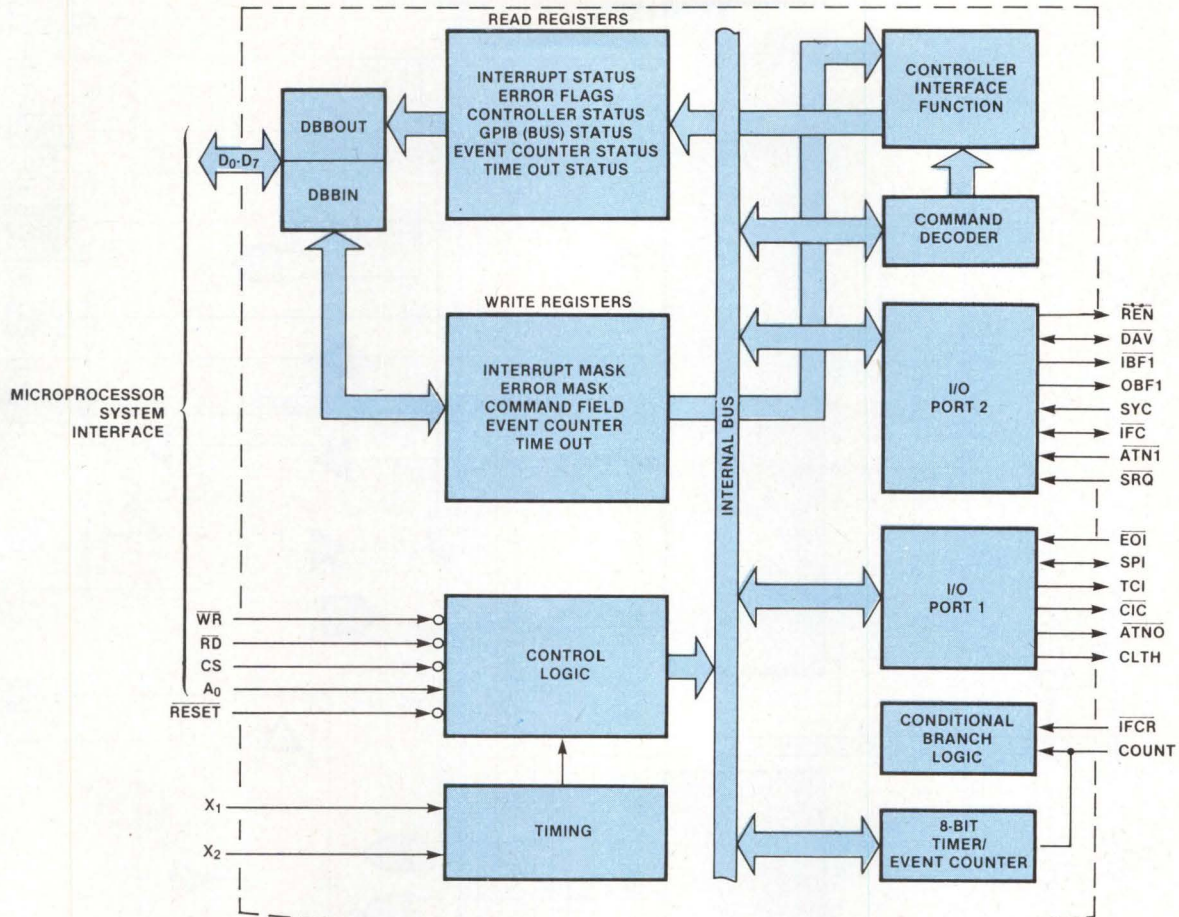
The three addressing modes permit flexibility in designating talkers/listeners. The dual primary address mode, for example, allows both a talker and a listener address to be assigned to a device. With the primary/secondary address mode, multiple devices of the same type can have the same primary address, but a different secondary address. In the third addressing mode, devices can have both dual primary and dual secondary addresses.

Data block transfers are made easier with the EOS register. This register holds the character that signals an end-of-block transfer. When a data byte loaded into the data-out register matches the byte in the EOS register, the talker/listener chip asserts the EOI line, signaling an end of transfer.

Controller Chip Capabilities

The 8292 controller chip (Fig 5) implements the controller function of the Standard. In conjunction with the 8291, the controller forms a complete standard interface, including the capability of handling the transfer control protocol. This ability gives the designer an option to accommodate multiple controllers on a single bus.

Additionally, the 8292 performs all the tasks necessary in a complete controller design. It responds to



IFCR	1	40	V _{CC}
X ₁	2	39	COUNT
X ₂	3	38	REN
RESET	4	37	DAV
V _{CC}	5	36	IBF ₁
CS	6	35	OBF ₁
GND	7	34	EOI
RD	8	33	SPI
A ₀	9	32	TCI
WR	10	31	CIC
8292		30	NC
SYNC	11	29	ATN ₀
D ₀	12	28	NC
D ₁	13	27	CLTH
D ₂	14	26	V _{CC}
D ₃	15	25	NC
D ₄	16	24	SYNC
D ₅	17	23	IFC
D ₆	18	22	ATN ₁
D ₇	19	21	SRQ
V _{SS}	20		

Fig 5 GPIB controller chip. 8292 chip works in conjunction with 8291 to perform GPIB controller interface functions. It implements local control commands from microprocessor according to IEEE Std 488 protocol. Additionally, it processes such inputs from bus as SRQ and EOI. Furthermore, it can send the full repertoire of GPIB control messages, including REN, IFC, ATN, and EOI

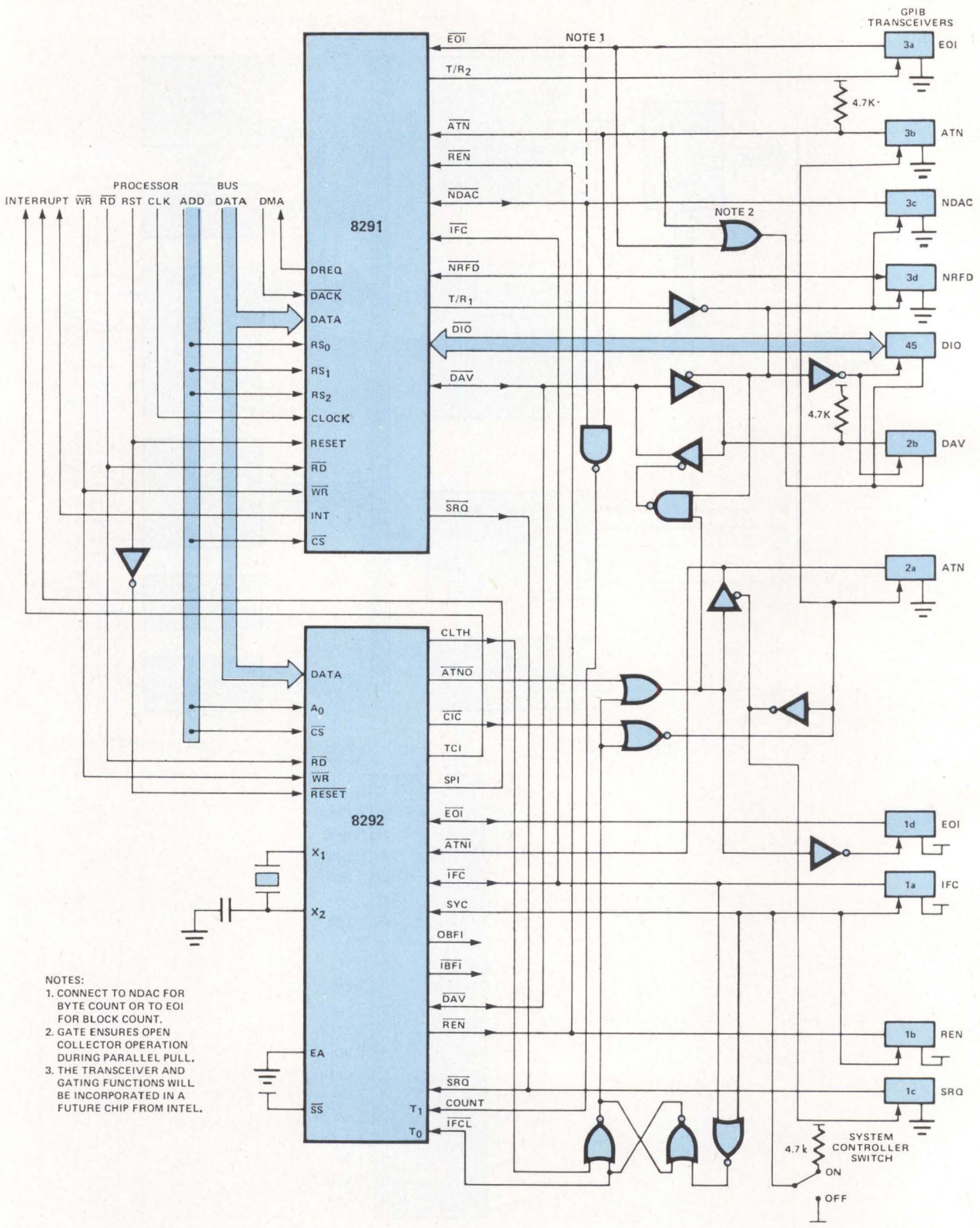


Fig 6 System configuration using chip set. In conjunction with 8291, 8292 performs complete controller function. Together with shared bus transceivers, chip set forms a complete IEEE Std 488 interface. In addition, DMA interface may be implemented through 8291 with 8237 DMA controller

service requests (SRQs), configures other devices on the bus for remote control by sending Remote Enable (REN), and sends Interface Clear (IFC), allowing for control seizure to reinitialize the bus. More importantly, the controller chip can take control of the bus synchronously with the handshake, preventing the destruction of any data transmission in progress.

Internally, the controller chip has 10 dedicated registers for programming and for monitoring status. Through the use of the Interrupt Status and Interrupt Mask registers, the designer can configure the controller to interrupt the microprocessor on selected events. An Event Counter and a corresponding status register are available to monitor and control either byte counts or block counts. A Time-Out register may be set by the designer to program a time-out error function; a corresponding status register contains the current value in the time-out counter. In conjunction with these registers, error control can be programmed with the Error Flags and Error Mask registers. Finally, Controller and GPIB Status registers are available. Each of these registers is read or programmed through a dedicated command buffer.

Chip Set Application

The talker/listener and controller chips connect to the standard interface bus through noninverting bus transceivers (Fig 6). These transceivers provide the 48-mA bus drive capability needed to meet the electrical portion of the IEEE Std 488 specification—not directly possible with existing metal oxide semiconductor (MOS) parts. The talker/listener chip can interface directly to microprocessor memory through a direct memory access (DMA) controller, such as an 8237.

The microprocessor drives the talker/listener with a short stored program (see Table), containing initialization conditions, such as data transfer rate, address mode, and other designer requirements. Microprocessor data handling is limited to taking bytes off the bus after they arrive or putting bytes of data on the bus. Interrupt service routines are necessary for each unmasked interrupt. Although 12 interrupts are available, not all have to be used. All other standard bus functions are handled by the 8291.

To send a byte of data, the microprocessor writes the byte into the talker/listener data-out register. The chip then transmits the data byte over the bus lines in conjunction with the handshake lines. Next, the NRFD line is checked to see if it is ready for data. If a ready for data message is detected, the talker/listener sends a DAV signal until it receives a data accepted message from the interface's NDAC line. The 8291 also generates a Byte Out (BO) interrupt, setting the BO flag in the interrupt status register. When its interrupt pin is activated, the microprocessor reads the interrupt status register and responds to the interrupt with an appropriate service routine.

The 8292 handles all hardware aspects of the controller function: SRQ input, ATN, IFC, EOI, and REN outputs. Meanwhile, the designer defined aspects of a

Talker (Transmitter) Initialization

8291 Register	Data	Comments
5W	02H	Reset
4W	01H	Address Mode 1 (Primary-Secondary)—Note that talk only could be selected here, eliminating need for controller address
6W	02H	Address 0 = 02H
6W	92H	Address 1 = 12H
0W	FFH	Enable All Interrupts
1W	3FH	Enable All Interrupts, DMA
5W	A4H	Enable High Speed Data Transfer
5W	00H	PON, Release Initialization State

given GPIB system are handled by processor software. For example, the processor is responsible for knowing which device on the bus corresponds to which device address. The processor then uses the 8291 to transmit coded Controller commands as the 8292 asserts ATN.

Summary

Bus interface designs that previously required 150 or 200 MSI/SSI chips may now be implemented with a GPIB peripheral chip set. For designers, this hardware set means less design time and cost, resulting in increased reliability and versatility in IEEE Std 488 bus interfaces custom programmed for dedicated applications.

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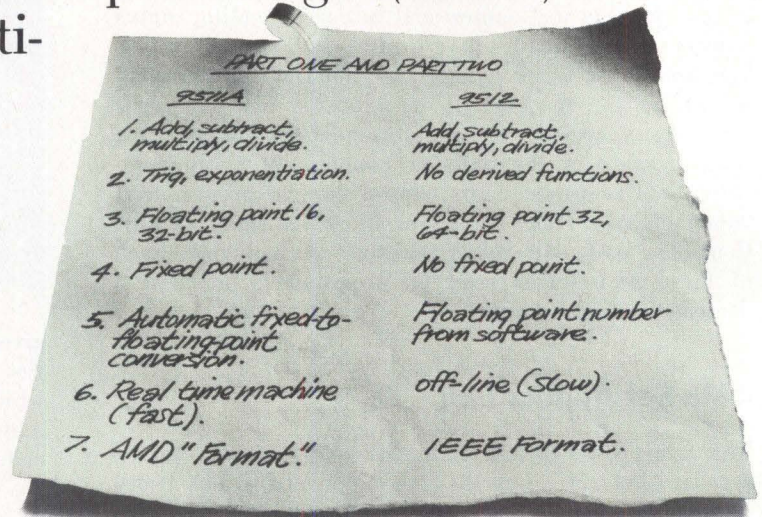


Ronald M. Williams is a product manager for peripheral controllers in Intel's Microcomputer Components Division. In addition to GPIB devices, he has been involved in introductions of dynamic RAM and CRT controllers. He holds a BS degree from Trinity College, an MS degree from Rensselaer Polytechnic Institute, and an MBA degree from the University of Chicago.

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Thermal printing technology has steadily advanced from earlier designs of heated styli and wax coated paper used on strip chart recorders to a high performance process with the latest innovations in integrated circuit designs for fabricating printheads, and in sophisticated chemical formulations for producing high contrast, fade resistant papers. Design considerations for a pagewide printhead with uniformly spaced resistive print elements, capable of fast print rates and high print quality, demonstrate the significant strides achieved in thermal printing technologies.

Technology Advantages and Disadvantages

As with other printing technologies, thermal printing will not solve all print output needs, but does offer distinct advantages, such as speed, reliability, quiet operation, and compactness. Similar to other nonimpact methods, thermal printing provides high speed output since there are no hammers, fingers, belts, chains, or ribbons to increase complexity. In its simplest form, that of a full width printhead, virtually the only moving parts in thermal printing are paper and platen. This simplicity

translates into higher speeds and more reliable operation. Mean time between failures (MTBFs) of 2k-h or 100M characters are common. Because it is a nonimpact method, thermal printing is quiet; sound pressure levels of less than 55 dBa are normal for thermal printers without sound-deadening enclosures. While not often considered a major advantage, thermal printing is clean because it requires no inks, ribbons, aluminized papers, or toners. These advantages, which also contribute to convenience and ease of use, plus compactness, make thermal printers



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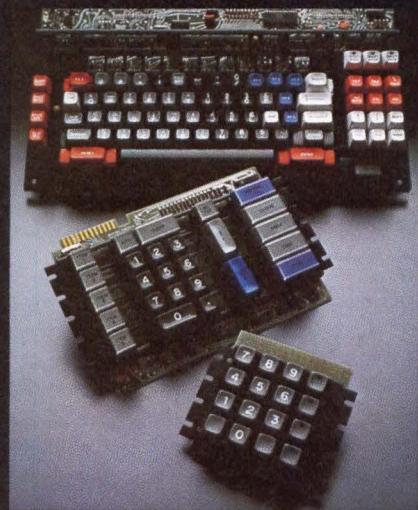
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Circle 71 for Data

ideal for integration into desktop computers, instruments, computer terminals, and analytical systems.

There are, however, some definite drawbacks. Among these are the cost of thermal paper, lack of simultaneous multiple copy capability, non-permanency of image, and occasional problems of making copies from thermal paper. Thermal paper is more expensive than plain—up to \$0.05/8.5 x 11" (21.6 x 27.9-cm) sheet for high quality, high contrast paper—compared to less than \$0.02/sheet for plain paper. However, this higher paper cost is gradually decreasing as thermal printing applications expand. Simultaneous multiple copies are not practical, but the high speed of thermal printing often makes sequential copies of output feasible if only occasional multiple copies are required. Improved chemical formulations, especially in black printing, have increased the fade resistance of thermal papers so that they are only slightly affected by sunlight or moderate heat. Paper reproducing in black also eliminates copying problems associated with some blue printing papers.

Image Forming

Thermal paper involves coating a normal base paper with a heat sensitive film of only a few micrometers thickness. This film contains particles of two separate colorless components—a dyestuff and a phenolic color former suspended in a solid binder. When heat is applied, the coating fuses and the two components flow together. Chemical reaction causes a colored image to appear; blue and black are the most common colors.

Printhead Technologies

There are several methods of applying heat to thermal paper in order to produce an image, the most common technologies being silicon mesa, thick film resistive, and thin film resistive. In silicon mesa technology, patented by Texas Instruments, printing elements are constituted of discrete silicon chips with a transistor-resistor pair deposited on the base (Fig 1). This chip is epoxy-bonded to a ceramic substrate in an array

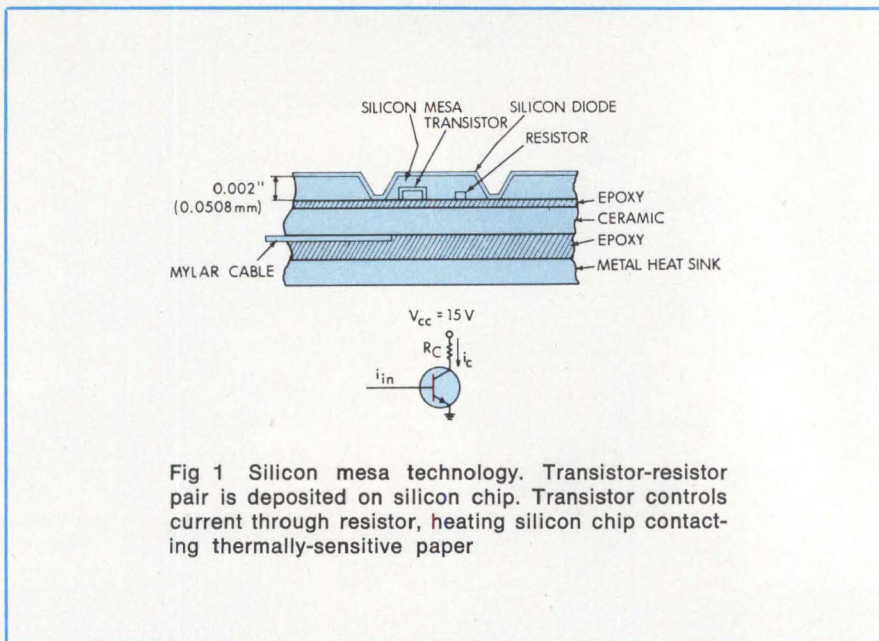


Fig 1 Silicon mesa technology. Transistor-resistor pair is deposited on silicon chip. Transistor controls current through resistor, heating silicon chip contacting thermally-sensitive paper

to form the print element. A small base current (i_{in}) controls a large current (i_c) through the resistor. Power dissipated by this resistor heats the silicon chip that is in contact with the paper. Print elements are thermally isolated from each other by a coating of silicon dioxide. Since silicon is highly resistant to abrasion, paper quality, and therefore cost, need not be as high as with other thermal technologies.

In thick film resistive technology, introduced by NCR, a resistive paste is silkscreened onto a ceramic substrate to produce individual print elements (Fig 2). Current is passed through these elements, and the power dissipated causes each to heat up while in contact with the paper. Depending on the thickness of the film, this method is also highly resistant to abrasion.

In thin film resistive technology, used extensively by Hewlett-Packard, the print elements are basically a resistive film, like the thick film method, but are only 500Å thick (Fig 3). The film is deposited on a ceramic substrate using a vacuum deposition method similar to that used in manufacturing integrated circuits. Because this method is more precise than silkscreening, higher print element densities are possible. This technique also produces a print element with a very low thermal mass. Elements can be heated and

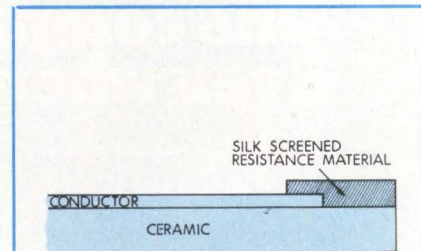


Fig 2 Thick film technology. Thick film of resistive paste is silkscreened onto ceramic substrate over conductive traces. Current through these resistors causes them to heat up and form image on thermally sensitive paper

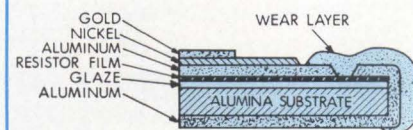
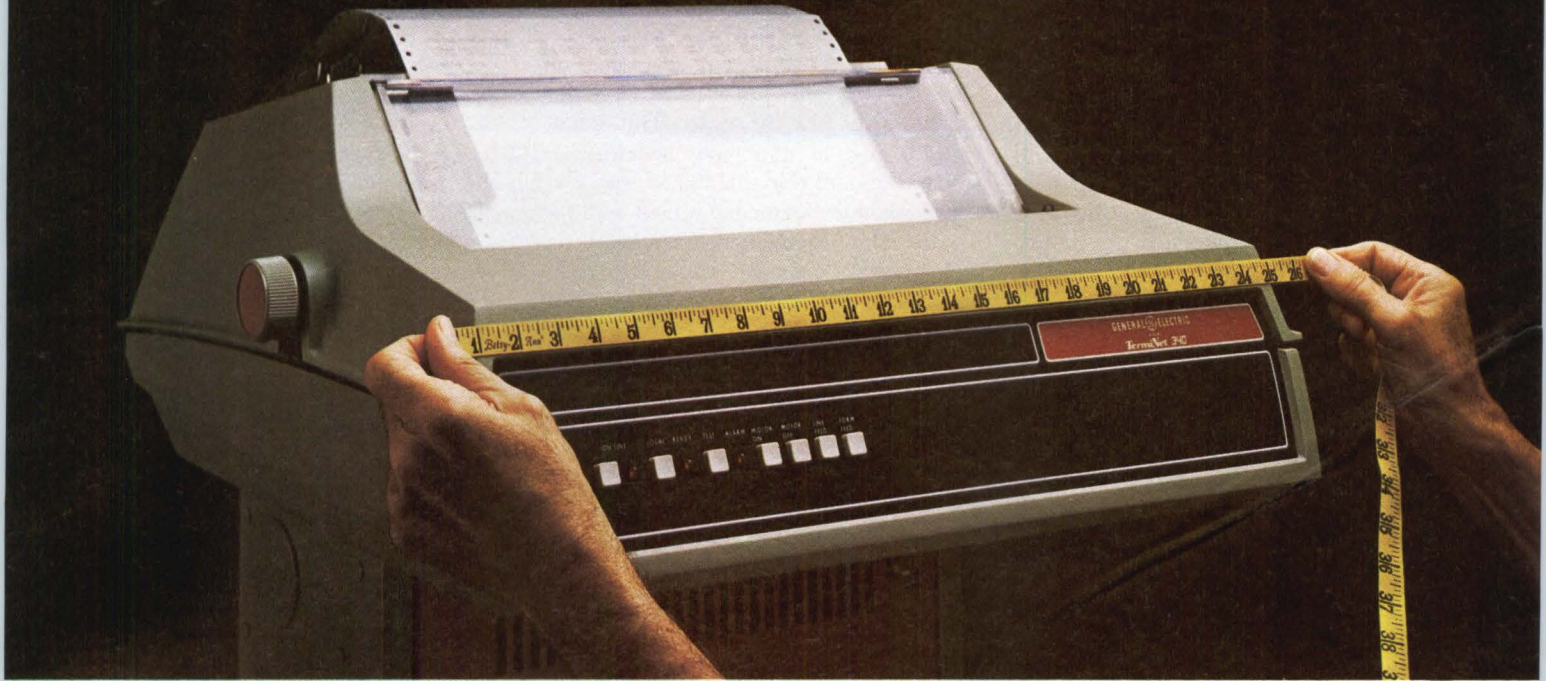


Fig 3 Thin film technology. Very thin (500-Å) resistive film is vacuum-deposited on ceramic substrate over conductive traces. Wear layer of aluminum oxide sputtered over print elements protects them from abrasion



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More reasons: print and ribbon systems that won't wear out prematurely and won't cause the problems other line printers do. Which is why the proven rotating-belt print system will last billions of characters. And why the ribbon cartridge will maintain very high print quality for at least 100 million characters.

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The fact is, TermiNet 340 line printers are such productive workers, they require very little attention and very little maintenance once they're up and running. Should service be needed, you can count on getting these printers back on-line in a hurry. That's because of convenient self-test features that make troubleshooting easy and fast. And because of a responsive nationwide service network that keeps downtime to a minimum and operating costs low.

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cooled quickly, allowing much faster printing than other methods, without smearing. To provide protection from abrasion, a wear layer of aluminum oxide is deposited over the print elements; low abrasion papers are recommended for maximum printhead life.

Printhead Mechanisms

For each thermal printhead technology, there are several methods of producing printed page copy. Most thermal printers produce characters made up of a dot matrix, with a 5-horizontal by 7-vertical dot array being the most popular. Patterns for these character sets are generally contained in a character buffer connected to a character read only memory (ROM), which translates 7- or 8-bit ASCII data-in characters into appropriate dot energization formats.

Characters are printed on thermal paper either by scanning a small

printhead array across the page or by moving the paper past a fixed pagewidth row of dots. The pagewidth row of dots may be either a single monolithic printhead or several smaller segments joined end-to-end. The segmented printhead is cheaper to produce, since the yield of a smaller segment is higher than that of a larger monolithic head. However, the requirements of matching resistances for uniform print quality and the mechanical complexity of precisely aligning the segments often overcome the initial lower cost of a segmented printhead. Inexpensive scanning head printers are usually lower in performance. Printing speed is limited by mechanical constraints to approximately 120 char/s, while fixed head printers can print up to 500 lines/min.

Thermal Printhead Architecture

As an example of recent thermal printhead architecture, mechanical

construction and data transfer design techniques are described for the 9876A 80-col thin film monolithic head thermal graphics printer. In the monolithic printhead (Fig 4), 560 equally spaced print resistors are positioned on 0.013" (0.33-mm) centers, across a 7.28" (185-mm) width, to print both alphanumeric data and high resolution graphics data. Printing and plotting are accomplished by moving thermally sensitive paper vertically in front of the print resistors while they are being selectively energized. The heating process causes the paper to darken where information is to be recorded. Print resistors are deposited uniformly and thinly on a ceramic substrate, and because of their low thermal mass, they can be heated and cooled rapidly so that speeds of up to 480 lines/min can be attained.

ASCII character data or control instructions pass into the printer through the interface chip, which

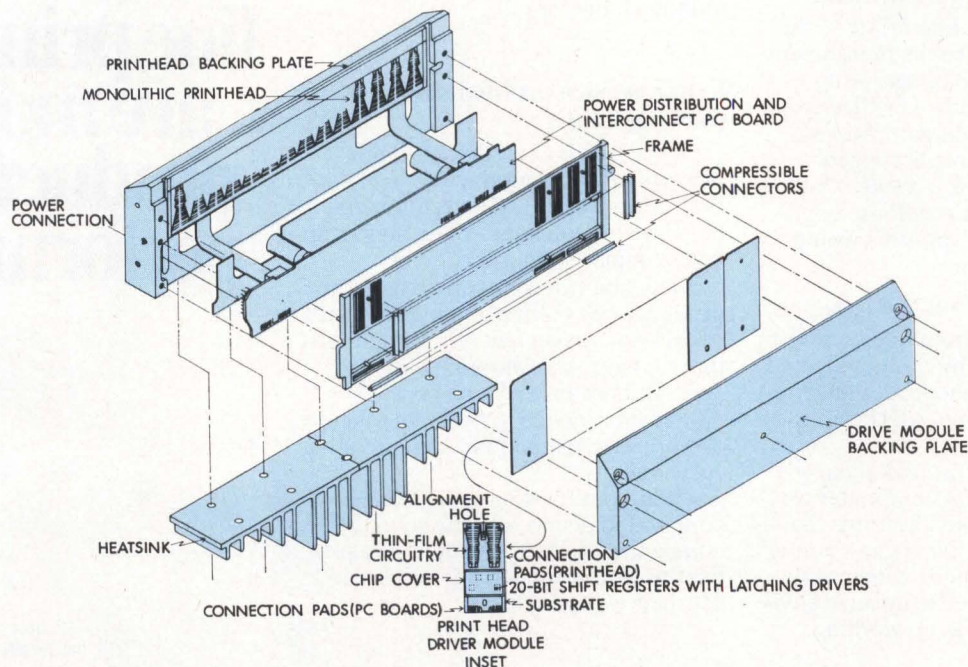


Fig 4 Exploded view of thermal printhead assembly. Each of seven printhead driver modules contains four 20-bit shift registers with latching print resistor drivers. These modules connect to monolithic printhead using compressible elastomeric connectors. Power and burn information come through single connector cable onto printed circuit board, which also connects to printhead with conductive elastomeric connectors. Two rigid backing plates hold entire printhead assembly together

WEDNESDAY

10

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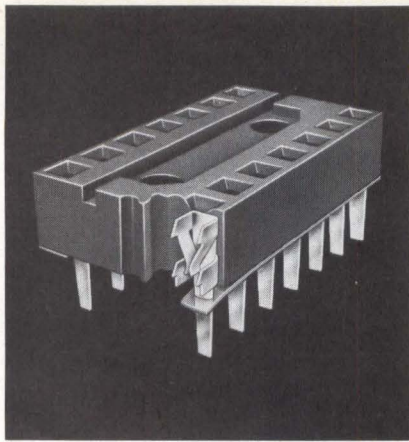
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controls handshaking with the data source. Character data enter the random access memory (RAM) buffer, which can store up to 80 characters, and then go to the character ROM, which encodes the characters into dot patterns. Character information to be printed arrives at the printhead one dot row at a time from the character ROM. Each printhead resistor can be accessed individually through seven shift register modules (Fig 5), with four driver

shift register, bypassing the character ROM, and then into the printhead.

Because power requirements to drive all 560 dots simultaneously would be excessive, maximum current to the printhead is limited to approximately 10 A. This value means that a maximum of 100 dots can be turned on at once. If more than 100 dots in a row must be "burned," several passes must be made with an increase in printing

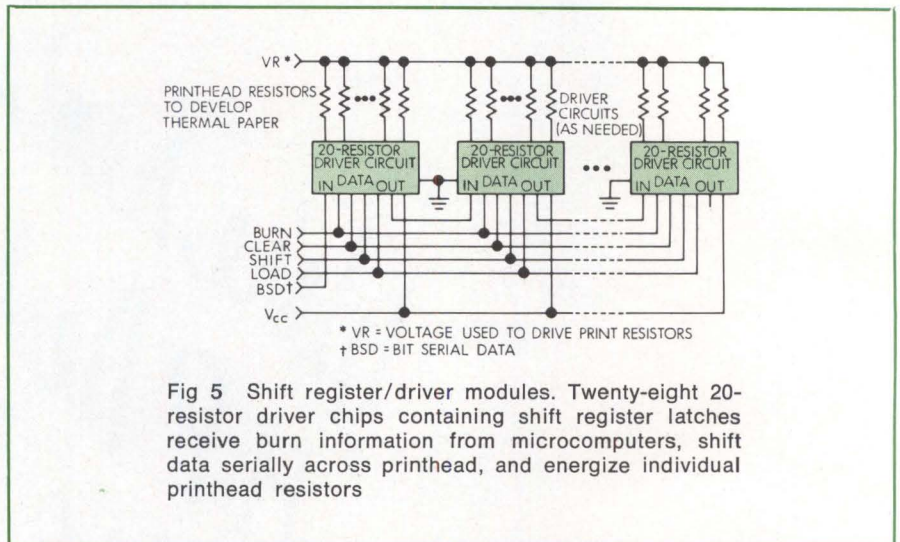


Fig 5 Shift register/driver modules. Twenty-eight 20-resistor driver chips containing shift register latches receive burn information from microcomputers, shift data serially across printhead, and energize individual printhead resistors

chips per module. Printing information is shifted serially through these modules and then latched into the driver chips, and current passed through the resistors "burns" the information onto the paper. Printing time is saved by loading the next dot row of data into the shift registers while the previous information in the latches is being printed. Dot patterns arrive in parallel format to the shift registers, and are shifted serially across the printhead until a full dot row is accumulated. This dot row is printed, and the stepper motor advances the paper vertically by an increment of one dot row. The sequence repeats until a full row of characters is printed. Then, the stepper motor advances the paper by a full line feed for spacing and the next line of text is initiated.

If graphics rather than character data are to be printed, a control instruction precedes the graphic data. The microcomputer interprets the data, not as ASCII characters, but as eight bits of graphic data. Via a multiplexer, these data pass directly to the parallel-in, serial-out

time. However, the decrease in normal printing speed or graphics applications is slight. In a typical alphanumeric printout, over 90% of the dot rows contain less than 100 dots that need to be "burned." In graphics mode, this percentage may increase or decrease according to dot density of the graphics output.

Summary

Depending on required printing speed, thermal printhead tradeoffs involve cost and wear characteristics for a particular application. Speeds on the order of 500 lines/min are available with printers using thin film resistive technology and page-wide fixed head mechanisms. Also, fixed head printers are capable of generating raster graphics. Offering easy interfacing as well as quiet reliable output, thermal printers are increasingly being used with computer terminals, mini- and microcomputers, automatic test equipment, graphics and medical systems, analytical laboratory systems, and data logging instruments. □

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141

Efficient Digital Encoding Scheme

Modified NRZ code immunizes record and playback systems against dc drift and bit slippage

Although the conventional non-return to zero (NRZ) code is the most efficient for recording digital data (if efficiency is measured by bits to unit length of tape ratio), it is subject to dc drift and bit slippage whenever long strings of 1s or 0s are encountered. Codes that insert check bits in the data to break up long strings alleviate this problem, but only at the expense of recording efficiency.

An improved code, called J-NRZ, gives 100% of NRZ efficiency yet also solves the dc drift problem. It does so by adding check bits in a specified format only when a long string is encountered. The rest of the data stream is encoded in standard NRZ format.

One such system is programmed to search for 32 consecutive identical bits. The playback system is able to handle up to 64 identical bits with-

out drift, thus ensuring a 2:1 error margin.

As shown in the Figure, the system converts the input data into NRZ, and a clock is generated from the data. If the input is already NRZ with a clock, it is routed to the next stage.

A preselected 32-bit word is stored in P/ROM, RAM, or other word generator. The word is symmetrical, ie, the same when played back in the forward or the reverse direction, and it is balanced with an equal number of 1s and 0s.

The circuit includes a counter that runs off the clock and resets each time there is a data transition. If the counter reaches a predetermined number (32 in this system), it triggers the controller to shift either the stored word, for a string of all 1s, or its complement, for all 0s into the data stream.

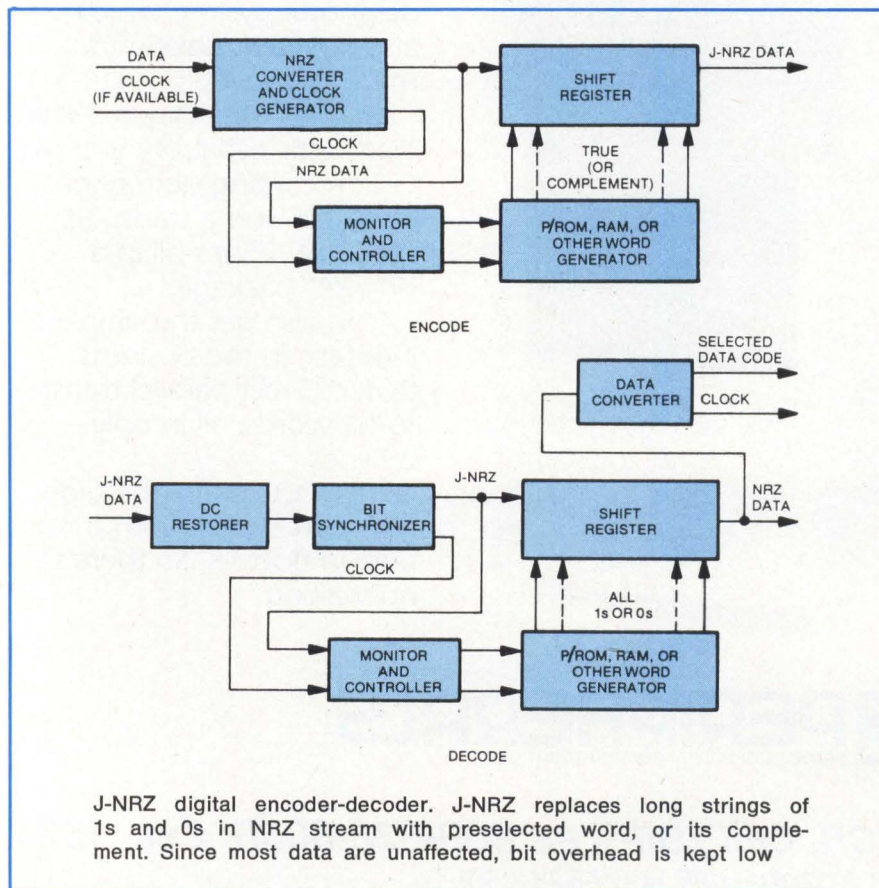
A shift register accepts the NRZ data bits in a serial train and holds them while the monitor, controller, and storage/transfer systems have time to function. If the predetermined number of 1s or 0s has been detected, the word is parallel shifted out of storage and into the shift register to replace the long string. The register then resumes serial transfer of the data.

On playback, the coded data are routed to a dc restorer and bit synchronizer. The input J-NRZ is processed by a monitor and controller stage that initiates a shift of all 1s upon detection of the coded word or of all 0s for the code word complement. Upon command from the controller, the storage P/ROM or RAM shifts all 1s or 0s back into the shift register, restoring the data to their original form.

Note

This work was done by David E. O'Brien III of Johnson Space Center. No further documentation is available. (MSC-18267)

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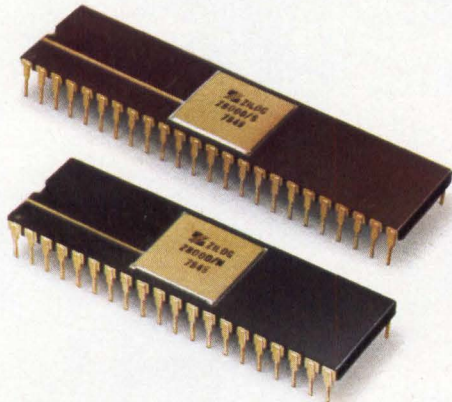
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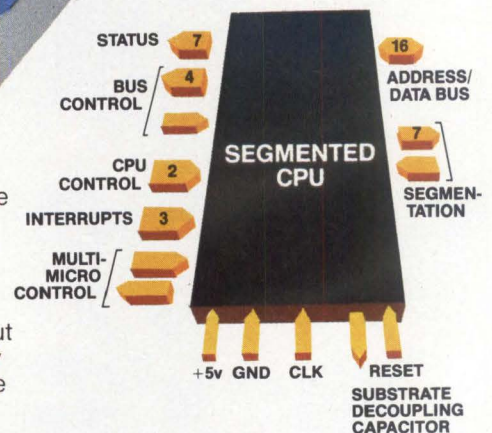


The Z8000 allows you to directly address up to 8 MB of memory. All 16 registers are a full 16 bits wide and are completely general purpose. The powerful, problem-solving instruction

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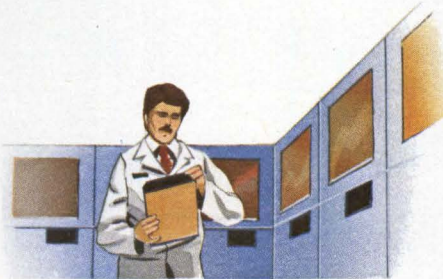
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CIRCLE 49 ON INQUIRY CARD

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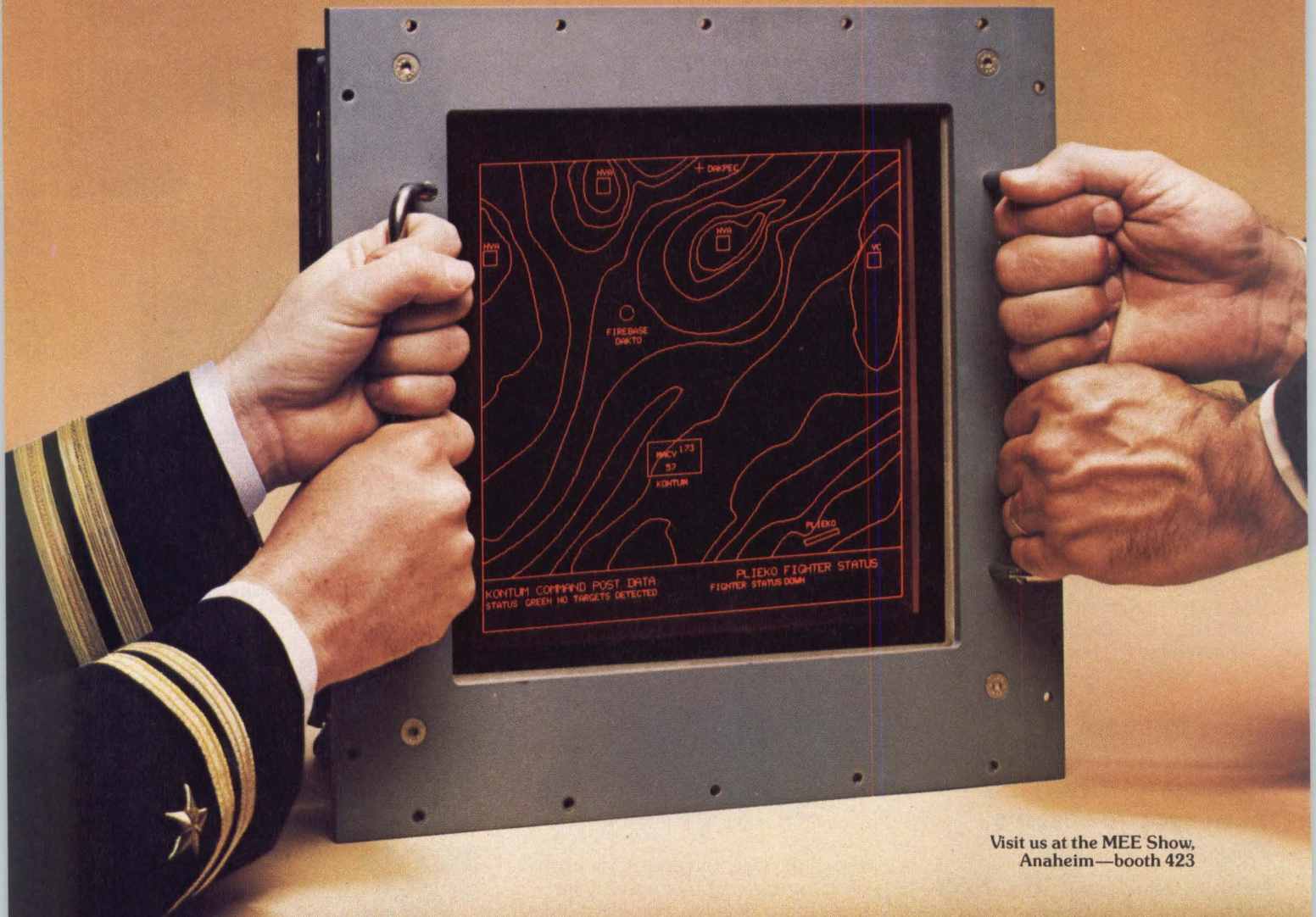
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INTERFACING FUNDAMENTALS: 6800 I/O AND SYSTEM CONFIGURATION

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Tychon, Inc

Andrew C. Staugaard
Jamestown Community College

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute and State University

Hardware aspects of the 6800 microprocessor require discussion in order to balance and augment the previous coverage of the chip's internal organization and instruction set. Examination of the pinout in Fig 1 shows that this microprocessor requires a single 5-V power supply and two nonoverlapping signals, which are labeled as $\phi 1$ and $\phi 2$. The standard 6800 chip has a maximum clock frequency of 1 MHz; however, 1.5- and 2.0-MHz versions are available—the 68A00 and 68B00, respectively. The $\phi 1$ clock signal is used for internal instruction sequencing, whereas the $\phi 2$ signal serves as an input/output control line for timing and synchronizing the 6800 with input/output devices. The usual 16 address lines, A0 through A15, and eight bidirectional data lines, D0 through D7, are provided to make up the external address and data buses, respectively.

Control signals for read/write (R/W) operations between memory and the 6800 chip are provided by the valid memory address (VMA) and R/W control lines. The R/W line indicates the direction of data transfer, being at a logic 1 for read and at a logic 0 for write. The VMA line goes to a logic 1 whenever the microprocessor places a valid 16-bit memory address on the address bus.

Hardware interrupts are provided through the RESET, IRQ, and NMI pins on the 6800 chip. These are all vectored interrupts that directly access interrupt service routines at specific memory locations. The 16-bit addresses of these locations are contained in the memory

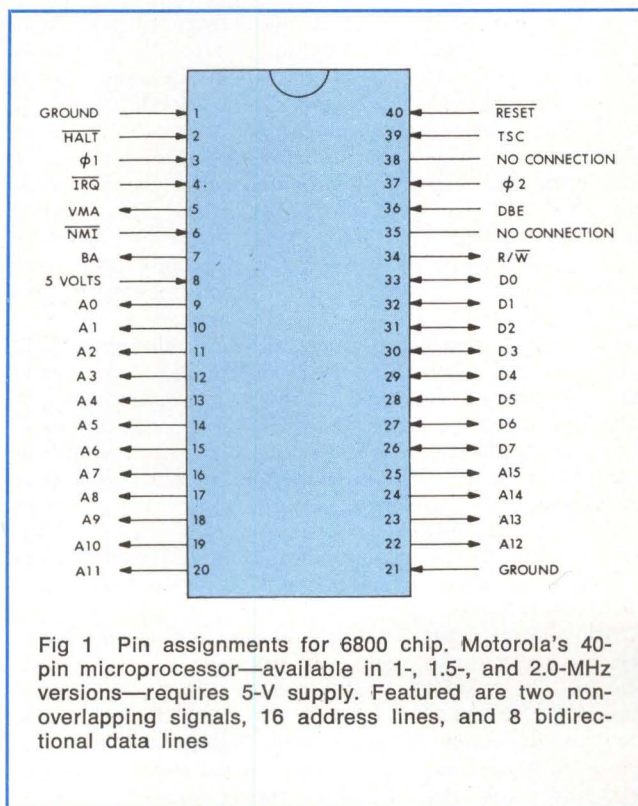


Fig 1 Pin assignments for 6800 chip. Motorola's 40-pin microprocessor—available in 1-, 1.5-, and 2.0-MHz versions—requires 5-V supply. Featured are two non-overlapping signals, 16 address lines, and 8 bidirectional data lines

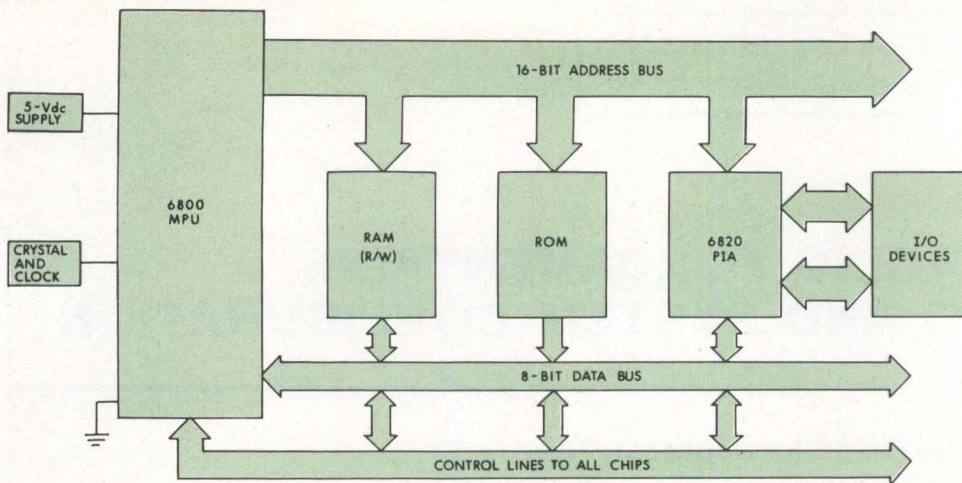


Fig 2 Microcomputer system configuration. Typical 6800 system which interfaces to I/O devices can handle majority of applications that are mainly aimed at small dedicated uses

region, FFF8H through FFFFH, where the letter H represents hexadecimal code. Three pairs of 2-byte addresses are stored in this region to facilitate the three different types of hardware interrupts. For example, $\overline{\text{RESET}}$ is used for system initialization and restart; the address for the routine is contained in locations FFFE_H (high byte) and FFFF_H (low byte). The $\overline{\text{IRQ}}$, or interrupt request, input is a maskable interrupt line that is ignored if the I flag bit in the internal condition code register is set. The address for the maskable interrupt routine is contained in locations FFF8_H and FFF9_H. Finally, the NMI, nonmaskable interrupt, input can never be masked out and is normally used for emergency interrupt situations. The address for the nonmaskable interrupt routine is contained in locations FFFC_H and FFFD_H. The microprocessor automatically stores its internal register contents on a stack in R/W memory when either the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ interrupts are acknowledged.

External bus control is provided with the bus control lines $\overline{\text{BA}}$ (bus available), $\overline{\text{DBE}}$ (data bus enable), and $\overline{\text{TSC}}$ (3-state control). These lines are normally used to effectively disconnect the microprocessor from the external bus system to allow direct memory access by external devices.

Fig 2 is a schematic diagram of a minimum 6800 system configuration. This type of configuration should accommodate at least 80% of the microcomputer applications since most microcomputers are used for small dedicated applications. The address bus contains address lines A0 through A15, the data bus contains data lines D0 through D7, and the control bus—which provides timing, synchronization, and supervision of data exchange between the microprocessor and external devices—normally contains ϕ_2 , $\overline{\text{VMA}}$, $\overline{\text{R/W}}$, interrupt lines, and bus control signals.

Also shown in Fig 2 are R/W memory, read only memory (ROM), and the peripheral interface adapter (PIA). The PIA is a programmable input/output (I/O) chip that simplifies interfacing with the "outside world." It provides decoding, latching, and 3-state buffering for I/O devices such as switches, keyboards, displays, analog to digital (A-D) and digital to analog (D-A) converters.

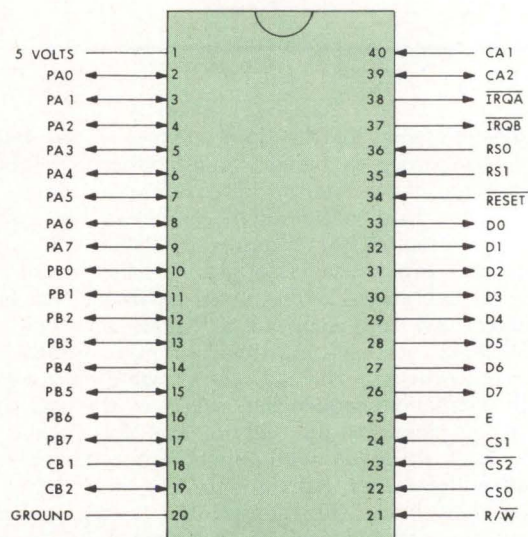


Fig 3 PIA pin assignments. Motorola's 6820 programmable PIA chip interfaces with peripherals. Functions performed are decoding, latching, and 3-state buffering. Ports A and B are both 8-bit I/O ports; CA and CB are two control lines for each port

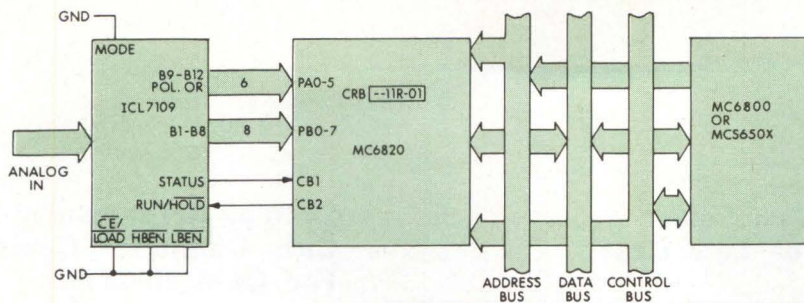


Fig 4 Interface to A-D converter. Microcomputer system is interfaced to 7109 A-D converter through 6820 chip. Both PIA ports are configured as input ports (Courtesy of Intersil, Inc)

The 6820 PIA contains two 8-bit I/O ports, called port A and port B. The eight bits within each port can be independently programmed as either input or output with the use of an associated internal data direction register (DDR) assigned to each port. For each port the PIA also has two control lines—CA and CB—that provide partial or complete handshaking capability. In the complete handshaking mode, one control, CA, is used as an interrupt input line and the other, CB, is used as an output strobe. The pin configuration for the 6820 PIA is shown in Fig 3.

Data communication between the microprocessor and an I/O device is provided through the use of the technique called memory mapped I/O. With memory mapped I/O, each I/O device is treated as a memory location or group of memory locations. No special input or output instructions are needed. For example, to send data to an I/O device, a store accumulator in memory (STA) instruction is executed; to read data from an I/O device, a load accumulator from memory (LDA) instruction is executed. Each port in the PIA chip in Fig 2 has a unique address assigned to it; to input or output data, memory R/W operations that address the proper port are executed.

Fig 4 demonstrates how the system in Fig 2 can be interfaced to an A-D converter. The A-D device used is the low cost Intersil 7109 12-bit A-D converter, which provides up to 30 conversions/s and can be operated in a direct or a complete handshaking mode. Given an analog input signal, the A-D converter provides 14 bits of data to the PIA: 12 data bits (B1 through B12) plus a polarity bit (POL) and an overrange bit (OR). The 12 data bits are divided into a low order data byte (B1 through B8) and a high order data byte (B9 through B12). The low order byte is connected to PIA port B lines PB0 through PB7; the high order byte, including POL and OR, is connected to port A lines PA0 through PA5. Therefore, both PIA ports are configured as input ports.

The PIA control line CB1 acts as an interrupt input and is programmed to generate an interrupt request to the 6800 on a high to low transition of the A-D converter's STATUS pin. Control line CB2 is programmed as an output line and is connected to the A-D converter via the RUN/HOLD pin. If CB2 is held high, the A-D converter is permitted to provide continuous conversions by interrupting the 6800 via the CB1 line as soon as each conversion becomes available; this is the RUN mode of operation. The A-D converter contains an output latch so that data will not be lost before the microprocessor acknowledges

the interrupt. If CB2 is held low, the conversion process can be halted. When desired, a conversion can be initiated by strobing the A-D converter with a pulse from the CB2 line. Similar considerations for the newer Motorola microcomputer chips will be examined, commencing with the MC6802 and MC6808.

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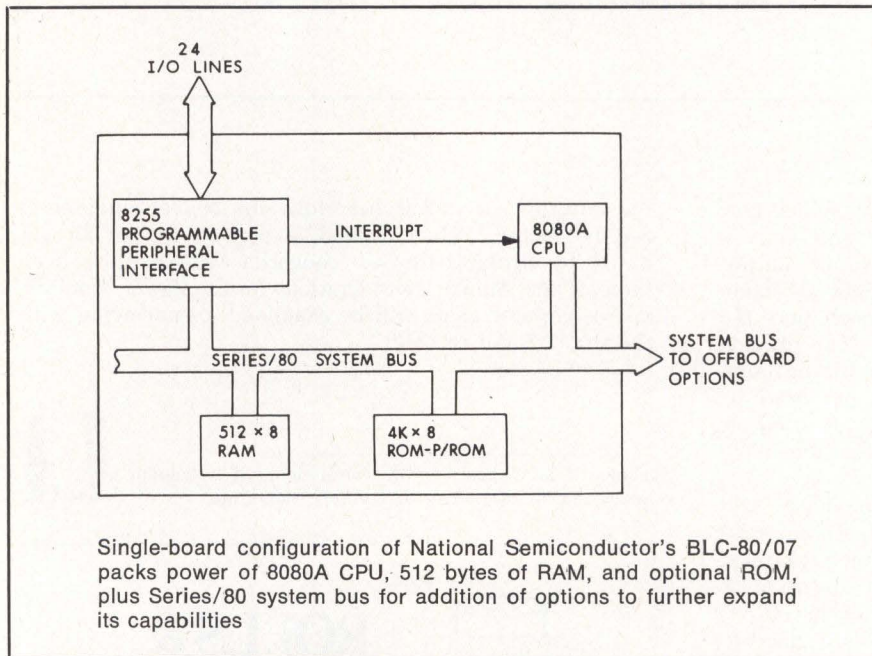
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Board Level Microcomputer Can Solve Dedicated Control Problems at Low Cost



Dedicated control and processing applications are handled by the BLC-80/07 single-board computer that offers the computing power of a BLC-80/10 at a lower cost of \$365. Based on the 8080A microprocessor, the MULTIBUS™ compatible computer can use BLC/SBC Series/80 hardware and software products. Expansion at a reasonable incremental cost is possible with the addition of such modules as a 4-slot chassis, power supply, RAM and ROM in combinations up to 64k bytes, various I/O controllers, and digital and analog I/O. National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, burns in all boards at 55 °C for 8 h.

System components are the 8080A CPU, 512 bytes of static RAM, sockets for up to 4k bytes of P/ROM, 24 parallel I/O lines, and a system clock. The TTL compatible I/O lines are controlled by an INS8255 programmable peripheral interface circuit. The lines configure to various unidirectional/bidirectional modes. Compatible I/O terminator modules are a 220/330-Ω divider and a 1-kΩ

pullup. The variety of driver circuit types for this I/O section are inverting, noninverting, high voltage, and open collector combinations with sink current capacity ranging from 16 to 48 mA. The computer addresses 64k bytes of memory and has an access time of less than 500 ns.

The CPU's single-level interrupt for recognition of events may originate from four sources or-tied to the single level. When an interrupt is received, an in-process instruction is completed and the program is then suspended. The CPU passes control to a user defined interrupt service routine which saves system conditions while the interrupt is processed.

Addressing modes are direct, register, register indirect, and immediate. There are 111 instruction types, six 8-bit general purpose registers, an 8-bit accumulator, 16-bit program counter, and 16-bit stack pointer. A subroutine mechanism uses the stack pointer with push and pop instruction to implement call and return instruction types. All address, data, and control signals are Tri-State™ TTL compatible.

System Arrangement Cuts Computer Costs For OEM Houses

The Semi-System concept of OEM computer systems was conceived by General Robotics Corp, 57 N Main St, Hartford, WI 53027, as a practical means of saving money. The OEM buys the system without the LSI-11 processor and disc drives installed; these are then purchased directly from Digital Equipment Corp and a disc drive manufacturer, eliminating the cost markup that a full system supplier would add.

Assembly of the whole system is easy. The LSI-11 PC module plugs into the backplane, and cables are plugged into the disc drive. Floppy disc drives are mounted with two bolts, and a cartridge disc drive is mounted in a rackmount cabinet.

The first floppy disc configuration is based on the company's GEMINI package with space for two floppy disc drives to be packaged in a 10.5" (26.7-cm) high rackmount or desktop box. It is complete with power supplies and fans, backplane and card cage, 64k bytes of RAM, hardware bootstrap, line frequency clock, and serial RS-232 port; the other configurations all contain these same features. A floppy disc controller handles either single- or double-sided double-density floppy discs using GCR techniques and storing up to 2.5M bytes. Shugart, Qume, and CDC are among the compatible drives. Price is \$4200 for quantity 50.

Based on the TRISTAR, the second floppy disc configuration can handle up to three floppies mounted in a separate box provided with the system. The controller is contained in a separate 5.25" (13.34-cm) rackmount or desktop box. The quantity 50 price is \$4900.

A hard disc system is similar, with a controller in a 5.25" (13.34-cm) package. Standard cartridge type drives that interface the LSI-11 Q-Bus include Pertec, CDC, EM&M, Western Dynex, and Diablo. The cost is \$4200 (quantity 50). Storage module drives, configured the same as this system, are \$4900 in quantity 50. It interfaces with most standard drives which have an SMD interface.

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CIRCLE 79 ON INQUIRY CARD

Essential Small Business Computer Elements Are Reduced To Three Cards

The minimum configuration electronic package of the model 770 consists of a CPU/video board, memory combination board, and I/O board—all 7 x 12" (18 x 30 cm)—in a 7-slot card cage with power supply and system cables. Psytek Computer Systems, 1900 Pickwick Ave, Glenview, IL 60025, has disregarded general purpose features and has instead included only the basic elements of concern to small business computer manufacturers and users. Physical compatibility with Intel's MULTIBUS™ structure permits expansion with peripheral cards that use this format.

The standard system comes with 48k characters of internal memory and with system diagnostics and load procedures resident in P/ROM. Two IBM compatible full-size floppy discs store 0.5M characters. These can expand to 294k characters internally and 35M characters externally. The 12" (30-cm) video monitor delivers 30 lines of 80 upper/lower case characters. A detachable keyboard also contains a separate numeric pad. Several printers can be attached to the parallel interface.

The CPU/video board contains a Z80A microprocessor, bus control electronics, and video system with 4k bytes of memory for the CRT display and the CPU's scratchpad. The 48k bytes of RAM and 4k bytes of ROM are on the memory board which allows 16 banks of 16k-byte RAM to be used in the system. The first of these banks is on this card; other banks are added with an optional PC card.

The final board interfaces the computer with up to four floppy drives, one keyboard, and one printer. Programmable tone generator and system control logic allow implementation of the computer's front panel on the system keyboard. Optional boards are a serial/parallel I/O board, a graphics display board for B/W and color graphics, and extended memory boards with four switchable 16k-byte banks of RAM.

System software includes extended BASIC, text editor, Z80 assembler,

program debugger, I/O and utility routines, and a disc operating system with sequential and random files, all of which run under the company's Supervisor. This allows the modules to interact efficiently. Software business applications are available. The system supports CP/M™; thus, users have a choice among several BASICs, FORTRAN IV, COBOL, PASCAL, and APL. Circle 411 on Inquiry Card

Desktop Computer Options Add Communications and Storage Capabilities

A dual diskette drive and two communications packages are major additions that Durango Systems Inc, 10101 Bubb Rd, Cupertino, CA 95014, is offering as options to the portable F-85 computer (see *Computer Design*, Dec 78, p 132). Model 8705 auxiliary drive option adds two 5.25" (13-cm) 473k-byte diskettes to extend the basic system's online storage to four drives totaling approximately 2M characters. It enables separate device oriented files and reduces diskette manipulation during processing. Housed in an 8.55 x 7.75 x 13.25" (21.72 x 19.69 x 33.66-cm) self-contained enclosure with power supply, the \$3085 unit connects to the computer via a single logic cable through an existing back connector. Drives, assigned physical addresses 2 and 3, operate in the same manner as integral drives 0 and 1.

Communications options transmit and receive data from remote computer systems. Both packages consist of a hardware and software module. The 8535 asynchronous package works over switched telephone network or private point-to-point lines. It supports features used by other computer manufacturers when operating in ASCII asynchronous serial bit mode. Included are batch, interactive, or combined modes; switched or private line operation; several full- or half-duplex protocols; error logging; and a horizontal tabbing facility. Transmission rates are from 50 to 9600 baud. The software provides data routing to a printer, video screen, or mass storage.

Using binary synchronous communications procedures, the 8535 package emulates the protocol used by IBM 2780 and 3780 data communications terminals. The emulator operates under control of the DX-85 operating system in batch mode.

On transmission to the F-85, all data are transferred from a named mass storage file while received data can be routed to the printer, video screen, or mass storage. Operation is in either point-to-point or multipoint mode. The protocol also includes block checking and automatic retransmission. Rates range from 2000 to 9600 baud.

Both packages contain command sets for specification of various line parameters and operating states. Prices are \$625 and \$1275, respectively. A \$115 security lock provides controlled access to the computer through a keylock switch on the keyboard. Three positions are disable, enable, and supervisory. A random access fixed disc drive with a storage capacity of 12M bytes is planned for the fourth quarter of 1979.

Circle 412 on Inquiry Card

Storage Ranges From 250k to 1.2M Bytes With S-100 Floppy Discs

S-100 systems running at 2, 4, or 5 MHz can accept any of three 8" (20-cm) full-sized floppy disc subsystems. Drives are mounted in single or dual cabinets with self-contained power supply, detachable line cord, and detachable 50-conductor signal cable. Also included are the Disk/ATE operating system and the BASIC-V advanced BASIC language interpreter with virtual memory addressing.

The single-density DISCUS I™ system holds 250k bytes of data, using IBM soft-sectored format, as do the other two systems. It uses the Disk Jockey I™ single-density controller which has 0.5k of ROM with disc utility subroutines, 256 bytes of RAM, and a software drive serial I/O port.

Quad-density DISCUS 2+2™ uses double-sided floppy disc drives to store 1.2M bytes of data. DISCUS 2D™ is a double-density floppy disc system with a capacity of 600k bytes; it uses a single-sided drive.

Thinker Toys, 5221 Central Ave, Richmond, CA 94804, has developed the Disk Jockey 2D™ controller for both of these systems. It features a serial I/O port with a UART and programmable baud rate generator, 1k of RAM, and 1k of ROM which executes such disc functions as read sector, write sector, and bootstrap. Jump start logic automatically loads standalone systems on power-up.

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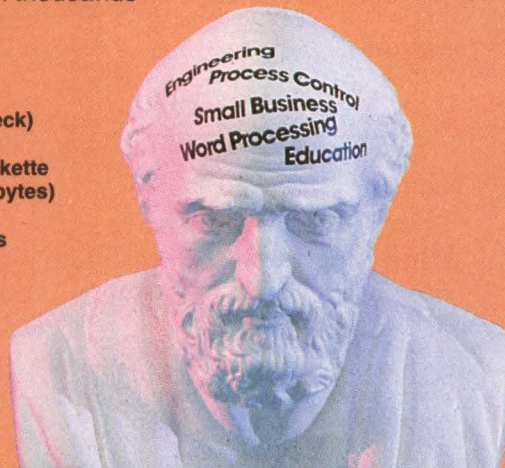
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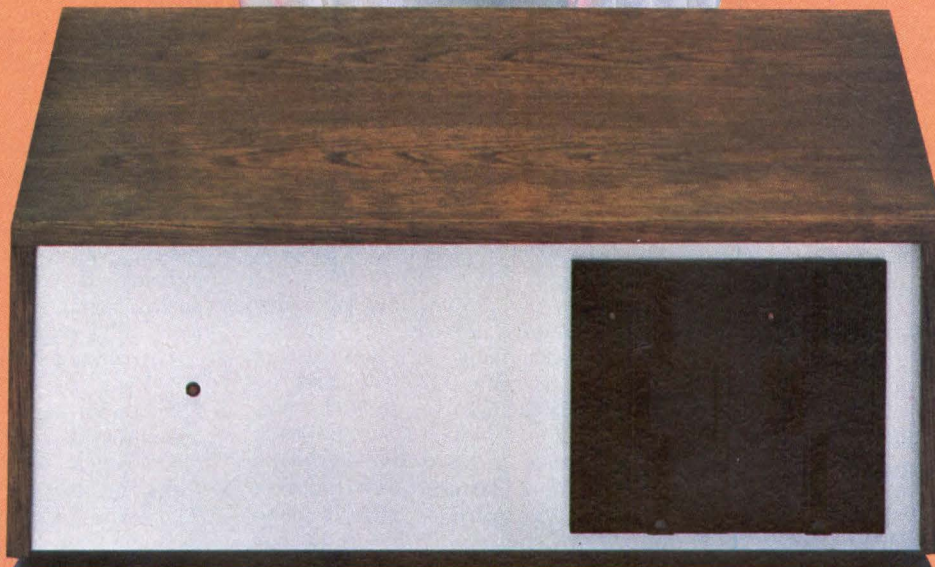
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CIRCLE 81 ON INQUIRY CARD

Faster Execution of Instructions Enhances 6800 Microprocessor

Using a 2.5-MHz clock, S68H00 executes one data access instruction/two clock cycles, obtaining a processing speed that is claimed to be 2½ times that of the standard 6800. High speed processing in instruments and numerical controllers can be performed more efficiently. American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, is supporting the processor with the newly introduced S68H21 peripheral interface adapter which has a 2.5-MHz speed. This enables configuration of a high speed microcomputer using two of the company's S2114 1k x 4 RAMS and an S4216B 2k x 8 ROM.

Other aspects of the microprocessor are identical to earlier versions. Available in ceramic and plastic packages, it uses 8-bit parallel processing, has an 8-bit bidirectional data bus, 16-bit address bus, and a 72-instruction set with seven addressing modes. Execution is from two 400-ns machine cycles for most instructions up to 12 cycles for a software interrupt.

Circle 414 on Inquiry Card

Slave Processor Aids Systems Requiring Distributed Power

The intelligent, Z80 based 1861A peripheral controller has up to 16k of memory and can address all the memory and I/O in the Flexibus II system to which it is added. Its four independent serial channels are configured by onboard jumpers to synchronous or asynchronous operation with internal or external clocks. Independent single-channel communications adapters provide full signal flexibility and modem control for each channel. These serve to interface standard TTL signals, output from the processor to 20-mA/PCS party lines, EIA RS-232-C, -422, or -423 interface signals. Internal clock rates are program selected. Data rates up to 500k bits/s are possible.

Communications channels are hardware compatible with such industry communications protocols as async, BSC, SDLC, HDLC, ADCAP, and Canadian, U.S., and European virtual telecommunication networks. Thus, the system can control subsystems from several manufacturers.

A multiprocessor debug tool has been announced simultaneously by Process Computer Systems Inc, 750 N Maple Rd, Saline, MI 48176. The accessory for the controller allows simultaneous debugging of multiple CPUs. Any memory locations in a designated processor can be examined and altered synchronously or independently. Breakpoints are set, cleared, or coordinated from either the local or development system console.

Circle 415 on Inquiry Card

Two Boards Generate High Resolution Graphics For MULTIBUS Systems

The RG-SBC-VGI vector generator and RG-SBC-MI refresh memory form the RG-SBC configurable graphics generator to produce a composite TV signal for display on a standard 525-line (625 optional) TV, used in conjunction with Intel MULTIBUS™ systems. Up to eight refresh memory boards combine with one vector generator to give graphics in black and white, color, or up to 16 shades of gray. Three refresh memory boards are required for red, green, and blue outputs for color monitors that accept TTL level RGB inputs. Resolution ranges from 320 x 240 to 640 (H) x 480 (V). Complex displays may be programmed in BASIC.

The instruction set that Raster Graphics, PO Box 23334, Tigard, OR 97223, has included controls the vector generator which automatically starts, issues a busy signal to the status port, and stops when the vector is written into the refresh memory. Instruction ports reside in one page of user selected I/O address space. Hardware performs the task of creating the vector, writing it into

refresh memory, and producing the TV signal, all transparent to the user. Chaining vectors together creates symbols, shapes, and patterns.

Single-refresh memory configurations are used with static display formats that are updated infrequently, or where higher resolution is required, using all the available memory. Dual-refresh memories are necessary for complex moving displays in order to eliminate objectionable R/W interference that occurs when data are written or read from the same memory. Users may display data from either refresh memory by issuing the switch command. Previously displayed data may be optionally erased or retained when memories are switched, thus providing stored and nonstored modes of operation. Single-refresh configurations need one stored and one nonstored mode; dual-refresh configurations require two of each mode.

Circle 416 on Inquiry Card

Impact Matrix Printer Produces µComputer Hard Copy at 132 Char/s

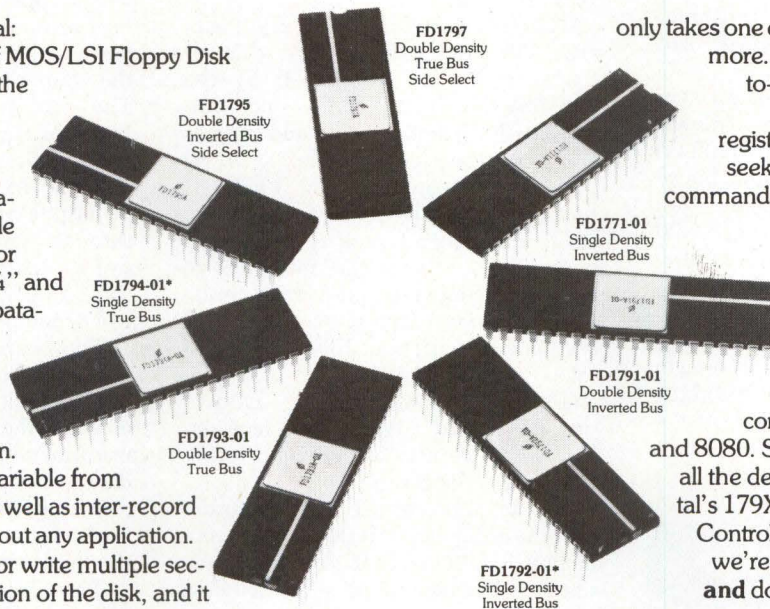
A stepper motor driven integral tractor mechanism with precision incremental paper motion and forms width and thickness adjustments, continuous loop ribbon with reinking roller for 3M- to 5M-character life, and only two moving parts to drive the printhead and drive motors are mechanical features of the model 801 that assure high quality for microcomputers such as Radio Shack's TRS-80, the Apple II, and the CompuColor. It connects via either an RS-232 serial interface or Centronics compatible parallel interface.

Distributed by Vitek, 1160 Barbara Dr, Vista, CA 92083, the unit prints 132 upper and lower case characters/s, 80 columns wide, on up to five copies of standard computer forms up to 9.875" (25 cm) wide. The standard set consists of 96 ASCII characters. A 127-character line buffer is standard. The printer produces a 7 x 7 dot matrix.

Circle 417 on Inquiry Card

The only complete family of floppy disk controllers

From Western Digital: a complete family of MOS/LSI Floppy Disk Controllers to meet the demand of double-density head-on. Introducing the 179X. A new generation of Single/Double density controllers for use with both the 5¼" and 8" drives. Full compatibility with the IBM 3740 and System 34 formats is standard. Need more storage? No problem. Sector lengths are variable from 128 to 1024 bytes as well as inter-record gap sizes to fit just about any application. You can even read or write multiple sectors within 1 revolution of the disk, and it



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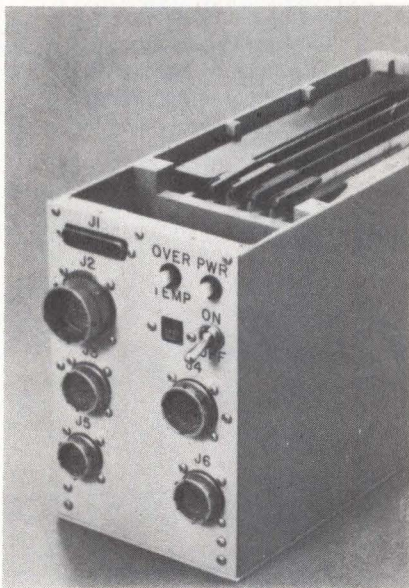
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Support Modules Erect Severe Environment Microcomputer System

A building block approach to designing a custom microcomputer system for industrial, military, and other severe environment applications simplifies the task and cuts development costs. The base of the SECS 80 system is the SECS 80/10A, a ruggedized version of Intel's iSBC™ 80/10A single-board microcomputer (see *Computer Design*, Jan 79, pp 146, 148). Support modules offer a choice of I/O expansion board, RAM, P/RAM, EPROM, digital tape recorder and controller, high speed arithmetic unit, A-D converter, power supplies, and chassis.

All modules are mounted on standard 9 x 6" (23 x 15-cm) full-ATX compatible PC cards. A half-ATX chassis with side ventilation houses either six cards or four cards and a power supply (28-Vdc or 115/220-Vac versions). Meeting MIL-E-5400, -16400, and -4158 requirements, the cards use NAFI style fork and blade connectors which withstand vibration levels as high as 20 g without intermittent connection. Each is uniquely keyed and may be blind mated.



Ruggedized module boards for harsh applications include I/O, memory, tape recorder and controller, arithmetic, and ADC that fit into EMM/SESCO's chassis with SECS 80/10A CPU card to form SECS 80 system

Integral heatsink and stiffening bars offer structural strength and thermal conduction efficiency. All microcircuits have been processed to MIL-STD-883 Level B. Operating temperature is -55 to 85 °C.

The 80/116 single-board RAM has 4k x 1 static devices, resulting in a 16k x 8-bit capacity. Starting address for 16k contiguous addresses is jumper selectable. R/W data buffers are included, and all data, address, and command signals on the bus are TTL compatible. Cycle time is 450 ns and access time is 385 ns.

The EPROM-P/RAM offers optional versions of 2k, 4k, 8k, 16k, and 32k. Addresses are jumper selectable for each 8k block. Programming is handled under software control from the SECS 80 bus. Both types of memory expansion are through direct SECS 80 bus interface.

The interface between the MIL-STD-1553 bus structure and that of the SECS 80 bus is handled by the 80/1553 bus interface. A microprogrammed controller, ALU and associated registers, control file, SECS 80 port, and two independent 1553 bus ports comprise the first section of the card. The second part is a memory port which allows the interface to appear as an I/O port with independent DMA capability. The final section contains two 1553 bus interfaces each consisting of an 8-bit shift register, Manchester encoder/decoder, and transmitter/receiver. The interface acts as a remote terminal or as a bus controller.

Up to four SETS-1 tape recorder units are directly interfaced and controlled by the TCI. It provides Manchester data encoding and decoding, preamble and postamble, and CRC generation and checking. Data transfer rate is 48k bits/s using phase encoding. EMM/SESCO, 20630 Plummer St, Chatsworth, CA 91311, has also included three 16-bit registers for command status and I/O register data.

Three other modules round out the system. The 519 programmable I/O expansion board has 72 programmable I/O lines with jumper selectable I/O port address and interval timer. Intel's 8259 programmable interrupt controller (PIC) provides vectoring for eight interrupt levels.

Algebraic, trigonometric, inverse trig, and logarithmic functions are provided by the AUI board, with single-precision (16-bit) fixed point format, double-precision (32-bit) fixed point format, or 32-bit floating point format. A 16-bit counter moni-

tors the Advanced Micro Devices AM9511 arithmetic processing unit. An option generates system interrupts 4, 5, 6, or 7 at the end of an operation.

Last, the A-D converter, a complete analog I/O subsystem, provides 16 single-ended input channels in its data acquisition section, along with sample/hold, programmable gain, and instrumentation amplifiers, and a 12-bit ADC. Analog output capability is possible with two optional 12-bit DACs and two optional 4- to 20-mA current outputs.

Circle 418 on Inquiry Card

Microcomputer Speaks With Help of Peripheral Card and Software

Verbal operator prompting or warnings are an added dimension to computer programs, made possible with the SuperTalker peripheral system. The card from Mountain Hardware, Inc, 300 Harvey W Blvd, Santa Cruz, CA 95060, plugs into the peripheral slot on the Apple II microcomputer to output high quality human speech through a loud speaker (or a PA or stereo system) under program control. It is particularly useful in control or monitoring applications.

The board's electronic circuits convert the analog microphone signals into a digital pattern that is stored in RAM; these stored speech data are manipulated like any other stored data. The board also accepts the digital patterns and transforms them back into audible signals through the loudspeaker.

The SuperTalker disc operating system allows output of human speech under program control with direct I/O routines. It also provides a preparation program for creation of voice files on diskette. The BASIC routines require only 1-line statements to output a word or phrase; the routines also support cassette storage.

Specifically, the operating system and editor package—VPS (Vocal Preparation System)—allows the user to develop a phrase diskette which may contain many tables of phrases (the basic data element accessible by the peripheral). Each table can contain several words, phrases, or whole sentences. Up to 47 phrase tables can be held on each diskette; 454 sectors on the diskette are available for the phrase tables.

The VPS is structured with three main levels. The main command level

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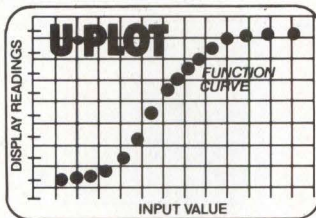
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```
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000,010-015
SELECT ONE
FUNCTION
1 MILLIVOLTS DC
2 OHMS
3 RTD
4 THERMOCOUPLE
5 BCD
```

CASSETTE LIBRARY. Once your program requirements have been defined, they can be saved on the built-in cassette. This lets you create a library of application tapes. Simply drop in a cassette and the Datalogger will completely program itself. Changing programs, therefore, is as easy as changing cassettes. The same cassette deck can be used to record measured data for future reference.

COMPLETE COMMUNICATION. The built-in CRT provides more information than possible with conventional datalogger displays. You can see 10 channels of system information at a single glance. For hard copy, a standard, built-in alphanumeric printer quietly records data. To communicate with peripheral devices, the 3000 offers the widest variety of interfaces. ASCII outputs, both serial and parallel, relay outputs, external condition input, and composite video output are all standard.

COMPLETE COMMUNICATION. The built-in CRT provides more information than possible with conventional datalogger displays. You can see 10 channels of system information at a single glance. For hard copy, a standard, built-in alphanumeric printer quietly records data. To communicate with peripheral devices, the 3000 offers the widest variety of interfaces. ASCII outputs, both serial and parallel, relay outputs, external condition input, and composite video output are all standard.

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affects whole phrase tables. At this first level, the user enters the configuration and confirmation mode, verifying the number of disc drives, the slots in which the controllers are located, and the drive numbers. Commands are included to delete, edit, initialize, list, and output phrases.

The second level is the Edit Command level, entered from the first level. Basically the same as the main level, these commands affect only one phrase table and those phrases within it. The bottom level—voice creation—is entered from the previous level. The user types a character string (up to 40 characters long) and then records the vocal phrases for the current phrase table.

In addition to software control of record and playback modes, the user may select the digitizing rate—512, 1024, 2048, and 4096 bytes/s of speech—and the playback volume—four software selectable levels. The higher the digitizing rate, the better the quality; the most useful rates are 2k and 4k/s. Frequency response is filtered to 300- to 3000-Hz human voice range for clarity.

The \$279 peripheral consists of the card, microphone, loudspeaker, software, and two ready to run programs—Accent, a talking language translator, and Talking Color Math. A 50-s realtime speech output can be stored at a 2k-byte rate on one Apple II diskette. A 2-W audio amplifier is contained onboard to drive the speaker.

Circle 419 on Inquiry Card

Design Method Integrates LSI-11/2 μ Computer With IEEE/CAMAC Standard

Packaging of Digital Equipment Corp's 16-bit LSI-11/2 microcomputer on a single-width CAMAC (computer automated measurement and control) board, allows the computer to be integrated into the MIK-11/2 system, which serves either as a stand-alone unit or as an auxiliary unit. The other elements—an asynchronous serial port for RS-232-C or 20-mA loop interfacing (functionally identical to DEC's standard serial port), a controller that interfaces the computer bus and CAMAC Dataway, 16k- to 32k-word RAM with automatic refresh, and a 256-word ROM with Dataway, memory, and register diagnostics—are compatible with the existing MIK-11 bus. Software support includes RT-11 and RSX-11 operating

systems, BASIC, FORTRAN, APL, FOCAL, and MACRO II, as well as other PDP-11 compatible software.

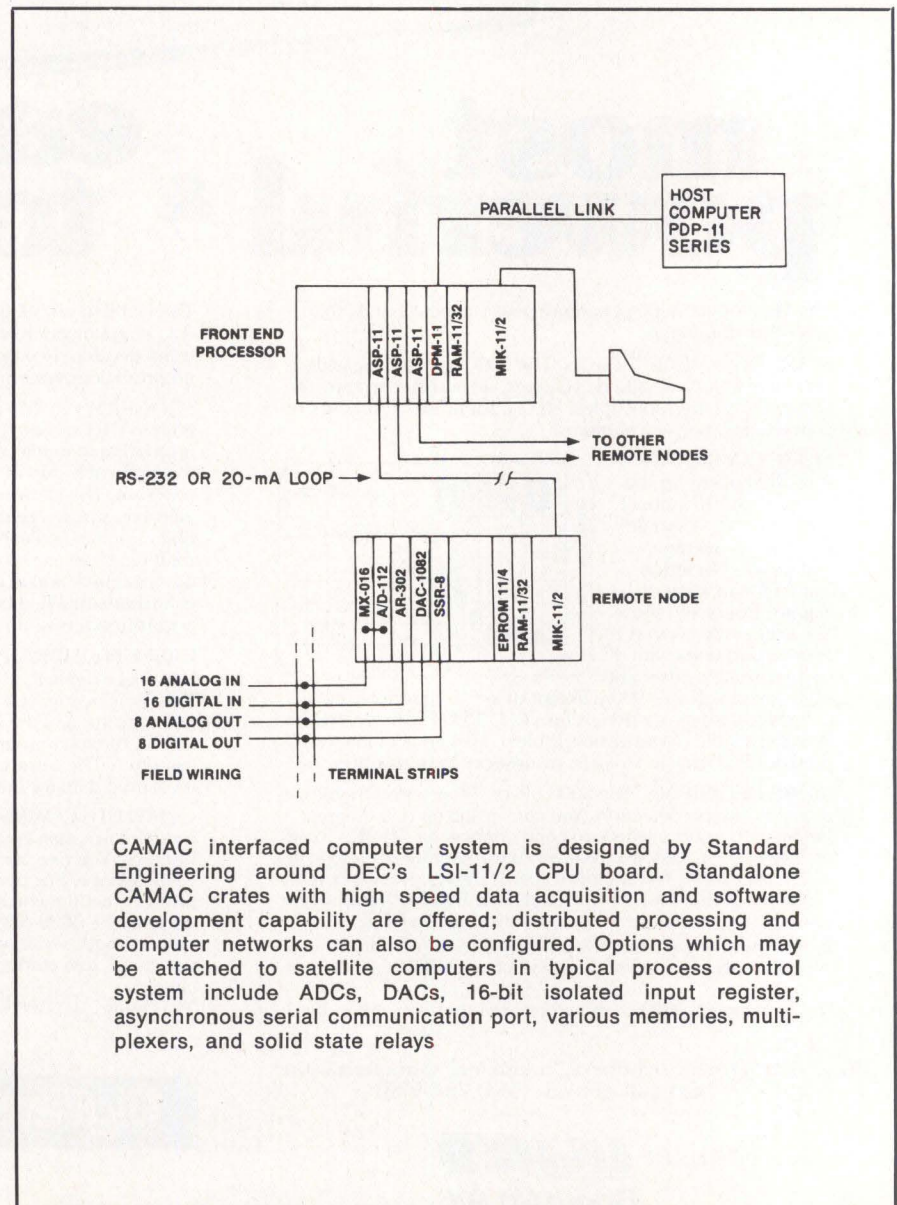
Characteristic of the Dataway interface is that it is mapped into a segment of Unibus address space, making it transparent to the LSI-11. Each subaddress and station number is assigned an LSI bus word address; thus for 16-bit transfers, the full power of the microcomputer's 400-instruction set is brought directly to the Dataway. Control status register and high data register contain all information relevant to a Dataway cycle. Both registers are readable and writable from the computer.

Standard Engineering Corp, 44800 Industrial Dr, Fremont, CA 94538, expands the capabilities of the LSI-11/2 by adapting it to process con-

trol, data acquisition, distributed processing, and computer networks. Combination of several satellite crate controllers with a larger host CPU offers one powerful configuration.

Selection of various options alter the system with the addition of a 16k- or 32k-word RAM with internal refresh and 256-word bootstrap P/ROM, 4k EPROM with onboard programming capability, 8k dual port static memory for sharing of a memory block by two processors, and dual floppy discs and interface. In addition, there are add-on asynchronous and synchronous serial communication port modules and a peripheral interfacing adapter board for all LSI-11/2 compatible devices.

Circle 420 on Inquiry Card



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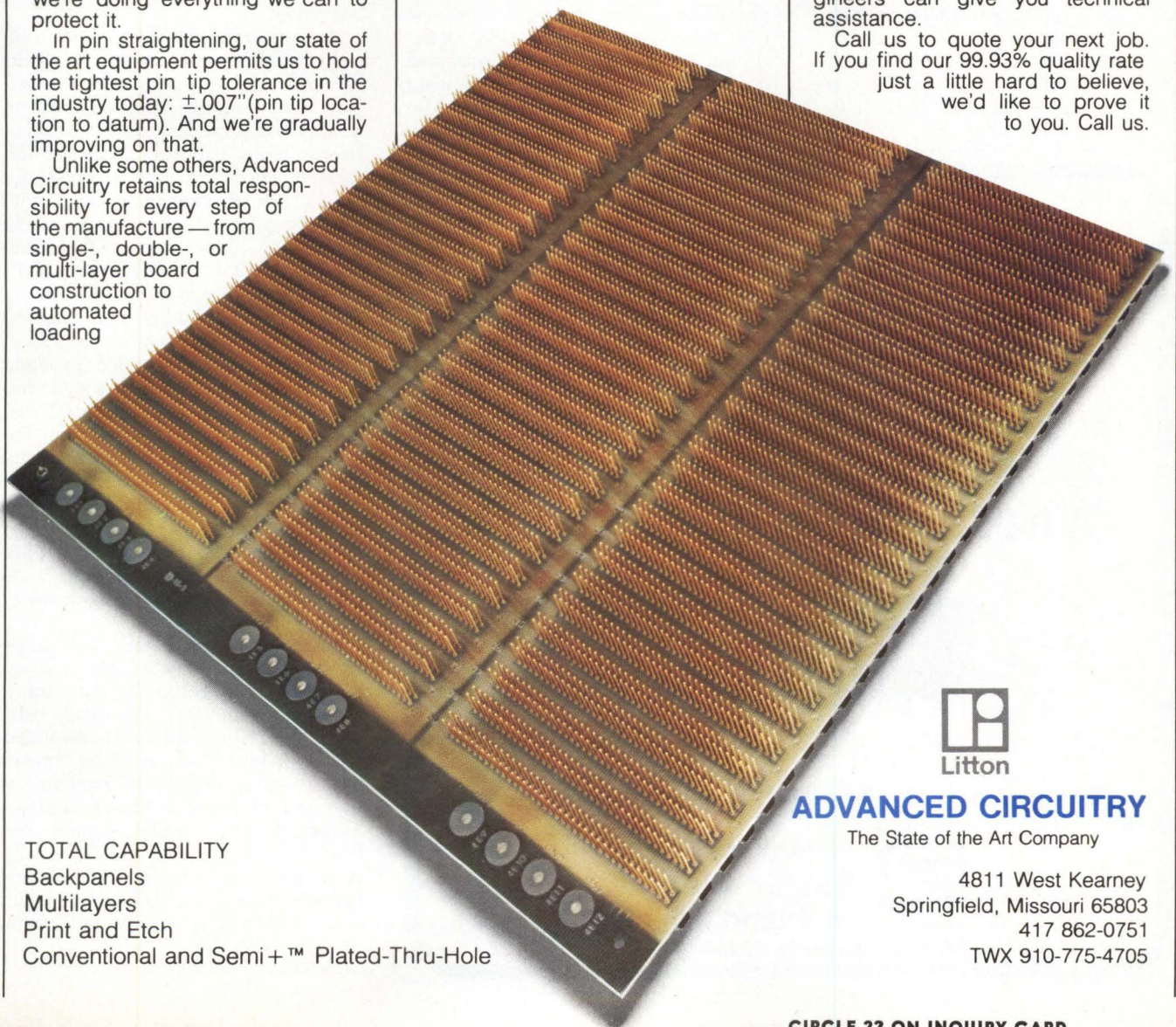
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CIRCLE 22 ON INQUIRY CARD

Selections of Add-On Cards Range From Memory To Math To Controllers

Additions to the MD Series™ of OEM microcomputer boards are all STD-Z80 BUS compatible (see *Computer Design*, April 79, p 148). Joint design of the bus by Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, and Pro-Log uses the Z80 CPU, producing a cost-effective OEM microcomputer system bus that supports the Mode 2 interrupt structure. The motherboard interconnect system concept handles any MDX card in any card slot. The 4.5 x 6.5" (11.4 x 16.5-cm) board size allows system partitioning by function and also makes system packaging easier. In general, the boards require only a single 5-V power supply. Most will also be offered in 4-MHz versions as well as 2 MHz.

MDX-SRAM cards are available in 4k, 8k, or 16k x 8 sizes. They use the company's MK4118 static RAMS

with selectable starting address on 4k boundaries. Another memory card, MDX-EPROM-4, contains eight sockets for maximum storage of 8k x 8 using 2758s (1k x 8), 16k x 8 using 2716s (2k x 8), and 32k x 8 using 2732s (4k x 8). Wait-state generate circuitry is included for 4-MHz operation. A universal memory card has eight sockets for use with MK4118 (1k x 8) and MK4802 (2k x 8) static RAMS, MK2758 (1k x 8) and MK2716 (2k x 8) EPROMS, and MK30000 (1k x 8) and MK34000 (2k x 8) ROMS. There are 16 memory configurations with 4k boundary addressing and selectable wait-state for each socket. It can run at 2.5 and 4 MHz.

An AMD 9511 math chip and an onboard MK3881 PIO chip perform the MDX-MATH card's data transfer and interrupt handling. Add, multiply, divide, subtract, trig and inverse trig functions, square roots, logarithms, exponentiation, and fixed and floating point operations are among the math functions performed. Also

contained onboard are a 2-MHz crystal controlled clock for asynchronous operation and wait-state insertion.

Containing a wd1771 controller chip and MK3883 DMA controller, MDX-FLP controls one to four drives with four software controlled select times. Drives may be 5 or 8" (13 or 20 cm), single- or dual-sided. However, all drives connected to the controller must be of the same type. It is compatible with IBM 3740 or other formats. Features include single-density operation, soft sector format with variable length sectors, automatic track seek with verification capability, diskette initialization/formatting capability, DMA or programmed data transfer, and interrupt driven or polled operation. It performs single-sector, multi-sector, or full-track data transfers. There are provisions for DMA daisy chain operation.

An operator interface with control switches and display readouts onboard, and a pushbutton for system reset comprise the system controller/diagnostic module. An onboard chip handles data transfer and interrupts. Space is available for up to 10k of EPROM or ROM, with memory address selectable on a 2k boundary within a given 16k boundary of the Z80 memory map. Software packages for the MDX-SC/D include monitor, handler, and diagnostic test for the MD series boards.

Offering 16 single-ended or eight differential input channels and two 8-bit analog output channels, the MDX-A/D analog I/O subsystem has I/O ranges from 0 to 10, ± 5 , and ± 10 V. It features input overvoltage protection to 35 V and a sample/hold amplifier for inputs. There is a single onboard precision reference circuit for the analog outputs, onboard dc-dc converter, and memory mapped I/O.

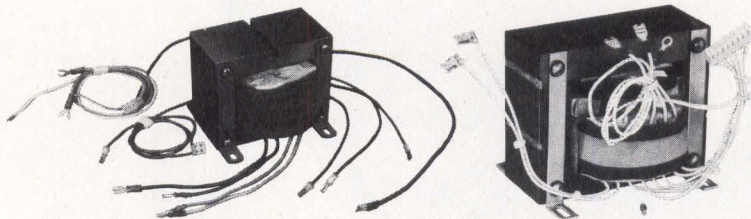
The final module—an A-D card—uses the MK5160 A-D chip and an onboard MK3881 PIO for data transfer and interrupt handling. MDX A/D8 has 16 multiplexed single-ended analog inputs and an 8-bit binary output; a sample/hold module is optional. Conversion time is 140 μ s. Three full-scale input ranges are from 0 to 1, 0 to 3, and 0 to 5 V. Accuracy is to $\pm \frac{1}{2}$ LSB with no adjustments required and no missing codes. Provisions allow additional channel expansion.

Circle 421 on Inquiry Card

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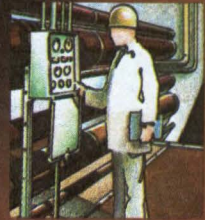
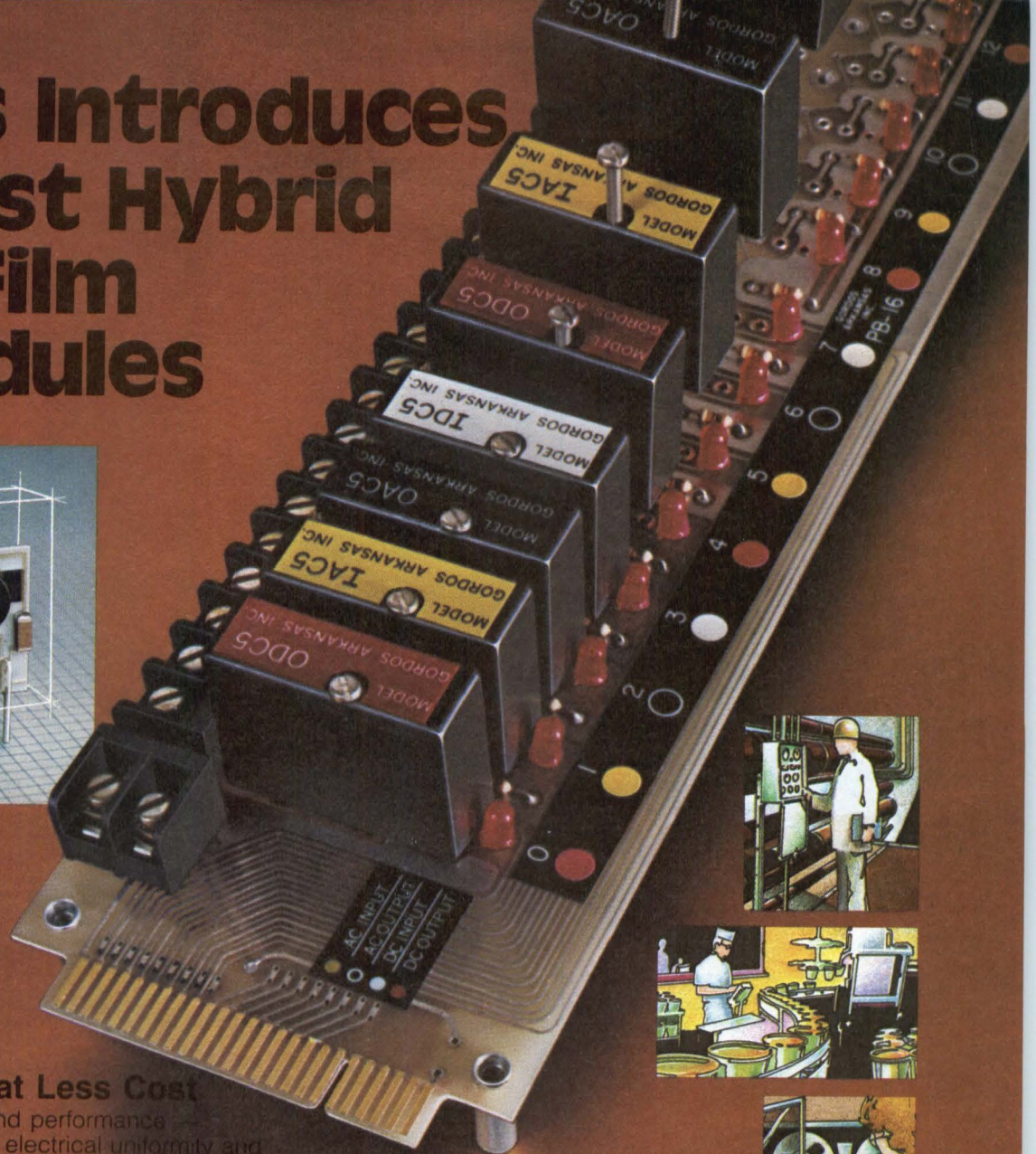
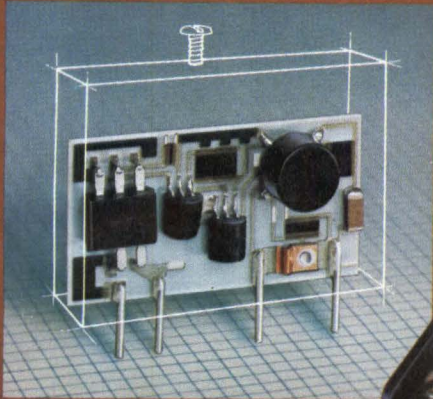
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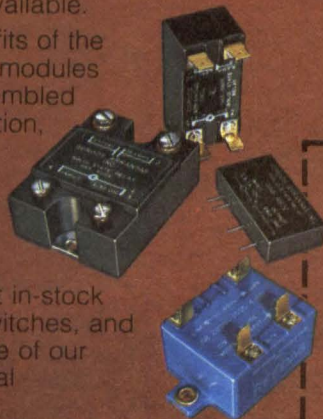
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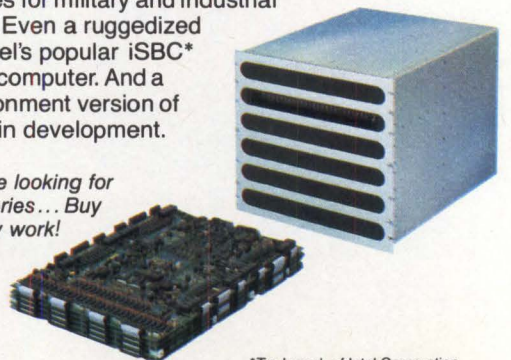
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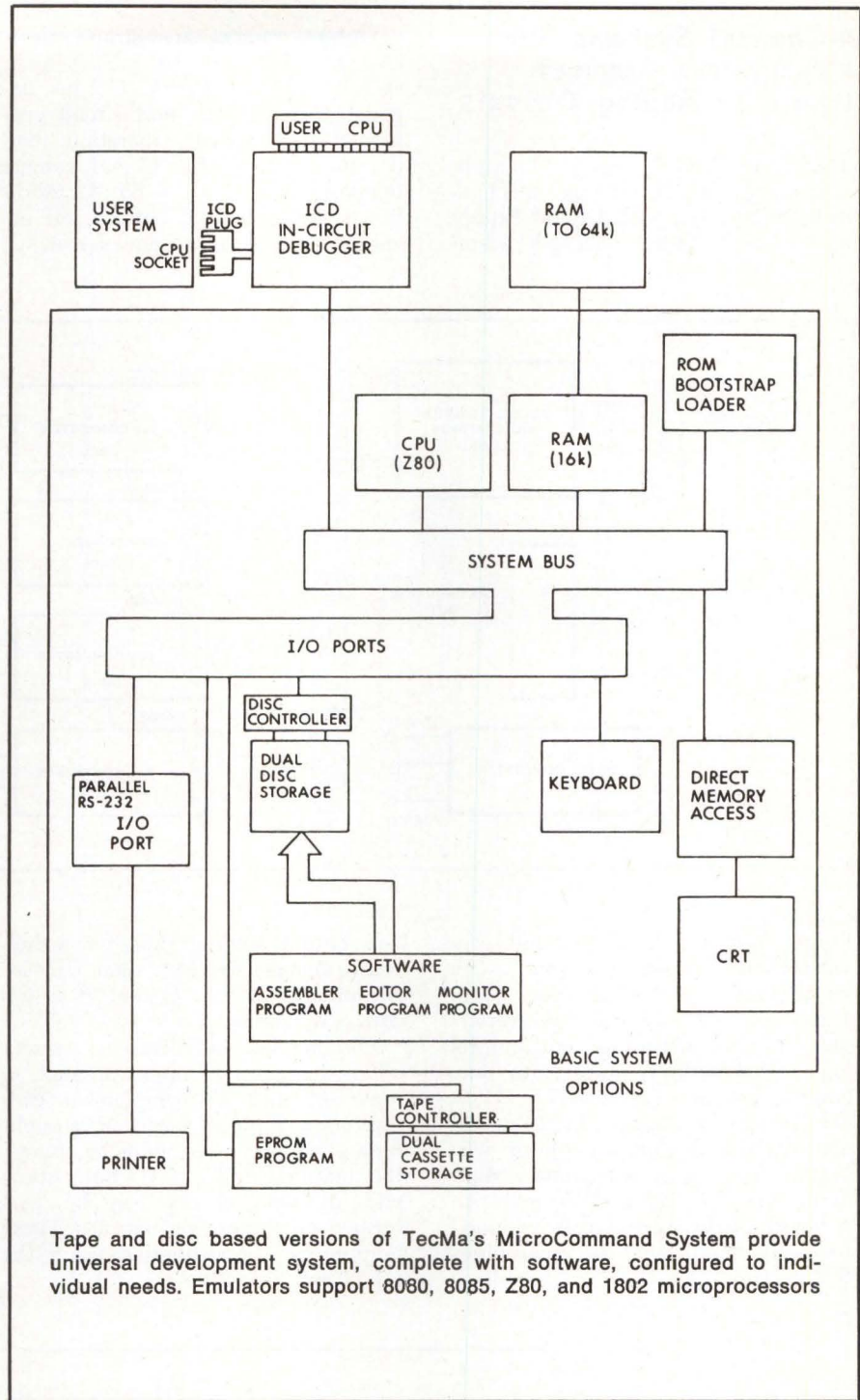
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Development System**

Supporting four realtime emulators—the 8080, 8085, Z80, and 1802 (with others under development), the ICC/MCS microprocessor development system is a universal low cost solution for users requiring additional in-circuit emulation stations. Designed with a dual-processor architecture, the system has inherent 16-bit capability. Expansion plans cover high level debug software, relocating macro assembler, and linking loader.

Both tape and disc based operating systems, complete with a free form CRT oriented editor, assembler, and monitor, are available. A Z80 based BASIC compiler is optional. The debugging monitor provides full register and selected memory region display, plus extended commands structure comprised of set/clear/display/execute on breakpoints, read/write object program, enable/disable user I/O, single step, enable/display high speed trace memory, and transfer memory contents. Also included are the DOS command set and text editor commands. Digital Research Corp's CP/M™ operating system allows the MCS to be used not only as a development system, but also as a business, scientific, and data processing system.

The in-circuit debugger, MCS ICD™, features a multiple architecture to support several microprocessors; therefore, the system CPU does not have to be converted from one object CPU to another. The debugger provides debug, test, display, and control capabilities.

MicroCommand System uses a Z80 processor for its internal logic; it provides an 8-level vector interrupt capability, as well as 16k to 64k of static RAM. The 512-byte load only ROM contains the bootstrap loader. A 40 x 24-char display CRT operates through DMA for fast display updates. Other components are a built-in ASCII keyboard, either dual 5" (13-cm) quad-density or dual 8" (20-cm) double-density floppy disc system, parallel and serial RS-232 output ports, EPROM programmer,



Tape and disc based versions of TecMa's MicroCommand System provide universal development system, complete with software, configured to individual needs. Emulators support 8080, 8085, Z80, and 1802 microprocessors

and optional dual cassette storage units.

TecMa, Inc, 2366 Walsh Ave, Santa Clara, CA 95051, has introduced three configurations. The dual cassette tape system, priced at \$4995, has the capability of disc based systems, but at slower speeds. Data transfer rate is 2000 bits/s. This is suited to uses requiring limited software de-

velopment, but much debug and emulation, such as testing and product checkout. The two disc based systems start at \$8450. Quad-density discs provide 315k bytes/diskette and a data transfer rate of 250k bits/s. The double-density discs offer 512k-byte diskettes with a data transfer rate of 500k bits/s.

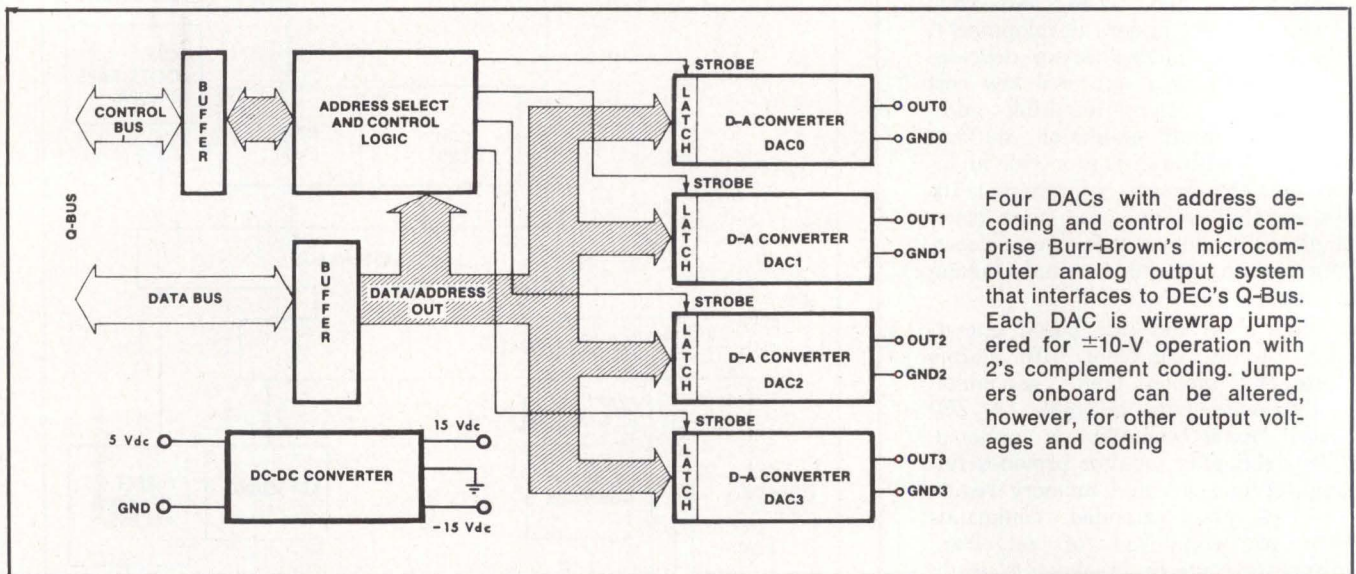
Circle 425 on Inquiry Card

4-Channel Systems For μ Computers Convert Inputs to Analog Outputs

The MP1104 analog output peripheral board, electrically and mechanically compatible with Digital Equipment Corp's Q-Bus, accepts 12-bit

Output ranges are strap selectable at ± 10 , 0 to 10, ± 5 , 0 to 5, and ± 2.5 V at 5 mA. Output impedance is 0.01Ω . Short circuit protection is included. Operating temperature is 0 to 70 °C and storage temperature is -25 to 85 °C. Additional specs are a tempco of accuracy drift of ± 30 ppm of FSR/°C,

Burr-Brown Research Corp, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734, has designed the system so that each D-A converter output may be filtered by adding an onboard feedback capacitor to each output op amp. This filtering may be used to smooth the output by limiting its bandwidth. The



Four DACs with address decoding and control logic comprise Burr-Brown's microcomputer analog output system that interfaces to DEC's Q-Bus. Each DAC is wirewrap jumpered for ± 10 -V operation with 2's complement coding. Jumpers onboard can be altered, however, for other output voltages and coding

inputs from the data bus and converts them to analog outputs with an accuracy of $\pm 0.025\%$ FSR. Consisting of four 12-bit D-A converters plus address decoding and control logic, the system plugs into any empty slot in the LSI-11, -11/2, -11/23, PDP-11/03, and -11/23 microcomputers and simply requires wiring of the analog connector. Minimum card spacing is 12.7 mm. An onboard dc-dc converter is included for operation from the computer's 5-Vdc supply.

and output settling time for a full-scale change of less than 10 μ s. Burning in at 70 °C for 48 h improves reliability.

On system initialization (reset) all D-A converter inputs are set to logic 0. With 2's complement coding on a bipolar range or straight binary coding on a unipolar range, the outputs go to 0 V. Both static and dynamic checks can be performed on the analog outputs. These outputs can be calibrated using the LSI-11 and its monitor.

feedback capacitor is in parallel with each DAC's internal feedback resistor.

The board is programmed as memory locations and any write instruction can be used. The DAC input occupies the 12 LSBs of a word. The address block is user selectable and can be placed anywhere in the upper 4k of memory. The base address of a board can be set to any 4-word boundary by jumpering (with wirewrap jumpers) its address selector. **Circle 426 on Inquiry Card**

Asynchronous Receiver/Transmitter Offers Two Full-Duplex Channels

Performing asynchronous serial data communications functions in microcomputer systems, the Z80 DART peripheral component has two independent full-duplex channels with separate modem controls. Quadruply buffered receiver data registers, doubly buffered transmitter, pro-

grammable interrupt vector, "status affects vector" mode for fast interrupt processing, and standard Z80 peripheral daisy chain interrupt structure for automatic vectoring without external logic are all featured.

The dual asynchronous receiver/transmitter in 40-pin plastic or ceramic DIP can be used as a serial to parallel, parallel to serial converter/controller. Data rates are 0 to 500k bits/s with a 2.5-MHz clock

or 0 to 800k bits/s with a 4.0-MHz clock. Break generation and detection include parity, overrun, and framing error detection.

Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, offers programmable options of 1, 1½, or 2 stop bits and odd, even, or no parity. Clocks may be 1, 16, 32, and 64 times the data rate in asynchronous modes. Temperature ranges are standard, extended, or Mil Spec.

Circle 427 on Inquiry Card

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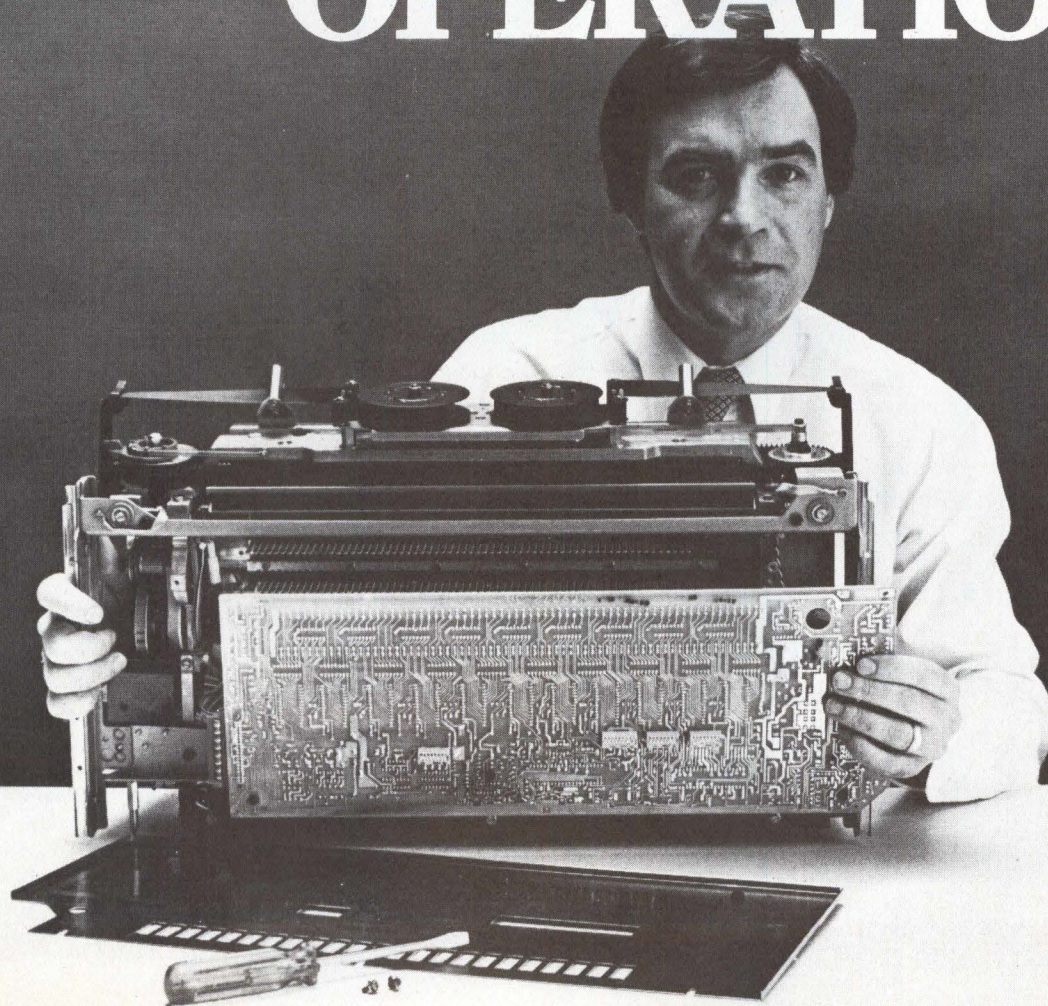
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SOFTWARE

**Program Recovers
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Data files can be salvaged from a diskette on which the directory has been partially or totally destroyed,

or recovered if mistakenly deleted using the automatic SALVAG ISIS-II disc utility program. The utility extensively analyzes any remnants of the directory. For any valid entries, the associated files are copied to a designated object diskette.

The utility next searches the source diskette sector by sector for data file link blocks. Those that are found are analyzed for validity, and at that point the associated data file is copied to the object diskette.

The user may optionally specify that files with an active directory entry be skipped. This is used when recovering files that were accidentally

deleted. If the specified source and object drives are the same drive, the utility pauses to allow diskette swapping. Thus, the program from Xener Corp, 6641 Backlick Rd, Springfield, VA 22150, can be used on systems with a single disc drive.

Circle 428 on Inquiry Card

**Dual In-Circuit Emulators
Debug Systems That Have
Multiple Microcomputers**

To alleviate the problems of multi-processor development which previously required two development systems, each with its own in-circuit emulator, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, has announced a software package that allows a single Intellec[®] Microcomputer Development System to control operations of two in-circuit emulators. The coordinated ICE[™] units debug most multiple microcomputer based processing and control systems.

This single-system Multi-ICE approach allows the user to enter commands for both emulators on one console and to record a coordinated set of trace information (up to 1022 microprocessor operating cycles), thus determining if related programs will mesh in realtime execution and providing an overview of multiprocessor operations. The seven types of microprocessors that are presently supported are 8085 CPUs, 8748, 8049, 8048, 8039, 8035, and 8021 single-chip microcomputers.

The resident software option for disc based Intellec model 800 and Series II model 220 and 230 development systems runs under the standard ISIS-II diskette operating system. As a software interface between the user and the ICE units, it executes a host process and two ICE processes. The host process translates commands from the console or diskette files into execution lists for itself and the two processes which then control the ICE units. Users control the ICE units individually or in combination. A dispatcher software subsystem provides overall coordination by determining the sequence in which tasks should be performed.

Software synchronization starts and stops two in-circuit emulators. For hardware synchronization, a sync line also allows either ICE unit to start or stop the other's emulation.

The interactive command language in plain English provides a common syntax for using the ICE units. It handles macro commands, symbolic debugging, assembler mnemonic displays, and other debugging techniques. □

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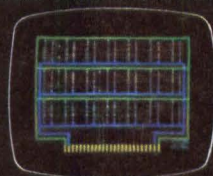
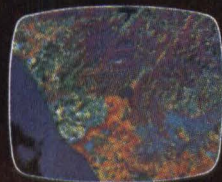
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CIRCLE 87 ON INQUIRY CARD

AROUND THE IC LOOP

VARIABLE MICROCYCLES IMPROVE SPEED OF BIPOLAR BIT SLICE PROCESSORS

Hank Brineen

National Semiconductor Corporation
Santa Clara, California

Advanced process and circuit technique improvements have enabled the fabrication of bit slice designs that promise dramatically increased system speeds over earlier low power Schottky bit slice implementations. Substantially increased throughputs (as much as 50 to 75%) are possible using various new approaches. Among these are "pipeline prediction" techniques in microprogram control, coupled with variable microcycle timing.

Critical Timing Paths

To identify potential areas for speed improvement using high speed 2900 type bit slice components, it is helpful to review the critical timing paths in a typical bipolar microprogrammed processor. Consider first the simple system organization shown in Fig 1. In this system, the address register is clocked at the beginning of the microcycle. When the microinstruction is valid at the read only memory (ROM) output, two basic paths must be considered.

One path consists of accessing data from the registers, propagating it through the arithmetic logic unit

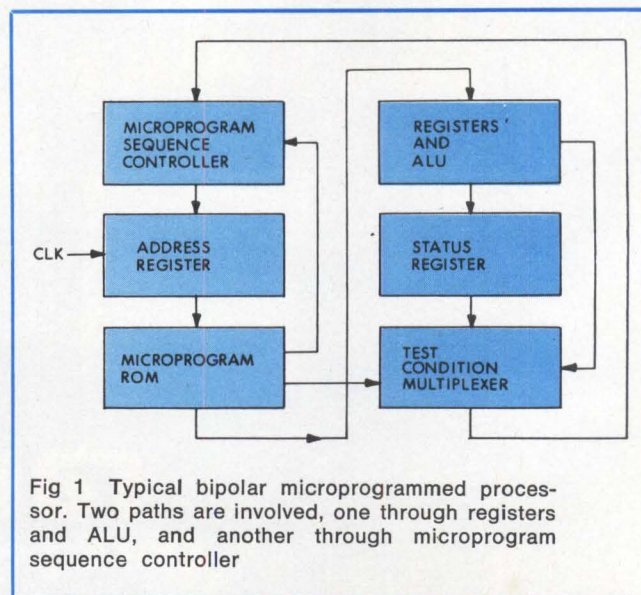
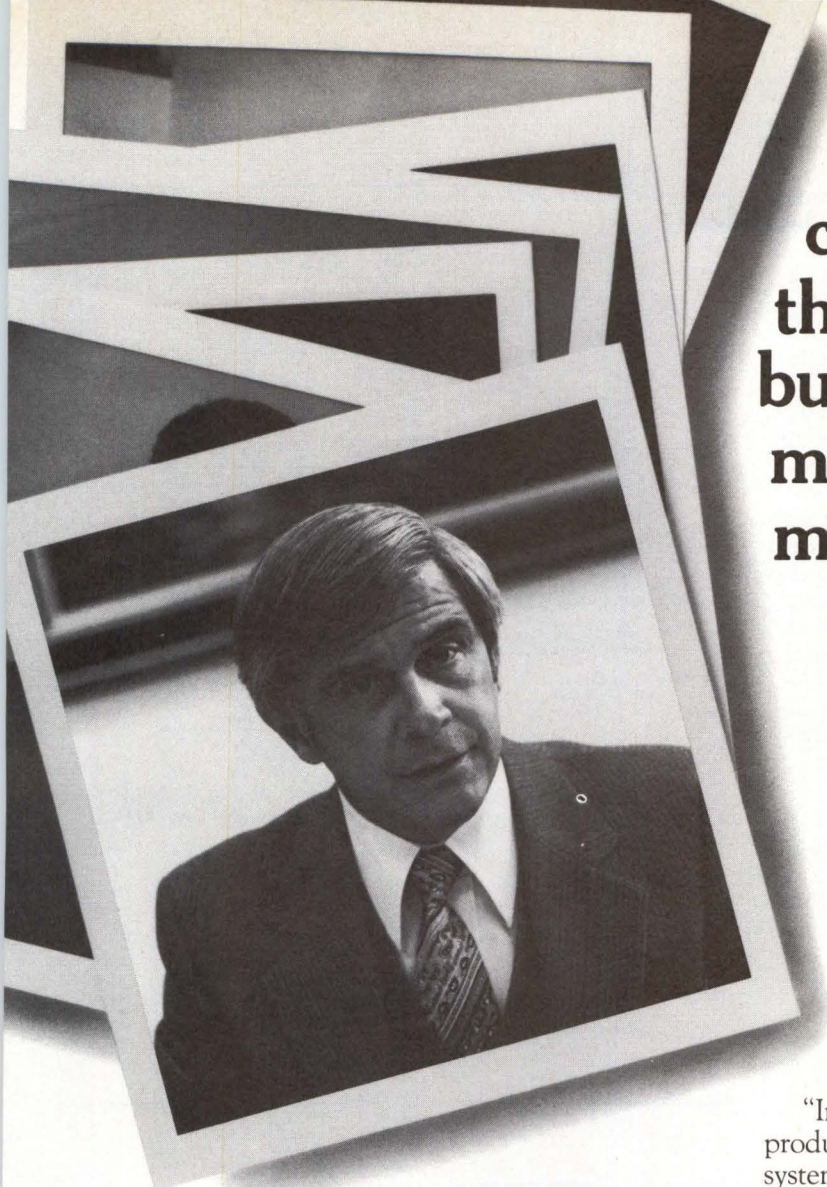


Fig 1 Typical bipolar microprogrammed processor. Two paths are involved, one through registers and ALU, and another through microprogram sequence controller



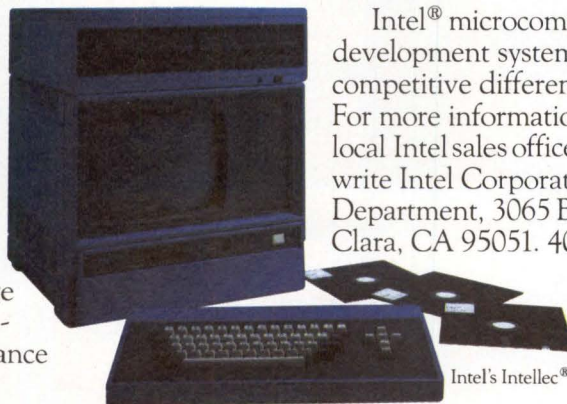
“The more competitive the video terminal business gets, the more Intel helps us maintain leadership.”

**Sal Nuzzo, President,
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Sal Nuzzo: “Intel’s introduction of the microcomputer revolutionized the computer terminal industry. We were first to use a microcomputer in a terminal — Intel’s 8008, years ago, and we’ve maintained a price/performance edge over the years by quickly taking advantage of Intel’s breakthroughs.

“This is a tough, competitive industry. Getting a product to market first can make all the difference. Any company that doesn’t move fast to take advantage of new technology will simply get left behind. So at Hazeltine, a key part of our strategy is to work closely with technology leaders — such as Intel. They introduced the microcomputer, and have continued to innovate with developments such as the 16-bit 8086 microcomputer. Taking advantage of their new products has enabled us to consistently give our customers higher performance and greater reliability.

“Intel makes it easy for us to apply their new products. An example is the Intellec® development system. Frankly, I don’t see how any company can design a product that uses microcomputers without a system such as the Intellec system. The Intellec system features such as in-circuit emulation (ICE) and PL/M programming language are essential time-savers. With our Intellec systems we can convert our existing programs for the 8080 microcomputer to Intel’s new 16-bit microcomputer, the 8086, quickly, and increase throughput ten times. That’s flexibility.”



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(ALU), and storing the result in a data register and status register. The other path involves the test condition multiplexer and sequence controller. The timing diagram (Fig 2) illustrates the relative timing for a system such as this. In a typical system design, the minimum microcycle period is limited by the delay path through the registers and ALU (shown as "ALU results may be clocked").

An organization frequently referred to as "pipelined" is illustrated in Fig 3. This nomenclature results from the fact that while one microinstruction is being executed, another is simultaneously being accessed. A microprogram register is added to the output of the ROM, and the clock causes the next microinstruction to appear at the output of this register. Output from the sequencer is allowed to access the microprogram ROM, fetching the next microinstruction while data are propagating through the registers and the ALU. This microinstruction will be ready to place in the microprogram register on the next clock. In this fashion, the access time of the ROM overlaps the execution of the microinstruction by the registers and the ALU.

Pipeline Prediction

As shown in the timing diagram (Fig 4), the sequencer output was valid early enough for the total access time of the ROM to be overlapped. To satisfy this condition, the test condition multiplexer inputs must be valid at an early point in the microcycle. This requirement is unfortunate, since it means that the test conditions based on the result of ALU operations in the current microcycle cannot be used.

An effective solution to this problem is the use of pipeline prediction; that is, the system is designed so

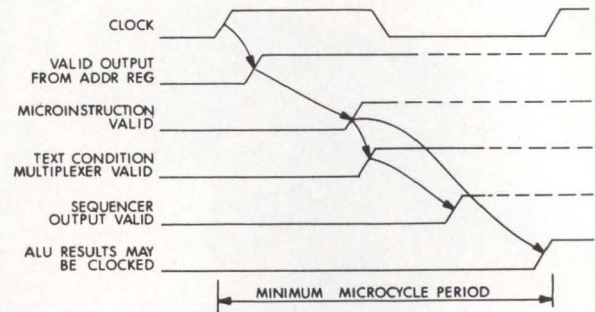


Fig 2 Timing diagram for processor of Fig 1. Minimum possible microcycle period is established by ALU path

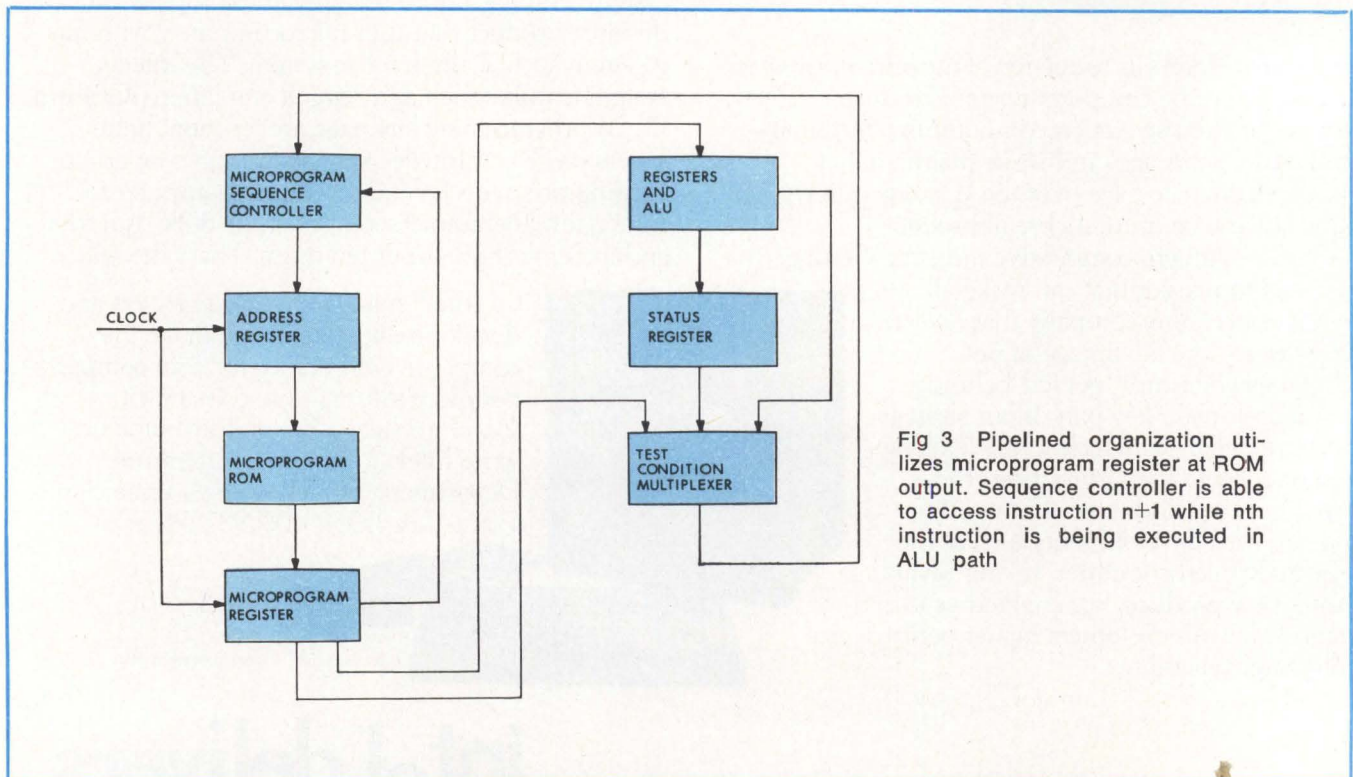


Fig 3 Pipelined organization utilizes microprogram register at ROM output. Sequence controller is able to access instruction $n+1$ while n th instruction is being executed in ALU path



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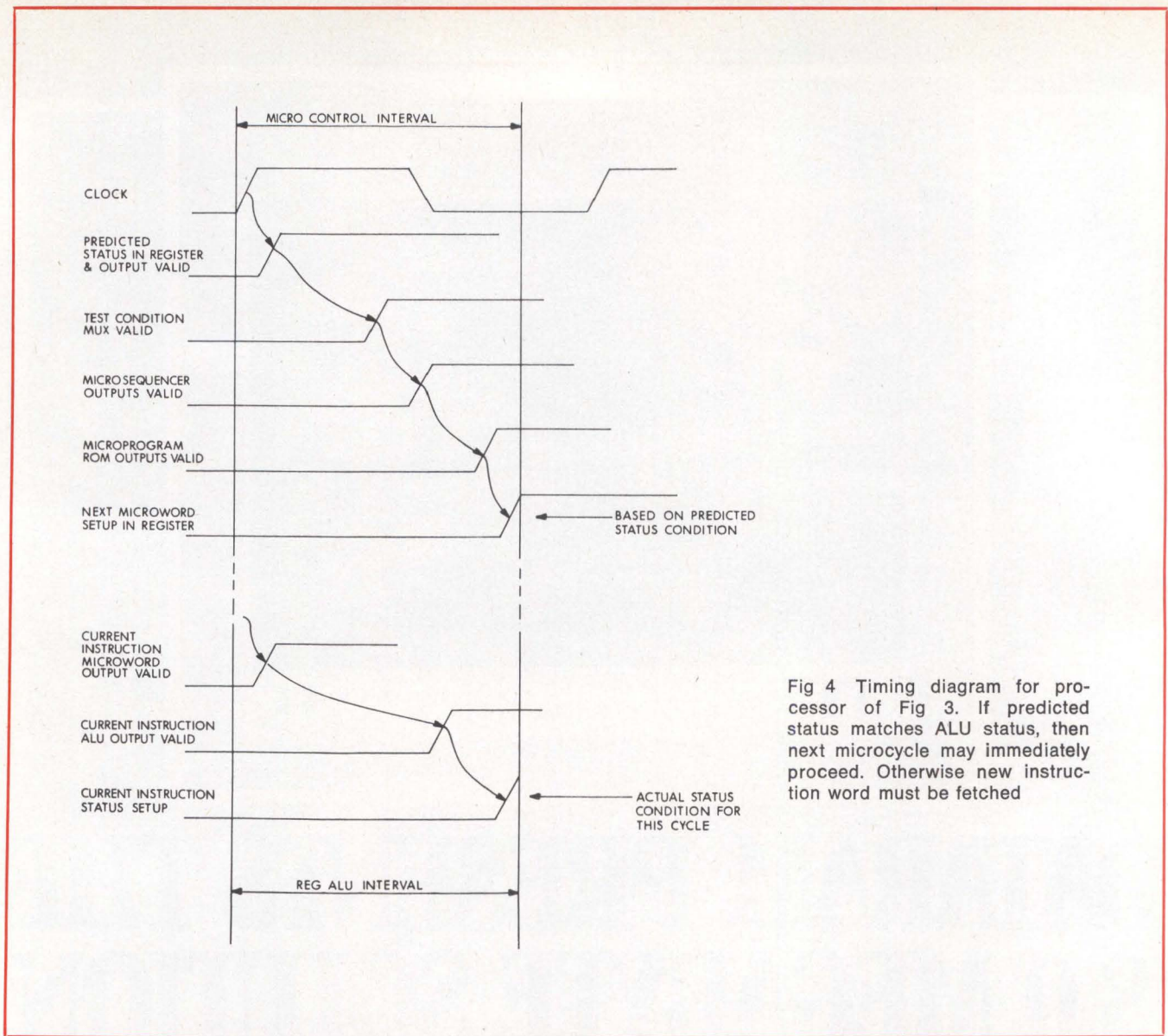


Fig 4 Timing diagram for processor of Fig 3. If predicted status matches ALU status, then next microcycle may immediately proceed. Otherwise new instruction word must be fetched

that the sequencer logic is conditioned on the basis of a predicted value for the test condition multiplexer output, and the ROM is accessed on this assumption. After the ALU result is stable and has propagated through the test condition multiplexer, the predicted value of the multiplexer output is compared with the actual value of its output. If the predicted value is correct, the next microinstruction in sequence (that is, the one being accessed) is executed. On the other hand, if the predicted value differs from the actual value, the conditioning of the sequencer logic is modified correspondingly, and the time duration of the microcycle is extended to allow time for the modification to propagate through the sequence controller logic and access the ROM.

Since the microprogrammer can frequently predict the results of test conditions with much better than 50% success frequency, a relatively small fraction of the microcycles must be extended. For example, in a microprogrammed multiply or divide algorithm, a loop counter must be tested on each pass through the loop. In a 16-bit machine, the test would typically be performed 16 times, but the result could be accurately predicted 15/16ths of the time.

Variable Microcycle Periods

As discussed previously, the delay through the registers and ALU is typically the path that limits system performance. The magnitude of this delay can vary considerably depending on which microoperation is being performed. Table 1 lists a variety of operations together with the microcycle period requirements for a pipelined system. Note that the longest operation requires about 75% more execution time than the shortest. The most straightforward design approach is simply to calculate the worst case time period and design the clock generator circuit to provide that time for all operations. However, it is evident that a speed improvement could be obtained if the clock generator were programmed to modify the microcycle time in accordance with the requirements of the operation to be performed.

System Performance Comparisons

It is helpful to look at numerical values obtained from a design study of five system organizations utilizing bit slice components such as the IDM2900 family from National Semiconductor. By performing a similar analysis

using specifications of available components, the designer can make realistic decisions of cost versus performance when choosing a system organization for a new design.

System 1 is a nonpipelined organization and test conditions are based on results of operations performed on the previous microcycle. A fixed microcycle period of 225 ns is used, necessitated by the multiply instruction (Fig 1).

Pipelined system organization (Fig 3) defines System 2. Test conditions are based upon results of previous microcycles and a fixed microcycle time of 172 ns is used. The pipelined organization allows the microcycle period to be reduced to 48 ns less than the cycle time for System 1.

System 3 is the same as System 2 except that test conditions based on results of the current microcycle are used and the technique of predicting test condition results is utilized. The microcycle period is fixed at 172 ns; the time necessary for the result of the current operation to propagate through the test condition multiplexer and determine whether an extended cycle is needed. An extended cycle adds 86 ns, one-half microcycle, to the normal microcycle period.

The configuration of System 4 is the same as that of System 2 except that a variable microcycle period is used. Test conditions are based on the results from the current microcycle; however, no prediction of test conditions with an extended cycle for incorrect prediction is performed. Instead, those microinstructions which require more time to allow for propagation of the result through the test condition multiplexer and sequence controller are simply programmed to be of longer duration. Microcycle periods of either 103, 137, 172, or 206 ns could be used depending on the needs of each microinstruction. Although this approach may require more microcode locations, it does offer even greater flexibility in tailoring the microcycle period to the needs of the operation being performed.

System 5 combines the techniques used in Systems 3 and 4. Variable length microcycles can be used. The

TABLE 1
Pipelined Microcycle Period Requirements

<u>Operation Performed</u>	<u>Microcycle Time (ns)</u>
Logic operation, status register not modified, no test of result	98
Arithmetic operation; status register not modified; no test of result	133
Add and shift; status register not modified; no test of result	172
Multiply cycle; Q _n used to determine I _n of 2901	172
Arithmetic operation; status register modified; no test of result	169
Arithmetic operation; status register not modified; result used as test condition (no extend caused by incorrect prediction)	165

technique of predicting test condition results is used, and, when the cycle is extended due to an incorrect prediction, an additional 86 ns is added.

Table 2 shows instructions typically used in a mini-computer that is configured in one of the previous system organizations. Execution times specified in Table 2 for each instruction type are derived by using the execution time of System 1 as a baseline reference.

TABLE 2
Bit Slice Instruction Execution Times (ns)
As Function of System Organization

<u>System Organization</u>	<u>Instruction Type</u>				<u>Loop for MOVE</u>
	<u>LD, JMP, ST</u>	<u>JSR</u>	<u>BOC</u>	<u>ADD</u>	
System 1: Nonpipelined; test condition from previous microcycle	920	1610	920 or 1150	920	920N
System 2: Pipelined; no prediction; test condition from previous microcycle	688	1204	688 or 860	688	688N
System 3: Pipelined with prediction; test condition from current microcycle	688	1204	599 or 731	688	688N
System 4: Pipelined; no prediction; variable length microcycle; test condition from current microcycle	480	960	482 or 619	549	617
System 5: Pipelined with prediction and variable microcycle length	480	892	412 or 549	549	549N

Note: The reason JSR and Loop for MOVE don't improve with System 3 is that a way was found to write a code without an extra cycle

TABLE 3
Relative Instruction Execution Rate
With Various System Organizations

System Organization	Instruction Type				Loop for MOVE
	LD, JMP, ST	JSR	BOC	ADD	
System 1: Nonpipelined, test condition from previous micro-cycle	1.0	1.0	1.0 or 1.0	1.0	1.0
System 2: Pipelined, no prediction, test condition from previous microcycle	1.34	1.34	1.34 or 1.34	1.34	1.34
System 3: Pipelined with prediction, test condition from current microcycle	1.34	1.34	1.64 or 1.57	1.34	1.34
System 4: Pipelined, no prediction, variable length microcycle, test condition from current micro-cycle	1.91	1.67	1.91 or 1.85	1.67	1.49
System 5: Pipelined with prediction and variable microcycle length	1.91	1.80	2.23 or 2.09	1.67	1.67

The relative execution speed for each of the five systems can best be appreciated by examining the data in Table 3, a transformed version of Table 2 that shows relative instruction execution rate with various system organizations normalized to System 1.

Variable Microcycle Potential

Popular as it has been with many system designers using bit slice architecture, the usefulness of the

variable microcycle approach may be shortlived, due to the increasing speed of bit slice components. As the microcycle interval becomes shorter and shorter—from 100 ns down to 65 or 70 ns for a simple add, and from 125 ns down to 75 or 80 ns for an add and shift—the advantages of the variable microcycle approach are severely diminished. There are alternatives available, however, and these are to be discussed in a later column.

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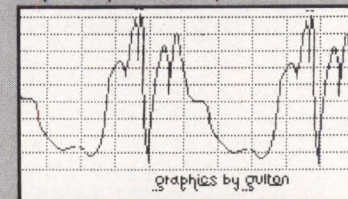


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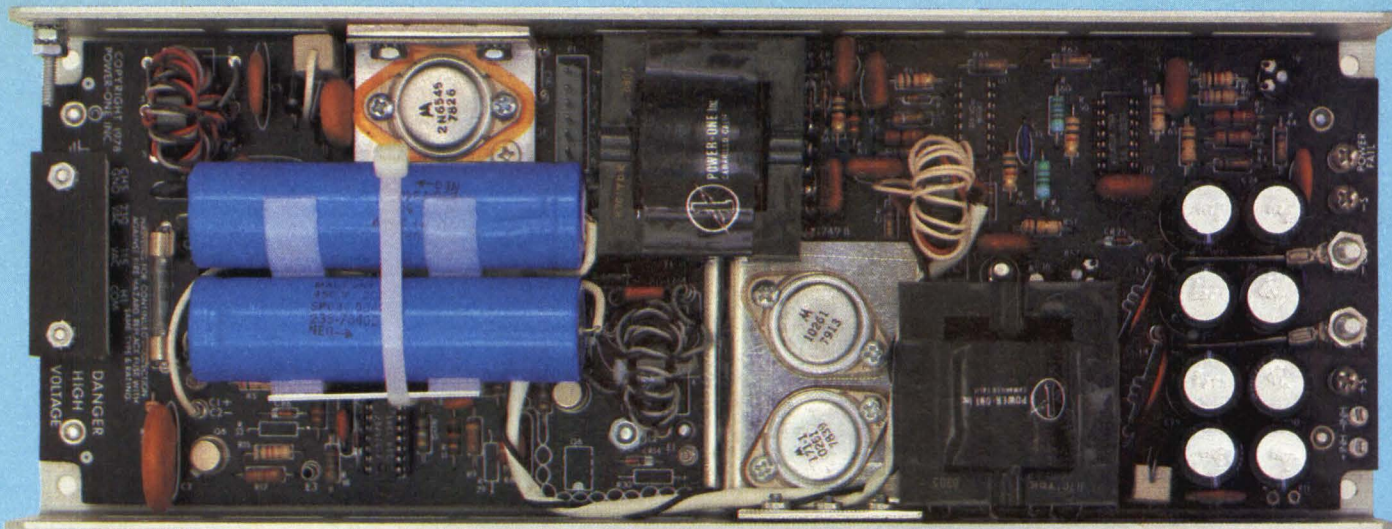
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a switching power supply as dependable as a linear.

When Power-One decided to build a switching power supply, we issued one simple mandate: it must be as dependable as our linears. Well, we did it. A direct drive 5-volt 40-amp switching power supply that's smaller, lighter, simpler, more reliable and less expensive than the rest.

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By using a self-driven switching stage, we've done away with the starting bias, drive and the current sensing transformers. A big reduction in weight plus lower cost, more precise drive control and fewer input to output noise paths. To assure maximum protection against AC line transients and fluctuations, a unique "volt-second" regulation circuit is employed.

Safeguard Design

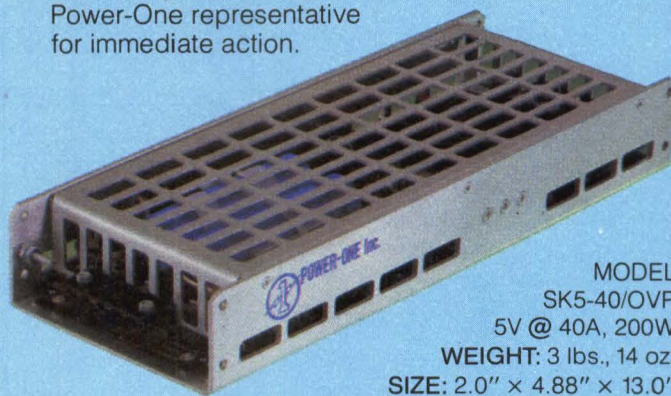
We've built in a number of safeguards. Like our digital feedback system which yields exceptional loop stability while maintaining positive control of critical switching parameters. And a unique anti-saturation circuit to protect the power transistors from the dire effects of transformer saturation. Plus, by putting inputs at one end of the supply and outputs at the other, we've eliminated inter-circuit cross talk. And speaking

of inputs, our dual range design permits either 115 or 230 VAC operation without changing jumpers.

The Bottom Line

Switching frequency: 28KHz — stable as a rock. Size: a mere 4.88 x 13 x 2 inches — more watts to the inch and more power for the buck. The price: \$250 for single units.

Send for complete details. Or better yet, contact your local Power-One representative for immediate action.



MODEL
SK5-40/OVP,
5V @ 40A, 200W
WEIGHT: 3 lbs., 14 oz.
SIZE: 2.0" x 4.88" x 13.0"
PRICE: \$250 Single Quantity

 **Power-One** INC.
D.C. POWER SUPPLIES

Power One Drive • Camarillo, California 93010 • (805) 484-2806 • TWX 910-336-1297

CIRCLE 91 ON INQUIRY CARD

Signal Processing Chip Operates As Microprocessor Peripheral

Customer developed arithmetic routines are available from a high speed CMOS signal processing peripheral (SPP) when it is interfaced to a microprocessor. The S2811 from American Microsystems Inc, 3800 Homestead Rd, Santa Clara, CA 95051, is a special purpose processor with onchip ROM, RAM, multiplier, adder/subtractor, accumulator, i/o, and 20-MHz crystal oscillator circuit, organized in a pipelined structure. Operating on 12-bit numbers, it can provide a multiply, add, and store sequence in 300 ns.

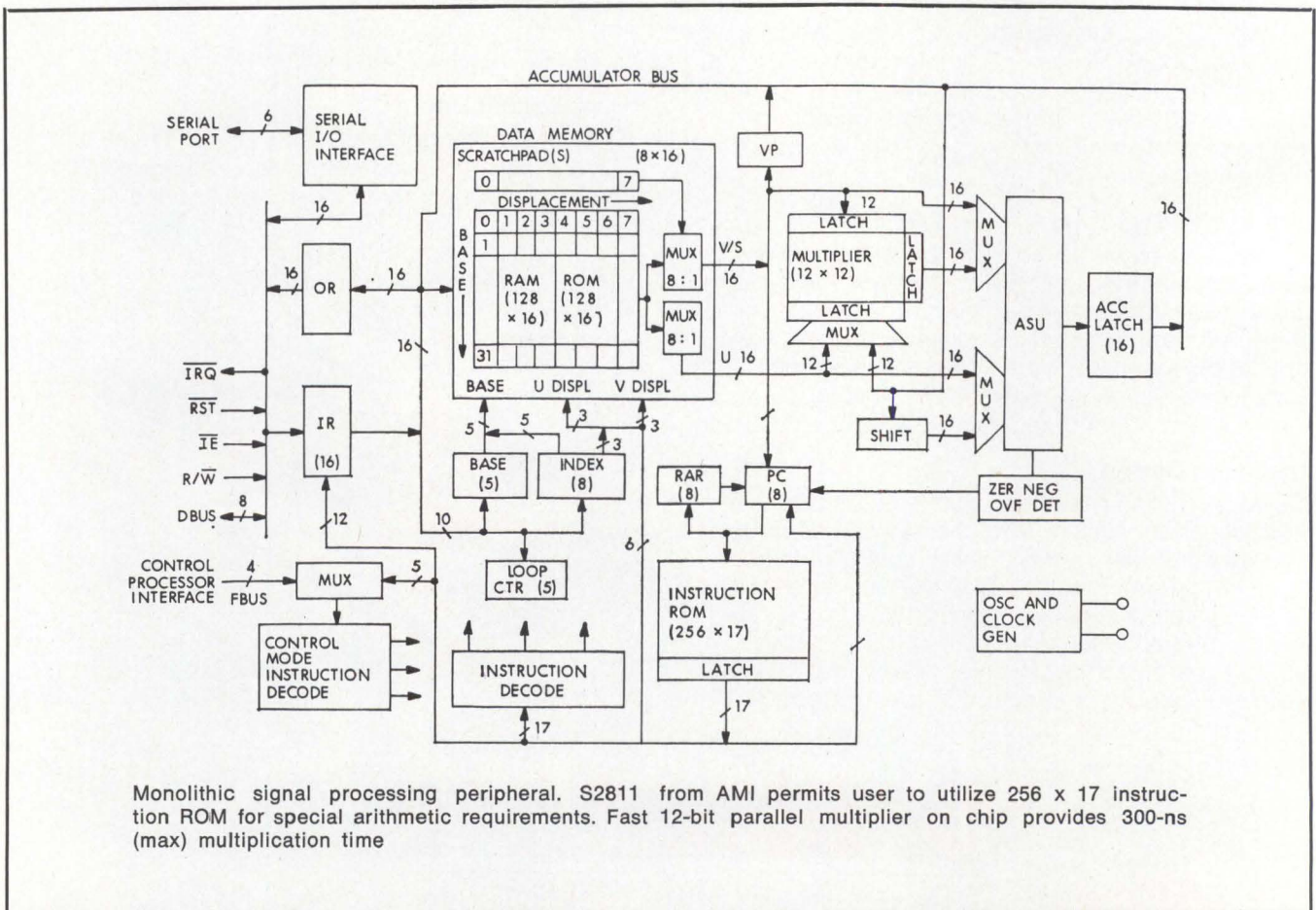
The microprocessor can call up an arithmetic routine by giving a command to the SPP. A powerful instruction set (including branching and one level of subroutine) permits

the SPP to function independently once the initial command is given. This leaves the microprocessor free to perform other operations until it is interrupted by the peripheral upon completion of the task. The high speed number crunching capability of the SPP gives a standard microprocessor system the necessary computational speed to implement complex digital algorithms in real time. (For a comparison between this and other approaches to arithmetic processing, see "External Arithmetic Processors" by S. Smith, *Computer Design*, Dec 1978, pp 144-149).

User programs are stored in a 256 x 17 read only memory. Of the 256 instruction locations in this ROM, 250 are accessible to the user, the re-

maining 6 locations being reserved for chip testing. The 17-bit wide instruction word facilitates multiple operations per instruction. One example of the programmable capability of the SPP is its use as a second order digital filter section. A second example is that of a sincos subroutine that computes the values of $\sin \omega$ and $\cos \omega$ using an approximation formula, useful in applications that require carrier generation. In general, the SPP is programmable for digital processing of signals in voice-grade communications systems and other applications with signals in the audio frequency range.

A high speed serial port provides direct interface to an analog to digital converter. In many applications,



WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.



Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional

rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development

capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation.

The Orion-60/S4.

For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

*CP/M is a trademark of Digital Research.

CIRCLE 92 ON INQUIRY CARD

realtime processing of sampled analog data can be performed within the SPP without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the peripheral processing.

An onchip data memory is divided into RAM and ROM sections, each organized as 128 x 16. There is a single input port to the total memory and two output ports, allowing simultaneous readout of two words.

Separate input and output registers exchange data with the SPP data ports. Serial interface logic converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

Four address lines define several control modes and operations to facilitate the interface between the SPP and a control processor. The SPP is a memory mapped peripheral, occupying 16 locations of microprocessor memory space. Providing the proper address will activate the corresponding control mode. Control modes include such operations as resets, specifying of MSB or LSB, the conversion between 2's complement and sign-magnitude serial data, and the enabling of specified ports. The control modes and the LIBL command (load input register contents to base register and loop counter) enable realtime modification of programs. This permits a single SPP program to be used in several different applications. For example, the peripheral might be programmed as a universal digital filter, with cutoff frequency, filter order, and data source (either serial or parallel port) selected at execution time by the control microprocessor.

A realtime in-circuit emulator for this device, the RTDS2811, is under development. This is a fully compatible hardware emulator with software assembler/disassembler and editor for rapid program development and debugging.

Absolute maximum ratings for the signal processing peripheral include an upper limit of 7 Vdc for supply voltage, with voltage at any pin limited to a range from $V_{SS} - 0.3$ V to $V_{CC} + 0.3$ V. Temperature must remain between 0 and 70 °C during operation and between -55 and 125 °C in storage. The device is provided in a 28-pin dual-inline package.

Circle 350 on Inquiry Card

4k Static RAM Features Low Supply Current

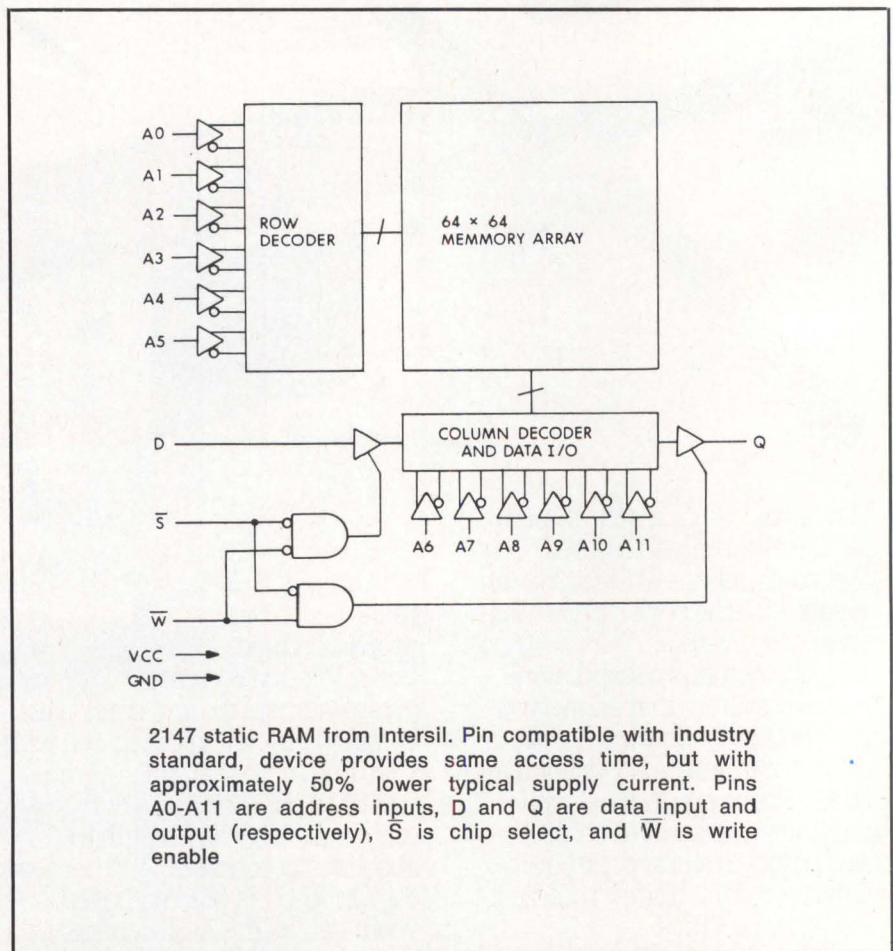
A 4096-bit static random access memory, the 2147, pin and function compatible with the industry standard 2147 RAM, is being sampled by Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014. Typical operating supply current is 50 mA, or (for the faster -3 suffix version) 60 mA, an approximate 50% reduction relative to the standard part. Maximum ratings are, respectively, 160 and 180 mA. Access time is 70 ns (55 ns for the -3 version). Both models are being manufactured by an advanced 3.5- μ fine-geometry NMOS process.

These RAMs feature a fully automatic power-down mode, controlled by chip select (\bar{S}). Less than one cycle time after \bar{S} goes high, supply current drops from 160 mA to a standby level of 20 mA, or from 180 to 30

mA for the -3 model. The completely static device requires no clock, and inputs and 3-state outputs are TTL compatible, allowing for direct interfacing with common bus system structures.

This memory is organized as 4096 words by 1 bit and operates off a single 5-V power supply with a $\pm 5\%$ supply fluctuation tolerance. Data are read out nondestructively with the same polarity as the input data. The device is available in an 18-pin ceramic dual-inline package.

Absolute maximum ratings require that V_{IN} , voltage on any pin relative to ground, lies between -0.5 and 7 V, and that I_{OS} , short circuit output current, does not exceed 20 mA. Ambient temperature under bias must remain between -10 and 85 °C and storage temperature between -65 and 150 °C. Power dissipation must not exceed 1 W.



2147 static RAM from Intersil. Pin compatible with industry standard, device provides same access time, but with approximately 50% lower typical supply current. Pins A0-A11 are address inputs, D and Q are data input and output (respectively), \bar{S} is chip select, and \bar{W} is write enable

Circle 351 on Inquiry Card

Another new terminal from Hazeltine!

Hazeltine 1552



Announcing a significant enhancement to the renowned Hazeltine 1500 Series. With an inventory of Standard Features so impressive, this new video terminal commands your attention for conversational applications.

Standard Features

- All 128 ASCII Codes
- 95 Displayable Characters including Lower Case plus 31 graphics symbols
- ✓ High Resolution Characters using a 7 x 10 dot matrix
- ANSI Standard Typewriter layout
- Cursor Control Keys
- Function Keys
- Alternate Key Pad Mode
- Separate Integral Numeric Pad
- Hold Screen Mode
- Graphics Mode
- ✓ Dual Intensity
- Cursor Addressing and Sensing
- EIA and 20 MA Interface
- Baud Rates up to 9600 Baud
- ✓ Auxiliary EIA Output
- Remote Editing Commands
- ✓ Standard or Reverse Video
- ✓ Programmable Key Switch Audio Feedback
- VT-52 Compatibility
- ✓ Clear Screen
- ✓ Clear Foreground
- Clear to End of Line
- Clear to End of Screen (background spaces)
- Audible Alarm
- Backspace
- ✓ Keyboard Lock
- ✓ Keyboard Unlock
- ✓ Insert Line
- ✓ Delete Line
- ✓ Field Tab
- Column Tab

- Enter/Exit Hold Screen Mode
- Enter/Exit Alternate Key Pad Mode
- Enter/Exit Graphics Mode
- Send Terminal ID
- ✓ Set/Reset Audio Key Switch Feedback
- Cursor Address (XY)
- Incremental Cursor Control
- ✓ Read Cursor Address
- Home Cursor

We interrupt this advertisement to bring you this special message...

VT-52 Users, here's the terminal you've been looking for. The Hazeltine 1552.

Besides fitting directly into your DEC system, it costs you much less. And it's available for immediate delivery! But that's just for starters. Of even greater significance are these two important bonuses:

"QUALITY" BONUS... the kind of Quality you've come to expect with every terminal bearing the famous Hazeltine name, backed by Hazeltine's exceptional Warranty Program. Ask for details!

"FEATURES" BONUS... with the impressive roster of Standard Features listed on this page, the Hazeltine 1552 more than matches the VT-52. Plus! All Features checked (✓), while standard on the Hazeltine 1552, are not available on the VT-52!

We now return you to the ad in progress.

It's a Hazeltine naturally!



Hazeltine Corporation, Computer Terminal Equipment, Greenlawn, New York 11740, (516) 549-8800 Telex 96-1435

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μProcessor Compatible Data Acquisition System Implemented On One Chip

Incorporating all the essential elements of a microprocessor data acquisition system, a monolithic CMOS integrated circuit includes an 8-bit analog to digital converter, an 8-channel multiplexer, and microprocessor compatible control logic. The device requires no offset or scale adjust and features a single 5-V supply and 15-mW power consumption.

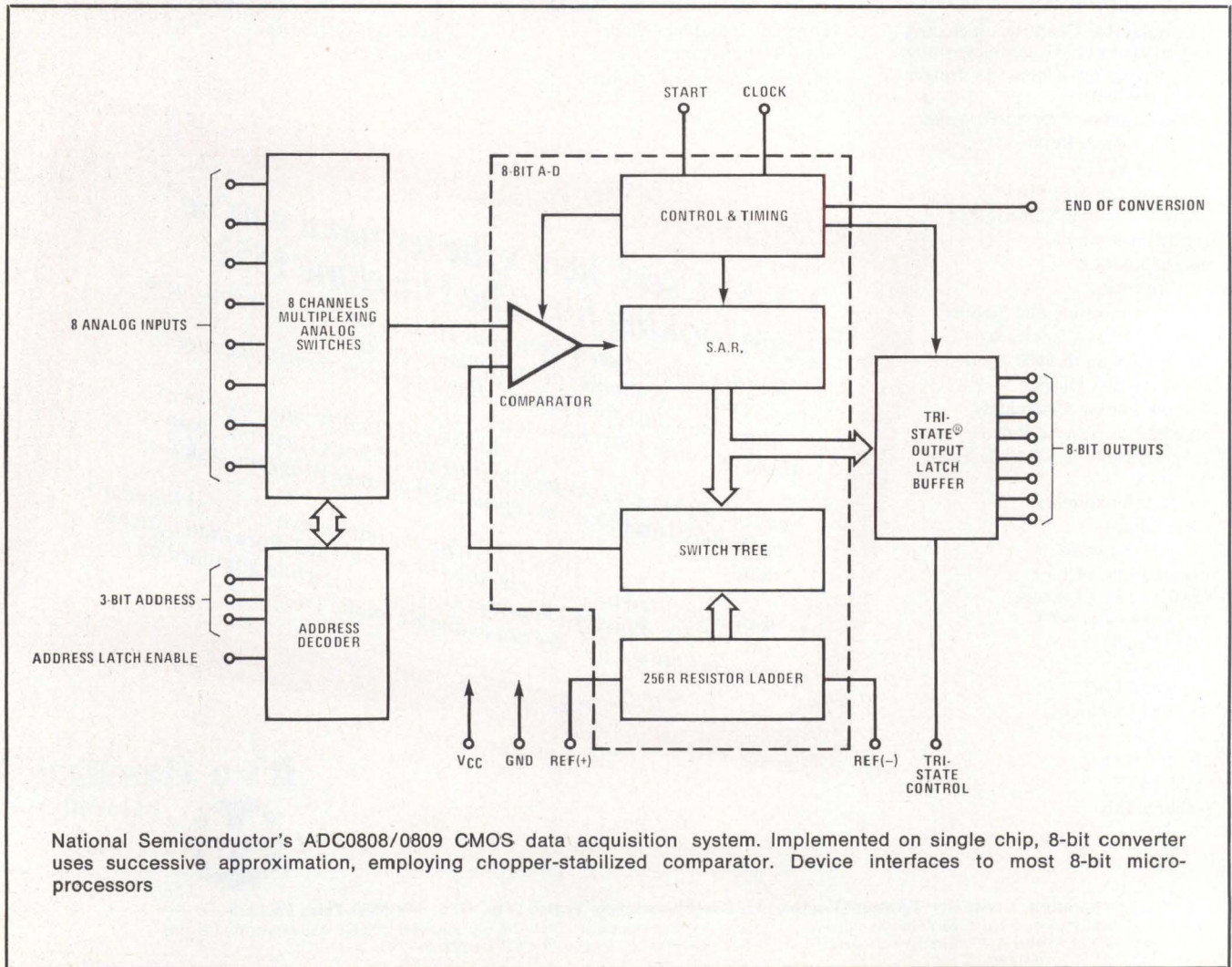
A successive approximation technique is used, employing a high impedance chopper-stabilized comparator, a 256-resistor voltage divider with analog switch tree, and

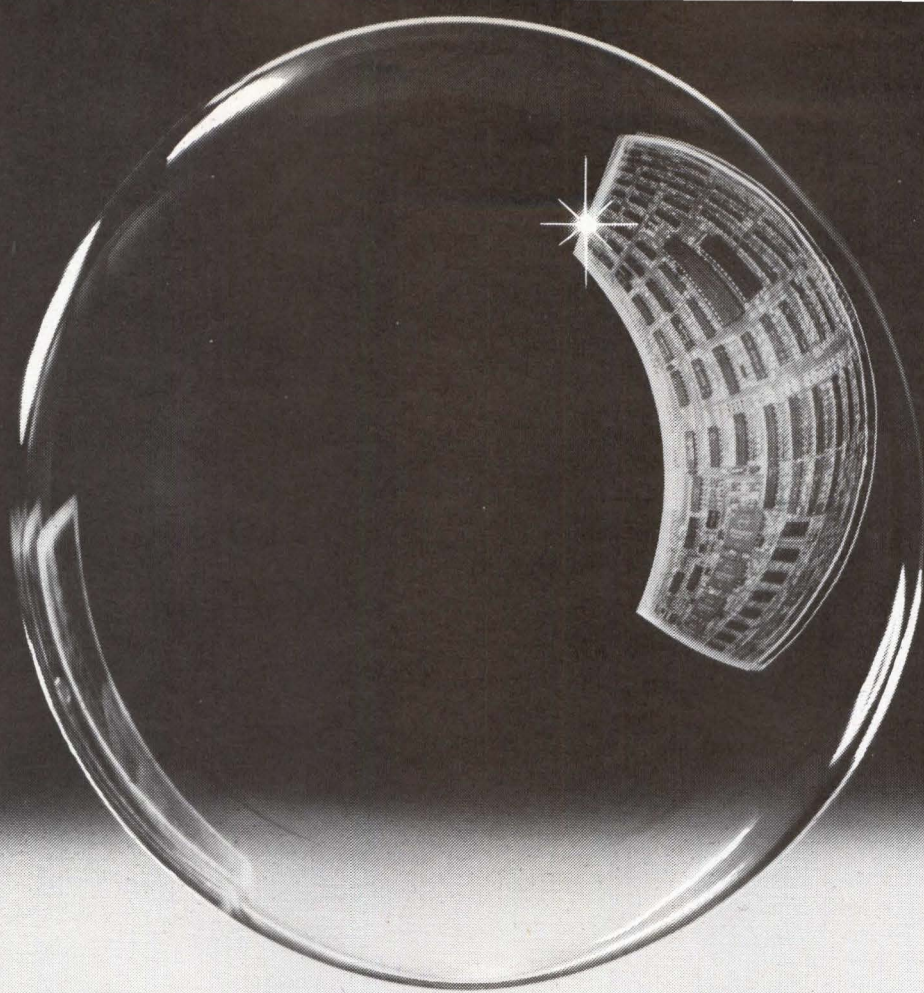
a successive approximation register. The chopper-stabilized comparator is said to provide the most effective and accurate conversion possible, making the entire device extremely immune to temperature, long-term drift, and input offset errors. This is done by transforming the dc input signal into an ac signal before amplification and then restoring the dc level after amplification. The 256-resistor ladder network approach was chosen over the more conventional R/2R ladder technique because of its inherent monotonicity, which guarantees no missing codes.

Produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, the system is available in two versions. The ADC 0808, supplied in a 28-pin cavity

dual-inline package, features a linearity error of $\pm\frac{1}{4}$ LSB (typ) and $\pm\frac{1}{2}$ LSB (max), a total unadjusted error of $\pm\frac{1}{4}$ LSB and an absolute accuracy of $\pm\frac{1}{4}$ LSB (typ) and $\pm\frac{1}{2}$ LSB (max). Supplied in a molded DIP configuration, the 28-pin ADC0809 has a linearity error of $\pm\frac{1}{2}$ LSB (typ) and ± 1 LSB (max), a total unadjusted error of $\pm\frac{1}{2}$ LSB, and an absolute accuracy of ± 1 LSB (typ) and $\pm\frac{1}{2}$ LSB (max).

Features common to both versions include the ability to perform a conversion in 100 μ s, 8-bit resolution, zero error and full-scale error of $\pm\frac{1}{4}$ LSB, and quantization error of $\pm\frac{1}{2}$ LSB. The 8-channel multiplexer can directly access any of eight single-ended analog signals. Latched and decoded address inputs and





Plessey bubble memories

standard add-ons and custom-built

Now you can confidently incorporate UK-originated bubble memories in your next development: Plessey is fully equipped to design and produce to your spec. Or you can buy add-in bubble memory cards for your Intel SBC systems. Plessey has a range of compatible systems actually in production – the first in Europe. Shouldn't you be talking to us now?

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Telephone: Towcester (0327) 50312. Telex: 31628.

Plessey Microsystems Inc, 19546 Clubhouse Road, Gaithersburg, Maryland 20760.

Telephone: (031) 948 2791. TWX: 710 828 9708

and at 1641 Kaiser Avenue, Irvine, California 92714.
TWX: 910 595 1930.

*Intel trademark.

CIRCLE 94 ON INQUIRY CARD

latched Tri-State[®] TTL outputs facilitate easy interfacing to most 8-bit microprocessors, including the 8060 sc/MP (by the same manufacturer), 8080, 8085, Z80, and 6800.

These 8-bit data acquisition chips are designed for users who may not require the full 16-bit multiplexing capability of the ADC0816, an existing monolithic device in the same product line. The newly announced units use the same techniques to provide fast, accurate operations with minimal power consumption. They are particularly suited to such applications as process control, industrial control, and machine control.

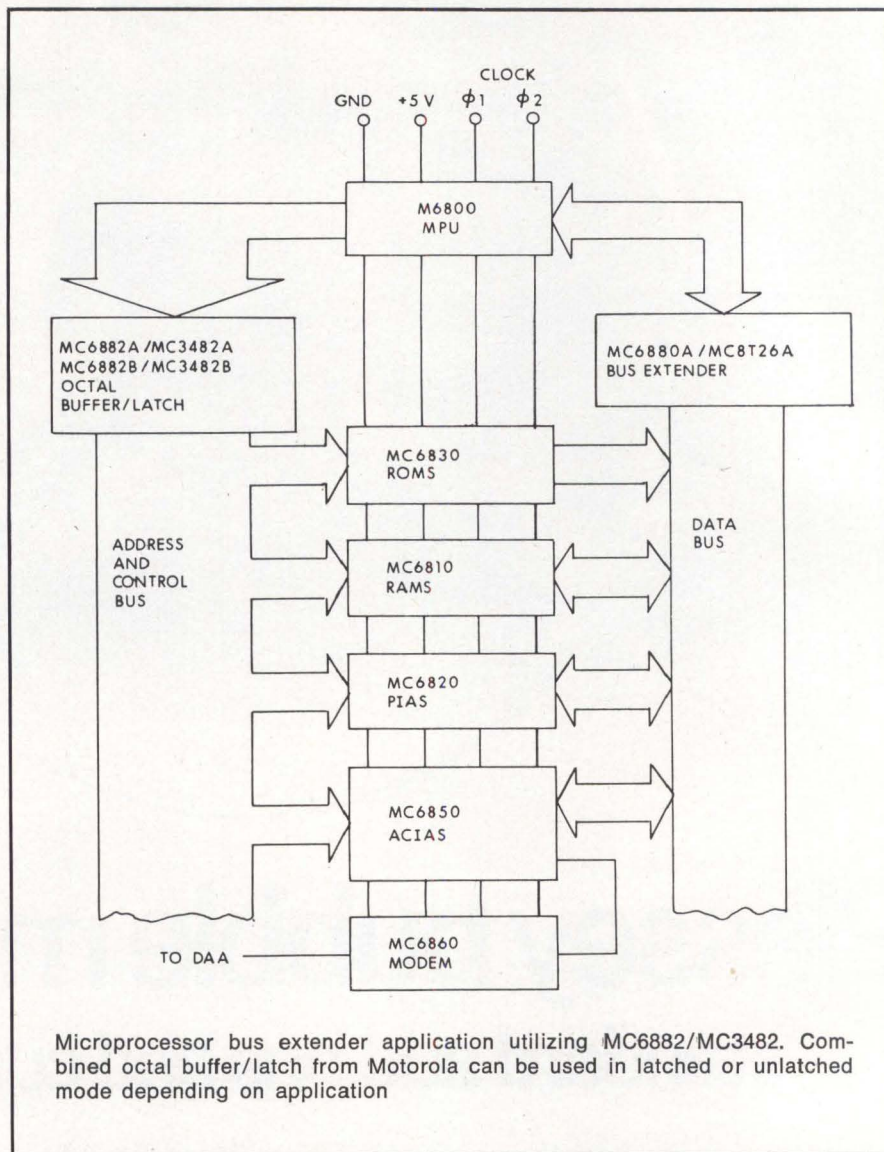
Octal Buffer/Latch Simplifies Interfacing Of Peripherals to μ Ps

Designed to interface between an 8-bit microprocessor and a loaded address bus, an octal 3-state buffer/latch has a propagation delay of only 8.0 ns (typ), with an output drive capability of 48 mA. Two octals eliminate the need for three previously used hexadecimal buffers and two octal latches, offering a cost saving and allowing higher system speed.

Eight transparent latches and buffers are included in a single package. The combined unit from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, is designated as the MC6882/MC3482. These devices are offered in both inverting (A suffix) and noninverting (B suffix) versions. The manufacturer indicates that they are pin-out and functionally compatible with the SN74LS373, a 3-state latch, while offering over double the output drive capability with equivalent speeds. In addition, they feature buffered control inputs, and all inputs have hysteresis to improve noise rejection.

Additional characteristics include a single 5-V power supply, full parallel access for loading and re-loading, and high impedance pnp inputs to assure minimal loading of the bus. The devices are based on Schottky technology and interface with a wide range of microprocessors, including M6800 microprocessor systems.

Absolute maximum ratings limit power supply voltage, V_{CC} , to 8.0



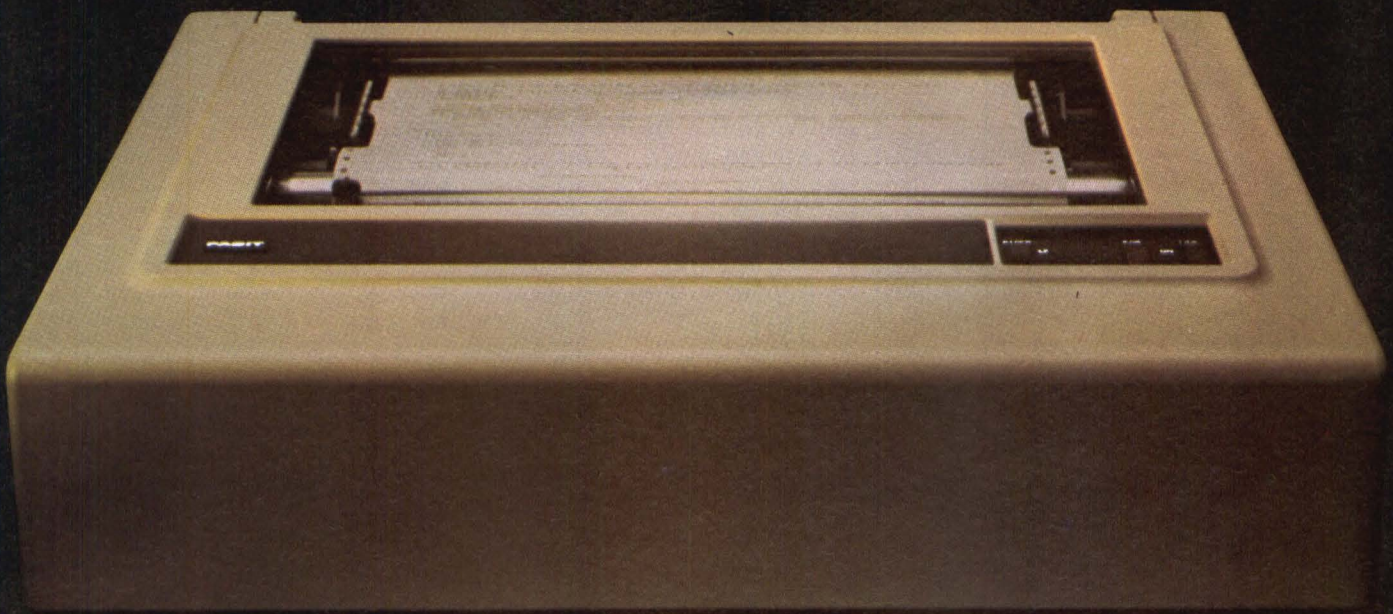
V_{dc} and input voltage to 5.5 V_{dc}. Allowable temperature range is 0 to 75 °C in operation and -65 to 150 °C in storage. The devices are provided in 20-pin ceramic dual-inline packages. Prices in hundreds are \$2.80 for the inverting and \$2.90 for the noninverting models.
Circle 352 on Inquiry Card

Floating Point Chip Performs 32- And 64-Bit Operations

Single precision (32-bit) and double precision (64-bit) add, subtract, mul-

tiply, and divide operations are provided by a floating point arithmetic peripheral processing unit. All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus, compatible with a wide range of 8- and 16-bit microprocessors. Internally, the monolithic device employs a microprogram controlled, stack oriented architecture with 16-bit wide data paths. Operands are pushed onto an internal stack, and a command is issued to perform operations on the data in the stack. Results are then available to the host processor by popping the stack, or additional commands may be entered.

The Am9512 floating point processor unit (FPU) from Advanced Micro



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The printhead on the Facit 4540 Serial Matrix Printer is so advanced, it practically thinks for itself.

A new concept of printhead design uses 9 stored force flexible hammers to print a 9 x 9 dot matrix pattern bi-directionally at 250 cps.

The printhead movements have been reduced to a minimum. The printing principle assures extraordinarily long printhead life. With no adjustment, no lubrication and practically no wear. In fact, outstanding sharp and consistent printing results are guaranteed for more than a minimum of 500 million characters before any service might be required on the printhead.

The Facit 4540 is a prime example of the integration of mechanics and electronics which has made Facit peripheral data products world famous.



Our revolutionary printhead makes Facit 4540 a matrix printer with line printer speed.

Write for more detailed information on how the 4540 Printer can get the most out of your system.

Facit, Inc., 66 Field Point Road,
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 **FACIT**
DATA
PRODUCTS

CIRCLE 95 ON INQUIRY CARD

AROUND THE IC LOOP

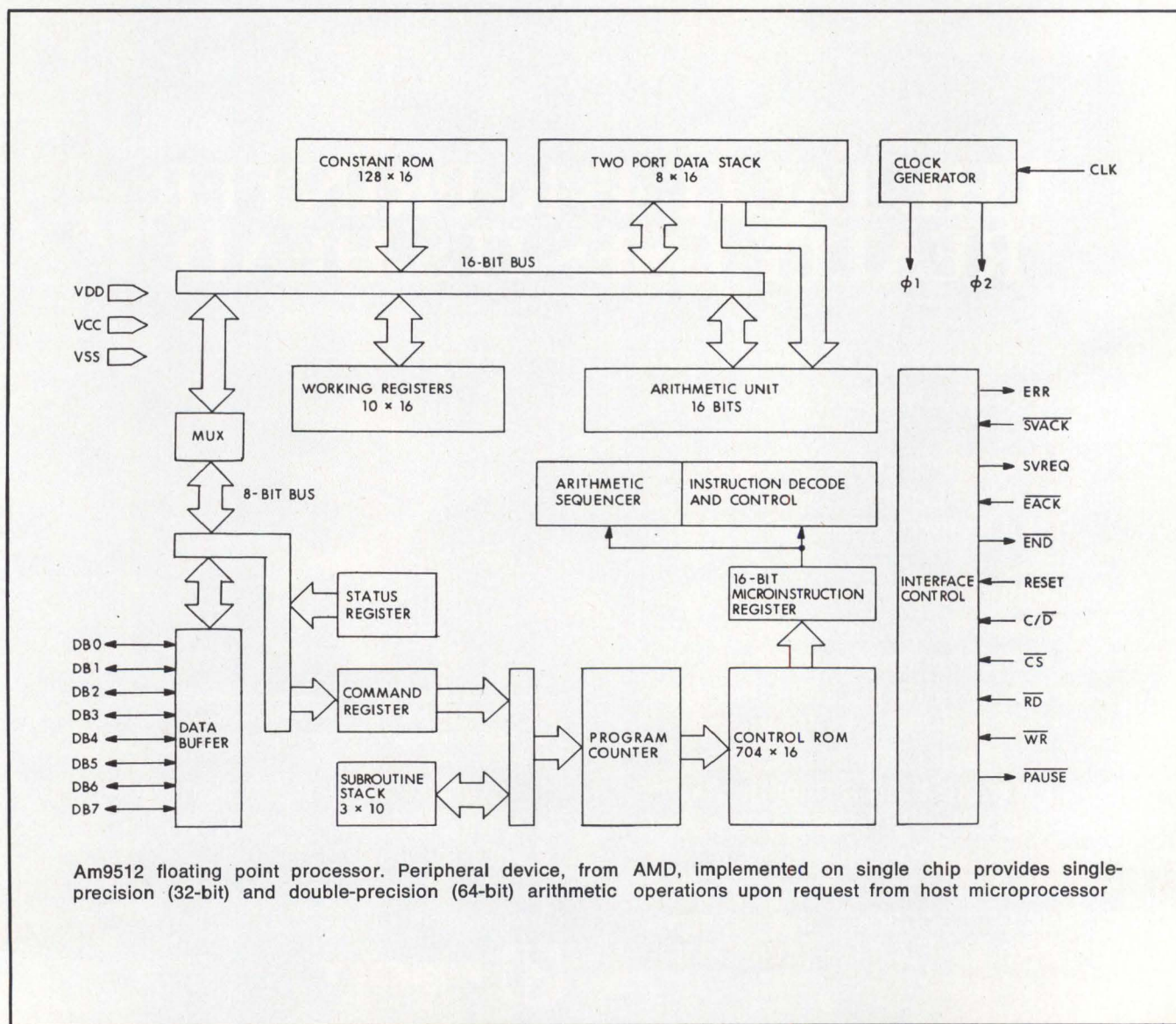
Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, supplements the existing Am9511A by the same manufacturer (see "External Arithmetic Processors" by S. Smith, *Computer Design*, Dec 1978, pp 144-149). Each is intended for nearly mutually exclusive markets, with the higher execution speeds and derived functions of the earlier device better suited for realtime applications. The newly announced FPU, on the other hand, is particularly oriented toward applications requiring high precision and wide dynamic range, such as data processing, scientific instrumentation, and educational systems.

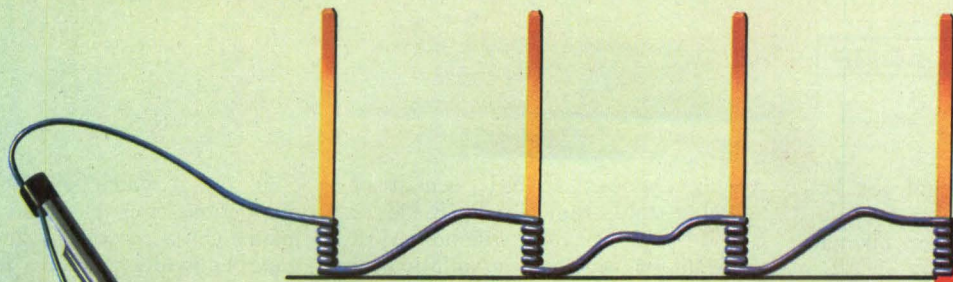
Transfers to and from the 9512 can be handled by the associated processor using conventional programmed I/O, or by a direct memory access controller for improved performance. Upon completion of each command, the FPU issues an end-of-execution signal that can serve as an interrupt to the CPU, helping to coordinate program execution. It also provides an error-output signal and status register to indicate the specific error.

In its single-precision 32-bit mode, it has a dynamic range of $2^{\pm 127}$ (6-bit exponent plus sign) and 24-bit precision. Double-precision or 64-bit

operations increase the dynamic range to $2^{\pm 1024}$ (10 bits plus sign) and precision to 52 bits. Minimum command execution times for single-precision operations using a 2-MHz clock are 28 μ s for an add or subtract, 93 μ s for multiplication, and 111 μ s for division. Equivalent double-precision execution times are 276, 253, 768, and 2043 μ s, respectively. A complex rounding algorithm causes it to be slightly slower than the Am9511A, which truncates results.

Other characteristics include versatility of interface (to almost any microprocessor), 12- and 15-V power supplies, and 850-mW power dissipation.





WHY CUT? WHY STRIP? WHY SLIT?
WHY NOT...

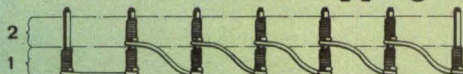
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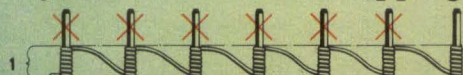
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pation (typ). The command list includes add, subtract, multiply, divide, copy, delete, exchange, change sign, and push zero.

Fabrication is based on n-channel, silicon gate MOS technology. The device is provided in a 24-pin package and undergoes 100% MIL-STD-883 reliability assurance testing.
Circle 353 on Inquiry Card

**Fast-Settling
12-Bit DACs
Need No Trimming**

A maximum settling time of 1 μ s to $\pm\frac{1}{2}$ LSB is provided by 12-bit monolithic CMOS digital to analog converters, featuring double layer metal interconnections for improved high speed operation and lower cost. Precision thin-film deposition resistors provide 12-bit linearity without laser trimming, thus eliminating any long-term instabilities that laser trimming might introduce. The use of compensating FET switches in the feedback resistor at the end of the ladder chain reduces gain error temperature coefficient to a max of 2 ppm/ $^{\circ}$ C.

Input current requirement is 2 mA (max) with less than 30 mW of power dissipation. The multiplying DACs, pin for pin replacements for

Analog Device's AD7541, consist of a highly stable thin film R-2R ladder and 14 CMOS current switches. Most applications require the addition of an output operational amplifier and a voltage or current reference.

The 8641 from Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, is the premium part with guaranteed 12-bit linearity for the designer who requires $\pm\frac{1}{2}$ LSB (0.012%) accuracy. The 8640 provides reduced accuracy of ± 1 LSB (0.024%) linearity error with 12-bit resolution.
Circle 354 on Inquiry Card

**Quad Op Amps Combine
Bipolar Programming With
FET Characteristics**

Consisting of four independent, high gain, internally compensated BIFET op amps, a family of programmable quad operational amplifiers combines the high input impedance and wide bandwidth characteristics of FET input devices with the programming capability of conventional bipolar devices. The four op amps within one of these amplifiers can be externally programmed by a separate set of control signals. This allows the user to optimize the performance of any one op amp on the

chip for a given allowable power dissipation, to select such performance characteristics as slew rate and gain-bandwidth product. The circuits are suited to active filter applications in telecommunication systems and channel bank filters, where circuit power dissipation is often a critical factor.

Produced by Exar Integrated Systems, Inc, 750 Palomar Ave, Sunnyvale, CA 94088, the 18-pin XR-096, the most versatile of the family, permits independent programming of each of its four op amps. The other two models are provided in 16-pin DIPs and have two independent programming pins. In the XR-094, one pin controls three of the chip's op amps and another controls the fourth, while in the XR-095, each programming pin controls two op amps, allowing the user to program them in pairs. These three monolithic circuits are the programmable versions of Texas Instruments' TL-074 and TL-084 series operational amplifiers.

Absolute maximum ratings establish allowable ranges of ± 18 V for supply voltage, ± 15 V for input voltage, and ± 30 V for differential input voltage. Package power dissipation may not exceed 625 mW for the plastic package (derated by 5.0 mW/ $^{\circ}$ C above $T_A = 25^{\circ}$ C) or 750 mW for the ceramic package (derated by 6.0 mW/ $^{\circ}$ C above 25° C).
Circle 355 on Inquiry Card

DEC USERS

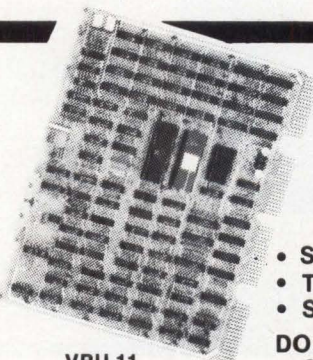
**ARE YOU HAVING PROBLEMS WITH
YOUR CRT DISPLAY APPLICATION?**

- SCREEN UPDATES BOGGING DOWN SOFTWARE?
- TOO MANY INTERRUPTS TO SERVICE?
- SCREEN GLITCHES AND POOR APPEARANCE?

DO YOU NEED?

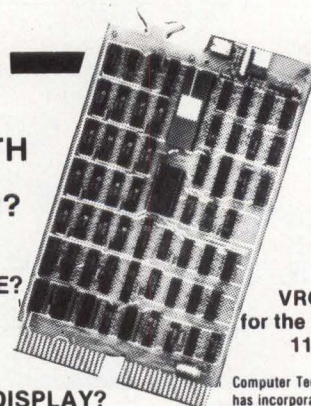
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**VRU-11
for the PDP-11/04
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Also available for
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Computer Technology has incorporated the most requested features from three years of video display experience into its newest cross-compatible family of video products. These features are available to your application NOW.

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Speaking of changing your mind, when you want to change address locations of either RAM or EPROM, it's done with two, on-board switches—providing 16 possible start locations for each memory.

Compare these features with our much improved read, write and refresh cycle times and you'll choose MSC first.

16K RAM Version

Up to 16K x 8 of RAM and up to 16K x 8 of EPROM on the same board.

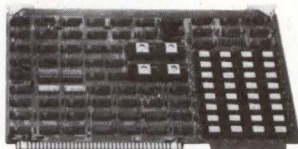
RAM expandable in 4K x 8 increments and EPROM expandable in 1K, 2K or 4K x 8 increments.

On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally MULTIBUS hardware and software compatible.

Limited one year warranty on parts and labor.



MSC 4502.....\$710

NOW \$675*
(16K)

64K RAM Version

Up to 64K x 8 of RAM and up to 16K x 8 of EPROM on the same board.

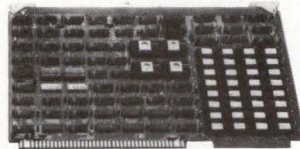
RAM expandable in 16K x 8 increments and EPROM expandable in 1K, 2K or 4K x 8 increments.

On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally MULTIBUS hardware and software compatible.

Limited one year warranty on parts and labor.



MSC 4602.....\$2175

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***Even greater savings on quantity.**

12-Bit ADC Replacement Operates Faster and Uses Less Power

A 12-bit hybrid analog to digital converter provides a 5- μ s conversion time and $\pm\frac{1}{2}$ LSB ($\pm 0.012\%$ fsr) linearity error, with power consumption of 1.6 W (typ). The ADH-8586 is a pin compatible replacement for the industry standard ADC-85, but operates at twice the speed, with reduced power, and extends the maximum operating temperature from 85 to 125 °C.

Typical applications include data acquisition systems, automatic test equipment, and electronic counter-measure systems. Produced by ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716, the ADC is processed to MIL-STD-883. With optional burn-in, its MTBF is 1.6×10^6 hours for ground fixed conditions and 25 °C case temperature.

The converter has five pin programmable input voltage ranges: 0 to 5 V and 0 to 10 V with complementary binary coding, or ± 2.5 , ± 5 , and ± 10 V with complementary offset binary coding. An internal input buffer amplifier can be used to increase the input impedance to 100 M Ω with only a slight reduction in speed. Speed can be increased by short cycling and by programming the internal clock for higher clock rate. A 3- μ s conversion time and 300-kHz word rate can be obtained with 10-bit resolution.

Two power supplies of ± 15 and ± 5 V are required. The device is housed in a 32-pin hermetically sealed triple DIP metal case, having dimensions of 1.75 x 1.05 x 0.22" (4.45 x 2.67 x 0.56 cm) and a weight of 0.67 oz (19 g). A lower speed option, the ADH-8585, consumes only 1.2 W (typ) with a 10- μ s conversion time.

Circle 356 on Inquiry Card

Low Noise Op Amps Are Second Sourced

Monolithic operational amplifiers having equivalent input noise voltages of 4.0 and 3.5 nV/ $\sqrt{\text{Hz}}$ (both typical values) are being offered on a second source basis by Texas Instruments Inc, PO Box 225012, Dallas, TX 75265. The devices are, respectively, the NE5534 and NE5534A,

designed to be interchangeable with the Signetics parts having the same designations. In addition to the typical equivalent input voltage of 3.5 nV/ $\sqrt{\text{Hz}}$, the -A suffix model has a guaranteed maximum of 4.5 nV/ $\sqrt{\text{Hz}}$.

These op amps typically exhibit a unity-gain bandwidth of 10 MHz, a common mode rejection of 100 dB, a large signal differential voltage amplification of 100 V/mV, a pk-pk output voltage swing of 32 V, a high slew rate of 13 V/ μ s, and the ability to drive a 600- Ω load. They operate over a large range of supply voltages, ± 3 to ± 20 V, and have output short circuit protection and input diode protection. Both models are characterized for operation over the commercial temperature range of 0 to 70 °C.

The op amps are internally compensated for a gain equal to or greater than three. Optimization of the frequency response can be achieved by use of an external compensation capacitor.

Circle 357 on Inquiry Card

Low Resolution Monolithic 4-Bit ADC Samples 30M Bits/s

Claimed by its manufacturer, TRW LSI Products, PO Box 1125, Redondo Beach, CA 90278, to be the industry's only monolithic 4-bit analog to digital converter available off the shelf, the TDC-1021J is available at \$29 in hundreds. It can digitize an analog signal at rates from dc to 30M samples/s without an external sample and hold circuit. The single chip is fully parallel, TTL compatible, and utilizes 1k closely matched bipolar components.

It finds application where high speed, small size, and low cost are important but high resolution is not. Among these applications are video data conversion, radar data conversion, high speed multiplexed data acquisition, image processing, and facsimile systems.

The circuit comprises 15 sampling comparators, combining logic, and an output buffer register. A single convert signal controls the unit operation. Additional capabilities include the option of binary or 2's complement output, two power sources (5 V and -6 V), 250-mW power dissipation, and an operating temperature range from -60 to 150 °C. Linearity is $\pm\frac{1}{2}$ LSB, and aperture jitter is 30 ps. The package is a 16-pin ceramic DIP that measures 0.3 x 0.8 x 0.17" (0.76 x 2.0 x 0.43 cm).

Circle 358 on Inquiry Card

4k Static RAM Offers Access Time Options From 150 to 450 ns

A 4096-bit static random access memory, the EA2114L, is available in five models offering access time options ranging from 150 to 450 ns. Produced by Electronic Arrays Inc, 550 E Middlefield Rd, Mountain View, CA 94043, and organized as 1024 x 4, the NMOS RAM is designed for memory applications where realtime I/O access, large storage, easy interface, and high performance are important, such as in microcomputers, video terminals, communication equipment, and computer peripherals.

Other characteristics include TTL compatibility, a single 5-V power supply, $\pm 10\%$ voltage supply margins, and 80 °C/W package thermal resistance. The memory offers economy through the elimination of dynamic clocks, strobes, and refresh circuits, as well as a compact density of 0.5M bits/ft² (5.4M bits/m²) of printed circuit board. It is system compatible with other static ROMs and EPROM elements.

Circle 359 on Inquiry Card

Low Cost 64-Word FIFO Guarantees >5-MHz Shift In/Shift Out Rate

A first in, first out (FIFO) bipolar serial memory is designed to fill the gap between very slow (1-MHz) MOS and very fast (10-MHz) memories. Having a storage capacity of 64 4-bit words and a shift in, shift out rate of 5 MHz (guaranteed), 8 MHz (typ), the single-chip memory is available at \$13.80 in hundreds.

The S67401 from Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, is intended to provide a less expensive alternative to high speed FIFOs in temporary data storage and data rate matching applications that do not require a maximum transfer rate. Its high density and medium I/O speed increase the options available to the designer of such devices as communication buffers, disc controllers, and Winchester type disc drives.

Additional characteristics include TTL inputs and outputs, asynchronous or synchronous operation capability, and packaging in a 16-lead, 0.3" (0.8-cm) wide DIP. It is readily expandable in bit dimensions, although not cascadable in a word direction.

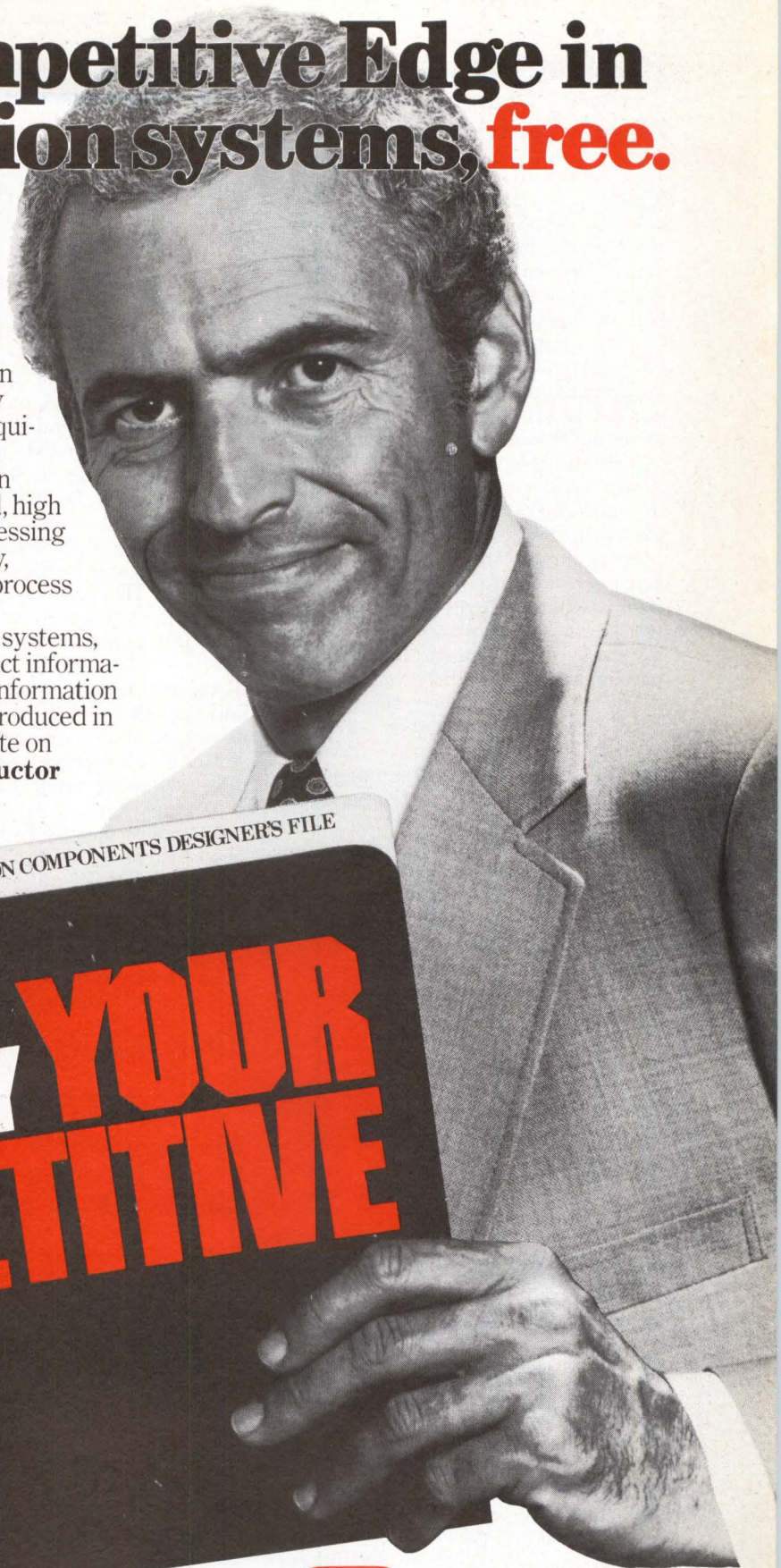
Circle 360 on Inquiry Card


Grab the Competitive Edge in data acquisition systems, **free.**

Today's advanced microprocessors and digital processing systems require high performance components to interface the digital/analog world. Harris Semiconductor has assembled a design file which presents a family of performance-proven data acquisition circuits and applications which will stimulate your design imagination. This designer's file could be the key to solving some of your most perplexing data acquisition problems.

Harris has a complete line of data acquisition components. All of which provide the high speed, high accuracy and high throughput you need for processing fast signals in all types of applications—military, aerospace/avionics, instrumentation, industrial process control, EDP, and others.

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*Harris Technology
... Your Competitive Edge*



**HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION**

A DIVISION OF HARRIS CORPORATION

Monolithic Device Contains Complete PWM Power Control Circuitry

Each device in a family of ICs from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, contains all the control circuits for a power supply inverter or switching regulator integrated on a single chip. The devices feature complete pulse width modulation control circuits, single-ended or push-pull outputs, and line and load regulation of 0.2%. Total supply current is less than 10 mA with an operating frequency beyond 100 kHz.

The sc1524, offered as a second source to Silicon General's part having the same designation, can be used for switching regulators of either polarity, transformer coupled dc-dc converters, transformerless voltage doublers, and polarity converters, as well as in other power control applications. It maximizes the efficiencies in any of the three basic types of switched-mode power supply circuits: forward converters, flyback converters, and push-pull converters. The device is specified for operation over the full military temperature range of -55 to 125 °C.

Specific circuits contained in the 16-pin dual-inline package are a voltage reference, oscillator, error amplifier, current-limiting circuits, pulse width modulator, and pulse steering flipflop. A commercial version, the sc73524, is available, specified over the 0 to 70 °C range. There is also an intermediate version, the sc2524, which shares the tighter electrical specifications of the top of the line model, while having the temperature characteristics of the commercial version.

Circle 361 on Inquiry Card

Ramp Oscillator, Logic, And Motor Logic ICs Control Stepping Motor

Three integrated circuits may be used in a variety of ways to provide low power signals for the control or actuation of stepping motor drive systems. The MSI devices provide alternatives to extensive software or numerous discrete components.

This chip set from Sigma Instruments Inc, 170 Pearl St, Braintree, MA 02184, consists of the 29G01 CMOS ramp control logic circuit (RCL), the 29G21 linear bipolar ramp control oscillator (RCO), and the 29G41

digital motor logic circuit (DML). The RCL is normally used in conjunction with the RCO. Together, the two circuits form a buffered ramp, able to accept a constant high frequency pulse train to deliver a variable frequency output with preset acceleration and deceleration profiles. The output of these chips can drive the DML motor logic IC or almost any other stepping motor drive. Used alone, the RCO can be employed in a number of ways to generate fixed or variable frequency pulse trains, including ramped frequency trains for speed control applications.

Intended to be the key element in a motor driver, the DML accepts a pulse train input and decodes it into a selectable, parallel output stepping motor phase excitation format. It has sufficient flexibility to fit most data input and output formats. Input can be either dual pulse trains, cw or ccw, or a pulse line and a direction line. The phase outputs can be 2-, 3-, or 4-phase in either full-step or half-step sequences, and can be selectively disabled for either standby power reduction or damping. In addition, the outputs can be in wave or overlapping sequences. There are separate connections for a reverse pulse damping input and an initial reset input.

The chips operate from 8- to 15-V power supplies, on typical logic level inputs, with most outputs open-drain active circuits for maximum noise immunity. RCL dimensions are 0.600 x 1.310" (1.524 x 3.327 cm); maximum dimensions for RCO and DML chips are 0.250 x 0.870" (0.635 x 2.21 cm).

Circle 362 on Inquiry Card

Bus Compatible Binary Up Counter Can Reach 10 MHz

An LSI 32-bit binary up counter with 32 latches, multiplexer, and eight 3-state outputs is capable of counting up to 10 MHz. The LS7060, produced by LSI Computer Systems Inc, 1235 Walt Whitman Rd, Melville, NY 11747, presents its information in 8-bit binary bytes, least significant byte first, to the 3-state outputs at clock rates up to 1 MHz. Successive data bytes are enabled to the outputs on each positive transition of the scan pulses.

A special cascading feature allows any number of the devices to be attached to the same bus. Information from the counters can then be read out in successive bytes in se-

quence within the cascaded string. Each successive scan pulse enables the next data byte and, when each counter finishes presenting its information, it enables the next counter.

The device is an N-channel MOS silicon gate chip in a high density 18-pin package with 0.3" (7.6-mm) row spacing. Inputs are TTL, CMOS, and NMOS compatible, and outputs are TTL compatible.

Circle 363 on Inquiry Card

CRT Timer-Controller Display, Monitor Formats Are User Programmable

A cathode ray tube video timer-controller is implemented in N-channel MOS as an LSI device. All frame formatting, horizontal, vertical, or composite sync, characters per data row, data rows per frame, and raster scans are completely user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8-bit internal registers from a bidirectional data bus. Four register address lines plus a CS line provide complete microprocessor program controlled setup. The device may be self loaded via an external P-ROM tied to the data bus. Formatting also may be programmed by a single mask option.

This timer-controller from Solid State Scientific, Montgomeryville, PA 18936, contains the logic functions required to generate timing signals for presentation and formatting of interlaced and noninterlaced video data on a standard or nonstandard CRT monitor. In addition to the control registers, the device has storage registers which hold the cursor character and data row addresses used to generate the cursor video signal. The contents of these registers also may be read out onto the data bus for update by the program.

Two versions of the chip are available. The SND5037 can be programmed for an odd or even number of scan lines per data row in both interlaced and noninterlaced modes. Programming it for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays. The SND5027 provides noninterlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. Circle 364 on Inquiry Card □

ROLM's Mil-Spec ECLIPSE® Data System... a new power in military computers

Military operations on the move make tough demands on data processing systems.

The computers must be compact, rugged, and reliable. The data base and operating system must be transaction-oriented for fast real-time, interactive processing.

That's why ROLM developed the Mil-Spec ECLIPSE Data System. It's tough and has all the proven advantages of Data

General's ECLIPSE® architecture and software. The key is a sophisticated multiprogramming Advanced Operating System (AOS), which controls real-time, multi-user, and batch operations... all while effectively managing up to 2 Megabytes of main memory.

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For shipboard systems, this flexible computing power is fully compatible with Naval Tactical Data Systems when joined

with ROLM's new 3400 Series Interfaces. These compact MIL-STD-1397 modules come in SLOW, FAST, ANEW, and SERIAL types with 8, 16, and 32-bit configurations. They are interchangeable and feature software transparency. Designers can configure a system to match the data requirements of any ship... without restriction on future expansion.

ROLM's Mil-Spec ECLIPSE System lets you move out with power never before available in a military computer system. Designed to meet MIL-E-5400, MIL-E-4158, and MIL-E-16400 specifications, it gives you extensive software, full peripheral support, and ROLM reliability and service.



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CIRCLE 100 ON INQUIRY CARD

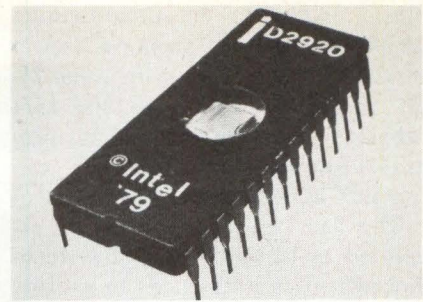
PRODUCT FEATURE

Single-Chip Analog Microcomputer Processes Complex Signals in Real Time

Multiple component and multicircuit analog subsystems required for real-time signal processing applications can now be replaced by a single-chip programmable analog/digital microcomputer. Claimed by its developer, Intel Corp, to be the first such analog input/output microcomputer, the 2920 signal processor provides capabilities equivalent to those of a microcomputer 10 times as powerful as the 8086 (or 100 times those of the standard 8080). For instance, the 8080 can operate as a signal processor at frequencies up to only a few hundred Hertz, while the digital processor on the 2920 executes its program at typically 13k times/s when used with a 10-MHz clock rate.

In operation, the signal processor converts analog input signals to digital information, manipulates that information in its onchip high speed, digital processor, and produces analog outputs in a realtime mode. Its frequency range covers those common in telecommunications, instrumentation, control, guidance, medical, and other electronic systems.

An SP20 hardware and software support package, introduced for use with the 2920, includes assembler, software simulator, erasable programmable read only memory (EPROM) programming personality board, and documentation. Both assembler and software simulator run on the Intellec® microcomputer de-



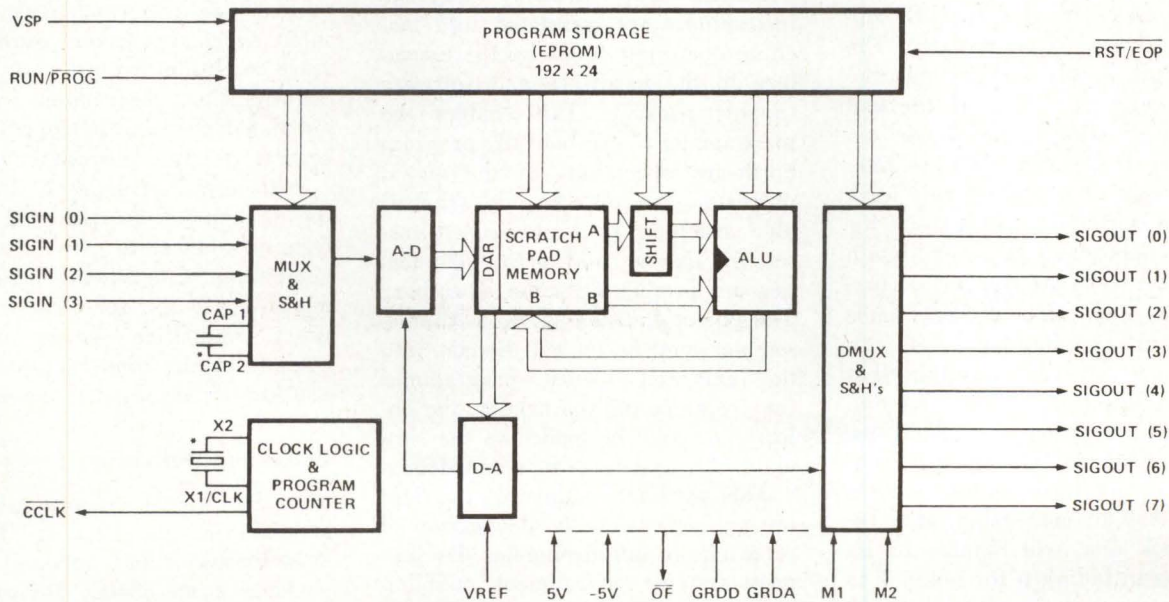
2920 signal processor

velopment system; the personality card allows EPROM on the 2920 to be programmed on an Intellec universal P/ROM programmer.

Signal Processor

Digital circuitry on the 2920 single-chip signal processor includes EPROM program storage, scratchpad random access memory (RAM), clock and timing logic, binary shifter, and arithmetic logic unit (ALU). Analog circuits include four inputs, input multiplexer, input sample and hold (S/H), analog to digital (A-D) and digital to analog (D-A) converters, output demultiplexer, eight outputs, and buffered output s/Hs. To achieve the efficiency and speed necessary for realtime operation, analog circuits operate simultaneously with digital ones.

EPROM consists of 192 24-bit words, with each word made up of six instruction fields that control individual subsystems (see functional



*EXTERNAL COMPONENTS

Functional block diagram of signal processor (run mode)

block diagram). In programming mode, EPROM is arranged as a 1152 x 4-bit memory with each 24-bit instruction loaded as six 4-bit nibbles. Once the EPROM is programmed, the signal processor can function as an analog subsystem.

The RAM read/write array is organized as 40 words of 25 bits each. Address space is extended to provide constants and access to a register (DAR) for interfacing the memory ALU with the analog conversion section. Both RAM and the ALU represent data in 2's complement format. All operations are performed in 2's complement arithmetic.

An external clock can be used or the signal processor can generate its own clock with an external crystal. The program counter is incremented one instruction count for every four master clock cycles and continues to increment until it reaches a count of 191 or is reset. Instructions are executed sequentially and no program jumps are provided. Sample rate is determined by the number of instructions in the program and the instruction cycle time.

A binary shifter between the memory "A" port output and the ALU "A" operand input allows the "A" operand to be scaled by any magnitude between 2^2 and 2^{-13} (left shift 2 to right shift 13). When a number is shifted right, vacated bit positions are filled with the sign bit.

The ALU calculates a 25-bit result based on an operation performed on the scaled "A" and the "B" operands delivered from memory. The 25-bit result is written back into the "B" memory location near the end of the instruction cycle. Logic accommodates the left shift scaling. For arithmetic operations, this logic is used to calculate a 25-bit result for normal operations and to maintain the sign bit when an overflow occurs.

Analog input channels are made up of four sampling switches with a common external capacitor that yields an offset of $< -1/2$ LSB and an acquisition time of < 2400 ns. Successive approximation A-D conversion is performed under program control. A 9-bit conversion, at a 10-MHz clock rate, will require 25 instructions including 6 for input, 1 to initialize the DAR to zero, and 18 for the A-D conversion.

Eight analog output channels include one s/H circuit/channel de-



SP20 hardware and software support package

multiplexed from a common, buffered D-A converter output. Signal output (SIGOUT) pins can be selected to be either analog out or TTL compatible.

The internal D-A converter requires a single, user supplied 1- or 2-V reference to establish its range. The resulting input and output signal voltage range is $\pm V_{REF}$.

Support Package

Symbolic 2920 assembly language instructions are translated into machine operation codes by the assembler in the hardware and software support package. This enables the programmer to symbolically program hardware operations of the signal processor. An object code (executable machine code), complete assembly listing, and error diagnostics are produced by the assembler. The object code output from the assembler may be loaded directly into the universal P/ROM programmer for programming the EPROM; the object code may be loaded to the simulator for system design and debug.

The software simulator provides testing and symbolic debugging of programs in microcomputer development systems environment, enabling designers to specify input signals; set breakpoints; collect and display input, output, and system variables; and display and alter contents of

memory location during simulation. Hex format object files produced by the assembler are accepted by the simulator. Output values and internal trace data may be saved on ISIS-II disc files for further analysis.

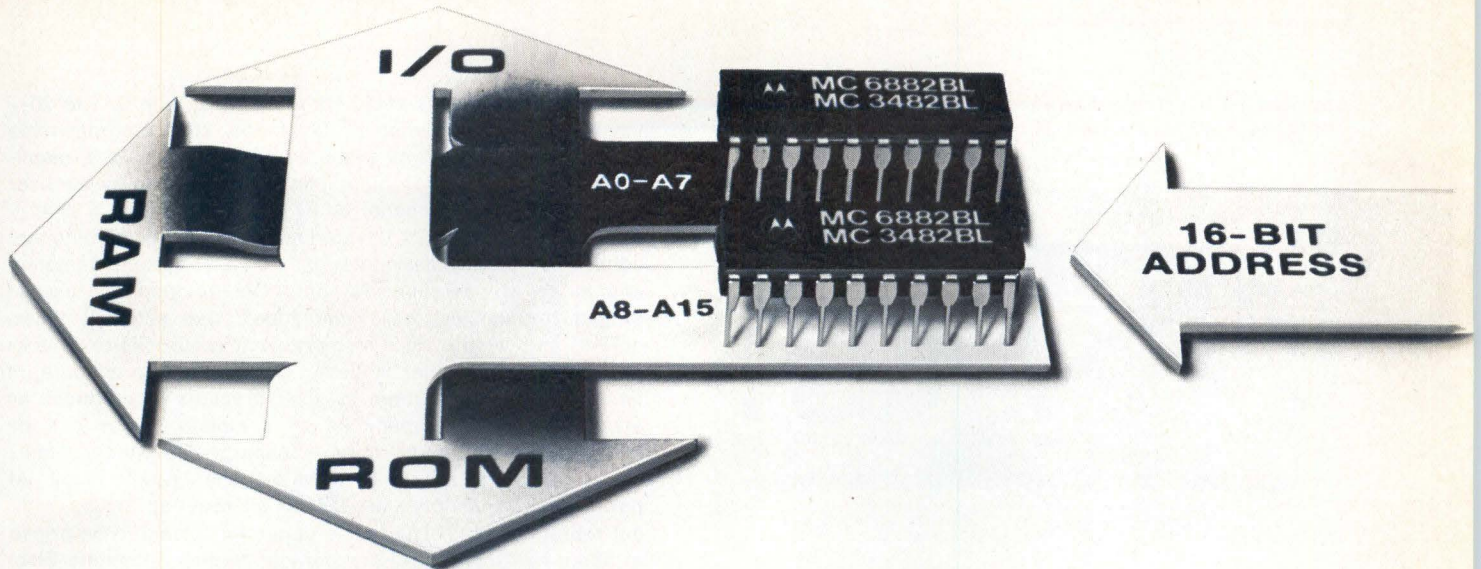
Simulation of signal processor machine instructions is performed in software. All internal registers, memory, input values, output values, and other system variables can be examined and modified. Speed of on-chip signal processing simulation varies with the complexity of the input signal, breakpoint setting, and trace condition. Exclusive of I/O time requirements, instructions will be simulated at a rate of approximately several hundred instructions/s.

After each instruction is simulated, the breakpoint is evaluated to determine whether to stop or continue simulation. Conditional breakpoints are also provided for debugging purposes. Simulation can be manually stopped at any time by pressing the ESC key on the Intellec console.

Price and Delivery

The 2920 signal processor is priced at \$250 in quantities of 100; the SP20 hardware and software support package costs \$3400. Deliveries of both began in September. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Tel: 408/987-8080. Circle 199 on Inquiry Card

Technological leadership.



Double your drive, tune out noise with Motorola's 3-state, octal buffer latch.

Despite being around for a while from multiple sources using known LS technology, quantities of octal buffer latches are usually gone by the time you get to the ordering stage. Even if you've been lucky enough to find any lately for MPU memory address bus buffering, chances are they haven't lived up to every performance parameter you could wish for.

Until now.

Now Motorola can supply a steady stream of these impossible-to-get parts with some new wrinkles that make the MC6882/3482 linear interface family an absolutely great find for enhancing system production and performance.

More margin, more boards, less noise.

The units furnish a full, 48 mA I_{OL} drive capability—twice what LS373 types offer. That means you've got much more margin to drive more memories and more boards without any increase in parts count. And this top performer drives a full 500 pF load. You can't do better than that anywhere.

Built-in hysteresis provides noise immunity. The output switches only when you want it to. And the part can be latched to further protect your system from noise.

Mux, demux, buffer and latch.

Together or separately. Inverting or non-inverting. You can use it on latched bus structures such as the '6801 or on unlatched

structures like the '6800 where buffers are latched to provide noise immunity.

When multiplexing with a pair, each drives 8 bits alternately from a three-state output.

It offers fast, 8 ns typ Schottky prop delay, single 5 V power supply requirements and high impedance PNP inputs to ensure minimum bus loading.

Last, not least, it's pin-for-pin, spec-for-spec compatible with LS373 types, so all you do is drop it into those designs and watch it take over. With more drive... and at nearly equal cost.

Device	Suffix	Inverting/Non-Inverting	Price (100-up)
MC6882A/ MC3482A	L (ceramic)	Inverting	\$2.80
MC6882B/ MC3482B	L (ceramic)	Non-inverting	2.90

Contact your authorized Motorola distributor or write Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for complete data and turnaround on the MC6882/3482.

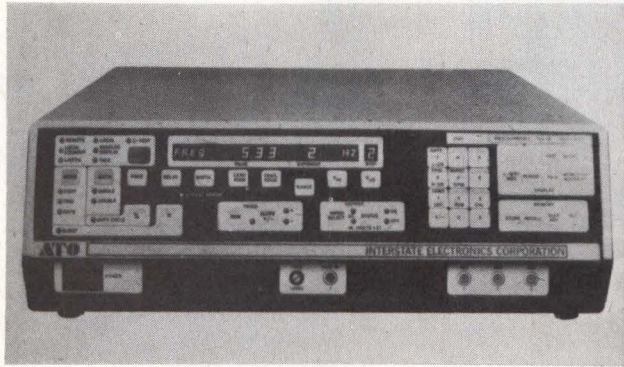
Together with our M6800 family of MPUs, MCUs and peripherals, you'll have your next complete generation of

Innovative systems
through silicon.



MOTOROLA INC.

Low Cost Programmable Pulse Generator Features Fast Response Time



Circle 200 on Inquiry Card

Repetition rate pulses of 10 Hz to 50 MHz, with 0.1- to 20-V amplitudes, are produced by the model 2021 programmable pulse generator in 7 ns (variable to 10 ms at 20-V amplitude). A 20-V amplitude pulse can be established by the user from either the front panel or by program control in a 40-V window from -20 to 20 V, referenced to ground. Annunciator lights and alphanumeric displays identify pulse parameters and mode of operation. An Auto Cal function, for use at critical frequencies, calls amplitudes, use and fall times, delays, and widths from memory. A microprocessor checks parameters and either initiates a correction procedure, if needed, that adjusts them to desired values or produces an error message. As many as 10 complete setups can be stored in the internal memory. A rechargeable battery retains the memory unit for up to 4 weeks when power is off. At power-up the memory unit recalls all required setups without reprogramming. This pulse generator is said to be priced at about half the cost of comparable models. **Interstate Electronics Corp.**, PO Box 3117, Anaheim, CA 92803.

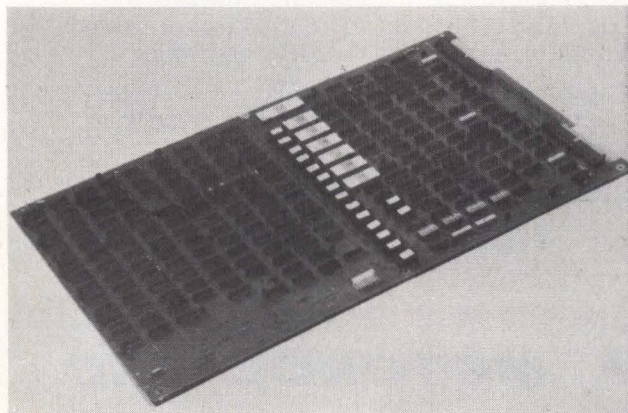
V.27 Compatible 4800-Bit/s Data Modem Fits Wide Range of Applications



Conformation to CCITT Recommendations V.27 bis and V.27 ter, MOS circuitry, and a complete range of system monitoring and fault isolation, including V.54 remote loopback and low speed V.23 secondary channel, enable the LSI/48/V.27 high speed data modem to meet a variety of user requirements. The device operates at 4800 bits/s over 2- or 4-wire leased lines or 2-wire dial networks, with fallback to 2400 bits/s, and uses 8-phase DPSK or QAM for primary signaling in the transmitter and receiver. Narrow band modulation and fully automatic adaptive equalizer (with other V.27 bis modems) assure low error rates under all conditions. Choice of switch or strap selectable operating modes allow system operation over degraded circuits. Point to point operation is over M580 or equivalent lines; a type M1020 line is recommended for optimum performance in multipoint applications. Other features include low frequency 75- or 150-bit/s secondary channel, EIA RS-232-C or CCITT V.24 compatible interface, and automatic or manual answer. **Codex Corp.**, 20 Cabot Blvd, Mansfield, MA 02048.

Circle 201 on Inquiry Card

Signature Analysis Provides Diagnostic Capability for Single-Board Tape Formatter

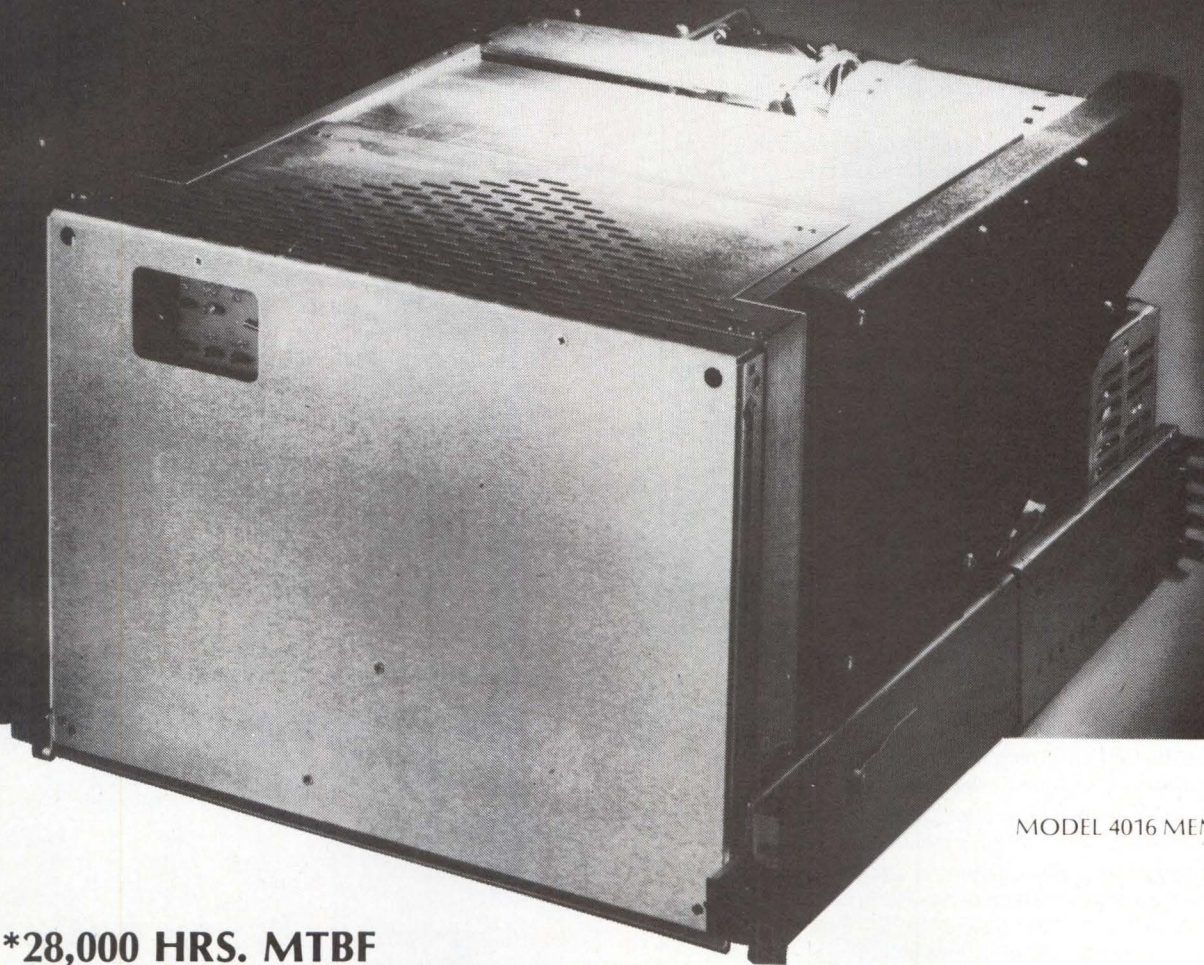


A bipolar bit slice microprocessor in the model 9X00F dual-density magnetic tape formatter provides a signature analysis capability that allows a technician to locate malfunctions by comparing microprocessor-generated patterns with those based in ROM. Presence of the microprocessor also improves control and reduces the number of needed ICs; the resultant reduced board size permits installation of the 13 x 8.5" (33 x 21.6-cm) single-board formatter in the chassis of the company's model 9000, 9100, 9300, 9700, or 9800 9-track read-after-write tape transports. As many as 4 daisy chained transports with 2 different speeds can be handled by 1 formatter. All logic required for reading and writing both 1600-char/in (630/cm) PE and 800-char/in (315/cm) NRZI formats for ANSI and IBM compatible tape is in ROM. Speeds from 12.5 to 125 in/s (31.7 to 317 cm/s) are selectable by onboard DIP switches. Switches also control status and address designations. **Kennedy Co.**, 1600 S Shamrock Ave, Monrovia, CA 91016.

Circle 202 on Inquiry Card

PROVEN RELIABILITY

THE RADIANT FEATURE
IN MEMORY



MODEL 4016 MEMORY

***28,000 HRS. MTBF
DEMONSTRATED AND IMPROVING
37.9 MEGABITS
8.5 MILLI SEC. AVE. ACCESS
.035 CENTS PER BIT O. E. M.**

***ASK FOR A COPY OF OUR MTBF STUDY**

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CIRCLE 102 ON INQUIRY CARD

MAGSTRIPE™ Card Readers



BY
AMERICAN
MAGNETICS

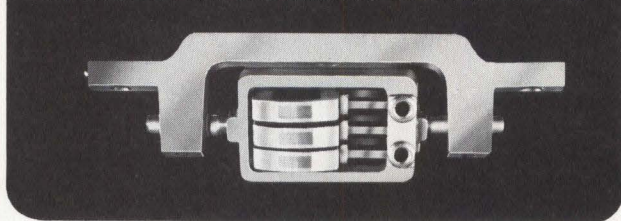
Proven, World-Wide Performance

Field proven, economical means for collecting data from magnetic stripe cards or badges.

Standard models read ANSI X 4.16 - 1976, any combination of tracks 1, 2, or 3 (75 and 210 BPI); special models available for any track density up to 400 BPI.

Self-contained spatial decoding electronics provide TTL (data and strobe) outputs. Card velocity range 3 to 120 inches/second; completely acceleration independent. Less than one error per 10^6 bits.

UNIQUE MAGSTRIPE™ HEADS INDEPENDENTLY-SUSPENDED, GIMBAL-MOUNTED



Reliability in reading warped and soiled cards is achieved by means of a patented read head assembly — each head individually suspended on parallelogram springs in a gimbal mount. Low contact force guarantees lowest head and card wear.

Rugged construction permits outside installation and exposure to the elements. Virtually maintenance free.

Many major system manufacturers, after extensive testing, have chosen our readers which out-perform all others in reading "real world" cards. Our MAGSTRIPE™ Readers are used world-wide in a variety of applications including:

- Airline Ticketing Terminals
- Bank Terminals
- Building Access Systems
- Bulk Fuel Dispensing Terminals
- Data Input for CRT Terminals
- Computer Access Devices
- Fare Collection Systems
- Identification & Badges
- POS Terminals
- Self-Service Gas Stations

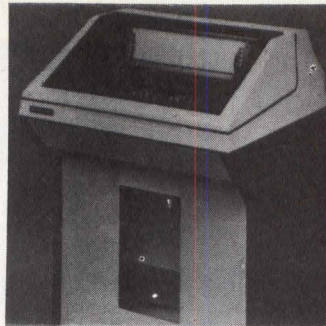


For more information and technical data, contact:

American Magnetism Corporation

2424 Carson St., Torrance, Calif. 90501
(213) 775-8651, TWX 910-349-6956

DUAL-SPEED STEEL BAND LINE PRINTERS



Enhanced print capabilities on both 300- and 600-line/min band printers enable line speed to be reduced to 170 and 350 lines/min respectively, in approx 4 s. Std high quality printout at 300 or 600 lines/min is suitable for day to day printing requirements or drafts, and quality obtained at 170 or 350 lines/min fills needs for special reports or final

copies. Dual print speed is accomplished through the micro-processor architecture of the printers. The print band speed can be switched under program control. Printers are designed for 30 to 40% duty cycles, and feature a 3000-h MTBF. Tabletop, pedestal, and quiet cabinet models are available. **NEC Information Systems, Inc**, 5 Militia Dr, Lexington, MA 02173.

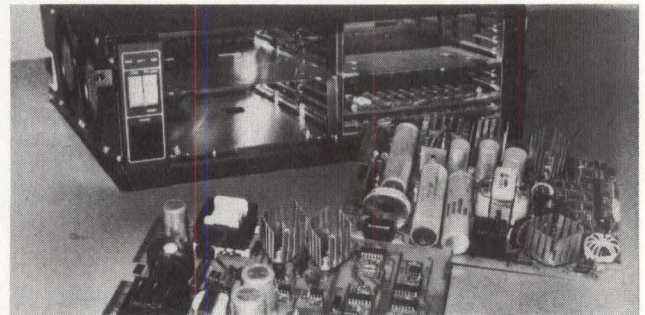
Circle 203 on Inquiry Card

HIGH CAPACITY FIXED MEDIA DISC DRIVE

4700 series drives based on 3350 technology yield high capacity, fast access, rapid data transfer, and high reliability. Device incorporates a mechanical package design that is small in size for easy installation and requires only 7" (17.8 cm) of vertical rack space. 112M- and 158M-byte configurations are achieved by use of either 3 or 4 disc platters, respectively. Performance characteristics are 30-ms avg access time (6-ms track to track), 9.40-MHz data transfer rate with a projected module life of 35k hours. Storage density is 6427 bits/in (2530/cm). Total per surface capacity is 22.6M bytes. Soft error rate is 1 bit/ 10^{10} ; hard error rate is 1 bit/ 10^{13} . **Microdata Corp**, 17481 Red Hill Ave, Irvine, CA 92714.

Circle 204 on Inquiry Card

MICROCOMPUTER POWER SYSTEM OPTIONS



Permitting the microNova™ MP/100 and /200 to operate during temporary power failure, the optional model 4315 battery backup is contained on a single PC board. With the addition of either the optional model 4316 battery pack or 2 ordinary car batteries, users can keep computers plus main memory operating when main ac power fails. All voltages are maintained and fans are kept operating. Battery pack consists of two 12-V batteries connected in series and includes mounting hardware and cable that plugs into backplane. The 2.5-Ah pack supplies power for 16 min to a 64k-byte MP/100 system, and for 7 min to a 64k-byte MP/200. **Data General Corp**, Rt 9, Westboro, MA 01581.

Circle 205 on Inquiry Card

AED ANNOUNCES ITS NEW PDP-11 LINE-UP.

Single card RM-02[®] emulation

The fullback for the PDP-11 team is AED's new STORM-02, a hex-card controller/format-ter for storage module drives.

We tried out a lot of fullbacks for the team but STORM-02 was the only player that could offer everything! Single hex-card electronics; RH-11, RM-02 and RM-03 emulation; the ability to plug right into the SPC slot on your PDP-11; plus the ability to get along with the media. That's the kind of compatibility we like!

A standard single board STORM-02 handles 4 SMDs. With an optional second hex-card, the STORM-02 can accommodate four more drives for a total capacity of over 500 megabytes.

Our big surprise was the bottom line on the contract. The OEM price for the STORM-02 is just \$2370 for the hex-card electronics — far less than any fullback in the league. The complete system with one 80-megabyte storage module drive, in quantities of one, is \$13,500 . . . about half the price of a comparable DEC fullback.

For the complete statistics and quick delivery, call or write Bob Deisher, Rigid Disk Products Manager.

Big disk RP-04[®] emulator

The noseguard for the PDP-11 team is the field proven AED8000. He anchors the line with his ability to tackle 4 CPUs at one time. The 8000 also provides microprogrammable data control and intermediate buffering between your PDP-11s and up to 8 mass storage drives — including Winchester — in any combination simultaneously. That means over 2200 megabytes of data storage on the gridiron.

This versatile player emulates the DEC RP Series controllers, thus saving management big bucks by always having software transparency with successive DEC operating system releases. And the 8000 will run DEC's disk system diagnostics as well!

Check this list of accomplishments:

- RP-03, RP-04 and RP-06[®] emulation
- Microprogrammable 24-bit power
- Handles any combination of Ampex, Calcomp, CDC, ISS and Memorex drives
- 56-bit Fire Code Error Correction
- 256 x 16-bit data buffer

For complete statistics on economical OEM prices and fast delivery, call or write Bob Deisher, Rigid Disk Products Manager.

Full color graphics system

The coach of PDP-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new PDP-11 'coach' a cost/performance leader include:

- DMA interfaces (Q-BUS[®] or UNIBUS[®]) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
- SUPEROAM panning over 1024 x 2048 contiguous pixels.
- Programmable character fonts and 8 programmable special function keys.
- \$6,875 with two colors only, excluding monitor and DMA.

For delivery information, write or talk to Jerry Kennedy, VP Marketing.

[®] Registered trademark of Digital Equipment Corp.

**ADVANCED
ELECTRONICS
DESIGN, INC.**

COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400

CIRCLE 104 ON INQUIRY CARD

COMDEX '79

December 3-5, 1979
MGM Grand Hotel, Las Vegas

If you are a distributor, dealer, commercial OEM, systems house, turnkey vendor, manufacturers representative, value adder, software packager or any other kind of independent "third party" seller, you should plan now to attend this stimulating three day conference and exposition.

Over 30 sessions will focus on the challenges and opportunities facing you as a dealer . . . for more profitable selling and a higher degree of professionalism.

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The National Conference & Exposition
for Dealers, Distributors and Reps

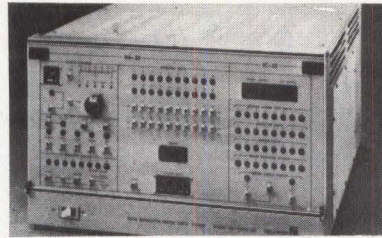
Another Conference and Exposition from
The INTERFACE Group

Producers of:
Data Communications INTERFACE, INTERFACE WEST,
FEDERAL DP EXPO, COMDEX

160 Speen Street, Framingham, MA 01701

PROGRAMMABLE WORD GENERATOR AND ERROR CHECK SYSTEM

DG-20/EC-20 provides both data generation and error check capabilities in a single benchtop or rackmount unit. It contains a variable clock source, 256-word x 20-bit data generator, and 8-bit error comparator. Internal clock oscillator



provides variable operation from 2.5k to 20M bits/s. Programmable word generator section provides 20 parallel outputs at ECL levels, suitable for driving 50- Ω coaxial line. Word length is integer variable up to

256 words. Error check section provides for error check comparisons on up to 8 input channels. Individual inputs may be masked out to inhibit error checking of those channels. Operational controls allow unit to continuously check input data or to stop on first error condition. **Tau-Tron, Inc.**, 27 Industrial Ave, Chelmsford, MA 01824.

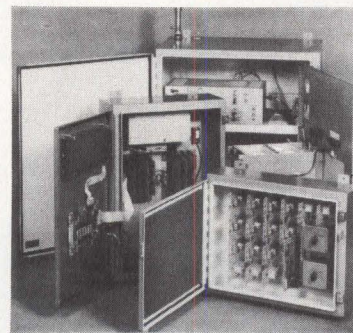
Circle 206 on Inquiry Card

ECLIPSE/NOVA 3 ADD-IN MEMORIES

Designed for use with Data General Eclipse and Nova 3, the in1560 has full software compatibility with the Nova 3, and incorporates onboard parity control. It has very low power dissipation, and high circuit density to reduce system cost. Battery backup operation can be supported. An onboard memory management and protection unit provides full 128k addressing and detection of 5 software violations. 32k and 128k configurations occupy a 15" (38-cm) board. For use with Eclipse computers, the in5150 is compatible with both core and semiconductor memories. It has onboard error logging facilities and can support 2-, 4-, or 8-way interleaving. An onboard cache memory gives a 200-ns access time. Capacity is 64k. **Sintrom Electronics Ltd.**, Arkwright Rd, Reading, Berks RG2 0LS, England.

Circle 207 on Inquiry Card

ANALOG AND DIGITAL I/O MULTIPLEXERS



Series 2300 provide I/O for industrial data gathering and control systems. Analog and digital inputs and outputs are transmitted and received via a serial communication link with either RS-422 or RS-232 interface at data rates up to 9600 baud. Std interfaces include dry contact inputs for supervised or unsupervised lines, 110-Vac digital inputs, 10-

and 12-bit analog inputs, 8- and 10-bit analog outputs (4 to 20 mA), and 3- and 10-A start/stop relay outputs. Each unit consists of NEMA 12 enclosure backpanel with connectors, I/O interfaces, and controller board containing microprocessor and communications interfaces. DGC 2331 handles digital inputs. 2333 accepts 4 analog inputs and generates 1 analog output; digital I/O can be either 16 inputs and 8 outputs, or 8 inputs and 16 outputs. 2320 has up to 16 I/O slots. **Logicon Process Systems Div.**, 10398 Democracy Lane, Fairfax, VA 22030.

Circle 208 on Inquiry Card

AED ANNOUNCES ITS NEW LSI-11 LINE-UP.

Low priced RX-02[®] emulator

The quarterback for the LSI-11 team is the new FLEX-02, a dual-width floppy disk controller/interface card. The FLEX-02 earned its starting role by proving its ability to completely emulate DEC's RX-02 while offering RX-02 users double-headed drive capabilities — a feature no other league quarterback has right now.

Best of all, in OEM quantities the single bluechip FLEX-02 dual-width PC board costs just \$700, including the bootstrap loader. (Try getting a 'quarterback' with this kind of talent elsewhere at the same price).

In full gear, a two-drive double-headed disk system with an AED power supply in a 5¼" DEC look-alike cabinet is only \$3940 for quantity one. The complete double-drive, single-headed system is just \$3440 in a quantity of one.

Whether you have RSX-11/M, RT-11V3A/B, I.A.S., RSTS-3, CTS-500 or CTS-310 operating systems centering the ball, the versatile FLEX-02 can now complete the line-up and lead your DEC data to the end zone.

For complete statistics and quick delivery, call or write Steve Loring, Diskette Products Manager.



COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400

RL-01[®] compatible Winchester

The linebacker for our LSI-11 team, the WINC-01, is surprisingly small for a pro. He consists of just two PCBs — one a microprocessor-based formatter/controller mounted with a SA-4008 drive, and the second, a dual-width Q-BUS interface card that inserts directly into the CPU backplane.

However, when WINC-01 proved he could deliver Winchester technology to DEC LSI-11, -11/2, -11/23 users, we signed him up immediately. He amazed us by playing with up to three SA-4008 Winchester drives and tackling up to a total of 60 megabytes of data. Additionally, he has the capacity to include a plug-in floppy disk drive.

Best of all, he bunked with the DEC RL-01 driver software and we can report they are very compatible up to 20 megabytes.

In contract talks, the WINC-01 demanded considerably less than the DEC hardware: his two boards sell together for under \$1150 in OEM quantities. The complete system, including the two PCBs, an AED power supply, one SA-4008 drive and a DEC look-alike cabinet sell for \$6700 in quantities of one.

For WINC-01 technical information and quick delivery, contact Bob Deisher, Rigid Disk Products Manager.

Full color graphics system

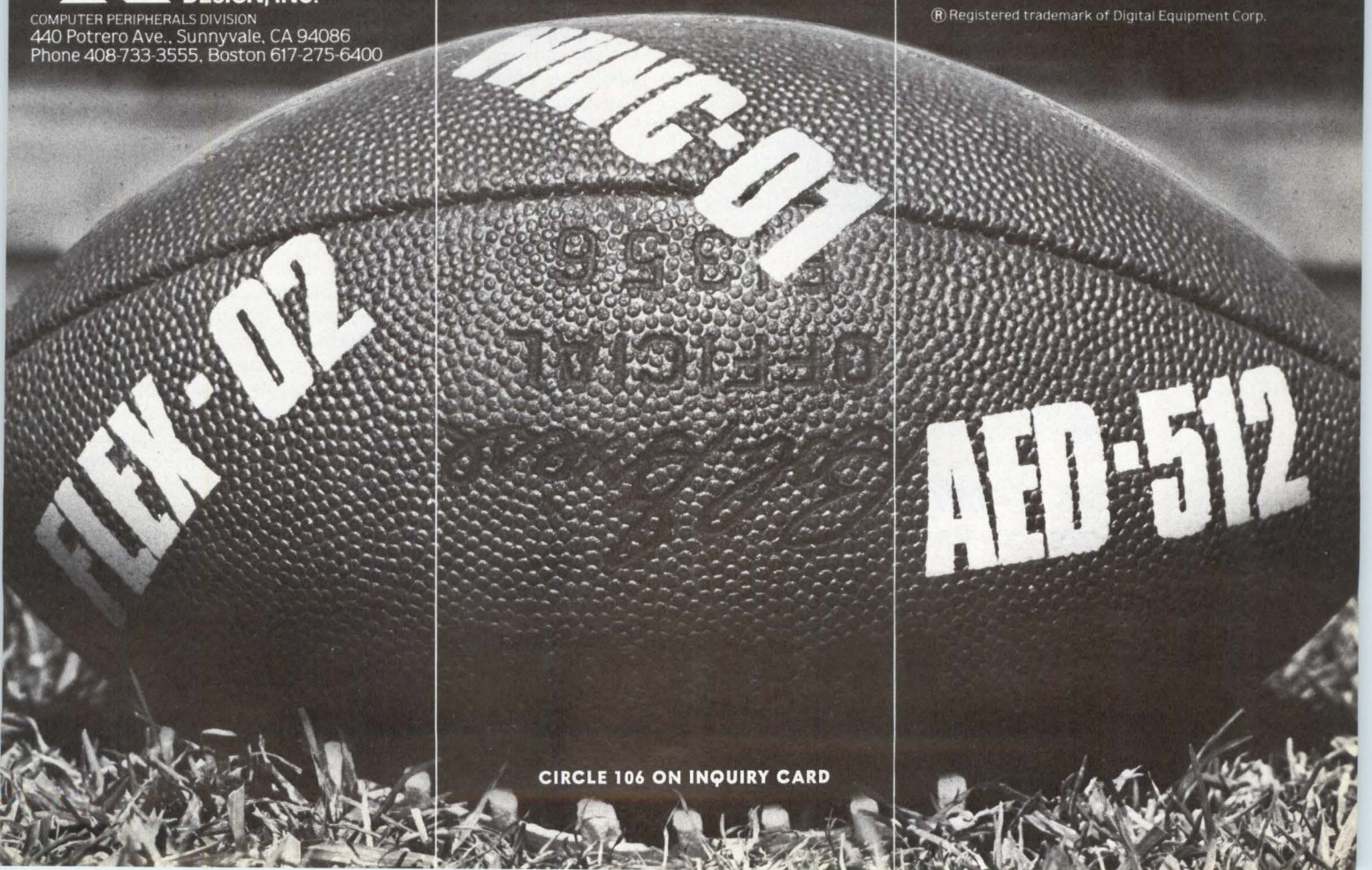
The coach of LSI-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new LSI-11 coach a cost/performance leader include:

- DMA interfaces (Q-BUS[®] or UNIBUS[®]) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
- SUPEROAM panning over 1024 x 2048 contiguous pixels.
- Programmable character fonts and 8 programmable special function keys.
- \$6,875 with two colors only, excluding monitor and DMA.

For delivery information, write or talk to Jerry Kennedy, VP Marketing.

[®] Registered trademark of Digital Equipment Corp.



CIRCLE 106 ON INQUIRY CARD

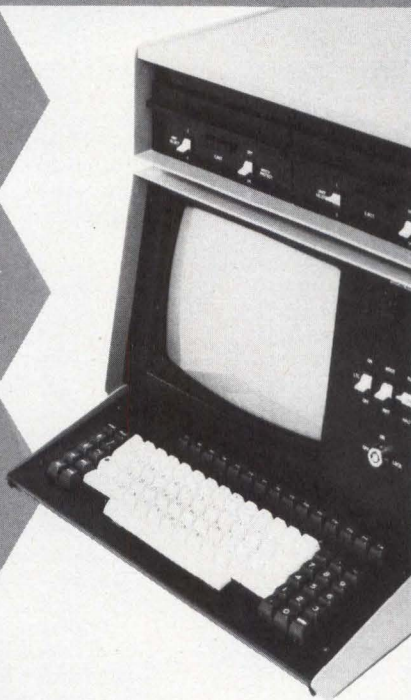
MULTIBUS*

Development/Target System

Floppy Disk Subsystem
Single/Double Density

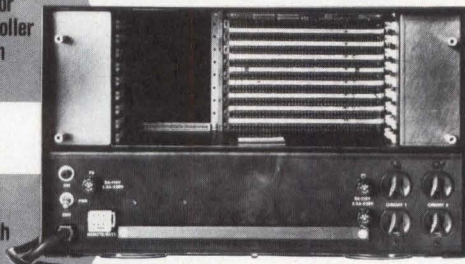
80 X 24 Display
7 X 9 Dot Matrix
Key Lock Control

ASCII Keyboard
15 Function Keys
Numeric Key Pad



9 Multibus Slots for
CPU Display Controller
Memory & System
Expansion

30 Amp +5V
Power Supply with
Switched AC



12" Integrated Computer System
64K Bytes RAM
Dual Floppy Disk Subsystem
8085 CPU
Price: \$8,935

ISIS • CP/M •
Fortran • Basic • Pascal •
Macro Assembler**

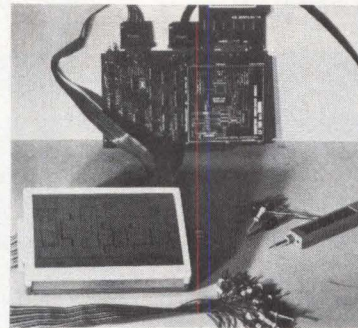
*Multibus and ISIS are Trademarks of Intel Corporation
**Configured to run all Intel supplied software

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(617) 894-7000 • TWX: 710-367-4318 **The BusMasters**

EXPANDABLE SIGNATURE ANALYSIS DATA MULTIPLEXER MODULE

Signature data multiplexer operates under software control in conjunction with the LS 100 series bus plug-in peripheral signature analyzer. Inputs to the LS MUX 32 multiplexer can be individual inputs to quick disconnect connectors, 40-pin



DIP clips for microprocessor and LSI component connection, and bus terminator/card edge connectors for computer card interface. By cascading analyzers and multiplexers in a microcomputer bus, a limitless number of signature data lines can be input. Multiplexer is totally controllable from the analyzer and user computer

system. Associated status and control words allow full software control. Software is available for Z80, 8080, 6800, and 6502 processors. **Phoenix Digital Corp**, 3027 N 33rd Dr, Phoenix, AZ 85017.

Circle 209 on Inquiry Card

MULTIUSER PROGRAMMING STATION FOR IN-CIRCUIT TEST SYSTEMS

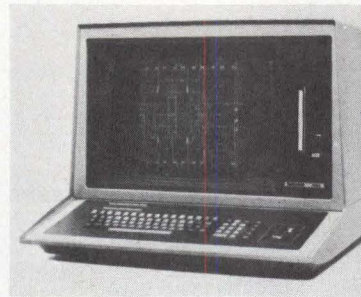
Designed to complement the 2270 test system, the 2290 off-line programming station allows simultaneous program generation by up to 4 users. By performing program generation offline, the unit increases productivity of the test system by eliminating machine time conflicts between programmers and production personnel. The station is equipped with a DEC PDP-11 based computer and 128k bytes of memory. It has a single CDC Hawk 10M-byte fixed head disc drive and controller. Two disc cartridges provided with the unit contain 2270 program preparation software, 2 have RSX-11M binary system software, and 2 are blank. The unit is housed in a single low profile vertical rack. **GenRad Inc**, 300 Baker Ave, Concord, MA 01742.

Circle 210 on Inquiry Card

GRAPHIC COMPUTING SYSTEM WITH DYNAMIC OPTION

Dynamic Graphics option provides users of the 4054 Graphic Computing System with the power to work directly with graphic elements of a design problem, in addition to points and lines. Simple BASIC commands allow users to create

and manipulate graphics objects as simple as line or word, or as complex as a 1000-vector object or user definable key menu. After being created, an object is saved in dynamic memory for later recall. With 13M addressable points, the 19" (48-cm) direct view storage tube offers high resolution graphics. Option 30

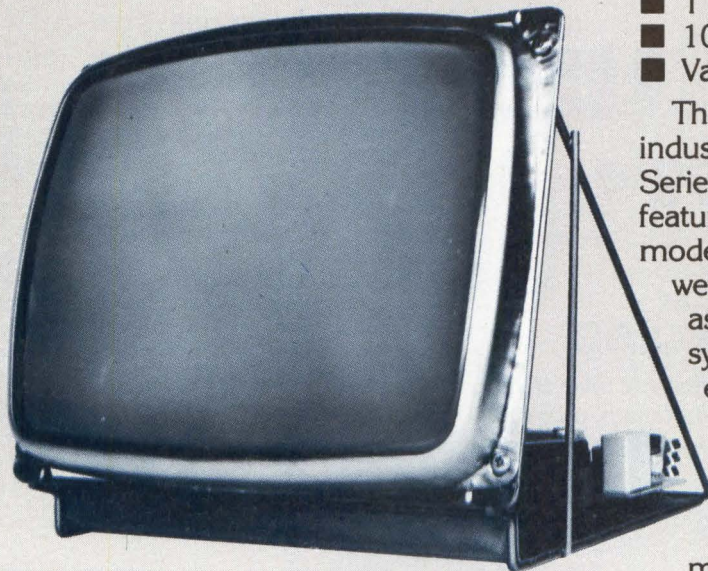


is a field installable circuit board containing microprocessor and 32k bytes of memory dedicated to creation and display of refresh objects, completely independent of the 4054's processor. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077. Circle 211 on Inquiry Card

In Data Display. . .

TV means performance with economy

**BALL TV Series general purpose displays
have advanced features**



BALL TV Series
general purpose
display

- 5, 7, 9, 12-inch sizes
- TTL-compatible sync interface
- 100% silicon circuitry
- Variety of frame styles

The TV Series is the standard of the industry for general purpose data display. TV Series users get many of the advanced features found on BALL high-performance models. Features such as strong and light weight wire frame design, simple sub-assembly construction, TTL-compatible sync interface circuits for direct drive, and electronic linearity control.

As with all BALL display products, the TV Series can be modified to suit your exact needs. You aren't hampered by lack of choice in mechanical or electronic specifications.

Even with the proven level of TV Series dependability, you'll be glad to know that BALL maintains fully staffed regional service centers, ready to deal quickly with any problems.

You can't buy a more dependable and low life-cost display than a BALL TV Series unit. Take a close look at life cycle costs, and you'll have a BALL every time.

**In data display,
BALL means
experience, quality
and service.**

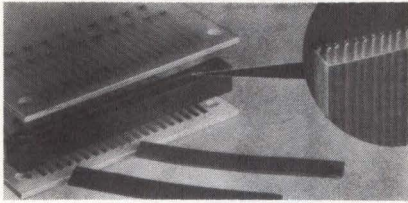


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Sales Offices:
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CIRCLE 108 ON INQUIRY CARD

PRODUCTS

PRINTED CIRCUIT BOARD STACKING CONNECTORS



CONMET provides electrical connection between PC boards mounted in mother-daughter fashion. Connector element is comprised of 0.003" (0.076-mm) dia wire, vertically oriented and equally spaced in 1 row and surrounded by solid silicone rubber except for contacting tips. High density of wires in element enables interconnection of any contact arrangement having at least 0.025" (0.635-mm) wide pads and 0.010" (0.254-mm) spaces. **Technical Wire Products, Inc.**, 129 Dermody St, Cranford, NJ 07016. Circle 217 on Inquiry Card

MICROPROCESSOR CONTROLLED THERMAL PRINTER ASSEMBLY



Capable of printing 2½ 20-char lines/s, the PL-20E thermal line printer uses a 5 x 8 dot matrix to form u/lc ASCII characters with descenders. The controller provides an invert mode for mounting this assembly in any position, a self-test mode, automatic carriage return and line feed for lines longer than 20 char, and std 8-bit parallel interface. Power requirements are 5 Vdc at 150 mA and 20 Vdc at 500 mA. **Telpar, Inc.**, 4132 Billy Mitchell Rd, Addison, TX 75001. Circle 218 on Inquiry Card

A new T-bar® miniature 6PDT Toggle Switch

Full Size.



2 million cycles
for computers, minicomputer and main frame
formatting, data communications equipment, medical,
industrial instrumentation, and stop-start test switching

T-BAR Series 202 6PDT Mini-Paddle Lever Switches are designed for "must operate" applications. T-BAR Edge-to-Dome™ bifurcated contacts provide the SitStill™ reliability that protects the integrity and stability of millions of circuits during continuous use or even long periods of inoperation. The 202 retains its initial characteristics through 2-million operations. Call for application help.

T-bar® INCORPORATED

SWITCHING COMPONENTS DIVISION

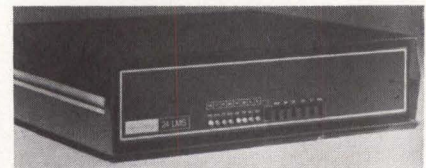
141 Danbury Road Wilton, CT 06897 Telephone: 203/762-8351 TWX: 710/479-3215

FIXED DISC EMULATING SUBSYSTEM

Interfacing with all Data General and DG emulating CPUs, the DMAA is a self-contained modular random access disc emulating controller which gives bulk memory addressing capability beyond 64k and speeds data transfers in existing operating systems. The unit is contained on a 15 x 15" (38 x 38-cm) PC board and occupies one card position in the computer chassis. The controller is compatible with existing RDOS, IRIS, and BLIS operating systems. **Mini Mag, Inc.**, 5611 Kendall Court, Suite 104, Arvada, CO 80002.

Circle 219 on Inquiry Card

IBM COMPATIBLE LOOP MODEMS



Designed to operate in conjunction with IBM 3600 financial communication loop systems, 12 and 24 LMS modems provide 1200- and 2400-bit/s operation as direct replacements for IBM 3603 terminal access unit. Features include automatic central site notification of network problems, fault isolation at unattended remote sites, and restoration of failed network components when used with the company's 185 network diagnostic controller or 200 network management center. Dial backup capabilities are provided. **Racal-Milgo, Inc.**, 8600 NW 41st St, Miami, FL 33166.

Circle 220 on Inquiry Card

PRODUCTS

DIGITAL CAPACITANCE MEASUREMENT PROBE

C-Probe II attaches directly to the input of any std frequency counter and causes the counter to directly display the value of capacitors from 0.1 pF to 10,000 μ F with a picofarad range accuracy of 0.25% to 200,000 pF and accuracy of 0.5%



in the microfarad range to 10,000 μ F. Measurement cycle times are 0.1 s to 30 μ F, 1 s to 3000 μ F, and 10 s above 3000 μ F. Controls include range selection, resolution (X1 or X10), user selectable gate times (0.1, 1, or 10 s), output signal attenuation (X1, X10, or X100),

10-turn calibration potentiometer for pico and microfarad ranges, and 10-turn potentiometer for stray or lead capacitance cancellation to 50 pF. **International Instrumentation Inc.**, Box 3751, Thousand Oaks, CA 91359.

Circle 212 on Inquiry Card

LARGE CAPACITY HIGH SPEED MEMORY BOARDS

Dynamic random access memory boards BLC-032, -048, and -064 provide 32k, 48k, and 64k bytes, respectively. Each includes all refresh, timing, control, and buffering circuitry, and 20-bit address decode which allows use in a 1M-byte memory. All boards have access time of 430 ns and full read or write cycle of 660 ns. BLC-064 has a max power requirement of 20.7 W. The boards operate as either 8- or 16-bit memories, and allow for 1-board expansion of 16-bit systems. Used in either advanced or delayed write mode, they have logic circuitry for battery backup and memory protection, for user installed byte parity, and onboard refresh logic. **National Semiconductor Corp.**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

HIGH RESOLUTION PARALLEL AND SERIAL INTERFACE PRINTERS

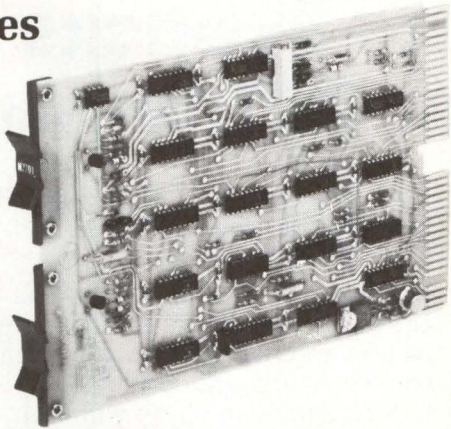


IPS-7048 and -7049 parallel interface printers and -7248 and -7249 serial Teletype compatible printers feature a 9-wire printhead and a 7 x 9 dot matrix instead of the 7 x 7 matrix provided by earlier parallel and serial models. All models print a 96 ASCII char set in a 7 x 9 matrix at 200 char/s. -7048 and -7248 feature a 500-char circular buffer; -7049 and -7249 offer a 3500-char buffer. Other features include programmable vertical format, control which allows operator selectable printing of either 6 or 8 lines/in (2.3 or 3.1/cm); audible alarm to alert operators to problems; self-test switch to aid in fault diagnosis; and full lower case descenders that offer clean printing with true descenders. **Dataroyal, Inc.**, Main Dunstable Rd, Nashua, NH 03061.

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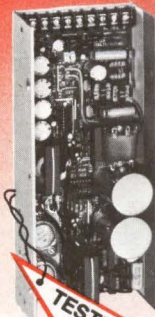
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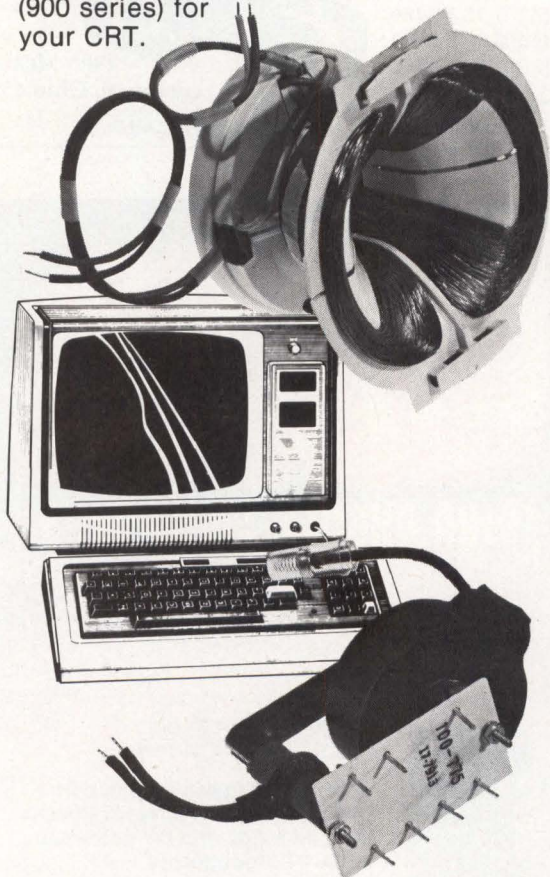
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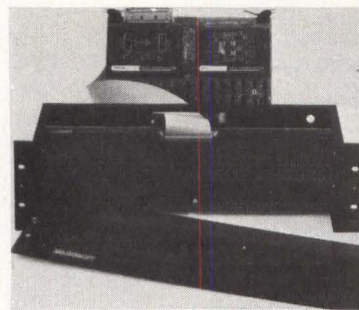


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UNIVERSAL SIGNAL CONDITIONING PANEL

Equipped with screw terminals for easy connection of analog signals, the DT701 provides a convenient junction and access point for up to 50 analog input signals. Signals may be generated by remote transducers having low level outputs, or by any of the company's microcomputer analog interface boards. The panel, a heavy duty PC board, has a std conductive-etch matrix pattern connected to analog inputs by 2 onboard screw type barrier strips; either 1 or 2 onboard 3M ribbon connectors mate via appropriate cable to computer.



Pattern of conductive etch allows user to install signal conditioning functions in up to 50 individual channels. 19 x 5" (48 x 12.7-cm) panel screws directly to std RETMA rack; for recessed mounting, the -MA option provides a RETMA std 19" mounting bracket. **Data Translation, Inc**, 4 Strathmore Rd, Natick, MA 01760.

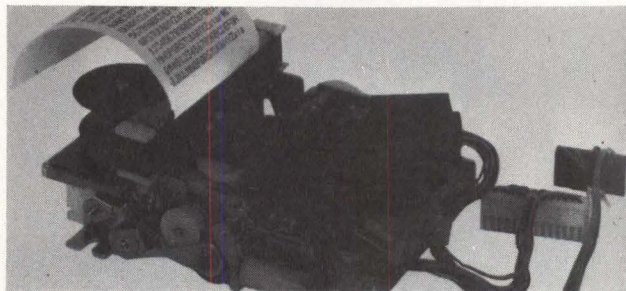
Circle 214 on Inquiry Card

LOW COST ENTRY LEVEL COMPUTER SYSTEM

A fully integrated, multiuser system, the 5000/ES offers 10M bytes of hard disc storage, 10M-byte capacity magnetic tape cartridge drive for software backup and recovery, and 4 user ports in its basic configuration. The system includes MULTUS multi-user timesharing executive. Disc storage expands in increments of 10M, 29M, or 58M to 184M bytes. Up to 4 tape cartridge drives may be installed in the basic tape module. Transfers between disc and tape cartridge may be performed programmatically, allowing up to 40M bytes of programs and data files to be transferred without physical handling of tape in a 4-drive configuration. **BTI Computer Systems**, 870 W Maude Ave, Sunnyvale, CA 94086.


Circle 215 on Inquiry Card

MINIATURE IMPACT DOT MATRIX PRINTER ASSEMBLY



Model DP-822 provides 21-col hardcopy printing at a speed of 2.5 lines/s. Its disposable 7-wire, 5-dot matrix printing head can be used with std adding machine tapes. Print-head has life expectancy of 15M char. Printer uses just one 12-Vdc motor to control head, paper feed, and ribbon mechanism. Miniature solenoids activate the 7 wires in the head. The unit weighs 650 g and measures 52.5 x 106 x 145 mm. The 5 x 7 matrix yields a printed character measuring up to 1.8 mm wide x 2.9 mm high. Line spacing is 4.24 mm. The mechanism is equipped with 2 pairs of connectors. One plugs into the controller or printer driving circuit, the other into the customer's software. **Star Micronics, Inc**, Pan Am Bldg, Suite 2308, 200 Park Ave. New York, NY 10017.

Circle 216 on Inquiry Card



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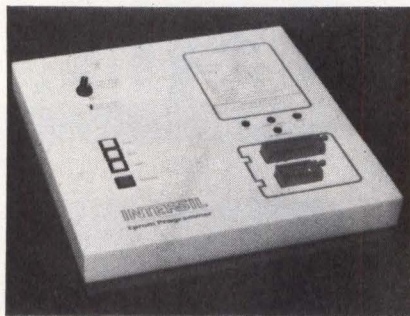
Burroughs

Circle 113 For General Information

Circle 114 For Detailed Specifications

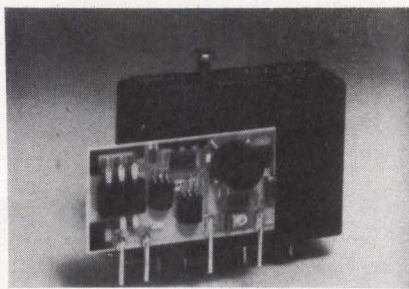
PRODUCTS

MICROPROCESSOR CONTROLLED CMOS EPROM PROGRAMMER



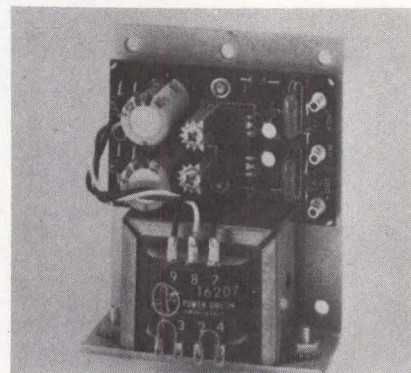
Designed for use with IM87C48/C41 single-chip microcomputers and with IM6653 1k x 4 and IM6654 512 x 8 CMOS EPROMs, the 6920 operates with terminal, as standalone unit, or as peripheral to computer, and features built-in RS-232-C and 20-mA current loop interfaces. Firmware contains 16 editing, loading, listing, and programming commands. Data may be loaded or dumped in ASCII, hex, or BNPF formats, or displayed in any of 15 bases. **Intersil Inc.**, 10710 N Tantau Ave, Cupertino, CA 95014. Circle 221 on Inquiry Card

HYBRID THICK FILM I/O MODULES



Hybrid modules feature components that are laser trimmed to within 0.3%, are resistant to severe vibration and physical and thermal shock, and have 600-V blocking and VDE specs. 8-, 16-, and 24-position boards have plug compatible logic contacts; 4-position version has screw terminal logic connections. All have a barrier strip with screw terminals for load connections, circuitry for pullup resistors, 5-A field replaceable fuses, LED status indicators, and color coded position indicators. **Gordos Arkansas, Inc.**, 1000 N Second St, Rogers, AR 72756. Circle 222 on Inquiry Card

DUAL-OUTPUT DC POWER SUPPLIES



Models HAD12 and 15 provide ± 12 V and ± 15 V at 0.25 A for PMOS, NMOS, CMOS, and linear devices. Std features include 115/230-Vac $\pm 10\%$ ac input capabilities, $\pm 0.10\%$ line and load regulation, and full short circuit and thermal overload protection. Max output ripple is 10 mV pk-pk. Both supplies meet MIL-STD-810B for shock and vibration. Size is 3.75 x 3.0 x 1.4" (9.5 x 7.6 x 3.6 cm); weight is 1 lb (0.45 kg). **Power-One Inc.**, Power One Dr, Camarillo, CA 93010. Circle 223 on Inquiry Card

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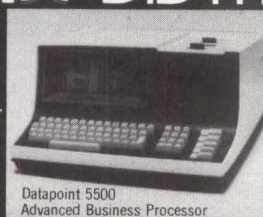


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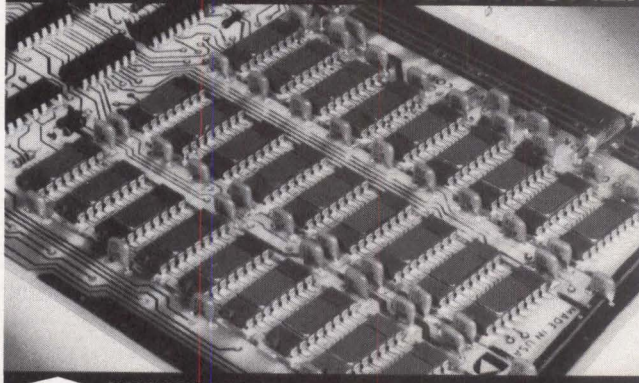
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The 6850 formatter can handle up to four 6253 drives. With an expansion option, it can be expanded to eight drives. An address select switch is also available as an option. In addition, the 6253 features automatic tape loading and Telex's Supr-Lite™ Capstan with the lowest inertia available.

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PRODUCTS

TRI-DENSITY TAPE DRIVE AND FORMATTER CONTROLLER

OEM oriented tri-density model 6253 mag tape drive and model 6850 formatter-controller combine 800-bit/in (315/cm) NRZI, 1600-bit/in (630/cm) PE, and 6250-bit/in (2460/cm) GCR formats in a single system. Any format can be selected manually, or automatically under program control, with specified tape speeds of 45, 75, or 125 in/s (115, 190, 320 cm/s). An optional dual-speed capability allows selection of two different operating densities. **Telex Computer Products**, 6422 E 41st St, Tulsa, OK 74135. Circle 224 on Inquiry Card

8-IN DISC SUBASSEMBLY



Incorporating a rotary actuator, deck plate with an integral spindle, recirculating air filtration system, plus cover, the Mini Fox 8" (20-cm) disc subassembly can mount up to four 200- or 210-mm discs for up to 51.2M bytes of unformatted storage. Operating conditions of the 8.75 x 14.75 x 5.0" (22.2 x 37.5 x 12.7 cm) unit specify 15 to 48 °C temperature and 10 to 80% relative humidity (noncondensing). **SLI Industries**, 21040 Victory Blvd, Woodland Hills, CA 91367. Circle 225 on Inquiry Card

ASYNCHRONOUS SHORT HAUL MODEMS

Extended range, limited distance ALD-XR modem provides a 50% increase in operating range over the std ALD, enabling 1200-bit/s transmission for up to 21 mi (33 km) and 9600-bit/s transmission for up to 6 mi (9.6 km) over the same type of cable. ALD-LP features board mounted varistors that protect its receive circuitry from high voltage surges; ALD-LP/XR is an extended range version of this unit. All provide half- or full-duplex data transmission over 2- or 4-wire facilities. **Prentice Corp**, 795 San Antonio Rd, Palo Alto, CA 94303. Circle 226 on Inquiry Card

REMOTE DATA ENTRY KEYPAD SYSTEM

With 34 data keys and a shift key arranged in a 5 x 7 matrix, system generates 2 codes for each data key depending on status of shift key. Key-top layout is user definable; a software lookup routine will convert to any desired code. Output conforms to RS-423, which is RS-232 compatible but allows transmission up to 2500' (750 m) on 24-gauge twisted pair wire with an RS-232 receiver. Std baud rate is 75; 300-baud is optional. **Gimix Inc**, 1337 W 37th Pl, Chicago, IL 60609. Circle 227 on Inquiry Card

DOUBLE-SIDED 8" DISKETTES

The single-density 742 is compatible with IBM 5110 systems. 7430 diskettes, for double-density applications, are available unformatted or in 256, 512, and 1024 formats for IBM System/34, 5110, and compatible systems. 743-2 versions are compatible with Shugart 850 drives. All have long wearing formulation of oxides and polymers. Low abrasivity protects read/write heads, promoting longer head life. **3M Co, Data Recording Products Div**, PO Box 33600, St Paul, MN 55133. Circle 228 on Inquiry Card

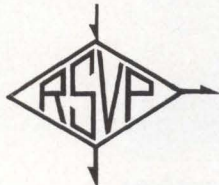
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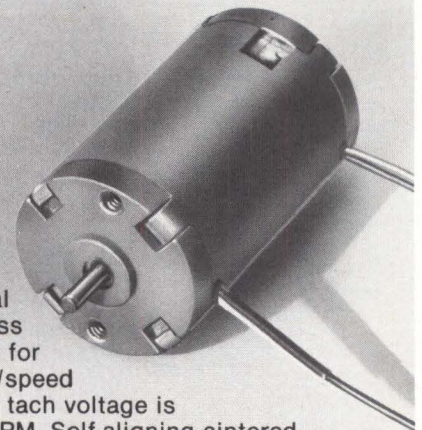
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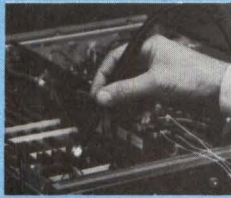
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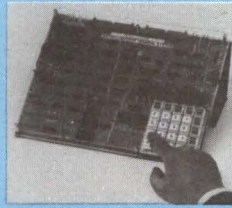
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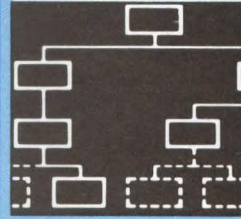
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Course 160—Four Days Microprocessors & Microcomputers



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Course 320—Four Days Structured Programming



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April 29-May 2

Course 330—Four Days PASCAL: The Structured Language

```
10: FUNCTION RFIB(N,LEVEL
11: VAR RF: INTEGER;
12: BEGIN
13: DOTS(LEVEL); WRITE
14: IF N>1 THEN
15:   RF:=RFIB(N-1,LE
16:   ELSE
17:     IF N=1 THEN RF:=
18:     ELSE RF:=0;
19:   RFIB:=RF;
20: DOTS(LEVEL);
21: Writeln('LEAVE, N='
22: END(*REACT*);
```

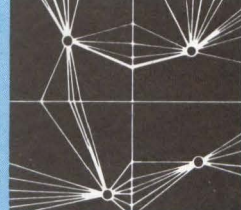
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May 6-9

Course 340—Four Days Engineering Project Mgmt.



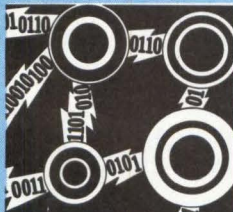
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February 19-22
ATLANTA
February 26-29
SAN DIEGO
March 11-14
BOSTON
April 15-18
WASHINGTON, DC
April 22-25
LOS ANGELES
April 29-May 2
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May 6-9

Course 350—Four Days Distributed Processing Systems



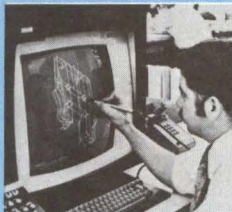
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February 12-15
ATLANTA
March 18-21
WASHINGTON, DC
April 29-May 2

Course 355—Four Days Computer Communication Networks



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May 6-9

Course 365—Four Days Computer Graphics



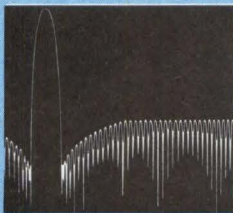
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February 12-15
SAN DIEGO
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April 15-18
SAN FRANCISCO
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April 29-May 2

Course 370—Four Days CAD/CAM



LOS ANGELES
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January 21-24
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February 25-28
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Course 412—Five Days Digital Signal Processing



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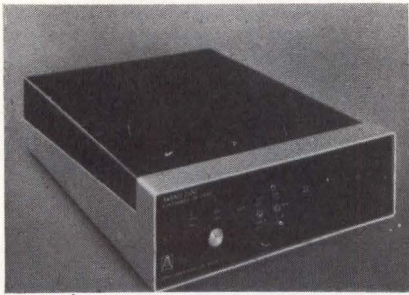
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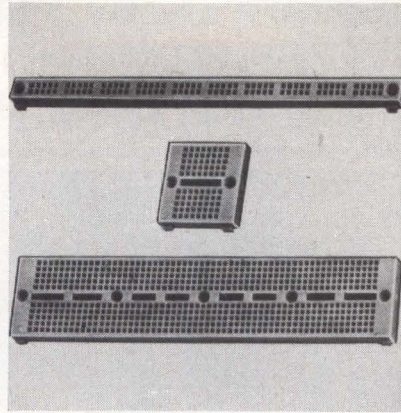
PRODUCTS

SYNCHRONOUS LINE DRIVER



Designed for cost effective inhouse or limited distance data transmission, the 2100 operates over unloaded lines, twisted pairs, or coaxial cables, at distances up to 10 mi (16 km). Output levels and spectrum conform to Bell Pub 43401. Std operating speeds are switch selectable at 2.4k, 4.8k, 9.6k, and 19.2k bits/s. Speeds of 40.8k, 50k, 56k, 224k, and 230.4k bits/s are available with Bell type 301/303 or CCITT V.35 interface. **Avanti Communications Corp**, Box 205, Broadway Station, Newport, RI 02840. Circle 229 on Inquiry Card

CIRCUIT MOUNT BOARDS



Boards feature solderless insertion type sockets on 0.100" (0.254-cm) centers. Each row has 5 common points. Larger boards also have 40-point bus lines; a separate bus strip model is available. All can accept std component leads including DIPs, while interconnections are easily made using std 22 AWG solid wire. Prototype boards range from small modules holding a single IC up to 1020-point panel mounted boards complete with binding posts. All modules are interlocking. **OK Machine and Tool Corp**, 3455 Conner St, Bronx, NY 10475. Circle 230 on Inquiry Card

INTELLIGENT TAPE CODE CONVERTER READER

Model 5030 is a compact unit designed using the Facit 4031 reader mechanism to read perforated tape in any 5-, 6-, 7-, or 8-level code and output in any 5-, 6-, 7-, or 8-level code via its RS-232-C serial interface. Baud rates and operating modes are switch selectable. The microprocessor controller is normally programmed to convert 5-level Baudot (US or CCITT) to 8-level ASCII. Other codes are available on request. An 80-char data buffer is included. **Data Science**, 1189 Oddstad Dr, Redwood City, CA 94063. Circle 231 on Inquiry Card

LINEAR HALL EFFECT SENSOR

Linear output Hall effect transducers (LOHET) are operated by the magnetic field from a permanent magnet or electromagnet, providing linear feedback for analog control systems. A 0.050" (0.127-cm) sq silicon chip mounted on a ceramic base holds Hall effect circuitry and amplifier. 2 models are rated through the -40 to 150 °C range; the third operates from 0 to 85 °C. Ratiometric, semiratiometric, and regulated outputs are available. **Micro Switch, a Honeywell Div**, 11 W Spring St, Freeport, IL 61032. Circle 232 on Inquiry Card

Tarbell Double Density Floppy Disk Interface

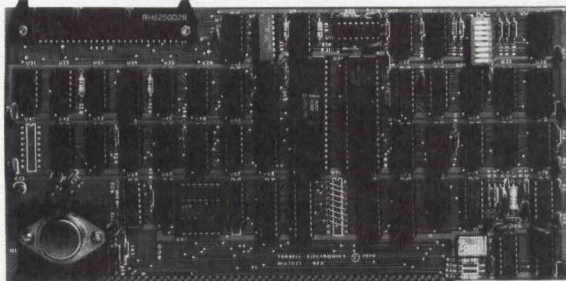
FOR 8" DISK DRIVES

Under Tarbell Double-Density CP/M, single and double density disks may be intermixed. The system automatically determines whether single or double density is in place.

- Software select single or double density.
- Phase-locked-loop and write precompensation for reliable data recovery and storage.
- On-board phantom bootstrap PROM is disabled after bootstrap operation so all 64K memory address space is available to user.
- DMA in single or double density permits multi-user operation.
- Extended addressing provides 8 extra address bits, permitting direct transfer anywhere in a 16 megabyte address range.
- Select up to 4 drives, single or double sided.
- New BIOS for CP/M included on single-density diskette.

Assembled and Tested \$425

CP/M is a reg. trademark of Digital Research.



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BEI Electronics, Inc.

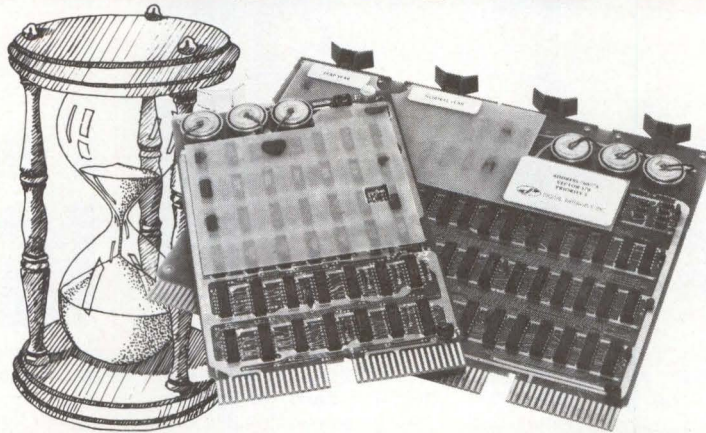
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TCU-150 • \$430

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- Automatic leap year.
- Patches for RSX-11M, RT-11 FB/SJ VO2, VO3 and UNIX.

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- Dual size board.
- Patches for RT-11 SJ/FB VO2, VO3B.

Lockheed SUE

TCU-200 • \$550

- Provides year, month, day, hour, minute, second and milli-second.
- Interval interrupts between 1/1024 seconds and 64 seconds.

Computer Automation (Naked Mini)

TCU-310 • \$385

- Provides year, month, day, hour, minute and second.

Multi-Bus**

TCU-410 • \$325

- Provides year, month, day, hour, minute and second.
- SBC/BLC compatible.

HP 2100

TCU-2100 • \$395

- Correct time restored after power failure.
- Compatible with the HP TBG card.

Serial Clock (RS 232 or 20 mA)

SLC-1 • \$575

- Connects between any terminal and host computer.
- Provides date, time and more!

All Digital Pathways TCUs have on board NICAD batteries to maintain time and date during power down. Timing is provided by a crystal controlled oscillator. Prices are U.S. domestic single piece. Quantity discounts available.

For more information on these products, contact:
Digital Pathways Inc.
4151 Middlefield Road
Palo Alto, CA 94306
Phone: (415) 493-5544

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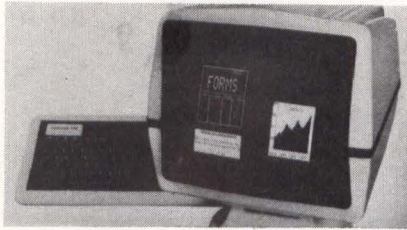


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DIGITAL PATHWAYS

PRODUCTS

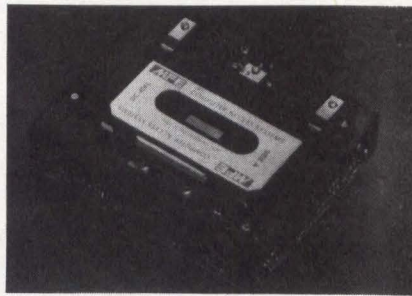
CRT TERMINAL WITH 4-PAGE DISPLAY MEMORY



Microprocessor based display terminal has an 80-char by 24-line screen, and provides forms control, u/lc, up to 19 user programmable function keys, line drawing graphics, and shared printing capabilities. Standard on the Concept 104 are 4 pages of display memory, windowing (multiple sub-screen), and networking between up to 3 communications lines. Other features include tiltable nonglare screen, detached keyboard, and audible key touch. **Human Designed Systems, Inc.**, 3700 Markey St, Philadelphia, PA 19104.

Circle 233 on Inquiry Card

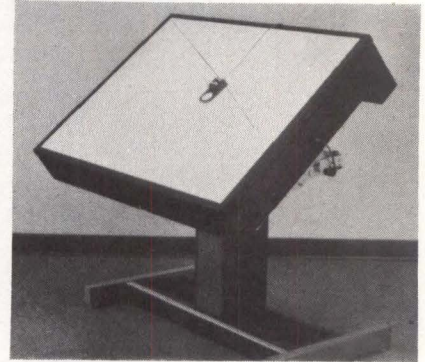
DUAL-TRACE CASSETTE TAPE TRANSPORT



ANSI/ECMA compatible model 452B features a 2-track read-after-write head that permits remote track selection, and eliminates need for operator intervention. After conventionally writing track 1, it rewinds in 30 s, electronically switches tracks, and writes track 2. Either recorded track can be accessed at will. With data transfer rate of 32k bits/s, the unit stores up to 720k formatted char. Offering 15k-h MTBF and 30-min MTTR, transport measures 4.5 x 5.5 x 4" (11.4 x 13.9 x 10.2 cm). **MFE Corp, Digital Products Group**, Keewaydin Dr, Salem, NH 03079.

Circle 234 on Inquiry Card

HIGH INTENSITY BACK-LIT DIGITIZER



Consisting of digitizing surface, interchangeable crosshair or pen cursor, and controller, backlit digitizers and tablets are available in 8 sizes from 11 x 11" (27.9 x 27.9 cm) to 42 x 60" (106 to 152 cm) with resolutions of 0.001 or 0.01" (0.025 or 0.254 mm). Adjustable high intensity light source provides even light distribution over digitizing surface with invisible grid lines. Std fluorescent bulbs, cooling fans, and simple bulb replacement procedure minimize downtime because of bulb failure. **GTCO Corp**, 1055 First St, Rockville, MD 20850.

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LA34 DECwriter IV	1,295	124	67	45
LA120 DECwriter III, KSR	2,295	219	120	80
LA180 DECprinter I, RO	2,095	200	109	74
VT100 CRT DECscope	1,895	181	99	66
VT132 CRT DECscope	2,295	220	119	80
DT80-1 CRT Terminal	1,795	172	93	63
T1745 Portable Terminal	1,875	179	98	66
T1765 Bubble Memory Term. . .	2,795	267	145	98
T1810 RO Printer	1,895	181	99	66
T1820 KSR Printer	2,395	229	125	84
ADM3A CRT Terminal	875	84	46	31
QUME Letter Quality KSR.	3,195	306	166	112
QUME Letter Quality RO.	2,795	268	145	98
HAZELTINE 1410 CRT	895	86	47	32
HAZELTINE 1500 CRT	1,195	115	62	42
HAZELTINE 1552 CRT	1,495	143	78	52
DataProducts 2230	7,900	755	410	277
DATAMATE Mini Floppy	1,750	167	91	61

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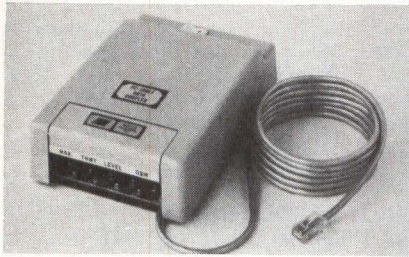
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PC-1001F is an interface unit designed to provide both the data access arrangement and the network control signaling. Prewired in either fixed loss loop (-4 dBm), permissive (-9 dBm), or programmable (-12 to 0 dBm) modes, it isolates customer equipment for protection of telephone plant and personnel from hazardous voltages, and detects incoming ringing signals to permit operation in unattended answering mode. **Precision Components, Inc.**, 1110 W National Ave, Addison, IL 60101.

Circle 236 on Inquiry Card

IEEE 488 DATA GENERATOR INTERFACE



Model 702 IEEE 488 interface allows model 725 data generator to operate as talker or listener in test system controlled by IEEE 488 GPIB compatible computer or calculator. Each symbol on data generator keyboard has been assigned an ASCII character; functions are accessed remotely by sending the appropriate character on the bus. **Moxon Inc.**, 2222 Michelson Dr, Irvine, CA 92715.

Circle 237 on Inquiry Card

5-V MOS MEMORY PROTECTORS

GMP-5 series TransZorb[®] transient voltage suppressors have max surge rating of 215 A for 50 μ s and 70 A for 1 ms. Protectors feature 6.9 V at 10 A max clamping level for impulse waveform of 10 x 1000 μ s. With theoretical response time of 1×10^{-12} s and low series resistance, devices protect VMOS, HMOS, NMOS, and CMOS circuits from unwanted transients while maintaining the circuit voltage level for continuous system operation. **General Semiconductor Industries, Inc.**, 2001 W 10th Place, Tempe, AZ 85281.

Circle 238 on Inquiry Card

RS-232-C AND IEEE 488 BUS CARTRIDGE RECORDERS

Single- or dual-drive digital cartridge recorders provide 2.4M bytes of storage/cartridge using 1600-bit/in (630/cm) PE recording on 0.25" (6.35-mm) mag tape in ANSI/ECMA format. Features include full read-after-write, automatic error handling, 2048-byte buffer and programmable formatting, and search and edit functions. Either RS-232-C or IEEE 488 GPIB interface is available. **Tandberg Data Inc.**, 4060 Morena Blvd, San Diego, CA 92117.

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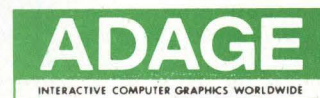
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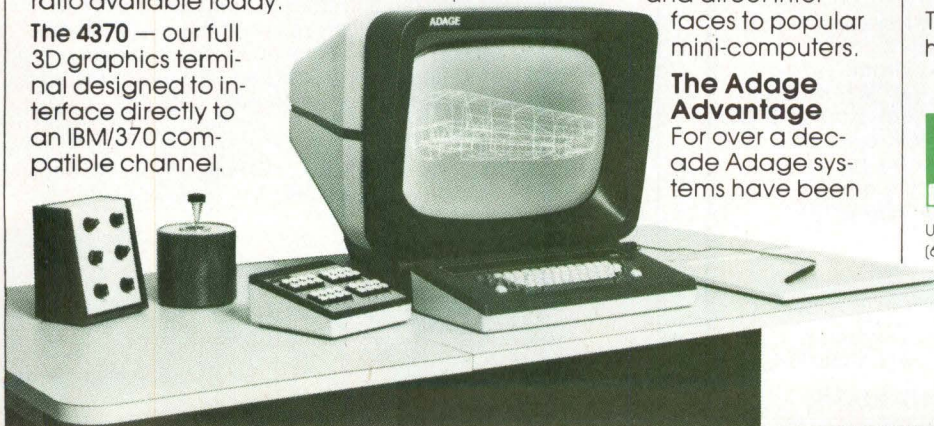
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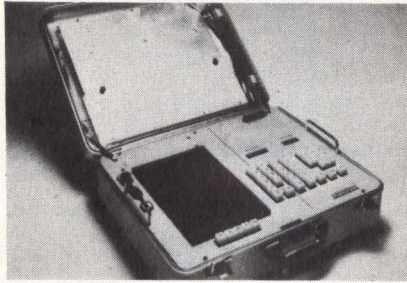
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am Elm, West Germany
Phone: 05353/1089, Telex 095528



CIRCLE 124 ON INQUIRY CARD

PRODUCTS

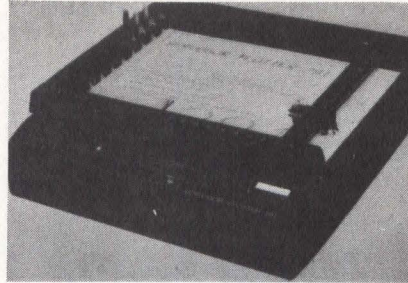
PORTABLE CONTROLLER PROGRAM DIAGNOSTIC UNIT



Reprogramming the MaxiMiser programmable controller in <1.5 min, diagnostic unit uses simple ladder diagram language to program or make changes in existing programs. The portable device can load a complete program into nonvolatile EAROM of the controller with optional cassette memory loader. Error and status indicator allows programming of diagnostics and digital display of system failures. **Cincinnati Milacron, Electronic Systems Div**, Mason Rd & Rt 48, Lebanon, OH 45036.

Circle 240 on Inquiry Card

MICROPROCESSOR CONTROLLED MULTI-PEN PLOTTER



A Z-80 microprocessor controls the automatic pen changing, off-scale data handling, and coordinate transformation for model 281 digital plotter. 8 separate pens may be colored fiber tips or isograph drafting pens. Firmware provides circle interpolation, character plotting in 5 fonts, generation of axes and grids, window plotting, and point digitizing. Plotter uses DIN-A3 std graph paper and interfaces via RS-232-C/V.24, 20-mA, or IEEE-488 bus. **Soltec Corp**, 11684 Pendleton St, Sun Valley, CA 91352.

Circle 241 on Inquiry Card

256k-BYTE SEMICONDUCTOR ADD-IN MEMORY SYSTEMS

DR-123S and DR-125S provide Data General Nova 3 and Eclipse minicomputers, respectively, with 256k bytes of add-in storage. -123S offers 500-ns cycle time, 325-ns access time, parity, and 8-position DIP to select starting address. Single-bit error correction is standard with the -125S that also features 500-ns read cycle, 700-ns write cycle, 350-ns access time, and 8-position DIP to set starting address. **Data-ram Corp**, Princeton-Hightstown Rd, Cranbury, NJ 08512.

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HIGH RESOLUTION RASTER GRAPHICS SYSTEM

With noninterlaced refreshing of the full 1024 scan lines 60 times/s, the GMDS-4000 monitor provides a clear stable display. It offers 1024, 864, or 768 pixels on each of the 1024 lines, with any 2 of these formats selectable under program control. Optional multiple memory planes can provide up to 16 levels of gray, support for 4 monitors, and display of constant background with variable data overlays on multiple monitors. **Image Automation, Inc**, 3350 Scott Blvd, Bldg 22, Santa Clara, CA 95051.

Circle 243 on Inquiry Card

Who's Who in Technology Today

Nuclear Magnetic Resonance • Lasers • Coal Gasification • Polymers
Oceanography • Hydraulics • Superconductors • Pollution Control
Microcomputers • Architecture • Solar Energy • Bubble Memories
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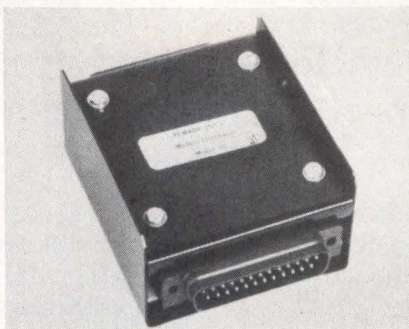
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MOHAWK DATA SCIENCES
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ERROR FREE DATA CARTRIDGE

Certified 100% error free at shipment, model 98200 data cartridge offers reliable data storage for series 9800 desktop computers and 264X series display terminals. Up to 5.4M bits of unformatted data can be stored on the 140' (42 m) of 0.150" (0.38-cm) wide tape with a 1600-bit/in (629/cm) recording density on 2 tracks. Speeds up to 90 in (228 cm)/s are possible. Acceleration rates of up to 2000 in (5080 cm)/s² keep start/stop distances minimum. **Hewlett-Packard Co.**, 1507 Page Mill Rd, Palo Alto, CA 94304. Circle 244 on Inquiry Card

MODEM ELIMINATOR



Model 30 permits direct connection between terminals and computers, eliminating need for short haul modems or acoustic couplers where limited distance is involved. The static device requires no ac or dc voltage. It transposes transmit data and received data and request to send and data carrier detect. Packaged in an aluminum housing measuring 3 x 2.5 x 1.5" (7.6 x 6.4 x 3.8 cm), input/output connections are provided by std 25-pin EIA RS-232-C connectors. **Remark International**, 4 Sycamore Dr, Woodbury, NY 11797.

Circle 245 on Inquiry Card

engineering

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Experience in active and passive electronic warfare systems and strong software and/or hardware background necessary.

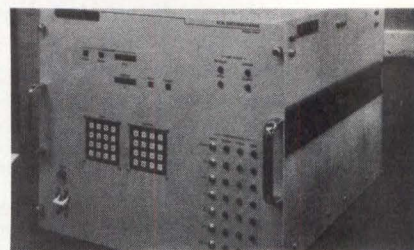
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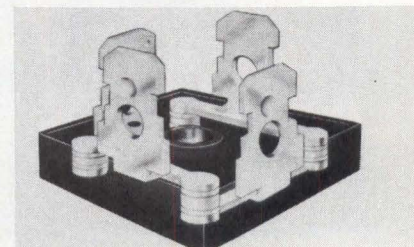
STORED PROGRAM FORMAT SYNCHRONIZER



Model 1126B is a microprocessor based unit featuring both formatting and data preprocessing capability. Data format features include data rates to 5M bits/s, conventional and adaptive sequential ratio probability synchronization strategy, up to 5 independent subframe synchronizers, multipoint output, and programmable RAM. Online data processing functions include data compression capabilities and computation. **Aydin Monitor Systems**, 401 Commerce Dr, Fort Washington, PA 19034. Circle 246 on Inquiry Card

PLASTIC CASE SILICON RECTIFIERS


Silicon rectifier bridges feature miniature size, quick connect terminals, and epoxy filled plastic cases rather than larger, more expensive metal cases. The single-phase, full wave bridge measures 0.8" (2.0 cm) sq x 0.3" (0.76 cm) high. Terminals are 0.250" (0.635-cm) quick connect for heat sink and chassis mounting. Ratings are 8 A at 50, 100, 200, 400, 600, and 800 V. Surge is 150 A as a result of large size junctions. **Electronic Devices, Inc.**, 21 Gray Oaks Ave, Yonkers, NY 10710.



Circle 247 on Inquiry Card



THE ULTIMATE INTERFACE



BELDEN EIA RS-232-C CABLE ASSEMBLIES

It's fast. Simple. Reliable. Accurate. In fact, it's the ultimate interface for your data terminal and communications equipment employing serial binary data exchange.

Belden's new 25 conductor molded cable assemblies are designed and built to meet EIA standard RS-232-C and types A through M standard interfaces.

These are cables you can count on. Belden's rugged 8459 cable (UL style number 2576) is used in these assemblies. This cable also passes the FR-1 vertical flame test and is the preferred cable for critical interfaces. And positive pin-to-pin mating using subminiature "D" type plug connectors means no mix-up.

Complete cable assemblies are now in stock in four standard lengths of up to 70' (21m). Bulk cable is available in put-ups of up to 1000'. Custom designed assemblies are also available on special request. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 319-966-6661. Out West contact our Regional Sales Office in Irvine, CA 714-833-7700.

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DC TO AC STATIC POWER INVERTERS

With capacities from 700 to 10k VA, inverters deliver ac power to sensitive loads. The devices operate from an input of 48 or 125 Vdc and produce a clean 120-V sinewave output at 60 Hz (50 Hz available). Output voltage regulation is held within $\pm 3\%$ of nom for full load and line change, and output frequency to within $\pm 0.5\%$. Output is fully protected against overloads and short circuit conditions. **Deltec Corp.**, 980 Buenos Ave, San Diego, CA 92110.

Circle 248 on Inquiry Card

REMOTE CLUSTERED CRT TERMINAL SYSTEM

Series 300 Interactive Display System utilizes Softprint microprocessor controlled display terminals which support std 24-line by 80-col formats and expanded 27-line by 132-col format. The system will emulate an IBM 3270 Information Display System and can be attached to a host computer by a BSC link. It will support user operational activities in cluster configurations of up to 32 devices. **Lee Data Corp.**, 5700 Green Circle Dr, Minnetonka, MN 55343.

Circle 249 on Inquiry Card

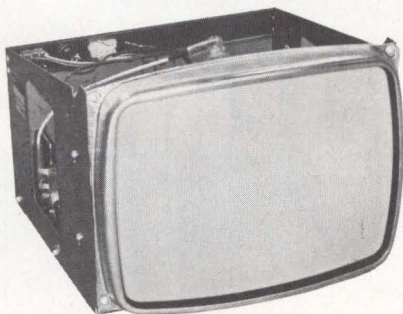
ANTI-ALIASING FILTER WITH IEEE 488/1978 INTERFACE



Incorporating the IEEE Std 488/1978 interface, 1-Hz to 100-kHz dual low pass filter provides AH1 (acceptor handshake), L1 (basic listener with listen only), and DT1 (device trigger) functions. Each channel provides a roll-off rate of better than 115 dB/octave; in cascade the 2 channels offer better than 230 dB/octave. Other specs are ± 0.25 -dB ripple and >80 -dB stop-band attenuation. Cutoff frequency range of the filter is adjustable from 1 Hz to 110 kHz. **Rockland Systems Corp.**, Rockleigh Industrial Pk, Rockleigh, NJ 07647.

Circle 250 on Inquiry Card

Announcing a new source for CRT data displays.



BHD-1200

An all-new line of data display monitors is now being manufactured by Bell & Howell for OEM applications.

Available in 5-, 7-, 9-, and 12-inch screen sizes, these units can be mechanically and electrically fitted to standard display terminals without modification, but can also be manufactured to meet custom specifications.

Wide range of options—hundreds of possible configurations

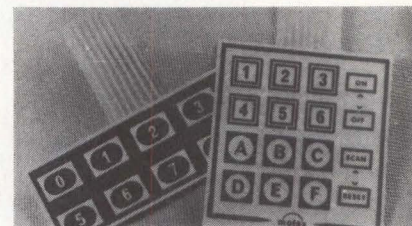
- 15.75 KHz, 16.2 KHz, 18.6 KHz or other scan rates
- Dynamic focus — standard
- EIA P4, P31, P39, or P42 phosphors
- Kits and metal chassis available for all screen sizes

For more information about these new data display monitors, contact Bell & Howell Display Devices, 4000 Birch Street, Newport Beach, CA 92660, (714) 752-7602.

DISPLAY DEVICES



MEMBRANE SWITCH SYSTEM



Construction of the 10900 membrane switch is based on deposition of conductive polymer ink to provide silver contacts and interconnections on 2 sections of thin, flexible polyester substrate. A spacer layer sandwiched between the sections before sealing has openings to create the contact gap, which decreases at actuation until contact surfaces meet to close circuit. Switches are custom designed to meet exact needs for contact spacing, aesthetics, mounting, and termination. **Molex Inc.**, 2222 Wellington Ct, Lisle, IL 60532.

Circle 251 on Inquiry Card

FIBER OPTIC COMMUNICATIONS LED

Microlensed LED is supplied in std hermetically sealed TO-46 package and is designed to couple to single fiber or fiber bundle through use of std connectors. IRE-161 has typ output of 2.0 mW into a 0.5 numerical aperture (30° half angle) when driven at 100 mA dc; at 70°C output is typ 1.5 mW. Second harmonic distortion is <40 dB. Typ rise and fall time is 10 ns. Wavelengths from 790 to 880 nm are available. **Laser Diode Laboratories, Inc.**, 1130 Somerset St, New Brunswick, NJ 08901.

Circle 252 on Inquiry Card

The Power Paradox:

The AC power your computer needs in order to operate is also a major cause of computer error, malfunction and damage.

The computers that control your operations (and therefore your profits) are designed to operate from a clean, steady supply of ac power.

This ac power *must* be kept within manufacturer-specified tolerances in order for the computers to operate properly and safely.

In fact, the U.S. Department of Commerce states that "if a computer's voltage exceeds 120% [of the rated voltage] for a duration as short as 1 to 10 milliseconds, the computer will make errors."¹ Unfortunately, interruptions and disturbances of this nature are commonplace occurrences within most computer facilities.

A comprehensive study of power line disturbances which affect sensitive computerized equipment was conducted by two IBM researchers. They concluded that such disturbances occur on an

average of 128 times each month.² For users of computer-based equipment, power disturbances can and do create a variety of costly problems.

Effects upon data processing computers.

When these power disturbances occur in your data processing center they can cause entry errors, program changes or loss, head crash, data loss, the generation of false or garbled data, the need to rerun programs, and computer downtime.

Effects upon computerized process control equipment.

Process control equipment is also vulnerable to power disturbances. Common problems created by these

disturbances include improper batch termination and even program changes. The program changes can result in the repetition of process errors and in downtime while equipment is being reprogrammed.

Effects upon energy management systems.

Most energy management systems use small computers to make energy-saving decisions, but their effectiveness can be offset by these same disturbances. Program changes and errors may prevent useful operation of these systems as energy savers.

Thus, the computers your company depends on to reduce operating costs actually may be increasing them.

Topaz power peripherals can protect all of your computers.

Topaz can provide the power peripherals specifically designed to keep your company's data processing, process control and energy management computers from making costly power-related errors.

And if you manufacture computers or computerized equipment, Topaz peripherals can make your product more reliable as well as reduce the requirements for needless service calls.

Immediate delivery and guaranteed solutions to power problems have made Topaz the leading computer power peripheral company in the world.

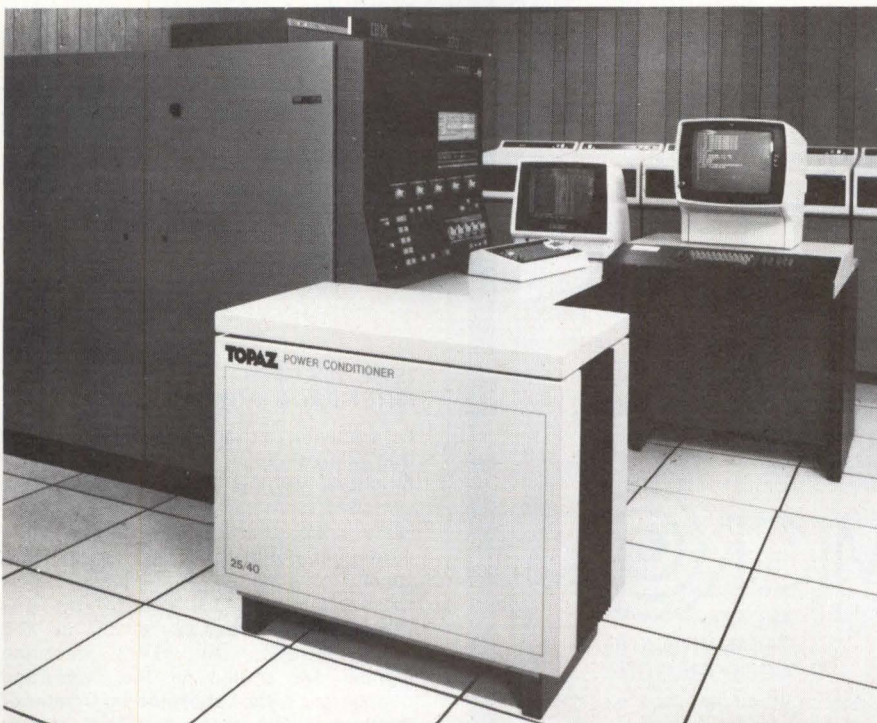
For more information about Topaz and its products:

1. Tear out this ad and mail it to us along with your business card; or

2. Call us:

TOPAZ
ELECTRONICS

3855 Ruffin Road, San Diego, CA 92123
(714) 279-0831 — TWX (910) 335-1526

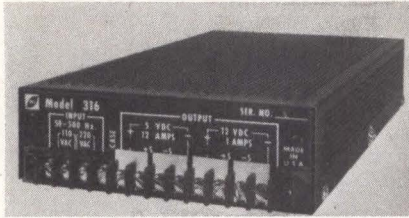


Topaz peripherals solve the power paradox by conditioning normal ac power for your computer and computer-based equipment.

CIRCLE 130 ON INQUIRY CARD

PRODUCTS

DUAL SWITCHING POWER SUPPLIES



Model 314 produces 5 V at 10 A and 12 V at 2 A; model 315 is rated at 5 V, 8 A and 12 V, 3 A. Model 316 outputs 5 V, 12 A and 12 V, 1 A. All come in a low profile package measuring 1.75 x 5.28 x 10.75" (4.45 x 13.4 x 27.3 cm), and have short circuit and current limiting protection. Overvoltage protection is std on all 5-V outputs. **RO Associates, Inc.**, 246 Caspian Dr, Sunnyvale, CA 94086. Circle 253 on Inquiry Card

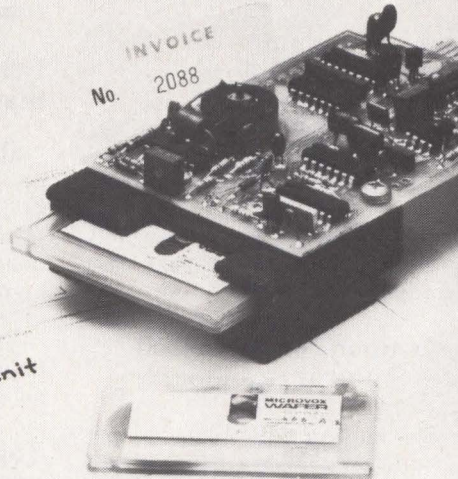
SMALL UNINTERRUPTIBLE POWER SYSTEM

Model UPS-102-1B, a 1-kVA rated UPS, consists of rectifier/charger, solid state inverter, and optional static or electromechanical bypass switch. Line power is rectified to dc, power is provided to a pulse width modulated transistor inverter, full charge is maintained on a nom 72-Vdc external battery, and the inverter reconverts the dc to 120 Vac 60 Hz. The unit is packaged in a 7" (17.8-cm) high rack-mounted chassis and weighs 70 lb (32 kg). Op temp range is 0 to 40 °C. **Elgar Corp.**, 8225 Mercury Ct, San Diego, CA 92111. Circle 254 on Inquiry Card

RO COMMUNICATIONS CORPORATION
80 BACON STREET
WALTHAM, MASSACHUSETTS 02154

Computer Tech. Inc.
190 Western Ave.
Albany, N.Y.

1000 @ \$69.00 per unit



A digital tape transport system for the price of an audio system

For just \$69.00 (in O.E.M. quantities) Micro's Read/Write Tape Transport System gives you size and performance features an audio system can't match.

You get higher read/write speeds—3 ips vs. audio speeds of 1.87 ips; higher tape densities—3200 fci vs. audio densities of 400 fci; and electronically, rather than mechanically, controlled starts and stops.

Just 6" in length, weighing less than 6 ounces, and housed in die cast aluminum, the Read/Write System can be conveniently designed into any microprocessor.

Ideal for program loading and data logging, the system features a 4800 baud transfer rate, up to 120K bytes of storage, TTL and CMOS

compatibility, and a start/stop time of 30/40 milliseconds.

RELIABILITY? The system's only moving part is the capstan motor. No springs. No clutches. No gears to wear out. That's why our performance rivals systems 3 times our cost.

Micro's Read/Write System . . . Digital Performance at Audio Prices.



MICRO COMMUNICATIONS CORPORATION

80 Bacon Street, Waltham, Ma. 02154
(617) 899-8111 • TWX 710-324-7600

CIRCLE 131 ON INQUIRY CARD

A BUCKEYE INTERNATIONAL COMPANY



COMMUNICATIONS PROTOCOL CONVERSION PROCESSOR



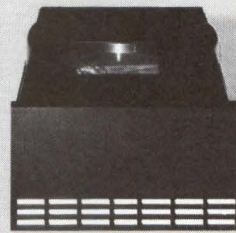
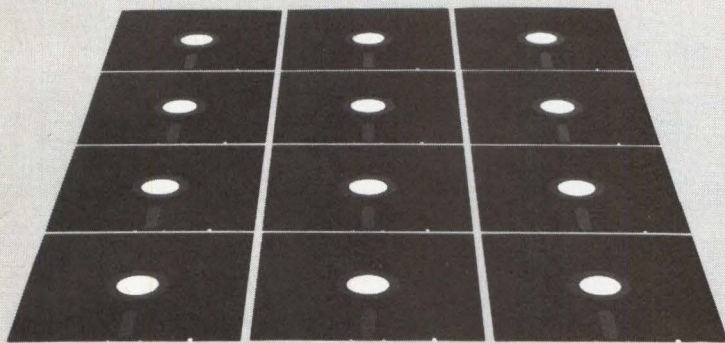
Connecting asynchronous or bisync equipment to mainframes or peripherals using Burroughs Poll/Select protocol, CA12-SIU/BPS also permits IBM or other mainframe users to use Burroughs equipment with minimal software modification. Operating transparent to the user, unit performs protocol conversion, data conversion, and function transformation, and provides up to 30 ports and up to 32k of buffer memory in the 16.7 x 16.9 x 5.25" (42.4 x 42.9 x 13.33-cm) package. **Industrial Computer Controls, Inc.**, 196 Broadway, Cambridge, MA 02139. Circle 255 on Inquiry Card

IEEE-488 GPIB INTERFACE MODULE

A software programmable I/O card that implements talker and listener functions of the IEEE-488 GPIB, the uP GPI-1 features selectable interrupts, onboard address recognition, and automatic handling of handshake protocol to simplify implementation of those functions in control systems where another device serves as the bus controller. All GPIB interface signals are routed to the card-edge connector. **Wyle Laboratories/Computer Products**, 3200 Magruder Blvd, Hampton, VA 23666.

Circle 256 on Inquiry Card

OLD. NEW.



Meet the Mini Wini™ The new 8" fixed disk drive that stores 20 megabytes.

It's the lowest-cost way of getting 20 megabytes in an 8" floppy slot. And with Winchester-type technology, to boot.

So you can expand the on-line capacity of your present desk-top system without having to redesign one bit of your present chassis.

Interfacing?

It's a snap. The Mini-Wini (alias the PCC D8000 fixed disk) has a microprocessor-controlled interface, featuring a bidirectional command/status bus and serial data transfer. It's easier and simpler to design the CPU interface.

And maybe best of all, it's made by Pertec Computer Corporation. At PCC, we don't just innovate. We have the production capacity to supply those innovative products when we say we will. Which is reassuring.

The PCC Mini-Wini. Small size. Big capacity. Call us for details.

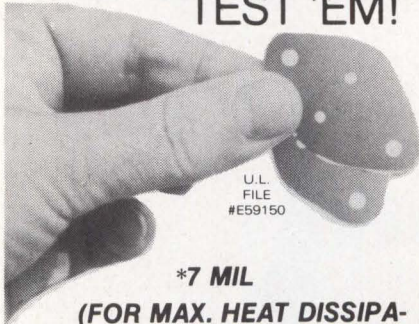
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PERTEC COMPUTER CORPORATION
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For further information, call toll-free 800-528-6050, Ext. 1323.

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HEAT SINK
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Since 1973, Bergquist has helped overcome heat-sink problems with "SIL-PADS". Eliminate messy grease and fragile mica or plastic film by using this exclusive development.

"SIL-PADS 400" are thin, tough layers of thermally-conductive silicone-rubber and fiberglass (laminated). Cut-through, tearing, breaking problems are gone. Assembly time is reduced; no solder bath contamination; consistent heat transfer.

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Minneapolis, MN 55435
Phone (612) 835-2322
TWX 910-576-2423

PRODUCTS

DATA ACQUISITION SYSTEM FOR MINICOMPUTERS

Interfacing with series V77 minicomputers, F2963 consists of 1 master chassis and up to 7 daisy-chained expansion chassis, each accommodating up to 16 plug-in modules for a total of 512 analog channels/chassis. In an 8-chassis system, up to 128 modules of any combination may be used to provide 4000 separate input channels of data. Available analog/digital components include simultaneous sample/hold, signal processors, D-A and A-D converters, and various multiplexers. **Sperry Univac**, PO Box 500, Blue Bell, PA 19424.

Circle 257 on Inquiry Card

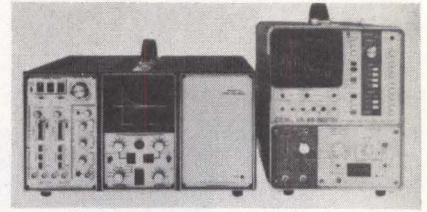
LOGIC ANALYSIS SYSTEM



Logic state, logic timing, and waveform recording functions of the System 5000 operate interactively as a total data system, or as independent analysis units. Interactive or linked triggering between analysis elements, and interfaces for RS-232, IEEE-488, and floppy discs are provided. Keyboard of portable system folds up to protect 9" (23-cm) CRT during transport and features positive action keys. Menu keys guide user through operation. **Paratronics, Inc.**, 122 Charcot Ave, San Jose, CA 95131.

Circle 258 on Inquiry Card

HIGH SPEED FREQUENCY ANALYSIS SYSTEMS



Models 4402A and 4404A combine a 2090 digital oscilloscope with the 446 Mini-Ubiquitous[®] FFT computing spectrum analyzer. 1- or 2-channel systems provide sampling rates to 20 MHz. The oscilloscope digitizes and stores up to 4096 input time samples; any 1024-sample block can be transferred to the spectrum analyzer. Input sensitivity of the scope is variable from ± 100 mV to ± 40 V. Sweep time for 1024 samples is variable from 51.2 μ s to 341 min. Amplitude accuracy is $\pm 0.5\%$ of full scale. **Nicolet Scientific Corp.**, 245 Livingston St, Northvale, NJ 07647.

Circle 259 on Inquiry Card

ENCAPSULATED MERCURY FILM RELAY

W1728 features bounce free performance and long reliability, and operates in any mounting position. Pins are arranged on std 1 x 0.2" (2.5 x 0.5-cm) centers. Self-healing contacts provide reliability. At loads ranging from 2 to 1 x 10⁻¹² A, reliability exceeding 2G MCBF may be expected at a 90% confidence level. Contact resistance over the life of the relay varies by no more than 0.02 Ω . **Fifth Dimension, Inc.**, 707 Alexander Rd, Princeton, NJ 08540.

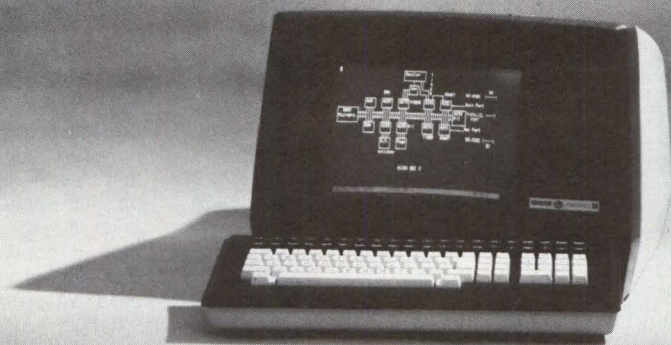
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Monstrous IDC problems solved.

See page 59



BEEHIVE INTERNATIONAL



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Micro **B**, Model DM1S EMULATION

VT52*, PRISM*, DASHER*, Beehive B150

Micro **B**, Model DM2S EDITING

Editing Capability, Expanded Keyboard with 16 Function Keys, Block Send

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8K RAM Multi-Page Capability, Parallel Printer Interface, Beehive B300 Emulator

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FLORIDA Altamonte Springs (305) 830-4666 **ILLINOIS** Arlington Heights (312) 593-1565

MASSACHUSETTS Woburn (617) 933-0202 **NEW YORK** New York (212) 682-2760 **OHIO** Centerville (513) 435-7073

PENNSYLVANIA Plymouth Meeting (215) 825-0243 **UTAH** Salt Lake City (801) 355-6000

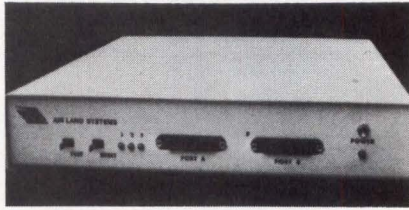
VIRGINIA Falls Church (703) 356-5133

EUROPE Amsterdam, The Netherlands Phone 020-451522

BEEHIVE INTERNATIONAL

Box 25668 • 4910 Amelia Earhart Drive • Salt Lake City, Utah 84125

PROTOCOL CONVERTER



The 8085 based PCU effects data conversion between 2 different communications protocols. With 2 serial I/O ports, the converter allows most RS-232 compatible devices to be put on-line. Each port under program control functions either synchronously or asynchronously at program selected baud rates. The converter features up to 8k of buffer storage and up to 8k of program storage. **Air Land Systems**, 2820 Dorr Ave, Fairfax, VA 22031. Circle 261 on Inquiry Card

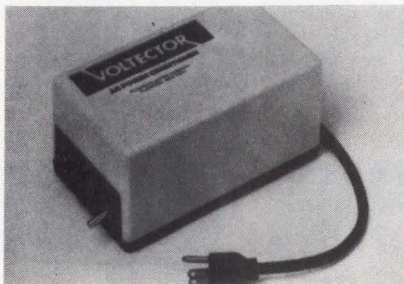
SUPER BRIGHT LED AND MOUNTING SOCKET

LED interchangeability and low profile packages are offered by packaging together model 180 screw-in super bright red, amber, or green LEDs, with clear or diffused lenses, and PS 200 series mounting sockets. This provides a lower profile than common T-1 $\frac{3}{4}$ LEDs plus a socket with built-in resistor for selection of operating voltage. The LED protrudes about 0.100" (2.54 mm) from the front of the mounting panel and the assembly fits into a 0.250" (6.35-mm) panel cutout. **Data Display Products**, 303 N Oak St, Inglewood, CA 90301. Circle 262 on Inquiry Card

RECEIVE ONLY LINE PRINTER

Capable of operating at speeds of 300 to 1500 lines/min, the Mark V RO 3780 printer simulates IBM 3780 line discipline. Std features are logic for determining type of text, space de-compression, multiple record capability, horizontal tabs, and vertical forms control including overprint. Double-hinged yoke assembly with monorail font guidance provides accurate print alignment. **Hetra**, 1151 S Eddie Allen Rd, Melbourne, FL 32901. Circle 263 on Inquiry Card

MINICOMPUTER SYSTEM AC POWER CONDITIONERS



W-model Voltector[®] series 5 remove electrical disturbances from power line to protect sensitive electronic equipment from noisy and unstable ac power. Reducing high voltage surges to safe levels and removing low voltage transients and various noise spectra, units handle up to 120 J of transient energy. They are effective in both common mode and transverse, or differential mode forms of interference. Models are rated 1, 2, 3, 5, 10, 15, and 20 A. **Pilgrim Electric Co**, 29 Cain Dr, Plainview, NY 11803. Circle 264 on Inquiry Card

6-FT WIDE DRUM PLOTTER

Continuous roll drum paper provides 6' (1.83-m) wide plotting capability with max drawing speed of 30 in (76 cm)/s. Model 1065 has resolution of 0.0005" (0.0127 mm) and linear pen actuation, and uses translucent, rag, vellum, or mylar papers, and pressurized ballpoint, liquid ink, nylon tip, and liquid ball type pens. Other features include Y-axis limit switches, paper supply monitor, plot time meter and speed control, return to last plotted position, and self-test diagnostics. **California Computer Products, Inc**, 2411 W La Palma Ave, Anaheim, CA 92801. Circle 265 on Inquiry Card

DATA COMMUNICATIONS LINE SWITCH

CLS-2VF connects both digital and VF sides of 2 modems to a single telephone line, and allows interfaces to be switched between the line and terminal or CPU. Switching of 4 isolated lines is provided between 2 separate and 1 common 6-position modular female jack. 20 commonly used EIA interface signals are also switched between Line A and Line B connectors. The device employs status indicator buttons to give a clear indication of which line is selected. **Electrodata, Inc**, PO Box 46130, Bedford, OH 44146.



Circle 266 on Inquiry Card

WINCHESTER DISC SYSTEM FOR DEC MICROCOMPUTERS

Winchester technology for the DFC LSI-11 series is available with the WINC-01 disc system. Two PCBs comprise the system: a microprocessor based formatter/controller mounted with a Shugart SA-4008 Winchester drive and a dual-width Q-Bus interface card that inserts directly into the CPU backplane. The system can accommodate up to three 20M-byte 14" (36-cm) Winchester drives, for a total sealed media capacity of 60M bytes. **Advanced Electronics Design, Inc**, 440 Potrero Ave, Sunnyvale, CA 94086. Circle 267 on Inquiry Card

**Veteran
tough guy meets
his match.**

See page 15

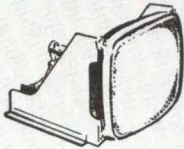
NEW! LOW COST CRT DISPLAY MODULE

MOST-REQUESTED FEATURES

Motorola's new 12-inch CRT display module offers low unit cost while maintaining the features most requested in volume OEM applications. Features such as 800-line resolution, excellent linearity and geometry, video response to 15 MHz—features that contribute to the module's capability of providing sharp, clean characters in a full 80 x 24 format. TTL-compatible direct drive operation and single 12V dc input requirement further simplify your design considerations.

CHASSIS OR KIT

The new module is available with sheet metal chassis as Model M3570, or with-



out the chassis in "kit" form as Model M3970, pictured below. Model M3970 offers superior economy—and has no metal boundaries to inhibit your own layout.

PRICED TO HELP HOLD DOWN YOUR PRODUCT COSTS

In addition to the already low unit price, maximum cost savings can be achieved by ordering either model packaged in bulk (subject to minimum purchase volume and shipping restrictions). These cost savings at the component level can have a noticeable impact on the price of your final product. Without compromising performance!

CALL TODAY

Call today for more information about the new, low-cost display from Motorola ■ Santa Clara, CA (408) 988-3422 ■ Tustin, CA (714) 838-5621 ■ West Chicago, IL (312) 231-4400 ■ Richardson, TX (214) 231-9901 ■ Windham, NH (603) 898-5921 ■ Shrewsbury, NJ (201) 544-9541 ■ Baltimore, MD (301) 821-0062 ■ Overseas and Canada call West Chicago, IL (312) 231-4400 ■ TWX: 910-230-3117

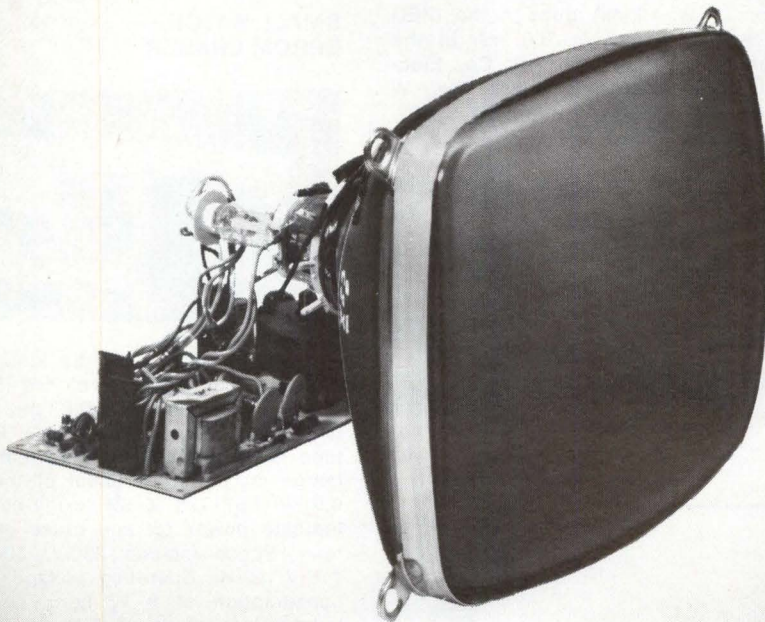


MOTOROLA INC.

Display Systems

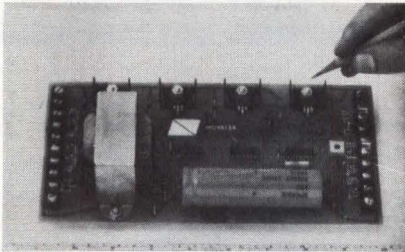
1155 Harvester Rd.
West Chicago, IL 60185

CIRCLE 134 ON INQUIRY CARD



PRODUCTS

LOW SPEED STEPPER MOTOR CONTROLLER



Eliminating heat generating resistors with an onboard 5-V power supply, compact controller for 5-V motors integrates power supply, oscillator, and translator in a single glass epoxy PC board. Screw terminal connections, integral standoffs, and external wiring schematic are provided. Compatible with 5-V, 4-phase steppers up to 1.6 A/phase and 200 steps/s, the 4.5 x 9 (11.4 x 22.9-cm) unit provides TTL or switch closure inputs that permit direct connection to computer or non-computer outputs. **Novatek, Inc.**, 79 R Terrace Hall Ave, Burlington, MA 01803.

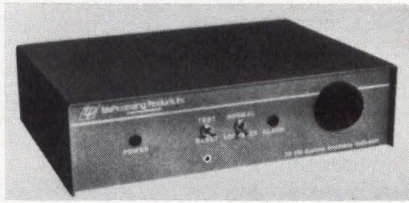
Circle 268 on Inquiry Card

DISC EMULATOR

Microprocessor based single-board controller, the PM-DC1100, emulates DEC[®] RP11 and provides compatibility with system software for RP11 and RP02/03 subsystems. One controller can handle two 80M- or 300M-byte storage modules, or with the addition of a multidrive interface chassis, up to 8 storage modules. Features include 3-sector data buffering, consecutive sector transfers, and transfers across track boundaries. **Plessey Peripheral Systems**, 17466 Daimler, Irvine, CA 92714.

Circle 269 on Inquiry Card

COMMUNICATIONS SYSTEM AVAILABLE INDICATOR



TP-210 provides both visual and audible indication of a communications failure between remote data terminal equipment and host system. The unit monitors the RS-232-C interface at the data terminal, and responds to either a failure to raise "request to send" or to loss of data carrier. Alarm condition activates audible signal, lights LED on front panel, and switches ac power to 115-Vac outlet on rear of unit. Indicator operates in either synchronous or asynchronous applications. **TeleProcessing Products, Inc.**, 4565 E Industrial St, Bldg 7K, Simi Valley, CA 93063.

Circle 270 on Inquiry Card

LOGIC TO POWER OPTO-ISOLATOR INTERFACE

H11G, a liquid epitaxial GaAs IRED optically coupled to a Darlington connected phototransistor, an extension of the MT2L line, operates in the -55 to 100 °C temp range. BV_{CEO} is up to 100 V with 2500-V rms isolation capability. Other features include high current transfer ratio and low degradation LEDs. 10 mA through the IRED will switch a load of 100 mA in the Darlington. **General Electric Co, Electronic Components Business Div**, W Genesee St, Box 14, Auburn, NY 13021.

Circle 271 on Inquiry Card

QUAD-LED LOGIC STATUS INDICATORS

Mounting GaAsP red LEDs in a 4-element array provides easier PCB mounting and wave soldering. Advantages include positive seating and spacing of light source to the PCB surface. Polarity is identified to assure error-free installation. Model 555-4001 has no integral current limiting resistor, -4003 is a current limited 5-V/6-mA unit, and -4007 is a current limited 5-V/3-mA unit. All can be driven directly from TTL. **Dialight, a North American Philips Co**, 203 Harrison Pl, Brooklyn, NY 11237.

Circle 272 on Inquiry Card

ACOUSTIC DATA COUPLER/MODEM

Model 247 is FCC approved for direct connection via modular jack or DAA, and may be used as acoustic coupler. All types of line connections are switch selectable and require no internal modifications. Compatible with Bell 103/113 type modems, the unit transmits and receives full duplex asynchronous data at speeds to 450 bits/s. It provides a dual-terminal interface for either EIA RS-232 or 20-mA current loop terminals. **Anderson Jacobson, Inc.**, 521 Charcot Ave, San Jose, CA 95131.

Circle 273 on Inquiry Card

SMALL BATCH EPROM ERASER

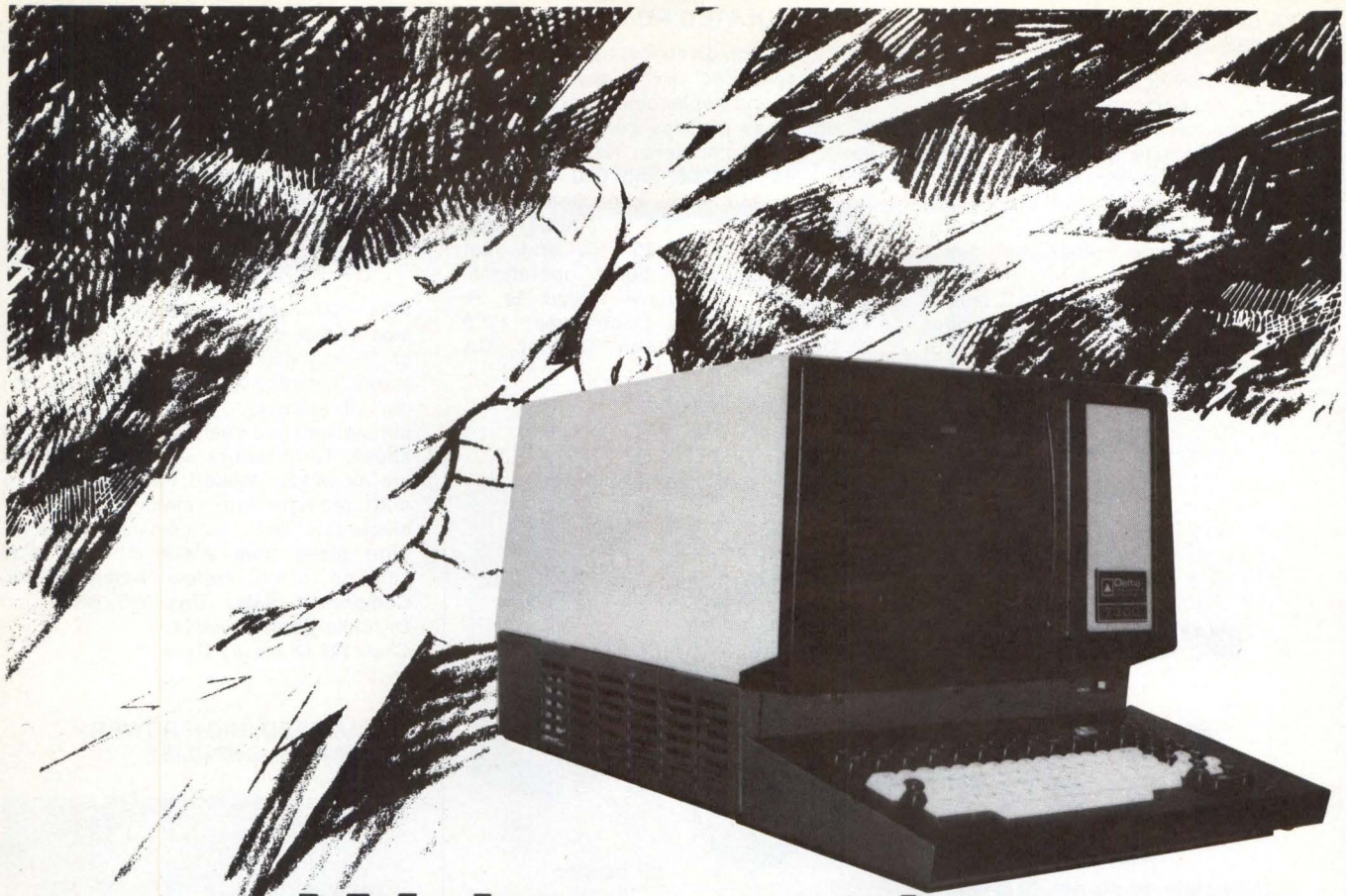


Up to 15 EPROMs can be loaded into the front sliding tray of the SE 15. Safety interlock disables the lamps when the tray is removed. Erasure time is presettable up to 40 min. Neon lamps on the front panel of the 11 x 9.5 x 4.5" (28 x 24 x 11-cm) unit indicate power on and erase in progress. Specs include 230-V, 50-Hz or 115-V, 60-Hz operating voltage, power consumption of 8 W nom, operating temperature range of 0 to 65 °C, and UV source wavelength 253 to 257 nm. **Stag Systems**, 2465 E Bayshore Rd, Suite 329, Palo Alto, CA 94303.

Circle 274 on Inquiry Card

Man's best friend is his _____.

(See page 114 for the answer.)



We've got the **POWER**

for OEM's and large systems users

The new DELTA 7000 Series 16-bit microcomputer display terminals... More power to you for data preparation, text editing and distributed processing applications

The DELTA 7000 Series of multifunctional terminals is a unique combination of hardware and software designed to meet sophisticated applications in large computer systems. This combination offers you a choice of display terminals with truly outstanding performance features, including:

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- DYNAMIC FONT GENERATION enables you to design special symbols, or modify existing characters from the keyboard and have them immediately available
- EXTENDED CHARACTER SETS provide display of up to four 248-character sets which can be PROM resident or RAM loaded
- LARGE TEXT MEMORY from 6K up to 36K characters adds applications flexibility and terminal power to meet your needs

Put the power at your fingertips with a DELTA 7000 Series video display terminal. Zing us a line, or call for more information, literature or applications assistance.

See us at Comdex '79, Booth 924

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Data Systems
Corporation

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Cornwells Heights, PA 19020
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Service in over 150 locations in the U.S., and 14 European countries and Canada.

DATA COMMUNICATIONS INTERCONNECT ADAPTER

Black Box RS-499 adapter performs all necessary adjustments for interconnection between RS-499 and -232. It includes 37-pin male and 25-pin female connector and provides 2 side access holes to facilitate optional connection of additional external cabling. Installation is made either by direct mounting on rear of terminal or by cable connection. 2 male and 2 female screwlocks are provided. **Expander Inc.**, 400 Sainte Claire Plaza, Upper St Clair, PA 15241.

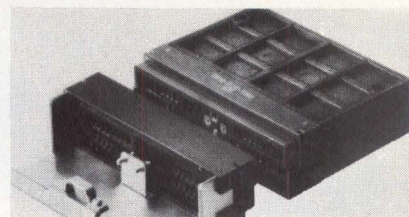
Circle 275 on Inquiry Card

ENCAPSULATED RC NETWORKS

Quick connect/disconnect pins on a line of encapsulated RC networks ease assembly and replacement in such applications as process control, machine tools, and computers. Networks have std ratings of 200 and 600 Vdc and 125 and 250 Vac, capacitance and resistance tolerances to $\pm 10\%$, temp range of -40 to 85°C , and min life expectancy of 200M operations. Heavy duty units have ratings to 2k Vdc and 480 Vac. **Electrocube**, 1710 S Del Mar Ave, San Gabriel, CA 91776.

Circle 276 on Inquiry Card

MULTI-CABLE CONNECTORS



FCN 120 cable connectors have ratings of 6 A max and contact resistance of 10 m Ω max. Housings are of heat stable, fire resistant, and self-extinguishing UL-approved glass filled polycarbonate and are resistive to mechanical abuse. Gold-over-nickel finish contacts are positively locked into the housing and provide firm mating with max electrical and mechanical integrity. Wire sizes from AWG #24 to #32 can be used. **Fujitsu America, Inc.**, Component Sales Div, 910 Sherwood Dr, Lake Bluff, IL 60044.

Circle 277 on Inquiry Card

CIQ Series

9" and 12" CRT DISPLAY MONITORS with a Horizontal Rate of 15.72 KHz

Compatible with
TV120 or TV90
Priced Below the
Competition
Built-in Quality,
Performance,
Dependability



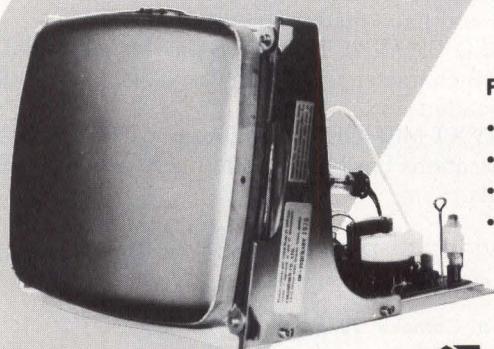
Kit Version

The low-cost CIQ-9 and CIQ-12 CRT Display Monitors with a horizontal rate of 15.72 KHz provide data equipment manufacturers with sharp, highly reliable image presentation.

Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

The completely new design of the compact integrated PCB utilizes the latest semiconductor and other components, providing a dependable performance level never before possible.

Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.



Chassis Version

FEATURES

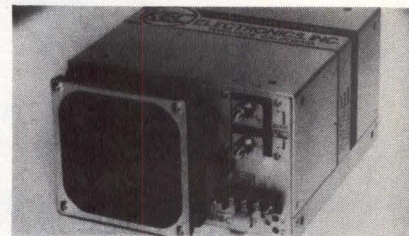
- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
- Squareness of Picture

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REGULATED, HIGH POWER SWITCHING SUPPLIES



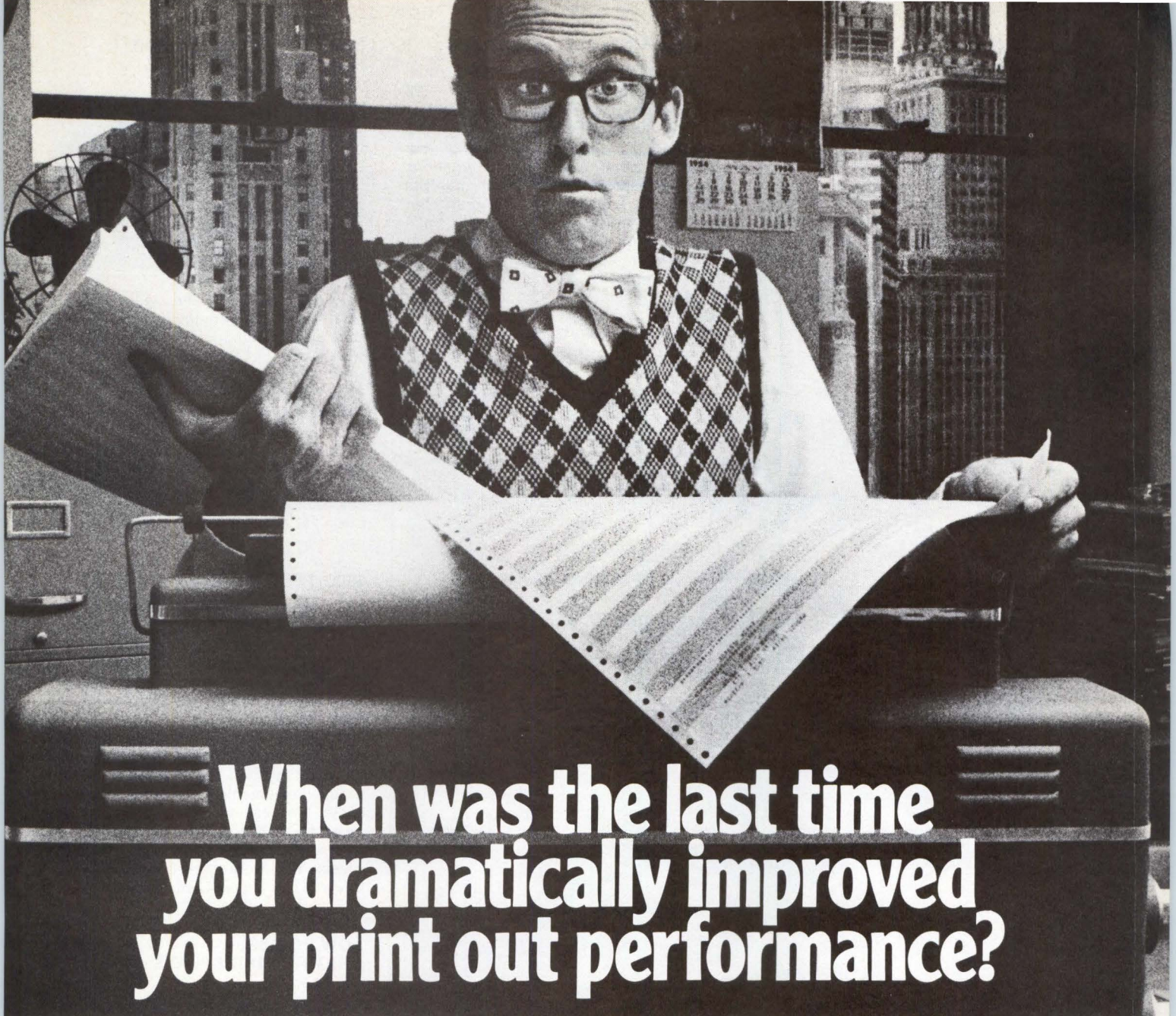
Tight line (0.1% max) and load (0.15% max) regulation are features of the 750-W SE series. Requiring 115- and 230-Vac inputs, units have brownout protection ranges of 97 to 127 and 194 to 254 Vac—15 to 10% of center voltages. Overvoltage and overload protection and integral thermal cut-off are included. 7.75 x 4.93 x 9.70" (19.67 x 12.52 x 24.64-cm) units provide 5 Vdc at 150 A, 12 Vdc at 64 A, and 240 Vdc at 32 A outputs. Efficiencies are 80% at 5 V to 85% at 24 V. **KEC Electronics, Inc.**, 21535 Hawthorne Blvd, Torrance, CA 90503.

Circle 278 on Inquiry Card

LINE PRINTER CONTROLLER

Controller handles any printer up to 500k bytes/s. The half-board plugs directly into any available I/O slot in either 16- or 32-bit Perkin-Elmer/Interdata computers. The module is fully software compatible with both OS/16 and OS/32, and host-supplied diagnostics. Pin compatible Interdata cables are provided which allow the host supplied Centronics or Data Printer interface to be directly replaced by the controller module. Switches are used to select attributes. **Macro-link**, 1740-E South Anaheim Blvd, Anaheim, CA 92805.

Circle 279 on Inquiry Card

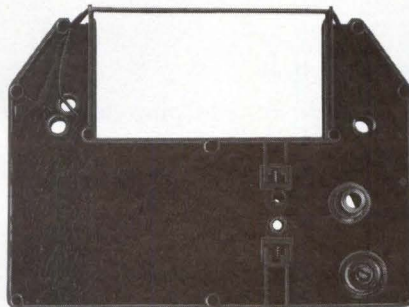


When was the last time you dramatically improved your print out performance?

Today's measure of a printer's performance goes beyond line speed and purchase price. A revolutionary Porelon reinking system now adds a new dimension to print out performance. It will dramatically increase the printing life of the ribbon in your impact printer and substantially reduce character cost.

Porelon's unique ribbon reinking system automatically begins to reink the impact

printer's ribbon only after re-inking becomes necessary. This is made possible through a patented delayed engage-



ment device. The printing life of the ribbon is maximized and printouts continue to be crisp and clean for a longer period of time.

Find out how simple it is to add this performance feature to your impact printers. Your competition may already be considering it. Call (615) 432-4134. Or write Porelon, Inc., Cookeville, Tennessee, 38501, for further information.

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YOUR LAST IMPRESSION IS WHERE WE BEGIN

MIL-STD-1553A DATA BUS INTERFACE

Model 3760 aircraft multiplex data bus interface for AN/UJK-19 and Eclipse computers operates in the 3 information modes specified in MIL-STD-1553A: system controller to remote terminal (RT), RT to system controller, and RT to RT. The unit consists of 2 printed wiring assemblies that interface any Rolm CPU to a pair of MIL-STD-1553A data buses through the CPU's I/O bus. **ROLM Corp.**, 4900 Old Ironsides Dr, Santa Clara, CA 95050.

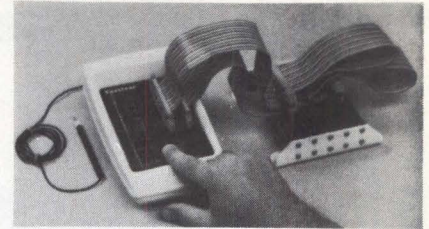
Circle 280 on Inquiry Card

DUAL-PRINTER CONTROLLER

The dual format of the S1403/dual controller maximizes use of an IBM 1403 printer by alternately interfacing the printer to any 2 IBM or non-IBM computers, and providing the interface, control, and power functions necessary to interface with non-IBM computers. A memory in the controller stores the universal char set for each type train or chain to be used, making the printer software compatible with both computers. **Spur Products Corp.**, 1904 Centinela Ave, Los Angeles, CA 90025.

Circle 281 on Inquiry Card

CONTINUITY TESTER FOR FLAT CABLE ASSEMBLY



Interface module and adapters of F-500 portable continuity tester enable quick testing of flat cable assemblies, with LED displays identifying shorts or opens. Unit tests 14- and 16-pin DIP, D series, and 20- to 50-contact PC edge connectors, plus 10- to 50-contact sockets. Probe allows testing of connectors of other than flat cable. Portable unit operates on 9-V battery. **Fasttest**, 921 Loraine Ave, Los Altos, CA 94022.

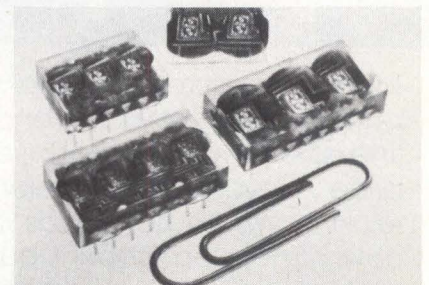
Circle 282 on Inquiry Card

6800 TEST PACKAGE OPTION

Fully programmable test package option allows MX-17 test system users to test and evaluate device operating modes and instruction sequences of all 6800 devices in less time than required by other systems. The 6800 test package includes a device programming unit, manual device board, and a test program for the device to be tested. Although written to MC68B00 specs, easily implemented software changes allow the test program to accommodate MC6800, MC68A00, and other specs. **Adar Associates, Inc.**, 154 Middlesex Tpk, Burlington, MA 01803.

Circle 283 on Inquiry Card

LOW POWER, BRIGHT LED DISPLAYS



Intended as alternatives to LCDs for self-illuminating use, DL-440M, -430M, -330M, and -340M LED digit displays draw <math>< 1.0 \text{ mW/segment}</math>. Displays with 0.150" (3.81-mm) high digits are available in 2- and 3-digit end stackable models; 0.110" (2.794-mm) high models have 3 and 4 digits. Displays are encapsulated and hermetically sealed in plastic packages with high impact plastic lenses. Typ luminance for all 4 models is 1.5 mcd at 5 mA/segment. **Litronix**, 19000 Homestead Rd, Cupertino, CA 95014.

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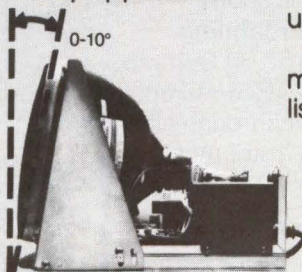
There's a bright new face in 12" data monitors.

If you've got a need for a 12" CRT monitor, Sanyo has a model that will fill it.

For cost-sensitive applications, choose the 5000 series. You get your choice of AC or DC power, P4 or P31 phosphors, and separate or composite video and sync inputs. 15 MHz bandwidth and standard 15.75 kHz scan rate provide excellent resolution and easy application.

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With either series, you get a



compact, rugged steel chassis with adjustable CRT tiltback to fit virtually any enclosure design. You also get adjustable scan size, plus remote brightness control capability. Single-PCB construction and one-connector hookup save time in assembly, testing, and maintenance. And Sanyo's many years of manufacturing field-proven CCTV monitors, and our unparalleled QC assure long, trouble-free service.

For all the facts on these exciting new open-chassis monitors, contact your local Sanyo sales representative listed below.



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1200 W. Artesia Blvd., Compton, CA 90220 (213) 537-5830

Contact your nearest Sanyo rep:

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BOSTON: Piper Associates (617) 449-1144 **CHICAGO:** George Petit Company, Inc. (312) 261-0342 **DALLAS:** The Crockett Sales Co. (214) 748-8209 **DENVER:** Mile-High Marketing (303) 457-2058
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CIRCLE 139 ON INQUIRY CARD

Successive Approximation ADCs

Data sheet gives block and timing diagrams, detailed specs, a sample circuit, and applications comments for 400- and 1000-ns monolithic ADCs. **TRW LSI Products**, Redondo Beach, Calif.
Circle 300 on Inquiry Card

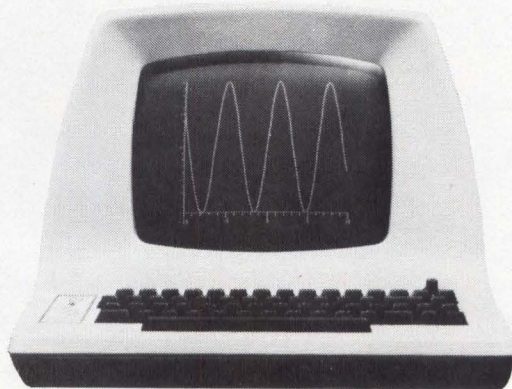
PC Mountable Switches

Featuring tiny toggle switches, slides, pushbuttons, and rotary switches for PCB mounting, catalog furnishes dimensional drawings and specs. **Alco Electronic Products, Inc.**, North Andover, Mass.
Circle 301 on Inquiry Card

Apple Computer Software

More than 100 business, demonstration, game, education, language, and utility programs for the Apple microcomputer are described in catalog along with hardware and accessories. **Rainbow Computing Inc.**, Northridge, Calif.
Circle 302 on Inquiry Card

Smart move



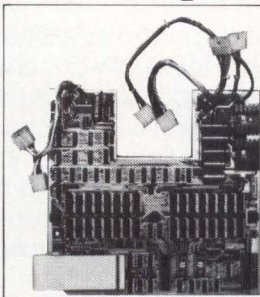
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Retro-Graphics transforms the ordinary Dumb Terminal into a sophisticated graphics terminal. Check these features:

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Mounts inside the Lear Siegler ADM-3A. Installation requires no



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Bridge Rectifiers

Selection chart lists specs including avg rectifier current, op temp, peak current surge, and voltage ratings for 1.5- to 30-A rectifiers; flip side provides dimensional drawings. **Electronic Devices, Inc.**, Yonkers, NY.
Circle 303 on Inquiry Card

Small Business System Evaluation

Brochure provides checklist of questions and discussion of considerations in evaluating vendor, software, hardware, total system, and financial aspects of a small business system. **Data General Corp.**, Westboro, Mass.
Circle 304 on Inquiry Card

Enhanced BASIC

COBOL, APL, and FORTRAN features of HP Enhanced BASIC including multicharacter identifiers, array operations, and function subprograms are outlined in brochure. **Hewlett-Packard Co.**, Palo Alto, Calif.
Circle 305 on Inquiry Card

Alternatives for Speed And Direction Control

Application notes present alternatives to standard speed, direction, and braking control for permanent magnet and shunt wound drive systems. **Bodine Electric Co.**, Chicago, Ill.
Circle 306 on Inquiry Card

2400-Bit/s Modem

Photos of front panels with explanations of indicators and switches illustrate capabilities of MX 2400 modem line in brochure which also details options, models, and features of the line. **Codex Corp.**, Mansfield, Mass.
Circle 307 on Inquiry Card



The Hughes Microprocessor Development System... an important addition to the 1800 CMOS microprocessor family

Hughes again brings its high-technology leadership and high reliability performance to the microprocessor users with a powerful development system for 1802 Microprocessor Products.

The **Hughes Microprocessor Development System (HMDS)** solves the problem of developing software and hardware for 1802 Microprocessor based designs. The HMDS contains an easy-to-use assembler plus editor and monitor software and in-circuit-debug for real time hardware development. High-level languages, PROM programmers and support of additional industry standard Microprocessors are just some of the available options.

Hughes offers a complete line of Microprocessor related devices including Hughes new Liquid Crystal Display Drivers (HLCD 0437 and HLCD 0438) along with those listed in the table.

Other advanced products will be announced soon. For further information on the growing Hughes product line call or write: Gary Des Rochers, Hughes Semiconductor Products, 500 Superior Avenue, Newport Beach, CA 92663, (714) 759-2907 (800) 854-3515. In Europe: Hughes Microelectronics Ltd., Clive House, 12-18 Queens Road, Weybridge, Surrey KT13 9XD, England. Telephone 932-47262.

THE 1800 MICROPROCESSOR FAMILY

(Available Now)

Number	Function
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HCMP 1822	256 X 4 RAM
HCMP 1824	32 X 8 RAM
HCMP 1831/2	512 X 8 ROM
HCMP 1833/4	1024 X 8 ROM
HCMP 1852	I/O Adapter
HCMP 1853	3 to 8 Decoder
HCMP 1854	UART
HCMP 1856/7	Bus Buffer/ Separator
HCMP 1858/9	Memory Latch/ Decoder
HCMP 1861	TV Interface

HUGHES

HUGHES AIRCRAFT COMPANY
SOLID STATE PRODUCTS DIVISION

CIRCLE 141 ON INQUIRY CARD

Linear Circuit Tester

Hardware and software components and test options for the Series Five linear IC tester are outlined in catalog, complete with block and circuit diagrams, photos, and sample programs. **Lorlin Industries, Inc.**, Danbury, Conn.
Circle 308 on Inquiry Card

Portable Cable Assembly Tester

Brochure details features and operating modes of AutoScan high speed portable fault finder that visually identifies fault as short, miswire, or open and provides pin number of defective wire. **Muirhead-Addison**, Mountainside, N.J.
Circle 309 on Inquiry Card

General Purpose Switches

Catalogs present specs and dimensions for basic, diecast limit, and thumbwheel switches, and also proximity switches. **Omron Electronics, Inc.**, Schaumburg, Ill.
Circle 310 on Inquiry Card

LED Assemblies

Curves in application brief plot typical forward current vs forward voltage for LED assemblies to aid in selection of LED within required voltage and current ranges. **Data Display Products**, Inglewood, Calif.
Circle 311 on Inquiry Card

Variable Reluctance Stepping Motors

Electrical specs, diagrams, and photos are included in catalog for commercial permanent magnet and variable reluctance stepping motors. **Clifton Precision, Litton Systems, Inc.**, Clifton Heights, Pa.
Circle 312 on Inquiry Card

Static RAM Family

Organization, speed, power consumption and power supply requirements, and package and pinout information for 2k, 4k, and 8k static RAMs are presented in data sheet. **EMM/SEMI, Inc.**, Tempe, Ariz.
Circle 313 on Inquiry Card

Statistical Multiplexer

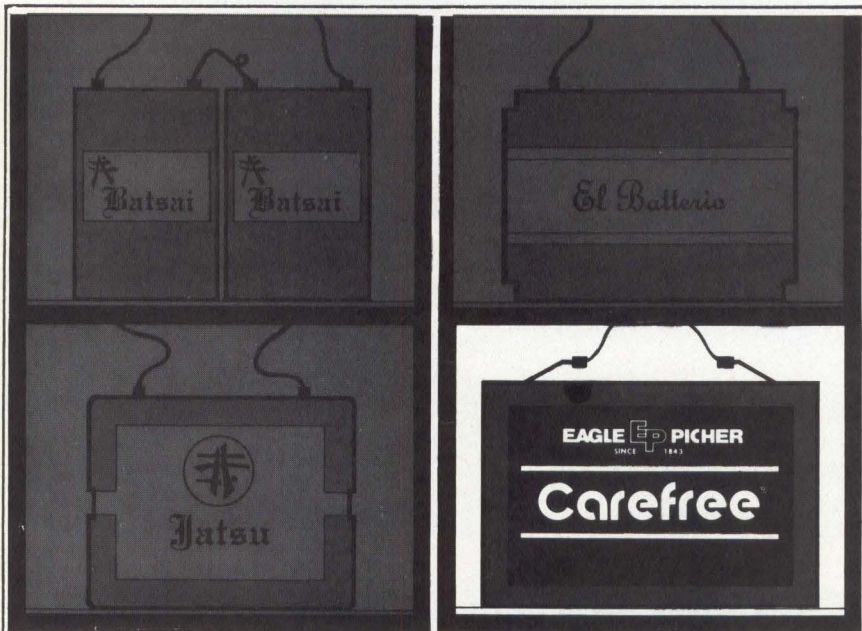
Features of 200% efficient statistical time division multiplexer including peak loading tolerance, error protection, and flow control are detailed in data sheet. **General DataComm Industries, Inc.**, Danbury, Conn.
Circle 314 on Inquiry Card

Electronics Enclosures

Constructed of ABS material with internal mounting bosses, rails, and vertical card guides, enclosures illustrated in catalog are offered as both kits and production models. **PacTec Div of LaFrance Corp.**, Philadelphia, Pa.
Circle 315 on Inquiry Card

POWER BASIC

Product Reference Guide for POWER BASIC exemplifies statements, commands, and functions, and describes evaluation, development, and configurable versions of the language. **Texas Instruments, Inc.**, Houston, Tex.
Circle 316 on Inquiry Card



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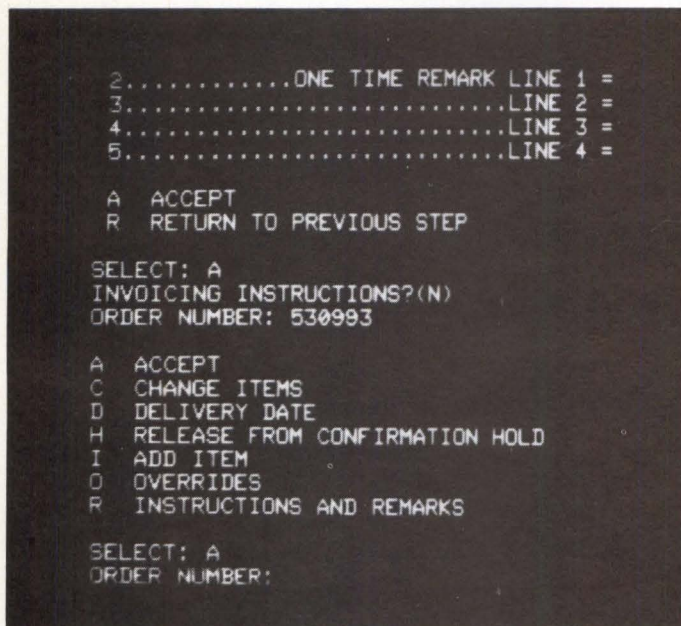
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To see or not to see? That is the question.



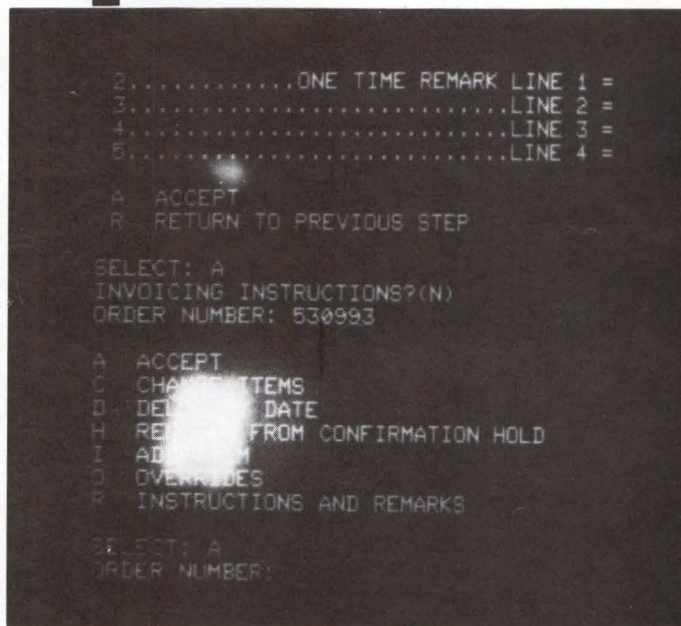
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And Polaroid has the answer: circular polarizer contrast-enhancement filters let you see your display under a variety of lighting conditions.

Circular polarizers kill reflections from CRT's by acting as a light trap. Ambient light can go through the circular polarizer, but after it is reflected from the tube face, it can't get out again. And circular polarizers can suppress up to 99% of reflected room light. They are far more effective than absorption-type filters for improving contrast.

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Display without polarizer.

We sell circular polarizers and offer technical assistance worldwide. For a free sample, just fill out and mail the coupon below. Or call Dick Adams *collect* at 617-577-3315. He'll recommend the contrast-enhancing filter that best meets your needs.

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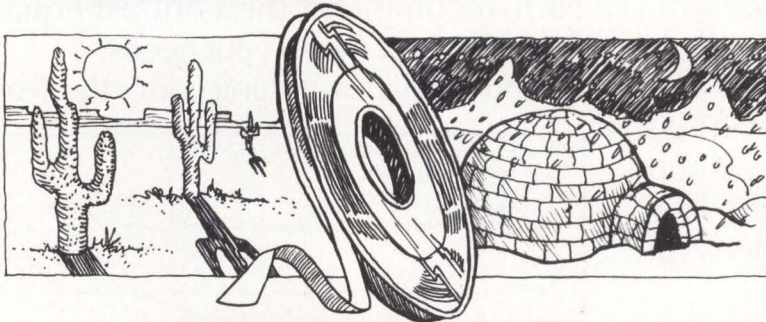
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CIRCLE 188 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

MATERIALS AND FORMS	PAGE		PAGE		PAGE
INKING MATERIALS AND SYSTEMS		LED Displays		Optoisolators	
Printer Reinking Systems		Litronix	232	General Electric/Electronic	
Porelon	231	Displays		Components Business	228
INSULATING MATERIALS AND FORMS		Beckman IDO	22	POWER SOURCES, REGULATORS,	
Plastic Wire Insulation		Noritake Electronics	95	AND PROTECTORS	
Pennwalt	12, 13	SOCKET BOARDS AND CARDS		Power Equipment	
Heat Sink Insulators		Socket Boards		Topaz Electronics	221
Bergquist	224	OK Machine & Tool	212	Power Supplies	
MAGNETIC MATERIALS AND FORMS		SOCKETS		Motorola Subsystem Products	54, 55
CRT Yokes and Flybacks		Sockets		Percom Data	98
Triad-Utrad	206	Cambridge Thermionic	140	Switching Power Supplies	
OPTICAL MATERIALS AND FORMS		WIRE AND CABLE		Deltron	205
Optical Filters		(See also Connectors)		KEC Electronics	230
Panelgraphic	208	Wire		Power-One	175, 204
Polaroid	237	OK Machine & Tool	8	RO Associates	222
		COMPONENTS AND ASSEMBLIES		Uninterruptible Power Systems	
HARDWARE		CAPACITIVE COMPONENTS		Elgar	222
CONNECTORS AND		Capacitors		Voltage Transformers	
INTERCONNECTION SYSTEMS		Union Carbide/Components	208	Basler Electric	160
Connectors		MOTORS; ROTATIVE COMPONENTS		Power Conditioners	
AMP	121	Motors		Pilgrim Electric	226
PCB Connectors		Pittman/Penn Engineering &		Power Inverters	
Technical Wire Products	204	Manufacturing	17	Deltec	220
Multicable Connectors		TRW Globe Motors	58	Batteries	
Fujitsu America/Component Sales	230	Servo Motors		Eagle-Picher Industries/Commercial	
Interconnection Components		Barber-Colman/Motor	210	Products	236
Spectra-Strip	15, 59, 114	Stepper Motor Controllers		General Electric Battery	92, 93
Flat Cable/Connector Systems		Novatek	228	Battery Backup Boards	
Robinson-Nugent	84, 85	PHOTODEVICES; PHOTODEVICE		Data General	198
Cable Assemblies		ASSEMBLIES		RELAYS	
Belden/Electronic	219	LEDs		Mercury Relays	
INDICATORS; READOUTS		Data Display Products	226	Fifth Dimension	224
DIGITAL DISPLAYS; LAMPS		Fiber Optic Communications LEDs		RESISTIVE COMPONENTS	
LED Indicators		Laser Diode Laboratories	220	RC Networks	
Diallight/North American Philips	228			Electrocube	230

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For further information contact
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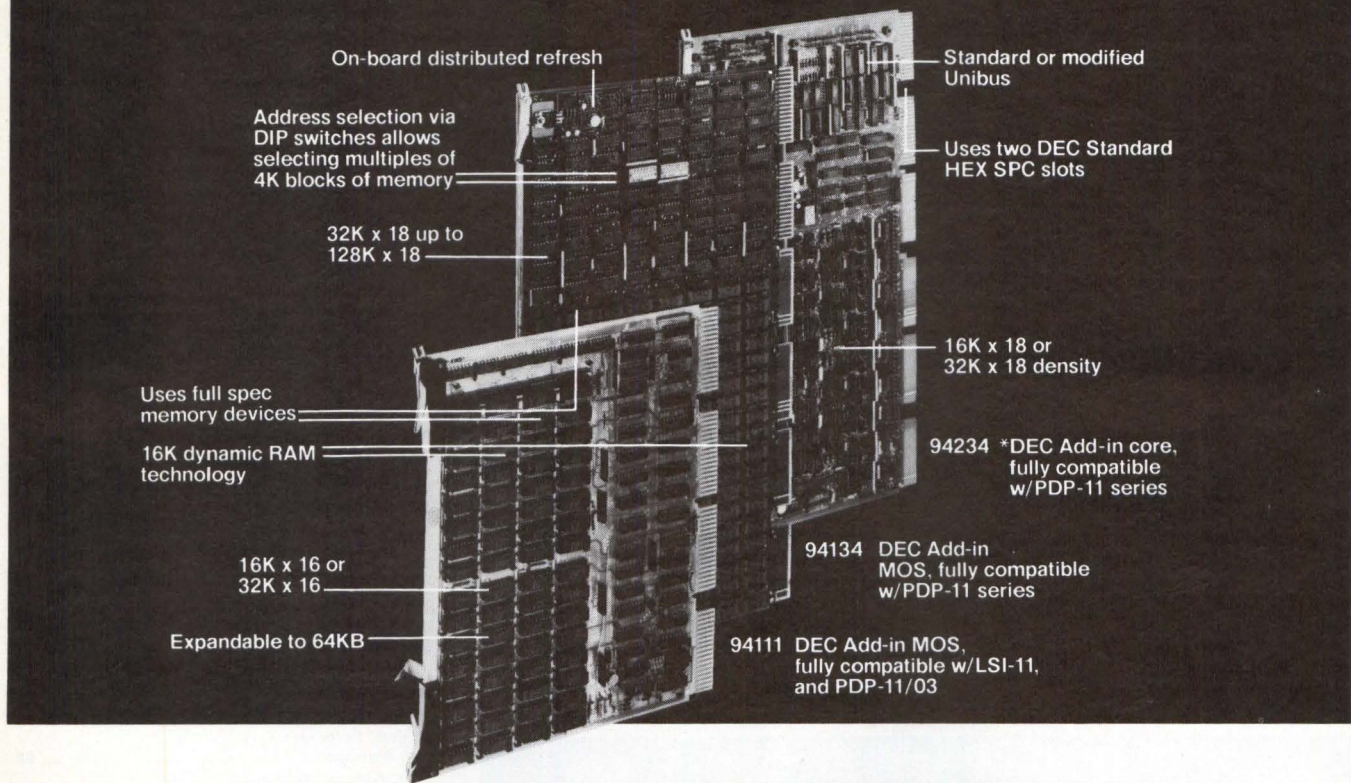
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CIRCUITS	
ARITHMETIC CIRCUITS	
Arithmetic Processor Chips	
Advanced Micro Devices	132, 133, 182
CIRCUIT CARDS AND MODULES	
Logic Modules	
Mostek	160
DIGITAL AND INTERFACE INTEGRATED CIRCUITS	
LSI ICs	
American Micro Systems	48, 49
Fairchild Semiconductor Products	20, 21
MOS ICs	
Solitron Devices	240
Memory ICs	
Fairchild Semiconductor Products	28, 29
RAM Controller Chips	
Intel	9
4k Static RAMs	
Electronic Arrays	188
Intersil	208
FIFO Memory ICs	
Monolithic Memories	188
Single-Chip A-D Microcomputers	
Intel	193, 194
Microprocessors	
American Microsystems	154

Add-on quality, Add-in quality with OEM memory from Control Data.

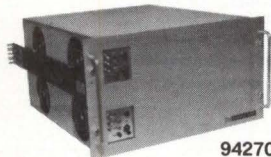


Control Data offers a complete line of semiconductor and core memory that's fully compatible with today's processors. Enclosures, too. And all are built with the same concern for quality that goes into every product we manufacture.

You see, Control Data believes in improving upon basic design when we make memory for mini-computer processors. All chips in our semiconductor memory are "full-goods." So you get all the quality and density you pay for. We use IC sockets instead of hardwiring our chips, so servicing is easier.

When your *PDP-11 needs more memory...

Add-in our 94234 Core Memory Module. It's fully compatible, of course, but you also get the inherent reliability and non-volatility of core memory technology.



Our Add-on core is fully compatible too, and fits into your PDP-11/70 rack. It gives you up to 512 Kbytes in a 10½ inch enclosure housing two power supplies, one

back plane, one controller circuit board, two to eight memory modules (in pairs), four interconnect cables and four terminator circuit boards.

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Our 94134 MOS RAM module is fully compatible with your PDP-11/34 and uses either the standard

or the modified unibus connector. Maximum configuration is 128K x 18, but smaller densities are also available. Refresh is automatic.

Our 94111 MOS RAM has block address selection via switches for the standard configuration of 16K or 32K x 16. It is pin-to-pin, voltage, signal, hardware and software compatible with *LSI-11 and PDP-11/03 systems.

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Jack Middlestaedt, Product Sales Manager CD-109
 Control Data Corporation, Computer Memory Division
 8001 East Bloomington Freeway, Bloomington, MN 55420

Please tell me more about memory for my _____ processor.

Name _____ Phone _____

Company _____ Title _____

Address _____

City _____ State _____ Zip _____



More than a computer company

	PAGE
Stepper Motor Control Chip Systems	
Sigma Instruments	190
Display Controller Chips	
Solid State Scientific	190
Signal Processing Chips	
American Microsystems	176
Communications Interface Chips	
Signetics	61
Receiver/Transmitter Chips	
Zilog	164
Data Acquisition ICs	
Harris Semiconductor Products	189
Data Acquisition System Chips	
National Semiconductor	180
A-D Converters	
TRW LSI Products	188
D-A Converters	
Teledyne Semiconductor	186
Counter ICs	
LSI Computer Systems	190
HYBRID CIRCUITS	
Hybrid A-D Converters	
ILC Data Device	188
LINEAR INTEGRATED CIRCUITS	
Octal Buffer Latches	
Motorola Semiconductor Products	182, 195
Op Amps	
Exar Integrated Systems	186
Texas Instruments	188
Power Control ICs	
Signetics	190
MEMORY/STORAGE EQUIPMENT	
FLEXIBLE DISC UNITS	
Flexible Disc Drives	
MFE	72, 73
Flexible Disc Interfaces	
Tarbell Electronics	212
Flexible Disc Controllers	
NEC Microcomputers	88, 89
Flexible Disc Systems	
Computer Technology	186

	PAGE
Data Systems Design	7
Thinker Toys	152
MAGNETIC CORE MEMORIES	
Core Memories	
EMM SESCO/Electronic Memories & Magnetics	162
MAGNETIC DISC AND DRUM UNITS	
(See also Flexible Disc Units)	
Winchester Disc Drives	
PCC Peripherals/Perlec Computer	223
Fixed Disc Drives	
Microdata	198
Shugart Associates	44, 45
Disc Controllers	
Dataram	5
Plessey Peripheral Systems	228
Xylogics	244
Disc Subsystems	
SLI Industries	210
Disc Systems	
PCC Systems/Perlec Computer	243
Winchester Disc Systems	
Advanced Electronics Design	226
MAGNETIC TAPE UNITS	
Tape Drives	
Digi-Data	122
Tape Transports	
Micro Communications	222
PCC Peripherals/Perlec Computer	141
Tape Formatters	
Kennedy	196
Tape Systems	
Telex Computer Products	209, 210
Cartridge Tape Recorders	
Tandberg Data	215
Cartridge Tape Systems	
Qantex/North Atlantic Industries	232
Cassette Transports	
MFE/Digital Products	214
Cassette Recorders	
Raymond Engineering	242
OTHER TYPES OF MEMORY/STORAGE EQUIPMENT	

	PAGE
Add-In Memories	
Control Data	239
Dataram	171
Sintrom Electronics	200
ROM/RAM PROGRAMMERS AND SIMULATORS	
P-ROM Programmers	
Sunrise Electronics	248
EPROM Programmers	
Intersil	208
EPROM Erasers	
Stag Systems	228
SEMICONDUCTOR MEMORIES	
Memory ICs	
Fairchild Semiconductor Products	28, 29
4k Static RAMs	
Electronic Arrays	188
Intersil	178
RAM Controller Chips	
Intel	9
FIFO Memory ICs	
Monolithic Memories	188
Semiconductor Memory Systems	
Dataram	216
Digital Equipment	104
Monolithic Systems	187
National Semiconductor	205
INPUT/OUTPUT AND RELATED EQUIPMENT	
AUDIO RESPONSE EQUIPMENT	
Voice Response Systems	
Mountain Hardware	156
BADGE READERS	
Badge Readers	
Sealectro/Programming Devices	27
COMPUTER PERIPHERALS—GENERAL	
Microcomputer Peripherals	
Comark	202
Desktop Computer Peripherals	
Durango Systems	152
DATA TERMINALS	
(See also Graphic Equipment)	
Printer Terminals	
Siemens	69
CRT Display Terminals	
Adage	215
Beehive International	225
Delta Data Systems	229
Hazeltine	179
Hewlett-Packard	24, 25
Human Designed Systems	214
Lear Siegler/Data Products	56, 57
Zentec	67
CRT Terminal Systems	
Lee Data	220
DISPLAY EQUIPMENT	
(See also Data Terminals and Graphic Equipment)	
CRT Display Monitors	
Ball/Electronic Display	203
Bell & Howell Display Devices	220
Motorola Display Systems	227
Sanyo Communications	233
GRAPHIC EQUIPMENT	
Color Graphic Display Equipment	
Aydin Controls	192
Ramtek	167
Color Graphic Display Terminals	
Intelligent Systems	143
Graphic Display Terminals	
Sanders Associates	75
Graphic Plasma Display Monitors	
Interstate Electronics	146
Graphics Translators	
Hewlett-Packard	87
Graphics Generators	
Raster Graphics	154
Graphics Subsystems	
Digital Engineering	234
Graphic Display Systems	
Image Automation	216
Digitizers	
GTCO	214
INTERFACE EQUIPMENT—CONTROLLERS	
Interface Boards	
MDB Systems	26, 103

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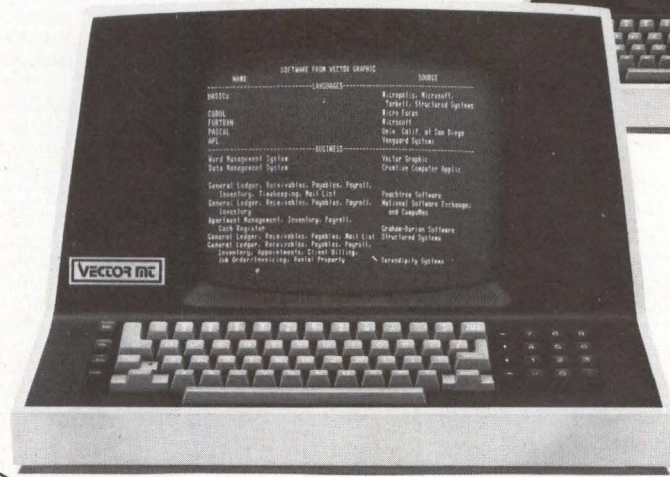
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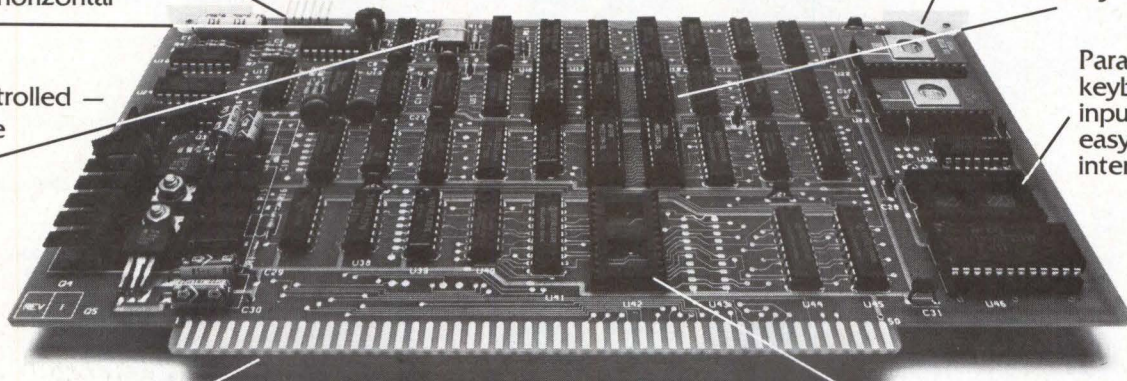
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	PAGE
Data Bus Interfaces	
Rolm	232
Flexible Disc Interfaces	
Tarbell Electronics	212
Data Generator Interfaces	
Moxon	215
Tape Formatters	
Kennedy	196
Disc and Tape Controllers	
Western Peripherals/Wespercorp Cover II	
Disc Controllers	
Dataram	5
Plessey Peripheral Systems	228
Xylogics	244
Flexible Disc Controllers	
NEC Microcomputers	88, 89
Fixed Disc Emulating Controllers	
Mini Mag	204
Peripheral Controllers	
Process Computer Systems	154
Line Printer Controllers	
Macrolink	230
Dual-Printer Controllers	
Spur Products	232
Stepper Motor Controllers	
Novatek	228
KEYBOARD EQUIPMENT	
Keyboard Switches	
Stacoswitch	247
Keyboards	
Micro Switch/Honeywell	135
Keypads	
Gimix	210
MAGNETIC CARD EQUIPMENT	
Magnetic Card Readers	
American Magnetics	198

	PAGE
PLOTTING EQUIPMENT	
Digital Plotters	
Houston Instrument/	
Bausch & Lomb	Cover III
Soltec	216
Drum Plotters	
California Computer Products	226
PRINTING EQUIPMENT	
Printers	
Centronics Data Computer	11
Computer Devices	90
Computer Printers International	30, 31
Facit	183
Integral Data Systems	71
NEC Information Systems	35, 198
Okidata	4
Tally	2
Teletype	165
80-Column Printers	
C. Itoh Electronics	139
Line Printers	
General Electric/Terminet	137
Hetra	226
Dot Matrix Printers	
Dataroyal	205
Impact Matrix Printers	
Vitek	154
Character/Graphics Printers	
Malibu Design Group	161
Digital Printers	
C. Itoh Electronics	166, 230
Thermal Printers	
Gulton Industries/Measurement &	
Control Systems	174
Telpar	204
Tape Printers	
Star Micronics	206

	PAGE
Line Printer Controllers	
Macrolink	230
Dual-Printer Controllers	
Spur Products	232
Printer Mechanisms	
Burroughs/OEM	207
Printer Elements	
Mark Stamp Steel/Mohawk Data	
Sciences	217
PUNCHED TAPE EQUIPMENT	
Punched Tape Code Converter Readers	
Data Science	212

COMPUTERS AND COMPUTER SYSTEMS

BUSINESS COMPUTERS	
Small Business Computers	
Psytek Computer Systems	152
GRAPHICS PROCESSORS	
Graphic Processors	
Magnavox Display Systems	177
Tektronix	202
Image Processors	
Grinnell Systems	51
MICROCOMPUTERS AND MICROPROCESSORS	
Microprocessors	
American Microsystems	154
Single-Chip A-D Microcomputers	
Intel	193, 194
Microcomputers	
Columbia Data Products	99
Cromemco	161
Digital Equipment	104
Monolithic Systems	40, 41
Motorola Semiconductor Products	195
National Semiconductor	150
North Star Computers	153
Control Microcomputers	
Standard Engineering	158
Microcomputers and Peripherals	
Schlumberger Products	161
Microcomputer Systems	
General Robotics	150
Severe Environment Microcomputer Systems	
EMM/SESCO	156
Microprocessor Development Systems	
Hughes Aircraft/Semiconductor	
Products	235
Intel	169
TecMa	163
In-Circuit Emulators	
Intel	166
Test System Programming Stations	
GenRad	202
Micro System Analyzers	
Millenium/American Microsystems	64, 65
Microcomputer Software	
Data Translation	206
MINICOMPUTERS; SMALL- AND MEDIUM-SCALE COMPUTERS	
Computers	
Hewlett-Packard	36, 37
Ruggedized Computers	
Rolm	191
Minicomputers	
Sperry-Univac	52, 53
Systems Engineering	
Laboratories	79, 81, 83
TIMESHARING/DISTRIBUTED PROCESSING COMPUTERS AND SYSTEMS	
Timesharing Computer Systems	
BTI Computer Systems	206
DATA COMMUNICATIONS EQUIPMENT	
COMMUNICATIONS COUPLERS	
Data Couplers	
Precision Components	215
COMMUNICATIONS INTERFACES	
Modem Eliminators	
Remark International	218
Communications Converters	
Industrial Computer Controls	222

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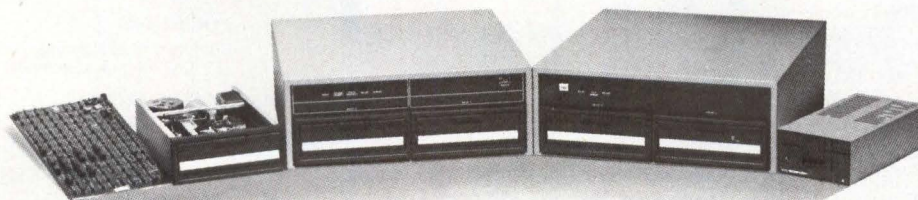
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	PAGE
Protocol Converters	
Air Land Systems	226
Communications Adapters	
Expander	230
COMMUNICATIONS MONITORS	
Communications Monitors	
TeleProcessing Products	228
COMMUNICATIONS MULTIPLEXERS	
Signature Data Multiplexers	
Phoenix Digital	202
COMMUNICATIONS SYSTEMS	
Format Synchronizer/Decommutators	
Aydin Monitor Systems	218
DATA TRANSMISSION EQUIPMENT	
Synchronous Line Drivers	
Avanti Communications	212
MODEMS; DATA SETS	
Modem Modules	
Rockwell International/ Microelectronic Devices	101
Data Modems	
Codex	196
Penril/Data Communications	19
Prentice	210
Racal-Milgo	204
Acoustic Coupler/Modems	
Anderson Jacobson	228
OTHER DATA COMMUNICATIONS EQUIPMENT	
Communications Line Switches	
Electrodata	226

DATA ACQUISITION AND CONTROL EQUIPMENT

A-D AND D-A CONVERTERS

A-D Converters	
TRW LSI Products	188

	PAGE
Hybrid A-D Converters	
ILC Data Device	188
D-A Converters	
Teledyne Semiconductor	186

ANGLE AND POSITION ENCODERS

Optical Encoders	
BEI Electronics	212

DATA ACQUISITION SYSTEMS

Data Acquisition Systems	
ADAC	63
Sperry Univac	224

DATA TRANSFER AND INTERFACE EQUIPMENT

I/O Modules	
Gordos Arkansas	208
Wyle Laboratories/Computer Products	222

I/O Subsystems	
Hitachi America	91

Analog Output Subsystems	
Burr-Brown Research	164

Analog and Digital I/O Multiplexers	
Logicon Process Systems	200

Data Generator Interfaces	
Moxon	215

MONITORING AND CONTROL EQUIPMENT

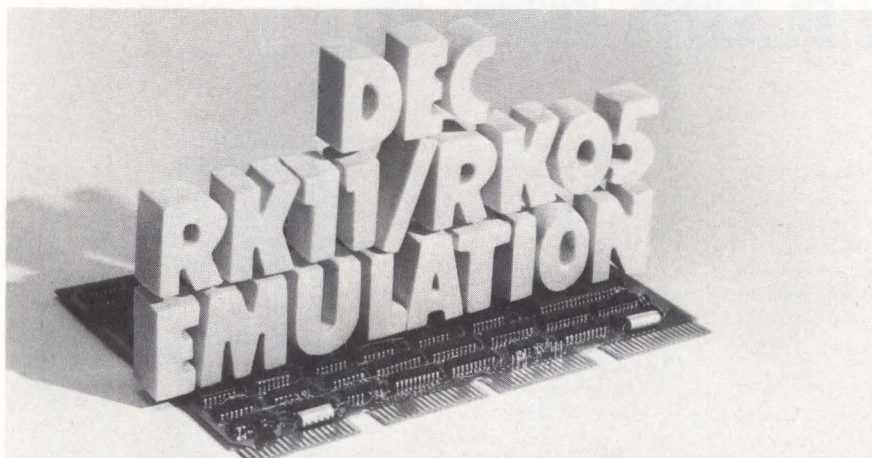
Control Microcomputers	
Standard Engineering	158

Programmable Controllers	
Cincinnati Milacron/Electronic Systems	216

TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION

COUNTERS; TIMERS

Time/Calendar Units	
Digital Pathways	213



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PAGE

DATA GENERATORS	
Pulse Generators	
Interstate Electronics	196
Programmable Word Generators	
Tau-Tron	200

DIGITAL EQUIPMENT TESTERS

Logic Analyzers	
Gould/Biomation	76, 77
Hewlett-Packard	151
Paratronics	224
Tektronix	43

Micro System Analyzers	
Millenium/American Microsystems	64, 65

INSTRUMENTATION RECORDERS

Data Loggers	
United Systems/Digitec	157

OTHER TEST AND MEASUREMENT EQUIPMENT

Digital Capacitance Measurement Probes	
International Instrumentation	205

Frequency Analyzers	
Nicolet Scientific	224

Flat Cable Assembly Testers	
Fasttest	232

SIGNAL PROCESSORS

Signal Conditioning Panels	
Data Translation	206

Filters	
Rockland Systems	220

VIDEO DIGITIZERS

Color Camera Systems	
Dunn Instruments	97

OTHER PRODUCTS; SERVICES

EDP ACCESSORIES AND SUPPLIES

Diskettes	
3M/Data Recording Products	210

Magnetic Tape	
Raymond Engineering	238

Data Cartridges	
Hewlett-Packard	218
3M/Data Products	47

Rolls and Tapes	
Eastern Specialties	149

EDUCATION

Seminars	
Integrated Computer Systems	211

EMPLOYMENT OPPORTUNITIES

Employment Opportunities	
Northrop/Defense Systems	218

Employment Services	
RSVP Services	210

EQUIPMENT BUYING, SELLING, AND LEASING

Distributors	
Radgo	205
SECO Sales	50
TransNet	214

Equipment Rentals	
Rental Electronics	159

EXHIBITIONS	
Conference/Exhibitions	
Invitational Computer Conferences	245

MARKET REPORTS	
Market Reports	
Frost & Sullivan	216

PRODUCTION AND ASSEMBLY EQUIPMENT	
Wirewrapping Tools	
OK Machine & Tool	185

PUBLICATIONS	
Directories	
Technology Recognition	216

SOFTWARE	
Software	
Xener	166

Microcomputer Software	
Data Translation	206

Test Package Options	
Adar Associates	232

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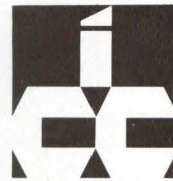
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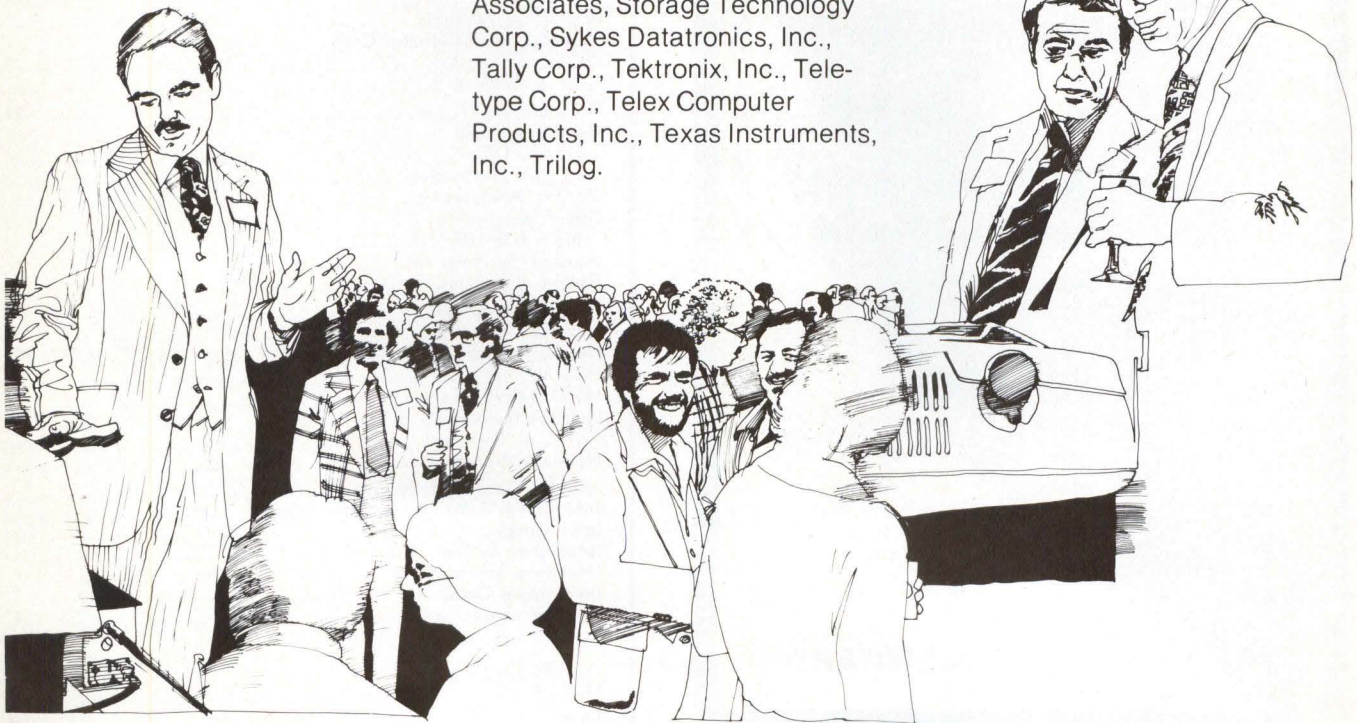
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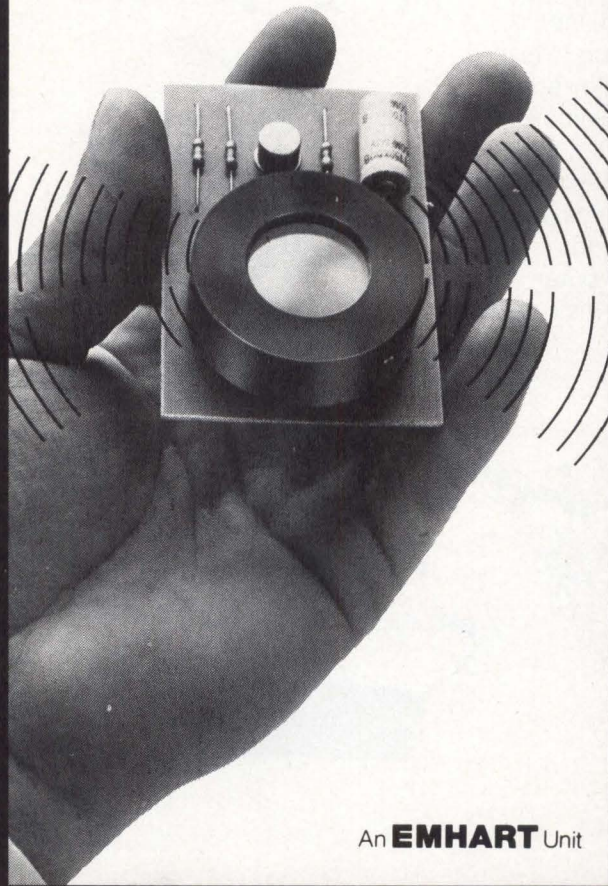
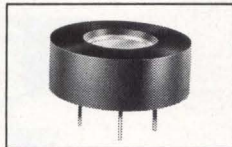
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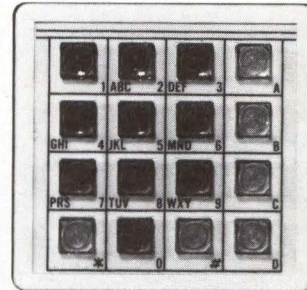
ADAC Corp.	70
Adage, Inc.	215
Advanced Circuitry	159
Advanced Electronic Design	199, 201
Advanced Micro Devices	132, 133
American Magnetics Corp.	198
AMP, Inc.	121
American Microsystems, Inc.	48, 49
Artec Electronics, Inc.	62, 63
Aydin Controls	192
Ball Electronic Display Div.	203
Barber-Colman Co.	210
Basler Electric Co.	160
Beckman IDO	22
Beehive International	225
BEI Electronics Inc.	212
Belden Corp.	219
Bell & Howell Display Devices	220
Berquist Co.	224
Burroughs OEM Div.	207
Cambridge Thermionic Corp.	140
Centronics Computer Data Corp.	11
Columbia Data Products	99
Comark Corp.	202
Computer Devices Inc.	90
Computer Printers International	30, 31
Computer Technology Control Data Corp.	186
Peripheral Products Group	239
Dataram Corp.	5, 171
Data Systems Design, Inc.	7
Datum, Inc.	200
Delta Data Systems	229
Deltron, Inc.	205
Digi-Data Corp.	122
Digital Engineering, Inc.	234
Digital Equipment Corp. Components Group	104
Digital Pathways, Inc.	213
Dunn Instruments, Inc.	97
Eagle-Picher	236
Eastern Specialties Co., Inc.	149
Electronic Memories & Magnetics Corp., Severe Environment Systems Co.	162
Facit Data Products	183
Fairchild Semiconductor Corp. Operations Div.	20, 21, 28, 29
Frost & Sullivan	216
G.E. Battery	92, 93
General Electric Termet Div.	137
Godbout Electronics	248
Gordos Arkansas	161
Gould Inc. Biomation Div.	76, 77
Grinnell Systems, Inc.	51
Gulton Industries, Inc.	174
Harris Semiconductor	189
Hazeltine Corp.	179
Hewlett-Packard Co.	24, 25, 36, 37, 87, 151
Hitachi, Ltd.	91
Hytec Microsystems, Inc.	102
Houston Instrument Div. of Bausch & Lomb	Cover III
Hughes Aircraft	235
Integral Data Systems, Inc.	71
Integrated Computer Systems, Inc.	211
Intel Corp.	9, 169
Intelligent Systems Corp.	143
Interstate Electronics	146
Invitational Computer Conferences	245
C. Itoh Electronics, Inc.	33, 166, 230
Johnson Wax Porelon	231
Kennedy Co.	1
Lear Siegler, Inc.	56, 57
Magnavox Display Systems Div. of North American Philips	177

Mallory Sonalert	246
MDB Systems, Inc.	26, 103
MFE Corp.	72, 73
Micro Communications Corp.	222
Micro Switch, a div. of Honeywell	135
Millennium Systems, Inc.	64, 65
Mohawk Data Sciences, Inc.	217
Monolithic Systems Corp.	40, 41, 187
Motorola Inc., Display Systems	227
Motorola Semiconductor Products, Inc.	54, 55, 195
NEC Information Systems, Inc.	35
NEC Microcomputers, Inc.	88, 89
Noritake Electronics, Inc.	95
Northrop Corp. Defense Systems Div.	218
North Star Computers	153
OK Machine & Tool Corp.	8, 185
Okidata Corp.	4
Panelgraphic Corp.	208
Pennwalt Corp.	12, 13
Penril Corp.	19
Percom Data Co., Inc.	98
Pertec Computer Corp. Microsystems iCOM Div.	243
Peripherals Div.	141, 223
The Pittman Corp.	17
Plessey Semiconductors	181
Polaroid Corp.	237
Power One, Inc.	175
Pro-Log Corp.	Cover IV
Qantex Div. of North Atlantic Industries	232
Radgo	205
Ramtek Corp.	167
Raymond Engineering, Inc.	238, 242
Rental Electronics, Inc.	139
Robinson Nugent, Inc.	84, 85
Rockwell International	101
Rolm Corp.	191
RSVP Services	210
Sanders Associates	75
Sanyo Communications Div.	233
Seaelectro Corp.	27
Seco Sales, Inc.	50
Shugart Associates	44, 45
Siemens Corp.	69
Signetics Corp.	61
Solitron Devices, Inc.	240
Spectra-Strip, Inc.	15, 59, 114, 224, 226, 228
Sperry Univac Mini-Computer Operations	52, 53
Stacoswitch, Inc.	247
Sunrise Electronics	248
Systems Engineering Laboratories	79, 81, 83
Tally Corp.	2
Tarbell Electronics	212
T-Bar, Inc.	204
Technology Recognition Corp.	216
Tektronix, Inc.	43, 160a*, 160b*
Teletype Corp.	165
Telex Computer Products Inc.	209
3M Company	47
Topaz Electronics	221
TransNet Corp.	123
Triad-Utrad	206
TRW Globe Motors	58
Union Carbide Corp.	208
United Systems Corp.	157
Vector Graphic, Inc.	241
Vermont Research Corp.	197
Western Digital Corp.	155
Western Peripherals Div. WESPERCORP	Cover II
Xylogics, Inc.	244
Zentec Corp.	67
Zilog, Inc.	144, 145

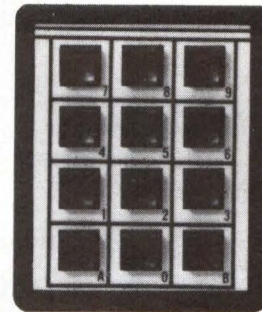
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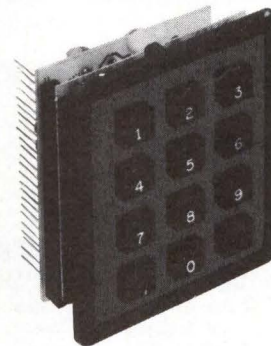
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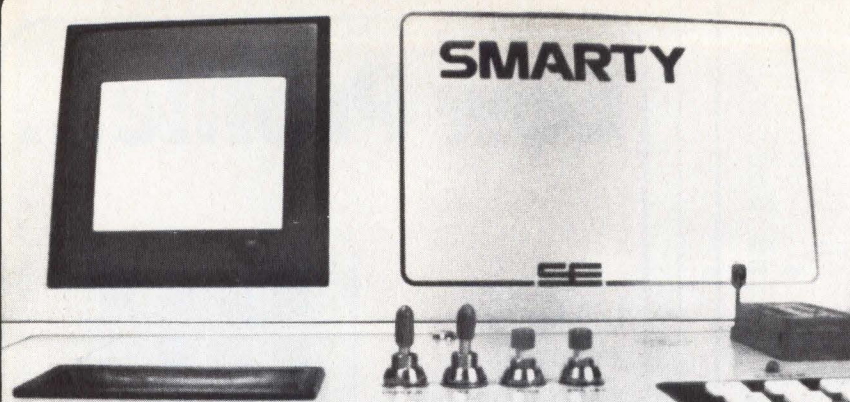


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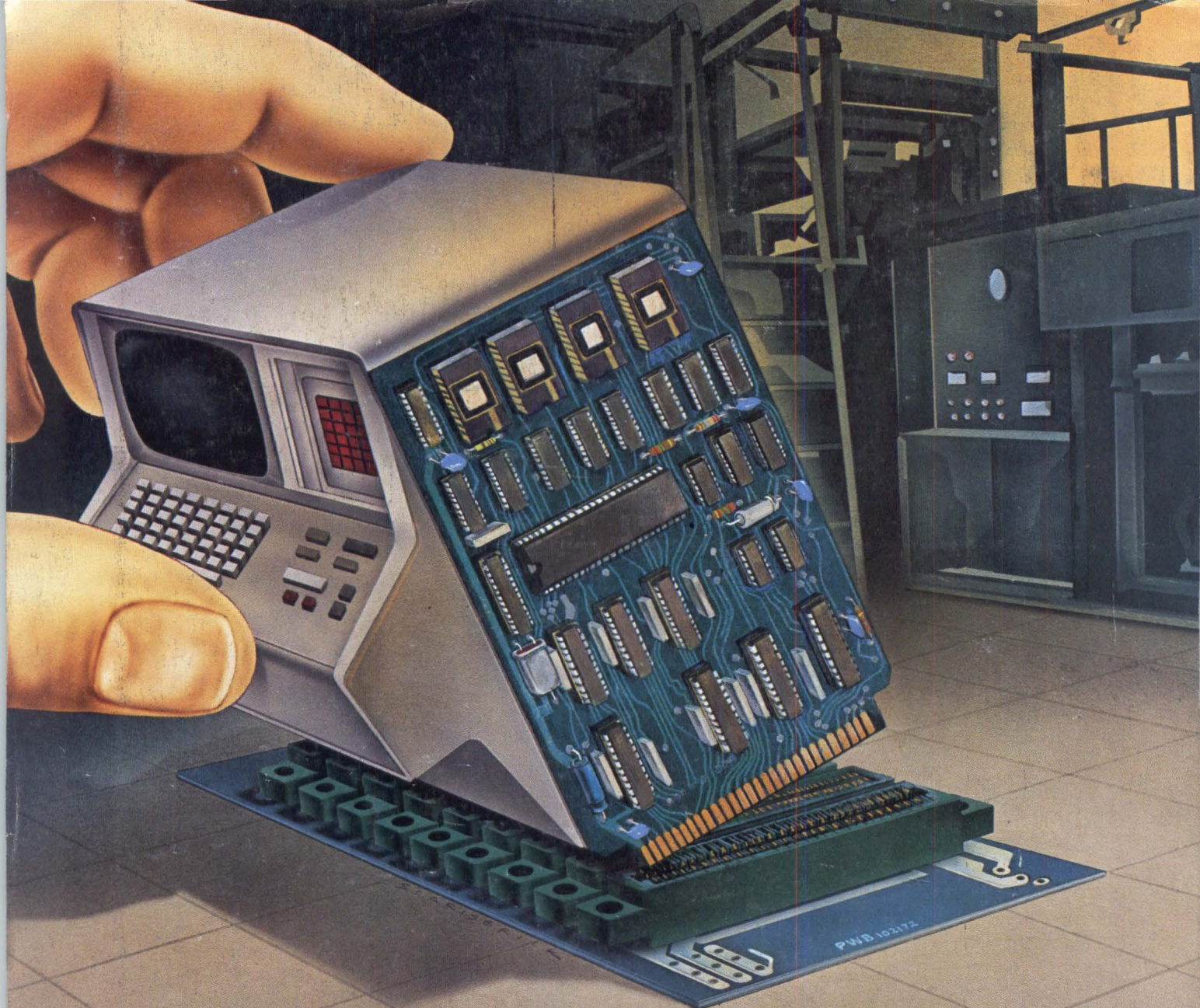
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