A PENNWELL PUBLICATION

APRIL 1982

COMPUTER DESIGN

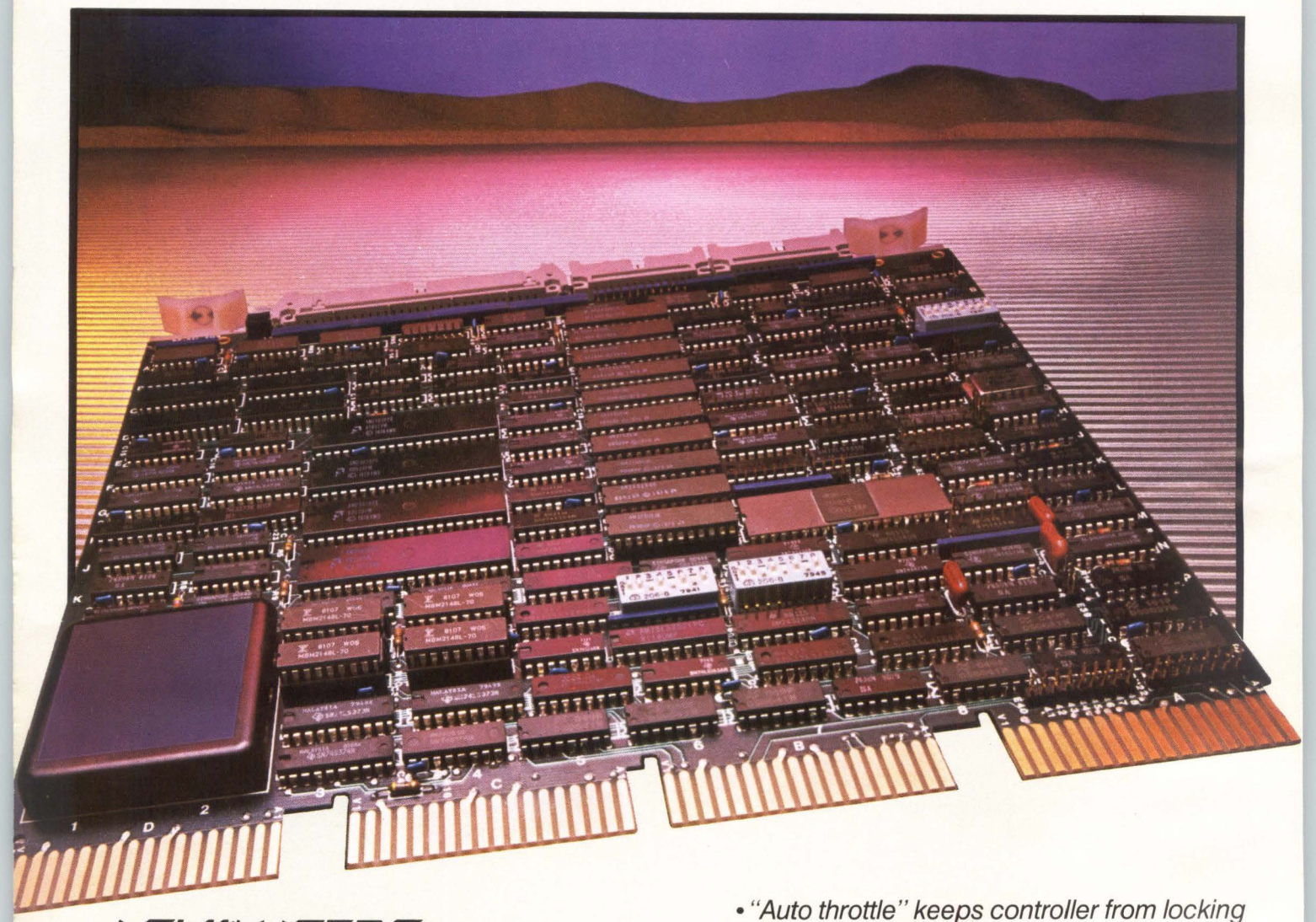
THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT: PERIPHERAL INTEGRATION HIGH TECHNOLOGY APPROACHES

DEBUGGING WITH FILTERED TRACES

A CLUSTER COMMUNICATIONS I/O PROCESSOR

EXTEND YOUR PERIPHERAL VISION.



LSI-11* USERS. The new DC-251 controller

is the first single quad board embedded SMD disc controller that lets you set your sights on maximum performance.

And it has the features to help you turn your vision into reality:

- *Mounts in any quad Q-bus* slot*
- *Emulates the DEC RM02 subsystem*
- *Each drive port has individual drive sizing switches*
- *Allows a mixed connection to drives having from 40 to 675 Mb capacity*
- *Three sector data buffer completely eliminates "data late" conditions*
- *"Auto throttle" keeps controller from locking out other peripherals*
- *Reads and writes at full disc speed*
- *Advanced micro-engine architecture*
- *One year factory warranty*
- *30 day delivery*
- *Backed by one of the best factory service organizations in the business*

Learn how your DEC LSI-11 computer can achieve maximum performance. Call or write:
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CABLE: WESPER.
In U.K.: 1st Floor The Parade, Frimley Camberley Surrey GU16 5HJ England, Telephone 0276-20934, TLX: 858306

western peripherals
Division of Wespercorp.
Number One in Controllers.

*Trademark name of Digital Equipment Corporation

CIRCLE 1

Only one company has the complete range of disks and disk backup—Kennedy

That's right. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8″ 40 MByte disk drive (Model 7300) and an 80 MByte 14″ Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼″ cartridge recorder (Model 6450), and Model 6809, ½″ Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼″ 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

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CIRCLE 2

New Cromemco System One shown with our high-capability terminal and printer.

A new small computer that won't limit you tomorrow

Here's a low-priced computer that won't run out of memory capacity or expandability halfway through your project.

Typically, computer usage tends to grow, requiring more capability, more memory, more storage. Without a lot of capability and expandability, your computer can be obsolete from the start.

The new System One is a real building-block machine. It has capability and expandability by the carload.

Look at these features:

- **Z80-A processor**
- **64K of RAM**
- **780K of disk storage**
- **CRT and printer interfaces**
- **Eight S-100 card slots, allowing expansion with**
  - **— color graphics**
  - **— additional memory**
  - **— additional interfaces for telecommunications, data acquisition, etc.**
- **Small size**

GENEROUS DISK STORAGE

The 780K of disk storage in the System One Model CS-1 is much greater than what is typically available in small computers. But here, too, you have a choice since a second version, Model CS-1H, has a 5" Winchester drive that gives you **5 megabytes** of disk storage.

MULTI-USER, MULTI-TASKING CAPABILITY

Believe it or not, this new computer even offers multi-user capability when used with our advanced CROMIX* operating system option. Not only does this outstanding O/S support multiple users on this computer but does so with powerful features like multiple directories, file protection and record level lock. CROMIX lets you run multiple jobs as well.

In addition to our highly-acclaimed CROMIX, there is our CDOS*. This is an enhanced CP/M† type system designed for single-user applications. CP/M and a wealth of CP/M-compatible software are also available for the new System One through third-party vendors.

COLOR GRAPHICS/WORD PROCESSING

This small computer even gives you the option of outstanding high-resolution color graphics with our Model SDI interface and two-port RAM cards.

Then there's our tremendously wide range of Cromemco software including packages for word processing, business, and much more, all usable with the new System One.

ANTI-OBSOLESCENCE/LOW-PRICED

As you can see, the new One offers you a lot of performance. It's obviously designed with anti-obsolescence in mind.

What's more, it's priced at only $3,995. That's considerably less than many machines with much less capability. And it's not that much more than many machines that have little or nothing in the way of expandability.

Physically, the One is small — 7" high. And it's all-metal in construction. It's only 14⅛" wide, ideal for desk top use. A rack mount option is also available.

CONTACT YOUR REP NOW

Get all the details on this important building-block computer. Get in touch with your Cromemco rep now. He'll show you how the new System One can grow with your task.

*CROMIX and CDOS are trademarks of Cromemco Inc.
†CP/M is a trademark of Digital Research

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CIRCLE 3

UP FRONT

NBS asks for aid in preparing network protocol standards

As part of its participation with the International Standards Organization (ISO) and the American National Standards Institute (ANSI) to develop international standards for computer network protocols, the National Bureau of Standards' (NBS) Institute for Computer Sciences and Technology (ICST) is asking for voluntary assistance from organizations with expertise in designing, implementing, and testing computer network protocols. ICST wants to test implementation of future standard protocols as a basis for preparation of standards, based on the architecture of the ISO's Reference Model for Open Systems Interconnection.

Assistance from qualified organizations would aid in the development and execution of procedures for testing and certifying such protocols. Documentation for the transport and session protocols, including formal specifications, implementations in the C language, and preliminary test plans, will be available from ICST. Organizations providing assistance will implement the specifications on their own systems, and connect to the ICST Network Protocol Laboratory through an S.25 based network (or other agreed type of connection) for cooperative testing.

Inquiries about program participation should be sent to Robert P. Blanc, ICST, NBS, Washington, DC 20234 (Tel: 301/921-3817).

Communication conference call for papers

Submission of manuscripts to be considered for presentation at the 1983 International Conference on Communications has been requested by program chairmen. ICC '83 will be held in Boston, Mass on June 19 to 23, and will cover all phases of communication. Complete manuscripts are due by November 1, 1982 for authors in North America, and by October 18 for all others. Program contacts are Dr L. J. Ricardi, MIT Lincoln Laboratory, PO Box 73, Rm D-422, Lexington, MA 02173 (for North America); Dr F. Tosco, CSELT, via G. Reiss Romali, 274, 10148 Torino, Italy (for Europe, Africa, and Middle East); Dr J. Valerdi and Dr J. Pomalaza, CICESE, PO Box 222, San Ysidro, CA 92073 (for Central and South America); and Dr N. Kuroyanagi, NTT Musashino, Electr Comm Lab, 9-11, 3 Chome, Midoricho, Musashino-Shi, Tokyo 180, Japan (for Asia and Oceania).

Technology exchange agreements

Intel Corp, Intersil Inc, and General Electric Co have entered into a 5-year technology exchange agreement that includes Intel's high density CHMOS process, that company's 80C51 single-chip microcomputer, and products to be developed by Intersil and GE. Intel will provide CHMOS process and design information, and will receive design information needed to manufacture Intersil and GE products for the CHMOS process or derived from the 80C51 architecture.

Advanced Micro Devices and Siemens (Munich) have reached an agreement in which AMD will manufacture Siemens' TDA 4700 switched mode power supply circuit under the designation Am6301.

SGS-Ates Semiconductor Corp has signed a 5-year technical collaboration agreement with Toshiba Corp of Japan, in which SGS will receive two high density CMOS processes and will gain access to all Toshiba products made using that technology.

UP FRONT

Pretriggers

Memory systems

Syquest Technology, Inc of Fremont, Calif, plans to reveal a micro Winchester cartridge and drive at NCC and Spring COMDEX. The 5M-byte cartridge does not require air purging and is claimed to be constructed with heads and media that are new to the small Winchester world. The company has yet to reveal the cartridge's form factor, but it is expected to be smaller than 5.25". An automated factory, complete with robotics, is being constructed to build the device.

Computers

A 3-board set made up of a complete 32-bit CPU, a 512k-byte integrated memory module, and a sophisticated I/O processor, Quadrabyte™ offers OEMs the heart of a 32-bit minicomputer for under $14,000. Features of the set, available from Gould's S.E.L. Computer Systems Div, suit it for CAD/CAM, numerical control, and industrial automation applications.

Among these features are its high speed throughput, frequent data update and summarization, ability to manipulate large amounts of data, accuracy and resolution, wide bandwidth, 16M bytes of memory addressing, and ease of expandability. Another plus is the library of CONCEPT/32 series software that includes the MPX-32 QB operating system, as well as FORTRAN, Pascal, COBOL, and assembly languages.

CINCH PAC™, a single-board distributed measurement and control computer, offers onboard intelligence, diagnostics, and power supply, thereby supplying local control at low cost. Designed by the Control Logic Industrial Systems Group of Iconix Corp for use in hostile environments, the device accommodates 32 digital and 16 analog input data points with 14-bit A-D accuracy. It responds instantly to alarm conditions without being polled by a host computer. Conversation between units or with other networks is supplied through its networking scheme.

Based on a chip level implementation of the Eclipse processor, two 16-bit realtime multiprocessing computers execute the Eclipse's instruction set. Supporting up to 512k bytes of main memory, the board level systems, developed by Data General's Technical Products Div, provide 70% of the S/140's performance at one-half the cost. For the systems, DG has developed the MP/AOS operating system and the SP/Pascal language. MP/AOS is a modular realtime multiprocessing system that supplies responsiveness in high performance realtime applications. MP/Pascal is a realtime system development tool that builds memory efficient code for direct execution on the machines.

Development systems

Network development system NDS-II from Intel allows the company's family of standalone Intellec microprocessor development workstations to act as nodes in an Ethernet network. A large number of users can simultaneously develop code creation, assembly, compilation, debugging, and program management.

With Ferranti's interactive ULA Designer system, users can specify, design, and verify custom LSI and VLSI circuits on their own premises.

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#1 **DATARAM M23**
See it first at NCC '82

Dataram M23

The Useable 4.0MB LSI-11®

A dramatic innovation unlocks the power of the LSI-11/23

The M23: The answer to your high-performance LSI-11/23 needs

What controllers can be used?
The key to the M23 System, Dataram's proprietary memory management Q-MAP enables you to use the full 4.0MB power of the LSI-11/23. It provides I/O mapping, which supports a wide range of existing peripheral controllers on an 18-bit bus (Q18). While still maintaining the 22-bit bus (Q22) for 4.0MB main memory addressing.

DEC® software compatibility?
The M23's Q-MAP emulates DEC's KT24 memory management, which means it operates with RSX11-M, RSX11-M PLUS, RSTS, UNIX, and all other DEC operating systems which support the KT24.

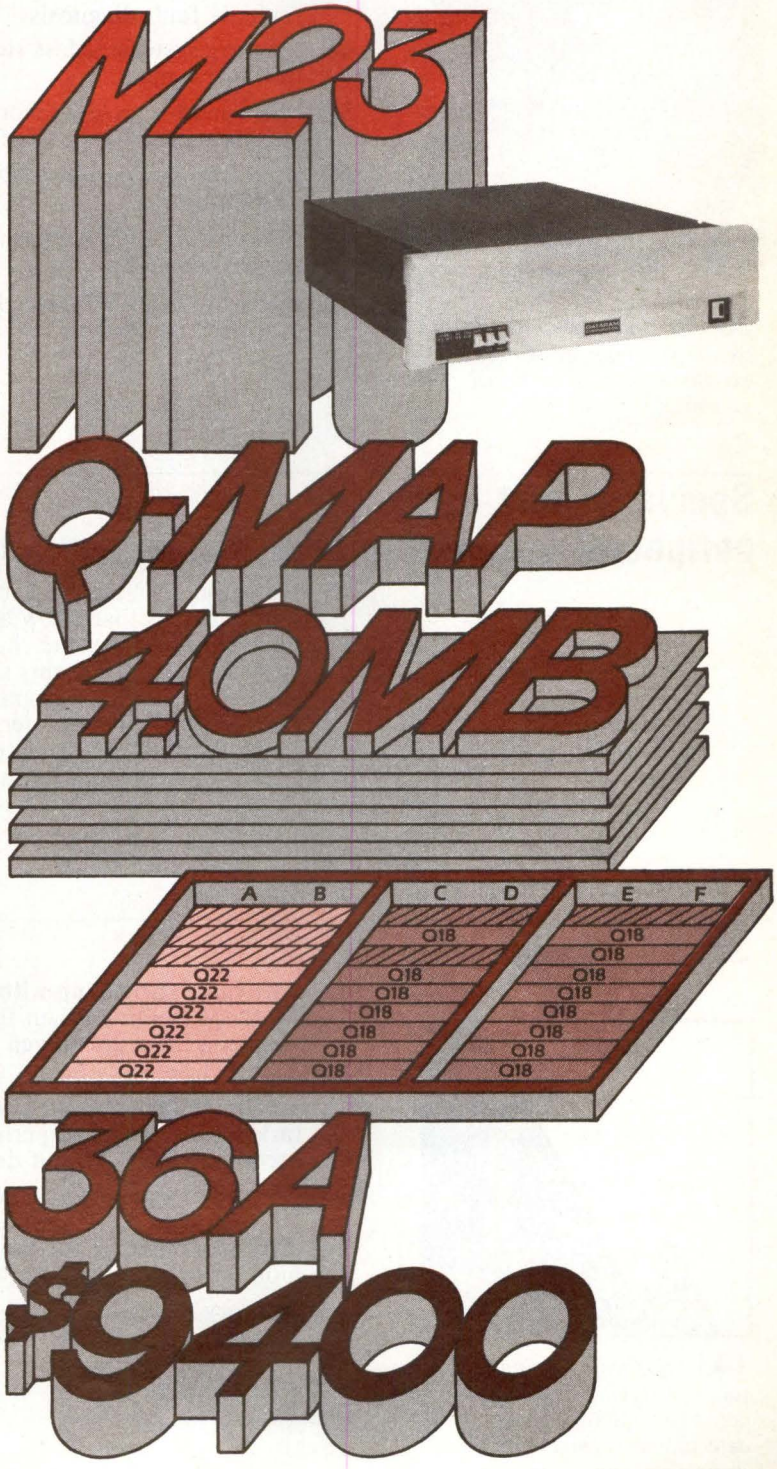
Memory?
A 1.0MB quad board is contained in the basic M23 configuration. Think of it, a full 4.0MB on only four DEC quad boards! And each additional 1.0MB is only $3400.

System configurability?
The 5¼" M23 provides an incredible 27 DEC dual slots. And since the basic configuration (LSI-11/23, OCU, two SLUs, Q-MAP, bootstrap/diagnostic PROMs, and 1.0MB memory) occupies only six of those 27 slots, that leaves you 21 slots to configure a high-performance LSI-11 system.

5.0 volt current?
36 amps.

Price?
$9400 for the basic configuration, with 1.0MB, in single quantity. Yes, only $9400...and considerably lower in OEM quantities.

More information?
Circle the reader service number below, or better yet, call Dataram now at 609-799-0071, or write to Dataram, Princeton Road, Cranbury, New Jersey 08512. Telex: 510-685-2542.



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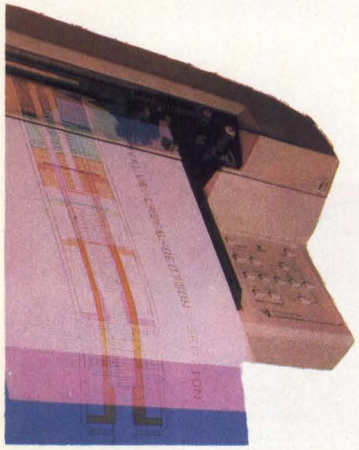
DATARAM CORPORATION

CIRCLE 4

COMPUTER DESIGN®

System technology



26 *Personal computer color plotter can interface to IEEE 488, HP-IB, or RS-232-C based systems*

Special report on peripheral integration/high technology approaches

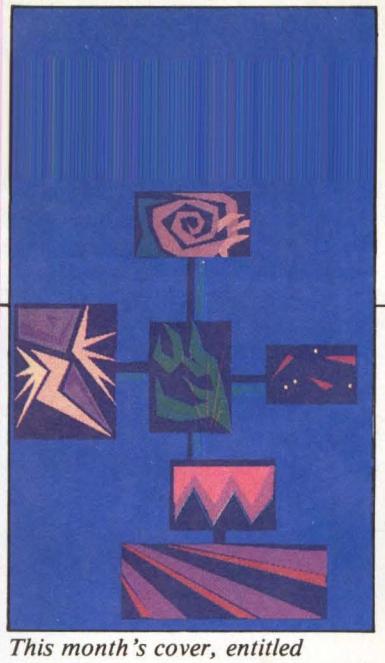
System design

143 *Software tracing is valuable capability for both debugging microprocessors and detecting abnormal conditions during program execution*

Vol 21, No 4
April 1982

Electro/82

SID '82



This month's cover, entitled "Smart Peripherals," was created by Diane Sparagano on the Digital Effects Video Palette III, a computer aided freehand drawing system

System components

Departments

Designers' Preference Survey*

Editorial reviewer for this issue:

Albert H. Ashley

*Appearing in Domestic issues only

GOULD BIOMATION K100-D

7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.

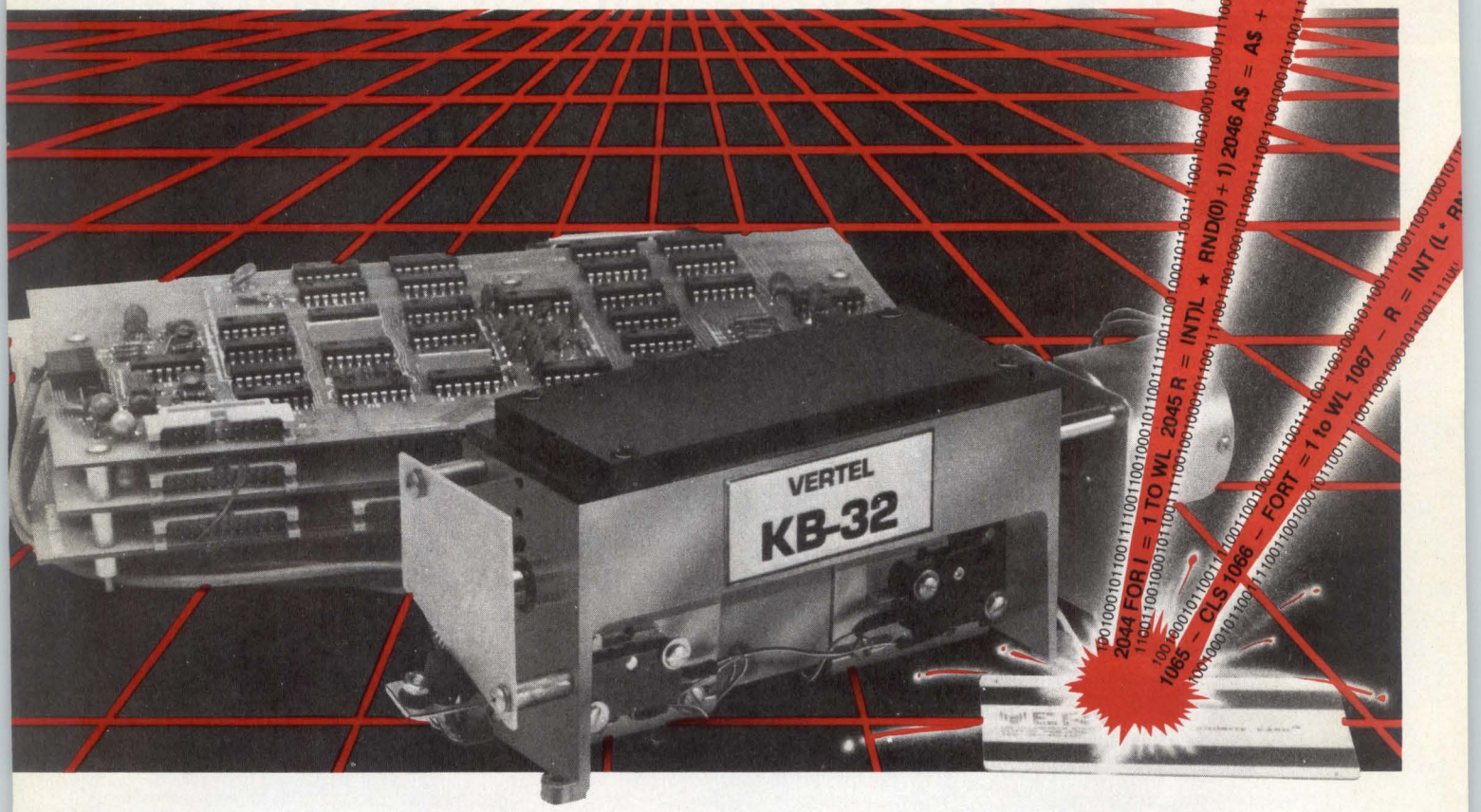
The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

GOULD

Electronics & Electrical Products

Circle 5 for Comparison Guide
Circle 6 for App. Note request form
Circle 7 for T-12 communicator data

At VERTEL, we just can't leave well enough alone.



We've doubled storage capacity and reduced reading time...simultaneously

Introducing the KB-32 Magnetic Card Reader/Writer. At Vertel we're always looking for ways to improve parameter loading. With our new KB-32 Card Reader/Writer, we have even outdone the KB-31 system...a system that has become an industry standard.

For example, we've doubled the storage capacity of our Kilobyte card™, which now means you can record over 2176 8-bit bytes on one card. And our new reader/writer has an improved head that reads all 4 tracks simultaneously...providing twice the amount of information in one-half the time, thereby improving reading time by a rate of 4.

Designed for microprocessor-based systems, the new KB-32 is ideally suited as a low cost peripheral for parameter loading and/or data storage in process control systems, medical data systems and other similar applications.

Call us today to see how the Kilobyte™ system can benefit you!

VERTEL

CIRCLE 162

125 ELLSWORTH STREET, CLIFTON, N.J. 07012 (201) 472-1331

COMPUTER DESIGN HALL OF FAME

THE FLOOR IS OPEN FOR NOMINATIONS

This December, *Computer Design* will celebrate its 20th Anniversary. While pondering all of the weighty and somewhat worn-out approaches to celebrating an anniversary, an idea suddenly began to gel.

Our industry is based, for the most part, on contributions from companies founded by individuals—entrepreneurs, originators, inventors, marketing strategists: all who had a better idea, an idea that became the cornerstone of a company that went on to prosper and grow. Not all such companies became gigantic corporations, and the founding ideas were not necessarily the ones that made the companies succeed. Moreover, many of the original founders of the significant corporate entities in our field are no longer with those companies; they either left to found other companies or retired.

To provide warranted recognition to the true industry pioneers, we have decided to dedicate this year's December issue to people and their contributions to the industry, entrepreneurs who founded or were principals in companies that started from virtually nothing but made significant technological contributions to our industry. Who should know these people better than you, our readers? Many of you have been around this industry as long, or longer, than *Computer Design* and most of you know who was a principal in what company that introduced a technological breakthrough in our field.

We have selected the largest and most august panel ever assembled to nominate the outstanding candidates for the *Computer Design* Hall of Fame—**YOU**, the 83,000 senior engineering people who read *Computer Design* and make this industry what it is today.

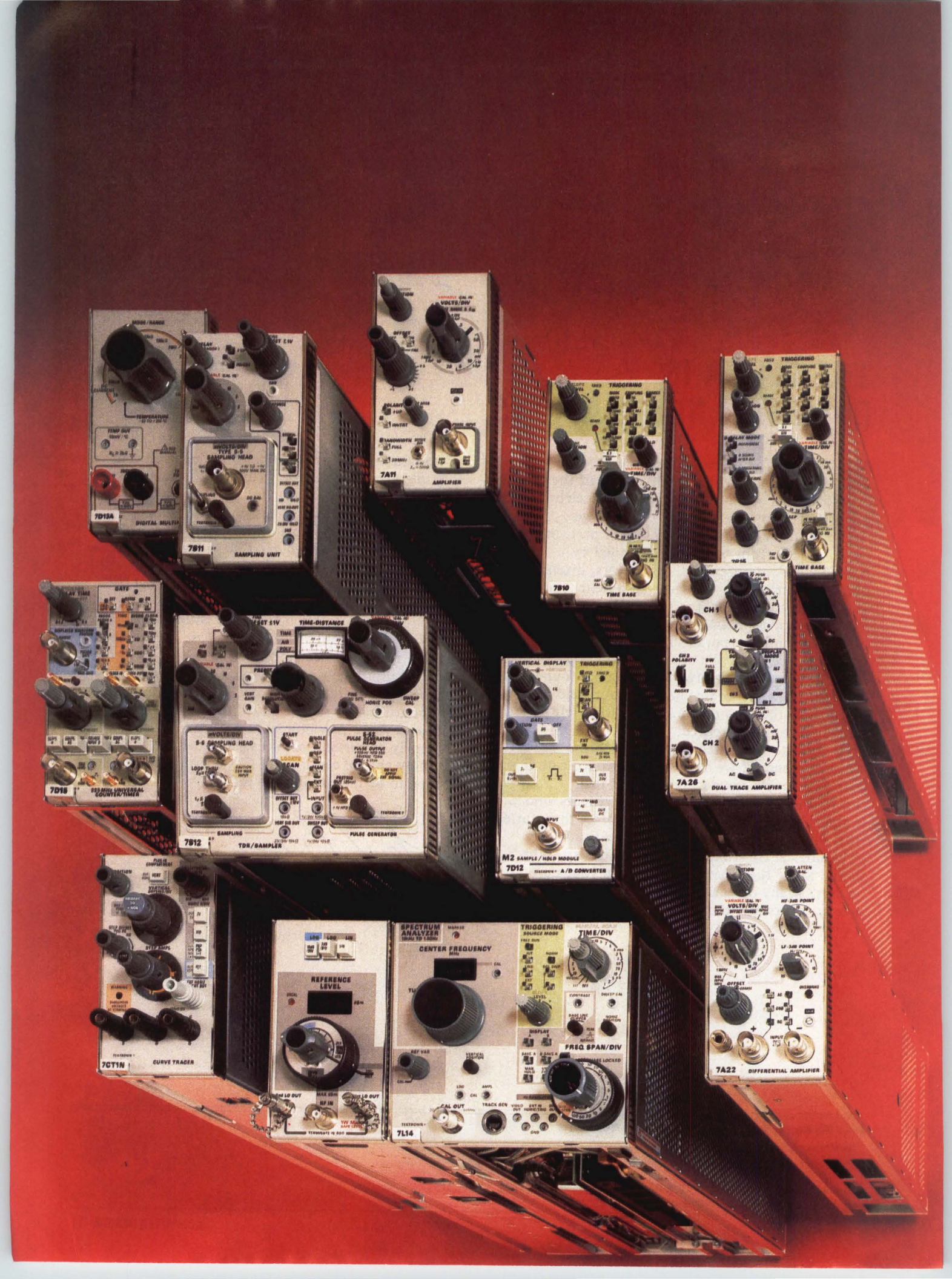
We invite you to list up to three nominations for us to review for a slate of candidates. Use the specially marked reader service card inserted behind the front cover of this issue to make your nominations. (If that card is missing from your copy, circle number 502 on a standard reader service card from this issue and we will send you a new nomination form.) Your input is extremely important, so please consider the choices carefully and be certain you send in your nominations in time to be included in the judging.

Saul B. Dinman

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—November
"Software Piracy and the Copyright Laws"
Richard H. Stern, Baker & Hostetler

This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.


7D13A
DIGITAL MULTI
7B11
SAMPLING UNIT
7A11
AMPLIFIER
7B10
TIME BASE
TIME BASE
7D15
7B12
TDR/SAMPLER
M2 SAMPLE / HOLD MODULE
7D12
A/D CONVERTER
CH 1
CH 2
7A26
DUAL TRACE AMPLIFIER
7CT1N
CURVE TRACER
REFERENCE LEVEL
SPECTRUM ANALYZER
CENTER FREQUENCY
TRIGGERING
TIME/DIV
FREQ SPAN/DIV
7L14
7A22
DIFFERENTIAL AMPLIFIER

TEK 7000 SERIES
MODULAR OSCILLOSCOPES

These days, who can afford to change scopes every time they change applications?

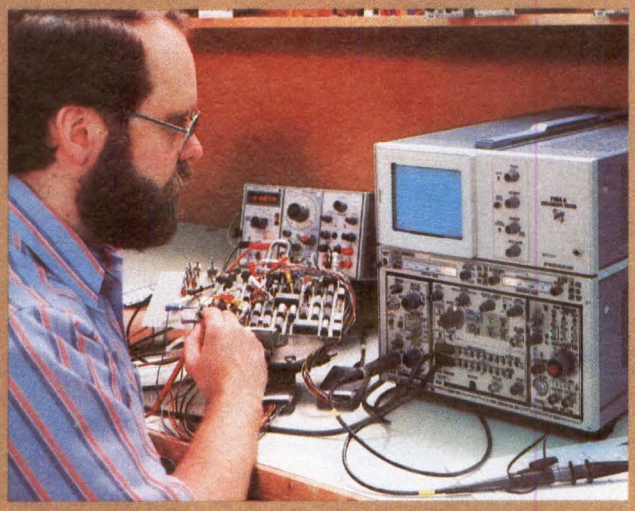
Now more than ever, Tektronix 7000 Series users know the performance and investment advantages of the world's most respected oscilloscopes.

While money has been tight and major equipment purchases few, they could respond to their evolving measurement needs by adding Tek 7000 Series plug-ins for a fraction of the cost of an entirely new scope.

Now, with new tax credits and other incentives at hand, that existing pool of plug-ins makes every new 7000 Series mainframe purchased all the more valuable.

Today, some 35 plug-ins support your 7000 Series investment. You start with a choice of 22 scopes, including the highest bandwidths, the fastest writing speeds, unique multimode storage and waveform digitizers.

As new applications require, you can add the appropriate plug-in. Add multimeters. Differential



amplifiers. Sampling units. Spectrum and logic analyzers. Curve tracers. Digital delay units. And much more. Tek's commitment to 7000 Series versatility is highly developed and still expanding.

It's the one scope package that keeps expanding in value. Digital designers, for example, often begin their Tek 7000 Series investment with the 7704A, a general-purpose 250 MHz oscilloscope. They can use the 7704A's multi-trace capabilities, for example, to view analog characteristics on up to four different logic lines.

For logic analysis, they simply plug in the 7D01 to enjoy the unique interaction of a multi-trace scope and a 16-channel logic analyzer, and simultaneously view both the digital and analog signal.

For power supply evaluation, they can plug in the 7A13 Differential Amplifier, and easily view millivolts of noise riding on power supply buses. Or add a 7D11 Digital Delay unit to find troublesome glitches several clock cycles downstream from the trigger point.

Each plug-in works with virtually all 7000 Series scopes. So if you ever need more than one high bandwidth scope, you can continue to use the plug-ins you have.

Call your Tektronix Sales Engineer today: Get expert help in selecting the right instruments for your evolving needs. Promise yourself all the performance you need now, plus insurance for the future.

For further information, contact:

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Layered software for applications programming... helps the pieces fit.

Meeting each minicomputer user's software requirements is a difficult and time-consuming task for the systems integrator. Now, with a unique layered approach to software, Gould S.E.L. makes applications programming more efficient and less costly. Each layer addresses a related set of user programming problems. Within each layer, there is a choice of software aids that focus on specific user requirements.

In addition to most modern high-order languages and the advanced MPX-32 interactive, real-time operating system, Gould S.E.L. offers extensive software libraries. They contain prefabricated code to eliminate repetitive programming. Our software tools and libraries allow the programmer to more efficiently generate, test, optimize and document applications programs and reduce development and maintenance costs. These tools also provide management with greater visibility and control.

Gould S.E.L. has the most comprehensive selection of software development tools and methodologies available today. We also offer the SOFTOOL 80® package as a licensed part of our standard product line. Memory requirements and CPU overhead are never a problem as all the tools and libraries are removed after program development is completed.

Our layered approach provides all the pieces for your applications programming needs...and they fit. Call or write the company with a lifetime of real-time experience and watch the pieces fall in place for you.

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CIRCLE 13

CONFERENCES

MAY 7-9 AND MAY 21-23—Computer Showcase Expo, Anaheim Calif; and Boston, Mass. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAY 9-12—Phoenix Conf on Computers and Communications, Phoenix, Ariz. INFORMATION: E. David Metz, Motorola Inc, MD B136, PO Box 2953, Phoenix, AZ 85062

MAY 10-12—IEEE Symposium on Circuits and Systems, Rome, Italy. INFORMATION: Institute of Electrical and Electronic Engineers Inc, 6411 Chillum Pl, NW, Washington, DC 20012

MAY 10-12—Electronic Components Conf, Sheraton Harbor Island Hotel, San Diego, Calif. INFORMATION: D. J. Bendz, IBM Corp, Dept 649/014-4, 1701 North St, Endicott, NY 13760

MAY 11-13—Society for Information Display Internat'l Sym, Town-Country Hotel, San Diego, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

MAY 17-19—Custom Integrated Circuits Conf, Americana Hotel, Rochester, NY INFORMATION: Constantine Anagnostopoulos, General Chairman, Research Labs, B-81, Eastman Kodak Co, Rochester, NY 14650. Tel: 716/477-6768

MAY 18-20—Northcon, Seattle Ctr Coliseum, Seattle, Wash. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 18-20—Control Engineering Conf and Expo, O'Hare Expo Ctr, Chicago, Ill. INFORMATION: Tower Conf Mgmt Co, 143 N Hale St, Wheaton, IL 60187. Tel: 312/668-8100

MAY 25-27—Electro, Sheraton-Boston Hotel, Hynes Auditorium, and Commonwealth Armory, Boston, Mass. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 27—IEEE Sym, Trends and Applications: Advances in Information Technology, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Allen Hankinson, Nat'l Bureau of Standards, Admin Bldg A209, Washington, DC 20234

JUNE 7-10—National Computer Conf, Astrohall, Houston, Tex. INFORMATION: AFIPS, NCC, PO Box 9658, 1815 N Lynn St, Suite 800, Arlington, VA 22209

JUNE 13-17—IEEE Conf on Pattern Recognition and Image Processing, Anaheim, Calif. INFORMATION: IEEE, Administrative Office, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386.

JUNE 14-16—Design Automation Conf, Caesars Palace, Las Vegas, Nev. INFORMATION: Bryan Preas, VR Informations Systems, Inc, 5766 Balcones Dr, MS 203, Austin, TX 78731

JUNE 15-18—National Computer Graphics Assoc Conf, Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, Inc, 2033 M St NW, Suite 330, Washington, DC 20036. Tel: 202/466-5895

JUNE 21-23—Technical Conf on emi/rfi Shielding of Plastics, Sheraton O'Hare Hotel, Rosemont, Ill. INFORMATION: Harold Chapman, D.M.E. Co, 1975 N 17th Ave, Melrose Park, IL 60160. Tel: 312/626-2900

JUNE 28-30—Comdex/Spring '82, Atlantic City Convention Hall, Atlantic City, NJ. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

JULY 19-21—Computer Simulation Conf, Marriott City Center Hotel, Denver, Colo. INFORMATION: Marlene Moller, The Aerospace Corp, PO Box 92957, Los Angeles, CA 90009. Tel: 213/648-6608

JULY 12-15—Powercon 9, Power Electronics Conf and Exhibit, Hyatt Regency Crystal City, Washington, DC. INFORMATION: Ronald Birdsall, General Chairman, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/656-1890

JULY 26-30—ACM Siggraph '82, Boston, Mass. INFORMATION: Elaine Sonderegger, General Chairman, PO Box 353, Derby, CT 06418. Tel: 203/735-9980

SEMINARS

MAY 24-26—X.25 for Long Haul and Local Networks, Packet Switching Protocols Seminar, Washington, DC. INFORMATION: Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. Tel: 213/394-8305

SHORT COURSES

MAY-AUG—EMC, TEMPEST, and emi/rfi course studies, various U.S. cities and dates. INFORMATION: Don White Consultants, Inc, Internat'l Training Ctr, State Rt 625, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030

MAY 10-11 AND 13-14—EMC Management, San Francisco, Calif, and San Diego, Calif. INFORMATION: Don White Consultants, Inc, Internat'l Training Ctr, State Rt 625, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030

MAY 10-14—Applied Interactive Computer Graphics, Univ of Calif, Los Angeles, Calif. INFORMATION: Marc Rosenberg, Continuing Ed in Engineering and Mathematics, 6266 Boelter Hall, UCLA, Los Angeles, CA 90024. Tel: 213/825-1047

MAY 24-26—VLSI/Gate Arrays: Technology, Logic Design, and Automation, Univ of Wisconsin Extension, Madison, Wis. INFORMATION: Avinash Vaidya, Dept of Engineering and Applied Science, Univ of Wisconsin Extension, 432 N Lake St, Madison, WI 53706. Tel: 608/262-8592

MAY 24-27 AND JUNE 28-JULY 1—Modern Telecommunications Networking: Electronic Messaging, Local Area, Packet Radio, and Satellite Communication Networks, UCLA, Calif, and Univ of Maryland Univ College, Md. INFORMATION: Dr. Izhak Rubin, Univ Extension, Continuing Ed in Engineering and Mathematics, 6266 Boelter Hall, UCLA, Los Angeles, CA 90024. Tel: 213/825-1047

JUNE 21-25—Personal Computers, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: James Austin, Director, Summer Sessions Office, MIT, Cambridge, MA 02139. Tel: 617/253-2937

JULY-AUG—Computer Science Courses, 13 course studies include computer graphics, data bases, local area networks, Ada, artificial intelligence, programming, and systems design, Univ of Calif, Santa Cruz. INFORMATION: Anne Earl, Institute in Computer Science, Dept B, Univ Extension, Carriage House, Univ of Calif, Santa Cruz, CA 95064. Brochure available. Tel: 408/429-5434

JULY 12-AUG 6—Technical Institutes/Courses, Union College, Schenectady, NY. INFORMATION: Union College, Office of Graduate and Continuing Studies, Wells House, 1 Union Ave, Union College, Schenectady, NY 12308. Tel: 518/370-6288

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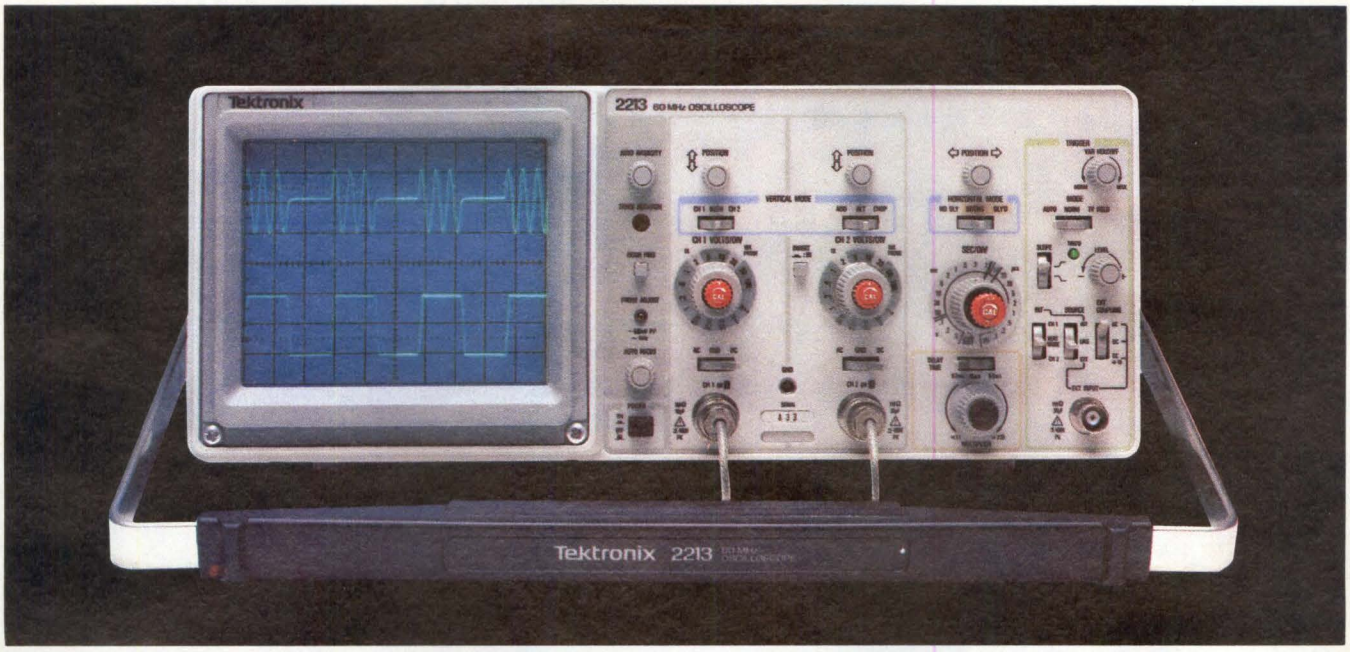

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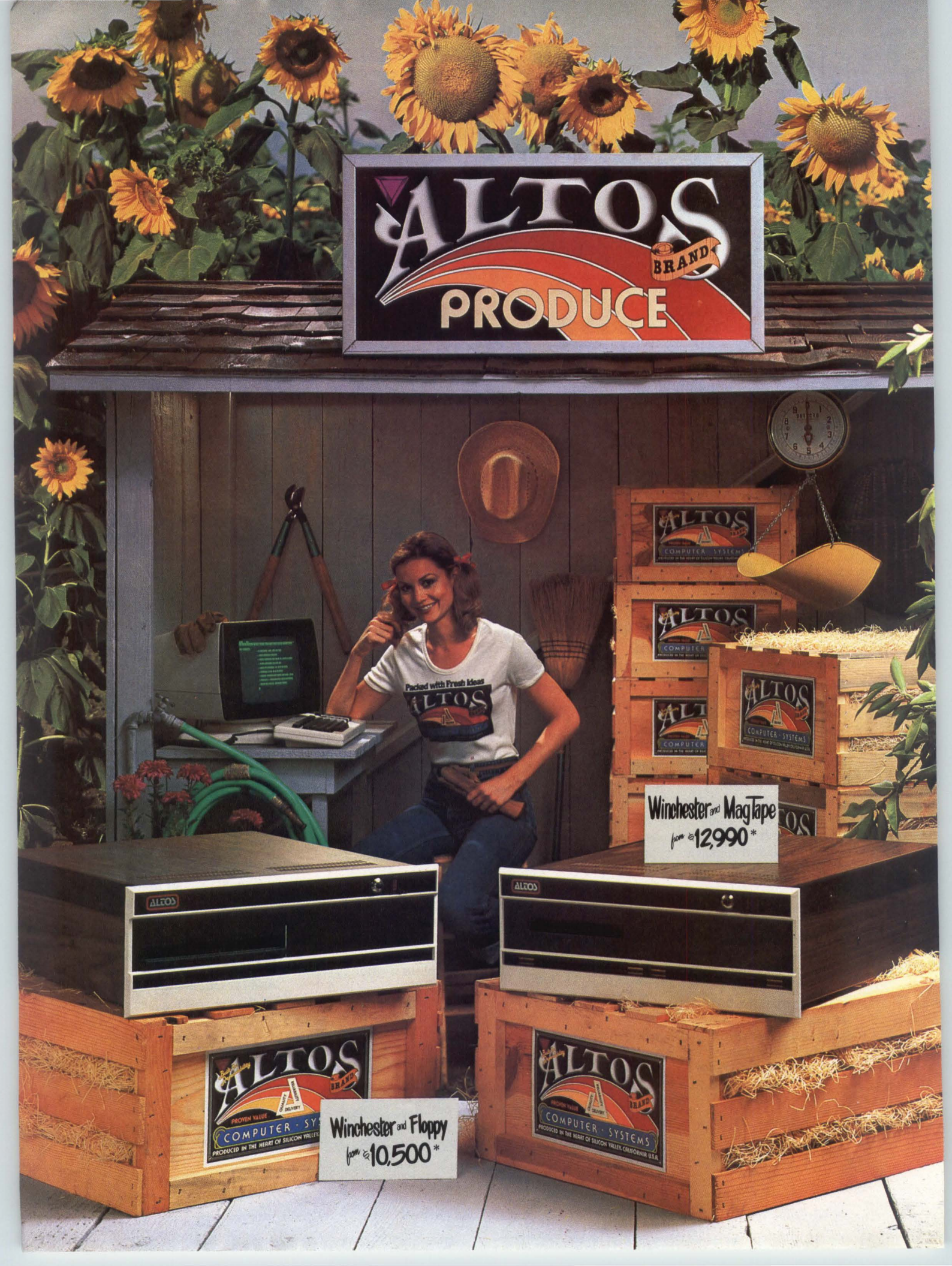
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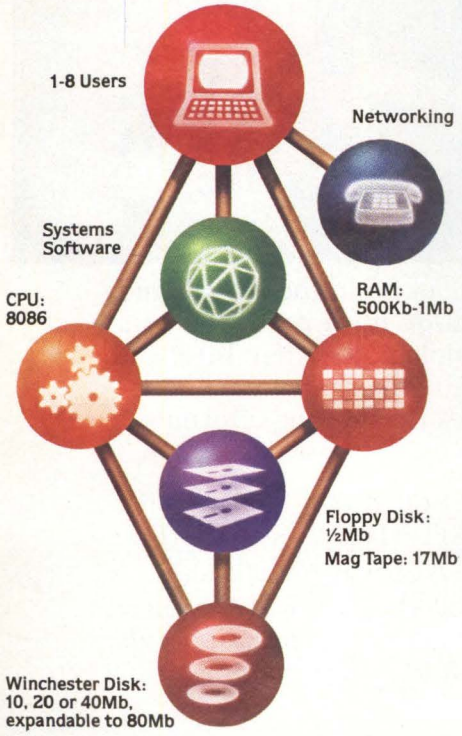

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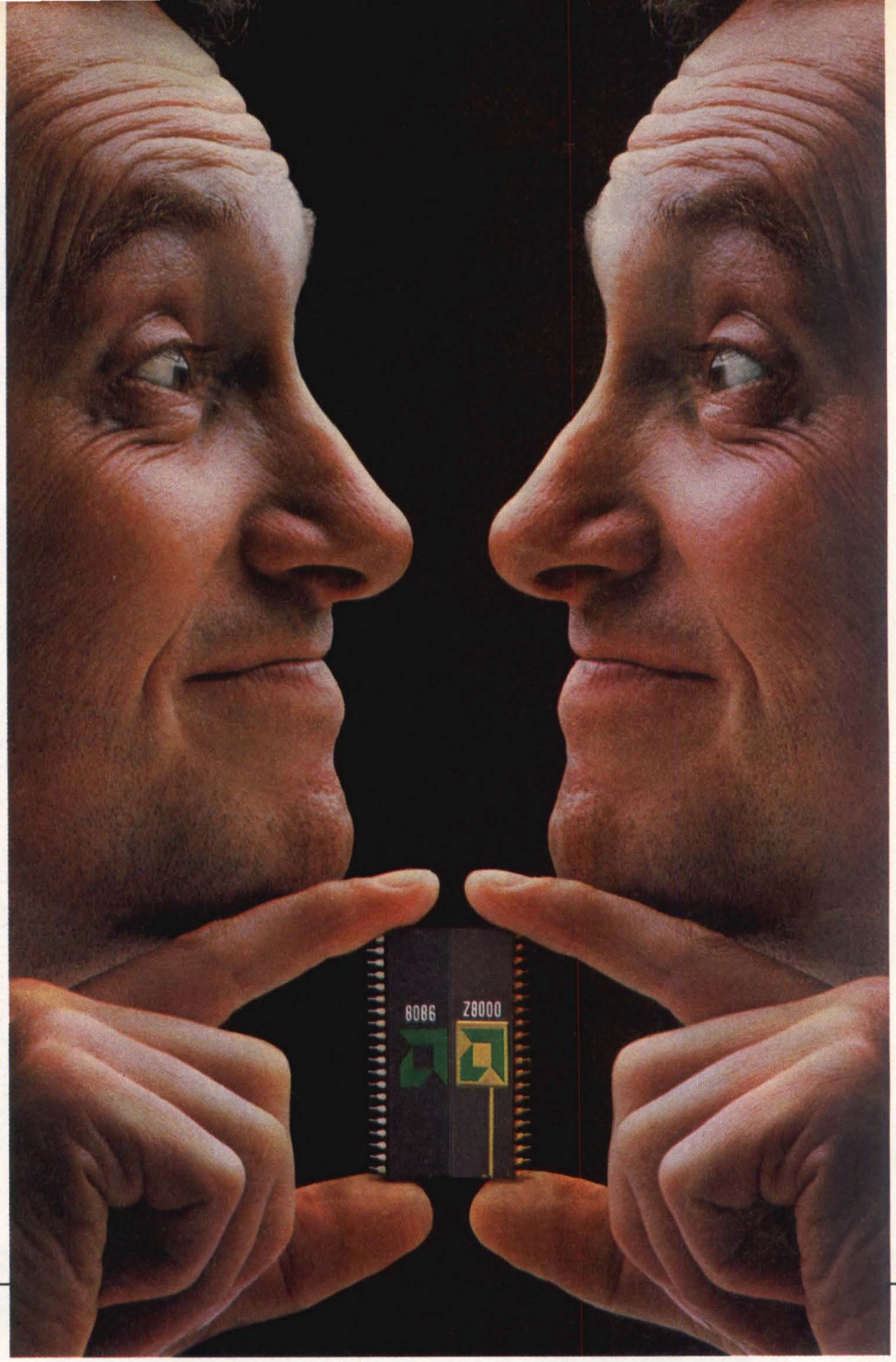
XENIX is a trademark of Microsoft and is a microcomputer implementation of the UNIX™ operating system. UNIX is a trademark of Bell Laboratories.
Ethernet is a trademark of Xerox Corp.

CIRCLE 15



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CIRCLE 16

To the Editor:
Your December editorial, "Watching the Japan Watchers," was typical of some of the problems facing United States industries today. Once the entrepreneurs have been replaced by professional managers who essentially are accountants and ex-salesmen, the essence of synergistic creativity has been replaced by the need to realize short term profits—for that is how these managers are evaluated by Wall Street and that diminishing breed, the stockholder. This has been covered in hundreds of magazine articles, so it's nothing new.

If you'd been to Business School you would have understood that case study does consider the human relations element in every case history—call it the holistic approach. It's impossible to study marketing, operations management, and forecasting without considering the human element.

Although the problems with United States industry are complex, you might discuss the attitudes of incompetence, whether it is on the management level or on the grunt level. And the public, becoming more aware, refuses to be continually ripped off by American-made junk.

Please take the time to enroll in some Business School courses. I suggest you write about something you understand—it's what they told us all in high school. Remember?

Frank J. DeFelice
Electronic Systems Section
AVCO Everett Research Laboratory, Inc
2385 Revere Beach Pkwy
Everett, MA 02149

The Editor Replies:
Not all companies have found the need to displace or replace the creative entrepreneurs with professional managers. There are companies that have succeeded in establishing equally important roles for the creative talents who drive a technology based company and, at the same time, managed quite successfully to retain a good Wall Street image. Digital, for example, has had a track record of sparking creative individuals into generating new product lines, either as teams or individuals. Whether or not they could have realized even greater short-term profits by not suffering through some of the product disasters they experienced is a moot point because they certainly have maintained a dynamic image in the public market. IBM, Hewlett-Packard, and Tektronix are all companies that have succeeded in providing the technologist with an attractive environment in which to create, with a dual-ladder approach that does not treat the technologist as a drone.

I have been to "B" school and, although it may have been before holism was even a popular term with psychotherapists, I don't think that the "B" schools have quite entered the "touchy-feely" phase of interpersonal relationships yet. In discussing the subject with an acquaintence, a well known Harvard Business School professor, he commented that Harvard has been one of the leading advocates for the holistic, or system theory, approach in the training of managers, but that it has led to a state of confusion at the "B" school because it is incoherently mingled with the more traditional quantitative approach practiced by most of the other leading "B" schools. Unlike the medical schools that have successfully separated their curricula into quantitative (scientific) and qualitative (clinical) approaches with clear cut methodology for the transfer of knowledge between the laboratory and the clinic, the "B" schools are still in the early phases of defining this connection because they are all coming from a traditional quantitative philosophy.

Incidentally, I do believe that 25 years of experience in the computer industry—about three quarters of which has been spent in a technical management function—does give me at least the right to believe that I have some germaine comments to make on the subject, whether or not you may agree.

To the Editor:
Just read your "Watching the Japan Watchers" editorial and had to convey my sincere compliments to you. Not only have you correctly labeled the "paranoia" of the Japan watchers, and exposed the hip-shooting response of the business schools and many of our large companies' managers, but you have given some much needed insight to the professional manager and employee mentalities that have allowed this to happen.

Business schools, corporations, managers, and individual employees need to consider returning respect for the individual and human relations to a primary position, rather than to the "bottom line".

Our company, TASA, is one of those garage startups. Our people have successfully invented and productized a control technology that is totally unique in the world of electronics. We believe it could be the human interface technology of the future for an almost infinite number of applications but, as good as it is, it is the people at TASA and not the technology that make it happen.

Robert Abler
Touch Activated Switch Arrays, Inc
2346 Walsh Ave
Santa Clara, CA 95051

To the Editor:
I read your editorial "Watching the Japan Watchers" and feel that it is an outstanding piece. I was much encouraged to finally hear from someone who was not joining in the panic of the moment with the distorted thinking that we must "become Japanese" in order to more successfully compete. Since when has American industry accepted defeat —"if you can't beat 'em, join 'em?!"

Ellyn Powelson
Tandon Corp
20320 Prairie St
Chatsworth, CA 91311

To the Editor:
Amen! This hits to the soul of the problem. (Ref: Dec 1981 editorial, "Watching the Japan Watchers.")

Anthony Barr
Barr Systems, Inc
3701-A Lake Boone Trail
Raleigh, NC 27607

To the Editor:
It's the best editorial ("Watching the Japan Watchers," Dec 1981) I've read in any trade or business/financial publication regarding Japanese competition. I'm all for participative management, but to completely submerge the drive and innovation of American entrepreneurship in the morass of mediocre "group think" a la Japan is idiotic!

Bob Novascone
Motorola Semiconductor
725 S Madison Ave
Tempe, AZ 85281

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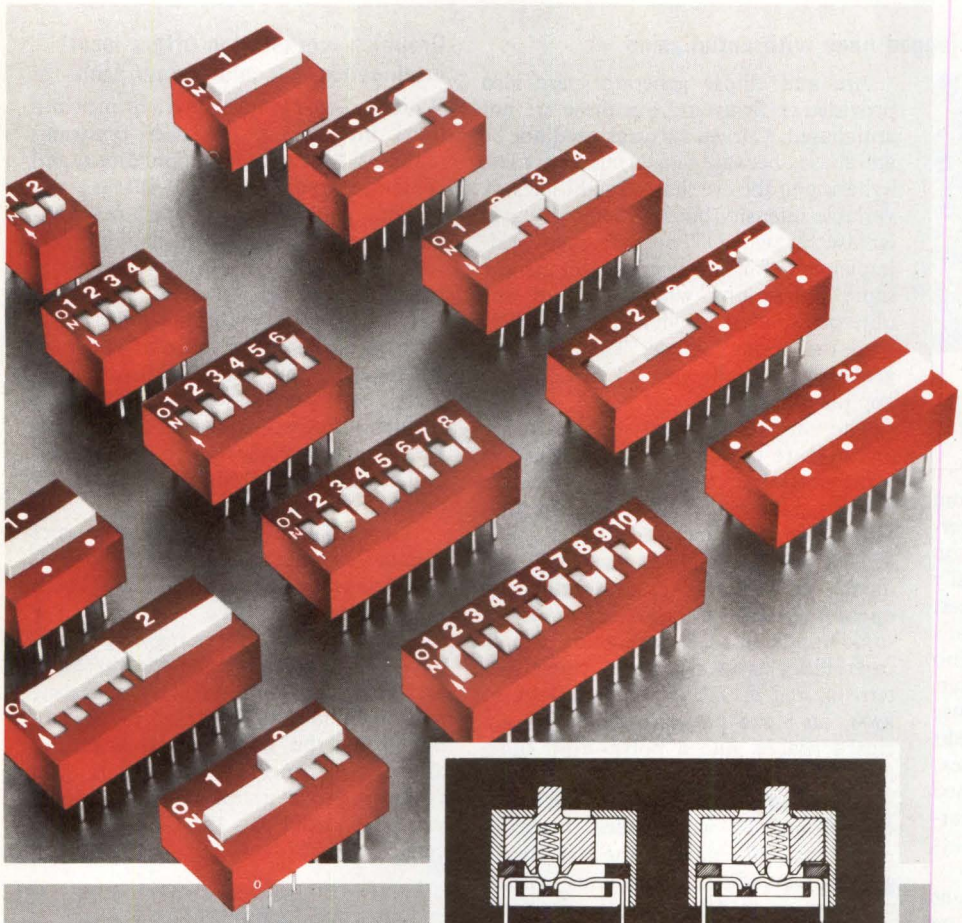
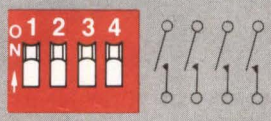
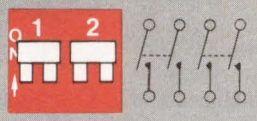


Available Circuitry

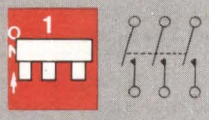
SINGLE THROW—
All "On" Positions Inline



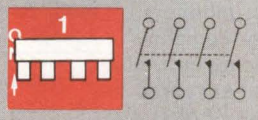
SPST, 2 - 10 stations;



2PST, 1- 5 stations;

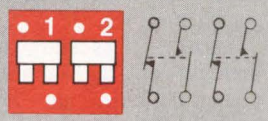


3PST, 1 - 3 stations;

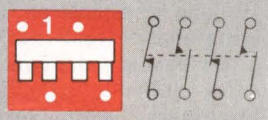


4PST, 1 or 2 stations.

DOUBLE THROW—
Alternating Side "On" Positions



SPDT, 1 - 5 stations;



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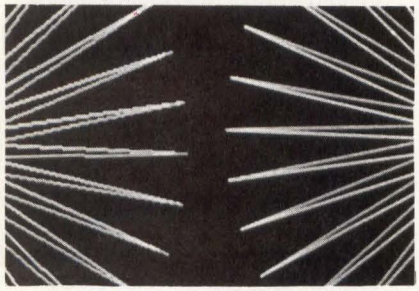
Raster graphics terminal smooths jagged lines with antialiasing



Antialiased image on right was generated by AED767 graphics terminal. It is contrasted to jagged image on left, typical of many raster terminals.

The AED767 graphics terminal from Advanced Electronics Design overcomes the problem of jagged lines on raster generated images by optically smoothing with antialiasing techniques. Images are processed by the terminal's firmware at draw time, and need no prior processing by the host computer. Total processing time is reduced because the host computer can now handle tasks apart from antialiasing routines, enabling the graphics terminal to be used for such applications as CAD/CAM, cartography, animation, and business graphics.

Antialiasing is primarily for straight lines with slopes greater than 20° where jagged lines become more pronounced. Firmware, resident in the terminal, optically blends the slopes of the vectors with the background through a process the company calls ramping. This involves a transition from one color to another in degrees, so that the two colors blend with each other. From the slope of the vectors, terminal firmware determines which adjacent pixels are to be blended, as well as the intensity, so the color of the vector gradually fades into the color of the background (usually black). Resulting vectors appear smooth, rather than jagged (Photo).

Only eight of the 256 simultaneously displayable colors can be antialiased, with 16 intensity values for each color that is used for the blending process. A color table already defined in the terminal can be used for antialiasing, or users can define their own color tables. If users do define their own color tables, they must ensure that those colors fade into the background color without clashing. The gray scale used to blend the color table is not user alterable.

Arc and ellipse generators are also provided in firmware, but these are not antialiased. Curved surfaces need not be antialiased because jagged curves are less irritating to the eye than straight lines. A variable intensity blueline reference grid is also provided. The reference grid, implemented in firmware, maintains the same dimensions when parts of the objects displayed are viewed more closely with the zoom feature. The reference grid is especially useful for layout applications.

The AED767 retains the hardware architecture of the AED512 to offer upward software compatibility, but also offers expanded memory (1k x 1k x 8-bit virtual address space) and a larger 768- x 575-bit viewing window. Such improvements allow the graphics terminal to operate at 60 Hz in interlaced mode for some applications, as well as offer such capabilities as user defined stipple patterns stored in 32k of ROM and 10k of RAM, an 8 x 8 pattern used to fill enclosed spaces, and a polygon-fill function.

Other standard features include a library of subroutines with which FORTRAN programs can access the terminal's graphic capabilities; continuous joystick panning; up to 42k bytes of RAM/ROM; support of two serial RS-232 ports and one parallel interface; and emulation of the Tektronix 4010 family for immediate compatibility with many existing programs. In addition, the terminal may be used with a digitizing tablet, as well as all hard copy devices having a standard RS-170 interface.

AED767 prices start at $18,000, depending on the number of memory planes desired. This price includes the keyboard, base unit, and 13″ std phosphor display monitor. Optional 19″ std phosphor monitors, as well as 13″ and 19″ long persistence phosphor monitors, are available from AED. The company offers OEM and discount pricing on the AED767 and all of its options. **Advanced Electronics Design, Inc**, 440 Potrero Ave, Sunnyvale, CA 94086.

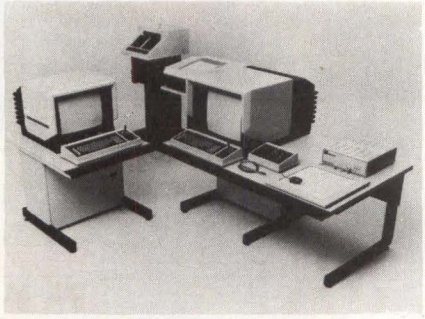
—Joseph Aseo, Field Editor

Circle 240

Graphics workstation offers local intelligence, 3-D color raster scan

Whizzard 7600 graphics system provides local intelligence for user programmability, 3-D surface manipulations, and realtime user/terminal interaction without dependence on the host computer. Incorporating multiple high performance processors for total graphics versatility, the 7600 is designed to provide realtime remote operations with central processors, including those of DEC, SEL, Harris, DG, and Univac. More importantly, an 8086 based local intelligent frontend processor (LIFE™) offloads the host computer while data are being input and manipulated, reducing dependence on the host.

Heart of the unit is the Graphics Engine™, which incorporates specialized graphics microprocessors. These processors are linked together for pipelined parallel processing of graphics data. The processors include the LIFE, and graphics, 3-D surface, 3-D transformation, and clip processors. All are linked by the dual bus architecture, allowing various aspects of graphics processing to be performed in the appropriate sequence by the required processor.



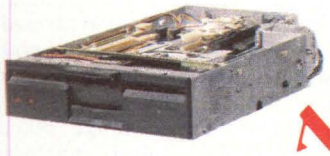
Computer graphics system combines local frontend intelligence (LIFE™), 3-D surface processsor, and several microcomputers to provide local intelligence and 3-D color raster scan in a single- or dual-user configuration.

Graphics capabilities include 8- and 16-color raster scan, monochrome raster, and stroke refresh. 4096 colors are available for 16-color applications. Either 512 x 512 or 1024 x 1024 screen resolution can be selected in raster systems. The stroke system provides 4096 x 4096 screen addressability. 3-D data address space is 4096 x 4096 x 4096. The high speed digital vector generator

(continued on page 26)

Introducing:

The new NEC FD 1165 diskette drive.



NEC

NEC Information Systems, Inc.

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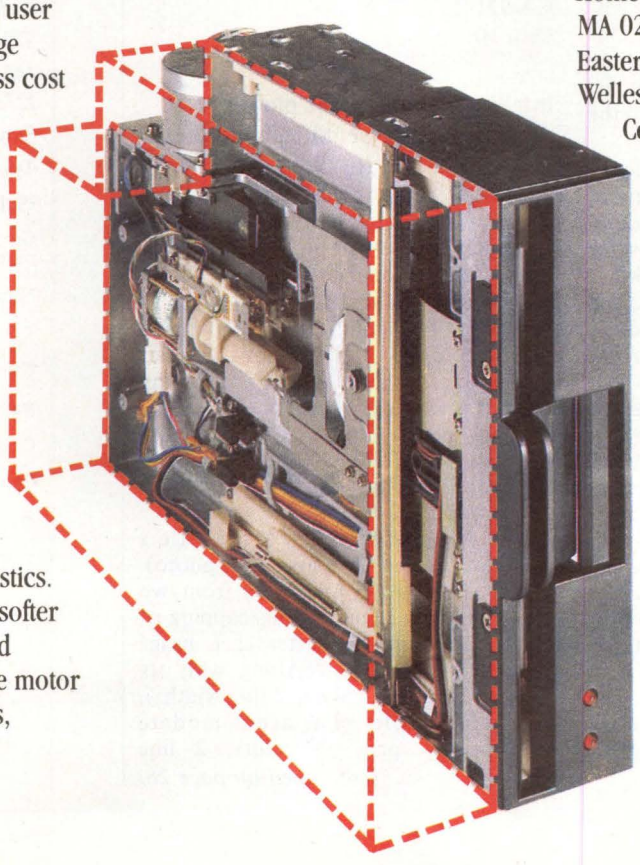
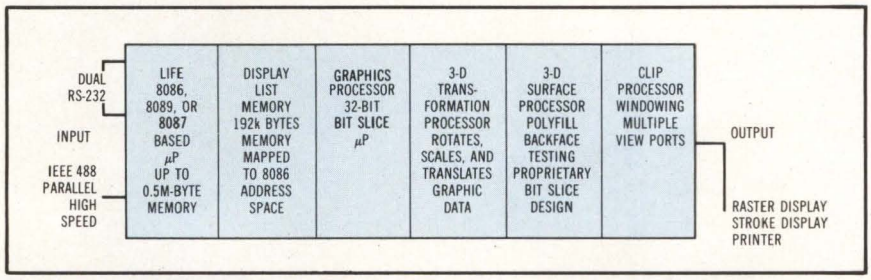
West Coast Office: 8939 S. Sepulveda Blvd., Suite 330, Los Angeles, CA 90045, (213) 670-7346



NEC's new Model FD 1165 diskette drive doubles your storage capacity—from 1.6MB to 3.2MB—without doubling your space.

CIRCLE 17



Graphics Engine in Megatek's Whizzard 7600 links specialized microprocessors over dual bus to provide pipelined parallel processing of graphics data. Output options include raster or stroke display and hardcopy printer.

in raster systems has average pixel writing time of 160 ns/pixel, enabling complex displays to be manipulated at standard 60-Hz frame rates.

Frontend intelligence on the interface is supplied by an Intel 8086 microprocessor with up to 0.5M bytes of user programmable RAM. Users can offload the host for event queuing or other application dependent tasks while achieving realtime interaction on the display. Both serial RS-232 and parallel high speed IEEE-488 interfaces are provided.

The display list memory contains 192k bytes of memory that is mapped directly into the 8086 address space. The proprietary graphics processor is a 32-bit wide bit-slice processor built by cascading eight 4-bit 2901 processors. This processor interprets vector and attribute information contained in the display list memory and controls flow of data to the vector generator.

3-D capabilities in the pipeline processing facility provide realtime rotation, scaling, and translation of graphics data. The 3-D surface processor provides for polygon fill, baseline fill, and backface testing. Any part of a line drawing can be filled to create a solid, textured, or patterned surface on both monochrome and color displays.

Polygons with up to 670 sides can be automatically filled with surface vectors; fill vectors are generated in less than 2.5 μs/vector. Fill density is programmable. Lines can be specified as horizontal or vertical, and all line styles can be used to create fills. True holes can be placed in objects to allow elements behind the hole to be seen. The clip processor allows windowing of data as required. Users can automatically fill in surface areas of both planar and curved objects without special software, extra display memory, or added involvement with the host.

As a remote graphics workstation, the unit provides high speed parallel communications via hardwire hookup to distances of 1000′ (305 m) from the host. The serial interface allows operation over standard telephone lines. Dual user capability permits two users to run different programs simultaneously.

Equipped with 8-color 19″ (48-cm) display, Graphics Engine, desk cabinet, keyboard with joystick, and WAND software, the unit costs approximately $55,000. When configured with dual workstations, 16-color raster graphics capability, remote drives, data tablet or digitizer, and dual-user hardware, price is in the $100,000 range. **Megatek Corp**, 3931 Sorrento Valley Blvd, San Diego, CA 92121.

Circle 241

Intelligent 2-pen color plotter designed for personal computers

Compatible with large and small Hewlett-Packard computers, including the recently announced HP-87 personal computer, the HP 7470 plotter can also be used with personal and business computers from IBM, Apple, and Commodore. The microprocessor based 2-pen color plotter features 2-color capability, high-resolution plotting ±0.001″ (±0.025 mm), a pen down plotting speed of 15″/s (38 cm/s) and a pen up speed of 20″/s (50 cm/s). Repeatability is 100 μm and pen acceleration is 2 Gs.

The plotter accepts 8.5″ x 11″ (21.6 x 28 cm) or ISO A4 size paper (See photo). Pens are selected by the plotter from two stalls. Automatic uncapping/capping of the pens before and after each usage reduces pen dry out. Along with HP fiber-tip pens (10 colors, 2 line widths), the pen stable can accommodate transparency pens (7 colors, 2 line

(continued on page 28)

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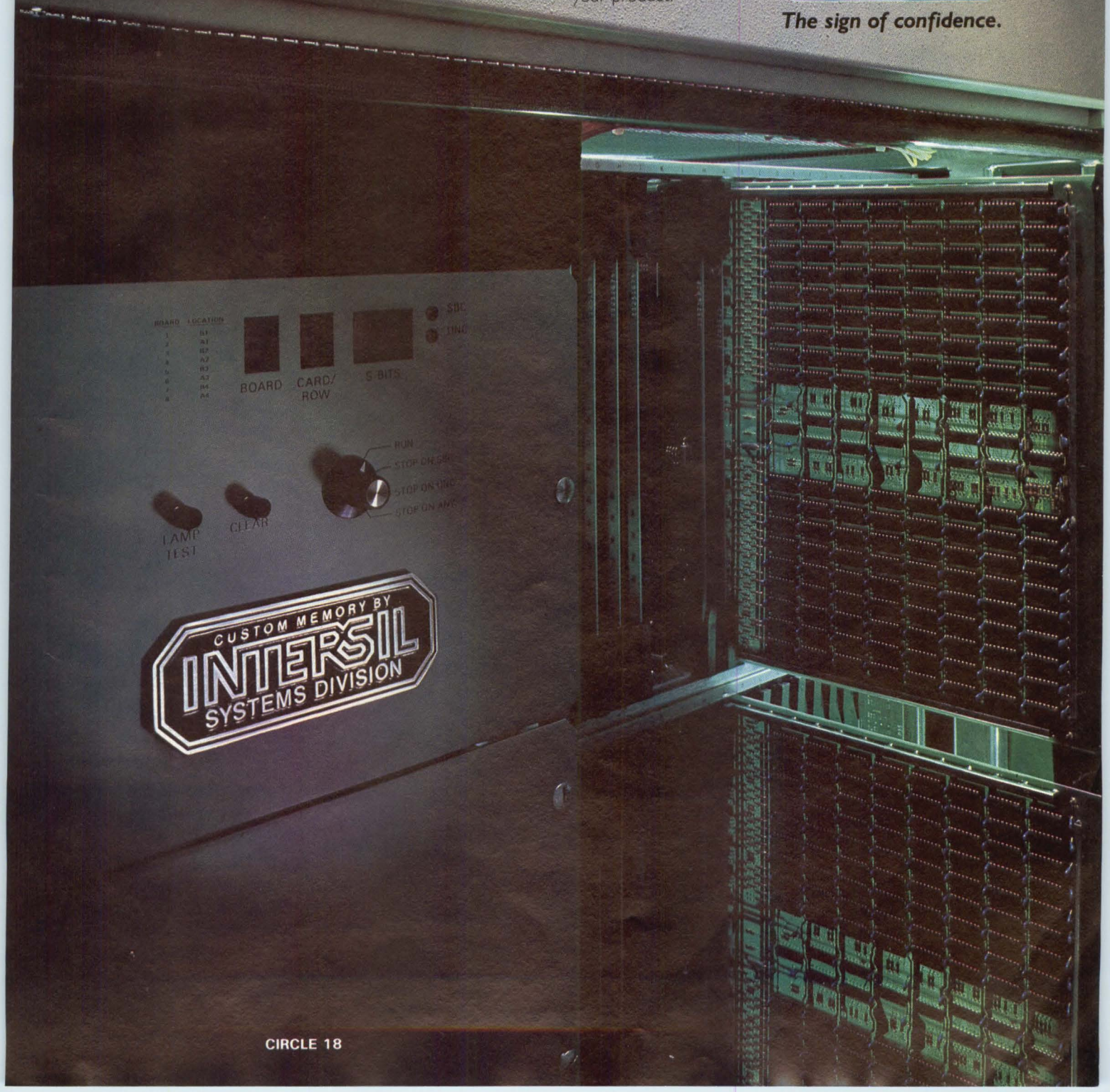
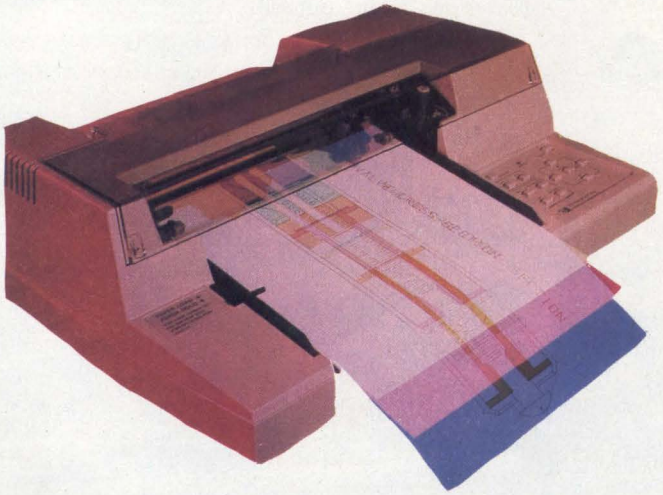


CIRCLE 18



widths) for product overhead projectors. Other features include a damping mechanism that protects the pen from damage, a variable relative velocity between paper and pen to suit special drawing conditions, and a view key that stops plotting activity and transports the paper away from the drive mechanism for review. The unit is equipped with one of two standard interfaces: HP-IB (HP's implementation of IEEE 488) and RS-232-C. It measures 17″ x 14″ x 5″ (43 x 36 x 13 cm). It requires a maximum of 25 W to operate, and is priced at $1550. It is equipped with built-in character generation, European character sets, vector plotting, and internal linetypes, and can condense, expand, enlarge, or reduce images and characters.

Hewlett-Packard graphics language interface instructions in the form of 2-letter control commands are permanently stored in the 8k-byte ROM. Over 40 individual instructions, from plot designations to pen commands, can be accessed. Eight primary ICs are mounted on the PC board: an 8-bit MC6802 microprocessor, two NMOS servo chips to drive the motors, two CMOS gate arrays, an interface LSI chip, the ROM, and a 256-byte RAM main memory (See Figure).

Use of a microgrip drive system, also used on the HP 7580A 8-pen color drafting plotter, eliminates heavy moving arms and paper transport drums and belts. This drive moves the drawing medium on the X-axis, while the drawing pen travels on the Y-axis. Inertia is minimized to include only the mass of the drawing medium and the pen being used to plot. The second pen remains in its holder.

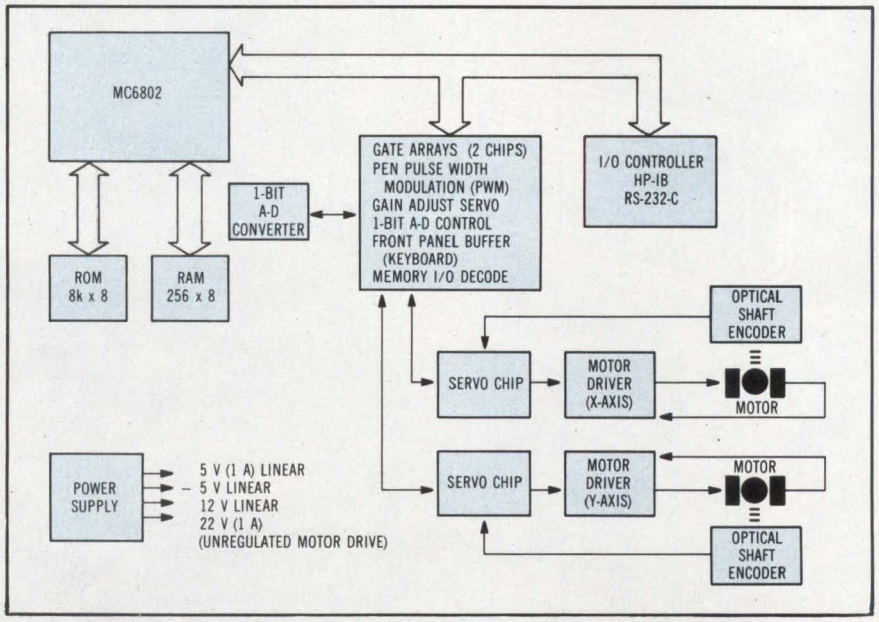
The microgrip drive consists of two rotating metal grit wheels, which hold each edge of the drawing medium firmly against a hard rubber pinch wheel. The sharp edges of the grit particles penetrate the surface of the drawing medium as it is passed through the plotter. This creates thousands of unseen microscopic indentations that realign themselves as the drawing medium makes subsequent passes through the plotter with the same grit particles that created them. Regardless of how many times the medium must pass through the plotter, the grit wheel registration pattern ensures excellent repeatability and graphic quality.

To load, the user raises a loading lever, passes the paper into the gap between the two sets of grit and rubber pinch wheels, and aligns the top and left edges of the paper with the appropriate guide stops on the plotter bed. Lowering the loading lever brings the grit and rubber pinch wheels together, firmly holding the paper between them, and the plotter is ready to go.

Two microprocessor controlled dc motors are used: one is directly attached to the microgrip drive system; the other to a belt that moves the pen. An optical encoder has been built onto each dc motor to keep track of the exact pen location. This encoder consists of an LED, a 500-slit encoder disk attached directly to the motor shaft, a phase plate, and a photo diode detector. This assembly results in a resolution of 2000 steps/revolution. Once assembled, the encoder never needs to be realigned.

As each dc motor revolves, the light emitted by its LED is encoded by the 500-slit disk and phase plate before being detected by the diode. Each of the resulting 2000 steps represents 25 μm in distance traveled by either the paper or the pen, giving a resolution of 25 μm. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 242



HP 7470 2-pen plotter. Processor implements generation of internal vectors and scaling ability. Interfaces include HP-IB, IEEE 488, and RS-232-C.

Logic Analysis System

The *PI*-540 packs virtually every measurement function you'll need in a single, easy-to-use instrument.

Advanced State Section

Up to 40 channels. Display data in hex, octal, decimal, binary and ASCII. Includes powerful qualification features, branch analysis, and 16 levels of triggering.

$7,300 (Base price)

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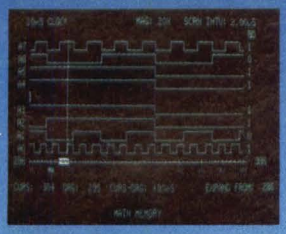
Dedicated μP probes with disassembly simplify software development tasks. *PI*-540 can accommodate 3 resident disassemblers.

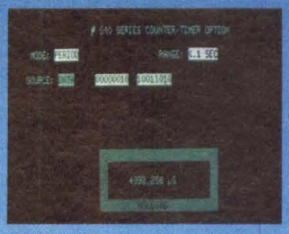
$950



50 MHz Timing Section

Independent, 8-channel, 1000-word timing analyzer with 5 ns glitch capture. Also provides 5 state display formats.

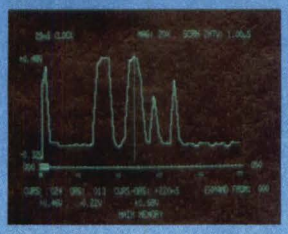
$9,500 (State and timing)



Performance Monitoring

100 MHz counter/timer measures hardware and software execution times. Includes industry standard signature analyzer.

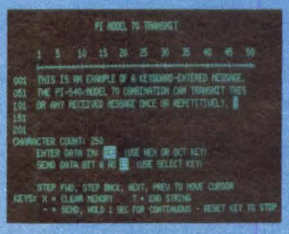
$950



Waveform Recording Section

50 MHz and 1000 samples. Waveform can be linked to other analysis sections for tracing analog and digital interactions.

$11,250 (State, timing, and waveform)



RS-232 Serial Testing

Model 70 probe converts *PI*-540 into powerful serial communications analyzer. Receive, edit, and transmit messages at rates up to 19.2 K b.

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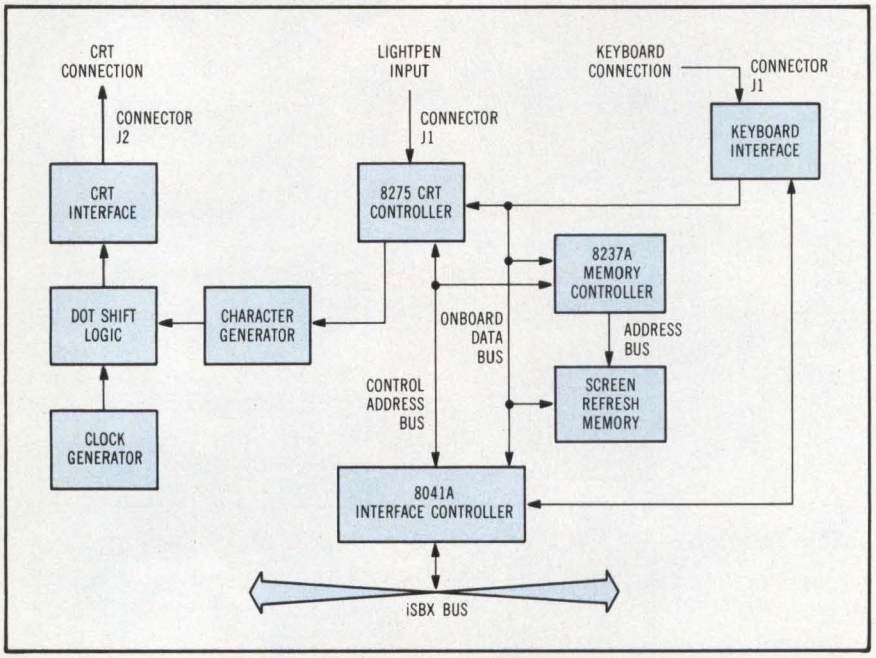
Leading the Way in Analysis Technology

The *PI*-540 resides in the expandable System 5000 mainframe. RS-232 and IEEE-488 interfaces are available.

For Additional Information Circle 19
For Demonstration Circle 25

Video display controller supports color for MULTIBUS systems



Video display controller block diagram. CRT controller and memory controller communicate with iSBX system bus via interface controller. Keyboard and light pen interfaces are also provided.

Intended to support intelligent video terminals for such applications as industrial control, word processing, and data base management, the iSBX 270 video display control, word processing, and database numeric character display of up to 256 characters for 8- or 16-bit MULTIBUS systems compatible with the iSBX™ bus. It works with any black and white or 8-color display monitor with at least 10 MHz of bandwidth, and provides either 50- or 60-Hz frame rate operation.

Combining cursor control, reverse video, blinking and underlining, the video controller has the ability to view characters in a paged or scrolled format. For black and white monitors the video controller provides TTL level signals for video, vertical sync, and horizontal sync. Two levels of intensity, normal and highlight, are also supported under program control. When using color monitors, the video controller provides TTL level 75-Ω line drivers for red, green, and blue video and sync, allowing 8 different colors to be displayed. Composite video is not currently provided on the video controller, but can be added with minimal circuitry.

Custom symbols are accommodated with the user alterable character fonts that are stored in EPROM. Any, or all, of the 128 characters already defined can be changed by reprogramming the 2716 EPROM used by the character generator; larger character fonts of up to 256 characters can also be obtained by using any compatible 2732A EPROM. Characters are displayed in either 5 x 7, 6 x 8, or 7 x 9 dot matrix patterns.

In addition to user alterable character displays, the video controller contains the 8041A interface controller that initializes and monitors such onboard components as the 8275 CRT controller and the 8237A DMA controller. This provides constant video display without interrupting the system CPU. Under firmware control, the 8041A provides communication between the baseboard and the controller circuitry via the iSBX data and control lines. Data may be displayed immediately following power-up, using default initialization information contained in the 8041A. In addition, eight high level commands are used to change the default information of the controller and determine status. Following initialization, characters are displayed on the CRT by simply writing to the proper I/O port.

Any keyboard I/O device works with the video controller via the J1 edge connector (Diagram). Up to eight TTL parallel data lines and one TTL strobe, either positive or negative, are accepted by the keyboard interface. In addition, control lines are provided for visual or audible indicators. A lightpen interface is also provided onboard the video display controller. A lightpen hit is triggered on the rising edge of a lightpen signal. This signal is recorded by a status bit on the interface controller, or by an interrupt.

Video display controller contains 4k bytes of high speed static RAM, as well as a high speed DMA controller that takes care of both writing data to the screen and refreshing the screen. It can be programmed to handle screen sizes of up to 35 rows by 80 characters wide, fits on 3″ x 7″ double-width iSBX MULTIMODULE™ board, is compatible with other 8- or 16-bit iSBC boards that support the iSBX bus, and will be supported with both the iRMX 86 and 88 drivers. All necessary timing and buffering functions are performed by the CRT controller.

The iSBX 270 video display controller, list priced at $750, is now available. OEM quantity pricing is available on request. **Intel Corp**, 520 NE Elam Young Pkwy, Hillsboro, OR 97201. Circle 243

SOFTWARE

Software tools adapt mainframe package to desktop computers

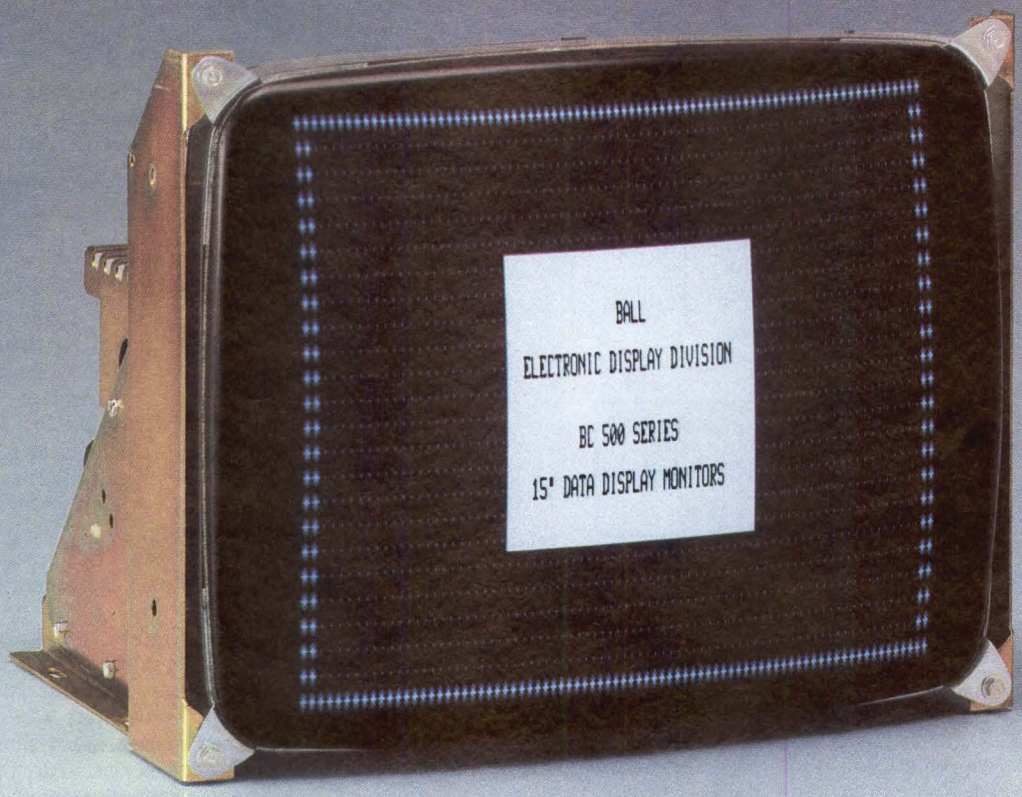
Easing software maintenance, COBOL Animator and Slideshow, make desktop computer applications user friendly. The products are aimed at making mainframe software available on microcomputer systems.

Acknowledging the growing shortage of skilled programmers, Animator enables less skilled staff members to function more efficiently. By displaying COBOL source code on the screen as it is executed, the package makes the process of correction or addition easier by making the logic of the program apparent to the programmer.

The package animates a program by displaying its source listing on the screen and moving the cursor from statement to statement as execution occurs. Programmers can run programs one statement at a time or continuously; speed can be adjusted to fit the user's most

(continued on page 32)

Introducing the BC-500. A simple display of intelligence.



Mechanical simplicity, uncomplicated circuitry, and ease of maintenance add up to a cost effective, quality display—the BC-500, the newest 15-inch CRT from Ball. But, design simplicity isn't all you get. The BC-500 gives you the features you want and the performance you have to have. Like an extended video bandwidth that assures crisp, clear alphanumeric presentation. Horizontal line rates available up to 23 kHz. All electronic components on one main circuit board for ease of maintenance.

In addition, the simplicity of the BC-500 gives you design flexibility. A variety of frames are available; wire or sheet metal frame chassis design is strong, compact and lightweight. And what's more, by virtue of the simple single circuit board, a 15-inch monitor is finally available in kit form for easy installation in custom applications.

But, best of all, incorporated into the Ball BC-500 is the experience of 20 years of design and over a million units in the field. That experience shows in the quality and reliability of each Ball product.

The Ball BC-500. High performance in a high quality raster scan display. For the 12-inch version specify BC-400. For a demonstration or information, call our nearest sales office. It's that simple.

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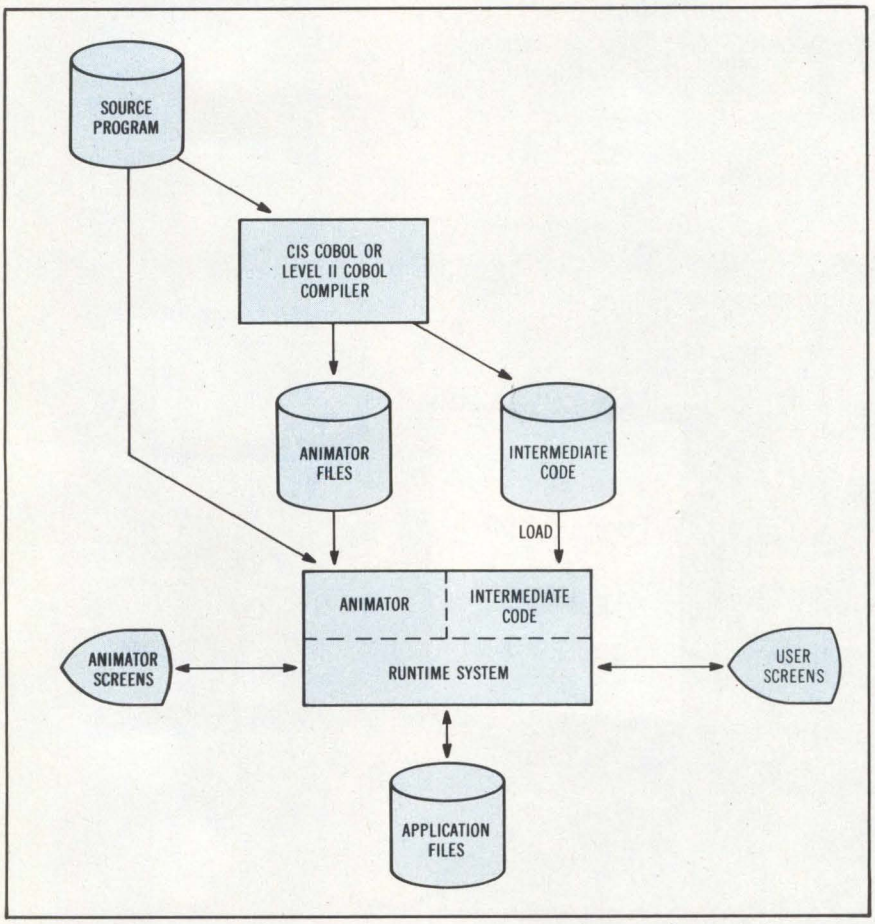
CIRCLE 20



Animator allows programmers to watch program execute, examine and change data values, and restart at any location. Package provides ability to set conditional breakpoints, find declarations, and perform immediate statement execution.

comfortable reading rate. Programs can be run normally, showing only user displays, then switched into animation mode to examine operation with a particular set of data.

Interactive debugging capabilities of the program comply with or exceed those of the GSA certification standard. During debugging, breakpoints can be set; data item values can be queried by moving the cursor to the item and issuing a simple command. Values can be changed or monitored after each statement is executed.

Providing insight into the operation of a program, the package overcomes inadequate documentation and relieves the programmer from having to flip through pages of documentation in an attempt to track the progress of the execution. It enables program maintenance—estimated to represent 67% of the life cycle cost of software—to be enhanced quickly and efficiently.

Animator can be used on any COBOL source program that conforms to the ANSI 1974 standard. It operates with the company's CIS and Level II COBOL compilers.

Self-tutorial application packages, developed using Slideshow, can guide users in operating a system or a software package. The package enables users to easily create menus, text displays, and still or moving color graphics displays. These displays can then be linked with other system elements, including application programs, and run together as a unit. This turns batch oriented applications into interactive ones.

Facilities are directly available to applications engineers and require no programming, freeing designers to configure and modify applications independently. The package treats an application as a number of discrete steps made up of display screens and individual programs linked with many alternative paths.

To use the package, the designer specifies a sequence of steps by creating a control file in which each record specifies a single step in the application. This package is currently being demonstrated on the Apple II. **Micro Focus Inc**, 1601 Civic Center Dr, Santa Clara, CA 95050. Circle 244

Standard Pascal extensions reduce cost of support for SBC-11/21

Parallel Pascal from Interactive Technology claims to reduce software support cost for DEC's Falcon SBC-11/21 single-board computer (*Computer Design*, Jan 1982, pp 26, 30). Priced at $950, the package is an ISO standard Pascal with extensions for writing multiple task programs for concurrent programming.

A multipass optimizing compiler within the package generates assembler text for the PDP-11 instruction set. Extensions that allow the creation of an unlimited number of concurrent tasks, synchronization of those tasks, interrupt handling, and direct I/O to hardware registers are included in the Pascal language superset. All this is done without using assembler language or machine code.

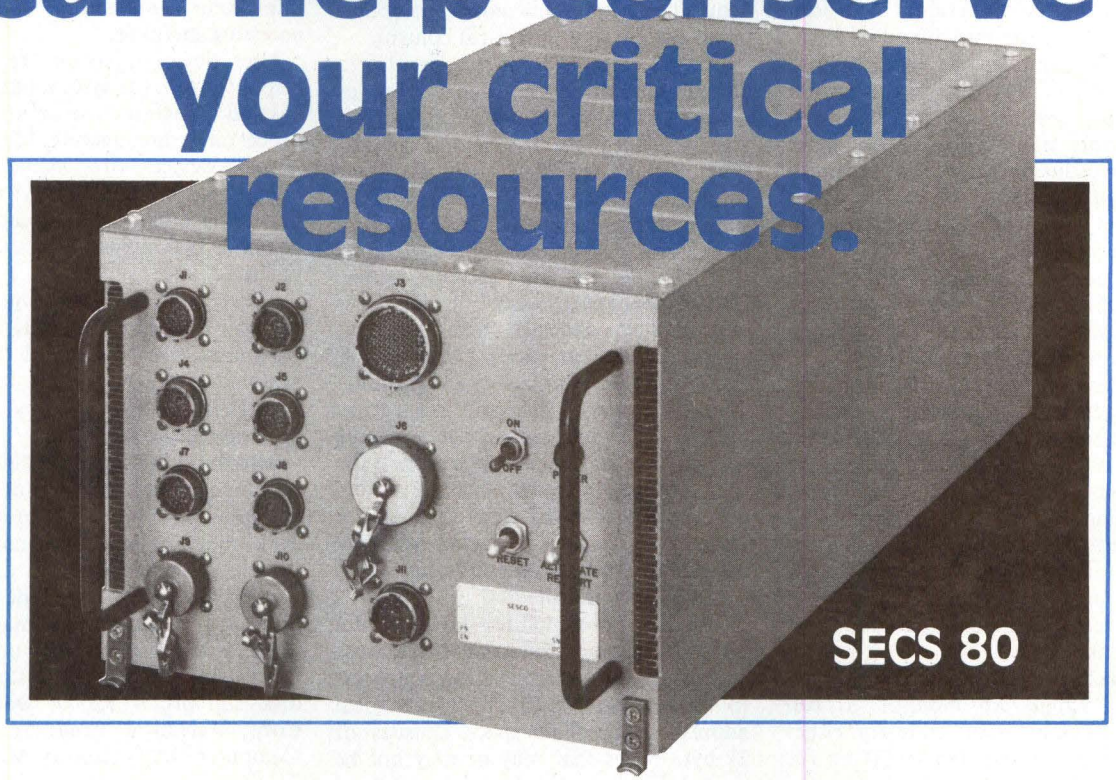
Parallel Pascal generates machine instructions, not interpreted code. The resulting speed is particularly significant for interrupts that are serviced directly under user code with no intervening system routines. All procedures, functions, and processes are reentrant; they can call themselves recursively. Subroutines can be used simultaneously by several tasks, and processes can be called many times, setting up a new task for each call.

Multiple task (concurrent) programming extensions have simple flexible parallel features. Process and interrupt define blocks of code to execute in parallel; signal is a special data type used to synchronize tasks. Others include send, wait, awaited, DOIO procedures, and fixed location declaration of variables.

Using the package, the entire application, including interrupt service and I/O,

(continued on page 34)

How EMM's Militarized Computer Systems can help conserve your critical resources.



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SECS 80, a total system including CPU, memory, I/O and peripheral expansion modules, is compatible with Intel standard microcomputer software and operating systems. Available software includes the SRMX-88 real-time multitasking Executive as well as *Fortran, Pascal, PL/M* and a *MIL-STD 1598B Jovial* (J-73) Cross Compiler.

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SECS 80 is field proven with over 1000 units in use. So why re-invent the wheel when EMM already has a versatile militarized computer system. Certainly it's far less costly than developing a system from scratch, and you'll be conserving those critical resources.

For complete details...

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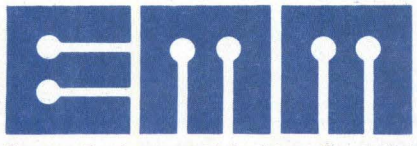
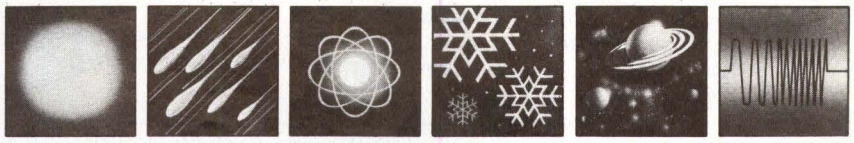


Severe Environment Systems Company
A Subsidiary of Electronic Memories & Magnetics Corporation
P.O. Box 668 • Chatsworth, CA 91311
Telephone: (213) 998-9090 • TELEX 69-1404



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CIRCLE 21

can be programmed in high level Pascal. It is also possible to program parts in MACRO-11 assembly language.

AND, OR, and NOT operators have been extended to operate bit-wise on integers. A variable can also be located at a chosen address by using the origin declaration, thereby accomplishing I/O with memory mapped devices. Read and write procedures accept an arbitrary number of parameters of varying types and convert between internal forms and character strings.

A scheduler controls switching among tasks. Scheduling is done on a round-robin basis with each task controlling the processor unit as it executes wait or send. Interrupts are treated as tasks that become active in certain conditions, and are handled by an interrupt process that is like a procedure but allows no parameter passing.

Modularity allows applications to be developed one piece at a time. System libraries can be built as modules are created. Interface to library modules is through calls; modules are loaded at system link time.

The package runs on the PDP-11 under the RT-11 single job monitor. It can generate floating point code for either the FIS or FPP instruction set. If no file I/O is done, the code produced by the compiler is completely independent of an operating system and can be put in ROM. The compiler for RT-11 is supplied on a CPU license basis. Package includes compiler, code generator, and runtime library in binary form, debugger, and support programs. **Interactive Technology, Inc**, 1225 NW Murray Rd, Suite 103, Portland, OR 97229.

Circle 245

32-Bit operating system supplies realtime performance

Advanced Operating System/Realtime 32-bit (AOS/RT32) provides realtime processing and high throughput for dedicated applications on Eclipse MV/family computers. Developed by Data General's Technical Products Div for MV systems, the package provides a high degree of control over applications, as well as the necessary tools to develop them rapidly.

A strict subset of the company's current 32-bit timesharing operating system AOS/VS, the package gives users the advantages of a development environment without sacrificing the performance required for runtime environments. Typical applications include process control, automated test equipment, data acquisition, communications, computer aided design, and numerical control.

The operating system supports up to 64 parallel processes, each having as many as 32 tasks. Multiprocessing offers users the flexibility to structure applications along logical functional lines. Modular design of the package builds in simplicity and reliability. Internal coordination and communication occur only through well-defined system routes. Independent subsystems include process, memory, and task management, as well as file system, block I/O, character I/O, and peripheral management. Straightforward system generation under AOS/VS puts only those segments needed by a particular application in the final AOS/RT32 system. Since the system uses the ring oriented architecture of the Eclipse MV/family, context switching incurs minimal overhead when processing a system call.

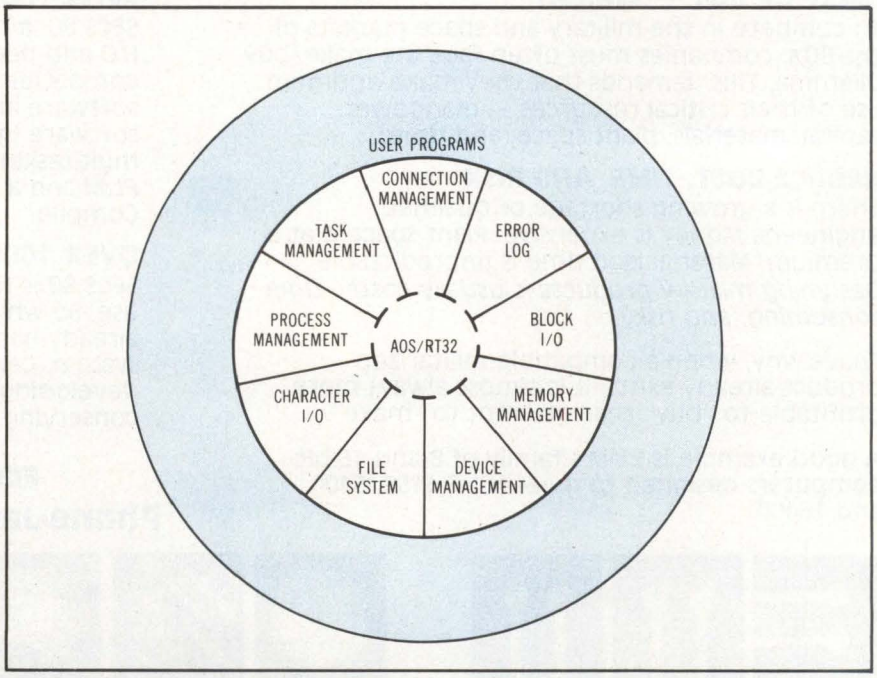
Support is provided for the maximum physical memory available on Eclipse processors. System calls allow a process to manipulate its 512M-byte logical address space. This space consists of 2k-byte pages that may or may not be shared. Formatted disks can be accessed by either AOS/RT32 or /VS, allowing the same package to be used on both systems. Unstructured disks permit users to implement application specific disk accessing methods.

User device interrupts receive quick response from the system because of the system design criteria and the processor's architecture. System supported devices are included in the operating system during system generation; user supported devices are introduced at runtime using AOS/RT32's IDEF facility.

Three high level languages are supported—FORTRAN 77, PL/1, and DG/L. Programs are developed under the AOS/VS operating system, allowing users to call on an existing library of software development tools.

Minimum hardware configuration for running AOS/RT32 consists of an Eclipse MV/family computer system with at least 256k bytes of memory, console, and system magnetic tape boot device. Supported peripherals include diskettes, disk subsystems, 9-track magnetic tape units, video displays, and printers. Initial license fee for the system without disk support is $5000. **Data General Corp, Technical Products Div**, 4400 Computer Dr, Westboro, MA 01580.

Circle 246



Independent subsystems within modular AOS/RT32 operating system are coordinated and communicate only over well-defined system routes. Only segments needed for a specific application are included in final system during system generation.

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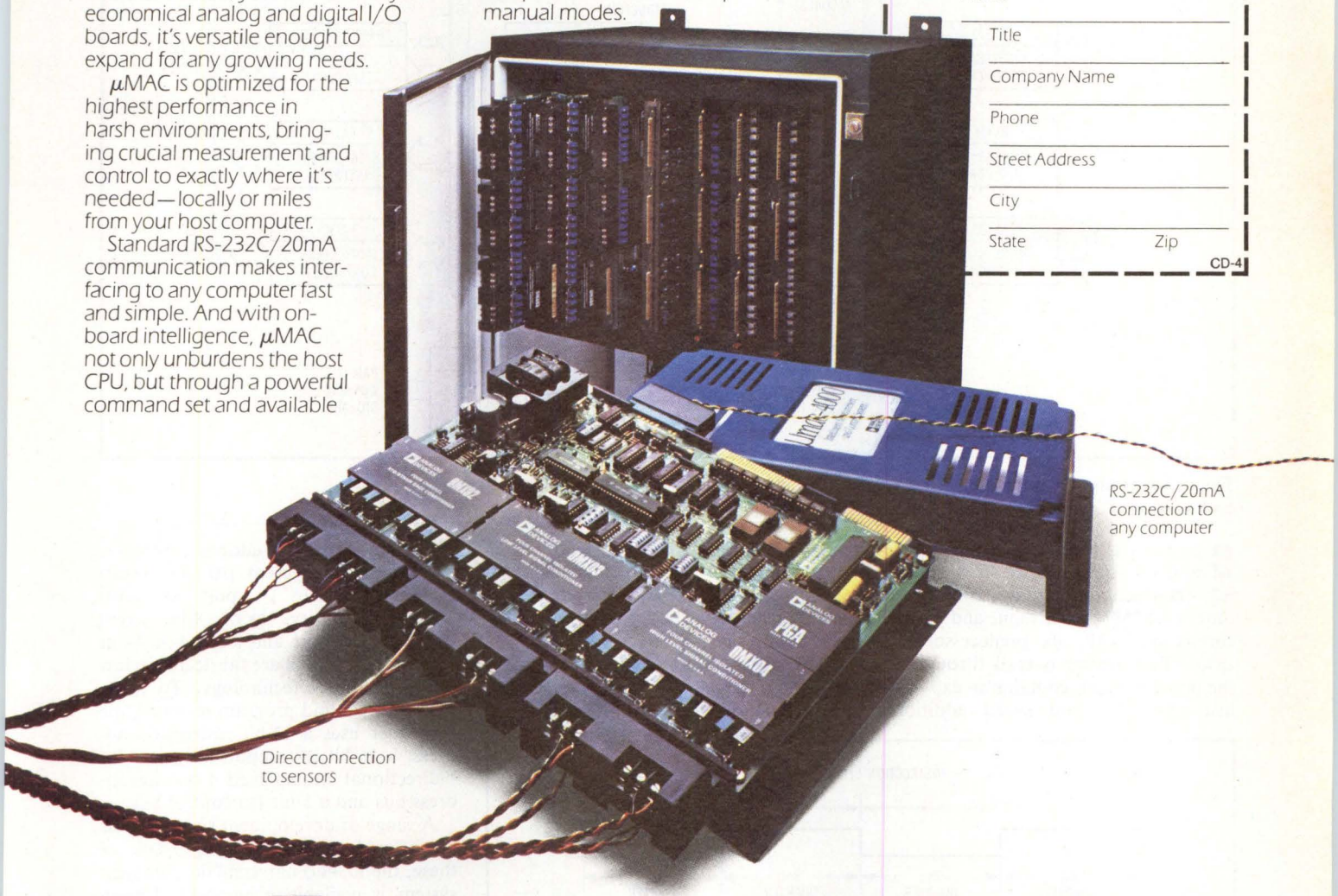

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Microcontroller with 200-ns cycle supported by seven added circuits

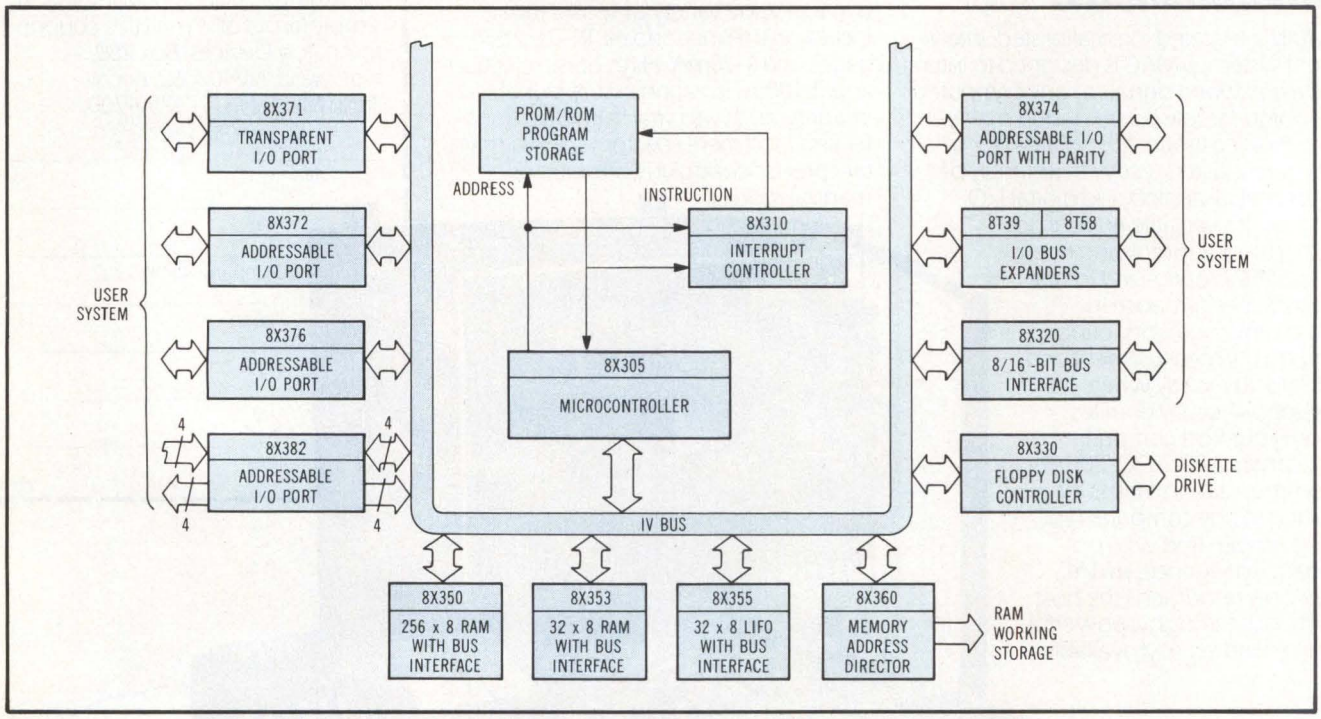

Fig 1 8X300 bipolar microcontroller family. Circuits are fabricated in low power Schottky technology. All data paths are 8 bits wide.

Signetics 8X305 microcontroller, implemented in bipolar low power Schottky technology, has a 200-ns cycle time. It is 25% faster than, and upward compatible with, its predecessor, the 8X300. To improve overall throughput, the new controller contains an expanded instruction set and seven additional registers. The part is supported by three 8X300 compatible support chips: the 8X320 8- through 16-bit I/O buffer, the 8X350 high speed RAM, and the 8X330 floppy disk controller.

Seven peripheral chips add interrupt handling, larger working storage, and parity support: 8X310 interrupt controller, 8X360 memory address controller, 8X371 8-bit transparent I/O port, 8X372 8-bit synchronous I/O port, 8X374 I/O port with parity, 8X376 8-bit asynchronous I/O port and 8X382 4-in/4-out I/O port (Fig 1). All are fabricated in low power Schottky technology. To interface with I/O and program memory, the controller uses a 13-bit instruction address, a 16-bit instruction bus, an 8-bit bidirectional multiplexed I/O data/address bus and a 5-bit I/O control bus.

A range of development support tools are offered to simplify design. One of these, the EZ-PRO universal development system, is available to support full speed in-circuit emulation. Software tools enable use of mainframe or minicomputers to generate software.

The 8X505 is the nucleus of the family. It can fetch, decode, and execute a 16-bit instruction word in 200 ns (Fig 2). Variable or fixed length data fields can be fetched, processed, operated on by the ALU, and moved to a different location within one instruction cycle. Fig 3 shows a fundamental system configuration. The 8X305 can directly address up to 8k words of program storage (ROM or

(continued on page 40)

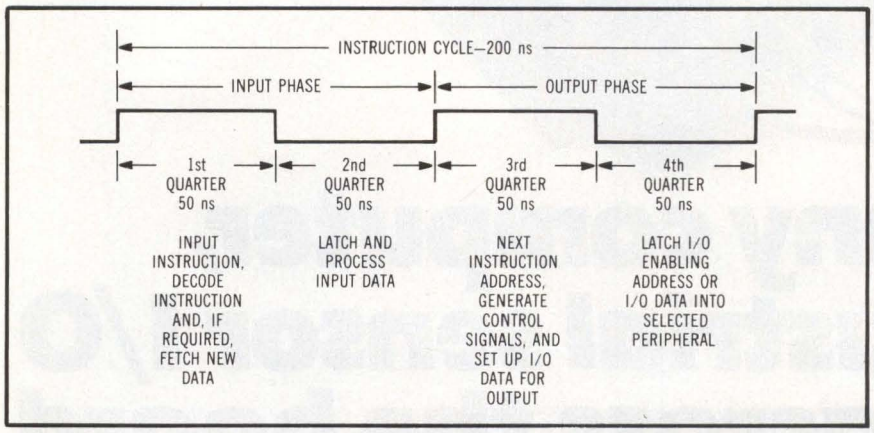

Fig 2 8X305 instruction cycle. 8-bit programming path can be programmed to rotate, mask, shift, and/or merge single- or multiple-bit subfields as well as perform an ALU operation. External data field can be input processed and output. Single- or multiple-bit data fields can be internally moved from source to destination.

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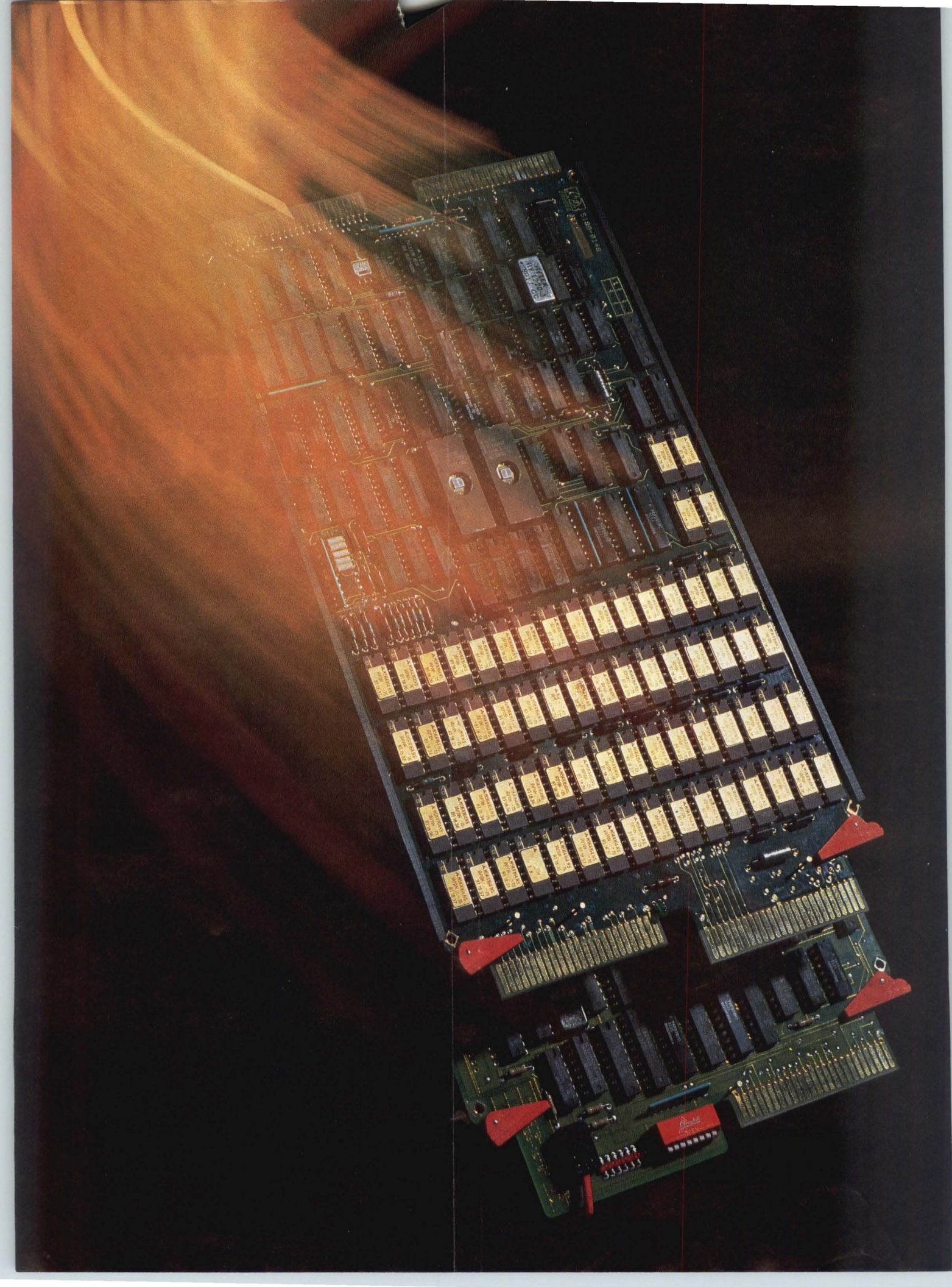

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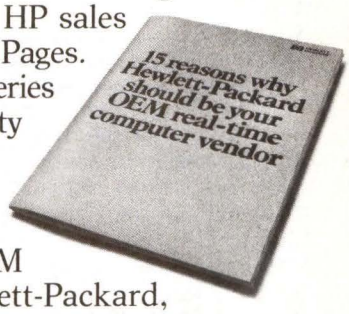

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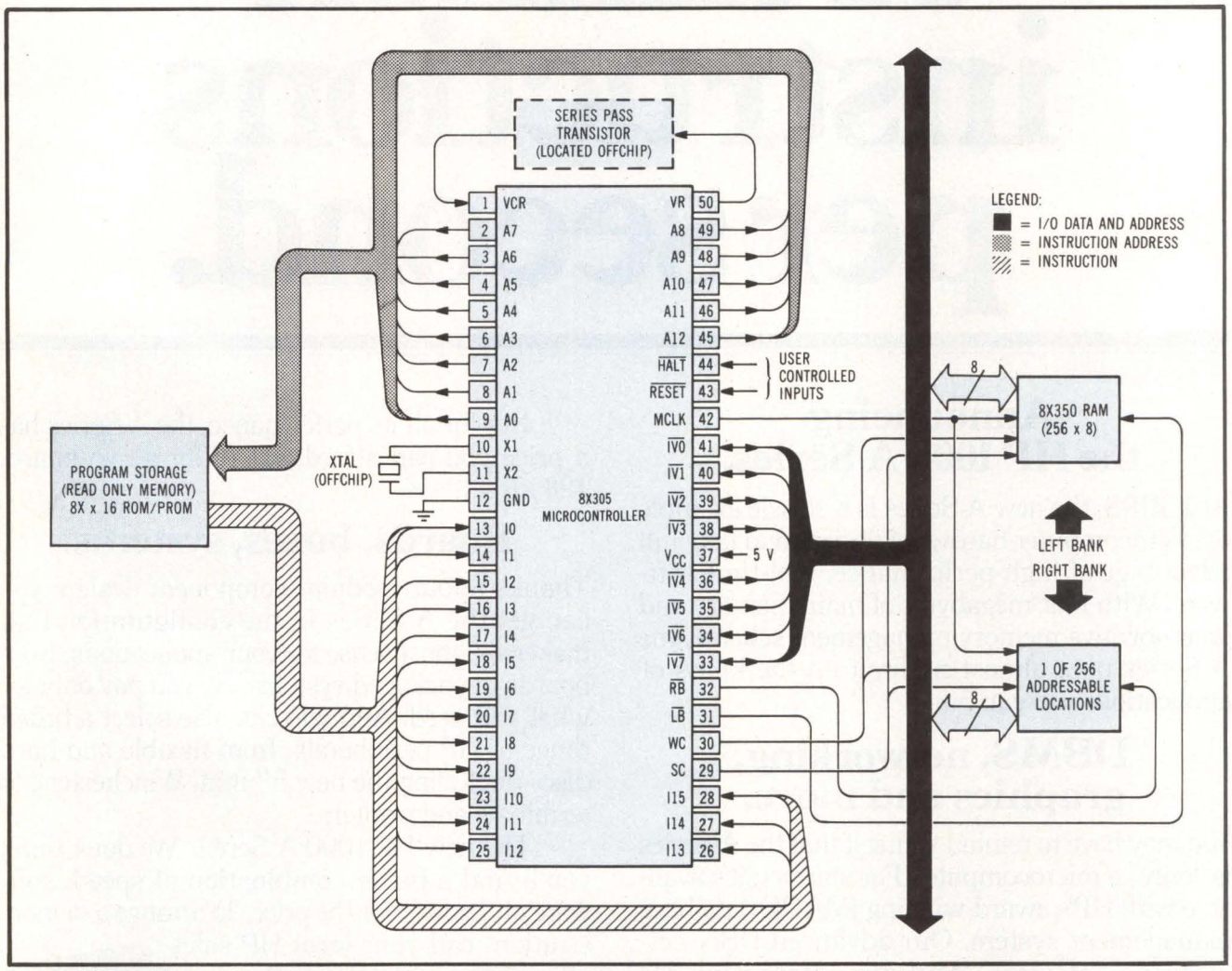

Fig 3 Fundamental 8X305 system configuration. Microcontroller addresses up to 8k words in either ROM or PROM. User interface ($\overline{IV0}$ through $\overline{IV7}$) addresses 256 I/O locations.

PROM).The user interface ($\overline{IV0}$ through $\overline{IV7}$) is capable of uniquely addressing 256 I/O locations and, with additional bank bits ($\overline{LB}$, $\overline{RB}$), is capable of expanding to 512. Each bank is composed of 256 addressable locations that can be used in a variety of ways. One method is shown in Fig 3. When $\overline{LB}$ is active low, the left bank is enabled and any one of 256 locations within the RAM memory can be accessed for I/O operations. A similar set of enable/access conditions are applicable to the right bank when $\overline{RB}$ is active low.

Program storage is connected to output address lines A0 through A12 (A12 = LSB) and inputs instruction lines I0 through I15. An address output on A0/A12 identifies one 16-bit instruction word which is subsequently input to I0/I15 and, in turn, defines the controller operation that is to follow, ie, one instruction word equals one completed operation. Provided the worst-case access time is compatible with the instruction cycle time used for the application, any TTL compatible memory can be used for program storage.

Referred to as the interface vector ($\overline{IV}$) bus, the 8-bit bidirectional I/O bus provides a link between the controller and the two banks of I/O devices. The left bank ($\overline{LB}$) and right bank ($\overline{RB}$) control signals identify which bank is enabled. When both $\overline{LB}$ and $\overline{RB}$ are high (inactive), neither bank is enabled and the $\overline{IV}$ bus is inactive (3-state).

The basic data processing path consists of the rotate/mask logic, the ALU, the shift/merge functions, onchip memory, and the bidirectional $\overline{IV}$ bus interface with its associated driver circuits and internal latches. Onboard memory and the $\overline{IV}$ bus are connected to both inputs and outputs of the ALU via internal 8-bit data paths (Fig 1). Inputs to the ALU are preceded by right rotate and data mask functions; the ALU output is followed by the left shift and merge operations. The 8X310 interrupt control co-processor enables efficient use of the microcontroller family in interrupt driven environments such as realtime control systems. In addition, the address control capabilities of the device can be used to support subroutine handling.

Five instructions are supported by the interrupt control co-processor: all are treated as NOPs (no operations) by the 8X305. Three prioritized interrupt pins for interface to the user system are included in the 8X310. When one of these pins receives an interrupt signal, the device performs two actions. First, the address of the next sequential instruction to be executed is stored in a 4-level pushdown stack in the 8X310. This

(continued on page 42)

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enables return to normal processing after the interrupt has been handled. Second, a JUMP instruction is placed on the 8X305's instruction bus, forcing transfer to an assigned memory location corresponding to the interrupt pin that initiated the action. The assigned memory location, in turn, can contain the address of the interrupt handling software. Since the device operates synchronously with the microcontroller, the actions are completed in two processor cycles, or 400 ns.

The 8X360 memory address director, designed for applications demanding large working storage and high speed data transfer, attaches to the $\overline{IV}$ bus of the microcontroller. All addresses are 16 bits in length, permitting attachment of up to 64k words of working storage through a single 8X360.

Address registers in the 8X360 are automatically incremented or decremented at the user's option. Address updating can be controlled, either from an external clock or through recognition of a specific port address on the 8X305 $\overline{IV}$ bus. The clock can be prescaled from 1 to 64 to facilitate various applications and speeds.

Designed to be as simple as possible, and require minimum microcomputer overhead, the 8X305 supplies the memory address director with a starting address and either an ending address or a block length. These addresses and/or lengths are preserved in a second set of internal registers in the 8X360 during error handling or reinitialization. As the operation proceeds, status information is maintained in an internal register and is also available to the user system through I/O pins.

The I/O port of the 8X371 is a latched bidirectional device designed for use as an interface element in systems that use TTL compatible buses. 8X371 consists of eight identical data latches—bits 0 through 7. All latches are accessed from either of two 8-bit buses—the microcontroller ($\overline{IV}$ bus) or the user data (UD) bus. Separate controls are provided for each bus and each bus operates independently, except when they attempt to input data at the same time; in such situations, the user bus always has priority.

8X372 and 8X376 are synchronous and asynchronous respectively, 3-state, bidirectional I/O ports with programmed addresses. Each I/O port is designed for use as a bidirectional interface element in systems that use TTL compatible buses. Each I/O port consists of eight identical data latches—bits 0 through 7—accessed through either of two 8-bit buses; one connecting to the controller and the other to the user system. Separate controls are provided for each bus and each bus operates independently, except when both attempt to input data simultaneously. In such a situation, the user bus has priority. Data latches are transparent in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output.

Circuitry to interface the microcontroller family to user systems that have high data integrity requirements and demand parity in the system design is provided by the 8X374 I/O port. It is an 8-bit, bidirectional device that operates synchronously with the MCLK of the microcontroller.

Operationally, the device is identical to the 8X372 I/O port, except that additional circuitry is included to enable parity checking for input data to the 8X305 and parity generation on output data. Pins function the same as on the 8X372, with four additional pins added to support the parity capabilities. These extra pins have the following functions: parity bit (input and output), parity select (odd or even), parity error flag, and error flag strobe.

When the 8X374 is being used to input data to the microcontroller, it reads 9 bits from the user bus, checks parity, and transmits 8 bits to the $\overline{IV}$ bus of the 8X305. If a parity error is detected, an error flag is latched into the device that can be tested, either immediately or at any later point prior to another input cycle. The flag remains set until the error flag strobe is pulsed. Conversely, on an output cycle, the 8X374 accepts 8 bits of data from the microcontroller, generates parity, and outputs 9 bits onto the user bus. Use of odd or even parity is a user option and selectable through a pin on the device.

The 8X382 I/O port is an addressable, 3-state device designed for use as an interface element in systems that use TTL compatible buses. Eight of the port's data latches, bits 0 through 7, are accessed through either of two buses—an 8-bit bidirectional $\overline{IV}$ bus connected to the controller, and a user data bus consisting of four dedicated inputs (bits UD0 through UD3) and four dedicated outputs (bits UD4 through UD7). All eight bits may be read from, or four data bits ($\overline{IV4}$ through $\overline{IV7}$) can be written into via the $\overline{IV}$ bus; eight bits of I/O address can be written from the $\overline{IV}$ bus. Separate controls are provided for each bus and operate independently. I/O data latches are transparent; when either bus is enabled for input, all transitions in input data are propagated to the other bus, if that bus is enabled for output.

The 8X305 is available now in plastic or ceramic and is priced at $25 in 100-piece quantities. Commercial and military temperature range versions are available. Advanced Micro Devices is second sourcing the part. Availability of other circuits in the family varies. **Signetics Inc,** 811 E Arques Ave, Sunnyvale, CA 94086.

—Douglas Eidsmore, Senior Editor

Circle 247

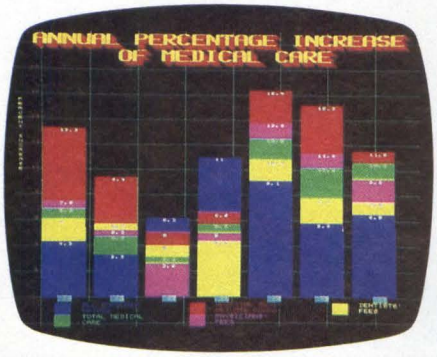
256k DRAM highly immune to soft errors

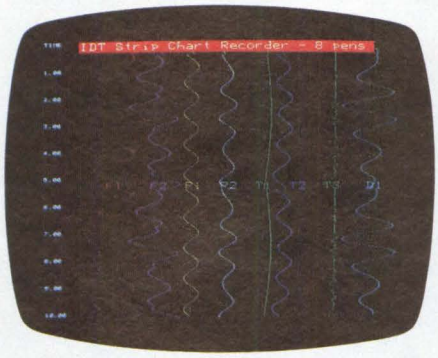
Hitachi's HM50256 will provide 256k of dynamic RAM in a standard 300-mil wide 16-pin DIP. It is implemented in double-poly NMOS with 2-μm design rules and direct stepping wafers, and appears to be highly resistant to alpha particle errors. Organized as 262,144 words x 1 bit, preliminary specifications reveal the part's performance is comparable to state of the art 64k DRAMs. For example, three versions with access times of 120, 150, and 200 ns are offered; power consumption is 300 mW active and 20 mW standby; and there are 256 refresh cycles at 4-ms intervals. Two DRAMs will be offered; one features page mode read and write operation, the other can operate in a nibble mode. In nibble mode, 4 bits are strobed out at a time for high speed applications. Primary use of the part is seen in main memory. Other characteristics of the DRAM are an on-chip substrate bias generator, common I/O using an early write operation, indefinite data out using CAS control, three refresh variations, and full TTL compatibility.

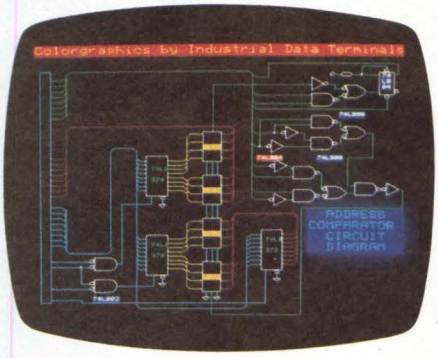
Architecturally the memory cell array is divided into four sections with horizontal metal bit lines split by 512 sense amplifiers on both sides and vertical multiword lines. This metal folded bit line structure was selected because of its superior alpha immunity, as well as lower coupling noise and larger area for memory cell capacitance. Soft errors are expected to be less than 1000 fit at typical operating conditions of 5 V_{CC} and 7-μs cycle time. This rate is obtained with normal 16-pin packaging without

(continued on page 46)

Bubble Breakthrough







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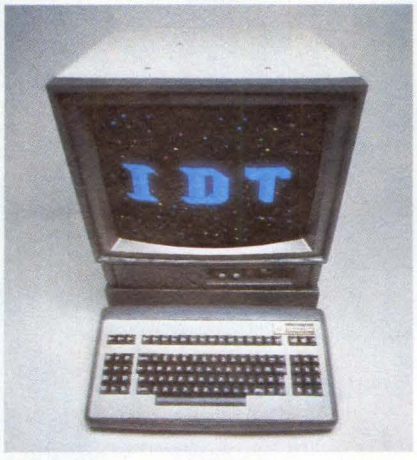

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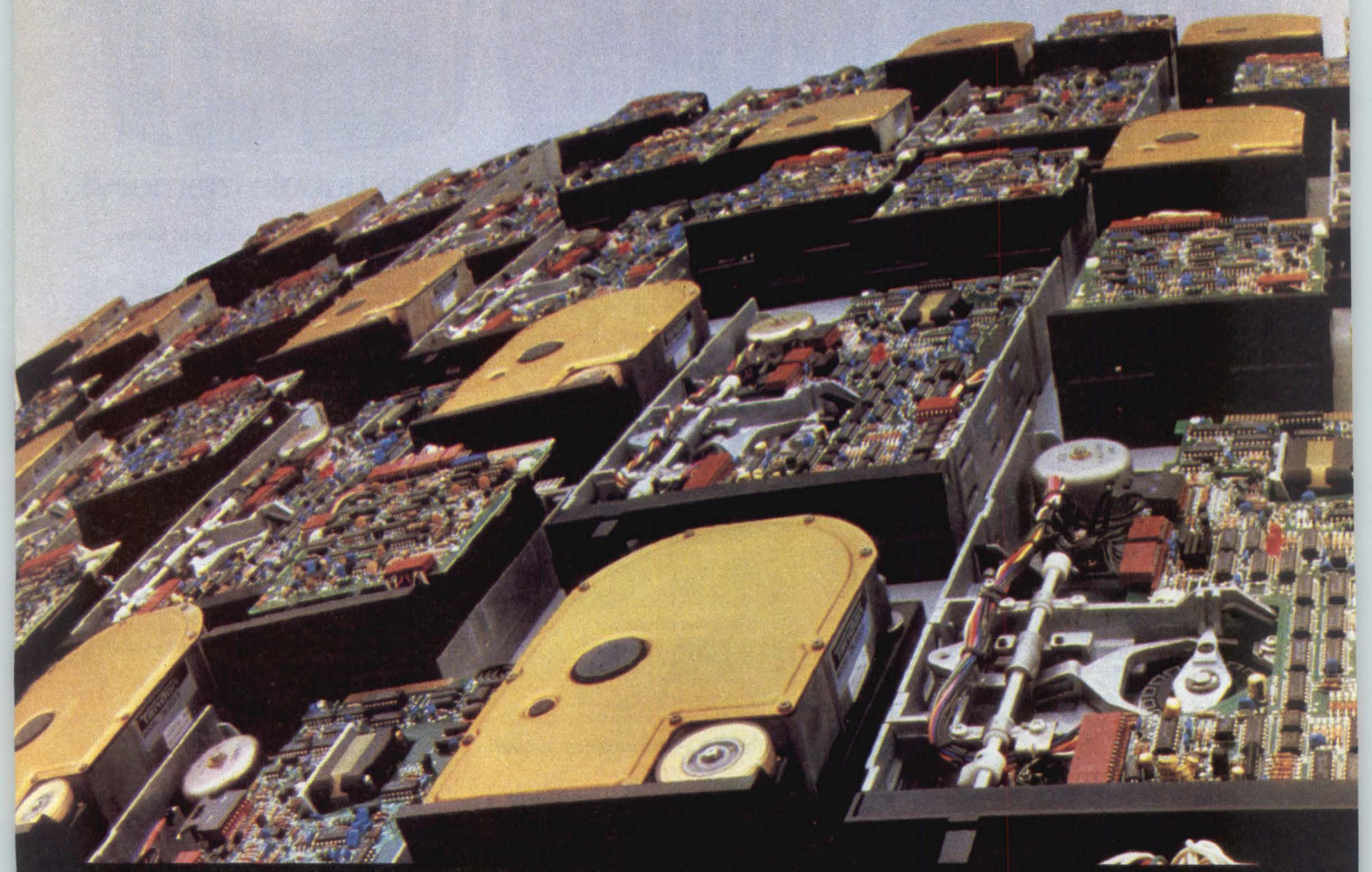

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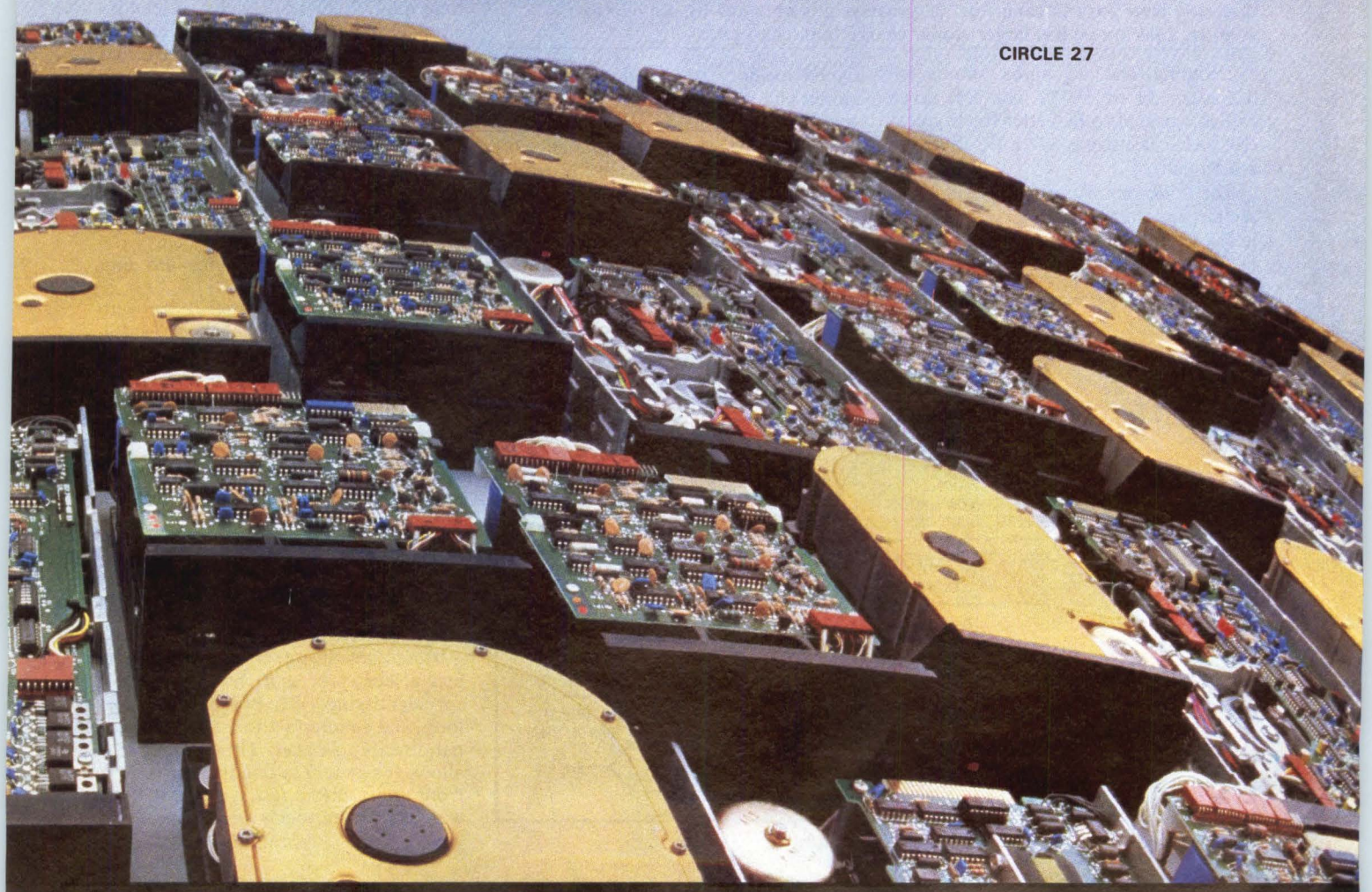

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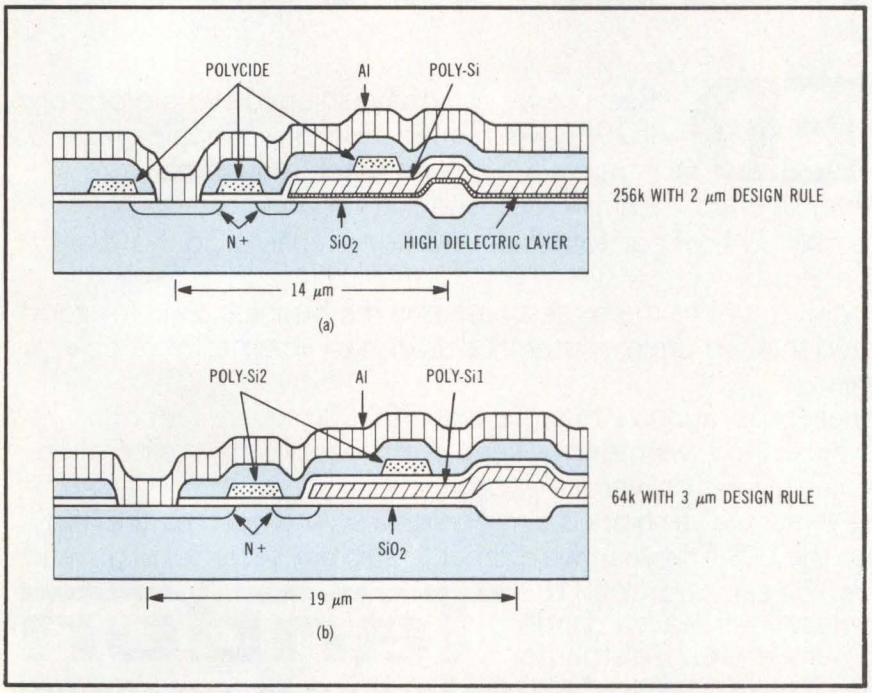


Fig 1 Cross sections of 256k and 64k RAMs. Hitachi's 256k DRAM uses high dielectric layer for cell capacitor. 2μ processing is obtained by use of wafer stepper. 256k DRAM has larger stored charge than 64k part.

overcoating and an alpha source of 0.2 α/cm^2.hr of ^{232}Th. The soft error rate is expected to be better than typical 64k RAMs. Die size is 377 x 192 mils (9.6 x 4.88 mm).

The 256k-DRAM's memory cell cross section and that of a 64k RAM are shown in Fig 1. The combination of the full V_{CC} (5 V) store circuits and the newly designed memory cell results in a larger stored charge (250fc) than a typical 64k RAMs (220fc).

To improve yield, a redundant row and column of electrically programmable fuses are built into the DRAM. Addresses of bits that are found to be defective are applied to the address pins during wafer probe testing. Fuses are blown to replace the defective bits. This procedure will improve yield by a factor of at least five. Spare row, column, and control circuitry use less than 2% of the chip area.

Operating temperature is 0 to 70 °C. Storage temperature is −65 to 150 °C. Power dissipation is 1 W. The memory part requires 5 V (±10%). Availability is expected this year. **Hitachi America Ltd,** 1800 Bering Dr, San Jose, CA 95112.

—Douglas Eidsmore, Senior Editor

Circle 248

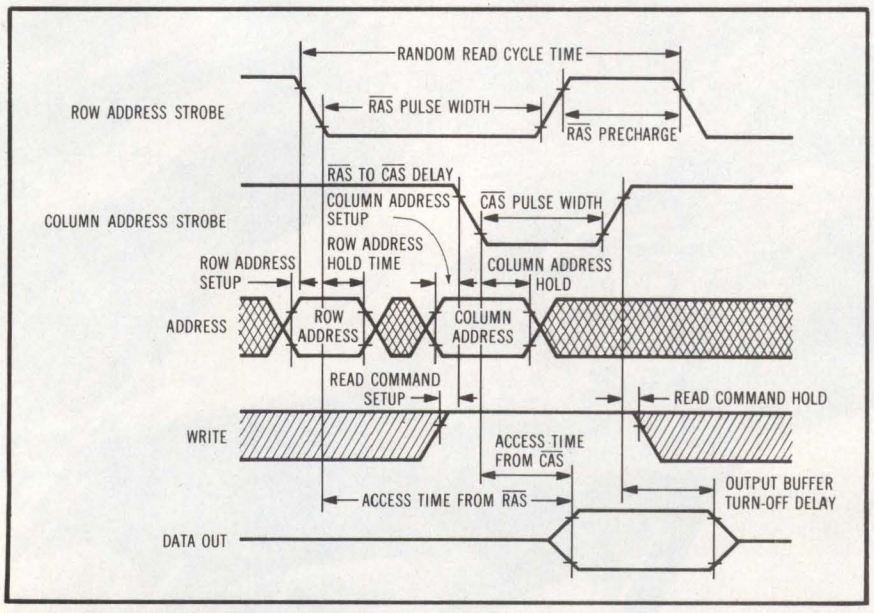


Fig 2 Hitachi 256k DRAM read cycle waveform.

TEST & MEASUREMENT

ATE control/analysis system improves PCB yields by realtime fault diagnosis

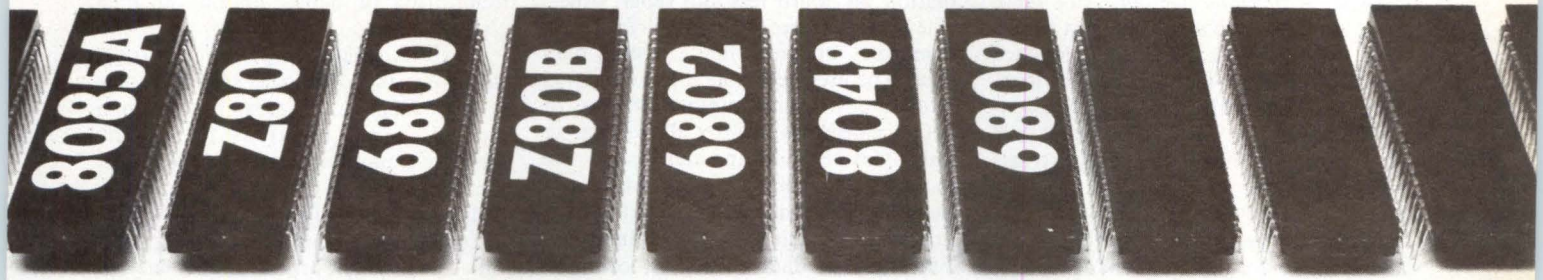
Test and repair analysis/control system (TRACS™) automatically collects test results from tester/repair/inspection and system test beds and provides real-time analysis of test results to identify critical problems when they occur. It has an accessible data base and furnishes management reports on test failures, yields, trends, and defects. TRACS uses a dedicated high performance network, and automatically transfers diagnostic/repair messages around the test loop. The GenRad system is comprised of three main hardware components: 2294 central station; GenRad designed TRACS terminals; and GRnet™ high speed data link.

Based on a PDP-11/44 processor with 1M-byte core memory, the 2294 central control station (*Computer Design*, Dec 1981, pp 104-106) contains the system central data base. All system reports are generated from this data base, either automatically or at the user's request. The 2294 can support several different mass storage devices, including 64M-, 80M-, and 300M-byte disk drives. Because the 2294 is expandable, it can address users' changing requirements. It also acts as master controller for GRnet and monitors activities and manages traffic flow across the network.

TRACS intelligent terminal incorporates a local processor, bar code reader for identifying each board in the test loop, and an interface that ties the terminal directly to GRnet. The terminal also allows the system to handle information from non-GenRad test systems. A software controlled touch screen provides a

(continued on page 48)

Applied Microsystems offers real-time emulation for:



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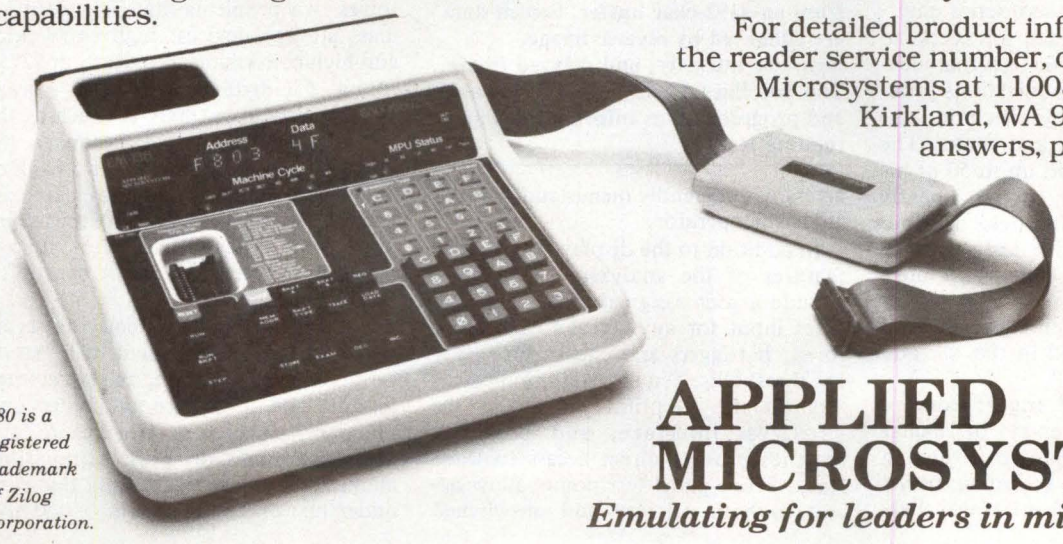

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APPLIED MICROSYSTEMS

Emulating for leaders in microprocessors.

CIRCLE 28

clean and simple user interface and eliminates the need for having keyboards or keypads on the production floor area.

GRnet (*Computer Design*, Aug 1980, p 32) is a dedicated automatic test equipment (ATE) network, specifically designed for use in a production test environment. Its high performance is an essential ingredient in TRACS, which is not only information intensive, but also sets a premium on data transfer accuracy and integrity. GRnet has a 655k-bps raw data rate. Its parallel transfer capability allows up to six simultaneous transfers, each at an effective rate of 40k to 60k bps. For accuracy the network uses the SDLC standard packet protocol with cyclic redundancy check (CRC) for transfer error correction. CRC detects multiple bit noise induced errors that are common in a communications environment.

High level system software provides menu type formats to aid in tailoring the system to specific production requirements. The software gives automatic reports on such key parameters as test trends, test result summaries, realtime warning reports, and productivity information on board test and repair times. These reports are all derived from the constantly updated online system data base. The user definable software allows him to devise any number or type of defect categories. TRACS allows him to quickly catch faults and apply corrective measures immediately, ahead of the test loop in the manufacturing process for improved quality and productivity. Paper driven data collection, common to many test systems, is eliminated.

Average cost of TRACS for a user already having three or four testers, a 2294 programming station, and GRnet is about $60,000. Deliveries are scheduled for third quarter, 1982. **GenRad, Inc, Board Test Div**, 300 Baker Ave, Concord, MA 01742.

—Jim Hughes, Senior Editor

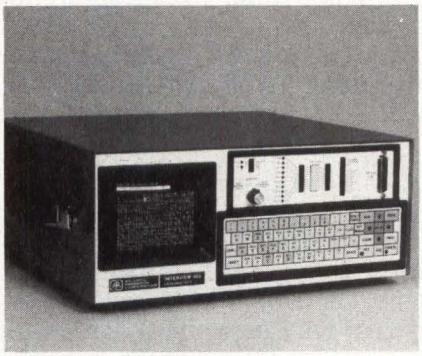
Circle 249

Data analyzer series features ASC11 keyboards, integral test libraries

Atlantic Research Corp has added three members to its INTERVIEW family of data communications test equipment. INTERVIEW 29A is the company's lowest cost analyzer with a HEX keyboard; 30A has a fully code converted ASCII keyboard; and 40A, also with the ASCII keyboard, is a fully interactive data analyzer, with bit and block BERT for sync and async. The analyzers are based on designs used in the 3500 (*Computer Design*, Jan 1980, pp 32-33) and 4500 (*Computer Design*, Jan 1981, p 39) data analyzers. The 29A/30A/40A series is operationally compatible with the more powerful 3500/4500 series unit.

A directory is provided for access to many complete diagnostic tests that identify specific data communications problems. Standard setups include 3270 Bisync, 3276 SNA, X.25, and IPARS. The user can design and add up to 50 of his own tests, which can be permanently stored or duplicated for field distribution. A fully interactive test, with 16 different continuously repeatable interchange transmissions, and the newest transmission measurement "errored seconds", are provided in the 40A and are optional in the 30A.

A simple, powerful trigger concept provides for literal entry of 8-char strings from the keyboard for trapping and selective display, including DON'T CARE, NOT EQUAL, and BIT MASK characters. User friendly menus and prompts guide the operator.



INTERVIEW 40A data analyzer. Each tester in this series has 5″ (12.7-cm) flicker free screen that displays 512 char of data and protocol sequences from an 8192-char buffer. Screen data are enhanced by reverse image, high/low intensity, and delayed freeze. Top two lines display operator prompts and program status information when running tests.

In addition to the display, front panel features of the analyzers (see Figure) include a user assigned input that provides input for any signal to be monitored. It triggers and checks for ±3-V EIA thresholds. Ten LED status indicators monitor the 10 primary leads of the RS-232/V24 interface, and breakout switches provide direct access to these leads. Front panel test points allow access to both primary and unswitched signal leads. These enable cross patching and reconfiguring of any of the primary or secondary leads. A panel mounted RS-232/V.24 connector allows uninterrupted monitoring or emulation on the data circuit.

Options include printer output, X.25/SDLC protocol trace, remote program exchange, library programmer module, and 3 (max) of 16 program memory expansion modules. This tester family is aimed at field service, tech control, and starter applications. A variety of conversion kits allow the user to start with the basic 29A or 30A, and, when network change or growth require, upgrade to the 40A.

Dimensions are 15.5 x 15.75 x 6.5″ (39.4 x 40.0 x 16.5 cm) and weight is 16.25 lb (7.37 kg). Units are supplied with technical manual, RS-232 "T" cable, power cable, and six patch cords. Prices (U.S. only) are: 29A, $2995; 30A, $3200; and 40A, $3750. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 250

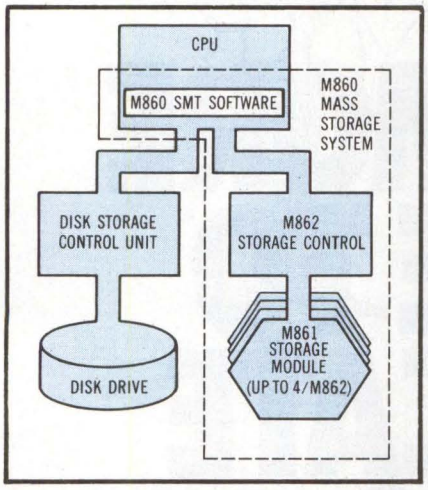
MEMORY SYSTEMS

Mass storage device stores 55 x 10^9 bytes in cylindrical fast access modules

Masstor System's M860 is a large capacity cartridge based data storage device. Each IBM compatible data cartridge has a capacity of 175 million bytes. A single storage module can store 55G bytes. A configuration with eight modules has a capacity of 440G bytes. The system is claimed to transfer data to the host processor at channel speed.

The company feels their product solves two problems that plagued prior mass storage devices: high entry price and high conversion cost. First, at $275k for a 55G-byte system, the storage system costs about half as much as the major competing device. Secondly, the user's CPU views the system as a bank of tape drives reducing the conversion cost and effort. The system also uses computer room space efficiently. A storage module occupies 10.8 ft^2; a density of 5100 x 10^6 bytes/ft^2.

The mass storage system consists of M860 storage management task (SMT) host computer software, an M861 storage module, and an M862 storage control unit (diagram). The M860 attaches to any Masstor, IBM, or plug compatible manufacturer's (PCM) CPU unit that runs under IBM operating system OS/VS2 MVS



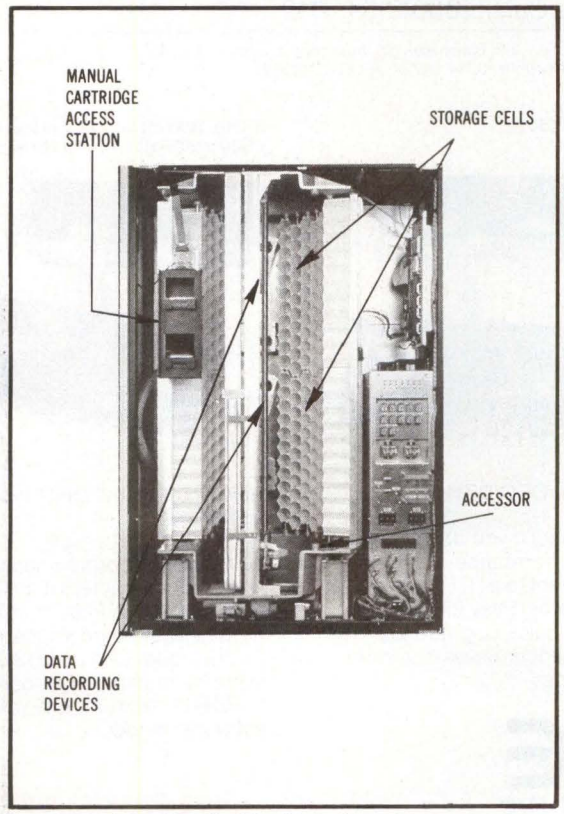
Components of the M860 mass storage system.

Release 3.7 or higher. Support is provided for attachment to single and multiple CPUs.

As with true tape subsystems, data sets stored in the M860 can be processed directly. Data can also be staged to disk, and processed like a normal disk resident data set. New or modified data sets are destaged to the M860. Staging and destaging can be done either explicitly with IBM or other standard tape to disk (disk to tape) utility programs, or implicitly by means of a direct access storage device management system. Up to four storage modules can be attached to a storage control unit. A maximum hardware configuration consists of two storage controls and eight storage modules.

The M860 SMT host program communicates with the storage control unit over dedicated control paths. Among the functions of the SMT are storing the location of every volume and data cartridge, communicating with other host processors in a multiple CPU environment, and sending high level, logical requests to the storage control. The SMT also services requests from the M862 storage control. Data are stored in the image of tape volumes. Volume manipulation, such as creation, deletion, mount, and dismount, is controlled by the SMT. The software also interfaces the MSS to operator commands. Error recovery and error statistics are other SMT tasks.

The two components of the M861 storage module are the data recording complex and the cartridge store complex. The cross section of the interior of the storage module is shown in the Photo.

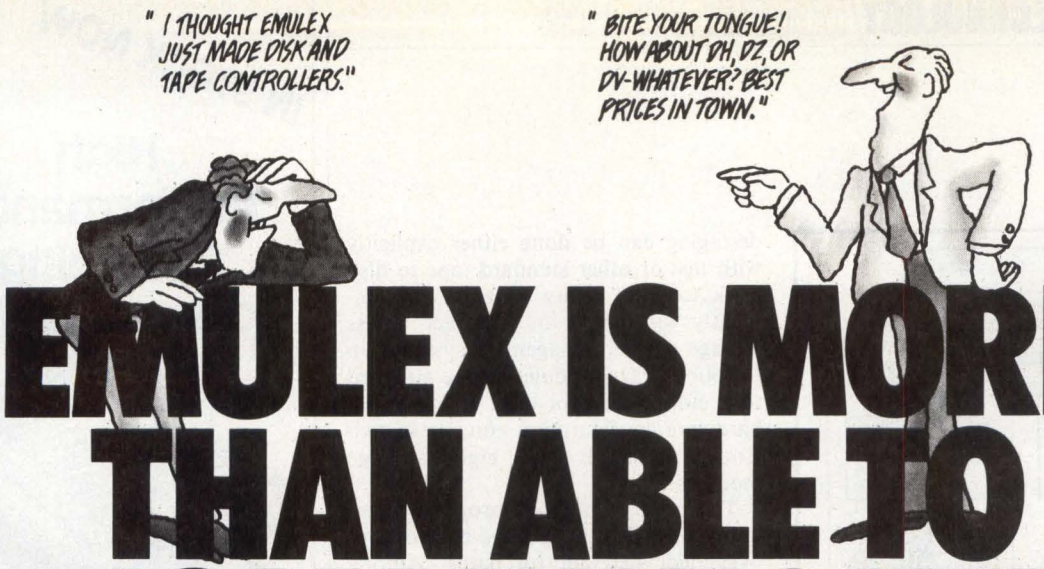


Cross section of cylindrical interior of storage module.

Data are recorded on the tape serially, bit by bit, in a series of diagonal paths called stripes. Each data cartridge contains 27,088 stripes. The first 40 stripes hold the cartridge table of contents. The remaining 27,048 stripes are available for user data.

Each stripe can contain up to 6652 bytes of data. The first 64 bytes and the last 64 bytes are reserved for internal use of the system for error checking and recovery. Each user data block or portion of a block within a stripe contains a 16-byte header and a 16-byte trailer. In addition, a cyclic redundancy check (CRC) byte is inserted after every 254 user data bytes. Therefore, the maximum number of user data bytes/stripe is 6466. The maximum

(continued on page 51)



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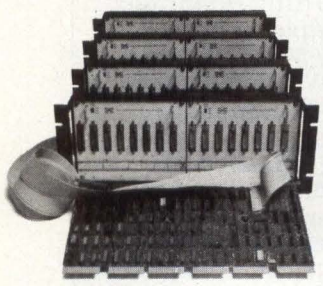
CS11/H (PDP-11) $7560 for 48 lines*
CS11/U (VAX-11) $7884 for 48 lines*



Up to 64 DH11 channels from one board.

DH11-compatible MUX lets you mix RS-232 & current loop interfaces in 8-line groups. Built-in DM11-compatible modem control. DMA output eliminates host interrupts. Self-test capabilities. Transparent to PDP-11 software. Emulex' own software on VAX.

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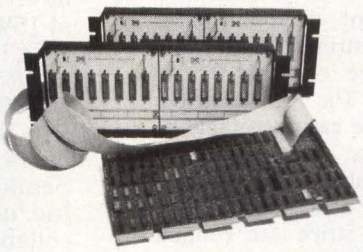

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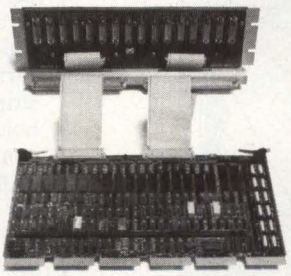

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CS21/U (VAX-11) $2844 for 16 lines*
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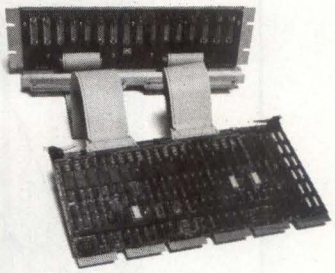

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*Price each in 100 quantities. All Emulex disk, tape, and communications products can be combined to reach quantity price breaks.

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CIRCLE 30

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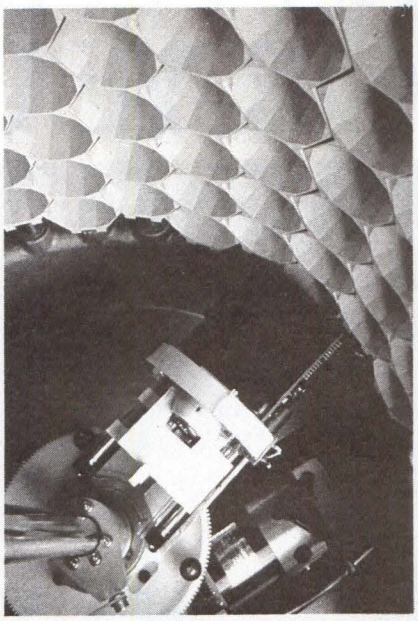

M861 storage module. Accessor travels vertically and rotates to remove data cartridges from hexagonal cells. Cartridge tape is read and written in data recording devices (DRDs). Cartridges can also be accessed manually.

user data capacity/data cartridge is 174,892,368 bytes (27,048 stripes x 6466 bytes/stripe).

The third major component is the M862 storage control. The M862 can be attached to the block multiplexer channel of these CPUs: Masstor MC/5, MC/6 and MC/8; IBM System/370 models 145, 148, 155-II, 158, 165-II, 168, 3031, 3032, 3033, and 3081; IBM 4341; and plug compatible manufacturer (PCM) versions.

Up to four storage modules can be attached to a single M862. The storage control provides a data path and a control path between the CPU and the M861 storage module, communicates with the M860 SMT operating in the host computer, and executes user channel command words. Each M862 storage control is equipped with a single channel attachment and one data recording control (DRC). The DRC can operate and control up to eight data recording devices (DRDs). Storage control options include 2-channel access, allowing the sharing of the M862; a second data recording control; and a dual data path. For purchasers of the 2-channel access option, a 2-channel access additional feature allows the M862 to be shared by up to four channels, only two of which can be on the same CPU.

The low cartridge access time (2.8 s accessor pickup and 4.6 s load and thread) and small volume of the storage system is a direct result of the design of the cartridge store complex that contains the storage cells, the manual cartridge access station, and the accessor. It accepts commands from the storage control and controls the data cartridge movement within the storage module.

Cartridges are stored in 320 hexagonal cells in a cylindrical honeycomb. Four of the cells are reserved for use by the M860 mass storage system. Therefore, 316 cells are available for storage of user data.

An accessor moves cartridges among the cell locations to the data recording devices and to the cartridge access station. The cartridge picker is located on the accessor. It travels vertically (Y direction) and swivels around the side and back walls (Z). When a data cartridge must be moved, the accessor control causes the accessor to move from its current location to the location of the data cartridge. Then the cartridge picker retrieves the data cartridge, and the accessor delivers it to the location specified by the accessor control (See Photo). **Masstor Systems Corp,** 541 Lakeside Dr, Sunnyvale, CA 94086.
Circle 251

Rotary actuator design gives accurate track following on 8″ Winchester drive

Using 3350 type heads and media, Kennedy's model 7300 stores 41.4M bytes in an 8″ Winchester drive. Improved head positioning and track following, and reduced power requirements and heat dissipation result from the unit's rotary actuator design.

In the design, a voice coil type actuator is located 2″ (5 cm) from the read/write heads at the end of the positioning arm, opposite the pivot point. Close mechanical coupling between actuator, servo head, and read/write heads eliminates inaccuracies caused by pivot bearing tolerances and arm resonance. This allows track following of ±100 μin, about half that of conventional rotary actuators. Shielding, along with a magnetic structure that is closed on both ends, keeps stray flux low.

The technique also reduces actuator power requirements and simplifies servo drive electronics. In addition, it allows the drive to operate in any position and supplies high tolerance to shock and vibration. Head positioning is done by a closed-loop servo system using servo tracks on the bottom side of the lower disk. *(continued on page 54)*

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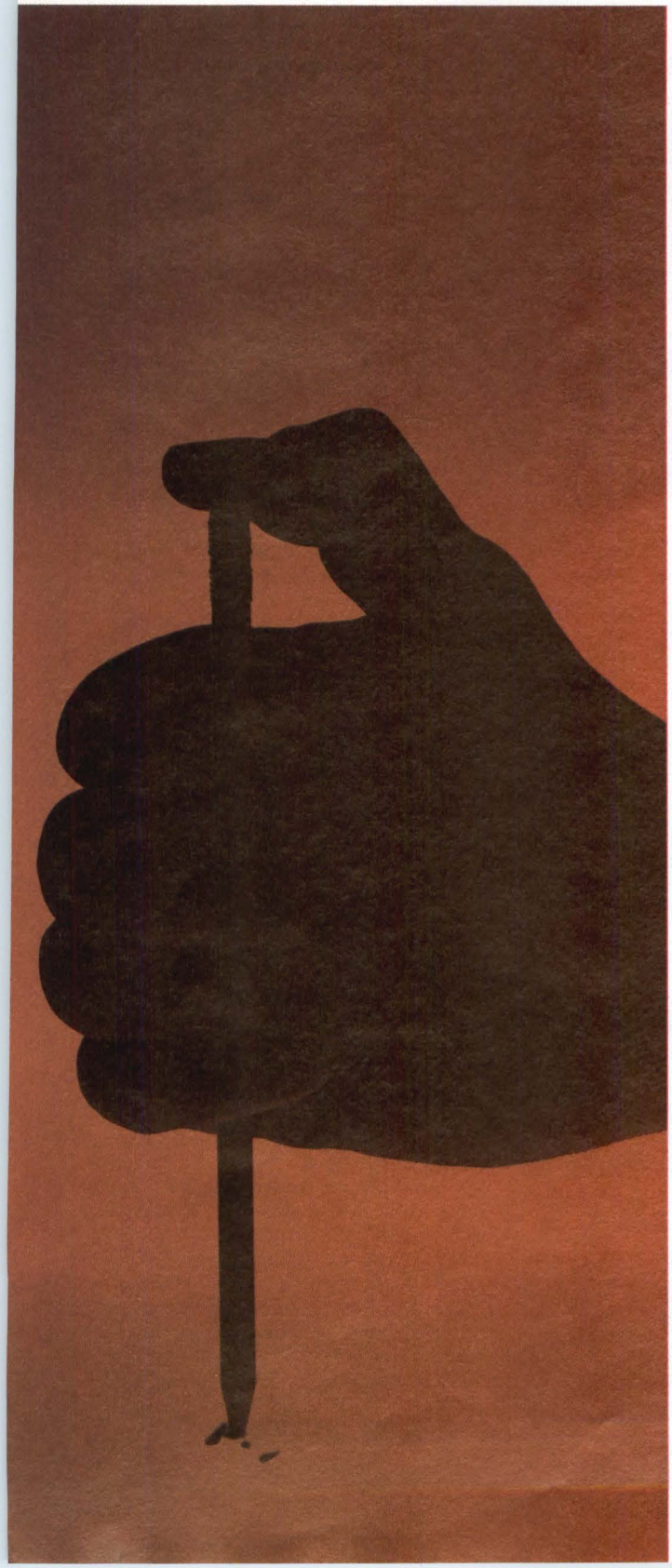

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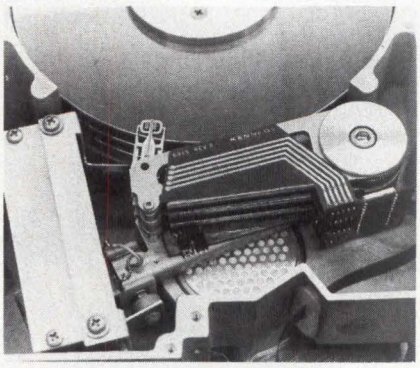
CIRCLE 32

Servo characteristics are modified according to seek length using an 8049 microprocessor with firmware. This processor determines the number of tracks the head has to move, optimum arm velocity, and establishes staircase acceleration servo signals. Calculating the distance remaining to the selected track, the processor adjusts staircase acceleration signals for the shortest seek times. Servo bandwidth is 1 kHz, reducing settling time to less than 3 ms.

In addition to drive control, the microprocessor provides internal fault detection and diagnostics. It continuously monitors spindle speed and power. Thus, it can inhibit write electronics within 500 ns, and can retract the heads and brake the motor if either should fail. Seek errors, CPU faults, read/write faults, head current, and head location are also monitored. Diagnostics include a series of seek exercise tests and microprocessor self-test routines. This combination of fault monitoring and diagnostics ensures rapid troubleshooting, resulting in a 30-min MTTR. Mean time between failures is expected to exceed 5000 h; no scheduled preventive maintenance is required.



PosiTrack actuator (lower left) in Kennedy's 8″ Winchester disk drive is located near heads to provide close mechanical coupling between heads and actuator. Design eliminates bearing tolerance inaccuracies and arm resonance, resulting in track following of ±100 μin.

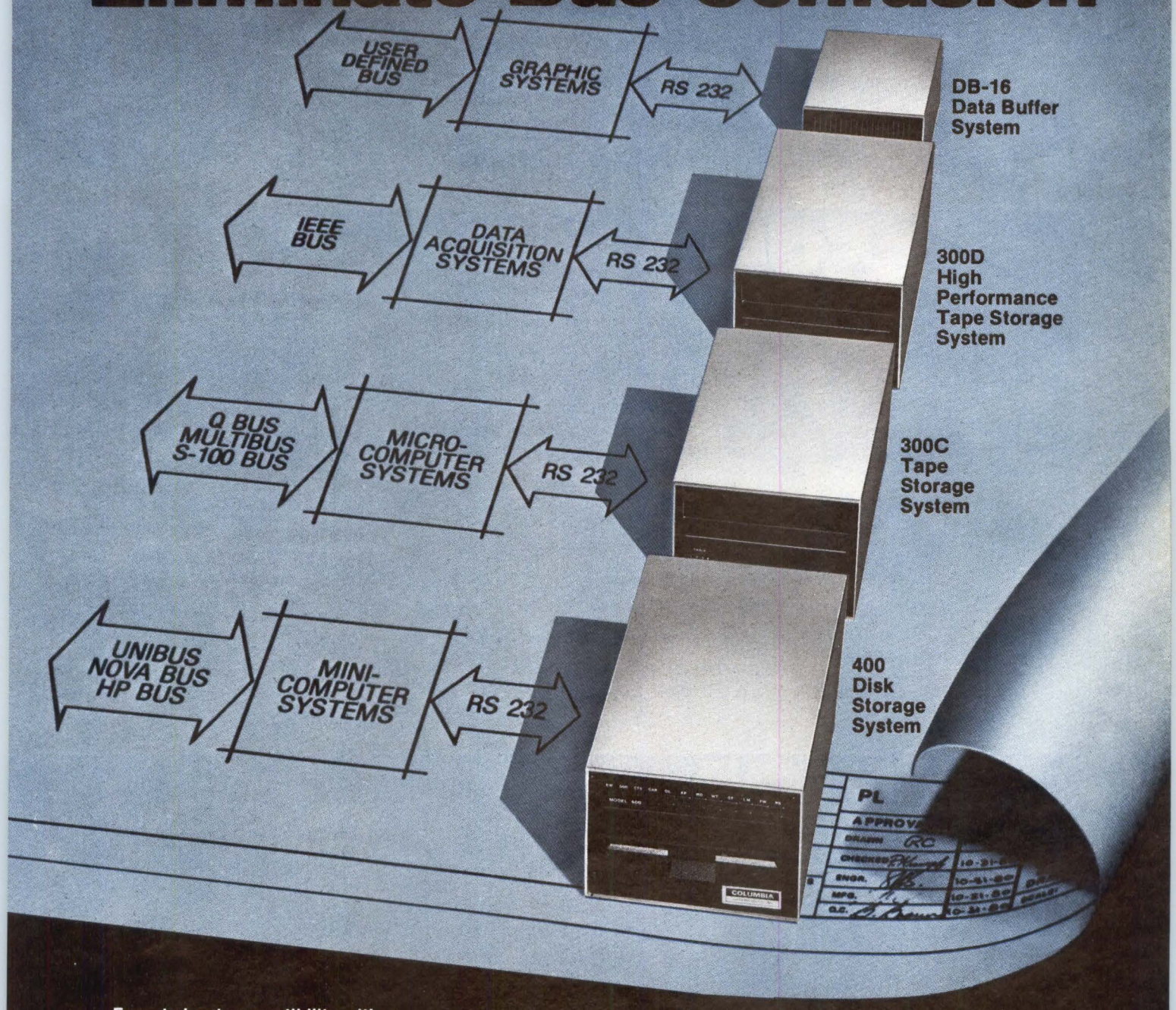
Equivalent in size to a floppy disk drive, the unit has recoverable error rates of less than 1 bit in 10^{10} and a hard error rate of less than 1 bit in 10^{12}. Format and interface compatible with CDC 9760 type storage module device controllers, it provides single track access time of 6 ms, average access time of 30 ms, and maximum access of 55 ms. Average latency is 8.33 ms based on a disk speed of 3600 rpm.

The unit uses MFM techniques with a 9.67-MHz data transfer rate. A preamplifier positioned near the read heads reduces noise for improved data integrity. Read to write recovery time is 0.3 μs; write to read recovery requires 10 μs. Bit density is 7130 bpi on the outer cylinder, 9420 bpi on the inner cylinder. The 3-disk drive has 5 recording surfaces, each with 404 data tracks and 7 spares. Heads fly 14 to 17 μin above the recording surface with a loading of 9.5 g.

The all direct current drive requires ±5, ±12, and 24 V. Maximum power consumption is 75 W. Price of the unit is $2240 in quantities of 500. **Kennedy Co,** 1600 Shamrock Ave, Monrovia, CA 91016.

Circle 252

Our RS-232 Peripherals Eliminate Bus Confusion



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CIRCLE 34

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- Buffered Printer Port
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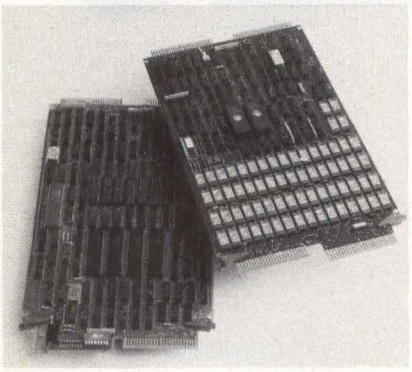
CIRCLE 35

Micro/minicomputers combine 1M-instruction/s speed with virtual memory support



Two cards form basis for 0.5M-byte computer. High performance bipolar bit-slice processor executes 1M instructions/s and includes dynamic mapping and virtual memory instructions in its basic set.

A-series machines from Hewlett-Packard match realtime industrial automation needs with I/O capabilities that supply a real world interface. Based on bipolar bit-slice microprocessors, the systems combine processing speed with networking, database management, and graphics software. Both the A600 microcomputer and A700 minicomputer process more than 1M instructions/s. This processing power is put to work by the RTE-A.1 operating system to supply realtime response in a multiprogramming multi-user environment.

Common to both of Hewlett-Packard's new machines is the ability to handle up to 4M bytes of main memory and up to 200M bytes of mass storage. Implemented using 64k dynamic NMOS RAMs, main memory has a 454-ns cycle time.

CPUs are implemented with four Schottky bipolar bit-slice microprocessors. The A600 microcomputer is horizontally microprogrammed with a 56-bit microword format that provides high parallelism and increased performance. The A700 is vertically microprogrammed with a 32-bit microinstruction format that facilitates user microprogramming. Both processors make use of programmable components, PROMs with built-in registers, and advanced Schottky technology to achieve high performance at low cost.

Distributed intelligence architecture places a separate I/O processor on each interface board. Implemented using proprietary SOS chips, the I/O coprocessors give every I/O board direct access to memory. This not only reduces CPU overhead and simplifies I/O programming, but also increases overall I/O bandwidth. Resulting bandwidth is 4.3M bytes/s for the A600 and 4M bytes/s for the A700.

Remote operating capability is supplied through a ROM based virtual control panel program. This permits VCP operators to examine and change contents of registers and memory locations, control program execution, and select a bootstrap loader and initiate system boot. The VCP can also be used for remote isolation of system faults. A microcoded self-test within the processor, on power-up, first checks the CPU and then passes control to a ROM based macrocode test that checks processor, memory, and I/O system.

Although the A700 minicomputer provides the same basic features as the A600, an optional computation acceleration processor (CAP) supplies higher speed calculations than are possible with firmware or software in the basic unit. CAP packages floating point processor, scientific instruction set, and vector instruction set firmware in three separate chips on a single board. The FPP has scientific and vector sets that provide 6 to 12 times faster floating point math, trigonometric and transcendental calculations up to 31 times faster, and 8 times faster vector and matrix arithmetic. It also supplies space for 2k words of user microcode PROMs. With single precision, the FPP can perform 308,000 conversions/s; more than 190,000/s in double precision.

The scientific instruction set puts the FPP's execution speed to work on the trigonometric, logarithmic, and transcendental functions required in scientific and engineering calculations. Single precision SIS speeds range from 35,000 hyperbolic tangent calculations/s to 57,000 square root calculations/s.

The machines execute the same base instruction set as other HP 1000 series machines. Except for dynamic mapping, virtual memory, memory reference, and I/O, other instructions have the same mnemonics and format facilitating program transportability between systems in the family.

In addition, the RTE-A.1 operating system supports programming in Pascal, FORTRAN 77, BASIC, and MACRO-1000 assembly languages. Virtual memory addressing enables programs to transparently access data arrays up to 12.6M bytes, stored either on disk or in main memory. An extended memory area feature promotes fast processing by permitting up to 2M bytes of data to reside in main memory at any one time. Each of up to 15 EMAs can be shared by as many as 32 different programs.

(continued on page 60)

In desktop package, A600 microsystem integrates up to 3M bytes of main memory with mini-floppy and mass storage, terminal, and hardcopy output. System supports realtime networking and graphics software.

VICOM

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The A600 is available as board level components, packaged rackmount computer, self-contained tabletop system, or as an integrated microsystem in desk height or 1.5-m vertical cabinets. The A700 is offered as a box computer or fully integrated into a choice of cabinets. Paraphraser, a microprogramming package available as an option for the A700, simplifies writing user microcode. This Pascal like language helps users develop microprograms that optimize system performance or focus the instruction set on special applications. Both computers support various HP 1000 series peripherals, interfaces, and HP instrumentation. Storage options include a 5.25″, 4.6M-byte Winchester drive, as well as 16.5M-, 28.1M-, and 65.6M-byte drives.

A board level A600 with 128k bytes of memory and built-in memory controller sells for $3400 in single quantities; $2448 in 100-piece units. In a rackmountable 18-slot chassis with power supply, the A600 with 128k memory sells for $7500. An 18-slot chassis with A700 CPU board and 256k-byte memory board carries a tag of $9700; with the optional computation acceleration processor, this unit sells for $14,000. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 253

Eurocard form factor microcomputer cards implemented with CMOS components

National Semiconductor's SERIES/800 board line is implemented on 3.9″ x 6.3″ (10.0 x 16.0 cm) Eurocard format boards with P²CMOS™ components. Since CMOS components means that boards are frugal and fast, power dissipation is 0.24 W and frequency is 2.5 or 4 MHz. True low power dissipation allows installation of the circuitry in sealed enclosures. Low power also means higher reliability. System costs can be reduced since cooling fans and filters are not needed, and battery backup of volatile memory is accomplished cheaply. An integral voltage regulator allows the system to be powered by unregulated dc which, in many applications, already exists, thus negating the need to purchase a power supply. Highly resistant to vibration and corrosion, the board's positive contact connectors are more reliable than cardedge connectors. Characteristic of CMOS, the boards are rated at −40 to 185 °F (−40 to 85 °C), allowing them to be installed in harsh environments.

CMOS and ECL Gate Array Comparison

Parameter	CMOS Gate Array	Standard CMOS Gate
Power dissipation (10 MHz)	0.2 mW	5 mW
Propagation delay	3 ns (typ)	8 ns (typ)
Parameter	**ECL Gate Array**	**ECL gate**
Supply current	2 mA	4 mA
Gate delay	1.5 ns (max)	2.9 ns
Interconnect delay (3 levels of logic)	≅ ons	3.0 ns
Total	1.5 ns	≅ 6 ns

The NSC800 8-bit microprocessor is the heart of the board line. This CMOS microprocessor has 158 instructions fostering efficient programming. NSC800 executes the Z80 instruction set which protects software investments. Other characteristics of the microprocessor are a typical power dissipation of 50 mW, a memory address of 64k, five interrupts, and power save onchip. The microprocessor is supported by three company products: the STARPLEX II development system, the NSC800 ISE emulator, and the NSC800 evaluation board. It is fully militarized to MIL-STD-883B.

Initial NSC800 offerings are CPU boards available in 3 speeds, RAM or PROM memory boards, serial and digital I/O boards, and A-D and D-A conversion boards. Two card cages in different sizes are also available. Support boards include voltage regulators, battery chargers and prototyping, and extenders. Realtime OS and firmware monitors are also offered to support the line.

A comparison of the SERIES/800 CPU board with similar MULTIBUS and STD BUS boards is shown in the Table. A more specific implementation comparison has been released. A system requiring CPU, RAM/PROM, digital I/O, and A-D and D-A channel boards was solved on paper, with both systems. The MULTIBUS system required three boards, a modified cabinet and the installation of an uninterruptible power supply, cooling fan, vent, and filter. The SERIES/800 required six boards and none of the extras. Power dissipated is 115 W for the MULTIBUS system and 18 W for the SERIES/800. Under one battery the SERIES/800 would operate for 24 h, and the MULTIBUS system for 1 h. Total costs are similar: $4560 for the MULTIBUS solution; $3930 for the SERIES/800. Of course, the above comparison stresses the advantages provided by the CMOS Eurocard board, ie, low power and compactness.

Applications for the board line are seen in controllers, robotics, pipeline monitoring and control, alarm systems, and engine monitoring and control. Peripheral controllers must keep up with the performance of state of the art CPUs. Performance demands on CPUs are limited to some extent by the distance an internal signal travels. Reducing signal travel with a CPU demands higher density, but density is limited by power dissipation/circuit. To solve this speed/power dilemma, manufacturers are turning to ECL gate arrays which minimize package to package propagation delays, power dissipation, and internal gate delays. At 10 MHz, CMOS gate arrays compare favorably with ECL arrays as shown in the Table. Boards should be available by mid-1982. **National Semiconductor**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 254

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CIRCLE 37

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CIRCLE 38

Microprocessor builds in memory protection and virtual memory access

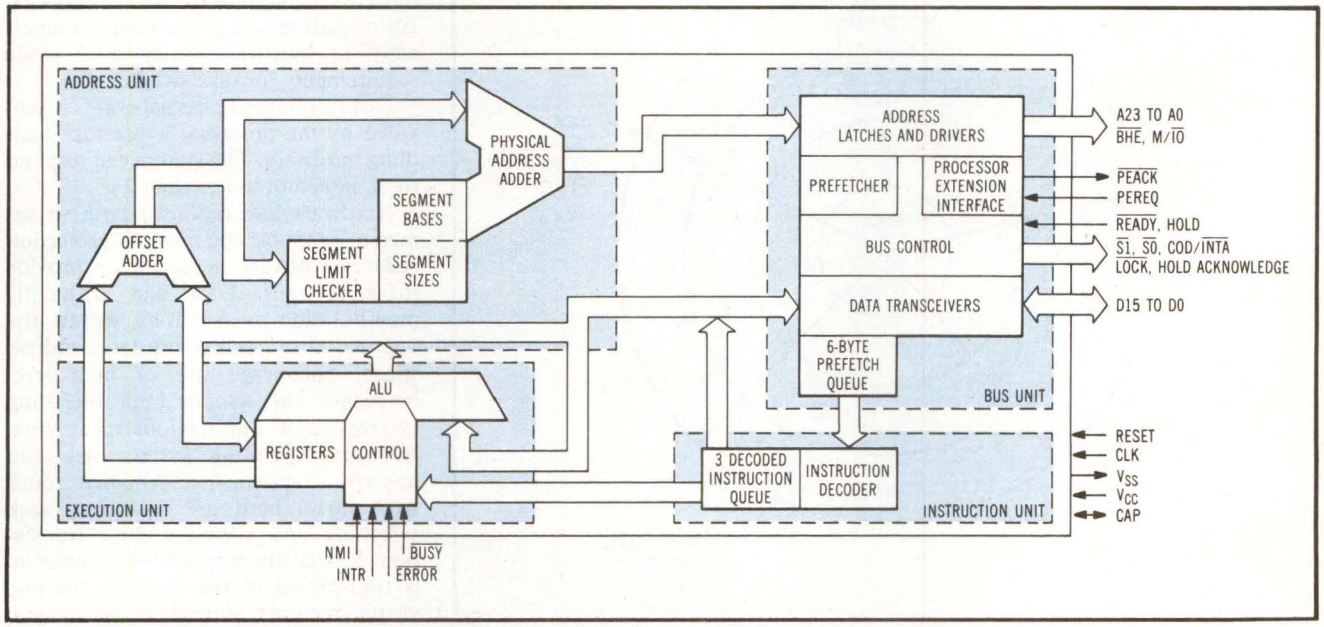

Fig 1 Organized in four pipelined functional units, Intel's 80286 fetches, decodes, and executes instructions in parallel to increase performance. Pipelining permits unit to detect invalid op codes before they are executed and to check out protection qualifiers without degrading performance or restricting memory access.

Answering the needs of distributed multiprocessing and multi-user systems, Intel's iAPX 286 microsystem provides data protection mechanisms, quick response, and rapid task switching. Needs of data acquisition systems are met by its 16M-byte real and 1G-byte virtual memory spaces. The machine's pipelined architecture permits it to offer memory management and protection without sacrificing performance.

The system is based on the 80286 CPU, an 8-MHz or 10-MHz processor that implements a multilevel protection mechanism, virtual memory address translation, and memory management capabilities onchip. Dedicated system support circuits simplify system hardware, while sophisticated hardware and software tools reduce both time and cost of product development.

Use of VLSI techniques increase throughput. Four independent processing units (Fig 1) are implemented within the CPU, each operating to minimize bus requirements and maximize CPU throughput. Combination of a demultiplexed bus structure with pipelining techniques doubles bus efficiency. This throughput is achieved without requiring proportional increases in memory speed. Bus interface and 10-MHz clock rate supply bus bandwidth of 10M bytes/s.

Because the processor's main functional areas are distinct from one another, they can operate simultaneously. Up to three instructions can be fetched and decoded during an extended ALU operation. This separation also serves to break up the otherwise sequential operation of a processor so that time can be compressed and performance increased.

The processor is based on a superset of the 8086/8088 instruction set. Existing code for either chip can be executed without modification in an 80286, which will perform the same application with higher performance. Minor modifications to existing code take advantage of the processor's memory management and protection features, as well as additional instructions and functions.

Pipelined architecture permits the CPU to detect invalid op codes well in advance of their execution. Also, it gives the chip time to check out the protection qualifiers, without degrading processing performance or restricting memory access.

The processor's four logical units—bus, address, instruction, and execution—are separate. The bus unit supplies a demultiplexed bus interface between the chip, system memory, and external I/O subsystems. It monitors bus cycle requests from other processors or from the processor's own address unit. When there is a pause, the bus unit's prefetcher grabs the next instruction and places it in a code queue, making it available to the chip's instruction unit.

Transfers to the instruction unit occur at a 1-byte/clock cycle rate. On receipt they are decoded, formatted, and placed in the instruction queue to await action by the execution unit.

CPU registers, arithmetic and logic unit, and microcode firmware for the CPU are within the execution unit. Instructions are executed under control of the ROM's internal microinstruction sequence. Prefetching of instructions keeps the execution unit operating at high efficiency.

The address unit performs the memory management and protection function by translating virtual addresses to physical addresses and simultaneously checking protection rights. It maintains an explicit cache containing all address mapping and protection information for virtual memory segments currently selected by the executing task. The

(continued on page 64)

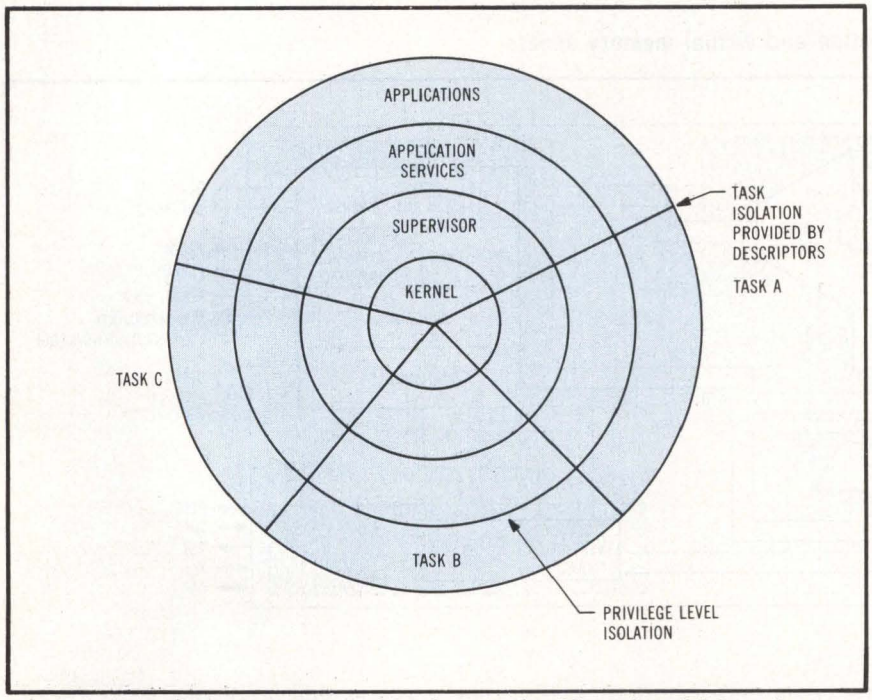

Fig 2 iAPX 286 hardware supports 4-level protection hierarchy with kernel reserved for vulnerable system software and applications area holding software with potentially erroneous routines. CPU prevents task from accessing any address to which it has no right of access.

onchip cache eliminates the need to access memory based address translation tables, and permits all functions to be performed in a single clock cycle.

Memory management and protection is an integral part of both the system architecture and the chip itself. This cohesive hardware architecture supplies increased reliability, easier implementation, faster operation, and reduced software overhead. Without extensive system software or add-on memory management units, the system protects users from each other, and the system software from the users. Each user has up to 1G byte of virtual memory space that can be split between shared and private use. This address space also contains the user's view of the operating system, speeding access to operating system routines.

Hardware supports a 4-level protection hierarchy (Fig 2), arranged from highest to lowest priority, with the kernel reserved for the most important and vulnerable system software routines. On the next level is the supervisor or system service level, then the applications service level, followed by the applications level.

Kernel software carries out critical tasks such as memory space management, task scheduling, and intertask communications. The supervisor handles I/O resource management, memory policies, and overall job scheduling. At the applications service level, programs support the applications software through file control, job control, language processing, and support utilities. The lowest level effectively isolates software with potentially erroneous routines, permitting faulty routines to be detected whenever they attempt to access an area to which they have no right of access.

Addressing up to 16M bytes of physical memory, the system has built-in virtual memory management support hardware that makes a much larger address space available. This onchip support enables as much as 1G byte of virtual address space to be allocated to each user. Operation of the MMU is transparent, requiring no special instructions for use.

Specialized onchip hardware also supports high speed system operation. The 16-bit multiply/divide instruction provided by the processor operates more than 10 times faster than those of the iAPX 86 or 88. String handling and high level language instructions further enhance performance.

Multitasking support hardware reduces the time required to switch from one task to another to less than 18 μs. All operations are performed automatically in hardware, eliminating code requirements for task switching.

Fast response to external events is provided by the processor's interrupt handling hardware. The system can respond to an interrupt in less than 3 μs.

Hardware integration of both virtual memory support and memory protection reduces software necessary to provide these features. Data and arithmetic manipulation instructions within the instruction set, along with large address space, encourage use of high level languages for writing both operating systems and applications programs. Reduced operating system size and improved system performance result from direct hardware control of task switching and virtual address translation. Virtual memory address translation is transparent to the software because virtual memory support is an integral part of the system architecture.

Clock chip, bus controller chip, address latch, and data transceiver chips complete the central processing subsystem. A bus arbiter chip supports MULTIBUS based applications, while a numeric processor fits high performance extended math computations.

Development support for the system is provided by the iAPX Evaluation Package running on Intellec Series III development systems. After programs have been developed using the package, they can be executed while their operation, including memory management and protection mechanisms, is monitored. During execution, the simulator program enforces all of the system's protection rules and executes all supported instructions. It verifies segment types, boundaries, and memory access privilege levels. Protection faults are trapped and indicated as the actual hardware would do it.

Software development tools include a full-scale macro assembler, system builder program, linker/binder program, librarian, and high level language translators. PL/M will be available in June, followed by Pascal and FORTRAN.

Price for the 68-pin 80286 will be $237 each in 100-piece quantities; sampling will begin in the third quarter. The Evaluation Package sells for $950 and is available now. **Intel Corp**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 255

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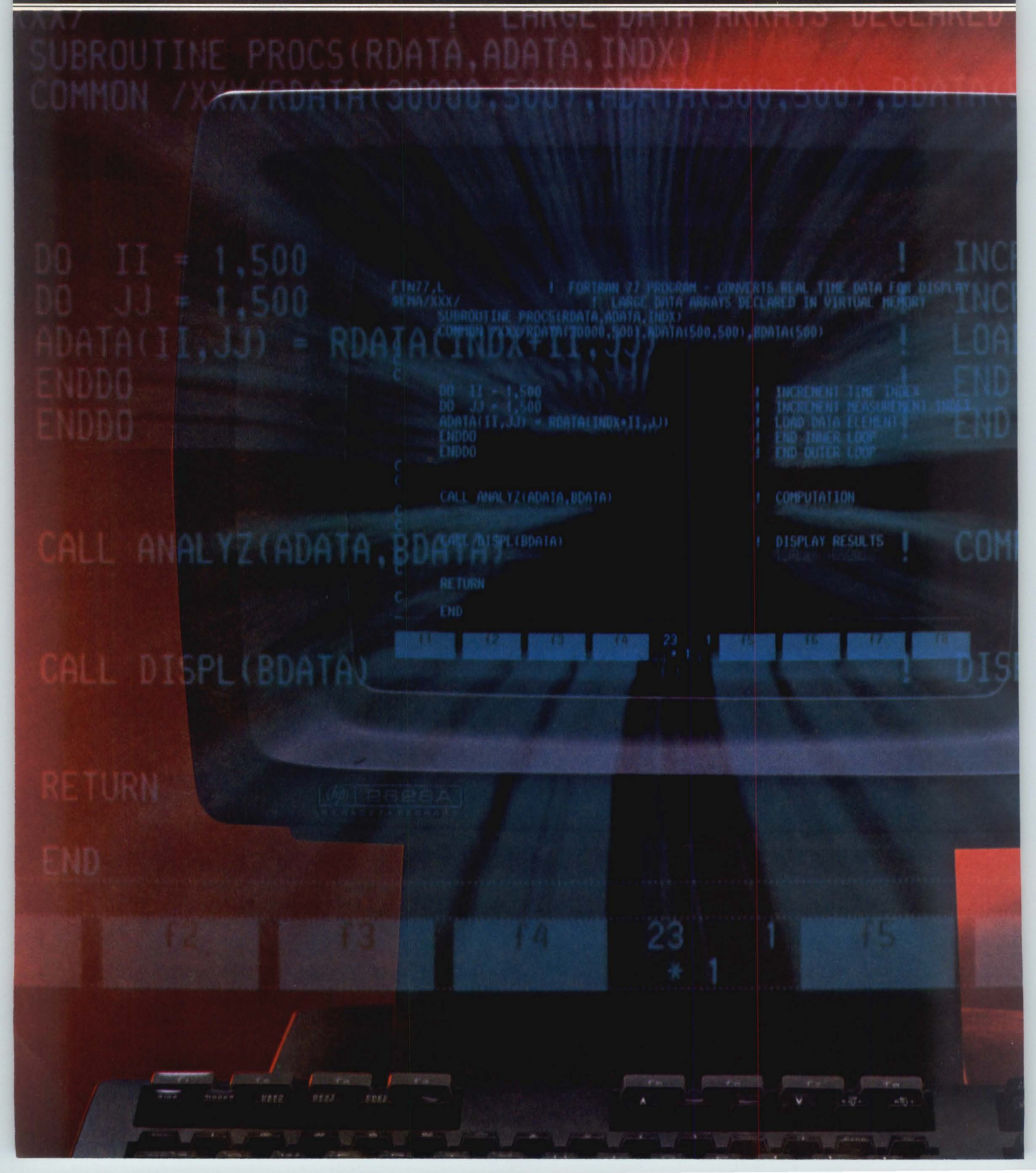
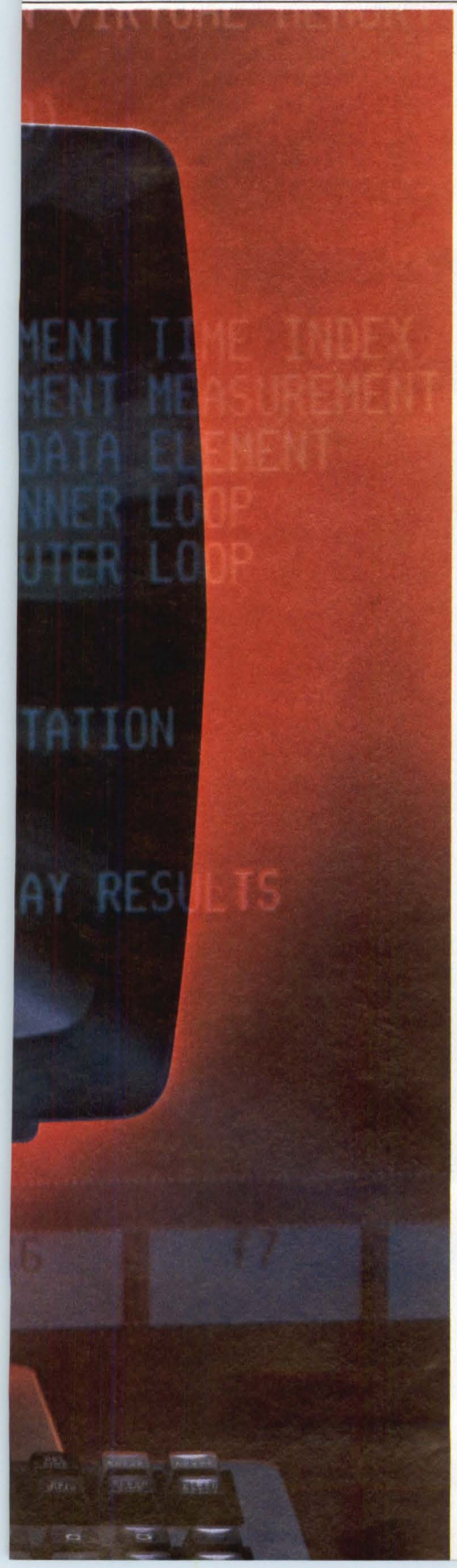
CIRCLE 40

The new HP you'd think you were



1000 Model 65: sitting at a mainframe.



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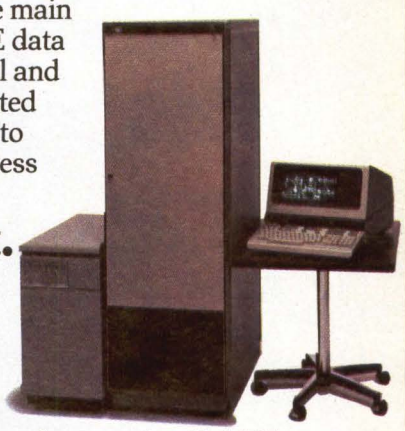

A one megabyte Model 65 development system is priced at under $65,000.

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CIRCLE 41

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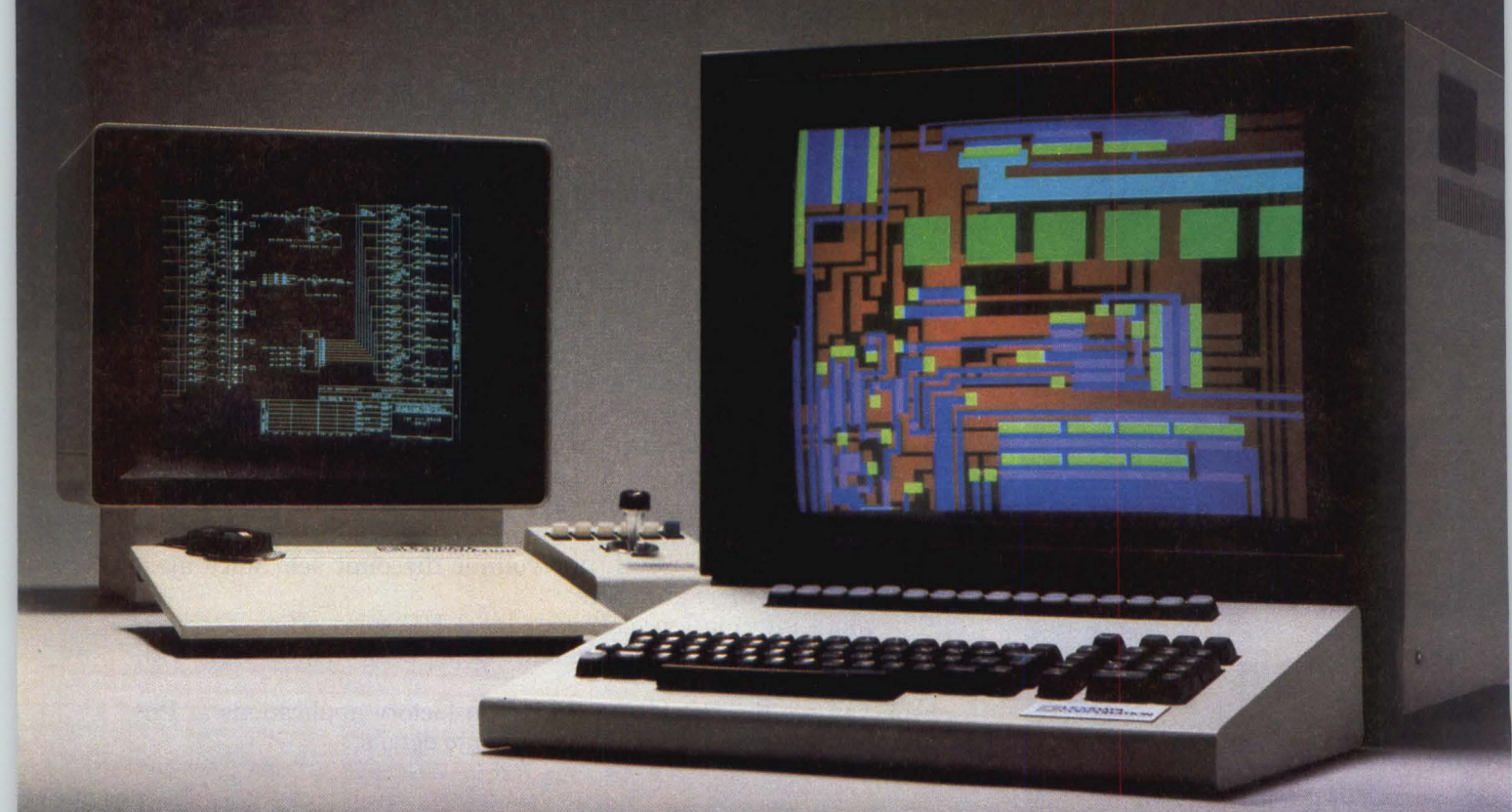
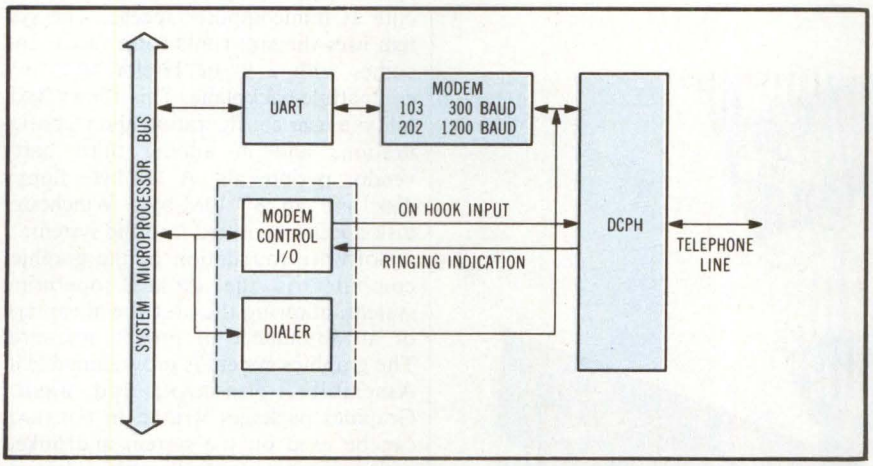


RASTER DISPLAYS...
FOR THOSE WHO DEMAND PERFORMANCE.

CIRCLE 42

FCC registered direct connect promotes modular modem design



Direct connect installation in custom modem. Cermetek's CH 1810 DCPH provides FCC approved connection to switched telephone network.

Designing a modem into a system offers system integrators advantages over purchase of a black box modem. For example, a black box requires its own power supply RS-232 port and housing, whereas a custom modem shares such resources with other system components. Just three elements are required in a custom modem: a system interface, a signal processor, and an FCC approved direct connect that interfaces the modem to the switched telephone network.

Cermetek Microelectronics recently introduced the CH 1810 direct connect protective hybrid (DCPH), which is registered under section 68 of the FCC rules. Using an approved part saves the system integrator the expense—and up to a 3-month delay—of obtaining approval through an FCC broker. Users of the part do not have to recertify their in-system modem.

Communicating data is almost as important as computing it, most digital system designers have discovered. As microcomputer costs spiral down, the system designer is forced to keep the communications aspect of a design on the same declining cost curve. Designing a modem into a system can result in a number of benefits. A modem can be incorporated into the basic product board, improving system integration, eliminating formal interfaces such as the RS-232, and saving component space and cost. Diagnostics can be embedded and customer related service problems minimized. Many low speed modem configurations are available for less than $100.

Design and construction of modems is basically an analog problem, which is avoided by digital system engineers plugging in an off-the-shelf modem board. DCPH allows a digital designer with little or no experience to build low cost 300-baud (at 30 cps) and 1200-baud (at 120 cps) modems, adequate for communicating data between microprocessor based systems and systems for data acquisition and collection.

Integrated component modules are fabricated using monolithic and hybrid technologies. For under $50, a user can design several 300- or 1200-baud class modems, complete with tip and ring telephone interfaces on one port and a generalized microprocessor compatible interface on the other port. Moreover, this component approach makes it possible to adapt a modem design to a specific data communications equipment requirement, eg, MULTIBUS, S-100, IEEE, RS-232, and STD BUS interfaces. Other capabilities include leased or switched network, strict Bell or CCITT compatibility, economy modems for dedicated leased lines, and proprietary communications links. Within each modem the designer has the option of selecting simplex or duplex transmission; originate only, answer only; originate and/or answer, automatic answer, and automatic dial.

DCPH is socket mounted into the PCB, and occupies less than 5 in^2 (32 cm^2). Connection to the DCPH is through center connector strips. Telephone line connection is via an external cable with a RJ11C or equivalent mating plug. A typical modem application is shown in the block diagram. The part, available immediately, is priced at $50 in quantities of 1000. **Cermetek Microelectronics Inc,** 1308 Borregas Ave, Sunnyvale, CA 94086.

Circle 256

COMPUTERS

High performance graphics computer, controller board targeted for OEMs

Eagle-1 graphics computer. Compact workstation can be reconfigured for different applications using standard MULTIBUS compatible peripherals.

Eagle-1 graphics computer, with advanced graphics hardware and software housed in a single system package, can operate either standalone or as an intelligent terminal in a distributed graphics network. Aimed at OEM systems builders in CAD/CAM and other applications, it can execute even large programs without mainframe intervention. Its hardware combines the graphics display with a general purpose computer.

(continued on page 70)

Display is presented on a high resolution 17″ (43.2-cm) CRT. The noninterlaced bit mapped raster display can achieve 1024- x 800-pixel resolution from a 256k-byte memory plane. Vector to raster conversion rate is 800 ns/pixel and data transfer rate from memory to display is 12 ns. An integral drawing processor calculates vectors, circles, arcs, and rectangles, and the memory planes have hardware controlled pan, scroll, and zoom.

Based on the 8086 16-bit CPU with optional 8087 floating point processor, the computer section has up to 1M-byte system RAM. Programs are said to execute at minicomputer speeds. The system uses the MULTIBUS form factor and comes with a 9- or 18-slot MULTIBUS compatible backplane. This allows flexibility in user configuration and reconfiguration, and in adding third party vendor peripherals. A 1M-byte floppy disk and an 8″ 10M-byte Winchester disk are incorporated into the system.

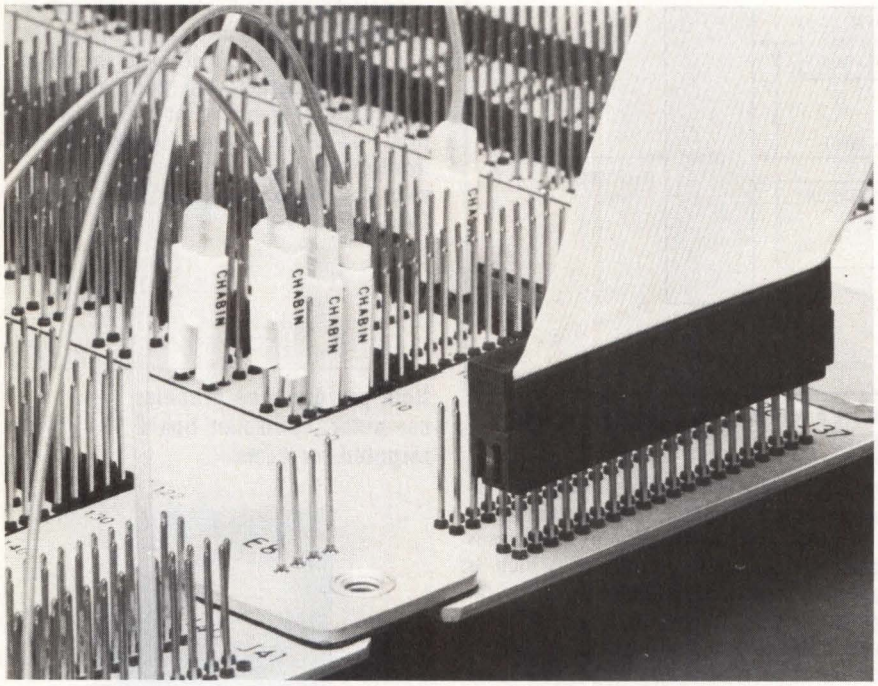
Software foundation of the graphics computer is the CP/M-86 operating system, allowing the user the advantage of an abundance of proven software. The graphics system is programmable in Assembler, FORTRAN, and BASIC. Graphics packages written in FORTRAN can be used on the system and linked with company supplied graphics drivers. Networking of workstations or remote file transfers is handled by extensive communications software. Most standard IBM protocols are available, including 2780, 3780, 3270, SNA, and HASP.

The Eagle-1 workstation stands 48″ (122 cm) high, is 23.75″ (60.3 cm) wide, and 24″ (61 cm) deep. It weighs 200 lb (91 kg). Power consumption is 1350 W at 110/220 Vac, 40-60 Hz. Price is $25,000 with quantity discounts available.

Heart of the graphics workstation, the HRG controller board, is also offered separately as a MULTIBUS compatible peripheral controller for raster scan monitors. It comes in five versions providing video output in resolutions from 512 x 512 to 1280 x 1024 pixels. The five standard hardware configurations are based on the number and size of memory planes and the video shift frequency. Access is via a high speed bidirectional DMA channel. ECL output to the video monitor is up to 80 MHz (12.5 ns/pixel). A daughter board containing up to 2M pixels of video refresh RAM may be used to obtain multiple memory planes per controller. The board measures 12″ x 6.75″ x 0.5″ (30.5 x 17.15 x 1.27 cm) and requires 5 Vdc at 4.3 A and -5.2 Vdc at 1 A. Prices start at $3150 in OEM quantities of 3 to 10 with delivery in 30 days. **Ikier Technology, Inc**, 7 Oak Park, Bedford, MA 01730.

—Jim Hughes, Senior Editor

Circle 257



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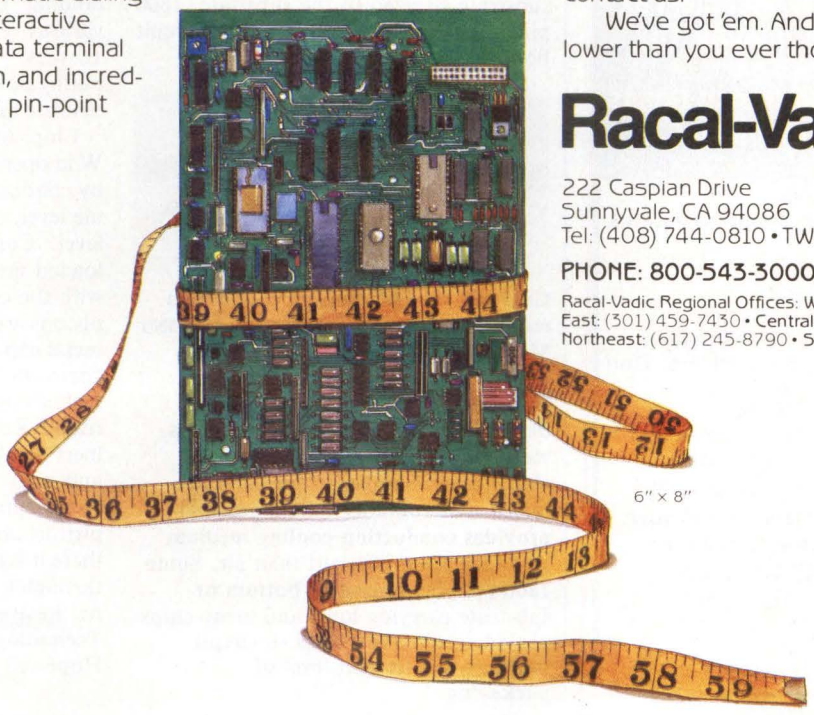

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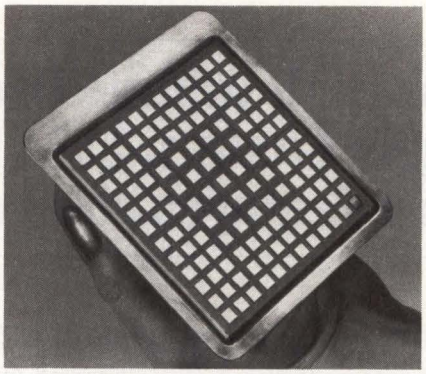
CIRCLE 36

Circuit packaging technique supplies high processor performance

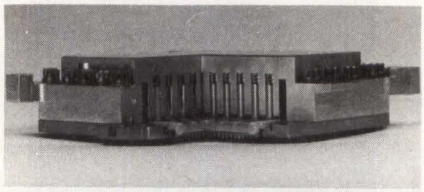
A thermal conduction module (TCM) contributes to the high performance levels of IBM's 3081 Model Group K processor complex. TCM protects, cools, and interconnects circuit components within the computer. In addition, it permits high density packaging necessary to shorten electronic delay time between components and produce high processing speeds. Designed at IBM's East Fishkill facility, each module contains a multilayer ceramic base that holds up to 133 logic and memory array chips within a helium filled, hermetically sealed chamber that dissipates generated heat.

The 90- x 90-mm multilayer ceramic substrates extend the technology used in the substrates made for 4300 series machines (*Computer Design*, Apr 1979, pp 39-40). The substrate typically contains 130 m of hair thin wiring that provides interconnecting circuitry for logic and array chips. High density packaging shortens the electronic delay time between components and results in higher processing speeds.



133-chip substrate, 90- x 90-mm square and 5-mm thick, on which chips are attached, contains 28 ceramic layers. Substrate package contains approximately 10,000 circuits and 300,000 array bits.

Approximately 10,000 TTL circuits and 300,000 array bits are packaged in the TCM-133 module. Each chip on the multilayer substrate can contain up to 704 logic circuits with logic chip level operating times in the 1-ns range. More than 10,000 flipchip solder joints connect chips to the substrate while 300,000 via holes interconnect circuitry within the 28 ceramic layers that make up the substrate. Brazed to the substrate, 1800 pins connect the module to the circuit boards.



Cutaway view of thermal conduction module circuit package used in IBM 3081 Model Group K processor complex, illustrates main functional elements. Unit consists of cooling hat, which dissipates heat conducted from chips via spring loaded pistons atop each chip. Inner chamber of hermetically sealed unit contains helium gas that provides conduction cooling medium six times more efficient than air. Some 1800 I/O pins brazed to bottom of substrate carrying logic and array chips provide interconnections to circuit board, which is next level of packaging.

Specifically designed to withstand rigorous manufacturing, environmental, and operating stresses, the logic and array chips in the module provide high reliability. In addition to material and physical design improvements, logic chips incorporate small transistors that speed circuit performance. These transistors reduce circuit delay to a little more than 1 ns—about twice the speed of similar circuits in 4300 series processors.

While similar to the logic chips used in 4300s, the silicon master slices incorporate smaller transistor geometries and their circuits operate at a higher current level. Selectively reducing the dimensions within circuit cell components lowers capacitance and achieves faster switching speeds.

High speed RAM array chips in the modules serve to supplement the logic circuitry. Their higher speeds result from both a modified design for internal chip circuitry and increased circuit density due to operation at lower power levels.

In the TCM-133, there is a 4.7- x 4.7-mm RAM chip that contains 3000 bits, organized in a 1k x 3 matrix and operating at a 10.5-ns access time. The module also incorporates a 2048- x 9-bit ROS chip that functions in the high speed control store section of the CPU.

Within the 3081 processor complex there are four circuit boards, each holding either six or nine TCMs of various configurations, including the TCM-133. One TCM can provide computing power equivalent to that of a System/370 model 148.

Chips within a TCM dissipate up to 300 W in operation. Resulting heat is removed by conduction cooling at chip and module level, and by water cooling at system level. Conduction cooling uses spring loaded metal pistons that make contact with the chips inside the module. These pistons are housed in a high conductivity metal cap hermetically sealed to a flange surrounding the ceramic substrate. Helium within this sealed system surrounds chips and pistons, serving as an inert medium that increases reliability and provides efficient heat conduction. Heat from the chips passes through the pistons and gas to the metal cap. From there it is transferred to water circulating through a water jacket and into an external heat exchanger. **IBM Corp, General Technology Div**, East Fishkill, Rte 52, Hopewell Junction, NY 12533.

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CIRCLE 45

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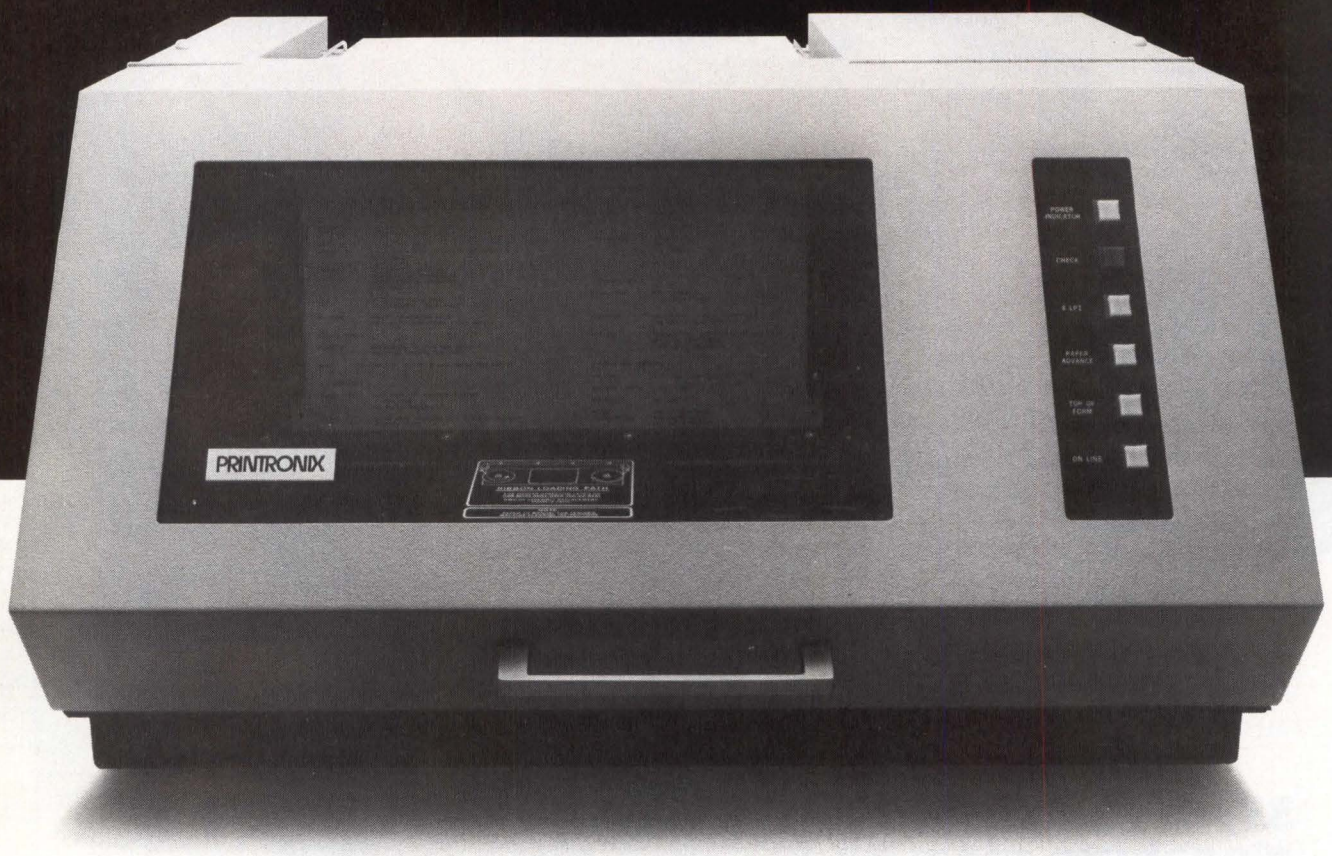

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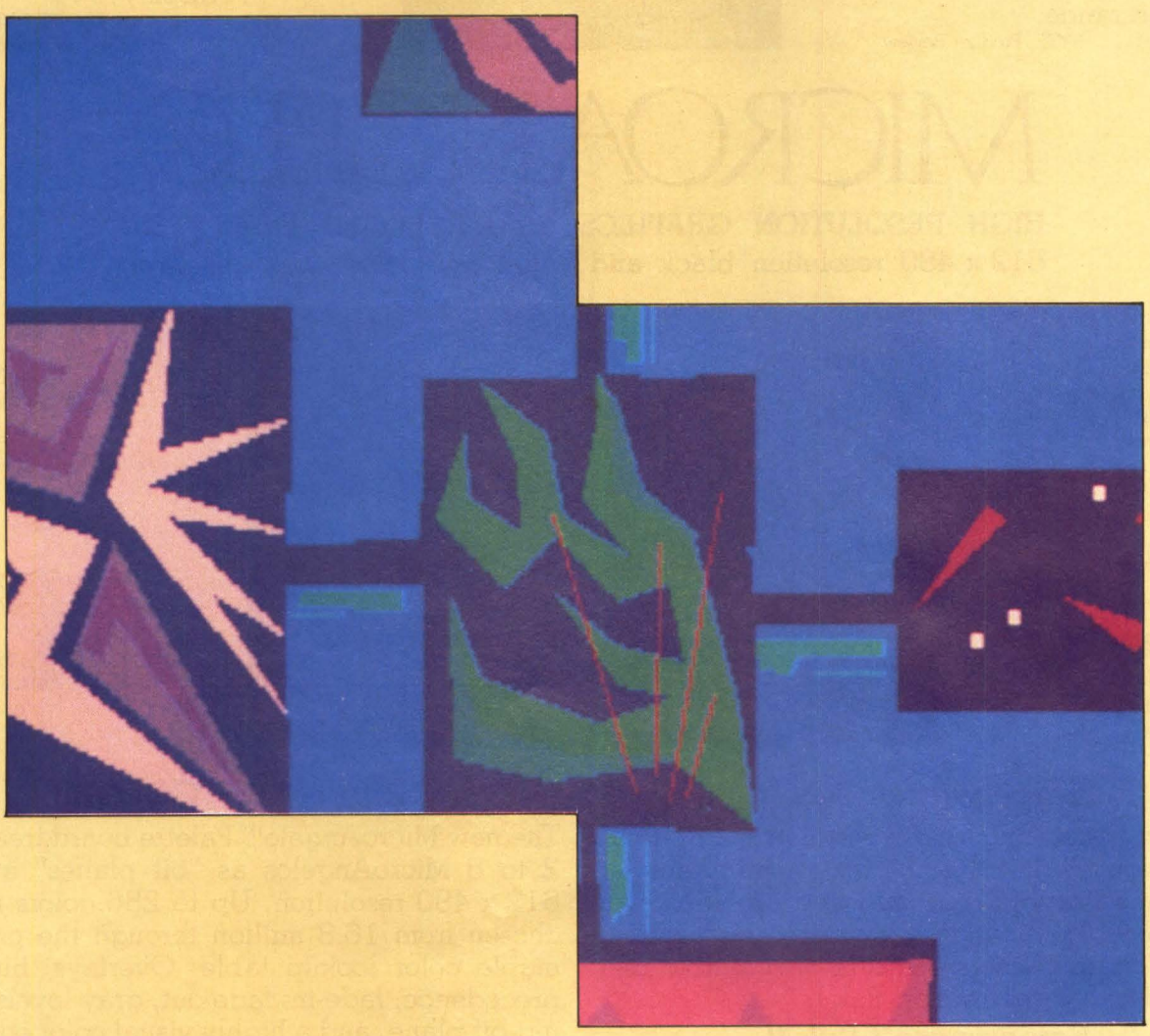
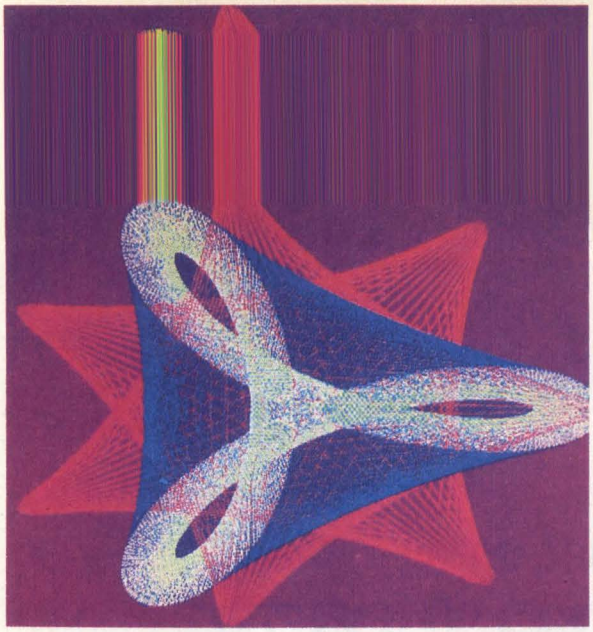
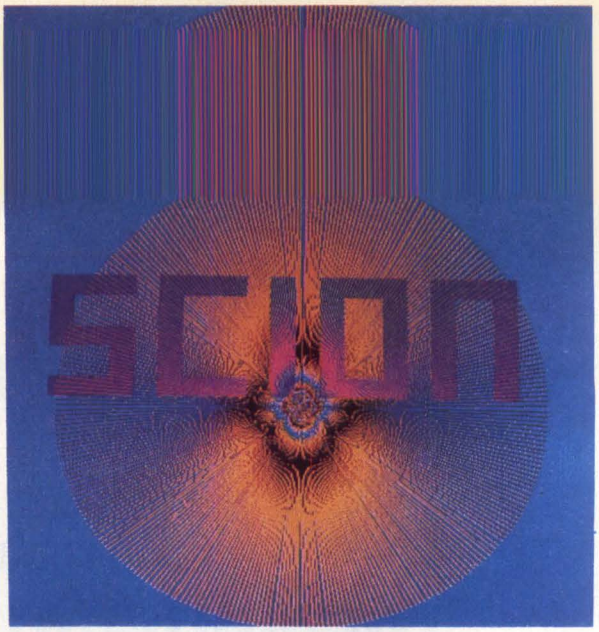
COMPUTER DESIGN

SPECIAL REPORT ON

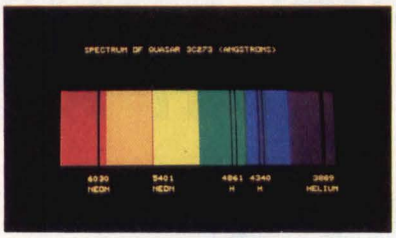
PERIPHERAL INTEGRATION HIGH TECHNOLOGY APPROACHES







"...stands well above other S-100 graphics displays in its price and performance range."
BYTE, Product Review



"...better monochromatic ...display...."
ELECTRONIC DESIGN, 1981 Technology Forecast

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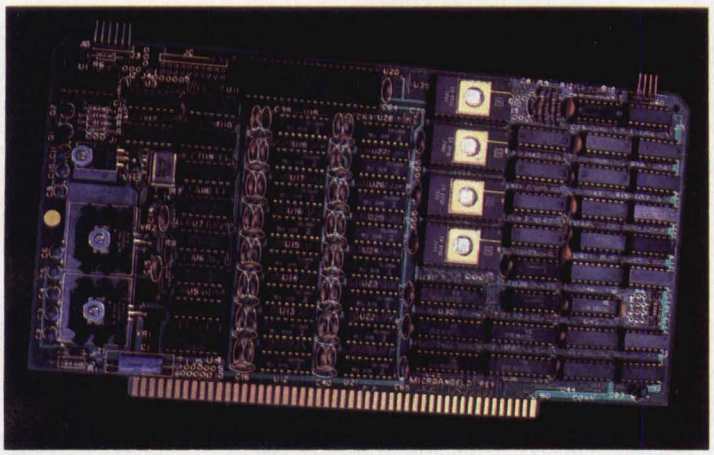

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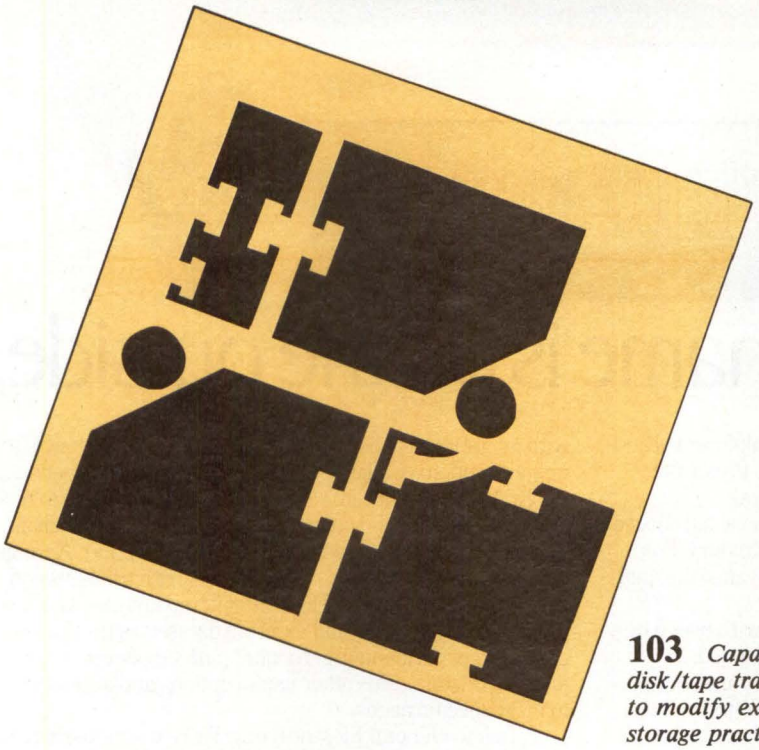
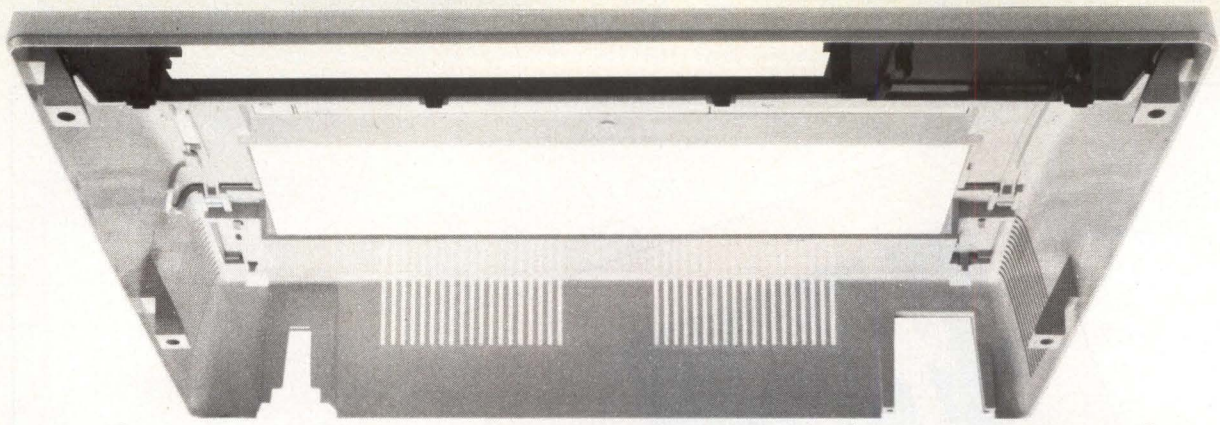


103 *Capability to make disk/tape transfers is certain to modify existing data storage practices*

Special report on peripheral integration/high technology approaches



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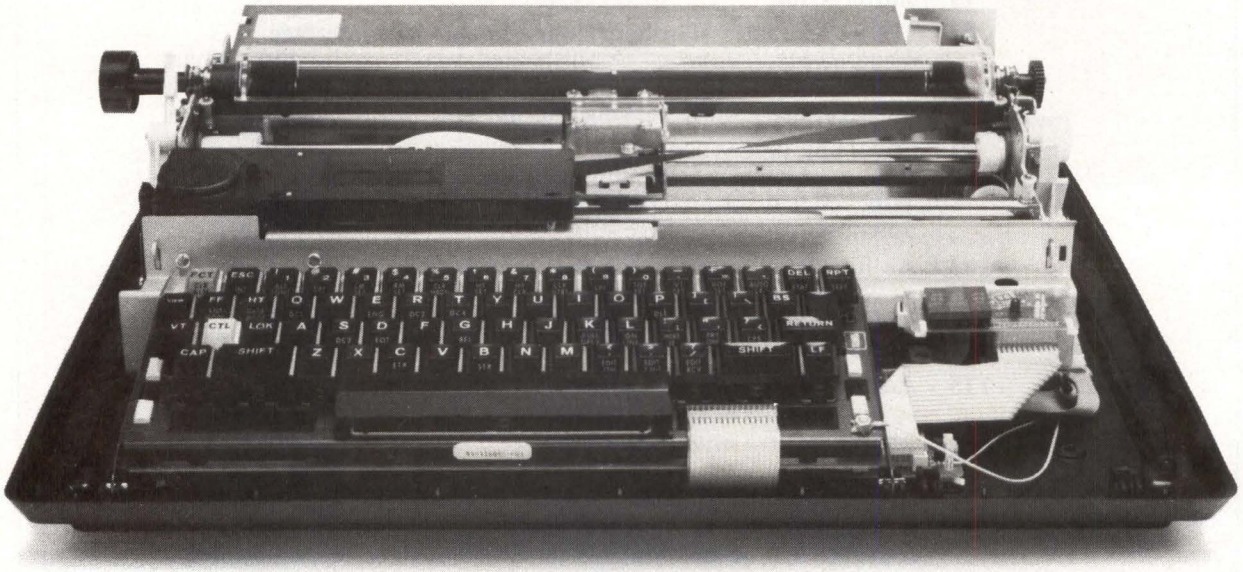

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GENERAL ELECTRIC

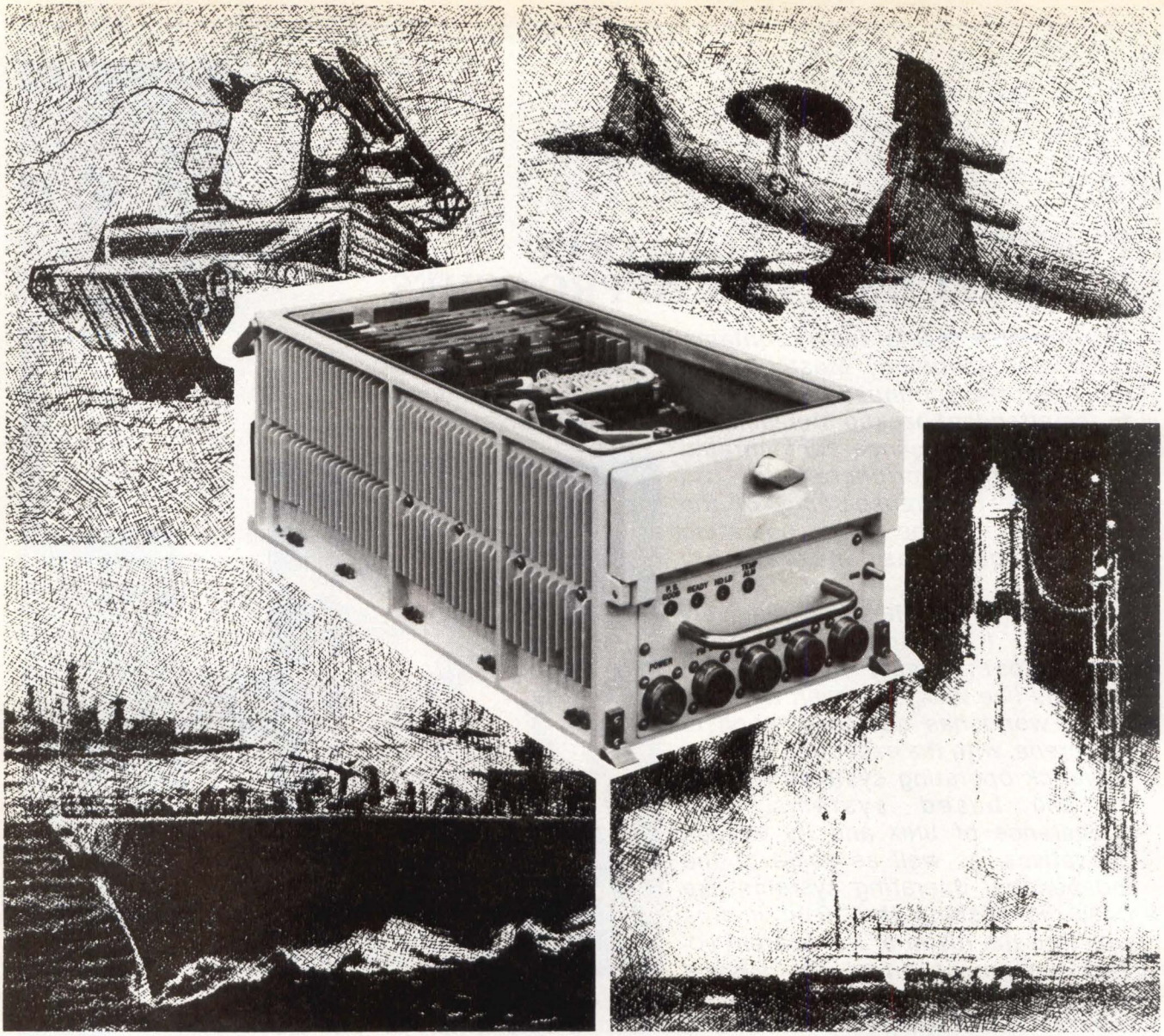
CIRCLE 48

PERIPHERAL INTEGRATION/ HIGH TECHNOLOGY APPROACHES

This month's special report contains a selection of articles on peripheral technology. Mostly concentrated in disk technology, they represent the continued push for greater densities and viable solutions to the attendant backup problems. As peripheral technology escalates—with more intelligence concentrated in both the peripheral and its controller—the transparency of the I/O software in the host's operating system becomes increasingly important.

The mini world has had relatively good I/O transparency for some time—most notably in operating systems like UNIX. However, the 8-bit micro world has not seen much in this arena, with the exception of a few maverick operating systems for 8080 or Z80 based systems. The appearance of UNIX and its various derivatives, as well as some of the independent operating systems like OASIS, is pushing the 16-bit micros well into the realm of transparent I/O. This equipment offers the system designer extended freedom in the handling of the widely varying formats of disks, tapes, printers, displays, and other smart peripherals that are popping up with increasing frequency and lots of native intelligence. They also offer the applications programmer the relative luxury of writing I/O independent software—software that reads and writes records of data to a "soft" I/O channel connected to a device driver, thus providing all of the formatting and device control considerations.

Saul B. Dinman
Editor in Chief



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CIRCLE 49

CONTROLLER MATES 10M-BYTE FLOPPY TO STANDARD INTERFACE

Sophisticated aerodynamics and a smart controller allow this 10M-byte, 8″ floppy to float within 10 μin of the drive head while packing 24k bpi

by Roderick J. Linton

Winchester-like performance in a flexible media subsystem can be achieved by combining several innovative technologies and design techniques in both the drive and the large scale integration controller. The disk storage subsystem is made up of a 10M-byte floppy disk housed in a hard plastic removable cartridge, the disk itself, and a large scale integrated controller with a host level, intelligent interface. Including the controller, the entire subsystem fits in the form factor of a standard 8″ floppy drive—a feature made possible by extensive use of large scale integration.

The result is a track density of 300 tracks/in, a linear bit density of 24,000 bpi, and a rotational speed of 1500 rpm—half that of Winchester devices. This capacity could only be fully and reliably utilized by a controller whose data channel, servo, and encoding technologies were sufficiently intelligent. At the same time, the controller had to be compatible with industry standard host interfaces to ease both hardware and software integration into systems.

Roderick J. Linton is director of quality and acting director of human resources at Iomega Corp, 4646 South 1500 West, Ogden, UT 84403, as well as one of the company's cofounders. Mr Linton served as program manager during the early development of the Alpha-10 subsystem. Mr Linton has a BSEE from the University of Utah.

Disk storage subsystem

Key to the high capacity of Iomega's Alpha-10 disk storage subsystem is the head/disk design, which uses what the company calls the "Bernoulli technology." Daniel Bernoulli, a Swiss mathematician, developed the theories in fluid mechanics that are the basis of the subsystem's design. Principles of fluid dynamics couple the media to the read/write head by essentially "flying" the media with respect to the head. An overview of the subsystem's capacity, as well as disk, track, and sector formats, is shown in Fig 1.

The primary challenge for the designer of any recording system that uses flexible media is to stabilize the physical motion of the media in the region of the read/write gap so that a stable recorded signal can be achieved. Any significant changes in the head to media spacing or in the data track alignment will result in modulation of the signal and corresponding reduction in data reliability.

In the Alpha-10 drive, a large flat surface—the Bernoulli plate—is mounted in close proximity [approximately 0.005″, (0.127 mm)] to the rotating disk. As the disk rotates in relation to the plate, it generates a pumping action that moves air radially outward, reducing the air pressure and causing the disk to be pulled uniformly toward the plate. The read/write head is mounted in an aerodynamically shaped coupler and accesses the disk through a slot in the plate.

By controlling the introduction of new air into the system at the disk hub, an equilibrium is achieved in which the disk is pulled toward the plate by the pumping action of the outwardly moving air, but does not touch

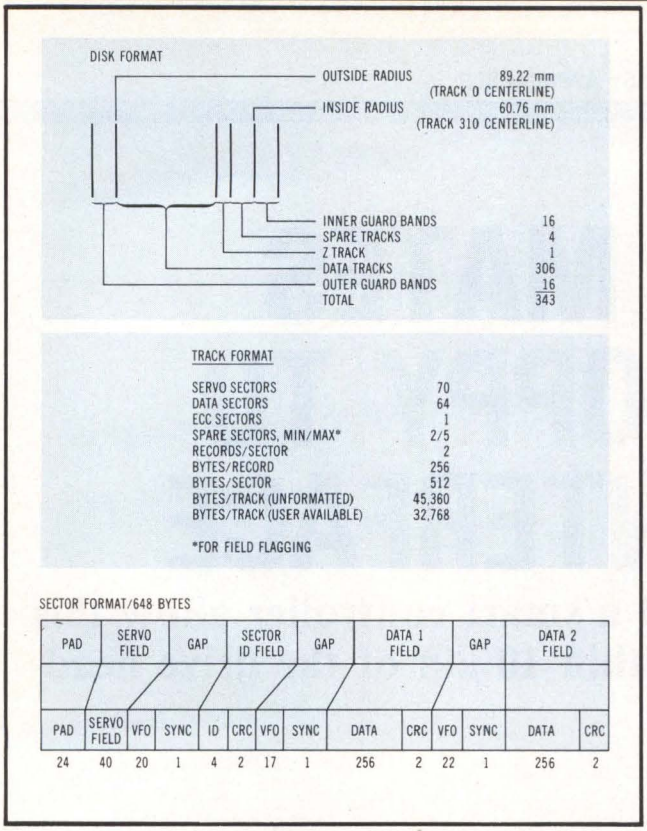

Fig 1 Alpha-10 disk, track and sector formats. Of 70 sectors on track, 64 are used as data sectors with one reserved for error correction code (ECC) information for entire track. Each sector has two 256-byte data fields, which may be viewed by operating system as either distinct or as one 512-byte unit.

it due to the radial flow of air between the disk and Bernoulli plate. In this equilibrium state, physical motion of the disk, perpendicular to the disk surface, is significantly reduced. Thus, aerodynamic coupling of the read/write head to the recording media can be achieved.

In the Alpha-10 drive, the read/write head is placed so that its contoured surface penetrates the rotating plane of the media. As the media spins, it must therefore move out and around the head surface. Because of the aerodynamic contour of the head surface, and the design of a small stabilizing coupler that surrounds the head, a coupling effect is achieved in the region surrounding the read/write gap. In this region, the media are actually flying over the head at a distance of less than 10 microinches. Because the system uses a noncontact, flying technology, and the coupling between head and disk is aerodynamic rather than mechanical (like the backside pressure pad in floppy disk systems), the wear and reliability characteristics of the system resemble those of noncontact rigid disk systems. However, the flexible disk system has certain advantages over rigid disk systems in terms of reliability. These include relative insensitivity to airborne contamination, low susceptibility to damage from shock and vibration, and simplicity in mechanical design.

Advantages over rigid disk systems

An air filtration system is not contained in the drive. Because of the radial air flow from the hub outward and the close spacing at the head/disk interface, airborne contaminants are flushed around the head and out of the system. In extremely rare instances when an airborne particle enters the head/disk interface, it simply decouples the media temporarily, flows through the interface, and then the media recouple. (See Fig 2.) Although a soft data error will be seen, no catastrophic damage occurs to the system. Tests have shown that the system meets a raw soft error specification of less than 1 soft error/10^{10} bits transferred in normal laboratory or office environments with no filtered air system. Even in the presence of extreme smoke environments, the device does not see a significant soft error rate increase.

In a rigid disk system, head to disk spacing is controlled by the design of the flying surfaces of the head, the rotational speed of the disk, and the spring pressure applied at the back of the head to force it toward the disk. Both head and disk are rigid surfaces so all compliance is controlled by the gimbal system attaching the head to the arm. Anything that disturbs the air bearing between head and disk can damage contact between the two members, and result in catastrophic failure of the total system. Therefore, rigid disk systems must be protected from airborne contamination and from moderate to extreme conditions of shock and vibration.

The head/disk interface is different in that the compliant member of the system is the media itself. Since coupling forces are aerodynamically generated, disturbances in the system cause the head and disk to separate rather than to join. In addition, mechanical shocks to the system are not easily transmitted through the flexible media and do not result in catastrophic failures of the head/disk interface. Decoupling can occur temporarily, without damaging the head or disk.

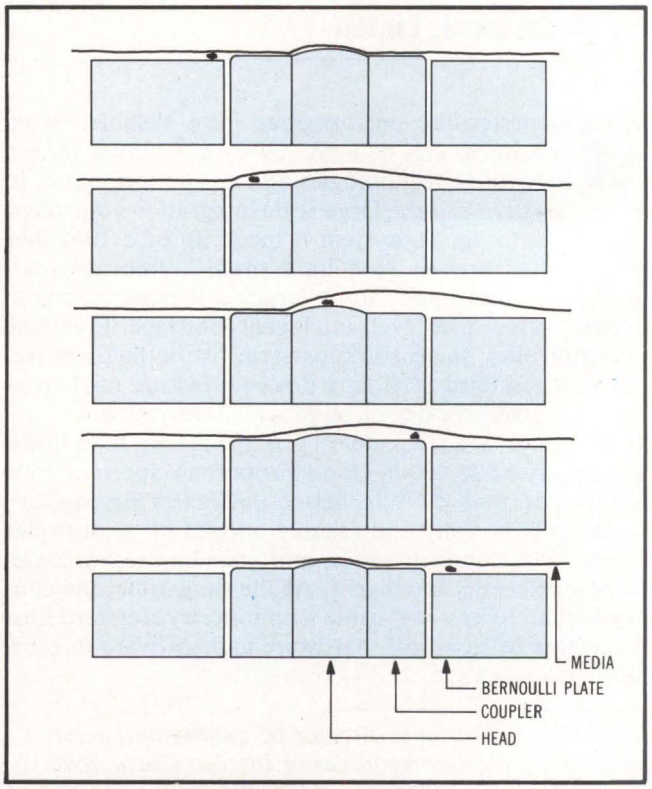

Fig 2 Bernoulli coupling with contaminant. In most cases, particle would be flushed around head by moving air. If contaminant passes directly between head and media, it causes only momentary decoupling and soft error rather than full-blown head crash.

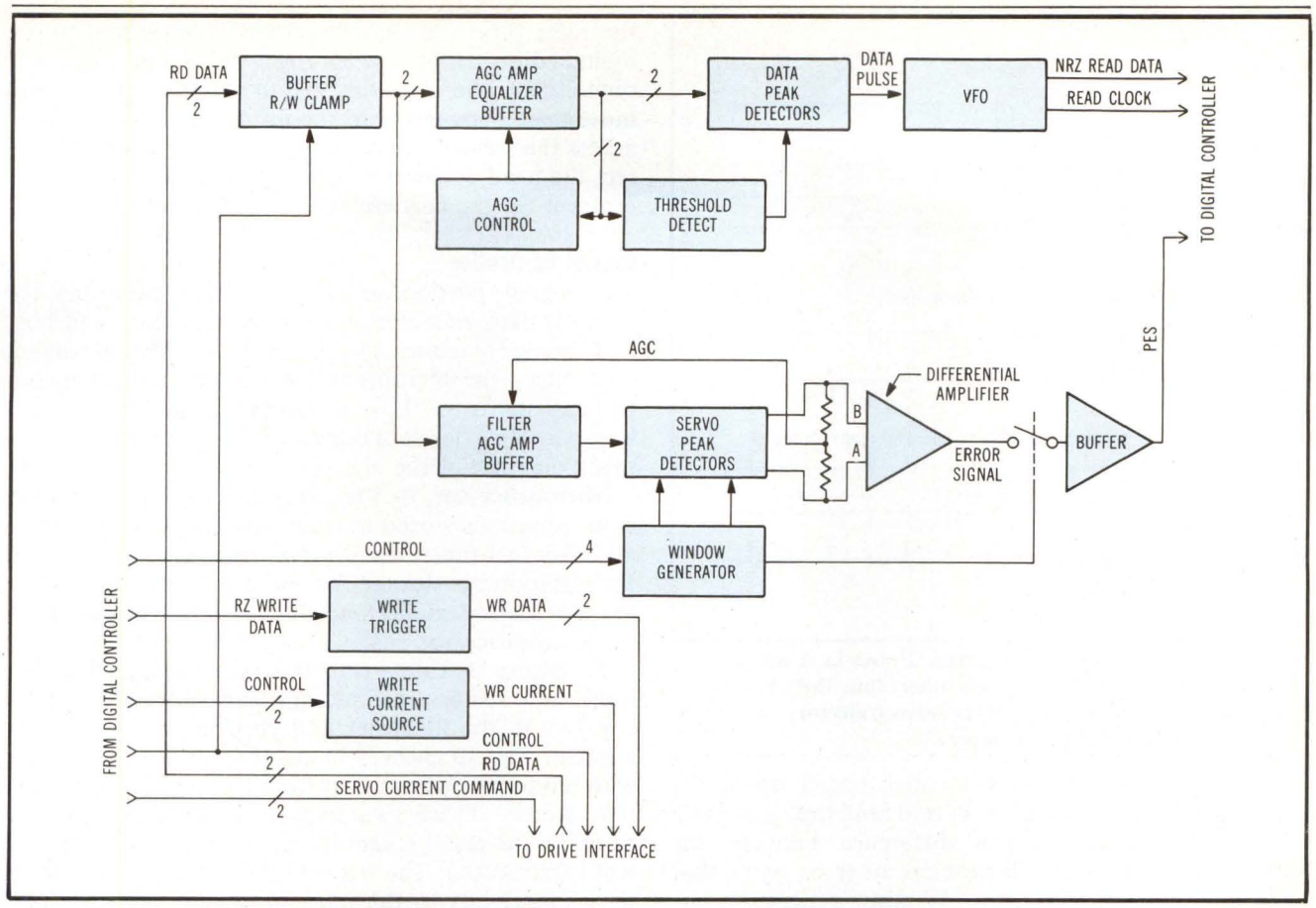

Fig 3 Analog portion of controller. Due to high bit density, signal conditioning is required for reliable data transfer. Conditioning includes filtering, AGC, and peak detection before signals are passed to digital logic. Analog portion also generates position error signal (PES) from pulses received from servo fields.

Only two of the four moving parts contained in the drive are part of the operating function—the spindle motor and the rotary actuator. Because the media loads to the head as it spins up, there is no head loading mechanism. Gimbal attachment of the head to the arm is unnecessary because all compliance in the system is in the flexible media. Finally, cams, levers, or other devices are not required to close air systems, open doors, load heads, or activate other mechanical systems.

Analog controller

While the Bernoulli technology makes high capacity on 8″ floppy media possible, it is the controller, containing both analog and digital large scale integration functions, that allows the system to fully exploit the capacity the technology provides. For instance, the analog portion of the controller provides four major functions in the total system. It provides a read clock that is synchronous with the speed of the data coming from the disk; filters and shapes the read data; interprets the sectored servo information; and controls write current and triggers write data. A block diagram of the analog controller is shown in Fig 3.

Read data signals are buffered and shaped through a series of circuits designed to preserve signal integrity. Automatic gain control (AGC) and threshold detect circuits are included to compensate for changes in the relative strength of the read signal; an equalizer circuit shapes the signal to compensate for the transfer characteristics of the head and media.

During a read process, the read data lines contain a series of positive and negative peaks that correspond with flux reversals recorded on disk. After shaping and gain control, the peaks are fed into peak detectors that output uniform pulses for each peak encountered. A variable frequency oscillator (VFO) locks onto the basic frequency of the pulses, providing a synchronous clock used to translate data pulses into standard nonreturn to zero (NRZ) format. At this point the data bits have not been decoded, but are in a transistor-transistor logic (TTL) form that can easily be used by the decoder in the digital portion of the controller.

Write data signals are converted from NRZ form to transitions by the write trigger. The write current source uses control lines from the digital controller to adjust the write current when the head moves between the inner and outer zones of the disk.

The subsystem uses a sectored servo approach to control head position with respect to the track, and head movement from track to track. Each sector on the track (70 total) contains a servo field that has been prewritten in the factory to provide positional information to the control system. Servo fields are written one-half track offset from data tracks (Fig 4). When the servo code is read, the relative amplitudes of the A and B field peaks, which are out of phase with each other, indicate how far the head is from a track center.

Servo information, available on the read data lines at the beginning of each sector, goes through a filter and control process similar to the read data. Servo peak

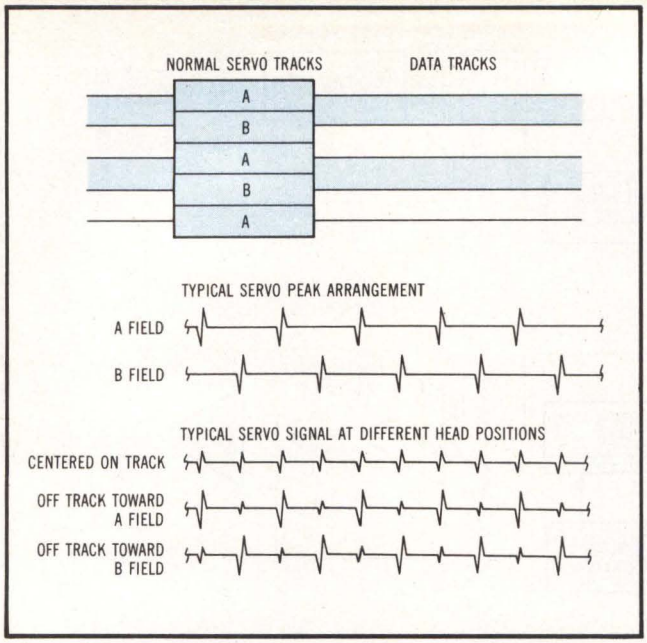

Fig 4 Head centering servo signals. Pulses in A and B fields are out of phase with each other, thus their relative amplitudes provide PES that gives servo trajectory to correct head position for following sector.

detectors on the analog controller board check the amplitude of the A and B peaks and send the results to a differential amplifier. The difference between the amplitude of the A and B peaks is an error signal that indicates the centering error. Window generation circuitry ensures that the peak detectors are turned on at the right time and that the error signal is sent to the digital controller only when the controller is ready. The digital controller uses this PES to determine what head movement commands it should send to the actuator across the servo current command lines in order to correct the head position with an anticipated trajectory to center it for the next sector.

Digital controller

The digital portion of the controller performs the control, data encoding, servo compensation, and host interfacing functions. Two major buses serve the digital controller—the microprocessor bus, which handles control and status for the microprocessor, and the channel bus, which carries data during reads or writes. Fig 5 is a block diagram of the digital controller.

Microprocessor, ID, CRC. A Z80 microprocessor works from programs stored in read only memory to oversee all subsystem functions. Random access memory is used for temporary storage of program variables. The microprocessor connects to these and other circuits via the microprocessor bus.

To ensure that data transfers take place at the right track and sector, the microprocessor loads a set of registers in the identifier (ID) checker with the target address. The ID checker loads another set of registers with the actual address read from the ID field of the current sector. These two addresses are compared for equality; the result is sent to the recording channel control logic (RCCL). The IDs can also be transferred from the channel bus to the microprocessor bus for direct reading by the microprocessor.

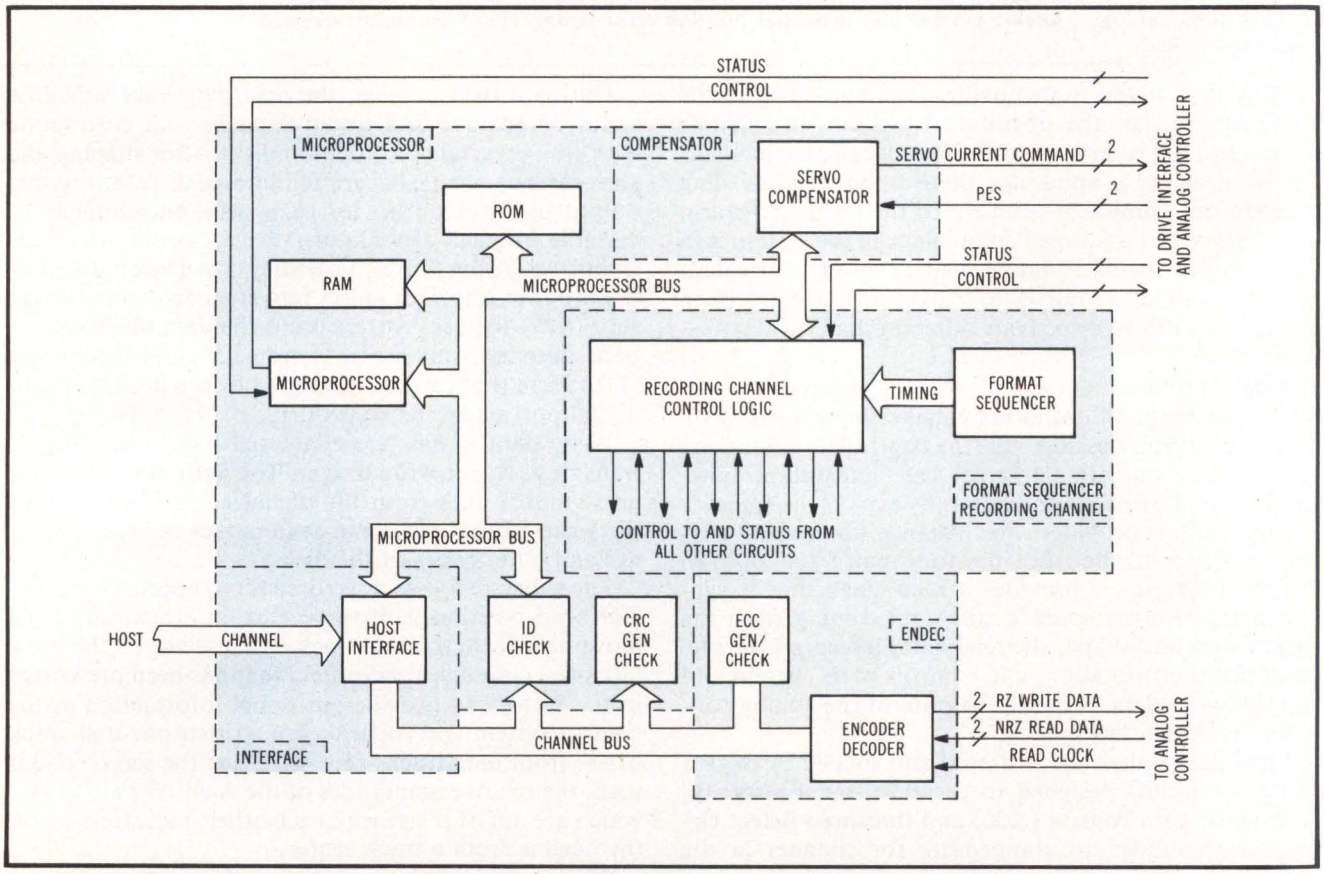

Fig 5 Block diagram of digital portion of controller. Microprocessor controls channel control logic, servo compensator, and host interface via its own bus, but does not directly handle data which pass over channel bus.

During a write, all data bytes are presented to the cyclic redundancy check (CRC) generator as they go to the encoder. The CRC generator prepares two bytes of check information for every record. CRC bytes are written at the end of each record and ID field and are used to verify data integrity during read operations.

Encoder/decoder, ECC. A unique data encoding scheme in the subsystem allows data to be packed more tightly on the disk. Bytes of write data are sent in parallel to the encoder across the channel bus where they are encoded, and sent serially to the analog controller board. Read data bits are brought serially from the analog board to be decoded, and presented in parallel bytes to the channel bus for transfer to the host.

Format sequencer. The format sequencer is a timing circuit that provides timing control signals to the drive throughout each sector. Using a sector timing mark as an index, the format sequencer communicates head position within the sector to the RCCL. RCCL combines the timing information with microprocessor commands and status from other controller circuits to control all operations. As the heart of the digital controller, the RCCL sends control, status, and timing signals to the other parts of the controller.

Servo compensator. Based on the PES from the analog portion, the servo compensator generates on track and off track information for the controller. It also accepts microprocessor controlled head movement commands and converts them to servo current commands that are used in the drive to move the actuator. Finally, it conditions the servo loop response.

To perform a seek, the microprocessor uses the servo compensator to induce offsets into the servo loop, causing the head to move off track. By controlling the amount of offset, the microprocessor can control the acceleration and velocity of the head. Offsets also can help recover data bits that have been damaged or written on an area with media defects. If a track or sector cannot be read by normal means, it can sometimes be read by moving the head slightly off track and retrying.

Error detection/correction. In typical magnetic storage devices, data errors tend to be bursts that cover several bits of unreadable data. Burst error length is a function of the size of the defect or contaminant causing the error, the linear bit density of the recorded data, and the data encoding scheme. Obviously, for a given defect or contaminant size, the burst error length becomes longer as the recording density becomes higher. The power of a particular ECC scheme can be measured by the burst error length it can correct, as well as the data space overhead the scheme requires. Typical burst error correction techniques used in magnetic storage devices correct 10 to 12 bits in error, at an overhead of 1.5% to 2.5% of the data record size.

Due to the very high linear bit density (24,000 bpi) of the drive and, consequently, the longer burst errors that might be expected, a more powerful ECC scheme than typically used in disk files was necessary. The Alpha-10 scheme is capable of correcting burst errors up to 512 bytes (4096 bits) in error with a data space overhead of 2.3%, and uses two distinct error codes for detection and correction.

First, a 2-byte CRC is appended to the end of each sector ID field and each 256-byte data record for error detection only. Although it does no correction, it is used to turn on the ECC system. CRC bytes are generated during a write operation by dividing the data to be written by a polynomial preselected for certain mathematical properties. The remainder of the divide operation is then appended to the end of the data record. When the data are read, the divide operation is performed again, using the same polynomial and comparing the remainder with the CRC bytes appended to the record during the write operation. Any discrepancies noted will activate the error correction system.

Second, a 512-byte ECC sector is written at the end of each track, which contains sufficient information to correct any total sector in error on that track. This ECC sector is generated by performing a sector parallel exclusive OR (XOR) operation around the track and writing the resultant parity sector in a sector location reserved for ECC. During error correction, any full sector on that track can be reconstructed by a parallel XOR of all other data sectors on the track, in addition to the ECC sector.

...the controller...allows the system to fully exploit the capacity provided by the technology.

Fig 6 is an example of ECC generation and data correction techniques, using short sectors for illustration. The technique works exactly the same way when using 64 sectors of 512 bytes each. In the ECC generation column, the ECC sector is generated by progressive XORing of sectors 1, 2, 3, etc. In the data correction column, an unreadable sector is restored by the same progressive XOR technique, but substituting the ECC sector for the unreadable sector.

Any time a sector is written on a given track, the controller automatically updates the ECC sector on the track being written. CRC errors during read operations automatically activate the error correction system. These activities are transparent to the host system so that corrected data are always sent to the host.

Z track

A special track in the subsystem is set aside to store information used by the controller. This configures the drive's operation to fit the system it is being used in.

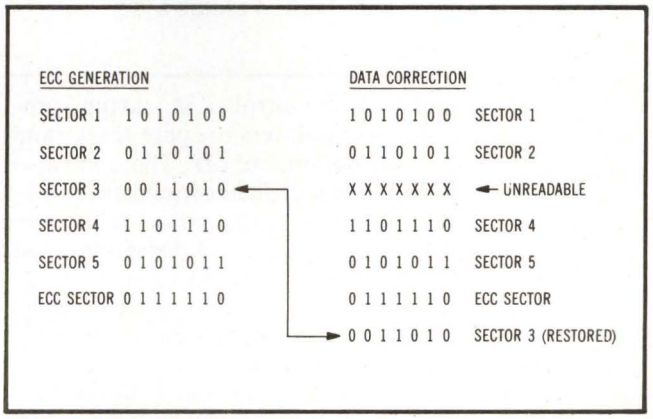

Fig 6 Examples of error correction by full sectors. ECC sector results from XORing all data sectors. Thus, one unreadable data sector can be reconstructed by XORing all other sectors and ECC sector.

Command menu

In addition to the standard SASI control lines and protocols, the subsystem provides the user with a command menu that can be summarized as follows:

Class 0 commands	(requiring no data transfer)
	Format Z Track
	Flag Sector
	Flag Track
	Seek
	Home
	Request Status
	Request Extended Status
	Test Controller Status
Class 1 commands	(transfer data from drive to host)
	Read Data
	Read ID
	Read Data With Offset
	Diagnostic Read
Class 2 commands	(transfer data from host to drive)
	Write Data
	Write ID
	Diagnostic Write

Format Z Track allows the user to specify whether the cartridge is to be furnished with ECC, what the sector interleave will be, and what the dwell time will be. The command writes the ECC, interleave, dwell time, and spare track information onto the Z track.

Flag Sector allows sector sparing of damaged or unreliable sectors. The command writes an FO (hexadecimal) pattern in the sector ID of the designated sector and copies the original sector ID onto the sector ID of the next available spare sector; the command automatically verifies that the operation has been successfully completed. If no other spare sectors are available on that track, the command returns an abnormal completion in the termination status byte.

Flag Track allows reassigning a defective or unreliable track to a spare track location. The controller locates and assigns the next available spare track. Spare track information from the Z track is obtained by the controller as part of the startup sequence each time a cartridge is inserted; proper interleaving of sectors on the spare track is done automatically. If spare tracks are not available on the cartridge, the command returns an abnormal completion in the termination status byte.

Seek causes the controller to perform an offline seek. As soon as the *Seek* command is accepted by the controller, the termination status byte is returned with normal completion. The controller is unavailable to the host for any other operation until the seek is completed. However, the channel is free for host operations with other controllers.

Home moves the actuator on the designated drive to track 0 and returns a normal completion in the termination status byte. The *Home* command, like the *Seek* command, is an overlap command; that is, the controller will return the termination status byte with normal completion as soon as the command has been accepted. The actual *Home* function is performed with the controller disconnected from the channel.

Request Status can be used, following receipt of the termination status byte, to request additional status information. The command returns four bytes of detailed status information regarding the command most recently executed on the designated drive. If that command has completed normally, the status bytes will contain the address of the last sector accessed. If it has completed abnormally, the status bytes will identify the error and the sector being accessed when the error occurred.

Request Extended Status returns 18 bytes of status information that pertain to the cartridge currently residing in the designated drive. The status information is derived from the cartridge Z track and from the write protect switch. It includes the following information: cartridge ECC/non-ECC designation, cartridge dwell time count, cartridge interleave factor, cartridge write protect status, and summary of the spare track inventory.

Test Controller Status tests the status of the controller and the drives attached to it (up to four). The command returns the following four bytes of status: drive selected, motors selected, cartridges loaded, and drives ready.

Read Data causes the drive to seek to the designated logical block and then begin reading the data. It ends when the designated number of blocks (up to 39,168) has been read. A multiblock read command that crosses a track boundary will result in an automatic seek to the next track. Both the command and parameter bytes allow the host to designate the starting logical block address and the number of logical blocks that are to be transferred.

This Z track is read by the controller at startup, providing such information as pointers to spare tracks and flags to turn the ECC system on and off. There are also factory prewritten patterns for diagnostics and setting the dwell time to choose how long the motor will remain running without the disk being accessed. Dwell time can be selected for times ranging from 2.5 to 30 minutes. By accessing the Z track, the user can also choose to interleave sectors to match the performance of a particular central processing unit. The subsystem provides 4 spare tracks/disk and 5 spare sectors/track. Since the pointers to these spares are read off the Z track at startup, the spares are automatically substituted for any that may have been found defective. There is no additional delay during seeks.

Host level interface

The controller contains a general purpose, 8-bit parallel direct memory access type interface, hardware compatible with the Shugart Associates Standard Interface (SASI). All host/subsystem communications are handled by the host interface. When the host sends commands to the subsystem, the interface receives them by a handshake process, sends them to the microprocessor across the microprocessor bus, and reports status back to the host. During data transfers, the interface uses its internal buffers to buffer data between the interim channel bus and the host. The microprocessor does not handle the data.

Host interfacing takes place within the interface module block of the digital controller. A major portion

Read ID causes the drive to read all IDs on the designated track.

Read Data With Offset reads the data field of the designated physical sector while automatically forcing the read head off track. The command is designed for use as part of a read recovery procedure; ECC is disabled during this read. Multisector reads with offset are not allowed.

Diagnostic Read allows the host to read data at any sector location on the disk, including flagged sectors and tracks, the Z track, and all spare tracks. Addressing is physical by track and sector to all of these data areas, except to a flagged sector. A special operation is required, as the sector ID of a flagged sector does not contain its physical address. The procedure requires that the host performs a *Read ID* command to the track on which the flagged sector is located. From the *Read ID*, the physical location of the flagged sector in relation to other sectors on the track can be determined. The *Diagnostic Read* command can then be issued, using a sector offset of not less than two and up to seven physical sector positions. ECC is disabled during this read.

Write Data causes the drive to seek to the designated logical block, begin writing the data, and end when the designated number of blocks (up to 39,168) have been written. A multiblock write command that crosses a track boundary will result in an automatic seek to the next track. Command and parameter bytes allow the host to designate the starting logical block address and the number of logical blocks to be written.

Write ID allows the host to rearrange sector IDs on a designated track to enhance performance. For example, a flagged sector that appears out of numerical sequence can be moved by the host back into sequential order. By issuing the *Read ID* command first, the host can determine the physical location of sectors on the designated track. A sector offset, similar to that used in the diagnostic read command, is used in locating the target sector.

Diagnostic Write allows the host to write a selected data pattern on the Z track at the reserved sector locations 8 through 15, 24 through 31, 40 through 47, and 56 through 63. Any data pattern is valid. Sector addressing is by physical sector address. Invalid sector addresses (any other than those noted above) will be rejected. Track addressing is automatic to Z track.

of this module is composed of two 256-byte buffers working in a flipflop mode. Each buffer has two effective data ports, one to the host and the other to the recording channel. Since the two buffers are independent, one can fill from the host port while the other empties to the recording channel port, and vice versa. This capability allows overlapped use of the buffer area and increases throughput.

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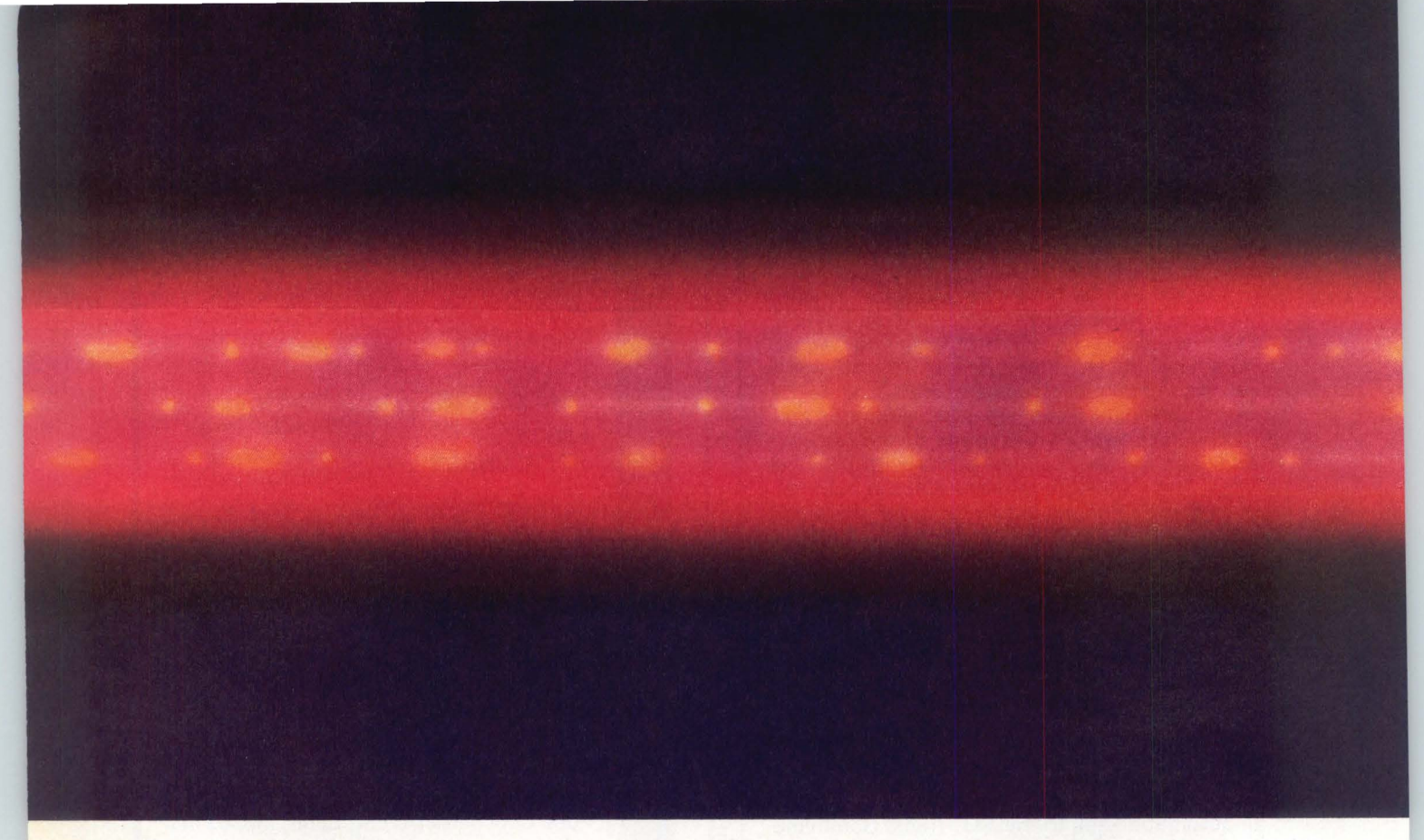

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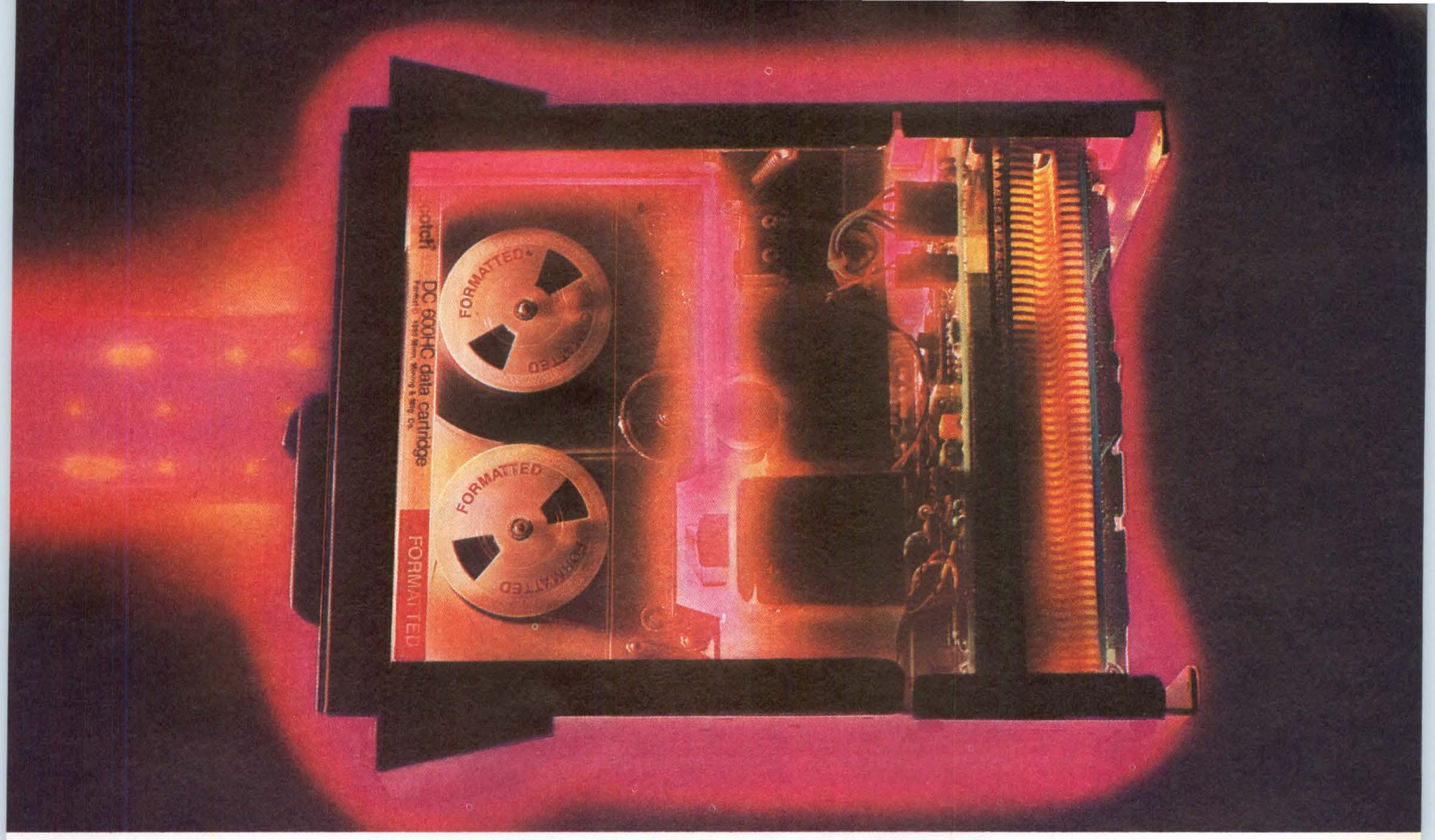

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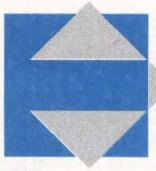

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CIRCLE 52

STREAMING TAPE SYNERGY

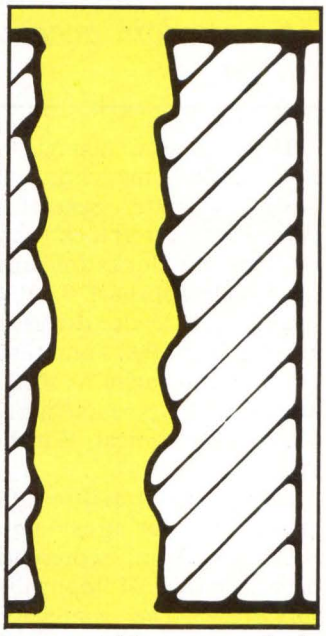
Streaming cartridge tape drives and mini-Winchester disks are changing the cost/performance design potential of mass storage subsystems

by J. V. Howell

Successful development of a reliable, high capacity streaming cartridge tape drive has given designers of small to medium sized systems unprecedented design opportunity and challenge. By combining 0.25″ streaming tape with 5.25″, 8″, and 14″ Winchester disks, designers achieve three objectives simultaneously: increased mass storage capacity, lower storage costs, and a high degree of media removability. The challenge is to make the Winchester/streaming cartridge subsystem work as effectively online as it does in theory.

Two misconceptions increase the difficulty of this task. The first is the view that the streaming tape cartridge is simply another form of Winchester backup—ie, that its principal uses are archival storage and protection against loss of data through operator error or equipment failure; the second is that the streaming tape cartridge is a typical peripheral.

Backup implies periodic, low priority functions such as end of day transaction storage or start of day program loads. Although the streaming cartridge can serve as a faster, higher capacity replacement for the conventional floppy disk in performing these chores, a more descriptive term would be Winchester extension. The streaming cartridge tape drive is truly a mass storage device, and is capable of playing a fully interactive role in any computer application in which most of the data are sequential and the information processing rate relatively limited.



Such applications include word processing, data logging, small business systems, intelligent terminal networks, and a variety of other high volume computer applications. In many of these instances, low cost, compact size, reliability, and removability of the streamer cartridge may make it suitable as the principal storage medium, reducing the role of the Winchester disk to that of a random access, file management buffer between the cartridge drive and the remainder of the system. In the long run, this could prompt a review of host computer architectures or, at the very least, a review of their resident operating systems.

Nearly all other peripheral devices, including keyboards, printers, and cathode ray tube (CRT) displays, communicate with the host computer through an essentially asynchronous interface. Data are transferred as they are available. Thus, the primary task of the system designer is to optimize throughput per dollar by implementing interfaces that will keep the devices operating at levels close to their performance limits. Any degradation in performance resulting from limited access or unavailable data is linear.

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Streaming cartridge drives do not have this characteristic. Any departure from continuous tape motion can abruptly degrade the efficiency and throughput of both the device and its associated subsystem components. It is imperative, therefore, that data be transferred to and from the drive at the specified rate for the selected model; nearly all of the considerations applying to the design of Winchester/streaming cartridge subsystems arise from this requirement. Fortunately, awareness of this requirement is increasing.

Streaming cartridge option

Streaming cartridge storage and retrieval rates are being standardized at approximately 30k and 90k bytes/s—within comfortable range of equivalent transfer rates for most Winchester disks, microprocessors, and minicomputers. Conventional buffering techniques can be used at the interfaces to sustain the data transfers, and rapid progress is being made in disk file management and application programming to capitalize on the unique benefits offered by the streaming cartridge option, even at this early stage in its development.

The streamer cartridge might...reduce the role of the Winchester disk to that of a random access, file management buffer.

High capacity. A single 0.25″ tape cartridge can store up to 45M bytes of data in a package the size of an 8-track cassette. Several factors contribute to this capability. Interblock gaps, large enough only to separate the blocks for error detection purposes, allow tape use to approach 97%, compared to 50% or less for start/stop cartridge drives. Storage bit densities are also very high: 10,000 nonreturn to zero inverted (NRZI) bit cells/in, equivalent to 8000 data bits or 1000 data bytes after (GGR) type encoding, compared to less than 7000 bits/in for typical Winchester disks and 0.5″ tape drives.

Low cost. At $20 to $35/cartridge, average storage media costs for streaming 0.25″ tape range as low as $0.50/megabyte, representing a fraction of the per megabyte costs of floppy disks or removable Winchester cartridges. The simplicity of the streaming drive mechanisms, compared to their start/stop counterparts, allows the drives themselves to be manufactured and sold at less than 50% of the cost of Winchesters with equivalent capacity. High capacities and fast transfer rates also reduce operating costs in terms of both operator time and processor overhead.

Compact size. A streaming cartridge drive has ten times the potential capacity of an 8″ floppy disk drive, yet it fits within the same dimensions. Special mounts are available for direct replacement in existing systems. Streaming cartridge data integrity is comparable to that of most Winchester products, achieving soft (correctable) error rates of one bit in 10^8 and hard (uncorrectable) errors occurring at a rate of less than one in 10^{10}. Write errors are automatically corrected by continuous rewrites, up to a hard error limit, without either stopping the tape or interrupting the host computer program. Design features contributing to this reliability include a combination of read after write amplitude and phase thresholds, a wideband sample and hold phase lock loop to track high frequency tape speed variations, and a low maintenance drive mechanism.

Three subsystem configurations

Three levels of host computer control over the Winchester/streaming cartridge subsystem can be identified. Both the Winchester disk and the streaming tape cartridge record data in a serial format, and are driven by mechanical assemblies that require control signals and feedback status reports. Separate controller/formatter circuits are therefore required.

Fig 1 shows the simplest interface hardware. In this configuration, the overhead burden is placed on the host computer. All data transfers to and from the disk and cartridge tape units must be processed through the host computer, interrupting its normal operations. Such transfers would also include the offloading of data from disk to streaming cartridge and the restoring of data to the disk, even though the stored records are mirror images of one another.

Computer main memory must also serve as a buffer to compensate for the inevitable differences in disk and streaming cartridge transfer rates. Winchester disk read and write rates average 500k bytes/s, compared to 30k or 90k bytes/s for streaming cartridge drives, depending upon whether the drive is streaming at 30 or 90 ips. These figures can be misleading, particularly if the disk is assembling or distributing files. Times for sector interleave, track seek, and rotational latency can sharply reduce the effective transfer rate so that buffering is actually required for a slower disk rather than the nominally slow streaming cartridge. To keep the tape in motion, the computer must accumulate a reasonable amount of data to warrant the transfer (eg, up to 100k bytes); alternately, the computer may direct the disk to concentrate data onto selected tracks reserved for this purpose, then make the transfer.

Fig 2 shows a more sophisticated configuration. Local intelligence has assumed most of the control and formatting functions. Equally important, the devices include buffers that help to match the transfer rates and ensure a steady stream of data to or from the streaming cartridge drive.

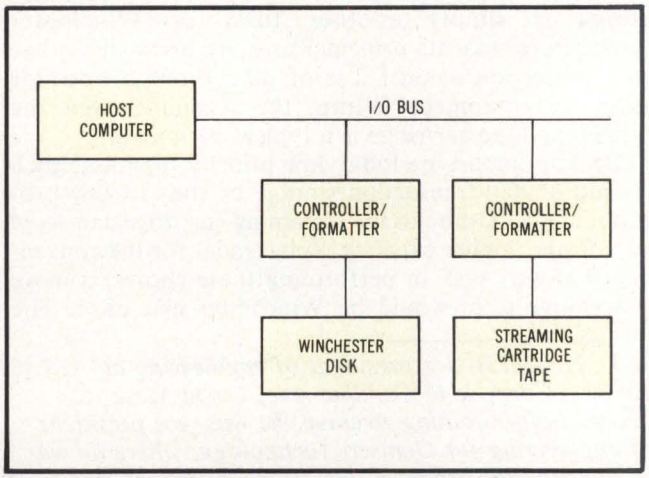
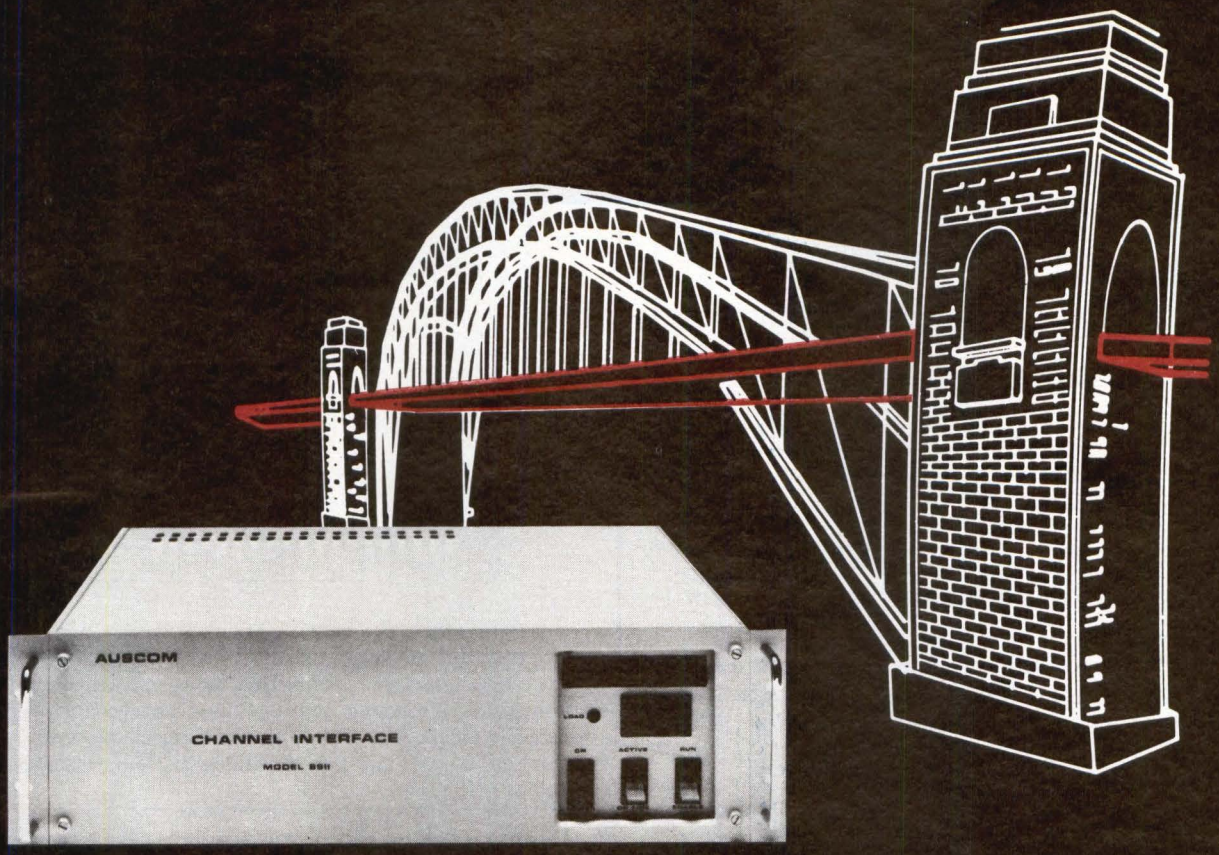


Fig 1 Simplest configuration for interface hardware. Controller/formatter circuits for two mass storage devices connect to host computer I/O bus as plug-in or add-on modules.



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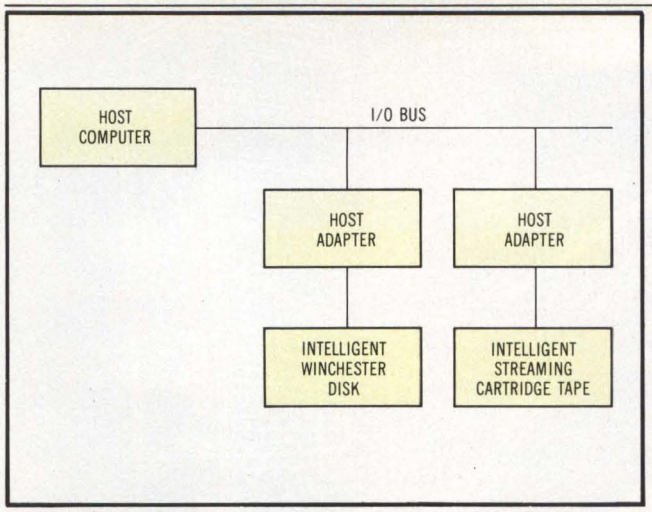

Fig 2 Host adapters serve as interfaces for intelligent versions of two mass storage devices. Data transfer still requires host CPU.

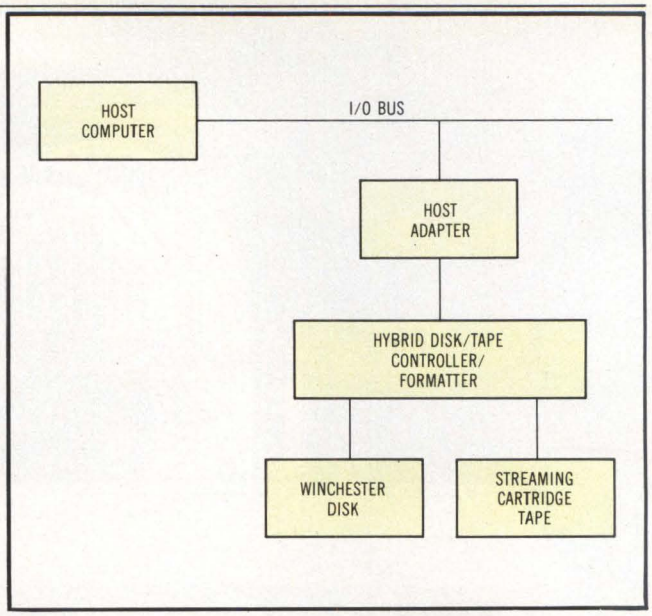

Fig 3 Hybrid interface. Connection between host computer and Winchester/streaming cartridge mass storage subsystem is reduced to single data and control interface. CPU need only send commands and parameters; actual data transfer takes place offline.

The host computer still serves as a conduit, however, and must supervise the transfers, even when data flow from one device to the other without alterations. Computer's load factor determines the effect of overhead burden on the efficiency of the total system. Complete transfer of a 20M-byte disk record can take up to 4 min; although unacceptable in an interactive, realtime environment, a 4-min transfer rate is satisfactory when the computer is inactive.

Hybrid interfacing can eliminate device to device penalties (Fig 3). Controller and formatter functions for both devices are independent of the host, and a direct channel is provided for device to device transfers, including the necessary buffer facilities. An off-the-shelf implementation of the Fig 3 subsystem takes a somewhat modified form, but the concept remains the same. Connection with the host computer is through an intelligent disk controller that interfaces, in turn, with an intelligent streaming cartridge drive. Once the required transfer commands have been issued, device to device transfers are totally transparent to the host.

System and host considerations

Winchester disk drives are available in a wide range of capacities, transfer rates, and average access times. Choice of streaming cartridge drives is more limited, but the designer must still make a decision whether, for example, a 20M- or 45M-byte cartridge would be more appropriate for a given application. Streaming cartridge tape transfer rates are directly tied to tape speed, with industry standards of 30k bytes/s for a 30-ips drive, 90k bytes/s for a 90-ips drive. Standard cartridge tape length is 450', so tape speed also affects the time required to search for a particular file or data block. Capacity is a function of the number of tracks recorded on the tape in a serpentine, ie, forward and backward, pattern (for instance, 9 tracks for 45M bytes, 4 tracks for 20M bytes).

Considering capacity alone, the selection of a particular disk and streaming cartridge combination depends upon the application, the subsystem configuration, and the characteristics of the host computer and its operating system.

If, for example, most of the data to be processed and stored by the application are sequential, storage costs can be minimized by specifying a high capacity cartridge and a lower capacity disk. A reverse order of capacities would be specified for fast, random file access, with only a limited need for long-term, removable storage. If archival backup is the only reason for adding a cartridge drive, the optimum solution would be to simply match the two capacities.

Subsystem configuration enters the selection process in the sense that it directly affects host computer overhead. Intelligence at the device level reduces this burden, since larger capacities and higher volume transfers can be supported. Intelligent, buffered interfaces also allow burst direct memory access (DMA)

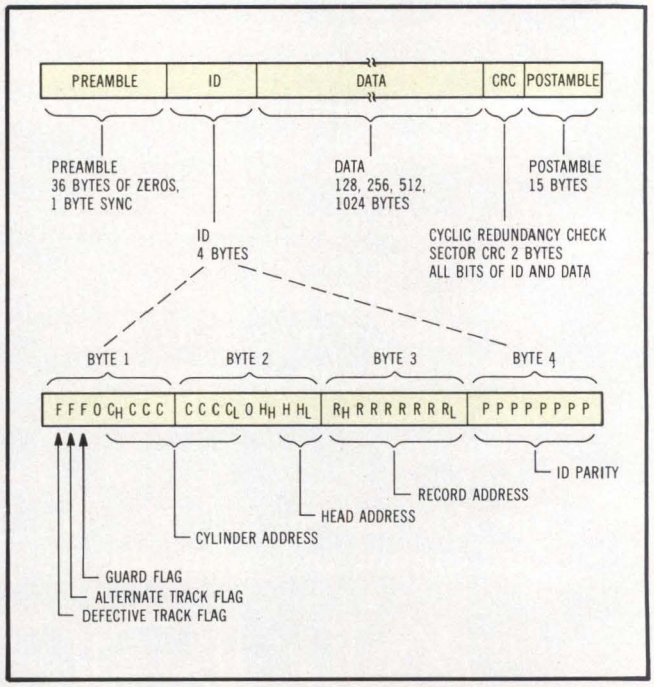

Fig 4 Typical Winchester disk recording format. ID field allows system to find individual sector at any time.

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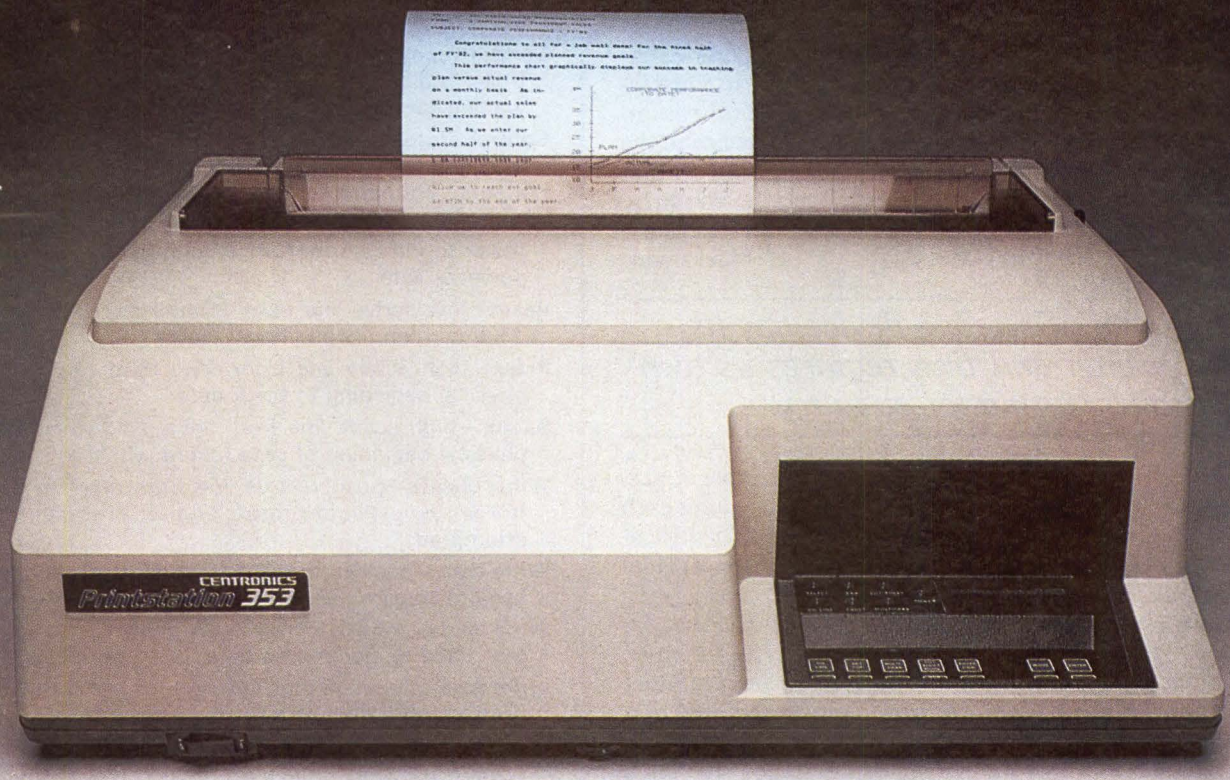

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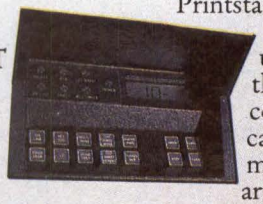

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transfers at rates up to 2M bytes, independent of the actual read/write rates of the two devices.

The true host computer interface would be the controller/formatter circuits: plug-in, add-on, or incorporated into intelligent devices. Depending on the computer, the operating system and the desired data transfer rate, the interface could use programmed I/O or DMA. In addition, cycle stealing transfers for byte oriented operating systems (CP/M) or high speed block transfers for multiple user systems (UNIX) could be incorporated to achieve higher throughput. No correlation exists between the stored records, even if mirror images are transferred from one mass storage device to the other. Each type of storage device has its own format and thus requires its own controller/formatter circuitry.

Fig 4 illustrates a typical Winchester disk recording format, using Century Data System's 14″ Marksman.

Each type of storage device has its own format and thus requires its own controller/formatter circuitry.

The data field for each sector is switch-selectable at 128, 256, 512, or 1024 bytes, with the first sector along each track identified by a physical index mark. An identification (ID) field allows the system to find an individual sector and rewrite the data at any time.

Data are organized by the controller/formatter circuits for the particular drive. The Panel, "Nonintelligent Disk Interface," lists the large number of input signals and implied precise timing required by a nonintelligent Winchester, again using the Marksman as an example. A much simpler signal interface (See Panel, "Intelligent Disk Interface") applies to the intelligent version of the same drive. Command repertoires for the two models (Panels, "Nonintelligent Disk Interface" and "Intelligent Disk Commands") reflect the added

Intelligent disk interface

Data/command/status—two high active 8-bit wide buses or one 8-bit wide bidirectional bus to transfer data, commands, and status between drive and CPU

Input ready—high active line from drive to CPU indicating that CPU is ready to accept commands or data

Control request—high active line from CPU used in conjunction with control acknowledge line to form handshake between CPU and drive

Control acknowledge—high active line from drive to CPU

Control ready—high active line from drive to CPU indicating drive is in input mode and waiting for command

Control status—high active line from drive to CPU indicating that data being sent to CPU are status information

Reset—low active line from CPU to provide drive with an unconditional reset

Abort—high active line from CPU causing drive to abort current command

Nonintelligent disk interface

Command/status—high active bidirectional 8-bit wide bus used to transfer commands and status

Control request—high active line from controller, used in conjunction with control acknowlege line to form a handshake between controller and drive

Control acknowledge—high active line from drive

Control ready—high active line from drive to controller indicating drive is in output mode and is waiting for command

Control status—high active line from drive to controller indicating that drive has placed byte of status information on command/status bus

Drive ready—positive true line from drive to controller to indicate that drive is up to speed and dc power is safe

Reset—low active line from controller that provides drive with an unconditional reset

Index—high active line from drive used to indicate physical beginning of track data

Sector—high active line from drive used to indicate physical beginning of data record within a track

Write unsafe—positive true line from drive to controller to indicate unsafe write process was attempted

Write data—positive true line from controller to drive used to transmit serial write data to drive

Write clock—positive true line from drive to interface used to clock write data from controller

Write gate—negative true line from controller to drive used to write data on selected head

Read data—positive true line from drive to interface used to transmit serial data to controller

Read clock—positive true line from drive to controller used to clock read data from drive

Read gate—positive true line from controller to drive to start lockup of phase lock loop in data separator

MPU clock—1-MHz clock provided for use by controller in functions that do not require synchronization to disk speed

Intelligent disk commands

Sequence—directs disk drive motor to power-up or power-down

Rezero—causes heads to be repositioned to cylinder zero, head zero, and verified

Status request—commands drive to return desired status byte as normal ending status

Seek—positions heads over specified cylinder and selects addressed head

Write buffer—places data from CPU into buffer

Write data—commands drive to write contents of buffer on cylinder and head specified by last seek command

Read data—reads data from specified sector into buffer

Read buffer—transfers data from buffer to CPU

Format—formats disk

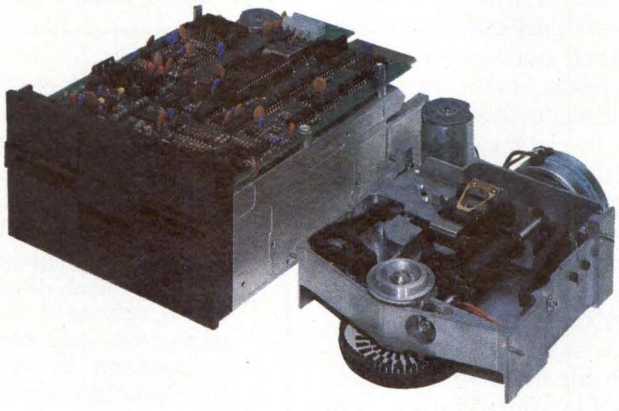
Boot—positions head over cylinder zero, head zero; record zero is then read into buffer and transferred to CPU

Fact:
The best 96 TPI 5¼" floppy is now better than ever.

Our Second Generation Floppy

It's a recognized fact that Micropolis is the undisputed leader when it comes to 96 Track-Per-Inch 5¼" floppy disk drives. We've delivered over 300,000 – more than all the others combined. And our drives are used by most media manufacturers as reference standards.

We designed our drives for double track density from the beginning, using a multiple step, silent stainless-steel leadscrew for highest positioning accuracy, a temperature compensated loop, and a superior diskette clamping mechanism.



Left: Model 1115 with industry standard mounting holes and bezel. Right: Inner chassis, model 1105, available separately for integration into OEM systems.

A Chassis Within a Chassis Plus Industry Standard Mounting Holes and Bezel

Our new 1115, second generation 0.5 (single head) and 1Mbyte (double head) floppies have a unique "chassis within a chassis" for unparalleled electrical shielding and reduced mounting stress. We've added a jewel follower to our positioning leadscrew for less friction and wear, and have reduced track-to-track access time to a solid 6 ms. The motor tach is no longer necessary since speed control is taken directly from the spindle pulley. This eliminates the need for an electrical adjustment as well as variations over time from belt and pulley wear.

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You can step up from 48 TPI to a solidly engineered Micropolis 96 TPI drive with no packaging or chassis modifications, and minimal hardware and software changes, immediately getting a 100% increase in capacity for less than 30% more cost. And it's easy to do with our new 1115 floppy which has industry standard mounting holes and bezel.

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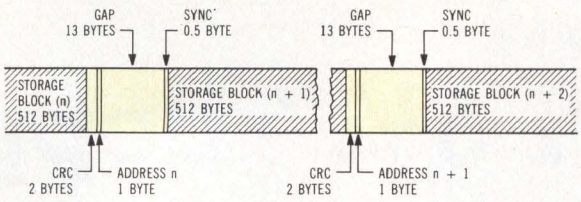

Fig 5 Format generated by intelligent cartridge drive. Blocks are identified sequentially and are found by counting file marks.

intelligence, allowing simple read and write instructions to take the place of complex data recovery, address decoding, and error detection procedures.

Streaming cartridge format shown in Fig 5 is similar to the Winchester record, yet shows distinct differences. Blocks take the place of sectors, but serve the same functions. Errors are detected at the block level, which is fixed at 512 bytes, and an address field serves to identify sequential blocks. Blocks in error carry the same identifying number, allowing the system to discard all but the last, error-free block when reading a series of blocks with identical addresses.

This system can also insert an illegal code "file mark" block at any point along the track. It is possible, therefore, to search for a particular record by counting file marks and blocks between the marks. Another technique would be to follow each file mark with an identification block or a directory of the stored information in the file.

Interblock gaps are very short, equivalent to only 13 bytes or 0.0013″, which is sufficient to separate the blocks but clearly not enough to stop and start the tape to access an individual block. By comparison, a start/stop cartridge format has interblock gaps that can range up to 600 bytes—a length equivalent to the data blocks themselves.

The tradeoff is between the requirement for continuous streaming and the twin benefits of high capacity and fast transfer rates. As a result, stopping for any reason—for lack of data or to reread a block of data—can seriously degrade the performance of the drive. Tape must decelerate, travel in a reverse direction past the desired restart point, and then regain forward speed before an attempt is made to read or write. Although the sequence may take only 1 s, up to 90k bytes of data could have been transferred during this brief interval. The three Panels, "Intelligent Streaming Cartridge Commands," "Intelligent Streaming Cartridge Interface," and "Nonintelligent Streaming Cartridge Interface," summarize the differences between nonintelligent and intelligent streaming cartridge signals and commands. As in the case of the equivalent Winchester disks, intelligence reduces the complexity of the signal interface and provides the host computer with a simple set of commands.

Intelligent streaming cartridge commands

Select drive—allows host to select one of up to four drives connected to controller

Beginning of tape—allows host to position tape in the cartridge in the selected drive to beginning of tape position

Erase—clears tape completely before writing first file of what is intended to become a multiple file tape

Retension—recommended by cartridge tape suppliers before writing or reading data when cartridge has been subjected to change in environment or not used for two or more weeks

Write file mark—generates a standard length data block with unique codes in user data field, a block address and a CRC

Read file mark—reads data (none is transferred to host)

Read status—provides host with information about controller and selected drive

Intelligent streaming cartridge interface

Data/command/status—8-bit bidirectional data bus

Online—host generated control signal, activated prior to transferring a read or write command and deactivated to terminate that read or write command

Request—host generated control signal indicating that command data have been placed on data bus in command mode or that status has been taken from data bus in status input mode, can be asserted by host only when RDY or EXC commands are asserted by controller

Reset—causes controller to perform same sequence as a power-on sequence

Transfer—host generated control signal indicating that data have been placed on data bus in write mode or that data have been taken from data bus in read mode

Acknowledge—controller generated signal indicating that data have been taken from data bus in write mode or that data have been placed on data bus in read mode

Ready—controller generated signal that indicates one of the following conditions

- data have been taken from data bus in command transfer mode
- data have been placed on data bus in status input mode
- a BOT, retension or erase command is completed following issuance
- a buffer is ready to be filled by host, or a WFM command can be issued in write mode
- a WFM command is completed in write file mark mode
- a buffer is ready to be emptied by host in read mode
- otherwise, controller is ready to receive a new command

Exception—controller generated signal indicating an exception condition in controller; host must issue status command and perform a status input to determine cause

Direction—controller generated signal which, when false, causes host data bus drivers to assert their data bus levels, and controller data bus drivers to assume high impedence states and assert their data bus levels

Nonintelligent streaming cartridge interface

GO—go control for capstan servo
REV—direction control for capstan servo
RES—reserved for track select bit 3
RES—reserved for track select bit 2
TR1—track select bit 1
TR0—track select bit 0
RST—reserved
DS3—drive 3 select control
DS2—drive 2 select control
DS1—drive 1 select control
DS0—drive 0 select control
RDL—read level output—a digitized derivative of analog read signal
RDP—read pulse output—a pulse per flux transition
UTH—upper tape position code
LTH—lower tape position code
SLD—selected response from selected drive
CIN—cartridge in place
USF—unsafe—cartridge safe plug is in unsafe position (ie, writing is enabled)
TCH—capstan tachometer pulses—each pulse equals 112 ±3% mils of tape movement
WDA—write data signal
WDA+—inverse write data signal
Reserved
HSD—high speed select control for model 3020B
WEN—write enable control
EEN—erase enable control

Intelligent hybrid interface

A single intelligent mass storage interface expands on the following advantages: only one physical connection to the host computer; simplified command structure; and, most important, offline data transfer between the mass storage devices.

One off-the-shelf product that implements this concept is essentially a Winchester disk controller/formatter with a streaming cartridge port and microprocessor firmware for controlling both devices simultaneously. Commands from the host computer direct the controller/formatter to transfer data, for example, between the computer and one of several Winchester disks or one of four daisy chained streaming cartridge drives. Three 2k-byte buffers are incorporated into the controller so that simultaneous transfers can occur. Data read from a disk can be loaded into one buffer while previously read data are transferred to the host from a second buffer. Acting together, the three buffers form a bucket brigade that reduces the chance that momentary delays in the receipt or transmission of data will interrupt the flow.

The tradeoff is between the requirement for continuous streaming and the twin benefits of high capacity and fast transfer rates.

The first streaming cartridge drive connected to the controller/formatter is an intelligent unit capable of supporting three additional drives. A similar bucket brigade of three 512-byte buffers provides further assurance that the data flow between the host and a selected cartridge drive will be continuous and uninterrupted.

Direct disk to tape transfers are also initiated by commands from the host computer. Included in the parameters for such transfers is a priority value, which determines the amount of data that can be transferred without interruption. If a direct access request is received while the transfer is in progress, an interrupt will occur at the earliest possible moment; this releases the facilities to the host computer for immediate access to any one of the disks. In this way, multiple users can communicate with their data bases, even when a transparent data transfer is occurring between the mass storage devices.

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High 704 *Average 705* *Low 706*

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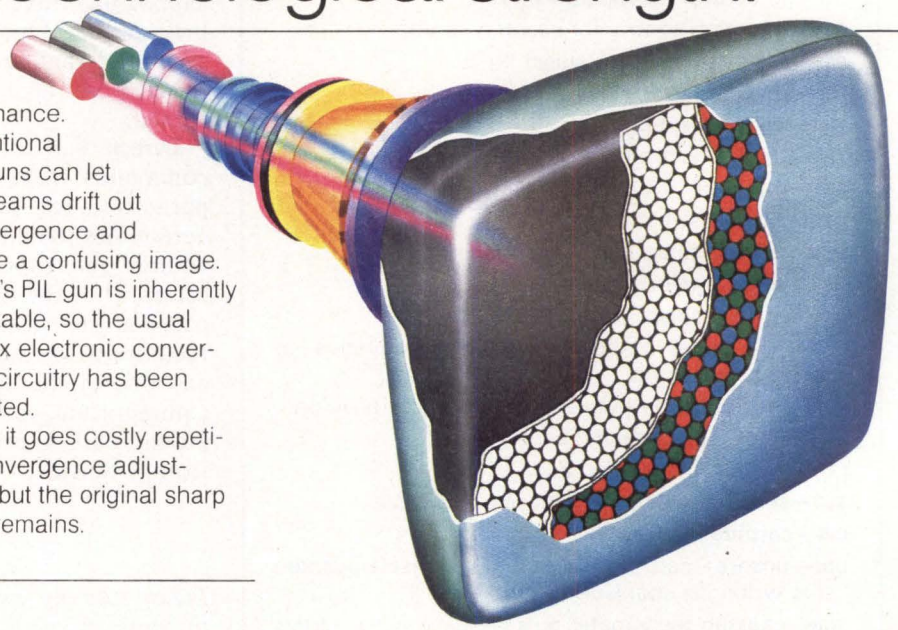

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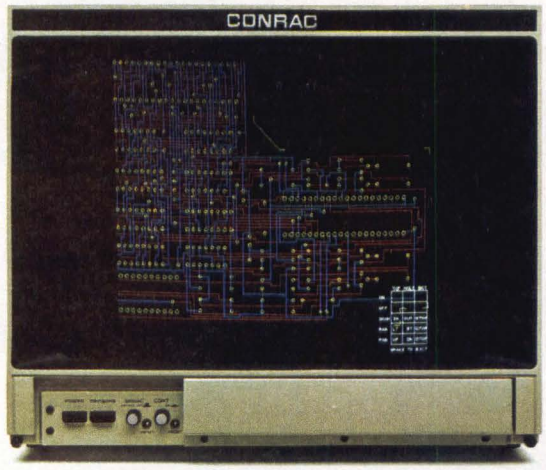
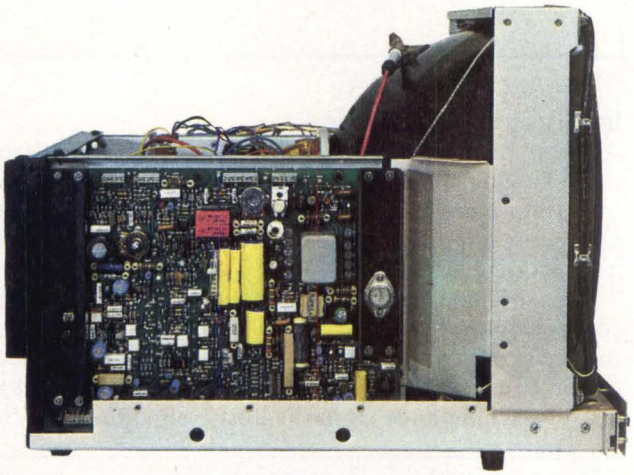
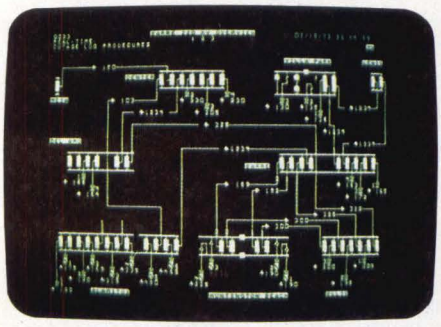
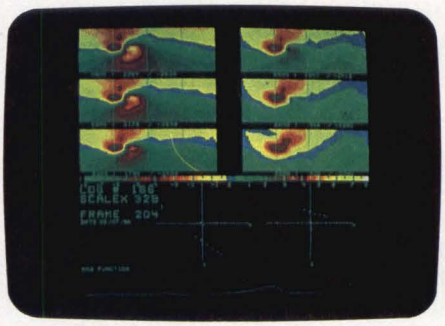


Screen data courtesy of Megatek Corporation.







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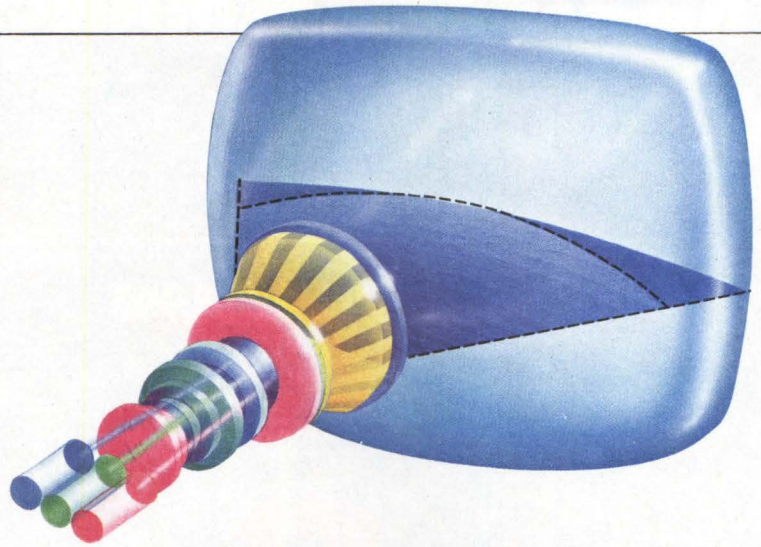

Dynamic focus: Clearly a Conrac edge.
This Conrac strong point assures center-to-edge image focus for ultimate clarity. Simpler display designs pretend the tube's screen is a concentric circle, with an equal radius from center to edge. The Conrac gun automatically compensates for the different gun-to-screen distances that are actually found in modern tubes. The end product is a consistently sharp image across the entire screen.

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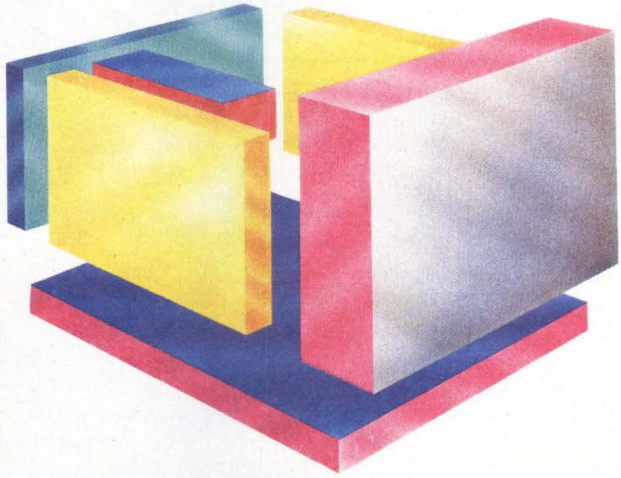

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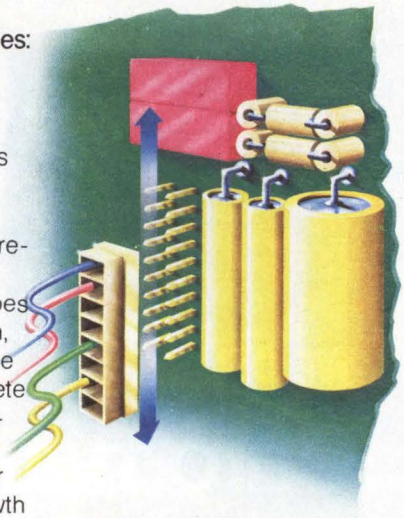

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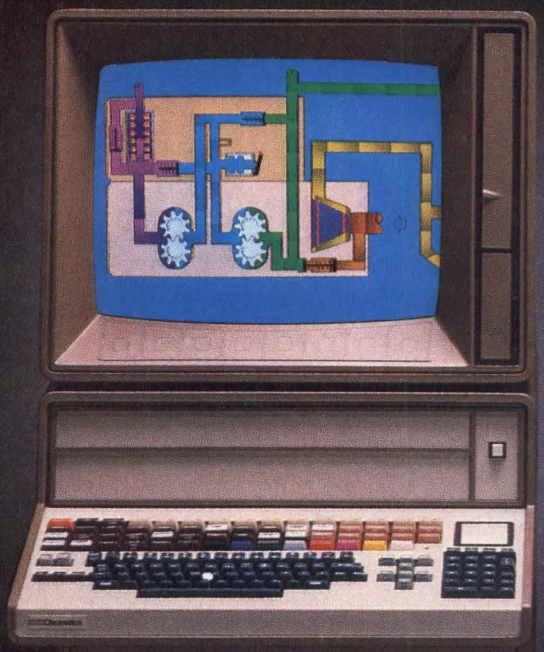

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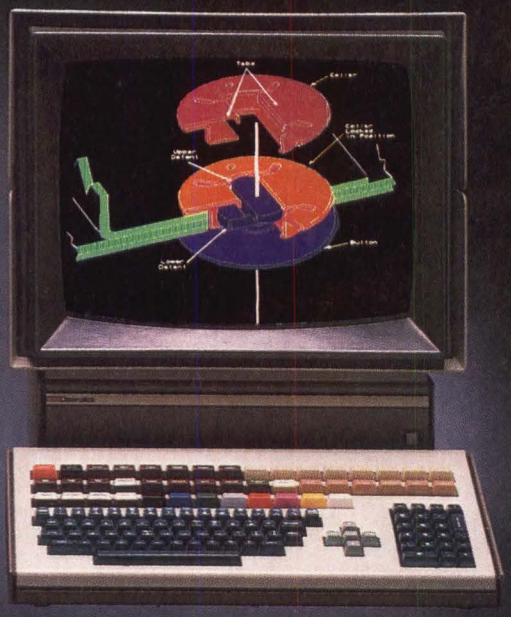

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CIRCLE 58

AN INTELLIGENT INTERFACE FOR DISK/TAPE SYSTEMS

When combined with an intelligent interface, disk and tape based storage units can carry out transparent offline transfers

by Richard Brechtlein

Development of a combined disk/tape system with hybrid interface is the result of converging trends in the design of small to medium sized computer systems. Fast, reliable Winchester drives with small to medium capacities have become the *de facto* standard for online storage, replacing the flexible disk and relegating it to a backup role. The availability of small 5.25″ and 8″ Winchesters is accelerating this trend, but there is a countertrend toward larger drives like the 14″, 20M- to 160M-byte Winchester that serves as the central storage and control element in the hybrid system described here.

A hybrid interface simplifies the task of integrating Winchester disks and streaming cartridge tape drives by using a single data and control cable to link the host computer to both disk and backup tape. Commands generated by the host determine the source and destination of data transferred across the interface. Equally important, data transfers between disk and tape can be accomplished completely offline, releasing the computer for other tasks. Even in this mode, however, the host can access the disk at any time by interrupting the transparent offline transfers.

Richard Brechtlein is vice president of marketing at Century Data Systems, 1270 N Kraemer Blvd, Anaheim, CA 92806. He has been involved in engineering and marketing of disk and streaming tape drives, video terminals, computer enhancement products, large mainframes, software systems, automatic test equipment, and interface devices.

Computer systems running under multi-user or time-shared operating systems, such as MP/M or UNIX, soon run out of storage capacity. The same situation can occur when a single-user CP/M system must support a variety of applications such as data processing, word processing, and graphics. In both cases, larger drives, partitioned into multiple logical disks, generally represent the most cost effective way to increase storage capacity without complicating the hardware or software.

Similar storage expansion forces are at work in the case of distributed processing systems and local networks. Economies of scale—the lower per-megabyte storage costs provided by larger Winchester drives—are leading to a recentralization of the data storage facilities. Thus Intel Corporation developed a firmware version of Digital Research's disk based CP/M-86 operating system. Applied to 8086 and 8088 processors, the firmware eliminates the need for fast access but higher storage cost at each user station.

Streaming cartridge backup

These trends, in turn, impact the techniques used to back up the Winchester drives, not only in archival storage and protection against hardware failure or operator error, but also in removable media storage for disk overflows, program loading, and exchange of programs and data among users.

Limited storage provided by even the highest capacity flexible disks means that multiple media exchanges must be performed by the operator whenever a large scale

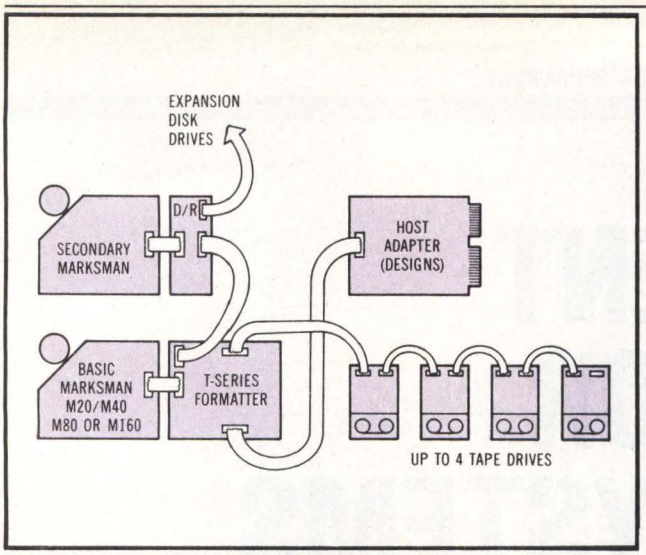

Fig 1 Expandable hybrid disk/tape system. Controller/formatter board mounted on first Winchester disk drive provides system intelligence. First streaming cartridge unit is also an intelligent drive. Fully expanded system has over 1G byte of disk storage and up to 180k bytes of tape backup without exchanging cartridges.

offload or restore takes place. Moreover, the amount of in-place backup storage immediately accessible to the computer is either limited or, if multiple drives are provided, expensive. One result has been a resurgent interest in economical, high capacity streaming tape. In the case of small to medium systems, there is particular emphasis on 0.25″ streaming tape cartridges offering data capacities of up to 45M bytes and drive form factors equivalent to those of an 8″ flexible disk.

To be efficient and effective, a streaming cartridge must literally stream. Step function degradations in performance can occur if the tape is frequently stopped and restarted. Interblock gaps pass under the read/write heads in approximately 30 ms and any interruption in data flow requires a time-consuming retrace and reacceleration before additional information can be written or read. Therefore, instead of the individual (eg, 512-byte) block transfers that characterize start/stop cartridge tape reads and writes, streaming tape dumps and restores are usually organized so that hundreds or thousands of kilobytes can be transferred in a single operation.

High volume transfers mean, even at the industry standard cartridge data rates of 30k or 90k bytes/s, both disk and tape are occupied for fractions of a minute up to several minutes. This is often an intolerable amount of time in terms of host access to other data files on the disk and a doubly intolerable interruption if the host itself must implement transfer by reading from one storage device and writing to the other.

Gigabyte storage system

Combining disk and tape into a single storage system with a hybrid disk/tape interface and a central storage system control circuit completely solves these problems. Such a system, illustrated in Fig 1, provides a separate offline data path for disk-tape transfers, freeing the host computer once the parameters of the transfer have been established. It is also possible to interrupt the generally low priority disk-tape transfers whenever a direct access to the disk is required by the application program or operating system. Except for an initial command sequence, the offline transfers are transparent to the host computer.

A controller/formatter board mounted on a Century Data Systems' T-series Marksman drive with a capacity of 20M, 40M, 80M, or 160M bytes is the central control element for the entire storage system. Computer system integration at the hardware level is reduced to the design of two elements: a host adapter board that plugs into the computer input/output (I/O) bus and a single cable between the host adapter and the controller/formatter. Software integration requirements are generally limited

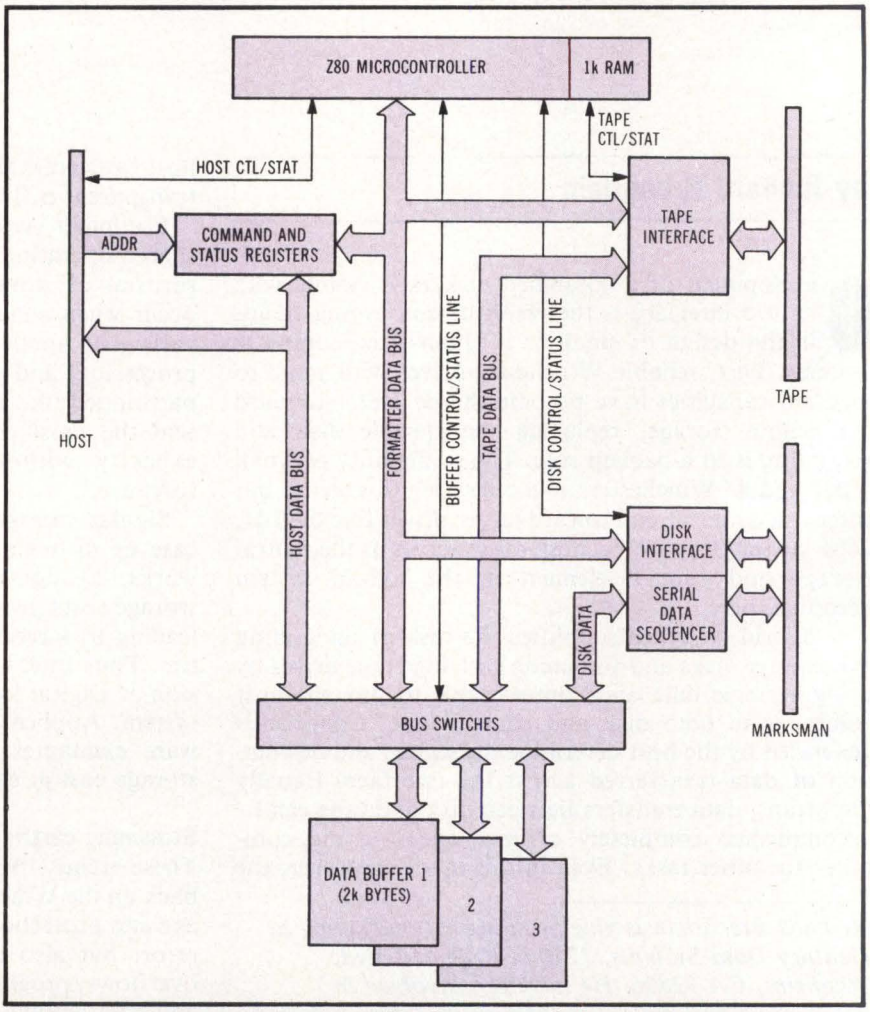

Fig 2 Hybrid storage system controller/formatter. Onboard microprocessor controls buffer switches that establish host-disk, host-tape, and disk-tape data paths. Command and status registers serve as communication links between host computer and microprocessor.

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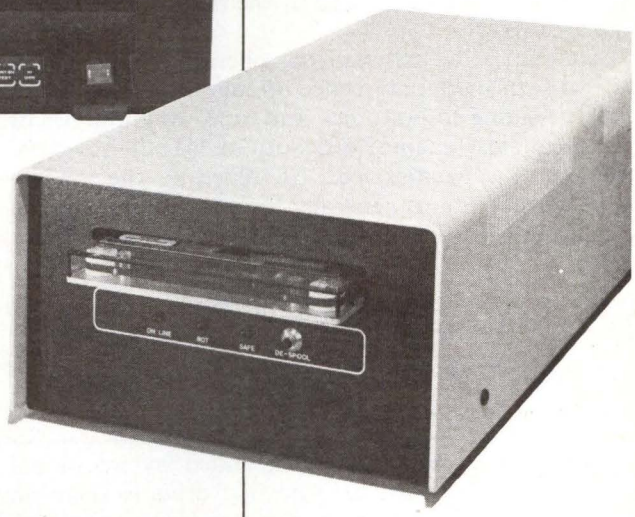

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TABLE 1

Hybrid Disk-tape System Interface Signal Net

Command/status register	Pin(s)
Data bus (8 lines)	2 to 9
Address bus (4 lines)	14 to 17
Host read	11
Host write	13
Host reset	19
High performance	
Data request	26
Transfer acknowledge	32
Host bus direction	23
DMA clock (2 lines)	33, 35
IM/T busy	24
Command complete	21
Transparent command busy	28
Transparent command complete	30

to modifications in the existing disk I/O driver and optional changes in the operating system or application programs to take advantage of the double-tiered disk/tape architecture.

Communication between the operating and storage systems is through a sequence of commands and status reports relating to both disk and tape. Any number of additional daisy chained disks (up to 255), in any combination of capacities, can be added to the system. Cable considerations generally limit the number to ten or less, but still allow expansion to over 1G byte of disk storage.

The software driver...can completely supplant the existing driver [in] the operating system.

Tape storage can also be expanded by additional streaming cartridge drives. The first drive is again an intelligent unit that interprets commands relayed by the T-series controller/formatter. Up to three expansion drives can be daisy chained to this unit to provide a total of 180M bytes of tape storage without exchanging cartridges.

Controller/formatter hardware

The onboard microprocessor shown in Fig 2 controls the flow of data through the controller/formatter circuitry but does not directly process the transfers. Instead, the connecting link that establishes a host-disk, host-tape, or disk-tape data path is a rotating bucket brigade of three 2k-byte buffers. Data are read into one memory module and read out of a second, with the third acting as the true buffer to compensate for average transfer rate inequalities. Thus, the host can communicate at burst rates up to 2M bytes/s while the disk is written or read at average rates that can range from a few kilobytes to over 500k bytes/s, depending on the location of the transferred files and the number of time penalties imposed by track seeks, sector interleaving, and rotational latencies. The three buffers ensure that at least 4k bytes of data can be read or written at the full streaming rate before the tape is halted.

Tape transfers flow to or from the intelligent streaming cartridge drives on byte wide paths. Tape formatting, cyclic redundancy check (CRC) calculations, and error detection/correction procedures are all performed by cartridge drive intelligence. A 1k-byte random access memory (RAM) stores tape status information for interpretation by the microprocessor firmware. A serial data sequencer associated with the disk interface (Fig 2) performs serial to parallel conversions for disk data and does CRC error checks on the serial data stream.

Hybrid interface cable

Three control lines and nine handshaking lines interface directly with the microprocessor, but the principal communications between host and microprocessor take place through two 16-byte registers. Commands and data transfer parameters are loaded into one register by the host computer and read by the microprocessor. The second register holds storage system status bytes that can be accessed at any time by the host software driver.

Data, command, parameter, and status bytes are all carried in bit parallel format by an 8-line bus terminating at a 40-pin cable connector on the controller/formatter bus (Table 1). Four additional lines address one of the 16-byte locations on either the command or status register. The balance of this basic command/status register signal set consists of three host control lines: a master reset for the entire storage system and two lines that indicate whether the host is writing into the addressed command register location or reading from the corresponding status register location.

The top location in both registers transfers read or write data bytes between the data bus and the first in, first out (FIFO) bucket brigade buffers. Simple storage or retrieval operations can be performed with the basic signal set. The remaining high performance lines in the interface cable increase the system throughput by signaling status instead of requiring the computer to periodically poll the status register. Four address lines specify one of 16 locations in either command or status register, depending on state of host write and host read control lines. Nine handshaking lines increase system performance but are not necessary for basic online and offline data transfers.

- *Data request*, when active, indicates that the storage system FIFO is ready for a data transfer, read or write.
- *Transfer acknowledge* is used by the storage system to indicate that it has read a write byte from the data bus or has a byte available for the host to read.
- *Host bus direction* indicates the direction of flow on the data bus. A low level indicates host to storage system; a high level indicates a reverse flow.
- *Intelligent Marksman/tape busy IM/TB* tells the host that the storage system is executing a direct command which, by definition, takes precedence over a transparent offline command. No other commands can be accepted while this line is active.
- *Command complete* signals that a direct command operation has been completed and that the storage system is waiting for a command acknowledge byte generated by the host computer.
- *Transparent command busy and completed* indicates the corresponding states for transparent disk-tape transfers that are accomplished offline and can be interrupted by any other direct command.

Two 8-MHz direct memory access (DMA) clock lines are for use by the host in a DMA controller.

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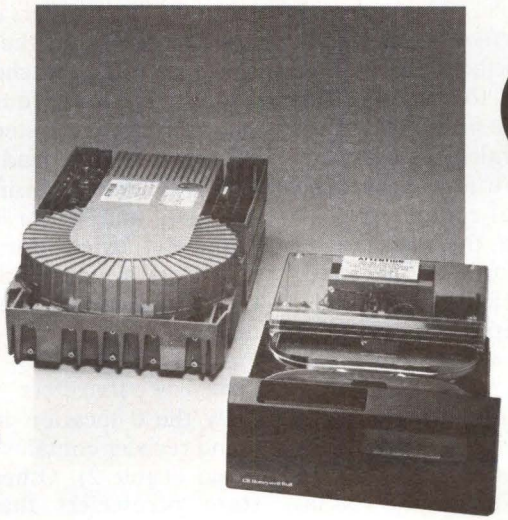

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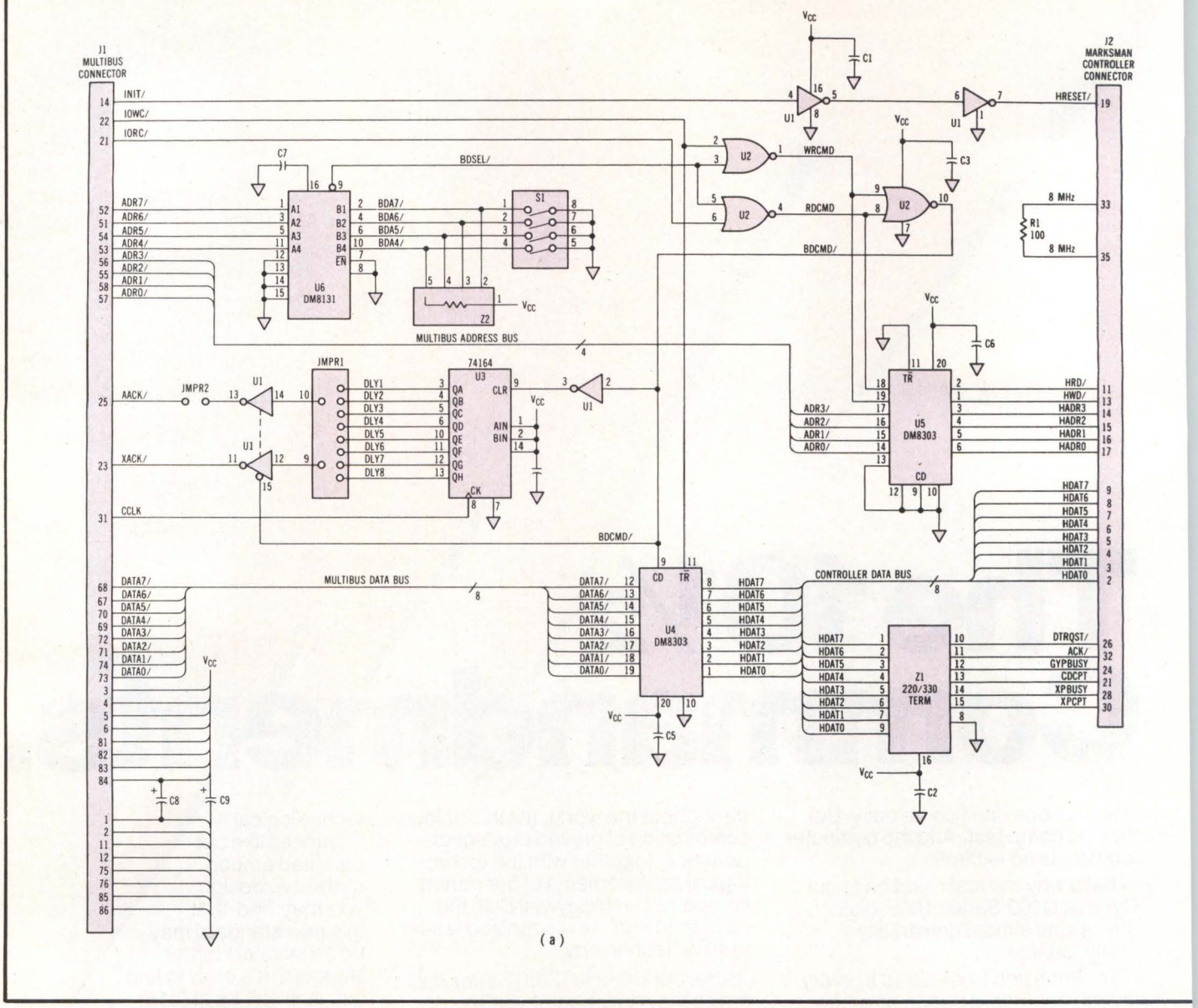


Fig 3 Host-adapter designs for MULTIBUS (a) and S-100 (b) computer systems. Address codes apply to 16-byte command and status registers on controller/formatter board. Device, cylinder, head, and sector addresses are transmitted to hybrid storage system as data transfer parameters.

Host adapter design

Relative simplicity of the hybrid interface is reflected in the host adapter circuitry that interfaces the storage system cable with the host computer I/O bus. Fig 3(a) shows a typical design for a MULTIBUS programmed I/O (MPIO) adapter. Fig 3(b) is the equivalent circuitry for an S-100 computer. Third parties are now generating similar interfaces for a broad range of computers.

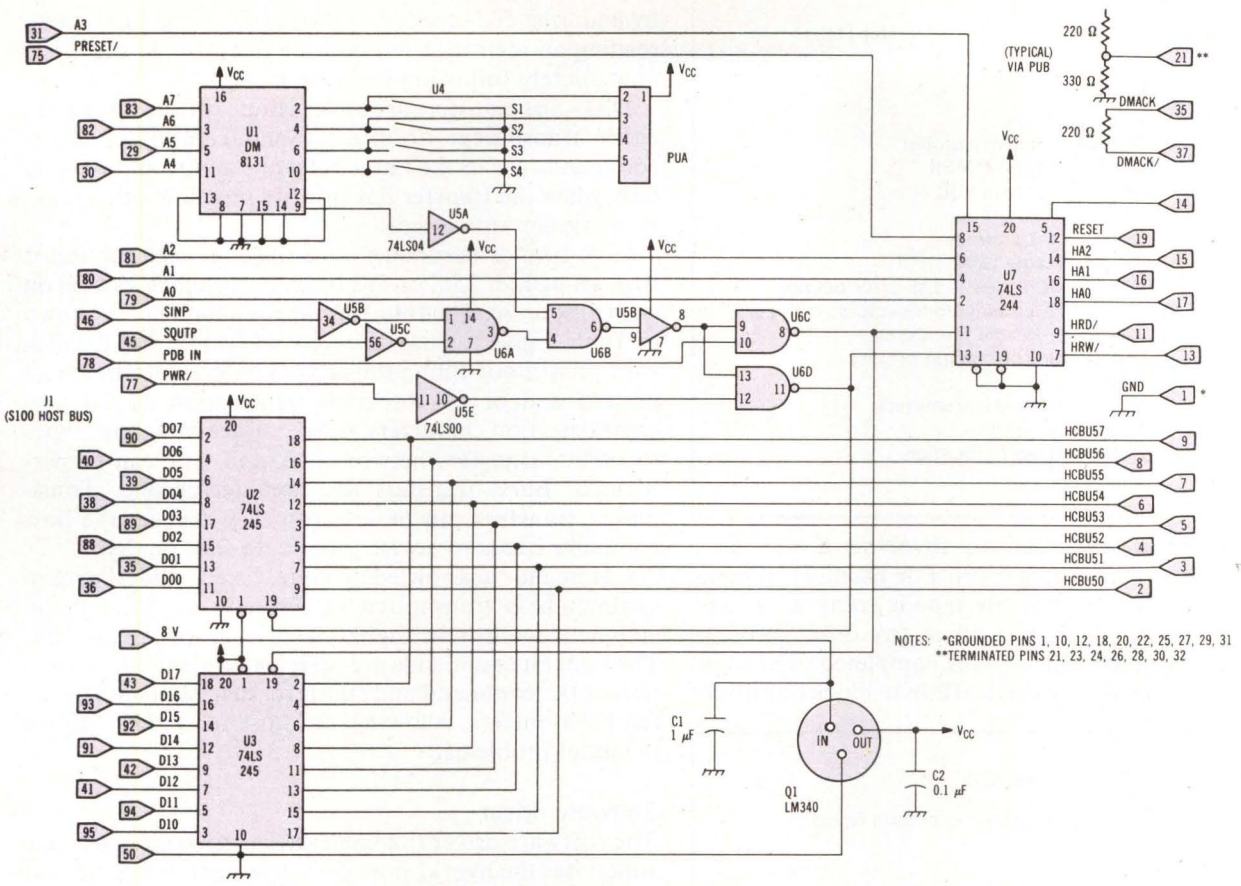
In the case of the MULTIBUS adapter, the host accesses the storage system via the 16 I/O ports on the MPIO, which generates all the MULTIBUS handshake signals. Jumper block 1 is used to select appropriate delays from the read or write strobe for the AACK/ and XACK/ signals required by the MULTIBUS. Delays are measured in clock periods from the strobe, or 250 ns for an 8-MHz clock. Jumper 2 enables the AACK/ signal.

Use of the MULTIBUS address lines to access the 16 command and status register locations is of special interest. The registers can be mapped to 16-byte boundaries anywhere in the 256-byte MULTIBUS I/O address space by using switches S1 through S4 to define a base address. The lower four bits of the I/O address go directly onto the storage system address bus to identify the appropriate read or load location.

All other addressing information, such as drive, cylinder, and sector numbers, are communicated as parameter bytes. Partitioning of a drive into two or more logical units is accomplished entirely in software by defining the first and last cylinders of each logical disk.

Command parameters

Only the 0 location in the controller/formatter command register contains a disk, tape, system, or test command (Table 2). Other available locations are used to store parameters that define the operation to be



(b)

performed. Principal function, therefore, of the software driver for the hybrid storage system is to translate operating system storage instructions into a correct sequence of command parameter bytes and status byte responses.

Several parameter bytes deserve special mention. The byte stored in location 8, for example, supports multiple sector accesses up to the full capacity of the disk. This increases, in turn, the compatibility of the system with such block oriented operating systems as UNIX and any local network architectures based on the transmission of blocks or messages.

Transparent command priority value stored in location 9 defines the number of consecutive cylinders to be transferred between disk and tape in an offline mode before the operation can be interrupted by a direct command from the host requesting immediate disk access. The lower the priority value, the more frequent the potential interruptions. The highest priority an offline transfer can have is nine cylinders, equivalent to approximately 1.5M bytes of data stored on a 40M-byte disk. The longest disk access timeout imposed on the host computer would therefore be less than 1 s in most cases.

Tape command parameters stored in location D initiate such specific streamer cartridge operations as rewinding, retensioning, and a complete erasure of all the data on the tape.

Command repertoire

Table 3 lists the command bytes recognized by the controller/formatter firmware. Nearly all are direct commands and cannot be superseded by loading another byte into location 0 of the command register until the specified operation has been completed and a command completion code (eg, successful execution or sector not found) has been stored in the status register. Hybrid storage system commands are stored in location 0. Location F serves as interface between host computer and FIFO buffers during data write transfers. Balance of active locations hold parameter values, defining operation to be performed.

Remaining commands are transparent. All relate to offline tape operations and can be interrupted by any

TABLE 2

Storage System Command Register Flags

Location	Definition
0	Command byte
1	Disk drive select number
2	Cylinder address MSB
3	Cylinder address LSB
4	Head select number
5	Start sector address
6	User definable byte
7	Number of retries if disk error occurs
8	Number of consecutive sectors, cylinders, blocks, or tape file marks
9	Transparent command priority
A to C	Reserved
D	Tape command parameters
E	Tape drive select
F	Data FIFO write location

subsequent direct command not involving a tape drive control, read or write operation. For example, a command to position (rewind) the tape is transparent and the host computer is free to issue any other nontape command before the operation is completed. The same is true of advance file marks—512-byte blocks of driver generated illegal code the user can insert into the tape record at any point to separate files and relocate them by counting file marks from the start of the tape, or by reading an identification code or directory in the block immediately following each file mark.

Disk-tape transfers are always done offline but can be either transparent or direct (noninterruptible). Burst commands are in the latter category and would be used only when the transfer has priority over any other computer system operations.

Disk format parameters are fixed, except for sector size, set at 128, 256, or 512 bytes by switches located on each disk drive. The four format command codes shown in Table 3 give the user a choice of formatting the disk with or without filling the sectors with a specified byte pattern and/or a subsequent verification of the CRC error detection characters and recorded data. Two types of offline transfers between disk and tape can be performed. Burst transfers are noninterruptible. Transparent transfers can be interrupted whenever the host computer needs to access other data files on disk.

Command acknowledge code listed under system commands is transmitted in response to a command complete handshake signal from the storage system. The five test commands are designed to verify the operation of the command and status registers and data transfer FIFO buffers, allowing the host to quickly isolate potential problems.

TABLE 3

Hybrid Storage System Command Bytes

	Opcode (Hex)
Disk commands	
Boot	10
Sequence drive up	20
Sequence drive down	30
Format	40 to 43
Read	58
Write	60
CRC track verify	70
Read drive status	80
Seek	90
Drive identification	A0
Tape commands	
Position	F0
Write data	F1
Write file mark	F5
Read data	F6
Advance file mark(s)	FA
Read status	FB
Disk/tape commands	
Burst disk backup	B0
Transparent disk backup	B4
Burst disk restore	B8
Transparent disk restore	BC
System commands	
No-op	00
Command acknowledge	C0
Read transparent command status	C1
Transparent command completion acknowledge	C2
Test commands	
Memory dump	01
FIFO fill	02
FIFO access test	03
Command/status register test	04
Formatter identification	08

Software driver

The software driver that generates these commands and supervises the hybrid storage system operations can take several different forms, depending on the computer, operating system, and objectives of the system programmer. It can completely supplant the existing driver incorporated into the operating system, or it can be attached to the existing driver software, thus adding to the capabilities of the system without reducing the hardware flexibility.

Both approaches have been incorporated into commercially available software packages. In one case, applicable to system environments such as CP/M 2.2, customized software is created by integrating the user's existing console, printer, and flexible disk drivers into a skeletal basic input/output system (BIOS) provided on magnetic media. Both cold and warm boot operations are supported by CP/Ms BIOS module. Conditional assembly switches allow the user to configure the hybrid system segments to the known capacity of the disk drive: 20M, 40M, or 80M bytes. The user must also establish the base address for the 16 command/status register I/O ports and reconfigure the computer memory to allow for the expanded system software. Logical 8M-byte disks defined by the driver are referenced, according to CP/M convention, by alphabetic characters starting with A.

The same software supplier offers a utility package that permits the user to quickly integrate hybrid driver patches into the existing host BIOS. The attach program has two sections. The first makes any necessary BIOS modifications such as changing jump locations for disk related subroutines. The second section is the BIOS coding required to drive the hybrid storage system.

Other programs included in the utility package facilitate disk formatting and verification operations.

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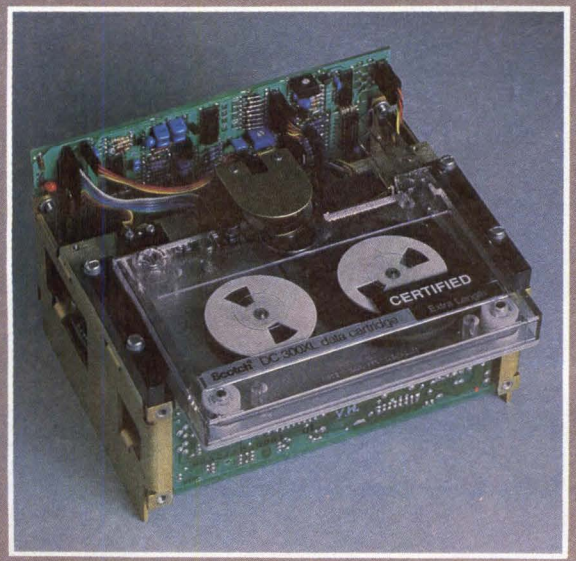

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Among other functions, the program creates a media map that automatically compensates for any defective areas encountered on the drive. The balance of the package consists of a disk/tape backup and restore utility that allows the user to transfer logical disks and selective files to and from the streaming cartridge drives.

Friendliness

The utility is a menu driven program prompting the user with the appropriate questions and valid answers at each decision point. For example, on entering the program, the user is given the following choices: B—backup; R—restore; S—transparent status update; and V—verify.

B option allows transfer from the disk to the tape, while R will reverse the process. During a transparent backup or restore operation the user can use the S option to read the status of the operation. V performs a tape/disk comparison to ensure data integrity.

After the selection of B, R, or V, the program responds with pre-backup (restore) positioning; E—erase tape; R—rewind tape; T—retension tape; and N—none of the above.

E and R operations perform the indicated functions. Retension command will move the tape with no transfer of data, from the beginning of tape (BOT) to the end of the physical tape and return to BOT. This helps reduce read or write errors by reducing any play in the tape cartridge.

If a restore or verify command was initially selected, the next option presented to the user will be: pre-restore file search, advance to a new file, enter Y or N. A yes response will result in the following question: number of files to advance from current tape position (1 to 9); enter 1 to 9.

Once the entry is made, the tape begins to move forward, looking for file marks. If a 1 is entered, the tape will stop at the first file mark and request the logical drive number. Additional prompts and responses allow the user to select a specific logical disk, a burst or transparent mode, and the level of priority for transparent transfers.

Availability and convenience of a system capable of making transparent disk/tape transfers is certain to modify existing data storage practices.

Summary

Availability and convenience of a system capable of making transparent disk-tape transfers is certain to modify existing data storage practices. Clearly, more than backup is involved. The entire 8M-byte contents of a CP/M logical disk, for example, can be transferred to tape, or restored, in less than 2 min. Number of users who can periodically, but routinely, use a computer system is no longer limited by the number of logical disks supported by the hardware and operating system. Instead, users can offload all stored data and programs at the end of each session, releasing the space for additional users.

File markers on the tape record also allow the user to perform a number of file management functions with each transfer between disk and tape. Records and files can be sorted and merged, for example, in a transparent mode without burdening the computer. Moreover, partitioning of a disk into fixed size logical units will usually leave a spare smaller logical disk, permitting the user to assemble or disassemble data at the disk level before or after a disk-tape transfer.

Applications such as these indicate hardware and software integration of the new hybrid storage systems is only the first step. Looking ahead, major changes will occur in the way applications are written and in the operating systems that process them. New hardware tradeoffs are also possible—affecting both the architecture and costs of future computer systems.

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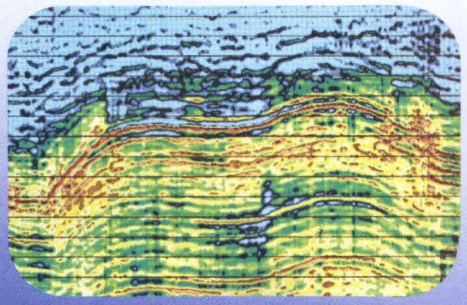

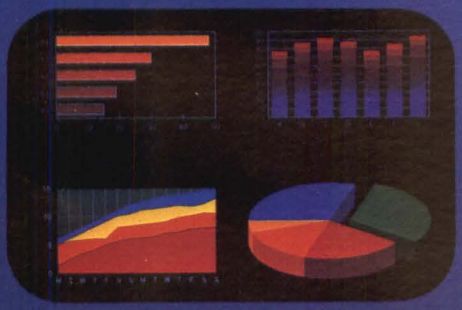

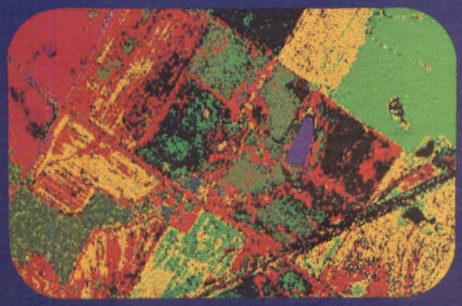

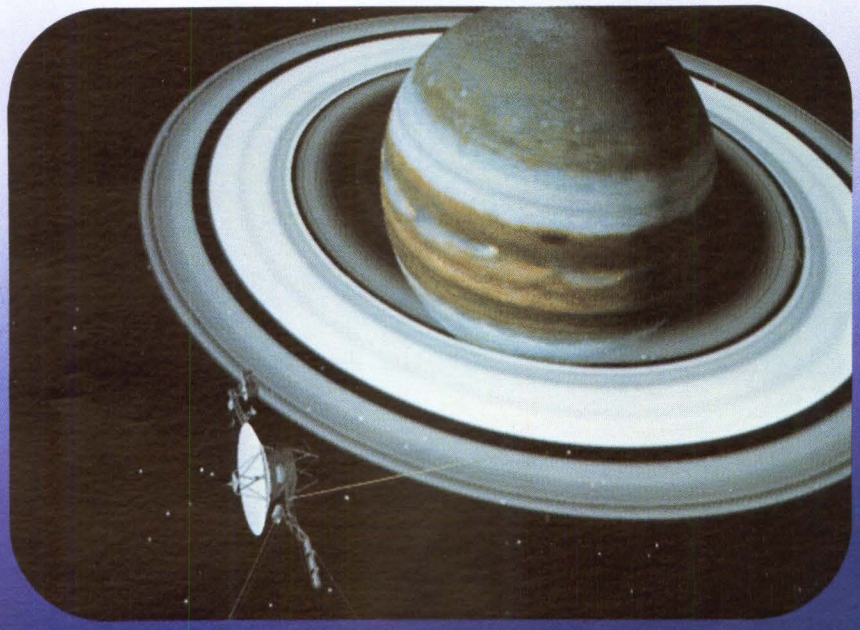

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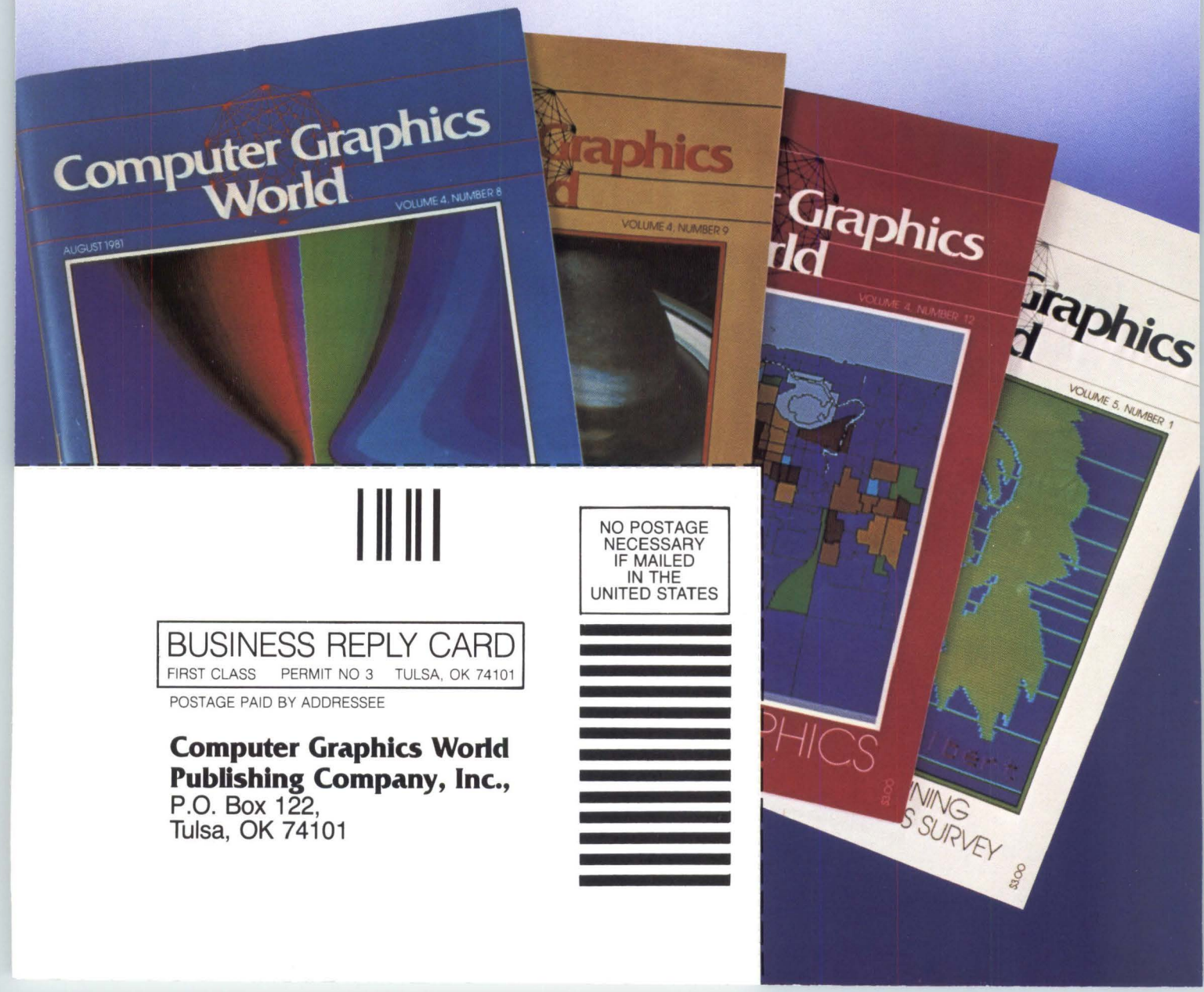

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A SMART OPERATING SYSTEM FOR 8-BIT MICROS

When intelligence resides in software rather than hardware, microcomputers gain I/O flexibility and mainframe features

by Roy Soltoff

After spending a few hours at computer shows such as NCC or COMDEX, it becomes obvious that all microcomputers look surprisingly similar. Each comes equipped with the same features: cathode ray tube monitor, keyboard, one or more floppy disk drives (usually 5.25″ mini-floppies), 48k to 64k bytes of random access memory, and a processor card. With the industry seemingly adopting CP/M as a pseudo standard operating system, Zilog's Z80 or Intel's 8080 are the processors usually chosen.

Though the design must be straightforward, each manufacturer attempts to make its machine more desirable. This is done by providing greater reliability, flexible interfacing, more peripheral support, additional hardware features, attractive packaging, and lower cost. However, an important ingredient often overlooked by both manufacturers and users is the cost effectiveness of using smarter software.

Alternative operating systems are available that bring a great deal of mainframe power to the microcomputer. One example is a truly powerful operating system designed for an 8-bit microcomputer that uses the Z80 processor chip. This system provides a single user system with device independence, dynamic file space allocation, extensive file management, job control language structures, and a large library of utilities, plus the ability to interface easily to disk storage devices with capacities from 88k-byte mini-floppies to 13M-byte Winchesters. In addition, error trapping and an English language command structure make Logical Systems' LDOS a user friendly operating system.

Roy Soltoff is vice president of Logical Systems, Inc, 5904 Edgehill Dr, Alexandria, VA 22303, where he is responsible for operating systems design. Mr Soltoff is the founding president of MISOSYS (a microcomputer systems company) as well as co-author and publisher of "The BØØK, Accessing the TRS-80 ROM." He has a BSEE from George Washington University.

Intelligent operating system

When confronting either a future machine design project, or perhaps a current one, a study should be made to weigh the relative merits of implementing additional features via hardware or software. Since the technical documentation supplied with LDOS is over 75 pages, only those elements of the operating system that will maximize intuition of design and enhance hardware will be discussed.

Fig 1 is a block diagram of the operating system. Essentially, the system has two interaction levels—command and primitive. At the command level, the operator enters a command that requests the execution of some function (listing a file, displaying a disk directory, running a BASIC program, or compiling a C language source file). The command interpreter parses the user entry, determines whether the request is for a system function or a user supplied function, and then arranges for the necessary system resources.

System resource allocation takes place on the primitive level, and is requested via a supervisor call processor (SVC). The SVC is associated with all system primitives (ie, get a character, put a character, open a

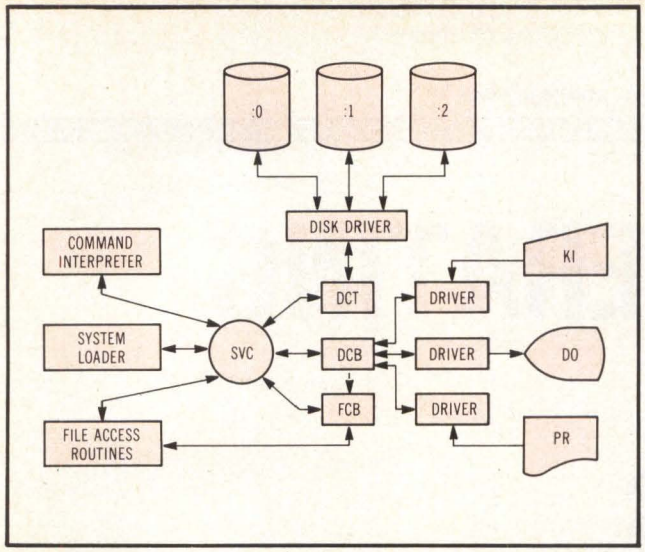

Fig 1 LDOS block diagram. Users interact with system on one of two levels, system or command.

file, add a task, read a directory record, etc). Application software written in a low level language such as Assembler makes direct use of primitive level SVC operations. Programs that use high level languages like BASIC, C, or Pascal do not need the SVC because system interfacing is done within the language interpreter or compiler.

This operating system supports up to eight logical disk packs or volumes, logically numbered 0 through 7. Each floppy is treated as a single volume. Rigid disk drives (Winchesters) can be treated as either a single volume or partitioned into multiple volumes. A drive code table (DCT) contains the parameters associated with each disk, such as number of cylinders, heads, and sectors/track, as well as interfacing the disk software driver to the system.

Byte input/output (I/O) devices such as keyboard, video display, printer, and RS-232 serial ports and their associated software driver routines, are interfaced to the system via device control blocks (DCB). I/O devices are identified by a 2-character device name including KI (keyboard input), DO (display output), PR (printer), and CL (communications line), and prefixed with an asterisk when entered as a device specification. Additional devices can be defined and added to the system once an appropriate software driver is available. Device name selection is left up to the user.

A file is denoted by a file specification. A complete file specification consists of a file name of up to eight characters, a file extension of up to three characters, a file password of up to eight characters, the logical drive specification, and as an option in certain cases of partitioned data sets (PDS), a member specification of up to eight characters. Whenever users institute a structured naming convention, most files are accessible via the file name reference only. The operating system will search all drives for a file if the drive specification is omitted from the file specification. Many system utilities and user applications can use default file extensions to separate files into classes. For example, if all BASIC programs use the file extension of BAS, it is unnecessary to enter the extension to reference the program file. Similarly, the operating system makes extensive use of default file extensions such as JCL for all job control language, ASM for assembler source, and CMD for all directly executable files.

One example of device independence is that file specifications and device specifications are generally interchangeable. Thus, wherever a file specification is needed, a device specification can usually be entered. For instance, the copy utility is primarily used to copy a file from one disk to another:

```
COPY ARTICLE/TXT:0 TO ARTICLE/TXT:1
```

which creates a duplicate on drive 1 of the file specified ARTICLE/TXT located on drive 0. In lieu of file specifications, device specifications could also be used:

```
COPY *KI TO *PR
```

which copies keyboard input directly to the printer. A keyboard can easily be added to a daisy wheel printer, making it a temporary typewriter. Perhaps a more useful illustration would be the convenience of directing program output to video display, printer, or a file depending on the device/file specification provided.

The acquisition of disk file space is completely transparent to the user. This frees the user from worrying about sectors, tracks, cylinders, heads, and even disk drives in most cases. File space is dynamically obtained for any given file when space is required. Since directory accesses are dynamic (ie, a disk access is made any time directory information requires updating), users can change floppy diskettes in a disk drive without logging the action as long as files are not in the process of being accessed on the removed diskette.

...the overall price of software intelligence can be significantly lower than the corresponding design and manufacturing costs of hardware intelligence.

Files do not have to occupy contiguous space on a disk, but can exist in chunks of space called extents. Linkage maps that connect each extent exist in a file's directory. Access to a file is achieved by placing the file specification in a file control block (FCB) and issuing the open SVC. Directory information, needed by the file access routines, is then placed in the open FCB. Thereafter, SVC requests for file positioning, reading, and writing are available to access any record in the file. Fixed record lengths from 1 to 256 bytes are directly available at the SVC level. Languages like BASIC generally provide for sequentially accessed files with variable record lengths.

Although the supported functions are many, the operating system requires a minimum of the machine's random access memroy space. Only frequently used routines are resident in memory while others are brought into an overlay region on an as required basis. All of the identified functions in Fig 1, except the device and disk drivers, are contained in a 4k memory space (4096 bytes), that includes a 1k overlay region (1024 bytes). The remaining 3k region (3072 bytes) is the resident part of the system (SYSRES). Fig 2 shows a rough memory map highlighting the block functions of SYSRES.

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CIRCLE 63

Task scheduler

The task scheduler (Fig 2) assigns the execution of small background tasks at periodic intervals. Primarily, a hardware generated interrupt to the Z80 processor determines the time intervals. A desirable minimum interrupt rate would be 40 to 60 Hz. This clock is software divided by eight to produce high and low level task control. The operating system provides for eight low level tasks and four high level tasks. For example, with a 40-Hz interrupt rate, four discrete tasks can be processed at 25-ms intervals while eight other tasks are processed at 200-ms intervals. Software time of day routines, printer despooling routines, address trace functions, keyboard type-ahead scanning, blinking cursor routines, or other processes that need to be examined at periodic intervals are types of tasks that would generally operate from the task scheduler.

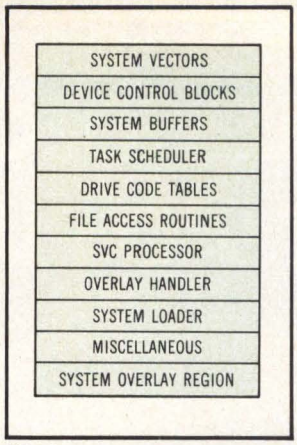

Fig 2 LDOS memory map. 3k of RAM is occupied by resident system programs and 1k (system overlay region) is reserved for less frequently used routines brought in from disk as needed.

The task scheduler is also used by the printer spooler's despooling function. Any device output can be spooled to the printer. The spooler implements a combination of memory and disk buffers to temporarily hold the printer output. This output is despooled to the printer under the control of the task scheduler. Transparent to the user, the function can continue the despooling even after the application generating the output is finished and another begun.

It is obvious, from the types of tasks handled by this scheduler, that many of the peripheral functions generally handled by hardware could just as easily be handled in software at a reduced cost. Keyboard type-ahead is a specific example of how software can reduce hardware costs. This feature is quite significant to a fast typist. Type-ahead is even advantageous to slow operator entry because of the ability to enter responses in anticipation of known queries. The operating system provides a 128-character type-ahead buffer that is more than adequate for all operators.

Storage directory

Facility for managing and accessing files on disk storage devices is the primary function of any operating system. Since the user must not be burdened with the physical details of the storage process, it is the operating system's responsibility to translate all file record access requests into specific drive, track, sector, and head parameters that pinpoint the storage location of each record. Because of the wide range of storage capacities supported by LDOS, it is important to detail the methods that accomplish flexibility of interfacing.

Organizing a disk pack. Each track is formatted into 256-byte sectors, with a maximum capacity of 32 sectors/track. Sectors are grouped into blocks—granules—that vary in size according to total track capacity. An additional granule is allocated whenever more disk space is needed for a file. The granule thus becomes the minimum storage unit. Where multiple headed drives are in use, the track numbers on a surface are duplicated on each surface with all similarly numbered tracks constituting a cylinder (track). Cylinder capacities also have an upper limit of 256 sectors/cylinder or 8 granules/cylinder, while the system supports 8 heads/drive, maximum.

Files are uniformly distributed across each surface to evenly use the entire disk surface. That means the head has a tendency to be randomly located whenever a directory access is needed. Because of this, each disk drive's directory is placed on the cylinder closest to its midpoint, minimizing the average seek time for directory accesses. The directory contains information on each file stored on the drive, as well as additional tables and codes pertinent to the drive.

The first sector of the directory contains a granule allocation table (GAT), bit mapped to each granule of space on the drive. One byte is used for each cylinder of storage with a maximum table capacity of 202 cylinders. Other fields in the GAT contain the pack name, date of creation, pack password, and data pertaining to the configuration of the drive. By multiplying the maximum capacities

(202 cyl/drive)(256 sec/cyl)(256 bytes/sec) = 13,238,272

a capacity of 13M bytes of directly addressable storage on each of eight drives is computed. Greater capacity rigid disk drives can be supported by partitioning them into two or more logical drives. Also, where a physical parameter exceeds the operating system's upper limits, translation techniques can be used in software.

For example, LDOS currently supports the Shugart SA 1000 Winchester, which has physical parameters of 32 sectors/track, 4 heads, and 256 cylinders, and a capacity of 8.39M bytes. The DCT is organized in the operating system as 128 cylinders of 256 sectors each. Moreover, the software driver easily translates to the drive's physical parameters. Similarly, the Seagate Technology's ST512 Winchester physically has 306 cylinders, 4 heads, and 32 sectors/track. The operating system organizes the DCT as if the ST512 were 153 cylinders of 256 sectors/cylinder. Again, intelligent software provides flexibility that allows for easy interfacing.

To open a file for access, the system needs to search the directory for its record. Using a hashing technique to reduce the 11-character string formed from the file name and extension to a 1-byte value ranging from 01 to FF (hexadecimal) minimizes search time. The hash code for each file is stored in the second sector of the directory, the hash index table (HIT). Each position in this table corresponds to a specific directory record, 32 bytes in length. A sector in length, the hash table can index 256 directory records or files, maximum. The directory, a maximum of one cylinder (up to 34 sectors), is sized according to disk capacity. Thus, the larger the disk storage capacity, the larger its directory, and the greater the number of file names that can be stored.

When a file is opened, the file name and extension are gathered from the specification and put through the hashing algorithm. The HIT sector is read and searched for a matching value. When a match is found, the directory sector containing the corresponding directory record is read. To guard against a different file

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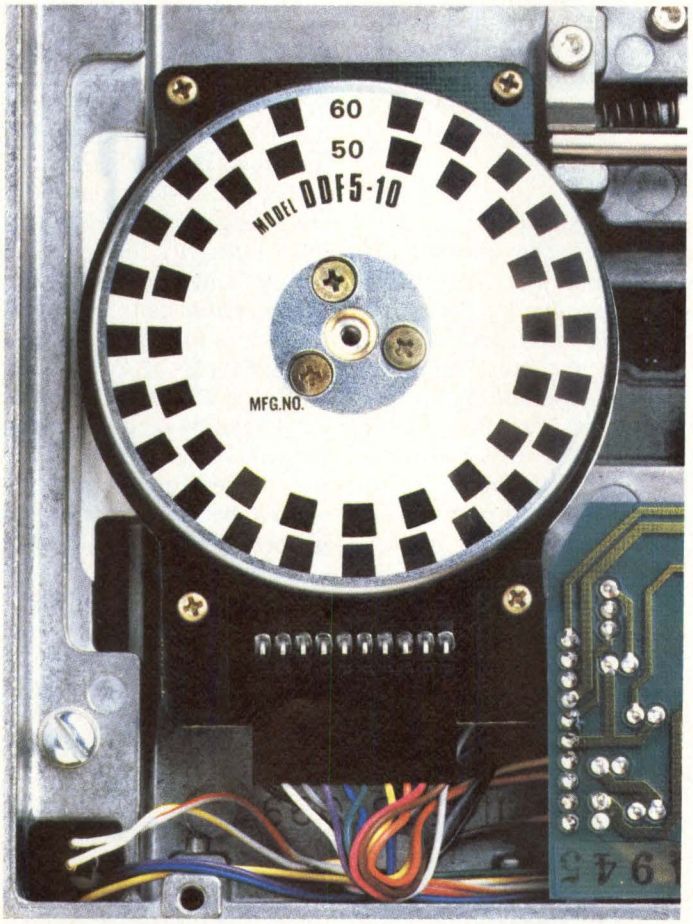
THE HIDDEN TRUTH ABOUT 5¼ INCH FLOPPYS

Belts and Brushes Murder on Life Span

The bad news for mini floppy disk drive buyers is that 5¼ inch drives are designed with belt and brush type AC motors . . . and they suffer the consequences. The good news according to high level authorities is that there is an exception. The Remex PICO™ 48/96 tpi, 5¼ inch flexible disk drive has no belts or brushes because it is the first mini-sized floppy with a direct drive DC motor. Direct drive means that improper belt seating is nonexistent so variations in speed and friction-producing side loading are eliminated. Motor life is also extended. A reliable industry source indicates that the MTBF of the PICO motor is 5 years—typically ten times that of most brush type motors. The President of the United States, in his comments, stated (continued on Page 5).

Trouble Maker Eliminated

"Tap-tap wear is a thing of the past" according to design engineers evaluating the Remex PICO 5¼ inch flexible disk drive. This major cause of media damage and wear on mini floppy drives, the loading and unloading of the head on the media, has been eliminated with the Remex PICO because the PICO has no head load solenoid.This design innovation also reduces magnetic leakage which may result in data errors. Rumors that PICO will receive an award from the Association for the Preservation of the Sanity of Systems Designers were not confirmed by Remex.



Direct drive DC motor saves life of 5¼ inch floppy.

Designers Spellbound by Interchange

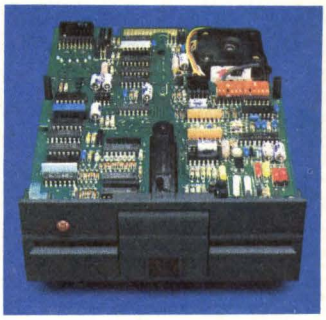
Reliable interchange of media between Remex PICO drives is enhanced by the precise speed control of the motor's closed loop servo. Speed is regulated to 1% on Remex PICO versus typically 2¼% on other small drives, therefore read/write errors caused by speed variation are not a major factor with PICO. The drive's speed control may also simplify controller design because phase lock loop requirements are less demanding. Vast crowds of cheering engineers stood outside the office of (continued on Page 11).

Drives Embezeled!

A choice of bezel sizes on the Remex PICO 48/96 tpi, 5¼ inch floppy makes this drive the appropriate choice for a wide variety of system configurations according to sources. Among the sizes available is a 2¼ inch low bezel which is ideal for space limited micro-systems. An "industry standard" bezel is optional.

Proud Parent Praises PICO

Remex is a Division of Ex-Cell-O Corporation, a Fortune 500 company with manufacturing and marketing arms in such industries as machine tool, aerospace and automotive as well as electronics. Ex-Cell-O Corporation through its Remex Division is committed to advanced technology development and quality manufacture of both 5¼ inch and 8 inch flexible disk drives.



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name/extension hashing to the same value—a collision—the 11-byte string is then checked for a match. If the correct record has not been retrieved, the HIT is examined further.

Information contained in the directory record includes the date the file was last modified, its update and access password codes, and its access level, as well as attributes—whether it is a SYStem or PDS file and if a backup has been made, the relative number of the last sector in the file, and the last byte within the last sector. The record also contains the physical storage in use by the file by pointing to the cylinder, relative starting granule, and number of contiguous granules for each extent linking up the file. When a file has more than four extents, additional directory records are used as required, with forward and backward pointers linking each record.

Flexibility of the file management utilities is considered an important feature by many users. Copying files from one drive to another, appending two files together, listing files with structured formatting, renaming files, removing files, obtaining disk directories, and making archival backups of favorite files are some popular functions. Backup is one of the most important in light of the tremendous capacity available in large storage devices.

Backup utility

Ever since small Winchester drives started to appear, interfaced to small microcomputers, the question of how to back up these devices loomed large. Although some installations consider streaming tape for backup (a relatively expensive added cost) and others incorporate video cassette recorder interfaces, the most popular, least expensive, and widely available method by far has been the use of floppy diskettes. However, floppies do have a serious drawback. Comparing available capacities of a single floppy to a small Winchester, it is obvious that several diskettes are required to back up the one hard drive.

A sophisticated backup utility can ease the frustration of archiving hard disk files. With the availability of 80-track, 2-headed mini-floppies, over 700k bytes can be stored on a single 5.25″ diskette when operating under double density modified frequency modulation format. With 2-headed 8″ drives, 1.2M bytes of storage exist on a floppy diskette.

The backup utility provides exceptional flexibility. For example

```
BACKUP :4 TO :2
```

will copy all files from logical drive 4 to logical drive 2. If both drives are floppies with the same physical configuration (ie, both 40-track, 2-headed with the same density), then the backup will automatically be performed track by track. This is the mirror image process. In addition,

```
BACKUP /TXT:3 TO :5 (OLD)
```

will copy all files with a file extension of TXT from logical drive 3 to logical drive 5, but only if the file already exists on logical drive 5. The use of the OLD parameter permits organization of archival copies.

```
BACKUP R$S/BAS:4 TO :2 (MOD,DATE=''11/09/81-
                        11/15/81'')
```

will make copies of all files from logical drive 4 with a file name that starts with the character R, has S as the third character, and accepts any character in all other file name character positions. Also, files must have last been modified between November 9, 1981 and November 15, 1981 inclusive to be included in the backup. In addition, the file must not have been backed up since it was last modified.

These examples illustrate flexibility in managing archival copies of working files. When used in a hard drive environment, large capacity floppy diskettes can store selected classes of files, with working files backed up in a structured manor only if they have been modified. As daily churning of working files is minimal, a procedure that enables a backup only if a working file has been modified within a class lends itself to optimal file management techniques without the need for expensive backup hardware. A separate utility provides diskette spanning capabilities for the backup when a single file exceeds the capacity of a single floppy.

In most machine environments, the command to obtain a directory display is frequently used. The operating system recognizes the utility of this function and provides many features for this command. For instance, the listing is sorted alphanumerically by file name/extension. When the length of a listing exceeds the video display's line capacity, paging is performed with a pause at each page. For each file in the directory, the listing provides data on the protection level, logical record length, file length (in kilobytes), date of last update, and whether a backup copy exists. A partial file specification can be requested to limit the listing to those files in the class similar to the backup utility.

Two types of access support disk files—record I/O and byte I/O. Logical records from 1 to 256 bytes in length can be read or written using the read or write SVC requests. Record I/O can be random access (by position SVC requests prior to read/write) or sequential access using repetitive reads or writes. File byte I/O is accomplished by get and put SVC requests and is essentially the same as record I/O with a logical record length equal to one. However, if get and put are used to implement sequential access, then a file can be considered a byte I/O device just like a printer, a serial port, or a video display. Therefore, a byte I/O request is independent of the physical device connected to the control block that requests the I/O. This makes the system device independent.

Several system library functions used to support device independence, such as the filter, link, reset, route, and set commands are provided by the system. An illustration of the use of these commands lends to an understanding of the full power of device independence. For example, if a suitable software driver (with a file name of RS232/DVR) is available for a serial port (RS-232 channel), then a simple

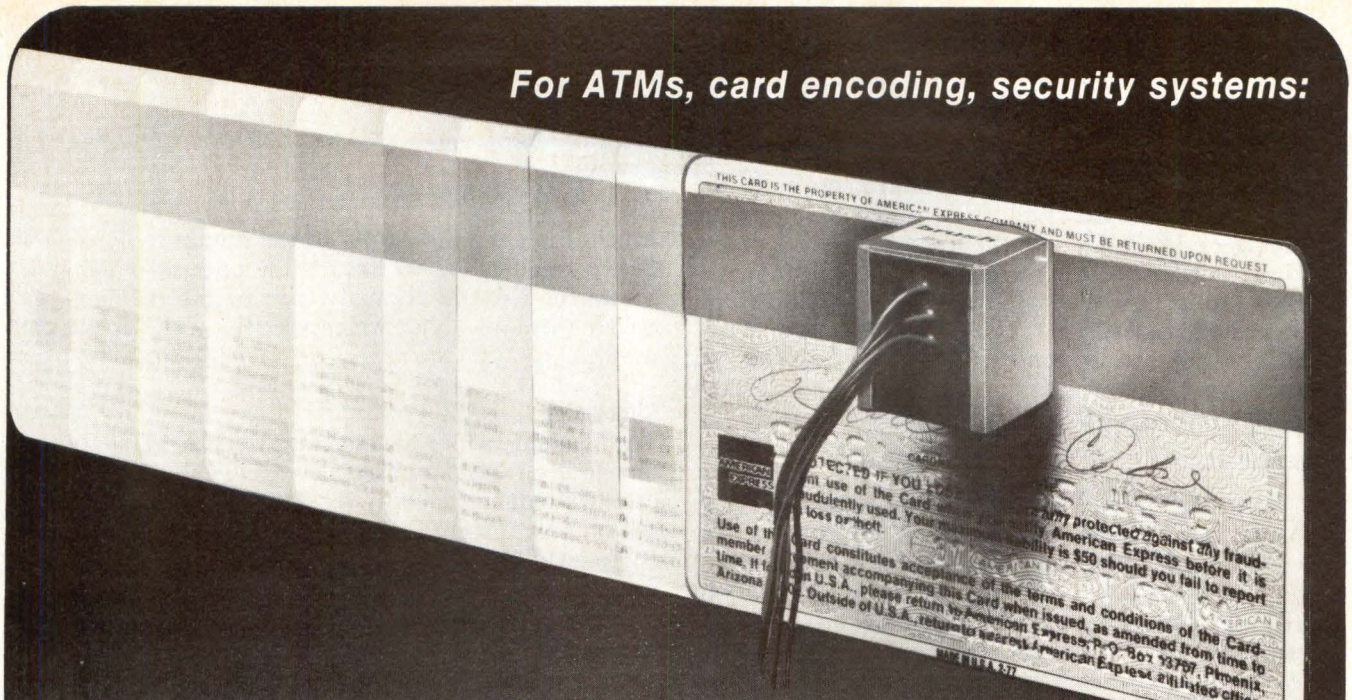
```
SET *CL TO RS232
```

will establish the serial port as a device, with CL as the device name. If the driver is written to accept parameter changes from the command line during installation, then a command entry of

```
SET *CL TO RS232 (BAUD=1200,WORD=8,STOP=1)
```

will establish the serial port using the parameters entered in the command line.

For ATMs, card encoding, security systems:



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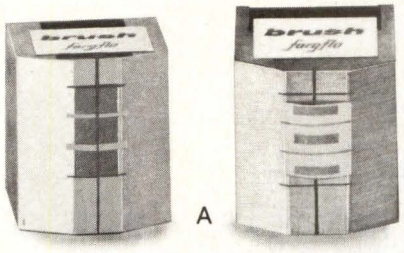
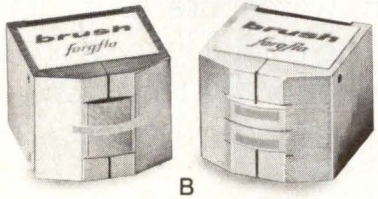
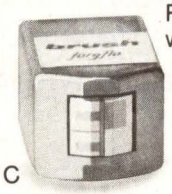


A



B



C

A: (left) Write Head; (right) Read Head.
3 tracks, top-to-bottom: IATA, ABA, THRIFT

B: (left) Write Head; (right) Read Head.
2 tracks, either IATA and ABA, or ABA and THRIFT

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CIRCLE 65

Now that such a device is available, the user can

```
LINK *KI TO *CL
LINK *DO TO *CL
```

and the micro is established as host because the serial communications line has been linked to both the machine's keyboard and its video display—the machine's primary input and output devices.

Device I/O can be further conditioned with transformation functions, called filters. For example, an Extended Binary Coded Decimal Interchange Code (EBCDIC) to American Standard Code for Information Interchange (ASCII) translation filter is available. When applied to the serial port by a simple

```
FILTER *CL WITH XLATE USING EBCDIC
```

the micro can be tied to an IBM mainframe that only supports EBCDIC ports. By simply filtering the *KI device with the Dvorak simplified keyboard (DSK) translation filter, the keyboard is reorganized—with no hardware changes required—to the DSK format. Many filters are available to format print output, trap specific character codes, perform upper/lowercase conversions—the limits are boundless.

Sometimes it is useful to redirect output from one device to another. The route library command performs this function. Device I/O can be directed either to another device or to a disk file. From a high level language like BASIC, sequential I/O normally deals only with files; however, the operating system permits such things as

```
5 FO$=''*PR'': REM Specify the PRINTER
10 OPEN''O'',1,FO$: REM Open file unit 1 for
  output
20 PRINT#1,''This is an example'': REM Write
  to unit 1
30 CLOSE1: REM Close file unit 1
```

which direct the file output to the printer by passing a device specification to BASIC's file opening command. Statement 5 would normally have been something like [FO$="DISKFILE/TXT"] which specifies a file as the I/O device.

Conclusion

The flexibility with which operating system software can interface various peripheral devices to a microcomputer can help reduce the hardware costs of a microcomputer system. As software does not introduce a continuous component cost factor, the overall price of software intelligence can be significantly lower than the corresponding design and manufacturing cost of hardware intelligence. Moreover, operating systems like LDOS contain features that bring the power and performance of the mainframe down to the level of the microcomputer.

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Screen Brightness Control from Keyboard	STD	NO
XON/XOFF Flow Control, Split for Xmitter and Receiver	STD	NO

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CIRCLE 66

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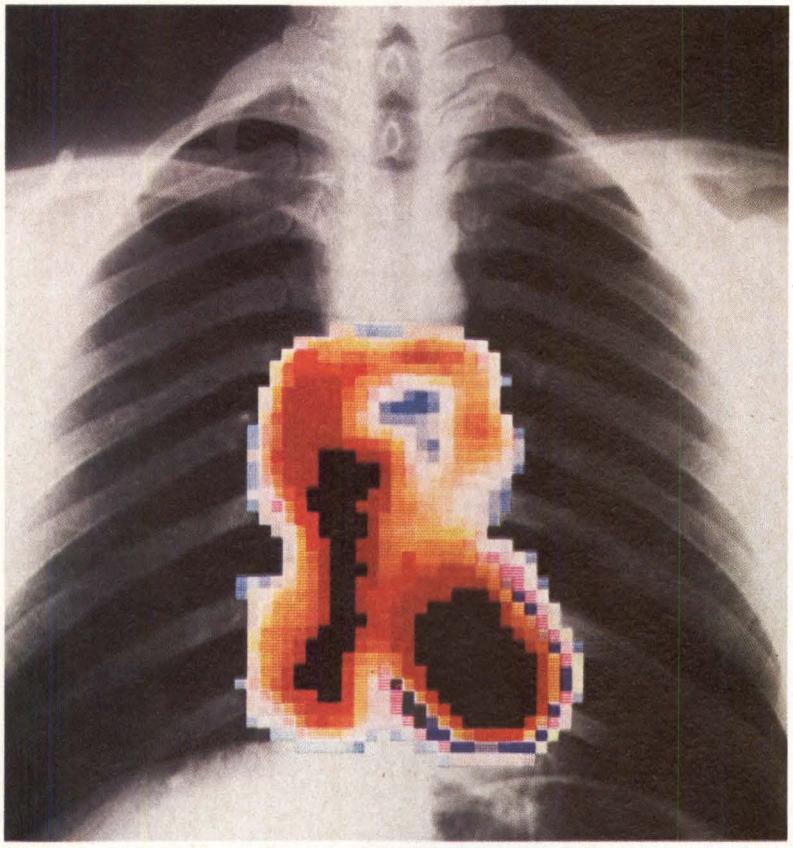

In nuclear medicine, doctors use Shugart's SA851 drive to store and playback images of the heart (shown here superimposed over x-ray). Photo courtesy of Technicare Corporation.

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CIRCLE 67

Cartridge Tape Drive Myth No.1:

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CIRCLE 68

INTERFACING INTELLIGENT PERIPHERALS

A single controller performs transfers offline and controls functions of interface, data integrity, and fault monitoring and diagnostics

by Doug Voigt and
Alan Brown

An intelligent peripheral combining online storage, backup, and configurable input/output capabilities can provide cost effective mass memory for minicomputer based systems. The unit discussed here includes defect handling, error logging, hardware diagnosis, and offline data transfers between disk and tape. Fewer components improve reliability and reduce space and power requirements.

The HP 7912 integrated storage product ties a 65M-byte disk drive and DC600 cartridge tape unit to a single controller (see Fig 1). An intelligent controller manages both disk and tape. Controller intelligence is applied in three areas: interface, data reliability, and fault monitoring and diagnosis. Thus, the host central processing unit (CPU) has little control over low level hardware operations. The controller is in charge of activities that require knowledge of the internal architecture of the storage devices, and their failure modes. This makes it easier for a CPU to control many peripherals with the same higher level protocol, in spite of differences in internal architecture. Operation of such a controller can be considered from two points of view; system software and methods of interfacing, and operation of the device itself.

System software

A breakdown of the system software involved in controlling a mass memory storage unit is shown in the Table. New peripherals do not effect the file system. Thus the driver must map standard read and write calls from the host into the protocol of the peripheral. Backup/restore and initialization utilities are more likely to be effected by a new device. The HP 7912 provides features which allow these utilities to be implemented more efficiently through use of specially designed diagnostic interface.

Ability to read or write an area of the disk or tape is provided by the driver. After the caller specifies a device address, the address of the data on the device, and a buffer in memory to be read or written, the HP 7912 command set allows the driver to execute these operations by exchanging only three messages over the interface.

A starting address on the device, an opcode indicating which operation is to be performed, and the length of

Doug Voigt is project leader at Hewlett-Packard Co, 11413 Chinden Blvd, Boise, ID 83707, working on the design and implementation of mass memory communication protocol. Mr Voigt holds an ASE from Northhampton County Area Community College, Bethleham, Penn, and a BSEE from Cornell University.

Alan Brown, a development lab engineer at Hewlett-Packard, is also working on mass memory communication protocol. Previously he was a computer programmer for the U.S. Army. Mr Brown holds a BS in electrical engineering from the University of Idaho, Moscow.

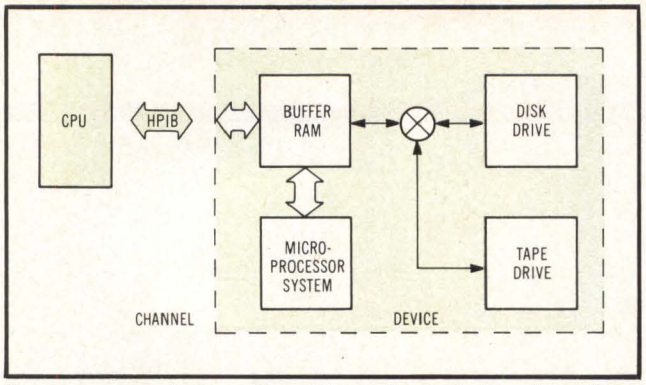

Fig 1 HP 7912 configuration. Controller is designed to allow CPU to establish data paths through buffer RAM, or to or from disk, tape, or microprocessor. Microprocessor can also cause internal reads or writes on either disk or tape.

the data to be read or written, is contained on the first message. When the device is ready for the second message that contains the data, it interrupts the CPU. Status of the operation prior to the data message is not checked by the host but, if an error has occurred, the device will either throw away the data, or generate a null message, depending on the direction of transfer. This expedites normal performance at the expense of performance during error recovery. When the device is finished with the operation, it interrupts the CPU again and sends a third message indicating success or failure of the operation. This sequence of messages constitutes a transaction.

Operation of the HP 7912 is message-based, with the transaction constituting the basic unit of work. This transaction also forms a model for the communication between a requester process requiring a service, and a server process that can provide it. Formalization allows all of the devices in the system to be incorporated into an interprocess communication network.

In error situations the read or write transaction is followed by a status transaction that gives detailed information about the failure. The host does not need to log hardware faults or data errors since the device automatically saves this information on the media.

In addition to read and write, the device driver provides an execute entry, which will execute the command, and get status if it fails. A device address, a transaction template, a command buffer, a data buffer, and a status buffer are each passed by the caller. Only the transaction template determines whether or not there is a data message, and specifies its direction. Utilities that know how to control the device use the driver function to execute transactions other than reads and writes, which gives utilities the power to invoke nonstandard device capabilities.

Normal read or write requests can be serviced by the driver with a minimum of channel communication. Since the interface driver handles channel hardware, transmitting or receiving messages over specific channels, the device driver can simply translate read or write commands into sequences of messages understood by the device. The command set of the device is designed to allow channel specific software to be isolated from device specific software. When this is done, any device that uses a common interface can use the same interface driver. Similar devices using different interfaces may be able to use the same device driver.

Mass Memory System Software Modules

Subsystem Utility	Invoked by	Function	Impact of New Peripheral
File system	User application	Provides standard access to named files	none
Device driver	File system backup/restore initialize operating system diagnostic interface	Provides standard peripheral interface for other modules	Drivers are typically impacted by new devices
Interface driver	Device driver	Controls channel hardware to send or receive messages	Impacted by new channels, but not new devices on old channels
Backup/ restore	User	Transports files between online and offline	Disk/tape copy command greatly impacts module
Initialize	Operator	Initializes file system on new media, maintains data reliability of old media	HP 7912 provides features that simplify implementation
Diagnostic interface	Operator/ service	Allows HP 7912 commands to be generated from a terminal	Designed for use with HP 7912

Utility design considerations

The tape unit used in the HP 7912 is a block structured streaming device incapable of stopping or starting the tape within the gap between data blocks. When the tape stops, it must back up and take a running start at the next block of data. Therefore, it is desirable to keep the tape moving between sequential blocks to keep performance up and device wear down. This is a primary consideration in the use of the drive, and enters into the design of the driver, backup/restore, and initialize software utilities. Maximization of streaming mode operation on the tape is a motivating force behind many of the features incorporated in the HP 7912.

Backup/restore utility and uses of the disk/tape copy feature

A backup operation is usually done by collecting files from various areas of the disk and writing them sequentially on the tape. The backup/restore utility can make read and write requests of the driver to transfer data from device to device through the host CPU's memory. However, with disk and tape units integrated into one device, this practice would stop the tape between driver requests unless concurrent transactions are supported in the device, and at the driver level. Even with concurrency of disk and tape operations, interface contention and software overheads could keep the tape from streaming. The best way to guarantee tape streaming is to allow the device to perform data copy operations directly between disk and tape.

Internal copies do not suffice if the disk and tape are not integrated into one device. However, if the two

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devices are on the same multidrop channel, such as the Hewlett-Packard interface bus (HPIB), it is possible to transfer data from one to the other without passing it through the CPU's memory. Using their combined internal buffering, two HP 7912s can achieve tape streaming in this manner. In instances where devices are on different channels, data must be buffered inside the CPU's memory. The HP 7912 is directed at small configurations that would probably support one or two storage devices on a single channel.

The data copy function is currently used in two schemes to improve performance and reduce wear during tape access. Disk buffering of data going to or from the tape can be performed in driver calls that read or write the tape. Direct disk/tape transfers can be used by utilities that invoke the execute function of the driver.

The command set allows the driver to execute operations by exchanging only three messages over the interface.

It is better to buffer data on the disk when writing to the tape in systems requiring existing backup/restore utilities to be used with new devices. These utilities use standard read or write calls to the driver which places data destined for the tape in a buffer on the disk. When that buffer is full, the copy command is used to stream the data to the tape. This allows tape performance to be improved without affecting system software other than the driver. Partial buffers must be posted when the CPU tries to read or write nonsequentially, or when the tape is unloaded.

Since the buffering scheme resides in the driver, it applies to any utility that uses the driver to read or write the tape. This improves reliability and performance on tape accesses from the file system, so user applications can take advantage of tape streaming as well. Because the tape is stopped between buffers, the size of the block being buffered determines the amount of improvement. For most system environments 64k bytes have been found to be an acceptable amount. Use of the copy command is compatible with existing system utilities, but is limited in the amount of streaming mode operation it provides. Buffering is useful only if typical data transfers to the tape are much smaller in size than the buffer.

If possible, the backup utility should specify data copy operations. One area of the disk to be backed up is copied to the next sequential address on the tape for each transaction. If the CPU can provide the next copy command soon enough, the tape can stream right on through. This is especially valuable on a small system with a low bandwidth input/output (I/O) channel, since data does not flow over the channel during a copy.

System activity is also affected by a copy command. Since the disk and tape are both busy during the operation, data on the disk are not accessible to the CPU. If the system needs access to the disk it must suspend backup activities, thus stopping the tape. Other architectures do allow disk access during backup but, if tape streaming is a consideration, the timing of disk accesses is critical. Extra system activity can easily cause tape motion to stop.

The initialize utility

The initialize utility locates any defects in the disk that cause data errors, and tells the controller to avoid those areas. It also sets up file system structures such as the directory, free space management tables, system logs, etc. Initialize is used when a new device is installed, or to clean up problems with a disk or tape currently in use.

There are two ways to obtain data error information from the device. While the disk is in use, it keeps an internal runtime error log that can be read and analyzed by system software. This allows the CPU to see what areas of the media are causing trouble during normal operation. Once a defect is identified, a spare command causes the device to avoid that section of media. Data stored there will be mapped by the device to a new physical location. Use of the runtime error log for sparing defects does not destroy data other than that directly over the defect, and it uses the user's data to locate pattern-sensitive defects.

During normal operation, the disk tolerates minor defects by using an error correction code and data retries. Error correction on the disk can detect and correct 12-bit errors without degrading performance. The retry feature rereads data once per revolution of the disk for a duration specified by the CPU. Errors that are recovered by retry are put in the error log to allow the CPU to spare marginal blocks of data.

A second means of finding defects is a write-then-read, error rate utility. The CPU commands the device to execute an error rate test on a certain area of the disk. A data pattern, which can be random, worst-case, or specified by the user, is written by the device and then read back internally. Errors are logged in so the CPU can use the log to spare any defective blocks. Error rate test use destroys user data, so any information to be saved must be backed up first. If the disk has never been used by the system, the error rate test will be more valuable. When a new disk is installed, a typical initialize utility will use the device's initialize command to cause its internal format to be reset, run an error rate test, spare any defects, and generate system data structures.

A describe command that returns information about the size and configuration of the device, and other operating characteristics is provided by the HP 7912. The CPU can use this information to set up free space allocation, and any special control needed by the driver. This command replaces a single word identification (ID) code used by system software on older devices to index into a table of attributes. Describe allows new products to be integrated into the system without having to update software unless differences in the new device are not parametric.

The HP 7912 allows the system to specify disk addresses with a single block number, as well as the traditional 3-vector format. This makes space management easier for the host, and allows each device to organize its addressing space for optimal performance during sequential access.

Tape defect handling

Defect handling on the tape is a different problem, since tape cartridges are prone to wear and are changed often. Since the tape drive does not have read after write capability, data errors are not visible until the defective block is read. New tapes need to be made free of

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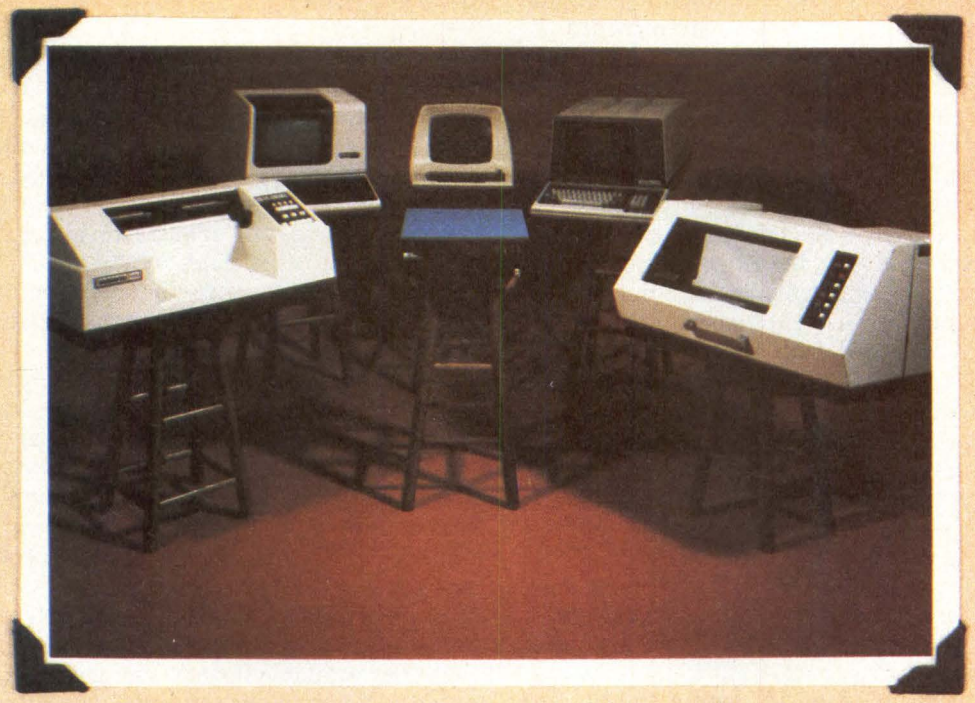

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defects, and old tapes must be cleaned and recycled. In addition to the sparing and error rate tests, tape certification and automatic sparing features are provided.

Since the block structured tape is a pseudorandom device, reorganization of data around a defect in such a way that it can be accessed randomly by block number, even though the media is best suited to sequential access, is a consideration. Thus, it is necessary to rearrange the logical addresses of blocks on the tape so that the defect is skipped over, while retaining the sequential order of the data blocks. On the HP 7912 this is called skip sparing. It optimizes sequential access, but loses all data after the defect because the logical addresses of data blocks have changed.

When accessed randomly, the system may have data stored all over the tape, and may not be willing to lose it when a spare operation is performed. In this case a spare command causes a reserved block that is not accessible to the CPU to be substituted for the bad block. This is called replacement sparing. Sequential accesses that encounter the spared block must seek to the location designated for that spare, access one block, then seek back to the block after the defect. This takes extra time on a tape device, but no data other than the defective block are lost.

The HP 7912 allows the CPU to choose the type of sparing to be performed, dependent upon how the file system accesses the tape (sequential or random), and the system's tolerance for performance degradation when a defect is found. If the CPU uses replacement sparing to preserve data, the initialize command should be used to convert to skip spares when the tape is recycled.

To assist the CPU in generating defect free tapes, the initialize command will invoke a tape certification procedure on new tapes. Certification is an error rate test that spares any defects it finds—it writes the entire tape with a worst-case pattern, reads it back under reduced margins, and uses skip sparing to eliminate defects from the host's addressing space. This reduces the probability of encountering tape errors during restore operations.

Automatic sparing can be enabled to get rid of defects that appear during realtime operations. The device keeps a log of errors encountered while reading the tape. Whenever a block with a history of errors is written, the device goes back and reads it to be sure it can be recovered. If it cannot, the block is immediately spared. Errors are noted during read, copy, verify, and error rate testing operations, and spares are generated during writes and copies.

Diagnostic interface

The diagnostic interface utility is provided to allow an operator or service engineer to invoke the HP 7912's internal diagnostics and utilities by building commands to be sent to the device from a terminal. Some operations are also performed automatically whenever the device powers-up, and some, such as error rate testing, are invoked at other times by the CPU. The diagnostic interface is used to verify the operation of a new drive when it is first installed on a system, and to stimulate the drive when looking for problems.

Twenty hardware tests built into the device are combined into 13 diagnostics that range from exercising critical components to full functional testing. Any failures return the number of the section of the test that failed, and the number of the subassembly most likely to be at fault. This information is also visible on a light emitting diode (LED) display, located on the microprocessor board in the device. Field service engineers use this information either locally or remotely to determine the nature of a failure.

Utilities available include various types of error rate testing and commands that provide access to data error logs, hardware fault logs, and spare tables. These utilities are used to obtain information on the realtime operation of the drive that may not be detected by hardware diagnosis. The fault log is especially valuable in diagnosing intermittent errors that occur during normal operation.

These same diagnostics and utilities are used extensively on the HP 7912 production line for final test and burn-in, and for diagnosing problems with hardware while it is being debugged or reworked. Hewlett-Packard has found that these capabilities have greatly reduced the amount of test equipment, time, and floor space required in manufacturing the HP 7912.

Implementation

Major components of the HP 7912 peripheral controller are the microprocessor system, the data memory access (DMA), and the drive interfaces shown in Fig 2. Other modules include the read/write electronics, the actuator controller, the disk spindle motor control, and the power supply. The overall purpose of the controller is to interpret commands from the host, to oversee or

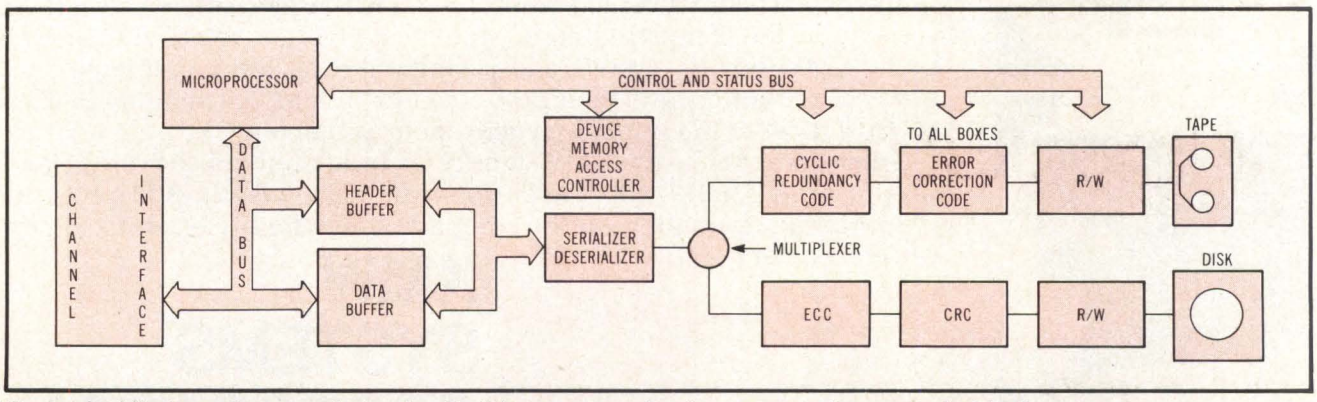

Fig 2 Architecture of HP 7912 electronics. In this arrangement, microprocessor has control of both data flow between host and subsystem, and over control and status of peripheral devices, but its control is excercised over separate buses.

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perform the required tasks that carry out those commands, and to keep account of how well the drive is doing its job.

Actuator electronics for each unit control all head movement while the spindle electronics control media motion. The microprocessor interprets commands from the CPU and directs the drive and controller electronics. During operation, it monitors the hardware for error and fault conditions, tries to correct those it can, and generates a status message to report results to the host. Other responsibilities include performing diagnostic tests of the entire drive, and maintaining drive information tables and logs of errors and faults.

The primary concern is...to always have data or buffer space ready for the tape when it reaches a new block.

DMA electronics provide a dual port buffer for the transfer of data between the channel and devices, or between devices. During transfers over the channel, it manages the data flow in either direction following the rule of first in, first out, servicing the channel and drive ports simultaneously. When transferring data from one drive to the other, the buffer is alternately switched between units.

Drive interface circuits provide translation of signals between the DMA and the read/write circuits, and the error correction code and cyclic redundancy code circuits. Error correction circuits repair most mistakes in recovering data from the media through the use of additional information within each sector and the appropriate error correction code (ECC) algorithm. The cyclic redundancy circuit (CRC) provides a test of the corrected data to ensure that the read is valid. Included in the tape interface are a 1-block buffer and all the necessary control logic to write the block on the tape so that parallel disk and tape transfers can occur.

Data transfer control

When the CPU sends a read command, the channel interface and DMA circuits route it into the buffer where the microprocessor interprets it. Servo electronics are directed by the microprocessor to seek to the track that holds the first sector to be transferred. The header of the next sector is read to determine the current location on the track. A data message is requested of the CPU via the channel interface. DMA is set up to transfer from the drive to the channel for the byte count set by the CPU. Just before the first desired sector to be read passes under the head, the processor enables the DMA to accept data from the drive. While the sector is being read it is determined whether the next physical sector is also the next logical sector, which will not be the case if sector interleaving is used. After each block is read, the processor checks for any hard errors before telling the DMA to transfer that block to the CPU. When the entire transfer is completed, a status byte is generated and sent to the CPU.

A write operation is very much the same. The DMA is set to move data in the opposite direction, and the timing is altered to get data from the CPU in time to reach the sectors on which it will be written. The CRC and ECC circuits are used to generate their codes which are then recorded on the disk after the data. In either case, once the channel is started it is allowed to send or accept bytes at whatever rate the CPU handshakes them until the buffer is empty or full, depending on the direction of transfer. If the CPU cannot handle the average transfer rate of the drive, latencies are automatically induced to allow it to catch up.

Reads and writes to the tape drive differ in that, instead of the heads, the media must be positioned before accepting data, and the sectors are 1024 bytes in length. An extra block of buffering is available on the tape interface but, should the DMA become full during a read, or empty during a write, the tape is stopped until enough data are transferred for the next block. The tape must then be repositioned before continuing. The data block that resides in the tape interface buffer (TIB) is automatically written or read by a state machine. Since this requires no interaction with either the data buffer or the microprocessor, the controller has about 25 ms of idle time during each tape operation.

A primary concern when moving data between devices is to always have data, or buffer space, ready for the tape when it reaches each new block. The problem is compounded when disk interleave is used, as it takes more than one rotation and an incremental seek to acquire the four disk sectors needed to write the next tape block. To ease the data copy function, which can adapt to any combination of starting addresses, disk sector interleave, and speed tolerances, the 4k-byte buffer is divided into two 2k-byte buffers that are alternately filled from one unit and emptied to the other.

To copy the disk to the tape, the HP 7912 first seeks to the starting location for each drive, then computes the physical location for the first eight sectors and reads them into the buffer in the order they pass under the head. To initiate the tape write operation, the first tape block is located and the first four sectors are sent to the TIB in their proper order. Since the tape interface can handle tape operations from this point without processor intervention, the second buffer can be filled with the next eight sectors in the physical order as before, with time to spare before the tape write operation is finished.

The controller keeps alternating between buffers, filling each with new disk data as soon as it is emptied into the TIB. This process continues to the end of a cylinder. First of the two blocks in the alternate buffer is used while the disk seeks to the next track, and the second is used if additional sectors are needed to pad out the buffer being filled at the end of the cylinder. This method has proven adequate to keep the tape streaming, unless retries or long seeks to spares are required on either device.

Drive maintainence

Both the tape and disk drives have media areas that are not available to the CPU for the direct storage of data. These include preallocated tracks, sectors, and blocks for sparing, as well as maintenance tracks and blocks set aside for the exclusive use of the controller.

The disk maintenance tracks hold the error and fault logs, the error rate test log, and the remapping table for spared tracks. Media errors and hardware faults that occur during normal realtime data transactions are kept

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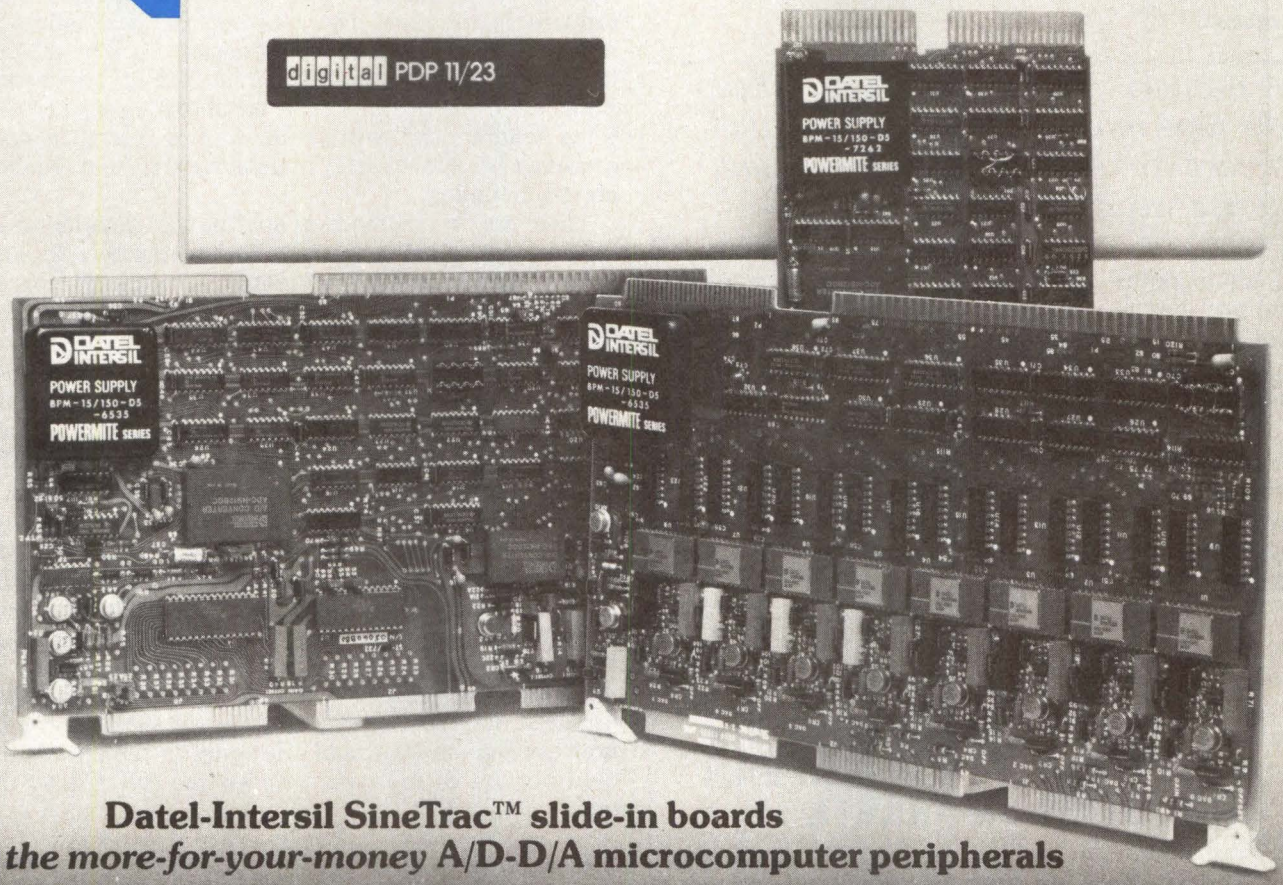

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in a table in the microprocessor's random access memory (RAM). When all of the available RAM for these tables is used up, the HP 7912 asks the CPU to release it. This allows it to take time for maintenance, posting the table to the appropriate maintenance track so that it may purge the RAM table for future logging. If the CPU grants the release or fails to respond within two seconds, the controller then posts the table. The error rate test log is used to record any media errors that occur when the corresponding test is run. This maintenance track is written as part of the diagnostic so no release is required.

A primary consideration is...to keep the tape moving between sequential blocks to keep performance up and device wear down.

Although the CPU cannot write to these logs, utilities are provided to read and transfer their contents to the CPU. This is used to determine which sectors should be spared, and to aid the service engineer in diagnosing intermittent faults in drives.

One sector on every disk track is set aside as a spare to be used as a replacement if one of the 64 normal data blocks proves to be defective. If a second sector on a track fails, the entire track is replaced by one of the spare tracks, and then logged in the spare track maintenance block.

The tape has blocks preallocated for the error and error rate test logs, the nondestructive media test area, the tape spare table, and the use log. The error log, error rate test log, and media test area are similar to the disk. The use log holds counters of how many block accesses have been made and how many times the tape has been loaded. This information is used to determine whether a high error rate on the tape is due to faulty hardware, media, or just excessive use.

One out of every 512-tape data blocks is set aside for sparing in a pattern that distributes them evenly throughout the tape. The addresses of these blocks is written to the spare table maintenance block by the initialization routine invoked by a format command. Because the blocks in this table are automatically skipped when reading and writing data, their presence only causes an occasional delay in data transfers and requires no CPU handling.

There are two methods of sparing bad data blocks—replacement and skip sparing. Both methods replace an unused address in the sparing table with the address of the bad block so that the bad block will be skipped and the spare released for use. Methods differ in the replacement mode. The closest available spare is linked directly to the bad block so that references to the old address are remapped to the spare, whereas skip mode simply causes the bad block to be skipped in place of the following spare block. The replacement mode causes a delay whenever the old block is to be accessed because the drive must seek to the spare block. However, it can be used in the middle of a file without affecting the addresses of data beyond it. The skip mode keeps performance up at the expense of scrapping the data that follows the bad block since the logical addresses of those blocks are altered by the operation. Even with that problem, skip sparing can be used for the majority of tape applications that add files only to the end of the used portion of the tape, or copy the full disk to the tape.

Diagnostics

HP 7912 has a full set of internal diagnostic routines that are invoked whenever the device is powered-on, a selftest pushbutton located behind a panel is activated, or the CPU sends a run diagnostics command. A set of routines, called microdiagnostics, that test isolated parts of the peripheral and a monitor that controls the flow from test to test comprise the diagnostic system. Microdiagnostics are called by the monitor in an order that tests paths from the microprocessor out, and from the most basic function to the most complex. It would check media rotation to be at least the minimum acceptable speed before moving the heads on it. Failure of any test results in the logging of a test error code that is used by the monitor to determine which boards have failed and to report bad board numbers to the operator through a display by the selftest switch, and to the CPU via status messages.

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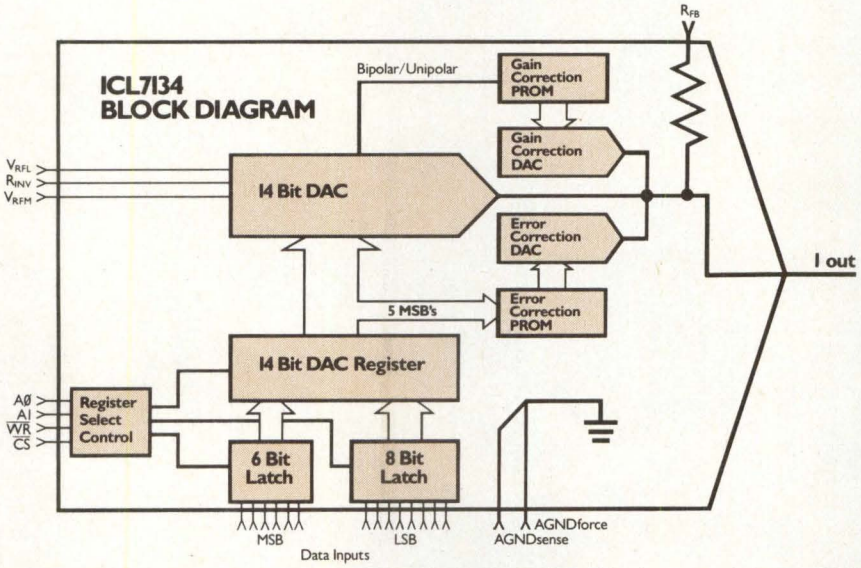

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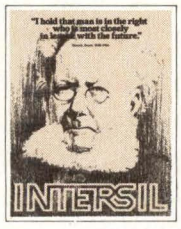

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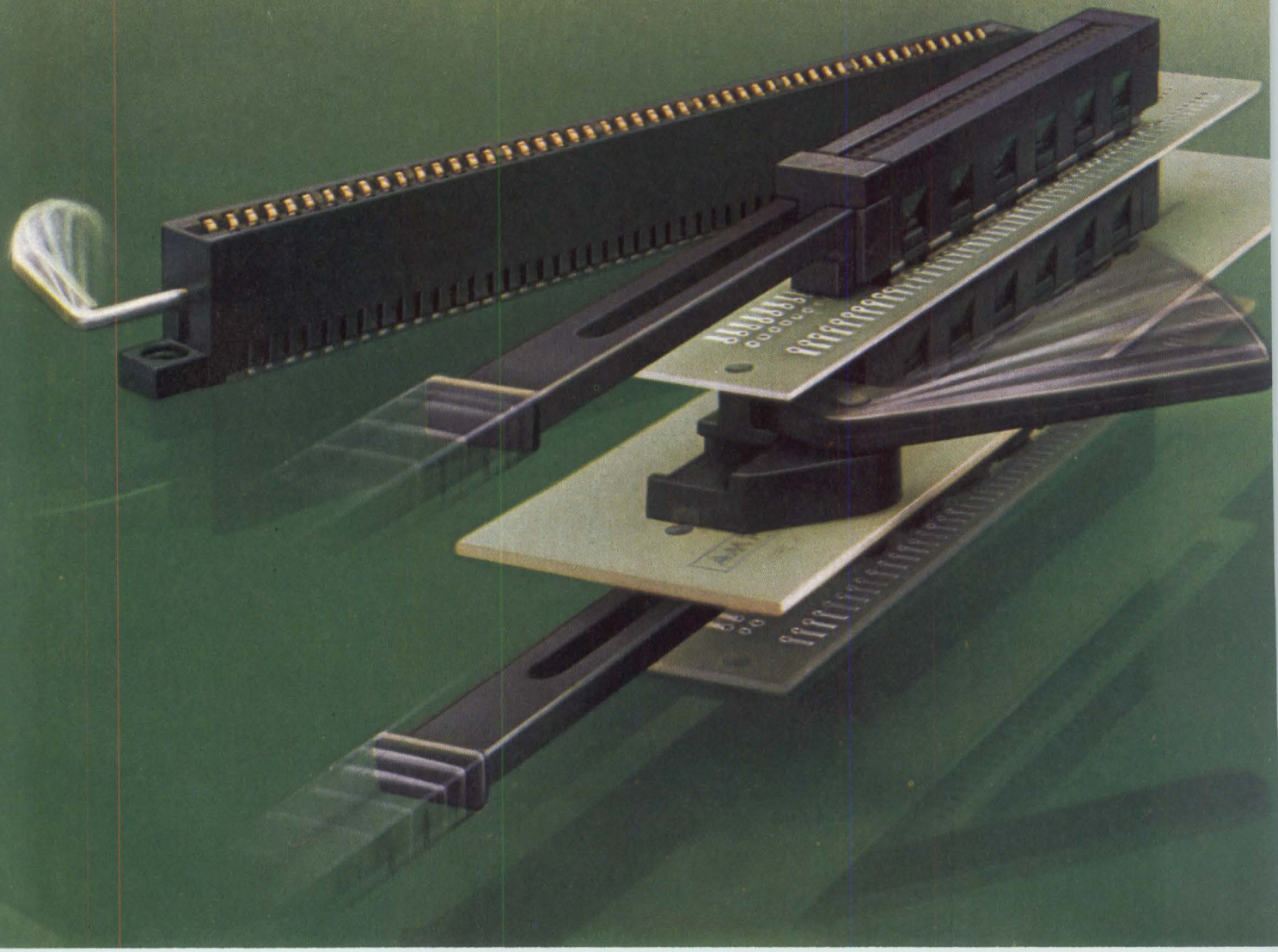

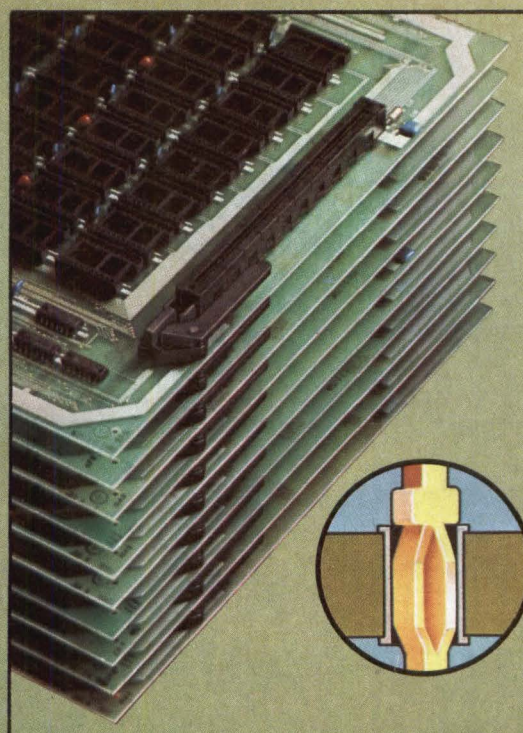

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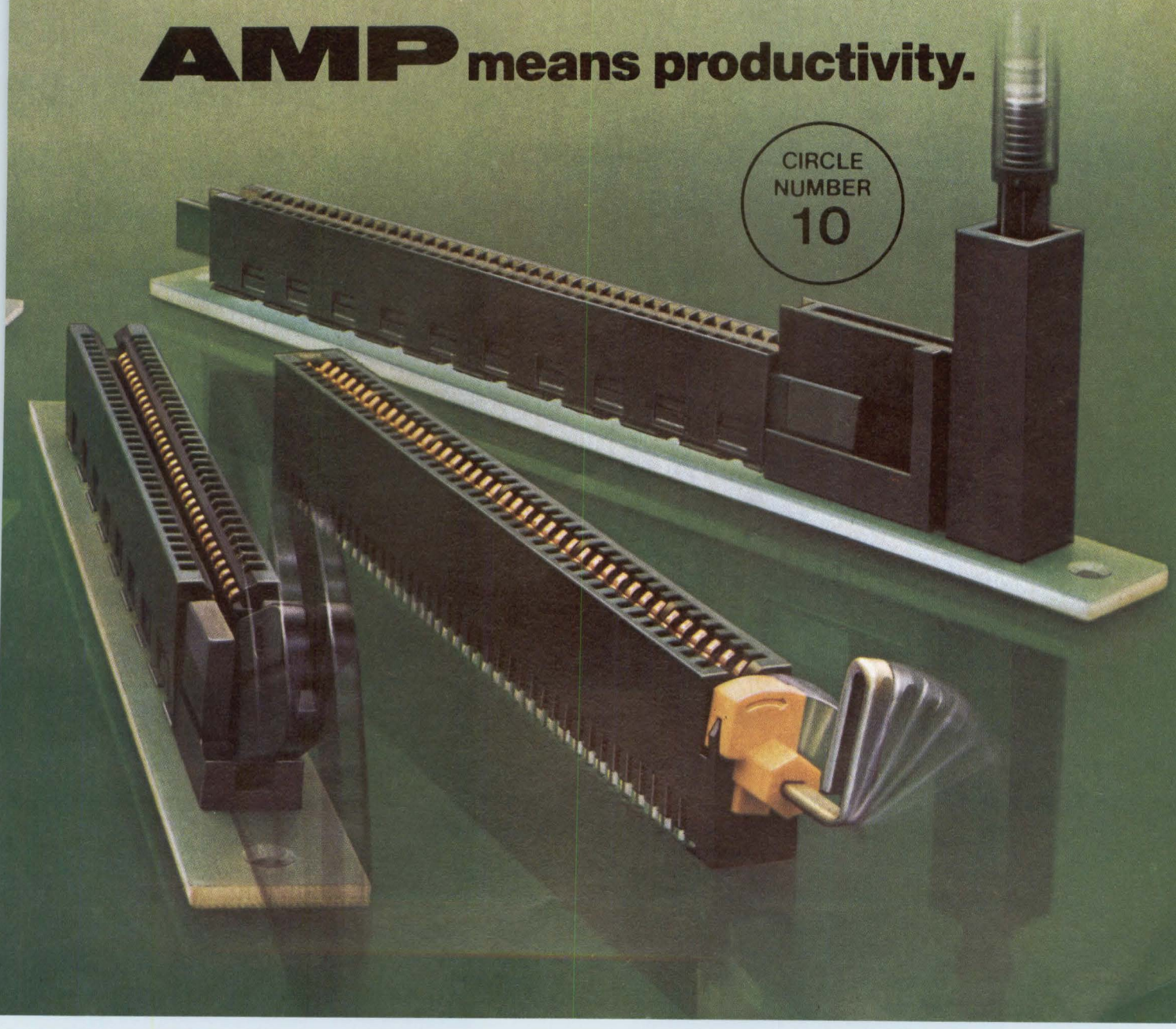

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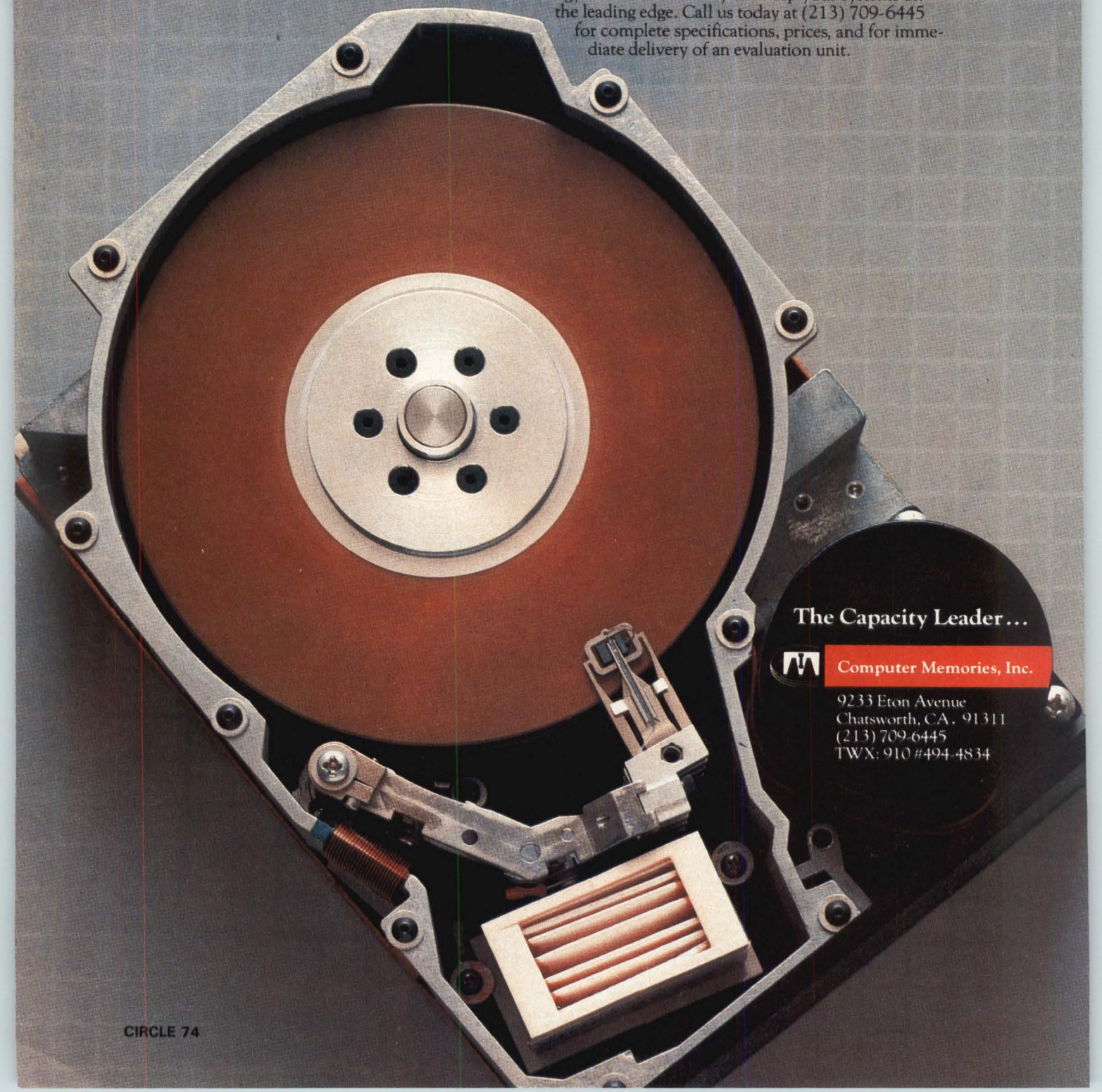

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CIRCLE 74

DEBUGGING WITH FILTERED TRACES

When filtered by the condition of certain processor registers, interrupt-driven tracing is a powerful debugging tool

by M. F. Smith

An interrupt-driven filtered trace technique combining hardware and software can greatly simplify debugging during microprocessor program development. The technique allows instructions to be traced or single-stepped when a combination of conditions is present (filtering). Ability to trace software conditionally is an extremely powerful tool for debugging microprocessors. The trace technique can also be used during normal program execution to detect abnormal hardware/software conditions.

Breakpoints and tracing

Use of breakpoints is a well established debugging technique. Breakpoints usually are initiated by restart or software interrupt instructions and can either be inserted directly into the source or object program, or inserted and deleted by the debug monitor. The normal outcome of a breakpoint is the printing of register contents and a halt program instruction.

Breakpoints are easily used and require no hardware. However, they do have limitations. For the programmer, the basic limitation of the breakpoint technique is the inability to see the effects of program execution dynamically. Since it is usually the case that program errors are

M. F. Smith received a BS in geology from the University College, Wales, U.K.; an MA in geology (micropalaeontology) from California State University; and a PhD in oceanography (instrumentation) from University College, Galway, Ireland. He has been working with microprocessors since 1975 and is the author of a number of articles on that subject. Currently, he is Lecturer in Microprocessors in the Department of Computer Science, University of Reading.

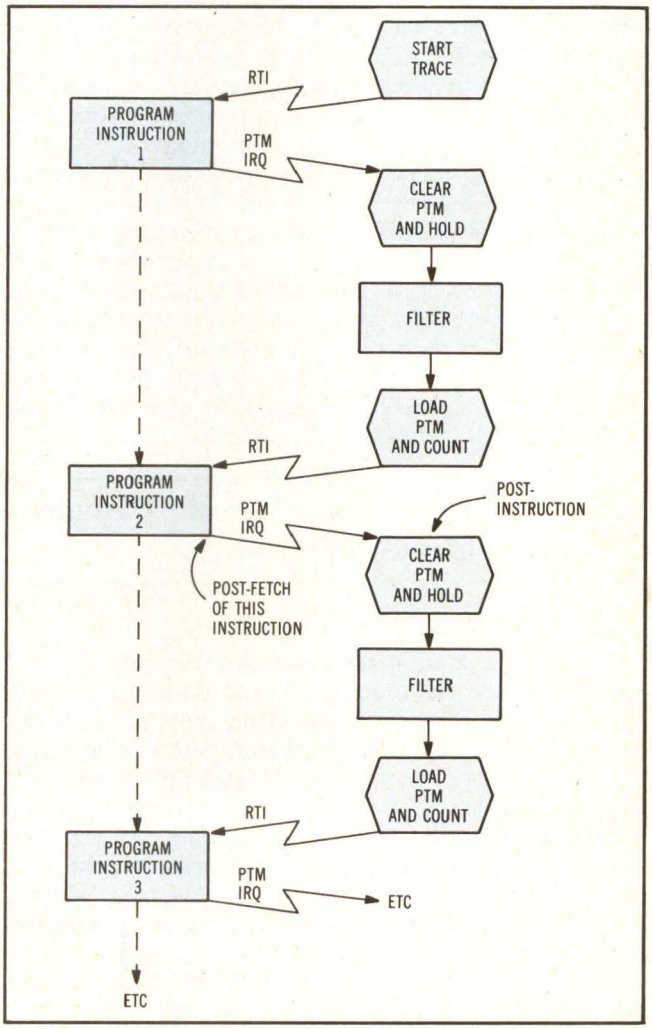

Fig 1 Action of interrupt-driven trace. Counter interrupts one clock cycle after end of every return from interrupt instruction (RTI) and just after fetch of next program instruction.

```
PROGRAM Trace_Start;

CONST
    channel_1 = 0                   {point to MC6840 PTM output}    ;
    channel_0 = 1                   {channels 0 and 1}              ;
    irq_mode  = 226                 {set PTM to interrupt}          ;
    non_irq_mode = 130              {set PTM not to interrupt}      ;

VAR
    ptm_control_0, ptm_control_1, ptm_data; INTEGER {PTM adrs}      ;
    delay_trace : INTEGER    {no. of cycles before trace starts }   ;


PROCEDURE    Trace_On               {Start the Trace}               ;
  BEGIN          {initialize the MC6840 PTM}
    ptm_control_1:=channel_0        {point to channel 0}            ;
    ptm_control_0:=irq_mode         {setup for IRQ mode}            ;
    ptm_control_1:=channel_1        {point to channel 1}            ;
    ptm_control_0:=non_irq_mode     {setup for non-IRQ mode}        ;
    ptm_control_1:=non_irq_mode     {setup channel 2, non-IRQ}      ;

    ptm_data:=delay_trace           {delay before trace starts}
  END;                              {then PTM channel 2 interrupts}



PROCEDURE    Trace_Off              {Stop the Trace}                ;
  BEGIN
    ptm_control_1:=channel_0        {point to channel 0}            ;
    ptm_control_0:=non_irq_mode     {disable IRQ}                   ;
  END;
```

Fig 2 Pascal program showing initialization of programmable counter (PTM) and starting and stopping interrupt-driven trace. In this example PTM is MC6840, but any other type should be suitable.

caused by completely unexpected events, these events can be discovered only by examining every step of the program. Another limitation of breakpoints is that debugging can be subtle if the registers are displayed only when a set of given conditions exist, since the conditions would not be tested for every instruction.

Fault tracing can be used with breakpoints by inserting a breakpoint between every instruction. Breakpoint tracing is most effective if done by the monitor during the trace operation, but programs can only be traced through random access memory (RAM). However, programs can be easily corrupted. When the monitor is inserting the breakpoints automatically, the program must be disassembled to find the beginning of the next instruction. This can be complicated, even with simple variable-length instruction processors.

Breakpoints are easily used...they do have limitations, however.

Enter the interrupt

Interrupts provide instruction tracing without the use of breakpoints or elaborate hardware. In addition, programs may be traced through either RAM or read only memory (ROM). Tracing will operate with either normal interrupts (IRQ) or non-maskable interrupts (NMI). IRQs have the advantage of allowing the trace to be disabled by the program being debugged, without disabling the counter. NMIs are more reliable, in that they cannot be disabled, but the trace cannot be disabled without stopping the counter. They also make tracing interrupt routines easier, since it is not necessary to unmask interrupts explicitly. Unfortunately without filtering, an NMI-driven trace may be able to trace itself.

With interrupts, a hardware counter is used to tally processor clock cycles after a return from interrupt (RTI) instruction. The counter interrupts the processor one cycle after the RTI, so that the next interrupt occurs after the next program instruction is fetched (Fig 1). At the beginning of each interrupt, the counter is cleared and disabled to prevent further interrupts during the trace routine. If tracing is to continue, the counter is loaded with the delay information at the end of the trace routine, and enabled just before the RTI instruction.

The counter used for trace interrupts can be a discrete hardware loadable down counter such as the 74163, controlled by a simple parallel interface. The parallel interface is required to clear and enable the counter. A microprocessor interfaced, programmable timer/counter (PTM) is more versatile than the simple counter. The PTM is simpler, less expensive, and does not require a parallel interface. It also allows the trace to be held off

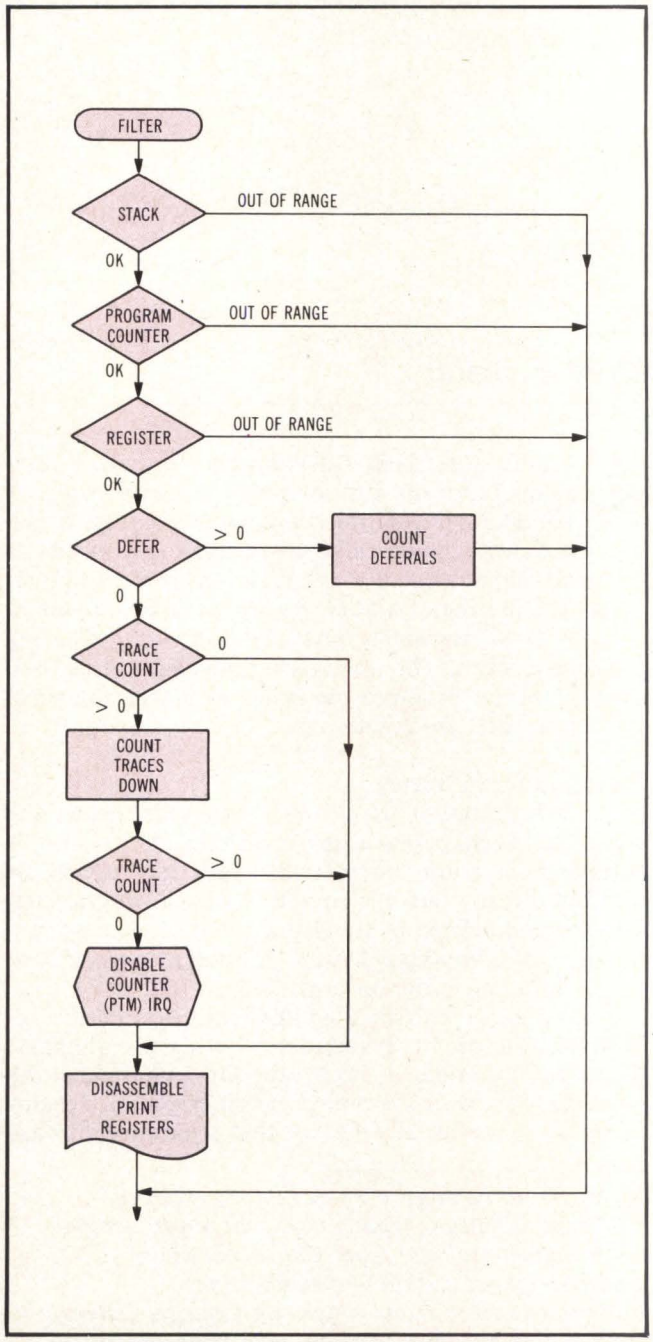

Fig 3 Flow diagram of filtering routine for interrupt-driven trace routine. Filter checks range of various parameters and only allows tracing when all conditions are satisfied. Addition of filtering to trace creates powerful and versatile enhancement to debugging.

```
PROGRAM  Trace;

CONST
    hold_off_trace = 12      {hold off time before next interrupt}
                             {processor (MC6809) dependent}
          cc =  0                {registers as stacked}          ;
           a =  1                {after an interrupt}            ;
           b =  2                {offset from 's' stack}         ;
          dp =  3                {pointer - this is a}           ;
           x =  4                {processor-dependent}           ;
           y =  6                {feature.  This example}        ;
           u =  8                {is specific to the}            ;
          pc = 10                {MC6809 microprocessor}         ;

VAR
    stack_bytes:ARRAY  cc..dp  OF BYTE  {byte registers on stack} ;
    stack_integers:ARRAY  x..pc  OF INTEGER {int reg on stack}  ;

    when_flag       : BOOLEAN     {register to test with range}   ;
    step_flag       : BOOLEAN     {trace will single step}        ;
    range_flag      : BOOLEAN     {address range will be tested}  ;
    stack_flag      : BOOLEAN     {stack limits will be tested}   ;

    when            : cc..pc      {register to test range}        ;

    for_count       : INTEGER     {count traces before stopping
                                   trace}                         ;
    defer_count     : INTEGER     {count traces before starting
                                   trace}                         ;
    when_minimum    : INTEGER     {minimum and maximum}           ;
    when_maximum    : INTEGER     {register range}                ;

    range_minimum   : INTEGER     {minimum and maximum}           ;
    range_maximum   : INTEGER     {address range}                 ;

    stack_minimum   : INTEGER     {minimum and maximum}           ;
    stack_maximum   : INTEGER     {allowed stack address}         ;

    stack           : INTEGER     {contents of the stack}         ;
    hit_flag        : BOOLEAN     {local variable for tests}      ;
    junk            : INTEGER     {local variable}                ;

PROCEDURE Filter(VAR x:INTEGER;min:INTEGER;max:INTEGER);
{compare given value with limits; set hit flag if false}
    BEGIN
      IF (x < min)  OR (x > max) then hit_flag:=FALSE;
    END;


        ******************************************
        *  MAIN PROGRAM IS ENTERED VIA IRQ/NMI     *
        *  IT IS ASSUMED THAT NO OTHER DEVICE      *
        *  CAN CAUSE THIS INTERRUPT.  THE VARIABLE *
        *  'stack' CONTAINS THE VALUE OF THE STACK *
        *  POINTER (s); ALL OTHER REGISTERS HAVE   *
        *  BEEN PLACED ON THE STACK.               *
        ******************************************

BEGIN
    junk:=ptm_control_1    {rest the PTM IRQ flag}                ;
    hit_flag:=TRUE         {set the anding flag}                  ;

{Test stack range if condition is enabled}
    IF stack_flag AND hit_flag THEN
       BEGIN
            Filter(stack,stack_minimum,stack_maximum);
            IF NOT (hit_flag) THEN Stack_Error                    ;
       END;     {do the stack error routine but continue tracing}

{Test address range if condition is enabled}
    IF range_flag AND hit_flag THEN
       Filter(stack_integers pc ,range_minimum,range_maximum)     ;

{Test register range if integer register has been specified}
    IF when_flag AND hit_flag AND (when>dp)  THEN
       Filter(stack_integers when ,when_minimum,when_maximum)     ;

{Test register range if byte register has been specified}
    IF when_flag AND hit_flag AND (when<dp)  THEN
         IF     {compare byte registers on the byte stack}
              (stack_bytes when  < when_minimum)
            OR
             (stack_bytes when  > when_maximum)
        THEN  hit_flag:=FALSE                                     ;

{do not trace until defer count is zero}
    IF (defer_count>0) AND hit_flag THEN
                       BEGIN
                            defer_count:=defer_count-1            ;
                            hit_flag:=FALSE                       ;
                       END;

{TRACING is now ALLOWED if hit flag is true until traces are
counted down to zero, if specified.  Single step mode may be
implemented.}
    IF hit_flag AND (defer_count=0) THEN
                BEGIN
                    IF (for_count>0) THEN
                       BEGIN
                         {keep track of number of traces if for
                         enabled}
                         for_count:=for_count-1                   ;
                         {turn off PTM interrupt when count hits
                         zero}
                         IF (for_count=0) THEN Trace_Off          ;
                       END;
                    Disassemble_Instruction {show mnemonic}       ;
                    Print_Registers   {print out registers}       ;
                  IF step_flag THEN Wait {wait until key pressed};
                END;

{End of filtering - prime next trace interrupt}

    {enable interrupts here}
   ptm_data:=hold_off_trace {PRIME COUNTER FOR NEXT INTERRUPT}    ;
    {return from interrupt instruction}
END.
```

Fig 4 Pascal program of main part of trace and filtering routine. Interrupted instruction is disassembled and registers are displayed if given conditions are satisfied. Procedure trace-off is defined in Fig 2; procedures wait, print-registers and disassemble-instruction are defined externally. Program is for MC6809 but may be altered for other processors easily.

for a given number of clock cycles; this is not practical with hardware counters. An MC6840 PTM is used in the example, but any other type should be suitable.

In Fig 2, the PTM must be initialized before the trace can commence. The PTM channel used for tracing must be enabled for interrupt operation, and the IRQ output from the PTM must be connected to the appropriate processor interrupt input. The PTM is then loaded with a delay value (Fig 2, delay-tract) to prevent the trace from starting until the initializing routine is finished. The delay value may also be used to hold off tracing for a given number of clock cycles.

Filtered tracing

A trace that displays every instruction of the registers can be useful but is usually not selective enough for most situations. The addition of filtering turns tracing into a powerful tool that can greatly speed and simplify debugging. When filtering is used, every instruction is interrupted; but the registers and other information are displayed only when certain conditions are met. Filters useful for debugging include the testing of accumulators, index registers, stack pointers and program counter in nonprogram memory (Fig 3). Other possibilities are testing of particular memory locations for contents or tracing for a given instruction (eg, only subroutine calls).

An example of a filtered tracing routine is presented (Figs 3 and 4). When all conditions are satisfied, the registers are displayed and the current instruction is disassembled. The tracing routine is much simpler and more reliable if all registers, including stack pointer, are saved in memory or on the stack on entry. This not only preserves the status of the background program, but also provides the filtering data, when the filter parameters are stored as lists in memory before the trace is initiated.

The addition of filtering turns tracing into a powerful debugging tool.

Other features of the trace routine (Fig 4) include the ability to defer register display for a given number of valid traces, the stopping of the trace and, after a given

number of traces, single-stepping. The only limitation to a filter driven trace routine is the amount of memory allowed and the ingenuity of the programmer.

Summary

The filtered tracing described causes an interrupt after every instruction. Thus instruction tracing and single-stepping through programs under development is possible. In addition, filtering can be used to allow tracing to occur only when certain conditions exist. This is an extremely powerful technique for program debugging. Unlike pure software techniques using breakpoints, interrupt driven filtered tracing allows ROM, RAM, and interrupt routines to be examined.

When all conditions are satisfied, the registers are displayed and the current instruction is disassembled.

A benefit of the tracing technique is its adaptability. Tracing can be used to detect and trap out of range or abnormal conditions in critical program segments during normal program execution providing they are not time sensitive. Possible causes might be stack underflow, illegal memory addressing, hardware malfunctions, memory corruption or execution of illegal instruction codes.

Simple filtered tracing requires only a hardware counter and a modest amount of program and variable memory, and can be used with any processor that allows interrupts. More importantly, the technique is sufficiently inexpensive that it can be incorporated into production equipment to improve the reliability of the software.

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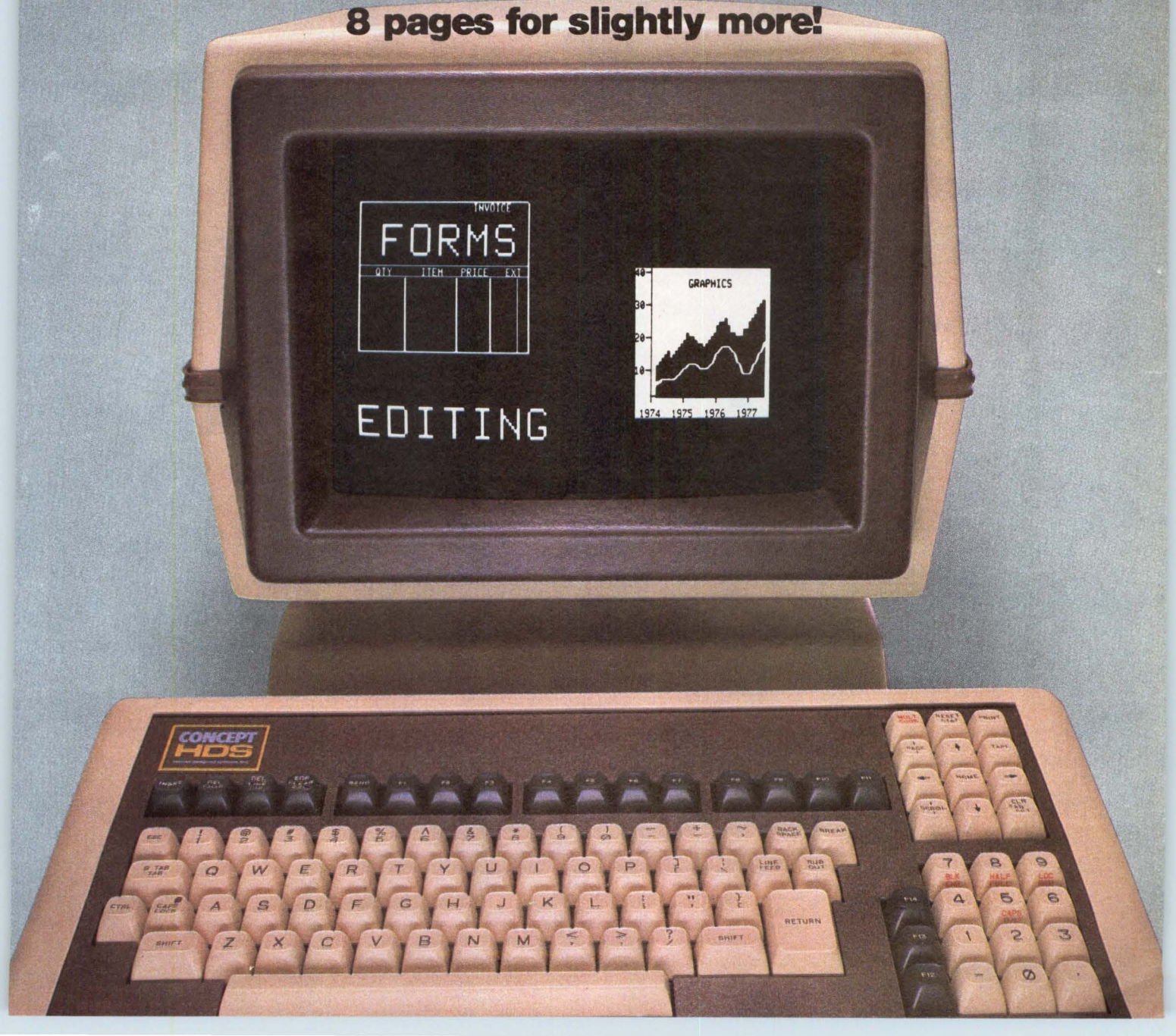

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CIRCLE 77

A CLUSTER COMMUNICATIONS I/O PROCESSOR

By offloading communication tasks to a specialized peripheral, more workstations can be accommodated without degrading data transfer rates

by Drew Hoffman and Henry Robinson

Computer efficiency can be increased with minimal modification to existing hardware and software by transferring routine processing tasks from the central processing unit to specialized peripherals. If the interface is governed by an industry standard, and the operating system is message based and modularly expandable, further efficiencies are possible (Fig 1).

Convergent Technologies had a requirement to expand a local area high speed communications cluster from a minicluster consisting of up to four multifunction workstations to a full cluster with up to 17 workstations. Each workstation was to have its own 16-bit processor, up to 1M byte of random access memory (RAM), a high resolution video monitor, a keyboard, and optional Winchester and/or floppy disk. In addition to running its own application, the master workstation was to provide disk, printer, and communications resources to the cluster workstations.

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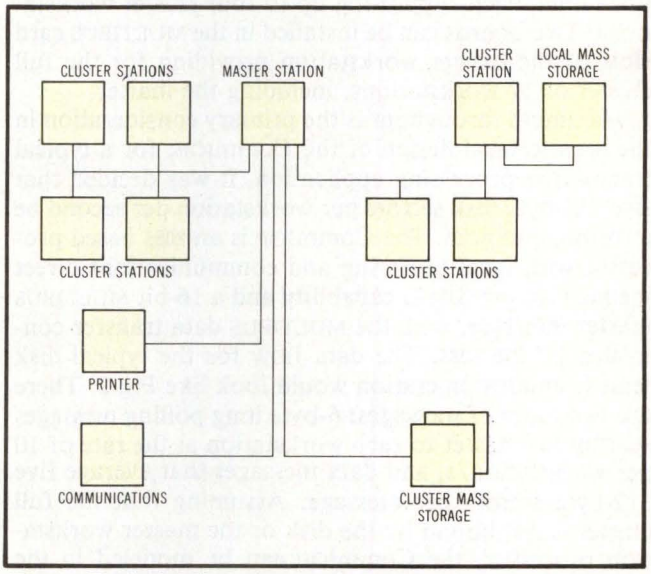

Fig 1 Typical full cluster facility. Both master and remote workstations are supported by communications I/O processors.

Functional upgrade to a full cluster had to meet the following requirements: no appreciable performance degradation in terms of throughput or response time at the cluster workstations; sufficient reserve power in the master workstation to run its own application without degradation; total user or application software transparency; no change to the master or cluster workstation form factors. The solution, the Communication I/O Processor (CommIOP), consists of an intelligent cluster communications frontend processor that resides in the MULTIBUS portion of the master workstation. Software performs all lower level protocol tasks such as polling, frame validation, and error recovery. Multiprocessing software links the CommIOP to the master workstation's central processing unit, the 8086 CPU, via a window in the master workstation RAM address space.

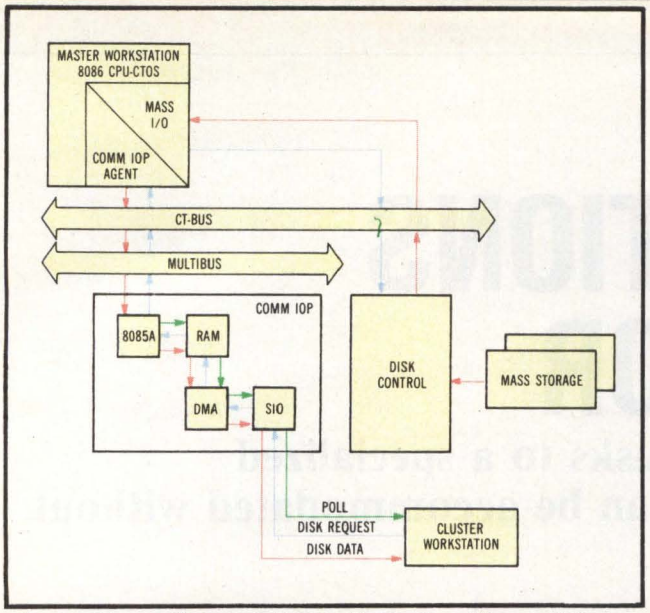

Fig 2 Cluster disk read data path. Both polling and data messages are sent from master to workstations.

CommIOP architecture

Each CommIOP board controls two cluster communications lines, each supporting up to four cluster workstations. Two boards can be installed in the MULTIBUS card slots of the master workstation providing for the full cluster of 17 workstations, including the master.

Maximum throughput is the primary consideration in the architectural design of the CommIOP; for a typical transaction processing application, it was decided that five 512-byte disk sectors per workstation per second be a throughput goal. The CommIOP is an 8085 based processor with local buffering and communications direct memory access (DMA) capability and a 16-bit MULTIBUS master interface, with the MULTIBUS data transfer controlled by the 8085. The data flow for the typical disk read CommIOP operation would look like Fig 2. There are two types of messages: 6-byte long polling messages sent by the master to each workstation at the rate of 10 per workstation/s, and data messages that average five 512-byte sectors per message. Assuming that the full cluster is not bound by the disk or the master workstation processor, the CommIOP can be modeled in the following fashion.

CommIOP local bus bandwidth = line (DMA) bandwidth
+ MULTIBUS transfer bandwidth
+ message processing bandwidth
= 1.00

Let

W = Number of workstations per CommIOP
T = Throughput = (sectors/workstation/second)
= (sectors/ws/s)
M = Message processing time = (s/msg)

And assume

Polling rate	10 poll messages/ws/s
Polling message size	6 bytes/poll message
Disk read size	5 sectors/data message
Serial I/O DMA transfer time	2.6 μs/byte
Average MULTIBUS transfer rate (based on an 8085A block transfer loop)	70k bytes/s

Data transfer message rate is

$$T\,\frac{\text{sectors}}{\text{ws/s}} \times \text{Wws} \times \frac{\text{data msg}}{\text{5 sectors}} = 0.2\,\text{TW}\,\frac{\text{data msg}}{\text{s}}$$

It may be assumed for simplicity that all cluster messages are polls and data transfers. Thus, the total message throughput is

$$10\text{W}\,\frac{\text{poll msg}}{\text{s}} \times \frac{\text{6 bytes}}{\text{poll msg}} + 0.2\,\text{TW}\,\frac{\text{data msg}}{\text{s}} \times \frac{\text{5 sectors}}{\text{data msg}} \times \frac{\text{512 bytes}}{\text{sector}} = (60\text{W} + 512\,\text{TW})\ \text{bytes/s}$$

The amount of CommIOP bus bandwidth used for local serial I/O DMA transfer is

$$(60\text{W} + 512\,\text{TW})\,\frac{\text{bytes}}{\text{s}} \times \frac{2.6\ \mu\text{s}}{\text{byte}} = 2.6 \times 10^{-6}\text{W}\,(60 + 512\text{T})$$

Data messages are passed over the MULTIBUS from main memory to CommIOP local RAM under 8085A program control. The MULTIBUS transfer bus bandwidth is

$$0.2\,\text{TW}\,\frac{\text{data msg}}{\text{s}} \times \frac{\text{5 sectors}}{\text{data msg}} \times \frac{\text{512 bytes}}{\text{sector}} \times \frac{\text{s}}{\text{70k bytes}} = 7.31 \times 10^{-3}\,\text{TW}$$

Each message has a certain amount of interrupt and processing overhead associated with it. The total message rate is

$$(10\text{W} + 0.2\,\text{TW})\,\frac{\text{msg}}{\text{s}}$$

Now, the total bandwidth is

$$2.6 \times 10^{-6}\text{W}\,(60 + 512\text{T}) + 7.31 \times 10^{-3}\,\text{TW} + \text{MW}\,(10 + 0.2\text{T}) = 1.00$$

Solving for T in terms of W and M

$$\text{T} = \frac{1.00 - \text{W}\,(1.56 \times 10^{-4} + 10\text{M})}{\text{W}\,(8.64 \times 10^{-3} + 0.2\text{M})}\ \frac{\text{sectors}}{\text{ws/s}}$$

Fig 3 shows throughput as a function of the number of workstations per CommIOP and the amount of message processing time. W = 8 workstations was the design goal and M = 2 to 4 ms was considered to be an accurate range of values for message processing time. This corresponds to a throughput range of 8 to 11 sectors/ws/s, greater than the design requirement for T, selected as 5.

Empirical analysis of the master workstation with no CommIOP yielded the following results; as more workstations were added to the minicluster, functions performed at the master workstation would, at times, appear sluggish due to interrupt processing during periods of high cluster activity; and response time at the cluster workstation tended to be longer than expected due to heavy usage of the communications line.

The introduction of the CommIOP provided a solution to both problems. Interrupt processing was eliminated by moving communications functions from the master workstation to the CommIOP. Overall performance of the cluster was improved by providing additional communications lines thereby reducing the number of cluster workstations per line.

Architecture that would not introduce new loads on the master workstation was required. Reduction of the

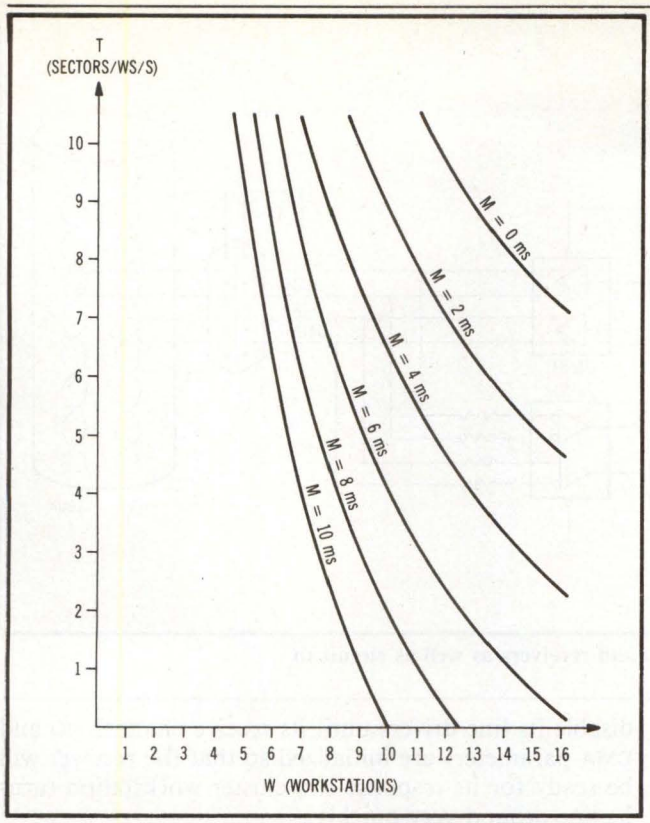

Fig 3 Line throughput performance. High data transfer rates are achieved by placing communication functions in communications I/O processor.

processing overhead of each request received from the cluster workstation was also needed. In addition, it was desirable to use existing Convergent Technologies CTOS™ operating system functions to ease integration.

Relocation of the communications functions from the master workstation to the CommIOP was the solution. Queues, located in the master workstation's memory, were introduced to handle communication between the master workstation and the CommIOP.

Local processor

Fig 4 shows a block diagram of the CommIOP hardware viewed in terms of local and multiprocessing elements. The local processor is a 3-MHz 8085A, selected for its simplicity; relatively few support chips are required to provide functions such as DMA and multiple interrupt sources.

Interrupts from the master workstation to the CommIOP are serviced by decoding one of four switch-selectable MULTIBUS output instructions. Output of the slave decoding logic is connected to the RST7.5 edge-triggered interrupt input on the 8085A. This logic also generates a MULTIBUS transfer acknowledge signal XACK that indicates to the master the cycle may be completed. Level interrupts from the line controller and programmable timer are connected to the RST 6.5 and RST 5.5 inputs, respectively.

The CommIOP contains 32k bytes of local dynamic RAM that consists of 250-ns dynamic 16k RAM chips controlled by an 8202A dynamic RAM controller. A

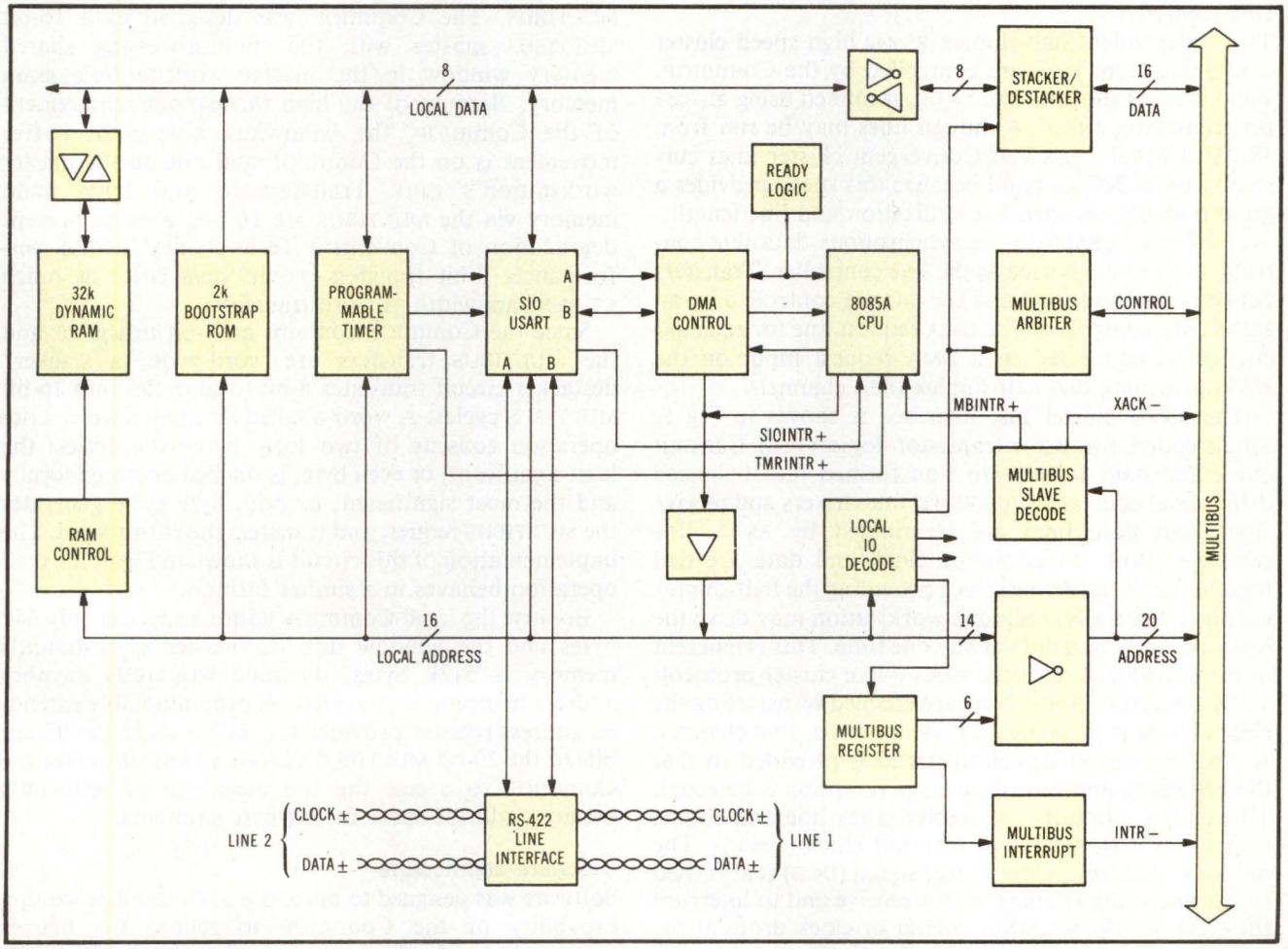

Fig 4 Communications I/O processor hardware block diagram.

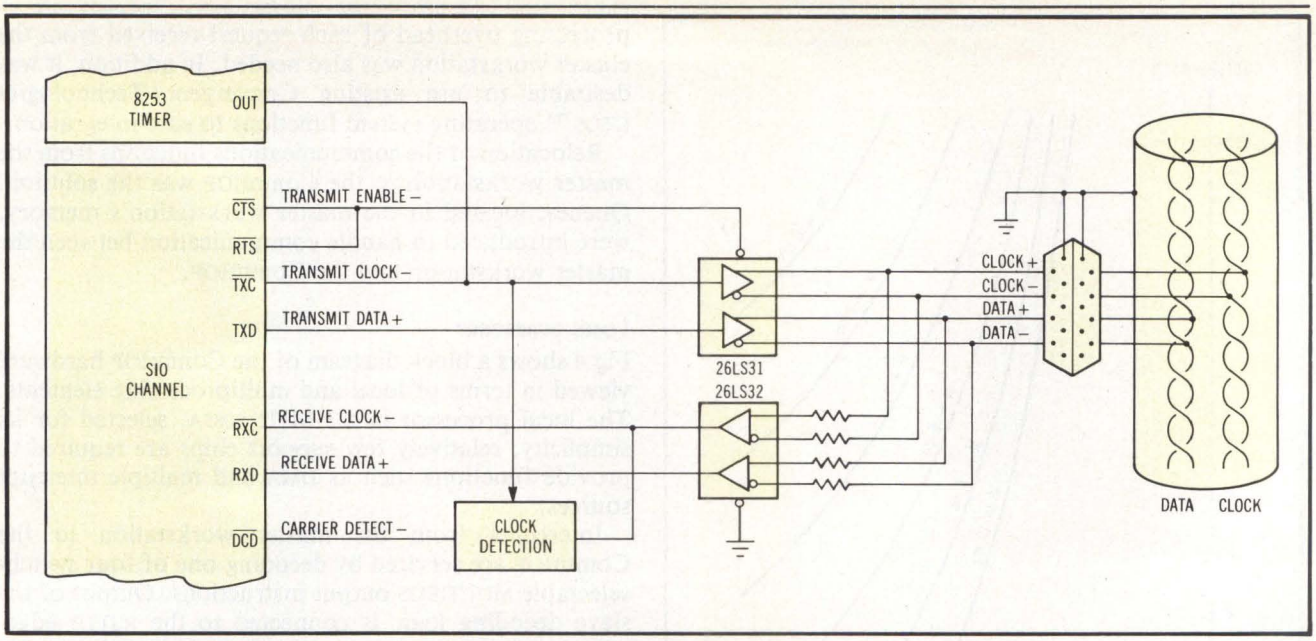

Fig 5 Cluster line interface. Circuit includes RS-422 line drivers and receivers as well as circuit to detect presence of clock online.

synchronous LSI RAM controller was selected as opposed to a faster asynchronous discrete controller because of board density limitations. The goal was to provide as much functionality as possible within the cost objectives. The result was a 6-layer board with as much logic implemented in large scale integration (LSI) as possible.

Line controller

Two independent half-duplex RS-442 high speed cluster communications lines are controlled by the CommIOP. Baud rates of the lines can be programmed using an 8253 programmable timer. Although lines may be run from 18.75 to 614.4k baud all Convergent cluster lines currently run at 307.2k baud because this speed provides a good tradeoff between line utilization and line length.

A Z80A-SIO USART in the synchronous data line control (SDLC) mode is used as the line controller. Transfers between the local RAM and the SIO are controlled by an 8257-5 DMA controller. The DMA request line for each SIO channel is connected to a DMA request input on the 8257-5 providing two half-duplex DMA channels.

The RS-422 cluster line interface is shown in Fig 5. Single-ended transistor-transistor logic (TTL) transmit clock and data signals are transformed into balanced differential equivalents by RS-422 line-drivers and receive clock and data lines are terminated by RS-422 line receivers. Both directions of clock and data are tied together at the RS-422 interface providing the half-duplex channel. Naturally, only one workstation may drive the line with clock and data at any one time. This is inherent in the polled nature of the ADCCP-like cluster protocol. The CommIOP's line drivers are enabled by asserting the clear to send (CTS) signal pin on the SIO for that channel. A clock or carrier detection circuit is provided so that the beginning and end of message reception is detected. This circuit monitors the receive clock line and counts transitions with respect to transmit clock periods. The output is the data carrier detect signal (DCD) that is used to automatically enable the SIOs receive and to interrupt the 8085A via the SIO when carrier or clock drops at the end of the message reception. The CommIOP does not disable its line drivers until its receive channel SIO and DMA parameters are initialized so that the receiver will be ready for its response if a cluster workstation turns its line around very quickly.

Multiprocessing hardware

Multiprocessing capability is provided via the MULTIBUS. The CommIOP was designed as a 16-bit MULTIBUS master with the multiprocessing shared memory window in the master workstation's main memory. Because of the high throughput requirement of the CommIOP, the bandwidth burden of buffer movement is on the CommIOP and not on the master workstation's CPU. Transfers to and from main memory via the MULTIBUS are 16 bits wide to prevent degradation of Convergent Technologies' CT-BUS performance; 8-bit transfers would steal twice as much CT-BUS bandwidth as word transfers.

Since the CommIOP contains an 8-bit processor and the MULTIBUS transfers are word-wide, a stacker/destacker circuit translates 8-bit local cycles into 16-bit MULTIBUS cycles. A word-aligned MULTIBUS word write operation consists of two local byte-wide cycles: the least significant, or even byte, is stacked or stored locally and the most significant, or odd, byte cycle generates the MULTIBUS request and transfers the entire word. The implementation of this circuit is shown in Fig 6; the read operation behaves in a similar fashion.

Because the local CommIOP address space is only 64k bytes and the window into the master workstation's memory is 512k bytes, dynamic MULTIBUS memory address mapping is provided. A programmable extended address register provides for the six most significant bits of the 20-bit MULTIBUS address which allows for the CommIOP to access the full megabyte of MULTIBUS memory address space in 16k-byte segments.

Software architecture

Software was designed to make use of the multiprocessing capability of the CommIOP to relieve the master workstation of all communications processing. It

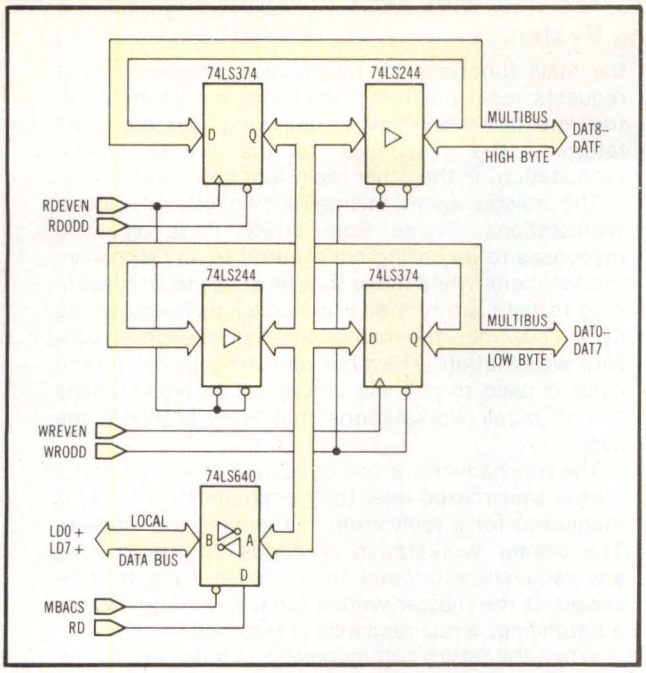

Fig 6 MULTIBUS stacker/destacker circuit. Circuit translates byte wide local cycles used by 8-bit 8085A into 16-bit word wide MULTIBUS cycles for master's 8086.

processes requests which the CommIOP received from the communications lines and places in queues located in the master workstation's memory.

The communications functions formerly performed by the master workstation were moved to the CommIOP. A new module, called the CommIOP handler, maintains queues to buffers in the master workstation's memory. These buffers can be shared by both processors. The CommIOP handler is an operating module that fields interrupts received from the CommIOP and processes entries placed in the queues.

Four communication queues are maintained (Fig 7). The first queue, called the free buffer queue, contains pointers to available buffers in the master's memory. When the CommIOP receives a request from the cluster workstation, it extracts an entry from this queue, copies the data into the buffer, and places the entry onto the incoming request queue. Entries in the incoming request queue are removed by the master workstation and submitted to the appropriate CTOS process for servicing. Results are placed on the outgoing response queue and are copied into the CommIOP's local memory for subsequent transmission over the communications line to the appropriate cluster workstation. The buffer is finally released and placed in the transaction complete queue. Entries from this queue are placed on the free buffer queue where the cycle begins again. This last operation is necessary to provide lock-free operation.

The communication code at the master workstation is replaced by the CommIOP handler that handles the queues and fields interrupts from the CommIOP. Interrupts are used only when the master workstation is idle; during normal operation, the queues are sampled until they are empty.

At initialization time, the master workstation resets each CommIOP. Diagnostic tests to ensure the correct functioning of hardware components (communications, timers, memory, etc) are then performed by the CommIOP to isolate faulty communications lines and inform the master workstation of any problems. The CommIOP downloads its operating code from the master workstation's memory. The operating code is soft (ie, RAM resident vs ROM resident) to allow future adaptations to cluster protocol. The initialization step is completed with the master workstation providing the CommIOP with runtime information such as line speed, number of cluster workstations per line, and the location of the queues in the master workstation's memory.

CommIOP software, designed for fast interrupt response time—a necessary function in the communications model of the cluster workstation—contains four processes: one for each communications line, a timer handler, and the queue handler. The communications and timer processes are interrupt driven, while the queue handler is a low priority process using up the spare CPU time.

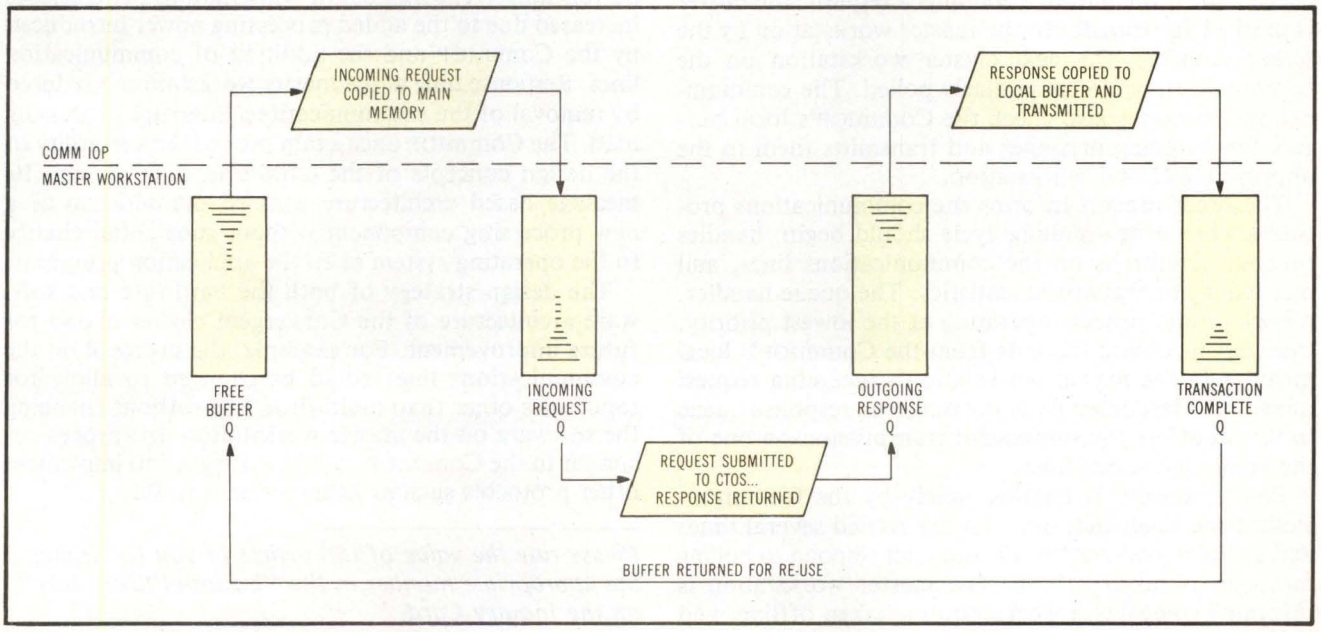

Fig 7 Queue management. Four communication queues are maintained by handler module in communications I/O processor.

The Operating System

CTOS, a message based operating system, consists of several processes that handle operating system tasks such as keyboard, video, and file management. Communications between these processes and user applications are accomplished through exchanges. When a service is to be performed, a request is placed on the exchange of the process that services the request. Completion messages, or responses, are returned to the calling process exchange.

In the cluster configuration of CTOS, certain processes are located on the master workstation allowing several workstations to share resources. In this configuration, the processes on the cluster workstations are replaced with an agent process that intercepts requests and transmits them over the communications line for servicing by the processes at the master workstation.

The protocol used for cluster communications is a subset of the American National Standard for Advanced Data Communication Control Procedures, ANSI X3.66-1979 (also known as ADCCP). The unbalanced, normal response mode with 2-way alternate transmission class of procedure is used. This protocol belongs to a group referred to as the bit oriented protocols that include IBM's synchronous data link control (SDLC) and the international standard for high level data line control (HDLC).

The master workstation assumes the role of the primary station in cluster communications, and as such, controls all operations over the communications link. Known as the master agent, this is one of the main functions of the process. Presentation of requests received from the cluster workstations to the master workstation operating system, and returning the responses to the proper cluster workstation, is the other main function.

The master agent maintains two lists of cluster workstations. Those from which it is receiving responses to its polling are referred to as responsive workstations while those that have not been responding to polls are termed unresponsive. Every polling cycle (100 ms), the master agent polls each responsive workstation. The time remaining in the polling cycle is used to poll any unresponsive workstations and to repoll workstations that were active in the cycle.

The mechanism for polling is as follows: a control frame, transmitted over the communications line, is monitored for a reply from the cluster workstation. The cluster workstation responds by transmitting any requests submitted to it for servicing by processes at the master workstation. If no requests are outstanding, a null response is returned.

When the return communication containing the request is received from the cluster workstation, the master agent performs a series of protocol and higher level checks on the transmitted data. Retransmission is requested if any of these checks fail. Otherwise, the request is sent to the appropriate process for servicing. When the response is returned, the agent adds protocol information to the response and transmits it to the cluster workstation.

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The two communications processes handle the messages sent to and received from the cluster workstations. Their operation is similar to the master's communications functions described previously. At regular intervals, a polling message is constructed for a cluster workstation and transmitted on the communications line. The line is then monitored for a response message from the cluster workstation, the return message is validated and, if the message contains a request, the buffer is marked for transfer to the master workstation by the queue handler. The next cluster workstation on the communications line is similarly polled. The communications processes also check the CommIOP's local buffers for outgoing messages and transmitts them to the appropriate cluster workstation.

The timer process informs the communications processes when a new polling cycle should begin, handles timeout conditions on the communications lines, and maintains line utilization statistics. The queue handler, a background process operating at the lowest priority, transfers incoming requests from the CommIOP's local memory to the master workstation's incoming request queue, and responses from the outgoing response queue to local buffers for subsequent transmission on one of the communications lines.

Error recovery is handled solely by the CommIOP. Polling messages that time out are retried several times and a cluster workstation that does not respond to polling messages is taken offline. The master workstation is informed whenever a workstation is taken offline, and purges any outstanding requests for that cluster workstation.

The CommIOP maintains various statistics including line utilization and communication errors. These statistics are sampled periodically by the master workstation and are used to evaluate cluster loading and to diagnose fault conditions on the communications lines.

Conclusions

The CommIOP provides several improvements in cluster performance. The number of workstations per cluster is increased due to the added processing power introduced by the CommIOP and the addition of communication lines. Response time at the master workstation is reduced by removal of the communications interrupt processing load. The CommIOP once again proved the versatility of the design concepts of the CTOS operating system. Its message based architecture enabled the addition of a new processing component without substantial change to the operating system or to the application programs.

The design strategy of both the hardware and software architecture of the Convergent cluster allows for future improvement. For example, the protocol on the communications lines could be changed to allow for topologies other than multi-drop line without changing the software on the master workstation. I/O processors similar to the CommIOP could be designed to implement other protocols such as Ethernet or IEEE 802.

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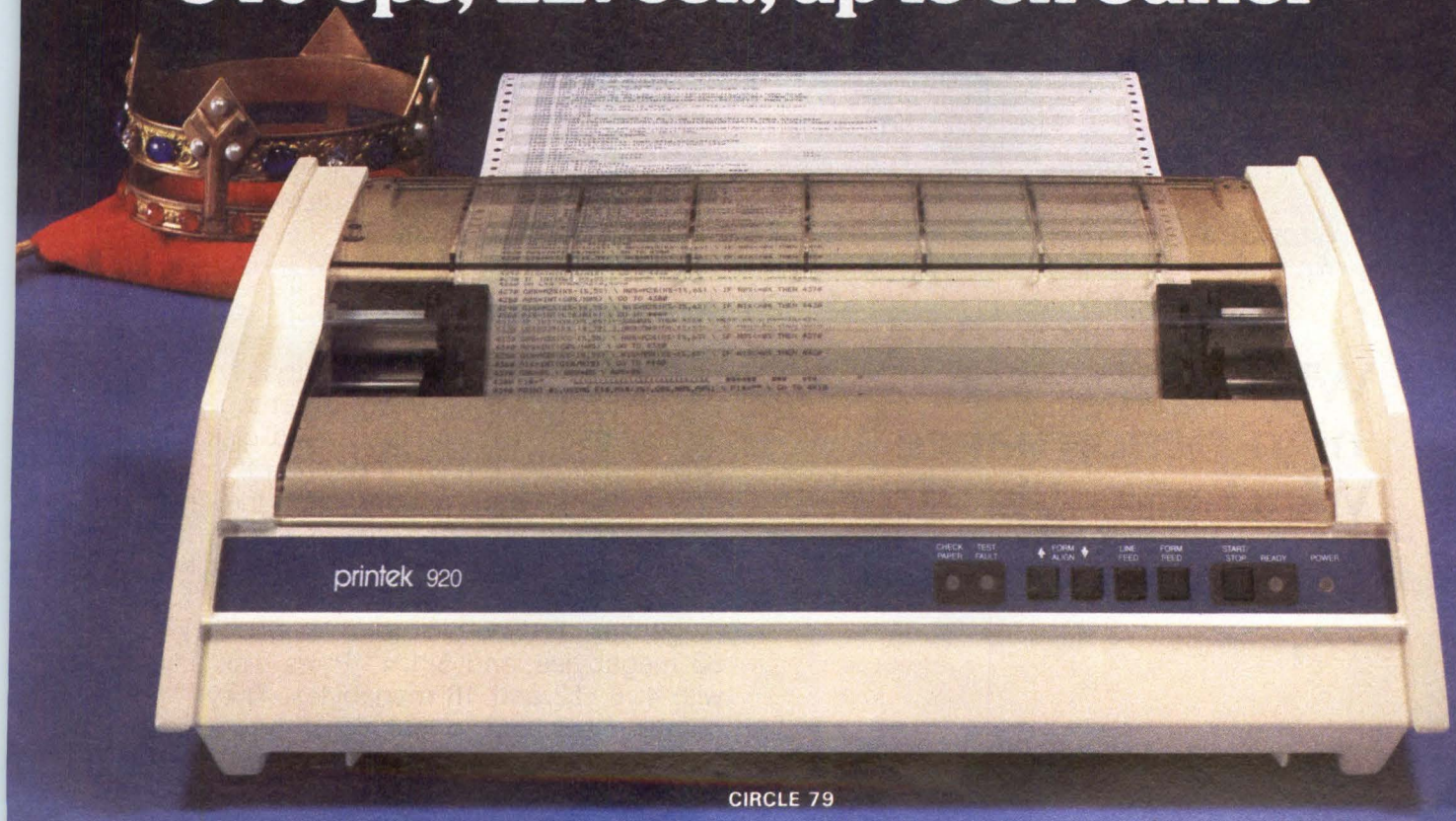

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CIRCLE 81

APPROACHING FILTERS DISCRETELY

Digital techniques can be used to approximate the effects of filters if the moving average statistical method is applied with monolithic signal processors

by Stan Mazor

Suddenly, the availability of low cost monolithic analog to digital converters, microcomputers, and new signal processor chips makes low pass digital filters practical; however, many computer experts lack experience with signal processing and filtering. Rather than the usual analog approach, an intuitive and digital point of view approach is feasible. The analysis technique is a moving average statistical method.

Statistics provide a set of analytical tools that aid in finding the true meaning concealed in a barrage of raw data. The moving average statistical technique is an easy way to identify a developing trend over time. It can be used to chart the price change of a stock, the value of a bushel of corn, or the cost of living in the inflated '80s. It is simply a smoothing technique for averaging a set of successive samples.

The processing of signals in real time can use the moving average statistical technique to filter a signal in order to separate it from noise. Fig 1 illustrates a 4-stage moving average network where T1, T2, T3, and T4 each hold a single sample of a signal. The four most recent samples are always remembered with T1 as the most recent and T4 the oldest. As each new sample is loaded into T1, the older samples are moved to the right while the oldest sample (in T4) is discarded. The averaging part of the network produces a result each sample time, ie, the average of the latest four samples. Physically, T1 through T4 are represented as registers or memory locations in a computer.

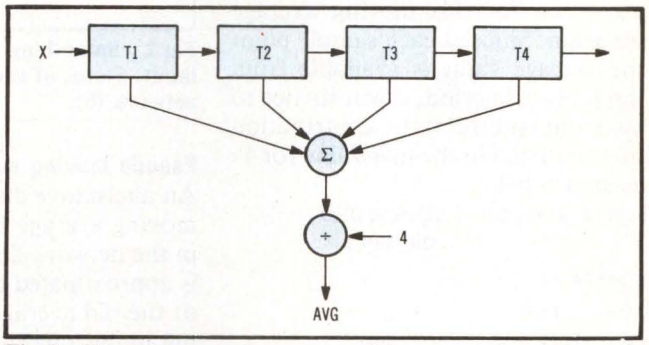

Fig 1 Four stage moving average filter network. T1 through T4 can be represented as either registers or memory locations.

Moving average example

To illustrate the smoothing characteristics of this network, two sample inputs are considered (Figs 2 and 3). For simplicity, only a simple digital waveform is used, and two different frequencies are analyzed.

In Fig 2(a) the input signal is zero except for one sample period in which it is 1 V. The output of the moving average network is shown for each sample period below the input (a). Note that the amplitude of the signal is reduced to 0.25, and the duration is four time units. Both the status of each storage location, and the resultant average for that stage, can be seen as the 1 is shifted through the network.

In Fig 3(a) the input goes to 1 V for eight sample periods. Building up to 1 V, the output then maintains this value after four sample periods [Fig 3(b)]. After the input value returns to zero, the output steps down to zero in four steps. If the input signal were longer, the output would more closely resemble the input.

If these cases are repeated, the frequency aspects can be considered. A high frequency signal (series of short pulses) would not faithfully pass through the network,

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while a low frequency (long pulse) would pass. This type of network is called a low pass filter.

Active program

A low pass filter can be built with microcomputer signal processor chips such as the Intel 2920. A typical moving average program is shown in 2920 symbolic code in Fig 4. The first four instructions shift the samples; the newest sample enters T1 from the analog to digital sample register (DAR). The average is actually computed by adding 0.25 of each value of the samples to SUM. The R02 designation causes the T1 value to be shifted two places to the right (0.25) before adding to SUM. This program is reiterated each sample period, with the value in SUM used as the filter's output.

Upon reflection, a clever programmer might suspect that for the steady state case, there is a simpler algorithm for this moving average program. Since at each sample point the average value is available from the previous period, it will suffice to back out (subtract) the contribution of T4 and add in the new value for T1 as shown below:

```
SUB SUM, T4, R02    ;Delete 0.25
                     old sample

LDA T4, T3
LDA T3, T2
LDA T2, T1
LDA T1, DAR
ADD SUM, T1, R02    ;Add 0.25
                     new sample
```

This program does not work for the first few passes, but in the frequency domain the startup stage is usually ignored while the steady state operation is focused on. The results obtained are similar to the previous program.

Tuning the filter

The number of stages, chosen arbitrarily as n = 4 for this filter, controls the range of frequencies that is passed or rejected. The most recent sample is multiplied by 1/n, and if more stages are used, the contribution of the incoming sample is reduced. Thus, increasing the number of stages increases the dampening and lowers the frequencies that are passed. However, if 100 stages were used, the program would require a large number of separate memory locations and a longer execution time for passing the data from stage to stage.

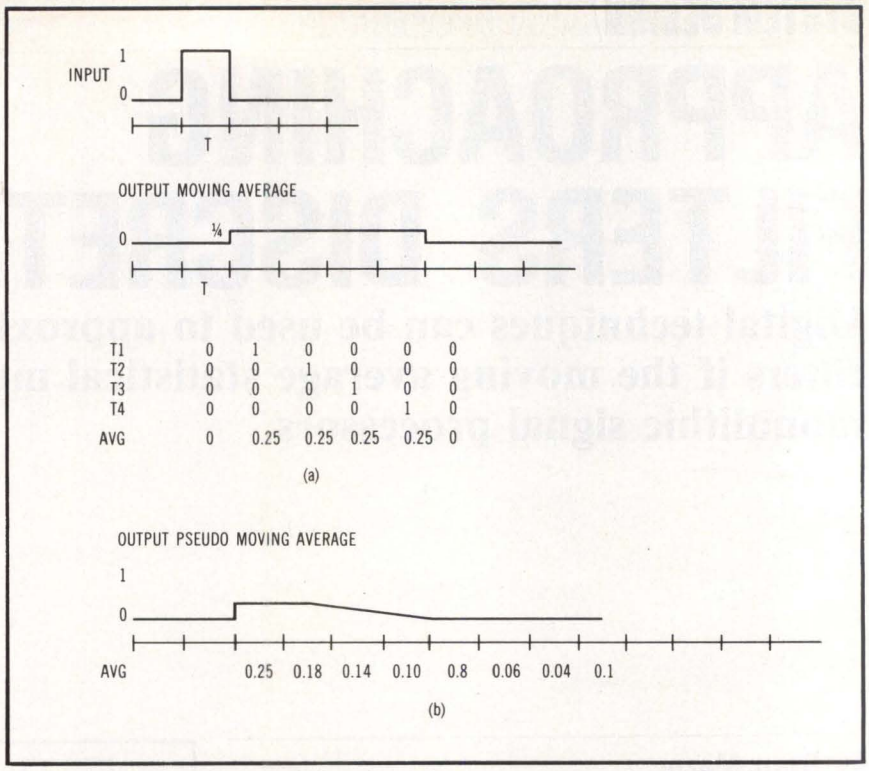


Fig 2 Smoothing characteristics of moving average network with low frequency input. Status of each storage location (a) and output of pseudo moving average network (b).

Pseudo moving average

An alternative discrete low pass filter can be designed by approximating the moving average function with a single memory location. This is illustrated in the network diagram in Fig 5. In this system, the 4-stage moving average is approximated by adding 0.25 of the incoming signal and subtracting 0.25 of the old average. This is not as accurate as taking out the oldest sample, but in the long run the average value removed is a good approximation. The pseudo moving average program for four stages requires only two instructions on the 2920.

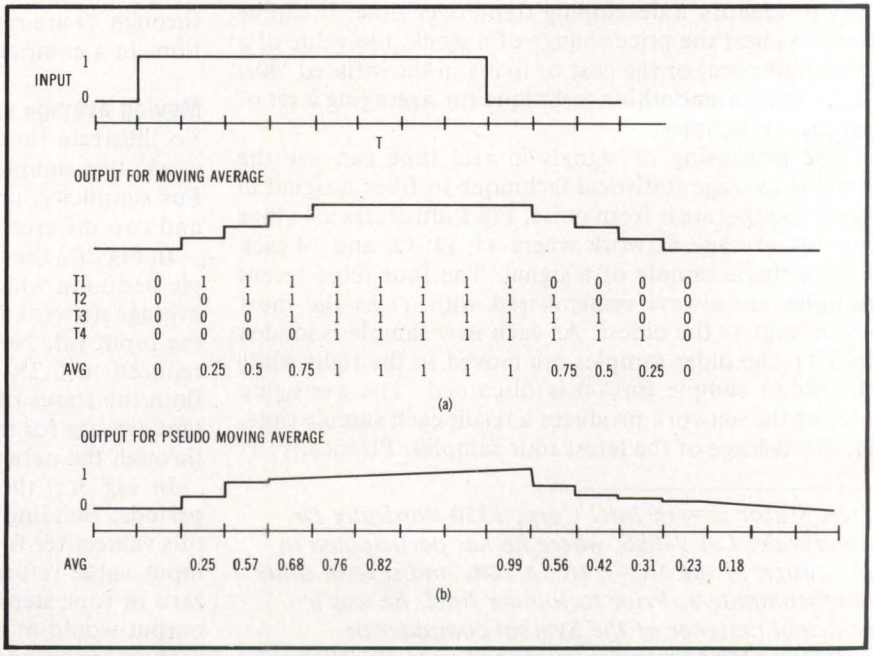
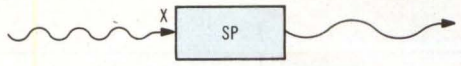


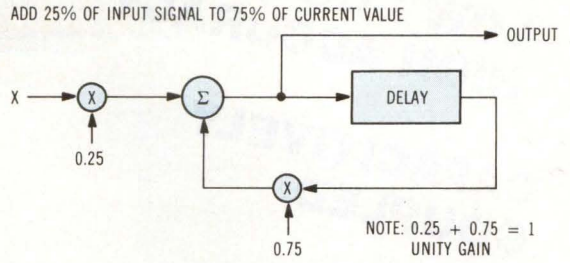
Fig 3 Smoothing characteristics of moving average network with high frequency input. Status of storage locations (a) and output of pseudo moving average network (b).



COMPUTE THE CONTINUOUS MOVING AVERAGE OVER 4 TIME STATES
OF AN INPUT SIGNAL X

```
LDA T4, T3          ;MOVE T3 TO T4
LDA T3, T2
LDA T2, T1
LDA T1, DAR         ;LATEST VALUE OF X
LDA SUM, KPO        ;ZERO THE SUM
ADD SUM, T1, RO2    ;ADD 0.25 T1
ADD SUM, T2, RO2    ;
ADD SUM, T3, RO2    ;
ADD SUM, T4, RO2    ;
;NOW OUTPUT SUM
```

Fig 4 Typical assembly code program for moving average network. Program is reiterated for each sample period.




```
PSEUDO MOVING AVERAGE PROGRAM
SUB SUM, SUM, RO2    ;    75% OF OLD AVERAGE
ADD SUM, DAR, RO2    ;    25% OF NEW VALUE
```

Fig 5 Pseudo moving average filter network. Only one memory location is used in approximation.

Example operation of pseudo moving average

To understand the smoothing operation of this network, consider the two sample input waveforms in Figs 2(b) and 3(b). These waveforms show the output for the pseudo moving average operation. In Fig 3(b) the output now achieves only 0.25 V output and then decays exponentially to zero. The fact that the output is very low illustrates the dampening effect the network has for high frequency signals. In Fig 3(b) for a lower frequency signal, the output more closely resembles the input, illustrating that this is a low pass filter. A general low pass filter can be represented by the equation

$Y_n = G * X + B * Y_{n-1}$ where

X—input sample
G—weighting constant for input
Y_n—currently saved value
B—constant weighting factor

For the 4-stage analogy, G = 0.25 and B = 0.75, ie,

$$Y_n = 0.25 * X + 0.75 * Y_{n-1}$$

Note that the SUM of the weighting coefficient = 1

To design a filter equivalent to a 16-stage moving average would require using values of B = 1/16 and G = 15/16 (B = 0.0625 and G = 0.9375). Using numbers that these numbers are powers of 2 and can be implemented as shifts. For the 2920, the code for 107-Hz low pass filter and 100-μs sample rate is implemented in two instructions:

```
SUB SUM, SUM, RO4      ;0.9375 * SUM
ADD SUM, DAR, RO4      ;0.0625 * INPUT
```

The Bode plot and low pass filters

Low pass filters are usually characterized by the frequencies they pass or block. A plot of the frequency response for a typical filter is shown in the Figure. The cutoff frequency F_C is marked, delineating the pass- and stopband region. Amplitude is shown in decibels, frequency in hertz. The constant coefficients (B and G) for a given sampling system can be simply derived to implement a low pass filter with a specified cutoff frequency F, with the equations $B = e^{-F \cdot T \cdot 2\pi}$ and G = 1 − B.

As an example, suppose a low pass filter is needed that will pass signals of 100 Hz or lower, in a system that takes a sample every 100 μs ($T = 1 \times 10^{-4}$).

$$B = e^{-F \cdot T \cdot 2\pi} = e^{-100 \cdot 1 \times 10^{-4} \cdot 2\pi} = e^{-0.06} = 0.94$$

$$G = 1 - 0.94 = 0.06$$

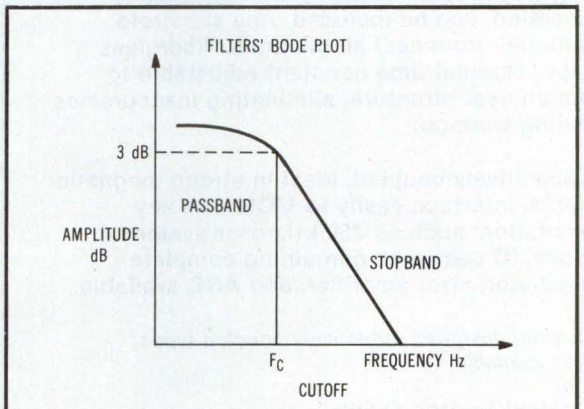
Then using equation 1,

$$Y_n = G * X + B * Y_{n-1}$$

$$Y_n = 0.06 * X + 0.94 * Y_{n-1}$$

The desired 100-Hz low pass filter can be implemented with two multiplications and one addition as shown above.

In certain cases, however, the specifications might be relaxed to simplify computer arithmetic. For example, a filter with cutoff frequency of 107 Hz gives B = 0.9375 and G = 0.0625. Recall from the Table



AMPLITUDE OF VOLTAGE IS PLOTTED IN DECIBELS WHERE $dB = 20 \log_{10}\left|\frac{V_0}{V_1}\right|$
THE AMPLITUDE AT CUTOFF FREQUENCY IS 3 dB DOWN (0.707)
THE SLOPE OF THE ROLLOFF IS 20 dB/DECADE (ie, AS FREQUENCY INCREASES BY FACTOR OF 10) OR EQUIVALENT TO 6 dB/BINARY OCTAVE FOR SIMPLE FILTERS

TABLE

$1 - 2^{-n}$

n	2^{-n}	$1 - 2^{-n}$	Stages Simulated
1	0.5	0.5	
2	0.25	0.75	4
3	0.125	0.875	8
4	0.0625	0.9375	16
5	0.03125	0.96875	32
6	0.015625	0.984375	64
7	0.007812	0.992188	128
8	0.00390625	0.99609375	256
9	0.001953125	0.998046875	512
10	0.0009765625	0.9990234375	1024

that are powers of 2 simplifies the multiplication because shifting can be used. (See the Table.) Regardless of the number of stages, the pseudo moving average technique uses only one memory location and is powerful, yet simple.

An alternative discrete low pass filter can be designed by approximating the moving average function with a single memory location.

Conclusion

When microcomputers receive signals containing noise, it may be practical to reject certain frequencies with low pass or bandpass filters implemented via digital programming logic. The use of this simple technique for simulating low pass filters can greatly enhance the value of the microprocessor or signal processor chips in complex system designs.

Acknowledgments

The author would like to acknowledge the work of Dr M. E. Hoff on the 2920.

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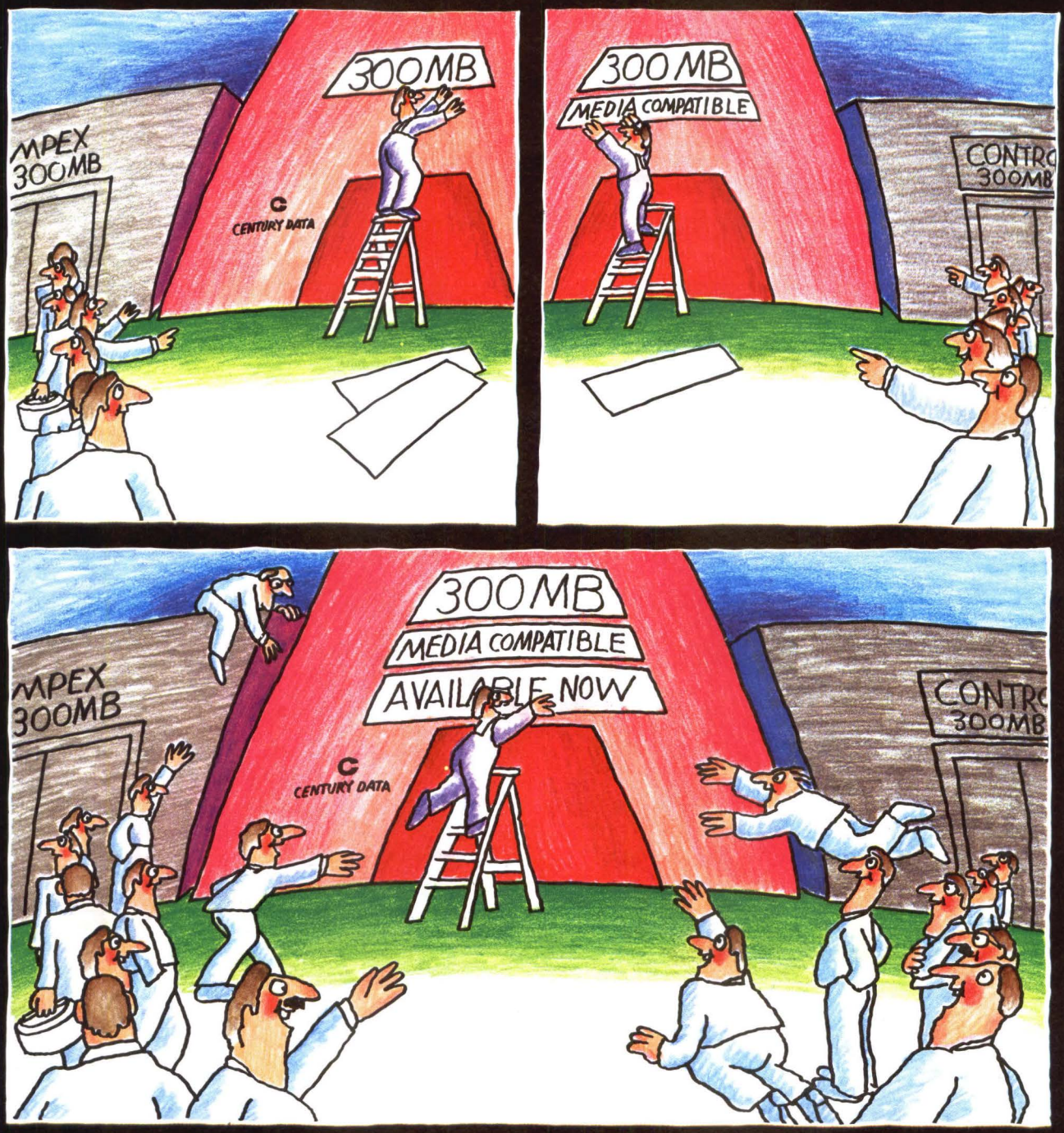

Century Data's new T306 disk drive: It's what a lot of 300 MB-removable users have been waiting for.

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Introducing the Trident T306 – ready for shipment today and well worth the wait. Because it's more than a match for any other removable-pack drive on the market.

Take the way our design attacks the problem of head crashes:

Continued on next page

"The last thing we ever needed was a spare Trident."

Tom Amerson, President
Consultant Field Engineering
Mission, Kansas

At Century Data, we always knew the quality of our Trident removable-pack disk drives could speak for itself. But a lot of Trident users are speaking up, too.

For instance, there's Tom Amerson, president of Consultant Field Engineering, an independent service company that maintains over 200 brands of computer equipment.

Mr. Amerson is also chairman of the board of IASCO, the International Association of Service Companies, a new organization that seeks to establish standards for the industry.

He has a lot to say about Tridents:

"Tridents are terrific. Three years ago, we bought a spare drive for one of our customers. But we never used it because the Tridents it was backing up never broke down.

"That isn't really unusual for a Trident, though. In the last six years, I haven't seen more than one head crash in a Trident. Which is something I sure can't say about other manufacturers' drives.

"Overall, Tridents are just amazingly reliable. In fact, we don't do much business writing service contracts on them. Most people would rather just call us once a year for maintenance. And really, that's about all the attention a Trident needs."

Needless to say, Mr. Amerson likes our Tridents a lot. We think your customers will like them, too. Why not give us a call, today, and get the details.

T306

Continued from first page

a catamaran head shape significantly improves aerodynamic performance.

And Century's special air filtration system helps eliminate contaminants that could cause a crash in the first place.

What's more, Trident T306 is quiet. Very quiet, in fact. Our design meets not only the NC55 quietizing standard for office environments, but even exceeds this standard.

We think of it as the Rolls Royce of disk drives. Quiet. Reliable. But with no price penalty.

We've been making removable-pack drives for 13 years—tens of thousands of them and there's plenty more where those came from.

In fact, new assembly and test facilities have significantly increased our Trident production capacity.

No other manufacturer has achieved our level of reliability because no other can match our design, engineering, manufacturing and testing capability and technology.

Put your order in today for the no-wait drive with maximum up-time. Trident T306.

Something few repairmen will ever see: Inside a Century Data Trident.

There are a lot of reasons why we call Tridents reliable. But basically, it's because we designed them right the first time.

And we manufacture them in an exacting way. In fact, every Trident that leaves our facilities is virtually a Winchester. If you never remove the disk pack, it's a Class 100 clean room environment inside.

These 50 MB through 300 MB drives are engineered for what you need. Lower maintenance costs over the life of the product. And easy maintenance when it is needed.

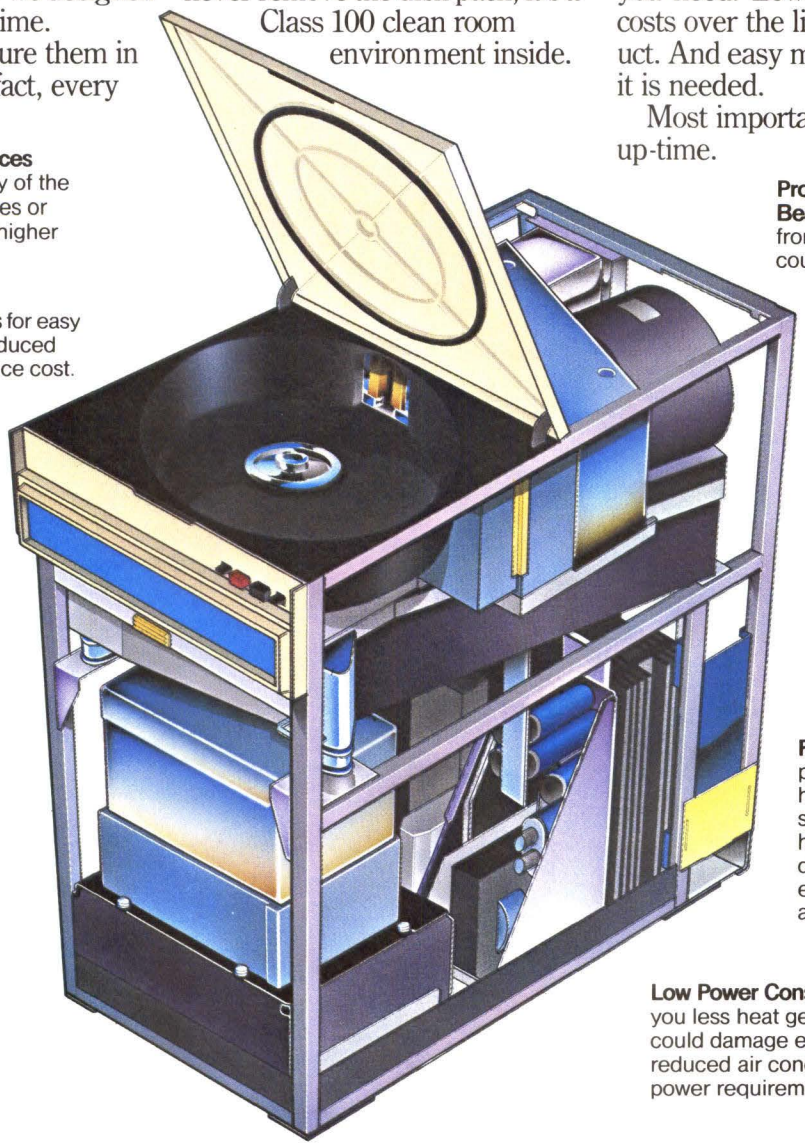
Most important: maximum up-time.

Parallel Disk/Head Surfaces assure far greater stability of the head over uneven surfaces or dust particles, providing higher data integrity.

Hinged Major Assemblies for easy maintenance, giving a reduced downtime and maintenance cost.

Advanced Seal Design keeps out airborne contaminants during repair or routine maintenance (other drives violate the purified-air section of their drives even for a head cleaning).

More Thorough Contamination Control has been a major goal at Century, and we've designed an absolute filtration system that removes particles to 0.3 microns. Air flow is routed in a full 360° pattern to purge all internal areas of contaminants (air leaves through a single port rather than the common method of air leaving the drive anywhere through several holes in the housing).



Protected Carriage Bearings are isolated from air movement that could dry out the lubricant.

Tunnel Cover over carriage acts further to keep contaminants out of the airstream, in effect creating an enclosed Winchester environment.

Symmetrical Carriage and Way is assured by a proven, high-precision tri-rail positioning and stabilizing system, giving the highest level of data integrity.

Rigid Deck Plate assures perfect alignment of head, carriage, disk, and spindle (other drives have flexible or independent support of these elements—a less reliable design).

Low Power Consumption gives you less heat generation that could damage electronics, plus reduced air conditioning and power requirements.

SMD-compatible 200 MB Tridents: Available now.

As modern office equipment grows more sophisticated, floor space grows more valuable. So when we developed our new Trident T202 removable pack drive, we decided to think small.

The result is a compact, low-maintenance 200 MB drive that not only saves floor space, but also makes a perfect plug and media-compatible replacement.

Being small has other advantages, too. It uses less energy.

Century T202. The only thing big about it is the way it performs.

We've packaged the ultimate mass storage breakthrough for microcomputers.

Maximized system performance. Minimized system overhead. A strong growth path for future data storage needs.

These are the ideals that the Marksman T-Series is designed to meet—a complete mass storage system of Winchester drive, streaming ¼" cartridge tape drive, intelligent and composite disk/tape formatter.

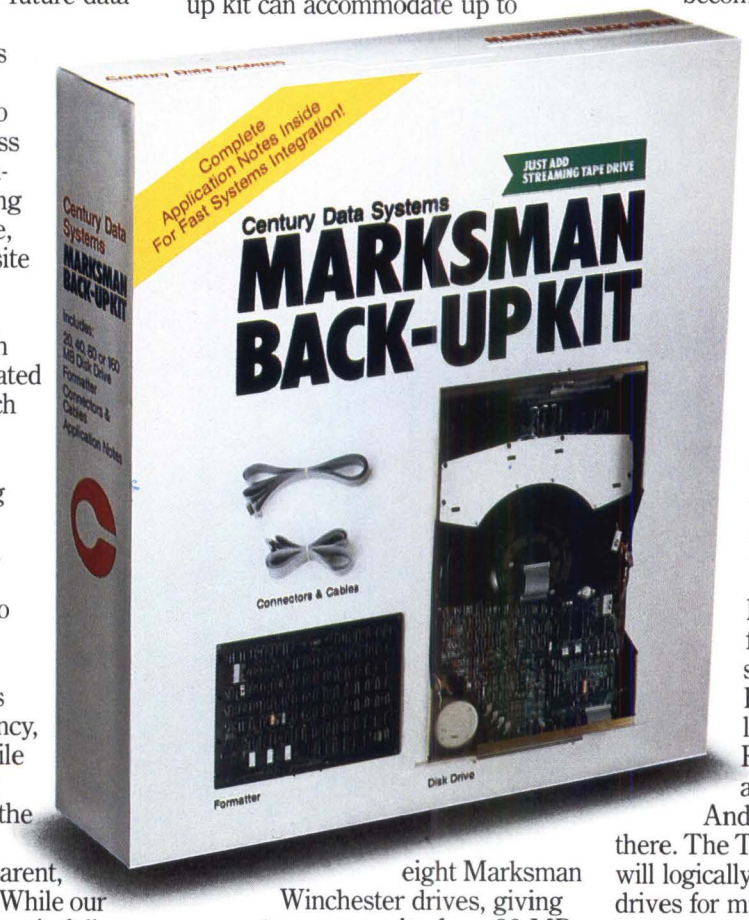
Enter a new era of mass data storage with T-Series. Easily integrated into bus structures such as S-100 or Multibus (with a simple host adapter) and operating system environments such as CP/M, MP/M, UNIX and others.

Plug our system into your system for mass storage that gives you extreme reliability, has the highest cost efficiency, and Winchester/tape file loading and unloading without downtime for the operator.

The secret is transparent, prioritized commands. While our new T-Series Marksman is fully or selectively backing up data onto ¼" streaming tape, direct requests from the CPU for access to data files on the disk can be given higher priority. The user is unaware of any time lapse as the back-up function is interrupted, the user's data need is fulfilled, and the back-up function is resumed, without further host system intervention.

Marksman Winchester.

The Century Data Systems back-up kit can accommodate up to eight Marksman Winchester drives, giving you a storage capacity from 20 MB to 160 MB per drive, enabling a total capacity as high as 1280 MB.



Plus, you get the reliability and random-access speed of Winchester, for the most user-friendly mass storage system available today.

1/4" Streaming Tape.

The Marksman T-Series ties into what may be the ultimate Winchester back-up device—¼" streaming cartridge drives. They are fast becoming recognized as the ideal sequential-data drive available today. Because dump/restore and program entry could never be performed as inexpensively and quickly before.

No other back-up drive has the cost-efficiency, speed and large removable capacity of ¼" streaming tape.

In fact, cost per megabyte never looked so good.

Ultimate Marriage.

From one up to eight Marksman drives, and from one up to four streaming tape drives. High data integrity and low cost per megabyte. Reliability. Non-stop user access to data files.

And the story doesn't end there. The T-Series formatter board will logically partition Marksman drives for multiple users. Each user is given continual access to dedicated files, and each user can interrupt a dump/restore command, which will resume after the request for data is completed.

Just fill out the coupon below, or give us a call for further information on the maximized storage system of tomorrow. Available today.

For the full Story of the Century: Just check the information you want, and we'll send it to you right away.

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CIRCLE 8 ON INQUIRY CARD

DESIGNERS, SHAKE HANDS WITH DATA STREAMING

Here's a way to mix and match mass storage units at 3M bytes/s

by Kenneth R. Lynch

Over the years, direct access storage technology has brought about a succession of devices that store more data in less space and transfer the data at faster speeds. Similarly, the performance characteristics of input/output interfaces have advanced to accommodate new devices.

For instance, the data streaming feature is a change to the IBM System/360 and System/370 input/output (I/O) interface, designed to advance its previous capabilities. Direct access storage device (DASD) developers at IBM were working on a new disk product whose speed would result in a data transfer rate of 3M bytes/s. In addition, since the amount of online data per system was projected to increase, the maximum interface length would have to be increased beyond the previous common interface length of 200′ (61 m). Increased interface length was needed so that more devices could be placed in the space around the system. Another projected increase was the number of DASD control units that attach to more than one system. Therefore, the future control unit would have to provide space for connecting more than one interface, allowing for attachment to two or more systems.

Moreover, the method of attaching the new DASD products had to be compatible with existing devices so that both old and new units could be mixed on the same I/O interface. Thus, the DASD products had four major requirements for future system support: a 3M byte/s transfer rate over the I/O interface; channel ability for the high data transfer rate at greater than 200′; avoidance of additional interface cable bulk beyond that required by the base I/O interface, allowing systems to provide more channels and enabling attachment of control units to multiple systems; and, finally, compatibility with existing devices. Although the then current bus extension feature met the data transfer rate compatibility requirements to mix old and new units, it failed to meet the specified data transfer rate at distances greater than 200′. Worse yet, the additional cable would further degrade I/O performance.

Kenneth R. Lynch is a staff engineer at IBM Corp, Dept E57, Bldg 702, PO Box 390, Poughkeepsie, NY 12602, working in I/O architecture. Previous experience includes technical writing for product publications and working in a large systems diagnostics group. Mr Lynch attended the University of Florida.

Data streaming

Data streaming, an extension to the base I/O interface definition, is the solution to these problems. It uses only the base unidirectional *bus in* and *bus out*, along with four tag lines—*service in, service out, data in*, and *data out*. In addition, data streaming can achieve a 3M-byte/s data transfer rate at distances up to 400′ (122 m). Thus, data streaming is a compatible extension of the base I/O interface, and allows the intermixing of both old devices and new devices that use data streaming I/O techniques.

The initial selection sequence performed by a data streaming device is the same as that for a conventional device. However, once the device using data streaming has been given a command, it is up to the device to signal how it wants to transfer the data (either the standard way or via data streaming). This intention is signaled by whichever tag (*data in* or *service in*) is raised first. If the device initiates data transfer by raising *data in* first, the data transfer proceeds using data streaming.

When data streaming is used, the rise and fall of *data in* or *service in* is independent of the rise and fall of *data out* or *service out*. Thus, in effect, the tag lines become clock pulses, with *service in* and *data in* that have an uptime or downtime not less than 270 ns. *Service out* and *data out* are required to have an uptime or downtime not less than 180 ns (See the Figure).

During an operation that transfers data to the channel, data must be valid on *bus in* from 22.5 ns after the rise of *service in* or *data in* until 247.5 ns (or more) after the rise of *service in* or *data in*. The channel does not generate the corresponding *service out* or *data out* until after the channel has accepted the corresponding byte of data from *bus in*.

Protocols

When the project to incorporate data streaming in the I/O interface was inaugurated several years ago, the capabilities of the I/O interface were those that have since been standardized by the U.S. Government. The definition contained the base I/O interface, which consisted of two 20-wire cables and included two pairs of tag lines for the control of data transfer.

The first tag pair is standard and consists of *service in* and *service out* lines. The second tag pair, which consists of *data in* and *data out*, is provided by the high speed transfer feature. An additional 24-wire cable is provided by the bus extension feature. When *service in* and *service out* or *data in* and *data out* tags are used, each pair of tags controls the validity of 1 byte of data on one of two unidirectional buses between the channel and the selected I/O device. Tag lines are interlocked on both the rise and fall of the signals.

The bus extension feature consists mainly of two additional unidirectional buses, one in and one out, that are used in parallel with the corresponding unidirectional buses contained in the base I/O interface. Thus, the tag pairs *service in, service out* or *data in, data out* (when the high speed transfer feature is used) can control the transfer of up to 2 bytes of data at a time.

Once a device is selected and a connection has been established, the device controls the beginning of data transfer. To transfer a byte of data to the channel (read operation), the device places the data on *bus in* and raises the tag *service in*. When the channel detects the rise of *service in*, it samples the data on *bus in* and, after accepting it, raises the tag *service out*. Similarly, when the device detects the rise of *service out*, it removes the data from *bus in* and drops *service in*. When the channel detects the fall of *service in*, it drops *service out*. The device can send another byte, if it has one, after it detects the fall of *service out*.

When transferring data to the device (write operation), the device raises *service in* when it is ready to receive a byte of data. The tag sequence is identical to that of the read operation; however, data are transferred on *bus out* and presence of data is indicated by the rise of *service out* and the fall of *service in*.

The high speed transfer feature controls the transfer of a byte of data over the same bus, used in conjunction with *service in* and *service out*. To prevent an overlap of data being transferred with *service in* and *service out*, the rise of *data in* is interlocked with the absence of the corresponding *out* tag (*data out*) and the rise of the opposite *out* tag (*service out*). Thus, the rise of one tag pair is overlapped with the fall of the other tag pair. Therefore, with the addition of *data in* and *data out*, a byte of data is transferred every two transitions on the interface, whereas before the addition, it took four transitions by using just *service in* and *service out*.

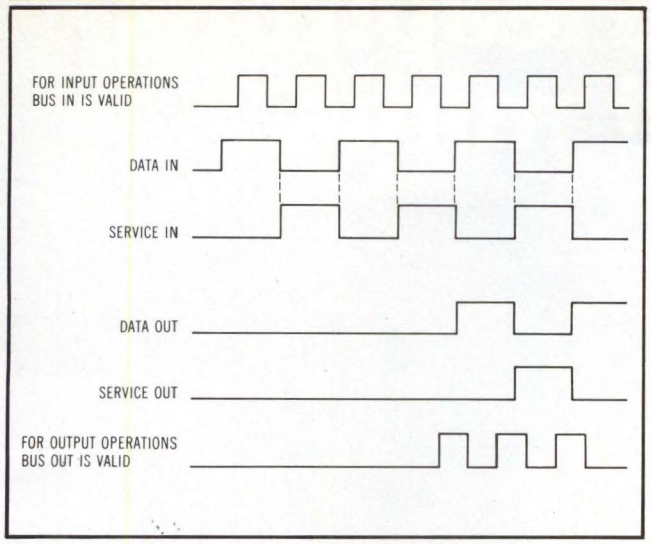
As distances increase, the data transfer capability decreases. Because of this, some IBM devices have elected to deviate from the full interlock protocol for data transfer under special conditions. The offset interlock protocol is the resulting scheme. When a device uses the offset interlock protocol, it drops *service in* or *data in* after a predetermined time, even if the corresponding *out* tag response has not been received yet. Duration of *service in* or *data in* is determined by the data transfer ability of the device, as well as the data transfer rate of the channel to which it is attached. The result is that the duration of *service in* or *data in* is not much greater than it would be if the device were attached to the channel with zero interface length.

To the channel, the operation appears to be a normal interlock protocol with a short interface length. Because the channel is unaware that the device drops *service in* or *data in* before the device sees the channel's corresponding *out* tag response, some problems are encountered when a device uses the offset interlock protocol. Since each channel established varies the amount of time it takes to respond to a request for data service, response can become so small that there is no assurance of being able to correctly sample the data from the appropriate bus. In extreme cases, the corresponding *out* tag response may never occur.

Another problem occurs when the channel prematurely ends the operation by responding with *command out* (stop) to either *service in* or *data in*. After signaling stop, the next tag that the channel sees would normally be *status in*. However, when the offset interlock protocol is used, the channel can receive an extra *service in* or *data in*. After signaling stop, the response to receiving the extra tags depends upon the channel implementation. The response can vary, from declaring an error, to responding with the corresponding tag, to no response at all, to again signaling stop by responding with *command out*.

During data transfers, the channel ensures that the data byte is valid on *bus out* 100 ns before the rise of the corresponding *out* tag, and until at least 100 ns after the rise of the corresponding *out* tag. When the channel does not respond in time to a preceding request for service, an overrun condition occurs that must be detected.

Because of the requirement to intermix both devices that are capable of data streaming and those that are not, the channel must contain some internal knowledge that the connected device is capable of transferring data with the data streaming feature. Definitions of both *service in* and *data in* existed before the data streaming feature; when both were in use, there were no restrictions on which one was to be raised first. The knowledge is necessary because the channel must react differently to channel overrun situations if it is transferring data by data streaming. When the channel detects that the device is overrunning the channel, the channel freezes and no longer responds to the device. This forces the device to detect an overrun and gives the device the option either to invoke command retry or to terminate the operation for software intervention.



Data streaming tag timing. ***In*** **tags operate independently of** ***out*** **tags and are, in effect, clock pulses.**

When the channel prematurely ends the operation by responding with *command out* to either *service in* or *data in*, additional *service in* or *data in* signals may, because of propagation delay, be received by the channel. Each such signal is responded to by the appropriate *service out* or *data out*. The total number of channel responses equals the number of I/O requests. If they are not identical, the device recognizes an error.

Once the interlocking of the tag lines is no longer part of the data transfer definition, other characteristics become of greater significance in limiting the maximum distance at which a 3M-byte/s transfer rate can be accomplished. Since the feature is compatible with the base I/O interface, the total amount of resistance handled by the drivers and receivers remains the same. This imposes a maximum limit on the length of interface cable that can be handled by the driver.

In addition, skew also becomes significant. Skew, a distortion in time of two or more signals generated simultaneously, results from a variation in the turn on and turn off speed of the drivers and receivers, as well as from a variation in the propagation time between the bus conductors. Thus, even if it is possible to simultaneously turn on all the drivers of the bus used to transfer data, the transitions do not arrive simultaneously at the receivers. Because it determines the minimum size pulse that can be sent on the different conductors that make up the bus, skew becomes another limiting factor.

Conclusion

The data streaming feature is an example of how the IBM System/360 and System/370 I/O interface has been changed to improve performance. As with previous changes to the I/O interface, the addition of the data streaming feature enables the interface to remain compatible with existing devices.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

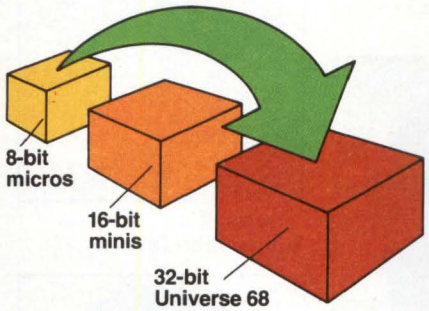
High 725 *Average 726* *Low 727*

Universe 68 leapfrogs the 16-bit minis.

CHARLES RIVER
DATA SYSTEMS

Introducing the first 32-bit supermicro for OEMs

Our new Universe 68 computer system offers powerful 32-bit architecture, a microcomputer price, the programming efficiency and portability of a UNIX-like operating system, and the refreshing experience of working with a computer supplier whose business practices are actually designed to make life easier for OEMs.



Jumping over outmoded 16-bit architecture

Built around the Motorola 68000 microprocessor, the Universe 68 system is a 32-bit supermicro that leapfrogs conventional 16-bit minicomputer technology. It has directly addressable, non-segmented address space of 16 million bytes, compared to the 64-kbyte limitation imposed by 16-bit architectures.

That means greater functionality per dollar, increased program development efficiency, and power to tackle demanding new applications.

The Universe 68/10 computer system

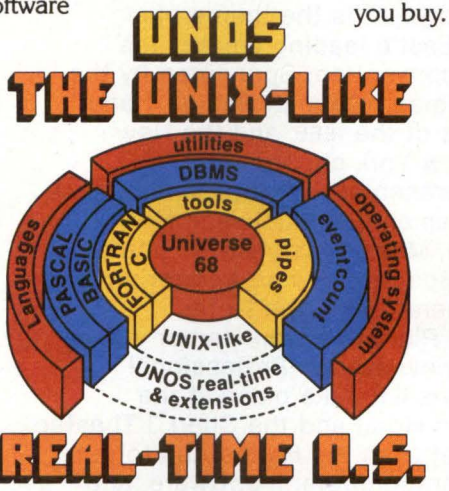
Outhopping supermini prices

The Universe 68 gives you 32-bit performance at micro prices – –while the big frogs in the minicomputer pond are still offering 32-bit technology only in expensive "superminis." A Universe 68/10 with 32-bit processor, 256 kbytes of memory, floppy disk, and Winchester disk sells for under $20,000. Order ten, and the unit price drops to $16,860, including system software.

Springing past conventional system software

UNOS, our UNIX-like operating system, is part of the new generation of more flexible, easier to use software written in the high-level systems programming language C. To help OEMs develop products faster and less expensively, it incorporates UNIX features (such as "pipes," I/O redirection, and hierarchical files), plus portability that conventional systems software can't match.

To its UNIX-like base, which supports FORTRAN and C languages, UNOS adds PASCAL and BASIC, an expanded data base management system (DBMS), and an array of run-time oriented, real-time transaction processing capabilities, including a highly sophisticated "Eventcount" process synchronization mechanism. These extensions can be the key to implementing real-time and information systems applications.



Croaking obsolete business practices

OEMs often find computer suppliers tough to deal with. Bundled hardware and software limit flexibility in configuring systems, while proprietary busses and assembly-language software can lock you in to one vendor.

We're out to change all that by offering OEMs a choice. You can buy complete systems from us, and just add application software. Or buy some components from us, and go elsewhere for others. You can even buy UNOS from us and run it on someone else's hardware. And by building the Universe 68 computer around standard, non-proprietary technology like VERSAbus, SASI bus, and the 68000, we've made second-sourcing easy.

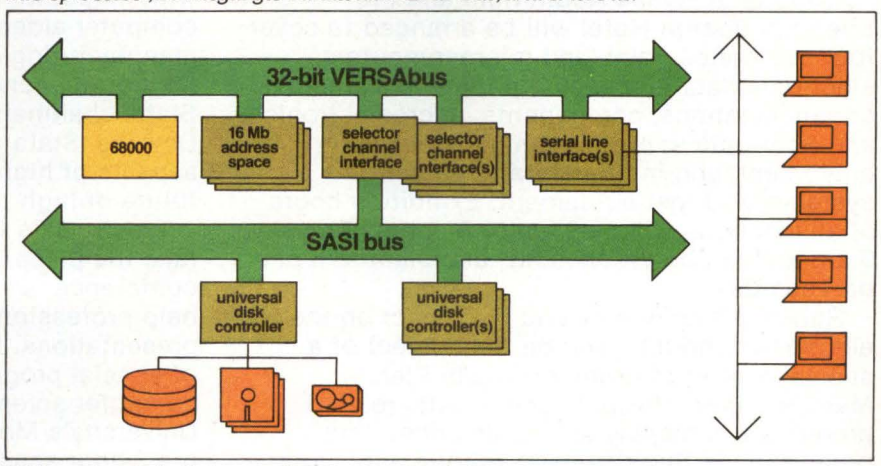
We've also introduced a more sensible approach to discounts. We give you discount credit for everything you buy. Our software discounts are based on how many licenses you buy, not in one year, but over *twenty* years. And they cut deep – all the way to 98%. We think this honestly reflects our costs: software development costs are almost entirely loaded at the front end, and support costs fall quickly once an OEM has gained experience.

Swallowing up the competition

If you need 32-bit power at a micro price and you can't wait for the minicomputer giants, you should know more about the Universe 68 computer and UNOS. For full information, call or write Charles River Data Systems, 4 Tech Circle, Natick, MA 01760, (617) 655-1800.

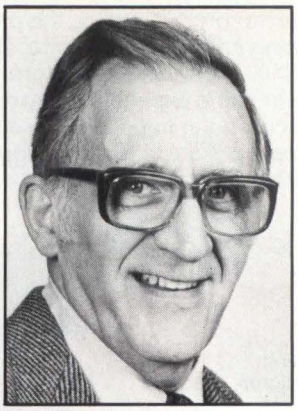
With the price/performance story we have to tell, we're ready to make a megasplash in the minipond.

The Universe 68 system takes advantage of standard building blocks, such as the 68000 microprocessor, 20-megabyte-bandwidth VERSAbus, and SASI bus.

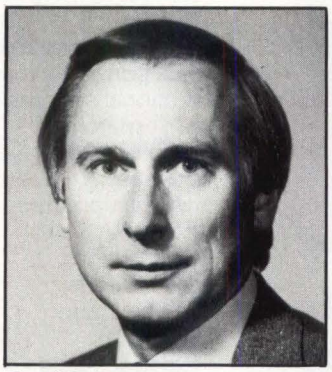


Electro/82

Electronic Show & Convention
Boston, MA
May 25 – 27, 1982



Ted Saad
Convention Director



Ray Stata
Keynote Speaker

Chuck Evans
Professional Program
Chairman

"Electronics Frontier" is the theme of Electro/82, the East's leading electronics exhibition and convention. Sponsored by the Central New England Council Region 1 and METSAC sections of the IEEE, and the New England and New York chapters of the Electronics Representatives Association (ERA), Electro alternates annually between New York, NY, and Boston, Mass. This year the conference will be held at Boston's Hynes Auditorium and the adjacent Sheraton-Boston Hotel. Commonwealth Pier at Boston Harbor will be the site for preview events. Professional Program sessions will take place at the Sheraton-Boston Hotel and the Cheri 3 Theater across the street from the Hynes Auditorium.

Exploring microcomputers, software, and careers, in particular, the Professional Program will reflect the scope and interest of engineering disciplines in New England's electronics industry. Rather than a highly specialized conference, however, Electro is mainly a "tutorial overview of technical disciplines needed by professionals in the region," according to Charles Evans of Teradyne, chairman of the Professional Program committee. Presentations concerning research, medical electronics, robotics, and speech recognition, as well as energy, memory, and gate arrays, have been planned. Professional Program sessions are scheduled in groups at 9:30 am, 1 pm, and 4 pm.

Exhibits at Hynes Auditorium and the Sheraton-Boston Hotel will be arranged to cover four categories: mini- and microcomputers, electronic data processing peripherals, and data communications; components, microelectronics, and fiber optics; production and packaging equipment; and instrumentation, control systems, and test equipment. Exhibition hours at all locations will be 9 am to 6 pm on Tuesday, 9 am to 7 pm on Wednesday, and 9 am to 5 pm on Thursday.

Robotics technology and its impact on the electronics industry will be the subject of a special exhibit at Commonwealth Pier. Manufacturers of robots and robotic-related products will display alongside consulting organizations that deal with robotic applications. Use of Commonwealth Pier for Electro/82 signals the start of an 18-month project that will convert the Pier into BOSCOM, a $100 million marketing center for high technology.

Preconvention activities taking place on Monday, May 24, include a conference on professional communications; a 2-day workshop on the application of technology forecasting methods; and three tutorial seminars dealing with industrial robots, local area networks, and computer aided design/computer aided manufacturing (CAD/CAM) graphics. Electro/82's Keynote Luncheon on Monday will feature Ray Stata, chairman and president of Analog Devices. Stata will address the economic aspects of high technology companies and the future of high technology in the Northeast.

Electro/82's Communications Conference will take the place of the traditional marketing conference, and present a program planned to help professionals improve their oral presentations. Dr Nicholas Washenko, director of special programs and chairman of the computer science department at Boston University's Metropolitan College, will present the 3-hour session, which begins at 8:30 am on

(continued on page 174)

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You *can* have it all! Along with the benefits of your DEC computer, you can get interface products that significantly extend the capability, flexibility and economy of DEC systems. MDB makes more DEC system boards than any independent manufacturer—some with plain vanilla compatibility; others with plain incredible performance boosting features. For example—

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- PROM memory modules, some with an on-board PROM programmer.
- General purpose interface and bus foundation modules.
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- LSI-11 system boxes with 22-bit addressing and switching power supplies.

In addition to the DEC compatible products, MDB also manufactures comparable interfaces for Data General, Perkin-Elmer, Intel and IBM Series/1 computers. All MDB products are available under GSA contract #GS-00C-02851.

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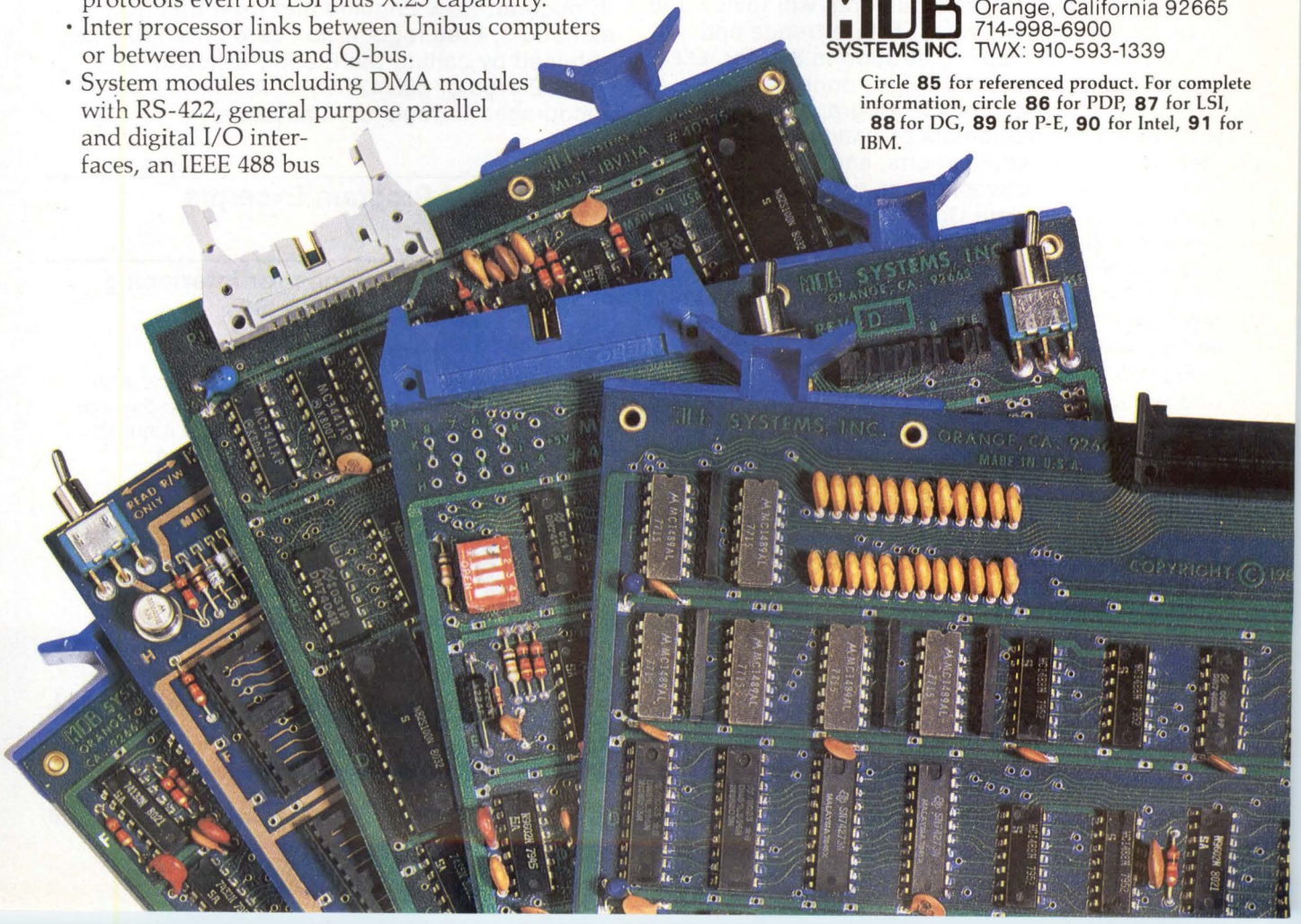
Circle **85** for referenced product. For complete information, circle **86** for PDP, **87** for LSI, **88** for DG, **89** for P-E, **90** for Intel, **91** for IBM.



Monday, May 24. Registration for the conference and Keynote Luncheon, both at the Park Plaza Hotel, is $35. If purchased separately, tickets for each event are $20. Tickets are available from the Electro office, 999 N Sepulveda Blvd, El Segundo, CA 90245.

Technology Forecasting workshop will pursue principles and techniques in an interactive training session held on Sunday and Monday. Participants will develop several technology forecasting methodologies, and consider technology forecasting as a management tool in research, performance goals, timing of new product releases, and early-warning signals. The special-fee workshop will begin at 8:30 am each day. Registration is $325 and is available through the Electro office.

Boston's section of the IEEE will present three extra-fee tutorial workshops at the Sheraton-Boston on Monday. These seminars will deal with industrial robots, local area networks, and CAD/CAM graphics. As organizer of the first session, concerning industrial robots, Hriday R. Prasad of Ford Motor Co, Dearborn, Mich, will discuss the fundamentals of robot technology, then focus on robotics applications and limitations. Advance registration is $125 for IEEE and ERA members and $155 for nonmembers.

Local area networks capable of providing high speed data transmission in a small geographic area will be examined in the second tutorial, coordinated by Joseph M. Erbacher of Prime Computer, Inc, Framingham, Mass. Five authorities on local area networks will review the state of the art and project future trends and challenges. Advance registration is $90 for IEEE and ERA members and $140 for nonmembers.

The third tutorial, a CAD/CAM graphics seminar, will present fundamentals of CAD/CAM graphics technology, and applications, and review historical perspectives. Organized by Walter M. Anderson of Lexidata Corp, Billerica, Mass, the session will discuss user options from do-it-yourself and integration of hardware and software to a complete turnkey system. Advance registration is $100 for IEEE and ERA members and $130 for nonmembers.

Electro/82's All-Industry Reception, the traditional opening night cocktail party, will salute Boston's historic past. Colonial New England will pervade the atmosphere at the Sheraton-Boston Hotel. Hors d'oeuvres, cocktails, beer, wine, soft drinks, and entertainment are planned for the festivity. Tickets for Tuesday's party are $15 each, and will be available at the door.

An international business center at the Sheraton-Boston will host foreign guests and provide complimentary registration. Electro/82 has been named to the U.S. Department of Commerce Foreign Buyer Program. Boston's District Commerce office is organizing a program that is geared to help developing nations enter the electronics market. Basic export strategies will be suggested and a panel workshop will deal with stringent new controls on export licensing. Wednesday, May 26, has been named "International Day," and will feature a seminar on import and export opportunities.

Electro Film Theaters will screen a series of scientific and technological motion pictures produced by universities, government agencies, corporations, and independent filmmakers. Films will be shown twice daily at Commonwealth Pier and the Sheraton-Boston complex; the program will be the same at both locations.

Each day of the convention free-fare shuttle buses will operate regularly 30 minutes before opening to one-half hour after closing between Commonwealth Pier and the Hynes Auditorium, Sheraton-Boston Hotel, and Cheri Theater complex. Buses will pick up and deposit passengers in front of the Commonwealth Pier and at the entrance of Hynes Auditorium. Buses also will link Commonwealth Pier with free parking lots along Route 128 in suburban Burlington and Natick beginning at 8:30 am each day. Last buses back to the suburbs will depart from Commonwealth Pier 30 minutes after closing each day.

Registration

At-door registration will be $10 for IEEE and ERA members and $20 for nonmembers. Complimentary registration cards are available from engineers at many electronics facilities throughout New England and from Electro exhibitors. Free registration cards may also be obtained by calling the Electro office at 617/232-4193 or 800/421-6816. Attendees are encouraged to register in advance.

Professional Program Excerpts

Session 1: Logic Designs for Interfacing Systems in the '80s

Tues 9:30 to 11:30 am

Advanced technology for interfacing systems with peripherals via high speed, low power logic designs will be considered. Speakers will conduct a question and answer period at the end of the session.

Chairman: S. Craig, Motorola, Inc

1/1 "Interfacing Enters a New Generation"
J. Binneboese, Motorola, Inc

1/2 "High Speed CMOS Logic: The Technology of the Future"
L. Wakeman, National Semiconductor

1/3 "CMOS Technology in Microprocessor Interface"
R. Broomfield, Mitel Semiconductor

1/4 "Using Complex Bipolar Functions in Interfacing Microprocessors"
D. Guzeman, Signetics Corp

1/5 "Advanced Schottky Logic Families from TI"
B. Stehlin, Texas Instruments, Inc

(continued on page 176)

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CIRCLE 92

Session 5: Managing New Design Processes in the Changing Design Environment of the '80s

Tues 1 to 3 pm

Designers and workers must adapt to an environment that will change dramatically over the coming decade. Emerging tools and techniques that will alter fundamental design and development processes will be the subject of this session.

Chairman: G. Rhine, Tektronix, Inc

5/1 "Computer aided Engineering: Do You Have a Choice?"
T. H. Bruggere, Mentor Graphics Corp

5/2 "ZyP: A New CAD System Based on Standard Cells for VLSI Design"
W. Loesch, Zymos Corp

5/3 "The Impact of Gate Arrays on the Design Process"
T. Miller, Texas Instruments, Inc

5/4 "Creatively Managing the Future Design Environment"
J. Yesenofski, Tektronix, Inc

Session 6: CMOS Fulfills Designer's Requirements for Low Power A-D Conversion

Tues 1 to 3 pm

New generation CMOS A-D converters are more versatile than before. Speakers will address application of CMOS in low power A-D conversion products.

Chairman: R. W. Haller, Analog Devices Semiconductor

6/1 "A 10-Bit Plus Sign A-D Converter"
J. Whitmore, Analog Devices BV

6/2 "Low Power A-D Conversion Applications"
L. Sherman, National Semiconductor

6/3 "Low Power High Resolution A-D Conversion for High Reliability Applications"
S. Wilensky, Hybrid Systems, Inc

6/4 "New CMOS A-D Converter"
A. Alaspa, Motorola, Inc

6/5 "A Monolithic 14-Bit 20-μs A-D Converter"
S. Sokolov, Intersil

Session 7: Display Devices and Systems

Tues 1 to 3 pm

Four areas of display technology will be presented: penetration CRTs for high resolution color graphics; large information content liquid crystal matrix displays; plasma panels, including trends in multicolor displays, high resolution and processing displays, and reduced drive electronics costs; and consumer, industrial, and military projection displays, including CRTs, laser-addressed liquid crystals, and light valves.

Chairman: L. T. Todd, Jr, Univ of Kentucky

7/1 "Review of Penetration CRT Technology"
G. R. Spencer, Raytheon Co

7/2 "Liquid Crystal Matrix Displays"
D. E. Castleberry, General Electric Co

7/3 "Plasma Displays"
L. F. Weber, Univ of Illinois

7/4 "Projection Display Devices and Systems"
L. T. Todd, Jr, Univ of Kentucky

Session 9: The Gate Array Approach to Circuit Design

Tues 4 to 6 pm

CAD and VLSI technologies in logic array design applications in many cases have supplanted the need for fully customized circuits or multichip designs. Simulation, auto routing, test pattern generation, and other software tools can combine with state of the art CMOS and bipolar cell layouts to integrate up to 5000-gate densities. Fast design turnaround and low volume production runs make the logic array approach widely available.

Chairman: P. Richmond, Mitel Semiconductor

9/1 "From Logic Design to Silicon"
J. Kroeger, International Microcircuits, Inc

9/2 "ISO-CMOS in High Speed/Low Power Logic Array Applications"
B. Broomfield, Mitel Semiconductor

9/3 "Converting SSI/MSI and PLA Designs to CMOS Logic Arrays"
R. Walker, R. Derickson, and K. Lobo, LSI Logic Corp

9/4 "Designing through Bipolar Logic Arrays"
T. Chambers, Texas Instruments, Inc

9/5 "A CMOS Gate Array Development"
C. Hardage, California Devices, Inc

Session 10: Linear in the '80s

Tues 4 to 6 pm

Linear design and component testing that will characterize future system design techniques will be described. Assumptions inherent in a linear test system and how they depart from actual component performance will be considered.

Chairman: T. J. Schwartz, Precision Monolithics, Inc

10/1 "IC Op Amp Combines Lowest Noise Performance Available with Precision and High Speed"
S. Bernardi, W. Jung, G. Erdi, and T. J. Schwartz, Precision Monolithics, Inc

10/2 "New Design Techniques Yield Very High Speed Bipolar 6- and 8-Bit A-Ds"
B. Gillings, Advanced Micro Devices

10/3 "Achieving the Impossible—Systems Level Linear ICs"
L. Counts, Analog Devices Semiconductor

10/4 "A Microprocessor Based Servo Loop Controller"
L. Hadley, G. Riehm, and S. Ohr, Signetics Corp

Session 11: Speech Recognition, Generation, and Synthesis

Tues 4 to 6 pm

Higher quality electronic speech, smaller memory size requirements, and single-chip generation in compact, reliable systems are in demand. Speech recognition, generation, compression, and synthesis techniques from both system level and chip perspectives will be observed.

(continued on page 178)

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Design Tomorrow into your system. The Sapphire 160 is a 160 megabyte, high density 14-inch Winchester drive, with SMD compatible interface. Simplicity of design and advanced technology give you much more for less than any comparable unit.

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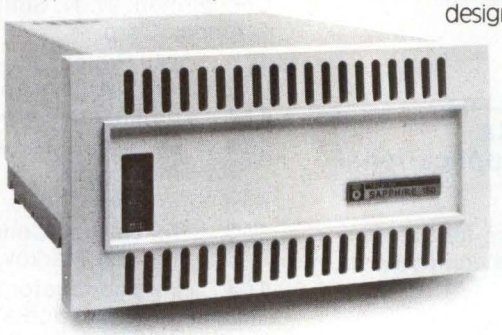

Less danger of head damage during transport. Because manual locks are so frequently neglected, a unique positioner solenoid lock automatically locks heads and disks in position whenever the power is off. Smaller size and weight make handling less cumbersome.

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CIRCLE 93

Chairman: J. J. Farrell III, Motorola, Inc

11/1 "Perceptual Issues in Speech Recognition"
T. A. Williams, Motorola, Inc

11/2 "High Quality Realtime Text to Speech Synthesis"
D. Gilblom, Telesensory Speech Systems

11/3 "A Speech Development System"
F. Wickersham, National Semiconductor

11/4 "Single-Chip Speech Synthesizer"
P. McLaughin, General Instrument

11/5 "Low Cost Voice Recognition Systems"
S. Viglione, Interstate Electronics

Session 12: Application of and Design Requirements for emi/rfi Test Equipment

Tues 4 to 6 pm

New government regulations call for specific testing and/or type approvals to verify that electrical and electronic equipment under test fulfills national and international standards for emi/rfi performance. Speakers will explain testing requirements and discuss specific rules that apply in particular countries, and within what frequency ranges; difference between radiated and conducted interference; evaluation of an actual test site; technical requirements for proper test equipment; and aspects of susceptibility.

Chairman: U. L. Rohde, Communications Consulting Corp

12/1 "EMI/RFI Testing Requirements per FCC, FTZ/VDE, and Military Standards"
H. J. Levine, Rhode & Schwarz

12/2 "Required Dynamic Range and Design Guides for emi/rfi Test Receivers"
U. L. Rohde, Communications Consulting Corp

12/3 "Measurement of Radiated Electromagnetic Emissions from Digital Devices"
S. Bennett, Hewlett-Packard Co

12/4 "Susceptibility of Electrical Instruments to rf Voltages
R. Woolhiser, Tektronix, Inc

12/5 "The Origins, the Effects, and the Simulation of Transients, as well as their International Standardization"
O. Frey, Emile Haefely & Co, Ltd

Session 13: IC Solutions for Data Communications Applications

Wed 9:30 to 11:30 am

Sophisticated LSI and VLSI peripheral ICs for data communications will be discussed and applications considered.

Chairman: A. Goldberger, Signetics Corp

13/1 "LSI Data Communications Devices for Special Applications"
G. Leger, Western Digital Corp

13/2 "High Integration LSI for Low Cost Asynchronous Communications"
C. Yager, Intel Corp

13/3 "Advanced ICs for Data Communications Applications"
S. Walters, Zilog, Inc

13/4 "New Datacomm ICs for the 68k Family"
J. Yarborough, Signetics Corp

13/5 "What's Wrong with LSI Datacomm Controllers—A User's Perspective"
A. Weissberger, Sr, Memorex

Session 14: Master/Slave Distributed Processing Systems

Wed 9:30 to 11:30 am

Slave microcontrollers and microprocessors, used in custom peripheral and intelligent subsystem control, offer control algorithm flexibility, distributed intelligence that offloads the CPU, and simple multiprocessor system architecture. New components and system architectures will be reviewed in this session, which will be informative for designers of microprocessor systems and peripheral controllers.

Chairman: P. Madan, Intel Corp

14/1 "Tightly and Loosely Coupled Master/Slave Distributed Processing Architectures"
P. Madan, Intel Corp

14/2 "Zilog Z8090 UPC—A High Performance Slave Peripheral Controller"
R. Perry, Zilog, Inc

14/3 "Programmable Solution for Distributed Peripheral Control in the NS16000 Family"
B. Gee, National Semiconductor

14/4 "Microprogrammable Slave Processor for Flexible Distributed Control"
K. S. Padda, Texas Instruments, Inc

14/5 "Intelligent Terminal Design on the 68000 Bus Using 68120 Slave Processor"
K. Livingston, Motorola, Inc

Session 17: Token Access Protocols

Wed 1 to 3 pm

Local area networks connect diverse company functions into an integrated information system. Session will open with a report on the status of the IEEE 802 network standards committee, followed by a detailed description of token access protocols and applications.

Cochairmen: W. N. Smith, Sytek Corp and D. Sze, Amdax Corp

17/1 "IEEE Project 802—Local Area Networking Standard—A Concept Status"
T. J. Harrison, IBM Corp

17/2 "Local Area Network—A Broadband Implementation"
I. Kong, Amdax Corp

17/3 "Token Ring Concepts for Local Area Networks"
R. Dixon and J. Markov, IBM Corp

17/4 "Semiconductor Encapsulation for Token Based Local Area Networks"
M. Stieglitz, Western Digital Corp

17/5 "Traffic Analysis Tools for Token Passing Distributed Polling Media Access Methods for Local Area Networks"
E. Arthurs and B. W. Stuck, Bell Labs

(continued on page 180)

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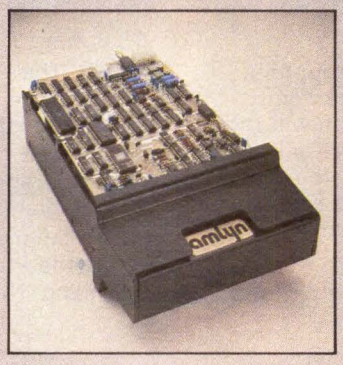

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CIRCLE 94

Session 18: New Microcomputer Numerics Solutions

Wed 1 to 3 pm

Advances in microcomputer numerics processing are allowing mathematical applications that previously were impossible—or impractical—for microprocessors. Cost/performance tradeoffs of selected microcomputer numerics implementations, ranging from firmware chips to floating point coprocessors, will be evaluated.

Chairman: B. Patterson, Intel Corp

18/1 "Broadening the Scope of Numerics Applications with the 8087 Numeric Processor Extension"
T. Zingale, Intel Corp

18/2 "Cost-Effective Numerical Computations in Microprocessors"
T. W. Starnes, Motorola, Inc

18/3 "Speed/Cost Tradeoffs of Using the TMS99110 Math Processor"
W. D. Hopkins, Texas Instruments, Inc

18/4 "Floating Point Processing with the Z8000"
D. Stevenson, Zilog, Inc

Session 21: CSMA/CD Protocols

Wed 4 to 6 pm

Local area networks provide an integrated information system for various company functions and office products. Session will cover carrier sense multiple access/collision detection (CSMA/CD) protocols and applications, concluding with a panel discussion on local area networks.

Cochairmen: W. N. Smith, Sytek Corp and D. Sze, Amdax Corp

21/1 "Local Area Network—A Broadband CSMA/CD Implementation"
J. Hunter, Sytek Corp

21/2 "Local Area Network—A CSMA/CD Implementation"
G. Hopkins, Ungerman-Bass

21/3 "VLSI Approach to Local Area Network CSMA/CD Controller"
J. Vi Hera, Mostek Corp

21/4 "Capacity of Ethernet"
B. Hawe and M. Marathe, Digital Equipment Corp

21/5 "Local Area Networks"
Panel: I. Kong, Amdax Corp; B. Stuck, Bell Labs; J. Hunter, Sytek Corp; and B. Hawe, Digital Equipment Corp

Session 22: Emerging Architectures for Digital Signal Processing

Wed 4 to 6 pm

Hardware parallelism is achieving high throughput with relatively low speed component subsystems. Architectural considerations in this session will focus on multiprocessor configurations. Speakers will address programmable LSI chips designed for signal processing, and partitioning of processing algorithms for use in parallel structures. One paper will describe a speech processing application of processor parallelism that uses currently available signal processing chips.

Chairman: T. Bially, MIT Lincoln Lab

22/1 "Partitioning Signal Processing Algorithms for Multiprocessor Architectures"
D. E. Dudgeon, MIT Lincoln Lab

22/2 "Optimal Implementation of Signal Flow Graphs on Synchronous Multiprocessors"
T. P. Barnwell and C. J. M. Hodges, Georgia Institute of Technology

22/3 "Some Design Considerations for Distributed Signal Processing Architectures"
J. M. Glass, Raytheon Co

22/4 "A Single-Chip Microcomputer Architecture Optimized for Signal Processing"
K. McDonough, Texas Instruments, Inc

22/5 "A Compact, Flexible LPC Vocoder Based on a Commercial Signal Processing Microcomputer"
J. A. Feldman, MIT Lincoln Lab

Session 23: Progress in Robotics and Automated Manufacturing

Wed 4 to 6 pm

Developments and applications for robotics and automated material handling systems, arc welding robotic systems, automated inspection systems, and related technologies will be presented.

Chairman: P. Villers, Automatix, Inc

23/1 "Cybervision: A System for Flexible Robotic Assembly"
G. Vander Brug, Automatix, Inc

23/2 "Automated Manufacturing/Integrated Systems"
L. J. Bradt, SI Handling Systems, Inc

23/3 "Designing Languages for Programming Manufacturing Cells"
D. A. Bourne and P. Fussell, Carnegie-Mellon Univ. Robotics Institute

23/4 "Improving Productivity through the Use of Robots and Group Technology"
A. Houtzeel, Organization for Industrial Research, Inc

23/5 "A 3-Robot Consight System"
M. Ward and J. Dunseth, General Motors Research Labs

23/6 "Robot Intelligence"
J. Justice, Productivity Systems, Inc

Session 25: Programming Single-Chip Microcomputers

Thurs 9:30 to 11:30 am

Program/programmer efficiency are important criteria in choosing single-chip microcomputers. Speakers will present state of the art microcomputer instruction sets, addressing modes, and other software considerations.

Chairman: J. Millar, Texas Instruments, Inc

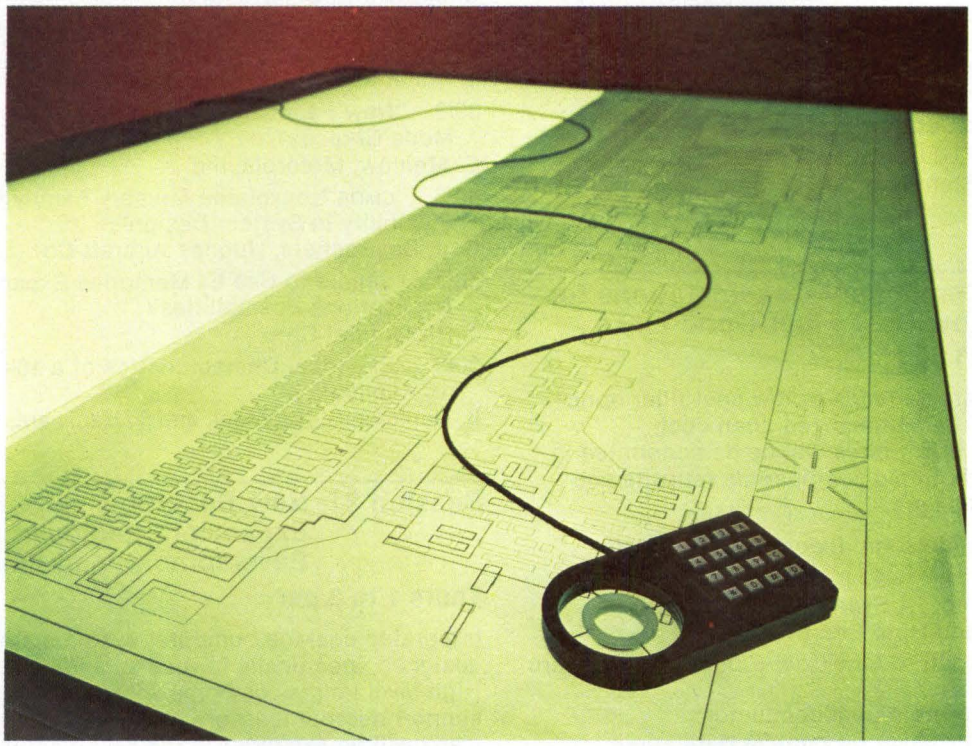
25/1 "The Programming Ease of the HMOS/CMOS M6805 Family"
J. A. Langan, Motorola, Inc

25/2 "The TMS 7000 Family: Programming and Microprogramming"
L. V. Kaplan, Texas Instruments, Inc

25/3 "Microprocessor Resident Tiny BASIC Interpreter Speeds Program Development"
J. Chiang, National Semiconductor

(continued on page 182)

Most digitizers are pretty much alike... the New CalComp 9000 Series is the exception.



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CIRCLE 95

25/4 "Fourth Generation Architecture Allows Performance of Larger Jobs with Smaller Programs"
J. Twardy, NEC Electronics, USA Inc

25/5 "Programming to Meet Time Critical Applications"
R. Dumse, Rockwell International

Session 26: Redundancy Considerations in High Density Memory Devices

Thurs 9:30 to 11:30 am

Redundancy may provide the answer for lowering cost per bit of semiconductor memory. Implications of onchip redundancy for user and vendor, especially testability and reliability considerations, will be discussed. Implementation of both laser and electrical redundancy techniques will be described.

Chairman: M. K. Phinney, Mostek Corp

26/1 "Laser Programmed Redundancy in Dynamic and Static RAMS"
R. T. Smith, Bell Labs

26/2 "Implementation of Onchip Redundancy Using Laser Fusing Techniques"
J. Flynn, Mostek Corp

26/3 "Testing Redundant Memories"
J. Altnether, B. Stenfland, and D. Champelin, Intel Corp

Session 27: Component Considerations for Low Cost Fiber Optic Links

Thurs 9:30 to 11:30 am

Performance characteristics of low cost fiber optic components will be summarized, then cost-effectiveness of fiber optics will be demonstrated in applications for both plug-compatible retrofits and optimized new designs.

Chairman: A. Mendelsohn, *Electronics Products Magazine*

27/1 "Fiber Optics, A Systems Approach"
J. Head, Honeywell Opto Electronics

27/2 "An Approach to Low Cost Fiber Optic Emitters and Detectors"
D. Stevenson, Motorola Semiconductor

27/3 "Low Cost Cables for Optical Data Links"
S. Minami, Mitsubishi Rayon Co

27/4 "A New Acrylic Core Fiber Optic Cable"
D. E. Willaeur, E. I. duPont deNemours & Co

27/5 "Semiautomatic Application of Low Cost Fiber Optic Connectors"
J. A. Leidy, AMP, Inc

27/6 "Fiber Optics Applications in Automobiles"
K. Sekiguchi, Nissan Motors

Session 29: More Single-Chip Microcomputer Advancements

Thurs 1 to 3 pm

Advances in single-chip microcomputer technology will be reviewed.

Chairman: E. Peatrowsky, Motorola, Inc

29/1 "The Economics of Offchip Peripherals"
T. Harper, National Semiconductor

29/2 "Self-Programmed Single Chips—The MC68705S"
B. Huston, Motorola, Inc

29/3 "Using Multiple One-Chip Computers"
R. Dumse, Rockwell International

29/4 "Versatile Microcomputers for the '80s"
J. Millar, Texas Instruments, Inc

29/5 "An Advanced Instruction Set Architecture for a High Performance Single-Chip Microcomputer"
D. Folkes, Mostek Corp

Session 30: New Nonvolatile Memory Features

Thurs 1 to 3 pm

Discussion of EEPROM and EAROM releases, as well as applications and features governing ease of use, will be highlighted by innovative system design opportunities.

Chairman: D. C. Ford, Motorola MOS Memory

30/1 "Design Innovations Reduce EEPROM Interfacing Requirements"
M. Kalet and E. Edwards, General Instrument Corp

30/2 "New Fast 32k EPROM Offers System Erase-Mode Choices"
C. Menlow, Motorola, Inc

30/3 "CMOS Nonvolatile Memory Family Offers Flexibility in System Design"
G. J. DesRochers, Hughes Aircraft Co

30/4 "Simple to Use E_2 Memories Expand Applications Possibilities"
J. Rizzo, Intel Corp

30/5 "Electrical Characteristics of a 16k EEPROM and its Application"
K. Uchiumi, S. Nacetani, and T. Hagiwara, Hitachi, Ltd

Session 31: New Desktop Computers Invite Expansion, Engineering Development, and Innovation

Thurs 1 to 3 pm

Integrated desktop computer systems are being designed specifically for use as engineering tools. High level languages come with the machines. All support microprocessors and operating systems, and many will be expanded via serial communications interfaces on proprietary buses.

Chairman: J. Holmgren, Data General Corp

31/1 "A Desktop Workstation Designed for Optimum Versatility"
D. Callan, Callan Data Systems

31/2 "The HP 9836 Offers Pascal Development Environment on a Desktop"
R. Ison, Hewlett-Packard Co

31/3 "The MPT/100 Technical Desktop Computer"
H. D. Bryce, Data General Corp

31/4 "Cromemco's Desktop Super Minicomputer
D. Rotow, Cromemco

(continued on page 184)

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CIRCLE 96

Session 32: Object Oriented Systems and Languages

Thurs 1 to 3 pm

Papers will present the history, purposes, and practical advantages of keeping data structures within computers, as both a hardware imposed constraint and a language oriented feature. Object oriented aspects of present and forthcoming languages, processors, and systems will be explained.

Chairman: B. Masnick, Hazeltine Corp

32/1 "Ada as an Object Oriented Language"
R. S. Freedman, Hazeltine Corp

32/2 "Object Oriented Systems and Provably Secure Operating Systems"
K. Levitt, Stanford Research International

32/3 "A History of Capability Based Machines"
H. Levy, Digital Equipment Corp

32/4 "Objects in Eden System"
G. Almes, Univ of Washington

Session 33: CMOS Microprocessor Systems

Thurs 4 to 6 pm

Key elements of CMOS microprocessors will be presented, along with peripheral, memory and logic IC, and interfacing techniques. Practicality of assembling a performance oriented multichip microprocessor system completely from low power CMOS components will be considered.

Chairman: B. Huston, Motorola, Inc

33/1 "A Commonsense Approach to Choosing CMOS Microprocessors"
P. Nyman, Conrac Corp

33/2 "New Peripherals Complement Friendly Architecture of CMOS CPU"
A. Wagner-Korne, National Semiconductor

33/3 "New Peripherals for CMOS Microprocessors"
E. Peatrowsky, Motorola, Inc

33/4 "1800 Series Multiprocessing for Maximum Performance"
D. Block, RCA Solid State Div

Session 34: LSI Memory Controllers: System Design Trends and Architectures

Thurs 4 to 6 pm

Information and analysis techniques helpful in determining memory design tradeoffs will be suggested. Dynamic RAM control and error correction will be considered for both add-on memory and microprocessor system memory.

Chairman: J. Vidal, Intel Corp

34/1 "The Rationale for Error Correction in Dynamic RAM Based Systems"
W. Miller and B. Threewitt, Advanced Micro Devices

34/2 "Microprocessor Oriented Dynamic RAM Controller"
B. May, Intel Corp

34/3 "High Performance Dynamic RAM Support Circuits"
C. Carinalli and M. Evans, National Semiconductor □

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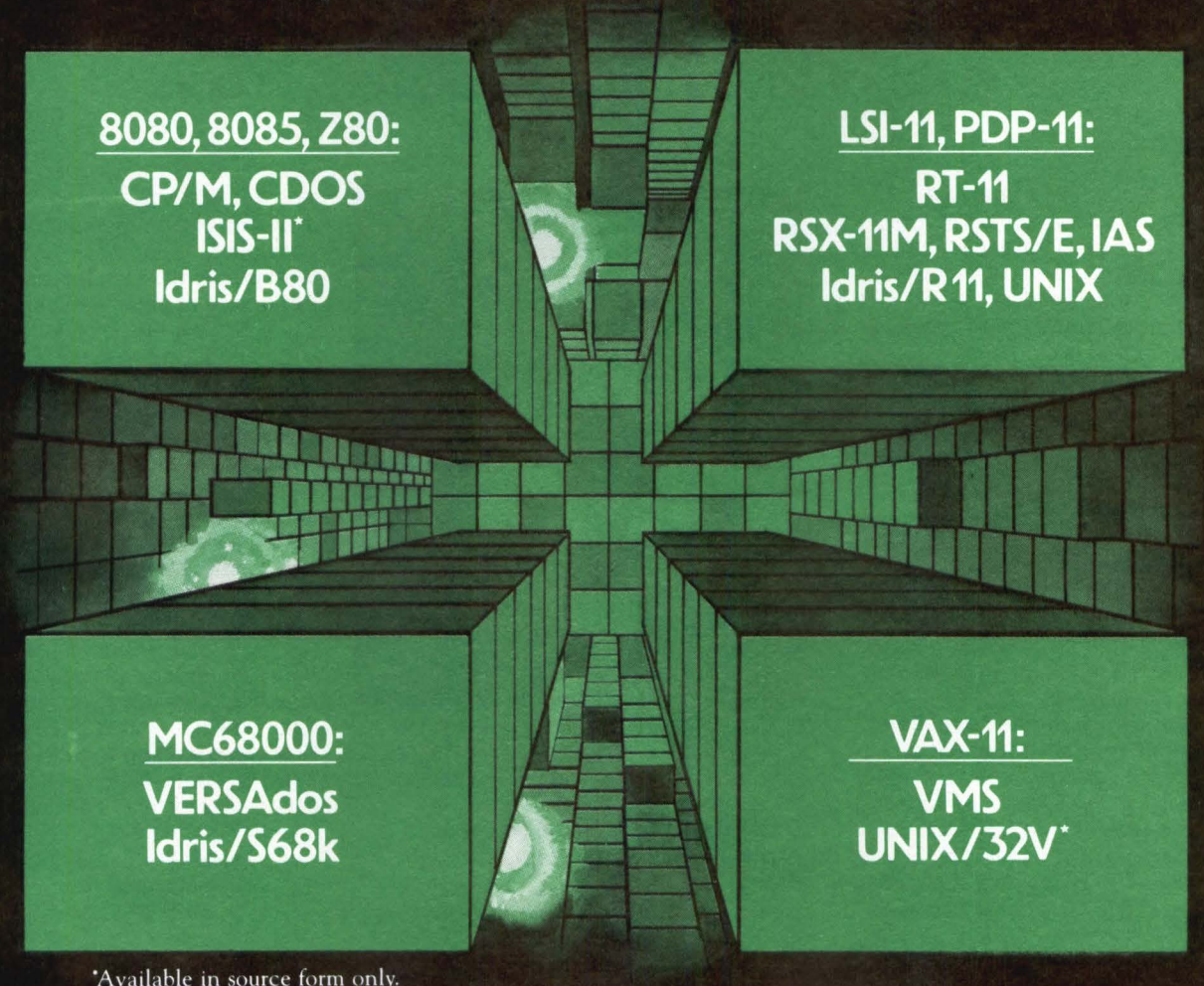

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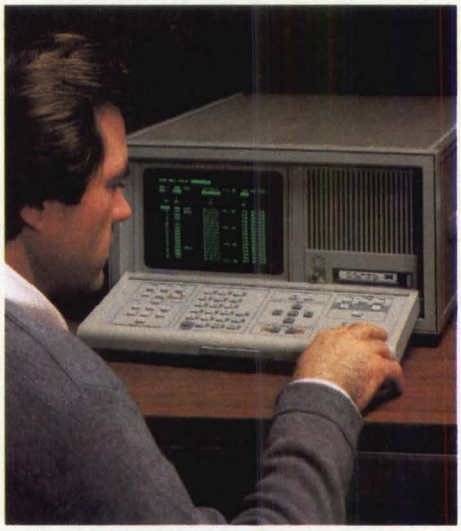

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Society for Information Display International Seminar and Symposium

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May 10 to 14, 1982

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Global progress in information display technology will be examined at SID '82, which will convene at the Town and Country Hotel, San Diego, Calif, on May 10 to 14. This year's Technical Program, covering 20 daytime sessions and three evening panels, will be presented by over 300 speakers from China, England, Finland, France, Germany, Japan, the Netherlands, Switzerland, and the United States. An international exhibition at the Town and Country Ballroom will highlight the latest developments in display technology. Exhibition hours will be Tuesday, 10 am to 5:30 pm; Wednesday, 9 am to 5 pm; and Thursday, 9 am to 1 pm.

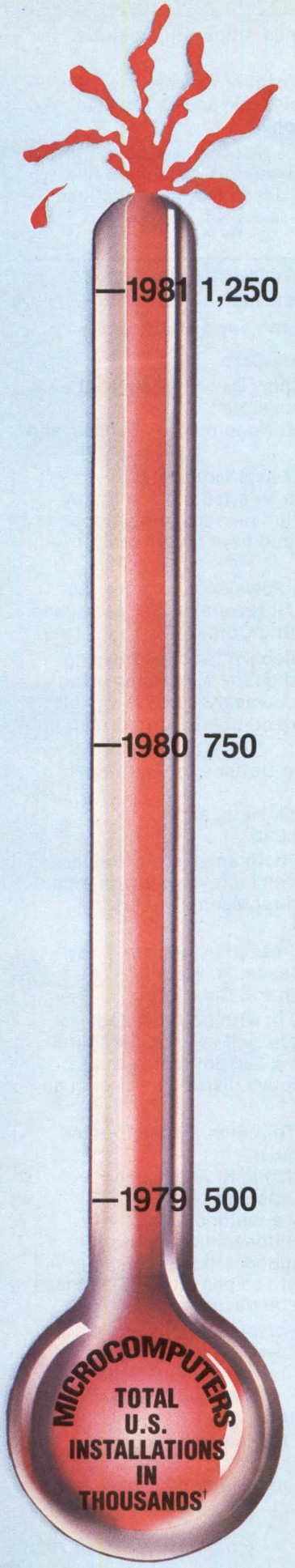
On Tuesday, the opening session of the Technical Program will feature Francis Ford Coppola. In the Keynote Address, "Electronic Cinema and Information Display," Coppola will review his experiments to develop the first all-electronic cinema at Zoetrope Studios in Hollywood, Calif. He will assess information display opportunities growing with the electronic cinema, along with advances in simultaneous display of script and picture information, high resolution computer graphics for special effects, and computerized systems for instant manipulation of text and picture content.

"Electronic Image Realism in Film Animation" will be the subject of Wednesday's Invited Luncheon address. Phillip S. Mittleman, president and chairman of Mathematical Applications Group, Inc, Elmsford, NY, will describe a CAD/CAM technology that creates 3-dimensional mathematical models of complex solid shapes—making it possible to calculate physical properties of the models and generate realistic, shaded pictures of nonexistent objects. Mittleman will explain applications of the process to animation, and how complex, 3-dimensional shapes can be modeled interactively.

A 2-day tutorial seminar will take place on the days immediately preceding and following the Technical Program. On Monday, May 10, four lecturers will evaluate major flat panel display technologies, and analyze the leading alternatives—plasma and thin film electroluminescent devices. On Friday, discussions will focus on users and applications. Speakers will explore how human factors influence the design and use of color displays and the man/machine interface, and assess display subsystem design and tradeoffs. A report on state of the art simulation technology, as applied to modern weapons systems, will conclude the talks.

Attendees may choose among Tuesday's three evening panel discussions. In the first, "Fatigue and Discomfort Associated with Visual Display Units," panelists will attempt to clarify issues regarding the effects of VDU design and use on operators, and review protective regulations spawned by concern for safety of VDU users. Participants in the second evening panel, "Large Screen Displays: Direct View vs Projection," will represent users and manufacturers of each

(continued on page 190)



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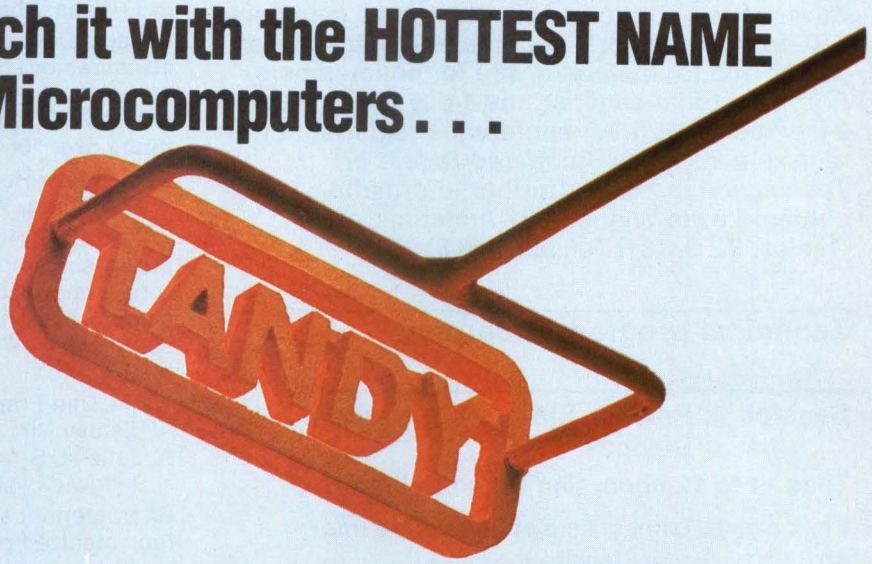

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CIRCLE 101

technology. How plasma and electroluminescent panels compete as viable alternatives will be argued by a panel of both plasma and electroluminescence advocates in the third evening session, "Plasma vs Electroluminescence." Both kinds of panels have similar structures; plasma is more established, but electroluminescence may offer higher luminous efficiency and brightness.

Author interviews planned after the Technical Program sessions on Tuesday, Wednesday, and Thursday will give attendees and speakers the opportunity to meet informally. On Tuesday, exhibitors will host a social hour in the Town and Country Ballroom.

Registration

Advance registration fee is $55 for SID members, $70 for nonmembers; at-conference registration will be $65 for members, $80 for nonmembers. For the tutorial seminar, the 1-day fee is $80; the 2-day fee is $125. All conference registrants will receive a 300-page illustrated *Digest of Technical Papers*. For further information, contact Lewis Winner, 301 Almeria, Coral Gables, FL 33134. Tel: 305/446-8193.

Technical program excerpts

Session 4: Powder Electroluminescent Devices

Tues 11 to 12 noon, San Diego Ballroom

Chairman: L. Tannas, Aerojet ElectroSystems

4/1 "DC EL Panel Stabilization"
A. Vecht and S. S. Chadha, Thames Polytechnic; and R. Hayes, Phosphor Products Co, Ltd

Report will cover application of interlayers; control and use of ambient and copper sulfide phases, yielding displays with 0.5% to 0.7% efficiency, 100 ft-L after 1000 h; and a reduction in forming power by a factor of 10.

4/2 "Characteristics of dc Electroluminescent Panel Under ac Operation"
L. Chou, X. Luo, and S. Xu, Changchun Institute of Physics

Referring to cells with luminance above 10 ft-L after 1000 h, speakers will describe frequency dependence of luminescence intensity, brightness waveforms, and other characteristics of dc electroluminescent powder panels driven by 50 Hz ac.

Session 6: Display Standards and Visual Fatigue

Tues 11 to 12 noon, California Ballroom

Chairman: T. Riley, Harris Corp

6/1 "Ergonomic Regulation: An Engineering View"
J. C. Greeson, Jr, IBM Corp

Potential health hazards have led to regulations governing display system design that can hinder the design process. Specific examples relating to character size and luminance ratios will illustrate several of these conflicts.

6/2 "Visual Fatigue and Display Viewing"
F. W. Umbach, J. W. H. Kalsbeek, and D. Bosman, Twente Univ of Technology

The human visual channel's resolving capacity for fatigue and a device that measures capacities of a visual environment will be described. Visual fatigue induced by VDT vs non-VDT tasks will be reported.

Session 7: Thin Film Transistor Arrays for LCD Addressing

Tues 1:50 to 5:10 pm, San Diego Ballroom

Chairman: A. Lakatos, Xerox Corp

7/1 "A Liquid Crystal Display Device Addressed by Tellurium Thin Film Transistors"
M. Matsuura, Y. Takafuji, K. Nonomura, F. Funada, and T. Wada, Sharp Corp

Speakers will describe a 17-segment/character, 10-character LCD addressed by a tellurium TFT array. TFTs use an evaporated tellurium semiconductor and anodized Ta_2O_5 insulator, and have on/off current ratios over 1000.

7/2 "Laser-Recrystallized Polysilicon TFTs for LCD"
T. Nishimura, Y. Akasaka, H. Nakata, K. Sugahara, and S. Ibuki, Mitsubishi Electric Corp

Laser-recrystallized polysilicon TFTs for addressing LCDs, constructed on fused quartz substrates using silicon LSI technology, will be analyzed. TFTs exhibit 50- to 150-cm^2/V-s mobility and on/off current ratio up to 10^5.

7/3 "Thin Film Polysilicon Devices for Flat Panel Display Circuitry"
A. Juliana, S. W. Depp, B. G. Huth, and T. O. Sedgwick, IBM Research Lab

Characteristics of TFTs, as both small grain and laser-recrystallized polysilicon, will be reviewed with regard to display applications and representative ICs in as-deposited polysilicon.

7/4 "Large Scale LCD Addressed by a-Si TFT Array"
Y. Okubo, T. Nakagiri, Y. Osada, M. Sugata, N. Kitahara, and H. Hatanaka, Canon, Inc

Stable operation over 1000 h, with both twisted nematic and guest host LCDs, will be evaluated for a transparent LCD with a 240- x 240-dot matrix over a 3.8″ x 3.8″ (9.7- x 9.7-cm) active display area using an a-Si TFT addressing array.

7/5 "Amorphous Silicon Thin Film Transistors for Liquid Crystal Display Panel"
S. Kawai, N. Takagi, T. Kodama, K. Asama, and S. Yanagisana, Fujitsu Labs, Ltd

Stable a-Si:H TFTs made by a method using SiO_2/a-Si:H/SiO_2 (gate insulator/semiconductor/passivator) continuous film deposition technology will be presented, and 5- x 7-dot LCD panel that uses these TFTs as a matrix driver will be described.

7/6 "Amorphous and Polycrystalline Silicon TFTs for Addressing Display Devices"
M. Le Contellec, F. Morin, J. Richard, P. Coissard, M. Morel, and M. Bonnel, Centre National d'Etudes des Telecommunications

Recrystallized silicon TFTs fabricated on a glass substrate will be characterized for off current, channel mobility, and switching speed. Method for making a 320- x 320-element, 4-element/mm a-Si:H TFT array will be explained.

(continued on page 192)

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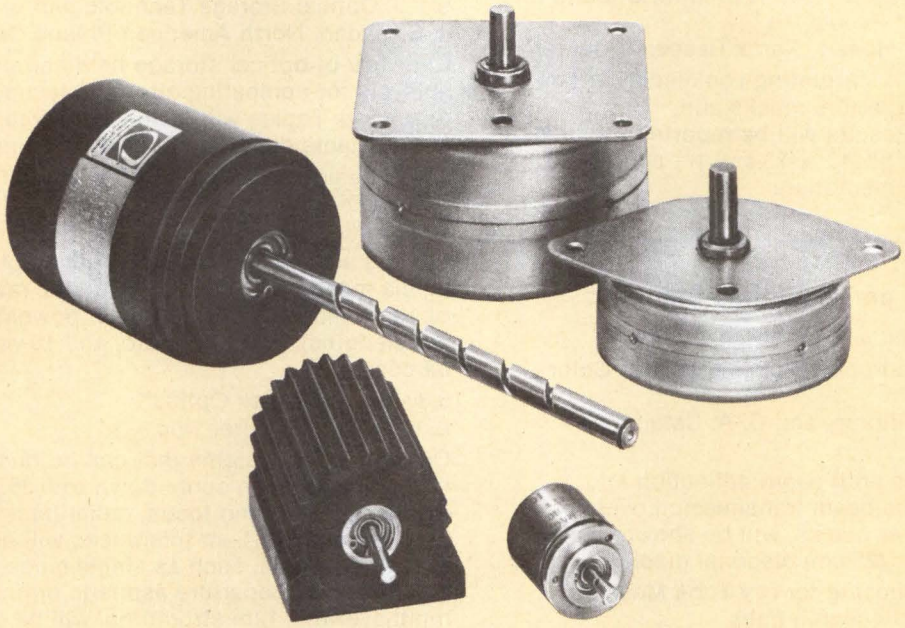

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CIRCLE 102

7/7 "Photolithographically Processed CdSe TFT Addressed LC Displays"
E. Lueder, T. Kallfass, W. Frasch, and B. Schaible, Univ of Stuttgart; and K. Koger, ITT-SEL

Speakers will explain photolithographic methods for addressing a 32- x 36-dot LCD by CdSe TFTs using an anodized Ta_2O_5 insulator with a 95% yield. Modifying anodization for improvements, liftoff steps, and electrode material will be described.

7/8 "Hybrid Processed CdSe TFT Matrix Circuits for Flat Displays and Panels"
F. C. Luo and D. D. Hoesly, Xerox Research Center

Hybrid process for constructing LCD display TFT matrix circuits combines aperture masks and photolithography. Results will be reported for 1″ x 1″ (3- x 3-cm) and 5″ x 5″ (13- x 13-cm) TFT addressed LCDs with 50-line/in resolution.

Session 8: Color CRTs

Tues 1:50 to 5:10 pm, California Ballroom

Chairman: I. M. Wilson, Zenith Radio Corp

8/1 "A Dipole-Quadrupole Focus Mask for Color Picture Tubes"
E. F. Hockings, S. Bloom, and C. A. Catanese, RCA Labs

Mask that produces both beam deflection and focusing, and triples beam transmission over conventional shadow masks, will be shown in an application to a 10″ (25-cm) diagonal display.

8/2 "Magnetic Focusing for CTV Tube Masks"
J. Verweel, Philips Research Labs

Quadrupole focusing with hard-magnetic bars can increase transparency in CTV tube masks by 50%. Methods for magnetizing masks and maintaining magnetic screening properties will be considered.

8/3 "An Inline Gun for Color Data Display"
H. Y. Chen, RCA Picture Tube Div

An inline gun developed for high resolution computer terminals will be evaluated, reporting test results on a 12″ (30-cm)V/90° tube that displays 25 rows x 80 characters.

8/4 "A Calligraphic/Raster Shadow Mask Color Display"
J. A. Mays, Systems Research Labs, Inc

A 25″ (64-cm) color display that operates in either 1023-line raster or stroke mode will be presented, along with solutions to problems that face dual-mode shadow mask displays used for simulation.

8/5 "CRTs for Avionics Displays"
J. Chevalier and J. P. Galves, Thomson-CSF

Beam penetration screen configuration and a high resolution electron gun using impregnated cathode that handles current densities up to 10^3 A/cm^2 will be discussed; cathode lifetimes over 10,000 h and efficiencies increased by a factor of 2 will be considered.

8/6 "A Fiber Optic CRT for Hard Copy in Color"
D. Denham, Tektronix, Inc

A system that produces full-color hard copy using a single fiber optic CRT is designed with a fiber optic faceplate employing three parallel strips of different colors.

8/7 "Application of Aberration Theory to Color Picture Tube Deflection Yoke Design"
Y. Nakamura, K. Ichida, Y. Sugii, and T. Saito, Sony Corp

Computer extended aberration theory will be applied into a quantitative study of misconvergence in a self-converging yoke. Computation time is shorter by a factor of 10 than with the trajectory tracing method.

Session 9: Optical Storage Technologies

Tues 1:50 to 5:10 pm, California Ballroom

Chairman: R. C. Durbeck, IBM Corp

9/1 "Optical Storage Technologies"
J. S. Nadan, North American Philips Corp

Overview of optical storage field and procedural analysis for comparing alternate technologies will be examined. Topics will include video/audio disks and field-writable digital optical storage disk systems.

9/2 "Design and Optimization of the Optical Data Disk"
A. E. Bell, Exxon Research and Engineering Co

Factors associated with write-once optical recording media meeting μ-hole requirements, raw bit error rate of 10^{-5}, moderate writing laser power (at GaAs laser wavelengths), 40-dB S/N ratio, and 10-year lifetime will be covered.

9/3 "Optical Disk Optics"
L. Laub, Vision Three, Inc

Optical heads/systems that can produce diffraction limited laser beam spots down to 0.25 μm while dynamically holding focus, radial tracking, and azimuth within 0.1-μm tolerances will be reviewed. Key optical elements, such as single-mode GaAs lasers, high numerical aperture aspheric optics, and multilayer thin film structures, will be considered, in addition to scalar diffraction theory for high convergence angles.

9/4 "Applications of Optical Disk Systems"
M. Goldberg, U.S. Department of Defense

Performance characteristics of optical disks will be explored for diverse applications, including online mass storage of 10^{15} bits, central archives, local data stores, and information distribution.

9/5 "Application of Video Disk to Commercial Systems"
W. H. Ford, Jr, International Institute of Applied Technology, Inc

Applications of video disk technology to commercial systems will be pursued, including point of sale, employee training, direct-home selling, and consumer education.

9/6 "The CED Video Disk System"
J. J. Brandinger, RCA Corp

Capabilities and applications—such as random access, stop-motion, and interactive operation—will be described for a video disk system that uses a diamond stylus to track grooves and sense video information for capacitance changes of 10^{-16} F on a 12″ (30-cm) vinyl disk holding 10^{11} bits/side.

9/7 "Performance Parameters of Reversible Amorphous Materials Used for Optical Data Storage"
D. Strand, Energy Conversion Devices, Inc

An amorphous optical storage medium that records at 8 mW with readback contrast of 12:1 and spot edge definition of 100 Å will be explained. Rewritable up to 1000 times, medium can be erased with multiple 5-mW laser pulses.

(continued on page 194)

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CIRCLE 103

Evening Panel 1: Fatigue and Discomfort Associated with VDUs

Tues 8 pm, San Diego Ballroom

Moderator: R. T. Hennessy, National Research Council

Panelists: H. L. Snyder, Virginia Polytechnic Institute and State Univ; M. Helander, Canyon Research Group, Inc; E. J. Rinalducci, Georgia Institute of Technology; M. Dainoff, National Institute of Occupational Safety and Health; and J. C. Greeson, Jr, IBM Corp

Physical and work environments in which VDUs are used, and the physiological and psychological effects on users, will be considered in light of regulations legislated to protect VDU users. Design restrictions resulting from the regulations, and design implications of adverse effects of VDUs on users will be discussed.

Evening Panel 3: Plasma vs Electroluminescence

Tues 8 pm, California Ballroom

Moderator: W. E. Howard, IBM Research Center

Panelists: E. Schlam, Electronics Devices and Technology Lab; L. E. Tannas, Aerojet ElectroSystems; P. Pleshko, IBM Corp; Y. Amano, Sony Corp; and R. Holly, Hycom, Inc

Plasma and electroluminescent flat panels have similar structures; both are matrix addressable and require high voltage drive. Factors influencing the choice of plasma or electroluminescence are controversial, and will be explored by a panel of plasma and electroluminescence specialists.

Session 10: Non-Emissive Displays

Wed 9 to 11:35 am, San Diego Ballroom

Chairman: P. Van Loan, Hewlett-Packard Co

10/1 "Electrophoretic Display with Photoconductor Addressing"

S. F. Blazo, Tektronix, Inc

An electrophoretic display addressed through a CdS photoconductor film has obtained switching lifetimes of 10^6 to 10^7 cycles. Unit accommodates panels measuring 11″ x 15″ (28 x 38 cm) with printed page viewability and resolution of 100 lines/in.

10/2 "A Photoconductor Addressed Electrophoretic Cell for Office Data Display"

N. K. Sheridon and M. A. Berkovitz, Xerox Research Center

Electrophoretic display addressed through a selenium photoconductor that employs a 3-stage switching technique will be described. Flicker-free images with light intensity levels and 250-dot/in resolution, in exposure density of under 1 erg/cm^2, have been obtained with CRT exposure.

10/3 "An Electrically Twisting Ball Display"

M. Saitoh, T. Mori, R. Ishikawa, and H. Tamura, Sony Research Center

A 25″ x 36″ (64- x 91-cm) display panel that provides 20-ms response and 85-dot/in resolution is based on electrostatically rotating spheres.

10/4 "A Solid State Iron-Garnet Crystal Film Magneto-Optic Display"

W. E. Ross, D. L. Cox, and G. R. Pulliam, Litton Systems, Inc

A 48- x 48-pixel display with LSI controlled electronic switching uses Faraday rotation of polarized light in epitaxially grown iron-garnet films. Display is temperature independent below the Curie point, and is capable of switching times in the microsecond range.

10/5 "Response Improved Electrochromic Display Based on Organic Materials"

T. Masumi, K. Nomura, K. Nishioka, H. Deguchi, and H. Ono, Mitsubishi Electric Corp

Providing 30-ms response time of over 10^6 cycles under a driving voltage of 1 V, the electrochromic display profiled in this session is designed with viologen polymer complexes and conductive powder composite films.

10/6 "Lutetium Diphthalocyanine Display Lifetime Study"

Y. Bessonnat, G. Gerard, and G. Leroy, Centre National d'Etudes des Telecommunications

Report on the effects of electrolytes and their acidity on electrochemical reactions with vapor-deposited $Lu(Pc)_2H$ thin films. Cyclic voltammetry and faradic impedance measurements will be discussed, along with benefits of improved reversibility and a lifetime over 10^7 cycles.

Session 12: Thin Film Electroluminescent Displays

Wed 9 to 11:45 am, California Ballroom

Chairman: T. C. Lim, Rockwell International

12/1 "Characterization of Electroluminescent Display Devices"

R. P. Tuttle, M. R. Miller, and E. Schlam, U.S. Army ERADCOM

Measurement techniques and profiles of efficiency, rise times, persistence, and luminance vs voltage will be presented on ac thin film electroluminescent devices from 12 proprietary sources.

12/2 "AC TFEL Displays"

L. E. Tannas and D. A. Treadway, Aerojet ElectroSystems

A 4″ x 6″ (10- x 15-cm) sunlight readable display using in-contact masks for all line definitions has been manufactured without photolithographic techniques. Sealed without a glass cover plate, the black layer electroluminescent display shows 192 x 320 lines, 64 lines/in.

12/3 "Reliability of Atomic Layer Epitaxy TFEL Devices"

J. Antson, Lohja Corp

Surface area capability, yield, and reliability of atomic layer epitaxy thin film electroluminescent units will be considered in terms of moisture resistivity, high temperature lifetime, and breakdown voltage.

12/4 "Low Voltage ac Thin Film Electroluminescent Displays"

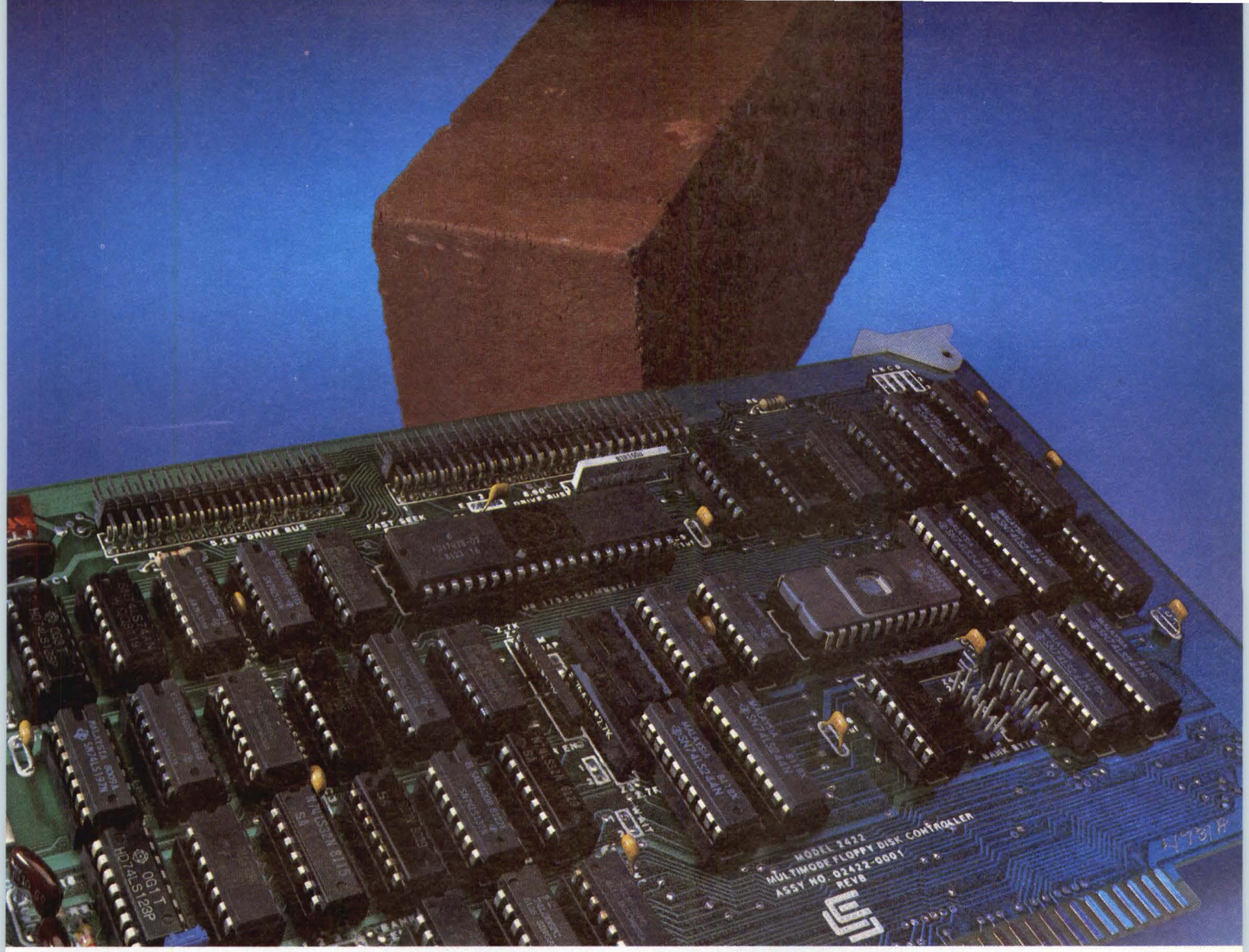
H. Kozawaguchi, J. Ohwaki, B. Tsujiyama, and K. Murase, NTT Ibaraki Electrical Communication Lab

Reducing thin film electroluminescence threshold voltages to under 50 V through metal insulator semiconductor structure and insulator materials will be explained. Luminance of 700 ft-L for ZnS:Mn and 200 ft-L for ZnS:Tb will be reported.

12/5 "Feasibility of a Dual-Color ac TFEL Device"

R. E. Coovert, C. N. King, and R. T. Tuenge, Tektronix, Inc

(continued on page 197)



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CIRCLE 104

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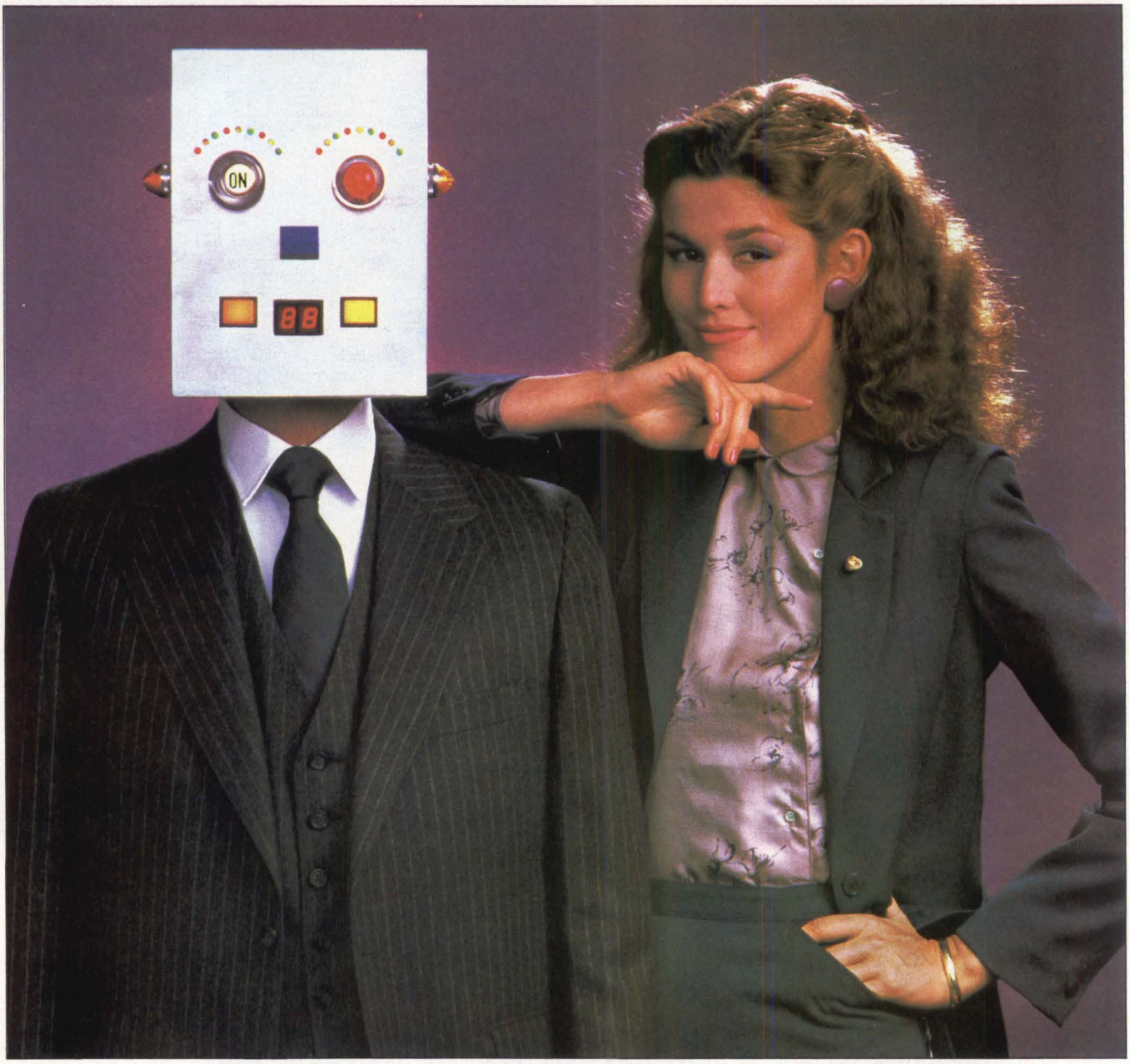

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DESIGN IN DIALIGHT

CIRCLE 105

Yellow/green fixed patterns using ZnS:Mn and $ZnS:TbF_3$ on a 4″ (10-cm) square substrate will be analyzed to assess the multilayer stacked construction technique; resulting color contrast will be described.

12/6 "A Silicon Compatible dc EL Device"
D. J. Robbins, C. Falcony, D. J. DiMaria, D. W. Dong, J. F. DeGelormo, I. F. Chang, and D. B. Dove, IBM Research Center

Method for obtaining luminance of approximately 80 ft-L using under 50 Vdc will be shown for dc thin film electroluminescent devices incorporating a silicon based electron injector.

Invited Luncheon Address

Wed 12 noon, Presidio Ballroom

"Electronic Image Realism in Film Animation"
P. S. Mittleman, Mathematical Applications Group, Inc

Slides and film clips will illustrate the technology behind Synthavision and compatible techniques, which can produce computer generated imagery that displays realism previously possible only through use of real objects or stop-motion photography.

Session 13: Displays for Visual Simulators

Wed 2:15 to 3:55 pm, San Diego Ballroom

Chairman: S. R. Black, Evans and Sutherland Computer Corp

13/1 "Visual Systems Used in Military Training and Simulation"
R. E. Holmes, System Research Labs, Inc

Developments in direct view, virtual image, and projected image and display devices used in simulation training for crews of armored vehicles, submarines, and aircraft will be presented.

13/2 "Quantification of Image Quality for CGI Displays"
E. D. Stoll and T. Lewis, Advanced Technology Systems

Parameters that account for computer generated image sampling effects, display mechanisms, and observer characteristics will be used to evaluate the effectiveness of information transfer from a computer image generator to a human observer.

13/3 "A Visual Simulator Image Generator Using a Laser Scanned Model"
G. G. Abbey, Singer Co

A 1024-line, 30-Hz image generation system has obtained 48° horizontal by 36° vertical field of view with brightness of 7 ft-L. Application to low level navigation flight simulation that uses a scanning laser beam over a 3-dimensional model board will be discussed.

13/4 "A Variable Acuity Display for Simulator Applications"
R. W. Fisher, McDonnell Aircraft Co

Display produces a 160° x 160° field of view with resolution of 2 arc-min by matching the information content of a standard 525-line raster to the variable acuity nature of the human eye.

13/5 "A Flight Simulation Color Calligraphic CRT Projector"
S. Elmer, Rediffusion Simulation, Ltd

(continued on page 198)

Computer image generator driving three projectors can present a 150° horizontal x 40° vertical image. A color system mounted on a motion platform, which uses nine enclosed Schmidt optic projectors, will be described.

Session 14: Ink Jet Printing Technology

Wed 2:15 to 3:55 pm, Golden West Ballroom

Chairman: H. L. Funk, IBM Corp

14/1 "Analysis of Drop on Demand Ink Jet"
T. Mizuno, T. Satoh, and T. Matsuda, Fujitsu Labs

Mathematical model for treating ink as a compressible fluid will be presented, and droplet ejection process simulated using an experimental printhead. Simulation results for a multinozzle head with 200-dot/in resolution will be reviewed.

14/2 "Drop on Demand Printing Technology and Acoustic Drop Shaping"
J. Heinzl, E. Kattner, G. Rosenstock, and W. Wehl, Technical Univ of Munich

Shaping of drops by acoustic waves will be compared with conventional drop ejection technique, and theory behind acoustic/fluid nozzle mechanics analyzed.

14/3 "High Speed and High Quality Color Ink Jet Printer"
M. Kobayashi, T. Takahashi, T. Okazaki, and T. Tanaka, NTT Yokosuka Electrical Communication Lab

Desktop color printer that handles 30 pages/hour will be described. Using continuous ink jet developed for display hardcopy equipment, printer produces 27 hues at 250-line/in resolution.

14/4 "The Application of Drop on Demand Ink Jet Printing to Color Facsimile"
F. Lee, R. N. Mills, and F. E. Talke, IBM Research Labs

Application of drop on demand ink jet printing to color facsimile will be investigated as a function of fluid design parameters.

Session 15: Plasma Display Technology

Wed 2:15 to 4:15 pm, California Ballroom

Chairman: P. D. T. Ngo, Bell Labs

15/1 "A 127-Line/in dc Plasma Display Panel"
Y. Amano, K. Yoshida, and T. Shionoya, Sony Corp

Constructed from screened electrodes, ribs, and dielectric layers, a 512 x 1024 panel operates at drive voltages of 30 V. Trigger electrode configuration provides intrinsic panel decoding to reduce the row drivers by a factor of 8.

15/2 "Meter Diagonal ac Plasma Display Panel"
R. E. Ernsthausen, Photonics Technology, Inc; D. R. Willis, Magnavox Electronic Systems Co; and D. K. Wedding, Univ of Toledo

Speakers will set forth performance measurements on a 1200- x 1600-element ac plasma display panel with 50-line/in resolution. Also presented will be performance of panels with resolution of over 100 elements/in, implemented in a 512 x 512 matrix.

15/3 "A 320-Character Self-Shift ac Plasma Display"
H. Yamaguchi, K. Yoshikawa, K. Kurahashi, and K. Oki, Fujitsu Labs, Ltd

Panel with 2500-cps input rate and 50-line/in resolution and a structure that eliminates barriers to confine the discharge will be described.

15/4 "Aluminum Foil Conductor Technology for dc Gas Discharge Panels"
G. H. F. de Vries, Philips Research Labs

Conductors for a dc gas discharge panel, formed by anodic thermocompressive bonding of aluminum foil to the glass substrate, will be explained. Conductor geometry has been achieved photolithographically.

15/5 "Brightness Control Technique for Memory ac Plasma Panels"
J. T. Suste and M. J. Marentic, Interstate Electronics Corp

Mixing two sets of drive waveforms can provide a 4:1 brightness control image for ac plasma display panels, without reducing input data rates. Effects on memory margins and other performance characteristics will be assessed.

15/6 "Color and Contrast Modification Techniques for ac Plasma Display Panels"
J. D. Schermerhorn, Electro-Plasma, Inc

Increasing background brightness can decrease the high contrast of ac plasma displays. Use of filtering for display color modification and a method to reduce distracting internal reflections by rear plate filtering will be presented.

Session 16: Liquid Crystal Technology

Thurs 9 to 10:30 am, San Diego Ballroom

Chairman: R. C. Tsai, Singer Librascope

16/1 "A Field Sequential Color CRT Using a Liquid Crystal Color Switch"
M. G. Clark and I. A. Shanks, Royal Signals and Radar Establishment

A uniform, flicker-free, field sequential color display based on a liquid crystal color switch and a monochrome CRT with matched phosphor will be examined.

16/2 "Development of Achromatic and Color LCDs and their Colorimetric and Ergonomic Evaluation"
T. Kosaka, H. Tsubota, and S. Kobayashi, Tokyo Univ; T. Shimomura, Kyushu Institute of Design; and R. Mizoguchi, Sanritsu Electric Co, Ltd

Optical characteristics of double-layered achromatic and color LCDs will be related in light of colorimetric and ergonomic considerations. Evaluation of both twisted nematic and guest host displays with developed polarizer and liquid crystal dye material will be reported.

16/3 "Double-Layered Guest Host Display with Wide Operating Temperature Range"
K. Sawada and Y. Masuda, Asahi Glass Co, Ltd

Characteristics of display response time, operating temperature range, and contrast ratio will be offered for double-layered guest host displays with two cholesteric layers of opposite sense of twist.

16/4 "Liquid Crystal Display Panel Using Plastic Substrates"
T. Umeda, T. Miyashita, and F. Nakano, Hitachi Research Lab

Optical analysis of liquid crystal displays with birefringent polyester film substrates, methods of optimization, and results of characterization will be presented.

16/5 "Thin Layer Electrochemiluminescence as Back Illumination for LCDs"
H. Schaper, Philips Lab

(continued on page 200)

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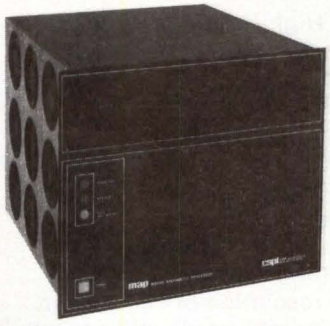

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An electrochemiluminescent, electrolyte-free light source suitable for LCD backlighting will be considered.

16/6 "Interconnection and Addressing for LCD with Reduced Lead Count"
A. R. Kmetz, Bell Labs

A modified interconnection method nearly doubles the number of addressable elements in a matrix LCD without increasing lead count. Application to pseudoanalog pointer, bar graph and annunciator, and general pattern LCDs will be explained.

16/7 "A Nonmultiplexed LCD Dot Matrix"
F. Gharadjedaghi and A. Lagos, Asulab

Along with discussions on display electrode structure and its interface, a static addressing technique applied to LCDs with improved electro-optical characteristics will be explored.

Session 17: Human Factors in Display Design

Thurs 9 am to 12 noon, San Diego Ballroom

Chairman: D. C. Hanson, Boeing Commercial Airplane Co

17/1 "The Influence of Camera Separation and Head Movement on Perceptual Performance"
R. E. Cole and R. L. Pepper, Naval Ocean Systems Center

Influence of camera separation and head movement on operator performance will be investigated. Head motion parallax cues on measures of stereoacuity, both under direct viewing and under TV viewing conditions, will be shown.

17/2 "Visual Accommodation as a Function of Display Color"
G. M. Murch, Tektronix, Inc

Test results for a shadow mask CRT comparing accommodation and the ability of the eye to converge as a function of color will be presented. Accommodation effects decrease when colors are produced with more than one of the three primary colors.

17/3 "Design Considerations for Sunlight Viewable Displays"
P. Christianson, Hewlett-Packard Co

Mathematical model for determining the extent to which luminous and chrominance contrast enhance the readability of alphanumeric displays refines existing theory by including the effects of ambient illumination and filtering.

17/4 "Color Selection and Verification Testing for Airborne Color CRT Displays"
R. M. Merrifield and D. Silverstein, Boeing Commercial Airplane Co

Color saturation effects and special display design considerations will be detailed in a discussion of color selection and visual testing methods for shadow mask color CRT cockpit displays used in the Boeing 757/767.

17/5 "Significant Reading Errors in 7 x 9 ASCII Numbers with 2% Dot Loss"
J. R. Pastor and J. A. Uphaus, Jr, AFWAL/FIG, U.S. Air Force

Significant test results ($p < 0.01$, 24 subjects) show that some 7 x 9 ASCII numbers with less than 2% dot loss can be confused with other numbers.

17/6 "Visual Changes with Prolonged Display Use"
M. Murch, Tektronix, Inc

Psychophysical measurements of visual function, made before and after a period of screen intensive study at both a storage display and a raster CRT, indicate that visual complaints of CRT operators have a physiological basis.

17/7 "Application of Large Screen Display Legibility Factors"
D. A. Shurtleff and F. Wuersch, Hughes Aircraft Co

Impact of display factors (including adaptation luminance, luminance ratio, off-axis viewing angle, and visual size) on an observer's ability to identify symbols on a large screen display will be examined.

Session 19: Hard Copy

Thurs 9 to 11:50 am, Council/Chamber/Cabinet Ballrooms

Chairman: A. Silzars, Tektronix, Inc

19/1 "High Capacity Hard Copy Using Direct Electrostatic Imaging"
E. R. Truax, Honeywell Information Systems

Current technology status, test data, and media and printing process modeling will be described for an electrostatic printing process and system operating at paper velocities over 100 ips.

19/2 "Modeling the Electrical Transfer of Conductive Toner in a Recording Process"
C. C. Lee, 3M Co

Major transfer parameters of resistivity, humidity, paper, and dielectric receptor characteristics, as well as contact time modeled with experimental confirmation using a magnestylus recorder, will be reported.

19/3 "Information Recording and Display on Low Voltage Photoconductor Materials"
M. R. Kuehnle, Coulter Systems Corp

Performance characteristics of crystalline electrophotographic materials (KC and KCY) will be outlined. Low voltage photoconductor materials have information capacity higher than that of magnetic tape and photographic film in both analog and digital formats.

19/4 "Paper Function Model for Wire Matrix Printing"
H. Wang and S. A. Hall, IBM Research

Based on optical measurements, a mathematical model for the force vs deformation characteristics of ribbon and paper in wire matrix printing will be explained.

19/5 "Heat Analysis for a High Resolution Thermal Printing Head"
Y. Tokunaga, T. Hayashi, and H. Kawahata, NTT Yokosuka Electrical Communication Lab and Nippon Electric Co, Ltd

Speakers will describe development of a 300-line/in thermal printhead having a linear array of 37 dots.

19/6 "High Resolution Thermal Printing Technology"
S. Nakaya, S. Kotani, K. Tsuli, Y. Okino, and M. K-kuchi, OKI Electric Industry Co, Ltd

A thermal printhead with a resolution of 400 lines/in that can produce a gray scale picture via pulse width modulation will be presented.

19/7 "Gray Scale Thermal Display"
S. Nakaya, S. Kotani, K. Tsuli, T. Araki, and H. Kanno, OKI Electric Industry Co, Ltd

Technique for using the temperature vs optical density characteristics of silver mercuric oxide in a bilevel

(continued on page 202)

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reversible thermal display, to obtain 16 levels of gray scale, will be examined.

Session 20: LCDs for Large Information Content

Thurs 1:30 to 4:10 pm, Golden West Ballroom

Chairman: A. R. Kmetz, Bell Labs

20/1 "Thermally Addressed Pleochroic Dye Liquid Crystal Display"
S. Lu, D. H. Davies, R. Albert, D. Chung, and A. Hochbaum, Kylex Div, Exxon Enterprises

Speakers will present thermally-addressed dye based smectic LCDs with 512 x 576 elements in a 6″ x 7″ (15- x 18-cm) panel, which can provide contrast ratios greater than 7:1 and about 30% brightness of standard white at writing speeds over 1000 cps.

20/2 "4M-Pel Liquid Crystal Protection Display Addressed by a GaAs Laser Array"
A. G. Dewey and R. W. Koepcke, IBM Research; and S. Anderson, G. Chenoff, J. Feng, C. Handen, H. Johnson, J. Leff, R. Lynch, R. Schmeideskamp, and H. Sierra, IBM General Products

Storage display system, in which a reflective smectic LC cell with a resolution of 2000 x 2300 pels can be projected at 16X onto a 40- x 48-cm screen, will be discussed. Cell is addressed by eight GaAs lasers using a fiber optic delivery system.

20/3 "Fast Liquid Crystal Displays with Low Power Addressing and Permanent Memory"
D. W. Berreman and W. R. Heffner, Bell Labs

Practical operations of 15-μm thick, cholesteric twist cells with permanent memory will be reviewed—20-ms/line writing speed, 0.1-s erasure rate, and 0.25-mW/cm^2 power consumption.

20/4 "Electrically Controlled Birefringence LC Matrix Display"
H. Schad, Brown Boveri Research Center

A reflective ECB LC matrix display capable of multiplexing 100 lines with a 7.5-V drive will be considered as a prototype text editor.

20/5 "A 5″ x 7″ Varistor Controlled LC Matrix Display"
D. E. Castleberry, C. A. Becker, and L. M. Levinson, General Electric Co

A 36-line/in varistor controlled reflective dichroic liquid crystal matrix display with a 8:1 contrast ratio, 35% reflectivity, and 50- to 100-ms response times will be described.

20/6 "Status and Prospects of MIM Addressed LCDs"
R. W. Streater, G. O. Este, S. Maniv, B. K. MacLaurin, and C. J. Miner, Bell-Northern Research Ltd

A 128 x 160, 40-line/in twisted nematic LCD multiplexed through a MIM nonlinear device array will be covered. Processing details including magnetron sputter deposition and plasma etching of conductor levels will be presented.

20/7 "CCD Addressed Liquid Crystal Light Valve"
M. J. Little, P. O. Braatz, U. Efron, J. Grinberg, and N. W. Goodwin, Hughes Research Labs

Design, performance, and applications of a 256- x 256-pel CCD addressed liquid crystal light valve will be reviewed. With a 100-Hz frame addressing rate and LC response times of 10 to 15 ms, the control device was built on a 10- x 10-mm die; 20- x 20-μm pel size gives an active area of 5 x 5 mm.

Session 21: Drive Circuits for Plasma and EL Panels

Thurs 1:30 to 4:15 pm

Chairman: A. Sobel, Lucitron, Inc

21/1 "High Voltage Display Driver Technologies"
P. A. Curran, Texas Instruments, Inc

Drivers for plasma and electroluminescent displays, which present problems not found in conventional ICs, must be designed using applicable device technologies. Speaker will outline such accommodations as incorporating serial to parallel conversion arrays on the same chip as high voltage output stages.

21/2 "High Voltage ICs for Electroluminescent Panel Addressing"
R. A. Blanchard, Supertex, Inc; and T. Gielow, Hycom, Inc

ICs capable of driving a 1000- x 1000-line electroluminescent display will be analyzed. Each chip consists of a low voltage logic section and 16 channels of high voltage drivers.

21/3 "Drive Circuits Integrated with Plasma Display Panel"
W. Henrion and M. Smalter, Texas Instruments, Inc

Technology and method of attaching plasma display driver ICs, packaged in chip carriers, directly to the glass-substrate of plasma display panels will be reported.

21/4 "A Low Voltage EL Drive System"
G. C. Smith, S. K. Tiku, and M. R. Johnson, Texas Instruments, Inc

A system for driving electroluminescent matrix displays requiring only a 60- to 100-V standoff for all address drivers will be covered, in which row and column drivers float on X and Y high voltage ac waveform generators.

21/5 "Switch Mode Drivers for Thin Film Electroluminescent Gray Scale Displays"
S. P. Graves, R. D. Ketchpel, M. K. Kilcoyne, and L. G. Hale, Rockwell International Corp

An approach for addressing gray scale electroluminescent displays using transistors in a switching mode reduces the complexity and power dissipation of the individual driver circuits.

21/6 "A Fully Integrated MOS EL Matrix Display Device"
K. Oki, Y. Ohkawa, K. Takahara, and S. Miura, Fujitsu Labs, Ltd

A 20- x 20-dot device that uses a 2-transistor and Zener diode architecture for the active matrix circuit will be explained. Addressing shift registers were integrated on the same silicon substrate.

Session 22: CRTs and CRT Devices

Thurs 1:30 to 3:55 pm, Council/Chamber/Cabinet Ballrooms

Chairman: J. A. Mays, Systems Research Labs, Inc

22/1 "High Luminance, High Resolution Special Purpose CRTs"
M. W. van Tol and J. van Esdonk, Philips Research Labs

Speakers will report on a 1″ (3-cm) CRT with a monocrystalline, epitaxially grown luminescent screen, producing a 9-μm spot size at 20 kV and a

(continued on page 204)

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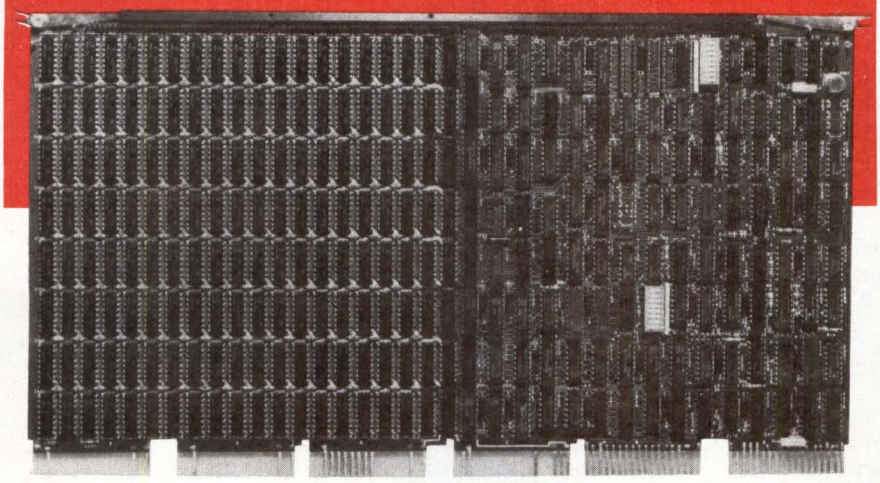

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PDP®-11	DR-114S	hex	256 KB
PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214SP	hex	1.0 MB
PDP-11	DR-144S	hex	256 KB
PDP-11	DR-244S	hex	4.0 MB
VAX®-11/750 PDP-11/70	DR-175S	hex	256 KB
VAX-11/780	DR-178S	extended hex	512 KB
DECSYSTEM 2020®	DR-120S	extended hex	512 KB
PDP-8/A	DR-118S	quint	128 K x 12

DEC, DECSYSTEM 2020, PDP and VAX are registered trademarks of Digital Equipment Corporation.

Dataram also provides core add-ins, core and semiconductor add-ons, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

CIRCLE 108

3.5-μA beam current with 1.9 x 10^8 cd/m^2 brightness. TV image has a 500-line resolution on a 12- x 16-mm^2 screen with a 7000 cd/m^2 luminance. Tube produces 64,000 cd/m^2 maximum at a lower resolution.

22/2 "Optical Performance of Contrast Enhancement Filters"

K. D. Jacobsen, Optical Coating Lab, Inc

Techniques for measuring contrast and resolution ratios of several contrast enhancement filters will be explored. Matrix filters, antihalation coatings, and antireflection coatings will also be evaluated.

22/3 "Holoform Oscillography with a Parallactiscope"

H. B. Tilton, Visionics Labs

Device with a horizontally moving slit and a CRT that can display realtime (opaque or transparent) 3-dimensional images will be discussed.

22/4 "A Model to Account for Rim Lighting in Direct View Storage CRTs"

B. Ostermeier, Tektronix, Inc

Stable luminescent areas adjacent to collector dots in direct view storage CRTs provide background luminance. Experimental evidence supporting a display model for this phenomenon will be presented.

22/5 "Experimental Display and Camera Tube for 1125-Line TV System"

E. Yamazaki, T. Ueda, F. Otsuka, Hitachi, Ltd

A 1″ (3-cm) camera tube and a 9″ (23-cm) projection CRT providing a 1125-line color image on a 55″ (140-cm) diagonal screen will be evaluated.

22/6 "Scan Expansion Lens for High Speed Storage Oscilloscopes"

A. S. Berger, Hewlett-Packard Co

An electrostatic crossover lens for use in a variable persistence, storage CRT features 99% deflection linearity and a center to corner spot growth of less than 30%. Computer modeling, used extensively for design optimization, will be analyzed.

22/7 "Performance of Color CRTs in Above Ambient Static Magnetic Fields"

M. E. Crost, U.S. Army Electronics Technology and Devices Lab

Effects of above normal magnetic fields on shadow mask or aperture grille types of color CRT will be reviewed. Results call for high permeability and high retentivity shield.

Session 23: Display Systems and Image Processing

Thurs 1:30 to 4:40 pm, Forum/Senate/Committee Ballrooms

Chairman: J. N. Price, Naval Ocean Systems Center

23/1 "A TV Based Multiscreen Display System"

M. J. Hauesing, Forschungsinst. f. Anthropotechnik

A system for displaying 4000- x 4000-point imagery will be covered. Four high resolution TV monitors forming a multiscreen matrix are driven from a common display processor, making it possible to present and manipulate large images with continuity.

23/2 "Increased CCD Resolution Using Image Shift Sampling"

K. A. Hoagland, Fairchild Weston Systems, Inc

Image shift sampling techniques in an experimental TV system have demonstrated enhanced resolution by a factor of 2. Method for extending the useful resolution of CCD image sensors and applications for other phototransmission systems will be investigated.

23/3 "A Minidisplay for Combined Map/Graphic Data Presentation"

P. C. Baron, Hughes Aircraft Co

Development of a handheld minidisplay for high ambient light environment (ie, tactical battlefield use) will be discussed. A compact Weiss prism magnifier and 1″ (3-cm) CRT with fiber optic faceplate accurately combine computer generated graphics/alphanumerics with map data on film chip transparencies.

23/4 "Requirements of Clinicians and Medical Imagers for Information and Display Processors"

W. Airth-Kindree, D. P. Lawrence, and A. B. Baskin, Univ of Illinois

Interactive display system that handles alphanumerics, graphics, and multiaxial imagery will be explained, along with display and processing applications for medical doctors.

23/5 "A Computer Graphics Tool for Design of Interactive CRT Workstations"

J. A. Roese and L. E. McCleary, Naval Ocean Systems Center

Computer graphics will be considered as a design tool in the development of a hierarchical family of interactive CRT workstations. Methods employed with a MOVIE.BYU graphics package that rapidly converts engineering concepts into realistic graphics images will be shown.

23/6 "3-Color IR Image Process"

J. J. Stapleton, Coast to Coast Consultants

Realtime, full-color 9″ (23-cm) display of three discrete infrared bands will be examined.

23/7 "A Surface Interpolation Algorithm"

T. A. Foley, California Polytechnic State Univ

An interpolation algorithm permits fitting a surface in three dimensions. This method is more stable than earlier such approaches, and is capable of smoothly filling in areas devoid of data. □

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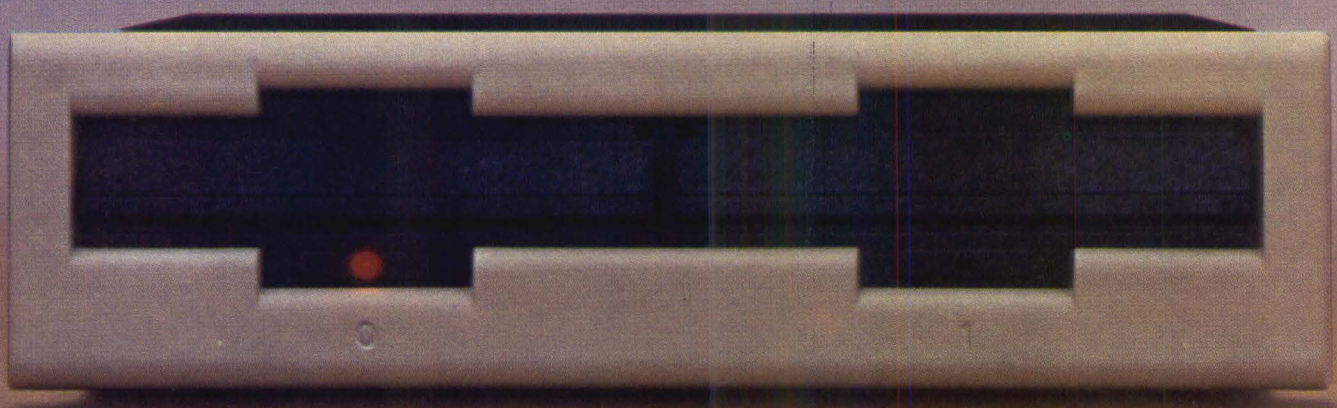

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"Compatible" doesn't mean "the same."

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Our 430 and 440 Floppy Systems are a case in point.

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Budgets being what they are, you'll be pleased to know there's a single-sided, double-density, 1-megabyte floppy system you can buy at a ridiculously low price.

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Like a built-in hardware bootstrap. LSI-11/23 4-level interrupts. On-board diagnostics. And more. All with a low 5¼" profile.

The DSD 440. Your full-featured alternative.

Our 440 has all the features of the economical 430, and then some.

Like our exclusive HyperDiagnostics,™ a built-in, stand-alone diagnostic system that lets you test, exercise and debug without a CPU. And, in many cases, lets you get back up and running without a service call.

The 440 works with the PDP®-11 as well as the LSI-11, and emulates both the RX02 and the RX01. What's more, it also supports the new LSI-11/23 Plus in the RX01 mode.

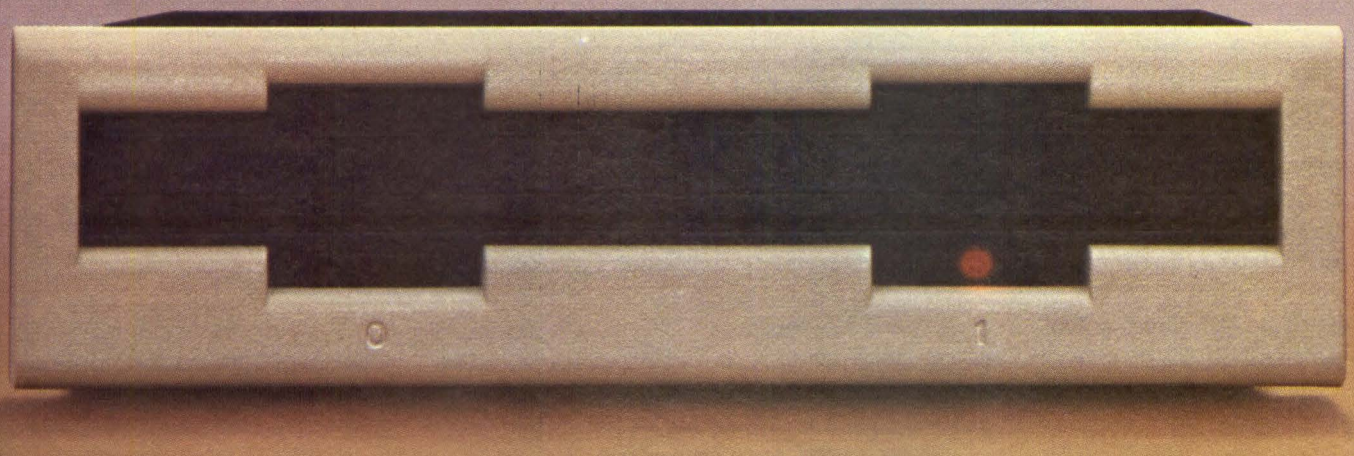
And the service and support to match.

Like the rest of our systems, we back up the 430 and 440 with DSD exclusives like our Rapid Module Exchange™ program, designed to give you next-day replacement of a faulty module. HyperService,™ which takes over when your 90-day warranty expires and covers everything. And a DEC-compatible sales and support network second only to Digital.

So you see, when it comes to a floppy for your Digital system, there really isn't an alternative. After all, why settle for something that's just compatible, when you can have a system that's incomparable?

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. Eastern Region Sales and Service: Norwood, MA, 617 769-7620. Central Region Sales: Dallas, TX, 214 980-4884. Western Region Sales: Santa Clara, CA, 408 727-3163.

DATA SYSTEMS DESIGN



INTERNATIONAL SALES: Australia 03/544-3444; Belgium and Luxembourg 02/7209038; Canada 416/625-1907; Central and South America (office in U.S.A.) 415/967-8818; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/298783; Italy 02/4047648; Japan 06/323-1707; Netherlands 020/45 87 55; New Zealand 4/693-008; Norway 02/78 94 60; Spain 34/433-2412; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 44/7073/34774; West Germany and Austria 089/1204-0; Yugoslavia 61/263-261.

Color Retro-Graphics.™ Our Terminal Enhancements Cross Yet Another Frontier.

For over three years now, Retro-Graphics™ terminal enhancements have transformed some of today's most popular alphanumerics terminals into impressively-featured graphics terminals. Now Digital Engineering, the pioneer in graphics upgrades and creator of Retro-Graphics, has taken its successful idea and made it a colorful one as well. An idea that makes sense to the business and scientific communities alike, by making sales and financial charts, as well as complicated engineering drawings, easy to produce—and startlingly easy to afford.

Introducing the DM800 Retro-Graphics Enhancement for the Datamedia™ Colorscan™ Terminal.

Here is a formidable tool. Eight colors, chosen from a 64-color palette, can be selected and displayed at once. And thanks to a high-quality 640 x 480 resolution, graphics images are displayed crisply and vividly. There is, of course, Tektronix® 4027 graphics terminal emulation, fully software compatible with ISSCO's® DISSPLA® and TELLAGRAF® and Tektronix PLOT 10® The enhanced Colorscan terminal does vector and arc drawing, point plotting, text generation, area fill and shading patterns, thus allowing complex graphics functions to execute with a single instruction. Graphics input options include a light pen for selecting and altering screen objects as well as a bit pad for fast entry of X-Y coordinates. And for color hard copy, the Retro-Graphics DM800 interfaces to a variety of printers, plotters and cameras.

Other Retro-Graphics terminal enhancements are available for Lear Siegler's ADM-3A and 5 Dumb Terminal® displays, TI's 940 Electronic Video Terminal and DEC's™ VT100™ and VT132™ Terminals.

All of the Above for Well Below the Competition.

High-quality, high-power color graphics at a price thousands of dollars less than competitive products. Suggested retail price for the Retro-Graphics enhanced Colorscan terminal is actually under $5000. Call your Digital Engineering distributor today for more information, or contact us directly.

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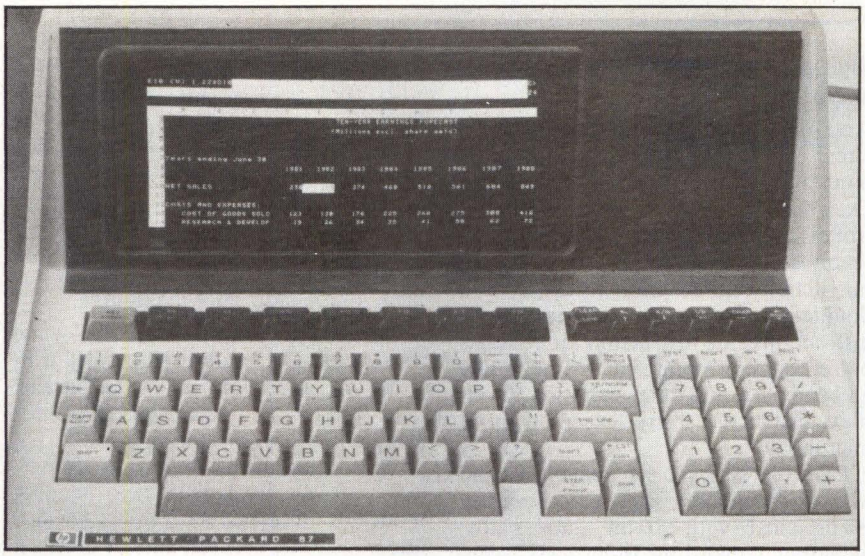
(916) 447-7600, TWX: 910-367-2009

CIRCLE 111

Personal computer with user memory to 544k bytes



The newest member of the HP series 80 family of personal computers, HP-87 has integrated text and graphics display, enhanced HP BASIC and expanded software support, and expandable user RAM up to 544k bytes. The system comes with 32k bytes of user RAM, 48k bytes of BASIC in ROM, and 16k bytes of display RAM. RAM automatically configures into a single contiguous block when machine turns on to make all memory usable for program execution and data storage. Memory modules come in increments of 32k, 64k, or 128k bytes. List prices of the modules are $295, $450, and $795, respectively.

Modules plug into 4 back ports to meet user selectable memory requirements. Maximum total RAM and ROM is 608k bytes. Large memory provides capacity to analyze complex problems with high data content, capabilities previously associated with larger systems. Using max memory capacity, system can analyze a VisiCalc® worksheet of 254 x 63 completely full cells.

Software

System 87 is upwards compatible with the HP-85. Company developed applications software includes ac circuit analysis, statistics, information management, word processing, graphics presentation, and financial packages. Engineering, accounting, and business programs are planned with third-party suppliers. VisiCalc PLUS for the HP-87, a more powerful software version that takes advantage of the increased memory capacity, is available for $250.

HP "SuperPacs" software combine 3 software pacs for statistics and electronics engineering, and are priced at $225 each. Statistical analysis pac includes general statistics, regression analysis, and data management; electronics engineering pac contains math pac, ac circuit and waveform analysis pacs.

HP 82900A CP/M system, with Z80 processor plug-in module, runs CP/M software. CP/M compatibility also allows machine to run programs in FORTRAN, Pascal, COBOL, and other languages. CP/M system sells for $495. HP qualified CP/M software includes WordStar™ word processing programs and dBASE II™ database management programs.

BASIC commands for plotting charts/graphs include string arrays, multi-character variable names, callable line labels, and indented program listing. Assembler ROM allows custom assembly language programming. Increased speed is obtained by redefining BASIC commands and creating custom BASIC key words. Assembler ROM comes with comprehensive manual and is available for $295. HP series 80 software catalog summarizes all HP and independently developed software applicable to the series.

Peripheral disk drives, printers, and plotters

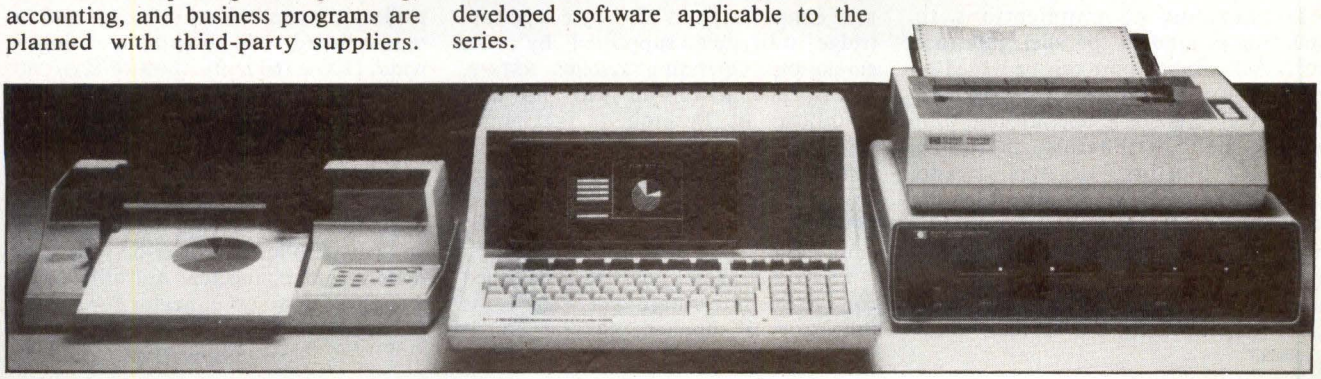
All previously introduced HP personal computer peripherals are compatible with the HP-87. Mass storage options include System 5, with computer and HP 82902M single-floppy drive with 270k-byte storage for $3995. System 10 consists of computer and HP 82901M dual-floppy drive with 540k-byte storage for $4695. System 30, with computer and HP 9135 Winchester fixed drive, gives 5M-byte mass storage with 270k-byte capacity on a built-in floppy disk drive and sells for $7995.

HP-IB, an enhanced IEEE 488 interface bus, provides communications capability with the existing peripherals. Compatible printers include HP 82905 impact printer at $795 and HP 2601 letter quality printer at $3950. Interface and printer commands in ROM are built into the HP-87—no other accessories are required for printer communication. HP 7470 graphics plotter provides professional quality graphics and is priced at $1550.

Data communications

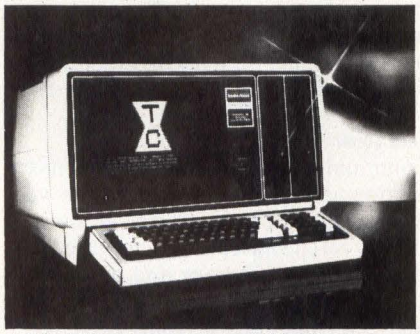
Communications between the HP-87 desktop unit and other systems is via HP 82950A modem, which connects directly to U.S. telephone lines. Modem features include storage and automatic dialing. Data can be collected and analyzed from other personal and larger computers, such as HP 3000 and HP 1000, and from database sources such as The Source™ and Dow Jones News/Retrieval Service™. Data communications pac software and serial interface handle communications in hardwire systems. Plug-in modules for RS-232-C serial, general purpose I/O, binary-coded decimal, HP-IL interface loop, and parallel printer are optional for communications with instruments, peripherals, and HP 41 handheld computers. Price of the interface modules range from $195 to $495. List price of the HP-87 is $2495. For further information, call the local **Hewlett-Packard** sales office.

Circle 263



16- and 8-bit TRS-80 CPU

TRS-80® computer model 16 features 16-bit, dual-processor architecture, and a multi-user operating system. The computer is capable of 512k internal RAM storage and 2.5M bytes of disk memory using 2 built-in, thin line double-sided 8″ disk drives. Additional external disk storage can be added. Combined RAM and disk memory capacity allows the model to use more sophisticated, user-friendly software with large file capacities. The desktop system will be available second quarter 1982 in 2 versions, both with 128k memory. A single-drive version with 1.25M bytes of disk storage (26-6001) will be priced at $4999. A 2-drive version (26-6002) with a total 2.5M-byte storage capacity will be available for $5798.



Model uses Z80A and 16-bit MC68000 microprocessors. MC68000 data path is 16-bits wide, and complex data can be processed at high speeds with internal 32-bit operations. Z80A as a second processor allows software compatibility with existing TRS-80 model II software. The Z80A optionally frees the main CPU for processing. Model 16 COBOL will be available, along with FORTRAN, and compiler and interpreter BASIC software.

Expansion to multi-user operation is possible with 1 or 2 added terminals that can be located remotely. Three users can access programs and information simultaneously, with no perceptible loss of performance. Model 16 is TRS-80 hardware compatible, and is equipped with 2 RS-232-C serial interface ports capable of bisynchronous communications to mainframes and a parallel interface port. A hard disk port can be added to permit use of up to four 8.4M-byte hard disk drives. System is upgradeable with off-the-shelf peripherals, including printers, plotters, digitizers, and telephone modems. It is compatible with the ARCNET local network; ARCNET can support any combination of up to 255 model II and model 16 computers. **Tandy Corp/Radio Shack**, 1800 One Tandy Center, Fort Worth, TX 76102.

Circle 264

High performance 16-bit bipolar microprocessor

Am29116 is a 78,000 mil^2 (50,322 mm^2) circuit manufactured using the company's proprietary IMOX™ process. Designed for high performance controller applications, the microprocessor features 100-ns microcycle time for all instructions. In addition to single- and double-operand logical and arithmetic instructions, the instruction set contains bit set, bit reset, rotate and merge, rotate and compare, and CRC generation. Complex instructions are executed in 1 microcycle.

Offering MIL-STD-883 reliability and INT-STD-123 quality, the microprocessor is designed with 16-bit data paths, including 32-word by 16-bit RAM, accumulator, data latch, barrel shifter, priority encoder, status register, condition-code generator/multiplexer, ALU, 3-state output buffers, and instruction latch and decoder. AmSTS™ 29/10 development system supports the microprocessor with symbolic development of microcode, high speed control store emulation, target system clock control, and logic state monitoring. Optional Am29/6310 high speed trace unit with logic state capabilities permits tracking of microinstructions and bus paths inside complex bit-slice architectures. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 265

4M-byte, 22-bit addressing/ 20.8M-byte disk for LSI-11/23

XL2400 provides 22-bit addressing capable of supporting up to 4M bytes of RAM. Subsystem includes an LSI-11/23 microcomputer and 256k bytes of memory. System is fully compatible with DEC hardware and software. Two serial RS-232 ports; diagnostics; and 8-slot, quad-width built-in Q-bus backplane to connect the processor, memory, and all device controller are provided. Unit also comes with a 20.8M-byte subsystem with RL02 emulation, and 17M-byte tape cartridge subsystem supported by TU10 emulation. Operating systems RSTS/E, RSX-11, and RT-11 run with no user modifications. Desktop or rackmount versions are available. Options include 4 serial ports, floating point processor chip, 256k-byte memory cards, and 550/80 disk subsystem with RMO2 emulation.

XL2000 peripheral package is designed for systems integration where the LSI-11 processor is supplied. System comes with a 20.8M-byte disk, 17M-byte tape subsystem, and 4 x 8 Q-bus backplane with power sequence and termination. A bootstrap and diagnostic kit are contained in a set of PROMs. **Xylogics, Inc**, 144 Middlesex Turnpike, Burlington, MA 01803.

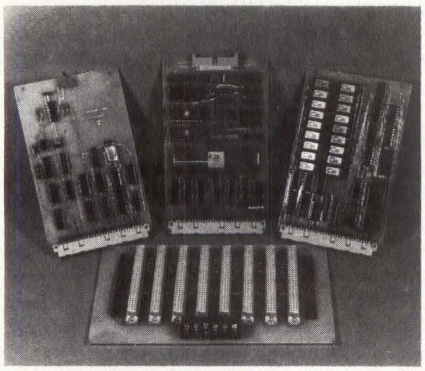
Circle 266

8048 single-chip microcomputer

M150 controller chip is an 8048 single-chip microcomputer, mask programmed with firmware to provide serial and parallel data interfaces to the EPSON M-150 dot printer. Features include 40-pin DIP, 5-V power requirement, 64-char ASCII set, and software selectable text or data mode. Dot addressable graphics are also under software control, and a full 96 x n line contiguous field is provided. Pinouts optimized for easy single-sided PCB layout, multiple sourced 8048 processor, and comprehensive self-test facilities are std. **Friday Partnership**, 22 Wentworth Close, Rudheath, Northwich, Cheshire, CW9 7EE, England.

Circle 267

Single-board modules with VME bus compatibility



Single-board modules based on Eurocard format are VME bus compatible and provide both single- and dual-connector formats. Format uses pin and socket style connectors rather than edgecard connectors. Evaluation boards available include a CPU, system controller, dynamic RAM boards, and a motherboard. All boards are single-width (100 x 160 mm). VME8100/68000 CPU board features 8-MHz CPU, up to 16k-bytes of EPROM, RS-232 port, strap selectable bus priority level, and capability to handle 4 levels of VME bus interrupts. VME8000/system controller board handles bus arbitration and timeouts, and has pushbutton power-on reset, and remote reset connector. A 16-MHz system clock and LED indicator for system fail line are included. VME8200/128k-byte

(continued on page 212)

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It is if you're shipping more than 10,000 logic systems a year.

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Because Microcell logic gates are in software, not silicon, you can get your prototypes in 18 weeks. And your savings go beyond lower chip costs because our semi-custom solutions reduce real estate, assembly, testing and rework. And eliminate all the interface problems of multi-chip designs.

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CIRCLE 112

memory board has selectable parity error generation, 200-ns dynamic RAM, and is addressable on any 128k boundary. VME8058/8-slot motherboard is fully terminated and has power connector for 5 Vdc, 5 Vdc standby, ±12 Vdc, GND, and ACFAIL. Also available is VME8900 debug monitor that resides in two 2732 EPROMs. **Mizar Design**, 2850 Bailey Rd, Newport MN 55055.
Circle 268

MULTIBUS CPU board

MULTIBUS compatible single-board compter utilizes 8-MHz 68000 CPU with up to 256k bytes of onboard RAM. It supports UNIX operating system, Pascal, or Ada software. Board features 2-level memory management system with multiprocessing capabilities, and includes up to 32k bytes of EPROM/ROM, 2 serial multiprotocol communications controllers for up to 880k-baud rates, 2 undecided timers, a 16-bit input port, and full multimaster capability on the MULTIBUS. A single 5-V supply powers the board. Memory management unit allows fast context switching between 16 simultaneous processes. Organization of the page map, for 2048 byte pages, includes all mechanisms to implement demand paging and virtual memory. Operating software available includes advanced USCD Pascal operating system, a 68000 macro assembler, plus Pascal and TeleSoft-Ada compilers. **Pacific Microcomputers, Inc**, PO Box A81383, San Diego, CA 92138.
Circle 269

Chip level PDP-11s

MICRO/T-11 chip 16-bit microprocessor has base level PDP-11 instruction set and is compatible with LSI-11 boards. The 40-pin microprocessor can be operated with a variety of industry std devices with user selectable 16- or 8-bit data bus. Chip enables high volume integration of PDP-11 instructions, and is used as the central processing unit for Falcon SBC-11/21. It is particularly suitable for controller type applications. Application programs can be developed on PDP-11 minicomputer or microcomputer systems using MACRO 11 assembly language. Chip will be available in limited sample quantities beginning in April, with volume shipments scheduled to begin in the summer. Unit price is $75 in volumes greater than 1000. **Digital Equipment Corp**, Maynard, MA 01754.
Circle 270

Floating point processor module

A floating point arithmetic (FPA) processor module that saves CPU time when performing trigonometric and other complex mathematical calculations is designed to enhance computing capability of the GL 868 microcomputer product line. Module is contained on a std 4.5″ x 6.5″ (11.4- x 16.5-cm) card that is inserted into the logic nest with std CPU. It provides for multiplication, division, transcendental functions, and 32-bit floating, 16-bit fixed point, 32-bit fixed point instructions, and std CPU instruction set. Device clock features a busy flag during computations, software reset and interrupt capabilities. Processor is address selectable to allow more than one FPA module to be used in a system. **Giddings & Lewis Electronics**, 666 S Military Rd, Fond du Lac, WI 54935.
Circle 271

Low cost 8-bit microprocessor

8020H, an 8-bit microcomputer with 1k-byte ROM, sells for $2 per device in quantities of 10,000 or more. It is a cost competitive alternative for configurations currently using 4-bit devices in high volume, price sensitive product markets. Device is based on the MCS-48 microcomputer family, and uses an 8048 instruction subset. Packaged in a 20-pin DIP, the self-contained device contains 1k x 8 ROM and a 64 x 8 RAM. Also onboard are an interval timer/counter, clock, and 13 I/O lines. Executing most instructions in 8.38 ms, the 5-V chip consumes 30 mA typ at 25 °C. Development and support systems available from the company include the EM-2 emulation board, ICE-49/MCS-48 and ICE-22 in-circuit emulators, and HSE-49 high speed emulator. **Intel Corp**, 5000 W Williams Field Rd, Chandler, AZ 85224.
Circle 272

Logic analysis this easy should be expensive. But it isn't.

Thanks to our PM3543's state-of-the-art technology, time-consuming logic analysis is a thing of the past.

Simply attach the 40 pin DIL clip to the microprocessor, select disassembly and instantly the logic analyzer is set up to look at address and data from the chosen microprocessor.

Then read.

The PM3543 has resident disassemblers for the most popular 8- and 16-bit microprocessors which are called up simply at the push of a button.

The 8-bit microprocessors include the 8048 family, 8080, 8085, 6800/02/08, Z80 and 6502/12 all in a single option. A second option includes the 16-bit microprocessors, the 8086 and Z8000 as well as the 6809, 8088 and 1802.

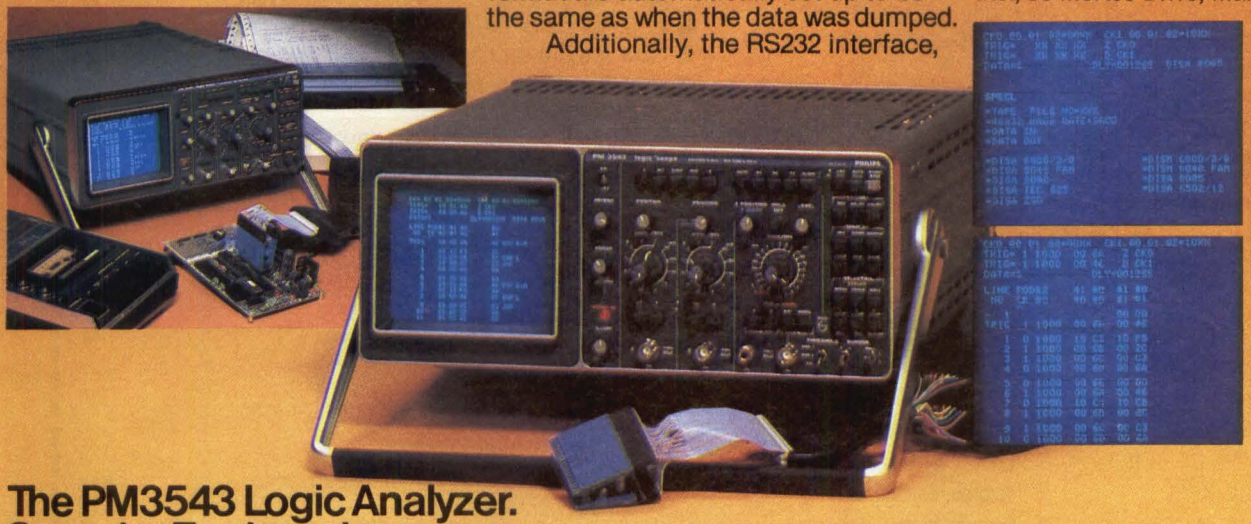
Using these options, data can be stored using an inexpensive cassette tape recorder. You may want to record a self-diagnostic routine in the lab and take it to the production line or into the field for servicing, or just for future reference. When loading back to the analyzer, both compare memory and trigger format are automatically set up to be the same as when the data was dumped.

Additionally, the RS232 interface, included, permits hard copy of the collected program through the use of a printer. Just select the baud rate and print out. (IEEE 488 also available.)

The PM3543 is so easy to use and so low priced you'll wonder how you ever got along without it.

Call or write today for a free eye-opening demonstration.

For nationwide sales and service information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, NJ 07430.



Special menu for disassembly and serial interface options, as displayed on PM3543 screen.

Our dual clocking PM3543 demultiplexes the multiplex bus microprocessors, enabling both address and data to be sampled from a single connection. This, combined with more than 20 possible ways of triggering and sampling data, gives ultimate user flexibility.

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CIRCLE 115

Everything you always wanted to know about DSP but didn't know who to ask.

Attend a free half day seminar coming to your area soon.

TRW LSI Products is the acknowledged world leader in VLSI components for high speed **digital signal processing**. A member of our applications engineering staff will conduct your seminar. If DSP are simply letters of the alphabet to you you'll learn some of the basics of this fast-expanding field. And if you're already knowledgeable in one area of DSP, this seminar will give you the overview you'd like to have. Here are a few of the highlights one of our technical experts will cover.

- What *is* digital signal processing, and what are its advantages?
- How do we use digital processing in an analog world?
- What components are used in digital signal processors, and how are they selected?
- What kinds of processing can be performed?
- How are digital filters designed and analyzed?
- How are digital signal analyzers designed and implemented?
- What new products are in development?
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CIRCLE 116

Enhanced microcomputer line

Enhanced versions of the QDP-100 microcomputer line feature automatic drive shut-off, true turnkey operation, and air filtering/cooling process. The automatic drive shut-off automatically turns off the disk drive motors after a user assigned preset time interval of system nonuse elapses. Interval can range from 1 to 99 min. Back panel ac outlets for peripherals are switched on/off by the front panel power key. Turnkey operation permits the CP/M to be automatically booted whenever the computer is reset or upon system power-up. **Quasar Data Products**, 10330 Brecksville Rd, Brecksville, OH 44141.
Circle 273

S-100 bus computer

Std S-100 bus computer is IEEE compatible and includes power supply, 8-slot motherboard, 2 Shugart 801R disk drives, 4-MHz Z80 CPUs, single- and double-density disk controller with std IBM formats, 64k dynamic RAM, 5 serial ports under software control, and a CP/M 2.2 operating system. Unit is compatible with RS-232 CRT terminals and printers. Computer supports BASIC, C BASIC, Pascal, COBOL, FORTRAN, and other high level languages. Applications software is available with selection of CP/M compatible programs. **Beavercreek Computer Systems**, 2465 Banyon Dr, Dayton, OH 45431.
Circle 274

PERIPHERALS

Graphics system

Color/monochrome graphics system G-6150 incorporates G-6000 advanced display computer, graphics processor, refresh memory, and a post processor. The 16-bit processor is PLA oriented, bit slice design, with internal instruction set time of 160 ns. It is equipped with 16k-byte PROM and 112k-byte RAM. Refresh memory is 768 x 512 x 4 full bit map, with 60-Hz non-interlaced for flicker free viewing. Sixteen colors or monochrome shades can be chosen from a palette of 64. Selectable raster DMA from host to refresh is provided to accommodate imaging requirements. Animation assist mode automatically erases the graphic during refresh to reduce erase/rewrite time by 50%. Post processor includes video timing, bit level scroll, integer zoom (1 to 16), and programmable video lookup table. Options include expanded resolutions to 1536 x 1024 x 4, additional overlay memory planes, interfaces for minicomputers, and RS-232-C interface. Dual-channel version is also available. **Genisco Computers Corp**, 3545 Cadillac Ave, Costa Mesa, CA 92626.
Circle 275

Attention, Multibus™ users...

Only the CD100M now supports CP/M and CP/M86 in the perfect desktop package.

Hear this, LSI-11 users...

Only the CD100L emulates a VT103, an RL02 and an RX02 in a single desktop package.

And both now include a 10 megabyte Winchester!

CD100M — THE TOTAL OEM SOLUTION

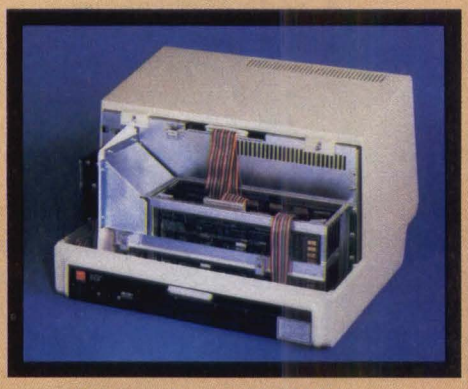
To give your Multibus microcomputer system increased file storage, the Callan™ CD100M Integrated Work Station now includes a high performance 10 Mbyte 5¼-inch micro Winchester disk drive complete with full DMA and fully automatic and transparent burst error correction. A one Mbyte unformatted floppy provides file entry and back-up. With its integral 6 slot Multibus compatible card cage, intelligent video terminal, and Winchester/Floppy disk system, the CD100M is the *only* single desktop package available to OEM and volume end-users who wish to configure a modular microcomputer system using any Multibus compatible card set. It's the perfect solution, significantly reducing product costs and development time.

CP/M AND CP/M86 CONFIGURATIONS

If you prefer the popular CP/M operating system, Callan can provide the CD100M with either 8-bit or 16-bit micros. A Z80 with 64K RAM and CP/M, or an 8086 with 128K RAM with error correction and CP/M86 are both available as the complete solution for CP/M compatible software. And both systems include 10 Mbyte Winchester performance.

If you're using Multibus cards in your system you must see the Callan™ CD100M Integrated Work Station.

CP/M and CP/M86 are trademarks of Digital Research. Multibus and 8086 are trademarks of Intel Corp. Z80 is trademark of Zilog.



Built-in card cage holds 6 Multibus or 7 quad/14 dual height LSI-11 cards.

Callan™

DATA SYSTEMS

2637 Townsgate Road
Westlake Village, CA 91361
Telephone: (805) 497-6837

CD100L — COMPLETE DEC COMPATIBILITY

For the OEM or end-user configuring an LSI-11 system, only the Callan™ CD100L Integrated Work Station can emulate a 10 Mbyte RL02 Winchester disk, a 0.5 Mbyte RX02 floppy, and a VT103 Terminal in a *single* desktop unit. Software presently running on RT-11, RSX-11 or other LSI-11 operating systems can now run on the CD100L, reducing hardware costs by as much as 30%. For users who prefer a more complete solution, the CD100L can also be ordered complete with LSI-11/2 or LSI-11/23 and RT-11.

MORE FOR LESS

No other solution compares for performance, features and price. The VT100/VT52 compatible terminal offers 6 video attributes, true split screen with separate scrolling regions standard. The LSI-11 Q-bus compatible card cage provides 7 quad or 14 dual height slots to house even the largest configurations. A Winchester controller is available to directly emulate the 10 Mbyte RL02. RX02 emulation is available either in a 1 Mbyte dual floppy configuration or as 0.5 Mbyte back-up for the Winchester.

If you're tired of multiple package or multiple vendor solutions, you must see the CD100L.

DEC, LSI-11, VT103, RL02, RX02, RT-11, RSX-11, VT100/VT52, LSI-11/2, LSI-11/23 are trademarks of Digital Equipment Corp.

Callan is trademark of Callan Data Systems.

CIRCLE 118

Digitizing option for IBM Personal Computer

Graphic analysis package #1 provides digitizing hardware and software support for the IBM Personal Computer. Package is designed so that digitizing can start without prior user experience. Hardware includes a digitizer with 0.001″ (0.0254-mm) resolution [11″ x 11″ (28 x 28 cm) to 42″ x 60″ (107 x 152 cm) active area are optional], digitizing stylus, power supply, and communications interface cable. Software supplied on disk can be used for such measurements as material usage and cost; length, distance, perimeter and area; and display of X, Y coordinates. Software is controlled by a 22-function block menu attached to the tablet. Eleven functions are predefined and 11 blank functions can be user defined. Programs allow user access to digitizer input driver, measurement routines, and menu to build custom digitizing programs. IBM Personal Computer graphic commands can be used interactively once the digitizer has been interfaced and input drivers developed. **GTCO Corp,** 1055 First Street, Rockville, MD 20850.
Circle 276

Portable terminal system

EXECUPORT[R] 4120 multimicroprocessor based portable terminal is designed to produce print copy at continuous speeds of 120 chars/s. A 16-element columnar printhead produces solid, high resolution chars; fully formed descenders permit printing below line with no paper movement and no decrease in throughput speed. Terminal includes a 9 x 11 font that prints both std and high resolution copy at 10 chars/in (3.9/cm) and a 5 x 7 font that produces 16.75 chars/in (6.6 char/cm) compressed print. By using software control, two 24 x 80 format pages can be printed side-by-side. Character sets include Japanese, Arabic, Greek, and Italic. Modem options are available. **Computer Transceiver Systems Inc,** E 66 Midland Ave, Paramus, NJ 07652.
Circle 277

Dual-mode printer

DIP-95 series of 9-wire impact printers has switch-selectable 9 x 9 matrix processing mode and a 11 x 9 correspondence mode. Six character sizes and 1- or 2-pass printing are user specified. Offering bidirectional printing, tractor/friction paper feed, continuous loop ribbon cartridge, variable line density, and continuous form length control, printer also features high resolution dot addressable graphics and special effects symbols. Baud rate up to 9600, parallel and serial RS-232-C transmission control, X-ON/X-OFF, std 1k FIFO character buffer, and full 96-char ASCII set are std. **DIP, Inc,** 745 Atlantic Ave, Boston, MA 02111.
Circle 278

Voice storage subsystem

Modular voice storage subsystem designed for communications and computer systems, the VoiceStor™ is easily integrated with communication systems to provide voice store and forward, advanced calling, and voice prompting. Subsystem relies on voice recording for its vocabulary and phrases; incorporated systems respond in human tones, complete with variations in timing and inflection. Changes in stored words and phrases and in the voice used are made onsite with no special equipment or setup required. Storage options include 100 to 200 s of onboard RAM for simple voice prompting and short term voice storage applications; digital tape cassette for permanent backup of std vocabularies; and 3 disk subsystems that can be configured to provide from 4 to 80 h of vocabulary, phrase, and message storage. Design permits expansion from 8 to 32 simultaneous I/O transactions, and storage of up to 24k messages, phrases, or words. Multiple microprocessors handle all I/O control, voice conversion, and memory management functions. **Voicetek Corp,** 15 Soldiers Field Pl, Brighton, MA 02135.
Circle 279

Announcing new standards for image processing.

COMTAL's new low cost, standard systems

COMTAL leads the way again. Now, COMTAL offers standard versions of its Vision One/10 and Vision One/20. For as little as $33,250, you can have a full-scale, real-time digital image processing system — with delivery in less than sixty days!

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COMTAL's new standard systems, the Vision One/10-M6 and the Vision One/20-M8, represent major breakthroughs in price and delivery for digital image processors. Because of COMTAL's continuing technical leadership in the industry, vigorous expansion in the market, and the economies of scale through expanded manufacturing facilities, only COMTAL can make this kind of offer.

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COMTAL's new standard systems perform maturely. Each can operate as a real-time, stand-alone or host-interfaceable system. Each provides real-time roam and zoom, pseudocolor processing, and contrast stretching. Even the operating systems are standard! The Vision One/10-M6 is a compact, table-top system. The Vision One/20-M8 is a more powerful system with a larger memory capacity, a second user channel capability, and a broader range of options.

From the leader

With these new, economical standard systems, COMTAL advances its tradition of innovative leadership in image processing. Only COMTAL can offer this combination of performance, price and predictable delivery. Check it out.

With the cost of digital image processing lower than ever before, isn't it time to explore how digital image processing can help you? Call or write today and learn how you can have a new standard for your image processing and analysis needs.

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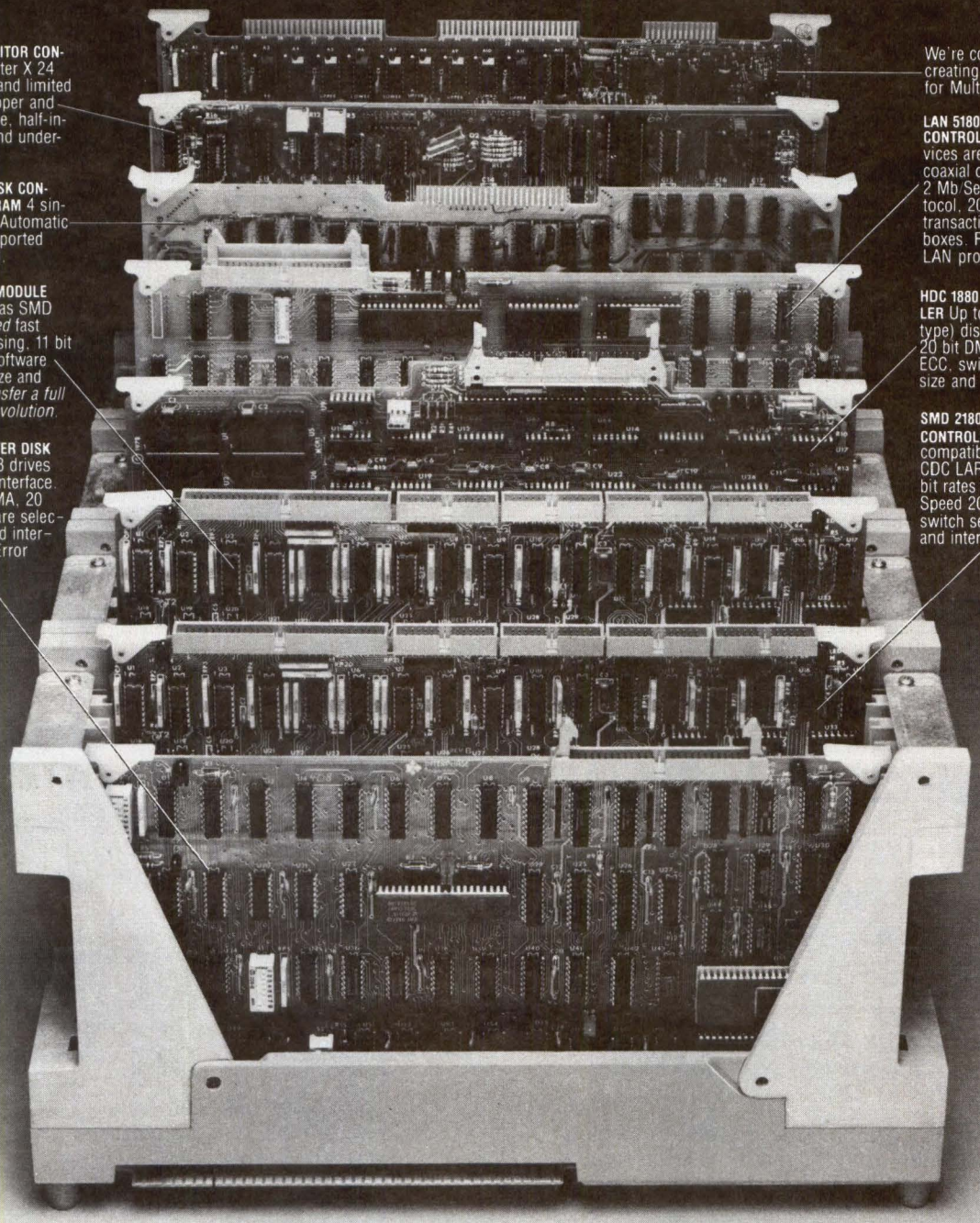
CIRCLE 119

More Multibus.™ And less.



VMC 186 VIDEO MONITOR CONTROLLER 80 Character X 24 line alphanumeric and limited graphic display. Upper and lower case. Reverse, half-intensity, flashing, and underline attributes.

FDC 1680 FLOPPY DISK CONTROLLER WITH 16K RAM 4 single density drives. Automatic DMA into the dual-ported on-Board 16K RAM.

SMD 2181 STORAGE MODULE CONTROLLER Same as SMD 2180 except *damned* fast DMA 24 bit addressing, 11 bit Error Correction, software selectable sector size and interleave. *Can transfer a full track in one disk revolution.*

WDC 2880 WINCHESTER DISK CONTROLLER Up to 8 drives with ANSI X3T9.3 interface. Very high speed DMA, 20 bit address. Software selectable sector size and interleave factor. 11 bit Error Correction.

We're constantly at work creating new capabilities for Multibus.

LAN 5180 LOCAL AREA NETWORK CONTROLLER Up to 255 devices are supported on a coaxial cable. Data rates up to 2 Mb/Sec. SDLC/HDLC protocol, 20 bit DMA, automatic transaction completion, mailboxes. First in a family of LAN products.

HDC 1880 HARD DISK CONTROLLER Up to 4 cartridge (5440 type) disk drives. High speed 20 bit DMA. Automatic Retry, ECC, switch selectable sector size and interleave.

SMD 2180 STORAGE MODULE CONTROLLER Up to 4 SMD compatible drives (including CDC LARK), 8-300 MBytes, bit rates to 20 Mb/S. High Speed 20 bit DMA, ECC, switch selectable sector size and interleave.

Now, the most talented Multibus specialists in the country bring you more Multibus options than ever before. And less.

More technology with less risk. More function with less cost. And more support with less hassle.

When you're ready to expand your Multibus capabilities, talk to us. We're the specialists who give you more. And less.

Entire rigid disk controller family is software interchangeable. Automatic completion of simple multisector commands, automatic recovery from errors, bad track mapping, full sector buffering, extensive diagnostic reporting. Variable burst DMA in 8 or 16 bit systems. Software drivers and disk subsystems also available.

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CIRCLE 120

Dot matrix printer with one print hammer

GP100 impact printer has single print hammer (Uni-Hammer) rather than 7 or more individual solenoids and print wires found in conventional dot matrix printers. Printer uses std fanfold paper, up to 9.5″ (24.1 cm) width and allows dot graphics, alphanumeric chars, and double-width chars to be mixed within a single line. Unit uses a rotating platen with protruding lengthwise splines, positioned behind the paper. Character or graphics image is formed by multiple hammer strikes in rapid succession as the printhead advances across the paper in front of the rotating platen. A precision gear train assures exact positioning of the print hammer relative to the splines on the platen, providing print quality and uniformity of the 5 x 7 matrix. Interface options are available. Printer is priced at $398. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340.

Circle 280

Color display station

Model 279 color display station is a 4-color, plug compatible replacement for IBM 3279/2A keyboard display. The keyboard station requires no controller or system changes for displaying alphanumeric data with colored fields. Features include nonglare screen, moveable keyboards with single-key clear, and program function keys. Options include row and column indicator, keystroke counter, and response time indicator. Station operates in existing 3274/3276 environments, and also is compatible with the company's 278 displays or IBM 3278 displays in the same cluster. It attaches to either a Telex 276 or IBM 3274/3276 controller. High resolution monitor displays up to 1920 chars on a 9 x 14 dot matrix. Operator selectable switch enables operation in a 2-color normal or high intensity mode as a Telex 278 or IBM 3278 equivalent. **Telex Computer Products, inc,** 6422 E 41st St, Tulsa, OK 74135.

Circle 281

Dolch.

advanced logic analysis

48 to 96 Channels, 300 MHz, plus Mnemonics

Order up your parameters. Dolch's LAM 4850A logic analyzer makes it easy with a new key — Monitor. Monitor gives you status information and comments on menu setups, and can be called up at any time to interpret each parameter, its range, and its interaction with the current setup. And, you can store your setups for three months without power, eliminating the need to reprogram.

Zero in fast. The LAM 4850A disassembles your code into Mnemonics and gives you the channels you need to trace data, address, port and control lines. And for future needs, you can expand to 64, or even 96, channels.

Hook up fast, too. Dolch personality probes clip right over your CPU chips so you don't waste time connecting dozens of individual hooks. And the probe takes care of clock, timing and signal interfacing — no need to worry about signal conditions.

300 MHz sampling across 16 channels. A revolutionary option gives you the ultimate in sampling resolution — 3.3 ns — to help you solve the toughest timing and phase related problems. A unique memory overlay configuration provides simultaneous dual asynchronous recording across 16 channels without compromising any of the LAM 4850A features.

Don't settle for less than Dolch. The basic LAM 4850A is truly a universal logic analyzer system with 50 MHz sampling rate, 1000 bits per channel source and reference memories, and sophisticated sequential trigger and multilevel clocking.

For details on the Dolch LAM 4850A, or any of our other troubleshooting tools, write: Dolch Logic Instruments, Inc., 230 Devcon Drive, San Jose, CA 95112. Or call toll free: (800) 538-7506; in California call (408) 998-5730.

dli DOLCH LOGIC INSTRUMENTS

Circle 123 for Demonstration
Circle 130 for More Information

Portable alphanumeric terminal

TransTerm 2 compact terminal is intended for portable and/or remote communication environments. Terminal consists of a single-line 80-char LCD display and a 58-key TTY style membrane, alphanumeric keyboard packaged in a 1.75″ x 12.75″ x 6.9″ (4.45- x 32.39- x 17.5-cm) case. Unit communicates in full-duplex RS-232 serial asynchronous ASCII with 20-mA current loop or optional RS-422. One of 8-baud rates (110 to 9600 baud) can be switch-selected, along with parity (even/odd/mark/space) at 7 bits/char. Terminal has memory capacity of 24 lines displayed data that can be locally viewed under operator control. Three switch-selectable operating modes provide TTY compatibility, block send mode, or multidropped/polling operation for up to 32 units. Optional features include memory up to 12k bytes, a 40-col alphanumeric printer, and battery powered operation. Terminal is equipped with 115-Vac plug-in power transformer, and it can also be powered by a 7- to 15-Vdc external supply. **Computerwise, Inc**, 4006 E 137th Terrace, Grandview, MO 64030.

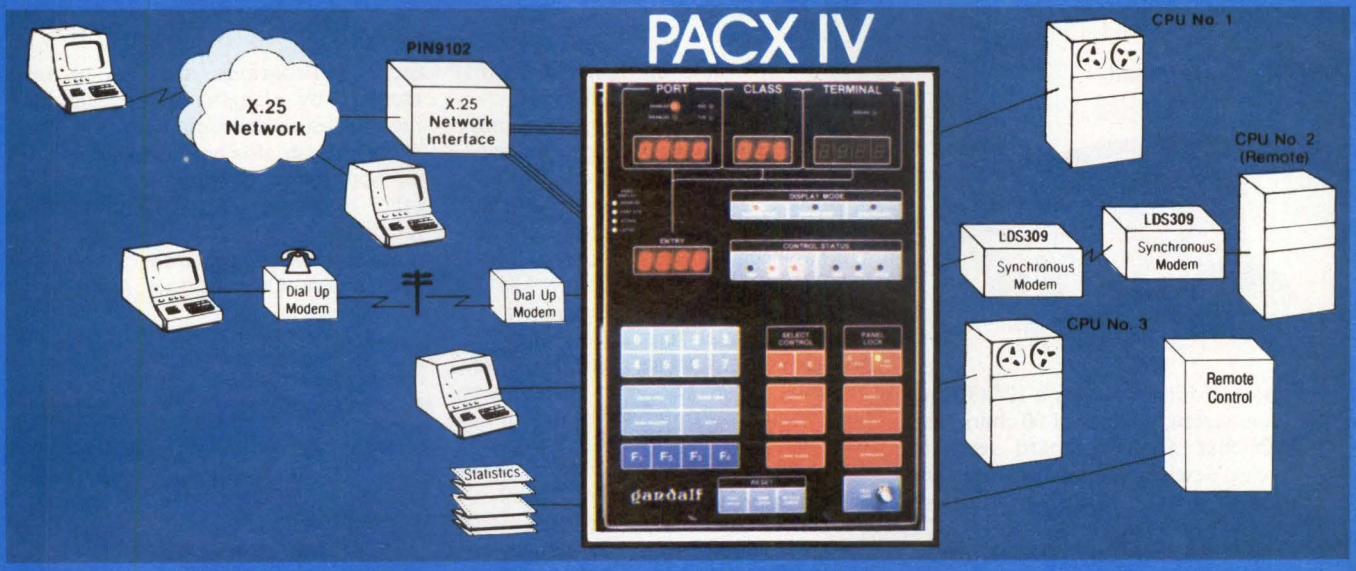
Circle 282

General purpose monitor

Off-the-shelf 9″ (23-cm) monochrome video monitor model 9VM967 is designed for surveillance control systems, industrial remote installation, and VTR playback applications. Unit features silicon transistorized circuitry, single chassis construction, high reliability, and easy maintenance. Front panel controls include brightness, contrast, vertical hold, horizontal hold, and on/off switch. Bandwidth is in excess of 10 MHz and horizontal resolution is 700 lines at center. Geometric distortion is less than ± 5% of display height. Input power required is 30 W at 120 Vac; all performance specs are met with line voltages between 105 and 132 Vac. A 240-Vac, 50-Hz model is also available. **Audiotronics Corp**, 7428 Bellaire Ave, North Hollywood, CA 91605.

Circle 283

Switch into tomorrow...



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Today multiple terminal users can switch and contend for multiple resources using Gandalf PACXs (Private Automatic Computer eXchangers). PACX IV meets your contention and switching needs **today.**

All Gandalf PACXs are compatible with each other. Easily expandable,too. Modular design allows for your needs **tomorrow.**

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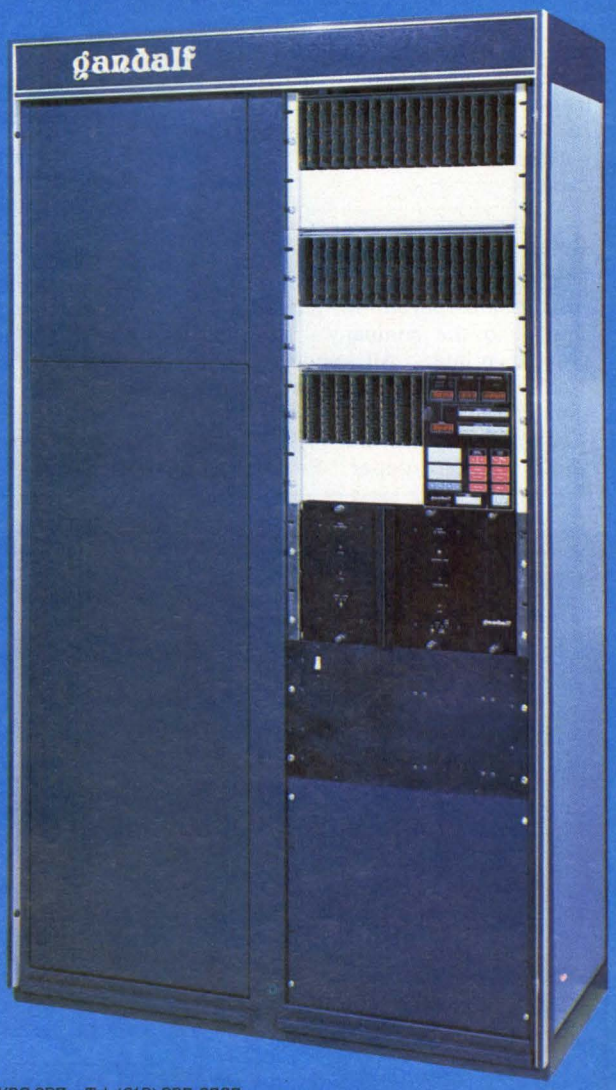

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Subsidiaries of Gandalf Technologies, Inc.

CIRCLE 125

2000-char terminal

100 series terminals employ a 12″ (30-cm) terminal screen, 24 lines of 80 chars, and full 96-char ASCII keyboard set with lowercase descenders. A 25th status line gives a total of 2000 displayable positions, each of which can display 1 of 2 switch- or software-selectable char sets. Protected fields appear in half-intensity and cannot be altered while in protect mode. Optionally, either the entire screen or only non-protected fields are transmitted when in protect mode. **JONOS Ltd,** 920-C E Orangethrope, Anaheim, CA 92801.
Circle 284

Color graphics printers

Models GC8000 and HR8002 color graphic printers incorporate ink jet technology similar to the company's IS8001 color graphic printer. All models produce 7-color hardcopy with 90-dot/in resolution and print a 10.7″ x 8″ (27.2- x 20-cm) display on std 14.9 (37.8-cm) width fanfold paper. Each version utilizes replacable ink cartridges sufficient for approximately 500 copies.

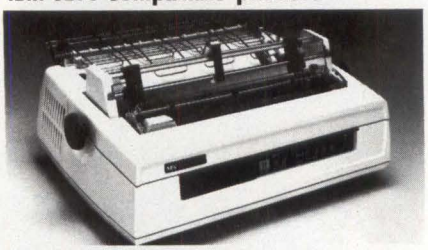
GC8000 transforms a host's memory resident color graphic image into hardcopy format. Unit accepts data through a std RS-232-C I/O port with a transmission time of 9 s. After the graphic image has been stored in memory, unit is able to print up to 255 copies while the host is free for further processings.

HR8002 printer/terminal is designed primarily to interface with Intelligent Systems 8001-H series microcomputers and terminals. Printer can be driven as a terminal, allowing the user to write directly into the internal display buffer. Expanded graphics software is available to increase plotting power. Additional features include downline loadable set of 512 graphics chars. **PrintaColor Corp,** PO Box 52, Norcross, GA 30071.
Circle 285

High capacity handheld computer

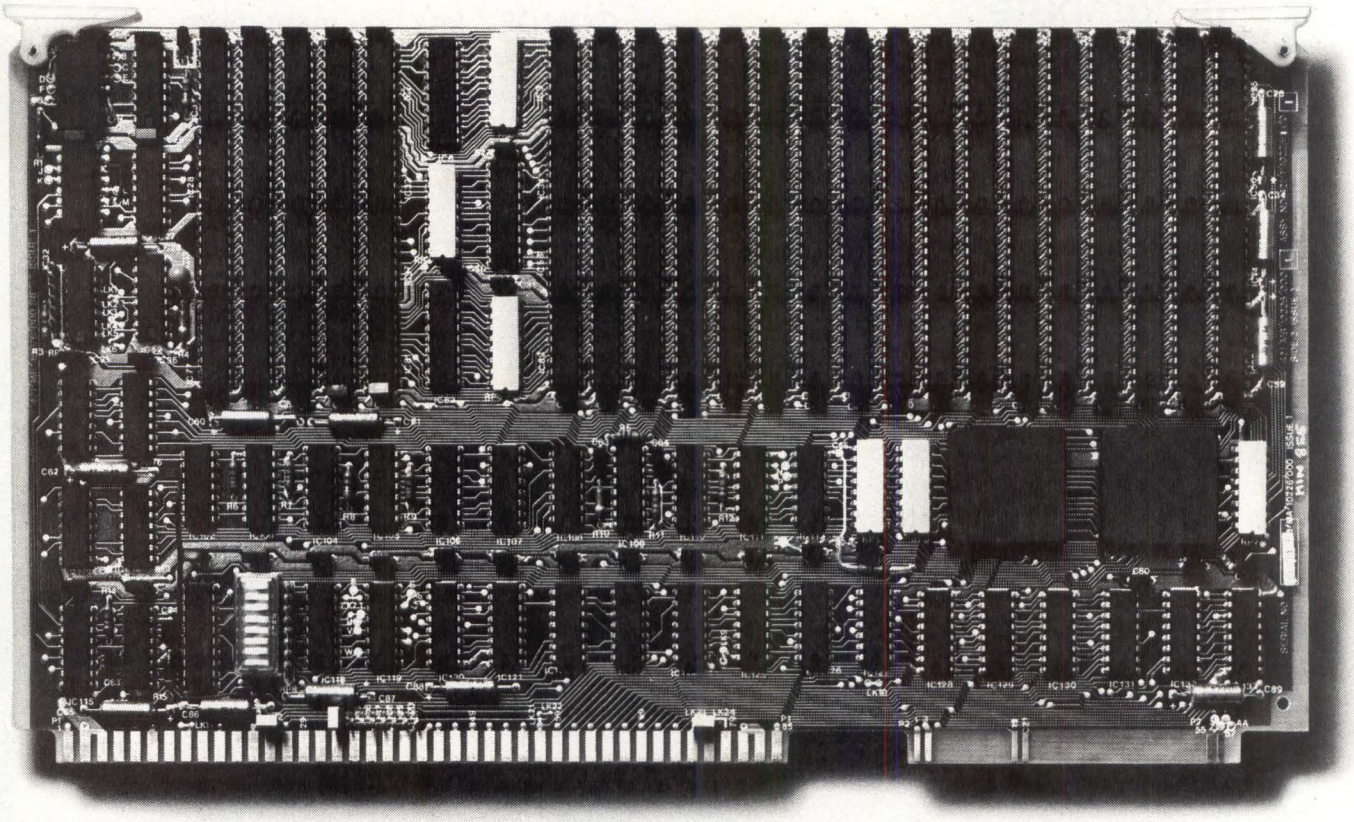
Self-contained, battery powered, programmable terminal MSI/88S can be equipped with up to 112k RAM for program and data storage. RAM is coupled with 8k-byte ROM that stores the terminal operating system, controlling load and execution of application programs. Features include a 2-line, 32-char LCD alphanumeric display and a choice of either CMOS or HMOS memory configurations. Display permits scrolling data, the use of prompts, and realtime clock displayed on one line with data on the second. Programs are loaded into memory by plugging a program load module into the communication port. Terminal can also be downloaded from an application development system or other host computer, either directly or remotely via an extended communications module. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626.
Circle 286

IBM 3270 compatible printers



Printer line features IBM 3270 compatible printer systems with 3 letter quality printers. Several serial dot matrix systems with print speeds from 120 chars/s to 300 lines/min, and band printers operating from 300 to 1800 lines/min are also available. Printers are hardware and software compatible with both Type A and Type B equipment. Quick forms access, tighter char pitch to save paper, and quiet operation are featured. Printers are priced 10% to 50% less than IBM equivalent models. **Printer Systems Corp,** 1 W Deer Park Rd, Gaithersburg, MD 20760.
Circle 287

512[K] Multibus memory with ECC: $1,750.*



*Quantity price good for one evaluation unit per customer, ordered on company letterhead or P.O.

Sure it's a ploy.

We figure you'll like the 50% we shaved off the list price, so you'll buy a PSM-512.

You'll figure it's a great way to get the storage you need to develop that 8086, 68000 or other 16-bit micro-based system of yours.

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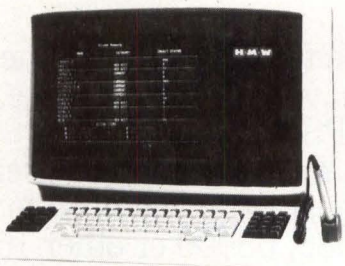
CIRCLE 128

IBM compatible color terminal

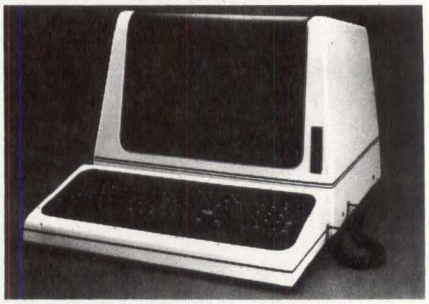
Model 9070 color terminal is a plug compatible replacement for IBM 3275-2. No software changes are required to output a data page of 5 colors. Color sorting of data is determined by programmed field attributes. High resolution, permanently converged CRT provides color saturation, focus, and spot size. Free standing solid state keyboard features N-key rollover, 12 program function keys, and 2 program action keys. Terminal can be configured as an integrated workstation. Terminal supports 2 serial ASCII printers. Printer ports are individually buffered, allowing keyboard interaction while the print cycle is active. Printers range from 50-chars/s daisy wheel terminals to 600-lines/min line printers. Options include lightpen and internal modem. **HMW Enterprises, Inc**, 604 Salem Rd, Etters, PA 17319.



Circle 288

VT100/VT132 emulation terminal

Designed for 80- or 132-col formats, model 3132 video display terminal features high resolution 15″ (38-cm) screen, and is plug compatible with DEC VT100, VT131, and VT132 systems. Printer port, detachable keyboard, 256-char receive buffer, and line/char insert and delete editing are featured. Terminal has 18 programmable function keys with storage of up to 96 chars. Screen displayed prompt legend allows selection of operating parameters; reverse video, blink, and underline are std. Batch transmissions include line, partial, or full screen. RS-232-C communications, selectable baud rates from 50 to 19.2k, and full-duplex and selectable local echo are provided. Self-test diagnostics are provided. **Cobar, Inc**, 1181 N Fountain Way, Anaheim, CA 92806.



Circle 289

Relief for terminal headaches.

Panasonic believes that terminal ergonomics should begin at the CRT screen. Fuzzy characters, excessive brightness, distracting glare and reflections can all lead to operator discomfort and "terminal headaches." That's why our newest monochrome and high resolution color CRTs are available with a team of innovations designed with "human factors" in mind: our new Super Dark high contrast screen and the famous Panasonic Direct Etch™ anti-reflection surface.

The Super Dark screen has been specially engineered for a high-contrast display that reduces operator fatigue caused by excessive brightness. The high contrast screen provides acceptable viewing at low brightness levels, so the CRT beam current is minimized and resolution is maximized. Characters are sharp, clear and easy to read. And the Super Dark screen helps reduce reflectance, while hiding normal long term screen burning too.

You can combine the Super Dark screen with our optional Direct Etch™ anti-reflection surface (available on most models), which effectively diffuses distracting ambient reflections without the drawbacks of bonded faceplates and plastic overlays. To minimize resolution loss, the screen glass is etched close to the phosphor; in tandem with the lower beam currents allowed by our Super Dark screen, resolution can actually be better than that of most conventional polished glass tubes. And operator comfort is much greater.

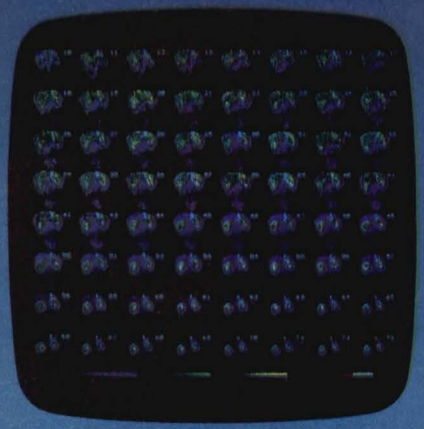
Super Dark Screen and Direct Etch™ are available on all popular-sized Panasonic data display tubes, including our affordable new high resolution in-line color CRTs. We're the CRT source to relieve everyone's terminal headaches. For prices and complete information, write Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, NJ 07094; or call (201) 348-5278.

Panasonic CRT screen ergonomics: Super Dark Screen and Direct Etch™.

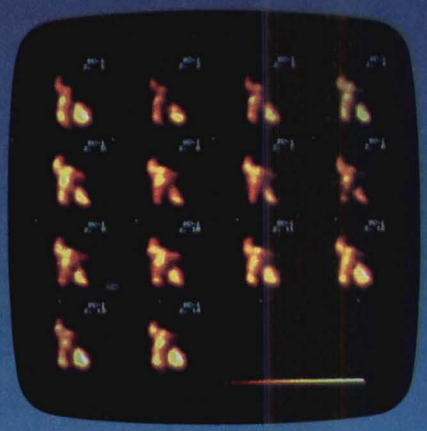
Panasonic®
just slightly ahead of our time

CIRCLE 131

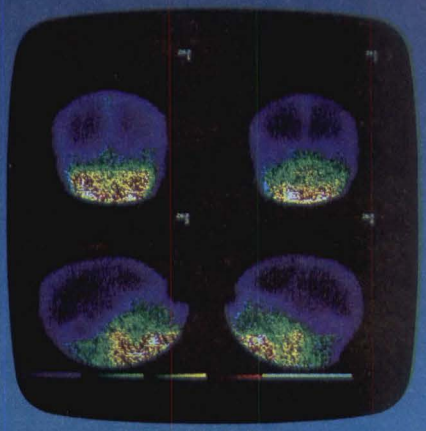
How to display nuclear medicine ...with some help from Grinnell.



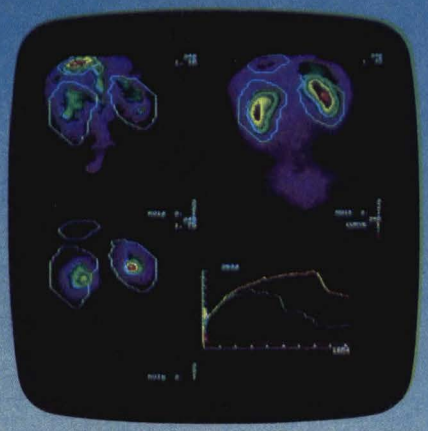
64 frames of a dynamic study
of the kidneys collected using varying frame rates



Gated cardiac study
using optional color scale



Static Brain Scan



Regions of interest drawn simultaneously in three quadrants with resulting time-activity curves in fourth quadrant

Frozen frame during cine mode
of gated cardiac data

When Nodecrest Medical Systems needed help in displaying high resolution, gamma camera color images rapidly, under enhanced conditions, they turned to Grinnell and the GMR 270 Image Processing System.

The GMR 270 is a powerful, high speed, modular system that meets almost any medical imaging requirement. Key features include:

- Real time digitizing of video information with up to 256 levels of grey scale or full color
- Displayable resolutions of 512 × 512 pixels with window display of 1024 × 1024 pixel images
- Split-screen, image toggling and host-loadable video function memories for contrast enhancement, ratioing and gamma correction
- Real time multiple image processing for enhancement, filtering, transformations and convolutions
- High speed image loading and switching to create "movie-type" displays
- Non-destructive pan and zoom of stored images
- Overlay display of image intensity distribution
- Graphic overlays with character, vector and rectangle generators
- Fortran-callable subroutines for easy implementation of application-oriented image processing

All of these and more, are available in competitively priced, modular systems that can include high performance display monitors and single or dual-port interfaces for most minicomputers. For details and/or a quotation, call or write today.

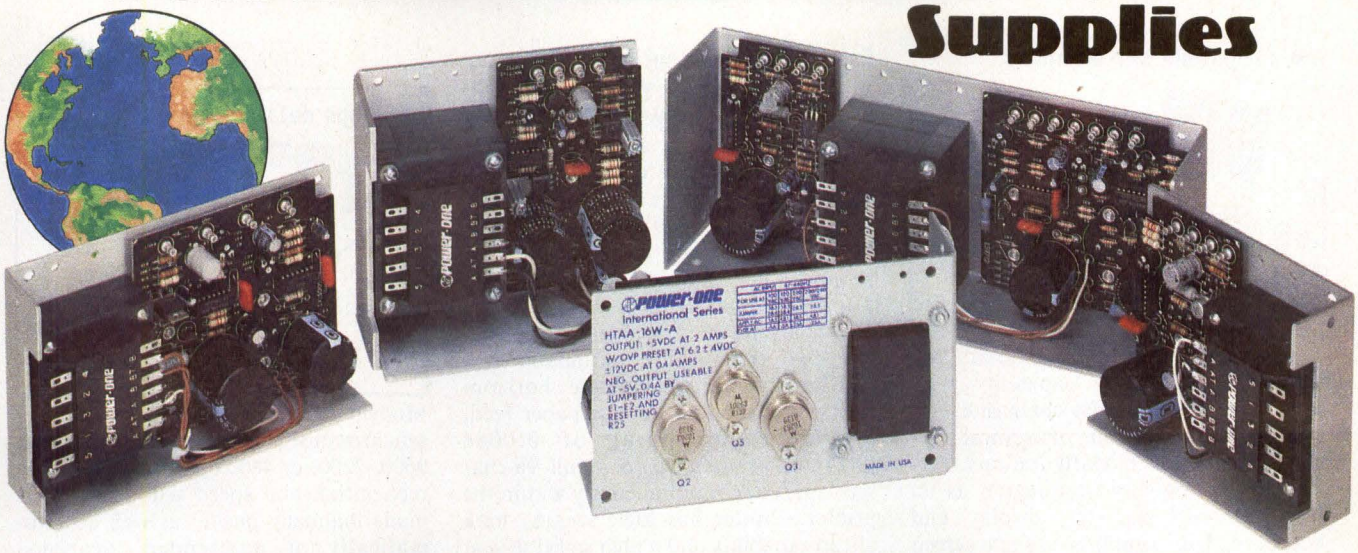
GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920 TWX 910-338-2145

Photos: Courtesy Nodecrest Medical Systems.

CIRCLE 132

Power One's International Series-The New World Standard in D.C. Power Supplies



One Power Supply for the Whole World

At last... a world standard in high reliability open-frame power supplies. Designed specifically for products sold throughout the world to make your international marketing simpler. And more profitable.

Meets International Safety Requirements, Worldwide

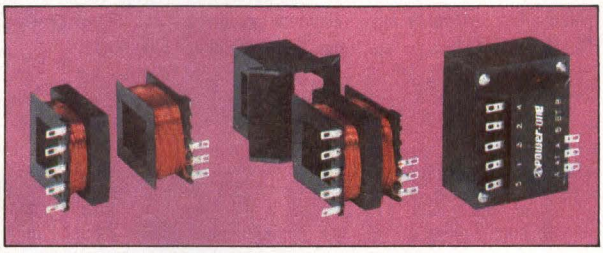
The International Series can be used anywhere, for almost any application. It's the only power supply available that meets the most important requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA. This was achieved by using our new patented winding process featuring separate, fully enclosed primary and secondary windings. This unique construction complies with worldwide safety standards, including:

Leakage Current, Line to Ground: 5.0 μa
Spacings, Live Parts to Dead Metal: 9.0 mm
Other than Field Terminals: 5.25 mm

Dielectric Withstand Voltage,
Input to Ground: 3750 VAC
Input to Outputs: 3750 VAC
Outputs to Ground: 500 VAC

Wide Choice of AC Input Power

Each unit is rated at 100, 120, 220, 230, and 240 volts, 47 to 63 Hz. So wherever your products are headed, one standard off-the-shelf power supply will serve. No more costly stocking of different units for different destinations.



Power-One's patented International Series transformers feature separate, fully enclosed, primary and secondary coils. Meets safety requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.

SINGLE OUTPUT MODELS		
MODEL	**VOLTAGE/ CURRENT**	**PRICE (1-24)**
5 VOLTS		
HB5-3/OVP-A	5V @ 3A	$ 32.95
HC5-6/OVP-A	5V @ 6A	$ 54.95
HN5-9/OVP-A	5V @ 9A	$ 74.95
HD5-12/OVP-A	5V @ 12A	$ 84.95
HE5-18/OVP-A	5V @ 18A	$119.95
12 VOLTS		
HB12-1.7-A	12V @ 1.7A	$ 32.95
HC12-3.4-A	12V @ 3.4A	$ 49.95
HN12-5.1-A	12V @ 5.1A	$ 69.95
HD12-6.8-A	12V @ 6.8A	$ 79.95
HE12-10.2-A	12V @ 10.2A	$109.95
15 VOLTS		
HB15-1.5-A	15V @ 1.5A	$ 32.95
HC15-3-A	15V @ 3A	$ 49.95
HN15-4.5-A	15V @ 4.5A	$ 69.95
HD15-6-A	15V @ 6A	$ 79.95
HE15-9-A	15V @ 9A	$109.95
24 VOLTS		
HB24-1.2-A	24V @ 1.2A	$ 32.95
HC24-2.4-A	24V @ 2.4A	$ 49.95
HN24-3.6-A	24V @ 3.6A	$ 69.95
HD24-4.8-A	24V @ 4.8A	$ 79.95
HE24-7.2-A	24V @ 7.2A	$109.95

DUAL OUTPUT MODELS			
MODEL	**OUTPUT #1**	**OUTPUT #2**	**PRICE (1-24)**
±12 TO 15 VOLTS			
HAA15-0.8-A	12V @ 1A OR 15V @ 0.8A	-12V @ 1A OR -15V @ 0.8A OR -5V @ 0.4A	$ 42.95
HBB15-1.5-A	12V @ 1.7A OR 15V @ 1.5A	-12V @ 1.7A OR -15V @ 1.5A OR -5V @ 0.7A	$ 54.95
HCC15-3-A	12V @ 3.4A OR 15V @ 3A	-12V @ 3.4A OR -15V @ 3A	$ 87.95
HDD15-5-A	12 TO 15V @ 5A	(-) 12 TO 15V @ 5A	$129.95
5 VOLTS PLUS 9 TO 15 VOLTS			
HAA512-A	5V @ 2A	9 TO 15V @ 0.5A	$ 49.95
HBB512-A	5V @ 3A	9 TO 15V @ 1.25A	$ 59.95
HCC512-A	5V @ 6A	9 TO 15V @ 2.5A	$ 94.95

TRIPLE OUTPUT MODELS				
MODEL	**OUTPUT #1**	**OUTPUT #2**	**OUTPUT #3**	**PRICE (1-24)**
HTAA-16W-A	5V @ 2A	9 TO 15V @ 0.4A	(-)9 TO 15V @ 0.4A OR -5V @ 0.4A	$ 54.95
HBAA-40W-A	5V @ 3A	12V @ 1A OR 15V @ 0.8A	-12V @ 1A OR -15V @ 0.8A OR -5V @ 0.4A	$ 75.95
HCAA-60W-A	5V @ 6A	12 TO 15V @ 1A	(-)12 TO 15V @ 1A OR -5V @ 0.4A	$ 89.95
HCBB-75W-A	5V @ 6A	12V @ 1.7A OR 15V @ 1.5A	-12V @ 1.7A OR -15V @ 1.5A OR -5V @ 0.7A	$ 99.95
CP131-A	5V @ 8A	12V @ 1.7A OR 15V @ 1.5A	-12V @ 1.7A OR -15V @ 1.5A OR -5V @ 0.7A	$119.95
HDBB-105W-A	5V @ 12A	12V @ 1.7A OR 15V @ 1.5A	-12V @ 1.7A OR -15V @ 1.5A OR -5V @ 0.7A	$134.95

SINGLE OUTPUT MODELS		
MODEL	**VOLTAGE/ CURRENT**	**PRICE (1-24)**
28 VOLTS		
HB28-1-A	28V @ 1A	$ 32.95
HC28-2-A	28V @ 2A	$ 49.95
HN28-3-A	28V @ 3A	$ 69.95
HD28-4-A	28V @ 4A	$ 79.95
HE28-6-A	28V @ 6A	$109.95

New International Series Models

DISK DRIVE MODELS				
MODEL	**OUTPUT #1**	**OUTPUT #2**	**OUTPUT #3**	**PRICE (1-24)**
CP205-A	5V @ 1A	-5V @ 0.5A	24V @ 1.5A/1.7A PK	$ 75.95
CP206-A	5V @ 2.5A	-5V @ 0.5A	24V @ 3A/3.4A PK	$ 99.95
CP162-A	5V @ 3A	-5V @ 0.6A	24V @ 5A/6A PK	$129.95
CP323-A	5V @ 2A	12V @ 4A		$ 79.95
CP379-A	5V @ 6A	-5V @ 1.2A OR -12V @ 1.2A	24V @ 3.5A/8A PK	$129.95
CP384-A	5V @ 9A	-5V @ 1.2A OR -12V @ 1.2A	24V @ 2A/8A PK	$129.95

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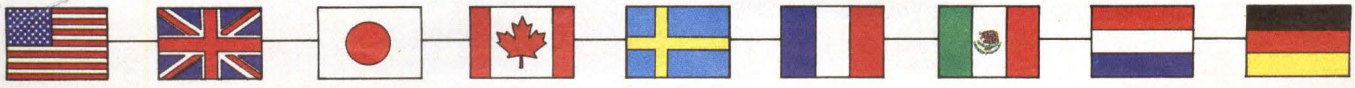
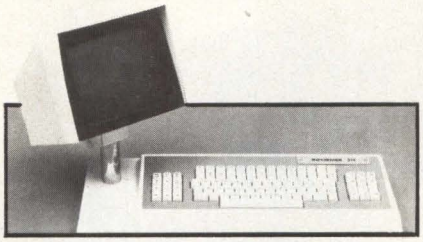
Power-One, Inc. • Power One Drive • Camarillo, CA 93010 • Phone: 805/484-2806 • 805/987-3891 • TWX: 910-336-1297



CIRCLE 133

IBM compatible CRT terminals



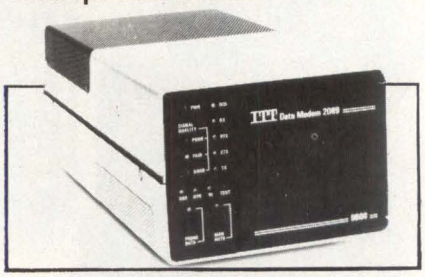
Model 314 series CRT terminals are IBM 3275-2 compatible and include a 25th status line, interface capability with serial printers, and daisy chain interface to permit connection of several terminals in multidrop configurations. Terminal has capability to function as an IBM 3271 with one 3277 display and keyboard. Unit supports std 3270 screen attributes and printer port functions. Series is designed to communicate with IBM host systems via multipoint binary synchronous communications protocol through std synchronous modems at speeds up to 9600 bps. **Informer, Inc,** PO Box 91054, Los Angeles, CA 90009.
Circle 290

Expanded printer series

A fully modular, field upgradeable 96-char dot matrix printer that utilizes add-on options for a wider range of applications, the 80-col Prism 80 yields correspondence quality print in an overlapping 24 x 9 matrix. Printing bidirectionally at up to 150 chars/s for proportionally spaced chars, the device allows densities of 10, 12, or 16.8 chars/in, plus double-width chars. Std features include automatic text justification, programmable horizontal/vertical tabbing, reverse paper feed, and fine positioning of 0.008″ (0.21-mm) chars. Up to 4 full 96-char sets can reside simultaneously within the printer. Printer has logic seeking look ahead capability and a high speed slew at line termination to maximize throughput. It has std RS-232-C serial interface as well as Centronics compatible parallel interface. Serial transmission rates from 300 to 9600 baud are switch-selectable. **Integral Data Systems, Inc,** Milford, NH 03055.
Circle 291

DATA COMMUNICATIONS

9600-bps data modem



Modem 2089 transmits and receives data synchronously on voice grade lines at 9600, 7200, or 4800 bps. Automatic rate recognition and speed selection can be made manually onsite, as well as automatically at unattended locations. Modem functions half-duplex over 2-wire public switched telephone networks, or full-duplex using 2 dialed lines. In leased line operation, modem functions half-duplex via 2-wire interconnect, or full-duplex when a 4-wire circuit is used. Unit incorporates a dial
(continued on page 236)

DILOG DISC & TAPE COMPATIBLES FOR DEC-11*

DILOG offers the widest range of single board DEC emulating disc and magnetic tape controllers for LSI-11, 11/2, 11/23, PDP-11 and VAX-11 compatibility.

DILOG/DEC controllers:

DISC

- Winchester—5¼", 8" and 14"
- SMD—Storage Module
- CMD—Cartridge Class
- Lark—Cartridge Class
- 2315/5440 Cartridge Class
- Flexible Disc

MAGNETIC TAPE

- ½" reel-to-reel NRZI/PE—Streaming or conventional
- ¼" 3M Cartridge

A wide range of emulations are offered. All fully supported by DEC operating systems.

If you're interfacing *any* popular drive to *any* DEC-11 computer, contact DILOG for the largest selection of DEC-11 compatible disc and magnetic tape controllers! Over 20 available now. Several more to be announced soon.

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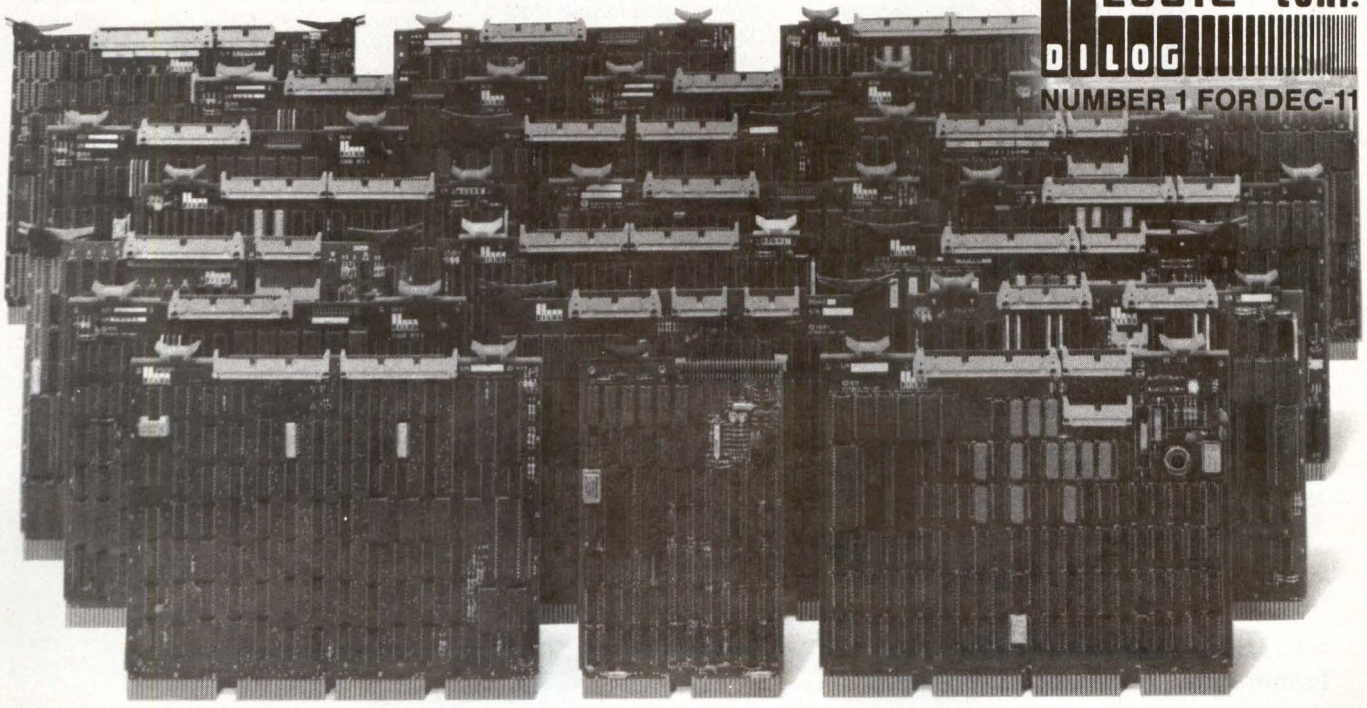
NUMBER 1 FOR DEC-11



*Trademark Digital Equipment Corp.

CIRCLE 135

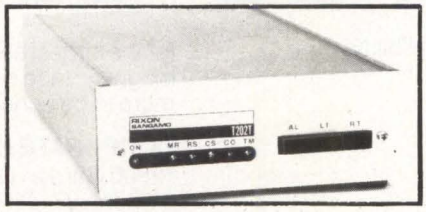
backup feature for line restoration and an automatic adaptive equalizer, providing a dynamic range of more than 40 dB. RTS/CTS turnaround is 27 ms, accomplished by strap option added to the modem's 253-ms RTS/CTS time. Option allows max efficiency in polled multidrop networks.

All main functions are controlled by an array of 4 microprocessors, allowing the modem to be software adapted. Built-in local and remote diagnostics include test loops and bit error measurements. Modem conforms fully to CCITT V.29 at all 3 speeds on 4-wire lines; digital interface with terminal equipment meets CCITT V.28 and V.24 (EIA equivalent RS-232-C). 25-pin interface connector arrangements are based on CCITT recommendation V.54. **ITT Corp, Data Equipment and Systems Div**, One World Trade Center, New York, NY 10048.

Circle 292

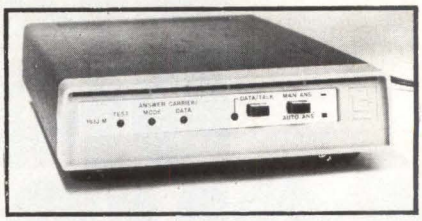
1.8k-bps asynchronous data modem

T202T data modem transmits and receives serial binary data up to 1800 bps asynchronously half-duplex over 2-wire, or full-duplex over 4-wire type 3002 or equivalent private lines. The LSI modem is compatible with Bell 202 type modems and 829 data auxiliary sets. Modem can be equipped with a 387-Hz reverse channel with signaling rates up to 5 bps. Reverse channel option allows simultaneous 2-way transmission on 2-wire facilities and can be used as a supervisory signal for error detection and control. Reverse channel can also be used to inform the transmitting modem that a signal is being received. Six front panel LEDs used in conjunction with 3 front panel pushbutton switches enable testing of the modem, terminal, and private line. Test features include analog loopback, local self-test, and remote test. Unit is available as either desktop standalone or card assembly for rackmount configurations. **Rixon Inc**, 2120 Industrial Pkwy, Silver Spring, MD 20904.



Circle 293

300-bps personal computer modem



Modem 103J-M, designed for home and small business computers, automatically answers incoming calls, or can be switched to manual operation. Unit operates over all dial telephone lines, and is fully line compatible with Bell equivalent 103/113 modems, and 212A units operating at 300 bps. Modem is equipped with both analog and digital loopback diagnostic test functions. Individual LEDs report operating modes, test functions, and data transmissions. Modem accepts a std modular telephone connector and 25-pin connector supplied with the data equipment. Options include call answering and terminating through the computer terminal. **General DataComm Industries, Inc**, One Kennedy Ave, Danbury, CT 06810.

Circle 294

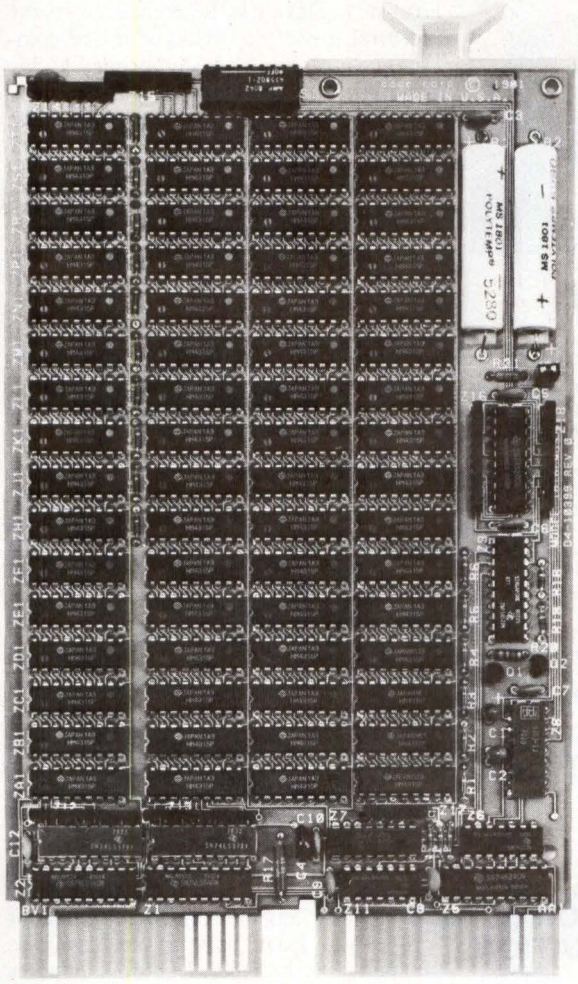
Bell 212A compatible modems

MT212A is a dual-speed 1200- and 300-bps replacement modem for the Bell 212A. MT212D is a 1200-bps only version with full 212A compatibility. Both modems provide full-duplex operation over dial-up lines, asynchronous or synchronous. Modems are available in standalone and rackmounted configurations, and provide originating and automatic answering capability. Voice to data transferring is via a pushbutton on the modem chassis, eliminating the need for special 502 exclusion key phones and adaptors. For originating applications, the user's telephone set can be connected to the phone line using either RJ11 or RJ45 modular connections. MT212A is priced at $850; MT212D is $695. **Multi-Tech Systems, Inc**, 82 Second Ave SE, New Brighton, MN 55112.

Circle 295

Only from adac...

Non-volatile CMOS memory for LSI-11 retains data during power failure.



- 16K word ADD-IN memory replaces bulky core
- On-board battery back-up assures data retention up to a full week without external power
- Decodes 18 bit address and allows the RAM to start on any 4K boundary
- Low power consumption (5 W typical)
- High speed 450 ns memory chips
- Self-recharging battery
- Long 3 year battery life
- Write protection in 4K blocks—acts like ROM
- Easily accessible switches allow card to be write-protected while in rack

The 1816 CMOS memory is another LSI-11, LSI-11/2 and LSI-11/23 compatible device from ADAC. It is ideal when it's important not to lose data during power outages. And it requires only a fraction of the space and power of comparable core memory. Contact ADAC for full details on this unique memory or any of our analog and digital function cards and complete systems for LSI-11.

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CIRCLE 138

Telecommunications monocircuit

Monocircuit MC14403 single-chip codec/filter integrates codec, filter, and voltage reference into a 16-pin package with no external components needed. Industry std 300-mil package minimizes board area required to implement codec/filter/reference function of digital switches. Using linear CMOS technology, integration of precision voltage reference as part of a complex D-A CMOS LSI circuit is possible. Voltage reference allows use of 3.1-V peak full-scale analog voltage to improve dynamic range and signal to noise ratio limited to a 2.5-V full-scale voltage. Monocircuit uses Si gate CMOS process for power dissipation of 60 mW in active mode and 2 mW when phone is on hook. Device can be used in systems requiring either TTL or CMOS interface. Included are automatic prescale divide circuit to generate internal 128-kHz sampling frequency from the data clock. European and U.S. spec models are available. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 296

Remote communications monitor

Remote protocol monitor provides troubleshooting on remote data communications lines from a central site. Monitor is completely transparent to the existing system and can operate with any modem, multiplexer, or protocol. System has a master unit at a central site (RLM-M) and a slave unit at a remote site (RLM-S). Slave can be connected to the central RLM-S via dialed or leased communication line and is controlled by the master. Remote RLM-S scans the transmission and receives data channels, clock, and control status of line under test. Scanned data are stored in 16k-byte RAM and simultaneously sent to the central site RLM-S. Units can trigger or trap on a specific char and/or an RS-232 interface event. Error protected data stream is displayed at the central site monitor. **Digilog, Network Control Div,** 1370 Walsh Rd, Montgomeryville, PA 18936.

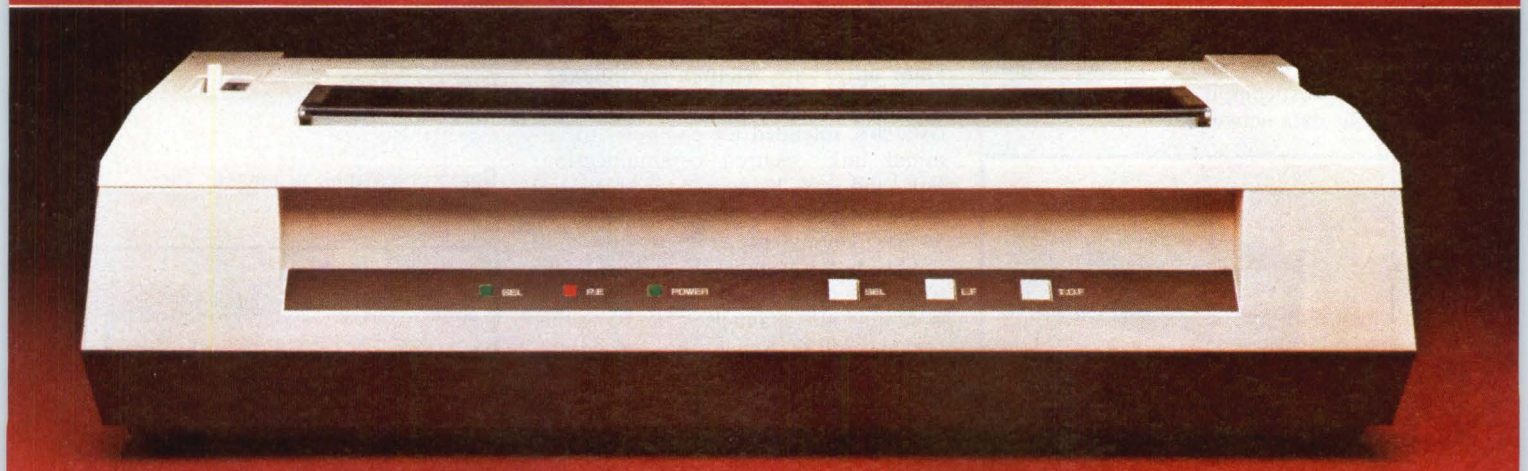
Circle 297

Communication buffer

DCS-8900 communication buffer for store and forward, protocol/format conversion, and data aquisition applications uses a Winchester disk as bidirectional FIFO message buffer to interface different baud rates and protocols. Optional IBM compatible tape drive provides a media compatible, removable data storage facility for source or destination. Buffer handles a mix of protocols, ranging from 50-baud Baudot to SDLC. Four basic input lines are expandable to 480. **Digital Computer Systems, Inc,** PO Box 180, Germantown, MD 20874.

Circle 298

8510A Pro/Writer



1550 Pro/Writer II

OUR LINE KEEPS GROWING WIDER.

C. Itoh's high-performance family of low-profile printers has grown bigger and better than ever. There's the Series 8500 Pro/Writer, our feature-loaded 8" compact with 120 cps print speed and 80-column capacity. And now there's Pro/Writer II, the new 15½" wide-track that prints up to 230 columns at a fast 120 cps print speed.

Both feature heavy duty castings and stepper motor, high reliability print mechanism, and a synthetic ruby print head that maintains a high print quality throughout its entire 100-million plus character life. No wonder Pro/Writers can deliver an estimated 15 months service (average use)—without a single failure.

You get consistent, correspondence quality printing too. Plus a long list of most-wanted features, including:

1. True incremental printing
2. Five unique alphabets, eight character sizes (two proportionately spaced)
3. Mixed fonts during a single line pass
4. Bidirectional, quick-cancel printing for higher throughputs than comparable printers spec'd at greater print speeds
5. Graphics mode with better resolution (144 x 160 dots per square inch) than many graphics plotters
6. Variable form length, six-channel electronic vertical formatting
7. Automatic vertical and horizontal tabbing
8. Bidirectional tractor and roll feed
9. 1K Byte buffer (expandable to 3K) for Series 8500 Pro/Writer. Pro/Writer II comes with 3K Byte buffer standard
10. Easy-load cartridge ribbon
11. Industry-standard parallel or serial interfacing with popular X/ON, X/OFF protocols

Pro/Writers are designed for easy maintenance throughout and feature "Microcomputer-on-a-board" technology and convenient, operator-replaceable print head. Result: Mean Time to Repair for a trained technician is just half an hour—worst case.

It all adds up to the dependability and high performance OEM's have been waiting for. C. Itoh's reliable Pro/Writer family of printers. It's growing wider all the time.

For full details, contact C. Itoh Electronics, Inc., 5301 Beethoven Street, Los Angeles, CA 90066. (213) 306-6700

C. ITOH ELECTRONICS, INC.

One World of Quality

DESIGNED FOR THE OEM

CIRCLE 140

Data routing switch

MULTI-SWITCH.25 routing device can forward data from an X.25 trunk to any other X.25 trunk, and is available in 4-and 8-trunk versions. A companion to the MULTI-PLEX.25, the device concentrates trunk lines from up to 7 MULTI-PLEX.25s onto 1 trunk. It can also connect 1 or more MULTI-PLEX.25s to more than 1 host computer, or to more than 1 public data network.

Switch units can be connected to build private data networks, creating distributed networking systems with redundant patches to minimize service outages caused by trunk failures. For large volume networks, switch builds branch or subnetworks, concentrating traffic from low volume areas into large capacity switching centers. Problems can be diagnosed and tables changed from any point in the network through calls to the switch debug port. Port is password protected to prevent unauthorized access.

Device is compatible with equipment used by GTE Telenet and Tymnet networks in the U.S., and also 8 international compatible systems. **Dynatech Packet Technology, Inc**, 6464-G General Green Way, Alexandria, VA 22312.

Circle 299

Low cost local data sets

Micro400 local data sets provide full-duplex short range operation, and are compatible with Bell spec 43401 for unloaded metallic circuits. Desktop or rackmount versions include asynchronous model 401 that transmits data up to 8 mi (12.9 km) at 1.2k bps, or up to 96k bps over 2.5 mi (4.0 km) over 26 gauge, 4-wire private or leased circuits. Desktop unit is $250; rackmount is $180.

Model 402 smart asynchronous data set offers identical facilities, with added dial-up emulation to replace low speed dial-up modems without changing software or communications protocol. It operates over 2-wire or 4-wire circuits, transmitting at 1.2k bps up to 10 mi (16 km), or up to 19.2k bps over 2 mi (3 km). Model is priced at $330 desktop and $270 rackmount. Model 421 has high speed synchronous operation, transmitting up to 9 mi (14 km) at 1.2k bps or up to 19.2k bps up to 3 mi (5 km). Price is $370 desktop and $300 rackmount. **Micom Systems, Inc**, 20151 Nordhoff Ave, Chatsworth, CA 91311.

Circle 300

Fiber optic synchronous multiplexer

Synchronous time division multiplexer OMX-9608, intended for computer to terminal link, secured communications link, and links between process control equipment, is plug compatible with std RS-232-C equipment. Unit provides full-duplex data transmission on 8 channels, to speeds up to 19.2k baud. Transmission on all channels can be either synchronous or asynchronous, programmable from the front panel keyboard. Each channel can be independently programmed at internally clocked increment synchronous speeds, or externally clocked synchronous or asynchronous modes, transparent to baud rate. Constant monitoring of optical link operational status is provided through both audio and visual LED indicators. Automatic transmission shutdown will occur if the optical link fails. Remote loopback testing of data, on a channel by channel basis, is provided under computer control. Local loopback testing is provided by front panel keyboard control on a channel by channel basis. **Phalo/O.S.D.**, 9240 Deering Ave, Chatsworth, CA 91311.

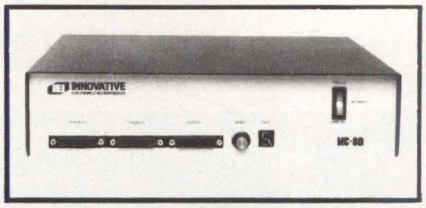
Circle 301

Line drivers

LD 210 AS (asynchronous) and LD 210 SA (synchronous) line drivers serve as low cost modems for short distance, full-duplex transmission over 4-wire metallic circuits. Units include 4 front panel status indicators, switch-selectable RTS/CTS delay, and analog and digital loopback capabilities. Asynchronous driver operates at any speed up to 19.2k bps. Unit has an RS-232-C interface to terminals and front ends, and conforms to Bell 43401 requirements on the line side. Device can be used in most applications not requiring the ring indicator (RI) control signal. Synchronous model is designed for the Supermux 480, 680, and 780 statistical multiplexers, and with the Supermux 790 network concentrator. Drivers are priced at $210 for the asynchronous model and $350 for the synchronous unit. **Infotron Systems Corp**, Cherry Hill Industrial Center, Cherry Hill, NJ 08003.

Circle 302

Communications processor for personal computers



Extended communications interface capability for MC-80s allows communication with Apple, TRS-80, IBM, and other personal computers. MC-80 communications processor supports communications protocols, and provides on- and offline diagnostics. On/offline diagnostics increases attachment maintainability. Diagnostics, provided through a 7-segment display, include indications for polled or selected devices, or transmission errors and modem status. Offline diagnostics are executed at system power-on, and can be operator initiated. CPU, ROM, RAM, and data paths are continuously tested. Third testing level is provided through test connect of outputs to inputs at each interface signal. Standalone, self-powered, microcommunications processor provides up to 16k ROM, 16k RAM, 3 serial communications ports, and 1 parallel printer port. An additional port allows 2 independent devices to be supported. **Innovative Electronics, Inc**, 4714 NW 165 St, Miami, FL 33014.

Circle 303

Computer/multiloop controller link

Serial communications link between the CINCH™ control computer and the MLC 100™ multiloop controller allows configuration of distributed control systems and ensures full compatibility throughout the system. Link also allows users to prepare and store libraries of alternative loop setups that are available for selection according to process conditions. Under CINCH/MLC 100 operation, loop parameters are entered by the

(continued on page 243)

SIEMENS

Ink Jet Printer Model 2712

Settling for less will cost you more.

Settle for less than our Ink Jet Printer Model 2712 and you'll get just that. Less than ink jet quality performance. Less than Siemens unmatched reliability. In fact, getting anything less than a 2712 printer will cost you more. And paying more for less just doesn't make sense.

The 2712 printer is designed and engineered for those discriminating individuals who require exceptional print quality from a highly reliable, super-silent, easy-to-maintain unit. Siemens "Drop on Demand" ink jet system forms a 12 x 9 dot mosaic, using 12 ink jets to ensure high quality character formation time and time again. The printing head life is rated in excess of 10 billion characters. Ten billion characters...that's reliability!

The 2712's modular construction ensures simplified service. Replacement modules, if ever needed, require no field adjustment and can be installed without removing a single screw.

Our highly reliable Ink Jet Printer Model 2712. Paying more won't get you anything better.

For further information, contact Siemens Corporation, OEM Data Products Division, 240 E. Palais Road, Anaheim, California 92805, (714) 991-9700 or call Atlanta, GA (404) 441-0882; Boston, MA (617) 444-6554; Dallas, TX (817) 461-1673; Iselin, NJ (201) 494-5311; Sunnyvale, CA (408) 735-7770.

Siemens. Committed to Quality.

CC/3020-003 SIQ 895

CIRCLE 142

California Computer Show

Date: April 22, 1982
Place: Hyatt Hotel
Palo Alto, CA.
Time: 12:00 - 7:00

TAKE A LOOK AT TOMORROW — meet the industry giants as well as the innovators who'll be tomorrow's leaders.

A single source computer show for OEM's, sophisticated end users, dealers and distributors, the California Computer Show features the industry's newest developments in a one-day regional format.

Featured will be the latest in computers, from minis to micros, graphics, peripherals, systems and software. You're in good company at the industry's only comprehensive one-day show with exhibitors representing IBM, CDC, Memorex, Qume, Versatec, DEC, Data General, HP, Shugart, Lexidata, Dataproducts and more.

Keep in touch with a volatile industry. See tomorrow's products ... today.

For more information or invitations contact Norm De Nardi Enterprises, 289 S. San Antonio Rd., Suite 204, Los Altos, CA 94022, (415) 941-8440.

COMING UP — a new, extended 2-day show, COMPUSOURCE '82, scheduled for December 8-9, 1982 at San Jose's new Red Lion Inn. MARK YOUR CALENDAR NOW!

NDN

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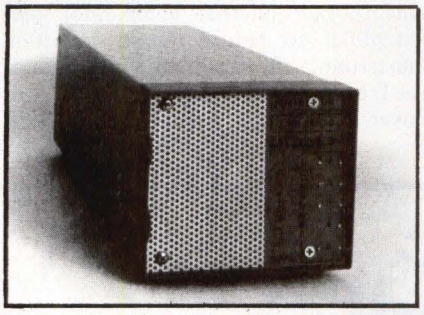
289 S. San Antonio Rd.,
Suite 204,
Los Altos, CA 94022
(415) 941-8440.

CIRCLE 143

operator at the controller's interactive graphics display terminal. Data are transferred to the control computer for storage on tape cartridge, and can be downloaded to the controller on user command. Warning/alarm status on any loop can be reported to the microcomputer automatically by the controller. Computer monitors system operation, including controller data, warning/alarm conditions, set points, and current output. CINCH also has direct control of initial MLC 100 outputs on all loops, and can take over control of a loop at any time. **Control Logic**, 10 Tech Circle, Natick, MA 01760.
Circle 304

Fiber optic data modem



LITEcat™ series of high performance, low error rate, fiber optic data modems provides 5 identical, completely transparent, full-duplex data channels, capable of operation from dc to 80k bps asynchronously and dc to 200k bps synchronously. Device is available with either unbalanced or balanced interface circuits. Framing and synchronization system results in error rates of approximately 10^{-10} when operating in noisy environments. Device contains 12 front panel indicators for channel, link, and power status. A crystal derived clock provides rates from 600 to 76.8k bps in 75 x 2^n increments. **INTEQ, Inc**, 3171A Spring St, Fairfax, VA 22031.
Circle 305

Custom designable modems

Line of Bell 103/113 compatible modems features custom applications for designs using 300-baud, full-duplex operating modems. The std device is a Bell 103J compatible, originate and answer, direct connect modem card measuring approximately 5.5″ x 8.5″ x 1.25″ (14.0 x 21.6 x 3.18 cm), but in custom configurations, board size can be reduced

(continued on page 244)

significantly. Card housings fit under std telephone handsets. Unit includes phone line protection circuitry, power transformer, switches for talk/data, orig/ans, and self-test. Also onboard are LEDs for power-on and carrier detect. Interconnection is made via 2 RJ-11 modular phone jacks and an RS-232 DB-25 connector. An extruded plastic housing and 6′ (1.8-m) power cord are optional. Combined hardware and software, and modular design approach utilizing universal base circuitry allow flexibility and volume pricing on shared components. **CTS Corp**, 1201 Cumberland Ave, West Lafayette, IN 47906.
Circle 306

Terminal enhancement

TCM Terminal Enhancer for RS-232-C teleprinter terminals enables use of 1 machine for data handling or preparation, and also for communication on DDD, TWX, or TELEX networks. Multiprotocol modem appears as a Bell 103J modem at the DDD port; as a Bell 101C modem (including restraint features) at the TWX port; and as a WU TIM-81-1, F1/F2 modem at the TELEX port. Automatic or manual dialing from the terminal keyboard is accomplished on all 3 ports. Modem automatically answers and time/date logs incoming calls on any network port during off hours, as well as storing the message in 16k expandable message buffer. Terminal can be used simultaneously for offline message preparation without loss or delay of incoming calls. Self-prompting text editor feature is included. **Datatronix Inc**, 2100 Reston Ave, Reston, VA 22070.
Circle 307

DATA CONVERSION

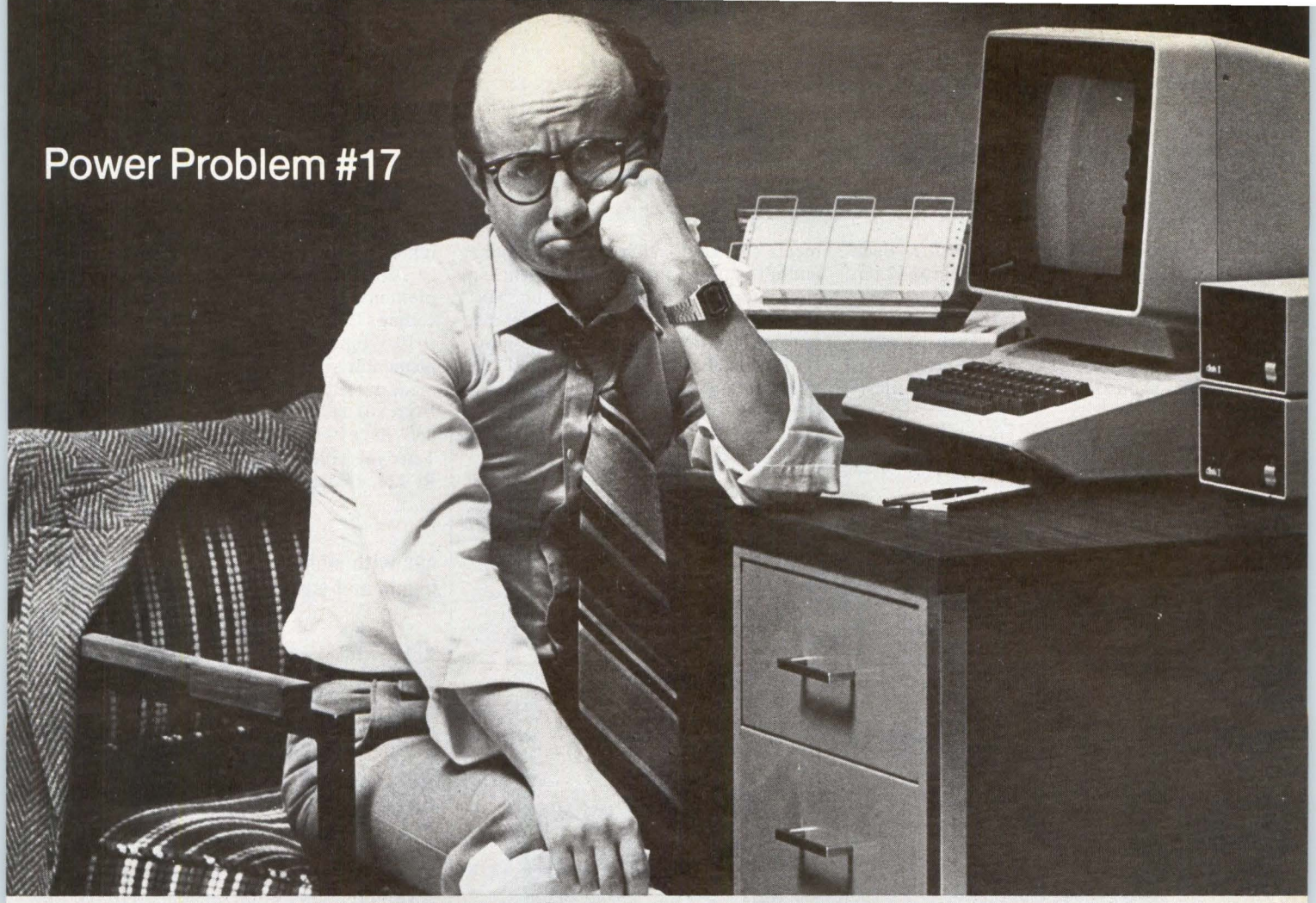
Optical incremental encoder

Optical incremental encoder 2300 series combines 2.25″ (5.72-cm) diameter with resolutions to 2540 cycles/rev. Encoder features a visible accurate code disk read by hermetically sealed phototransistors and solid state light sources, all metal sealed housing O-ring, high noise immunity, high reliability, and long life. Device can be mounted in any position with either servo ring or bolt hole circle. A 2-track option provides separate count outputs for English/metric applications. Electronic decoding of outputs can extend angular resolutions to greater than 10k counts/cycle. **Northern Precision Laboratories, Inc**, PO Box 1016, 11 Madison Rd, Fairfield, NJ 07006.
Circle 308

Hybrid ADCs

Family of improved ADC85 type 12-bit ADCs features max integral and differential linearity errors of ±½ LSB, and guarantees no missing codes over specified temp ranges. Also featuring guaranteed max 7-μs conversion time, the successive approximation type ADCs incorporate internal comparator preamplifier to reduce output transition uncertainty thresholds to a typ value of ±1/8 LSB. TPADC85 is fully specified over −25 to −85 °C (ambient); TPADC87

(continued on page 246)



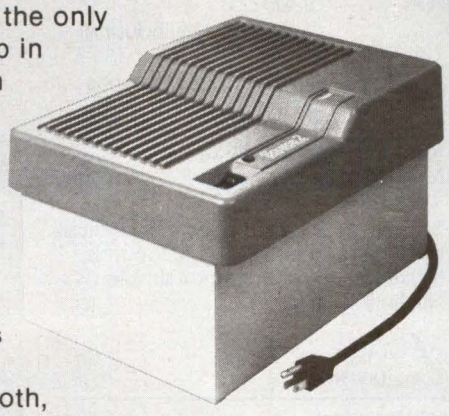
HOW DO YOU STOP BLACKOUTS FROM LEAVING BAD MEMORIES?

Answer: With a Topaz Source 2® Standby Power System.

Power failures can cause real problems for computers. Your word processor shuts down mid-sentence without a word of warning. Your intelligent terminal loses data and draws a blank. Worst of all, you spend hours trying to replace the data that was lost.

And blackouts aren't the only problem. A momentary dip in voltage or a brownout can put small business computers out of business.

But there is a bright side. Now you can put a Topaz Source 2 between your computer and your power problems. The moment AC voltage drops below normal, Source 2 takes over to deliver smooth, sine-wave power to keep your computer up and running. Even during a total blackout you'll have plenty of backup power to save memory contents — and plenty of time to shut down the system in a businesslike manner.



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TOPAZ

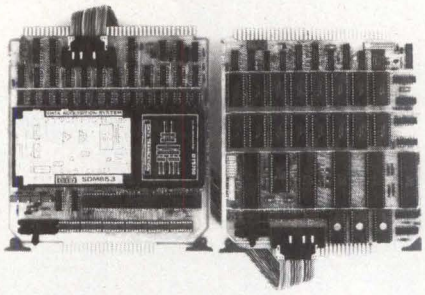
SOLUTIONS TO POWER PROBLEMS™

CIRCLE 146

over −55 to 125 °C (ambient). Each model is hermetically sealed in std 32-pin DIP and can be screened to MIL-STD-883, method 5008. Models include user selectable direct/buffered inputs; parallel/serial outputs; pins for short-cycling, clock adjustment, zero and gain adjustments (for optional initial calibration); and all required logic/measurement circuitry for implementing a 12-bit ADC. Internal clock and precision reference outputs are available at device pins. Both models can be configured for unipolar and bipolar operation over 5 input voltage ranges. Connection for 0- to 10-V unipolar inputs produces complementary straight binary output coding. Connection for ±2.5-, ±5-, or ±10-V bipolar inputs allows either complementary offset binary or 2's complement output coding. All models operate from std ±15- and 5-V power supplies and have typ 1200-mW consumption. **Teledyne Philbrick**, Allied Drive at Rt 128, Dedham, MA 02026.

Circle 309

ADC with multiplexed inputs and memory



53A-519 data acquisition subsystems (DAS) plugs into any function card slot of the CDS 53A-002 card cage. Subsystem is externally programmable via the IEEE 488 bus or RS-232-C, or locally from the CDS 53A-MPX basic language system controller. DAS contains a high speed ADC that can digitize 12-bit, single-channel voltage levels at a rate of 25k readings/s. Moreover, it can store results in a 16k-word 12-bit memory, or scan, digitize, and store in memory measurement data from up to 16 randomly multiplexed voltage input channels at a rate of 21k 12-bit readings/s. DAS measures dc voltage, scans and digitizes up to 160 temp input channels using solid state temp to current transducers covering the temp range of −50 to 150 °C. Subsystem has 3 programmable input voltage ranges, and can control A-D sampling rate by programming delay between each A-D conversion in 1-ms steps. Device can program a voltage trigger level on any channel, and then digitize input voltage levels on 1 or more channels. Memory can be configured as a circular buffer to allow storage of measurement data before and after a trigger event. When measurement sequence is complete, the DAS can be programmed to preprocess measurement data stored in memory before returning the data. **Computer Data Systems**, 3301 W Hampden Ave, Unit C, Englewood, CO 80110.

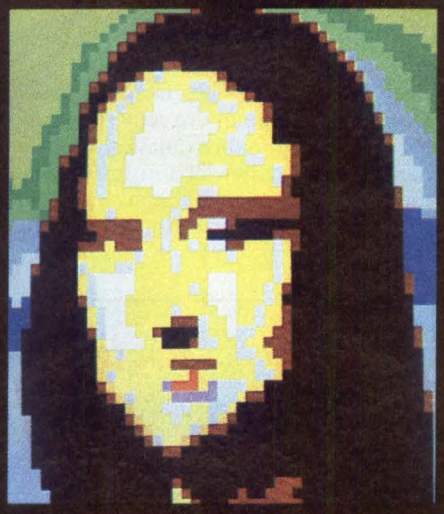
Circle 310

We can give you Mona's smile, but business color is our business.

The exciting age of color business graphics has arrived, and Panasonic is there with a complete line of color CRT/chassis assemblies that can display business graphics like nobody's business.

Our full line of color CRT displays features a choice of the most popular sizes – 12″, 13″, 15″ and 19″ (measured diagonally) – plus modular construction, advanced yoke design, high-integrity mounting and much more. Optional switching power supplies – for display, logic or both – come mounted directly on the zinc-coated ferrous metal chassis.

Panasonic color data displays are designed to provide optimum performance in business graphics applications. They're "value engineered" for exceptional quality, simple installation and easy serviceability. At very affordable prices.



If you're looking for a color display for your next business computer terminal, choose Panasonic. Why? For quality and delivery you can depend on. Plus comprehensive parts availability and 7 service-center locations. And because business color is our business.

We also offer a complete line of monochrome displays, to meet even more of your terminal requirements. For full data and OEM prices, write or call: Panasonic Company, Data Display Dept., Industrial Sales Division, One Panasonic Way, Secaucus, NJ 07094; phone (201) 348-5385.

Panasonic high and mid resolution data displays.

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CIRCLE 148

8-bit ADC

ADC-830 8-bit CMOS A-D converter operates directly with std control bus of 8080 microprocessor derivitives via 3-state outputs. Converter appears as a memory location or I/O port to the microprocessor without interface logic. Digital control inputs are active low. Using successive approximation and a modified potentiometer resistor ladder, the ADC achieves 8-bit conversion in 100 μs with a max total adjusted error of ± 0.5 LSB. No zero adjust is needed. Differential analog input allows the user to increase common mode rejection and offset zero value of input. Converter operates ratiometrically, with 2.5- or 5-V power supply, or, to allow encoding of smaller voltage ranges, an analog span adjusted reference. Internal clock generator requires only an external RC network, or it can be driven by an external clock at a frequency range of 100 kHz to 1.2 MHz. Unit is packaged in a 20-pin plastic DIP and operates over temp range of 0 to 70 °C. Power requirement is 5 Vdc. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.

Circle 311

100-MHz sampling rate quantizer

Designed for high speed A-D conversion, Am6688 quantizer can output a 4-bit word at sampling rates up to 100 MHz. Resolution above 4 bits, up to a max 8 bits, can be obtained by stacking the devices. Overrange output signal indicates when input has exceeded the full-scale limit, and is also the enable gating signal used to encode higher order output bits in a stacked configuration. Features of the 18-pin device include 5-ns max encode delay, 8-bit accuracy, bipolar input voltage range, Q and $\overline{Q}$ outputs on MSB for 2's complement conversion, and compliance to MIL-STD-883. Two high speed latch enable inputs are intended to be driven from complementary outputs of a std ECL gate, or from a high speed comparator. Outputs are open emitters, requiring external pulldown resistors of at least 200 Ω to -2.0 V, or 500 Ω to -5.2 V. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086. Circle 312

Protocol converter

Universal protocol converter UPC-80 operates with a universal set of I/O data protocols. Protocols can have any mixture of serial or parallel formats. The protocol converter also performs string/code conversions such as ASCII to EBCDIC. It has 6 bidirectional ports; 3 ports are serial and 3 ports are parallel. Of the 3 serial ports, 2 support synchronous byte protocols such as 2780 or 3270 BISYNC, and will also support asynchronous communications. The third serial port is asynchronous and supports either SDLC or HDLC communications. All 3 serial ports are RS-232-C compatible with baud rates up to 19.2k bytes. Parallel ports are TTL compatible.

(continued on page 251)

CIRCLE 149

Digital's new PDP-11/23 PLUS microcomputer gives you all the flexibility you need to design your own system.

Thanks to our new high-density memory chips, you get 1/2 megabyte of memory, plus a CPU, on a total of just two boards. Which leaves room for seven boards of your choice.

For example, you can add another 1/2 megabyte board for less than $3500*. Or you can add any of the 40 other boards in our micro family, plus hundreds of compatible boards made by other companies.

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*U.S. Domestic prices

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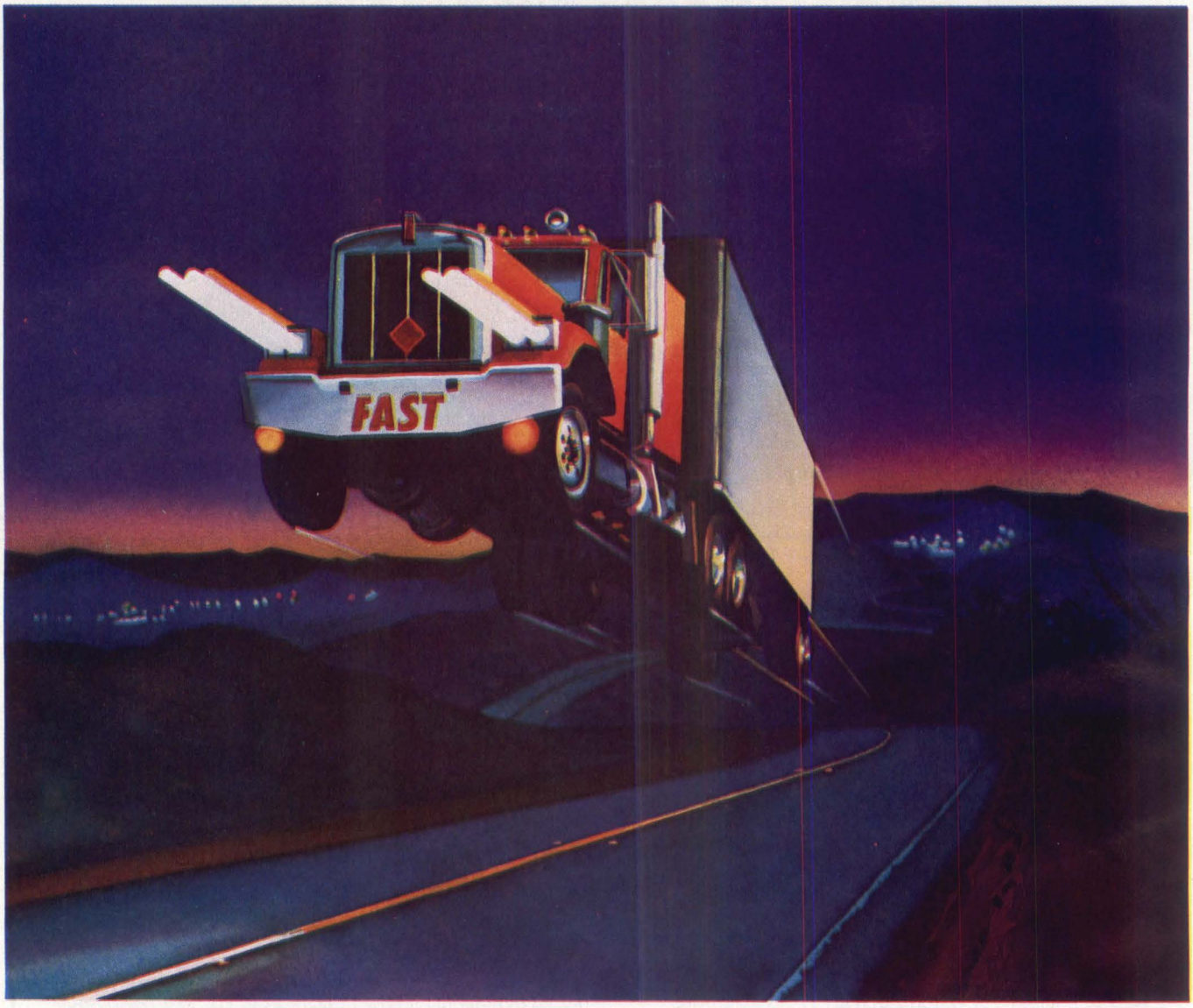

FAST Delivery.

Until now, there were only 134 reasons to think FAST.™ 134 low-power, high-speed, defined functions. Including latches, buffers, flip-flops, counters, registers, multiplexers and LSI.

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The fact is, we've been going at a fast and furious pace for the last three years. Millions of units are being produced every month. And we're getting them off our shelves, and into the hands of our customers, at a fast clip.

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Whatever you do, just make sure you're on the FAST track. Fairchild Digital Division, 333 Western Avenue, South Portland, Maine 04106. Tel: (207) 775-8100. TWX: 710-221-1980.

Digital

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CIRCLE 150

Converter consists of a single board containing a 4-MHz Z80 microprocessor, 16k dynamic RAM for operational storage, 8k-bytes EPROM for firmware modules, and 1k-byte nonvolatile RAM for alterable parameters. **Equinox Data Systems, Inc**, 517 Newman Springs Rd, Lincroft, NJ 07738.
Circle 313

INTERFACE

Interface converters

IFC 200 interface converter series permits interconnection of terminals and modems with electrical and mechanical differences in cable/plug assemblies. Series covers the full range of cable/plug specs encountered on DTE and DCE. Units include EIA, Bell, and CCITT specs. All models are fully transparent to data and other signals. Modem for DCE connects via a 5′ (1.5-m) cable terminated with appropriate plug to fit the interface. Terminal for DTE connects at the rear panel receptacle where cable/plug assembly from the terminal equipment plugs in. Installation requires no adjustments; converters operate when connected to modem, terminal, and power source. Standard 115-Vac ± 10%, 60-Hz power is required. Front panel outlet can be used to power the modem. Custom units are available for other supply voltages and/or frequencies. Each converter measures 8.5″ x 4.5″ x 3.25″ (21.6 x 11.4 x 8.26 cm). **Gandalf Data Inc**, 1019 S Noel, Wheeling, Il 60090.
Circle 314

Color graphics board

RG-GG6C graphics generator is a 2-board set of MULTIBUS compatible boards for use in raster graphics board color applications. Consisting of a smart vector generator board that interfaces to the MULTIBUS, the graphics generator accepts high level commands to produce variable size ASCII chars, to draw circles and vectors from specified endpoints, and to generate reverse video displays. Dual-refresh memories of 512 x 480 elements resolution are designed to move displays, allowing 1 memory set to be updated while data are displayed from the other set. Three RS-170 compatible composite TV signals are output at BNC connectors on the refresh memory board for connection to the RGB color monitor. **Raster Graphics,** PO Box 23334, Tigard, OR 97223.
Circle 315

Disk controller for VAX-11/750

SC750 disk controller is designed for VAX-11/750 systems and is functionally identical to the DEC RH750 Massbus adapter combined with RM03, RM05, and/or RM80 disks. Users can tie various drives having SMD interfaces to the VAX-11/750. Controller is transparent to the DEC virtual memory system and other VAX operating systems, and to DEC diagnostics. Controller PCB mounts in system adapter slots with no wiring modifications needed. Features include automatic self-test during power-up, intelligent buffer management, mixed drive handling, and operation at disk rates up to 15 MHz. **Emulex Corp**, 2001 E Deere Ave, Santa Ana, CA 92705.
Circle 316

Interface package for AIM65

SET1 interface package allows the AIM65 computer to read 16 parameters in system expandable up to 128 analog inputs. Device plugs into the AIM65 application port to provide an additional application port, as well as screw terminals for the 16 inputs. No soldering or special cabling is required for interface connection. Each 0- to 5.12-V input is converted to an 8-bit number. Input impedance is typ 2M Ω; conversion time for each input is less than 70 ms. **Connecticut microComputer, Inc,** 34 Del Mar Dr, Brookfield, CT 06804.

Circle 317

Plug compatible interface for line printers

Plug compatible interface that operates on the Datapoint parallel channel with models 6080 and 6081 line printers offers a 25 to 40% price/performance benefit. Price for the 6081 with plug compatible interface is $8095; 6080 is priced at $9500. Interface allows direct connection to the parallel channel of processors and has addressing capability. It is supplied with a 2-connector cable for daisy chaining. Model 6080 is totally enclosed to provide office environment operation with a noise level of less than 60 dBa. Band printers operate at 600 lines/min and offer 48-, 64-, and 96-char bands in a range of char sets. **Centronics Data Computer Corp,** Hudson, NH 03051.

Circle 318

CP/M capability for Apple II and III

Plug-in Z-card allows Apple II and III users to implement CP/M in conjunction with SOS. Unit contains its own Z80A microprocessor, allowing the Apple machines to run virtually any software designed for CP/M based microcomputers. No hardware or software modifications are needed. Once installed, users can switch among CP/M and DOS, or SOS, using software commands. Synergizer Software, the CP/M operating system delivered with the device, includes an enhanced directory command, format and copy in one pass, and use of 60k RAM. Unit is fully compatible with the Smarterm 80-col display board and Add-Ram 16k RAM board. **ALS, Inc,** 1195 E Arques Ave, Sunnyvale, CA 94086.

Circle 319

DEVELOPMENT SYSTEMS

Satellite emulation system

ES series satellite emulator provides real-time, transparent emulation of 8- and 16-bit microprocessors. The universal emulator incorporates a std mainframe with plug-in control cards and pods that tailor the unit to specific microprocessor families. Emulator currently supports the Z8001; unit is planned for plug-in support of most 8- and 16-bit devices by year end.

Communication is via 2 RS-232 ports. Emulator can hook up to user's present development system, minicomputer, or automatic test system to allow upgrading of existing equipment with hardware/software integration and debug capabilities, and to support new microprocessor designs. System can operate as a stand-alone unit when coupled with any ASCII CRT terminal. While debugging is performed on the satellite emulator, the host system is free for use in other design tasks. User control is menu driven, and prompts are CRT screen relayed. A disassembly firmware package provides mnemonic display of target system programs.

Emulator contains 16k-byte mappable overlay RAM in 1k-byte segments. System can be expanded to 64k bytes when larger programs are tested. Breakpoint events can be combined to provide trace start/stop/hold, to cause a trap, and for oscilloscope loop signal output functions. Breakpoint features include 4 condition states defined by address, data, status bits, pass count, and jump controls. Combining algorithms include AND, OR/XOR, NOT, IF THEN, inclusive and exclusive functions. **Applied Microsystems Corp,** 11003 18th Pl NE, Kirkland, WA 98003.

Circle 320

Desktop/rackmount STD BUS package

Designed to meet UL, VDC, CSA, and FCC requirements, 701 μPackage contains a choice of 12- or 21-slot STD BUS card cages, triple power supply, and pushbutton power and reset. The 5-V, ± 12-Vdc power supply delivers a full 15 A; forced air cooling capacity up to 450 W is sufficient for a system drawing full supply current. Package can be customized by user installed hardware such as I/O module mounting rack or mini-floppy disk drive. Front panel and approximately half the rear panel can be removed and are flat surfaced for easy modifications. Full-scale mechanical drawings are available for documentation support. Package can be mounted in a std 19″ (48-cm) RETMA rack. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 321

Development system

Microcomputer and development system DIS-1 combines a 6502 based AIM 65 microcomputer with full keyboard, printer and display, and 64k dynamic RAM. Floppy disk controller modules, PROM programmer, power supply, 2 double-density floppy disk drives, 12″ CRT monitor, and BASIC or Forth software are included. System can be customized for specific applications with off-the-shelf modules. Expansion modules include IEEE 488 controller, ACIA, solid state relays, clock and calendar, and CMOS memory with battery backup. System can be configured to accept up to 10 added modules—6 Eurocard size and 4 EXORciser size. Additional software includes assembler and PS/65. System enclosure allows use of the AIM 65/40 microcomputer in place of the AIM 65. **Dynatem Inc,** 20881 Paseo Olma, El Toro, CA 92630.

Circle 322

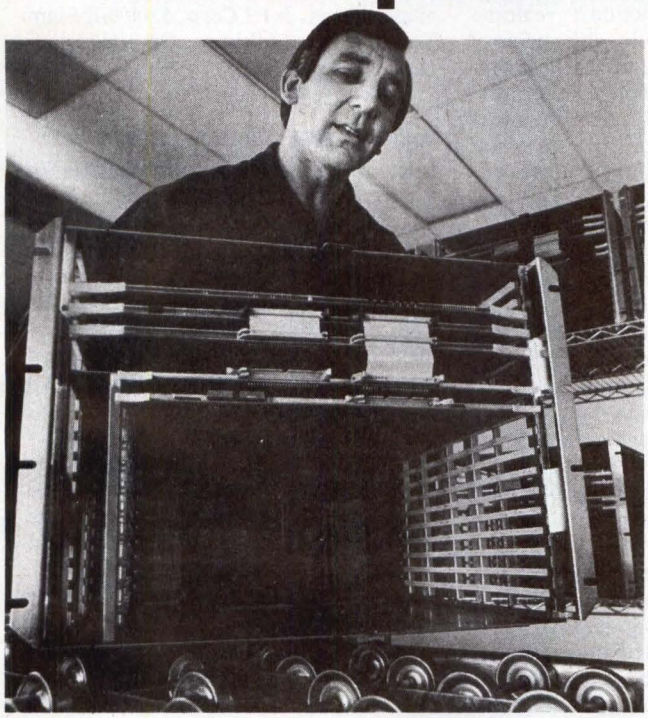
Development support for 8000 series microprocessors

In-circuit emulation development system support, the Co-emulator™ Power Probe permits simultaneous co-processing for 8086/8087 and 8088/8087 processor pairs. Co-emulator allows the development system to provide complete software debugging and software/hardware integration to the processor

(continued on page 254)

There are two leaders in 32-bit minicomputers.

Perkin-Elmer is the one that offers a 'no-frills' 32-bit processor at $19,100.



Our new 3210/A OEM processor—at $19,100 it's the no-frills alternative to 16-bits.

The new Perkin-Elmer Model 3210/A lets the OEM choose only the components he needs to custom tailor the 32-bit system he wants. At $19,100 (OEM quantity 100), the high-performance Model 3210/A is actually priced lower than many smaller, less powerful 16-bit machines.

The Model 3210/A gives you 32-bit power and component options at a price that can do great things for your product line—and your bottom line.

The basic unit includes a fully functional 32-bit processor with 512KB of state-of-the-art high-density memory mounted in a chassis with control panel and two communications lines.

All other components are available separately at off-the-shelf prices. These include 30- or 50-inch high cabinets, DC power system, air-cooling assembly, floating-point processor, and attractively priced add-on memory to a maximum of 4MB.

The Model 3210/A gives you a path for future growth plus a broad range of available systems and applications software.

Looking for a 32-bit minicomputer supplier? Look to Perkin-Elmer—the company with more installed 32-bit minis than any other company except one. We're the one that gives you more. More performance. More support. More value. Call or write for details. Perkin-Elmer, Oceanport, NJ 07757. Tel: 800-631-2154. In NJ 201-870-4712.

We're the one.

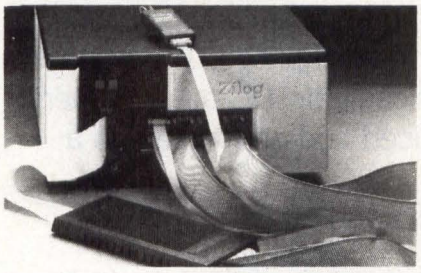
PERKIN-ELMER

CIRCLE 151

pairs. System is user configurable to emulate the 8086 and 8088 separately. Co-emulator is compatible with FutureData's 2300 series development systems in both single- and multi-user networks. The emulator complements and can be used in simultaneous multi-emulation with the Z8001/Z8002, Z80, 68000, 6809, 6809E, and 6502.

System consists of an emulator interface circuit board, probe, cables, and support software for use with the 2302 slave emulator and 2300 series development system console. Full, transparent emulation to 8 MHz for the 8086, 5 MHz for the 8088, and 2 MHz for processor combinations is provided. Emulator supports all features of the 8088 and 8086. Support for the 8087 provides emulation and debugging capability; program and data memory can exist on the prototype or mapped into emulator ROM simulator memory. Debug software provides error trapping/handling and 8087 status/register contents determination commands. Software development can be in assembly or Pascal languages. **GenRad, Development Systems Div**, 5730 Buckingham Pkwy, Culver City, CA 90230.
Circle 323

Networkable realtime emulator for microprocessor family



An intelligent emulator subsystem EMS 8000 supports the entire Z8000 CPU family and can be networked to facilitate product development for distributed processing and multiple microprocessor applications. Subsystem offers realtime emulation, complex triggering, a large partitionable trace memory, and up to 126k bytes of mappable memory. Up to 8 microprocessors at speeds of 6 MHz max can be emulated simultaneously. Device monitors message passing from source to destination; triggering capability enables 1 unit to trace message sending in a particular network node, while a different emulator monitors message receiving in other nodes. Network node, while a different emulator monitors message receiving in other nodes. Network debugging is supported by group break feature that permits multiple units to begin and end emulation simultaneously.

Hardware consists of a central controller with 256k dynamic memory and 16k ROM; 2-board trigger module with 3 parallel trigger comparators that serve as building blocks to configure trigger, trace and timing functions; realtime trace partionable module with memory to reduce debugging time; external probe interface module; mappable memory module; and microprocessor personality module. Emulator gives the user full access to target microprocessor's registers, memory, and I/O space. Special I/O and MMU functions are supported through substitution of MMU physical addresses for logical addresses in debugging. Static memory can be mapped with resolution of 2k bytes anywhere in the user's memory space. Each 2k-byte block can be declared unprotected, write-protected, data memory only, or nonexistent. Logic state analysis is provided for target CPU address, data, status, control, and external probe bits; these fields are bit-maskable in a 64- x 1024-bit deep trace.

Software provides screening functions such as default, configuration, programming, system debugging and self-test. Software is down loaded during initial power-up, and can be upgraded or custom programmed. **Zilog**, 10340 Bubb Rd, Cupertino, CA 95014.
Circle 324

PROM programmers

Online programming of EPROMs, bipolar PROMs, and PROM based central processors is provided by iUP-200 and iUP-201. Model iUP-201 includes unit to provide offline programming, with PROM duplication, editing, and program verification independent of the host system. Data are downloaded from a development system into RAM for offline programming. Programmer can serve as a standalone unit, accepting data into RAM from a ROM or PROM device. Self-diagnostics are included on both models. Programmers interface directly with Intel development systems having 64k bytes of user memory. Each unit contains 8085A CPU, selectable power supply, 2.3k bytes of static RAM, 8k bytes of programmed EPROM, programmable timer, and circuitry for personality module interface.

Software utility iPPS commands are entered through the development system ASCII keyboard and are CRT displayed. Commands allow data reading and writing from logical devices, the target PROM, system memory, or disk file system. Additional commands enable user control of program execution to display information and status, rearrange data from any of 3 logical devices, and obtain assistance from a help command library. **Intel Corp**, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.
Circle 325

In-circuit emulation package

In-circuit emulation support package for the NSC800 CMOS chip is designed for the ECL-3211 line of universal development systems. Package provides all hardware and software for the ECL-3211 to perform full-speed, realtime, in-circuit emulation, simulation, and software development for the NSC800. Included are target interface pod, chip driver software and disassembler, macro cross assembler, linker, and universal PROM programmer utility. All features and operating modes of the NSC800 are implemented at all clock rates of the chip. NSC800 emulation controller is functionally transparent to the target and does not steal interrupts, address space, or stack space. Package provides a 511-record, 48-channel realtime trace analyzer selectively controlled by 8 hardware breakpoint actions. Trace analyzer displays data, disassembled mnemonics, status of 8 external lines, and all chip status and control lines. Four logical switches used both as breakpoint actions and trap conditions permit concatenation of multiple breakpoints. Package provides byte resolution memory mapping and permits full-speed, no wait state operation under any conditions or mix of external/internal memory mapping. **Emulogic Inc**, 3 Technology Way, Norwood, MA 02062.
Circle 326

Universal realtime emulation

ICEBOX™ emulation station allows debugging of 8- or 16-bit microprocessors with realtime emulation. Universal station is supported by field installable memory and functional options, including a 1M-byte floppy disk system and ROM based relocatable macro assemblers. Station serves as an extension of a std development system; as a hardware development arm for minicomputers via an RS-232-C link; or as an attached processor handling high speed

(continued on page 256)

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Minneapolis, Minnesota 55441
612/553-1533

Multiwire/West
3901 East La Palma Avenue
Anaheim, California 92807
714/632-7770

CIRCLE 152

assembly and debugging functions. Model is available with in-circuit emulation consisting of 64k- to 256-byte emulation RAM, a communications library card, a DEC/Intel compatible communications interface, Z80 assembler, and Z80 SPICE in-circuit emulator. Station incorporates 4 serial I/O channels, asynchronous/synchronous serial communications, RS-232-C, RS-422-A, RS-449 serial I/O connections, MULTIBUS and P-796 bus compatibility, IEEE 488 GPIB with talker, listener, and controller, and Centronics interface printer. **Relational Memory Systems**, 1180 Miraloma Way, Sunnyvale, CA 94086.

Circle 327

INTEGRATED CIRCUITS

High speed microcontroller family

Based on the 8X305 microcontroller, a family of high speed devices provides a complete microsystems approach to high speed controller solutions, including support circuits and development systems. Microcontrollers come with complete documentation and applications support. Microcontroller based system development is supported by an incircuit emulator module.

Implemented in bipolar low power Schottky technology, the standalone byte oriented microcontroller family features a 200-ns cycle time, and contains an expanded instruction set and 7 additional registers to improve throughput. Device is offered in ceramic and plastic packaging, in both commercial and military versions with op temp ranges of 0 to 70 °C and −55 to 125 °C, respectively.

Seven peripheral chips will be introduced to add capabilities for interrupt handling, large working storage, and parity support. **Signetics**, 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086.

Circle 328

Single-chip floppy disk controller

Family of single-chip floppy disk controller/formatters WD279X integrates all essential control functions, plus data separation and write precompensation, into a single LSI device. Controllers directly interface both 5.25″ and 8″ floppy drives to a system host processor. Family is an evolution of the industry std FD179X controllers. Device can replace 4 or more devices by integrating a high performance phase lock loop data separator, write precompensation logic, VCO, and phase comparator on a single chip. Device is software compatible with the FD179X. Family consists of 4 components for combinations of single- and double-density, true or inverted data bus, and single- or double-sided drives. Onchip VCO and phase comparator allow frequency adjustment of the drives. Designed for soft sectored systems, devices feature automatic track seek with verification, DMA, or programmed data transfers from a double-buffered 8-bit bidirectional bus, and 8 control lines for microprocessor compatibility. They can perform single- or multiple-section read/write with automatic search, or read/write the entire track. Clock rates are 2 MHz. Fabricated in NMOS, the 40-pin DIP is available in either plastic or ceramic. **Western Digital Corp**, 2445 McCabe Way, Irvine, CA 92714.

Circle 329

4k CMOS static RAMs

HM6147H series provides 6 types of high speed 4k complimentary MOS static RAMs in 18-pin DIPs. The RAMs consume approximately 25% the power of a high speed 4k NMOS static RAM, but have a comparable max address access time of 35 ns. High speed address access time is possible with the RAM polysilicon structure and 2.5-μM processing. Hi-CMOS design also allows the RAM cells to be made by NMOS process and peripheral circuits by CMOS process. Applications include cache, buffer, and program memories, and terminals for medium and small computers. Power requirement is 5 V, ±10%. Power consumption during operation is 150 mW typ. **Hitachi America, Ltd**, 1800 Bering Dr, San Jose, CA 95112.

Circle 330

CCD line image sensors

Charge-coupled device (CCD) based TC101 and TC102 line image sensors incorporate 1728 and 128 elements, respectively. Features include enhanced spectral response and high response with internal dark/white references. Sensors are fabricated with virtual phase MOS technology that utilizes a junction gate region set at dc substrate potential to perform identical gating and charge transport as a separate gate electrode. Virtual phase uses single level gate to achieve charge transfer, eliminates possible gate to gate shorts, and produces devices with high quantum efficiency, uniformity, and low dark current.

The 2 sensors are functionally equivalent. Transfer register is adjacent to the image sensor elements. When voltage is low, charge is transferred into transport CCD shift registers that move alternate charge packets to an output amplifier. Reset and transport clocks provide alternate delivery of charge packets and handle sequencing of charge transfer. Buffer CCD shift registers minimize the effect of peripherally generated dark current. Units have 4 additional sensor elements providing dark signal reference. Both devices also include a white signal generator for reference of output signal. TC101 is supplied in a 24-pin DIP for insertion in mounting hole rows on 600-mil centers. TC102 is provided in a 10-pin package with 300-mil centers. **Texas Instruments Inc**, PO Box 202129, Dallas, TX 75220.

Circle 331

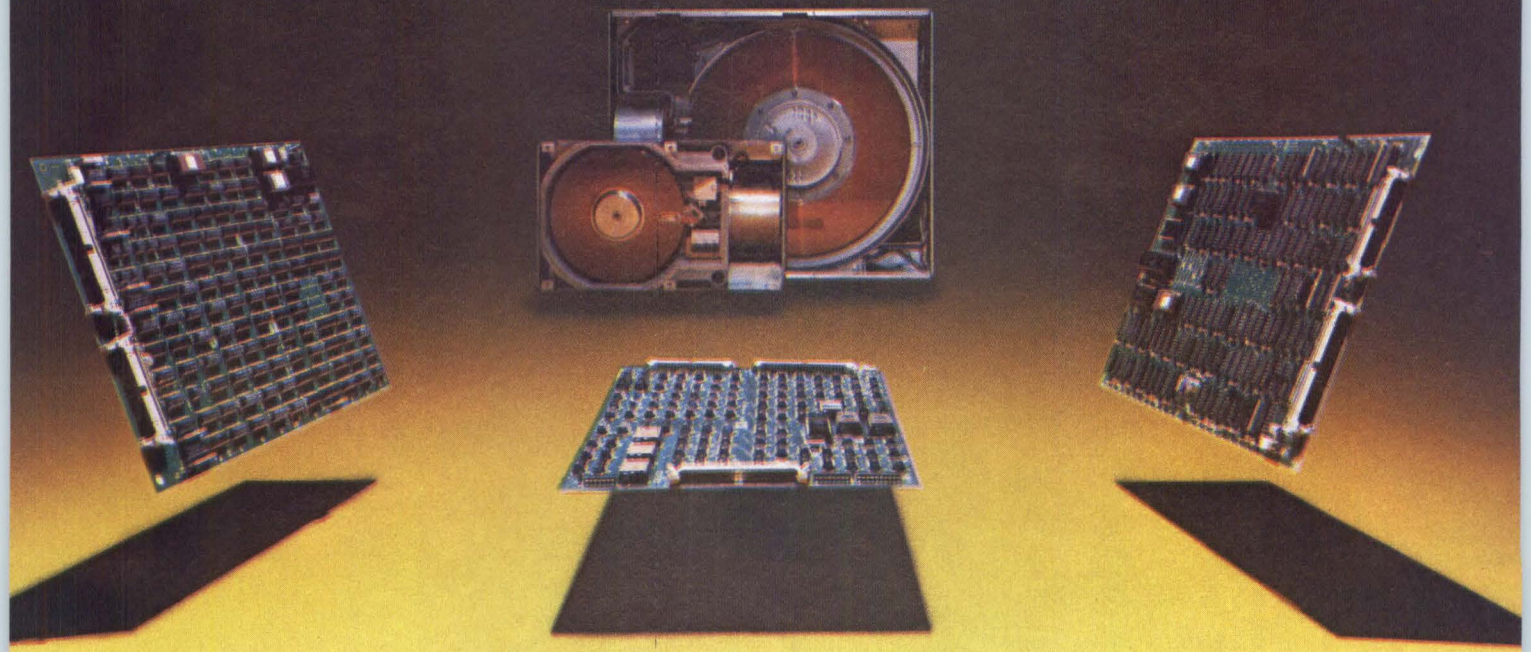
Industry std UART

Model CDP6402 industry std 6402 UART interfaces microprocessors to asynchronous serial data channels, operates at max frequency of 3.2 MHz, and dissipates 7.5 mW when running from a 5-V supply. Two versions are offered—plastic packaged E-suffix for op temp range of −40 to 85 °C, and ceramic housed D-suffix for range of −55 to 125 °C. Both packages have 4- to 10.5-V power supply capability. Baud rates range from dc to 200k bps when operating from a 5-V supply, and dc to 400k bps with a 10-V supply. Device is a pin for pin replacement for the industry std HD6402 and IM6402 UARTs. The CMOS UART provides all formatting and control for interfacing between serial and parallel data channels. It is fully programmable with an externally selected word length of 5 to 8 bits, a parity inhibit, odd or even parity, and 1, 1.5, or 2 stop bits. **RCA/Solid State Div**, Rt 202, Somerville, NJ 08876.

Circle 332

Have you written to the Editor today? Do it now!

SMART BACKUP!



PRIAM's Intelligent Interfaces For Winchester Discs And Tape Drives

Save time and money by using PRIAM's intelligent interfaces. PRIAM has expanded the SMART family to support *backup* to your Winchester disc systems. Take your pick from 1/4-inch streaming cartridge tape or 1/2-inch tape. PRIAM SMART Interfaces can be mounted on PRIAM drives or separately, and they can be powered from PRIAM's disc drive power supplies.

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Lowest in cost of PRIAM's three intelligent interfaces, the SMART Interface is smart indeed. It includes error checking, disc formatting, selectable sector sizes, full-sector buffering, defect mapping, self-test, and power-down data protection.

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Also low in cost, the SMART-E provides all the SMART functions, plus ECC with error correction transparent to the host and high-performance hardware/firmware. Backup is provided by daisy-chaining the EPI STR-Stream* 17-megabyte 1/4-inch cartridge drive or the Pragma DAC 2080* 80-megabyte 1/2-inch cartridge drive.

SMART-T

Compatible with the SMART and SMART-E, the SMART-T provides off-line streaming backup with host access to the database during backup. The SMART-T controls Archive Sidewinder*, DEI Streamer* and Cipher Quarterback* 1/4-inch streaming cartridge tape drives.

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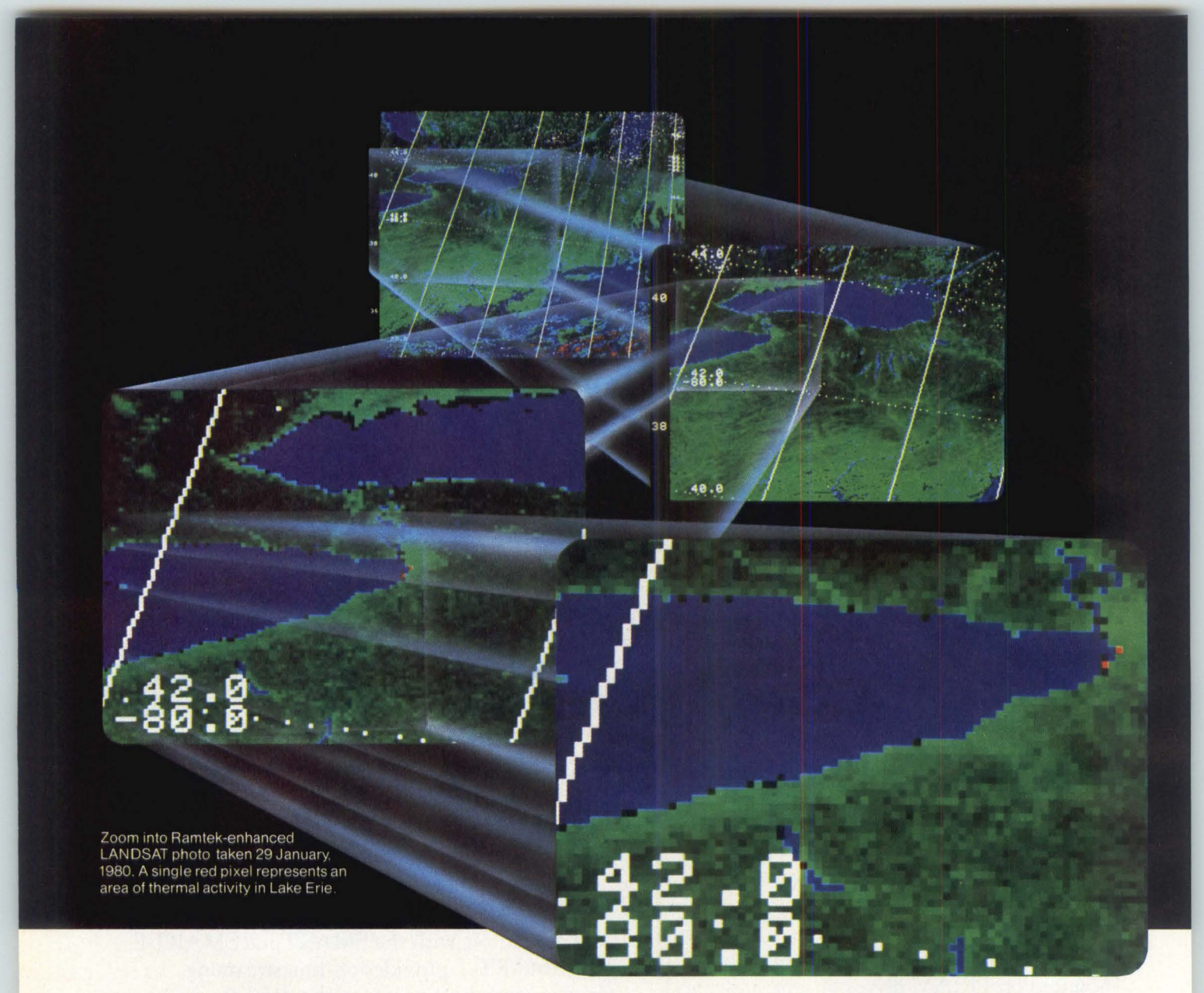

Zoom into Ramtek-enhanced LANDSAT photo taken 29 January, 1980. A single red pixel represents an area of thermal activity in Lake Erie.

Zoom, pan, flood and a lot more, for a lot less.

Our new 9450 display system brings high-performance color graphics and imaging down to a price everyone can afford. Compare the 9450 and its low price to other high resolution display systems.

Do they offer 640 x 512 or 1280 x 1024 resolution? 256 colors (or gray-scale tones) at once from a palette of 16 million at both resolutions? How about a writing speed of 16,000 vectors per second?

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If you can find this kind of performance and quality—plus zoom, pan and flood—in a comparably priced system, buy it. If you can't, our worldwide direct sales and field service offices are waiting to hear from you. Call the office nearest to you, or write us at 2211 Lawson Lane, Santa Clara, CA 95050.

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Digital filter/utility peripheral

S2815 digital filter/utility peripheral performs signal processing, measurement, conversion, and generation functions. Device features parallel multiple bus architecture and 300-ns instruction cycle time for processing wide bandwidth signals. The 21 preprogrammed routines can be cascaded together with indirect jump instructions to form more complex functions.

Preprogrammed software routines include 2 independent 30-TAP transversal filters that can be cascaded into a single 60-TAP filter, as well as 2 independent recursive filters that provide 16 filter sections. Other preprogrammed routines include signal integration and rectification, μ-Law to linear, linear to μ-Law, and linear to decibel conversions; block multiplication; sine wave generation; and pseudo random noise generation. Independent parallel I/O ports provide interface with any 8- or 16-bit microprocessor, and also linear ADCs, DACs, and μ-Law codecs. **American Microsystems, Inc**, 3800 Homestead Rd, Santa Clara, CA 95051.

Circle 333

SOFTWARE

Multiprocessor OS for the 68000 micro

MTOS-68k realtime, multitasking, multiprocessor operating system is ROMable, modular, and designed for high throughput. System runs on any 68000 configuration; only hardware required is clock for periodic interrupts and lockable bus. All modules are assembly language coded for optimum compactness. The OS manages task coordination, up to 32 memory pools with user allocation/deallocation, I/O, priority scheduling, interrupt processing, and the multiple processors. System accommodates 2048 tasks, and runs on up to 16 separate processors sharing common memory. All processors are equivalent—there are no masters or slaves. One copy of the OS can execute on all processors. Without changing application software, system performance can be improved by adding processors. Application software can be written in assembly language, or in a higher level language such as Pascal or C. Dynamic debugging allows the user to set breakpoints, inspect and change memory, and control task execution. The OS is the latest member of the company's family of realtime, multitasking, multiprocessor operating systems. **Industrial Programming Inc**, 100 Jericho Quadrangle, Jericho, NY 11753.

Circle 334

Software drivers for HP-85 and Apple II

Software drivers AC1818 and AC1820 provide software support to transform HP-85 and Apple II computers into programmable measurement and control systems. Drivers permit a user to monitor and control local or remote process using μMAC-4000 measurement and control system as a front end. Analog input commands can be used for data logging operations. Analog or digital output commands provide realtime control of motors, valves, and actuators. Drivers handle all communications between the host HP-85 or Apple II and the μMAC-4000. User selects 1 of 21 BASIC subroutines by using a GOSUB command. Commands such as SCAN, read several analog inputs; SET, set a digital output bit; SDAC, set an analog output to a specified value; and LIMIT, set a high/low limit for an analog channel, and access a full range of analog/digital measurement and control functions. Each driver includes an application program. **Analog Devices, Inc**, Route 1 Industrial Park, PO Box 280, Norwood, MA 02062.

Circle 335

32-bit realtime operating system

Advanced operating system realtime 32-bit AOS/RT32 is designed for the ECLIPSE[R] MV/ family computers for dedicated applications requiring realtime processing and high throughput. The system is a strict subset of AOS/VS; both AOS/RT32 and AOS/VS can run on the same computer. System supports up to 64 parallel processes, each with a max of 32 tasks. Multiprocessing allows applications to be structured along logical function lines. Internal coordination and communication occur through well-defined system routes. Independent subsystems include process, memory, and task management, and file system,

(continued on page 260)

block I/O, character I/O, and peripheral management. Only segments needed by a specific application are selected for inclusion in the final AOS/RT32 system. Application programs are priority based scheduled.

Max physical memory available on the processor is supported. System calls allow manipulation of the 512M-byte logical address space, consisting of 2k-byte shared pages. Disk can be formatted with std AOS/VS utilities, or left unstructured. Formatted disks can be accessed by either OS, allowing the same pack to be used by both systems. Unstructured disks allow the user to implement application specific accessing methods. System supports FORTRAN 77, PL/1, and DG/L™ languages. Existing library of AOS/VS software development tools can be used. **Data General**, 4400 Computer Dr, Westboro, MA 01580.
Circle 336

High speed CP/M

"Super CP/M" software has increased CP/M speed, with a run time of 230 s, and implementation bootable from any drive, including hard disks and tape drives. Once a system is upgraded, the user no longer needs a system disk. Loader determines memory size and builds the largest system allowed. One version of CP/M is required for all memory sizes. CP/M implementation uses 1024-byte sector sizes, to increase throughput speed by up to 4 times. Increased sector size also allows for 1.26M-byte formatted data on a double-sided floppy disk drive. Error management scheme virtually eliminates data loss due to disk errors. When an error occurs, the logical CP/M device number (A-P) is supplied, along with track, head, and sector number. There is also an error code for any 1 of 13 unrecoverable error types. **Systems Group**, 1601 Orangewood Ave, Orange, CA 92668.
Circle 337

Software displays memory/CPU utilization

VRX-STATUS software allows users of Virtual Resource Executive operating system to display graphic representations of real memory and CPU utilization on a CRT screen. Software consists of two programs, MEMSTAT and CPUSTAT. MEMSTAT multitasked job periodically samples real memory and displays sampled data in 4 formats: specific job display of the last 15 samples of real memory used; all job display of real memory used by each active job; memory map display of total real memory used over the last 15 sample times; and available real memory display of the last 15 samples of available free memory. CPUSTAT multitasked job produces 6 CPU utilization displays in response to parameter cards or unsolicited operator requests. Specific job display shows the last 15 samples of CPU usage. Available display shows the last 15 samples of CPU power available for use during the sample period. Processor display depicts the last 15 samples of total CPU power used in a processor. All jobs display shows CPU power used by each active job in the system, kernel satellite, and CPU power still available at the time of the last sample. MAP display shows total CPU power used over the last 15 sample periods. All time display is identical to all jobs display, except graph shows actual CPU time in seconds rather than as a percentage of total use. VRX-STATS is available for any V-8000 series system having at least one NCR 796-201 or 796-401 CRT terminal with graphics capabilities. **NCR Corp**, Dayton, OH 45479.
Circle 338

UCSD Pascal advanced OS

UCSD Pascal advanced operating system AOS 1.0 provides enhanced program development and source compatibility with existing UCSD Pascal systems. It has compilation UNIT scheme, program chaining, I/O redirection, conditional compilation, and concurrency features of USCD Pascal version IV.0. Dynamic memory allocation schemes of versions IV.0, II.0, and II.1 Apple Pascal can be reproduced. Code segment management is compatible with versions II.0, II.1, and IV.0. Memory required equals that of a II.0 system. Included are one pass compiler, file handler, advanced system editor, spooler, and utilities. No linker is required. The AOS allows modification to, and addition of, I/O drivers, programming of custom exception and breakpoint handlers, and augmentation of the basic operating system. Editor provides extended edit modes, macro execution, nested editing, and change logging. Command language processor allows linked execution of system functions with preprogrammed input and conditional execution. **Advanced Digital Products**, 7584 Trade St, San Diego, CA 92121.
Circle 339

FORTRAN 77 for desktop computers

HP PLUS, a FORTRAN 77 compiler, is claimed to convert approximately 80% of existing FORTRAN programs to HP 9835 and HP 9845 desktop computers. Program provides access to large software libraries written in FORTRAN on other computers, and transports applications in FORTRAN to the company's desktop systems.

A third-party program development system for the compiler, written by International Electronics Machinery, Inc, is available as part of the compiler program. The full OS includes screen oriented text editor, graphics library, HP-IB, and general I/O library, as well as std linker, loader, and compiler/runtime support.

Programs written in FORTRAN are compiled into a pseudocode that is the native language of a hypothetical, stack-oriented pseudomachine. The program development system contains a pseudomachine emulator that executes the pseudocode like native code. Runtime execution is from 3 to 15 times faster than comparable interpreted BASIC programs, depending on the operations performed. **Hewlett-Packard Co**, call local sales office.
Circle 340

Software support for LSI-11 and PDP-11

RSXLIB software support package for DEC LSI-11 and PDP-11 compatible analog data acquisition and control interfaces is designed for use in realtime, multi-task, multi-user programming. Package consists of a set of drivers, configuration command file, and a subroutine library linkable to RSX-11 FORTRAN programs. Combining RSXLIB and analog I/O boards gives increased data aquisition and control for the DEC systems running either RSX-11M or RSX-11S operating systems. Data transfer is supported at the max rate provided by the analog I/O boards. Compatible interface boards available include up to 64 analog input channels; sampling rates up to 135 kHz; choice of 12-, 14-, or 16-bit resolution; optional 1, 2, 4, 8 programmable gain; and thermocouple compensation input option.

Library includes 26 primary subroutines that interface the application program to the appropriate device drivers. Subroutine library provides routines for single-buffer data transfers (single sweep to or from memory), and

(continued on page 262)

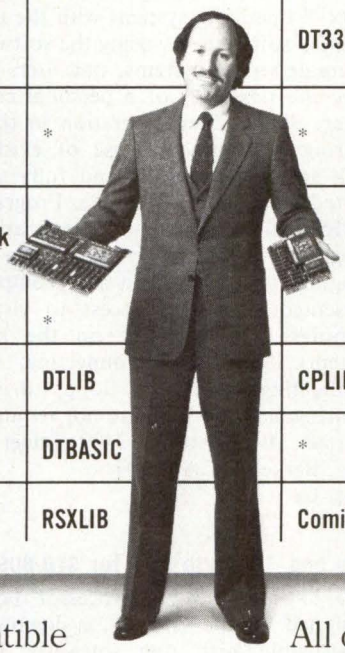
"When it comes to analog I/O, Data Translation will DEC™ you."

Fred Molinari, President

DEC COMPATIBLE BOARDS AND SOFTWARE

	LSI-11™ SERIES			PDP-11 UNIBUS™
	LOW COST **Dual** 12 to 16-Bit Resolution	**DMA** **Dual** 12 to 16-Bit Resolution	**CONTINUOUS DATA** **Quad/Dual** 250kHz A/D	**DMA** **Hex/Quad** 12 to 16-Bit Resolution
Analog Input (16 to 64 Channels)	DT2762 High Level DT2764 Low Level DT2765 Isolated	DT2782 High Level DT2784 Low Level	DT3362 Dual Port DT3382	DT1712 High Level
Analog Output	DT2766 4-Channel 12-Bit DT2767 4-Channel 8-Bit	DT2771 2-Channel Point Plotter	DT3366 Dual Port 8-Channel Expandable DT3371 2-Channel Point Plotter	DT1716 8-Channel 12-Bit
Analog I/O (16 Channels IN/ 2 Channels OUT)	DT2781 High Level DT2785 Low Level	*	*	DT1711 High Level DT1715 Low Level DT1719 Isolated: 4 Ch.
Other Functions	• Analog Expansion • Prog. Real-Time Clock • Parallel Digital I/O • Isolated Digital I/O • IEEE-488	*	• Analog Expansion • Dual Port RAM	*
RT-11™ FORTRAN Subroutines	DTLIB	DTLIB	CPLIB	*
RT-11 BASIC Subroutines	DTBASIC	DTBASIC	*	*
RSX-11™ FORTRAN Subroutines	RSXLIB	RSXLIB	Coming Soon	RSXLIB

*Not available



Nobody supplies more DEC-compatible analog I/O than we do.

We offer peerless hardware and software. Including new high-performance RSX-11 and RT-11 compatible software packages for both LSI-11 and PDP-11. Good stuff.

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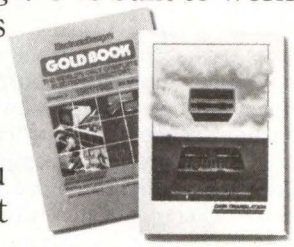

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CIRCLE 154

multi-buffer transfers that allow an application program to process a continuous stream of data and/or to transfer data continuously to or from a mass storage device. Subroutines control programmable gain option, single- or multi-channel operation sampling, A-D sampling rate, D-A output, and A-D sampling mode. Software is available on diskette, disk pack, or magnetic tape. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752.
Circle 341

Simulation software

EXTEND/SP extended facility simulator for the IBM system 370 uses IBM MVS/SP3 system control program without IBM hardware modification. Software is a transparent simulation of the MVS/SP operating system that substitutes std system 370 instruction set for machine instructions introduced in the extended facility. It is available for the 370 uniprocessor, attached processor, and multiprocessing systems, including models 158 and 168. Combined software and MVS/SE or MVS/SP operating systems increase system performance by 12% without added memory. **National Advanced Systems,** 800 E Middlefield Rd, Mountain View, CA 94043.
Circle 342

8086/8088 operating system

Memory resident, multitasking operating system controls operation of 8086/8088 realtime systems. OS package serves as interface between user hardware and application software. By augmenting hardware with software functions capabilities, application software development is simplified. OS access is provided through service calls; resources are allocated to prioritized tasks. Multitasking allows programs performing individual functions of a total application to run concurrently, controlled by events such as external interrupts or realtime clock. Operating system is written in assembly language.

OS includes routines to perform either binary or formatted I/O transfers to logical devices. Formatted transfers are facilitated by an interpreter operating on FORTRAN-like format statements. Programs can be written in any language that generates 8086 object code. Access to executive services is provided to assembly language routines through macros and to high level programs through interface subroutines. The complete operating system occupies 12k bytes of PROM and controls tasks executing with either PROM or RAM. RAM requirements average 256 bytes/task plus program space. **Modular Integration Inc,** 1505 NW Gilman Blvd, Issaquah, WA 98027.
Circle 343

CP/M simulator for DEC systems

BRIDGE CP/M simulator links PDP/11 or VAX systems running RSTS, RSX, or UNIX™ operating systems with the user friendly software. By using the software to create virtual systems, DEC users can have the flexibility of a personal computer. Shared files, operation in time-sharing environments, use of existing high speed peripherals, and fully supported equipment is possible. Programs are loadable similar to other applications programs for the computers. Once the program is requested, a std prompt is presented. User has access to virtual floppies (files resident on the host system). Supporting, connecting, and duplicating terminals, floppy drives, printers, and modems are not required. **Virtual Microsystems,** 2409 Telegraph Ave, Berkeley, CA 94704.
Circle 344

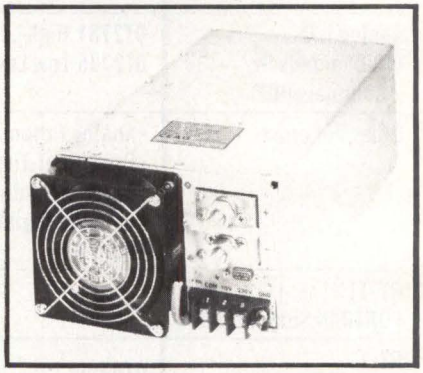
CPU and 16k-byte RAM for STD BUS

STD CPU-Z, an 8-bit processor board designed for the STD BUS, is downward compatible with 8080 software. Unit operates at up to 6-MHz clock speed, and is memory addressable on any 8k-byte boundary with DIP switch. Up to 8k bytes of onboard memory, or 2716 EPROM or Hitachi 6116 RAM chips, can be added. Power on CLEAR generates SYSRESET; on SYSRESET or power-on, unit can jump to any 265k-byte boundary. Baud rate software is selectable up to 19.2k baud. Unit comes with onboard UART for serial communication with terminal/printer, and can be addressed by UART as a 4-port block anywhere on I/O map. CPU, UART, and 8k-byte optional memory functions complete the standalone computing system.

The 16k-byte STD RAM is suited for industrial control or other applications in which nonvolatile storage is crucial. Fully static design improves reliability and makes the device CPU independent. RAM chip is fully socketed for easy maintenance and fully bypassed for trouble free operation in noisy environments. RAM comprises 2 independently addressable 8k-byte blocks, and accepts shadow RAM chips in 1k increments for up to 16k-byte nonvolatile storage. Unit features 300-ns access time and low power consumption. **G & G Engineering,** 13708 Doolittle Dr, San Leandro, CA 94577.
Circle 345

POWER SOURCES & PROTECTION

Single-output 1500-W switchers



Modular single-output switching power supplies model SP4001 provide outputs from 2 to 48 Vdc and up to 1500-W output power. The commercial units have MIL-style packaging and combined line and load regulation is 0.25%, efficiency 70% min. Input for all models is single-phase, 115- or 230-V, 57- to 63-Hz line power. Models can operate at full load over 0 to 71 °C temp range without derating. Noise, ripple, and spikes are less than 100 mV peak to peak. Supplies meet or exceed standards of UL, CSA, and VDE, as well as FCC and VDE emi standards. Features include min 30-ms holdup following power line outage, and parallel operation. Both dc output and ac input overvoltage protection are provided, along with soft-start, remote sensing, and bit output. Basic circuitry is full-bridge inverter with 4 pairs of switching transistors. Transformer-coupled proportional base drive minimizes possible transistor failure due to cross-conduction. Nine std models provide adjustable dc voltage outputs in increments from 2 to 48 Vdc. Output ranges form 2 Vdc at 300 A to 48 Vdc at 35 A. **CEAG Electric Corp, Power Supply Div,** 1324 Motor Pkwy, Hauppauge, NY 11788.
Circle 346

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DATA PRODUCTS, INC.

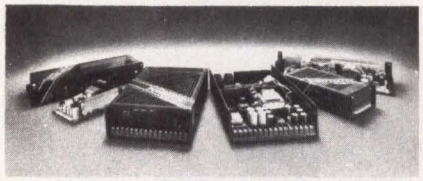
CIRCLE 155

4-channel programmable power supply

Programmable power unit (PPU) is available with up to 4 separate channels, and a choice of 3 voltage ranges for each channel: 0 to ±6 V at 12 A, 0 to ±18 V at 10 A, and 0 to ±32 V at 3.5 A. User can computer control the PPU over either an RS-232 or IEEE 488 bus. Computer controls channel voltage, current limit, and overvoltage point; sets high and low voltage margins; and commands any or all channels to automatically slew about the nominal voltage setting. PPU also enables the host system to read back voltage and current output for each channel. User can increase current capacity of a channel by adding up to 4 external power amplifier units (PAUs) per channel. The optional PAUs are controlled by the PPU. Max current output using 4 PAUs is 252 A for the 6-V channel, 110 A for the 18-V channel, and 57 A for the 32-V channel. Front panel enables manual readback of voltage or current level for each channel on a digital panel meter. The 7.5″ (19.1-cm) high PPU can be mounted in a standard 19″ (48-cm) rack. **Carlton Industries, Inc**, 22661 Lambert St, El Toro, CA 92630.

Circle 347

EMI protected power supply



Series 19 ValuSwitcher™ switching power supplies feature FCC and VDE emi protection and are designed for 50- to 300-W applications. Switchers provide regulated main output and a choice of fully regulated or semiregulated auxiliary outputs. OVP is std on main output and optional on auxiliary outputs. Additional options include power fail signal and cover and brownout protection below 85 or 170 Vac. Input filtering, logic inhibit, ac under voltage, inhibit and remote sense features are std. Full or semiregulation allows the open frame switchers to be used in protected noise margins. Switchers are field strappable and available as openframe or completely enclosed models. Series comprises over 24 models. **PowerTec Inc**, 20550 Nordhoff St, Chatsworth, CA 91311.

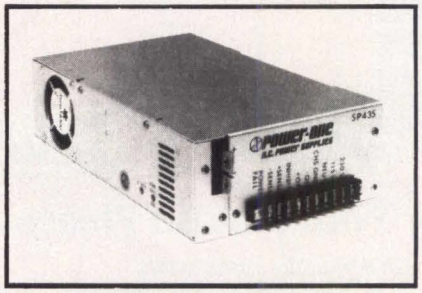
Circle 348

Programmable dc converter

PC77020 20-W dc converter can be programmed for output voltage range of 0 to 40.96 V in steps of 10 mV, and a load current range of 0 to 2.56 A in steps of 10 mA. Both voltage and current control loops are continuously active; crossover between constant voltage and constant control modes is automatic as determined by the more restrictive of either voltage or current reference. A programmed step in voltage is completed in 2 ms. Unit uses 100-kHz switching and power conversion to provide low switching frequency ripple at both input and output terminals. **Interplex, Inc**, 2680 Bayshore Frontage Rd, Mountain View, CA 94043.

Circle 349

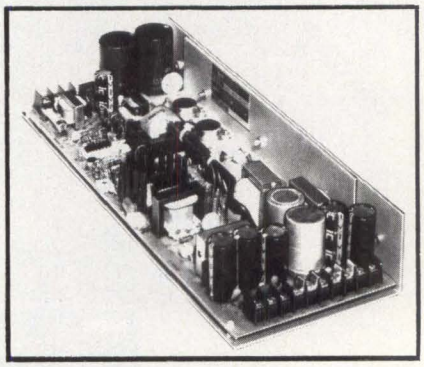
Switching power supplies



SN series switching power supplies provide up to 600-W output power and are enclosed in a 3.4″ (8.6-cm) package. Features include 75% min efficiency and a power to density ratio of 1.8 W/in^3. Voltage/current ratings of models are: SN5-120— 5 V at 120 A; SN12-41.7—12 V at 41.7 A; SN15-40—15 V at 40 A; SN24-25—24 V at 25 A; and SN28-21.4—28 V at 21.4 A. Holdup time of 20 ms min and brownout protection are std, providing immunity to ac line transients and disturbances. Each model features dual-input capabilities of 90 to 130 Vac and 180 to 260 Vac, and internal rfi/emi filtering. Units weigh 9.2 lb (4.2 kg) and measure 12.63″ x 8.0″ x 3.4″ (32.08 x 20 x 8.6 cm). **Power-One Inc**, Power One Dr, Camarillo, CA 93010.

Circle 350

200-W switchers



Series MOX-200 openframe, 200-W switching power supplies provide 4 or 5 voltages and meet or exceed FCC and VDE rfi stds. Five std models include regulated and adjustable ±5-V outputs and a choice of ±12 or ±15 V, or additional 24 or 12 V with high surge current capability. Main control loop regulates 5-V output line and load to ±1%. Second control loop regulates line and load of ±12- or ±15-V outputs to ±2%. Cross regulation of adjustable outputs is ±1%, and on all others ±3%. Output buffering assures high power supply isolation and minimizes crosscoupling. Overvoltage protection is std and all outputs are individually current limited. Typ current ratings are 25 A for 5 V; 4 A for ±12 or ±15 V; 1 A for −5 V; and 8 A peak for 24 V. Supply inputs can be converted from 115 Vac to 230 Vac with jumper. Full regulation during brownout is approximately 75% of input line voltage; holdup time following power outage is 16 ms min under full load. **Todd Products Corp**, 50 Emjay Blvd, Brentwood, NY 11717.

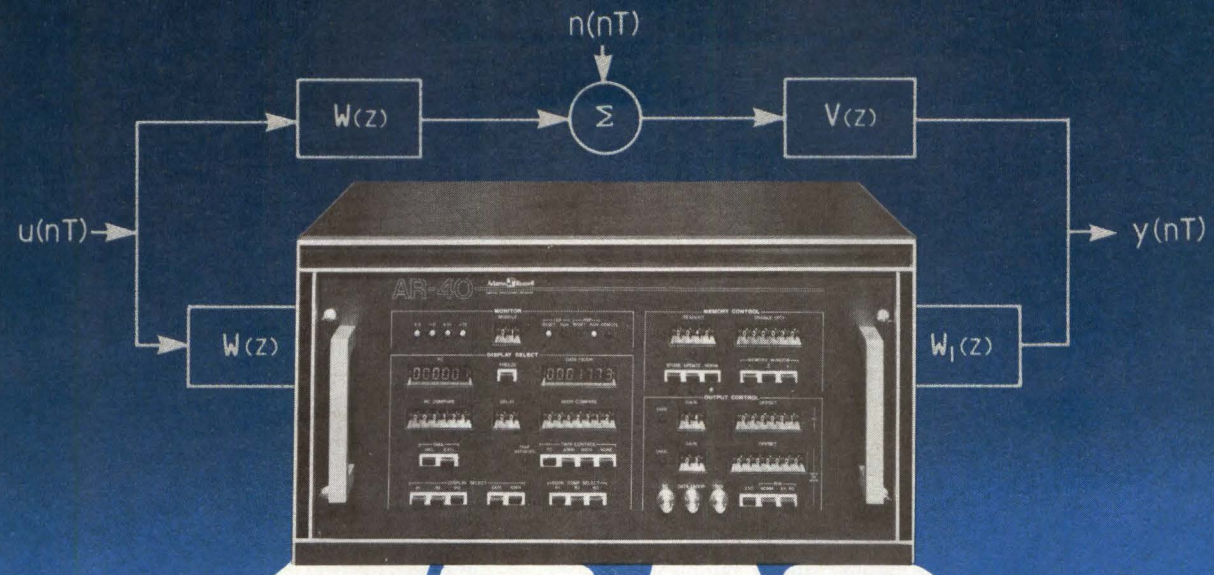
Circle 351

1150-W, 5-output switcher

5-output switching regulated power supply is intended for use in large memory systems where additional power is required. Unit delivers up to 1150 W at 2.20 W/in^3. It is packaged in a std 5″ x 8″ x 13″ (13- x 20- x 33-cm) slot configuration. Supply is equipped with redundant cooling fans. 5-V 150-A main channel and auxiliary channels within the range of 2 to 28 V provide efficiency greater than 65%. Device meets UL and CSA safety stds and FCC emi stds. Other features include overvoltage/overcurrent protection, remote sensing, and massive heatsinking that allows the unit to run indefinitely under brownout conditions. **Qualidyne Systems, Inc**, 2256 Main St, Chula Vista, CA 92011.

Circle 352

Making the Complex Simple.



The High-Speed Signal Processor/Microcomputer

Real-time signal processing calls for very sophisticated computing power. High instruction rates with each instruction doing as much processing as possible. Also, real-time data reduction, analysis and decision-making/control requires branching and testing in its instruction set. High I/O data rates should be supported cleanly to keep your software working at maximum efficiency. And you need easy programmability and effective debugging aids. *That's complex!*

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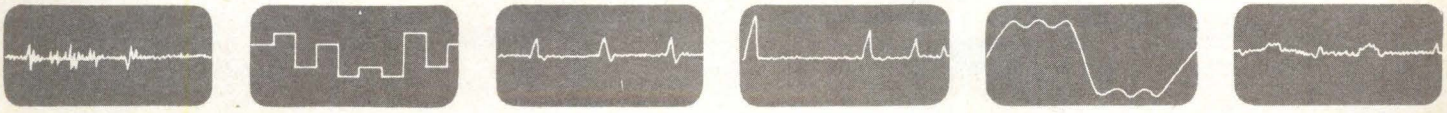
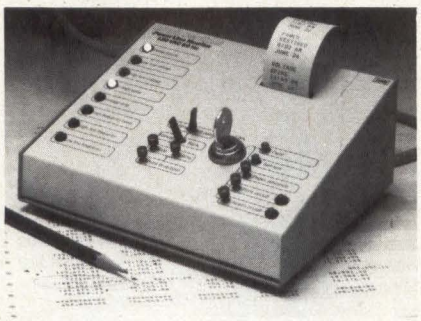


CIRCLE 156

Power monitor with built-in printer



Glitch Sentinel power line monitor GS-2 diagnoses power problems for mini- and microcomputer systems, communication and test equipment, or any equipment that uses std 120-Vac supply. Monitors distinguish between equipment faults and power induced faults. Built-in printer provides documentation of date, time, and type of power disturbances. Monitors check for power failure, low or high line voltage, voltage spikes or drops, high frequency noise, and line frequency errors. With built-in clock, calendar, and audio alert for line disturbances, the Z80 based monitor has factory preset alarm thresholds. Users can also adjust thresholds through a limited range with trim pots. **Billings McEachern Inc**, 333 Cobalt Way, Sunnyvale, CA 94086.
Circle 353

400-W open frame switchers

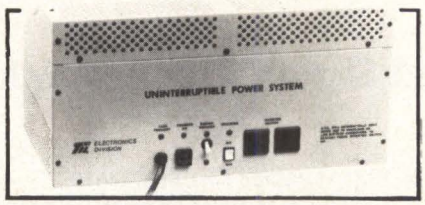
Series NT400 and NQ400 switchers feature triple- and quad-output configurations with semiregulated or postregulated auxiliary outputs. Std input capability ranges from 90 to 132 and 180 to 264 Vac, 47 to 440 Hz. Main output is 5 V at 50 A. Alternate configurations with up to 3 auxiliary outputs are 5, 12, 15, or 24 V at 4 A each, postregulated; 12, 15, or 24 V at 10 A each, semiregulated; and any combination of 4-A postregulated or 10-A semiregulated outputs.

Unit measures 16.87″ x 6.0″ x 2.75″ (42.85 x 15 x 6.99 cm); op temp range at 70% typ efficiency is 0 to 50 °C. Holdover storage is 16 ms min. Ripple and noise are 50 mV peak to peak in main output and postregulated auxiliary outputs, and 1% of nom on semiregulated auxiliary outputs. Transient response recovery to within 1% of nom output voltage occurs within 500 μs for 25% load step. **National Power Technology**, 2111 Howell Ave, Anaheim, CA 92806.
Circle 354

Pulse width modulating regulator

Pulse width modulating regulator XR-2230, for use in switching power supplies, contains a sawtooth generator, 2 error amplifiers, and logic control that drives 2 open collector power transistors. The 18-pin regulator features protective thermal shutdown to prevent damage to the chip in the event of overheating. High speed remote shutdown input protects the circuit being driven. Error amplifiers, with ±5-V input, allow the user to set predictable output voltage and current. Input voltage range is −18 to 18 V, regulator outputs voltage in a range of −0.5 to 18 V. Op temp range is 0 to 75 °C. **EXAR Integrated Systems, Inc**, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088.
Circle 355

Uninterruptable power supply



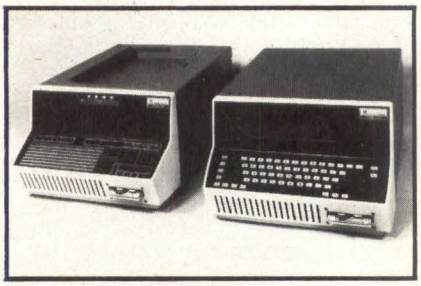
Uninterruptable power supply is designed to maintain circuits during loss, drop, or dip, and delivers 400 W in clean, sinusoidal ac format. The UPS provides battery output that is recharged from a std power outlet. Batteries completely isolate downcircuit components from power line and continue ac output for a min of 20 minutes during power outage, preventing memory drop. Output is within 3% total harmonic distortion held to a crystal controlled clock frequency. During rated 133-Wh interval, output is pure, regulated, and sinusoidal. Automatic shutoff prevents battery damage during extended blackout. Indicators provide continuous monitoring of UPS operational modes. Std voltage output is 120 Vac, single-phase with ±3% regulation, 60 Hz ±0.1%, and sine wave with 3% max harmonic distortion. Op temp is 0 to 40 °C. **TII, Electronics Div**, 1375 Akron St, Copiague, NY 11726.
Circle 356

TEST & MEASUREMENT

Digital IC test system

Model 1732M digital IC test system is a microprocessor controlled benchtop unit for dc parametric and functional testing of both SSI and LSI devices. Tester includes all features of the std 1732 IC tester, plus increased multiprocessing operation, menu programming with user defined forceI/measure V or forceV/measure I on any pin, increased binning and failure categorizing/results reporting capabilities, isolation tests on unused pins, and compatibility with the 1732 program library. Three processors are used for throughput testing and interactive control between system and operator. Z80 microcomputer with 128k-byte RAM controls the system and operates the CRT display. Magnetic tape unit is operated by a second processor. A third processor for pattern generation applies test vectors at rates up to 2 MHz while implementing subroutine and loop instructions. Test vectors are stored in pattern memory with 4k- x 4-bit storage for each drive/sensor pin. DC parametric measurements are made by switchable system under software control to any test pin. Parameters are checked against internal precision voltage source and automatically calibrated software. Interface is through IEEE 488 bus and RS-232, or 20-mA current loop. **GenRad, Inc**, 170 Tracer Lane, Waltham, MA 02254.
Circle 357

20-MHz functional test system

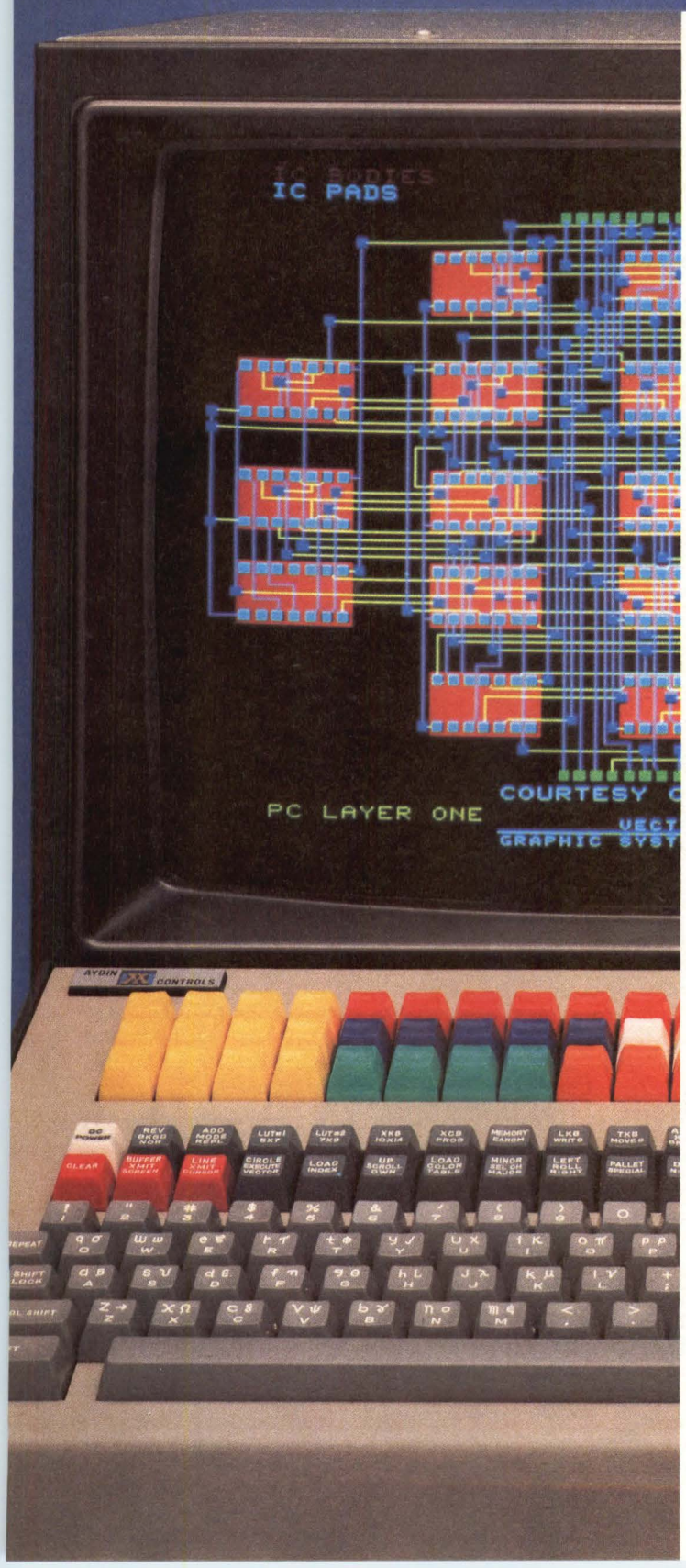


Sophisticated pin electronic design enables the 3PX800 test system to operate MSI, VLSI, and microprocessor based logic assemblies at realtime operating speeds. Pass/fail testing and automatic or manual diagnostics identify latent dynamic faults within a controlled environment. Bidirectional capability, achievable in real time at a 20-MHz rate, allows fully interactive microprocessor board testing at function speed. Serial and parallel data application modes are available. Computer directed guided

(continued on page 268)

Quickens Your Draw

Aydin user-oriented, full-color graphic systems let you tackle complex design and processing projects quickly and easily.



Aydin 5216 high-resolution multiprocessor-based color graphic systems lead the industry in fulfilling the needs of intricate process control CAD/CAM, simulation, C³I, image processing and many other sophisticated applications.

Versatility is the result of the Aydin growing family of hardware and 2D, 3D, imaging and CORE software modules. The 5216 gives you both the flexibility and programmability to design and implement your ideas efficiently and economically; a true man-machine interface. For example, AYGRAF instruction sets provide both standalone and distributed processing capabilities to support 2D graphics in a standardized manner. The 3D system, which supports standalone and host-driven applications, is designed to give the user the full benefit of sophisticated graphics, all with interactive control that doesn't burden the host computer.

Aydin modular design also means that you can customize the 5216 to your strictest requirements, easily expand memories, add storage and utilize various user-programmable lookup tables. In addition, a host of interactive devices are available, including joysticks, trackballs, graphic tablets, touch panels and lighted or non-lighted function keys.

It all adds up to a user-oriented 5216 color system that is a reliable, flexible and economical solution to your graphics and image processing needs. Quicken your draw with Aydin, the industry leader in high-resolution, intelligent color graphics. For more information, contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel.: 215-542-7800. (TWX: 510-661-0518.)

Leadership Features:

• High-performance multiprocessor bus architecture • Pixel or graphic DMA block mode data transfer (800 nanoseconds per 16-bit pixel) • Multiple pixels per word • Wide selection of display formats up to 1024 x 1024 x 16 • Video processing through lookup table RAM at bit rates to over 40mHz • High-speed hardware vector and character generation • Four sizes of alpha characters • High-speed hardware math • Both parallel and serial peripheral interfaces available • User programmable • 16-Bit microprocessor.

AYDIN CONTROLS

CIRCLE 157

probe isolates faults on board under test; IC pins to be probed are identified on the display.

Std configuration of 64 bidirectional TTL driver/sensor pins is expandable to 256 in 32-pin groups. Pin memory of 1024 bits allows preloading and broadside application of 20-MHz data across 256 pins simultaneously, and test software can expand this 1024-bit capacity through realtime subroutines. **Three Phoenix Co**, 21639 N 14th Ave, Phoenix, AZ 85027.

Circle 358

Semiconductor tester

Model 5150 discrete semiconductor tester monitors triacs, SCRs, transistors, opto couplers, FETs, zener diodes, and diodes. Resident prompt sequence programs define 32 device tests that appear on the alphanumeric display. Optional program storage uses 2716 EPROM programmer/reader. Test time is typ 50 to 300 ms depending on number and limits of tests. Parameters are measured and displayed through successive approximation routine included as std in the unit. Handler interface is std for single pass/fail result. Binning option provides 8 relay contacts to the handler. Other interfaces available include RS-232-C, CRT terminal, and additional memory. Special tests can be created to accommodate multiple-pin assemblies. **Scientific Test, Inc**, PO Box 40811, Garland, TX 75040.

Circle 359

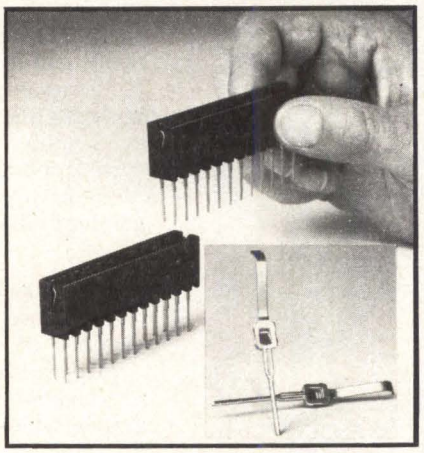
EPROM/PROM programmer

Zero hardware redundancy allows programmer via terminal strips to connect to I/O RS-232 devices, power supply, and computer. Programmer is Z80 based, with 4k-byte RAM, firmware in two 4k 2716 EPROMs, and 48 parallel I/O pins. Two RS-232 data ports provide transfers in 19.2k bps max. Data can be burned into most std EPROMs/PROMs; protocols for 15 std PROMs and EPROMs are internal. DIP sized wirewrapped headers are dropped into 2 ZIF sockets—the only hardware alterations required for new EPROMs. System can be used in standalone mode, communicating with an RS-232-C compatible terminal. Terminal controls programmer's operation and provides data to be burned in EPROM. In computer driven mode, a computer is used for short production runs or rapid prototyping of EPROM programs. File transfers occur in hexadecimal format. Programmer can operate in transparent mode for communication between terminal and host computer. **P&E Microcomputer Systems**, PO Box 2044, Woburn, MA 01888.

Circle 360

INTERCONNECTION & PACKAGING

Discrete edge connector PCB interface



Discrete edge connector series 157-1118 utilizes a compliant pressfit contact that interfaces to a PCB without soldering. Connector can be assembled inhouse, contact can be removed from the top rather than removing the entire insulator. Connector is designed for use in computers, telecommunications, instrumentation, and computer peripherals. Insulator material is polyester and conforms to UL rating of 94VO. Modular in design, contact positions available are 2 to 24 on a 0.200 x 0.200 grid. Contact platings available include gold, selective gold, solder plate, and unplate alloy 725. **Methode Electronics, Inc, Connector Div**, 7447 W Wilson Ave, Chicago, Il 60656.

Circle 361

Fiber optic connectors

Series of fiber optic connectors satisfy military requirements and feature combined coupling of split tube and bushing for precise axial and angular alignment, as well as interface gap control. Reliability testing of 500 mating/unmating cycles resulted in no significant degradation of insertion loss. Seals protect connectors from adverse environments. One connector can accommodate a range of fibers from 100 μm to 1.16 mm. Std connectors available include multichannel circulars in 2-, 4-, and 6-channel hermaphroditic designs; multichannel rectangulars for mixing of fiber optic, coaxial, and power contacts; custom designs for PCB mounting; and single-channel connectors. **Hughes Aircraft Co**, 17150 Von Karman Ave, Irvine, CA 92714.

Circle 362

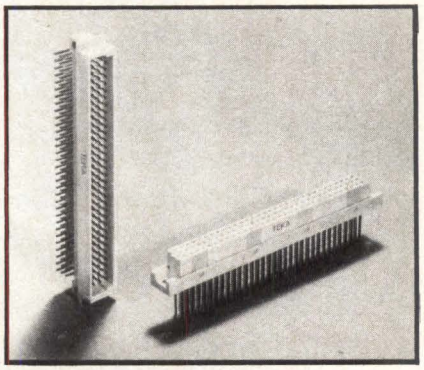
Ribbon/flat cable interface socket assembly

Ribbon or flat cable socket assembly RIS is designed to speed wiring connections and uses discrete wiring for mating. The track mountable assembly consists of a PCB, ribbon connector, and 2 terminal blocks. Track mounting provides assembly ease for single or multiple units. Track comes in 48″ (122-cm) lengths and holds from 7 to 16 RIS assemblies. Headers feature positive acting, snap type hook retainers and are designed to mate with all std connectors. Terminal blocks are made of break resistant thermoplastic material. **Curtis Industries, Inc**, 8000 W Tower Ave, Milwaukee, WI 53223.

Circle 363

Eurocard connector system

Eurocard DIN connector system is a precision 2-piece unit available in densities of 96-contacts/housing—3 rows, 32/row—on 0.1″ (0.25 cm) pitch; and 64-contacts/housing in 2 rows. Terminations offered are solder dip or wire wrappable. Pin arrangements and plating options include gold and tin alloy; std or reverse mounting configurations are available. System conforms to European IEC 603-2 and VG95324 standards and MIL-C-55302 specs. **Teka Products, Inc**, 60-06 39th Ave, Woodside, NY 11377.



Circle 364

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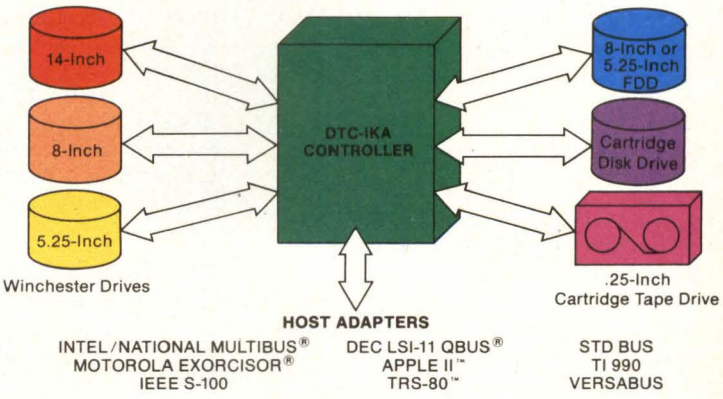
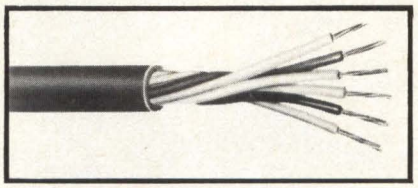
OVERVIEW



Data Technology Corp.
2775 Northwestern Parkway
Santa Clara, CA 95051
Telephone: 408-496-0434, Twx: 910-338-2044

Control and audio cable



Unshielded multiconductor control and audio cable is designed for control and processing, communications, and instrumentation systems. Insulation is color coded polyvinylchloride over cabled, stranded tinned copper conductors; jacket is grey polyvinylchloride. Features include voltage rating of either 150 or 300 V and a temp range of either 60 or 80 °C, depending upon the particular UL style. Cables are resistant to acids, alkalis, oils, moisture, solvents, and fungus, and are manufactured using CSA approved inner conductors. **Dearborn Wire & Cable Co,** 9299 Evenhouse Ave, Rosemont, Il 60018.

Circle 365

Coaxial cable connectors

Heli-Grip series BNC and TNC coaxial cable connectors offer a tapered helical gripping surface and a series of annular retaining rings that provide reliable connection and moisture barrier. Connectors reduce cable preparation time by 50% and can be field assembled or replaced without special tools. Intended for small and medium coaxial cables, connectors can withstand cable pullout forces of 85 lb (39 kg) max when used with RG-59/U cable. Connectors meet or exceed all requirements of MIL-C-39012, Class 2, Category A. **Delta Electronics Corp, Inc,** 93 Park St, Beverly, MA 01915.

Circle 366

MEMORY SYSTEMS

5.25″ Winchester and flexible drive combination

A 5.25″ Winchester drive and a Winchester/flexible disk drive combination offer high speed, large capacity mass storage for the company's personal, desktop, and microcomputer systems. The HP 9134 Winchester drive provides 4.6M-byte (6.38M-byte unformatted) capacity, with 45- to 60-ms access time. Tape or flexible disk drives within computer systems become backup devices when the Winchester drive is attached. Drive controller emulates an HP 9895A 8″ flexible disk master with 3 slaves, allowing several mass storage ROMs supporting the 9895A to also drive the Winchester. All software currently used by the 9895A can be used on the Winchester without change.

For larger backup capacity, and an 8″ format, model HP 9138 combines an HP 9134 Winchester and an HP 9895A 1.15M-byte single flexible disk drive in separate enclosures. A combination mass storage unit, the HP 9135 includes the 4.6M-byte Winchester and the company's 5.25″ 270k-byte flexible disk drive, both in a single enclosure. Model provides the same high speed and large capacity as the 9134 and features removable medium and backup capability of the flexible disk. Model is targeted for the HP series 80 personal computer. **Hewlett-Packard Co** (contact local sales office).

Circle 367

8″ rigid disk and controller

Model 4181 8″ rigid disk provides 13.5M-byte formatted, 6.75M-byte fixed media, and 6.75M-byte removable media storage. Features include front loading, high throughput, and microprocessor based logic. Controller model 4180 mounts in any std CPU and can control up to two 8″ drives or any combination of 26M-, 67M-, or 256M-byte single-port drives. **Modular Computer Systems, Inc,** 1650 W McNab Rd, Ft Lauderdale, FL 33310.

Circle 368

DEC compatible semiconductor add-ins

Semiconductor add-ins for DEC PDP-11 minicomputers and LSI-11 microcomputers are based on 64k RAM devices. Hex board models (each 1M byte) are DR-214 and DR-244 for the PDP-11 series, and the dual-board DR-215 (256k bytes) and quad-board DR-213 (1M byte) are for the LSI-11/23 series. Both -214 and -244 provide 22-bit addressing in configurations up to 4M bytes and are strappable in 2- or 4-way interleave. DR-214, compatible with the 256k-byte MS11-LD memory, is organized as 512k x 18 and has onboard parity control. It will operate in PDP-11/24 and -11/44 minicomputers; -244 is designed to provide error correction check (ECC) in the PDP-11/44 system. It functions as a 512k x 16 memory system, although internally configured as 256k x 39. Internal 39-bit word consists of two 16-bit words plus 7 ECC bits.

DR-215 is fully compatible with the MSV11-LK memory module. Full-function parity control with control status register and 22-bit addressing are std. DR-213 provides byte parity bits in a 512k x 18 configuration, but parity control must be supplied externally with a parity controller board. 22-bit addressing is std. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512.

Circle 369

LSI-11 streaming cartridge tape emulates DEC system

DEC LSI-11 compatible controller with streaming cartridge tape drive, LSI-30 integrates 30-ips DEI streaming tape drive and emulates DEC TM-11 tape system. Controller provides file oriented backup/restore operations under std DEC utilities at typ 1.5M-byte/min transfer rate. Each cartridge stores up to 20M bytes. Operating on 5 Vdc at 2.2 A, system is configured as a single quad-size controller. Optional LSI-30/P configuration allows offline de-spool of tape data to a serial printer with no need for operator or LSI-11 intervention. Controller is priced at $2480 as tablemount subsystem. **Alloy Engineering Co, Inc, Computer Products Div,** 12 Mercer Rd, Natick, MA 01760.

Circle 370

Multishared memory subsystem

Multishared memory subsystem MSM-1 permits linking of up to 4 Q-bus or UNIBUS systems to provide faster data access and improved communications between multiple processors. Subsystem provides a memory block from 4k to 64k bytes that can be shared by any combination of 2 to 4 LSI-11 and PDP-11 computers. Shared memory is configured on an 8-slot quad-board backplane housed in a rackmountable 19″ (48-cm) box connected via 50′ (15-m) shielded cables. Memory can be mapped at different addresses for each computer. Mapping includes 18 bits of address for UNIBUS systems and 22 bits of address

(continued on page 273)

The Pragma non-streamer... *non* is better

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CIRCLE 159

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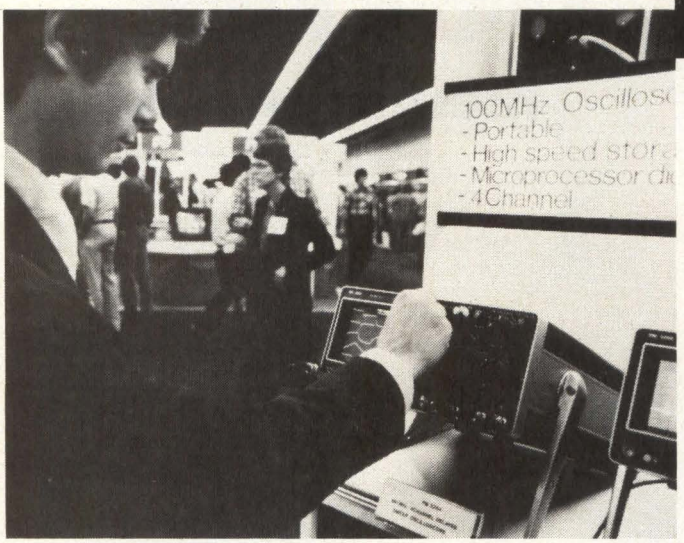

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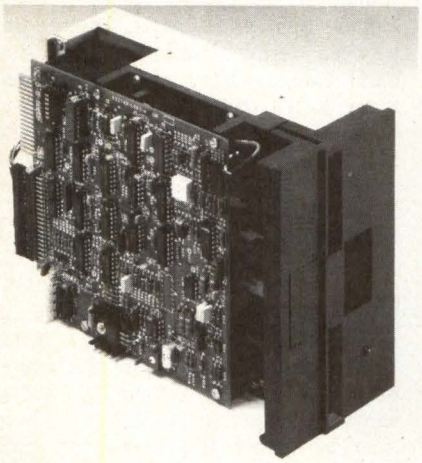
CIRCLE 160

for Q-bus computers, in 4k base address increments. Any computer sharing memory can send up to 2 vectored interrupts to any other computer in the configuration, as well as a simultaneous broadcast interrupt to all computers. Base address, interrupt level, and priority are all switch-selectable for each computer. Optional watch dog timer monitors all systems sharing memory; if any one CPU does not respond to timed interval polls or interrupts, the system assumes the CPU has failed and notifies any or all computers sharing memory. **Ranyan Computer Enhancement Systems,** PO Box 790, Huntington Beach, CA 92648.
Circle 371

Band/stepper mechanism



Band/stepper motor mechanisms FDD 111-5 single-head (48 tracks/in) and FDD 221-5 double-head (96 tracks/in) improve accuracy of head positioning in series of 5.25″ flexible disk drives. Drives incorporate proprietary band/stepper motor head positioning to provide high speed access and temp compensation allowing more accurate tracking of media size changes due to temp fluctuations. Head can be aligned by moving stepper motor without adjustments to capstan or band. For single-density applications, FDD 111-5 accommodates up to 125k bytes of unformatted data; double-density (MFM encoding) device provides unformatted storage to 250k bytes on each side. For single-density applications, FDD 221-5 accommodates up to 500k bytes of unformatted data; double-density recording (MFM encoding) gives unformatted storage capacity to 1M byte. Both drives can have up to 4 units daisy chained on a single bus for 4M-byte online data storage. Track to track access time of 5 ms produces a random average access time of 80 ms for 40 tracks (FDD 111-5) and 146 ms for 80 tracks (FDD 221-5). Data are transferred at 125k bps with single-density or 250k bps with double-density. Power consumption is 13.5 W operating and 8 W standby. **Siemens Corp, OEM Data Products Div,** 240 E Palais Rd, Anaheim, CA 92805.
Circle 372

5.25″ Winchester with backup

MiniMega 5.25″ hard disk and floppy backup subsystem is designed to work with most microprocessors through host adapters. Use of existing operating and applications software is extended so that all CP/M programs will run with machines now using CP/M. With the addition of the MicroSoft Z80 Softcard, Apple II users can also use Z80 CP/M programs. Error correction coding (ECC) feature corrects media errors, making them transparent to the host computer. Subsystem contains an onboard microprocessor for independent functioning of the host computer CPU. Disk is available in 5M- or 10M-byte configurations, or integrated with a 5.25″ 1M-byte floppy backup. Included with the disk system are controller, host adapter, operating software, power supply, cable, cabinet, and operating instructions. **Santa Clara Systems,** 560 Division St, Campbell, CA 95008.
Circle 373

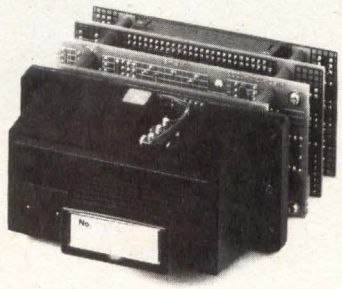
Winchester mass storage

Two ISIS-II compatible Winchester mass storage subsystems, models 4030 and 1010, provide 29M and 10M bytes of unformatted storage, respectively. Units are totally transparent with Intellec 800 series II and III. Model 4030 features a 14″ Winchester disk; model 1010 has an 8″ Winchester. Both models include an 8″ double-density floppy disk for program load and backup. Single MULTIBUS host adapter card plugs directly into the host development system, and is connected by 1 cable to either disk system. Host interface controls bus as a master during DMA transfer operations. Controller, disk, and transfer faults are flagged and retried; disk data are corrected with 48-bit ECC. Units are divided into virtual partitions that to the Intellec system appear as std Intel disk subsystems. Users address logical drives; no change in system commands is required. Model 4030 Winchester transfer rate is 7.1M

(continued on page 274)

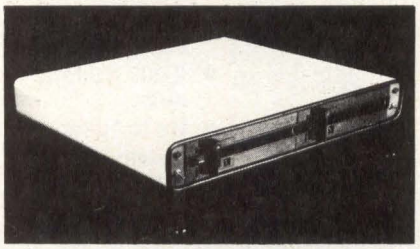
baud. Average access time is 64 ms; track to track access time is 20 ms. The 8″ Winchester transfer rate is 4.34M baud; average access time is 70 ms; track to track access time is 19 ms. **Data Management Labs**, 2148 Bering Dr, San Jose, CA 95131.
Circle 374

32k-byte bubble cassette system



A configuration of the company's 32k-byte bubble cassette system has modular type holder with built-in control card. Peripheral circuits are designed for ease of attachment to other equipment, such as test and measurement equipment and portable recorders. Maintenance-free system has no moving parts and is suitable for external memory applications in severe environments. Cassette is built to withstand dropping, vibration, and dust. Average access time is 7.5 ms; in 3 s 32k bytes can be transferred. The 8-bit parallel interface can be connected to any type of microprocessor. System memory can be expanded to 128k bytes by combining 3 FBM-U004 slave holders to the FBM-U404 master holder. A special nonexpandable holder FBM-U404P operates in a temp range of −30 to 70 °C. **Fujitsu America, Inc, Component Sales Div**, 918 Sherwood Dr-23, Lake Bluff, IL 60044.
Circle 375

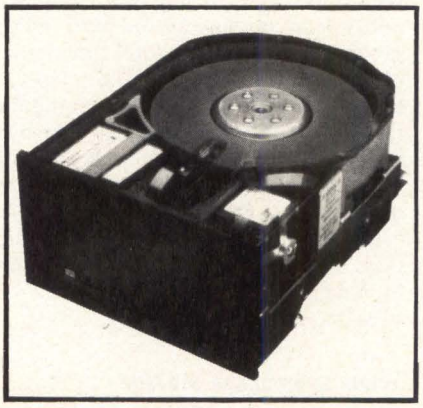
4-drive subsystem



CMS 1600-4 8″ disk driver subsystem provides twice the storage capacity of std drives in half the space. Subsystem utilizes 4 Tandom Thinline™ DS/DD 8″ drives. Drives are one-half the thickness of std drives, enabling the entire unit to be enclosed in the space of a std 2-drive cabinet. Storage capacity is 4.8M bytes. Subsystem uses std Shugart compatible interface for 8″ CP/M disks, and includes power supply, cables, and a choice of cabinets. **Columbia microSystems, Inc**, 905 E Broadway, Columbia, MO 65201.
Circle 376

12M-byte 5.25″ disk drive

ST412 5.25″ micro-Winchester disk drive features 12.76M-byte unformatted storage and 10M-byte formatted storage. The drive utilizes manganese-zinc heads and a stepper motor design for higher track density; ST412 offers double the storage capacity of the ST506 in the same form factor and with complete compatibility to allow use of the same interface, power supply, and controller design. Onboard microcomputer provides buffered seek and a fast step algorithm, and maintains compatibility with the ST506. **Seagate Technology**, 360 El Pueblo Rd, Scotts Valley, CA 95066.



Circle 377

Cache disk system

Disk drive subsystem group 3000 has storage of up to 600M bytes and 4 cache options for HP 3000 series 30, 33, 40, 44, and 64 central processors. System emulates the HP 7925 disk drive system and has features to emulate the HP 7935. The 360M-byte capacity can be expanded in field installable 120M-byte increments to the full 600M bytes. Microprocessor based controller can support a total capacity of 1.92G bytes. Seek and latency times are 20.33 ms. Dual I/O ports facilitate operation with 2 processors. Cache options include storage configurations providing 200% to 300% increased data throughput by eliminating mechanical delays inherent in the disk drive. **Qualex Technology Inc**, 31220 LaBaya Dr, Westlake Village, CA 91362.
Circle 378

Mini-floppy terminal

Mini-floppy RS-232 storage device MiniMate III provides up to 408k of storage on a single-sided diskette. Operation is code switchable 7-bit ASCII or 8-bit binary. Binary operation stores 8-bit program codes for microprocessor and machine tool applications, allowing paper tape units to be replaced by the 5.25″ diskette. Device includes file management system, and is provided with automatic and manual controls for standalone operations. Other features include dual RS-232 ports for insertion between terminal and modem; dual band rates and answerback message; X-ON, X-OFF code response; power-up restart during ac power failure; and automatic disk motor timeout to extend disk life. **Western Telematic Inc**, 2435 S Anne St, Santa Ana, CA 92704.
Circle 379

ROM emulator

HHP-16k EPROM memory for the HP-41C/CV calculators has low power requirement and 4k-, 8k-, and 16k-storage capacity increments. Device is a system ROM emulator. Box connector cable plugs directly into 1 of the 4 ports at the top of the calculator. EPROM box address is DIP switch-selectable with additional flexibility of plugging the EPROM box into any of the port openings. Two boxes can be simultaneously plugged into the HP-41CV calculator for a total 32k storage positions for program and table data. Average running current is 1.7 mA. Device is produced either with or without ZIF sockets. **F.M. Weaver Associates, Inc**, 6201 Fair Valley Dr, Charlotte, NC 28211.

Circle 380

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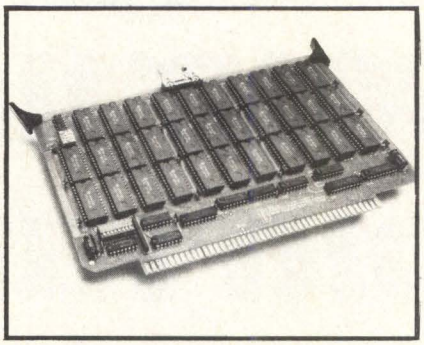
64k static CMOS RAM



Module 9638 64k-byte static CMOS RAM is designed for operation with the M6800/6809 microprocessor bus. It is pin and outline compatible with the Motorola EXORciser and Micromodules. Module provides over 65.5k bytes of storage when fully populated to 64k bytes. Partially populated versions providing 32k-, 48k-, and 56k-byte storage are also available. Unit is configured as eight 8k blocks that can be independently placed in the memory map by onboard switches. Module also provides for decoding of 4 additional address lines for use in memory management systems. Typ access time is less than 200 ns. Power required is 150 mA typ from a single 5-V supply. **Creative Micro Systems**, 3822 Cerritos Ave, Los Angeles, CA 90720.

Circle 381

Apple compatible disk drive

A 5.25″ disk drive for Apple systems has compatible operating systems and software for plug-in and run reliability. Added power, speed, and flexibility are provided with disk storage. The 40-track drive is priced at $395; 80-track version is $495. All units include enclosure, connecting cables, and warranty. **A.M. Electronics, Inc**, 3446 Washtenaw Ave, Ann Arbor, MI 48104.

Circle 382

Dynamic memory board

CI-6800-2 dynamic memory system is designed for operation with EXORciser I and II and the AIM 65 system. Memory is available in 16k, 32k, 48k, or 64k configurations. Board plugs directly into existing EXORciser connectors. System has onboard hidden refresh control logic. Access time is 225 ns; cycle time of 400 ns allows unit to operate as a static RAM at clock rates in excess of 1.5 MHz. Board can be configured to utilize a clock stealing refresh for 2-MHz operation. Onboard memory select is in 4k increments up to 64k on either VUA or VXA control inputs. Memory has onboard even parity with output jumper, selectable to the system bus as parity error or nonmaskable interrupt. Power consumption is less than 7 W. **Chrislin Industries, Inc, Computer Products Div**, 31352 Via Colinas, Westlake Village, CA 91361.

Circle 383

Intelligent floppy disk system

Intelligent 8″ floppy disk system I-47 is compatible with Heath/Zenith hardware and software, and produces automatic density sensing/switching and copying/formatting. System consists of 2 double-density, double-sided 8″ drives with 1.25M-byte formatted capacity/drive in a master/slave relationship. Up to 3 slave drives can be daisy chained to the master for capacity in excess of 5M bytes. A 6800 microprocessor on the master drive automatically handles all control and formatting functions, and gives direct access to signal status. System supports 5 single-density and 8 dual-density disk formats. A 128-byte sector format capability in dual-density encoding is also available. **Data Compass, Peripheral Products Div**, 2730 Regal Park Dr, Anaheim, CA 92806.

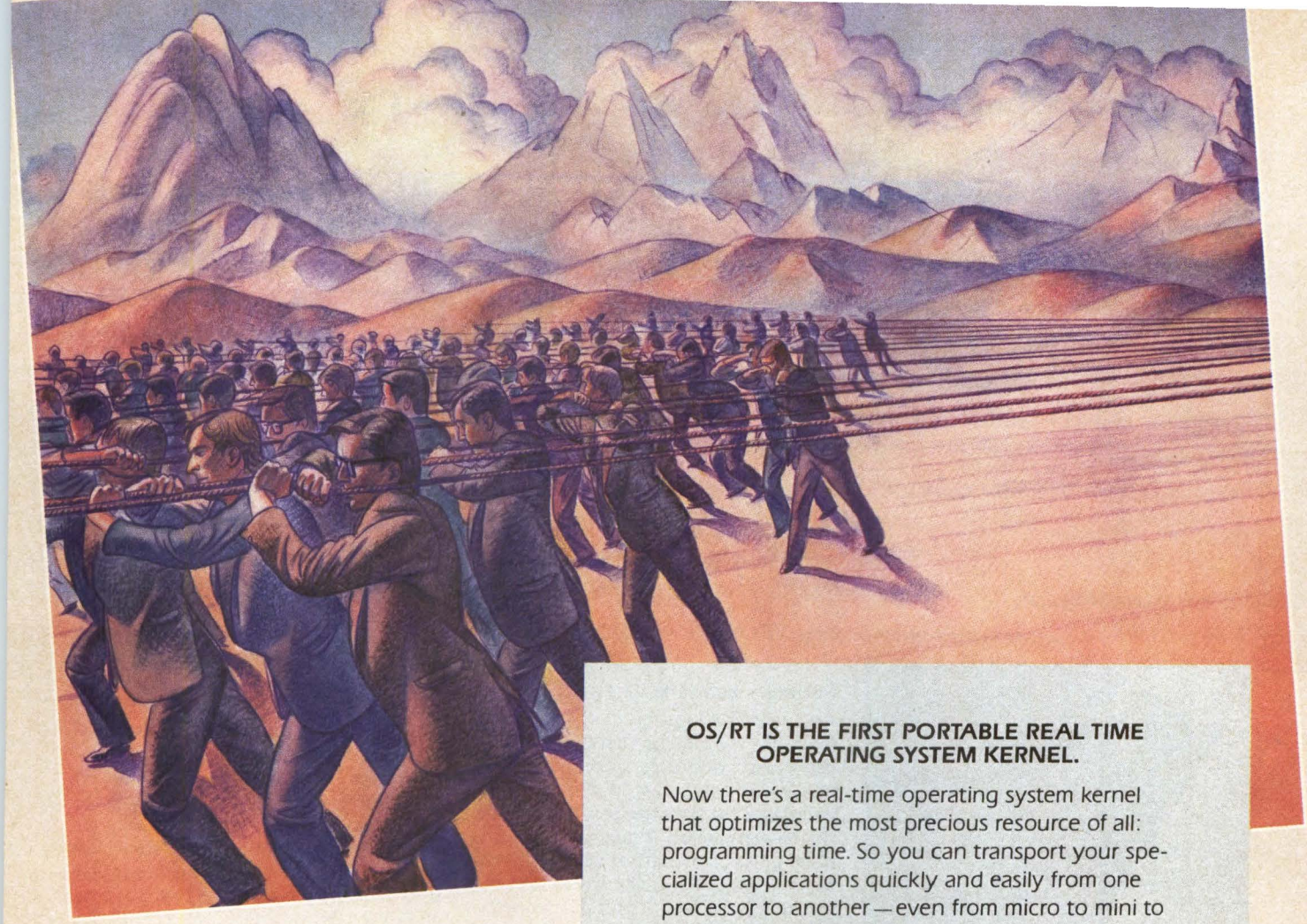
Circle 384

SYSTEM ELEMENTS

Fiber optic data link

FOT110 and FOR110 fiber optic transmitter and receiver, together with fiber optic cable, form digital data and analog signal link. TTL data up to 2M baud NRZ applied to transmitter input is converted to an optical signal. Signal is accepted by the receiver and reproduced as TTL data at its output. Receiver has Auto Threshold™ adjustment, including a squelch function. True dc response is achieved; recovery scheme is independent of data pattern. An analog signal of 10 Hz to 1 MHz can also be transmitted with high linearity. Link lengths greater than 1.7 km can be obtained with silica fibers. Link lengths up to 7 km without repeaters are possible with the infared (IR) transmitter version. Hybrid package permits PCB mounting. FOT110 transmits at data rates of 0 to 2M baud. It can transmit an analog signal by amplitude modulation simultaneously with digital

(continued on page 278)



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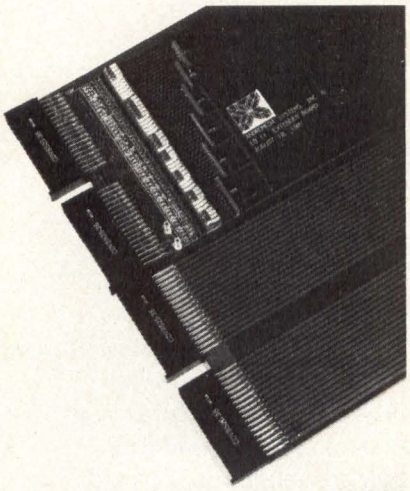
TTL signal over 1 cable. Pin selectable LED phasing can be used to generate biphase data through the link. FOR110 high sensitivity receiver is capable of 0 to 2M baud NRZ typ. Data thresholds are continuously set for max noise immunity. A single external capacitor can reduce bandwidth to lower bit error rate and increase sensitivity at low baud rates. **Burr-Brown Research Corp**, International Airport Industrial Park, PO Box 11400, Tucson, AZ 85734.
Circle 385

Q-bus extender board



Model EB11 switchable extender board provides line isolation capability for Q-bus systems. Each data and control line comprising the Q-bus can be isolated through banks of miniature switches. Pullup resistors are provided on switch card side to maintain a high (negated) state if line is system controlled. All Q-bus control signals are brought to 1 row of tests points on either the Q-bus side or 1 row on the board under test side of the isolation switches. Test points are in functional order, rather than in physical order of the Q-bus connector. Terminals are provided with 5-V connection for measurement or auxiliary circuits. Extender board is available in quad-widths (EB11) or dual-widths (EB11/2). Both models are $250, quantity one. **Andromeda Systems, Inc**, 9000 Eton Ave, Canoga Park, CA 91304.
Circle 386

Replacements for tantalum capacitors

Single-ended miniature aluminum electrolytic capacitor type 510D is designed as an alternative for solid tantalum devices. Capacitor has parametric stability approaching that of solid tantalum units. Units operate over temp range of −40 to 125 °C. At full rated voltage, dc leakage current ranges from 1 to 5 μA. Dissipation factor limits at 120 Hz range from 6% to 18%, with typ values at 50% of the specified limits. Std capacitance tolerance is ±20%. Capacitors are supplied in 6.3-, 10-, 16-, 25-, 35-, 50-, and 63-Vdc ratings, in 5 std case sizes, with thermoplastic insulating sleeves and straight wire leads. Capacitance values range from 1.0 to 33 μF. A polymer coated end seal is optional. **Sprague Electric Co**, 555 Marshall St, North Adams, MA 01247.
Circle 387

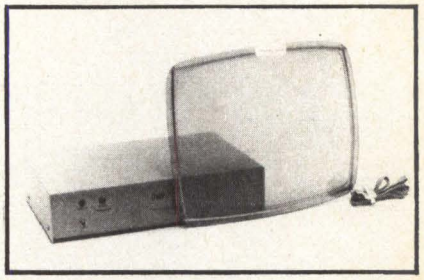
Software controllable switch

ASCI switch allows users software controllable switching between any 2 peripherals with only 1 computer port, or allows 2 computers to share the same peripheral by software switching of the shared peripheral. Duplicate computer serial ports or peripheral devices are not needed. I/O ports of the switch are controlled by sending 1 of 128 user selectable ASCII codes. Control code and baud rate are user selectable. Switch can be controlled by data terminal or data communications equipment without a null modem. Two models are available: model A10 switches 10 lines, and model A25 switches 24 lines of the RS-232 serial interface. The CMOS device is powered by battery or ac adapter. **Advanced Systems Concepts, Inc**, PO Box Q, Altadena, CA 91001.
Circle 388

Print buffer

Model 200 print buffer allows simultaneous use of printer and computer. Information to be printed is transferred at high speed from computer to print buffer, which then transfers data at a slower rate to the printer. Buffer maintains complete printer control, freeing the computer to perform other tasks. Storage capacity is 80k char max. Computer can be used immediately after the buffer is loaded. System can continue to load information into the buffer without interruption for control to be returned to the terminal after printing is completed. Either parallel or serial RS-232-C interface can be used for connection. Two or more buffers can be connected for increased storage capacity. **Modular Microsystems, Inc**, 28-17 201 St, Bayside, NY 11360.
Circle 389

Touch screen



High resolution touch screen TF-15 enables data access on touch display. The touch screen digitizer consists of a thin, transparent, curved panel that mounts in front of a std 15″ (38-cm) CRT display monitor and an electronic board connected to the panel. Touched location of the screen is measured and sent to the host computer as an RS-232-C message. Digitizer acts as a data entry device and can replace keyboard or graphic tablet. Three configurations include a complete package for fitting an existing terminal with touch input, an unpackaged serial version, and a parallel data version. **TSD Display Products, Inc**, 35 Orville Dr, Bohemia, NY 11716.
Circle 390

Motherboard/card cages for STD BUS

A pair of 8- and 16-slot motherboards and compatible card cages allow STD BUS assembly without backplane wiring. Motherboards have etched circuits for active termination to reduce power requirements. Faraday ground shielding on all bus lines eliminates cross talk. Boards meet all STD BUS requirements. Boards are available completely assembled, as kits for user assembly, and as bare boards only. Complimenting card cage CCK13S measures 19″ x 9″ x 5.25″ (48 x 23 x 13.34 cm) and mounts in any std rack. Model CCK135AS measures 10.25″ x 9″ x 5.25″ (26.04 x 23 x 13.34 cm). **Vector Electronic Corp, Inc**, 12460 Gladstone Ave, Sylmar, CA 91342.
Circle 391

Film foil capacitors

Series of general purpose wound film foil capacitors use polystyrene, polypropylene, and polyester films as dielectrics. Polystyrene capacitors are rated at 33 to 630 Vdc with a capacitance range of 20 to 100,000 pF. Manufactured entirely by automatic machines, the capacitors are among the least expensive high Q, tight tolerance capacitors available with defined tempcos. Polypropylene

(continued on page 280)

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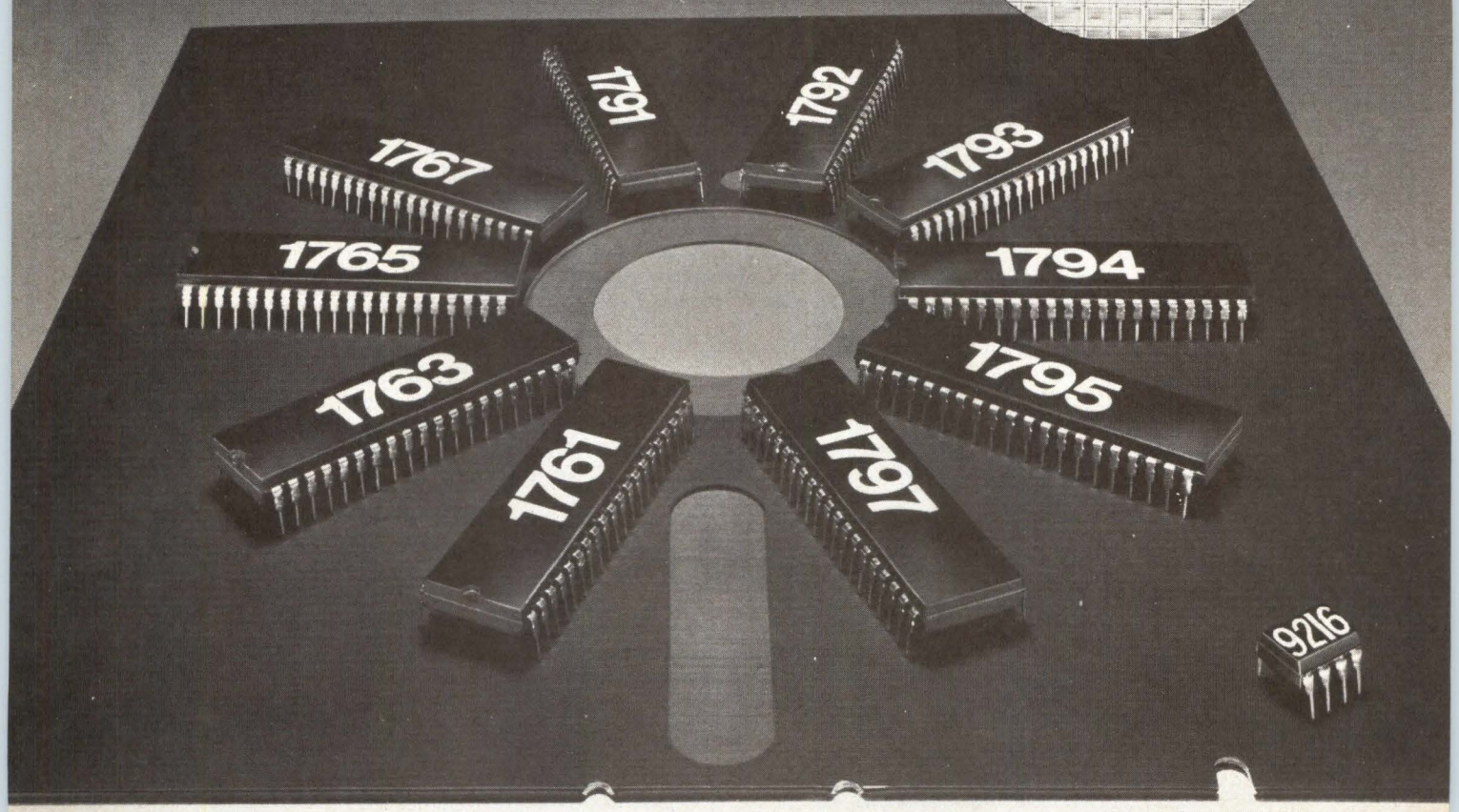

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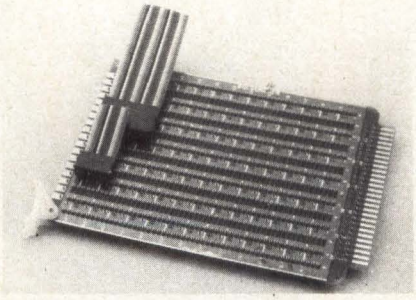
CIRCLE 166

capacitors are rated at 160 to 630 Vdc, with a capacitance range of 220 to 27,000 pF, and feature a working temp limit of 85 °C. With a dissipation factor of less than 0.05%, they are recommended for high power circuits. Polyester capacitors are rated at 160 to 630 Vdc with a capacitance range of 0.001 to 0.1 μF. They have the highest Q available in polyester film capacitors. **TRW Universal Capacitors**, 312 West O Street, Ogallala, NE 69153.
Circle 392

Socket boards with STD BUS compatibility



Series of "Quick/Connect" insulation displacement socket boards is compatible with STD BUS boards and features 28/56 card-edge fingers for I/O; accommodation of forty-two 16-pin or twenty-seven 24-pin ICs; 91 V_{CC} and 98 ground terminals; and 18 test points on top of board. Universal socket pattern accepts 0.3" (0.8-cm) and 0.6" (1.5-cm) DIPs. Std contact plating in 30 μin of gold, with tin/gold option available. Prices are $64 each in quantities of 10 with tin/gold option. **Robinson Nugent, Inc**, PO Box 470, 800 E Eighth St, New Albany, ID 47150. Circle 393

Card frame/power supply for multiple modems

Z-Frame card frame and power supply houses up to 16 variable speed Z9600C asynchronous modems designed for short operations of up to 10 mi (16 km) at speeds up to 9600 bps. Edge connectors provide all power and signals to modems, which can be inserted or removed without affecting each other. Each card slot operates independently and is connected to external devices via RS-232 and line connectors attached to the motherboard. Unit measures 19" x 5.25" (48 x 13.33 cm). Power is 110 V/60 Hz with optional 220 V/50 Hz. **Madzar Corp**, 37490 Glenmoor Dr, Fremont, CA 94536. Circle 394

Multilayer extender cards

Controlled impedance extender cards DE2ET-ML, DE4ET-ML, and DE6ET-ML incorporate buried power layers and ground planes, and control line widths and spacing between layers. Impedance achieved is approximately that of the bus structure. Improved signal transmission through the card and low power and ground voltage drops across the planes result. The multilayer cards are shorter than the company's universal series to permit use of std I/O extenders and flat cable jumpers to adjacent cards. **Hybricon Corp**, 410 Great Rd, Littleton, MA 01460.
Circle 395

Coreless motors

Coreless subfractional dc motors have rotor formed by self-supporting bonded wire coil rather than core laminated rotors. Coil wire design provides small rotor mass for low rotor inertia, fast response time, smooth operation at low speeds, limited cogging, and low electrical/mechanical noise performance. Models available include 6-Vdc 0.87" (22-mm) diameter motor, and two 12-Vdc 1.18" (30-mm) diameter motors. Rated torque range is 0.28 oz-in (20 g-cm) to 1.97 oz-in (50 g-cm). Rated speed range is 3500 to 6200 rpm. **Canon U.S.A., Inc, Electronic Components Div**, One Canon Square, Lake Success, NY 11042.
Circle 396

Low resistance metal film resistors

Resistance of 0.27Ω is available from A21 series of metal film resistors. Series features a flame retardant epoxy coating and is designed to minimize space requirements while maintaining MIL-R-22684 environmental specs. Series includes 0.5- and 2-W sizes, both with minimum resistance of 0.27Ω with a max of 10Ω and 27Ω, respectively. Tolerances range from 1% to 10%, depending on model. Resistors are designed to operate with full rated power at 70 °C. **Dale Electronics, Inc**, PO Box 609, Columbus, NE 68601.
Circle 397

Replacements for RN style resistors

Designed as single-sized precision resistors for high density, low profile electronic assemblies, radial lead type MK precision film resistors can directly replace 5 sizes of RN style. Std resistance values range from 30 Ω to 100 MΩ in a fully encapsulated package measuring 0.3 in^2 x 0.1" (1.9 cm^2 x 0.25 cm) thick. Model MK 132 and MK 632 feature ±1% resistance tolerances std; tolerances of ±0.1% are available. Full power rating is 0.75 W over temp range of −55 to 125 °C; max operating temp is 175 °C. Tempco is 50 ppm/°C for values up to 10 MΩ, and 80 ppm/°C for values to 100 MΩ. Resistors require less board space than 0.05-W RN 50 style resistors, allowing max packaging densities. **Caddock Electronics, Inc**, 1717 Chicago Ave, Riverside, CA 92507.
Circle 398

Long life momentary switch

K101 momentary pushbutton switch is designed with an electrical life of 25M cycles. Device is a spst, normally open switch with overtravel, and can be either panel or PC mounted. Electrical specs include contact rating of 0.4 VA max at 24 Vac or Vdc max, contact resistance of 20 mΩ max initially, insulation resistance of 1000 MΩ min, with a capacitance of 1 pf max, dielectric strength of 10k Vac rms at sea level and op temp of −25 to 85 °C. Applications include keyboard and trigger switch, multiple keyboard installations, and data input. **C&K Components, Inc**, 15 Riverdale Ave, Newton, MA 02158.
Circle 399

Solid state synchro transformers

Series of solid state synchro control transformer modules are direct replacement for conventional electromechanical control transformers, and provide digital control of existing analog servo systems. Modules are 2.6" x 3.1" x 0.82" (6.6 x 7.9 x 2.08 cm) and have std accuracies of ±6, ±15, or ±30 min of arc. They simultaneously accept synchro or resolver inputs of 11.8 or 90 V, 400 Hz; or 90 V, 60 Hz; and 14-, 12-, or 10-bit binary digital data. Model SCT 40 requires 26- or 115-V, 400-Hz ac reference input and 15 Vdc at 60 mA, −15 Vdc at 25 mA, and 5 V at 75 mA. Op temp ranges are 0 to 70 °C or −55 to 85 °C. **Computer Conversions Corp**, 6 Dunton Court, East Northport, NY 11731. Circle 400

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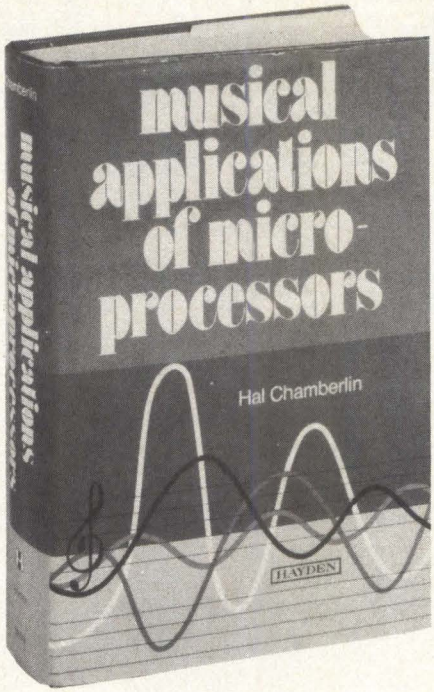

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Microcomputer Applications, 166 pages, 6 x 9, 1981, $11.95
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Operating Systems: Concepts and Principles by *John Zarrella.*

Used by Intel, Zilog, and Harris for software training. The most important component of system software is the operating system. This book provides an introduction to current operating systems technology. Operating systems concepts, capabilities, and terminology are explained.

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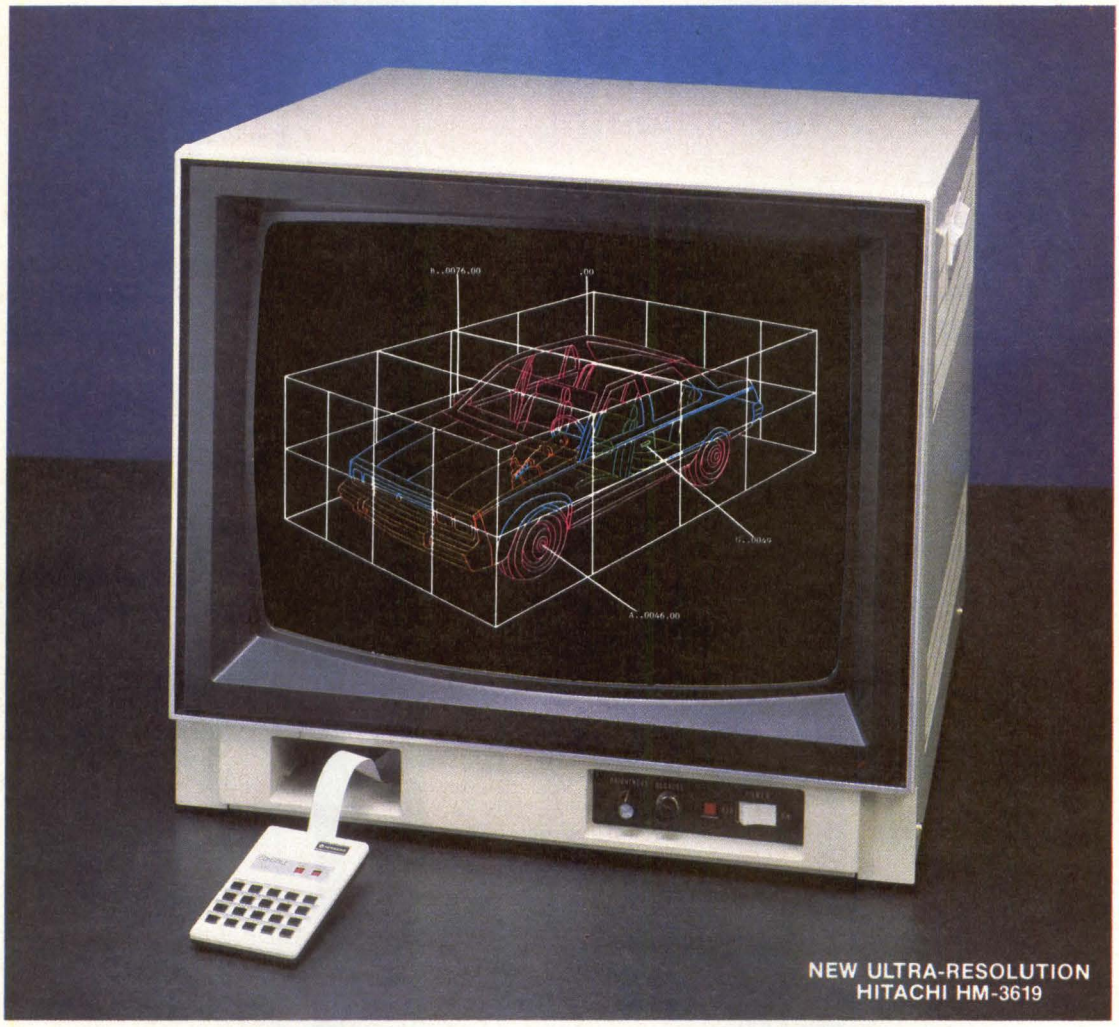
Circle 460

innovation*



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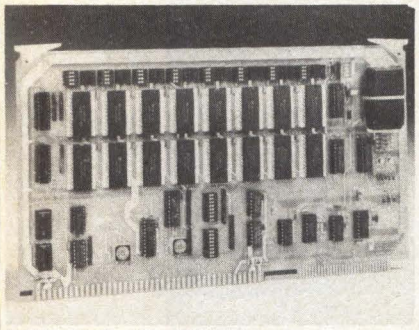

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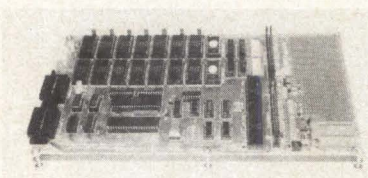

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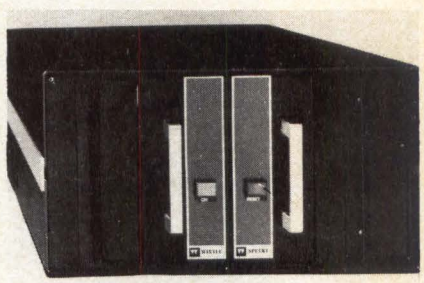

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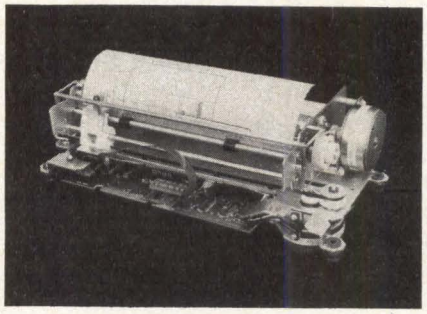

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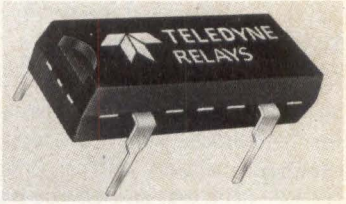

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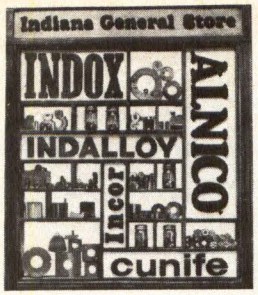

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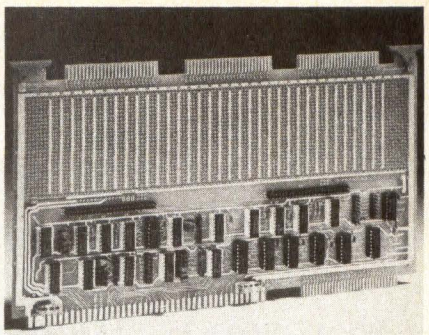

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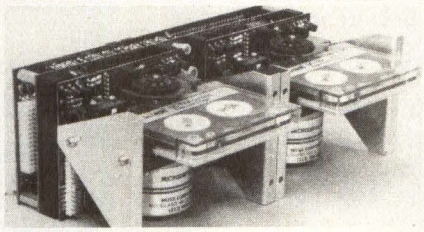

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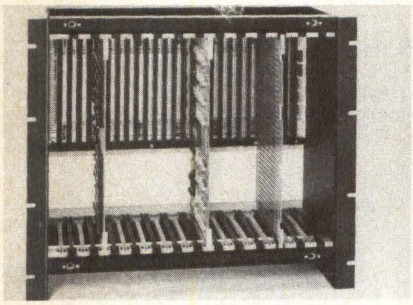

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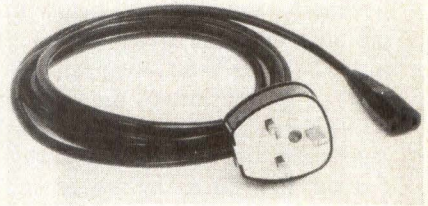

INTERNATIONAL CORDS AND CORDSETS

Standard cords for use in European countries, Australia, U.S. and Canada are available from stock or with shorter delivery times than custom cords. Cords have approvals at VDE, SEV, SEMKO, and other national test agencies as well as CSA certification and UL listings. Power supply cords can be installed permanently; cordsets with CEE-22 connector are detachable. Bulk cordage is available in sizes 3 x 0.75 mm², 3 x 1.0 mm², and 3 x 1.5 mm². **PANEL COMPONENTS CORP.**, P.O. Box 6626, Santa Rosa, CA 95406. Tel: (707) 523-0600. **CIRCLE 488**

CAREER OPPORTUNITIES

WHAT DOES IT TAKE TO MOVE AN ENGINEER TO CLEVELAND?*

Relocation, the very thought of uprooting one's family to move on and pursue greater opportunities, can create anxiety with employee and employer alike. Very often, the sole determining factor in whether or not an offer is accepted depends on the applicant's feelings toward the area in which his family will now establish new roots.

Resulting from the recent increase in demand for design talent, most financial packages tend to be very similar in terms of salary and benefits. Subsequently, it is this important aspect of geographical preference on which a significant share of the growth of the high technology industry may very well depend.

Computer Design, recognizing this fact, recently surveyed its readers in hopes of presenting the industry with a capsulized look at what areas of the country are most and least desirable for relocation by design engineers.

Surprisingly, the Mountain States, presently the least industrialized area of the United States, held the greatest appeal for engineers in all disciplines. Software engineers awarded this area a higher mark than any given area throughout the survey. Hardware designers were the least enthusiastic.

The West Coast scored the second highest marks with most of the enthusiasm coming from both software and data communications designers. The West Coast was closely followed by the Southwestern area of the country, in which CAD/CAM designers exhibited a particularly high preference.

The Southeast, following the trend towards the warmer climates, came in next with the highest scores from both the CAD/CAM and software professionals.

Finally, grouped well below in preference by all disciplines, were the areas of New England, Mid-Atlantic, and the Mid-West, respectively. Software and CAD/CAM designers showed the greatest interest in these areas while hardware engineers scored the Mid-Atlantic as the least desirable area in the survey.

One final note, the opportunity to relocate overseas scored higher marks than relocating to either the Mid-Atlantic or the Mid-West by all disciplines.

As W.C. Fields said, "All things considered, I'd rather be in Philadelphia." Or was that Paris?

***BEST ANSWER PRIZE:** A Cuyahoga River Fire Extinguisher

Who will be first to see through the walls of the future?

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We built the first working laser, and today our electro-optics, fiber optics, thermal imaging and infrared systems are like second sight.

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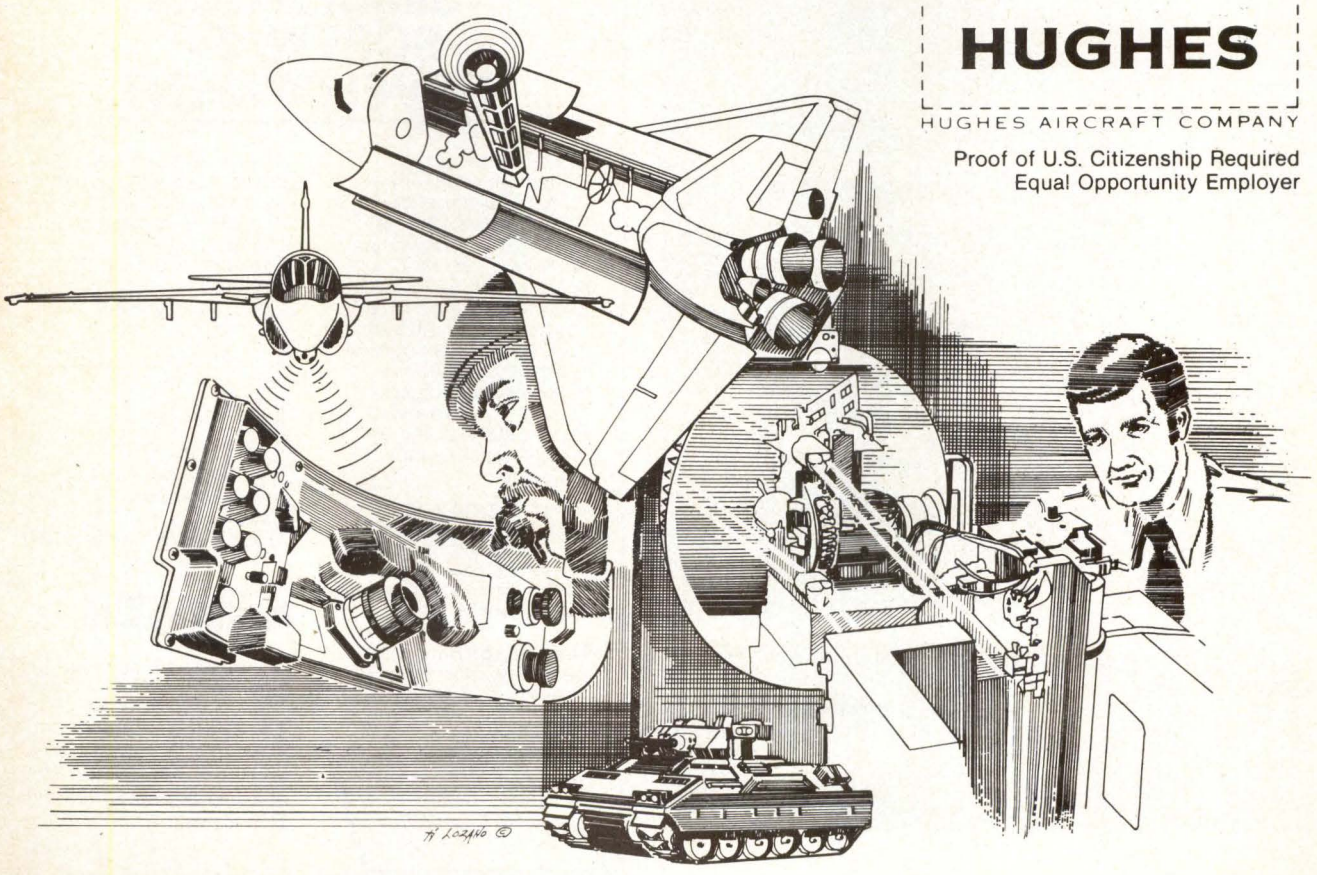

CIRCLE 170

WANTED

A Director for the Computer Center.

Yarmouk University needs a Director for the Computer and Information Center. Applicants should satisfy the following requriements:

1. To hold a Doctorate in Computer Science or Mathematics; otherwise, a Master's degree in Computer Science or Mathematics with practical experience in the field of Computers for a minimum period of 8 years.
2. Ability for planning, organizing, directing, and follow up of Computer Work, with a good knowledge of system analysis, programming and operation and ability to develop the systems and methods of work in Computers.
3. Fluency in English and preferably in Arabic.

Applications to be sent to Personnel Office, Yarmouk University Irbid, P.O. Box, 566, Jordan, not later than the end of April, 1982.

YARMOUK UNIVERSITY

CIRCLE 174

CIRCLE 172

Ever reflect on a career in the Nuclear Navy?

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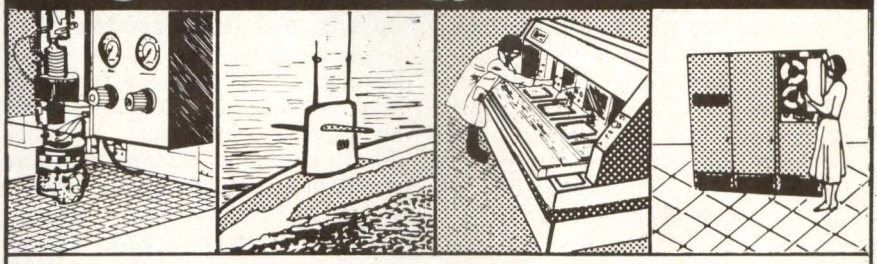

Kollmorgen Corporation is a diversified high technology innovator with proprietary positions in discreet segments of the communications, computer and computer peripherals, business equipment and industrial machinery/controls markets. It expects to double sales and earnings every 5 years and achieve a 20% return on shareholder's average investments---a pretty fast track indeed! To achieve its goals, Kollmorgen will have to continue to stay on top, technologically, by developing new products and processes and initiating breakthroughs in production and marketing know-how.

This is the primary task of PCK Technology, a dynamic division of Kollmorgen Corp., specializing in proprietary electronic interconnection technologies, systems and hardware. We are dedicated to innovation and being on the leading edge of state-of-the-art high technology. Our single most important objective is to find, motivate and hold the right kind of people—because only a select breed of professional has the talents and perseverance necessary to envision and attain new products and technological breakthroughs.

We are currently seeking motivated individuals in the following areas:

SENIOR ELECTRONIC ENGINEER

We have a technically challenging, high growth potential position for a Senior Electronic Engineer in our newly created Technical Products Division. This key specialist will be responsible for leading the development of the next generation of Multiwire machines and related electro mechanical products. Major challenges include working closely with our Advanced Development staff to bring new product concepts from the conceptual feasibility stage, thru design and development to release to manufacturing. In addition, this professional will function as our electronic and systems engineering expert for new ventures and products. Success and achievement will lead to a position of major importance in a new Kollmorgen business within the next several years. Successful candidates must have 5 years of electronic engineering experience in some combination of the following areas:

- **Hardware and software design experience in real time minicomputer and microprocessor applications;**
- **Experience with NC controlled products;**
- **Digital hardware and software design. PDP, Motorola 6800 experience a plus.**

SYSTEMS ENGINEERS

The demand for Multiwire CAD Technology, vital to the rapidly expanding Multiwire circuit board market, has created the need for an advanced systems development team. We have immediate openings for junior and senior systems engineers, who enjoy the challenge of functioning at the leading edge of systems technology. Each engineer is assigned major project responsibilities for computer aided designs, design automation and software applications packages. These positions offer unusually creative freedom to apply your Systems RXS11, Fortran and PDP 11 skills in a highly sophisticated technological environment. Position qualifications range from 1-3 years of experience in some combination of the following areas:

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- **Fortran programming with PDP 11 computers;**
- **Experience in applications systems, especially CAD systems;**
- **Background in RT11 assembler M6800 applications.**

By joining PCK Technology you will become a member of the Kollmorgen team, and as such, you will experience a unique environment that provides a high degree of professional freedom, entrepreneurial incentives, and the opportunity to reach the next rung on your career ladder.

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Capacitors and MIL-STD ceramic disk
Catalog details high and low voltage ceramic, chip, and mica capacitors with photos, diagrams, and size/capacitance/voltage tables and performance curves; data sheet provides specs for MIL-STD thermal ceramic disk capacitors. **KD Components, Inc,** Santa Ana, Calif.
Circle 410

Fiber optics
Fiber optic system design guide provides design-it-yourself format for communications links with charts, graphs, tables, and operational parameters. **Belden Corp,** Geneva, Ill.
Circle 411

Absolute/incremental encoders
Optical encoder catalog describes high resolution encoders, including Digisec[R] RA series absolute and RI series incremental rotary optical shaft angle encoders, and MicroSeries[R] rotary absolute optical shaft angle encoders. **Itek Corp, Measurement Systems Div,** Newton, Mass.
Circle 412

Digital transmitter/receiver
Data sheet describes OIS 4000 series of fiber optic transmitters and receivers with specs and configuration dimensions. **Optical Information Systems,** Elmsford, NY.
Circle 413

Integral modems
User's manual for integral modems doubles as introductory text on data communications equipment, with design and applications for R24 1200/2400-bps modem subassemblies. **Rockwell International, Electronic Devices Div,** Anaheim, Calif.
Circle 414

Rackmount power supplies/systems
Bulletin describes line of rackmount power supplies and multiple output/redundant output power systems, with prices noted. **Acopian Corp,** Easton, Pa. Circle 415

MIL-STD microcircuits
Capabilities/facilities brochure emphasizes custom Hi-Rel hybrid microcircuits for MIL-STD applications, custom CMOS design, std electronic modules for high density configurations, and miniaturized subsystems. **Circuit Technology Inc,** Farmingdale, NY.
Circle 416

Op amps and data converters
Applications/selection guide contains full specs for modular and microcircuit signal conditioning products—wideband and power operational amplifiers; logarithmic, instrumentation, and sample/hold amplifiers; ADCs and DACs; voltage to frequency and frequency to voltage converters, and regulated modulated power supplies. **Teledyne Philbrick,** Dedham, Mass.
Circle 417

High reliability switchers
Flyer announces 33 models of high reliability switchers, including single- and triple-output units from 15 to 2.24 kW, and includes product evaluation coupon for 30-day free trial period. **Calex Manufacturing Co Inc,** Pleasant Hill, Calif. Circle 418

Systems components
Catalog contains photographs, descriptions, and prices of systems expansion and maintenance products, cables, components, and power distribution systems. **Digital Equipment Corp,** Maynard, Mass.
Circle 419

AC line regulators
Brochure contains specs and features of low cost, synchronous solid state power line regulators, with discussion of voltage fluctuations and solutions. **Deltron Inc,** North Wales, Pa.
Circle 420

Power conditioning
AC power line problems and estimated cost of corrective measures for line glitch, brownout, and blackout are outlined for 17 systems in brochure. **Gould Inc, Electronic Power Conversion Div,** San Diego, Calif.
Circle 421

Power supplies
Brochure provides overview and specs for SCR and EM family of single- and 3-phase power supplies. **Electronic Measurements Inc,** Neptune, NJ.
Circle 422

1G-bps test equipment
Brochure describes line of test equipment suitable for applications to 1G bps, and includes specs for data generator, bit error rate transmitter/receiver, and clock source. **Tau-Tron, Inc,** Chelmsford, Mass.
Circle 423

Elastometric connectors
Elastometric connector design guide illustrates mounting of LCDs to PCBs using solderless, conductive silicone ZEBRA connectors. **TECKNIT,** Cranford, NJ.
Circle 424

Factory automation
Electronically reprogrammable modular automation control (ERMAC[TM]) system, a microcomputer based system for factory control and production analysis, is described in brochure. **Everett/Charles Automation Modules, Inc,** Rancho Cucamonga, Calif.
Circle 425

Book/software reference guide
Reference guide to all current editions of books and software published by the company includes technical level ratings, outlines of table of contents, illustrations, and prices. **SYBEX, Inc,** Berkeley, Calif.
Circle 426

Computer graphics
Overview guide to computer graphics software, systems, and services contains source material, descriptions, names and addresses of U.S. and international suppliers. Send letterhead requests with SASE (prestamped $0.37 in U.S.) to **Harvard Newsletter on Computer Graphics,** PO Box 89, Sudbury, MA 01776.
Circle 427

Fixed/removable 5.25″ Winchester drive
Brochure describes Micro-Magnum 5/5 drive, with discussion of "CushionAire" read/write heads, reliability, transportability and changeability, and system integration. **DMA Systems,** Santa Barbara, Calif.
Circle 428

Communications/telecommunications equipment
Product catalog highlights data communications and telecommunications, and networking equipment, including analog and digital instruments. **Halcyon Communications, Inc,** San Jose, Calif.
Circle 429

Custom ICs
Brochure profiles with descriptions and photographs custom ICs and end user products, and charts the custom IC market and development sequence. **Silicon Systems Inc,** Tustin, Calif.
Circle 430

When You Need . . .

WINCHESTER DISK SYSTEMS

FOR THE Q-BUS

See us at DEXPO 82 Booth 1002
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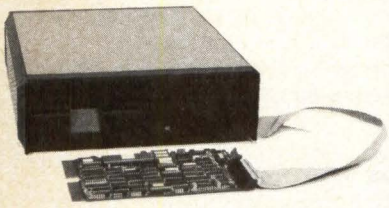
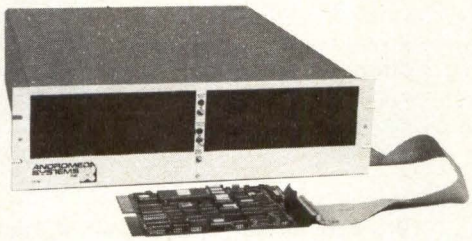
(Near U.S. Spring DECUS Symposium)

ADD-ON SUBSYSTEMS

MWDS



WDS

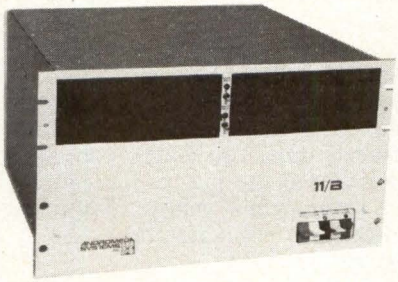


RPX60

5-1/4″ DISKS

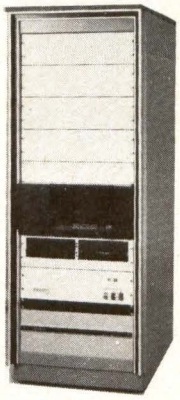
11/M-W

8″ DISKS



11/B-W

14″ DISKS



11/B-WTS

FULL TURNKEY COMPUTER SYSTEMS

. . . think of Andromeda

Andromeda Systems, Inc. offers the Q-Bus user a wide selection of Winchester disk based mass storage systems. Both add-on subsystems and full turnkey computer systems are available. Current storage capacities range from 2.5mb to 160mb. The Winchester disk controllers emulate DEC RK-05, RL-01/02, and RP-02/03 devices for compatibility with existing operating systems. Winchester disks in 5¼″, 8″ and 14″ formats are used to obtain the best possible performance in a variety of package sizes.

Back-up is to floppy disk or streaming magnetic tape. The 5¼″ and 8″ systems may be specified with an intregral floppy disk drive; these systems use the Andromeda WDC11 controller that includes an RX-02 emulating floppy disk controller on the same dual-width card. Also available for backup is a separate, high performance, non-emulating floppy disk controller, the DFDC11/DMDC11. This proprietary controller offers 25 to 61 percent more storage along with a data transfer rate 2.25 times faster than the RX-02.

We offer a complete line of Q-Bus based systems and other LSI-11 related products. For details, contact:

ANDROMEDA SYSTEMS INC.
9000 Eton Ave.
Canoga Park, Calif. 91304
Phone: 213/709-7600
TWX: (910) 494-1248

Digital panel meter
Brochure details electrical/mechanical specs of DM-31 single-board differential 3½ digit DPM, with block diagrams, mounting and connection methods, applications circuits, and ordering guide. **Datel Intersil,** Mansfield, Mass.
Circle 431

International data communications
International products catalog contains photos, illustrations, and descriptions of modems, multiplexers, and network diagnostic/control systems. **General DataComm**, Danbury, Conn.
Circle 432

Switching power supplies
Brochure highlights LY series of open frame switching power supplies, with spec listings of over 50 triple-, dual-, and single-output models. **Lambda Electronics, Div of Veeco Instruments Inc,** Melville, NY.
Circle 433

Power supplies
Bulletin introduces MK series switching power supplies with dimensional drawings, specs, and listing of 40 std models. **NJE Co,** Dayton, NJ.
Circle 434

DC power supplies
Technical catalog lists more than 250 dc power supplies in range of 10 to 1000 W, 3 to 320 Vdc, 35 mA to 200 A; specs, dimensional drawings, electronic/electrical parameters, and prices are outlined. **Standard Power Inc,** Santa Ana, Calif.
Circle 435

Automatic test equipment
Applications guide provides building block solutions to automatic test equipment development problems, with typ test/measurement applications shown for CDS 53A smart hardware system. **Computer Data Systems,** Englewood, Colo.
Circle 436

Thermal printer/plotter and R/O printer
Data sheets describe Miniterm model 2100 receive only thermal printer and Q160 thermal printer/plotter with specs and operational characteristics. **Computer Devices Inc,** Burlington, Mass.
Circle 437

Circuit board indicator
Updated circuit board indicator catalog provides specs for over 60 types of indicators, with schematics and dimensional application configurations. **Dialight,** Brooklyn, NY.
Circle 438

Network switching
Product brochure features NetSwitch network controller for switching from host to selected destination port, and direct system connect to multiplexing equipment. **Digital Communications Associates, Inc,** Norcross, Ga.
Circle 439

MULTIBUS card enclosures
Brochure details specs, features, and cost-effectiveness of ESF 80 custom MULTIBUS card enclosures. **Electro-Space Fabricators, Inc,** Topton, Pa.
Circle 440

Indicator lights
Product supplement form FSG182 covers Super-Brite and Extra-Super-Brite unmounted LEDs, LED lenses, panel and PCB mounted LED indicator assemblies, and neon glow lamps. **Industrial Devices, Inc,** Edgewater, NJ.
Circle 441

Semicustom ICs
Application note profiles digital semicustom IC designs, including LSI TTL gate arrays. **Interdesign, Inc,** Sunnyvale, Calif.
Circle 442

4-quadrant power supply
Bus controlled 200-W bipolar 4-quadrant power supplies with built-in IEEE 488 listener interface are described in catalog 146-1402. **Kepco, Inc,** Flushing, NY.
Circle 443

UPS
Brochure includes system description and specs for switching power supplies and uninterruptible power systems available in 150- and 300-W output capacities. **Lorain Products,** Lorain, Ohio.
Circle 444

Custom cable and assemblies
Brochure features custom engineered cables and assemblies for microminiature, military, video, medical, marine, and computing applications. **National Electric Cable, Div of National Electric Control Co,** Portland, Ore.
Circle 445

DC to DC converters
Catalog describes line of 5- and 10-W dc to dc converters; 60 models are profiled with electrical/mechanical specs, configurations, and prices. **Power General,** Canton, Mass.
Circle 446

Switching magnetics
Brochure highlights switching magnetics for switch mode power supplies with schematics, electrical specs, and transformer size selection guide. **Pulse Engineering Inc,** San Diego, Calif.
Circle 447

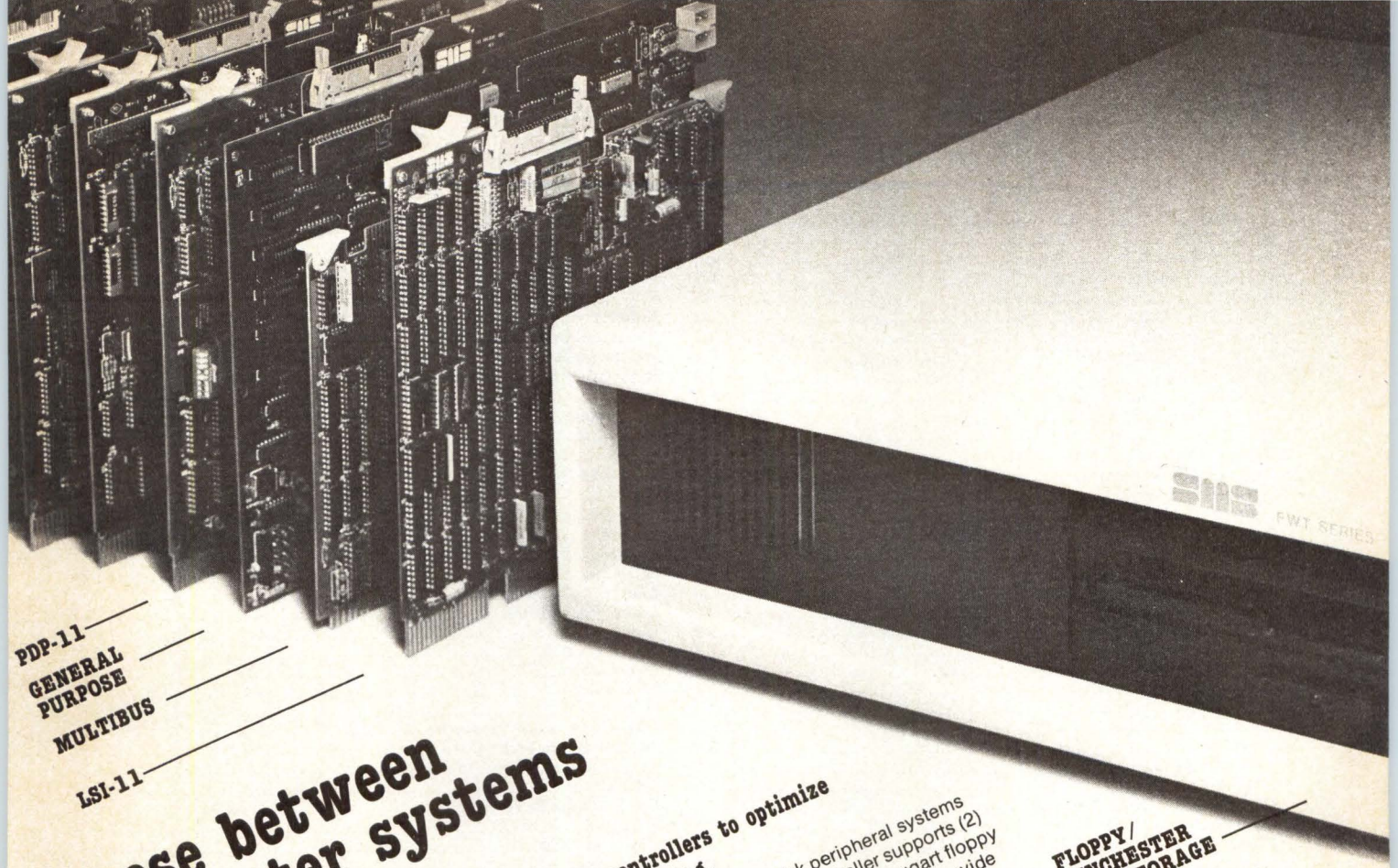
Process controller
Operation, specs, and English language programming structure for microcomputer based UDAC-II process controller are outlined in brochure. **Reliance Electric Co, Control Systems Div,** Worthington, Ohio.
Circle 448

Resistors
Cross reference guide to resistors from domestic/foreign manufacturers features over 100 wirewound, metal and carbon film, high voltage, and power oxide resistors, and resistor networks. **RCD Components Inc,** Manchester, NH.
Circle 449

Ceramic disk capacitors
Brochure describes temp compensating, general purpose, and barrier layer capacitors, with ranges, technical characteristics, performance graphs, and ordering information. **Thomson-CSF, Passive Components Div,** Canoga Park, Calif.
Circle 450

Switching multiplexer
Data sheet profiles the Switching Multiplexer, for distributed data switching networks, an enhanced member of the company's family of statistical multiplexers/data concentrators. **Timeplex, Inc,** Rochelle Park, NJ.
Circle 451

Synchro/resolver simulator
Data sheet highlights series 3800C-6 IEEE 488 compatible, programmable synchro/resolver simulator for bench or ATE applications, profiling local, remote, and optional dynamic modes, specs, and pin designations. **Transmagnetics, Inc,** Farmingdale, NY.
Circle 452



PDP-11
GENERAL PURPOSE
MULTIBUS
LSI-11

FLOPPY/ WINCHESTER DISK STORAGE SYSTEM . . . UP TO 40M BYTES OF STORAGE

Choose between Winchester systems or controllers

Complete systems to minimize system costs . . .

SMS FWT series disk peripherals provide up to 40M bytes of 8" Winchester disk storage and 1M bytes of floppy disk storage for DEC's* PDP-11, LSI-11, and VT103, INTEL Multibus** and other microcomputers! In only 5¼" of table top or rack space you also get the following benefits:

- Choose 8.9Mb, 17.8Mb, 26.7Mb or 35.6Mb of formatted Winchester disk storage.
- Up to 427K bytes/sec data transfer for Winchester and 63K bytes/sec for floppy.
- Supports IBM single and double density diskette formats plus DEC's RX01/RX02 formats or INTEL 202 format depending on host computer.
- Single board interfaces are compatible with PDP-11 Unibus, LSI-11 Q-Bus, INTEL Multibus or use your own adapter card for special microcomputer busses.
- Convenient Winchester backup requires only 40 seconds per 1.2M byte floppy diskette.
- Off-line and on-line system and drive tests verify correct disk and controller operation.
- Automatic error retry, ECC (Error Correction Code) and Winchester disk flaw management insure exceptional data integrity.

Or, just controllers to optimize system packaging.

All controllers used in SMS disk peripheral systems are available separately. Each controller supports (2) Shugart/Quantum Winchester and (2) Shugart floppy disk drives, utilizes patented PLL circuitry to provide maximum margins for worst case bit shifted data recovery, incorporates ECC (Error Correction Code) and includes on-board self test! Additional features are:

DEC PDP-11/LSI-11

- Single LSI-11 dual height or PDP-11 quad height interface plus formatter board.
- On board bootstrap.
- Standard RT-11, RSX-11M, UNIX,*** and SMS utility software support selective file backup and load operation.
- High performance data transfer of up to 543K bytes/sec.
- Emulates DEC RX02 floppy disk controller.
- Automatic recognition of RX01, RX02 and IBM diskette formats.

INTEL MULTIBUS

- Single Multibus compatible PC board requires only 5A (max.) @ 5 volts.
- Direct connection to (2) Shugart/Quantum and (2) Shugart floppy disk drives. Eliminates external data separator board.
- Interface and command compatible with INTEL iSBC 215A and iSBX 218 controller boards.
- Supports IBM and INTEL iSBC 202 diskette formats.

GENERAL PURPOSE

- Single board controller requires only 5A (max.) @ 5 volts.
- Interface, dimension and connector compatible with Shugart 1403D.
- Direct multi-sector disk transfer of up to 543K bytes/sec.
- Easy to use byte parallel general purpose interface.

SMS **Scientific Micro Systems**
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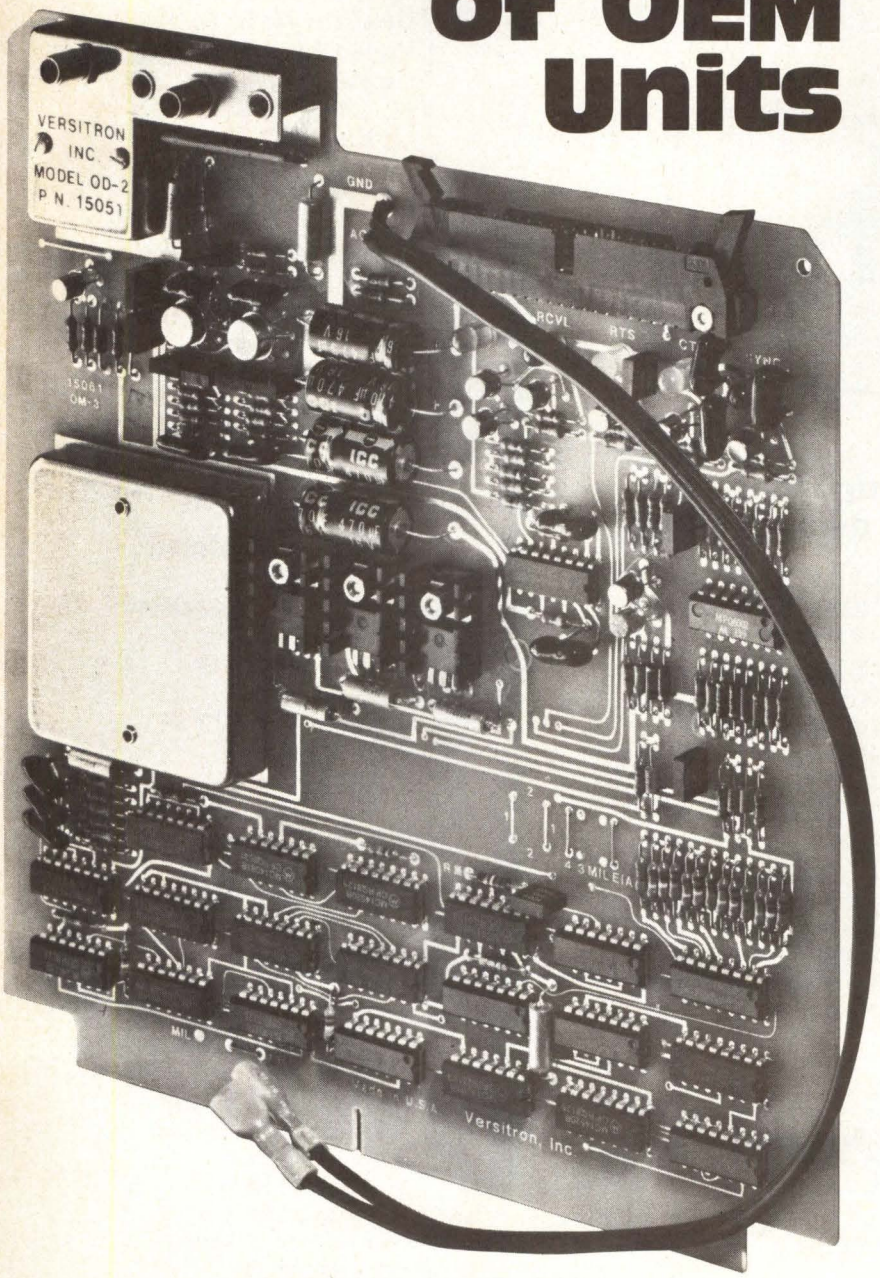
AD INDEX

Plug-in Fiber Optic Modem Expands Capabilities of OEM Units



Equipment manufacturers can now integrate a powerful, new Fiber Optic Modem directly into their equipment; resulting in a device that will provide exceptional data throughput performance in any local distribution environment.

The use of fiber optics for local data distribution assures that your end product will perform as it was designed; regardless of the environment in which it is used. Unlike conventional wire cables, optic cables are totally unaffected by rfi, adjacent noisy cables, or heavy duty electrical equipment. A big plus is that it is also effectively immune to wire tapping; yet costs about the same as coaxial cable.

In addition to the inherent advantages of fiber optics, Versitron's OM series of plug-in modems offers an impressive list of performance specifications. These include: operating range up to two kilometers (6500 feet), synchronous or asynchronous operation at data rates up to 38.4 KBPS, true EIA handshaking (three separate control signals in each direction are multiplexed along with the data), and an optional alarm circuit that will shut down all traffic if the cable is tampered with.

For details on how our optical modem can help you to significantly improve the marketability of your end product, give us a call at (202) 882-8464; or write Versitron, Inc., 6310 Chillum Place, N.W., Washington, D.C. 20011.

VERSITRON, INC.

CIRCLE 178

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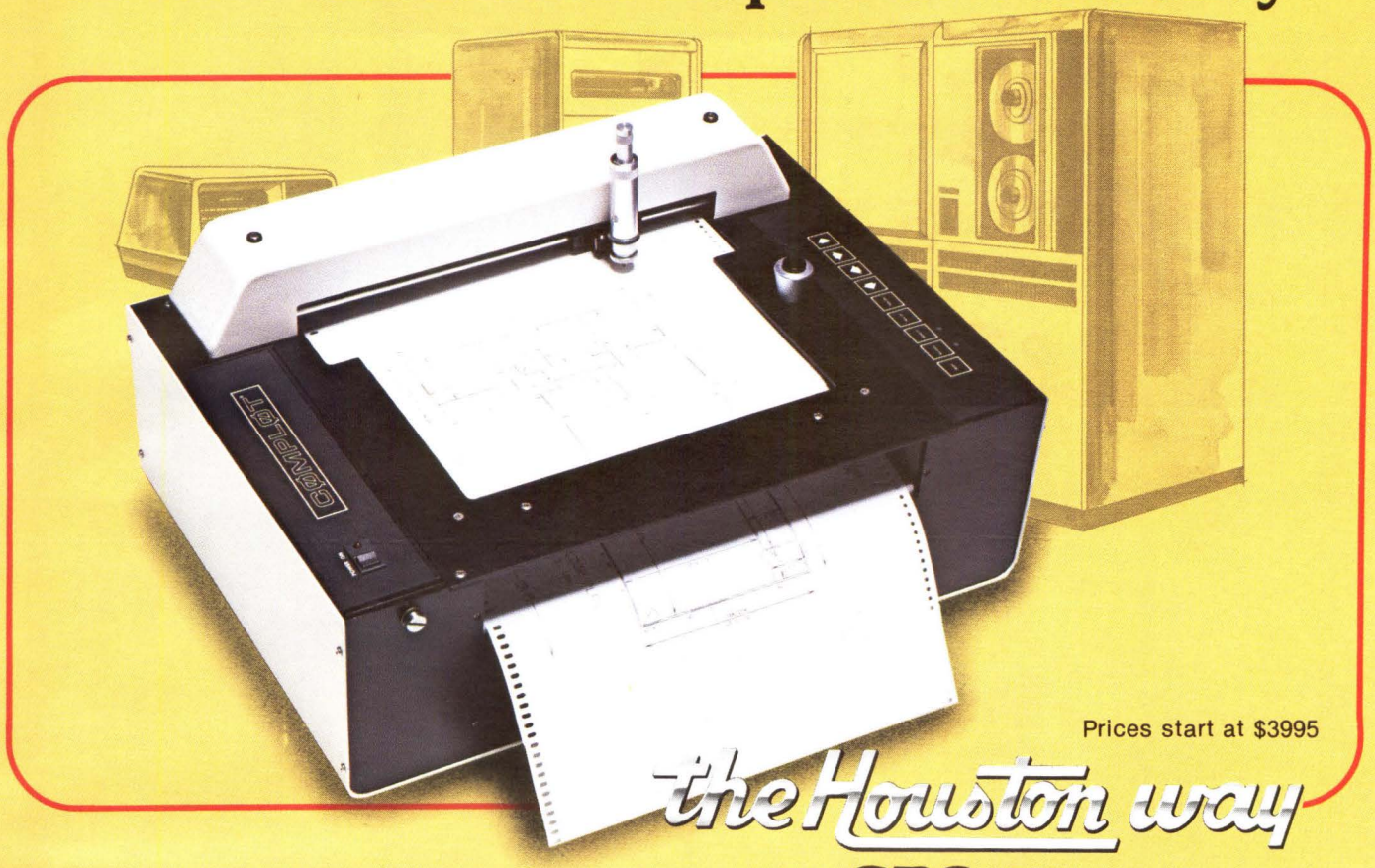

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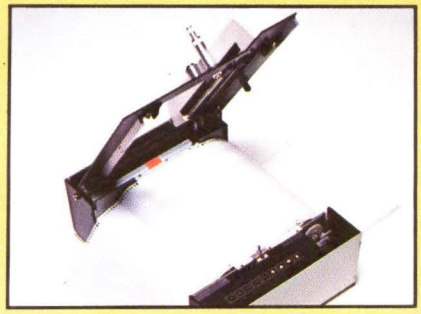

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