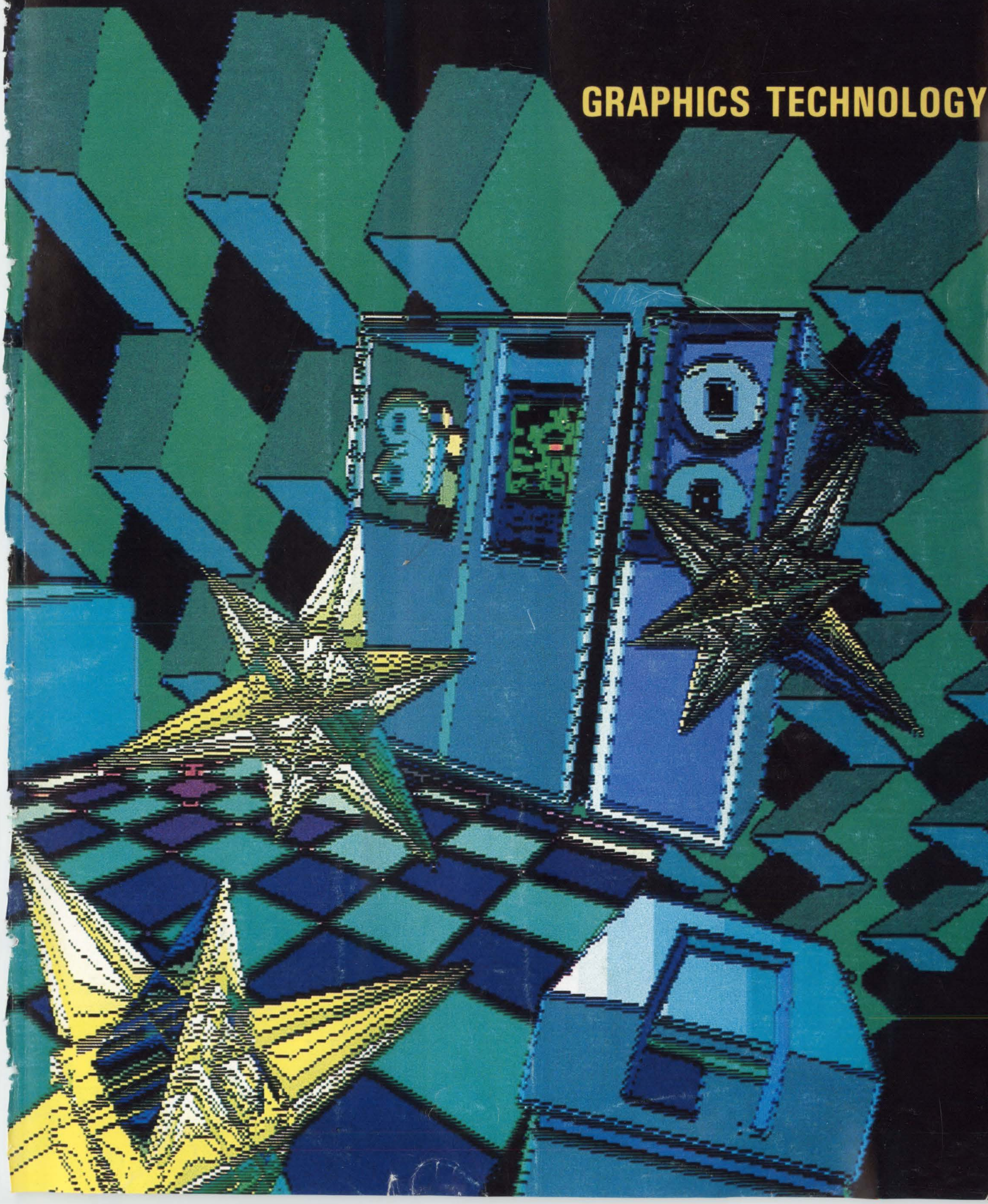
PennWell Publication

JULY 1983

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

GRAPHICS TECHNOLOGY



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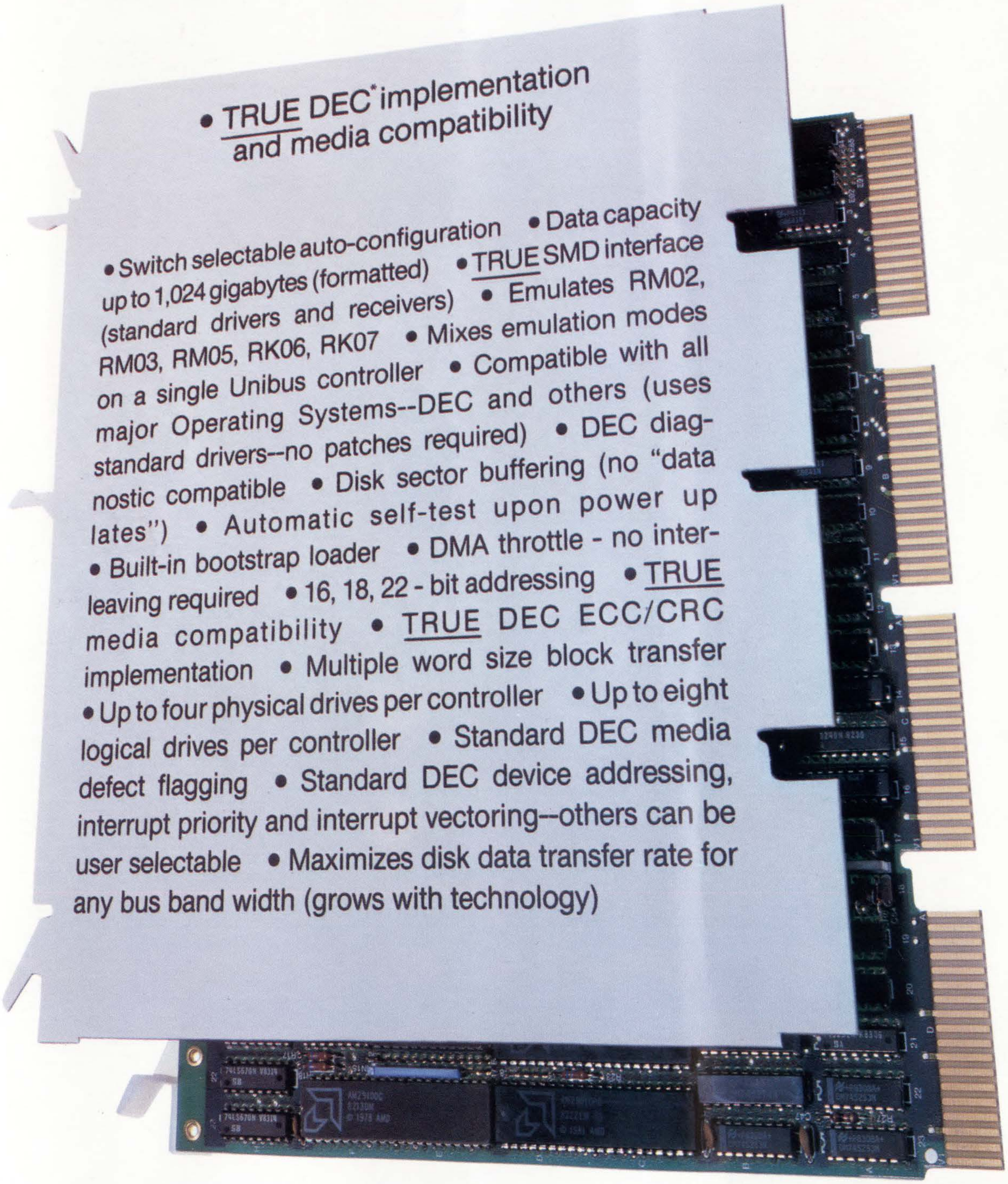

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CIRCLE 4

UP FRONT

Late announcements back up engineering workstation report (see pp 143-160)

"Diagram," a multifunction design engineering and layout system, provides IC design engineers with logic and schematic capture as well as design verification for gate arrays and standard cell layouts. Via Systems has integrated Diagram into its series 100 CAD/CAM systems to provide a "full range of concept-to-chip" support tools.

CAD/CAM system software for automatic component placement and circuit routing announced by Telesis Systems is claimed to significantly speed up the PCB design process. Three standard routing algorithms give the designer a high degree of control over the placement and routing process, including interrupt and restart in the same or another algorithm. Most routes can be completed automatically within only a few hours.

Engineers who have little previous IC design experience can translate schematics into custom VLSI circuits with an integrated CAE/CAD IC design package introduced by VLSI Technology. The package includes all tools needed to enter a system schematic, verify the design, build a physical layout, and verify functions.

Dual stations in a computer graphics system from Evans & Sutherland share a common control unit that includes a graphics control processor, mass memory, and a display processor. Greater interactive performance can be provided by using a second graphics control processor.

An addressable resolution of 1536 x 1024 pixels on its 19″ color monitor is said to provide Lundy Electronics & Systems' Computer Graphics Div's workstation with a very sharp display. The S5484 also offers high speed polygon fill, Tektronix 4014 emulation, and a Tektronix emulation "software switch."

First production quality Ada compiler meets DoD standards

Department of Defense validation of the Rolm Ada compiler, the first production quality compiler to be tested and validated by the DoD's Ada Joint Program Office, has been announced jointly by Rolm and Data General. Both companies will sell Ada software development systems based on Rolm Ada software and Data General Eclipse computers. AJPO validation ensures that the Ada compiler meets the ANSI/MIL-STD-1815A-1983 Ada language standard. (Copies of the Ada compiler validation test suite are available to compiler developers. *Letter requests* should be sent to Dr T. H. Probert, Institute for Defense Analyses, 1801 N Beauregard St, Alexandria, VA 22311. Include two 2400′ reels of magnetic tape.)

Scientist proposes national network of research computers

Linking the supercomputers at national laboratories and major universities could speed the development of advanced computer designs and software, according to John J. Roberts, an associate director of the Argonne National Laboratory. In testimony before a combined meeting of the House Committee on Science and Technology's subcommittees on energy development and applications, the scientist proposed that regional research centers would attract the best talent from their areas, and these collaborations would aid U.S. competition with other countries in developing supercomputer systems.

UP FRONT

Pretriggers

Zilog's entry into the 32-bit microprocessor arena, due to appear in mid-1984, will have full 32-bit internal architecture, including multiplexed data and address lines, for a physical address capability of 4G bytes. The Z80,000 will have an onchip MMU for virtual memory schemes and will provide an instruction set that is binary compatible with existing Z8000 software.

A single-board, multi-user, multiprocessor microcomputer system that combines a 16-bit CPU with four 8-bit processors will be shown by CompuPro at CP/M'83 East in Boston from Sept 29 to Oct 1. The system contains 384K bytes of RAM that emulate a disk drive, dual 5¼" floppy disk drives, seven serial ports, and a parallel printer port. Each 8-bit processor has its own 64K bytes of memory.

A personal communications terminal introduced by Rolm is considered to be a major technological step toward implementing a digital desk. The terminal consists of a 9" CRT, dashboard with function keys, digital telephone, and detachable alphanumeric keyboard. All personal data are stored in 8K bytes of nonvolatile RAM. Program RAM has a 5-min battery backup.

Both synchronous and asynchronous architecture are used in the Numerix MARS-432 array processor. The full floating point CPU is said to operate three times faster than other high performance array processors in the same price range. Add and multiply times are 100 ns; DMA transfers are at I/O bus rates of 20M bytes/s.

A development system for 16-bit microcomputers, the Intellec Series IV improves productivity of designing and developing systems by incorporating network-like functionality in standalone workstations. Intel's 430/431 combines hardware and software tools to improve designer productivity and shorten product time to market.

By separating resource allocation from task processing, a multi-user system from Computer Automation's Naked Mini Div permits applications running under standard operating systems to coexist with applications under a proprietary operating system. The Omnix 186 uses a minicomputer for peripheral management and I/O processing and microprocessors for program executions.

A speech recognition scheme that looks for specific sounds instead of entire words promises speaker independence and small memory requirements. The Universal Speech Access system from Voice Control Systems uses feature analysis to look for the spoken order of consonant sounds, rather than match the initial utterance with a vocabulary of reference words.

Acceptance of images encoded in the North American Presentation Level Protocol, developed by AT&T from the Canadian Telidon graphic standard, is among the capabilities of a graphics terminal introduced by Verticom. The terminal has three Multibus expansion slots.

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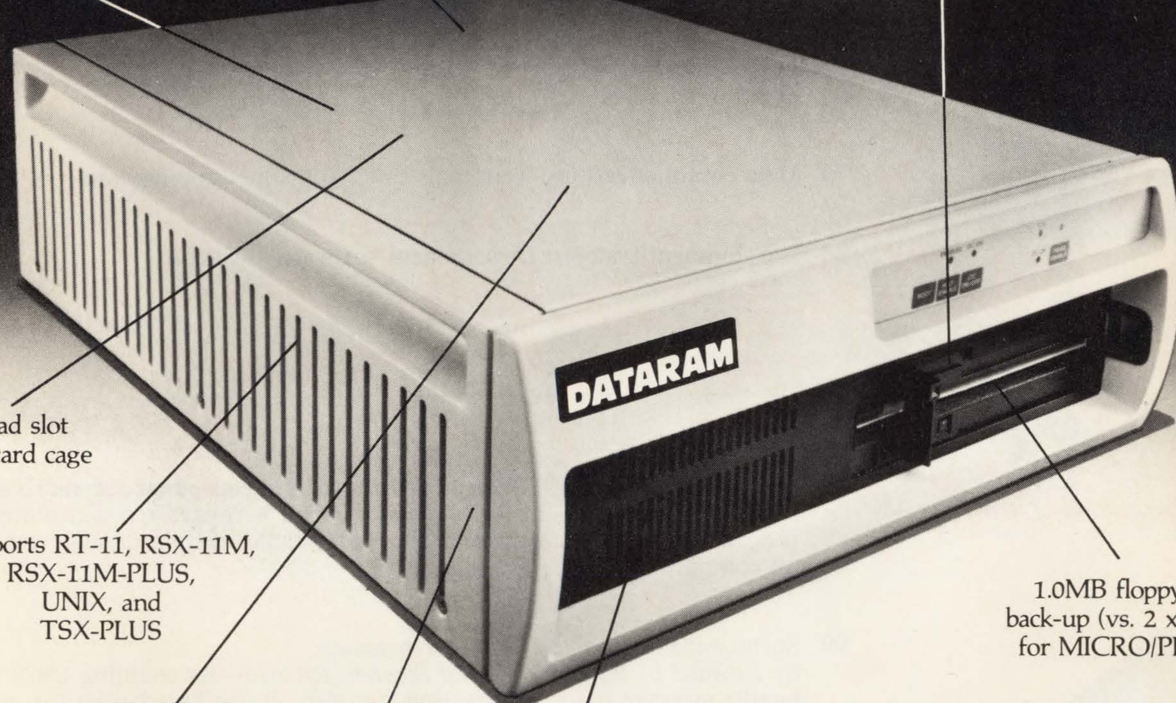

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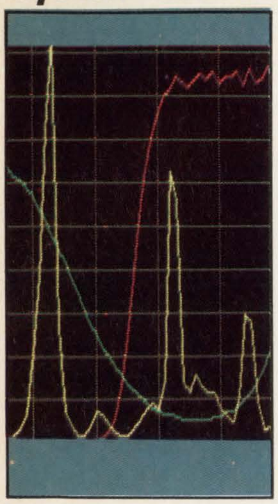

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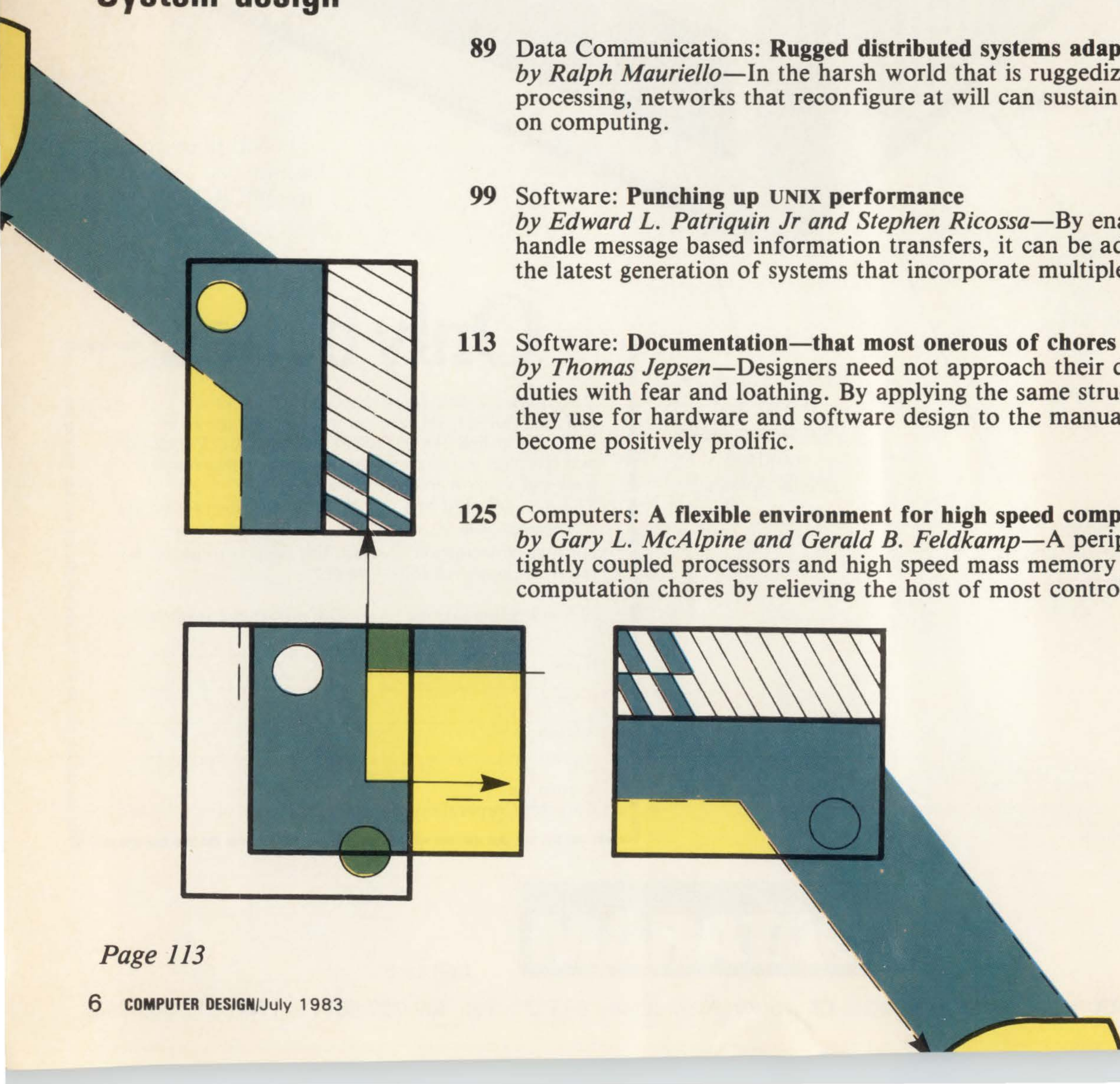
System design



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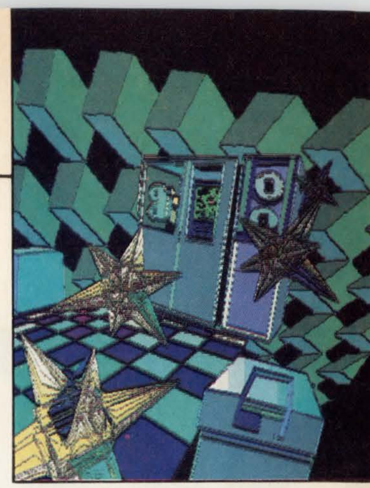
Vol 22, No 8
July 1983

Special report on graphics technology



This month's cover, entitled "Monday 9 am Computer Room," was created by Mark Lindquist and Alan Green on the Digital Effects Video Palette III and D-48 high resolution camera system.

System components

Departments

Designers' preference survey*

Editorial reviewers for parts of this issue:

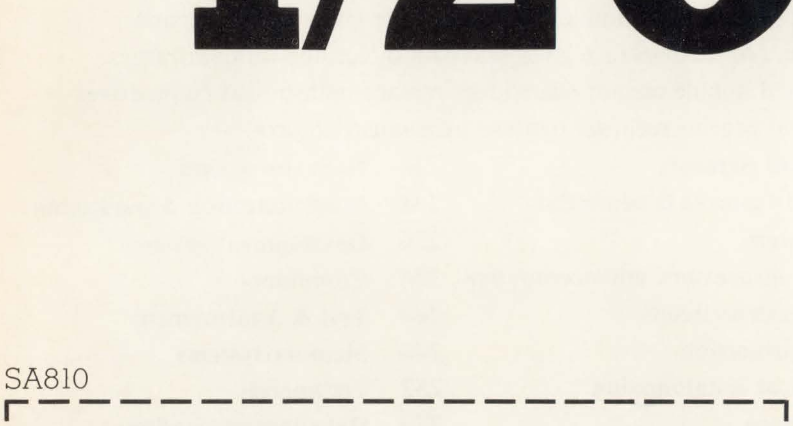
G. Perrone
John F. Wakerly

*Appearing in Domestic issues only

SHUGART DRIVES.

1/2 OFF.

SA810



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No, it's not a sale.

It's just a way of telling the world that Shugart now has a whole line of half-height floppy disk drives.

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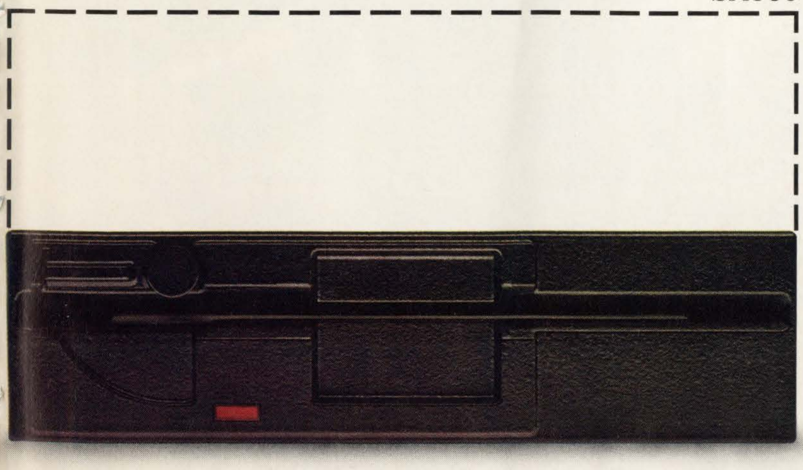
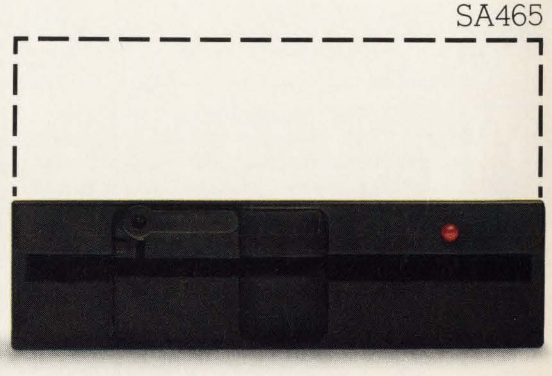


SA465



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PLANNING FOR GROWTH

***Computer Design*'s new Editor in Chief, Mike Elphick (left), confers with Managing Editor Syd Shapiro.**

Though readers are, of course, familiar with *Computer Design* as a magazine, they may not know that it is also the flagship of a fleet of publications that form the Advanced Technology Group of our parent PennWell Publishing Company. Now, I am proud to announce that I have been appointed Editorial Director of this division.

While I shall continue to be closely connected with *Computer Design*, its readers, and its editorial planning, I shall also be exploring ways to continually provide new services for computer based system designers and to expand the audience we serve. Toward this end, I will explore possible product-line extensions, such as extra single-subject issues and even start-up publications. Additionally, I will be addressing other high technology publishing arenas of interest that will help accelerate growth within the Advanced Technology Group. In this pursuit, I may call on some of you for your suggestions. In the meantime, I thank you for the kind words, the criticism, and the many editorial contributions that you have given us throughout my past few years as *Computer Design*'s Editor in Chief. Every input has been most valued and helped us to shape the evolution of the magazine.

Therefore, with your continued support very much a priority, it is with great pleasure that I reintroduce you to Michael S. Elphick, who becomes Editor in Chief of *Computer Design* with this issue. When Mike joined us as Executive Editor almost a year ago, he brought with him an extensive background in engineering and in high technology publications. His expertise has benefited our staff and magazine immensely, and I expect many more good things to come from Mike in his new position. In departing, I ask you to be as helpful to Mike with your feedback and contributions as you have been to me.

Like the economy and the computer business, publications also grow, and these advances are likely to accelerate. Growth usually heralds change—in products as well as in organizations. Since you are a prime moving force behind our progress at *Computer Design*, please continue to support us through your input. Help us ensure that through our organizational growth, we never lose sight of our primary end product—the highest quality publication possible.

Saul B. Dinman

Saul B. Dinman
Editorial Director
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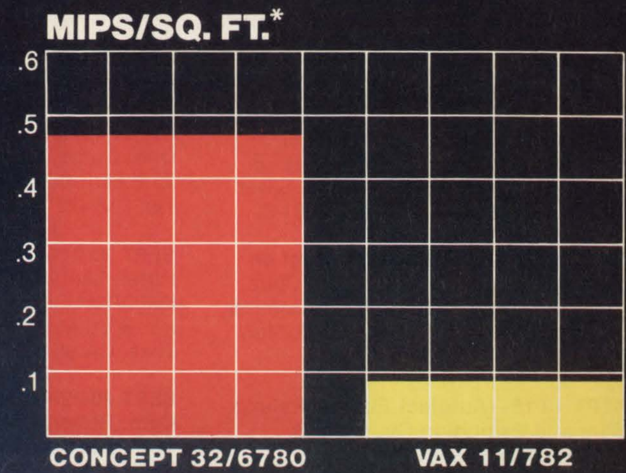

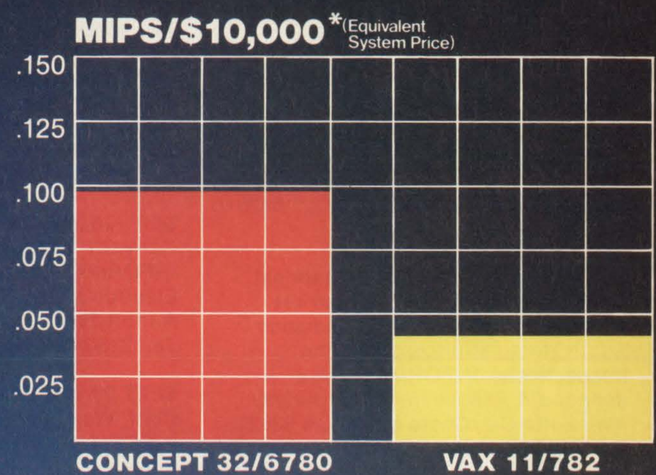

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CIRCLE 12

CONFERENCES

AUG 9-11—World Congress on the Human Aspects of Automation, Univ of Michigan, Ann Arbor, Mich. INFORMATION: Pat Van Doren, Technical Activities Dept, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1080 X369

AUG 23-26—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 12-14—IEEE Internat'l Conf on Computer Aided Design, Santa Clara, Calif. INFORMATION: John A. Domiter, American Bell Inc, PO Box 3505, New Brunswick, NJ 08903

SEPT 13-15—Autofact Europe, Palexpo Conf and Exhibition Ctr, Geneva, Switzerland. INFORMATION: Automated Systems Assoc, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

SEPT 13-15—Federal Computer Conf, Washington Conv Ctr, Washington, DC. INFORMATION: Federal Education Programs, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181; 800/225-5926 (outside Mass)

SEPT 13 AND SEPT 29—Invitational Computer Confs, Newton Marriott Hotel, Newton, Mass, and Radisson South Hotel, Minneapolis, Minn (respectively). INFORMATION: B. J. Johnson & Assocs, Inc, 3151 Airway Ave, Suite C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

SEPT 13-15—Midcon, O'Hare Expo Ctr and Hyatt Regency O'Hare, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Mini/Micro-Midwest, O'Hare Expo Ctr, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Peripherals, Moscone Ctr, San Francisco, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

SEPT 13-15—WPOE (Word Processing and Office Environment Show and Conf), San Jose Conv Ctr, San Jose, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 19-21—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Henry Morris, Control Engineering, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840

SEPT 19-23—IFIP (Internat'l Federation for Information Processing) World Computer Congress, Paris, France. INFORMATION: Philip H. Dorn, Dorn Computer Consultants, Inc, 25 E 86th St, New York, NY 10028. Tel: 212/427-7460

SEPT 20-21—Data Storage, Marriott Hotel, Santa Clara, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 20-22—Informatics Exhibition and Conf, Roberto Clemente Coliseum, San Juan, Puerto Rico. INFORMATION: Informatics '83, 3421 M St NW, Suite 219, Washington, DC 20007. Tel: 703/920-9595

SEPT 26-29—Compcon Fall, Marriott Gateway, Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 26-28—Maecon, Kansas City Conv Ctr, Kansas City, Mo. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 29-30—CAD/CAM and Simulation Conf, Westin Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888

OCT 2-5—Robotech (Internat'l Conf and Exposition for the Application of Automated Manufacturing Technology), Curtis Hixon Convention Hall, Tampa, Fla. INFORMATION: Tom Will, Latcom Inc, 4135 Laguna, Coral Gables, FL 33146. Tel: 305/667-5150

OCT 3-6—Data Communications Symposium, Sea Crest Lodge, Falmouth, Mass. INFORMATION: Kenneth J. Thurber, Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

OCT 8-10—PC (Internat'l Exposition and Conf Featuring IBM Personal Computers and Compatibles), Bayside Exposition Ctr, Boston, Mass. INFORMATION: Gerald A. Milden, Northeast Expositions, 826 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

OCT 10-13—ISA (Instrument Society of America) Internat'l Conf and Exhibit, Astrohall, Houston, Tex. INFORMATION: Philip Meade, ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

OCT 12-14—Fiber Optic Communications Local Area Network Applications, Atlantic City, NJ. INFORMATION: Tom Coggeshall, IGI, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

OCT 18-20—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Doris Thomas, PO Box 371, Cedar Knolls, NJ 07927. Tel: 201/267-7120

OCT 24-26—IEEE Internat'l Symposium on Electromagnetic Compatibility, Shoreham Dunfey Hotel, Washington, DC. INFORMATION: IEEE EMC '83, PO Box 2228, Rockville, MD 20852. Tel: 301/984-8400; 800/638-0111 (outside Md)

OCT 31-NOV 3—Internat'l Conf on Computer Design: VLSI in Computers, Rye Town Hilton, Port Chester, NY. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

WORKSHOPS

JULY-OCT—Control Technology, various cities and dates. INFORMATION: Bette McLaughlin, Public Relations, The Foxboro Co, Foxboro, MA 02035. Tel: 617/543-8750

AUG-SEPT—Feigenbaum on AI: Expert Systems and Knowledge Engineering, various cities and dates. Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD 21044. Tel: 301/596-0111

AUG 16-20—Nonvolatile Semiconductor Memory Workshop, Marriott's Mark Resort, Vail, Colo. INFORMATION: Gary Derbenwick, Inmos Corp, PO Box 16000, Colorado Springs, CO 80935. Tel: 303/630-4345

AUG 16-19 AND AUG 29-SEPT 2—Software-Oriented Computer Architecture, Boston, Mass, and Palo Alto, Calif (respectively). INFORMATION: Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD 21044. Tel: 301/596-0111

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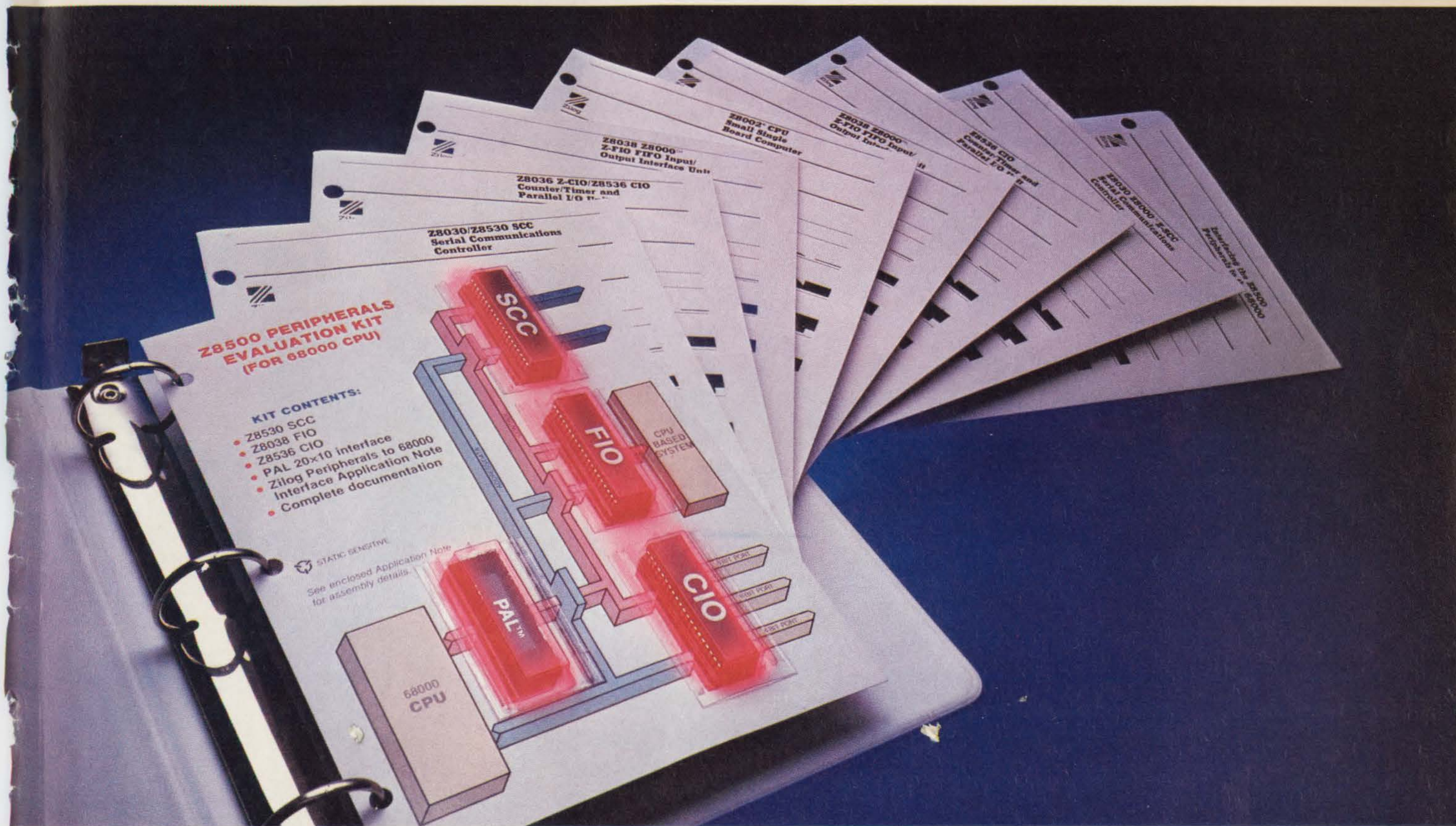

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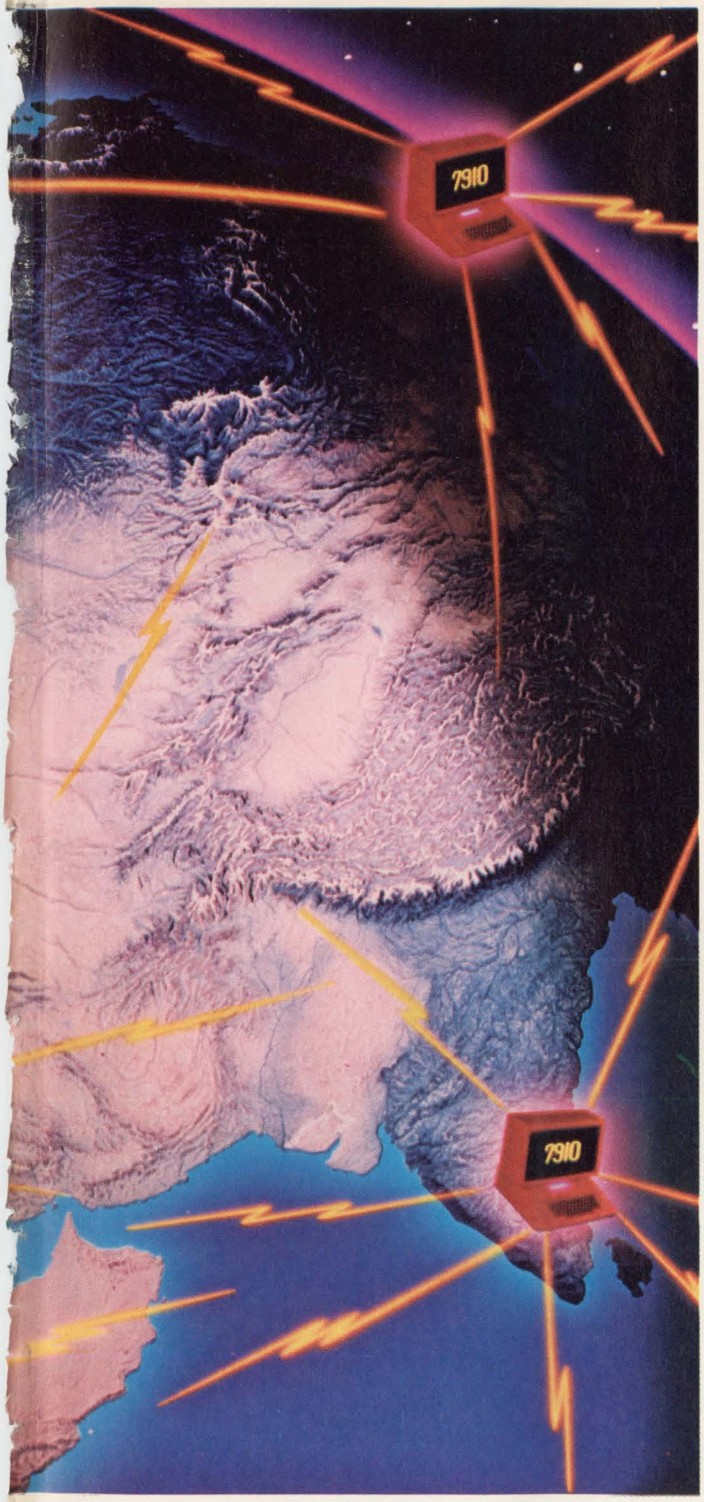

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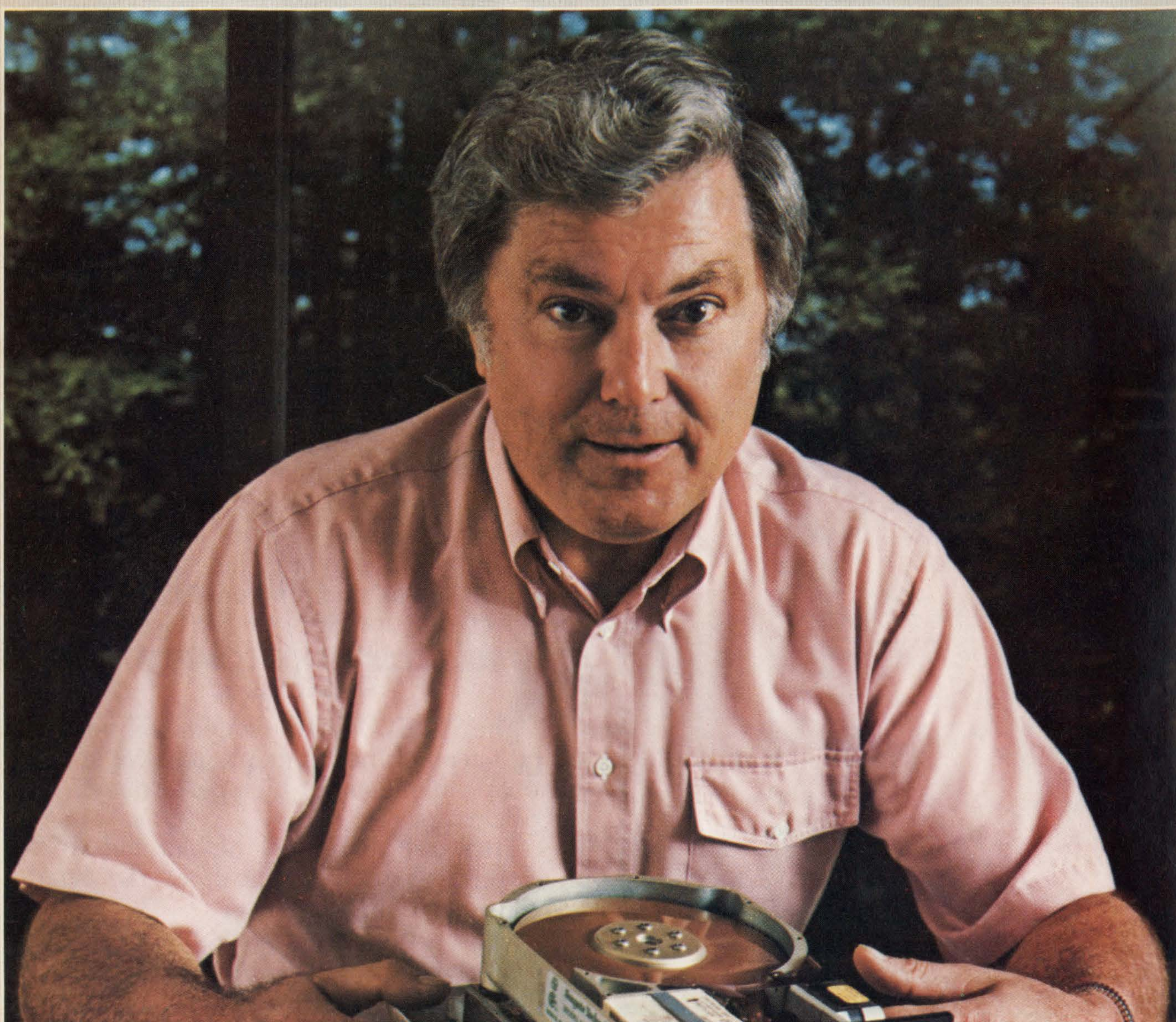

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CIRCLE 14

LETTERS TO THE EDITOR

Score one for the tiny floppies

Your flexible diskette evolution article, "Tiny Floppies Squeeze in the Bits" by Peg Killmon (May 1983, p 231), is one of the more informed, objective write-ups I've had the pleasure to read. There are, however, a few issues that I believe could benefit from further enlightenment.

The statement that 3″ media must push technology to achieve 5¼″ floppy compatibility is not consistent with actual experience. Media used in the 3″, 3¼″, and 4″ drives are virtually identical to those in the Iomega drive. Taking into consideration that the flux density of the Iomega application is twice that of 0.5M-byte 3″ media, and the track density is three times as great, 3″ media have more than enough potential to operate at up to 2M bytes. In addition, the Amlyn and Drivetec drives, which use the same media, are now operating at densities equivalent to a 3″, 1M-byte diskette.

By contrast, the original 3½″ product started out with a less than optimal, but available videotape media and head design. This is the product used in the Hewlett-Packard computer systems. But this medium couldn't meet the performance needs of the Microdisk Standards Committee (MSC) and wasn't compatible with existing digital head products. Consequently, a compromise was proposed to the ANSI committee that would accommodate Hewlett-Packard, yet be upgradable to 1M-byte capacity. According to Sony Research publications, still another medium is needed for future 1.6M-byte applications. Ironically, this future 3½″, 1.6M-byte medium will essentially be compatible with current 3″, 3¼″, and 4″ media. Thus, it is doubtful that the 3½″ MSC proposed product will offer greater reliability than the existing 3″ or 3¼″ designs.

Price sensitive end users are more likely to buy for value than for a corporate logo. Apparently, both the 3″ and 3¼″ products will have distinct performance and upgrade advantages over the 3½″ product. In addition, both the 3″ and 3¼″ originators are more experienced with and vertically integrated in digital storage technology. Through using one medium to cover a range of capacities, having access to internally developed, superior media substrates, and retaining media compatibility with evolving digital read/write head technology, the smaller sizes should have a decided cost advantage over the 3½″ concept. For these reasons, the future of the 3½″ product should not be taken for granted.

James DeStefano
Dysan Corp
5201 Patrick Henry Dr
Santa Clara, CA 95050

Give us the guidelines

Many journals carry articles on software design guidelines (discussing such topics as modularity, clarity, and maintainability). I would very much enjoy reading a tutorial on hardware design guidelines, discussing both the reliable design of hardware and such topics as redundancy, device-dependent rules, and documentation. Hardware design engineers can certainly profit by studying software guidelines, but there remain hardware-specific areas untouched by these. I feel that other design engineers would also enjoy such an article.

Robert Seidensticker
Aydin Computer Systems
401 Commerce Dr
Fort Washington, PA 19034

Glad you asked

Be sure to see the article on documentation (p 113) in this issue. Next month, don't miss the article we've scheduled on designing for reliability with microprocessors. Nice timing!

Clearing any confusion

My article, "Authoring a Dedicated Operating System in Pascal" (Apr 5, 1983, p 119), states that DEC is working on RSX-11M support for MicroPower/Pascal. This is not a current project. My apologies to the readers for any inconvenience this error may have caused.

Christopher DeMers
Digital Equipment Corp
Two Ironway
Box 1003
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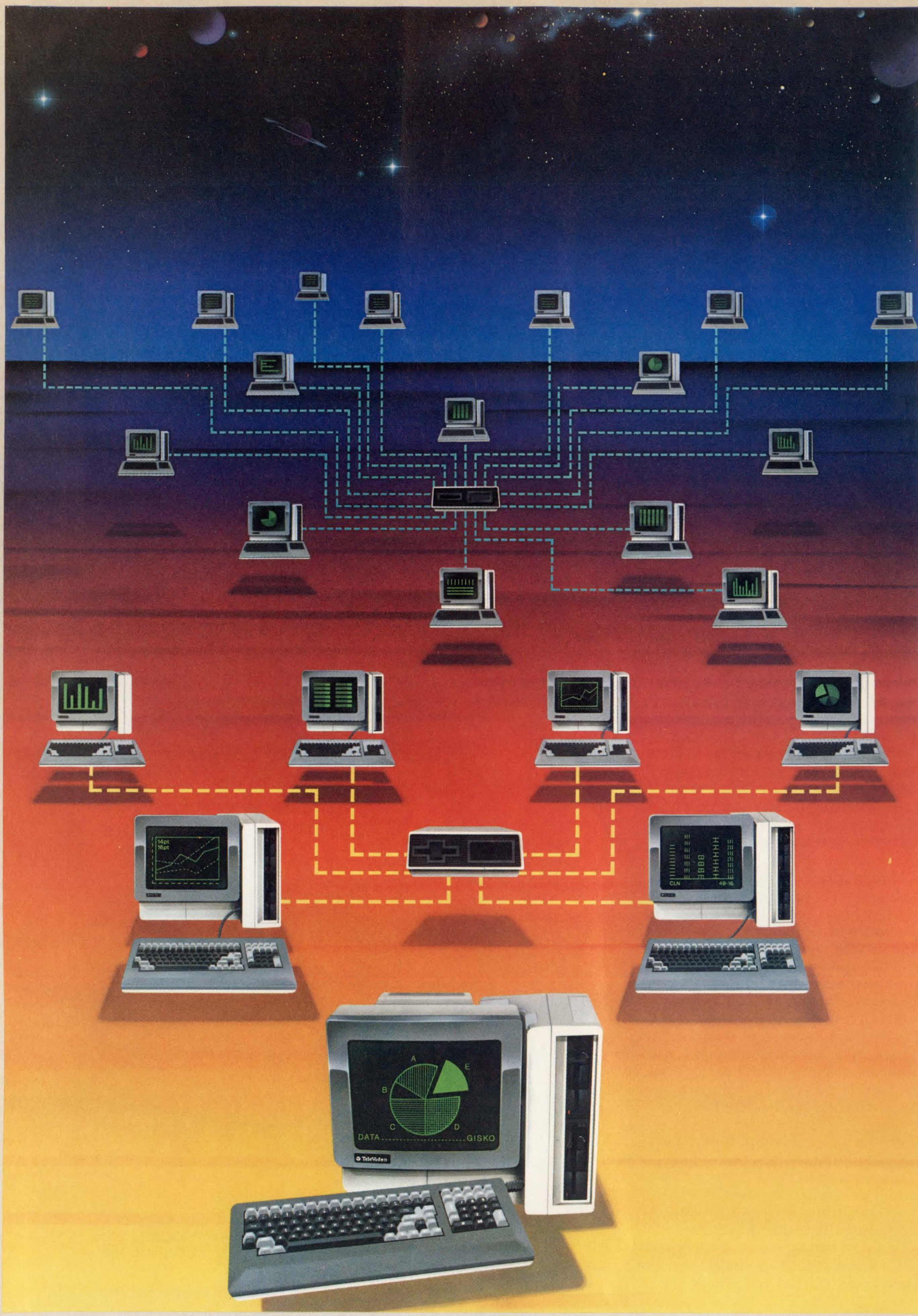
CIRCLE 16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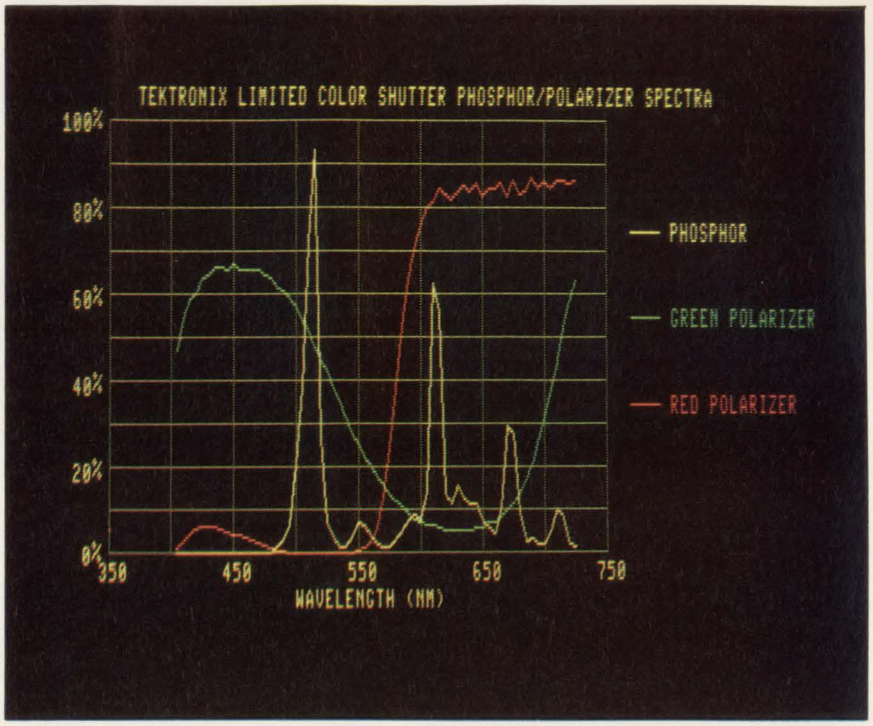
TeleVideo

Display combines CRT and LC technologies

Advancements in various display technologies are starting to yield innovative products for the system engineer. Prompted by the need for user friendly displays, some system manufacturers are developing displays for their products that combine different technologies to arrive at a desired resolution and color spectrum.

One such development was discussed and demonstrated at the Society for Information Display conference, held in Philadelphia, May 10-12. Engineers from Tektronix, Inc presented two papers focusing on a color display system that combines liquid crystal (LC) and CRT technologies. The system unites a monochrome CRT and liquid crystal "color switch" to produce a high-resolution field-sequential color display. The demonstration units have a spacial resolution of 480 lines x 640 dots on a 6.5" screen.



The display from the prototype unit shows the optical characteristics of the two polarizers and the phosphor of the 6.5" black-and-white screen.

Using a black-and-white CRT eliminated the need for cumbersome shadow masks and expensive penetration phosphors. Three liquid crystal color filters switch at the scanning field rate and eliminate the possibility of convergence problems. This results in a small package, according to company researchers. The compact design allows for practical color capability. "Applications could include computer workstations, where high color resolution is important, and word processing equipment, where monochrome displays have typically been used because high-resolution color displays are not possible or are too expensive," says John McCormick, manager of display research.

The CRT/LC display allows addition of color without any degrading resolution. Thus, it is also suitable for small instrument displays such as oscilloscopes, logic analyzers, and spectrum analyzers.

Functionally, the CRT has a simple phosphor with two separate emission peaks that are typically, but not limited to, red and green. The phosphor does not require any spattering or special process steps. In any one scanning field, the data written on the screen appear only in the color selected by the electronic switch. Each color is repeated at a 60-Hz rate, and with two interlaced fields, runs at a 120-Hz rate. The field-sequential system can mix all possible color combinations obtainable from the two primary colors within the phosphor.

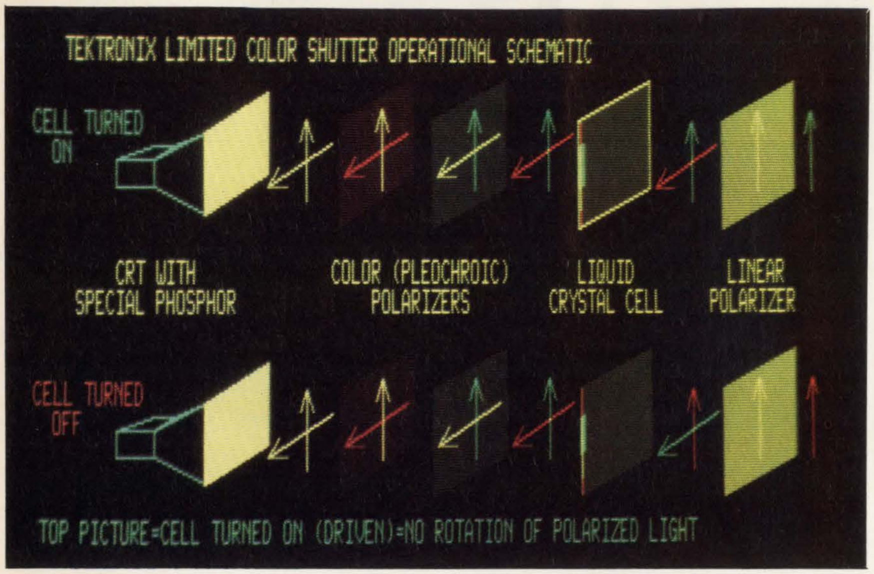
Previous attempts at producing a field-sequential system have suffered from lack of a suitable fast color switch. The LC color display uses a proprietary fast LC optical switch with a relaxation time (ie, time for the material to respond to an input voltage) of 1.7 ms, according to Tektronix engineers. The relaxation times of conventional twisted nematic LC devices to their twisted state are much longer, primarily because of the backflow-induced alignment phenomenon. One technique for obtaining fast response is to use "dual-frequency" twisted nematic devices. This technique, however, requires drivers that can deliver high-frequency signals to large capacitive loads. Other problems with this technique are the limited temperature range of the devices and the difficulty of getting cells to switch uniformly over large areas.

The company's system uses a single-frequency material in an LC device called a "π-cell." The LC device is sandwiched between and optically coupled to an orthogonal set of color polarizers and a linear polarizer. The package is placed in front of the CRT and switched synchronously with the fields of a sequentially addressed CRT. In this way, alternate fields are viewed through different colored filters; the eye integrates these to produce color images.

Flicker-free operation at 120-Hz rates requires LC cells that are capable of millisecond transition times for both the ON and OFF states. Company engineers claim that the very fast, bounce-free relaxation from the ON to the OFF state of the π-cell is comparable to, or better

(continued on page 28)

CRT/LC display
(continued from page 26)



In the LC/CRT sequential color display, the red and green information is sequentially written on a multicomponent phosphor screen. Color polarizers orthogonally polarize emitted red and green lights. The control logic sequentially rotates colored information into the transmission axis of the linear polarizer.

than, the response of dual-frequency LC materials under similar voltage-drive conditions and cell thicknesses. The LC device significantly reduces LC driver and driving waveform complexity and power consumption. In addition, the required single-frequency drive exhibits better stability in the device response to temperature and drive-frequency fluctuations. Moreover, the π-cell system has a large viewing angle for both of its dynamic states. This is due to a "self-compensating" feature in its dynamic OFF state and the thin LC layer for the ON state. The engineers believe that systems exhibiting a minimal color shift over a 90° viewing cone are now feasible.

Finally, a very high contrast ratio of 20 to 1 is achieved by combining color polarizers with either a diffusing or an antireflection coated linear-polarizer assembly. The contrast can be electronically tuned by modulating the CRT Z-axis to produce a display with good visibility in a high ambient-light environment.

Company engineers say that the good switching characteristics and viewing angle of the π-cell can be attributed to the critical, ultra-thin, uniformly spaced LC cells. They developed techniques for spacing cells from 3 to 10 μm apart with a 300-nm tolerance. Such tolerance is achieved in cells ranging from 5 to 40 cm on the cell diagonal without using preselected or ultra-flat glass. The engineers believe that these techniques could also allow cells to be built at reasonable costs over a wide range of sizes.

So far, company researchers have limited their development to using the two given fields of an interlaced raster system. Research continues to extend the concept to three fields, with three primary colors; this will produce a full-color gamut, comparable to, or better than, conventional color display technologies. **Tektronix, Inc, Imaging Research Lab,** PO Box 500, Beaverton, OR 97077.

—Nicolas Mokhoff, Senior Editor
Circle 240

TEST & MEASUREMENT

Logic analyzer speeds system integration

Software analysis and hardware/software integration abilities offered by Gould's K-105D satisfy the needs of 8- and 16-bit microprocessor system designers. Within the analyzer's chassis, users can plug in up to 72 state and timing sample inputs along with RS-232, GPIB communications, and data storage.

Three data board slots in the chassis hold one or two cards providing eight 100-MHz sample inputs and one or two cards supplying 32 inputs that sample at 20 MHz. The chassis also contains I/O board with RS-232, GPIB, and disk control circuitry; clock/threshold board; and MPU and data display boards.

The unit can be set up to sample 32 or 64 inputs at 20 MHz and 8 or 16 inputs at 100 MHz. Internal memory is divided into main, storage, and reference sections. Each memory is 1024 bits deep and up to 72 bits wide.

System activity can be synchronously sampled by combining eight external clock inputs into four Boolean expressions. Eight levels of trace control using up to 32 different word patterns allow precise analysis path definition and the selection of particular operational segments for recording and reviewing.

Main inputs, which normally monitor the microprocessor's activity, and high speed inputs are linked to aid in software integration. Optional disassemblers for 68000, 8086, 8088, Z80, 8085, and 8080 allow microprocessor operation to be monitored in assembly language mnemonics rather than in object code. This greatly improves debugging productivity.

Performance measurements such as graph and histogram modes allow system performance to be quickly characterized. Program tracking and data capture are provided by clocking and trace control features. These allow complex program flow to be followed using symbolic debug

(continued on page 32)

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CIRCLE 19

Selecting the right microprocessor...

—GARY L. TOOKER,
Senior Vice President, Motorola Inc. and General Manager, Semiconductor Products Sector

Logic analyzer
(continued from page 28)

to capture only data blocks of interest. These features also allow conditional jumps between levels and trigger recording using selected bit patterns or mnemonics.

System integration efforts are supported by a combination of 8-channel 100-MHz plug-ins armed and triggered by software-oriented, 32-channel, 20-MHz plug-ins. Eight-channel analyzer does high speed sampling and provides noise margin analysis and 5-ns glitch capture. The 32-channel analyzer supplies complex clocking and either 14 levels of triggering or 8 levels of trace control.

The system is able to compare expected versus actual operation on a bit by bit basis. Tolerance analysis can be added within user specified ranges. A range of times in which events occur can be selected by entering edge tolerances for entire data recordings, edges of specific interest, or a combination of these two.

Noise margin analysis automatically compares circuit operation over a range of thresholds and displays the results against normal operating voltages. This reduces test time, simplifies the complex measurement, and provides a system's maximum allowable noise specification.

Expanding the system to include the optional storage system further increases productivity. Storing up to 70 setup and measurement data files on this unit's two 5¼" floppy disk drives makes them readily available for reuse or reference.

Menu-driven screens make the K-105D setup easy. Parameter fields can be accessed sequentially or randomly via a parameter field cursor. Parameters are selected sequentially or randomly. The keyboard supplies soft function keys as well as a set of cursor keys that are used for both setup fields and recording displays. An additional help key activates a brief onscreen explanation of each parameter field's functions and selections. Further help is available from onscreen display of a 28-page users' mini manual. **Gould Inc, Design and Test Systems Div,** 4600 Old Ironside Dr, Santa Clara, CA 95050-1279.

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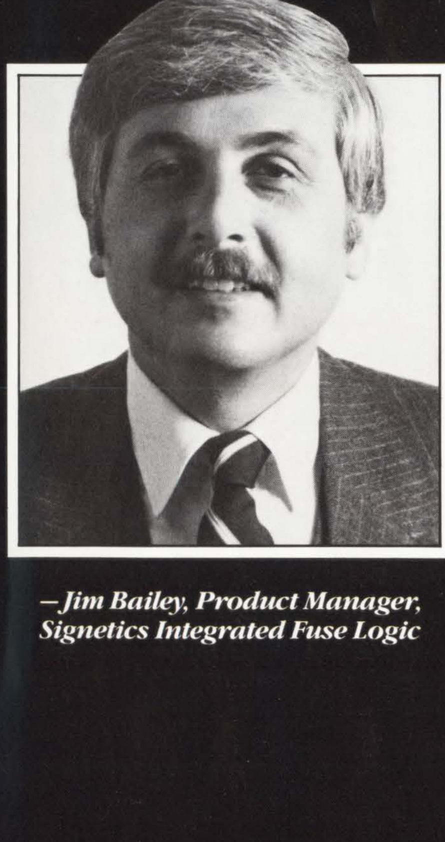
CIRCLE 20

"Where do you go from SSI/MSI instead of going to gate arrays?"



—Jim Bailey, Product Manager, Signetics Integrated Fuse Logic

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It's such an easy step to take. Instead of filling up breadboards with loads of TTL, you take a shortcut with the simplest, programmable logic on the market—Signetics' short circuits.

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If you can write a Boolean equation, you're home free.

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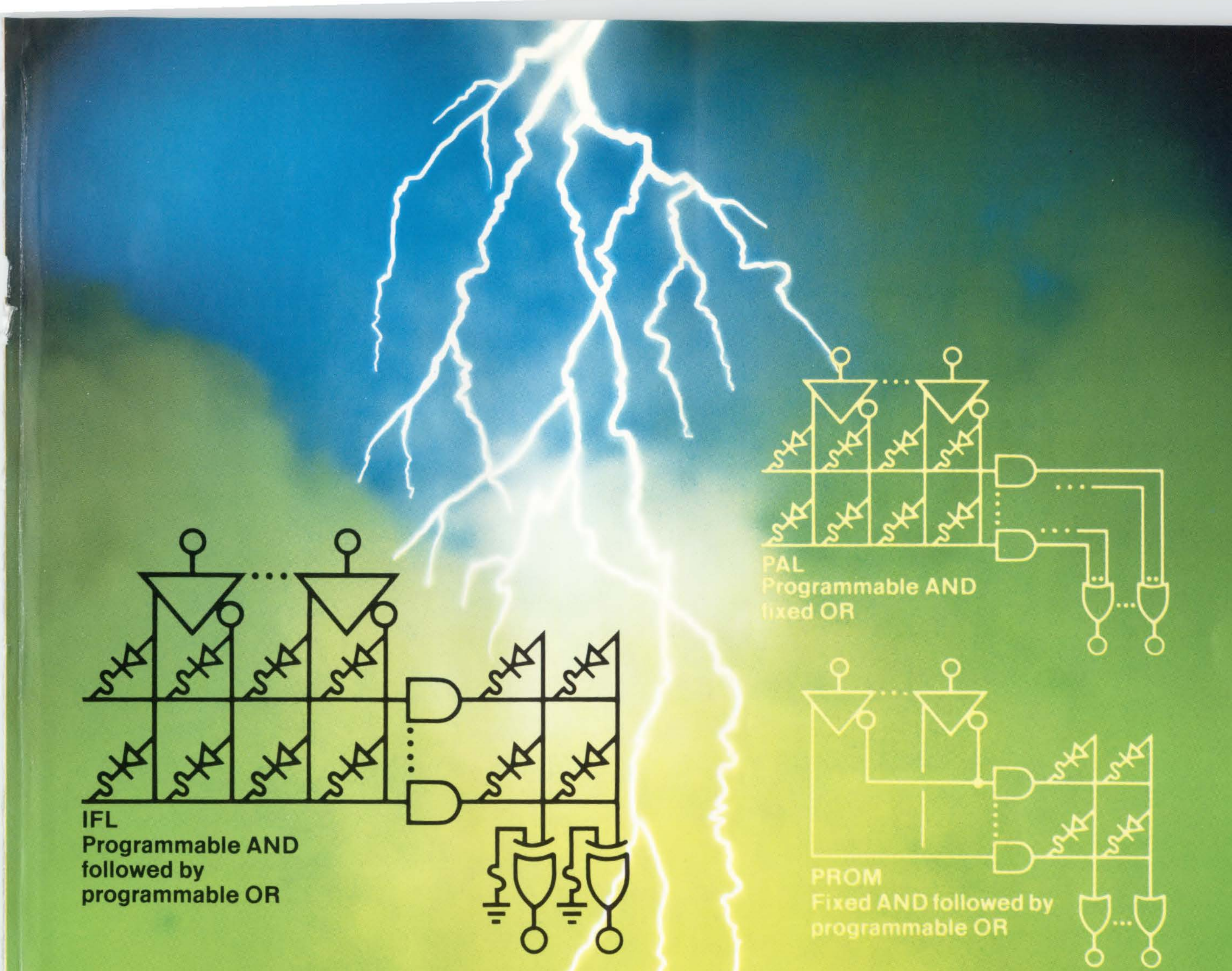
"Our short circuits blow other devices right out of the water."



When you stack them against standard TTL, it's simply no contest. Our circuits are field programmable, with customizable functions and a high level of integration. We cut your PC boards down to size—often using as little as 1/10 the area—and improve the reliability of your system.

Compared with gate arrays, we offer a shorter development cycle, lower initial cost, less design risk and off-the-shelf availability. It only takes you 30 seconds to blow our fuses, versus 6 to 8 weeks just to get a gate array mask.

And our short circuits, technically known as Integrated Fuse Logic (IFL) here at Signetics, have a lot more going for them than the other programmable logic devices you can buy, such as PALs.™

"We're a lot friendlier than PALs."

You may have heard about PALs (Programmable Array Logic). But have you heard that IFL combines the advantages of PROMs and PALs by offering both programmable "AND" and programmable "OR" arrays in one device?

That's not all. Depending on the device complexity, our IFL circuits offer several additional features that give you even more design flexibility—such as programmable active output levels. You can also count on us to deliver reliable parts in quantity, since we use proven PROM technology. And, since you use standard techniques to program our circuits, you can get the necessary equipment from a variety of sources.

As you can see, our IFL architecture provides a much more flexible approach than the PAL.

Our devices are unique in their ability to implement logic directly. They offer the most useable P-terms per output, the most inputs and outputs, and the most straightforward programming of any logic device in the industry. This all goes to show what powerful design capabilities our flexible IFL offers you compared with the fixed AND or fixed OR arrays of other circuit types.

In short, when you use our circuits, you'll find it very smooth sailing.

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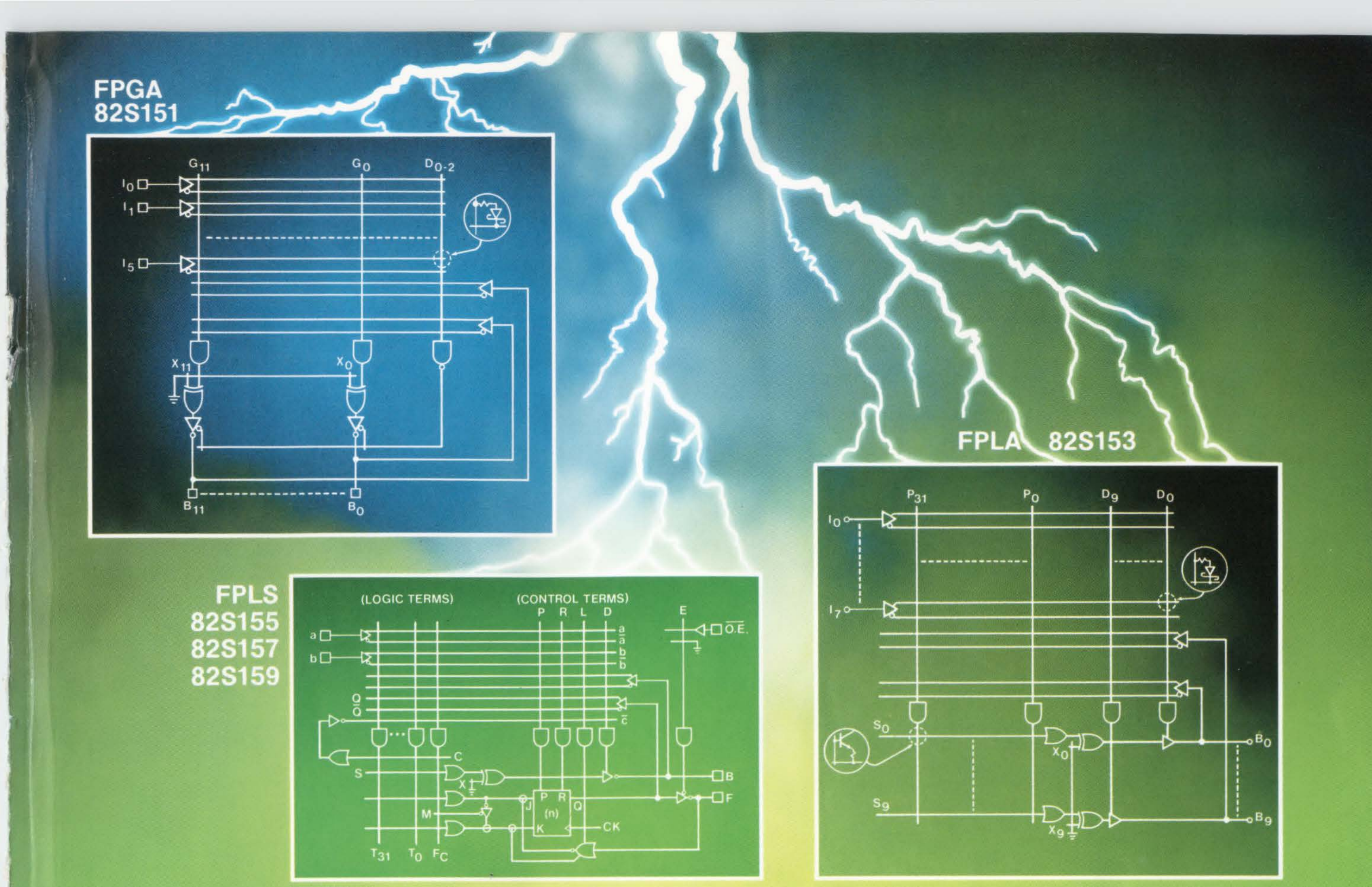
"It's a short family, but it's long on flexibility."



Since you can make our IFL circuits do just about anything you want, you don't need a huge catalog of parts. In fact, you'll find all you need in our three basic short circuits: the Field Programmable Gate Array (FPGA), the Field Programmable Logic Array (FPLA) and the Field Programmable Logic Sequencer (FPLS) which come in 20-, 24- and 28-pin packages. In both plastic and cerdip.

The 82S151 FPGA consists of 12 AND gates with fusible link connections for programming I/O polarity, I/O direction output enable control and true or complement inputs.

Typically, you'd use this 20-pin circuit for random gating functions, address decoding for peripheral selection, memory mapping, fault monitoring and machine state decoding.

If you need a byte-organized device, the 28-pin fixed I/O 82S103 will do the job. It has 9 AND/NAND gates sharing 16 common inputs.

The 20-pin 82S153 FPLA is made up of two-level logic, having 32 AND gates and 10 OR gates, with fusible link connections for programming I/O polarity and direction. Its uses are similar to those mentioned above, plus function generation and multiplexing.

The 82S100 fixed I/O, 28-pin FPLA can be used in CRT display systems, code conversion, microprogramming, character generation, data security encoding, frequency synthesis, interfacing, and random logic replacement. It has 16 dedicated inputs and 8 dedicated outputs.

These FPLA devices are extremely popular because they use the familiar AND/OR/Invert architecture to implement custom sum-of-product logic equations directly.

The 20-pin 82S155/7/9 FPLS devices consist of registered logic elements combining AND/OR arrays with clocked J/K flip-flops, which are dynamically convertible to D-type. These circuits have 4, 6 and 8 registers respectively, all of them having three state outputs and programmable I/O.

These Logic Sequencers are ideal for synchronous up/down counters, shift registers, random sequential logic, bidirectional data buffers, timing function generators, and priority encoder/registers.

The 28-pin 82S105 is a Mealy-type programmable state machine. It contains logic AND-OR arrays with user programmable connections which control the inputs of on-chip state and output registers. It offers six state registers, with 16 input variables and output functions as fixed I/Os.

You can use them for interface protocols, sequence directors, periperal controllers, timing generators, sequential circuits, counters and shift registers.

We now offer more than 20 IFL circuits. And 38 bipolar PROMs. That gives you all kinds of flexibility for designing your next system with user programmable logic. And you'll find it easier, faster and less expensive with our short circuits than any other way.

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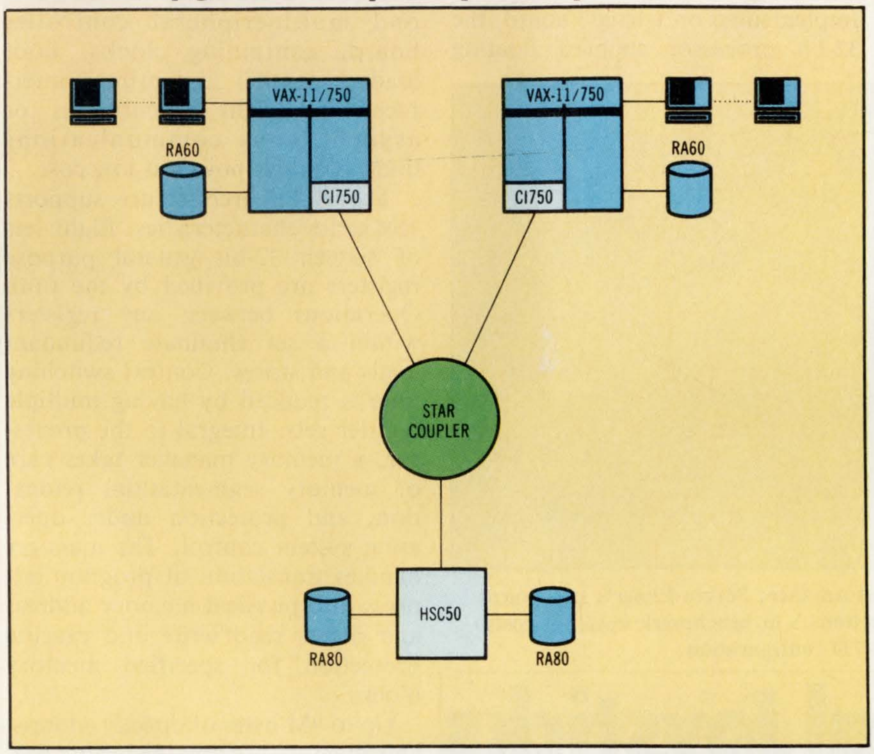
Cluster upgrades capacity and performance



VAXcluster system configured for high availability can include dual-ported disk units connected between pairs of storage controllers to provide an entirely redundant link from each processor to stored data. VMS operating system will provide data integrity and availability features to match the system's hardware potential. One such feature is an automatic switchover of disk devices to prevent interrupting an HSC50 operation.

VAXcluster extends level of computing power, storage capacity, and existing computer system availability. To this end, Digital Equipment Corp's technology permits multiple computers and intelligent storage subsystems to function as a single system. The concept presents "a new way to grow systems" without sacrificing existing investments, according to the company.

A star coupler serves as the common connection point for all cluster configuration nodes. Delivered in an 8-node version, the coupler accommodates computer interconnect (CI) bus cables in a radial or star arrangement. CI buses are redundant 70M-bps data paths. Each bus consists of two transmit and two receive cables and handles up to 16 nodes. Each node can be a processor or storage subsystem consisting of an intelligent mass storage controller with up to 24 disk drives. Processors connect to the CI bus through microcoded intelligent controllers—the CI780 to the VAX-11/780 and the CI750 to the -11/750 processor.

The HSC50 hierarchical storage controller simultaneously handles multiple operations on several disk drives and optimizes physical operations to gain maximum throughput. It relieves the host systems of utility operations such as volume shadowing, image copying, and image backup.

Connecting to both CI bus paths, the CI interface uses whichever path is available. Using both paths enhances throughput; however, if one path is not available, traffic shifts automatically to the remaining one.

The loosely coupled multiprocessor design not only supplies modular system growth, but also increases system availability. Using a message-oriented interconnect allows cost effective systems to be built. A clustered configuration can survive processor, controller, or disk disruption by use of multiple copies of the operating system.

A key component of the cluster architecture, VAX VMS operating system software is integral to cluster operation. Its facilities support system availability, multisystem file and record sharing, and the addition of processors and storage devices. VMS Version 3.3 supports a mix of -11/780 and /782 processors and HSC50 storage controllers with shared disk support. The software supports dual-porting disks between two storage controllers for increased fault tolerance. Version 3.4 extends these features to the /750. Future releases will take advantage of the hardware's data protection and fault-tolerance potential; they will be able to survive and reconfigure around individual failed nodes. In addition, facilities will be supplied to ensure that data stored in a cluster remain in a known state.

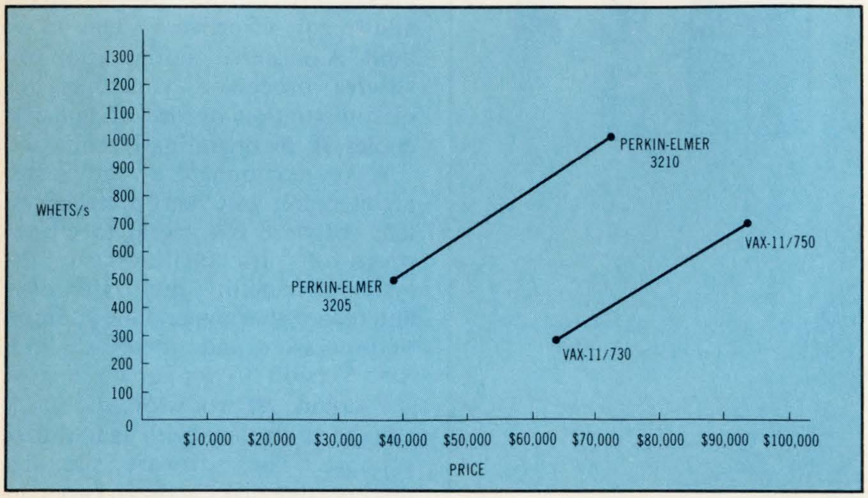
DECnet-VAX communication software enables a cluster processor to function as a long distance network node. The interface can also be used within a system, with the CI bus as the main communication link.

Price of a CI780 interface to VAX-11/780 and /782 systems is $19,500. The star coupler equipped to receive eight nodes is $7500; an upgrade kit to expand this from 9 to 16 nodes costs $5500. The HSC50 intelligent storage controller carries a price tag of $32,500, with disk channels at $7100 each. **Digital Equipment Corp,** Maynard, MA 01754. **Circle 242**

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

Compact supermini cuts computing costs

Model 3205 drives down the cost of 32-bit computing. At a price of $9950 (quantity one), users gain entry to the 3200 series family that ranges upward to the 21M-instruction/s 3200MPS superminicomputer. Implemented on a single board, the 32-bit processor supplies floating point capability, selector channel, and 512K bytes of memory. A second multiperipheral controller board, containing clocks, boot loader, parallel line printer interface, and eight synchronous or asynchronous communications lines, provides power at low cost.



Ranking between VAX-11/730 and /750 in performance, Perkin-Elmer's 3205 churns out 506k single-precision Whetstone instructions/s in benchmark tests, yet costs less than half as much as a comparable 11/730 configuration.

The 32-bit architecture supports 3200 series characteristics. Eight sets of sixteen 32-bit general purpose registers are provided by the CPU. Operations between any registers within a set eliminate redundant loads and stores. Context switching time is reduced by having multiple register sets. Integral to the processor, a memory manager takes care of memory segmentation, relocation, and protection under operating system control. The manager handles translation of program address into physical memory address and offers read/write and execute protection for specified memory blocks.

Up to 4M bytes of directly addressable memory are obtained using 64K RAM technology. Leadless carrier packaging technology reduces the memory's physical size. This leaves room for 3M bytes of memory on the memory expansion board; the CPU board itself holds 1M byte.

The multiperipheral controller relies on microprocessor technology to implement most common I/O functions on a single board. Among the features of this card are eight RS-232 full-duplex communication lines that support asynchronous, synchronous, SDLC, HDLC, or Bisync operations at 50 to 19.2k baud.

Data handling assist supplies efficient operation for data communication applications. The loader storage unit automatically loads the OS/32 operating system from secondary storage after a power fail/restart sequence or for initial program load. The board also provides universal clock, watchdog timer, parallel printer port, and self-test features.

Dual communication buses allow the I/O configuration to fit specific

(continued on page 44)

 CIRCLE 21

New Amdek 3" micro-floppydisk drive system!

AMDISK-III . . . OEM's choice:

- Works with standard 5¼" controllers
- Up to 1 megabyte of unformatted double density storage
- Ideal for industrial data collection/storage applications
- Microfloppy's hard plastic diskette offers increased durability vs. 5¼" floppies
- Automatic shutter protects media
- Small form factor for easy storage

Specifications

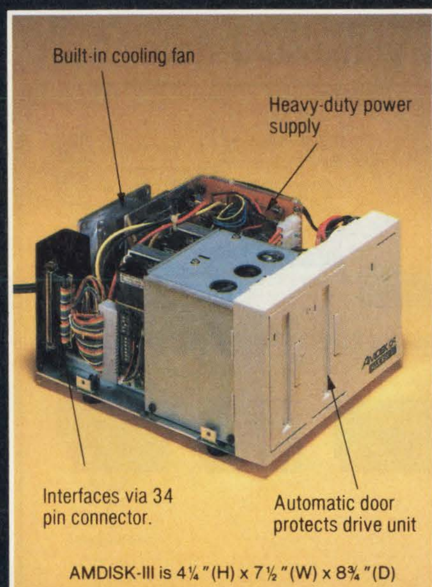
	Unit	Double Density
Capacity		
Unformatted Per Surface	Bytes	250K
Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	0.7 (min)
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10^{-9}
Hard Error		10^{-12}
Seek Error		10^{-6}
Media	3-inch Cartridge	
Drive Interface	Plug Compatible with 5.25 inch FDD	

External Interface

Connector: 34-pin (Shugart)

Pin No.	Signal	Pin No.	Signal
2	Unused	20	Step
4	In use (option)	22	Write data
6	Drive select 3	24	Write gate
8	Index	26	Track 00
10	Drive select 0	28	Write protect
12	Drive select 1	30	Read data
14	Drive select 2	32	Unused
16	Motor on	34	Ready
18	Direction	1-33	Ground

NOTE: Single head per drive



AMDISK-III is 4¼"(H) x 7½"(W) x 8¾"(D)

Evaluation samples $480

Includes two-drive Amdisk unit with built-in power supply, 4 diskettes and application literature . . . Call (312) 364-1180.

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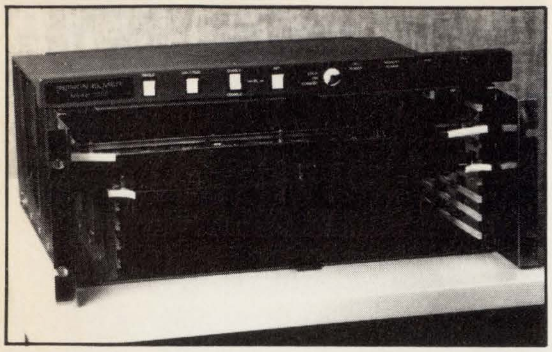
CIRCLE 22

Compact supermini
(continued from page 42)



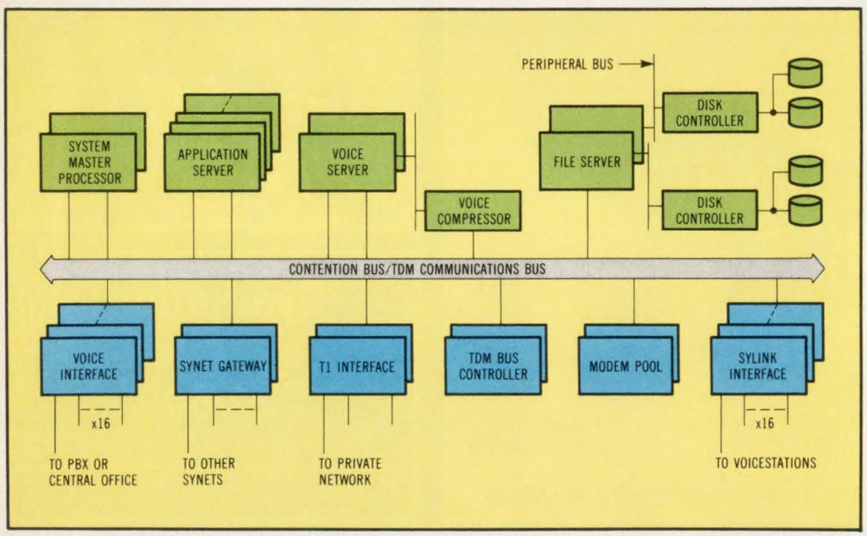
needs. The multiplexer bus handles transfers at 334k bytes/s; the selector channel bus caters to high speed devices with its 1.5M-byte/s rate.

Software compatible with other series 3200 processors, the 3205 runs under the company's OS/32 and Edition VII Workbench. Languages include universally optimizing ANSI-77 FORTRAN VII, Pascal, COBOL, BASIC, CAL MACRO, RPG II, and CORAL 66.

Users can migrate applications developed on larger systems down to the 3205 for execution at low cost.

Priced at $6169 in OEM quantities of 100, the unpackaged version includes CPU board with 512K bytes of memory, multiperipheral controller, and 7″ (18-cm) chassis with five I/O slots and one memory expansion slot. The processor is also available as a complete system. Packaged with 512K-byte memory, system console, power supply, 40M-byte Winchester disk, selector channel, and disk controller, the unit sells for $24,950. **Perkin-Elmer Corp, Data Systems Group,** 2 Crescent Pl, Oceanport, NJ 07757.
Circle 243

Local network integrates voice and data



In the SIM, the SyNet bus is really two buses; the TDM communications bus and the contention bus. The operating system allocates tasks to the application servers as needed. File requests are routed to the file servers. Digitized voice messages are switched via the TDM bus while data travel over the contention bus.

A distributed computing system integrates data with digitized voice and lets users access both computing and telecommunications resources. This is done via an integrated desktop workstation called VoiceStation that is connected to a central multiprocessor system through 2-wire phone lines. The VoiceStation system, by Sydis, Inc, does more than switch voice lines among system users and the outside world: it employs digitized voice information to perform digital recording and store-and-forward services.

Central to the office automation system is the Sydis Information Manager (SIM), which incorporates multiple 68000 processor boards with
(continued on page 46)

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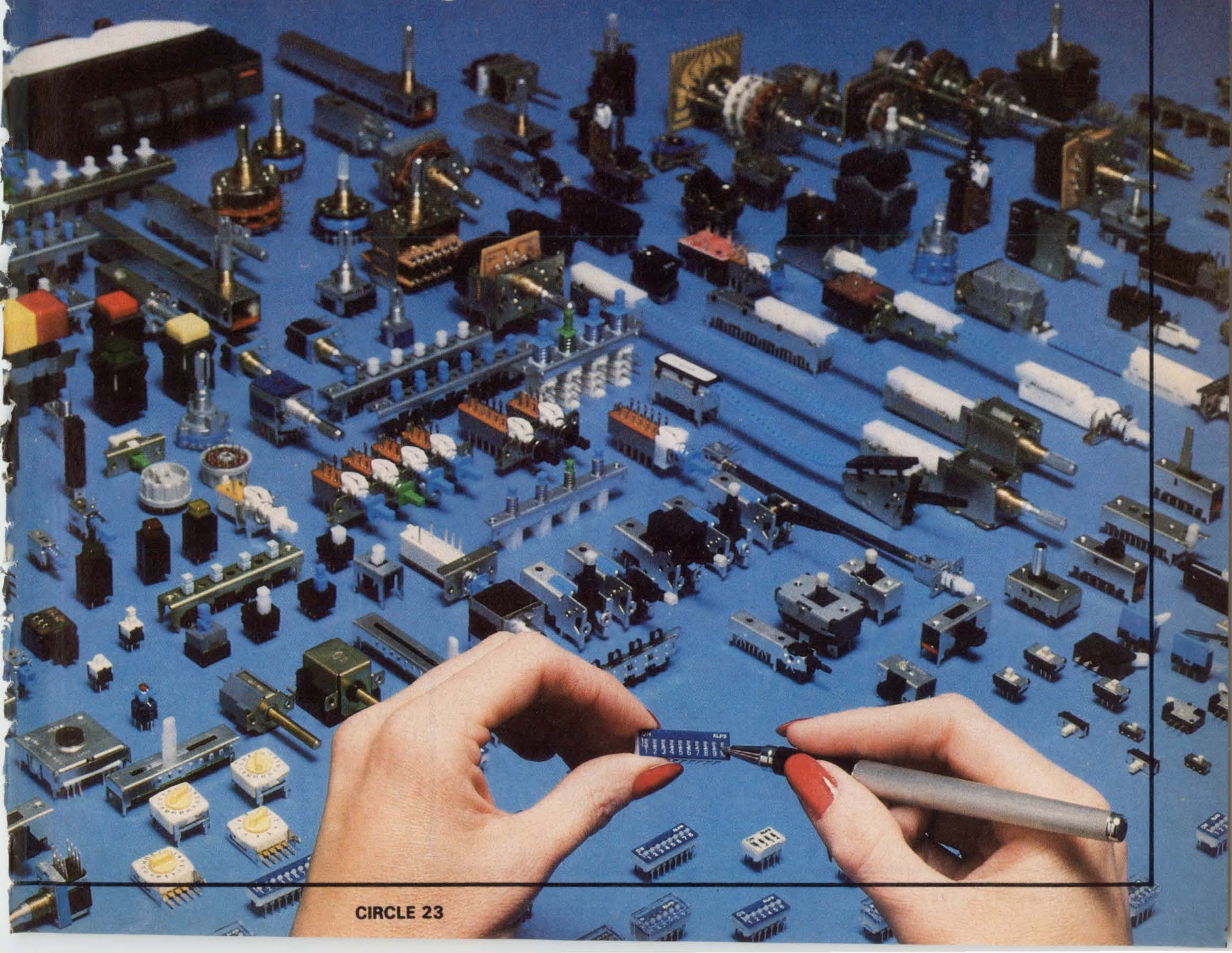

CIRCLE 23

Local network
(continued from page 44)

between 512K and 2M bytes of memory on a time division multiplexed (TDM) communications bus. The entire system incorporates an extended version of the Unix operating system that assigns tasks to CPUs as needed rather than dedicating a processor to a user. Boards attached to the bus fall into two groups: the processor group and the communications group.

In the processor group, the processor boards, or server processors, are further classified into application servers, file servers, voice servers, and a system master. The server processors are connected to the SyNet bus, which is really two buses. One of these is the redundant TDM bus, which is similar to buses used in many digital private branch exchanges (PBXs). It can switch 468 full-duplex time slots at 128k bps per time slot. Under the control of the Unix operating system, the system master dynamically allocates these time slots.

Within the SyNet bus, the other bus is the contention bus. It is a redundant 64M-bps carrier sense multiple access/collision detection bus used for data transfers between server processors. Third in the SIM system—but not part of the SyNet bus—is the peripheral bus. Through it, disk and tape controllers communicate with the file servers and their attached devices.

The communications group of boards contains one or more voice interfaces; modem pools; T1 interfaces; gateways to other SyNets; or one or more SyLink interfaces that are used to communicate with the voice stations. Each SyLink interface can connect to 16 voice stations over a single twisted pair of standard telephone wire at a bandwidth of 320k bps per channel. Each channel is further broken down into five 64k-bps channels: three voice or data channels, one command channel, and one link overhead channel. The SyLink interface performs the timing and synchronization required to map the channels into TDM bus time slots.

Forming the company's voice station is a terminal with a built-in multiline speakerphone and handset, detached keyboard, and a mouse for positioning the cursor on the 832- x 608-pixel display. Telephone function and line keys are placed along the left edge of the display, and soft function keys are mounted along the bottom edge. Key status is displayed graphically in the screen's windows. As further status indicators, graphic icons represent various familiar office objects such as a word processing file, a voice memo, or a graph.

In addition to a dual UART for digital I/O from the phone keypad, keyboard, and mouse, the company's voice station contains a link circuit for digital communication over the 2-wire link to the SIM. This link circuit transfers digital data to and from display memory and the digital I/O circuits over the internal 68008 bus. It also contains a codec that digitizes voice from the handset for transmission to the SIM. An internal 68008 processor in the voice station controls an 8-bit programmable DMA sequencer as well as 128K bytes of terminal and bit-mapped RAM. Up to four separate windows can be displayed and manipulated on the screen at one time. These represent up to four processes that one user can run simultaneously.

The voice server (one of the process servers previously mentioned) handles digitized voice in various ways to create, edit, and listen to voice messages. Functions are accessed via soft keys in terms of standard tape recorder functions (eg, play, stop, and rewind). The voice server also performs silence detection and voice data compression to 24k bps. Voice messages can then be stored, retrieved, and edited as digital data files.

Voice messages can be appended to data files (eg, word processing files) as voice memos or comments.
(continued on page 49)

 CIRCLE 24

The Lundy UltraGraf® is absolutely the fastest draw in the West or anywhere else.

This is the fastest, most intelligent 3-D computer graphics workstation available. The superlatives would seem to indicate a high price, too. But the Lundy UltraGraf workstation is surprisingly low cost considering its unmatched performance features.

At Lundy we don't develop technology for its own sake; we develop it to meet your needs. In the case of 3-D computer graphics workstations, you needed more speed, higher IQ, larger display and easier operation. UltraGraf delivers all four.

The Lundy UltraGraf is first when it comes to speed and IQ.

Keys to UltraGraf's instant response are a high speed microcomputer and a high resolution vector display, both developed by Lundy.

Besides these features, we've designed more intelligence into the workstation, so UltraGraf places fewer demands on your host computer.

The result is unmatched interaction while freeing up your host computer to concentrate on other operations.

19 × 15 inches sets a new screen standard.

UltraGraf's 21-inch CRT has the largest viewing area—19 × 15 inches—in the industry. Fast vector drawing and minimum operator time produce easy-to-read, flicker-free images. Spot size is only one ten thousandths of an inch, which produces remarkable crispness and clarity.

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Lundy helps you see more in graphics.

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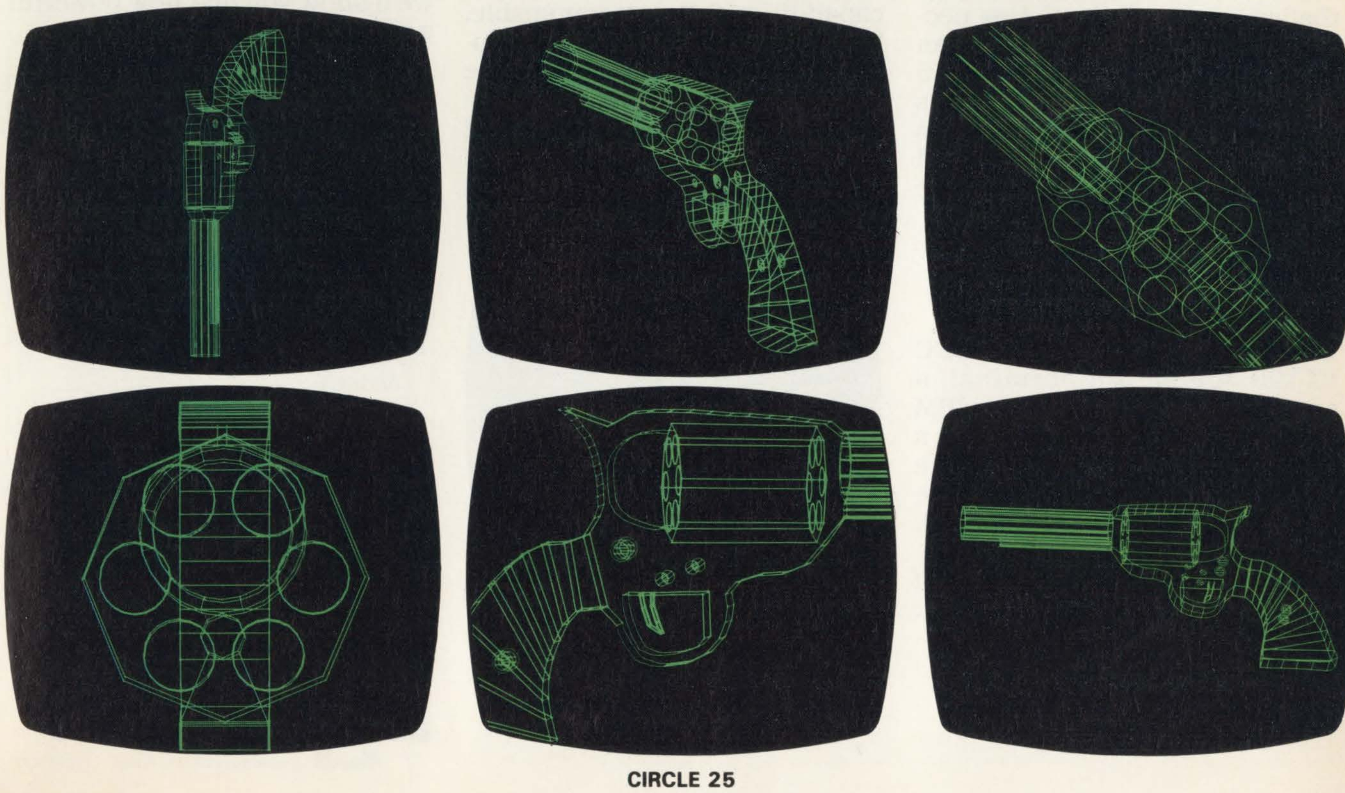
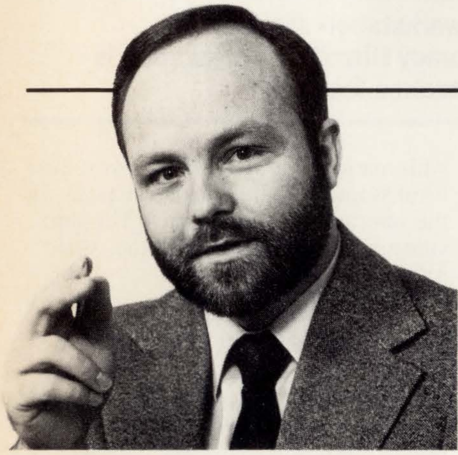


CIRCLE 25

"Our new CRT terminal chips give you a lot more features to work with. And a lot less parts to pay for."



—James Goodhart, Applications Engineer

Last year, we introduced a four-chip CRT set that lets you build an entire terminal in LSI. With a total of only 13 parts. Not a typical dumb terminal, either; this set gives you quite a list of features.

Now we're giving you even more to work with. We're adding two new chips to the family, to give you the only color chip set on the market. First, there's our SCN2674 Advanced Video Display Controller (AVDC), an NMOS part that generates all the timing necessary for a CRT monitor. Then there's our high-speed SCB2675 Color/Monochrome Attributes Controller (CMAC), a bipolar chip that controls video attributes and generates color or monochrome video inputs to the monitor.

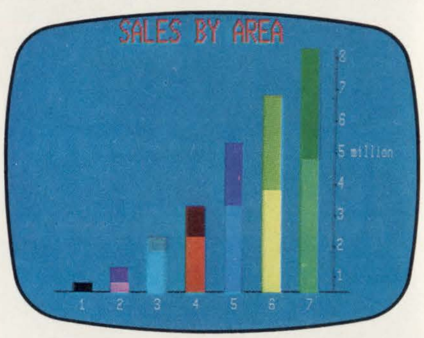
"We designed in a lot more features. And a lot more flexibility."

Whether you're building a DEC VT100 compatible terminal, a small business computer, an IBM 327X compatible product or a process control display, these chips make it easy to choose exactly the capabilities you need, just the way you asked for them. We've designed the attributes of all these terminals into this set. We've given you color or monochrome modes. Four gray shades. Character and graphics modes. Bi-directional soft or pop scrolling. Business graphics. User-selectable bit-mapped graphics. And a dot rate of more than 25MHz.

In the color mode, a user can simultaneously select eight colors for character video and eight for background video. In monochrome mode, the display can be set up on a white, gray or black screen background, with characters and background programmable to any of four intensities (black, gray, white or highlight).

Both modes include double height, double width, underline, blank, blink, dot-stretching and dot width modulation attributes. And since these two chips manage these functions with a minimum of CPU intervention, the result is a higher overall level of system performance.

Better yet, we've made all these capabilities fully programmable. We've also given you several memory addressing modes to choose from, including row table addressing, so you're not stuck using just one kind of architecture. With all this flexibility, you can build almost any kind of terminal you like with this set. In a lot less time, and with a much simpler inventory. Obviously, this also makes it a lot easier to respond to changes in the terminal or system specifications.



Our two new chips let you build a mid-range CRT terminal with less than 20 parts. In living color.

"You won't believe what we've done for your costs."

If you thought you couldn't afford to build all these functions into a low-cost terminal, you're in for a surprise or two. Because we've made the price of this color set one of its best features. In fact, the system cost is actually lower than what you'd pay to build a dumb monochrome terminal with anyone else's parts. To make things even more interesting, we've also cut the price of last year's four-chip set to an all-time low.

So whether you're designing a monochrome or color terminal, get in touch with us now. We'll send you complete app notes, data sheets, and samples. Best of all, we'll show you just how powerful a price list can be.

Please send full information on all your chips for CRT terminals, small business computers, and other display applications.

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Local network
(continued from page 46)

The voice editor displays broken lines that depict utterances in order to help the user position the cursor for playback and speech segment editing.

In addition to the usual Unix package of C programming tools, the company includes several application programs called Knowledge Tools. These feature word processing, electronic mail, telephone call processing, etc. Other tools include callable library functions that integrate OEM-written applications with the soft function keys, telephone keys, and voice annotation, as well as dictation and transcription. **Sydis, Inc**, 4340 Stevens Creek Blvd, San Jose, CA 95129.
Circle 244

Collision avoidance accelerates transfers

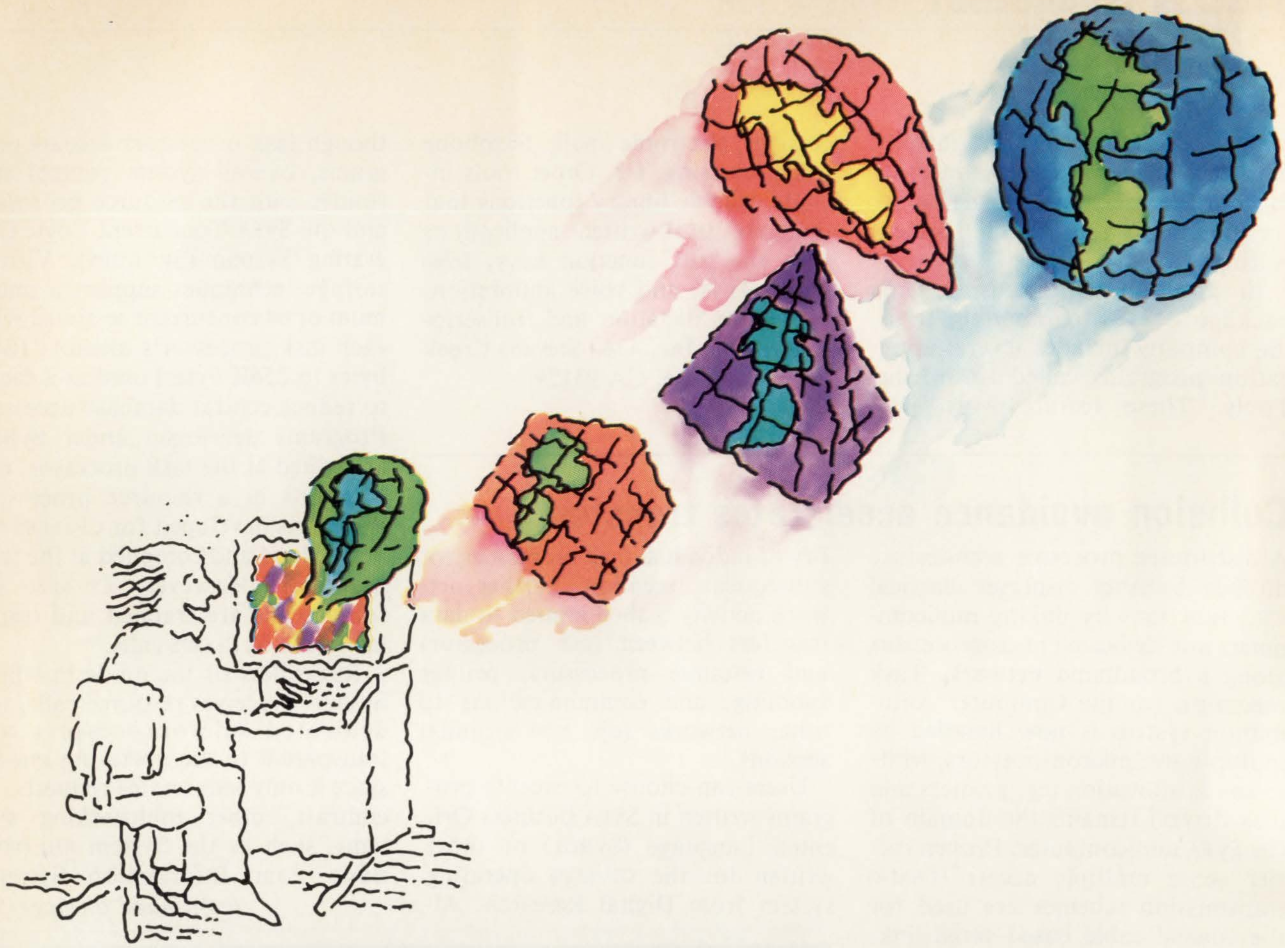
A distributed processor architecture dubbed SyFAnet disperses classical CPU functions by linking minicomputers and dedicated microprocessors along a broadband network. Task execution for the Computer Automation system is now handled by multiple 8088 microprocessors, while resource allocation (eg, printers and disk drives) remains the domain of the SyFA minicomputer. Proven carrier sense multiple access (CSMA) transmission schemes are used for the coaxial cable based serial link. However, the company opts for collision avoidance rather than collision detection (a la Ethernet) to increase actual data throughput to about 1.5M bytes/s.

Minicomputers are ideal as resource processors since their operating systems efficiently handle memory and peripheral management. They can also handle I/O processing that requires high throughput, as well as data communications. On the other hand, program execution takes up an excessive amount of CPU time, with noticeable performance degradation as users are added to the system. Microprocessors can quickly execute single task code with rapid screen updates. Consequently, if dedicated to execute single tasks, microprocessors carry no operating system overhead. Performance can be maintained if more task processors are added as users join the system.

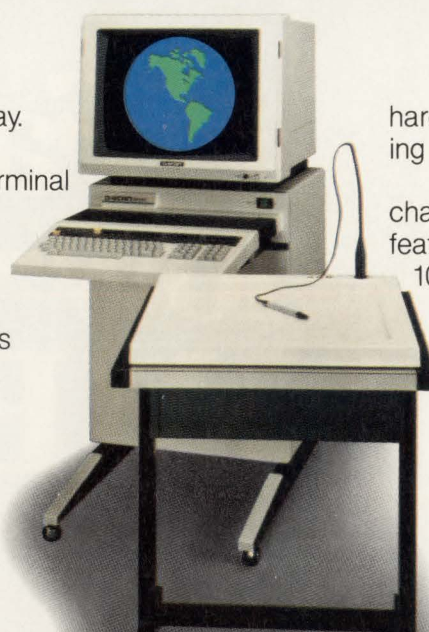
As implemented in SyFAnet, individual task processors request application programs from the resource processor. These programs are passed in their entirety from the central data base to the working memory of individual task processors for subsequent execution. Further network activity is then limited to data transfers between task processors and resource processors, printer spooling, and communications to other networks (eg, 3270 terminal session).

Users can choose to execute programs written in SyFA Business Oriented Language (SyBOL) or those written for the CP/M-86 operating system from Digital Research. Although task processors execute programs, overall system control still resides with the resource processor and the SyFA Concurrent Logic Operating System (SyCLOPS). Virtual storage techniques support a maximum of 64 concurrent sessions, with each task processor's memory (64K bytes to 256K bytes) used as a cache to reduce central database accesses. Programs developed under SyBOL are edited at the task processor, but compiled in a resource processor. Programs developed for CP/M-86 are both edited and compiled at the task processor. However, CP/M-86 resource calls are trapped and translated into SyCLOPS calls.

Regardless of the mode in which SyCLOPS receives resource calls, the dedicated microprocessors are transparent to the operating system since it only sees service requests. In contrast, other multitasking systems, such as the System 810 from Basic Four Information Systems
(continued on page 51)



CHANGE THE WORLD.



GR-2412 with standard 20-in. x 20-in. digitizing tablet. GR-2212 (monochrome) also available.

Or anything else you can display. Easier and faster than you imagine. Because D-SCAN's new GR-2412 terminal is changing the cost/performance standards for raster scan graphics.

Its world address space, for example, is a full 32K by 32K. Large enough to handle the most ambitious project. Yet easily manageable with dynamic zoom, pan, window, and viewport commands.

Its zoom operation faithfully preserves resolution and detail, instead of simulating it with pixel replication.

And those aren't all the improvements we've made.

Our dual microprocessor architecture draws 12,500 short vectors per second while transferring data at 19.2 kilobaud. And our exclusive anti-aliasing hardware removes jaggies without affecting drawing speed.

About the only thing we didn't change is our long list of standard features. Like our high resolution 1024x780 display. Local transformations. Up to 768K bytes of local segment memory. 4014 emulation mode. And the 10 years of Daini Seikosha (Seiko) craftsmanship in every D-SCAN product.

If you're ready to make some changes, contact us at Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051. Telephone (408) 727-0768.

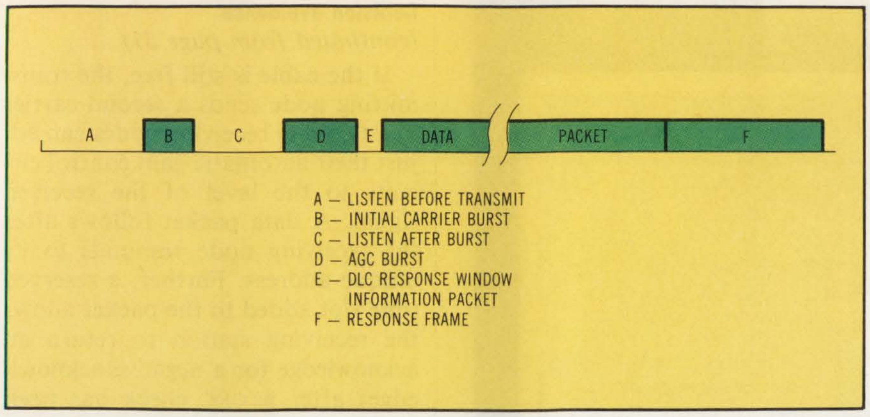
We'll give you a terminal that can take on the world.

D-SCAN

Seiko Instruments U.S.A., Inc.

CIRCLE 28

Collision avoidance
(continued from page 49)



A proprietary CSMA/CA scheme implemented by Computer Automation differs from collision detection schemes, such as Ethernet, by adding a second carrier sense (C). In this way, the transmitting node has exclusive use of the cable. A response frame (F) allows the receiving node a chance to acknowledge packet reception.

(*Computer Design,* July 1982, p 26), have multiple processors viewed as a pool of resources managing disk drives or printers. Consequently, their operating systems increase in complexity as tasking semaphores and mailboxes are added to synchronize tasks and ensure file security. Extensive system overhead results.

The broadband network acts as a backplane bus so that the dispersed resource and task processors act as a cohesive unit. Reliable data transfers at high transmission rates are prime requirements. Unlike a backplane bus, however, both resource and task processors must contend for equal network access; there is no master/slave protocol as in conventional bus designs. Likewise, the 10M-bps data transfer rate possible using a broadband transmission scheme is tempered by severe signal attenuation (30 dB maximum) as nodes are placed at extreme ends of the 3000′ (914-m) coaxial cable used as the physical link.

The company chose to implement a CSMA/CA (collision avoidance) scheme rather than collision detection for data transfers to provide high throughput during peak periods of use as well as to ensure data integrity. Collision detection schemes like Ethernet suffer degradation in throughput as network traffic increases. These schemes impose random wait states on contending nodes before retransmission is possible.

As the likelihood of collisions increases as traffic increases, this mechanism is used more frequently as retransmissions occur. More significantly, such schemes rely on the occurrence of detectable signal corruptions as signals collide. According to the company, widely separated nodes may have no detectable collisions on the broadband network due to severe signal attenuation.

As implemented on SyFAnet, each node listens twice (carrier sense) before transmitting data packets. The first carrier sense detects whether any node is active on the bus. If the cable is free, an initial carrier burst is sent. The second carrier sense detects a possible collision with another node if the two modulated carrier bursts generate a beat signal with high frequency components. This initial phase requires little overhead since its duration is approximately that encountered with the carrier sense portion of the Ethernet scheme.

(continued on page 52)

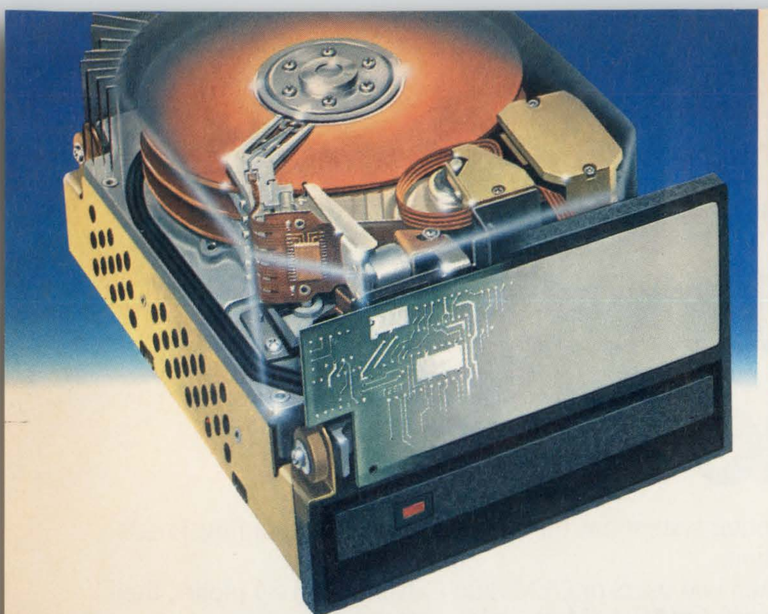
Collision avoidance
(continued from page 51)

If the cable is still free, the transmitting node sends a second carrier burst so that receiving nodes can adjust their automatic gain control circuits to the level of the received signal. A data packet follows after the receiving node responds to its unique address. Further, a reserved time slot added to the packet allows the receiving station to return an acknowledge (or a negative acknowledge) after a CRC check has been performed. This requires that the receiving node's data link controller be able to perform the CRC calculations and construct the response frame "on the fly." Currently, the necessary logic is implemented as discrete logic, but soon will be integrated into a single gate array. As a result, virtual circuit capability is provided in hardware to further reduce software overhead.

Proprietary radio frequency broadband receivers use a center frequency of 48 MHz so that standard television circuits can be used. Furthermore, each transceiver supports four attached processors to further reduce connection costs. Network interface units, resident in either task or resource processors, identify attached processor addresses. They also prepare data packets for transmission. No active components (eg, amplifiers and repeaters) are used to support 254 addressable nodes along a maximum of 3000 cable-ft.

A maximum of 32 task processors are available clustered in a single chassis to support dumb display terminals, or as standalone workstations. Existing communication capabilities available for either configuration include 2780/3780, 360/20-HASP, 3270 and SNA/SDLC PU Type II, and CCITT X.25 protocols. The resource processor manages these resources and also serves as a gateway to other networks. Price and configuration information are available upon request from the company. **Computer Automation, Inc, Commercial Systems Div,** 2181 Dupont Dr, Irvine, CA 92713.

Circle 245



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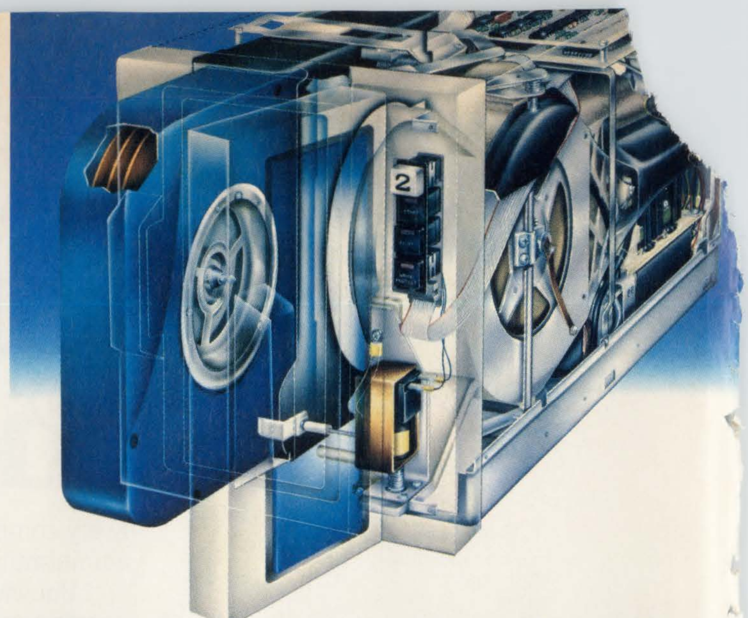
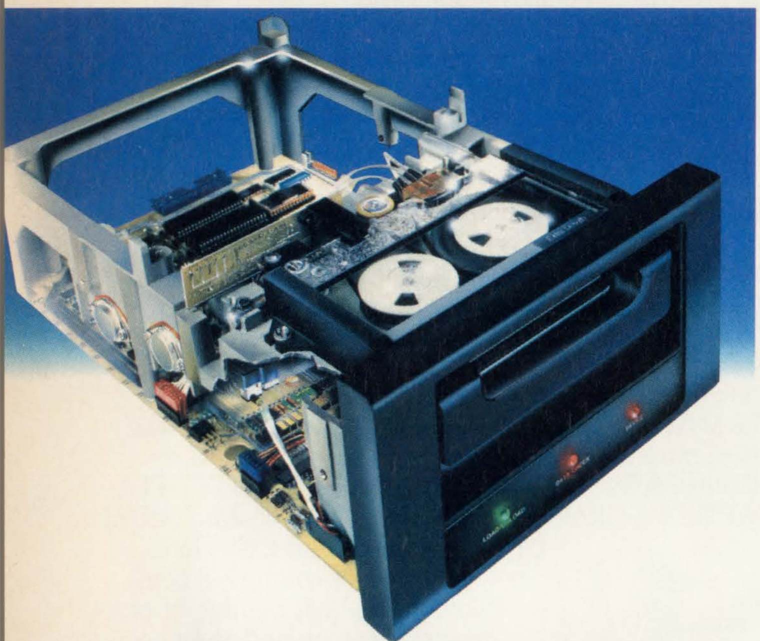
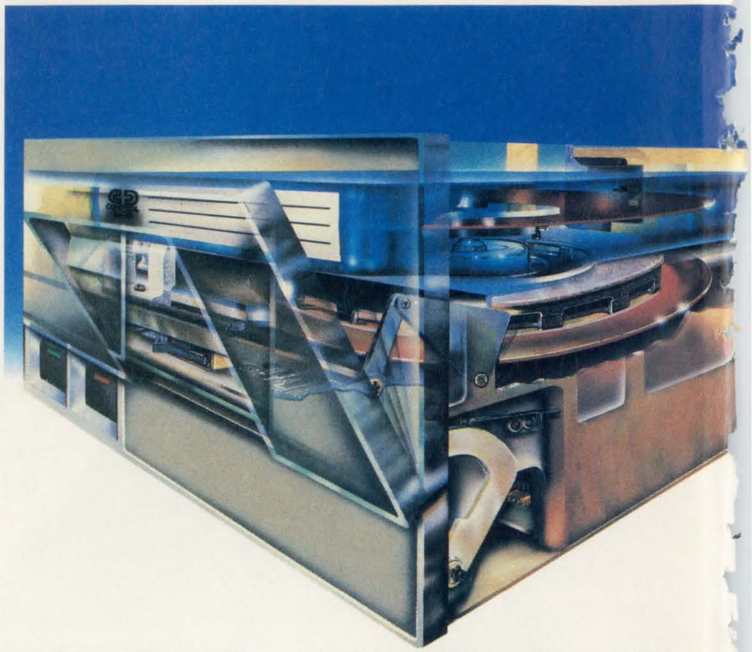


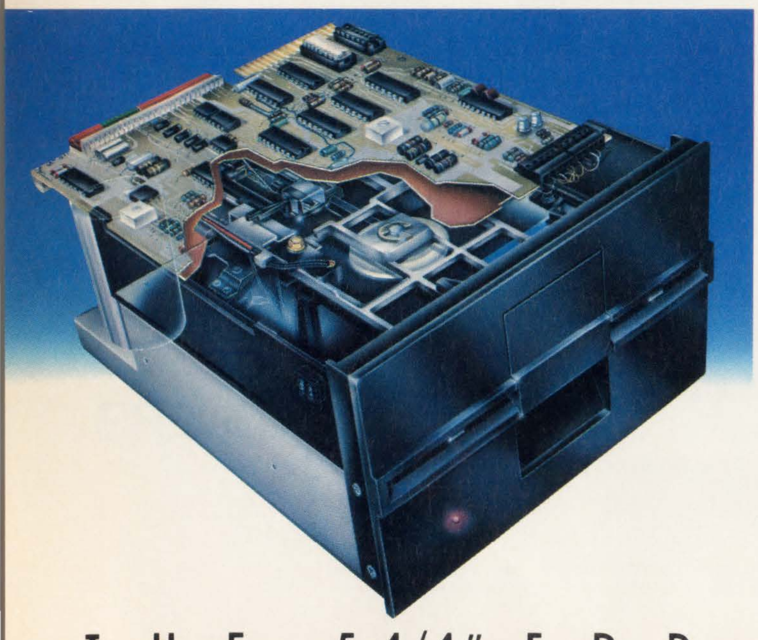
THE RSD



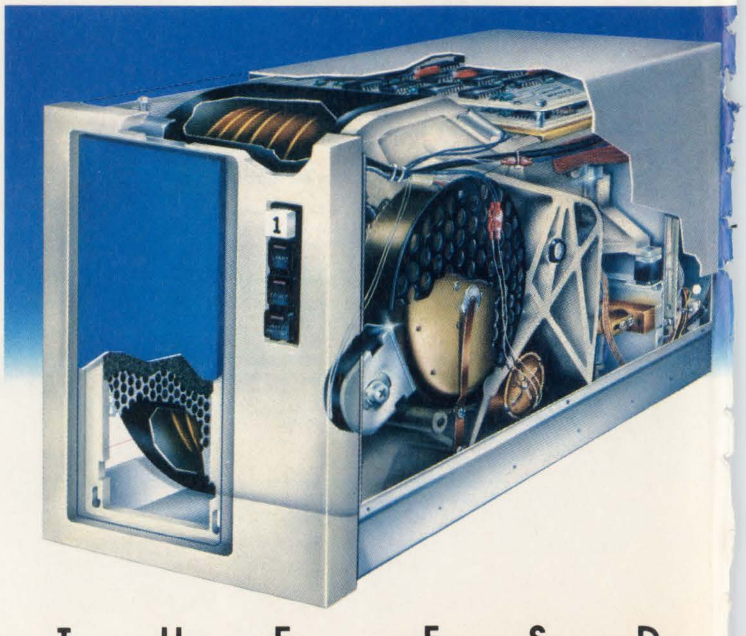
THE SENTINEL



THE LARK™



THE 5-1/4" FDD



THE FSD

CONTROL DATA: AFTER 25 YEARS, STILL THE LEADER IN THE PERFORMING ARTS.

Designing peripherals with exceptional performance is as much an art as a science. We know. We've been doing it since 1962. From the beginning, we've been dedicated to giving you solutions to on-line and back-up storage needs. Example: the Storage Module Drive (SMD) we introduced became the industry standard for removable media disk drives. The SMD is just one of the high-performance products that helped make us the world's leading independent supplier of storage peripherals.

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CONTROL DATA

CIRCLE 32

Schematic capture links with VLSI layout

A dual-display CAE system automates the custom IC layout process along with the logic design process. The SCALDstar from Valid Logic maps the cursor position on the logic schematic (displayed on a monochrome terminal) to the corresponding position on an adjacent color layout display, and vice versa.

Schematic capture and logic design (SCALD) software is the same as that used by the company's SCALD I system for logic design. In addition to the schematic capture and editing programs, the software includes timing verification and simulation programs that produce verified net lists. Layout programs can use these lists for the manufacturing process. This approach allows logic design and layout processes to share information with each other so that the whole design process can proceed with faster feedback between various design stages.

The layout software uses a modified version of the CEASAR layout editor developed at the University of California at Berkeley. Completing the entire design process before running design rule checks (DRCs) and electrical rule checks (ERCs) is not required, however. By incorporating DRC and ERC into the layout process, these checks, which can take a CPU hours on large mainframes, are alleviated.

Even in custom VLSI, many cells are very often replicated. Once such a cell is designed and laid out, it can be checked internally for compliance with all design rules. When this is accomplished, the cell can be replicated, and all the geometries within its boundaries will comply. The only areas that require further checking are those where the cell either connects with, or is directly adjacent to, other circuit elements. For the purposes of rule checking, such a cell can be represented as a hollow rectangle or "doughnut." Only those parts of the cell's geometry that can connect or abut are shown in this doughnut as a boundary area.

In the SCALDstar system, the figure shown on the color display is a doughnut representing circuit elements that have been subjected to DRCs and ERCs and then validated. The elements within the boundary do not require further validation and, for purposes of external connections, can be ignored.

As an extension of this process, circuit elements made up of other elements that have been checked internally need only have their doughnuts subjected to the DRC. This forms yet another, larger doughnut of elements that have been scrutinized. The rule checking takes place at various points in the layout process (eg, when the designer writes the element to a file). Thus, it does not require that a large mainframe devote hours to it at the end of the layout process. Since mistakes are caught and corrected at this stage, there is seldom a need to laboriously search for errors or rerun the entire rule check.

In addition to automation within the layout process, the system can pass information to the logic design process. This transfer can be done, for example, in the form of capacitive loading information that assists the timing verifier programs in estimating propagation and wire delays. Problems encountered in timing verification can then be passed back to the layout process for correction before they proceed too far. This feedback loop lets the timing verifier focus on the resulting physical design characteristics for final verification.

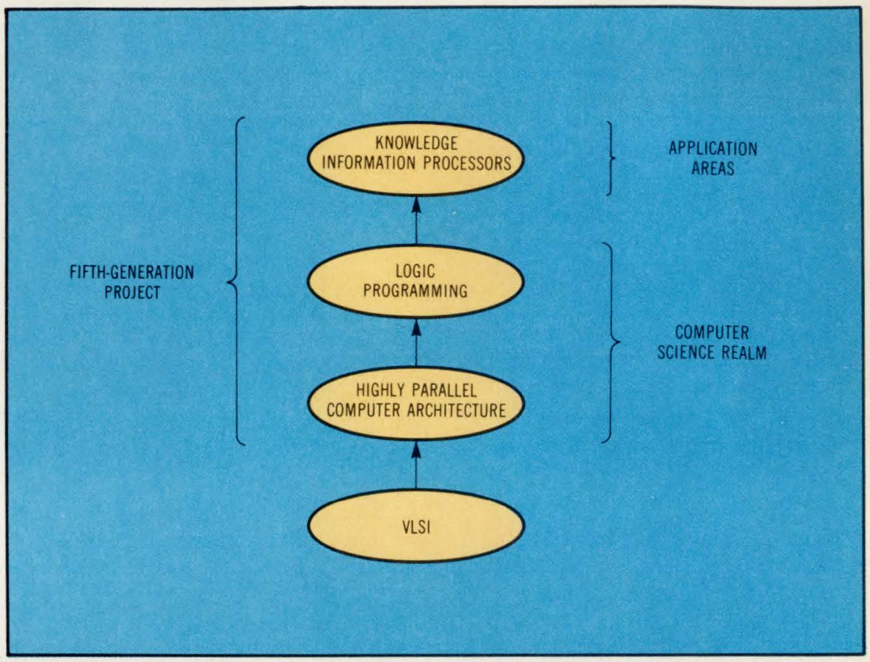
Each element in the SCALD data base thus consists of four elements: the logic schematic; the actual graphic layout information; the pin connection information; and the doughnuts created by rule checking. Timing verification information is associated with the layout data and the doughnuts, and can be updated as the design approaches its final form. **Valid Logic Systems, Inc,** 650 N Mary Ave, Sunnyvale, CA 94086. **Circle 246**

Radical approach for future CPU design

Today's computers are mainly number crunchers. Computer scientists, however, believe that future computers will be human problem solvers behaving much like doctors, lawyers, and engineers. To become a problem solver, the computer must be programmed to possess knowledge about the subject and infer answers to problems as a human would.

Development of a knowledge based processor has been the elusive goal of the artificial intelligence community for more than 20 years. A few "expert systems" have been developed for limited applications. However, these are confined to the same computer architecture and processing tools that mark the rest of the computer population (*Computer Design,* Apr 21, 1983, p 65-76). To develop a new generation of knowledge based systems, computer scientists agree that a new thinking process for designing computers has to prevail. For that to happen, a concerted effort on the part of government, academia, and industry is required. Such programs have shown up on both sides of the Pacific Ocean—Japan's Fifth-Generation Computer Project and this country's Microelectronics and Computer Technology (MCT) Corp. MCT consists of 12 high tech companies and is still writing its charter. On the other hand, Japan's effort is, as usual, a coordinated government-backed project to develop new computer technology for the 1990s.

At a recent week-long science symposium, Kazuhiro Fuchi, director of the Institute for New Generation Computer Technology (ICOT) Research Center in Tokyo, discussed the theoretical issues for achieving the goals of the fifth-generation machines. ICOT, made up of some 80 researchers from the labs of such companies as Fujitsu, Hitachi, NEC, Toshiba, and Sharp, is conducting the Japanese project. ICOT's idea of fifth-generation machines is to develop a new information processing technology composed of elements from diverse scientific fields. These fields include behaviorial science, linguistics, psychology, mathematical logic, and neurophysiology.



While a knowledge information processor is highly dependent on clever VLSI design, intensified research for an efficient, highly parallel computer architecture and logic programming is at the core of fifth-generation computer development.

Fuchi says that developments over the past 10 years in these various fields have recently been found to be closely related. While interdependent efforts have not reached the stage of practical application to computer technology, Fuchi contends that they inspire the feeling that information processing technology will be integrally reorganized in the near future. This means that the way people think about computers and the way computers are designed will change dramatically.

Principles of the internal structure of computers have not changed much since Von Neumann synthesized the physiology of logic elements that form the basis of today's computers. But as software programs advance beyond human comprehension, and VLSI chips evolve at an exponentially increasing rate, a new overall viewpoint of computer architecture has to emerge. Such modern approaches as associative processing, parallel processing, and variable structures and architectures based on high-level languages have all been tried on an individual basis. While each approach performs well in individual applications, a new implied theory is needed to organically position and employ each approach. This theory should focus on both hardware structure and programming.

So far, experimental machines for parallel processing and associative processing have been built to provide higher performance capabilities and more sophisticated functions. These, however, are very difficult to program despite certain unique characteristics of the systems in some cases. Fuchi believes that this situation is about to change. Dataflow type architecture is becoming very attractive because the architecture describes the computing processes in terms of the flow of data rather than by the conventional approach, which centers around control logic. In this architecture, parallel operations are described along with the flow of data.

(continued on page 64)

The World's Most Elegant Microprocessor Family is Banishing Current Benchmarks to Computer History.

Be advised: the NS16000 family is establishing all new benchmarks for 8-, 16-, and 32-bit microprocessors.

Here is proof beyond doubt that any NS16000-based product will outperform any other microprocessor-based product.

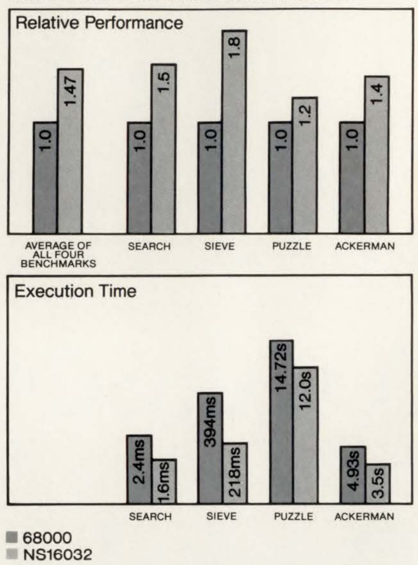
Of course, comparing the NS16000 family and the microprocessors your competition is banking on is difficult—perhaps even irrelevant—because the NS16000 family is, fundamentally, much more advanced.

No other commercial processor (micro, mini *or* mainframe) is designed to fully support the use of high-level languages. All members of the NS16000 family of CPUs,[1] however, feature not only 32-bit internal architecture, but also a high degree of regularity in the arrangement and use of their 32-bit registers. Data can be read or written 1, 8, 16, or 32 bits at a time, as sophisticated programs require, and transfers from one register to another are not restricted.

Moreover, the symmetrical instruction set of the NS16000 CPUs includes over 100 genuine two-operand instruction types, but avoids special-case instructions that compilers cannot use. All instructions can be used with the addressing modes common to most microprocessors (register, immediate, absolute, and register relative), as well as with powerful HLL-oriented modes that only the NS16000 offers: top-of-stack, scaled indexing, memory relative, and external. And any operand length and any general-purpose register may be used with any mode.

The combination of these virtues makes it possible to write especially lean high-level language programs on NS16000-based systems. The simplicity with which a programmer can implement a compiler, for instance, is matched only by the compiler's increased speed of execution. In effect, the dream of being able to pack the enviable working environment and performance of a large computer into a microprocessor has become reality.

HIGH-LEVEL LANGUAGE COMPARISONS[2]



Putting large-computer performance into a microprocessor is further advanced through the implementation of the NS16000's Demand Paged Virtual Memory —a strategy equivalent to that used in such systems as the VAX-11 series and all present IBM mainframes.

With an architecture that supports uniform addressing, the NS16000 is the first commercial microprocessor able to feature Demand Paged Virtual Memory as a means of solving large-memory-management problems. As a result, an NS16000-based system, blessed with this completely flexible memory configuration, can maximize the use of its physical and virtual memory resources and achieve a level of performance heretofore unrealized.

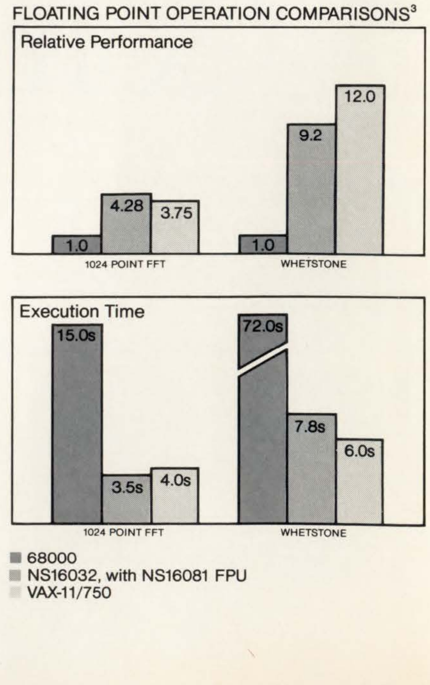
With the NS16082 Memory Management Unit (MMU), only the information most recently used is kept in RAM: other information is swapped in and out from mass storage, as needed. Consequently, each programmer, each program, each task has access to a uniform addressing space of 16 Mbytes simultaneously and independently, without reservation or special exception. (And more efficiently than on any other commercial processor—micro, mini, or mainframe.)

Among the reasons for the MMU's prowess is its support of a *two-level* page-table translation, whose process is speeded up by an associative on-chip cache. Utilizing a very fast Least-Recently-Used (LRU) algorithm and a powerful "referenced bit," the NS16082 MMU achieves a translation cache hit rate of over 98 percent.

The NS16081 Floating Point Unit (FPU) extends the NS16000 instruction set with very high-speed floating-point operations for both single- and double-precision IEEE operands.

Designing the FPU into a system allows programmers to treat floating-point numbers as they would any other data types, and to use any of the addressing modes to reference them. For example, the scaled index mode permits an array of floating-point data elements to be addressed by its logical index, rather than its physical address. The power this can add to a system makes it especially applicable for graphics and engineering work-stations.

FLOATING POINT OPERATION COMPARISONS[3]

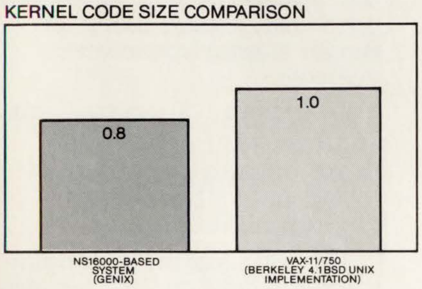


With the introduction of National's proprietary GENIX™ operating system, even the advantages of using UNIX® on a large computer have been ported to the NS16000 microprocessor family.

GENIX is an elegant implementation of the proven Berkeley 4.1 bsd version of UNIX. Created in-house, to facilitate the development of software for NS16000-based applications, it is the first UNIX operating system to support Demand Paged Virtual Memory in a microprocessor.

Here, then, is a demonstration not only of the pure functionality of the NS16000 family architecture, but of the large-computer-like results now possible on a microprocessor-based system using GENIX.

KERNEL CODE SIZE COMPARISON



When you consider applications for the NS16000 microprocessor family—from elegant personal and business computers, to graphics work-stations, to industrial control systems—keep in mind that:

1. The NS16032 CPU and the NS16201 TCU are in production now.
2. The NS16082 MMU, the NS16081 FPU, and the NS16202 ICU are being sampled now.
3. Evaluation tools are available now.
4. Development tools are available now.
5. Training classes are in progress now.
6. Third-party software for the family is available now and increasing daily.
7. The software you write now will work *without modification* if you move your product line from one NS16000 CPU to another in the future.

   Similarly, the optional use of the NS16000's MMU and FPU slave processors—integral parts of the NS16000 architecture—will allow you to determine price/performance trade-offs while preserving your initial software investment.
8. Only the NS16000 family can make it possible for you to put a large-computer-like product on the market today—at microprocessor prices.

Footnotes:

1.
The NS16032 CPU, the first of the NS16000 CPUs, has a 16-bit-wide data path to memory and 32-bit internal architecture. Before the end of this year, CPUs implementing the same 32-bit internal architecture, but with 8- and 32-bit-wide data paths to memory will also be available, to allow maximum price/performance flexibility within your product line.

2.
Results for the 68000 were taken from *Computer Architecture News*, Vol. 10, No. 4, June 1982, pp. 17-28. The 68000 was run at 10MHz, with no Wait States. Source programs in Pascal.

Results for the NS16032 were obtained on a DB16000 at 10MHz, with no Wait States. Source programs in Pascal. All variable sizes are 32-bit.

3.
Results for the 68000 were obtained on a SUN System at 10MHz, with no Wait States, using Motorola's ROM-based floating point subroutine package.

Results for the NS16032, utilizing the NS16081 FPU, were obtained on a DB16000 at 10MHz, with no Wait States. IEEE floating point, variable sizes.

Results for the VAX-11/750 were obtained without using floating point accelerator.

NS16000

Elegance is everything.

See it.

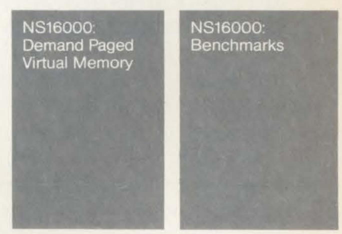
The NS16000 microprocessor family will be on exhibition at WESCON.

Talk with us.

Please call the National Sales Representative nearest you for more information, and the answers to your questions. Ask to meet with one of our Field Applications Engineers, too. Or, circle the number below.

Read about it.

You haven't heard the last word on the NS16000 microprocessor family yet. In the meantime, you may want to further your understanding of what we've accomplished by requesting copies of *NS16000: Demand Paged Virtual Memory* and *NS16000: Benchmarks.*



National Semiconductor

MICROCOMPUTER SYSTEMS DIVISION

CIRCLE 34

If you don't find the logic
you probably don't need

Meet the logic analyzer family that spans a wide spectrum in design. It's a family you can rely on in hardware design, software test and debug and even system performance analysis. One that's equally at home testing and troubleshooting low-cost single processor designs or sophisticated multiprocessor systems.

You can choose from a wide selection of different logic analyzer configurations with HP. And when you do, you'll have an analysis solution that can help accelerate your design cycles...and speed your products to market.

The 1630A and 1630D...for confidence in tackling the day-to-day logic problems.

Choose one of these logic analyzers and you'll have the combined power of timing, state, and software performance analysis in one convenient, low-cost instrument. At just $8,600*, the 1630A gives you 35 channels of state/performance analysis (to 25 MHz), or 8 channels of timing (to 100 MHz). In the interactive measurement mode, it delivers 27 channels of state and 8 timing.

For $10,630*, the 1630D offers 43 channels of state/performance analysis or 16 timing. In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing.

As your primary tool in hardware test and debug, the 1630 provides new triggering power to help you isolate the source of timing errors. This includes pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. This is the capability that helps you quickly solve difficult hardware problems such as timing errors, transient effects and handshake malfunctions.

Use the 1630 in software development and integration phases and you have sequencing, triggering, store qualification, and sequence restart power to isolate targeted areas of code and view just the measurement information you desire.

To optimize your system performance, the 1630 gives you a nonintrusive view of system software in action. One that lets you analyze system activity at the level of procedures and tasks instead of the instruction level. Histogram displays make it easy to spot software bottlenecks and inefficiencies. The result can be improved system performance, and a more competitive product...with minimal additional design effort.

The 1630 also gives you interactive measurement capability for greatly enhanced analysis power. The ability to cross arm and trigger between state and timing analyzers helps you get to the problem source quickly when the difficulty could be either a hardware or software malfunction.

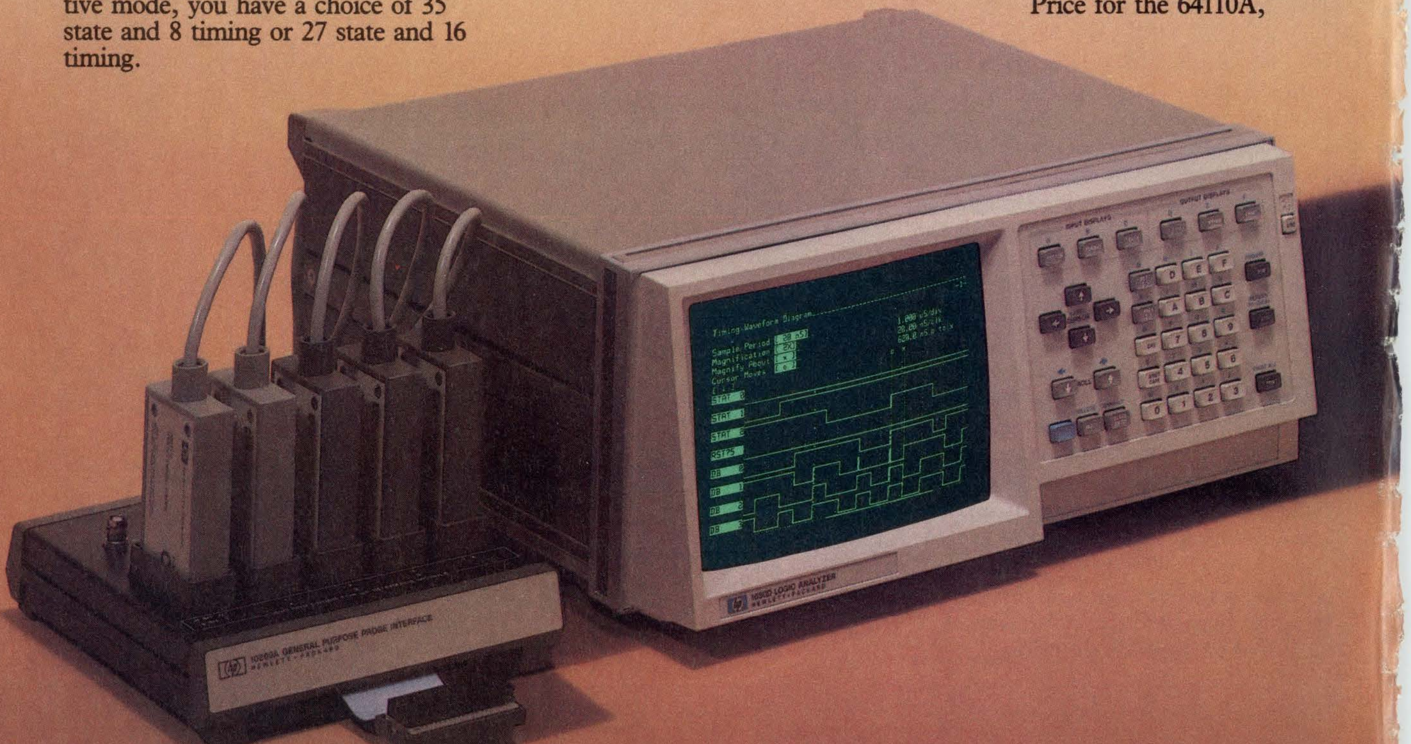
Throughout the development cycle, you'll find the 1630 easy to use. That's because menus simplify operation. Label assignments let you view results in your system's terminology. And inverse assembly, via low-cost peripherals, displays listings in familiar target microprocessor mnemonics.

The 64110A...a configurable analyzer that can handle those complex problems found in multiprocessor environments.

This logic analyzer is, in reality, a number of different analyzers, depending on how you configure it. For example, it can be a standalone timing analyzer with 8 or 16 channels.

It can also be a standalone state analyzer with up to 120 channels. You can combine timing and state with performance overview. Or, combine multiple state or timing analyzers in the same station.

Price for the 64110A,



CPU design
(continued from page 58)

In conjunction with parallel processing is the concept of functional programming. Data-flow machines and functional programming provide possibilities for developing the "inference machine," considered to be the new type of computer, or the true form of a computer, according to Fuchi.

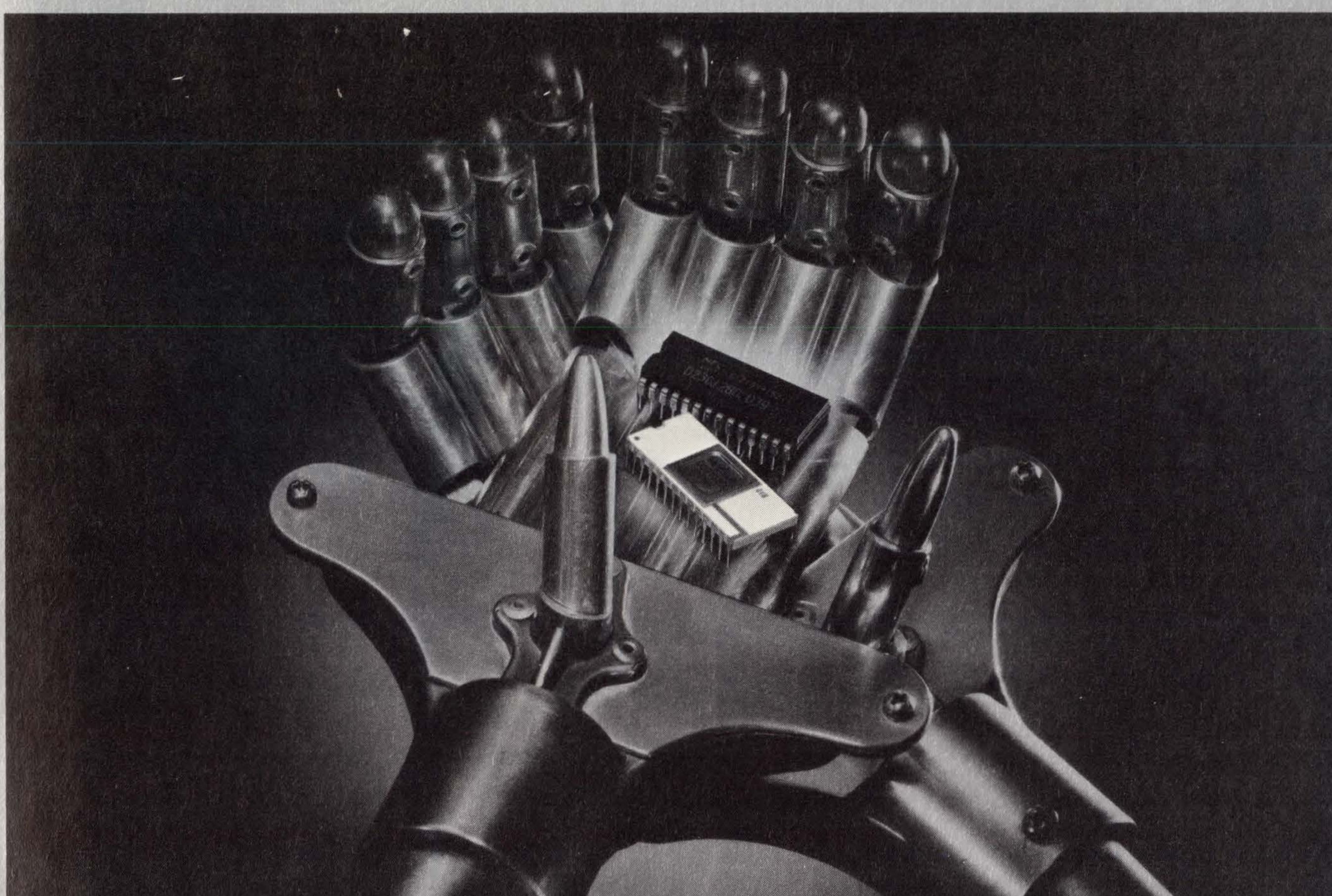
Functional programming and predicate calculus-type programming have at their core the use of a certain form of logic itself as the programming language. The two types use a formal specification language. Formal specifications may be regarded as a type of highly abstract program that can be converted and made concrete in accordance with system requirements. Making the conversion in the same language could be achieved by using actual logic blocks. This, according to Fuchi, will alleviate the problem of verifying programs. One reason that program verification is difficult is the low level of languages currently in use. For this reason, other programmers are slow to accept it. This phenomenon can be traced to the existing antiquated computer architecture. So, one cause for the "software crisis" lies in the very system of existing computers.

Verifying that programs are written correctly involves nothing more than verifying that the meanings of two statements are identical. Stated another way, it is simply a problem in semantics. While some current artificial intelligence languages may have simplified semantics, the languages actually present considerable difficulties. Fuchi says that, while the syntax of artificial intelligence languages often appears general and simple, the meanings of the words used within these syntaxes are quite specific and complex. This parallels the difficulties encountered in semantics of natural languages.

Fuchi contends that these difficulties reinforce the need for innovative programming styles and languages to support them. He says that while conventional languages are dedicated to the Von Neumann-type machine and are therefore semantically complex, logic-type languages with simple semantics infer that logic-type machines will also be simple. Thus, he calls logic programming "the missing link between knowledge engineering and parallel computer architectures."

The first task of the Fifth-Generation Computer Project is to develop the Personal Sequential Inference (PSI) machine that in effect, is a LISP machine using Pro-Log programming concepts. It will provide user interface facilities comparable to the LISP machines, have up to 2M bytes of memory, and exhibit a performance of 20k Pro-Log procedure calls per second. Following will be a more powerful and better-designed
(continued on page 66)

 CIRCLE 36



CPU design

(continued from page 64)

super PSI. In a parallel effort, a logic based database unit will be built and interfaced to the PSI machines.

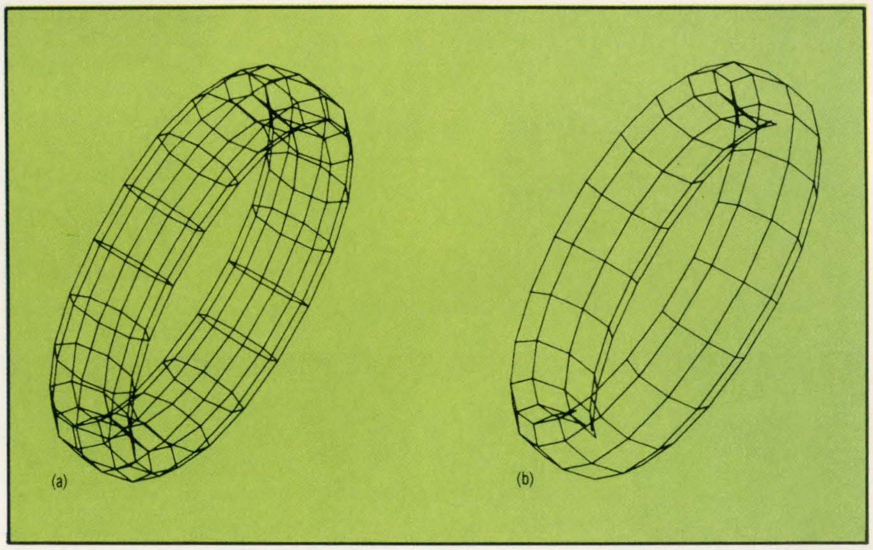
For the long range, a fifth-generation system is scheduled to have the following functions: problem-solving and interface, knowledge based management, and an intelligent interface. Targeted for this machine, which will be composed of 1000 processing elements of CPU and memory, is a performance of 100M- to 1G- procedure calls per second. The knowledge based management system, corresponding to today's disk and file systems, is expected to have a capacity of up to 1000G bytes. The intelligent interface system is supposed to contain a vocabulary of up to 10,000 words including 2000 grammar rules. This system will ensure a 99% accuracy in syntactic analysis of written natural language. In addition, a speech recognition system will be able to recognize up to 50,000 words with 95% accuracy, while a graphics system will be able to store up to 10,000 pieces of graphics and image information.

These ambitious plans are, of course, for a research machine and do not constitute feasibility for commercial applications until well into the next decade.

—Nicolas Mokhoff, Senior Editor

Image transform adjusts hidden surfaces

Sophisticated 3-D mathematical models can nearly mirror the physical characteristics of real-world objects. Yet, graphical display limitations have hampered their use in computer simulation, animation, and computer-assisted design. However, Manufacturing Consultants and Services' recent enhancements to the Anvil 4000 mechanical CAD/CAM system point to the possibility of integrating hidden feature removal into the 3-D model itself. On the other hand, Megatek Corp's Template® graphics package focuses on feature removal as part of the image transformation process.



Two toroids generated by the Template graphics package illustrate the benefit of hidden line removal for complex 3-D objects. Note that eliminating backface polygons (b) removes the ambiguity of orientation found in (a).

Although Template is a graphics subroutine package and Anvil 4000 a fully developed application, both use 3-D mathematical models for image transformations. Real-world objects are defined in terms of a 3-axis coordinate system (ie, length, width, and depth) as well as attributes that describe these objects as unique entities (eg, four connected line segments form a rectangle). Once an object has been described in terms of an absolute coordinate system (independent of view orientation), an image of this object is generated with vector or raster coordinates. This display list is what a user sees on a display terminal. Any changes the user makes to the image do not alter the mathematical model. In other words, vector endpoints (or raster coordinates) are changed, not the coordinates described in the mathematical model.

Template can only eliminate hidden features once the user defines visible ones. Working with either raster coordinates or vector endpoints, the user transforms the image to the desired shape and attaches attributes to polygon faces that make up the image. Part of the attribute information describes the direction in which polygon vertices are defined (clockwise/counter clockwise). Normal vectors to each polygon face are automatically calculated. Users then have a series of options that eliminate all (or a selected portion) of polygon faces pointing into the screen. This backface elimination process thus acts as a filter after image transformation occurs. A selective erase option also allows users to manually delete features from selected views (eg, menus and dimensions).

Since each display session does not affect the 3-D model, changes can be quickly processed locally without accessing the central data base where the model is kept. Changes to the model usually require that new display lists be generated and displayed again on the user's terminal. As a result, system overhead increases, according to Bob Bruns, Template development manager.

However, according to Anvil 4000 development director, Ross Stoutenborough, multiple display lists must be stored if hidden features have been defined for many views. In fact, Template does store these lists as metafiles for direct viewing, or as input for further image

(continued on page 70)

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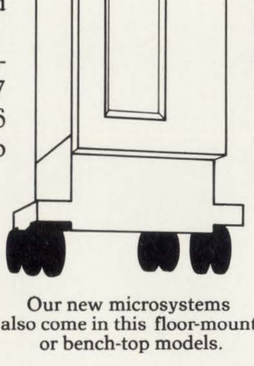

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*A600+ microsystem component, 128Kb memory, box, Winchester disc.

Prices are U.S.A. list in OEM quantities of 100 and include integrated peripherals, one interface card, RTE-A execute and 512Kb of memory for Micro 26 and Micro 27. Micro 29 includes 768Kb of memory.

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1 MIPS for
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3 MIPS, plus floating point hardware and microprogramming, for $16,350
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1 MIPS, plus floating point hardware and microprogramming, for $13,140
Whatever the level of performance you pick, it fits in this little 7" x 19" x 25.5" package.
CIRCLE 38

Image transform
(continued from page 66)

transformations. Memory requirements further increase since the 3-D model must be saved at the end of each session, according to Stoutenborough.

To reduce memory requirements, Anvil 4000 maintains graphical attributes within the 3-D model itself. Thus, 3-D coordinates are used in place of the 2-D coordinates typically used for display lists. Physical characteristics (ie, height, width, depth) are retained. Likewise, geometrical relationships and textual information are stored. Even with the 3-D mathematical model, implementations like Template lose such attribute information when display lists are generated since they deal in 2-D coordinates.

Associating display attributes with the 3-D model allows polygon faces to hide all (or a portion) of other polygons without graphical computations. Anvil 4000 knows each view is to be displayed, and changes in one view do not impact the display of other views. Rather than work with polygon faces that approximate the actual object (a la Template), users manipulate the mathematical definition of that object. As with Template, users can select surfaces to hide other surfaces, or explicitly declare features to be hidden in a view. However, surfaces can also be partially hidden because the system is aware of the geometrics involved.

Since the hidden surface facility works on the graphics data base, display lists viewed at the terminal are not saved. Images are regenerated at the start of every session because part of the graphics data base is loaded locally at the terminal. Only state information (eg, changed attributes) contained in that data base is stored when the session ends—display lists disappear altogether.

Although such state information is not associated with the Template 3-D model, Bruns claims that application developers are free to implement such relationships when they use Template subroutines. **Manufacturing and Consulting Services, Inc**, 17942 Cowan, Irvine, CA 92714; **Megatek Corp**, 3985 Sorrento Valley Blvd, San Diego, CA 92121.

—Joseph Aseo, Field Editor

Circle 247—Manufacturing and Consulting Services, Inc
Circle 248—Megatek Corp

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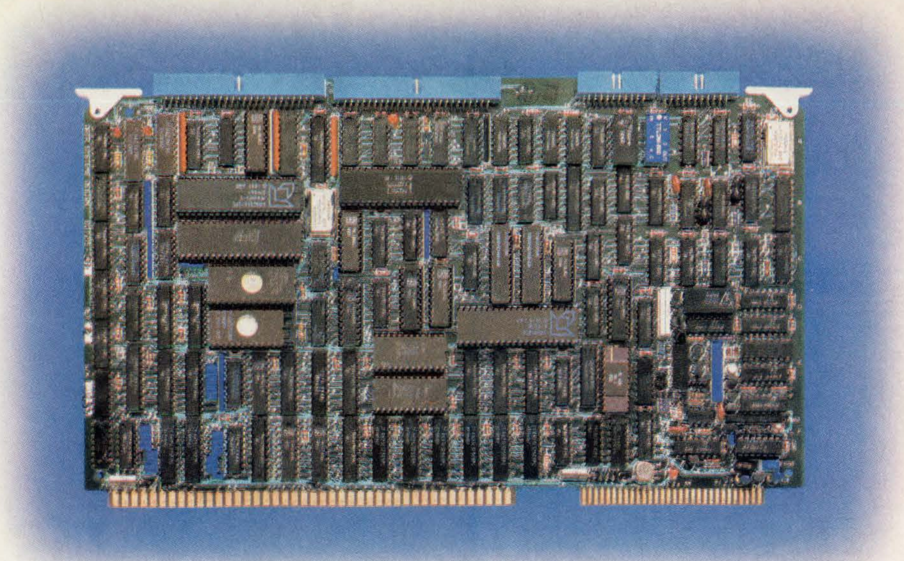
CIRCLE 39

ONE SLOT SHOPPING.



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DATA SYSTEMS DESIGN

CIRCLE 41

CP/M heads for the big time

A Z80 chip, a custom gate array, and interface software from Virtual Microsystems provide a CP/M coprocessor for users of DEC's LSI-11/23 based computers. The combination gives users access to the many available CP/M programs on the market. Both the Z80A and the gate array are packaged in a 40-pin DIP (the z-Chip), which is inserted in the floating point chip socket on the LSI-11/23, Micro-11, J-11, or DEC Professional Computer processor board.

Because of the proprietary gate array, the Z80 appears like an ordinary DEC floating point chip to the LSI-11 operating system. This design also lets the Z80 address system memory. In addition, the Z80 runs at its full 4 MHz, taking its timing signals from the system. When using the z-Chip with systems that only have one floating point chip socket, such as the Professional, the floating point option is unavailable. On LSI-11s with two sockets, however, both can run simultaneously.

The software package, called The Bridge, has two functions. Without the z-Chip, it acts as an 8080 simulator, running 8080 machine language programs 4 to 10 times slower than a 1-MHz 8080 would. If the z-Chip is present, the package runs programs at almost the full 4-MHz speed of the Z80.

As a simulator, the software package allows the sophisticated debugging and tracing utilities, which are native to the LSI-11 system, to be used in developing 8080 or Z80 based software. In conjunction with the z-Chip, it provides access to popular word processing and spreadsheet programs, along with access to the large-capacity hard disks and sophisticated peripherals of the LSI system.

DEC's recently introduced single-user systems do not yet have a large base of applications software for business or professional use. Thus, the z-Chip provides the system integrator with added functionality when configuring systems. It is the lowest priced (and least capable) of VMI's line of add-ons, which give DEC, Data General, and Prime minicomputer users access to 8-bit microcomputer programs and response times.

The company's z-Boards, which interface with Q-bus and Unibus machines, have four Z80s, each with 64K RAM. These boards also provide single-user response times and access to 8-bit software without loading the host operating system.

Similar z-Boards are also available for Data General's MV series (4000, 6000, 8000, and 10000), as well as the C and Nova series. The company has also signed an agreement with Prime Computer of Natick, Mass, to product boards and software to work with Prime's machines.

This configuration does more than provide a ready source of existing software for DEC's single-user systems. With it, OEMs and system configurers can give users large minicomputer power with microcomputer response and friendliness. Even though microcomputer software is significantly less expensive than equivalent programs written for minis, it has many useful features. Moreover, this software also alleviates the problem that information system managers often have with microcomputers—system incompatibility.

Since the system is intimately connected to the minicomputer and uses its storage and printers, the problems of incompatible disk formats or expensive separate printers, modems, and support are eliminated. On the other hand, spreadsheets, word processors, and other, essentially 8-bit utilities can run without loading down the mini's 16-bit operating system.

With the Bridge software included, the z-Chip is list priced from $495 for the DEC Pro to $695 for the LSI-11/23, with OEM discounts available. The Bridge software is separately priced at $1000 to $3500, depending on configuration; z-Boards are priced near $1000 per user. **Virtual Microsystems,** 2150 Shattuck Ave, Berkeley, CA 94704. **Circle 249**

DATA COMMUNICATIONS

Terminals cater to distinct applications

As AT&T divests its regulated business from the unregulated side, Bell's competitors can expect a steady stream of products for the home and office markets from its unregulated side. In anticipation of the breaking up of the Bell System, AT&T planners have orchestrated product introductions to fall within the timeframe stipulated by the antitrust settlement.

Thus, to no one's surprise, Teletype Corp, a subsidiary of Western Electric, used this year's May 16-19 National Computer Conference forum to toll its bell. The company announced four terminals that are expected to be available later this year. The terminals include a dot-mapped graphics display unit, two different asynchronous interactive units, and an IBM 3270-compatible terminal with a 5¼" diskette controller.

Long identified with the Teletypewriter Exchange System (TWX), Teletype has not introduced a new product line since 1975 when it came out with the 4540 and 4400 dumb terminals. These, however, were available only to users who signed up for AT&T's regulated business transmission service. With its chains broken, the company has now unleashed an intelligent dot-mapped display terminal. Driven by Bellmac-32 (the 32-bit microprocessor from Bell Laboratories), the terminal uses the Unix operating system for its application programs.

This powerful combination allows programmers to simultaneously download multiple software programs

(continued on page 74)

Graphics display terminal
(continued from page 73)

from a host computer. The screen can then be divided into up to six windows of varying lengths and widths, allowing programmers to develop different portions of a single program, or multiple programs, in each window. Various editions of the same program can be displayed concurrently with both old and new editions of any program accessible during editing. The 5620 terminal can compile one program while users continue working on another. Thus, users can work on one program, display a second, and have the terminal execute a third. In this way, data can easily be compared. Users can also examine two sets of files at the same time, from more than one data base.

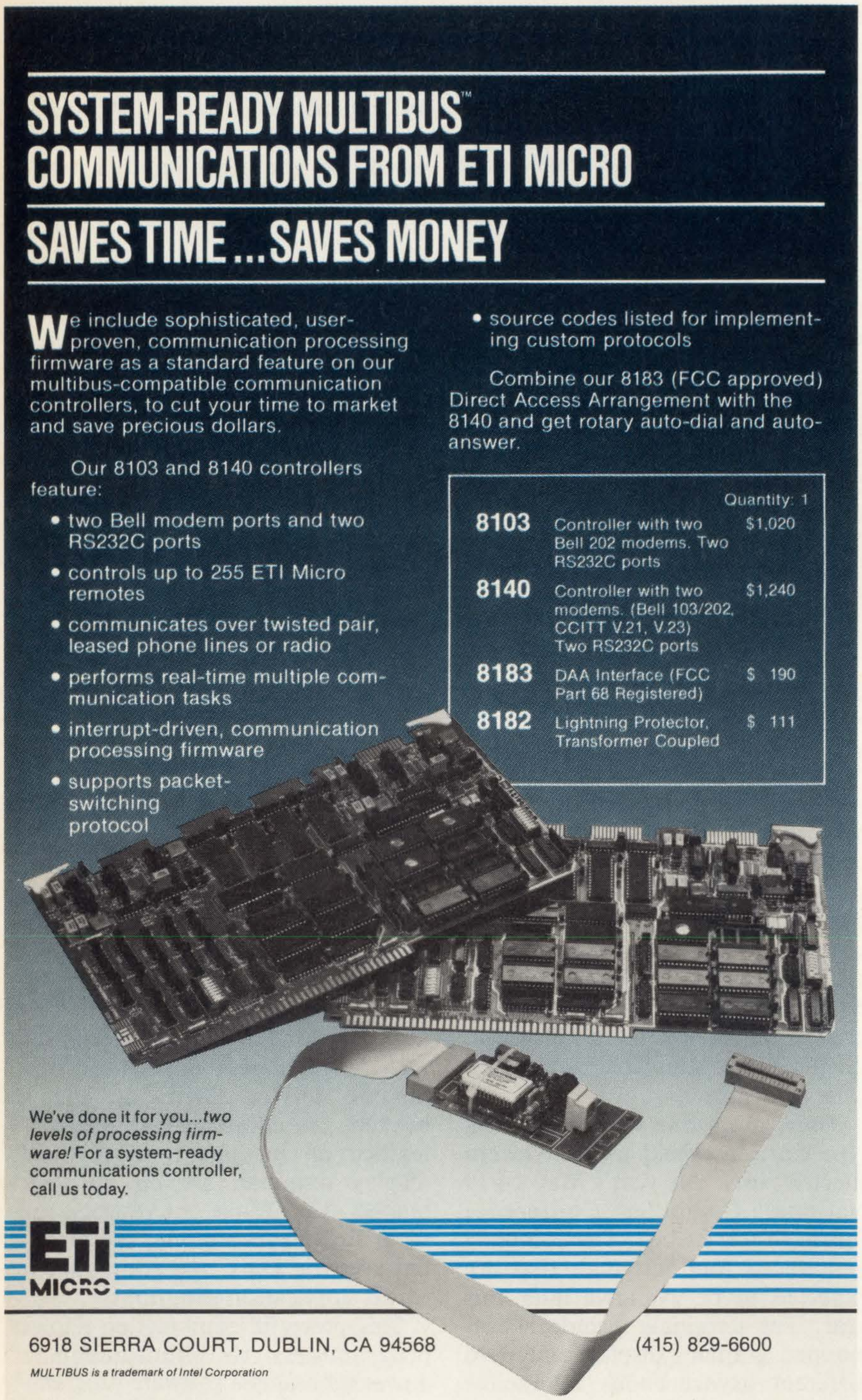
Data are displayed on a 800-dot x 1024-scan line 15"- diagonal screen that allows both graphics and line drawings to be viewed to a 100-dot/in resolution. The detachable low-profile keyboard has eight programmable function keys for different fonts and for cursor control. An optional mouse for controlling the cursor is also available.

Data are manipulated using internal 256K-byte RAM and 48K-byte ROM. Baud rates for transmission are key selectable and range from 300 to 19k bps. The unit is priced at $6115. The 5620 is intended, not as a standalone device, but rather to run with hosts under the Unix operating system Release V. This latest version of Unix should be available when the terminals are shipped in the last quarter of this year.

Complementing the 5620 are three terminals to be used in conjunction with host computers. The 5410 is an asynchronous terminal for applications in timesharing, inquiry response, data retrieval, and software development. It is a buffered version of the 5410. Both terminals are based on the ANSI 3.64 specifications for conversational terminals. The 5410 operates in a character-at-a-time mode while the 5420 has a buffer memory for 72 lines of display. This gives the user four modes for manipulating the data into a desired display.

Furthermore, the user can scan all 72 lines of available memory in the scroll mode. The horizontal split screen mode partitions the display into fixed and scrolling regions. The windowing mode divides the display into as many as four addressable windows that can look into the display's memory. Finally, the page mode splits memory into three distinct 24-line pages that emulate three exclusive terminals.

The 5420 display can be changed from 80 to 132 columns to meet the needs of applications such as accounting spreadsheets and linedrawn graphics. Up to eight
(continued on page 76)



 CIRCLE 42

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Graphics display terminal
(continued from page 74)
system-defined function keys can be downloaded from a host, and up to eight other keys can be defined locally and stored in a nonvolatile memory. All keys are defined by an 80-character string and labeled as 16-character words on lines 26 and 27 of the display. Labels change as key functions are altered. A standard bidirectional buffered printer port accommodates local and online printing. The 5420 lists for $1495. The less costly ($995) 5410 has a character set that consists of the standard 128 ASCII characters plus a 96-line drawing graphics and special symbols capacity.

All the terminals feature nonglare displays with tilt and brightness controls. The keyboards meet the 30-mm DIN height specification. All keyboards can be stored on a shelf under the display, giving the operator more working space.

The fourth terminal is the company's answer to compatibility with IBM's computers. The 5540 is compatible with IBM's 3270 asynchronous terminal. It supports SNA/SDLC protocols as well as BSC line protocols. The terminal can replace existing SNA terminals without host software modifications. A 5¼" floppy disk drive is included for controller programming. The terminal contains a dual-microprocessor based controller for clustering up to 32 devices. Upgrading from BSC to SNA/SDLC is done by changing diskettes. The 5540 is also compatible with Teletype's 4540 displays and printers.

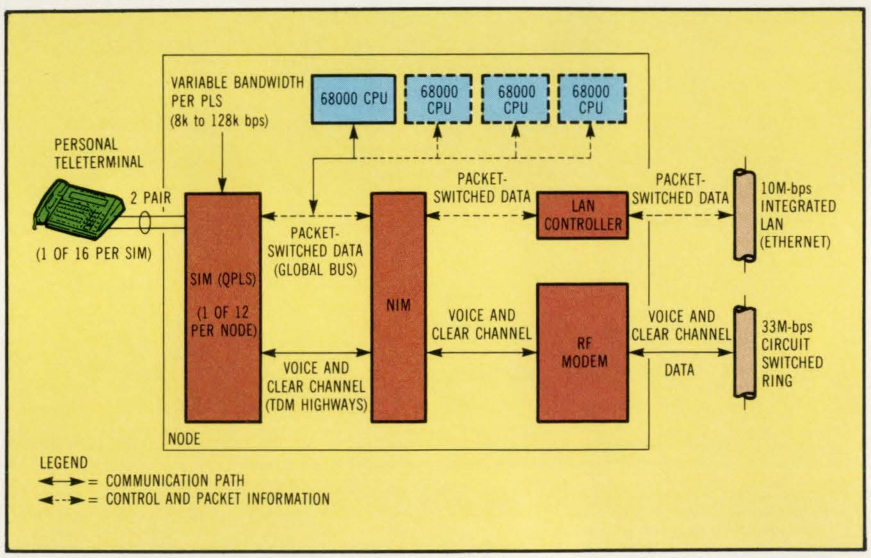
A lightweight low-profile keyboard with 3270-like key layouts includes 24 programmable function keys, an insert mode, an erase-to-end-of-file function, and a primary stroke capability on often-used keys. The list prices of the 5540 controllers range from $4500 to $11,500. The smaller 5548 display with the standard 24 programmable function keys lists for $1633. The optional lightpen, compatible with the 5540 displays, lists for $417. A typical cluster configuration, consisting of one controller, four displays, and one character printer has a list price of $13,234 while a controller, 24 displays, and two quiet-line printers together list for $61,882. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60077. **Circle 250**

Information system inherits PBX and LAN traits

Simultaneous voice and data transmissions are promised for a distributed communication system that combines per-line switching of private branch exchanges (PBX) and packet switching of local area networks (LAN). The Rose information exchange from CXC Corp has the flexibility to handle anywhere from 192 to 50,000 subscribers on multiple processing nodes. Furthermore, the system is claimed to be the first to dynamically allocate bandwidth from the user's terminal or telephone to the long haul network.

By borrowing extensively from both PBX and LAN technology, the Rose exchange seeks to offer the advantages of both without being hindered by the limitations of either. Per-line switching present in PBXs is adept at handling fixed numbers of subscribers by using cross-point arrays (implemented currently as integrated circuits or stored programs). However, subscribers must be geographically concentrated due to the PBX's central location. Likewise, expansion requires installing several fixed capacity PBXs since incremental growth cannot be accommodated.

To extend the geographical range, LANs include sender and receiver ID



Solid arrows indicate the communication path from the CXC teleterminal through the Rose information exchange's node processor. Control and packet information (broken arrows) are split off for transfer to the Ethernet network.

information in all transmissions. The sender issues a datagram that includes a physical address and the intended receiver's symbolic address. If identified on the network, the intended receiver returns a physical address and the original sender's address on another datagram. This establishes a virtual circuit for actual message transfer.

However, the elaborate encoding and decoding process precludes using packet switching for short haul transmissions. Also, extensive signaling and overhead information must be used regardless of actual message size. Thus, fixed bandwidth schemes prevalent for such networks emphasize long messages.
(continued on page 82)

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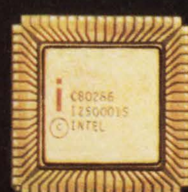

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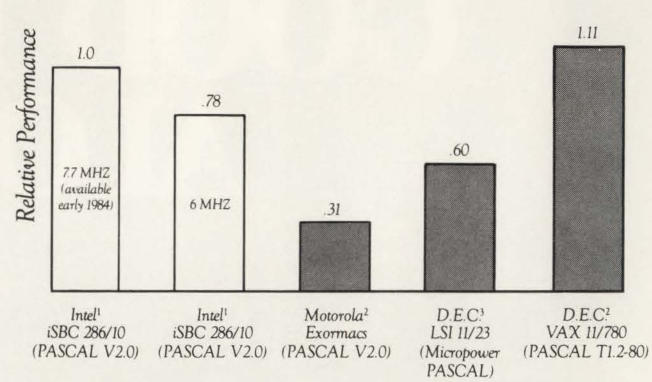

[1]Based on Eratosthenes Sieve Benchmark in PASCAL. Details available from Intel's "Eratosthenes Sieve Prime Number Benchmark on the ISBC 286/10 Board," literature order number 210984. [2]"Eratosthenes Revisited," BYTE. Jan., 1983.
[3]"A System/Architecture Approach to Microcomputer Benchmarking." Digital Equipment Corporation. Sept., 1982.

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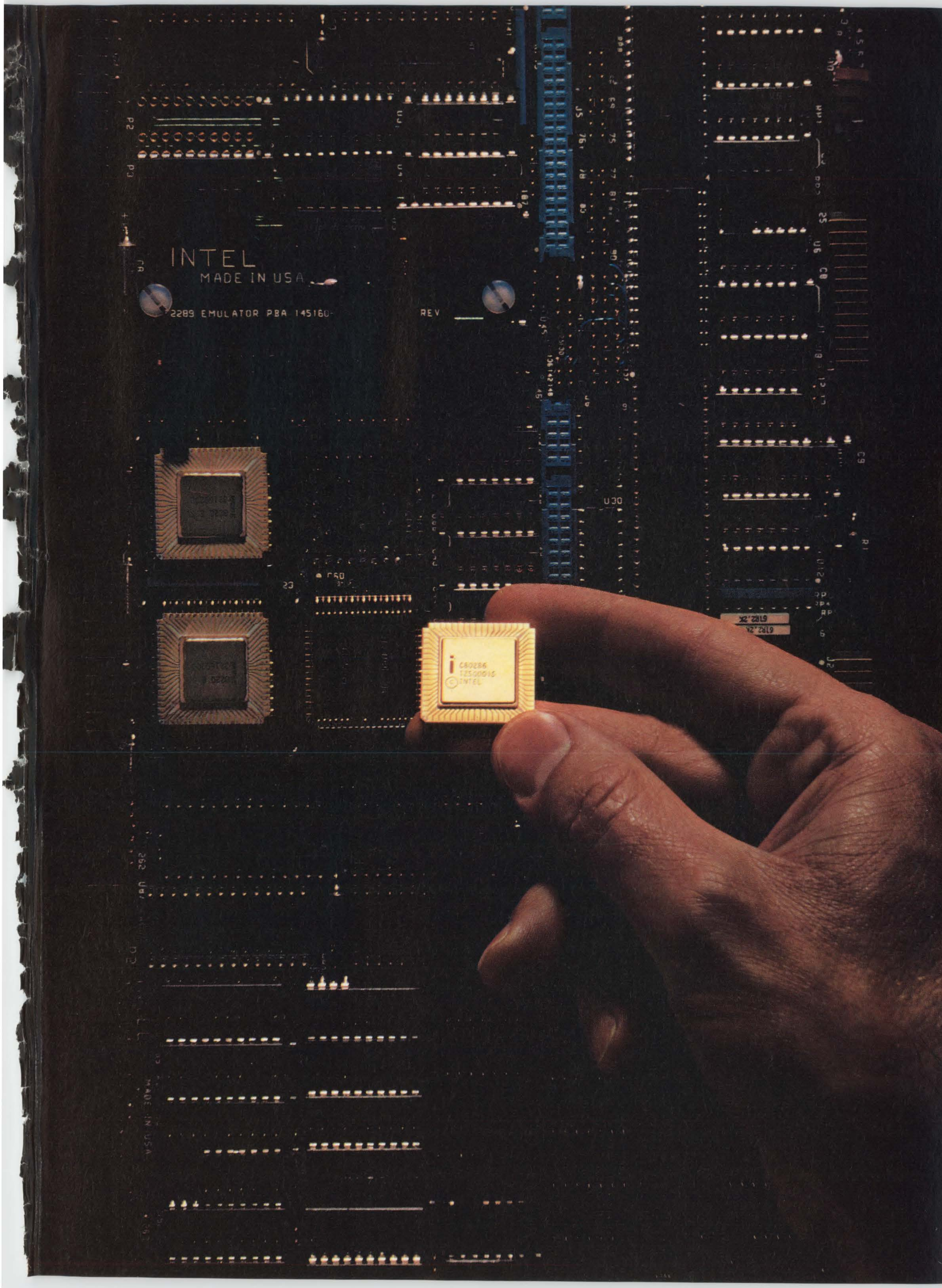
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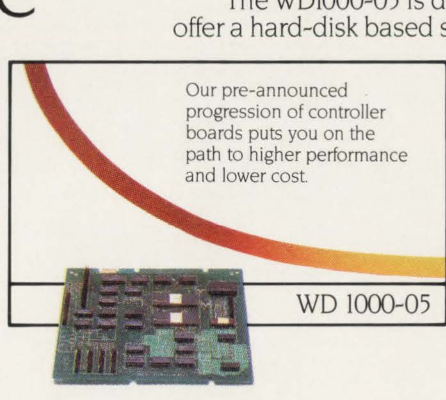

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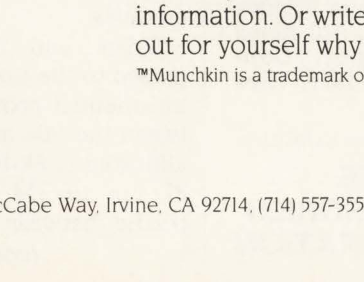

A single read line is the only input required to recover serial FM or MFM data from the disk. Data rates are selectable. So are sector lengths. And a new programmable Motor On feature pre-enables the spindle motor. Stepping rates are compatible with the FD1793. Or, for rates of 2, 3, 5 or 6 msec, specify the WD1772 version.

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WESTERN DIGITAL
C O R P O R A T I O N

Information system
(continued from page 76)

That is, they combine several short messages into a single long one if sent to the same receiver.

The CXC exchange overcomes these limitations by supporting intranode communications (a node containing up to 192 subscribers) with per-line switched station interface modules (SIM) and internode communications with packet-switched network interface modules (NIM). As many as 64 node processors can be linked in a cluster to serve 12,288 subscribers. More than 50,000 subscribers are linked when a maximum of four such clusters are connected. Both broadband and baseband network techniques establish virtual circuits between subscribers on different node processors.

The Rose revolves around SIM functions. Digitized voice and data transmission are passed at 192k bps between a user's telephone/terminal and one of four quad-per-line-switches (QPLS) contained in a single SIM. Since 2-pair wire is used as a transmission medium, time division multiplexing (TDM) techniques split the 192k-bps frame of information into two clear channels of voice and data with 64k bps allocated to each. A third 64k-bps channel is used for packet and control information.

Intranode transmission usually involves switching within a SIM (each SIM handles 16 lines) or between any of the three SIMs contained in a node processor. Data transmissions can be increased from 64k bps to 128k bps if there is no simultaneous voice transmission. If all four lines controlled by a single QPLS are tied together, data transmission rates jump to 512k bps. Variable bandwidth allocation in 8k bps TDM windows allows the node to dynamically configure as a ring or multidrop network topologies in addition to traditional point to point communications.

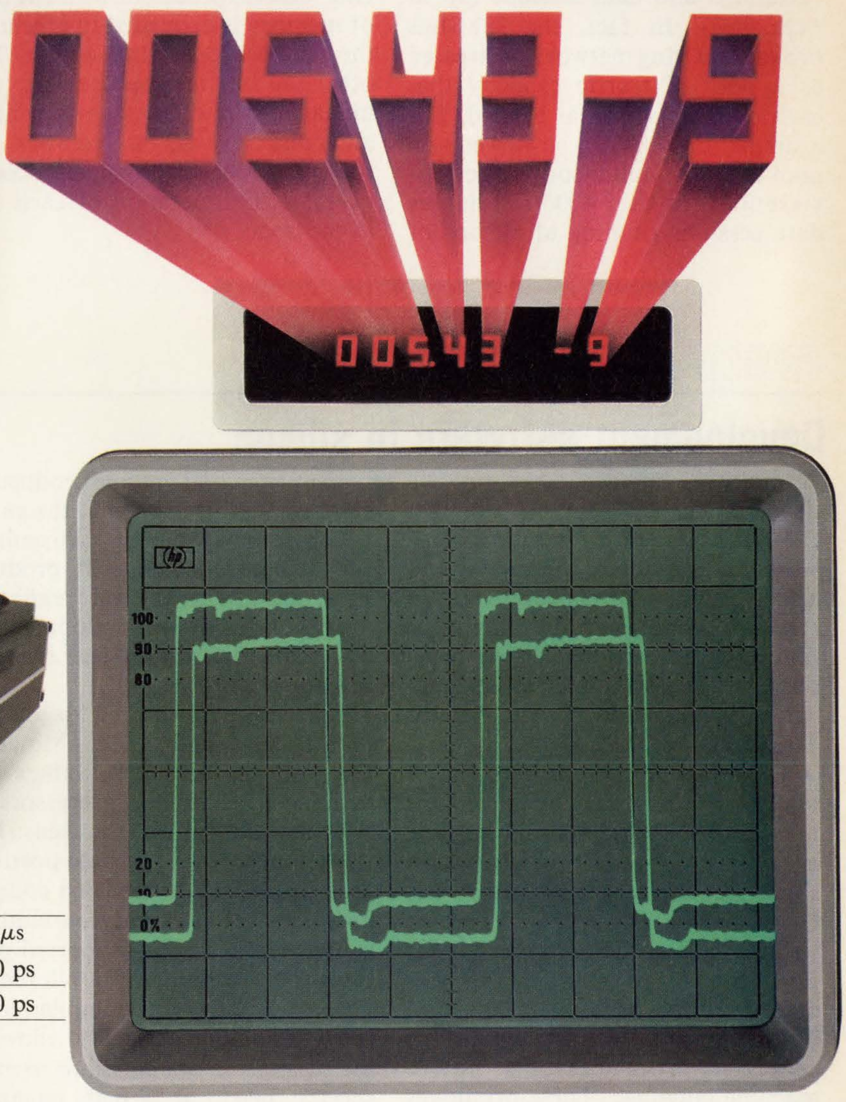
For internode transmissions, the SIM splits the control and packet information from the voice and data frames, and passes it to the NIM for transmission on an Ethernet network. The Ethernet network provides message routing between nodes. Datagram services for message routing are provided on the Ethernet network. Actual message transfers occur on the virtual circuit established on the broadband network. Each NIM handles 12 station modules.

Voice and data channels are passed to the NIM with an HDLC-like bit-oriented protocol. The path between the SIM and NIM can also be allocated in 8k-bps increments from 8k bps to 2M bps. Likewise, the traffic between the NIM and the

(continued on page 84)

 CIRCLE 45

For the first time...an oscilloscope to match the timing accuracy demands of today's fastest technologies.



Laboratory quality timing accuracy plus the convenience of a portable oscilloscope.

If the accuracy of your timing measurements must keep pace with the latest technology, the HP 1726A Time Interval Oscilloscope is your best solution. It can handle tough timing problems. Although most general-purpose, laboratory oscilloscopes solve a variety of problems, their timing accuracy is typically design limited to ±500 picoseconds. This simply is not adequate for designing and producing many of today's products.

Introducing the 50 ps scope.

HP's 1726A time-interval oscilloscope solves this timing limitation with a revolutionary approach. Its new method of making timing measurements is based on combining HP counter technology with HP's advanced oscilloscope triggering circuits. The results? New levels of accuracy (±50 ps), resolution (±10 ps), and repeatability (±30 ps). All this in a portable package

TIME-INTERVAL MEASUREMENT

TIME INTERVAL	500 ps	5 ns	1.2 μs
1726A Accuracy	±50 ps	±50 ps	±50 ps
1726A Resolution	±10 ps	±10 ps	±10 ps

that won't clutter your bench or test station. Typically, the 1726A's accuracy is a factor of ten improvement over most laboratory scopes, including the one you're probably using or planning to purchase.

Also, it provides accurate first-pulse measurements...and it's easy to use.

Check the time interval table.

With the 1726A, your time-interval answers are consistently accurate...and oscilloscope timing calibration is preserved even with its Time/Div vernier out of detent. In fact, intervals as long as 1.2 μs can be measured with ±50 ps accuracy.

For unprecedented convenience and ±30 ps repeatability, dial in start/stop trigger levels with 1 mV resolution, position the on-screen markers, and read the answer on the 1726A's LED display. You get fast, convenient, results you can trust...time after time.

Meeting the needs of today's technology.

With continuing IC advances, you'll need the capabilities of the 1726A in your lab or production area. Use it to uncover 400 ps clock skew in computer mainframes. Determine 200 ps propagation delays in IC's or hybrids. With the 1726A's 50 ps accuracy, observe the 20 ns round-trip delay of a test signal within a test system. Or, tie the 1726A to your data-logging system through its HP-IB interface. And with its time-interval module turned off, you'll find the 1726A to be a high-quality, general-purpose, dual-channel 275 MHz oscilloscope.

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CIRCLE 46

Information system
(continued from page 82)

broadband network can vary from 8k bps to 24M bps.

Thus, total traffic can vary between not only intranode and internode transmissions, but also between simultaneous voice (56k-bps) conversations and data sessions (up to 512k bps). In fact, the 33M-bps broadband ring network is treated as a pool of traffic capacity that each node draws on as needed. For example, this bus can be viewed as a pool of 512 simultaneous voice conversations, or over 4000 full-duplex data sessions running at 8k bps or less. Each node can also handle such tasks as voice and text mail, message store and forward, and call cost accounting. In addition, up to four MC68000 microprocessors are available for application software. One MC68000 processor with 1M byte of memory is dedicated to executing the network operating system. The other 16-bit microprocessors can manage peripherals, such as printers and disk drives, as network resources. A single 8-bit microprocessor oversees the operation of each SIM in the node.

Each subscriber can access the Rose exchange system with a teleterminal that incorporates a speakerphone, 30-key alpha keyboard/speed dialer, RS-232 interface, and LCD display. Users need only minimal training to access system functions because the LCD display prompts them through the operation of the terminal's 14 soft keys.

The CXC Rose is scheduled for production late this year. Price and configuration are available upon request. **CXC Corp**, 2852 Alton Ave, Irvine, CA 92714. **Circle 251**

DEVELOPMENT SYSTEMS

Development software in silicon

A totally silicon based target-resident development environment supports the development of realtime software on the actual target system. Sphere, from Infosphere, uses a threaded code Forth-like language that blurs distinctions between various language facilities. This language can be augmented with user-defined extensions.

The Sphere system fits into 16K of ROM and is built around a run-time nucleus that includes a multitasking executive, run-time primitives, and some commonly used device drivers. Other device drivers can either be written in the system's high level Forth-like language or in the processor's native assembler. The run-time primitives are written in the target microprocessor's native machine language. These primitives adapt the microprocessor to a standardized 16-bit architecture. This architecture includes such operators as arithmetic and stack manipulators, interrupt handling operators, and task control operators.

To support an unlimited number of tasks, the multitasking executive uses interprocess communication and a round-robin execution of equal priority tasks. The run-time nucleus can be used as the minimal run-time environment in the final system once software development is completed and volume production started. With this system, the entire 16K-byte development environment can remain in the final product. This allows for software enhancements or for field development of different applications (eg, realtime control systems).

Currently implemented for the DEC PDP-11/LSI-11 family, the Motorola 6809, and the Zilog Z80, Sphere can be adapted to further processors by rewriting the run-time nucleus. For those time-critical program portions requiring absolute machine code, a processor-specific native assembler is provided for each supported processor. In addition, the development system features a compiler-compiler, a language facility allowing the adaptation of extensions to meet specific needs at a high language level. Using the self-defining characteristics of a Forth-like language, the user can create new language elements and data types that are specific to a given application.

For instance, the standard operator set includes emulators for programmable logic arrays and programmed logic sequencers. Such operators, as well as others that can be user defined, allow implementation of the state machine characteristics of embedded realtime systems. As a result of the system's threaded code characteristics, applications become an integral part of the programming environment. Applications are made up of one or more concurrent tasks and can include a subset of the system's supplied, predefined operators in addition to user-defined operators.

Two complete configurations of the development system are available for the DEC Falcon SBC-11/21 single-board computer. One version includes the pretested Falcon computer, a VT-103 terminal, Sphere license and software, power supply, mass storage, and I/O expander. The other version is available without terminal, power supply, or mass storage. **Infosphere, Inc**, 4730 SW Macadam Ave, Portland, OR 97201. **Circle 252**

August Preview—
Watch for a major staff-written review on 16-bit operating systems.

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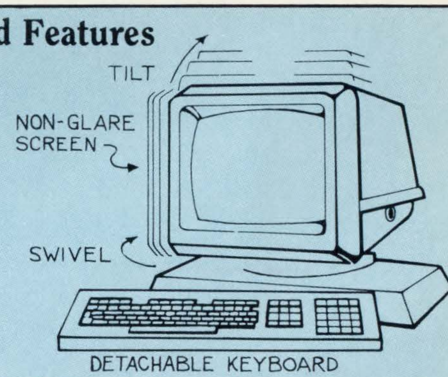

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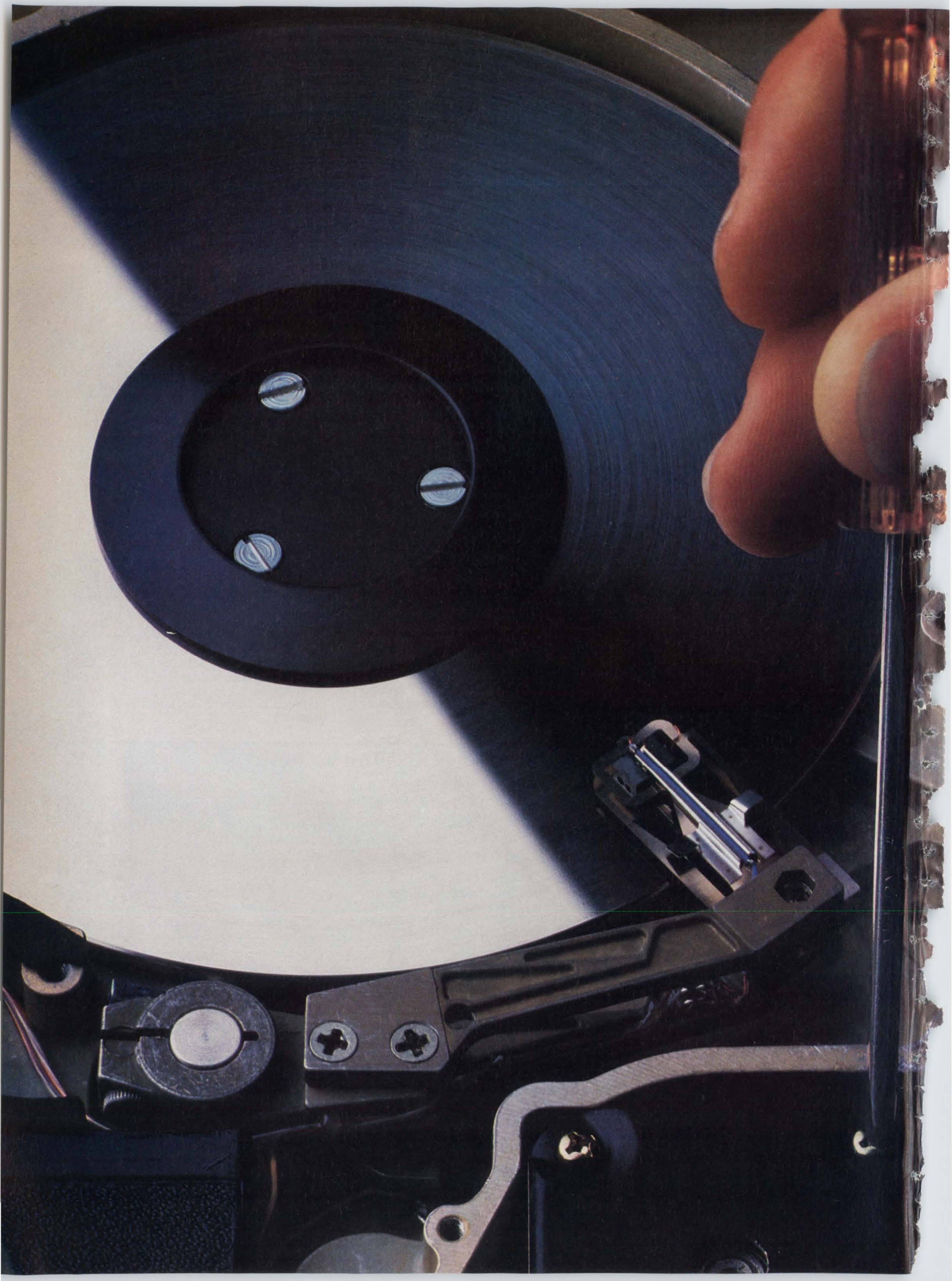

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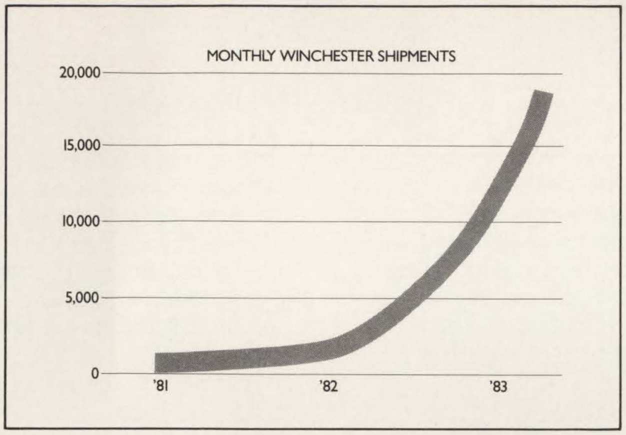

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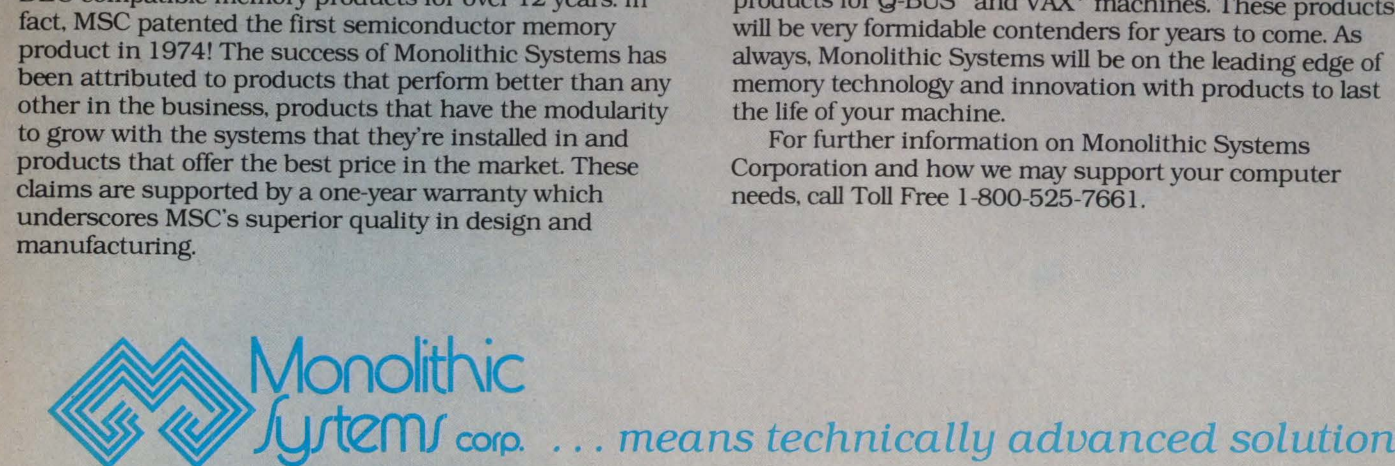

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RUGGED DISTRIBUTED SYSTEMS ADAPT FOR SURVIVAL

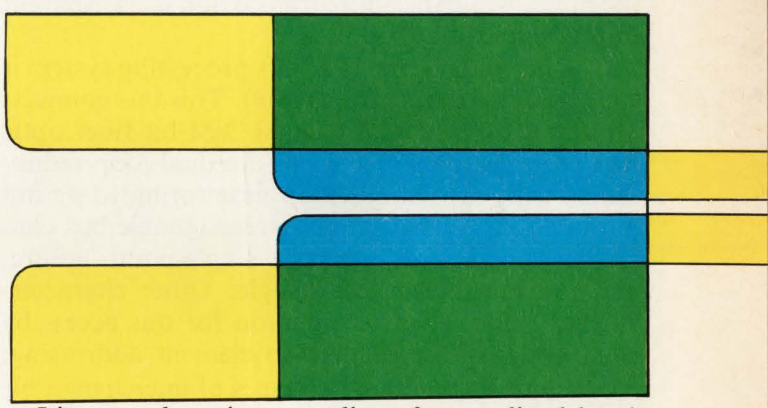
In the harsh world that is ruggedized distributed processing, networks that reconfigure at will can sustain damage yet keep on computing.

by Ralph Mauriello

As distributed processing applications multiply, designers are paying increasing heed to matters of reliability and system recovery. Nowhere is this trend more prevalent than in the ruggedized installations common to many military settings. In such places, the failure of a communication path or system node can have serious consequences. The simple inconvenience and lost time associated with such failures in less harsh environments now literally become matters of life and death.

As a result, novel schemes for distributed systems are constantly being developed. In such schemes, hardware embodying new technology, software capable of recovering from catastrophic failure, and system concepts that embrace redundancy are at the fore. By adopting these concepts, system manufacturers can improve distributed system performance for office, factory, and other civilian areas.

Ralph Mauriello is a senior technical staff member at Litton Data Systems, MS 44-52, 8000 Woodley Ave, Van Nuys, CA 91409, where he is responsible for distributed processing technology applications. He is also interested in emulation design and applications. Mr Mauriello has a BSEE from the University of Southern California and an MSEE from the University of California, Los Angeles.



Litton, a longtime supplier of ruggedized hardware, uses a unique approach to the problems of reliable distributed systems. The advantages of this approach are that processing, data, and control are all truly distributed around the system and configurability allows the system to change according to real-world conditions.

In this system, each node's processing ability can range from one low cost, software compatible distributed processing system (DPS) microprocessor to multiple, high throughput number crunchers. The application programs are distributed as determined by system response time requirements.

The system data base, which is also distributed, has portions that can be replicated at various nodes to ensure that system response time requirements are satisfied. However, only one change authority for each data element of the data base is allowed. Along with the processing and the data base, the

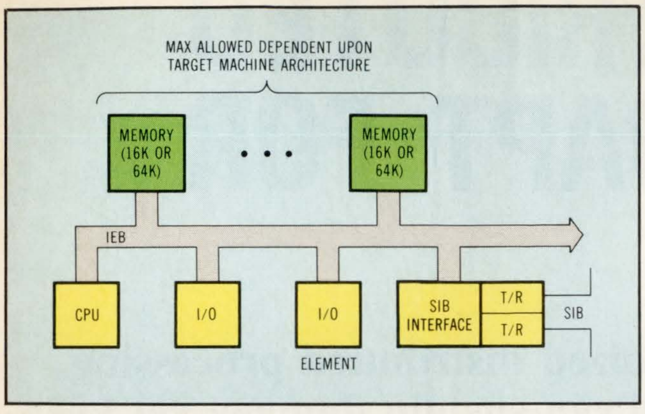


Fig 1 The simplest form of a node is called an element. Board-level CPU, I/O, and memory and interface modules connect by means of an intra-element bus.

system control is also distributed. Local or nodal control is exercised at each node by a replicated executive program. Overall system or network control is accomplished by an executive module that can be located at any one of the system's nodes.

This distributed processing system provides efficient handling of functionally partitioned software tasks. Each software module can issue action requests to other modules, whether local or remote to the node, while the entire transaction is transparent to the requesting module.

The unifying element of this processing system is the serial interelement bus (SIB). This bus connects all nodes by means of a serial 20M-bit fiber optic link. Key features of the bus are dual-loop redundancy with continuous loop monitoring to permit automatic reconfiguration, a reassignable bus controller function to preclude single-point failure, and replicated bus access logic. Other characteristics include self-determination for bus access by each node; direct element to element addressing; four addressing modes; two types of interchangeable transmission media—fiber optics and coax cable; support for system and remote bootload request capability; provision for multiple bus systems; and a 20M-bps transfer rate. These combined features eliminate the possibility of a single failure bringing down the entire system.

The SIB consists of a primary loop for data and a secondary loop for backup. Broken cables or failed nodes are automatically detected and the bus reconfigured to permit complete fail-safe operation. Bus operation is under the control of the bus controller node, which can be any node on the bus. This node continually monitors bus operation for abnormal conditions. There is also a backup bus controller that monitors both the bus and the bus controller. This backup assumes control when it determines that the current controller has failed. Control logic for bus access is fully replicated and independent in each node.

A node's processing ability can range from a single central processing unit (CPU) element to a large multiprocessor. The heart of an element, the simplest form of a node (Fig 1), is a standard internal bus known as the intra-element bus (IEB). All CPUs, memories, and input/output (I/O) interface cards are required to interface with the IEB. The I/O cards can interface with peripheral devices that are currently used in military computer systems.

One of the many configurations possible is a cluster (Fig 2). Adding memory management provides memory protection and paging for up to 2M words of shared memory. Four elements are shown, each capable of simultaneous, independent computation. Elements and clusters can be tied together using the company's SIB. Fig 3 shows a large distributed system configured for a typical military application. All elements and clusters are interconnected to permit complete exchange of

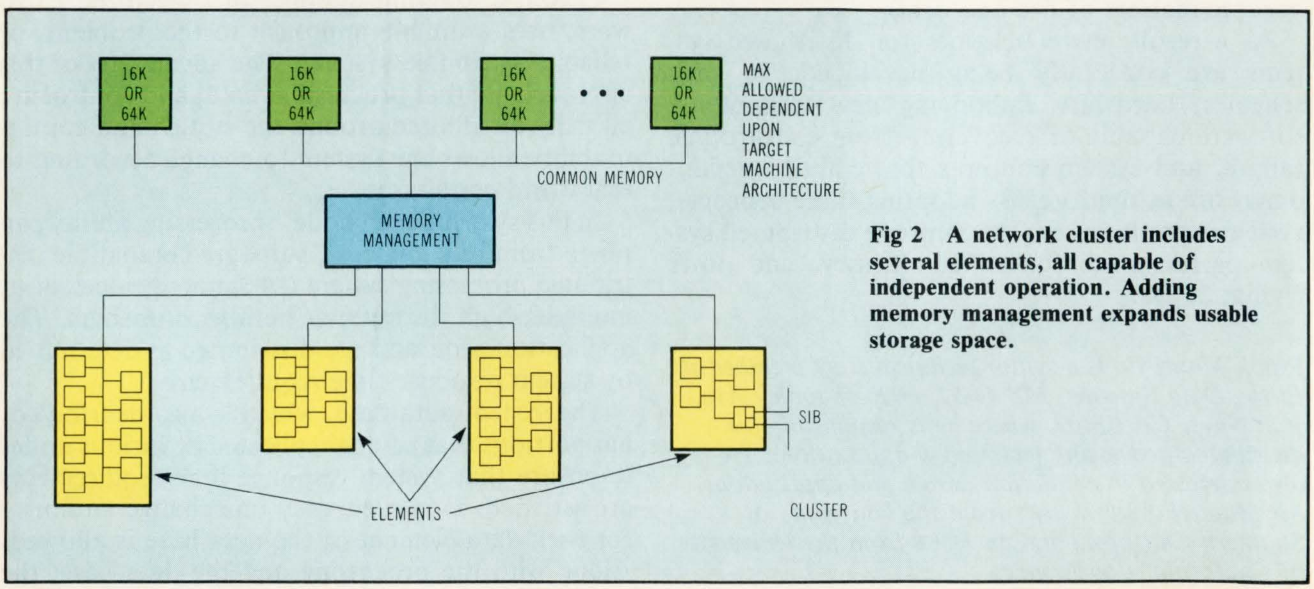


Fig 2 A network cluster includes several elements, all capable of independent operation. Adding memory management expands usable storage space.

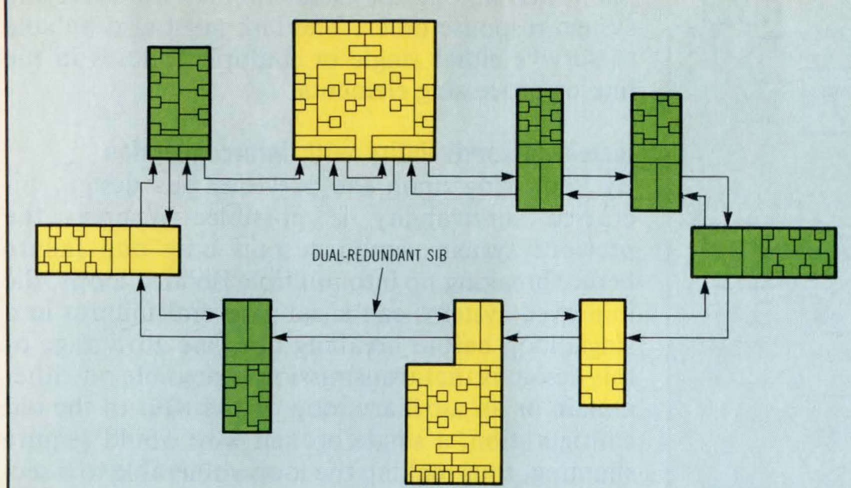


Fig 3 A typical distributed processing system sports nine nodes of varying complexity (clusters are yellow; elements are green). In such a system, reliability, survivability, and reconfigurability are served by an interconnect scheme that allows both control and data exchanges.

control and data. With the DPS hardware and firmware support, the software design can be greatly simplified to permit this function.

The three major functions of the DPS software are system initialization, system control, and local control. System initialization permits bootloading and startup of all processors from a single initiation point. Programs required by all processors reside in a single mass memory bootload medium that can be replicated if desired. Once the system has been initialized, the control software periodically monitors bus and processor performance with fault recovery and degraded mode routines. The software also oversees all bus controller functions and allows a unit that has been removed for maintenance to return to normal operation. The local control software, replicated in every processor, is based on available military operating systems. Those portions of the operating systems not applicable to distributed processing are removed, and the modules required for control and distributed processing are added.

Simulation testing stresses reconfigurability

The first application of the DPS was in a combat simulation test system (CSTS) aboard a U.S. Navy destroyer of the Spruance class. The CSTS simulates a total combat situation at dockside or at sea. Using the ship's installed equipment, realistic training is provided for the entire combat team. Simulation is provided for the principal sensors of the gunfire control system, the underwater fire control system, the missile fire control system, the search radar, and internal ship sensor systems. In addition, simulating external communication permits data exchanges with other ships and intercepting aircraft to be included. Before DPS based simulations, most ships' systems operated on a standalone basis, a situation that limited training and precluded realistic interaction between the various systems.

By providing common surface, subsurface, and air targets to the ship's combat system, the CSTS can simulate the entire ship's external environment. This test system translates complex, multithreat scenarios for operator training. Detailed scripts, entered on disk files, define threats from surface, subsurface, air targets, or various combinations thereof. Each scenario can generate up to 999 tracks; as many as 64 of these tracks can be displayed simultaneously. Scenarios can be suspended, advanced, changed, or resumed at any time.

A 20M-bit serial bus in the CSTS is implemented in a dual-loop configuration [Fig 4(a)]. Information transfer on the primary and secondary loops occurs in opposite directions; the loops are completely independent of each other. In normal operation, the primary loop is used for data transfer while the secondary loop carries a predefined idle pattern. This technique allows each node in the loop to constantly monitor the status of both loops. A failure of either loop—loss of signal/synchronization—will be detected and the bus automatically reconfigured [Fig 4(b)]. Since all nodes are operational and internode communications are intact, the training exercise will proceed without interruption. Should a node fail, the exercise will continue as though battle damage or circuit failure has caused the loss of a sensor.

Combat system requirements, which are naturally more stringent than those for training and test systems, dictated special care in distributed nodes and data bus design. Increased survivability, minimized host interference, minimized software impact on the host processor by using a bus interface card set, and dual-loop interconnectability were the

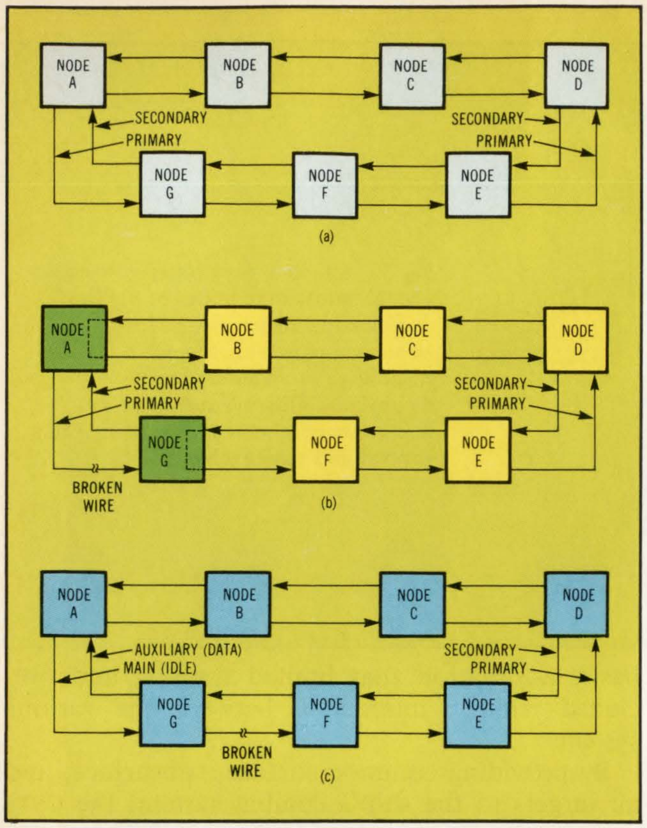


Fig 4 A dual-loop, 20M-bps bus with data flow in contra rotation (a) is the basis of the distributed system. The bus can be reconfigured by shunting (b) if a broken cable of a failed node disrupts normal operation. If a failure in the primary link occurs (c), control can be switched to an auxiliary link to avoid shunting.

needed improvements. As a result of the stringent criteria in these areas, a modified design now provides a 3-card set for interfacing the nodal interface bus (NIB)—the name for the improved 20M-bit serial bus—and the IEB.

This 3-card set improves survivability, the first important criterion, by increasing the number of available transmission paths. Survivability, a major requirement in ruggedized systems, permits operation after battle damage and/or equipment malfunction. This requirement is usually met by the use of redundancy and maintainability; usually, only surviving single-point failures are addressed. Recently developed tactical systems stress continued operation, despite battle damage, by the use of distributed processing with a high speed data bus interconnecting distributed resources.

Key to achieving greater survivability is the design of both the system elements and the communication links between the distributed system's elements. Communication links must be both high in speed and efficient in order to handle the volume of communication between elements; they must also provide acceptable response times. The basic system design requires that processing take place either at the elements where the data are collected or at the location where the processed data are required. This processing location is determined by reducing the amount of data that must be communicated among the elements, and by satisfying system response times. The link must also be able to survive either single or multiple failures in the link or processing elements.

Increased survivability with interconnection

By improving upon the previous bus design, increased survivability is possible. Whereas the previous systems could sustain only one failure before breaking up into multiple isolated loops, the improved systems can sustain several failures in a single loop before breaking up. One advantage of this design is that transmission is possible on either a main or an auxiliary loop of the NIB. In the old configuration, a single broken wire would require shunting, thus making the loop vulnerable to a second failure. With the improved designs, however, several cable failures can be sustained without shunting. Fig 4(b) shows that a single failed cable in the old system results in a shunt condition. Fig 4(c) shows that data transmission around the loop can be achieved in spite of the broken cable. This can be done without shunting by simply switching to the auxiliary loop. Fifty percent of subsequent failures can be accommodated by shunting, thus keeping the NIB fully intact.

Furthermore, a new scheme (Fig 5) increases system survivability by interconnecting the main loop with the succeeding downloop nodes. The auxiliary loop is interconnected so that it skips a node; any failure on the main loop causes automatic switching to the auxiliary loop. As with the scheme shown in Fig 4(c), subsequent failures to the main loop will not affect operation. This interconnect scheme can also sustain failures in the auxiliary loop while maintaining complete communication between all nodes. Though the algorithm for implementing the reconfiguration is more complex than that required for the interconnect scheme shown in Fig 4(c), the added reconfigurability gives this interconnect scheme greater use.

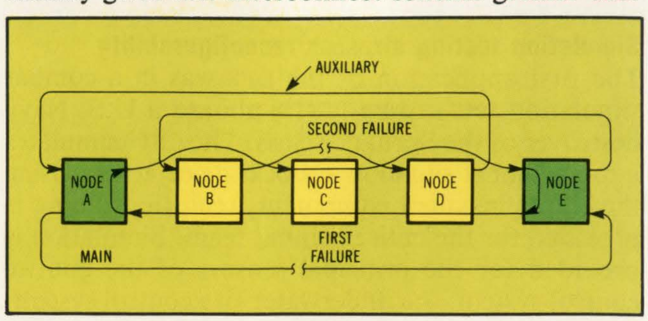


Fig 5 Reconfiguration allows the system to operate when both the main and the auxiliary links have sustained damage. Failure in the main loop causes automatic switch to the auxiliary loop. A second failure in the auxiliary loop causes shunting of nodes A and E. Communication is thus maintained between all nodes.

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Besides survivability, the 3-card set design meets other improvement requirements. Direct memory access for the card set and a programmable microprocessor within the card set permit execution of all bus functions within the microprocessor. Dual-loop capability is improved by an additional 3-card set that provides an interface to the second NIB and direct interconnection of the interface card sets, thereby eliminating node processor software and interference.

Reduced interference with the node CPU and minimized impact on the node processor software directly result from using a microprocessor in the node interface controller. This permits bus protocols, bus controller functions, and message routing to be supervised at the interface controller, thus removing these responsibilities from the node processor. Resulting response time improvements meet the requirements of a realtime combat system. The software impact on the node main processor is now limited to the development of an I/O handler appropriate for the architecture being emulated.

Litton's DPS concept calls for the use of multiple architectures. Before the DPS, all bus functions had to be implemented in software and, therefore, in the native language of the target computer being emulated. Placing all of these functions outside the node processor eliminates the costs traditionally associated with developing the bus function software.

In applications where survivability and reconfigurability are paramount, this network scheme proves to be a viable architecture. Although the network criteria described here are currently the sole province of military application systems, this will not be the case for very long. As distributed systems proliferate to other settings—such as hospitals, financial institutions, and realtime control environments—the need for reliable, reconfigurable performance will become evident. Moreover, as manufacturers and system integrators assume increasing liability for their products' shortcomings, their incentive to ensure continued operation—or, at the very least, graceful failure under less than optimum conditions—will increase.

The DPS provides a viable alternative to link failures. The design's simplicity is likely to attract both generals and general managers concerned with their distributed processing systems' ability to keep on computing in both simulated and real-world conditions.

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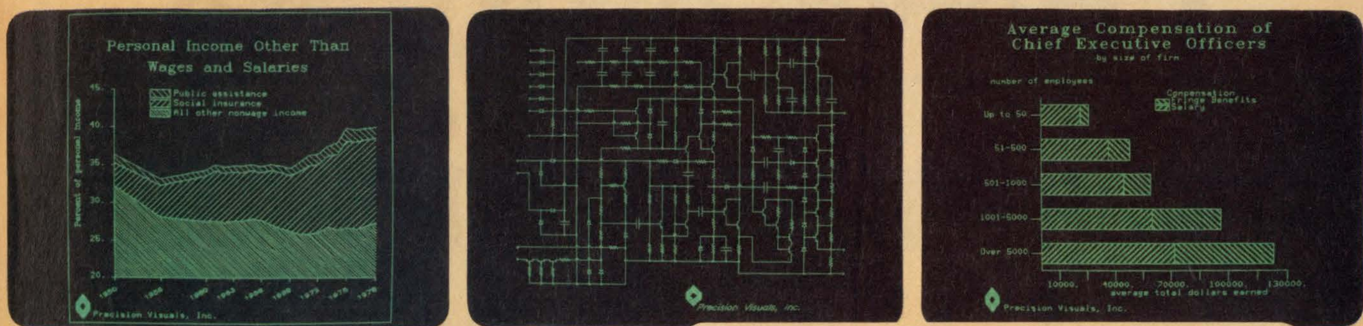

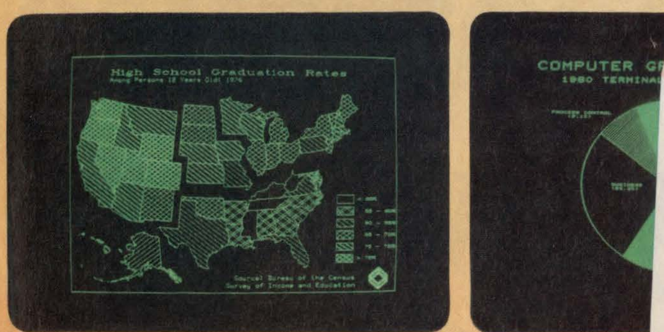

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Vertical Resolution	585	585	240	480	240	480	240	240	480
Horizontal Resolution	768	768	640	640	800	800	1225	1225	780
Dot Density Ratio	1:1	1:1	1:2	1:1	1:3	1:1	1:4	1:4	1:1
Screen Size	14"	14"	12"	12"	12"	12"	12"	12"	12"
Tektronix 4014 Compatible	STD	STD	NO	NO	NO	STD	NO	STD	STD
Data Tablet Support	STD	STD	NO	NO	OPT	OPT	NO	NO	NO
Multi-Vendor Printer Support	STD	STD	OPT	OPT	OPT	OPT	OPT	OPT	OPT
8 Dir. Cross Hair Cursor	STD	STD	NO	NO	NO	NO	OPT	OPT	OPT
Programmable Function Keys	STD	STD	NO	NO	NO	NO	NO	NO	NO
Tilt/Swivel Enclosure	STD	STD	NO	NO	NO	NO	NO	NO	NO
Compatibility	VT52 ADM3A H1500 D200	VT100 VT52 ANSI X3.64	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52
PRICE (suggested list*)	$2,495	2,695	3,025	3,355	3,025	3,510	2,890	3,390	3,190

*Retrothoughts price includes DEC VT100® terminal based on published information as of 4/1/83.

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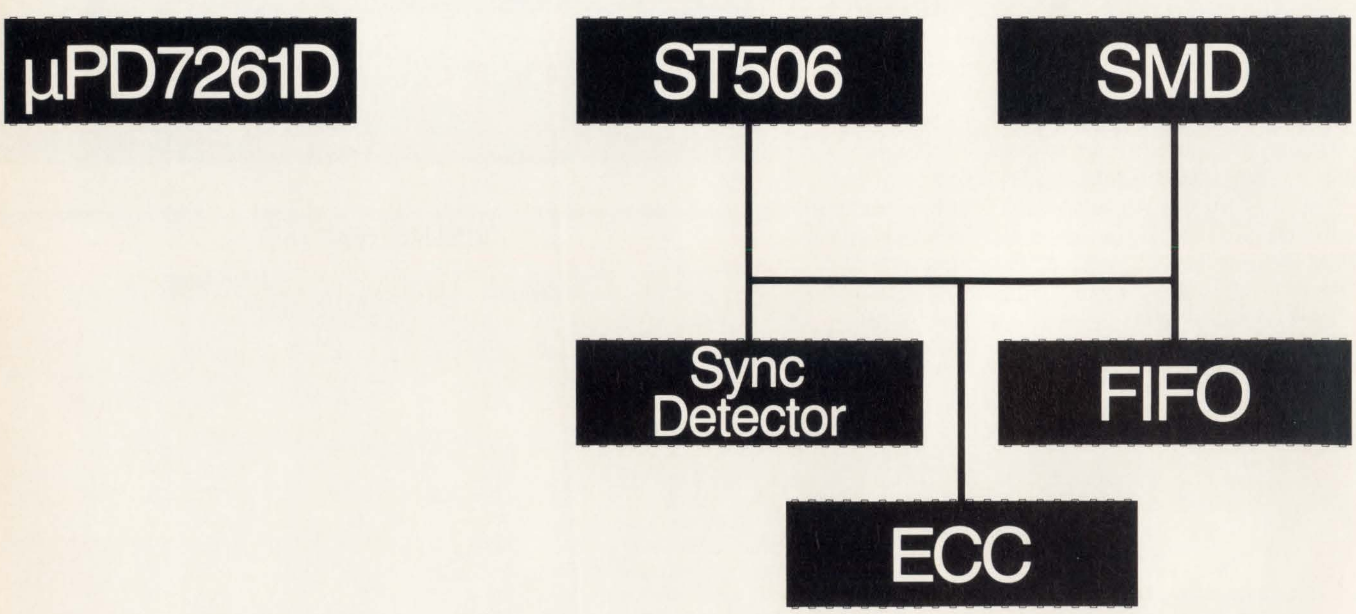
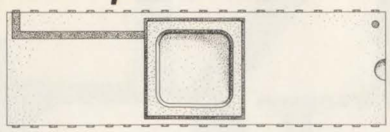


μPD7261D



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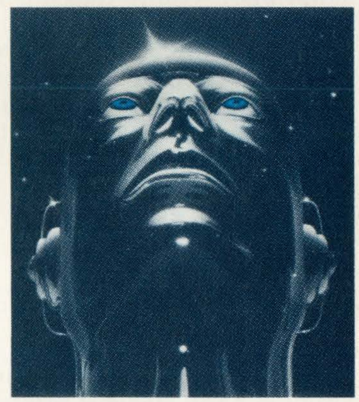

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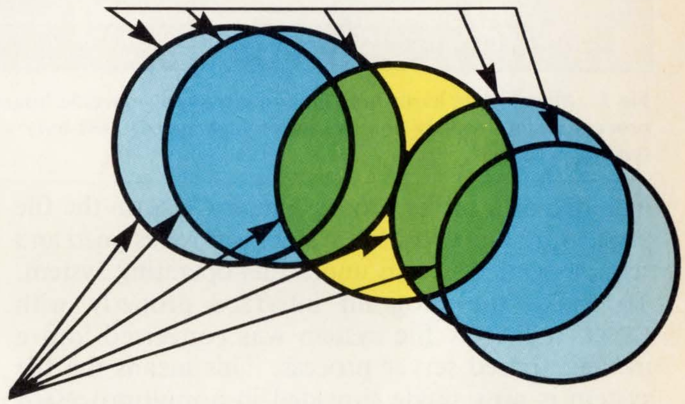
CIRCLE 54

PUNCHING UP UNIX PERFORMANCE

By enabling UNIX to handle message based information transfers, it can be adapted for use on the latest generation of systems that incorporate multiple file processors.

by Edward L. Patriquin Jr and Stephen Ricossa



The advent of distributed processing and intelligent workstations has proved a boon to the localization and dissemination of computer power. As remote workstations and terminals become more powerful, however, the overall system software has had an increasingly difficult time in coordinating the activities of the many elements it must oversee. Worse still, performance is often diminished as data exchanges and system processes are forced to file through hardware bottlenecks *en route* to their destinations.

Many coping strategies have been invented to redress this situation. One of the most promising is a combined hardware/software approach that uses function-specific hardware and software modules to perform diverse system operations. In such a system (Fig 1), several types of board-level computers serve specific functions. Four types of processing are provided in the system depicted in Fig 1: user terminal (RS-232), cluster workstation, applications and mass storage/file handling.

Coordinating operations remains a problem, however. In the case of Convergent Technologies' MegaFrame system, this problem is amplified. The reason is the system designer's desire to allow two separate operating systems, Convergent Technologies' operating system (CTOS) and UNIX, to coexist within the same multiprocessor system. This combination enables users to have the best of both worlds by running standard UNIX System V software in a realtime, message-passing environment.

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Stephen Ricossa is a software engineer at Convergent Technologies' Data Systems Div, where he is responsible for operating systems software. He has a BS in electrical engineering and computer science from the University of California, Berkeley.

Software design

The two major software challenges facing the software designers were the desire to use the existing software base running under CTOS, and to maintain full compatibility with Bell's UNIX System V. CTOS is a message based operating system with a realtime kernel. Because system services needed by an operating system (eg, terminal handling and file management) are built on top of the kernel, each processor can be endowed with only the functions it needs. For example, the terminal processor (TP) has no file management ability, and the file processor has no terminal handling ability.

Individual operating systems running on different processors can communicate because each processor can access memory in any other processor. This enables mailbox-like, message based information transfers to occur. As a message based operating system, CTOS required several changes to perform this task, but UNIX, which has no real concept of message passing in discrete packets, required a whole new software layer to be written. This layer allows the operating system to communicate via messages to all other processors in the system (Fig 2).

To improve performance and allow file resource sharing, the UNIX file system was offloaded and

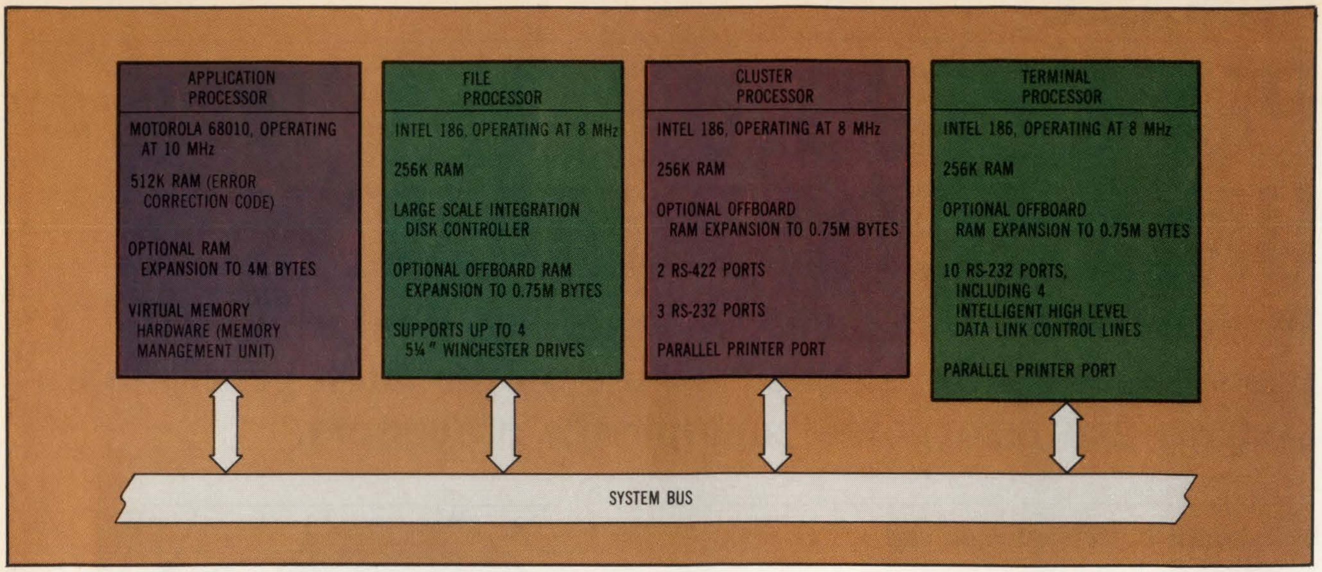

Fig 1 MegaFrame hardware components supply specific board-level computers for various system tasks. All processor and memory boards share a high speed, 11M-byte/s bus. Actual systems may contain several of each type of processor.

included as a server process under CTOS on the file processor. The UNIX file system was redesigned and reimplemented to run under this operating system. To make the program interface properly with CTOS, the UNIX file system was converted into a message based server process. This means the file system is now single threaded in a multiprocessor environment. A parallel server process using the same data structures as the regular file system was added. Any operation modifying a data structure is sent to the single-threaded file system server for completion. This allows high volume traffic, such as normal reads and writes, to flow quickly around the single-threaded bottleneck. It also eliminates concurrency problems that arise with multiple-threaded operation.

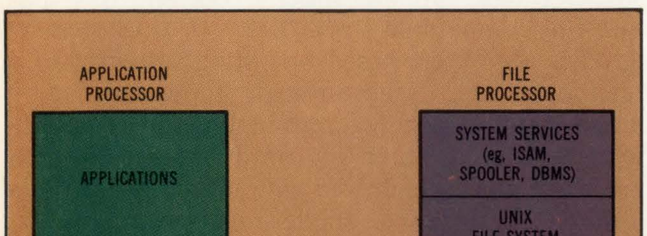

Fig 2 CTOS and UNIX compatibility is gained via the ICC software layer. This protocol allows the passing of messages across the system bus. Messages can be either requests or responses relating to the status of tasks.

Controlled access files

UNIX was designed to allow as many simultaneous reads and writes as desired. In a multiple-processor environment, a question often arises as to which processor has the most recent file update. Normally, there is only one process writing to any particular file at a given time. When there are multiple processes writing on the same processor, UNIX buffers them properly. A problem exists when the file is already open and is then accessed again for write by a different processor. This situation, known as a controlled access, causes the file processor to pick a file master for that file. From that point on, all operations concerning this file funnel through this file master to the file processor until the file is closed, eliminating ambiguity.

In addition, UNIX assumes that all of its processes are running on the same processor, implying that all information concerning them is in one central place. With multiple processors, this is obviously no longer the case. Ensuing confusion is eliminated by assigning unique process identification numbers and teaching the utilities to use this information in a manner consistent with standard UNIX.

Running multiple operating systems on the same machine is pointless without a method of sharing service resources and data. To let UNIX share services with CTOS, the message handler running in the UNIX kernel had to be enhanced. This allowed full CTOS message handling, including sending messages directly to another processor, to be used under UNIX. Thus, it became possible to route messages to the proper service process, allowing any UNIX user to access the standard existing CTOS system services, including indexed sequential access method (ISAM), systems network architecture (SNA), 3270, 2780, X.25, and Convergent Technologies' database management system (CT-DBMS).

The message structure that CTOS uses (and adapted to UNIX) is a simple request/response algorithm. For each request sent to a process, the process must respond in some way (including expiring). To reach a process, a request or a response must pass through an exchange (a place where messages wait to be received).

The entire algorithm is driven by the concept of a request code and the associated service exchange (Fig 3). A request code specifies the basic format of a request and the location of the service exchange. A service exchange is the exchange on which a request is queued for service by some process. The service process, in turn, dequeues each message and services that request. Upon completion, the service process calls a subroutine to respond to the request. The exchange to which the response is queued is embedded in the request. Because request blocks are self-descriptive, they can be checked for validity regardless of the actual request.

To communicate with other processors, known as Inter-CPU Communication (ICC), the request and response circular queues can be accessed by all processors. This is achieved by setting a lock flag in the requestee's (server's) memory. Since this operation must be uninterruptible, a locked test and set instruction is used by all processors. Once the flag is set, the requester places the CPU identification and the address of the request/response in the requestee's memory in a circular queue. The lock is then removed and the server processor is interrupted and informed that an addition has been made to the ICC request or response queue. Once the processor receives the interrupt, it determines whether the message is a request or a response. Then, the message is copied from the client processor to an area in the server processor.

If the message is a response, the processor finds out which exchange the response is to be queued on. If there is a process waiting for something to be queued on that exchange, the process is woken up to process the response. When the message is a request, the processor finds out if there is any one process that services that request on the requestee's processor. If not, an error code is set within the request and a response is initiated.

The system's distributed design made it easy to functionally partition the software. In turn, this partitioning simplified the entire software effort and made configuration and expansion easy for original equipment manufacturers because of the reduction in interprocessor coordination that is required.

To service workstation needs, the cluster processor (CP) needs only a file processor. The CP controls communication on the high speed cluster

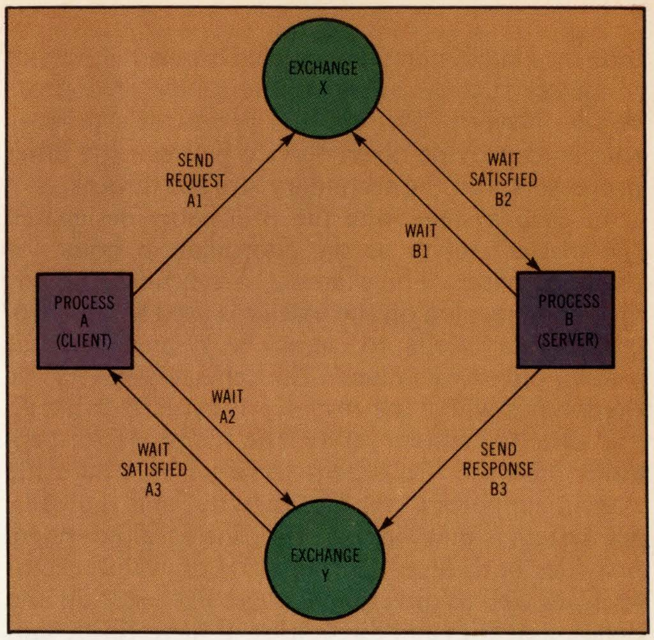

Fig 3 CTOS message structure is based upon a request/response algorithm. Exchanges are similar to mailboxes and provide a place for messages to reside while they are waiting to be received.

lines, on which both workstations and terminals can be placed. The CP software polls each workstation or terminal connected to the cluster line and runs all the communication software including X.25, 3270 and 2780 emulation, and SNA. It also allows both a daisy wheel and a Centronics-compatible printer to be connected at the same time.

The TP is designed to handle up to 10 RS-232 lines at speeds of up to 19,200 baud each. To run the lines at that speed, it is necessary to poll for input characters every 500 μs. This polling loop consumes 18% of the total processor bandwidth; the remaining bandwidth handles communication utilities.

Home of the UNIX kernel is the application processor (AP). While externally it is still Bell System V UNIX, the kernel has been converted from a swapping system to a virtual memory system. Even though there can be many processors all running UNIX, the system still appears to the user as a single processor.

For instance, a unique process identification is assigned to make a process status (PS) command look as it would on any other commercial UNIX system. This command, however, is extensively modified. Included is a facility to query process information from other processors across the bus. This information is then processed and displayed in the same manner as the standard PS command.

The file processor and its software

The file processor's role is important because it is not merely a device controller but a complete computer running CTOS configured with the UNIX file interface subsystem. It can also run other service processes such as an ISAM file server or a DBMS server. Nevertheless, the file processor's primary role is to provide direct service between the other processors and the secondary storage devices.

In each system, one file processor, designated the master, serves as the coordination point for many activities. For example, a central name service implemented on the master is used by any processor that needs to access a system resource known only by its name. The central name service determines where the resource is actually located.

As the file system server, the file processor provides the base file system services. This base file system supports CTOS files directly, and the UNIX file system is built on top of it. The base file system provides both input/output (I/O) on a disk sector level, as well as directory services like creation and deletion of files and directories. It has a fixed, simple directory hierarchy: the top level addresses the physical disk device, the middle level a particular directory within that device, and the bottom level a particular file within that directory. The interface subsystems that allow a specific type of file and directory access method to be based on these abilities, such as the UNIX access methods, provide the code that maps their particular structures to the base file system.

Thus, the base system remains constant while retaining flexibility in the type of application file access methods that can be built on top of it. This furnishes several benefits. First, it provides flexibility in supporting diverse operating systems with their special needs for file service. Second, it allows the storage devices to have one format such that backup and restoration operations always function regardless of the type of application file system supported. Third, it means that the basic operating system/file system software running in the file processor need not change when a new file system or file access method is added.

In providing its directory services, each file processor controls all accesses to the files resident on the devices connected to that file processor—and only those files and devices. That is, each file processor has complete control over file storage on the devices connected to it, but cannot operate on files residing on devices connected to any other file processor.

Furthermore, a file processor (other than the master) has no information about the devices and files on the other file processors, except that they exist. The particular parameters describing the directories, files, or even open files reside exclusively in the controlling file processor. This separateness is further imposed on the file handles created for open files, and on the device names themselves. Due to this functional partitioning of device control, requests originating at other processors must be routed to a particular file processor. This is the job of the ICC subsystem.

In its support of a base file system, the file processor performs all the functions required of an efficient secondary storage driver. For disk devices, it optimizes the execution of multiple sector transfers by transferring as much data as is physically possible for each single I/O operation. The disk driver schedules all pending I/O operations and also performs overlapping seeks by issuing buffered seeks to each drive at the highest possible rate.

The file processors function as the main data servers for the distributed processing system and, in fact, are the only processors that control storage devices. This puts a high demand on them for producing and consuming secondary storage data. Demand comes from all the processors, but especially from the APs. In general, all file processors have to provide secondary storage service for the system when online. In addition, the master file processor is responsible for bootstrapping and downloading code to all other processors. The software uses the file processor's ability to establish a direct memory access (DMA) channel between the disk device and the memory of a remote processor to achieve the high disk bandwidth. Reading and writing the disks is the most common service the file processor provides (Fig 4).

When a file processor receives a request to read some number of sectors, the disk data destination may be a remote processor. That is, the requesting process could be running in a processor other than the one receiving the request. The request block information contains the buffer address where the disk data are to be delivered. This address has two basic components: a single-byte hardware-encoded bus address of the processor, and the linear address relative to the beginning of the destination processor's memory.

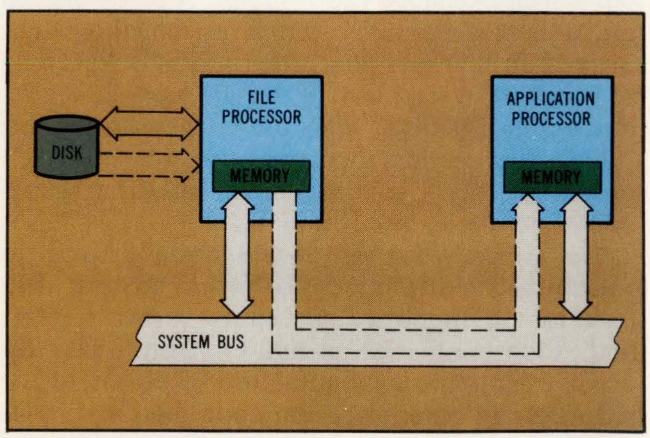

Fig 4 Disk read/write operations can take place as remote DMA transfers initiated by a file processor. Here, data are received from the disk controller (dashed lines), assembled into 4-byte packets, and transferred in 32-byte bursts.

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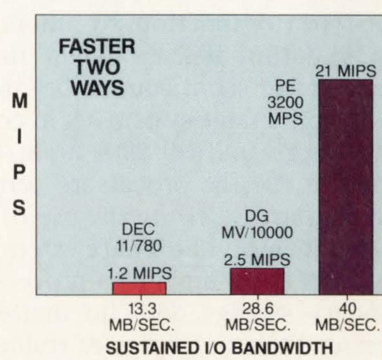

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CIRCLE 56

Such a linear address is required because the iAPX 186 based processor boards and the 68010 based processor boards store information in memory with adjacent bytes in reverse order. When the file processor software determines that the disk is ready to start the data transfer, it issues a read operation to the disk controller, along with a start remote DMA operation to the DMA logic onboard. From the software viewpoint, this causes the entire disk transfer to run to completion, although the hardware is performing several discrete steps.

Downloading, which occurs during system bootstrap and any other time a processor must be downloaded and started, is a special responsibility of the master file processor. This downloading process is a coordinated one where the master file processor is in control and all other processors in the system act as slaves.

The master file processor executes its bootstrap read only memory like the other processors. However, since it can determine through a hardware status port that it is the master file processor, it proceeds to read the bootstrap code from a local device (its own disk or tape) and starts up the operating system. The master then turns its attention to the other processors, polling each possible bus slot position. It then determines if a processor is connected to this slot at all; if a processor does exist but failed its self-test; or if the processor passed its self-test and is waiting for bootstrap service.

If the master file processor finds that all is well, or that a sufficient number of working processors are present, it reads each processor's request for service, downloads the appropriate system image into each processor, and issues an interrupt to that processor—waking it up and causing it to execute the code that was downloaded into it. Thus, the master file processor is the critical element in bringing the system to life.

Inter-CPU communication the key

Permitting several autonomous processors of the same type to function by interacting with each other and thus deliver higher throughput is the system's most significant ability. Multiple file processors in the same system act in concert to support a very large unified data area. Software implemented in the file processors permits this unified large data area, despite the use of discrete processors and memory. Software extensions to the CTOS file system allow any given processor to access any secondary storage data no matter on which file processor the storage device resides.

The software subsystem that ties all multiple file processors together, allowing them to function as a unit, is the ICC. Multiple file processors use the ICC to achieve unified file system service in three different ways. First, the master file processor broadcasts requests to ensure that all file processors are synchronized for certain situations. Second, ICC routes all file system requests that involve a pathname (device, directory, file and specification) to the master. The master file processor then determines which file processor services the device name specified and performs another ICC route to that file processor (Fig 5). Third, the file processors utilize the ICC's ability to route file system requests that contain a file handle for an open file directly to the file processor servicing that file.

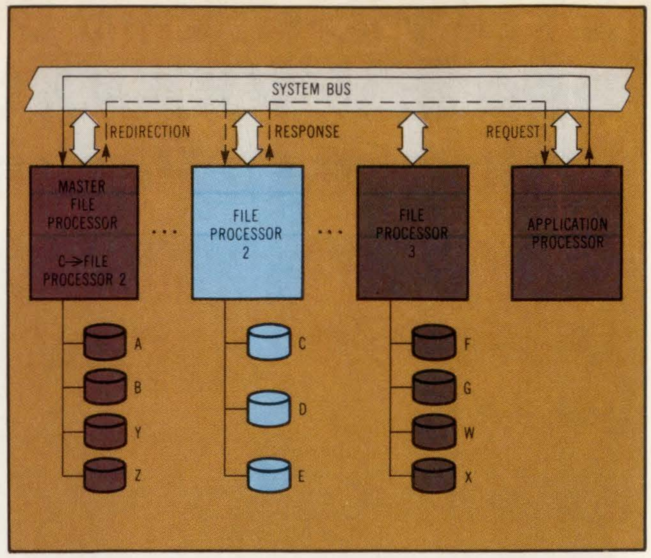

Fig 5 Routing of a file system request for volume C entails several steps. When the application processor requests to open a file, the request is routed to the master file processor. Here, it is determined that file processor 2 serves volume C. The message is redirected to file processor 2 and completes its request/response action (dashed lines). It now responds directly to the requesting application.

Although each file processor manages the devices and the data on them virtually independently, a small class of information and activity is synchronized among the file processors. When this synchronization is required, the relevant original request is routed to the master file processor, which implements the synchronization. Shared information is the CTOS user profile information. Since a user or some application process may potentially access data on any file processor, each file processor must have user profile information available for every user.

Activities that have global implications for file system storage must be synchronized. There are two such cases. First, the file system supports requests that permit a user to close all currently open files. Since the user may have files open on any device, each processor must receive the request so that any of that user's open files controlled by that processor can be closed. Second, the file system must be able to suspend all disk activity. Again, this request must be broadcast to all file processors so that all activity can be stopped.

The master file processor functions as a filter process for requests; responses are routed directly. One exception, however, is when the master is the processor that services the request. In this case, the master does not act as a filter but instead actually services the request and posts completion to the original requester using ICC.

Furthermore, one of the primary jobs of the open request, in terms of request routing, is to cause the open request to establish a logical connection between the requesting user application and the file processor serving the file being opened. When a file is opened, the file system returns a file handle to the user. This handle uniquely identifies the file. This is then used when subsequent requests for service on that file are issued.

To enable the ICC to route the subsequent requests that pass file handles for that open file, the file processor servicing the open request places an encoding of its processor bus address into the file handle. The ICC mechanism uses this encoding to route requests from the user application, such as read sector or write sector, directly to the servicing file processor. This produces the logical connection that allows efficient, direct routing to take place.

When the user application is finished with the file, it issues a close file request using the file handle. The servicing file processor closes the file and considers that file handle invalid. The logical connection has now been severed. However, the ICC itself knows nothing of the file system activities; so, if the user application should erroneously issue another file request using that file handle, the ICC would route it to the correct file processor. Upon arrival, the file processor would determine that the file handle is not currently valid and post a completion status with an error indicating an invalid file handle. Thus, the ICC mechanism and the special software in the file processors function in concert to form a unified storage system distributed among devices controlled by several processors.

In the system described, true distributed processing within a local environment is used to produce a powerful, high bandwidth, distributed computing system. Key to the system is the software that allows the use of multiple backend file processors. These processors improve system throughput by offloading the major part of the I/O activity from the other processors. Since these file processors are true computer systems in themselves, they also support sophisticated applications such as database management.

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CIRCLE 59

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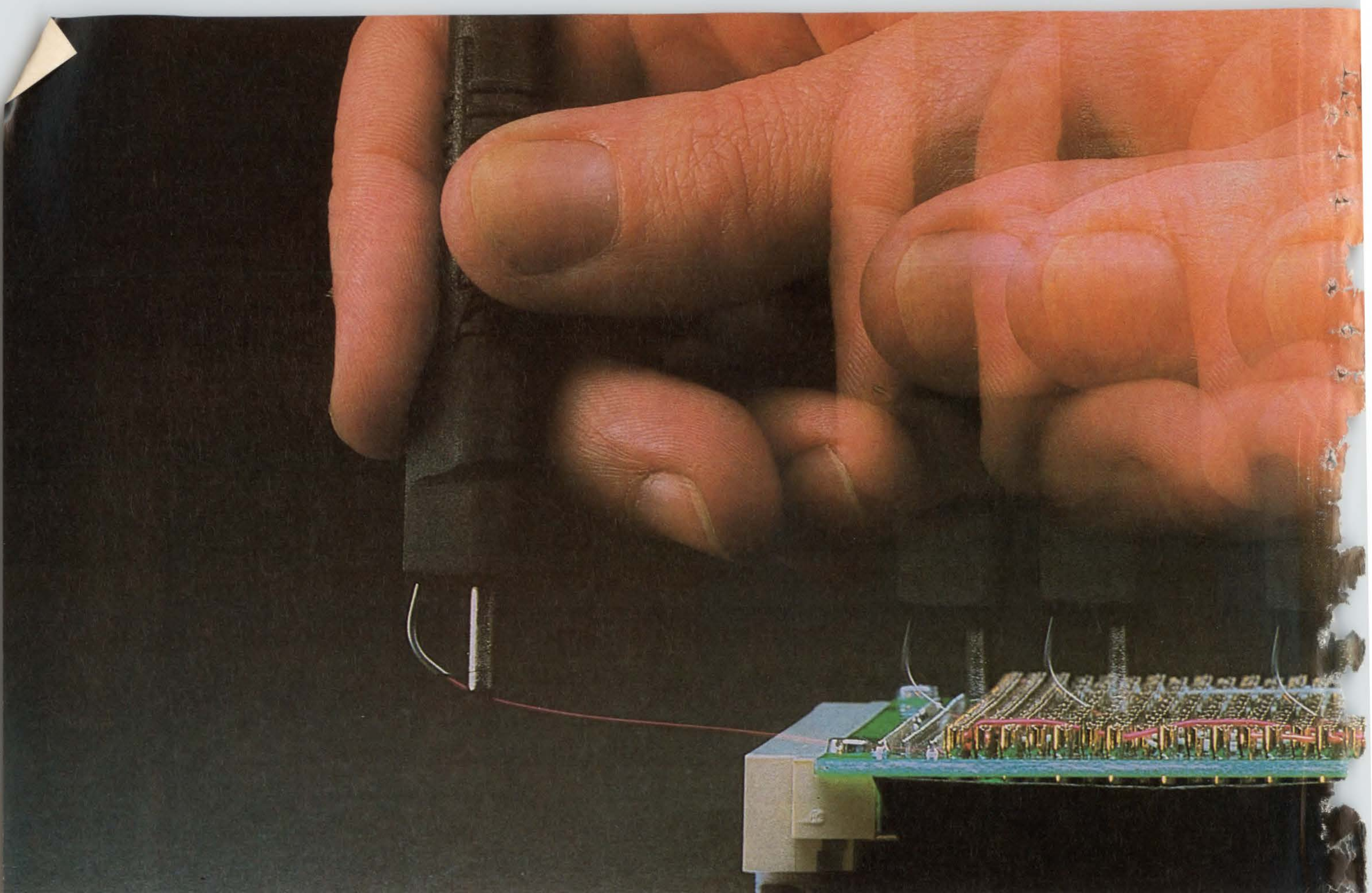
SPACE BLASTERS



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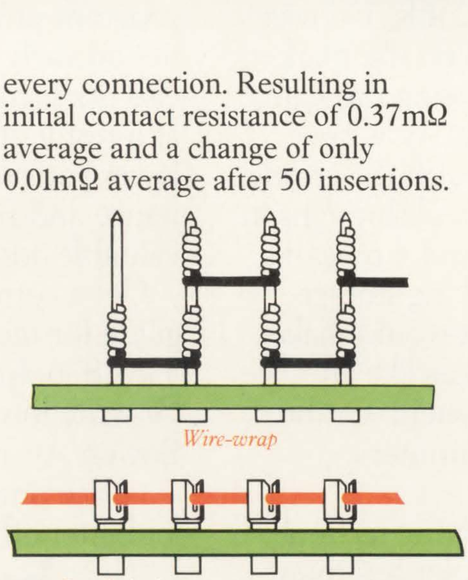

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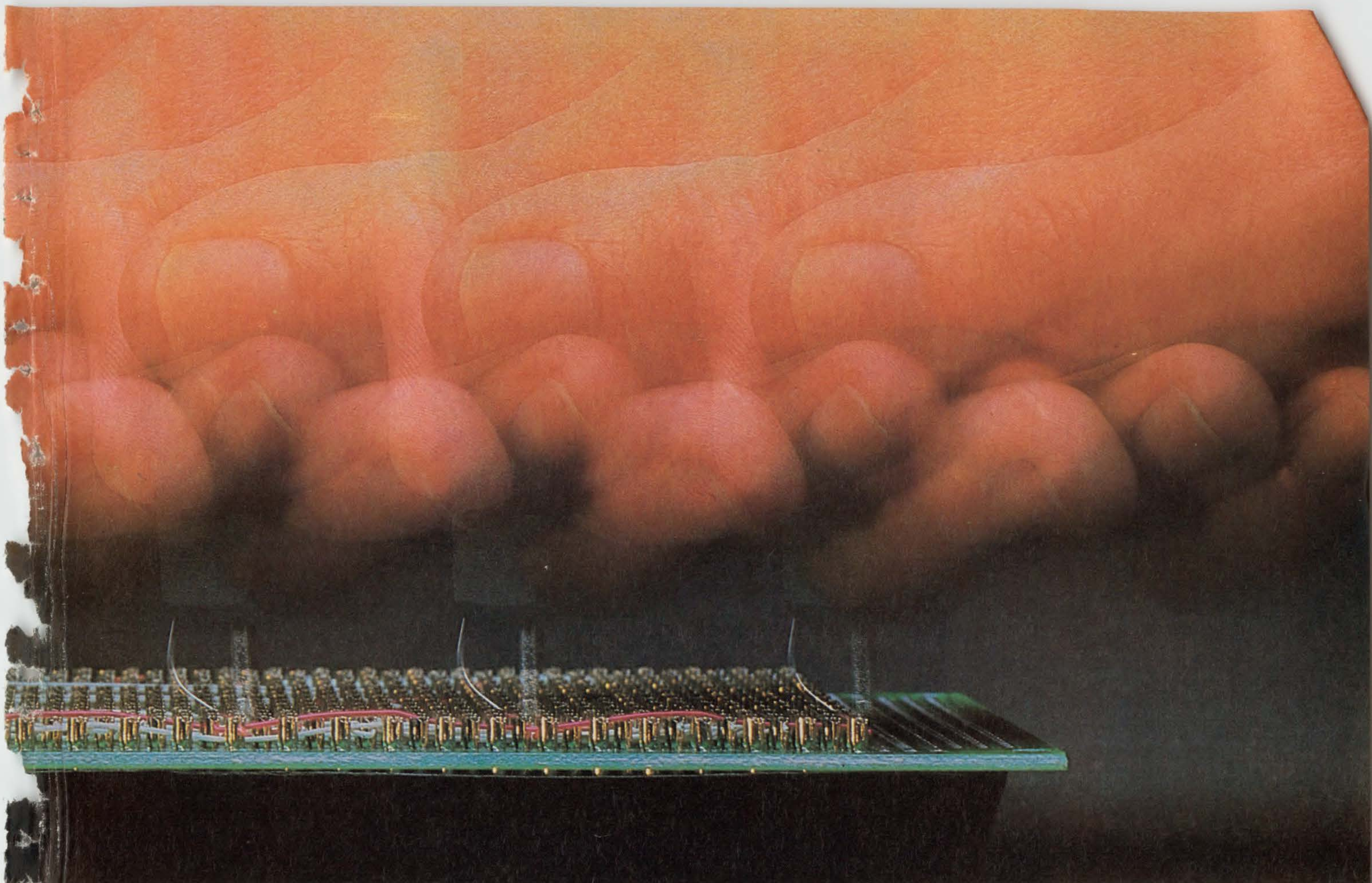

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CIRCLE 62

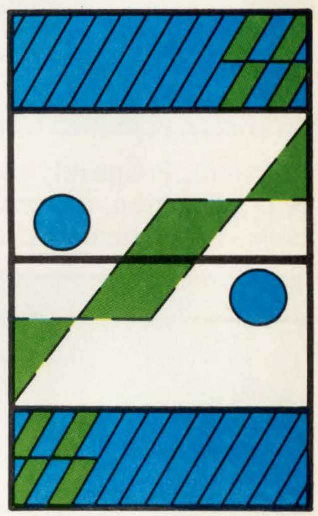
DOCUMENTATION— THAT MOST ONEROUS OF CHORES

Designers need not approach their documentation duties with fear and loathing. By applying the same structured techniques they use for hardware and software design to the manual, designers can become positively prolific.

by Thomas Jepsen

As engineering projects grow in size and complexity, their documentation is of increasing concern to engineering managers. Ad hoc documentation approaches that sufficed for smaller, simpler designs, are woefully inadequate for projects requiring the coordinated design and implementation of hardware and software. In fact, the design and implementation phases of development can suffer serious setbacks from the lack of a sufficient, well-written product definition. Corporate documentation standards are often outdated and inappropriate. In addition, most standard reference works on system design give little coverage to documentation. Thus, the responsibility for creating documentation often falls upon engineering personnel who are unprepared for the task.

In today's multifaceted engineering environment, documentation must be viewed as a design effort similar in concept to hardware/software design. As with hardware/software design, when structure and methodology are imposed, the end product exhibits fewer defects and is easier to maintain. The Table provides a comparison of structured and unstructured documentation methods, noting the advantages of the former.



With the advent of structured design techniques in both hardware and software, the notion of evolutionary design phases has become widely accepted. Implicit in this notion is the concept that each phase or step entails different functions. The phases common to hardware/software design find counterparts in documentation design as well. The predominant design phases include architecture, design, implementation, integration, test, and manufacture.

Individual documentation requirements form a hierarchy of documentation types with each document fulfilling a specific purpose (Fig 1). It is no more feasible to combine several documentation requirements in the interest of economy than it is to require the chief hardware designer to write all the software.

Thomas Jepsen is a senior technical writer at Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027, where he is responsible for documentation. At the time this article was written, Mr Jepsen was with the company's Microtechnology Div. He is currently with the company's subsidiary, STC Communications. Mr Jepsen has studied electrical engineering at the Milwaukee School of Engineering.

Documentation types

The functional specification is by far the most critical document in the entire design exercise. Yet, it is rare to find a functional specification that even marginally fulfills its basic purpose (ie, specifying

Documentation Scorecard Comparison

Project Milestone	Project A (Structured Approach)	Project B (Unstructured Approach)
Initial funding	Functional specification exists and is readable; upper management understands project and provides adequate funding	No functional specification exists; upper management rejects proposal (or provides inadequate funding)
Scheduling	Due to good documentation, milestones are identifiable	No well-defined schedule; many setbacks
Identification of functional requirements	All functional requirements are identified; responsibilities are clearly defined; project proceeds on schedule	Schedule setbacks occur due to discovery of missing requirements; staffing is found to be inadequate
Testing	Product is testable due to a good functional definition	Product is inadequately tested due to lack of functional definition
Manufacture	Easy transition to manufacturing environment; high reliability of shipped product	High failure rate in quality assurance due to nonstandard assembly, lack of standards
Marketing	Good customer acceptance due to readable end-user documentation and well-organized marketing strategy	Vague claims and misunderstandings
Installation/Operation	Product is easy to install and operate	Product is difficult to install; unforeseen operational problems
Maintenance	Excellent field support due to high quality documentation	Poor field support; many units returned to factory

function). Frequently observed defects include lack of organization, excessive detail, and the lack of a table of contents. User requirements and the limitations of current technology are two driving forces present during the architectural phase of product design. The functional specification is the primary means of establishing a compromise between these two forces.

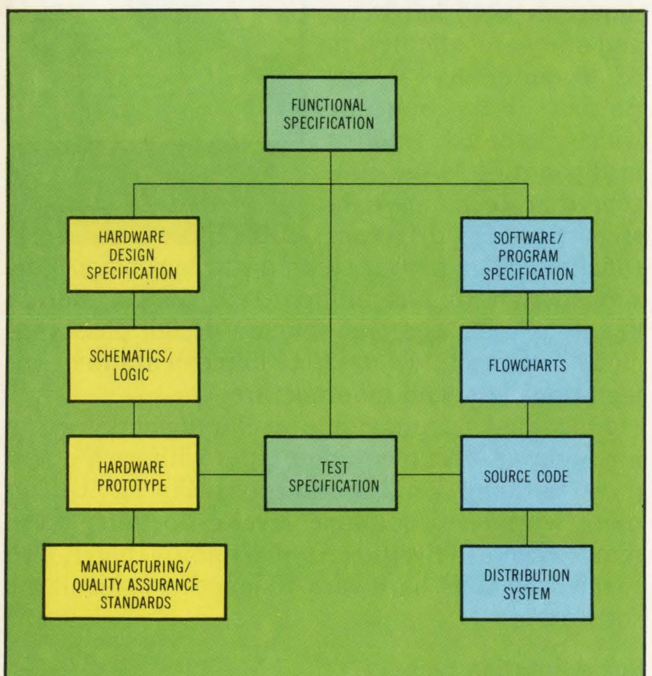


Fig 1 Each document in the documentation hierarchy has a particular purpose. Important to note is the central nature of the functional specification.

In some situations, the end user may directly supply system requirements in the form of a procurement specification. This is often the case with defense and other government projects. In other cases, a marketing organization that has determined a market exists for a particular system represents the end user. From a marketing standpoint, the definition of this system is often given in a marketing requirements or product objectives document. In either case, user requirements must be mediated by available technology limitations. From the user viewpoint, the ideal system performs all conceivable functions, is extremely simple to operate, and inexpensive to purchase and maintain.

Conflicts inevitably arise between system designers and end users (or their representatives) during the architecture design phase. Differing expectations cannot be ignored or left for later resolution. Failure to adequately define system architecture at an early stage often causes later problems.

A common tendency at this stage is to become immersed in the details of implementation, such as deciding which integrated circuit family or compiler/assembler to use. Exactly what constitutes implementation is often difficult to define and varies from one design project to the next. A good rule to follow is that a functional specification should not differentiate hardware-performed functions from software-performed functions. The functional specification refers to the entire system's functions, rather than to individual component functions.

Developing the documentation structure

A typical functional specification might consist of an introduction; a system overview; system interfaces; configurations; data flow and control flow; functional descriptions; performance requirements; reliability, availability, and serviceability; and a glossary of terms. The introduction describes, in simple and unambiguous language, what the system does. This point is often overlooked since it is easy to forget that first-time readers do not start out with a sense of the system's overall purpose. In addition, the original product concept is often vague and ill-defined. Putting it in writing aids in creating a structured product definition. The introduction should also define the functional specification's purpose, the document's organization, and the intended audience. Some functional specifications can be used for presentation to end users and customers. Others may be strictly for internal use.

In a system overview, the system is broken down into its functional components. Each component is described in summary format. For a complete computer, this section describes the processing unit, peripheral devices, main memory, the operating system (OS), and the functional software. For an OS, this section might describe job management, data management and storage management routines.

System components communicate with one another and with the outside world at a high level in the system interfaces section. For example, in a telecommunications network, this section defines the network data transfer protocol. For a computer system, it defines console communications abilities, channel interfaces, and teleprocessing features.

Most large systems can be configured in various ways, depending upon their application. All possible configurations should be defined, with emphasis upon maximum and minimum configurations. This includes the number of peripheral devices, the number of stations in a network, multiprocessing capability, and so forth. Fig 2 is a typical treatment of this documentation chore.

Structured programming concepts greatly emphasize the difference between data flow and control flow. Data flow describes the actual user data that the system processes. Control flow describes how data flow can be controlled or altered. The data flow section typically explains data format and structure while control flow explains the command structure. If elaborate descriptions of data formats or command listings are required, these descriptions can be made into appendices.

With functional descriptions, the terminology defined in preceding sections exhaustively lists system functions. Since all system components and interfaces have been defined, functions can be described as interactions between system components and the outside world. For example, if the function to be described is the creation of a file, then much information has already been defined. The system interface section, for instance, describes the user system interface that allows the user to create a file; the data flow section describes the format of the data in the file; the control flow section describes the command used to initiate file creation; and the system overview section describes the system components that must interact in order to create a file.

With this information, a functional description can be straightforward and use previously defined terminology. Fig 3 gives an example of a functional description using this approach. As shown in this figure, the user enters the FILE CREATE command at the console at 1. At 2, component F creates a

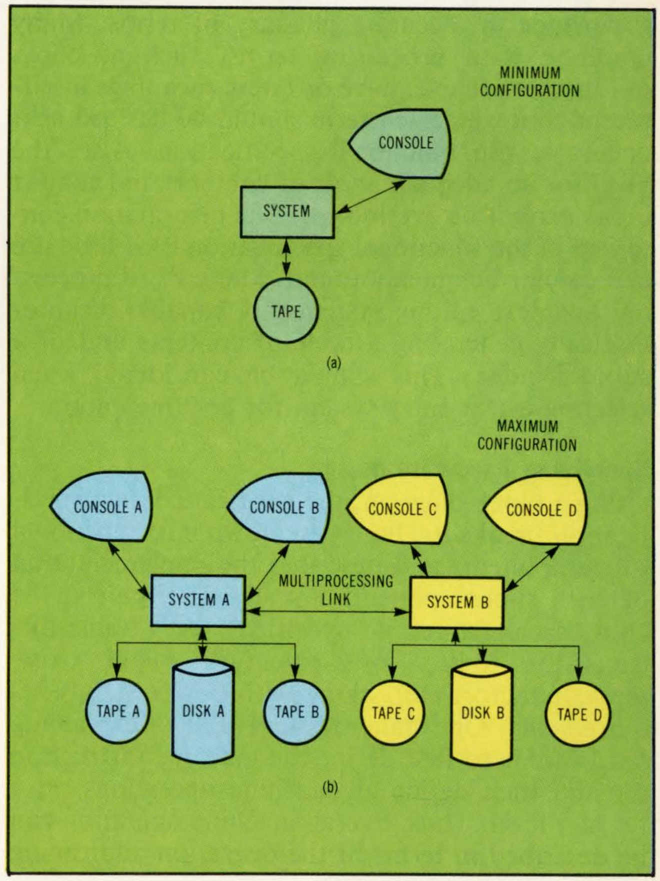


Fig 2 The system configurations section of the functional specification defines how possible systems can be best arranged, and emphasizes minimum (a) and maximum (b) configurations.

proper size data buffer. At 3, data arrive over the teleprocessing interface and are reblocked and placed in the buffer. At 4, component E begins input/output (I/O) protocol over channel interface Y and transfers the contents of the data buffer to disk. At 5, after successful completion of I/O, the response message is returned to the console. Otherwise, an error message is generated.

The numerically quantifiable requirements for proper system functioning are listed in the performance requirements section. Generally, performance is measured in terms of time, such as the number of required operations per second, or the length of time required to perform a specific function. Performance requirements must be based on actual user requirements. They must also be capable of verification by testing and/or benchmarking.

Reliability, availability, and serviceability must also be addressed. Required system reliability, such as mean time between failures, possible degraded mode operational scenarios, and anticipated maintenance support functions, are defined at a high level. Maintainability should be investigated at an early stage since special maintenance considerations can affect system architecture.

During systems documentation, it is important to include an accurate glossary of terms. Many common data processing terms, such as copy, modify, or archive, have different meanings in different contexts. Each term should be defined as it occurs in the functional specification. Also, the need for an adequate table of contents and subject index cannot be overlooked. The information contained in the functional specification is of little use if it cannot be quickly found. Many word processing and text editing systems are capable of automatically generating a table of contents and/or a subject index. This should be considered when selecting a text entry system for documentation.

Specifying hardware design

Using a block diagram, the hardware design specification breaks the hardware down into functional subcomponents and describes the implementation of each subcomponent. For digital circuitry, the chip architecture is specified (eg, transistor-transistor logic, complementary metal oxide semiconductor, etc), along with power supply requirements. One standard approach to explaining hardware is to first define the machine instruction set and then define all machine operations on a register level. Thus, overall machine operation can be described in terms of the operation and timing of individual components.

System timing is an important part of a design specification as well. System clocking, instruction cycle definitions, and memory access timings must be defined, preferably by means of timing diagrams. Fig 4(a) shows a typical hardware system laid out in a block diagram. Fig 4(b) supplies a register/component description.

An adequate bus structure definition is also critical. Often this becomes a separate, independent section of the design specification. Important items that should be defined include the number of lines, line definitions, signal levels, and bus protocol. In addition, for microcoded machines, the hardware design specification often defines the microcode instruction format and instruction set. For extremely complex machines, however, a separate microcode specification may be necessary.

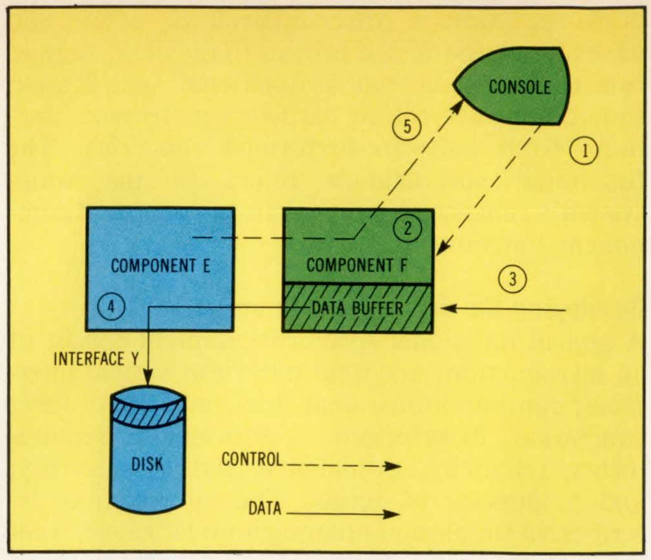


Fig 3 Pictured is an example of the FILE CREATE function. Using previously defined terminology helps describe system functions.

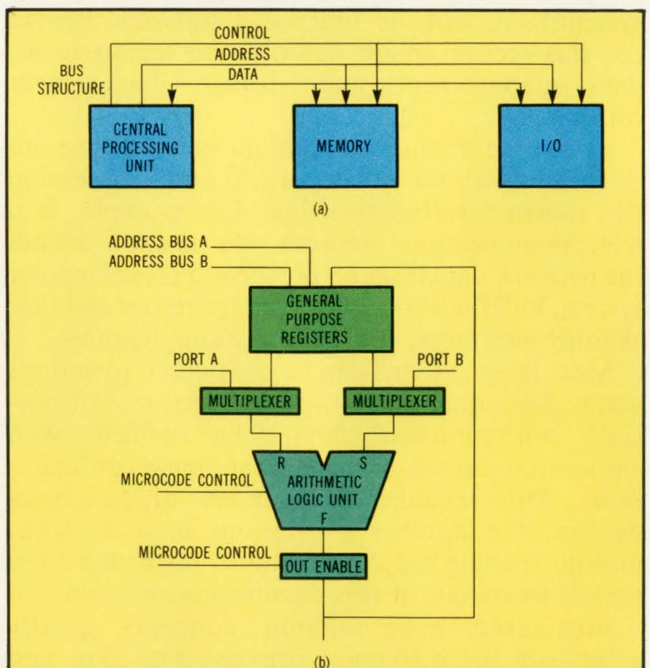


Fig 4 The hardware design specification should break functions down into a block diagram (a) and a register/component (b). Timing diagrams may also be included when necessary.

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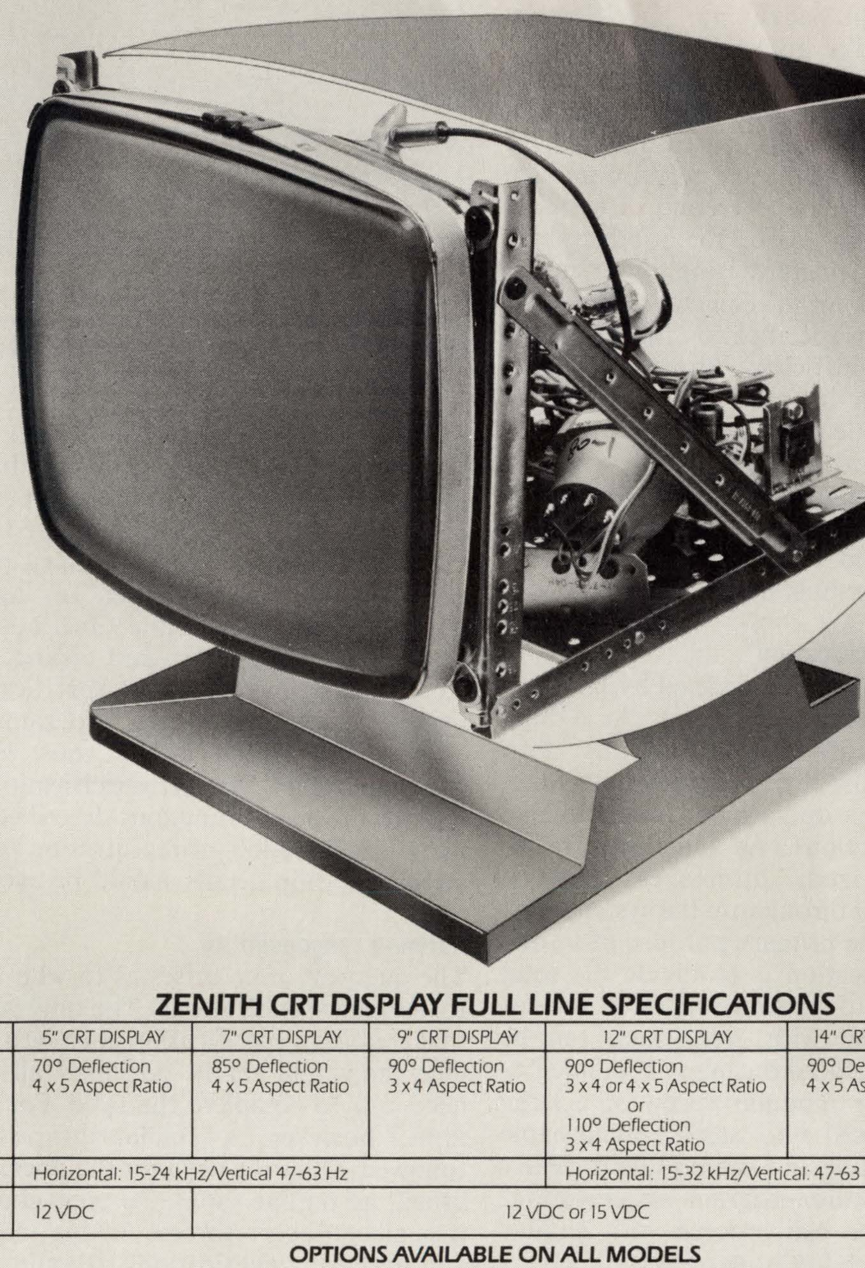

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Synchronization	Horizontal: 15-24 kHz/Vertical 47-63 Hz			Horizontal: 15-32 kHz/Vertical: 47-63 Hz		
Input Power Requirement	12 VDC	12 VDC or 15 VDC				24 VDC

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CIRCLE 64

One area often overlooked is physical/packaging specifications. This includes a description of the frame or card cage, printed circuit (PC) card requirements (physical dimensions, multilayer requirements), and physical layout of the hardware. In many cases, bus structure may dictate a preferred PC card arrangement for addressing purposes. This physical/packaging specification should be documented at an early stage.

Other areas that must be documented are power and environmental requirements. Depending upon where in the world the product is used, it may have to undergo Underwriters Laboratory, Canadian Standards Association or Verband Deutscher Elektrotechniker testing. Also, the product may have to operate under widely varying power conditions—an important point to remember. The completed hardware design specification must give the experienced designer sufficient information from which to draw a circuit diagram, and to begin construction of a prototype machine.

At this time, attention should also be given to design automation capabilities. If schematics or logic diagrams are to be generated using automated logic or computer aided design systems, the choice of an adequate system must be considered.

Software/program specification

System software functions are defined by breaking them down (ie, modularizing them). At a high level, this entails dividing functions into supervisor-state and problem-program-state functions, or into mainline operational functions and diagnostic mode functions. As functions are increasingly modularized, interfaces between modules and data flow throughout the system must be clearly defined. One primary purpose of a software/program specification is to divide the total development effort into separate units that various programmers can deal with, yet which can be readily and easily interfaced during system integration. Fig 5 shows the modularization of a large software effort (an OS) into small, manageable modules. If each module and submodule is clearly defined in the software/program specification, coding and integration can proceed with relative ease and a high probability of success.

The experienced programmer should be able to develop a software function flowchart directly from the information given in the software/program specification, and begin code module development. I/O data formats should be clearly explained. Programming language, coding, commenting, and flowchart development requirements must also be stated.

Moreover, a test method must be established to verify that the particular product performs as described in the functional specification. System testing usually consists of writing test programs to confirm various aspects of system functioning. This normally takes place after the hardware prototype and the source code have been separately developed, debugged, and integrated.

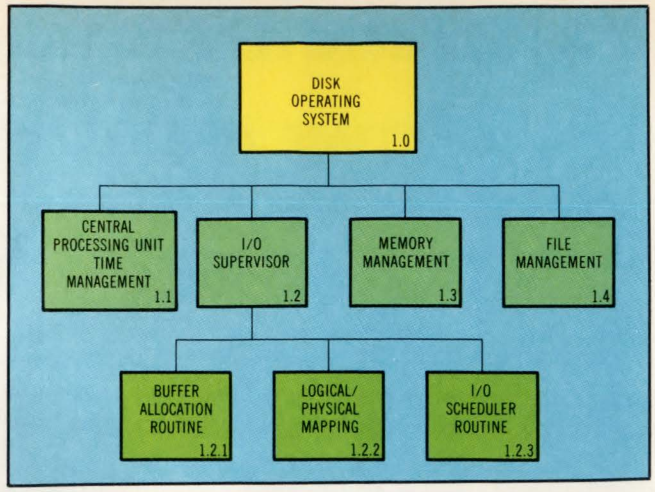


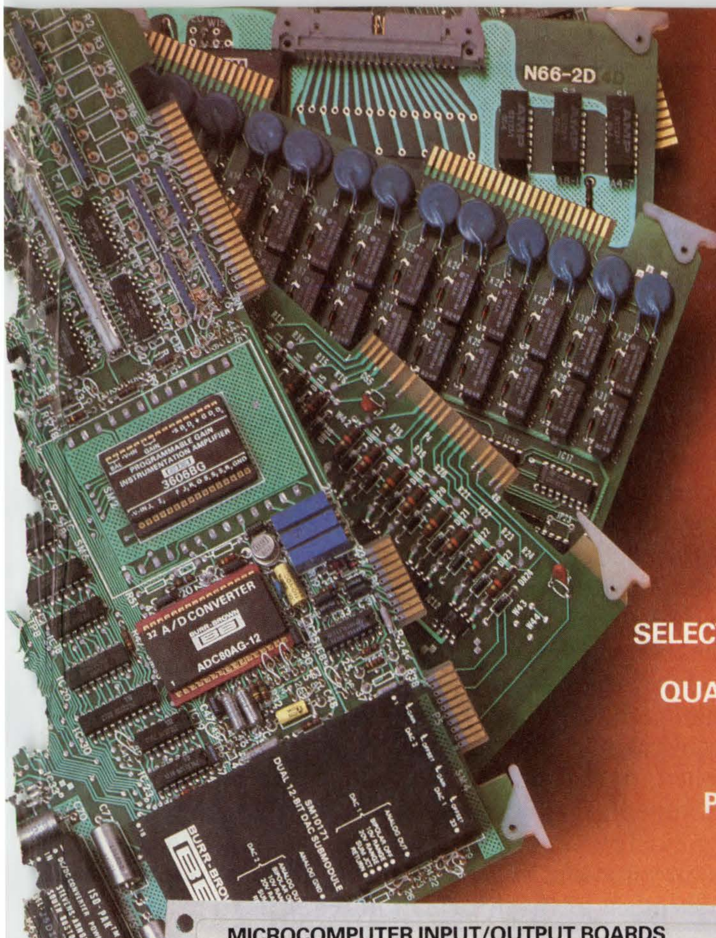
Fig 5 Breaking functions down into well-defined modules makes coding and flowchart generation easier. Software documentation is also served by a modular approach where each unit of code is clearly documented.

The test specification's primary purpose is to define an approach to testing. Testing can concentrate on verifying mainline functions through the use of test cases, worst-case testing, or a combination of the two. The test specification also describes the structure of test programs and defines dummy data structures that must be developed. Remember that the test specification must refer back to the actual functions described in the functional specification—concentrating on confirming implementation details should be avoided.

Defining responsibility

The question often arises as to who is responsible for writing specifications. The only good answer is that creating a specification must be a group effort. One individual rarely possesses all of the skills necessary to complete the task. For all specifications, however, a similar process should be followed. Once the need for the document is established, an outline should be created and reviewed, then all conflicts resolved. At this point, those with appropriate qualifications should write each individual section.

In general, the people responsible for product architecture should also be responsible for putting the functional specification together. All personnel that review product architecture should also review the document. Technical writers might be asked to provide support at various stages of document production. An experienced professional writer may be able to help with the outline and original structure of the document, and to provide editing support. Responsibility for the finished product, however, remains with engineering management.



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MP8418-PGA	15-channel Differential/31-channel single-ended, Fixed gain, 12-bit.
MP8418-PGA	15-channel Differential/31-channel single-ended, Programmable Gain, 12-bit.
	ANALOG INPUT/OUTPUT
MP8418-AO	15-channel Differential/31-channel single-ended input, Fixed Gain, 12-bit. 2-channel output, ± 10VDC, 12-bit (individual DACs)
MP8418-PGA-AO	15-channel Differential/31-channel single-ended input. Programmable Gain, 12-bit. 2-channel output, ± 10VDC
	ANALOG OUTPUT
MP8316-I	16-channel 0-20mA, 12-bit (common DAC).
MP8316-V	16-channel ± 10VDC, 12-bit (common DAC).
	SPECIAL PURPOSE INPUT
MP8430	16-channel RTD 3-wire (100 ohm or 1000 ohm).
	DISCRETE OPTICALLY ISOLATED INPUT
MP810	24-channel Dry-Contact Closure, 1.5mA Wetting Current at 24VDC.
	DISCRETE REED RELAY OUTPUT
MP802	32-channel Relay, 0.5A at 28VDC
	DISCRETE INPUT/OUTPUT
MP830-72	72-channel TTL levels. User configured in 8-channel increments of inputs or outputs.
MOTOROLA EXORCISER COMPATIBLE	
Motorola Exorciser, Rockwell System 65 and Synertek Systems.	
	ANALOG INPUT
MP7217	16-channel, single-ended, Fixed Gain, 12-bit.
	ANALOG INPUT/OUTPUT
MP7432-AO	32-channel Differential/64-channel single-ended inputs, Fixed Gain, 8-bit. 2-channel output, ± 10VDC, 8-bit (individual DACs).
	DISCRETE OPTICALLY ISOLATED INPUT
MP710	24-channel Dry Contact Closures, 1.5mA Wetting Current at 24VDC.
	DISCRETE REED RELAY OUTPUT
MP702	32-channel relay, 0.5A at 28VDC.
DEC LSI-11 COMPATIBLE	
LSI-11, -11/2, -11/23 PDP 11/03, 11/23	
	ANALOG INPUT
MP1216-PGA	16-channel Differential/32-channel single-ended, Programmable Gain, 12-bit.
ZILOG Z80 COMPATIBLE Z90, MCS	
	ANALOG INPUT/OUTPUT
MP2216-AO	16-channel Differential/32-channel single-ended inputs, Fixed Gain, 12-bit. 2-channel ± 10VDC outputs, 12-bit (individual DACs)

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CIRCLE 65

The review process is also important. Outside groups, such as field support and marketing, can provide valuable insight. In fact, as many outside groups as is practical should be allowed to participate in the review cycle. Reviewers generally suggest changes and make corrections. A revision system allows documentation updates—these revised documents should be circulated as often as required.

Responsible hardware/software managers should be in charge of writing hardware/software specifications. Since these specifications are generally for internal use only, and are primarily intended for specifying the design effort, their writing and review often takes place completely within the design/programming groups. A competent, experienced writer, however, can provide valuable support.

Once the design process is completed and manufacturing has begun, new documentation requirements emerge. The product must be installed, operated, and maintained in the user environment. If the design is adequately documented, a good foundation exists for generating end-user documentation. The design documentation provides much of the information required to produce marketing, installation, operation, and maintenance manuals. If adequate design documentation has not been prepared, however, user documentation is prepared in a react mode (ie, in response to demands from irate users).

In today's fast-changing, complex hardware/software environments, engineering managers must take a carefully planned, step-by-step approach to developing large systems documentation. Specifications that fulfill the requirements described result in a product that is fully functional, well-defined, testable, and relatively fault-free. It is also wise for designers to remember that if one of the system requirements cannot be adequately documented, it is likely that it does not exist in any useful fashion in the first place.

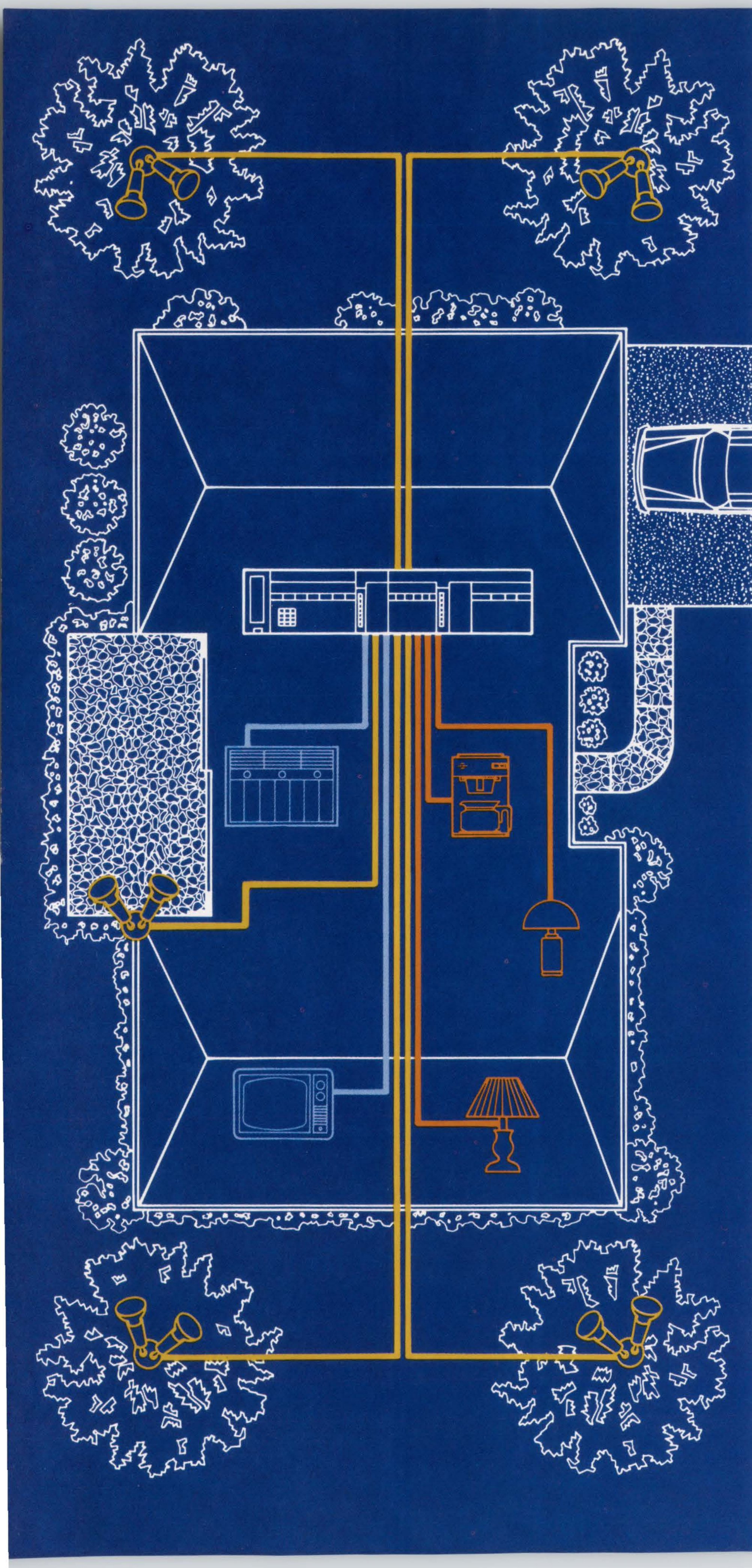
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 707 *Average 708* *Low 709*

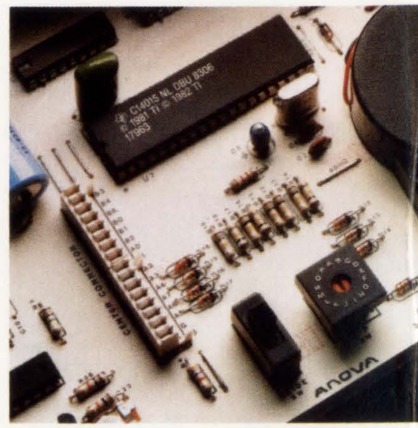
Texas Instruments and Anova team up for peace of mind when you're away... and extra convenience when at home.

- **High functionality, low cost** of TI's TMS7040 8-bit microcomputer contributes to Anova's pioneering intelligent electronic control for modern homes *(Page 2)*.
- **Two new additions** to TMS7000 single-chip microcomputer family combine outstanding NMOS performance with CMOS low-power dissipation *(Page 3)*.
- **Dependable, economical assistance** that helped Anova achieve cost-effective design is available from any of the TI Regional Technology Centers *(Page 4)*.

▶



Only TI's demands



It was a tall order. A microcomputer with large, on-board memory. On-chip timer. Sufficient I/O ports. With performance capability that would minimize hardware to hold costs down. And meet overall system size constraints. TI's TMS7040 8-bit, single-chip microcomputer fit the bill.

Result: Anova Electronics' sleek, new remote Control Center brings a greater degree of security to American homes and small businesses. Total convenience in the operation of lights and appliances. And significant energy savings. Whether anyone is on the premises or not.

Outstanding cost/performance ratio

The Anova Control Center handles up to 16 individual lights and/or appliances. Instantly. Or automatically by program which can vary from day to day. With immediate display of what's going on, including the status of each light or appliance.

The TMS7040 has 128 bytes of on-board RAM that readily accommodate all necessary programming. Plus 4K of on-board ROM which, with the TI TMS1000 4-bit microcomputers in the outlet modules, provide the intelligence for the "status" feedback.

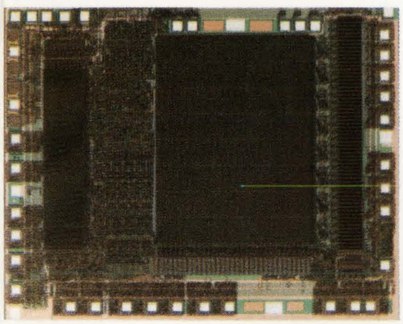
◀ **Electronic control of home or business** is now possible with new Master System designed by Anova Electronics. The Control Center utilizes TI's TMS7040 8-bit microcomputer to handle infinitely variable control of up to 16 lights or appliances. When Control Center is linked with Protection and Telephone centers, the highly functional TI microcomputer provides all necessary unification.

7000 8-bit μC passes stiff design of new Anova home control center.

TMS7000 Strip Chip Architecture yields smaller, microprogrammable chips.

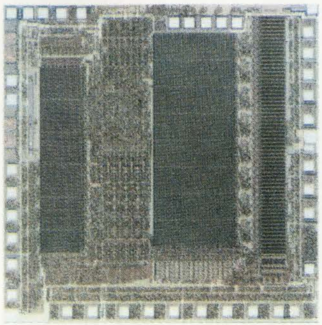
TI's unique Strip Chip Architecture Topology (SCAT) gives the TMS7000 family today's smallest 8-bit microcomputer chip. One that is low cost, microprogrammable, and that can be customized.

SCAT eliminates as much random logic as possible in favor of defined individual sections — such as control, ALU, and registers — for easy interconnection. For example, registers for the timer, I/O control, interrupt handling, ALU, etc., are arranged in a strip. Any additional 8-bit registers can be added to the strip with the eight interconnect lines already being available. There is no need for randomly locating additional registers and then routing interconnect lines all over the bar.



TMS7040 Microcomputer Strip Chip derived from TMS7020 Chip

SCAT allows TI to develop new family members easily from the basic TMS7000 chip. The TMS7040 microcomputer chosen by Anova was economically created from TI's TMS7020 by separating the memory border and inserting an extra 2K of memory.



TMS7020 Microcomputer Strip Chip

Another development using SCAT technology is TI's new TMS70120 microcomputer. The memory area has been expanded to 12K bytes of ROM and brings TMS7000 family advantages to a broad range of larger, more complex applications. Check your TI sales office for availability.

Because a control ROM replaces random logic for defining the instruction execution sequence, the original TMS7000 instruction set can be replaced by new, user-defined instructions. In some applications, such microprogramming can substantially enhance performance and improve the efficiency of on-chip program memory.

Contributing to TMS7040 functionality are 32 configurable I/O ports that permit the display and keyboard multiplexing. And, an internal, on-chip timer that provides for different delays within the software. As well as three fully utilized interrupts.

So much functionality packed into a device enabled Anova to hold parts count down, simplify its design, maximize reliability, and achieve cost goals.

Effective design help from Regional Technology Center

In designing the trim, compact Control Center, Anova relied on TI's convenient Regional Technology Center.

Anova engineers determined what functions the Control Center was to perform — defined the specifications — and left the development of the software code up to the specialists at the TI center. For both the TMS7040 and TMS1000 microcomputers.

By contracting to have the center perform the programming, Anova was able to utilize its engineering staff more effectively. And eliminated the need to invest in a development system.

For more details on TI's growing TMS7000 8-bit and popular TMS1000 4-bit microcomputer families, check numbers 1 and 2 on the coupon.

New TMS7000 members combine CMOS/NMOS advantages.

Well suited to telecommunications, portable instrumentation, and high-performance consumer products are two unique additions to the TMS7000 series. Both combine the performance capabilities of TMS7000 NMOS microcomputers with a CMOS typical power dissipation of only 50 mW at 5 volts. Reducing power even further are a "wakeup mode," dissipating 4 mW (typical), and a "halt mode" that typically requires only 2 mW.

The new TMS70C20 is a CMOS version of the TMS7020, with 128 bytes of RAM, 2K bytes on-chip ROM, 3- to 6-V operation, and 3 MHz nominal operating frequency.

The new TMS70C00 is a ROM-less 8-bit microcomputer intended for software development.

Engineering samples of both the TMS70C20 and TMS70C00 are available now in 40-pin, 600-mil, dual-in-line plastic packages.

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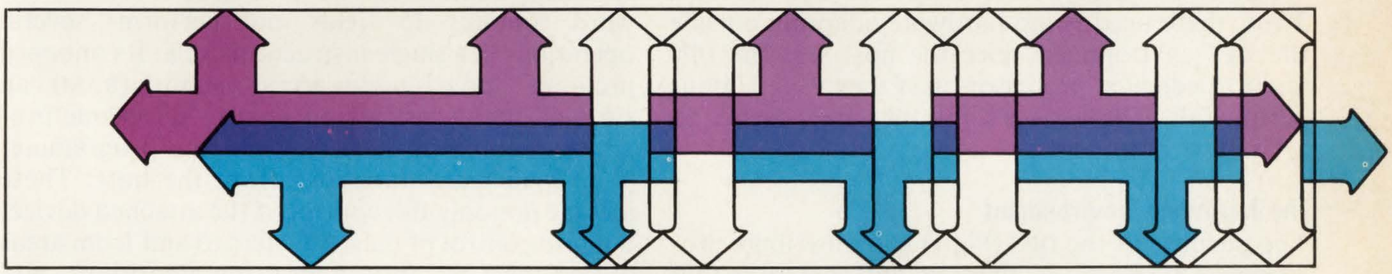
A serial port in TI's new TMS7041 microcomputer enhances I/O and communications capability. Otherwise identical to the TMS7040, the TMS7041 operates in several modes. One permits interface with Universal Asynchronous Receiver/Transmitter (UART) peripherals as well as multiple microcomputers. Serial links are implemented by standard asynchronous protocols. In the unique "isosynchronous mode," transmission rates are 16 times those of the asynchronous mode. A serial I/O mode can be used to expand I/O lines using external shift registers and to communicate with peripherals requiring a non-UART serial input. Check with your TI sales office for details on availability.

A FLEXIBLE ENVIRONMENT FOR HIGH SPEED COMPUTING

A peripheral system of tightly coupled processors and high speed mass memory can attack large computation chores by relieving the host of most control tasks.



by Gary L. McAlpine and Gerald B. Feldkamp

The headaches involved in running complex scientific programs in image processing or seismic data interpretation are many. Most prevalent are the host overhead and input/output bottlenecks encountered in getting data first into the system, then into the processing format an array processor requires. Even when the array processor is capable of very high speed computation, keeping it fed with data often proves impossible.

In most processing situations, even 32-bit superminis contend with a great deal of host overhead and memory use. The host is in charge of loading programs into an array processor. Moreover, host memory must be allocated to read data in from a disk or tape drive. Also, the host must send data to the array processor and then accept the results into its main memory. Further processing and buffering are usually necessary before the desired results are achieved, and every step devours host processor time, input/output (I/O) channels, and expensive peripherals. The net result is that many host resources are unavailable while numbers are being crunched.

But why not offload host control of peripherals while simultaneously allowing them to work at their full potential? This can be accomplished by providing dedicated control processors for each device and intelligent memory buffering along with high speed addressing, data transfers, and formatting. In addition, why not provide general-purpose hardware that can be tailored along broad lines to suit an application? The hardware world thus created can then be further defined by software to optimize resources and eliminate the throughput bottlenecks with minimal host intervention.

Aptec's Dimensional Processing System does exactly that. It is designed to connect to Digital Equipment Corp PDP-11 or VAX-11 computers using

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Gerald B. Feldkamp is currently manager of software development at Aptec Computer Systems. He is responsible for DPS-2400 software design and development. Mr Feldkamp holds a BS in computer engineering and an MS in communications engineering, both from the University of Michigan.

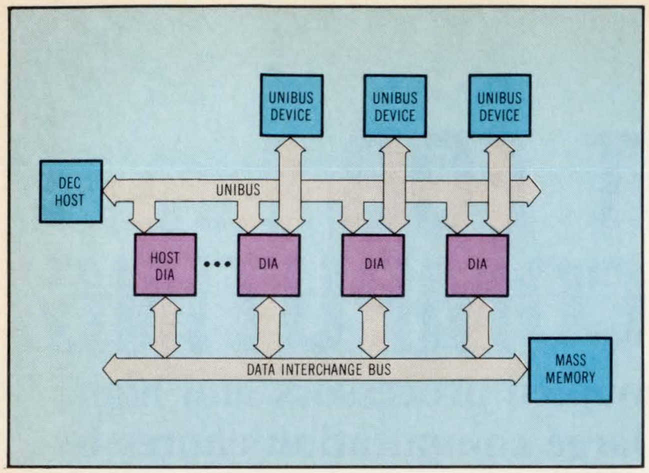

Fig 1 As shown in this DPS-2400 system block diagram, the host can access Unibus devices by calls or programs in the DIAs, or, directly in the hardware transparent mode, via a host-resident driver.

DEC's Unibus. Devices used with the DPS attach to connections that look exactly like the Unibus. Thus, there need be no hardware adapting outside the DPS environment since the host sees the DPS and its dedicated processors as if they were Unibus peripherals. The devices think they are attached to a Unibus computer.

The hardware environment

The purpose of the DPS (Fig 1) is to distribute processing, I/O resources, memory, and control so that attached Unibus devices can be maximized. That is, data transfers can be conducted at full speed without the usual performance degradations arising from operating system overhead and device contention.

Each peripheral is connected into the DPS through a dedicated processor, called a data interchange adapter (DIA). The DIA accesses the Unibus registers of the attached device via a private bus that is not directly connected to the host. Connection to mass memory in the DPS is via an internal, 32-bit wide, 24M-byte/s data interchange bus (DIB). In addition, DIAs are Unibus devices and thus connect to the host through the Unibus. A DIA hardware transparent mode is also available wherein the standard host device driver can control the attached device without any DIA hardware interference. This is essential if an evolutionary path to using the DPS is to exist.

Mass memory consists of up to 27, 1M-byte, plug-in boards with onboard error detection and correction circuitry. Although up to 27 boards can be plugged into a full-blown system, some slots are reserved for DIAs. For each DIA needed, one less memory board can be included. Therefore, while broadly configurable because of the emphasis that can be placed on the number of attached devices or the amount of memory, the DPS is obviously not really application specific.

All DIAs are physically identical (Fig 2). Each is built around a 2901 bit-slice bipolar processor capable of both 16- and 32-bit integer operations. Every processor accepts interrupts from any devices including other DIAs. A DIA's 48-bit instruction word contains 15 fields and performs several operations in a single instruction cycle. Its onboard program source random access memory (RAM) can store 4K 48-bit instruction words. Microcode programs residing in the DIA allow the programmer to offload many functions from the host. These include not only full control of the attached device, but also control of data transfers to and from areas of DPS mass memory, addressing algorithms, and on-the-fly data formatting.

The types of programs residing in the DIA include device specific drivers, various utilities, a standard monitor program call Diamon, as well as an interpreter, called STAPLE (Structured Application Language and Executive). This interpreter runs DIA control programs. One system DIA is always defined by software as the host DIA (HDIA) and is the host's port into DPS mass memory. By convention born of practicality, no device is attached to the HDIA.

With DPS, a system can be designed in segments by adding DIAs with attached devices and 1M-byte

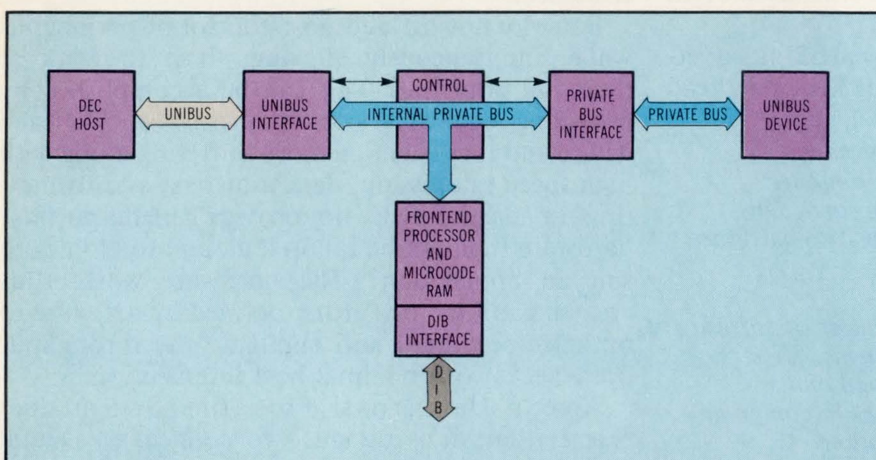

Fig 2 This DIA block diagram reveals that an internal private bus allows 3-way data transfers. In the hardware transparent mode, the host sees the device exactly as if it were on the Unibus. Host access to DPS mass memory, however, requires using host DIA routines. The microcode RAM stores microcode modules called by the host or by STAPLE.

increments of mass memory. Thus, mass storage (tape and disk) and array processors can be added without eliminating the general-purpose hardware environment. At the same time, hardware, such as data acquisition or imaging systems, can be added for specialized applications. Any given DPS configuration can be easily changed to suit a different set of applications by loading different microcode modules into the DIAs' program source memory.

The modular nature of the DPS and the general nature of DIAs give programmers access to all hardware capabilities and allow them to use those capabilities via software. It is possible, for instance, to use the processing and communication abilities of the DPS to apply multiple array processors to the same computation, dramatically improving throughput. Users can also implement a variety of buffering and I/O schemes to smooth data flow among buffers in mass memory and peripherals.

The basic approach to programming an application using the DPS is to distribute a very large job among tightly coupled processors. Each part of the job is assigned to that processor controlling a device best suited to the task. The programmer's job, then, is to coordinate the data flow among peripheral processors, DIAs and their attached devices, mass memory and its buffers, and the host.

An imaging application using radar data highlights a number of DPS uses. Such a signal processing task requires several manipulations of a very large set of complex data. In its raw form, radar data collected from a flying aircraft consists of a set of data points positioned at the intersections of a polar grid. To produce an onscreen image, however, the collected data must first be processed to form a rectangular grid of data points upon which a 2-dimensional fast Fourier transform (FFT) must then be performed. At this point, results can be sent to an image display system.

The basic task is to ensure a continuous flow of data in its raw form.

Such a task typically requires taking a raw data set of 18M complex points—or 36M bytes—and producing a 1024 x 1024 byte image that a human can analyze. Implicit in this task is interpolating the polar-arrayed data to roughly 8M data bytes lying on a rectangular grid. While complex, the actual processing is a familiar problem and can be attacked with a minicomputer and an attached array processor.

However, the sheer mass of data brings with it buffering, I/O control, and formatting problems. In such data manipulations, even the most powerful array processors work at a fraction of their potential speed, thus taking an excruciatingly long time to produce meaningful results. To some extent, dedicating disk and tape devices to the array processor might mitigate the dilemma. This approach, however, risks denying these expensive resources to the host and to other users.

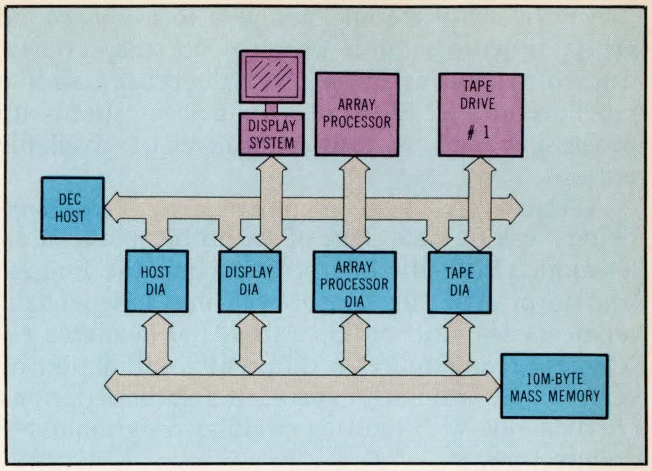

Fig 3 This DPS system configuration can handle a radar signal processing problem. The DIAs required take 4 of the 27 available expansion slots so there is room for up to 13M bytes more DPS mass memory.

One possible DPS configuration designed to address this problem is shown in Fig 3. Note that with the exception of the image display system and its connected DIA, the arrangement represents a fairly general-purpose system. In the event some future specialized tasks arise, the display system need only be detached and its DIA used for whatever device replaces it.

Since it is impossible to dump 36M bytes of data into mass memory at once, the basic task is to ensure a continuous flow of data in its raw form on tape to buffer areas in DPS mass memory. Data can then be sent to the array processor for interpolation into rectangular form. This reduced data can be stored in an 8M-byte buffer representing one grid. Once the 8M-byte buffer has been filled, its contents will be passed once again through the array processor for a 2-dimensional Fourier transform and scaling to produce a 1M-byte data set. In turn, the display's DIA will send this set to the display system.

Various I/O and control tasks are assigned to several DIAs. The tape and array processor DIAs share two buffers for records read from tape; while one fills, the other is read. These two DIAs can share a synchronization flag in mass memory that indicates which buffer is full. The array processor's DIA will also write its first results into the 8M-byte buffer. When that operation is completed, the 2-dimensional Fourier transform and scaling can be carried out on that buffer. The final results are sent out to the 1M-byte buffer where the display's DIA picks them up for transfer to the display.

Another choice could be made to use a second array processor and DIA to do the Fourier transform, thus using the two array processors in a pipelined mode. Such an arrangement speeds up processing and is also indicative of available options.

Alternatively, two or more array processors might work on each stage of the problem in a parallel mode. Both the interpolation and the Fourier transform problems can be split into independent segments for distribution across the available resources. This requires a different combination of steps, flags, and buffer space; but all these options are available with the DPS modular programmable architecture.

However, once an analysis of the problem has led to a decision on the hardware configuration and processing task allocation, attention must turn to programming. The objective is to set up the DPS so that a simple command from the host puts it in motion. The host need not be disturbed again until the job is done or the subsystem has intermediate results to pass back to the host. The general-purpose software modules available to do this reside in three places: on the host computer, in each DIA, and in DPS mass memory.

The software environment

The host computer has access to the DIAs through a host software driver that supports the DIAs as Unibus devices. Similar to many other device routines, application programs running on the host computer can send calls via the driver to a given physical device (in this case, a DIA). Such calls can request services or simply start a program that can then run entirely within the DPS. To address DPS mass memory, the host must also go through this driver and through a DIA because DPS mass memory is not connected directly to the Unibus.

The real heart of the DPS software resides in the program memory of the individual DIAs in the form of DIA program source (PS) load modules. Load modules consist of various pieces of microcode that fall into four major categories: the DIA monitor program, Diamon; various utility routines for data transfer between host, DIAs, and mass memory; device-specific routines; and the STAPLE interpreter mentioned earlier. The DIA PS modules are loaded into every DIA. Each module contains an identical copy of Diamon and the STAPLE interpreter along with other microcode modules as needed.

This STAPLE interpreter executes programs stored in mass memory. Such programs usually call on microcode routines and utilities stored in the DIA. STAPLE is a high level structured language akin to Rational FORTRAN (RATFOR). STAPLE programs are written, compiled on the host into pseudo-object code, then loaded into a file area in DPS mass memory. The DIA-resident STAPLE interpreter reads and executes the pseudocode on host command.

The real heart of the DPS software resides in the program memory.

Since Diamon's major responsibility is to communicate with the outside world, it interfaces with the host-resident driver and accepts calls to run microcode subroutines linked into the DIA's PS load module. A microcode library of commonly used routines—especially host/mass memory data transfer routines, as well as several that allow a Floating Point Systems array processor to read and write mass memory—has been developed for the DPS. With no device attached, the HDIA contains all the microprograms needed for host/mass memory transfer in its load module. Additionally, the user can write device or application-specific microcode to link into the load module with Diamon and STAPLE.

DIA runtime microcode is presently available in the library of general DIA primitives and DIA I/O primitives. In addition, a set of special mass memory I/O routines has been developed for FPS-100 and AP-120B array processors. These routines enslave the DIA to the array processor. In this arrangement, the array processor issues I/O commands to the DIA for reads and writes to DPS mass memory. The user can also write specialized microcode via the DIA assembler and linker on the host. Examples of DIA I/O primitives provided in the microcode library are H2MM16, which transfers buffers of 16-bit data from the host to DPS mass memory; and PB2MM32, a utility that moves 32-bit data directly from the DIA's private bus (to which a Unibus device is attached) into DPS mass memory.

Microcode routines linked into DIA PS modules can be run via calls passed to Diamon from the host driver or via calls issued by a STAPLE program. To execute from the host, Diamon receives the task's name from the driver and attempts to match it to its table of available routines. On making a match, Diamon accepts any arguments to be passed to the called routine, which executes, returns output parameters, then transfers control back to Diamon. Users can easily begin working with DPS-2400 by calling DIA microcode routines directly from FORTRAN programs via the host driver. Later, they may wish to let an increasing number of operations migrate into the DPS itself in the form of STAPLE programs.

Although the 4K-word program space on the DIAs is sufficient for quite a bit of microcode—certainly enough for very sophisticated device drivers—needs


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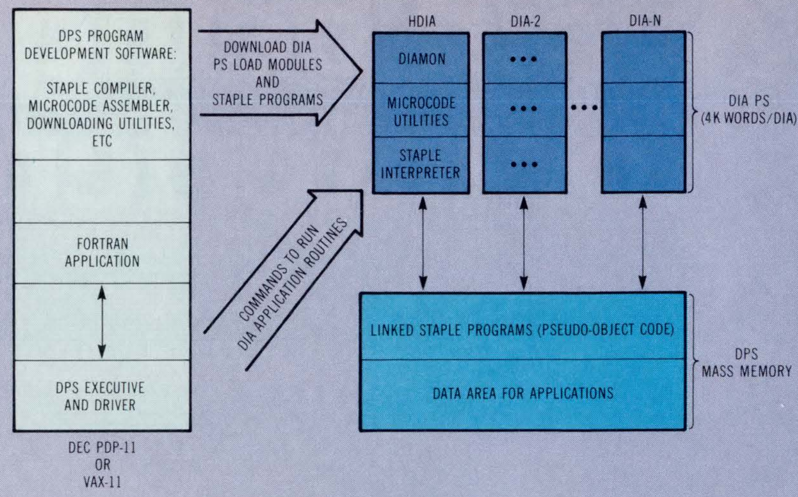

Fig 4 The DPS software organization depicted reveals an interpretive approach to program execution. STAPLE programs can, however, easily call onboard microcode routines for increased efficiency. Software development is considerably simplified by the high level programming language.

will most likely arise for rather complex buffering, flag sharing, and interaction of multiple devices and DIAs. This will require more program space than available on the DIAs. Therefore, a block-structured language, DIA-STAPLE, was designed to use DPS mass memory as its program storage and to provide high level control structures. STAPLE simplifies the programming of complicated control and synchronization operations required in advanced applications.

Programs running in the STAPLE interpretive environment are not cross-compiled into DIA machine code, but into a pseudo-object code to be executed by the interpreter. STAPLE programs compiled on the host are downloaded into the file area in DPS mass memory using a host-resident utility. Here, they are available to all DIAs. All microcode routines called by a STAPLE program must be resident in the PS DIA's memory, which runs the STAPLE routine. An overview of DPS software organization is given in Fig 4.

There are trade-offs inherent in using the STAPLE interpretive approach. On the plus side, users can program in a high level language and applications can grow without regard to the finite size of PS memory. On the other hand, using an interpretive approach is slower than running machine code directly on the DIA, though integer operations run at speeds comparable to similar operations coded in DEC PDP-11 assembly language. Users, however, have the opportunity to optimize application programs by properly balancing the STAPLE code and certain microcode routines that may be chosen for hand coding some speed-critical operations.

Using the system intelligently

Obviously, using the DPS-2400 requires several considerations. First, some rather general decisions must be made concerning the amount of mass memory needed and the type and number of attached devices required. Remember that each device requires its own DIA, plus an additional DIA to serve as the HDIA. Once defined, the hardware configuration can be easily expanded with additional devices and/or 1M-byte memory boards.

Software is another consideration. As indicated, the load modules must each contain, in addition to Diamon and STAPLE, all those microcode routines and utilities that the system manager anticipates will be needed. System users can choose to interact with devices attached to DPS transparently. Access can be gained to DPS devices via standard FORTRAN programs or by calling DIA device-specific microcode routines via the host based DIA driver; STAPLE programs can also provide access. Users can develop new microcode required to meet special speed-critical operations; the appropriate DIA PS load modules should then be relinked and reloaded into the affected DIAs and tested. These options provide an evolutionary path so that existing FORTRAN programs can use DPS with very little modification. Later developments can be implemented in STAPLE or special microcode as the user sees fit.

For instance, in the radar imaging example, the hardware selected uses about 10M bytes of mass memory, one tape drive, one array processor, and one image display system—for a total of four DIAs including the HDIA. Routines for reading and writing between the array processor and mass memory, and between tape and mass memory, are included in the function library. These routines can be linked into the load modules for those devices' DIAs. At this point, display system routines have to be user programmed in STAPLE with calls to some combination of new and existing microcode routines. Of course, the HDIA contains all needed memory transfer and allocation routines.

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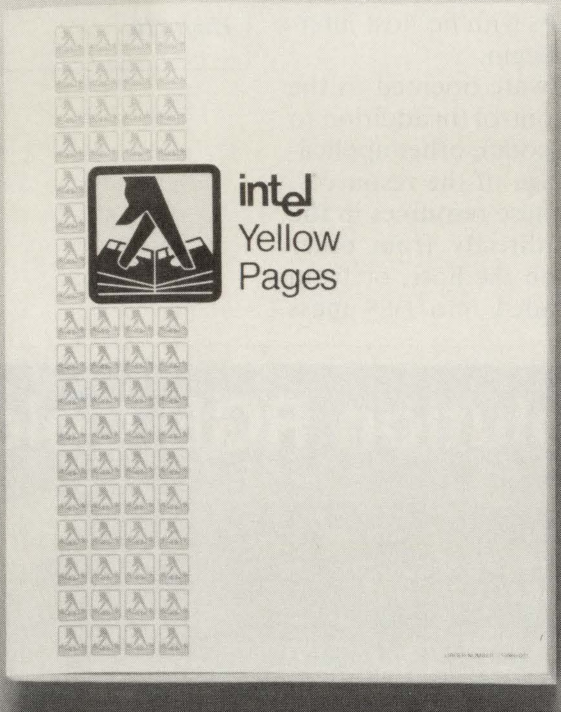

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To read and process the raw data, the programmer needs to write and compile a STAPLE program to read the tape, and a program to do the interpolation and FFT computations. The array processor DIA will operate in the slave mode, accepting I/O requests and conducting the data transfers between the array processor and mass memory. In this limited example, it would be possible to read an entire 36M-byte file from tape, perform the buffering, interpolation, Fourier transform, and display of a single image entirely on the DPS with no host intervention beyond the signal to begin.

Since the DIAs contain software oriented to the functions of the devices they control (in addition to any application-specific microcode), other applications can readily take advantage of the resources. The system manager defines these resources in the DIA PS load modules either directly from other FORTRAN programs running on the host, or from other STAPLE procedures loaded into DPS mass memory. Thus, the flexibility inherent in the DPS-2400 system extends from the general hardware definition through DIA device-specific programming to application coding. System designer priorities determine hardware choices and application needs. Application programmers can, by choice, work in a well-defined context—at a high level if they do not use optimization options in microcode. Thus, application coding, predicated solely on the requirements of the problem and the abilities of the hardware, is finally a reality.

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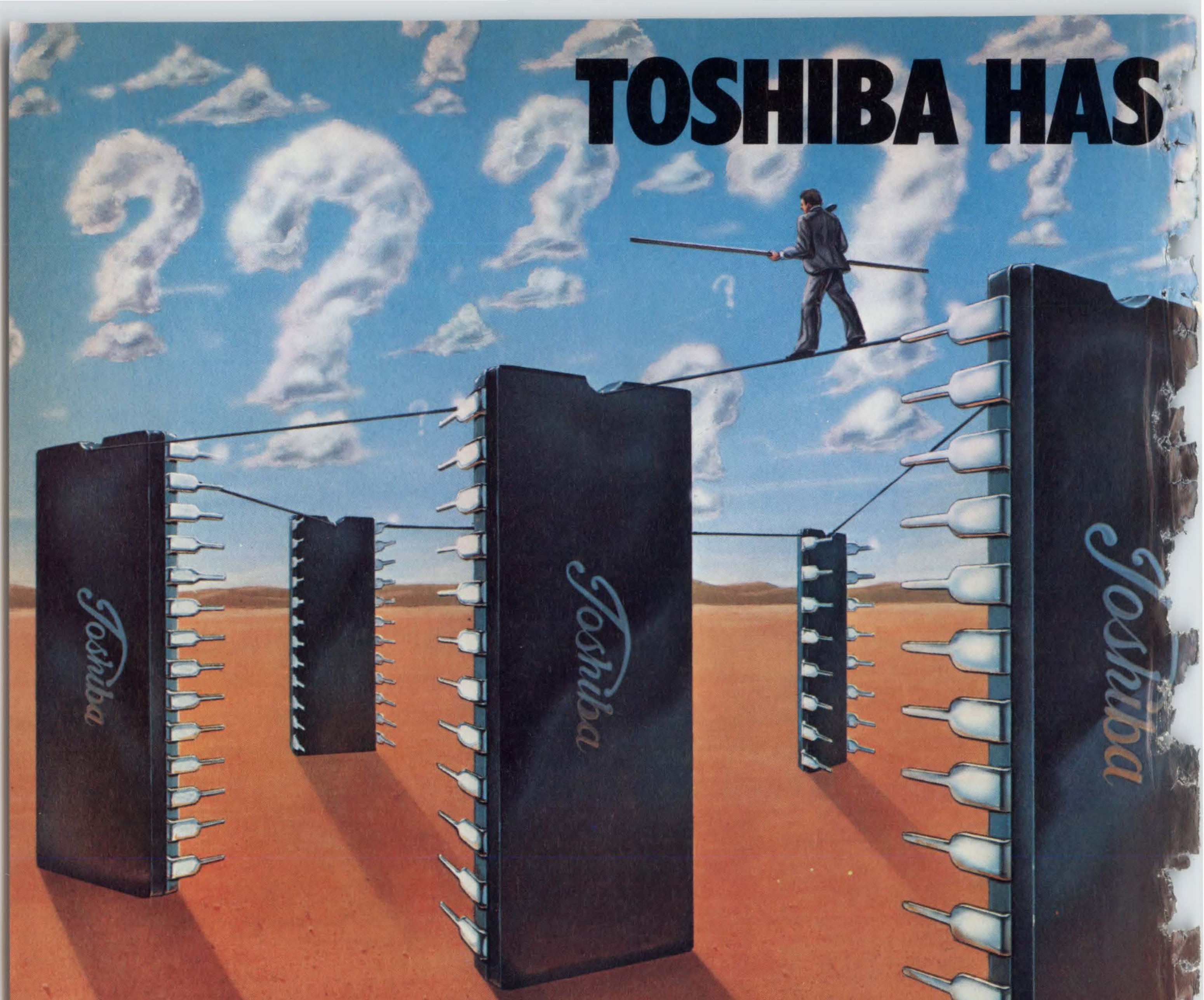

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Quiescent Power Diss. (typ) (GATE)	0.01μW	8mW	0.01μW	0.01μW
Noise Margin V_{IH} (min)/V_{IL} (max)	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current $\|I_{OH}\|$ (min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
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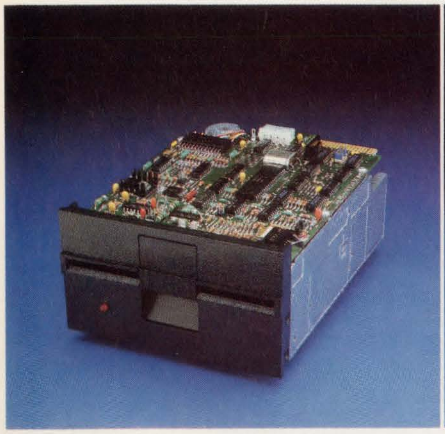
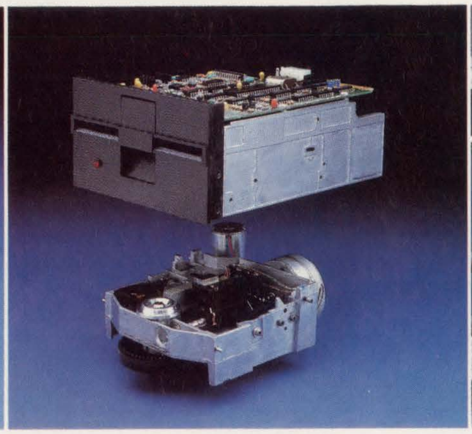
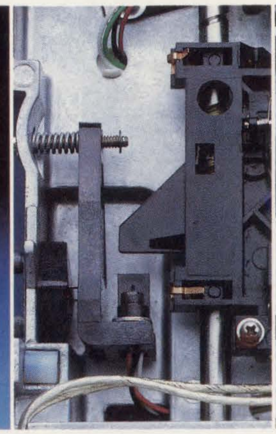


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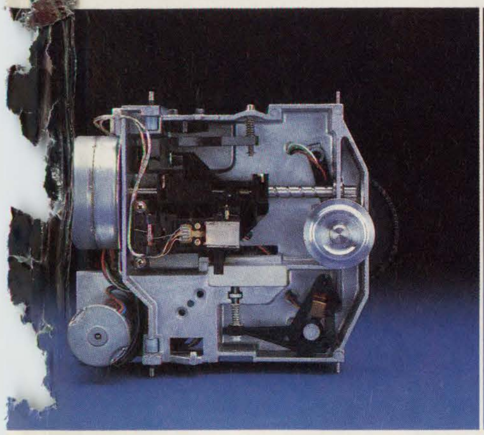

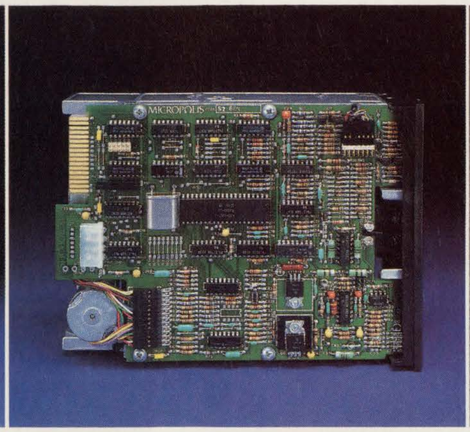

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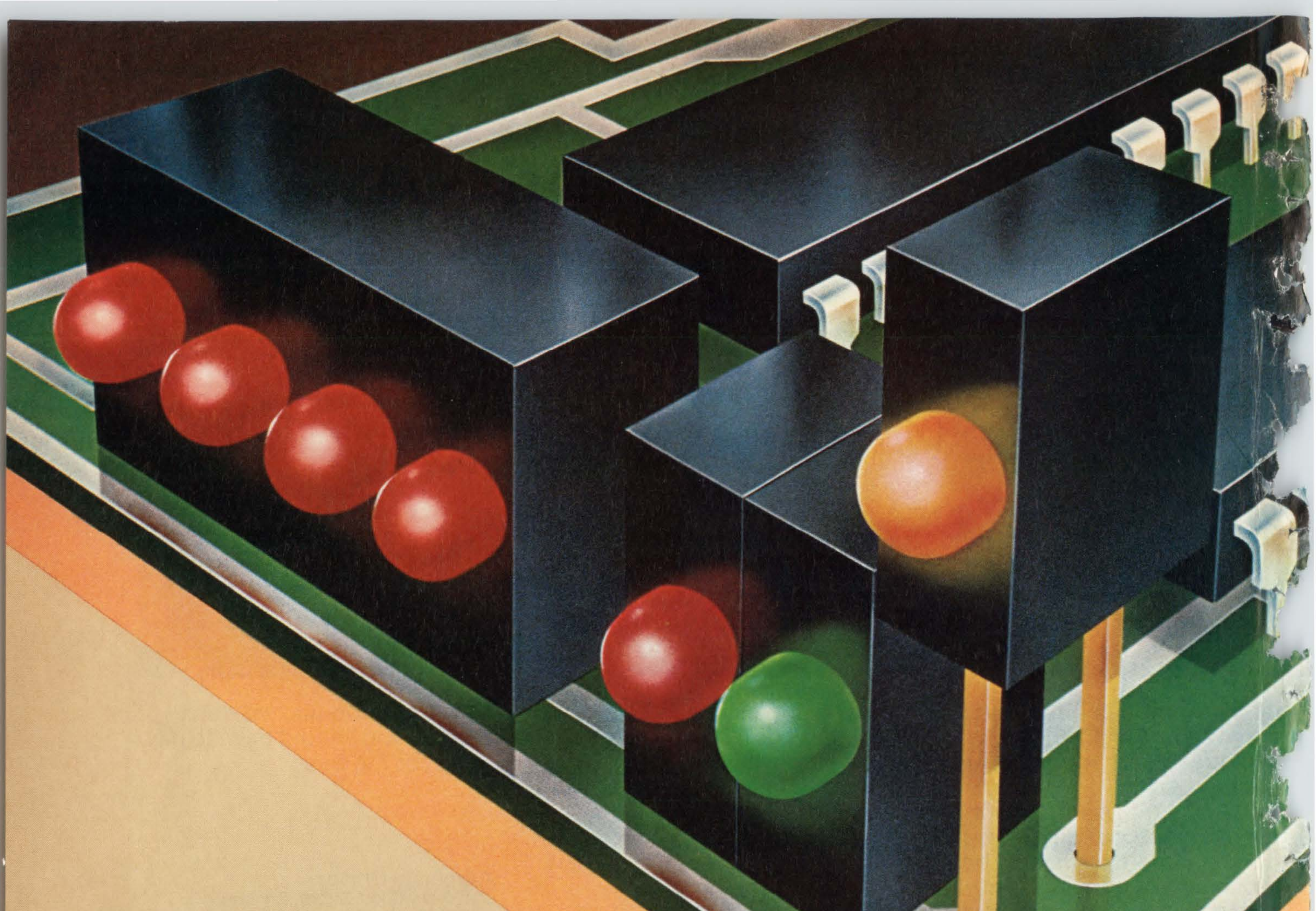

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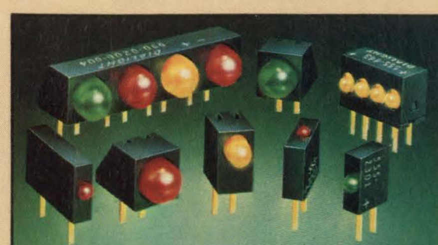

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CIRCLE 74

SPECIAL REPORT ON

GRAPHICS TECHNOLOGY

The adage that "a picture is worth a thousand words" has long had a double meaning for designers of computer based systems. Of course, it's true that graphics capability can speed the delivery of information and thus make a system more friendly and more productive. But it's also true that a really useful picture requires many words of stored data—plus the ability to rapidly retrieve and process the data. Hence, until quite recently, advanced graphics capability was restricted to very expensive systems, such as those for military simulation, motion picture production, or medical diagnostics.

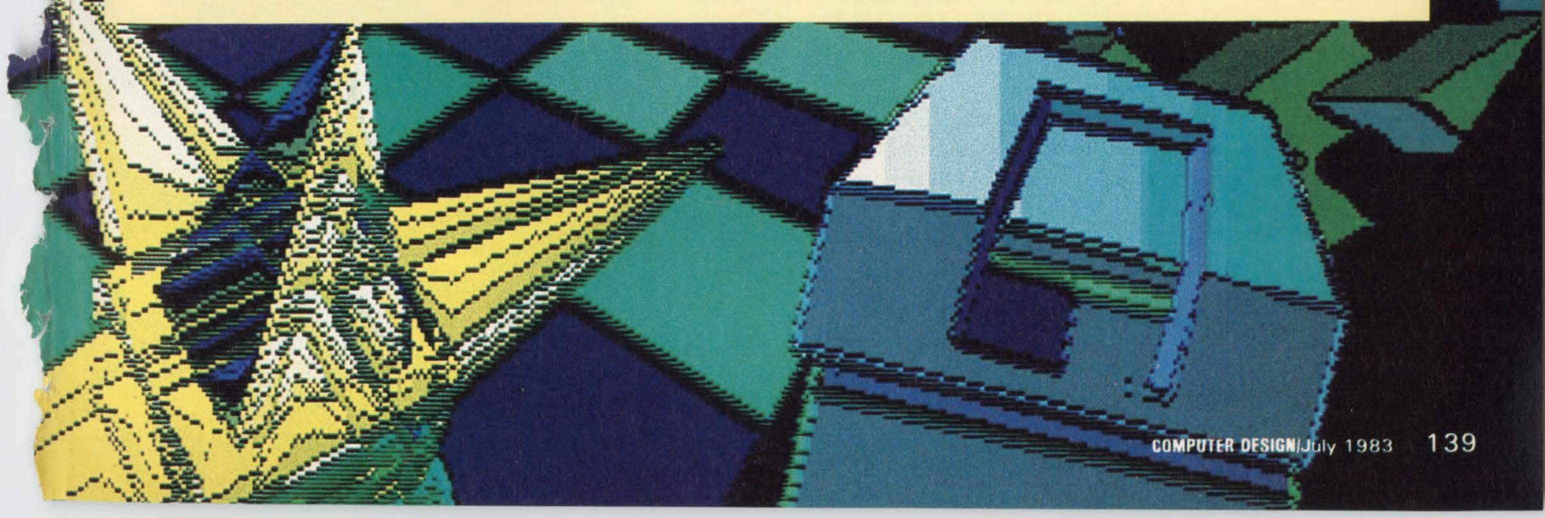
In the last few years, however, tumbling costs and improved performance of memories, microprocessors, and other hardware have triggered explosive growth in graphics capability for most computer based systems. Emerging standards for graphics software should further slash system costs by eliminating the need to "reinvent the wheel" and by allowing much frequently used software to be embedded in inexpensive silicon chips.

Perhaps because of the proliferation of video games and inexpensive home computers, people increasingly demand advanced graphics capability in the workplace as well. But the "throwaway" costs of video games are not easily duplicated in more demanding application areas. Many apparently advanced graphics features of games are really illusions—for example, the use of simulated 3-dimensional images and a limited palette of colors. Of course, video-game designers have also been able to embed most of the software in custom IC chips that can be produced cheaply because of the huge market volume.

For professional, industrial, and business system designers, the solution is to employ some of the same strategies used by game designers. Costs can be cut if the graphics capability embraces only a limited range of applications—hence, the emergence of families of dedicated workstations that perform only those tasks required in a specific application area. Then, for example, a workstation for a mechanical designer might have 3-dimensional graphics, whereas one for an accountant would merely provide, say, a simulated overlay of related forms. Of course, dedicated workstations can then be networked to form larger systems in which a mechanical designer might send cost information to an accountant.

One type of workstation that vitally concerns system designers is the engineering workstation, because engineers are involved as both designers and users of these systems. Therefore, we have chosen engineering workstations as the subject for our staff report in this issue. Unfortunately, many so-called engineering workstations emphasize graphics to the exclusion of other desirable features. So you should act now and help define the requirements of engineering workstations—or else the tools of your trade may continue to be inadequate.

Michael Elphick
Editor in Chief



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❧ My dad worked a lot of overtime the month he bought me my first mechanical drawing set.

Even so, we couldn't really afford the set I wanted. But he bought it anyway.

He said, "Quality always pays for itself."

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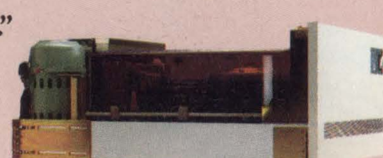

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CIRCLE 75

Special report on graphics technology

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CIRCLE 76

WORKSTATIONS THAT TAKE CHIP DESIGN FROM END TO END

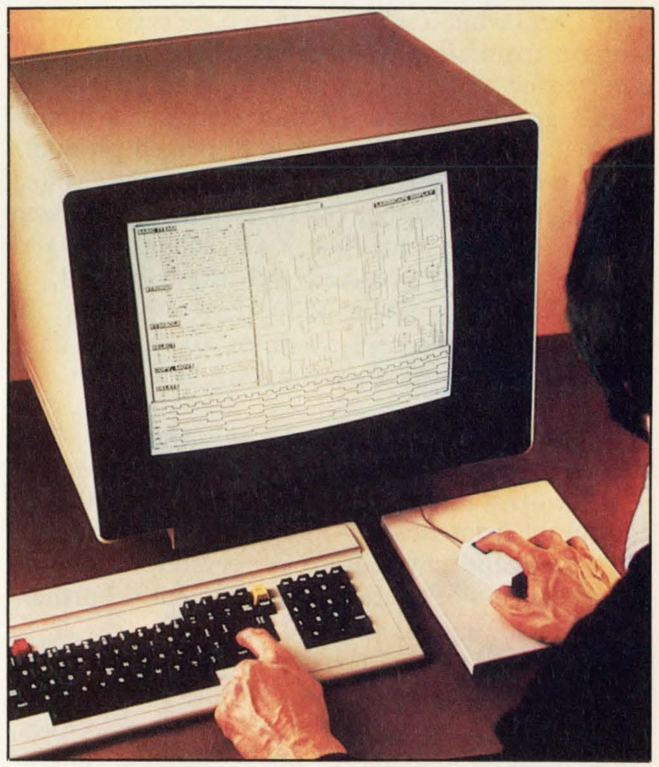
The proliferation of inexpensive memory, CRT controllers, and microprocessor ICs is fueling the development of powerful engineering workstations, some of which can do the entire design and simulation task.

by Richard Parker, Contributing Editor and Sydney F. Shapiro, Managing Editor

They are interchangeably called computer aided design and computer aided engineering workstations. Sometimes the blanket labels ''engineering'' or ''graphics'' workstations are used, which can apply to either or both types of workstations, depending on the definition.

But regardless of whether they are design or engineering workstations—and there are important differences between them—they are both modern design-automation tools. Moreover, they are changing the way microelectronic circuits are made, from their conception to their final package. Semiconductor technology itself is propelling such workstation developments, from inexpensive memory and controller chips for better graphics displays, to more powerful 16- and 32-bit microprocessors. Computer networking and software developments have blended these devices together to create powerful automation tools.

Who needs engineering workstations? Consider this: studies have shown that many circuit designers spend only about half their time doing actual design work. The other half is spent on such tasks as documentation, management and planning, component evaluation and selection, and technical



Powerful graphics are available from the PERQ 2 engineering workstation, a joint development of Three Rivers Computer and International Computers Ltd. The Unix based machine has a 13″ CRT display with 1280- x 1024-pixel resolution and can support any combination of graphics and text.

Do-it-yourself workstations

The very semiconductor device technology that drives high resolution graphics workstations is also making it possible for users to assemble their own systems from a collection of semiconductor parts—at a lower price, of course. Such systems' performance levels could not come close to those of high performance systems in the $50,000 range, but some rudimentary applications could do well enough with cheaper, home-built workstations.

Semiconductor RAM, for example, is widely available at less than $1 per kilobyte. So are a host of relatively inexpensive graphics controller chips that can easily handle 1024- x 1024-pixel graphics resolutions. As if that is not enough, a little more money can buy powerful graphics controller boards. And, of course, microprocessor technology has become so pervasive that powerful 16-bit units, many of them board-level based, can be affordably purchased.

Probably the one flaw with these parts is the cost of software development to tie everything together into a working system. But, again, that cost depends on the system performance level one is looking for—a level that, for many basic applications, may well be affordable for the do-it-yourselfer.

consultations—duties that are repetitive and ripe for automation. Thus, in an age when the byword is better automation for higher productivity, it benefits management to consider using the available design automation tools to improve design productivity. And what a selection they have before them, ranging from simple, inexpensive, personal computer based workstations all the way up to the "do it all" graphics terminals that translate a microcircuit from a simple idea to a packaged product.

To be sure, engineering workstations, called computer aided design (CAD) systems, have been around for quite some time. CAD systems were and still are primarily involved with the back end, or physical layout, of the chip design process. In attending to this process, many CAD systems have been dubbed glorified drafting machines.

Revolution in the workstation environment

The emergence of computer aided engineering (CAE) workstations, with their ability to take on additional frontend chip design tasks such as logical design and simulation, is revolutionizing the engineering workstation environment. Furthermore, local area network (LAN) advances have meant that relatively inexpensive CAE workstations can be tied together at different and remote locations that can share in the network's resources. Parallel developments in mass storage, microprocessors, and graphics controller chips have accelerated the spread of engineering workstations.

Although there is a deluge of high quality engineering workstations on the market, only a few, like the PERQ 2 from Three Rivers Computer (Pittsburgh, Pa), stand in a class by themselves when it comes to powerful graphics capabilities. Jointly developed by Three Rivers and England based International Computers Ltd, the Unix based workstation offers exceptional graphics capabilities.

For example, the 13" (33-cm) cathode ray tube (CRT) display with 1280- x 1024-pixel resolution (at 100 dots/in) supports any combination of graphics and text; presents drawings; erases instantly; offers freehand artwork and easy rotation of 3-dimensional models; and allows individually created typefaces to be generated for any design. The display can be highlighted for any area with scroll, pan, and zoom capabilities. PERQ 2 can be used as an independent workstation or as part of a network of distributed workstations. It has 32-bit virtual memory, an optional 20" (51-cm) landscape-type display, 2M bytes of maximum main memory, and 32M bytes of mass storage Winchester disk memory (a second 32M-byte Winchester disk drive is optional).

Many modern high quality engineering workstations include such advanced display features as windowing. This feature allows an engineering workstation to simultaneously display several unrelated events, so the user can study several displayed documents at once.

User interface with the Telesis Systems' workstation is simplified by a lightpen interactive CRT display. Called the "function screen," this display emulates functions that might require five separate functions on other workstations.

Kontron Electronics' KDS configurable development system/electrically erasable workstation provides all the tools needed for hardware and software development. Expansion capabilities cover the complete design cycle for microprocessor based products.

In the windowing concept, which is rapidly taking hold in engineering as well as office graphics workstations, the user typically selects the desired window (object) via a mouse, keyboard, or some other interactive device. Once selected, the window is enlarged to show its contents (traits) in greater detail. Such detail can be further scrutinized via soft keys that allow the user to zoom in on local and microscopic features in a desirable manner (schemas).

These abilities—objects, traits, and schemas—are a sampling of features to come for many more graphics workstations. Already, the objects, traits, and schemas approach is widely used in artificial intelligence. Expert systems in this area will be the future computers that will design other computers.

An example of improved operator interface to engineering workstations can be seen in the "function screen" on the workstation from Telesis Systems Corp (Chelmsford, Mass). As the only device used to input information into the workstation, it accelerates the user learning curve and improves the user interface. A keyboard is presented right on the "function screen," a lightpen interactive CRT display. This display emulates functions that require as many as five distinct input devices in other workstations (eg, trackballs and digitizer tablets). The CRT display provides a user definable soft key menu that automatically reconfigures in response to selected commands and design objectives. As users gain experience with the engineering workstation, they can use the soft key menu to modify the system.

More microcomputing muscle

Powerful 16- and 32-bit microcomputers are beginning a new phase for engineering workstations. Before such relatively inexpensive computing devices became widely available, both CAD- and CAE-type workstations suffered from two main traits: high price and great dependence on larger mini and mainframe computers with their attendant delays. This situation is rapidly changing for the better.

Low cost is a powerful incentive behind the drive for microcomputer based workstations. Microprocessors like the 16-bit MC68000 lead that drive. For a CAE workstation to earn that title, it must be small and relatively low priced (under $10,000) in order to be practical in a networking environment. In this application, several workstations can share the network's valuable resources. It is no wonder that microprocessor based personal computers, many of which can be called super personal computers, are aspiring to be engineering workstations.

Use of the personal computer as a workstation is promoted by FutureNet Corp (Canoga Park, Calif). That company's DASH-1 schematic designer converts the IBM PC into a low cost workstation that automates circuit and schematic system design. VTERM, a software package, allows the personal computer to emulate a DEC VT-100 terminal so that DASH-1 data can be transferred to a DEC VAX or PDP-11 computer system. In addition, the DASH-1 XT also converts the IBM XT personal computer into a workstation.

However, before personal computers can be accepted as engineering workstations, appropriate software operating systems must be developed. Such software will allow all networking workstations to operate in a virtual memory mode so that local and remote mass memory is accessible with the same speed and ease.

One approach for implementing virtual memory in an engineering workstation network is to use a dedicated microprocessor based circuit just for the virtual memory function. Whenever demand paging of virtual memory defaults and a page of information is not ready, the dedicated circuit takes over to supply the missing information page.

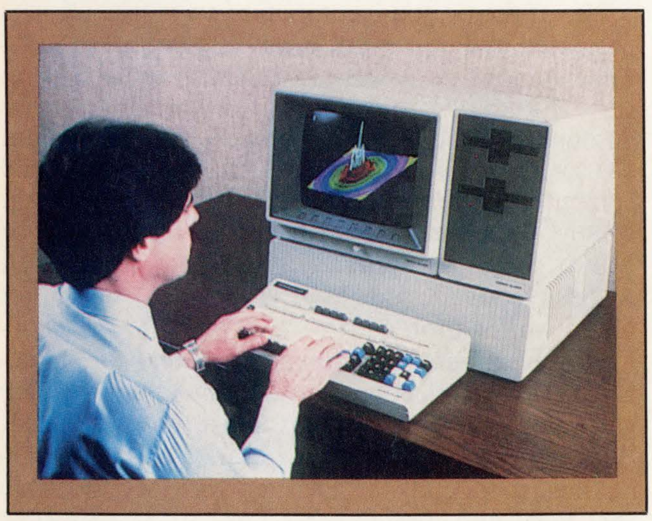
But, microprocessor power by itself is not a complete answer. It is extremely difficult, if not impossible, to handle all software languages with one microprocessor. While running LISP, for example, most microprocessors lose speed when used with a conventional instruction set. When LISP is compiled for conventional microprocessors whose architectures have reserved bits for data types (untagged architecture), throughput is slowed down. Many MC68000 microprocessor based engineering workstations, when used in a timesharing mode, suffer from this problem.

A recently announced microprocessor based development system workstation is the KDS from Kontron Electronics (Culver City, Calif). Although initial systems are available with a Z80 processor and a CP/M V2.2 operating system, a version with a 68000 central processing unit (CPU) and Unix operating system is expected to be announced presently. In the latter version, the Z80 becomes the 68000's input/output (I/O) interface processor.

With the KDS, only the 16" x 10" (41- x 25-cm) CRT unit and detached keyboard are set on the bench; all remaining components are located elsewhere. A computer module supports up to four in-circuit emulator modules and one timing and state logic analyzer module that function together as an instrument package for microprocessor hardware debugging and software/hardware integration.

16-bit micros take charge

Despite limitations, many emerging engineering workstations are capitalizing on existing 16-bit microprocessors. A good example is the structured



The model 7500 scientific computer, based on the Motorola MC68000 microprocessor, is available in both color and monochrome versions. Each Perkin-Elmer workstation includes two 5¼" floppy disk drives, the Unix-like IDRIS operating system, two RS-232 ports, ASCII keyboard, full-feature BASIC interpreter, and keyboard overlay.

computer aided logic design (SCALD) workstation from Valid Logic Systems Inc (Sunnyvale, Calif), which is based on the 16-bit 68000 microprocessor. The workstation allows designers to design gate-array circuits as large as 500k gates and to do local simulation. Such a task formerly required using a large and powerful mainframe computer like the IBM 370 or the DEC VAX. Although the SCALD workstation does not provide the processing speed of a large mainframe computer, it does provide many powerful features that make it cost effective.

Using the SCALD workstation, for example, a designer can interactively validate and debug portions of a logic design before it is committed. The workstation runs on the Unix operating system and has all the tools required to create structured top-down logic diagrams. The SCALD's software allows the development of a design data base that contains module definitions, device parameters, and component interconnections. Logic design timing can be verified and simulated for entire circuits and even circuit parts. A postprocessor is included to provide net lists and verifiers. A single cluster controller manages up to four SCALDs that each have a 1024- x 800-pixel display. Each controller can handle up to 4M bytes of error-correcting memory.

Perkin-Elmer (Oceanport, NJ) recently introduced its MC68000 based model 7500 scientific computer, which is essentially a packaged workstation. It features multi-user program development, data acquisition, data reduction, and graphics display. A monochrome version includes 416K bytes of memory and a video module with a 13" (33-cm) monitor; its color counterpart has 640K bytes of memory and can display any combination of 16 colors out of a 27-color palette. Both use the Unix-like IDRIS operating system and are supported by ANSI, FORTRAN 77, BASIC, and C.

Another powerful yet relatively low cost engineering workstation based on 16-bit microprocessors is the model 230 advanced color graphics terminal from Envision (San Jose, Calif). The workstation is based on the Intel 8088 and NEC 7220 microprocessors. It provides a designer with a local display that allows vector storage manipulation in the terminal. Graphics objects and schematic symbols can be defined, stored, and manipulated within the terminal without host computer intervention and overhead burden. Graphics drawings are made in a 16k- x 16k-bit virtual address space. The workstation features up to 16 colors from a 4096-color palette, zoom and panning, graphics drawing primitives, and compatibility with Tektronix Inc's (Beaverton, Ore) Plot-10 software package. Two-dimensional transformations like scaling, translating, and rotating can be performed on drawing segments. In addition, object and segment operations such as picking, copying, and changing visibility can be done locally.

Envision's model 230 advanced color graphics terminal is an example of how powerful 16-bit microprocessors are propelling engineering workstation performance. This terminal uses both Intel 8088 and NEC 7220 microprocessors. Vectors allow designers to store and manipulate elements such as graphics objects and schematic symbols all within the terminal without host computer intervention.

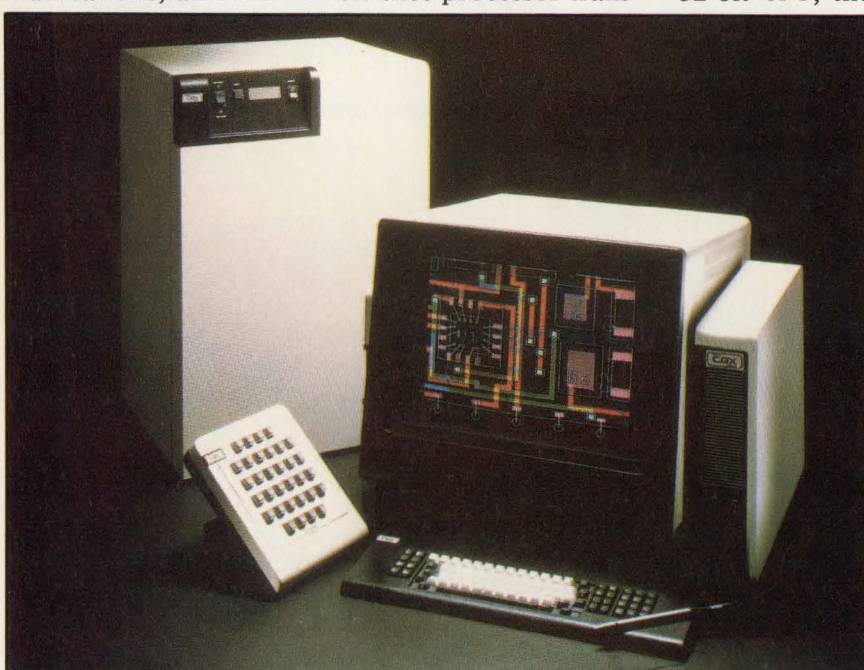
Still another 8088 based graphics display system is the model 2001 from CGX Corp (Acton, Mass). This system has three microprocessors on its processor board, each dedicated to specific tasks. An Intel 8088 command processor supervises internal timing, data transfers, interrupts, and control panel communications; an AMD 2091 bit-slice processor transfers data from the host computer to a data buffer; and an Intel 8089 I/O processor transfers that information to a selected display station. This multiprocessor one-on-one architecture enables users to mix independent color raster and monochrome vector terminals on a single-cable IBM compatible network of interactive workstations.

Two 16-bit 8086 microprocessors as well as dual 16-bit high speed floating-point 8087 coprocessors power the AYCAD CAD system from Aydin Corp (Fort Washington, Pa). The turnkey system also includes a bit-slice bipolar microprocessor for hardware graphics vector generation and an 8080 microprocessor to run the system's digitizer. Running on the CP/M-86 operating system, the CAD system features a high resolution 1024- x 1024-pixel raster-scan display, a separate alphanumeric system console, full ASCII keyboard with calculator pad, a 36" x 48" (91- x 122-cm) digitizer tablet, 35M bytes of Winchester disk drive storage, and 1.2M bytes of floppy disk drive storage.

Even 32-bit micros play a role

There is no question that 16-bit microprocessors provide limited intelligence to engineering workstations. As powerful as they are, many engineering workstations are going the 32-bit microprocessor route to obtain the necessary intelligence independent of larger mini and mainframe computers.

Hewlett-Packard Co (Palo Alto, Calif) adheres to that method. The firm has announced a 5-chip set that includes a 32-bit CPU. The chip set will form the basis of the HP-9000 family, powerful engineering workstations the firm claims will perform like "personal" mainframe computers. Besides the 32-bit CPU, the chip set includes a 128K-bit static



CGX graphics display systems consist of a vector display station, a color raster display station, and a channel unit containing processor and channel interface boards. The systems run from the IBM 360/370, 30XX, and 43XX family, or from IBM compatible host mainframe computers.

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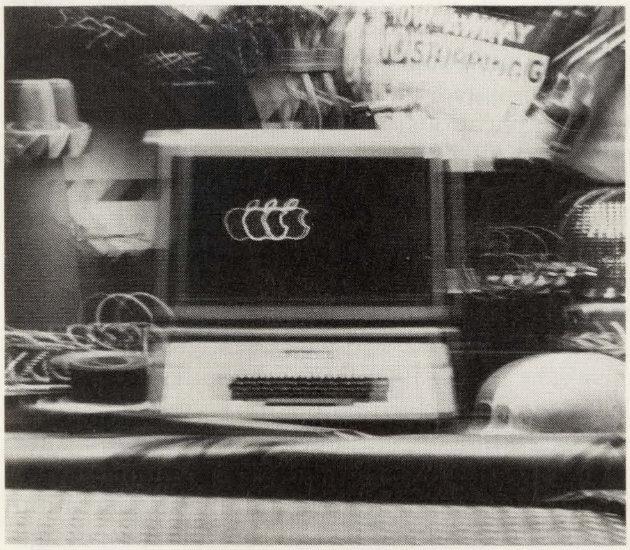

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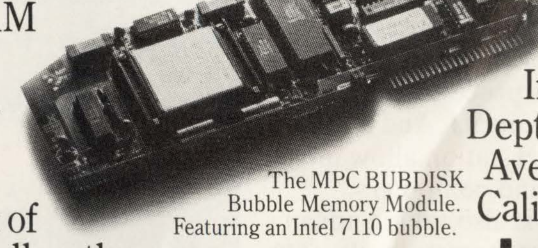

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Advanced engineering workstations such as the AYCAD from Aydin can just about do it all. This turnkey system runs on the CP/M operating system and includes many features. Separate microprocessors run the system's digitizer tablet and graphics vector generator.

random access memory (RAM), an I/O processor, a memory controller, and an 18-MHz clock generator. The set interfaces with any of three local area networks: Ethernet, the forthcoming IEEE 802, and Hewlett-Packard's shared resource manager (SRM). Each HP-9000 workstation will be able to house as many as three 32-bit CPUs. The top-of-the-line workstation will have a color CRT display with menu-prompting soft keys, 2.5M bytes of error-correcting RAM, a 27K-byte floppy disk drive, a 10M-byte Winchester disk drive, a built-in thermal printer, and a wide range of software packages. Software capability includes single-user BASIC and multi-user Hewlett-Packard UX operating systems, FORTRAN and Pascal compilers, and a Hewlett-Packard graphics library.

The CPU chip has a microcoded stack architecture that supports 280 instructions, including IEEE standard floating-point arithmetic formats. Offering a processing capability of 1M instructions/s (at the 18-MHz clock rate), the CPU supports direct addressing of 500M bytes of memory, more than any microprocessor around. In addition, the CPU is fast: it can perform 550-ns executions for a register load, 5.94-μs executions for a 64-bit floating-point addition, and 10.34-μs executions for a 64-bit floating-point multiplication. When used in the HP-9000 workstations, each workstation can handle 36M bytes/s over the system's processor bus. RAM can be added in 256K-byte increments. And multiple I/O processors within each workstation allow interfacing to other workstations and computers.

Teletype Corp (Skokie, Ill) is also taking advantage of 32-bit microprocessor power in its 5620 workstation. Based on the 32-bit Bellmac 32 processor from Bell Laboratories (Murray Hill, NJ), the workstation includes a monochromatic 15" (38-cm) CRT display. It runs on the Unix operating system that allows users to work on several programs at once, displaying them concurrently on the CRT screen. The 5620 lets users create up to six windows of any shape or size on the display.

While the workstation executes one program, the user views and manipulates another on the screen. Software can be downloaded from the host CPU into the 64K-byte main memory of the 32-bit semiconductor RAM. Firmware is housed in 24K bytes of 16-bit erasable programmable read only memory (EPROM). The workstation has full graphics capability with an 800- x 1024-pixel resolution. A mouse as well as three programmable keys is available to facilitate CAD applications. The 5620 can communicate with other terminals as well as with computers via an RS-232-C port at speeds ranging from 300 to 19.2k baud.

Another CAD workstation based on 32-bit microprocessors is the CDX500 from Cadnetix Corp (Boulder, Colo), whose performance rivals that of mini- and mainframe computer based systems. The system is aimed at printed circuit board (PCB) design applications. It includes a microcomputer with 32-bit internal architecture, up to 3.5M bytes of main memory, a 19" (48-cm) ultrahigh resolution color display, a 5¼" 40M-byte Winchester disk drive, and a 1M-byte floppy disk drive. Other features include a detachable keyboard, mouse input device, and an object-oriented user interface.

Powerful CDX5000 software packages allow interactive schematic generation, automatic component placement, high speed automatic trace routing, interactive editing of component placement and trace routing, and continuity and design checking. Additionally, the software allows automatic generation of PCB artwork and numerical control tapes; design documentation, including assembly drawings and bills of materials, can also be automatically generated.

The trend toward 32-bit microprocessors to support advanced engineering workstations can be seen in machines such as the CDX500 from Cadnetix. Aimed at PC board design applications, system features include a 32-bit microcomputer, up to 3.5M bytes of main memory, and 40M bytes of Winchester disk drive memory. A 19" CRT display provides high resolution.

A family of workstations from Orcatech Inc (Ottawa, Ontario, Canada) consists of a low end Orca1000 for engineers who require minimum capabilities and flexibility; the Orca2000 for the single user who wants growth capabilities; and the top-level Orca3000, designed around the Motorola MC68000/68010 32-bit microprocessors. The family's Unix based operating system is integrated using the Special Interest Group on Computer Graphics (SIGGRAPH) Core standard. The top-level system has parallel architecture that allows designers to simultaneously update a display image with the system's graphics processor, send data to the host computer, perform design calculations, and store the resultant picture.

A different approach

Despite microcomputer technology's powerful attributes, many engineering workstation manufacturers prefer to rely on general purpose computers, which provide greater number-crunching abilities than even the most powerful micros, but, of course, are higher priced and physically larger. For example, CAE Systems Inc (Sunnyvale, Calif), Mentor Graphics Inc (Tigard, Ore), and Calma Microelectronics Div of General Electric (Santa Clara, Calif) have opted to use the 32-bit Domain workstation computer from Apollo Computer (Chelmsford, Mass) for their engineering workstations. Like many other workstations, Domain runs on the popular Unix operating system.

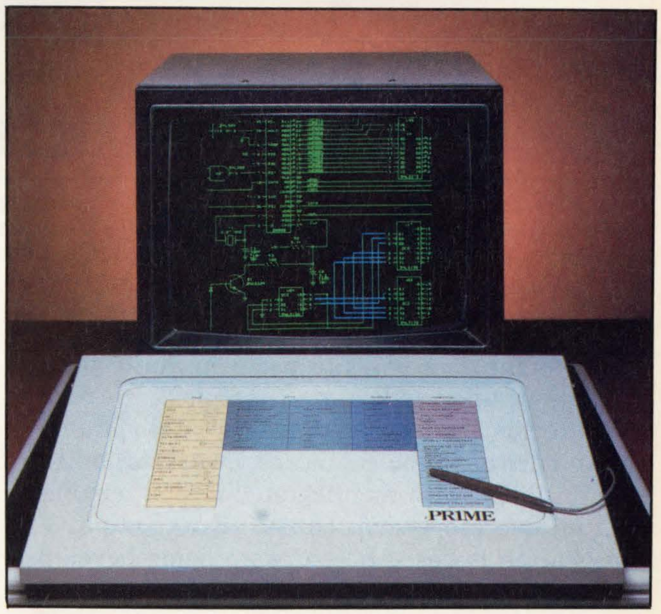
The Domain computer has a 300M-byte optional disk drive memory, local disk storage, virtual memory capability, and local networking options; it can also interface with larger mainframe computers. Its DN 600 color computational node has a palette of over 16 x 10M colors, up to 2M bytes of dedicated dual-ported display memory, 16M-byte virtual address space per process (15 processes per user), and up to 3.5M bytes of main program memory. It provides seven software selectable color display modes and 4, 8, or 24 color planes on a 19″ (48-cm) 1024 x 1024 bit-map raster display. Vectors are drawn at more than 1M pixels/s under control of the company's Aegis operating system.

Powerful computer aided design/computer aided manufacturing (CAD/CAM) systems like the Electronic Design Management System (EDMS) from Prime Computer Inc (Natick, Mass) derive their performance from powerful computers like Prime's 32-bit 50 Series. The menu-driven, multiuser EDMS for interactive digital logic design analysis and drafting has an electronic component and a circuit design data base, both controlled by a database management system (DBMS). The EDMS has a color graphics and alphanumeric display and is compatible with other Prime computers and communications software.

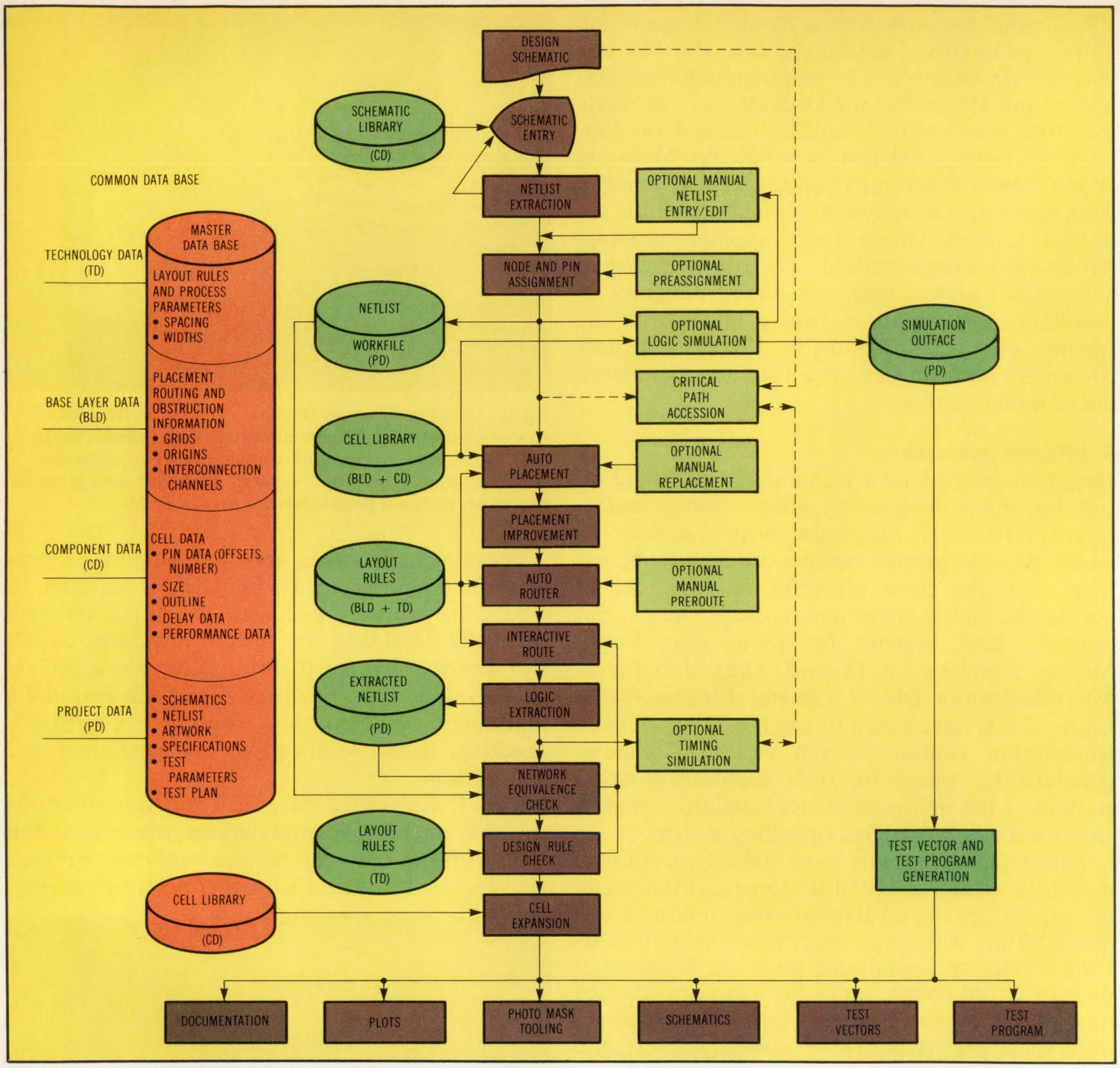
Apollo Computer's DN600 Domain workstation fits into a LAN of dedicated 32-bit computational nodes connected by coax cable. Each workstation contains VLSI CPU, memory, 19″ color graphics monitor, separate keyboard, and graphics processor; optional peripherals are also available.

Speaking of software, good general purpose software for engineering workstations is difficult to find. Most software packages on the market were originally developed for custom integrated circuit (IC) designs, making them ill-suited for universal gate-array designs. Such packages lack automatic placement and routing routines, continuity checking, layout verification, and gate-array cell digitization.

Very few so-called integrated software solutions exist for engineering workstations. Many CAD and CAE workstations still require multiple software packages that contain their own operating systems,



Powerful CAD/CAM systems, such as Prime Computer's Electronic Design Management System (EDMS) depend on equally powerful computers like that company's 32-bit 50 series. The menu-driven, multi-user engineering workstation can handle all aspects of interactive digital logic design and drafting.

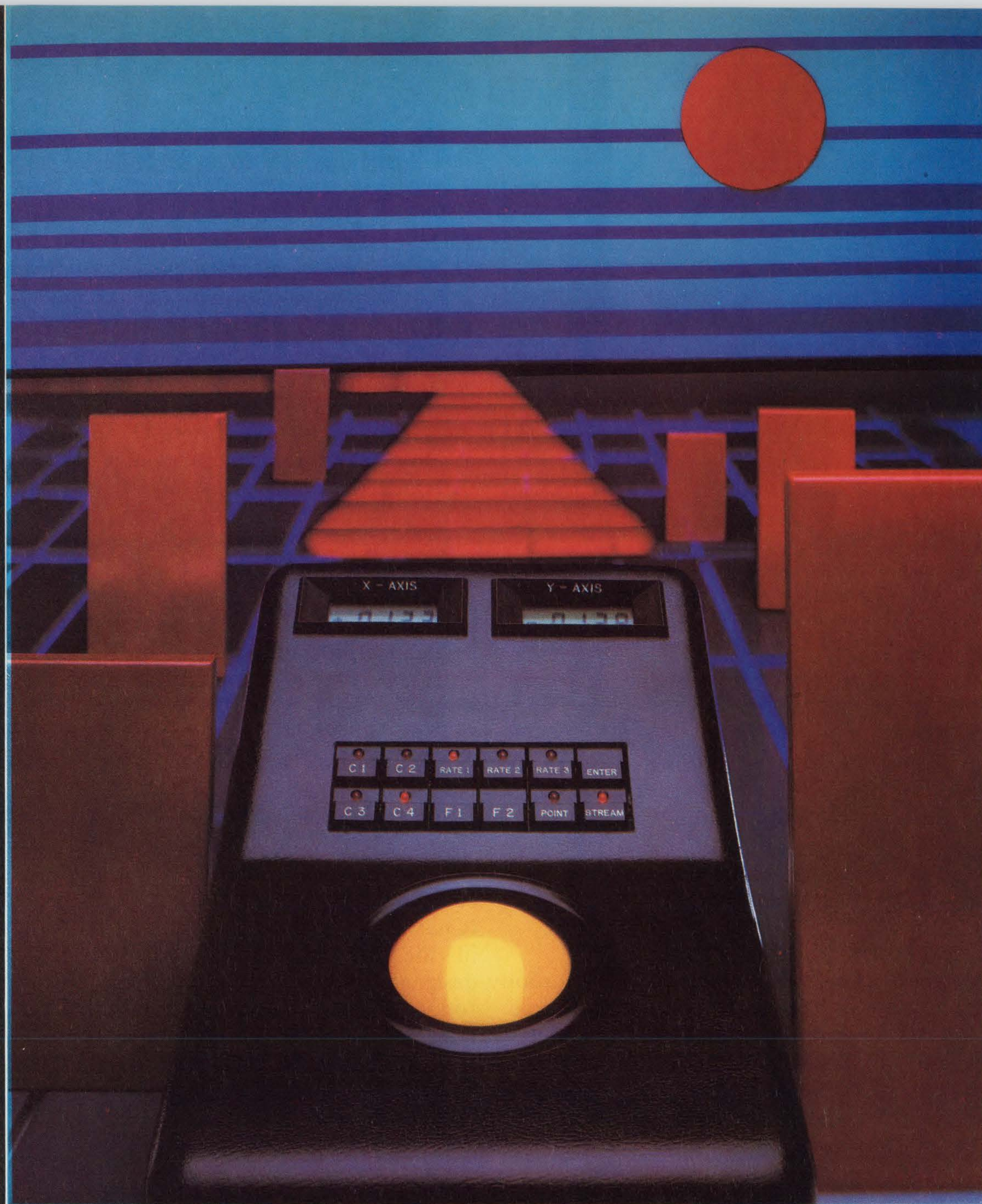


As an answer to the lack of integrated software in engineering workstations, California Devices' integrated design, engineering, automation system (IDEAS) provides the design and verification tools for gate arrays. Software developed at the firm will include modules for layout, simulation, masking, and testing. The modules will share a common data base. (Source: Electro/83 Professional Program.)

run programs written in different languages, and use different data bases to perform the IC design, simulation, and verification functions.

California Devices Inc (San Jose, Calif) thinks it has an answer to the engineering workstation software problem with its integrated design, engineering, automation system (IDEAS) workstation. The workstation is based on software being developed at Computer Devices Inc and provides integrated design and verification tools for gate arrays. The software modules currently used for layout, simulation, masking, and testing are being integrated into a single cohesive system with a common data base. System modules, linked by interface drivers, take input data from the common data base to generate the output files required at each step of the evolving design. Each design phase is fully interactive, allowing the designer total control.

The IDEAS workstation features a common data base accessible by system modules; a schematic entry package that allows direct entry of logic and circuit schematics, with optional entry of network list descriptions; and logic and circuit simulation. It also features automatic placing and routing, a network equivalence check, tooling database conversion, and an automatic interactive test program. Workstation outputs include pattern-generation tapes, schematics, layouts, bonding diagrams, production test programs, test patterns, and documentation.



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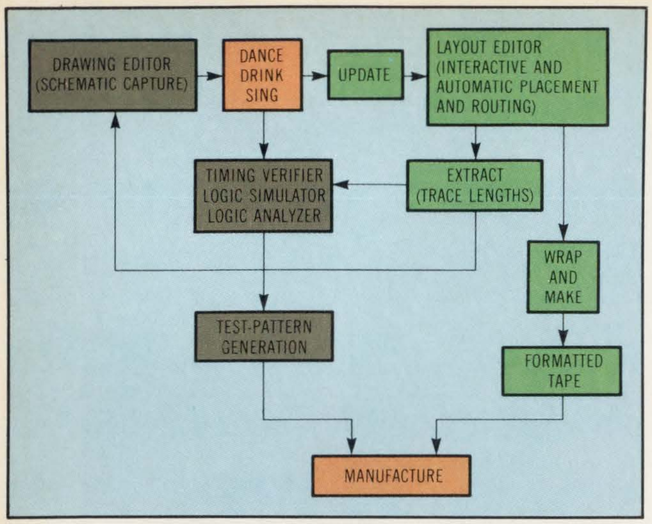


Good engineering workstation software follows a hierarchical scheme like the software in Daisy Systems' Gatemaster workstation. Three software packages (DANCE, DRINK, and SING) follow an integrated hierarchical structure format.

CAE Systems already offers an engineering workstation (the CAE2000) with truly integrated software. Unlike many engineering workstations whose software is limited in scope (ie, it is maximized for either initial schematic capture or for final physical layout), the CAE2000 has an integrated software package that addresses the entire electrical design cycle, from behavioral definition and analysis through physical layout and testing.

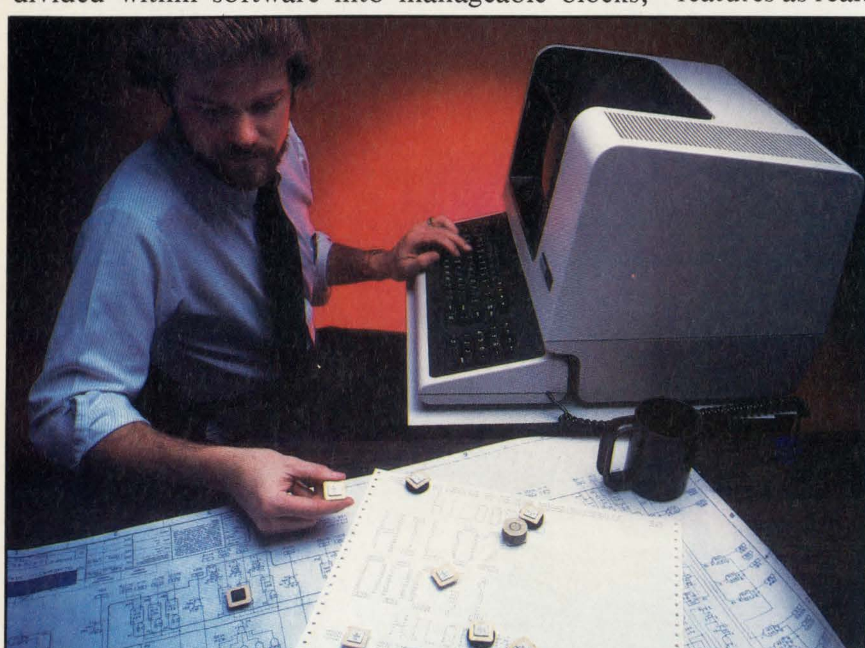
Hierarchical structure needed

One requirement for good engineering workstation software is that it follow a hierarchical scheme. That is, a gate-array design problem should be subdivided within software into manageable blocks, each of which should be designed and checked before going on to the next one. The software development system of the Gatemaster workstation from Daisy Systems Corp (Sunnyvale, Calif) described later, is a good example. The system's three software packages, DANCE, DRINK, and SING, follow an integrated hierarchical structure format.

Fortunately, other firms are producing better software packages for the engineering workstation environment, in many cases optimizing them for a specific part of the design cycle. An example is GenRad Inc's (Santa Clara, Calif) HILO-2 software package, a high speed universal logic design simulator optimized for accuracy and efficiency. Aimed at semicustom IC designs such as gate arrays, cell arrays, and custom ICs, as well as conventional standard IC designs, the software package's resources facilitate fast, accurate logic design verification and effective test validation.

Developed at Brunel University in Uxbridge, England, HILO-2 features gate-level and functional-level logic design simulation and timing verification, test validation, a high power language for functional modeling, and a menu-driven interface. The software package runs on 32-bit virtual memory computers like DEC's VAX-780.

Artificial intelligence is also finding its way into CAD/CAE software development tools to create software programs that are not only more powerful, but are also user friendly. Symbolics Inc (Chatsworth, Calif) now uses MIT's LISP language in the Symbolics' 3600 workstation, allowing designers to develop complex software programs for specific applications like very large scale integration (VLSI) designs. These programs allow such features as realtime object manipulation and object



The HILO-2 software package from GenRad is optimized for universal high speed logic design simulation. Aimed at workstations for semicustom IC designs such as gate and cell arrays, the software package allows fast and accurate logic design verification and effective test validation.

relation of several manipulated objects. A software program developed by the 3600 processor, for a VLSI circuit for example, would define objects like gates and paths which influence the circuit's simulation. The 3600 workstation has a 36-bit microprogrammable CPU, with 32 bits assigned to integers (28 for bit pointers and 4 for data types) and 4 bits assigned to keep track of stack pointers and other manipulations.

Relational DBMSs excel

Getting the right DBMS for an engineering workstation is crucial, for it is the DBMS that allows all workstation pieces—eg, CAD programs, graphics software packages, and processor—to work together harmoniously. A relational-type DBMS is the most flexible for computer aided engineering workstations. Certainly, there are other, more efficient DBMSs than relational ones (such as hierarchical and network types). However, efficiency is not a major problem for computer aided engineering applications, since database accessing is not very frequent and access paths can be optimized because the paths are known in advance.

For higher efficiency, Mentor Graphics employs a hybrid form of the relational DBMS approach in its Idea 1000 workstation. By letting each schematic component form its own small data base, the Idea 1000 workstation keeps each relation's size (ie, the number of parameters) comparatively small. The distributed engineering workstation is autonomous, connecting to Apollo Computers' 12M-bps Domain local area network, and is supported by a distributed database structure. At each Idea 1000 workstation, a designer can break down a logic diagram, graphically simulate circuits, and change circuit components as well as circuit features. The system maintains a list of components and documented circuit changes, and analyzes and evaluates the circuit according to user defined parameters. Each network workstation holds in its own memory all the work done at that particular station. The 32-bit system employs the Aegis virtual memory operating system, has a fast main memory expandable to 3.5M bytes, and large (300M-byte) disk drive storage capacity.

An important feature of the Idea 1000 workstation is the DBMS' flexibility. A special file, which is a relational statement script of database changes, is paired with a data dictionary file that governs all database files involved in the workstation. This approach allows the database configuration to gradually adapt to any new needs as the files are accessed. There is no need to shut down the workstation merely to reload the data base. All database file changes are automatic and transparent to the user.

A recent addition to the list of DEC VAX-11 based design/management systems is the Series 8000 from

Computervision's Instaview interactive design workstation can be used for a variety of CAD/CAM applications. A wide range of specialized software capabilities plus PCB and integrated circuit design significantly increase the designer's productivity.

Cadtec Inc (San Jose, Calif). This hardware/software system integrates the company's model 8200 interactive graphics workstations with model 8500 graphics office stations. Heart of the Series 8000 is the CORD data system, a relational database system with an object-oriented interface. Although initial application software focuses on logic design, future extensions will enable the system to support all levels of IC and electronic system design.

The workstation/office station system concept is based on the belief that an engineer needs a workstation's high performance only 20% of the time. Office stations suffice the rest of the time and give the engineer required access to all project data on the VAX via standard RS-232 communications protocols and a local area network.

Digital Equipment Corp (Marlboro, Mass) also offers its own CAD/CAM system, based on the company's VAX series 32-bit computers. The VAXstation family workstations can form a network that allows several engineers to work simultaneously on different parts of a complex VLSI circuit design, then pass the resulting design on to other engineers for circuit layout, software development, and manufacturing.

How much local computing?

Just how much local computing power an engineering workstation should have is under debate. The need to rely on a large and often external mainframe computer is one of the problems plaguing engineering workstations, some of which do not possess sufficient intelligence to handle complex graphics requirements.

Although many engineering workstations can respond to host computer commands and store data locally, they may still be under the control of an application program that runs on the mainframe host computer. Thus, much of the host computer's processing time may be spent on simple graphics routines that could be performed locally on a more intelligent workstation.

This problem is exacerbated for timeshared systems. In addition, time is wasted as data are transferred between the host computer and the local workstation. Moreover, inherent reliability is a problem for any communications link to another computer—if either the host computer or the communication link fails, the workstation loses all graphics abilities.

Some workstations, like the Omega 400 from Metheus Corp (Hillsboro, Ore), claim to be intelligent enough to handle an entire design problem from back to front. The system carries a chip designer from product conception and block diagram to layout simulation and test-vector generation. The workstation, with its 1024- x 1024-pixel graphics display, has an impressive drawing speed of 1M pixels/s. It features 4- and 8-bit display planes that provide up to 16M color shades, an onboard signature analyzer, and self-test microcode.

Ideally, a workstation with a graphics presentation should provide the highest resolution possible.

Last November, Metheus introduced the λ750, a VLSI system that spans all phases of the IC design process: logic design, simulation, and mass layout. The engineering workstation is based on a powerful 32-bit standalone computer that allows it to capture, simulate, and verify both logical and physical VLSI IC designs. It is Multibus based and uses three 68000 microprocessors—two in the CPU and a third as a display list manager for a bit-slice graphics processor. Unix based, the workstation supports virtual memory operations and is available with 1M byte of main memory (expandable to 16M bytes), 30M bytes of 5¼" Winchester disk, and 1M byte of floppy disk memory. An even more recent version, the λ740, provides logic design and simulation but not mass layout.

The trend toward more intelligent graphics engineering workstations is also evidenced in the model 4110 from Tektronix. This graphics workstation performs some fairly complex graphics manipulations, freeing the host computer's valuable time and increasing system reliability. Intelligent graphics workstations like this generally have the appropriate software packages and sufficient semiconductor RAM and mass memory to do their stated tasks. The 4110, for example, can perform low level graphics routines like manipulating local picture segments, forming 2-dimensional images, and executing higher level commands. It allows users to communicate with it through a scrollable-dialogue display that retains a graphics image on the CRT screen.

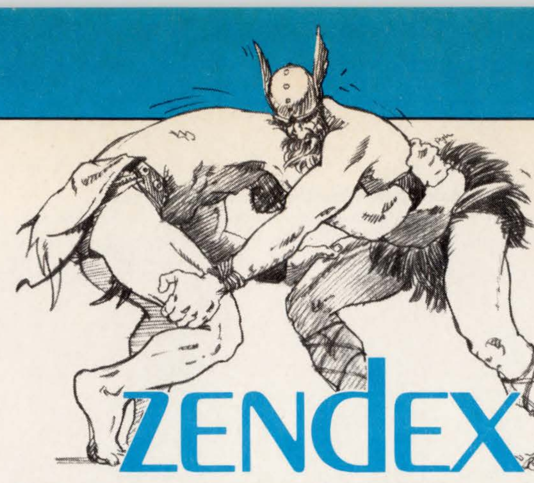
Convergent Technologies Inc (Santa Clara, Calif) takes a dual-processor approach in making a more intelligent graphics workstation. It uses a pair of 16-bit 8086 microprocessors in its IWS-110/120 workstations to cut down system throughput delays for complex graphics. One 8086 microprocessor is used as the main CPU while the other is dedicated to graphics processing. The IWS-110 is a desktop unit; the IWS-120 is a floor-standing model. Each has a bit-mapped 15" (38-cm) noninterlaced display with a 660- x 512-pixel resolution. The workstations provide both bit-mapped and character-oriented displays and include vector and raster-scanning display modes with multilevel software interfaces.

Software programs called CADISYS were made available to Mentor Graphics by California Automated Design Inc (Santa Clara, Calif). By using the Idea 1000, they are claimed to reduce the logic design and physical layout time of a VLSI circuit pattern of 2500 gates. Three subsystems are involved: automatic placement, automatic routing, and interactive graphics. Programs are written in Pascal or FORTRAN. Recently announced Idea 1200, 1300, and 1400 CAE workstations function either alone or as part of a network. In addition to the 32-bit Apollo Domain computer, each node contains a graphics display with an optional electrostatic printer, up to 1.5M bytes of program memory, and up to 34M bytes of Winchester disk storage.

Optimizing design locally

Some engineering workstations are optimized for local logic design, leaving simulation and modeling to a remote host computer. The advantages of this approach are more local design flexibility than if the same workstation were to handle design, simulation, and modeling, and greater design economies, particularly for custom IC designs. The Logician engineering workstation from Daisy Systems exemplifies this approach. It can be linked via the Ethernet LAN to other system elements such as mass storage devices, printers, and mainframe computers.

Even more powerful is Daisy's Gatemaster, which reportedly reduces gate-array development time by 50% to 70%. Based on the 10-MHz 16-bit 8086 microprocessor, the workstation employs multiple processors for the I/O ports, a special bit-slice microprocessor for graphics, and a complete set of software packages. The Gatemaster allows designers to experiment at the gate level with a gate-array design; this can be done for several different types of gate arrays. The workstation is compatible with gate arrays of all major manufacturers and accommodates both metal oxide semiconductor and bipolar technologies. A 19" (48-cm) high resolution CRT display, programmable keyboard, and optional bit-pad digitizer tablet are all available.



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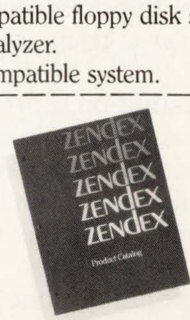

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Three Major Graphics Display Technologies

Parameter	Raster scan	Vector scan	Storage tube
Cost	Low to moderate	Moderate to high	Moderate
Resolution	Poor to fair	Excellent	Excellent
Brightness	High	High	Low
Contrast	High	High	Low
Color capability	Excellent	Limited	Virtually none
Selective erasure	Yes	Yes	Limited
Image (dynamic manipulation)	Poor	Excellent	Limited
Freedom from flicker	Good	Good (poor with large amounts of data)	Good (poor for "write-through" mode)
Memory dependency	Moderate	High	None

The three software packages previously mentioned propel the Gatemaster's performance to new heights: Daisy Network Connectivity Extractor (DANCE), Daisy Resolving Linker (DRINK), and Simulator Input Generator (SING). DANCE checks syntax errors and any missing connections or conflicting parameters; DRINK links multiple pages together and allows an incomplete design to be operated on as a complete entity; and SING creates component and network lists and checks for design-rule errors.

Reaching resolution requirements

Ideally, a workstation with a graphics presentation should provide the highest resolution possible. This is particularly important for complex graphics presentations. Unfortunately, extremely high resolution means more refresh memory, which translates into more money. An engineering workstation with about 128K bytes of graphics refresh memory costs about $5000 to $10,000—a price range that can skyrocket to $40,000 or more for a 1024K-byte system. That is one reason why raster-scanning graphics display technology is popular, since it provides the lowest cost and best overall performance of any of the three major graphics display technologies for a given size refresh memory. (See the Table.)

High resolution is probably not needed for every application. The staircase effect produced with a raster-scan type display is apparently not a big problem for many applications, as is evidenced by the dominance of this technology in all kinds of graphics workstations. For applications requiring higher resolution, one can, of course, improve raster-scan display resolution by adding more memory to the system. However, that will negate the system's original advantage—its low cost.

A more promising approach appears to be using antialiasing hardware and software to smooth out the graphics "jaggies." Some workstations, such as the Graphics-32 from Applicon Inc (Burlington, Mass), have antialiasing algorithms already built in. One algorithm in the Graphics-32, for example, lessens the jagged effect by displaying with less intensity the pixels adjacent to ones located on the edges of jagged lines.

With the proper antialiasing algorithm, sufficient resolution can be achieved from a raster-scan workstation display. Given the right antialiasing circuit, for example, a 1024- x 1024-pixel display, commonly found on many graphics workstations, can achieve resolutions close to those possible from much more expensive systems. This method is used in the System 3400 from Lexidata Corp (Billerica, Mass), the Vistagraphics 3000 from California Computer Products Inc (Anaheim, Calif), and the CG7900 from Chromatics Inc (Tucker, Ga).

Many such systems employ special techniques to improve graphics resolution while keeping the overall system cost down. The Lexidata 3400, for instance, allows the user to assign four work areas to the display for such features as zoom, scroll, pan, and wraparound. Both this system and the Vistagraphics 3000 allow individual pixel blinking. On the other hand, the Chromatics CG7900 has outline boxes in place while depicted objects are moved about. Regardless of these uses, many applications, such as those involving complex interactive designs, usually require the higher resolutions found on vector-scan and direct-view storage tube technologies.

Better graphics standards to come

There is a growing need for graphics standards. Ideally, graphics software programs written for one engineering workstation should be useful on another. Realistically, that is not the case, primarily since the industry does not agree on what the appropriate graphics standards should be. Fortunately for the user, the computer graphics industry has begun to recognize this problem and to

treat it more seriously. ANSI and the International Standards Organization (ISO) are trying to establish meaningful graphics standards.

The struggle for standards has come down to one of two graphics standards: the Graphical Kernel System (GKS) and the Core system, with ANSI and the ISO appearing to favor the former. The GKS was originally developed by the Deutsches Institut für Normung (DIN), West Germany's official standards body. Core, on the other hand, is a *de facto* standard created by the SIGGRAPH Graphics Standard Planning Committee of the Association for Computing Machinery. Several thousand software engineering workstation programs have already been written in Core since 1977 when the first Core specification was published; few, if any, GKS software packages are available. In short, many U.S. firms have made a considerable investment in Core software.

While Core is a rich system that includes both 2- and 3-dimensional functions, the GKS system is simpler, handling only 3-dimensional functions. GKS' simplicity is its selling point to ANSI and the ISO. The ISO and ANSI's X3H3 Committee on Graphics Standards have rejected the Core system. Nevertheless, it has been used since 1977. Still, the ANSI X3H3 Committee has not totally ruled out Core, preferring to work on it as a possible U.S. standard.

Though both Core and GKS are incompatible with one another, both can provide a device-independent mechanism through which an application program can access a wide variety of physical devices. An important ramification exists concerning ANSI's recent decision to support the GKS as a graphics standard. GKS does not address raster-scanning technology as Core does, which is the most pervasive graphics display technology around. Thus, the decision is not yet made as to which technology will win.

Besides working on an overall graphics standard, ANSI and the ISO are also working on a virtual device interface (VDI) standard for graphics input and output devices; a virtual device metafile (VDM) standard for picture storage by creating a file with VDI-compatible parameters and instructions; and programmer's minimal interface to graphics (PMIG) standards for 2-dimensional and personal computer graphics.

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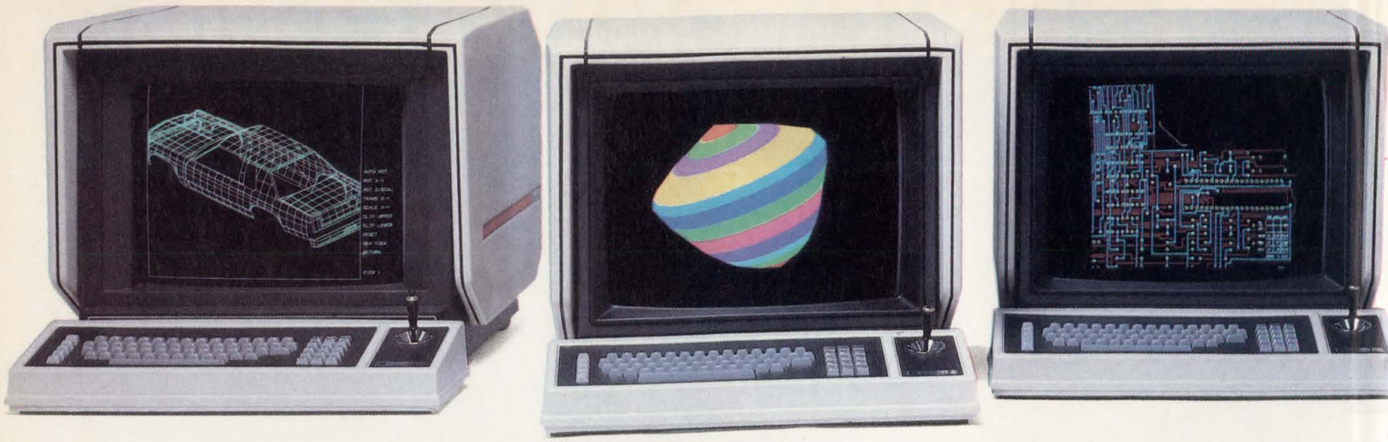

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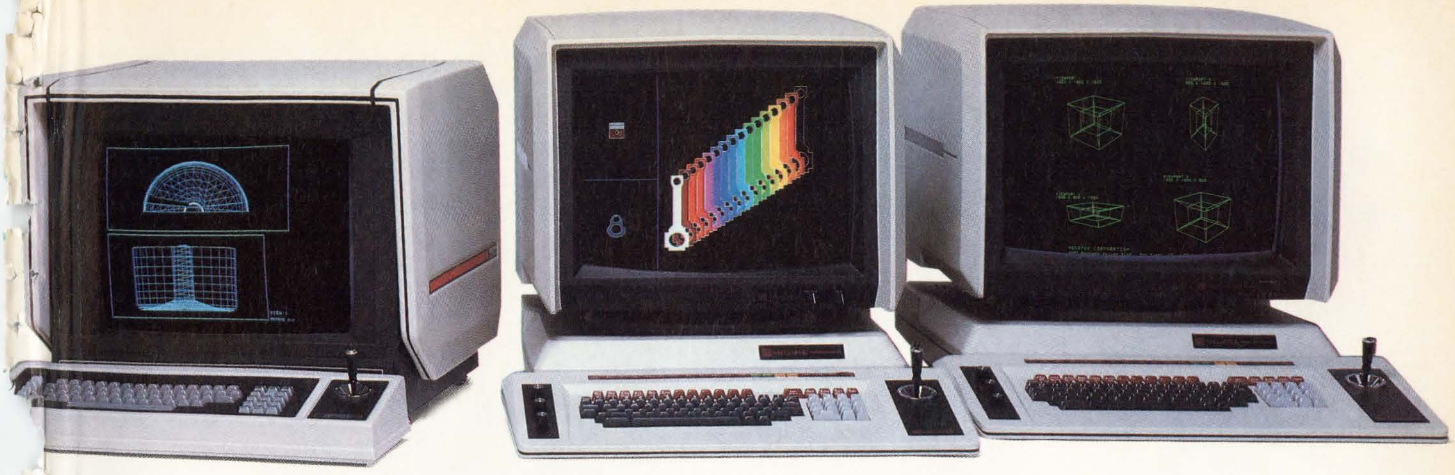

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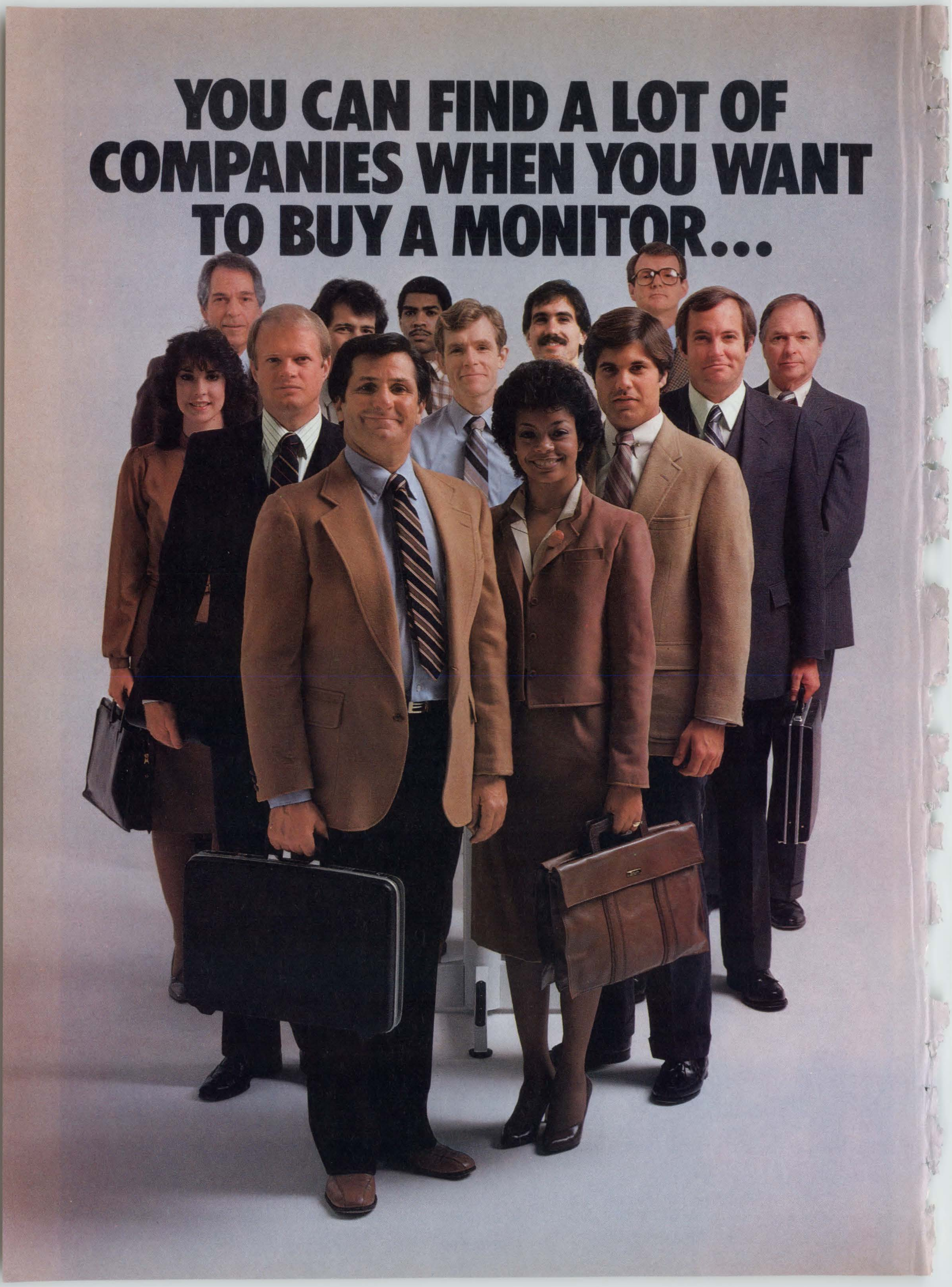
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CIRCLE 86

ADAPTING APPLICATIONS TO THE GRAPHICAL KERNEL SYSTEM

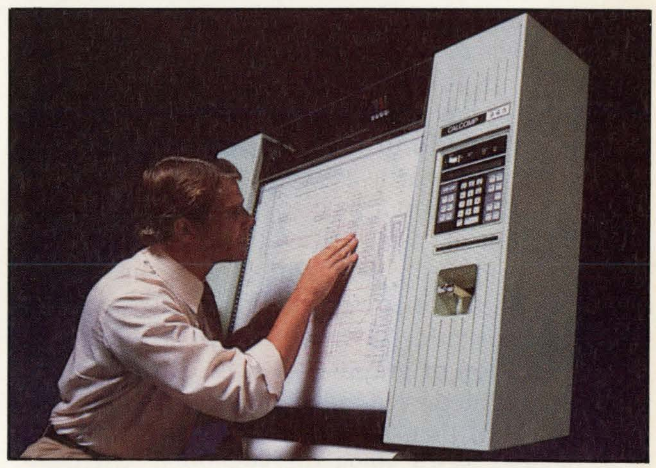
Conversion to this popular standard gives graphics applications portability and device independence. Deciding if conversion is appropriate, however, is up to the programmer.

by David H. Straayer

The Graphical Kernel System is rapidly gaining acceptance as a worldwide standard for computer graphics. It was originally developed by the Deutches Institute für Normung, the official standards-making body of West Germany. The International Standards Organization is in the final stages of converting the Graphical Kernel System from its current status as a Draft International Standard (formal designation: DIS 7942) to an International Standard. ANSI is also in the process of adopting the Graphical Kernel System as an American National Standard. Many vendors, including Tektronix, Sigma, Spectragraphics, Data General, ISSCO, Graphics Software Systems, and Digital Research Inc, have either announced products compatible with the standard or an intention to produce them.

In essence, the Graphical Kernel System (GKS) is a standard for a graphics programming interface—a standard graphics subroutine package. The implications of such a standard, however, extend beyond graphics subroutine packages. This is because the existence of such a standard suggests that specialized hardware will become available to perform graphics functions. Indeed, GKS workstations are already beginning to appear.

GKS hardware availability has far-reaching implications for the future of existing application software. To extend and protect the value of existing applications, many programmers need to decide if conversion is appropriate. Probably the most important reason for converting an existing computer



CalComp's multipen plotter is supported by one of the oldest and proven software interfaces. Because the interface was designed for such X,Y pen plotters, both interactive graphics and filled areas can be difficult to produce. However, its very simplicity aids conversion to GKS.

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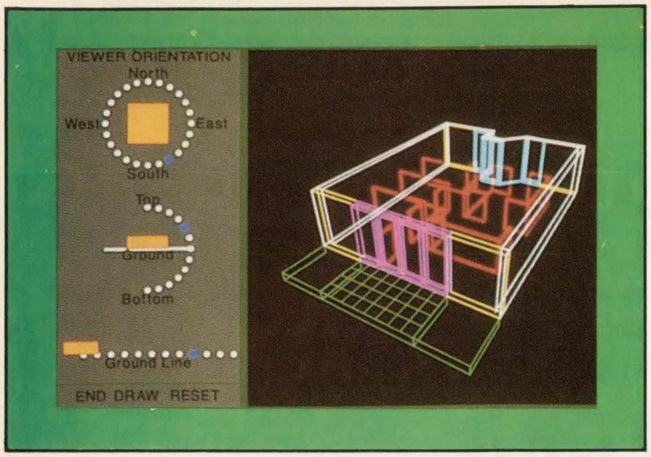


This example of DI-3000 graphics, from Precision Visuals, Inc, is patterned on the ACM SIGGRAPH Core graphics system. It includes 3-dimensional graphics, which GKS does not. Interfacing to GKS should not be difficult, however, since GKS was patterned after the Core.

graphics application to GKS is to enable the software to draw its pictures on a new terminal, plotter, or other graphics device. Although computer graphics devices with improved performance, features, and lower prices are being introduced almost daily, appropriate software is needed to use them.

Most existing software supports graphics equipment that improved devices are rendering obsolete. This software must be replaced or modified to take advantage of these devices. But, software is far from free; in fact, today's computer graphics solutions to real world problems often entail as much software cost as hardware cost.

One option, of course, is to rewrite existing software so that it uses a new piece of computer graphics equipment. The trouble with this type of approach is that it solves the immediate problem, but does not address tomorrow's problem—the next generation of graphics devices. If the application is based on device-independent software, however, it would then be much easier to adapt to a new device. With device-independent software, writing or buying a device driver (a software adapter) often completes the conversion. Thus, the application works nicely. If the graphics software is not based on a device-independent package, then converting to GKS will provide these advantages since it is by design device independent.

Dealing with device independence

Is there any reason to consider converting an application that is already based on a device-independent package? While there is a lot of truth to the old saying: "If it ain't broke—don't fix it," nonetheless, conversion can be justified. First, GKS is an official standard for device-independent computer graphics software packages. Second, as mentioned earlier, much work is being done with it in the computer graphics vendor community, and many GKS-compatible products are expected in the near future. Hardware vendors embrace GKS because it will lead to a large base of compatible graphics software. As more devices that support GKS software are introduced, improved computer graphics technology becomes easier to use. Thus, the strongest argument for converting existing application software to GKS is to make this software compatible with new hardware, and new applications that are likely to be written. In addition, GKS could simplify software maintenance and conversion by having all graphics software based on the same standard.

It makes sense to base software on GKS because GKS also has some significant advantages as a graphics interface. For example, unlike previous proposals, GKS has a published binding to FORTRAN. This binding specifies the actual names and argument sequences for graphics functions. Therefore, if an application is written for one vendor's GKS package, and another vendor's version is substituted later (perhaps to run on a different host computer, or to use a new device not supported by the first vendor's GKS), the original code has an excellent chance of being able to run without any modification. However, GKS does allow the use of special features from particular devices through an escape mechanism. This requires additional work converting programs that use the mechanism. Thus, programming managers should be aware of the problems involved in using nonstandard functions in graphics programs and decide if these functions should be used in production packages.

GKS has a workstation model that makes it easy to use different graphics devices, and particularly easy to use the best features of each device. For example, using color on a color device and dash patterns on a monochrome device for the same graph is simple and does not require a program change. The ability to control and display text as a part of computer generated pictures simplifies application writing. In addition, GKS has powerful segmentation and input systems.

Surveying existing graphics packages

One of the oldest software interfaces to graphics is listed in Table 1. It was originally written to support pen plotters produced by CalComp. Many other plotter manufacturers have supplied CalComp-compatible software for their plotters, and many application programs have been based on this interface. Since the interface was originally designed for plotters, programs that use it are not likely to be interactive, nor are they likely to use many of the newer graphics features such as filled areas or dynamics. This will simplify GKS conversion of CalComp based applications despite the package's device-independent nature.

The PLOT 10 Terminal Control System (TCS) is a software product introduced by Tektronix to support one of the earliest affordable computer graphics terminals in wide use—the 4010. The direct view storage tube (DVST) technology of the 4010 terminal has left an imprint on TCS. Since selective erase is impossible on a DVST, TCS is only partially interactive. It has a rich repertoire of coordinate systems, including a device-independent virtual coordinate system and the device-dependent terminal coordinate system. Although TCS was originally intended to be device dependent, the addition of the 4014 terminal and 4662 plotter to the company's product line resulted in some TCS device independence. There are numerous TCS based applications due to the achievements of the 4010 series of terminals. In addition, many PLOT 10-compatible terminals have extended the life of TCS based application software.

TCS has significantly more routines than the CalComp package, but like the CalComp package, TCS is mostly nonmodal. This means that there are commands to draw different styles of lines, rather than commands that establish the line drawing mode. There are, for example, different routines to draw solid and dashed lines rather than a mode-setting routine that specifies whether subsequent lines are to be dashed or solid. Table 1 shows a typical TCS interface routine. With more routines and input, converting TCS based applications will be more difficult than converting CalComp based applications.

An example of the Special Interest Group on Computer Software (SIGGRAPH) Core software is DI-3000 (Table 1). This class of graphics interface software is based on the Status Report of the Graphics Standards Planning Committee, which operated under the Association for Computing Machinery (ACM) SIGGRAPH. The original status report was published in 1977 and updated in 1979. The Core has been used as a *de facto* standard by computer graphics manufacturers for both software and hardware functions. The Core is not radically different from GKS since early versions of GKS were patterned after the Core.

Tektronix's PLOT 10 Interactive Graphics Library and Megatek's Template® also implement Core functions. However, since no binding of Core functionality was ever published in FORTRAN, all three FORTRAN packages use their own subroutine names and calling sequences. This, along with the failure of ANSI to adopt the Core as an American National Standard, has caused GKS to replace the Core as a computer graphics standard.

Like several other Core implementations, DI-3000 permits 3- as well as 2-dimensional graphics. Since GKS is currently only a 2-dimensional standard, any applications requiring 3-dimensional functions cannot presently be converted to standard GKS. However, 3-dimensional extensions to GKS have been proposed, and there are even products that offer 3-dimensional graphics and GKS compatibility. Core systems also feature segmentation (ie, the ability of a graphics system to store and manipulate parts of pictures), which is unavailable in either CalComp or TCS systems. DI-3000 supports a variety of graphics devices, as do other Core packages. A good software selection is available for such Core systems.

TABLE 1

Typical Graphics Package Subroutine Calls

CalComp
(CalComp Inc plotters)

```
CALL PLOTS...
CALL PLOT(X,Y,IPEN)...
```

PLOT 10 TCS
(Tektronix graphics equipment)

```
CALL INITT
CALL MOVEA(XA,YA)
CALL DRAWA(XB,YB)
```

DI-3000
(SIGGRAPH Core package)

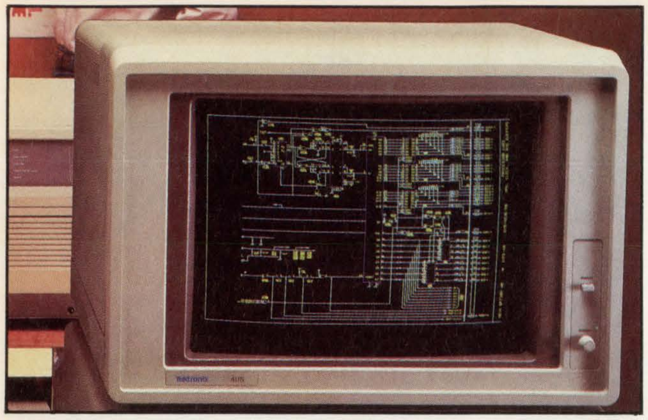
```
CALL JBEGIN
CALL JMOVE(X1,Y1)
CALL JDRAW(X2,Y2)
```

Although GKS is two dimensional and the Core is three dimensional, in most other respects GKS is a superset of the Core functions. Most Core based applications should be relatively easy to convert to GKS. However, applications that use uncommon or esoteric Core functions could pose special problems.

Methods of GKS conversion

There are three different strategies for converting software to the GKS standard. The first is to make GKS look and act like an existing package. The second is to convert the application completely to use GKS. Finally, there is a combination of the two, which is the preferred solution under certain conditions.

Making GKS look like an existing interface entails building a software interface on top of GKS. Such an interface must provide subroutines that match the names and calling sequences of the original application package. This approach is justified if a lot of application software already exists. It is particularly attractive if a source code is



Pictured is an example of Tektronix's PLOT 10 TCS graphics, displayed on a 4115 terminal. Although originally designed to support the 4010 terminal's DVST display, it has been enhanced to deal with more advanced devices.

unavailable for all of the software. In the latter case, it may be the only possible solution. This approach is also advantageous because it does not affect the original source code.

Since GKS is powerful, device independent, and rich in functions, it is usually larger than the original package, and adding a software layer can only make it bigger. However, given that today's computers are larger, faster, and less expensive than those for which many existing applications were written, this will not always be a serious concern. Acquiring the interface software could be a problem, however. While buying commercial packages, where they exist, would be economical and practical, building a custom interface would yield the exact functions needed at a somewhat higher cost. The chief obstacle to buying prewritten interface packages is that none currently exist. As the market for GKS applications expands, however, these packages will no doubt be written and marketed.

Building an interface layer may be necessary if satisfactory commercial software is unavailable. It will be easier to build interfaces for simple systems like CalComp than for complex ones like the Core. The biggest problem will be coping with the heavy device dependence of packages such as TCS. Building such a layer will require a detailed knowledge of the original graphics interface package as well as GKS.

If extensive modification of the source code is called for, then the appropriate method would be conversion of the existing applications to GKS. This approach will also have the largest impact on the original application's source code. Converting an application requires intimate knowledge of the original graphics package, the application program itself, and GKS. However, this strategy is appropriate when there are only a few application programs, or when existing programs are worthy of overhaul (eg, to use new features). One benefit of this approach is a reduction in the application program size, since GKS can handle many graphics operations that the applications programmer previously had to hand code.

Several tools prove helpful when converting software to GKS. For example, source code listings with cross-reference can aid in locating and modifying calls. A more modern method of accomplishing the same goals is to use a good interactive text editor. A user manual for the current graphics package is needed to determine the functions of calls to graphics subroutines. User manuals for the devices supported by current packages show what the calls can do. Then, a good working knowledge of GKS draws it all together.

Generally, the first step in conversion is to identify which parts of the application call on graphics. Next, classify the calls into major types: control functions, actual drawing functions (primitives), calls that modify appearance (attributes), transforms, "windowing" calls, and others. Once the procedure is understood, make a trial recoding and use the system to help debug the software. In graphics, it is often the final display, rather than error messages, that shows whether or not a program is correct.

Taking the hybrid approach

While it is easy to make adapters for packages like CalComp, the complexity of the Core often makes it easier to modify the applications. In such cases, a hybrid approach incorporating parts of the original code and the newly written code is advised. The intent of this approach is to modify the original source code as little as possible and avoid having to construct an adapter that covers all situations. If an adapter is unavailable, and the amount of application code to convert is not too large, this hybrid approach is the easiest (and probably the quickest) method.

The general approach involves making adapters for the most commonly used routines—the graphics primitives in particular. Adapters for initialization and termination routines can aid in the performance of tasks such as buffer management. When these adapters are complete, convert the less frequently called routines on a case by case basis. If a frequently used routine is encountered, it may be beneficial to build an adapter. A major technical problem emerges, however, because GKS does not have a "current position" (which is analogous to the location of a pen on a plotter), a feature usually included in previous graphics packages. This problem is easily solved by creating a current position via a FORTRAN-named common, or an equivalent facility in other languages. Routines, such as text display and line drawing routines that need to know the current position, can access this common information and update it if necessary.

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TABLE 2

Unbuffered Line Segment Adapters

```
SUBROUTINE MOVE(X,Y)
COMMON /CP/ XCP,YCP
XCP=X
YCP=Y
RETURN
END
SUBROUTINE DRAW(X,Y)
COMMON /CP/ XCP,YCP
REAL XS(2),YS(2)
XS(1)=XCP
YS(1)=YCP
XS(2)=X
YS(2)=Y
XCP=X
YCP=Y
C * GPL IS THE POLYLINE ROUTINE OF GKS
CALL GPL(2,XS,YS)
RETURN
END
```

One decision that must be made is whether or not to buffer line segments. Buffering reduces the number of calls to GKS. Applications where efficiency is not critical can tolerate the unbuffered approach. The best illustration of this is found in the code examples in Table 2.

If the example in Table 2 seems inefficient, consider the example in Table 3, which buffers arrays of connected line segments. Note that the current position is maintained as the last point stored in the XB,YB arrays. Not included in this example is a text drawing routine that would flush the buffer and set the current position to match the behavior of the original graphics package. This is often a difficult calculation. Thus, it is wise to make sure the calculation is necessary, since many application programs never use the updated cursor position value. If the application programs being converted draw polylines of many connected line segments—a common occurrence when curves are approximated by short line segments—this method greatly reduces the number of calls to GKS.

There are a few other housekeeping chores to consider in a buffered environment. For example, it is important to ensure that the buffer is properly initialized; an adapter to start up routines (INITT in TCS, PLOTS in CalComp, etc) can help do this. Be sure to flush the buffer before inputting operations and before termination. Also, remember to flush the buffer before most calls to GKS routines in the application. Finally, try to make buffer size very flexible so that it is possible to tune performance by balancing the memory required for buffers with the run-time overhead of calls to the system.

TABLE 3

Buffered Line Segment Adapters

```
SUBROUTINE MOVE(X,Y)
PARAMETER MAXB=100
COMMON /XYBUF/ N,XB(MAXB),YB(MAXB)
IF(N.GE.1) CALL FLUSHB
N=1
XB(1)=X
YB(1)=Y
RETURN
END


SUBROUTINE DRAW(X,Y)
PARAMETER MAXB=100
COMMON /XYBUF/ N,XB(MAXB),YB(MAXB)
IF(N.EQ.MAXB) CALL FLUSHB
N=N+1
XB(N)=X
YB(N)=Y
RETURN
END


SUBROUTINE FLUSHB
PARAMETER MAXB=100
COMMON /XYBUF/ N,XB(MAXB),YB(MAXB)
CALL GPL(N,XB,YB)
XB(1)=XB(N)
YB(1)=YB(N)
N=1
RETURN
END


BLOCK DATA
PARAMETER MAXB=100
COMMON /XYBUF/ N,XB(MAXB),YB(MAXB)
DATA N/0/
END
```

When all the issues are considered, conversion to GKS may not be appropriate for all graphics application programs. Programs that require substantial investment and that show potential for future adaptation to new graphics devices will benefit most from GKS conversion. The ultimate goals of GKS are to provide the portability and device independence of application programs. Indeed, these goals are highly valuable to computer graphics users, but reaching these goals requires an investment of time and money in conversion to GKS.

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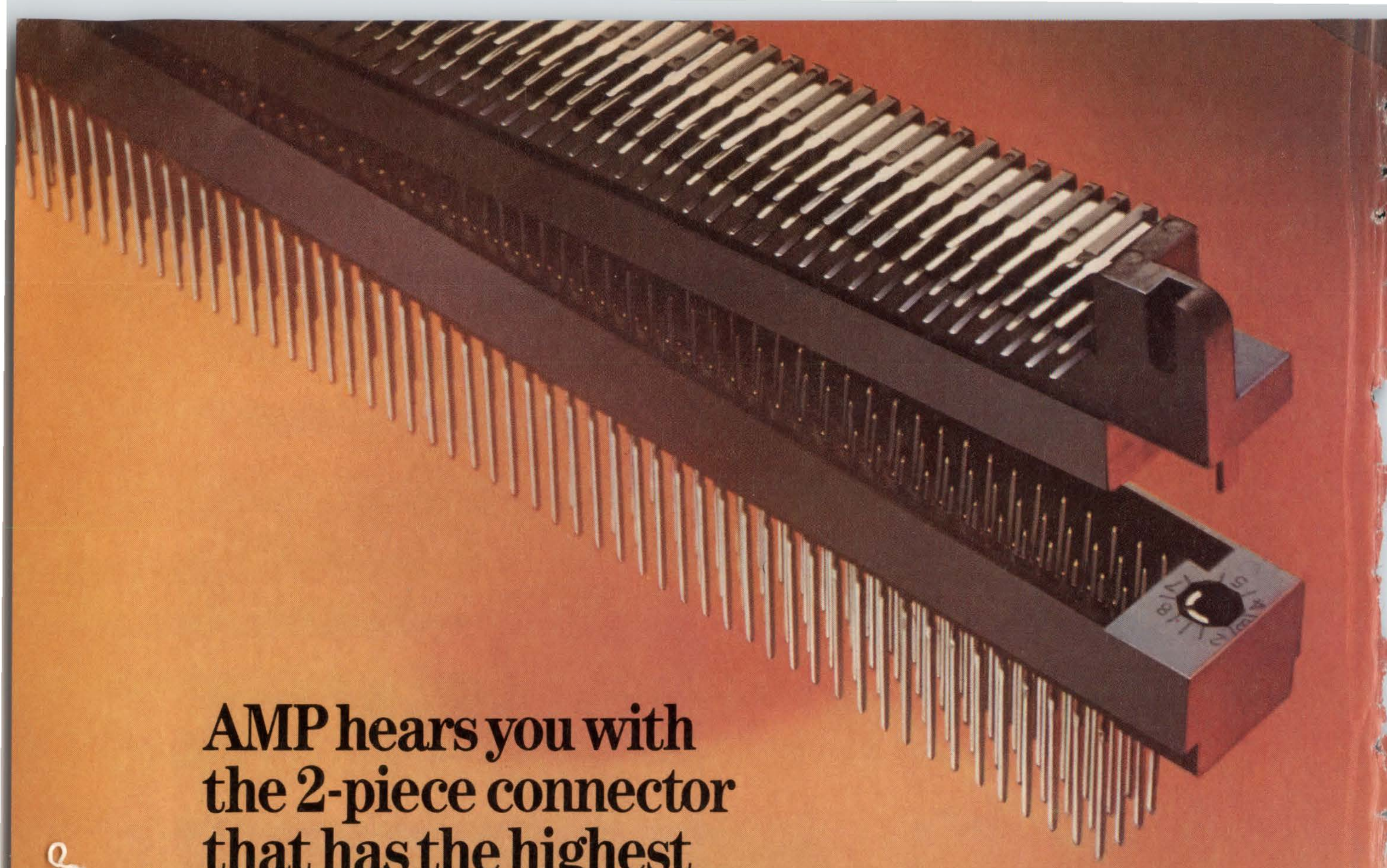

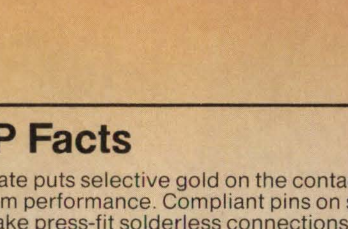

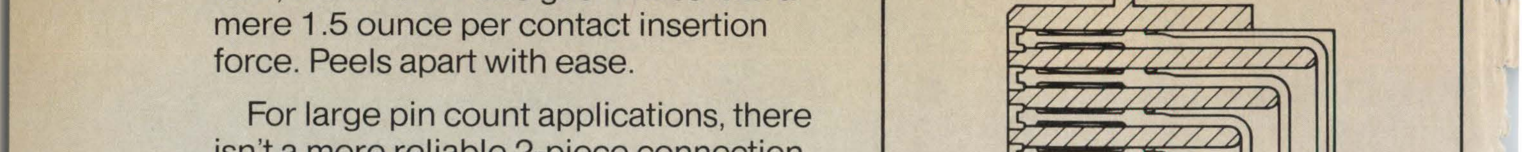

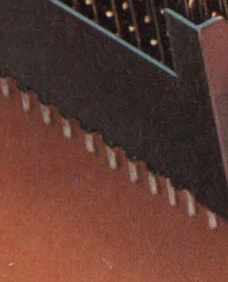

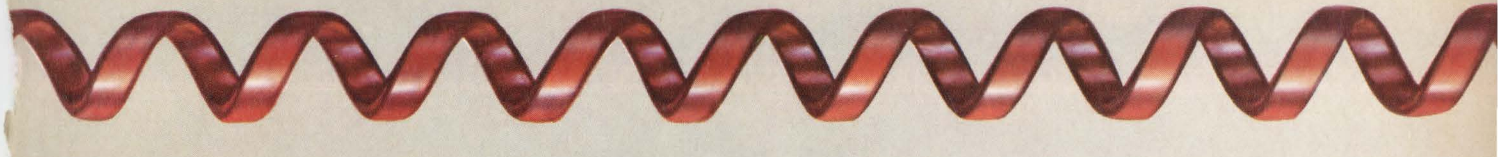

CIRCLE 10

MAMMOTH DISPLAYS THAT MEASURE IN METERS

Plasma displays with pixel counts in the millions and diagonal dimensions in meters are migrating from military to commercial markets. For designers, the result is expanded graphics horizons.

by Donald K. Wedding, Roger E. Ernsthausen, Thomas J. Soper, and Donald J. Ewing

The evolution of large, flat panel, ac gas discharge (plasma) displays has been constant, if not speedy. Developed by university researchers in the early sixties, the first ac gas discharge displays were 1″ x 1″ (3- x 3-cm) units with 16- x 16-pixel display matrices. From this humble beginning, these displays have advanced to the point where meters are the units of dimensional measure and pixel counts are in the millions.

Accompanying this size increase have been multiple control, design, and fabrication problems. As these issues are overcome, large flat panel displays using ac gas discharge technology proliferate. Adding impetus to this growth is the increased emphasis on display size, readability, resolution, and user interface. Although military applications presently hold the lion's share of ac gas discharge display installed bases, these displays are finding their way into commercial application realms as well. IBM, for instance, is offering its recently developed large ac gas display as an option to its system customers.

Photonics Technology recently introduced the first meter-diagonal display with an active area of 80 x 60 cm and 1600 x 1200 pixels. The company designed and produced the meter-sized ac gas discharge (plasma) display under a teaming arrangement with Magnavox Electronic Systems. This high resolution, 1-m diagonal, flat panel display has a resolution of over 400 pixels/cm^2 and a total of about 2M pixels. The active display area is 5.3 ft^2 (0.48 m^2)—making it the world's largest, fully populated, non-projected display, according to the company.

This display is part of a terminal and its control electronics are housed in a window frame cabinet. This cabinet is 4″ (10 cm) deep and surrounds the display panel (see Photo). This packaging design

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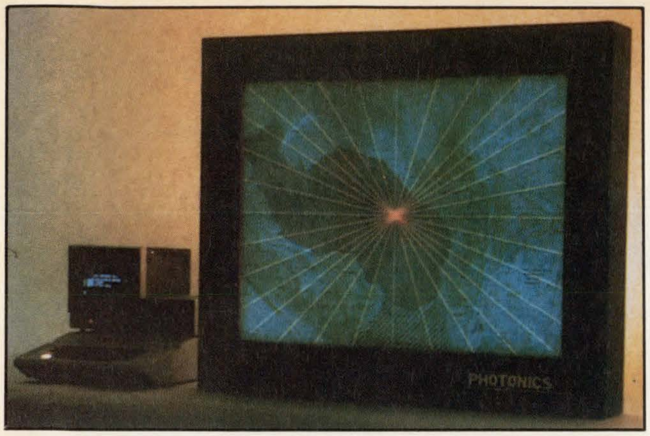
Donald J. Ewing is chairman of computer science and engineering at the University of Toledo. He is also a Photonics consultant, responsible for IBM 581 interface development. He holds a BSEE from the University of Toledo, an MSEE and MSCS from Massachusetts Institute of Technology, and a PhD in electrical engineering from the University of Wisconsin-Madison.



Photonics' meter-sized display terminal features an active display area of 5.3 ft^2. The display is nonprojected, fully-populated, and has high resolution.

preserves display transparency and allows rear projection of film positives and rear mounting of maps to be used as visible reference backgrounds to the dynamic electronic display overlay. Optional features include an interactive touch panel, back lighting, and brightness control.

The display system operates from ac or dc voltages with required power less than 200 W. Using an Intel 8086, a Motorola 68000, or a DEC microprocessor and a high speed interface, the display can be updated at over 3.2 M pixels/s. The system is available with a second integral processor and a 1M-byte memory system for local computation and display management.

AC gas discharge display technology

Sandwiching an ionizable neon based gas mixture between two glass substrates creates the ac gas discharge flat panel display. Each substrate contains an array of parallel electrodes covered by a thin layer of dielectric material (Fig 1). The two substrates are oriented so that the electrodes of one substrate are perpendicular to the electrodes of the other substrate. The substrates are sealed together to form a 3- to 5-mil chamber between the opposed dielectric surfaces. This chamber is filled with the neon gas mixture.

The assembled flat panel contains a matrix of X-Y electrode crossover points formed by the X-axis electrodes on one glass substrate intersecting the Y-axis electrodes on the opposite glass substrate. Each X-Y electrode crossover defines a light emitting pixel; the total number of pixels equals the multiple of the number of electrodes on each axis. Consequently, in a display matrix with 1024 x 1024 electrodes, there are 1,048,756 intersecting pixels.

In an ac gas discharge display, each electrode is dielectrically insulated from the gas. By comparison, dc gas discharge electrodes are not covered with a dielectric layer and are in direct contact with the gas. The presence of the insulating dielectric layers in the ac gas discharge display allows each pixel location to act as a capacitor and store electrical wall charges on each dielectric surface. A simplified model for a single pixel is shown in Fig 2. Here, C_d represents dielectric capacitance, and C_g represents neon gas capacitance. Capacitance is defined as

$$C = \frac{e(\text{area})}{t}$$

where e is the dielectric constant and t is the thickness of the material, dielectric or gas.

The cross-sectional area is the same at each pixel location for both the dielectric layer and the gas. For each insulating dielectric layer, the dielectric constant e is much greater than is the dielectric constant of the gas layer. Also, the thickness of the gas layer is much greater than that of the dielectric layer. Thus, capacitance across the gas C_g is low relative to capacitance across each dielectric layer C_d.

Since voltage is inversely proportional to capacitance, most of the voltage drop occurs across the low capacitance gas layer. A small voltage drop also occurs across the high capacitance dielectrics. This voltage drop across the gas layer causes the electrical charges created by the gas discharge to collect and be stored on the dielectric surfaces.

Typical design parameters affecting the capacitance ratios are as follows: for dielectric layer, e

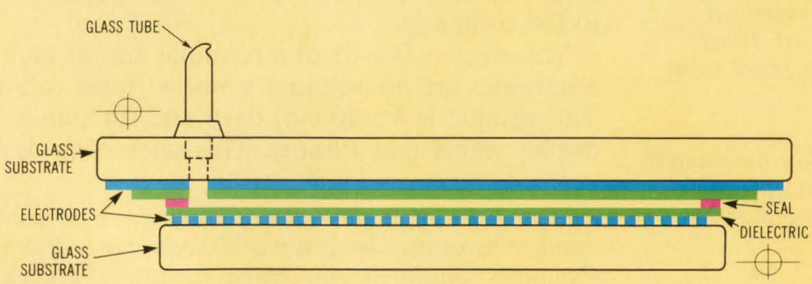


Fig 1 A cross-section of an ac gas discharge display panel reveals a sandwich construction. Substrates containing electrodes (blue) are positioned perpendicular to each other and covered with a thin dielectric layer (green). A gas-filled chamber 4 mils wide contains neon gas that is excited at electrode crossover points. Each point creates a light pixel.

might equal 10 and t might equal 1 mil. For the gas layer, e equals 1, and t could equal 4 mils. These values yield a C_g of 0.25 (area) and a C_d of 10 (area). The resulting capacitance ratio (C_d/C_g) equals 40. In the design of some dielectric layers, e may approach 20 and t may be 0.25 mil with a resulting C_d of 40 (area) and a capacitance ratio of 160.

Electrical charges (electrons and ions) are produced when the gas volume is ionized and discharged at a selected pixel site when proper operating voltages are applied to selected X-Y electrodes. Charges are collected upon the dielectric wall at specific locations defined by the crossovers of opposite electrodes. These charges develop an electrical field opposing the electrical field that created them, eventually terminating the gas discharge for the remainder of the half-cycle and aiding initiation of the gas discharge on the succeeding opposite half-cycle of applied voltage. The stored dielectric wall charges add to and reduce the magnitude of the external applied voltage required to initiate the succeeding discharge. The benefit is that a selected pixel can be maintained in an on state, ie, discharging at each succeeding half-cycle, at a significantly reduced applied voltage. Thus, ac gas discharge displays have an inherent electrical memory characteristic.

Resolving gray-scale and resolution issues

Different gray-scale or variable intensity modulation techniques are used in large ac gas discharge displays. These include ordered dither techniques such as time modulation and pixel-intensity modulation.

The ordered dither technique produces an appropriate arrangement of on and off pixels to provide intensity differences or gray-scale effects. Predetermined dither threshold values are assigned to each display pixel of the matrix. When the intensity of any given picture element is greater than the predetermined threshold value, the pixel is turned on. Otherwise, it is off.

The time-modulation technique varies the amount of time that the pixel is on within the refresh cycle in order to control viewer-perceived intensity. When the pixel is on for a low proportion of the refresh cycle, the perceived intensity is low; conversely, it is high when the pixel is on for a large proportion of the refresh cycle.

With the pixel-intensity modulation gray-scale technique, the sustaining voltage required to provide a pixel bi-stable operation is reduced. This reduced voltage is below the minimum that will sustain the on-state condition in a pixel that has previously been energized by an appropriate exciting voltage pulse. When the sustaining voltage is reduced, as described, and the pixel is energized by an appropriate voltage pulse, enough charge is injected into the pixel so that a discharge continues on successive pixel cycles. But, since the sustain voltage is reduced, the resultant repetitive gas discharge at the pixel site diminishes with each successive cycle until the discharge at the pixel is exhausted. The number of cycles that occurs during the discharge depends on the magnitude and duration of the initial exciting pulse. Therefore, the initial exciting pulse determines perceived intensity.

Quite often, large area ac gas discharge displays are used in applications requiring display transparency for rear projections and/or rear mounting of maps. Selecting the exact display resolution for applications requires consideration of trade-offs between map readability and electrode producibility. Currently available 1024 x 1024 displays at resolutions of about 23 to 25 pixels/cm have 3- to 3.5-mils electrode width with a 60% to 65% transmissivity factor.

For 1- x 1-m to 2- x 2-m displays, 2048 x 2048 pixels will suffice for many applications. Thus, the resolution for these displays will range from about 10 to 20 pixels/cm (100 to 400 pixels/cm^2) with allowable electrode widths up to 7 or 8 mils and electrode matrix transmissivity above 60%. Higher resolutions of 30 to 60 pixels/cm have been successfully demonstrated for smaller panels containing 512 x 512 pixels. A 1024 x 1024 panel at a resolution of about 32 pixels/cm was recently demonstrated in a radar application. Panel resolutions of 400 to 4k pixels/cm^2 are also feasible.

There is no evidence that higher resolution panels up to 1600 pixels/cm^2 have a shorter

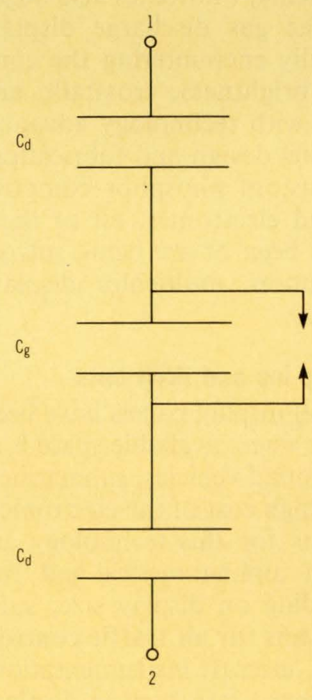


Fig 2 The capacitance model for an individual pixel reveals that the dielectric capacitance (C_d) is much greater than the gas capacitance (C_g). Charges, which are stored on the dielectric, ionize gas at selected pixel sites upon application of an external ac voltage.

TABLE 1

Display Technologies

Projection		Nonprojection		
CRT	Light Valve	CRT	Flat	
			Nonemissive	Emissive
Refractive	Liquid Crystal		Liquid Crystal	Light emitting diode
Reflective	Deformable Oil Films		Electrochromic	Electroluminescent
	Cathodochromic		Electrophoretic	Vacuum fluorescent
	Magneto-optic			Gas-electron-phosphor
	Electro-optic			dc gas discharge
				ac gas discharge

operating life, particularly when the panels have an adequate operating window. Likewise, crosstalk between pixels is not a problem with an appropriately designed, high quality panel.

Color is becoming a greater issue in display systems. Neon components in the ionizable gas mixture produce the traditional orange color of the ac gas discharge display. However, by using gas mixtures with an invisible or colorless discharge, selected photoluminescent phosphors can be excited by photons from the gas discharge to produce a variety of colors. Prototypes of such panels were fabricated in the early seventies under government contract. Government funding for the early color work has terminated because of serious technical problems including very short operating life, lack of brightness, crosstalk between adjacent pixels, and high operating voltages.

In conjunction with high resolution activities and large area developments, Photonics also began developing multicolor ac gas discharge displays several years ago, initially encountering the common problems of life, brightness, crosstalk, and high voltage. However, with technology advances involving innovative panel design and fabrication, special gas mixtures, custom phosphor compositions, filters, and hybrid electronics, all of these prior art problems have been or are being solved. Small area, high resolution, multicolor displays will soon be introduced.

Display technologies: drop-ins and drop outs

AC gas discharge (plasma) display panels have been used primarily in settings where available space is at a premium, such as in ground vehicles, submarines, and aircraft. Due to the high cost of the electronics, most current applications for this technology are military, requiring both alphanumerics and full graphic abilities. Depending on display size, such applications include systems for air traffic control, airborne command post, aircraft instrumentation, naval shipboard, intelligence information display, data recording, tactical and battery computers, army night vision, integrated fire support, telemetry integrated processing, radar or sonar, satellite communication, and briefcase terminals.

Although some commercial applications use segmented character structures, almost no applications use the dot-matrix structure. The commercial or military user can choose from a variety of display technologies, some of which are summarized in Table 1. Among the nonprojected displays, the commercial user has mostly selected the ever-dominant and economical cathode ray tube (CRT). From the nonprojected flat displays, the commercial user has typically selected liquid crystal display (LCD), light emitting diode (LED), vacuum fluorescent display (VFD), and dc gas discharge. Some of the projected displays, particularly the CRT, have also been used commercially.

The commercial road in ac gas discharge has a history of drop outs. In 1977, Control Data Corp switched from ac gas discharge to CRT displays for its licensed Plato terminals. Interestingly, the ac gas discharge display, developed at the University of Illinois, was meant for Plato.

In July 1978, Owens-Illinois stopped producing ac gas discharge display panels and heads (monitors) after trying to develop a commercial market for over seven years. With the exception of a few Plato terminals sold to Control Data and the University of Illinois, almost all of Owens' sales were to a few prime military contractors, including SAI Technology Company and Magnavox, with some direct sales to the U.S. Department of Defense.

Other commercial manufacturers have also dropped the technology, including Texas Instruments (in 1981), and Control Data Corp (in 1982). In May 1981, Magnavox stopped manufacturing its commercial Orion terminal, after producing it for a decade, to concentrate exclusively on the military market. Both a producer and user of segmented and dot-matrix commercial displays, NCR Corp recently stopped operating after a decade; it is now converting to LCDs.

Nippon Electric Corp manufactured and sold panels and monitors for the commercial market

throughout the seventies and advertised in numerous commercial and trade publications. However, these advertisements appear to have ceased during the last three years. The company is now engaged in other flat panel technologies including liquid crystal. Fujitsu, an early player in ac gas discharge display technology, advertised on a small scale and made a few U.S. sales, but mostly sold commercially in Japan and Western Europe. Fujitsu, like NEC, appears to be switching to other technologies such as liquid crystal.

Things are not as grim as they might seem, however, for the ac gas discharge display. Despite those firms who have left the technology behind, IBM announced in March 1983 the availability of its new ac gas discharge terminal, model 3290, as an option to its CRT terminal model 3270. IBM is also offering this 10k-character display on an original equipment manufacturer (OEM) basis through contracted distributors.

Table 2 presents a list of applications with available and future display technologies. As shown in this table, all of the major nonprojected display technologies have been used for small indicator displays, primarily in the commercial market. Most of these displays are segmented except for a few dot-matrix models such as the Burroughs 480-character dc gas discharge.

Larger, page-sized displays of 1k to 6k characters have been used for both commercial and military applications. For example, the U.S. Navy is using a 2k- and a 6k-character ac gas discharge display. The U.S. Army is also using a 2k-character ac gas discharge display. Numerous other commercial and military applications make use of thousands of 2k-character CRTs.

AC gas discharge displays produced up to now have either 2k or 4k characters. The Plato terminal now uses both ac gas discharge and CRT displays with 4k characters. Most of the military terminals marketed by SAI Technology in the past eight years have been 4k-character ac displays. LCD and electroluminescent (EL) have only recently become available in 1k- to 2k-character displays. VFD and gas electron-phosphor (GEP) are only at the laboratory stage of development and must be considered only as a future technology.

For tactical military and for command, communication, control, and intelligence (C^3I) display applications, the CRT dominates because of its low cost. However, ac gas discharge is being specified more often for some programs. Corresponding commercial applications requiring 300 in^2 (1935 cm^2) or more of display are served 100% by CRT.

At present, all large area briefings and status displays are limited to ac gas discharge. Projection displays hold sway in the commercial market, however, with cost as the controlling factor. In the military market, however, ac gas discharge technology is challenging the projection displays developed by General Dynamics, Hughes Aircraft, and Singer Librascope. These projection displays have low resolution (4 to 12 pixels/cm) compared with the much higher resolution ac gas discharge (15 to 40 pixels/cm). However, projection displays do offer multicolors while ac gas discharge is presently limited to a single color (orange, yellow, or green). These characteristics are subject to change in the near future.

Large area displays of the future

During this year and next year, Photonics Technology will introduce a series of large area displays measuring 3 m diagonal. These displays will have an active matrix of from 2048 x 2048 pixels to 4096 x 4096 pixels. However, there are unique process and

TABLE 2

Display Applications and Technologies

Application	Display area (square inches)	Available technologies	Future
Large area briefings and status displays	1000	ac gas discharge	
Tactical and C^3I displays	300	CRT ac gas discharge	GEP
Page-sized display	100 (1k to 6k characters)	CRT ac gas discharge LCD EL	GEP VFD
Indicator displays	50 (6 to 480 characters)	CRT LCD LED VFD dc gas discharge ac gas discharge EL	

equipment problems associated with manufacturing large-sized ac gas discharge displays from 1.5 to 3 m in diagonal. For example, extreme care must be taken in selecting and handling the large, heavy glass substrates to avoid microscratching of surfaces and chipping of edges. Throughout the process, panel substrates must be protected from contaminants. Solvents, moisture, airborne particles, and the like are of great concern. Special protective coverings for the substrates are a must between process and assembly stations.

Large area panels are capital-intensive and equipment for their manufacture is not commercially available. Thus, all of the major processing equipment must be specially designed and built. Procurement of acceptable electrode artwork requires special source development with lead times up to 12 months. Manufacturing large area panels also requires skilled labor, especially for inspection and process control. Inspection times in excess of 300 h per panel are common. In a 1-m x 1-m display, over four miles of electrodes must be microscopically examined.

As display size increases, operational failure at spacer locations becomes a major quality control problem. Accordingly, Photonics has developed a proprietary Microspacer display panel. Prior panels have relied on many spacer rods to maintain uniform gas discharge distance throughout the display area. However, each spacer rod causes up to 40 inoperative or nonfunctional pixels, a serious problem in large area displays. For example, in a 1-m x 1-m display, spacers may cause over 15k pixels to be inoperative. The Microspacer panel avoids this difficulty and provides a display with less than 0.001% inoperative pixels—a total of less than 40 inoperative pixels in a 2048 x 2048 display.

It is likely that large area display terminals of the eighties and nineties will use a nonprojected, fully populated, multicolor ac gas discharge flat display panel with gray scale. Panels will have less than 0.001% inoperative pixels, a resolution of 400 to 4k pixels/cm^2, and a diagonal of 0.5 to 3 m. These displays will compete with CRT, LCD, GEP, and military projection displays. They will also compete in the commercial market as electronic manufacturing costs decline and computer based graphics applications become widespread.

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CIRCLE 93

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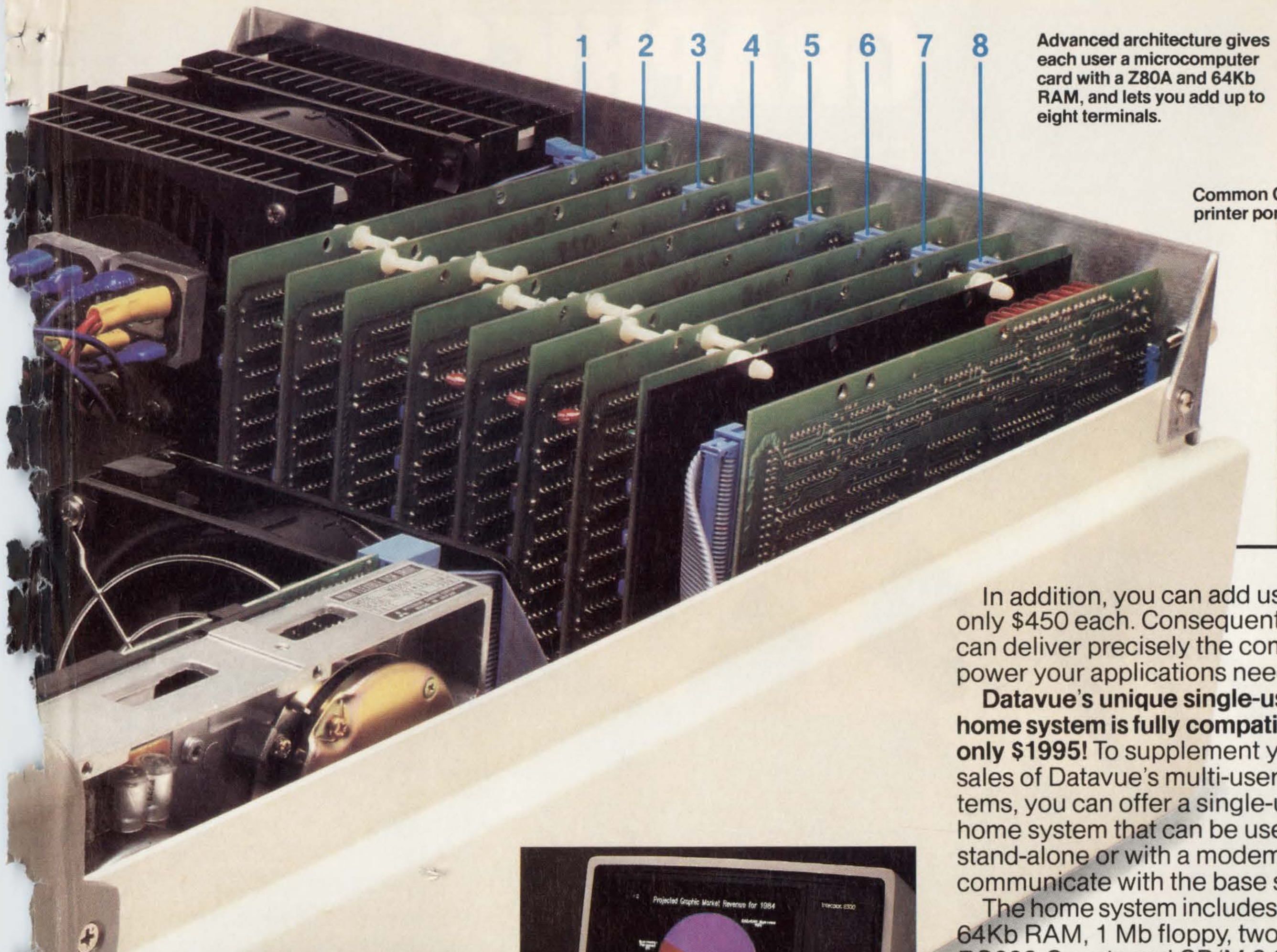

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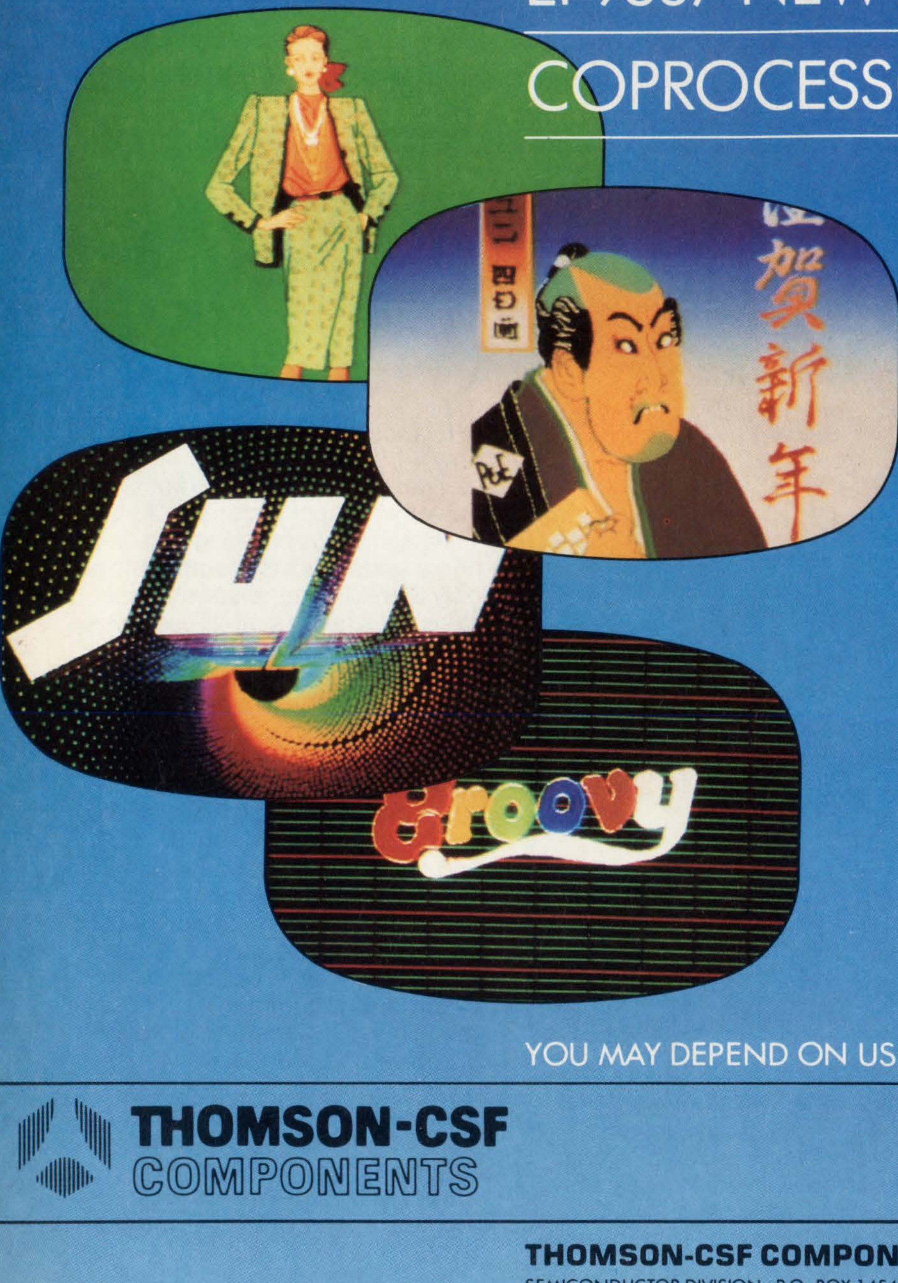
CIRCLE 94

HIGH RESOLUTION GRAPHICS

EF9367 NEW MULTISTANDARD COPROCESSOR (512 x 1024)



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CIRCLE 95

DISTRIBUTED SYSTEM FORMAT AIDS GRAPHICS DEVELOPMENT

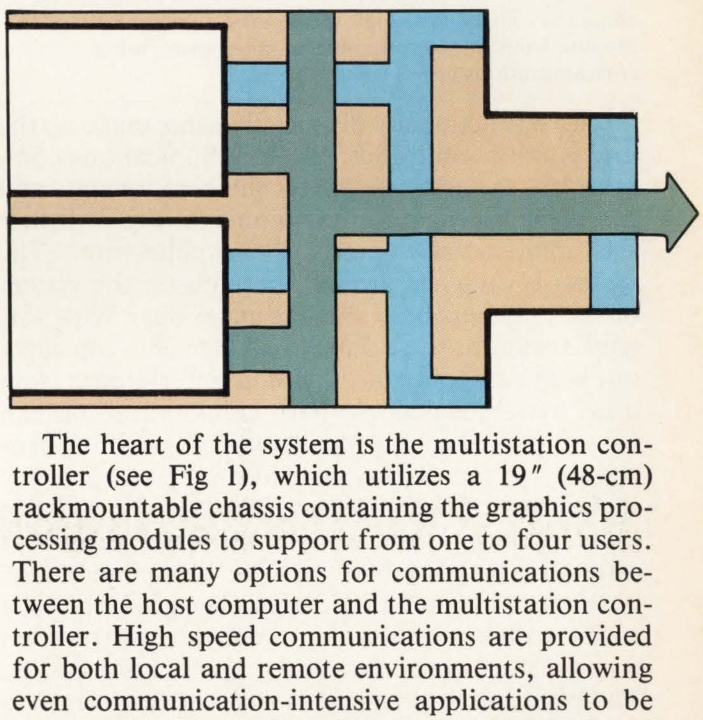
Full-function graphics workstations can access mainframe data bases and can up productivity and project size with local image manipulation.

by John Moreland

Engineering applications requiring image manipulation and graphics data bases have greatly expanded in the past several years. These applications need flexible workstations that have a very high performance color or monochrome raster display, sophisticated local graphics capability, and the ability to be expanded and upgraded to meet evolving requirements. They must also be able to communicate with other workstations and mainframes and have an efficient means for transferring data and programs. In addition, a well-defined software interface with other systems is essential.

To address these needs, Spectragraphics' System 1500 is a system of distributed, high performance computer graphics workstations. Designed as a cost-effective solution for sophisticated graphics requirements, the 1500, built around its multistation controller, provides high resolution displays, realtime raster screen updates, and an advanced concept in graphics database processing.

John Moreland is director of marketing for Spectragraphics Corp, 10260 Sorrento Valley Rd, San Diego, CA 92121. He holds a BA from California Lutheran College and a PhD from Claremont College for work done in probability theory, formal logic, and the theory of languages.



The heart of the system is the multistation controller (see Fig 1), which utilizes a 19" (48-cm) rackmountable chassis containing the graphics processing modules to support from one to four users. There are many options for communications between the host computer and the multistation controller. High speed communications are provided for both local and remote environments, allowing even communication-intensive applications to be supported with workstations up to hundreds of miles from the host computer.

Each workstation can be configured with its own workstation processor, providing local control of all intelligent workstation peripherals. Peripheral options include keyboards, joysticks, data tablets, digitizers, light pens, programmable functions switches, and programmable functions dials.

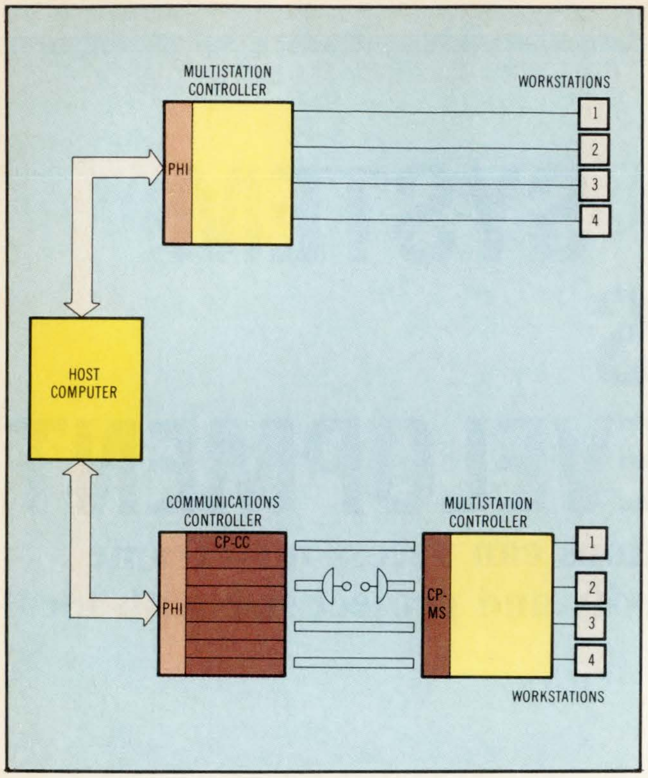


Fig 1 System 1500 supports configurations in which its multistation (MS) controller is directly connected to the host computer, using a parallel host interface (PHI), or in which a communications controller (CC) is connected to the host computer. This allows high speed serial communications to the multistation controller several miles away, using communications processor (CP) pairs.

Three functionally distinct elements make up the multistation controller: the communications components, the graphics processing components, and the display generation components. Fig 2 depicts the multistation controller's architecture. The system is designed around three buses: the system bus, the group bus, and the pixel bus. With this configuration, these functional elements can carry out their respective tasks without interference from other system functions. Host communications can be accomplished independently of graphics processing, as can display generation.

A subset of the Multibus, the system bus allows graphics data transmission to and from the host at rates up to 2.5M bytes/s. The group and pixel buses are of proprietary design. The group bus is a 16-bit wide bus supporting 10M-byte data transfers for vector endpoint data and graphics instructions. The pixel bus is designed to support fast transfers of raster pixel data at 12M pixels/s. This supports a pixel drawing rate of 83 ns/pixel.

Choices for communication

With the available communication options, the needs of a wide variety of computing and workstation environments can be met. These options include serial and high speed parallel direct memory access (DMA) interfaces, as well as a communications controller that supports several high speed formats.

High speed communications between the multistation controller and the host computer are supported by parallel host interfaces (PHIs). These are optional modules that reside in the multistation controller. Each supports DMA data transfers at up to 2.5M bytes/s (depending upon the host computer).

When the multistation controller is located near the host computer, a PHI can be used to attach it directly to the host's input/output bus [Fig 3(a)]. These configurations usually require the controller to be within 100′ to 200′ (30 to 60 m) of the host computer, depending on the particular host involved.

However, when the controller is located more than 200′ from the host computer, the system offers some communication options. One option is the communications controller, which supports communication rates up to 1.544M bps. The communications controller is attached to the host computer using a PHI [Fig 3(b)]. A single communications controller can support up to 16 multistation controllers and 64 workstations, using multidrop coaxial links.

Communications media include coaxial cable; low speed telephone; T1 telephone; and either

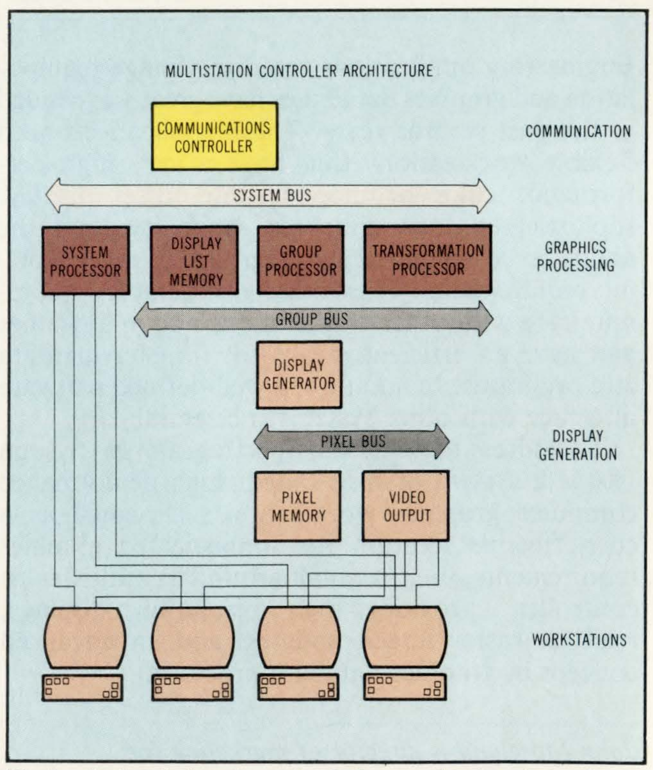


Fig 2 A chassis housing a backplane and printed circuit boards form the multistation controller. The modules include a variety of interfaces, system processor, display list memory, group processor, transformation processor, display generator, pixel memory, and video output.

fiber-optic cable or microwave link, using modems. Supported protocols include both T1 and V.35, with rates up to 1.544M bps between communications processor pairs.

Graphics processing

Three standard modules and one optional module handle multistation controller graphics processing functions. Every controller includes a system processor, a display list memory (DLM) module, and a group processor. An optional transformation processor can be added to improve performance and to add 3-dimensional graphics functions.

The system processor manages all system resources and interactive user input. It has an Intel 8086 microprocessor with a DMA floppy disk controller and nine RS-232 ports. One of the RS-232 ports is for remote diagnostics; four others are dedicated to input from the four workstations. The remaining four ports are unallocated and can be used for low speed host communications (to 19.2k baud) or additional peripheral support. The system processor also has 256K bytes of random access memory (RAM) firmware storage, with a small amount of electrically programmable read only memory for firmware boot routines. At power-up, the processor boots PRISM-MS—the multistation controller's RAM based system firmware—from its mini-floppy disk drive.

One of the system processor's primary tasks is DLM management. The multistation controller uses a memory management system that allows DLM to be allocated to a user depending upon application requirements. Thus, a user is not limited to some fixed portion of DLM, but has all unused memory available at any time.

With the available communication options, the needs of a wide variety of environments can be met.

Another system processor function is managing interactive input from the four workstations. Each workstation, configured with a set of interactive graphics peripherals (keyboards, joysticks, data tablets, etc), has its own workstation processor. The system processor manages communications with the workstation processors and executes the interactive commands issued by each workstation processor, which manages all input from the interactive peripherals. This offloads the task from the host computer. The workstation processor uses an Intel 8051, which multiplexes peripheral input to an RS-232 link to the system processor.

In addition to the system processor, a multistation controller can be configured with up to 1M byte of DLM. DLM is contained on one or two

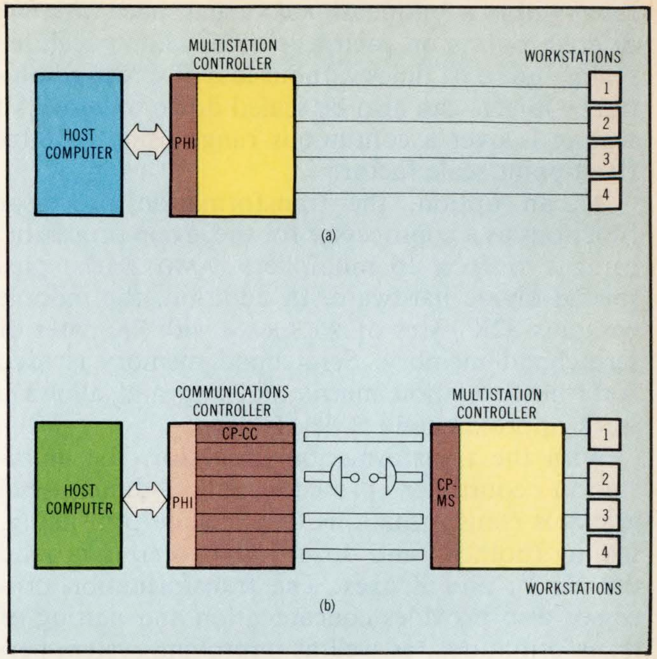


Fig 3 In a local configuration (a), the multistation controller is connected to the host computer using a PHI. Each controller supports up to four workstations (monitor plus graphics input devices). In a remote configuration (b), the communications controller is also connected to the host computer using a PHI. It supports up to eight communication processors. These processors are AMD 2901 based microprogrammable modules capable of supporting various communication rates and protocols.

boards, each of which holds up to 512K bytes of RAM (64K dynamic RAMs). The standard configuration consists of one DLM module with 128K bytes of RAM. Memory can be added in 128K-byte increments.

The DLM is dual ported and can be simultaneously accessed from both the system bus and the group bus. Thus, data transfers can be accomplished between the host computer and DLM while graphics data are being processed for display.

Last of the standard modules is the group processor. A bipolar bit-slice processor using AMD 2901s, the group processor provides all graphics processing functions for up to four users. It contains 64K bytes of RAM for writable control store (WCS), 8K bytes for character and symbol storage, 8K bytes for scratchpad memory, and 4K bytes for table storage to speed computations such as trigonometric functions. Character storage RAM allows user-defined symbols and characters. The 2901 processors use a variable cycle time, optimized for the individual instructions within the system instruction set.

Group processor functions also include graphics command execution, 2- and 3-dimensional graphics data processing, 2-dimensional graphics transformations, viewport clipping, hardware text generation, and realtime fill of complex polygons. All functions are performed within a 16-bit device coordinate system. Thus, graphics data bases are defined within a 3-dimensional virtual space with 64k discrete points on each axis. This allows realtime scaling up to 64 times without loss of screen resolution. Objects can also be scaled down to zero. All scaling is over a continuous range using a 16-bit fixed-point scale factor.

As an option, the transformation processor functions as a coprocessor for the group processor, using two 16 x 16 multipliers (AMD 29517s) plus special divide hardware. In addition, the module contains 32K bytes of WCS RAM with 2K bytes of scratchpad memory. Scratchpad memory is used for transformation matrix stacking and allows a stack approximately 50 levels deep.

With the transformation processor, the multistation controller provides full 3-dimensional graphics transformations that include translating, scaling (both up and down), and rotating around the X, Y, and Z axes. The transformation processor also provides concatenation and nesting of transformations, as well as improving system performance on 2-dimensional transformations.

Moreover, the transformation processor can perform a full 3-dimensional transformation of a vector (including scale, translation, and rotation) in approximately 1 μs. When this transformation capability is combined with the group processor's graphics processing functions, the multistation controller can update graphics displays at rates in excess of 300k vectors/s. This performance is well beyond realtime animation rates.

Both the group processor and the transformation processor perform their functions by accessing graphics commands and data in DLM using the group bus. Vectors, text characters, or other graphics entities are processed and passed over the group bus to the display generator for display processing.

Display processing and generation

The display generator, pixel memory modules, and video output modules perform display processing. These modules do vector to raster data conversions, store rasterized graphics data, control display colors on color systems, and refresh the workstation raster display monitors.

Conversion of vector-formatted data to raster pixel-formatted data, generation of fast hardware character font output, pixel memory array update, and display refresh are display generator functions. It also stores cursor X-Y locations for display list picking functions.

With a proprietary design built from discrete components, the display generator uses a proprietary algorithm for vector to raster conversion at a constant 83 ns/pixel (12M pixels/s). This is more than an order of magnitude faster than most raster devices. Many other raster display devices require the host computer to perform this time-consuming process.

An important characteristic of the display generator's function is that its performance is independent of the angle of trajectory of the vector being converted. Many raster devices specify only their rates for generating horizontal vectors, since this is much faster than for other vectors. The display generator's rate is independent of the angle of the vector.

After being processed by the multistation controller's display generator, raster data are written into the appropriate workstation's pixel memory array. The workstation's display is refreshed from this array.

In addition, each workstation supports up to 4096 simultaneous colors. The number of colors is determined by the number of pixel memory "planes" associated with that workstation. Each multistation controller pixel memory module contains four 1024 x 1024 planes (up to three of these modules can be configured for each display). With one module (four planes), a workstation provides 16 simultaneous colors or gray-scale shades. With two modules (eight planes), a workstation provides 256 simultaneous colors. Master buffered pixel memory architecture enhances display generation performance (Fig 4). A set of pixel memory arrays supports each workstation's display. In addition to pixel memory arrays, the system is configured with one or two master buffers.

A master buffer is a set of pixel memory arrays used in the picture update process. To update a display, the updated image is written into a free master buffer. Once the updated image has been placed in the buffer (this usually takes a fraction of a second), several things happen simultaneously. On the next display refresh cycle, the new image is displayed on the appropriate display. At the same time, the image is copied into the appropriate user pixel memory array and the buffer is erased. After

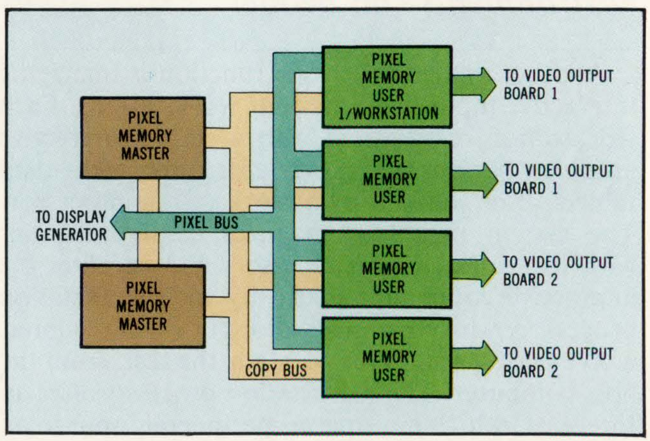


Fig 4 Master pixel memory buffers allow display images to be created without erasing the user's pixel memory. New images are copied to the user's pixel memory during a single refresh cycle.

one refresh cycle, the displayed image has been updated and the master buffer has been cleared for updating another display. As a result of combining master buffering with the display generator's fast vector to raster conversions, realtime screen updates can be done on a raster display.

Both 16- and 256-color systems use a color lookup table that resides on the video output module. This color lookup table allows the colors to be chosen from a broad range of colors, allowing color codes to be matched to an application's requirements or to those of a real-world object. It also facilitates continuous-tone shading of solid objects.

The video output module controls a "live" cursor for echoing user interactive input. Many interactive input devices, such as joysticks and data tablets, require a displayed screen cursor. Under input device control, the video output module displays a screen cursor, updating its position continuously. Because of this "live" cursor function, the cursor can be updated without regenerating the displayed image, and without using the extra pixel memory plane required by many raster systems.

Supporting software

PRISM, a library of host software routines for mini and mainframe computers, supports the System 1500. PRISM was designed to work in conjunction with the PRISM-MS firmware. PRISM's host computer routines interface to the multistation controller and provide protocol formatting and host-dependent driver routines for control of the multistation controller's functions. Function organization is the same in both PRISM host software and PRISM-MS firmware. PRISM and PRISM-MS were written to conform to Graphical Kernel System standards. They provide standard graphics capabilities organized for easy implementation.

In addition, PRISM has extensions for applications that require more than the standard functions. These extensions have been designed to facilitate interactive engineering and scientific applications. They include 3-dimensional functionality, advanced structured graphics database capabilities, and a range of raster graphics features. In each case, the host software provides easy access to the multistation controller's firmware and hardware.

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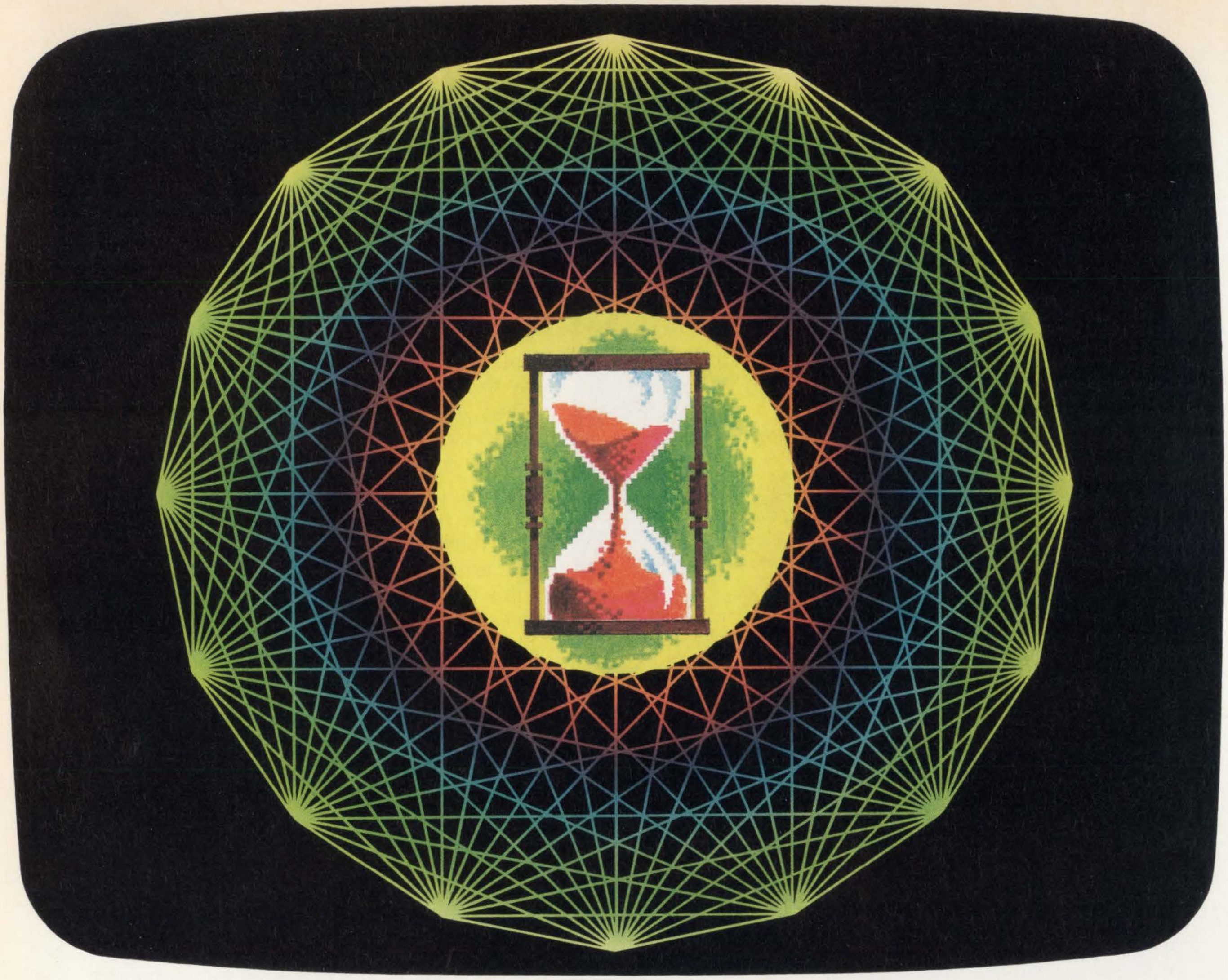

SYSTEM ARCHITECTURE SPEEDS MULTITASKING IMAGE PROCESSING

Specialized hardware and the Motorola 68000 microprocessor enable a digital image processor to independently perform complex image transformations.

by Ted J. Cooper and William K. Pratt

When intelligent controllers and cheaper random access memory chips for image storage appeared in the late 1970s and 1980s, it became economically feasible to store a large number of images in an independent digital image processor. This led to architectures containing arithmetic logic units and multiple lookup tables that could be hardwired to perform arithmetic and logical image combinations. Image convolution became possible by a sequence of addition and spatial offset operations. Although these second-generation processors were powerful, they were also relatively inflexible. Third-generation processors, introduced in the early 1980s, use a bus structure in which image memories, dedicated processors, and a 16-bit microprocessor can be interconnected modularly. Relatively complex image processing algorithms can be rapidly executed by a sequence of point, ensemble, and spatial operations; and general purpose computing can be done as needed. This structure makes possible a standalone digital image processor that does not require host computer support.

These digital image processors are computationally powerful and flexible, but suffer from a limitation: they can usually perform only a few operations concurrently. Many applications need to simultaneously digitize, display, process, and record images for multiple users. The multitasking digital image processor was developed to satisfy this requirement.

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William K. Pratt is president and chairman of the board at Vicom Systems, Inc. Previously, he was an electrical engineering professor at the University of Southern California. Mr Pratt holds a BSEE from Bradley University and an MSEE and a PhD from the University of Southern California.

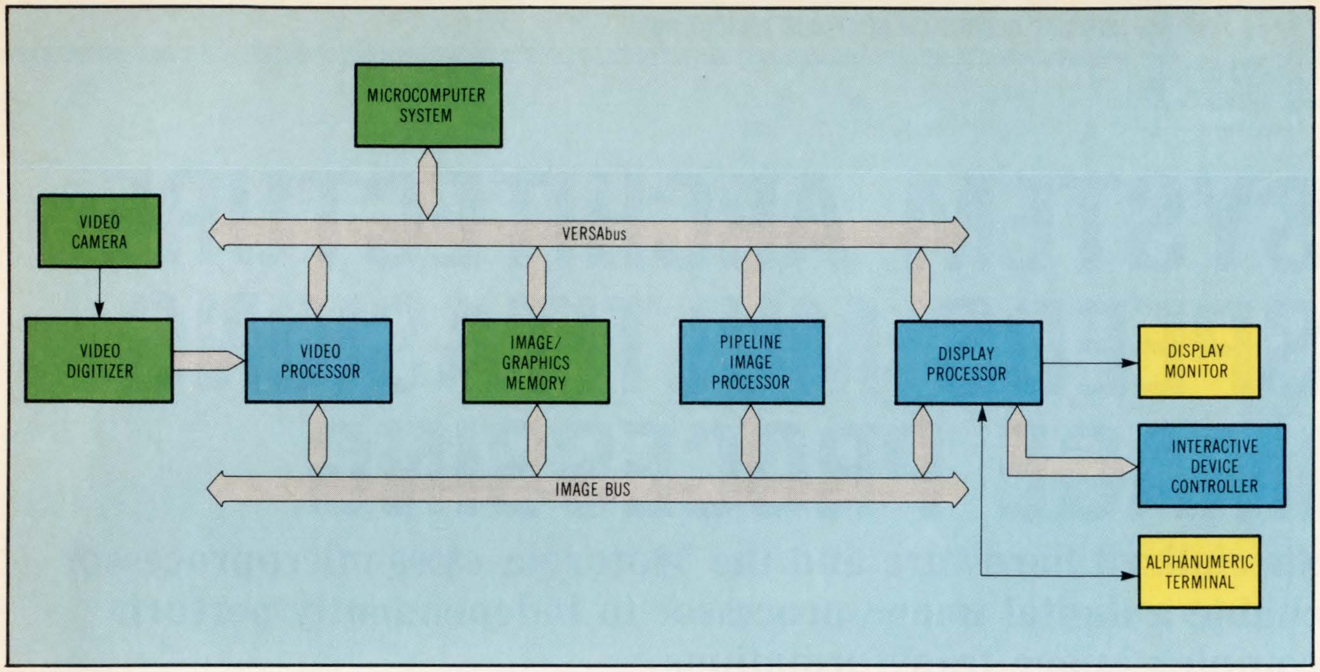

Fig 1 The processor has two primary buses: a VERSAbus and a high speed image bus. High speed image processing modules digitize, store, process, and display images at digital video rates.

The multitasking Vicom digital image processor contains two buses: a microcomputer bus (the Motorola VERSAbus) and a high speed image bus (Fig 1). Attached to the microcomputer bus is a microcomputer system consisting of a Motorola 68000 microcomputer and its associated peripherals. Connected to both buses are high speed image processing modules that digitize, store, process, and display images at digital video rates.

Digital images are input to the system via a high speed parallel port in the microcomputer system. Analog video is externally digitized, then spatially and temporally processed by the video processor before being stored in the image/graphics memory. The pipeline image processor executes image processing algorithms on stored images. Images to be displayed are transferred to the display processor, which then performs such display-oriented operations as zooming and scrolling.

By software command, image/graphics memory can be logically configured into rectangular arrays of height J and width K. This can be done over a wide range. All pixels in the image memory are memory mapped and uniquely addressable by the microcomputer. Pixels can be represented as 16-bit integers for logical and graphics operations or as 16-bit 2's complement numbers for arithmetic operations. In 2's complement form, each pixel is represented as

S.M(1) M(2) . . . M(15)

where S is the sign bit (0 = positive, 1 = negative) and M(1 . . . 15) are the magnitude bits. An imaginary binary point is shown after the sign bit. With this representation, all pixels are scaled in amplitude between ± 1. Black is usually represented as 0.0 and white as 1.0. The negative numbers accommodate image arrays produced by subtractive processes.

A pixel's low order 4 bits, or nybble, can be write protected so that only the microcomputer can modify them. In this way, pipeline processing of the upper 12 bits will not affect them. This feature permits the bottom nybble to store image-associated graphics such as boundary outlines or text. Another application is pixel labeling for image segmentation and classification.

Working faster with the microcomputer system

The complete form of a microcomputer system consists of a Motorola MC68000 microprocessor, program memory, disk and magnetic tape controller, and communication interfaces connected to the Motorola VERSAbus (see Fig 2). The MC68000 microprocessor has a direct 16M-byte address space that permits users to quickly manipulate image memory without resorting to "mapping windows." With this feature, parts of several images can be manipulated at dramatically greater speeds, a benefit that is typical in ensemble and convolutional operations. The MC68000 also eliminates multiple user contention for access to the mapping window. Any user, at any time, can manipulate any image since all image and program memory is universally available. The operating system can limit multi-user access, if necessary, through a memory management unit (MMU).

Another major strength of the 68000 is its large number of available general purpose registers: 15 of the 16 data/address registers are always available.

More user registers allow more data manipulations without having to move intermediate results to a stack. This, in turn, means fewer instructions and less execution time for a given algorithm.

High speed image processing modules provide realtime computation of generalized imaging algorithms. If customized or unique modules are required, the speed of the central processing unit's data manipulations determines the final throughput rate. The large number of general purpose data/address registers, along with their 32-bit width, makes the 68000 microprocessor an excellent companion for dedicated high speed hardware.

In a digital image processor, extending the address space to 16M bytes (64M bytes when separate user/supervisor and program/data spaces are used) gives image manipulation and storage ample room. The 8-MHz 68000 used in the digital image processor performs 16-bit memory to memory moves in 1.6 μs and 16-bit x 16-bit multiples in 8.75 μs. The 16-MHz version of the 68000, to be available soon, will cut these times in half.

By adding an MMU, the 68000 microcomputer system readily adapts itself to multi-user, multitasking environments. The MMU permits many users to share a single copy of a program. This is accomplished by transparent partitioning of memory and data spaces. It also permits programs to be compiled or assembled and linked so that they can reside anywhere in physical memory. This feature is particularly important in realtime applications where context switching between several tasks must be quick and efficient.

The Motorola VERSAdos operating system provides realtime, multi-user, and multitasking capabilities. The system's realtime nature is essential to image processing systems because the acquisition, analysis, and display of data occur at digital video data rates. The VICOMSYS task that operates under the VERSAdos environment provides simple image processing primitives. These primitives handle all standard operations and can be chained together into sequences that emulate the most complex algorithms. Several users can view separate images, using various combinations of display buffers/display generators/graphics generators without affecting each other.

Other users can concurrently edit files; compile programs; and execute full intertask communication, synchronization, and control functions. High level programming languages such as FORTRAN and Pascal, as well as assembly language, are available. Extensive program debugging tools are also offered.

Image processing and multitasking

Most image processing algorithms can be reduced to a sequence of primitive operators involving point, ensemble, and spatial processing. Such algorithms can be efficiently executed in the recursive pipeline structure shown in Fig 3. In this structure, the microcomputer initializes the pipeline controller and one of the processors. An original image is read sequentially from image memory and the pixel stream is directed to one of the processors. The processed image is then stored in a work space in image memory.

The pipeline processor executes single pass in about 33 ms. After the first pass, the microcomputer initializes the pipeline controller and another processor in preparation for the next pass. During the next pass, the previously processed image is directed to a processor, then stored again in a work space. The procedure is repeated until the algorithm is completed.

Cost effectiveness is the major advantage of the recursive pipeline processing technique. Relatively simple, low cost primitive operators can be combined to rapidly execute complex algorithms, typically in 1 s or less. For example, the pipeline image processor can compute an image's moving

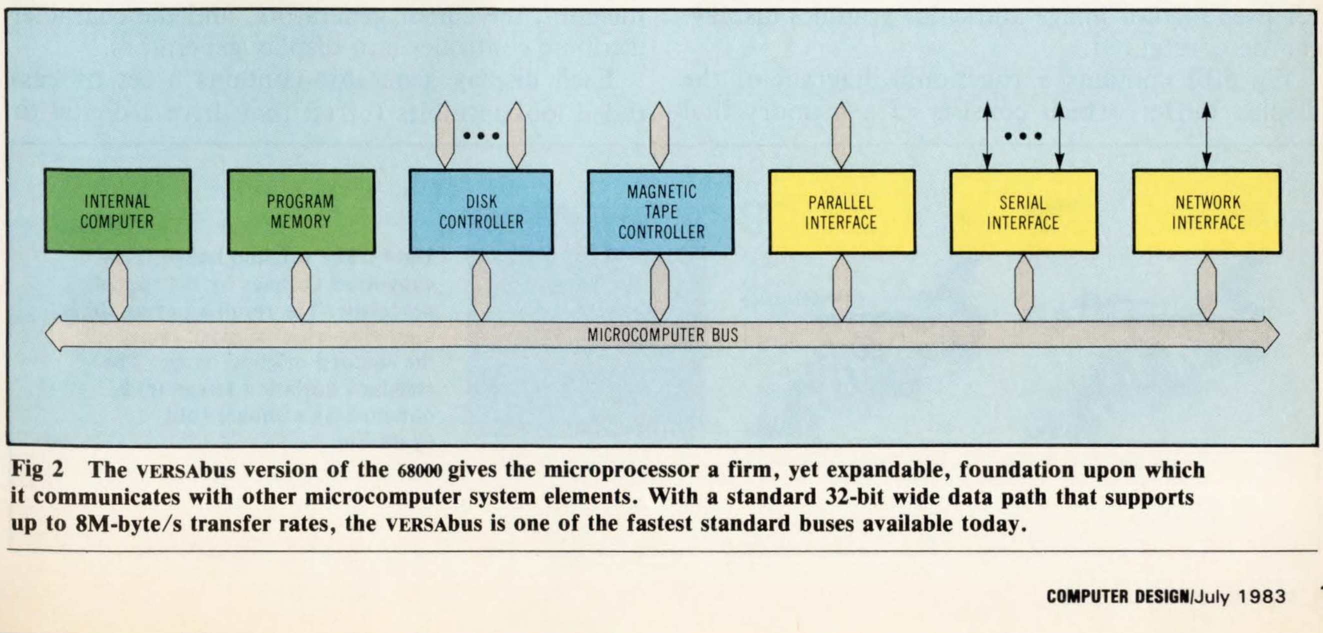

Fig 2 The VERSAbus version of the 68000 gives the microprocessor a firm, yet expandable, foundation upon which it communicates with other microcomputer system elements. With a standard 32-bit wide data path that supports up to 8M-byte/s transfer rates, the VERSAbus is one of the fastest standard buses available today.

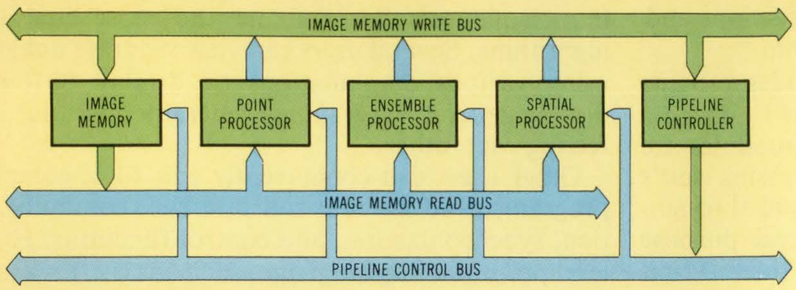

Fig 3 A recursive pipeline structure efficiently executes image processing algorithms. The system's microcomputer initializes the pipeline controller and one of the processors, which then processes a pixel stream read from the image memory.

window standard deviation at each pixel. In the first processing stage, the original image is convolved by the spatial processor with a 3- x 3-pixel convolution mask or kernel. This operation is performed Q times to produce an array M(j, k), which is an L x L moving window average of the original image where $Q = (L - 1) \div 2$. In order to obtain the desired L x L response, the small generating kernel algorithm can choose the 3 x 3 kernels, K, for each repetition.

Following this series of operations, the original image is squared pixel by pixel by the point processor, and then is convolved Q times. This results in the moving window average of the squared image. Next, the point processor squares the mean image M(j, k) and the ensemble processor subtracts it from the squared image's average. A square root operation by the point processor then results in the standard deviation image. Fig 4 shows an example of this process.

Display and video processor features

The display processor consists of display buffers and display and graphics generators. Fig 5(a) illustrates the interconnection for a color image and a red/green/blue color graphics display. Modules for monochrome image and graphics display, or for pseudocolor image and color graphics display, can be configured.

Fig 5(b) contains a functional diagram of the display buffer, which consists of a memory that stores a 512- x 512- x 16-bit or a 1024- x 1024- x 16-bit pixel image. This image is read in at the pipeline rate over the image bus. The image data are read out from the buffer memory at digital video rates to the display generator through a zoom/scroll processor that performs integer zoom up to 16:1 and nonwraparound scroll.

The graphics generator provides four graphics overlay planes, two cursors, alphanumeric text characters, and graphics generation. Graphics can be superimposed over the entire image and also created within a vertical strip that resides next to the image and is one-fourth its width. The two cursors are independent; their shapes are programmable up to one-eighth the display area size. The character font is programmable within an 8-column by 10-row cell, and the text memory contains 256 character entries. Each character can be independently blinked, underlined, or inverted.

The graphics generator contains a microprocessor and a special purpose controller that rapidly draws vectors and arcs and performs high speed filling of closed contours. The processor supports four RS-232-C ports to connect interactive control devices (eg, a joystick, trackball, data tablet, or mouse). Each pixel's graphics bits are read out at digital video rates from the overlay memory, the cursor generators, and the character attribute controller into display generators.

Each display generator contains a set of cascaded lookup tables (LUTs) that drive a digital to

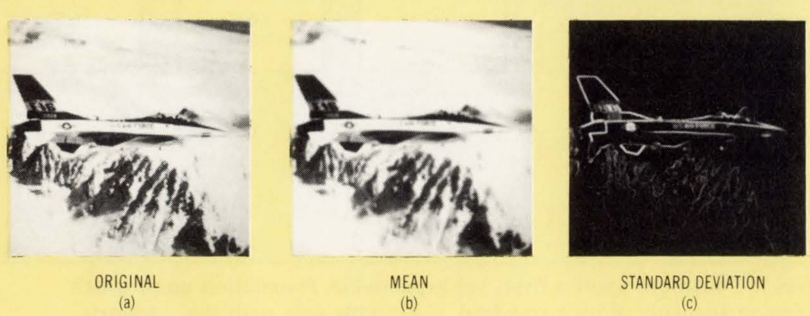

Fig 4 The original image (a) is convolved Q times by the spatial processor. The resulting array (b) is a moving window mean image of the squared original image. The standard deviation image (c) is obtained by a square root operation.

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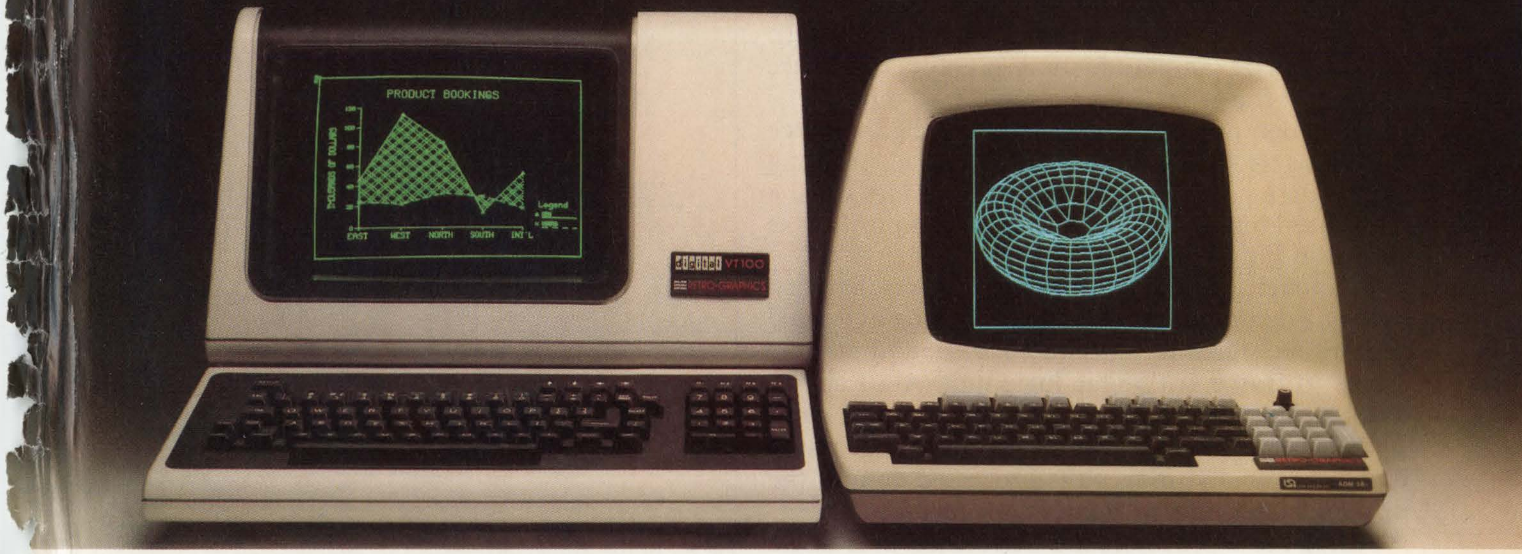

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analog converter (DAC). In a display buffer, the G-LUT merges image-associated graphics data derived from main image memory with display-associated graphics data from the graphics generator. The pixel amplitude data, representing pixel luminance or color component values, enter the Y-LUT for amplitude modification (eg, gamma correction, contrast stretching, and windowing). Finally, pixel amplitude and graphics data are merged in the M-LUT to create the DAC input.

The video processor module in the digital image processor is the gateway for external realtime digital data to enter the system. It resides on the high speed bus and has a functional composition as shown in Fig 6.

Moreover, the video processor acquires digitized data at video rates, provides preprocessing as needed to improve signal to noise (S/N) ratio, and permits frame to frame arithmetic logic unit (ALU) operations on the current data with respect to past data. It then performs LUT operations on the incoming data and, finally, moves the processed data to the display buffer and/or main image memory.

All of these processes are performed in a single frame time. They permit complex video digital data manipulation even before the pipeline processor is called upon to perform other image processing tasks. An excellent example of how these sophisticated features are used is digital angiography in medicine. In this application, a contrast dye is injected into the patient's veins. Then, the physician uses a video digitized X-ray fluoroscopic unit to view the dye as it progresses through the patient's circulatory system. The dye is significantly diluted in the patient's blood by the time it appears in the arteries, resulting in reduced visual contrast. To improve contrast and cancel bone structure, a frame to frame subtraction is made of pre-dye injection and post-dye injection images.

In the video processor, several successive frames of a still object can be averaged to reduce camera or sensor noise effects. To accommodate conventional disk transfer rates, a 512 x 512 image can be averaged and subsampled to produce a 256 x 256, a 128 x 128, or even a 64 x 64 array. When the video processor's 512 x 512 memory has been filled, as many as 64 frames of subsampled video data can be transferred at one time to the display buffer and/or main image memory. While resolution is reduced in the subsampling scheme, the number of frames/s that can be saved on disk is significantly increased.

Because the video processor can do LUT arithmetic and image feedback, a user can perform image addition, subtraction, logarithmic, and masking operations with past data on a frame to frame basis and can view the results as they occur. Raw or uncorrected data can be simultaneously transferred to main image memory and stored on disk so that a

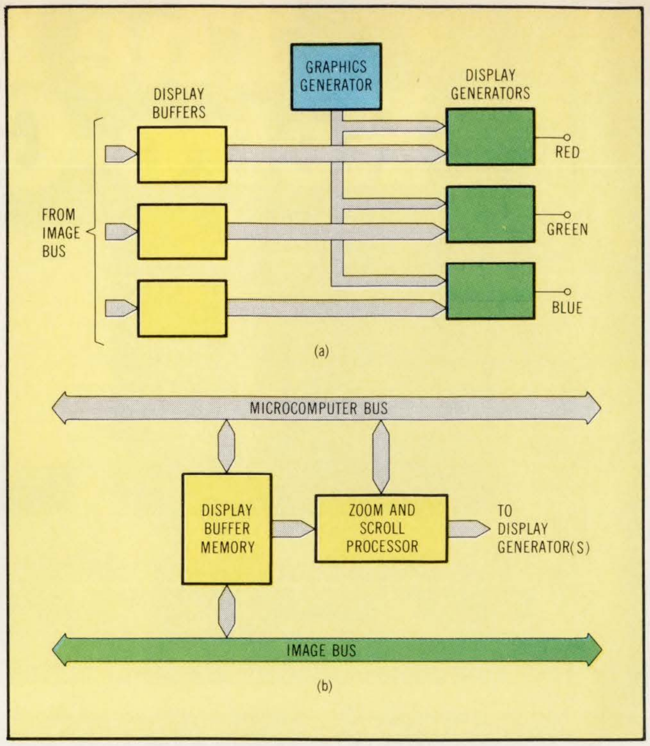


Fig 5 In the display processor (a), modules can be configured for either monochrome or pseudocolor image and graphics display. As shown in the functional diagram (b), image data are read out from the memory to the display generators.

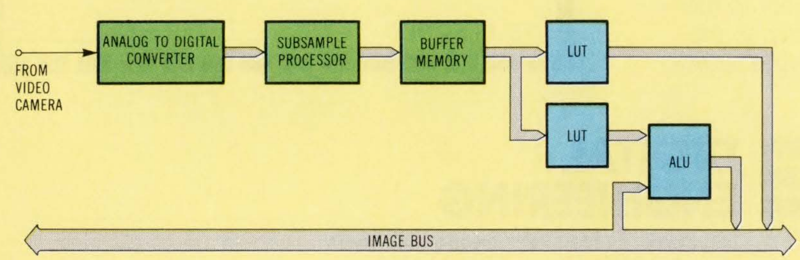
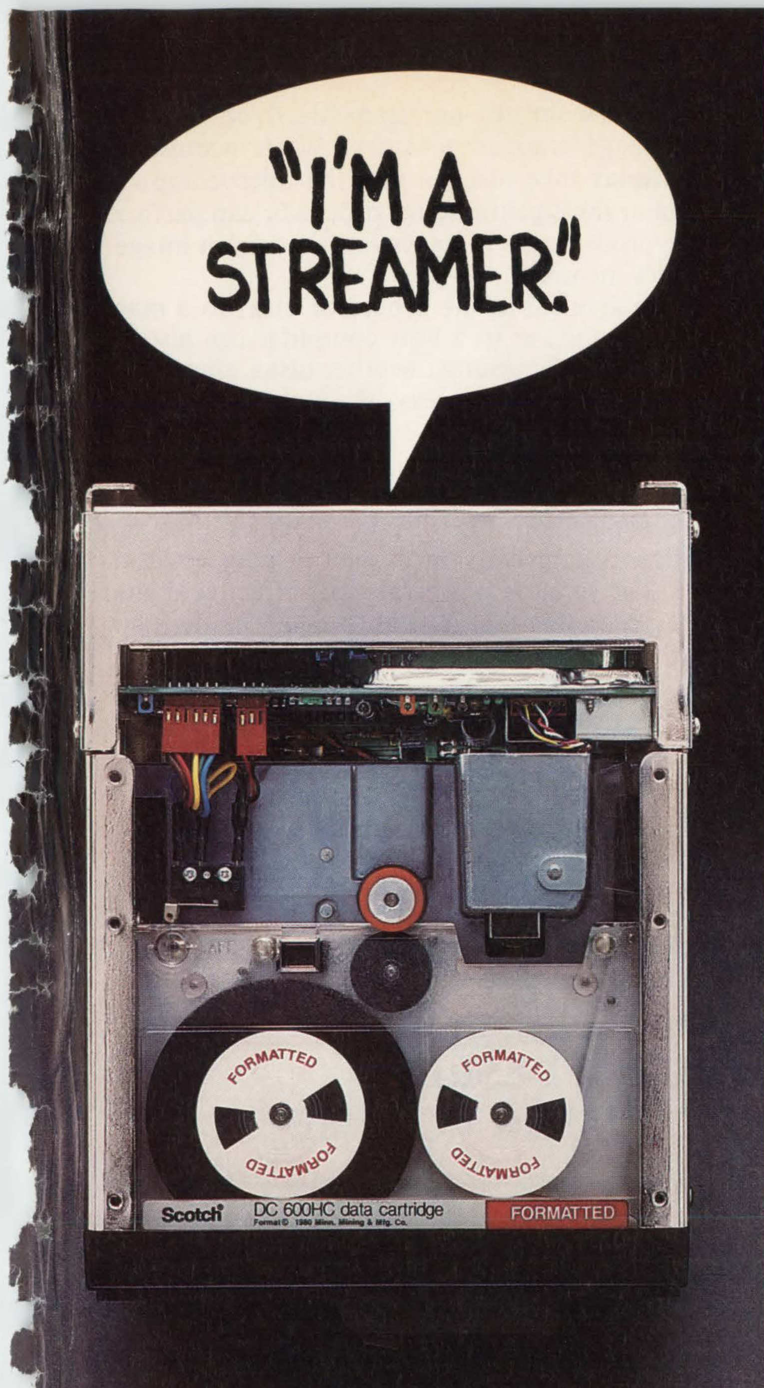
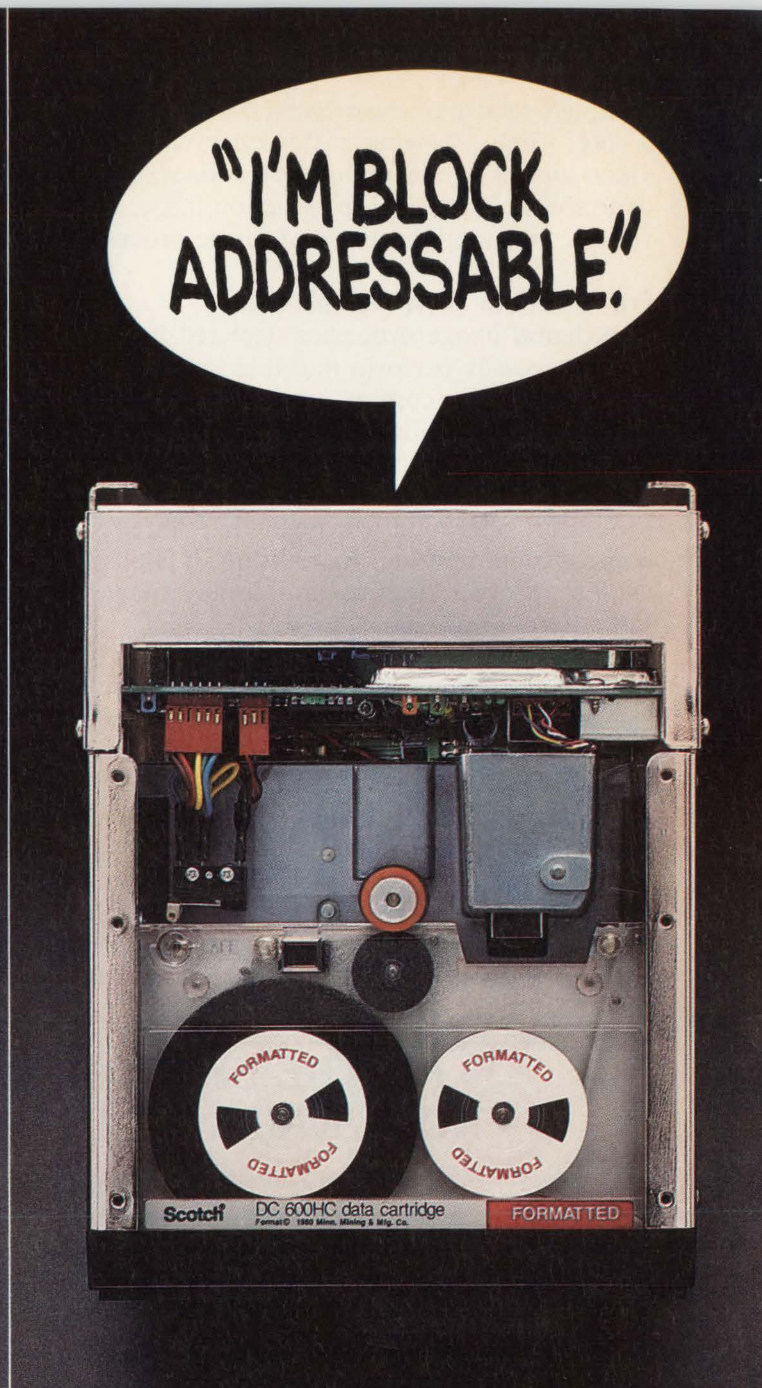


Fig 6 The video digitizer performs many processes in a single frame time to allow complex video data manipulation. Among other tasks, the digitizer acquires digitized data, improves S/N ratio by preprocessing, and performs lookup table operations.





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Frame buffers allow multiple tasks

The digital image processor depicted in Fig 1 can simultaneously perform multiple image processing tasks through its combination of high speed buses, shared image memory, and software control. In the microcomputer system, users can edit and compile programs. At the same time, they can control processor operation through timeshared, MMU-controlled computing. In addition, it is possible to acquire, process, archive, and display images at the same time.

These abilities are available because both the video and display processors contain frame buffer memories. All analog video frames are digitized; the video processor then stores them in a frame buffer. Later, the digital data can be transferred to the image/graphics memory at the synchronous pipeline processing rate.

Concurrent with other processing, images can be continuously displayed and locally manipulated by the display processor, which contains a frame buffer for each displayed monochrome or color image. New images are transferred on demand from image/graphics memory. While acquisition and display take place, either the microcomputer system or the pipeline image processor can perform image processing on images retrieved from image/graphics memory.

Image archival to the processor disk, to a magnetic tape unit, or to a host computer can also be done without disrupting the other tasks, since there is direct memory access through the shared memory.

This generation of digital image processors combines high speed computational elements with image acquisition and display modules that can function concurrently in a multitasking environment. The result is powerful, cost-effective digital image processing that is vital to many modern applications.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 725 | *Average 726* | *Low 727*

Powerful 16-bit portables travel light

Though the dust is far from settled over the portable computer fray, two recent contenders are delivering 16-bit computing power in a lightweight, briefcase-sized enclosure. When it comes to computing and data management power and flexibility, the two indicate similar goals. However, the particulars of implementing these goals and the balance of standard vs optional features differ. Whereas Sharp's 11-lb (5-kg) PC-5000 is more Spartan, enhancing a package of industry-proven elements through a meaty selection of options, Gavilan's 9-lb (4-kg) mobile computer boasts of numerous standard features and several proprietary solutions to the packaging and interface puzzle. Sharp's computer measures in at 12.81" x 12" x 3.44" (32.54 x 30 x 8.73 cm), while Gavilan's is a bare 11.4" x 11.4" x 2.7" (29.1 x 29.1 x 6.9 cm).

Both computers are based on Intel's 8088 microprocessor and support the MS-DOS 2.0 operating system. Besides industry standard packages, the two companies are developing sturdy plug-in applications software to withstand the jostling incumbent on carry-along elements. Sharp is putting its applications in bubble memory cartridges; Gavilan, in proprietary ROM based capsules. Both offer word processing, communications, and spreadsheet analysis functions; to these Sharp adds a database manager and Gavilan, a forms processor. In addition, both load software from standard floppies. Sharp also accesses software through a built-in read/write cassette interface.

The Sharp computer programs in BASIC; the Gavilan, in BASIC and Pascal. Also, Gavilan's computer comes with development system software including a cross-compiler for high level languages, debug tools, capsule and message-holder builders, and access to human-interface and data structuring software. Development software runs on the portable unit or on the IBM PC with the main unit as the target system.

Gavilan particularly caters to the user interface. A proprietary touch panel is key to the company's claim that nonprogrammers can become familiar with the system within 15 min. Controlled by an Intel 8051 dedicated processor, this solid state "mouse" eliminates control functions, gearing the human interface visually toward the display onscreen, instead of toward the keyboard. By moving a finger over the touch panel, a user correspondingly moves a display pointer that identifies the desired function, file, or item. The panel detects X-Y movement at finger speed; proprietary algorithms figure pixel-to-pixel resolution. Built-in system software contains the touch panel control, as well as the operating system kernel, interpreter, and data structuring operations. Data structuring software manages document storage and provides a uniform human interface and data integration across applications.

Gavilan's 9-lb mobile microcomputer comes with 80K-byte internal memory, full-sized keyboard, 420 x 60 graphics/ 66 x 8 alphanumeric display, internal microfloppy drive, and unique "touch pad" user interface. Optional printer and acoustic coupler/modem are each equipped with a self-contained battery pack.

Considering their size, both units offer appreciable main memory and backup storage options. In Sharp's case, 128K bytes of RAM can be expanded to 256K, with 128K ROM for cartridge applications using MS-DOS and GW BASIC. Another 128K bytes of optional bubble memory can be devoted to the applications software. Gavilan uses nonvolatile, static CMOS main memory, providing 80K bytes (with 32K user space) augmented by up to 128K bytes through its plug-in CapsuleWare. Another 128K bytes of processor memory can be added to the system's disk drive and memory expansion module.

Gavilan's built-in 3" drive stores 320K bytes formatted. The drive controller handles a second, identical drive external to the main unit. One of Sharp's 2 optional 5¼" disk drives fits into the main unit to provide 320K bytes formatted; its second drive attaches externally.

Each machine features a flat LCD that folds over its full-sized keyboard. Sharp's display resolution is 640 x 80 pixels, while Gavilan's is 420 x 60 pixels. Both have bit-mapped graphics. The displays shape up into 8-line x 80-col and 8-line x 66-col formats, respectively. Though Gavilan's 66-char line presents a minor drawback, the computer includes an interface that allows it to hook up with full-screen video displays using standard software. Sharp's keyboard includes 8 soft function keys, whereas Gavilan eliminates keyboard entry of control functions by designating 10 function areas on its touch panel.

(continued on page 208)

(continued from page 207)

Sharp's PC-5000 portable microcomputer offers 128K bytes of RAM, 640 x 80 graphics/80 x 8 alphanumeric display, and full-sized keyboard with 8 programmable function keys. The 11-lb unit accepts a range of peripheral options including printer, audio cassette, minifloppy disk drive, and 300-bps auto-dial modem.

In both cases, I/O interface is via RS-232-C. Gavilan has an integral 300-baud modem and direct phone interconnection with an optional acoustic coupler/modem that allows the portable unit to communicate with other computers over standard phone lines. Sharp's optional 300-bps, 10-key auto-dial modem plugs into phone lines with a standard Bell jack. It is also equipped with a speaker for 2-way conference calls.

Printers are optional in both units, although they plug into either computer without extending the footprint. Sharp's high density, dot-matrix thermal impact printer produces near letter-quality copy in thermal mode on thermal paper. It will also print with carbon ribbon on plain bond. The printer produces 80 chars/line, 12 cpi or 66 chars/line, 10 cpi; print speeds are 37 or 30 cps, respectively. Gavilan's 50-cps thermal ribbon printer outputs single-sheet correspondence quality copy on plain bond. The 80-col unit comes with its own battery pack.

Both main units power from built-in battery packs and ac adapters are standard in each. Base price for the PC-5000 is \$2500; the Gavilan mobile computer is \$4000. **Gavilan Computer Corp**, PO Box 5004, Campbell, CA 95008; **Sharp Electronics Corp, Systems Div**, 10 Sharp Plaza, PO Box 588, Paramus, NJ 07652.

Circle 261—Gavilan Computer Corp
Circle 262—Sharp Electronics Corp

Minifloppy drives top 3M bytes per diskette

Two 5¼" drives provide twice the nominal industry standard per-disk data capacity, storing over 3M bytes of data on a single diskette. Meanwhile, standard interfacing and a 5¼" form factor facilitate upgrades from lower capacity systems. Model 1560's interface is functionally compatible with SA460-type minifloppy drives, while model 1860 interfaces with SA850-type 8" floppies. The double-sided drives use UHR-II high coercivity 600-Oe flexible diskettes and record data in FM, MFM, or M^2FM encoding format. Each drive transfers data at 500k bps; average rotational latency is 83 ms with 2-ms track to track access time. Average seek is 88 ms.

Proprietary features developed for the company's Minipac 5¼" floppy disk cartridge drives (*Computer Design*, Sept 1981, p 95) provide 9.5k-bpi recording densities with 170-tpi track density. In both drives, an Intel 8051 microprocessor with 4K PROM controls a closed loop servo system that handles realtime control functions. It manages head positioning and compensates for dimensional changes in the diskette caused by environmental variations or misclamping errors—without embedded servo data in the data tracks. The system also accommodates database conversions and software developed for 48-, 96-, and 100-tpi formats.

Moreover, single-element read/write heads have a tunnel erase feature that stores erased data between tracks. Positioning the heads to one reference track on each diskette instead of on a drive assembly ensures interchangeability and eliminates track 00 adjustment and head alignment.

A photoetched optical scale on the head carriage defines track centerlines after the reference track is analyzed. Scale lines are 590 μin apart; track centerlines are 5.9 mils (10 scale lines) apart. A 1.8° precision stepper motor attached to the read/write head carriage provides accurate positioning and reduces access times; the head carriage moves in 59-μin increments.

Weighing just 2.5 lb (1.1 kg), models 1560 and 1860 mount in a 3.25" x 5.75" x 8" (8.25- x 14.61- x 20-cm) cabinet. In quantity 500, the drives cost $370 each. **Amlyn Corp**, 2450 Autumnvale Dr, San Jose, CA 95131.
Circle 263

Ethernet compatible IBM PC system executes spoken commands

Templates storing up to 200 words provide the vocabulary for a voice-actuated computer networking system. Separate vocabularies can be loaded and unloaded to accommodate different applications and operators, then saved on disk for later use. The voice recognition unit can be trained to respond to a particular voice for each vocabulary. Transferring vocabulary files via Ethernet lets users take advantage of voice recognition on any properly equipped computer in the network from a remote telephone.

Basic configuration of the ComNet Executive consists of IBM Personal Computers equipped with a 10M-bps Ethernet link over thin coaxial cable; the Ethernet Companion expansion board, which handles voice digitization, storage, and display; and a Bell 103/212A modem. The ComNet network supervises tasks like Winchester disk sharing, print spooling, and remote job execution. In addition, it supports an electronic mail function that carries spoken or keyboard-input messages. A message can be heard or read from any node, as well as sent or received over standard phone lines from a remote location.

Though the network supports multiple servers—each equipped with a hard disk—server disk drives can support data storage and retrieval for other network terminals. One server will support a network of IBM PCs with neither floppy nor hard disk drives.

The hardware key to the network is its Ethernet Companion board, which converts voice signals to data signals, then back again. Speech can be digitized at any node and sent to any other node for storage and/or replay. Special voice functions include annotated text, store/forward, and forward/store.

Direct-connect 300- or 1.2k-baud modem comes with automatic DTMF pulse/tone dialer and optically coupled auxiliary ring indicator output. An additional voice circuit allows the modems to transfer voice or data in both directions. Telephone emulation software includes single-line CBX support and lets users specify access codes for network security.

The company is designing software geared to accept voice recognition input. ComNet Executive system with voice recognition and software costs $2995 quantity-one. **Tecmar, Inc**, 23600 Mercantile Rd, Cleveland, OH 44122.
Circle 264

A Lot More Than Meets The Eye

Sure, our CM4000 display module features brilliant, full color spectrum, high resolution graphics and precise alphanumerics. Very impressive indeed! But, turn a CM4000 around and you'll find a display with a lot more going for it.

The CM4000 also boasts the industry's tightest convergence specifications: 0.2 mm center, 0.5 mm corners. The CM4000 generates up to 2,600 characters at horizontal scan rates ranging from 15-25 KHz. In our exclusive, Step Scan Plus™ mode it automatically maintains full vertical display size for "eye popping" full-screen graphics.

In addition, Motorola engineers designed the CM4000 to operate on less power. The resulting reduction in heat dissipation means longer life. In fact, the CM4000 was designed for an MTBF goal of 20,000 hours!

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MOTOROLA INC.
Display Systems

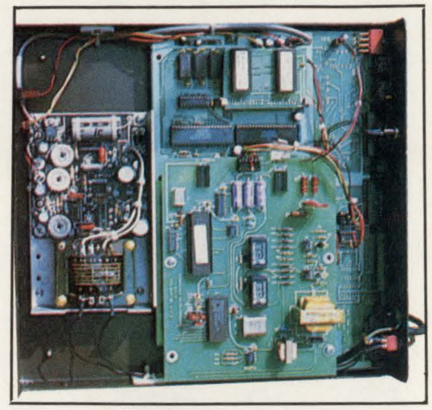
CIRCLE 105

Multiprotocol communications controller ensures data security

A hardware independent communication gateway controls access to shared resources between computers with different protocols. Through the ETC 140 controller, any type of terminal—from mainframe to microcomputer—can talk to an intelligent modem, printer control buffer, time of day/date clock, and hardware encryption unit. Automatic online electronic messaging provides remote access while the system concurrently performs other tasks, such as printing or communications.

In addition to uploading and downloading data and protocol formats, system monitors feature interactive command structure, transparent control codes for automatic operation, and monitor control transfer. Local and online data encryption and error correction overcome security problems often encountered in local area networks. A proprietary encryption algorithm surpasses the NBS standard, while multiple-key encryption is available for greater security. Programmable encoding formats handle serial data interface with disk and tape units as well as with data channel formats. Manchester, NRZ, NRZI, FM0, and FM1 methods are supported.

Based on a 6809E central processor and a 1-MHz system clock, the Bell 103/202 compatible unit offers user selectable transmission rates of 300 or 1.2k baud. Moreover, the controller arbitrates between telephone lines and synchronous or asynchronous protocols at speeds from 45 to 19.2k baud. System memory comprises 16K RAM, expandable to 64K, and 8K ROM, expandable to 24K. In addition, the controller has two 8-bit parallel ports and 4 RS-232 serial ports (RS-422 optional). Each of 2 identical programmable serial interfaces supports 2 serial channels that can be programmed individually for asynchronous or synchronous operation in a variety of formats. The channels also support RS-242 modem control signals.



The 4-user, multitasking ETC 140 system costs $1595. **Computer Development Inc**, 6700 SW 105th St, Suite 200, Beaverton, OR 97005. **Circle 265**

Bisync/Async interface gives micros a direct line to mainframes

A single-unit communications board with protocol converter and hard disk store/forward device makes it possible to sequentially load different protocols. This eliminates the intermediate dumb terminal or frontend controller link usually employed for connecting microcomputers with mainframes. Just a year after entering the microcomputer market, the company is announcing this communications board which enables its 8-bit System 800 and 16-bit System 1600 microcomputers to follow 4 IBM mainframe protocols: Async, batch-processing Bisync 3780, Bisync 3270, and Bisync HASP.

Async mode offers a store/forward function that transfers files to mainframe systems such as IBM, CDC, Hewlett-Packard, DEC, Prime, Data General, and Honeywell. While looking like a terminal to the host, the interface can cause backup files to accumulate, then send and receive several together.

Intelligent batch-processing Bisync 3780 mode makes the system look like an IBM 2770, 2780, 3741, 3780, or a CPU. In Bisync 3270 mode, the interface communicates with any IBM network as if it were a 3270-type terminal—thereby allowing the computer to receive files on disk as if the data were going to a printer. Finally, Bisync HASP mode makes the microcomputer functionally equivalent to an IBM 3777 programmable terminal or System/360 model 20 CPU. In this case, the computer emulates a HASP multileaving workstation.

Two asynchronous I/O ports are standard; one connects directly to the microcomputer's CPU while the other goes to the mainframe. Two ports can be added to handle additional traffic. The company anticipates that users will soon operate the 4 communication modes within the same computer. Existing series 800 and 1600 units can be field upgraded with the communication enhancement.

Moreover, Microsoft will supply MS-DOS 2.0 operating system software for TAB's 16-bit machines. This will make the computers compatible with about 90% of 16-bit application software, as well as with IBM's PC-XT microcomputer. CP/M-86, MP/M-86, and CP/NET operating systems are already standard. **TAB Products Co**, 1451 California Ave, Palo Alto, CA 94304.
Circle 266

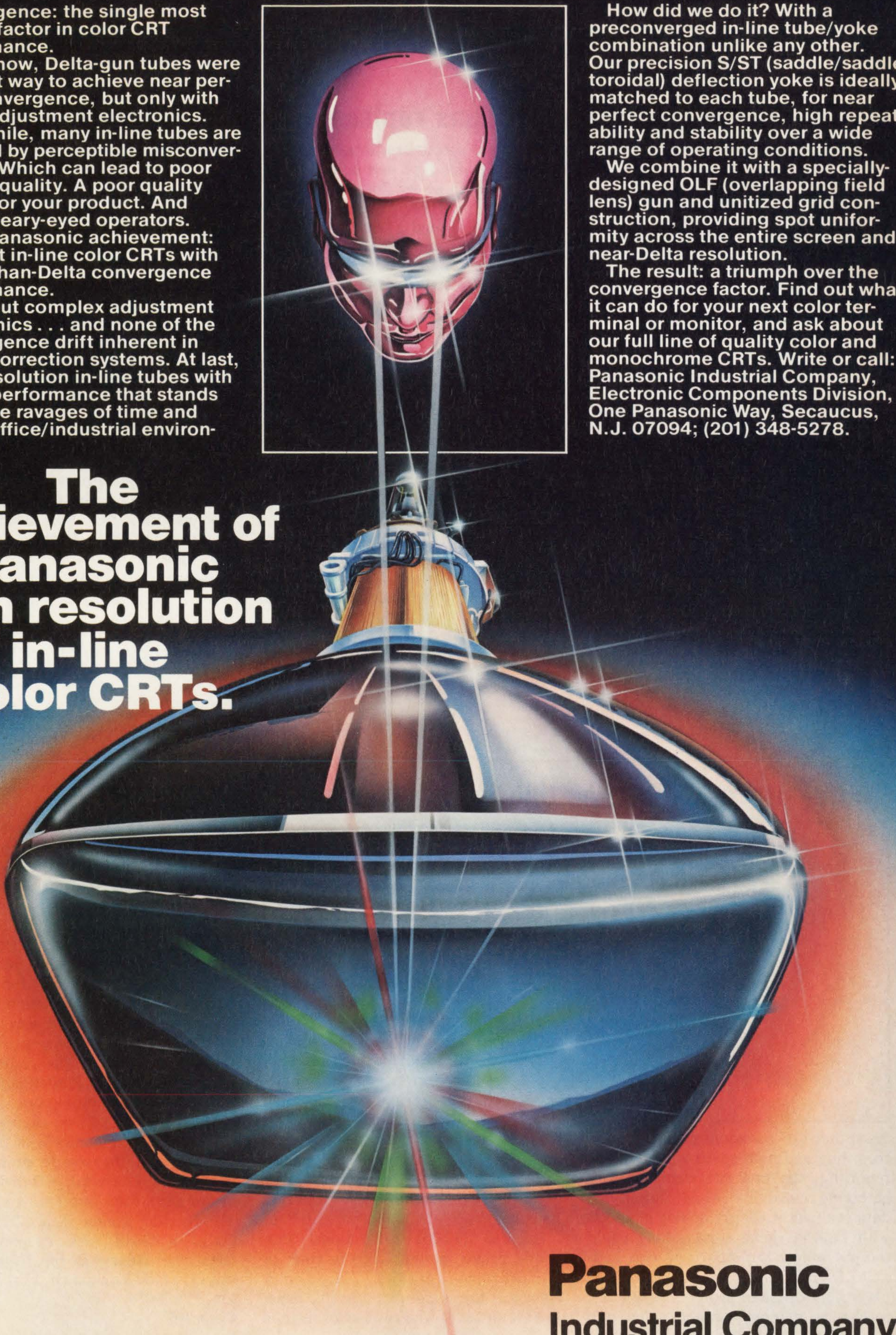
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.



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We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

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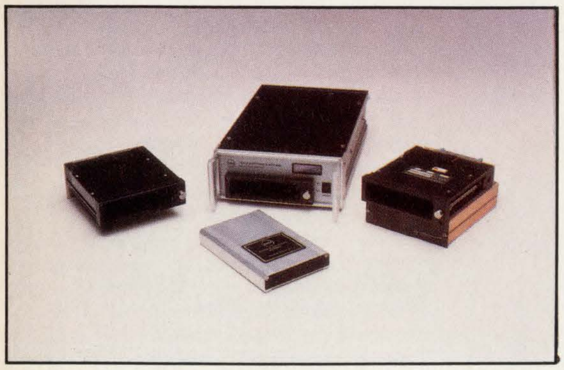
CIRCLE 106

Rugged bubble memory cartridges replace built-in disk/tape drives



Targeted for harsh, remote, and portable applications, a family of solid-state memory cartridges comes in 128K- and 256K-byte capacities. Bubble memory data storage systems greatly increase reliability over traditional moving magnetic-media recording systems, particularly in extreme conditions; typical bit-error rate of the new cartridges is 1 x 10^{-14} and MTBF, 180k h. Average access speeds are faster than those for tape and on a par with those for floppy disk drives.

Three versions revolve around a removable bubble memory cartridge whose standard size, shape, and interface can be used for program or data storage with other nonvolatile solid-state memory technologies. The CH2100 interface provides serial or parallel I/O for connection to an internal controller. Serial interface is RS-232-C or TTL compatible, with switch-selectable rates to 19.2k baud; parallel interface transfers data at 12.5k bytes/s. The unit comes as an aluminum cartridge holder with interlock latch, a separate circuit card with serial or parallel interface, and removable bubble memory data cartridge. Configurations to 1M byte, to be announced shortly, will be compatible with the present interface. Average access time is 48 ms, 96 ms max; standard op temp ranges are 0 to 55 °C and 10 to 40 °C; −20 to 60 °C range is optional.

Two versions besides the CH2100 are available. The DR3101 data recorder connects to the host via an RS-232-C or an IEEE 488 interface. Software emulates a DEC TU-58 cartridge tape recorder or an HP floppy disk drive. With the RS-232 interface, communication rates are switch selectable to 38.4k bps. Solidrive FDE525 is electronically compatible with 5¼″ and 8″ ANSI standard floppy drives and operates transparently to the host. DIP switch settings provide for change of standard format. Prices range from U.S. $2175 to $7437 each. **Targa Electronics Systems Inc**, PO Box 8485, 3101B Hawthorne Rd, Ottawa, Canada K1G 3H9.

Circle 267

Digital process recorder tightens instrument control

A synthesis of advanced analog process recording and high speed alphanumeric reporting, the DPR 1500 steps up data gathering capability while simplifying data evaluation. Thirty analog channels with built-in signal conditioning equip the instrument to monitor process variables from 17 sensor types. Digital displays show operator prompts in addition to channel number, variable value, and engineering units. High/low set points can be tied to an alarm for each channel. Flexible presentation format organizes sampled data on a universal chart in trend, tabular, or deviation report.

A single-chip microcomputer controls analog signal input processing; each input is conditioned, then applied to a dual-slope 15-bit A-D converter. Thermocouple, 100-Ω RTD, voltage, and current analog inputs are scanned every 5 s. The microcomputer linearizes RTD and thermocouple inputs and compensates for temperature variations in the thermocouple reference junction.

Integral 170-cps bidirectional dot-matrix printer outputs copy in color or monochrome (purple). Single-color approach forces pressure-sensitive paper against an anvil, whereas 6-color method employs an ink-filled color wheel. Dot-fill technique based on a microprocessor algorithm creates continuous lines; preselected chart speed or log interval determines printing frequency.

Reporting formats include trend, for continuous record; trend with deviation, for comparing processor inputs with reference input; tabular, for periodic records; and tabular deviation. Message option with trend format alerts operator to specified event or annotates the chart for quality control. The recorder configures for 4 ranges—extendable to 8—with remote switching option.

Print formats can be changed easily, since chart paper comes with preprinted grid lines only; the recorder prints the rest of the data. Universal, 100-division calibrated paper folds into 8½″ x 11″ sheets. The recorder comes in a 12.25″ x 19″ (31.12- x 48-cm) rack- or panel-mount metal case. **Honeywell Inc, Process Control Div**, 1100 Virginia Dr, Fort Washington, PA 19034.

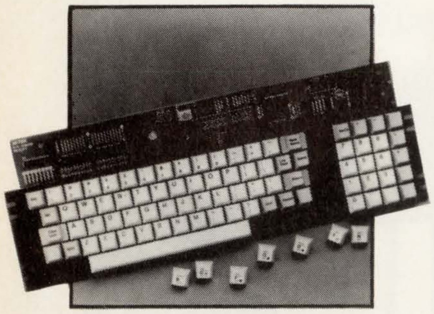
Circle 268

THE WINCHESTER BACKUP SYSTEM

Just plug it in your computer system. No additional hardware or software is needed. Transfer data to a 17.2 megabyte tape cartridge. Perform file search, update records, edit and reformat data. Use it for Winchester backup, data logging, or archival storage applications. Interfaces are built-in for RS-232, Multibus, S-100, 8-bit parallel, or Ohio Scientific. For full details on the Model 150 contact: **North Atlantic Qantex,** 60 Plant Avenue, Hauppauge, NY 11788 (516) 582-6060

CIRCLE 107

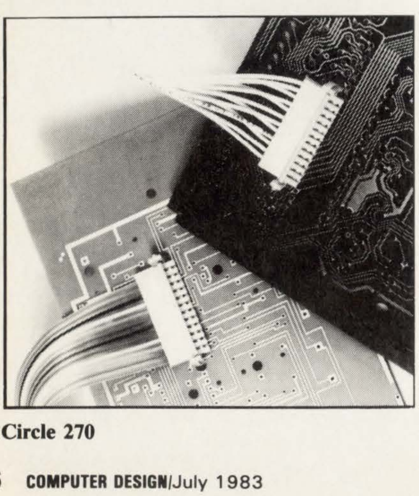
Low profile keyboard



Low-Profile series keyboards measure 18.4 mm, allowing designers an additional 11.3 mm to meet DIN computer terminal standards. The keyboards are available encoded or in simple matrix form. For encoded boards, 8048 microprocessors are used; for early prototype design, the 8748 EPROM version is used; and for large configurations, the 8049 with additional memory is used. Key switches are available with linear or tactile feel as well as with full N-key rollover. A nonencoded, 60-key array in 10k-piece quantity is less than $30. **Hi-Tek Corp,** 7274 Lampson Ave, Garden Grove, CA 92641. **Circle 269**

Surface mount connector

This surface mount midboard connector on 0.10″ (2.54-mm) centers is an addition to the family of Jaguar IDC connectors. The connector is designed to snap-lock onto the PC board and to provide polarized wire to board interconnection in any location on the board. It is available in 4 to 12 positions for use with 22 to 30 AWG wire. Contacts are tin-plated copper alloy, and the glass reinforced housing is UL-94VO rated material. Priced at less than $0.03 a position, the connector is rated at 3 A. **Methode Electronics, Inc, Interconnect Product Div,** 1700 Hicks Rd, Rolling Meadows, IL 60008.



Circle 270

Alphanumeric displays

Two series of 4-digit, solder-glass sealed LED displays are available. Both series have a true hermetic seal and operate in a temp range of −55 to 85 °C. The HDSP-245X is viewable from approx 10′ (3 m), and as a 5 x 7 LED matrix, displays an ASCII 128-char set with heights of 6.9 mm (0.27″), while the HDSP-231X is 5.0 mm (0.20″). For uniform front panel appearance, high efficiency red, standard red, and yellow are all categorized for luminous intensity. Devices are TTL compatible, end stackable, and have a viewing angle of 45°. The displays range in price from $85.50 to $115 in quantities of 10 to 99. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 271**

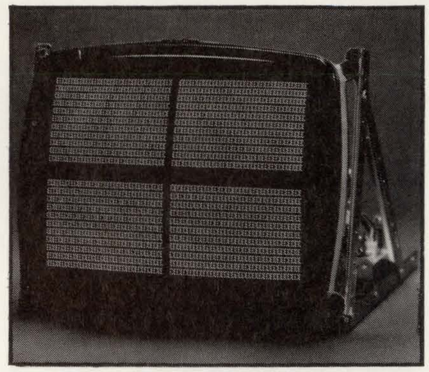
Small heat sink

The series 5932 heat sink has fins that alternately angle backward and forward; each fin is twisted at the ends. This results in greater air turbulence and more effective cooling. With a 5-W input, the heat sink has a 59 °C rise above ambient under natural convection. Used with plastic power semiconductor devices, the vertically mounted heat sink is equipped with tinned tabs for wave soldering to PC boards. Aluminum alloy devices are available in a black anodize or gold chromate finish. Series 5932B (black) heat sinks are priced at $0.29 each in 1000 quantities. **Aavid Engineering Inc,** 30 Cook Ct, Laconia, NH 03246. **Circle 272**

Low cost power MOSFET

With applications in amps and power supplies, wire and hammer drivers, motor controls, disk drives, and brushless motors, the ECONOFET BUZ71 MOSFET was designed to replace the 2N3055 bipolar transistor. The device has a 100 mΩ (typical) on-resistance due to a wide but short channel. The MOSFET blocks 50 V, handles continuous current up to 12 A, has no second breakdown, and switches faster with fewer circuit components. The device is available in a TO-220 package in N-channel configurations for $0.62.5 in quantities above 10,000. **Siemens Components, Inc, Colorado Components Div,** 800 Hoyt St, Broomfield, CO 80020. **Circle 273**

High contrast CRT display

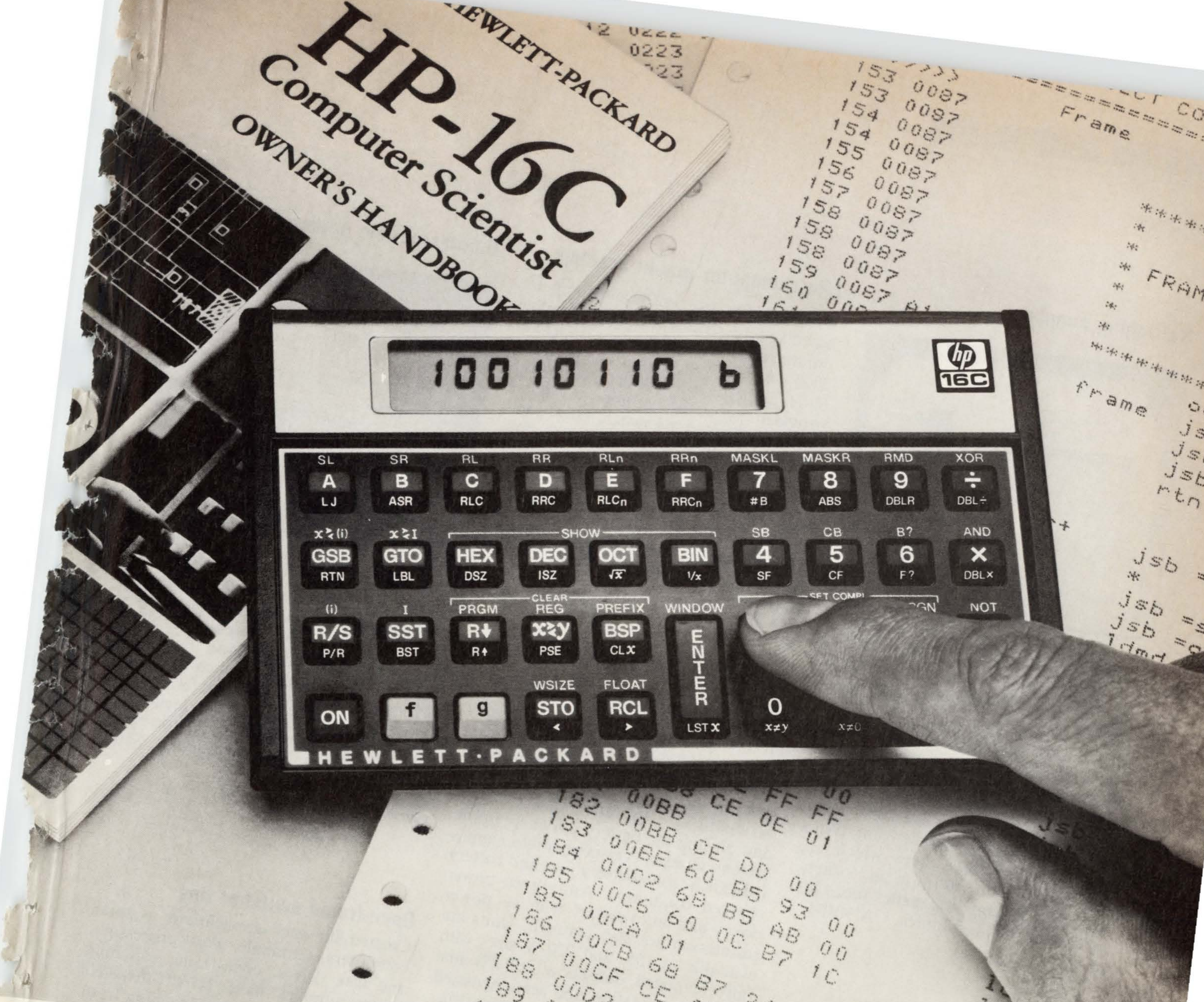


The Chromagold CRT display features an amber pigment with yellow emitting phosphors. This color configuration gives preference figures 4 times greater than other displays. Available across the full line of 5″ to 15″ diagonal displays, the CRT is suited for areas with high ambient light such as offices. Coating the inside of the faceplate surface with amber pigment allows improved contrast without sacrificing brightness. The device meets European ergonomic stds for computer operator comfort. **Zenith Radio Corp,** 1000 Milwaukee Ave, Glenview, IL 60025. **Circle 274**

DC motors for robotics

A line of permanent magnet dc motors are available for robotic applications. Small cube (¾″) and std (2, 3, and 4″ diameters) feature high torque to inertia ratios with low inductance. Used for precise movement control in the pincer, wrist, and other moving robotic joints, the motors provide rapid response at all operating speeds. Line also includes samarium cobalt motors, which provide higher peak-torque for applications involving greater loads. **Clifton Precision, Litton Systems Inc,** Marple at Broadway, Clifton Heights, PA 19018. **Circle 275**

Coming in August—
A Special Report on microsystems software.



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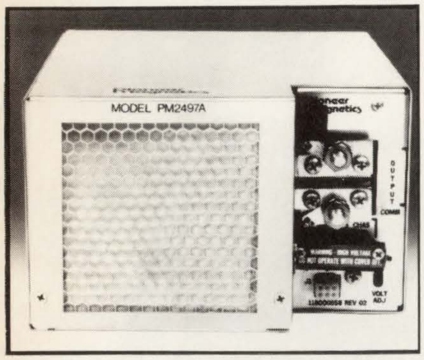
CIRCLE 108

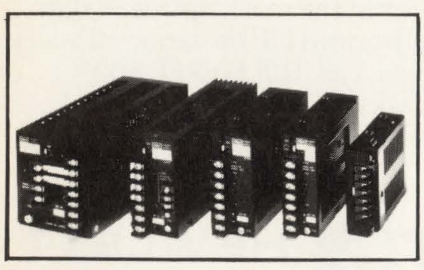
Switching supply



Model PM2497A type 3.3D150 offline switcher provides 3.3 V ±10% at 150 A. The 500-W supply has MTBF over 74k h and is protected against overloads, overvoltage, overtemp, and reverse voltage. Std features include remote sensing, ac input fuse, and brownout protection obtained from a 30-ms power loss holdup circuit. Supply regulation is ±100 mV for conditions such as ±20% input voltage change, static loads from 0% to 100%, dynamic load steps which are 25% of full load, and ripple and switching spikes. **Pioneer Magnetics Inc,** 1745 Berkeley St, Santa Monica, CA 90404.
Circle 276

High speed converters

Lightweight, single-output, DX series dc-dc converters are designed for high speed switching (50 or 100 KHz) whenever small power supplies are needed. Models in the 15- to 24-W, 30- to 48-W, 60- to 100-W, and 90- to 150-W classes have dc inputs of 12, 24, and 48 V. DC input of 110 V is used in 15-, 25-, 50-, 100-, and 150-W classes. With a 100-piece minimum, prices range from $0.45 for 15 W to $2.03 for 150 W. **KSC Electronics, Inc,** 543 W Algonquin Rd, Arlington Heights, IL 60005.



Circle 277

Microcomputer power systems

Designed for use with minicomputer based systems, the GPS-2K series of online uninterruptible power systems is rated at 2000 VA. System operates from a 120-Vac 60-Hz utility power line and has backup provided by sealed batteries. Available options include static switch, RS-232 communication interface, additional batteries, rack or standard enclosures, and various voltage and frequency options. Batteries are capable of sustaining full-rated load for 10 min. Prices start at $3950. **General Power Systems,** 1400 N Baxter St, Anaheim, CA 92806.
Circle 278

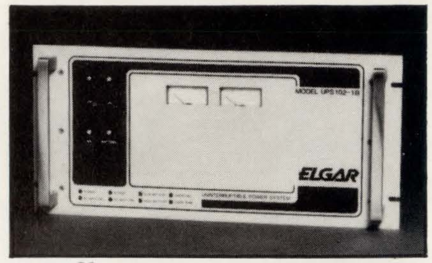
Power supply family

EHVQ switching power supply family offers optional battery backup to guarantee uninterrupted power. Implementation is achieved by plugging an additonal PC board into the EHVQ power supply and placing the battery anywhere in the system chassis. TTL-compatible signals indicate ac low, battery low, and battery charged conditions. Auto-timed power down and auto-restart with ac power restoration are also featured. Units are available in 155- and 220-W sizes with fully regulated outputs at ±0.2% line and load regulation and semi-regulated outputs at ±5% load regulation. **Tii Electronics,** 226 Terminal Rd, E Setauket, NY 11733.
Circle 279

Mini power converters

The PKA series of dc/dc converters for primary voltages of 24 and −48 Vdc are targeted for industrial and telecommunication use. Eight models within the 25- to 40-W power range are available for digital (5-V) and analog (12-V) electronic circuitries, with switching frequencies of 300 kHz. Converters weigh 3.53 oz (100 g) and measure 3" x 3" x 0.68" (76 x 76 x 17 mm). With an MTBF of more than 200 years at 113 °F (45 °C) and an op temp of −45 to 85 °C, the devices have applications in servomechanisms, telephone and radio communications, and industrial process control. **Rifa Inc,** Greenwich Office Park 3, Greenwich, CT 06830.
Circle 280

Uninterruptible power systems



Elgar B series uninterruptible power systems (UPS) are available in 1-, 3-, 5-, 10-, 15-, and 25-kVA single-phase, and 25-, 37.5- and 50-kVA 3-phase models. The 1-, 3-, and 5-kVA units feature a pulse width modulated static inverter and a std electromechanical bypass switch. Smaller models include an inverter sync frequency window of ±60 Hz, slew rate of 1 Hz/s, and auto forward transfer to bypass switch after an overload-induced reverse transfer. Units have full diagnostic and annunciation package and operate from a 72-Vdc battery. **Elgar Corp,** 8225 Mercury Ct, San Diego, CA 92111.
Circle 281

Open-frame switcher line

Created for such applications as small computers, terminals, word processors, and disk drives, open-frame switching power supplies have 11 off-the-shelf models in 5 package sizes, ranging from 40 to 250 W. Designed to meet VDE, UL, IEC, CSA, and other stds, the units also meet emission limits of FCC Docket 20780 Class A and VDE 0871/6.78 Class A. International series ac input ranges include as std 90 and 132 V for domestic and Asian applications, and 180 to 264 V for European applications. **Power-One Inc,** Power-One Dr, Camarillo, CA 93010.
Circle 282

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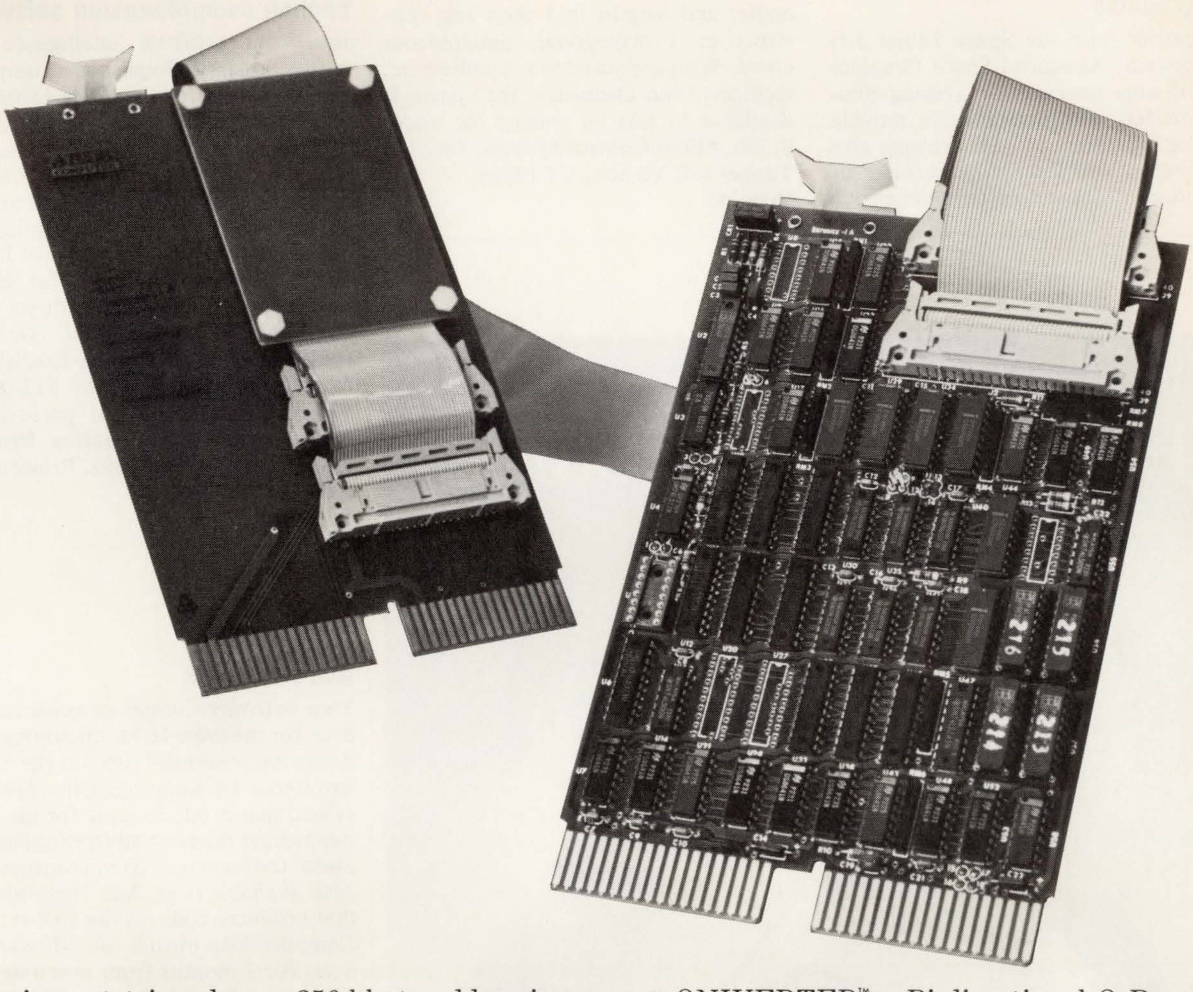
PDP-11/23 with 4 Megabytes of Q-BUS Memory. Impossible? Read On.



If you've outstripped your 256 kbyte addressing capability, if you want a reliable solution to your memory expansion needs, and if budget is a concern, we have the answer. We have made life on the Q-Bus a lot easier. QNIMAP,™ another outstanding Q-Bus product from Able Computer, allows for full memory expansion up to 4 megabytes of main memory and the use of existing Q-Bus DMA devices. With QNIMAP,™ you get system performance you never thought possible along with complete support from Able. The QNIMAP™ consists of two easy to install dual width boards and is software compatible with RSTS/E, RSX-11 and UNIX.

If you have other Q-Bus needs, Able has many exciting products:

- ABLE Q/DH™ – Direct memory access communications controller – gives you DH11 performance on your PDP-11/23 Q-Bus system.
- QNIVERTER™ – Bi-directional Q-Bus to Unibus/Unibus to Q-Bus signal converter for memory and peripheral devices.
- UNIMAP™ – Memory expansion to 4 megabytes on the PDP-11/23. Allows use of 18 bit Unibus devices.
- INTERLINK™ – DMA interprocessor link between two Unibus, two Q-Bus, or one Q-Bus and one Unibus system.

Find out more about QNIMAP™ and the rest of of our Q-Bus products. Write or call for details. Able Computer, 1732 Reynolds Avenue, Irvine, California 92714. National offices: Irvine CA (714) 979-7030, Burlington MA (617) 272-1330, Rumson NJ (201) 842-2009. International offices: Canada (Toronto) (416) 270-8086, England (Newbury) (0635) 32125, W. Germany (Munich) (089) 463080. For immediate, toll-free information, dial (800) 332-ABLE.

ABLE COMPUTER

Q-Bus, Unibus, RSTS/E, RSX/11 and PDP are trademarks of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories.

CIRCLE 109

3-D graphics

Compatible with the Space Tablet 3-D CAD system, Advanced Space Graphics is a software package for creating complex models. Features include moving and editing points in 3-D, drawing arcs and circles, and generating surfaces of revolution. Software can auto-dimension angles and lengths in 5 ways and construct in 3 orthogonal, simultaneous views. With applications in architecture, medicine, and chemistry, the system is available to IBM PC owners for under $1700. **Micro Control Systems, Inc,** 143 Tunnel Rd, Vernon, CT 06066.

Circle 283

English comprehension software

Based on artificial intelligence techniques, RAMIS® II English is a component for the RAMIS II DBMS. The component processes English requests and responds to questions. The knowledge base consists a general dictionary of the English language, a file dictionary, and optional file specific dictionaries for applications. With the processor, data do not have to be copied or restructured for English processing because there is direct access to sequential, VSAM, and ISAM files stored in data bases. The English processor is available from $12,000 to $24,000 based on CPU performance rating levels. **Mathematica Products Group, Inc,** PO Box 2392, Princeton NJ 08540.

Circle 284

Ada compilers

Two software compilers generate Ada code for the Z8000 16-bit microprocessor. Zilog/ICSC compiler runs on the System 8000 under an enhanced Unix operating system that produces code for the Z8001® (segmented memory addressing) and the Z8002® (nonsegmented) microprocessors. Also available is an Ada cross-compiler that produces code on the VAX-11 series. Compiler lists include all software updates for 3 months from purchase date. Zilog compiler is priced at $8000/copy. **Zilog, Inc,** 1315 Dell Ave, Campbell, CA 95008.

Circle 285

Xenix operating system

Developed for the iAPX 286 line of microprocessors and board-level products, the Xenix 286 operating system is a multitasking multi-user system for high performance OEM applications. The combination of the 80286 and Xenix provides improved performance, multi-user access, record- and file-locking, and power-fail disk recovery. Operating system also includes driver support for 5 controller boards ranging from terminal communications to tape support. Xenix for the 80286 and the 286/10 is priced at $3000 with OEM volume discounts; licensing and support arrangements are available. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 286

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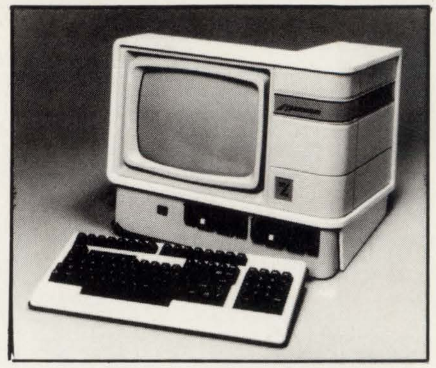
GATES ENERGY

CIRCLE 111

Expandable CPU

The DBC68K2 is an MC68000 based single-board computer that features dual-bus architecture, 128K bytes of memory, iSBX multimodule interface, and operating systems that include Xenix. Standard is a PROM capacity of 128K bytes and interrupt circuitry; optional is SBX connection for use with Multimodule I/O, 128K-byte RAM module, and a segment- or page-oriented MMU. Applications range from process control at the low end to simulation at the high end. Prices are $1995 for 10 MHz and $2195 for 12 MHz with OEM discounts available. **Microbar Systems Inc**, 1120 San Antonio Rd, Palo Alto, CA 94303.
Circle 287

Desktop microcomputer



A M68000/Unix based workstation, the alphanumeric 32/4, features DMA, 0.5M bytes of 150-ns main memory, and a proprietary MMU. Standard equipment includes display controller board, 12" green phosphor screen, keyboard, and two 5M-byte Winchesters. System provides 4 serial ports, SASI interface port, multi-user Unix operating system, C, word processing, and spread-sheet software. The 32-bit desktop microcomputer sells for $4495 in large OEM quantities. **Momentum Computer Systems International,** 965 W Maude Ave, Sunnyvale, CA 94086.
Circle 288

Multi-user microprocessor

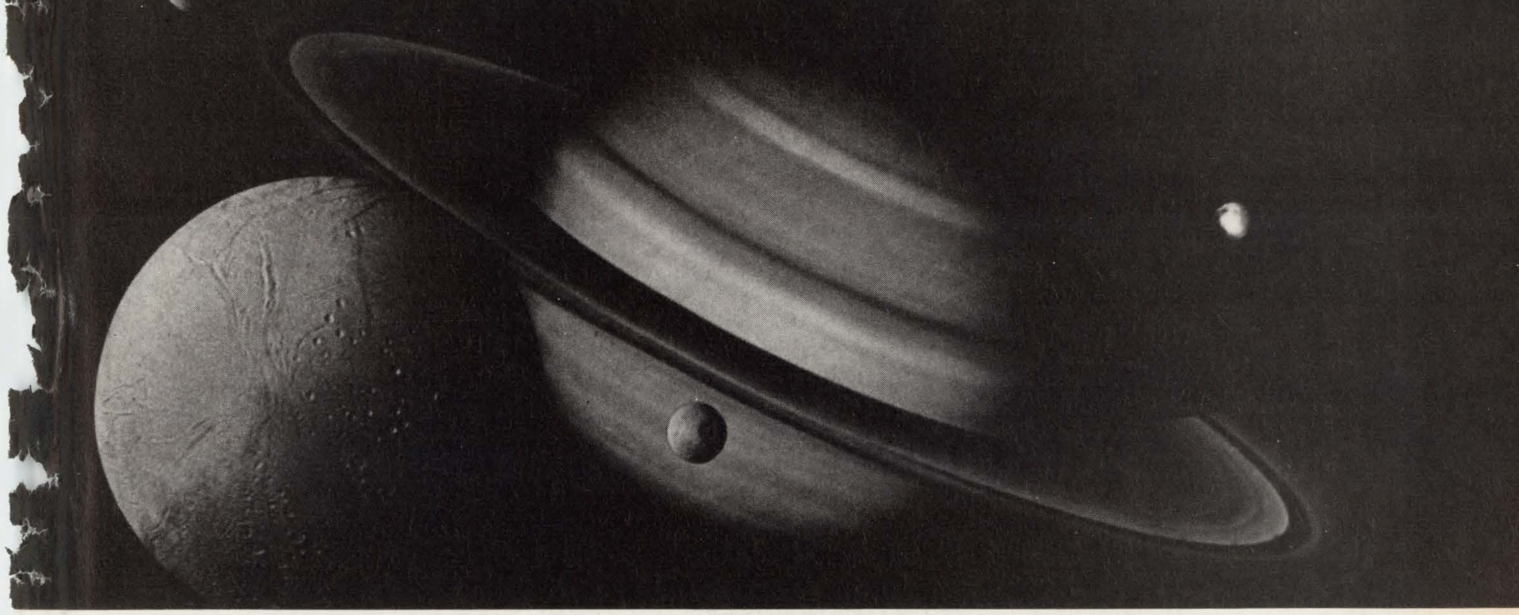
Incorporating a 16-bit 8086 microprocessor and a Xenix operating system, the NABU 1600 offers a low cost multiuser multitasking system. Featuring 256K or 512K bytes of RAM, 8K ROM, 4 I/O ports and a disk drive controller, the microcomputer allows 3 users to access the system at once. Available software includes program development tools, high level languages, and applications programming such as word processing and database management. **NABU Manufacturing Corp**, 1051 Baxter Rd, Ottawa, Ontario K2C 3P2.
Circle 289

32-bit microcomputer

Based on the NS16032 CPU chip, the MegaMicro 16032 is a 32-bit, virtual memory microcomputer. The system provides demand-paged address and data space of 16M bits, supports 16 hard disk drives for a memory access of 1600M bytes, and can perform 161,000 floating point multiplications/s. System operates on the Multibus std (IEEE 796). Price for the system starts at $15,000 with a board version available for $4000. **The Logical Microcomputer Co**, 140 S Dearborn St, Chicago, IL 60603.
Circle 290

 CIRCLE 112

EXPAND YOUR MULTIBUS SYSTEM'S OUTER LIMITS.



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The new Xylogics 450 peripheral controller provides even more performance for Multibus disk control applications. The 450 can address up to 16MB of memory and control up to four SMD disk drives at data rates of up to 1.8 MB/sec. non-interleaved.

The new Xylogics 472 is a high performance, single-board tape controller for streaming and start-stop tape drives. It can address up to 16MB of memory and control up to four tape drives – running at speeds from 12.5 ips to 125 ips and at densities of 800 bpi NRZI, 1600 bpi PE, 3200 bpi, or 6250 bpi GCR.

The 440, 450 and 472 feature advanced channel control techniques and are designed to work together for system optimization. For Multibus users, this means low bus usage, non-interleaved disk operation and true high-speed streaming with no repositioning. All three work with any 16, 20 or 24 bit address Multibus system.

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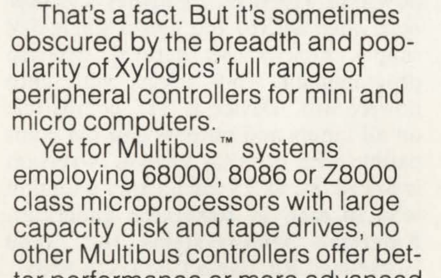
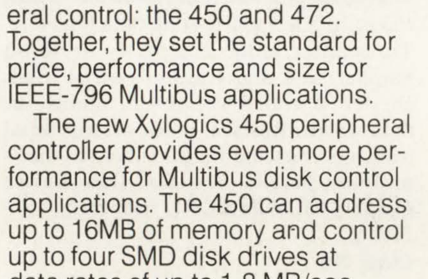
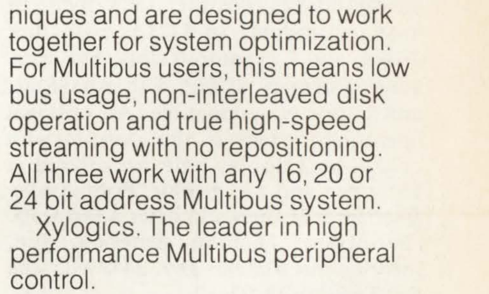


Xylogics 450 Multibus Disk Peripheral Controller.



Xylogics 472 Multibus Tape Peripheral Controller.



Xylogics 440 Multibus Disk Peripheral Controller.

Comm controller

A programmable single-chip peripheral, the F16456PR multiple protocol communications controller, interfaces with 16000, 8080, and 8086 based systems. Controller offers both sync and async communications on 1 chip with bit-oriented protocol, byte control protocol, SDLC, ADCCP, and IBM Bisync. Device operates in full or half duplex, and in normal or transparent modes. Available in 40-pin DIP or cerDIP, controller is priced at $59.50 in quantities of 100. **Fairchild Camera and Instrument Corp, Microprocessor Div,** 450 National Ave, Mountain View, CA 94042.
Circle 291

8-bit micro

With applications in remote control, motor control, and tuning, the PIC16C58 is a programmable 8-bit microcomputer. Features include 32 8-bit RAM registers, 512 x 8-bit program ROM, 2-level stack for subroutine nesting, and a realtime clock/counter with mask programmable rescaler. Device has 4 input, 8 output, and 8 bidirectional I/O lines, with low power standby mode (5 μA) and 3.2 to 6.0 V in a power supply operating range. Microcomputer is priced at under $2.30 in 50k quantities. **General Instrument, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.
Circle 294

PCM line filter chip

Pin compatible with industry std 2912 and 2912A, TCM2912B line card component is used with codec ICs in telecommunication applications. The chip reduces jitter and eliminates the need for an external capacitor by using a 2-pole active lowpass smoothing filter. This eliminates the 256-kHz clock frequency generated at the output of the switched capacitor filter. Made with NMOS technology, the circuit dissipates 60 mW in normal operation and under 1 mW in standby. **Texas Instruments Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.
Circle 297

16-bit microcomputer

The T300 personal/business computer system includes monochrome or color display, detachable keyboard, and system unit. The system unit consists of an 8088 microprocessor, 192K bytes of RAM (expandable to 512K), 640K disk drives, and 7 expansion slots. Std operating system is MS-DOS with T-BASIC-16; unit is IBM PC compatible. An optional operating system is the CP/M-86 with CBASIC-86; 2 display units are offered, a 12" green and 14" 8 color. Both display 80 chars x 25 lines and offer a 650 x 500 resolution. **Toshiba America, Inc, Information Systems Div,** 2441 Michelle Dr, Tustin, CA 92680.
Circle 292

Multi-user microcomputer system

Super Slave processor provides a dedicated CPU for every user without limiting system size. This is done by sharing data with the host only when accessing drives or other common peripherals. Processor board includes a Z80A CPU, 4 serial and 2 parallel I/O ports, 2K to 4K of EPROM, and 64K to 128K of bank-switched RAM. Each board is linked through the S-100 bus to the master board, forming a network that uses the Turbo-Dos operating system. Boards are available with full documentation and warranty for $650; OEM discounts are available. **Advanced Digital Corp,** 12700 B Knott Ave, Garden Grove, CA 92641.
Circle 293

INTEGRATED CIRCUITS

56-pin terminal bit processor

BUS-64100 complies with MIL-STD-1553A/B and MacAir specifications A-5690, A-3818, A-4095, and A-5232. The hybrid processor interfaces a serial MUX data bus transceiver to a parallel 3-state data highway. Transmitter mode accepts 8- or 16-bit parallel data and transmits serial Manchester II coded command, status, or data words. Receiver mode accepts serial transmissions and outputs them to the 8- or 16-bit parallel bus. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.
Circle 295

High speed A-D converters

Three video speed A-D converters are available. TDC1014 is a 6-bit converter with ±0.4% linearity and a conversion time of 25M samples/s. TTL compatible, the device has a power dissipation of 1 W and digitizes a 1-V peak to peak signal. TDC1029 has 6-bit performance at 100M samples/s and provides a full-scale analog input bandwidth of 50 MHz. TDC1027 offers 7 bits at 18M samples/s with ±0.4% linearity and aperture jitter of 50 ps. This device consists of 127 clocked latching comparators, combining logic, and an output buffer register. Converters are priced at $46 in quantities of 1000. **LSI Products Div, TRW Electronic Components Group,** PO Box 2472, La Jolla, CA 92038.
Circle 296

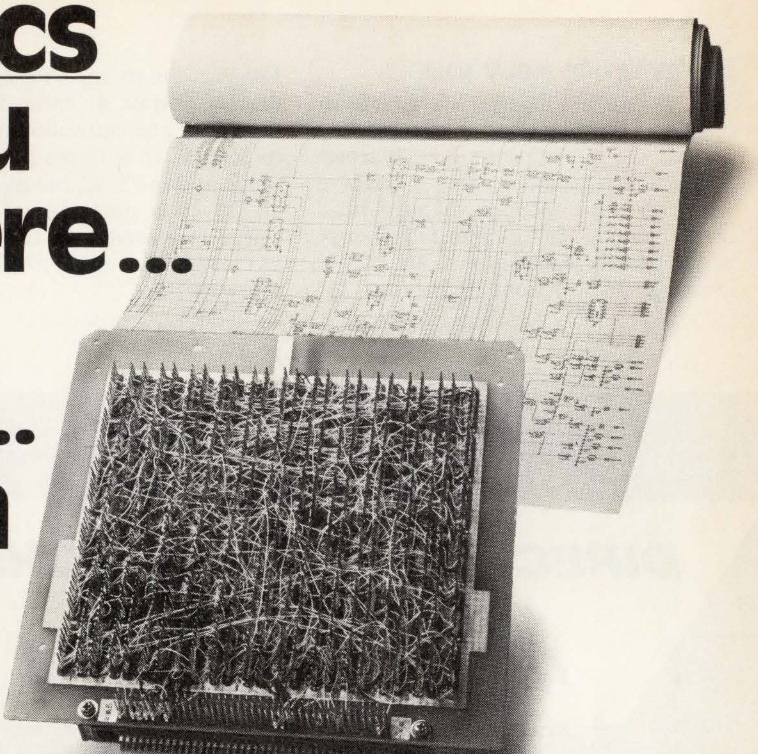
Low power 128K ROM

Organized as 16K words x 8 bits, the 2 NMOS ROM versions (S23128 A and B) feature access times of 350 and 250 ns, respectively. Chip maintains a standby power of 110 mW, dissipates 220 mW max when active, and uses a single 5-V supply. ROM is user defined, offering programmable chip selects with auto powerdown. Device is TTL compatible on all inputs and outputs and pin compatible with 27128 UV EPROM. A-version is priced at $8.75 each; the B-version is $9.50 each in 1000-piece quantities. **American Microsystems Inc,** 3800 Homestead Rd, Santa Clara, CA 95051.
Circle 298

Nonvolatile RAM

Operating from a single 5-V supply, NCR 52212 nonvolatile RAM is a 256-word x 4-bit array with EEPROM for backup. Typ access time is 200 ns, with max at 300 ns (commercial) and 450 ns (military). Chip is suited for applications where critical data are continually modified, and where data are to be retained during power interruption. Fabricated with an N-channel silicon-nitride-oxide-silicon process, RAM has at least 10^4 store cycles with 1-year data retention. Other features are auto power-up recall, memory margining, and TTL compatibility. In 100-piece quantities, price is $7.30. **NCR Corp, Microelectronics Div,** 8181 Byers Rd, Miamisburg, OH 45342.
Circle 299

Who'd believe that Wire Graphics can take you from here...



to here... in less than 2 days?

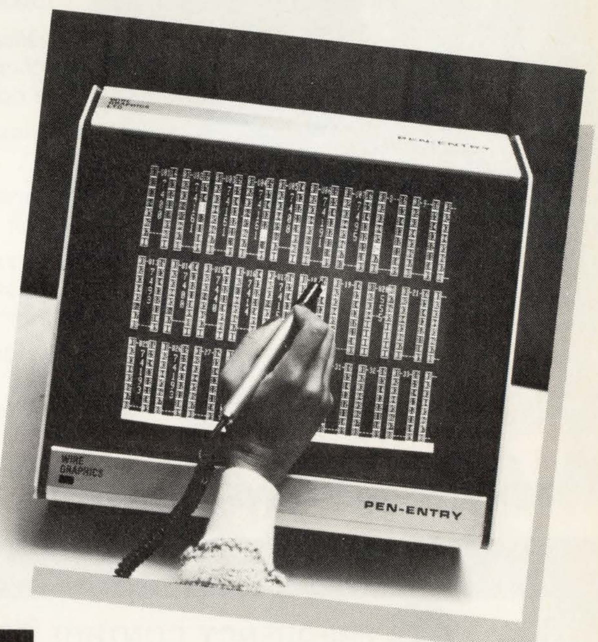
Eastman Kodak did. Eaton's AIL Division did. Hazeltine did. Harris PRD did. And dozens more do.

THE "UNBELIEVABLE" SYSTEM

PEN-ENTRY 4000/8000* is a unique approach to N/C tape preparation. Utilizing interactive graphics and a light pen, wiring connections can be programmed for such processes as Wire-Wrap*, Multiwire*, Stitchwire*, Quick/Connect*, etc. Using the light pen the operator can wire and layout components on the CRT display working directly from schematic, eliminating the need for "from-to" lists. PEN-ENTRY is loaded with features that save valuable time in trouble-shooting and testing. PEN-ENTRY's floppy disk data storage allows ready revision of previously stored data; this means E.C.O.'s can be processed faster and more efficiently. An in-house system offers numerous advantages in cost and time savings in prototyping and production.

PEN-ENTRY also has application in the automated manufacture of P.C. Board Test Head Fixtures for ATE.

The "unbelievable" price: $25,990 for a complete system.



THE "UNBELIEVABLE" SERVICE

The Wire Graphics' Customer Service Center (CSC) provides engineering support utilizing PEN-ENTRY CAD to help you through the headache of data preparation. In less than 2 days the CSC can detect errors in your schematic and furnish an N/C tape for your wire termination equipment, or provide total job service, including MIL spec, Wire-Wrap* or Stitchwire*.

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Wire Graphics, 215 B Central Ave., Farmingdale, NY 11735.

Wire Graphics

*Pen-Entry 4000 8000 Trademark of Wire Graphics
Wire-Wrap Trademark of Gardner-Denver, Cooper Electronics
Multiwire Trademark of Kollmorgen Corp.
Stitchwire Trademark of Interconnection Technology, Inc.
Quick Connect Trademark of Robinson Nugent, Inc.

CIRCLE 114

Energy-saving motor chip

The HV-1000 motor chip is capable of complex computations while running directly off the ac power line. It senses the load on a motor and controls a TRIAC to use a reduced voltage with a lightly loaded motor and full voltage with a heavily loaded motor. The chip is available in 2 versions: the HV-1000 for 120 Vac, the HV-1000A for 240 Vac. Both devices operate at either 50- or 60-Hz frequency and can withstand line surges to 3500 V. In a 16-pin DIP with a temp range of 0 to 75 °C, the HV-1000 is priced at $13.75 in quantities of 100. **Harris Corp, Semiconductor Group**, PO Box 883, Melbourne, FL 32901.
Circle 300

Monolithic 16-bit DAC

Designed for digital audio applications, PCM52JG-V and PCM53JG-V 16-bit DACs include low noise zener voltage reference, fast settling current switches, and a low noise output op amp. THD is 0.002% (FS input, 16 bits) typ; 0.02% THD typ for −20 dB, 16 bits; differential linearity error is 0.001% FSR at critical bipolar zero point. Compatible with systems that use high sampling frequencies and digital filters, DAC has a dynamic range of 96 dB and a typ settling time of 5 μs. Applicable to industrial measuring equipment, recording and playback studio equipment, and sonar, the devices are priced at $23 in 100s. **Burr-Brown**, Box 11400, Tucson, AZ 85734.
Circle 301

Intelligent display controller

As a single-chip bar graph and numeric display controller, the 10951 can drive a 16-segment bar graph, a 7-segment display with 16 positions, or 50-V vacuum fluorescent displays. Onchip functions include RAM buffer, PLA segment decoder, output drivers, and control logic. The device adjusts brightness and refresh rate while being controlled by a host computer through serial interfacing. Applications of the 40-pin DIP include interactive terminals, automation, and instrumentation. In volume quantities, the device is priced at $5.25. **Rockwell International, Electronic Devices Div**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 302

Macrocell array

The MCA2800ALS TTL-compatible array is composed of 130 internal (major) cells that can be personalized via computer as OR/NOR gates (4/cell) or more complex functions (2/cell) with 600-ps propagation delays. Additionally, 120 I/O cells can be personalized as offchip drivers, receivers, or bidirectional cells. Using ECL internal circuits and TTL I/O levels, the array features over 70 defined macro functions, LSSD diagnostic macro, and a 32 x 9 super macro. Packaged in a 149-pin grid array ceramic package, the unit is approx $160/part in 500-unit quantities. **Motorola Semiconductor Products Inc**, PO Box 20912 Phoenix, AZ 85036.
Circle 303

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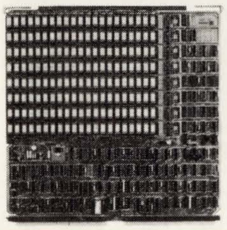
Dataram has been delivering Data General-compatible memory since 1974, today offering the industry's most extensive range of such products — from ADD-IN memory to BULK MEMORY disc emulation systems.



AND STILL GROWING. We've just introduced a versatile, highly reliable 1.0 MB ADD-IN for Data General's NOVA 4 and ECLIPSE S/140 minicomputers, which puts it at the head of an already impressive class of ADD-INs:

DATARAM ADD-IN	MAXIMUM CAPACITY	DATA GENERAL MINI
DR-240 (semi)	1.0 MB	NOVA 4; ECLIPSE S/140
DR-225 (semi)	1.0 MB	ECLIPSE S/130 AND OTHERS
DR-123S (semi)	256 KB	NOVA 3
DR-123 (core)	32 KB	NOVA 3
DR-124 (core)	32 KB	NOVA 2
DR-1200 (core)	32 KB	NOVA 1200

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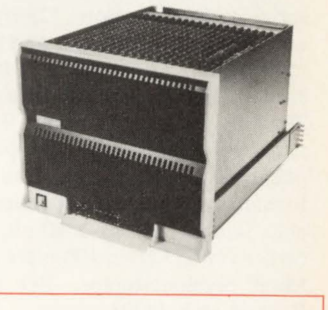
MORE THAN COMPATIBLE. Many of Dataram's products incorporate enhancements not available from comparable Data General products. For example, our 1.0 MB NOVA 4 compatible ADD-IN provides an extra ECC bit (giving you 6 ECC, rather than Data General's 5 ECC bits), transparent to the host mini, which allows full double-bit error detection.



AND FOR LESS COST THAN YOU'D EXPECT for highly reliable, proven memory products.

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DATARAM BULK MEMORY	EMULATION	MAXIMUM CAPACITY
BS-303 (semi)	6063/6065 (AOS compatible)	8.0 MB
BC-303 (core)	6063/6065	2.0 MB
BS-301 (semi)	NOVADISC	4.0 MB
BC-301 (core)	NOVADISC	2.0 MB

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DATARAM

Dataram Corporation □ Princeton Road □ Cranbury, New Jersey 08512 □ (609) 799-0071 □ TWX: 510-685-2542

CIRCLE 116

Fast CMOS converter

TML1073 7-bit flash ADC operates at a sampling rate of 10 MHz and draws 150 mW of power. Operating current is programmable. Max linearity error is ±1 LSB, and max quantizing error, ±0.5 LSB. Required reference levels are ±3.2 V. Conversion is accomplished with one pulse from the external clock. Open drain outputs allow interface to TTL, CMOS, or ECL circuits. **Telmos, Inc**, 740 Kifer Rd, Sunnyvale, CA 94086.
Circle 304

CMOS ROM

The MB83256 is a 256K-bit CMOS static ROM. The device, organized as 32,768 8-bit words, offers double the memory density of a 128K ROM in a JEDEC-compatible 28-pin DIP, with a 250-ns access time. Features of the device include CMOS technology, to reduce active power dissipation to less than 83 mW; TTL compatibility; single 5-V supply; and fully static operation. Chip is suited for applications where large memory capacity and high speed/low power operation is required. **Fujitsu Microelectronics, Inc**, 57 Wells Ave, Newton, MA 02159.
Circle 305

Data switch IC

A high speed data switch circuit, the MD68SC84A offers chip-to-chip micronetworking. Chip functions include serial communication, 128-byte storage and distribution control, and bus or time multiplexing. Four serial I/O highways contain 32 channels and transfer data at 2M bps. Serial outputs are 3 state with software or hardware control. With applications in interfacing, data switching, formatting, and timing generation, the chip is available in a 40-pin plastic or cerDIP for $57.50 in 100-piece quantities. **Mitel Semiconductor**, PO Box 1663, Buffalo, NY 14203.
Circle 306

High speed, high density EPROM

Am27128, a 128K-byte UV EPROM, features access times of 150 ns over commercial temperature range and 200 ns over the military range. Organized as 16,384 x 8, the EPROM requires a 5-V power supply, has TTL compatible inputs and outputs, and uses only 525 mW of power in the active state and 130 mW in standby. To reduce programming time, device can be programmed with 1-ms pulses, allowing a typical programming time of 3 min. For 28-pin cerDIP, the price is $88.40 in 100-piece quantities. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 307

32-bit floating point chip

Available for use in high speed floating point processors, the WTL1032 (multiplier) and the WTL1033 (ALU) feature 5M-flop performance, offer all floating point functions, and can operate in either pipeline or flow-through modes. Pipeline mode has throughput latency of 900 ns, while flow-through mode offers a 600-ns latency, reducing 1-time operation delay. The 32-bit chip consumes less than 2 W and is compatible with IEEE 754 in rounding modes, infinity representation, and overflow. The circuits are individually priced at $325 or $650/set in quantities of 100. **Weitek Corp**, 3255 Scott Blvd, Santa Clara, CA 95050.
Circle 308

200-ns access time ROM

The 23256A MOS ROM offers 32K bytes of storage and conforms to JEDEC-B standards for byte-wide memories. With a 200-ns access time and a 5-V supply, the device has an active current of 100 mA and is TTL compatible. Chip features a 2000-V electrostatic discharge protection circuit on all inputs and outputs. It is available in 28-pin ceramic or plastic packages, which are priced at $25.00 in 1000-piece quantities. **Signetics**, 811 E Arques Ave, Sunnyvale, CA 94086.
Circle 309

Memory interface chips

The CDP1881/1882 series of CMOS 6-bit latch and decoder chips operate directly on the multiplexed address bus of the compatible CDP1800 microprocessor. Chips, designed for operation with both 2K- and 4K-byte memories, operate over a voltage range of 4 to 10.5 Vdc. The 1881 contains memory R/W input lines to enable chip select outputs. In 20-pin package, the 1881 (5-V plastic) is priced at $2.30 while the 1882 is $1.64 in an 18-pin, 5-V plastic. **RCA Solid State Div**, Box 3200, Somerville, NJ 08876.
Circle 310

Fast DRAM

Organized as 16K x 4, the IMS2620 dynamic RAM allows implementation of high-memory bandwidth applications. Offering worst-case access times of 100, 120, and 150 ns with worst-case cycle times of 160, 190, and 230 ns, respectively, the DRAM also features CAS-before-RAS refresh-assist, which requires less support circuitry. Packaged in an 18-pin plastic DIP, the 100-piece pricing is $13.20 for 100 ns, $10.40 for 120 ns, and $8.70 for 150 ns. **INMOS**, PO Box 16000, Colorado Springs, CO 80935.
Circle 311

Cascadable FIFO

Organized as 64 x 4 and 64 x 5, models C/67401B and C/67402B are cascadable FIFOs with 16.7-MHz shift-in/-out rates. Applications include data rate matching between digital video systems and their peripherals, data acquisition, and telecommunications. FIFO provides structured pinouts, TTL inputs and outputs, and async operation. In quantities of 100 to 999, the 64 x 4, 16-pin DIP is $35.43; the 64 x 5, 18-pin DIP is $43.46. **Monolithic Memories, Inc**, 1165 E Arques Ave, Sunnyvale, CA 94086.
Circle 312

ECL static RAM

The F100480 is a 2K-byte RAM that features 25-ns max commercial address access time and is organized in a 16,384 x 1 format. Fabricated with an oxide isolation and fine line photolithography process, the RAM is 10K and 100K ECL compatible. With typ supply currents of 160 mA the device is packaged in a 300 mil 20-pin cerDIP or a 20-pin flatpak. Production of the F100480 is scheduled for Sept. **Fairchild Camera and Instrument Corp, Advanced Bipolar Div**, 441 Whisman Rd, M/S 23-1250, Mountain View, CA 94039.
Circle 313

64K hybrid CMOS static RAM

Featuring true output enable, the 64-02 combines 4 Hitachi HM6116s and a decoder chip in an 8K x 8 CMOS RAM. Packed in a std 28-pin cerDIP, the hybrid is pin for pin compatible with the std 64K-bit EPROM, as well as with 64K-bit CMOS RAM monolithics. It operates from a 5-V supply at 250 mW typ and provides 100-ns memory access time. **Integrated Circuits Inc**, 13256 Northrup Way, Bellevue, WA 98005.
Circle 314

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Preston Scientific's building block approach provides fast and accurate ADC and DAC Instrumentation Systems. They feature 15-bit resolution with conversion rates from 40kHz to 1MHz – that means multiplexed A/D conversion at one million samples per second.

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Preston's GM Series Systems are used extensively in high quality testing and research applications for a broad spectrum of industries ranging from aerospace to automotive. And, Preston ADC-DAC Systems interface to most computer systems such as DEC, HP, Gould/SEL, Perkin-Elmer, as well as array processors from Floating Point Systems, CSPI and Analogic.

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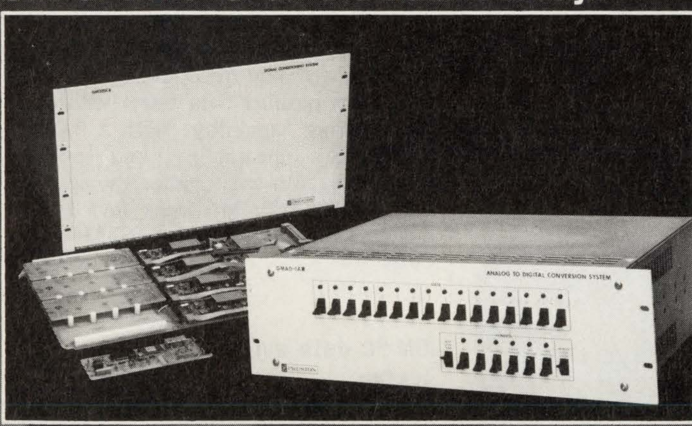

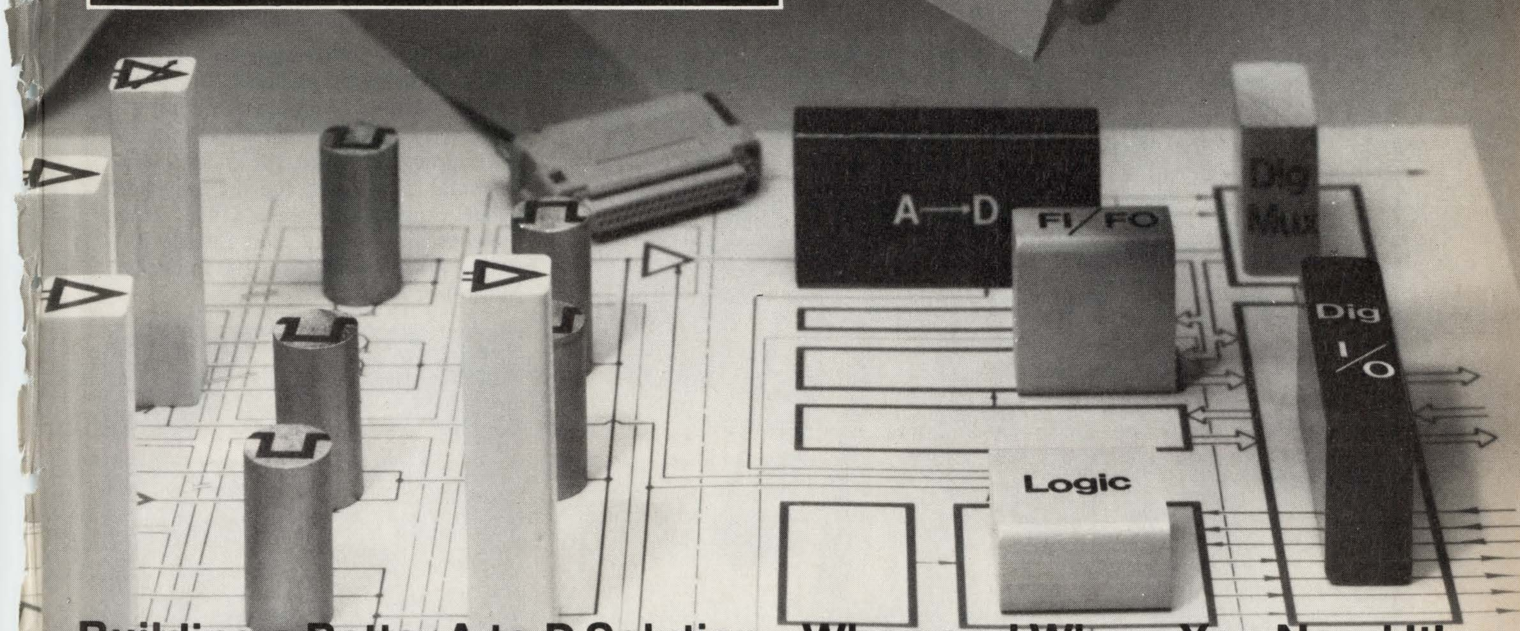

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Wide bandwidth FET op amp

Characterized by a differential input impedance of 100G Ω, gain bandwidth product of 300 MHz, ±250-V/μs slew rate, and 90-dB open-loop gain, the AH0008C is a field effect transistor op amp in an 8-pin DIP. Op amp is suited for current to voltage conversion; A-D, D-A, and sample/hold; and video amplification. With a settling time of 300 ns to 0.1% of intended value, output is ±10 V into a 1k-Ω load with a ±10-mA drive current. Op amp is sold in 100-piece quantities for $42.50. **Optical Electronics Inc**, PO Box 11140, Tucson, AZ 85734. **Circle 315**

Single-chip micro RAM

X2444, a 256-bit nonvolatile RAM, serves as a direct interface to single-chip microcomputers. Packaged in an 8-pin DIP, RAM has a sync serial communication bus with 3 I/O lines, serial data I/O, and clock. Additionally featured is an instruction to place the chip in a low power condition; this reduces current from the 15-mA active level. This RAM has a 5-V supply, 16 x 16 organization, and 2 memories—an EEPROM overlaid on a static RAM. Data are transferable between the 2 memories by store and recall operations. **Xicor Inc**, 851 Buckeye Ct, Milpitas, CA 95035.
Circle 316

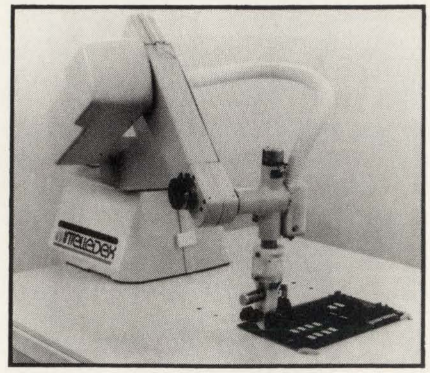
EMI PROTECTION

Filter kits

A general purpose kit and a digital systems kit are available to aid prototyping emi control. The General Purpose Kit contains 48 filters from 4 series in both solder eyelet and bolt style configurations. The Filter and Filter Assembly Kit contains 30 solder eyelet filters from 5 series, 3 filtered connector assemblies, a 37-position type D, and a 50-position latch type pin header. Each kit has filters functioning between 2 MHz and 18 GHz and an instruction manual. **AMP Inc**, Harrisburg, PA 17105.
Circle 317

CONTROL & AUTOMATION

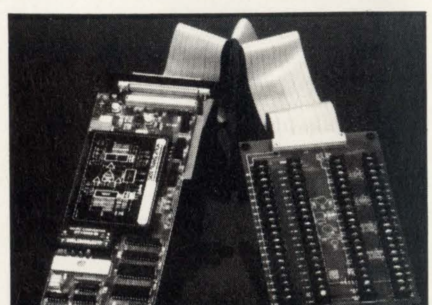
Manufacturing robot



Designed for precision parts handling and light material transfer applications, the 505T is a 5-axis robot. Arm is free standing for installation and motion flexibility, while programming is simplified by a personal computer and Robot BASIC. System features 3 RS-232 ports and four 8-bit parallel data buses with full handshaking capability. With a 0.001" (0.025-mm) repeatability, and robotic hand with auto-tool change the system sells for $38,000. **Intelledex Inc**, 33840 Eastgate Cir, Corvallis, OR 97333.
Circle 318

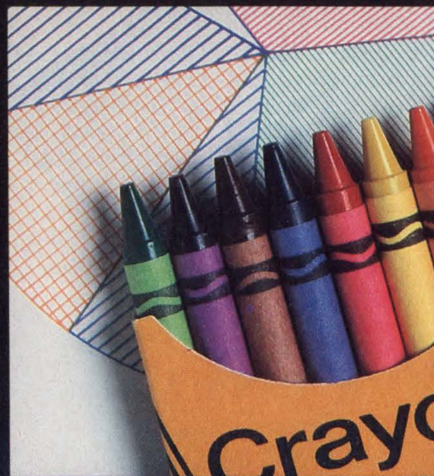
IBM-PC data acquisition system

The DT2805 is a single-board I/O system that features an 8 channel 12-bit ADC with software selectable gains of 1, 10, 100, or 500. Board includes 2 DACs with 12-bit resolution, 16 lines of digital I/O, and an onboard programmable clock. Microprocessor based, the system is programmable in BASIC and assembly language. Single-unit price is $1295, which includes user manual and sample programs. **Data Translation**, 100 Locke Dr, Marlboro, MA 01752.



Circle 319

A coloring book for your computer.



This is no children's toy. This is no-nonsense quality, yet affordable. It's the Panasonic Digital Plotter — the high-speed peripheral that turns business computer graphics into high resolution full color hard copy.

Nothing can match the Panasonic Plotter in its price range. It provides six-color graphics at a fast 400mm (16″) per second, with a choice of fiber, ball point or plastic tip pens in black, red, purple, blue, green and brown.

What's more, it's got a high level of built-in intelligence that greatly simplifies external programming. With simple commands, you create lines, circles and a full ASCII character set. Plus complex, colorful grids, bar graphs and pie sections. All as easy as pie!

It features an electrostatic paper-holding system for secure, high-stability plotting. An Automatic Chart Advance option for continuous, un-attended plotting. And three available interfaces — 8-bit parallel, RS232C serial and GP-IB — for compatability with most common minis and micros, as well as for instrumentation graphics.

For complete details, write or call today: Panasonic Industrial Company, Information Systems Group, One Panasonic Way, Secaucus, NJ 07094; (201) 348-5337. In Chicago call (312) 981-4824.

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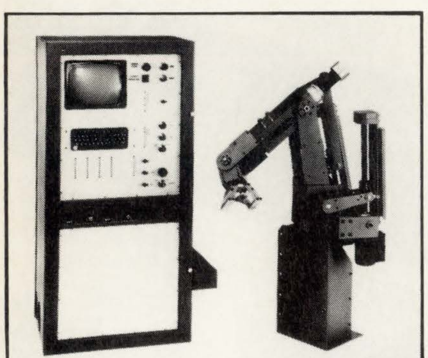
CIRCLE 119

Industrial micro robot

Microbot Alpha is a programmable micro robot for use in small-scale industrial applications such as electronics, precision instruments, and pharmaceuticals. The self-contained system uses a 5-axis humanlike arm with an 18″ reach and motions that include base rotation of 330°, shoulder bend 140°, elbow bend 140°, wrist roll 360°, and wrist pitch 180°. Robot offers 2 programming options. One is a handheld device to retain 227 sets of working positions. The other is through an RS-232-C interface, using other computers with the proprietary language, ARMBASIC. System is priced at $8500. **Microbot Inc**, 435-H Ravenvale Dr, Mountain View, CA 94043.
Circle 320

Robotic system



With a controller and gripper, the Charger is a 6-axis robot for industrial and educational applications. Controller is capable of running 2 motors in addition to the robot. It allows the robot to operate a double gripper or linear slide base. The 8-axis controller incorporates an Apple IIe and 2 disk drives, making it software programmable. The robot features a self-test/diagnostic program, 12 types of hands, a payload of 50 lb, and a resolution and repeatability of 1 mm or better. Standing 28″ (71 cm), the device sells for $20,000. **Rhino Robots, Inc**, 2505 S Neil St, Champaign, IL 61820.
Circle 321

Resource management

An integrated system for manufacturing resource planning (MRP), the HiNet/MRP provides 5 workstations (expandable to 32) and a set of software modules. Hardware consists of 2 user stations with 256K RAM, 3 with 64K RAM, and 46M-byte Winchester storage. Software consists of a CPM based LAN with office automation and business graphics. Modules offer inventory control, sales order entry, and material requirements planning. They also feature an auto update on other modules in the closed loop system. With multitasking capabilities and a training program, the system sells for $39,950. **Digital Microsystems**, 1755 Embarcadero, Oakland, CA 94606.
Circle 322

Industrial control system

The 6400 programmable controller system consists of a controller board programmed by the development system for specific applications. Board features include: 4K to 16K bytes of memory, 8-bit resolution 8-input ADC, RS-232 serial port, 24K EPROM space, 10-bit resolution DAC, three 8-bit parallel ports allowing 24 I/O lines, and 3 programmable counter/timers. The development system contains a power supply, monitor software, 16K RAM, and an EPROM programmer. The board is priced at less than $800; an IEEE 488 option is less than $300, and the development system is less than $1250. **Norland Corp**, Rte 4, Norland Dr, Fort Atkinson, WI 53538.
Circle 323

INTERFACE

Multibus printer controller

The MLP-2000 is a dual line printer controller that supports 2 Centronics or Dataproducts compatible printers from a Multibus slot. Accessing both printers over 2 independent high speed DMA channels, the interface has a parallel data transfer rate of 1.6M bytes/s max. I/O addressing is 8- or 16-bit switch selectable. The controller features a self-test that lets the user test either printer by flipping a switch. The test sends a 96-char ASCII pattern to a printer that checks controller operation without CPU intervention. The printer is $650. **Systech Corp**, 7630 Miramar Rd, San Diego, CA 92126. **Circle 324**

IEEE 488/IBM PC interface

PC-MATE interface board uses the IEEE 488 (GPIB) protocol and offers a companion software package. Implementing the Intel 8291A and 8292, the board provides talker, listener, and controller capabilities while allowing a programmable data transfer rate and handshaking. With test and measurement, process control, and laboratory applications, the interface board is available for $395. The software package, with high-level language interfaces, sells for $95. **Tecmar Inc**, 23600 Mercantile Rd, Cleveland, OH 44122.
Circle 325

Host adapter

Single-board emulating host adapter UC01/LX emulates the RLV11/RLV12 controller with multiple disk units to support drives in the 5.2M- to 83.2M-byte range. Adapter supports 22-bit addressing to provide full 4M-byte memory capacity for LSI-11s. Other features include self-test microcode, 3 selectable bus register start locations, and 2 vector addresses/register set. The adapter also emulates 2 independent register sets in a single-quad board. List price is $1900 with OEM discounts. **Emulex Corp**, 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.
Circle 326

Error correcting controller

Hard disk controller board, model HDC-1001 operates up to four 8" or 5¼" disk drives and has error correcting capability via a 32-bit computer generated polynomial. Other features include 8-bit single burst correction, multiple burst detection, and programmable correction/detection span. S-100, IEEE 696 compatible, the board has data rates up to 5M bytes/s, 256 sector addressing range, and CRC generation/verification on ID fields. Complete with CP/M BIOS diskette, the controller is priced at $500. **Advanced Digital Corp**, 12700 B Knott Ave, Garden Grove, CA 92641.
Circle 327

Cached disk controller

The ASC-525 is an integrated disk controller. The 5¼" board uses SCSI and ST506 interfaces to control up to three 5¼" drives. Between the interfaces is a 256K- to 512K-byte cache for fast access times. An 8088 performs host communication, disk transfers, and cache management; the Western digital chip set is used for Winchester control. Track caching is performed by the processor, with an LRU algorithm, and tracks are read and written (with no interleaving) for fast performance. Initial unit pricing is $1500 for the 256K version. **Advanced Storage Concepts, Inc**, 8720 S Gessner, Houston, TX 77074. **Circle 328**

DATA CONVERSION

A/D package

FASTRAK is a hardware/software analog conversion package for use with LSI-11/23 based systems. Analog conversions occur at a rate of 100k samples/s into files as large as 16.7M samples. A 200k-Hz throughput rate to disk can be achieved. A watch mode displays data passing to memory (for error detection). In addition, a data sensitive triggering feature allows slow-rate gathering until a predetermined criterion is met. Complete hardware/software package is priced at $6180. **ADAC Corp,** 70 Tower Office Pk, Woburn, MA 01801.
Circle 329

A-D converters

The MN5290 and MN5291 are 16-bit A-D converters with an extended temp range. Designed for operation over the full −25 to 85 °C and −55 to 125 °C temp ranges, the converters guarantee ±0.003% FSR max linearity error and no missing codes for 14 bits at room temp. The MN5290 also guarantees ±0.006% FSR linearity and no missing codes over the entire temp range. Devices are packaged in a 32-pin ceramic chip and consume 1.08 W max. Prices range from $137 (100s) for the MN5291 commercial version to $199 (100s) for the MN5290 883 screened version. **Micro Networks Co**, 324 Clark St, Worcester, MA 01606.
Circle 331

16-bit S/R-D converter

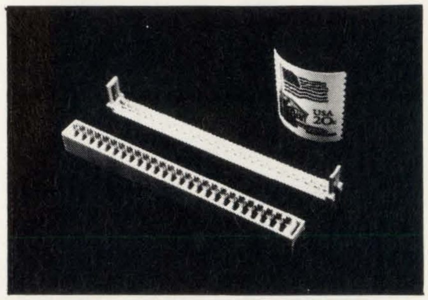
SDC/RDC1721 synchro/resolver to digital converter has a 3-rps tracking rate with typ accuracy of ±40 arc-seconds. Based on type 2 servo loop, the tracking technique produces continuously updated, TTL-compatible digital output in byte selectable format. Internal transformer isolation is to 500 Vdc on signal and reference inputs with operation from 360 Hz to 2.9 kHz. Housed in a 2.625" x 3.125" x 0.8" (66.675- x 79.375- x 20.3-mm) module, the converters operate with ±15- and 5-V power supplies; typ power dissipation is under 1.9 W. **Analog Devices, Inc,** Rte 1 Industrial Park, Norwood, MA 02062.
Circle 330

Data acquisition for IBM PC

As a plug-in data acquisition board for the IBM PC, the DT2805 features low-level software gains of 1, 10, 100, and 500. The board offers an 8-channel 12-bit A-D converter system, 2 D-A converters with 12-bit resolution, 16 lines of digital I/O, and an onboard programmable clock. Combining the onboard microprocessor with microcode, the system acts as the interface between computer and board, controlling I/O operations and self-test functions. Single unit price for the DT2805 is $1295 complete with user manual and sample programs. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752.
Circle 332

INTERCONNECTION & PACKAGING

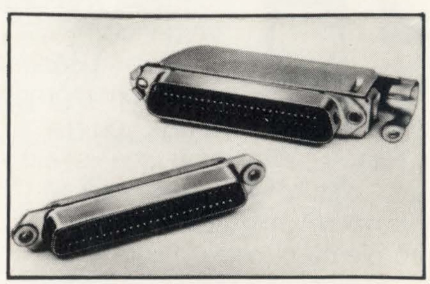
Socket connector



Compatible with MIL-C-83503, a low profile socket connector with polarity bump is available in sizes from 10 to 60 pins. Designed for mass termination of 50-mil flat cable, the device ensures positive connection by using 2 cutting surfaces, gas-tight connections by abrasion, and gold-over-nickel plated contact areas. With a temp range of −55 to 105 °C, current rating of 1 Adc, and a 20 mΩ max at 6 Vdc contact resistance, the connector is priced at $1.88 in quantities of 1-99. **Belden,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 333

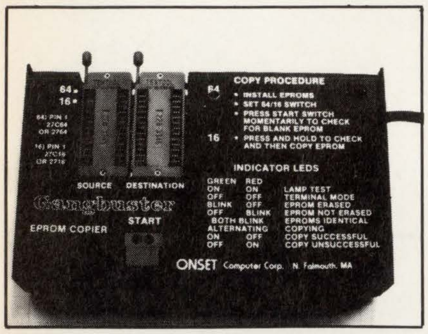
Telecomm connector

The MIL-C-83515 is a MIL-Spec version of the standard circuit Cinch telecommunications ribbon connector. The connector covers 6 styles of 14, 24, 36, and 50 contact plugs and receptacles in both std and high barrier types with solder-well and PC terminations. The connector's contact plating is 30μ in select gold plate. No formal qualified parts list status exists for the device, but first article inspection is required for each contract that uses the ribbon connector. **TRW Connector Div,** 5725 E River Rd, Chicago, IL 60631.



Circle 334

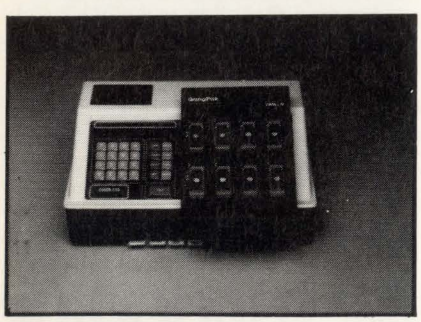
Fast EPROM copier



Gangbuster is an EPROM copier/programmer that allows copying of 16K EPROMS in as little as 15 s and 64K EPROMS in 30 s. When connected to a terminal or computer, copier can on/offload hex files, display and alter single bytes, or move data in blocks from EPROM to EPROM. Gangbuster can program 2716, 27C16, 2764, 27C64 EPROMS and, together with a personal computer, forms a low-cost development system. Price is $450. **Onset Computer Corp,** PO Box 1016, North Falmouth, MA 02556.
Circle 335

Multiple PROM programming

GangPak will program up to 8 MOS PROM sets and wide words in one operation. Separate downloading and programming operations can be eliminated as the operator loads device type and set size. The data are then partitioned by the software into appropriately sized blocks. Programming algorithms are software controlled with each device programmed by a 4-digit code. Other features include device testing and programming of single-voltage EEPROMS, 16k x 8 EPROMS, and 32k x 8 EPROMS. GangPak sells for $2150. **Data I/O,** 10525 Willows Rd, NE/C-46, Redmond, WA 98052.



Circle 336

Debug system

The Integrated Instrumentation and In-Circuit Emulator (I[2]ICE) is designed for development and integration of complex microprocessor systems. System consists of 3 tools: a 16-bit in-circuit emulation system, high-level language debugger, and a 16-channel, 100-MHz logic timing analyzer. PSCOPE software provides support for symbolic references, high-level language constructs, and generalized break and trace functions. Emulation system performs transparent, realtime emulation at processor clock rate for the iAPX 16-bit micros. The price for the Emulator Base System is $16,200. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 337

PROM programmer

The PROM-200 programs all industry std EPROMS, single-chip microcomputer EPROMS, 16-, 20-, and 24-pin bipolar PROMS and 20- and 24-pin programmable gate arrays. With CP/M disk based software to provide reading, verifying, and programming of different PROMS, the board offers 5 adapter cards. Software is user friendly and has a programming algorithm that cuts programming time from 50% to 70%. An expansion connector allows a Gang programmer to be added that can program 8 devices at the same time. **Advanced Microcomputer Systems, Inc**, 3501 University Dr, Coral Springs, FL 33065.
Circle 338

EPROM and EEPROM programmer

For use with RM 65/RME bus-compatible microcomputer systems, the RM65-2901E is a PROM programmer for EPROMs and EEPROMs. The module programs 1K-, 2K-, 4K-, and 8K-byte EPROMS and 2K-byte EEPROMS; fits std RM 65 card cages; and has an onboard converter. The programmer supports 2758, 2758L, 2508, 2716, 2516, 2732, 2732A, 2532, 2764, 2564, 68764, and 68766 EPROMS, as well as 2816, 5213, and 48016 EEPROMS. Module is priced at $295 with volume discounts available. **Rockwell International, Electronic Devices Div**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 339

Automated drafting system

System A-CADS/1 comes with 512 x 256 resolution CRT, LSI-11/23 CPU, 64K-byte RAM, 5 serial RS-232-C ports, video display controller, floppy/Winchester controller, plotter, and digitizer. Running under DEC's RT-11, DesignGraphix® interactive software permits a variety of predefined symbols and allows the user to create figures. The system includes text handling and graphics editing capabilities. Mass storage capacity is 5M bytes, with 512K-byte removable floppy storage. System price is $24,000. **Andromeda Systems, Inc,** 9000 Eton Ave, Canoga Park, CA 91304. **Circle 340**

COMPUTERS

Small computer

A small computer system, the HP 86B has a built-in electronic disk that provides high speed mass storage capabilities. The system includes a 12″ monitor and an HP 9121S 3½″ disk drive. For disk-intensive applications, the data transfer rates are approx 10 times faster than a flexible disk drive. Computer features 128K bytes of user memory, expandable to 640K bytes, and an HP-IB interface for connections to the HP 9121 3½″ disk drive. Available with local language keyboards, the system sells for under $3000. **Hewlett-Packard,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 341

HP's 5180A...the Waveform Recorder for bench and ATE.

From now on, your waveforms have few secrets.

Now, those difficult time, amplitude, and frequency measurements of repetitive and transient signals needn't be a problem. Because HP's 5180A Waveform Recorder lets very few signals escape detection. And it reveals your captured waveform's important characteristics. The reason? It combines the features you need for reliable signal capture, accurate digitizing, and fast processing.

For example, flexible digital triggering snares those hard-to-capture random transients. You get the entire signal, single shot, from the 5180A's 10 bit resolution, 20 MHz ADC. And a 16k-word memory gives you lots of storage for complex events. The 5180A also delivers exceptional dynamic performance, which means accurate results. That's important in tasks such as frequency domain analysis where your results must be reformatted. And DMA (Direct Memory Access) means fast data transfer to a computer for rapid signal processing.

Your solution for benchtop or system use.

As an integral part of your custom automatic test system, the HP 5180A, is the first in a new generation of universal waveform recorders. All front-panel controls are accessible via HP-IB. Measurements stored in memory can be read out in either ASCII or binary format, or transferred at up to 1 Mword/sec via DMA. Combined with an HP Series 200 desktop computer, the HP 5180A forms the core of a very powerful and versatile waveform capture and analysis system.

In benchtop applications, simply attach an HP 1332A display and you have a powerful, stand-alone test instrument. For truly impressive hardcopy output, connect a digital plotter such as the HP 7470A directly to the built-in HP-IB port for fully annotated plots.

In either environment, the 5180A can do the job of several instruments, saving you cost and complexity.

Can the 5180A handle your difficult measurements?

In disc drive testing, the 5180A's 16k memory can capture an entire sector of data.

You can use the 5180A's bi-level trigger to capture DC-erased drop-outs. And an external timebase input allows compression of data to capture long events or equivalent time sampling of repetitive signals up to 70 MHz. In the video world, post trigger delay lets you capture a specific line in a frame. And 40 MHz bandwidth means there's no phase distortion. For VCO testing, the 5180A provides a dual timebase for measuring both settling time and post tuning drift in a single record. Have you ever needed to strip off the AM and FM modulation from a single radar pulse? With the 5180A you can do it. In fact, this waveform recorder is built to handle a host of difficult measurements, including power-supply characterization, radar IF processing, laser pulse measurements, and many more.

HP has the support you need for those critical applications. A large and growing library of contributed software is available to you, including 1 second Fast-Fourier Transform (1K record) and DMA routines. In addition, each HP 5180A, like every HP product, is backed by our worldwide service and systems engineering staff.

Want more information?

Contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department, and request a copy of our full color data sheet.

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HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

CIRCLE 122

YOUR ANSWERS TO THESE QUESTIONS HELP US SERVE YOU BETTER

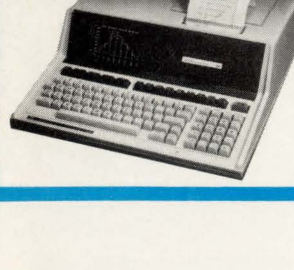
YOUR ANSWERS ARE IMPORTANT. The results of these surveys help our editors select topics, features and technical data that will be on target with your design activities. Your inputs also alert manufacturers to your needs and can result in the development of product speeds, ranges, capacities, and other specs that you require.

YOUR ANSWERS CAN ALSO WIN YOU A VALUABLE PRIZE!

Each questionnaire returned gives you a chance to win a special prize. Drawings are made after each issue, with a grand prize drawing at year end.

***MONTHLY DRAWING* — HP 41CV PROGRAMMABLE CALCULATOR**

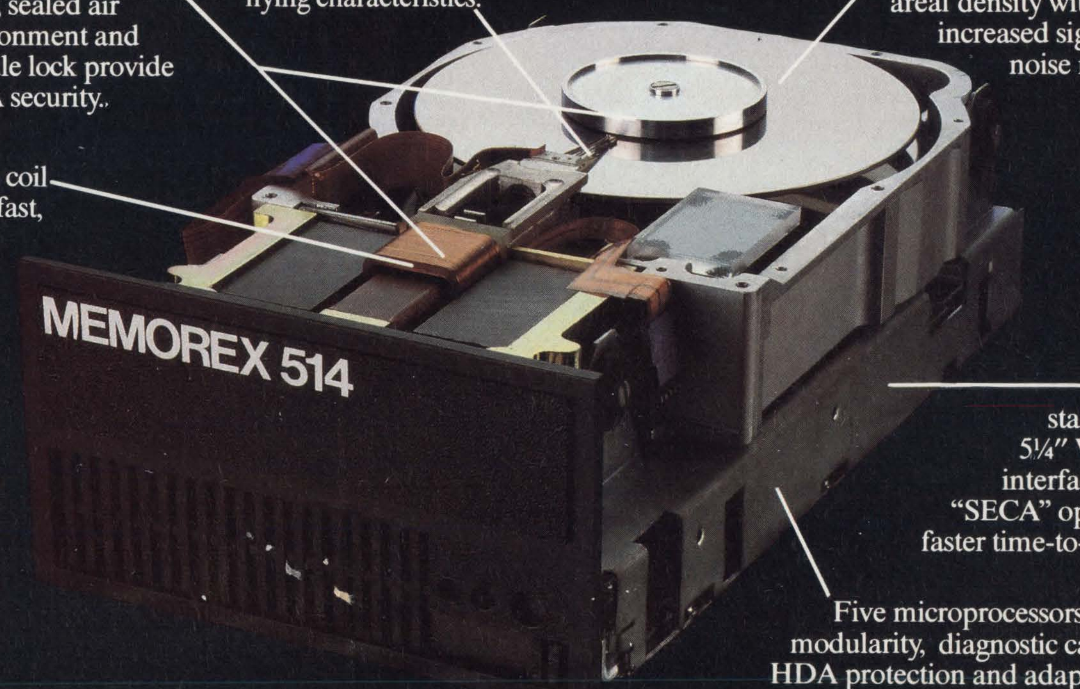
The HP 41CV offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total functions in program library. Memory expandable to almost 6,500 bytes.



***ANNUAL DRAWING* — HP 85 DESK TOP COMPUTER**

This portable (20 lb.) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56K byte memory, CRT screen, and 150 built-in BASIC language commands. You can add peripheral and software packages to expand system capability. A $2800 value!

70 Mbytes. 5¼" Package. Memorex Quality. And Just The Beginning.



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The Memorex 500 Family: Expandability, Accessibility And Reliability.

The first three members of our 500 Family, the 510 Series, feature a choice of 30, 50 and 70 megabytes of capacity with an industry-standard 5¼" disc drive interface. Average seek time is 25ms which, when combined with our switch-selectable "SECA" mode, significantly reduces net system time-to-data. Our linear voice coil actuator and advanced servo design give a maximum seek time of only 45ms and a track-to-track time of just 3ms. But even more significantly, this technology sets a base for future drives with higher capacities and even faster access times.

Above all else, reliability and quality are key to the 500 Family design. By choosing a base design with capabilities well beyond the current series, our drives feature servo and read channels with extremely wide operating margins. And by using an advanced electronic architecture with five interconnected microprocessors, we provide adaptive control systems which continually monitor critical parameters throughout the life of the drive and make dynamic adjustments to compensate for wear and component aging. In this way we obtain and retain true reliability throughout the life of the system.

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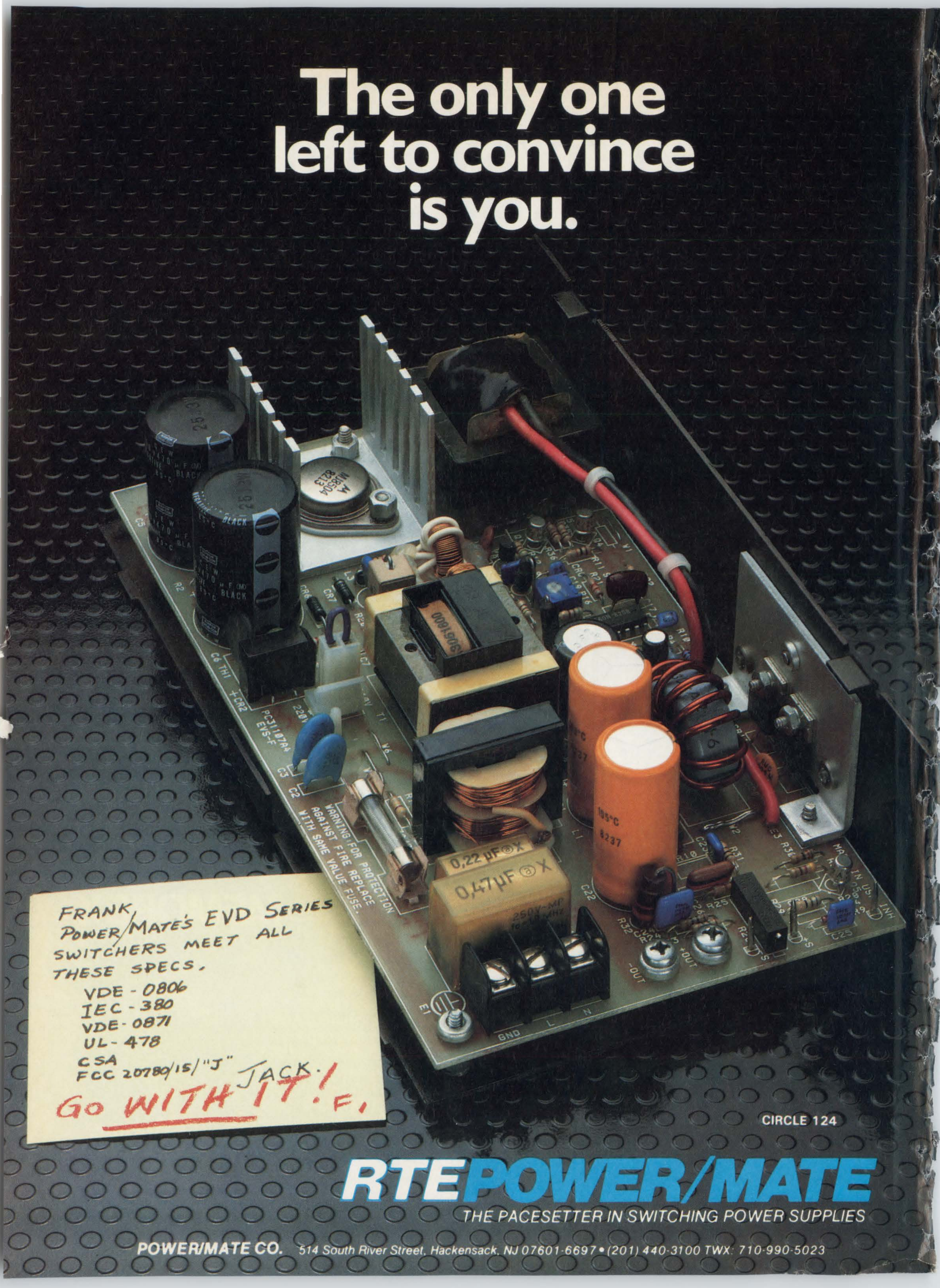
CIRCLE 123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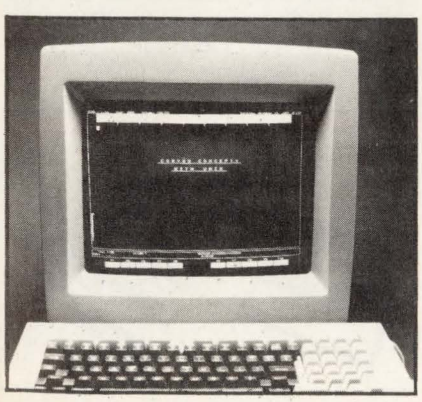
Personal business computer

The Executive is a portable, personal computer for business applications. Featuring 128K bytes of memory, 7″ amber video display, 80-col capability, and universal terminal emulation for mainframe communication, the system also includes 2 half-height disk drives with 200K bytes/disk. Software package includes CP/M plus (3.0), Wordstar, and various BASIC versions. Computer has a soft keyboard and writable font for customized symbols and matching key definition for mainframes. System retails for $2495 complete; modem option is available for $265. **Osborne Computer Corp**, 26538 Danti Ct, Hayward, CA 94545.
Circle 342

Office automation workstation

The Concept+ is a multitasking workstation with applications in word processing, database management, and scheduling. Based on the M68000 microprocessor, the system I/O structure includes 2 serial ports, 4 bus slots for peripherals, and LAN capability. C language processors are included with the system, while versions of Pascal, BASIC, FORTRAN, and COBOL are also available. Priced at $6995, the system will be available in August. **Corvus Systems**, 2029 O'Toole Ave, San Jose, CA 95131.



Circle 343

Array processor

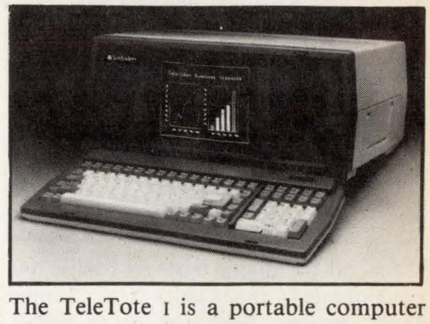
A 64-bit array processor, model MAP-6410 allows micro, mini, or superminicomputers to perform iterative math functions with mainframe accuracy. All arithmetic operations are true floating point in a 64-bit Hex format, providing over 16 decimal digits of precision. Three levels of software are available: MAXPAK, which allows FORTRAN programmers to use the device without knowledge of array processors; SNAP II operating system with FORTRAN callable functions; and assembly language utilities. Prices start at $50,000 for the basic system, that consists of 16-slot chassis with power supply, CSPU control processor, 64-bit wide arithmetic processor, 128K bytes of program memory, and 512K bytes of data memory. **CSP Inc**, 40 Linnell Cir, Billerica, MA 01821.

Circle 344

16/8-bit professional computer

Designed to be used as a standalone unit or as a workstation on an office communications network, the 16/8 professional computer offers concurrent processing via 2 microprocessors in 1 system. The 16-bit microprocessor is based on the Intel 8086 and has an expandable base of 128K bytes of memory, while the 8-bit microprocessor uses a Z80A with 64K bytes of memory. Available operating systems include CP/M 86, MS-DOS and CP/M 80. Storage options include single-sided and double-sided/double-density 8″ disk drives, or 5¼″ drives with an expansion module. System price ranges from $3395 to $5295 depending on storage capacity. **Xerox Corp, Office Products Div**, 1341 W Mockingbird Ln, Dallas, TX 75247.
Circle 345

Compact computer



The TeleTote I is a portable computer with network capability. It has a 9″ display and 640 x 240 resolution and is software and media compatible with the 8-bit TS803. Based on the Z80A, the system features 64K-byte RAM, 9368.6K-byte (formatted) 5¼″ floppy disk drive, a super mouse port, and 2 RS-232 printer/modem ports. Computer comes with the CP/M operating system, GSX-80 graphics extension, word processing, spread sheet, and graphics software. Compact system is priced at $1499; network option is $495. **TeleVideo Systems Inc**, 1170 Morse Ave, Sunnyvale, CA 94086.
Circle 346

Upgradable computer system

MegaFrame is a computer system that allows the OEM to start with a small system and add specialized processing units as needed. These units include an application processor that runs programs under Unix with performance of 8 MIPS; a file processor that executes the file system; and the terminal and cluster processors that control communications with SNA, 3270, X.25 and 2780/3780 protocols. Systems range from the single-enclosure system that sells for $17,546 to the 5-enclosure system that sells for $110,250. **Convergent Technologies, Data Systems Div**, 3055 Patrick Henry Dr, Santa Clara, CA 95050.
Circle 347

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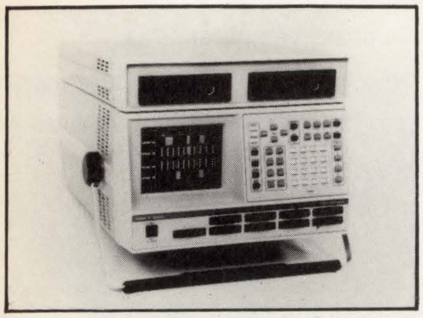
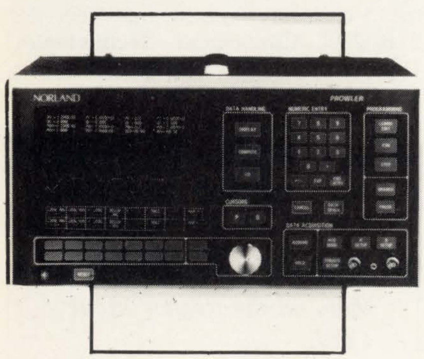
Modular logic analyzer



Intended for digital systems design and development, the K105-D is a 72-input logic analyzer. With a modular design, the analyzer can be set at 32 or 64 main (20-MHz) and 8 or 16 high speed (100-MHz) state and timing sample inputs. RS-232 compatible, with disk storage and disassemblers for 8- and 16-bit microcomputers, the device uses menu-driven screens for interactive aid and can be expanded with an integral storage system. Base unit sells for $5000 with the max-configured system selling for $17,585. **Gould Inc, Design & Test Systems Div**, 4600 Old Ironsides Dr, Santa Clara, CA 95050-1279.
Circle 348

Digital scope

The Prowler is a portable processing digital scope with a sample rate of up to 20 MHz. It features 1 or 2 channels of acquisition where each channel has 4K to 16K of acquisition memory. The scope is also user friendly via the CRT, which offers step by step instruction through each mode. The front panel uses a softkey approach, and processing capabilities include integral, derivative, multiply, divide, add, subtract, natural log, peak to peak and trig functions. **Norland Corp,** Rte 4, Norland Dr, Fort Atkinson, WI 53538.



Circle 349

Analyzer emulates data comm protocols

Data link analyzer 803B provides full emulation capabilities for data communication protocols including interactive X.25. As a monitor, the device features auto detect of protocols, data rates, bit-per-character values, and parity. As an emulator, the analyzer provides emulation for async and sync byte-controlled and bit-oriented protocols at data rates up to 56k bps. Unit has a full ASCII keyboard, 7" CRT display, and dual microfloppy disks that provide 640K bytes for user program data and storage. Depending on options, the analyzer is priced between $14,000 and $16,000. **Halcyon Communications Inc,** 2121 Zanker Rd, San Jose, CA 95131.
Circle 350

Linear and digital test system

The 1735 component test system combines linear and digital test capabilities for applications in incoming inspection, device characterization, and device failure analysis. The system consists of a mainframe controller and 2 plug-in boards, 1 for linear testing (op amp family board) and 1 for digital testing (universal family board with AppsPac applications package). Prices for the system begin at $35,000 with deliveries scheduled for the third quarter of this year. **GenRad Inc**, 170 Tracer Ln, Waltham, MA 02254.
Circle 351

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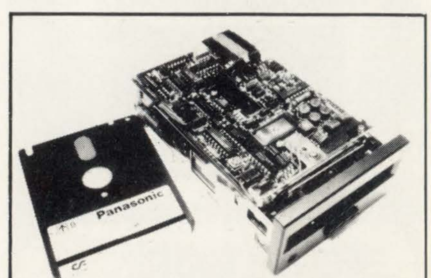
Component test board

The LTS-2600 transistor/diode family board is capable of testing bipolar, MOSFET, and JFET transistors, diodes and optocouplers. Specs include voltage force and measurement from 10 mV to 600 V and current from 100 pA to 20 A. An onboard 16-bit microprocessor handles pulse and measurement timing of the DUT test signals. It also coordinates test functions and programs pulse width from 50 to 300µs. Board has an overall test accuracy of ±0.25% to ±2.0% and comes with system software for component testing. Base price of the LTS-2600 is $7000, including additional power supply. **Analog Devices,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.
Circle 352

MEMORY SYSTEMS

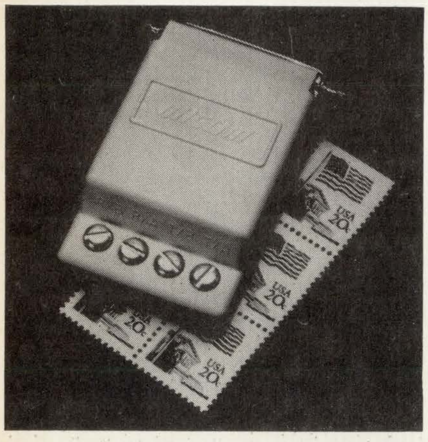
3" floppy disk drive

EME-101 3" floppy disk drives offer recording method, data transfer rate, and disk rotation speed compatible with 5¼" floppy drives. Drive storage capacity is 500K bytes/disk (double side, double density). Unit uses a direct-drive brushless dc motor with a steel band for fast access time. Up to 4 drives can be connected in a daisy chain. Disks are available in 500K-byte capacity, 100 tracks/in, and 300 rpm. **Panasonic**, One Panasonic Way, Secaucus, NJ 07094.



Circle 353

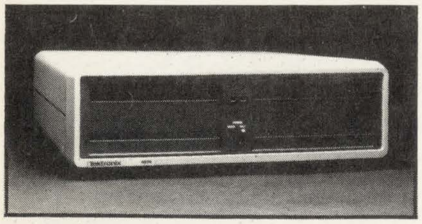
Data sets for local networking



For connecting terminals and computers in a local environment, the Micro400 local data set models 430 and 431 are available. Units plug directly into a terminal or computer RS-232 interface and are powered by the unit they support. Both devices provide full-duplex async communications and can send data over 3 mi when operating at 9.6k bps (further at lower speeds). Model 430 can cover more than a mile at 19.2k bps—intended for use on customer-owned lines—while the model 431 complies with Bell publication 43401 for operations over telephone company supplied circuits. The 430 is priced at $85; the 431 at $95. **Micom Systems, Inc,** 20151 Nordhoff St, Chatsworth, CA 91311. **Circle 354**

Mass storage device

Designed for use with the 4100 series terminals, the 4926 10M-byte hard disk uses 5¼" Winchester technology in which the disk media and drive heads are sealed. Disk has a standard 10M-byte formatted capacity, and an additional 10M bytes can be added. The drive connects to an intelligent interface in the terminal that features the mass storage interface bus (MSIB) and conforms to the SCSI spec. Interface includes DMA to take advantage of data rates over the MSIB, which allows 7 mass storage device controllers for additional capacity. The device is priced at $4200. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

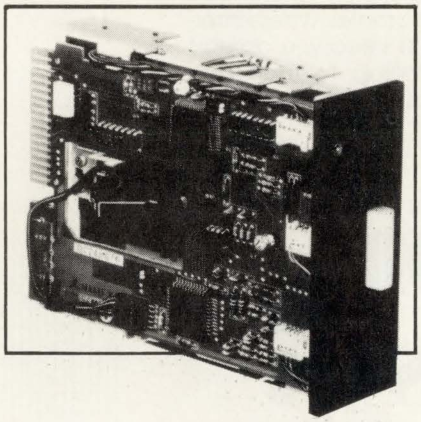


Circle 355

Bubble memory

With an extended temp operating range of −20 to 85 °C, the 7110-5 bubble memory is available in a production or prototyping kit. The memory includes VLSI controller with support circuits, 128K bytes of storage (nonvolatile from −55 to 100 °C), and has applications in navigation, robotics, and communications. Immune to the effects of dirt, vibration and shock, the memory has a 40-ms access time. Prototype kit is priced at $2390 and production kit sells for $1290 in lots of 1000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 356

High density/capacity drive



Model MF351 is a 3½" flexible disk drive that is 5¼" compatible. In 250K- and 500K-byte capacities, the drive features twice the density of conventional drives. With a 3-ms track to track access time, a 94-ms seek time, and a 50-ms head loading time, the drive uses ferrite heads in a Gimbal mounted assembly and a headload celonoid. Production will begin in the last quarter of this year; the device is priced at $190 in OEM quantities of 1000. **Mitsubishi Electronics America Inc,** 991 Knox St, Torrance, CA 90502.
Circle 357

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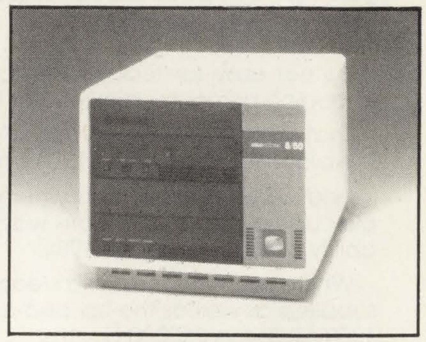
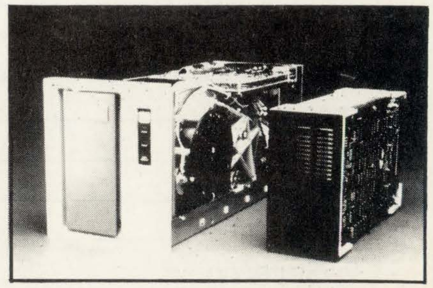
Disk modules increase storage



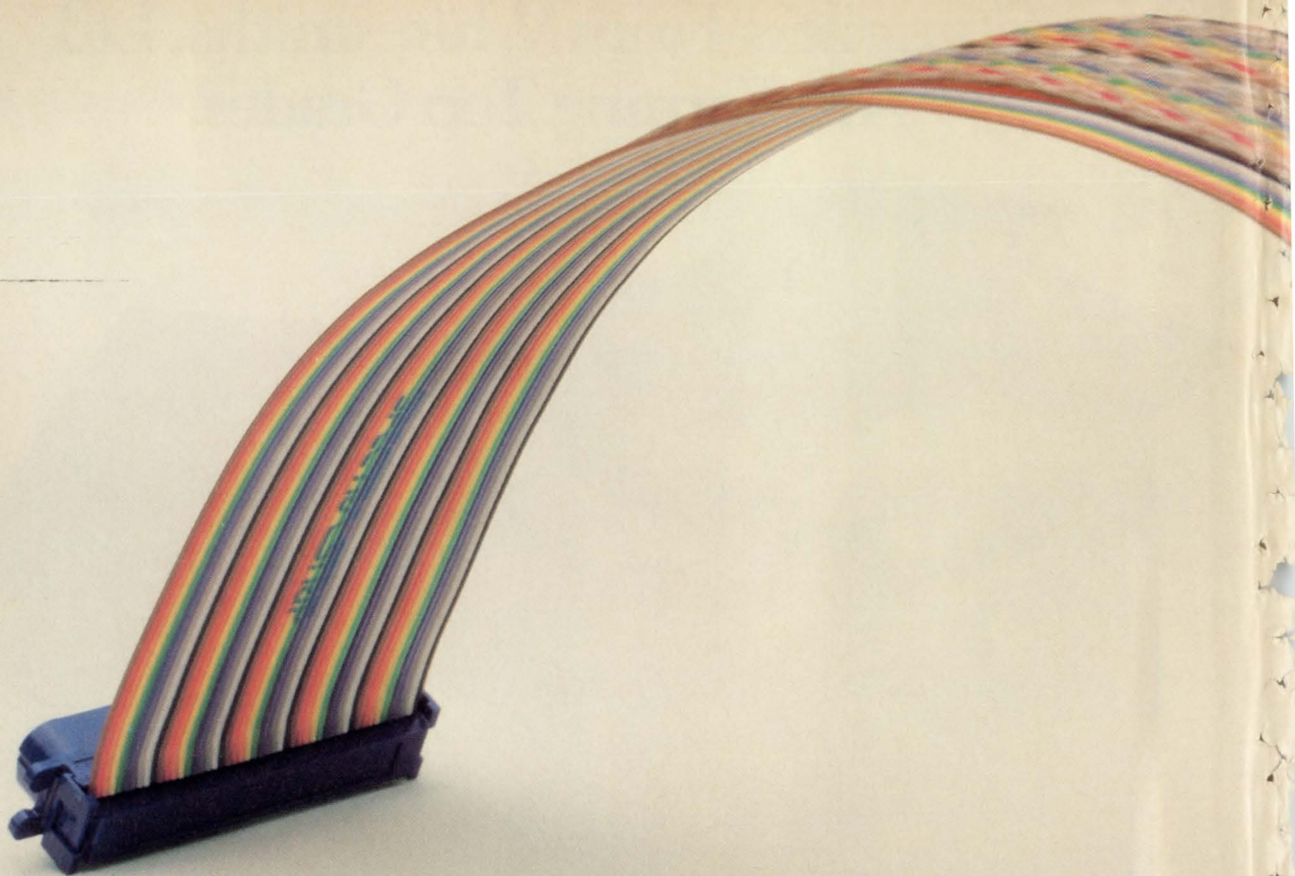
An optional disk system allows the 1116 workstation to expand its data storage capabilities. The 8/50 provides 50M bytes of hard disk storage in fixed (42.2M-byte) and removable (10.6 M-byte) Winchester formats, while the 8/80 provides two 42.2M-byte fixed drives. Features of the module include embedded servo, MFM recording, and linear voice coil actuator. System has all dc power and a microprocessor for servo, spindle, monitoring, and interface control. **SOLOSystems Inc,** 482 Oakmead Pkwy, Sunnyvale, CA 94086.
Circle 358

8" SMD Winchesters

The 1400 series of 8" Winchesters includes an 80M- and a 160M-byte unit. Drives are plug compatible with drives using the SMD interface and have a 22-ms average access time. Winchesters consume 125 W of power and have a 55-dB a rate. Units can be specified with 2 options: a 100/240-V, 50/60-Hz power supply; and a dual-port interface that permits 2 separate computers to access stored data. Initial pricing is $2387 for the 80M-byte 1403 SMD and $3013 for the 160M-byte 1460 SMD in 500 quantities. **Micropolis Corp,** 21329 Nordhoff St, Chatsworth, CA 91311.



Circle 359



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COMPARE

FEATURE	MICRO DIGI-PAD	vs.	MOUSE
Low cost	Yes		Yes
Small Package	Yes		Yes
Ergonomic	Yes		Yes
Low Power	Yes		Yes
Single Voltage	Yes		No (RS-232C Model)
Absolute Coordinates	Yes		No
Off Screen Menu	Yes		No
Trace Graphics	Yes		No
Stylus Option	Yes		No
4D (Stylus tilt output)*	Yes		No
4 buttons	Yes		No
Digitizer Compatible	Yes		No
Dual RS-232C	Yes		No
Hostile Environment	Yes		No
Proven Supplier	Yes		?

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CIRCLE 127

Cassette backup for IBM PC-XT

A streaming cassette tape backup system for the IBM PC-XT (hard disk version), the Sysgen Image includes controller, drive electronics, and tape drive. Storage capacity is 20M bytes; under software control, the system allows backup at 2.5M bytes/min. Image has 2 backup modes: preserve backs up data to and from individual disk volumes, while file-save allows files to be saved from the hard disk to streaming tape. Compatible with PC-DOS or CP/M-86, the system sells for $995. **Sysgen Inc**, 47853 Warm Springs Blvd, Fremont, CA 94539.
Circle 360

Memory boards offer increased throughput

ODP RAM-disk memory boards program microcomputer systems to access memory as a disk. This provides a tenfold increase in disk system throughput. While not a disk drive replacement, the boards eliminate disk I/O bottlenecks of CP/M, allowing faster program and execution time. Using the S-100 double height board, existing software can be used with no loss of compatibility. RAM-disks are available in 256K or 512K versions. **Quasar Data Products, Computer Systems**, 10330 Brecksville Rd, Cleveland, OH 44141.
Circle 361

Winchester backup

An integrated Winchester disk storage and backup subsystem, Secure is designed for the IBM PC and CP/M based computers. Software package includes utility for mirror imaging or selective backup and restoration of hard disk files on cartridge tape. Cartridge tape drives are available in 2 forms: the 45M-byte version (formatted) has transparent error detection/correction, data buffering, extended status reporting, and async data input; while the 26-byte version (formatted) offers floppy interface and compatible power requirements. With OEM and quantity discounts available, the system is priced at $3995. **Data Technology Corp**, 2775 Northwestern Pkwy, Santa Clara, CA 95051.
Circle 362

Memory subsystems

With capacities of 256K, 512K, and 1M bytes, Model 250 is a computer memory subsystem. Compatible with the Prime 2250, each memory card contains 64K bytes of RAM and a switch that allows users to turn the memory card off at any time. The four support options offered are onsite memory plan (OSM) as a backup system; OSM+ plan allows purchase of spare board; before repair replacement plan; and the factory repair or replacement plan. Fully upgradable, the memories are priced at $3900 for 256K bytes, $6450 for 512K bytes, and $9800 for 1M byte. **EMC Corp**, 385 Elliot St, Newton, MA 02164.
Circle 363

Small system Winchester

The RD 51 is a 5¼" Winchester for business and personal computer systems. The 10M-byte capacity disks interface with the Professional 350 computer and the MICRO/PDP-11. Characteristics of the medium include 345 tracks/in, a density of 9074 bpi and a peak data transfer rate of 5M bps. Drive has an average access time of 85 ms and a rotational latency of 8.33 ms. Organized as 1224 tracks of 16 sectors each, the drive has 2 data platters and 4 data surfaces. Disk drive is available at $1695; pricing as complete subsystems with controller is dependent on system packaging. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 364

Talk to the editor
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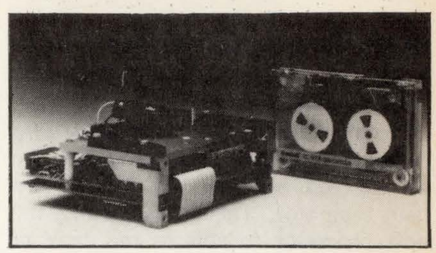
Cartridge tape drives



Two tape drives, model 6430 and model 6440 are intended for remote battery powered data logging applications. Power requirements are 11 to 14 Vdc at 0.6 A and 5 Vdc at 1.8 A typ; standby mode causes the drive to be switched off, eliminating power supply drain. Drive stores 17.3M bytes of data on a single data cartridge at 30 ips and has std and serpentine head configurations. The ¼" cartridge tape weighs 2.5 lb (1.1 kg) and dimensions are 3.25" x 5.75" x 6.90" (8.25 x 14.60 x 17.53 cm). **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, MD 20794.
Circle 365

10M-byte Winchesters

The ComFiler CR-1510 is a 5¼" Winchester disk drive that is compatible with the Epson QX-10. Disk drive features a storage capacity of 10M bytes (formatted) or 12.8M bytes (unformatted). The system is compatible with the CP/M 2.2 operating system and the QX-10/VALDOCS software system, and includes a controller and a QX-19 interface. Drive measures 5.25" x 7.8" x 14.5" (13.33 x 19.8 x 36.8 cm) and has a MTBF rating of 11k h. The CR-1510 retail price is $2295. **Comrex International, Inc**, 3701 Skypark Dr, Torrance, CA 90505.
Circle 366

High density recording media

The Isomax flexible disk is a high density magnetic recording media that extends the storage capacity of 5¼" diskettes. With the design of flexible disk drive systems that use 5¼" disks, the new media will operate at densities of 40k fcpi and increase storage capacity from 5M to 10M bytes for track densities of 96 and 200 tpi. When used with modified recording heads, the Isomax flexible disks support perpendicular recording with minimum phase distortion. **Eastman Kodak Co**, 343 State St, Rochester, NY 14650. **Circle 367**

Drives have SCSI interface

Model 31802 Winchesters have a single-board implementation of the SCSI. The drive plugs into a 6-slot backplane of a dedicated module that contains the drive's read/write logic, controller, and data separator. The board permits the host processor to address the drive in logical terms to reduce I/O programming. The drive uses an 8-bit bidirectional parallel bus in DMA mode. Transfer operations are monitored by an onboard 8085 microprocessor. The 8", 212M-byte Winchesters are priced at $6220 in single-unit quantities; $3700 in 500-lot orders. **MegaVault, an SLI Co**, 6431 Independence Ave, Woodland Hills, CA 91367. **Circle 368**

PERIPHERALS

Printer for COBOL workstation

The P/200 printer gives printing capabilities to the SOLOsystem 1116 workstation. The impact dot-matrix printer offers 200 cps in data processing mode or 50 cps in correspondence-quality mode. Standalone desktop system allows OS/VS COBOL programmers to write, edit, compile, and test their programs independently of a mainframe computer. Other specs include 132 cols at 10 cpi or 218 cols at 16.5 cpi (switch selectable), 9 x 7 or 18 x 40 dot-matrix format, and an RS-232-C interface. **SOLOsystems Inc**, 482 Oakmead Pkwy, Sunnyvale, CA 94086.
Circle 369

High speed printer

The 4245 line printer combines engraved steel-band technology and a 2000-line/min speed with a std character set. Features include 132 print positions at 10 chars/in, 6-part form capacity, full width ribbon, and a power assisted form stacker. System can be attached to 4300, 3031, or virtual storage/370 processors. Software support is DOS/VSE, and character sets include EBCDIC, scientific, FORTRAN/COBOL, and commercial. Printer sells for $63,500 with a monthly maintenance charge of $650; volume discounts and leasing options are available. **IBM Corp**, 900 King St, Port Chester, NY 10573. **Circle 370**

OCR scanner

The AlphaWord® series 80 contains 3 models (A, B, and C) of optical character recognition (OCR) page readers. Models A and B can scan 145 pages/hr, while model C scans 250 pages/hr. All models support RS-232-C, sync, and async interfaces. Features include self-diagnostics, the ability to read popular typestyles, and an operator message display and menu. With auto-formatting capabilities, model A sells for $12,990, B for $13,990, and C for $14,990. **CompuScan Inc**, 81 Two Bridges Rd, Fairfield, NJ 07006.
Circle 371

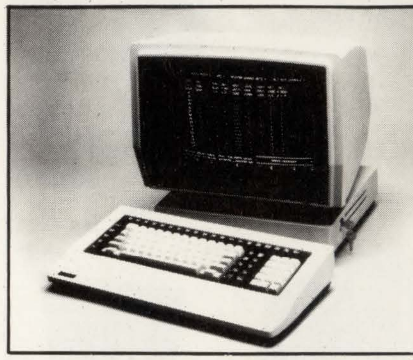
Personal computer mouse

For use with the IBM PC or MS-DOS based personal computers, the Microsoft Mouse comes with 3 application programs. The programs include a tutorial, practice application, and NotePad (a text editor software package that includes insert and delete features). Mouse standard interface driver supports BASIC, FORTRAN, and Pascal. Also available for use with the mouse is the Multi-Tool Word writing system. System allows users to insert, delete, and reposition blocks of text without using the keyboard. Mouse is priced at $195. **Microsoft Corp**, 10700 Northup Way, Bellevue, WA 98004.
Circle 372

Emulating terminal

The TDV 2235 terminal emulates the 6053/D200, while providing additional features including a 15" screen and a 7 x 9 dot matrix (vs 5 x 8). Selections from 4 menus are made from the keyboard or host computer and are stored in nonvolatile EAROM. Often-used words, phrases, or code can be stored via a fifth menu. A sixth menu controls tab rack setup. Terminal is certified to meet 1985 German ergonomic std. Its stand has height, swivel, and tilt adjustment. A 60-Hz refresh rate ensures flicker-free character display. Light intensity control adjusts text and background light for optimum contrast. Single-unit price is $1875. **Tandberg Data, Inc**, PO Box 99, Labriola Ct, Armonk, NY 10504.
Circle 373

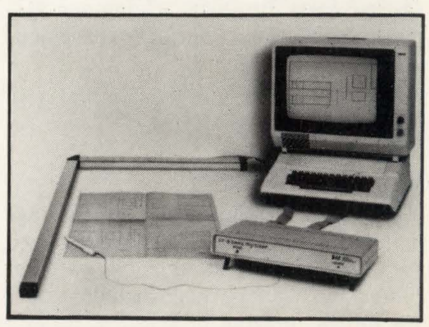
IBM-compatible display stations



Model 8278 display stations, compatible with the IBM 3278 series, come in 4 models. They operate in SNA and non-SNA network structures and attach to the Racal-Milgo 4270 series of remote and cluster controllers. Models 8278-2, -3, -4, and -5 have alternate screen formats, and all formats fill the 15" diagonal display. Std features include offline testing; security keylock; a detachable keyboard; and blink, underline, and reverse video. Price is $1999 to $2556 for single quantity. **Racal-Milgo, Computer Products Div**, 6250 NW 27th Way, Fort Lauderdale, FL 33309. **Circle 374**

Sonic digitizer system

Sonic digitizer GP-8 employs an 8-bit microprocessor that allows the unit to perform 5 std program functions via menu entry. Either stylus, cursor with cross-hairs, or both are used for menu selections and data entry. Basic specs include resolution of 0.01 (option to 0.005), digitizing rate of up to 50 points/s, and baud rates switch selectable to 19.2k. System applications include data processing, recording, and transmission equipment. **Science Accessories Corp**, 970 Kings Highway W, Southport, CT 06490.



Circle 375

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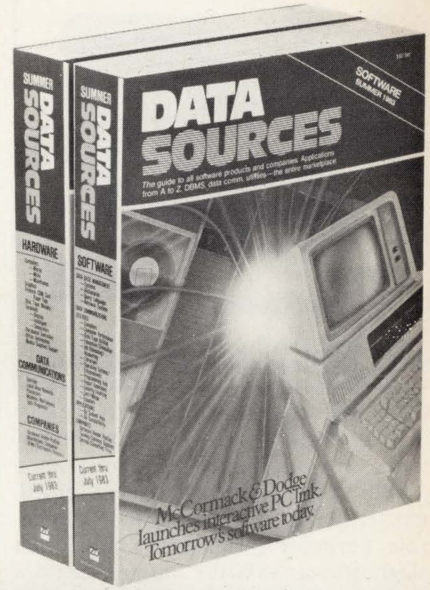

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T023

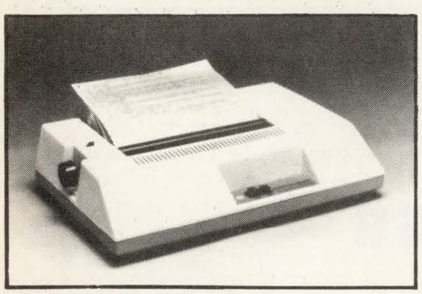
CIRCLE 128

Emulation terminal

Operating in conjunction with the virtual terminal system, the ICOT 700 terminal provides support for a serial ASCII printer and acts as a replacement for IBM 3278 terminals. Features include detachable keyboard, calculator mode, and diagnostic capability. Configuration options are available in choice of display, terminal, or printer transmission. The terminal is priced at $1095; combined with the terminal controller, a 6-position cluster can be purchased for $2062/position. **ICOT Corp**, 830 Maude Ave, PO Box 7248, Mountain View, CA 94039.
Circle 376

Full-size, high speed printer

Model EX1601 high speed printer combines speed with low maintenance. Printer offers 240 cps with full ASCII character set and 128 additional symbols. Interfaces include standard parallel, RS-232-C and 20-mA serial, or IEEE-488. The unit consists of 4 plug-in modules for servicing. Quantity discounts are available. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340.



Circle 377

Video display terminal

The WY-300 color VDT features an 8-color display, soft character generation, 2 RS-232 ports, and a plug-compatible mode for other ASCII terminals. Terminal can display data in red, green, blue, yellow, cyan, magenta, white, and black as either background or foreground colors. With soft character generation, the user can display italics, typesetting symbols, and line drawings. Ports have full-modem control at speeds of 19.2k bps and are compatible with the monochromatic WY-100. Terminal is priced at $975 in quantities of 100. **Wyse Technology**, 3040 N First St, San Jose, CA 95134.
Circle 378

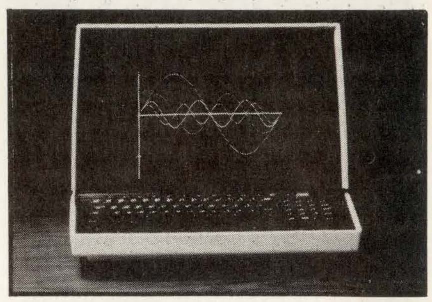
Smart display terminals

With the ability to handle functions that require host computer processing, models 915 and 924 VDTs have applications in data entry, information retrieval, and software development. Terminals' editing capabilities include line insert and delete. The 924 can also edit a full page. To facilitate offline editing, the 924 has 4 pages of memory; the 915 has 2 pages. Programmable function keys are available on the 924, in addition to a keyboard that can be reconfigured, a block and character graphics mode, and double-width characters. The 915 is priced at $695; the 924 is $895. **Televideo Systems, Inc,** 1170 Morse Ave, Sunnyvale, CA 94086.
Circle 379

High resolution terminal

The AED 1024 is a color graphics terminal with a 1024- x 768-pixel high resolution screen. Of the 16.8M colors offered, 256 can be simultaneously displayed while the character font set accommodates an 80 x 25 alphanumeric display format. Standard capabilities include 8 memory planes for layered designs and a bit-mapped mode to transfer images from host memory to terminal at the rate of 1M byte in 2 s. User definable symbols are also included. Terminal also has a 16-stage programmable zoom function. Price is $9995, including base and keyboard. **Advanced Electronics Design, Inc,** 440 Potrero Ave, Sunnyvale, CA 94068.
Circle 380

Graphics terminal



With dual processor speed, the GTC 224 color graphics terminal offers a Tektronix 4027-compatible graphics command language, up to 63K bytes of RAM, and a fully programmable keyboard with 32 function keys. Terminal provides a register of colors that can vary in hue, saturation, and lightness, plus a function that allows any of 8 (from a selection of 4096) colors to create a variety of patterns. Terminal also features 3-char sets; ASCII, and 2 user programmable sets with cell sizes up to 256 x 128 pixels. Price is $4900 in small OEM quantities. **Psitech,** 2842-C Walnut Ave, Tustin, CA 92680-7057.
Circle 381

Versatile ink jet printer

Silent printer Exxon 965 offers a variety of software driven fonts and characters. Std font selections include domestic, international, and scientific; users can access up to 8 fonts through keyboard commands from the model 500 workstation. Equations or special symbols are displayed as entered. Priced at $4400 for the basic unit, it operates at rates of 60 to 90 cps. **Exxon Office Systems Co,** 777 Long Ridge Rd, Stamford, CT 06923.

Circle 382

"Image processing has never been simpler...or more powerful"

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Discover a new world of image processing with our new Vision Two Series systems and CIPAL—Comtal's Image Processing Application Library. Together they provide all the capability of high-performance, hardware-based image processing at an entry level price. At another level, it contains a powerful 32-bit processor with Fortran to create your own programs, and features real-time, interactive operation. And, in between are hardware and software configurations to handle any image processing situation.

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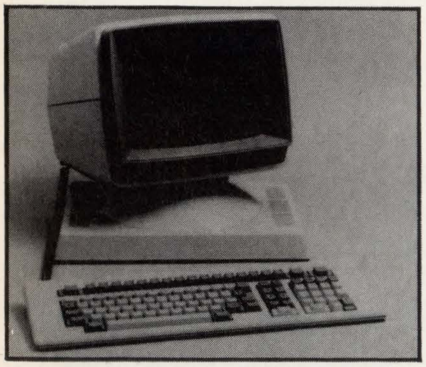
CIRCLE 129

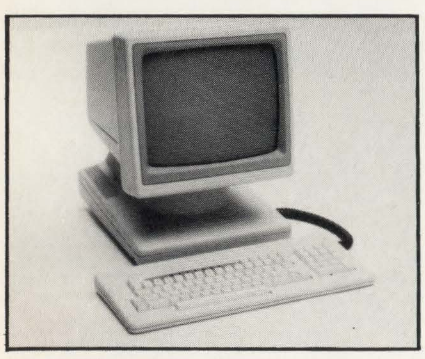
Video display terminal



The ADM 24E smart terminal provides a 48-line display memory with a 24-line window to scan it. The terminal includes 16 programmable function keys that can be shifted to perform 32 functions. It uses a nonglare green phosphor CRT with a tilt-and-swivel console and a low profile Selectric® type keyboard. Additional features include selectable international character sets, nonvolatile terminal setup from the keyboard, and full editing functions. The terminal is priced at $1250. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803. **Circle 383**

DEC-compatible terminal

The CIT-101e is a video display terminal featuring full DEC VT100 compatibility. The terminal conforms to European DIN stds and includes a 14" tilt-and-swivel screen and low profile keyboard. Video features include a 24-line x 80/132-character format, variable speed smooth scroll up to 2.4k baud, window erase, and split-screen operation. A 96-character ASCII subset and an alternate 128-character special set are both std. The terminal is single-unit priced at $1495 with OEM discounts available. **CIE Terminals Inc, Div of C. Itoh Electronics Inc,** 2505 McCabe Way, Irvine, CA 92714.



Circle 384

Portable teleprinter

Providing the user with a direct connect device for transmitting information, the Easywriter teleprinter uses a std telephone jack or built-in 300-baud acoustic adapter. A std feature is a typewriter keyboard to send and receive messages that can be stored for transmission at a later time. The teleprinter can auto-receive and print incoming messages without the presence of an operator—before, during, and after business hours. Model 18 TP is $1500 with a $24/month maintenance charge. The 300AA modem is $350 with a $5 monthly charge. **STC Systems, Inc, sub of Storage Technology Corp,** 4 North St, Waldwick, NJ 07463.
Circle 385

APL video terminal

Targeted for simulation, data analysis, and design engineering, the VT102 APL terminal allows APL to run on the VAX, DECsystem-10, and DECsystem-20. Also available is a field-installable kit to upgrade VT102 terminals to APL capabilities. Terminals are supplied with a keyboard that has APL characters on the front of the keycaps and std ASCII characters on the top. Users can switch between APL and ASCII modes from either the terminal or the host. The VT102 APL is priced at $2300; the upgrade kit is $895, min of 3 kits. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 386

Multipurpose terminal

For multi-database timesharing and dedicated, direct computer-connected applications, the APT terminal incorporates user friendly features. The terminal provides menu-controlled operation, programmable communication requirements, and a built-in, direct connect modem. A full-stroke keyboard and a flexible membrane keyboard are offered; both generate an audio tone. Terminals provide video output for either an 80- or 40-char, 24-line display. They also offer an rf output for a 40-char display on channel 3 or 4 of a std TV. Prices range from $399 to $598. **RCA MicroComputer Products,** New Holland Ave, Lancaster, PA 17604.
Circle 387

Impact printer

The NAP-24-I is a line of panel-mounted printers. They operate at 42 (24-col) lpm with a printer mechanism that has a MCBF of 500k operations. Characters are formed in a 5- x 7-dot matrix on plain paper; character set is the 96 ASCII. Input buffer allows printing while data are being received at speeds up to 9.6k baud. Features include selectable inverted printing, electronic end-of-paper sensing with a front panel LED indication, and a DTR (data terminal ready) signal. The printer is priced at $495 with an optional power supply (ac) at $60. **Keltron Corp,** 225 Crescent St, Waltham, MA 02154.
Circle 388

Intelligent terminal

The series 921 is an intelligent terminal that combines 3270 networking, personal computing, async terminal operations, and voice communications. It features a teleconferencing capability that allows interaction of voice and data on a single phone line. The Smart Button automates 16 computing or communications activities and allows access to functions with a single keystroke. Up to 9 controllers per system permit each installation to be configured for a single task or a variety of concurrently-run tasks. The series 921 is priced at $17,569 for a typ 5-station cluster including a shared IBM PC. **Davox Communications Corp,** 6 Continental Blvd, PO Box 328, Merrimack, NH 03054.

Circle 389

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CIRCLE 131

PC and small business printers

Multimode serial 18-pin printers from the Pinwriter series include 3 models—P1, P2, and P3, all with 180 cps. P2 and P3 also offer program or operator selectable dual-pass printing capability at 35 cps and an IBM PC interface or an optional RS-232. Prices range from $799 to $1250. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.
Circle 390

Letter/data printer

The Wenger 4/1 is a matrix printer offering correspondence quality at 110 cps, and data processing output at 400 cps. Character sets include national character, font and size programmable, and 96 USASCII. Text handling capabilities include left and right justify, underline, double intensity, and center text. Interfaces are RS-232, RS-422, Current Loop, and Centronics—all standard. Options are sheet feed, bar code generator, multicolor printing, and graphics. **Wenger Datentechnik,** Im Kägen 23/25, CH-4153 Reinach, Switzerland.
Circle 391

OCR reader

The OCR WAND® is an optical character reader with the option of 3 input devices: handheld reader module, slot reader, or a read-head module. The single-board reader controls baud rate, OCR font, magnetic stripe formats, error message, and application-dependent data editing and checking. Units can be designed with user requirements preprogrammed. Or, OEMs can configure new applications by using ROM programming equipment and a programming package. **Recognition Equipment Inc,** PO Box 222307, Dallas, TX 75222.
Circle 392

Letter-quality printer

The MT 180 printer is compatible with both 16-bit microcomputers (IBM PC, DEC Rainbow) and 8-bit microcomputers (Apple II, IIe, and Osborne). Combining letter-quality printing with 132-col, high speed printing, the device features both serial and parallel interfaces, a compressed printing option (264 cols on 1 line), a 160-cps rate for report and spread-sheet preparation, and a 40-cps rate for letter-quality printing. Right-hand justify, auto centering, print pitch, and proportional spacing can be programmed from the front panel or through the computer. Prices range from $998 to $1098. **Mannesmann Tally Corp,** 8301 S 180th St, Kent, WA 98032. **Circle 393**

DATA COMMUNICATIONS

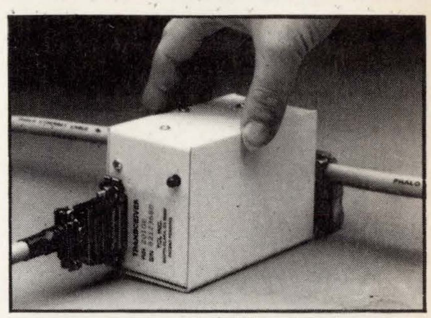
AC line carrier modem

The LCM400 series of modems are designed for transmission over ac power lines. The multichannel line carrier modem has the capability of networking up to 4 peripherals at 9.6k baud. Up to 300 peripherals can be used in communications networks by employing a reliable polling option. Compatible with standard 3-wire RS-232 protocol, the modem is full duplex and async. LCM400 list price ranges from $247 per pair for 50 to 99 pairs to $447 for 1 pair. **Communications Research Corp,** 1720 130th Ave, NE Bellevue, WA 98005.
Circle 394

SNA network processor

A graphics network processor, the SNA model 451, sends and receives EBCDIC or binary data in SNA networks with an SDLC protocol. Processor offers operator console support, duplicate character compression, and SNA standard interleaved communications for operation of multiple logical devices. System emulates IBM 3776 models 3 or 4 or the 3777 model 3 RJE workstation that allows software support. Communications in byte-parallel formats occur at speeds up to 350k bps, while RS-232-C interface offers a switch-selectable 2.4k, 4.8k, 9.6k, or 19.2k baud. Available 45 days ARO, the system is priced at $8500. **Versatec, a Xerox Co,** 2710 Walsh Ave, Santa Clara, CA 95051.
Circle 395

Ethernet transceiver kit



Operating at 1M, 4M, and 10M baud, the 2001E, 2004E, and 2010E LAN transceivers are small sized, lightweight, easy to install and meet Ethernet protocol. They measure 5.4 x 7.0 x 10.2 cm, weigh 9 oz, and allow single-tap installation without shutting down the entire system. Priced at $228 each in single-unit quantities (tap block included), transceivers have a 1-yr limited warranty. **TCL Inc,** 2066B Walsh Ave, Santa Clara, CA 95050. **Circle 396**

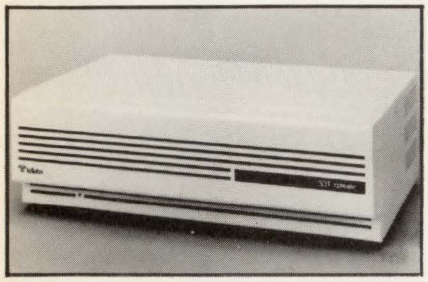
Intelligent comm controller

Allowing DEC LSI-11 users to interface to a variety of serial communications protocols, the COM-11 includes an onboard 16-bit microprocessor with 64K-byte RAM. The single PC board occupies 1 quad slot in the backplane, and has 4 full-duplex serial ports with modem control. Each port is programmable for async, bisync, or SDLC/HDLC operation. A set of program development tools is available to generate object code for the host system using MACRO-11 or a high level language. Single quantity prices start at $2995 with volume discounts available. **Tri-Dev Inc,** 7 Williams St, Medford, MA 02155. **Circle 397**

Interface MUXes

For high capacity trunks, the INSTATRUNK480i multiplexer has 128 channels on T1 communication link running at 1.544M bps. INSTAMUX470i plug-in multiplexer has 8 async channels and can be used for trunking over short distances and supporting local terminal clusters. The interfaces rely on firmware at $800 per port. INSTATRUNK480i is priced at $1500, while the INSTAMUX470i is $650 for 4 channel and $850 for 8 channel. **Micom Systems Inc.,** 20151 Nordhoff St, Chatsworth, CA 91311.
Circle 398

Switching stat MUX



A high performance mechanism for switching virtual circuits, the 331 data switching system offers port selection, group selection, and group password protection. The stat packet-switching MUX is designed for local and wide area distributed data networks and can function locally as a standalone port concentrator. In wide area applications, the MUX's topology allows support of 128 nodes, these can be joined in multilink frontend, remote-hub, and tandem-switch configurations. Extended network support package adds closed user groups, auto virtual circuit rerouting, and loadsharing over redundant data links. **Tellabs, Inc**, 4951 Indiana Ave, Lisle, IL 60532.

Circle 399

Protocol analyzer

The Interview 4600 interactive protocol analyzer provides flexibility by using a menu-driven system. System allows users to modify block check rules to fit protocols and has remote/program/data transfer to send or receive test programs or captured data samples. A library is available that stores up to 100 tests on a single tape minicartridge. Options exist at the link level for DECnet and at the packet level for X.25. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 400

Distributed communications processor

Functioning as a frontend processor, network processor, or remote concentrator, the DCP/10 has 3 main components: a processor, local storage, and communications line modules. The distributed communications processor interfaces to X.21 (circuit) and X.25 (packet) public data networks, has 512K bytes of error-correcting memory, and accommodates async, sync, and wideband transmissions at speeds of up to 64k bps. The DCP/10 may be purchased for $33,542 or leased for $768/month. **Sperry Corp, Computer Systems**, PO Box 500, Blue Bell, PA 19424.

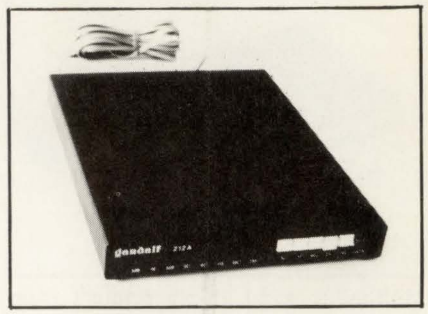
Circle 401

Ethernet chips

An Ethernet chip set includes the MB8795 data link controller and the MB502 Manchester encoder/decoder. With CMOS technology, the controller is configured in separate transmitter and receiver sections. Each section has a parallel interface port and provides sync buffering, byte parity checking, and parallel to serial conversions. The MB8795 also provides 4 modes of address recognition and a loopback feature for self-testing. The encoder/decoder offers low power, fast lock-on, and minimal jitter. Featuring both ECL and Schottky logic, the MB502 is available in a 24-pin std DIP. **Fujitsu Microelectronics, Inc**, 57 Wells Ave, Newton, MA 02159.

Circle 402

Auto-dialing modem

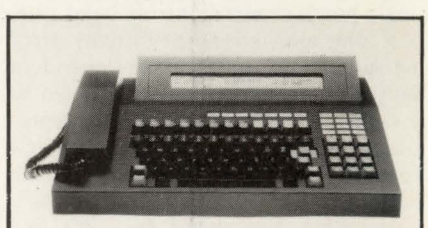


The SAM 212A is a Bell-compatible, FCC registered modem with an auto-dialer. Operating at both 300 bps (FSK) and 1.2k bps (DPSK) in full-duplex mode, the modem is also compatible with Bell 103/113 at 300 bps. Microprocessor based, the 212A offers speed control, transmitter timing, char length, auto-answer, and answer mode indication, all of which are set by the terminal operator. Providing last number dialed and loopback diagnostics, the modem sells for $618. **Gandalf Data Inc**, 1019 South Noel, Wheeling IL 60090.

Circle 403

Terminal combines phone and computer

An integrated telephone/computer terminal, the TelTerminal features a package that gives the user single key access to a complete array of communication and information capabilities. In addition to PBX telephone features, the terminal's processing abilities include a programmable financial and/or scientific calculator, calendar, and message center. The system is software compatible with the IBM PC and offers a module that can provide specific menu drivers, protocol and format needs, and transmission speed requirements when accessing proprietary data bases. **Digital Transactions, Inc**, 1033 Washington Blvd, Stamford, CT 06901.



Circle 404

AT DATRICON WE BELIEVE THE STD-BUS SHOULD FOSTER INNOVATION NOT STIFLE IT.

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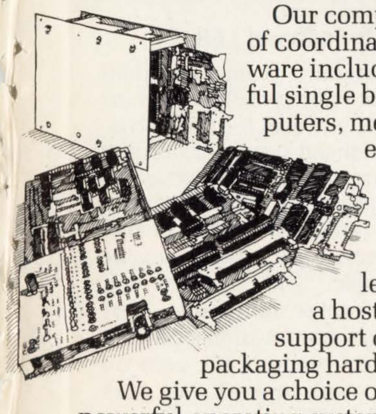

Our complete line of coordinated hardware includes powerful single board computers, memory expansion cards, and analog, serial and parallel I/O. Plus a host of system support cards and packaging hardware.

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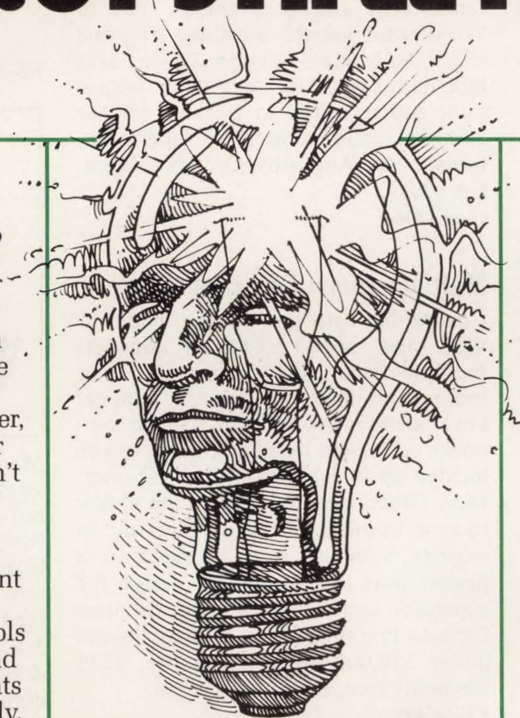

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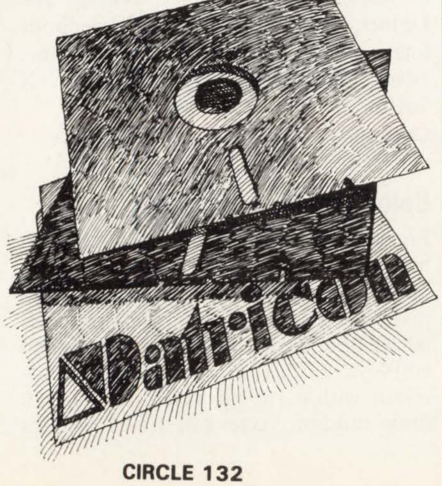

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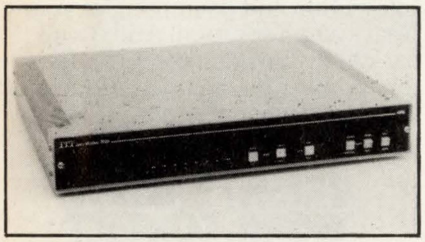
* OS-9, trademark of Microware

CIRCLE 132

Micro based modem

Designed for 4.8k-bps sync data transmission, the 2088 is a data modem with auto-dial backup control for unattended sites. An auto-adaptive equalizer provides a clear to send delay of 28 ms (18 ms on short links). In addition, a transmit delay of 11 ms gives a high throughput in polled multipoint networks. With diagnostic facilities, the microprocessor based modem offers a selectable transmission speed (to 2.4k bps) for severely degraded lines. **ITT Standard Radio & Telefon AB**, Box 501, S-162 15, Vällingby, Sweden.



Circle 405

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Cordially,

Bob Dromgoole

Robert P. Dromgoole
Circulation Director

High speed modem

A full duplex 1.2k-bps modem, the 212-LP is Bell 212A-compatible in high speed mode and performs sync to async and async to sync conversions. The modem has a 25-pin EIA-RS-232-C connector that provides data-to-terminal interfaces. User can program 9-, 10-, or 11-bit word lengths including stop and start bits. Modem provides 2 switches: a talk/data switch for data mode indication, and a switch to establish answer and originate modes of operation. **Inmac**, 2465 Augustine Dr, Santa Clara, CA 95051.
Circle 406

Multiple comm line connection

Compatible with DEC System 10 and 20, VAX, and PDP-11, ATTACH connects multiple communication lines to one or more computers. Up to 128 terminal lines can be connected with a single composite cable, and terminal clusters can be located up to 1 km from the host interface. Other features include the ability to support multiple host adapters and to reassign terminals. Also provided are a printer port and a modular design for expansion and repair. Domestic list price for a 64-line single host configuration is under $16,000. **Able Computer,** 1732 Reynolds Ave, Irvine, CA 92714.
Circle 407

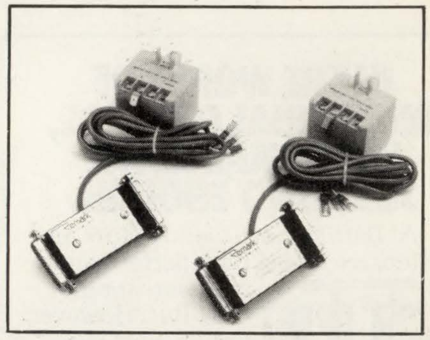
Telecommunications package

Omnilink 1200 consists of an Omnitec 300/1200-baud full-duplex modem (model 5212), telecommunications card, and Softlink software. Designed to turn the Apple II, Apple II+, and Apple IIe into high speed intelligent terminals, the package requires 48K RAM, one disk drive, and a monitor. Async serial format is compatible with packet switching networks such as Tymnet, Telenet, and Uninet, as well as regular telephone lines. **Texas Microdata Systems, Inc,** 1414 Texas Bldg, Fort Worth, TX 76102.
Circle 408

Color graphics controller

For use with 100-MHz video bandwidth high resolution color monitors, the Ω500 display controller supports 1280 x 1024 pixel screen resolution and provides 60 Hz noninterlaced refresh. The system employs a custom bit-slice microprocessor with a 167-ns cycle time that can draw random vectors at 1.5-M pixels/s and fill rectangles at 35-M pixels/s. Controller has self diagnostics and a built-in signature analyzer with options in communications interface and tablet graphics input. **Metheus Corp,** PO Box 1049, Hillsboro, OR 97123.
Circle 409

RS-232 to RS-422 converters



Models 63-3S and 63-4S are a series of RS-232 to RS-422 converters. Each model is self-powered via a wall-mounted transformer and internal regulation circuitry. Signals on the RS-232 connector swing over the range of ±11 V while the differential signals are in the range of 0 to 5 V. Converters also act as modems designed to transmit and receive full duplex data at 100k baud up to 4k ' over 2 twisted pairs. Each unit includes an 8 ' line cord and a transformer and sells for $126 in singles and $99 each in 100s. **Remark Datacom Inc,** 4 Sycamore Dr, Woodbury, NY 11797.
Circle 410

High speed broadband LAN

Providing integrated communications capabilities, the VIDEODATA® LAN/I offers a token-passing protocol for traffic control. As a broadband system, it operates as a logical ring or circular message network. Microprocessor based network interface units (NIUs) connect the communicating elements on the system to the broadband cable. The interface unit handles data packet formatting, port contention, and transmission acknowledgment. System supports 10k users on 5-channel pairs with network data rates up to 2.5M bps. The system supports both sync and async devices and yields a $360 per port connection cost with 8-port NIUs. **3M,** Dept BC83-121, PO Box 33600, St Paul, MN 55133.
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Power distribution systems
Booklet offers technical diagrams, application drawings, and product spec charts for Guardsman, Isoshield®, and Isoreg®. Typical problems in unfiltered utility power, use of surge suppressors and dedicated power lines, and alternatives to modular power distribution systems are reviewed. **Isoreg Corp,** Littleton, Mass.
Circle 431

Single-chip microcomputers
Pamphlet gives functional block diagrams, pin descriptions and configurations, device operating characteristics, and electrical specs for NCR 6500/1 and 6500/1E. **NCR Corp,** Dayton, Ohio.
Circle 432

OS/VS COBOL workstation
Tear sheet lists general features, programming and system tools, and product specs of 1116 workstation for writing, editing, compiling, testing, documenting, and maintaining programs independently of a mainframe computer. **SOLOSystems, Inc,** Sunnyvale, Calif.
Circle 412

In-circuit system analyzer
Interactive analyzer for 6502 software development and test is outlined in tear sheet relating general features, specs, and application diagram. **DA-TECH Corp,** Ivyland, Pa.
Circle 413

Protocol monitor/simulator
Pamphlet discusses model 1600 features, summarizing specs, communications parameters, operational modes, and data display/memory capacity. **Dynatech Data Systems,** Springfield, Va.
Circle 414

Printer character set supplements
Catalog gives samples of over 80 daisy wheel and thimble print elements from Qume, Diablo, and NEC, as well as Xerox compatible units. **Misco Inc,** Marlboro, NJ.
Circle 415

Magnetic components
Basic facts on switch mode magnetics, inductors, and transformers detail product descriptions; design worksheets help specify standard and custom items. **Dale Electronics, Inc,** Columbus, Neb.
Circle 416

Dot-matrix impact printers
Catalog covers complete functional specs, operating characteristics, dimensions, features, and ordering information for printers, print mechanisms, and printheads. **Eaton Corp, Count Control/Systems Div,** Watertown, Wis.
Circle 417

DC servo controllers
Leaflet gives overview of NC400 series plug-in dc PWM units; photos, diagrams, and spec tables describe and illustrate features, options, and technology. **Contraves, Motion Control Div,** Pittsburgh, Pa.
Circle 418

Assembly robot
Technical bulletin highlights ERMAC® (electrically reprogrammable modular automated component) series 26; complete technical and dimensional specs are given for robot, controller, and handheld programmer. **Everett/Charles Automation Systems Inc,** Pomona, Calif.
Circle 419

Data comm analyzer
Brochure covers menu-driven interactive programming capabilities, EEPROM, CRC/LRC, buffer transfer, and built-in interface breakout; it also illustrates representative screen formats. **Digilog, Network Control Div,** Montgomeryville, Pa.
Circle 420

Wire and cable
Reference guide to wires, braids, and cables provides tables for full characteristics and specs, along with charts for attenuation and comparative properties of plastic insulation and conductor coatings. **Vertex Electronics, Inc,** Farmingdale, NY.
Circle 421

Packet network data concentrator
Data sheet describes Microplexer® X.25 packet assembler/disassembler with stat MUX; features, specs, configurations, and CCITT recommendations are examined. **Timeplex, Inc,** Woodcliff Lake, NJ.
Circle 422

Communications measurement
Brochure gives overview of telecommunications, lab, and operational test and measurement sets, with brief description and photo of each. **Tau-tron Inc, unit of General Signal,** Chelmsford, Mass.
Circle 423

Printed circuit tester modules
Data manual discusses features, operation, programming, electrical specs, and options for PIC series, which test application programs before they are committed to a masked ROM. **General Instrument Corp, Microelectronics Div,** Hicksville, NY.
Circle 424

Shielded terminals and keyboards
Leaflet illustrates and describes emi/rfi protected structural foam CRT enclosures and keyboards; engineering drawings and photos complement text. **Bud Industries, Inc,** Willoughby, Ohio.
Circle 425

Stepping switches
Background on engineering considerations, rotary switch and forward drive operation, and basic control circuits leads into catalog of stock and custom designs; complete specs, dimensional diagrams, and load circuit decks are shown. **Ledex Inc,** Vandalia, Ohio.
Circle 426

Capacitive DIN keyboard
Data sheet introduces low profile, high performance full-travel keyboard, examining standard features, options, applications, and dimensional diagram with switch specs. **Digitran Co, Keyboard Div,** Pasadena, Calif.
Circle 427

Data concentrator/stat MUXes
Catalog details low-cost stock line that allows 2, 4, or 8 terminals to share a telephone line; concentrator's composite output rate can be 9.6k, 1.8k, or 1.2k bps, sync or async. **Black Box Catalog,** Pittsburgh, Pa.
Circle 428

X.25 data concentrator
Tutorial summarizes CCITT recommendation X.25, packet switching concept, and role of packet assembler/disassembler (PAD), then describes Micro800/X.25 PAD features, specs, applications, and network configurations. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 429

Linear and switching power
Catalog details 100- to 400-W supplies with accessories and options, listing specs and voltage/current ratings for various output configurations; photos and dimensional drawings for each size are included. **Deltron Inc,** North Wales, Pa.
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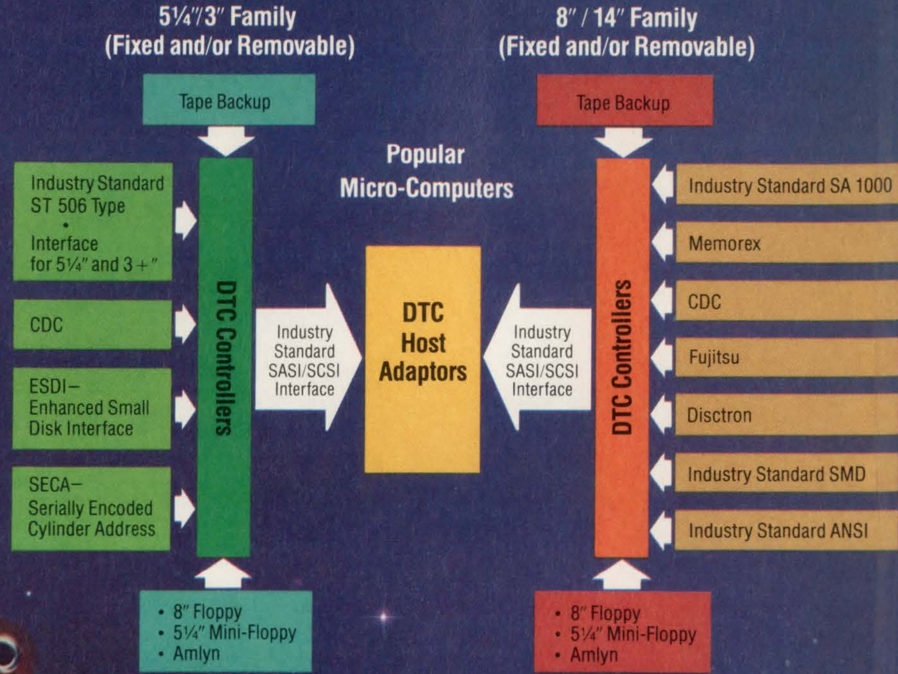

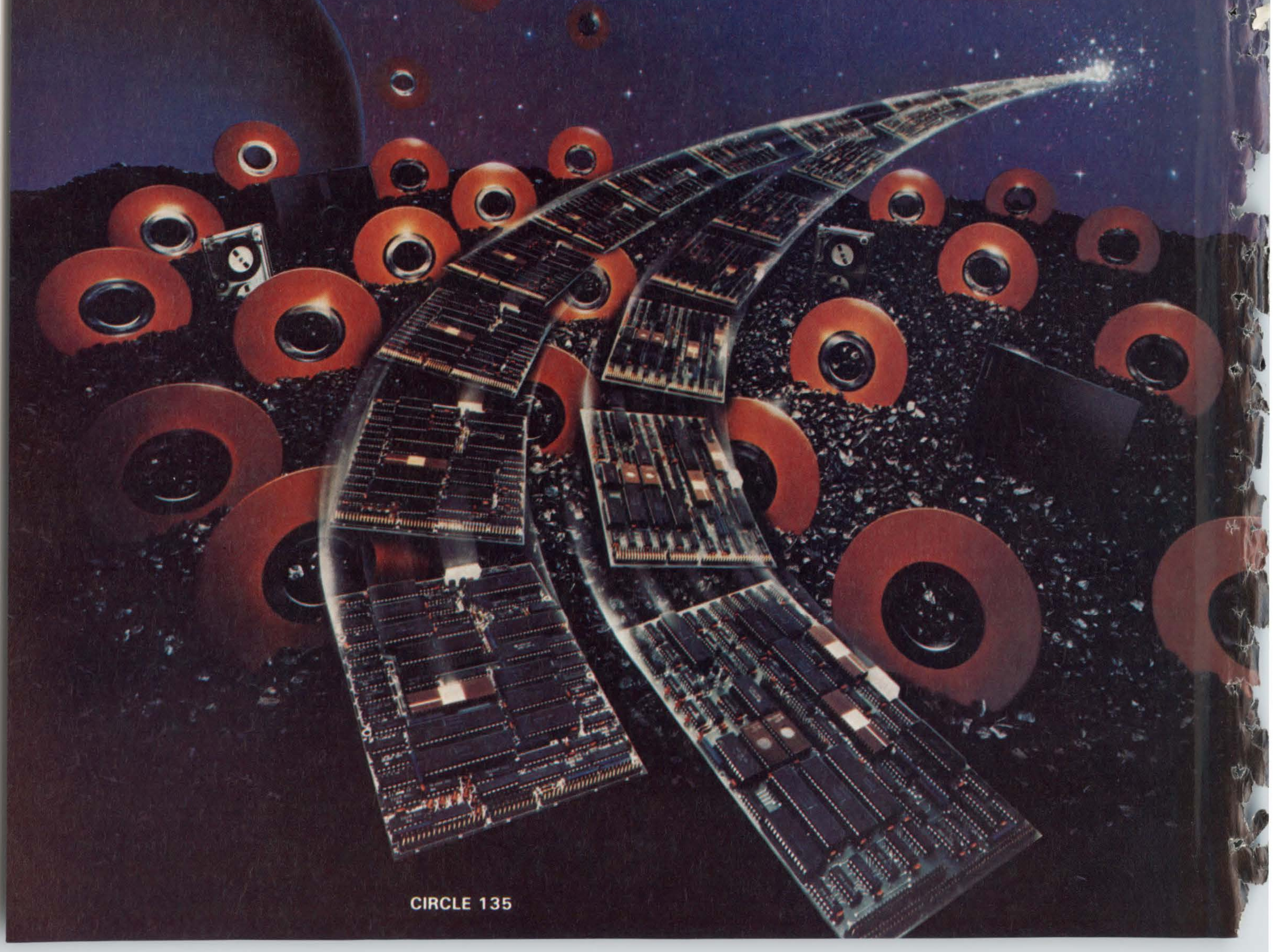

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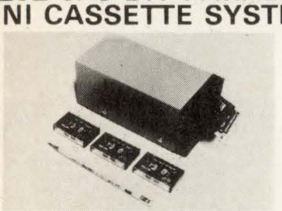

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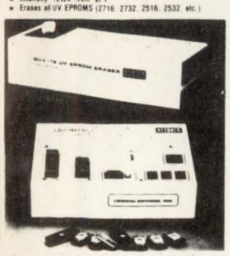

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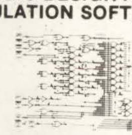
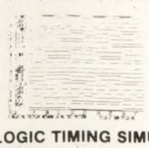


MICRO-LOGIC DIAGRAM



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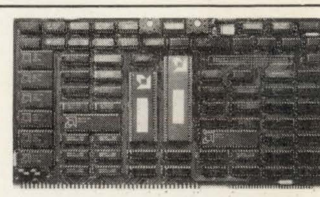

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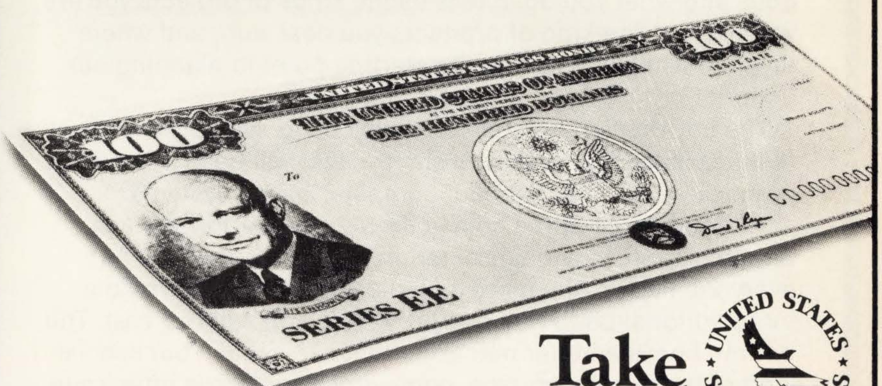

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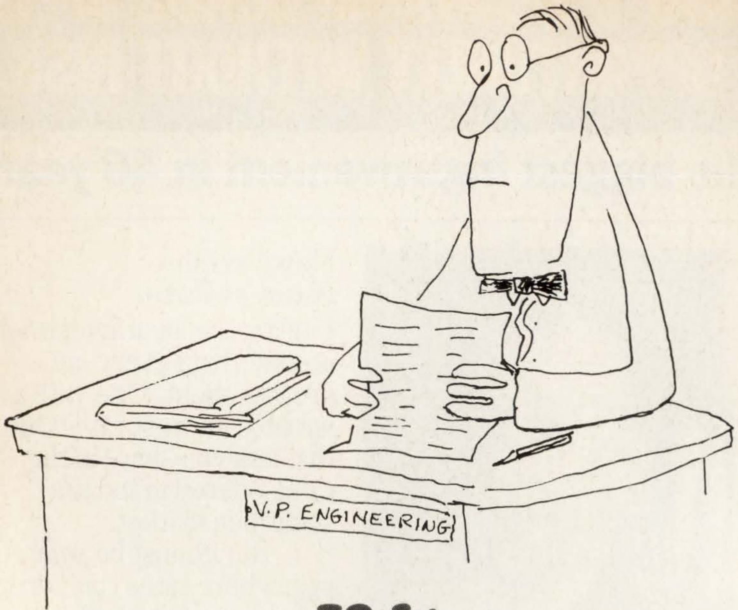

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