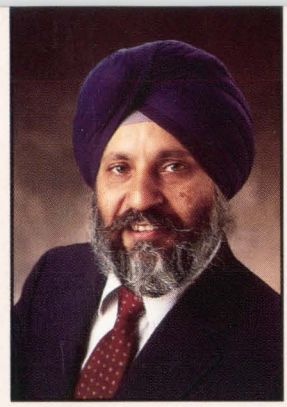

Inder Singh on Posix

A PENNWELL PUBLICATION MARCH 1, 1991

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

Fuzzy logic simplifies complex control problems

Many barriers slow quest for single-chip ethernet adapter

Are mixed cells and arrays the solution ASIC vendors claim?

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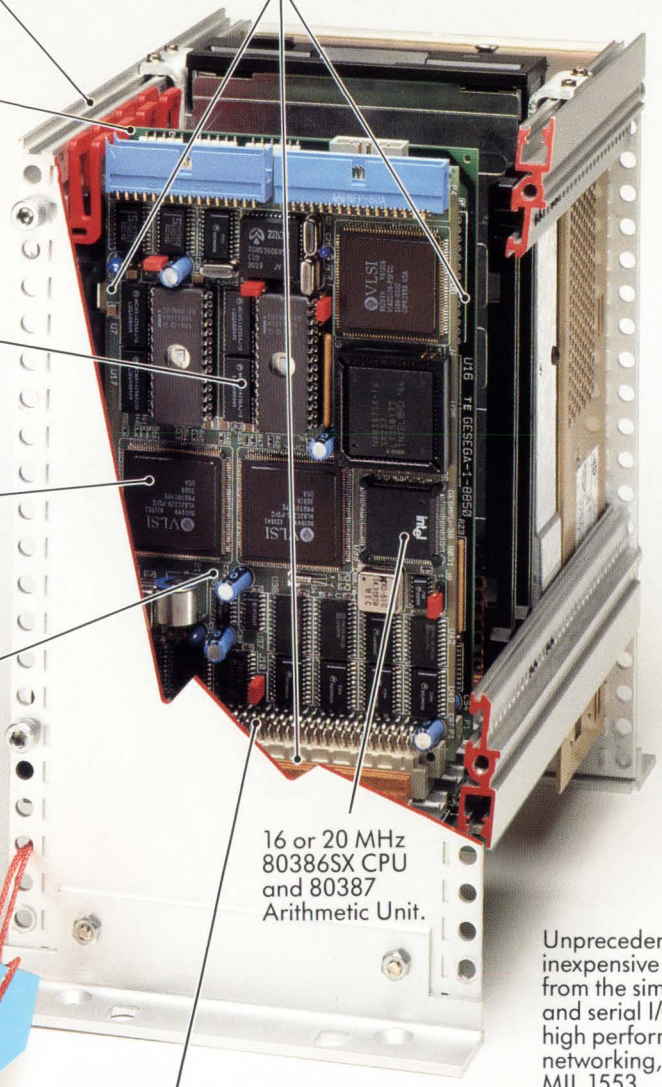

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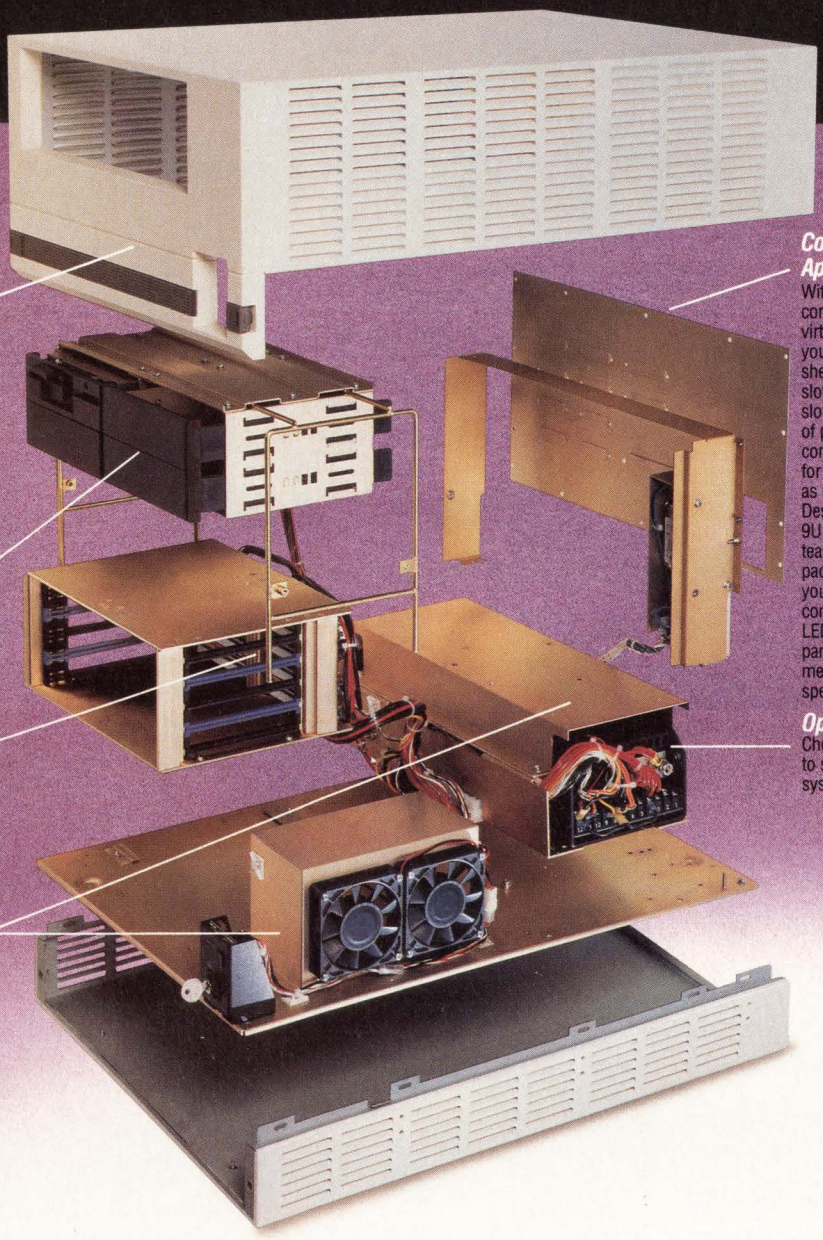
CIRCLE NO. 1

O M E G A

New



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CIRCLE NO. 3

VOL. 30, NO. 5 MARCH 1, 1991

COMPUTER DESIGN

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Inder Singh on Posix
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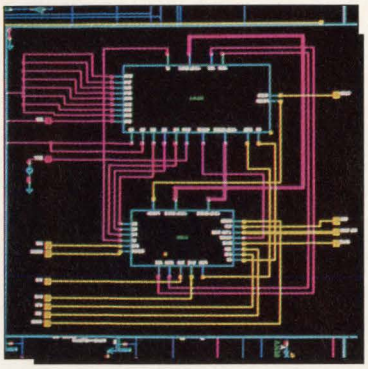

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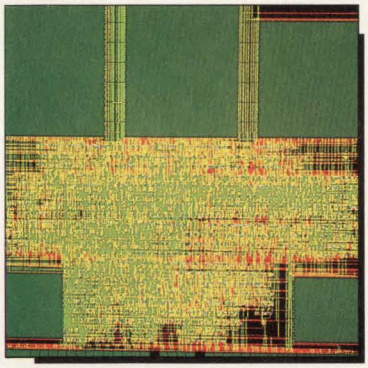

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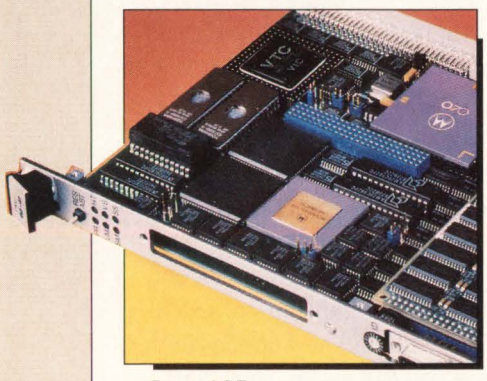
COVER STORY

Fuzzy logic simplifies complex control problems

Fuzzy logic is proving a powerful methodology for control applications. Over 2,000 patents have been issued in Japan. Now, development tools and hardware are becoming available in the United States, and application possibilities abound 90



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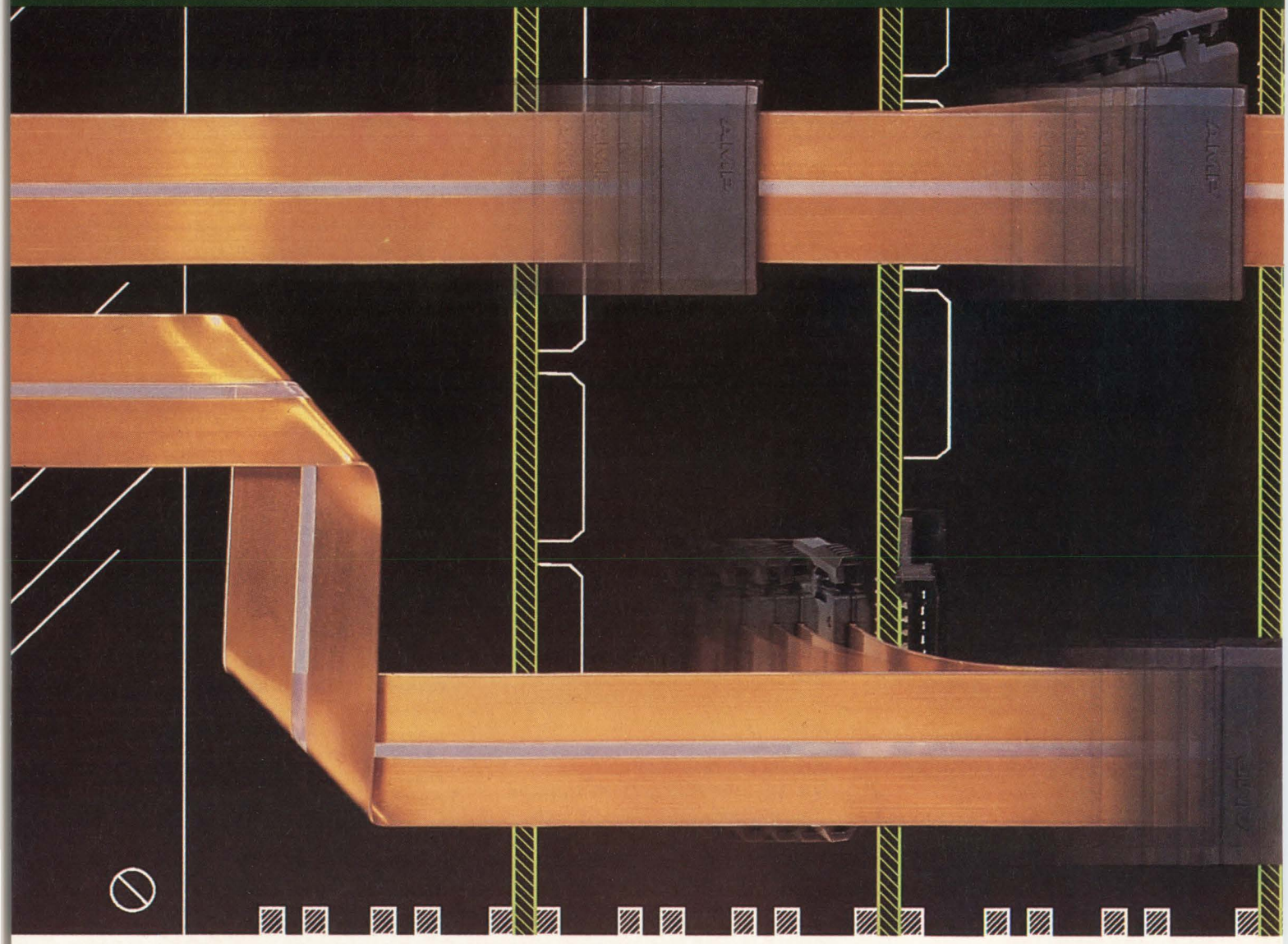
Putting high-performance power distribution on the fast track.



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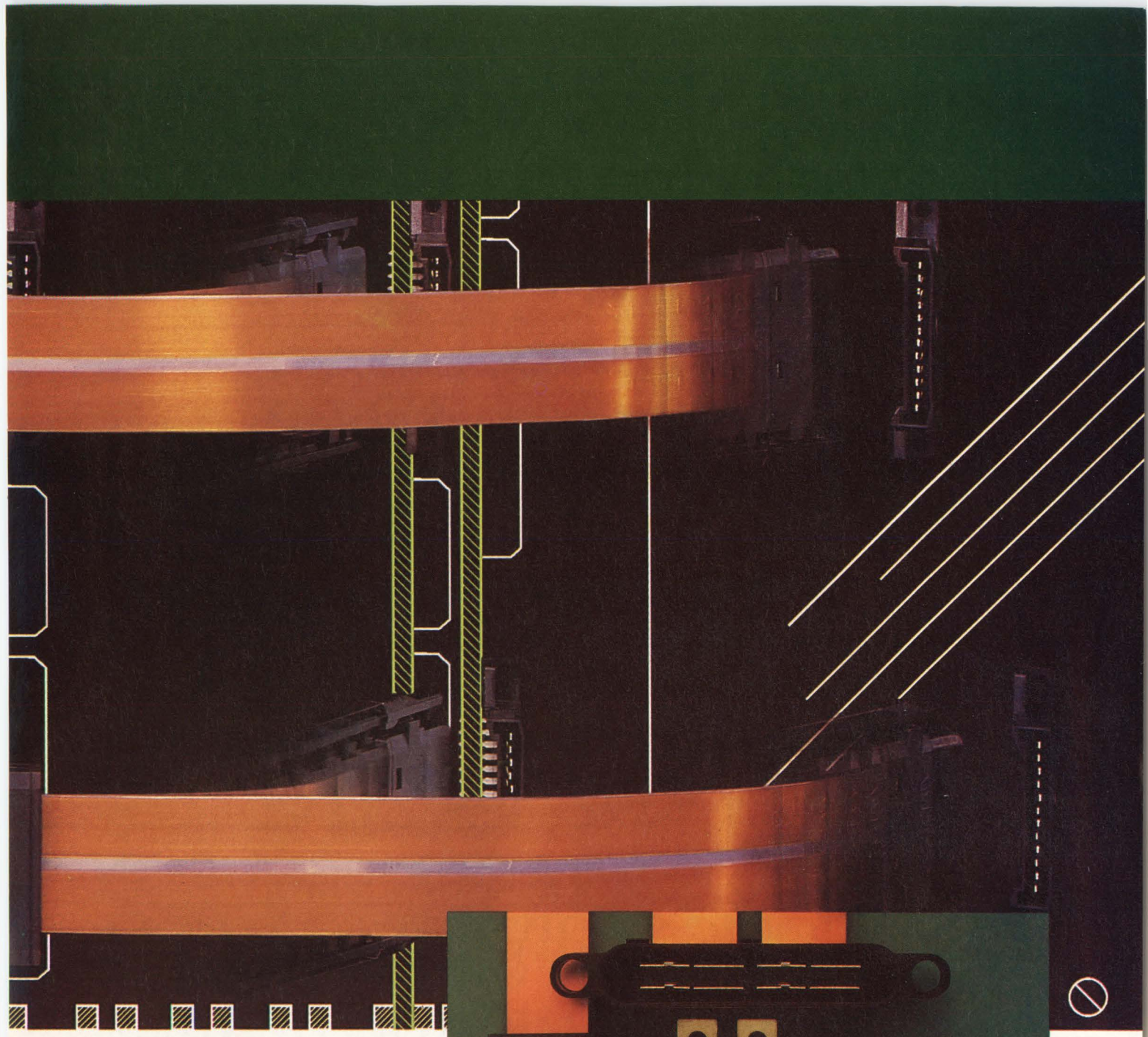

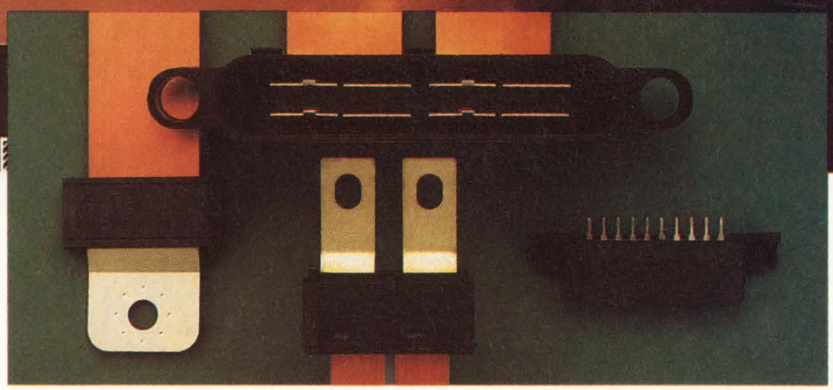

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A basic comparison: Record all state and timing data on an 8-bit microprocessor with multiplexed bus, 8-bits for address, 3 control signals and a clock.	HP 1654B	Tek PRISM/MPM	Philips PM 3580/30
Probing: Channels used	48[1]	48[2]	20
One connection	No	No	Yes
Setups	Two	Two+	One
Interfaces to learn	Two	Two+	One
Integrated state & timing triggering	No, only one arming condition	No, only indirect 4-bit Teklink	Yes, 8 levels
State & timing data per pin	No	No	Yes
Price	$6700	$8600	$4250

Footnotes: 1) 8 channels lost to de-multiplexing
2) De-multiplexing requires double probing and only nine high-speed channels on basic unit

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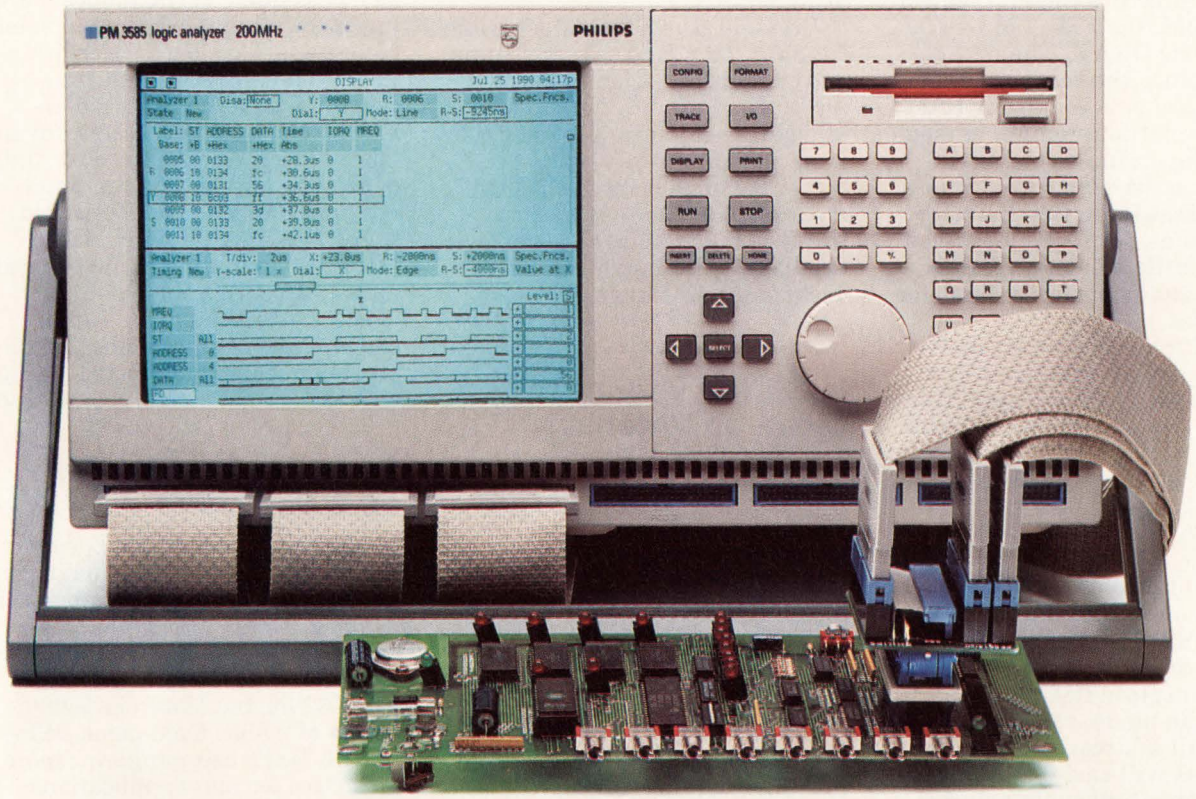

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FAST ANSWERS.

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CIRCLE NO. 5

Ramtron manufactures ferroelectric DRAM

Ramtron (Colorado Springs, CO) has combined breakthroughs in ferroelectric materials, electronic design, and processing to successfully manufacture the first nonvolatile DRAM, the FMx 1208 4-kbit ferroelectric DRAM. The new device combines the read/write characteristics of semiconductor RAM with nonvolatile retention of magnetic storage. And ferroelectric DRAMs can be used throughout a system because they consolidate the functions normally performed by nonvolatile memory, volatile memory, and nonvolatile data storage devices.

The 1208 uses a two-transistor, two-capacitor memory cell structure and has two operating modes: dynamic and nonvolatile. In the dynamic mode, the memory uses the high linear dielectric constant of its ferroelectric cells to store data as an electrical charge, and read/write endurance is unlimited. In this mode, the 1208 operates as a nonmultiplexed DRAM and requires, like a conventional DRAM, periodic refresh to retain data. But in the nonvolatile mode, refresh operations to all addresses prior to a power loss will cause an applied pulse to spontaneously polarize the ferroelectric cell, thereby retaining data for a minimum of one year without power.

The 1208 evaluation vehicle is available on a single-board development system. Ramtron is also expanding its technology to high-density memory products and ASICs through strategic alliances. *—Barbara Tuck*

Process could boost optical disk capacity

Researchers at Advanced Technology Materials (New Milford, CT) have discovered a new method for growing high-quality thin films of barium titanate, a nonlinear optical material used in optics research. The method promises to halve the cost of the optical-frequency doublers used in optical disk applications. With the new process, optics researchers can incorporate high-quality thin films of barium titanate in high-speed parallel optical processing designs.

Crystals grown from the barium titanate compound take the 1-μm wavelength radiation from commercially available diode lasers and generate a strong, second harmonic signal in the visible spectrum. The higher-frequency light makes it possible to store four times as much information on optical disks, according to Advanced Technology Materials. *—Jeffrey Child*

Is '91 the year of the cache on VMEbus?

The year 1991 is the "year of the cache," predicts Ray Alderman, technical director of the VFEA International Trade Association (Scottsdale, AZ). Cache—or more precisely, cache coherency—has been one of the major buzzwords of Futurebus+, and the cache-coherency fever seems to be spreading. At Buscon/91-West, attendees of the VITA technical committee meeting were treated to a surprise suggestion that a cache-coherency mechanism be added to VMEbus.

Not all the merits of this scheme are clear, however. One advantage is that it would permit VME to map into Futurebus+ far more easily than the current scheme calls for. But outside of simplifying the bridge, the advantages may or may not outweigh the disadvantages.

First, the VITA technical committee is considering adding the cache-coherency mechanism to revision D of the VME64 specification before it's ratified and approved by the IEEE. This would effectively delay final approval of the VME64 spec. In addition, it's not clear at this time how the cache-coherency mechanism will work, or what will have to be sacrificed (in terms of pins, and so forth) to implement it.

Finally, there has been no great clamor for the capability. Like the 64-bit addressing capability of VME64, will cache coherency be something that no one uses? And will implementation of the spec call for a new generation of interface silicon?

The answers will become clear as more details of the proposal are unveiled. While VME may in some respects be too slow to use with a fully cache-coherent multiprocessor system, the proposed enhancement may bring some advantages to specific applications. And, depending on how a cache-coherency mechanism is implemented, it may also be useful for tasks other than updating caches. For example, it conceivably could be used as a technique for rapidly exchanging messages, once and for all standardizing message passing on VME. *—Warren Andrews*

Real-time kernel runs on a DSP chip

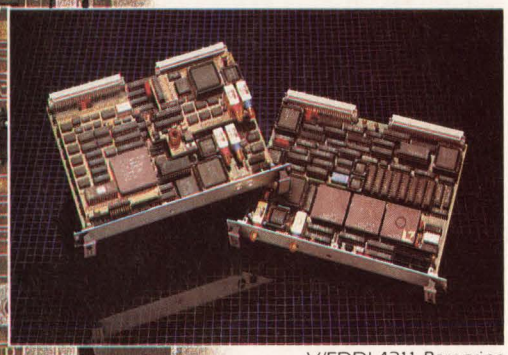
In what may be the first port of a mainstream commercial real-time kernel to a digital signal processor, Ready Systems (Sunnyvale, CA) and Motorola (Tempe, AZ) have announced the availability of VRTX32 for the Motorola 56000 family of 24-bit, fixed-point DSPs.

With DSPs becoming ever more attractive for mass applications such as multimedia, voice and video compression, there's an increasing need for standard operating system interfaces. VRTX32 makes it possible for applications written in C for VRTX on standard microprocessors to be ported to the 56000.

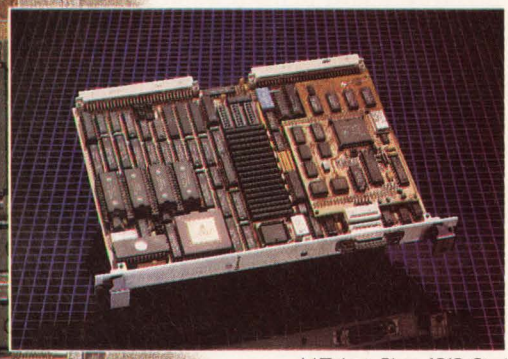
Development environments for the 56000 are already in place. VRTX32/DSP56000 is available for personal-computer or Sun host platforms. Motorola provides an application development system board, a C compiler, assemblers, emulators, and a software simulator that run on PCs, Macintoshes, and Sun-3 workstations. In addition, Ariel (Highland Park, NJ) offers a development board for the Sparcstation, to which VRTX has been ported, as well as an SBus card. *—Tom Williams*

Continued on page 10

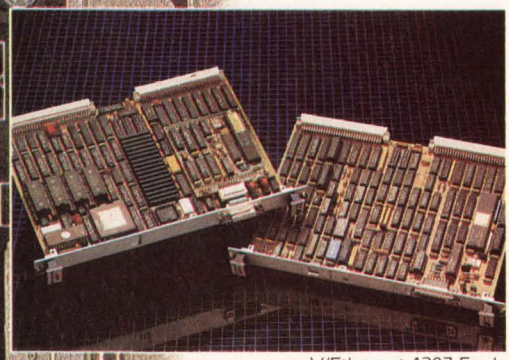
NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
V/Ethernet 3207 Hawk

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The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face. Interphase delivers those solutions.

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PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

ETHERNET CHOICES

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

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CIRCLE NO. 6

NEWS BRIEFS NEWS BRIEFS NEWS BRIEFS NEWS BRIEF

Continued from page 8

National standardizes on Silvar-Lisco tool

Intensive efforts by Silvar-Lisco (Sunnyvale, CA) to promote its two-to-N-layer-metal SL-Series of layout and analysis tools for gate arrays and cell-based designs appear to be paying off. National Semiconductor (Santa Clara, CA) has adopted the Silvar-Lisco SL-Array product as a standard for all National gate array products. With its hierarchical placement and linear routing algorithms, SL-Array addresses critical-path technology in arrays of up to 300,000 gates.

National's design automation director, Roy McGuffin, points to the "technical superiority of SL-Array" and "Silvar-Lisco's excellent customer service" as reasons for standardizing on the software and integrating it into National's DA4 design automation system. SL-Array reportedly has no problem accommodating the SRAMs embedded on National's new arrays.

Silvar-Lisco's SL-Array has a long way to go before it catches up with the industry's mainstay in gate array layout, Gate Ensemble from Cadence Design Systems (San Jose, CA). The tight coupling of the Cadence software to the company's other framework-based tools presents an argument in its favor before the user even does a performance comparison. The same holds true for the recently introduced Parade place-and-route software that Mentor Graphics (Wilsonville, OR) has integrated into its framework-based toolset.

—Barbara Tuck

IBM unlocks door to minilaser production

Scientists at an IBM research laboratory (Zurich, Switzerland) have developed a way to build as many as 20,000 lasers—each only a fraction of an inch long—on a semiconductor wafer just 2 in. across. According to IBM, it's the first time scientists have been able to both mass-produce and test semiconductor lasers on a complete wafer. Such lasers are now used in CD players, laser printers and fiberoptic transmission.

IBM scientists expect the new method, called full wafer technology, to be faster, some 50 percent cheaper and result in a much higher percentage of working lasers per wafer. The advancement also holds substantial promise for integration of the lasers, which range in length from 1/32 in. to 1/64 in., with other electronic components on "optoelectronic" chips that use both light and electric current to carry information.

—Mike Donlin

SBus off and running

SBus got another shot in the arm last month when Motorola (Tempe, AZ) announced plans for using the bus as a mezzanine bus in its Futurebus+ products. Though Motorola had previously endorsed Futurebus+ publicly, the company hadn't announced any product or product family based on the bus. Motorola's decision to back SBus provides yet another critical endorsement helping SBus on its way to becoming the high-performance I/O bus of choice for next-generation workstation products.

To keep pace in the commercial computer business, Motorola will have to go a step or two beyond what's available—or possible—on VME. Since the firm has already endorsed Futurebus+, that approach would be the most logical one for its server-based systems. But where will all the I/O come from? With its VMEbus-based systems, there are catalogs full of VME I/O cards, but that's not the case with Futurebus+. And if Motorola uses a 6U×160-mm form factor (the same as VME) for its Futurebus+ product line, as Motorola Computer Group vice-president Tom Beaver has hinted, there will be no readily available I/O to draw on.

Furthermore, Motorola has never developed its own mezzanine bus, as have some 20-odd other VME board makers. Motorola's move to take advantage of the already large base of SBus vendors (now topping the 140 mark) makes a lot of sense. SBus will do exactly what a standard bus is supposed to do—provide an industry-standard architecture to give OEMs and users more flexibility at a low cost while greatly speeding time-to-market. Motorola's decision to back SBus will probably shave as much as a year off the company's ability to get a complete Futurebus+ product to market.

—Warren Andrews

Intel launches review effort for compatibility

Bringing together a group of key industry representatives, Intel (Santa Clara, CA) has set up a review board to ensure the compatibility of binary applications across open-system software platforms targeted for 386- and 486-based hardware platforms. The first item on the board's agenda is the second edition of Intel's 386 Architecture Binary Compatibility Specification (iBCS-2).

With Intel acting as a neutral party in resolving any conflicts, the review board consists of four independent software vendors in the CAD, office automation, database, and graphics areas. OEM representatives involved include customers from Santa Cruz Operations, AT&T Unix Systems Laboratories, Open Software Foundation, and Interactive Systems. Also in the group is one end-user representative from the User Alliance of Open Systems.

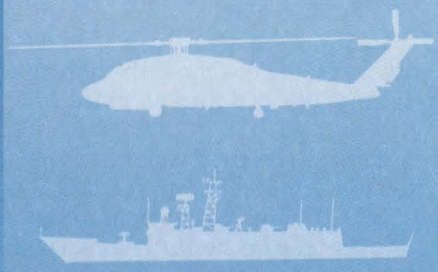
Following the review of the iBCS-2 draft, the group will submit review comments for consideration by Intel prior to publishing the approved specification. A draft of the iBCS-2 will be available March 15. Intel plans to publish a final version in May.

—Jeffrey Child

DY 4 VME

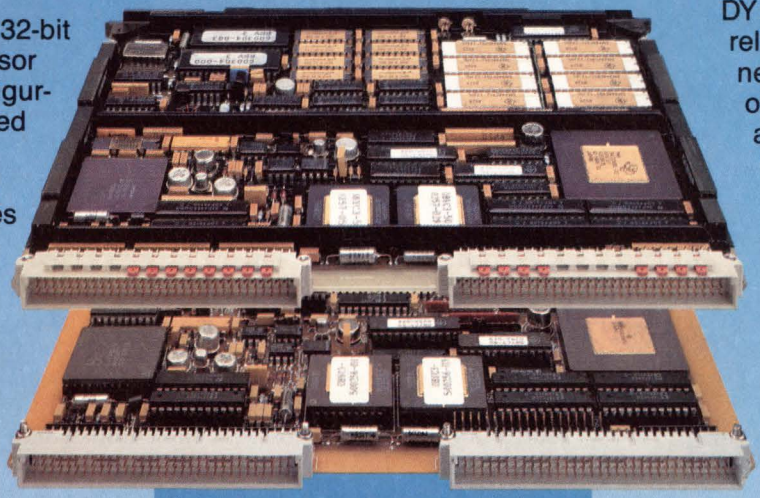
When you must win!

NEW!



GRAPHICS CONTROLLER

Conduction-cooled and air-cooled versions for military/aerospace applications:



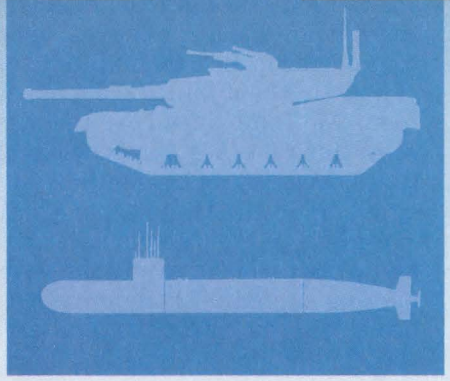
☑ High performance 32-bit Graphics System Processor (TMS34020) can be configured to operate in host-based or stand-alone system. Operates at 32 MHz rate, achieving instruction rates of up to 8 MIPS.

☑ Modular Graphics Engine (MGEbus) interface allows two Graphic Controllers to operate in parallel with double performance and more bit planes.

☑ Multiple video display formats from 480×480 to 1280×1024. From one to four buffers depending on format.

☑ Composite video input accepted from remote video (e.g. image sensor). Video output port supports display of superimposed locally generated graphics on video input.

☑ RGB video output port for color graphics display applications.



Ready-to-run VMEbus systems from DY 4 are selected overwhelmingly by systems integrators for aerospace and defense programs world-wide.

DY 4 provides performance, reliability and cost effectiveness through a full range of NDI VMEbus products and services to military, rugged and commercial standards.

DY 4's system solutions incorporate Ada™ board support packages (configured Ada run-time environment), drivers, and diagnostics.

DY 4 provides a comprehensive quality program to MIL-Q-9858A and configuration management to MIL-STD-483; design procedures to MIL-STD-1521; manufacturing quality control to MIL-I-45608 and soldering to MIL-STD-2000 in an ESD-controlled environment.

Ada is a trademark of the United States Department of Defense

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Tel: (603) 595-2400
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Tel: +61-2-484-6314
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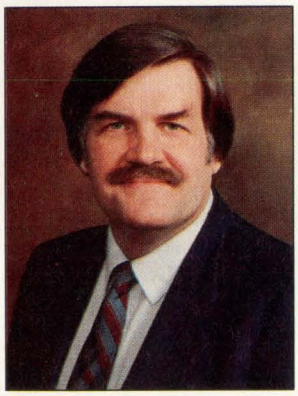
CIRCLE NO. 7

Will we now learn from our own example?

If we can make effective electronic weapons, why are foreign competitors beating us in commercial markets?



John C. Miklosz
Associate Publisher/
Editor-in-Chief

Along with all of the anguish surrounding the Persian Gulf war, there's also a flush of high-tech euphoria. It's hard to resist the urge to root for a Patriot missile making a kill, or to remain calm when watching a video image of a laser-guided bomb being directed with incredible precision.

This is the first time that the general public has been exposed to this broad a sampling of U.S. high-tech weaponry, and everyone seems to have gone gaga, including more than a few radio and television commentators. With such a public display of potent high tech (barring the failures that the Pentagon may be keeping from view), an obvious question has popped up—if we can make such fantastic and effective electronic weaponry, why are foreign competitors beating us in key electronics and computer markets? It would be an interesting question if the answers weren't obvious.

First, military systems aren't price-sensitive. We, or rather, the Pentagon and Congress, have been prepared to pay whatever the high-tech systems have cost, barring utterly dismal performance (the Sargent York gun, for example) or a galactically outrageous price (the B1 stealth bomber, for example, which would have cost, literally, its weight in gold).

Second, the R&D of military systems is fully subsidized. A large amount of R&D at universities and government laboratories is subsidized directly, and the R&D done by contractors building systems is ultimately built into the price when it's not supported directly.

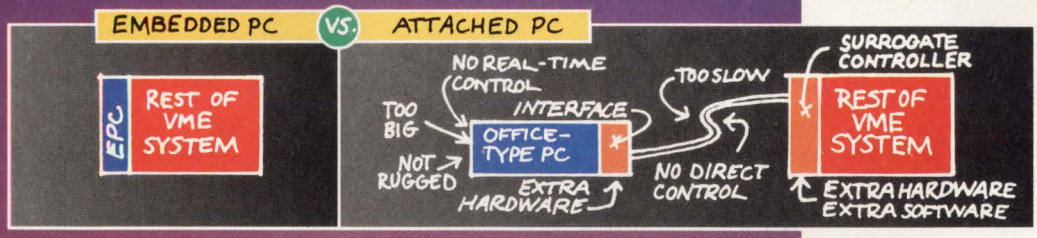
Third, the procurement of military systems has required a long-term commitment. While it's true that military systems are subject to annual budget review, the chances of a project being killed in midstream have traditionally been small. It took years to kill the Sargent York gun, for example; and the "hero" of the gulf war, the Patriot missile, went into service years ago. Compared to the consumer market, the military systems market is quite stable.

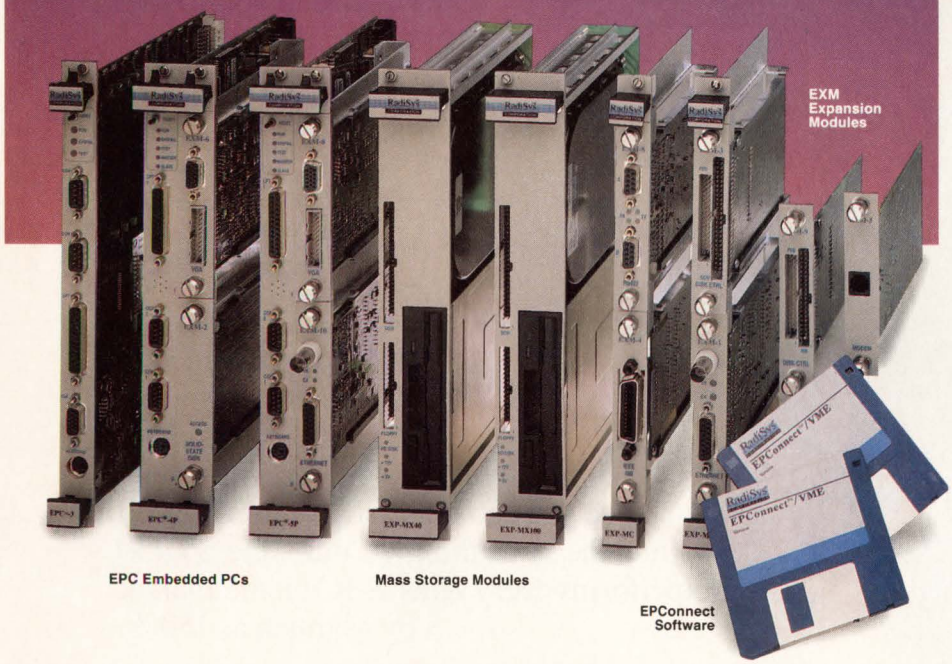
Fourth, the military systems market is a protected market. U.S. high-tech companies have the market to themselves—and rightly so in this case. We may now be relying on components manufactured overseas, but essentially all of the systems and subsystems suppliers in the United States have had the field to themselves.

A protected market, long-term commitment, subsidized R&D, and price insensitivity. Along with the genius, innovation and engineering skills that U.S. universities, laboratories and industry brought to the party, these other factors essentially guaranteed the kind of high-tech performance we've been seeing. The question we now have to answer is, what mix of the three bulwarks of our military systems development—a protected market, long-term commitment, and subsidized R&D—should we bring to bear on the battlefield of commercial competition?

Our competitors have used all these factors to ensure their success, and we've just proven to ourselves that they work. Will we now learn from our own example?

RADISYS GIVES VME THE INSIDE ADVANTAGE





Integrating a PC with your VME system is a smart move. The "PC advantage" provides a superior human interface and access to the PC's huge base of system, application and development software.

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Only RadiSys EPC® Embedded PCs completely integrate the strengths of PC and VME. An EPC, with its exclusive EPConnect™ Software, is the only 386- or 486-based, PC-compatible computer with software that integrates the VMEbus into the DOS, Windows, UNIX and OS/2 environments. EPCs give your VME systems:

- **Highest system performance** from the real-time responsiveness of the direct 32-bit interface between the 386 or 486 and the VMEbus.
- **Improved system packaging** in 1/10th the volume, with integral VME ruggedness, and no bus link baggage.

And EPCs cost you less. EPC-based systems avoid the costly pitfalls of attached PC systems. No extra interfaces, cables, surrogate controllers, or the software to make them work.

Give your VME systems the EPC advantage. Call (800) 950-0044. We'll send all the details. No strings attached.

EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl.
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX,and OS/2			

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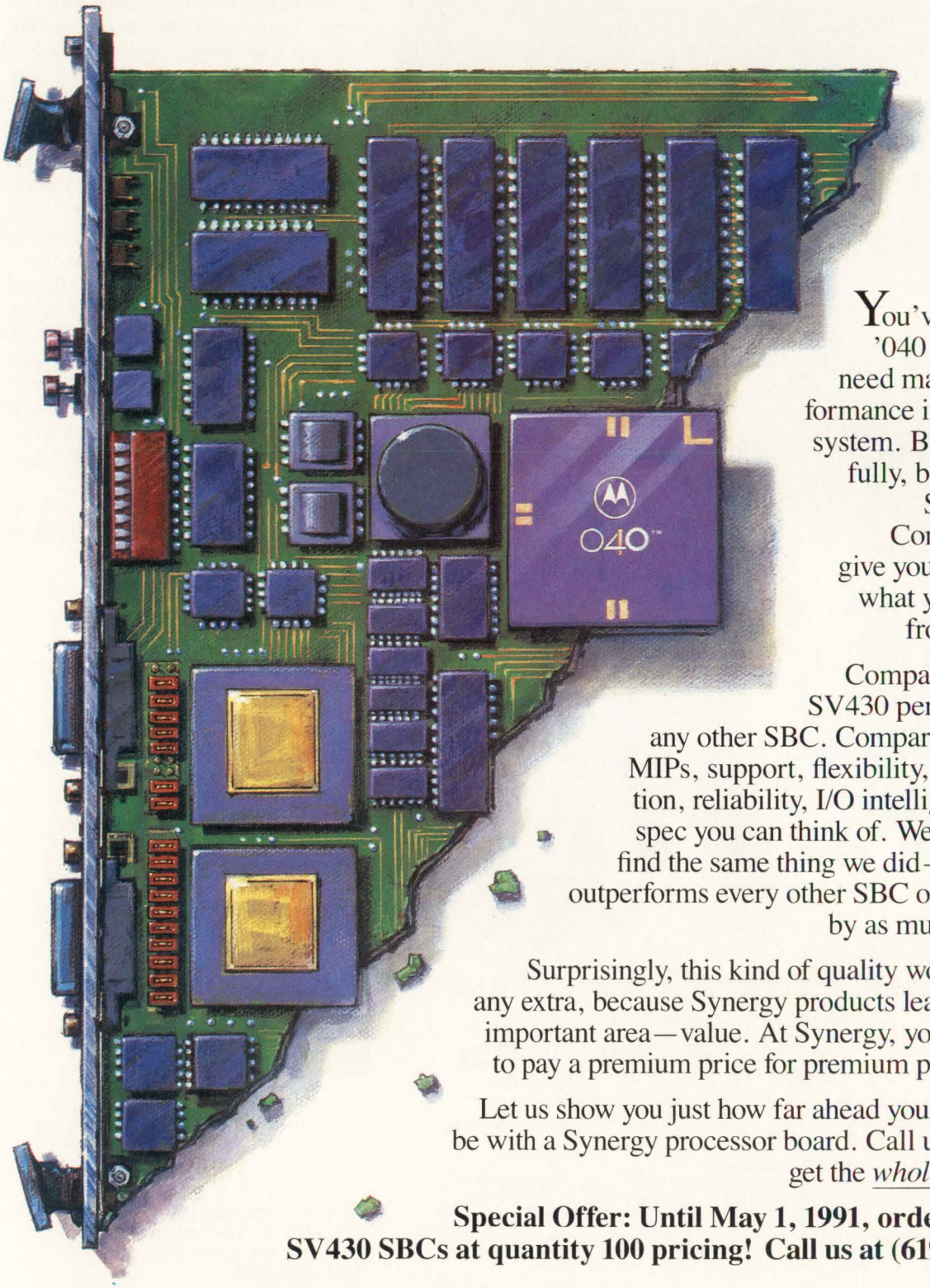
CIRCLE NO. 8

Why Settle for ½



You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

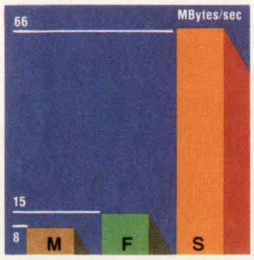
Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Special Offer: Until May 1, 1991, order up to five SV430 SBCs at quantity 100 pricing! Call us at (619) 753-2191.

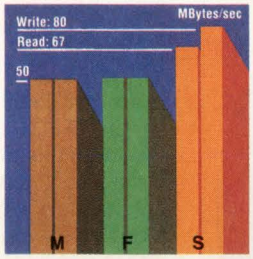
an '040 Board?

Compare our specs. Synergy is superior across the board!



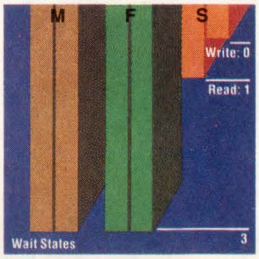
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



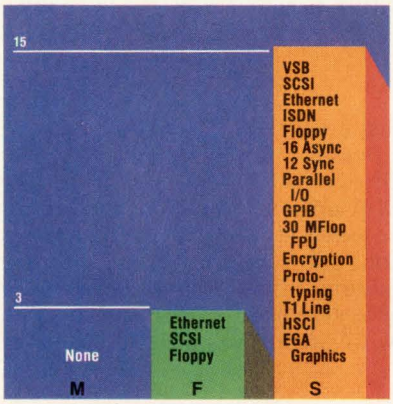
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



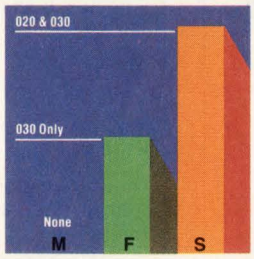
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



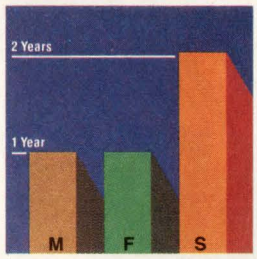
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



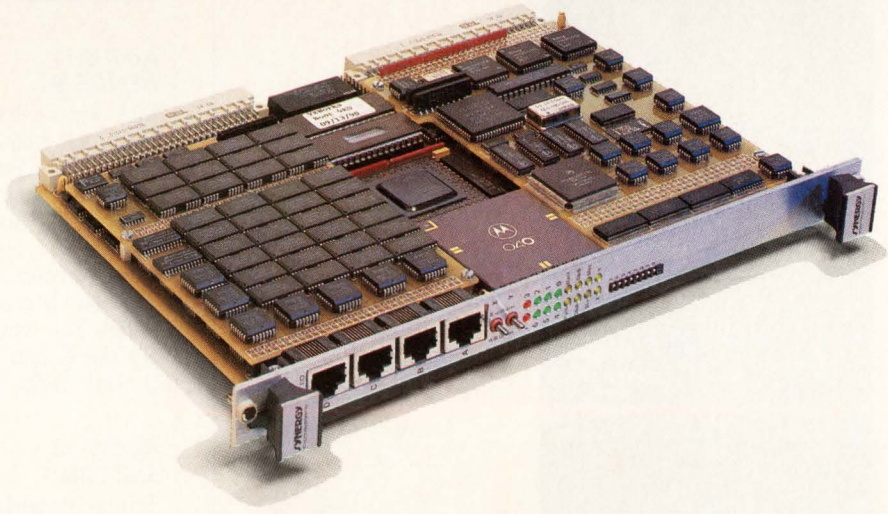
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

Synergy Microsystems, Inc.
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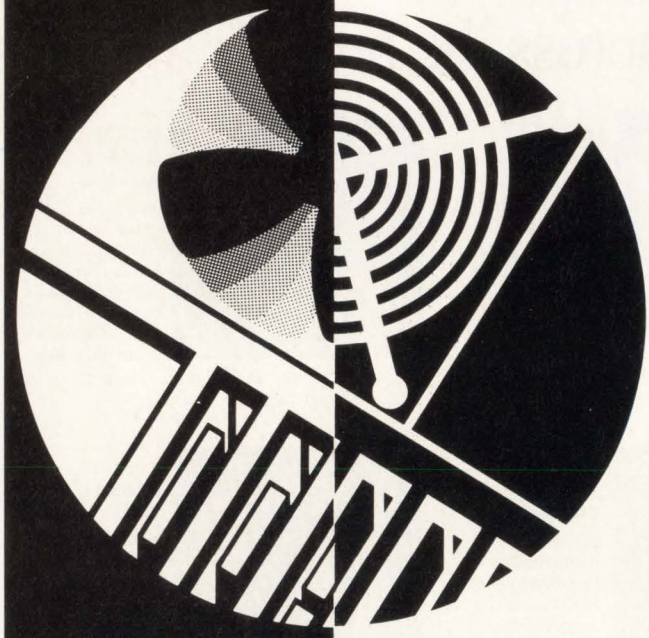
SYNERGY microsystems

CIRCLE NO. 9

NEW & NOW

VMEbus System Enclosure



Ironics now offers the next generation system enclosure with *superior* cooling power.

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ADVANCING VME MULTI-PROCESSING

CIRCLE NO. 10

CALENDAR

CONFERENCES

March 13-20
Hannover Fair CeBIT '91

Hannover Fairgrounds, Hannover, Germany. The more than 4,000 exhibitors from 40 countries at CeBIT will attract computer and communications professionals from 100 countries. The show includes NetWorld Europe, an exhibition and conference presenting 200 networking and connectivity firms from around the world. Information: Hannover Fairs USA, 103 Carnegie Center, Princeton, NJ 08540, (609) 987-1202. **Circle 366**

March 26-28
Southcon '91

Georgia World Congress Center, Atlanta, GA. This concurrent electronics conference and exhibition brings together design, test, manufacturing, and telesystems in one show. Exhibitors' products and technology are geared for the entire design and development team, from R&D through final test. Also, the National Telesystems Conference will be held in conjunction with the Southcon show. Information: Southcon '91, 8110 Airport Blvd, Los Angeles, CA 90045-3194, (800) 877-2668. **Circle 367**

April 2-4
Idea '91

San Jose Convention Center, San Jose, CA. The International Design Engineering and ASIC exposition will offer exhibits from more than 60 ASIC and EDA tool vendors, new product announcements, panels, and a technical/business education program. Topics include making price/performance and time-to-market trade-offs and ensuring first-time product success. Information: *ASIC Technology and News*, 480 San Antonio Rd, Suite 245, Mountain View, CA 94040, (800) 848-IDEA. **Circle 368**

April 8-11
NEMDE '91

McCormick Place, Chicago, IL. The National Electronic Manufacturing and Design Exposition and Conference is designed to present a complete spectrum of products and equipment to the entire engineering and management team. The conference will include 14 technical sessions, 12 workshops and 8 professional advancement courses. Sessions include "Design for Thermal Management," "Functional Test" and "Infrared Reflow Soldering Considerations." Information: Cahners Exposition Group, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60017-5060, (708) 299-9311. **Circle 369**

April 9-12
SMTCON

Trump Plaza Hotel and Atlantic City Convention Center, Atlantic City, NJ. More than 250 suppliers will demonstrate products at the second annual Surface-Mount Technology Conference and Exposition. The exposition will offer a comprehensive range of components, equipment, materials, and services used in

Continued on page 18

If you're tired of pouring on SRAM to get 128Kbyte cache performance,

Take a load off.

Introducing an amazing new cache chip that gives crowded motherboards a new lease on life.

It's called 386™ Smart Cache, a family of chips that integrate a cache controller with up to 16Kbytes of SRAM onto a single, one-million-transistor chip. The result is a 16Kbyte chip that really cleans up, equalling the performance of 128Kbyte caches.

Intel's 386 and 386SX Smart Cache are one-chip solutions that give you extra space on your motherboards for other applications.

And when you stack them up against other caching solutions, you'll find their innovative architecture costs substantially less.

Give your motherboard a lift. Send in the attached card today for a free copy of our unique 386 Smart Cache video, performance report and documentation. Or if the card's been ripped off, call 1-800-548-4725, dept. HA47.

Because the reasons to look into 386 Smart Cache are really starting to pile up.

intel®

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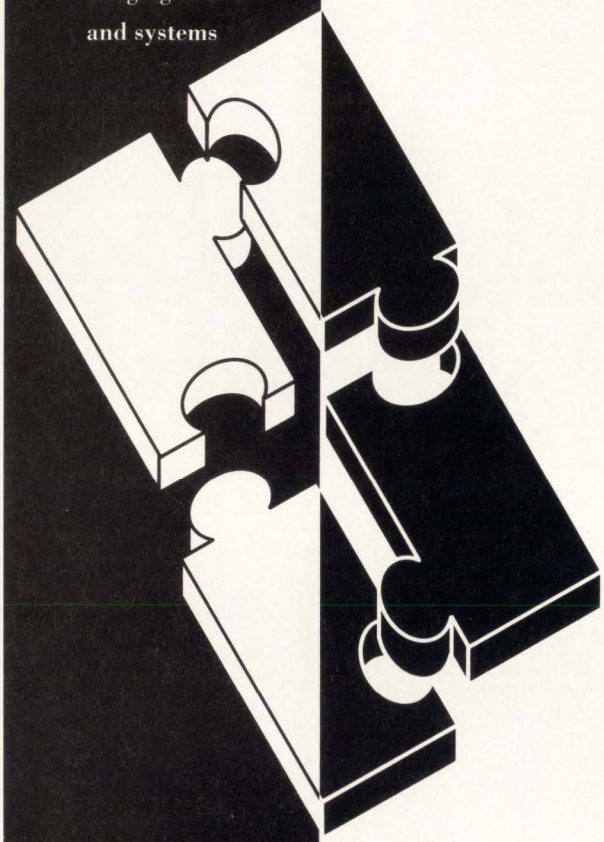
CIRCLE NO. 11

NEW & NOW

Graphics and imaging boards and systems



Ironics now offers a *complete* graphics and imaging pipeline.

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ADVANCING VME MULTI-PROCESSING

CIRCLE NO. 12

CALENDAR

CONFERENCES

Continued from page 16

the design and manufacture of surface-mount and mixed technology products. The conference features advancement courses, technical forums, technical sessions, and workshops. Information: IC Management, 900 N Franklin St, Suite 700, Chicago, IL 60610, (312) 944-3434. **Circle 370**

April 16-18
Electro/International

Jacob K. Javits Convention Center, New York, NY. This three-day electronics conference and exhibition will feature more than 500 exhibits and demonstrations; a technical program with tracks including digital systems and software and IC technology; a purchasing conference; and a VMEbus/Futurebus+ seminar. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045-3194, (800) 877-2668. **Circle 371**

April 22-25
NCGA '91

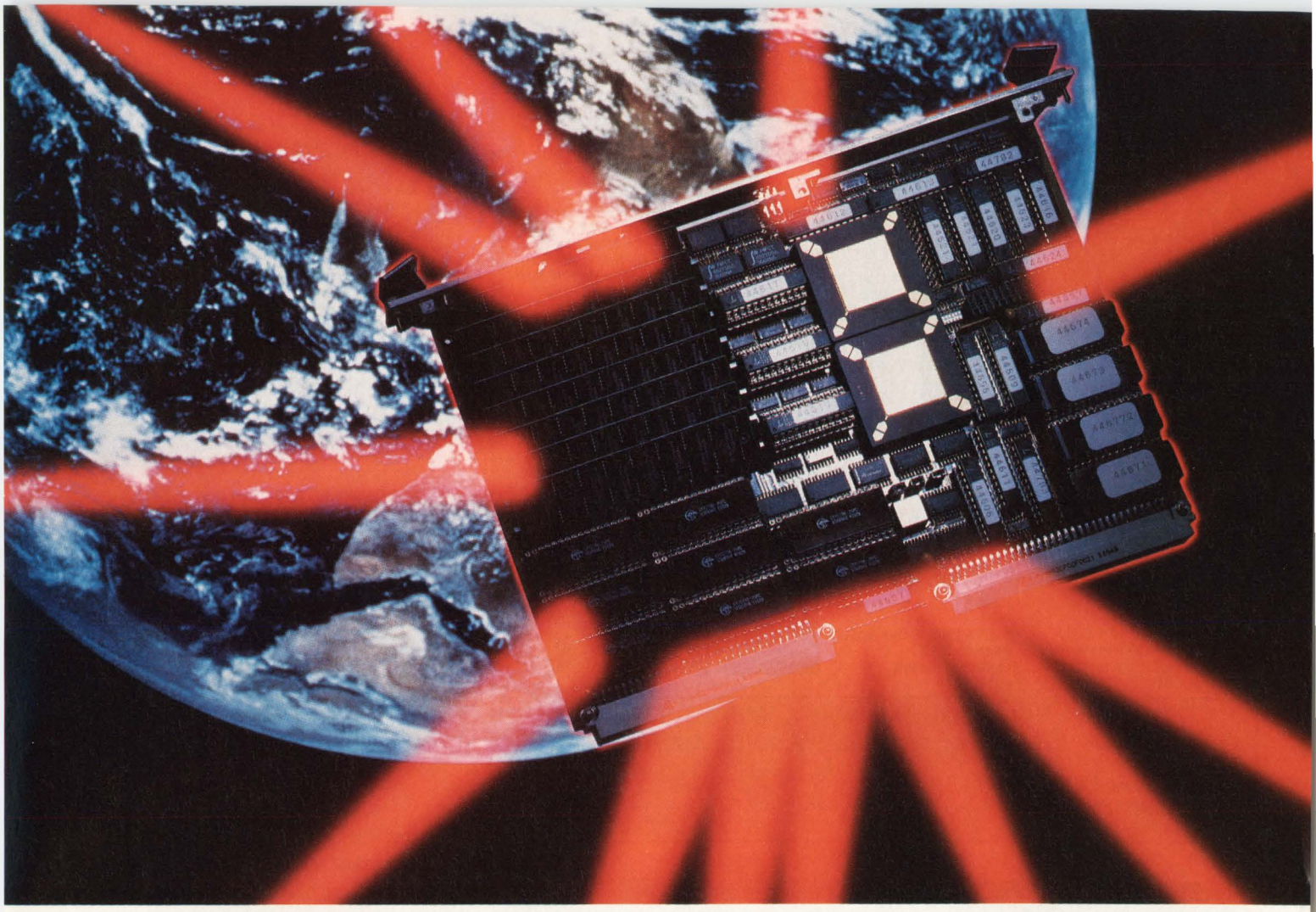
McCormick Place North, Chicago, IL. The 12th annual conference and exposition sponsored by the National Computer Graphics Association will feature more than 200 exhibitors and a conference program geared toward computer graphics applications, including architecture, engineering, graphic design and publishing, and more. Information: National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031, (703) 698-9600. **Circle 372**

April 30-May 1
The Canadian High Technology Show

Place Bonaventure, Montreal, Quebec. Nearly 500 exhibitors from Canada, the United States, Europe, and Asia will display products in components and microelectronics, instrumentation, production and packaging equipment, and design automation systems. This electronics exhibition and conference—Canada's largest electronics show—attracts engineers, purchasers, management and marketers from high-tech industry, government and institutions. Information: Connelly Exhibitions, 2487 Kaladar Ave, Suite 214, Ottawa, Ontario K1V 8B9, (613) 731-9850. **Circle 373**

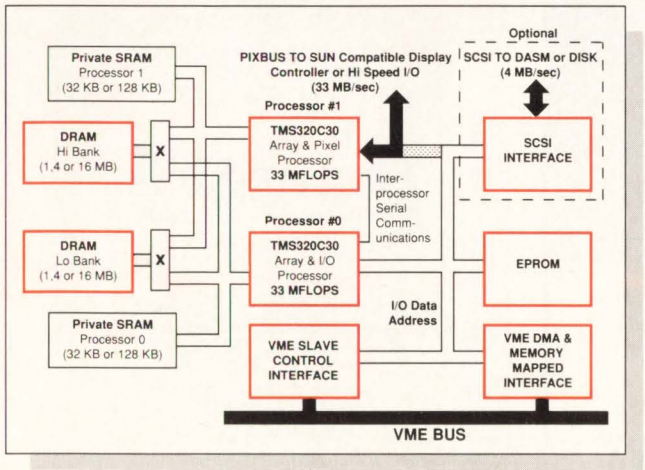
April 30-May 2
EDS

Las Vegas Hilton Hotel, Las Vegas, NV. The three-day Electronic Distribution Show and Conference will feature exhibits, conferences and seminars on topics including limited distribution lines, market opportunities, and the distributor's role in enabling concurrent engineering. Information: Electronic Industry Show, 222 S Riverside Plaza, Chicago, IL 60606, (312) 648-1140. **Circle 374**



For Those Who Like It HOT

Announcing the MSP-6C30
66 MFLOP VME Array Processor



The MSP-6C30 is a 66 MFLOP, floating-point, VME array processor optimized for signal and image processing. High performance is assured through a unique, multi-banked, crossbar memory architecture, and high bandwidth is achieved with multiple, fast, industry standard I/O ports. Also available in a PC-AT version with optional VGA compatible display controller.

Features

- Under $100/MFLOP (single qty.)
- Dual TI TMS320C30 Processors
- 66 MFLOP, 32 MIPS Peak Rate
- Up to 32 Mbytes On-board Dynamic RAM
- High Speed Private SRAM
- Optional SUN Compatible Frame Buffer
- Optional SCSI I/O (disk, tape, A/D, D/A, Video, DR11-W)

Applications

- Medical
- Geophysics
- Defense
- Communications
- Digital Signal Processing

For Further Information Contact: Howard Cohen
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8 Centennial Drive, Peabody, MA 01960-7987
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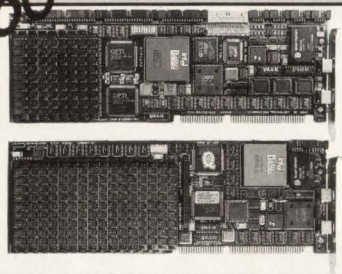
CDA COMPUTER DESIGN AND APPLICATIONS

CIRCLE NO. 13

25 & 33MHz
486/386 Single Board Computers
Thousands Shipped

486



CAT1010
- Fully Integrated 80486 25/33MHz /AT CPU
- Up to 32Mb DRAM Memory
- 8Kb Internal CACHE
- 6,8,12MHz Bus Speed
- Phoenix BIOS
- Floppy Interface
- SCSI & IDE Interface
- 2 Serial/1 Parallel Port
- Up to 512Kb PROM
- On-board Battery
- 4.7 X 13.4"

CAT1000
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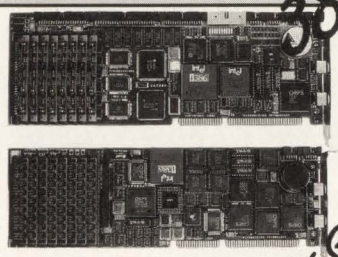

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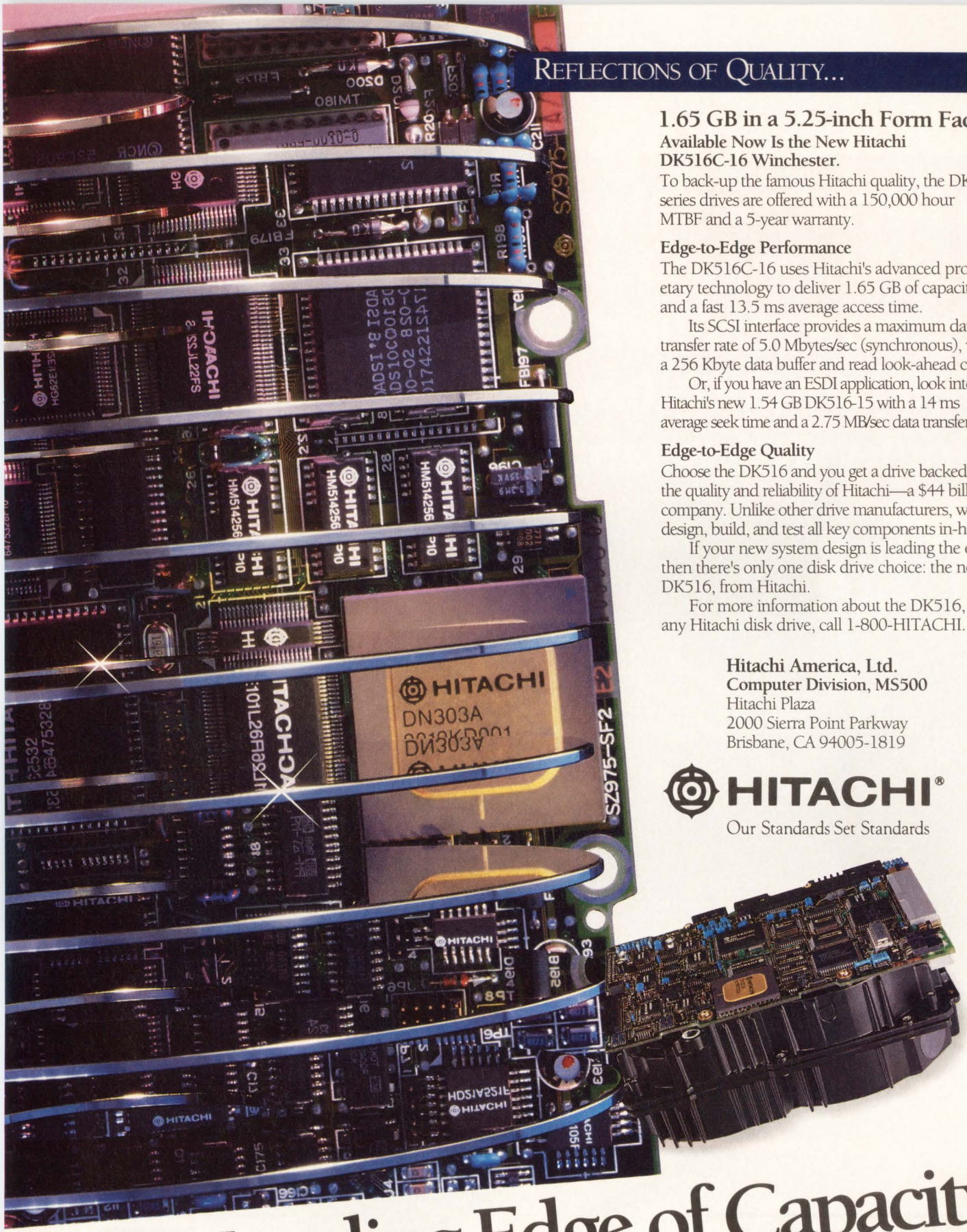

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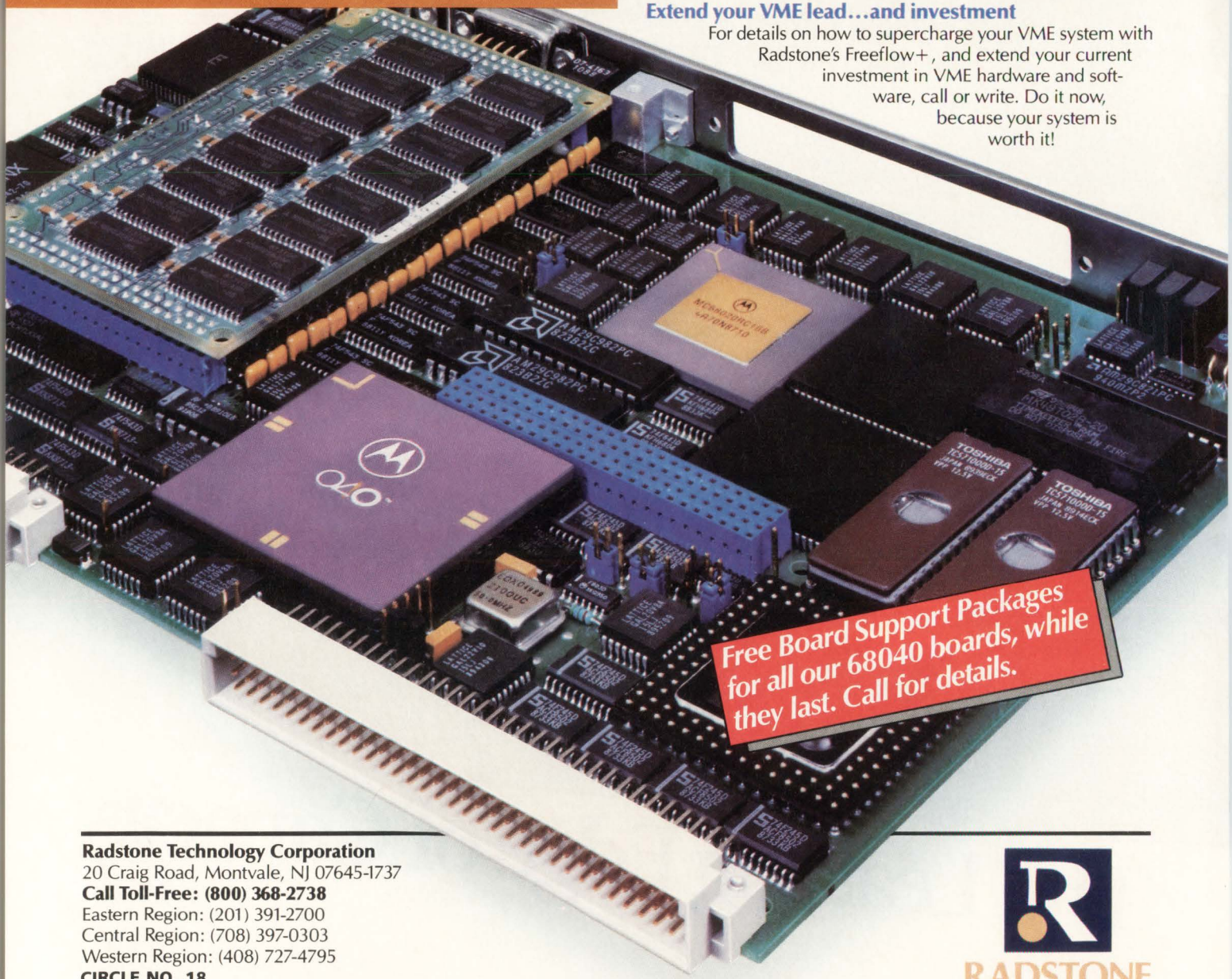

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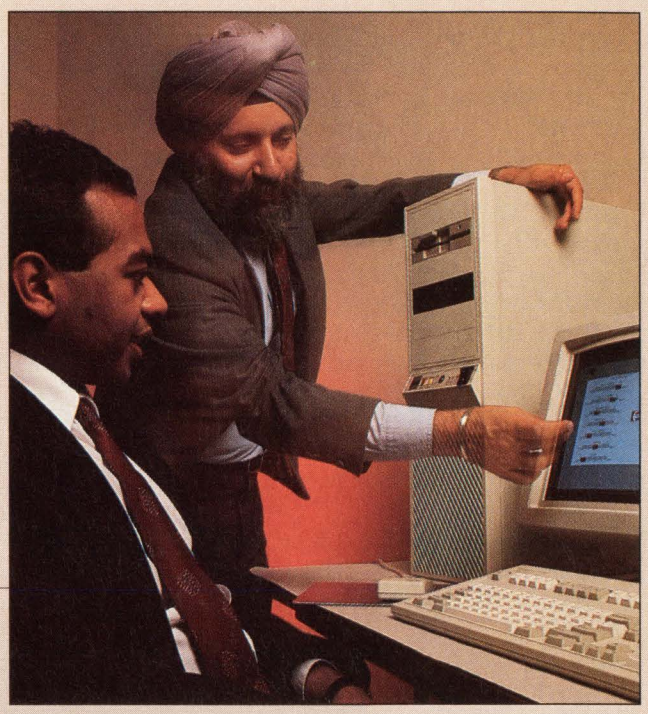
Inder Singh on: Posix



Long dominant in the real-time field, proprietary kernels are faced with a shrinking market share due to the convergence of several strong market factors, not the least of which is the move toward standards.

During recent years, the computing world has made major progress toward standard, open systems based on the Unix operating system and the emerging Posix standards. The significant attractions of standard, open systems include vendor independence; protection from technological obsolescence; preservation of software investment; availability of off-the-shelf applications software from independent suppliers; availability of trained programmers familiar with standard environments; and connectivity between dissimilar computers within the user organization.

In stark contrast with this trend toward open, standard platforms, the world of real-time computer applications is fragmented: dozens of proprietary operating systems and restricted kernels with limited capabilities are in use. No single software environment has succeeded in capturing a significant portion of the market. This makes the development of real-time applications unnecessarily more complicated, unwieldy and expensive than that of other applications.

Developers of real-time applications find themselves stuck with a single kernel vendor, and often with specific hardware platforms. They are forced to start each project from scratch, and are unable to build upon previous work or mix solutions from multiple vendors. The lack of a standard platform (or even of a widely used one) has discouraged the development of a third-party software industry for real-time applications or development tools. The real-time kernels provide minimal facilities compared with those of complete operating systems such as Unix, forcing programmers to reimplement features commonly available to the non-real-time developer.

Because of all the problems faced by real-time developers working with these proprietary kernels, there has been a strong and growing interest in Unix/Posix operating systems for real-time applications. All of the open-system benefits previously mentioned are equally applicable to real-time applications. As the only "open," fully featured, multitasking operating system that has been ported to many CPU architectures and which is available from many vendors, Unix is an extremely attractive candidate for a standard real-time operating system. The development environment of Unix is also quite popular among software developers.

Will a Unix/Posix standard dominate?

The move toward open real-time systems based on Unix/Posix is gaining momentum with the emergence of standards such as the IEEE-1003.1 and -1003.4 Posix standards. Also contributing to this momentum is the commercial availability of products, such as LynxOS, that conform to the standards and eliminate the performance limitations of previous real-time Unix solutions. In fact, Unix/Posix will dominate the high-performance real-time world, just as it's beginning to dominate scientific, technical and other computing markets.

The IEEE-1003.1 Posix standard essentially defines a standard application programming interface for Unix, and the IEEE-1003.4 Posix standard defines a set of extensions to this interface for real time. Together, these provide for the first time a standard programming interface for real time. This opens up the possibility of writing portable real-

time applications, something that has been sorely lacking in the real-time world. The fact that these standards specify the interface rather than the implementation is particularly significant, since Unix itself is notoriously poor for real time. This allows Posix-compliant operating systems such as LynxOS—which is implemented from the ground up for real time without using any actual AT&T code—to provide all the benefits of Unix and open systems without compromising on performance.

But why is a full-fledged operating system like Unix necessary for real time? Why can't the task be accomplished through the use of kernels and real-time executives, which, though restricted in functionality and limited in their non-real-time capabilities, have been the mainstay of the real-time market?

The reasons include the increasing complexity of real-time applications; the so-called RISC freeway effect; the federal policies on Posix and commercial off-the-shelf products; the cost savings provided by open systems; development time; and the availability of products that eliminate Unix' real-time limitations.

Why were proprietary kernels popular?

Before discussing each of these reasons in detail, it may be helpful to examine the three main reasons why restricted real-time kernels have been popular despite their limited capabilities. Proprietary kernels were once popular because Unix couldn't meet the performance requirements of real-time applications, so developers had no choice but to use a proprietary, limited-function kernel. The key performance consideration was fast, bounded system response times to external events or timers. A new generation of Posix-compliant operating systems is becoming available that provide the fast, deterministic response times previously available only with the restricted kernels, along with all the functionality of a full-fledged operating system such as Unix.

In the past, most real-time applications were so simple that they didn't need a full-fledged operating system. As the complexity and sophistication of real-time applications increases, and software starts to dominate the costs of many projects, real-time developers will look for more help from the operating environment than restricted kernels can provide.

Small kernel size used to be important for cost-sensitive, high-volume embedded applications where the operating system must utilize as little RAM or ROM as possible. While memory isn't free, at under $50 per megabyte it's much less expensive than in the past and not a predominant cost factor in most real-time applications.

Since real-time performance, simplicity and memory costs are the three primary advantages that restricted kernels provided, the emergence of high-performance, ROM-able Unix/Posix operating systems and the falling cost of memory are starting to rob these limited kernels of much of their market advantage. But why the market share of kernels will shrink as real-time Unix/Posix grows needs to be examined in greater detail.

Complexity and the RISC freeway effect

As mentioned, two of the reasons for Unix/Posix' emergence as the dominant operating system in real time are the increasing complexity of real-time applications and the RISC freeway effect. These two phenomena are closely coupled. Real-time applications are growing more complex at the same time that users of real-time applications expect software to provide much of the user friendliness associated with non-real-time programs. In addition, these users increasingly expect that real-time systems will integrate well with other non-real-time systems in their environment.

Take a typical real-time application, such as a medical or scientific instrument, a data acquisition module, or a process controller. In the past, this type of application would have involved a simple control algorithm for a microprocessor-controlled piece of hardware with some lights and switches on a control panel. A real-time kernel provided a convenient base for implementing such an application. In fact, in many cases system developers implemented the code directly on the hardware, or they implemented a minimal home-brew kernel.

Today, the user of such a system—who's familiar with a wide variety of sophisticated, user-friendly non-real-time products on personal computers and workstations—has much higher expectations. He looks for a sophisticated user interface involving a CRT display (possibly with graphics and color), and on-line help. An inexpensive hard disk to log operational information or provide additional features isn't uncommon. Sooner or later, connecting this piece of equipment to other computer systems will also be required. Finally, users look for systems to be flexible and expandable.

To handle the increasing complexity demanded of today's real-time systems, the real-time applications developer needs the power and richness of a full-featured Posix operating system, particularly in such areas as graphical user interfaces, connectivity, and mass-storage support. With a Unix/Posix system, he has access to many standard facilities that save him from having to reinvent the wheel, and provide far more powerful and user-friendly solutions. In the user interface area, for example, he can build on X Windows and Motif. Connectivity solutions such as Transmission Control Protocol/Internet Protocol, Network File System, Open Systems Interconnection, and X.25 are easy to fold in. With RISC technology, increasing computing

power to support these software tools is available at an affordable price.

Conversely, the availability of increased computing power at lower prices provided by RISC CPUs, along with the functionality provided by real-time Posix operating systems, creates an increasing appetite for ever more complex and demanding real-time systems. This is the phenomenon we call the RISC freeway effect, and it's analogous to the situation of a freeway being over capacity from the very day that it's opened. Despite the best traffic surveys of people traveling from point A to point B without a freeway, transportation planners find that the mere existence of the freeway and its convenience encourages people to travel between A and B, even though they didn't before the freeway was built.

The impact of federal standards

Federal policies on Posix compliance and commercial off-the-shelf products not only demand Posix-compliant operating systems but require that those systems run on relatively inexpensive off-the-shelf hardware. This means that custom hardware systems will be excluded from many contracts, as will kernels and operating systems that aren't fully Posix-compliant.

It's important to note that the government standards forcing the move toward Posix don't specify the actual implementation of a Unix version. Instead, they require conformance with the Posix standard, which specifies the interface between the operating system and applications. The focus is on portability of applications—not on the code inside the operating system.

The U.S. government provides a test suite through the National Institute of Standards and Technology to verify Posix 1003.1 compliance, and is establishing certification procedures for conformance testing. This can be expected to be extended to Posix 1003.4 as well. Posix conformance, as defined by the IEEE Posix committee, requires support of all interfaces as defined in the standard. Products that implement some Unix-like features or provide some mechanisms to work in conjunction with Unix won't qualify. Increasingly, Posix compliance will separate a successful contract bid from an also-ran.

Reduced costs and development time

A Posix-compliant operating system running on commercial, off-the-shelf hardware brings more benefits to users than just the convenience of standardization: it reduces both hardware costs and development time (and reduced development time also results in further cost savings). Cost savings in hardware come from the use of readily available, mainstream products that are competitively priced and use the latest technology—examples of such products include PCs, workstations and general-purpose computers.

Further, in later phases of a real-time system's life cycle, the user retains the option to migrate his application to the most cost-effective platform using the latest technology, perhaps from a different vendor.

The user can also achieve considerable savings in the costs of software development and maintenance. With restricted real-time kernels, the developer has to reinvent functions that are provided by a fully featured Posix-compliant operating system. Several off-the-shelf development tools are also available for the Unix/Posix environment.

In addition, applications developers don't have to learn two operating systems—one for development and another for run time—nor do they have to learn a specialized real-time programming language. With Posix and commercial off-the-shelf products, the user can develop applications in C or Ada and then run them without modification.

Training costs for both programmers and users are reduced since more and more people are already familiar with Unix.

Further cost savings come from the ability to use off-the-shelf software for numerous applications including graphics, networking, databases, and spreadsheets. Further development cost savings result from the ability to migrate existing C or Ada applications to a real-time system.

A standard programming interface opens up the possibility of writing portable real-time applications.

The advent of the Posix standards, particularly Posix 1003.4, legitimizes the concept of Unix-compatible, real-time operating systems. We will see an expanding role for full-featured, Posix-compliant operating systems and a shrinking market share for limited-function, proprietary real-time kernels. Widespread acceptance of open, Posix-compliant real-time operating systems will foster a market for third-party tools and applications, and facilitate the development of real-time applications. This will fuel a major growth in the overall size of the real-time market.

There will continue to be a significant niche for the proprietary real-time kernels for small, high-volume, cost-sensitive applications, but the big growth will be in the Posix area. We will see many of the proprietary kernel vendors come out with Posix-compatible libraries and extensions in an attempt to defend their market share.

Inder Singh is president of Lynx Real-Time Systems (Los Gatos, CA).

SOFTWARE

Real-time Unix develops multiprocessing muscle

Tom Williams, Senior Editor

The attractions of the Unix operating system environment have spurred efforts by a number of companies to provide versions of the operating system that can be used for real-time applications. There are now efforts to expand the successful real-time adaptation of Unix to multiprocessor architectures.

At least two companies have made significant progress: Modcomp (Ft. Lauderdale, FL) with a multiprocessing version of its Realix real-time Unix system, and Lynx Real-Time Systems (Los Gatos, CA). Lynx offers several multiprocessing versions of its Lynx/OS that conform to the Portable Operating System Interface for Unix (Posix) standard. Realix is a functional superset of AT&T Unix System V, Release 3.2 and supports the Posix 1003.1 standard. It will incorporate the 1003.4 real-time extensions when they're finalized. Posix is a subset of the Unix application interface but doesn't provide compatibility with libraries and utilities often associated with Unix systems.

Lynx is tailoring versions of its Lynx/OS Posix-compliant operating system to three different multiprocessor architecture schemes. Lynx/OS incorporates both the Posix 1003.1 interface standard and the 1003.4 real-time standard, draft 9. Later releases of the real-time standard will be supported as they're finalized, and draft 9 will continue to be supported for those who choose to design with it now.

Multiprocessing offers choices

Lynx has characterized the three multiprocessor architectures it supports as "tightly coupled," "snugly coupled" and "loosely coupled." According to Lynx vice-president of engineering, Mitch Bunnell, a symmetrical, tightly coupled multiprocessor system is one in which all memory and data structures are shared by all CPUs. Snugly coupled, a term Lynx coined, refers to a system with multiple CPU boards plugged into a backplane where certain areas of each CPU's memory are allocated for shared communication. Each CPU also has its own local memory that's not shared. In addition, separate memory boards can be plugged into the system to act as global, or shared, memory. The third characterization, loosely coupled, refers to a system where multiple CPUs pass messages via a LAN such as Ethernet. Often there's no shared memory in a loosely coupled system.

In snugly and loosely coupled systems, each CPU has its own copy of the kernel. In a tightly coupled system, there's one copy of the kernel that all CPUs use. In this system, where all CPUs potentially have access to all memory and kernel data structures, it's important to control access to critical kernel data structures while maintaining maximum performance. As Bunnell puts it, "The

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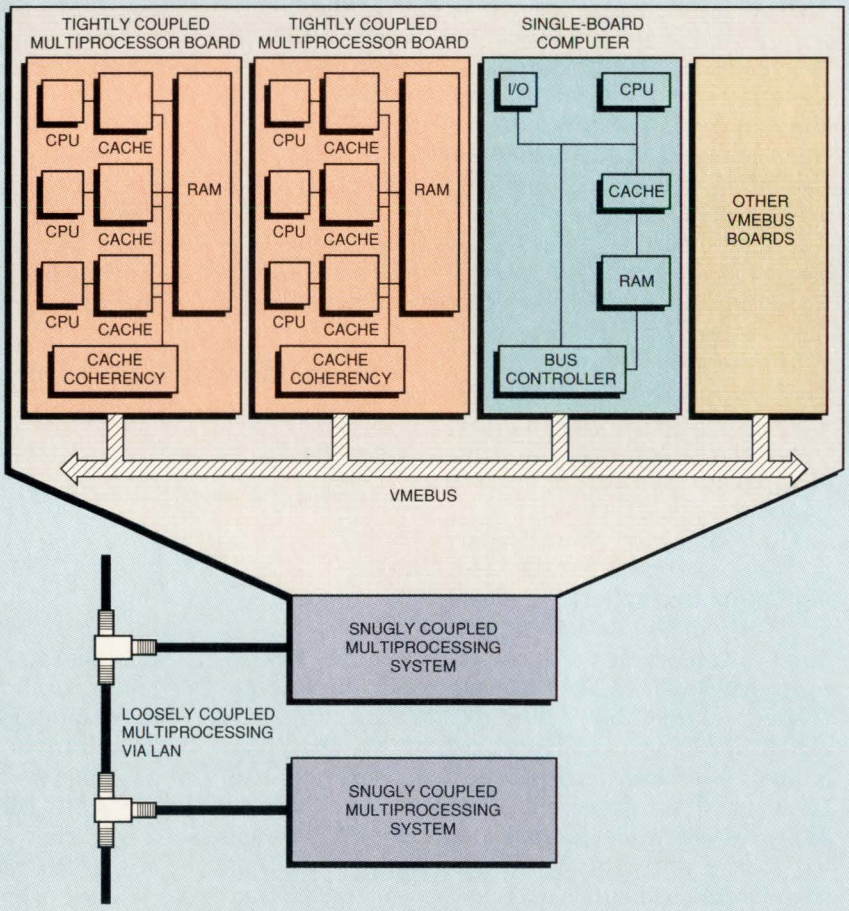
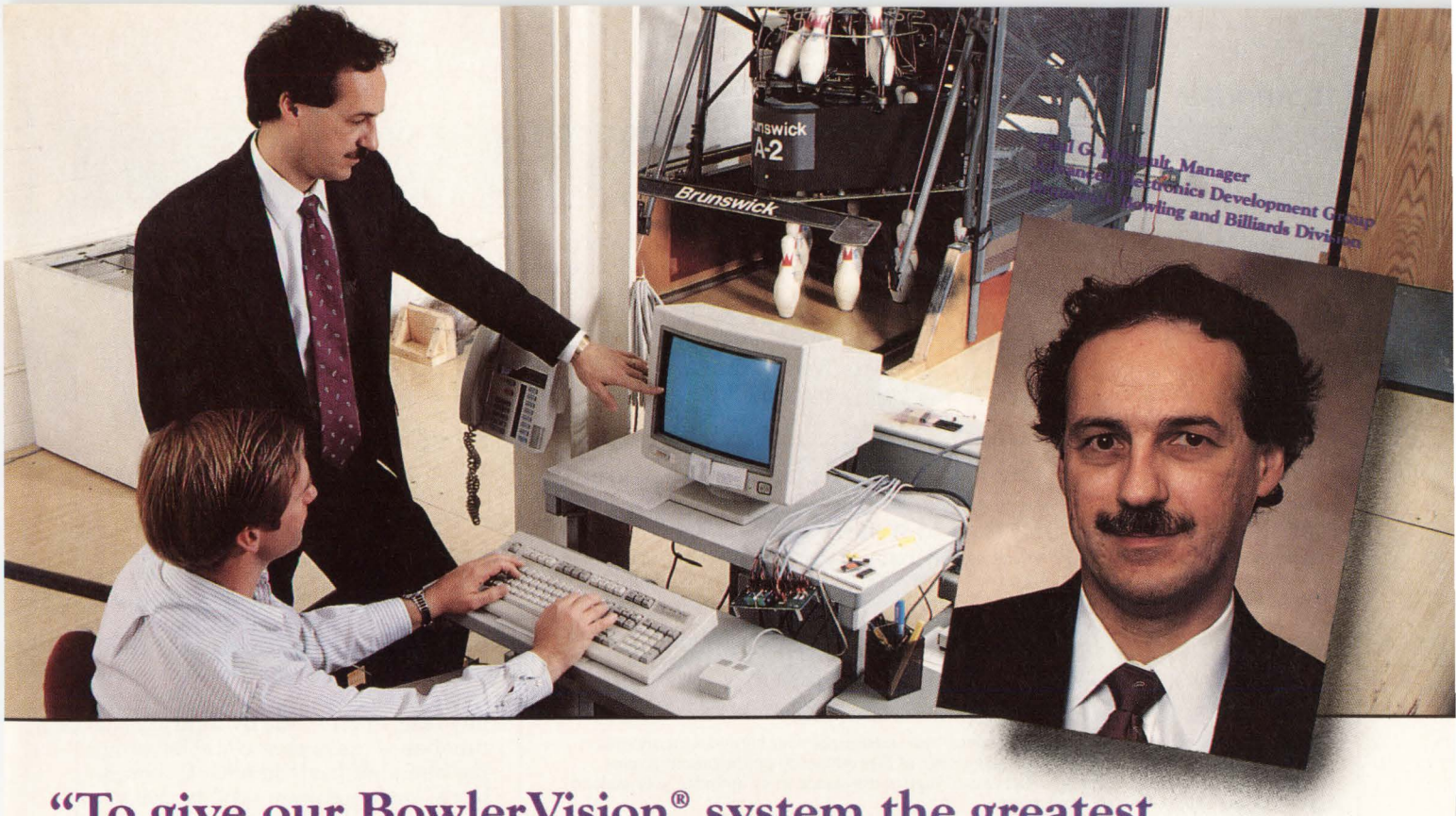


A hierarchical multilevel multiprocessing system can encompass all three forms of multiprocessing. In the symmetrical, tightly coupled system, multiple CPUs on the same board share all memory and data structures via a single copy of the operating system kernel while maintaining cache coherency. They can coexist on a bus with other single-CPU boards in a "snugly" coupled arrangement. Communication between systems takes place via reserved areas of shared memory. Here, each board on the bus has its own copy of the kernel. Additionally, single-CPU board or snugly coupled systems can be configured in a loosely coupled system where interprocessor communication takes place over a LAN.



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more independently a CPU can run, the more throughput you'll get. On a tightly coupled system, other CPUs are going to steal some memory cycles, which is why you limit the number of processes."

A normal Unix kernel is not preemptable by real-time interrupts. Real-time developers either licensed the kernel from AT&T and modified it to support interrupt handling or wrote their own functional equivalents from scratch. Real-time kernels generally have areas defined where a higher-priority interrupt can preempt a running process without endangering data structures. According to Bunnell, Lynx has taken a different approach. They've written the kernel from scratch so there are few areas that can't be preempted.

Predictable control

When one process has control of one of these nonpreemptable areas, other processes encounter a "spin lock," a busy wait loop, before they can have access. It can happen that a number of processes queue up for access to a spin-locked area. They would, of course, get access according to their priority. The designer must be able to calculate the worst-case time for any task to complete by figuring the number of tasks that could be pending ahead of it along with the number of such nonpreemptable areas it could encounter in the kernel.

Modcomp's Realix is tailored for a symmetrical, tightly coupled system using up to 10 Motorola MC68030 and 88000 processors and up to 512 Mbytes of 16-way interleaved main memory. The Modcomp operating system kernel uses spin locks to maintain data structure integrity when the lock time is very small—for example, less than the time of two context switches. For longer lock times, the system uses suspend locks, which allow execution to switch to another runnable process while the desired kernel resource is blocked. Realix supports only symmetric, tightly coupled multiprocessing.

In the snugly coupled scheme, CPUs communicate via areas of their own memory or system memory set aside to be shared while the loosely coupled scheme passes messages via the network. In each of these schemes every CPU has its own copy of the kernel, but the same preemption mechanism is used to handle local tasks of varying priorities.

Real-time architectures

Although Lynx supports all three architectures, Bunnell thinks that the snugly coupled approach may be best for real-time. While the tightly coupled approach may have advantages in terms of overall throughput, it doesn't allow the designer to dedicate hardware resources to critical tasks. In the snugly coupled scheme, a critical task can be assigned a high

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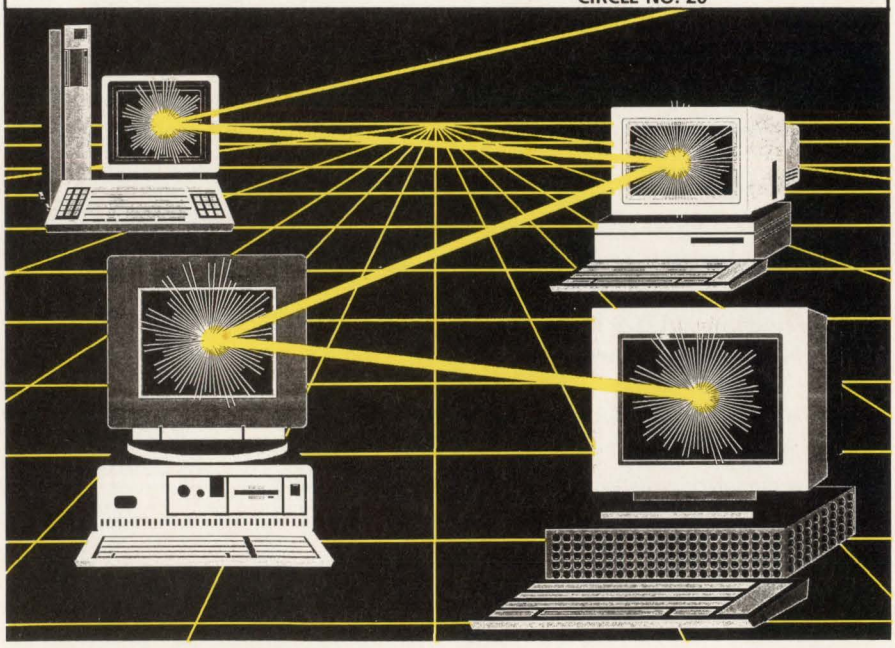

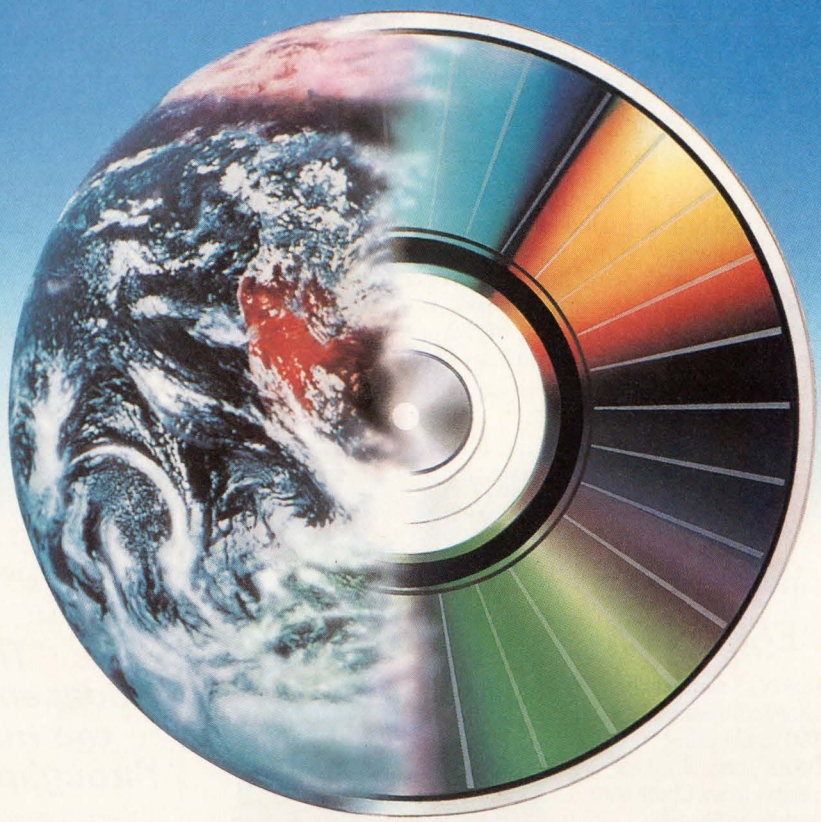

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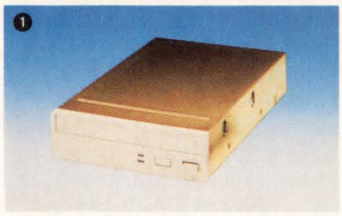

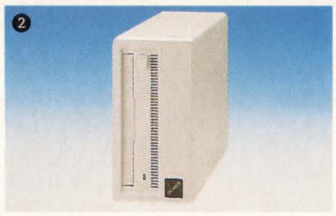

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CIRCLE NO. 21

SOFTWARE

priority and be set to run locally on a given CPU. Other, less-critical tasks can be made to run globally on whatever CPU is available. This means that bus timing has to be factored into the tasks' execution times, but it's still possible to maintain deterministic behavior. In the loosely coupled system, tasks can run deterministically on local CPUs, but due to the random nature of Ethernet's collision/retry communications, it's difficult or impossible to maintain determinism over the network.

Modcomp's Realix system, while currently confining itself to symmetrical, tightly coupled architectures, does allow the programmer to dedicate resources. According to Joel Wagner, principal programmer I for multiprocessor operating systems, one can lock processes in local memory as well as a process to a processor. "Normally the system decides automatically where a process can run based on the least-busy CPU," Wagner says. "We offer a choice. The default is complete load balancing, but you can ask for targeting."

"The more independently a CPU can run, the more throughput you'll get."

—Mitch Bunnell, Lynx Real-Time Systems

■ ■ ■

Lynx will soon offer a symmetrical, tightly coupled multiprocessor version of its single-processor Lynx/OS for the Motorola 88000 immediately. The company will then introduce a module to implement a snugly coupled system. When the snugly coupled module is added, it's possible to boot the entire system from a single disk. A definition file knows which kinds of processors are on the system and can download the appropriate code to each one. A loosely coupled version of Lynx/OS will be introduced later in the year.

Each kernel contains the full Posix 1003.1 interface with the 1003.4 real-time extensions. Modcomp has a group that is porting Realix to various architectures as the market demands. Realix offers the ability to run at the System V, Release 3.1 or 3.2 level or to "turn on" Posix as the user requires. Posix isn't necessarily integrated with the kernel. ■

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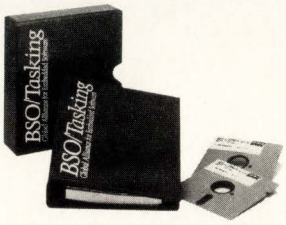

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CIRCLE NO. 23

DESIGN AND DEVELOPMENT TOOLS

Tool suites address elusive analog problems

Mike Donlin, Senior Editor

Higher levels of integration are bringing components off circuit boards and onto chips, hybrids and multichip modules. These levels of integration, however, bring design problems to engineers who must consider analog effects of tightly packed high-speed digital components as well as the headaches that come with mixed analog/digital circuits. Tool vendors are responding with a spate of analog design environments to address these concerns and assist engineers who may not have adequate experience in analog circuit design.

"I've seen some research that estimates that there are only two or three thousand analog IC experts out there," says Eric Filseth, director of IC product marketing at Valid Logic Systems (San Jose, CA). "Until recently, designers didn't have to worry about analog effects, because there wasn't a lot of pressure on them to incorporate analog functions on a chip. Now that the technology's available, designers are having to contend with the vagaries of analog effects."

Integrating analog tools

Perhaps one of the most important developments in analog tool technology is the tight integration of schematic capture, layout, analysis and simulation with component libraries. The underlying frameworks and databases that are the foundation for this integration lead engineers through the logical flow of circuit design by providing a sequence of choices at levels of increasing detail. Tool suites such as Valid's Analog Workbench contain a standard set of basic circuit elements, including ideal semiconductors, for layout, analysis and simulation.

"A framework lets users translate the parts and connectivity data from the schematic to the layout," says Dirk Wauters, Valid's director of marketing. "It lets users take parameters that were simulated and optimized in the schematic and transfer them to the layout."

Tight integration not only enhances communications, it also keeps tools abreast of the analog effects caused by component placement. As clock frequencies get higher and device densities increase, the analog effects of component placement become critical. Toolsets that can back annotate simulation results into the schematic or layout editor allow users to experiment with "what-if" scenarios without leaving the design environment.

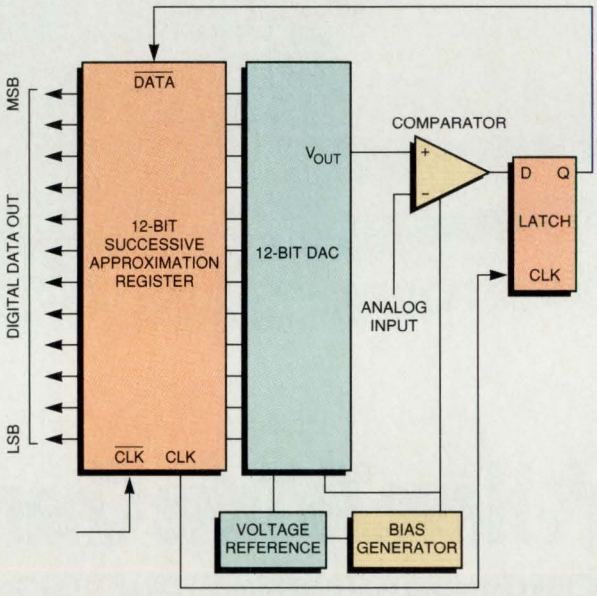
"Physical layout is more important than ever," says Kevin Jorgensen, product marketing manager for analog and mixed analog/digital systems at Viewlogic (Marlborough, MA). "Line length constitutes delays, and proximity of one line to another constitutes a transmission line. So you have those two forces working against each other. If you shorten your lines, you bring components closer together and have to deal with those effects. This is why both pre- and postlayout simulation is so important. You need to know not only the behavior of the ideal device but also the effects of the real layout."

Multiple simulation choices

There are, of course, many levels of simulation, depending on how detailed a result the designer needs. If the device under consideration hosts a relatively small number of transistors that are being pushed to maximum performance, then the simulation must be a compute-intensive, transistor-level electrical simulation, including models of the interconnects. A more-complex device, on the other hand, that isn't pressing the state of the art in performance can be characterized at a higher, or behavioral level of simulation. And in mixed-signal simulation it might be necessary to do some of each.

Viewlogic's Viewsim/SD mixed-signal simulator, for instance, can look at a circuit at either level, depending on the needs of the application. To simulate a 12-bit, successive-approximation analog-to-digital converter, for example, it's necessary to model the behavior of the separate analog and digital functions, but choices can be made on how to simulate each.

A FUNCTIONAL APPROACH TO SIMULATION



Viewlogic's Viewsim/SD separates the components of this model successive-approximation analog-to-digital converter into analog and digital functions to accurately simulate performance. In this model, there were over 400 active devices, shown here in a hierarchical representation that allows designers to think of complex circuits as functions.

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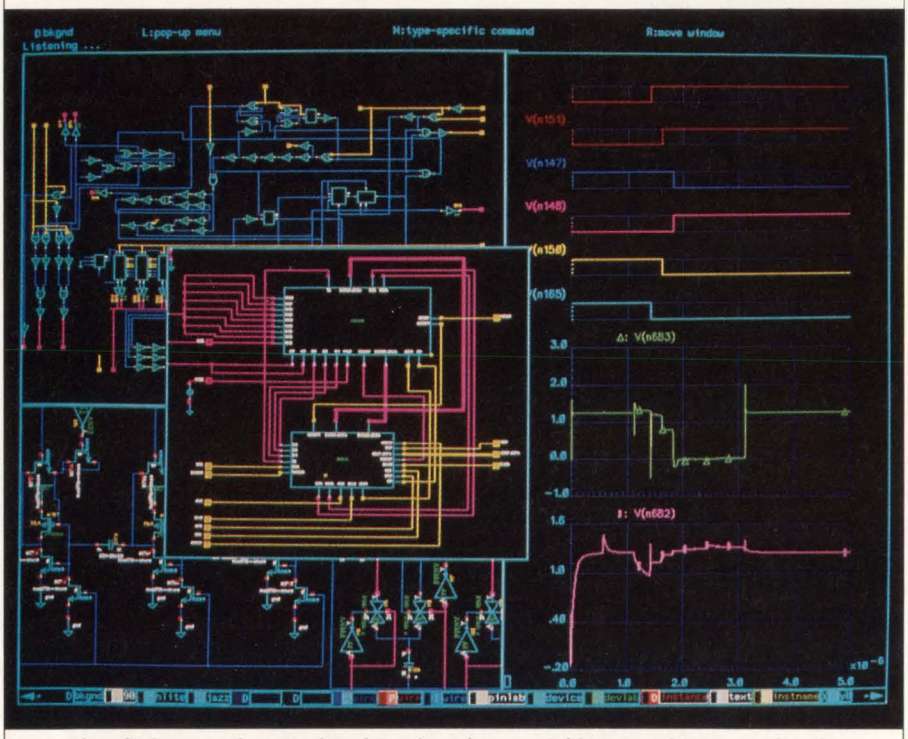
DESIGN AND DEVELOPMENT TOOLS

The successive-approximation register (SAR), a digital portion of the circuit, feeds the analog portions: the band-gap reference, the D-A converter, the bias generator, and the comparator. In reality, the digital word coming from the SAR represents a voltage, but in a mixed-signal simulator, the designer may choose to simulate the SAR with logic primitives or with a behavioral language such as VHDL. The output of a logic simulator is a state, not a voltage, so to integrate the logic representation with the transistors in the D-A converter portion of the circuit, the designer requires some way of mapping the digital states into actual analog voltages. Viewlogic has developed special software to handle this mapping in its Viewsim/SD mixed-signal simulator.

The SAR is a good example of a logic device that can be modeled with either logical primitives or a behavioral language. In the case of this converter, which was a benchmark model at an IEEE-sponsored event in September 1990, the VHDL description of the SAR took 80 lines of code that synthesized into about 300 gates. The synthesis software also generated a schematic of the synthesized gates. And even though writing 80 lines of VHDL takes less time than drawing 300 gates, the real benefit is that the VHDL synthesis process optimizes the gate-level design for either speed or chip area.



Complex designs, such as National Semiconductor's 8-bit successive-approximation analog-to-digital converter, challenge mixed-signal design tools. In this example, Cadence Design Systems' Analog Artist Mixed-Signal Simulation System partitions the analog and digital portions of the design. The center window shows the top-level schematic with the analog and digital signals highlighted. The top and bottom windows on the left show the next level of hierarchy below the top-level digital and analog blocks. The window on the right shows the mixed-signal simulation results.

Mixed-mode simulation must, therefore, take into account the actions and interactions of analog and digital models and the translation of terms between each technology. "A transistor, which is treated as an analog model, that's driving the input of a NAND gate, which is treated as a digital model, is a good example of interconnect problems," says Doug Johnson, vice-president of marketing and sales at Analogy (Beaverton, OR). "The transistor must know the input impedance and loading of the NAND gate so that the simulator can accurately predict the analog charging time. Unfortunately, digital models don't contain loading information at the accuracy level required for analog simulation. Likewise, an analog model doesn't contain the information to handle multiple logic strengths or unknown states."

To handle these conditions, whether in a common simulator or between two different simulators, Analogy has developed Hyper-Models. These models are automatically inserted at the boundary connections between any analog and digital models. They're implemented as analog models in Saber and contain the needed characteristics and translational data to interface specific analog and digital techniques.

Extracting parasitics

As clock speeds of MOS ICs reach 50 MHz and beyond, traditional analog problems—such as interconnect delays due to parasitic effects and signal coupling between parallel lines—are becoming problems for digital designers as well. Making software models of these complex effects is, however, a difficult task.

"High-speed designs dictate the need for sufficient parasitic extraction," says Dick Akers, director of the analog business unit in the simulation and test division at Mentor Graphics (San Jose, CA). "It's no problem for two nets of parasitic extraction to have hundreds of factors of resistance, loading and capacitance between them. So a design with 1,000 transistors could end up with 100,000 elements to be extracted."

Because such a large amount of data would slow most simulation systems to a crawl, the trick is to figure out which parasitic elements are relevant. "There's a lot of work going on to make parasitic extraction more efficient," Akers says. "Though all the effects that can be abstracted are real, some don't really affect your design. Trying to build that intelligence into a simulator is the key."

Many parasitic extraction tools on the market today use an averaging technique that examines worst-case scenarios and provides a profile of the effects of a certain net. While

certainly better than ignoring these effects, these methods can either overstate or underestimate the effect of a parasitic on a given circuit.

Sizing components

Analog design dictates the use of variable component sizes for design optimization. Specifying parameterized cells (Pcells) lets designers minimize the effort of editing and entering and reduces design-rule violations. "When you design a bipolar transistor or an analog CMOS transistor, the size and shape of it tends to be more complex," says Tom Quan, director of marketing for the analog division at Cadence Design Systems (San Jose, CA). "Being accurate when you're choosing the actual size of the transistor affects performance, and routing must be a consideration when you're connecting different component sizes. On a pin-to-pin trace, for instance, you might go through a different layer, and each one represents a different parasitic capacitance or resistance. A designer must match those traces so that there's a parallel path from one to the other."

"There's a lot of work going on to make parasitic extraction more efficient."

—Dick Akers, Mentor Graphics

Cadence's Analog Artist layout editor lets users parameterize layout data, change its length and width, and fold it into multiple segments or other configurations. For analog bipolar processes, Pcells can include arcs, circles, paths, and texts. With the editor, engineers can take drawn data and create stretched parameters, then compile from a menu button. The tight coupling of the schematic and layout editors helps translate Pcell information from design engineers to layout engineers.

"Traditionally the design and layout personnel are in different departments," says Cadence's Quan. "So if the intent of the designer is a certain type of transistor, tight integration of the tools ensures that the layout will match the schematic. So when a part is taken from the schematic and dragged over to the layout window, the correctly sized part will be available for placement. This eliminates a lot of errors."

Thermal effects considered

In addition to transmission-line effects and component size, thermal considerations also affect analog de-

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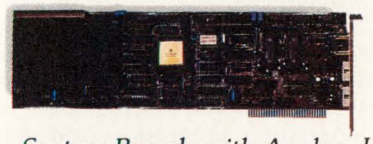
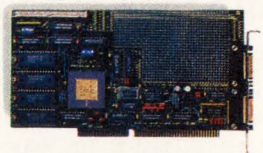
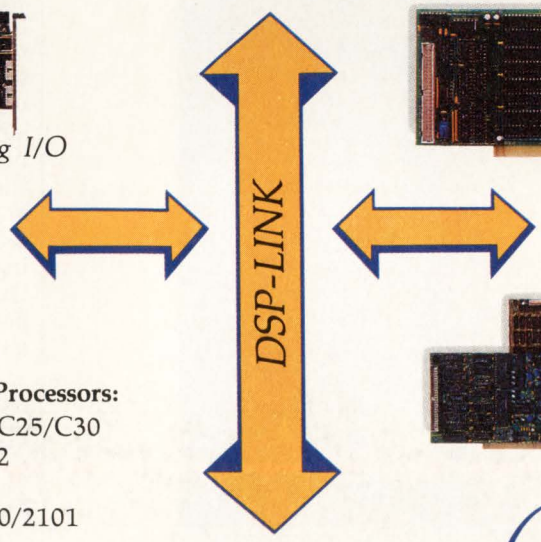
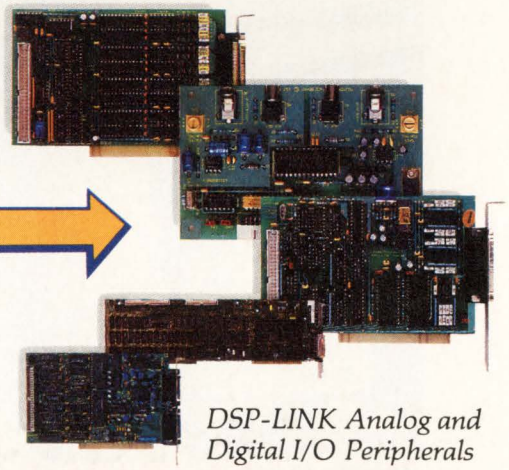


System Boards with Analog I/O



Processor Boards





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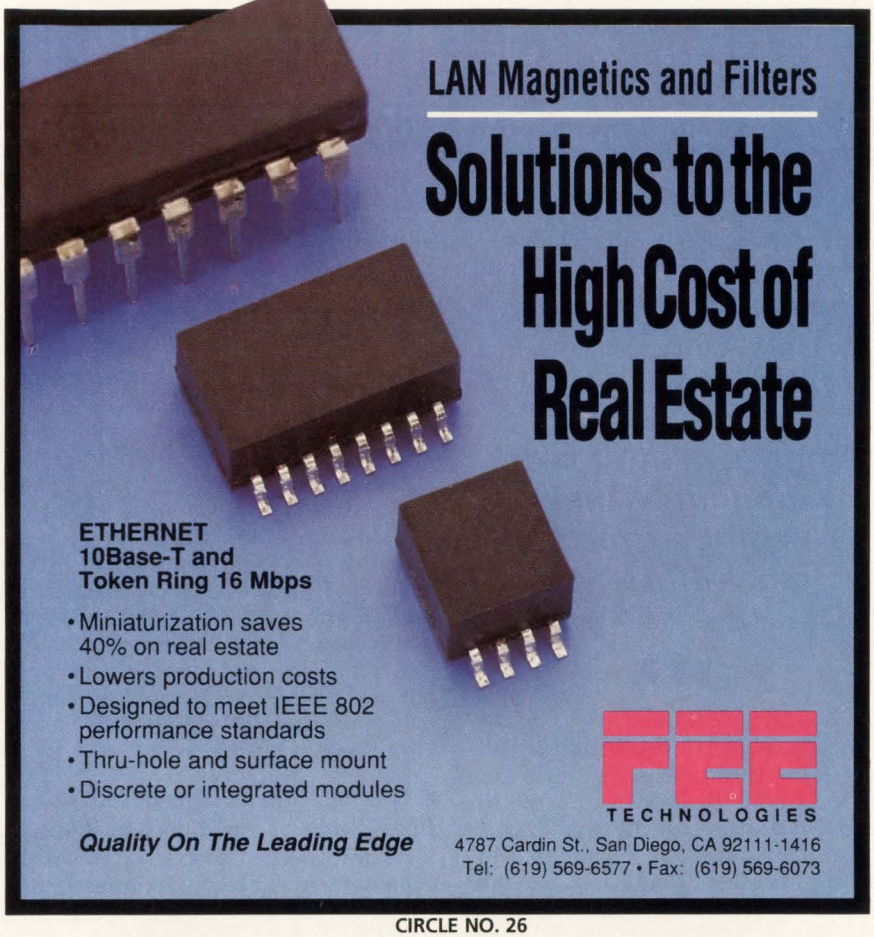

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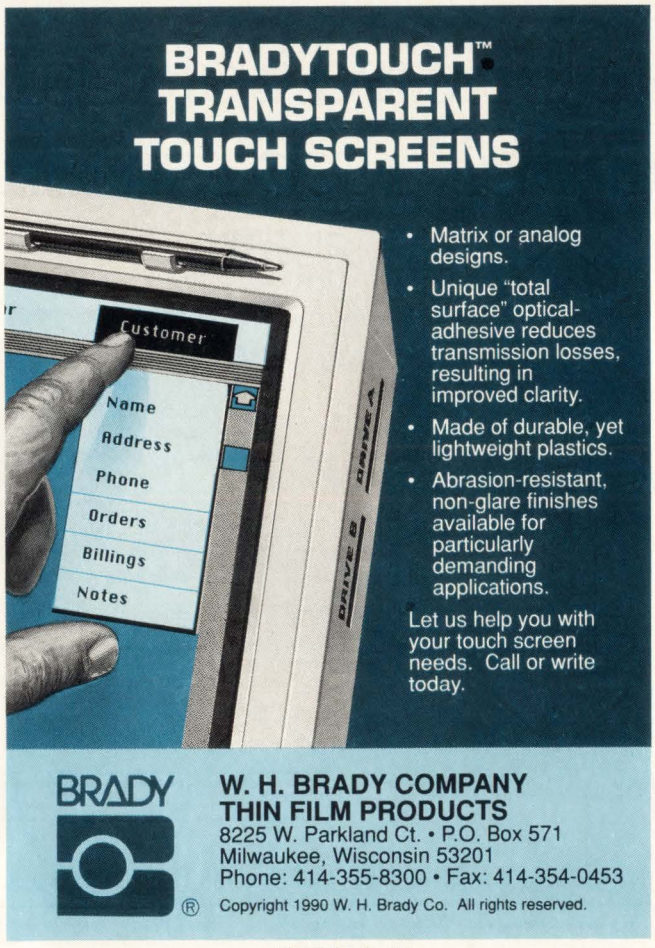

CIRCLE NO. 27

TECHNOLOGY UPDATES

DESIGN AND DEVELOPMENT TOOLS

sign. Though temperature considerations are important in any design, the necessity of keeping analog behavior as stable as possible makes thermal analysis especially important in analog layout.

"One of the terms in component placement has to be thermal behavior," says Quan. "Thermal symmetry over a line is important to ensure that the gradient is the same. In an op amp, for instance, the reference current source tends to be sensitive to temperature changes because the two transistors feeding the current source have to be exactly matched. While thermal effects in digital placement are important for reliability, they can be critical in analog design for performance."

"Tight tool integration ensures that the layout will match the schematic."

—Tom Quan, Cadence Design Systems

■ ■ ■

As clock speeds increase and geometries shrink, the problems that analog designs create for engineers will only get worse. Tool vendors are looking for ways to enhance their tool suites to address these problems without demanding excessive hardware overhead to run design and simulation programs. And for the near future at least, the expertise of the analog designer will still play a key role in efficient, high-performance designs. "There's no replacing a good analog designer," says Quan, "because there's too much expertise needed that today's systems and tools can't provide." ■

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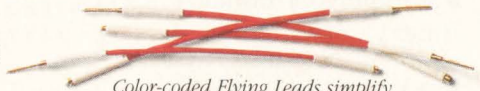

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CIRCLE NO. 28

INTEGRATED CIRCUITS

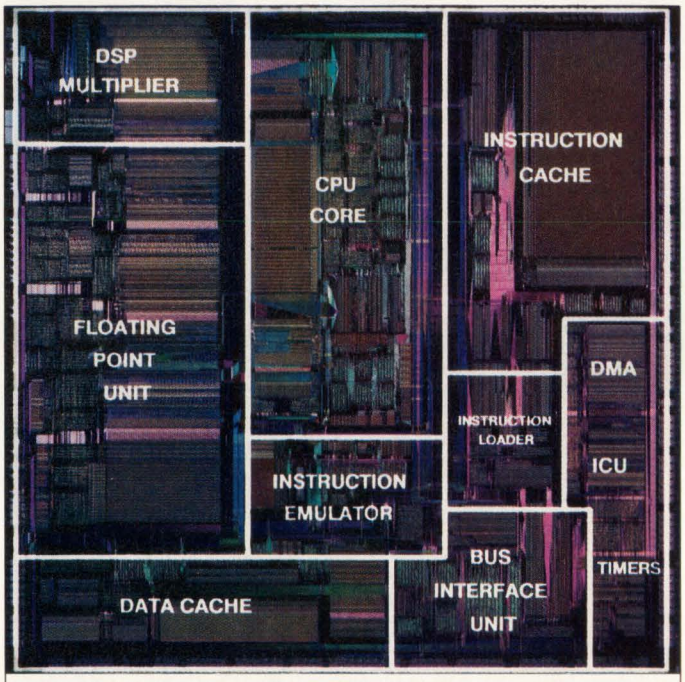
Embedded processor hits 100-Mips mark

Warren Andrews, Senior Editor

The RISC revolution has spawned a number of high-performance embedded processors vying for a competitive advantage in a fast-growing market. The winners of this race will earn a share in a market that's expected to top $1 billion by 1994. If today's performance is any indicator, National Semiconductor (Sunnyvale, CA) seems to have gained the pole position by releasing the industry's first 100-Mips processor.

"Swordfish, as we call the new processor, is more than just an embedded processor," says Phil Gibson, National's marketing manager, Imaging Business Center. "First, it combines both the function of a high-performance processor, using National's patented process, and digital signal processing functions on a single chip."

In addition, Gibson points out, the processor has many other features that let it be easily designed into a system. Further, he adds, "Swordfish is basically a core technology similar to our CG or GX products where peripheral functions can be added or taken away to tailor a chip to a specific application."



Swordfish integrates peripheral functions to ease systems design. The 64-bit data bus circuitry automatically configures itself to 8-, 16- and 32-bit buses and can operate at 25 or 50 MHz. The on-chip DMA controller supports two independent DMA channels, and the interrupt control unit supports 15 interrupt priority levels.

Winning performance

Bulent Celebi, group director of National's systems products, says the chip's processing power comes from a combination of its advanced superscalar architecture; its fast, double-level metal CMOS process; its added DSP functionality; its 64-bit data bus; and National's own optimizing compiler. "And while its performance tips the scales at the high end, other features such as a half-speed bus interface and dynamic bus sizing make it extremely easy to design with," says Celebi.

The real key to the 100-Mips performance is the chip's superscalar pipelined architecture. The pipelined execution unit includes two integer units that execute integer, control and load/store instructions. Each of the integer units uses a four-stage pipeline. The integer register file used by both integer units has six parts that let it read four operands and write two results for each clock cycle. Executing two instructions per cycle of the 50-MHz clock yields the 100-Mips speed.

In addition, integer multiply instructions allow a 32×32-bit multiplication in a single clock cycle for DSP applications.

These multiplications are executed on the floating-point multiplier, which also aids in performing complex number calculations by allowing for 16×16-bit multiplications in a single clock cycle, producing a signed 32-bit result.

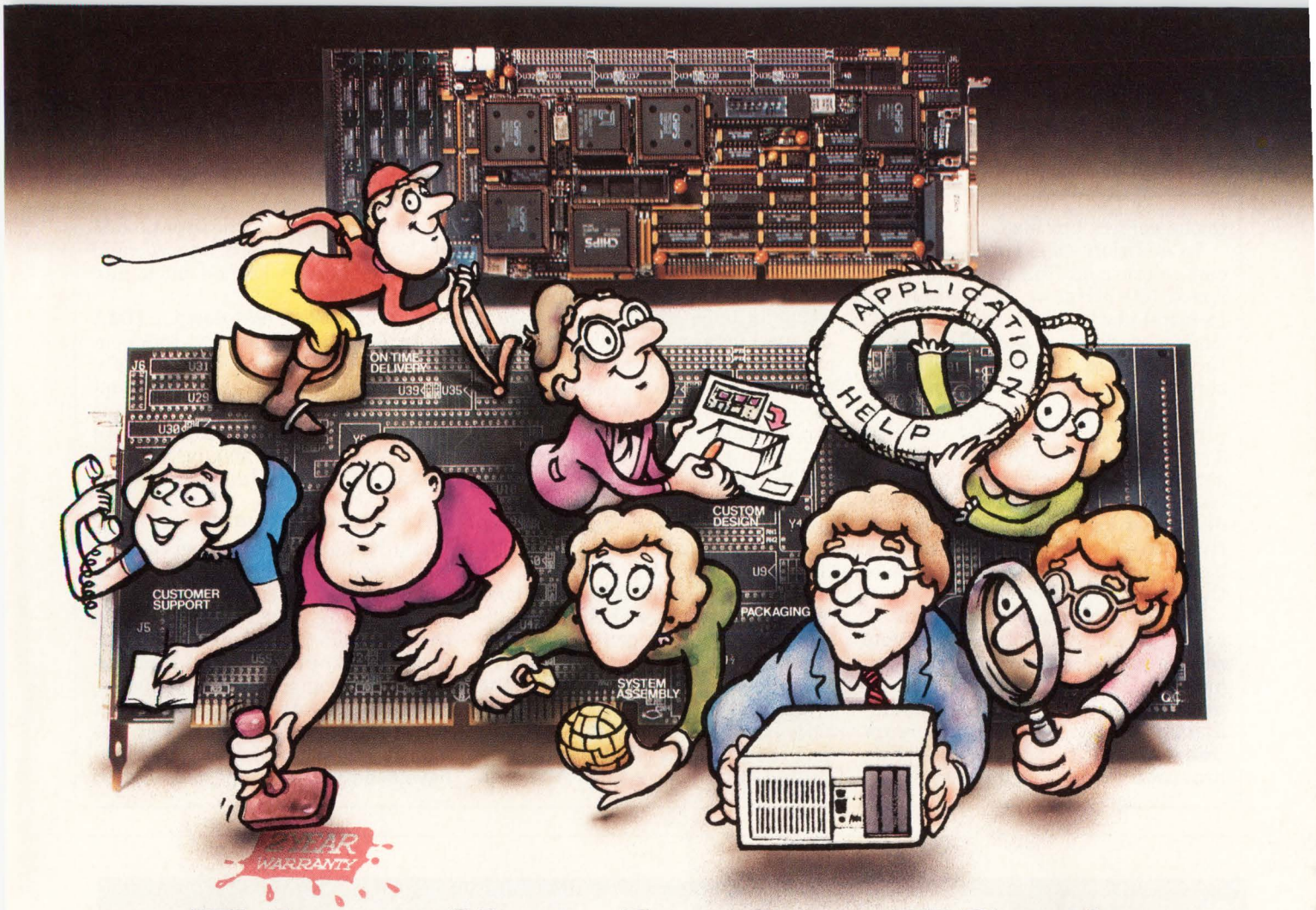
Floating point with DSP

The on-chip floating-point circuitry uses IEEE-754 format and provides single- and double-precision operations. Comprising an adder, an array multiplier and a divider, the floating-point unit allows a 32- or 64-bit result each clock cycle for addition and every other clock cycle for multiplication.

Although the 20-MFlops floating-point performance may not look as impressive as that of dedicated DSP machines, Gibson says tests have shown that Swordfish outstrips them in many real-world applications. "That's because the RISC and DSP architectures combine with the optimizing compiler (designed in parallel with the hardware) to provide both DSP and conventional processor functions—both of which are required in real-world applications," he says.

On-chip caches also play a significant role in Swordfish's performance. Both the 4-kbyte instruction cache and the 1-kbyte data cache are two-way, set associative. And because the processor may share memory with other processors in a system, it's equipped with bus snooping logic that tracks the external bus transactions and invalidates the appropriate cache line when data is modified in the external memory. The 4-kbyte instruction cache is large enough to hold a complete program in real-time applications where deterministic performance is required.

"Swordfish has been designed to provide ease of design into a variety of systems with a minimum of glue logic or other functional blocks," Gibson says. The 64-bit data bus, for example, supports an interface to 8-, 16- and 32-bit systems. Using a technique Gibson calls "dynamic bus sizing," the bus interface circuitry reads the pins on power-up and automatically configures itself



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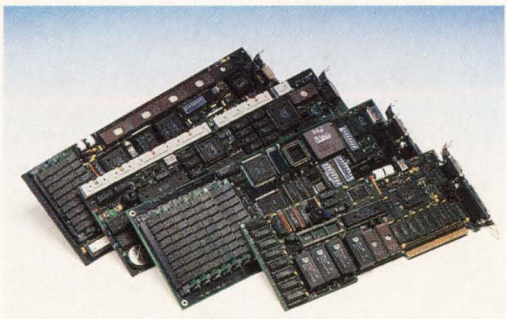

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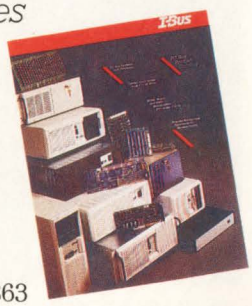

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to the correct bus size.

In addition, says Gibson, the bus can operate at full nominal clock speed (50 MHz) or at one-half the internal clock speed. All of the bus timing parameters are referenced to the bus clock. To allow the use of slower, less-expensive memory, the chip includes circuitry supporting pipelined and interleaved memory. This is done by allowing for two sets of control signals for two interleaved memory banks. In addition, dedicated logic can detect consecutive accesses to the same memory bank and then serialize access to that bank.

"Other system enhancements," says Gibson, "that both simplify and reduce cost of system design as well as enhance performance include an in-page output pin, serial communications port, DMA and interrupt control unit." In addition, he says, provision is made to lock-step processors for fault-tolerant operation. This same capability can be used to monitor the program counter when debugging software.

The in-page output pin flags consecutive access to the same DRAM page, allowing the system to take advantage of the fast-access page mode of DRAMs. The chip provides a page-batch input pin to tell the processor that the current access is to the DRAM space, letting it keep track of DRAM accesses even if they are mixed with other address spaces.

For in-circuit emulation, the chip offers a serial port that allows reading and modifying internal registers without affecting the internal states and contents of the caches. In operation, an input pin is signaled to stop or "freeze" the microprocessor. Next, the port is activated in the output mode, letting the contents of all registers be shifted out one at a time. After the registers are empty, the input mode of the serial port is activated, and modified data is shifted back into the registers.

To keep system cost down, a DMA controller supporting two independent DMA channels is built into the chip's circuitry. Also, the chip supports 15 interrupt priority levels through its on-chip interrupt control unit. For even more flexibility, a 16-bit timer is also included.

For embedded control

While National's Swordfish has the power and many of the amenities of a conventional RISC microprocessor, it's being targeted primarily at the embedded processor market. Swordfish is likely to find competition there from a variety of sources, most prominently MIPS and Sparc architectures. Within the past few months versions of both machines have been paired down and pointed

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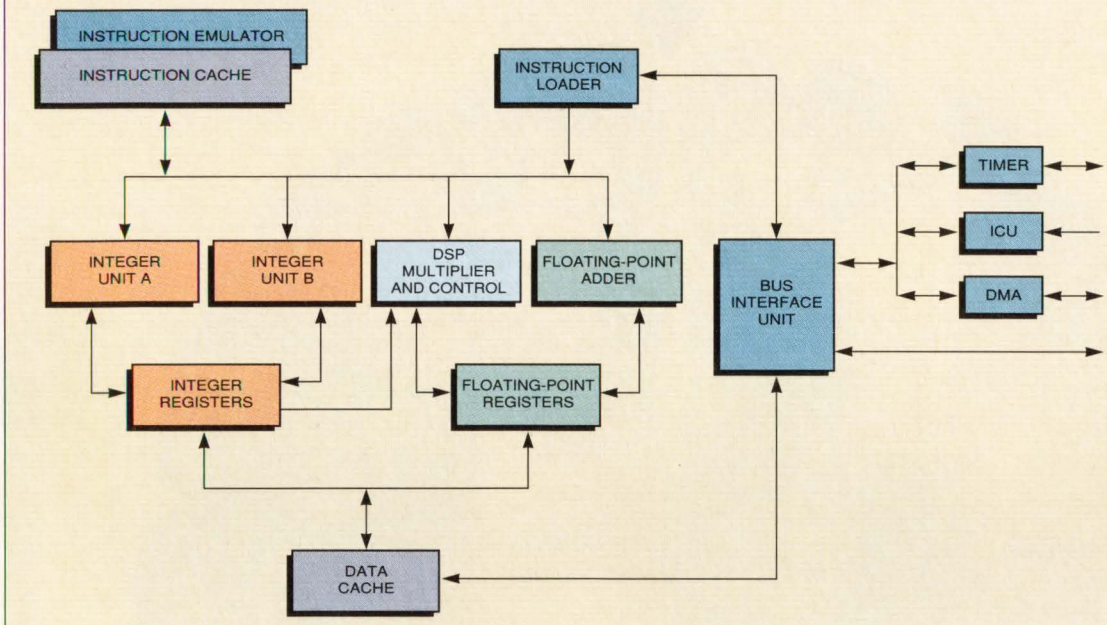
SWORDFISH PROCESSOR ARCHITECTURE



National Semiconductor's 100-Mips embedded processor, dubbed Swordfish, depends on a superscalar pipelined architecture for performance. The processor includes a pipelined execution unit, comprising two integer units, each with a four-stage pipeline; a floating-point multiplier, using IEEE-754 format; a DSP multiplier; and two-way, set associative caches for data and instructions.

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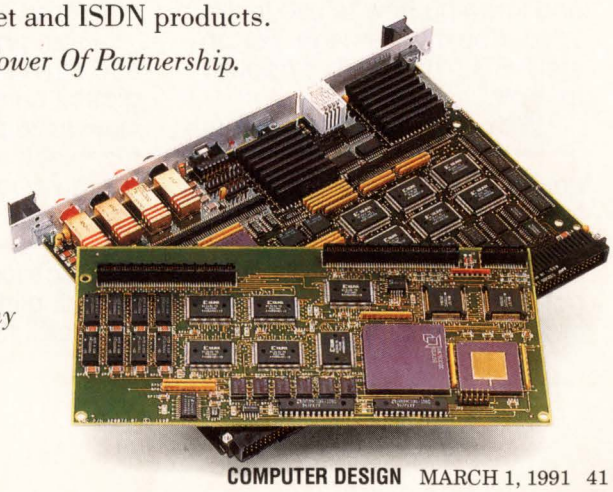

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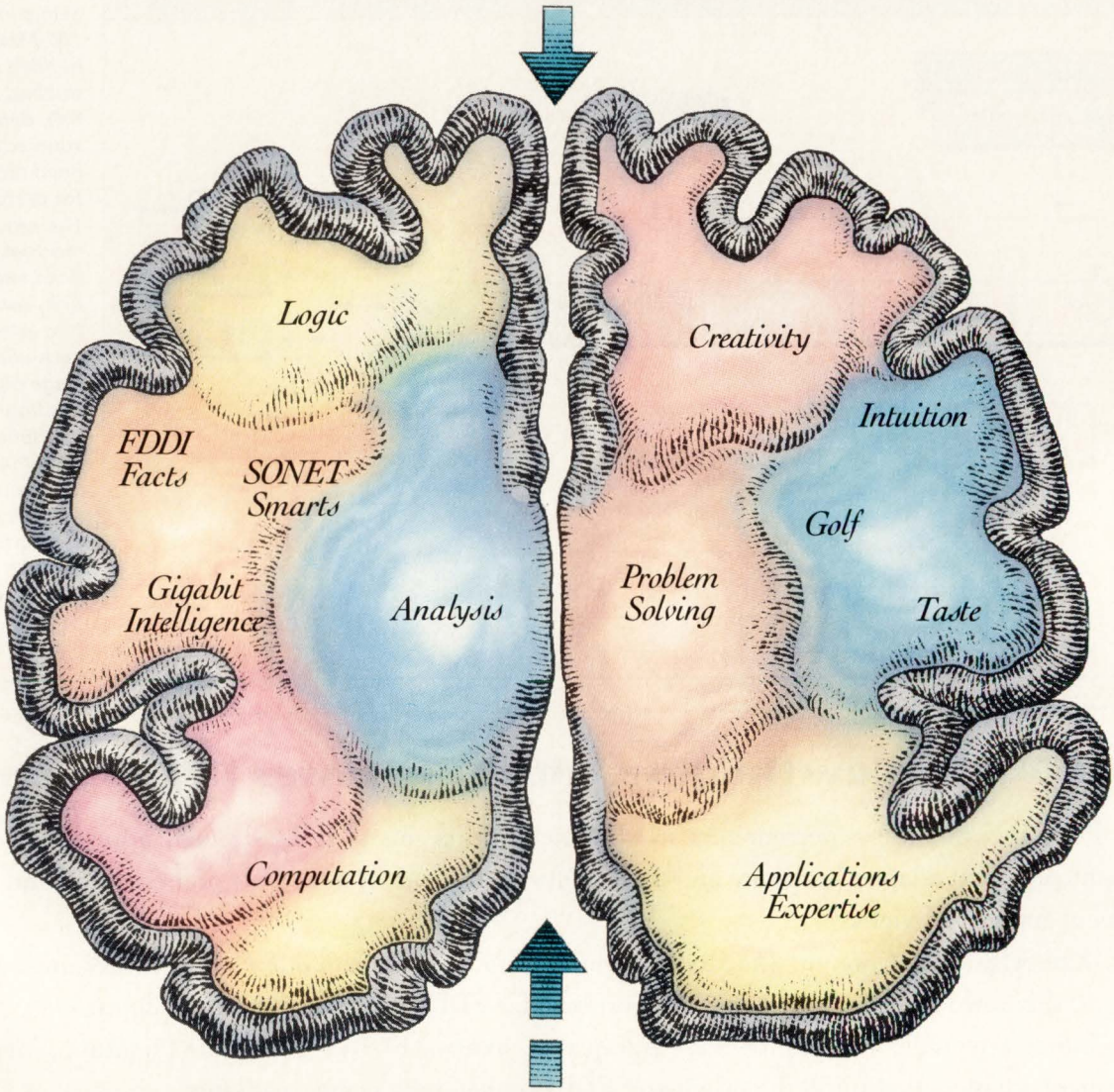

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at the embedded marketplace. Performance Semiconductor developed an embedded version of its MIPS machine, while LSI Logic had its equivalent in a Sparc architecture. Both are far below the performance level of National's device.

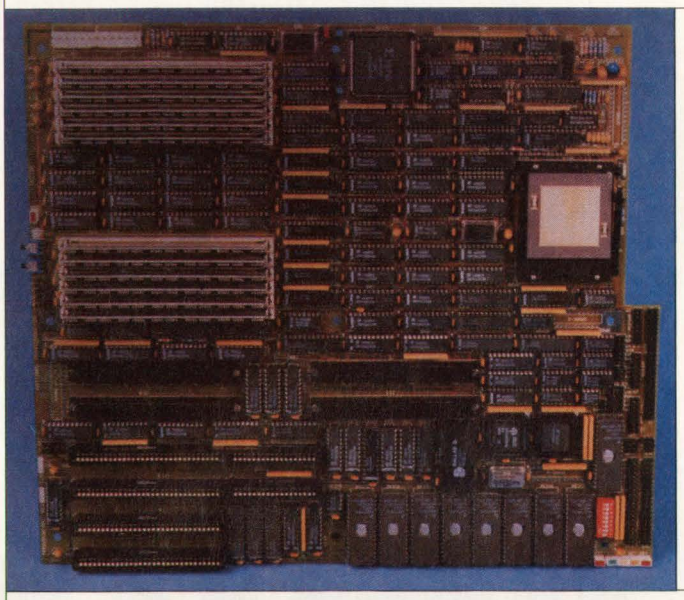
But other high-performance design alternatives are on the way. At last month's International Solid State Circuits Conference, a number of high-performance processors were presented, including a 100-MHz processor based on Intel's 80486 architecture; a 50-MFlops superpipelined data-driven processor from Mitsubishi; and a 65-MHz floating-point coprocessor (for a RISC processor) codesigned by Texas Instruments and Hewlett-Packard. In addition, MIPS Computer System recently unveiled its R4000 superpipelined architecture (see "MIPS rethinks RISC with superpipelining," *Computer Design,* Feb. 1, p 28), looking to a pipeline running at twice CPU speed to provide performance on the high end of the processor market.

Obviously features like on-chip DMA controllers, dynamically configurable bus sizing and on-chip interrupt controller do more than simply make a system designer's life easy. These features eliminate additional ICs and associated real estate, decrease design and assembly time, reduce end-product size, and increase reliability. Integrating these critical functions often reduces all-important time-to-market.

These advantages, however, account for only part of the gains achieved by the denser chips. National's Swordfish, for example, measures 13×13 mm—better than ½ in. per side—fabricated in a 0.8-µm CMOS process. On one hand, the chip is a milestone; on the other, it's an expensive hunk of silicon.

It, and others that achieve such exalted Mips ratings, will obviously find applications first where performance outranks price. Ultra high performance laser printers is one area that Gibson has mapped out.

An evaluation board and compiler for Swordfish will be available after this month. Volume chip production is scheduled for the third quarter of this year. ■



The evaluation board for the Swordfish processor will serve high-volume users as a development target and low-volume customers as an OEM platform. The board, available after this month, is designed to implement a complete embedded controller.

A fierce race

The race for the high-performance embedded controller slots is destined to become a fiercely competitive battle providing a broad variety of price/performance options. A key to the formula, one that National's designers have at least partially addressed in Swordfish, is overall system—rather than single-chip—cost.

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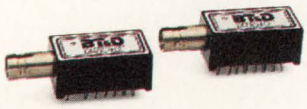

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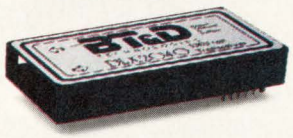

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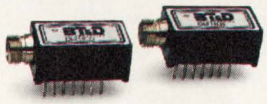

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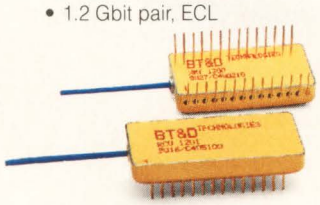

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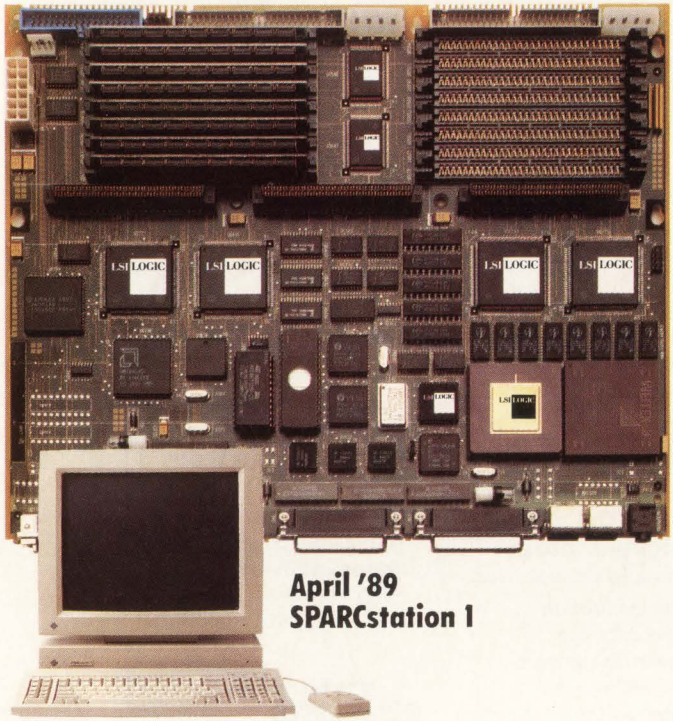

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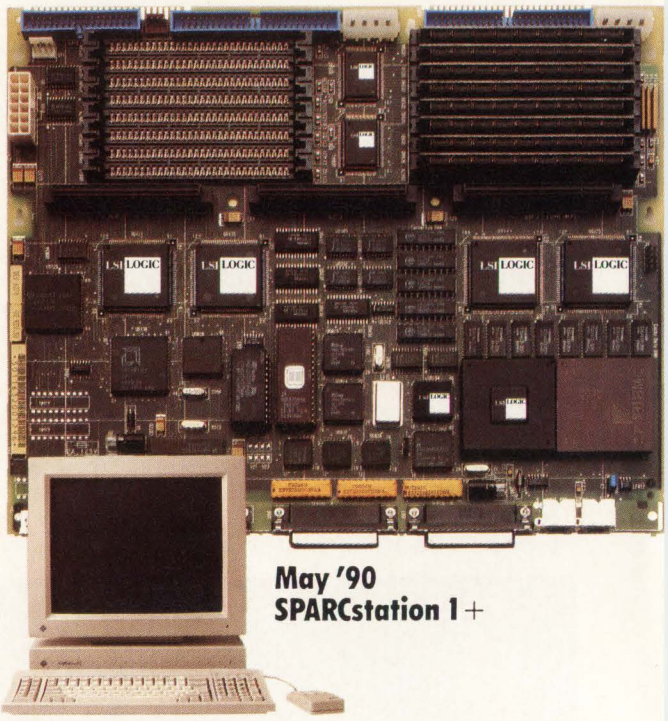

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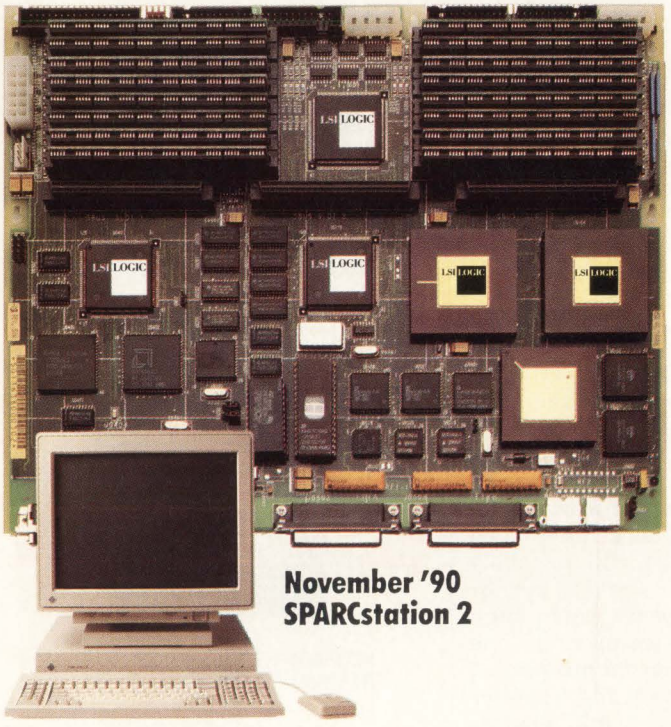

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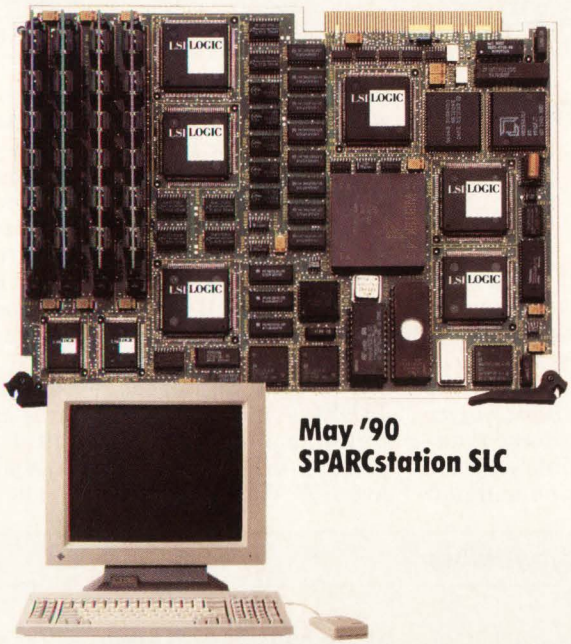

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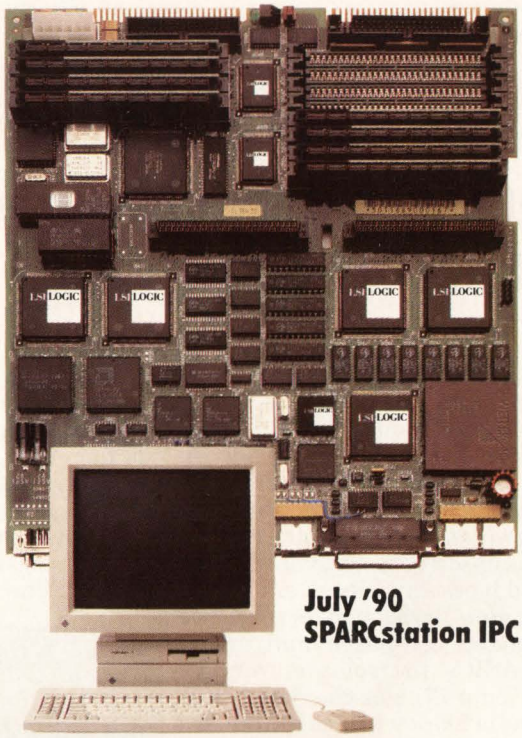

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CIRCLE NO. 32

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JEDEC committee proposes standard ASIC terminology

Barbara Tuck, Senior Editor

Rapidly changing ASIC design technology has led the industry to a point where a friendly discussion on the state of the art can lead to a heated battle over terminology. *Megacell, megafunction* and *megamodule,* for example, are all used to describe a cell-based, fully diffused block that's been embedded onto a gate array masterslice (see "Are mixed cell-based and array-based ASICs the solution vendors claim?" on p 77). For the time being, this type of block will lack a standard name, but the JEDEC ASIC committee is revising more-mainstream ASIC terms and definitions.

Committee chairman Allin Kingsbury, strategic marketing manager for ASICs at the Mitsubishi Electronic Devices Group (Sunnyvale, CA), reports that additions and modifications to the 12-1 standard are on their way to standardization. By press time, in fact, they might have cleared final ballot with the JEDEC Council.

Synthesis a major reason

It's not surprising that the definition of a field-programmable gate array (FPGA) is one that has been under discussion. The darlings of the ASIC arena, FPGAs are in an explosive growth stage. So much so, that wherever the term FPGA can somewhat reasonably be applied to a programmable device, it's being stretched to do so. The JEDEC ASIC committee has made a distinction between an electrically programmed gate array and a process-programmable gate array.

Much of the new terminology is synthesis-related since no one knew several years ago when the 12-1 JEDEC ASIC standard was drafted that synthesis would become the rage. With design complexity hitting tens of thousands of gates, synthesis has made a home for itself with the ASIC design community. Differentiating logic synthesis from silicon compilation was among the tasks taken on by the JEDEC ASIC committee.

As for array- and cell-based technologies, the trend toward on-chip application-specific blocks has led to a few terminology revisions. The definitions for *macro function / soft macro* and *macro cell / hard macro* have been reworded to make a distinction between a flexible vs. fixed layout. The word *function* will now imply a flexible layout, whereas *cell* will imply a fixed layout. And something new has been added—a standard definition of a module generator. In addition, there's a definition for a parameterized macro cell. The committee has even defined the library generation tool we call the module generator as that which creates a parameterized macro cell.

To order a copy of the revised 12-1 JEDEC standard on ASIC terms and definitions, call (202) 457-4971 or write to JEDEC, 2001 Pennsylvania Ave NW, Washington DC, 20006. ■

Some JEDEC ASIC terminology

Behavioral description Algorithms or equations defining a function.

Field-programmable gate array (FPGA) A gate array IC that can be electrically programmed. (Note: Process-programmable gate arrays are characterized by the ability to inventory partially fabricated wafers prior to interconnection.)

Gate equivalent (ECL) One-eleventh of the minimum circuitry necessary to implement a single-bit full-adder.

Geometric description A representation of a function in terms of its physical implementation.

Hierarchical description A description containing two or more nested levels of primitives.

Logic synthesis The process of transforming behavioral, structural, or register-transfer-level descriptions into structural descriptions based on a given set of implementation criteria.

Macro cell/hard macro A precharacterized fixed layout and interconnection of primitives that implement an electrical function. (Note: Precharacterization may be done either by measurement of fabricated devices or by computer simulation or by both. Precharacterization may include the following aspects: physical dimensions, logic functionality, testability, layout-rule compliance, ac and dc electrical performance, and reliability.)

Macro function/soft macro An interconnection of primitives and/or hard macros that implements an electrical function but has no predetermined physical layout.

Module generator A tool that, when given a high-level description of a desired function and relevant parameters, produces a specified implementation—for example, behavioral, structural, or geometric description, etc.—of the function used within an IC design. (Note: Some functions commonly produced by module generators are RAM, ROM, ALU, and data path.)

Parameterized macro cell A macro cell generated to meet one or more characteristics specified by the user.

Process-programmable gate array A gate array IC that is programmed as part of the IC manufacturing process.

Register-transfer-level description (RTL) A hybrid between a behavioral description and a structural description at the level of clocked registers.

Silicon compiler A design automation system that, when given a high-level description—behavioral, register-transfer-level, etc.—of desired functionality, will generate sufficient information for manufacture and verification of an IC design.

Structural description A definition of a function in terms of an interconnection of primitives.

Source: the JEDEC ASIC committee

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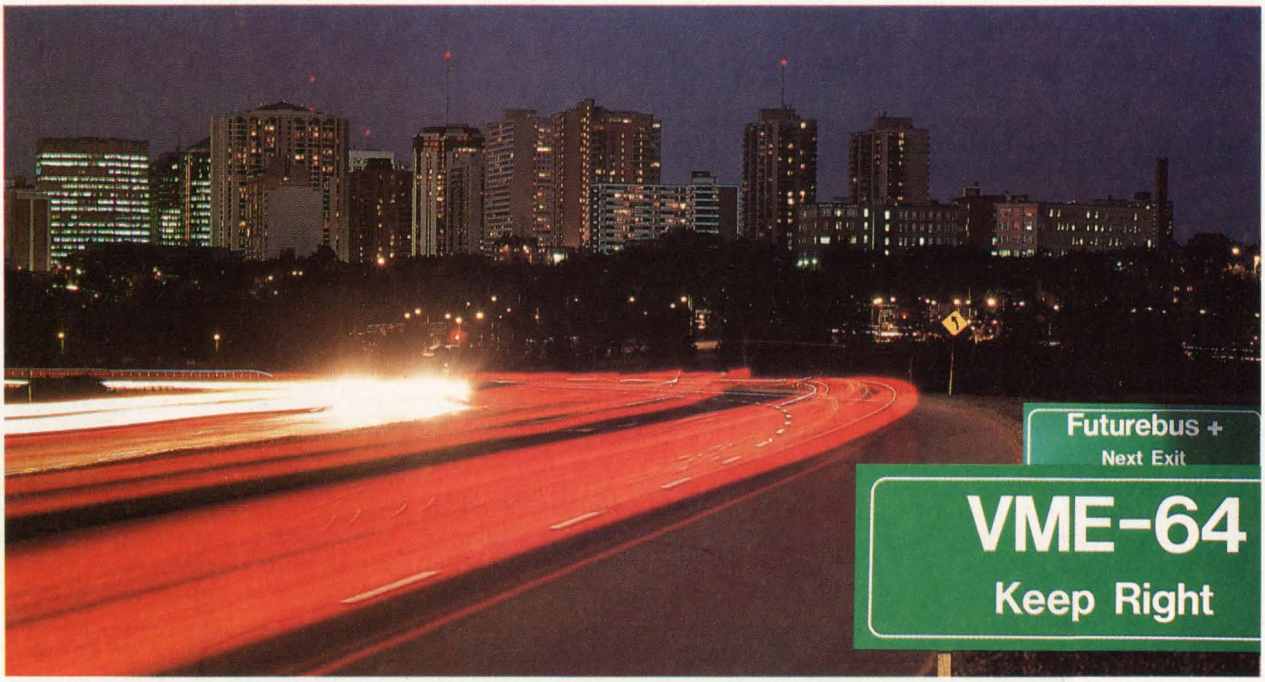

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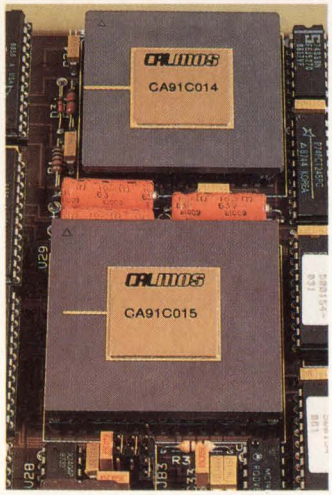

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CIRCLE NO. 33

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CrossCheck testability reaches commercial gate array family

Barbara Tuck, Senior Editor

It took longer than expected, but, more than three years after CrossCheck Technology (San Jose, CA) was founded, the first commercial silicon implementation of CrossCheck's ASIC testability approach is available from LSI Logic (Milpitas, CA). LSI has just begun to quote designs on the 1-µm CMOS LFT150K gate arrays with customized test structures embedded onto the base wafer for design observability and control.

The combination of on-chip test electronics and CrossCheck software tools, which have been integrated into LSI's Modular Design Environment, cuts the overall ASIC design cycle in half, according to LSI. The CrossCheck software performs test-pattern generation, fault simulation, and diagnostics. Once a circuit design is initialized and has functional patterns that toggle all nodes, claims LSI, 98 percent fault coverage is achieved in a very short time.

Can ASIC designers expect to get nearly total fault coverage for zero effort without paying a price? LSI's CrossCheck-based ASIC has, like everything else, an upside and a downside. The upside is that the CrossCheck approach carries with it the promise of no penalty to performance. On the downside, though, is a double whammy.

First, area overhead, to be expected with any design-for-test strategy, is between 20 and 25 percent on the initial LSI double-layer-metal masterslices. Based on LSI's LCA100K Compacted Array Plus gate arrays, the LFT150K masterslices range from 86,000 available gates with 37,000 usable and 270 signal pins to 190,000 available gates with 80,000 usable and 410 signal pins. The second whammy is that all the LSI R&D dollars, CrossCheck royalties, extra circuitry and silicon translates into a price premium of somewhere between 25 and 50 percent, depending on complexity, size, and volume of the design.

Is it possible that CrossCheck technology will help designers turn their LSI arrays around fast enough to compensate for such a price premium? "Absolutely," says Bill Alexander, LSI product marketing manager for advanced arrays, who reports that getting an ASIC to market even one day early could mean a return on investment of as much as a million dollars.

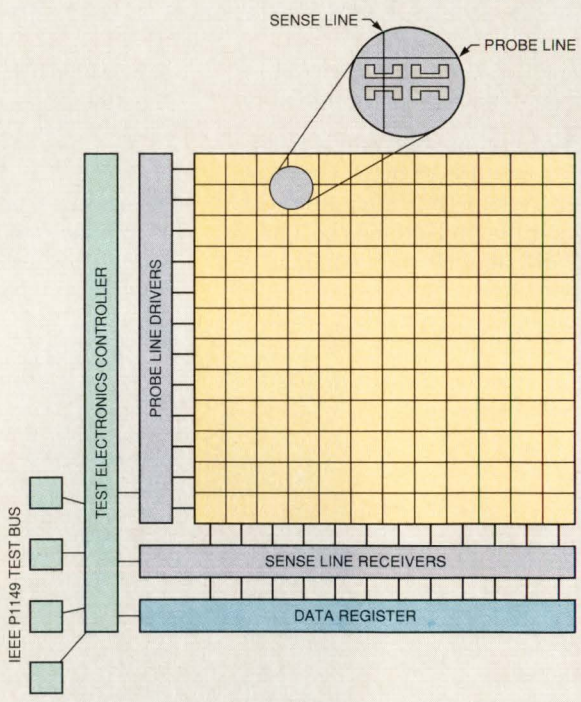
Up-front test no longer the issue

It's unlikely that any ASIC designer would deny that testability is eating up the biggest chunk of the design cycle. Designers are being bombarded with high-complexity test-critical designs requiring top-notch fault coverage, while management is increasingly demanding shorter design cycles. The result is that up-front design for testability is no longer the issue. Choosing which design-for-testability techniques to adopt is the issue.

Having followed LSI's lead in licensing the embedded test technology, Harris Semiconductor, the Advanced Device Center of Raytheon, Fujitsu Microelectronics, and Oki Electric Industry are also working side by side with CrossCheck to implement silicon. The partners have formed a specification group to promote a standard interface to all CrossCheck-based ASICs. The standard CrossCheck test access port will be used stand-alone or as a slave to a Joint Test Action Group 1149.1 test access port for board-level test. An application note and a JTAG soft macro will enable customers to build JTAG-compatible designs.

LSI first embedded CrossCheck test electronics into a 1.5-µm CMOS prototype more than a year and a half ago. After gaining some experience with CrossCheck's technology and implementing a few more designs, LSI applied the technology to its LFT150K gate array masterslices, which were fabricated in 1-µm technology at the re-

CROSSCHECK'S ON-CHIP TEST STRATEGY



When a design is placed and routed onto a base array containing CrossCheck test electronics, it's connected to the free terminals of the embedded sampling transistors. Each transistor has a probe line connected to its gate and a sense line connected to its drain, leaving the source free to be connected to a test point. The test electronics controller manages the data collected from the sense point array in the data register and interfaces to a four-pin testability bus.

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quest of customers. At present, LFT150K designers can use a 100-macrocell subset of LSI's LCA100K libraries. Prototypes will be shipping in June.

Massive observability is key to the CrossCheck approach. The two main components of the technology, which have to be built into the base wafer, are sense points and a test controller. Though details of implementation may differ from one CrossCheck silicon partner to another, the manner of dealing with CrossCheck silicon will be uniform for customers.

As interpreted by LSI in its LFT150K gate arrays, the CrossCheck technology involves a sense point array consisting of a probe- and sense-line grid, with the probe and sense lines orthogonal to one another. Small sampling transistors are located at each intersection of the probe and sense lines. The gate of each sampling device is connected to a probe line, the drain to a sense line, leaving the source free to be connected to a test point.

When a design is placed and routed onto the base array, the design is automatically connected to the free terminals of the sampling transistors. The resultant large number of test points are accessed through a 2-D addressing scheme. The results are then fed into a multiple-input linear-feedback shift register that compresses the test data on the sense lines into a signature. The test controller manages the data collected from the sense point array and interfaces to a four-pin testability bus.

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In addition to allowing a high degree of observability, the CrossCheck test methodology permits analog signal measurement of the test signals as well as signal injection into test nodes. So customers are rewarded not only with extremely high coverage of conventional stuck-at faults but also with high coverage of such fault modes as opens, shorts, stuck-open or stuck-closed FETs, and noise margins.

Other offerings

A leader in the military/aerospace market, the Advanced Device Center of Raytheon (Mountain View, CA) also has working silicon based on CrossCheck technology. Though its customer base is now limited to mil-

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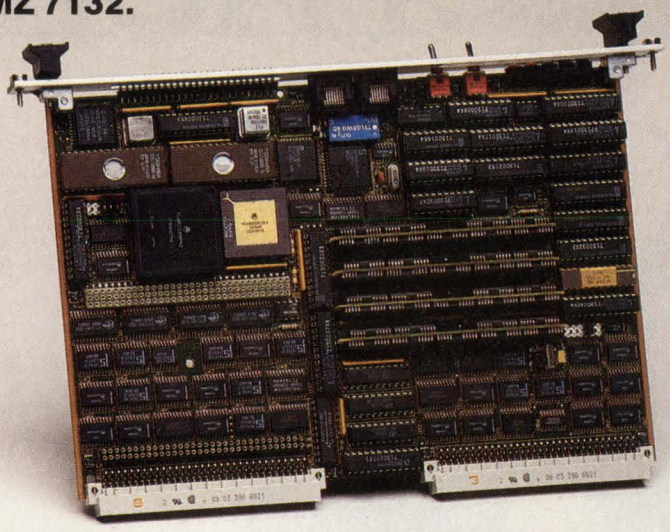

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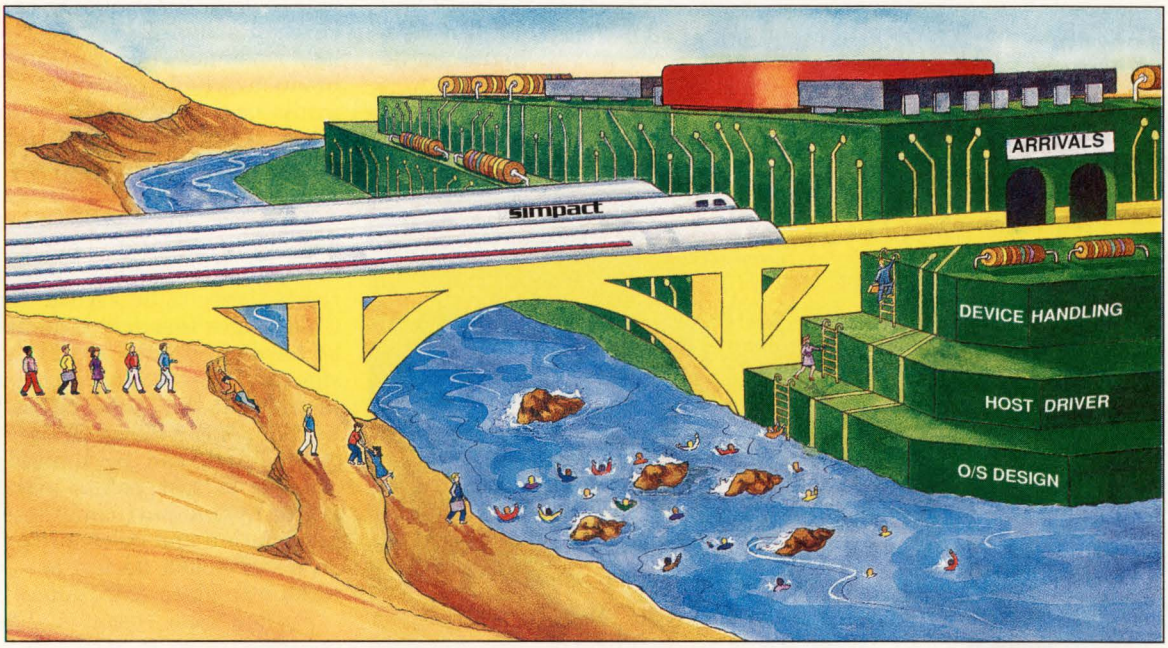

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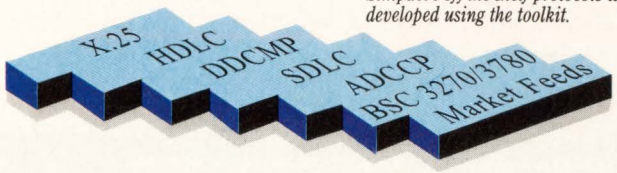

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itary users, Raytheon is considering whether to offer CrossCheck-based ASICs to the outside market. Like LSI Logic, Raytheon has gone with a CMOS sea-of-gates implementation, with an effective channel length of 0.7 µm (0.9 µm drawn).

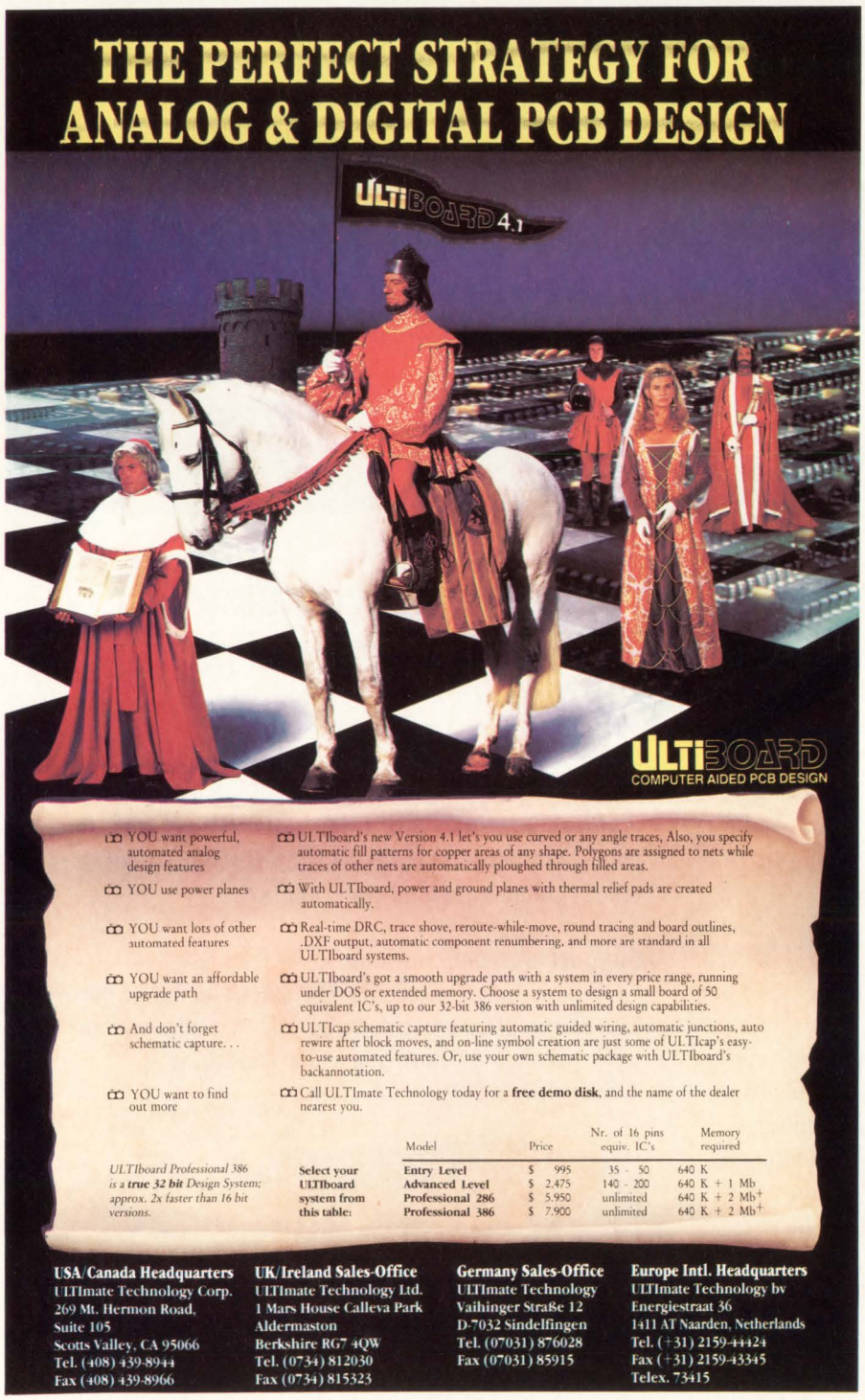
Design support engineering manager John De Falco expects that area overhead will be about equal to that of a design using scan methodology.

Harris Semiconductor (Melbourne, FL) is alone in its choice of a cell-based, mixed-signal implementation for CrossCheck silicon. In development, the cell-based design will be fabricated in a 19- or 20-V BiCMOS process technology that will accommodate analog capability. Director of design systems Nick English assumes that support for the product, which will most likely be available next year, will include compilers and a cell library. Harris will offer its product to military and commercial customers.

Area overhead for a CrossCheck-based ASIC is design-dependent. For instance, the overhead for a gate array is likely to be greater since the CrossCheck test grid structure must be hardwired onto a gate array design, and the test point total must be targeted at the highest possible utilization. A cell-based design, on the other hand, can be limited to the number of test points actually required by that particular design. The information and rules for test points on a cell-based design are incorporated into place-and-route software.

Fujitsu (San Jose, CA) hasn't yet decided how it will implement CrossCheck silicon, according to Sunil Wadwani, product marketing engineer for software. The company is considering a 0.8-µm CMOS array-based design for now, although a cell-based design may appear in the future. Fujitsu doesn't have silicon at present but is hoping to be defining designs with customers by the third quarter of this year; the target date for silicon is the end of the year.

Meanwhile, LSI intends to delay a decision on future implementations until it sees how the marketplace accepts the LFT150K gate arrays. LSI does plan to integrate CrossCheck tools into its Concurrent Modular Design Environment. Customers will also be able to use LSI's Silicon 1076 VHDL environment to design LFT150K arrays. ■



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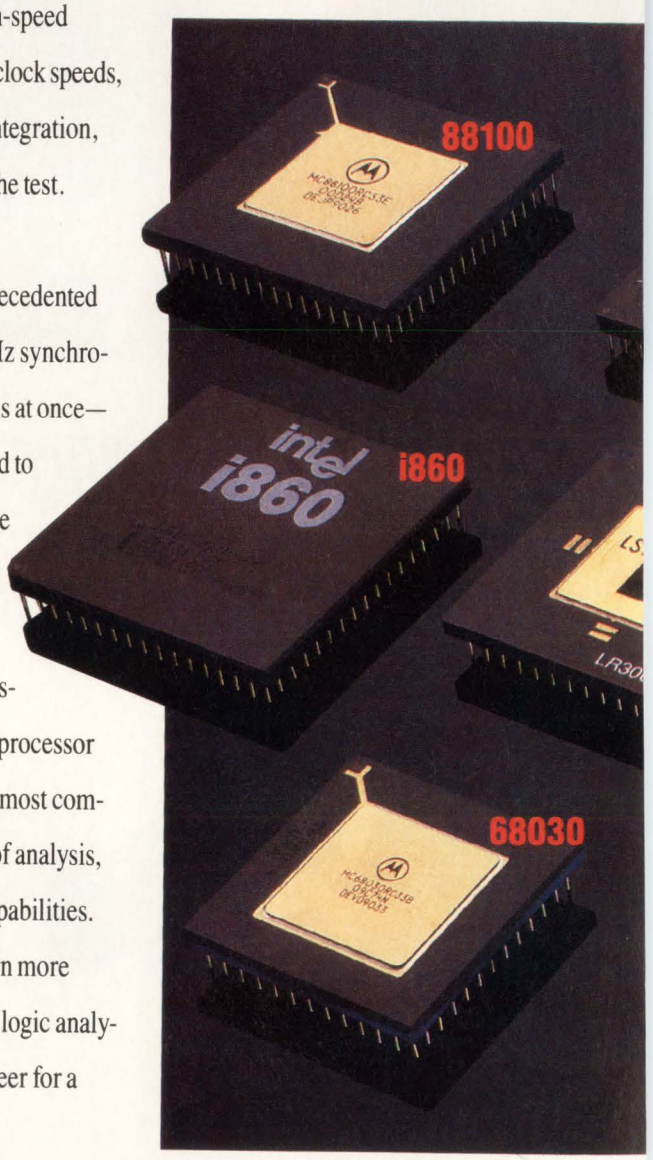

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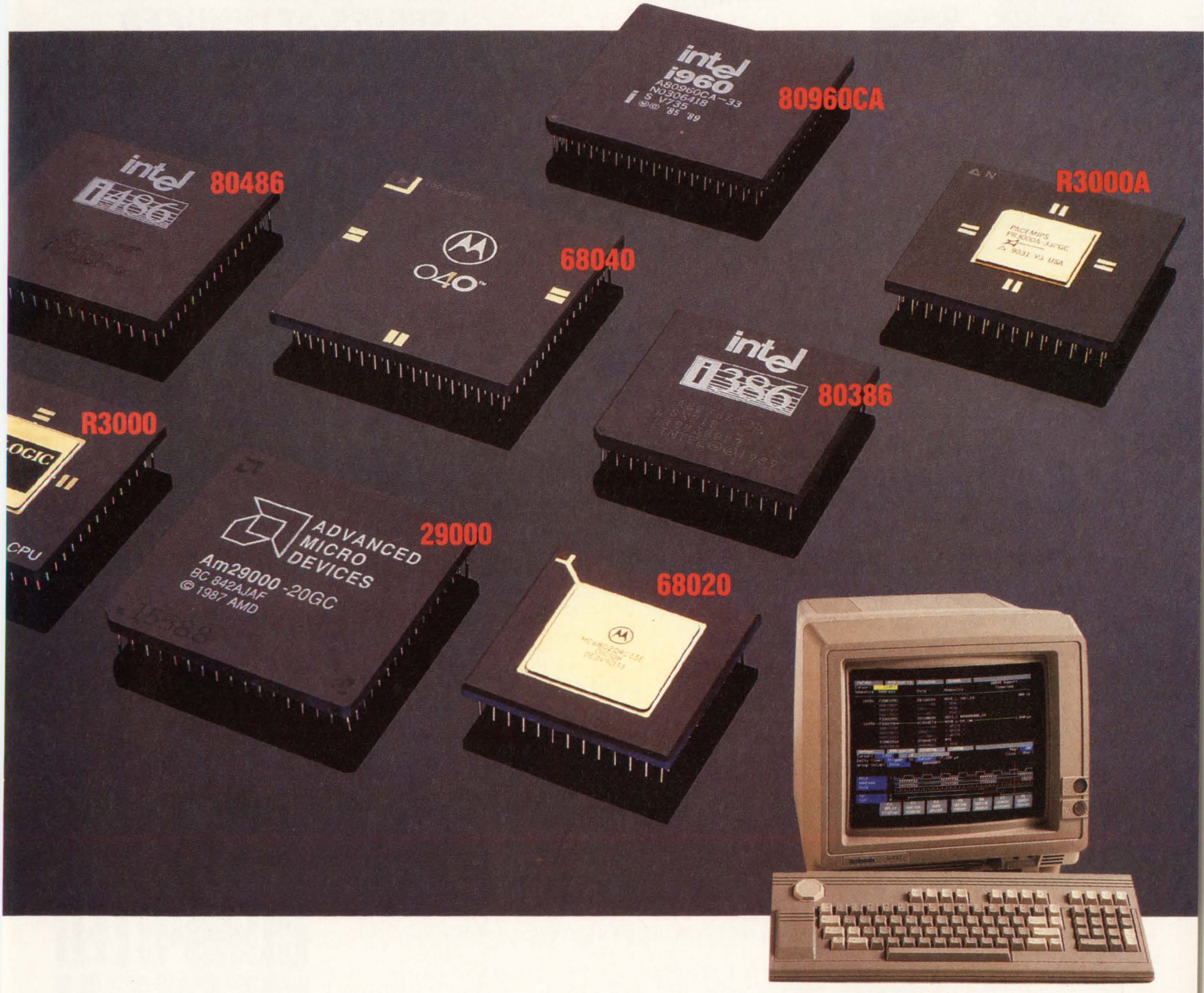

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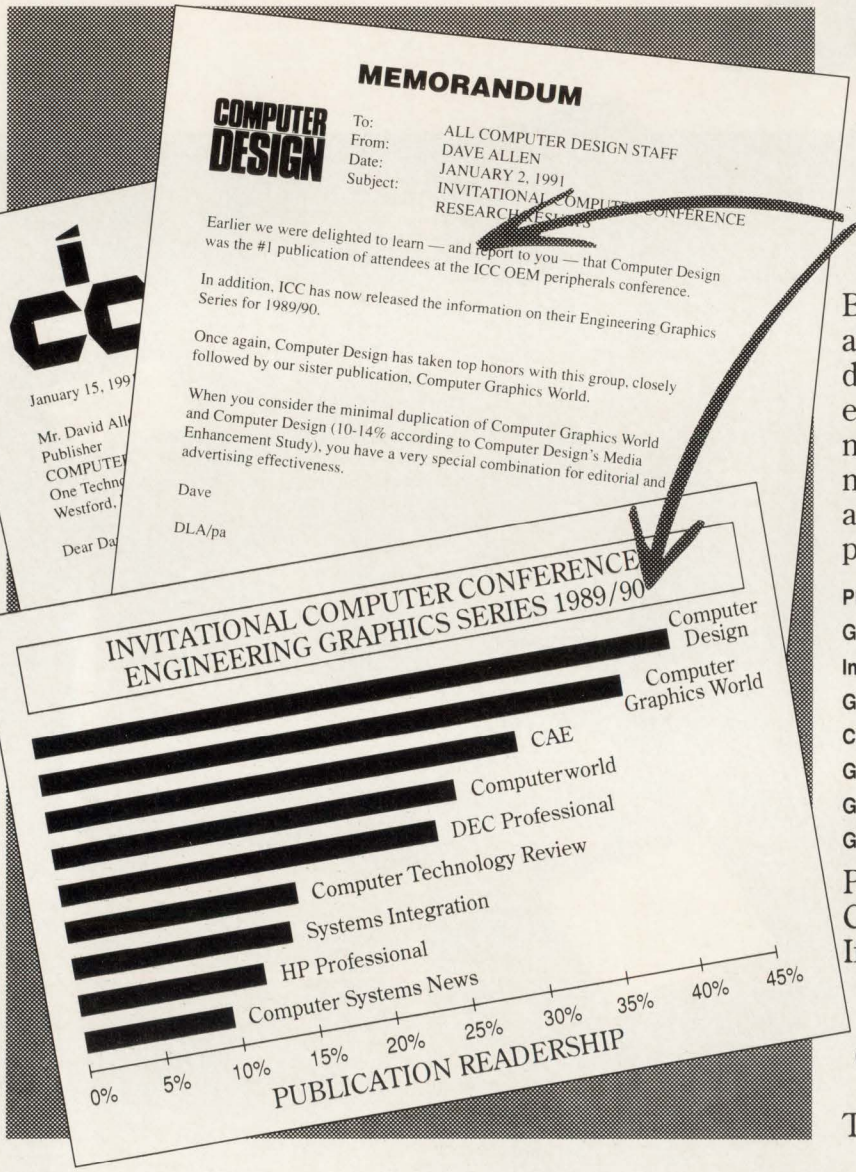

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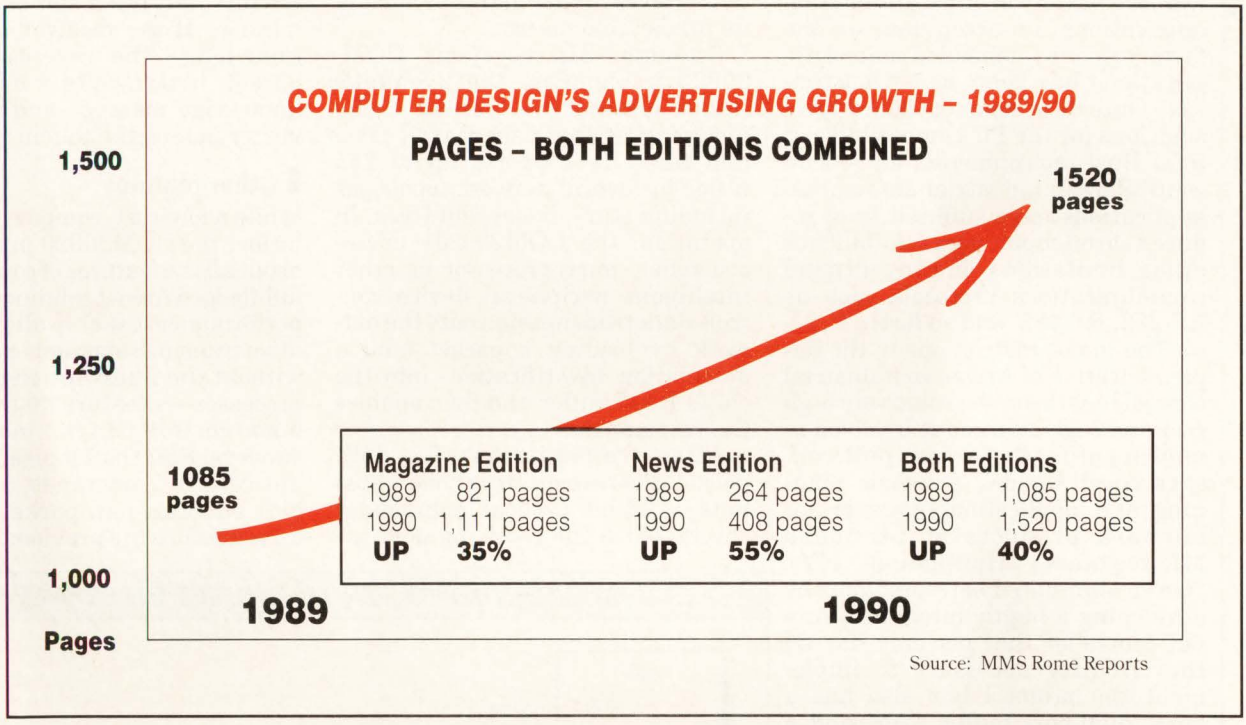

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CIRCLE NO. 70

INTEGRATED CIRCUITS

Single-chip controller eases Arcnet into industrial environment

Warren Andrews, Senior Editor

While Arcnet has been tremendously successful in a broad variety of office automation applications, its acceptance on the factory floor in embedded control applications has been somewhat limited. Outside of complete board-level solutions for the PC-compatible and STD Bus environments, embedded controllers in industrial automation applications have suffered from reduced throughput, poor reliability or other limitations of conventional communications protocols such as RS-232, RS-488, and so forth.

"The major restrictions to the implementation of Arcnet in industrial control have been the relatively high cost and high chip count involved in implementing the Arcnet protocol," says Ariel Hendel, strategic planning and application manager for network products at Standard Microsystems (Hauppauge, NY). "We've eliminated both problems by developing a highly integrated Arcnet controller that not only has all the circuitry necessary to implement the protocol but also has a large dual-port buffer RAM and a complete microprocessor interface."

With only two chips—the COM20020 Arcnet controller and a microprocessor—designers can now implement a low-cost Arcnet communications scheme. The controller, a 2k×8-bit dual-port SRAM buffer and glue logic all fit in either a 24-pin DIP or a 28-lead PLCC. By eliminating the external chips, Standard Microsystems has reduced the parts count by a factor of 5 as compared to conventional approaches, Hendel claims, and has cut the cost in half.

Why Arcnet?

Most conventional industrial networks depend on transmission rates that are often measured in kilobits per second—usually under 100 kbits/s. Arcnet, on the other hand, features a speedy transmission rate of 2.5 Mbits/s. In addition, because of its token-passing protocol, Arcnet provides a predictable worst-case response time that's critical for many industrial applications. Even when compared with Ethernet, Arcnet often receives higher marks because of its predictable nature.

Standard Microsystems' COM20020 implements the 2.5-Mbit/s Arcnet protocol over various media including twisted pair, coaxial cable and fiber. It supports up to 255 nodes in several network topologies including stars, buses and trees. In operation, the COM20020's microcontroller, microprocessor or other intelligent peripheral device controls data transmission onto the network by loading a packet (and a destination identification) into the chip's RAM buffer and then enables the transmitter.

After transmission of a data packet, the transmitting node transmits a 16-bit cyclical redundancy check, which the receiving node acknowledges if the packet was received successfully. The reception of the acknowledge message allows the transmitter to set the appropriate status bits indicating the packet transmission was successful. An interrupt mask permits the COM20020 to generate an interrupt to the microcontroller once the status bits indicate a successful transmission. If the receiver fails to acknowledge the reception of the packet, it transmits a negative acknowledge message and the transmitter passes the token.

Other features

While a low-cost, compact Arcnet solution, the COM20020 provides just about all the features of conventional, full-fledged Arcnet solutions. To speed performance, the chip allows consecutive transmissions and/or receptions without the intervention of the host processor—a feature known as command chaining. In this mode, a dual, two-level FIFO buffer pipelines transmit/receive commands and status bits, enabling new packets to be received before the previous packet in-

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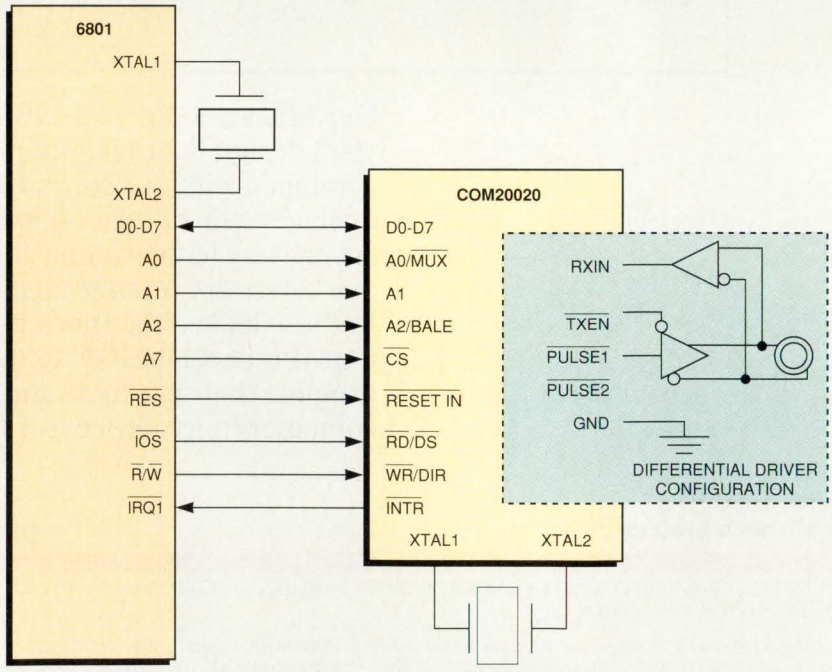

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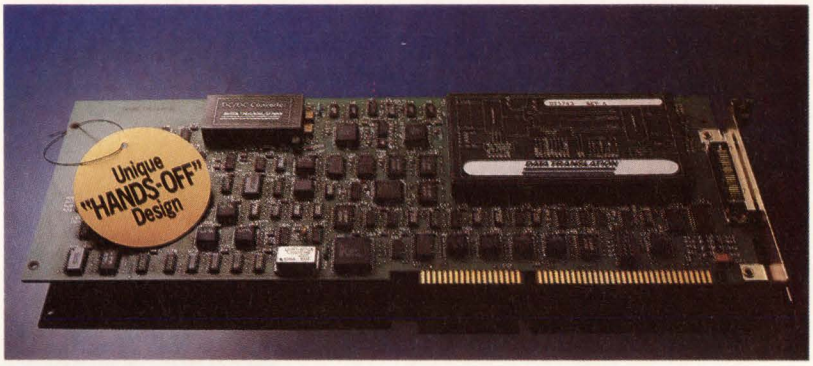

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terrupt is acknowledged and serviced. Such command chaining guarantees that a buffer will always be available for reception of a data packet, thus eliminating wasted tokens on the network.

Another of the chip's features that maximizes flexibility and enables nodes to adapt to network changes is the automatic reconfiguration protocol. Whenever a new node is turned on, the COM20020 transmits a reconfigure burst. The burst is also activated whenever a node fails to receive the token after a predetermined period, or after a software test. The reconfiguration burst destroys the token and prevents any other node from gaining control of the line, and then automatically reconfigures the network.

Also, the network automatically reconfigures when a node leaves the network. But this reconfiguration doesn't require destruction of the token, or a temporary halt of network activity. An active node senses that another node has left the network when it's unable to send the departed node the token. On receiving no response, the sending node bypasses the unresponsive node and reconfigures the network by incrementing its destination node ID number until the ID number matches that of the next highest active node.

Memory is key

According to Hendel, the inclusion of the 2k×8-bit, dual-port static memory is key to both the COM20020's performance and the reduced parts count in systems using the COM20020. "In conventional systems," he says, "it's been necessary to use external buffer memory and some cumbersome associated multiplexed address/data bus schemes." Furthermore, he adds, such approaches require control interfaces and additional glue logic such as latches.

By integrating the RAM on-chip, Standard Microsystems has been able to reduce the Arcnet function implementation area by as much as 50 percent. In normal operation, the on-chip RAM is partitioned as four 512-byte pages, two each for transmit and receive. For applications that use smaller packet sizes, the memory can be partitioned into any combination of 256- and 512-byte pages. When smaller packet sizes are used, the additional memory can be freed up for use as scratch-pad storage.

Putting the RAM on-chip also speeds memory access significantly, since the dual ports arbitrate between the Arcnet function and the associated microcontroller/microprocessor. This arbitration takes place in a single clock cycle with no wait states and independent of the network data rate. In discrete approaches, accessing memory in a

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CIRCLE NO. 43

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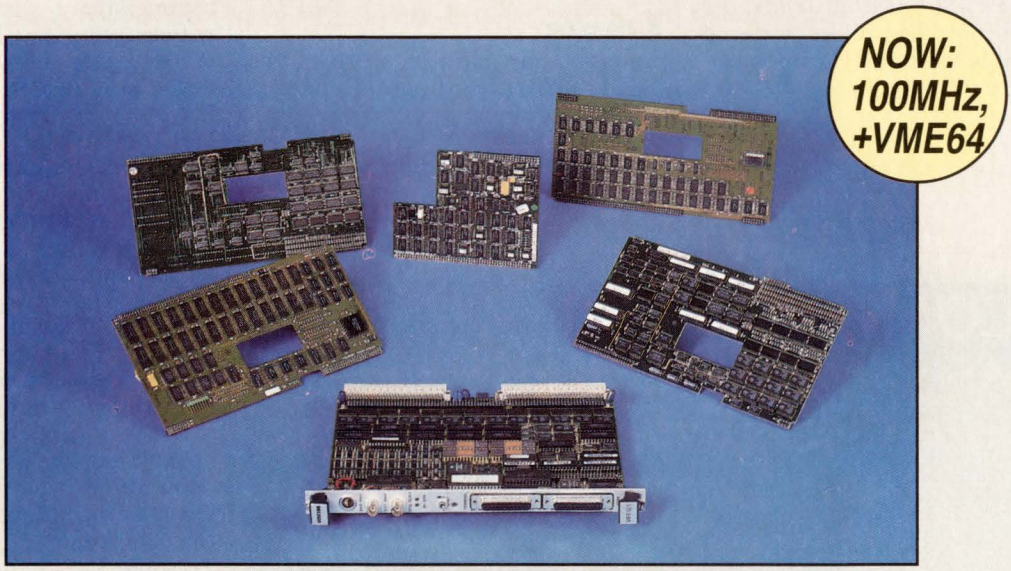

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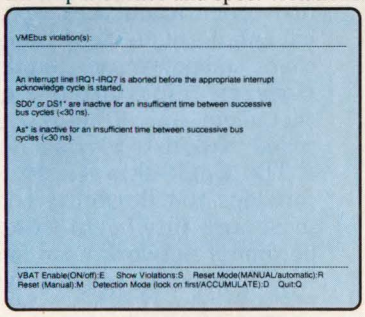
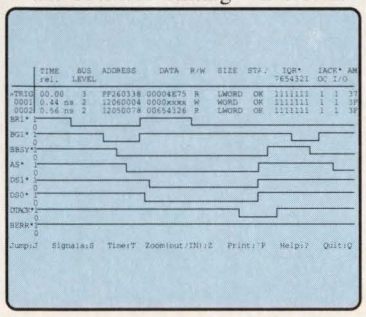
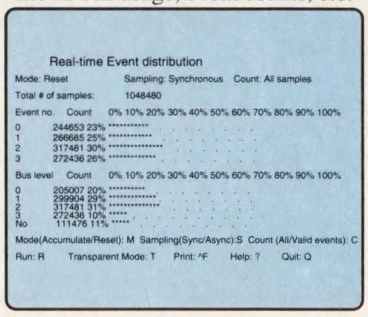
VMEbus Anomaly Trigger reveals incompatibilities and spec. violations.



Combined VMEbus State trace and 100MHz Timing Waveform.



Real-time VMEbus histograms shows bus usage, event counts, etc.



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INTEGRATED CIRCUITS

single cycle degrades the processor performance. Because most microcontrollers have no ready line, the LAN controller that handles arbitration and microcontroller address decoding is unable to extend the microcontroller's read/write cycle. To work with slower memory, the microcontroller must therefore operate at a slower rate.

No glue

Another important feature of the COM20020, according to Hendel, is its universal interface. This interface comprises an 8-bit data bus, an address bus and a control bus. To accommodate a variety of controllers without additional logic or greatly increased pin count, the COM20020 automatically detects and adapts to the type of microcontroller interface being used. This automatic adaptation occurs on hardware test, where the chip's circuitry first determines if the read/write control signals are separate signals such as in the Intel 80XX family, or direction and data strobe signals such as in the Motorola 68XX family. Once the signal type has been determined, the chip remains in the assigned mode until the next hardware reset.

Arcnet's support of various media is particularly useful in industrial applications, where factors other than basic performance are often major considerations. Fiberoptic lines, for example, may be required for safety in explosive atmospheres, or other types of cable may be needed to resist abrasion or other effects of harsh industrial environments.

Where long transmission distances are involved or where other networks use a transceiver interface, a conventional Arcnet transceiver interface can be used. This requires a hybrid transceiver that transfers pulse-code data between twisted pair or coaxial cable. Because the transceiver uses transformer coupling, it provides excellent isolation and common-mode rejection.

For cost-sensitive, short-distance applications such as backplanes and instrumentation, the chip provides a backplane mode that reduces parts count and power consumption. In this mode, the chip is directly connected to the media, and straight, rather than coded, NRZ data is transmitted.

The single-chip Arcnet controller provides the flexibility to allow almost any intelligent subsystem to become a network node for monitoring, updating or control. Wide availability of the chip is likely to further ingrain Arcnet in the industrial arena. ■

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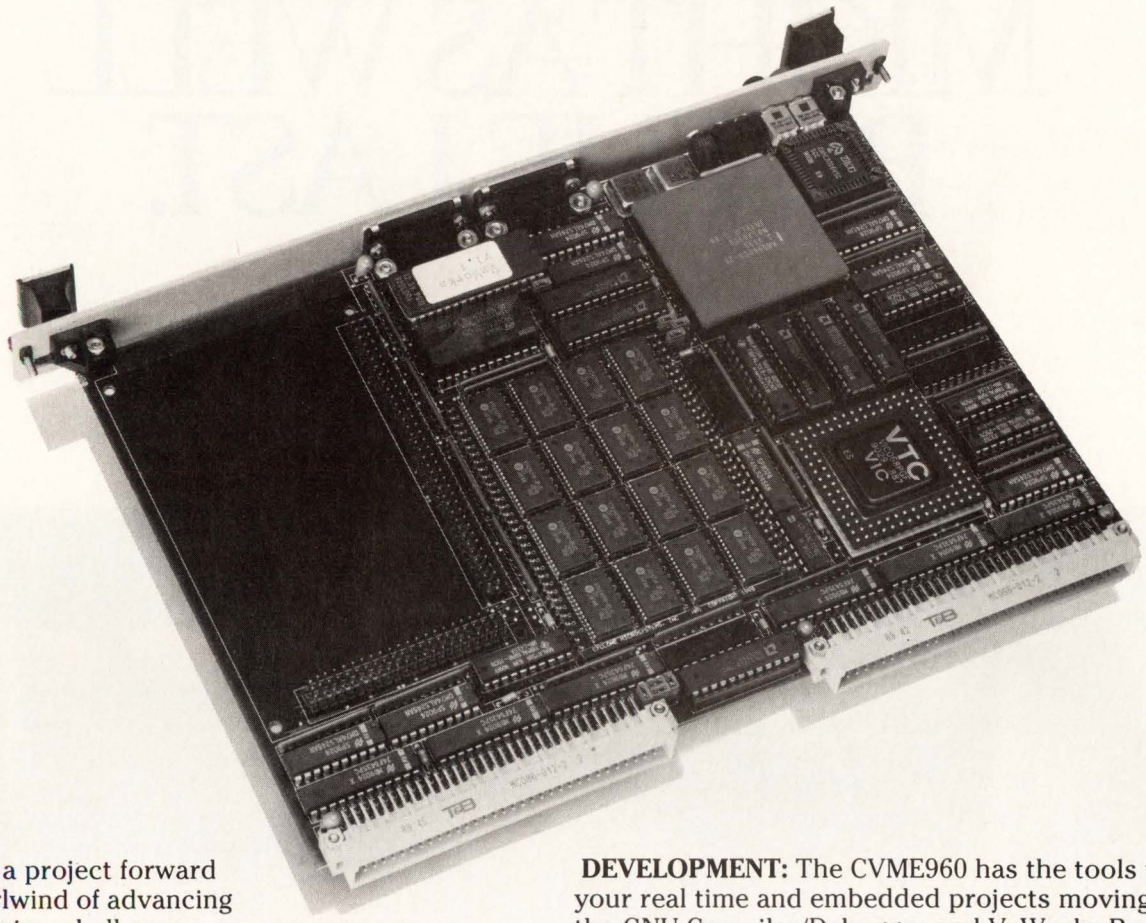

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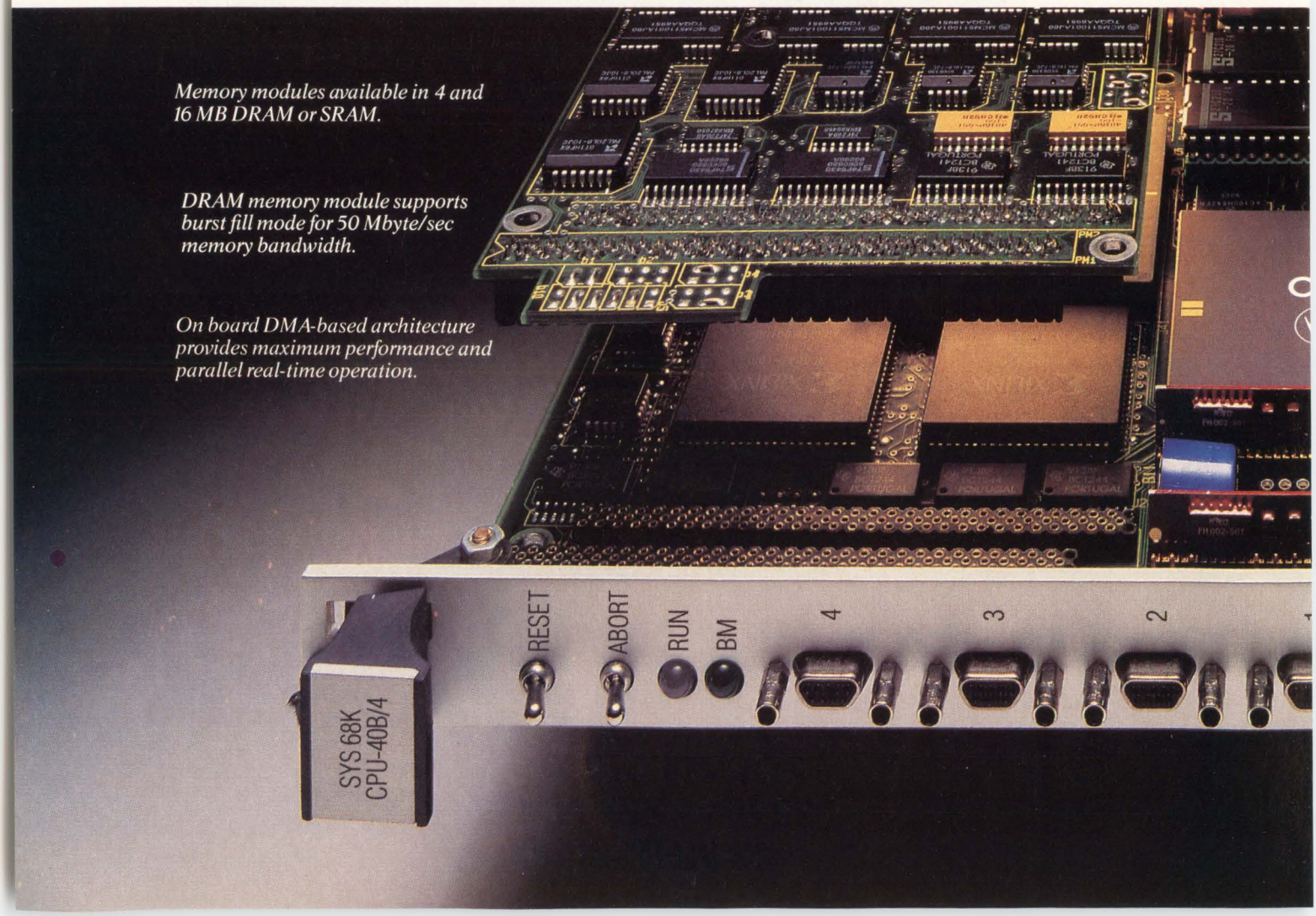

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Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

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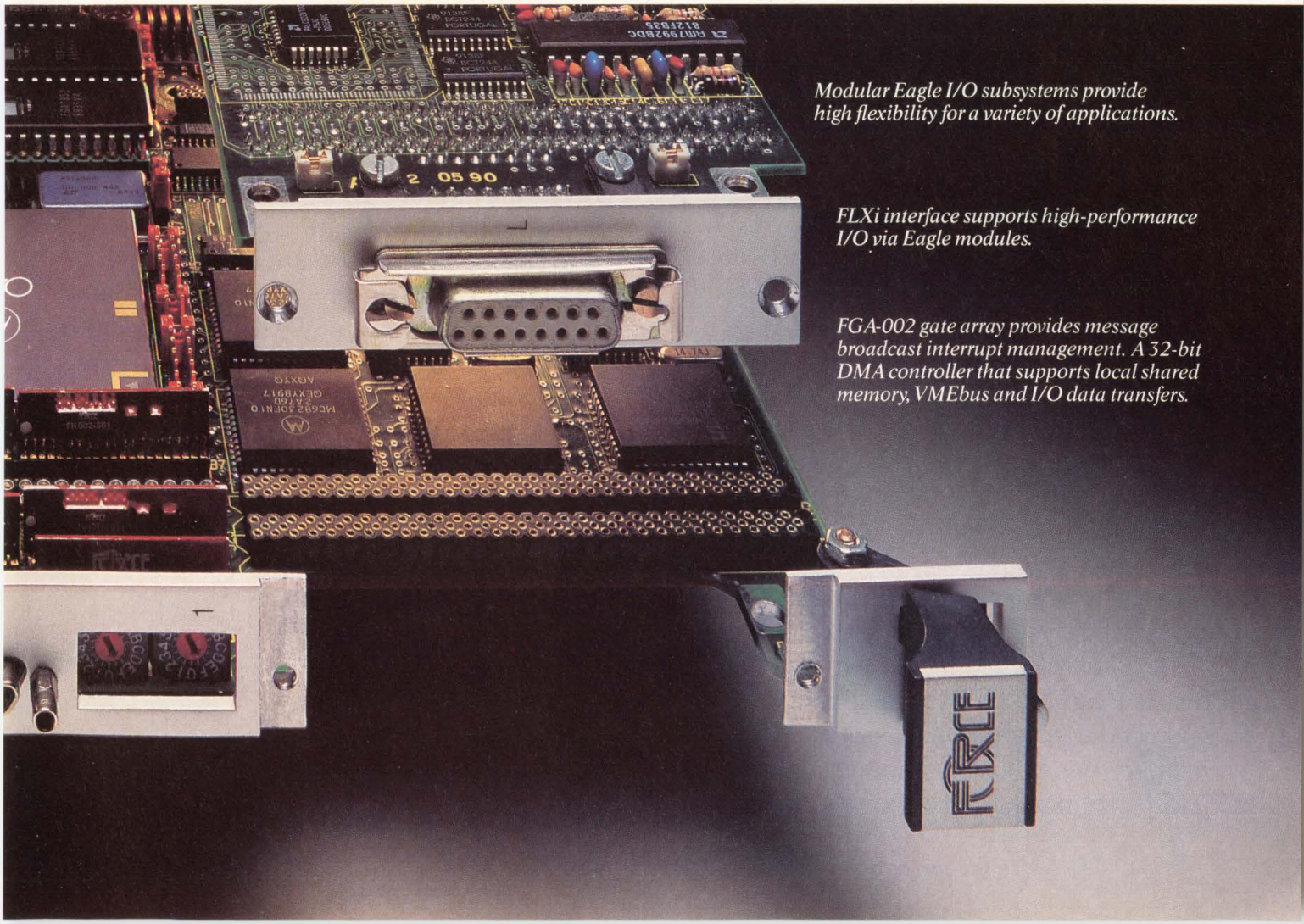

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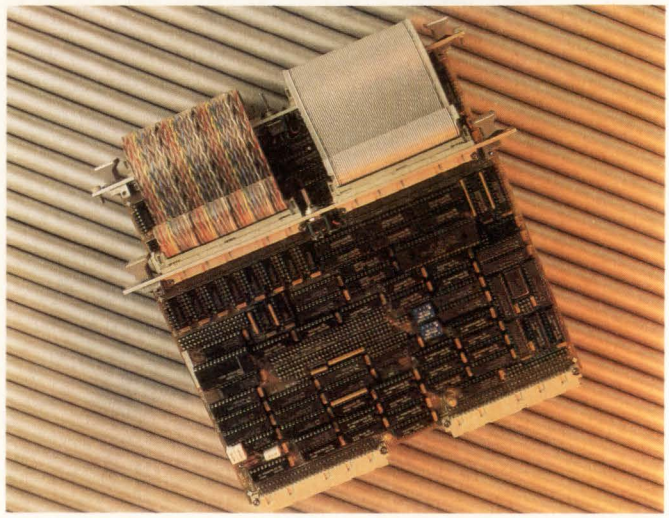

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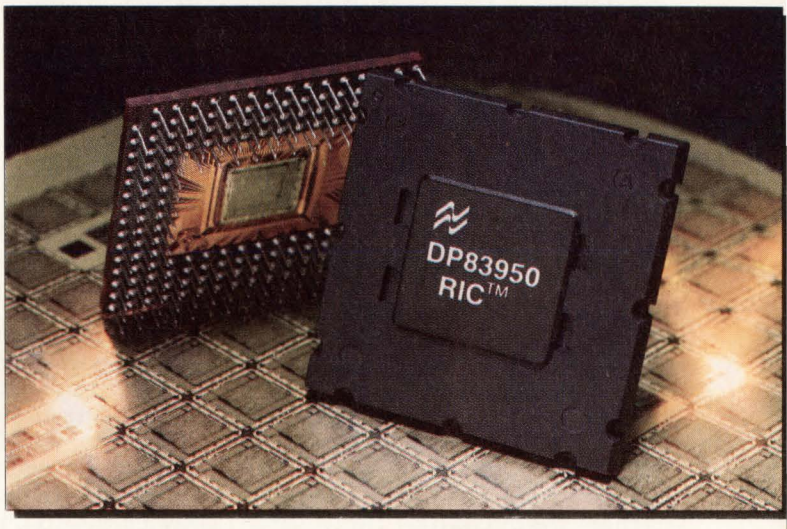
CIRCLE NO. 48

Many barriers slow quest for single-chip Ethernet adapter

Like knights seeking the grail, vendors of Ethernet controller ICs are pursuing a single-chip LAN adapter. But like the legendary cup, this goal may also prove elusive.

Ron Wilson
Senior Editor



National Semiconductor has developed a hardware-based strategy for dealing with network management. The company's new 10Base-T Repeater Interface Controller chip, shown, works in conjunction with the Sonic Ethernet controller to extract management data at the hub.

If the ultimate goal of network architects is to integrate all communication with a single standard, the ultimate goal of network hardware developers is to reduce that standard to a single chip. Vendors of Ethernet controller chips are now working to squeeze Ethernet onto one chip.

The benefits of such integration are obvious—reduced space, reduced power consumption and shortened design time. If a single chip could connect directly to a personal computer or workstation I/O bus on one side, and directly to the LAN medium on the other side, a lot of people should be much happier. But the picture isn't quite that simple.

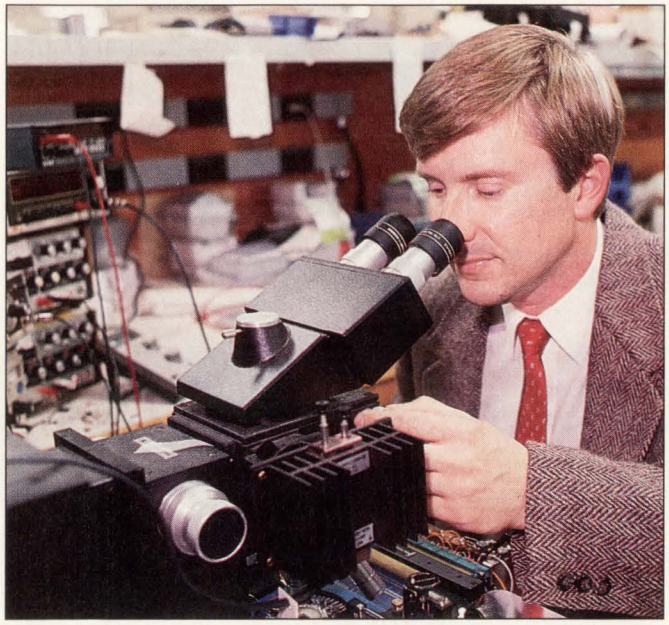
A number of technical barriers stand between current LAN product lines and the fully integrated adapter. These include everything from tough analog designs to process incompatibilities and marketing problems. But even when these difficulties are overcome—as most vendors feel they will be shortly—not everyone will rush to buy single-chip adapters. At least in the beginning, the new parts will be suited only to some particular segments of the LAN market.

Swarm of technical issues

"All the vendors I know of are working on a one-chip adapter—a chip that would go directly between the PC bus and the LAN wire," says Bruce Olenchuk, product line manager of the LAN group at Intel (Folsom, CA). "It's just a question of who gets there first." The most obvious impediment to getting there is a swarm of technical issues, which Olenchuk groups into three categories.

"First, you need an accepted Ethernet controller architecture. Next, you need the process and design capabilities to do the front-end hardware—the twisted-pair and attachment unit interface (AUI) connections. And third, you need the ability to design a high-performance bus interface." Each of these large issues covers quite a number of nontrivial smaller problems.

The issue of an accepted controller architecture is an example. The design job is not so hard that a reasonably funded design team couldn't come up with a good new controller. Even throwing in some of the latest features, like address filtering, buffer management and generation of network management data, the controller design is a reasonable under-



Bruce Olenchuk, product line manager of Intel's LAN group, puts the technical issues vendors face in their quest for a single-chip Ethernet adapter into three categories: "First, you need an accepted Ethernet controller architecture. Next, the process and design capabilities to do the front-end hardware. And third, the ability to design a high-performance bus interface."

taking. But the existing vendors have already staked out the market to the point there would be considerable resistance to a new architecture—no one wants to rewrite drivers. "We've had volume customers tell us they would give up a 10 percent reduction in parts cost rather than change their software," says Mike Villott, vice-president of marketing at Seeq Technology (San Jose, CA).

The front-end hardware presents a different kind of problem. First, to achieve a single-chip adapter, the controller, Manchester codec (encoder/decoder), and network attachment have to be integrated onto one die. But because of its complexity, the controller needs to be CMOS. So the first step in the integration is to extract the fast, jitter-sensitive codec and the current-hungry transceiver electronics from their native bipolar technologies.

Process and circuit challenges

"Moving these components to CMOS is the first step in integration," says Villott. "And in a way we had a built-in advantage there. Most vendors had great bipolar processes, and naturally used them for their Manchester encoders and transceivers. They said the codec in particular had to be bipolar at 10 Mbits/s. But for us, necessity was kind of the mother of invention—we didn't have a bipolar process, so we developed a CMOS codec several years ago. It's familiar ground for us now."

"There was some difficulty early on with CMOS codecs," agrees Olenchuk. "It took some work for us to get a part that would meet the IEEE's 18-ns jitter specification." Most vendors now are either offering or preparing a CMOS codec device.

An almost equal problem is the transceiver—the electronics that go between the TTL bit stream coming from the codec and the variously defined analog signals that actually go onto the network medium. And here the issue neatly divides into two pieces: twisted-pair and everything else.

"It would be very difficult to do a universal bus interface. It's better to try to do each individual bus well."

—Bob Jones, NCR

Most vendors are confident they can meet 10Base-T twisted-pair specifications with a CMOS transceiver. In fact, since the twisted pair is a local connection to a hub, not a shared, electrically isolated medium, the transceiver chip can connect directly to the wire through a few passive components.

Everything else—big yellow cable, little yellow cable, optical fiber, and so forth—connects to the transceiver through the AUI. And the AUI has some more demanding requirements, such as the ability to handle substantial currents through transformers. David Avny, field product specialist at Fujitsu (San Jose, CA), says, "We have twisted-pair capability in CMOS, and we are currently integrating that transceiver with our Ethernet controller to produce a single-chip 10Base-T product. But because of the current requirements for co-ax we will stay with a bipolar transceiver there—the co-ax solution will look like a three-chip set: an integrated CMOS controller/codec, a bipolar transceiver and a dc-dc converter package replacing the usual transformers."

NCR (Fort Collins, CO) has gone through similar problems. "You can do the AUI in CMOS, but it requires some very clever analog design," says Bob Jones, director of communication products in NCR's business unit. "You have common-mode voltage problems, differential drivers, and you have to be very careful with the chip layout to isolate the analog stuff—otherwise you create jitter problems in the codec section. In our latest part, we've solved these problems."

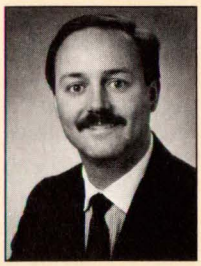
Coping with buses

After overcoming the problems of developing a jitter-compliant CMOS codec and a CMOS AUI connection, questing vendors must face the next obstacle: the enormous variety of I/O buses their customers might want to use. Ideally, the single-chip Ethernet adapter would work with the AT bus, the Micro Channel, the EISA bus just in case, and the SBus for the workstation market. And it would be nice if it could play right on the local bus with the 386, 386SX and 486 microprocessors. Of course it will need to do programmed I/O for the AT bus, but it must have bus master capability to adequately use the bandwidth of Micro Channel.

"Even if you could do a generic bus interface," says Olenchuk, "that just pushes the design burden onto the board designer. What people really want is a chip for their specific bus. Naturally, we will go after the highest-volume opportunities first, which means the AT bus."

"It would be very difficult to do a universal bus interface," agrees

Single-chip LAN: Ethernet, token ring or both?



Two common questions in networking today are "When will there be a single-chip Ethernet?" and "When will there be a single-chip token ring?" Both questions are driven by semiconductor integration. The integration of multiple-chip functions into single-chip devices is standard semiconductor practice. But every so often, market requirements stimulate true innovation in chip design.

Who needs a single-chip networking solution? The LAN OEMs that sell adapter cards are not likely to benefit from a single-chip Ethernet or token-ring solution, beyond minor cost savings. Their products are typically add-in cards, with sufficient area to easily accommodate the required functions without further integration. But manufacturers focusing on adding networking as a built-in feature of their products are in real need of motherboard real estate savings and cost savings. The LAN requirements in this product arena, including PCs, X-terminals and computer peripherals such as laser printers and plotters, are growing at an increasingly rapid rate.

Manufacturers integrating LAN capabilities into their products are scrambling to ride the rising tide of networked computing, already a requirement for sale to many Fortune 500 customers. Many manufacturers and users now achieve networking by purchasing add-in cards for PCs and other computer equipment. But single-chip network solutions are the key to achieving the layout area and cost savings necessary to get LAN adapters on the motherboard of PCs and similar products.

Token-ring market growing

Should an Ethernet or token-ring network be supported on a motherboard? Ethernet has the longest history, greatest installed base and currently leads in shipments—46 percent in 1990, according to market research firm Dataquest (San Jose, CA). Token ring, however, is the faster-growing market, with shipments now approaching those of Ethernet. Dataquest estimates that token ring is growing nearly 50 percent faster than Ethernet and will match Ethernet shipments by 1994. And, because it's IBM compatible, token ring is very important to Fortune 500 companies, which currently represent the strongest growth sector for PC networking.

Manufacturers focusing on networking as a built-in feature need motherboard real estate and cost savings.

To these manufacturers the choice of a network is important because the costs of engineering, manufacturing and inventory are significant. For now, much of the market is hesitating instead of integrating. Add-in cards are the current stop-gap solution for supplying Ethernet or token-ring connections.

Can both Ethernet and token ring be supported by a single chip? Could one chip provide a complete network interface? Before either question can be answered, some technical issues must still be resolved. For example, all of the existing, and different, Ethernet and token-ring cabling alternatives (physical layer) must be considered. For Ethernet, this means standard Ethernet (attachment unit interface), Cheapernet and 10Base-T; for token ring, it's shielded or telephone twisted-pair cable, or even fiber.

Single-network option

One possible solution might be to put all common Ethernet and token-ring support into a single chip on the motherboard, with standard interface to a physical layer off-board that can select the cable or protocol needed. This method lets Ethernet and token ring be added to a motherboard with selectable physical layers, without sacrificing flexibility or incurring costs associated with the physical layer. Engineering, expansion bus and inventory costs for two separate networking alternatives also would be eliminated. And this alternative would let selectable physical layer interfaces be built into cable connectors similar to some of the recently introduced 10Base-T transceivers.

A single chip with both Ethernet and token-ring support is an attractive alternative to a single-chip Ethernet or single-chip token ring. The question that remains is whether a dual-network chip or a single-network alternative will best meet the market's requirements.

Leon Adams, BS/Engineering Physics, open systems marketing manager, Texas Instruments Semiconductor Division

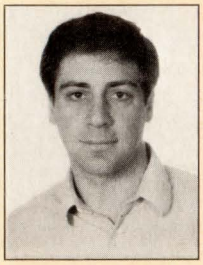
NCR's Jones. "It's a lot better to try to do each individual bus well—that means specific chip versions for each bus. And there's a lot more than just the handshake logic involved. For instance, if you try to be a bus master on the AT bus, you will have much different control logic and FIFO requirements than if you do the same thing on the Micro Channel."

And vendors' problems don't end with the relatively leisurely timing of I/O buses. "If you're going to put the adapter on the motherboard—which a lot of people are planning to do—there's no reason not to connect directly onto the CPU local bus," says Jones. Such a connection would give the best access to main memory, an issue of increasing importance for throughput.

But the range of CPU buses in just the PC world adds further to the proliferation of chip versions. The technical problems are not insuperable—most vendors already have most of the requisite interfaces in their cell libraries—but the resulting array of products promises to become a marketing headache.

A further complication comes from the software end of the network world. Ethernet users are growing increasingly shrill about the need for hardware-supported network management features. The ability to collect network statistics, to reconfigure nets on the fly and so forth is almost mandatory in the sprawling ad-hoc tangle of networks that has sprung up in many corporations. And the bases of these features lie not in software but in hardware at the

Integrating Ethernet vs. Arcnet adapters



Even with the most highly integrated devices available, Arcnet and Ethernet LAN adapters require careful design. The differences between the two LAN protocols force designers to make substantial choices.

The smaller packet size of Arcnet and the inclusion of flow control and acknowledge services in its protocol mean that all a controller needs is 16 kbits of buffer RAM (far less than Ethernet). Arcnet controllers can incorporate the buffer on-chip, increasing speed and reducing the number of pins. Yet 16 kbits allow double buffering of transmit and receive packets. Flow control guarantees that the node won't be sent packets unless it has free memory to store them, and the acknowledge enables the transmit process to free up its memory immediately after transmit completion.

Network media

For twisted-pair support, Arcnet adapters need only one pair, while Ethernet needs two pairs (one to detect collisions). Arcnet adapters don't need different transceivers for co-ax and twisted-pair cables. Ethernet adapters supporting multiple options need one type of transceiver for co-ax buses and another for twisted-pair star topologies. No dc-dc converters are needed in Arcnet adapters.

Ethernet started as a bus backbone, in its thick and thin co-ax embodiments, and was only recently given a star topology option by the 10Base-T specification. Arcnet originally used a star (or distributed star) topology and was expanded to include bus extensions. All combinations of network architecture and physical media share the same signaling scheme in Arcnet. With Ethernet, there's no bus topology with twisted pair and no star topology with co-ax.

Arcnet allows simple transformer coupling for twisted-pair balance and common mode rejection. Arcnet adapters don't require any special signal conditioning such as 10Base-T's predistortion. Signal levels are higher than 10Base-T's, making it less sensitive to crosstalk from other signals on adjacent pairs (such as phone ringers).

Arcnet allows changing from star to bus topologies by removing a termination resistor. Ethernet is not portable from its original bus topology on co-ax to twisted pair. It needs a new "medium-dependent interface," namely a twisted-pair interface transceiver. Dc-dc converters are typically needed to provide the required isolation.

Additional interfaces

Ethernet adapters and single-chip controllers also need to support the attachment unit interface (AUI). A three-pair differential interface is mandatory for that purpose in addition to the chosen medium interface. Originally, the co-ax Ethernet interface required a bus with no drops and restricted places in the cable where connections could be made. The AUI lets the transceiver be removed from the node via a 50-m three-pair interface.

Arcnet controllers can incorporate the buffer on-chip, increasing speed and reducing the number of pins.

Supporting this extra interface requires supplying power to the transceiver and adds three transformer-coupled pairs, whose design considerations are similar to the two 10Base-T pairs. The AUI also complicates VLSI partitioning and pin multiplexing by imposing an interface with tight timing and level requirements.

Ethernet adapters have unique addresses programmed at manufacturing time while Arcnet adapters are assigned addresses at installation time. Having a unique address is an advantage for Ethernet adapters because it removes the burden of address management. Ethernet adapters have to include the nonvolatile storage for the factory-programmed 48-bit address. Arcnet adapters generally have an 8-bit DIP switch for the locally administered Arcnet address.

Network diagnostics

Ethernet controllers and boards typically need more-involved fault-diagnosis functions such as link integrity, polarity, jabber, and late collision (Arcnet uses one LED for all purposes). Link integrity and polarity were added to twisted-pair Ethernet to help the installation process. Confusion can occur between cables as well as with the polarity of each pair.

The link-integrity function provides activity in a network like Ethernet where a node is usually inactive unless a software driver is installed and running. It checks whether the link between the node and the concentrator is working properly. With Arcnet, tokens are constantly circulating through all nodes, so the wiring of the entire network is continuously checked. Token passing also checks the node receiver, transmitter and protocol operations. Arcnet only requires one transmit LED on each node and one per port at the hub to visually monitor correct wiring and node operation.

To check the transmit/receive paths in Ethernet, an external loopback test is required. Loopback testing, however, is not possible in twisted-pair Ethernet because the function was eliminated to make room for collision detection.

Late collisions usually indicate a network with excessive delays due to excessive cable lengths, levels of concentrators or other reasons. Excessive delay in Arcnet usually manifests itself immediately during network configuration. And in Arcnet, long delays are less-severe mainly because Arcnet's hubs are self-timed and have little delay or delay variance.

An Ethernet high-integration controller or adapter designer has to make provisions for a certain minimum performance, otherwise the node functionality collapses. For Arcnet the node gracefully decreases its performance with the system, never losing functionality.

The main parameters in an Ethernet system that might affect the node functionality are the bus bandwidth, interrupt latency and the DMA latency (for DMA architectures). If those parameters are degraded, the node will eventually lose packets and waste network bandwidth in retransmission. In Arcnet, the built-in flow control will slow down the packet rate to what each node can handle.

Ariel Hendel, MSEE, strategic planning manager, Standard Microsystems Components Division

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LAN controller chip level.

"The IEEE has defined 37 network statistics that should be captured," says Jones. "And our customers tell us they want to be able to do this at their local terminal, not on some specialized piece of hardware. So we've designed our controller to capture the data and report it through status registers." Jones says he expects to see this capability showing up in both nodes and concentrators.

National Semiconductor (Santa Clara, CA) sees things a bit differently. The company is assembling a network management strategy centered on the hub of a 10Base-T network. The key to the National approach is a pair of chips, the elaborate Sonic controller chip and a new companion device, a 12-channel 10Base-T Repeater Interface Controller (RIC) chip.

"We believe the major issue in 10Base-T is that it provides a central point for managing the network," says Richard Brand, strategic marketing manager in National's LAN product group. "So we've put together a chip architecture where the RIC and Sonic work together to capture the management objects the IEEE has defined. Then the hub controller can pass those objects to higher-level management software, such as Simple Network Management Protocol or Open Systems Interconnection."

The emergence of such hardware provisions for network management has important implications for vendors rushing toward the single-chip adapter. Because data collection has to go on in the controller, it's important for vendors to get the necessary hardware features into the controllers before they integrate. Otherwise the single-chip part could end up unable to support the customer's network management needs. Whether this is a concern for the node end of 10Base-T networks—where the single-chip parts are most likely to be used—or just an issue for hub designers remains to be settled.

The cost of speed

Finally, the vendor must face the issue of performance. Throughput on the network node is not really a matter of controller speed. "We are currently sitting at about 1,100 kbytes/s, compared to a theoretical maximum of 1,130," says Fujitsu's Avny. Rather, actual performance is an issue of how protocol processing gets handled.

"It's a religious issue," says Wayne Ward, networking product line marketing manager at Interphase (Dallas, TX). "Sure, you can use your CPU to run the LAN protocol software. But people buy that 486 for their application, not for TCP/IP (Transmission Control Protocol/Internet Protocol). That feeling seems to get stronger as the CPU gets more powerful. In the Unix world, for instance, we see a lot of people buying adapters with on-board protocol processing. Even in the Sun-IV 70s and 90s, you get substantially better performance if you don't use a dumb Ethernet adapter."

"We've had volume customers tell us they would give up a 10 percent reduction in parts cost rather than change their software."

—Mike Villott, Seeq Technology

The problem of protocol processing has two important implications for the single-chip adapter quest. First, it will limit the market for single-chip solutions to those nodes requiring just connectivity, not high throughput. "I expect that people who have single-chip adapters built onto their motherboards just won't use them if they need high performance," says Ward. The high end of the market will still need adapters with on-board protocol processing, and those adapter vendors will look for the best feature set in their chips, not the smallest footprint.

Second, the protocol problem may drive yet another round of integration. "TCP/IP on the chip would require more intelligence than today's products have, but you may see it in the next couple of years," says Intel's Olenchuk. "We have the capability to put a CPU on the controller chip now—it will become more viable as geometries get smaller."

The vanishing adapter

As geometries shrink, another unfortunate fate begins to threaten the single-chip solution: the possibility of a zero-chip adapter. Once the whole Ethernet chain is in CMOS, there's no reason why the adapter can't be integrated into a motherboard chip set, or even onto a single-chip PC. Certainly the level of integration would be far beyond current mass-produced products, but it's not beyond reasonable speculation. "We have considered putting LAN capability into the chip set," says Olenchuk. "The question is when to do it, and which LAN to support—Ethernet, token ring, Arcnet, or some combination?"

So in fact the single-chip adapter may not be such a holy grail after all. The problems in getting there are mostly solved, at least on paper and in the lab. But the chip will not be everyone's cup of tea. Demanding high-end users will want more powerful adapters with local processing. Mass-market customers may just use the one-chip products to bid down the cost of existing multichip solutions, as has happened in the PC chip set market. And the chip set vendors are already taking aim on LAN capability as a next opportunity to add value to their own products.

In the end, the single-chip solution will serve two purposes. It will be an excellent fit for space-constrained, moderate-performance applications such as Sun's SBus environment. And it will be a technical stepping stone to two even more integrated products, the LAN-in-a-chip-set and the controller with on-chip protocol processing. The product will not be an ultimate goal, perhaps, but an important milestone nonetheless. ■

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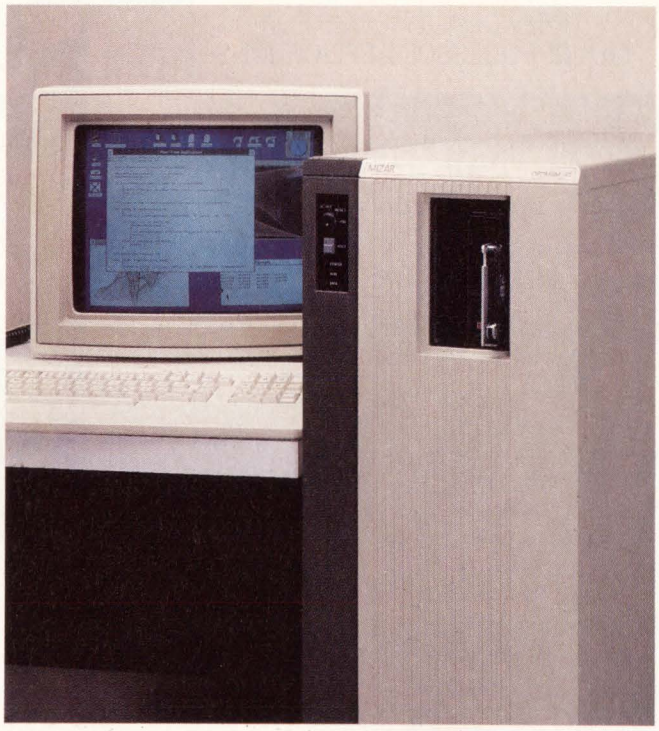

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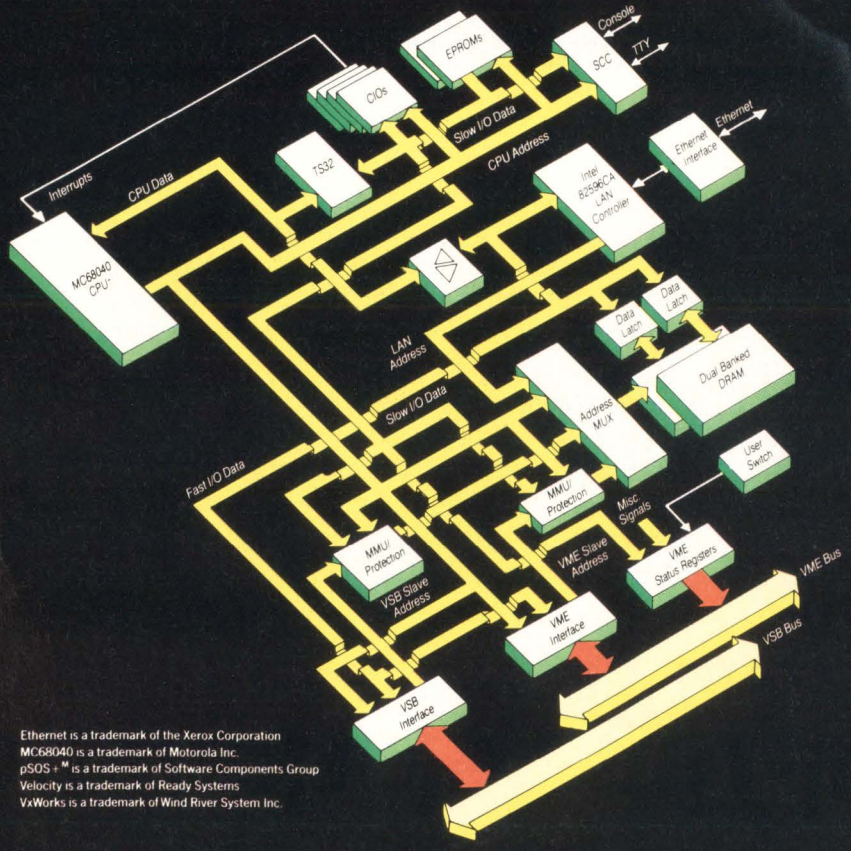

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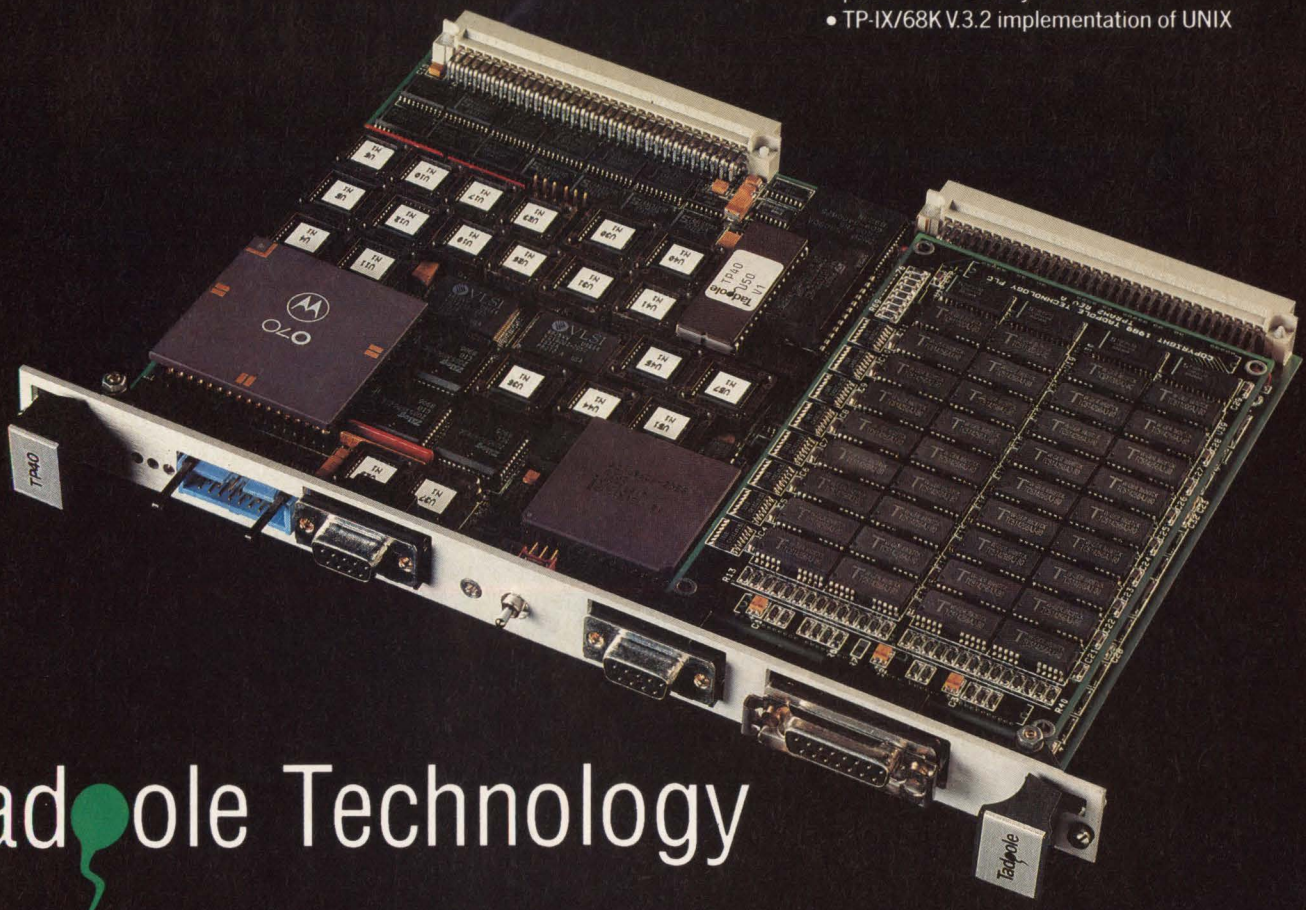

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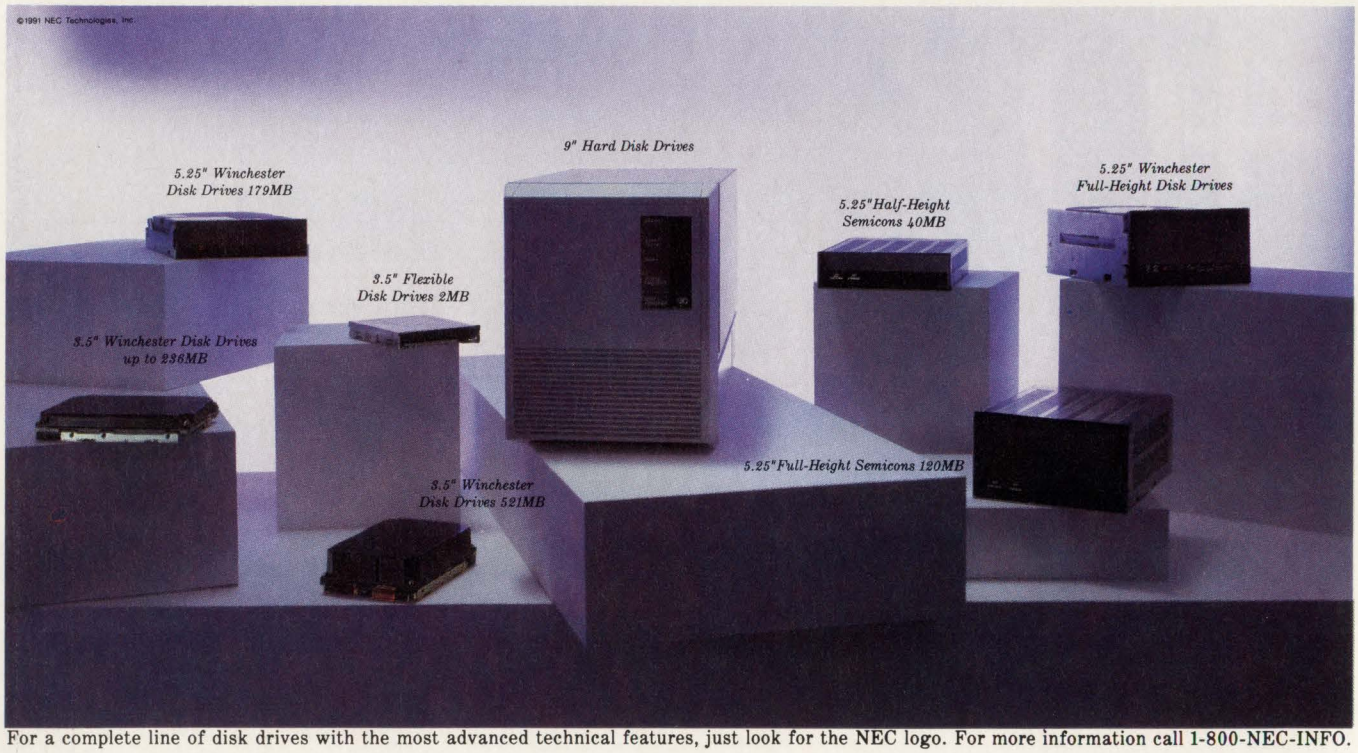

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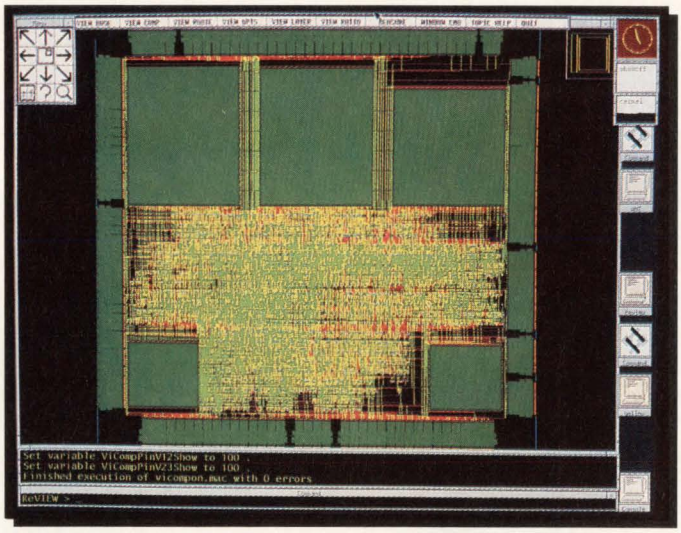
CIRCLE NO. 52

Are mixed cells and arrays the solution ASIC vendors claim?

Does embedding fully diffused blocks on gate arrays really offer designers the best of both worlds?

Barbara Tuck
Senior Editor



As customers clamor for shorter turnaround times for complex ASIC designs, silicon vendors are pushing the practice of putting down a custom or compiled block of memory or other application-specific function onto a base array. Not a new concept, mixed-architecture design has been implemented by large OEMs for years. But as chips get larger and functionality demands increase, vendors are enriching their cell-based libraries and developing software that will enable them to extend this technology to all customers.

Whether benefits to customers will outweigh the disadvantages of mixed-architecture design remains to be seen. In the meantime, it's certain that design activity in this area will affect the standard-cell market. Mixed-architecture designers will be rewarded with the density, speed and flexibility of a standard-cell-based approach and at the same time will benefit from the quick turnaround times and fixed die sizes associated with gate arrays.

One example of this approach involves prediffusing cell-based blocks onto a gate array masterslice even before customers submit a netlist with design details. And where base arrays can be used more than once, with modifications to the logic and perhaps to the memory configuration through metallization, the cost of fabricating customized wafers could be amortized across a number of designs.

Complex gate array designs challenge place and route tools. Mentor Graphics' Parade has been designed to reduce the layout time of highly complex ASICs by up to 90 percent. The tool can move arbitrary blocks during routing, when additional routing resources are needed between blocks.

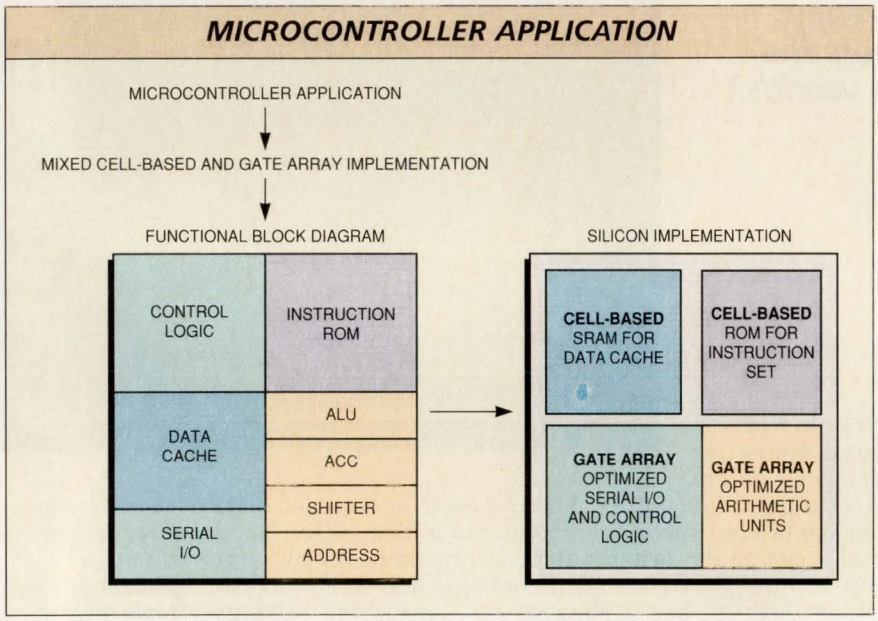
What's the bottom line?

Lack of enthusiasm for mixed-architecture ASIC design on the part of leading standard-cell vendors makes one wonder to what degree this trend is customer-driven and to what degree it's a business strategy on the part of gate array vendors (see "Consider all factors in choosing ASIC approach," p 82 and "Alternative to embedded arrays speeds turnaround for standard-cell designs," p 84). Gate array vendors benefit because they're able to differentiate product through custom or compiled application-specific function blocks rather than by process technology alone.

And there are other questions. Will the optimized elements customers require accommodate themselves to embedded arrays? And will NRE (nonrecurring engineering expense) charges and turnaround times for mixed-architecture designs be close to those for gate arrays, or will they be much closer to standard-cell costs and cycle times? Finally, if the cost of custom-

ized masterslices has to be amortized across multiple designs, how many customers will be willing to commit to masterslices early in the design cycle? How many will be willing to support inventories of base wafers?

A significant underlying factor in this latest ASIC trend is an industry-wide emphasis on the end application. The emphasis is clear whether vendors mix standard-cell and gate array architectures or offer pure standard-cell approaches with application-specific cores. Even standard product vendors are, in some cases, offering customers predefined application-specific functions that can be integrated on-chip along with the designer's own logic. It would seem that both ASICs and standard products are moving toward application-specific standard products (ASSPs).



The microcontroller application lends itself to a mixed cell-based and array-based design architecture. Designers would define a masterslice with diffused cell-based ROM and SRAM blocks and then would use the gate array portion for their own logic structures. Designers could then synthesize those logic structures, optimizing for area and speed with the ASIC vendor's Synopsys library.

Structured to embedded array

LSI Logic (Milpitas, CA) is generally credited as the pioneer of the practice of mixing cell-based and array-based techniques. The LSI structured array featured a gate array base with embedded memory block of fixed size and fixed location. As customers demanded more flexibility, LSI introduced the customer-defined LEA100K embedded array series. The LSI CMOS arrays, with 0.7-μm channel length and 1-μm gate length, have up to 150,000 equivalent gate capacity and up to 422 signal I/O.

Customers can place cell-based memory and other function blocks, microprocessor cores and any user-defined semicustom cores in any location on user-defined gate array masterslices. LSI offers the capability of converting soft-coded LSI and MSI building blocks that it calls megafunctions into hard-coded large building blocks that the company refers to as megacells. ASIC designers can generate single and multiport RAMs and ROMs with LSI's Memcomp memory compiler.

Simon Napper, LSI's director of design tools marketing, claims that the company's silicon-specific Modular Design Environment (MDE) software reduces cycle time for mixed-architecture designs.

With MDE software, designers can check the functionality of the design by running extensive simulation with user-defined test patterns. Floorplanning tools then optimize the placement of functional blocks and generate estimated block delays. LSI uses this information to start fabricating the base wafers while the placement and routing of the rest of the design continues. Finally, at metal fabrication, the vendor-generated masks are used to metallize the prefabricated base wafers for the customer's design.

Reusable masterslices

A significant side benefit of mixing array-based and cell-based architectures is that the same customized masterslice may be used multiple times, even in various parts of a single system. For each additional time the masterslice is used, the engineering costs incurred are more like an array-based design.

Prem Nath, LSI marketing director for the Sparc Systems Division, says the company will be basing products to be announced later this year on internally designed LEA100K embedded array masterslices. Nath reports that the LSI Microprocessor Group designed the 64811 integer unit of the Sparc microprocessor for the Sparcstation II on an embedded array in less than a year. The 64811 has three fully diffused register files embedded on the base array.

LSI also used an embedded array for the 64815 memory management, cache control and cache tags unit for the Sparc microprocessor. The 64815 has a RAM block embedded on the gate array masterslice. In addition to basing ASSPs on these masterslices, LSI intends to offer ASIC designers a 64811 masterslice. By varying random logic on the gate array portion, designers will be able to personalize the masterslice.

Custom RAM cell generator

Motorola's ASIC Division (Chandler, AZ) is extending that company's support of mixed cell-based and array-based architecture, which Motorola refers to as the customer-defined array concept. A custom RAM cell generator, jointly developed with Mentor Graphics, is scheduled to be released later this year. It will be part of the second-phase introduction of the up-to-318,000-gate submicron CMOS H4C gate arrays, adding a library of embedded blocks of fully diffused RAM.

"The H4C series moves us a step closer to supporting the large architectural blocks necessary to reduce time-to-market and harness the functional density of submicron processes," says L.J. Reed, vice-president and general manager of Motorola's ASIC division. H4C silicon is being made available in concert with design tools that will allow utilization of the density levels, ac-

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cording to Motorola.

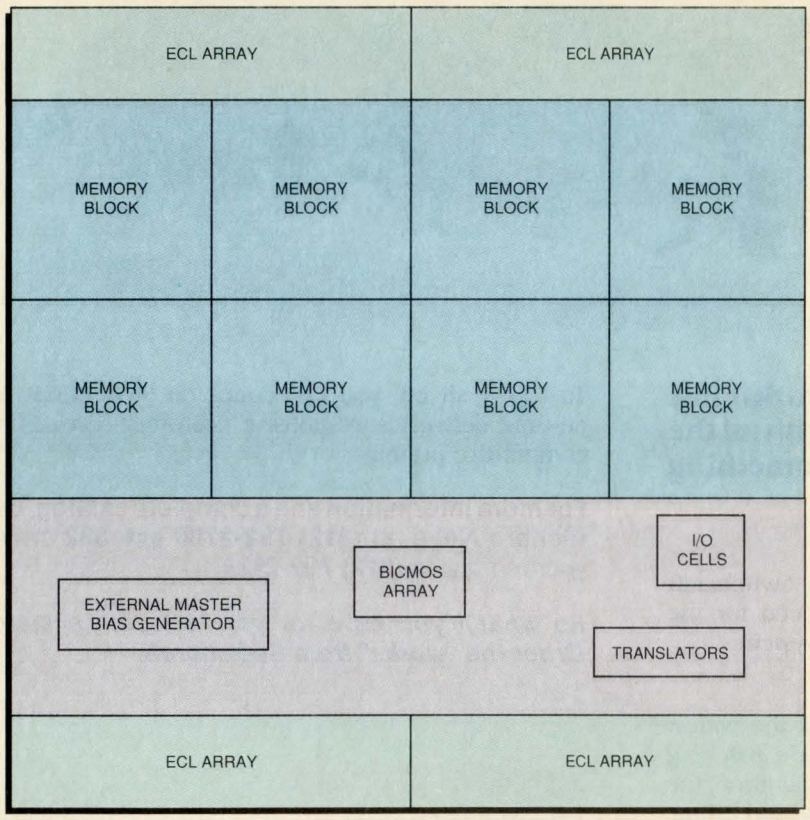
Motorola first applied its customer-defined array concept to its MCAIV series of ECL/BiCMOS arrays. The company reports that the 50,000-gate, 90-ps MCAIV arrays have been eclipsed by the next generation of bipolar-based arrays to be introduced next month. In the meantime, the semiconductor giant expects a much larger customer base for the CMOS H4C arrays.

Jerry Prioste, manager of the Bipolar Applications and Design Center, says that Motorola is still doing a lot of customization, involving proprietary tools and manual intervention, with bipolar technology partners. The initial round of bipolar customer-defined arrays didn't involve full engineering workstation support, but Motorola expects that future generations will. Though Motorola is implementing optimized, dense custom blocks and embedded cores with technology partners, the company may never release that kind of functionality to the public because of the amount of software involved.

In addition to the custom RAM cell generator for the H4C CMOS customer-defined arrays, Motorola is using synthesis software from Synopsys (Mountain View, CA) and Verilog, Gate Ensemble place and route tools, and Dracula for verification from Cadence Design Systems (San Jose, CA). For schematic capture, Motorola is supporting Mentor on Apollo and Valid Logic Systems on Sun workstations.

With regard to the price of the additional set of masks required for a mixed-architecture design, Motorola says that production pricing will be something between that of a standard cell and that of a gate array. The second time customers use a base wafer with embedded memory, for instance, they would have the customized diffusion set for memory, so the second-time-around cost would be more like that for a gate array.

NATIONAL'S ABIC IV ARRAY ARCHITECTURE



The up-to-62,000-gate ABIC IV BiCMOS arrays from National Semiconductor contain both ECL (typical delays of 100 to 160 ps) and BiCMOS (typical delays of 270 ps) gates and have embedded blocks of SRAM. The fully diffused memory blocks are not customer-definable; they have a fixed size and a fixed location.

Texas Instruments (Dallas, TX) refers to its mixed-architecture ASICs as user-specific arrays and offers them with compilable memory functions, macro generators and flexible ECL/CMOS/TTL I/O cells with standard footprints. The capability for embedded functionality will be extended, TI claims, to datapath elements.

The capability to embed fully diffused functional blocks on a base wafer is limited by the base process technology. At present, TI customers can elect to embed CMOS cell-based blocks on a CMOS gate array masterslice or to embed CMOS and/or BiCMOS blocks on a BiCMOS masterslice

Prediffusing blocks on array

TI gains cycle time by beginning to process material through the wafer fab before the customer hands off a netlist, says Tom Sprunger, high-performance ASIC manager. This scenario has the customer sitting down with TI to specify the blocks to be prediffused and to figure out the die size required for those blocks and the designer's own logic. "If the customer uses the base wafer just one time, the cost will be more like a standard-cell design," says Sprunger. But each additional time the base wafer is used, the cost would be more like gate array costs. The user-defined arrays are attractive to customers who can foresee the need to do multiple designs and can envision the variations in those designs up front.

In those instances that involve reusable arrays, large blocks have to be preplaced. That task of floorplanning blocks with regard to the gate array section of a mixed-architecture design, sometimes done prior to having a netlist, involves a lot of extra effort. "You have to figure out what might be good locations in view of future designs," says Sprunger. TI so far has been preplacing large blocks manually but is developing proprietary software that will help automate that task and make the design flow more efficient.

Although Sprunger sees mixed-architecture design initially fitting in at the high end, he thinks that in the next two to five years, as software becomes more automated and costs come down, it will become a very popular architecture with vendors and customers alike.

That optimistic outlook for mixed-architecture ASICs is not shared by

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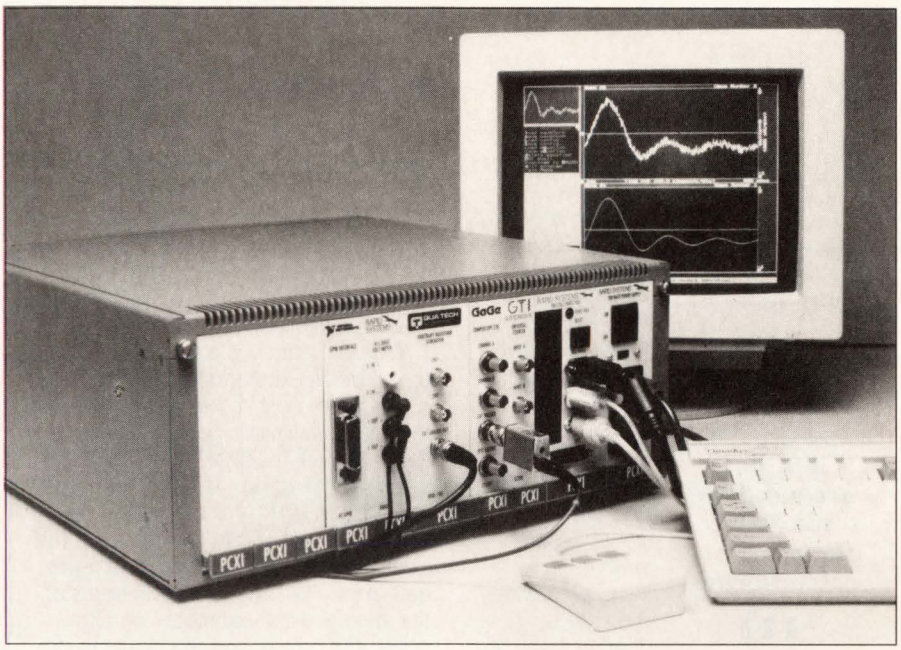

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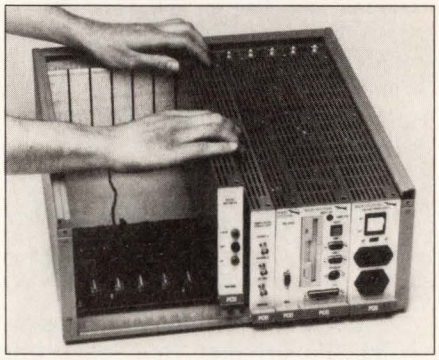

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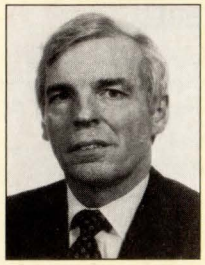
CIRCLE NO. 58

Consider all factors in choosing ASIC approach



At one time ASICs were easy to categorize: gate arrays for applications requiring fast turnaround time and standard cell for applications that had to be cost efficient. But the world of ASICs is changing fast. Today's high-performance, high-density, silicon-efficient gate arrays are available with turnaround times of eight days or less, standard cells six weeks and embedded arrays somewhere in between. The actual turnaround time of embedded arrays will depend on how early in the design cycle the engineer can freeze system requirements for gates, memory and I/O.

Which ASIC style is best suited for an application depends on many factors including design complexity, required test methodology and production requirements. Quality, NRE (nonrecurring engineering expense) and business risk factors also must be considered.

At Toshiba, all new sets of base wafers undergo a rigorous internal qualification exercise before they go into production. This applies to all new standard-cell designs as well as gate array masterslices. Production ramp-up time for an embedded array is the same as for a standard-cell design unless the designer is going to take the risk of manufacturing base wafers before the design is system-proven. The most important question for the ASIC designer to answer before committing to any particular design style is whether it will result in cost-effective, reliable silicon.

Where memory is a significant part of the design, a standard-cell solution is often the most cost-effective.

In some cases, an embedded array approach is correct provided the necessary steps are taken to ensure that devices of the required quality and reliability can be manufactured in production. Because of their competitive design costs and short turnaround times compared with other solutions, gate arrays are now the main route for producing high-performance, production ASICs and many application-specific standard products. With three layers of metal interconnect, they can compete with full custom designs for most applications.

Where memory is a significant part of the design, a standard-cell solution is often the most cost-effective, due to the area gain over a gate array implementation. A Toshiba TC25SC 0.8-μm standard-cell design with 10,000 gates and 16-kbit RAM, for example, needs only 20 percent of the silicon area of the same function implemented on a 1-μm gate array. The other big advantages of the standard-cell approach are high-power I/O drivers and the ability to design analog cells into the I/O ports.

Toshiba's approach to the mix of solutions needed for ASICs is to offer volume-capability 0.8-μm gate arrays and standard cells along with design house expertise if required.

Frank R. Ramsay, strategic marketing manager, Semicustom Unit, Semiconductor Group, Toshiba America Electronics Components

Robert Nalesnik, silicon product line manager at VLSI Technology (San Jose, CA). VLSI, a leading standard-cell vendor and also very active in gate arrays, is conspicuous by its absence among mixed-architecture advocates. Nalesnik reports that the company, which approaches customer requirements more on a custom basis, sees mixed-architecture designs affecting only 5 to 10 percent of the total number of cell-based designs.

Though advantages are attractive, says Nalesnik, they don't outweigh the disadvantages. He says mixed-architecture design seems to be able to improve only prototype lead time, not production lead time. The optimized elements their customers request tend to be heavily datapath-oriented and do better in cell-based designs since such elements are hard to lock into a design early in the cycle. Changes to datapath-intensive designs tend to involve overall structure rather than just a few gates. Perhaps the richest element of VLSI's cell-based library is the Acorn microprocessor core.

VLSI's product line marketing manager, Steve Kompolt, says the issue for designers shouldn't be how quickly a mixed-architecture ASIC can be designed, but how significant the benefits of the design are. Kompolt suggests potential customers ask themselves (1) can we reuse the base, and (2) if so, are we willing to commit to inventories of base wafers? If customers can reuse a masterslice and can also commit to inventories, Kompolt agrees they'll be rewarded with a quick turnaround time on subsequent designs.

Users to define mix

Flexibility is key to the approach Applied MicroCircuits Corp (San Diego, CA) is taking in high-performance mixed-architecture design. Applied MicroCircuits Corp (AMCC) begins with a bipolar BiCMOS or Bi^2CMOS array on which the customer can specify the number and location of BiCMOS and ECL cells as well as die size. An AMCC alternative would begin with an existing array, optimized for a specific standard package, that had a predefined mix of BiCMOS and ECL cells. Several die sizes and package options would be available. In either case, the AMCC customer would then work with floorplanning tools, within the constraints presented by the I/O and the array's power busing structure, to embed fully diffused digital and/or analog function blocks in place of existing cells. Fast-access RAM could also be compiled into the base should designers require it. The base silicon could then be released to the fab while the customer designed the interconnect. Representative functional blocks would include nanosecond ECL memory, GHz phase lock loops, or high-speed and high-density BiCMOS static RAM.

AMCC's director of strategic marketing, Marc Friedmann, says the company will offer designers such mixed-architecture design capabilities about a year from now. AMCC will offer floorplanning and recon-

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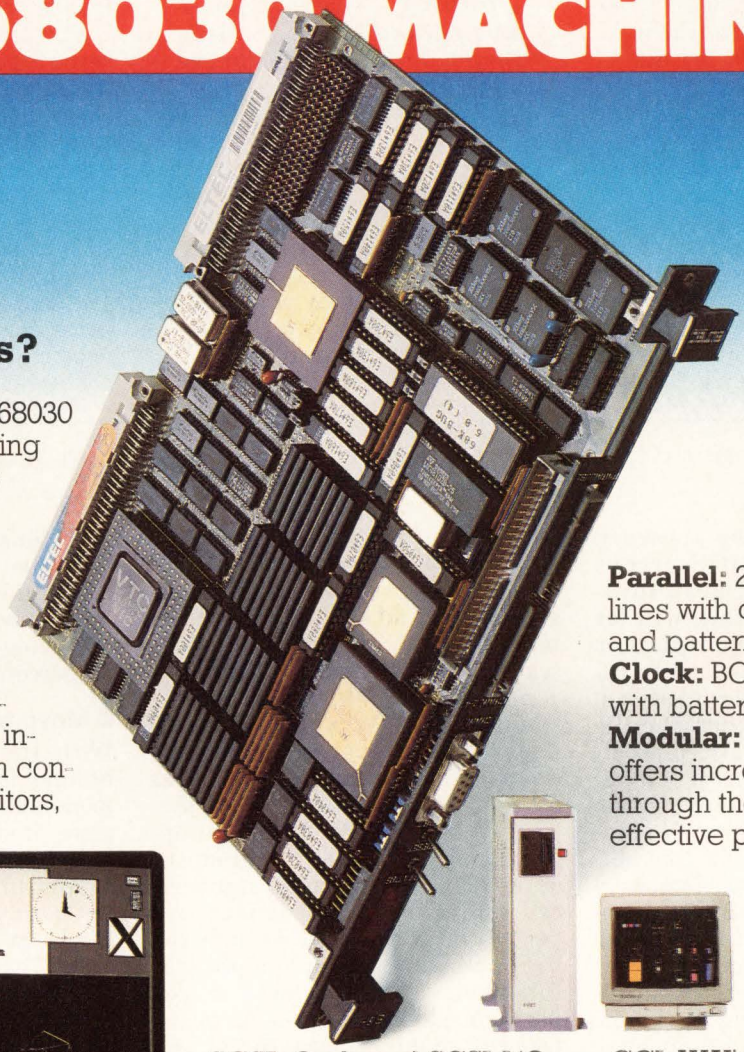

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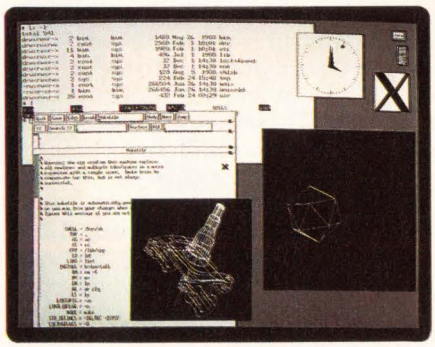

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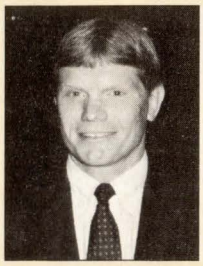
CIRCLE NO. 54

Alternative to embedded arrays speeds turnaround for standard-cell designs



Embedded arrays and their associated interconnect overhead are acceptable to some systems houses. Some customers, however, primarily in high- volume production, aren't especially keen on paying that extra area penalty. As part of their quick turnaround strategies, these systems houses are intent on driving down silicon area to optimize piece price.

The FastTurn standard-cell design methodology from AT&T Microelectronics is an alternate approach for achieving high density and quick turnaround. With it, design objectives are achieved without sacrificing any of the regular standard-cell methodology's major design benefits.

Unlike embedded arrays, FastTurn focuses on a packed final layout using AT&T's standard-cell library, including macros, to minimize design time. Both 1.25-mm and 0.9-mm two-level-metal CMOS technologies are included.

The key acceleration point is the customer design handoff-to-mask order interval of two weeks. That's followed by a four- to six-week mask-to-prototype period. Tight turnaround is enforced by strictly adhering to the use of routine library elements, avoiding potential delays associated with customized cells.

FastTurn focuses on a packed final layout using AT&T's standard-cell library.

Basic cell enhancements combine with design guidelines to cut down on time-consuming design tasks. Guidelines cover the netlist, vectors, power and ground pins, as well as timing- and hazard-analysis simulation.

Among netlist design guidelines are a maximum of 10 global and 50 local clocks, plus specified gate and signal names. Other requirements include a 30,000 total gate limit, a maximum of 10 signals driven by buffer cells (including all global clocks), and the elimination of asynchronous loops. Specific vector guidelines also contribute to tightening the design period. They stipulate a 60,000 vector ceiling with 20,000 vectors used for high-speed verification and the remainder for fault coverage.

More time is saved on designs by adhering to power and ground pin guidelines. Designers are guided to calculate the minimum number of power and ground pins to avoid lengthy ground bounce simulation and analysis.

Finally, as part of the simulation guidelines, each design must pass an audit for timing hazards to ensure manufacturability. A vector set doesn't pass hazard analysis until simulation values and expected values match. Another stipulation is that nodes are not oscillating.

John Harrington, department head, Custom VLSI Design Development, AT&T Bell Laboratories

figurable rules-checking software to support its Bi^2CMOS arrays and analog and/or digital function blocks. The software will let customers change a floorplan or embed a function block onto an existing array. Friedmann sees a heavy emphasis on synthesis for the gate array portion of mixed-architecture designs. He expects synthesis and floorplanning tools will be interactive though not entirely automated at the start. AMCC has announced support of the Synopsys Design Compiler for its BiCMOS arrays and expects to do the same for the newer ECL Compiler next year. The Synopsys ECL Compiler has all the elements, according to Friedmann, to make it viable in this market as its installed base grows.

Floorplanning tools

Vitesse Semiconductor (Camarillo, CA) also adds the support of the Synopsys Design Compiler to its up-to-100,000-gate FX series of GaAs gate arrays. And to facilitate floorplanning and the preplacement of embedded blocks on those GaAs arrays, Vitesse has developed an interactive graphical preplacement program. Ira Deyhimy, vice-president of product development, reports that customers will have access to the floorplanning tool that, at this writing, is in testing with selected customers.

By next fall, Oki Semiconductor (Sunnyvale, CA) will also have a floorplanning tool for customers doing mixed-architecture designs on its 0.8-µm CMOS gate arrays. Cliff Vaughan, strategic marketing manager for logic LSI products, says Oki—a full-custom, standard-cell and gate array vendor—expects a large share of its high-volume parts to have embedded functions. Having offered single-port embedded memories for years, Oki will make a major thrust over the next year or so in the mixed-architecture design direction.

The first multiport memories and memory-related logic blocks will be available in April, with first silicon of more elaborate memories and microcontroller peripheral blocks expected in May or June. By fall, the Oki library plus its floorplanning tool will be ready for customers.

Vaughan says Oki engineers underestimated the area savings that could be achieved with embedded function blocks, anticipating a savings of about 10 percent but actually achieving a savings of as much as 50 percent.

Move toward ASSPs

With the push to turn products around fast and the need to pack more and more functionality on a piece of silicon, Vaughan says cell-based embedded blocks will play a significant role in moving the industry more and more toward ASSPs. Intel's 16-bit 80C186EB ASSP processor, based on a fully static core and a 1-µm cell-based library of peripheral and memory circuits, lends credibility to Vaughan's statement.

Though mixed-architecture designs are expected to have an impact on pure cell-based designs, it's not expected that the embedded array approach will affect the mixed analog and digital standard-cell market—at least until vendors and designers alike achieve more design control. A second prerequisite for analog and digital mixed-architecture design is an advanced BiCMOS

At Interferometrics Laboratories Todd Brackett, Control System Group Leader on NRL's Big Optical Array Project, adjusts the optics on a laser interferometer.

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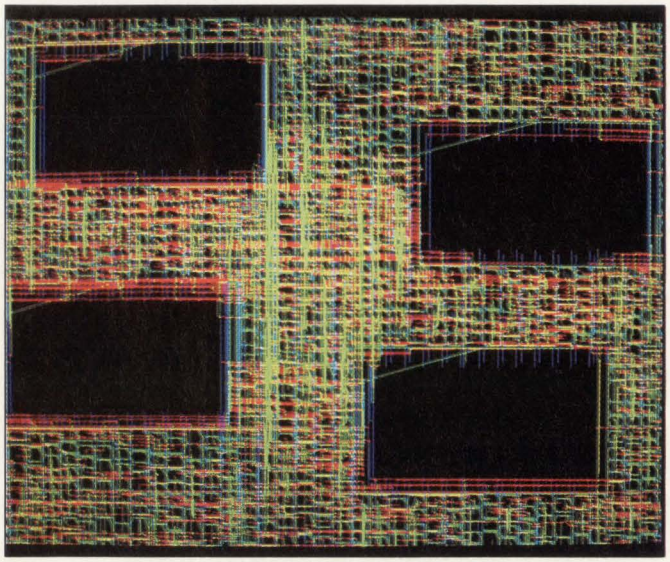

Designs that mix a sea of gates and embedded blocks on a single piece of silicon present no special challenge to the Cadence Gate Ensemble place and route tool. Though the CMOS-oriented router accommodates BiCMOS mixed-architecture designs, the ECL version of Gate Ensemble is ready as high-performance bipolar-based BiCMOS gate arrays become available.

process like the 0.8-µm ABIC IV from National Semiconductor (Santa Clara, CA).

Analog blocks, too?

Two other ASIC vendors have some but not all of the ingredients for BiCMOS analog and digital mixed-architecture ASICs. SGS-Thomson Microelectronics has a BICMOS cell-based analog and digital library, and NCR Microelectronics, which claims a number one position in mixed-signal cell-based ASICs, has 1.5-µm and submicron CMOS analog and digital cell-based libraries. Even if a vendor had in its hands the appropriate process and libraries for analog and digital mixed-architecture ASIC design, routers smart enough to analyze coupling problems between analog and digital blocks are not available yet, says analog guru Jim Solomon, president of the Cadence Analog Division.

Though place and route tools can handle primarily digital mixed-architecture designs, Dan Skilken, director of ASIC marketing for Mentor Graphics' IC group (San Jose, CA), reports that place and route time for a large gate array can be even longer than for a standard-cell design. Mentor's new Parade place and route tool, claimed to be 10 times faster than the competition's, supports variable-width routing tracks that let it move arbitrary blocks apart during routing to add resources on the fly like a standard-cell router.

More and more submicron-ASIC customers are choosing to cut down NRE charges and increase design control, according to Skilken, by placing and routing their own designs. In such instances, a silicon vendor tunes the place and route tool to the vendor's base-array technology and releases the tool to the customer, along with a back-annotated netlist for the design.

All this activity in mixed-architecture ASICs goes to prove that design directions are difficult to predict. With functionality and fast turnaround times the essential design ingredients, it seems safe to say that ASIC vendors and standard product vendors will be moving more and more toward ASSPs with predefined functional blocks that will tie the customer to the vendor. ■

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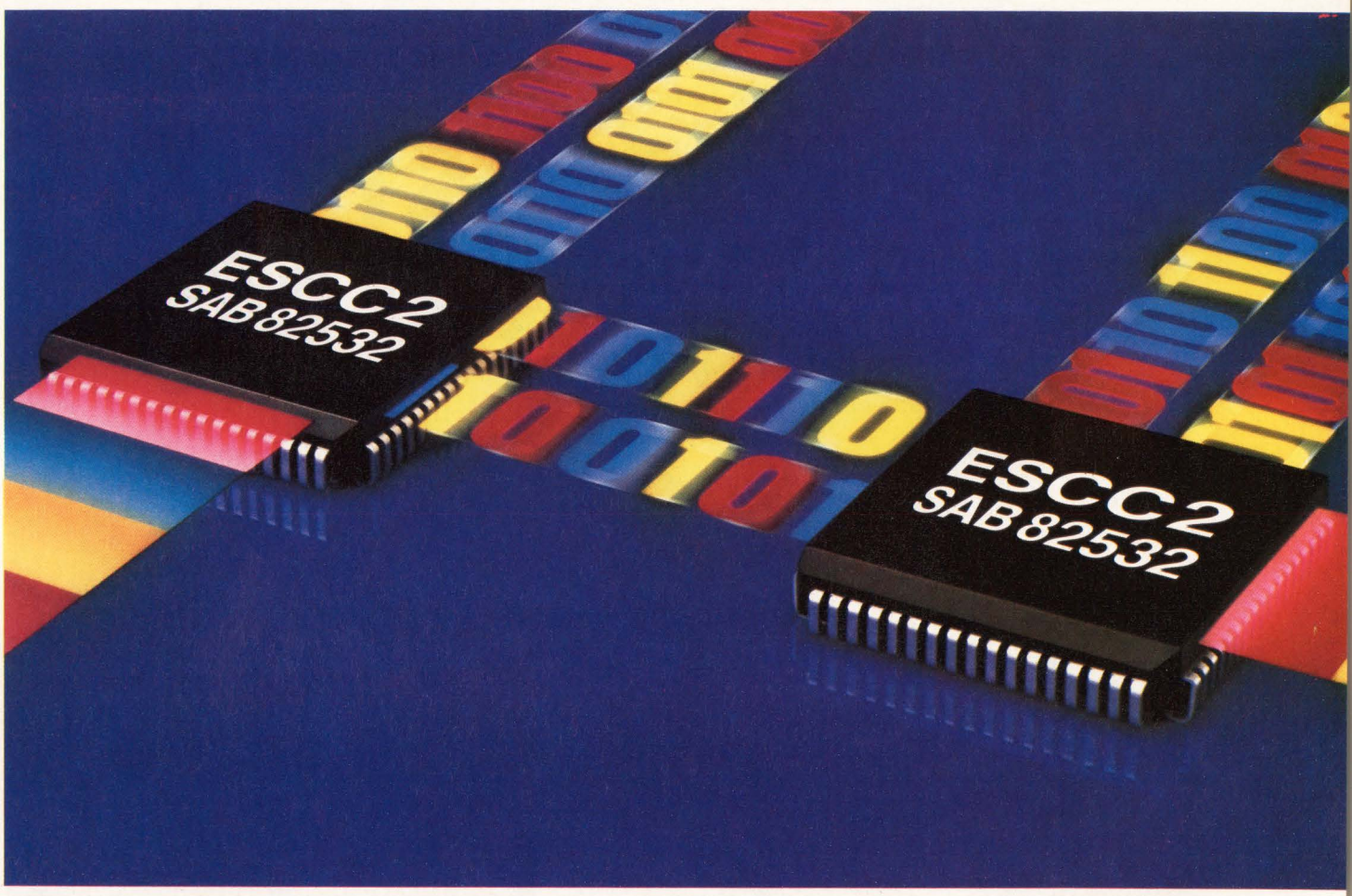

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CIRCLE NO. 57

Fuzzy logic simplifies complex control problems

Tom Williams
Senior Editor

Fuzzy logic is proving a powerful methodology for control applications. Over 2,000 patents have been issued in Japan. Now, development tools and hardware are becoming available in the United States, and application possibilities abound.

On close examination, "fuzzy logic" turns out to be like Fuzzy Wuzzy in the nursery rhyme, not so fuzzy after all. The inputs, calculations and outputs of fuzzy logic all involve precise numbers handled in a mathematically rigorous manner. What's vague about fuzzy logic is the linguistic expression of a problem and its solution, not the numeric representation. But a vague or general linguistic expression of a problem can be very powerful. It lets users develop and refine a numeric representation without requiring them to develop or even understand a detailed numeric model. In fact, fuzzy logic can now be applied to complex logical and combinatorial problems for which it's impossible to build numeric models because of the enormous number of possible combinations.

It's said that fuzzy logic deals with vagueness and ambiguity, and this is true. It deals with relations between fuzzy sets, first described by professor Lotfi Zadeh of the University of California at Berkeley. Consider whether a man of 50 is old, for example (see "Fuzzy logic works with degrees of truth," p 98). The fuzzy set OLD MEN might appear to be arbitrarily drawn, but a somewhat different curve could with equal justification represent OLD MEN. Different ages would yield slightly different degrees of membership. Such differences reflect the expert knowledge or research results that define the set. And not all experts agree 100 percent.

The mathematical precision of fuzzy sets derives from the precise mapping of input values to degrees of membership. The linguistic power of fuzzy logic lies in its ability to define and manipulate sets that contain varying degrees of membership without having to deal in detail with all the combinations they can produce. The descriptive power of fuzzy logic comes from its ability to let experts express their knowledge in language they understand.

How fuzzy logic works

The use of adjectives to describe a problem is one key to fuzzy logic's ability to accommodate ambiguity: adjectives describe an application's fuzzy aspects. For example, what does a person mean when using terms like "small," "large" or "fast"?

Membership functions and rules provide the ability to handle complex combinations easily, which is an important benefit of fuzzy logic. An application's rules and membership functions also contain the expert's knowledge about a system.

The adjectives used to formulate rules are more rigorously defined in an application's membership functions. The shapes of the membership functions can be changed, though "experience has shown that a relatively small number of triangular and trapezoidal membership functions is adequate for many control applications," according to David Brubaker, president of the Huntington Group (Menlo Park, CA) consulting firm.

When a processor scans an application's rule base, it tests each rule to determine whether its IF conditions have been satisfied. When the IF conditions are met, execution branches to the rule's THEN path, and the rule is said to have "fired."

Although a control application's logic may be fuzzy, the measured inputs from a physical system, and the outputs required to control it, will be precise. Precise values in fuzzy logic systems are termed "crisp."

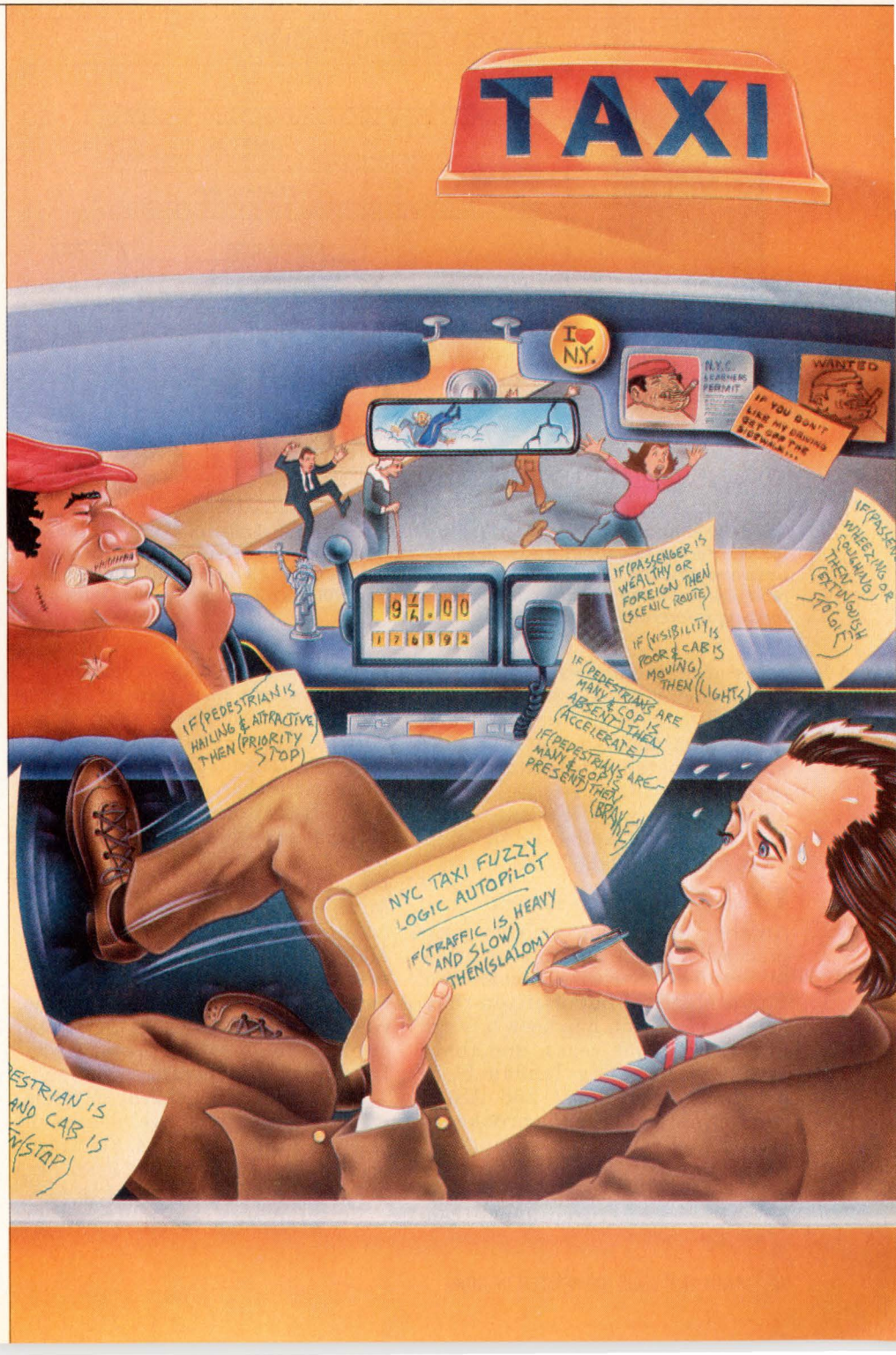
In most cases, several rules fire and contribute to the output. The output values must then be resolved to yield a crisp value. Current prac-

tice employs several methods to derive a precise output value from multiple-rule executions.

One common means of "defuzzification," obtaining a crisp output from a group of membership functions, is the centroid, or center of gravity, method. This requires overlaying the portions of output membership functions produced by several rules and calculating the center of gravity of the resulting shape as the final output value. Another popular method, called max height, involves selecting from a range of possible discrete output values the one that receives the greatest degree of belief from fuzzy processing. Yet another method is simply averaging the output values.

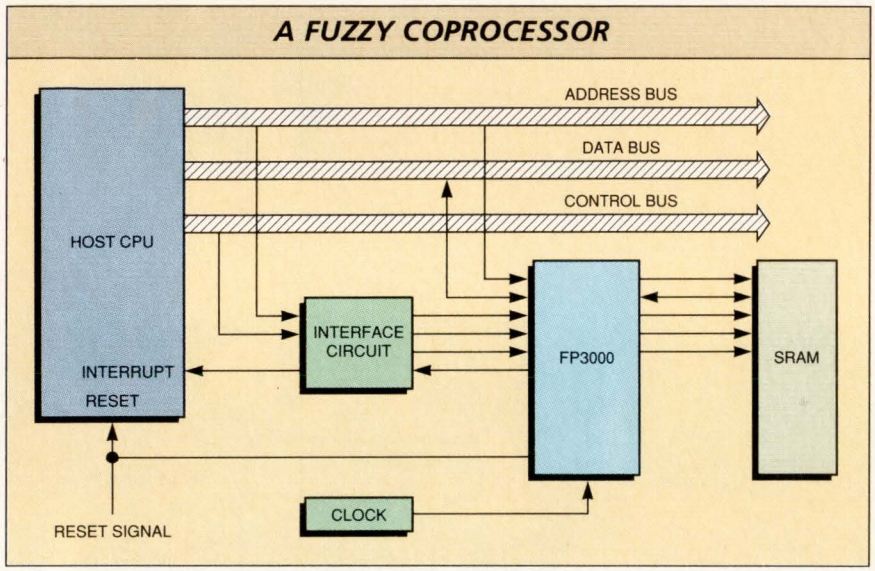
Fast and simple

The simplicity of the pendulum problem's expression (see "An example of fuzzy logic control," p 93)—11 two-input rules and three sets of five membership functions—suggests that fuzzy logic can handle much more complex problems with far fewer rules than traditional, crisp expert systems. "Nuances in the interpretation of rules can be handled by degree of membership functions without having to deal



with the detailed combinations that may arise," says Brubaker. "The result is that the number of rules goes way down." By relegating complex combinatorial problems to fuzzy sets, users are therefore allowed to express rules for the behavior of a system in the linguistic form that's closest to the way humans think.

The familiarity of the language used allows rapid description of problems, resulting in fast prototyping of fuzzy solutions. After establishing a "shell" (a minimal set of rules and membership functions that demonstrates feasibility), the designer can refine the system by experimenting with different rules and membership functions. Such prototyping is, of course, greatly aided if there's an adequate set of hardware and software development tools at hand.



The FP3000 fuzzy processor from Omron has an interface similar to that of an SRAM for interfacing to various hosts. In expanded mode with an attached SRAM for rule base memory, the FP3000 can handle up to three sets of 128 rules each. The host can read and write the rule memory whenever the FP3000 is idling, but not while it's performing inferences.

Fuzzy recognition system

Another application embeds fuzzy processing inside a database search to perform character recognition. The problem of handwritten-character recognition has been a tough nut to crack for years, and that's just in recognizing Roman block printing, or at most 256 ASCII characters. Imagine the problem of recognizing handwritten Japanese characters.

The new PTC-500 palmtop computer from Sony (Tokyo, Japan) contains a fuzzy logic database structure enabling it to recognize 3,535 hiragana, katakana and kanji characters. A built-in stylus lets users hand-write these characters on the screen. According to Hironobu Kawai of Sony's Supermicro Systems Group, the PTC-500 does it all with a 64-kbyte program in ROM and a ROM database of only 128 kbytes.

Complex kanji characters are classified into smaller groups of strokes. The strokes in those groups are then classified by their length, direction and relation to each other. The database is a tree structure, but the connections between nodes on the tree are fuzzy rules. A rule might state something like "IF line A is shorter than line B and parallel to B, THEN branch to the node that satisfies the greatest degree of belief in the conditions." That would be an example of max height defuzzification.

The attributes "shorter" and "parallel" are evaluated according to their membership in fuzzy sets. The database knows the standard forms of the characters and evaluates the stroke combinations for their degree of conformity to the standard.

Each stroke in a character takes the evaluation one level deeper in the tree-structured data. For every level down, a number of branches at that level may have a degree of validity. When the analysis has gone through all its levels, there may still be various "leaves"—nodes with no further branch paths—that are assigned some degree of validity. Some may even represent the same character, since there are about 1 million leaves in the entire database. The leaf with the highest degree of belief is turned into a crisp value and selected as the character to be recognized.

Complex controls

Some control applications may entail not only servo-type situations, such as the inverted pendulum, but also complex combinatorial problems, such as the efficient dispatch of elevator cars in a large building to minimize the individual waiting time for passengers. Mitsubishi Electric (Osaka, Japan) has applied fuzzy logic to elevator car dispatch and achieved a 15 to 20 percent reduction in average waiting time and a 30 to 40 percent reduction in long waits of 60 seconds or more.

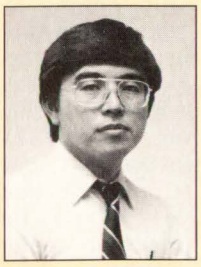
The AI-2100 Elevator-Group control system makes use of two kinds of fuzzy rule sets, off-line rules and on-line rules. Off-line rules use fuzzy logic to decide which on-line rules should be applied. Off-line rules decide, among other things, where cars not in use should be parked to ensure efficient dispatch in highly variable traffic demands. On-line rules are applied when hall calls are registered—that is, when somebody pushes a button. They include rules that prevent "bunching" by assigning calls so that cars don't travel in groups. This may result in an individual call not getting the car that could actually be there the quickest, but the overall waiting time is greatly reduced. The rules used were created by experts in group supervisory control.

An example of a rule preventing bunching is "IF a call from the high zone (of a building) is registered AND the number of cars ascending is large, THEN select a car from among those already ascending using an evaluation rule."

This prevents assigning another idle car to the group of ascending cars and running the risk that a call from a lower floor made after the dispatch decision will go unanswered for an unacceptably long time.

Using fuzzy logic, the system designer can make additions to the rule base to improve decision mak-

An example of fuzzy logic control



A classical example of how a fuzzy logic control system works is the problem of balancing an inverted pendulum, implemented here by Togai InfraLogic (Irvine, CA) in its TILShell development environment. A weight at the end of a shaft is mounted on an electric motor that's used to balance it in an upright position, as shown in the center window. If the pendulum starts to fall to one side, current is applied to the motor in the opposite direction to bring the pendulum upright again. A closer look reveals that there are three factors of interest: The angle (theta) between the pendulum and vertical; the speed (delta theta) at which the pendulum is falling; and the amount of current to be applied to the motor.

Intuitive reasoning would try to express some rules governing the system. It would tell us that if the pendulum is just a little bit off-center, a small amount of corrective current should be applied. But if the pendulum is off by a large degree and its speed is increasing rapidly, a large amount of current should be applied to bring the pendulum back to a stable position.

The key point here is that adjectives have been introduced to the description of the problem. It's the adjectives that constitute the "fuzzy" elements. Just what is "a little bit" or "a large amount"?

The actual inputs to any physical system trying to solve this problem will be exact in terms of degrees and degrees-per-second. And only a precise current output will make the system behave properly. Such values in fuzzy systems are called "crisp."

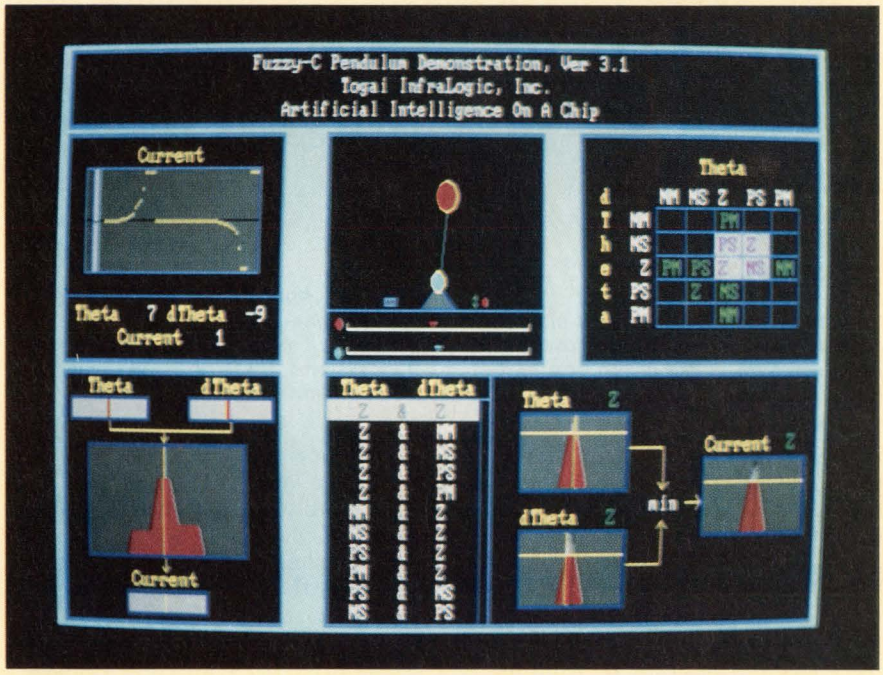
It's the rules that are general and the membership functions that are fuzzy because they cover complex combinations that otherwise would be unmanageable. The rules and membership functions are also the repositories of an expert's knowledge about a system. Once the expert writes "a little bit" in a rule, he or she must define what "a little bit" means in a membership function.

For the purposes of the pendulum problem, a set of five membership functions has been declared for each input: negative medium, negative small, zero, positive small, and positive medium. They can be shown graphically as a series of triangles and trapezoids that cover a range of –1 to 0 to +1. Actual input value ranges are normalized to this generalized range.

The next step is to become a little more linguistically rigorous and declare a set of formal IF-THEN rules, such as "IF angle theta is positive small and delta theta is zero, THEN current is negative small." Even though one membership function is called zero, there are still some small positive and negative values that belong to it. It could just as easily have been called "center." The upper right window shows the rule matrix. The inputs (IF) are along the axes of the matrix, and the outputs (THEN) are at the intersections.

When the processor scans the rule base, some rules "fire" according to the input conditions. In the screen's upper right window, rules that fire are highlighted in gray. When a rule fires, its IF conditions have been met, and execution branches to the THEN path of the statement. The rules are evaluated according to fuzzy logical operations, and various output membership functions are combined to produce a final crisp output. The lower center window shows the rule list with the membership functions of the highlighted rule displayed in the lower right window.

In this example, the output is a value of current to the motor. The lower left window dynamically shows how varying input values affects the combined output membership functions, and how those are "defuzzified" with the center-of-gravity method. The upper left window graphs the magnitude and direction of current to the motor.

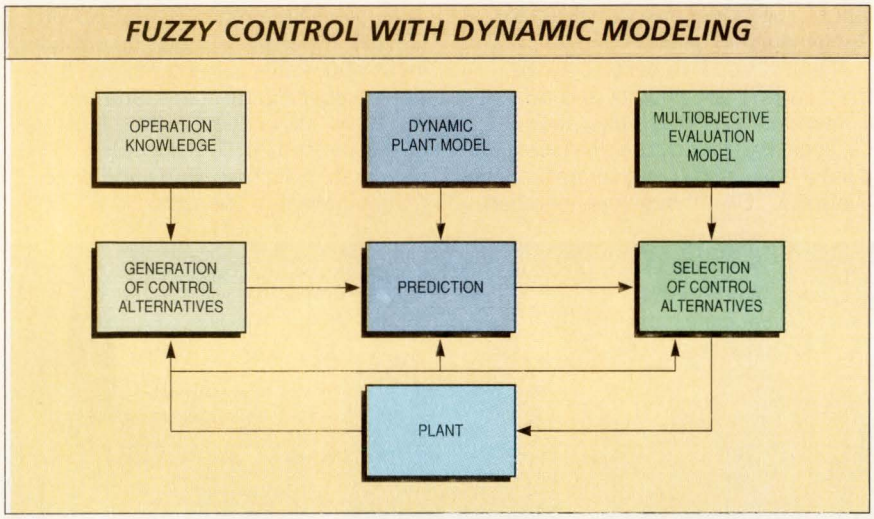


An inverted pendulum can be balanced with familiar binary logic. After all, the whole thing is carried out by a digital microprocessor system. But the natural language character of the problem's expression makes it easily understandable to persons whose primary expertise isn't computer science.

Fuzzy logic solutions are robust. In the pendulum example, the weight, the length of the shaft, and the strength of the motor can all be changed without altering the rules and membership functions. What changes is the scaling, or normalization, of input and output values.

Maski Togai, PhD, chairman and CEO, Togai InfraLogic

ing, without necessarily having to rewrite the program. For instance, since a hall button doesn't tell the system how many people are waiting on a floor, the elevator controller can add the factor of hall congestion to aid in car dispatch. A video camera compares its image of the hall and the people waiting with a stored image of the empty hall. Based on the image comparison, a membership value of empty, medium or heavy congestion is established and used by the fuzzy rule base as a factor in the decision to dispatch elevator cars.



In the predictive fuzzy control algorithm developed by Hitachi, control alternatives are gauged against a dynamic model of the system under control. The results are then evaluated according to how well they fit an overall model that may have multiple objectives. Unlike interrupt priorities in binary systems, these objectives may have priorities that are also characterized by a certain amount of fuzziness.

Control with multiple goals

Another way of handling a system with multiple goals was developed by Hitachi's System Development Lab (Kawasaki, Japan) in an intelligent train control. Starting and stopping a train smoothly and efficiently is a task that must achieve many objectives—for instance, running time, energy conservation, safety, comfort, and stopping accuracy—and some of them may not be entirely compatible. Hitachi has developed a predictive fuzzy logic system that evaluates the effects of several control commands to select the one that most satisfies all the system requirements. The result is a subway train in Sendai, Japan that's legendary for its ride and efficiency. Passengers don't even need hand grips when the train starts and stops within 1.5 cm of a mark on the platform.

Most of the previous examples involve control situations that are "smooth" in the sense that they don't involve random interrupts that require fast context switches and deadline scheduling. A fuzzy logic system is supposed to behave so as to maintain the illusion that all the rules in its rule base are evaluated simultaneously. Of course, they're evaluated sequentially like any other processor code.

A fuzzy logic system differs from traditional expert systems in that it has far fewer rules to evaluate. So the time constraint on a fuzzy-based system is that it can't be allowed to change so fast that control can't be maintained within the time the processor takes to scan the rule base. Thus, for more complex systems, there will be a constant push for more processor power and speed. Complex real-time systems characterized by large numbers of random interrupts probably don't lend themselves to fuzzy solutions yet.

Fuzzy logic processors

Given the advantages of hardware assist, it's not surprising to find that several companies are offering dedicated fuzzy processors. The most prominent are Togai InfraLogic (Irvine, CA) and Omron (Kyoto, Japan). Togai is marketing its FC110 processor as a separate part and as an integrated set of up to four processors on its FCA10VME accelerator board. Two dedicated fuzzy processors, the FP3000 and the FP5000, were developed by Apt Instruments (Sunnyvale, CA) and then licensed to Omron. Omron is expected to offer versions of the two processors in the United States by the middle of the year. Apt is also developing a VME-based board, the truth value flow inference (TVFI) module, that will incorporate a new proprietary fuzzy processor designed by Apt. Apt also intends to market the new processor separately in the United States.

The Togai FC110 is a 10-Mips CMOS RISC processor with a specialized instruction set for fuzzy rule base evaluation. These include six instructions for fuzzy rule evaluation, such as LHS for "left-hand side," which evaluates the IF portion of a rule. The RHSC instruction evaluates the THEN portion of a rule, using the center-of-gravity method for defuzzification. FZAND and FZOR instructions perform fuzzy AND and OR (min./max.) operations.

Rules, membership functions and the FC110's program instructions reside in a knowledge base memory (KBM). The KBM can be EPROM, RAM or ROM and have a maximum size of 64,000 16-bit words. Inputs and outputs are 8-bit precision, and membership functions have 8 bits of resolution as well. Depending on the complexity of the rules, the KBM can handle up to 800 rules with their membership functions, and the FC110 can perform up to 100,000 rule evaluations per second.

The Omron FP3000 is a 24-MHz (max.) part that's intended to run in a system as a coprocessor to a host microprocessor. It can execute 100 single-antecedent, single-consequence rules, or 20 five-antecedent, two-consequence rules in 650 ms. Rules can have up to eight antecedents and two consequences and can be arranged in up to three groups of up to 128 rules each. The FP3000 has an interface for external SRAM, which is where the rules and membership functions are stored. Membership functions have a resolution of 12 bits, so each function can associate 4,096 values with input variables.

Hybrid control strategies

This type of coprocessor arrangement for both the Togai and the Omron processors could lend itself to design of mixed fuzzy and crisp real-time systems. In such a system

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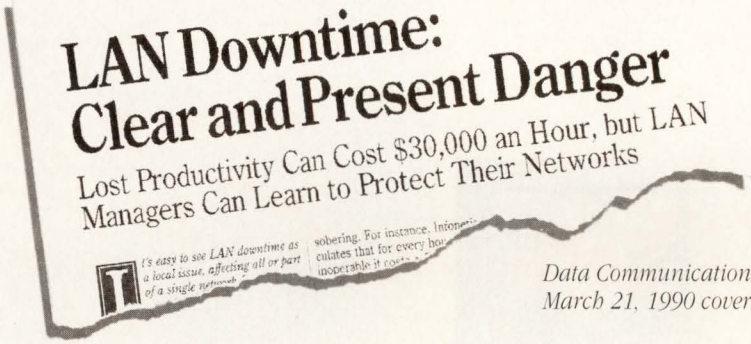

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Data Communications Magazine
March 21, 1990 cover story

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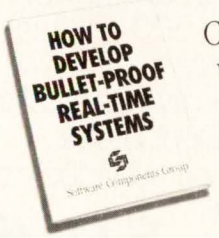

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the host CPU could accept and handle interrupts caused by external events while monitoring and controlling other functions using fuzzy logic. It's even possible for an external event to cause an interrupt that the CPU would service by invoking one or another fuzzy rule set to be run on the coprocessor as long as the system's time constraints could be guaranteed. Of these processors, the Togai FC110 is currently shipping in the United States; the Omron parts are expected to be available by second quarter 1991.

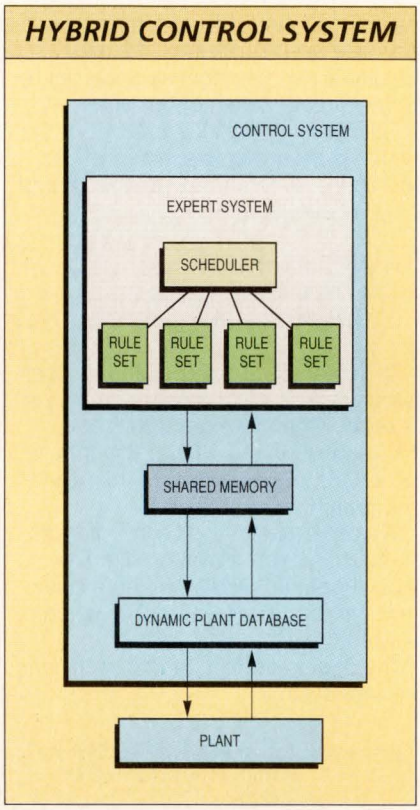
It should be noted that comparing performance figures for fuzzy processors is such a new game that the figures are truly fuzzy. Much depends on the kinds of rules—whether they have one, two, or more inputs and one or two outputs. The resolution of I/O and of membership functions also influences the "rules-per-second" performance claims, as does the kind of membership function used. A membership function represented by a triangle or trapezoid (that is, straight lines) where only the height, width and slope of the lines may be specified lends itself to interpolation or implementation as a lookup table. A curved membership function defined by an equation will necessarily take longer to compute than a triangular function.

A fuzzy logic system need not be digital. Apollo Electronics (Fukuoka, Japan) has developed a machine that's now used to evaluate the results of orthodontic treatment, but this machine is capable of being adapted to many specialized applications. It allows inferences to be made of pre- and post-treatment conditions compared with a more or less ideal norm. The ideal norm isn't achievable in all patients, and is based on the subjective knowledge and experience of experts, but an assessment of how close one has come and how good a job has been done can be made.

The Apollo machine uses a circuit board for each tooth, and membership functions have been set as analog values by adjusting variable resistors. This makes it easy to change the membership functions as well, since each board contains its own rule set and membership functions. The "before" and "after" values are entered with potentiometers, and an assessment is given for each tooth and then an overall assessment is inferred. This same technique used for such a specialized application as orthodontics has potential for many types of complex analysis that require expert knowledge and for which there isn't an absolute norm.

Fuzzy development tools

Engineers with real application problems need more than new, unfamiliar processors. They require board-level products and software development environments to develop and prove design concepts and build first-generation products. "Fuzzy logic is applied in the United States today, but only by engineering companies such as Apt and Togai who do projects for customers," says Xiwen Ma, vice-president of R&D for Apt Instruments. "The availability of tools and hardware should make fuzzy logic available to general engineering."



In the expert system developed by Mitsubishi Electric, Boolean logic-based rules are used by the scheduler to focus on fuzzy rule sets to apply to given situations. The system interacts with the plant model via shared memory, so it can easily be applied in distributed configurations.

Development tools for fuzzy logic are available, and more are on the way, both from the United States and from Japan. Omron, for instance, has been offering its digital signal processor-based FZ3000 fuzzy logic board with the FT6100 support tool in Japan for some time. The FT6100 runs on the NEC 9801 personal computer, and so would require some modification for the U.S. market. Mitsubishi Atomic Power Industries (Tokyo, Japan) has a development toolset, called Fuzzic-1, that's written in QuickBasic for the NEC 9801. And the company has announced plans to convert Fuzzic-1 to C and port it to Unix for marketing in the United States.

Fuzzic-1 allows the user to graphically specify rules and membership functions and to simulate the behavior of the target software on-screen before compiling it to run on the target system. It's possible to watch shaded areas of membership function graphs change with input variables and to observe the effects on output membership functions. This allows the user to experiment with different rules and membership function specifications to try to optimize the application's performance.

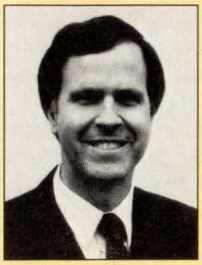
Fuzzy CASE system

Togai currently offers its FC110-based VME board and a development environment, called TILShell, that runs under Microsoft Windows. TILShell could almost be called a fuzzy CASE environment. It starts out with a facility that lets the user graphically define the structure of a fuzzy system using input, output and processing objects that can then be assigned attributes. Attributes can define storage type, range of values, and membership functions.

TILShell also contains a membership function editor that lets the user graphically define the shape of a set of membership functions associated with a variable. Straight-line-type membership functions can be drawn with a mouse using the editor's point-and-click tools. If an application requires membership functions that are complex curves, such as a bell-shaped distribution curve, an equation editor lets the user specify the membership function using a set of math functions. A fuzzy editor works with a rule editor and a fragment editor to allow the user to define and edit rules and to add and delete rules and C code fragments to and from the rule base. The rule editor is menu-driven, while the fragment editor lets the user enter and edit C source code as text.

Once the fuzzy logic system has been defined, TILShell provides three options for generating code. The Fuzzy-C compiler generates C

Fuzzy logic works with degrees of truth



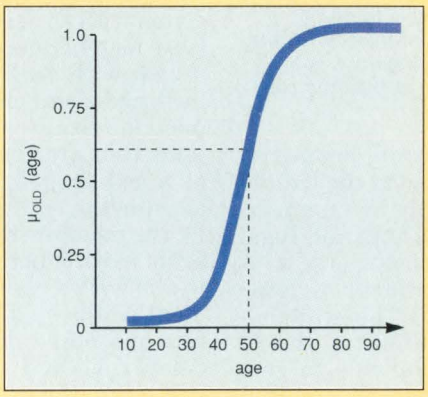
Fuzzy logic is an extension of traditional bilevel (or Boolean) logic. While Boolean logic requires a statement or a condition to be either completely TRUE or completely FALSE, fuzzy logic allows partial truth and partial falseness.

For example, consider a 50-year-old man. To say that he is OLD isn't entirely true, and yet we likewise can't say that he's NOT OLD. We're dealing with an in-between region, in which traditional logic has problems.

Turning to fuzzy logic, we can create a function relating age in years to oldness, and given this, we can say that the statement "the 50-year-old man is OLD" is 60% TRUE. The statement is also necessarily 40% FALSE. An assertion being simultaneously TRUE and FALSE is often a difficult concept for someone used to working with Boolean logic, but the world tends to be more gray than black-and-white.

Fuzzy logic is derived from the more-general theory of fuzzy sets. Using fuzzy sets to represent the previous example, we can say that the function relating age to oldness is a curve relating age to a degree of membership in the fuzzy set OLD. Degree of membership is typically designated μ, and the degree of membership of the fuzzy set OLD as a function of age is given by $\mu_{OLD}(age)$. For consistency with traditional logic, μ ranges from 0 to 1, with 0 indicating null membership in the set and 1 indicating full membership.

A possible function for $\mu_{OLD}(age)$ is shown in Figure 1 (at right). The age 50 years is a member of the fuzzy set OLD with degree of membership $\mu_{OLD} = 0.6$. We might similarly say that the 50-year-old man is a member of the set OLD with degree of membership $\mu_{OLD} = 0.6$.



Fuzzy logic variables can be combined using operators similar to those for their Boolean cousins, although the operations are necessarily defined differently. The standard fuzzy operations are AND, OR and NOT, which correspond respectively to INTERSECTION, UNION and COMPLEMENT for fuzzy sets. Although many definitions of fuzzy logic operators have been suggested, the most popular are those originally proposed by professor Lotfi Zadeh of the University of California at Berkeley. In terms of the degree of their membership functions, operations on two fuzzy variables A and B are defined as

$$A \text{ .AND. } B = \min.(\mu_A, \mu_B)$$
$$A \text{ .OR. } B = \max.(\mu_A, \mu_B)$$
$$\text{.NOT. } A = 1 - \mu_A$$

To demonstrate the use of fuzzy operators, we shall expand our example. Let us say our friend weighs 200 lb and that $\mu_{HEAVY}(200\text{ lb}) = 0.91$; and that he has a waist measurement of 36 in. and that $\mu_{FAT}(36\text{ in.}) = 0.75$.

We can evaluate the degree of truth of the expression (Waist is .NOT. FAT) .AND. (Weight is HEAVY)—this includes an instance of the fuzzy .NOT. operator as well.

The degree of membership of the entire expression is

$$\mu_{expression} = (1 - \mu_{FAT}) \text{ .AND. } (\mu_{HEAVY})$$
$$= \min.(1 - 0.75, 0.91)$$
$$= 0.25$$

This expression also sets the stage to introduce the dominant fuzzy control mechanism—the IF (condition) THEN (action) rule. Borrowed from expert systems, it requires that actions be executed if the condition part of the rule is at least partially true. But in a fuzzy system, this structure also has a powerful twist: *the action is executed with the degree of membership of the rule's condition.* If a condition is only minimally true—say, for example, $\mu_{condition} = 0.1$, then the action is executed with that same μ, $\mu_{action} = \mu_{condition} = 0.1$.

Returning to our example, we would like to devise some rules to help our friend lose weight. While both diet and exercise are appropriate, for this example we shall address only diet.

We will work with two inputs, Waist and Weight, and each will be represented by two fuzzy sets—NORMAL and FAT for Waist, and NORMAL and HEAVY for Weight. We shall define a single output, Diet, which will also have two fuzzy sets—WEIGHT LOSS and MAINTENANCE.

Given these, we can create a two-rule system to govern our friend's eating habits:

- IF (Waist is FAT .AND. Weight is HEAVY) THEN (WEIGHT LOSS)
- IF (Waist is NORMAL .AND. Weight is NORMAL) THEN (MAINTENANCE)

Figure 2 (facing page) shows how these rules would be applied to his current condition. The control flow of the figure starts in the lower left corner (the inputs) and is vertical as the inputs are translated into degrees of membership (μ's) in the input fuzzy sets. The flow then proceeds horizontally toward the right, as the inputs and their μ's are applied as conditions to the rules. Finally, the flow moves downward toward the lower right corner (the output), as the rule actions are translated into an actual crisp output.

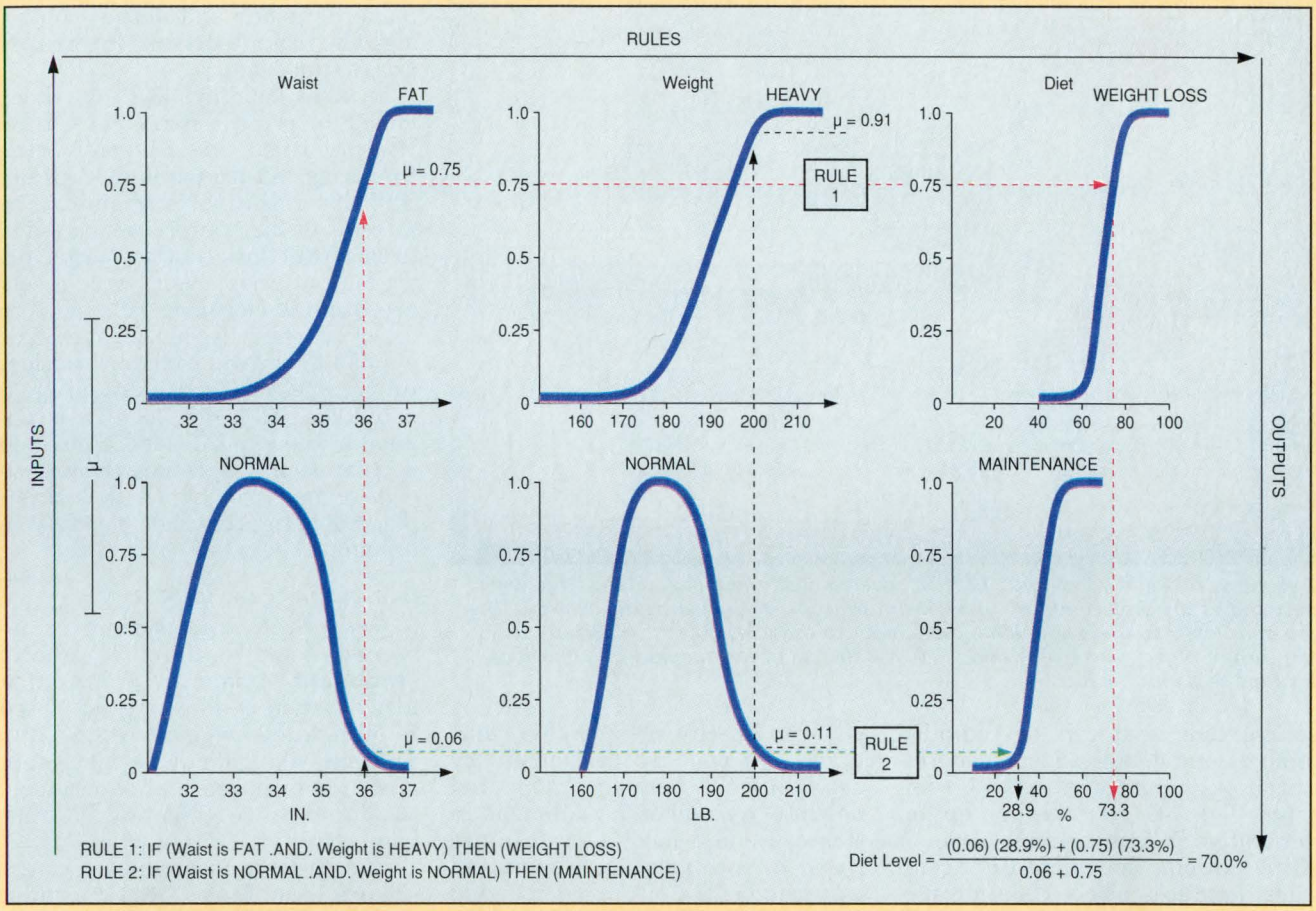
The sequence may seem complex at first, but it's actually straightforward. Let's step through the single iteration shown in the figure:

The current waist measurement, 36 in., is applied to the two fuzzy sets, FAT and NORMAL, for the input Waist, resulting in $\mu_{FAT} = 0.75$ and $\mu_{NORMAL} = 0.06$. Our friend's waist is obviously more FAT than it is NORMAL.

His current weight, 200 lb, is applied to the two fuzzy sets, HEAVY and NORMAL, for the input Weight, resulting in $\mu_{HEAVY} = 0.91$ and $\mu_{NORMAL} = 0.11$. Again, his weight is far more HEAVY than it is NORMAL.

The condition of Rule 1 requires a degree of membership (μ) of the expression (Waist is FAT .AND. Weight is HEAVY). The .AND. is performed using

David L. Brubaker, PhD, president, the Huntington Group



the minimum function, resulting in

$$\mu_{expression} = \text{min.}\ (\mu_{FAT}, \mu_{HEAVY}) = \text{min.}\ (0.75, 0.91) = 0.75$$

The μ of the rule's condition is applied to the rule's action, in this case (for Rule 1) WEIGHT LOSS. Rule 1 results in a Diet level of 73.3% (in this example a 100% diet corresponds to fasting and 0% to complete gorging).

Similarly, for Rule 2 the condition requires the μ of (Waist is NORMAL .AND. Weight is HEAVY).

$$\mu_{expression} = \text{min.}\ (\mu_{NORMAL}, \mu_{NORMAL}) = \text{min.}\ (0.06, 0.11) = 0.06$$

The μ of Rule 2's condition is also applied to its action, MAINTENANCE. Rule 2 therefore results in a Diet level of 28.9%.

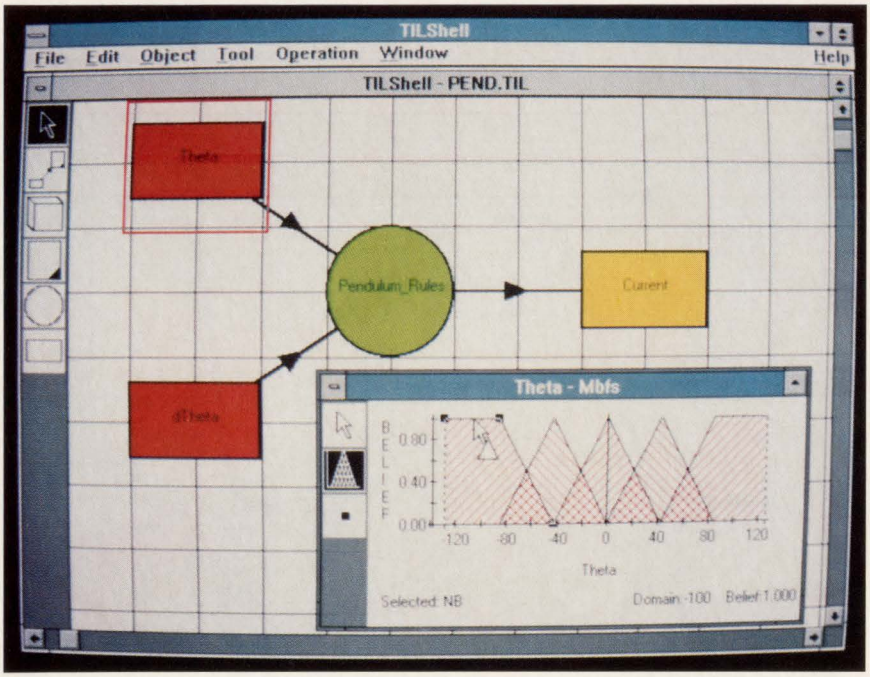
Finally, several techniques exist for combining these two outputs into a single, executable action. One of the more intuitive methods is to use an average, weighted by the respective degree of membership values. If we take this approach, the solution is

$$\text{Diet level} = \frac{(0.06)(28.9\%) + (0.75)(73.3\%)}{0.06 + 0.75} = 70.0\%$$

The required action is that our friend participate in a fairly heavy duty diet.

This has been a single iteration. To achieve the desired end result (shown by the two NORMAL curves to be a waist measurement of 33 to 34 in. and a weight of 180 lb), the rules will be executed on an on-going basis. As Diet (dominated by its WEIGHT LOSS component) is executed, both inputs (Waist and Weight) will start to decrease, resulting in lower μ's for both FAT and HEAVY and higher μ's for both NORMALs. Ultimately Rule 1 will cease to have a significant effect, and Rule 2 will dominate, dictating execution of a MAINTENANCE diet. If the MAINTENANCE diet is set too low (allows too great a fat and caloric intake), our friend may start regaining his lost weight, and the WEIGHT LOSS component of Diet will again become increasingly active.

Surprisingly complex and powerful systems can be implemented by extending these basic techniques. The use of the fuzzy logic is especially appropriate, and often necessary, for complex systems, where an adequate system model is difficult or impossible to define; expert-controlled systems; systems with moderately to very complex continuous inputs and outputs; and systems where vagueness is common, such as those used in economics, natural sciences, and behavior sciences.



Two views of Togai InfraLogic's TILShell development environment. The large window shows the project editor's view of the structure of the pendulum example. The red input objects, theta and delta, theta input to the rules object, which outputs to the current object. The small window shows the set of five membership functions for the theta input object.

source code that can be compiled and run and debugged on a general-purpose computer that has a C compiler. The FC110 compiler option generates FC110 machine code. A third option, the micro-FPL compiler, produces object code for several popular microprocessors, such as the MC 680X0 family and the H8.

Fuzzy design environments

For its new TVFI board, Apt Instruments is developing a software development environment called Fide (Fuzzy Inference Development Environment). Fide is expected to be available about the same time as the board (second quarter of 1991). The TVFI board is intended to operate in a system environment with a host CPU. At system boot-up, the application running on the host selects the appropriate fuzzy rule sets from disk files and loads them into the board's local memory. The host then places input data into input buffer space and reads outputs from output buffers in the board's memory.

Fide consists of a rule language, a compiler, a simulator, a debugger, and a graphical interface. The rule language is simple, according to Ma. To specify rules, you use simple IF-THEN constructs. There are two ways to specify membership functions. You can list parameters by specifying the midpoint, slope and height of a membership function. In this case, intermediate values are found by interpolation. The second way is to list the entire membership function as a lookup table. Input value ranges are normalized to a zero-to-one scale, and membership functions have 8 bits of resolution. The TVFI compiler compiles the rules and membership functions into code that the board's new processor can use.

A fuzzy system differs from traditional expert systems in that it has far fewer rules to evaluate.

Several Japanese companies have created in-house development environments for fuzzy application development. Besides Mitsubishi Atomic Power Industries, which created Fuzzic-1 for internal needs, Mitsubishi Electric has developed an environment, called Eric (Expert Real-time Intelligent Control), that uses both crisp and fuzzy logic in a hierarchical structure. Systems designed with Eric use a fixed time cycle in which they take in data, make decisions and output control signals. Event-driven interrupts aren't supported.

It takes roughly 30 to 40 times longer to process fuzzy rules than Boolean rules, the trade-off being that crisp rule sets are much larger. Still, it's desirable to minimize the amount of fuzzy processing needed to ascertain the situation. With Eric, a group of crisp, Boolean rule sets are used as "focusing rule sets" to select which fuzzy rule set should be applied to a given control situation. Advantages are thus drawn from both types of logic: Boolean is applied at the upper level of control to determine quickly where the knowledge of an expert, which is best implemented in fuzzy logic, needs to be brought to bear.

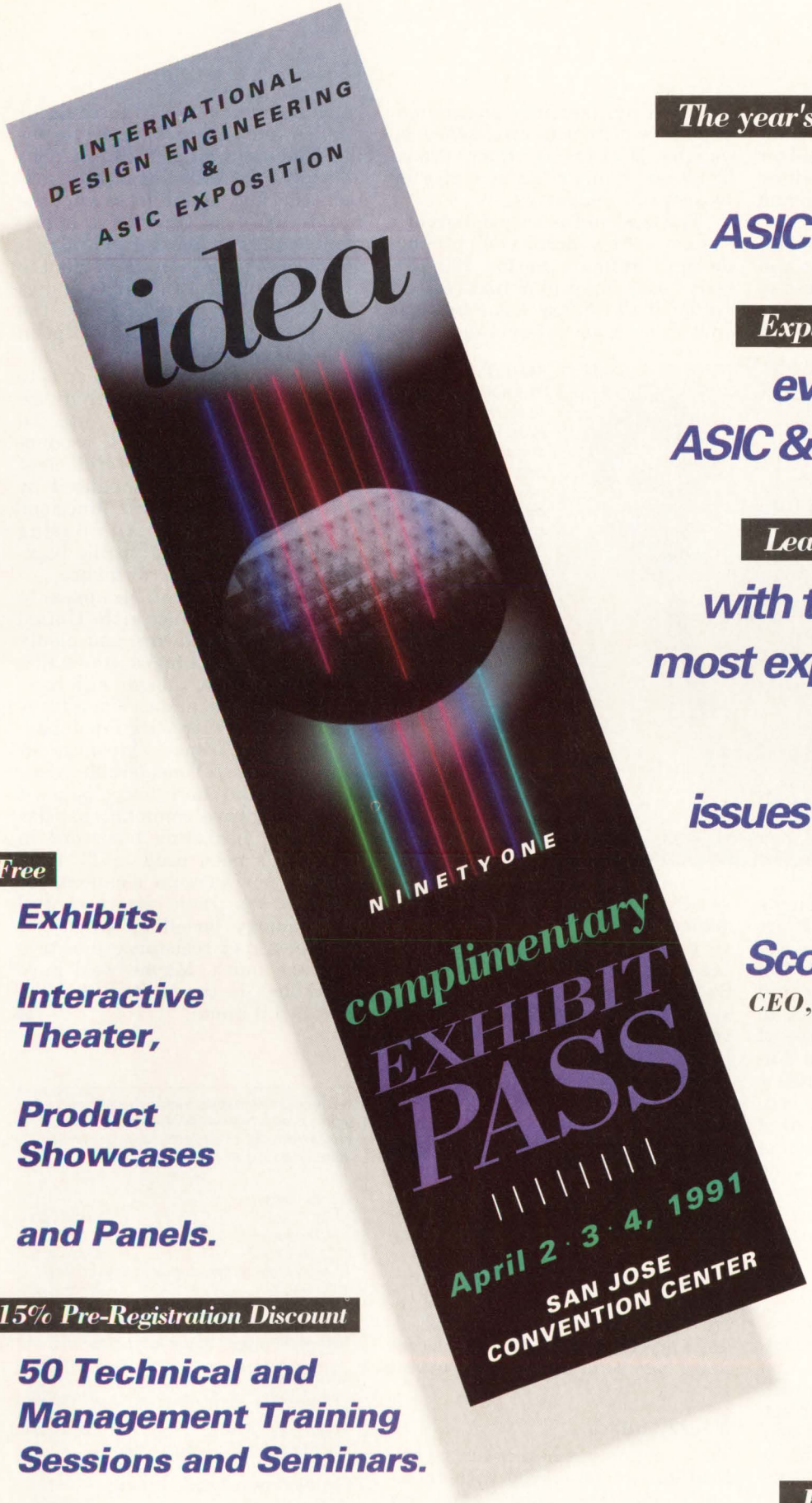
Issues in fuzzy logic

Since a fuzzy logic system is designed from humans' linguistic statements about a situation, a fuzzy system is only as good as the human knowledge it represents. That knowledge may be very deep, gathered over years of experience, but it can have gaps and be fragmentary.

"Fuzzy logic is engineering, not science," cautions Toyoo Fukuda, manager of the advanced systems group for Mitsubishi Electric. "In control, for example, it's necessary to verify if the system is stable. We can't show that through fuzzy logic." In other words, fuzzy logic is still a young discipline and lacks the theoretical basis for proving its validity. The alternative to theory is empirical verification, which by its very nature can seldom be complete.

Reliability proven empirically

The lure of fuzzy logic is that by using human experience, it's fairly easy to get a system to seem to work. But a great deal of analysis, research and simulation is often required to get it to work well and to establish confidence in its reliability. For example, Matsushita (Osaka, Japan) has introduced various consumer products that incorporate fuzzy logic. These include a vacuum cleaner, rice cooker, a camcorder with image stabilization, a kerosene heater, and a washing machine. The washing machine has a single but-



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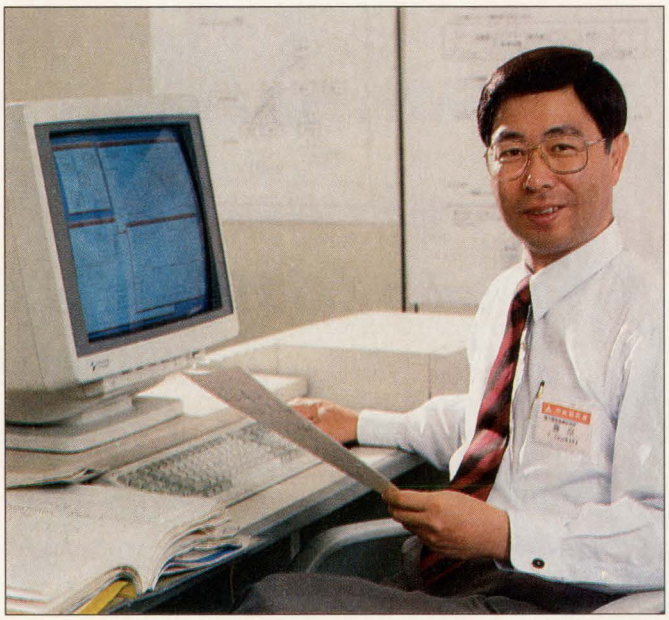
ton. It's able to sense both the size of the load of clothes and the amount and type of dirt—whether it's soil- or oil-based—and automatically adjust the amount of soap and water and the washing time.

The load is sensed simply by filling a preset amount of water and turning the agitator a few times to measure the current drawn before starting the cycle. The amount and type of dirt is sensed by a single optical sensor. The sensor and its logic measure how much the water is clouded, how long it takes for the clouding to reach saturation and what the level of saturation is to determine the type and degree of dirt. According to Yoshihiro Fujiwara, director of the intelligent electronics lab at Matsushita's central research laboratory, "You need to gather a lot of data and do a lot of simulation before you can determine these things." Once a prototype is developed, rules and membership functions must be refined by further simulation and analysis.



Matsushita's Yoshihiro Fujiwara feels that fuzzy logic is particularly suited to consumer products because of its ability to deal with nonquantifiable concepts. "Consumers want a good human/machine interface, so the nonquantifiable image or concept is familiar to the user of appliances incorporating fuzzy logic."

Verifying performance

There are two major theoretical problems facing fuzzy logic today, according to Fujiwara. One is that there is as yet no rigorous mathematical way of verifying the correctness of a fuzzy system. The second is that it's not currently possible to optimize the efficiency of a fuzzy system to an assured level of 100 percent. Exploring solutions to these problems is the main goal of the Laboratory for International Fuzzy Engineering (Yokahama, Japan), which was established by Japan's Ministry for International Trade and Industry and is supported by some 50 companies.

"The trade-off is easy design of a system at the sacrifice of optimum design; optimum means 100 percent," says Takeshi Yamakawa, director of the Fuzzy Logic Systems Institute, a privately funded research foundation. "But if we can achieve 95 percent efficiency, that's very good, and it's easy to design at the sacrifice of that last 5 percent." So it's possible to know that a fuzzy system is working better than a conventional one, and even to measure how much better, but we still can't know exactly how good a fuzzy system can potentially be.

According to Yamakawa, simulation is the ordinary way to verify a system using fuzzy logic, but it hasn't been sufficient to gain the confidence of mathematicians and control engineers. "But some in the fuzzy field have recently begun to research the stability and reliability of fuzzy systems," says Yamakawa, "so it will be easier for mathematicians and control engineers to accept fuzzy logic, and that's an important step."

Fuzzy trends

The question is whether fuzzy verification can be solved with traditional equations. Both Yamakawa and Fujiwara see hope in the use of neural networks, which are being used by Matsushita to develop rules and membership functions for applications. A neural network has the combinatorial power to exercise all of the possible input combinations of a rule, and to show what the results will be. "The rule is implemented and run, and the neural network shows the results of all the different input conditions," says Fujiwara. "So you can shape the membership functions to correspond with what the results will be."

Matsushita's next likely step is to move the neural network from the development environment into the product. Through use, a product would "learn" to be more efficient and become more personalized by tuning its membership functions and, possibly, by eliminating unneeded rules from its rule base, resulting in faster performance.

Fuzzy logic applications appear to be ready to come of age in the United States. Tools, hardware and plenty of application examples are available. Some people, though, still have trouble with the name. When fuzzy logic was first introduced in Japan, it was called "aimai" (Japanese for fuzzy), and met considerable resistance. But the word "fuzzy," since it has no negative connotations, has become a marketing buzzword in Japan—it's been used in TV commercials for vacuum cleaners, for example. It's ironic that a control methodology based on linguistic principles met resistance due to a language quirk. Maybe we'd have better luck in the United States if we called it aimai. ■

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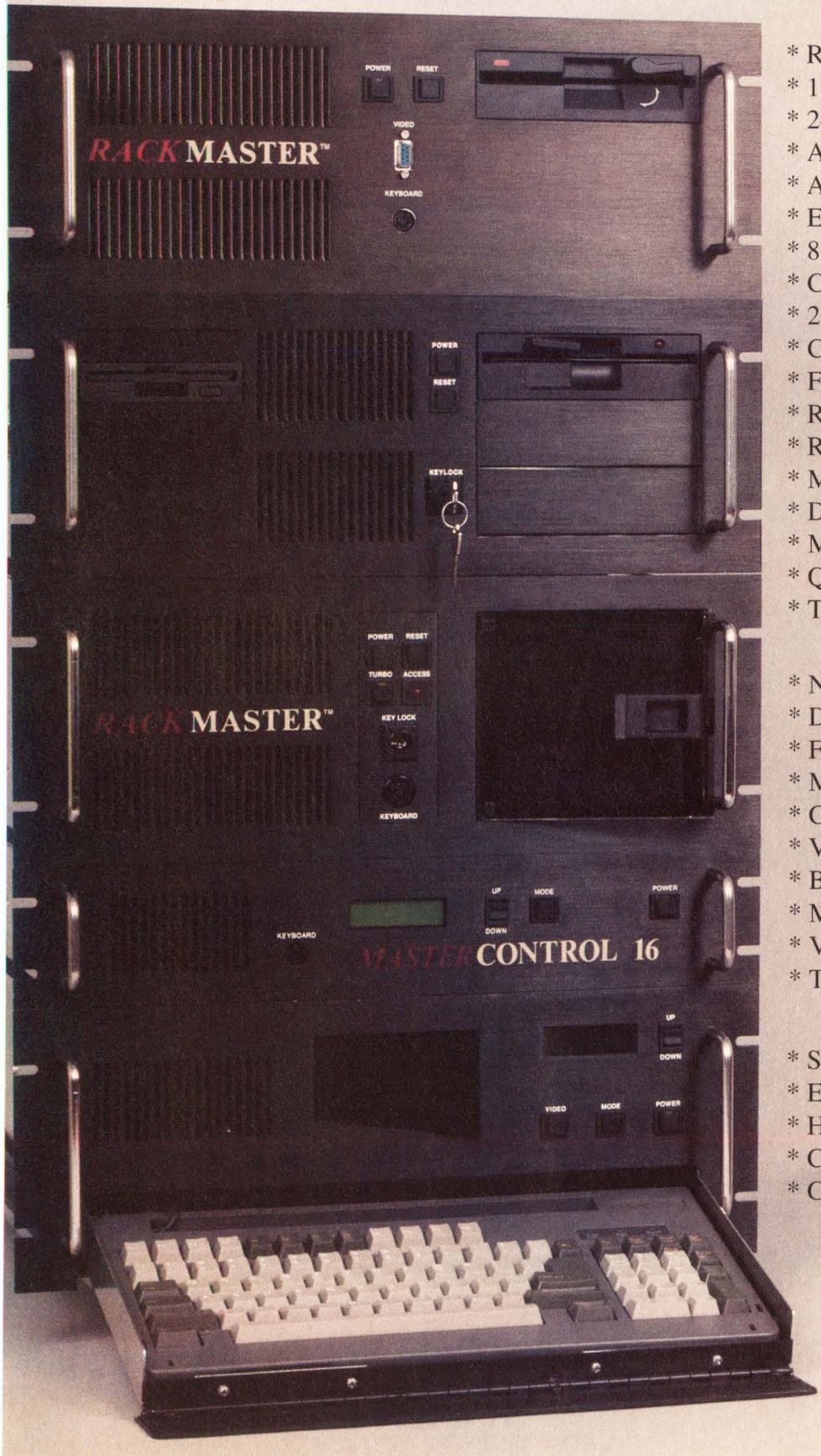

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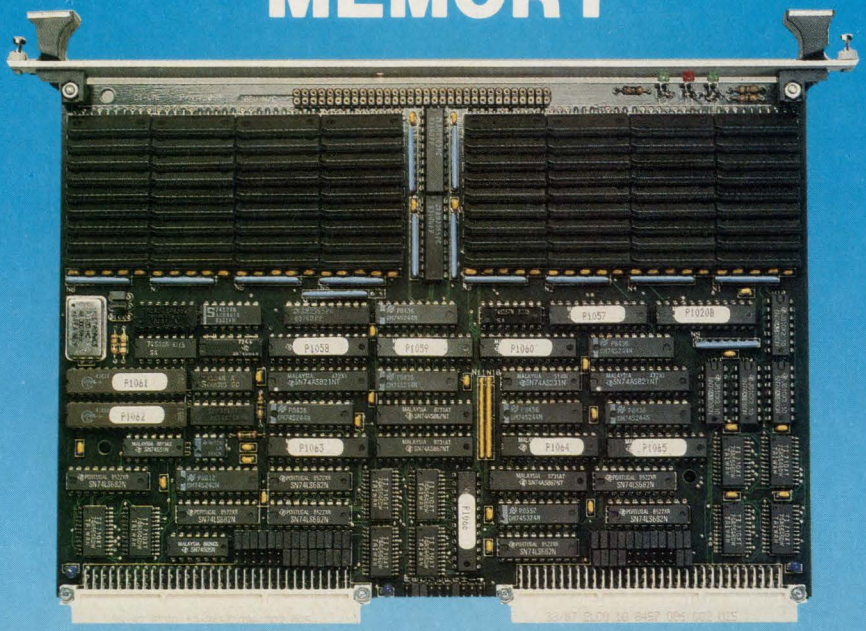

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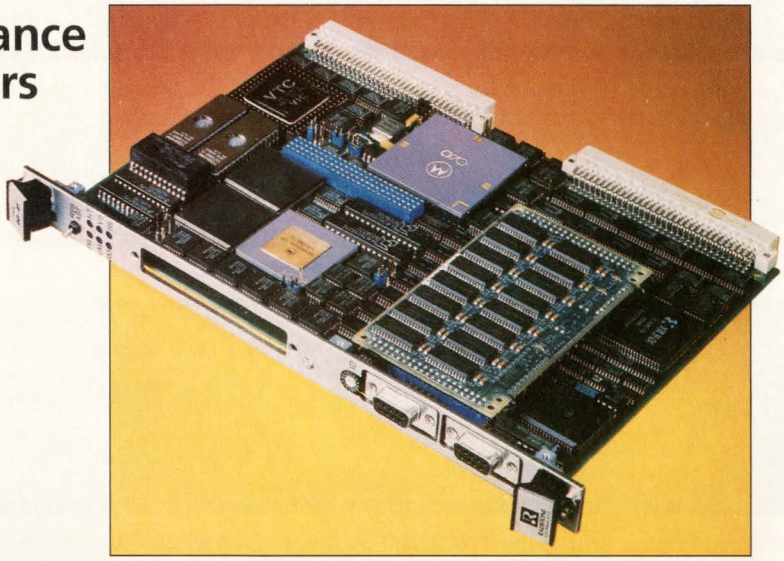
High-performance microprocessors push limits of VMEbus

Jeffrey Child, Associate Editor



The 68-41 from Radstone Technology takes a dual-processor approach to offload the 68040 from I/O tasks. A dedicated 68020 processor on the board controls a complete intelligent I/O subsystem, letting the board operate at full performance even when all its local and external interfaces are in use.

Advances in ICs and system architecture have pushed the VMEbus bandwidth to the limit and beyond. While board vendors are preparing for next-generation designs in VME64 and Futurebus+, many are also squeezing what they can from the existing VME standard. Designing boards based on state-of-the-art microprocessors, like the 68040, have forced board designers to get creative as they try to extend the performance of VME.

In order to minimize traffic on the VMEbus, designs must provide alternate paths over which data can be sent. To do this, mezzanine buses, custom on-board subsystem buses, and the VME subsystem bus (VSB) are being used to provide the necessary bandwidths.

While the majority of VME CPU cards are based on Motorola 68000-family processors, the board business is becoming less single-minded.

More processors

"In the past you were either of the Intel religion or the Motorola religion, and no one really crossed those boundaries," says Todd Wynia, marketing product manager at Heurikon (Madison, WI). "Now, with some of the software ventures that have come about, the transition from one processor to another has become more transparent. Today people are more willing to put aside their religious affiliation to a particular CPU architecture and are moving to whatever will give them the performance needed for their applications." And an increasing number of new products are based on alternative RISC and CISC microprocessors.

Despite the creeping of RISC processors into VME, the 68040 offers one irresistible factor: it's code compatible with previous generation 680X0 cards. At least a dozen companies are offering 68040-based boards. These implementations range from simple 68030-to-68040 upgrades to innovative architecture aimed to get the most out of the 68040. While methods vary widely, most high-performance designs based on the 68040 involve freeing the main processor from I/O tasks.

"People are more willing to put aside their affiliation to a particular CPU and are moving to whatever will give them the performance needed for their applications."

—Todd Wynia, Heurikon

Integration yields flexibility

"You're still faced with trying to squeeze as much power as you can on a single-slot board," says Joel Silverman, marketing manager for commercial products at Radstone Technology (Montvale, NJ). "At the same time you need to provide enough flexibility so you can really make use of that processing power and avoid wasting it."

Exemplifying this trend is Radstone's 68-41 board. Using a dual-processor approach, the 68-41 features a complete 68020-based I/O subsystem that offloads the main 68040 processor from I/O tasks. The intelligent I/O subsystem lets the board operate at full performance even when all its local and external interfaces are in use. Combined with up to 4 Mbytes of dedicated I/O memory, a dedicated 68020 processor forms the core of the 68-41's I/O subsystem.

Working with the gateway controller and datapath ASICs, the board's 68020 initiates DMA-type movements that handle data flow between the 68040 processor and I/O areas. This eliminates I/O bottlenecks and allows maximum data throughput. Also part of this subsystem is an intelligent SCSI interface offering an internal SCSI processor, on-chip 32-byte FIFO, a built-in DMA controller, and SCSI-2 capability.

Besides making use of multiple processors, the 68-41 also enlists multiple buses to allow maximum data throughput. To accomplish this the board offers two high-performance bus interfaces. First is a 32-bit VMEbus, implemented by the VIC068 interface with the aid of a 40-Mbyte/s DMA controller. The

Model	CPU	CPU clock speed (MHz)	Math coprocessor	Memory (bytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/ interboard expansion	Price
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XC120	68020	20	68881/2	2 M	90	—	3 RS-232/422	—	—
XC103	68000	12.5	—	512 k	90	2 or 4	5 RS-232/422, 8 or 16 A-D/D-A	—	—
American Eltec 479 S Marengo Ave, Pasadena, CA 91101 (818) 449-1558									**Circle 302**
Eurocom-6	68030	20, 25, 50	68882	1-32 M	320	—	4 RS-232, 2 parallel, 1 SCSI	mezzanine, IPIN	$4,200
Eurocom-7	68040	25, 33	—	4-16 M	280	—	4 RS-232/422, 2 parallel, 1 SCSI	mezzanine, IPIN	—
Eurocom-80	88100	25	—	4-32 M	320	—	4 RS-232/422, 2 parallel, 1 SCSI	mezzanine, IPIN	$6,900
Compcontrol 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032 (408) 356-3817									**Circle 303**
CC103	68020	16	68881	1 M	—	1 32-bit	2 RS-232	interboard connection	$5,425
CC112	68030	20	68882	4-16 M	—	—	2 RS-232, 1 SCSI	—	$4,179
Concurrent Computer 1 Technology Way, Westford, MA 01886 (800) 631-2154									**Circle 304**
Series 7000	68040	25, 33	in CPU	8-32 M	80	1	1 Ethernet, 4 RS-232	—	$14,500
IBIM	68030	40	68882	4 M	50	1	1 mezzanine, 1 general I/O	mezzanine, 32-bit interboard	$5,000
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VMPU-4M	68020	16	68881	4 M	100	—	1 RS-232	—	$2,950
VMPU-SBC	68030	25	68882	4 M	100	—	2 RS-232	—	$3,650
DY-4 Systems 21 Fitzgerald Rd, Nepean, Ontario, K2H 9J4 (613) 596-9911									**Circle 306**
SVME-144/ DMU-144	68040	25, 33	—	4-16 M	80	1 32-, 64-bit	2 EIA-232	VSB or SCSI	—
SVME-148/ DMU-141	68030	20, 25	68881/2	1-16 M	—	1 32-bit	2 EIA-232	VSB	—
SVME-153/ DMU-152	68020	16/20	68881/2	512 k-4 M	—	1 32-bit	2 EIA-232	—	—
Dynatem 15795 Rockfield Blvd, Suite G, Irvine, CA 92718 (714) 855-3235									**Circle 307**
DCPU30	68030	20	68882	2 M	100	—	1 sync/async, 3 async, 24 discrete	custom bus	$2,417
Force Computers 3165 Winchester Blvd, Campbell, CA 95008 (408) 370-6300									**Circle 308**
CPU-40	68040	25, 33	—	4-16 M	—	1 32-bit, 1 8-bit	4 serial, 1 parallel, 1 SCSI, 1 Ethernet	FLXi	$3,995-$5,995
Sparc CPU-1E	Sparc	20	Weitek	4-16 M	100	2 32-bit	2 serial, 1 SCSI, 1 Ethernet	SBus	$6,995
CPU-30	68030	20, 25	68882	4-16 M	100	1 32-bit	4 serial, 1 RS-232 3 RS-232/422/485	—	$4,490

Model	CPU	CPU clock speed (MHz)	Math coprocessor	Memory (bytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/ interboard expansion	Price
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General Micro Systems 4740 Brooks St, Montclair, CA 91763 (714) 625-5475									**Circle 309**
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GMS V36	68030	16, 40	optional	2-8 M	80	—	1 Ethernet, 1 SCSI, 8 RS-232/422	local mini-SAMbus	$1,798-$2,395
V07/V17/47	68020/30/40	16, 50	optional	2-8 M	20	—	2 RS-232	VSB optional, SAMbus	$1,271-$1,695
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HK80/V960E	80960	33	—	2-8 M	70	4 32-bit	1 Ethernet, 1 SCSI, 4 serial, 1 parallel	VSB	$3,995-$5,795
HK68/V30XE	68030	33	68882	4-16 M	70	4 32-bit	1 Ethernet, 1 SCSI, 2 serial, 1 parallel	—	$4,395-$7,995
HK68/V3F	68030	33	68882	2-8 M	70	—	2 serial	VSB, Corebus	$3,495-$5,295
HK68/V4F	68040	50	in CPU	2-8 M	70	—	2 serial	VSB, Corebus	$4,795-$6,595
Ironics 798 Cascadilla St, Ithaca, NY 14850 (607) 277-4060									**Circle 312**
IV-3234	68EC030	20	68882	1-4 M	—	32 32-bit	16 serial	daughterboard	—
IV-3206	68030	25, 50	68882	4-16 M	—	—	2 serial, 1 SCSI	daughterboard	$4,650
IV-3207	68040	25	in CPU	4-16 M	—	—	4 serial, 1 SCSI, 1 Ethernet	daughterboard	—
IV-SPRC-25A	Sparc/Cypress	25	CY7C605	4-16 M	—	—	2 serial	Mbus, VSB	$6,995
IV-9001	AM29000	25	AM29027	2-8 M	—	—	2 serial	daughterboard, VSB	$5,995
Logical Design Group 6301 Chapel Hill Rd, Raleigh, NC 27607 (919) 851-1101									**Circle 313**
VME-0486/XPS	80486	25, 33	—	1-16 M	80	4 8-bit, 4 16-bit	2 serial, 1 parallel, 1 keyboard	P2/AT	—
VME-RVX1	RTVAX300	16	—	1-16 M	80	1 32-bit	2 serial, 1 SCSI, 1 Ethernet	VSB	$3,800
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 231-8000									**Circle 314**
MD-CPU330	68030	25	optional	1-8 M	—	1 32-bit	1 EIA-232 1 RS-232/422/485	Dbus	$2,295
MD-CPU320	68020	16, 25, 33	optional	1-8 M	—	1 32-bit	1 EIA-232, 1 RS-232/422/485	Dbus	$1,895

PRODUCT FOCUS/VME CPU boards

Model	CPU	CPU clock speed (MHz)	Math coprocessor	Memory (bytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/ interboard expansion	Price
Micro Industries 8399 Greenmeadow Dr N, Westerville, OH 43081 (614) 895-0404									**Circle 315**
PG960CA	80960 CA	33	—	1-4 M	—	4 32-bit	1 serial	OME	$2,495
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (214) 446-2664									**Circle 316**
MZ 7132	68030	25	68882	16 M	80	—	2 RS-232, 1 serial	VSB optional	$3,995
MZ 7170	Sparc	20	Weitek	1 M	35	—	2 RS-232, 1 serial	—	$5,995
MZ 8134	68030	25	—	4 M	80	—	2 RS-232, 1 serial	MXbus	$1,995
Motorola Computer Group, Technical Systems Div 2900 S Diablo Way, Tempe, AZ 85282 (602) 438-3500									**Circle 317**
MVME133XT	68020	12.5, 16.7, 20	68882	1-4 M	100	—	3 RS-232C	—	$1,865
MVME141-3	68030	33, 50	68882	32 k	—	—	2 RS-232C	VSB	$9,995
MVME165	68040	25	in CPU	4 M	60	—	2 RS-232C	VSB	$3,995
MVME187	88100	25	—	4-32 M	80	3 32-bit	parallel, serial SCSI, Ethernet	—	$7,000
MVME188QP-1	88100	25	in CPU	16 M	80	—	2 RS-232C	—	$11,495
Oettle & Reichler Sieglindenstr 19 1/2, D8900 Augsburg 1, Germany (800) 543-3830									**Circle 318**
VCPU20	68020	16, 25, 33	optional	2-8 M	100	—	2 RS-232/422/485	VLX bus, daughtercards	$2,029
Omnibyte 245 W Roosevelt Rd, West Chicago, IL 60185 (708) 231-6880									**Circle 319**
OB68K/VSBC20	68020	16, 25, 33	68882	4 M	80	—	2 RS-232C, 2 parallel	mezzanine	$2,395
OB68K/VME40	68040	25, 33	in CPU	256 k	20	—	2 RS-232C, 2 parallel	mezzanine	$2,995
OB/ACP-VR3000	MIPS R3000	25	R3010	32 M	800	—	1 RS-232C	—	$5,795
PEP Modular Computers 600 N Bell Ave, Carnegie, PA 15106 (800) 228-1737									**Circle 320**
VM-20	68020	16.7, 25	68881/2	1-8 M	100	—	2 RS-232C	—	$1,725-$4,000
VMPM68KD	68030	16.7, 25	68881/2	1-3 M	100	—	2 RS-232C	custom bus	$2,700-$4,800
VM-40	68040	25	—	4-32 M	100	—	2 RS-232C	custom bus, mezzanine boards	$4,500-$6,000
Performance Semiconductor 610 E Weddell Dr, Sunnyvale, CA 94089 (408) 734-9000									**Circle 321**
PV3400	PR3400	25, 33	in CPU	4-16 M	80	3 32-bit	2 RS-232C, 1 SCSI	mezzanine	$9,995-$11,695
PV1750AE256	PACE1750AE	30, 40	in CPU	256 k	25, 35	—	2 RS-232C	—	$16,620-$20,950
PV1750A256	PACE1750A	30, 40	in CPU	256 k	25, 35, 45	—	2 RS-232C	—	$12,000-$16,000
Performance Technologies 435 W Commercial St, East Rochester, NY 14445 (716) 586-6727									**Circle 322**
PT-VME140	68030	25	—	4 M	40	2 32-, 64-bit	2 serial	PTI E-PAK/E-Board	$3,995
PT-VME118/120 PT-VME130	68020/30	12.5, 16.7, 25	68881/2	1-2 M	80	—	1 serial	PTI E-PAK/E-Board	$1,595

Model	CPU	CPU clock speed (MHz)	Math coprocessor	Memory (bytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/ interboard expansion	Price
RadiSys 19545 NW Von Neumann Dr, Beaverton, OR 97006 (800) 950-0044									**Circle 323**
EPC-4	80386	25	80387	4-16 M	80	4 16-bit	2 serial, 1 parallel	EXMbus	$5,930
EPC-5	80486	25, 33	in CPU	4-16 M	80	4 16-bit	2 serial, 1 parallel	EXMbus	$7,495
Radstone Technology 20 Craig Rd, Montvale, NJ 07645 (800) 368-2738									**Circle 324**
68-41/42	68020/40	40/20	in CPU	36 M	80	4 or 5 32-bit	4 RS-232/422/485	VSB, APEX	$6,495-$6,995
68-33	68030	50	68882	5 M	30	2 32-bit	2 RS-232/422	VSB, APEX	$3,220
CPU-20	68020	20	68882	4 M	40	2 32-bit	2 RS-232	—	$6,530
CPU-3A	68030	20, 25, 33	68882	4 M	25	2 32-bit	2 RS423	VSB	$7,300
SBE 2400 Bisso Ln, Concord, CA 94520 (415) 680-7722									**Circle 325**
VPU-25	68020	20, 25	68882	1-4 M	160, 200	2 IP modules	2 multiprotocol	—	$1,380
VPU-30	68030	20, 25	68882	1-8 M	160, 200	—	2 multiprotocol	SCSI	$1,950
VPU-31	68030	20, 25	68882	4-8 M	160, 200	—	2 multiprotocol	VSB	$1,940
Simpact Associates 9210 Sky Park Ct, San Diego, CA 92123 (800) 488-4188									**Circle 326**
ICP6000/9000	68020	16	—	1 M	80	32 8-bit	4 to 16 serial	mezzanine	$3,250
Tadpole Technology 8310 Capital of TX Hwy, Suite 375, Austin, TX 78731 (512) 338-4221									**Circle 327**
TP881V	88100 (up to 8)	20, 25	—	8-128 M	—	2 32-bit SCSI, 1 32-bit Ethernet	2 SCSI, 1 Ethernet, 4 serial	VSB optional	—
TP32V	66030	16, 33	68881/2	4-8 M	—	4	1 SCSI, 1 floppy, 1 Ethernet, 4 serial	—	—
TP960V	80960 CA	16, 33	—	2-16 M	—	4 32-bit	1 SCSI, 1 Ethernet, 2 RS-232	DRAM on mezzanine	—
TP887V	88100 (up to 4)	20, 33	—	16-64 M	—	3 32-bit	2 SCSI, 1 Ethernet, 2 serial	custom bus	—
TP40/41V	68040	25, 33	—	2-32 M	—	—	1 Ethernet, 1 SCSI/VSB, 2 serial	—	—
Themis Computer 6681 Owens Dr, Pleasanton, CA 94588 (415) 734-0870									**Circle 328**
132/133	68030	20, 25	68882	1-16 M	—	Ethernet DMA	2 RS-232C, 1 Centronics	exp. modules, VSB	$3,380-$3,620
130	68030	20, 25	68882	1-16 M	—	—	4 RS-232C	exp. modules, VSB	$2,765
143	68040	25, 33	in CPU	2-8 M	80	Ethernet DMA	2 RS-232, 1 Centronics	exp. modules, VSB	$5,950
VME 538A Valley Way, Milpitas, CA 95035 (408) 946-3833									**Circle 329**
V401	RTX2000	20	—	128 k	55	—	2 serial, 1 parallel	—	$1,895
Xycom 750 N Maple Rd, Saline, MI 48176 (800) 289-9266									**Circle 330**
XVME-602	68020	16	68681	256 k	150	—	2 RS-232	custom bus	$1,650
XVME-683	80386	20, 25	80387 or Weitek	1-4 M	100	—	2 RS-232, 1 parallel, 1 SA450, SCSI	PC/AT bus	$5,150-$6,150

COMPUTERS AND SUBSYSTEMS

other bus interface is the 32-bit VSB that offloads the data traffic from the main VMEbus. The VSB has a complete 32-bit multimaster interface and its own DMA controller.

Memory, ASIC solutions

While high-performance microprocessors have added new problems to CPU board designs, advances in other areas, such as memory and ASICs, are providing solutions. "People want more and more on-board memory and I/O on the CPU board itself," says Fred Rehhausser, vice-president of operations at Force Computers (Campbell, CA). "With the memory on-board, more and more of the programs and bits and pieces of the programs and application code tend to be local, thus eliminating bus traffic and avoiding tying up bus bandwidth."

And thanks to the availability of 1- and 4-Mbit DRAMs, board designers can now cram a lot of memory on-board. This is a substantial increase in the amount of memory that can be accessed locally by the CPU's main processor. At the same time an ever-increasing use of ASICs helps board designers pack more I/O functions onto a single-board computer.

Force's 68040-based board, the CPU-40, uses the company-designed VME interface chip, the FGA002. Because the FGA002 has its own on-chip DMA, it can mediate a substantial amount of DMA between I/O and memory without involving the 68040.

The CPU-40 is the first of Force's products to offer its newly developed I/O mezzanine interface. Called FLXi, this interface provides a 32-bit address and datapath to attached Eagle daughtercards. The first daughtercards offer SCSI, Ethernet and floppy functions. Additional Eagle modules will provide VSB and Ethernet.

While offloading the main processor is important, it's not the only consideration in maximizing a CPU board's performance. Jerry Gipper, product manager of boards and engines at Motorola's Microcomputer Group (Tempe, AZ), touts an advanced memory array as the key to optimum 68040 performance. The MVME165, Motorola's 68040-based VME CPU, features a quad-memory architecture that takes advantage of the 040's cache-burst mode. Unlike more-conventional single- or dual-bank memory architectures, the MVME165 has a four-bank, four-way interleaved memory array where each bank is 32 bits wide. With four banks of memory the processor can access the first bank in four cycles and then access each of the next three banks in one cycle each. While other vendors offer quad-memory architecture, the MVME165 provides the fastest first accesses, Motorola claims.

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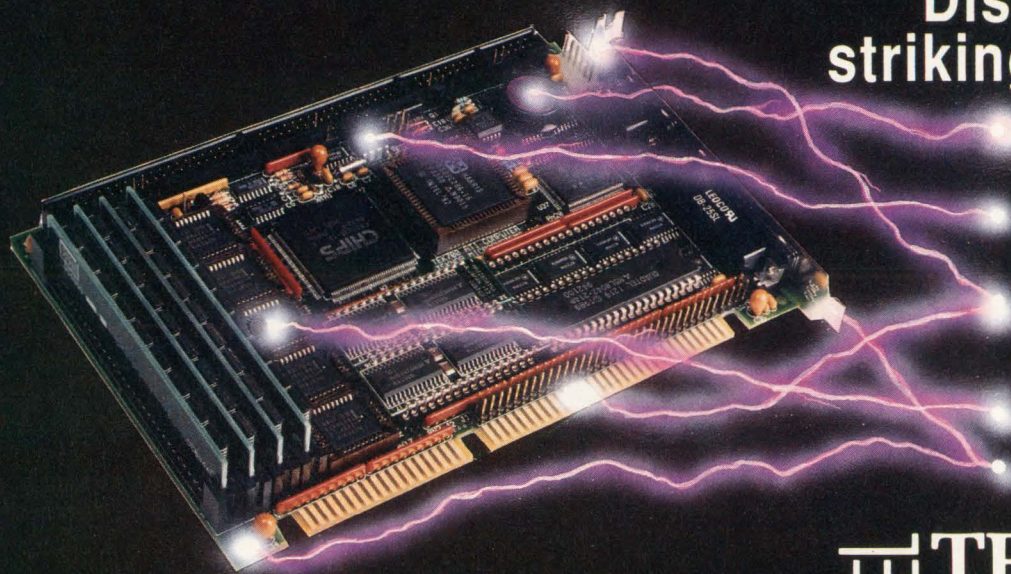

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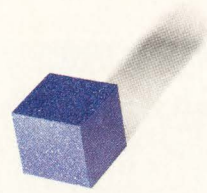

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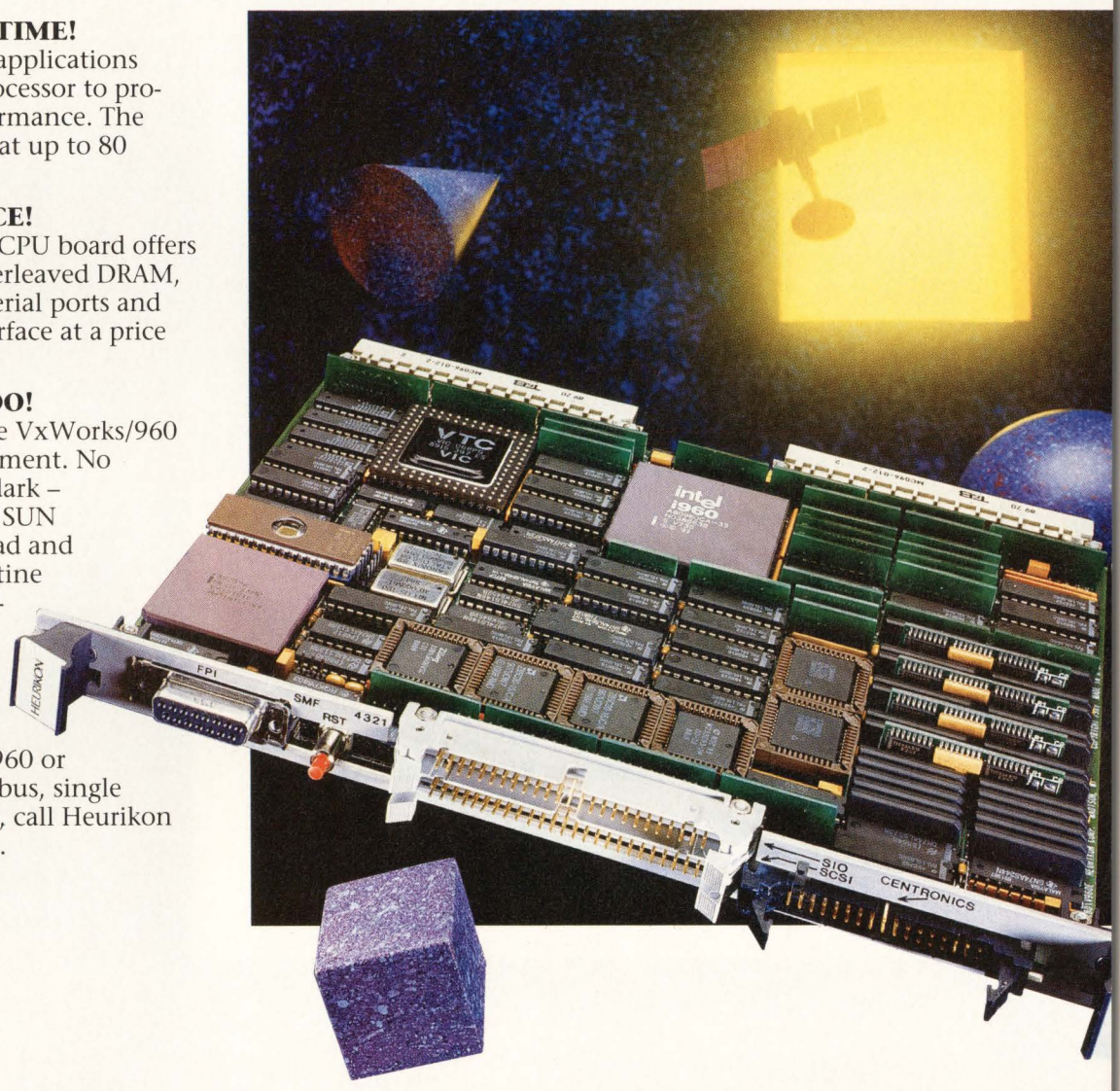

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VM40	68040	20	50	4/8/16/32/ DRAM	Ext.	1	●	2	EEPROM LXB	5 – 8	-40 to +85
VM20	68020/68882	4	16/25	1/2/4/8 DRAM	Ext.	2	●	2		4 – 6	-55 to +125
VMPM 68KD	68030/68882	6	16/25	0.5–3 SRAM	Ext. or Battery	0,5	●	2		10 – 12	-55 to +125
VMPM 68KC-2	68020/68882	4	12/16/25	0.5–3 SRAM	Ext. or Battery	0,5	●	2		9 – 11	-55 to +125
VSBC-1	68HC000	1	12/16	0.1–1 SRAM	Ext. or Battery	0,5	●	2	SCSI	4	-40 to +85
VSBC-2	68HC000	1	16	0.1–1 SRAM	Ext. or Battery	1	●	6		2	-55 to +125
VSBC-3	68HC000	1	16	0.1–1 SRAM	Ext. or Battery	1	●	4	20 x TTL	3	-55 to +125

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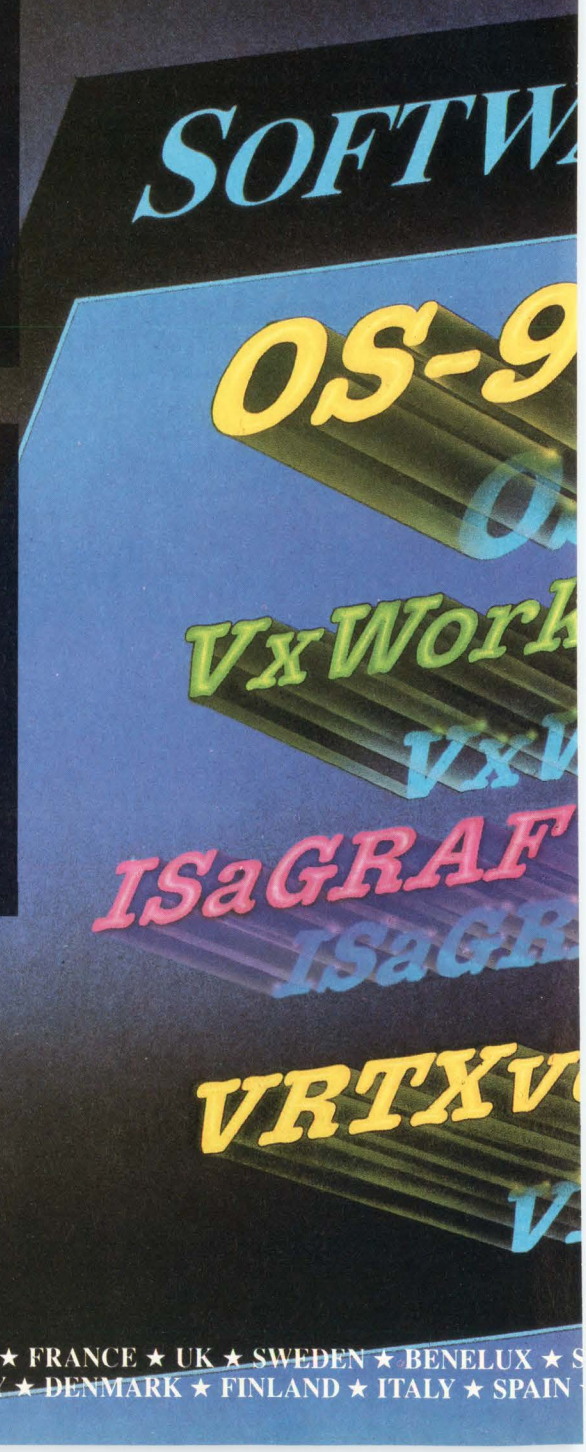

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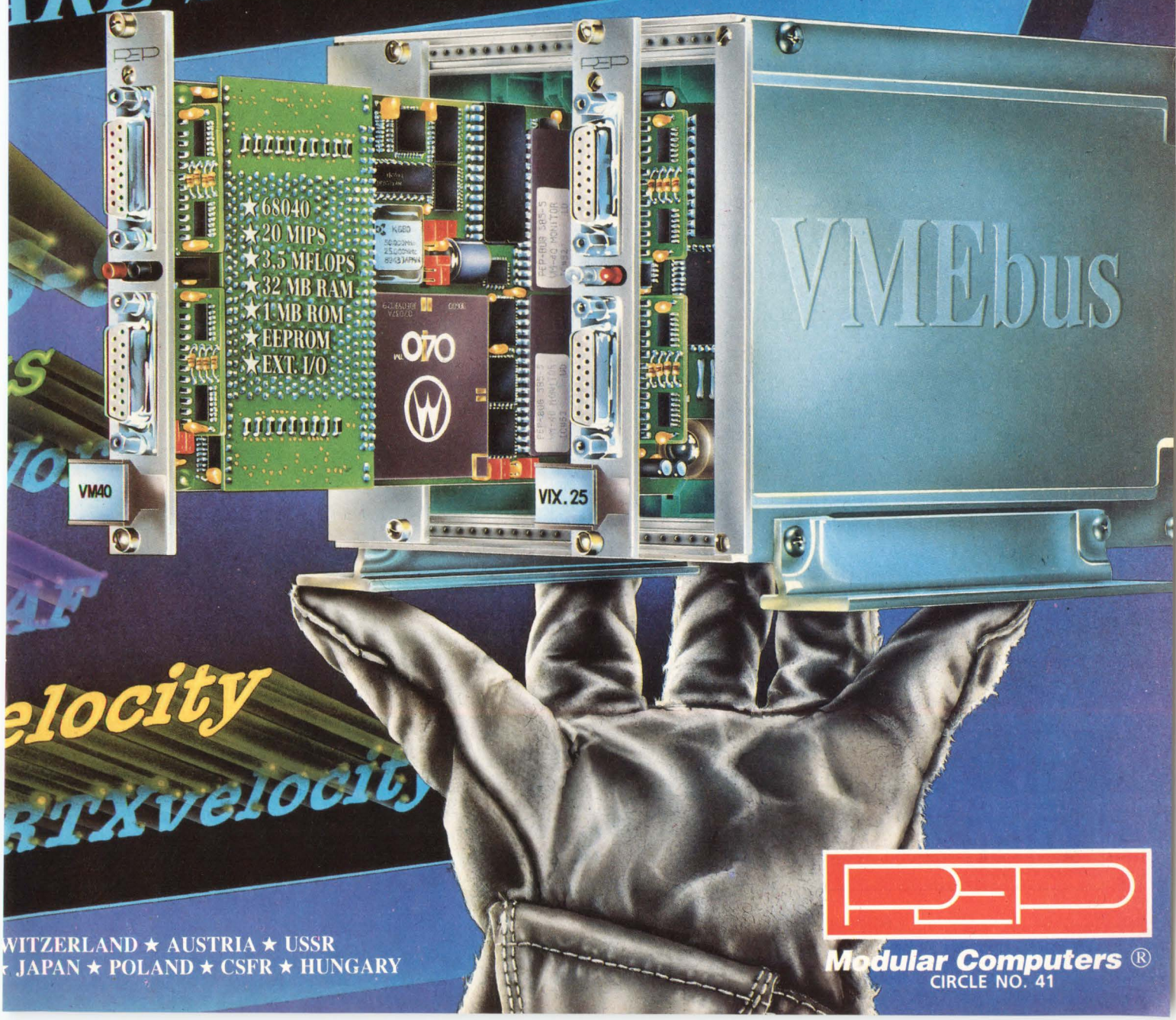

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COMPUTERS AND SUBSYSTEMS

Available with 4 to 16 Mbytes of DRAM, the MVME165 also extensively uses ASICs to reduce the number of components and provide a degree of customization. Besides the memory controller, both the programmable VME and the VSB interface are implemented in ASICs.

Expanding with mezzanines

Although more than a dozen manufacturers have developed their own mezzanine buses, philosophies vary regarding the role of these buses. Some see them as an alternate datapath between boards in a system, while others see them as a way to extend on-board resources. A third view sees mezzanine buses as a gateway to other areas of processing such as graphics or something application-specific.

The 68040-based HK68/V4F board from Heurikon offers a mezzanine bus that's an integral part of its architecture. The board incorporates Corebus, a high-performance mezzanine bus that supports 200-Mbyte/s bus transfers. The strategy of Corebus is to provide on the main base board a minimal set of options common to a broad range of applications. Corebus modules can then be attached to provide the additional functions required including SCSI, Ethernet, serial I/O, memory, and graphics.

If more than 8 Mbytes of main on-board memory are required, a VSB interface accommodates up to 960 Mbytes of off-board memory.

RISC invades VMEbus

While 680X0-based boards dominate the VME CPU market, the appeal of RISC is having an increasing impact. Several VME CPU board manufacturers, both old and new, are offering products based on the RISC processor. The chips used include the Intel 960, the MIPS R3000 and the Motorola 88000 and 88100. These board designs require a more substantial cache than CPU boards based on CISC processors, manufacturers say.

The MVME187 is the latest RISC-based single-board computer from Motorola. Based on the 88000 processor, the MVME187 operates at 25 MHz, providing 32 Mips performance. For a more detailed look at this board, see "Single-board RISC computer puts it all together," p 116.

Another RISC-based VME CPU card, the PaceRunner/3400, from Performance Semiconductor heralds the company's first foray into the commercial board business. Delivering up to 28 VAX Mips performance, the PaceRunner/3400 is based on Performance's own implementation of the MIPS RISC architecture—an integrated RISC CPU/floating-point unit chip set, available with operating speeds of 25 or 33 MHz. ■

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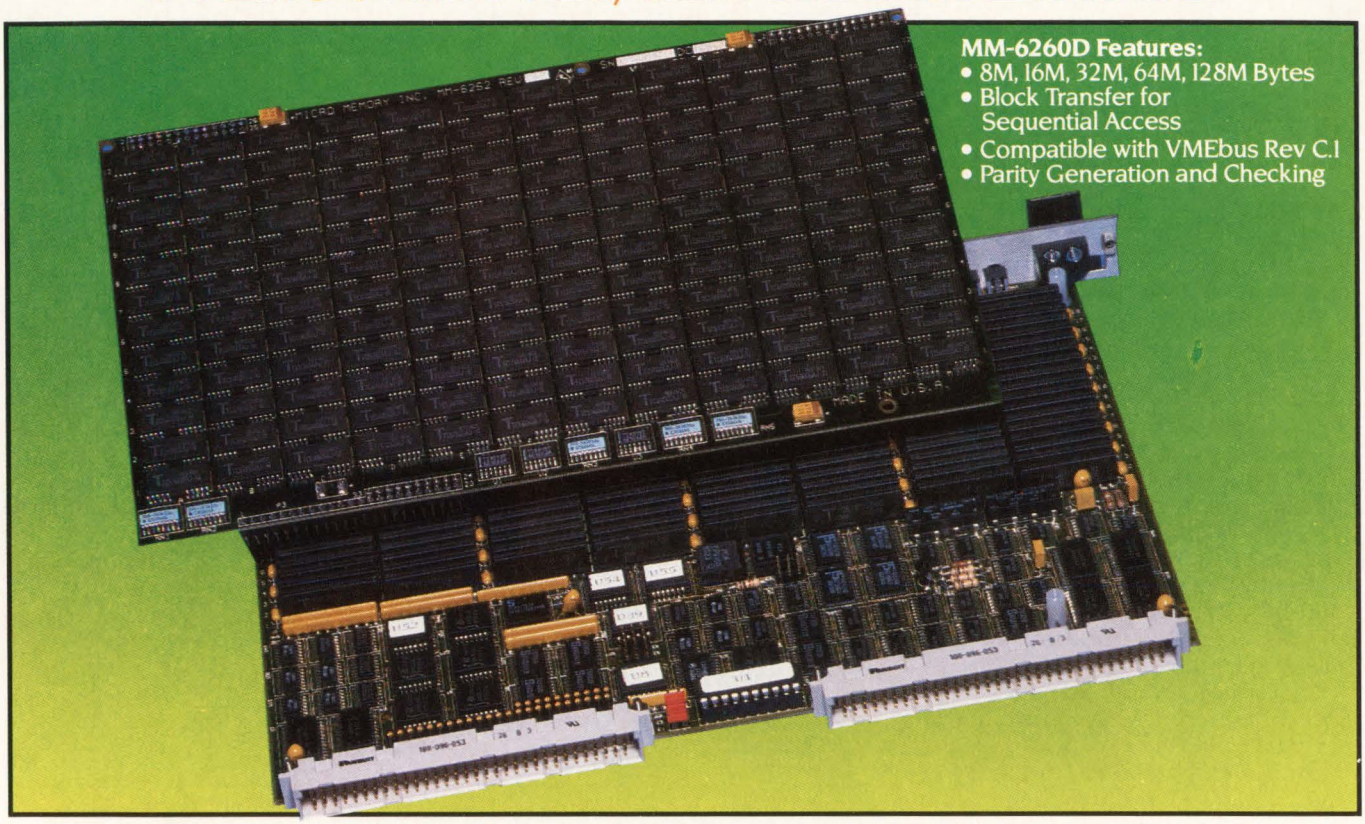

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MM-6326D	8M - 64M	125/75	5.5	Parity, Dual-Port, VME/VSB, UAT, BLT
MM-6320D	4M - 16M	275/200	4.8	Parity, Dual-Port, VME/VSB, UAT, BLT
MM-6316D	4M - 16M	275/220	4.8	Parity, Dual-Port, VME/VSB, UAT, BLT
MM-6260D	8M - 128M	120/90	3.8	Parity, UAT, BLT, Page, A32/A24, D32/D16/D8
MM-6240D	2M - 16M	250/130	4.5	Error Correction, 32-bit CACHE, UAT, BLT
MM-6230D	4M - 16M	240/175	2.9	Parity, Fast Write, UAT, BLT
MM-6220D	2M - 16M	240/175	3.8	Parity, 32-bit CACHE, CACHE Hits = 75 nsec
MM-6216D	4M - 16M	240/175	3.0	Parity, Fast Write, UAT, BLT
MM-6202D	1M - 4M	145/130	2.9	Parity, UAT, BLT, Page

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MM-6704C	512K - 4M	150/100	2 yrs./2 wks.	2.1	RTC, UAT, BLT, A32/D32
MM-6702C	512K - 8M	125/125	3 yrs./4 wks.	1.7	UAT, BLT, A32/D32
MM-6700D	64K - 1M	150/150	4 yrs./8 wks.	1.0	A32/D32
MM-6500C	32K - 512K	200/200	5 yrs./12 wks.	1.1	RTC, A24/D16

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COMPUTERS AND SUBSYSTEMS

Single-board RISC computer puts it all together

A VME single-board computer based on the Motorola 88000 RISC processor extensively uses ASIC technology to incorporate serial and parallel I/O, SCSI interface, Ethernet LAN interface, a large cache, ROM/EPROM, timers, and even a time-of-day clock. The MVME187, developed by the Motorola Computer Group, includes features that previously required five separate boards. In addition to ASIC technology, exclusive use of CMOS electronics has kept the board's power consumption down to 20 W. The board's target markets include computer OEMs, process control, simulation, and electronic publishing.

The MVME187 contains an M88100 microprocessor running at 25 MHz and two M88200 cache MMUs, each handling 16 kbytes of instruction and data cache. The basic 32 kbytes of cache are expandable to 128 kbytes. The board also provides 4 to 32 Mbytes of DRAM main memory, which is field-expandable by means of a mezzanine board. Main memory is organized in four banks with four-way interleaving. Four 44-pin sockets can accommodate up to 2 Mbytes of on-board ROM or EPROM for various applications such as real-time kernels and embedded ROM-based applications software.

Motorola has optimized the board design to off-load the CPU and increase overall performance by reducing unnecessary bus traffic. Based on Dhrystone 2.1 measurements, the MVME187 running at 25 MHz is capable of 32 Mips.

ASIC, VLSI investment

The company says it has invested more than $10 million in developing an all-new set of ASICs and VLSI controllers for memory control, networking, SCSI control, serial and parallel communications, and VMEbus control.

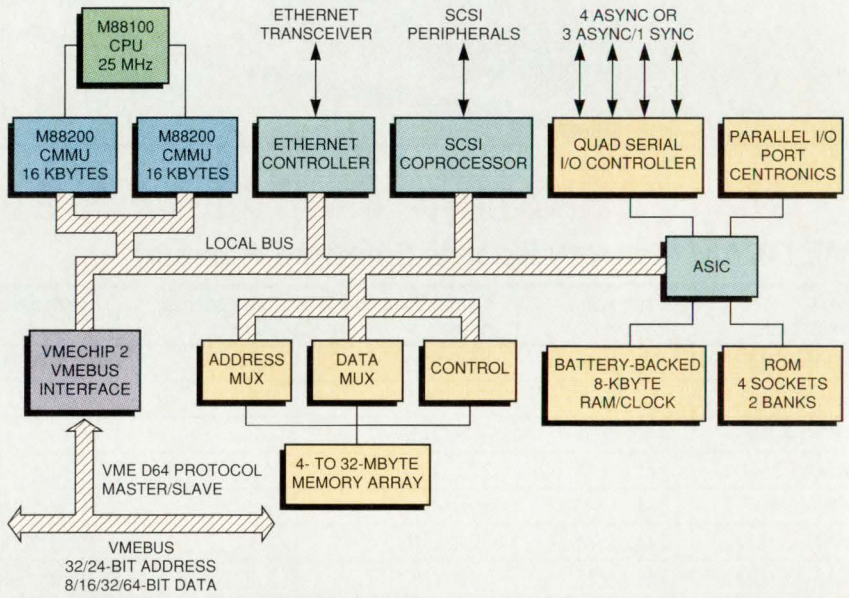
The biggest ASIC on the board, a 499-pin VMEchip 2 bus interface chip, provides both a master and a slave interface with 32 or 24 bits of address and 64, 32, 16, or 8 bits of data. The VMEchip 2 incorporates a VMEbus map decoder that eliminates decoder jumpers. It also has a 32-bit DMA controller that allows block transfers across the VMEbus and burst transfers over the local bus. Using VME D64 protocol boosts VMEbus bandwidth to a full 40 Mbytes/s. In addition, the VMEchip 2 provides a seven-level VMEbus interrupter with status/ID register, VMEbus system controller with programmable bus timer and global control and status registers, as well as a software-programmable interrupt handler.

ASICs and VLSI chips provide Ethernet and X.25 synchronous communication with 32-bit DMA capability on the local bus. Data is transferred directly to on-board DRAM, eliminating processor copies from buffers to DRAM. The LAN section supports protocols including Transmission Control Protocol/Internet Protocol, network file system, synchronous data link control, and high-level data-link control. The SCSI coprocessor supports 32-bit DMA burst capability on the local bus and supports all SCSI peripherals. The SCSI driver firmware can be updated via software so that the SCSI device library can keep up with new SCSI peripherals.

The MVME187 will be provided with a full range of software to include Unix System V/88, Release 3.2. Motorola will supply the VMEexec real-time executive for target and host as well as on-board monitor and debugger firmware. The board is compatible with the over 1,000 applications developed for Motorola's higher- and lower-end multiboard RISC platforms, the MVME188 and MVME181, respectively. It's also compliant with the binary and object compatibility standards defined by the 88Open Consortium.

The MVME187 will ship in sample quantities this May to key customers who are expected to thoroughly exercise it for any remaining bugs. The board will also ship at that time to independent software vendors, such as real-time kernel suppliers, who will be adapting their kernels and software development tools. Production shipment is scheduled for October. Single-unit price will be $7,000. —*By Tom Williams*

MVME187 ARCHITECTURE



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Circle 351

INTEGRATED CIRCUITS

BiCMOS arrays up to 150,000 gates offer compiled memory

Seven base arrays in 0.8-µm triple-layer-metal BiCMOS from Texas Instruments have from over 10,000 to over 100,000 usable gates. The TGB1000 base arrays integrate CMOS and BiCMOS internal cells, optimizing high-speed path requirements. The I/O structure of the arrays allows mixing of ECL and TTL/CMOS interface levels. The TGB1000 libraries support designs using compiled SRAMs and ROMs as well as datapath elements.

The TGB1000 gate arrays range in density from a 13,000-gate base array with 10,000 usable gates to a 150,000-gate base array with 112,000 usable gates. Advanced metallization schemes let designers use 75 percent of the available gates. Up to 320 signal pins are supported in specially designed packaging.

With the TGB1000 arrays, TI offers memory and datapath compilers to let users take advantage of the high levels of functional integration possible with submicron BiCMOS. Up to 128 kbits of SRAM and 256 kbits of ROM can be compiled. Typical on-chip SRAM access time is 3 to 6 ns. Adders, ALUs, barrel shifters, and multipliers can also be compiled.

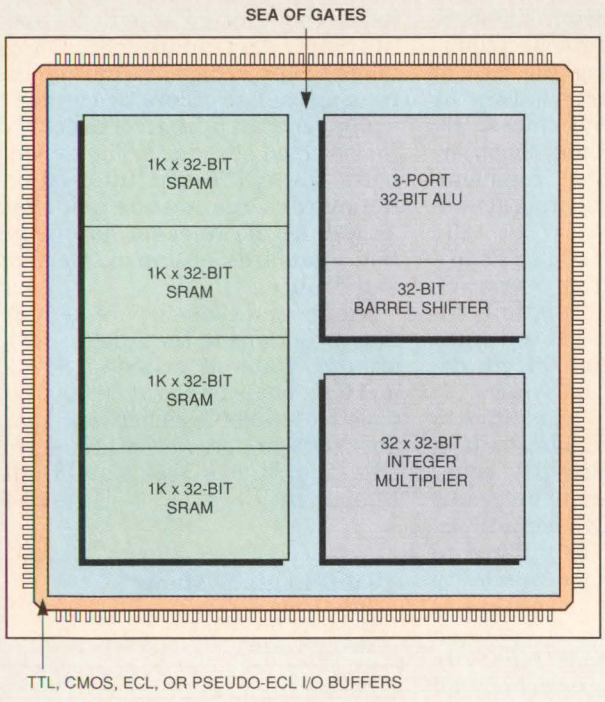
The TGB1000 library offers 61 peripheral macros in four process options: TTL, CMOS, ECL, and pseudo-ECL. Testability macros for Joint Test Action Group implementation are also included in the library.

Typical BiCMOS gate delay in the TGB1000 base arrays is 320 ps; typical CMOS delay is 550 ps. The arrays have a flip-flop toggle frequency of greater than 400 MHz. A maximum I/O frequency of greater than 200 MHz makes the arrays suitable for telecommunication switching applications.

For designing the arrays, TI supports Mentor, Cadence, Synopsys, Valid, and Ikos software tools running on Apollo and Sun. Proprietary software supports power and prelayout delay estimation, rule checking, resistance-capacitance back annotation, and floorplanning.

NRE (nonrecurring engineering expense) charges for the TGB1000 arrays, which are available now, start at $70,000. — *Barbara Tuck*

TGB1000 GATE ARRAYS



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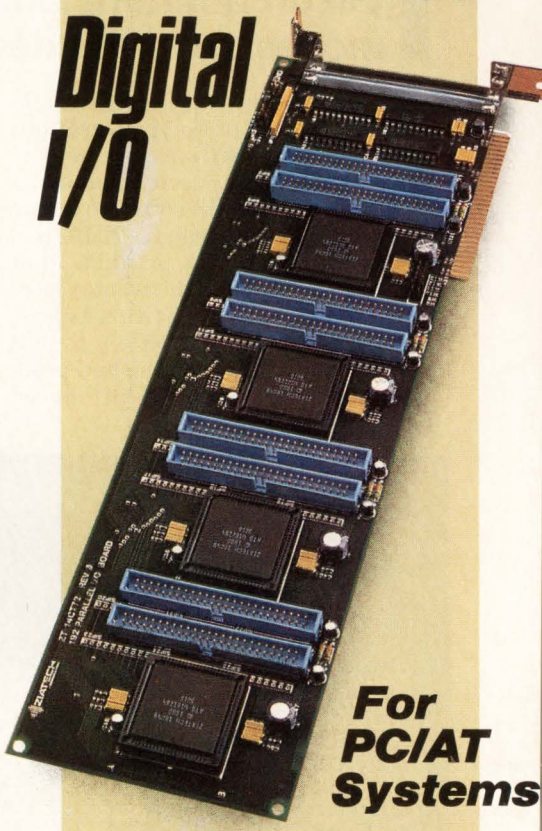

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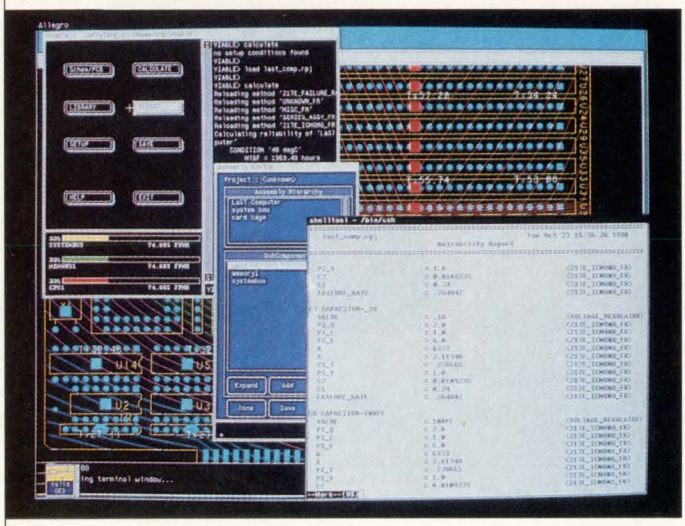
CIRCLE NO. 71

DESIGN AND DEVELOPMENT TOOLS

Circuit board reliability analysis moves up in the design cycle

With time-to-market windows shrinking and costs of prototype iterations growing, many hardware vendors are turning to analysis tools to predict a product's behavior in software before committing to a design. EDA tool vendors are offering products that model many physical characteristics of a design, such as thermal behavior and reliability prediction, so that decisions that affect a finished product's performance can be introduced early in the design cycle.



Add to that list of tools a product from Valid Logic Systems dubbed Viable—a reliability analysis tool that offers both pre- and postlayout support for circuit boards, multiwire boards, hybrids, and multichip modules.

The tool lets users predict the reliability of designs at the component, board and system levels as soon as schematics have been completed and physical packages assigned. Viable derives its predictions from device operating voltage, current, power, temperature, duty cycle, and manufacturing processes. Viable provides mean-time-between-failures predictions, as well as relative and absolute failure rates prior to physical implementation.

Environmental conditions

In addition, the tool can predict reliability across a series of changing temperatures or other environmental conditions, enabling users to perform mission profile analysis in accordance with military standard requirements. Viable can also be used after component placement to further refine reliability predictions based on thermal contours, heat sinks and other considerations.

To eliminate discrepancies that can occur when separate libraries are used for packaging and placement, Viable calculates its predictions from a single library. To ensure data integrity, the tool operates directly from the Valid design database without requiring the use of translators or interfaces. By using the intertool communications capabilities of the Validframe framework, Viable is fully integrated into the Allegro design system.

In addition to Viable's built-in MIL-HDBK-217E reliability equations, engineers can write programs to generate their own equations. These equations can be tailored to meet specific corporate reliability standards or to take advantage of the reliability engineer's hands-on experience with various reliability factors. Equations can model special system reliability requirements such as fans or power cords that are not normally part of the circuit design. In addition, Viable provides user-programmable report formatting capabilities that enable companies to preserve and transfer specialized reliability information across all of their design projects.

Cals-out package

In conjunction with Viable, Valid has developed Cals-out, an integrated package that automatically generates release and process documentation to meet Computer-Aided Acquisition and Logistics Support (CALS) documentation standards. With Cals-out, users can produce assembly drawings, fabrication drawings and other documentation in standard drawing formats, and deliver data files and documentation electronically in the International Graphics Exchange Specification (IGES) 4.0 format. IGES is the interchange standard for CAD vector graphics, including the underlying engineering information, and is a required format of the U.S. Department of Defense's CALS initiative.

The Cals-out package lets users select a documentation template at the beginning of the documentation phase in the design process. After selecting a standard, all design documentation is automatically formatted to the selected standard's specifications. Any additional changes made to the design, including engineering change orders, are automatically generated in accordance with the selected standard. The tool supports the ANSI and International Standards Organization guidelines, as well as the relevant documentation standards of Japan, Germany and France.

Viable and Cals-out are available now as options to the Allegro design system. Viable is priced at $12,000 and Cals-out is priced at $6,000. Both tools are available as network-shareable software on workstations from IBM, Sun Microsystems and Digital Equipment Corp. —*Mike Donlin*

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Logic analyzer houses 1-Gsample/s oscilloscope

As clock speeds of today's CMOS and ECL devices increase, designers are troubleshooting problems that they've been able to overlook in the past. Parametric waveform phenomena could sometimes be ignored in slower designs, because there was adequate time for these effects to settle down before the next clock cycle. But with clock rates going beyond 50 MHz, all that has changed. To address these needs, test equipment manufacturers are offering faster oscilloscopes and coupling them with logic analyzers, for an integrated troubleshooting system.

Hewlett-Packard has unveiled its latest addition to this growing number of products with the HP 16532A, a 1-Gsample/s digitizing oscilloscope module for the HP 16500A logic analysis system. According to HP, the system has the speed and accuracy required to troubleshoot and test all CMOS and many ECL-based designs.

The oscilloscope provides a 250-MHz real-time bandwidth, which gives the single-shot capability required for detailed analysis of high-speed CMOS designs, as well as ECL-based designs with 50- to 80-MHz clock rates. In addition, the scope offers 8-bit resolution, which provides users with a complete view of parametric waveform phenomena such as ringing, overshoot, crosstalk, induced noise, and ground bounce.

Time-interval accuracy up

Time-interval accuracy of the HP 16532A is better than ±150 ps, which provides guaranteed timing margins in designs approaching 10 ns. According to HP, the scope's sampling techniques provide approximately 10 times better time-interval accuracy than 2-Gsample/s timing analyzers. The module can handle up to 18 channels at 1 Gsample/s.

When teamed up with the HP 16500A's 1-GHz timing module and 100-MHz state module, the scope can make time-correlated measurements and display them in multiple windows. All of these modules can cross-trigger each other, permitting the designer to trigger on the symptom of a problem with one measurement module while capturing the cause with another. Other features include automatic pulse measurements, autoscale and built-in user calibration.

The HP 16532A oscilloscope module, available now, costs $9,000.

— Mike Donlin

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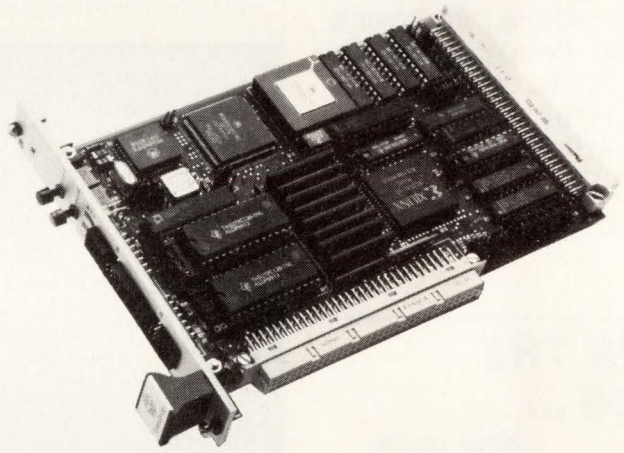

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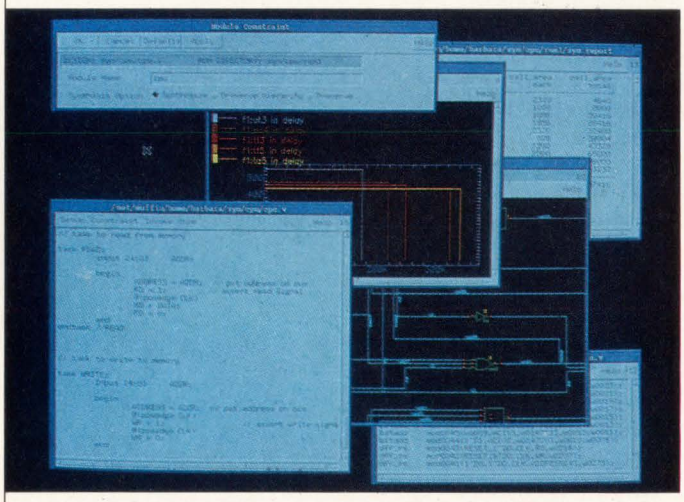
DESIGN AND DEVELOPMENT TOOLS

Cadence integrates synthesis for front- to back-end design

Synthesis technology developed by Cadence Design Systems has been integrated into its Amadeus System Design Series and Opus IC Design Series, both based on Design Framework II. A two-product solution, the Cadence synthesis and optimization software includes the Improvisor and Optivisor, both available now on Unix-based workstations. The Improvisor synthesizes mixed-level hardware description language inputs to gate-level descriptions and explores design alternatives. The Optivisor, which requires at least one Improvisor, provides optimization and technology-mapping capabilities.



As an integral part of a framework-based system, the Verilog-based mixed-level synthesis solution offers IC, ASIC and systems designers certain advantages. Top on the list is the use of a single library for simulation and synthesis, as well as for timing analysis and fault simulation.

Next, Cadence synthesis, tightly integrated with analysis and physical layout, allows for the forward and backward transfer of design data, facilitating resynthesis if necessary. Moreover, Cadence claims that its software partitions very large designs by recognizing relationships between circuit elements and by placing artificial boundaries automatically within the code.

Cadence synthesis technology lets designers input HDL-based designs at multiple levels of abstraction, supporting both Verilog constructs at the register transfer level and schematics at the same time. A common delay calculation capability automates the function of tracking timing constraints consistently through various levels of abstraction as well as between design tasks.

The Improvisor supports technology-independent design and generates trade-off data, based on a range of user-specified timing and area goals, for users to analyze before committing their designs to a custom IC, ASIC or programmable logic device technology. Once a technology has been decided upon, designers direct the Improvisor results to the optimization and mapping capabilities of the Optivisor for implementation.

The Optivisor accepts gate-level descriptions and, guided by user constraints, finds an optimal design implementation in a given library. The tool's partitioning techniques, based on advanced timing optimization algorithms, are claimed to preserve optimization opportunities based on recognized relationships between circuit elements.

Users can expect Cadence synthesis tools to support a higher level of abstraction in the second half of this year. Enhancements will include support for VHDL and resource allocation. The Improvisor is priced at $15,000, regardless of platform. The Optivisor starts at $35,000.

—By Barbara Tuck

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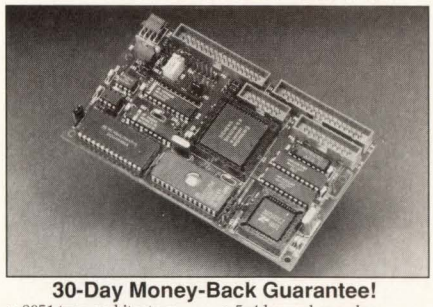

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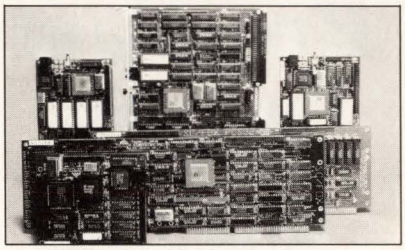

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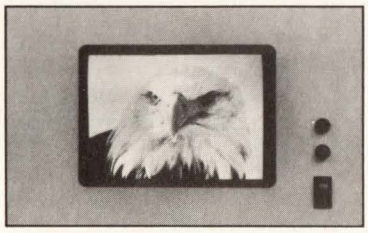

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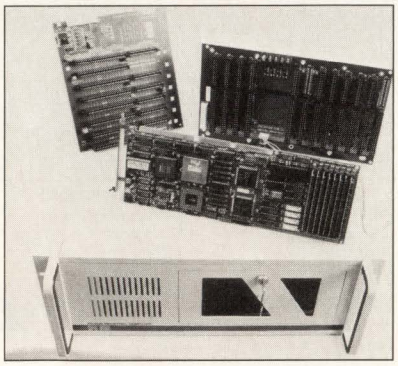

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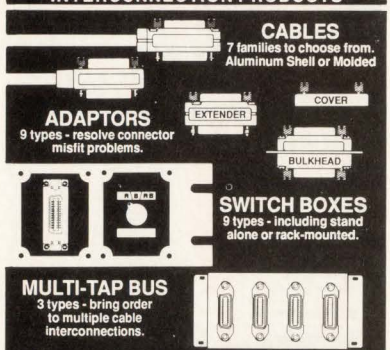

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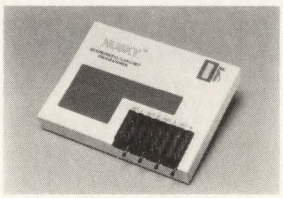

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March 1*	Fuzzy logic in embedded control *Tom Williams*	Mixed CMOS, ECL & BiCMOS — *Barbara Tuck* LAN controllers ICs — *Ron Wilson*	VME CPU boards *Jeff Child*
April 1 Electro	PCB layout tools *Mike Donlin*	Communication with standard buses — *Warren Andrews* Designing ASICs for testability — *Barbara Tuck*	Static RAMs *Jeff Child*
May 1* CICC, Comdex	Superfast processors *Ron Wilson*	High-level design languages — *Mike Donlin* Object-oriented programming — *Tom Williams*	Emulators *Jeff Child*
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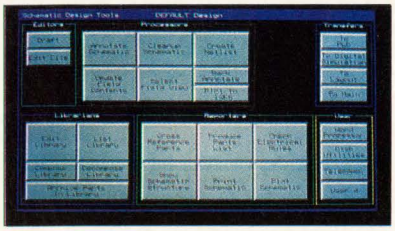

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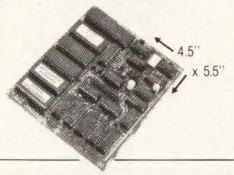

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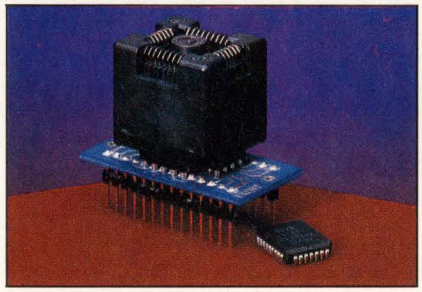

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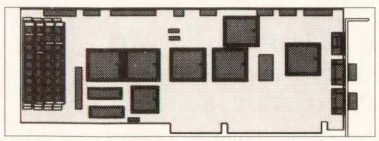

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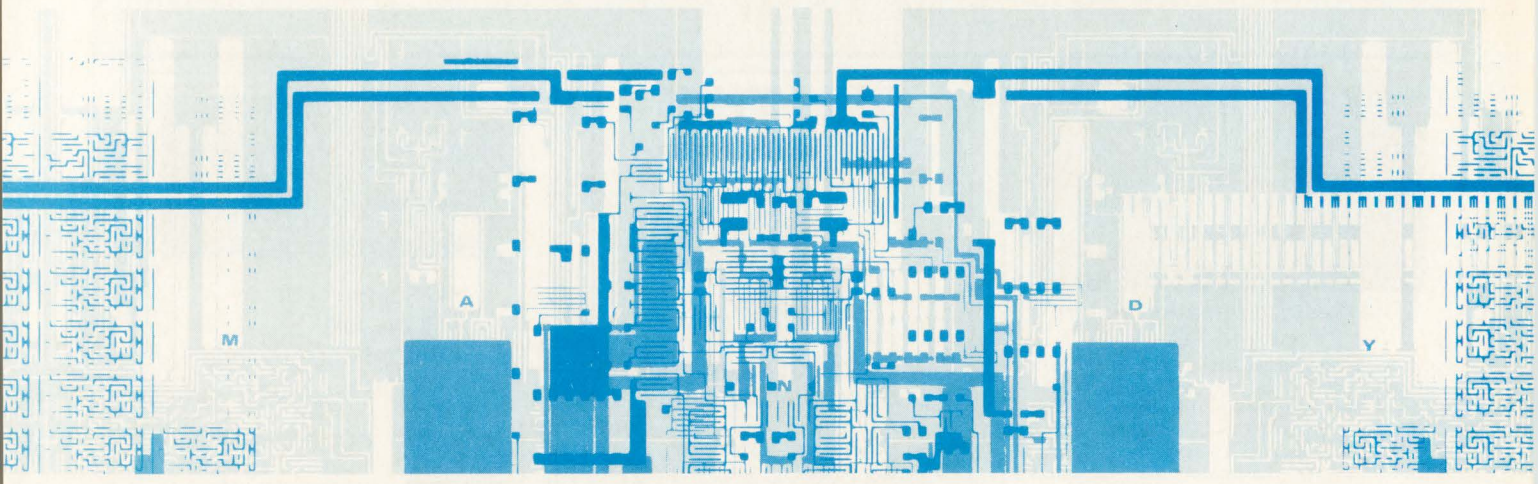

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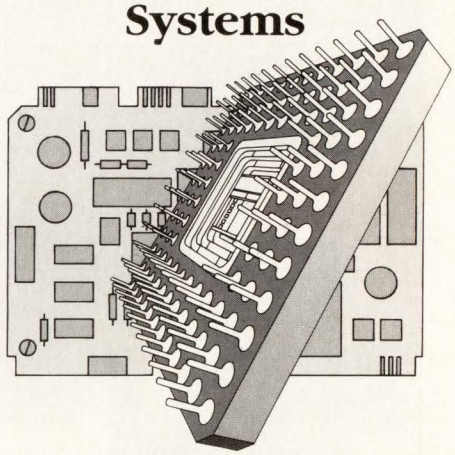

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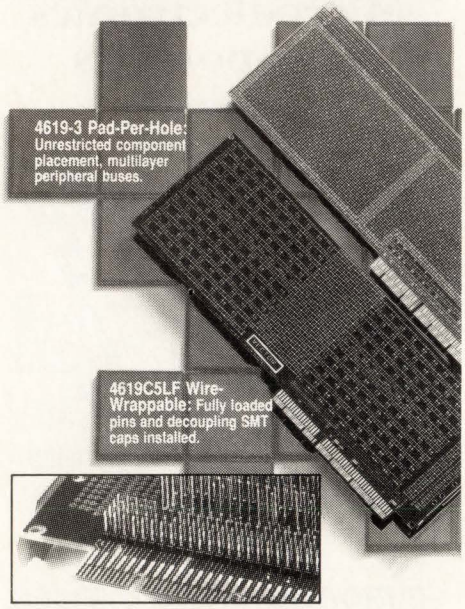

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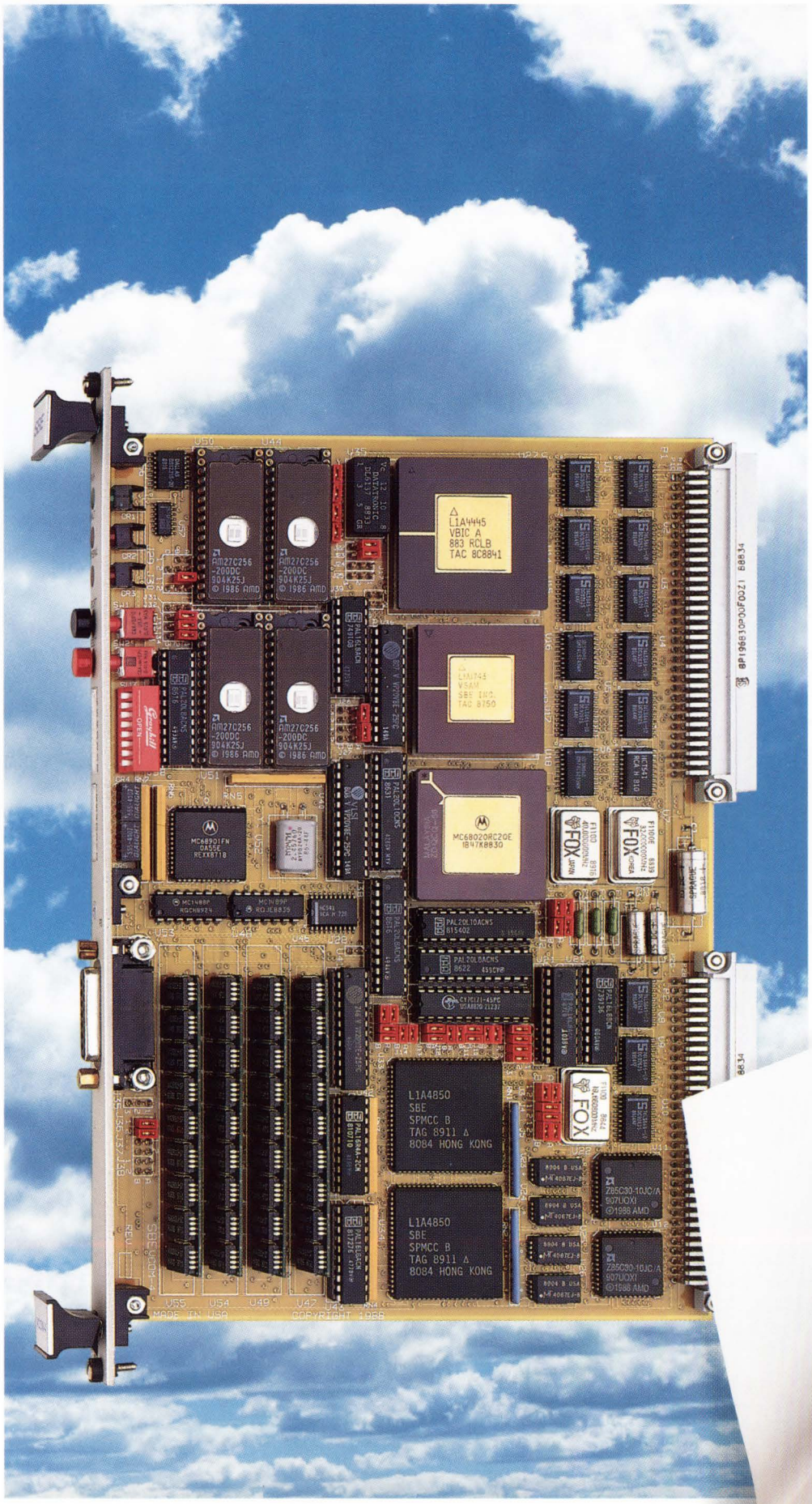

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